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DEVELOPMENT OF A MICROELECTROMECHANICAL SYSTEM FOR SMALL SATELLITE THERMAL CONTROL

by

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14. ABSTRACT

Trends in space technology require future satellites to be smaller and cheaper than their contemporary counterparts. This new direction requires a similar evolution in thermal control. Previous techniques such as heat pipes and conventional radiators have large masses themselves and are not scaleable to fit these smaller designs. Microelectromechanical Systems (MEMS) offer unique advantages in mass and scalability. By coating a satellite with thousands of MEMS devices, thermal control can respond to variations in thermal capacity. This project involved the development of a variable radiator that would control a satelliteŸs temperature by changing the heat conduction between the satellite and a MEMS surface coating. These MEMS devices operate by using a voltage to deflect an emissive surface layer into thermal contact with the structure below. By designing for a voltage of 20 to 24V, these devices can operate on the bus voltage supplied by many satellites produced today. Testing has shown that these devices operated at this desired voltage level. The electromechanical and thermal properties of the device were modeled. These models provided insight into the design dimensions that dominated the voltage and power characteristics as well as the heat flow. The devices were tested for both their thermal and electrostatic properties. The modeling predictions were found to be accurate for the required device voltages. With the insight gained from modeling and testing, a new design was made offering greater thermal performance while maintaining low operating voltages. This design incorporated different materials allowing easier device fabrication and higher wafer yields. It also used different physical dimensions to improve thermal performance. Finally, this project developed the packaging requirements of this device for flight on the MIDSTAR I satellite. The groundwork has been laid for its flight into space in 2006 through a package design specific to this device. The Interface Control Document outlining hardware interfaces, power specifications, and satellite orientation has been completed.

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Abstract

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This project involved the development of a variable radiator that would control a satellite's temperature by changing the heat conduction between the satellite and a MEMS surface coating. These MEMS devices operate by using a voltage to deflect an emissive surface layer into thermal contact with the structure below. By designing for a voltage of 20 to 24V, these devices can operate on the bus voltage supplied by many satellites produced today. Testing has shown that these devices operated at this desired voltage level.

The electromechanical and thermal properties of the device were modeled. These models provided insight into the design dimensions that dominated the voltage and power characteristics as well as the heat flow. The devices were tested for both their thermal and electrostatic properties. The modeling predictions were found to be accurate for the required device voltages. With the insight gained from modeling and testing, a new design was made offering greater thermal performance while maintaining low operating voltages. This design incorporated different materials allowing easier device fabrication and higher wafer yields. It also used different physical dimensions to improve thermal performance.

Finally, this project developed the packaging requirements of this device for flight on the MIDSTAR I satellite. The groundwork has been laid for its flight into space in 2006 through a package design specific to this device. The Interface Control Document outlining hardware interfaces, power specifications, and satellite orientation has been completed.

Keywords: microelectromechanical devices, MEMS, microfabrication, thermal variables control, variable emissivity, SU-8, satellite applications, packaging

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List of Symbols and Acronyms

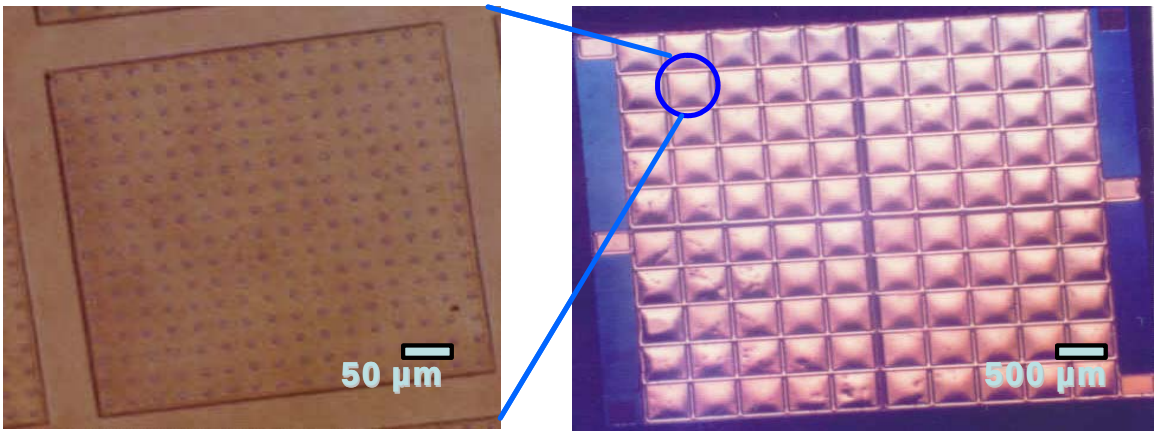
A	Area (m^2)
APL	Johns Hopkins University Applied Physics Laboratory
C_t	Thermal Capacitance (J/K)
C&DH	Command and Data Handling Unit and Central Computer for Satellite
COTS	Commercial Off-the-Shelf
E	Youngs Modulus (Pa)
E_g	Power Generated (W)
ECU	Electronics Control Unit for MEMS Devices
G	Thermal Conductance (W/K)
G_{int}	Thermal Conductance through Package-Chip Interface (W/K)
G_0	Thermal Conductance through Package-Heater Interface (W/K)
G_{var}	Thermal Conductance through Variable Conductivity Layer (W/K)
g_0	Gap Between bridge and Substrate at Zero Bias (m)
g_{int}"	Thermal Conductance through Package-Chip Interface per Unit Area (W/m^2K)
g_0"	Thermal Conductance through Package-Heater Interface per Unit Area (W/m^2K)
g_{var}"	Thermal Conductance through Variable Conductivity Layer per Unit Area (W/m^2K)
h	Height or Thickness of the Layer (m)
ICD	Interface Control Document
IR	Infrared
k	Spring Constant (N/m)
k_{th}	Thermal Conductivity ($W/m \cdot K$)
MEMS	Microelectromechanical Systems
MUMPS	Multi-User MEMS Processes
M	Mass of membrane or bridge, kg
m	milli-, 10^{-3} or meter
$\dot{Q}_0$	Rate of Energy Transfer (W)
q_{in}"	Heat Flux In (W/m^2)
q_{out}"	Heat Flux Out (W/m^2)
ST-5	Space Technology 5 Satellite
T_{Al}	Temperature of Aluminum Package Base (K)
T_{Au}	Temperature of Gold Membrane (K)
T_0	Package Thermal Model: Temperature of Satellite (K) Device Thermal Model: Temperature of Substrate (K)
T_1	Temperature of Gold Membrane (K)
T_{Si}	Temperature of Silicon Substrate (K)

t	Time (s)
VEC	Variable Emissivity Coating
V_{pi}	Pull-in Voltage or Activation Voltage
ε	Emissivity
ε_0	Permittivity of Free Space (F/m)
f_0	Fundamental frequency, Hz
σ	Biaxial Residual Stress (Pa) or Stefan-Boltzmann Constant (W/m^2K^4)
μ	micro-, 10^{-6}
ν	Poisson's ratio

1. Introduction

In the new generation of nano- and pico- satellites, with a total weight of sixty kilograms or less, the need for lightweight thermal control is essential. A lower mass also translates to a smaller thermal capacitance, which is a measure of the thermal energy stored in a structure. This requires a thermal control system with greater flexibility and scalability capable of responding to increased thermal fluctuations. Current control systems such as heaters, thermostats, or heat pipes are large and non-scalable[1], thereby limiting their performance. These larger thermal control devices also require a greater amount of power than future satellites can supply. This project focused on a microelectromechanical system (MEMS) for providing the necessary thermal equilibrium, utilizing voltage control to change the satellite's radiated heat. Integral in this process was the correct design of the device for acceptable levels of heat transfer, structural stability, and space environment survivability. This device also required the proper packaging for control, data output, power supply, and mechanical support. This project employed material, mechanical, and electrical engineering to produce an operational device capable of being launched on the next Naval Academy satellite.

In order to understand the scope of this project, the terms 'device', 'die', 'device array', 'package', and satellite system 'configuration' must be defined. These terms are used to describe the varying size and scope at each level of this project. The physically smallest piece of the project is the MEMS 'device,' shown in Figure 1(a). The device, with dimensions comparable to a pin head, is the primary focus of this project. One single device is controllable, functions independently, and controls thermal radiation through its area.



(a) **(b)**

Figure 1. (a) Picture of MEMS device and (b) MEMS die containing 100 devices.

To improve performance, not just one, but dozens of devices were placed together on a single piece of silicon and controlled by one source. This is referred to as the MEMS 'die,' using the same terminology as is used for semiconductor devices. In this particular project the square die varied in area from 0.25cm^2 to 1 cm^2, or 0.5 cm to 1 cm on a side. This size is the basic unit, and primary focus, for all testing and applications contained in this project. When multiple die are controlled collectively, a device array is produced. This array can vary anywhere from a small number of test structures to the thousands of die that would be necessary to coat an entire satellite exterior. The die contained in the array can be controlled independently or collectively to provide the desired thermal control for any testing or real world application.

In order to utilize these micro- devices in the real world, the array needs mounting specifications and signal interfaces. To accomplish this integration, a 'package' is necessary. The package will provide any structural stability the devices require as well as connection to their control element. For this application the package would consist of a 100 cm^2 mounting platform that would connect mechanically and electronically to the satellite. The electronic

connection would require an additional package internal to the satellite containing all interface-conditioning hardware necessary. The satellite system 'configuration' would include both of these packages to create the overall scope of the project in relation to the satellite platform. Figure 2 shows the packages included in launching the MEMS devices aboard MIDSTAR, as well as the other systems on board the satellite.

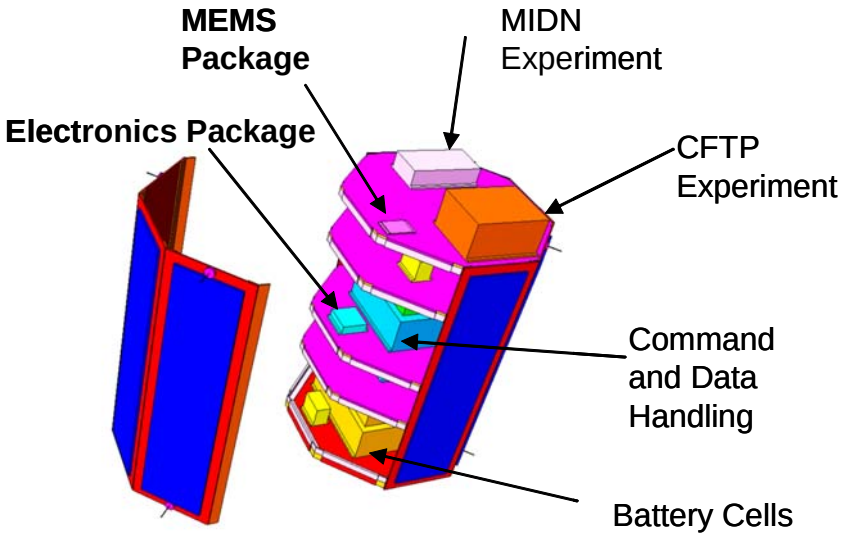


Figure 2. Diagram of MIDSTAR system with both packaging components for this experiment in bold. These packages create the total project configuration.[1] The MIDN and CFTP experiments are other payloads.

Although the focus of this project was initially on packaging the array, greater attention was focused on MEMS device development as it became apparent that a significant device redesign would be required. Packaging remained an important aspect, despite the shift in focus, as the future testing of these devices aboard MIDSTAR I was an important project goal. The package chosen for this device was based on a package developed at the Johns Hopkins University Applied Physics Laboratory (APL) for NASA's ST-5 program, which utilized an

[1] MIDSTAR Structures Page, http://cadigweb.ew.usna.edu/~midstar/index.php?sect=struct

alternative implementation of MEM thermal control. Modifications to the ST-5 design were necessary for this specific application and included a change in voltage supplied to the device, a different interface with the satellite, and a new MEMS test configuration. The devices launched on MIDSTAR I will be those developed by this project.

The project began with setting up both electrostatic and thermal test facilities in order to characterize device performance. After the initial fabrication, the device die were studied using an optical microscope and an optical profiler. Dimensions were measured in order to better predict operation. After collecting the necessary device and die measurements, an electromechanical model was created; this was used to predict the necessary activation voltage for the devices. Measurements of the activation voltages for the devices were made to verify the model. Multiple thermal models were also generated for the device; these predicted heat flux through the device in the on and off states, and provided package design constraints. Thermal testing provided additional information for the model. The new device designs also required modifications to the fabrication process.

Before settling on the modified ST-5 package, an alternate package for the devices was studied. This design process gave insight and ideas for changes necessary to integrate the ST-5 package with the new devices and with MIDSTAR I. The previous package was for a different MEMS device and operation platform, and required significant modification. Changes were made to the planned interface between the satellite and the device array, as MIDSTAR I required a purely serial data connection and different software protocols than the ST-5 satellite.

1.1 Microelectromechanical Systems Background

MEMS have the ability to revolutionize modern technology. Today researchers look to incorporate these devices into almost all aspects of life. Current uses include accelerometers for car air bags, disposable blood pressure sensors, optical fiber components and switches, and micro-optomechanical components for identify-friend-or-foe systems. With a combined world market of approximately $2 billion dollars ($200 million from the Defense Advanced Research Projects Agency), the future of MEMS devices and applications seems to have no limit[2].

MEMS utilize integrated circuit fabrication technology to create controllable, mechanical structures that perform the same tasks of much larger devices, all on a microchip. By uniting macro-scale systems with batch-fabrication techniques and scalability, MEMS deliver the same results at a lower cost in money and volume[3]. A recent explosion in microfabrication technology has produced an endless number of applications for smaller and cheaper MEMS devices.

The Department of Defense is also taking an interest in the possible applications of MEMS. Recent conflicts involving the United States military have proven the necessity of an advantage in technology and information. The cost and size of MEMS allow their use in an extended variety of applications. For instance, microtechnology could enable a field of distributed, unattended sensors. These sensors would have the capability of monitoring enemy traffic and defensive perimeters, at a lower cost in size and power than current systems. MEMS are also being developed for use in the conventional warheads of the Navy and Marine Corps. Embedded devices for inertial guidance and control will increase accuracy and decrease the number of rounds required. With an annual Department of Defense requirement of 250,000-500,000 shells, this is a significant opportunity for MEMS development[4]. Other applications

include fluidic systems for chemical or biological analysis capable of detecting the use of weapons of mass destruction.

The Department of Defense also continues to research space technology. Satellites have given the military the Global Positioning System (GPS), extremely capable intelligence tools, and global communication capabilities. The Defense Advanced Research Projects Agency (DARPA) is currently sponsoring a "Microsatellite Propulsion and Attitude Control System." The project will improve current thruster reliability because the micro-thruster, made from static structures built with MEMS fabrication technology, contains no moving parts, valves, or external tanks[5]. DARPA sees the tactical advantage that will come with the production of a nanosatellite constellation capable of far more than the bulkier satellites of today. These nanosatellites require the miniaturization of onboard systems and sensors. A large portion of these systems will require the use of MEMS to meet mass and power requirements.

1.2 MEMS Packaging

While the emphasis of MEMS research has been in the design of the actual devices, equally important is the interface between these devices and their environment. The environment includes all influences that the devices will come into contact with in operation. This includes potentially harmful elements such as humidity, static charge, and dust. The environment also contains those properties critical to the device, such as the environmental element being studied by a MEMS sensor or a path for thermal transport in the case of the devices considered here.

The worldwide systems packaging market totals 109 billion dollars, of which a small but crucial 3 billion is spent on thermal packages[6]. The package must first be able to power, cool,

and protect the device. This will allow the device to perform as expected for the duration of its life. Packaging must also provide input and output connections so that control of the device can be maintained and feedback collected. Meeting these requirements is often more demanding than the development of the device itself[7]. The package combines electrical, mechanical, and material technology. The electrical aspect of the signal environment includes attenuation, distortion, radiation, and cross talk. Mechanical technology must provide reliability and reduce corrosion, deformation, and cracking. The materials used must lend themselves to the operating conditions and environment.

While MEMS are an offshoot of microelectronics, the packaging needs are more complex. Where an integrated circuit can usually be completely isolated in thick plastic, a MEMS device must interact directly with its surroundings. This requires a design that is much more device specific and creative than that of an integrated circuit.

Because the package often dominates device cost, the details of commercial microelectromechanical device interfaces are highly proprietary. At the same time, academics do not often develop their devices beyond operation, un-packaged, in the lab. As a result, there is little published on MEMS packaging issues. However, some groups have published work on chemical sensor packaging[8], implantable electronics[9], and on general MEMS packaging issues[10].

1.3 MEMS in Satellite Thermal Control

The goal of thermal control is to maintain a temperature that is within the operational design specifications for the system. With any space-based system, such as satellites, thermal control becomes very important and challenging. Without conduction or convection in space, heat must be generated within the satellite to keep components from freezing. When excess heat

is generated, however, the satellite must be able to radiate all excess heat before temperatures become too high.

One approach is to coat the satellite with a variable emissivity coating (VEC). Emissivity is the ratio of heat radiated by a surface to that of a black body at the same temperature. By varying the emissivity of a structure, one can alter the heat dissipation rate in response to operational conditions. Highly reflective surfaces, such as polished metals, have low emissivities. The emissivity of electroplated gold is 0.03[11]. Black paints have some of the highest emissivities, which can be as high as 0.97. Surface roughness also causes an increase in emissivity. By changing the satellite's emissivity, the heat radiated into space can be controlled.

Figure 3(a) illustrates a louver-design VEC. Mechanical motors control the position of hinged flaps that either close or open above a high emissivity layer. When the flaps are closed, heat can only be radiated by the low emissivity flap material. On the other hand, when opened the heat is radiated from the high emissivity surface beneath the flaps. This change in emissivity causes a different rate of heat flux out of the radiator in the open and closed positions.

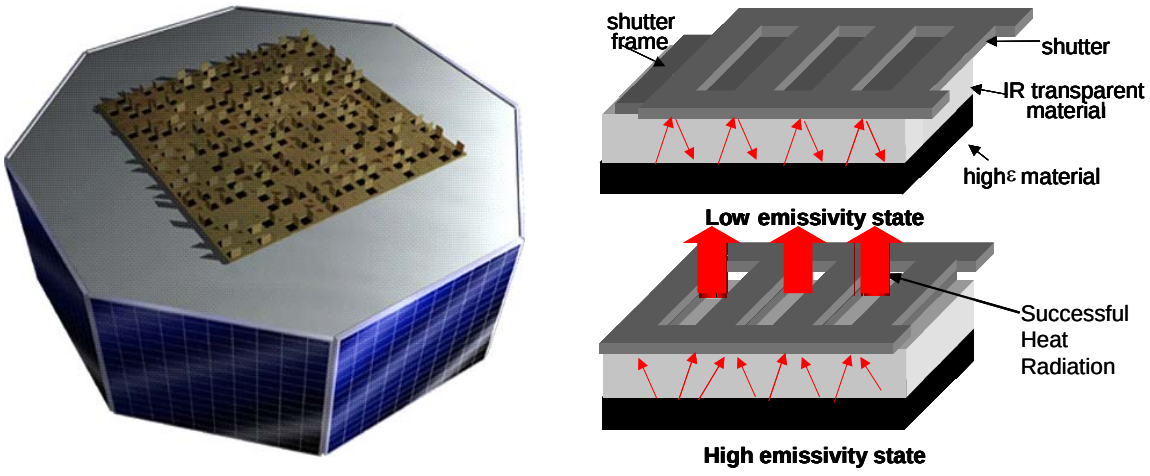


Figure 3. VEC devices: (a) flaps design and (b) shutter device design.

Figure 3(b) shows a shutter design alternative. When activated, a perforated, low emissivity plate is moved to reveal the high emissivity surface below. The flap has the advantage of utilizing a greater percentage of the surface area, while the shutter design requires a much smaller range of motion[12]. Similar structures have been used in a number of different MEMS devices to date, including an optical sensor 'eyelid'[13], a micro-shutter for intensity modulation[14], and a magnetically actuated shutter[15].

Both of these devices have been designed and built at Johns Hopkins University Applied Physics Laboratory (APL). The shutter design will be launched as part of NASA's New Millennium Program on the Space Technology 5 (ST-5) mission in 2004. For this test flight, an aluminum test panel will be mounted on the exterior of the satellite and will support 36 shutter radiator die (12.65 mm x 13.03 mm). The shutters require an activation voltage of 60 Volts that will be supplied by an Electronics Control Unit (ECU) mounted in the satellite's interior. The ECU's microprocessor can open or close all of the devices, provided the satellite's Command and Data Handling Unit (C&DH) sends the ECU permission. The ECU will communicate with the ST-5 C&DH via two control lines. The satellite's C&DH sends commands that tell the ECU whether the ECU will control the louvers independently or whether control will come directly from the satellite[16]. These commands ensure the satellite has the additional power available that these devices require.

1.4 United States Naval Academy Satellite MIDSTAR I

In 2006, the United States Naval Academy intends to launch its satellite MIDSTAR I. This 115 kg satellite will be connected to the Delta IV rocket via a Secondary Payload Adapter (SPA) along with up to five other secondary satellites. A MEMS test configuration will be

implemented on the satellite for prototype testing. Once in orbit, the satellite will have an average payload power of 27 watts from its 20 solar cells. Communications between the satellite and earth will be via the 12 meter satellite dish at the USNA base station. The satellite will be equipped with a 100 kb/s uplink and a 68 kb/s downlink able to transmit all necessary data daily. This will facilitate daily information updates on the MEMS device[17].

MIDSTAR I is the perfect test vehicle for the MEMS structure. The MIDSTAR satellite is simple, yet sophisticated enough to allow communication and provide ample power. Since MIDSTAR is representative of many space systems, the data collected could be used for future integration of the thermal control system on other satellites. MIDSTAR's mission is not dependant on the performance of this test bed, so the experiment is a low risk means to demonstrate the satellite's role as a test platform and the suitability of the device for space flight.

This test bed is not going to provide thermal control for MIDSTAR I, rather it will be used to collect data on device performance in space. The package attached to the external skin of MIDSTAR I will be thermally isolated by limiting contact with the satellite. A heater embedded in the package will provide two levels of temperature data as the devices are switched on and off, therefore varying the heat radiated into space. If the mission were to actually control the temperature of MIDSTAR I, the device would be in thermal contact with the satellite and occupy a location on the exterior closest to heat sources, such as circuitry and motors. This is the future intent of these devices, but before they are used for cooling, their operation and space flight tolerances must be established.

2. Variable Conductivity Thermal Control Device

Fabrication of an APL-designed variable conductivity thermal control device began in the spring of 2003. The device, like other MEMS, used the same wafer engineering techniques as the semiconductor industry. Three similar designs were included in this fabrication run. Having these separate designs has enabled multiple verifications of models and provided more than one set of data to draw upon.

The variable conductivity thermal control device is not a new concept in satellite thermal control. These systems have been designed and produced on the macro- scale by Sensortex, Inc.[18,19,20] Sensortex's approach involves using a voltage to control the amount of heat radiated from the satellite. The primary drawback for their macro- design, however, is the large voltage required. By scaling this technology to the micro- scale, the nano- satellites of the future need only supply the 20-24 Volts, as described earlier.

Fabricated in parallel with these three designs was a different set of devices made by MEMSCAP based in Bernin, France. These devices were not the focus of this research but did lend additional data and interesting ideas to the design process.

2.1 Operation Principle

The APL thermal control MEMS device consisted of a suspended gold membrane supported by a narrow polymer frame or post over a silicon substrate. The membrane should be coated with a high emissivity material. This design was based on the principle that in the vacuum of space heat can only be dissipated through radiation. The silicon substrate would be in thermal contact with the satellite, allowing heat conduction to the silicon. While the device was off, both the poor thermal conductivity of the polymer and the gap between membrane and

substrate minimize radiation. This state is shown in Figure 4(a). When heat dissipation would be desired, applying a voltage between the gold membrane and silicon substrate would produce a capacitive force large enough to bend the membrane into contact with the substrate, as is shown in Figure 4(b). A thin dielectric layer coating the silicon substrate prevented current flow between the membrane and the silicon.

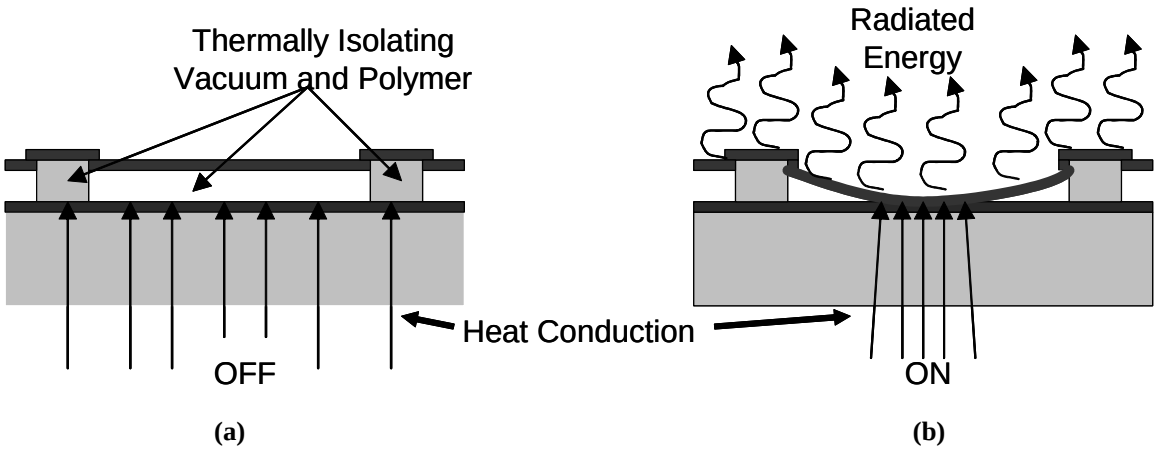
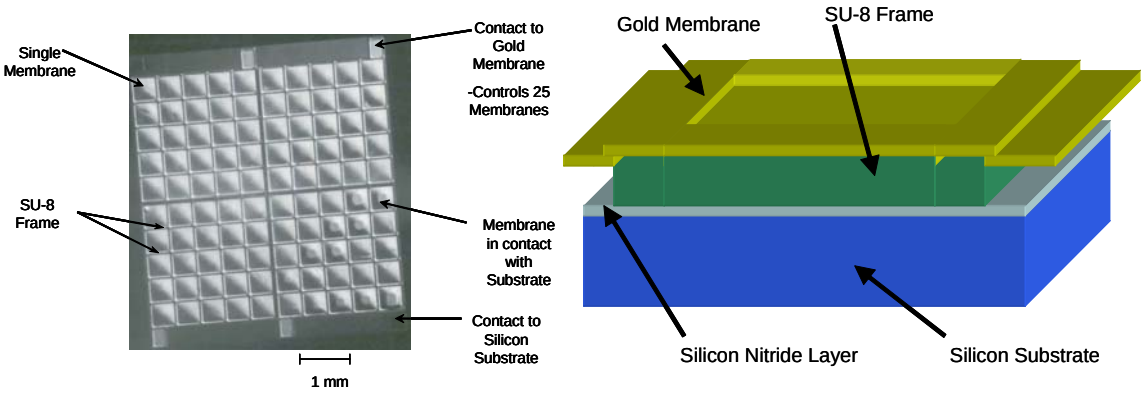


Figure 4. Heat conduction and radiation in the on and off states.

This approach to thermal control has a number of advantages. Current thermal switches require much higher voltages than the satellite produces, which required additional hardware for operation. This variable thermal conductivity device was designed so that the required voltage could be directly supplied by the satellite. Also, this design required very little power because the device only drew current when changed between the on and off states.

Two separate designs were explored in order to compare tradeoffs in stability versus thermal conductivity. The first device uses a polymer frame for each membrane. By supporting the gold on every side, the structure is more resistant to damage and "stiction," which is a yield limiting problem for MEMS in which capillary forces in the drying process result in permanent

contact of the membrane and substrate.

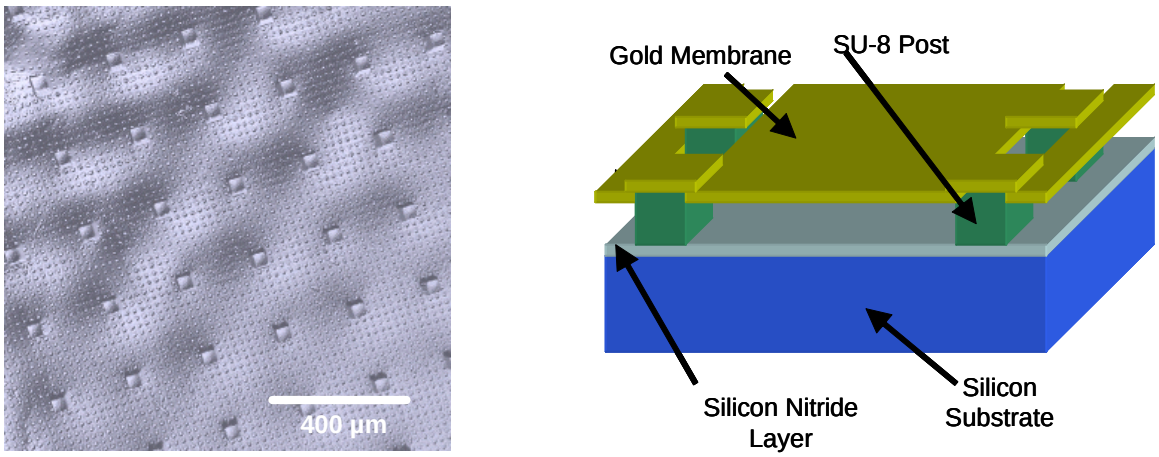


(a) **(b)**

Figure 5. (a) Overhead view of released frame type MEMS die and (b) materials in frame device.

Figure 5(a) shows a microscope image of a released frame-type device. Each square is a gold membrane capable of coming into contact with the silicon. Each of the 4 gold contacts controls the deflection of 25 membranes. Also visible in the bottom, right quadrant is the contact for the lower electrode.

The second design utilizes polymer posts to support the membrane. These posts allow a greater area of thermal contact, thereby increasing device performance. On the other hand, the membrane has less support and is more susceptible to damage and stiction. While only one size frame was designed, two separate post designs were fabricated. One uses a larger post with nearly twice the separation between supports. The other uses smaller posts packed closer together. There are four times more posts per die with the smaller post design. Figure 6 shows a close up image of a released portion of the post type design. Each quadrant contains 64 of these 250 μm^2 posts.



(a) **(b)**

Figure 6. (a) Wyko Interferometer image of small post structure and (b) structure materials.

The devices created using the MEMSCAP multi-user process had both drawbacks and advantages over the APL designs. Unfortunately with the multi-user process, the polymer SU-8 could not be used and polysilicon was used despite its high thermal conductivity. The multi-user process MEMS compensated by replacing posts or frames with support arms shown in Figure 7. Each bridge structure was supported by either four or two arms that ran from the side of the bridge to the substrate. These support arms were longer than the posts, which provided better thermal characteristics. The bridge was suspended 2 µm above the substrate, the same as the APL designs. When a voltage was applied, the supports flexed until the bridge came into contact with the substrate.

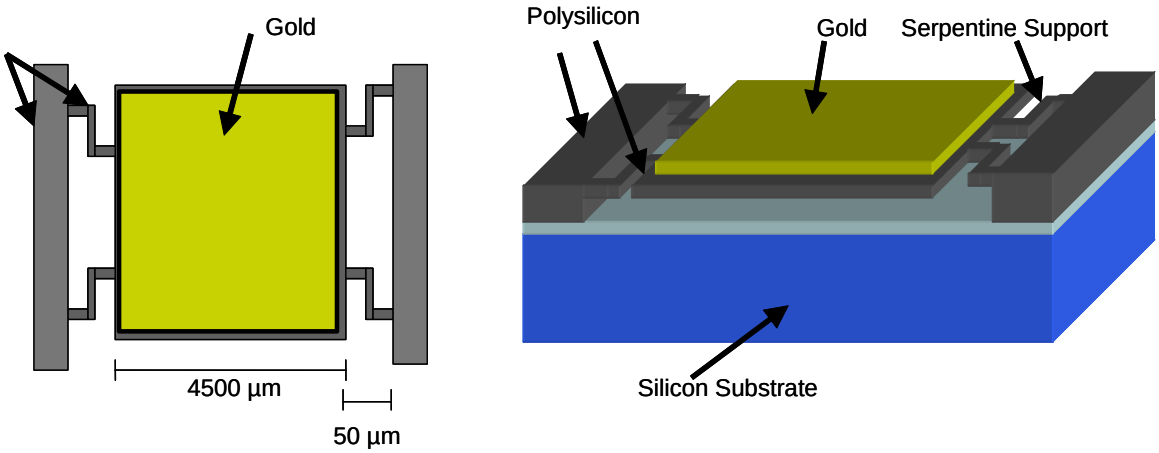


Figure 7. MUMPS design utilizing serpentine horizontal supports.

The major flaw with serpentine supports is their relatively low fundamental frequency. The post and frame designs have fundamental frequencies in the tens of kilohertz. The fundamental frequency, Hz, can be defined as

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k}{m}} \quad \textbf{(1)}$$

where k is the effective spring constant, in N/m, and m is the mass of the membrane or bridge, in kg. With a lower fundamental frequency, the design is more susceptible to damage from vibration. This problem was seen in the production and testing of the serpentine devices. The MUMPS structure pictured above had a fundamental frequency of approximately 20 kHz, which was less than half the value of the post of frame designs.

2.2 Device Fabrication and Release

The fabrication process originally created by APL is outlined in Figure 8.

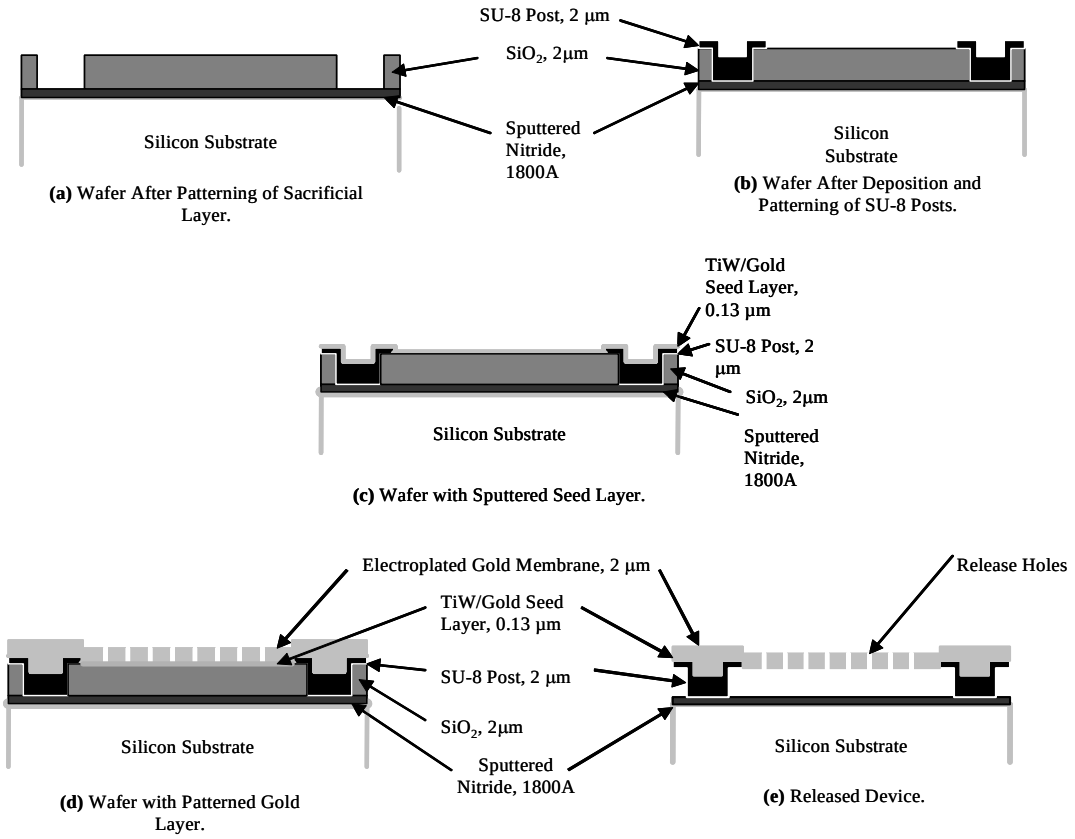
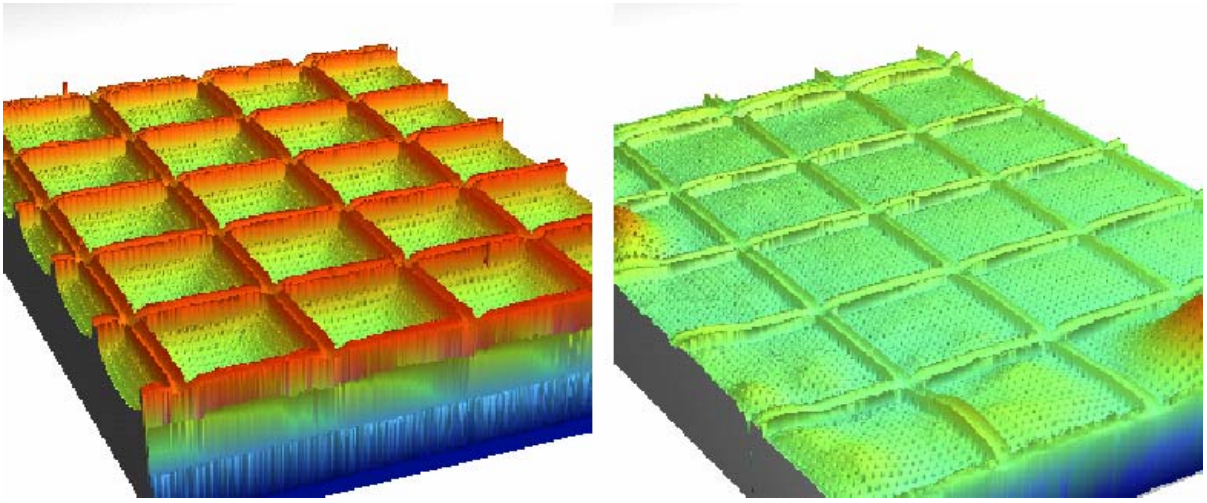


Figure 8. Illustrations of fabrication steps.

The first step in this fabrication is to coat the entire wafer with a thin layer of silicon nitride followed by a patterned layer of silicon dioxide. With the silicon dioxide in place, the polymer SU-8 can then be deposited. The next step is to sputter a thin gold and titanium tungsten layer on the wafer. With that in place, two micrometers of gold can then be electroplated. The final step of fabrication is the release phase. In this phase, the wafer is rinsed in a hydrofluoric acid bath to remove the silicon dioxide. With the silicon dioxide removed, the gold membrane is purely supported by the SU-8. The removal of this silicon dioxide layer is called the release phase. The first batch of MEMS devices were released in August of 2003, but were not yet examined or tested.

The Trident Project began with measuring and testing the first generation of these devices. An optical interferometer was used to gain initial data about the mechanical structure of released devices. The interferometer illuminates the structure with a collimated beam while varying the distance between sample and detector. The resulting interference fringes produce a three dimensional representation. A sample of two interferometer scans of the device can be seen in Figure 9. The concave deformation in Figure 9(a) depicts a typical die in the first release batch, while (b) shows a later release batch without any deformation.



(a) **(b)**

Figure 9. 3-D Renderings from optical profiler scans of identical devices in first release batch with deformation(a) and subsequent batch (b) that included the removal of the adhesion layer beneath the membranes.

Through testing, it was determined that the first fabrication sequence had two distinct problems, membrane deformation and a lack of adhesion between the silicon and SU-8 posts. Membrane deformation is distortion of the intended shape in the unactuated state. An adhesion problem occurs when a device layer breaks apart or "lifts off" from an adjacent layer. With the deformation shown in Figure 9, the fabrication process or device design needed to be reexamined

to determine its cause. The uniformity of the deformation indicated that the cause of the deformation must have been fabrication stress in a uniform layer. Gold is naturally slightly compressive, which should force the membranes to flatten. It was hypothesized that the cause was the titanium tungsten layer attached to the underside of the bridge. Despite its relatively small thickness, the tensile force is enough to deflect the bridges from 0.5 μm to 1.5 μm. The hypothesis was tested with the help of the APL clean room technicians, who used a hydrogen peroxide etch to dissolve the titanium tungsten while leaving the other parts of the device intact. Imaging of the resultant structures, Figure 9(b), revealed the deformation was absent, supporting the hypothesis.

Additional batches of devices were subsequently released by the APL staff in a hydrofluoric acid bath and in a hydrogen peroxide bath with rinse phases in between. The effects were varied based on the times that each device spent in the baths. With the increased rinse times came greater issues with adhesion. Not only was silicon/SU-8 adhesion a problem, but the gold membrane began peeling off the SU-8 posts on some die. Figure 10 shows a device where the gold and SU-8 lifted off from the silicon substrate. The SU-8 post, center square, is still attached. The surrounding holes are the release holes. It was clear that the shorter the time the device was in hydrofluoric acid, water, or hydrogen peroxide, the greater the yield. Yield describes the percentage of functional MEMS devices created per wafer.

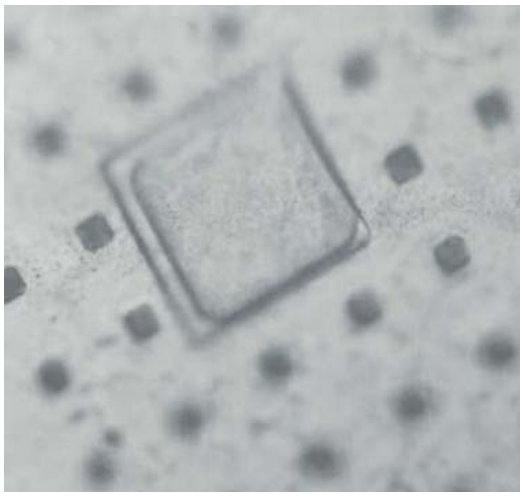


Figure 10. Optical microscope view of peeled underside to gold membrane.

With a long enough rinse, the titanium tungsten between the post and gold is actually etched away. This, however, did not happen to every device and has only limited the yield. In particular, the post designs were more susceptible to adhesion problems because of the smaller gold/SU-8 interface area. The frames were able to withstand the rinse and were used in electromechanical testing.

In order to increase the device yield, steps were taken to increase adhesion between the SU-8 interfaces. Initially chrome, an element used for its adhesion to SU-8[21], was sputtered onto the silicon nitride. This change positively affected wafer yield, but adhesion issues still remained a problem. To further promote adhesion between the SU-8 and silicon, the sacrificial layer of silicon dioxide was replaced with copper. By switching to copper, it was possible to pattern a thin layer of silicon dioxide beneath the SU-8. The silicon dioxide created an additional adhesion layer to the SU-8.

The device fabrication does not yet include a high emissivity layer. This aspect of device performance is absolutely critical, but remains a problem. Without a high emissivity layer, the

heat radiated by the gold membrane will be very low, due to the low emissivity of electroplated gold (ε=0.03). The issue has been addressed by attempting to coat the device after fabrication and release. This problem will not be completely solved, however, until the high emissivity layer becomes part of the actual device fabrication and can be attached before the device is released.

3. Device Modeling

In order to produce insight into the operation of the device and how the package would have to be designed, an electromechanical model and thermal model were developed by the author.

3.1 Electromechanical Model

The electromechanical model is necessary to determine what voltages and forces will be present in the operation of the device. The model described below assumes that the membrane is circular and supported around its circumference. Another model based on a bridge device supported on two ends was also considered to approximate the post devices. After comparing the models and looking at the post devices when activated (the contact to the substrate is nearly circular), the circular membrane model was chosen for all three designs. For the designs to fit this model, the area unsupported by SU-8 was used to estimate an effective area were the membranes circular. The estimation method and results are shown in Figure 11 and Table 1.

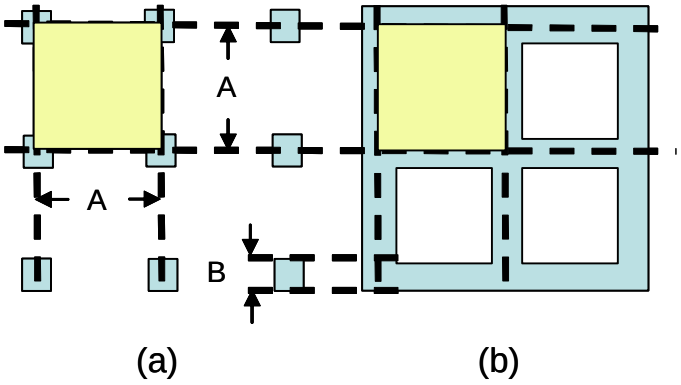


Figure 11. Device dimensions for (a) post design and (b) frame design used to calculate membrane area.

Table 1. Measurement of unsupported membrane area.

Dimensions	A[µm]	B[µm]	Unsupported Membrane Area [m2]
Frame Design	450	50	1.6E-7
Small Post Design	250	50	6.0E-8
Large Post Design	450	100	1.93E-7

It was necessary to know the voltage these devices will require to operate, known as the actuation voltage. This allowed experimental results to be compared, the validation of the circular membrane model. This actuation voltage can also be called the device pull-in voltage. Capacitive plates such as the membranes used here are subject to a phenomenon called “pull-in.” The electrostatic force on the moving plate is inversely proportional to the square of the gap, while the restoring force is proportional to the deflection. This results in an instability where the moving plate snaps down once the voltage across the plates exceeds a threshold, called the “pull-in” voltage. One goal was to design for a pull-in voltage of less than 28 volts. Since this is a typical satellite bus voltage, less signal conditioning would be necessary to drive the device.

The key device parameters that determine pull-in voltage are shown in Figure 12.

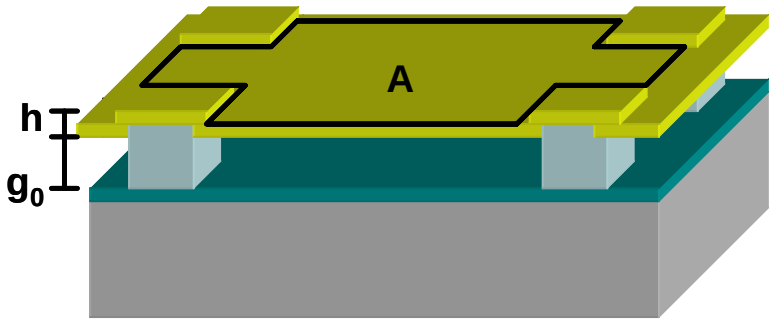


Figure 12. Dimensions used for electromechanical model.

The pull-in voltage is given by[22]

$$V_{pi} = \sqrt{\frac{8k}{27\varepsilon_0 A} g_0^3} \tag{2}$$

Here V_{pi} is the pull-in voltage (V), k is the effective spring constant (N/m) of the structure, g_0 is the gap at zero bias (m), ε_0 is the permittivity of free space (F/m), and A is the area of the electrode (m^2), given in Table 1 and shown in Figure 12. In order to find the spring constant, the device will be approximated by a circular diaphragm of equal area, with spring constant given by[6]

$$k = \frac{16\pi^2 E h^3}{3A(1-\nu^2)} + 4\pi\sigma h \tag{3}$$

Here E is Young's modulus of the membrane (Pa), h is the membrane thickness (m), A is the area of the membrane (m^2), ν is Poisson's ratio, and σ is the biaxial residual stress (Pa). Table 2 shows the material properties used in both the electromechanical model and the thermal model. The theoretical values for V_{pi} are shown in Table 3. Post design 2 was designed for a much higher actuation voltage for comparison. The higher voltage design should be more rugged because of the higher spring constant.

Table 2. Relevant material properties for design[23].

Property	Au	SU-8[24]	SiO_2	SiN
k_{th} [W/(m•K)]	320	0.2	1.1	30.1
E [GPa]	80	---	---	---
ν	0.42	---	---	---
σ [MPa]	+10	---	---	---

Table 3. Estimated pull-in voltages.

Design	Membrane Thickness [µm]	Effective Membrane Width [µm]	With Adhesion Layer		Without Adhesion Layer	
			Effective* Initial Gap [µm]	Theoretical Pull-in Voltage [V]	Effective Initial Gap [µm]	Theoretical Pull-in Voltage [V]
Post Design 1	2	550	0.8	5.1	2	20.0
Post Design 2	2	300	1.5 - 1.8	57.9 – 73.6	2	89.2
Frame Design	2	400	0.6	11.5	2	28.2

*measured by interferometric microscope

3.2 Thermal Model

3.2.1 MIDSTAR, Package, and Device Model

A thermal model of device operation was necessary to determine the device's cooling ability. When the package and satellite were taken into consideration for the model as well, package design configuration could be optimized. This model would also be necessary to interpret the data from the thermal testing onboard MIDSTAR I.

This device is a variable conductivity radiator, and as such insulates the satellite in the off position by denying a good thermal conduction path. The heat is insulated by the SU-8 and vacuum interface. The SU-8 will allow only a small amount of heat to conduct to the gold membrane, and the vacuum will only allow a small amount of heat to radiate from the silicon nitride. In the on-state, bringing the gold membrane into physical contact with the substrate

creates a conduction path to the high emissivity layer at the surface. This contact will have a thermal conductance, G, that depends on the closing force, which in turn depends on the voltage applied and the dielectric constant of silicon nitride. Thermal contact conductance is higher in a vacuum than in air. This may seem counterintuitive given that contacts between macro-structures have lower contact conductance in a vacuum. The difference has been attributed to the small surface roughness of micro-scale structures. The air impedes the contact instead of supplying an alternate path of conduction as is seen on the macro-scale. The low relative roughness of the gold membrane has also been shown to increase thermal conductivity.

The variation in k_{th}, thermal conductivity, between the on and off states is the primary characteristic of device performance. In order to measure its value, the temperature of the substrate will be measured in the on and off states. This temperature difference must then be correlated to the conductivity change using a model, such as is shown in Figure 13.

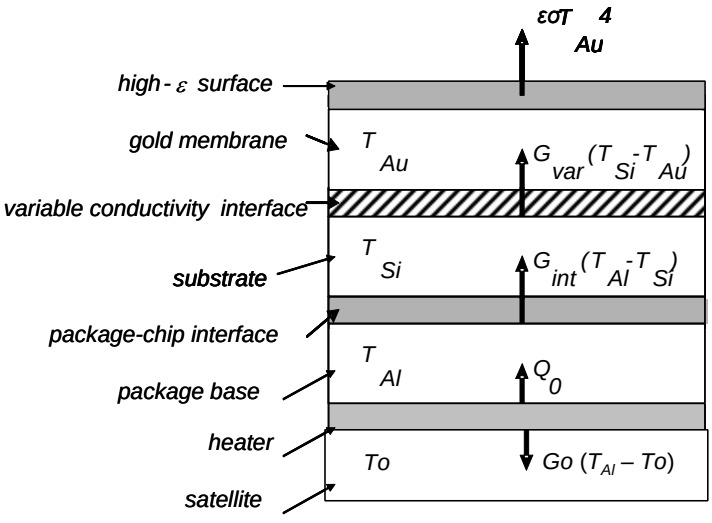


Figure 13. Illustration of heat flows for basic thermal model to describe testing on MIDSTAR I.

The following assumptions were made. The temperature of each material is considered to be constant throughout each material layer. This is a reasonable estimate with layers of such

small thickness and of such high thermal conductivity. All heat is modeled to conduct vertically, not radiating from the sides of the layers.

The principle equation governing heat flow is given by:

$$q_{in}^{"} \cdot A + \dot{E}_g - q_{out}^{"} \cdot A = C_t \frac{dT}{dt} \quad \textbf{(4)}$$

Here q_{in}" is equal to the input thermal flux (W/m^2), A is area (m^2), E_g is the rate of internally generated thermal energy (W), q_{out}" is the output thermal flux (W/m^2), C_t is the thermal capacitance (J/K), and dT/dt is the change in temperature with respect to time, (K/s).[25] The conductance of a material can be described by:

$$G = \frac{k_{th} \cdot A}{h} \quad \textbf{(5)}$$

Here G is thermal conductance, (W/K), k_{th} is the thermal conductivity (W/mK) and h is the height or thickness of the layer (m). For this device, performance is better described by the net thermal flux per unit area. Therefore, each term in the balanced energy equation is divided by the area of a single device, such that q_0" is $\dot{Q}_0$ divided by the area of thermal contact between satellite and package. Also, g" is G divided by the boundary surface area.

These equations can be used to describe each layer of the thermal model.

$$q_o^{"} - g_{\text{int}}^{"}\left(T_{Al} - T_{Si}\right) - g_0^{"}(T_{Al} - T_0) = \frac{C_{t,At}}{A} \cdot \frac{dT_{Al}}{dt} \quad \textbf{(6)}$$

$$g_{\text{int}}^{"}\left(T_{Al} - T_{Si}\right) - g_{\text{var}}^{"}\left(T_{Si} - T_{Au}\right) = \frac{C_{t,Si}}{A}\frac{dT_{Si}}{dt} \quad \textbf{(7)}$$

$$g_{\text{var}}^{"}\left(T_{Si} - T_{Au}\right) - \varepsilon\sigma T_{Au}^4 = \frac{C_{t,Au}}{A}\frac{dT_{Au}}{dt} \quad \textbf{(8)}$$

In Equation 8, the quartic dependence of the radiation term complicates the solution for this system of equations. The equations must then be linearized by assuming that the change in temperatures of each layer is negligible when compared to the constant temperature of the satellite, T_0. The substitution, $T_{Al} = T_0 + \Delta T_{Al}$ can then be made. The same substitution can also be made for T_{Si} and T_{Au}. In equation 8, this substitution allows for:

$$T_{Au}^4 = (T_0 + \Delta T_{Au})^4 = T_0^4 + 4T_0^3 \Delta T_{Au} + ... \approx T_0^4 + 4T_0^3 \Delta T_{Au} \quad \textbf{(9)}$$

This system of equations can then be solved for the steady state change in temperature for each layer. These equations are dependant on nearly every aspect of the thermal model and therefore dictated package design aspects, such as material choice for the package/chip interface, and packaging thickness.

3.2.2 Device Thermal Model

Due to the complexity of MIDSTAR, Package, and Device Model, a simpler model for the thermal operation of the device alone was created. The model in Figure 14 shows the flow of heat through the device in the on and off positions. A constant heat flow, like that which will be seen from the package's heater, simplifies the thermal transfer equations. This configuration represents how the devices will be tested on MIDSTAR 1. The devices will be thermally isolated from the satellite so that testing the devices will not interfere with satellite operation. A separate heater on the underside of the device will simulate different operation conditions.

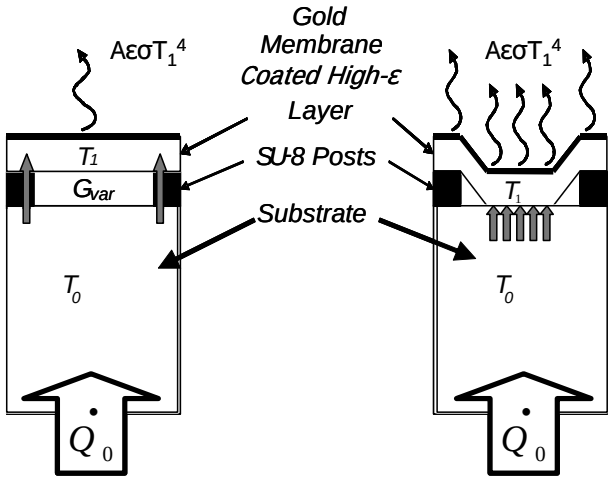


Figure 14. Model of Thermal Device Characteristics.

A critical design variable is G_{var}, the thermal conductance between substrate and gold membrane. This parameter determines the rate at which heat flows, and thus controls the rate limiting step. When the device is off, conduction should limit the heat dissipated. When the device is on, heat dissipation should be limited by radiation. The difference in G_{var} between on and off determines the ability of the device to control the satellite's thermal capacitance. G_{var} also determines the temperature gradient across the device, and consequently the temperature, T_o.

By supplying a constant heat flux to the device, the temperature of the silicon can indicate device performance. Based on Figure 14, the energy equations become:

$$\dot{Q}_0 - G_{\text{var}}(T_0 - T_1) = C_{t,0}\frac{dT_0}{dt} \qquad \textbf{(10)}$$

$$G_{\text{var}}(T_0 - T_1) - 4A\varepsilon\sigma T_1^4 = C_{t,1}\frac{dT_1}{dt} \qquad \textbf{(11)}$$

In steady state, the substrate temperature, T_0, is therefore given by:

$$T_0 = \frac{\dot{Q}_0}{G_{\text{var}}} + \left(\frac{\dot{Q}_0}{4A\varepsilon\sigma}\right)^{1/4} \quad \textbf{(12)}$$

Therefore, the temperature difference between the off and on states is:

$$\Delta T_0 = \frac{\dot{Q}_0}{G_{\text{var},off}} - \frac{\dot{Q}_0}{G_{\text{var},on}} \quad \textbf{(13)}$$

If $G_{var,off}$ is less than $G_{var,on}$, then the change in temperature can be estimated as::

$$\Delta T_0 \approx \frac{\dot{Q}_0}{G_{\text{var},off}} \quad \textbf{(14)}$$

Using Equation 5 for thermal conductance, G, the MEMS designs have values for thermal conductance while in the off position as shown in Table 4.

Table 4. Thermal conductance for different designs.

Design	**$G_{var,off}$ [W/K]**
Large Post	3.68
Small Post	2.5
Frame	13.1
MUMPS-Suspended	0.3

With these values for thermal conductance, the temperature difference between the steady state on and off positions can be derived. Assuming good contact between gold and silicon when on and that the gold is coated with a perfectly emissive layer (ε=1), the temperature difference is shown in Figure 15. Temperature difference between on and off states as a function of conductance in off state. The figure assumes a power of 1 watt flows through devices covering an area of 6.25 cm^2.

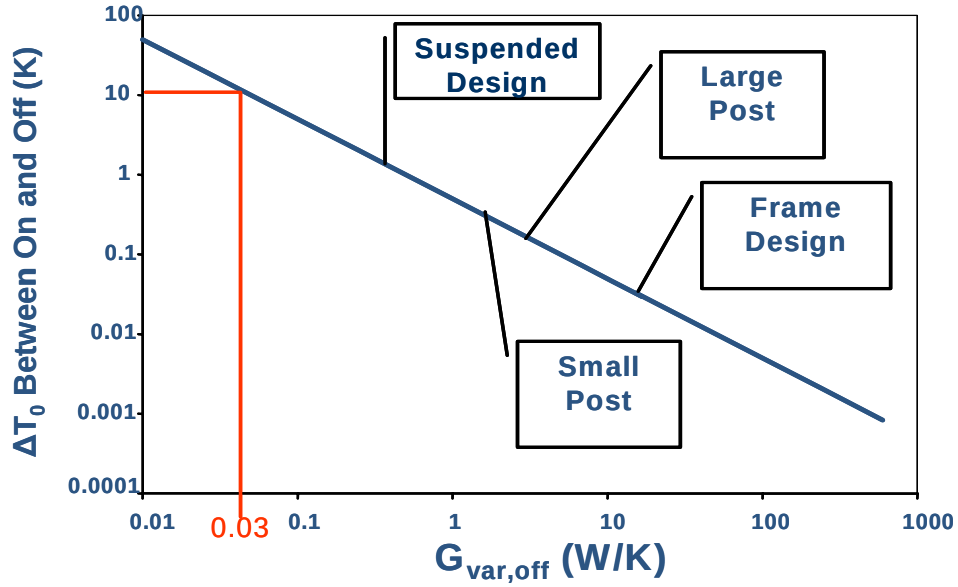


Figure 15. Temperature difference between on and off states as a function of conductance in off state.

The model indicates that $G_{var,off}$ must be 0.03 W/K for a 10 K change in temperature, which is the performance goal. The current designs fall far short of this goal, however the suspended design shows that $G_{var,off}$ values below 1 W/K are attainable. Figure 15 also shows the trade off between good thermal properties and a robust design. While the frame design was considered the best device for wafer yield and voltage performance, its model has the worst thermal performance. For the redesign, the conductance goal of 0.03 W/K must be met even at the cost of durability. The advantage of the suspended design was that its emissive surface was supported by four serpentine polysilicon arms. The thermal path through the serpentine pattern is considerably longer than through the SU-8 posts or frames.

The two variables that affect $G_{var,off}$ are SU-8 area and gap height. For low $G_{var,off}$, it is better to have a larger gap height and a smaller SU-8 effective area, which implies a larger separation between posts. The adjustment of either one of these variables also affects the pull-in voltage as can be shown in Equations (2) and (3). However, an increase in gap height increases pull-in voltage while a decrease in SU-8 area decreases pull-in voltage, so $G_{var,off}$ can be adjusted without compromising V_{pi}.

4. Experimental Setup

In order to validate the device and package models, experimental analysis of both the thermal and electrical properties were undertaken, which required the design and assembly of appropriate experimental apparatuses.

4.1 Optical Characterization

The pull-in voltage required to activate the device is a key indicator of performance and is also necessary for design of the package. The pull-in voltage was measured on a probe station, which is a device that combines a microscope with probes for electrical contacts, controlled by micromanipulators.

With the device stabilized on a vacuum chuck, two probes were used to make voltage connections to the device's positive and ground pads. With the use of the microscope and camera, pictured in Figure 16, the membranes were visually determined to be activated when the membrane became flat against the substrate. The voltage and current could then be read from the power source, placed on the bench next to the microscope.

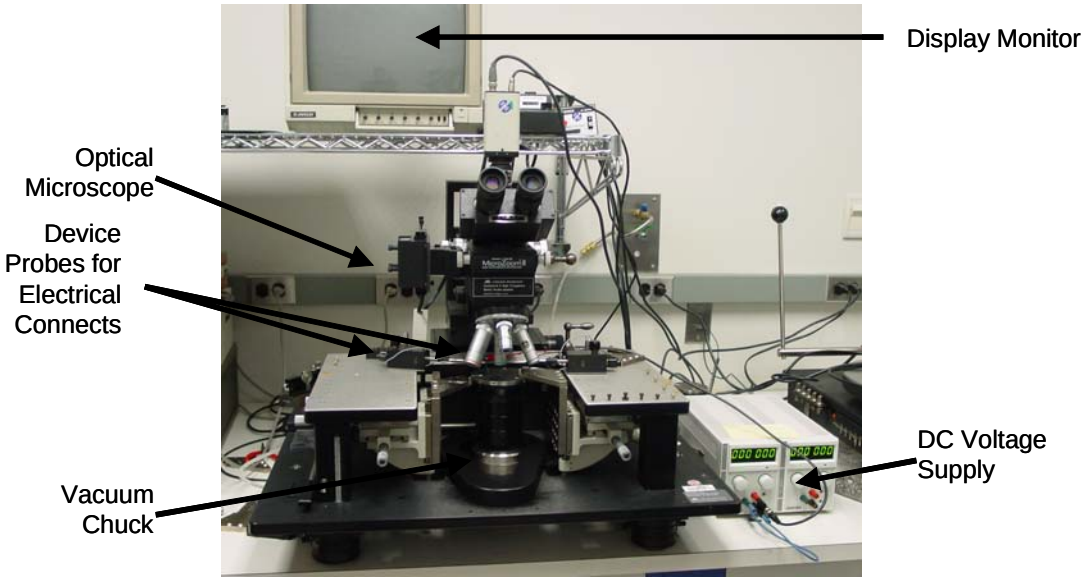


Figure 16. Probe station test setup.

4.2 Vacuum Chamber Design

Thermal measurements required the construction of a vacuum chamber that would allow electrical contacts, temperature measurements, and infrared imaging. A close up of the vacuum chamber can be seen in Figure 17. A single die was placed on a gold fixture that was then screwed into place on top of copper plate. The fixture used wire bonding to attach connections from the die electrical pads to the fixture leads. The fixture also contained the standards used to determine emissivity. The copper plate has an embedded K type thermistor for measuring the copper's temperature. On the underside of the copper plate is a 6.25 cm^2 foil heater. The heater supplied up to 2 watts of power for testing the devices. The copper plate is supported inside the chamber by two sets of bars attached to the chamber walls.

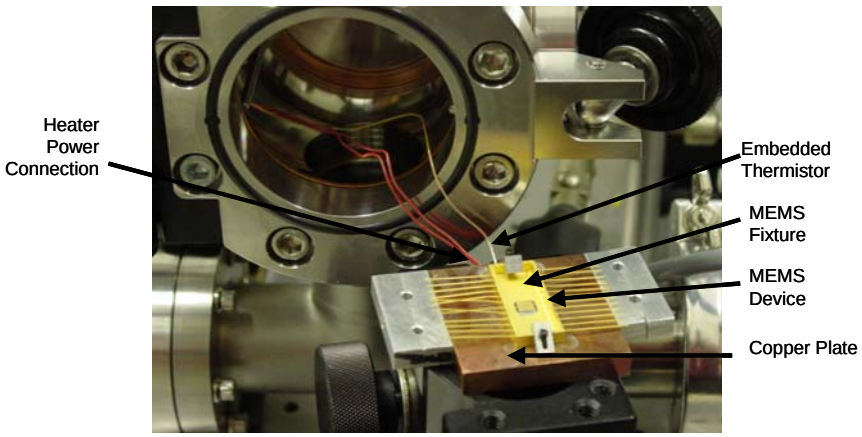


Figure 17. Inside of vacuum chamber.

The vacuum chamber was evacuated by both a roughing pump and a turbomolecular pump, shown in Figure 18. The roughing pump was used until pressure was low enough to engage the turbomolecular pump. The heater and thermistor were relayed via an interconnect through one wall of the chamber to a power supply and data collector, respectively. Above the chamber was the Amber Radiance infrared camera. This was used to measure the emissivity of the surface.

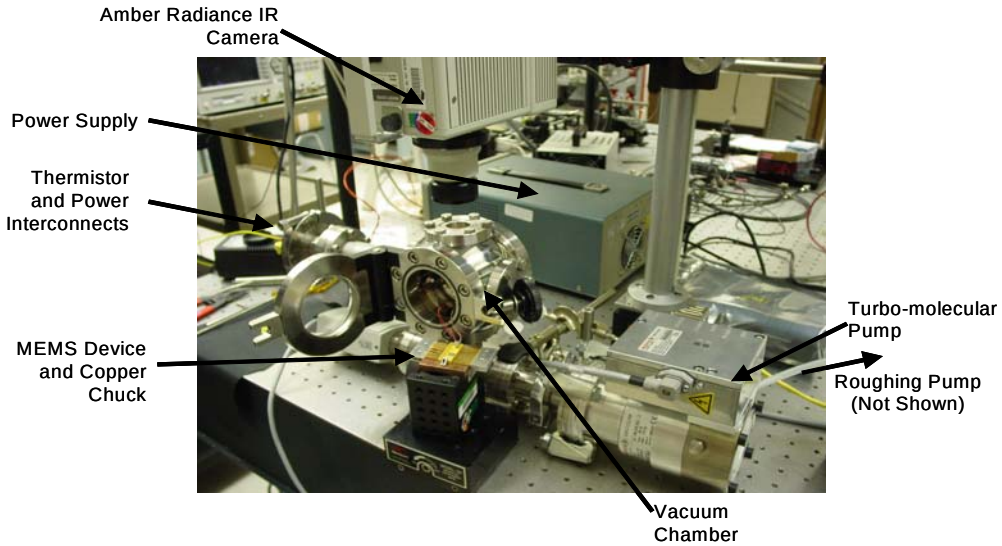


Figure 18. Vacuum test setup.

5. Results

5.1 Electrostatic Results

After fabrication, the initial gap heights were measured with the interferometer. The pull-in voltages were then measured on the probe station. The pull-in voltage testing occurred in air at standard temperature and pressure ($\varepsilon_{air} = 1.00054\varepsilon_0$). The effects the sagging membrane had on pull-in voltage measurements are shown in Table 5. According to equation (2), V_{pi} is directly proportional to the effective initial gap, g_o, raised to the three-halves power. Therefore, the small variation in gap height due to sagging resulted in wide variations in pull-in voltage. Furthermore, once a few membranes in an array have completely deflected, it was difficult to further increase the voltage on the entire array. This was because any greater voltage applied to the deflected devices caused dielectric breakdown. This dielectric breakdown would then cause the membrane to explode. The removal of the titanium tungsten adhesion layer, in addition to eliminating the sagging effect, also produced a more uniform membrane resulting in more uniform activation voltages. The frame designs proved to be the most consistent. These devices showed a much smaller degree of variation in g_0.

Table 5. Device dimensions and resultant voltages.

Design	Membrane Thickness [μm]	Effective Membrane Width [μm]	With Adhesion Layer			Without Adhesion Layer	
			Effective Initial Gap [μm]	Theoretical Pull-in Voltage [V]	Meas. Pull-in Voltage [V]	Theoretical Pull-in Voltage [V]	Meas. Pull-in Voltage [V]
Large Post	2	550	0.8	5.1	7-12	20.0	21
Small Post	2	300	1.5 - 1.8	57.9 - 73.6	18 - 25+	89.2	91
Frame Design	2	400	0.6	11.5	9 - 11	28.2	20-25

With the increased yield and quality of devices available through the improvement of the fabrication steps, an activation voltage of 91 V was measured for the small post design with a 2 μm gap height. The die that produced this data had a very uniform gap height and an easily measured activation voltage as a result.

5.2 Thermal Test Results

The vacuum chamber provided insight into the thermal properties of different samples produced in the laboratory. With the gold acting as the emissive surface very little heat would radiate, however. It was imperative that a layer with much higher emissivity be attached to the gold membrane. This proved to be challenging when fabrication steps would require the layer to be attached after device release. This was necessary because this layer could potentially block the release holes. Coating a 2 μm, loosely supported gold membrane meant that any added stress could deform or even destroy the devices. Also, if the coating fell through the release holes, it might have increased stiction, caused shorting, or decreased thermal conductivity performance.

Primarily two different methods of coating the gold membranes were investigated by the author. One solution involved coating the device with black paint using an aerosol sprayer. The black paint boosted the emissivity, and by using an aerosol sprayer individual dots dried on the membrane rather than a complete layer. The advantage of unconnected dots of black paint was a significant decrease in the stress felt by the membrane. To further promote a thin and disjointed paint layer, the device was heated during application. The heat caused rapid drying of the liquid on contact. Figure 19 shows three die heated by a highly emissive black heat source. The scale shown is a relative measurement of radiation detected from each pixel of the infrared image. The index materials were used to scale the results.

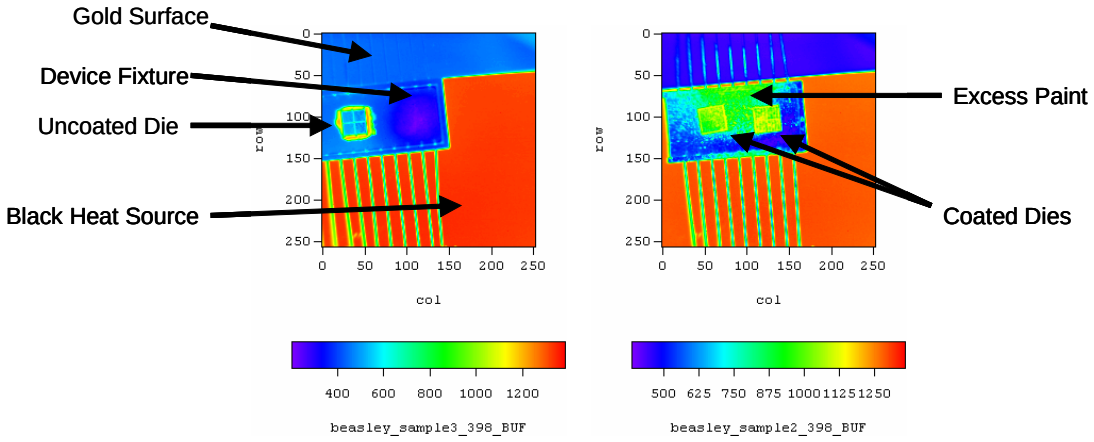


Figure 19. Infrared spectrum of (a) uncoated device and (b) device coated with black paint.

The uncoated die in Figure 19(a) had a color identical to the gold surface, which was used as a control surface for comparison. This means the die, as expected, has an emissivity nearly equal to that of polished gold, which has an emissivity of 0.02. The ring of high radiation surrounding the die is the epoxy used to fasten the die to its fixture. Figure 19(b) shows two unreleased die coated heterogeneously with black paint. This coat provided an emissivity from 0.5 to 0.8. Air brushing of released die would be difficult because the force used to spray the paint would damage the membranes.

The second approach was complicated but could offer a more advantageous solution. Research is currently being conducted at APL to 'grow' carbon nanotubes onto gold plates. By controlling the formation of these very small carbon tubes, specific properties can be obtained. Previously, carbon nanotubes were bonded to gold and showed a high emissivity. An attempt was made to bond nanotubes to a gold membrane similar to the membrane in this project. Unfortunately as Figure 20 shows, the attempted coatings did not yield any significant change in emissivity.

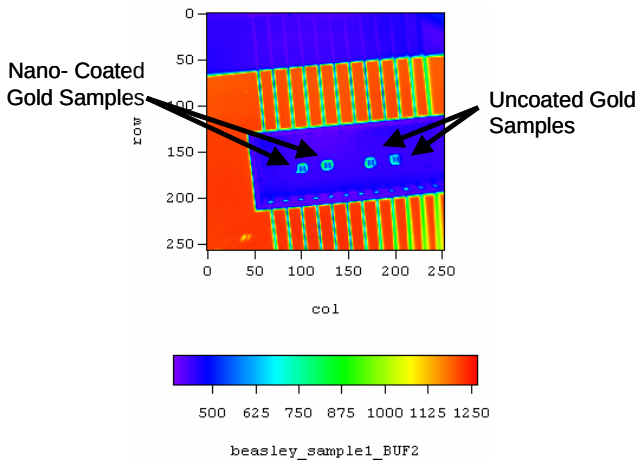


Figure 20. Nano- coating experiment.

The change in temperature between the on and off states for the devices has not been measured. As the thermal model predicted, ΔT_0 would not change appreciably. The thermistor used in the test setup is a type K thermocouple from Omega (5TC-TT-K-40-36). The resolution with the electronics included is ~0.1ºC. This measurement must wait until the new device designs are fabricated that produce a measurable temperature difference.

6. New Device and Wafer Design

Through modeling and testing, serious shortcomings were uncovered in the first APL design. The thermal conductance is too high in the off state, the fabrication process is not robust, and the high emissivity layer has not been integrated with the device. Revisions to both the fabrication process and device design were necessary. Changes to the design include new physical dimensions, altered wafer layout, the addition of testing markers, and new materials. The results of the thermal model made clear that a new device needed to have less conduction when off. In particular, to reach a variable conductance, G_{var}, for the device in the off state of

0.03 W/K, the area of SU-8 would need to be kept to a minimum. For the devices to reach this goal it was necessary to ensure that SU-8 occupied only 1.2% of the die. For the post design, this required using 16 posts per quadrant (like the large post design) with dimensions of less than 60 µm by 60 µm (the small post design used 50 x 50 µm posts). The frame design is not able to meet the goal of 0.03 W/K, as it would require the frames to be 4 µm in width versus the current 50 µm. This is too small for fabrication tolerances. A realistic next generation design with frame widths of 25 µm would reach $G_{var,off}$ of 0.21 W/K.

The ground pads have also been relocated to the center of the sides of the die. This is to allow gold membrane contacts to anchor each corner. It was found in fabrication that these membrane pads actually contributed to keeping the SU-8 attached to the silicon, as seen in Figure 21. Another important addition for testing purposes is a marker on the die so that each quadrant can be discerned.

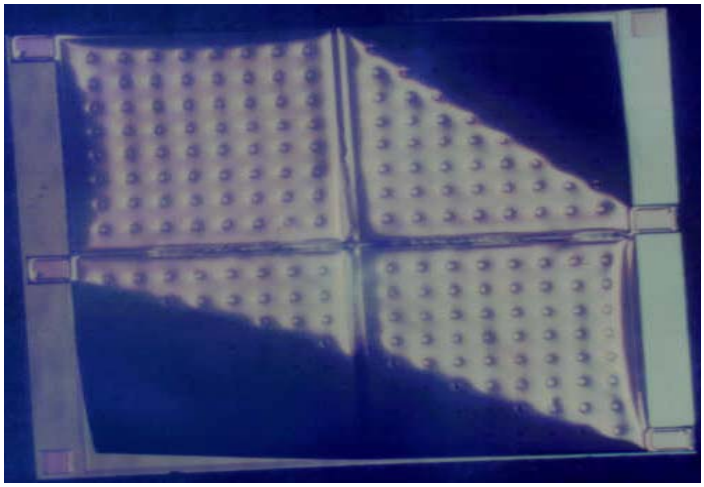


Figure 21. Released die with "lift off" at corners not anchored by bond pads.

Changes to the mask set also had to be made to ensure they could be used when future fabrication techniques are available. For instance, post heights are currently built to 4 µm, but work has begun to increase the SU-8 post height to 5 µm. To capitalize on this ability, the overlap of SU-8 on the silicon dioxide layer had to be doubled from 5 µm to 10 µm. This is to ensure that there is no gap between SU-8 and silicon dioxide where copper etchant could dissolve the adhesion layer between the posts and the silicon.

The dimension variables of the devices on the new mask set are shown in Figure 22.

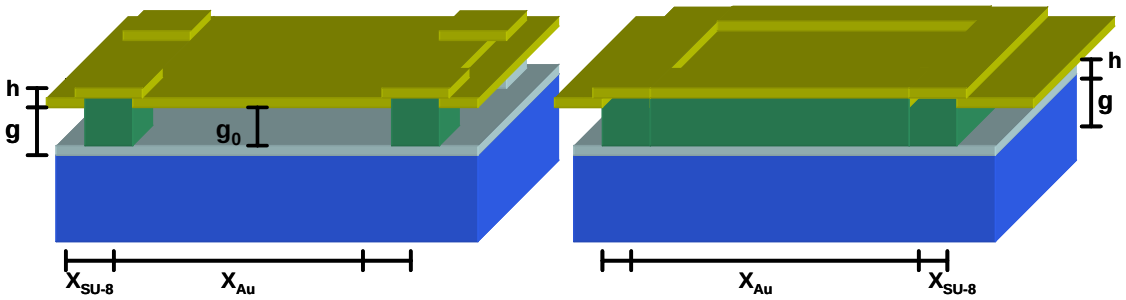


Figure 22. New device dimensions.

The properties of these devices are given in Table 6. The resonance frequencies are estimated from (1), but using an effective mass and using the density of bulk gold, which is greater than that of electroplated gold. These values are therefore an underestimate.

Table 6. New device properties.

Design	X_{Au} [µm]	X_{SU-8} [µm]	g [µm]	g_o [µm]	h [µm]	V_{pi} [V]	$G_{var,off}$ [W/K]	f_o [kHz]
Post 1	500	25	5	5	2	70	0.006	50
Frame 1	500	25	5	5	2	89	0.23	50
Post 2	500	25	5	2.2	2	20	0.006	50
Frame 2	500	25	5	2.2	2	26	0.23	50

There are two different values for the gap height shown in the table. With the increase in SU-8 post height to 5 µm, the thermal properties were greatly improved, but the voltages are no

longer less than 24 V. Using the lesson from the fabrication process, the devices can be fabricated with intentional membrane deformation by controlling the thickness of titanium tungsten in the released device. The necessary film thickness will be found experimentally, but testing has already shown up to 1.5 µm deflection with a 0.13 µm titanium tungsten layer.

A suspended structure, such as that built by the multi-user process, MUMPS, was added to the new wafer design. The fabrication will differ, so SU-8 will be used for the sidewalls, but gold must be used for the suspended supports, as shown in Figure 23. This design uses shorter arms and a lighter gold plate than the MUMPS design, to keep the fundamental resonance frequency at a level close to the previous post and frame designs that did not show sensitivity to vibration. Device dimensions for this design are given in Table 7.

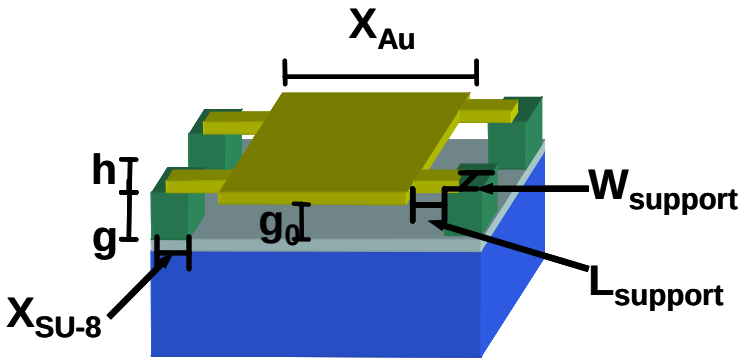


Figure 23. New suspended design using APL process.

Table 7. Suspended device specifications.

Design	X_{Au} [µm]	X_{SU-8} [µm]	$L_{support}$ [µm]	$W_{support}$ [µm]	g [µm]	g_o [µm]	h [µm]	V_{pi} [V]	$G_{var,off}$ [W/K]	f_o [kHz]
Suspended	500	25	35	10	5	5	2	25	0.003	50

7. Package Development

The package design is critical to this project as it will allow the testing of the MEMS thermal control device in space on MIDSTAR I. In order to test the MEMS device, the package must have all necessary components and comply with specified thresholds. The testing done on the device will allow for a better package design based on electrical and thermal data. Also by including the package in the thermal model, the characteristics and results of the tests aboard MIDSTAR I can be varied with packaging solutions.

The package to be used on MIDSTAR I is a necessary testing apparatus, but would not be the same package as would be used for this device to operate as a radiator. The MIDSTAR I package must isolate the device thermally from the satellite in order to have more control over the heater power conducted to the device during verification. Isolation is integral for measuring the temperatures, and consequently the heat dissipated, when the heater is off.

The Interface Control Document (ICD), Appendix A, was produced as part of this project. The contents of the ICD were created from requirements of both the satellite and the planned MEMS packages. The ICD outlined the mechanical and electrical connections between the device package and MIDSTAR I and lays the groundwork for package development. Mass limits and power requirements were set, neither being a large concern as MIDSTAR I is currently underweight and the device requires little power. The power requirements of the heaters, however, will require permission from the C&DH before turning on. This information will be carried on the control lines between the ECU and the C&DH.

7.1 Original Package Design

Creating a unique package could optimize performance of the device, while revealing any necessary implications of testing requirements. Initial concerns in designing this package included the interface between the device and MIDSTAR I, the thermal properties such that the device would operate effectively, and the mechanical properties so that the device could be safely transported. After considering development costs, however, the APL team determined that it would be more cost effective to modify the package developed for the ST-5 program for this new device and platform. Many of the lessons learned in consideration of an alternate package can be applied to this modification. For discussion of the initial package design, see Appendix B.

7.2 APL ST-5 Adaptation

The previous package design built at APL must be modified to meet the specific performance requirements of this MEMS device and to interface with MIDSTAR I. This MEMS device will require a power supply providing 20 to 30 Volts, where the previous design supplied 60 Volts. In order to correct this problem, a new circuit board will use a voltage multiplier. The original design could not use a multiplier because of restraints placed on electrical components. MIDSTAR I, with its focus on COTS technology, has no such requirement. This will also allow all electronics in the Electronics Control Unit to fit onto one circuit board, instead of the original design's two.

The device will also be controlled differently in the new package design. Instead of an array of 36 louver MEMS being controlled simultaneously, as shown in Figure 24(a), each

variable thermal conductivity die will be controlled independently. This will allow for a larger data set by having six separate device trials.

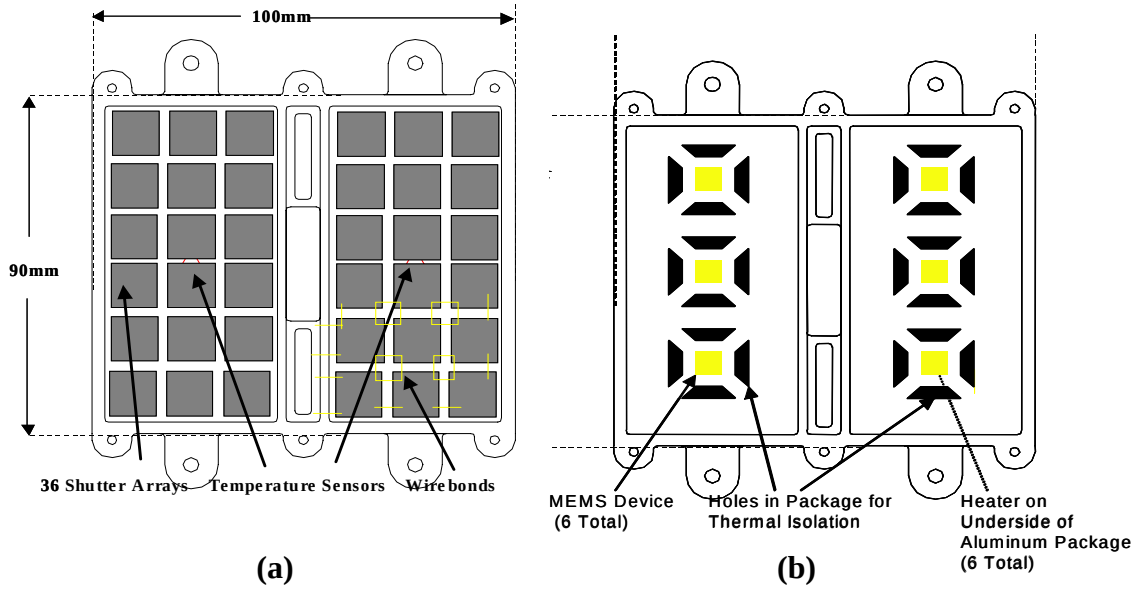


Figure 24. Illustration of (a) package developed for ST-5 louvers and (b) package design for MIDSTAR.

Figure 24 also shows how the new package design will thermally isolate the MEMS device. By placing the device on a suspended piece of aluminum, the thermal path from other sources other than the heater is greatly diminished. This will allow the model to more accurately reflect the actual package and device when the heater is on.

The Electronic Control Unit will also be modified in both its physical layout and its programming. The new design will use only one circuit board with a COTS microprocessor and electrical components. The new package uses a "DB 9" connecter with four lines used to communicate both ways using RS-422 protocol. The power source of 5.2 V will also use this connection. In order to implement this digital, serial connection, the microprocessor will require reprogramming. The ECU currently uses assembly language to control its connections. Switching to a RS-422 connection will allow the ability to debug any programming errors.

8. Future Work

The next generation of these devices was designed during the course of this project. Fabrication will take place at APL in the summer of 2004 and the devices will be tested using the apparatus built for testing the first generation devices. The development of the new fabrication procedure would require an iterative process, expecially for producing the intentional deformation described in section 6. In the future, it is vital to add a high emissivity coating to the device during the fabrication process. Work on aerosol spray and carbon nanotube coatings is ongoing at APL, and may be able to provide a solution to the high emissivity coating problem.

While, the Interface Control Document outlines all requirements of the package, it will still be necessary to physically build this package. The package will be worked on next year by MIDN Chris Schuster as a Bowman Scholar Project. MIDN Schuster will program the PIC microprocessor that will communicate with the satellite and collect data from the experiment. Finally, the satellite team in 2006 will place this experiment aboard MIDSTAR I.

9. Summary

This project involved the development of a satellite thermal control system component based on microelectromechanical switches. Electrostatic and thermal models for device operation were developed and confirmed with data. The results were used to develop a new, more effective thermal controller design. Finally, the integration requirements were determined for testing the system in space on the Naval Academy satellite, MIDSTAR I.

This Trident Project has had a change in focus since first described last spring. The project shifted from a single focus on the packaging of the device to working much closer with

the MEMS devices and designing a new package based on the lessons of APL's ST-5 design. There has also been a focus on modifying the fabrication process, which affects the future device design. Electromechanical and thermal models were also created to understand the MEMS performance and for future designs. The electrostatic testing confirmed the electromechanical model for the device. The results from the voltage tests are a proof of concept for the Variable Thermal Conductivity Device. The thermal models revealed that temperature differences for the current devices may be too small to measure. However, a vacuum thermal test chamber was developed for use with future devices, and emissivity data was obtained for different coatings. One aspect that was not addressed in the redesign is that of the integration of the high emissivity coating. It is a critical design parameter for these devices in the future. Without this coating, the devices will simply not function as modeled.

The fabrication process, and in particular the release issues, was the basis for the paper presented by the current author at the IEEE Photonics West Conference in January 2004, shown in Appendix C. The MEMS design and electromechanical model was the basis for the paper presented by Dr. Robert Osiander at the Space Technology and Applications International Forum in February 2004, shown in Appendix D. Finally, the thermal model was the basis for the paper that is going to be presented at the Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems in June by the current author, shown in Appendix E.

Structural changes to the package have been finalized and an Interface Control Document has been written. The MEMS device has been redesigned for better thermal properties with the fabrication process already developed during the past year. The APL team will fabricate the new device design in the summer of 2004, and prepare the device for launch on MIDSTAR I in 2006.

The project has contributed an electrostatic model and the validation of this model. A thermal model has been created that is based on a temperature change and the experimental setup has been created to validate the model. New fabrication methods were developed by the autho with the assistance of the APL staff. Finally, the groundwork for integration and testing aboard MIDSTAR I has been laid, and these devices should fly in 2006.

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Appendix A

Thermal Control Device and Electronics Control Unit (ECU) Interface Control Document

MidSTAR-1 Mission

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List of Abbreviations

ECU……Electronics Control Unit

EELV……..Evolved Expendable Launch Vehicle

ESPA……...EELV Secondary Payload Adaptor

FPGA……...Field Programmable Gate Array

MEMS…….Microelectromechanical System

MidSTAR-1……Midshipman Space Technology Applications Research

PCB…….Printed Circuit Board

PI…….Principal Investigator

SC……Spacecraft

SSP……..Small Satellite Program

TBD……To Be Determined

TCD……... Thermal Control Device

USNA……..United States Naval Academy

VDC……Voltage, Direct Current

1. INTRODUCTION

1.1. Scope

This document governs all interface issues arising from the integration of the MEMS Thermal Control Device and ECU into the Midshipman Space Technology Applications Research-I (MidSTAR-I) satellite.

1.2. Experiment Description

The ECU consists of two Printed Circuit Boards (PCBs). These boards are enclosed in an aluminum housing, 0.1068 m (4.20 in) by 0.03874 m (1.53 in) by 0.0877 m (3.45 in). The total mass is no more than 3 kg (6.6 lb). Electrical interface is via one, 9 pin connector providing a regulated voltage of 5.2 ± 0.1 V and a RS-422 serial port data connection to MIDSTAR Command and Data Handling. The ECU contains a microprocessor, voltage multipliers, and an A/D converter.

The Thermal Control Device Package (TCD), mounted external to the satellite, contains the MEMS devices that will be tested. The package dimensions are 0.1195 m (4.70 in) by 0.0163 m (0.64 in) by 0.1000 m (3.94 in). This package is connected to the ECU for power, data, and control. The TCD total mass is no more than 2 kg.

2. ADMINISTRATION

2.1. Configuration Management

This document shall be updated as needed upon agreement between the MEMS technology Principal Investigator (PI) and the Director of the USNA Small Satellite Program (SSP). New versions of the document shall be issued at their discretion.

2.2. Precedence of Documents

This document has precedence over any and all other documents dealing with interface issues. In the event that discrepancies or conflicts arise, they shall be resolved by direct negotiations between the CFTP PI and the SSP Director.

2.3. Reference Documents

Secondary Payload Planner’s Guide for Use on the EELV Secondary Payload Adaptor, Version 1.0, 8 Jun 2001.

3. INTERFACE DEFINITIONS AND DESCRIPTION

3.1. Conventions

3.1.1. Units

Units and dimensions shall be quoted in English and metric units. All values will be quoted to the following number of decimal places:

Mass (kg or lb): .x
Moments/Products of Inertia (kg-m^2 or lb-ft-s^2): .xx
Center of mass (meters): .xxxx
Center of mass (inches): .xx

The following conversion factors will be used to convert from metric to English units:

2.205 lbf = 1 kg
0.73757 lb-ft-s^2 = 1 kg-m^2 39.37 in = 1 m

Reciprocal values to the same number of decimal places will be used to convert from English to metric units.

3.1.2. Coordinate Systems

The MidSTAR-I coordinate system is consistent with the EELV Secondary Payload Adaptor (ESPA) interface and is shown in Figure 3.1.2.1.

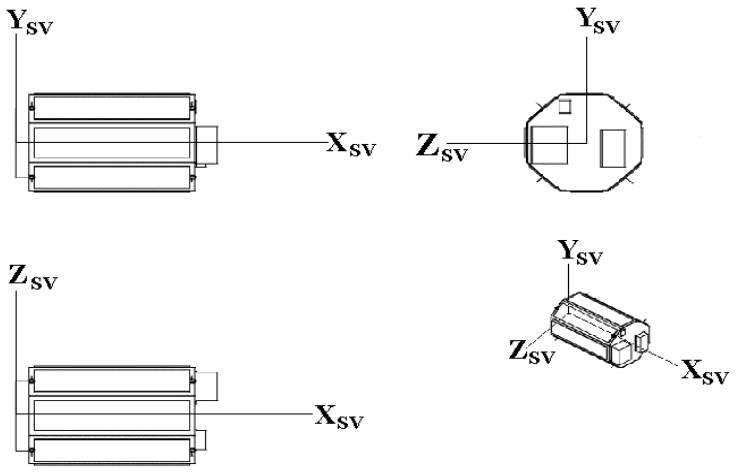
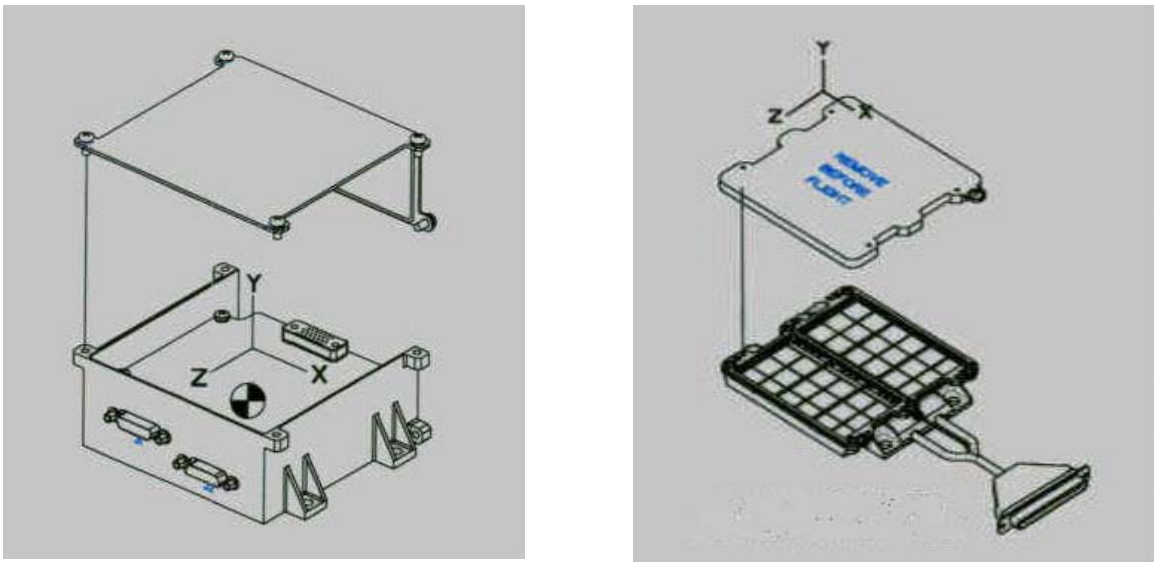


Figure 3.1.2.1 MidStar-1 Coordinate System

The ECU and TCD will use right-handed coordinate systems, shown in Figure 3.1.2.2. Each package will have their coordinate origins at their respective geometric centers. For the ECU, the x-axis is parallel to the 0.1068 m (4.20 in) side of the envelope, the y-axis is parallel to the 0.03874 m (1.53 in) side, and the z-axis is parallel to the 0.0877 m (3.45 in) side. See Attachment 1 for the ECU coordinate system. The TCD will have an x-axis parallel to the 0.1000 m (3.94 in) side, y-axis parallel to the 0.0163 m (0.64in) side, and z-axis parallel to the 0.1195 m (4.70 in).



(a) (b)

Figure 3.1.2.2. (a)EDU and (b) TCD Coordinate System

3.2. Mechanical Interfaces

3.2.1. Physical Properties

3.2.1.1. Dimensions

The ECU payload has a height of 0.03874 m (1.53 in), a width of 0.1068 m (4.20 in), and a length of 0.0877 m (3.45 in).

The TCD has a height of 0.0163 m (0.64 in), a width of 0.1000 m (3.94 in) and a length of 0.1195 m (4.70 in).

3.2.1.2. Mass

The ECU mass will not exceed 3 kg (6.6 lb).

The TCD will not exceed 1.5 kg (3.3 lb).

3.2.1.3. Center of Mass

The ECU and TCD centers of mass are +/- one inch from the center about each axis.

3.2.1.4. Moments of Inertia

The ECU coordinate system axes coincide with its principal axes.

3.2.1.5. Surface Treatments

The ECU will have an Alodine/ black anodize finish.

The TCD will have an Alodine/ bare aluminum/ clear anodize finish.

3.2.1.6. Surface Flatness

No requirements exist.

3.2.2. Mounting and Alignment

The ECU will be positioned near C&DH with 9-pin connector facing C&DH.

The TCD will be positioned on the +X face of MidSTAR-I. Place the connection face of the TCD (+x face, parallel to the z-axis) nearest the wire harness hole.

3.2.2.1. Mounting Specifications

The origin of the ECU coordinate system will be at (MIDSTAR coordinates (x,y,z): (0.0207 m (0.815 in), 0.0 m (0.0 in), 0.1928 m (7.589 in)).

The origin of the TCD coordinate system will be at (MIDSTAR coordinates (x,y,z): (0.0081 m (0.32 in), 0.0 m (0.0 in), -0.1898 m (-7.473 in)).

The x coordinates are relative to each shelf that the package is attached to. The ECU is attached to Middle Shelf. The TCD is attached to Outer Deck.

3.2.2.2. Alignment Specifications

The ECU will be aligned so that the serial ports face C&DH. The TCD will be aligned so that its connection will face the Wire Harness Hole.

3.2.2.3. Obscura

An effort should be made to place the TCD away from any object that will obscure the radiation of heat from the package. This is not a requirement but may affect experimental results.

3.2.2.4. Vent Paths

No vent path requirements exist from ECU or TCD.

3.2.3. Moving Parts and Deployment Mechanisms

The MEMS devices internal to the TCD contain moving parts. The range of motion is up to 5 micrometers in the Y direction.

3.2.4. Thermal Interfaces

3.2.4.1. Temperature Limits

The temperature limits on the ECU and the TCD are from -40˚C to 80˚C.

3.2.4.2. Temperature Monitoring Components

Temperature monitoring is essential to this experiment. Six thermistors will be placed on the TCD and will be monitored by the ECU. The thermistors will be provided by experiment team. The satellite team is only responsible for recording digital thermistor data and transmitting it to the ground station.

3.2.4.3. Thermal Control Components

The MEMS being tested are thermal control components, but are not essential to TCD survivability. No critical thermal control components are in either the ECU or the TCD. Both pieces will rely on the satellite's existing thermal control components to maintain the necessary temperature range.

3.2.5. Electrical Connections

3.2.5.1. The ECU requires one dB 9 connector originating from the C&DH.

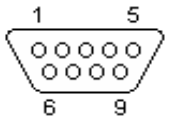
For its data connection it will use a RS-422 serial connection protocol. Two of these connections well be maintained between the ECU and C&DH, requiring four pins. The ECU power will require an additional two pins. All wires will be 24 gauge. Experiment engineers will provide both male and female interfaces.

3.2.5.2. Grounding Straps

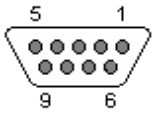
Grounding will occur through the power connection. Ground connections will occur at pins 7 and 8.

3.2.5.3. Connector Pin-outs

See Figure 3.2.5.3 for the pin-out diagrams.



DB-9 Male



DB-9 Female

Pin	Allocation
1	1 - RS-422 (+)
2	<none>
3	Power Supply (+5.2V)
4	<none>
5	2 - RS-422 (+)
6	1 - RS-422 (-)
7	Ground
8	Ground
9	2 - RS-422 (-)

Figure 3.2.5.3. Pin out Diagrams for C&DH/ECU Connection

3.2.5.4. Bonding Specifications

The ECU and TCD packages require no bonding specifications. The connectors used all require good electrical conductivity (ECU to C&DH, TCD to satellite frame, satellite frame to ECU).

3.2.5.5. Intra-payload Harness

No requirement exists.

3.2.6. Mechanical Interface Drawings

The mechanical interface drawings are Attachments 1 and 2.

3.3. Electrical Power

3.3.1. Voltage

The regulated bus voltage required is 5.2 ± 0.1 V.

3.3.2. Current

ECU:

High Voltage Generator – 1mA
Microcomputer – 8mA @ 1.3824 MHz
Program Memory (8K x 8 PROM) @ 1.3824 MHz –5mA
Analog Circuitry – 6.4mA

Estimated Average Current = 20.4mA

Maximum Current Allocated (w/o Heater) = 43.4mA average and 73mA peak.
Maximum Current Allocated (w/ Heater) = 343.3mA average and 373mA peak.

3.3.3. Power Quality

Maximum Power Allocated (w/o Heater) = 350mW.
Maximum Power Allocated (w/ Heater) = 1.850W.

3.3.4. Loads

The ECU loads are the microprocessor, the high voltage generator, the program memory, and the analog circuitry.

The TCD loads are the heater and the device actuators.

3.3.5. Grounding

Grounding will occur through the C&DH connection. Ground connections will occur at pins 7 and 8.

3.3.7. Power Draw Profiles

Table 3.3.7.1: Power Requirements

Operating Power	350mW
Peak Power	373mW
Standby Power	350mW
Survival Power	0mW
Duty Cycles	26.7%(Heater on)

Table 3.3.7.2: Schedule of Power Requirements for Each Orbit

	Orbit														
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
Thermal Control Devices	Off	On	Off	On	Off	Off	On	Off	On	Off	Off	Off	Off	Off	Off
Heater	Off	Off	On	On	Off	Off	Off	On	On	Off	Off	Off	Off	Off	Off
Electronics Power, mW	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35
Heater Power, mW	0.00	0.00	1.50	1.50	0.00	0.00	0.00	1.50	1.50	0.00	0.00	0.00	0.00	0.00	0.00
Total Power During Cycle, mW	0.35	0.35	1.85	1.85	0.35	0.35	0.35	1.85	1.85	0.35	0.35	0.35	0.35	0.35	0.35

The satellite will make 15 orbits per day, and use the last 5 (11-15) for transmitting to the base station. The heater and technology will switch on and off as shown in Table 2 so that data can be collected for both ‘hot’ and ‘cold’ levels of technology performance. This cycle will continue each day for the lifetime of the satellite or until C&DH changes the parameters mid flight.

3.4. Discrete Electrical Signals

3.4.1. Discrete Analog Inputs

No requirements exist.

3.4.2. Discrete Analog Outputs

No requirements exist.

3.4.3. Discrete Digital Inputs

Two digital inputs will be sent to the ECU from C&DH. One of these signals will tell the ECU when the heater can be activated. The second will tell the ECU when to turn the actual MEMS thermal control devices on.

3.4.4. Discrete Digital Outputs

None required for the ECU.

3.5. Serial Digital Communications

3.5.1. Input Signals

3.5.1.1. Signals Characteristics

The ECU requires RS-422 standard signal characteristics.

3.5.1.2. Command Protocols

The command protocols of the ECU will follow Internet Protocols (IP).

3.5.1.3. Data Input Protocols

Data input protocols of the ECU will follow IP.

3.5.1.4. Command Upload Protocols

Command upload protocols will follow Transfer Connect Protocol (TCP)/IP.

3.5.2. Output Signals

3.5.2.1. Signals Characteristics

The ECU will produce RS-422 standard signal characteristics.

3.5.2.2. Telemetry Output Protocols

Telemetry output protocols will follow IP.

3.5.2.3. Data Output Protocols

Data output protocols will follow TCP/IP.

Appendix B

Initial Package Design

Creating a unique package allows peak performance of the device and any necessary implications due to testing requirements. Initial concerns in designing this package included the interface between device and MIDSTAR I, the thermal properties such that the device would operate effectively, and the mechanical properties so that the device could be safely transported. The package is shown in Figure 1.

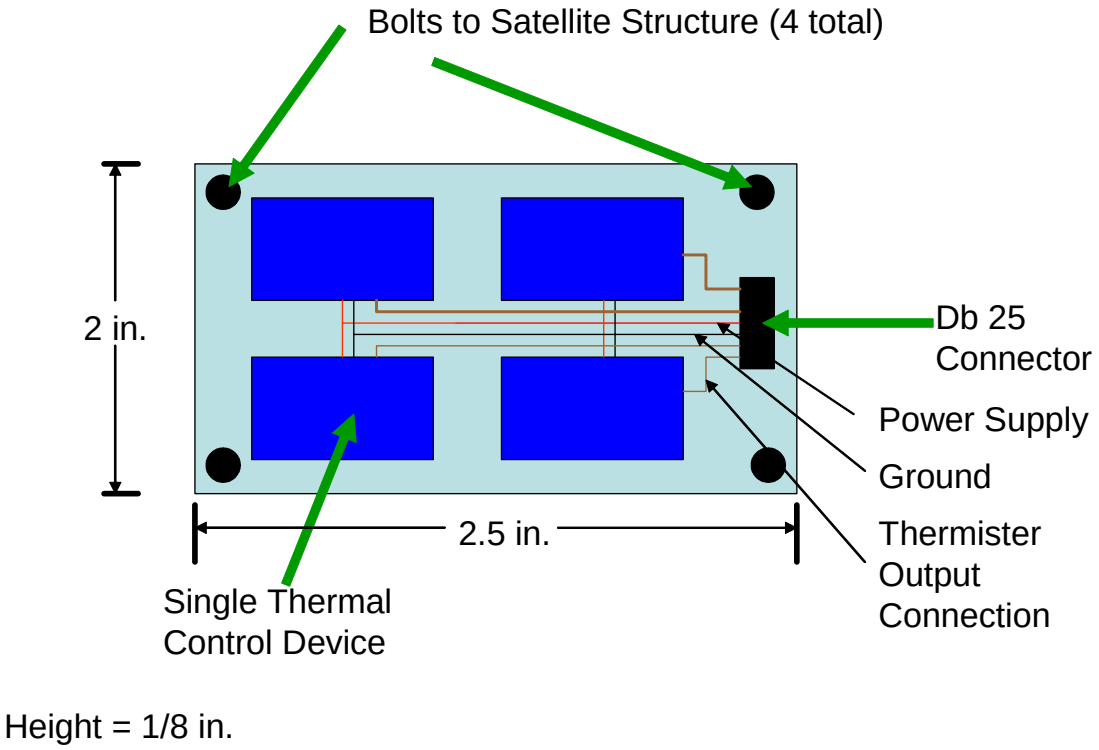


Figure 1. Initial Package Design

The number of dies to incorporate into the design was determined by the number of control lines available from MIDSTAR I. Eight control lines dictated the use of four dies. These four dies would be placed two by two in order to minimize overall package size and thereby give a greater heat flux per area when packaging is taken into consideration. The only other limit on

package size was the pin connection that would attach wires coming from the skin of the satellite to the devices inside the package. The connecter chosen was a Nanonics Military Off-the-Shelf (MOTS) connector. This 15 pin connector would actually form a section of one of the package walls.

Inside the package, the wires from the Nanonics connector would attach to a circuit board that would attach the connections to each device. The devices were sitting directly on top of the circuit board. Underneath the circuit board, a tungsten copper alloy plate would form the base of the package. The alloy was chosen due to its coefficient of expansion being close to that of the circuit board. A pure copper base would provide greater thermal conductivity, but have too large of the coefficient of expansion. The package walls were to be metal so that the materials could connect easy. Ceramic walls may cause trouble when attempting to attach them to the base. These walls would have to be coated with a non emissive surface so that heat is not able to flow out of the package regardless of the device's current operational state.

Two thermistors would be used in this design. One thermistor would measure the temperature of the copper tungsten base and the other would measure the device's silicon substrate. The copper would act as the heat source because of its large size in comparison to the size of the devices. The temperature difference would be used to measure the heat flux through the device.

The lid to the package must be transparent to the infrared spectrum, where gold radiates energy. A sapphire window was chosen because of its transparency to IR. The high cost of sapphire was acceptable because of the small package size. The window would not be hermetically sealed, allowing space to create the vacuum internal to the package. Vacuum sealing the package prior to launch would have been time consuming and unnecessary.

Appendix C

MEMS thermal switch for spacecraft thermal control

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ABSTRACT

Small satellites with their low thermal capacitance are vulnerable to rapid temperature fluctuations. Therefore, thermal control becomes important, but the limitations on mass and electrical power require new approaches. Possible solutions to actively vary the heat rejection of the satellite in response to variations in the thermal load and environmental condition are the use of variable emissivity coating (VEC), micro-machined shutters and louvers, or thermal switches. An elegant way to control radiation is to switch the thermal contact between the emitting surface and the radiator electrostatically. This paper describes the design and fabrication of an active radiator for satellite thermal control based on such a micro electromechanical (MEMS) thermal switch. The switch operates by electrostatically moving a high emissivity surface layer in and out of contact with the radiator. The electromechanical model and material considerations for the thermal design of the MEMS device are discussed. The design utilizes a highly thermal conductive gold membrane supported by low-conductance SU-8 posts. The fabrication process is described. Measured actuation voltages were consistent with the electrostatic model, ranging from 8 to 25 volts.

Keywords: Microelectromechanical devices, MEMS, Micromachining, Microfabrication, Thermal variables control, Variable emissivity, SU-8, Satellite applications

1. INTRODUCTION

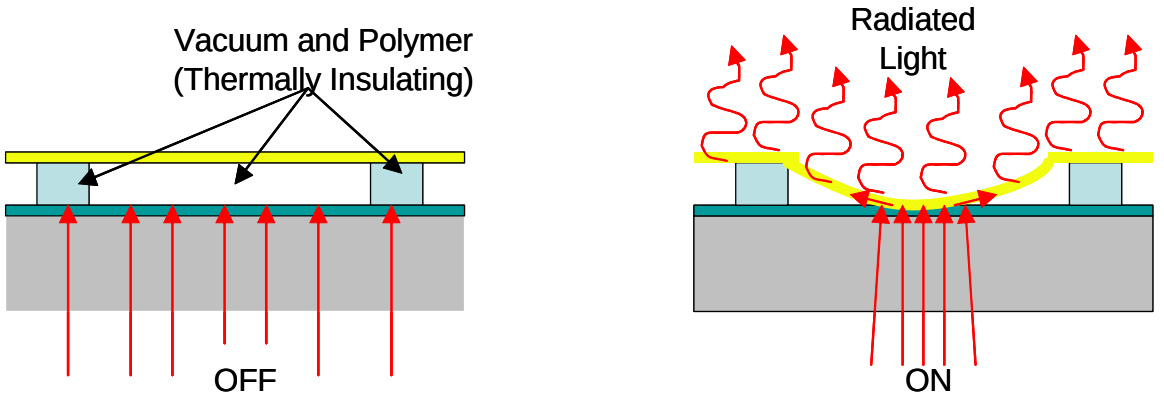
The traditional approach to spacecraft thermal control involves large radiators connected to the spacecraft by heat pipes, large and bulky thermostat controlled louver structures which allow controlling heat loss of the radiators, and power-hungry heaters which maintain the satellites operating temperature on a low offset temperature given by the radiator area. These approaches do not work anymore for small satellites below 20 kg, so-called nanosats and picosats. These satellites with their low thermal capacitance are vulnerable to rapid temperature fluctuations. Therefore, thermal control becomes important, but the limitations on mass and electrical (battery) power require new approaches[1]. One possible approach is to coat the satellite radiators with a variable emissivity coating (VEC) that can be used to actively vary the heat rejection of the satellite in response to variations in the thermal load and environmental conditions. Another way is the use micromachined louvers or shutters, which open and close the radiator substrate to space much like their macroscopic counterparts[1,2]. Such systems have been built and tested using microelectromechanical systems (MEMS). MEMS are well suited to small spacecraft; they are lightweight, low power, and relatively inexpensive to fabricate. These advantages of MEMS, including lower power and weight, have led to our past experimentation with micro fabricated louvers and shutter arrays[1,2]. Another way to control the heat loss by the radiator is the use of thermal switches to control the thermal connection to the radiator. An elegant solution is to switch the thermal contact between the emitting surface and the radiator electrostatically. This can be done on a relatively small area with very little power[1], but it requires switching voltages in the hundreds of Volts, not compatible with the power sources of small satellites. We developed a new thermal control radiator based on a MEMS thermal switch with switching voltages in the order of 20 – 30 V. Novel aspects to this design are the geometry and support structures, which are designed for low thermal conductance and low pull-in voltages, as well as the use of the polymer SU-8, a negative photoresist, that provides low thermal conductivity and good adhesion to silicon, making an ideal material for membrane support structures[3]. SU-8 has found multiple uses in MEMS particularly for high-aspect-ratio applications[4]. High-aspect ratios coupled with

deviations in thickness from 1 μm to 1 mm make SU-8 a cheap alternative to components such as cantilevers for stress sensors regularly made of silicon[4, 5].

2. THEORY

While many variable emittance coatings are based on a change of the emissivity of the radiating surface, the design of this radiator is based on a thermal switch, which connects the high emittance surface to the radiator. A thin membrane with a high emittance coating is suspended over the radiator substrate, and is, in vacuum, thermally connected to the substrate (radiator) via the small thermal conductance of the support structure and the radiative heat transfer between the substrate and the membrane. A schematic of this arrangement is shown in Figure 1. When a sufficient voltage is applied between the substrate and the membrane, the capacitive force will bend the membrane into contact with the substrate; heat will flow into the high emissivity membrane and will be radiated into space.

Using this approach to thermal control has a number of advantages. Current thermal switches, which typically connect the radiator to the spacecraft, require relatively high currents connected with a relatively low conductivity in the on state at a high weight. Similar approaches to the one described, using large suspended high emittance membranes, require much higher voltages than the satellite produces which requires additional hardware for operation. The design goal for this variable thermal conductivity device is a switching voltage that can be directly supplied by the satellite. Also, being purely electrostatic, this design requires very little power since it only draws current when changing between the on and off states.



(a) Heat Conduction and Radiation in the Off State. (b) Heat Conduction and Radiation in the On State.

Fig. 1. Principle of the Thermal Switch Radiator.

Two separate designs were explored in order to compare tradeoffs in mechanical stability versus thermal conductivity. The first device uses a polymer frame to support each membrane on all four sides. This type of structure is expected to be more resistant to damage and stiction, which can be a yield limiting problem for MEMS in which capillary forces in the drying process result in permanent contact of the mechanical structures and the surface of the substrate. The second design utilizes polymer posts to support the membrane. These posts allow a greater area of thermal contact in the on state, while they are a higher thermal resistance in the off state, thereby increasing device performance. On the other hand, the membrane has less mechanical support and may be more susceptible to damage and stiction. While only one size frame was designed, two different post designs were fabricated. One uses large posts spaced well apart, while the other uses smaller posts packed more closely together.

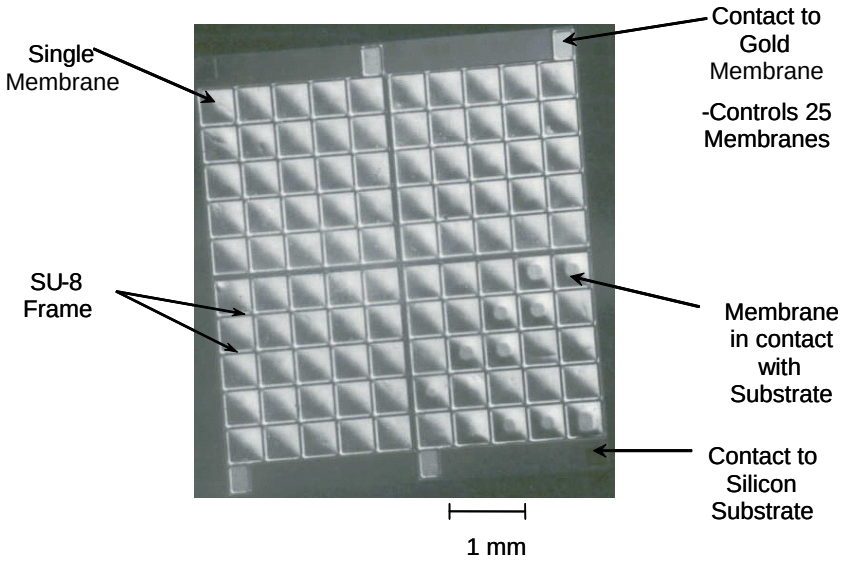


Fig. 2. Optical Microscope Image of MEMS Thermal Switch Array.

Figure 2 shows a microscope image of four 5x5 arrays of frame-type devices. Each square membrane is capable of coming into contact with the substrate. Each of the four contact pads controls the deflection of 25 membranes. Also visible in the bottom, right quadrant is the contact for the lower electrode (substrate). Figure 3 shows an optical image of the post type design. Each of the four quadrants as seen in Fig. 2 contains 64 of these 100 μm x 100 μm posts.

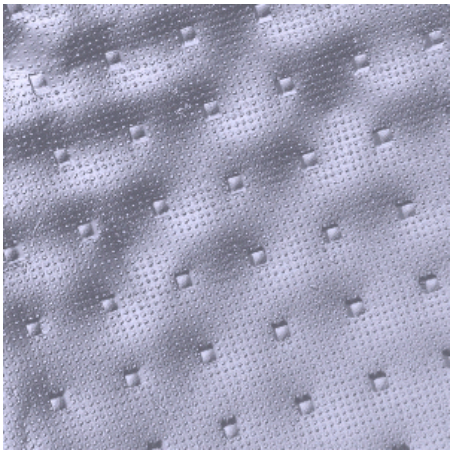


Fig. 3. Optical Profiler Image of Small Post Structure.

3. DESIGN PRINCIPLE

In choosing materials and device dimensions, one needs to address both the electromechanical design and the thermal design of the structure. The electromechanical design is a trade-off between device robustness and actuation voltage, while the thermal design is most concerned with the ratio between the thermal conductance in the on and off states, which ultimately determines the overall emissivity change.

3.1. Electromechanical Design

The actuation voltage for the device is set by the pull-in voltage. Capacitive plates such as the membranes used here are subject to a phenomenon called "pull-in." The electrostatic force on the moving plate is inversely proportional to the square of the gap, while the restoring force is proportional to the deflection. This results in an instability where the moving plate snaps down once the voltage across the plates exceeds a threshold, call the "pull-in" voltage. One goal is to design for an actuation voltage of less than 28 volts. Since many satellites supply this voltage, less signal conditioning would be necessary to drive the device.

The pull-in voltage is given by[6]

$$V_{pi} = \sqrt{\frac{8k}{27\varepsilon_0 A} g_0^3} \quad , \tag{1}$$

where V_{pi} is the pull-in voltage (V), k is the spring constant (N/m), g_0 is the gap at zero bias (m), ε_0 is the permittivity of free space (F/m), and A is the area of the electrode (m^2).

In order to find the spring constant, the device will be approximated by a circular diaphragm of equal area, with spring constant is given by[6]

$$k = \frac{16\pi^2 E t^3}{3A(1-\nu^2)} + 4\pi\sigma t \quad , \tag{2}$$

where E is Youngs modulus of the membrane (Pa), t is the membrane thickness (m), A is the area of the membrane (m^2), ν is Poisson's ratio, and σ is the biaxial residual stress (Pa). The theoretical values for V_{pi} are shown in Table 2. Post design 2 was designed for a much higher actuation voltage for comparison. The higher voltage design should be more rugged because of the higher spring constant.

3.2. Thermal Design

Assuming a high-emissivity coating at the top surface of the device, the difference in heat radiation between the two states is dependent on the difference in the thermal conduction from the substrate to the membrane for the two states. Our goal is to maximize the conductivity ratio while maintaining a robust design and reasonable actuation voltages. Heat flow, Q, through a space of thickness h and area A is related to the temperature difference ΔT and thermal conductivity k_{th} by the following relationship:

$$Q = Ak_{th}\frac{\Delta T}{h} \quad . \tag{3}$$

In the off-state, the rate-limiting step for conduction is the conduction through the polymer posts. In the on-state assuming a good contact at the membrane-substrate interface, the rate-limiting step is set by conduction through the gold layer. Therefore, the ratio of conduction in the on-state to conduction in the off-state is given by:

$$\frac{Q_{on}}{Q_{off}} \propto \frac{A_{contact}}{A_{post}} \times \frac{k_{th,mem}}{k_{th,post}} \times \frac{h_{post}}{h_{mem}} \quad , \tag{4}$$

where $A_{contact}$ is the membrane area that comes into contact with the substrate when a voltage is applied, A_{post} is the post area, $k_{th,mem}$ is the thermal conductivity of the membrane material, $k_{th,post}$ is the thermal conductivity of the post material, h_{post} is the height of the post and h_{mem} is the thickness of the membrane. This expression gives the best case performance ratio. In reality, the contact conductance in the on state will degrade the overall conductance ratio (Song, 2002). Furthermore, if the emissivity ε of the membrane is low (ε<1), radiation will limit heat transfer instead of conduction at the interface. We are developing a more complete thermal model for the device, which takes into account the interface conductance and the emissivity of the top surface.

3.2. Material Considerations

In order to optimize thermal performance, (4) indicates that we should maximize the ratio of the conductivity of the membrane material to that of the post material. Typically, surface micromachining processes utilize polysilicon, silicon dioxide or silicon nitride as the post or anchor material. However, as can be seen in Table 1, the use of SU-8 can provide a 5-fold improvement over silicon dioxide, and a 150-fold improvement over silicon nitride. SU-8 is also a photoresist and can therefore easily be incorporated into the fabrication process.

We selected gold for our membrane material because of its relatively low Young's modulus, which results in a smaller spring constant and therefore a lower pull-in voltage, as well as its high reflectivity to IR, which prevents radiation from underlying surfaces from escaping the structure.

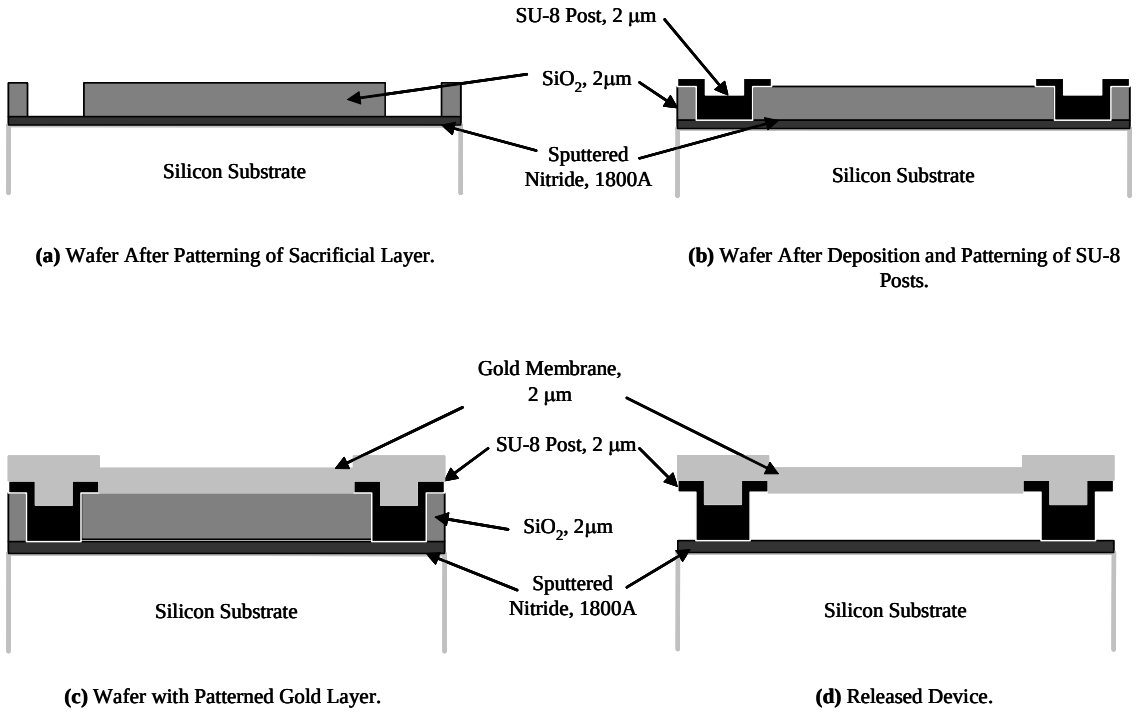
TABLE 1. Relevant Material Properties for Design.

Property	**Au**	**SU-8**[7]	**SiO_2**	**SiN**
k_{th}	320 W/mK	0.2 W/mK	1.1 W/mK	30.1 W/mK
E	80 GPa	---	---	---
ν	0.42	---	---	---
σ	+10 MPa	---	---	---

4. FABRICATION PROCESS

The fabrication sequence for the thermal switch is illustrated in Figure 1. The switch was fabricated on an n-type (.005-.020 Ω-cm) silicon substrate that serves as the lower electrode for device control. A thin (1800Å) layer of silicon nitride was first deposited onto the substrate to form an insulator between the substrate and membrane when the device is in the on state. A 2 μm thick layer of silicon dioxide was then deposited and patterned to form openings where the supports for the suspended membrane would be located. A 2 μm thick layer of SU-8 resist, a photosensitive, epoxy-based polymer, was then applied and patterned to form the support structures. SU-8 was chosen because its low thermal conductivity reduces the rate of heat flow to the membrane in the off position, and because it can readily be patterned using standard photolithographic techniques.

Next, an adhesion layer of titanium-tungsten (300Å) and a seed layer of gold (1,000 Å) were sputtered across the wafer. The wafer was then patterned and additional gold was electroplated to a final thickness of 2 μm. The pattern used to electroplate the membrane included an array of 5 μm diameter "release holes" spaced 25 μm apart that were not plated with the thicker gold. The thinner metal in these areas was then removed by etching the gold seed layer in a commercially available, cyanide-based solution, and by etching the titanium-tungsten in hydrogen peroxide at 50°C. Once these penetrations through the membrane were opened, the sacrificial oxide layer beneath the membrane was removed in concentrated hydrofluoric acid, leaving the gold membrane suspended above the surface of the substrate. Finally, the titanium-tungsten layer on the underside of the membrane was removed using hydrogen peroxide.



(a) Wafer After Patterning of Sacrificial Layer.

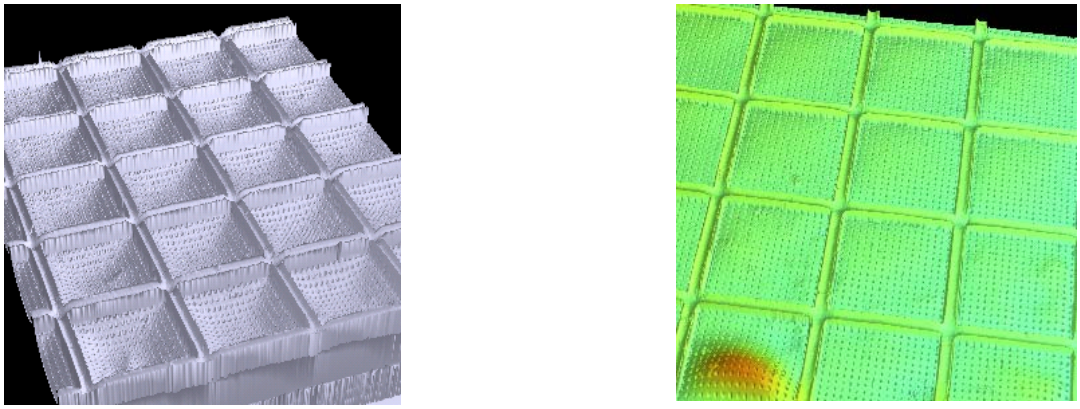
(b) Wafer After Deposition and Patterning of SU-8 Posts.

(c) Wafer with Patterned Gold Layer.

(d) Released Device.

Fig. 4. Illustrations of Fabrication Steps.

This final step was required in order to minimize the residual stress of the completed membrane. Although the layer of titanium-tungsten is very thin in comparison to the overall thickness of the membrane, measurements have shown that this material is under high compressive stress (about -1975 MPa). This results in a large and undesirable initial deformation of the membrane. Removing this thin layer produces a final membrane that is relatively flat and has a residual stress that is only slightly tensile (about 10 MPa). This effect can clearly be seen in Figure 2.



(a) **(b)**

Fig. 5. 3-D Renderings from Optical Profiler Scans of Identical Devices Before (a) and After (b) Removal of the Adhesion Layer Beneath the Membranes.

5. RESULTS

After fabrication, we examined the devices, as seen in figure 5, with an optical profiler allowing us to measure final device dimensions. Pull-in voltage testing was conducted on the devices. The pull-in voltage testing occurred in air at standard temperature and pressure ($\varepsilon_{air} = 1.00054\varepsilon_0$). Table 2 shows the effects that the sagging membrane had on pull in voltage requirements. According to equation (1), V_{pi} is directly proportional to the effective initial gap, g_o, raised to the three halves power. Therefore, the small variation in gap height due to sagging resulted in wide variations in pull-in voltage. Furthermore, once a few membranes in an array have pulled in it becomes difficult to further increase the voltage on the entire array because the device becomes more prone to dielectric breakdown. The removal of the TiW layer, in addition to eliminating the sagging effect, also produces a more uniform membrane resulting in more uniform activation voltages. The frame designs proved to be the most consistent. These devices showed a much smaller degree of variation in g_0.

TABLE 2. Device Dimensions and Resultant Voltages.

Design	Membrane Thickness	Effective Membrane Width	Conduction Ratio	With Adhesion Layer			Without Adhesion Layer	
				Effective Initial Gap	Theoretical Pull-in Voltage	Meas. Pull-in Voltage	Theoretical Pull-in Voltage	Meas. Pull-in Voltage
Post Design 1	**2 µm**	**550 µm**	**20,000**	**0.8 µm**	**5.1 V**	**7-12 V**	**20.0 V**	**--**
Post Design 2	**2 µm**	**300 µm**	**13,000**	**1.5 - 1.8 µm**	**57.9 – 73.6 V**	**18 – 25+ V**	**89.2 V**	**--**
Frame Design	**2 µm**	**400 µm**	**3,000**	**0.6 µm**	**11.5 V**	**9 – 11 V**	**28.2 V**	**20-25 V**

6. CONCLUSIONS

A MEMS-based device capable of switching thermal conductivity as a means to control heat radiation has been designed and fabricated. The electromechanical performance of the device is consistent with theory. We have demonstrated device pull-in voltages that are compatible with space-craft voltage resources. The fabrication process has succeeded in producing testable, working devices. Future efforts will focus on verifying the thermal performance of these devices and developing a technique for the attachment of a high emissivity coating.

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Appendix D

Microfabricated Thermal Switches for Emittance Control

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Abstract. The trend to smaller satellites with limited resources in weight and power requires a new approach to thermal control. This paper describes an actively controlled radiator based on a micro electromechanical (MEMS) thermal switch. The switch operates by electrostatically switching in and out of contact with the radiator. The thermal and electromechanical design of the MEMS device is discussed. A proof-of-concept design has been fabricated that uses a gold membrane suspended on polymer posts. In the open position, actuation voltages range from 8 to 25 volts; this was consistent with our electromechanical model for the devices.

INTRODUCTION

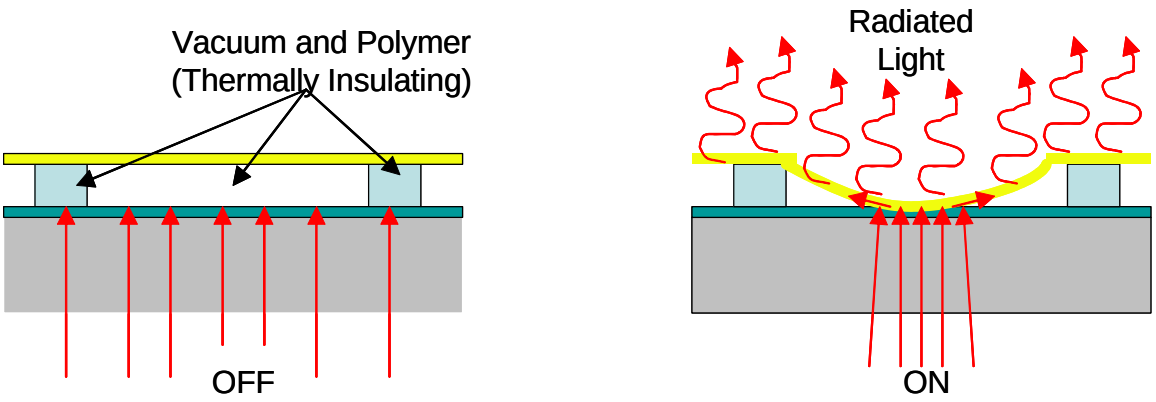
The use of nano- and pico-satellites in present and future space missions requires a new approach to thermal control. Small spacecraft have low thermal capacitance, making them vulnerable to rapid temperature fluctuations. At the same time, traditional thermal control technologies such as heaters, thermostats, and heat pipes do not scale well to meet the constrained power and mass budgets of smaller satellites (Douglas, 2001). One approach is to coat the satellite radiators with a variable emissivity coating (VEC) that can be used to actively vary the heat rejection of the satellite in response to variations in the thermal load and environmental conditions. One way to create such a coating is the use of micro-electromechanical systems (MEMS). MEMS utilize integrated circuit fabrication technology to create controllable, mechanical structures that perform the same tasks as much larger devices, all on a microchip. By uniting macro-scale systems with batch-fabrication techniques and scalability, MEMS deliver the same results at a lower cost (Judy, 2001). MEMS are well suited to small spacecraft; they are lightweight, low power, and relatively inexpensive to fabricate (de Aragón, 1998). These properties have led to our past experimentation with microfabricated louvers and shutter arrays (Champion, 1999)(Douglas, 2001).

OPERATION PRINCIPLE

While many variable emittance coatings are based on a change of the emissivity of the radiating surface, the design of this radiator is based on a thermal switch, which connects the high emittance surface to the radiator. A thin membrane with a high emittance coating is suspended over the radiator substrate, and is, in vacuum, thermally connected to the substrate (radiator) via only the small residual thermal conductance of the support structure and the radiative heat transfer between the substrate and the membrane. A schematic of this arrangement is shown in Figure 1. When a sufficient voltage is applied between the substrate and the membrane, the capacitive force will bend the membrane into contact with the substrate; heat will flow into the high emissivity membrane and will be radiated into space.

Using this approach to thermal control has a number of advantages. Current thermal switches, which typically connect the radiator to the spacecraft, require relatively high currents connected with a relatively low conductivity in the on state at a high weight. Similar approaches to the one described, using large suspended high emittance membranes, require much higher voltages than the satellite produces which requires additional hardware for operation. The design goal for this variable thermal conductivity device is a switching voltage that can be directly supplied by the satellite. Also, being purely electrostatic, this design requires very little power since it only draws

current when changing between the on and off states. Finally, MEMS utilize integrated circuit fabrication methods that allow batch manufacturing.



(a) Heat Conduction and Radiation in the Off State. **(b)** Heat Conduction and Radiation in the On State.

FIGURE 1. Principle of the Thermal Switch Radiator.

Two separate designs were explored in order to compare tradeoffs in mechanical stability versus thermal conductivity. The first device uses a polymer frame to support each membrane on all four sides. This type of structure is expected to be more resistant to damage and stiction, which can be a yield limiting problem for MEMS in which capillary forces in the drying process result in permanent contact of the mechanical structures and the surface of the substrate. The second design utilizes polymer posts to support the membrane. These posts allow a greater area of thermal contact, thereby increasing device performance. On the other hand, the membrane has less mechanical support and may be more susceptible to damage and stiction. While only one size frame was designed, two different post designs were fabricated. One uses large posts spaced well apart, while the other uses smaller posts packed more closely together.

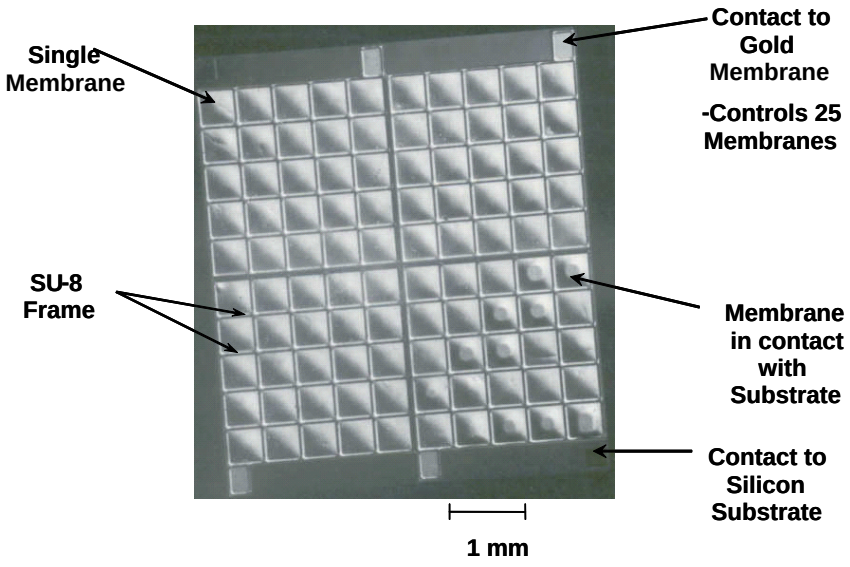


FIGURE 2. Optical Microscope Image of MEMS Thermal Switch Array.

Figure 2 shows a microscope image of four 5x5 arrays of frame-type devices. Each square membrane is capable of coming into contact with the substrate. Each of the four contact pads controls the deflection of 25 membranes. Also visible in the bottom, right quadrant is the contact for the lower electrode (substrate). Figure 3 shows an optical

image of the post type design. Each of the four quadrants as seen in Fig. 2 contains 64 of these 250 µm x 250 µm posts.

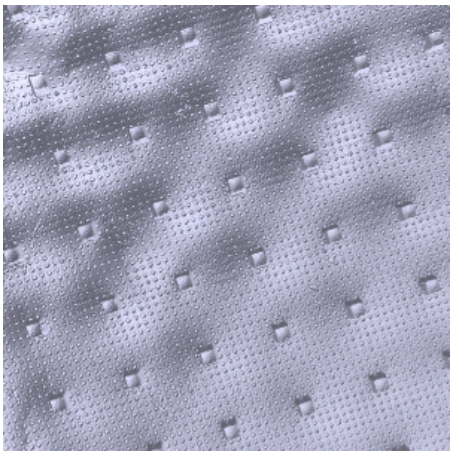


FIGURE 3. Optical Profiler Image of Small Post Structure.

DEVICE DESIGN

In choosing materials and device dimensions, one needs to address both the electromechanical design and the thermal design of the structure. The electromechanical design is a trade-off between device robustness and actuation voltage, while the thermal design is most concerned with the ratio between the thermal conductance in the on and off states, which ultimately determines the overall emissivity change.

Electromechanical Design

The actuation voltage for the device is set by the pull-in voltage. Capacitive plates such as the membranes used here are subject to a phenomenon called "pull-in." The electrostatic force on the moving plate is inversely proportional to the square of the gap, while the restoring force is proportional to the deflection. This results in an instability where the moving plate snaps down once the voltage across the plates exceeds a threshold, call the "pull-in" voltage. One goal is to design for an actuation voltage of less than 28 volts. Since many satellites supply this voltage, less signal conditioning would be necessary to drive the device.

The pull-in voltage is given by (Rebeiz, 2003)

$$V_{pi} = \sqrt{\frac{8k}{27\varepsilon_0 A} g_0^3} \quad , \tag{1}$$

where V_{pi} is the pull-in voltage (V), k is the spring constant (N/m), g_0 is the gap at zero bias (m), ε_0 is the permittivity of free space (F/m), and A is the area of the electrode (m^2).

In order to find the spring constant, the device will be approximated by a circular diaphragm of equal area, with spring constant is given by (Rebeiz, 2003)

$$k = \frac{16\pi^2 E t^3}{3A(1-\nu^2)} + 4\pi\sigma t \quad , \tag{2}$$

where E is Youngs modulus of the membrane (Pa), t is the membrane thickness (m), A is the area of the membrane (m^2), ν is Poisson's ratio, and σ is the biaxial residual stress (Pa). The theoretical values for Vpi are shown in Table 2. Post design 2 was designed with a much higher voltage in order to test the possible of effects of using lower

voltages. The higher voltage should prove to be a more rugged design because a greater force is required for deflection of the membrane.

Thermal Design

Assuming a high-emissivity coating at the top surface of the device, the difference in heat radiation between the two states is dependent on the difference in the thermal conduction from the substrate to the membrane for the two states. Our goal is to maximize the conductivity ratio while maintaining a robust design and reasonable actuation voltages. Heat flow, Q, through a space of thickness h and area A is related to the temperature difference ΔT and thermal conductivity k_{th} by the following relationship:

$$Q = Ak_{th}\frac{\Delta T}{h} \quad . \tag{3}$$

In the off-state, the rate-limiting step for conduction is the conduction through the polymer posts. In the on-state assuming a good contact at the membrane-substrate interface, the rate-limiting step is set by conduction through the gold layer. Therefore, the ratio of conduction in the on-state to conduction in the off-state is given by:

$$\frac{Q_{on}}{Q_{off}} \propto \frac{A_{contact}}{A_{post}} \times \frac{k_{th,mem}}{k_{th,post}} \times \frac{h_{post}}{h_{mem}} \quad , \tag{4}$$

where $A_{contact}$ is the membrane area that comes into contact with the substrate when a voltage is applied, A_{post} is the post area, $k_{th,mem}$ is the thermal conductivity of the membrane material, $k_{th,post}$ is the thermal conductivity of the post material, h_{post} is the height of the post and h_{mem} is the thickness of the membrane. This expression gives the best case performance ratio. In reality, the contact conductance in the on state will degrade the overall conductance ratio (Song, 2002). Furthermore, if the emissivity ε of the membrane is low (ε<1), radiation will limit heat transfer instead of conduction at the interface. We are developing a more complete thermal model for the device, which takes into account the interface conductance and the emissivity of the top surface.

Material Selection and Fabrication

The materials used for this device allow high thermal insulation in the off state, and high emittance for high radiation when on. A cross-section of the thermal switch is shown schematically in Figure 4. The switches are fabricated on low resistivity silicon that forms the bottom electrode of the device. A thin, insulating layer of silicon nitride over the surface of the silicon serves to electrically isolate the membrane from the substrate when the switch is in the on state. We selected gold for the membrane material because it is fairly easy to deposit and has desirable mechanical and optical properties in this application. Being malleable allows the gold to bend without permanent deformation. Since gold also has a high reflectivity and low emissivity, emissions from below the membrane are reflected back to the substrate. In addition, gold may allow the selective attachment of a high emissivity coating layer in post-processing. The gold membrane is left suspended above the surface of the substrate by depositing over a sacrificial layer of silicon dioxide that is removed at the end of the fabrication process.

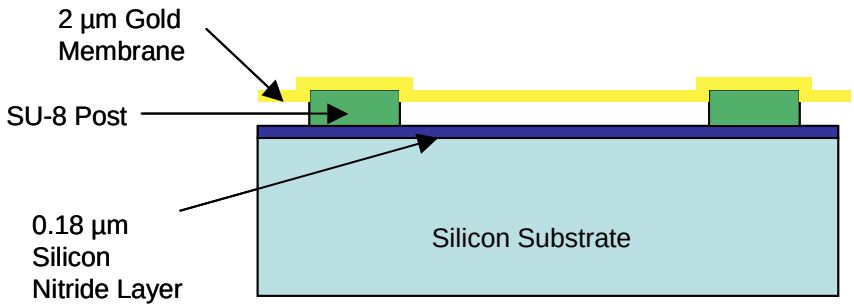


FIGURE 4. Material Dimensions of Device.

From (4) it can be seen that for good thermal performance it is desirable for the posts to be small and sparsely placed, and that they be made of a material with a much lower thermal conductivity than the membrane material. For this purpose, we used SU-8, an epoxy-based polymer that is typically used as a photoresist. When fully cured, this material has a thermal conductivity that is lower than that of common inorganic insulator materials, such as silicon dioxide and silicon nitride, which are typically used in microfabrication. The relevant properties for the materials selected are listed in the table below. Figure 5 shows a SEM image of the completed structure illustrating the release holes that facilitate the removal of the sacrificial oxide layer beneath the membrane.

TABLE 1. Relevant Material Properties for Design.

Property	Au	SU-8[†]	SiO_2	SiN
k_{th}	320 W/mK	0.2 W/mK	1.1 W/mK	30.1 W/mK
E	80 GPa	---	---	---
ν	0.42	---	---	---
σ	+10 MPa	---	---	---

[†] Shaw, 2000

As previously discussed, we experimented with three different membrane designs. Two of the designs used posts to provide a larger area ratio for better thermal performance. One of these designs was tailored to have an actuation voltage of less than 28 V, which will require less signal conditioning on board of a satellite. However, such a device may be more susceptible to failure during fabrication due to the small spring constant and large, unsupported area of the membrane. Therefore we also explored a "frame" design in which the membranes are mechanically isolated from one another. This design is expected to be much more robust, but have poorer thermal performance. The three designs are summarized in Table 2. The conduction ratio assumes that 50% of the membrane comes into contact during actuation.

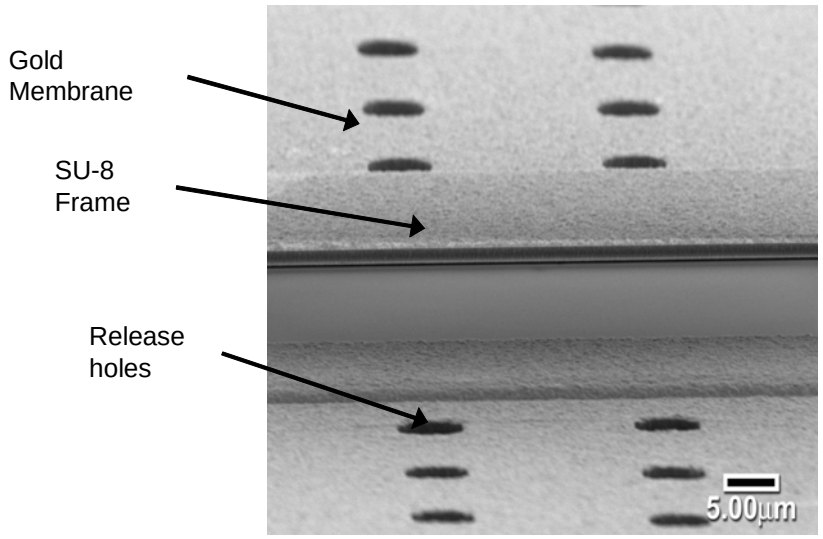


FIGURE 5. SEM Picture of Device Taken Almost Parallel to Gold Membrane.

RESULTS

After fabrication, we examined the devices, figures 2, 3, and 5, with an optical profiler allowing us to measure final device dimensions. Pull-in voltage testing was conducted on devices with measured gap heights, $g_{0,}$ of 2µm and

0.6μm. The pull-in voltage testing occurred in air at standard temperature and pressure ($\varepsilon_{air} = 1.00054\varepsilon_0$). These values are very close to the anticipated voltage levels and confirm our electromechanical model for the membrane behavior. Table two shows that experimentally measured pull-in voltages were very close to those predicted by our electromechanical model. According to equation (1), V_{pi} is directly proportional to the effective initial gap, g_0, raised to the three halves power. This shows that a wide range of voltages can be measured with only a small difference in g_0. Both post designs have not yet been fabricated with a g_0 equal to 2 μm. The largest error occurs in the testing of post design 2, the small posts. This is because g_0 varied greatly in the samples tested. While only a fraction of the membranes would activate at the 18-22 V range, more voltage could not be applied without damage to the membrane. The frame designs proved to be the most accurate. These devices showed a much smaller degree of variation in g_0.

TABLE 2. Device Dimensions and Resultant Voltages.

Design	Effective Initial Gap	Membrane Thickness	Effective Membrane Width	Theoretical Pull-in Voltage	Experimental Pull-in Voltage	Conduction Ratio
Post Design 1	**0.8 μm**	**2 μm**	**550 μm**	**5.1 V**	**7-12 V**	**20,000**
Post Design 1	**2 μm**	**2 μm**	**550 μm**	**20.0 V**	**--**	**20,000**
Post Design 2	**1.5 - 1.8 μm**	**2 μm**	**300 μm**	**57.9 - 73.6 V**	**18-22V**	**13,000**
Post Design 2	**2 μm**	**2 μm**	**300 μm**	**89.2 V**	**--**	**13,000**
Frame Design	**0.6μm**	**2 μm**	**400 μm**	**11.5 V**	**9-11 V**	**3,000**
Frame Design	**2 μm**	**2 μm**	**400 μm**	**28.2 V**	**20-25 V**	**3,000**

CONCLUSION

MEMS technology offers a potential means of satellite thermal control. A MEMS-based device capable of varying thermal conductivity as a means to control heat radiation has been designed and fabricated. The electromechanical performance of the device is consistent with theory. We have demonstrated device pull-in voltages are compatible with space-craft voltage resources. Future efforts will focus on verifying the thermal performance of these devices and developing a technique for the attachment of a high emissivity coating. We plan to test a radiator with these devices aboard the United States Naval Academy satellite, MIDSTAR I, which is set to launch in 2006.

ACKNOWLEGMENTS

The authors wish to acknowledge the help of the staff at Johns Hopkins University Applied Physics Laboratory, the USNA satellite team, and the Trident Scholar Program Committee.

NOMENCLATURE

V_{pi} = pull-in voltage (V)
k = spring constant (N/m)
g_0 = zero bias bridge height (m)
ε_0 = permittivity of free space (F/m)
A = area of membrane (m^2)
E = Young's modulus of gold membrane (Pa)
t = membrane thickness (m)
σ = biaxial residual stress (Pa)
ν = Poisson's ratio
ρ = resistivity (Ωcm)

Q = heat flow (W)
k_{th} = thermal conductivity (W/(mK))
T = temperature (K)
h = thickness of material (m)

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Appendix E

DESIGN AND PACKAGING FOR A MICROELECTROMECHANICAL THERMAL SWITCH RADIATOR

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ABSTRACT

Smaller satellites will require low-power, lightweight thermal control. This paper describes a technology based on a thermal switch which controls the conductivity between the radiator and a highly-emissive surface. The device is going to be tested aboard MIDSTAR 1, a small satellite that is being designed and built by students at the United States Naval Academy. This paper presents a discussion of the device design, and a detailed thermal analysis that shows how the power dissipation for the device relates to design parameters. The package and testing procedure are also described.

KEY WORDS: microelectromechanical system, satellite thermal control, thermal model, package design.

NOMENCLATURE

A	area, m^2
C	thermal capacitance, J/K
E	Youngs modulus, Pa
g_o	initial gap height, m
G	thermal conductivity, W/K
h	layer thickness, m
k	spring constant, N/m
k_{th}	thermal conductivity, W/(m-K)
Q	heat flow, W
T	temperature, K
t	time, s
V	Voltage, V

Greek symbols

ε	emissivity
ν	Poisson's ratio
σ	Stefan-Boltzman constant, $W/m^2\text{-}K^4$

Subscripts

0	satellite
1	radiator
2	gold membrane
pi	pull-in
t	thermal
var	variable thermal conductivity layer
eff	effective

INTRODUCTION

The planned use of constellations of nano- and pico-satellites in future space missions requires new thermal control methods for handling rapidly varying thermal environments. Traditional thermal control technologies such as heaters, thermostats, and heat pipes do not have the flexibility required, and in addition do not scale well to meet the constrained power and mass budgets of smaller satellites [1]. One approach is the use of variable emissivity coating in order to actively vary the heat rejection of the satellite radiator in response to variations in the thermal load and environmental conditions. In the past, we have examined a variety of approaches such as micromachined louvers and shutter arrays [1, 2] to vary the emissivity of a radiator surface.

Fig.1: Optical image of louver array, with louvers all in closed position.

While these approaches and many other variable emittance coatings are based on a change of the emissivity of the radiating surface, we are presenting a radiator design based on a micromachined thermal switch that connects the high emittance surface to the radiator. A thin membrane with a high emittance coating is suspended over the radiator substrate, and is, in vacuum, thermally connected to the substrate (radiator) via the small residual thermal conductance of the support structure and the radiative heat transfer between the substrate and the membrane. A schematic of this arrangement is shown in Fig. 2. When a sufficient voltage is applied between the substrate and the membrane, the capacitive force will bend the membrane into contact with the substrate; heat will flow into the high emissivity membrane and will be radiated into space.

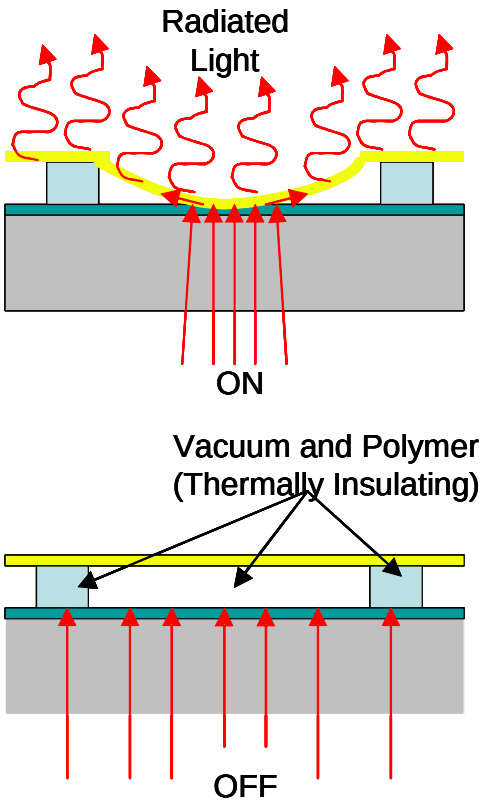

Fig. 2 Operation Principle of the Thermal Switch Radiator

Using this approach to thermal control has a number of advantages. Current thermal switches, which typically connect the radiator to the spacecraft, require relatively high currents for the actuators, connected with a relatively low conductance in the on state at a high weight. Similar approaches to the one described [3], using large suspended high emittance membranes, require much higher voltages than the satellite produces which requires additional hardware for operation. We have previously shown [4,5], that with this microfabricated approach we can achieve a switching voltage that can be directly supplied by the satellite. Also, being purely electrostatic, this design requires very little power since it only draws current when changing between the on and off states. Figure 3 shows a microscope image of four 5x5 arrays of devices. Each of the four contact pads controls the deflection of 25 membranes. Also visible in the bottom, right quadrant is the contact for the lower electrode (substrate).

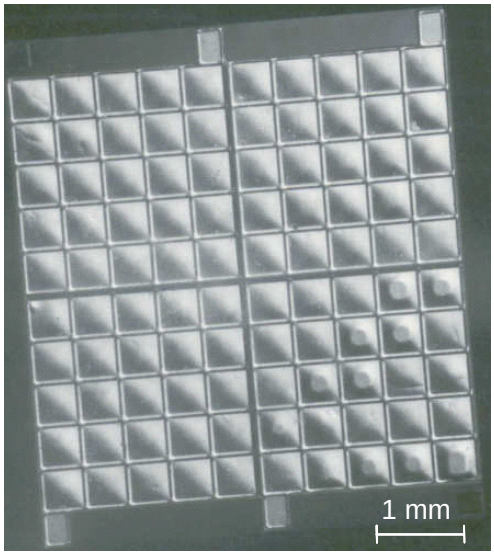

Fig. 3 Optical Microscope Image of Thermal Switch Array

This paper presents a more detailed thermal model of the device. This device is going to be tested on MIDSTAR 1, which is a small satellite launched by the United States Naval Academy. With a mass of 90 kilograms, MIDSTAR offers a platform that shows future promise of being thermally controlled by MEMS devices. The satellite's bus voltage of 18 Volts is also near the level required to operate the devices allowing for easier integration. The package designs for the device aboard MIDSTAR are described.

DESIGN

The electromechanical design of the device represents a trade-off between device robustness and actuation voltage, while the thermal design is most concerned with the ratio between the thermal conductance in the on and off states, which ultimately determines the overall emissivity change. Both aspects of the design are described below.

Electromechanical Design

The actuation voltage for the device is set by the pull-in voltage between capacitive plates such as the membranes used here. The electrostatic force on the moving plate is inversely proportional to the square of the gap, while the restoring force is proportional to the deflection. This results in an instability where the moving plate snaps down once the voltage across the plates exceeds a threshold, call the "pull-in" voltage. One goal is to design for an actuation voltage of less than 28 volts. Since many satellites supply this voltage, less signal conditioning would be necessary to drive the device.

The pull-in voltage is given by [6]:

$$V_{pi} = \sqrt{\frac{8k}{27\varepsilon_0 A} g_0^3} \quad \textbf{(1)}$$

where V_{pi} is the pull-in voltage (V), k is the spring constant (N/m), g_0 is the gap at zero bias (m), ε_0 is the permittivity of free space (F/m), and A is the area of the electrode (m^2).

In order to find the spring constant, the device will be approximated by a circular diaphragm of equal area, with spring constant is given by [6]

$$k = \frac{16\pi^2 E h^3}{3A(1-\nu^2)} + 4\pi\sigma h \quad \textbf{(2)}$$

where E is Young's modulus of the membrane (Pa), h is the membrane thickness (m), A is the area of the membrane (m^2), ν is Poisson's ratio, and σ is the biaxial residual stress (Pa). The relevant structural properties of gold, which was the material used for our membranes, is summarized in Table 1.

Table 1. Relevant Material Properties for Design.

Property	Au	Poly-Si	NANO™ SU-8[i]	SiO_2	SiN
k_{th} (W/mK)	320	20-50	0.2	1.1	30.1
E (Gpa)	80	170	---	---	---
ν	0.42	0.22	---	---	---
σ (Mpa)	+10	-10-15	---	---	---

Thermal Design

This device is a variable conductance radiator, and as such insulates the satellite in the off position from the radiating surface. The key parameter for the system is G_{var}, the thermal conductance between the substrate and the membrane material. In a lumped thermal model, conductance for a slab of material is related to geometry and material properties by:

$$G = \frac{k_{th} A_{eff}}{h_{eff}} \quad \textbf{(3)}$$

where k_{th} is the thermal conductivity, A_{eff} is the effective area and h_{eff} is the effective thickness of the material.

In the *off* state for this device, heat travels from the substrate to the membrane via the small posts, which are made out of a material with a low thermal conductivity. We chose SU8, which is a photodefinable epoxy, for the post material. The effective area in this case is given by the total device area multiplied by a fill factor that captures the area of the posts relative to the total device area. Radiative heat transfer from the silicon nitride to the gold membrane is negligible.

In the *on* position, a conduction path is created by bringing the gold membrane into physical contact with the substrate and the SiN coating. For this state, heat conduction is dominated by the contact conductance between gold and silicon nitride [7], which depends on the effective area of the contact and the closing force. This force, in turn, depends on the voltage applied, the spring constant of the membrane, and the dielectric constant of silicon nitride. It has been shown that in microstructures, thermal conductance between interfaces is higher in a vacuum than in air. Air impedes the contact instead of supplying an alternate path of conduction as in seen on the macro- scale. The low relative roughness of the gold membrane has also been shown to increase thermal interface conductance [7]. Figure 4 shows a schematic for the different heat flows throughout the device in the off and on positions.

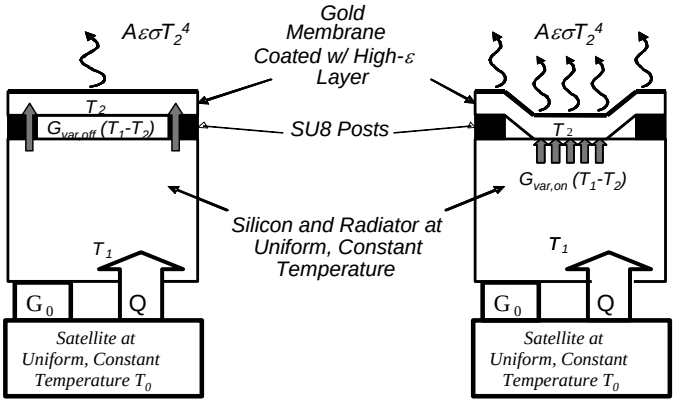

Fig. 4 Illustration of heat flows in (a) off mode and (b) on mode.

The radiator structure and silicon substrate are assumed to be at a uniform temperature T_1 while the gold membrane is at temperature T_2. Heat is radiated from the gold membrane via the high emissivity coating. In either operation mode, the energy equation for the gold membrane is [8]:

$$G_{\text{var}}(T_1 - T_2) - A\varepsilon\sigma T_2^4 = C_2 \frac{dT_2}{dt} \quad \textbf{(3)}$$

where G_{var} is the thermal conductivity (W/K) of the interface layer between the silicon layer and gold membrane. G_{var} depends on the device state in the manner discussed above.

T_1 is the temperature of the silicon layer and the radiator (K) and is assumed to be uniform because of the relatively high thermal conductivities of the materials involved as well as the relative thickness of the layers. T_2 is the temperature of the gold membrane (K). A is the area of the radiating surface, (m^2). The emissivity of the surface and the Stefan-Boltzmann constant is given by ε and σ, respectively. C_2 is the thermal capacitance of the gold membrane, (J/K). All heat is modeled to conduct vertically, not radiating from the sides of the layers.

The satellite is at a fixed temperature T_0 and is connected to the radiator/silicon layer by a thermal conductance G_0 (W/K). When the device is in normal operation, G_0 will be very high. However, when it is tested aboard MIDSTAR the device will be mounted on a radiator that is thermally isolated from the satellite itself, so that its operation will not affect the overall

functioning of the satellite. For the experiment planned on MIDSTAR, we will heat the radiator itself with electrical power Q_0 to simulate different operation conditions. The energy equation for the radiator is then given by

$$Q_0 + G_0(T_0 - T_1) - G_{\text{var}}(T_1 - T_2) = C_1 \frac{dT_1}{dt} \quad \textbf{(4)}$$

where C_1 is the thermal capacitance of the silicon/aluminum radiator (J/K).

In the MIDSTAR experiment, switch performance will be monitored by thermistors attached to the radiator. We therefore need to use the thermal model to relate G_{var} to the temperature of the radiator. Equations (3) and (4) can be solved in the quasistatic case for T_1 as a function of G_{var}. Assuming the radiator is thermally decoupled from the satellite ($G_0=0$), and that the structure is in thermal equilibrium ($dT_1/dt = dT_2/dt = 0$), the temperature T_1 of the radiator is given by

$$T_1 = -\frac{Q_0}{G_{\text{var}}} + \left(\frac{Q_0}{A\varepsilon\sigma}\right)^{\frac{1}{4}} \quad \textbf{(5)}$$

Therefore, the difference temperature between the on and the off state is simply given by the differences in inverse thermal conductance for the two states,

$$T_{1,on} - T_{1,off} = Q_0\left(\frac{1}{G_{\text{var},off}} - \frac{1}{G_{\text{var},on}}\right) \quad \textbf{(6)}$$

Equation (5) and (6) allow the calculation of the radiator temperature as well as the temperature difference between the on and off state for different switch designs. In addition, the conductance in the on state is so large relative to the conductance in the off state that the temperature difference reduces to

$$T_{1,on} - T_{1,off} \approx \frac{Q_0}{G_{\text{var},off}} \quad \textbf{(6)}$$

The material properties of interest are listed in Table 1.

FABRICATION AND PACKAGING

The fabrication for the current generation of the thermal switch has been described elsewhere [4]. It is a surface micromachining process that uses electroplated gold for the membrane material, SU-8 for the support posts, and oxide as the sacrificial layer. Gold has been used as a membrane material in part because a number of self-assembly technologies can be used to achieve a high emittance coating. Figure 5 shows schematics of the two major designs, one with posts and one with a frame. A number of both devices have

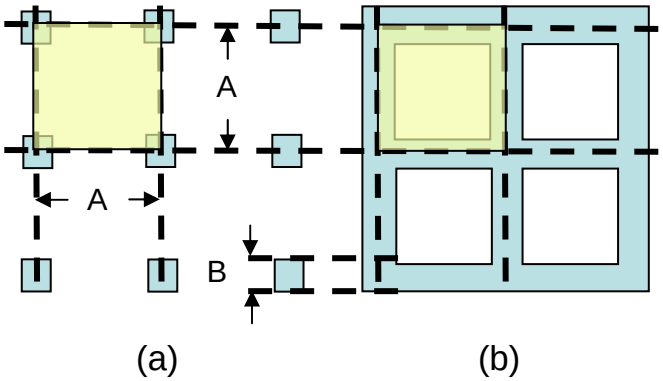

Fig. 5 Schematic for the post (a) and the frame (b) design. For all experimental devices, B is 100 μm.

been fabricated with different dimensions for the post or frame width (B) and the membrane width (A). Each device has a size of about 12.7 mm x 12.7 mm. The different designs are summarized in Table 2. Post design 2 was designed for a much higher actuation voltage than the desired level of less than 28 volts in order to offer a contrast. The higher voltage design should be more rugged because of the higher spring constant.

Each test device for the midstar experiment is expected to consist of 4 devices, mounted onto a thermally decoupled radiator. The radiator package is shown in Figure 6. It is a modified version of the packaged developed for thermal shutters in the Space Technology-5 (ST-5) mission [9]. Each radiator section can be controlled separately from an Electronic Control Unit (ECU) located within the spacecraft which interfaces with the satellite's central Command & Data Handling (C&DH) unit, provides the switching voltage of about 60 V [10], controls the heating power and measures the temperature of each radiator section. Since thermally decoupled from the spacecraft, the radiator needs to be heated to stay within the operating temperature range of the devices, -80°C to +80°C. Figure 6 shows the adaptations that will be made to the ST-5 package. Each of the radiator sections will be thermally isolated and measured independently. A solar aspect detector will also be placed on the radiator to be able to account for incident solar radiation.

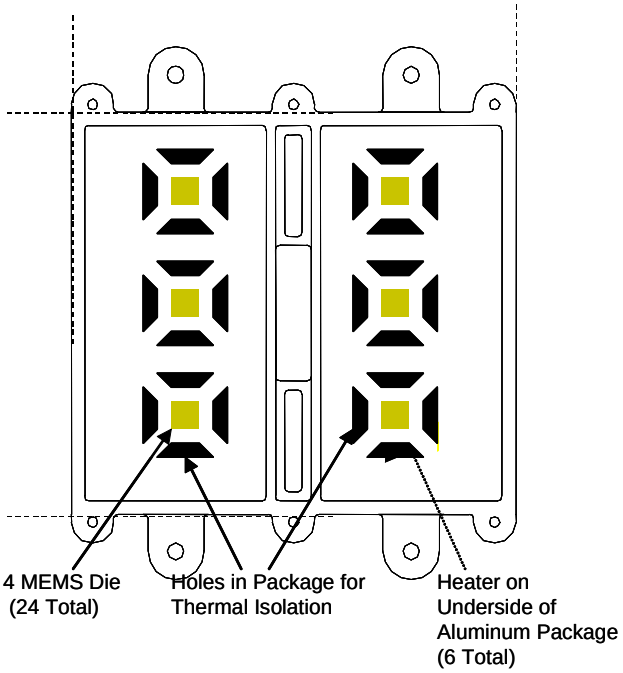

Fig. 6 Illustration of Package to be Built for MIDSTAR I.

RESULTS

We have fabricated prototype devices in order to verify our electromechanical model, but have not yet implemented the high emissivity coating. Pull-in voltage testing has been conducted on the devices. The pull-in voltage testing occurred in air at standard temperature and pressure ($\varepsilon_{air} = 1.00054\varepsilon_0$). Table 2 shows that experimentally measured pull-in voltages were very close to those predicted by our electromechanical model. The largest error occurs in the testing of post design 2, the small posts. This is because of the variations of g_0 in the samples tested. According to equation (1), V_{pi} is directly proportional to the effective initial gap, g_0, raised to the three halves power. Therefore, small variations in the gap height result in wide variations of the pull-in voltage. A fraction of the small post membranes activated in the 18-22 V range. As the voltage level was further increased we observed dielectric breakdown and were therefore unable to measure the pull-in voltage for many of the membranes. The frame designs proved to be the most consistent. These devices showed a much smaller degree of variation in the initial gap thickness g_0.

Table 2. Device Dimensions and Resultant Voltages.

Design	Eff. Initial Gap	Membr. Thick.	Eff. Membr. Width(*)	Theor. Pull-in Voltage	Meas. Pull-in Voltage	G_{off} W/K(**)
Post Design 1	**0.8 µm**	**2 µm**	**550 µm**	**5.1 V**	**7-12 V**	**3.68**
Post Design 1	**2 µm**	**2 µm**	**550 µm**	**20.0 V**	**--**	**3.68**
Post Design 2	**1.5 - 1.8 µm**	**2 µm**	**300 µm**	**57.9 - 73.6 V**	**18-25+V**	**2.5**
Post Design 2	**2 µm**	**2 µm**	**300 µm**	**89.2 V**	**--**	**2.5**
Frame Design	**0.6µm**	**2 µm**	**400 µm**	**11.5 V**	**9-11 V**	**13.1**
Frame Design	**2 µm**	**2 µm**	**400 µm**	**28.2 V**	**20-25 V**	**13.1**

(*) Effective membrane width corresponds to A+B in Fig. 5 for design (a), A-B for design (b).
(**)The off- conductance for a (2.54 cm)^2 device

The thermal conductance in the off state has been calculated for each of the designs and is shown in Table 2. As expected, it is much smaller for the post designs than it is for the frame designs. The off-state conductance is the variable which dominates the temperature difference between the on and the off state. For a thermally isolated radiator section, a heating power of about 0.5 W is required, according to equation (5) with ε=1, A=6.25 cm^2, and σ=5.67x10^{-8} w/m^{2}K^4, to keep the radiator at a temperature of about 340 K.

Figure 7 shows the temperature difference between the on and the off state as a function of the off-state conduction, according to equation (6), with 0.5 W of heating power. Fig. 7 shows, that the present designs, which concentrated more on the electrostatic and mechanical aspects, do not create temperature differences of impact, which is due to the limitations in the off state conductivity. Reducing the post dimension B to 10 µm x 10 µm will reduce the off conductance by a factor of 100. This is probably the most desirable approach, since a change in gap thickness also would change the pull-in voltages. We are also testing an alternative design, fabricated through the polyMUMPS process, which utilizes serpentine polysilicon supports and has a factor of 10 smaller off-state conductance. Combining the serpentine support geometry with the use of SU-8 should yield a much better thermal performance level. We are also currently working on the development of the high emissivity coating for the structures.

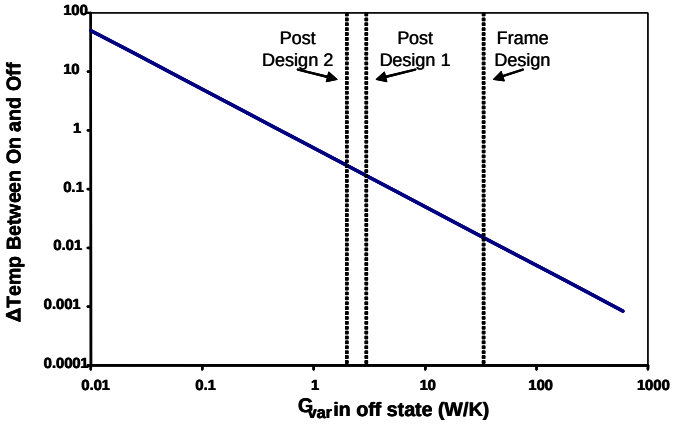

Fig. 7 Temperature difference for (2.54 cm^2) radiator sections in the on-off state as a function of off-conductance for 0.5 W heating. The different designs from table (2) are depicted.

SUMMARY

The design aspects for a MEMS-based satellite thermal control device, based on a thermal switch, has been described. A electromechanical and thermal model has been developed for the device which allows to calculate the pull-in voltages required as well as device dimensions for the thermal considerations. A radiator assembly has been designed which will allow different devices to be tested aboard MIDSTAR 1, a small satellite that will be launched by the United States Naval Academy. The prototypes under development are expected to create measurable temperature differences between the on and off states.

Thermally switched radiators are expected to play a major role in the thermal esign of small nano- and picosatellites. The devices introduced in this paper show one solution for thermally switched radiators which is compatible with the voltage, power, and weight requirements for these satellites.

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