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PicoDyne has developed Ultra-Low-Power(ULP) CMOS design techniques and processes, and combined them with Radiation Hardened By Design methodologies to form it's Cool-RAD™ process. Complex ULP and Cool-RAD™ parts have been built, including data compression devices, Reed-Solomon Encoders and Decoders, and digital signal processors. Memory blocks have been embedded in ULP chips. Radiation Tolerant Memory presents new challenges to the chip designer. During the course of this SBIR, PicoDyne developed a memory architecture for use in Cool-RAD™ parts. We started with a small memory cell pair that is insensitive to single event effects, and will scale to smaller geometries to provide the same performance. We then designed arrays of that memory to build up blocks to be used in complex Cool-RAD™ parts such as microprocessors and digital signal processors.

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# Executive Summary

PicoDyne has developed Ultra-Low-Power(ULP) CMOS design techniques and processes, and combined them with Radiation Hardened By Design methodologies to form it's Cool-RAD™ process. Complex ULP and Cool-RAD™ parts have been built, including data compression devices, Reed-Solomon Encoders and Decoders, and digital signal processors. Memory blocks have been embedded in ULP chips. Radiation Tolerant Memory presents new challenges to the chip designer. During the course of this SBIR, PicoDyne developed a memory architecture for use in Cool-RAD™ parts. We started with a small memory cell pair that is insensitive to single event effects, and will scale to smaller geometries to provide the same performance. We then designed arrays of that memory to build up blocks to be used in complex Cool-RAD™ parts such as microprocessors and digital signal processors.

# Research Issues

### THE PROBLEM:

Electronics for missile systems are growing ever more complex, mirroring the complexity of microelectronics in our everyday lives. Systems designers are being asked to perform more complex tasks without increases in budget, schedule, area, or power allotments. Meeting these goals requires access to modern, fast, and low power semiconductor processes for circuit design. Typical commercial processes can meet the speed and area goals, but cannot endure the radiation environment required of the application to missile systems.

### PROJECT GOAL:

The goal of this SBIR is to demonstrate radiation tolerant, ultra low power (ULP) VLSI combining breakthrough techniques in ultra low power with SEU mitigation techniques using commercial processes. This activity leverages an ultra low power technology demonstration program (CULPRiT) that is being undertaken under sponsorship of DoD. CULPRiT has produced CMOS technology that operates at supply Voltages near 0.5 Volts, with a goal of pushing that Voltage down to 0.25V in the future. A 100-fold reduction in power levels is realized in comparing 5V and 0.5V processes in digital electronics. Specifically, this SBIR will demonstrate a Rad-Tolerant (RT) version of a 0.5V ULP circuit implementing blocks of memory to be used in ASICs.

The following graphic describes the many benefits of developing embeddable memory blocks for use in Rad-Hard Ultra Low Power chips:

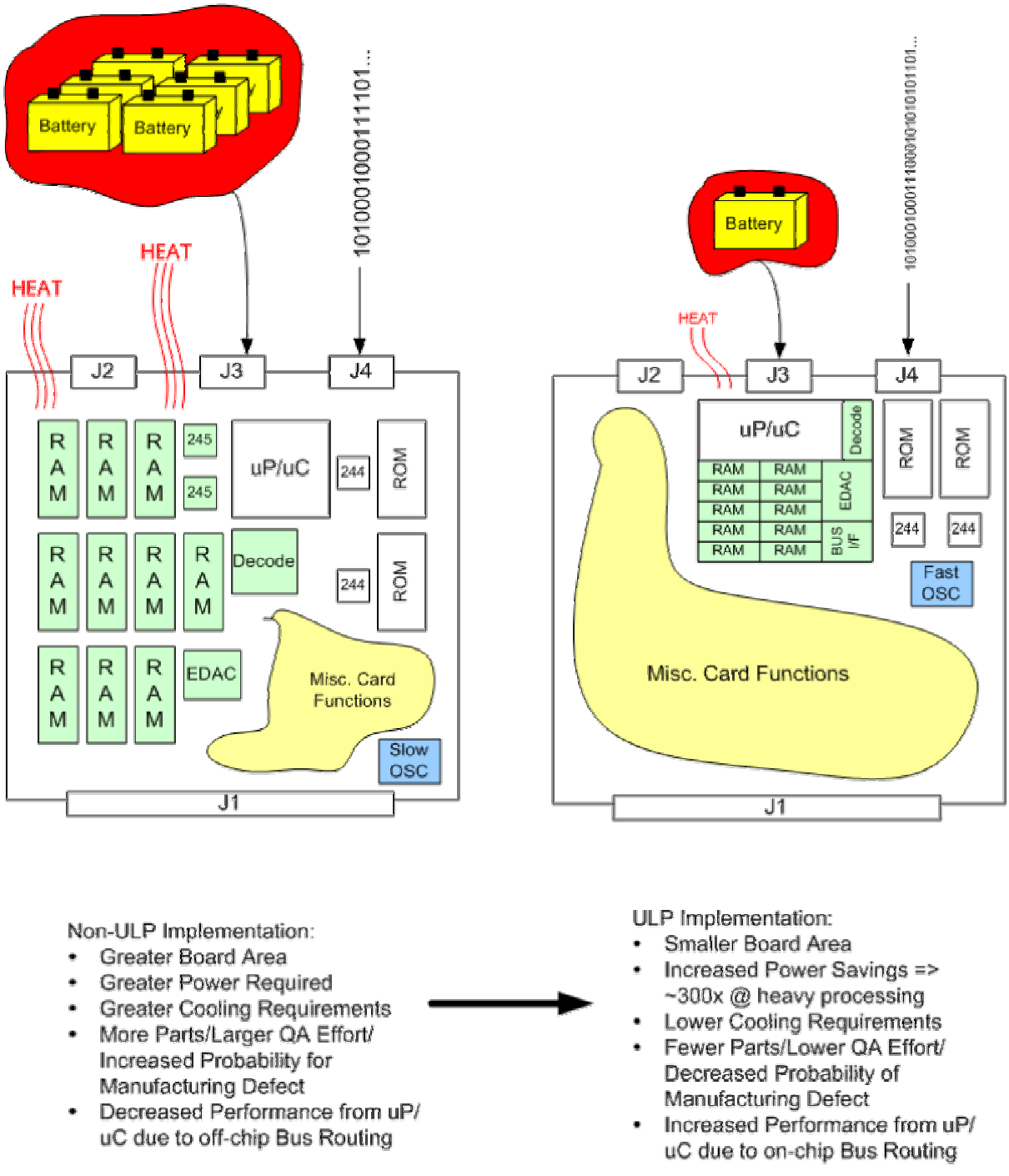


**Figure 1 - Benefits of ULP Technology**

# Technology Description

## ULP TECHNOLOGY

The energy consumed in a CMOS switch, $E_{CMOS}$, is given by the sum of the AC switching energy, DC leakage energy, and short circuit energy, namely, $E_{AC}$, $E_{DC}$, $E_{SC}$, respectively.

$$E_{CMOS} = E_{AC} + E_{DC} + E_{SC}.$$

The AC switching energy is the energy consumed in charging and discharging the various circuit node capacitances. The DC leakage energy is the energy consumed by the steady state leakage currents of the biased devices. The short circuit energy is the energy consumed during the brief moment of a logical state transition when both n-channel and p-channel transistors are on, and charge flows. The short circuit energy is generally 10% of the total, scales with voltage, and can be neglected in this analysis. A graph of the AC switching energy, the DC leakage energy, and the sum of the two is shown in Fig. 2, for a given circuit activity factor and logical depth.

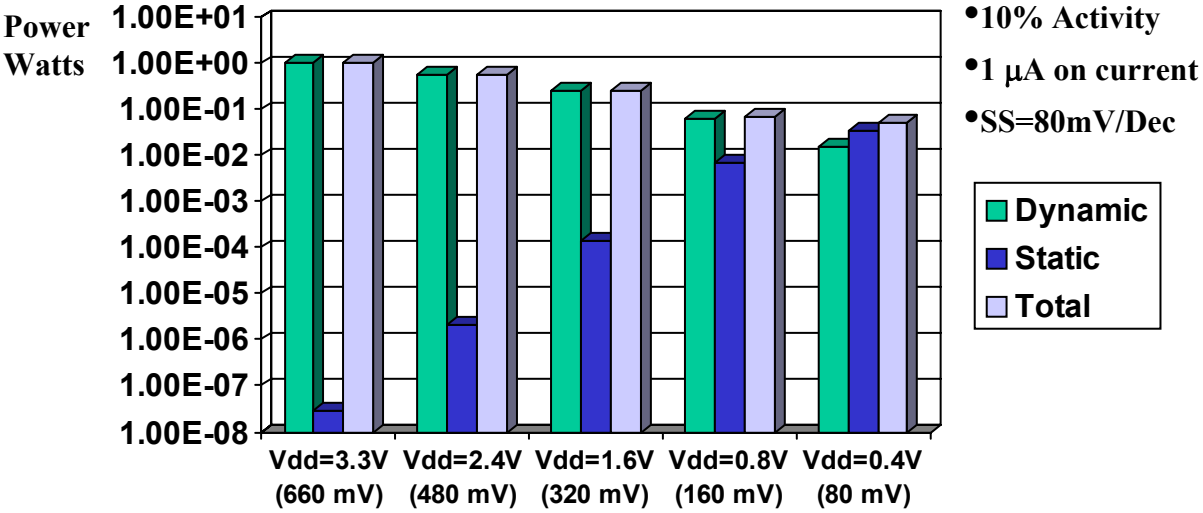


**Figure 2 - AC switching energy, DC leakage energy, and the sum of the two, for a given circuit activity factor and logical depth**

As shown in Fig 2, the minimum energy in a CMOS circuit occurs when the DC power dissipated is equal to the AC power dissipated; consequently,

$$E_{AC} = E_{DC},$$

and,

$$aCV^2 = I_{off} V / f,$$

where a is the activity of the circuit, $I_{off}$ is the off state leakage current of the circuit, C is the capacitance, V is the applied drain bias ($V_{dd}=V_T$ for minimum energy), and f is the maximum switching frequency. The maximum switching frequency is given by,

$$f = \frac{I_{on}}{l_d CV},$$

the on current divided by the total charge moved in each cycle, scaled by the logical depth of the circuit, $l_d$. Substituting terms gives the relation,

$$aCV^2 = \frac{I_{off}}{I_{on}} CV^2 l_d,$$

which simplifies to the relation,

$$\frac{I_{on}}{I_{off}} = \frac{l_d}{a}.$$

Consequently, maximum energy efficiency permits large off state transistor leakage currents when the circuit switching activity is high and the logical depth is small. The circuit with the most ideal topology for energy efficiency using ULP technology (although functionally not useful) is the ring oscillator. A ring oscillator formed from inverters with uniform I-V characteristics, a logical depth of 1, and an activity factor of 50%, will function at minimum energy when $I_{on}$ is just twice $I_{off}$; however, the output voltage will not reach all the way to the supply rails. The maximum leakage current is also limited by bus fan-out, i.e., when a single n-channel device pulls down with $I_{on}$ against N devices, each pulling up with $I_{off}$. In this case, $I_{on}/I_{off} > 10N$ is required to swing the output to within 90% of the supply rails.

The ULP approach to high performance low power circuits is to electrically adjust the threshold voltage near zero volts in active circuits, in order to optimize energy and performance according to the level of activity. This adjustment of threshold voltage is controlled by the substrate bias. The threshold voltage on the transistors is set so that the drain current when the transistor is on, divided by the drain current when the transistor is off, is

approximately the ratio of the logical depth in the circuit divided by the circuit activity. The ratio given by,

$$\frac{I_{on}}{I_{off}} = \frac{l_d}{a} = 100,$$

is suitable for a typical logic function, such as a microprocessor or microcontroller.

Recent measurements of a ring oscillator structure fabricated in a 0.25 um low-threshold process operated at 1.5 GHz. @$V_{dd}$=2V, 850 MHz. @$V_{dd}$=1V, and 350 MHz. @$V_{dd}$=0.5V. The corresponding intrinsic fanout-1 delay times are 34 ps, 58 ps, and 139 ps, respectively. The thresholds in the 1.5um technology were 0V. The thresholds in the 0.25um technology were 180mV. Simulations indicate that if the thresholds in the 0.25um process were reduced to 0V, the performance at $V_{dd}$=0.5V would increase to over 1GHz as shown in the table below.

| *$l_g$ (um)* | *$V_T$ (mV)* | *Delay (ps) $V_{dd}$=0.3V* | *Delay (ps) $V_{dd}$=0.5V* | *Delay (ps) $V_{dd}$=1.0V* | *Delay (ps) $V_{dd}$=2.0V* |
|---|---|---|---|---|---|
| 0.25 | 400 | - | 9400 | 85 | 25 |
| 0.25 | 180 | 300 | 139 | 58 | 34 |
| 0.25 | 0 | 40 | 25 | 20 | 17 |

There is an opportunity to achieve excellent performance at very low supply voltages, provided the threshold voltage is also aggressively reduced. Operating at such a low voltage supply requires some form of threshold compensation to reduce process and environment induced on and off current variations, hence the need for back-bias to improve worst-case performance and manage standby power dissipation.

Noise

Internal noise sources scale at least as fast as the supply voltage, as shown in the table below:

| *Coupling* | *Variation* | *Long Channel* | *Short Channel* | *Ballistic* |
|---|---|---|---|---|
| Capacitive | $(C_{ab}/C_b)V$ | V | V | V |
| Resistive | IR | $V^2$ | V | $V^{3/2}$ |
| Inductive | L(dI/dt) | $V^3$ | V | $V^2$ |

The capacitively coupled noise scales as the voltage V; the resistively coupled noise as $V^2$, and the inductively coupled noise as $V^3$ in long-channel limit and V in the short-channel limit. Thermal noise does not scale, but is only about 100 uV ($V^2$ = 4KTRf). Relative noise margins tend to degrade with aggressively scaled thresholds, but are still sufficiently large enough to support a broad range of logic styles.

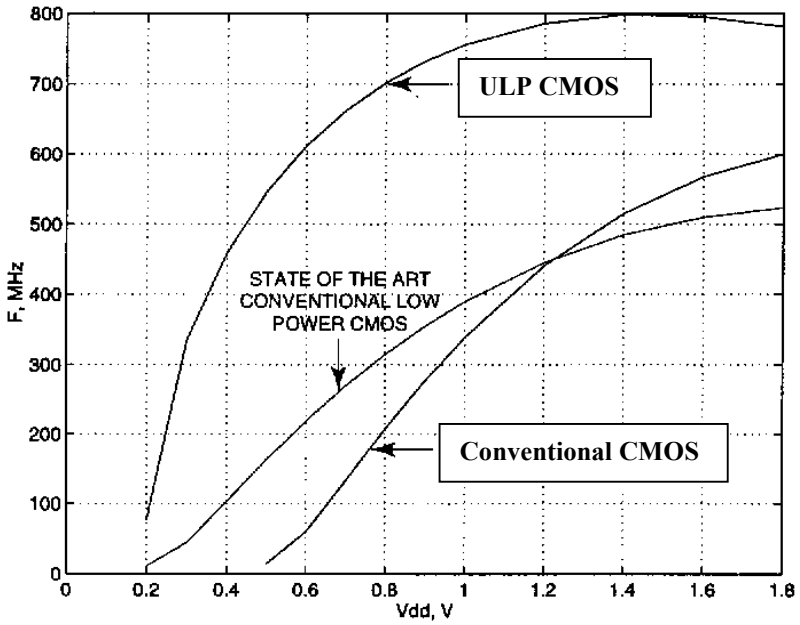


**Figure 3 - Performance comparison of ULP technology, conventional CMOS, and state of the art conventional low power CMOS.**

Figure 3 illustrates a performance comparison of ULP technology compared to both conventional CMOS and state of the art conventional low power CMOS. The graphs for the conventional low power process are a compilation of industry data points for advanced development 0.25 um processes.

Fig. 4 illustrates the power consumption of high speed ULP and low energy ULP technology compared to conventional CMOS. The graph for the conventional CMOS is a compilation of industry data points. The ULP graphs parallel the SIA roadmap of conventional CMOS and are simulated using parameters that would (properly selected) accurately model the ULP processes.

In summary, the case for ULP technology is as follows:

1. Lowering $V_T$ can make low voltage digital logic circuits operate at a higher frequency, without loss of functionality.
2. Counterintuitively, the higher leakage at low threshold leads to greater energy efficiency because it allows the system to achieve the necessary performance at lower supply voltage, which quadratically reduces the switching energy. At minimum energy the excess power consumed by off state leakage current is balanced by the lower power consumption from operating at lower voltages.
3. Using back bias, the $V_T$ design point and power dissipation can be reduced further. At lower $V_{dd}$ and $V_T$, the MOS transistor constraints associated with higher voltage are eliminated (impact ionization, hot electron effects, …), and device structure can be modified to increase performance. Transistors optimized to operate at low

voltage have higher mobility, lower series resistance, and lower junction capacitance.

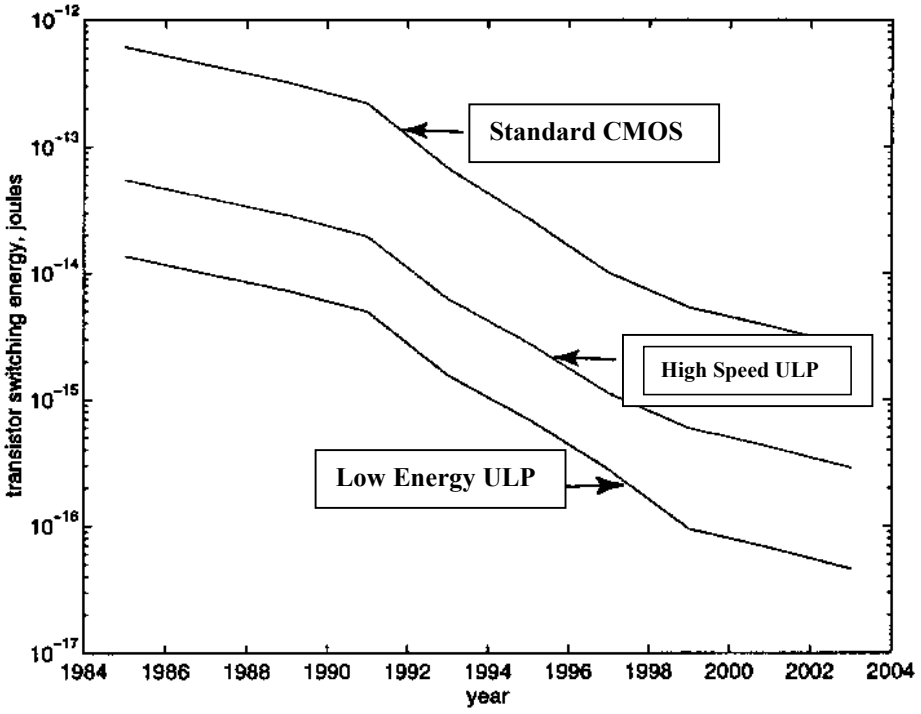


**Figure 4 - Transistor switching energy on the SIA Roadmap, for standard CMOS, High speed ULP CMOS, and ultra low energy ULP CMOS.**

The CULPRiT program has conducted tests to directly measure the performance of ULP devices against functionally equivalent devices in standard technology. Both NASA GSFC and The Johns Hopkins University Applied Physics Laboratory have flown a 1.2um gate array implementation of a NASA standard Reed Solomon encoder designed by the Microelectronics Research Center (MRC) at the University of New Mexico (also IAuE) to operate at 20 MHz. This design was re-implemented on the AMI 1.0um process that operates at 5 V, on the AMI 0.35um process that operates at 3.3V and on the ULP-enabled process that operates at 0.5V. Radiation tolerant versions were also made of both devices using the MRC latchup and SEU mitigation techniques. All of the versions of this circuit were tested at 20 MHz using the same data set for all three designs. As shown in figure 5, the power reduction over the existing flight part was a factor of 333, while the savings by the ULP part over the conventional 3.3 V part was a factor of 120. These results were achieved with the first production run of ULP technology and are considered conservative lower bounds to what is achievable using ULP. Similar reductions in power consumption have been demonstrated for other processors now in development, including a C50 Digital Signal Processor.

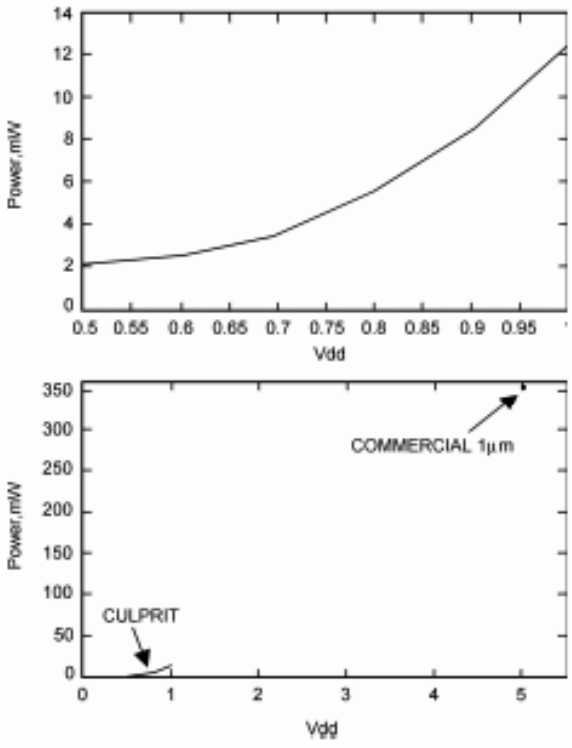


**Figure 5 - Power consumption of the Reed Solomon encoder.**

In a simple review of the benefits of ULP, these formulas show the contributors to power consumption:

**Active Power:**

**Pd = frequency * Cload * $V^2$**

Where Pd Dynamic power dissipation; frequency = operating frequency
Cload load capacitance; $V^2$ = the square of the operating voltage

**Standby Power:**

**Ps = V * Leakage = V * e-Vth/kT**

Where Ps Static power dissipation; V = operating voltage

kT a constant times temperature Vth = threshold voltage

As can be seen above, active power is dominated by the operating voltage; standby power is dominated by leakage, which is directly affected by the threshold voltage. In our base technology, we balance these to be most efficient at high circuit activity.

## *RT TECHNOLOGY*

### THE SEU PROBLEM:

Single Event Effects are produced in the natural space environment by galactic cosmic rays, solar enhanced particles and energetic protons and neutrons. The passage of a single high energy particle through a MOS device can create a high-density ionization track which results in charge collection in a localized region of the circuit. A Single Event Upset (SEU) occurs when the charge transferred as a result of the generated currents is of sufficient magnitude to alter the logic state of a susceptible node. An upset node may further cause the alteration of the contents of circuit memory elements or alter the operation of the circuit in such a way to cause an error in the logic function.

Methods typically employed to inhibit SEUs in CMOS circuits involve increasing the "critical charge" required to produce an upset. These methods include "resistive hardening" and/or "capacitive hardening" which amount to building "low pass" filters into the digital circuits in order to distinguish the real signals from the "glitches" and/or reducing the voltage excursions due to particle induced charge collection. These techniques impose constraints on the maximum operating rate of circuits as well as increase their power consumption.

As operating voltages are reduced in order to reduce power system requirements the charge being switched at circuit nodes is also reduced, which decreases the critical charge and makes it even more difficult to distinguish the real signals from the induced charge collection.

### PICODYNE RT MITIGATION APPROACH:

The PicoDyne SEU hardening technology produces SEU-immune circuits using standard CMOS processing, with no additional mask or processing steps, and further minimizes cell size, circuit speed, and power consumption costs. The technology is based on three fundamental concepts. First, information storage redundancy is used to maintain a source of uncorrupted data through an SEU. Second, feedback from a non-corrupted data storage location causes the corrupted data to recover after a particle strike. Finally, the "intelligence" needed in the feedback to cause recovery of the proper location can be derived from the fact that the current induced by a particle hit flows from n-type diffusion to p-type diffusion. If a memory cell is constructed from only p-type transistors then it cannot be upset to a 0 while storing a 1. A memory cell constructed from only n-type transistors cannot be upset to a I while storing a 0. Thus, rather than attempting to prevent SEU through critical charge reduction techniques which become more and more difficult with lower operating voltages the PicoDyne licensed technology is based on rapid detection and correction of upsets when they do occur.

Also included in the circuit designs are special buffers that inhibit the propagation of glitches from recovering memory elements and their capture from combinational logic circuits into memory elements.

PicoDyne's partner, the MRC, has demonstrated that this Radiation Tolerant technology is hard against SEU and SEL in several commercial processes ranging from 1.0 um to 0.35 um and at operating voltages of 5V and 3.3V, and, in combination with ULP technology, to 0.5V. During tests at the Brookhaven National Laboratory's Single Event Upset Test Facility (Twin Tandem Van de Graaff Accelerator) conducted June 9-10, 1998, the following results were obtained from special test chips designed utilizing a Radiation Tolerant 0.5um Standard Cell Library using MRC Technology and fabricated at a commercial foundry and operating at 3.3 volts. Similar results were also obtained utilizing a 0.35um version of the same library also operating at 3.3 volts.

- No Single Event Latch-up to an LET of 120 MeV/mg/CM2
- No memory element (flip-flop) Single Event Upset to an LET of 120 MeV/mg/CM2.
- Effective cross-section of clock edge coincident upsets captured into memory elements reduced by at least one order-of-magnitude.

Preliminary circuit simulations indicate that these techniques can be successfully adapted to the ULP process, which operates at 0.5 V. (In addition, the Ultra-Low-Power 0.5V approach yields higher total dose immunity in standard processes.)

The memory cell design first proposed by Whitaker[i] and the improved low power version use the same three fundamental concepts as the Rockett[ii] cell, but instead of adding storage nodes and feedback to the standard six transistor cell and loading the clock to turn all of the added circuitry off while data is written to the cell and to drive "data" to one of the redundant nodes during data storage, the Whitaker cell represents a completely new approach. The low power Whitaker cell, shown in Figure 6, consists of two loadable storage structures.

The lower storage structure is a modified six-transistor cell consisting of only n-type devices and the top structure is a modified six-transistor cell consisting of only p-type devices. The lower structure stores un-corruptible 0s and the top structure stores un-corruptible Is. In order for the feedback mechanism to effect recovery from SEU, transistors M2 and M4 are sized to be weak compared to M3 and M5 while M13 and M15 are sized to be weak compared to M12 and M14.

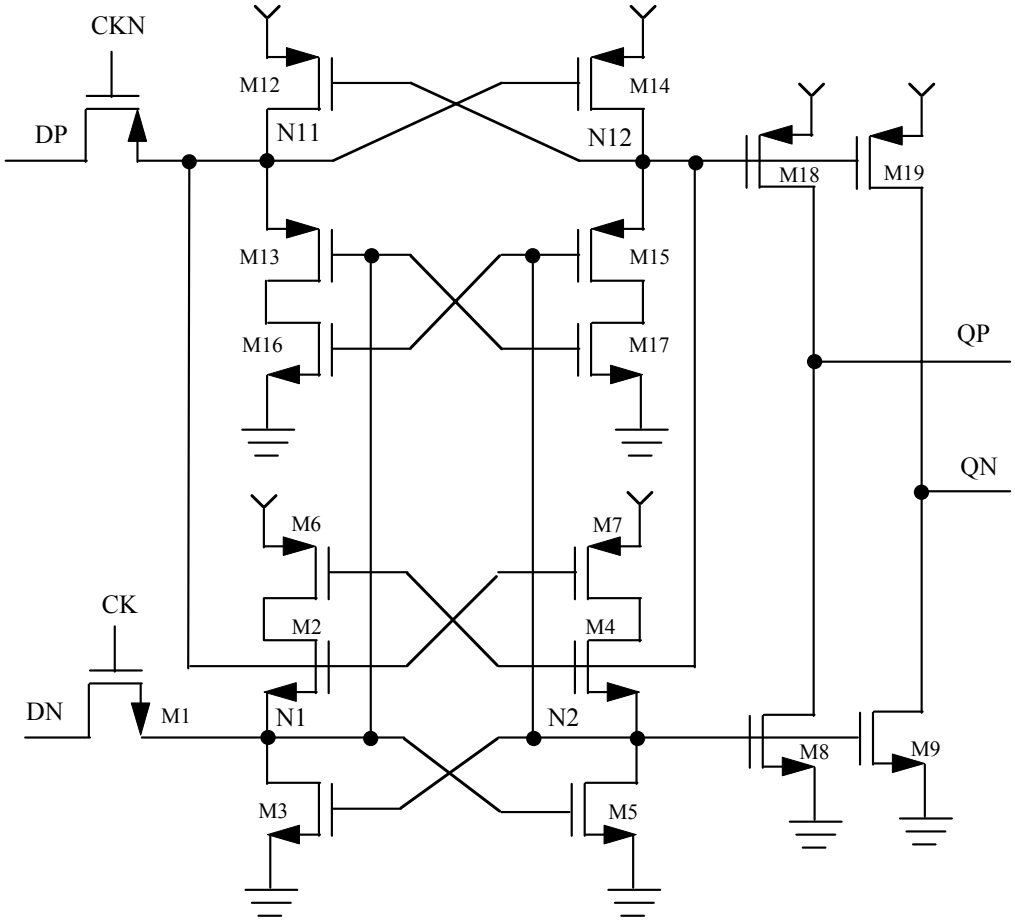


**Figure 6 - Buffered Low Power Whitaker Cell - SEU Radiation Hardened**

Complementary n-channel devices M 16 and M 17 are added to disconnect the dc-current path in the p-channel section eliminating the static power consumption that otherwise results from the weak I level produced at NI (N2) not turning M13 (M15) completely off. Similarly pchannel devices M6 and M7 are added to disconnect the dc-current path in the n-channel section. The other transistors are sized using the normal design considerations for a memory cell to meet the performance required. By not requiring p-channel devices to be stronger than particular n-channel devices, the transistor sizes can be kept smaller while still meeting the SEU recovery constraints. The cell buffer transistors M8, M9, M18, and M19 restore the output voltage levels to the rails, isolate the storage nodes from high capacitance loads, and tri-state the cell output during SEU recovery. By tri-stating during SEU recovery and not driving outputs to upset values, the capacitance on the cell output maintains the correct output voltage levels during recovery. Supplying separate input signals to the n-channel and p-channel sections combined with an inherent feature of the cell eliminates the capture of propagated upsets that are coincident with clock edges. (note: This cell design forms the basis for our radiation tolerant storage cell, and is being advanced with further research to produce Design-Hardened latch specifically for use in ULP.)

It is recognized that there are differing requirements for the varied applications of electronics

in space. There are trades to be made between levels of TID resistance, SEE tolerance or immunity, speed, power, reliability, development cost, and device cost. To meet these varied needs, PicoDyne uses three approaches. Each approach is characterized by the inclusion of Design-Hardened ULP standard cells, with features to prevent SEL. From there we separate the approach taken:

1. The use of single-string random logic cells, with RT latches and Flip Flops, using a single input. This approach is used where SET is not deemed to be an issue, and the LET requirements can be met with just RT latches;

2. The use of single-string random logic, but with temporal separators used to prevent the propagation and storage of Single-Event-induced Transients.

3. With the most stringent Radiation requirements, we implement RT storage cells with dual-redundant inputs, and instantiate dual-redundant strings of random logic between the storage elements.

The research proposed here answers the question of where each approach is appropriate in a memory array, and then develops an architecture for the design of circuitry using the selected method for a given application, while maintaining a commercial design flow and the power efficiency of a ULP implementation.

## TOTAL DOSE RADIATION

Commercial foundries do not design their processes with total dose hardness in mind. However, as feature size diminishes, tests have shown an increase in tolerance. Processes with feature size of 0.5um have tested in the range of 20-60 Krad tolerance. Processes with feature size of 0.35urn and 0.25um have shown similar, if not greater tolerance. The ability to use commercial processes for space electronics provides many advantages, including high speed, predictability due to the high volume of parts run on the foundry, associated reliability, and reduced cost.

Significantly, PicoDyne has learned through testing that our ULP process is quite resistant to the effects of trapped charge due to total ionizing dose (TID). The circuit structures used in ULP serve to drain off any excess charge, resulting in negligible parameter shift into the hundreds of KiloRads[iii]. We are confident that the mechanism at work here will remain in effect both in smaller geometries, and into the Mega-Rads of total dose radiation. Thus far, such testing has not been performed (above 300 Krad(Si)) due to concerns about ITAR restrictions.

# Work Performed

## *UNDERSTANDING THE ENVIRONMENT*

PicoDyne Engineers met with SMDC personnel to determine the likely application of Embedded ULP/RT memory. Given the information and resources from that meeting, we determined that many of the environmental survivability issues we deal with in civil space applications apply to military missile electronics as well.

With the exception of the dose rate problem encountered in some military electronics systems, the radiation requirements match those of the most stringent space applications with regard to Total Dose and Single Event Effects such as Single Event Upsets and Single Event Latchup. A table was developed with the following limits as goals for any electronics developed for these applications. Of course, each particular military or space application develops its own requirements based upon its mission, but these are representative:

| | **High Performance** | **Strategic** | **Civil Space** |
|---|---|---|---|
| **Total Dose** | | | |
| **Goal** | 500 krad(Si) | 2 Mrad (Si) | 500 krad(Si) |
| **Requirement** | 300 krad(Si) | 1 Mrad(Si) | 25-100 krad(Si) |
| | | | |
| **Single Event Upset** | <1e-9 errors/bit day | <1e-10 errors/bit day | 1e-10 errors/bit day |
| | | | LETth > 35 Mev |
| | | | |
| **Latchup** | Dose Rate 5e8 rad(Si)/sec | Dose Rate 1e9 rad(Si)/sec | LETth > 85 Mev |
| | | | |
| **Dose Rate Upset** | 5e8 rad(Si)/sec | 1e9 rad(Si)/sec | N/A |
| | | | |

Reference [iv, v]

Other factors include operation in the absence of an atmosphere, which applies to ballistic missiles as well as satellites, and the requirements to operate over large temperature ranges. These are common requirements to the RT circuits previously designed and implemented by PicoDyne.

Speed and complexity of missile systems electronics rival those of commercial electronics. Systems designers want the benefits of the most recent technology to achieve higher processing speeds, data throughput, and memory density.

This supports the need for development of memory blocks to be embedded within Ultra-Low-Power ASICs. In addition, the desire for high processing speeds and greater integration of

functions within one device points the electronics developer to newer foundry processes with ever smaller feature sizes.

# *DETERMINING THE MEMORY ARCHITECTURE*

## ALTERNATIVE MEMORY ARCHITECTURES

We examined memory architectures on two scales: the block level, and the cell level.

At the block level, we have experience in performing trades between speed, size, and radiation tolerance. A fully commercial memory has the advantage of speed and small size, but no resistance to the effects of radiation. Traditional Rad-Hard memory solves the radiation issue, but at the expense of both speed and area. We have also implemented memories with faster, smaller cores, using Error Detection and Correction to compensate for the reduced resistance to radiation.

At the cell level, there are also trades to perform. Our Radiation Tolerant storage cell has proven performance at 0.65um, 0.5um, and at 0.35um. However, as feature sizes shrink, critical nodes are being placed closer together, resulting in the possibility of having multiple nodes within a single storage cell upset with a single heavy ion strike.

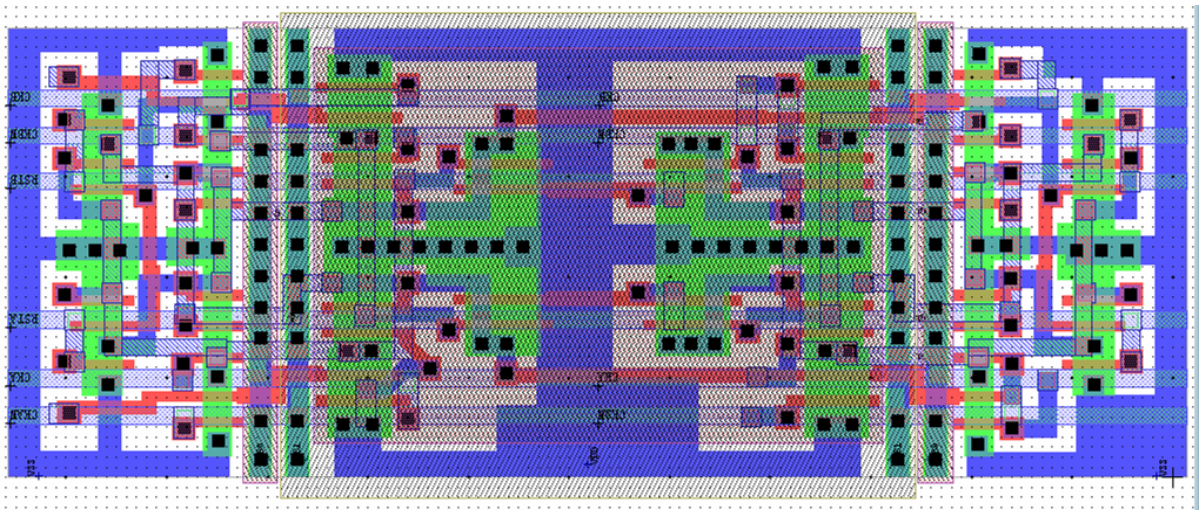

**Figure 7 - Plot of basic SERT Cell**

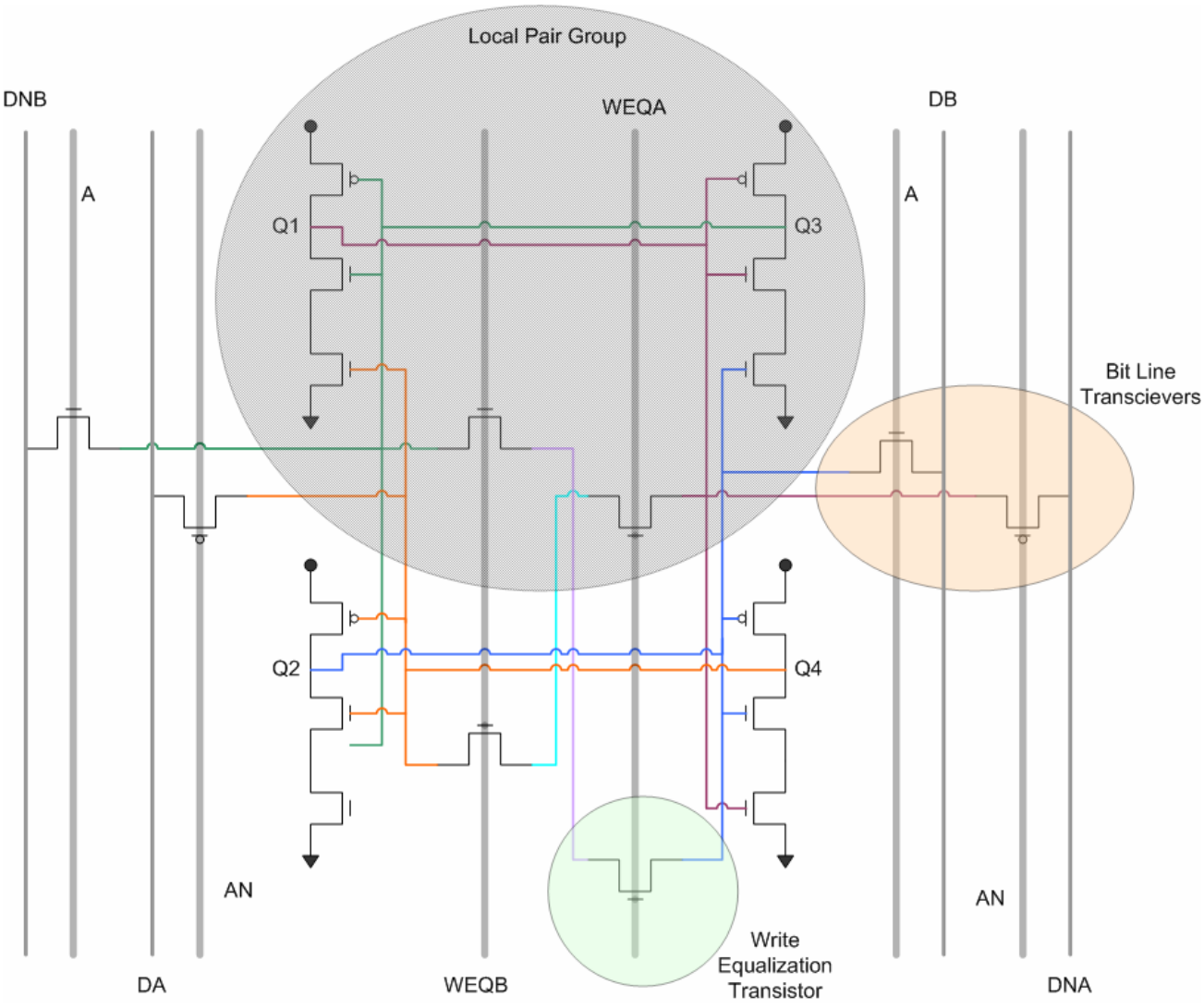


**Figure 8 - Single Event Radiation Tolerant Latch**

As the schematic (figure 8) of our basic Single Event Radiation Tolerant(SERT) cell shows, there are 'local pair groups' which provide the corrective ability of the cell after being struck by a heavy ion. If these nodes become physically closer as feature sizes shrink, the effectiveness of our SERT cell may be reduced. This effect is demonstrated in the drawing below (Figure 9). The amount of energy deposited by a heavy ion passing through silicon does not change, but the number of features per unit area increases, thereby having more of an effect if the circuit is not designed to accommodate.

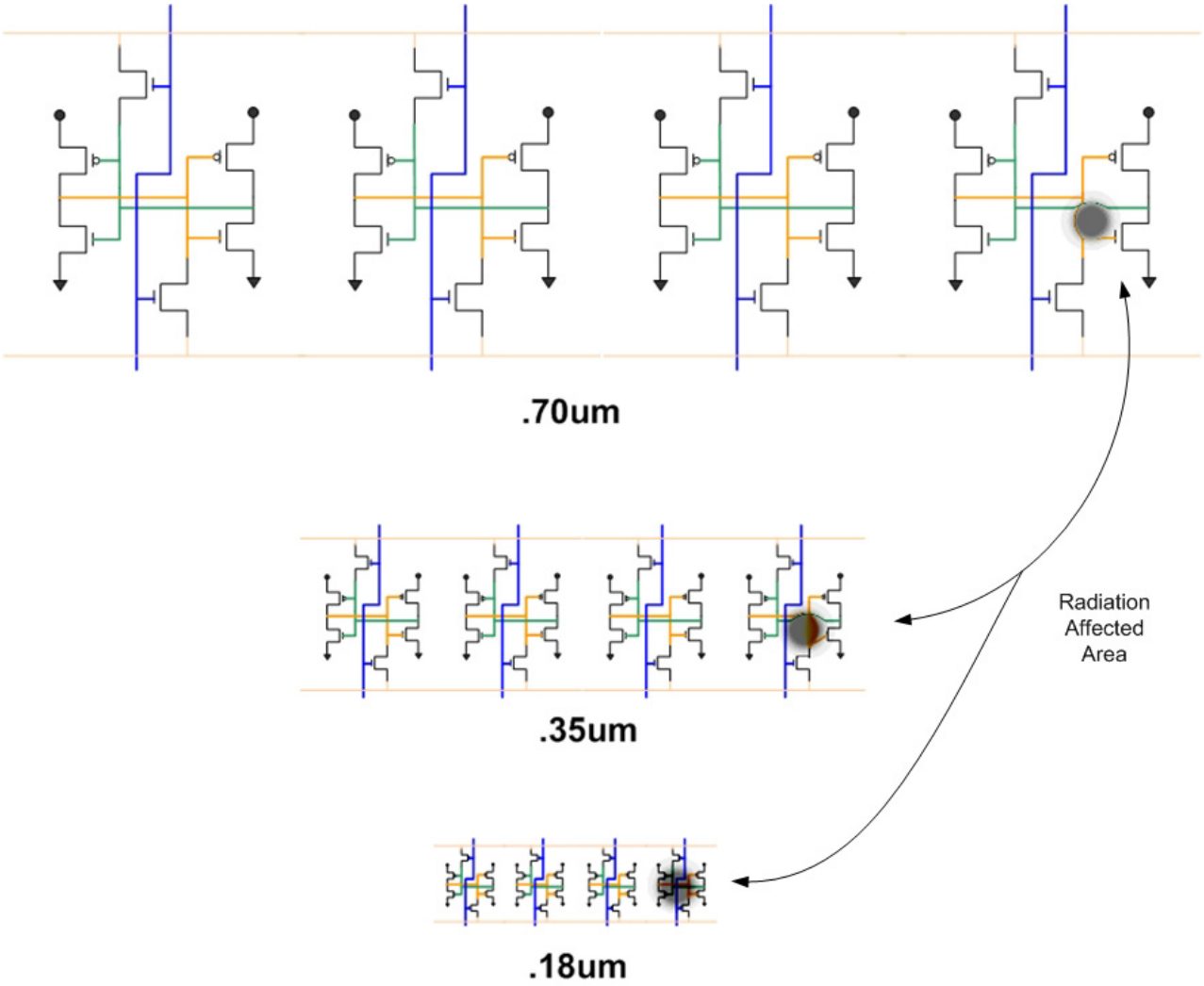


**Figure 9 - Radiation Effects as Geometries Shrink**

However, all is not lost for the future of CMOS storage cells. We have developed a methodology to take advantage of our SERT cell at smaller feature sizes as well. We have created a Double-Bit Spatially Protected Memory Cell, which uses the same fundamental schematic design of the SERT cell, but spreads out the critical nodes. As seen in figure 9, the storage circuit for a single memory bit can be spread out, greatly reducing the likelihood of a single heavy ion creating an upset within the cell.

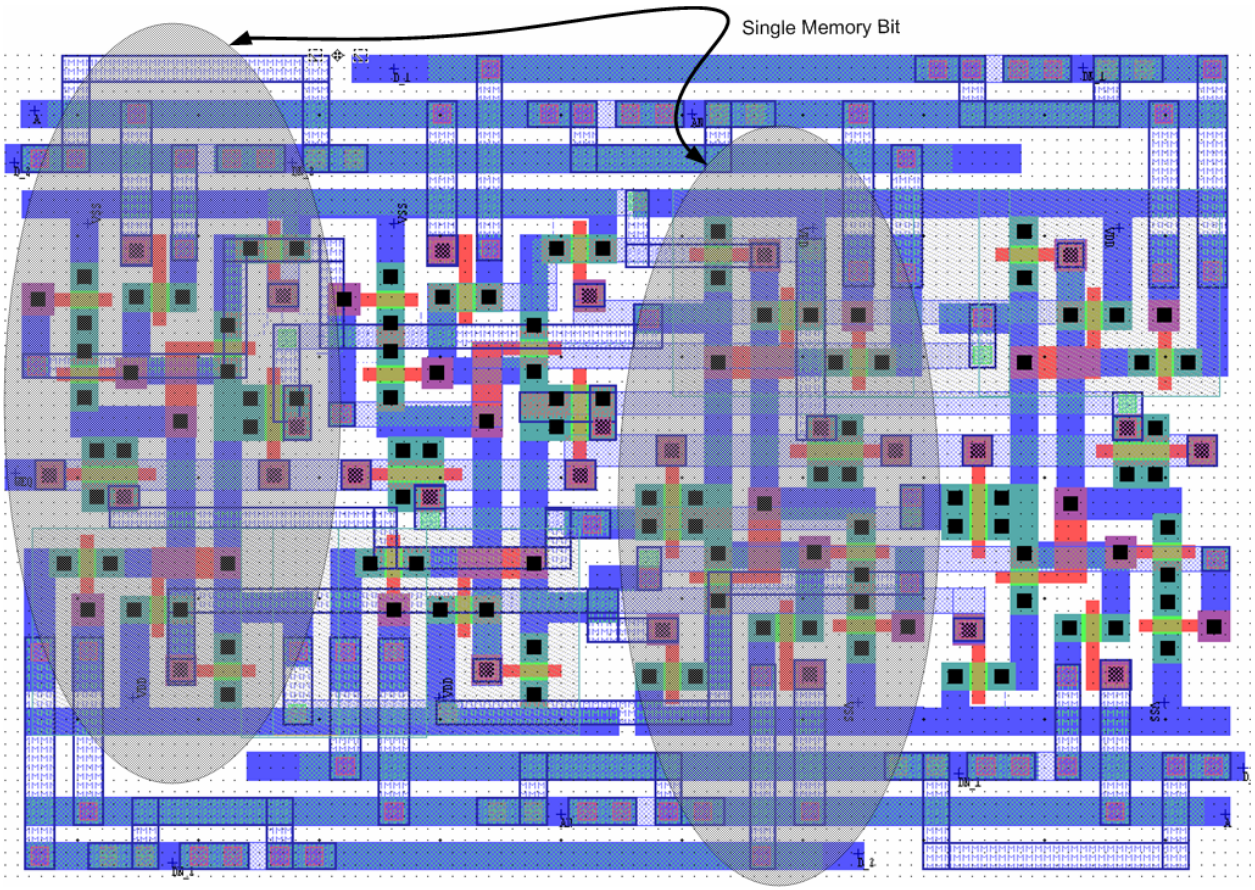


**Figure 10 - Double-Bit Spatially Protected SERT Cell**

The initial layout shown in figure 10 implements the solution for spacing critical nodes. The size will be slightly less than two SERT cells due to the overhead of creating a cell. Since storage is most often used in groups of at least 8, this will result in a more area-efficient layout of memories. There are rare cases where one storage element within the cell will go unused, but since our cells are quite area-efficient in general compared with other solutions such as the DICE cell, we still recommend this approach.

The simulation waveforms shown in figure 11 exhibit the storage nature of the cell. SEU simulations with SPICE also showed proper functionality in the event of charge deposition on critical nodes, and in the case where charge is deposited on a critical node for two different storage elements with one SEU event. This is the desired result, and shows that this approach is valid.

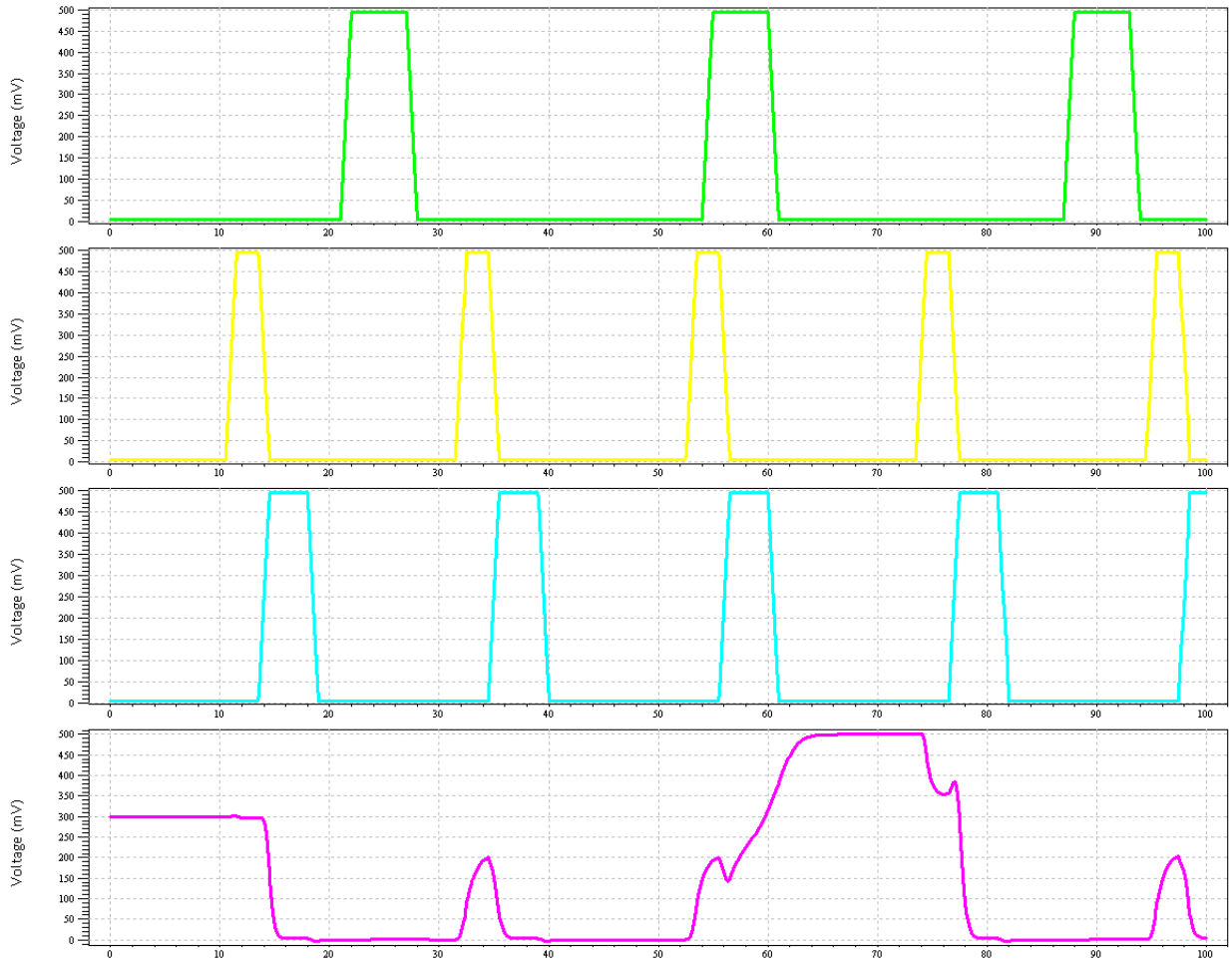


**Figure 11 - Simulation of Double-Bit Spatially Protected SERT Cell**

## CHOOSE ARCHITECTURE FOR LARGER-SCALE IMPLEMENTATION

Since 0.35um, the technology node where we are currently building ULP/RT parts, is being replaced by 0.18um, and even smaller geometries, we feel that a memory implementation using the Double-Bit SERT Cell would solve our current radiation issues, while preparing us well for embedded memory in future technology nodes.

We will therefore concentrate our efforts on building fully Rad-Hard Embedded Memories using the Double-Bit SERT Cell, rather than using EDAC protection or making larger, less area-efficient single-bit SERT cells. However, other methods will be used on the test chip for direct comparison.

# *IMPLEMENTATION PLAN*

## ARRAY SIZING APPROACH

Using physical design tools and analysis, we determined that embedded memories will be built in groups, starting with the double-bit cell, building that up to a byte-wide block, and so on up to large memory arrays. Byte-wide cells can be used as-is for registers, or grouped with others to create 16-bit and 32-bit wide registers. Trading drive strength and routing issues against the desire to be as compact as possible, we determined that the best size for a memory block is 1 Kbytes. Memories of greater size will be built of these 1K blocks arranged in array fashion around the remaining logic of the chip being built.

## DESIGNS SELECTED FOR PHASE II IMPLEMENTATION

For phase II, we will propose to build two devices. First, a test device, which contains memories designed using different techniques for comparative purposes would be built. This will allow 'apples-to-apples' testing using a single silicon chip. The device would contain at least the following circuits:

| | **Standard 6-transistor Memory** | **Single-bit Memory** | **Dual-bit Memory** |
|---|---|---|---|
| **Single-Cell** | X | X | X |
| **Register** | X | X | X |
| **1K Block** | X | X | X |

In addition, a functional chip design will be built that requires an on-chip memory block. We will likely choose a processor for this test. We will configure embedded memory for the chip using the Dual-Bit Memory in an array of more than one 1K block, and build an entire chip as the first demonstration of the technology.

The test chip will be subjected to radiation testing to prove the design techniques and to gather quantitative data regarding relative performance. We fully expect to see errors on the 6-transistor cell-based memory, and a great reduction in error count in the radiation-hard memory blocks made up of Double-Bit SERT Cells.

# Conclusion

During the course of this SBIR, we met the goal of developing an approach to creating and implementing Radiation Tolerant memory blocks using our Ultra-Low-Power technology.
We addressed the issue of reduced feature size and its effect on critical node placement. Our existing Cool-RAD™ standard cell library elements are fully compatible with the Double-Bit SERT Cell memory proposed, allowing for ASICs of arbitrary complexity to be built. We chose a 1K-byte block size for embedded memory implementation based upon manageable block size and expected applications.

# Future Work

To prove the efficacy of this work, it is necessary to built and test devices. We propose to build first a test chip, with sufficient circuits to test and compare results of this and other methods, then a fully functional ASIC using the memory blocks developed here. We would also like to extend the theories tested here regarding critical nodes to non-ULP memories on a commercial 0.18um process to determine whether we can achieve similar levels of radiation tolerance on those processes, thereby allowing ASICs to be built using MOSIS for the smaller quantities normally required of space and military systems.

# References and Endnotes

[1] K. Joe Hass and Jody W. Gambles. Mitigating single event upsets from combinational logic. In *Proceedings of the 7th NASA Symposium on VLSI Design,* pages 4.1.1-4.1.10, October 1998.
[2] K. Joe Hass and Jody W. Gambles. Single event transients in deep submicron CMOS. In *Proceedings of the 42nd Midwest Symposium on Circuits and Systems*, pages 122-125, August 1999.

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[i] S. Whitaker, J. Canaris, and K. Liu. “SEU Hardened Memory Cells For A CCSDS Reed Solomon Encoder”. *IEEE Transactions on Nuclear Science*, 38(6):1471-1477, December 1991.

[ii] L. R. Rockett, Jr. “An SEU-Hardened CMOS Data Latch Design”. *IEEE Transactions on Nuclear Science*, 35(6):1682-1687, December 1988.

[iii] M. Xapsos, G. Summers, E., "Enhanced Total Dose Tolerance of Bulk CMOS Transistors Fabricated for Ultra-Low Power Applications" *IEEE Transactions on Nuclear Science,* Vol 46, No. 6, pp. 1697 -1701, December 1999.

[iv] DARPA Rad-Hard By Design Workshop, “HBD Target Radiation Levels”, February 2003

[v] NASA Practice No. PD-ED-1258, “Space Radiation Effects on Electronic Components in Low-Earth Orbit”, April 1996

# APPENDIX A – SPICE SIMULATION FILES

```
* Circuit Extracted by Tanner Research's L-Edit Version 10.00 / Extract Version 10.00 ;
* TDB File:  V:\CN1080-MDA\Eng\Layout\MemoryCell.tdb
* Cell:  TwoBits  Version 1.190
* Extract Definition File:  Spice\mamin035_gta.ext
* Extract Date and Time:  04/22/2003 - 09:46

.include lvl49hith_020225_gta.md

* WARNING: Node/Element Name Conflicts Found.  The following are the
*          Node/Element names that have been renamed.
* Node A has been modified to A_1
* Node AN has been modified to AN_1
* Node D_1 has been modified to D_1_1
* Node D_2 has been modified to D_2_1
* Node DN_1 has been modified to DN_1_1
* Node DN_2 has been modified to DN_2_1

* NODE NAME ALIASES
*      1 = VSS (31.45,7.5)
*      1 = VSS (22.6,7.5)
*      2 = VDD (30.15,21.25)
*      2 = VDD (21.3,21.25)
*      4 = VSS (9.15,21.4)
*      4 = VSS (0.3,21.4)
*      5 = VDD (10.45,7.65)
*      5 = VDD (1.6,7.65)
*      51 = A (-1.25,24.65)
*      52 = DN_1 (29.1,25.9)
*      53 = D_1 (9.15,25.85)
*      54 = AN_1 (17.8,24.55)
*      55 = D_2_1 (-1.85,23.15)
*      56 = DN_2_1 (6.2,23.15)
*      57 = A_1 (33.25,4.25)
*      58 = DN_2 (2.75,2.85)
*      59 = D_2 (22.6,3.1)
*      60 = AN (14,4.25)
*      62 = D_1_1 (33.75,5.6)
*      63 = DN_1_1 (25.5,5.45)
*      70 = WEQ (-1.8,14.15)

Cpar1 49 0 C=6.9152825f
Cpar2 A 0 C=6.89516f
Cpar3 D_1 0 C=5.1108f
Cpar4 AN_1 0 C=6.94752f
Cpar5 DN_2_1 0 C=5.65653f
Cpar6 A_1 0 C=6.88898f
Cpar7 AN 0 C=6.94752f
Cpar8 61 0 C=8.36938f
Cpar9 DN_1_1 0 C=5.60091f
Cpar10 64 0 C=6.81486f
Cpar11 65 0 C=6.7284175f
Cpar12 66 0 C=5.0869175f
```

Cpar13 67 0 C=8.22679f
Cpar14 68 0 C=7.5506025f
Cpar15 WEQ 0 C=11.294623f
Cpar16 75 0 C=8.8697f
Cpar17 76 0 C=6.9838125f
* Warning: Node 78 has zero nodal parasitic capacitance.
* Warning: Node 79 has zero nodal parasitic capacitance.
* Warning: Node 80 has zero nodal parasitic capacitance.

M1 VDD 75 49 80 PH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (20.4 18.3 20.75 19.1)
M2 75 49 VDD 80 PH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (18.15 20.3 18.95 20.65)
M3 DN_2_1 AN_1 49 80 PH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (22.45 16.95 22.8 17.75)
M4 64 68 VDD 79 PH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (11 9.8 11.35 10.6)
M5 VDD 64 68 79 PH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (12.8 8.25 13.6 8.6)
M6 64 AN DN_1_1 79 PH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (8.95 11.15 9.3 11.95)
M7 76 61 VDD 79 PH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (2.15 9.8 2.5 10.6)
M8 VDD 76 61 79 PH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (3.95 8.25 4.75 8.6)
M9 76 AN DN_2 79 PH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (0.1 11.15 0.45 11.95)
M10 VDD 67 65 80 PH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (29.25 18.3 29.6 19.1)
M11 67 65 VDD 80 PH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (27 20.3 27.8 20.65)
M12 DN_1 AN_1 65 80 PH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (31.3 16.95 31.65 17.75)
M13 75 A_1 D_2 78 NH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (20.35 9.25 20.7 10.05)
M14 3 76 VSS 78 NH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (17.05 7.85 17.4 8.65)
M15 3 49 75 78 NH L=350n W=800n AD=720f PD=3.4u AS=1.6p PS=4.05u $ (18.15 10.95 18.95 11.3)
M16 75 WEQ 77 78 NH L=350n W=1.6u AD=1.6p PD=4.05u AS=1.44p PS=5u $ (17.05 12.2 17.4 13.8)
M17 71 75 49 78 NH L=350n W=800n AD=720f PD=2.6u AS=720f PS=3.4u $ (22.3 11.7 23.1 12.05)
M18 VSS 61 71 78 NH L=350n W=800n AD=720f PD=3.4u AS=720f PS=2.6u $ (22.3 9.55 23.1 9.9)
M19 49 WEQ 66 78 NH L=350n W=1.6u AD=1.44p PD=5u AS=1.44p PS=5u $ (21.15 14.6 22.75 14.95)
M20 D_1 A 68 78 NH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (11.05 18.85 11.4 19.65)
M21 VSS 65 6 78 NH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (14.35 20.25 14.7 21.05)
M22 68 64 6 78 NH L=350n W=800n AD=1.6p PD=4.05u AS=720f PS=3.4u $ (12.8 17.6 13.6 17.95)
M23 69 WEQ 68 78 NH L=350n W=1.6u AD=1.44p PD=5u AS=1.6p PS=4.05u $ (14.35 15.1 14.7 16.7)
M24 64 68 72 78 NH L=350n W=800n AD=720f PD=3.4u AS=720f PS=2.6u $ (8.65 16.85 9.45 17.2)
M25 72 67 VSS 78 NH L=350n W=800n AD=720f PD=2.6u AS=720f PS=3.4u $ (8.65 19 9.45 19.35)
M26 50 WEQ 64 78 NH L=350n W=1.6u AD=1.44p PD=5u AS=1.44p PS=5u $ (9 13.95 10.6 14.3)
M27 D_2_1 A 61 78 NH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (2.2 18.85 2.55 19.65)
M28 VSS 49 7 78 NH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (5.5 20.25 5.85 21.05)
M29 61 76 7 78 NH L=350n W=800n AD=1.6p PD=4.05u AS=720f PS=3.4u $ (3.95 17.6 4.75 17.95)
M30 66 WEQ 61 78 NH L=350n W=1.6u AD=1.44p PD=5u AS=1.6p PS=4.05u $ (5.5 15.1 5.85 16.7)
M31 76 61 73 78 NH L=350n W=800n AD=720f PD=3.4u AS=720f PS=2.6u $ (-0.2 16.85 0.6 17.2)
M32 73 75 VSS 78 NH L=350n W=800n AD=720f PD=2.6u AS=720f PS=3.4u $ (-0.2 19 0.6 19.35)
M33 77 WEQ 76 78 NH L=350n W=1.6u AD=1.44p PD=5u AS=1.44p PS=5u $ (0.15 13.95 1.75 14.3)
M34 67 A_1 D_1_1 78 NH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (29.2 9.25 29.55 10.05)
M35 8 64 VSS 78 NH L=350n W=800n AD=720f PD=3.4u AS=720f PS=3.4u $ (25.9 7.85 26.25 8.65)
M36 8 65 67 78 NH L=350n W=800n AD=720f PD=3.4u AS=1.6p PS=4.05u $ (27 10.95 27.8 11.3)
M37 67 WEQ 50 78 NH L=350n W=1.6u AD=1.6p PD=4.05u AS=1.44p PS=5u $ (25.9 12.2 26.25 13.8)
M38 74 67 65 78 NH L=350n W=800n AD=720f PD=2.6u AS=720f PS=3.4u $ (31.15 11.7 31.95 12.05)
M39 VSS 68 74 78 NH L=350n W=800n AD=720f PD=3.4u AS=720f PS=2.6u $ (31.15 9.55 31.95 9.9)
M40 65 WEQ 69 78 NH L=350n W=1.6u AD=1.44p PD=5u AS=1.44p PS=5u $ (30 14.6 31.6 14.95)

VB1 80 0 0
VB1a 79 0 0
Vb0 78 0 0

```
* Rail Voltages
*VDD VDD 0 1.00
VDD VDD 0 0.500
VSS VSS 0 0

* Control Lines
VAddr A 0 dc 0 BIT ({ 3(00000000011100)  10000(0)} pw=1.5n on=0.495 off=0.005 rt=1n ft=1n)
VAddrn AN 0 dc 0 BIT ({ 3(11111111100011) 10000(1)} pw=1.5n on=0.495 off=0.005 rt=1n ft=1n)
VAddrR A_1 0 dc 0 BIT ({ 3(00000000011100) 10000(0)} pw=1.5n on=0.495 off=0.005 rt=1n ft=1n)
VAddrnR AN_1 0 dc 0 BIT ({ 3(11111111100011) 10000(1)} pw=1.5n on=0.495 off=0.005 rt=1n ft=1n)

VWEQ WEQ 0 dc 0 BIT ({ 3(00000001100000) 10000(0)} pw=1.5n on=0.495 off=0.005 rt=1n ft=1n)

*Data Cell 1
VData D_1 0 dc 0 BIT ({ 3(00000000000000011110000) 10000(0)} pw=1.5n on=0.495 off=0.005)
VDatan DN_1 0 dc 0 BIT ({ 3(11111111111111100001111) 10000(1)} pw=1.5n on=0.495 off=0.005)
VDataR D_1_1 0 dc 0 BIT ({ 3(00000000000000011110000) 10000(0)} pw=1.5n on=0.495 off=0.005)
VDatanR DN_1_1 0 dc 0 BIT ({ 3(11111111111111100001111) 10000(1) } pw=1.5n on=0.495 off=0.005)

*Data Cell 2
V2Data D_2 0 dc 0 BIT ({0000000000000000000000} pw=2n on=0.495 off=0.005)
V2Datan DN_2 0 dc 0 BIT ({0000000000000000000000} pw=2n on=0.495 off=0.005)
V2DataR D_2_1 0 dc 0 BIT ({0000000000000000000000} pw=2n on=0.495 off=0.005)
V2DatanR DN_2_1 0 dc 0 BIT ({0000000000000000000000} pw=2n on=0.495 off=0.005)

*.print tran V(49,0)
*.print tran V(75,0)

*.print tran V(68,0)
*.print tran V(64,0)

*.print tran V(61,0)
*.print tran V(76,0)

.print tran V(67,0)
*.print tran V(65,0)

.print tran V(A, 0)
.print tran V(WEQ, 0)
.print tran V(D_1, 0)
.print tran P(VDD)

*.print tran V(D_2, 0)

*.options maxmsg=0
.tran/op 100p 100n method=bdf

* Total Nodes: 80
* Total Elements: 937
* Total Number of Shorted Elements not written to the SPICE file: 0
* Output Generation Elapsed Time: 00.125 sec
* Total Extract Elapsed Time: 09.000 sec (9.000 sec)
.END
```