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13. ABSTRACT (Maximum 200 words)

Report developed under SBIR contract for topic A01-58. PHOCI is an optical imaging system that is suitable for both image capture and reception of optical communications data. The envisioned system, called PHOCI includes a novel image/data capture chip that imbeds a high-speed optical data communications receiver technology into the image capture array of a digital video camera system. In addition to the development of a new image/data capture chip, the system includes the design of a hardware interface that allows the PHOCI system to pass both image and optical communication data through a USB (or similar communications link) to a COTS host computer. In addition to providing the device drivers necessary to communicate with the PHOCI hardware, the system software provides the data structures and graphical user interface (GUI) that allow a system operator to see the camera image along with the location and recent movement vector for communication sources in the image. The phase 1 activity illustrated the technical feasibility of the device and discovered that the technology is commercially feasible especially for harsh environments that are not normally well suited to electromagnetic communications such as that found in a factory floor.

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1. Introduction

This final report summarizes the accomplishments in the Phase I effort on the PHOCI project. The PHOCI Phase I effort established the technical and commercial feasibility of creating a fully functional optical imaging system. The system included a novel image/data capture chip that embeds high-speed optical data communications receiver technology into the image capture array of a digital video camera system.

In addition to the development of this new, special-purpose imaging chip, Phase I evaluated the design of a hardware interface that allows the PHOCI system to pass both image and communication data through a USB (or similar communications port) to a COTS portable computer.

Also during the Phase I effort, system software was developed that demonstrates the graphical user interface of a mock PHOCI application. System level analysis was done to provide a platform for high-level simulation and evaluation of algorithms required to utilize the PHOCI sensor data.

The results of the Phase I are summarized in the following sections:

- *PHOCI Architecture*: Summarizes the high-level architecture and functional overview of the Phase I PHOCI system design.
- *PHOCI Sensor*: Summarizes the implementation of the data-integrated CMOS imaging sensor, as well as specific accomplishments relating to the proof-of-concept sensor fabricated during the Phase I effort.
- *PHOCI Board:* Summarizes the architecture and design of the support hardware required to interface with the sensor and manage sensor resources.
- *PHOCI Host*: Summarizes the impact of standard communication interface technologies used to interface with the PHOCI board on overall system performance. This section also describes the mock PHOCI application software and simulation platform.

2. PHOCI Architecture

A significant portion of the Phase I effort was concentrated on refining the initial design presented in the Phase I proposal and investigating key technical issues through modeling, simulation, and prototyping. The resulting architecture of PHOCI is depicted in Figure 1. This figure shows the interaction between the three high-level components that compose the overall solution. The operation of the system can be summarized as follows:

- A photo-detector within each pixel senses the intensity of the incident light and presents this signal to both a threshold circuit and an analog sample/hold circuit. The threshold circuit is calibrated to detect the presence of an active laser communication source. The sample/hold circuit is used to capture and hold an image intensity value.

- Based on a data-sampling clock, the output of the threshold circuit is clocked into the pixel buffer. If the detector is above the threshold, a logic '1' bit is stored in the buffer, otherwise a logic '0' bit is stored. If a '1' is detected, the Active Pixel Latch is set marking the pixel as 'active' (i.e. holding communications data).
- Based on the video frame rate clock, the sample/hold circuit captures the detector signal in order to acquire an image incident on the sensor chip.
- The video controller is responsible for collecting the active/inactive status of each pixel and routing the analog video signals through the A/D converter to the video buffer. Note: separate video and data busses on the sensor chip allow the video and data paths to operate independently.
- The data channel controller is responsible for collecting communications data from the pixel buffers. Since the bandwidth required to collect high-speed communications data from all pixels would be astronomical, the data channel controller maintains a list of 'active channels' that it collects data from. This list is held in the active channel buffers. One of the key technical issues for PHOCI is the design of algorithms used to select data channels and optimize the use of available bandwidth while maintaining the integrity of the communications stream.
- The host link controller is responsible for processing commands received from the host computer as well as packaging and delivering data from both video and communications data buffers to the host computer across the particular host link technology.
- The PHOCI system driver is a low-level software component that manages the communications link between the COTS host computer and PHOCI system hardware. The driver interfaces with a communications stack to abstract the details of the PHOCI technology and provide application developers with a standard interface for integrating video and data communications into their applications.
- By interfacing with the communications stack, application developers can develop a variety of applications that require video acquisition, high-speed optical communications, and communications data source tracking.

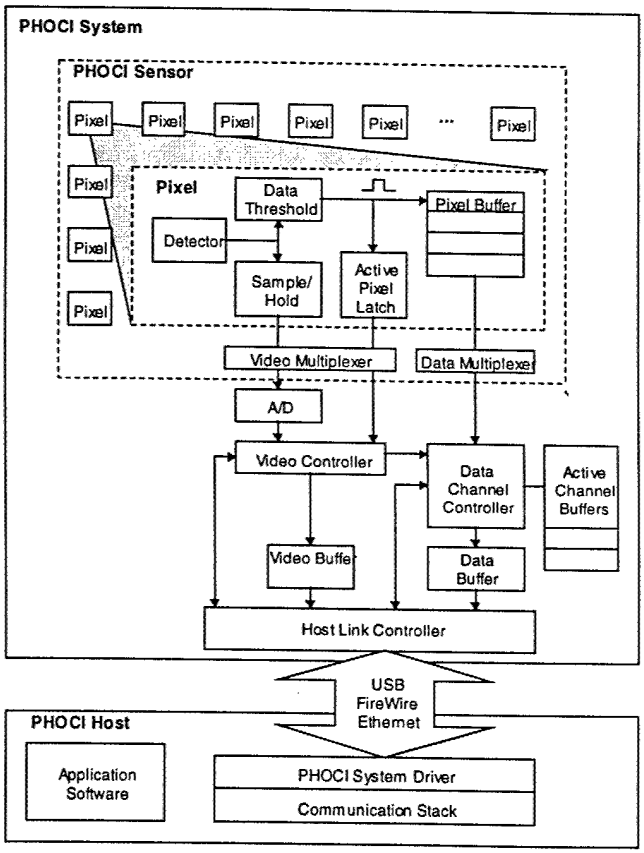


Figure 1– PHOCI Architecture

In order to establish the feasibility of this design, the Phase I effort addressed key technical issues by developing prototypes of the various system components. For the PHOCI sensor, a tiny-chip design that contained prototypes of the detector, sample/hold, threshold detector, and pixel buffer was developed and submitted for fabrication. For the PHOCI system, the video controller, and data channel controller were modeled and simulated using VHDL, with the resulting designs targeted for implementation on an FPGA. For the PHOCI host, an application was developed that provided a mock GUI, and high-level system simulation which was also used to

investigate various behavioral models of the PHOCI architecture and required algorithms.

The following sections provide a detailed presentation of the Phase I results.

3. PHOCI Sensor

The image/data capture device is the heart of the PHOCI system. The primary function of this component is to extract both image information and optical communications data from an input image. While the device is conceptually similar to a digital video camera, the merging of image capture and optical data acquisition exceed the capabilities of standard digital video cameras, which are not suitable for acquisition of high-speed optical communications data.

As suggested by Figure 1, one of the benefits of the PHOCI sensor over a standard digital video camera is the ability to independently read image data and communications data from separate pixels. This allows video content to be read from the sensor in a framed fashion at speeds that are compatible with low to medium frame rate digital video systems. In addition, communication data can be read from individual pixels within the sensor at data rates that are much faster than the video frame rate could support.

To demonstrate the feasibility of this novel image/communications sensor, we have developed a proof-of-concept sensor chip. While this small sensor chip (limited to 7 x 7 pixels) is not suitable for true imaging applications, it allows us to test our device concepts with cost-effective custom hardware. In addition to gaining some insight to the functionality and performance requirements for the PHOCI sensor, fabrication of the sensor chip is allowing us to develop the support/control hardware that will enable simultaneous acquisition of image and communications data. Further, by integrating the PHOCI sensor with board level control circuitry, it has been possible to explore the impact of connecting the PHOCI system to a COTS computer with a commercially available data link technology (e.g., USB, FireWire, and Ethernet).

In the following sections we describe the proof-of-concept PHOCI sensor developed during the Phase I effort.

3.1. Tiny-Chip Architecture

Based on a Photonic VLSI device technology that is compatible with commercial CMOS fabrication processes, the PHOCI sensor includes an array of multi-function pixels and the support circuitry required to read image and/or communications data from any pixel in the array. For the proof-of-concept prototype we have developed a sensor chip with a 7 x 7 pixel array. The chip is being fabricated using the ABN 1.5 µm CMOS process available from American Microsystems, Inc. The first chip (a 2.2 mm x 2.2 mm tiny chip) is being fabricated through MOSIS using the AMI foundry.

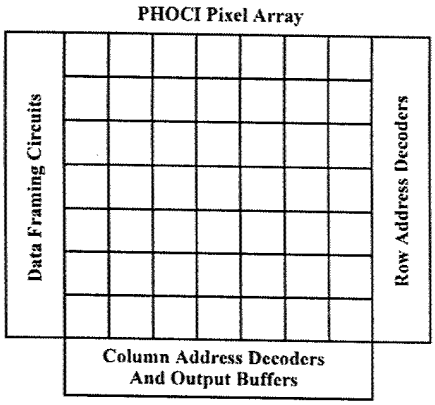


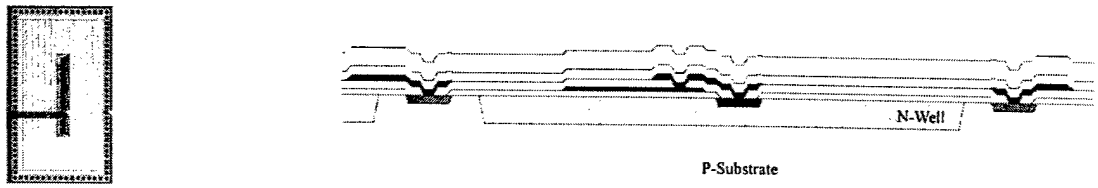
Figure 2 Floor plan for the tiny chip

Figure 2 shows a basic floor plan for the tiny chip. As suggested in the figure, the video and communications data held in each pixel can be accessed by providing both row and column addresses. Since the video and data addressing circuits are completely independent, it is possible to access image data from one pixel while accessing communications data from a second pixel.

The functionality of this first iteration prototype is limited to just the capture of image and communications data. Due to limitations of chip size and process technology the tiny-chip is only capable of capturing a very limited image size (7 x 7 pixels) and 4 bits of communication data from up to 2 simultaneous data channels. Further, the chip does not include any clock recovery or data synchronization circuitry. Thus, this first iteration prototype will not be well suited for collecting data transmitted over large distances.

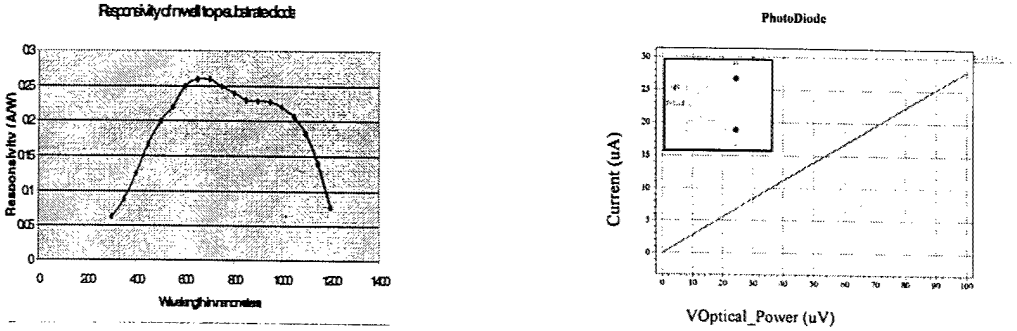
Regardless of these limitations, the chip is well suited to meet the primary objectives that have been driving the development of this PHOCI prototype. These objective include:

- Demonstrate the feasibility of using a single sensor for collecting both analog image information and digital communications data.



a) b)

Figure 4 Photodetector layout (a) and device cross-section (b) for the photodetector used in the tiny chip.



a) b)

Figure 3 Simulated spectral responsivity (a) and I-L characteristics (b) of the photodetector used in the tiny chip.

- Identify the technological limitations that ultimately determine systems size and performance.
- Provide a basic sensor that will enable the development of an application test bed where data management algorithms, support hardware, and system software can be evaluated.

The following sections describe each of the key circuit elements that make up PHOCI sensor.

3.2. Photo Detector

The PHOCI sensor chip uses a photodetector technology that is monolithically integrated with the CMOS circuitry. For this initial prototype chip, we are using the N-well to P-Substrate diode as a pn junction photodiode. Although the frequency response of this detector structure is limited a few hundred kHz by the slow recombination of electron hole pairs in the Silicon substrate, detectors of this type have been well characterized by members of the development team and have proven to be dependable photodetectors with repeatable I-V and I-L characteristics.

Figure 4 a) shows an image of the detector layout used in the tiny-chip design. The detector has dimension 45μm x 86.25μm. A cross section of the detector structure is shown in Figure 4 b). Results from previous work have shown this detector to have an optical responsivity as shown in Figure 3 a. The shorter wavelength cut-off in the optical responsivity curve is associated with absorption of the optical signal near the silicon surface. The long wavelength cut-off in the optical responsivity characteristics is associated with the fact that the detector becomes transparent for wavelengths where the photon energy is less than the bandgap energy of silicon.

To facilitate SPICE level simulation of the full pixel, a SPICE sub-circuit was developed to simulate the photodetector responsivity. Figure 3b shows the I-L characteristics generated using the sub-circuit shown in the figure inset. It should be noted that the scaling factor used in the voltage dependent current source can be used to simulate the optical responsivity of the detector. For the visible to near infrared regions of the optical spectrum, the photodetector structure is expected to have an optical responsivity in the range from 0.23-0.29 A/W. This value has been experimentally confirmed by previous experimental work.

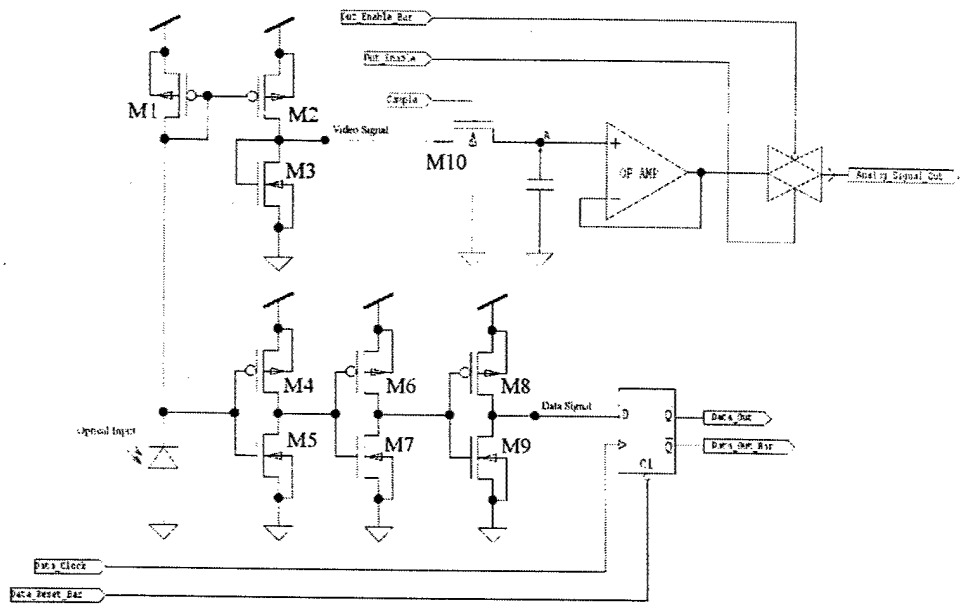


Figure 5 Circuit diagram for the photoreceiver circuit that captures both the digital and video information.

3.3. Image and Data Detection

Figure 5 shows the circuit diagram for the photoreceiver circuit incorporated into the prototype sensor. The circuit includes both image and data detection circuitry. The image detection portion of the photoreceiver circuit functions in the following manner:

- Optical illumination of the photodetector causes a photocurrent to flow through transistor M1.
- The photocurrent is replicated and amplified by a factor of two by the current mirror (transistors M1 and M2).
- The replicated photocurrent is then driven through an active load device M3 causing a change in the voltage level at the node labeled "Analog Signal".
- When the "Analog Sample" line is pulsed high, the storage capacitor is charged up to the voltage on the "Analog Signal" node.
- When the "Optical Enable" lines are set appropriately, then the "Analog Output" line goes from a high impedance state to the output voltage generated by a simple OP Amp based unity gain buffer.

The data detection portion of the photoreceiver circuit functions in the following manner:

- Optical illumination of the photodetector causes a photocurrent to flow through transistor M1.
- While transistor M1 serves as the input side of a current mirror for the image detection circuit, it acts as an active load device for the data detection portion of the photoreceiver circuit. As the photocurrent increases, the voltage dropped across transistor M1 increases, leading to a decrease in the voltage across the photodetector.
- Transistors M4-M7 act as a pair of push-pull amplifiers that amplify the photodetector voltage.
- Transistors M8-M9 implement an inverter that is used as a threshold circuit to produce digital logic levels suitable for latching into the data buffer.

Figure 6 shows simulated I/O characteristics for the photoreceiver circuit. As shown in the figure, the image detection circuit has an approximately linear response over the range of expected optical power

levels for image input. The data detection circuit has an optical power threshold of 21 μW. While this threshold value is significantly larger than the 50 nW threshold power desired in future applications, it is more than sufficient for operation of the prototype system being developed. Adjusting the power threshold level is relatively easy with the addition of larger load transistors and more amplification stages. These components were not included in the tiny chip in order to conserve space in the pixel layout and allow for a larger number of pixels in the prototype sensor.

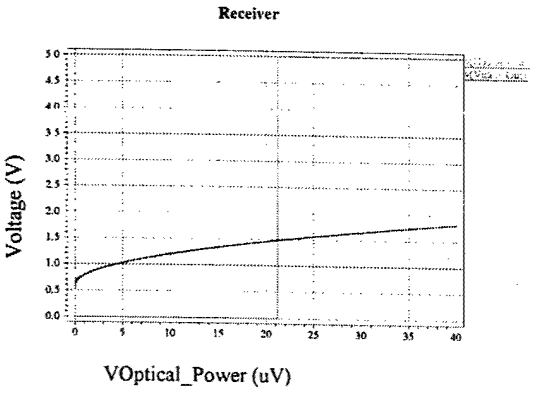


Figure 6 Simulated I/O charactersitics for the photoreceiver circuit. Note: Optical power is shown in units of V due to the use of a voltage controlled current source to emulate the photodiode.

3.4. Pixel Buffering

Figure 7a shows the circuit diagram for the data storage buffer. This 4-bit buffer is based on a simple SRAM cell shown in Figure 7b. The input to the storage buffer comes from a D flip-flop that holds the detected data bit in the photoreceiver circuit. As indicated in the figure, the data bit is passed to all 4 storage cells simultaneously. One of four write enable lines is then activated to store the detected data bit into the appropriate storage buffer location. A support circuit outside of the pixel array controls framing of the data bits. Currently the data framing circuit continuously cycles through activation of the 4 storage cells in the data buffer.

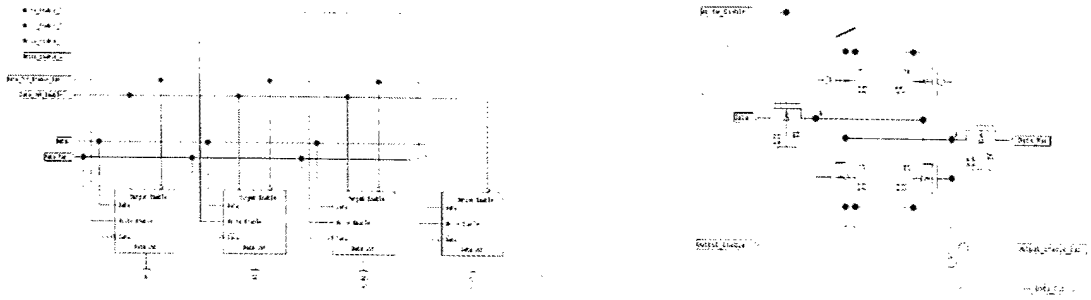
The output from each SRAM cell is passed through a tri-state buffer to a common 4-bit data bus that runs through each column in the sensor array. This allows for independent row selection during the data read-out process.

Figure 8 shows a simulated timing diagram for the data read, data latching and data storage processes. As shown in the diagram data is latched on the rising edge of the data clock. When the write enable line is activated the value of the data bit is stored into the appropriate bit position of the storage buffer.

3.5. Support Circuitry and External Interface

The prototype chip includes three basic support circuits. First as described above, a data framing circuit controls the generation of the write-enable signals that are passed to the data storage buffers in the pixel array. This circuit is implemented with a 4-bit circular shift register. A reset signal loads the shift register with a '1' in the first bit position and a '0' in all other bit positions. After initialization of the circuit with the reset signal, the '1' is cyclically shifted through the register using the same data clock used to latch data into the photoreceivers D flip-flop.

Row address decoders are included for both the video and data output paths. These decoders which are implemented with 3 input NAND gates generate the video out enable and data out enable signals that are



a) b)

Figure 7 a) Circuit diagram for the data storage buffer. b) Circuit diagram for the SRAM used in the data storage buffer.

distributed across each row in the pixel array.

Column address decoders are included for both the video and data output paths. Like the row decoders, the column decoders use NAND gates to generate bus enable lines. In addition, the column decoders include the tri-state buffers that allow the 7 video and data buses (connected through each column of the pixel array) to be merged into single output buses for passing video and digital data off chip.

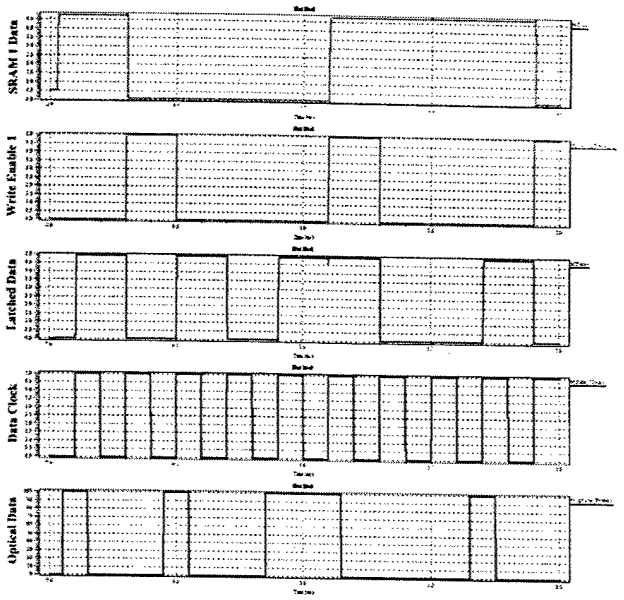


Figure 8 Timing Diagram for the first cell in the data storage buffer.

3.6. Sensor Characterization, Testing, and Integration

Figure 9 shows images of the pixel layout and full chip layout. In addition to including all of the circuitry described above, the pixel in the upper right corner of the pixel array has been hard-wired to test pins. Using these pins it will be possible to test all of the critical circuitry inside the pixel and most of the support circuitry.

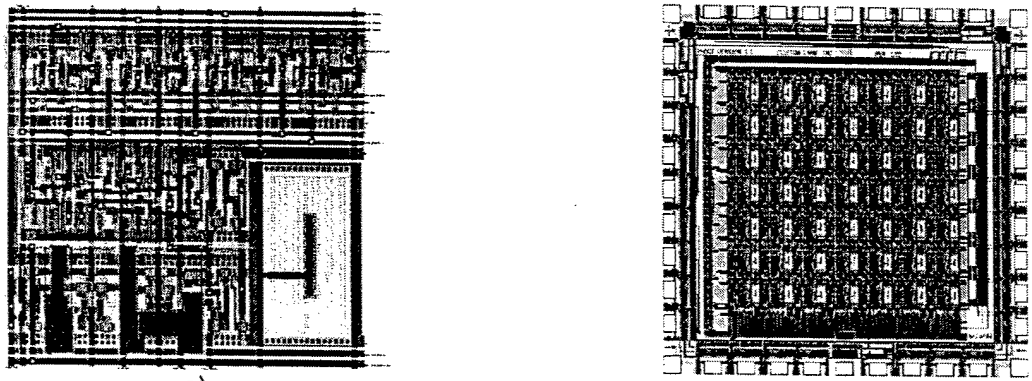
The full chip layout was submitted for fabrication on April 29, 2002. Chips arrived from the foundry on June 28, 2002. Testing was immediately initiated to verify the functionality of the test pixel with very promising results thus far. It is anticipated that full chip functionality will be verified by July 29, 2002.

Full scale chip testing will be followed by incorporation of the chip into 1) a simple test rig for chip evaluation at a remote site and 2) a PHOCI board as described in the following section. Completion of the simple test rig is anticipated for early August. Completion of the PHOCI board with complete support hardware is expected by mid -August.

4. PHOCI Board

The technical feasibility of the PHOCI board design was established during the Phase I effort by refining the design presented in the Phase I proposal through analysis, modeling, simulation, and prototyping of key functional elements. This portion of the Phase I effort addressed the following technical issues:

- The electrical interface of the sensor array including required control signals, data signals, and bus cycle timings.



a) b)

Figure 9 Pixel layout (a) and full chip layout (b) submitted for fabrication.

- The required size of the pixel data buffer, and pixel data bus width within the sensor for various active data channel counts, communication data rates, and system bus frequencies.
- The algorithms used by the system to make optimal use of sensor bandwidth to maximize the number of concurrent active data channels, and still provide data integrity and data source tracking.
- Tradeoffs of implementing system level functions in silicon (ASIC), programmable logic (FPGA), or software.
- The impact of various transmission protocols and encoding schemes on the performance of the PHOCI system.
- The maximum achievable throughput of the PHOCI system with respect to the host link technology (USB, FireWire, Ethernet), number of pixels, active data channel count, and communication data rate.

The board-level technical issues were addressed in the Phase I activity by developing a prototype implementation of the system for use with the tiny-chip sensor described in the previous section, performing mathematical analysis of system performance, and through high-level behavioral simulation of algorithms.

4.1. Tiny-chip Prototype System Architecture

Based on the tiny-chip sensor previously described, a preliminary implementation of the required support functions were designed and implemented in VHDL. The prototype system architecture was targeted for implementation using a FPGA prototype platform that allows for quick deployment of proof-of-concept designs in real hardware. Although the physical realization of a complete proof-of-concept system is not scheduled to occur until August 2002, after the fabrication and characterization of the tiny-chip sensor, valuable information about the PHOCI board design was gathered through modeling and simulation activities.

During Phase I, structural VHDL models of the video controller and data channel controller were developed to interface with the tiny-chip sensor. A VHDL behavioral model of the tiny-chip sensor was also developed that reflected the results of SPICE simulations performed on the evolving circuit design of the tiny-chip sensor array. The resulting system-level simulation provided a foundation for refining the interfaces between the various components. One result of this simulation was the required electrical pin-out of the tiny-chip. Another result was timing diagrams that fully described the operation of both the video path and data path for the proof-of-concept system.

4.2. Pixel Buffer Size and Pixel Data Bus Width

One of the major issues outlined in the Phase I proposal was the determination of the optimal size of the data buffer and data bus required by the pixel. Figure 10 shows just the components from Figure 1 that are responsible for controlling the flow of data through the PHOCI sensor/board. The constraint that determines the minimum size of the pixel buffer is simple; the pixel buffer must be emptied before it overflows. However, the amount of time it takes for this to occur depends on a number of inter-related factors.

- **D**: The data sampling clock frequency determines the rate that new data bits are clocked into the pixel buffer. Depending on the encoding scheme of the communications data, this clock rate may need to over-sample the incoming data stream in order to accommodate clock skew and variations in data rates among communication sources.

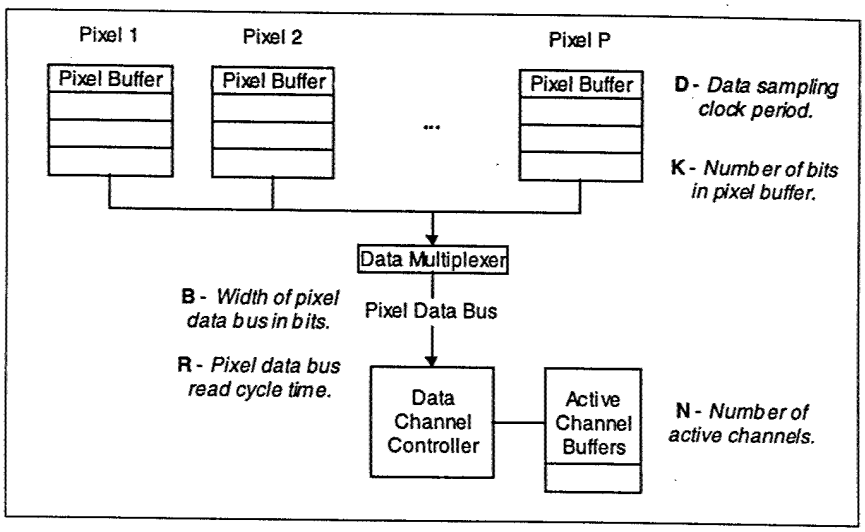


Figure 10 - Components from the PHOCI sensor and interface board that effect data flow in the PHOCI system.

- **K**: The size of the pixel buffer in bits. This is always a multiple of the pixel data bus width, thus the amount of time required to completely fill the pixel buffers is K/D.
- **B**: The width of the pixel data bus in bits.
- **R**: The pixel data bus frequency determines the amount of time required to read B bits from the pixel buffer, thus it requires K/(R*B) to completely transfer all data from a pixel buffer.
- **N**: The maximum number of simultaneous active data channels, thus the amount of time required to completely read all N pixel buffers is N*K/(R*B).

Given these variables and the data flow architecture depicted in Figure 10, one can guarantee that no incoming data bits will be lost as long as:

$$\frac{N*K}{R*B} \le \frac{K}{D} \quad \text{and} \quad \frac{N*D}{R*B} \le 1$$

Figure 11 summarizes the interdependence between the number of active channels and maximum sustainable communications data rate. Each line in the chart corresponds to a different data bus width or bus frequency.

This analysis clearly shows how design choices associated with the data bus on the PHOCI sensor will impact the overall performance of the system. The number of simultaneous active channels determines the theoretical maximum number of parallel data sources that the PHOCI system will be capable of receiving data from with 100% assurance that no communications data will be dropped. Depending on the algorithm used by the data channel controller to collect communication from data sources and track the position of data sources, the maximum number of simultaneous data sources may be less than the

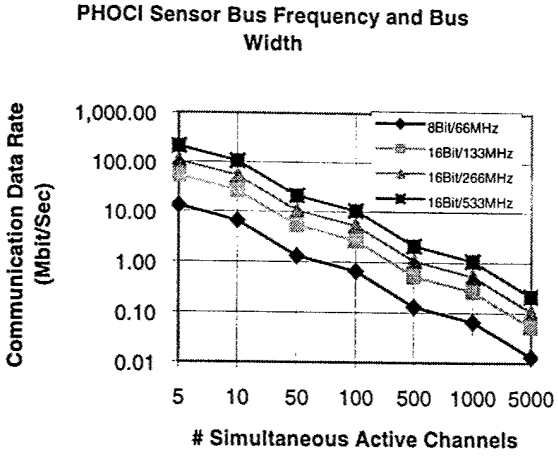


Figure 11: Effects of Pixel Bus Width and Frequency

theoretically achievable maximum. For example, if the data channel controller designates one channel as the primary channel but requires an additional four channels to be used for error correction, and to detect movement of the data source, the maximum number of simultaneous data sources would be one fifth of the maximum number of active channels determined from Figure 11.

Also note that in most communication networks the transmitted data occurs in bursts of packet data. This analysis demonstrates the maximum number of data sources that may communicate at the same time and determines the saturation limit of the PHOCI sensor. In a practical application, the PHOCI sensor can reassign its active channels across a greater number of bursty data sources as communication streams start and end.

Another significant point derived from this analysis is the impact that the implementation of the pixel data bus will have on performance. In applications where high-bandwidth communications are required, the data bus between the sensor array and the data channel controller may need to be moved onto the sensor chip itself in order to achieve the 500+ MHz bus frequency. For lower bandwidth systems or systems with lower channel counts, the data channel controller can be moved off chip into an FPGA.

4.3. Data Channel Controller

As mentioned in the previous sections, the data channel controller plays a critical role in the overall performance of the system. The data channel controller is responsible for optimizing the available pixel data bus bandwidth among multiple active channels in order to accurately receive communication data and track the movement of communication sources.

In the proof-of-concept tiny-chip system developed in the Phase I effort, the data channel controller simply monitors all pixels for communications. Since the tiny-chip sensor contains such a small number of pixels there are no significant bandwidth limitations placed on the pixel data bus.

In order to investigate the performance of various data channel controller algorithms to be used on a large-scale sensor array, a high level behavioral model of PHOCI was developed. The behavioral model of the PHOCI system and PHOCI sensor provide the simulated data displayed in the mock GUI application described in the following section.

4.4. FPGA Prototype System

As previously mentioned, an FPGA prototype system was selected to provide a suitable platform for the proof-of-concept system. The XSA-100 FPGA prototype board from Xess Corporation was selected. This prototyping platform provides a 100,000 gate Xilinx Spartan II FPGA with 16 Mbytes SDRAM, a VGA monitor port, a prototyping interface, and various push-buttons and LED's.

The final proof-of-concept system will utilize the resources of the XSA board to demonstrate the following:

- Allow for the direct measurement of sensor responsivity using the hardwired test pixel and laboratory test equipment.
- Demonstrate the measurement of spot intensity across the pixel array by displaying each of the pixel intensity levels on a VGA monitor connected to the XSA prototype board.
- Demonstrate the ability to detect communications data by displaying a unique color that indicates the presence of communications data at that pixel.
- Demonstrate the ability to accurately receive and distinguish between two separate laser sources by displaying a unique color that indicates either the presence of Channel A or Channel B at each pixel in the array.
- Demonstrate the ability to receive at least voice-grade communication bit streams.

As previously mentioned in this report, the proof-of-concept system has an anticipated completion date in mid-August. Upon completion of the characterization of the tiny-chip sensors, we will begin integrating the sensors into the FPGA prototype system.

5. PHOCI Host

The PHOCI host is an ordinary COTS computer system that executes the PHOCI system drivers and interfaces to the PHOCI system hardware. During the Phase I activity, a mock-up of an example PHOCI application was created, and analysis of various data link technologies was performed.

5.1. Host Data Link

The host computer interfaces with the PHOCI system hardware through a standard data link such as USB 1.0/2.0, IEEE1394 (FireWire), or Ethernet. Maximum bandwidth for these data link protocols is shown in the adjacent table.

Data Link Technology	Bandwidth (MBit/Sec)
Ethernet	10
USB 1.0	12
Fast Ethernet	100
IEEE 1394 (FireWire)	400
USB 2.0	480
Gigabit Ethernet	1000

In a PHOCI system, the bandwidth of the data link is divided among the video data, communication data, and control data transferred between the host computer and the PHOCI board. The amount of available bandwidth consumed by the video data stream depends on the frame rate of the PHOCI sensor, the number of pixels in the sensor array, and the amount of compression that is applied to the raw video data. The amount of available bandwidth consumed by the communication data stream depends on the communication data rate, and the number of simultaneously active communications data channels.

The choice of data link technology depends on the application of the PHOCI system. Figure 12 shows the relationship between the number of communication data sources and communication bit rates using various data link technologies under the following conditions:

- 384x288 sensor pixel array
- Video frame rate of 30 frames per second
- Average video compression ratio of 4:1
- An optical network utilization of 20%, meaning that due to the bursty nature of the laser communication sources, each data source is actively transmitting data only 20% of the time.

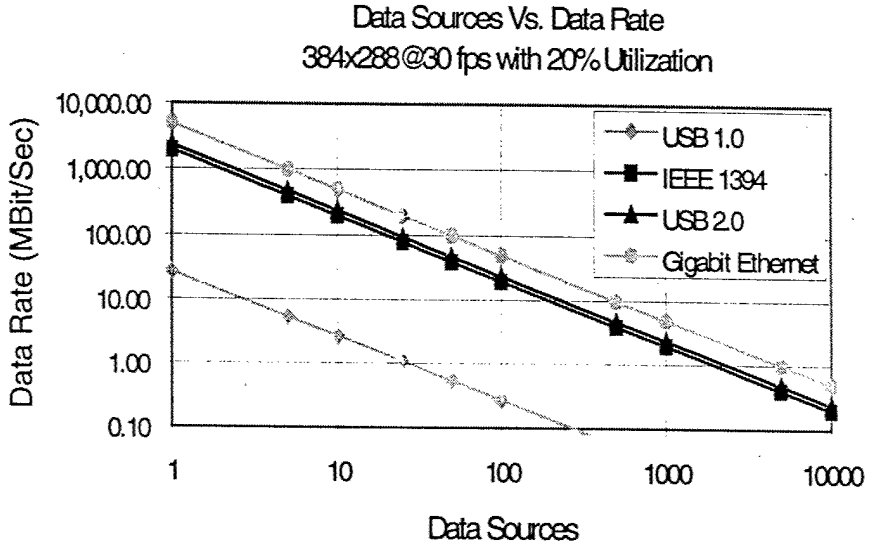


Figure 12: Host Link Data Sources vs. Data Rate

5.2. Host System Software

During the Phase I effort a mock-up of a PHOCI application was developed that provided a sample graphical user interface (GUI) of a PHOCI-based communication application. The application presents the user with a simulated video image superimposed with communication data sources. The user can select a data source and view the information received from the selected data source.

The GUI of the mock application was developed to provide a platform for developing and evaluating algorithms that are critical to the functionality of the PHOCI technology. In this sense, the GUI is a front-end to a behavioral simulation of a PHOCI-based communication system.

The application provides a framework where the following attributes and algorithms of the system can be effectively evaluated in a simulated environment:

- *Data Sources*: Laser data sources can be created that emit virtual signals onto a simulated sensor in order to evaluate and verify the system's ability to receive and process known communication sequences.
- *Disturbance Sources*: Each laser data source is also associated with a disturbance source that simulates the spread of the laser signal as it travels through the environment. The disturbance source also provides a means of generating noise and physical disturbances such as obstructions or atmospheric effects.
- *Image Sources*: Simulated environmental images can be created that emit either still images or video onto the simulated sensor.
- *Motion Sources*: Both data sources and image sources can be tied to a motion source that modifies the spatial location of the source as a function of time. For data sources this simulates the movement of the data source in the field of view of the sensor. For image sources, this simulates the movement of the sensor itself.
- *Virtual Sensor*: A model of the PHOCI sensor and its internal components was developed that allows different sensor designs to be evaluated in the simulation environment.
- *Data Channel Manager*: As previously described in this section the data channel manager plays a crucial role in managing the resources of the PHOCI sensor. The simulation framework allows various implementations of the data channel manager to be quickly evaluated within the context of a known simulation environment. The simulations performed during the Phase I effort highlighted the importance of this component in developing a useful system based on a data-integrated image sensor.
- *Host Data Link:* The data structures that would be transmitted across a PHOCI host data link were also simulated using the mock application. The virtual PHOCI sensor and virtual PHOCI board communicate with the mock application GUI through a message queue. By isolating the host application from the details of the PHOCI board, it was much simpler to determine the information that would be required by a real-world PHOCI application and the costs of transmitting that information across the host data link.

6. Commercialization

The commercial feasibility of the PHOCI data-integrated sensor was established during the Phase I effort. Our research and communications with individuals in the commercial sector revealed a number of opportunities commercializing the technology. The sensor chip itself is a novel application of CMOS imaging technology, and it will be the first sensor on the market to combine the capability of high speed data transfer with video acquisition.

During the Phase I we developed four possible strategies for commercializing the PHOCI technology that are summarized in the following sections.

Product 1: Production and Sales of PHOCI sensors and support chips
Product 2: Production and Sales of PHOCI boards
Product 3: Sales of PHOCI IP cores
Product 4: Related Engineering services

Product 1: Production and Sales of PHOCI sensors and support chips

Perhaps the most obvious avenue of commercialization for this project is production and sale of PHOCI sensors and support chips. According to "Semiconductor Business News", the market for CMOS video sensors was $367M in 2001 and is projected to grow to $1B by 2005. This will put CMOS imagers at approximately 47% of the video sensor market, with most of the remaining going to CCD technologies. Data-Integrated sensors are a new technology that will come as the direct result of this project, so market data does not yet exist. If 5% of current applications will benefit from data integration, the market for data-integrated sensors would have been $18M in 2001 and will be rising to $50M by 2005. Note that this technology will enable entirely new categories of products and therefore projections could be vastly understated.

Potential markets for the PHOCI sensor and support chips include:

- Free Space Optical Networking Products
- Video Projection Systems
- Emerging Product Areas

Free Space Optical Networking Products

Companies such as Terabeam, Lucent Technologies, and Sorrento Networks currently have products on the market to enable communication at high data rates (in the gigabit per second range) in free space. These products are relatively new, but have shown great promise in several key areas:

- In dense urban areas where the cost of installing new cables underground is prohibitive.
- In situations where the need for communication capability arises suddenly or is needed temporarily. The New York Times recently reported that in the aftermath of the September 11th attacks in New York City, free space optical networking became an area of particular interest to the companies located in the affected areas as a way to quickly restore critical infrastructures that were destroyed.
- In situations where data security, electromagnetic interference, or other concerns prohibit RF wireless communications.

However, current technologies have several obstacles to overcome. In order to achieve the highest communication speeds possible, detectors in current receivers utilize a one-pixel sensor that is very fast, but provides the transmitter with an extremely small target. Relative movement between the transmitter and receiver is typically unavoidable, due to factors such as wind, building sway, etc.

The laser tracking capability of PHOCI data-integrated video sensors is a perfect match for existing high-speed free space optical communications systems. The PHOCI sensor would augment the high-speed receiver, allowing it to track the transmitter as it moves relative to the receiver. One can imagine that PHOCI sensors could be installed at each end of such a high-speed link, to provide two-way communication between the transmitter and receiver. This communication channel would be utilized for control signals between the transmitter and receiver to help keep them aligned.

Current commercial applications of free space optical networking have been focused on point-to-point communication between buildings and other areas where installing wiring is difficult or impossible. Other advantages that optical networking can have over traditional wireless networking (e.g. 802.11b) include:

- Bandwidth can scale much more easily than it can with RF networking. Simply adding transmitters and receivers will increase bandwidth. This approach does not work with RF networking products as the RF band becomes saturated as more traffic is added to it.

- No sensitivity to RF interference. In some environments, such as on factory floors, large motors and transformers emit RF interference degrading the communication capabilities of wireless technologies such as 802.11b.
- No RF emissions. In some environments RF interference is unacceptable. Examples of these environments include some types of manufacturing facilities, hospitals, and in places where information security is critical.
- Simultaneous video capture. Some applications that would benefit from wireless networking could also benefit from the video capture capabilities that the wireless receiver would have due to its nature. An example of this could be in a hospital emergency room. Telemetry data from heart monitors, drug pumps, IV bags, etc could be handled through free space optical networking and video could be stored as treatments were performed. This could help hospitals protect themselves from malpractice suits.

Of the application areas presented, our Phase I efforts concentrated mainly on manufacturers and applications on the factory floor. During the Phase I we received letters of support from manufacturers expressing interest in free-space wireless networking in the context of networking the factory floor. In addition, there were several cases where the companies verbally indicated their interest in the product, but because of confidentiality or liability reasons, they are unwilling to submit letters to accompany this proposal.

These letters were received in direct response to discussions with individuals working in the manufacturing and/or production departments of these companies. One of the contacts at Whirlpool Corporation mentioned that the idea of wireless networking on the factory floor had a nice fit with an emerging area called "cellular" (also "lean" or "agile") manufacturing. This is a technique where the factory floor is divided into "cells" of production. Each cell is designed to be highly reconfigurable and the people within the cell act as a team. Because of the need to reconfigure equipment frequently, traditional wired network is not a good fit for this type of production, and traditional wireless solutions have the shortcomings previously mentioned.

Video Projection Products

According to Pacific Media Associates, video projection units currently have estimated sales of $2.1B. Furthermore, the referenced report states that sales flattened in 2001. This is not surprising since the opportunity for innovation in this field is limited. We feel that data-integrated sensor technology can provide a significant improvement to the current crop of video projectors.

Specifically video projectors can be augmented with a video sensor that can read data broadcast by a special laser pointer that will act like a mouse. This will allow control of the computer running the projector from anywhere within line of site of the screen. In addition, the transmitter could have any number of buttons on it to allow a large variety of messages to be sent to the projector. Lastly, multiple transmitters can be used with a single screen to allow multiple users to interact on a single screen. Imagine a collaborative video whiteboard where each member of the team can make annotations with their own transmitter. The software could attribute these annotations to the proper user, turn on and off certain annotations, etc. There are many possibilities for this type of product, and there are many vendors of these products to approach.

Another benefit of integrating PHOCI technology into video projection products is the capability of capturing video from presentations. The projector itself would have the capability of capturing audio and video from the presentation, which could be stored on the computer running the presentation. This video could be used in a variety of ways including archival storage and live web broadcasting of presentations, and alleviates the need for a separate piece of hardware to enable these capabilities.

Emerging Product Areas

The last category we call "emerging products". These areas are less clear in nature (and higher risk) but overall could be the largest segment of the data-integrated sensor market. Products in this category could be applications of a nature that have never been available. For instance, "augmented reality" products that allow a person to receive data from the environment as they walk around. Imagine walking down the street and having stores communicating information to you about the products, specials,

menus, etc available to you. Perhaps this information would come across a PDA type device, or perhaps it would be overlaid into the user's field of view by lasers on their retinas.

A less exotic application could be cars with data-integrated sensors built into them. A car equipped with such a sensor could communicate with the other cars in the area, perhaps transmitting speed and directional information. This could be used as a basis for a collision avoidance system. The video capability of the sensor could be used to provide a video log that could be valuable in analyzing crashes. In addition to car-to-car data transmission, there could be transmitters and receivers along the highway system providing a wealth of information to the drivers on the highway. For instance, route information could be fed into the car's computer, and then based on real-time traffic conditions (provided via laser from the side of the highway) "optimal" routing could be provided to the driver. Alternatively, queries could be made to the environment as to where the closest Mexican restaurant is located in the area. There are many possibilities for this type of application.

Product 2: Production and Sales of PHOCI boards

While some customers will be interested in integrating our technology through the acquisition and integration of sensor and support chips, others will be looking for a more complete solution. A key part of our plans include developing a reference implementation for proof-of-concept and demonstration purposes. As discussed previously, this implementation will be a "plug and play" solution with support for COTS computing platforms. Given sufficient interest we will consider the production and sales of this reference implementation as a product.

Product 3: Sales of PHOCI IP cores

A natural extension that can be made to the sales of integrated circuits is the sale of their IP cores. IP cores consist of the source files that compose the design. (Often they are obfuscated in some way to make copying the design more difficult.) Making cores available makes it possible for others to utilize PHOCI technology in their own integrated solutions.

One advantage of selling cores as opposed to selling fabricated chips is that distribution is much simpler for source files than for a physical product; it can happen over the Internet or through burning compact disks in a low volume scenario. Also, the pricing for IP cores is generally *much* higher than for individual chips because the manufacturer can use the core to produce virtually limitless numbers of their own chips. The biggest hurdles in this area are negotiating the legal challenges of intellectual property rights, as well as pricing the product correctly within the market.

Product 4: Engineering services

We plan to offer engineering services in order to achieve the level of service that our customers will require. Field application engineers will be available on an hourly (plus expenses) basis. For large and new customers, we will have to decide if there is sufficient ROI for offering such services at no charge.

7. Conclusion

Overall, the PHOCI Phase I effort was a great success. The initial concept for the technology presented in the Phase I proposal was refined to produce a proof-of-concept system design that addresses the technical objectives outlined in the original proposal. Based on this design, a working implementation of the proof-of-concept design is expected in mid-August 2002. The results of the design and simulation performed during the bulk of the Phase I effort certainly established the technical feasibility of the technology, and it is expected that the results of the proof-of-concept implementation will confirm these results. The market research and response from commercial contacts demonstrated not only a potential market for the technology, but also a definite interest in applying the technology to both ad hoc and permanent networks in harsh environments.