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Principal Investigator : Kerry Vahala

BACKGROUND

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OVERVIEW

Ultra-fast byte-wide data transmission between high-speed computers can be achieved using a spectral data bus where each bit is assigned a different wavelength and data is transmitted on one optical fiber [1]. All-optical signal processing for header recognition, routing, error correction or encryption can improve the throughput of a cluster of linked computers. All-optical logic operations on PolSK (Polarization Shift Key) coded data using ND-FWM (Non-degenerate four-wave mixing) in SOAs (Semiconductor Optical Amplifiers) which exploit the polarization properties of the non-linearity have been proposed and demonstrated [2-4]. Furthermore, FWM on PolSK coded bits can be used to construct higher-level logic elements to implement truth tables involving several WDM (Wavelength Division Multiplexed) data bits without resorting to elemental Boolean functions such as NAND/NOR.

There are interesting front-end signal processing possibilities associated with spectral bus transmission including byte-wide error correction and detection [5] and, possibly, improved security. Front-end here means a device that is situated between the bus and whatever the bus is linked to (presumably a computer). In order to enable detection and correction of errors in transmission on an optical fiber, there must be an addition of parity-bits. Currently, this encoding and decoding is performed in the electrical domain, before transmission and after detection, respectively. However, in a simple fiber-optic databus, coding and decoding for error correction can be implemented using such all-optical logic gates. This is schematically shown in Figure 1.

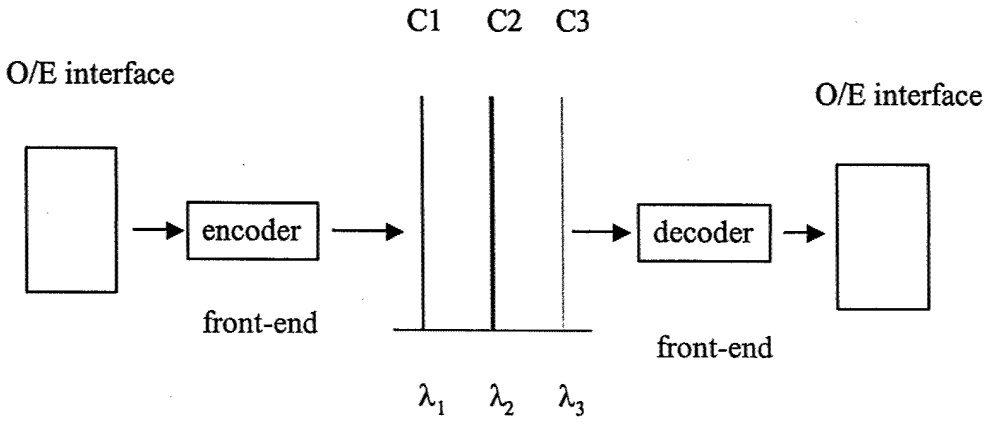


Figure 1 : All-optical logic circuits for on-the-fly signal processing on a spectral bus. A three-bit byte is shown here.

The error correcting code we have used is the simplest for single-error correction, the (3,1) Hamming Code [6] which uses one data bit and two parity bits. The transmitted word is [C1,C2,C3] = [0,0,0] or [1,1,1]. In this case each bit, Ci, corresponds to a different wavelength, λ_i (i = 1,2,3). If an error occurs on any bit, an undesired word is received. With the EC-receiver, the error is detected and corrected for.

This research project involved designing and developing all-optical logic circuits for coding and decoding using the (3,1) Hamming Code. The performance of the circuits was tested at high bit-rates. Error-free detection with BER < 10^{-9} was obtained even when the transmitted 3-bit word had random errors on one of the bits. The successful operation of these circuits proved the feasibility of the scheme to implement all-optical logic using the selection rules of multi-photon scattering processes.

PRINCIPLE OF OPERATION

The all-optical logic circuit that performs on-the-fly error correction on the (3,1) Hamming Code is now described. The binary word is PolSK modulated, where the binary states "1" and "0" are represented by orthogonal linear states of polarization (SOP) along the fast and slow axes of a Polarization Maintaining (PM) fiber. This scheme enables implementation of the NOT function for binary data by the use of passive elements such as a half-wave plate.

Byte-wide transmission is achieved by assigning each bit to a separate wavelength channel, thus the optical fiber acts as a parallel data-bus. Also note that since the coding and decoding is accomplished in a byte-wide fashion the redundancy added by the code does not slow down the transmission rate. For the purpose of discussion, the 3-bit spectral word is assigned channels C1, C2 and C3. The logic operation realized in the error-correcting circuit is

$$EC = (C1 \cap C2) \cup (C2 \cap C3) \cup (C3 \cap C1) \qquad (1)$$

where "$\cap$" denotes the logical AND, "$\cup$" denotes the logical OR function and EC is the error-corrected information.

The co-propagating electric field E_k, generated by the FWM process is given by

$$E_k(\omega_{EC}=\omega_{C1}+\omega_{C2}-\omega_{C3}) \propto \chi^{(3)}_{klmn} E_l(\omega_{C1})E_m(\omega_{C2})E_n^*(\omega_{C3}) \qquad (2)$$

where ω_i, i = EC, C1, C2 and C3, is the angular frequency of the optical wave and $(^*)$ denotes complex conjugation. $\chi^{(3)}_{klmn}$ is the third-order nonlinear susceptibility, which is a tensor of rank four and is dependent on the SOP of the electric fields of C1, C2 and C3. The geometry of the FWM process considered in this work is such that the three input waves are launched into a single transverse mode waveguide (here a semiconductor optical amplifier) along the same direction of propagation. The extracted product-wave hence propagates along the direction of incidence. The wavelength channels used in the experiment along with the FWM signals generated are shown in Figure 2 below.

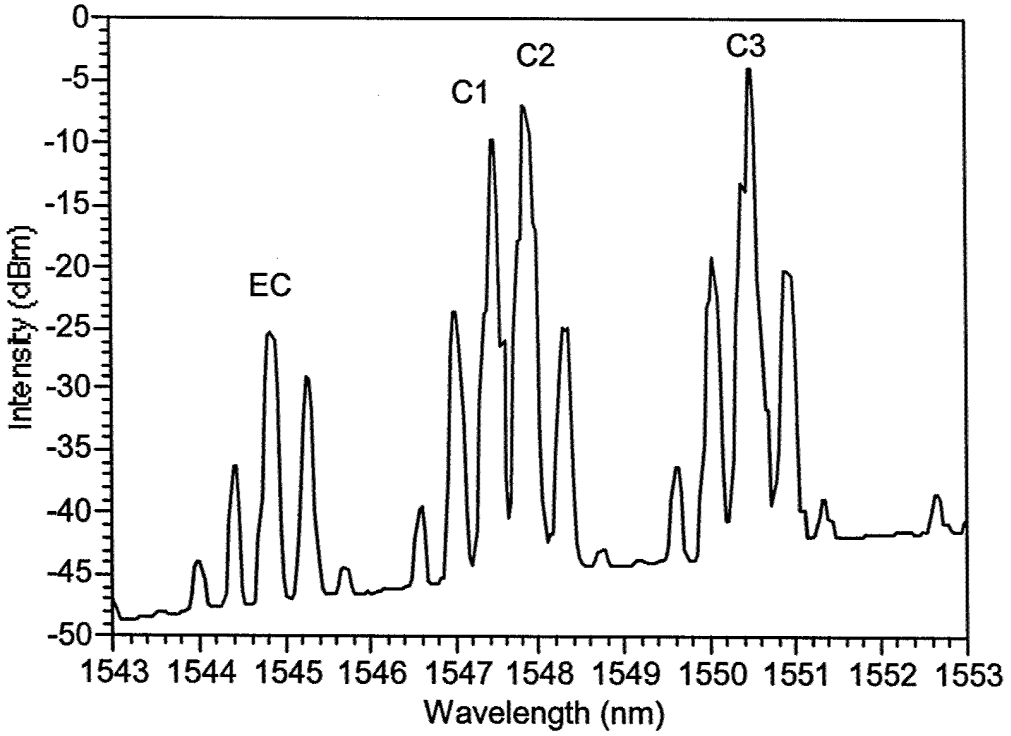


Figure 2 : Spectrum at the output of the SOA in the presence of three wavelength channels

In a bulk semiconductor medium, the polarization dependence of the mixing product at ω_{EC} is given by

$$\hat{e}_{EC} \propto \left[\left(\hat{e}_{C1}\cdot\hat{e}^*_{C3}\right)\hat{e}_{C2} + \left(\hat{e}_{C2}\cdot\hat{e}^*_{C3}\right)\hat{e}_{C1}\right] \qquad (3)$$

where $\hat{e}_i$, i = EC, C1, C2 and C3, is the unit vector along the direction of the electric field. The terms in Equation 3 can be physically interpretted as the FWM signal at EC being generated as follows - C3 forms dynamic gain and index gratings with C1 (or C2). Then, C2 (or C1) scatters off this grating to generate two FWM side bands, one of them being at ω_{EC} [7]. These processes are diagramatically represented in Figure 3.

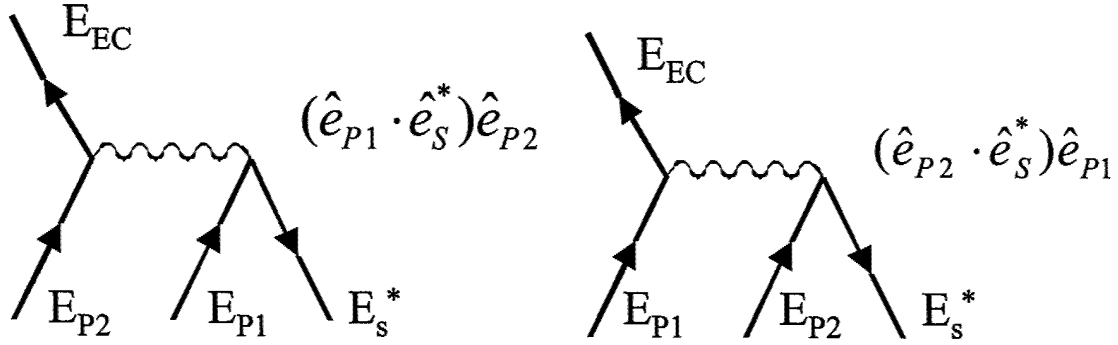


Figure 3 : Diagrammatic representation of the non-degenerate FWM process

In the semiconductor optical amplifier (SOA), the unit vector $\hat{e}_i$, representing each binary state, is aligned along the TE or TM direction of the waveguide structure. The EC signal is generated in one of the following ways

- When all three input electric vectors are parallel (corresponding to identical bits on each channel, i.e. no errors are present), the electric field of the mixing signal at ω_{EC} is parallel to the three inputs. This is used, in turn, to generate an output when no error correction is necessary.
- When one of the electric fields is orthogonal to the other two (corresponding to an error on that bit), a product wave at ω_{EC} is generated only when C1 and C2 are orthogonal. In this case C3 creates a grating with either C1 or C2 (the one whose polarization is parallel to C3), which scatters energy off the third wavelength to generate a FWM signal at ω_{EC} that is orthogonal to C3. This property is utilized to correct for errors.

The error-correcting circuit requires at least three SOAs (only two are required if retaining the PolSK format on the EC channel is not important) to generate the proper FWM signal in all possible cases. The circuit is designed in such a way that the FWM product at ω_{EC} occurs in only one SOA at a time. This is done in order to avoid interference of the desired FWM signal with additional spurious signals that would degrade the performance of the circuit. This is accomplished by adding a pre-processing element before each SOA as shown in Figure 4. In the preprocessing element, one of the sub-elements is a polarizer with its transmission axis aligned to either the fast or slow axis of the PM fiber. The other element is a wavelength selective half-wave plate which will be referred to as the birefringent element (BE). It acts as a half-wave plate for C3 and a full-wave plate for C1 and C2. The result is that the SOP of C3 gets rotated by 90 degrees (and thus inverts the binary state on C3) while that of C1 and C2 remain almost unchanged.

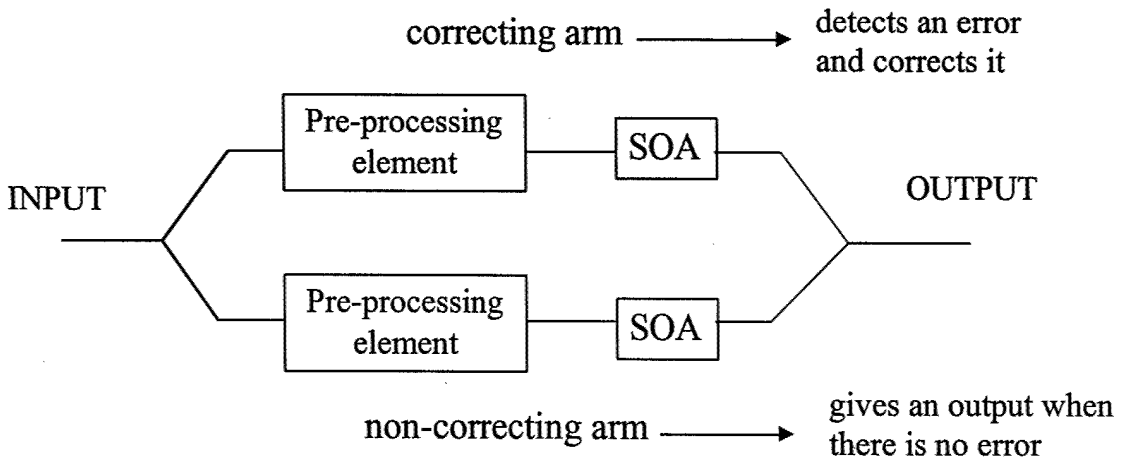


Figure 4 : Schematic diagram of the EC circuit

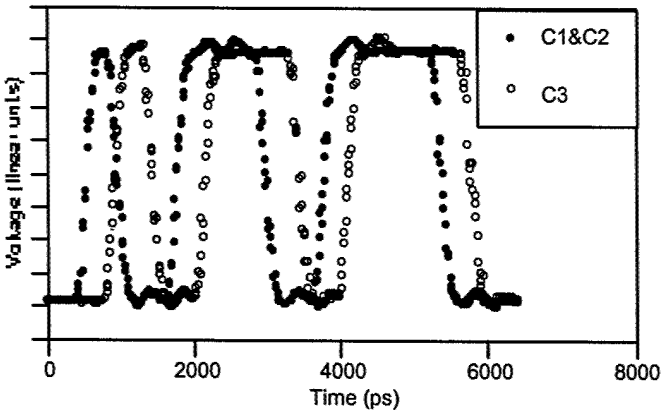
The output of the circuit for each possible case is as follows:

- In the absence of any errors, C1, C2 and C3 are parallel at the input and mixing at ω_{EC} occurs in the SOA after the polarizer (SOA 1) whose axis coincides with C1, C2 and C3. The mixing signal is parallel to the input bits and has the same binary state as the input bits. Thus the output is generated without error correction and it is for this reason that this arm is called the "non-correcting" arm. (It should be noted that a polarizer changes PolSK modulation to ASK modulation. Hence if PolSK modulation is to be preserved, two such non-correcting arms are required, each with a polarizer as a pre-processing element aligned to the slow and fast axes of the PM fiber respectively.) Furthermore, when C1, C2 and C3 (all being parallel) pass through the BE which is the pre-processing element in the other arm, C3 becomes orthogonal to C1 and C2. In this case, no mixing at ω_{EC} takes place in the SOA after the BE (SOA 2) in accordance with Equation 3.
- In the presence of an error, C1, C2 and C3 will not all be parallel and thus will not pass through the polarizer. Hence no mixing will occur in SOA 1. There are two possible cases. When the error is on C3, it is orthogonal to both C1 and C2. After passing through the BE, C3 will become parallel to C1 and C2 and the mixing signal in SOA 2 will have the same binary state as C1 and C2. Thus an error on C3 will be corrected. When the error is on either C1 or C2, C3 will align with the incorrect bit (since it gets inverted by the BE) and will form a grating which will scatter off the correct bit to give a mixing signal parallel to the correct bit. Thus an error corrected signal is generated and hence the arm with the BE as the pre-processing element is called the "correcting arm".

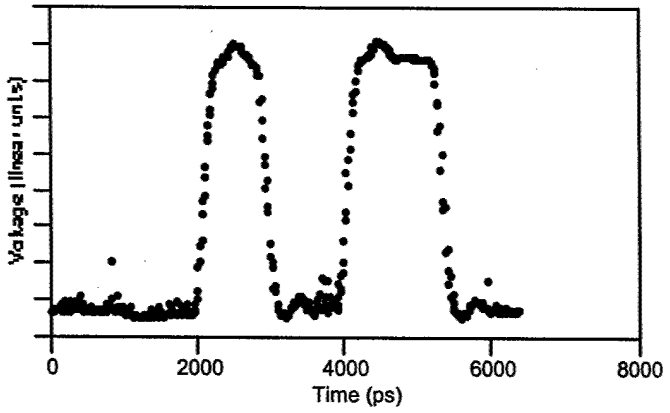
RESULTS

Figure 5(a) shows a 16-bit pattern [1001110011110000] at 2.5 Gbit/s on each channel. The variable time delay is adjusted so that there is a one bit delay on C3 relative to C1

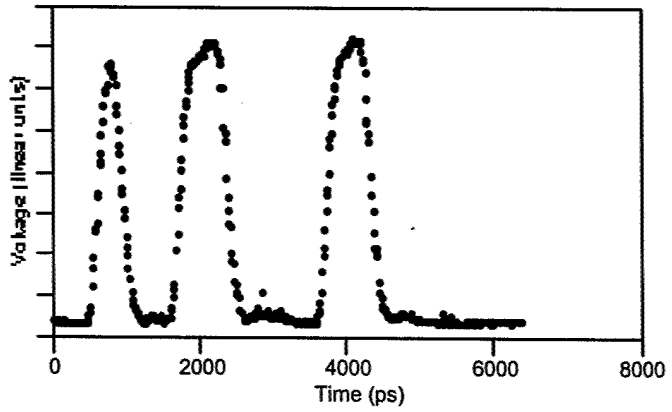
and C2. Thus C3 is the channel which has occasional errors. The resultant patterns on ω_{EC}, which are obtained from the non-correcting and correcting arm separately, are shown in Figure 5(b) and 5(c) respectively. Figure 5(d) shows the pattern on ω_{EC} after both arms have been combined and is identical to the pattern on C1 and C2. This shows that the data stream with errors was corrected.



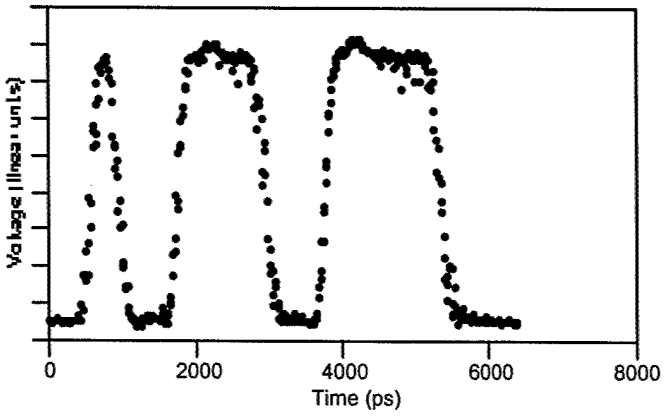
(a)



(b)



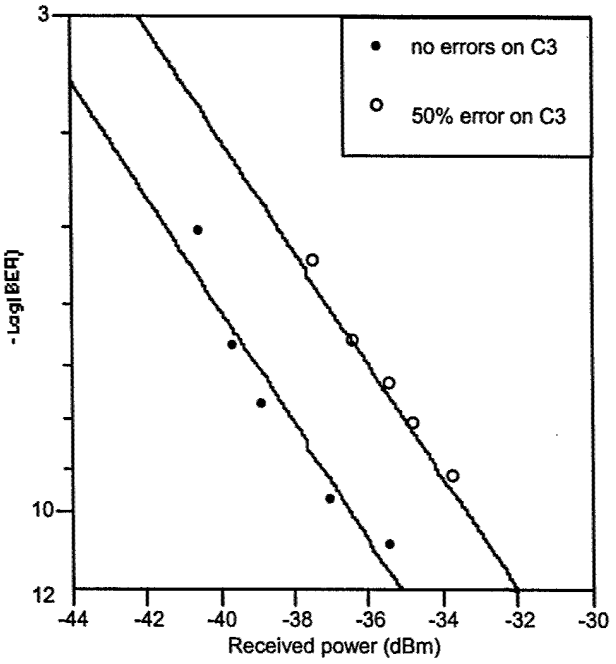
(c)



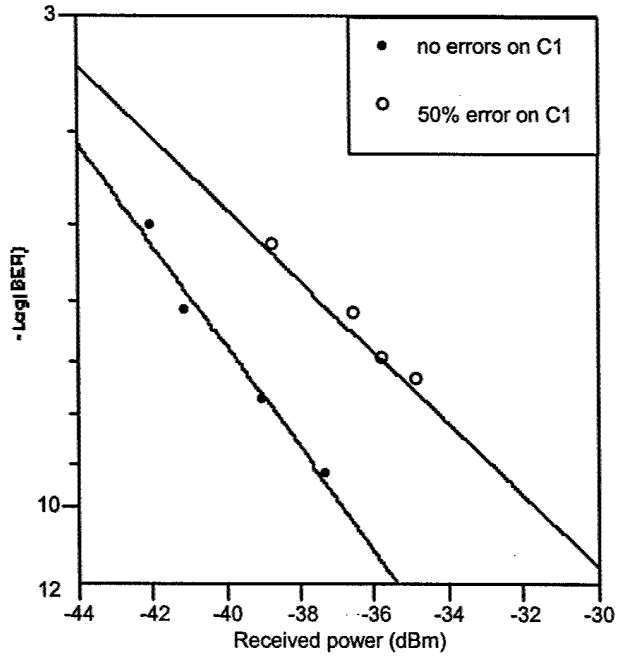
(d)

Figure 5 : Oscilloscope traces of (a) 16-bit patterns on channels C1, C2 and C3 at 2.5 Gbit/s, (b) EC output from the non-correcting arm, (c) EC output from the correcting arm and (d) EC output from both arms combined.

We further demonstrate the dynamic operation of this circuit by modulating C1, C2 and C3 with a pseudo random bit stream (2^7-1 PRBS), with a one bit time delay on C3 relative to C1 and C2. In this case the binary state on C3 is complementary to the state on C1 and C2 approximately 50 percent of the time (i.e., error rate of 0.5). Figure 6(a) shows the Bit Error Rate (BER) versus received power (in 0.5 nm Resolution Bandwidth) of the EC channel for this case. This is compared to the case when there is no errors on C3 relative to C1 and C2. Detection with a low BER of $<10^{-9}$ is demonstrated despite the high rate of errors on the input word (0.5). Similar results are obtained by modulating C1, C2 and C3 with PRBS with a one bit delay on C1 relative to C3 and C2, in which case the binary state on C1 is complementary to that on C2 and C3 approximately 50 percent of the time. The BER for this is shown in Figure 6(b). The slight degradation after error correction in Figure 6(b) compared to Figure 6(a) can be explained by the lowering of FWM efficiency in the correcting arm when C1 and C2 are orthogonal compared to when C1 and C2 are parallel, as determined by Equation 3.



(a)



(b)

Figure 6 : BER versus received power (in 0.5 nm Resolution Bandwidth) at 2.5 Gbit/s for (a) random errors on C3 and (b) random errors on C1.

The operation of the logic circuit was further tested when the information on C3 is severely distorted, so that a BER no better than 30 percent could be achieved on C3. This is achieved by changing the DC-bias of the MZ modulator. Thus the information on C3 is ambiguous in that there are no clearly defined binary states on it. PRBS data on C1 and C2 was detected to be error-free upon transmission through the circuit. Figure 7 shows the BER versus received power on the EC signal for this case. Once again a low BER of $<10^{-9}$ on the mixing signal for ambiguous data on C3 and error-free data on C1 and C2 is demonstrated. This shows that error correction on certain ill-defined states is also possible.

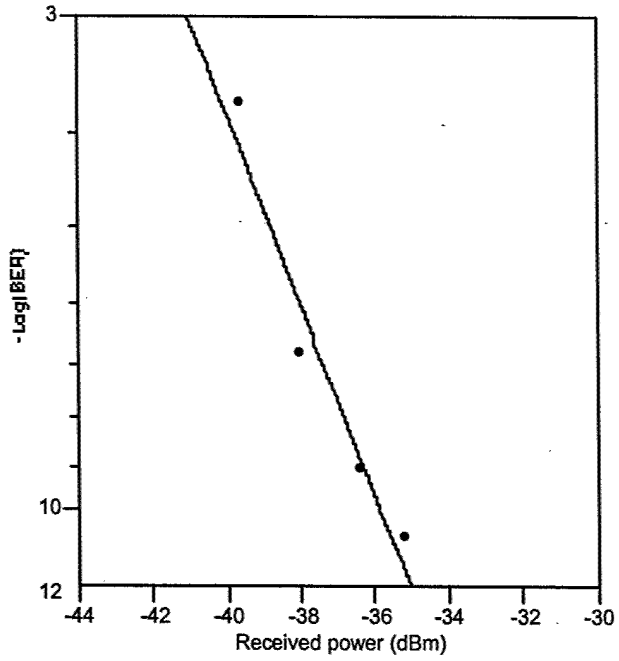


Figure 7 : BER versus received power (in 0.5 nm Resolution Bandwidth) at 2.5 Gbit/s for error correction on ill-defined states with 30% errors on C3.

CONCLUSIONS

We have shown that FWM on PolSK coded bits can be used to construct certain higher-level logic elements without resorting to the standard 2-input gates. Taking the simple example of the (3,1) Hamming code, we have demonstrated on-the-fly error correction on severely distorted data. The data is recovered with a BER $<10^{-9}$. To the best of our knowledge, this is the first demonstration of a fiber-optic logic circuit that performs signal processing on more than two input channels simultaneously. The bit rate of the experiment was limited to 2.5 Gbit/s by the bandwidth of the modulators. Since FWM is an ultra-fast nonlinearity, the error correcting circuit can be made to perform at much higher bit rates.

[1] G. Jeong and J.W. Goodman, "Long-distance parallel data link using WDM transmission with bit-skew compensation", J. Lightwave Technol., **14**, 655-660 (1996).

[2] A. Bhardwaj, P.O. Hedekvist, H. Andersson and K.J. Vahala, "All optical front end error correction on a spectral data bus", presented at the Conf. Lasers and Electro-Optics, Paper CWI5, May 2000.

[3] P.O. Hedekvist, A. Bhardwaj, K.J. Vahala and H. Andersson, "Advanced all-optical logic gates on a spectral bus", submitted to Appl. Opt.

[4] A. Bhardwaj, P.O. Hedekvist and K.J. Vahala, "All-optical logic circuits based on polarization properties of non-degenerate Four-Wave Mixing", submitted to J. Opt. Soc. Am. B.

[5] S.K. Shao and M.S. Kao, "WDM coding for high-capacity lightwave systems", J. Lightwave Technol., **12**, 137-148 (1994).

[6] R.W. Hamming, "Error detecting and error correcting codes", Bell Syst. Tech. J., **29**, 147-160 (1960).

[7] R. Paiella, G. Hunziker, U. Koren and K.J. Vahala, "Polarization-dependent optical nonlinearities of multiquantum-well laser amplifiers studied by four-wave mixing", J. Sel. Top. Quant. Electron., **3**, 529-540 (1997).