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MICROELECTROMECHANICAL (MEMS)-BASED DATA STORAGE

Hewlett Packard Laboratory

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13. ABSTRACT ***(Maximum 200 Words)***

This project developed and demonstrated design and fabrication technologies required to enable mass production of MEMS micromovers and electrostatic motors required to actuate these structures, including suspension systems of unprecedented high aspect ration by Hewlett Packard. Single and multiple level electrical interconnect fabrication techniques were developed and refined by Cornell University. A technique to fabricate large arrays of field emission tips was developed by U.C. Davis.

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PROGRAM OVERVIEW

This final report documents the major accomplishments of the MBDS contract through its end date in February of 2002. The technical progress is reported by each of the three participants (Hewlett Packard Laboratory, Cornell University, and University of California at Davis) in separate sections below.

A. HEWLETT PACKARD

HIGH ASPECT RATIO SUSPENSION DEVELOPMENT

PETER HARTWELL, UIJA YOON
HEWLETT PACKARD LABORATORIES

A.1. INTRODUCTION – MICROMOVERS AND SURFACE DRIVES

The MBDS data storage medium will be a flexurally suspended silicon plate that is scanned beneath the read/write field emission tips. This media plate must have a wide in-plane scanning range of +/- 25 μm, while maintaining a media-tip separation which is stable to within +/- 50 nm. To meet these requirements, the out-of-plane, z-axis stiffness of the flexure suspension must be at least 1000 times greater than both the x and y-axis suspension stiffnesses. From simple beam theory, such a stiffness ratio demands that the suspension have a height to width aspect ratio of at least 32:1.

The project is devoted to developing a fabrication process for these high aspect-ratio suspension structures. In addition, the static and dynamic response of fabricated suspension structures will be examined, allowing optimization of the suspension design. To allow a margin of safety, a target aspect ratio of 40:1 has been established. We have selected a bipolar electrostatic surface motor for the actuation of the micromover. This motor has the advantages of large travel ranges for a given operating voltage and allows data and motor to occupy the same area of the chip.

The HP bipolar electrostatic motor was first presented by Storrs Hoen at the 1997 International Conference on Solid-State Sensors and Actuators in Chicago in June, 1997. We will briefly describe the motor here for completeness. The bipolar electrostatic motor is a series of long, finger-like electrodes made on the surface of the micromover (rotor). The micromover wafer is mated with a second wafer (stator) with a similar electrode pattern. A gap of a few microns is maintained between the bonded wafers. The aligned electrode pairs form the electrostatic surface actuator. Electrodes are energized with one of two different voltages, hence the term bipolar. The rotor and stator electrodes are initially energized in a simple alternating pattern. Electric fields between the electrode pairs create a potential energy well causing the rotor to lock into the position of minimum inplane force. The equilibrium position can be changed by changing the electrode bias pattern on the stator. As shown in Figure A1, changing a single electrode from one bias to the other causes a shift in equilibrium position corresponding to one "step".

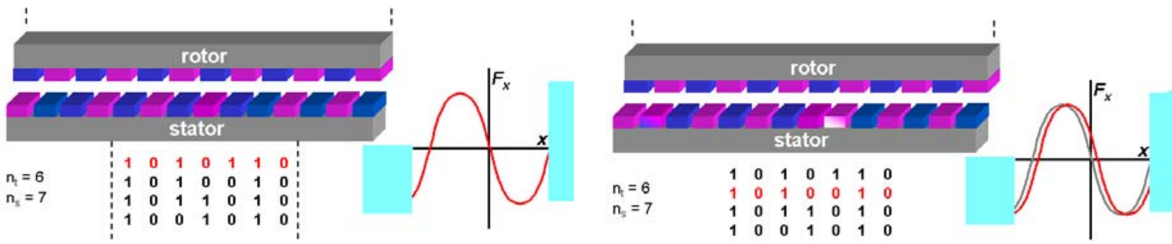


Figure A1. Bipolar motor electrode patterns. Left shows state 1, right shows state 2. One electrode has changed potential causing a shift of the rotor by one "step" to the right.

The size of a step can be calculated from the following formula:

$$d = \frac{P_r}{n_s}$$

where P_r = the pitch of the rotor electrodes and n_s = the number of stator electrodes

For example, with 7 stator electrodes in a group and a rotor electrode pitch of 3.5 um, the step size would be 0.5 um. Each progressive switch of one electrode advances the micromover 0.5 um. In addition to the inplane forces caused by the electric fields between electrodes, a large out of plane force component is also generated. The out of plane force acts is an attraction between the rotor and stator and is also termed pull down force. The pull down force is another reason a high stiffness ration is need for the micromover device.

The bias voltages on the electrodes are generally selected to be ground and some positive bias referred to as the drive voltage. The drive voltage is carefully selected to provide enough inplane force for desired travel distance without causing pull down. The higher the stiffness ratio of the flexural suspension, the larger drive voltage can be used.

This report will cover the development of the micromover platform and suspension suitable for using in the MDBS device with an integrated bipolar surface drive. The report documents short loops undertaken to develop process steps needed for the most challenging parts of fabrication. The fabrication process for the flexures and improvements made to the process, and process yield are then covered. Then, the development of testing apparatus to measure the parameters of the fabricated suspensions and evaluations of the devices relative to the project goals. Finally we will summarize the successes of this project and offer some insight into the future.

A.2. PROCESS SHORT LOOPS

A.2.1. Flexure etching

A process for the deep-reactive ion etching (DRIE) of high aspect ratio silicon structures has been developed. A typical suspended test structure is illustrated in Figure A2. In order to minimize the processing complexity, the surface drive electrodes will not be fabricated in this initial test process. Instead, a thin layer of permalloy will be deposited onto the media plate, allowing magnetic actuation of the flexures. This permalloy will not be included in the final fabrication process for the surface drive actuator.

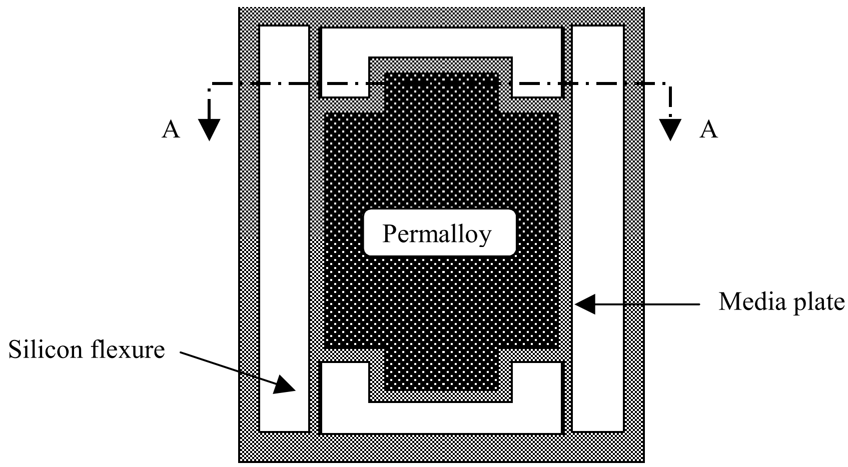


Figure A2: Typical test structure layout.

The simplified fabrication process flow chart is shown in Figure A3. The starting substrate is a silicon on insulator (SOI) wafer consisting of a 100 μm silicon device layer bonded to a 400 μm silicon handle wafer via a 1 μm buried SiO_2 (oxide) layer (Figure A3a). Initially, the wafer is coated with a 200 nm film of low stress silicon nitride (LSN) which will serve as a protective mask during subsequent KOH etching. The front and back sides of the wafer are then photolithographically patterned. The backside pattern defines a region where the handle wafer silicon will be removed from beneath each structure. The front side pattern consists of alignment marks that will be used to align subsequent layers to these backside cavities (Figure A3b). Next, a permalloy seed layer is sputtered onto the front of the wafer. Photoresist is deposited and patterned, and a 1 μm permalloy layer is selectively electroplated onto the seed layer. After stripping the photoresist, the seed layer is removed via ion milling (Figure A3c). The device layer silicon is then etched by DRIE using a photoresist mask (Figure A3d). The front side of the SOI wafer is bonded to a wax-coated carrier wafer to protect the etched structures from KOH etching and dicing (Figure A3e). The wafer is then immersed in KOH, etching deep cavities into the handle wafer (Figure A3). The SOI wafer is diced, and heated acetone is used to free the dice from the carrier wafer. Finally, a 1-minute soak in concentrated HF is used to remove the oxide membrane, freeing the suspended test structure (Figure A3g). The released test structures may then be actuated using an external magnet to test the static and dynamic behavior of each flexure suspension.

An SEM microphotograph of a typical released structure is shown in Figure A4, while cross-sectional views of the deep-etched flexures are illustrated in Figure A5.

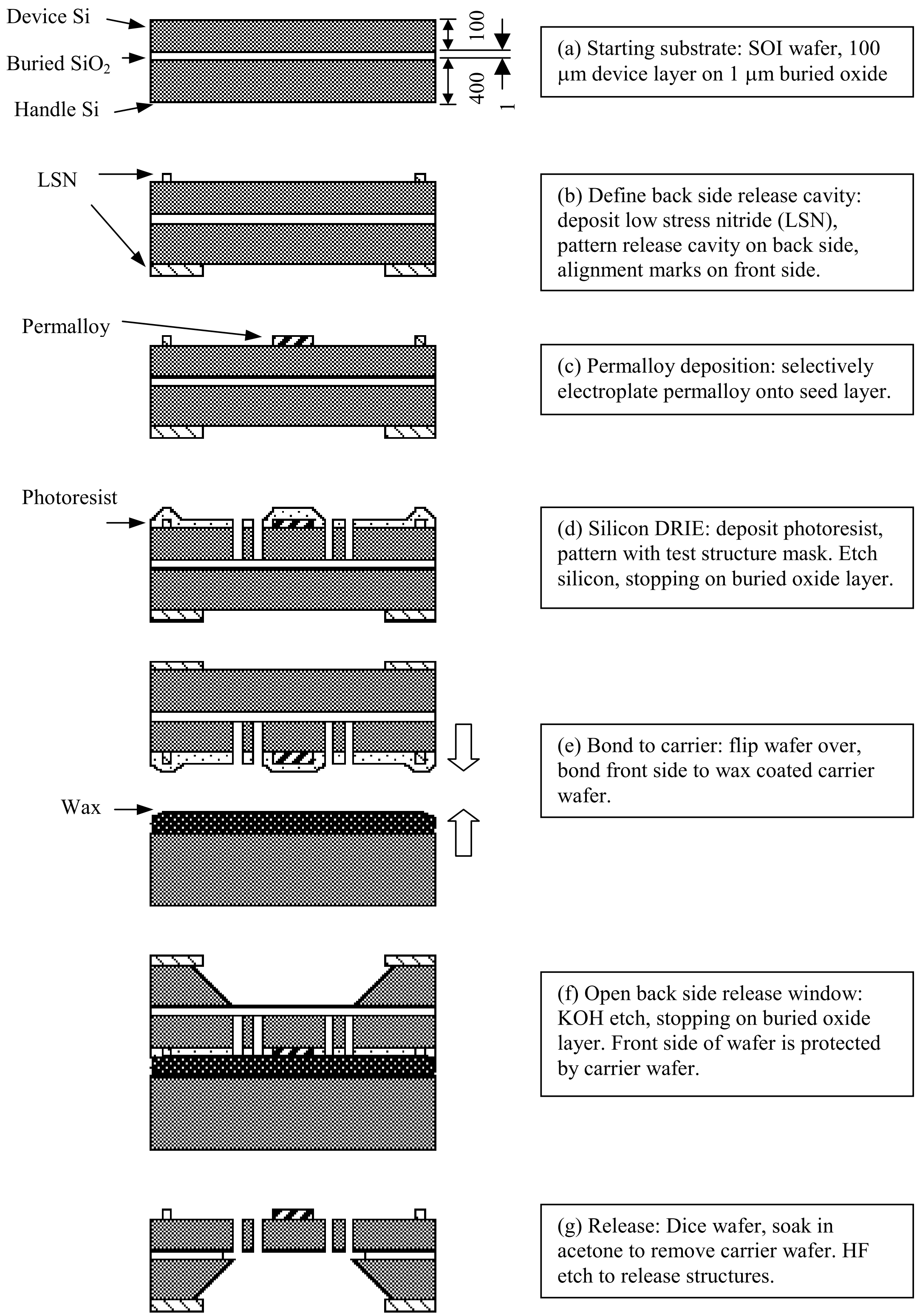


Figure A3: SOI DRIE process flow chart

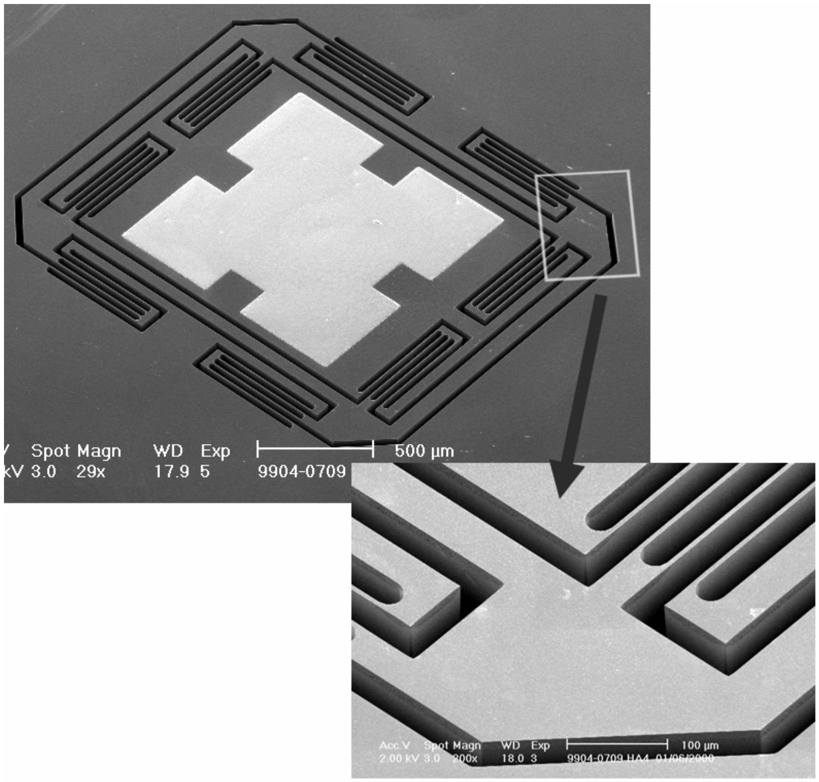


Figure A4 SEM photomicrograph of a completed NiFe coated micromover.

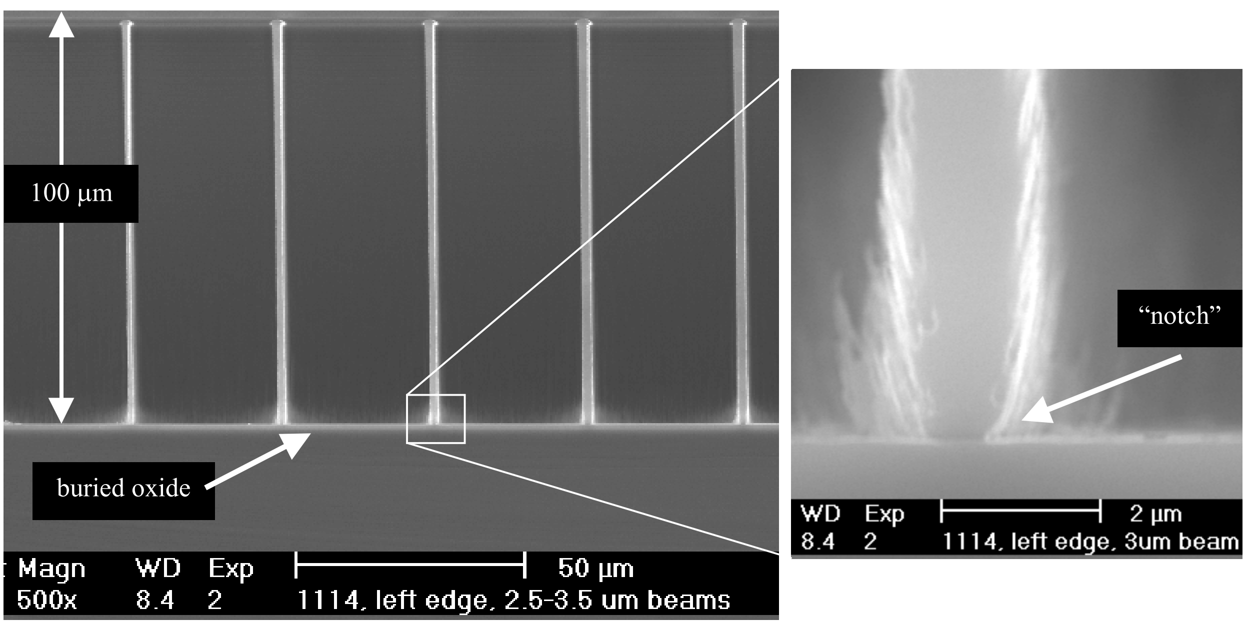


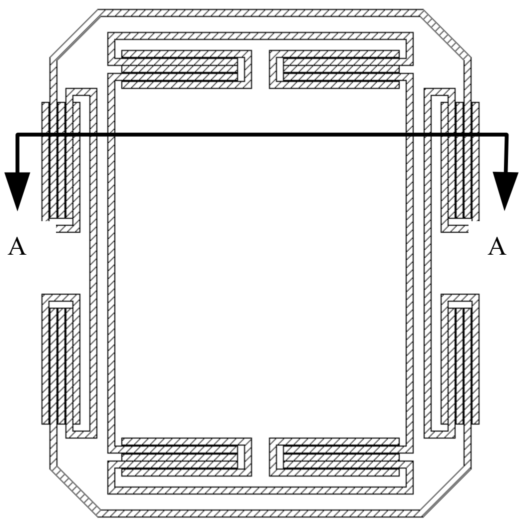
Figure A5 Cross-Sectional SEM photomicrographs of deep-etched flexures.

A.2.2. Flexure aspect ratio

Correlation of the mechanical performance of each deep-etched test structure with the fabrication process variables requires the ability to perform metrology on these structures. We have developed a method that allows us to cross-section suspended test structures after mechanical testing. By understanding how flexure geometry relates to suspension performance, we will be able to focus on controlling those processing variables that have the greatest impact on this performance.

Released, suspended test structures have been cross-sectioned as follows. First, a single test structure die is potted in low-viscosity epoxy. To eliminate air bubbles trapped around the deep etched flexures, the sample is loaded with 50 PSI of hydrostatic pressure before curing. The potted sample is then lapped until the desired location on the die is exposed. Finally, the lapped surface is mechanically polished with slurries of successively finer grit.

A typical cross-section obtained in this fashion is illustrated in Figure A6 below. Close-up images of the flexure suspension are illustrated in Figure A7.



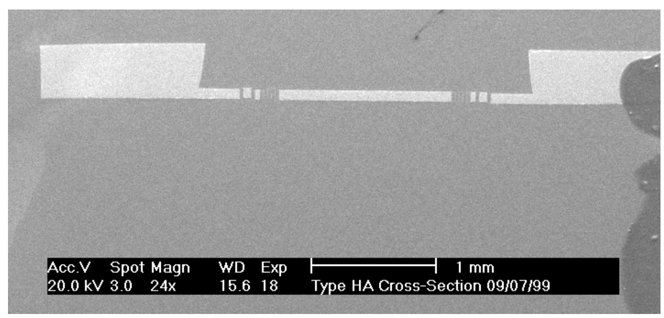


Figure A6: Left: layout of a typical test structure. The cross-section is indicated by line AA. Right: SEM micrograph of the cross-sectioned device

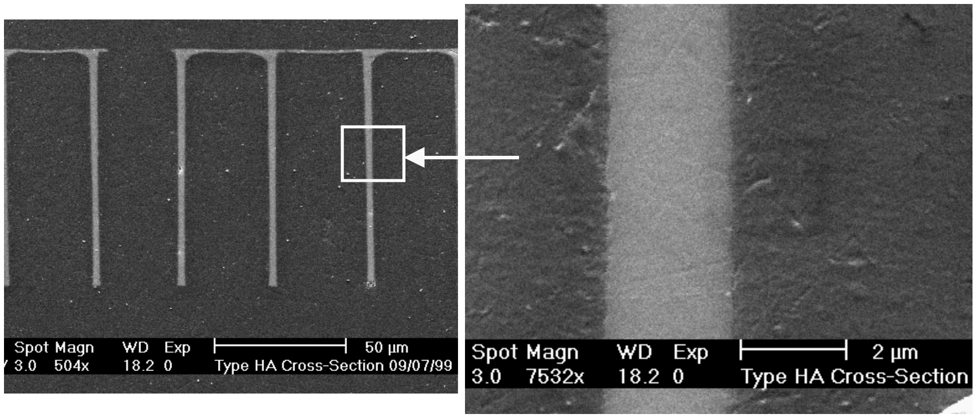


Figure A7: SEM micrographs of epoxy-potted cross-sections.

A.2.3. Platform flatness

The MBDS device requires the media be at a constant distance away from the emitter. The media need be positioned at the focal point for the emitters and have a minimum of excursion from this distance. Currently we have designed the depth of focus (or allowable excursion) to be +/- 50 nm. Experiments are done to examine the platform flatness as fabricated.

Measurements using a WYKO white-light interferometer has determined that the micro-mover was not flat, but instead was bowed across the top. The WYKO data is presented as Figure A8 and shows a bow of 400 nm over a 1500 um wide micromover. The micromover shown in Figure A8 has the integrated actuator on one side and no materials on the back. While the bowing exceeds our desired specification, it is thought that the residual stress of the media material can be controlled to compensate for this bowing which is probably a result of the actuator structure.

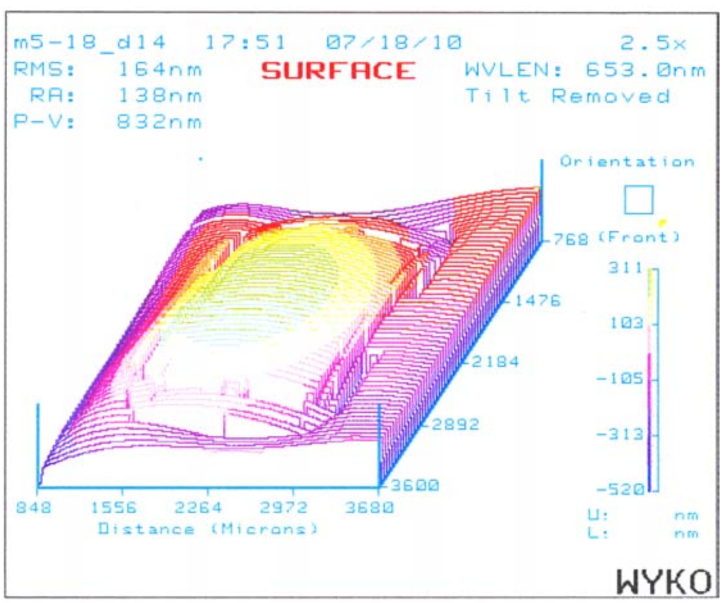


Figure A8. Surface contour map of micro-mover

A.2.4. Metal on flexures

The electrostatic surface drive requires a metallization on one surface of the released rotor platform. Electrical interconnection must be made to the layer, passing over the flexure structure, to allow the correct bias signals to be applied to the motor electrodes. A process short loop was undertaken to create the structure and test the electrical interconnection. The process is shown schematically in Figure A9. A silicon wafer is coated with a low-stress nitride (LSN) dielectric layer, a Mo metallization, and a low-temperature CVD oxide (LTO) masking layer. The oxide, metal and nitride stack is then plasma etched. The patterned, three-layer stack will serve as a mask during the subsequent silicon etch that forms the high-aspect ratio flexures. This approach is used to produce Mo interconnect traces which run on top of the silicon flexures. The fact that the same mask is used to pattern the Mo, nitride and silicon produces interconnect that is self-aligned to the flexures. The exposed silicon on the front side of the wafer is plasma etched 100 um deep, forming high aspect-ratio flexures.

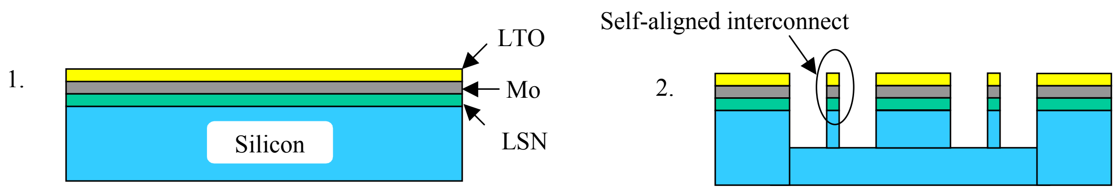


Figure A9: Short loop interconnect test. (1) a silicon wafer is coated with a low-stress nitride (LSN) dielectric, a Mo metallization, and a low temperature CVD oxide (LTO) masking layer. (2) The oxide, metal, nitride, and silicon stack is plasma etched to form flexure with an insulated metal layer on top.

A cross-sectional view of the top surface of a flexure is shown in Figure A10. Based on the layout geometry, the flexure resistance was calculated to be 1.2 kΩ for a 3 micron wide flexure. The actual width of each metal trace was reduced to 2.4 microns by undercut during processing, resulting in a measured flexure resistance of 1.5 +/- 0.1 kΩ.

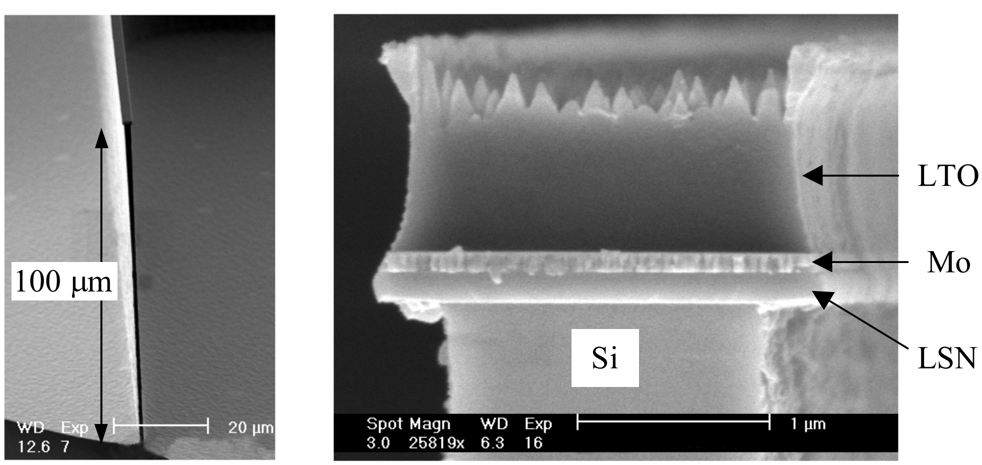


Figure A10: (left) Cross-sectional SEM of a flexure with 100:1 aspect ratio. (right) Cross-sectional SEM of self-aligned interconnect metal.

A.3. Integrated Actuator Process Design

As described in previously, suspended test structures have been fabricated by deep etching high aspect-ratio flexures into silicon on insulator (SOI) wafers. These structures incorporated a magnetic material for actuation. We also presented a process for fabricating metal interconnect lines over silicon flexures. A major limitation of the SOI process was that the structures were released by etching deep cavities into the back side of the wafer after the flexures had been formed on the front face of the wafer. Wafer handling during etching and lithography damaged the delicate flexures, resulting in low yield. A new process was developed to eliminate this problem. In addition, the new process integrates the capability of forming metal interconnect that is self-aligned to the deep etched flexures.

The modified process flow is illustrated in Figure A11. A silicon wafer is coated with a LSN dielectric layer, a Mo metallization, and a LTO masking layer. The oxide, metal, and nitride stack is then plasma etched to serve as a mask during the subsequent silicon etch that forms the high-aspect ratio flexures. This one mask step produces an interconnect that is self-aligned to the flexures. Next, deep cavities are plasma etched into the back side of the wafer. The etch is timed so that a 100 micron thick membrane of silicon remains at the bottom of each cavity. The wafer is then bonded to a carrier wafer using photoresist. The exposed silicon on the front side of the wafer is plasma etched, forming high aspect-ratio flexures into the silicon membrane. Finally, the finished device wafer is separated from the carrier wafer in an acetone bath.

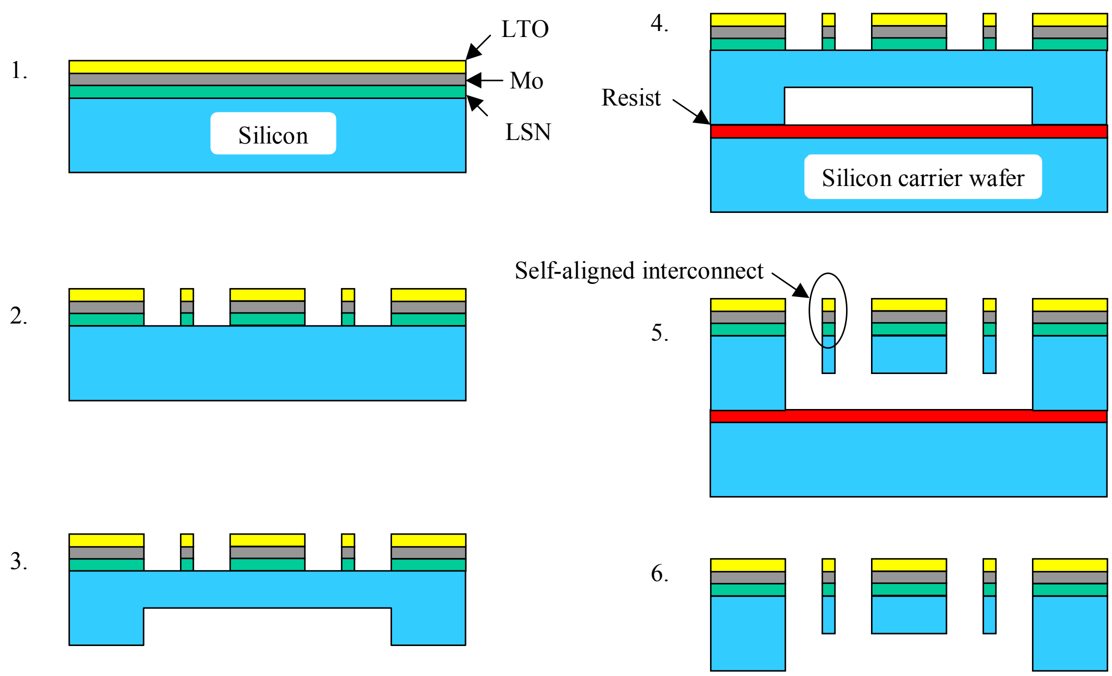


Figure A11: Modified process flow for producing micromovers with metallization. (1) a silicon wafer is coated with a low-stress nitride (LSN) dielectric, a Mo metallization, and a low temperature CVD oxide (LTO) masking layer. (2) The oxide, metal, and nitride stack is plasma etched. (3) Deep cavities are etched into the back side of the wafer. (4) The wafer is bonded to a carrier wafer with photoresist. (5) Flexures are deep etched on the front side of the wafer. (6) The carrier wafer is removed in acetone.

A.4. FABRICATION

A.4.1. Process Improvements

The preceding section described a fabrication process where by suspended structures are created from two deep silicon etches. The first etch, from the back of the wafer, is timed so a 100 micron thick membrane of silicon remains at the bottom of each etch cavity. The second etch is done from the front of the wafer creating the suspending flexures. The flexure etch also includes the capability of forming metal interconnects that are self-aligned to the deep etched flexures. The process is referred to as “cavity first” given the order of the deep silicon etches.

Cavity first was an improvement from our previous processes using silicon on insulator (SOI) wafers for fabricating the suspended structures. Structures in the old process were released by etching deep cavities into the back side of the wafer after the flexures had been formed on the front face of the wafer. Wafer handling, during etching and lithography for the backside etch, damaged the delicate flexures and resulted in low yield. The older process is characterized by the “flexure first” order of the deep silicon etches. Suspended mover structures were successfully fabricated using the cavity first process.

However, continuing development of the cavity first process revealed other yield issues that needed to be addressed. As reported previously, the deep silicon etch used to fabricate the high aspect ratio (40:1 or greater) flexures required for the MBDS device has a very precise processing window. The etch was developed on bare silicon substrates. The Bosch deep silicon plasma etch is a predominately chemical reaction etch. The rate of reaction, and thus the silicon etch rate, is very dependent on process parameters such as temperature. The STS deep silicon etcher uses a helium cooled wafer chuck to ensure uniform and controlled process temperature of the substrate. A flexure etch on a wafer with deep cavities etched into the backside is subject to much different temperature conditions than a flexure etch done on a blank silicon wafer. The cavities serve as insulating pockets that prevent heat conduction to the helium cooled back of the wafer. The higher substrate temperature during the etch results in a degraded etch profile. The flexure etch process can not be used to make the desired high aspect ratio flexures on this type of substrate.

Non-uniformity in the silicon etch rate across the substrates created additional difficulties. Etch non-uniformity is typically a 5-10% variation in etch depth from the center of the wafer (faster etching) to the edge of the wafer. A 450 um deep backside etch has a depth variation of 30 um or more. The subsequent 100 um frontside etch now requires a 30% over etch to account for the 30 um of backside etch variation. This significant over etch of the flexures severely degrades the flexure profile.

It is thought that with significant etch development, the flexure etch could be changed to produce the correct structures on substrates with back side cavities. Given the significant amount of effort already placed into developing the flexure etch recipe, it was concluded that going back to a flexure first process would be the faster road to success. Flexure first will solve the temperature problems with the cavities. Etch non-uniformity is best taken care of by returning to SOI substrates with a 100 um silicon device layer.

The new flexure first process solves the wafer damage during the subsequent backside etch by using a specially fabricated handle wafer as shown in the process flow in Figure A12.

A SOI silicon wafer is coated with a low-stress nitride (SiN) dielectric layer and a Mo metallization. The metal and nitride stack is then plasma etched using a photoresist masking layer. The resist is left in place and the stack now serves as a mask for the silicon etch that forms the high-aspect ratio flexures. A deep silicon etch, which stops on the buried oxide layer, is done to create the flexures. This approach produces

Mo interconnect traces on top of the silicon flexures and since the same mask is used to pattern all three materials, the result is interconnects self-aligned to the flexures. With the flexures etched, frontside processing is complete. A special carrier wafer with a 20 um deep recess is then resist bonded to the frontside of the wafer. The recess is larger than the device allowing the carrier wafer to be bonded without touching the fragile device area. Deep cavities are then plasma etched into the back side of the wafer using a thick resist mask. The cavity etch also stops on the buried oxide layer.. The finished device wafer is separated from the carrier wafer in an acetone bath. This also removes the residual frontside and backside etch masks. Finally, the wafer is etched in hydrofluoric acid (HF) to remove the buried oxide layer and release the MEMS devices.

Key to the flexure first process is that the critical or precision deep etch is done on a wafer with no cavities. This ensures a good etch profile for the flexures as the substrate temperature is controlled. The profile for the backside cavity etch is not as critical. The cavities are also larger than the device area and a non-vertical etch profile, the result of substrate temperature variations, can thus be tolerated.

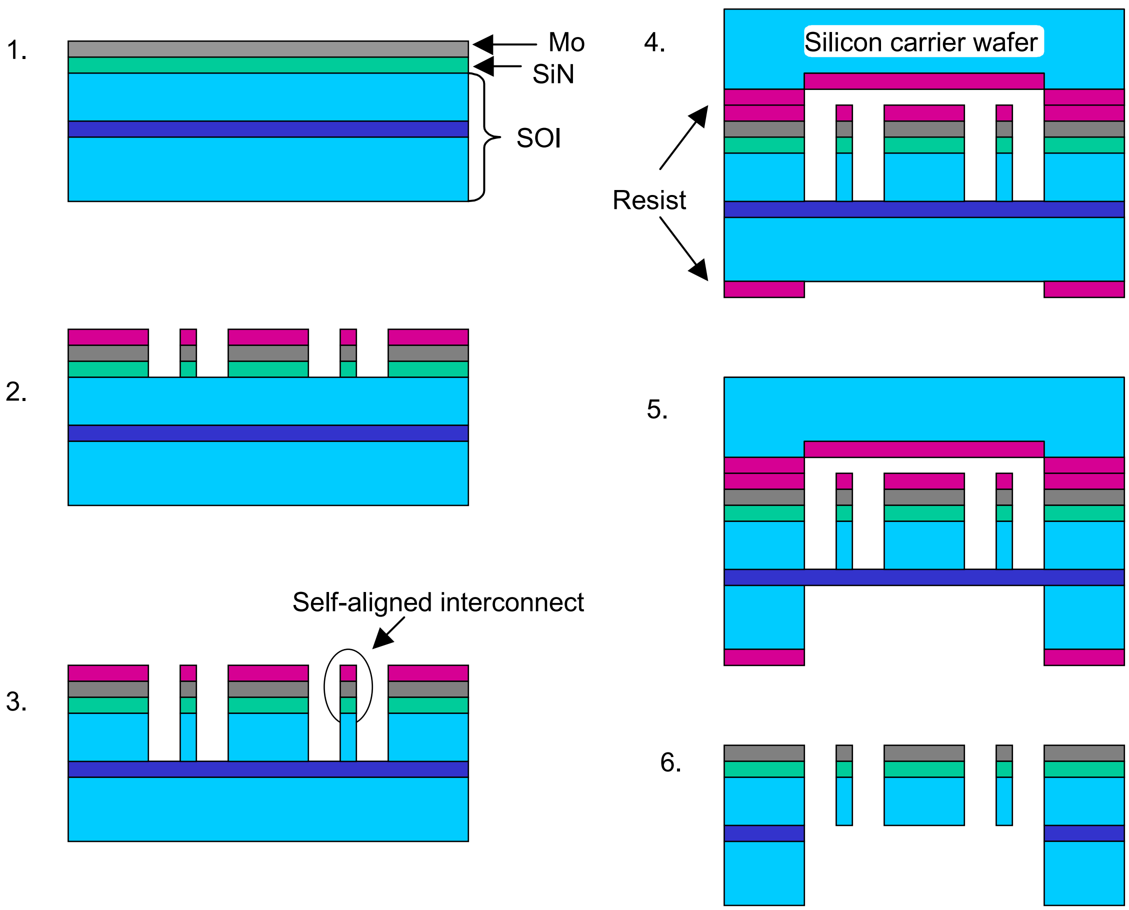


Figure A12. Flexure first process flow. (1) SOI silicon wafer is coated with a low-stress nitride (LSN) dielectric and a Mo metallization. (2) Photoresist mask is used to pattern the metal and nitride stack. (3) Flexures are deep etched with the same mask. (4) Carrier wafer with a recess, bonded with photoresist, is used to protect the front side of the wafer during backside processing. (5) Deep cavities are etched into the back side of the wafer with a thick resist mask. (6) The carrier wafer is removed in acetone and the structures are released in a liquid HF dip.

A.4.2. Completed device

The revised flexure first process produced wafers with near 80% yield for micromover structures. A robust fabrication process allows integration of the suspended micromover structures with the proprietary HP bipolar electrostatic drive. The self aligned interconnect process is used to pattern and contact a set of actuator electrodes on the suspended mover structure. A second wafer, patterned with the other set of electrodes for the actuator, is bonded to the flexure side of the micromover wafer. The two wafers are bonded together with a precise wafer to wafer spacing. Figure A13 shows a device on the bonded wafer stack. The suspended micromover is seen at the bottom of a backside cavity.

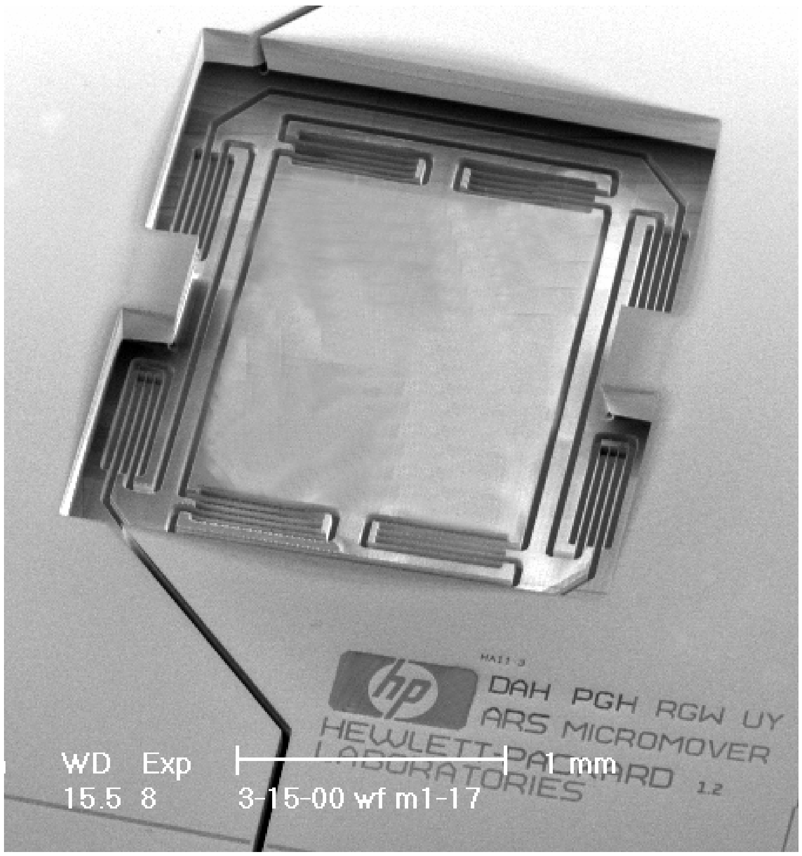


Figure A13.SEM image of the back-side of a completed suspended test structure.

A.4.3. Process yield

Another area of great interest to the fabrication of micromover devices is effects relative to the position of the device on the wafer during the fabrication process. As the number of wafer pairs containing micromovers continues to increase, it becomes possible to look at yield statistics associated with the position of the device.

Eight rotor wafers were analyzed. Each wafer contains 93 of the HP designed micromover devices. The designs fall into 3 major categories but have variations. The total number of variations is 11. Initially, the parts have been inspect to determine if the flexural system is intact at the completion of the fabrication process.

Overall yield from the 8 wafers was 421 good devices out of a total of 744 for a yield of 56.5%.

Analysis of the results by device type show the following yields: type F 59.8%, type B 59.8%, type H 47.6%. The type H design is a “stage-in-a-stage” design with the two axis suspensions connected in series. Type F and B designs have the suspension systems connected in parallel. Results from the magnetic mover test vehicles indicated much higher yields for the type H movers in that process than for the type F or B movers. It is unclear what has caused this reversal of device yield by design.

Analysis can also be grouped by flexure dimension. The current set of designs incorporated 3 flexure widths: 2.5, 3, and 4 um as drawn in the CAD package. Given a nominal etch bias of 0.5 um, this should result in devices with flexure widths of 2, 2.5, and 3.5 um. The results were as follows: 2.5 um 43.7%, 3 um 58.0%, 4 um 56.3%. As expected, yield was lower for the narrowest flexures. However, yield appears to be consistent once a certain minimum width is achieved. For the MBDS device, a finished width of 2.5 um, giving a flexure aspect ratio of 40:1 in a 100 um thick deivce, is required. This appears to be greater than the minimum width, and good yield should be possible for this size flexure.

Two designs of micromovers used on the wafer include a hybrid flexure design with flexures of different widths in different areas of the suspension. The device account for 136 of the 744 total devices. Yields on these parts were 66.1% and 63.8%, considerably higher than the average yield from the wafers. This result indicates that a careful study of the forces and process steps responsible for yield loss and then a design tailored to be resistant to these forces and also meet the MBDS performance requirements could result in a much higher yield in the micromover process.

Micromover Yield(Rotor wafer)

Good Dies/Total dies

	Column	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Row																	
A										5/8	5/8	4/8	4/8				
B				1/8	3/8	3/8	3/8	5/8	5/8	5/8	6/8	6/8	4/8	5/8	5/8		
C				2/8	2/8	3/8	5/8	5/8	4/8	6/8	4/8	4/8	1/8	6/8	5/8		
D				2/8	1/8	1/8	5/8	4/8	2/8	5/8	5/8	7/8	4/8	7/8	5/8	6/8	
E																6/8	1/8
F																5/8	4/8
G																5/8	3/8
H																	5/8
I		2/8	X	5/8	6/8	5/8	5/8	5/8	7/8	4/8	7/8	8/8	6/8	6/8	6/8	X	
J		3/8	5/8	6/8	5/8	7/8	6/8	6/8	7/8	6/8	6/8	7/8	5/8	5/8	3/8		
K		2/8	5/8	1/8	4/8	5/8	6/8	4/8	6/8	4/8	7/8	6/8	5/8	6/8	1/8		
L																	
M																	
N																	
O																	
P						2/8	2/8	4/8	3/8								

Table A1. Location of micromover devices on 4” wafer and yield at that location.

Further analysis of the yield data and early performance testing (covered in a following section) led the team to update the micromover design and process. The new devices and process were referred to as HP Labs Rev B. (This lead to the first parts being called HP Labs Rev A). The data in Table A1 refers to Rev A parts.

One of the key elements of the micromover architecture is the ability to leverage the parallel nature of semiconductor processing. Dozens of micromovers can be fabricated at the same time on a single wafer.

The high performance of the MBDS system requires this to occur at the chip level. Our current system designs have arrays of 2x2 to 6x6 micromovers on a single chip, all operating simultaneously. In addition to meeting the required performance specifications, the micromover must also be designed to achieve an efficient packing in an array as well as a high yield so all array members are functioning.

Array packing has been a key design parameter for the micromover. Array yield has been examined by looking at device yield over the entire wafer. HP Labs fabricates micromovers on 100 mm substrates. The Rev B substrates contains 208 micromover devices spaced on a 5 mm grid. One can think of this grid as a "sparse array", similar to the array needed on a MBDS chip with every over device removed. A study of the sparse array on a wafer should yield statistics that will apply to a dense array on a chip.

YIELD				
Rev B	**Flexure width (um)**			
	2.5	**3**	**4**	**5**
f	**63.9%**	**75.0%**	**93.3%**	**98.1%**
h	**80.6%**	**88.0%**	**99.0%**	
Rev A				
f	**60.0%**	**60.7%**	**57.5%**	
h	**31.3%**	**50.9%**	**56.3%**	

Table A2. Yield data from micromover process.

Table A2 shows yield data comparing two lots of micromovers, Rev A and Rev B, fabricated in the HP Labs micromover process. Rev B parts are a design revision of micromovers towards the requirements of the MBDS device and is a sample set of four wafers. Yield data for Rev A micromovers is summarized from before and represents a sample set of eight wafers. F and B refer to 2 styles of flexure configurations used in HP Labs micromovers. The flexure width is the as drawn dimension in the layout package. Since the substrates are a uniform thickness, changing the flexure width directly changes the flexure aspect ratio.

The table shows a significant increase in good parts from the Rev A lot to the Rev B lot. This can be attributed to significant design changes in the F style micromover and tweaks to the fabrication process. As expected, yield is higher for wider flexures due to their increased stiffness and resulting toughness to external forces. Most yield loss can be attributed to wet etching steps in the release portion of the fabrication process. It is very encouraging to see yield numbers approach 100% for the wider flexures – a major accomplishment in a research facility. In a production facility with automated handling equipment, it is safe to assume that yields will go up to similar levels for the narrow flexures.

Figure A14 illustrates the yield of micromovers as a function of flexure width. There is a knee in the curve where yield levels off and an increase in width is unnecessary for increased yield. This was also seen in the Rev A parts. Moving to a production facility should shift the knee in the plot to the left, allowing arrays of MDBS spec micromovers to be fabricated with high yield.

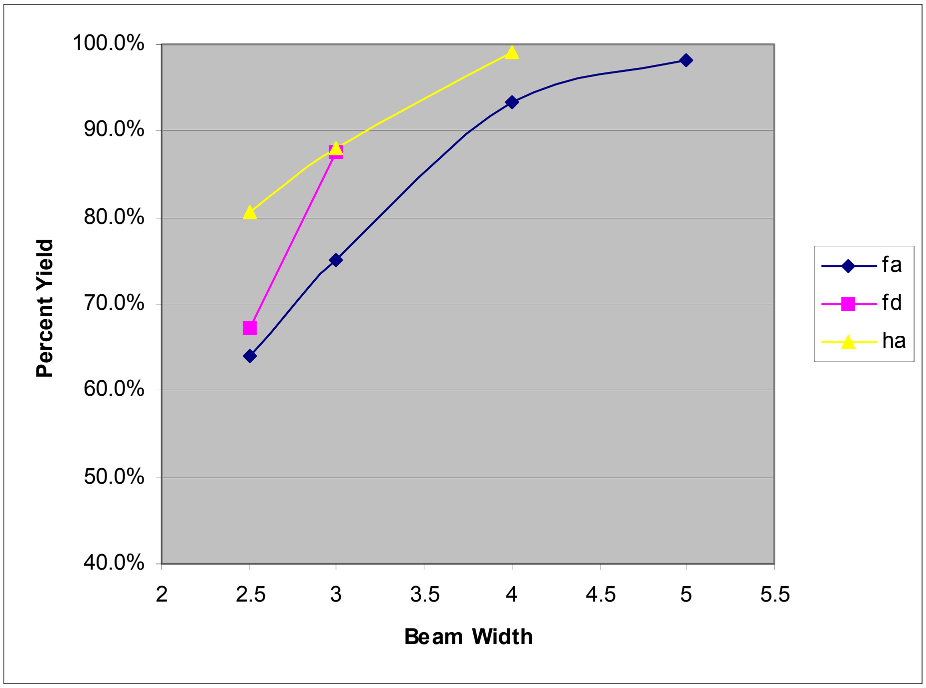


Figure A14. Percent yield as a function of flexure width. Yield data from the Rev B micromover process demonstrates that we can successfully fabricate arrays of working micromovers at HP Labs.

A.5. TESTING

A.5.1. Test setup

A new testing setup, as shown schematically in Figure A15 was constructed to characterize two-axis MEMS stage devices required by the MBDS project. The setup applies external forces to the device and then uses optical and interferometric position measurements to determine the response of the device. Testing is automated with an integrated computer system. This setup allows the testing and optimization of the magnetic micromovers short loop devices without the need for a completed MBDS device.

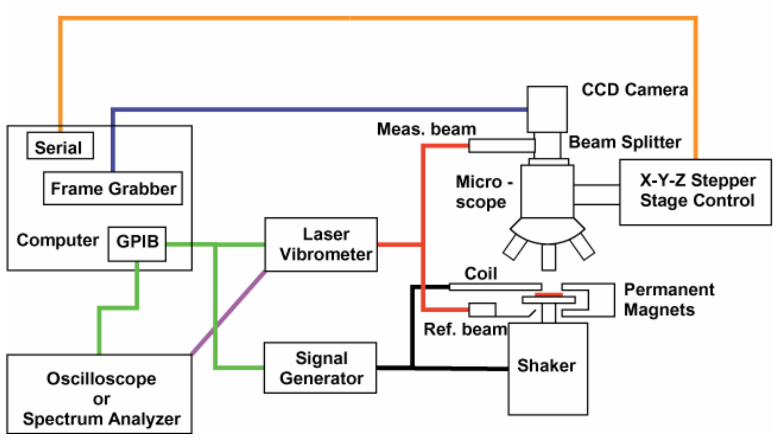


Figure A15. Schematic of micro-mover evaluation system.

The setup uses permanent and electro-magnets for in-plane actuation of a special run of prototype micro-movers (Figure A16). The movers are fabricated with a NiFe layer deposited on the stage area to respond in the magnetic fields. Special sample holders have also been designed to allow precise positioning in the magnetic field.

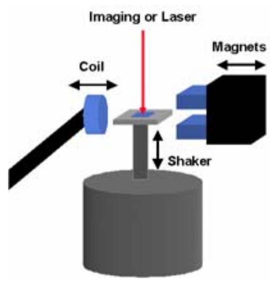


Figure A16. Magnet and shaker configuration for off chip excitation of micro-movers.

Once assembled, improvements to the DC magnet positions and to the AC coil geometry were installed. The result is enough in-plane force with the DC magnets to get full displacement of the micro-movers (30 um – the trench width around the mover). This allows device characterization at static displacements from equilibrium. The AC coil is wound to a large heat sink allowing 1-2 amps of current to be applied. The coil is easily able to excite the in-plane modes of the movers. The coil creates enough field that both in-plane axes of a device can be actuated without having to change the testing geometry.

Additionally, the movers are mounted on a vibration shake table to excite out-of-plane vibration modes. The shaker is integrated with the magnetic actuators to allow simultaneous in-plane and out-of-plane excitation of the devices.

Device responses are measured with optical based techniques. The system uses an optical microscope mounted on a XY positioning stage controlled with stepper-motors. A laser Doppler vibrometer (LDV) setup is used for measuring the out of plane response of the micro-mover test structures. A CCD camera mounted on the microscope is used with a frame grabber board and image analysis software to measure the in-plane response. The microscope is integrated into the magnetic testing system and allows precise, computer controlled positioning and focus of the measurement beams. This allows aiming the measurement beams anywhere on the test structure by moving only the optics and not the sample or excitation hardware.

The mechanical response of the testing system was characterized and an accelerometer was added to the sample holder to measure the exciter response. This serves as a reference measurement for the system. A dynamic signal analyzer is used to display the device response which is the difference between the reference and measurement signals.

Programs have also been written to computerize the data collection of the out-of-plane (Z-axis) natural frequency measurements. Integrating these programs with the motion control programs automates the testing and provides a faster, more repeatable characterization of the movers. The automation also enables a large number of movers to be tested to allow data to be collected for inter- and intra- wafer statistical analyses.

Figure A17. Photographs of the test setup and the support equipment rack.

The micro-mover evaluation system, as shown in the images in Figure A17, is an invaluable tool for characterizing micro-mover designs. With the off chip excitation system and integrated measurement techniques, precise, repeatable measurements the device parameters can be performed. The system enables prototype micro-movers to be evaluated and will determine whether MEMS XY stages can be fabricated with in the design specifications for the MBDS project.

Once micromovers with the integrated actuator were completed, they were also tested with the measurement system. The step data Figure A26 was measured using the frame grabber board in the computer to acquire images from the CCD camera mounted on the microscope. The interface for the software, written at HP, is shown in Figure A18. A region of interest is defined on the images and the brightness profile is examined. Edge detection routines analyze the profile to determine the location of the edges of the trench in the silicon that defines the mover. Pixel size on the image was carefully calibrated to allow this gap to be converted to a measurement in microns. The trench width in the device layout was 30 um. Deviation from 30 um corresponds to device motion.

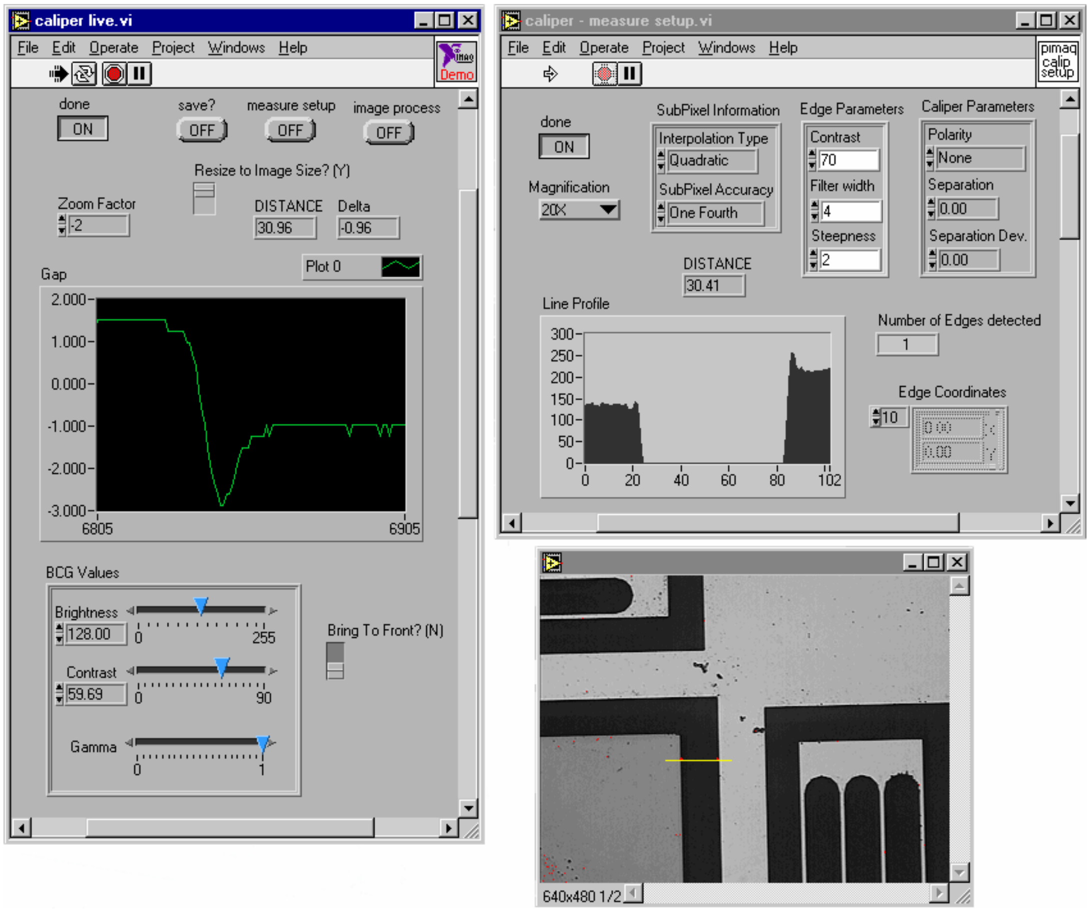


Figure A18. Caliper software, written at HP, to measure the motion of MEMS devices. Optical measurements are done by determining the gap between moving and fixed members using image analysis routines. The left widnow shows the user interface. The bottom right window is the device with the measurement region of interest shown as a thin yellow line bridging a trench. The top right window is a display of the image analysis routine. The brightness profile of the region of interest is shown in the "line profile" plot.

The caliper software has been optimized for speed and can achieve a frame/measurement rate of 30 Hz. The measurement rate is fast enough to allow DC motions of the device to be accurately monitored. Measurement limits and resolution are determined by the final objective lens used on the microscope. Maximum resolution with a 100X objective lens is about 100nm. Using a 10X objective lens, motions greater than 100 um can be measured with correspondingly lower resolution.

The MBDS device is required to operate in a high vacuum condition internal to the package. Proper development of the performance of the mover requires evaluating it under high vacuum. We have designed and constructed a custom, stainless steel vacuum chamber for integration with the LDV based measurement system. The vacuum chamber is approximately 8"x8"x24". A photograph of the vacuum chamber is presented in Figure A19. The chamber was designed for maximum flexibility to test packaged and unpackaged chips, rows, and whole wafers.

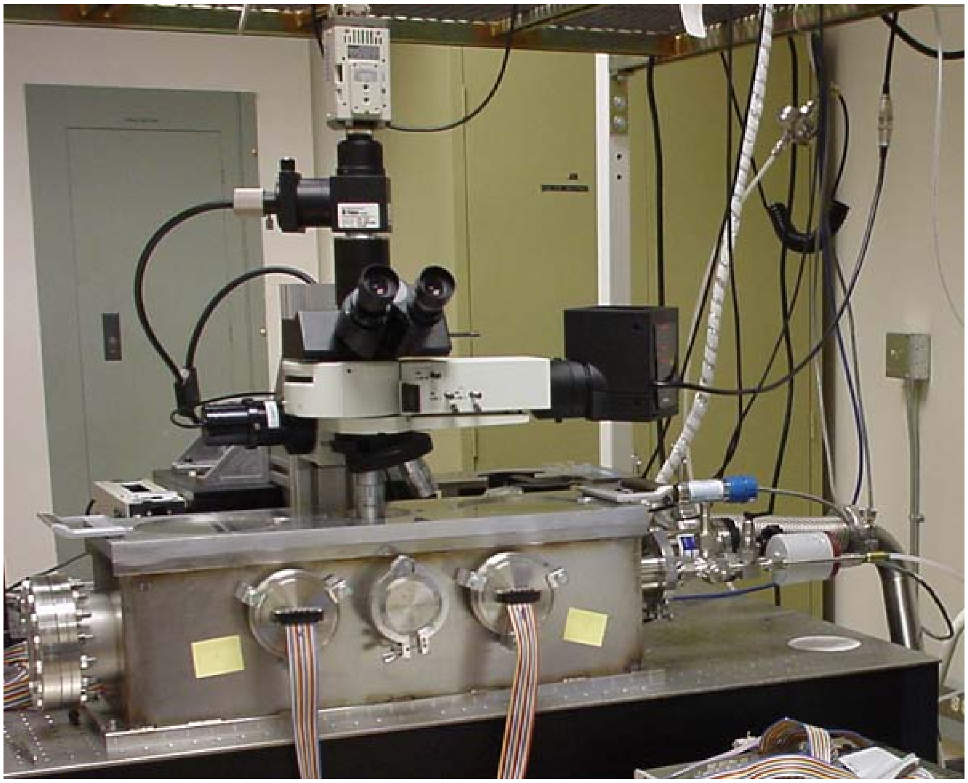


Figure A19. photograph of coffin integrated with MEMS testing system

The chamber holds two micromanipulators, each with a custom 15 pin probe card attached. Each probe card makes electrical contact with our standard configuration of 15 bond pads along one edge of the micromover chip. Mounts for probing samples were made to hold single chips, a row of chips, or a complete wafer.

In the center of the lid is a port allowing optical access to the micromover. This port is a sapphire window, 2” in diameter, to minimize distortions under pumped conditions. The sample can be mounted close enough to the window to allow the use of Mitutoyo long working distance lenses with a working distance greater than 30 mm. This allows a 20x lens to be used giving the optical test system a final magnification near 200x. Using the optical/video measurement technique previously reported, we can achieve a 200 nm resolution.

A CAD drawing of the vacuum chamber, probe manipulators, and other parts of the system is included as Figure A20.

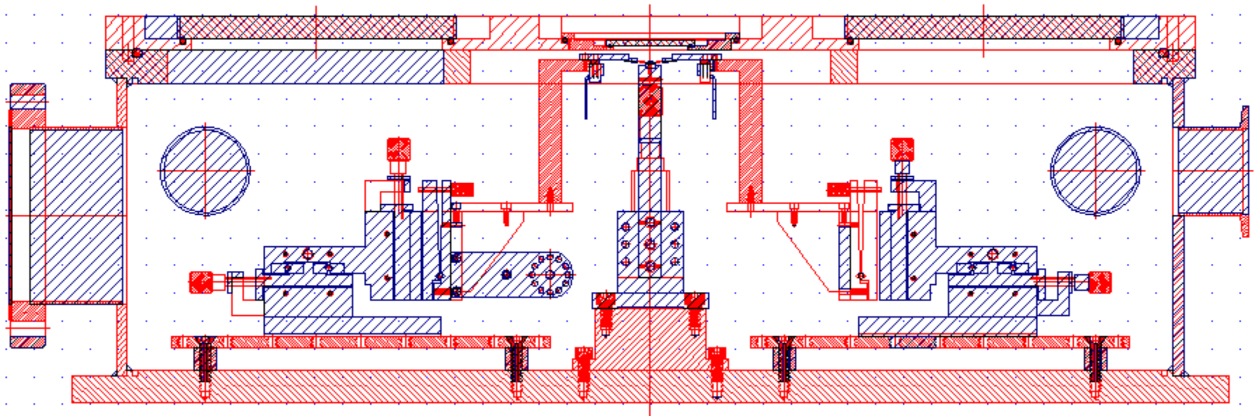


Figure A20. Coffin CAD drawings

Initial electrical measurements at atmospheric pressure and under vacuum have been done. Micromovers have been successfully actuated under vacuum.

A.5.2. Mechanical properties

More than sixty different micromover structures from five wafers have been tested using the method described in the preceding section. The goal of this testing has been to answer two questions. First, for a particular suspension design, what is the relationship between the height-to-width aspect-ratio and the ratio of the in-plane to out-of-plane stiffness? Second, how does this ratio change as a function of in-plane displacement?

As described in the introduction, the micromover must provide a 40 micron range of motion in each of the two in-plane axes while restricting out-of-plane motion to less than 0.1 micron. To satisfy this requirement in the face of similar in-plane and out-of-plane loads, the micromover suspension must have a ratio of out-of-plane to in-plane stiffness that is better than 400:1. Linear beam theory predicts that a rectangular cross-sectioned beam will have a ratio of out-of-plane to in-plane stiffness that is proportional to the aspect ratio squared, or: $kz/kx = (AR)^2$. This theory provides a theoretical limit for the maximum achievable stiffness ratio. The fact that the micromover must move in two axes requires a cascaded suspension with flexures for each axis, reducing the stiffness ratio by a factor of two.

The stiffness ratios of multiple devices with aspect ratios varying from 30:1 to 48:1 were measured and are plotted along with this theoretical limit in Figure A21. The measured suspension stiffness ratios are lower than the theoretical limit because assuming that the flexures are in pure bending is an oversimplification. In reality, there are additional stiffness losses from thick links which couple the various flexures together, and from torsional bending in the links and flexures. Additionally, the plot shows that the measured dependence of the stiffness ratio on $(AR)^2$ is sub-linear. This result stems from the fact that the torsional stiffness of the flexures declines with increasing aspect ratio, effectively increasing the torsional bending losses described above.

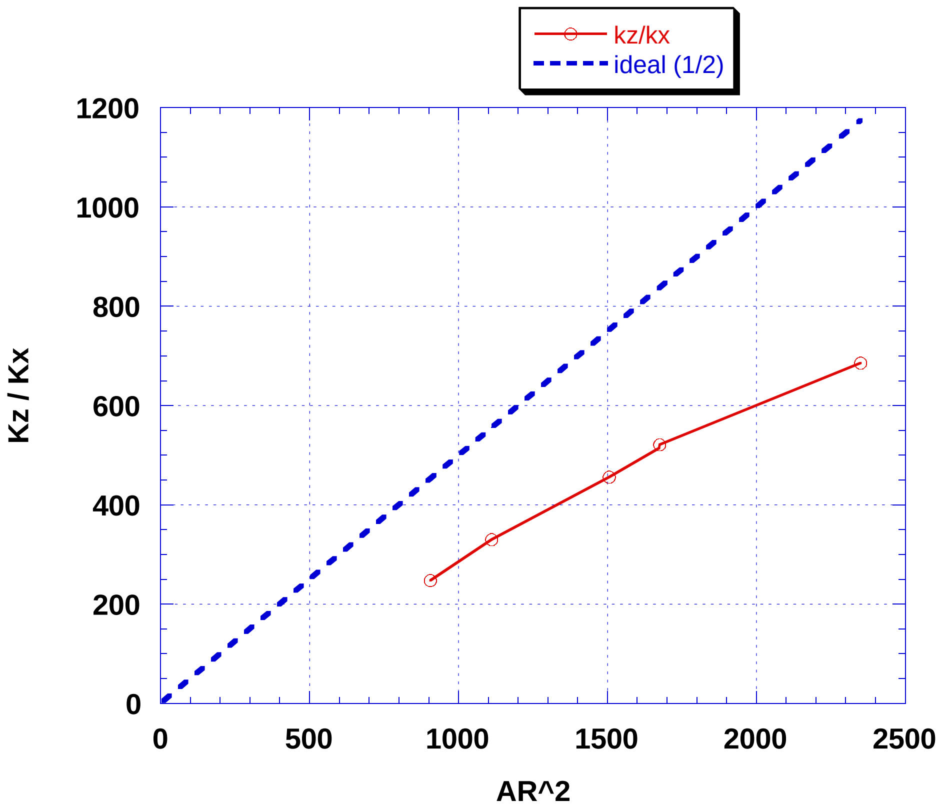


Figure A21 Measured suspension stiffness ratio (kz/kx) as a function of flexure height-to-width aspect ratio (AR).The ideal dashed line is the theoretical limit for a rectangular cross-sectioned beam in pure bending.

The dependence of the stiffness ratio on in-plane motion was also investigated. The measured results are shown in Figure A22 for suspensions with varying aspect ratios. In general, between a 10% to 20% loss in out-of-plane stiffness was observed over a 30 micron range of deflections. As the micromover translates in-plane, the flexures are deflected and the lever arm acting to produce torsional bending on each flexure is increased, reducing the out-of-plane to in-plane stiffness ratio. A model for this effect is given by:

$$kx/kz(x) - kx/kz\,(0) = a(x/L)^2,$$

where *kx/kz(x)* denotes the inverse of the stiffness ratio as a function of in-plane displacement (*x*), *L* is the flexure length, and *a* is a constant. The right hand side of this equation represents the loss in stiffness ratio as a function of displacement. This stiffness loss term is plotted in Figure A23. The behavior of each device follows the parabolic curve predicted by the model, but there is some unexplained scatter in the coefficient *a* used to model each device.

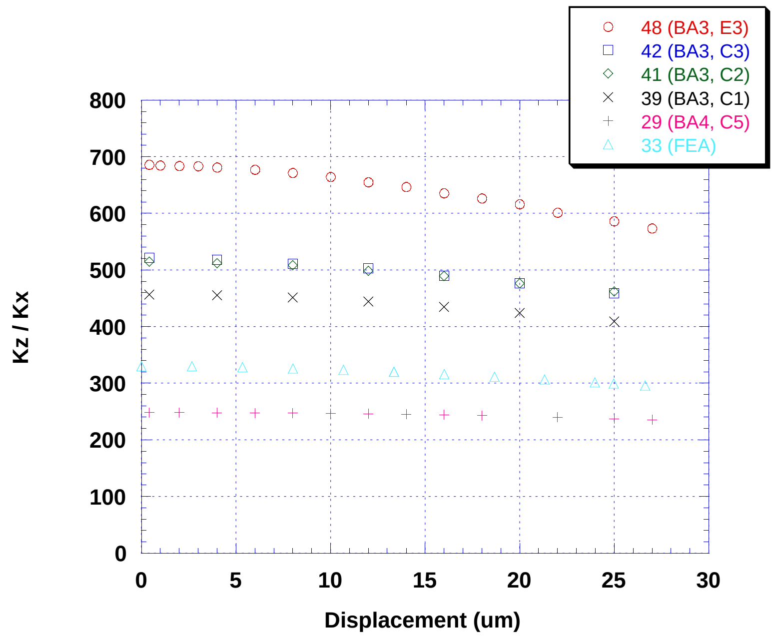


Figure A22 Loss in stiffness ratio versus displacement. The aspect ratio of each specimen is indicated in the plot legend.

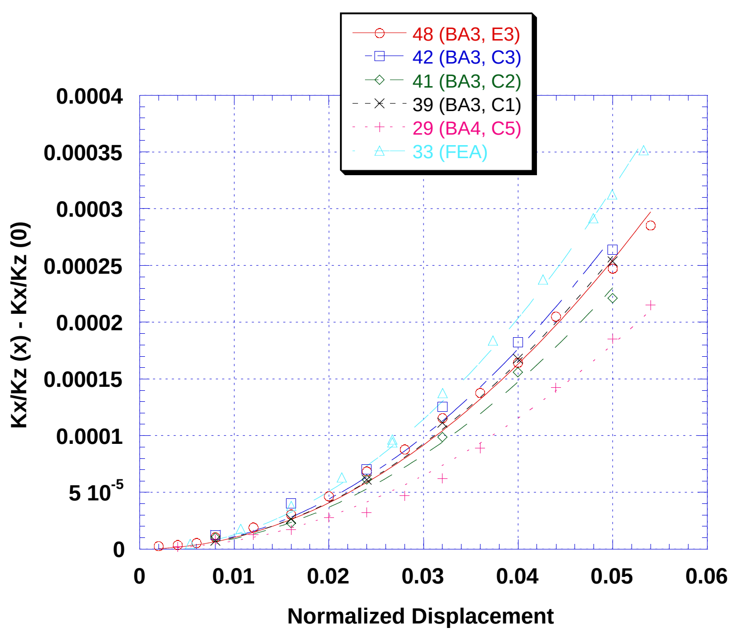


Figure A23 Nonlinear stiffness loss versus displacement for various aspect ratios. In each case, the measured change in kx/kz is plotted and fit with a parabola in x^2.

The stiffness ratio dependence versus displacement was analyzed further and also presented at the Solid-State Sensors and Actuators Workshop 2000, in June 2000, at Hilton Head Island, South Carolina. The paper was titled "Multi-Degree of Freedom Dynamic Characterization of Deep-Etched Silicon Suspensions." The results show how a nominal beam width can be determined for a given device and used to compare device parameters to theory. A summary of the results follows here for completeness.

The measured stiffness ratio (k_z/k_x) of seven devices along with the ratio calculated by FEA (finite element analysis) is represented as Figure A22. Test samples with both 3 um and 4 um as-drawn flexure widths were tested, with the 3 um beams having a higher stiffness ratio than the 4 um beams. However, varying beam profile caused the stiffness ratio to vary from device to device. Devices with 5 um flexures were too stiff to be displaced by more than 10 um and do not appear on the plot. The FEA model had the same geometry as the test samples and a 3 um flexure width. The nominal stiffness at zero displacement, k_{x0}, was used in preparing this plot.

$$\frac{k_x}{k_z} = \left(\frac{w}{h}\right)^2 + \alpha\left(\frac{x}{L}\right)^2 \qquad (1)$$

In general, the out-of-plane stiffness diminished parabolically with in-plane displacement, as described by Equation (1), where w, h, and L are the width, height, and length of the flexure, x is the inplane displacement and α is a constant. The data in Figure A23 corresponds to the inverse of Equation (1). When plotted in this form, the stiffness loss increases with aspect ratio, however, the parabolic loss term, α, is largely independent of aspect ratio. The constant is theoretically equal to 0.14 for a simple beam with aspect ratio greater than 5:1, but tested suspensions consisted of cascaded beams of two lengths, each of which was subjected to a different deflection to achieve a particular stage displacement. Correcting for these factors, the predicted parabolic loss term for these suspension designs was 0.09. The 3 um flexures had an average measured parabolic loss constant of $\alpha = 0.09$, while the 4 um flexures had a slightly lower measured loss constant of $\alpha = 0.07$.

While the devices with 3 um flexures have a higher stiffness ratio than those with 4 um flexures, there is a great deal of variation from device to device. This variation is due to the edge-to-center beam profile variations. A convenient way of comparing the various devices is to plot the nominal stiffness ratio of each as a function of the flexure aspect-ratio. Direct measurement of the beam profile would require destructive cross-sectional analysis, so a simpler approach was adopted. Assuming a rectangular beam profile, the nominal beam width was estimated from the ratio of the measured natural frequency to that predicted by the FEA model:

$$w = w_{FEA}\left(\frac{f_x}{f_{x,FEA}}\right)^{2/3} \qquad (2)$$

Despite the fact that the fabricated beam profiles deviated slightly from rectangular, the estimates calculated from Equation (2) proved reasonably accurate. Two cross-sections measured using a SEM are shown along with estimated widths in Figure A24.

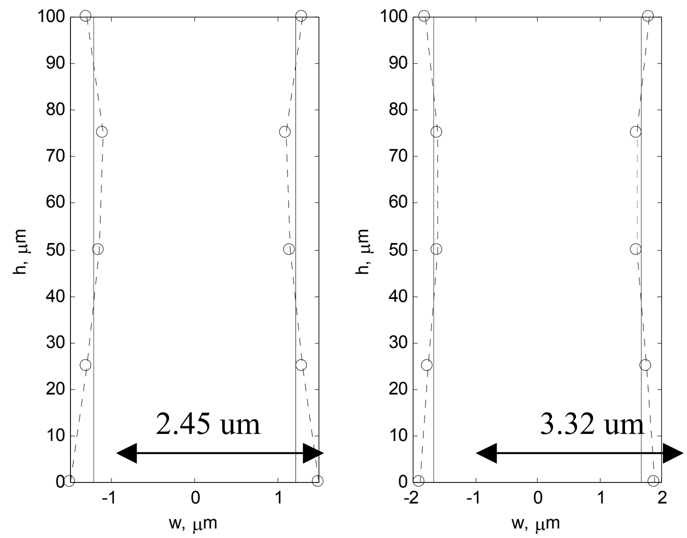


Figure A24. Measured beam profiles and widths estimated with Equation (2).

The nominal stiffness ratio at zero displacement is plotted in Figure A25 as a function of the aspect ratio computed from Equation (2). The theoretical relationship between the stiffness ratio and aspect ratio can be found from the ratio of the mass moments of inertia as $k_z/k_x = (h/w)^2$. The x-y micromover design cascades two axes of motion in series to allow two degress of freedom. This series combination of elements reduces the theoretical relationship between stiffness ratio and aspect ratio by a factor of 2, $k_z/k_x = ½(h/w)^2$. This theoretical value is plotted as a solid line in Figure A25, while a linear fit to the data is plotted with a dashed line. The slope of this fit is 0.32, or 36% lower than the theoretical maximum stiffness ratio. The fact that the FEA data also fits close to this curve suggests that the suspension design is the main source of this loss, rather than any nonideality in the flexures themselves.

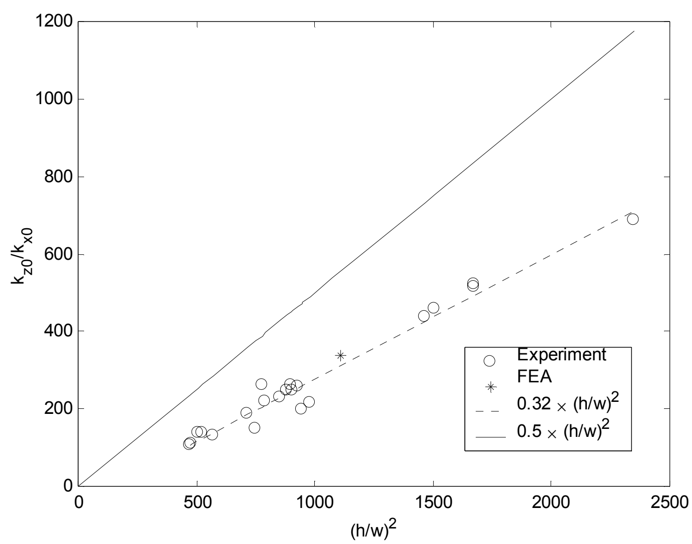


Figure A25.Nominal stiffness ratio (k_{zo}/k_{x0}) vs. aspect ratio squared. A linear fit to the data is indicated with a dashed line, while a solid like indicated the theoretical limit.

A.5.3. Electrical performance

Micromover devices from the Rev A process were successfully tested in June 2000. On these parts, the actuator was energized and used to move the suspended structure in one axis +/- 20 um for a total travel of 40 um, the target for the device. Over this range of travel, the measured Z displacement was < 20 nm, also within device specifications. The device performance matches the electrostatic and mechanical models that have been developed for the micromover with integrated motor. The ability to fabricate 40:1 aspect ratio flexures lets the mover have large inplane travel and also resist the pull down force generated by the actuator.

A video demonstration of the micromover and integrated actuator was presented at the DARPA MEMS PI meeting in August 2000, in Boston, MA.

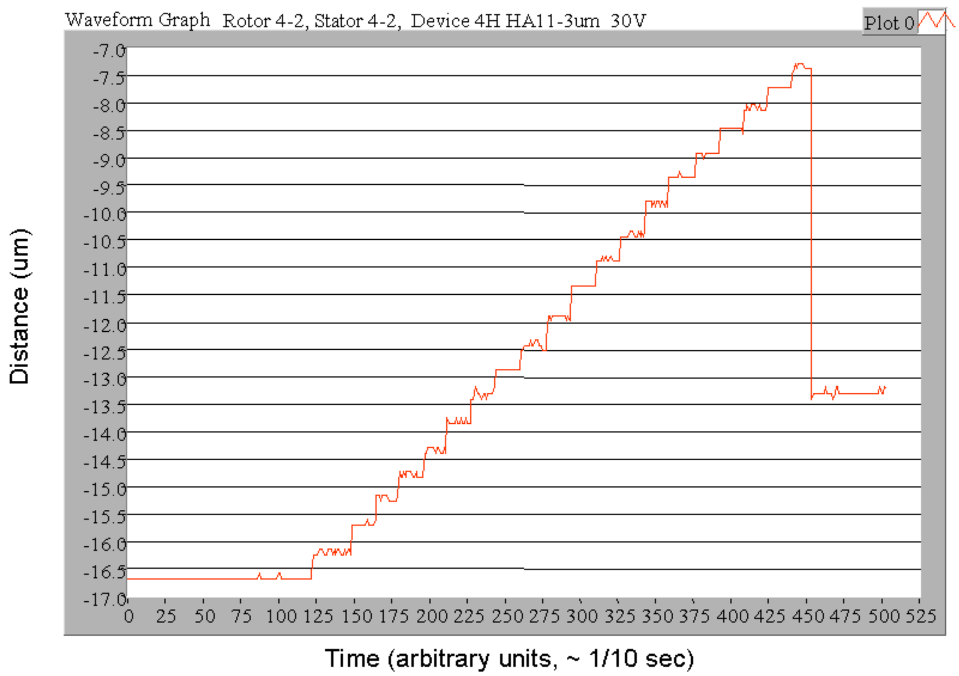


Figure A26. Micromover motion by integrated bipolar electrostatic motion. Step size is about 0.5 um.

A micromover device, fabricated with 2 um flexure width on a 80 um thick substrate was use to generate the data in Figure A26. The plot shows a progression of 20 steps taken by the micromover at a drive voltage of 30 V. At a time index of approximately 450, the position of the mover changes by about 6 um as the result of a decogging of the stepper motor. Decogging occurs when the motor attempts to take an inplane step to a location where the restoring force of the flexural suspension is now greater than the inplane force generated by the actuator. The position of the micromover shifts by one period of a stator electrode group to a minimal force position that is closer to the flexural equilibrium of the device. This event allows us to determine the performance of the actuator relative to the flexural suspension.

The data shown in Figure A26 was collected using the micromover evaluation system described earlier. The system, shown schematically in Figure A15, integrates a microscope, computer, LDV system, and custom sample holders for actuating and monitoring MEMS devices. The step data was measured using the frame grabber board in the computer to acquire images from the CCD camera mounted on the microscope. Edge detection routines analyze the profile to determine the location of the edges of the trench in the silicon that defines the mover. Pixel size on the image was carefully calibrated to allow this gap to be converted to a measurement in microns. The trench width in the device layout was 30 um. Deviation from 30 um corresponds to device motion.

A.6. EVALUATION

A.6.1. Comparison to models

Measurements of the travel distance where the decogging of the motor occurs can be compared to mover performance determined with an electrostatic simulation package. The simulator was developed at HP for general MEMS actuator studies. The data are summarized in Table A3.

Bias Voltage (V)	Measured steps before decogging	Distance at decogging (um)	Calculated distance at decogging (um)
10	8	4	4.8
15	11	5.5	6
20	17	8.5	7.2
30	25	12.5	11.2
35	29	14.5	13.2
40	35	17.5	16.8
45	40	20	19.2
50	48	24	24
55	57	28.5	28.8
60	66	33	33.6
65	75	37.5	38.4
70	89	44.5	45.6

Table A3. Measurement of decogging distance and comparison with simulation.

The simulator was run with approximate parameters input from the process run, such as device thickness, flexure width, and rotor/stator gap. The simulator calculates the stiffness of the device, the forces generated by the actuator, and the equilibrium position for the rotor. The results indicate that flexural suspension performs as calculated by the simulator. Small discrepancies are due to the discretizations from the finite step size.

Measuring the micromover motion with the electrostatic actuator has served as another verification of the design and performance of the flexural suspension.

A.6.2. In-plane Micromover performance with integrated actuator

The initial functioning micromovers with integrated actuators (Rev A) were very successful. The Rev B parts were further optimized to the capacity and performance goals of the MBDS project. To meet the low power requirements, the actuator and suspension have been redesigned to the limits of the processing window that has been developed at HP Labs. The micromover was enlarged and the electrode pitch on the actuator reduced to allow a micromover to reach its full travel requirement at an operating voltage of 40 V or less.

In-plane movement is two-dimensional movement that the micro-mover is designed to perform, such that an emitter can access a particular section of media. In the redesigned wafer set M5-18, the chip D14 is a H-style micromover with a 3 um wide flexure as drawn in CAD. D14 moved 104 steps in the x-direction at an operating voltage of 40 V. The new electrode pitch creates a physical step size of 0.4 um. The required micromover travel for full capacity is +/- 20 um, corresponding to 100 steps. Thus, the Rev B micro-movers are able to meet this MBDS project specification.

The in-plane travel limit is a function of the operating voltage. The higher the voltage, the more force generated by the actuator and the further the mover can travel against the restoring force of the mechanical suspension. Position is not a function of operating voltage for our actuator, but rather the position limit depends on voltage. Device performance is best determined by measuring the number of steps a mover can travel at a given operating voltage before a decog event occurs at the position limit. The maximum number of in-plane steps was compared to the applied voltage for several chips from the M5-18 wafer set and shown in Figure A27. The number of steps was discovered to be approximately proportional to the squared voltage, agreeing with theoretical modeling of the bipolar surface actuator. The variation in the performance of a given device (seen as a variation in slope in Figure A27) is a function of the suspension design and flexure width.

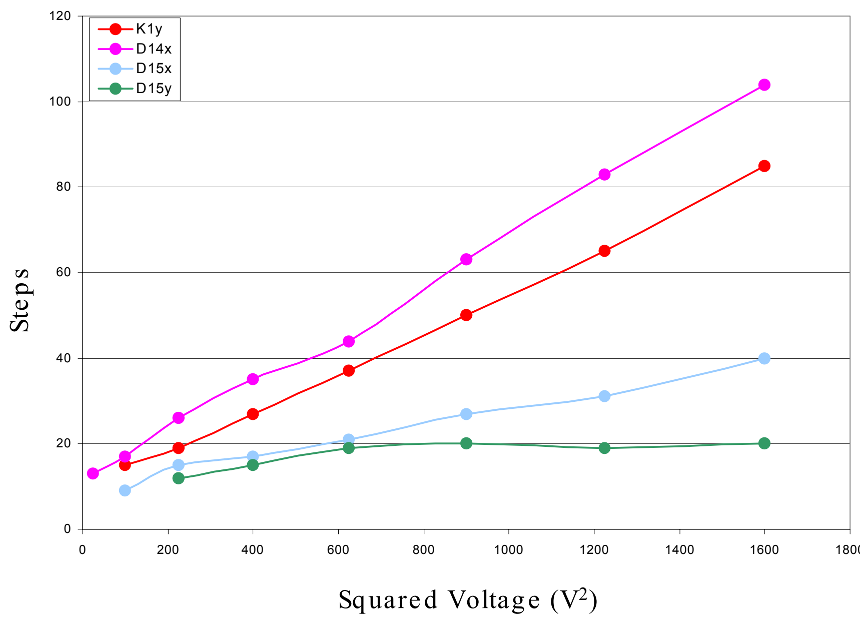


Figure A27. Micro-mover steps as a function of squared voltage

A.6.3. Z height Stability

The z-height stability of the micromover is crucial to the MBDS device operating correctly. The storage medium must be positioned at the correct distance relative to the electron emitters for proper interaction. In addition to the initial flatness of the micromover platform, z distance variations could cocur during platform motion. Motions in the z-direction can be caused by external stimulus, such as shock, or internal forces generated by the actuator. Changing electrostatic potentials in the bipolar surface actuator alter z-directional attractive forces and thus the position of the micromover relative to the emitters. The two situations during which this motion may occur are initial electrode charging and stepping motion of normal operation.

(1) Initial Electrode Charging

Initializing electrodes involves charging select electrodes, Figure A28, which had all previously been grounded while the device was in a standby or off state. When charged, the electrodes create electric fields which attract the micro-mover to the stator. This is the pull-down-force associated with the bipolar surface actuator.

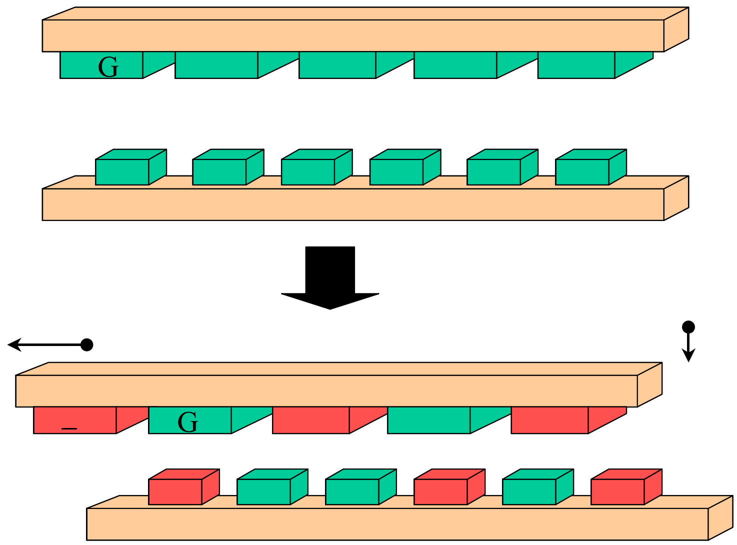


Figure A28. Initializing electrode movement

Using the LDV based testing system and an oscilloscope, the displacement in the z-direction was measured as a function of voltage during electrode initialization. The oscilloscope screen is shown in Figure A29. The purple line is the applied operating voltage and the green line is the measured displacement. The displacement was found to vary parabolically with a linear voltage ramp. This is the linear displacement as function of squared voltage that is predicted by models of the actuator. The maximum z-displacement measured is 51 nm at the operating voltage of 35 V.

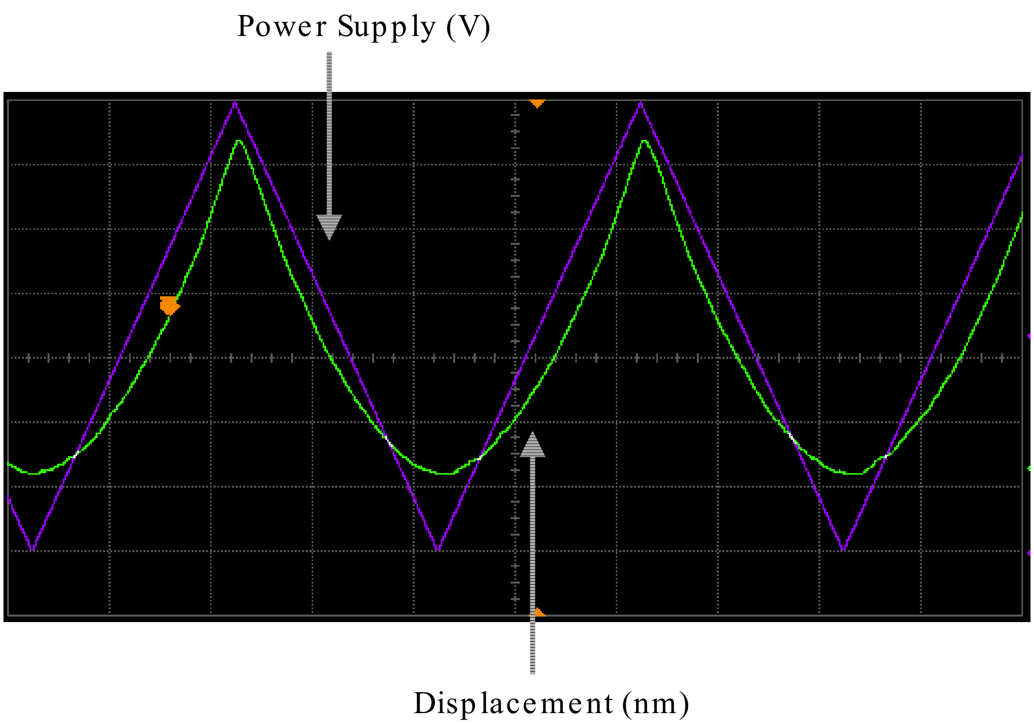


Figure A29. Plot of z-axis displacement as a function of voltage. Power supply is a scale of 5 V/div. Displacement is 10 nm/div.

(2) In-plane Micromover Operation

During normal operation of the micromover, z-directional movement may occur due to a change in the potential of a single electrode. Figure A30 illustrates the change of one electrode on the stator (denoted with a – symbol on the bottom wafer) and the subsequent shift of the rotor to the left; the device has taken a step. In addition to in-plane motion, out-of-plane movement may also occur during this event due to changes in the electric fields.

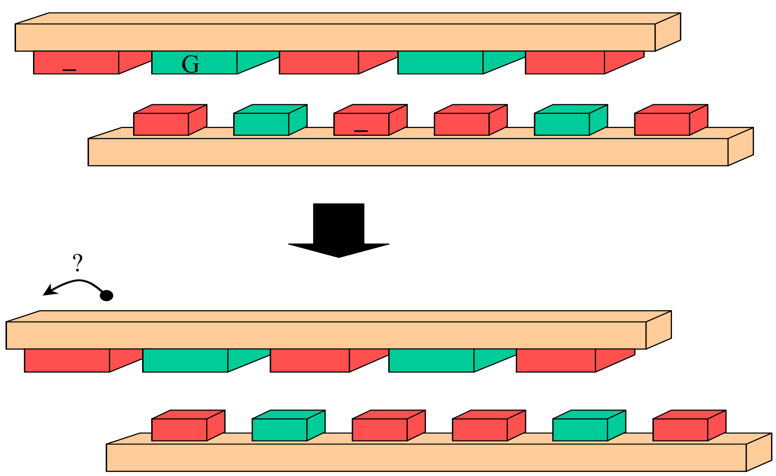


Figure A30. Stepping electrode movement

The micromover electrodes are initialized. An oscilloscope plot, Figure A31, can then be captured depicting z-directional displacement triggered by charging a single electrode to a potential of 30 V. This act of taking a step shows a sinusoidal pattern of z-displacement develop after the event. The amplitude of this pattern is 2.2 nm, and the frequency is 1333 Hz. Previous measurements using a WYKO white-light interferometer has determined that the micro-mover was not flat, but instead was bowed across the top. The WYKO data is presented as Figure A8 and shows a bow of 400 nm over a 1500 um wide micromover. Trigonometric analysis reveals that for an inplane motion of a single step (400 nm), the change in micro-mover height is approximately 2 nm. This height is the same as the amplitude of the oscillating wave on the oscilloscope plot. Additionally, previous experimentation concluded that the resonant in-plane frequency was 1344 Hz, which is very close to frequency of 1333 Hz measured with the oscilloscope. Therefore, by taking an in-plane step, the in-plane resonant frequency is excited, and the micro-mover vibrates at that frequency as it settles in the new position. The measured z-directional displacement resulted from the bowed shape of the micro-mover, not from any true micro-mover z-directional displacement. Therefore, z-axis displacement can be said to be negligible during stepping.

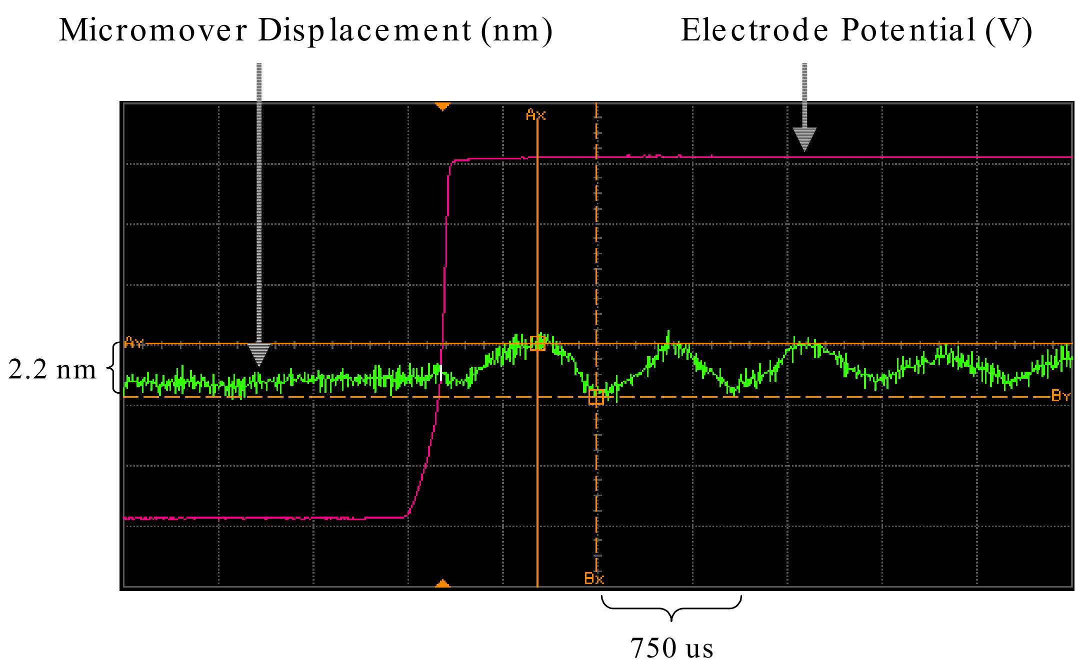


Figure A31. Plot of z-axis movement as a function of stepping voltage

(3) Summary

By measuring the z-axis motion in the two states of the actuator, we conclude that the micromover shows negligible z-motion (< 2 nm) under operation. The z-axis performance satisfies this MBDS project specification.

A.6.4. Comparison to design parameters for system

In evaluating the fabrication process and suitability of the micromover design for the MBDS, it is important to determine the key parameters of the completed micromover for comparison with expected design values.

Micromover performance can be compared to results from the modeling software developed at HP Labs by performing a multitude of tests of device performance and characteristics. The pull down test just described is useful in determining the gap between the rotor and stator wafers, one of the key parameters in the performance of the actuator.

The natural frequencies of the device are measurable quantities that give insight into the mass and stiffness of the mechanical system. As previously reported, the electrostatic actuator, when energized, affects the apparent stiffness of the system. It is both possible and important to measure the natural frequencies of the system off and energized to accurately determine the individual components.

Finally, as discussed in before, determining the number of steps a device can take at a given operating voltage without decogging gives a measure of the force generated by the actuator.

These measurements have an overlap of parameters that can be extracted. By combining the results of these measurements, the modeling software can be used to determine the most likely values for critical micromover device parameters by making sure the individual test results are consistent with the modeling.

The next three figures present comparisons between measured data from a device, D14, and results from modeling. For example, one period of data can be extracted from Figure A29 to be compared to simulated values of the micromover device. Figure A32 shows the modeling data with some of the input parameters to the simulation and the pull down data from Figure A29.

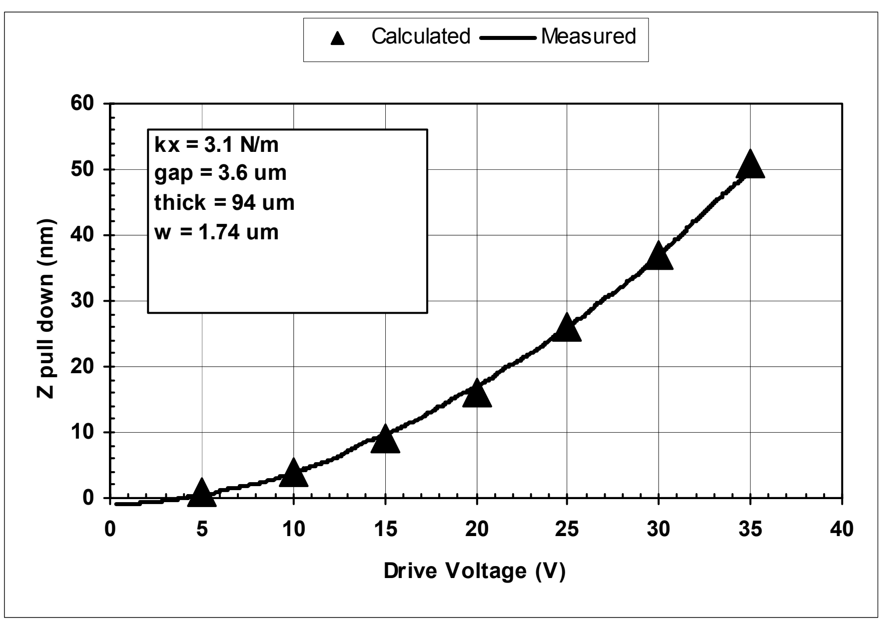


Figure A32. Theoretical and Experimental z-axis displacement as a function of voltage

Figure A33 is a replot of the measured values for D14 from Figure A27 with the results from the HP modeling software for the micromover system.

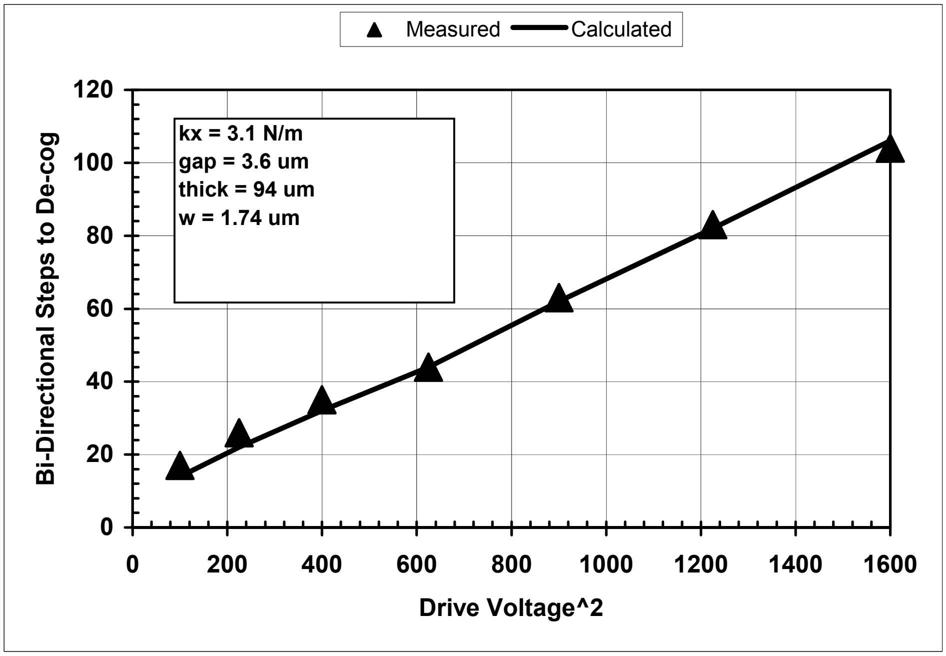


Figure A33. Calculated and measured values for steps to decog event as a function of operating voltage.

Figure A34 plots measured values for the inplane natural frequency as a function of operating voltage on the actuator. Higher operating voltages create more restoring force in the actuator and appear as a stiffening of the system. The frequency is seen to rise from 350 Hz at 0V to 1344 Hz at 30V.

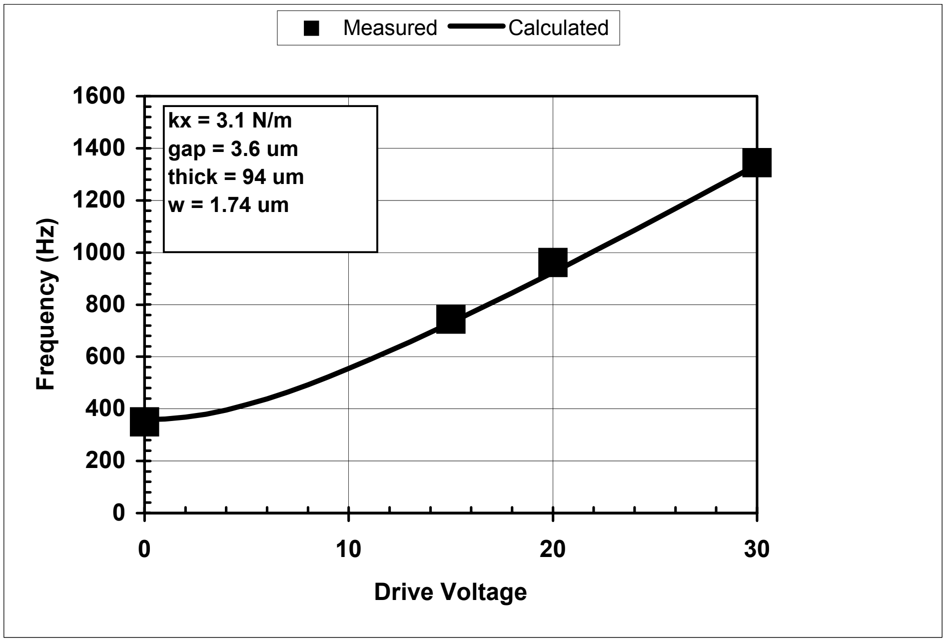


Figure A34. Calculated and measured values for the dependence of in-plane natural frequency on operating voltage.

Figure A32, Figure A33, and Figure A34 show generally good agreement between results from the HP Labs micromover modeling software and measured data from a working micromover. To get a good fit, the correct device parameters must be input into or derived by the software. Certain parameters can be measured such as the data in the plots, the device natural frequencies, and thickness of the rotor wafer. Others are derived from the modeling using best guesses to seed the calculations and then iteration to make all the modeling results match the measure results. The large amount of measured data and varied techniques for collection build confidence that the determined parameters are as accurate as possible. A table of parameters extracted for D14 is presented in

Reference: xyha11			M5-18, D14	
Beam Width, wf (μm) =	1.76		kx (N/m) =	3.17
Beam Height, h (μm) =	94		ky (N/m) =	2.96
Rotor Thickness, t (μm) =	100		kz (N/m) =	2250
AR =	53		kz/kx =	710
			kz/ky =	760
fx (Hz) =	413		mxeff (μgm) =	471
fy (Hz) =	349		myeff (μgm) =	616
fz (Hz) =	10828		mzeff (μgm) =	486

Table A4. Extracted device parameters for M5-18, D14.

Another key component of the micromover design is its inherent positional accuracy. The step-wise nature of motion, where position is not dependent on voltage level, but rather electrode configuration, allows for a digital nature for position addressing. The Rev B design uses a 2.8 um pitch on the rotor electrode and a stator group containing 7 electrodes. This gives a natural step of 2.8/7 or 0.4 um for the device. One change in stator electrode state will cause a 400 nm shift in micromover position.

The MBDS system desires a smaller bit size than 400 nanometers – smaller bits equals higher storage density. To achieve this, the electrodes are driven with a digital to analog converter (DAC). Instead of two voltage levels (off and on) the electrode can now have voltages in steps at the resolution of the DAC. Eight bit DACs have been used in micromover testing. When the micromover is actuated from one position to the next, one electrode is changed in voltage level, either to on or off. This electrode is called the proportional electrode. When connected to a DAC, the proportional electrode can shift by one LSB (least significant bit) resulting in a much smaller motion.

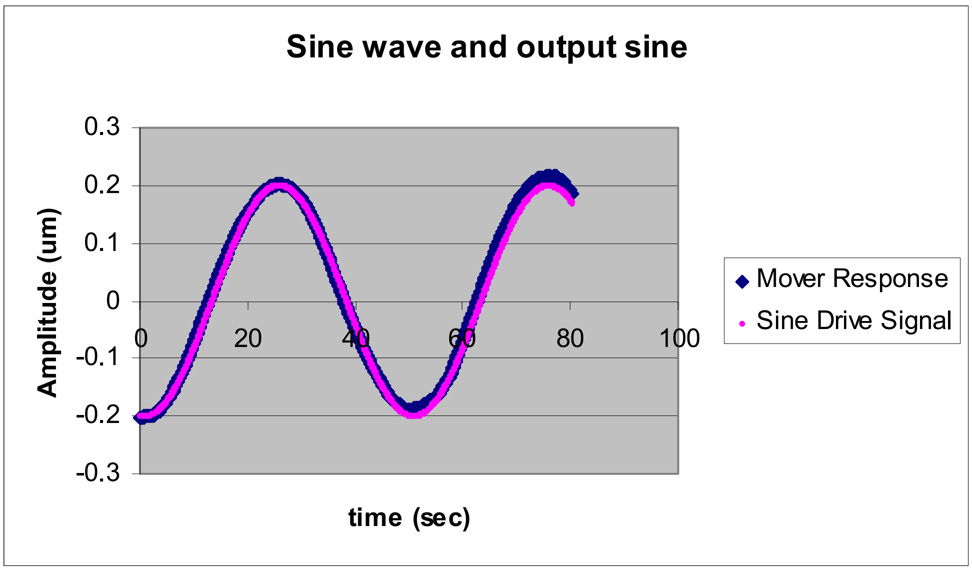


Figure A35. Response of micromover to sine wave on proportional electrode.

Figure A35 shows the response of the micromover to a sine wave signal driving the proportional electrode. The pink dots are the sine wave input and the blue diamonds are the measured position from the MEMS characterization system we have previously described. A laser interferometer is used to measure the postion of the micromover as it moves between two major steps, or an amplitude of 0.4 um. From the figure, it can be seen that the micromover identically tracks the drive signal.

Thus we have demonstrated that position between two major positions (400 nm apart) varies linearly with voltage on the proportional electrode. Using a 8 bit DAC effectively divides a major step into 256 sub-steps. The size of a sub-step is thus 400 nm / 256 = 1.56 nm.

Using a laser measurement system, we have shown a repeatable step size at one LSB change in the DAC output. The test setup allows the DAC to be connected to each proportional electrode in succession, providing for fine resolution over the entire travel of the micromover. The device demonstrated repeatable behavior in the noise free environment of the testing lab.

The micromover full range travel is 40 000 nm with 1.56 nm positional resolution, or 39 ppm.

This resolution is much greater than the proposed 50 nm bit size in the MBDS system. High position resolution allows a servo loop to be closed for position maintenance of the device for operation in the real world of portable electronic devices. The usage of a DAC maintains the digital nature of the micromover position addressing. To facilitate position maintanence, micromovers have been fabricated with integrated position sensors. The sensors, servo loop, and position control have been successfully tested on a two axis micromover.

A.7. Two Axis Motion

We have previously reported full travel, one axis motion for the micromover. This would enable a device to scan along a track of data. Two axis motion is required to step the read/write position from track to track. Rev B micromovers have been fabricated that are capable of full travel, 2 axis motion.

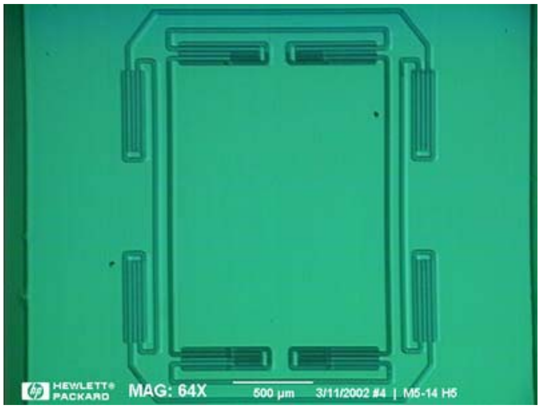


Figure A36. A 4um H-style micromover, device number H5 from wafer M5-14.

Figure A36 shows a two axis micromover device from a Rev B wafer. The device is numbered H5 and has 4 um flexures drawn in the CAD layout. Figure A37 – Figure A40 show a close up view of the upper right hand corner of the device in Figure A36.

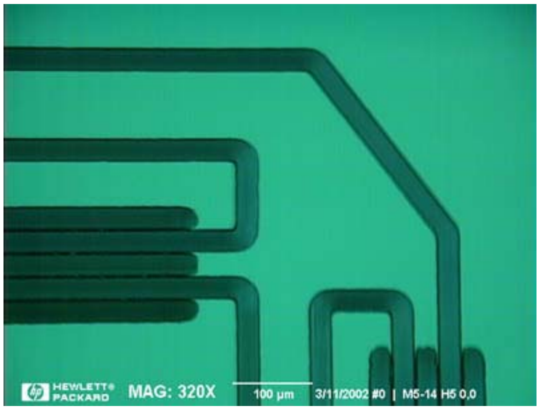


Figure A37. Device H5 at the home position.

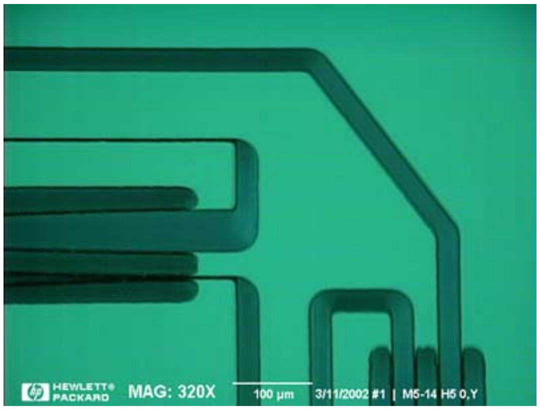


Figure A38. Device H5 at the Y max position

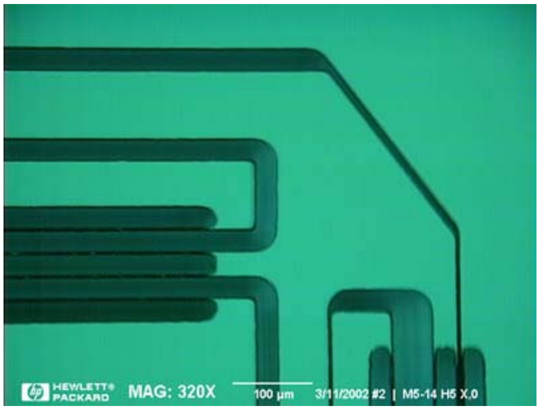


Figure A39. Device H5 at the X max position.

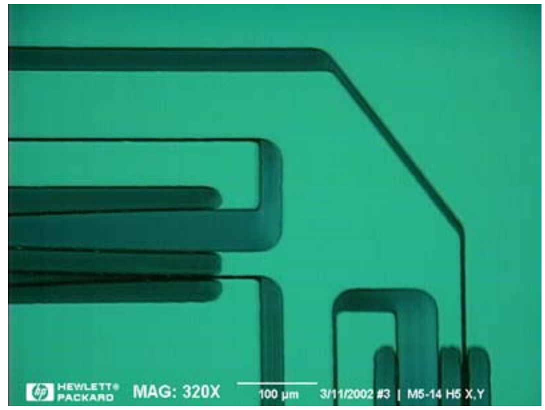


Figure A40. Device H5 at the X and Y max positions.

The "gaps" in the figures are the 25 um wide trench etched to produce the flexures. Flexures are defined by the gap between two adjacent trenches. For device H5, this was 4 um. The figures show device at rest (Figure A37), with full travel in one axis (Figure A38, Figure A39), and with full travel in both directions (Figure A40). Full travel corresponds to the point where the device has crossed the trench, a distance of 25 microns. Given a natural step size of 0.4 um, full travel should occur at 62.5 steps. The device in the figure was moved 61 steps from the home position seen in Figure A37. The device can also move an equal distance in the other two directions, Y min and X min.

A.8. Conclusions

This report has presented a full, static characterization of a working micromover. Device parameters have been extracted for comparison to the design specifications. The effort has included the development of the design, fabrication process, simulation tools, and testing techniques for the micromover. The result is a device that far exceeds the original performance expectations for the project. We have successfully designed, fabricated, and characterized the media translation element necessary to build a MEMS Based Data Storage system.

Analysis of completed micromovers to this point has been limited to static parameters. Left to be done are studies of the micromover dynamics. This is especially important as the micromover will be operated under vacuum in the MBDS system. Further measurement and modeling needs to be done on the dynamics of the micromover, such as quality factor and frequency response, under the true operating environment.

B. CORNELL UNIVERSITY

MICROMOVER PROCESS DEVELOPMENT
NORMAN C. TIEN
SCHOOL OF ELECTRICAL ENGINEERING
CORNELL UNIVERSITY

B.1. INTRODUCTION AND GOALS

In this project, we have developed a fabrication process to realize single-level and multi-level interconnects over bulk micromachined single-crystalline silicon with a high aspect ratio. In the process, oxide-refilled trenched are utilized to isolate movable structures, so that more complicated structures and interconnects can be achieved. Employing the process, a two-dimensional micromover, which can be driven along x-direction and y-direction separately, has been designed and fabricated. We have developed a process to realize double-side (front and back of the silicon layer) interconnection with copper-plated through holes to connect the two sides. Using the through-wafer holes provides another local and/or global interconnection layer, which will be very useful for the proposed data storage system.

The work meets the objectives and milestones of our portion of the micromover program: single level interconnect over silicon springs; through-wafer metallization; double-level metallization over springs; and front and back side metallization of a silicon layer with through-wafer interconnection. The resulting technologies (particularly the etch and metallization developments) have allowed the creation of other MEMS devices that have resulted in many publications that are listed at the end of this report.

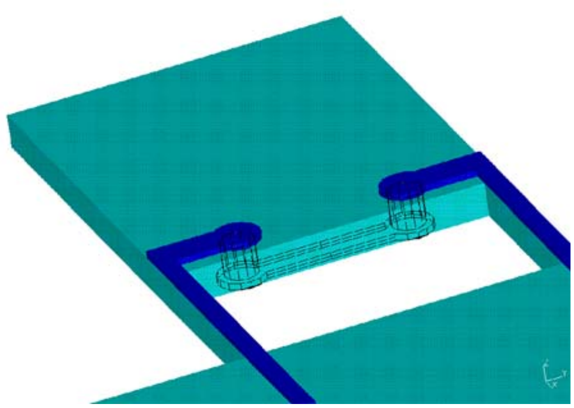


Figure B. The overall objective of this portion of the program is to provide interconnection to the micromover.

Structures utilizing single-crystalline silicon beams have been fabricated using the Bosch deep reactive ion etching (DRIE) process. A process for integrating this etch with Al interconnects has been developed. In this process, SOI (silicon-on-insulator) wafers are used to fabricate microstructures with metal interconnection. This process provides numerous advantages. Namely, Al with thickness of 0.5μm and SiO_2 with thickness 0.3μm are used as interconnection and isolation materials, respectively; and have good electrical performance. Additionally, the Al and oxide layers are very compatible with the standard CMOS process and can correspond directly to the interconnect layers in a CMOS process. Therefore, the microstructures can be fabricated after CMOS fabrication, and it is very easy to integrate the micromover with ICs fabricated in a standard foundry. Interconnects, dielectrics, and microstructures are formed using single mask lithography with self-alignment, and therefore the fine feature size can be achieved without critical alignment. The process can be easily extended to multi-level metal interconnects so that the complex interconnects between movable microstructures and signal-processing circuits can be achieved. The problem of stiction is avoided because no wet release step is used. The capability of DRIE process limits aspect ratio of a trench to be 20:1, but it has no such limitation for a beam. Therefore, though we only demonstrated a beam with the maximum aspect ratio of 10:1 (20μm-thick and 2μm-wide), this process allows much higher aspect ratio such as 40:1.

An oxide-trench-refilling isolation technology has been developed. Using this technology, the movable microstructures can be electrically isolated from the fixed substrate or other microstructures, and therefore complicated MEMS devices can be realized. A novel two-dimensional micromover with the isolation structures, in which two sets of comb drives were used to drive the micromover along x and y-axes separately, has been designed and fabricated. The test structures using two-level Al interconnects have also successfully been fabricated. The measurement results showed that the fabricated structures have high electrical and mechanical performance.

We have developed a process to realize double-side interconnection with copper-plated through-holes. Afterwards, the front-side Cu can be planarized by CMP or an etch-back process to form the through-wafer plug; the Cu on backside can be patterned by a thick-photoresist process to form local or global interconnection. The process can be easily integrated into our process to fabricate the micromover. Using the through-wafer holes provides another local and/or global interconnection layer, which will be very useful for data storage system.

B.2. Process to Fabricate Metal Interconnects on a Single Crystal Silicon Beam

B.2.1. Basic Process

The basic process that allows bi-level metal to be fabricated on top of a bulk micromachined structure is shown in Figure B1. In the figure, only one level metal is shown. It is easy to form the second level metal by repeating the steps for forming the first level.

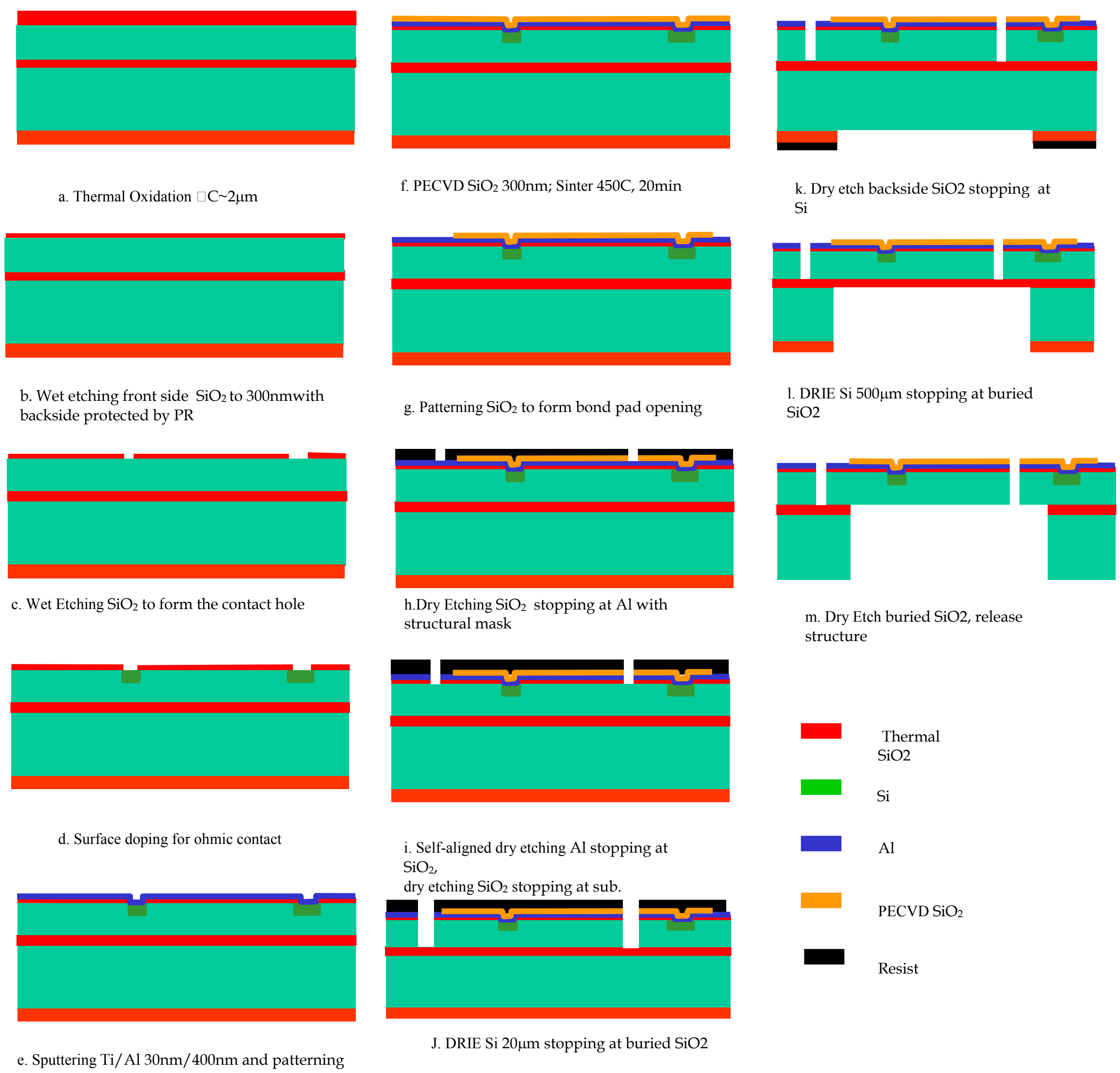


Figure B1 The basic process flow to fabricate metal interconnects on a single crystal silicon beam

In this process, SOI (silicon-on-insulator) wafers are used to fabricate microstructures with metal interconnection. This process provides numerous advantages. Al and SiO_2 used as interconnection and isolation materials, respectively, which have good electrical performance, are very compatible with the standard CMOS process. In fact, the Al and oxide layer can directly use the corresponding layers in CMOS process, and the microstructures can be fabricated after CMOS fabrication. Therefore, it is very easy to integrate the micromover with ICs fabricated in the standard foundry. Interconnects, dielectrics and microstructures are formed using single lithography with self-alignment, so the fine feature size can be achieved without critical alignment. The process can be easily extended to multilevel metal interconnections so that the complex interconnects between movable microstructures and signal-processing circuits can be achieved. Stiction problem is avoided because no wet release step is used.

The experiment began with a 4” SOI wafer with a 20μm lightly doped top layer and 2μm buried oxide layer. The reason to use lightly doped top layer is for integration with IC. The process was partially successful on the first run. A fabricated micromover with Al interconnection before backside etching is shown in Figure B2. The shape of the micromover is similar to a resonator. The double-folded beams are used as springs, and the comb drive is used as the actuator. In the figure, bond pads can be seen clearly. Close-up views of different parts are shown in Figure B3. Figure B3(a) shows a part near the bond pads, Figure B3(b) shows a part of the comb drive, and Figure B3(b) shows a part of the beam. All structures have a sandwich of layers composed by SiO_2/Al/SiO_2 on the SOI top layer. Figure B4 shows a more close-up view of the comb drive, where a little undercut of Al caused by lateral etching can be found..

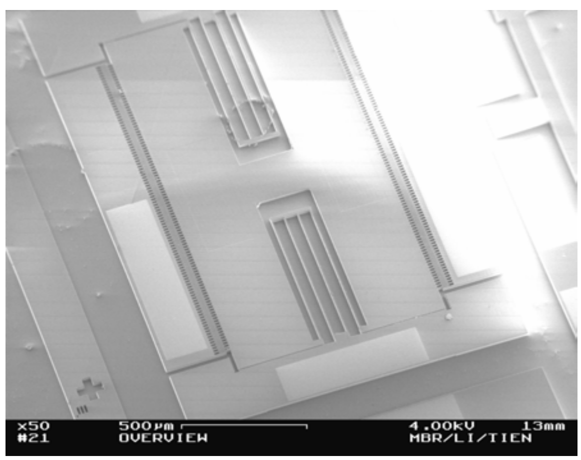
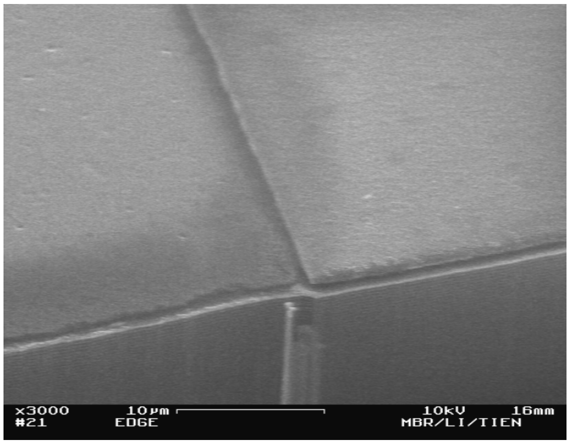
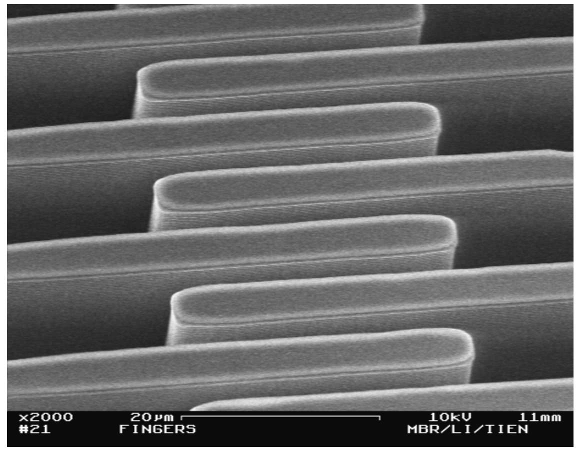


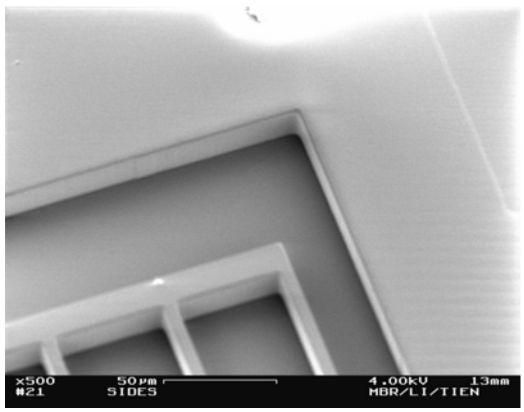
Figure B2 A fabricated mover with Al interconnection before backside etching



(a)



(b)



(C)

Figure B3 Close-up views of different parts. (a) a part near bond pads, (b) a part of the comb drive, and (c) a part of the beam.

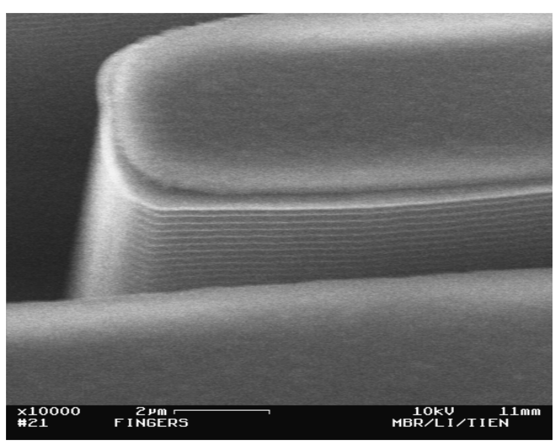


Figure B4 A more close-up view of the comb drive

A two-dimensional micromover before backside etching was designed and fabricated on the wafer (shown in Figure B5). The micromover has double frames, two sets of comb drives and double folded beams. According the design, the micromover can move along x-axis and y-axis by more than 15μm under electrostatic force.

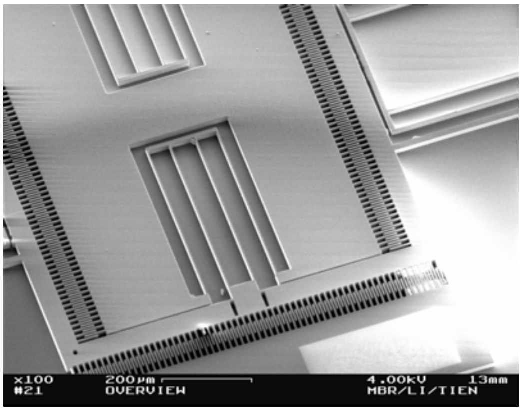


Figure B5 A two-dimensional mover before backside etching

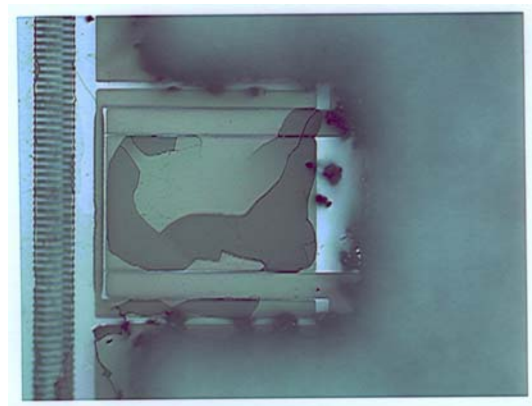


Figure B6 A picture of backside where the buried oxide buckled and broken because of the residue stress.

Unfortunately, however, the basic process has two major problems. . First, the residue stress in buried oxide after backside silicon etching was so high that most structures were broken before HF release. . Figure B6 shows a picture of the backside, where it can be clearly seen that the buried oxide buckled because of the residual stress. The residual stress may come from the process of making the SOI wafer, thermal oxidation and/or wafer bonding. The stress is instinct and very difficult to reduce. To avoid the stress that destroyed the delicate microstructures, the process flow should be improved (shown in Figure B7). In the improved flow, the backside etching will be done before the microstructure information (Figure B7j and k). Then the buried oxide was removed by DRIE (Figure B7l), followed by the microstructure etching (Figure B7m). Because the oxide is removed before microstructures formation, no residual stress problems will damage them. Figure B8 shows the two-dimensional mover after backside etching, in which no damage was found. Secondly, there is no isolation structure between x-direction and y-direction actuator, and therefore the mover cannot be driven along x-direction and y-direction independently.

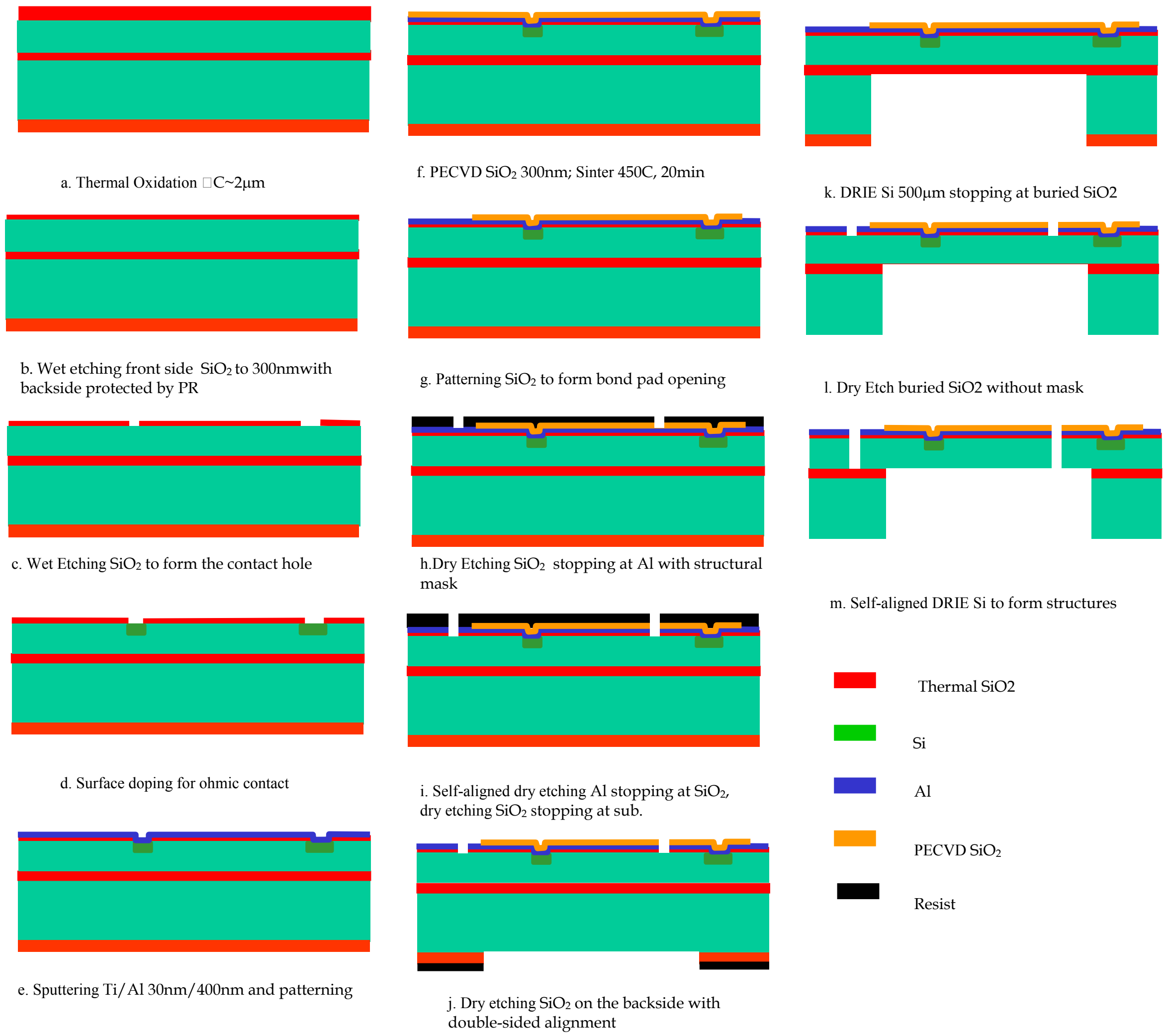


Figure B7 The improved process flow to fabricate metal interconnects on a single crystal silicon beam

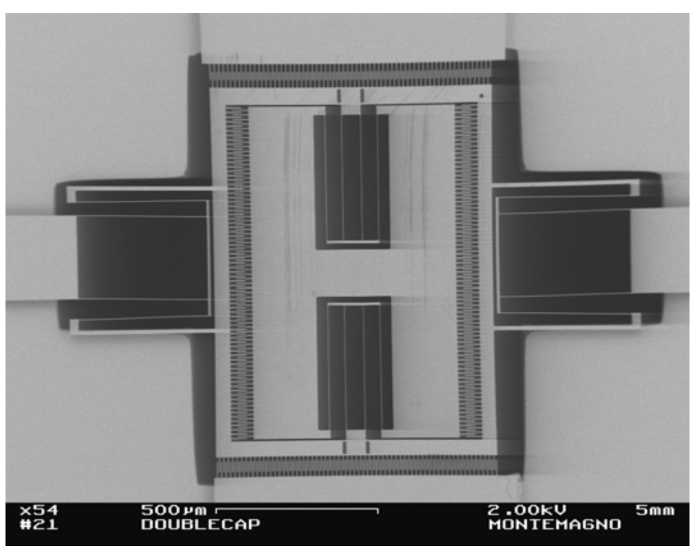


Figure B8 A two-dimensional micromover after backside etching

B.2.2. Improved Process

The improved process flow including isolation structures is shown in Figure B9. The experiment began with a 4” SOI wafer with a 20μm lightly doped top layer and 2μm buried oxide layer. The reason to use a lightly doped top layer is for integration with IC.

Following is the process flow described in further detail:

a) Deep trenches with width of 2μm (some 3μm trenches for test) are etched through the device layer using the buried oxide layer as an etch stop.

b) The trench is filled with LTO (low temperature oxide) of 2.5μm, and then the oxide is planarized from the front side by chemical mechanical polishing (CMP). The trench is overfilled to guarantee the trench is well sealed.

c) Another 0.3μm LTO layer is deposited to be an insulator and seal the probably exposed voids during CMP process. Then the layer is patterned, and then etched away to form the contact areas.

d) Using the thermal oxide as a mask, the contact holes are doped by ion implantation for ohmic contact.

e) 30 nm of Ti then 400 nm of Al are successively deposited by sputtering, patterned and etched.

f) 300 nm of oxide is deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition) and sintered at 450C for 20 minutes.

g) The oxide layer is photolithographically patterned and dry etched to form the bond pad.

h) The oxide is dry etched using the structural mask with the metal layer as an etch stop.

i) The metal is dry etched in a self-aligned fashion with oxide as an etch stop, then the oxide is dry etched in a self-aligned fashion with the substrate as an etch stop.

j) The thermal oxide on the backside is patterned using double-side alignment and etched through to the substrate by

k) DRIE (deep reactive ion etch) of Si from the backside to the buried oxide layer.

l) Dry self-aligned etch through the buried oxide layer with the device layer Si as an etch stop.

m) Self-aligned DRIE of front side Si to form the structures.

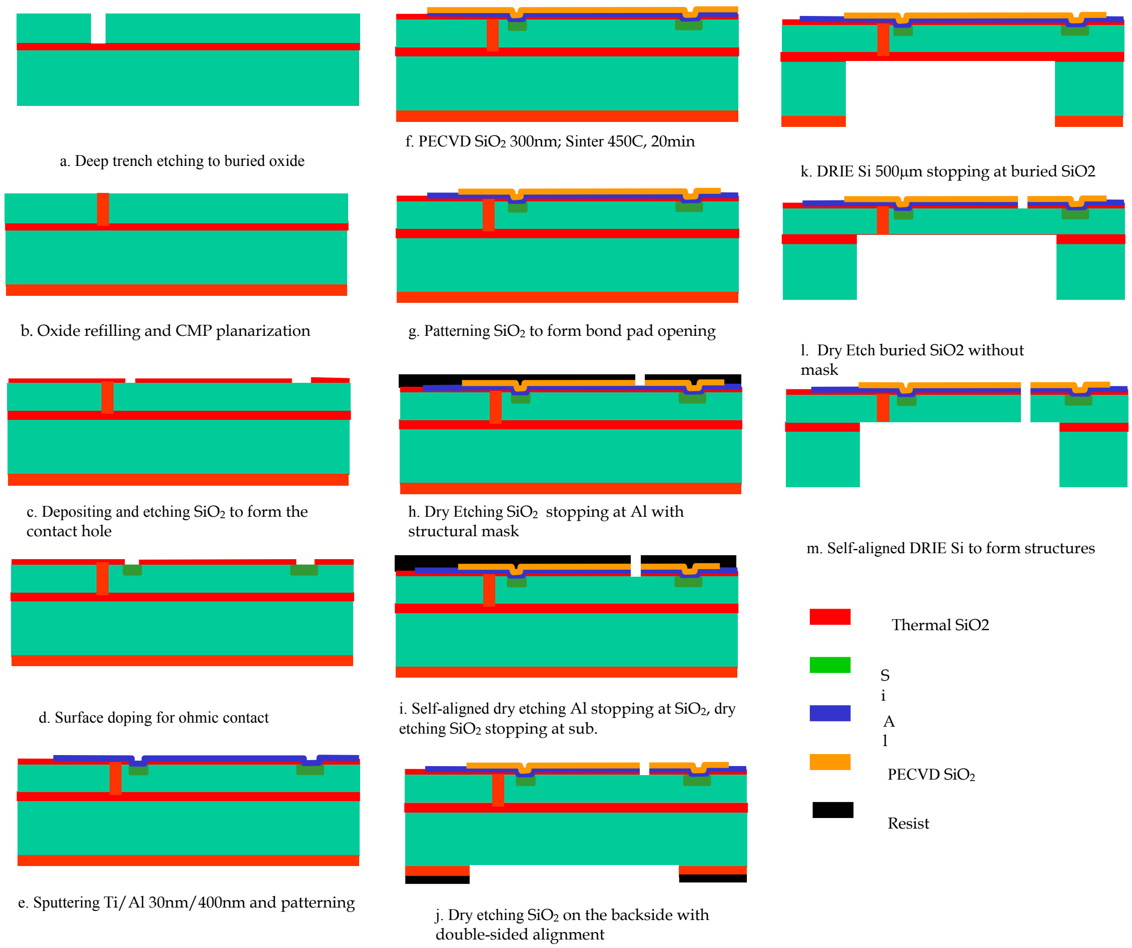


Figure B9 The improved process flow to fabricate metal interconnects on a single crystal silicon beam with isolation structures

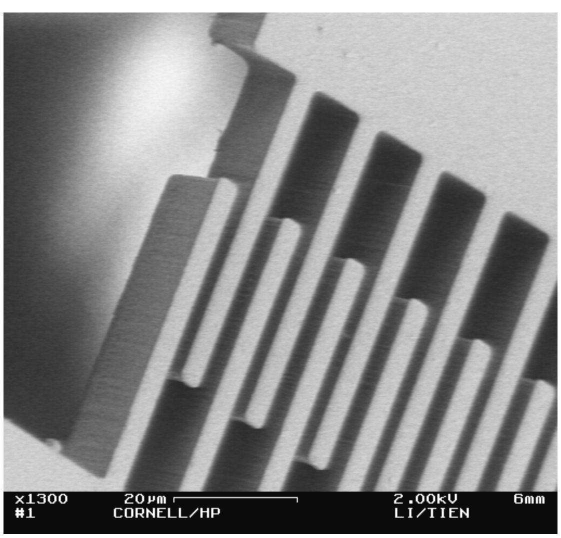


Figure. B10 A SEM photo of a fabricated structure with Al interconnection

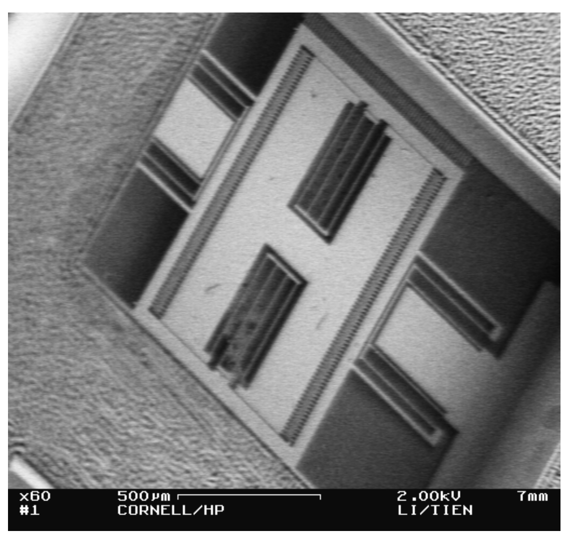
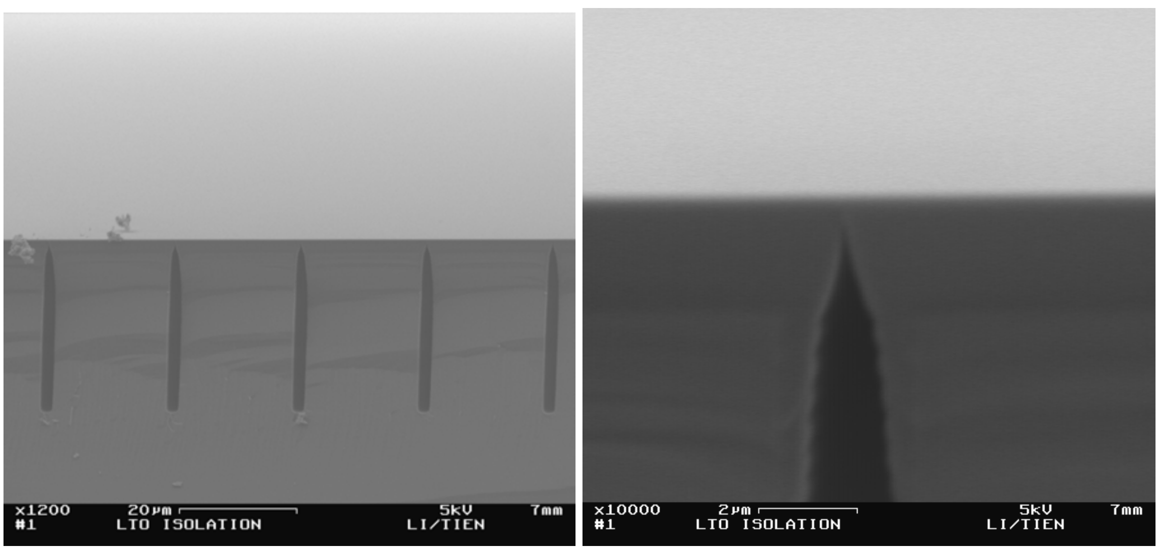


Figure B11 A SEM photo of the backside of a fabricated device

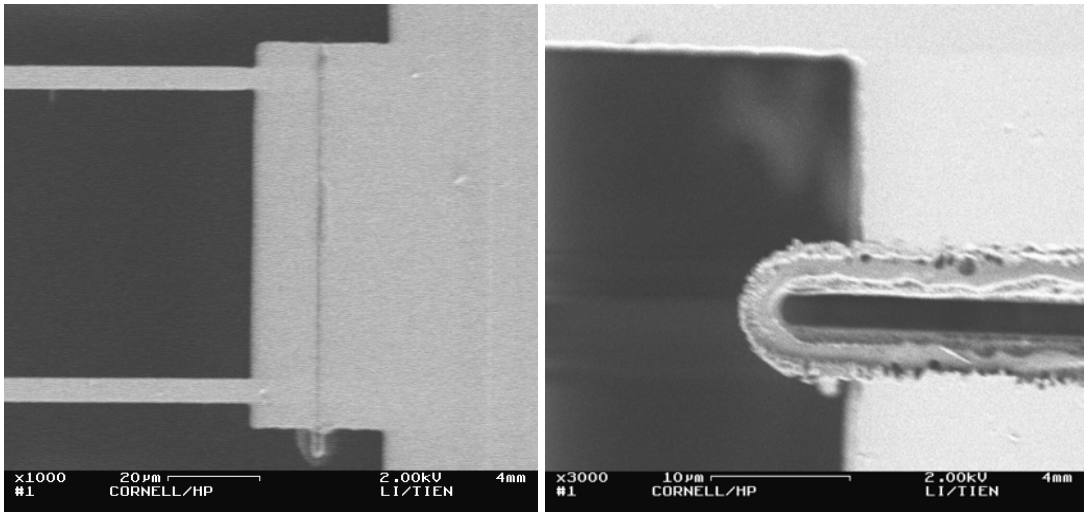
The process was successfully finished. A fabricated structure with Al interconnection is shown in Figure B10, while Figure B11 shows a SEM of the backside of the chip. The feature size is 3μm, and the aspect ratio is approximately 7:1. The aspect ratio can be more than 20:1 according to the process capacity.

Figure B12a shows a refilled isolation trenches array after CMP planarization as test structures, while Figure B12b is part of a trench at a higher magnification. It can be seen that there is a void in the isolation structure, because the LTO (low temperature oxide), which is used to refill the trenches, has poor conformality. If LPCVD TEOS (Low Pressure Chemical Vapor Deposition $Si(OC_2H_5)_4$) is used, the voids will be eliminated or, at least become much smaller. In fact, the voids are not a big problem for our application. It can be seen that the trenches are well sealed with a planarized surface, which is most important. Therefore, the Al lines can cross the isolation structures without discontinuities, and the microstructures can tightly connected. Figure B13a shows a front view of the isolation structure with Al crossing it. Figure B13b shows a backside view of the isolation structure. The oxide used as an isolation layer is etched a little bit and the void is exposed during the buried oxide removal.



a b

Figure B12 (a) The filled isolation trenches array after CMP planarization as test structures, and (b) a part of a trench at a higher magnification. A void can be seen in the trench, but it is well sealed on the surface.



(a) (b)

Figure B13 (a) A front view of the isolation structure with Al crossing it, and (b) a backside view of the isolation structure.

We studied on the performance of the isolation structure in details. Figure B14 shows a typical test structure. The beams with widths of 2μm, 3μm and 4μm, respectively, were crossed by a series of oxide isolation bars. An aluminum line went over the beam with an oxide layer under it. In hundreds of test structures, no broken or buckling was found, which means the isolation structure has good mechanical performance. However, there were more requirements for the structure. For a good structure, the aluminum line should have good interconnection, and the silicon substrate should be well isolated. Some failure mechanisms are found in the structure, which show in Figure B15. The worst case occurred at the most right oxide bar in Figure B15, where aluminum line was discontinuous. The failure was caused by the void in the oxide bar, which was created by bad conformality of LTO (low temperature oxide) and exposed in CMP (chemical mechanical polishing) process. If the surface of the isolation trenches is well sealed (shown in Figure B12b), no such failure occurs. It can be controlled by optimizing the geometry of trenches and process conditions, or using LPCVD TEOS to fill the trenches.

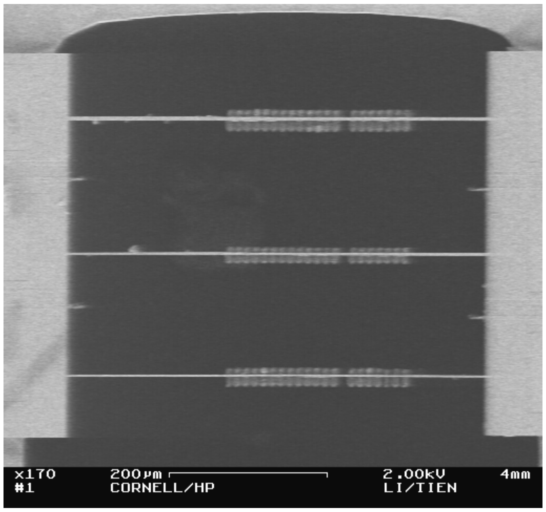


Figure B14 Structures to characterize the performance of isolation structures. Widths of beams are 2µm, 3µm and 4µm from bottom to top.

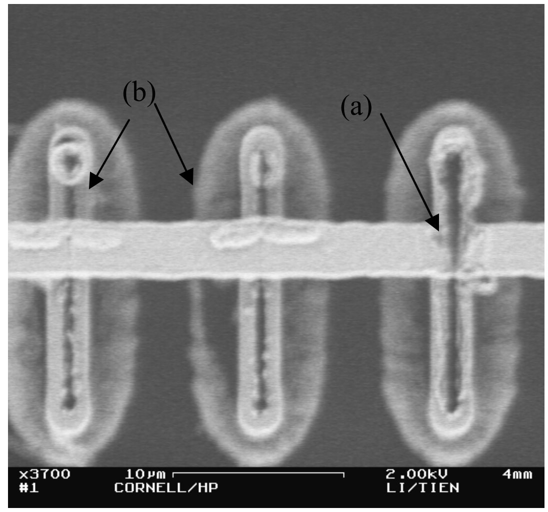


Figure B15 Two failure mechanisms of isolation structures. (a) Al discontinuity caused by void in oxide bar, and (b) Silicon ring

Figure B16 shows I-V curves for aluminum lines over beams with and without isolation structures. It can be seen that the isolation structures do not result in a significant resistance change, as long as the surface of isolation structure is well sealed and planarized. In the figure, the resistance of the aluminum line over beams with oxide bars is even smaller, which may be caused by process variation.

Figure B15 also shows an interesting phenomenon, which is another failure mechanism. After silicon beams were etched through, even with a little bit overetch, silicon around an oxide bar was still not etched completely, and a "silicon ring" was formed. The reason is probably that the silicon bar is charged by plasma during DRIE, and the etched rate is reduced. The silicon ring formed an unexpected conductive path and degraded isolation performance. The measured resistances of a silicon beam with silicon rings were several to tens mega ohms, which depends on overetch time (Figure B17). Silicon rings can be removed by extra overetch, which may increase lateral etch and the "footing effect". Fortunately, the lateral etch is ignorable in the DRIE process, and the footing effect is not severe in our process, because the backside silicon and buried oxide are etched before structures etch. Figure B13b shows a backside view of the isolation structure after silicon rings were removed. The measured resistance of a silicon beam without silicon rings was beyond our measurement capability, $10^{10}\Omega$ (Figure B17).

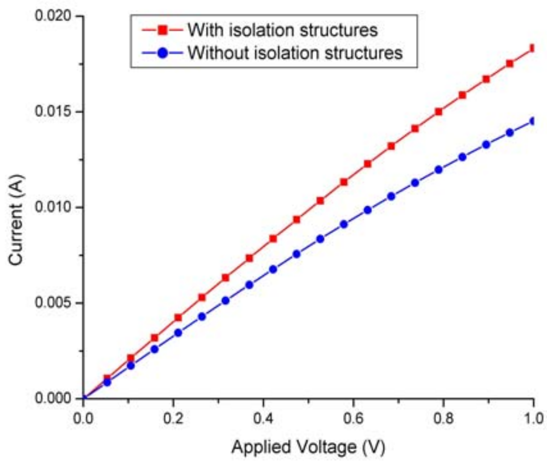


Figure B16 I-V curves for aluminum lines over beams with and without isolation structures

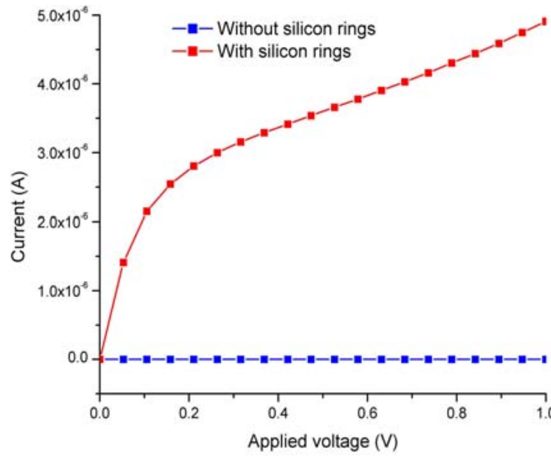


Figure B17 The measured resistances of silicon beams with isolation structures before and after silicon rings are removed

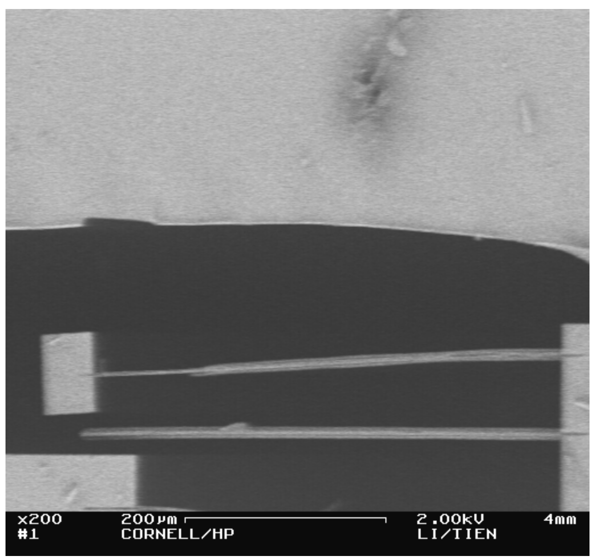


Figure B18 Long oxide bars (400µm) with and without silicon proof mass attached to the tip.

Figure B18 shows long oxide bars (400µm) with and without silicon proof mass attached to the tip. The result shows that oxide bars have potential to be mechanical beams. This topic was beyond the object and was not studied in details.

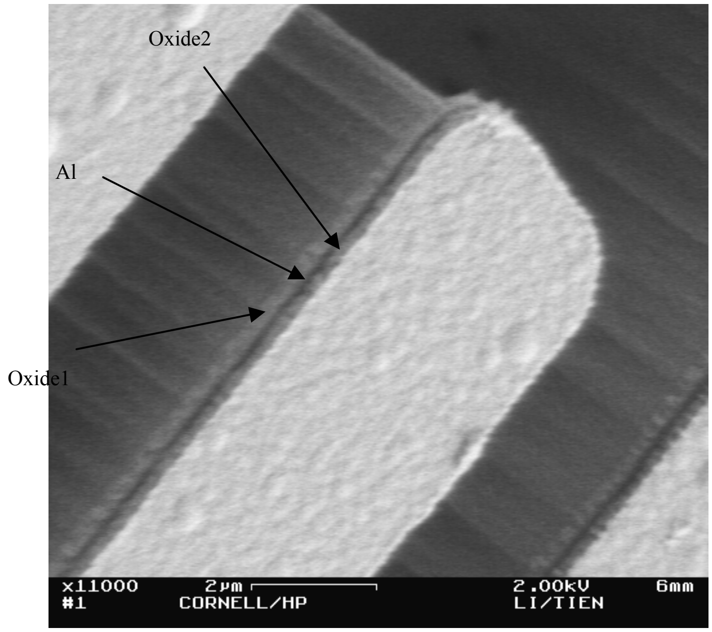
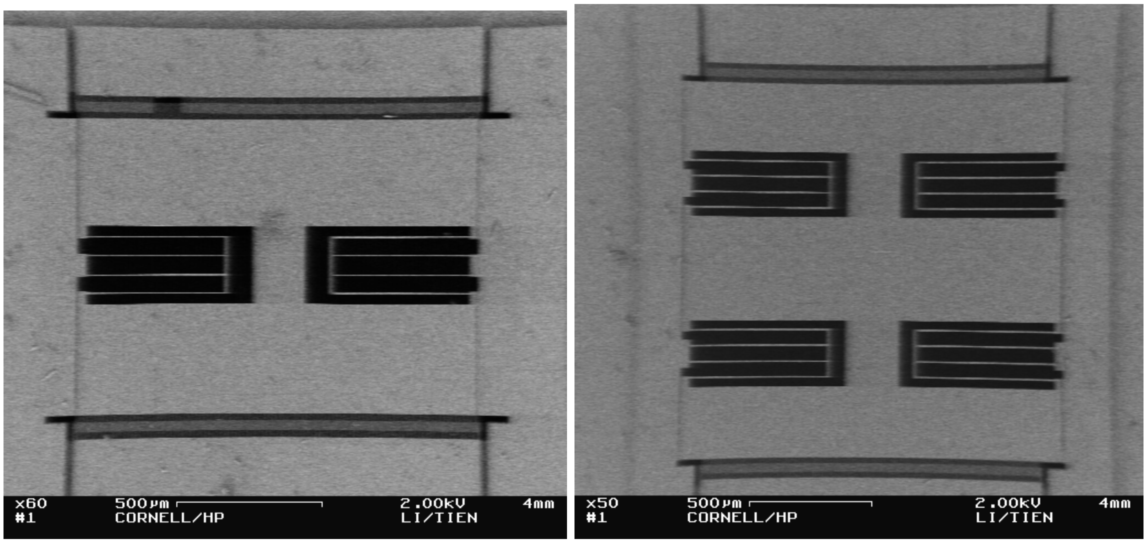


Figure B19 A SEM photo The oxide-Al-oxide sandwich structures used as interconnects over the movable structures. A little undercut of Al caused by lateral etching can be found.

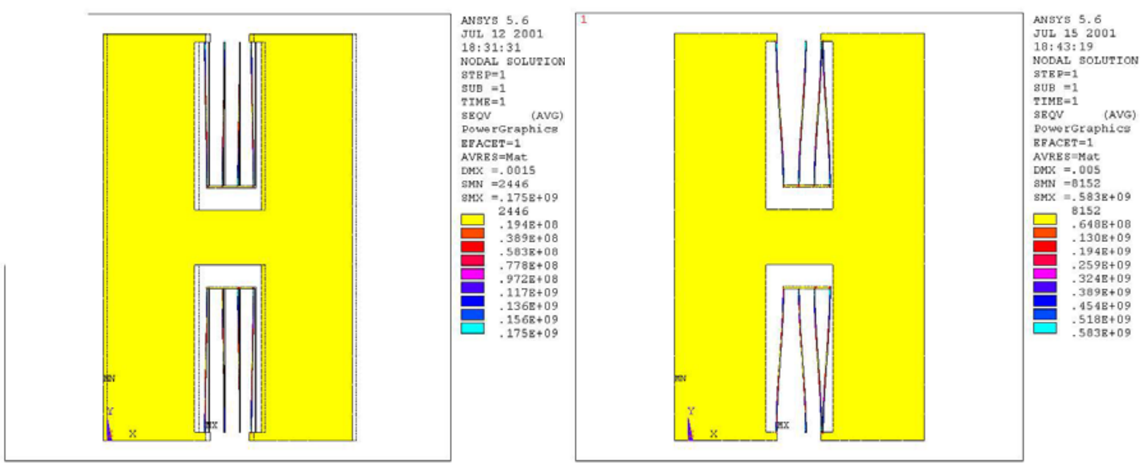
The oxide-Al-oxide sandwich structures used as interconnects over the movable structures are shown in Figure B19, where a little undercut of Al caused by lateral etching can be found. We utilized two types of resonators to test the performance of the Al interconnects (shown in Figure B20). The Al lines went over the springs of the resonator. Both resonators were electrically driven at their resonant frequency with amplitude of about 15µm. After continuous operation for 72 hours, no changes of resonant frequency or resistance were found, which gives indication that no fatigue or unrecoverable deformation occurred. This result shows that the interconnect structures have high electrical and mechanical reliability. We used ANSYS, a FEM software, to analyze the structure. Figure B20a shows stress distribution of Al line on the resonator with a displacement of 15µm. The maximum stress locating at the base of the spring was 17.5Gpa, about one tenth of the yield strength of Al, 170GPa. Figure B20b show shows stress distribution of Al line on the resonator with a displacement of 50µm. The maximum stress located at the base of the spring was 58.3GPa, still about one third of the yield strength of Al.



(a) (b)

Figure B20 Two types of resonators to test the performance of the Al interconnects. (a) With one set of folded springs, and (b) With two sets of folded springs.

The interconnection structures with two-level Al layers were also fabricated. A SEM photo a beam is shown in Figure B21. The beam was oxide (500nm)/Al (300nm)/oxide (300nm)/Al (300nm)/oxide (300nm)/Si with self-align fashion. The process for two-level Al has no essential difference from the one for one-level Al, except one more layer of oxide and Al is deposited and patterned. Therefore, we only fabricated the structures on the silicon wafer instead of a SOI wafer, and no detailed performance characteristics were obtained.



(a) (b)

Figure B21 Using ANSYS, the simulated stress distribution of Al line on the resonator. (a) With a displacement of 15μm, and the maximum stress is 17.5Gpa. (b) With a displacement of 50μm, and the maximum stress is 58.3Gpa.

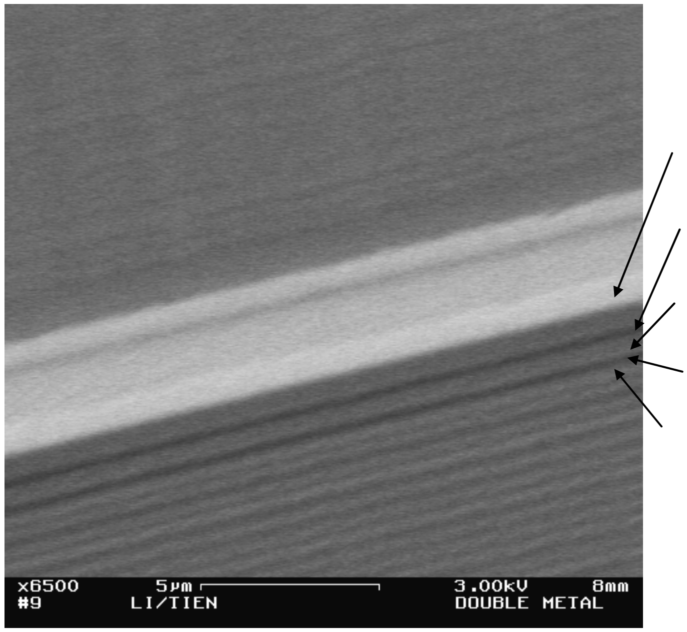


Figure B22 A SEM photo of a fabricated beam using the interconnection structures with two-level Al layers, oxide (500nm)/Al (300nm)/oxide (300nm)/Al (300nm)/oxide (300nm)/Si structure.

The interconnection structures with two-level Al layers were also fabricated. A SEM photo a beam is shown in Figure B22. The beam is oxide (500nm)/Al (300nm)/oxide (300nm)/Al (300nm)/oxide (300nm)/Si with self-align fashion. The process for two-level Al has no essential difference from the one for one-level Al, except one more layer oxide and Al is deposited and patterned. Therefore, we only fabricated the structures on the silicon wafer instead of a SOI wafer. Using the similar method, multi-level interconnection over beams can be realized.

B.2.3. Two-Dimensional Micromover

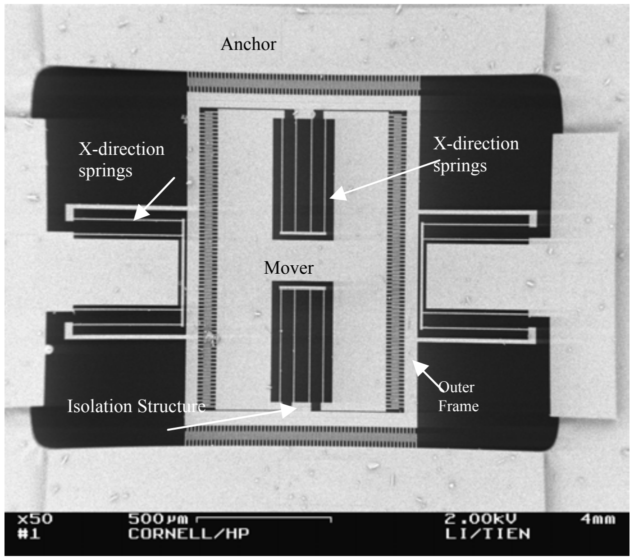
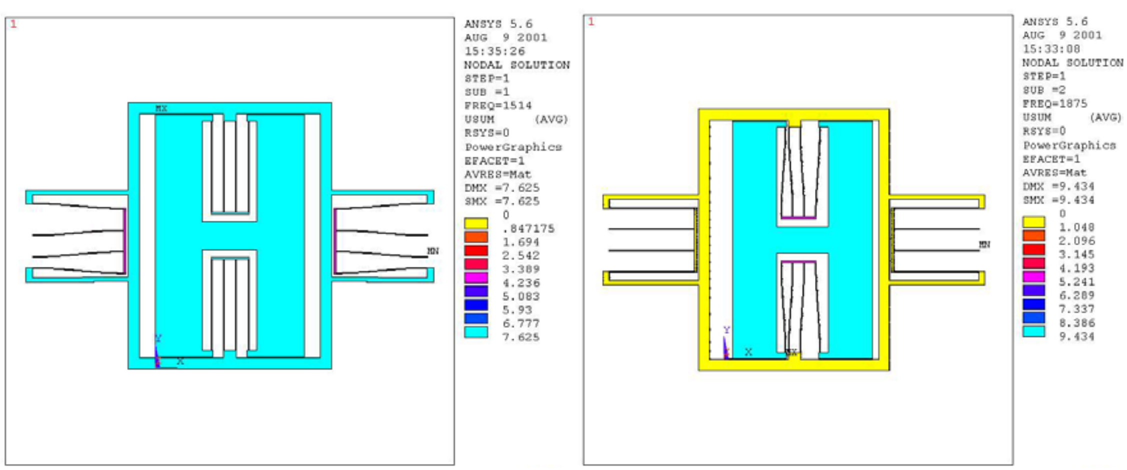
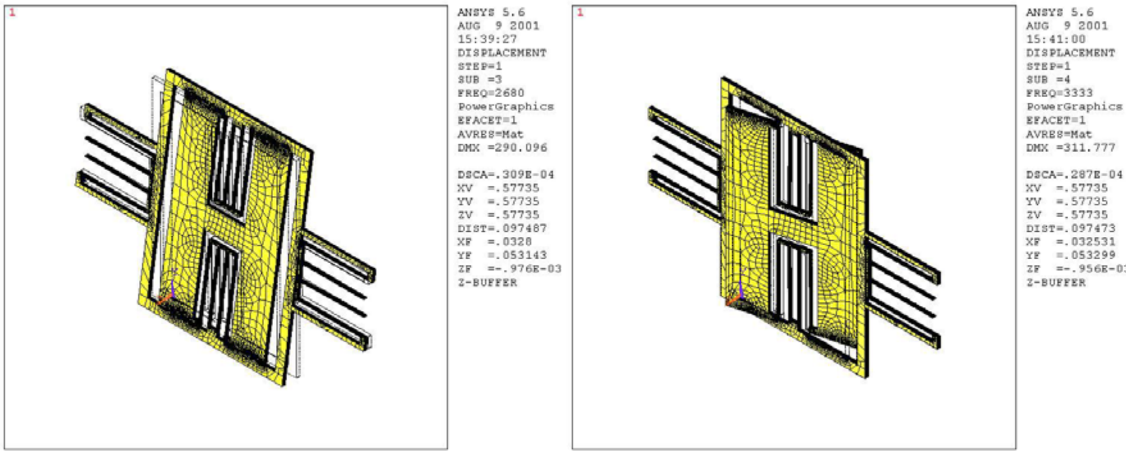


Figure B23 The SEM photo a two-dimensional micromover using the isolation structures

With the isolation structures and interconnection over beams, we have designed and fabricated a two-dimensional micromover. The SEM photo is shown in Figure B23, and the backside view is already shown in Figure B11. The comb drives were employed to drive the micromover, and double folded springs suspend it. Therefore, the micromover has a wide range of displacement. More importantly, the micromover could be controlled in *x* and *y*-directions independently because of the isolation structure and Al interconnection over the springs. The Al lines can be also used to interconnect the devices on the micromover, which are most important for the data storage microsystem.



(a) (b)



(c) (d)

Figure B24 The first four modes of the 2-dimentional micromover simulated by ANSYS. The resonant frequencies are 1514Hz, 1875Hz, 2680Hz and 3333Hz, respectively.

Figure B24 shows the first four modes of the two-dimensional micromover simulated by ANSYS. The resonance at the first mode is along x-axis, and the frequency is 1514Hz (Figure B24a); the resonance at the second mode is along y-axis, and the frequency is 1875Hz(Figure B24b). The resonant frequency along the y-axis is higher than along the x-axis is because the frame does not move at the second mode, and the mass is less, though the stiffness of springs along x-axis and y-axis are designed to be the same. The comb drives for the x and y-axes are also the same, and, therefore, the displacement will be same at the same driving voltage. Because a misalignment (about 2μm off the tolerance, shown in Figure B11a) in the process occurred, the oxide-filled trench structure does not isolate the micromover in the two directions. The isolation resistance is about 1MΩ, which comes from the low doped top silicon layer which is not been isolated due to the misalignment. However, the fabricated device can still be driven at both at x-axis and y-axis, and the measured frequencies at the two modes are 1613Hz and 2002 Hz, respectively.

The test of the reliability of the Al interconnects were also done for the two-dimensional micromover, and the same results were obtained: no changes of resonant frequency or resistance were found after continuous operation at resonant frequency with 15μm amplitude for 72 hours.

B.3. PROCESS TO REALIZE THROUGH-HOLE INTERCONNECTS

The process flow is shown in Figure B25. For compatibility with our micromover process, the experiment also begins with a 4" SOI wafer with a 20μm lightly doped top layer and 2μm buried oxide layer.

Following is the process flow described in further detail:

A. Grow 0.1 μm thermal SiO_2 and deposit 0.2μm LPCVD Si_3N_4 on both sides as hard mask during KOH etching.
B. Pattern and etch backside SiO_2 and Si_3N_4; etch Si with KOH stopping at buried SiO_2 with front side protected by SiO_2 and Si_3N_4
C. Etch buried SiO_2 under the membrane with RIE
D. Pattern front side, RIE SiO_2 and Si_3N_4 to form hard mask, DRIE top-layer silicon to form the through holes, and remove SiO_2 and Si_3N_4
E. Grow 0.3μm thermal oxide for an isolation layer
F. Sputter 100Å Ti/2000Å Cu as seed layer on the front side

G. Sputter 100Å Ti/2000Å Cu as seed layer on the backside
H. Electroplating Cu to refill the holes copper with Technic™ solution, under current density of 12.5mA/cm^2 at room temperature.

After that, the front-side Cu can be planarized by CMP or etch-back process to form through-wafer plug; the Cu on backside can be patterned by a thick-photoresist process to form local or global interconnection. The process can be easily integrated into our process to fabricate the micromover.

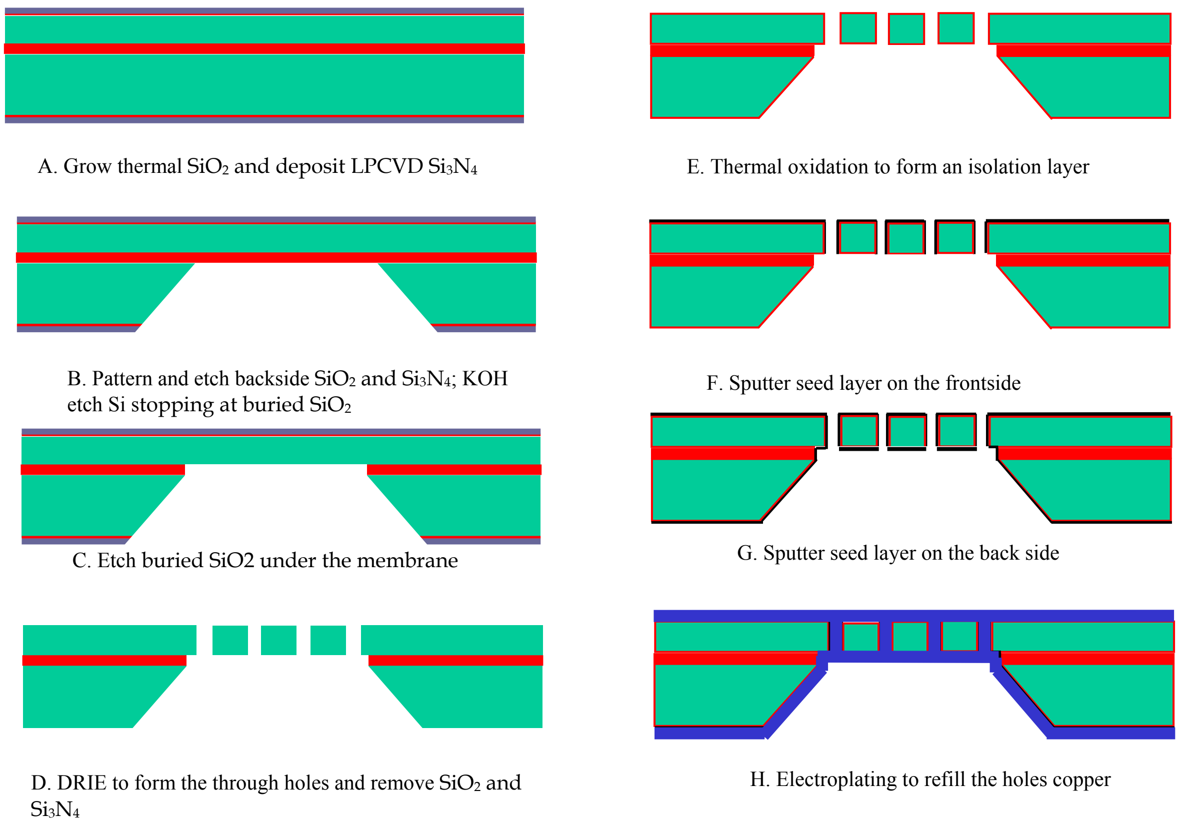
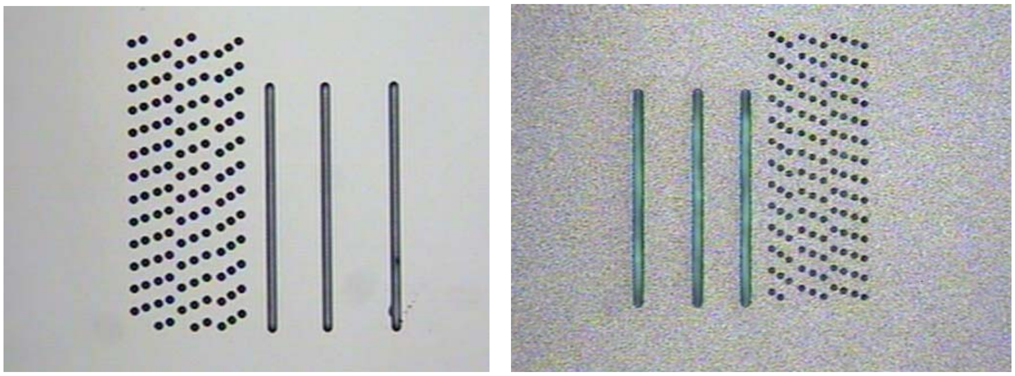


Figure B25 The process flow to fabricate double side metal

Figure B26a and Figure B26b show micrographs of testing structures on front side and backside before copper plating, respectively. Both diameter of holes and width of trenches are 5µm. Figure B27a and Figure B27b show micrographs of testing structures on front side and backside after copper plating, respectively. It can be seen both holes and trenches are sealed on both sides.

Figure B28 shows cross-sectional SEM picture of a filled hole with a flat surface. Figure B29 shows a plug that is broken during sample preparing. It can be seen that a little void is in the plug, which is formed during copper plating. The void will not increase series resistance or degrade the reliability of though-hole plug significantly, since it is very small compare to the diameter of the hole.

Figure B30a shows a well-filled though-hole plug interconnecting the top metal layer and the bottom metal layer, while Figure B30b is a close-up view. The silicon structure layer is constructed by the top layer of the SOI wafer. The top metal layer, bottom metal layer and plug are formed by electroplating simultaneously.



a b

Figure B26 Micrographs of testing structures on front side (a) and backside (b) before copper plating.

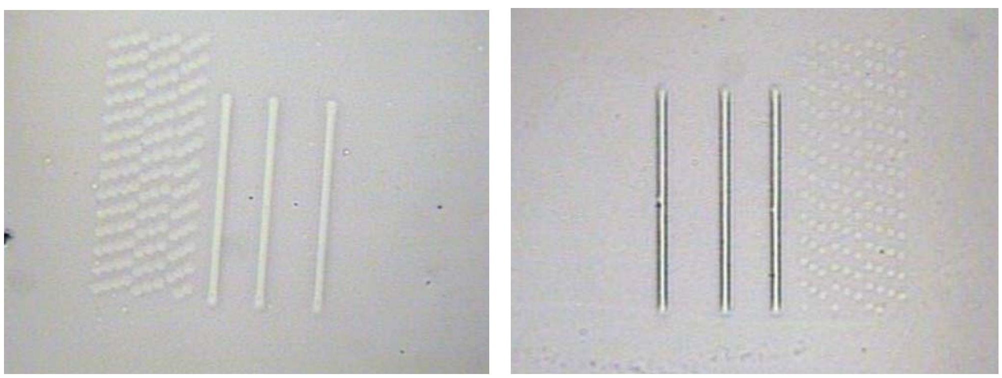


Figure B27 Micrographs of testing structures on front side (a) and backside (b) after copper plating.

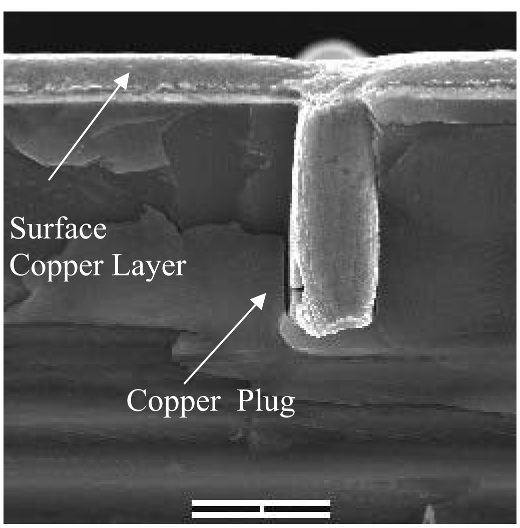


Figure B28 Cross-sectional SEM picture of a filled hole with a flat surface

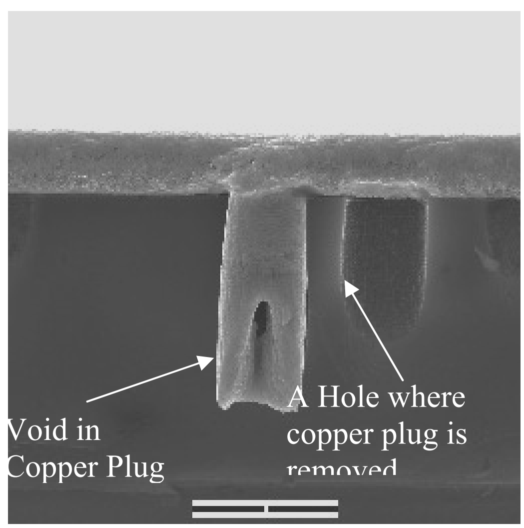


Figure B29 A plug that is broken during sample preparing

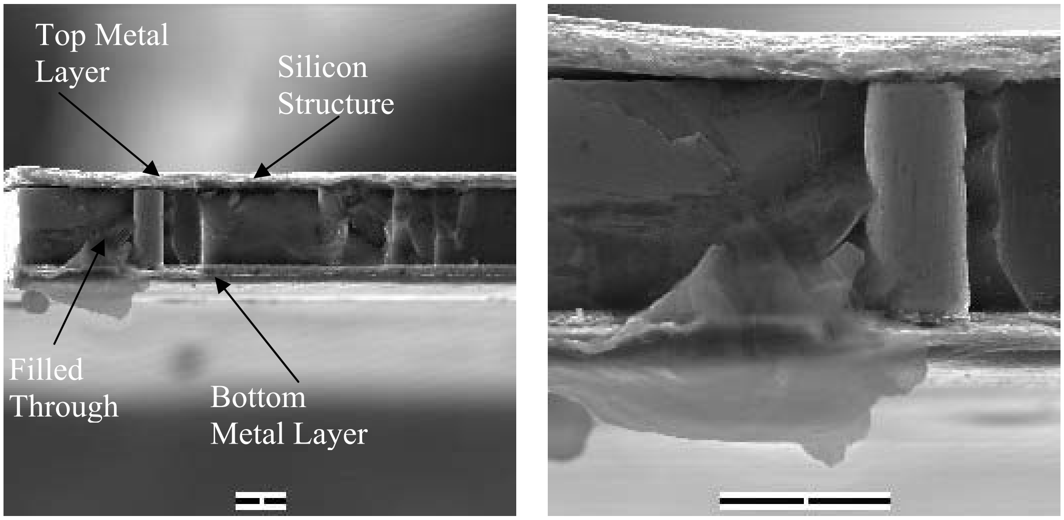


Figure B30 (a) A well-filled though-hole plug interconnecting the top metal layer and the bottom metal layer. (b) A close-up view

B.4. CONCLUSION:

The objective of this portion of the project was to develop interconnection technologies for the micromover. Single and double-level interconnects over thick silicon springs have been developed. Initial reliability tests indicate that these interconnects are electrically and mechanically stable and robust over periods of spring flexing. Through-wafer interconnects were also developed and this is a means in which front and backside metallization can be connected and this was demonstrated. In addition, the resulting technologies such as the etch techniques, the oxide block formations, the metallizations (electroplating) have also been able to allow the creation of other new MEMS devices.

B.5. BIBLIOGRAPHY:

"Integrated polysilicon and DRIE bulk silicon micromachining for an electrostatic torsional actuator," J.-L. A. Yeh, H. Jiang, and N. C. Tien, Journal of Microelectromechanical Systems, vol. 8, no. 4, pp. 456-465, 1999.

"Copper-encapsulated silicon micromachined structures," J.-L. A. Yeh, J. Chen, H. Neves and N. C. Tien, Journal of Microelectromechanical Systems, vol. 9, no. 3, pp. 281 - 287, 2000.

"Fabrication of high-performance on-chip suspended spiral inductors by micromachining and electroless copper plating," IEEE International Microwave Symposium Digest, Boston, pp. 279-281, 2000.

"Fabrication of a high-performance on-chip copper-encapsulated silicon inductor suspended over a cavity," H. Jiang, Y. Wang, J.-L. A. Yeh, and N. C. Tien, IEEE Transactions on Microwave Theory and Techniques, vol. 48, no. 12, pp. 2415 – 2423, 2000.

"A universal MEMS fabrication process for high-performance on-chip RF passive components and circuits ", H. Jiang, B. A. Minch, Y. Wang, J.-L. A. Yeh and N. C. Tien, Solid-State Sensor and Actuator Workshop Technical Digest, Hilton Head, SC, pp. 250-254, 2000.

"Fabrication of thick silicon-dioxide sacrificial and isolation blocks in a silicon substrate," H. Jiang, J.-L. A. Yeh, K. Yoo, and N.C. Tien, Journal of Micromechanics and Microengineering, 2001.

C. UNIVERSITY OF CALIFORNIA AT DAVIS

SUBTRACTIVE FIELD-EMISSION TIP DEVELOPMENT

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C.1. INTRODUCTION

C.1.1. Previous work at UCD (background)

The investigation into silicon field emission sources was begun by this research group at UCD in 1989 with a study in the formation of field emission points using single crystal silicon. We have shown that points potentially useful for field emission sources could be fabricated using both isotropic and anisotropic wet chemical etchants. [1]

The anisotropic etchant used in our studies is potassium hydroxide (KOH), mixed with various types of alcohols. These etchants provide a method of forming sharp points with different base to height aspect ratios, depending on the type of alcohol added to the solution. The etching is uniform over a large area of the 4 inch wafer. However, the resulting points were somewhat dull and the slope of the point is limited to, at best, the 45° angle of the exposed {331} crystal planes to the {100} wafer surface.

The isotropic etching is done with a mixture of hydrofluoric, nitric, and acetic acids (3:25:10, standard reagents by volume). This etchant produces much sharper points with steeper slopes. Both of these features are extremely important in obtaining field emission. The major challenge in fabrication of these points are the nonuniformity of the etching over the surface of a sample. It is difficult to fabricate large arrays of points with any reliability. Work on solving this problem is progressing.

The sharpness of the acid etched tips inspired an investigation into methods of tip sharpening using thermal oxidation. Silicon tips fabricated at Lawrence Livermore National Laboratory in collaboration with UC Davis were thermally oxidized under conditions known to be optimal for the formation of sharp corners in silicon. This method of sharpening produced silicon tips having points of atomic dimensions. The method was developed at Bellcore, in collaboration with the New Jersey Institute of Technology, Lawrence Livermore National Laboratory, and this research group at UC Davis.[2]

Having fabricated suitable field emission cathodes, current-voltage measurements were made. Field emission currents have been measured from sharpened and non-sharpened points formed with both types of etchants. Currents from diodes have been shown to be as high as 0.2 μA/tip at voltages as low as 10 V when a cathode to anode spacing of about 0.9 μm is used. It has been shown that this current is field emission current by measuring the temperaure stability of the devices. Stable, temperature independant currents have been measured over a wide range of temperatures.[3]

Fabrication of triode structures consisting of single crystal silicon emitters and either a polysilicon or chrome gate were successfully performed. The polysilicon gated structure were made using the etched gate technique described below. An SEM of this device is shown in Figure C1.

Preliminary tests have been done on-+ both types of triodes. These tests have shown that the sloped gate of the etch-gate structure, Figure C1, produces unwanted gate emission, particularly if the anode-gate spacing is small. This field emission current measured from the gate has lead to an interest in the development of polysilicon emitter points. Some encouraging, preliminary results have been obtained from the lift-off structure. The primary triode fabrication method used in this research will be the lift-off devices due to their self-alignment and relative ease of fabrication.

C.1.2. Need for these tasks

The subtractive tip fabrication process is divided into the following fabrication tasks; 1) SOI based tips, 2) metal etch stop tips and 3) tips with focusing surfaces.

Although, polysilicon field emitters offer flexibility in substrate type and size, single crystalline devices are needed as a standard for baseline measurement of specific surface orientation tips.

The metal etch stop in the singly addressable tip arrays provides a better tip fabrication control for the resistor structure and high tip geometry uniformity across the 4 inch wafer. A novel advantage of metal etch stop is the graphoepitaxy; a process which determines a specific surface orientation using polysilicon deposition method of tip material. Graphoepitaxy uses artificial surface relief structures to induce crystallographic orientation in thin films. It predicts that materials that can be deposited on smooth amorphous substrates to produce a crystalline texture can be uniformly oriented by appropriate surface relief structures. Uniformly oriented silicon films of 0.5 μm thickness over surface relief gratings etched into amorphous fused silica substrates have been achieved by graphoepitaxy. The silicon may first be deposited as an amorphous film and then crystallized using a scanned Ar laser beam. The [100] directions in silicon are orthogonal to substrate plane and parallel to the grating. Furthermore, uniformly doped (phosphorous ; $2.4x10^{17}$ atoms/cm^3) films have an electron mobility of at least 40% of the bulk value. [4,]

A detailed description of the fabrication process for singly addressable tip arrays is provided below.

The electron beam divergence of an activated tip may provide an unacceptable spot size or resolution for potential applications. The most practical approach to limit the beam divergence is to fabricate focusing surfaces on or around the field emitter tip. There are two possibilities; aperture-focused (Figure C2b) or concentric focus (in-plane) tips (Figure C2a). Both of these approaches supplement the gated top (proximity-focused) with a focus electrode. The aperture focused approach allows higher anode voltages at the expense of larger gate capacitance and higher drive voltage than the concentric focus tips. In terms of fabrication, for concentric focus, a lateral second gate (concentric with the first gate) can be placed at the same level on the gate mask without any complications. However, the aperture-focused tips requires a more complicated fabrication process. The second gate may be added by depositing another dielectric and metal layer to the already lifted-off layers. The second gate will then have to be manually aligned with great precision to the first gate and is no longer self-aligned like the first gate.

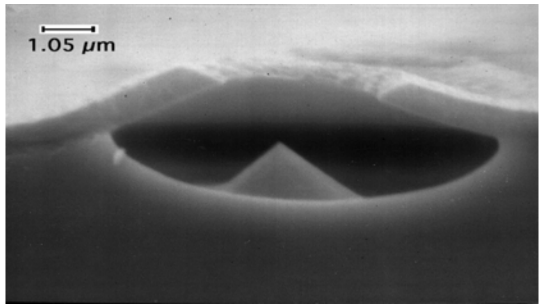


Figure C1 An etched gate device consisting of a single crystal silicon emitter tip, a SiO_2 dielectric layer, and a polysilicon gate.

C.2. SPECIFIC DESCRIPTION OF PROPOSED TASKS

C.2.1. Singly addressable tip array fabrication

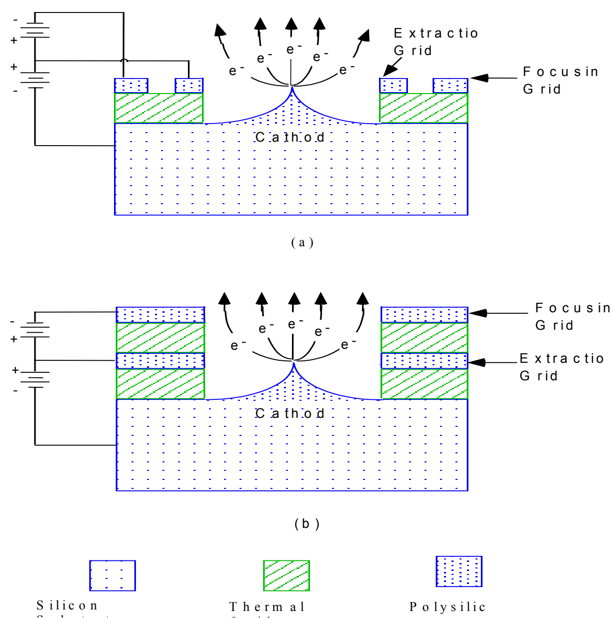


Figure C2: a) concentric focus gate. b) aperture focus gate

The research is built upon prior experimental work in this area at UC Davis. Design, fabrication, and measurement tasks investigate novel cathode architectures, specifically using single tip addressable arrays of field emission cathodes. The objectives are to improve the uniformity in fabricated cathodes, maximize gain in single emitter triode devices, lower cost and improve manufacturability, and minimize noise. In investigating single cathodes, rather than arrays of cathodes, the focus is on the surface physics of the emission process through our measurements; the intent is to asses the inherent statistical variability between physically similar emitting cathodes and thereby make projections concerning the applicability of these devices to specific products.

C.2.2. Process description

The fabrication process requires a silicon/oxide/silicon structure consisting of a silicon substrate with at least 1 µm of oxide and 3 µm of polycrystalline silicon. The dopant concentrations of the silicon thin film will depend on it's thickness. The specified resistors are to have a 1Meg/□ resistivity when the process is complete.

The wafers are then oxidized forming a 100 nm oxide on the silicon film. This is then coated with Chromium to provide an etch mask. Mask #1, the tip electrode mask is patterned and the tip electrodes are etched using a vertical RIE etch. Then Mask #2, the tip mask is patterned. This mask exposes the resistor and tip portion of the tip electrodes, leaving a 1µm (diameter) tip cap where the tip is to be formed. The polysilicon is etched again, this time using an isotropic RIE etch. The tip etch continues until just before the 1 um diameter cap falls off. The Chromium layer is then stripped, the wafers are cleaned (RCA) and are oxidized in order to sharpen the remaining polysilicon tips.

The wafers are then patterned with Mask #3, the contact via mask, to open the contact via windows and to etch the oxide in these vias down to poly-Si layer. The wafers are then coated with gold to form the gate electrode. A 10 nm thick Cr layer is used as an adhesion layer between silicon dioxide and gold layers. The gate metal is then patterned with Mask #4, the gate address line mask, and the remaining gold is etched.

Finally, the wafers are scribed half way through, to secure die separation. The wafer, or the individual dies are then ready for cap lift-off in BOE.

The SOI fabrication process is similar to poly silicon process.

The metal etch stop is the same as the process described above, except that a Cr layer is deposited in-between the polysilicon layer. The upper poly layer determines the tip height while the lower layer determines the resistor structure. During isotropic tip etch, the upper poly layer is etched down to the Cr etch stop, thus ensuring tip height uniformity across the 4 inch wafer. The exposed Cr is then etched away before tip sharpening oxidation and the polysilicon process is followed to completion.

The fabrication issues for focusing surfaces have been addressed above.

EXERIMENTAL PART

The UC Davis Vacuum Microelectronics Group is investigating application of MEMS fabrication techniques for the formation of subtractive-tip field emission arrays. The personnel now working to assist the PI are one Research Associate, one Postdoctoral Assistant, and one Ph.D. graduate student. Capital equipment is all ordered; most is now delivered and installed; there are some attachments which remain to be made operational . There are four main tasks, ongoing in parallel, with the fifth, measurement, overlapping the main tasks.

C.3. SINGLY-ADDRESSABLE ARRAYS OF POLYSILICON FIELD-EMISSION CATHODES.

Polysilicon is a promising candidate material for field-emission microelectronics devices. It can be competitive for large-size, cost-sensitive applications such as flat-panel displays and micro electro-mechanical systems. Singly-addressable arrays of field-emission cells were fabricated in a matrix configuration using a subtractive process on Polysilicon-On-Insulator substrates. Matrix rows were fabricated as insulated polycrystalline silicon strips with sharp emission tips; and matrix columns were deposited as gold thin film electrodes with round gate openings. Ion implantation has been used to provide the required conductivity of the poly-Si layer. To reduce radius of curvature of the polysilicon tips, a sharpening oxidation process was used. The final device had polysilicon emission tips with end radii smaller than 15 nm, surrounded by gate apertures of 0.4 μm in diameter. Field emission properties of the cathodes were measured at a pressure of about 10^{-8} Torr, to emulate vacuum conditions available in sealed vacuum microelectronics devices. It was found that an emission current of 1 nA appears at a gate voltage of 25 V and can be increased up to 1μA at 70 V. Over this range of current, no "semiconductor" deviation from the Fowler-Nordheim equation was observed. I-V characteristics measured in cells of a 10x10 matrix, with a cell spacing of 50 μm demonstrated good uniformity and reproducibility.

Low-voltage field-emission cathodes are a promising type of electron source for vacuum microelectronics devices. During the last ten years, a broad collection of new emissive materials such as diamond and diamond-like carbon, compound semiconductors, noble metals, etc., have been used for field-emission cathode fabrication. Single crystal silicon, because of its advantages in VLSI technology still remains one of the most frequently used materials for many applications including flat-panel display, multi-beam lithography, microscopy, and data-storage devices [6,7]. However as the size of the single-crystal Si substrates increases, the factors related to manufacturing cost and technological complexity impose further limitation on fabrication of the cathodes for flat-panel displays and micro electro-mechanical systems. Polycrystalline silicon may be considered as a good alternative to single crystalline silicon because it can be cost-effectively deposited over larger size dielectric substrates and still be compatible with traditional semiconductor manufacturing methods.

Recently, it was found by E. Boswell and colleagues in diode emission tests, that the polycrystalline silicon field emitters fabricated using wet etching method, exhibit an emission behavior similar to single crystal silicon emitters [8]. It was observed that the oxidation sharpening had little effect on the field-emission characteristics due to the presence of sharp emitting silicon tips in a polycrystalline material. In a structure fabricated by H. Uh and others, both single and polysilicon gated field-emission arrays were fabricated on oxidized silicon substrates using RIE etching and sharpening oxidation. Stable emission currents of 0.1 μA/tip were measured at 82 V for polycrystalline tips with a gate aperture of 1.2 μm and at 80 V for single-crystal tips with gate aperture 1.6 μm [9]. This result is similar to the data obtained previously from excellent, uniform, very-low turn-on voltage single crystal silicon field emission arrays described by M.Ding et al [10].

In this paper we present a new version of a low-cost and dependable method of fabrication of singly-addressable arrays for multi-beam vacuum microelectronics device applications.

C.3.1. Experimental Details

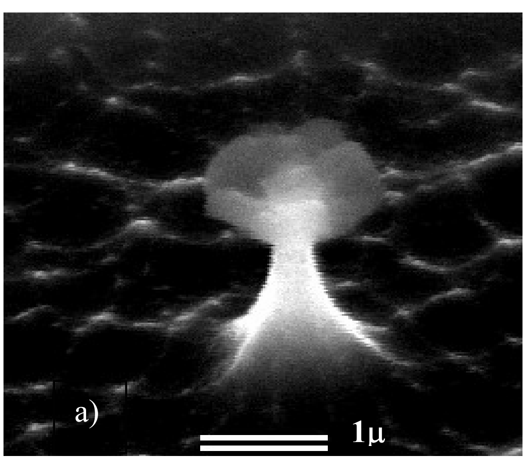
The singly-addressable field-emission cathodes matrix consist of polysilicon "stripes" in which the emission tips are formed, over coated with oxide and having metal stripes, perpendicular to the polysilicon lines, which is used to form the gates.

The fabrication process requires a silicon-oxide-silicon structure consisting of a silicon substrate with at least 1 µm of oxide and 3 µm of polycrystalline silicon. Initial poly-silicon deposition techniques, performed at standard 620 C°, resulted in a surface with significant roughness and large silicon grain size. This influenced the minimum feature size obtainable (we use Karl Suss MA-6 vacuum contact lithography) and had a negative effect on the shape and geometry of the silicon tips. To reduce the grain size and to provide a more smooth coating, we lowered the deposition temperature to the lower value of 590 C°.

The initial resistivity of the polycrystalline silicon layer exceeded 100 kΩ-cm, which was excessively high for our application. To reduce the resistivity, the layer of polysilicon was doped by phosphor ion implantation using a dose of 3×10^{14} cm^{-2} at of 80 keV. No subsequent annealing was performed. The polysilicon was oxidized with total time 2 hours at 1100°C to obtain a 0.15 µm thick SiO_2 layer. The oxidation time was sufficient for annealing and impurity activation. After oxidation, the measured bulk resistivity of the polysilicon layer was close to 3 Ω-cm and the sheet resistance was 10 kΩ/□. This resistivity inherent to the polysilicon enabled us to obtain series resistors of 1 MΩ for each emission tip. The resistors proved to stabilize the field emission current from the individual tips, as expected.

Following the ion implantation step, the oxide layer was coated with 0.1 µm chromium to provide an etch mask. The process flow of the singly addressable array fabrication includes two chrome-oxide-polysilicon structure-etching steps. The first step produces a simple system of insulated polysilicon cathode stripes, which do not require high-resolution lithography. A variety of wet etching processes of chromium, silicon dioxide and polysilicon layers were tested for obtaining these stripes. Good results were obtained, including tilted sidewalls of the polysilicon stripes in which the cathodes are later etched. The cross-section shape provided effective step-coverage of the cathode stripes afterward with the gate metal layer. Although dry etching of polysilicon was also investigated, the sidewalls were excessively vertical and it was found that wet etching resulted in better uniformity across a 4-inch wafer.

The second masking and etching step forms the tip portion of the cathode electrodes, leaving a 1 µm diameter chrome/oxide tip cap where the tip is to be formed. Because of the grain structure of polysilicon it is extremely important doing tip etching to use isotropic reactant. Plasma etching in a SF_6/O_2 gas mixture as well as pure SF_6 was attempted. It is found that pure SF_6 provides more smooth and uniform etching in comparison with mixtures using 10% and 50% O_2.



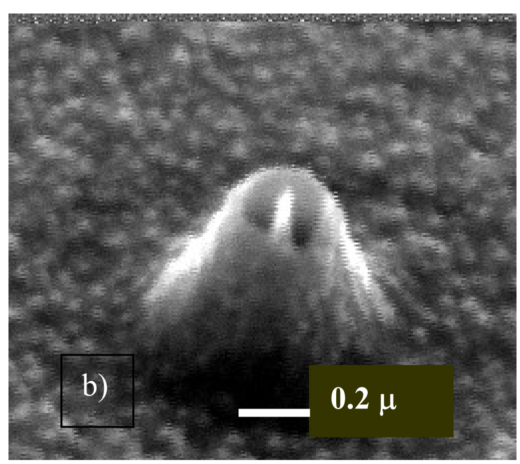


Figure C3. a) Polycrystalline silicon tip before oxidation sharpening. Oxide cap is on top of the tip.b) A completed volcano-type field-emission cell, having 0.3 μ gate opening and approximately 15 nm tip curvature radii.

The tip etch is continue until the diameter of the narrowest part of the tip decreases down to 0.2 μm as it is shown on Figure C3. At this point oxidation sharpening is carried out. A combination of wet and dry oxygen is used because tip sharpening is more effective in dry oxygen at low temperature; however the oxidation time would be excessively long if only dry oxidation is used. This oxidation also increased the thickness of oxide on the surface of cathode stripes and reduced the gate-cathode current leakage.

The gold film used as a gate electrode was deposited by electron-beam evaporation using the method we have previously described elsewhere [6]. As a result, the gate metal is coated on the sidewall of the tip and is barely masked by the oxide cap. This method allows us to form the gate aperture, having a diameter of 0.3-0.4 μm using conventional optical lithography technology with resolution normally producing larger feature sizes. Tip caps were subsequently removed by wet etching of the silicon dioxide. The final “volcano-type” emission cell is shown in Figure C3b. The typical tip curvature radius is estimated using microscopy, to be on the order of 15 nm.

C.3.2. Discussion.

We tested the electrical and emission properties of the cathodes in a matrix configuration. No electrical cross-leakage between the cathode stripes and the gate electrodes in air was observed (up to 10 V DC and 1 nA sensitivity). Field emission properties of the cathodes were measured in a vacuum chamber under a residual gas pressure of 10^{-8} Torr. Characterization was performed without bake out of the vacuum system. No tip conditioning or field forming steps was performed. The Hewlett-Packard 4142B modular DC source/monitor was used to acquire the emission data. The gate electrode was grounded, positive potential (up to 100 V) applied to stainless steal foil anode, and the cathode had a negative bias. Anode-cathode spacing was approximately 1 mm.

Figure C4a shows current-voltage characteristic, obtained from a single-cell cathode with a gate opening of 0.4 μm. It was found that emission current of 1 nA is first registered at a gate voltage 25 V, increasing to 10 nA at 30 V. The Fowler-Nordheim (FN) plot for this region is a straight line, as it shown on Figure C4b. To achieve 1 μA we needed to increase the voltage between the tip

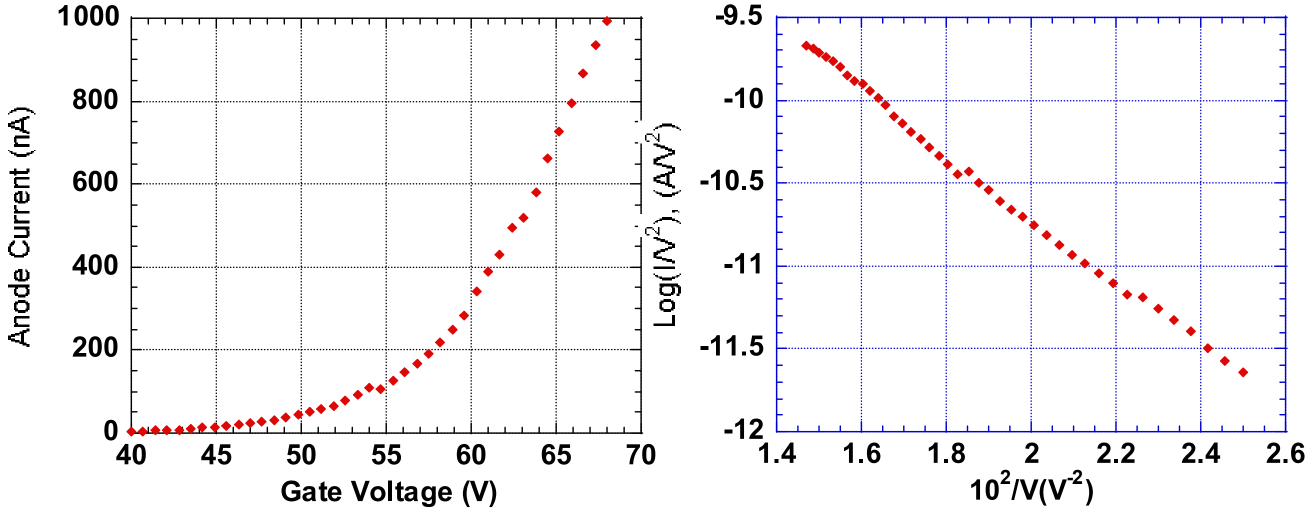


Figure C4. a) (left) Anode current vs. gate voltage plot and b) (right) the Fowler-Nordheim plot for the anode current up to 1000 nA.

The gate to 68 V. For the tested range of current no "semiconductor" deviation from Fowler-Nordheim equation was observed. We consider that combination of sufficient doping level within silicon grains and high sheet resistivity on the grain borders are responsible for this behavior. The minor shifts in the plot on Figure C4b could be explained by fluctuations of emission current, which are usually significant for single tip field emitters. The dependence of the anode current varying with gate and anode voltage as a parameter (e.g. “triode characteristics”) is shown in Figure C5 Lifetime of an individual cathode cell was up to 200 hours. Several cathodes were damaged under attempts to extract and maintain maximum possible levels of emission current. It was observed that tip damage by emission current occurred under loading of 1.5 μA per tip. These attempts often resulted in the tip destructing, as shown in Figure C6.

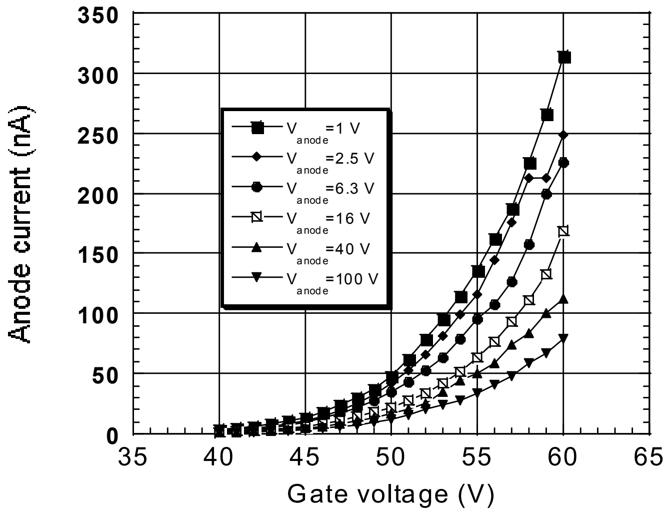


Figure C5. Anode current vs. gate voltage at different anode potentials relative to gate potential (e.g. "triode characteristics").

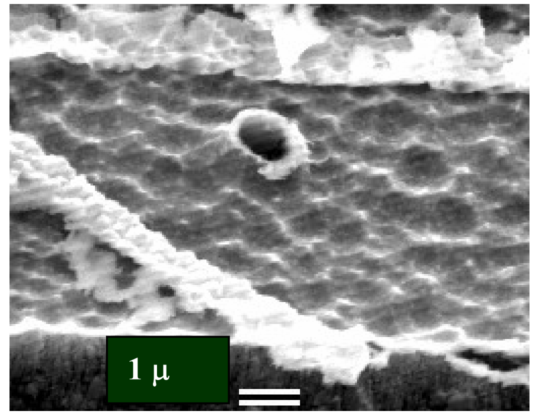


Figure C6. SEM picture showing an exploded cell, caused by excessive steady-state cathode current

High electrical and heat conductivity of the gold gate film and MΩ resistivity of cathode strip minimized damage of the structure, which is important for high-density matrix applications. I-V characteristics of separated cells in the 10x10 matrix, with the distance between adjacent emitters of 50 micron were tested demonstrating good uniformity and reproducibility. The emission current does not appear to be significantly affected by the random crystalline orientation of the emitting tip crystallite of each cathode.

Polycrystalline silicon on an insulated substrate is suitable for field-emission cathode fabrication instead of SOI wafers as it allows us to avoid the cost and size limitation.

We developed subtractive technology of singly-addressable cathode matrix fabrication, which provides a gate opening as small as 0.3 micron using contact lithography with a resolution of 1 micron. Loading resistors of any required resistance could be integrated with the cathode because of high intrinsic resistivity of polycrystalline silicon layer. An anisotropy of resistance of polycrystalline layer in lateral and orthogonal directions improve linearity of Fowler-Nordheim characteristics of the field-emission cathode.

The emission current up to 1 μA was extracted from a single tip at a gate voltage not exceeding 70 V.

C.4. SURFACE TREATMENT ON SILICON FIELD-EMISSION CATHODES

Silicon field emitters have demonstrated their viability as electron sources for various vacuum microelectronics applications. In recent years, the attention is drawn towards post-fabrication seasoning processes aiming to improve the performance of the field emitters. In the current work, we attempt various methods of surface treatment of single-crystal silicon emitter arrays fabricated by the well-developed subtractive manufacturing process [12]. The arrays of 50x50 tip emitters were fabricated from p-type (4-6 Ωcm) Si (100) substrate by the above process. Firstly, thermal grown oxide of 2000 Å thick and a 1000 Å thick chromium layer on the Si were patterned into a 1.8 μm-diameter disk. Using the chromium and the SiO_2 disk as a mask, the outline of the emitter tip was formed by means of ion reactive etching with SF_6 as shown in Figure C3 (a). The tips were then sharpened using the method of oxidation sharpening as we have previously described elsewhere [13]. Tip caps were subsequently removed by wet etching of the silicon dioxide. The typical tip curvature radius is estimated using microscopy, to be on the order of 15 nm.

We investigate three methods of seasoning during the operation of the field emitters – conditioning of the emission surface using low-energy electron-stimulated desorption, surface treatment by residual gas ions, and surface cleaning using hydrogen-enhanced residual gas atmosphere.

C.4.1. Results and Discussion

We tested the electrical and emission properties of the cathodes in a diode configuration as shown in Figure C7. A flat Si anode, spaced nominally 150 μm or 6 μm from the cathode by using a quartz spacer of a proper thickness, was used. Field emission properties of the cathodes were measured in a vacuum chamber under a residual gas pressure of 10^{-8} Torr. Characterization was performed without bakeout of the vacuum system. The Hewlett-Packard 4142B modular DC source/monitor was used to acquire the emission data. A positive potential (up to 100 V) was applied to anode, and the cathode had a negative bias. The field emission properties of the cathodes were measured after the tips were conditioned for 3 days.

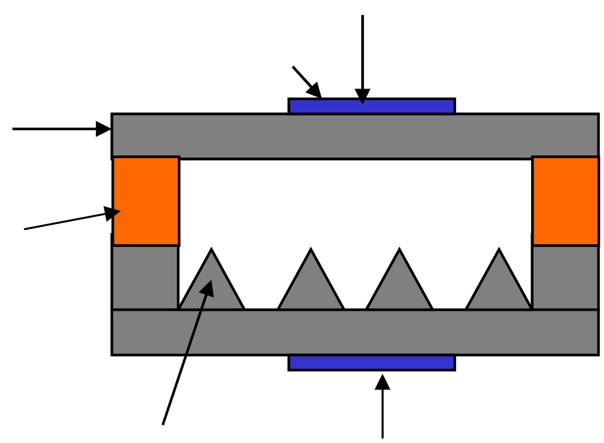
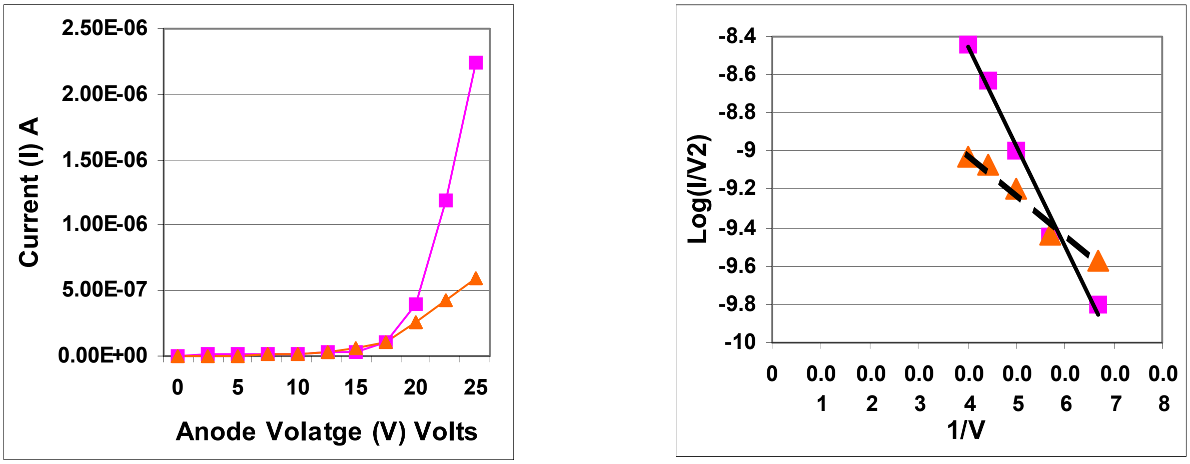


Figure C7. Test structure. The Cathode is mounted on to a TO_3 Transistor package



(a) (b)

Figure C8. I-V characteristics (a) and the F-N characteristics (b) before (lower curve) and after (upper curve) the surface conditioning by low-energy electron stimulated desorption under low current loading.

First method of conditioning consists of cleaning of the surface by low-energy electron stimulated desorption under low-current loading. The first treatment method was performed in a slightly different configuration compared to one shown in Figure C7: instead of the flat silicon anode we have used the same tip structure as the cathode to be treated. The reverse bias voltage was in the region from 16 to 22 V, which allowed us to obtain the emission from the anode tip array to the cathode tip array. We have observed the initial I/V characteristics and the short-term current behavior of the “fresh” silicon cathodes (Figure C8a, lower curve), then we reversed the polarity of the electric field by applying negative voltage to a silicon anode and using the silicon field emitter as an electron collector without changing the geometry of the cathode-anode “sandwich”. In this configuration we ran the diode for a period up to 16 hours. The current density during the treatment was maintained on the level of 10^{-4} A/cm^2. The electron energy was in the range between 16 to 22 eV. The Coulomb dosage applied to the cathode surface was estimated to be on the level of $6*10^{-2}$ C/cm^2. No changes in the emission from the anode were observed during the entire treatment. After the treatment, an increase of the emission current by a factor of 5 (Figure C8a, upper curve), along with stabilization of the I/V characteristics were observed.

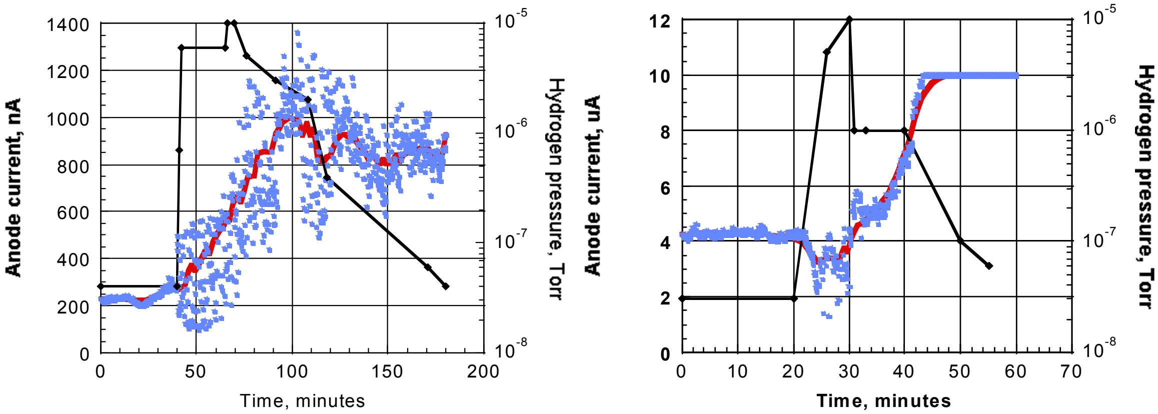
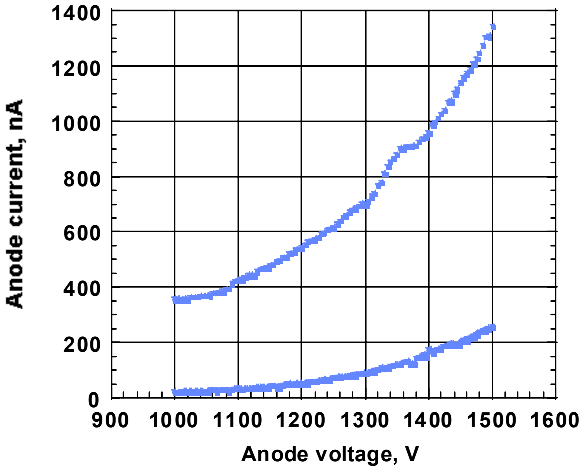


Figure C9. The effect of hydrogen treatment on silicon field-emission array cathodes under (a) (left) high (1500 V) and (b) (right) low (22V) anode voltage.

We believe that the electron bombardment using low-energy electrons helps to clean the surface of the emissive tips.

The second method consists of the surface cleaning using hydrogen-enhanced residual gas atmosphere during the operation of the cathode [14]. The getter ST-172 was heated up to 700°C to produce the hydrogen enriched atmosphere [15]. The treatment using a getter as a hydrogen source was suggested as a simple and cost effective method to use in the laboratory vacuum system. This method also can be easily used in industrial manufacturing of sealed vacuum devices equipped with modern getters. The experiment was performed for high voltage (1500V, 150 μm gap) and low voltage (22V, 6 μm gap) diodes as shown in Figure C9a. and C9b. In the figures the solid line indicate the change in hydrogen pressure from $4x10^{-8}$ to 10^{-5} Torr , the curve indicate the average emission current over time and the dots indicate the actual emission current. It is seen in Figure C4a that for high voltage diode there is a considerable increase in the emission current for about a factor of 5 after approximately 1 hr of treatment in hydrogen atmosphere. The same effect is observed for the low voltage diode during the time range of 20 min to 30 min. After the surface was cleaned using hydrogen-enhanced residual gas atmosphere, the tips were tested for a day at a pressure of $4x10^{-8}$Torr. It was observed that the emission current remained approximately at the value immediately following the surface treatment. We suggest the following mechanism for the FEA performance improvement: that the electrons emitted from the cathode help to break the hydrogen molecules and/or ionize the hydrogen atoms from the hydrogen enhanced atmosphere. These ions and atoms react with the surface contamination like oxide, carbon residue etc. of the tips and clean the surface lowering the work function.

The third method, accelerated “natural” surface conditioning was performed by increasing the pressure of residual gases. This was done by interrupting the pumping in the vacuum chamber during prolonged operation of silicon emitters from several hours to several days. The I-V characteristic seen in Figure C5a corresponds to the two curves measured before (lower curve) and after (upper curve) the experiment. It is seen from the two graphs that there is a considerable increase in the emission current.



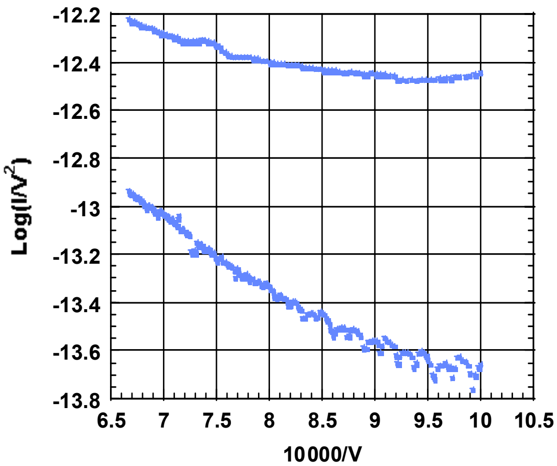


Figure C10. I-V characteristic and the F-N characteristic before (lower curve) and after (upper curve) the "natural" surface conditioning was performed by increasing the pressure of residual gases.

We believe that the short-term exposure to the enhanced residual gases atmosphere helps to remove an initial film of contaminants and adsorbents by ion sputtering. The two main disadvantages of this method are the following: first it requires a prolong treatment to achieve a desirable value for the emission properties, and second this method is not very advantageous to achieve the highest emission properties as obtained in the above two processes.

It should be noted that all the above methods resulted in comparable improvement in reproducibility of I-V characteristics taken after the treatment.

Three methods of surface treatment were applied to silicon field emitter arrays fabricated by subtractive process. All three methods – low energy electron-stimulated desorption, hydrogen seasoning, and residual gas ion conditioning, were performed in a simple small-volume stainless vacuum system. The methods clearly show improvement of emission characteristics, increase of emission current and stabilization of cathode performance. The hydrogen treatment seems to be suitable for improving the properties of the gated field-emission cathodes.

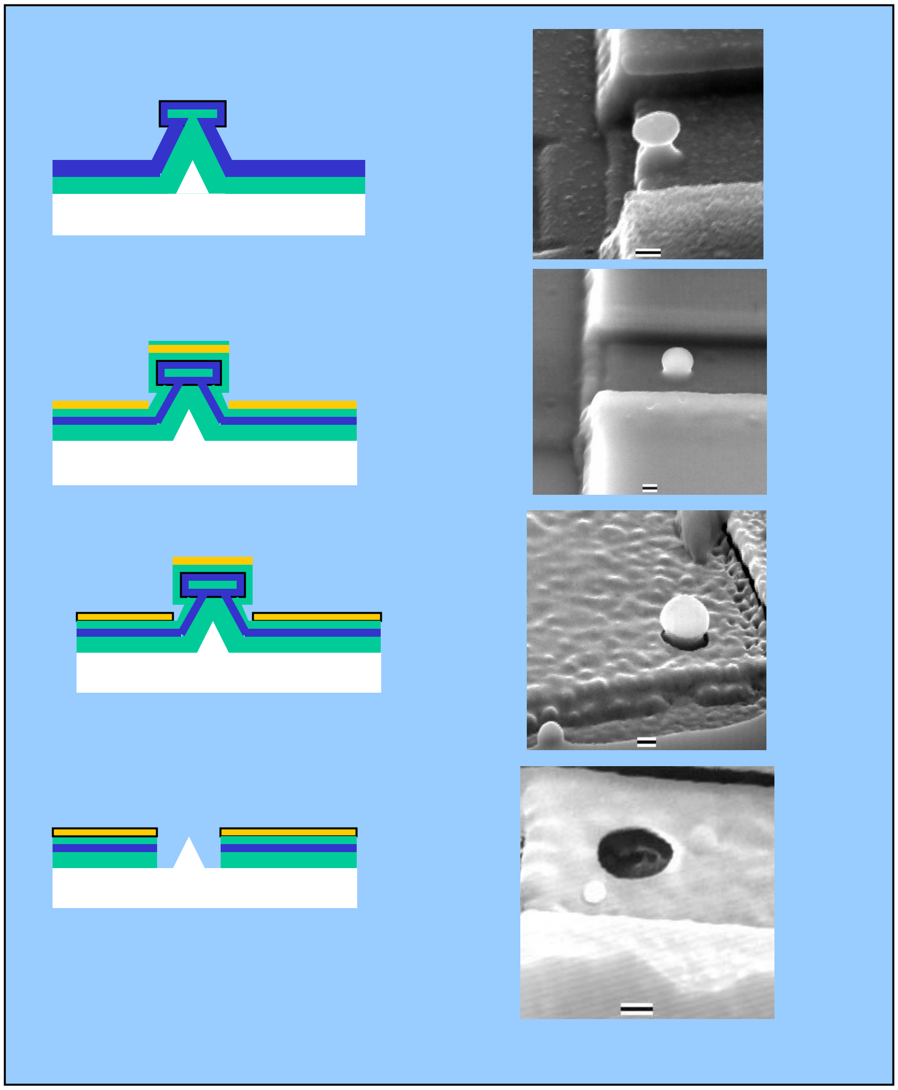


Figure C11 The schematic diagram of the double-gated cell fabrication process.

C.4.2. Double-Gated Singly Addressable Polysilicon Tip Array

The schematic of the second gate integration into a polysilicon field-emission cell is shown in Figure C11 a-d. After oxidation sharpening, the structure is coated with a polysilicon layer with a thickness of about 0.5 micron (Figure C11a). This layer is oxidized, producing an oxide thickness up to 0.5 micron on the top of the polysilicon. The oxidation changes the size and the shape of the tip, which is illustrated by the SEM micrographs (Figure C11b). The tip cap acquires an almost perfect spherical shape. This shape changes the shadowing effect of the cap, affecting the parameters of the next step - the deposition of the gold focusing grid (Figure C11c). The sequence of several etching steps removes the cap from the top of the structure and opens up the final emission cell (Figure C11d).

It has been found during the process development, that with variation of the film thickness and the process conditions, two different types of emission cells could be fabricated. The first configuration is very close to the coaxial electron-optic type. The lens electrode is placed above the gate electrode and is separated from the gate by an insulator layer. Figure C12 illustrates this configuration by the SEM micrograph (a) and the geometric depiction (b). Another type of the double-gated emission cell, of the coplanar type, is illustrated by Figure C13a,b. These two types of double-gated cells have significant differences in electron-optical properties, but both of them can be utilized in various types of microelectronic devices**.**

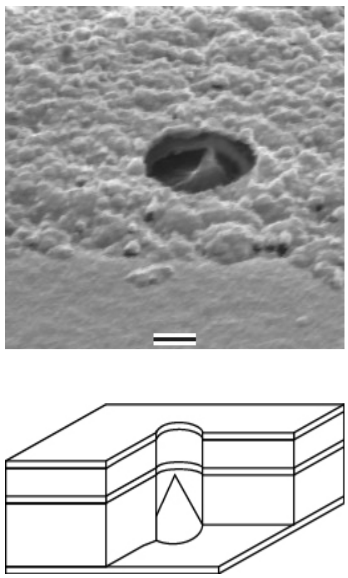


Figure C12 . The coaxial type of focusing field-emission cell

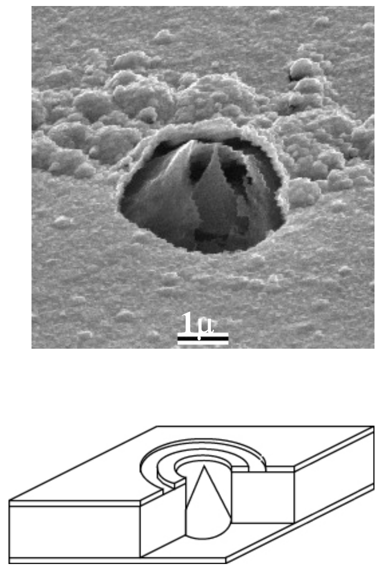


Figure C13 The coplanar type of focusing field-emission cell

The goal of the work is not limited by double-gated cathode cell fabrication, but also involves the design and fabrication of the 10x10 matrix test device along with packaging suitable for vacuum chamber tests. figure C14 shows the optical micrographs of the 10x10 field emission matrix device. the matrix consists of 10 vertical polysilicon stripes as cathode columns, and two layers of grid rows. the cathode columns have contact pads on both (upper and lower) ends, which is necessary for resistivity control. contact pads for polysilicon extracting grids are located on the left side of the chip, and for the focusing gold grids - on the right side. the actual size of the matrix is 500 μm, with each stripe of 34 μm in width and 16 μm gap between them. the measured cathode line resistance was about 1 mΩ, extracting grid stripe resistance was nearly 200 kΩ, and gold stripe resistance did not exceed 6 Ω. using polysilicon technology is able to provide extremely wide range of built-in resistances for individual cathodes by simply changing the doping level of the polysilicon.

To test the matrices, the tetrode package for the visual and the electrical testing of the double-gated field-emission arrays was designed. The package, shown in Figure C15, consists of a ceramic integrated circuit carrier with 24 electric leads, a conductive phosphor screen used as an anode, and a cathode matrix. Most of the grid and cathode stripes of the test device were connected with carrier leads by the gold wire bonding. To improve optical resolution of the focused image, the phosphor screens were made using electrophoretic deposition of low voltage phosphor powder, with particle size less than 1 μm, onto glass slides coated with conductive indium-tin oxide. Figure C16 shows an actual view of the test package. The test chip with the field emission matrix is placed at the top of the carrier to provide a reference scale. The external size of the chip is 5x5 mm.

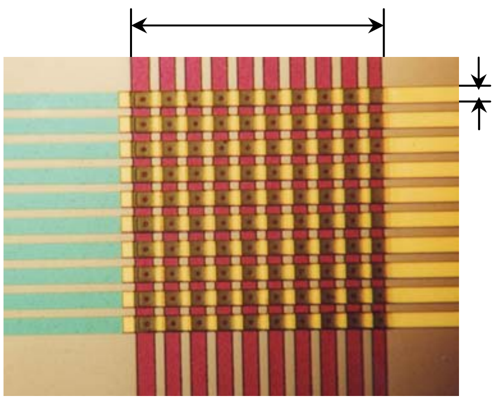


Figure C14 . Optical micrograph (30x) of the 10x10 matrix of the test device

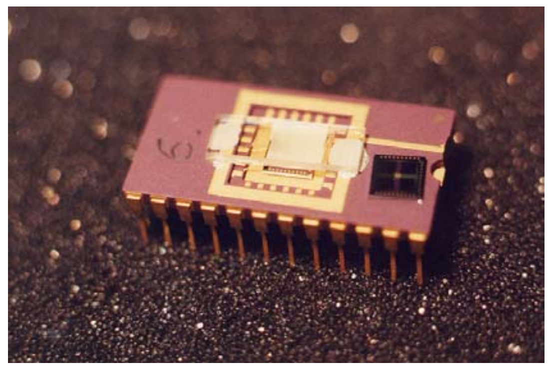


Figure C15 Test device package

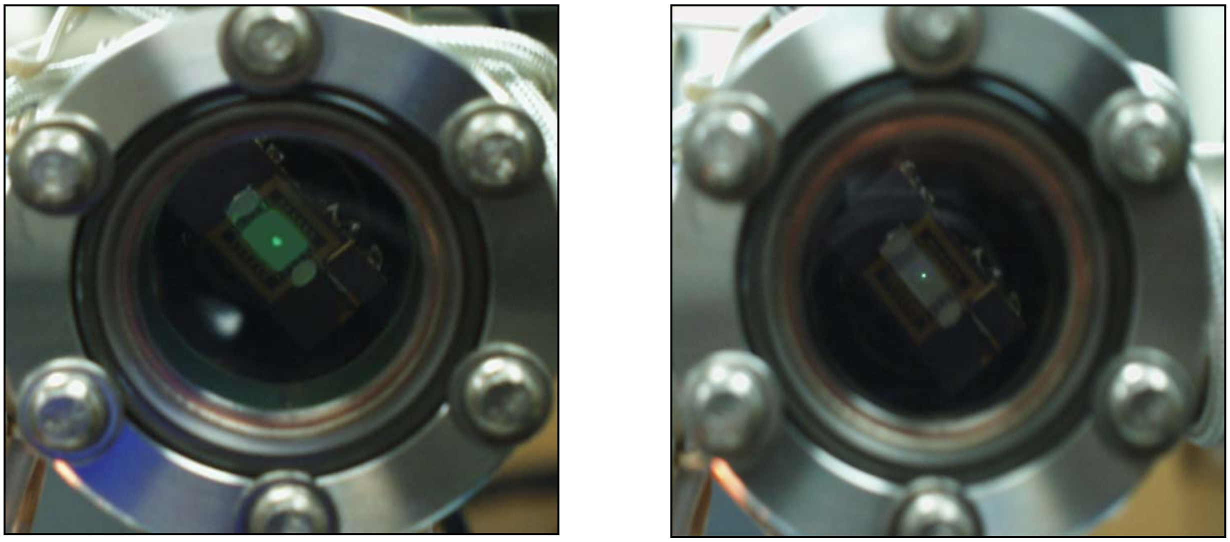


Figure C16 Focusing at various terminal voltages and constant anode current 80 nA. a) extracting and focusing grid potential +215 V Anode voltage +500V b) extracting grid under +230 V focusing grid grounded, anode voltage +800 V

Preliminary results of the focusing electrode influence on electron beam shape is shown in Figure C6. To provide a fair comparison, the focusing measurements were performed at constant anode current of 80 nA. The diameter of the observed light spot changes following the variation of the second gate voltage under constant anode current. In Figure C16a diffused spot of light of 2 – 2.5 mm in diameter is obtained under the same positive potential for the extracting and the focusing grids. The extracting and the focusing grid potentials were set to 215 V; the anode voltage was 500V. This condition is similar to the electron optics of a single-gated cell. On Figure C16b sharp and bright focused spot with the diameter of ~0.6 mm is obtained as a result of applying the ground potential (which is equal to the cathode potential) to the focusing grid. Under these conditions, the extracting grid voltage had to be increased to 230 V, and the anode voltage had to be increased to 800 V to keep the anode current constant. A visual linear size of the focused light spot was reduced by a factor of four. We consider this observation as a promising result demonstrating a proof of principle for the focusing technique.

C.4.3. Surface treatment of the emission tips

The device configuration considered for the surface treatment of the emitters is the "bed of nails" which is an array of un-gated single crystal Si emitters placed in an area of 4 cm2 with a tip-to-tip spacing of 6μm. The emitters were formed from p-type (1-10Ωcm) Si (100) substrate by the subtractive tip fabrication process. Firstly, thermal grown oxide of 2000 Å thick and a 1000 Å thick chromium layer on the Si were patterned into a 3.0 μm-diameter disk. Using the chromium and the SiO2 cap as a mask, the outline of the emitter tip was formed by means of reactive ion etching with SF6. The tips were then sharpened using the method of oxidation sharpening. Tip caps were subsequently removed by wet etching of the silicon dioxide. The typical tip curvature radius is estimated using SEM microscopy, to be on the order of 15 nm.

We tested the emission properties of the cathodes in a diode configuration. The packaging of the cathodes containing the array of ungated Si-tips for testing in a high vacuum environment is done by placing quartz spacers, 60 – 70 μm thick between the cathode and the phosphor screen, which acts as an anode, as seen in Figure C17.

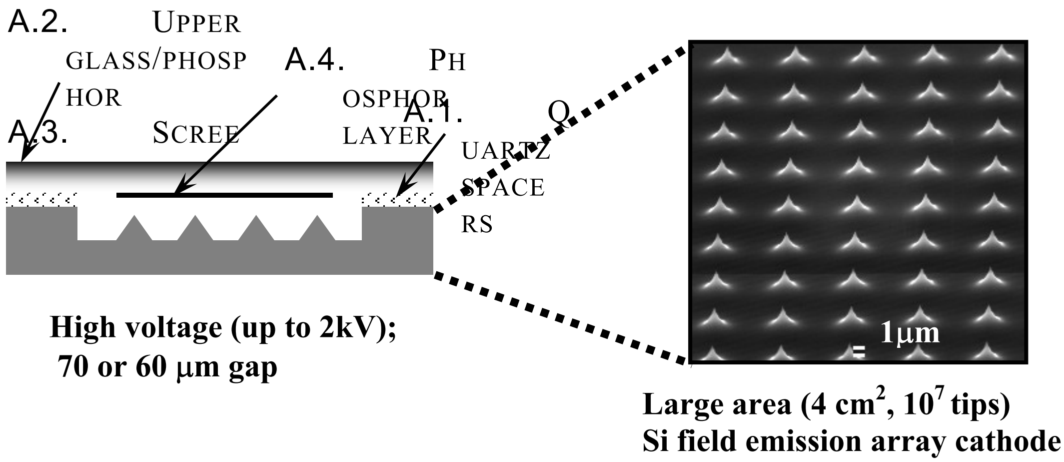
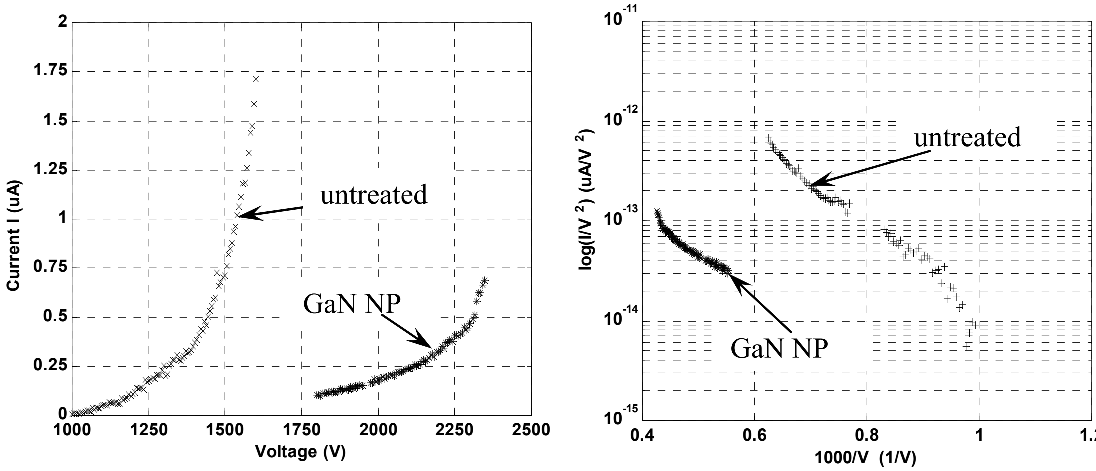


Figure C17. Test structure: Diode design for Si-tip array testing

The whole assembly is then held together on both sides by a spring. This arrangement helps us to remove the sample after the measurements, maintain the same measuring set up before and after the surface treatment and also allows us to compare the emission characteristic before and after treatment of the arrays. A medium voltage green-color phosphor (Osram Sylvania 9420) was deposited on patterned ITO glass by electrophoresis. The advantage of this process was that the deposition was carried out in room temperature with a very uniform thin layer of small particle phosphor being deposited. The phosphor screen helps us to visually investigate the distribution of the emitting tips.

Field emission properties of the cathodes were measured in a vacuum chamber under a residual gas pressure of 10^{-8} Torr. A positive potential (to 1000 volts) was applied to the anode, and the cathode had a negative bias. The field emission properties of the cathodes were measured after the tips were conditioned for 3 days under a constant DC bias.



(a)

(

Figure C18. (a) I-V characteristic and (b) the F-N characteristic of the before and after the emitter surface was coated with GaN nanoparticles (NP)

The I-V characteristics as seen in Figure C18a correspond to the two curves measured before and after the surface of the emitter was coated with GaN nanoparticles (particles size about 2-20nm). It is seen from the two curves that there is an increase in the turn on voltage and there is considerable degradation in the emission current. Figure C18b is a Fowler-Nordheim plot. Again, both the treated and untreated case have straight F-N behavior. The I-V characteristics, as seen in Figure C19a, correspond to the two curves measured before and after the surface of the emitter was coated with nanocrystalline diamond (particle size about 5-10nm). It is seen from the graph that there is a considerable reduction in the turn on voltage and there is no degradation of the maximum extracted emission current. The results suggest that the reduction in the turn on voltage is due to the decrease in the effective workfunction of the emitter. Figure C9b is a Fowler-Nordheim plot of these data. It is seen from the graph that the emission characteristics shows a straight line behavior in both the treated and untreated case. It is also observed that the uniformity in emission from the array is increased in the region of low voltage operation when the surface of the emitters is coated with nanocrystalline diamond.

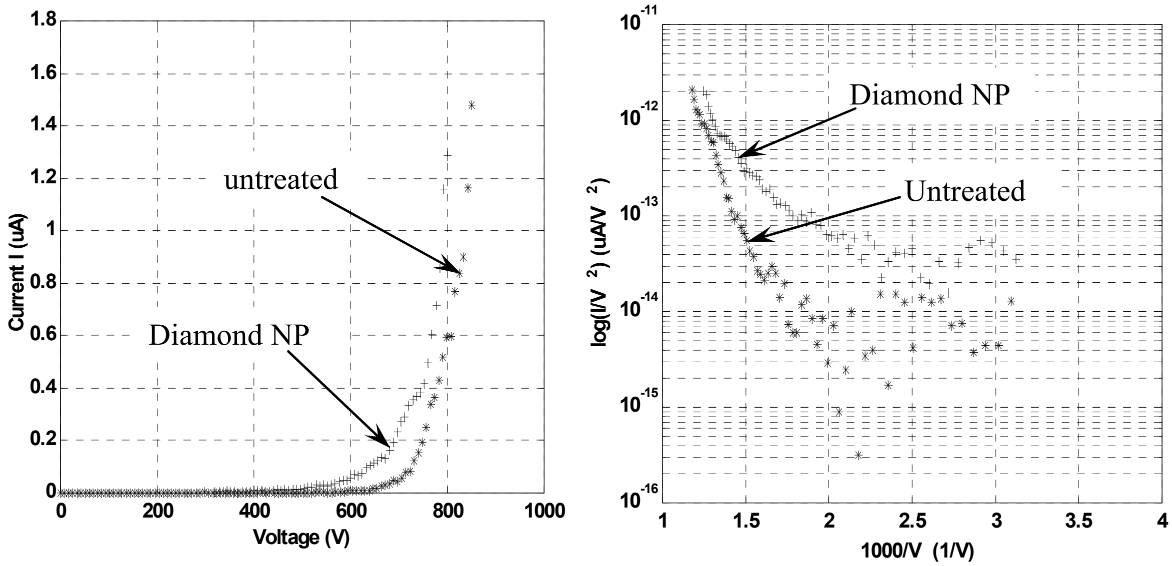


Figure C19 (a) I-V characteristic and (b) the F-N characteristic of the before and after the emittersurface was coated with nanocrystalline diamond.

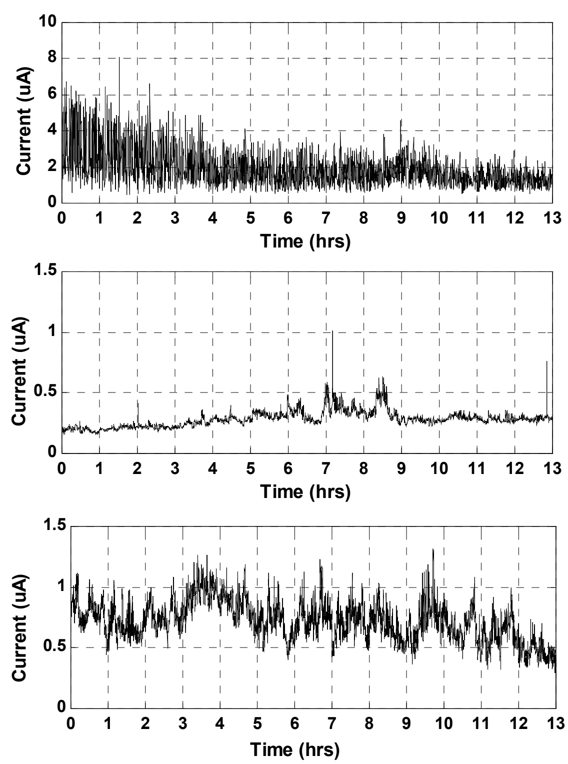


Figure C20. Current versus Time characteristics of an array of silicon emitter: (a) untreated; (b) coated with GaN nanoparticles; (c) coated with nanocrystalline diamond

The current versus time characteristics as seen in Figure C6 shows the emission current stability of an untreated (a), coated with GaN nanoparticles (b) and coated with nanocrystalline diamond (c) emitter array over an operating cycle of thirteen hours. In case of untreated silicon as seen in Figure C20a, the standard deviation of current fluctuation was about 49% of the average current value (1.91μA). The emitter surface coated with GaN nanoparticles and nanocrystalline diamond as seen in Figure C20b and C20c show a significant improvement in the current stability. The standard deviation of current fluctuation was about 24% of the average current value 0.28μA and 0.72μA respectively. The improvement in the current stability is due to the chemically inert intrinsic behavior of diamond and gallium nitride. It acts as a protective layer for the sharp conductive core from ion bombardment.

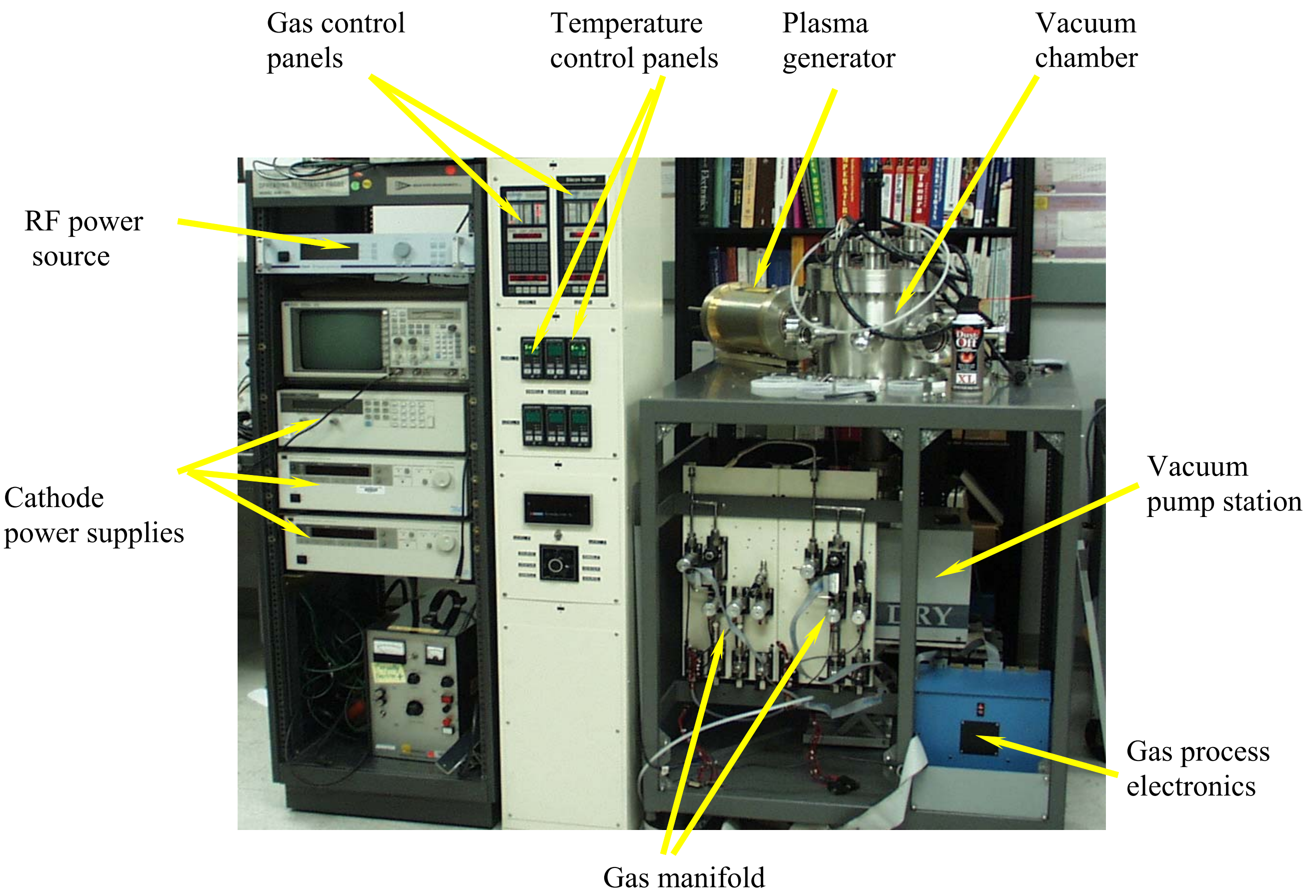


Figure C21 Burn-in test bed

Plasma treatment (burn-in) system the 13.56 Mhz, air cooled, plasma source is used to generate a dense gas plasma for the emission surface post-processing, pre-treatment, burn-in and possible modification (seasoning). addition of the plasma source directly to the UHV measurement system make it possible to precondition/cleaning of the tips and array assemblies, to study the emission surface treatments/coating effects, and to achieve in-situ enhancements of the field emission properties. a dense plasma discharge is formed for a very brief time (from few seconds to a few minutes) inside the middle of the source region and contained by the dielectric process tube of the plasma source. Vacuum chamber interface is accomplished through 2.75” standard vacuum flanges, lock valve and the orifice. a downstream process application includesprocess gas introduction at one end with the active plasma species emerging at the opposite end. The field emitter conditioning/coating enhancement process occurs inside the vacuum chamber. Figure C21 shows the downstream plasma source used for cathode array cleaning and burn-in. The plasma discharge is used directly prior to the measurements using oil less turbo/dry diaphragm pumping. For the following operation of the FEA, the plasma source is isolated from the vacuum chamber by closing the UHV valve; the measurements are performed using pumping by the turbo or ion pump.

High pressure (10-1000 mTorr) plasma generation is used for confined narrow-beam plasma flux treatment of the cathode using reactive gases (H_2, CF_4, SF_6). The directional plasma stream entering the chamber through the orifice is seen in the background. The field emission array position in the plasma flux can be adjusted using linear translation manipulator. The anode assembly (not shown) can be moved away from the plasma flux path using a vertical motion feedthrough.

Low pressure (0.1 – 10 mTorr) is used for FEA treatment by accelerated ions of chemically inert gases (Ar, N_2). The plasma uniformly fills the entire chamber. The tip array can be grounded or electrically biased during the treatment.

C.4.4. Study of Emission Behavior of UNCD Coated Silicon Field Emitter Array in Different Gases and Pressures.

We investigated the field-induced electron emission properties of ultrananocrystalline diamond (UNCD)-coated Si microtip arrays. Silicon field emitter array was fabricated by the subtractive process as discussed earlier. In Figure C23 we can see the SEM images of the fabricated array. Highly conformal, uniform, smooth UNCD films as shown by high-resolution scanning electron microscopy in Figure C24 were grown on a high-density array of 1 μm height Si microtips using a patented microwave plasma chemical vapor deposition (CVD) technique with a new CH_4-Ar-rich chemistry developed at Argonne National Laboratory. We used two seeding processes both involving exposure of the tip arrays to a liquid suspension of nanocrystalline diamond (ND) powder. In the first one, the tip array is immersed in the ND powder suspension in an ultrasound bath, while in the second one the tip array is immersed in a bath in front of a Pt electrode to produce seeding via electrophoresis. The ultrasound bath seeding produced the best results in terms of inducing extremely conformal, smooth UNCD coatings on the microtips.

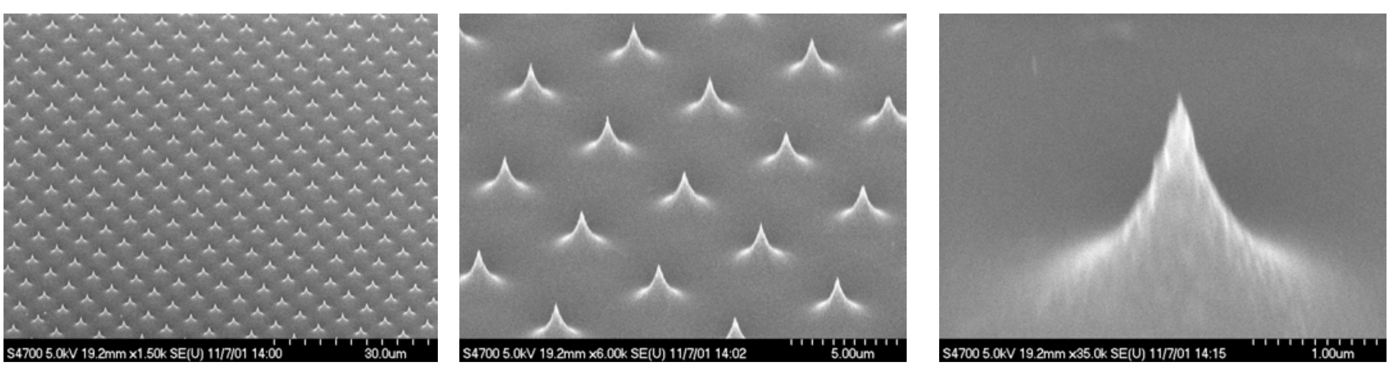


Figure C22 Bare silicon tip array, fabricated by subtractive technology.

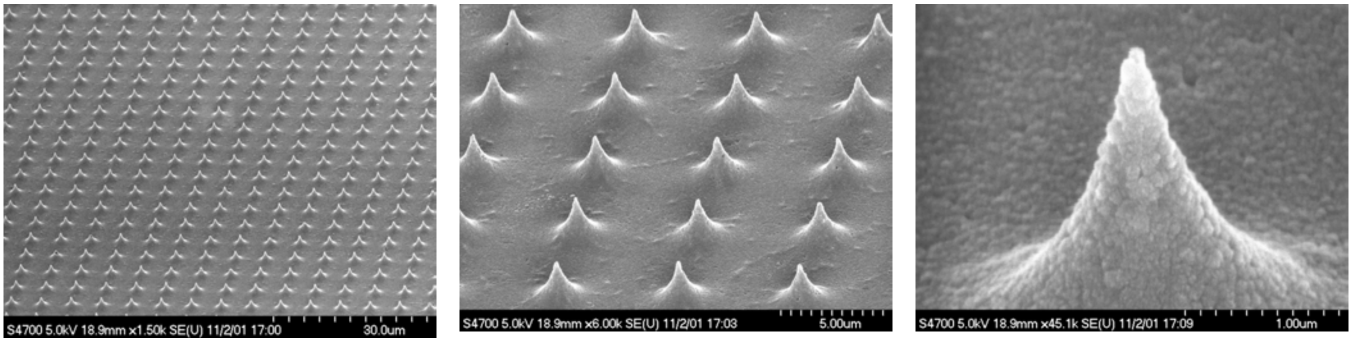


Figure C23 The same silicon array coated with uniform diamond film

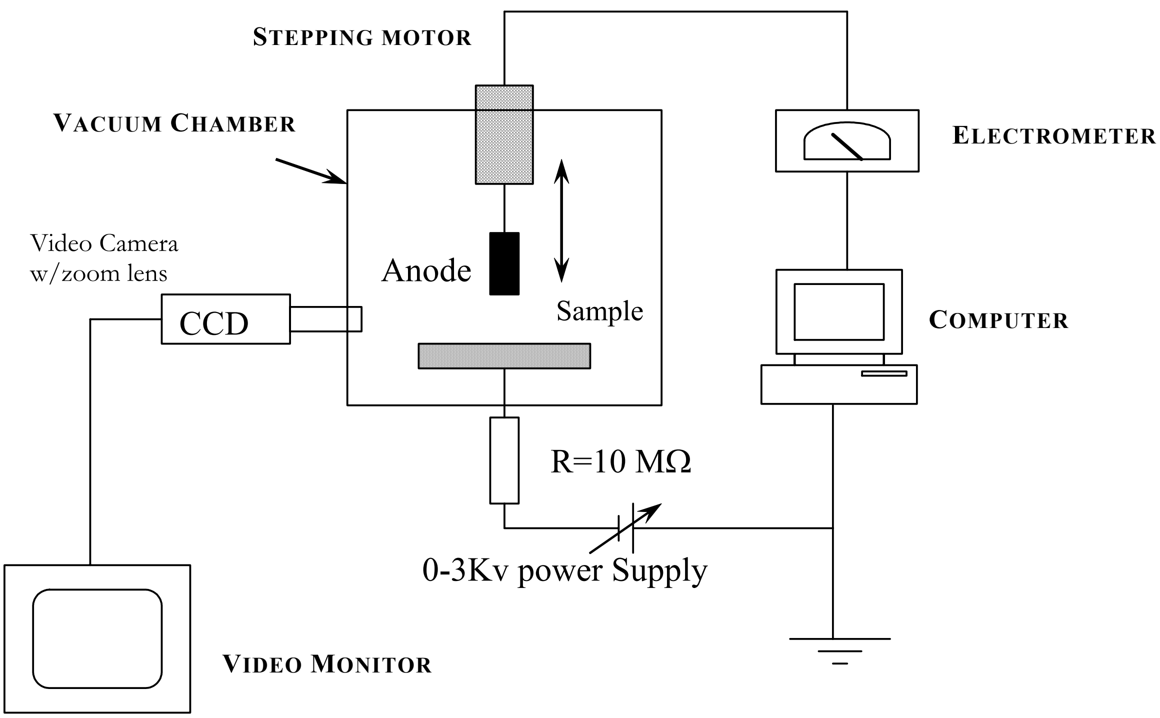


Figure C24. Measurement system to obtain I-V characteristics of diamond coated silicon arrays

Figure C24 Shows the measurement setup used to investigate the field emission characteristics before and after coating. The setup consists of a computer-controlled current-voltage testing system. The emission current was measured using an anode of 2mm in diameter with rounded edges to suppress arcing at sharp edges. The anode-cathode (tip emitter) spacing was determined by using a high magnification charge coupled device (CCD) camera. The anode voltage was increased under computer control until the emission current reached a preset value (usually 10^{-5} A) and then decreased to zero.

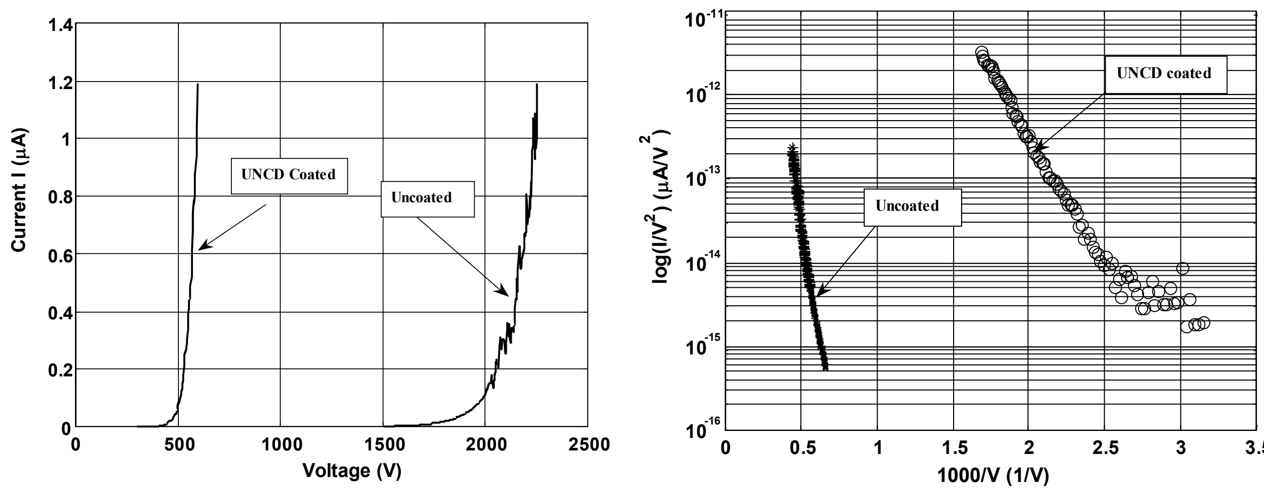


Figure C25. I-V and Fowler-Nordheim characteristics of uncoated and UNCD coated field-emission array

Figure C25 shows the I-V and F-N characteristics of silicon field emitter array before and after the UNCD coating. The UNCD-coated microtips exhibit very low emission threshold field (~ 2-3 V/μm) and stable emission current, as compared to uncoated Si tips.

C.4.5. Effect Of Gases on the Field Emission Properties of UNCD Coated Silicon Field Emitter Arrays

We performed studies of electron emission from ultra nano-crystalline diamond (UNCD)-coated ungated silicon field emitter during in situ exposure to various gases during I vs. Time measurements. The emission characteristics of the coated tip arrays were studied in the diode configuration, using an anode (2 mm diameter) with rounded edges to suppress arcing as seen in Fig 24. Significant enhancement of the electron emission was observed after the emitting surface was exposed to hydrogen at pressures in the 10^{-5} and 10^{-4} Torr range as seen from Figure C26. The initial current of about 2 μA increased by a factor of about 2.7 to 4, followed by subsequent current decrease to the initial value. The emission current then remained stable at 2 μA upon evacuating the hydrogen to a vacuum of $1x10^{-9}$ Torr. The repeatability of the emission current variation as a function of hydrogen exposure indicates that the effect is due to hydrogen exposure. The emission current practically did not change when exposing the emitter array to up to 10^{-5} Torr. Exposure to N_2 resulted in reduction of the emission current for ambient of up to 10^{-5} Torr as seen in Figure C27. This effect was reversible as the emission

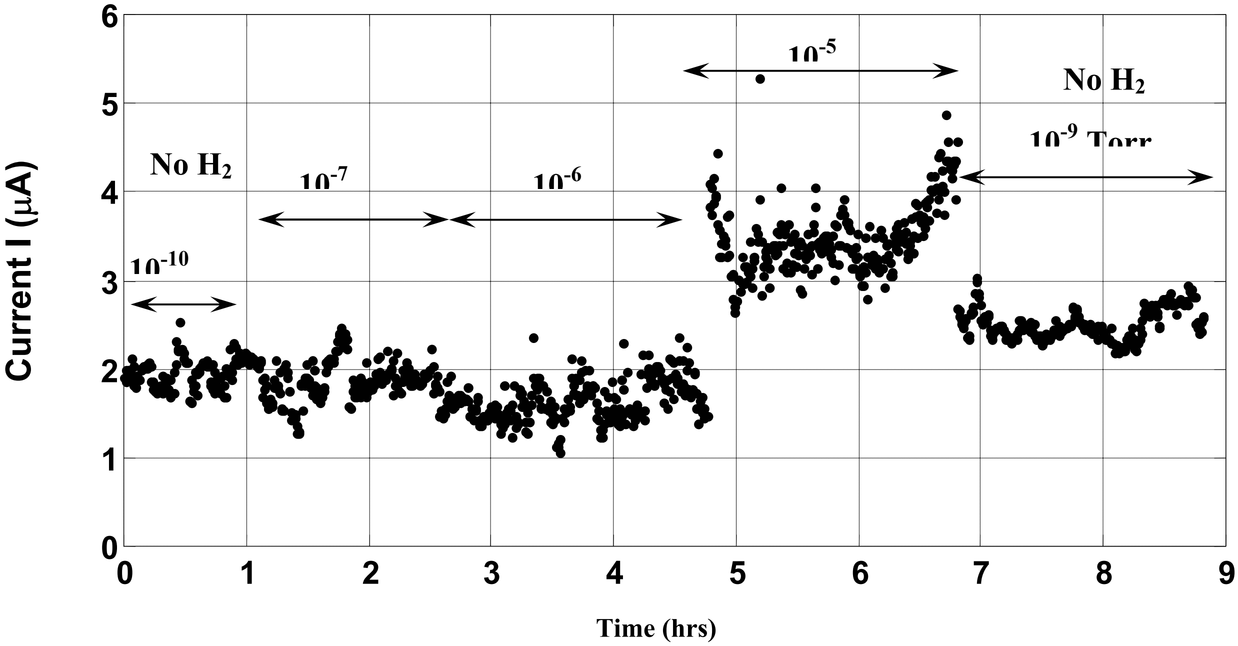


Figure C26: Plot of the emission current levels from UNCD coated silicon emitter array in Hydrogen atmosphere at three different pressures $1x10^{-7}$, $1x10^{-6}$, $1x10^{-5}$ Torr.

The last two hours for each experiment is plotted current attained its original value after nitrogen was pumped out and the background pressure in the chamber reached the original value of 8×10^{-10} Torr. The effect of the investigated gases on the emission characteristics of UNCD-coated Si tip arrays can be attributed to a modification of the effective work function at the localized sites from where electrons are being emitted.

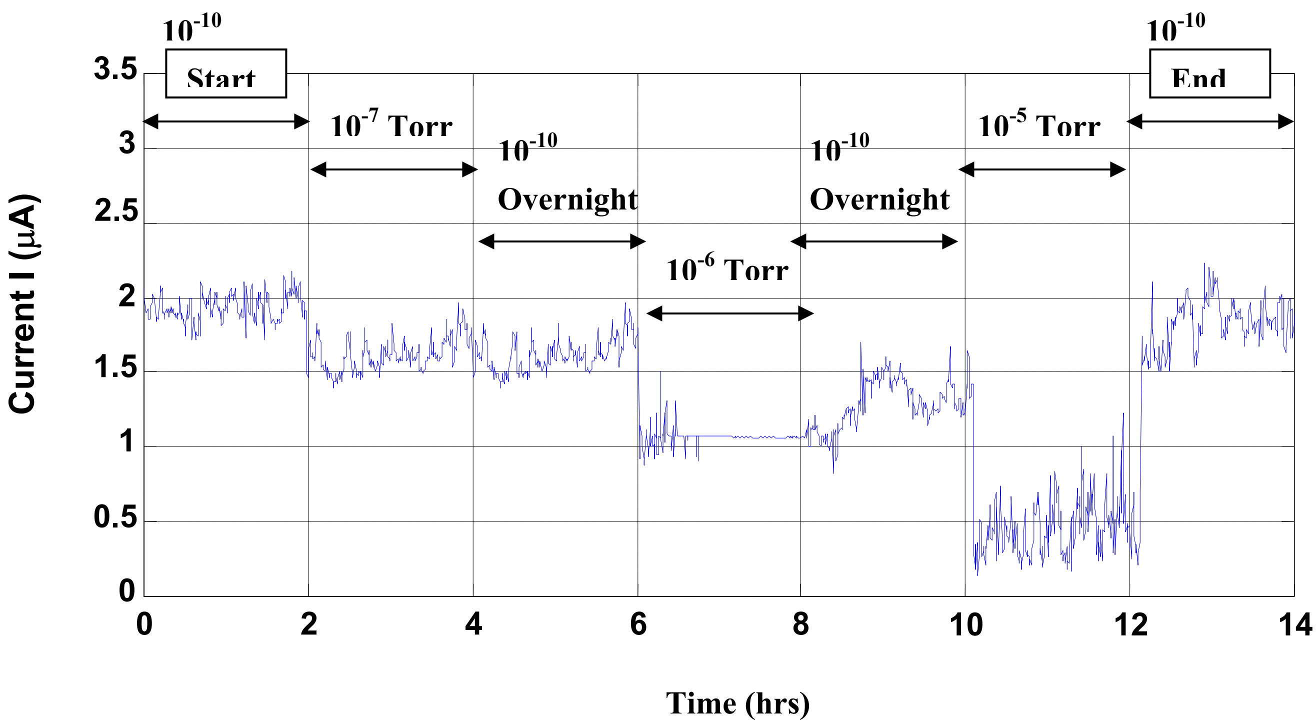


Figure C27: Plot of the emission current from UNCD coated silicon emitter array in Nitrogen atmosphere at three different pressures 1x10^{-7}, 1x10^{-6}, 1x10^{-5} Torr.

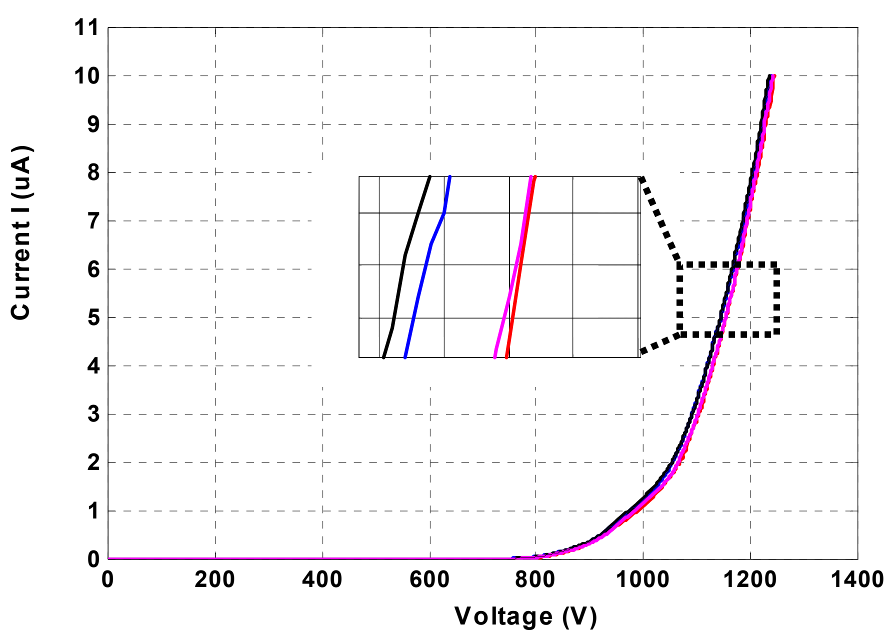


Figure C28 I-V Characteristics (after 240 hrs Operation)

Figure C28 Shows a set of two up and down sweep IV characteristics after 240 hrs of operation. The inset shows that there is no hysteresis, the curves are reproducible. In spite of emission properties of the diamond coated array dropping down during 240 hours of operation as seen Figure C29, it's still much better then clean silicon. Also, current stability and reproducibility improved significantly.

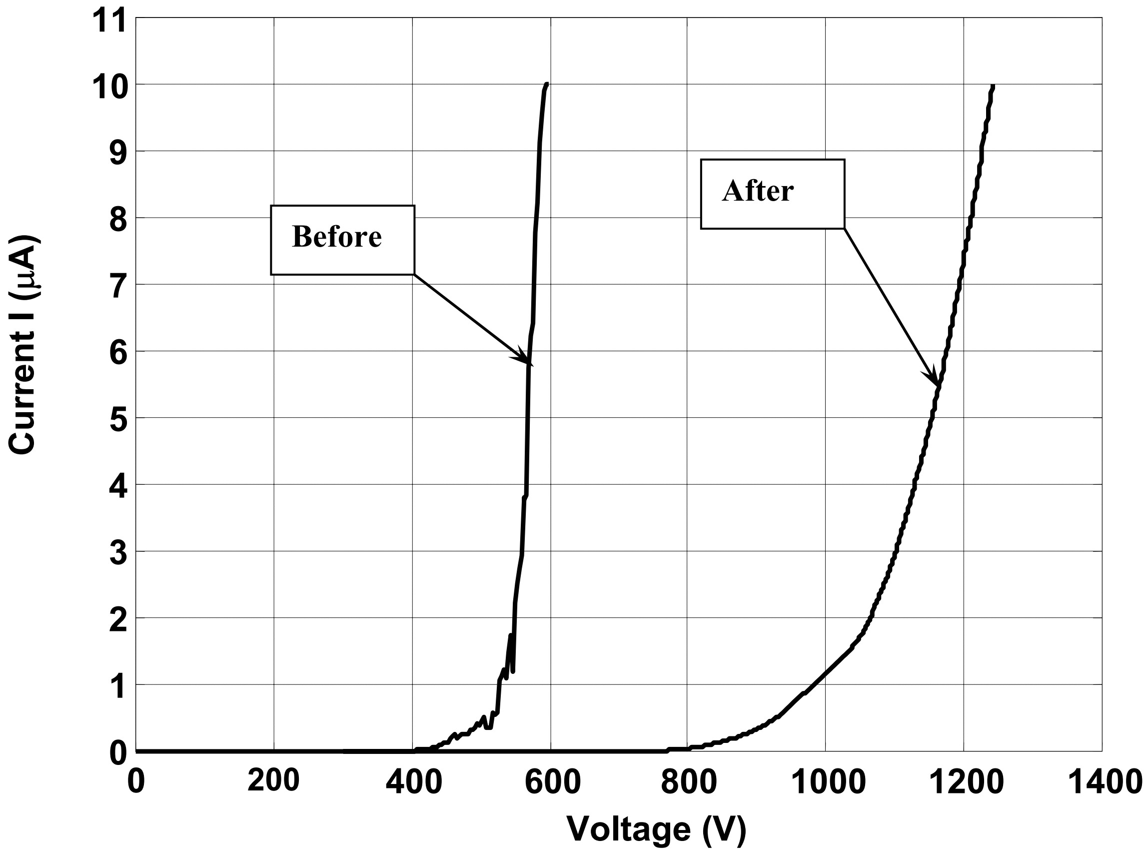


Figure C29 I-V Characteristics (Before and After 240 hrs of operation)

C.5. Study of Field Emission Characteristics from Silicon Field Emitter Arrays Coated with Ferroelectric Material

C.5.1. Deposition Process

The PZT thin film studied had the composition Pb ($Zr_{0.52}$ $Ti_{0.48}$) O_3 and were prepared by the sol-gel method. The PZT thin films were synthesized using a modification of the sol-gel procedure described by Budd, Dey, & Payne [15] using lead acetate trihydrate, titanium-IV isopropoxide, and zirconium-IV propoxide as precursors and 2-methoxyethanol as a solvent. Additionally, 4 vol % formamide was added as a drying control agent after refluxing the above solution. The resultant PZT solution had a concentration of 0.4 M. Additional information on the process has been reported elsewhere [16].

The substrates used for this investigation were 2.5cm x 2.5cm die with an active area of 1cm x 1cm array of Si emitters fabricated as discussed above. A syringe with a 0.1 μm Whitman filter was used to deposit PZT sol-gel solution onto the stationary substrate prior to spinning for 30 seconds at 2500 rpm. Next, the film was pyrolyzed on a hotplate at 350°C for 2 minute. After the pyrolysis, the films were crystallized using the Heatpulse model 610, rapid thermal annealing furnace using a dwell at 700°C for 30 seconds. The deposition continued for up to 3 layers on three different samples.

The emitters coated with PZT thin film were analyzed by SEM. The SEM images as seen in Figure C30, Figure C31 and Figure C32 shows the emitter surface coated with one, two and three layers of PZT thin films. Figure C30a shows the image of one layer PZT thin film coated sample. It can be seen from the image that the coating is not crack free. The cracks arise due to the stress in the film during the crystallization process. This stress is due to the difference in the coefficient of thermal expansion coefficient of silicon and the PZT thin film. The no. of cracks increases and deepens as the no. of coating layer increases as seen from the Figure C31a and Figure C32a. It is observed from the SEM images above that the Si emitter array coated with a single layer of PZT thin film of thickness 0.1μm preserves the shape of the emitters. As the number of layers of PZT thin film coating increases, it introduces artifacts around the emitters and does not preserve the shape of the emitters as seen in Figure C31c and Figure C32c

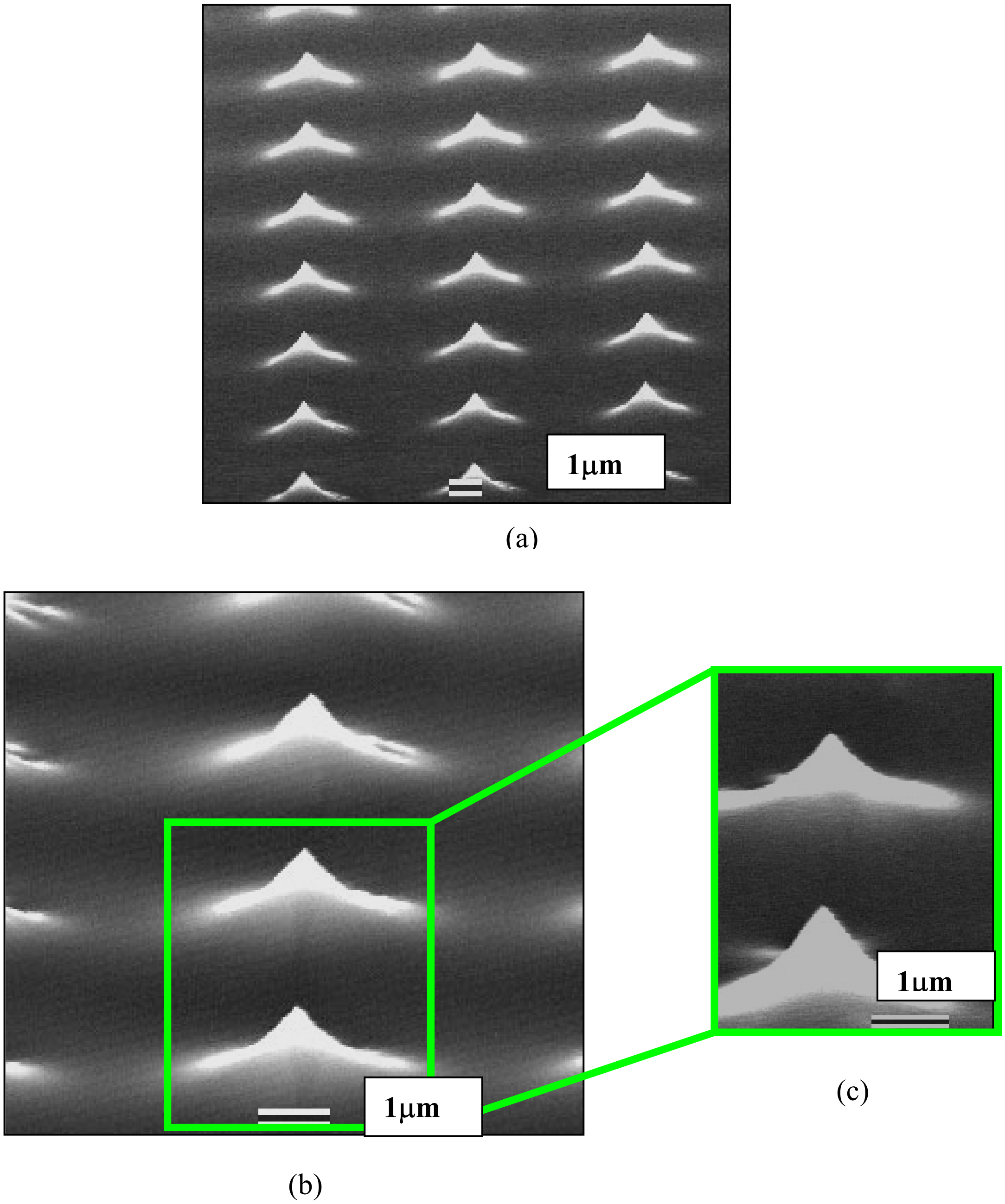


Figure C30: SEM of 1-Layer PZT thin film coated silicon emitter array

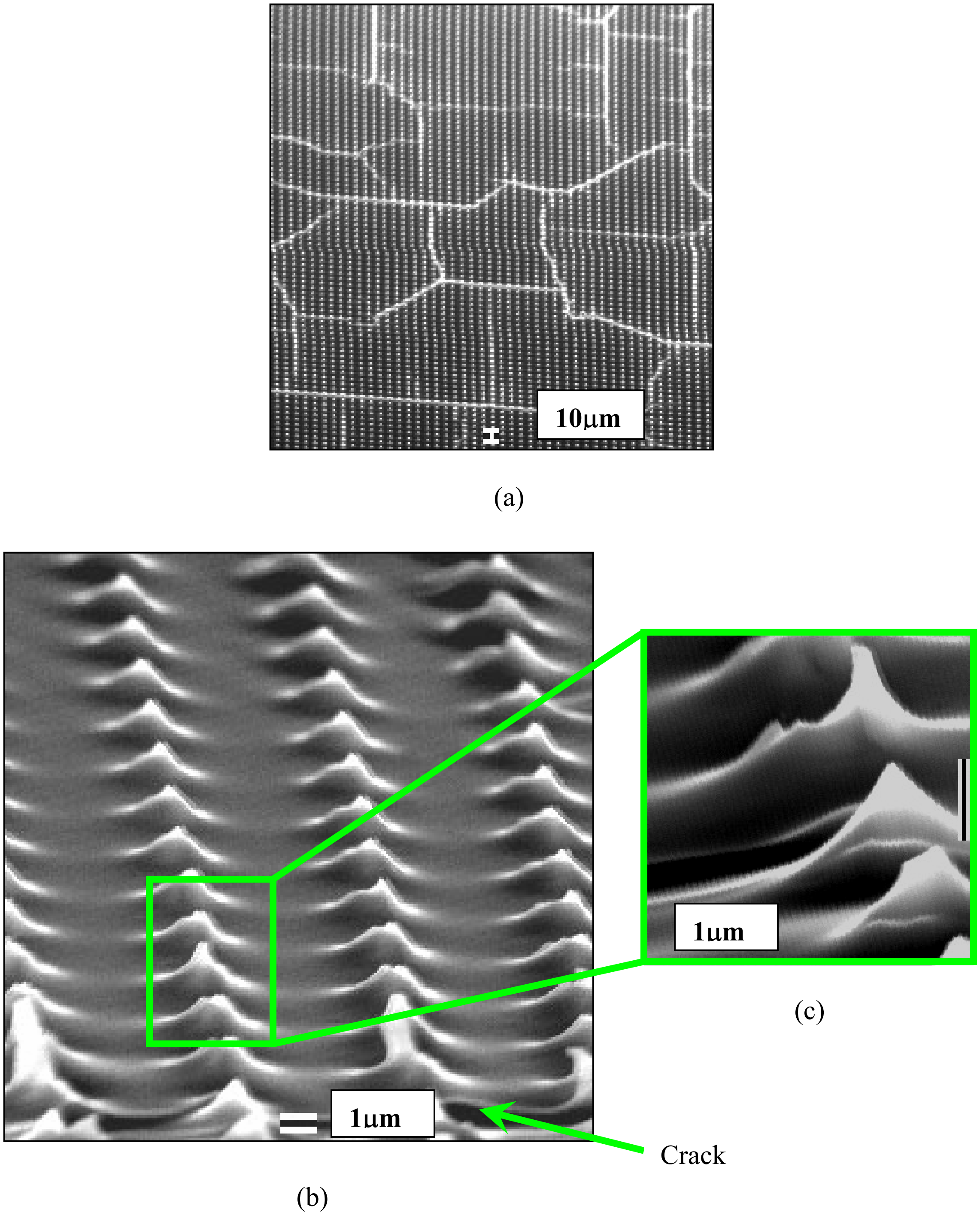
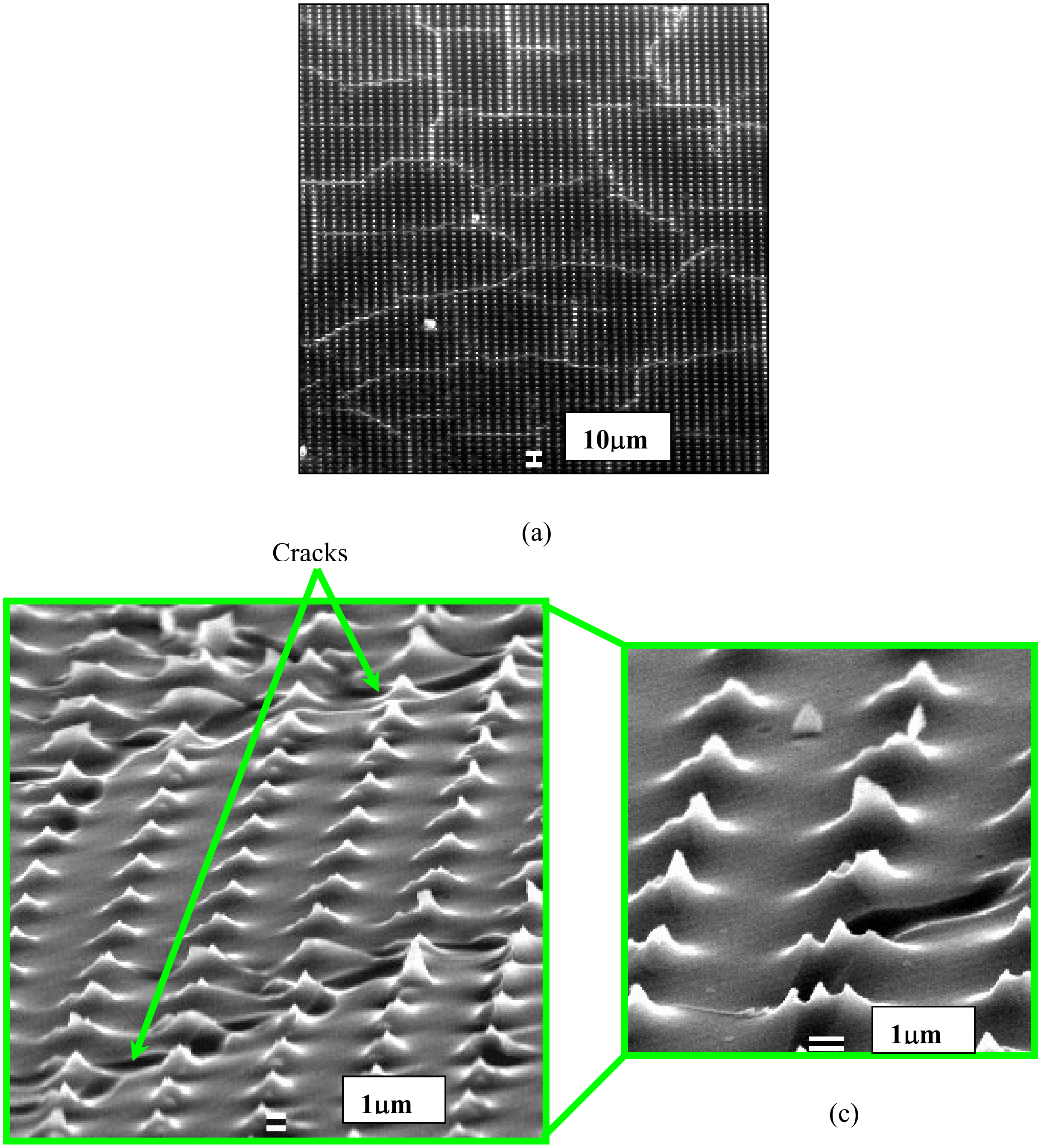


Figure C31: SEM of 2-Layer PZT thin film coated silicon emitter array



(a)

(b)

(c)

Figure C32: SEM of 3-Layer PZT thin film coated silicon emitter array

C.5.2. Measurement Setup

Field emission properties of the bare and coated cathodes were measured in a stainless steel vacuum chamber under a residual gas pressure of 10^{-8} Torr. The Hewlett-Packard 4142B modular DC source/monitor was used to acquire the emission data. A positive potential (to 1000 volts) was applied to the anode, and the cathode was grounded. The anode used here was a stainless steel rod of diameter 1.25mm connected to an adjustable manipulator. The cathode is mounted on a copper plate to ensure electrical contact, which in turn is mounted on a fixed manipulator. Moving the anode back and forth can change the gap between the anode and the cathode.

The field emission properties of the bare cathodes were measured after the tips were conditioned overnight under a constant DC bias of 900V at a current level of about 1μA. The conditioning of the emitters is also known as the forming process. The forming process is associated with the removal of the native oxide, burn off the fine protrusions (artifacts of the etching process) on the surface of the emitters and possible surface impurities, which helps to achieve stable and reproducible emission current showing linear Fowler-Nordheim characteristics. After the initial emission measurements, the silicon emitter arrays were coated with one, two and three layers of PZT thin film by the sol-gel process discussed above. As seen from the SEM images the sample coated with one layer of PZT thin film preserved the structure of the emitters in the array, hence we decided to study and compare the field emission properties of silicon emitter array before and after coating.

C.5.3. Results and Discussion

The I-V characteristics as seen in Figure C33a correspond to the two curves measured before and after the experiment. The anode-cathode gap for the experiment was about 20μm It is seen from the plots that at anode voltage of 600 V, the emission current from the array decreased from 4.22μA for bare Si emitters to 0.125μA for one layer PZT coated Si emitters. The turn-on voltage increased from 533 V to 829 V after coating the emitter surface. Turn-on voltage is defined as the anode voltage applied to achieve a current level of 1μA. In other words, the electric field reduces from 26.65 V/μm for untreated to 41.45 V/μm for treated emitter surface. Figure C33b confirms the occurrence of F-N tunneling current since the plot of ln (I/V^2) versus 1/V forms a linear line. The slope of the F-N curve increased from 5.33 A/V for bare emitters to 10.35 A/V after surface coating.

The above-obtained I-V measurement from the coated sample was taken by applying a constant electric field to the cathode. As we know that field emission (FE) occurs in ferroelectric materials under continuous external perturbation of the ferroelectric crystal, such as temperature variation, mechanical stress, reorientation of polar axis, etc. that leads to disturbance of the initial charge equilibrium and to the appearance of an unscreened charged and an electrostatic field at the free polar surface. Thus, FE is generated from a nonequilibrium charged ferroelectric surface. As in the present experiments, the PZT thin film is under a constant electric field, here we did not take advantage of the FE properties of the ferroelectric material. Hence we don’t see any improvements in the emission characteristics of the coated array when compared to the bare, uncoated array. We can obtain high density FE current from ferroelectric materials by fast switching of the polar axis and this can be done under a pulse electric field. At present emission measurements are being carried out under this condition.

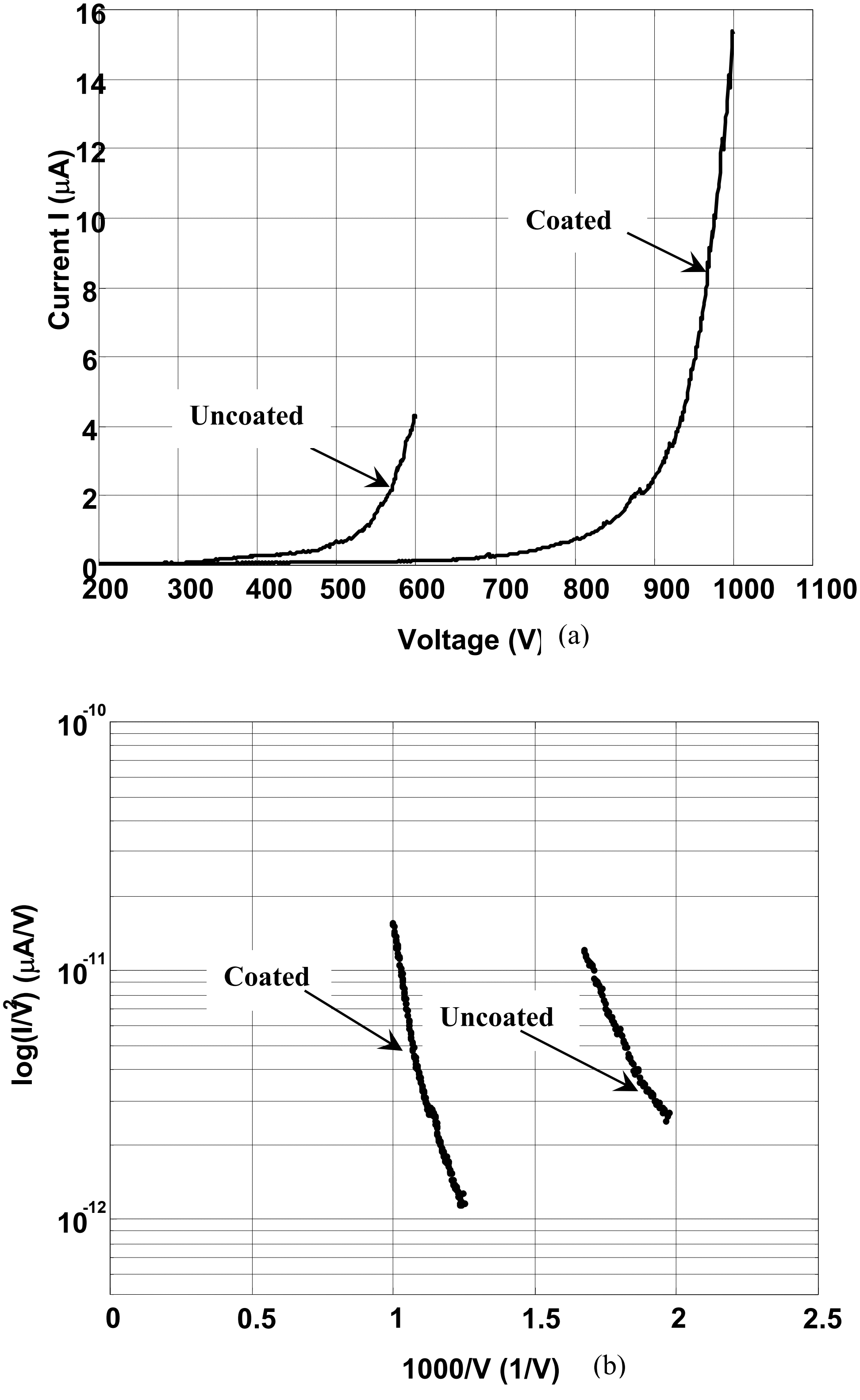


Figure C33: (a) I-V characteristics (b) FN characteristics of bare (uncoated) and one layer PZT coated silicon emitter array

C.6. PUBLISHED ARTICLES

N.N. Chubun, A.G. Chakhovskoi, C.E. Hunt and M. Hajra Fabrication and characterization of singly-addressable arrays of polysilicon field-emission cathodes, Solid State Electronics, 45 (2001), pp.1003-1007

N.N.Chubun, A.G.Chakhovskoi, M.Hajra, C.E.Hunt Field Emission Characterization of the 10x10 Singly-Addressable Double-Gated Polysilicon Tip Array. Proceedings of the 14th Int. Vacuum Microelectronics Conference, Aug 12-16, 2001, Davis, CA, p.137-138.

M.Hajra, N.N.Chubun, A.G.Chakhovskoi, C.E.Hunt, K.Lui, A.Murali, S H. Risbud, T.Tyler, V.Zhirnov Field Emission Characterisation of Silicon Tip Arrays Coated with GaN and Diamond Nanoparticle cluster, Proceedings of the 14th Int. Vacuum Microelectronics Conference, Aug 12-16, 2001, Davis, CA, p. 121-122.

N.N. Chubun, A.G. Chakhovskoi, M. Hajra, and C.E. Hunt, Double-Gated Singly-Addressable Polysilicon Tip Array Fabrication And Characterization MRS 2001 Spring meeting abstracts, p.96

M.Hajra, N.N.Chubun, A.G.Chakhovskoi, C.E.Hunt, K.Liu, A.Murali, S H. Risbud, T.Tyler and V.Zhirnov. Field Emission Characteristic Of Silicon Cathodes Coated With GaN Nanoparticles MRS 2001 Spring meeting abstracts, p.97

M. Hajra, N.N. Chubun, A.G. Chakhovskoi, and C.E. Hunt Surface Treatment on Silicon Field-Emission Cathodes Mat. Res. Soc. Symp. Proc. Vol.621, Warrendale, PA, 2001, R1.4.1-5.

C.7. REFERENCES

J.T. Trujillo and C.E. Hunt, "Fabrication of Silicon Field Emission Points for Vacuum Microelectronics by Wet Chemical Etching," *Semicond. Sci. Technol*, vol. 6, pp. 223-225, 1991.

R.B. Marcus, T.S. Ravi, T. Gmitter ,K. Chin, D. Liu, W.J. Orvis, D.R. Ciarlo, C.E. Hunt, J.T. Trujillo, "Formation of silicon tips with <1 nm radius," *Appl. Phys. Lett.*, vol. 56, no. 3, pp 236 - 238, Jan. 15, 1990.

C.E. Hunt, J. T. Trujillo, and W. J. Orvis, “Structure and electrical characterization of silicon field-emission devices,” IEEE Trans Electron Devices, vol. 38, no. 10, pp2309-2313, 1991.

M. W. geis, D. C. Flanders, D. A. Antoniadis and Henry I. Smith, “Crystalline silicon on insulators by graphoepitaxy,” IEDM Technical Digest, pp 210-212, 1979, Washington D.C.

W. D. Kesling and C. E. Hunt, “Field-Emission Display Resolution”, SID 93 Digest, pp 599-602, Society for Information Display, 1993.

J. T. Trujillo and C. E. Hunt, low-voltage silicon gated field-emission cathodes for vacuum microelectronics and e-beam applications, JVST B, 11 (2), 1993, pp. 454-458,

J.H. Lee, S.W. Kang, S.G. Kim, Y.H. Song, K.I. Cho, H.J. Yoo A New Fabrication method of Silicon Field Emitter Array with Local Oxidation of Polysilicon and Chemical-Mechanical-Polishing. Proceedings of the 9th International Vacuum microelectronics Conference, July 7-12, 1996, St. Petersburg, Russia, pp.415-418.

E.C. Boswell, S.E. Huq, M. Huang, P.D. Prewett, P.R. Wilshaw, Polycrystalline silicon field emitters. JVST B 14(3) May/Jun 1996, pp. 1910-1913.

H.S. Uh, S.J. Kwon, J.D. Lee Process design and emission properties of gated n^+ polycrystalline silicon field emitter arrays for flat panel display applications. JVST B 15(2) Mar/Apr 1997, pp J. 472-476.

M. Ding, H. Kim, and A.I. Akinwande, High Uniformity and Low Turn-on Voltage Si FEAs Fabricated with CMP. Proceedings of the 12th International Vacuum microelectronics Conference, July 6-9, 1999, Darmstadt, Germany, pp.370-371.

J.T. Trujillo, A.G. Chakhovskoi and C. E. Hunt, Low voltage silicon field emitters with gold gates, Proceedings of the 8th International Vacuum Microelectronics Conference, Portland, OR, July 30-Aug. 3, 1995, pp. 42-46.

J. T. Trujillo and C. E. Hunt*, low-voltage silicon gated field-emission cathodes for vacuum microelectronics and e-beam applications*, JVST B, 11 (2), 1993, pp. 454-458,

R.Meyer, presented at the 9th IVMC Conference, Kyongju, Korea, 1997 (unpublished).

Advanced Porous Getters. St 172 Series. Technical publication G870530. SAES getters S.p.a. Milano, 1987

K. D. Budd, S. K. Dey, and D. A. Payne, *Sol-Gel Processing of $PbTiO_3$, $PbZrO_3$, PZT, and PLZT Thin Films*, British Ceramic Processing, Vol. 36, pp. 107-21, 1985.

F. Chu, T. Su, and S. Trolier-McKinstry, *Effect of Thickness and Texture on the Ferroelectric Properties of Lead Zirconate Titanate Thin Films by Sol-Gel Processing*, Proc. The 8th US-Japan Seminar on Dielectric and Piezoelectric Ceramics, pp. 120-3, 1997.