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13. ABSTRACT (Maximum 200 words)

"Report developed under STTR contract" for topic "ARMY02-T005". We have investigated the feasibility of using self-aligning kinematic optoelectronic mounts for active 3-D RF/optoelectronic microstructures. The mechanical interconnect features allow rapid and very precise assembly of multiple silicon layers into rigid structures with self-assembling electrical and thermal pathways. The major thrust of this Phase I investigation was to study these interconnects to determine their mechanical registration precision, heat removal capacity, and ability to couple high frequency RF electrical signals between the multiple layers. The results of our electrical simulations demonstrate that the electrical interconnect performance of these layered optoelectronic circuits should be excellent for designs up to at least 20 GHz using finite-ground coplanar waveguides. Solder columns, which are integral to the electrical interconnect structures between layers, are also excellent thermally conductive paths that allow the heat generated by RF circuitry to be removed. Passive placement of multimode fiber optic components should be possible based on our tests and modeling of the precision mechanical interconnects. These investigations indicate that layered, RF optoelectronic microstructures with precision mechanical interconnects should have excellent thermal, electrical and optical performance while benefiting from direct compatibility with existing planar RF devices and ease of manufacture.

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1 Executive Summary

We have investigated the feasibility of using self-aligning kinematic optoelectronic mounts for active 3-D RF/optoelectronic microstructures. The mechanical interconnect features allow rapid and very precise assembly of multiple silicon layers into rigid structures with self-assembling electrical and thermal pathways. The major thrust of this Phase I investigation was to study these interconnects to determine their mechanical registration precision, heat removal capacity, and ability to couple high frequency RF electrical signals between the multiple layers.

The results of our electrical simulations demonstrate that the electrical interconnect performance of these layered optoelectronic circuits should be excellent for designs up to at least 20 GHz using finite-ground coplanar waveguides. These structures are easy to pattern and route and can be cascaded to multiple layers with minimal effect on return loss. The cascade structures we modeled included solder columns from level-to-level and metallized vias from side-to-side of a single silicon layer. More careful design could push beyond the 20 GHz barrier, but we did not have adequate confidence in our simulations above 20 GHz.

Solder columns, which are integral to the electrical interconnect structures between layers, are also excellent thermally conductive paths that allow the heat generated by RF circuitry to be removed. With four layers of circuitry, each dissipating 100 mW, the peak temperature excursion was only 5.2 C above ambient with appropriate solder volumes between layers and worst-case thermal resistance at silicon-to-silicon interfaces. Increasing the dissipation of one layer to 1000 mW increased the peak temperature excursion to 25.2 C above ambient. These figures allow considerable headroom for various active devices.

Passive placement of multimode fiber optic components should be possible based on our tests and modeling of the precision mechanical interconnects. These investigations indicate that layered, RF optoelectronic microstructures with precision mechanical interconnects should have excellent thermal, electrical and optical performance while benefiting from direct compatibility with existing planar RF devices and ease of manufacture.

Although a manufacturing analysis was not part of this study, in prior work we assembled passive prototype devices using these microstructures at a rate of 12 parts per minute. The benefit of these structures is their inherent compatibility with the existing manufacturing infrastructure of pick-and-place components.

2 Analysis of Interconnects

Shown schematically in Figure 1, Avanti Optics' silicon micro-machined structures can be patterned with planar RF and optoelectronic devices to assemble 3-D RF optoelectronic microstructures. These micro-machined structures are compatible with existing microelectronic manufacturing methods and are designed for precise automated placement by conventional pick-and-place robots.

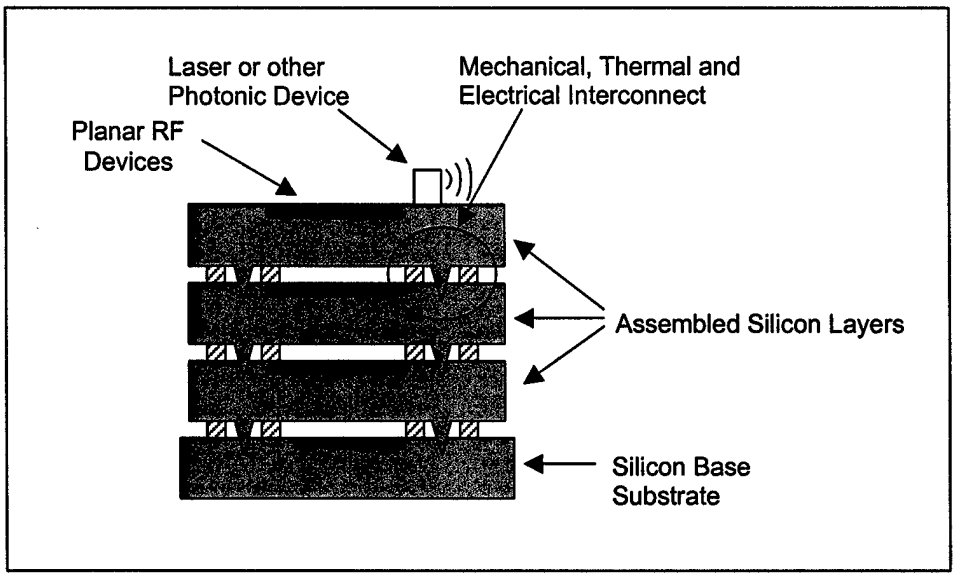


Figure 1. Schematic of layered, 3-D RF microstructure with kinematic interconnect.

Figure 2 shows an enlarged view of a layer-to-layer interconnect. V-grooves and mesa-like features are anisotropically etched into {100} oriented silicon as appropriate to form the kinematic mechanical interconnects. The solder columns form electrical interconnects between layers, may be used to mechanically attach the layers, and also provide thermally conductive paths between the layers. The mechanical, thermal, and electrical performance of these interconnects is presented in the following sections in order to determine the feasibility of using the layered approach, as shown in Figure 1, to build 3-dimensional RF optoelectronic microstructures.

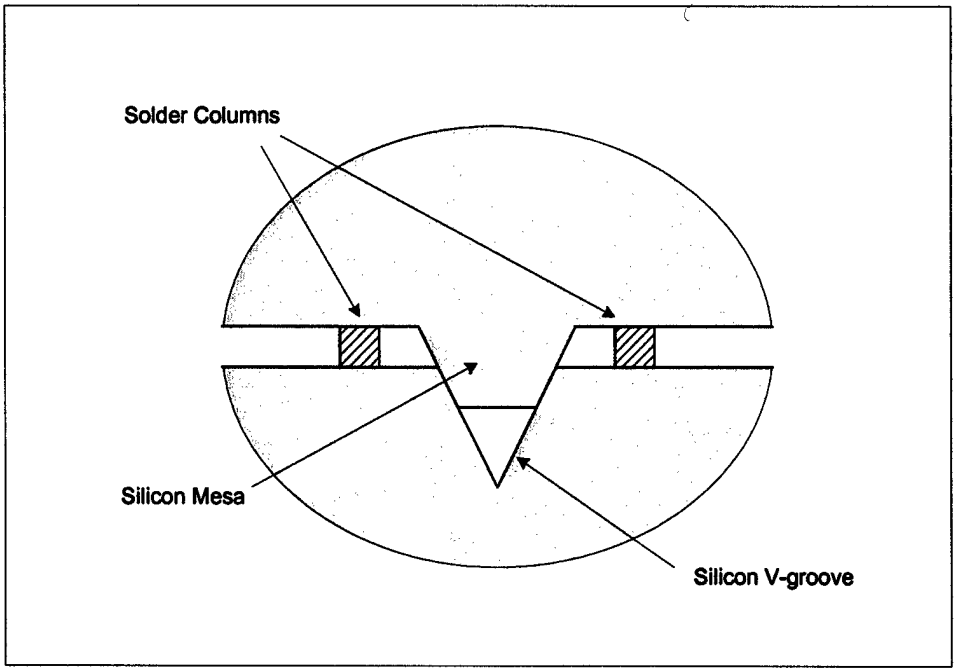


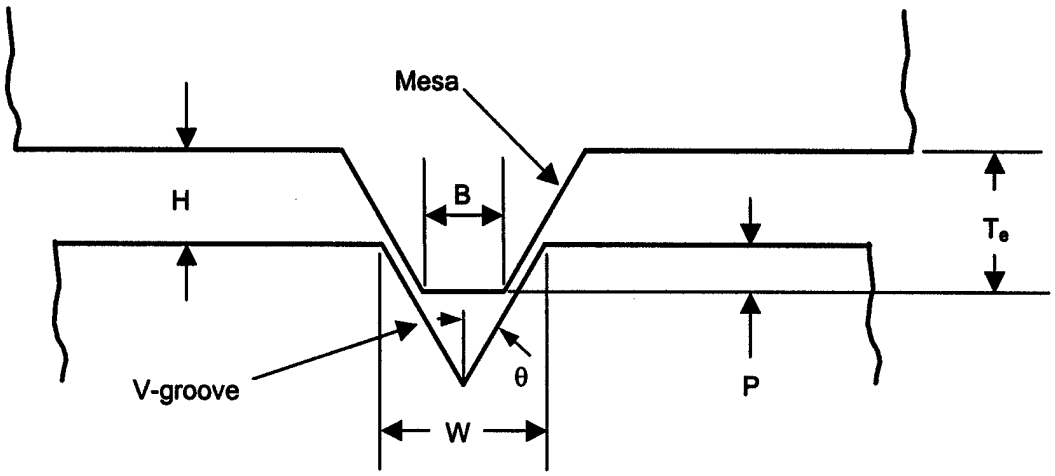
Figure 2. Enlarged view of a layer-to-layer interconnect.

3 Mechanical Interconnects

The kinematic interconnect features allow rapid assembly of multiple silicon layers. We have attempted to define the expected mechanical precision level of assembling multiple silicon layers through a number of tests, models, and analyses. A set of relationships was derived to determine the effects of dimensional changes in the kinematic features, tests were performed to determine how repeatable the kinematic mounting features could be mated together, and a Monte Carlo computer simulation was developed to statistically predict the variations in position of the laser or photonic device based on these tests and relationships.

3.1 Effect of V-groove and Mesa Width Errors

A set of simple relationships was developed to model the effects of silicon v-groove and silicon mesa width tolerances. Shown in Figure 3 are the definitions of the kinematic mount using anisotropically etched silicon. The etch angles of the mesa and v-groove are controlled by the crystal orientation of the silicon.



H = Separation of Stacked Layers
P = Penetration of mesa into substrate
B = Mesa width
W = V-groove width
Te = etch depth
θ = V-groove half angle (35.26 deg)

Figure 3. Kinematic seating definitions

$H = T_e - (W - B) / (2 \tan \theta)$,
$P = (W - B) / (2 \tan \theta)$.

The sensitivity of H and P to changes in v-groove width is given by:

$\Delta H = - \Delta W / 2 \tan \theta \cong -0.7 \Delta W$,
$\Delta P = \Delta W / 2 \tan \theta \cong 0.7 \Delta W$.

So, for example, if the v-groove width, W, increased by 0.5 μm, the upper layer would seat lower by about 0.35 μm.

The sensitivity of H and P to changes in mesa width, B, is given by similar equations.

$\Delta H = \Delta B / 2 \tan \theta \cong 0.7 \Delta B$,
$\Delta P = -\Delta B / 2 \tan \theta \cong -0.7 \Delta B$.

3.2 Effect of Foreign Particulate in the Kinematic Mount

Dust or other contaminants in the kinematic mount will shift the seating position. The effect of a dust particle is shown in Figure 2. A particle of size D will shift the seating location by the amounts:

$\Delta X = D \cos\theta,$
$\Delta Y = D \sin\theta,$

where θ is given by the v-groove half-angle of 35.26 degree. For example, a 1.0 μm dust particle will shift the seating location by 0.58 μm in the vertical direction and 0.82 μm in the lateral direction.

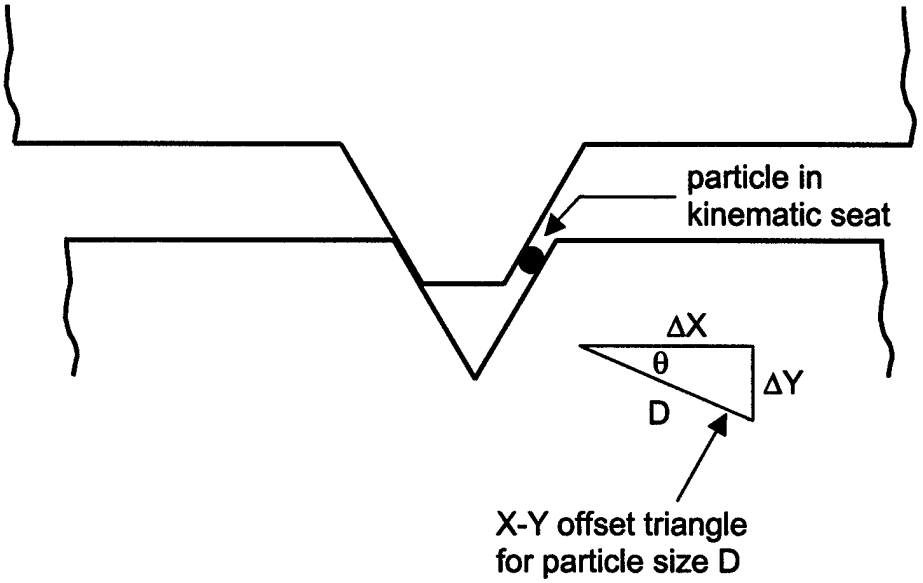


Figure 4. Effect of dust particle on kinematic seat.

3.3 Kinematic Insertion Repeatability Tests

A true kinematic mount would have six points of contact between two mating objects to precisely locate the two objects in six degrees of freedom (X, Y, Z, θ_X, θ_Y, and θ_Z) relative to each other. If there are more than six contact points, then the mount is over-constrained and it is possible for the two objects to seat at multiple different positions relative to one another. The micro-machined v-groove and mesa silicon features used to form the Avanti Optics' "kinematic" mount have six small planar contacts and hence the mount is slightly over-constrained. We performed a number of insertion repeatability tests to determine the likely mating errors due to the slightly over-constrained mounts and to help quantify the expected mechanical precision level of assembling multiple silicon layers. The variables that we found had an affect on the repeatability included:

- V-groove and mesa layout and dimensions
- Amount of initial offset between mesas and v-grooves
- Vibrational assistance

3.3.1 Kinematic Seating Measurement Fixtures

A schematic of the measurement fixture that was used to determine how repeatable our micro-machined silicon layers would mate together is shown in Figure 5. The manual translation stages are used to start the engagement of the top and bottom silicon layers. A constant seating force is then applied to the top silicon layer. The top silicon layer can slip side-to-side and rotate slightly on the vacuum nozzle to help the engagement of the two layers. A small vibrational force can also be supplied to overcome the static friction between the small, planar silicon surfaces of the mesas and v-grooves. Two fibers are attached to the top and bottom silicon layers to determine the relative X and Y displacement of the top and bottom layers.

A fiber is attached to each of the upper and lower silicon layers in order to measure the repeatability of the insertion. To self-compensate for mechanical drift of the measurement system, a reference fiber is attached to the lower silicon layer. The difference in the two fiber locations, or delta spot, is measured as the upper silicon layer is seated into the lower layer.

To measure the difference in fiber locations a custom measurement system called a spot tracker is used. As shown in Figure 6, visible light is launched into the measurement and reference fibers. A high-resolution video system images the output of the two fibers. The data analysis computer records the difference, or delta spot, in the X, Y locations of the two fiber cores.

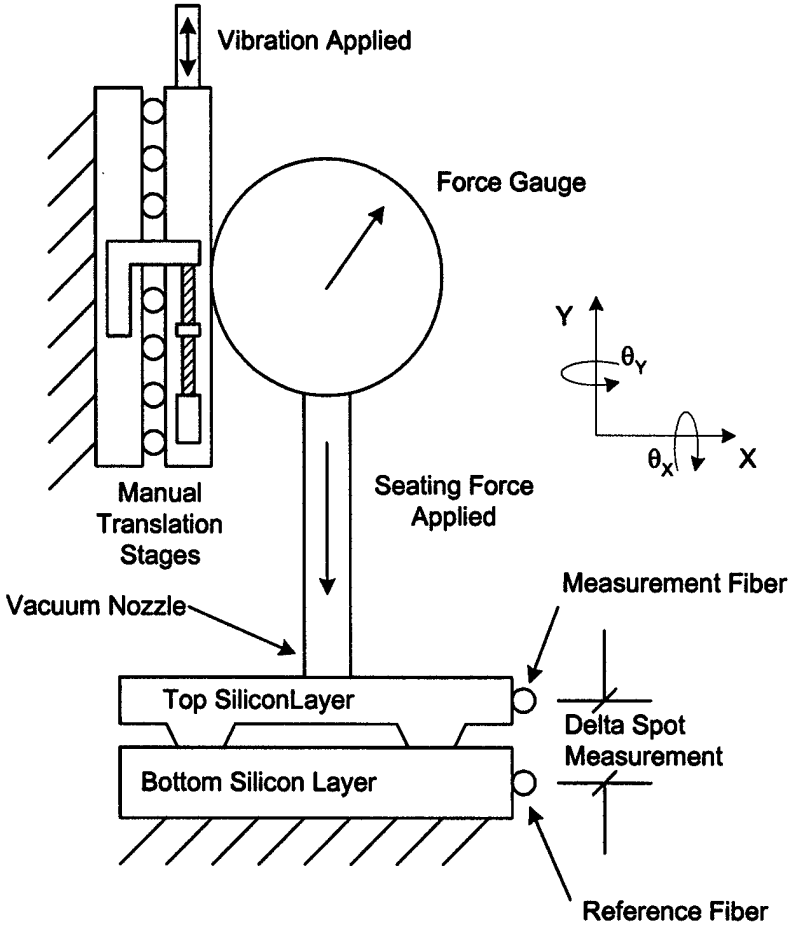


Figure 5. Schematic of kinematic seating test fixture.

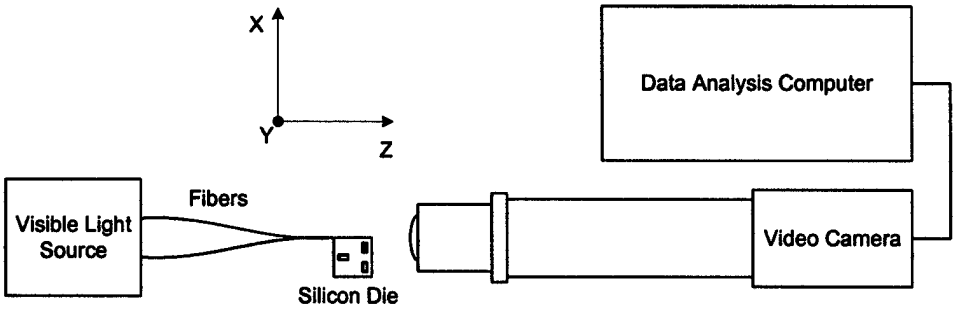


Figure 6. Spot tracking schematic.

3.3.1.1 Example Spot Tracker Output

Shown below in Figures 7 and 8 are example outputs from the spot tracking system for the Y and X-axes, respectively. The fiber core location data points are collected 5 times each second (this is programmable). In this example, the Y-axis had approximately 50 nm non-repeatability in the second and third insertions compared to the location where the top layer was initially seated. The X-axis had approximately 1.1 μm non-repeatability in the second and third insertions compared to the location where the top layer was initially seated.

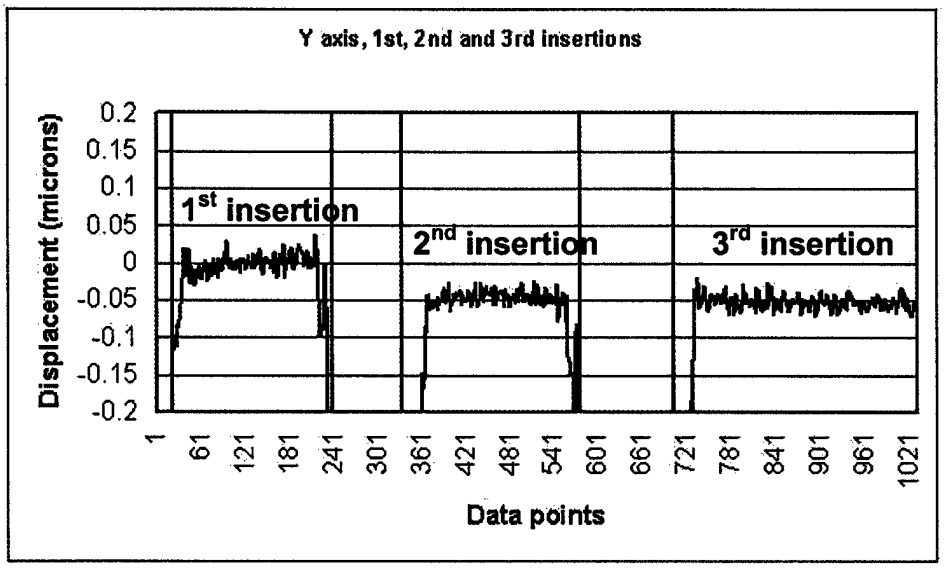


Figure 7 Spot tracker output: Y-axis displacement for multiple insertions.

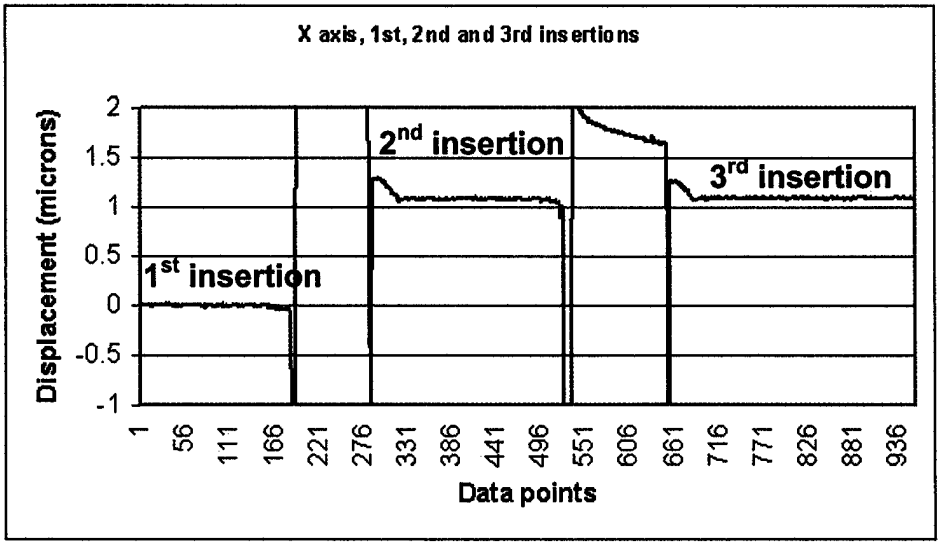


Figure 8. Spot tracker output: X-axis displacement for multiple insertions.

3.3.2 Silicon Part Layout

We performed kinematic insertion tests on two sets of micro-machined silicon parts that had different mechanical dimensions and layouts. The first tested set of silicon micro-machined parts had a mesa layout (and corresponding v-groove layout) as shown in Figure 9. The mesas have a design width of 200 μm and a length of 400 μm and are creatively referred to as the "large parts".

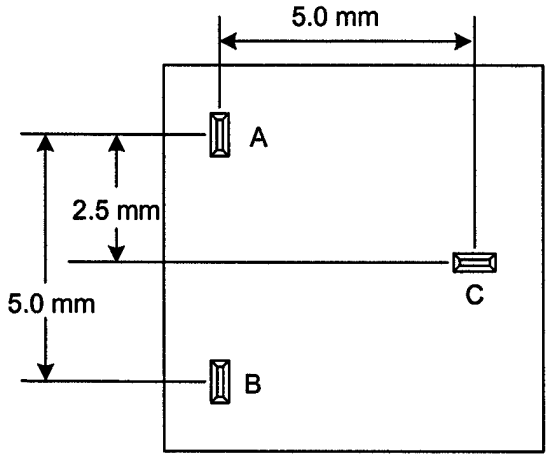


Figure 9. Large part mesa layout.

Figure 10 is a photographed sub-section of the anisotropically etched silicon substrate that mates with the silicon layer of Figure 9. The three larger v-grooves that approximately form an equilateral triangle are used for the kinematic registration features. A reference designator, T2, is also etched into the substrate and is used as an aid when manual placement is used.

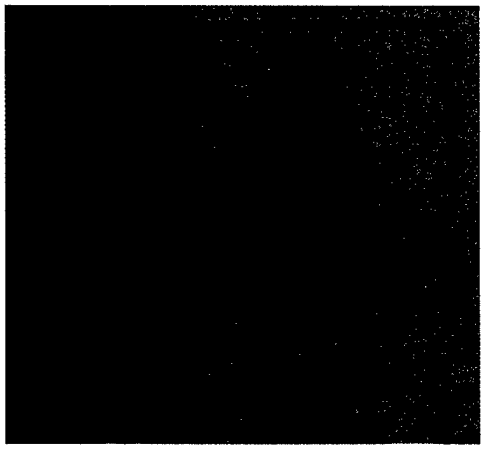


Figure 10. Photograph of silicon substrate.

The second set of silicon micro-machined parts that were tested had smaller dimensions than the previously tested parts and with mesa C spaced closer to mesas A and B. These parts had a mesa layout (and corresponding v-groove layout) as shown in Figure 11. The mesas have a design width of 110 μm and a length of 250 μm and are referred to as the "small parts".

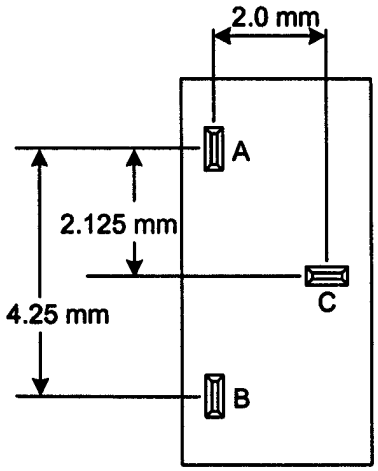


Figure 11. Small part mesa layout.

3.3.3 Kinematic Insertion Test Procedure

The insertion repeatability tests were performed as follows:

- A new set of parts is prepared with attached measurement and reference fibers.
- The mesas of the top silicon layer were inserted into the v-grooves of the bottom silicon layer.
- The spot tracking system was used to record the X, Y location of the measurement fiber relative to the reference fiber.
- Next, the top silicon layer was completely removed and then inserted back into the bottom silicon layer.
- The spot tracking system was used to record the new X, Y location of the measurement fiber relative to the reference fiber.
- The difference (or non-repeatability) in the X, Y locations between the 1st and 2nd insertions was recorded.

3.3.4 Large Part Kinematic Insertion Test Results

The points in the scatter plot of Figure 12 correspond to the X, Y difference between the 1st and 2nd insertion for large silicon parts. After the 1st insertion, the top layer was removed straight up and inserted directly back down into the bottom layer. This is referred to as the "straight insertion" condition as opposed to slightly offsetting the parts relative to each other before re-inserting. No vibration assistance was used. The

maximum repeatability error was about 0.25 μm in the Y-axis and was about 1.5 μm in the X-axis. Each data point represents a test with a new set of prepared large parts.

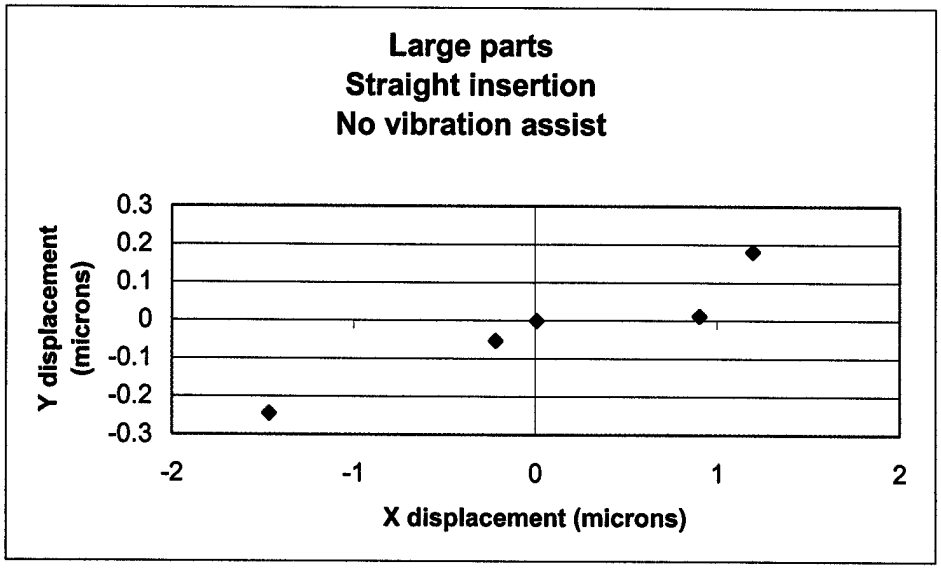


Figure 12. Insertion repeatability: large parts, straight insertion, no vibration assist.

Vibration assist was then added and the following repeatability data shown in Figure 13 was taken. The maximum repeatability error was about 50 nm in the Y-axis and was about 0.3 μm in the X-axis. In this case, the vibration assistance clearly helped in the seating process.

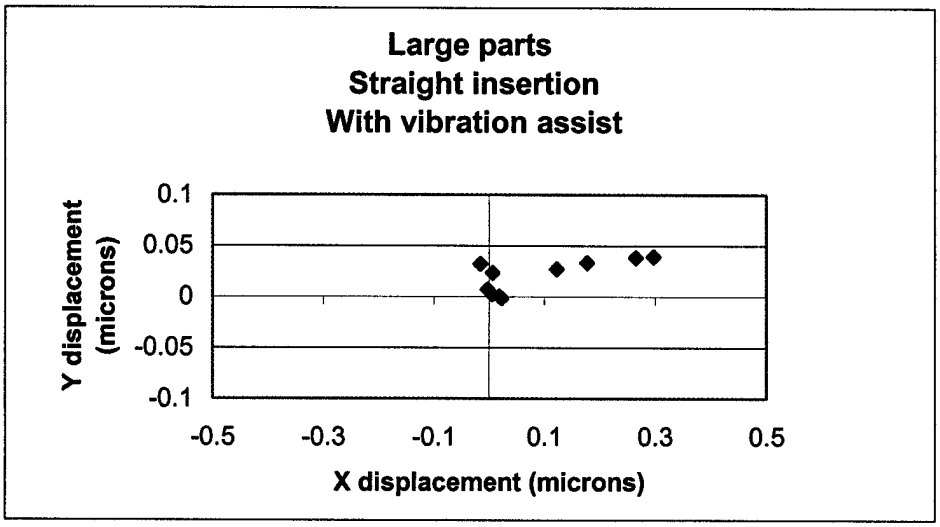


Figure 13. Insertion repeatability: large parts, straight insertion, with vibration assist.

Next, the repeatability test sequence was modified to include offsetting the bottom silicon layer by 10 μm in the X-axis prior to reinserting it into the bottom silicon layer. The offset is used to more accurately emulate initial alignment offsets that will likely occur when pick-and-place robots are used to mate the layers in a manufacturing environment. The maximum repeatability error was about 1.1 μm in the Y-axis and about 11 μm in the X-axis as shown in Figure 14. The relatively large errors in the X-axis may have been due to the fact that only mesa C controls the X-axis position and it is spaced a long distance from mesas A and B and from where the fibers are attached.

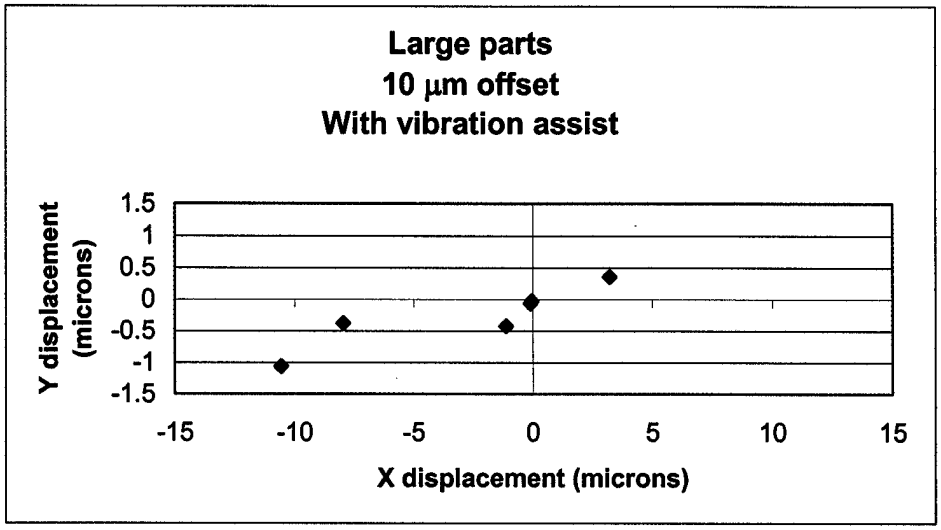


Figure 14. Insertion repeatability: large parts, straight insertion, with vibration assist.

3.3.5 Small Part Kinematic Insertion Test Results

The insertion repeatability of the small parts was measured with vibration assistance. The displacement results with no offset between the first and second insertions as well as the results with a 10 μm offset between the first and second insertions is shown in Figure 15. Most data points were within about 0.1 μm and the maximum repeatability error was about 0.3 μm in the Y-axis. The offset insertion results are much better with the smaller parts than with the larger parts. One possible explanation is that mesa C, which controls the X-axis position, is closer to mesas A and B.

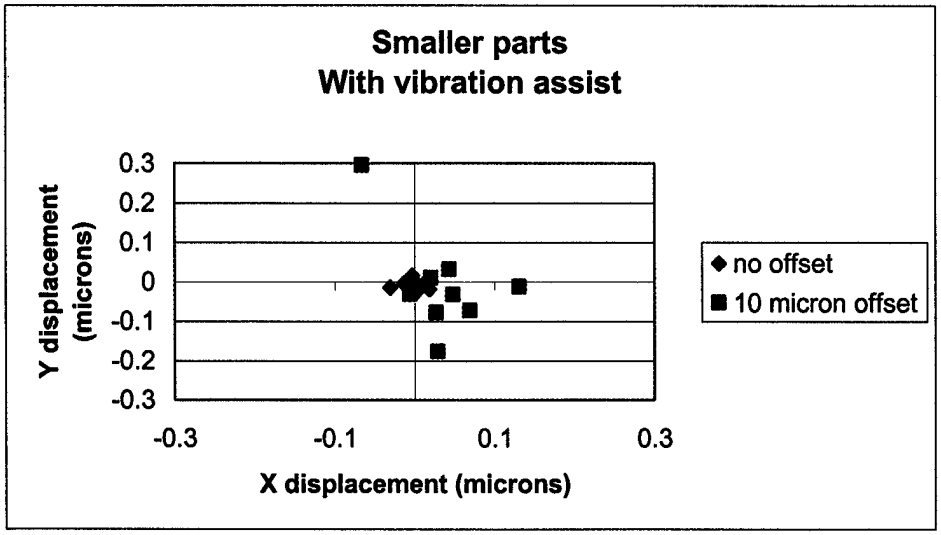


Figure 15. Insertion repeatability: smaller parts with vibration assist.

Further investigation of kinematic seating errors will be required in Phase II. Possible mesa layout improvements could include adding a 4th set of mesas and v-grooves to give better positional control at the expense of further over-constraining the kinematic mount.

The insertion test results reported here were used as an input basis for the optical element location Monte Carlo simulations of the following section.

3.4 Monte Carlo Simulation of Optical Element Location

A Monte Carlo simulation was performed to study the positional error of the laser (or other optical element) induced by kinematic seating errors and manufacturing tolerances of the anisotropically etched mesas and v-grooves. Three sets of parameters were allowed to randomly vary in the simulations. These parameters were:

- The local height, H, at each mesa/v-groove interface (refer to Figure 3)
- Thickness of each silicon layer
- Mask registration errors between the top v-groove features and bottom mesa features on each silicon layer

The local height variations arise from a combination of error sources including kinematic seating error, silicon v-groove and mesa width processing tolerances, small amounts of contamination in the kinematic seats, etc. As shown highly exaggerated in Figure 16, each of the layers will tilt due to local height errors, H, and there will be a linear and angular positional shift of the laser (or other optical element). It was assumed in the simulations that there were 4 layers total and the nominal thickness of each layer was 0.525 mm.

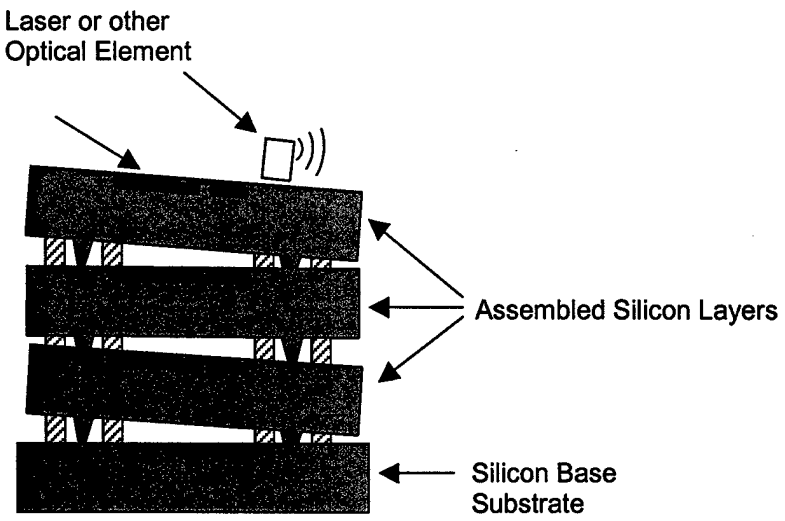


Figure 16. Tilted silicon layers.

3.4.1 Monte Carlo Simulation Tolerance Levels

For each Monte Carlo cycle, each of the parameters listed in section 3.4 were randomly set for each layer using a defined range. The statistical distribution within the range was assumed to be a uniform distribution. The magnitude of the linear offset position of the laser was then calculated for each cycle. A total of ten thousand cycles were performed to constitute a single Monte Carlo trial. The "large part" dimensions for the v-grooves and mesas were used as shown above in Figure 9. Three trials with different tolerance levels were run. The tolerance levels for each trial is listed below in Table 1.

Parameter	Local Direction	Tolerance			Units	Statistical Distribution
		Trial #1	Trial #2	Trial #3		
Local height H	Y	+/- 0.5	+/- 1.0	+/- 2.0	μm	uniform
Mask registration	X	+/- 1.0	+/- 2.0	+/- 3.0	μm	uniform
Mask registration	Z	+/- 1.0	+/- 2.0	+/- 3.0	μm	uniform
Silicon layer thickness	Y	+/- 1.0	+/- 2.0	+/- 5.0	μm	uniform

Table 1. Tolerance levels for Monte Carlo simulations.

3.4.2 Monte Carlo Simulation Results

The calculated X, Y, Z shifts of the laser for trial #1 are shown in Figure 17. Of the cycles in Trial #1, for example, 80% had an X, Y, Z shift magnitudes of less than 1.6 μm. Greater than 99% of the cycles had X, Y, Z shift magnitudes of less than 4.0 μm. Positional errors of this magnitude should be allowable for multimode fiber applications.

For high-performance single mode applications, a final active alignment step will most likely be required.

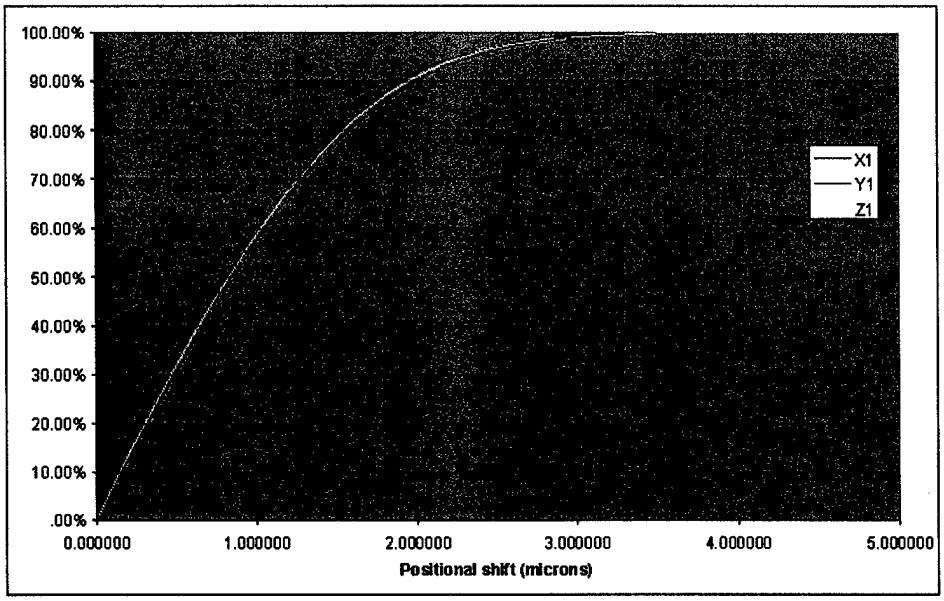


Figure 17. Percentage of Trial #1 cycles with given X, Y, and Z displacements.

The calculated X, Y, Z shifts of the laser for Trial #2 are shown in Figure 18. Of the cycles in Trial #2, 80% had X, Y, Z shift magnitudes of less than 3.2 μm. Greater than 99% of the cycles had laser X, Y, Z shift magnitudes of less than 5.8 μm.

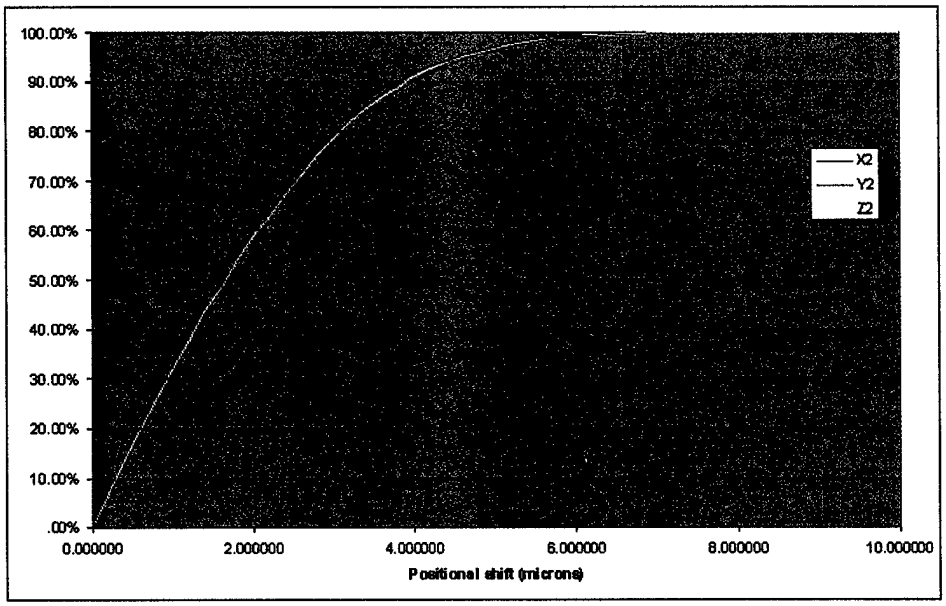


Figure 18. Percentage of Trial #2 cycles with given X, Y, and Z displacements.

The calculated X, Y, Z shifts of the laser for Trial #3 are shown in Figure 19. Of the cycles in Trial #3, 99% had X, Z shift magnitudes of less than about 9.0 μm and the Y positional shifts were worse due to the large silicon layer thickness tolerance in Trial #3. Some form of active alignment may be required with these tolerances even for multimode applications.

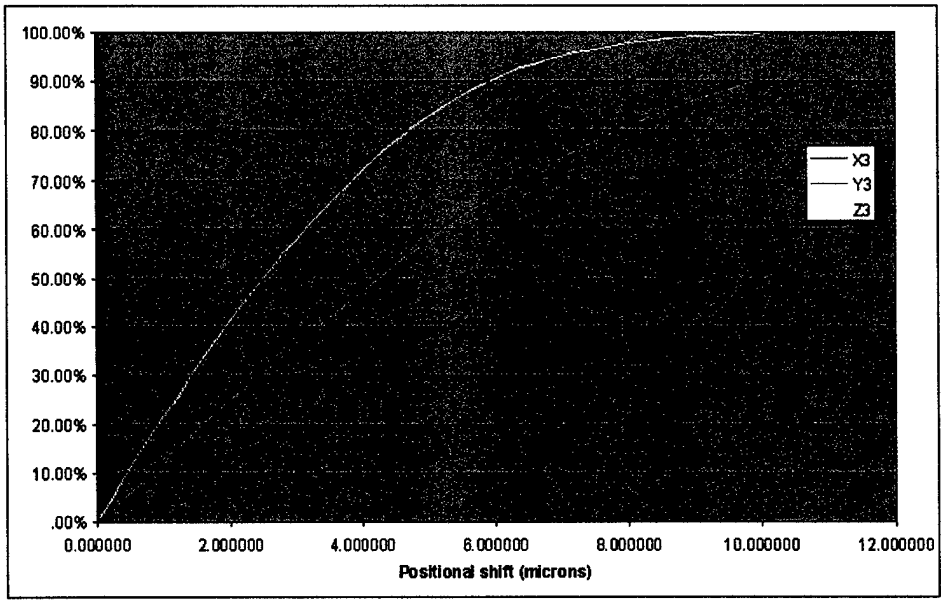


Figure 19. Percentage of Trial #3 cycles with given X, Y, and Z displacements.

4 Thermal Interconnects

Thermally conductive paths must be provided in the layered microstructure shown in Figure 1 in order to remove the heat generated by the high frequency RF and optoelectronic circuitry. A finite element model of the layered microstructure was established to determine the heat removal capacity. The conceptual model used for the finite element thermal model is shown in Figure 20.

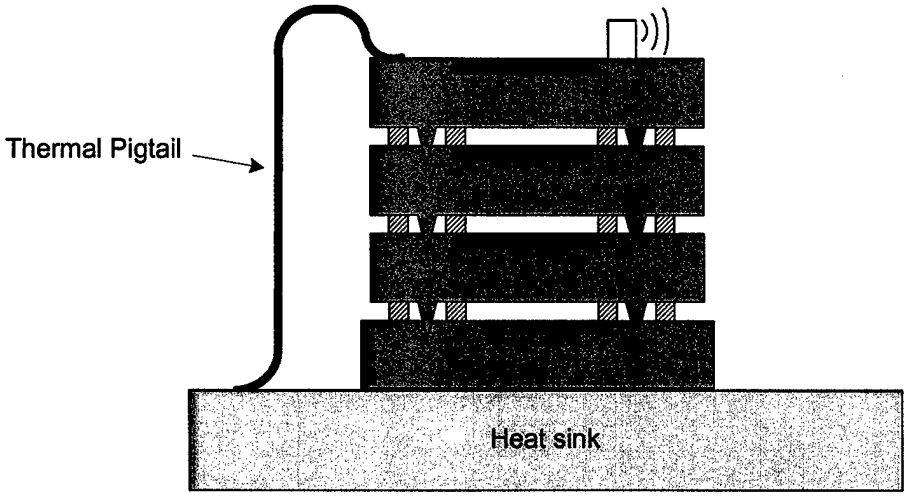


Figure 20. Conceptual model for finite element thermal interconnect analysis.

4.1 Finite Element Thermal Simulations

Dr. James Starr, from Altec Solutions, performed the finite element thermal simulations with input and guidance from Avanti Optics. Some of the assumptions were:

- Silicon die size = 3.0 X 3.0 X 0.425 mm
- Die spacing = 61 μm
- No heat transfer by conduction or radiation
- Heat flux is applied to a 1.0 X 1.0 mm area on the die
- The bottom surface of the heat sink is held at 0° C

The mesas and v-grooves, that form the kinematic mounts between the layers, were laid out in a triangular fashion as shown in Figure 21. Figure 22 shows the meshing generated by the finite element program, COSMOS, and Figure 23 is a close-up view of the meshing showing a silicon mesa seated into a v-groove.

Figure 21. Kinematic mount layout for thermal interconnect analysis.

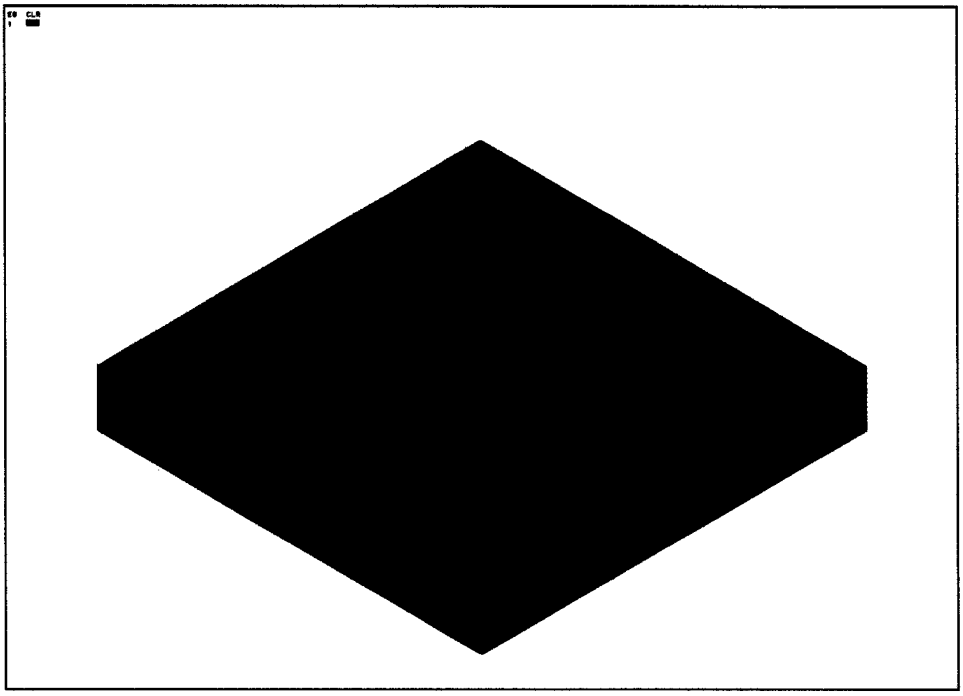


Figure 22. Finite element mesh.

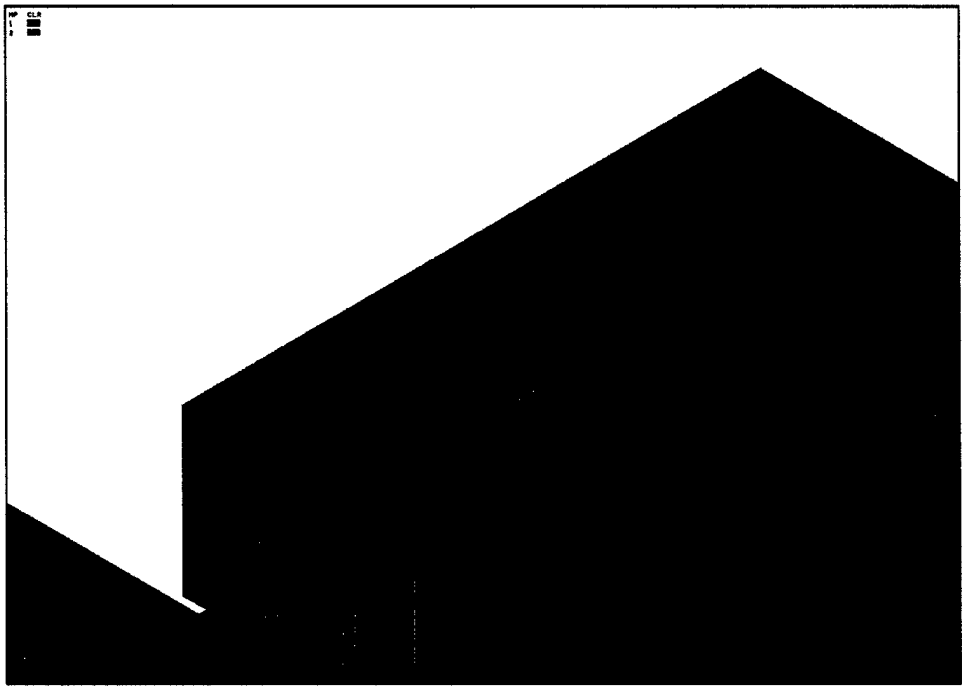


Figure 23. Close-up view of finite element meshing showing mesa seated into a v-groove.

4.2 Finite Element Simulation Results

The following variables were studied to see the affects on heat removal capacity:

- Finite contact resistance between the silicon mesas and v-grooves
- Solder interconnects
- Thermal pigtail
- Heat sink material

4.2.1 Effect of Mesa and V-groove Thermal Contact Resistance

The simulations started by assuming there was perfect thermal contact between the silicon mesas and v-grooves. Also, the heat sink was assumed to be silicon. Figure 24 shows the results obtained by the finite element program when 100 mW was applied to each of the 4 layers (total power = 400 mW). A maximum temperature rise of 13.3 °C was predicted. By exploiting symmetry to reduce computation time, only half of the structure needs to be analyzed. A cross sectional view from Figure 24 through the v-grooves and mesas is shown below in Figure 25.

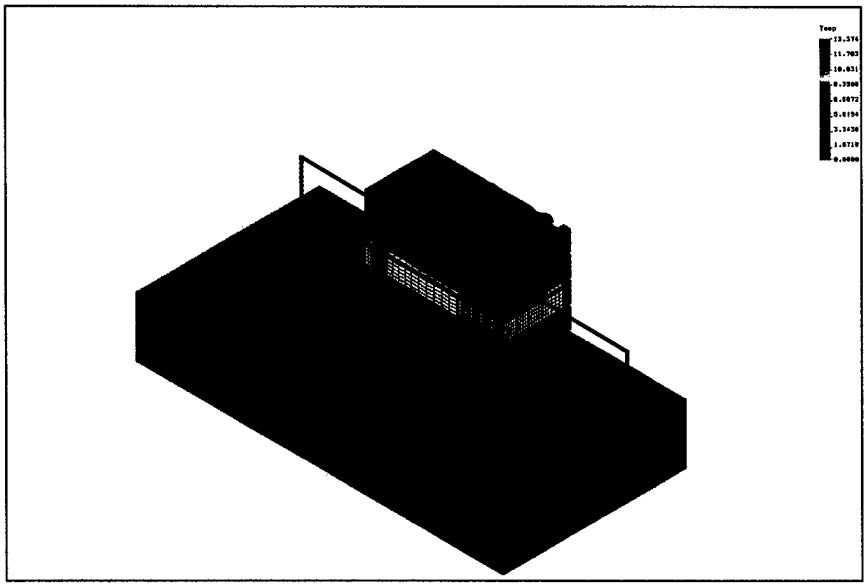


Figure 24. Results for perfect thermal contact between mesas and v-grooves.

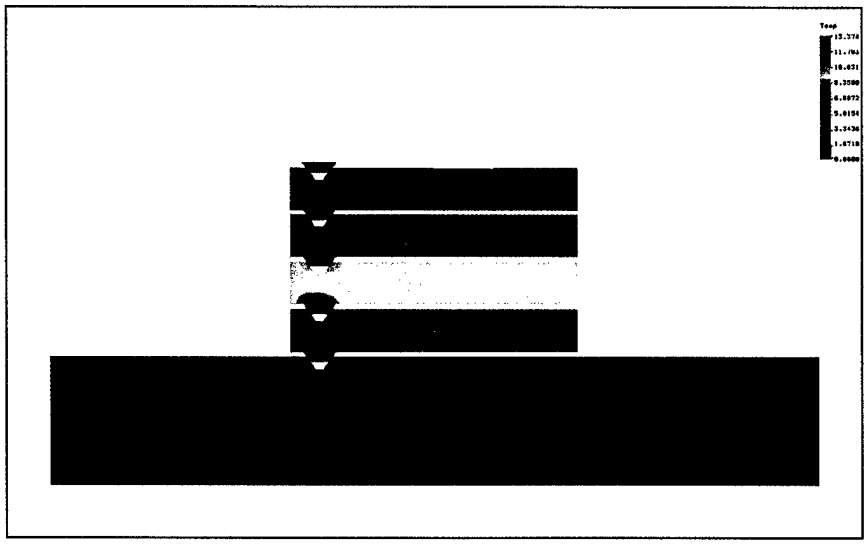


Figure 25. Cross-sectional view showing mesa and v-grooves.

To model contact resistance effects between the silicon mesas and v-grooves, a one-micron layer was inserted between them. By assigning a thermal conductivity of silicon to this one-micron layer, a zero contact resistance is simulated. By assigning a thermal conductivity equal to that of air, an extremely high contact resistance may be simulated by the air gap.

Figure 26 shows the results obtained with a one-micron air gap is inserted between the silicon mesas and v-grooves and 100 mW is applied to each of the 4 layers. A maximum temperature rise of 801 °C is predicted. Clearly, the heat removal capacity of this structure without solder interconnects or a thermal pigtail is strongly influenced by the thermal contact resistance between the mesas and v-grooves.

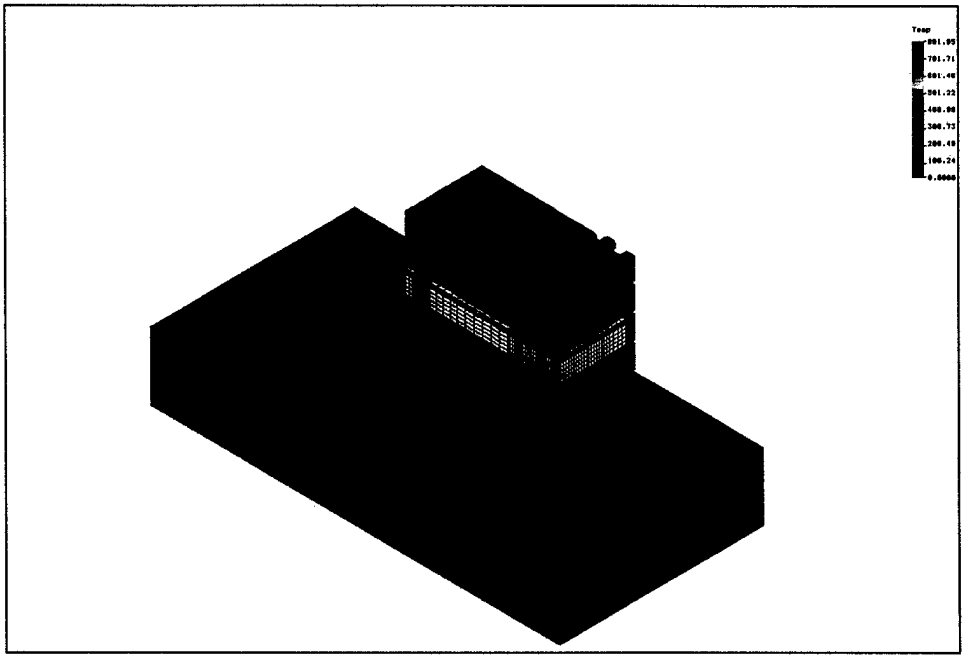


Figure 26. Results for 1.0μm air gap between mesas and v-grooves.

4.2.2 Effect of Solder Interconnects

The effects of the solder interconnects were modeled by assuming there were pads of eutectic SnPb solder between each die. For modeling simplicity, only 3 large pads of dimensions 600 μm X 600 μm X 61 μm were used to simulate multiple, smaller solder pads. This is shown in Figure 27. A maximum temperature rise of 5.2 °C was predicted when 100 mW was applied to each of the 4 layers, a one-micron gap between the mesas and v-grooves was assumed, and there were solder pads between each layer. Recall that without the solder and with a one-micron air gap between the mesas and v-grooves, the maximum predicted temperature rise was 801 °C.

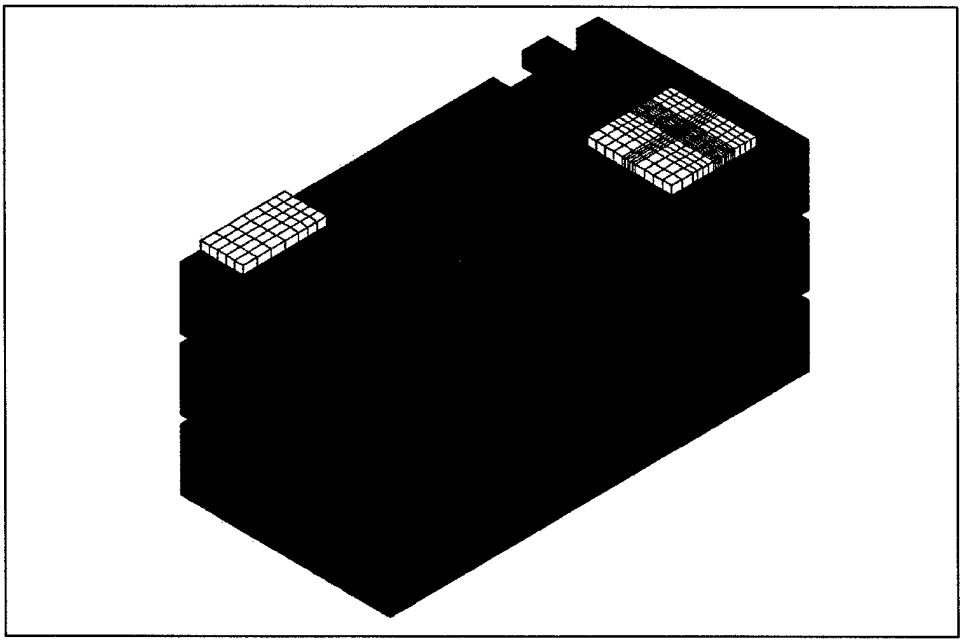


Figure 27. Solder pad layout for thermal simulations.

4.2.3 Effect of Thermal Pigtail and Kovar Heat Sink

The finite element model was finally extended to include a thermal pigtail, which consisted of a copper strap, and a Kovar heat sink instead of silicon. This is shown in Figure 28. The yellow layer on the bottom is Kovar, the pink layer between the Kovar and the silicon substrate is a 50-micron layer of epoxy. The copper strap (thermal pigtail) is shown in red. A 150-micron thick eutectic AuSn solder (turquoise) is modeled to attach the copper strap to the silicon. The bottom layer of the Kovar heat sink is held at 0 °C. By setting the thermal conductivities to that of air, the various features and layers could selectively turned off. The properties of the various layers are summarized in Table 2.

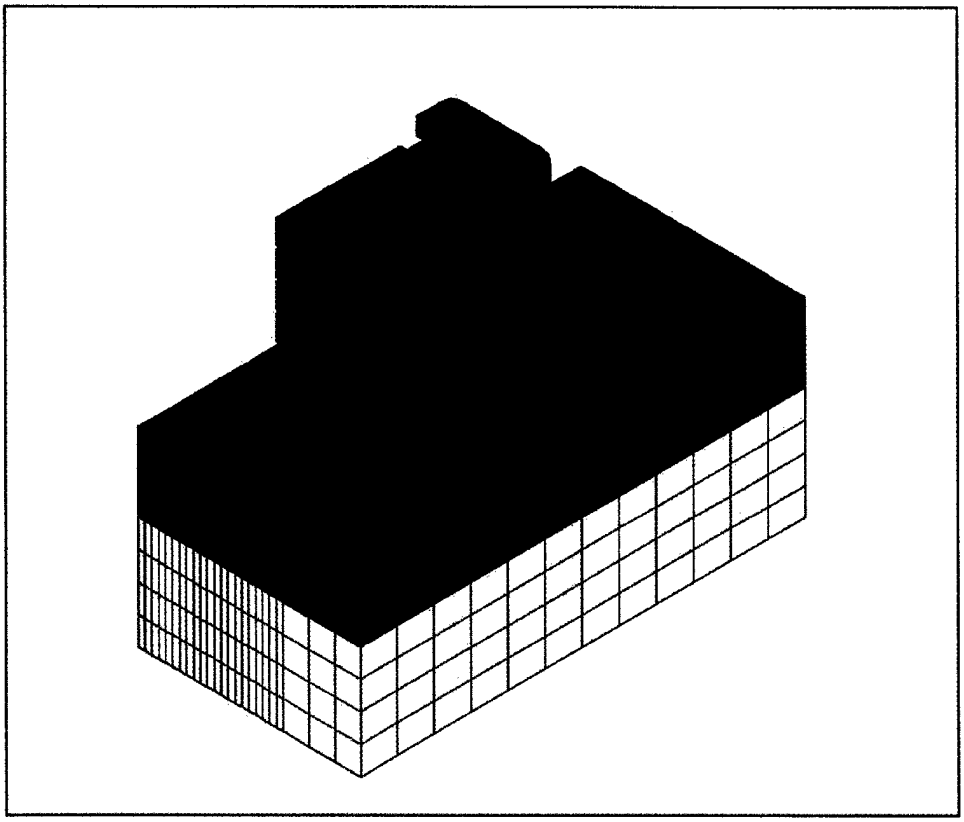


Figure 28. Finite element model with thermal pigtail and Kovar heat sink.

Material	Color	Thermal Conductivity (W/m°K)
Silicon	Blue	157
Air	Green	0.0242
AuSn solder	Turquoise	58
Copper	Red	710
Epoxy	Pink	4
Kovar	Yellow	17.3
PbSn solder	White	55

Table 2. Figure 28 material properties.

A matrix with the three variables: kinematic seating contact resistance between mesas and v-grooves, solder bumps between silicon layers, and thermal pigtail, was established. The thermal conductivity of the mesa and v-groove interface was either set to air (1.0 μm gap) or silicon (perfect thermal contact). Setting their respective thermal conductivities to that of air could also effectively turn off the solder and thermal pigtail features. The maximum predicted temperature rise predicted by the various combinations is summarized in Table 3 for a heat flux load of 100 mW on each layer.

Mesa gap	Solder bumps	Thermal pigtail	Max temp rise (°C)
Silicon	No	No	14.0
Air (1.0 μm)	No	No	802
Silicon	Yes	No	4.29
Air (1.0 μm)	Yes	No	5.22
Silicon	No	Yes	5.85
Air (1.0 μm)	No	Yes	165
Silicon	Yes	Yes	3.17
Air (1.0 μm)	Yes	Yes	3.55

Table 3. Simulation results for a thermal load of 100 mW applied to each layer.

Figure 29 is a graph summarizing the maximum temperature rise with perfect thermal contact between the mesas and v-grooves. Figure 30 summarizes the maximum temperature rise with a 1.0 μm air gap between the mesas and v-grooves. The temperatures are plotted on a logarithmic scale.

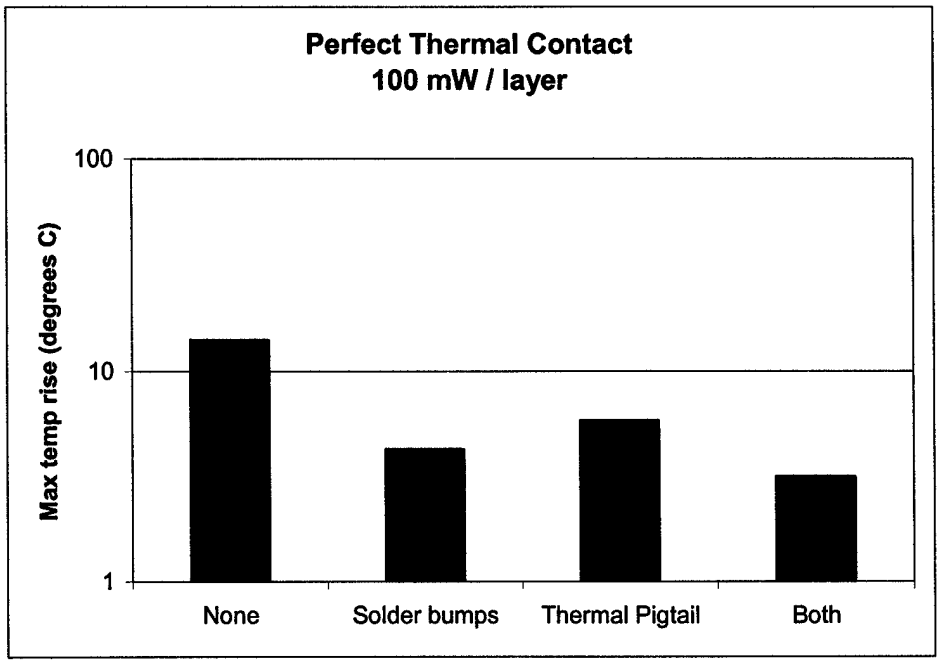


Figure 29. Maximum temperature rise for perfect thermal contact between mesas and v-grooves.

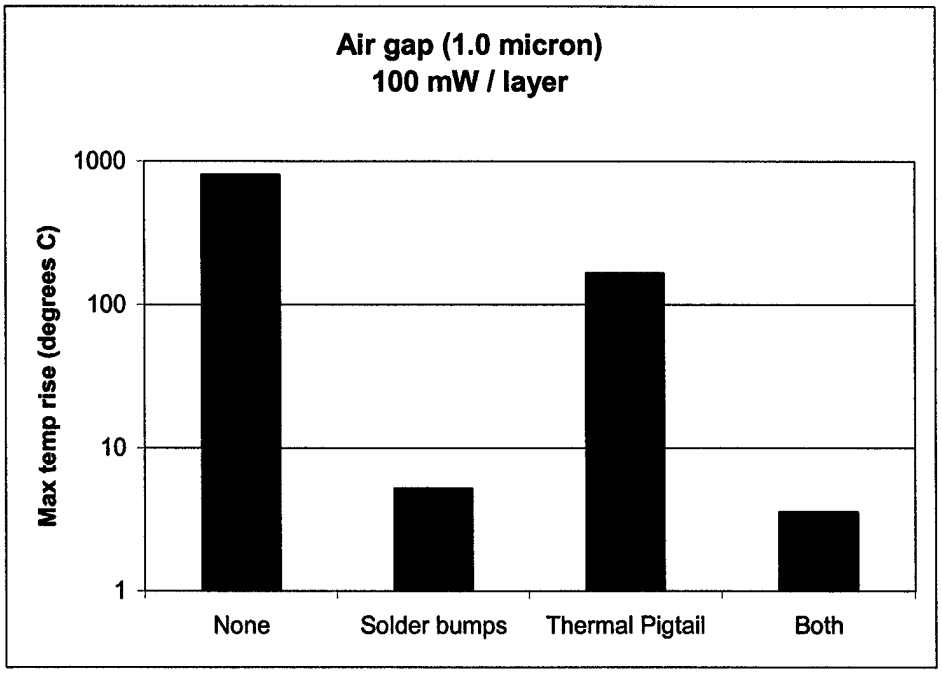


Figure 30. Maximum temperature rise with air gap between mesas and v-grooves.

Both the solder bumps and the thermal pigtail significantly reduce the maximum temperature in the system. In general, the solder bumps are much more effective than the thermal pigtail in reducing the maximum temperature. By looking at cross sectional data, the maximum temperature usually occurs on the top surface of the top silicon layer. However, the thermal pigtail can result in the peak temperature occurring in the second silicon layer from the top. Also, by comparison with the previous model having silicon as the heat sink layer, the addition of the Kovar and epoxy layers, in general, resulted in an increase in maximum temperature of only 0.2 °C per 100mW of total heat input into any of the layers.

4.2.4 Effect of Large Thermal Load on Top Layer

We were also curious to find out what would happen if the heat flux load of one of the layers was raised considerably higher than the other layers. Table 4 summarizes the effect of increasing the heat flux load on the top layer to 1000mW while keeping the load on the other three layers at 100mW.

Mesa gap	Solder bumps	Thermal pigtail	Max temp rise (°C)
Silicon	No	No	65.3
Air (1.0 μm)	No	No	3689
Silicon	Yes	No	20.6
Air (1.0 μm)	Yes	No	25.2
Silicon	No	Yes	22.1
Air (1.0 μm)	No	Yes	175
Silicon	Yes	Yes	15.6
Air (1.0 μm)	Yes	Yes	17.5

Table 4. Thermal load of 1000mW on top layer, 100 mW on three lower layers.

Figure 31 is a plot of the maximum temperature rise with 1000 mW applied to the top layer, 100 mW applied to the lower three layers, and an air gap of 1.0 μm between the mesas and v-grooves. Again, the solder bumps do an excellent job of reducing the maximum temperature.

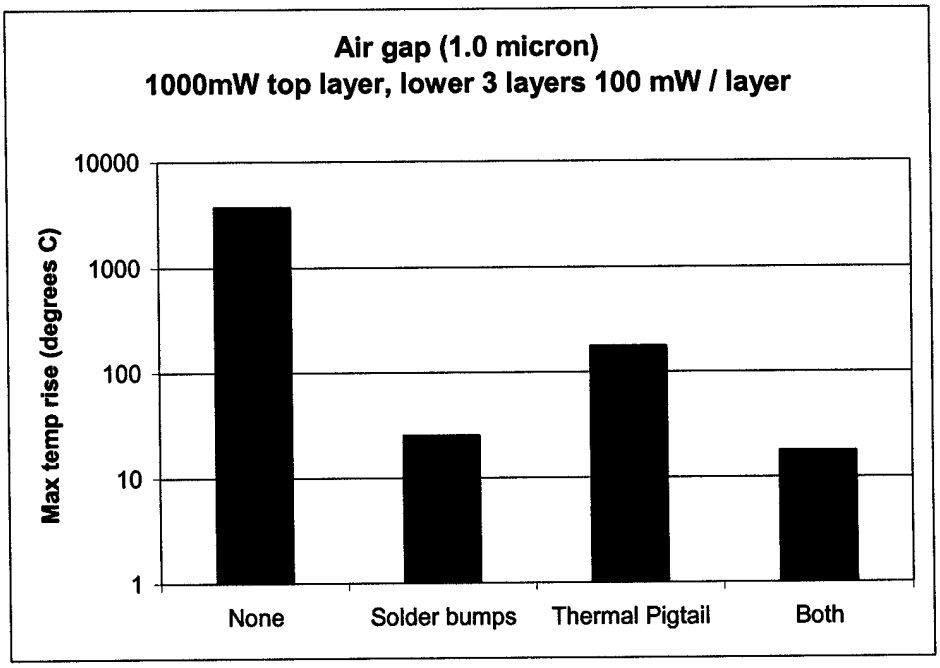


Figure 31. Maximum temperature rise with 1000 mW applied to top layer.

5 Electrical Interconnects

There were three main tasks in exploring the electrical feasibility of 3D micro-scale interconnects. The first was to identify appropriate electromagnetic simulation methods. Several simulation packages were considered. Ansoft's High Frequency Structure Simulator (HFSS) was chosen, as it is readily available and was thought to be the most accurate package evaluated.

Once a suitable software package was selected, the electrical performance of arbitrary 3D passive structures could be simulated. High-speed digital and microwave applications require controlled impedance circuits, thus an electrical waveguide was designed. Common transmission line structures were considered before a Finite-Ground Coplanar Waveguide (FG-CPW) was designed. Upon selection of the transmission line structure, a number of different physical interconnect structures were simulated to determine their performance in routing high-speed signals. From our simulations, lumped parameter models were extracted that can be cascaded to model the behavior of multiple levels in a stacked structure.

Finally, electromagnetic field simulations of 3D structures are presented that successfully compared to HFSS simulations. Due to the brief phase 1 schedule and limited funds, existing structures and test fixtures were used to establish this correlation. Specifically, surface mount 0402 thin-film resistors on alumina were chosen for experimental verification because they are similar to Avanti's thin-film resistive heaters. The 0402 thin-film resistors were mounted on microstrip printed circuit board test fixtures and measurements were compared to simulations. This provided a useful data point in validating the ability to simulate three-dimensional electrical structures. The measurements and simulations agree very well to 15 GHz.

This report covers only the important conclusions drawn from the electrical study. Additional experiments and the development of the knowledge gleaned is contained in more detail in the monthly reports.

5.1 Select Electromagnetic Simulation Software

5.1.1 Available Simulation Packages

5.1.1.1 ADS Empirical Models

Agilent's Advanced Design System (ADS) provides linear RF and SPICE transient simulation capabilities. Common distributed circuit effects are characterized with empirical models. The accuracy of the empirical modeling is

limited in frequency and geometry. For example, the models of microstrip transmission line discontinuities are valid for certain ratios of line width to substrate height. At extreme aspect ratios, the empirical equations begin to lose accuracy. When situations arise where more precision is desired, or structures outside the ranges of the empirical models need to be simulated, electromagnetic solvers can be used. The ADS environment is extremely user friendly however and can be used as a platform to compare simulation results from other software packages as well as measured data.

5.1.1.2 MOMENTUM Planar EM Solver

Agilent's MOMENTUM is a full wave 2D electromagnetic solver based on a method of moments engine. MOMENTUM is integrated into the ADS environment and is fairly simple to use. Simulations are limited to planar metallization however. Thus, planar transmission line effects can be studied very accurately but true 3D structures such as vias and solder bridges cannot. In addition, MOMENTUM makes the assumption that the circuit substrate is infinite in extent. While this is generally of little consequence for transmission line simulations, it is very limiting in our multi-planar substrate stack up.

5.1.1.3 Ansoft's High Frequency Structure Simulator

Ansoft's High Frequency Structure Simulator (HFSS) is a full-wave 3D finite element method electromagnetic solver. The software package begins with a 3D CAD module for creating physical models. A materials manager allows material properties, such as dielectric constant, conductivity and magnetic permeability, to be assigned to objects defined in the physical model. An extensive materials library is included as well as the ability to create linear and non-linear user-defined materials. A boundary manager allows boundary conditions to be assigned at the edges of the physical model and on any 2D surface inside it. A metal trace can thus be specified as a 3D box with material properties, or a 2D rectangle with a boundary condition. Specifying the object as in the later case typically reduces the aspect ratio of the model as well as the number of cells that are created during the numerical solution process. There is a definite tradeoff in that all physical structures are 3D in nature, but the speed gained in the simulation process and the ability to successively iterate and develop a physical model far out weigh the loss in accuracy from these types of simplifications.

5.1.2 Justification for Choosing HFSS

5.1.2.1 Accuracy

Based on the overview of the simulators evaluated, the decision was made to use HFSS. Ansoft provides other 3D electromagnetic simulation packages, such as Maxwell 3D, that implement a variety of approximations to Maxwell's equations to gain simulation speed. The sizes of the structures being simulated in our

application however are not insignificant. Cascading multiple waveguiding structures together gives physical dimensions on the order of 1cm.

In addition, high-speed digital signals contain significant spectral content at the 3rd and 5th harmonics of the clock frequency. For a 10Gbps, 0101 data pattern, significant energy can be expected at 5GHz, 15GHz and 25GHz. In free space, a 25GHz sine wave has a wavelength of 1.2cm. Thus we are clearly approaching significant electrical length and the full-wave analysis of HFSS is justified.

5.1.2.2 Availability

HFSS was also readily available at the start of this subcontract. Copies were available in several labs at the University of Minnesota, as well as at Wavecrest Corporation.

5.1.2.3 Experience

Past experience was also considered and proved to be a motivating factor in selecting HFSS. Developing a user-level proficiency with an electromagnetic solver typically requires months of exposure. Since HFSS is generally considered to be the industry standard for simulating 3D high-speed structures, significant documentation in the form of articles, training materials, and example projects, is readily available.

5.1.2.4 Lumped Utility

HFSS is our choice for field simulations of the different physical structures investigated. Cascading multiple copies of the same structure, as in a multi-level 3-D circuit, is impractical in HFSS, and unnecessary. For cascaded simulations, we extracted lumped parameter models and plugged them into ADS.

5.1.3 Simulation Correlation Study

A brief study was performed to verify the simulation packages. A microstrip step discontinuity on a material similar to FR4 (Nelco 4000-13) was modeled in ADS, MOMENTUM and HFSS. The three models appear below along with the s-parameter results. From the plots, excellent agreement between the modeling techniques was determined to 20GHz. This simple exercise provided an important confidence builder in the ability to construct and simulate the MOMENTUM and HFSS electromagnetic models.

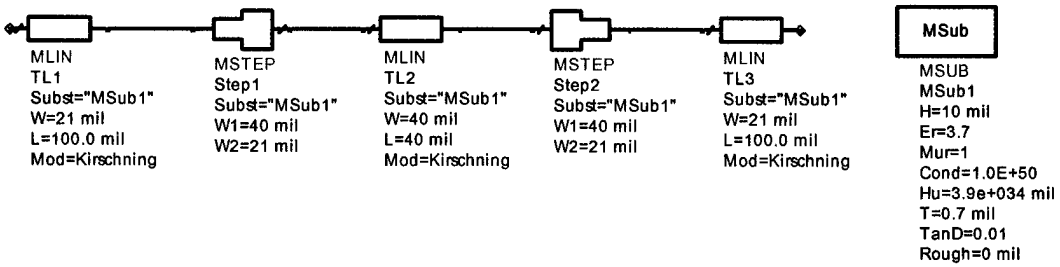


Fig 32. ADS Circuit Simulator Microstrip Step Discontinuity Model

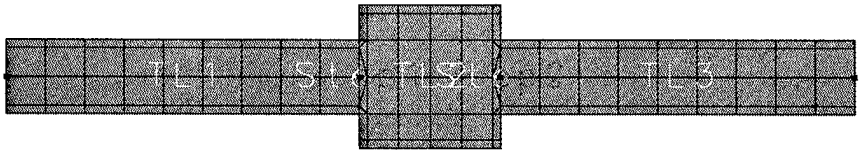


Fig 33. MOMENTUM Microstrip Step Discontinuity Model

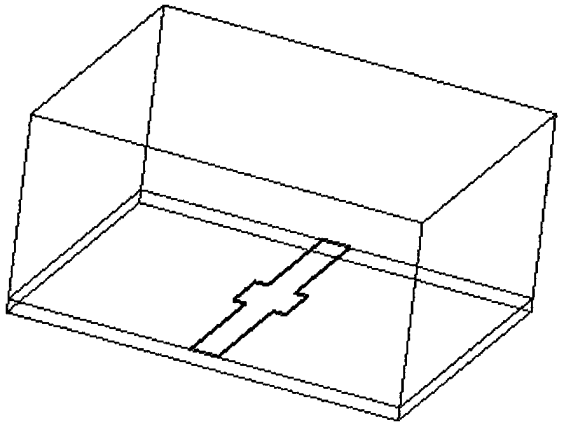


Fig 34. HFSS Microstrip Step Discontinuity Model

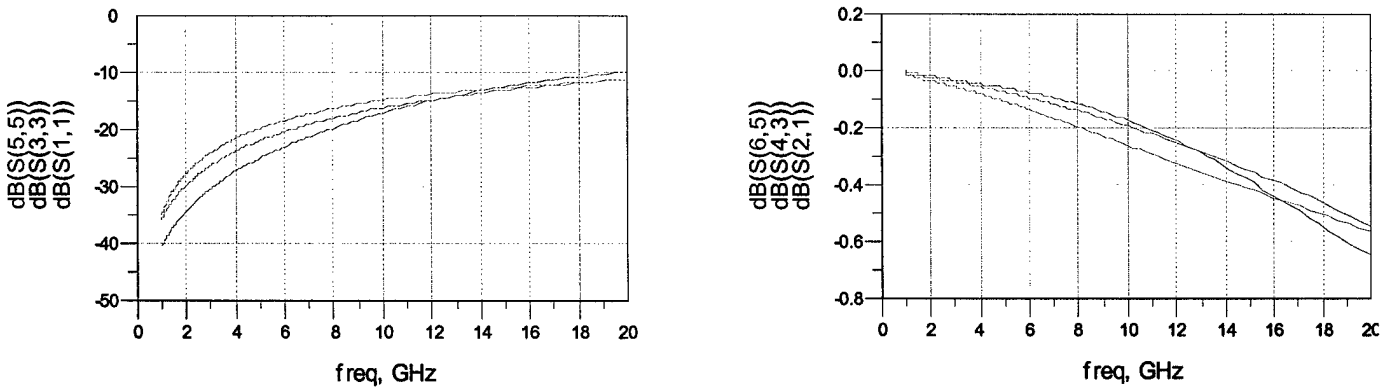


Fig 35. ADS (red), MOMENTUM (blue) and HFSS (pink) Simulation Correlation

5.2 Design Waveguide Structure

5.2.1 Select Type of Waveguiding Structure

Due to the broadband spectral content of high-speed digital applications, the interconnects were designed to maintain controlled 50 ohm impedance. The structures need to be DC coupled multi-conductor waveguides, or transmission lines. Microstrip, stripline, and coplanar strip waveguides were considered. A coplanar waveguide (CPW) was selected as the best candidate because right angle interconnects can be made in any orientation with electrical contact being made at one surface only. Joining two stripline structures for example would require making electrical contact in three planes; top ground, middle signal, and bottom ground.

5.2.2 Design Waveguide Dimensions

Avanti's prototype component mounts are 5mm X 3mm silicon rectangles with a standard wafer thickness of 525um. The design process was to enter the die thickness and electrical parameters for silicon into Linecalc, an empirical transmission line calculator available in ADS. A reasonable signal center conductor width of 200um (~8mils) was set. Linecalc then solved for the gap spacing (115um) between the center conductor and ground traces required for 50 ohm impedance. A picture of this waveguide appears below in fig 36. The light blue rectangle is the silicon die and the red rectangles are the metal traces.

A finite ground coplanar waveguide (FG-CPW) was also designed. In this structure, the ground strips do not extend to the edge of the silicon surface as in CPW. Since no empirical models currently exist for FG-CPW in ADS, the dimensions had to be designed and verified with HFSS. A picture of the FG-CPW appears below in fig 38.

5.2.3 Simulate Isolated Waveguides

5.2.3.1 HFSS Results

The physical model of the CPW on silicon was simulated in HFSS. The silicon substrate was defined in the material manager as having a dielectric constant of 11.9. The metal traces were constructed with two-dimensional rectangles and given perfect electrically conducting boundaries. This approximation does not give up much accuracy as the likely thin film deposition process will have a thickness of 1um or less, which is clearly orders of magnitude less than the trace width of 200um.

The model was simulated from 2GHz-20GHz and s-parameters were provided from the field quantities. A plot of the return loss appears below in fig 37.

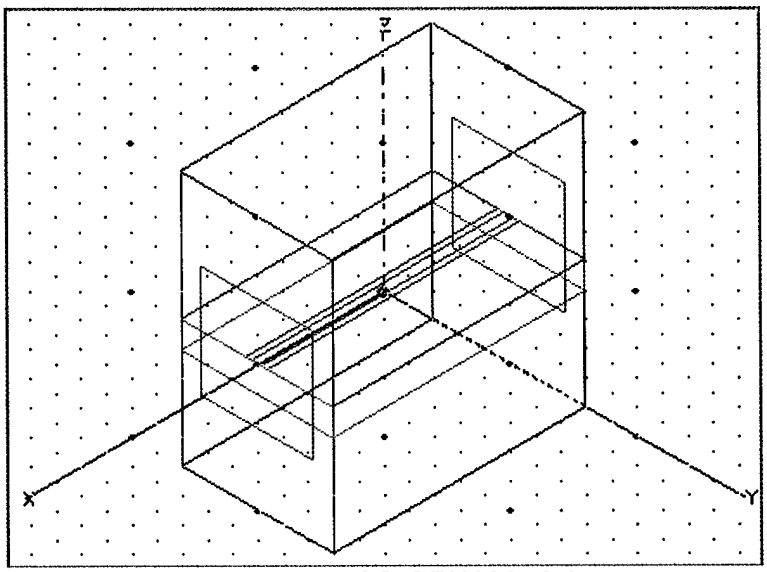


Fig 36. HFSS CPW Model

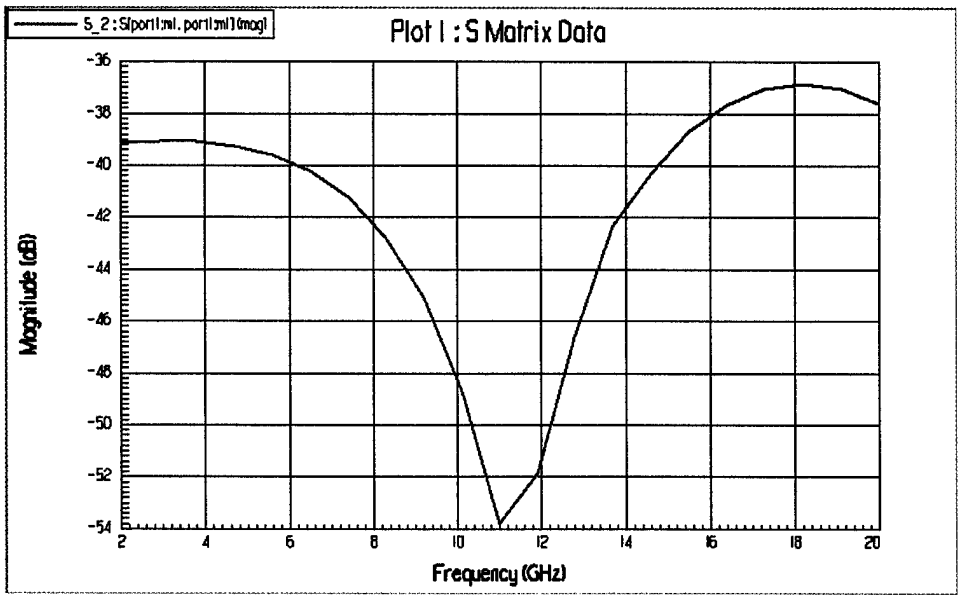


Fig 37. HFSS CPW Return Loss

In an identical manner, a FG-CPW model was created in HFSS. The widths of the ground strips were reduced to 400um. This had the effect of decreasing the amount of capacitance to ground for a given length of the waveguide. To compensate for the effect and re-tune the waveguide to a 50 ohm impedance, the ground strips were moved closer to the signal conductor. A gap spacing of 100um (115um in CPW) produced a structure with good return loss. The HFSS model of this structure, along with the simulated return loss, appears below in figs 38 and 39.

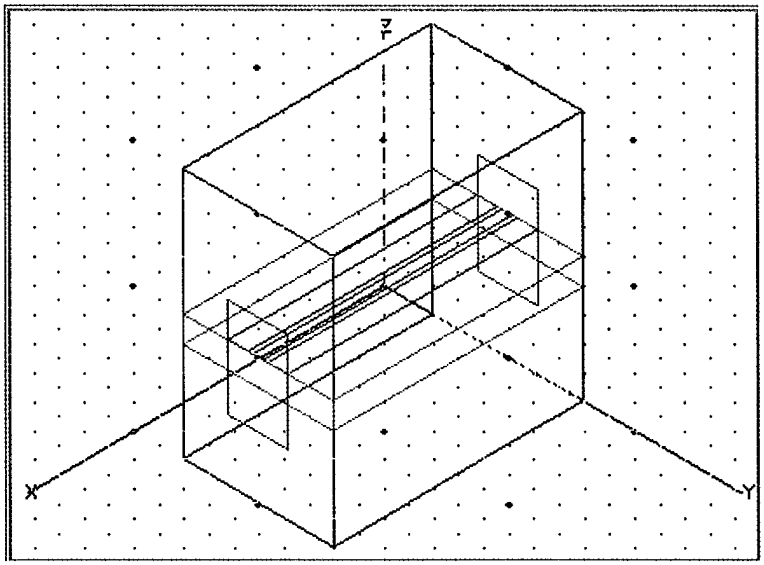


Fig 38. HFSS FG-CPW Model

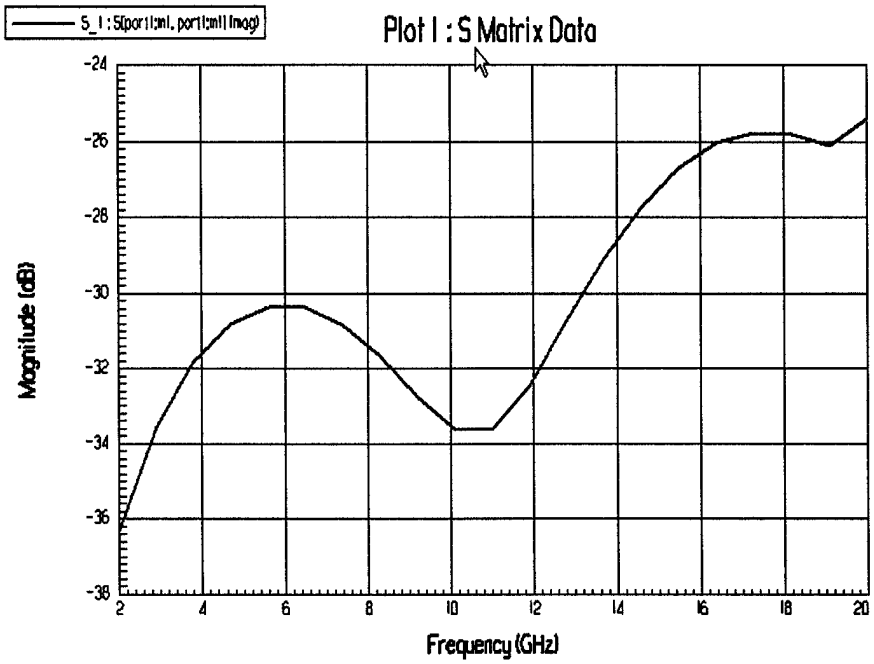


Fig 39. HFSS FG-CPW Return Loss

5.2.3.2 S-parameters, Return Loss, and Step Response

HFSS numerically solves for the electric and magnetic field quantities throughout the physical model. Field quantities however provide little meaning to circuit designers. Thus, the software package computes and plots s-parameters. S-parameters are linear network parameters and are algebraically related Y or Z parameters and ABCD matrices. S-parameters are convenient quantities for analysis because they can be easily measured and verified with a network analyzer. S-parameters are frequency domain quantities however, and do not necessarily provide the most useful information for high-speed digital applications.

An important feature in a high-speed digital system is the step response. A step response is analogous to a 0 to 1 transition in a digital waveform and provides important quantities such as rise time and settle time. Structures that have good return loss (S11), above and below their –3dB bandwidth, typically have linear phase delay, lower group delay, and a better step response. For this reason, optimizing and verifying return loss is of great importance.

5.3 Investigate Waveguide Transitions

5.3.1 Solder Bridges

Solder bridges were modeled with HFSS to simulate the transition from one waveguide structure to another. The solder profile and dimension as well as the air spacing between the waveguides were varied. It was found that for small air gaps (~100um) the solder profile was less critical. An example of solder transition appears below in fig 40.

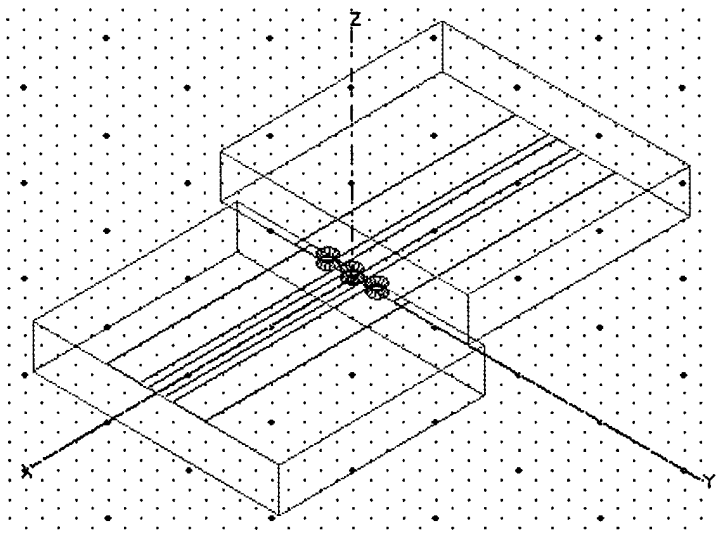


Fig 40. 100um Solder Air Gap on FG-CPW

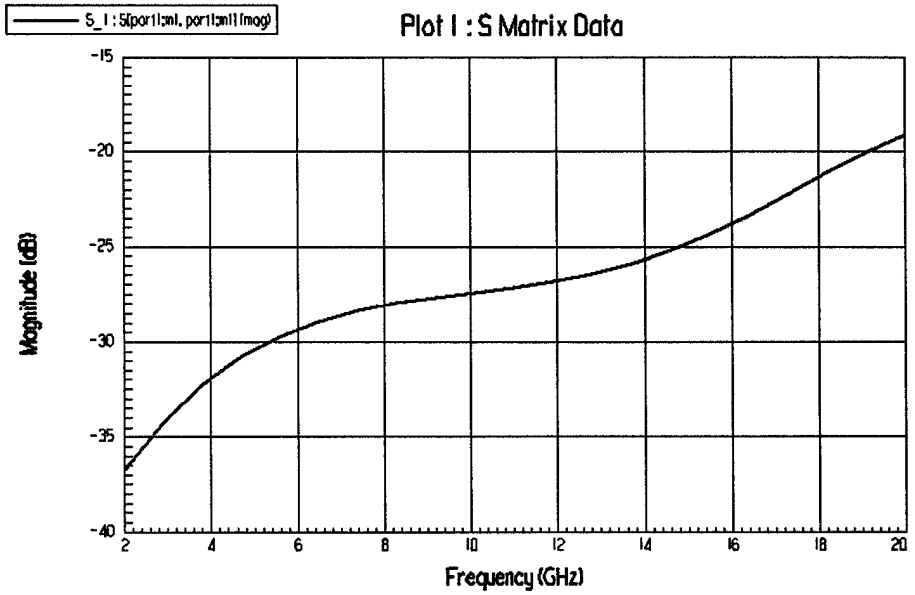


Fig 41. 100um Solder Air Gap Return Loss

From the plot above, it can be seen that this transition exhibits a high degree of impedance control to 20GHz.

At 400um air gaps, the profile of the solder was found to be more critical. Cylindrical, pumpkin and hourglass shapes were simulated. The results below show the best performance is achieved with an hourglass shape. Thinning the solder in the middle realizes a series inductance that tunes the capacitive discontinuities at the right angle transitions.

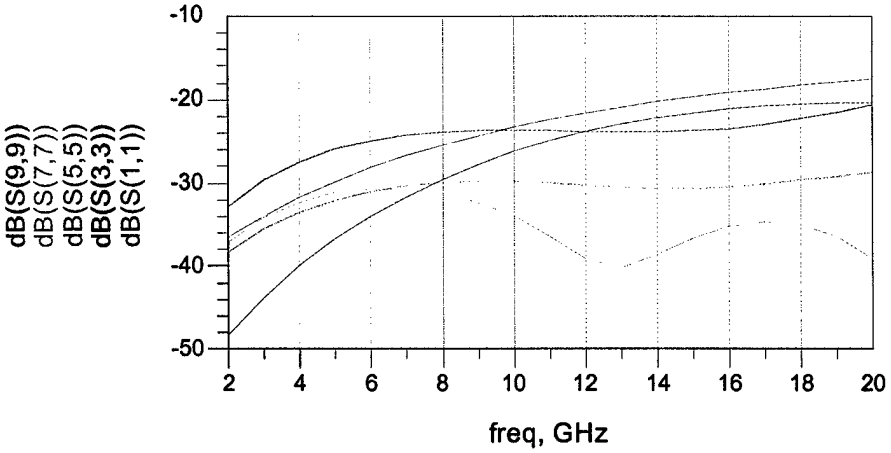


Fig 42. Various Solder Profiles for 400um Gap Spacing
Cylinder, Pumpkin, >Pumpkin, Hourglass, >Hourglass

Given lumped parameter models, we used ADS to simulate cascades of up to five interconnect structures with acceptable results. As the number of layers and other potential impedance discontinuities is application specific, we will not present the details here. Some examples are available in the monthly reports.

We used *Surface Evolver*, a freeware software product that simulates the behavior of surfaces under the influence of surface tension, gravity, and other energies, to develop a realistic shape of likely solder columns with these geometries.

Our electrical simulations showed a low sensitivity of the electrical performance to the central diameter of the hourglass solder column. Using Surface Evolver and the properties of tin-lead solder, we learned that the central diameter of the solder columns of interest are rather robust to changes in solder volume that may result during manufacture. For solder columns 100 um in height sitting on 200 um pads with a central width of about 120 um, a ten percent change in solder volume results in only a 7 percent change in central width. The following images illustrate a 33% difference in volume between the first and second images (second is about 120 um at center) and a 10% difference in volume between the second and third.

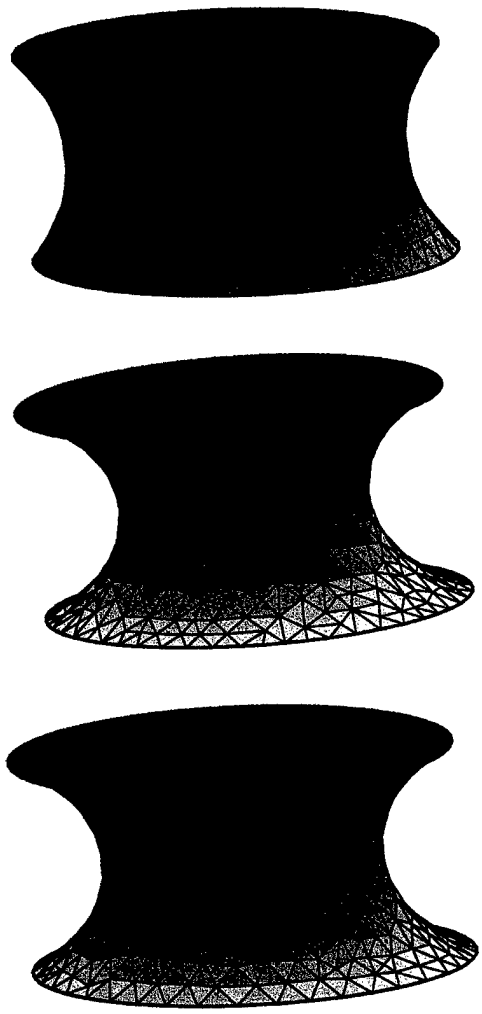


Fig 43. Detailed shape of various volumes of solder between 200 um pads with 100 um air gap.

We approximated the shape of these evolved surfaces in HFSS with a smooth curve. The electrical performance of the resulting smooth solid was compared to that resulting from the two truncated cones modeled in Figure 40. Electrical performance was virtually indistinguishable between the two shapes when the diameters at the ends and middle were matched. Therefore, we conclude that the easier to simulate cone structures are sufficient for study.

5.3.2 Thru Vias

Thru vias were modeled in the silicon waveguides. Initially, circular, plated drills were simulated. A picture of 100um diameter drills through the silicon die appears below in fig 44 along with the HFSS simulation of the return loss in fig 45. The metal plated vias transition the FG-CPW from one surface of the silicon structure to the other.

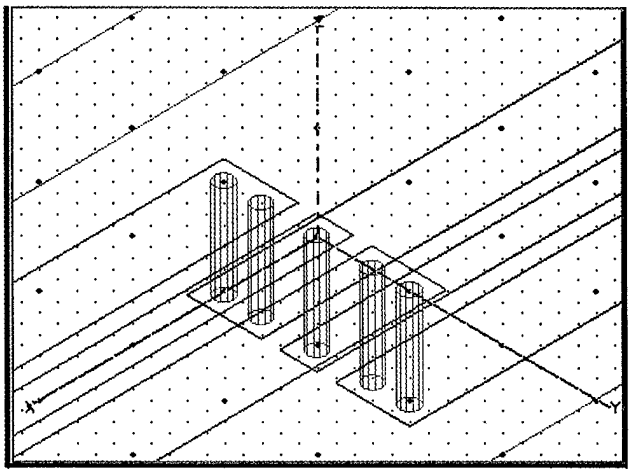


Fig 44. 100um diameter thru vias

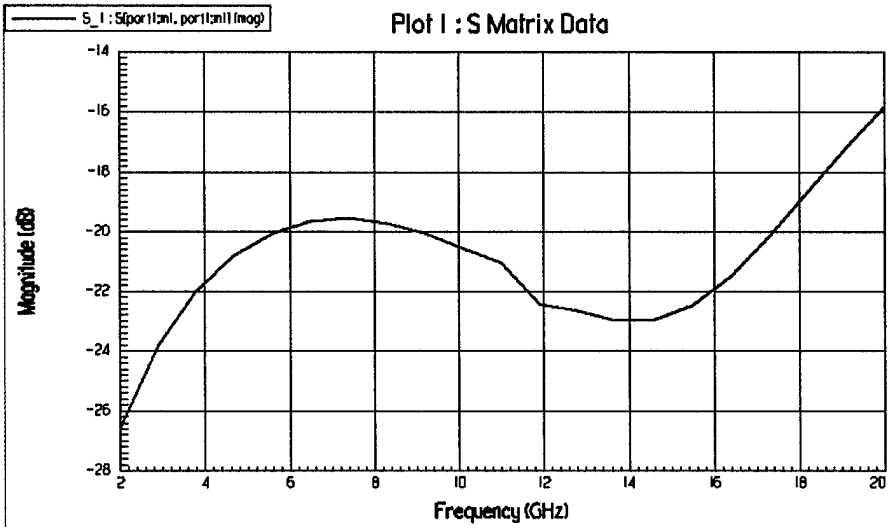


Fig 45. Cylindrical Thru Via Return Loss

Anisotropically etched v-grooves via structure were simulated as well. The v-grooves penetrate the die completely and plating on the walls of the grooves connects metal on both surfaces. The ground vias are etched from the opposite surface as the signal center conductor for density. A picture of the v-groove via structure and return loss plot appear below in figs 46 and 47. The return loss of this structure is extremely poor.

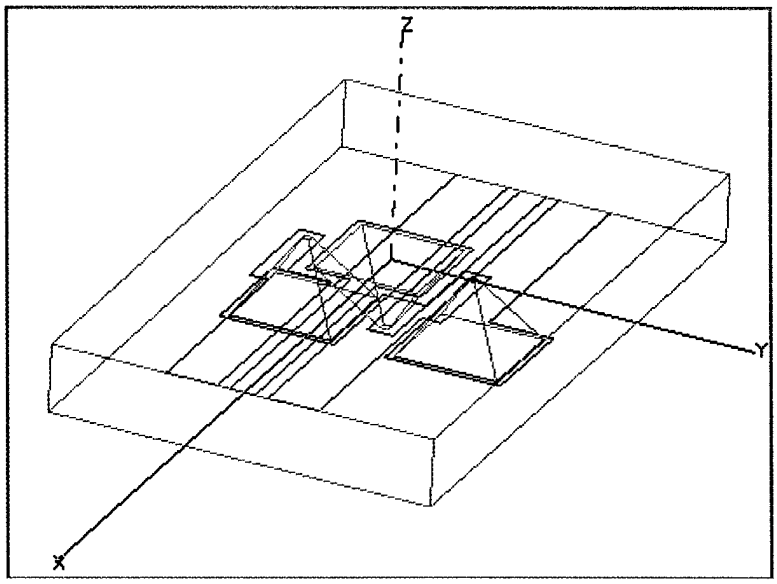


Fig 46. Anisotropically Etched V-groove via transition.

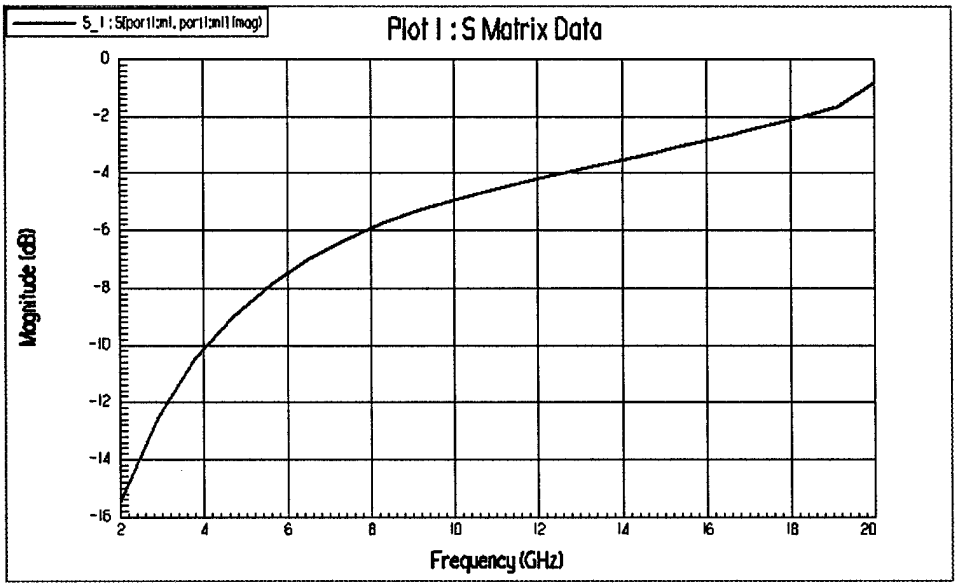


Fig 47. V-groove Via Return Loss

5.4 Verify Simulator with Measurements

5.4.1 Structures Available for Measurement

Due the brevity of the phase 1 schedule and the limited funds available, it was not possible to fabricate either of the above CPW or FG-CPW waveguides for verification of the simulations. Instead, we used existing devices and test fixtures as verification of our simulations. Several types of resistors, thin film on alumina and thick film on alumina,

were available in multiple values and packages. Thin film resistors are similar to the thin film heaters Avanti has used to melt solder between the stacked layers. The majority of the data was collected with thick film resists mounted on 0402 packages. A microstrip test fixture designed for previous experiments was used with slight modifications.

5.4.2 Justification and Validity of Structures

The film resistors provided readily available devices of considerable value. The dimensions of the resistors (1.6mm x 0.8mm X 0.25mm) were similar to the dimensions of the silicon waveguides. In addition, the high dielectric constant of alumina (9.6) provided electromagnetic properties comparable to silicon.

5.4.3 Measurements and Results

5.4.3.1 Test Fixture Description

A test fixture with improved coaxial-to-microstrip launch was designed to de-embed the resistor model. A signal launch was obtained by cutting away board material on the test fixture and exposing the first signal ground layer. Semi-rigid coax was then soldered directly to the ground plane. The center conductor of the coaxial cable was soldered directly to the microstrip line as well. This launch scheme obtained significantly improved bandwidth and impedance continuity over standard SMA connections (edge launch and flange mount) because the ground reference of the microstrip and coaxial cable had direct electrical contact. A diagram of the coaxial-to-microstrip launch appears below.

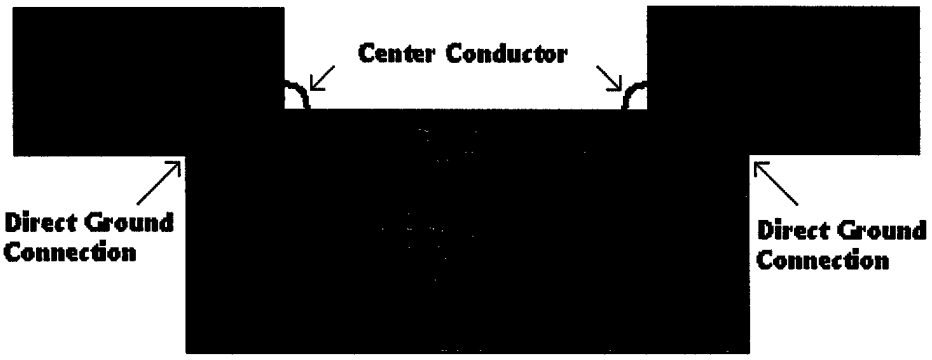


Fig 48. Coaxial-to-microstrip Test Fixture Launch

The performance of the test fixture launch was compared to a standard edge-launch SMA connector. The test fixture consisted of two connectors or coaxial launches to a 1.7-inch microstrip thru line. The test fixture coaxial launch has bandwidth of about 20 GHz and maintains 15dB of return loss to 15GHz.

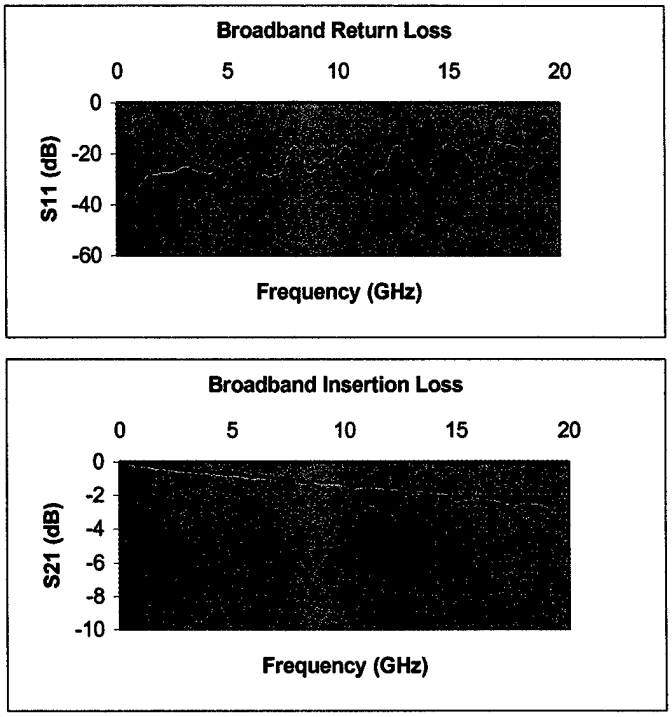


Fig 49. Comparison of Coaxial Launch and SMA Launch on Test Fixture. Coaxial Launch – Red : SMA Edge Launch Connector – Blue

In addition to providing an improved signal transition to the test fixture, the coaxial-to-microstrip launch lends itself to modeling. The coaxial cables were measured accurately with calipers, as was the microstrip line length. The part of the coaxial center conductor that extends into free space was modeled as a lumped inductor. A circuit model of the test fixture was created in ADS.

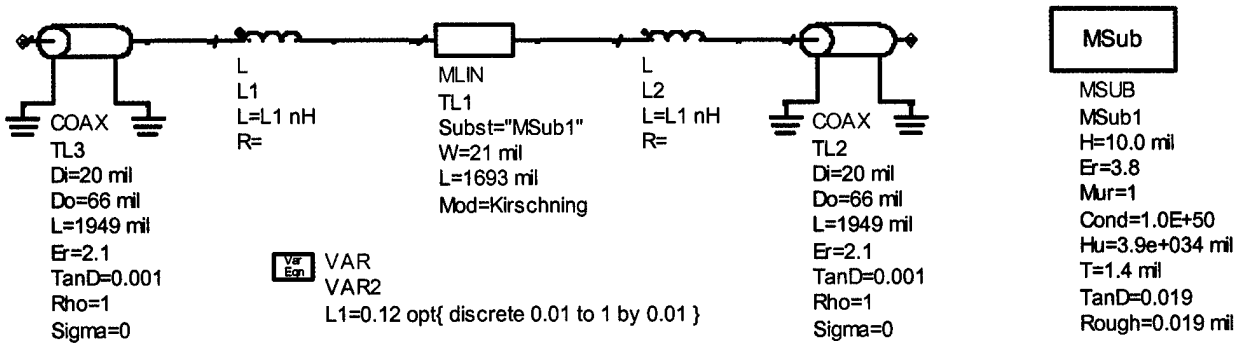


Fig 50. ADS Circuit Model of Test Fixture

The unknown center-conductor inductance was set as a variable (L1) and the ADS optimizer was set to match the test fixture model simulation to the measured s-parameter data. The s-parameter plots below show good agreement between the model and the measured test fixture data.

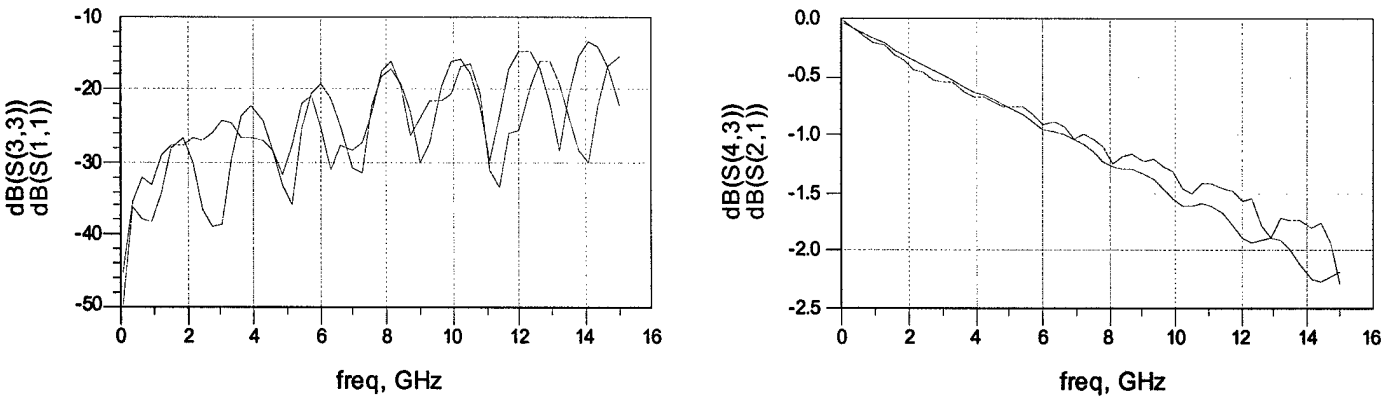


Fig 51. Measured and Simulated Test Fixture Frequency Response
Measured Data– Red: ADS Circuit Model- Blue

5.4.3.2 Resistor Measurements and Modeling

The test fixture characterization and modeling allowed component evaluation. The general procedure used was to mount a component to the test fixture and measure the s-parameters. The measured data was then imported into ADS. The model of the test fixture with device was then intuitively and iteratively developed such that at each iteration, a proposed model was simulated with various lumped inductances and capacitances optimized to match the data. The model that produced the best correlation between data was assumed to be the approximate, first order equivalent circuit.

The first component studied was an 0402 resistor mounted in series with the microstrip lines of the test fixture. As outlined above, the measured data was imported into ADS and compared to the circuit model being developed. For this particular component, shunt capacitances through the substrate and across the resistor were proposed along with series lead inductance as in initial guess. After several iterations, the capacitances were removed and the resulting resistor package model was a series inductance corresponding to the end cap metallization of the resistor. The ADS circuit model of the test fixture, resistor and dominant package parasitics, appears below along with a comparison of the measured data and model simulation.

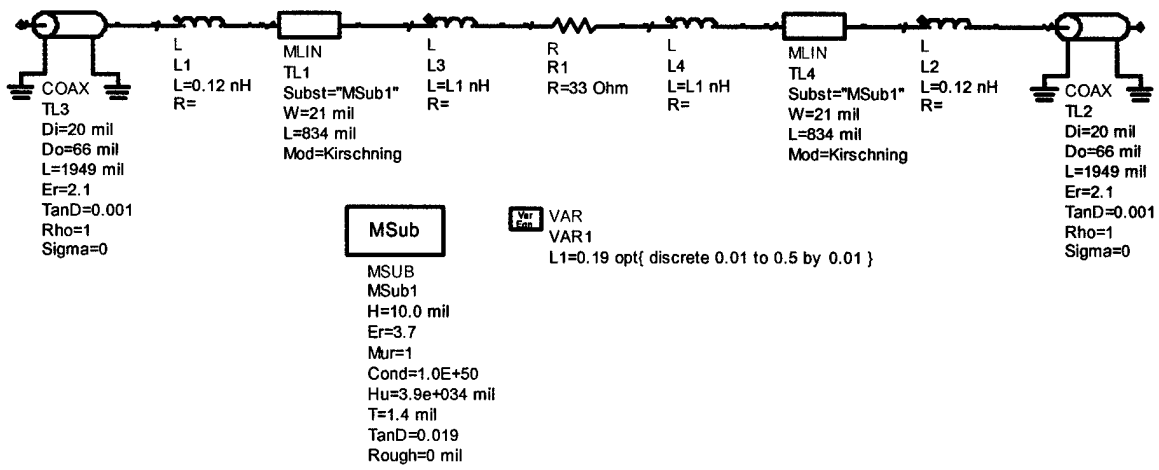


Fig 52. Series Resistor Test Fixture Model

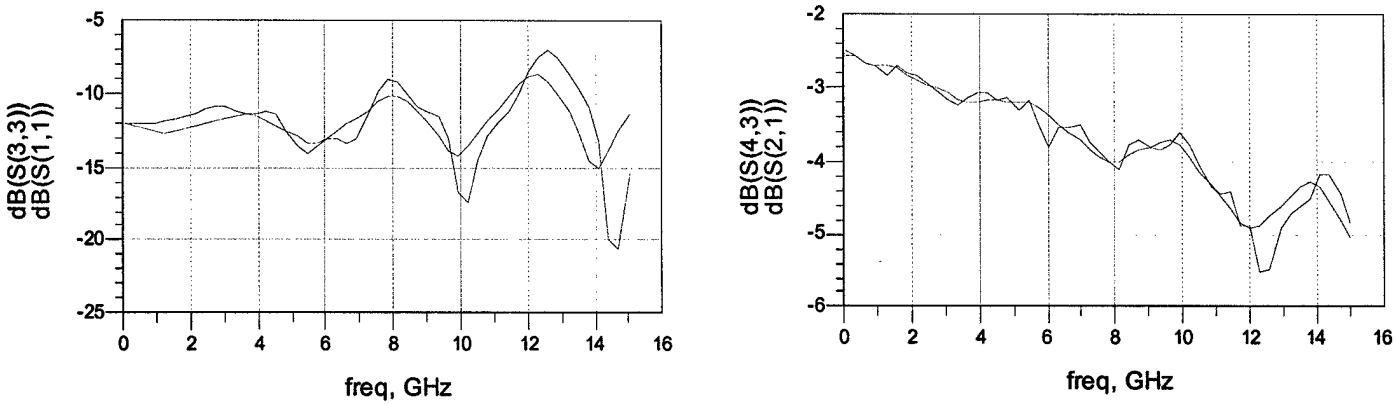


Fig 53. Measured and Simulated Series Resistor and Test Fixture Frequency Response
Measured Data – Blue: Simulated Data – Red

This experiment was repeated for several different resistors ranging in value from 15Ω to 400Ω. The ADS circuit simulator repeatedly optimized the lumped inductor package model to be between 0.18nH and 0.21nH per end cap.

The 0402 resistor was also de-embedded in a shunt fashion. The shunt component test fixture was characterized as above and the de-embedding procedure repeated. The shunt resistor model includes microstrip gap coupling across the resistor as well as the effect of a via to the internal ground plane. The shunt resistor, package parasitics and test fixture model along with the simulated and measured data, appears below.

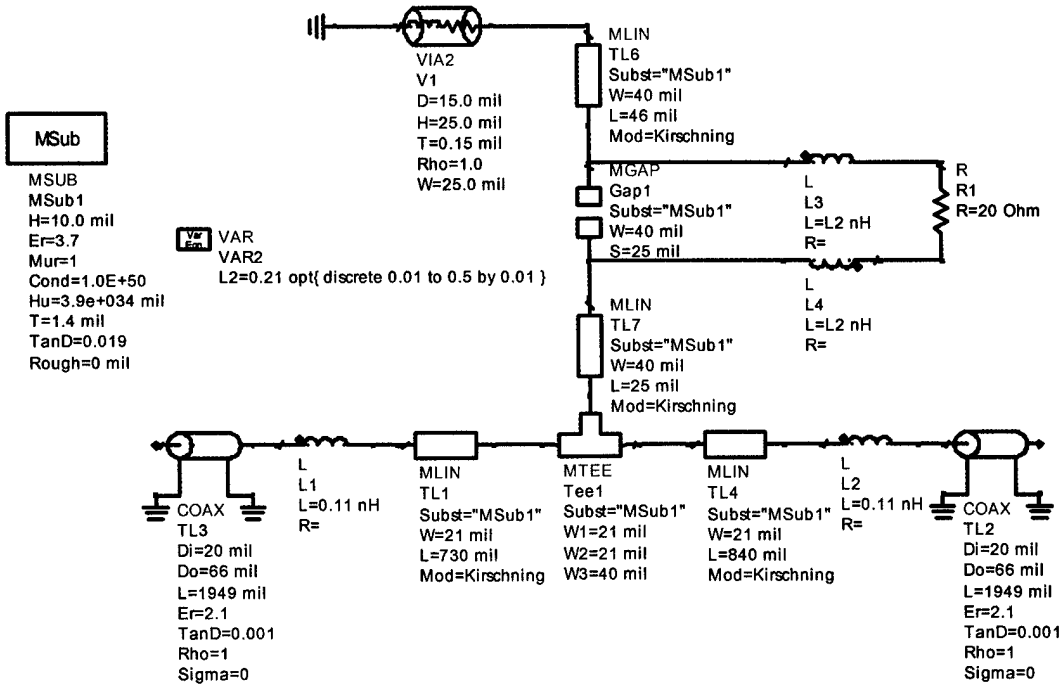


Fig 54. Shunt Resistor Test Fixture Model

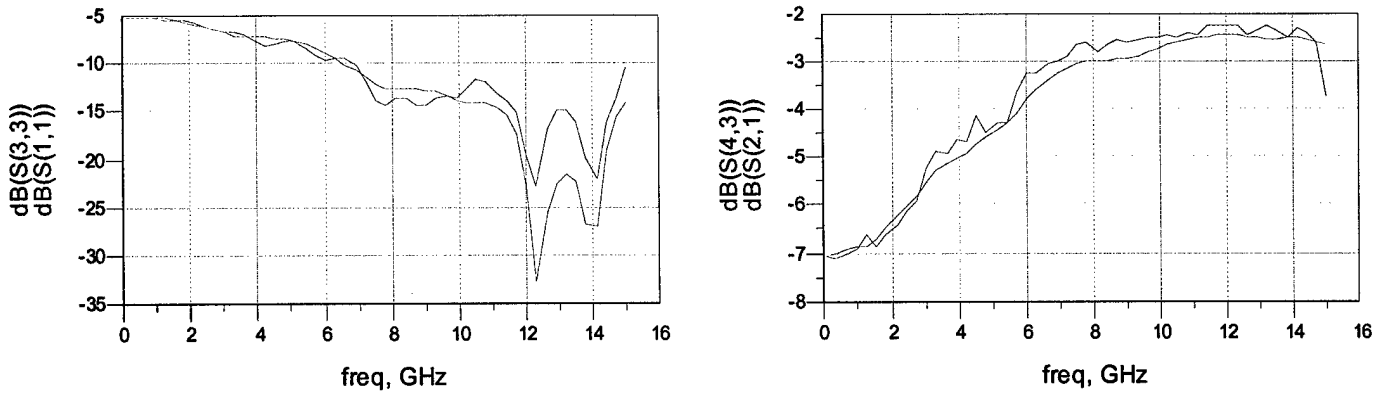


Fig 55. Measured and Simulated Shunt Resistor and Test Fixture Frequency Response
Measured Data – Blue: Simulated Data – Red

This experiment was repeated as above for the same resistance values as in the series case. In all cases, the ADS optimizer tuned the lumped package inductance to be between 0.18nH and 0.21nH.

5.4.3.3 0402 HFSS Model

The 0402 resistor mounted in a series configuration on a microstrip line was modeled in HFSS. The model used a 96% alumina substrate for the resistor and a surface impedance boundary for the thin film. It included finite end cap terminations of 2mil thickness and non-infinite conductivity. The microstrip lines were also modeled with a finite height of 1mil. The circuit board substrate was 10mil thick Nelco 4000-13. The physical model of the resistor and microstrip line appears below.

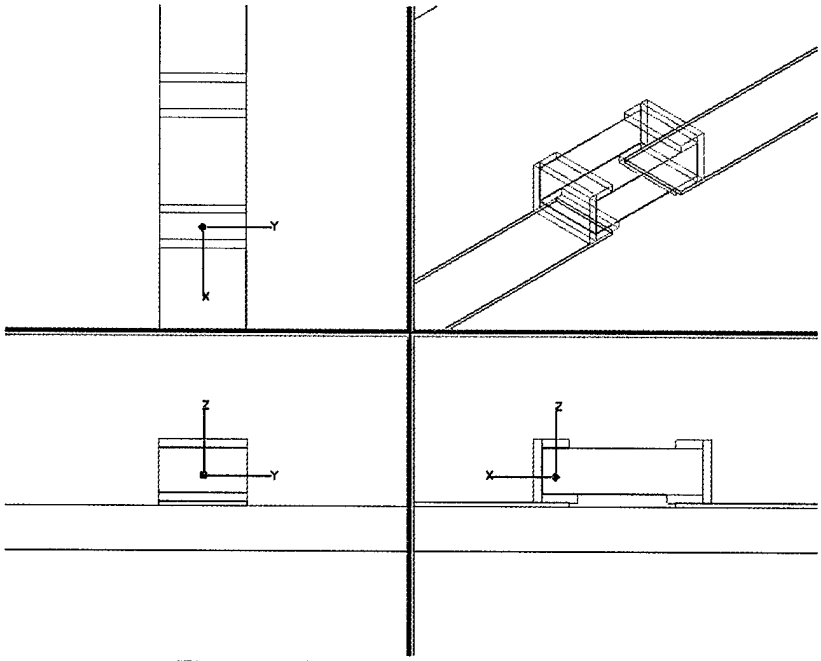


Fig 56. HFSS Resistor Geometric Model

A corresponding ADS model was constructed. It consisted of microstrip feedlines to the resistor and open-end effect microstrip stubs to model the copper underneath the resistor. The model consisted of an ideal resistor and lumped inductors for the end cap terminations. The lumped inductances were set as a variable and optimized to make the s-parameters of the ADS simulation match the HFSS simulation data. The ADS model appears below.

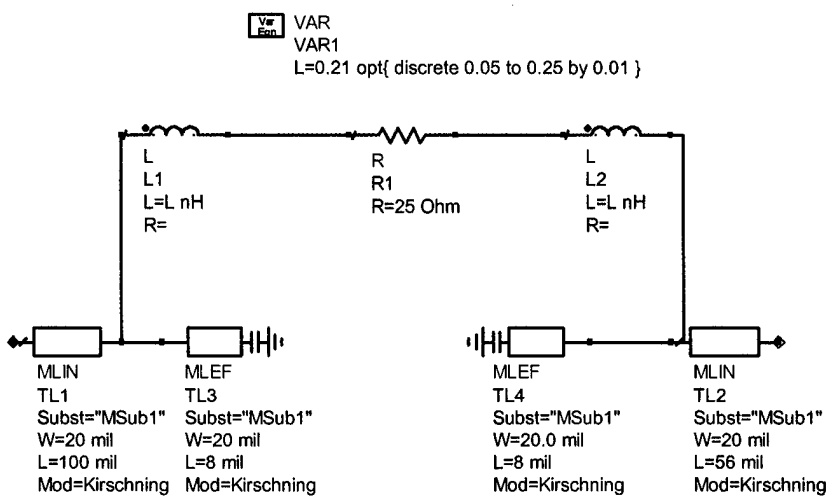


Fig 57. ADS Circuit Model for HFSS Correlation

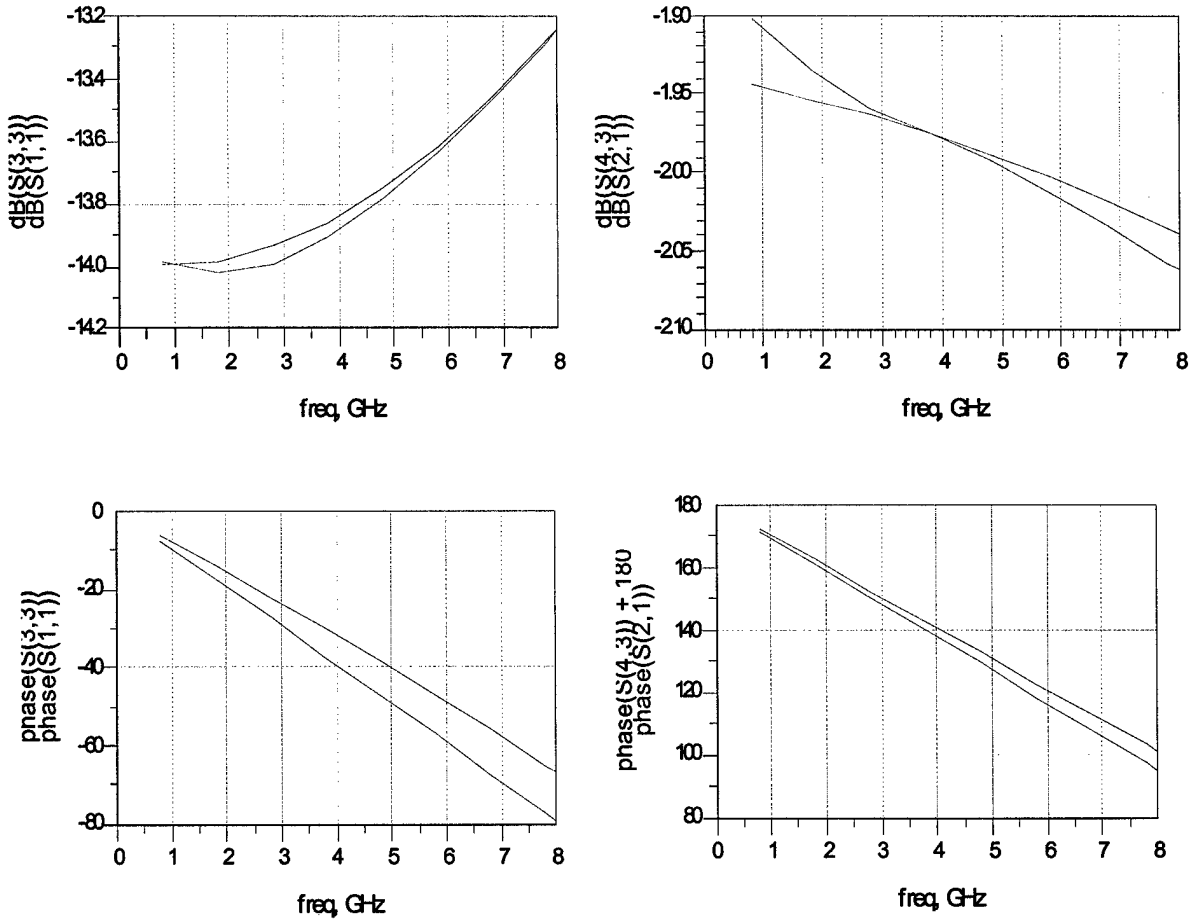


Fig 58. HFSS and ADS 0402 Resistor Simulation
HFSS – red: ADS – Blue

The ADS optimizer repeatedly tuned the lumped parasitic inductance (L) in the circuit model to 0.21nH in order to match simulation data. Thus, measured data, ADS circuit models and HFSS fields simulations are in consistent agreement with the package model of approximately 0.2nH per end cap termination. The frequency response of the two simulations below shows excellent agreement between the two models.

6 Conclusions

We have investigated the feasibility of using Avanti's self-aligning kinematic optoelectronic mounts for active 3-D RF/optoelectronic microstructures. The focus of this Phase I investigation was to study the interconnect structures to determine their mechanical registration precision, heat removal capacity, and ability to couple high frequency RF electrical signals between the multiple layers. We employed a number of simulations as well as experiments to quantify the performance of the interconnect structures.

Overall, we are very enthusiastic about the electrical feasibility of these microstructures as a way to construct high-performance, layered, optoelectronic circuits. Our electrical simulations demonstrated it is relatively easy to construct high-performance interconnects that are both manufacturable and consistent with Avanti's approach without unusual expertise on the part of the designer. For designs up to 15 or 20 GHz, it seems feasible that simple CAD design rules will suffice for guiding the designer. Beyond 20 GHz, we cannot say because we are not confident the simulations remain accurate. However, experience suggests that this methodology will support designs well above 20 GHz. The only uncertainty is the level of burden on the designer to "tweak" the design.

Coplanar and finite ground coplanar waveguides on silicon were designed and simulated with HFSS. The return loss plots demonstrate that the structures can easily be designed to function properly and that the 3D electromagnetic simulations were modeled and run to produce satisfactory and reasonable results.

The focus of the electrical study was on three dimensional waveguide transitions. Air gap solder bridges perpendicular to the waveguide were found to provide good electrical interconnect performance. It appears to be feasible to maintain –20 dB return loss up to 20 GHz even with several cascades of inter-level interconnect. In general, it was found that decreasing the air gap spacing (increasing circuit density) decreased the precision with which the solder profiles need to be controlled. For larger gap spacings, it was found that the solder towers needed to realize a series inductance to maintain impedance. This series inductance was realized by making the solder profiles hourglass in shape with narrower cross sections in the middle.

Thru vias in silicon were modeled with HFSS. Cylindrical plated vias provided reasonable return loss but present more complex fabrication issues. Anisotropically etched V-groove via models with bulk plating everywhere inside the V-grooves showed very poor performance. Structures of this type would be easy to fabricate but we did not have time to simulate structures with controlled line widths descending along the angled

surfaces. Our intuition suggests parts of this type, with masked traces on the V-groove surfaces, will perform better, but fabrication is more difficult.

High frequency measurements of 3D structures were correlated to simulations. Because existing structures and test fixtures were used, a sub-step was required to correlate the measured data to the field simulations. First, the measurements were matched to ADS circuit simulations. This allowed modeling of the test fixture and de-embedding of the device under test (DUT). A process was found to consistently de-embed DUT characteristics in ADS. Finally, full-wave 3D HFSS simulations of the DUT mounted on microstrip lines were found to agree well with the ADS models. Thus HFSS simulation data was linked to measured data through equivalent ADS circuit models.

On the thermal front, removal of heat generated by the RF and optoelectronic circuitry is aided tremendously by solder columns, which are also integral to the electrical interconnect structures between layers. We modeled a four-layer stack, plus base layer, under a variety of assumptions including imperfect thermal contact, presence/absence of solder, and the attachment of a "thermal pigtail." With 100 mW of power dissipation on each layer (a total of 400 mW), the temperature rise was only 5.2 C above ambient with poor thermal contact between the mesas and v-grooves. Adding 900 mW to the top layer (1300 mW total) produced only 25.2 C temperature rise. These are reasonable power densities and manageable temperature rises for the types of circuitry to be expected.

The mechanical precision of the kinematic interconnects should allow for optoelectronic components to be positioned to within a few microns with very high yield (90 – 99 %). This will facilitate passive placement of multimode fiber optic components. It is also possible to assemble devices at high speed, under certain conditions, to about one micron with a yield of 60 percent. This is sufficient for some single mode applications where volume of production is more important than coupling efficiency. We have also identified several potential approaches to improve the repeatability of the kinematic mounts, but these will require further testing.

To sum up, these investigations indicate that layered, RF optoelectronic microstructures with precision mechanical interconnects should have excellent thermal, electrical and optical performance while benefiting from direct compatibility with existing planar RF devices and the broad manufacturing infrastructure of the planar fabrication industries (both IC and PCB).