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This document describes a new CCD camera controller adapted to Schmidt telescopes. If several large CCD detectors can be adapted in the focal plane of a large Schmidt telescope, deeper digital images can be obtained, the operating cost of a CCD camera is several orders of magnitudes smaller than that of glass photographic plates. This also opens new ways of using Schmidt telescopes; i.e., real time detection of celestial sources.

This report contaings the following sections:
Requirements analysis
Description of the Loral CCD442A CCD
Description of the camera controller
Physical implementation of a mono CCD camera
Physical implementation of a multi CCD camera
Appendix 1: Controller schematics
Appendix 2: Data sheets of the the major components
Appendix 3: Information about the microcontroller and its software

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The O.C.A. Schmidt telescope CCD camera controller

Alain Maury

December 1996

This document describes a new CCD camera controller adapted to Schmidt telescopes. It is the final report for EOARD contract ##SPC-93-4007. 93W00076

It contains the following sections :

- **Requirements analysis**
- **Description of the Loral CCD442A CCD**
- **Description of the camera controller**
- **Physical implementation of a mono CCD camera**
- **Physical implementation of a multi CCD camera**

The schematics of the controller can be found in Appendix 1, and the data sheets of all the major components in Appendix 2. Information related to the microcontroller and its software can be found in Appendix 3.

Cover image : Comet Hale Bopp near Globular cluster Messier 14, taken with the OCA Schmidt telescope CCD camera, on October 30th 1996. 30 seconds exposure without filter. Alain Maury.

The main reason leading to the replacement of photographic plates by CCD detectors in wide field telescopes is the progressive discontinuation of photographic plates by Eastman Kodak.
The second factor is that the larger and larger CCDs are manufactured, and the price of large CCDs is decreasing. It becomes possible to build a large multi CCD camera for a relatively low price. If several large CCD detectors can be adapted in the focal plane of a large Schmidt telescope, deeper digital images can be obtained. the operating cost of a CCD camera is also several orders of magnitudes smaller than that of glass photographic plates.
This can also open new ways of using Schmidt telescopes, i.e. real time detection of celestial sources. This project has been mainly oriented toward the real time detection of Earth Grazing Asteroids (EGA).

Requirements analysis

The first step is to determine the different properties of the electronic system (the "controller") required to drive several CCDs at the focal plane of a Schmidt telescope. These are examined in detail in the following paragraphs.

Schmidt focal sphere :

A typical "big Schmidt" telescope focal plane is in the order of 30 to 35 cm wide on a side, with a focal length not too different from 3.15 meters, giving a scale of slightly larger than 1 arc minute per mm, or 15 microns per arc second.
In the Schmidt telescope optical design, the focal locus is a sphere, and this means that the usual photographic plates are bent in a special chassis in order to obtain sharp images.
In order to use flat detectors it is necessary to use field flattening optics, unless the detector is itself small enough to intercept a part of the sphere small enough to be considered flat (typically less than 10 mm wide).
In our case, the CCDs have a 30.72mm side and this would lead to a defocalisation of +/- 37 microns across the CCD diagonal. Such a defocalisation is usually clearly visible in focus plates, and could cause deterioration of image point spread function (psf) across the field (which in turn could give inaccuracies in psf based photometry).

Space requirement :

The small size of CCD detectors, combined with the large size of the camera dewars and electronics have prevented their use inside Schmidt telescopes until now when technology and reduced price has allowed to design multi CCD cameras for smaller telescopes.
The group working at the University of Tokyo is the current leader in the developement of multi CCD arrays for wide field telescopes with an array of 8x8 1K CCDs in use at Las Campanas Observatory in Chile. The same group is also involved in the large CCD camera currently built for the Sloan Digital Sky Survey.

Elsewhere, when CCDs have been used with Schmidt telescopes, they have mainly been conventionnal observatory cameras used either at the "newtonian" Schmidt focus, (Brorfelde, CTIO, KPNO) i.e. the camera being mounted on the side the telescope's tube, and the optical path being sent outside the optical tube by a flat mirror at 45° angle, or at the Cassegrain focus (Uppsala), an hyperbolic mirror bringing the optical path behind the main mirror.
A "true" Schmidt CCD camera, i.e. placed directly at the focal plane, can contain many large chips, using very compact electronics and non obstrusive cooling systems. Usual cameras are mounted at the back of the telescope, and space is not a major problem. A typical plate holder is less than 10 centimetres thick, and cannot generate much heat in the optical path without affecting the quality of the images.
The CCDs can be mounted in individual cold boxes, each having its own field flattening lens. They can also be abutted, but these specially made CCD chips and packages are usually more expensive than off the shelf CCDs, and finally the CCDs chips can be mounted on a single silicon substrate. For cost reasons, we have chosen the first approach.

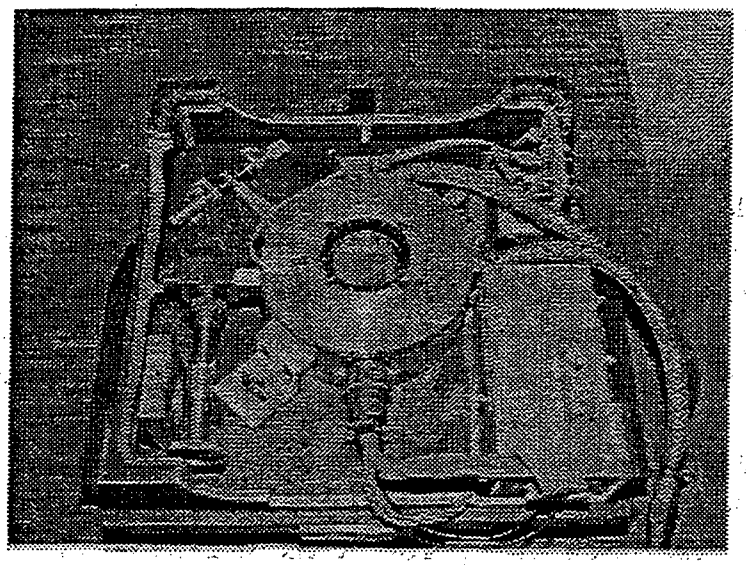
Budget requirement :

Because these telescopes are not large telescopes with important budgets, and because of the high price of the technology used, it is important to find ways to substantially lower the price of a multi CCD camera so as to be able to convert the telescope from photography to CCDs.
For example, a typical price for a thinned 2048*2048 pixel chip from SITE/Tektronix is in the order of $80,000. A typical commercial price for a single camera controller without CCD is in the order of $20,000 or higher. The complete price of such a multi CCD camera using commercial hardware, not taking into account the price of the associated computer system could easily cost several years of the regular operating budget of these instruments.
Procuring 9 large CCDs may also be a difficult task, mainly if the CCDs are thinned back illuminated models. We chose to use a "catalog" CCD, i.e. one which we knew we could order off the shelf. The Loral CCD442A is such a CCD. While grade 1 versions cost $20,000 each, grade 4 is only $2,000 a piece, and we felt we would cover more sky (i.e. discover more objects) using 9 grade 4 than a single perfect grade 1 chip. Our experience has shown that most of these grade 4 were quite useable with only a small numbers of defects, except one chip which we will have to replace.

Mechanical requirement :

Since flat field correction lenses should be used, it is preferred to place small plano convex lenses in front of each CCD instead of a single large lens which would introduce a much larger chromatic aberration. Flat fielding a Schmidt telescope focal plane using plano convex lenses is a technique developed almost with the invention of the Schmidt telescope. We use silica plano convex lenses of 1040 mm radius of curvature. Simulations made by an optician at the O.C.A.

have shown that distorsion and other aberrations created by such a small lens are negligeable. Because the focal surface of a Schmidt telescope is spherical, each CCD must be positioned precisely tangent to this sphere. This involves a mechanism able to move precisely the CCD in height (focus), local tilt in X and Y, rotation (in order to get the CCD lines oriented in respect of the right ascension and declination), and translation in X and Y in order to place the CCD correctly with respect to the other CCDs in case of a multi CCD camera.
This mechanism has to be relatively compact in order to fit inside the telescope's focal plane. This can be done either during assembly, the CCDs being glued in place, (preferably the right one), or the CCDs can be installed on adjustable support, which can be adjusted afterwards if necessary. Test images, similar to focus plates allow to measure the relative positioning of the CCDs and permit precise corrections to be made. An iterative alignment process should be completed in less than a week.



The current camera system is a single CCD module, and tilt adjustments are provided by the focalisation system of the regular photographic plate holder, which uses three separate focussing screws of high precision. The picture above shows the modified plate holder with the camera cold box at its center. The CCD chip is seen under the field flattening lens. A vaccuum valve is seen on the left of the box. A rotation system is seen at the upper left (tangent arm with adjustment screw and counter spring). Glycol pipes are seen going out of the right. The "command" and "data acquisition" boards are contained in the small box in the lower right. Not seen here is a filter wheel and shutter assembly which covers the whole unit while inside the telescope.

CCD arrangement :

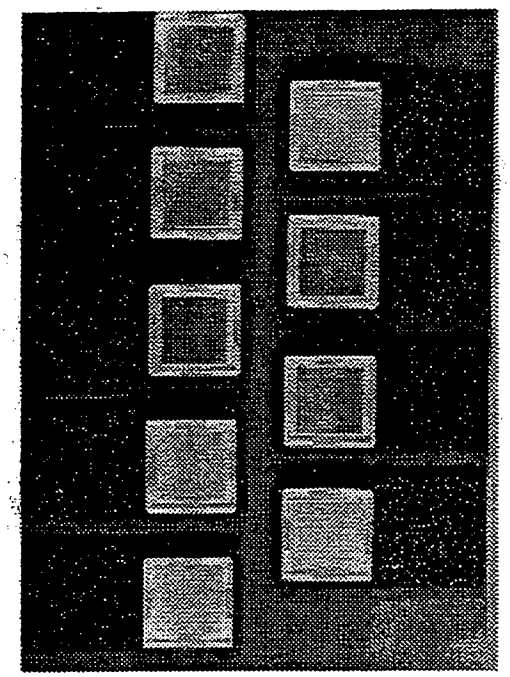
In the current camera, the CCD is placed simply at the middle of the field. Off the shelf CCDs are generally not buttable. When and if we will use several CCDs inside the plate holder, the

logical choice will be to use a staggered array design (see following picture), which allows independent assembly of each individual CCD camera. 9 CCDs could be used in this camera, giving a vertical field of view of 5 degrees, i.e. compatible with the regular field of view of a Schmidt telescope.

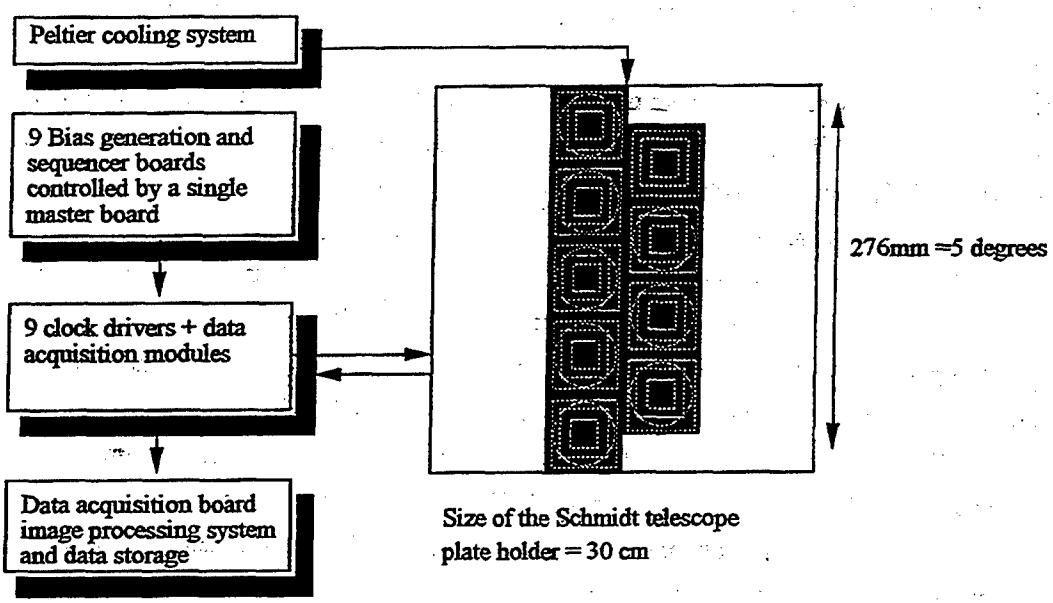
In this design, each CCD is separated from the others in the matrix by exactly one CCD field. This way, a given CCD will image an area of the sky comprised in declination between the one above it and the one below it in the other column with a small overlap.

Dealing with the data flow of such a camera is possible using today's computer technology.

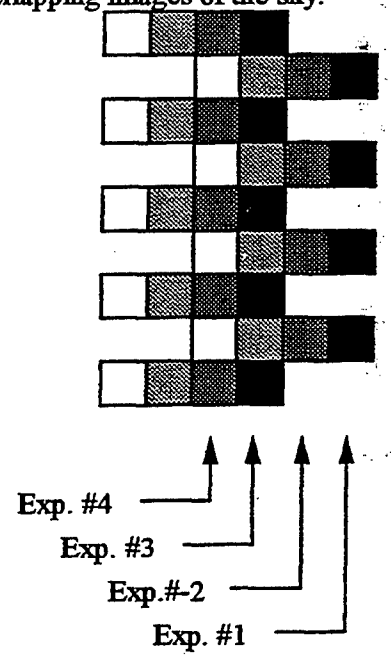
While currently the Loral 442A is the less expensive CCD (as far as $/cm^2), larger CCDs, while more expensive allow to build cheaper cameras, since less electronics and mechanical hardware is required to use them. The logical choice is always to use the largest possible CCDs available. For example, it would be easier to replace the current CCD in our camera with a newly produced Philips 7x9K chip (84x110mm of sensitive area, or almost 10 times the sensitive area of a 2K device) than to build a multi CCD camera using 9 individual 2K devices requiring complex adjustment systems and several controllers. In this case, another type of relative positioning of the CCD must be decided upon, but the general idea of staggering the CCD eases the non redundant coverage of wide sky areas.



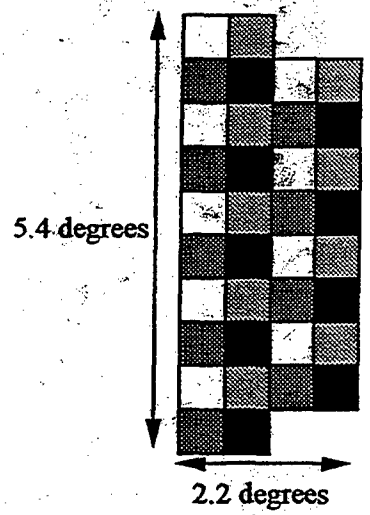
Positioning of 9 CCD modules in the focal plane of the Schmidt telescope



RA shift mode : Several exposures with a 30 arc minutes drift in right ascension give several overlapping images of the sky.



Quad-exposure mode : 4 individual exposures recreate a contiguous 11 square degrees exposure



Readout rate : A typical Schmidt telescope has a very fast F/ratio, leading to bright images which are most of the time photon noise limited unless using inteference filters. When a small amount of Moon and cirrus clouds are present in the sky, it becomes very difficult to obtain images which are not saturated. Under these conditions, it can be proven that the readout time

of the CCD must be relatively short. Astronomers tend to read CCDs at a typical 40000 pixels per seconds rate so as to preserve a low readout noise. Increasing this rate increases the readout noise of the camera, but it is necessary to realise that the value which needs to be improved is the final signal to noise ratio (SNR) of the image.

Because of our fast F/ratio, time is better spent collecting photons than reading them with the uttermost precision. The slight loss in SNR is easily compensated by a slightly longer integration, much shorter than would have required a longer readout time.

The total time required for the exposure is the exposure time *Te* plus the readout time *Tr*. The readout time is equal to the total number of electrons collected divided by the electron flux per second. This number of electrons is equal to the number of incident photons on the detector times its quantum efficiency in the given passband.

$$T = Te + Tr = \frac{E}{\psi} + Tr \qquad (1)$$

A simplified expression for the Signal to Noise Ratio of the sky in a given CCD exposure, not taking thermal current into account, is :

$$SNR = \frac{E}{\sqrt{E + RON^2}} \qquad (2)$$

Where RON is the readout noise of a CCD controller. It decreases with the square root of the readout time. If the readout noise has a given value at a given time, the readout noise for another time is given by :

$$RONt = RONo \times \sqrt{\frac{To}{T}} \qquad (3)$$

Squaring equation 2, and inputing equation 3 in order to express E in function of a "reference" readout time gives equation 4 :

$$E^2 = SNR^2 \times (E + RONo^2 \times \frac{To}{T}) \qquad (4)$$

Solving equation 4 in E gives equation 5 :

$$E = \frac{SNR^2 + SNR \times \sqrt{SNR^2 + 4RONo^2 \times \frac{To}{T}}}{2} \qquad (5)$$

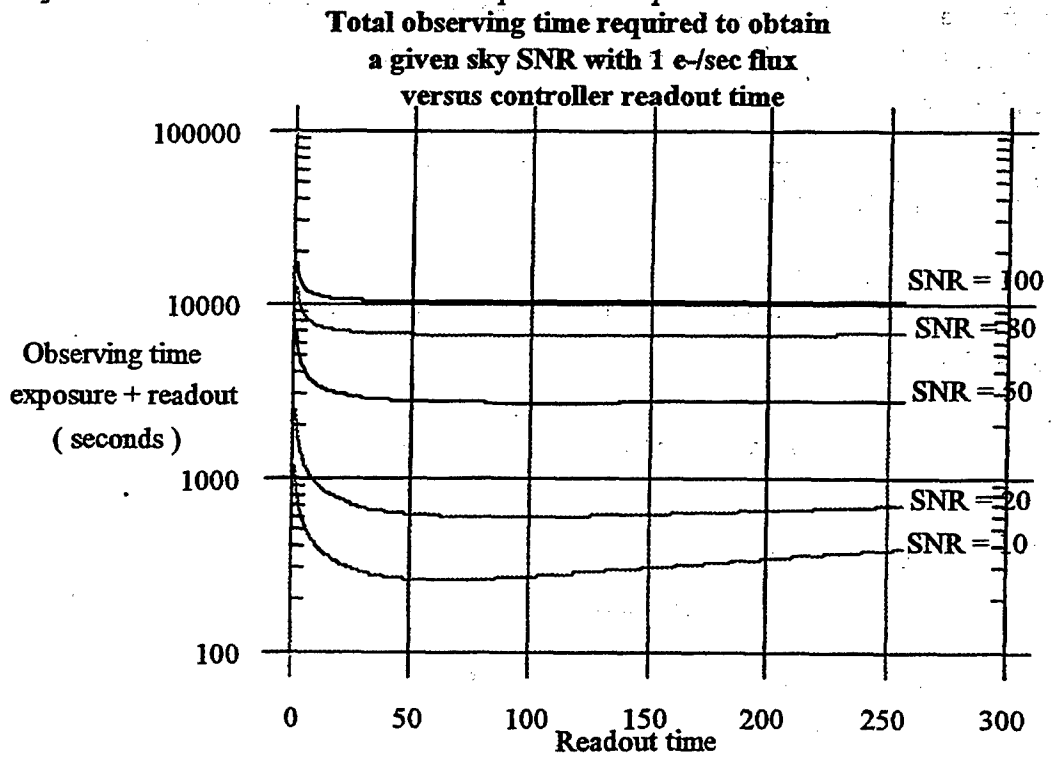
Using equation 1 and 5, we can obtain equation 6 which gives the total exposure time versus the photon flux, the controller "reference" readout noise and the readout time :

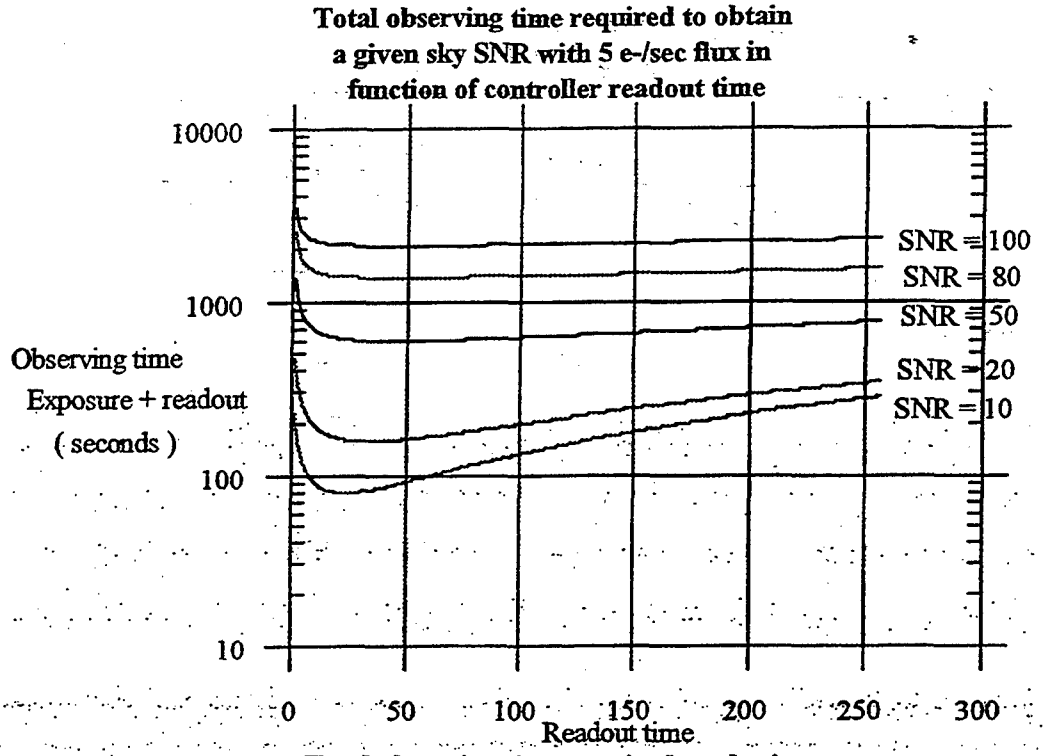
$$T = \frac{SNR^2}{2\psi} + \frac{SNR}{2\psi} \times \sqrt{SNR^2 + 4RONo^2 \times \frac{To}{T}} + Tr \qquad (6)$$

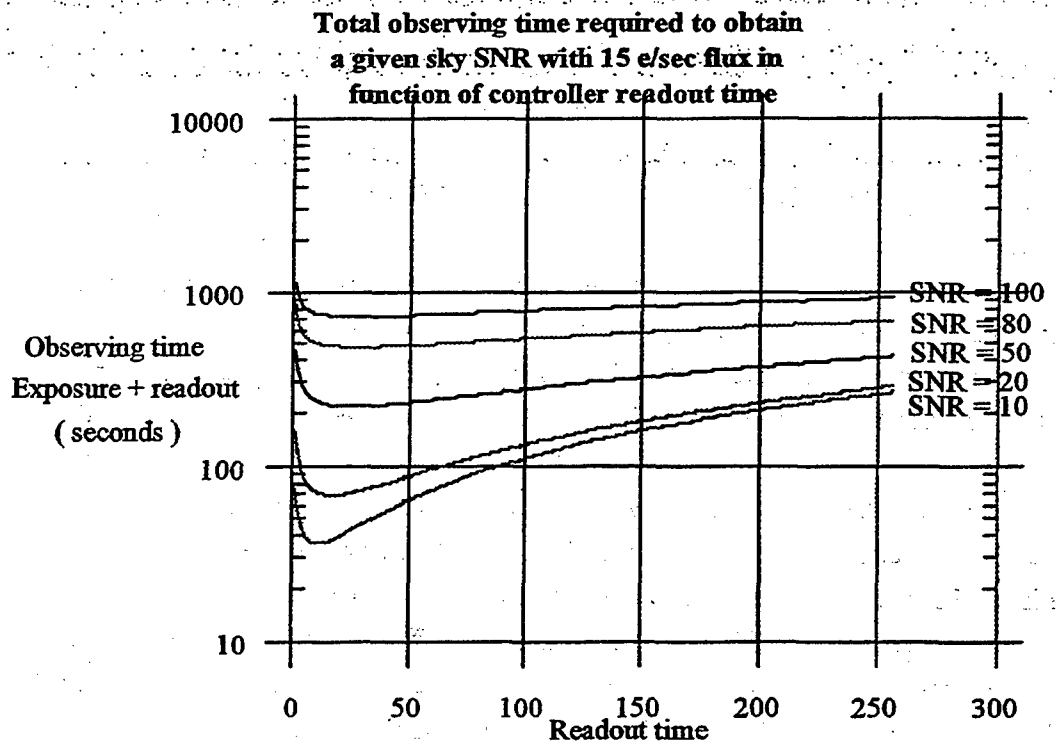
I ran a short simulation using a spreadsheet program using equation 6 with typical values in order to plot the required observing time (exposure plus readout) versus readout time for different sky signal-to noise ratio. To generate these tables, I used the case of a controller with a readout noise of ten electrons at 35000 pixels per second readout rate (28 microseconds per pixel). This would cause a 2K CCD to be readout in two minutes. From this value, we can extrapolate other readout noise at faster conversion rate.

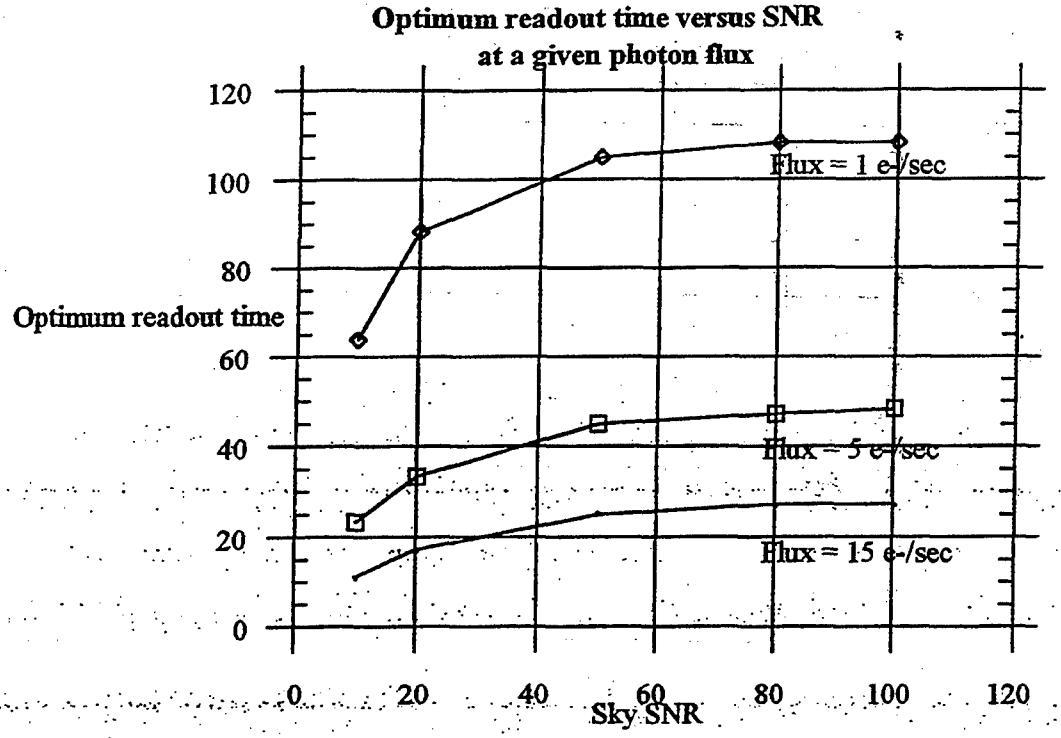
I chose 3 different electrons fluxes which are representative of the average sky brightnesses at our site in different conditions (without and with filters, depending of the filter).

I obtained the data of the fourth plot using the optimum points obtained in each curve of the first three. They show obviously that a good CCD controller should be able to adjust its readout rate with the expected sky flux of the exposure being read. It also means for example that an exposure taken with an optical filter should not use the same readout rate as an unfiltered image, provided that telescope time is considered important or expensive. This optimisation of telescope time should be mandatory on large telescopes. Most modern controllers are able to change their sequencing on the fly, and it is surprising that the adjustment of readout rate is not a widespread technique.




Total observing time required to obtain
a given sky SNR with 5 e-/sec flux in
function of controller readout time
10000
1000
100
10
Observing time
Exposure + readout
(seconds)
SNR = 100
SNR = 80
SNR = 50
SNR = 20
SNR = 10
0
50
100
150
200
250
300
Readout time


Total observing time required to obtain
a given sky SNR with 15 e/sec flux in
function of controller readout time
10000
1000
100
10
Observing time
Exposure + readout
(seconds)
SNR = 100
SNR = 80
SNR = 50
SNR = 20
SNR = 10
0
50
100
150
200
250
300
Readout time



Scan mode :

In order to decrease the effect of loss of observing time caused by CCD readout periods while covering large sky areas, it is also possible to use the CCD in scan mode. In this mode, the telescope stays at rest, with star images corssing the field of view at a regular pace. Electronic charges are shifted across the CCD in synchronicity with the drift of the stars across the CCD, and a continuous readout is performed. This mode is also called Time Delayed Integration (TDI). In order to do this, the CCD needs to be precisely aligned with the direction of the motion of stars (i.e. vertical register exactly perpendicular to the celestial equator).

If the telescope is at rest (so called sidereal scanning), the frequency of charge shift is proportional to the pixel scale, and the sky's rotation period divided by the cosine of the declination.

In our case, the field flattened camera has a focal length of 3140mm, one pixel equals 15 microns, or 0.98534 "/pixel, and we find that in order to shift the charges at the right speed, we need a time interval between each line of 65510.06813/cos(declination) microseconds.

From this, we can understand that this scanning frequency is different between the bottom and the top of the telescope field of view which are 5 degrees apart on the sky. Hence, in a multi CCD system, each individual CCD must be clocked at a different rate. Because of the asynchronicity between each detector, great care must be taken in order to avoid crosstalk between each CCD. In order to minimise this problem, the sequencer boards have a special reset and clock circuitry which automatically synchronises all the sequencer boards to a fraction of the microcontroller clocks. Also the master board which controls all the sequencers could generate a pixel synchronisation line on which a sequencer could synchronise its pixel readout.

There are other effects which are to be taken into account with the scan technique. The scanning performs a projection of a curved sky onto a flat detector. Two effects occur because of this : differential trailing is caused by the fact that the ideal scanning speed should be different between the top and the bottom of a CCD, and field curvature occurs because at high declination a star will not stay on the same line during its motion across the CCD.

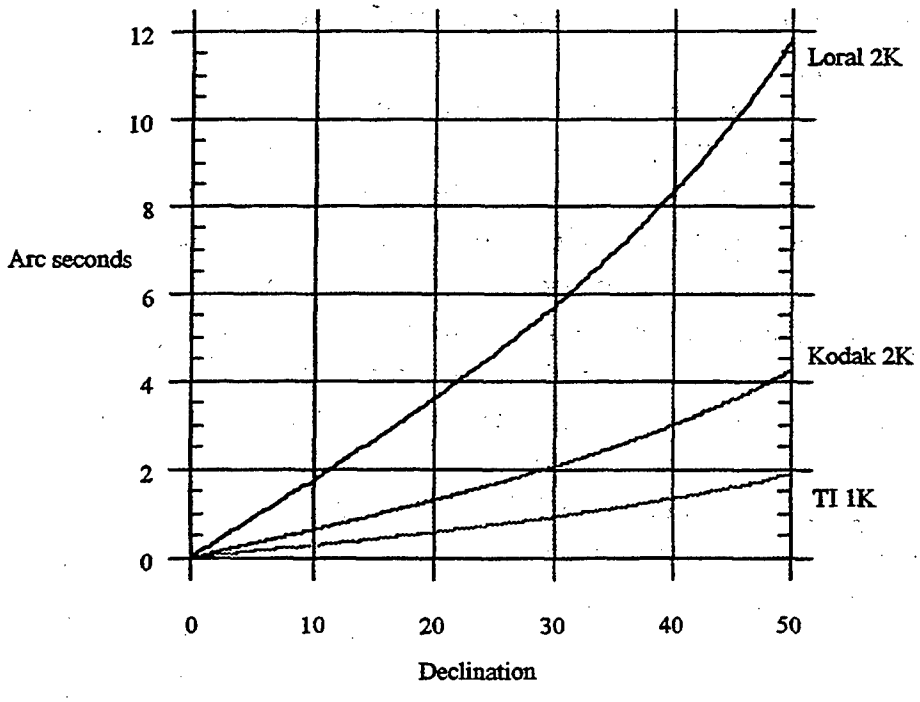
The beginning of the scan image shows a signal ramp caused by the fact that objects have integrated during a time which depended on their position on the chip when the shutter opened. Similarly, there is a ramp down at the end of the scan. The following diagram plots the trailing in arc seconds in the upper part of the CCD when clocked so that the central pixels are correctly drifted with 3140mm of focal length for 3 types of CCDs, i.e. Loral 2K (15 microns pixels, 30.72 mm on a side, 134 seconds of exposure time in sidereal scanning with our telescope), Kodak 2K (9 microns pixels, 18.4mm, 81 seconds) and TI 1K (12 microns pixels, 12.3 mm, 54 seconds).

If a is the field of view of the CCD, d the declination of the image, the trailing in arc second (if the angles are expressed in degrees) is :

$$t = 3600 \times \alpha \times \cos\left(\delta + \frac{\alpha}{2}\right) \times \left(\frac{1}{\cos\left(\delta + \frac{\alpha}{2}\right)} - \frac{1}{\cos(\delta)} \right)$$

In practice, with the CCD we use, differential trailing is visible at declinations higher than 10 degrees, and becomes unbearable at declinations higher than 25 degrees, as shown in the following diagram. With smaller CCD, the useable range is much higher, but the limiting magnitude is also much smaller.

Trailing at the north edge of a CCD in scan mode with the OCA Schmidt telescope



In our case, field curvature is not seen at declinations higher than 35 degrees, so is not a real problem.

A big advantage of scanning is related to the fact that since a given pixel in the final image is the average of all the pixels in a given line, images tend to be much cleaner in terms of cosmetic quality.

One of the requirements is that the readout time of a line be shorter than the time interval between two line transferts. One can increase the readout time (thereby decreasing readout noise) to the largest possible value. On the other hand, it is possible to move the telescope eastward so that the line transfert interval decreases to line readout time. In our case (pixel acquisition time of 5.5 microseconds, line readout time of 11.35 milliseconds), one can scan at the equator at about 5 times higher than sidereal rate, and cover an area of 43 square degrees per hour per CCD, to the expense of course of an integration time reduced to 26 seconds. This mode is very interesting in order to detect fast moving objects, which for longer integration times would have trailed over several pixels. Using 9 CCDs simultaneously, the coverage on the equatorial zone can be of 4600 square degrees in a single 12 hours night, or about 9% of the visible sky. Covering the whole sky twice per run becomes theoritically feasible.

The main problem is that the detection software has to be able to handle very large individual files, since we typically obtain 170 megabytes files in a matter of 45 minutes of observing time.

The main limitation in our case is the fact that the sky zone which can be scanned is limited in declination around the celestial equator.

In order to avoid these effects there could be three possible solutions :

- Scan along great circle (any circle containing the center of the celestial sphere). This is not possible in our case since the motorisation system of our telescope does not allow continuous motion in declination. Replacing the declination drive for example with a direct motor drive is a possible solution in that respect.
- As shown above, use smaller CCDs, since this will limit the viewing angle of the CCD. This solution is not practical since smaller CCDs provide shorter exposure times.
- Use a faster readout controller, so that the proportion of time spent reading out the CCD in stare mode be relatively small compared to the exposure time. The limit of this system is that readout noise increases with the square root of readout time, and that fast conversion time analog to digital converters of high accuracy are very expensive, bringing the price of the system much higher. I used a compromise by choosing a converter which main application is audio conversion, thereby allowing a low price, fast readout rate (1 pixel / 5 microseconds), and high accuracy (18 bits precision, truncated to 16 with 14 bits of linearity).

In term of time spent, scanning starts to be more efficient with our controller as soon as the length of the sky is larger than 6 degrees. Any speed gain over the converter we have been led to choose would become more expensive by a minimum factor of 6 (See budget requirements above...).

Reliability :

It seems clear to many users that the most often encountered failures are related to power supplies and to connections inside the camera. The actual design tendency is to limit the number of boards of the camera electronics to the minimum, and to use connectors soldered to the printed circuit board whenever possible.

Anti blooming :

Because the field of view of each CCD at our telescope (34 arc minutes) is quite large, and because their limited dynamic range, there are always bright stars in the field of view which end up being saturated. The charges bleed alond the column giving the familiar aspect of bright stars in CCD images.

Apart from the purely cosmetic problem, this may cause bright stars to hide other faint stars, and creates two more serious problems : The detection software will tend to detect fake stars across the blooming. In turn, this fake stars will tend to be aligned in successive frames, which will create fake asteroids detections. The second problem is even more serious : The best astrometric references are those of the Hipparcos catalogue, and are all brighter than the 10th magnitude. These stars are fully bloomed and are not measurable. The second best choice for an astrometric catalogue is the Space Telescope Guide Star Catalog, which is known to have precisions of only 0.3" in the best cases, compared to 0.001" for the Hipparcos stars.

These are a few reasons why a Schmidt telescope camera controller must include a provision for an anti blooming system. Such a system involves using a peculiar clocking pattern of the CCD during integration. This mode, also called partially inverted mode has been invented by Jim Janesick at NASA's Jet Propulsion Laboratory.

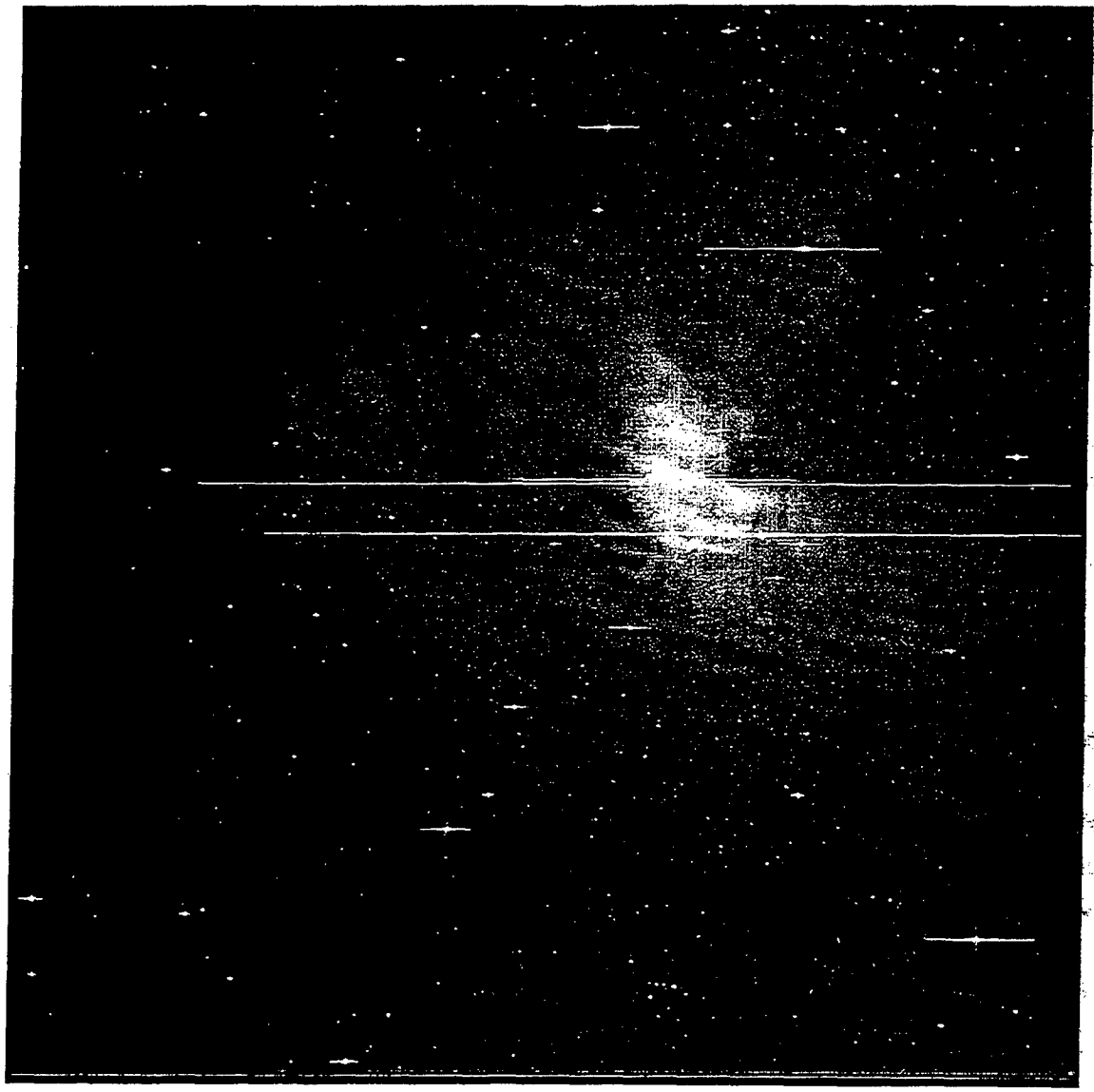
Tested thoroughly on Loral CCDs by a group at the University of Bonn led by Dr Reiss, it has also the very interesting property of doubling the potential well of the CCD. The penalty is that the thermal current is multiplied by 8 compared to the regular MPP mode operation.

For simplicity reasons, we chose to run the antiblooming frequency to a frequency just slightly higher than the time taken by a horizontal line readout (currently approximately 61 Hz), so that we would not have to invert the vertical lines while the horizontal register is being read. This is a relatively low "pumping" frequency, but it was find to prevent serious blooming from even magnitude 2 stars on a 30 seconds unfiltered exposure. The readout noise has been found to increase from 27 to 35 e-, which is still very adequate taken into account our average sky background signal. This mode has become the standard mode of exposure. Efforts are currently being made in order to use this mode during scanning.

Temperature control :

This leads to the last consideration of this "wish list", i.e. that of temperature control. To decrease the CCD thermal current it is necessary to refrigerate it. The rule of thumb is that the

30 seconds exposure with the OCA Schmidt telescope CCD camera using the antiblooming mode.



Same conditions as previous exposure, but using regular MPP (non antiblooming) mode.

thermal current doubles every 7 degrees C. There are two classical ways of cooling a CCD : Thermoelectric cooling and liquid nitrogen cooling. The first technique is able to lower the CCD temperature to -50° in the best cases (lower temperatures can be obtained with smaller CCDs, but 2K CCDs are relatively large), and the other is typically used at -100 ° which removes all the problems associated with thermal current, since it is virtually inexistent at such temperatures (thermal current of 0.8 e-/hours have been measured for partially inverted CCDs at such temperatures). Whereas thermoelectric cooling is inexpensive, they are limited in their lowest temperature, and the heat generated by the Peltier modules has to be evacuated outside the telescope. In our case, we evaluate that the total wattage per CCD is in the order of 70 watts per module, leading to more than 600 watts to be evacuated from the telescope tube. On the other hand, liquid nitrogen systems are more expensive on the long run (up to 10 liters of LN2 may be used per night), but are very easily temperature regulated. The first mono CCD camera built using this controller is Peltier cooled, and the multi CCD system could be either liquid nitrogen or Peltier cooled.

We can derive from these consideration that a CCD camera controller adapted to a Schmidt telescope has the following properties :

- it has to be very compact
- it should not generate excessive heat
- it should be able to clock and read its several CCDs in a totally independent manner.
- It should be built so as to minimize the crosstalk between each CCD.
- It should allow stare and scan mode with fast readout (200k pixels/seconds) using dynamic anti blooming mode.
- Finally, it must be relatively inexpensive to build.

Description of the Loral CCD442A CCD

We chose to use Loral 442A CCDs. Their characteristics are listed below

Size	2048*2048
Pixel size	15 microns
Physical size	31.72 mm
Angular field of view	34.5 '
Number of CCDs/5 degrees	9
Pixel scale	0.979 "
Full well potential	220,000 e- in partially inverted mode
Price per sq. mm	$2.12

These CCDs are produced in Milpitas (CA - USA) by Loral Fairchild.

These CCDs are thick front side illuminated chips, which do not have a good blue sensitivity, but overall provide a quantum leap compared to photography since a 2 minutes exposures detect stars which would have required more than 30 minutes of exposures using a photographic plate.

Price considerations led to the use of grade 4 CCDs. The current price is $2,000 per chip. They should have a relatively high number of cosmetic defects, but most of these are hot spots (pixels generating a very high thermal signal), which disappears when the CCD is cooled down (lower than -30° C) and the CCD becomes almost as good as a grade 1 CCD, with only a few defects such as dead lines and the like. However, the price difference is such that 9 grade 4 CCDs are less expensive than a single grade 1 device. In fact the production of these CCDs have made such progresses that most of the chips sold as grade 4 are in fact grade 3 or better.

These CCDs have two readout registers, but because of a manufacturing options, only one can be read at a time, i.e. it is not possible to read the CCD as two 1k x 2k CCD. Their amplifiers have a peculiar double stage structure optimised for lower noise at very fast readout time.

While the package has 56 pins, a much smaller number needs to be brought out of the vaccuum. In order to simplify connections, we decided to connect the unused ATG pins to the positive rail of the vertical clocks. The other one (one the side of the amplifier being used) is run in parallel with vertical clock #3 (A3). Thus the pins coming out of the cold box and their operating voltages are the following :

Vertical clocks :

A1 +3 to -8 volts
A2 +3 to -8 volts
A3 +3 to -8 volts
ATG -8 volts

Horizontal clocks :

H1 +5 to -5 volts
H2 +5 to -5 volts
H3 +5 to -5 volts
OSG +5 to -5 volts

Reset gate clock:

RG +8 to 0 volts

Other voltages :

VSS 0 volts
VRD 13 volts
VRT 3 volts
VOG 1 volts
VDD 22 volts

This is a total of 14 wires coming out of the CCD cold box (plus 2 for the temperature control and 4 for the peltier power supply).

Description of the camera controller

In order to achieve a fast readout rate, it was decided to use individual low cost controllers for each camera module linked together by a single master board able to give orders to and synchronise each modules. In single CCD mode, the program on the sequencer board interprets the data directly from the PC (master board not needed).

External backplane:

Each controller is made of four main boards. One contains all the power supplies and bias generation for the CCD and is usually located outside the telescope's tube. Another board is the sequencer board, and is also a Euroboard. These euroboards fits into a double G64 rack having two backplanes. Such backplanes are commercially available. They use DIN40162 connectors. The connection of these backplanes are given in a following figure. A master board, able to interpret orders from the PC and able to send orders to all or a single sequencer can also reside on this backplane.

Connexion to the euroboard backplane:

Pin	Name	New	Pin	Name	New
1b	GND	GND	1a	GND	GND
2b	A8	Reset	2a	A0	32MHz
3b	A9		3a	A1	
4b	A10		4a	A2	
5b	A11		5a	A3	
6b	A12		6a	A4	
7b	A13		7a	A5	
8b	A14		8a	A6	
9b	A15		9a	A7	
10b	*BRQ		10a	BGRT	
11b	*RRQ		11a	RGRT	
12b	*BGACK		12a	*HALT	
13b	Enable		13a	MCLK	
14b	*RES		14a	*VPA	
15b	*NMI		15a	RDY	
16b	*IRQ		16a	*VMA	
17b	*FIRQ		17a	R/*W	
18b	IACK		18a	Halt Ack	
19b	*D12		19a	*D8	

20b	*D13		20a	*D9	
21b	*D14		21a	*D10	
22b	*D15		22a	*D11	
23b	*D4		23a	*D0	
24b	*D5		24a	*D1	
25b	*D6		25a	*D2	
26b	*D7		26a	*D3	
27b	*Berr.		27a	*Page	
28b	Chain In		28a	Chain Out	
29b	+5 Batt.	30v	29a	-5V	
30b	-12v	+20v	30a	+12V	-20v
31b	+5v	+10v	31a	+5V	+10v
32b	GND	GND	32a	GND	GND

Notes :

- Pins 1 a and b, 29a, 30,31 and 32 a and b are used for power supplies. Please note the inversion between the polarity of 12->15 volts signals (-12 becomes +15 and +12 becomes -15v)
- Never use pin 28 a and b. In the original G64 bus, they are used as a way to daisy chain signals (i.e. 28b of a given board is connected to 28a of the next one on the backplane and so on).
- All the other pins can be used to send reset, clocks and communication signals from the master board to the power boards in a multi CCD system (communication from the master board to the sequencer boards).

Sequencer board:

The sequencer is a 87C750 Philips microcontroller. In the early phases of devlopement of this project, I chose to use an IFX780 Flexlogic circuit made by Intel, but it proved to be not flexible enough to allow on the fly reprogrammation in the different modes required by the camera. Moreover this particular chip is not made anymore The 87C750 is a limited version of the industry standard 80C51 microcontroller, with a master clock running at up to 40 MHz. This allows to clock the I/O ports with pulses as short as 300 ns. It is a small integrated circuit (24 pin DIL), having just the required function for our task. This part and its program is fully described in Appendix 3.

The microcontroller communicates via an asynchronous serial line implemented with 2 of the I/O pins to a PC interface board. In the case of a multi CCD system, these lines would be

replaced by a synchronous line (already implemented, but currently replaced by a simpler asynchronous line) generated by a Master board. This board would also be 80C51 based and able to drive up to 15 camera. The communication to the sequencer board can be made either directly through a pair of fiber optics emitter and receiver, or these can be disconnected and orders can be sent directly through the backplane. The connections to the backplane can be made through wire wrapping, allowing to configure the lines used for each particular sequencer board (allowing to address several sequencer boards independently).

Other I/O pins generate the timing required by the CCD. Adequate chips are used to send and receive these signals from the sequencer board and on the voltage translator board. A 34 conductor flat ribbon cable connects the sequencer board to a voltage translator board located near the CCD. Signals between those two boards are TTL levels. The connection plan for this cable is given in the following figure.

Connexion of the 34 flat ribbon cable.

1	VOD	2	VATG+
3	VRT	4	RG+
5	VRD	6	VA3-
7	VOG	8	VOSG+
9	VRG-	10	VH3+
11	VOSG-	12	VH3-
13	+15Va	14	-15Va
15	VA1+	16	GNDa
17	VH1+	18	VH2-
19	VH2-	20	VA2+
21	VH1-	22	VA1-
23	GNDd	24	VA2-
25	GNDd	26	+5Vd
27	P0-1	28	P0-0
29	Reset	30	P0-2
31	GNDd	32	GNDd
33	32 MHz	34	GNDd

Notes :

The negative voltages ramps of the clock signals all connects to the NC (normally closed) pins of the Max333A analog switches. The positive ones connects to the NO (normally open) pins of the switches.

I/O port assignment :

port 1 :	
pin 0 : H1	Horizontal clock 1
pin 1 : H2	Horizontal clock 2
pin 2 : H3	Horizontal clock 3
pin 3 : OSG	Output Serial Gate
pin 4: RG	Reset Gate
pin 5: CL1	First clamp, first channel
pin 6: CL3	Second clamp, first channel
pin 7 : Casc	Cascade pin

Note :

- Pins 3 to 6 of port 1 which are unused are brought to a small header which could be used for various purposes, such as controlling a shutter or rotating a filter wheel.
- Pin 7 is used to put the AD converter in the cascade mode, this allows to send the result of the conversion on both channels as a single 32 bits word. This allows to read channel 2, i.e. perform a temperature read.

port 3 :	
pin 0 : A1	Horizontal clock 1
pin 1 : A2	Horizontal clock 2
pin 2 : A3	Horizontal clock 3
pin 3 : ATGU	Upper Arrray Transfert Gate (in fact, no connect)
pin 4 : ATGL	Lower Arrray Transfert Gate (in fact, no connect)
pin 5 : CL2	1st Clamp, second channel (also used as TRANS)
pin 6 : CL4	2nd Clamp, second channel
pin 7 : STCVT	Start convert

Port 3 drives the three vertical clocks, and port 1 drives all the signals related to horizontal clocks and pixel conversions. In order to avoid jitter, it was decided not to use interrupts in the program. Another reason for this was that the 16 bits timer is too fast for our purpose.
The other bias voltages for the CCD come from the power supply board, and are linked to the CCD via an RC filter. We found out that several ideas we had about the sequencer (such as using binning modes, windowed modes, and other more exotic modes of operations) have never been used in practice. Recently, we cleaned up the software and removed all thes unused features. It is likely that if the camera had to be rebuild, a 16 bits solution or higher (i.e. 16 bits

microcontroller or DSP system) would be chosen. Having to count higher than 256 (a line count is 2048) is much simpler with a 16 bits system, whereras the 8 bit system requires a double loop whose synchronicity can not be maintained easily.

Power supply board:

The power board contains voltage regulators to provide for +5v and +/- 15 volts. It contains also voltage followers to generate adjustable power supplies. This board is inspired by the design of the Palomar controller (Gunn et al 1987) which we have used at the OCA for many years. It contains outputs which can be set between + and - 15 volts, and four others which can be set between 0 to 24 volts. We followed two suggestions by Dr F. Harris at the U.S. Naval Observatory Flagstaff, i.e. instead of using LF347 as in the original design, we use pin/pin compatible OPA470 which have a much lower noise. The higher voltage generators layout have also been slightly modified . The voltage reference is still an LM399. A 64 wire flat ribbon cable connects this power supply board to the voltage translator board (half of the wires are ground signals). No periodic signal which could perturb the CCDs are on this cable.
It is likely that in the future we will build a D/A based voltage board in order to automatically test the CCDs and find the best setting of a given CCD in laboratory. Prices of octuple D/A converters are now so economical that such a board might in fact be less expensive than the current model.

Voltage translator board :

The voltage translator board is 60mm x 150mm long. It contains all the electronics receiving the signals from the sequencer boards and driving the CCD. A similar board is mounted piggy back on this one and contains all the acquisition chain (analog and digital power supplies to the acquisition chain go through the 64pins flat ribbon cable going to the voltage translator board). Because of the anti blooming mode, it is required that the vertical drivers be relatively slow. This allowed us to use simple analog switches to drive both the vertical and horizontal clocks of the CCD. We chose Max333A quad SPDT switches, which receive both voltage ramps of the CCD clock from the power supply board, a logic signal coming from the 87C750, and drive the CCD pin through an RC filter.

Acquisition chain :

The acquisition chain is made of 2 OPA627 operational amplifiers by Burr Brown. A load resistor is connected to the video output of the CCD. Then comes a coupling capacitor hooked to an analog switch to provide an input clamp currently used as a line clamp (active during vertical time). The first op amp has a gain which is set around 10. The output of this op amp goes through another clamp active during the first video level. The second op amp is just a voltage follower. The analog switch used for clamping is a Maxim DG445, which we have

replaced recently with a faster, pin to pin compatible DG412 switch from the same manufacturer. The Analog to Digital converter is a Burr Brown part labeled DSP102, and is derived from the PCM1750, except its control is much simpler and its outputs are adapted to Digital Signal Processors (DSP). The DSP 102 is an 18 bits 5 microseconds conversion time and 14 bits linearity double converter. Input level must be between + and - 2.75 volts. We use it as a 15 bits converter. The clamp signals of the acquisition chain as well as the start convert signal are generated by the 87C750. While we have two acquisition channels on our camera system, we also found out we were never using the second one since our CCDs cannot be used with both amplifiers at a time. There is an option called "cascading" which allows reading of both channels and emission of the converted values as a single 32 bit word. We use this mode to read the temperature through a PT100 sensor connected to channel B of the converter. The "cascade" pin which allows this mode is controlled by the 87C750. It activates both the "cascade" feature of the converter and an extra Max333 analog switch in order to connect the temperature system to the input of the A/D converter. The DSP102 requires 8 and 16 Mhz clock to work at its maximum conversion rate. We drive the 87C750 at 32 MHz and use a binary divider (74HCT93) to generate the 16 and 8 MHz from the 32 MHz master clock. The A/D converter requires + and - 5 volts which are locally generated from the + and - 15 volts through low power 78L05 and 79L05 voltage regulators. The three outputs of the converter are emitted through fiber optics emitters made by Toshiba. These parts have the advantage of being directly TTL compatible. This board is actually routed using DIL circuits, but could be rerouted in a much more compact size using Surface Mount Technology versions of the different circuits, except for the microcontroller and the DSP102, which would be purchased in 24 pins flat packages, and the fiber optics drivers which are not available in any other packages than those actually used. It is also likely that if a faster converter becomes available (but in the same price and quality range than the DSP102), it will replace the existing one. Analog Device is said to sell sometimes in 1995 a 16 bits low cost 2.5 microseconds converter which will be called AD7882. Maxim has another interesting A/D converter named Max121 which, while only 14 bits in resolution, is faster (3 microseconds per pixel) and would be an interesting replacement.

Connexion to the CCD :

The connection of the controller board to the CCD is made through a regular DB25 connector. The connector on the cold box side is a vaccuum proof 26 pins circular connector. Connexion from the inside of the connector to the CCD is done using thin enameled copper wire.

Connexion of the DB25 connector to the CCD head

Pin number DB 25	Signal name CCD	Pin number circular conn.	CCD pin
1	A1	P	21, 48
2	A3 + ATGu	A	19, 47, 12, 51
3	OSG	C	24, 52
4	GNDa	G	1-3, 13-18, 22, 26-31, 41-46, 50, 54-56
5	GNDa	K	idem
6	GNDa	G	idem
7	GNDa	K	idem
8	VATG+ = VATGl	a	23, 40
9	VRT	M	6, 34
10	VOG	c	25, 53
11	NC		
12	GNDa	X	
13	PT100 F-	V	PT100 F-
14	A2	R	20, 49
15	ATGU	NC	
16	RG	D	4, 32
17	ATGL	NC	
18	H3	T	11, 39
19	H2	b	10, 38
20	H1	S	9, 37
21	VOD	N	8, 36
22	VRD	Z	5, 33
23	NC		
24	PT100 S-	V	PT100 S-
25	PT100 F+	E	PT100 F+
Video out upper		H	
Video out lower		J	
Peltier 1		L	
GND Peltier 1		Y	
Peltier 2		F	
GND Peltier 2		W	

CCD clocking :

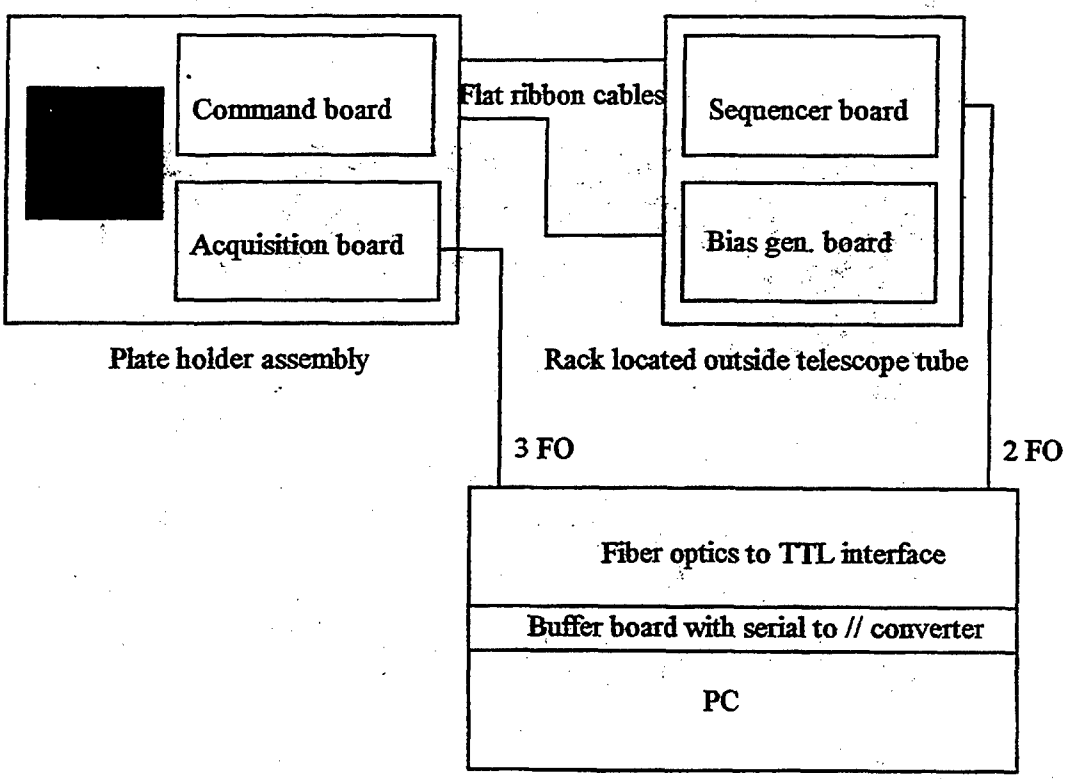
It follows the manufacturer's documentation. Please refer to it in Appendix 2 for more information.

The antiblooming mode is done according to the few published papers on the subject. The reference paper is "Preventing blooming in ccd images", J. Janesick. NASA Tech Brief Vol. 16, No 7, Item #71 from JPL Technology report NPO-18363/7886. Another more detailed one has been published by Kohley et al. from the radioastronomy institute of the Bonn University Bonn. our preprint is labeled " operating a large area MPP-CCD with antiblooming.

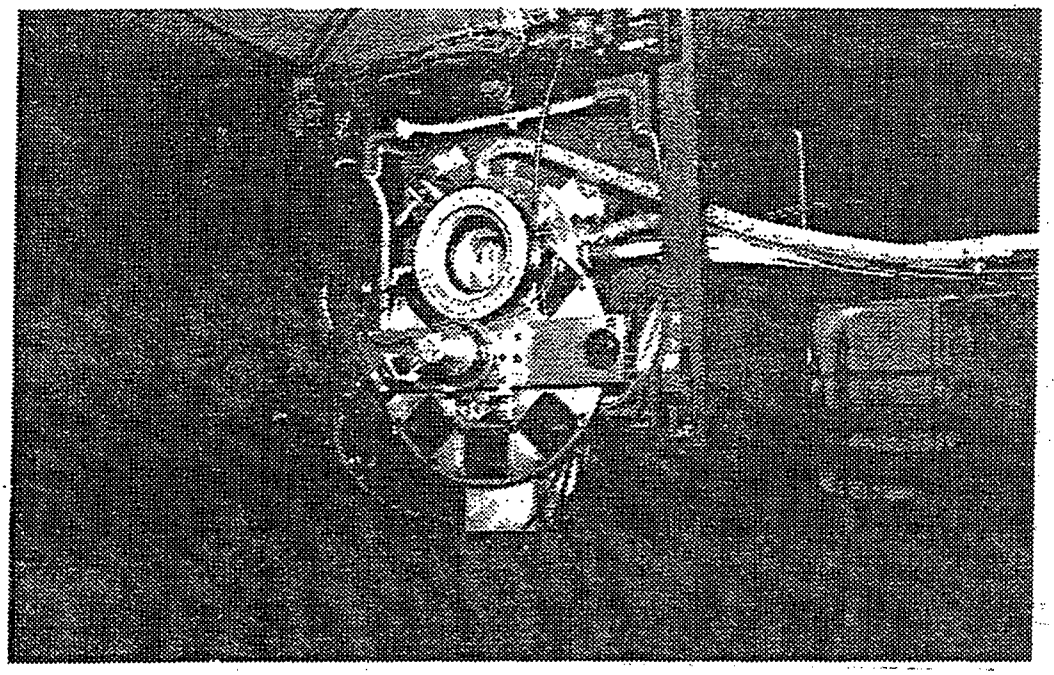
Implementation of a single CCD camera

Using this set of board, we built a single CCD camera. The overall configuration is given in the following figure. The control of the sequencer is done using a PC based interface board connected to its fiber optics transmitter and receiver through a simple TTL to fiber optics interface. This board has an 8.5 megabytes memory buffer large enough for a single 2K image. This interface board sends commands to the sequencer board, which drives the CCD. The video signal is sent through fiber optics to the interface board. When the transfert is done, the interface board memory is dumped into the PC main memory.

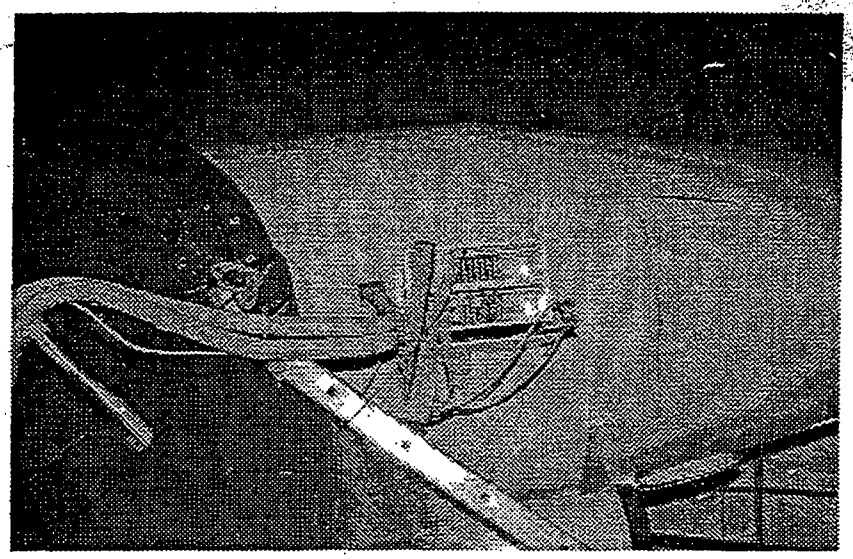
General layout of a single CCD system :



The camera plate holder being installed inside the telescope : The filter wheel and shutter assembly covers the camera body (this picture is an early assembly, now the electronic board has been mounted at the lower right of the plate holder instead of being located below the camera cold box as shown here).



The electronic rack located outside the telescope tube :



With the current system, we measured a signal chain gain of 4.6 e-/Data Number and a readout noise of 27 e- using a dual flat/dual dark method (the reduction method is described page 246

of Volume 22 of the Astronomical Society of the Pacific Conference Series "Astronomical CCD Observing and reduction techniques". CCD Data: The Good, The Bad, and the Ugly by Massey and Jacoby).

Readout time is currently around 50 seconds.

This camera is currently involved in several programs and since its commissioning, photography is now canceled at the telescope. We are using it 50% of the available time in order to detect Near Earth Asteroids. The detection software has been completed only recently and has enabled us to perform more than 400 detections on 141 individual objects in a 3 nights run (Minor Planet Circulars, December 1996).

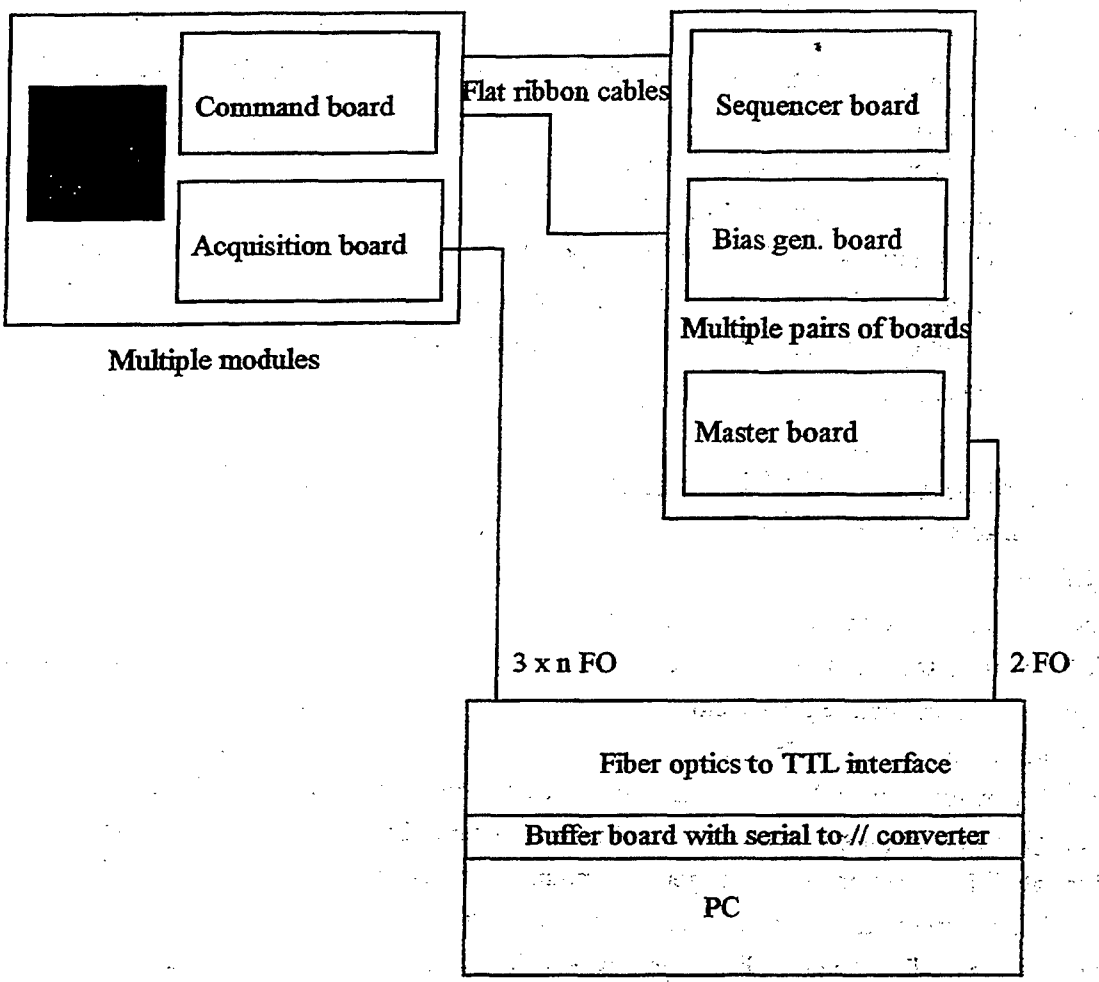
Implementation of a multi CCD camera

A system able to drive several CCDs can be implemented using the following design :

CCD control :

Each CCD has its own set of power and controller board located on the external rack, as well as its own voltage translator and acquisition chain. A master board, also on the backplane supplies a synchronous 32 MHz clock to each power board, as well as a general reset and serial interface to each module. It contains an 8051 microcontroller which is driven by an RS232C interface by the control PC. The connection of each module to a given backplane signal is made through wire wrapping connections. On the master board, the clock and reset signals are driven through TTL gates in order to get the required throughput. The clock line of the serial interface is synchronous to all the CCDs hooked to the system and generated by an I/O line of the microcontroller. The data line is generated using the other 15 I/O lines of the master board microcontroller. When the PC sends an order to this master board, it tells whether the order is relevant to a given CCD or to all the CCDs, the master board programs the CCDs adequately and waits for other orders.

Since each command board + acquisition board module is located in a 50x76x165mm box, such a camera would have to be installed in a specially designed holder (not a regular plate holder), with electronics board going on the side of the compact CCD cold boxes. The current electronic rack is large enough to contain up to 15 bias generation boards and sequencer board as well as the master board.


Command board
Acquisition board
Multiple modules
Flat ribbon cables
Sequencer board
Bias gen. board
Multiple pairs of boards
Master board
3 x n FO
2 FO
Fiber optics to TTL interface
Buffer board with serial to // converter
PC

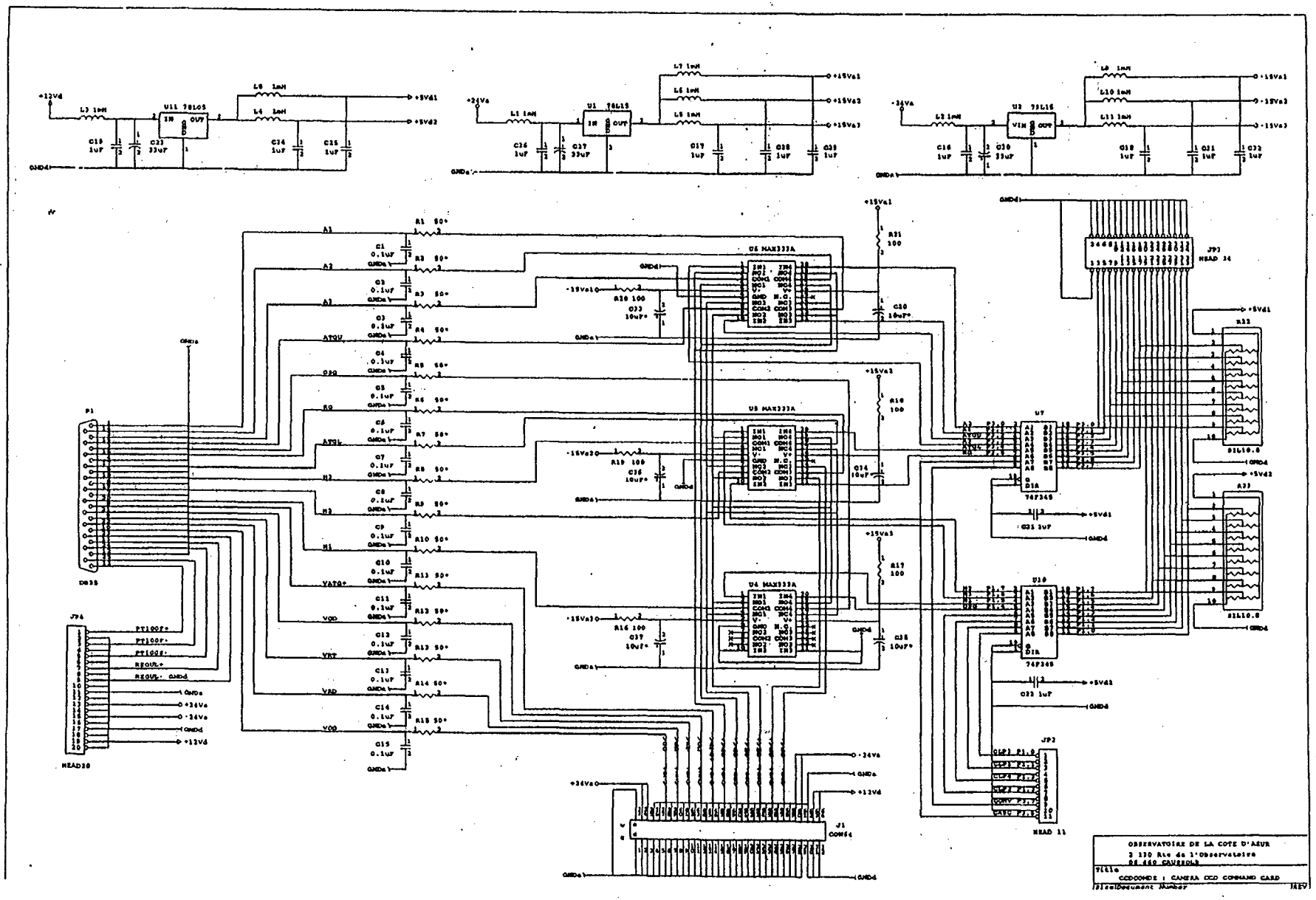
Appendix 1 :
Electronic Schematics of the controller

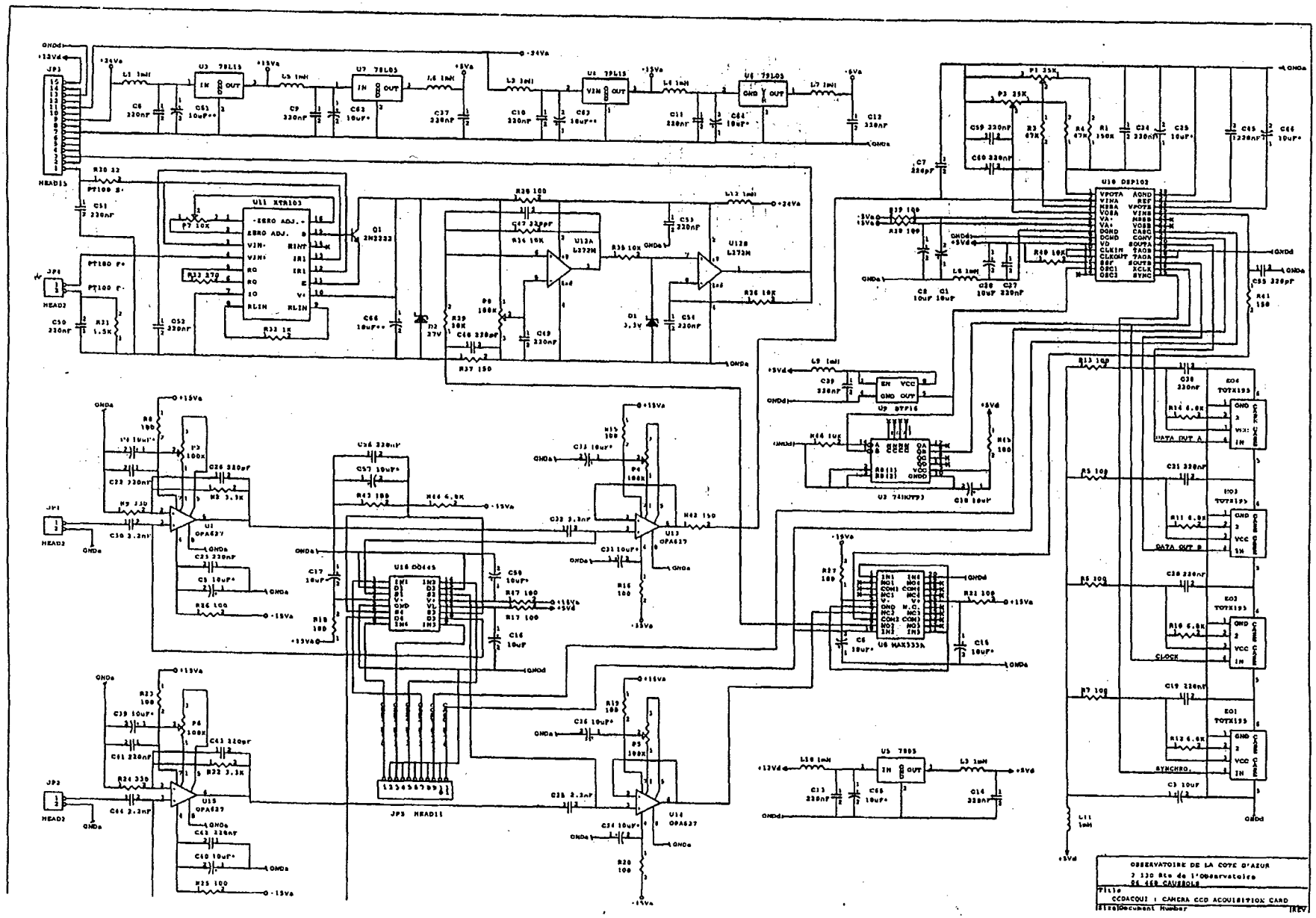
The schematics for the camera ave been edited using the Orcad package. The routing of the boards have been made either in Orcad's PCBII or using another package made by Protel. The following figures have been printed using a postcript printer (.ps extension)
For each design, there are several files with different extensions :
.sch -> schematics
.bom -> bill of material, these files have been edited in order to provide information about the manufacturers and/or the adress of the retailer we used.
.net -> netlist
.brd -> Board for Orcad
gbr files, including :
.tol

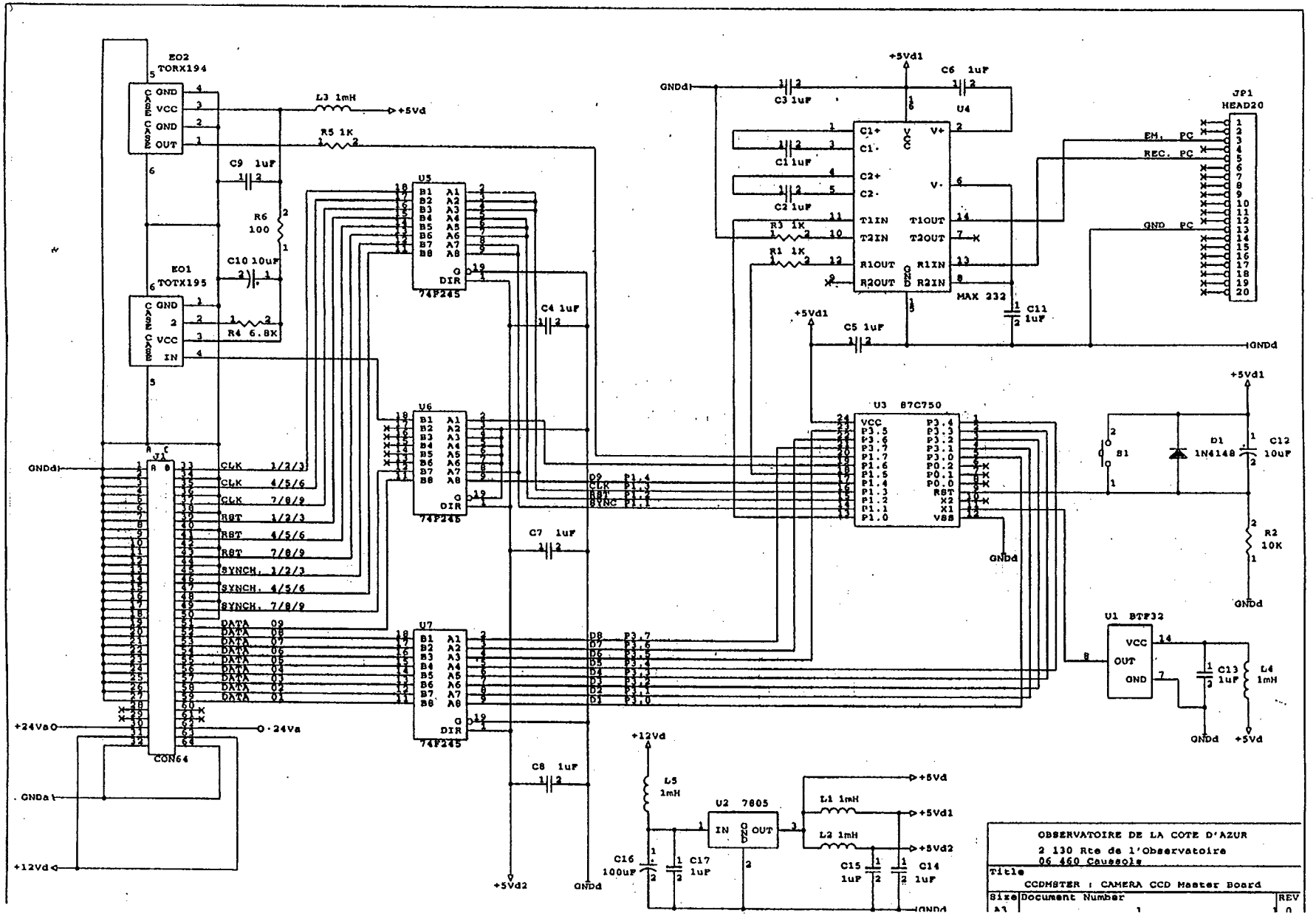
.gnd -> ground plane layer
.top

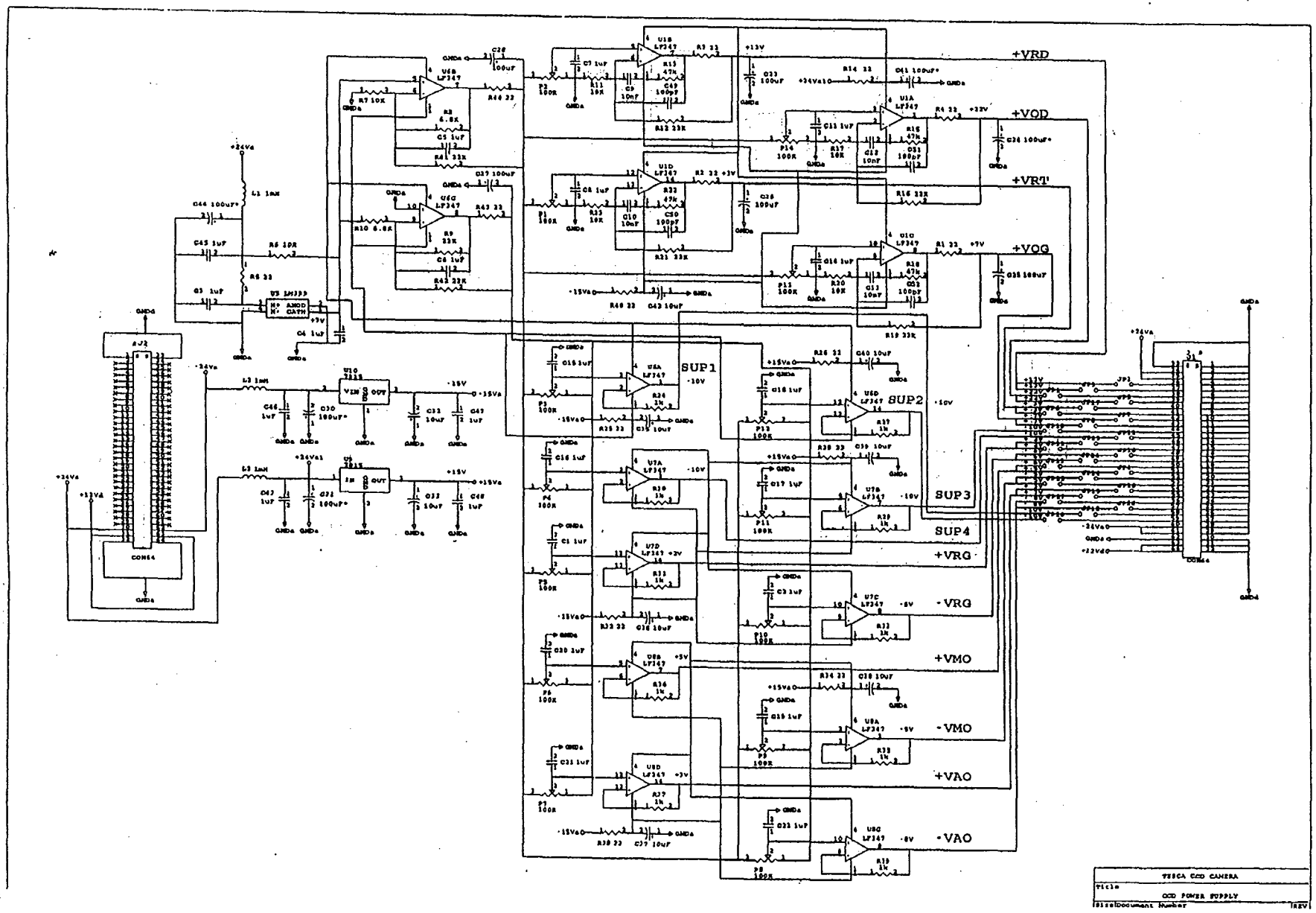
There are seven orcad based designs related to this controller.:
CCDSEQ is the sequencer board. It can be used in single camera mode without any master board or can be slaved to a master board.
CCDMSTER is the master board, which receives order from the PC printer board using a serial PWM communication protocol, and which gives orders to individual sequencers and provides a synchronisation signal so that eventhough the vertical transferts can be asynchronous, the pixel acquisition stays synchronous.
CCDPOW generates all the bias clock voltages required by the CCD.
CCDACQUI is the board which contains the amplifier chain and the A/D converter.
CCDCMDE is the board which receives signals from the sequencer (CCDSEQ) and from the bias generation board (CCDPOW) to generate the clocks to the CCD. It also generates its own power supplies.
PELTIER is a schematics for a current regulated power supply in order to use peltier modules. Since the parts are mounted on a large heat sink, there is no printed circuit board for this design.
CCDSUP relates to the CCD support, the small printed circuit board that supports the CCD inside its cold box.

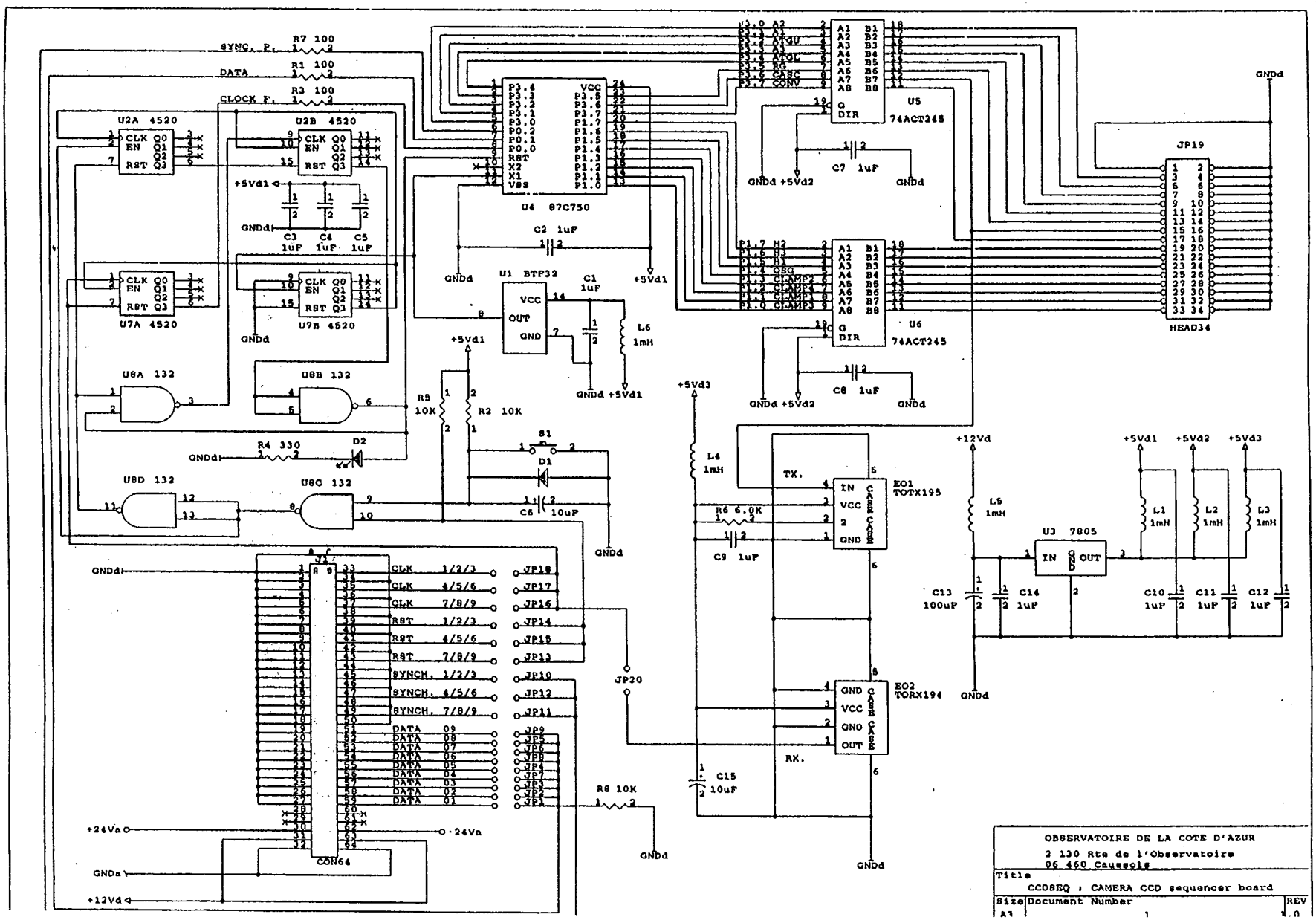
These, as well as information related to the programming of the sequencer and its use are also available through anonymous ftp at taranis.obs-azur.fr as a single file called OCACCD.zip. This file will be regularly updated as more functions are programmed into the sequencer.
It is highly recommended to ftp these files rather than to use the files decribed in this report. Also it is better to take contact with us (maury @ obs-azur.fr) since we have already have those boards fabricated and that the prices for these boards will be less expensive here since the required tooling fee for their fabrication has already been paid for. This design is going to evolve in the following months, and this is also why the latest version will be available from ftp or from us directly. We will improve it using faster converters, more elaborate sequencers and will implement a multi readout CCD system relatively rapidly now. Also on the drawing board is a low cost EPP (extended printer port) interface. We have been able to sustain 2 megabytes transfert rates using this technique. A faster PCI parallel board interface system will also be implemented if we change the camera system to much faster converters (like 2 MHz converters).
Following in the following pages are postscript prints of the schematics of the boards composing this camera.


OBSERVATOIRE DE LA COTE D'AZUR
2 130 Rte de l'Observatoire
06 460 CAUSSOLS
CCDCOMDE : CAMERA CCD COMMAND CARD
REV


OBSERVATOIRE DE LA COTE D'AZUR
2 320 Rte de l'Observatoire
06 460 CAUSSOLS
Title
CCDACQUI : CAMERA CCD ACQUISITION CARD
Document Number
REV


EO2
TORX194
GND
VCC
GND
OUT
L3 1mH
+5Vd
R5 1K
C9 1uF
R6
100
EO1
TOTX195
C10 10uF
GND
VCC
IN
R4 6.8K
U5
74F245
U6
74F245
U7
74F245
C4 1uF
C7 1uF
C8 1uF
J1
CON64
CLK 1/2/3
CLK 4/5/6
CLK 7/8/9
RST 1/2/3
RST 4/5/6
RST 7/8/9
SYNCH. 1/2/3
SYNCH. 4/5/6
SYNCH. 7/8/9
DATA 09
DATA 08
DATA 07
DATA 06
DATA 05
DATA 04
DATA 03
DATA 02
DATA 01
+24Va
-24Va
GNDa
+12Vd
GNDd
+5Vd2
+5Vd1
C3 1uF
C6 1uF
U4
C1 1uF
C2 1uF
R3 1K
R1 1K
C1+
C1-
C2+
C2-
T1IN
T2IN
R1OUT
R2OUT
V+
V-
T1OUT
T2OUT
R1IN
R2IN
MAX 232
C11 1uF
C5 1uF
JP1
HEAD20
EM. PC
REC. PC
GND PC
U3 87C750
VCC
P3.5
P3.6
P3.7
P1.7
P1.6
P1.5
P1.4
P1.3
P1.2
P1.1
P1.0
P3.4
P3.3
P3.2
P3.1
P3.0
P0.2
P0.1
P0.0
RST
X2
X1
VSS
S1
D1
1N4148
C12
10uF
R2
10K
U1 BTF32
VCC
OUT
GND
C13
1uF
L4
1mH
U2 7805
IN
OUT
L5
1mH
L1 1mH
L2 1mH
C16
100uF
C17
1uF
C15
1uF
C14
1uF
OBSERVATOIRE DE LA COTE D'AZUR
2 130 Rte de l'Observatoire
06 460 Caussols
Title
CCDMSTER : CAMERA CCD Master Board
Size
Document Number
REV


+VRD
+VOD
+VRT'
+VOG
SUP1
SUP2
SUP3
SUP4
+VRG
-VRG
+VMO
-VMO
+VAO
-VAO
YERCA CCD CAMERA
CCD POWER SUPPLY



OBSERVATOIRE DE LA COTE D'AZUR	
2 130 Rte de l'Observatoire	
06 460 Caussols	
Title	CCDSEQ : CAMERA CCD sequencer board
Size A3	Document Number 1
REV	1.0

Appendix 2 : Data sheets of the main components of the controller

This section contains the data sheets of the components used in this controller. It does omit passive parts, as well as other usual parts as 78xx voltage regulators and the like.

- CCD442A
- 87C750
- MAX333A
- DG445
- OPA627
- DSP102
- TOTX195
- TORX194
- LM399
- OPA470

This information is only available of course in the printed form of this report. In case you ftp-ed this file, here are the U.S. addresses of the manufacturers of these parts :

- CCD442A

Loral Fairchild
Mr Jim Johnson 408 433 2550
1801 Mc Carthy Bd
Milpitas - CA95035 USA
Fax : 408 433 2508

- 87C750

Philips Semiconductors
811 East Arques Avenue
Sunnyvale - CA 94088-3409
1 800 234 7381
Fax : 1 708 296 8556

- MAX333A, DG445

Maxim Integrated products
120 San Gabriel Drive
Sunnyvale, CA94086
1 408 737 7600
1 800 998 8800 for litterature and samples in the U.S.A.

- OPA627, DSP102

Burr Brown
P.O. Box 11400
Tucson - AZ 85734-1400
Tel : 1 602 746 1111
1 800 548 6132
Fax : 602 741 3895

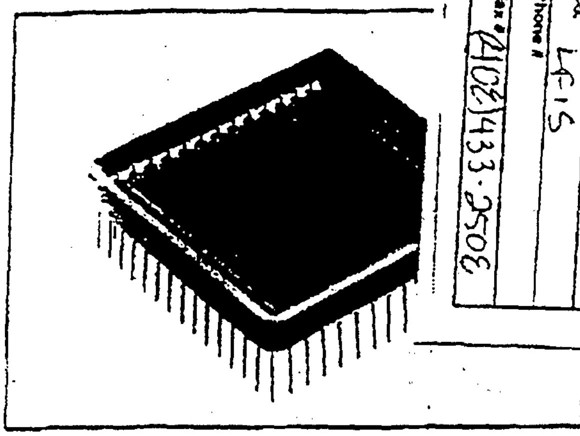
- TOTX195, TORX194:

Toshiba corporate headquarters
9775 Toledo way
Irvine CA 92718
Tel: 714 455 2000

- OPA470
Analog Devices
One Technology Way
P.O. Box 9106
Norwood - MA02062-9106
Tel : 1 617 329 4700
Fax : 1 617 326 8703

LORAL
Fairchild Imaging Sensors

CCD442A
2048 x 2048 Element Full Frame Image Sensor



FEATURES

- 2048 × 2048 Photosite Array
- 15μm × 15μm Pixel
- 30.72mm × 30.72mm Image Area
- Near 100% Fill Factor
- Multi-Pinned Phase (MPP) Option
- Readout Noise Less Than 7 Electrons at 250k pixels/sec
- Dynamic Range 10000:1
- Three Phase Buried Channel NMOS

GENERAL DESCRIPTION

The CCD442A is a 2048 × 2048 element solid state Charge Coupled Device (CCD) Full Frame area image sensor which is intended for use in high resolution scientific, industrial, and commercial electro-optical systems. The CCD442A is organized as a matrix array of 2048 horizontal by 2048 vertical CCD photosites. The pixel pitch and spacing is 15μm. For dark reference the top and bottom eight rows and the left and right eight columns are covered by a light shield. The available imaging area is thus 2032 rows by 2032 columns.

The imaging array may be operated in one of three modes, Buried Channel or Multi-Pinned Phase (MPP). The Buried Channel operation offers low noise performance and excellent charge transfer efficiencies. An additional implant under one vertical phase creates a virtual well which collects the photo-electrons with all Vertical clocks low during integration. This MPP mode decreases dark current down to 25 pA/cm² @ 25°C. Excellent low noise performance is achieved by use of the buried channel CCD structure and a dual stage low noise output amplifier with an output conversion of 3μV/e.

Device processing is done using 2.5 micron design rules. The single metal, triple-poly process allows a photosite layout with smaller pixel geometries and fewer array blemishes.

FUNCTIONAL DESCRIPTION

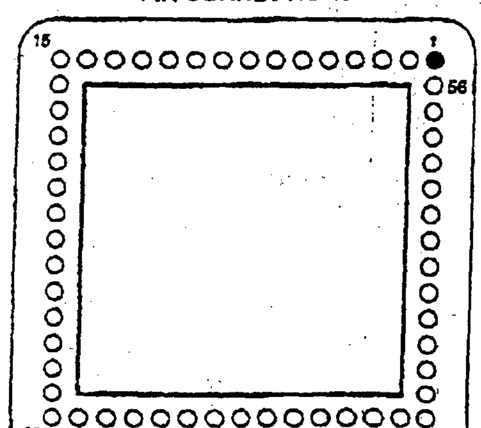
The CCD442A consists of the following functional elements illustrated in the block diagram.

Image Sensing Elements: Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photo-electrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

PIN NUMBER/NAME

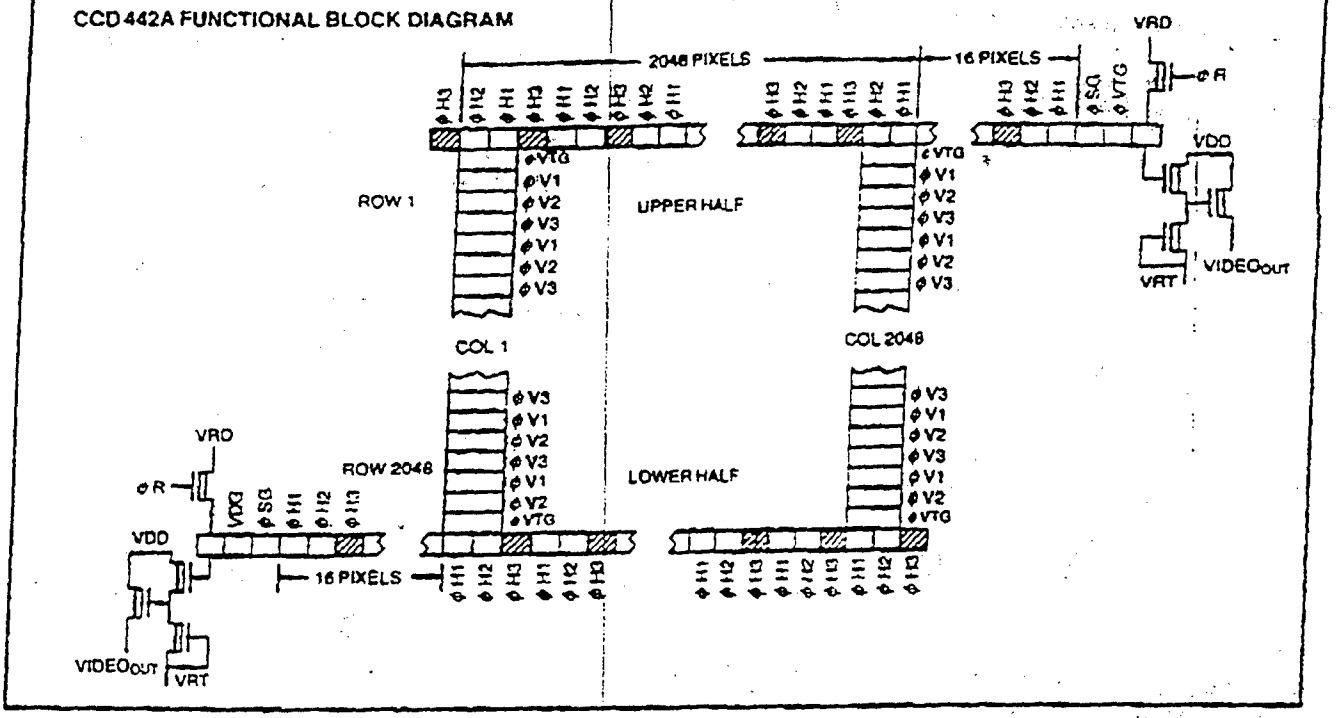
1	NC	20	$\phi V2_U$	39	$\phi H3_L$
2	NC	21	$\phi V1_U$	40	ϕVTG_L
3	V_{SS}	22	V_{SS}	41	V_{SS}
4	ϕR_U	23	ϕVTG_L	42	NC
5	VRD_U	24	ϕSG_L	43	NC
6	VRD_U VRT_U	25	VOG_L	44	NC
7	$VIDEO_{OUT}$	26	V_{SS}	45	V_{SS}
8	VDD_U	27	V_{SS}	46	V_{SS}
9	$\phi H1_U$	28	V_{SS}	47	$\phi V3_L$
10	$\phi H2_U$	29	NC	48	$\phi V1_L$
11	$\phi H3_U$	30	NC	49	$\phi V2_L$
12	ϕVTG_U	31	V_{SS}	50	V_{SS}
13	V_{SS}	32	ϕR_L	51	ϕVTG_U
14	NC	33	VRD_L	52	ϕSG_U
15	NC	34	VRT_L	53	VOG_U
16	NC	35	$VIDEO_{OUT}$	54	V_{SS}
17	V_{SS}	36	VDD_L	55	V_{SS}
18	V_{SS}	37	$\phi H1_L$	56	V_{SS}
19	$\phi V3_U$	38	$\phi H2_L$		

PIN CONNECTIONS



Loral Fairchild Imaging Sensors
1801 McCarthy Blvd., Milpitas, CA 95035
1 800 325-6975, TWX 910-373-2110, (408) 433-2500

CCD442A FUNCTIONAL BLOCK DIAGRAM



The photosite structure is made up of contiguous CCD elements with no voids or inactive areas. In addition to sensing light, these elements are used to shift image data vertically. Consequently, the device needs to be shuttered during readout.

Vertical Charge Shifting: The Full Frame architecture of the CCD442A provides video information as a single sequential readout of 2048 lines containing 2048 photosite elements. At the end of an integration period the ϕV_1, ϕV_2, and ϕV_3 clocks, are used to transfer charge vertically through the CCD array to the horizontal readout register. Vertical columns are separated by a channel stop region to prevent charge migration.

The imaging area is divided into an Upper and Lower half. Each 1024 x 2048 half may be clocked independently or together. Horizontal Transport registers along the top and bottom permit simultaneous readout of both halves. The CCD442A may be clocked such that the full array is readout the Upper or Lower Transport registers. The package pinouts are arranged so that the device may be rotated 180° without timing changes.

The Vertical Transfer Gate (ϕVTG) is the final array gate before charge is transferred to the serial horizontal shift registers. For simplified operation ϕVTG may be tied to ϕV_3.

Horizontal Charge Shifting: ϕH_1, ϕH_2, and ϕH_3 are polysilicon gates used to transfer charge horizontally to the output amplifier. The horizontal transport register is twice the size of the photosite to allow for vertical binning. The array can be operated normally at full resolution or some lower resolution with binning.

The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 16 additional register cells between the first pixel of each line and the output amplifier. The output from these locations contain no signal and may be used as a dark level reference.

The last clocked gate in the Horizontal registers is twice as large as the others and can be used to horizontally bin charge. This gate requires its own clock which should be tied to ϕH_1 for normal full resolution readout. The output video is available following the high to low transition of ϕSG.

The reset FET in the horizontal readout, clocked appropriately with ϕR, allows binning of adjacent pixels.

Output Amplifier: The CCD442A has one output amplifier at the end of the horizontal transport registers. They are dual FET floating diffusion amplifiers with a reset MOSFET tied to the input gate.

Charge packets are clocked to a precharged capacitor whose potential changes linearly in response to the number of electrons delivered. This potential is applied to the input gate of an NMOS amplifier producing a signal at the output V_{OUT} pin. The capacitor is reset with ϕR to a precharge level prior to the arrival of the next charge packet except when horizontally binning. It is reset by use of the reset MOSFET.

The output amplifier drain is tied to VDD. The source (Video Out) is connected to an external load resistor to ground. The source constitutes the video output from the device.

Multi-Pinned Phase: MPP is a CCD technology which significantly reduces the dark current generation rate. CCDsc are endowed with this capability by the addition of an implant during the semiconductor manufacturing process.

This implant creates a virtual well in the array which allows charge integration while maintaining pixel integrity with the Vertical clocks in the low state. Leaving the Vertical clocks in the low state during the integration cycle is the method used to implement MPP mode.

A drawback to utilizing the MPP mode is reduced full well capacity. The virtual well created by the MPP implant does not hold as much charge as the normal buried channel operating mode which leaves one Vertical clock in the high state during integration. The CCD442A may be operated in the conventional buried channel mode with increase in charge capacity over the MPP mode.

DEFINITION OF TERMS

Charge-Coupled Device—A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Vertical Transport Clocks ϕV_1, ϕV_2, ϕV_3—The clock signals applied to the vertical transport register.

Horizontal Transport Clocks ϕH_1, ϕH_2, ϕH_3—The clock signals applied to the horizontal transport registers.

Reset Clock ϕR—The clock applied to the reset switch of the output amplifier.

Dynamic Range—The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4–6 times the RMS noise output.

Saturation Exposure—The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Responsivity—The output signal voltage per unit of exposure.

Spectral Response Range—The spectral band over which the response per unit of radiant power is more than 10% of the peak response.

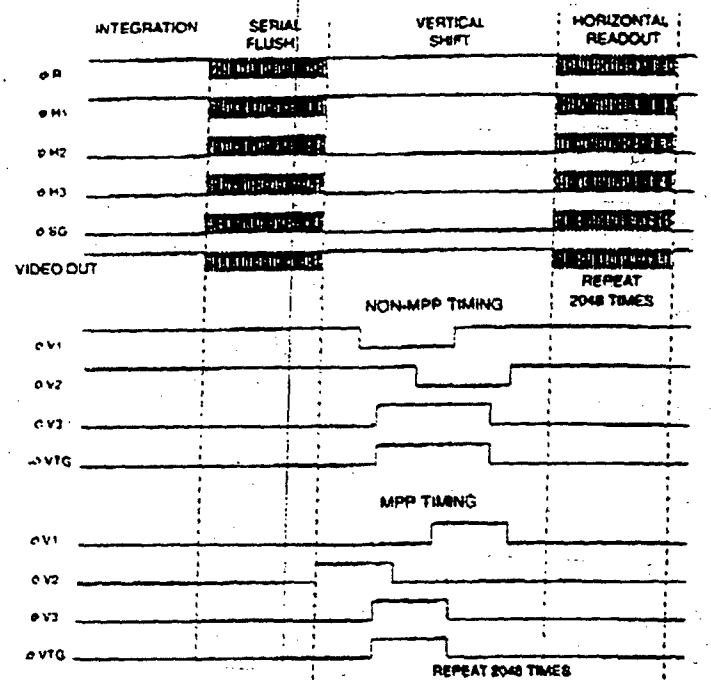
Photo-Response Non-Uniformity—The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

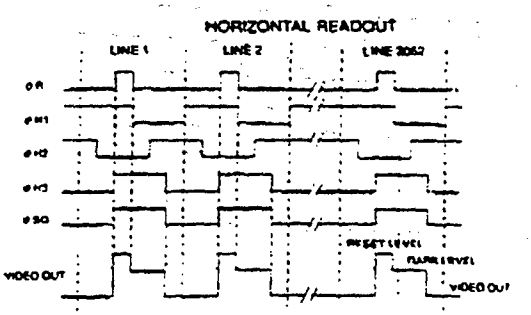
Dark Signal—The output signal in the dark caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

Vertical Transfer Gate ϕVTG—Gate structures adjacent to the end row of photosites and the horizontal transport registers. The charge packets accumulated in the photosites are shifted vertically through the array. Upon reaching the end row of photosites, the charge is transferred in parallel via the transfer gates to the horizontal transport shift registers whenever the transfer gate voltage goes high.

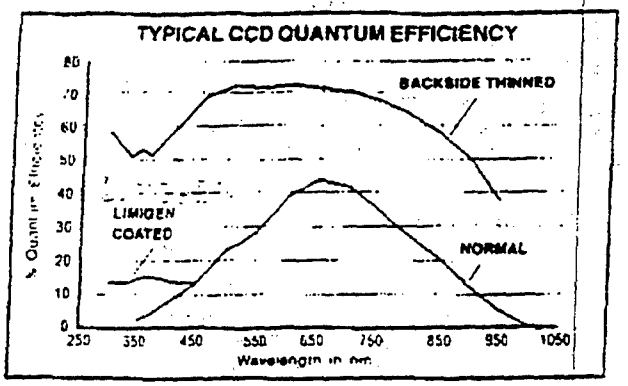
Pixel—Picture element or sensor element also called photoelement or photosite.

TIMING DIAGRAM





CCD442A



QUANTUM EFFICIENCY ENHANCEMENTS

On a custom basis, our large area CCDs can be backside thinned for increased QE. The CCD is bump mated to a fanout and thinned to approximately 15 microns. The incident illumination enters through the backside of the array. Since no photons are absorbed in the polysilicon gate structures, the QE increases. We can also coat frontside illuminated devices with a fluorescent dye that absorbs UV light and fluoresces in the visible range. This provides CCD response at wavelengths less than 400nm.

TYPICAL DC VOLTAGES

SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
V_{DD}	DC Supply Voltage		20.0	25	V	
V_{RD}	Reset Drain Voltage	12	13.0	16	V	
V_{OG}	Output Gate Voltage		1.0		V	
V_{SS}	Substrate Ground		0.0		V	

TYPICAL CLOCK VOLTAGES

SYMBOL	PARAMETER	HIGH	LOW	UNIT	REMARKS
$V\Phi H_{(1,2,3)}$	Horizontal Multiplexer Clock	+5	-5.0	V	
$V\Phi V_{(1,2,3)}$	Vertical Array Clocks	+3.0	-8.0	V	
$V\Phi R$	Reset Gate Clock	+8.0	0.0	V	
$V\Phi VTG$	Array Transfer Gate Clock	+3.0	-8.0	V	

Note ΦH=400pF ΦV=60,000pF

PERFORMANCE SPECIFICATIONS

SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
V_{SAT}	Saturation Output Voltage	300		1200	mV	Note 1
	Full Well Capacity	100,000		400,000	e-	
	Output Amp Sensitivity		3.0		μV/e-	
PRNU	Photo-Response Non-Uniformity Peak-to-Peak			10	$\%V_{SAT}$	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak			1.0	mV	
DC	Dark Current	0.025		2.0	nA/cm²	Note 2
R	Responsivity		1.0		V/μJ/cm²	
V_{ODC}	Output DC Level		14.0		V	Note 3
Z	Suggested Load Register	1.0	5.0	20	kΩ	Note 3

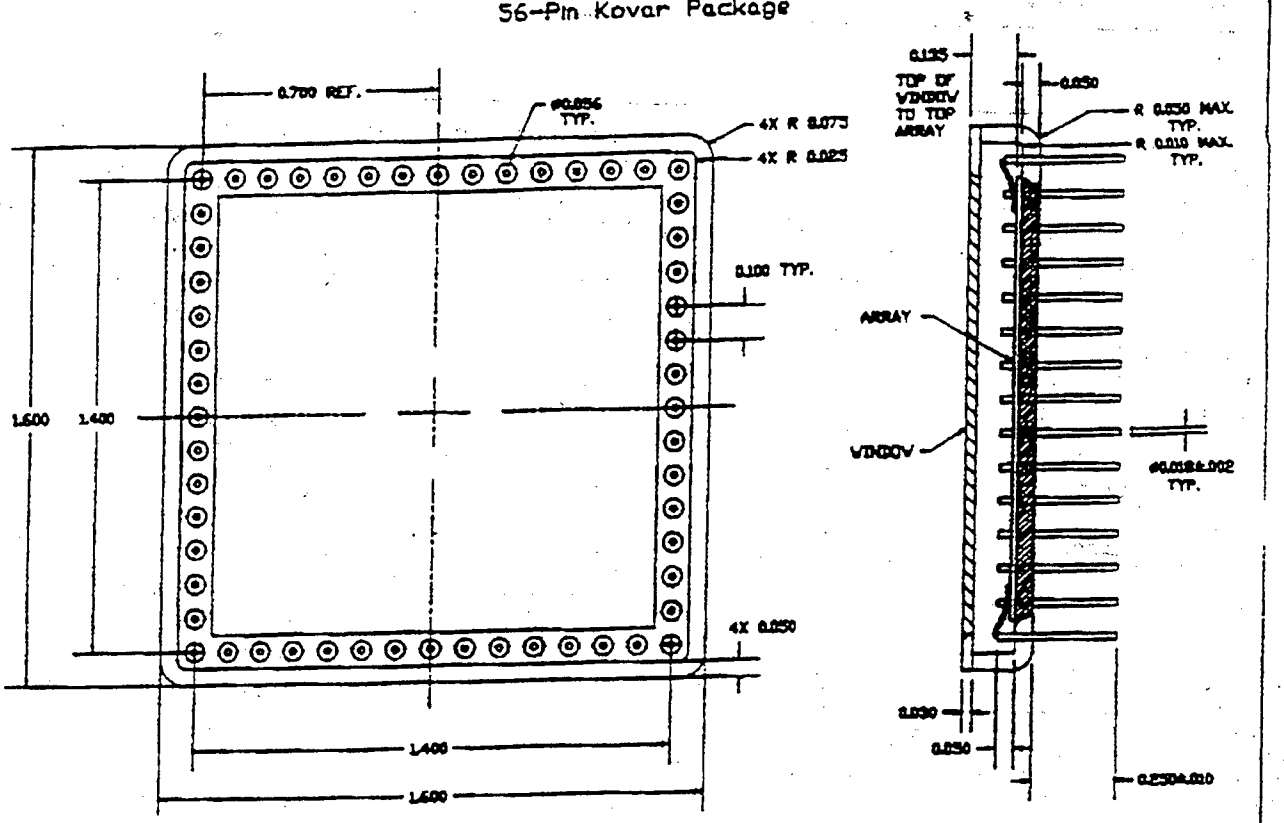
Note 1 Maximum well capacity is achieved operating in Buried Channel Mode minimum capacity is in MPP mode

Note 2 Values shown are for 25 C Dark current doubles for every 4 - 6 C

Note 3 Standard test conditions are nominal MPP clocks and DC operating voltages 1MHz Horizontal Data Rate 6uSec Vertical Shift Cycle

CCD442 PACKAGE OUTLINE

56-Pin Kovar Package



COSMETIC GRADING

Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels and for different device temperatures.

The CCD442A is available in various standard grades, as well as custom selected grades. Consult the factory for available grading information and custom selections.

WARRANTY

Within twelve months of delivery to the end customer, Loral Fairchild will repair or replace, at our option, any Loral Fairchild camera product if any part is found to be defective in materials or workmanship. Contact factory for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Loral Fairchild Division certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specification under which it is furnished.

LORAL
Fairchild Imaging Sensors

ANALOG DEVICES

Very Low-Noise Quad Operational Amplifier

OP-470

2

ATURES

- Very Low Noise ..... 5nV/$\sqrt{Hz}$ @ 1kHz Max
- Excellent Input Offset Voltage ..... 0.4mV Max
- Low Offset Voltage Drift ..... 2μV/°C Max
- Very High Gain ..... 1000V/mV Min
- Outstanding CMR ..... 110dB Min
- Slew Rate ..... 2V/μs Typ
- Gain-Bandwidth Product ..... 6MHz Typ
- Industry Standard Quad Pinouts
- Available in Die Form

RDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE CERDIP 14-PIN	PLASTIC	LCC*	OPERATING TEMPERATURE RANGE
400	–	–	OP470ARC/883	MIL
400	OP470AY*	–	OP470ATC/883	MIL
400	OP470EY	–	–	IND
800	OP470FY	–	–	IND
1000	–	OP470GP	–	XIND
1000	–	OP470GS**	–	XIND

For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

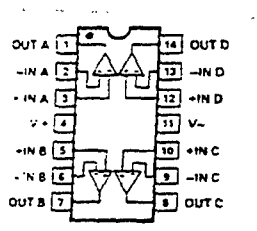
For availability and burn-in information on SO and PLCC packages, contact your local sales office.

ENERAL DESCRIPTION

e OP-470 is a high-performance monolithic quad operational amplifier with exceptionally low voltage noise, V/$\sqrt{Hz}$ at 1kHz Max, offering comparable performance to l's industry standard OP-27.

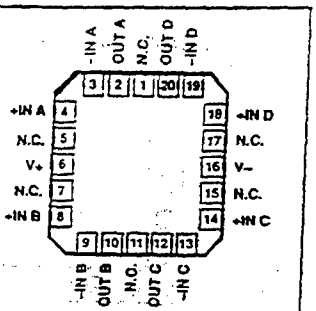
e OP-470 features an input offset voltage below 0.4mV, cellent for a quad op amp, and an offset drift under 2μV/°C, aranteed over the full military temperature range. Open-p gain of the OP-470 is over 1,000,000 into a 10kΩ load insuring excellent gain accuracy and linearity, even in high-gain applications. Input bias current is under 25nA which reduces errors due to signal source resistance. The OP-470's CMR of over 110dB and PSRR of less than 1.8μV/V significantly reduce errors due to ground noise and power supply fluctuations. Power consumption of the quad OP-470 is half that of four OP-27s, a significant advantage for power con-

PIN CONNECTIONS

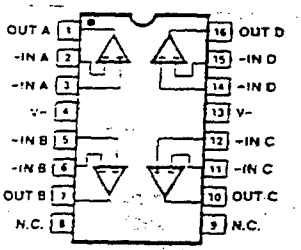


14-PIN HERMETIC DIP
(Y-Suffix)

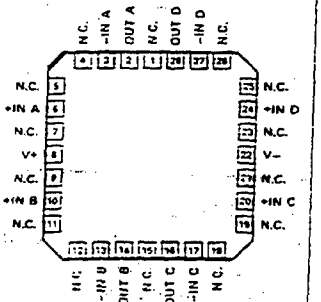
14-PIN PLASTIC MINI-DIP
(P-Suffix)



20-LEAD LCC
(RC-Suffix)

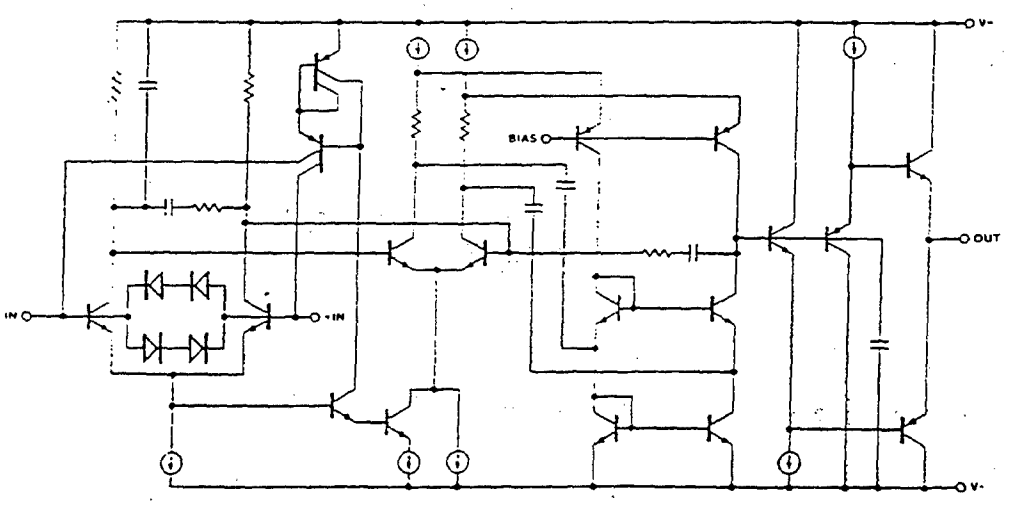


16-PIN SOL
(S-Suffix)



28-LEAD LCC
(TC-Suffix)

MPLIFIED SCHEMATIC



OP-470

scious applications. The OP-470 is unity-gain stable with a gain-bandwidth product of 6MHz and a slew rate of 2V/μs.

The OP-470 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, quad buffers, and low-noise active filters.

The OP-470 conforms to the industry standard 14-pin DIP pinout. It is pin compatible with the OP-11, LM148/149, HA4741, HA5104, and RM4156 quad op amps and can be used to upgrade systems using these devices.

For higher speed applications the OP-471, with a slew rate of 3V/μs, is recommended.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 2) ..... ±1.0V
Differential Input Current (Note 2) ..... ±25mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, TC, Y-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... –65°C to +150°C
Operating Temperature Range
OP-470A ..... –55°C to +125°C
OP-470E, OP-470F ..... –25°C to +85°C
OP-470G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note-3)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	30	°C/W
28-Contact LCC (TC)	70	28	°C/W
16-Pin SOL (S)	88	23	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. The OP-470's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.
3. Θ_A is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO and PLCC packages.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

			OP-470A/E			OP-470F			OP-470G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.1	0.4	—	0.2	0.8	—	0.4	1.0	mV
Input Offset Current	I_{OS}	V_{CM} = 0V	—	3	10	—	6	20	—	12	30	nA
Input Bias Current	I_B	V_{CM} = 0V	—	6	25	—	15	50	—	25	60	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	80	200	—	80	200	—	80	200	nV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1kHz (Note 2)	— — —	3.8 3.3 3.2	6.5 5.5 5.0	— — —	3.8 3.3 3.2	6.5 5.5 5.0	— — —	3.8 3.3 3.2	6.5 5.5 5.0	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1kHz	— — —	1.7 0.7 0.4	— — —	— — —	1.7 0.7 0.4	— — —	— — —	1.7 0.7 0.4	— — —	$pA/\sqrt{Hz}$
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 10kΩ R_L = 2kΩ	1000 500	2300 1200	— —	800 400	1700 900	— —	800 400	1700 900	— —	V/mV
Input Voltage Range	IVR	(Note 3)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	110	125	—	100	120	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	—	0.56	1.8	—	1.0	5.6	—	1.0	5.6	μV/V
Slew Rate	SR		1.4	2	—	1.4	2	—	1.4	2	—	V/μs

ECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

AMETER	SYMBOL	CONDITIONS	OP-470A/E MIN	OP-470A/E TYP	OP-470A/E MAX	OP-470F MIN	OP-470F TYP	OP-470F MAX	OP-470G MIN	OP-470G TYP	OP-470G MAX	UNITS
pply Current Amplifiers)	I_{SY}	No Load	—	9	11	—	9	11	—	9	11	mA
ı Bandwidth Product	GBW	$A_V = -10$	—	6	—	—	6	—	—	6	—	MHz
nnel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 1)	125	155	—	125	155	—	125	155	—	dB
ut Capacitance	C_{IN}		—	2	—	—	2	—	—	2	—	pF
ut Resistance ferential-Mode	R_{IN}		—	0.4	—	—	0.4	—	—	0.4	—	MΩ
t Resistance mmon-Mode	R_{INCM}		—	11	—	—	11	—	—	11	—	GΩ
ing Time	t_s	$A_V = -1$ to 0.1%	—	5.5	—	—	5.5	—	—	5.5	—	μs
		to 0.01%	—	6.0	—	—	6.0	—	—	6.0	—	

TES:
uaranteed but not 100% tested.
ample tested.
Guaranteed by CMR test.

ECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-55°C \le T_A \le 125°C$ for OP-470A, unless otherwise noted.

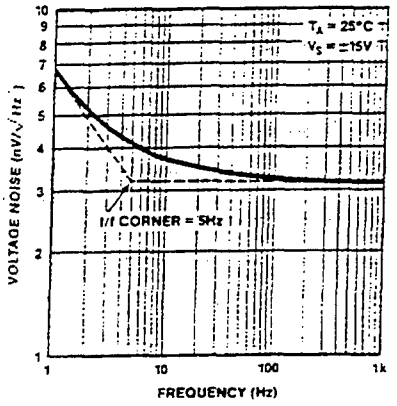
IAMETER	SYMBOL	CONDITIONS	OP-470A MIN	OP-470A TYP	OP-470A MAX	UNITS
ut Offset Voltage	V_{OS}		—	0.14	0.6	mV
rage Input set Voltage Drift	TCV_{OS}		—	0.4	2	μV/°C
ut Offset Current	I_{OS}	$V_{CM} = 0V$	—	5	20	nA
ut Bias Current	I_B	$V_{CM} = 0V$	—	15	50	nA
ge-Signal oltage Gain	A_{VO}	$V_O = \pm10V$ $R_L = 10k\Omega$	750	1600	—	V/mV
		$R_L = 2k\Omega$	400	800	—	
ut Voltage Range	IVR	(Note 1)	±11	±12	—	V
.ut Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	—	V
mmon-Mode ection	CMR	$V_{CM} = \pm11V$	100	120	—	dB
er Supply ection Ratio	PSRR	$V_S = \pm4.5V$ to $\pm18V$	—	1.0	5.6	μV/V
ply Current Amplifiers)	I_{SY}	No Load	—	9.2	11	mA

OTE:
Guaranteed by CMR test.

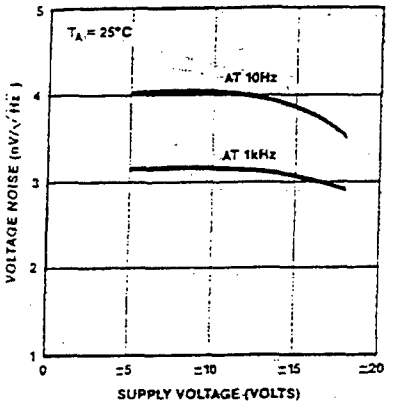
OP-470

TYPICAL PERFORMANCE CHARACTERISTICS

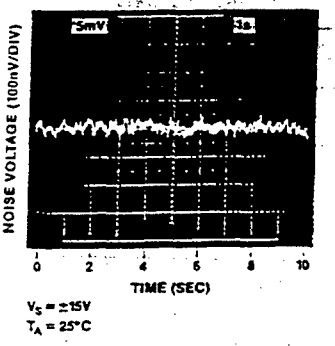
VOLTAGE NOISE DENSITY vs FREQUENCY



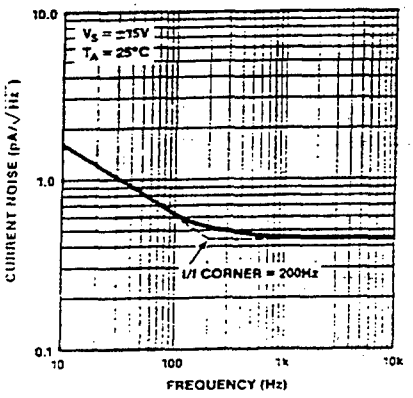
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



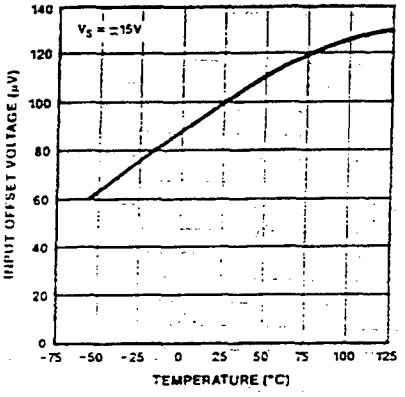
0.1Hz TO 10Hz NOISE



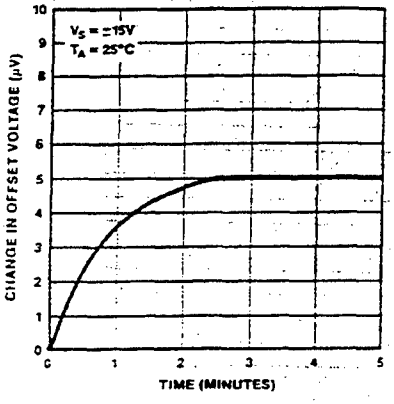
CURRENT NOISE DENSITY vs FREQUENCY



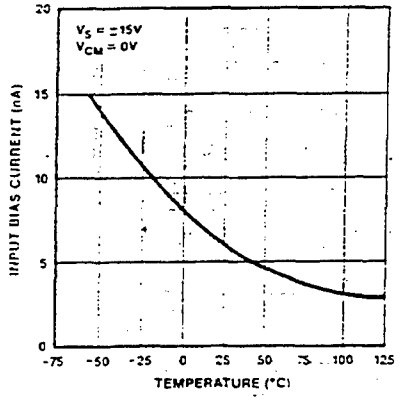
INPUT OFFSET VOLTAGE vs TEMPERATURE



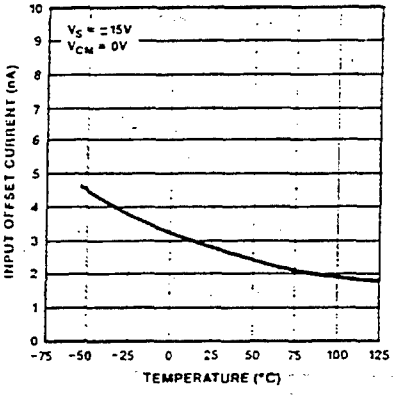
WARM-UP OFFSET VOLTAGE DRIFT



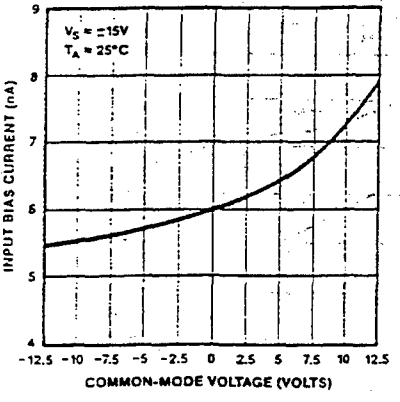
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

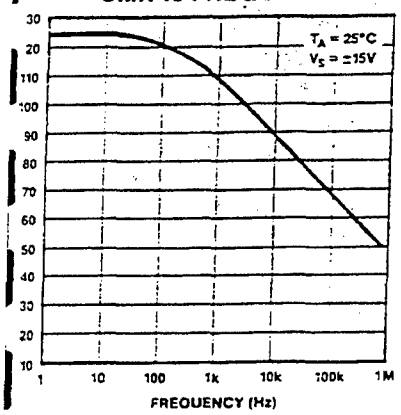


INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

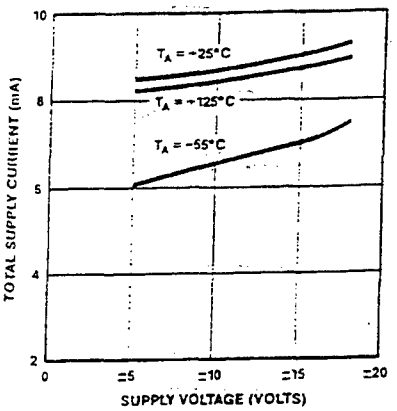


TYPICAL PERFORMANCE CHARACTERISTICS

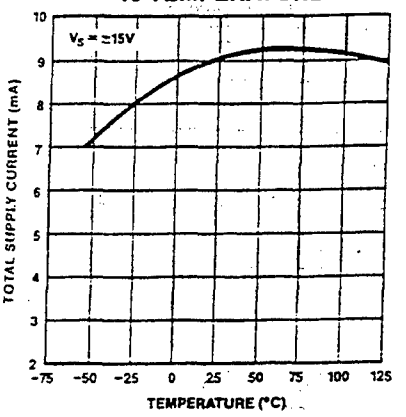
CMR vs FREQUENCY



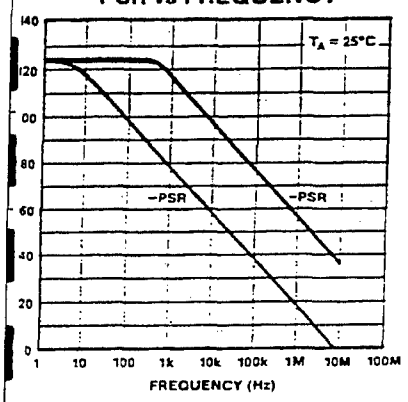
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



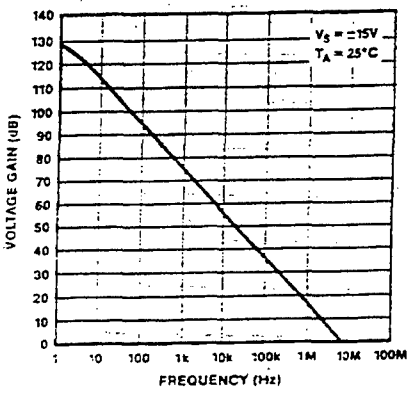
TOTAL SUPPLY CURRENT vs TEMPERATURE



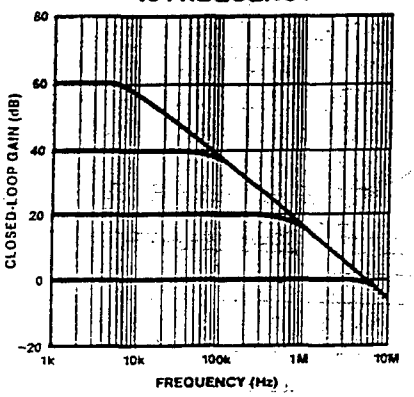
PSR vs FREQUENCY



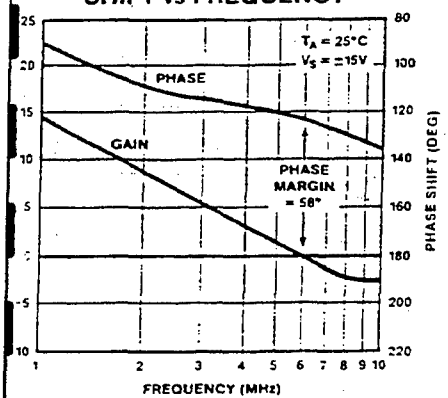
OPEN-LOOP GAIN vs FREQUENCY



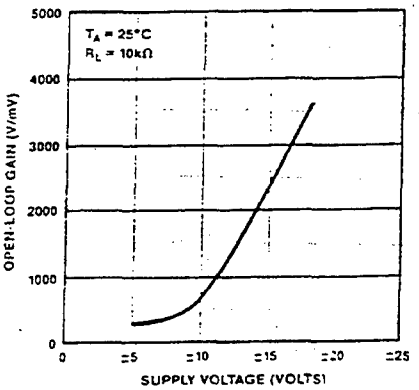
CLOSED-LOOP GAIN vs FREQUENCY



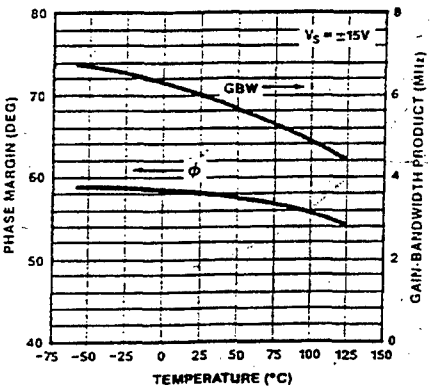
OPEN-LOOP GAIN, PHASE SHIFT vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE



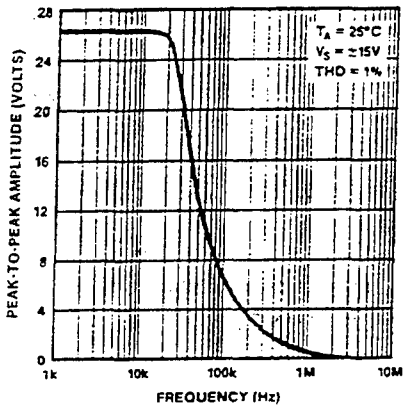
GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



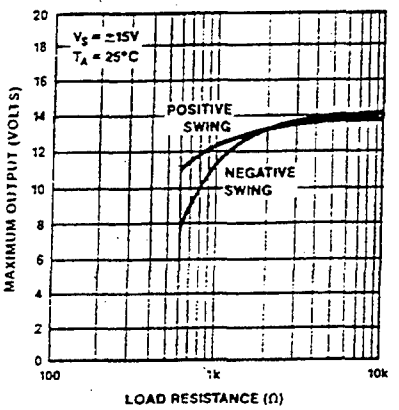
OP-470

TYPICAL PERFORMANCE CHARACTERISTICS

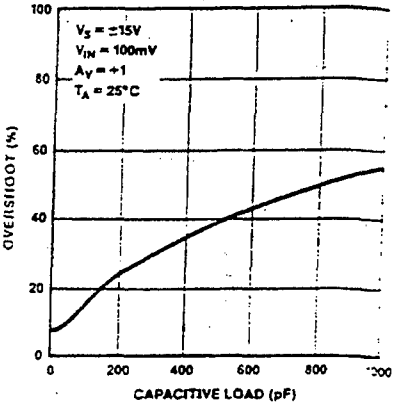
MAXIMUM OUTPUT SWING vs FREQUENCY



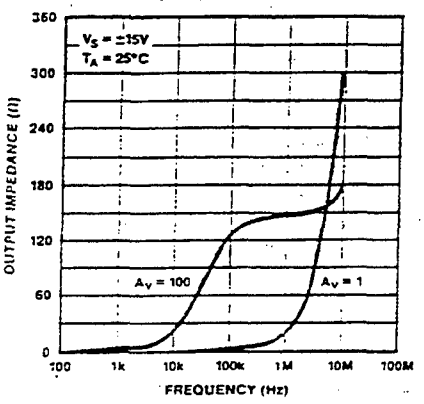
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



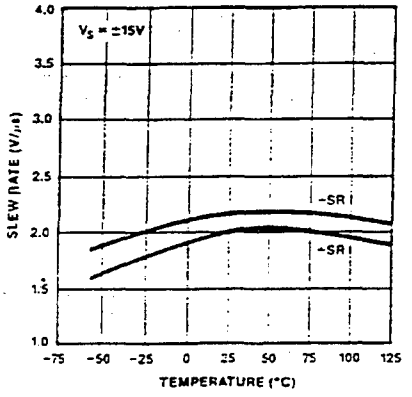
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



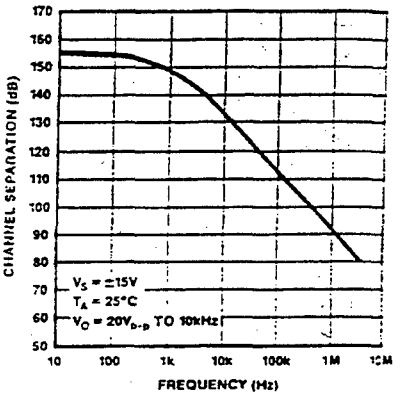
OUTPUT IMPEDANCE vs FREQUENCY



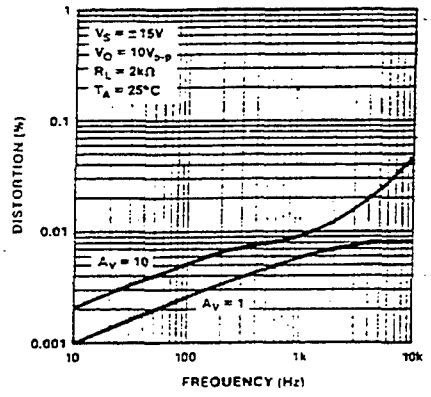
SLEW RATE vs TEMPERATURE



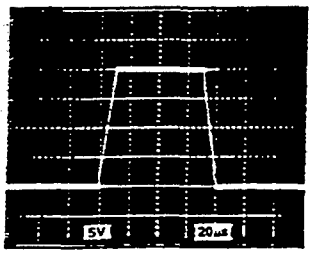
CHANNEL SEPARATION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

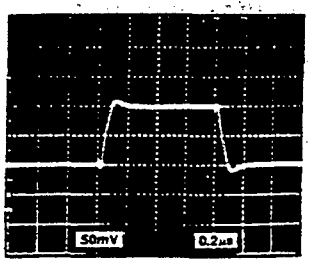


LARGE-SIGNAL TRANSIENT RESPONSE



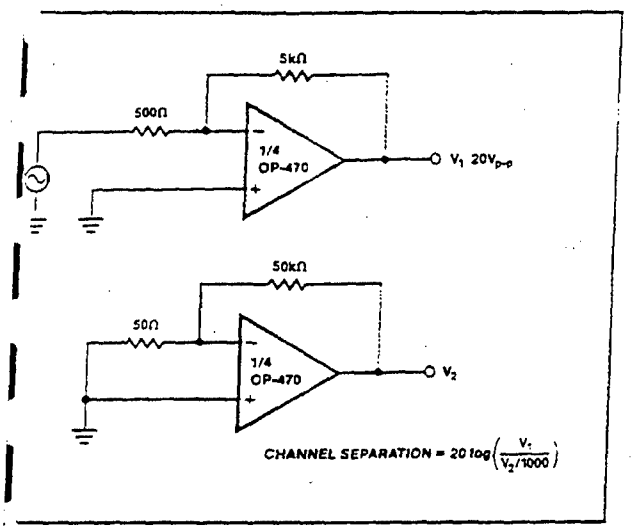
T_A = 25°C
V_S = ±15V
A_V = +1

SMALL-SIGNAL TRANSIENT RESPONSE

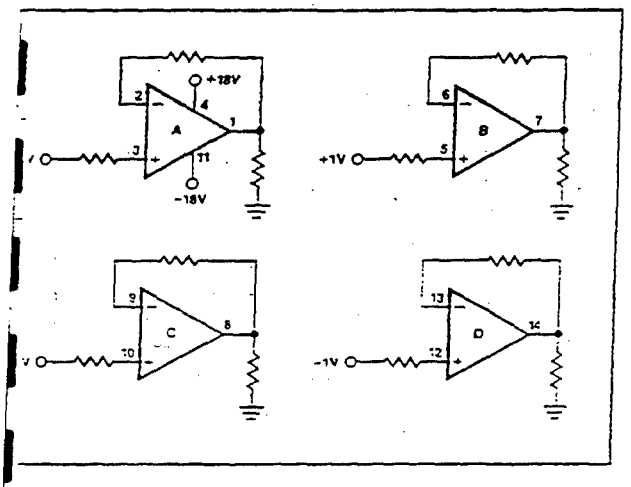


T_A = 25°C
V_S = ±15V
A_V = +1

NNEL SEPARATION TEST CIRCUIT



N-IN CIRCUIT



ICATIONS INFORMATION

TAGE AND CURRENT NOISE

OP-470 is a very low-noise quad op amp, exhibiting a al voltage noise of only 3.2nV/√Hz @ 1kHz. The ptionally low noise characteristics of the OP-470 is in achieved by operating the input transistors at high col- r currents since the voltage noise is inversely propor- l to the square root of the collector current. Current e, however, is directly proportional to the square root of collector current. As a result, the outstanding voltage performance of the OP-470 is gained at the expense of nt noise performance, which is typical for low noise ifiers.

btain the best noise performance in a circuit it is vital to rstand the relationship between voltage noise (e_n), cur- noise (i_n), and resistor noise (e_t).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calulated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_t)^2}$$

where:

E_n = total input referred noise

e_n = op amp voltage noise

i_n = op amp current noise

e_t = source resistance thermal noise

R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 1 shows the relationship between total noise at 1kHz and source resistance. For $R_S < 1k\Omega$ the total noise is dominated by the voltage noise of the OP-470. As R_S rises above

FIGURE 1: Total Noise vs Source Resistance (Including Resistor Noise) at 1kHz

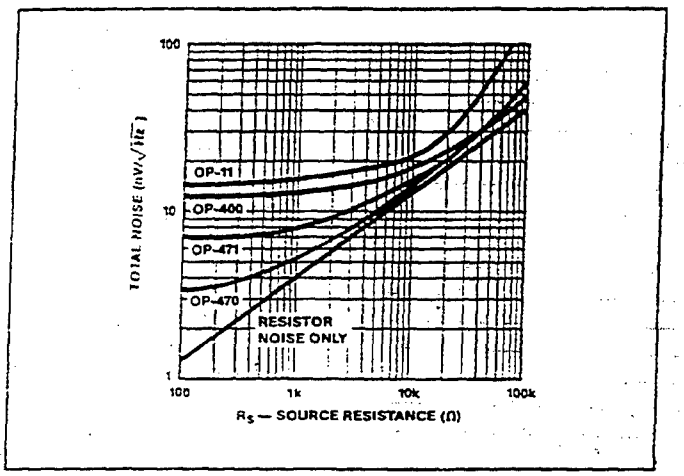
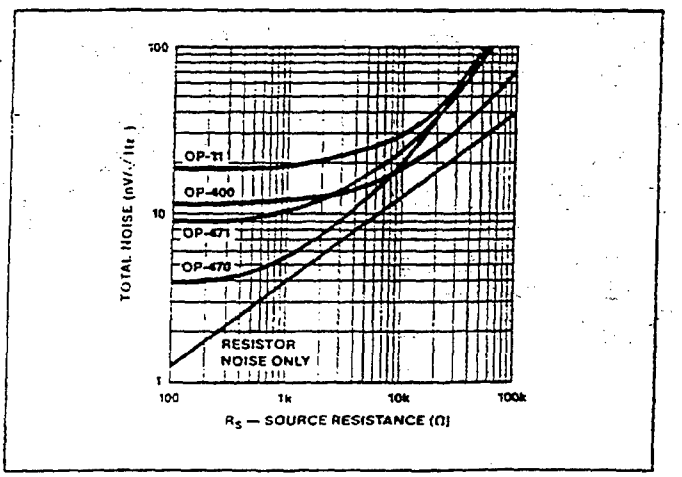


FIGURE 2: Total Noise vs Source Resistance (Including Resistor Noise) at 10Hz



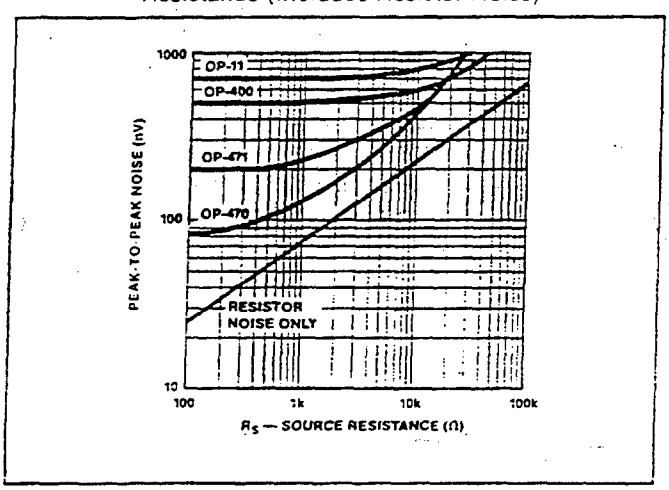
1kΩ, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the OP-470. When R_S exceeds 20kΩ, current noise of the OP-470 becomes the major contributor to total noise.

Figure 2 also shows the relationship between total noise and source resistance, but at 10Hz. Total noise increases more quickly than shown in Figure 1 because current noise is inversely proportional to the square root of frequency. In Figure 2, current noise of the OP-470 dominates the total noise when $R_S > 5k\Omega$.

From Figures 1 and 2 it can be seen that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP-400, with lower current noise than the OP-470, will provide lower total noise.

Figure 3 shows peak-to-peak noise versus source resistance over the 0.1Hz to 10Hz range. Once again, at low values of R_S, the voltage noise of the OP-470 is the major contributor to peak-to-peak noise with current noise the major contributor as R_S increases. The crossover point between the OP-470 and the OP-400 for peak-to-peak noise is at $R_S = 17k\Omega$.

FIGURE 3: Peak-To-Peak Noise (0.1Hz To 10Hz) vs Source Resistance (Includes Resistor Noise)



The OP-471 is a higher speed version of the OP-470, with a slew rate of 8V/μs. Noise of the OP-471 is only slightly higher than the OP-470. Like the OP-470, the OP-471 is unity-gain stable.

For reference, typical source resistances of some signal sources are listed in Table I.

TABLE I

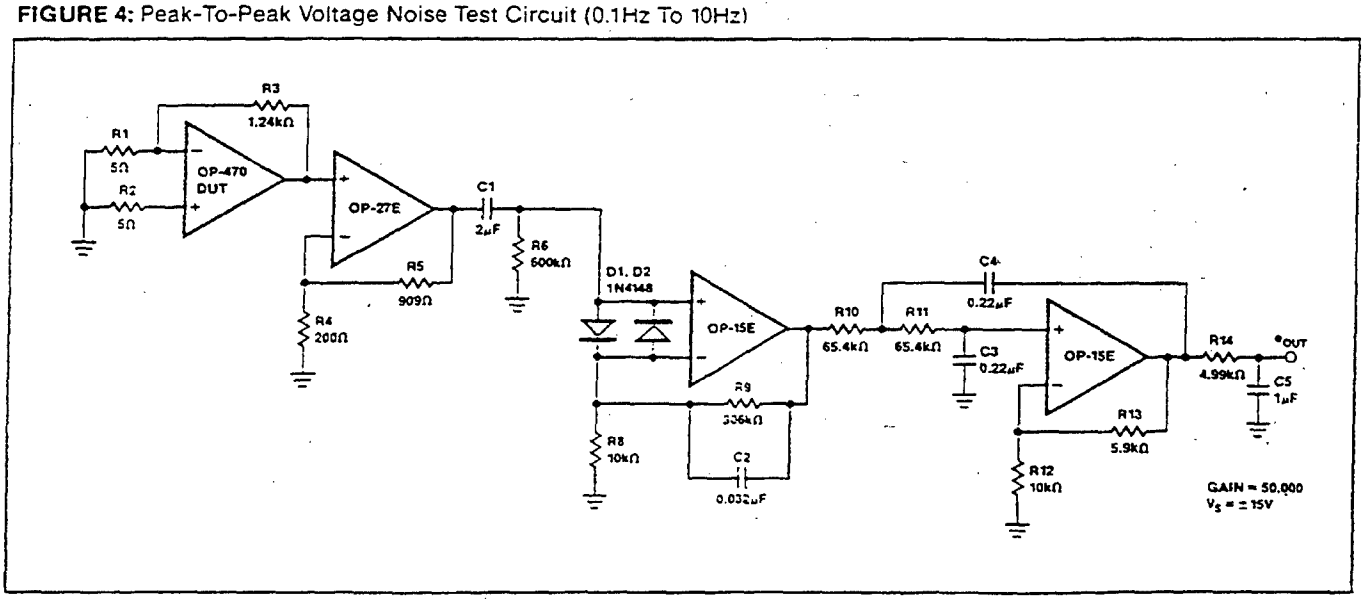
DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-470 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-470 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications," Application Note AN-15.

NOISE MEASUREMENTS — PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 4 is a test setup for measuring peak-to-peak voltage noise. To measure the 200nV peak-to-peak

FIGURE 4: Peak-To-Peak Voltage Noise Test Circuit (0.1Hz To 10Hz)



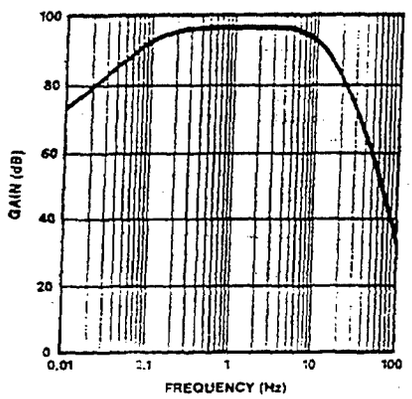
se specification of the OP-470 in the 0.1Hz to 10Hz range, ollowing precautions must be observed:

ne device has to be warmed-up for at least five minutes. s shown in the warm-up drift curve, the offset voltage pically changes 5μV due to increasing chip temperature ter power-up. In the 10-second measurement interval, hese temperature-induced effects can exceed tens-of-nanovolts.

or similar reasons, the device has to be well-shielded om air currents. Shielding also minimizes thermocouple ffects.

udden motion in the vicinity of the device can also "feed-rough" to increase the observed noise.

URE 5: 0.1Hz To 10Hz Peak-To-Peak Voltage Noise Test Circuit Frequency Response



4. The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 5, the 0.1Hz corner is defined by only one pole. The test time of 10 seconds acts as an additional pole to eliminate noise contribution from the frequency band below 0.1Hz.
5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.
6. Power should be supplied to the test circuit by well bypassed low-noise supplies, e.g. batteries. These will minimize output noise introduced via the amplifier supply pins.

NOISE MEASUREMENT — NOISE VOLTAGE DENSITY

The circuit of Figure 6 shows a quick and reliable method of measuring the noise voltage density of quad op amps. Each individual amplifier is series-connected and is in unity-gain, save the final amplifier which is in a noninverting gain of 101. Since the ac noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101\left(\sqrt{e_{nA}^2 + e_{nB}^2 + e_{nC}^2 + e_{nD}^2}\right)$$

The OP-470 is a monolithic device with four identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

$$e_{OUT} = 101\left(\sqrt{4e_n^2}\right) = 101\ (2e_n)$$

URE 6: Noise Voltage Density Test Circuit

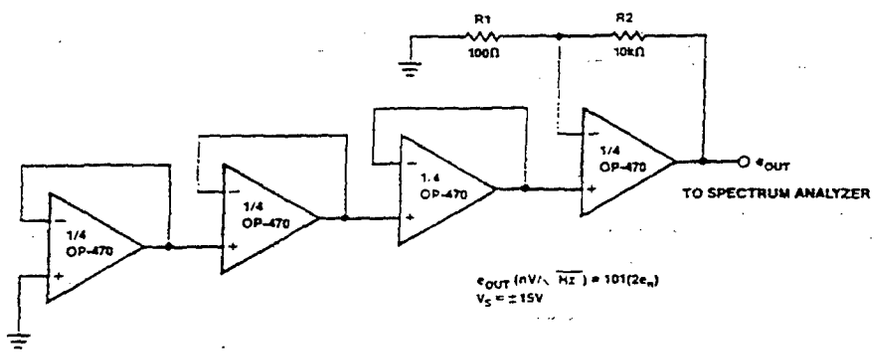
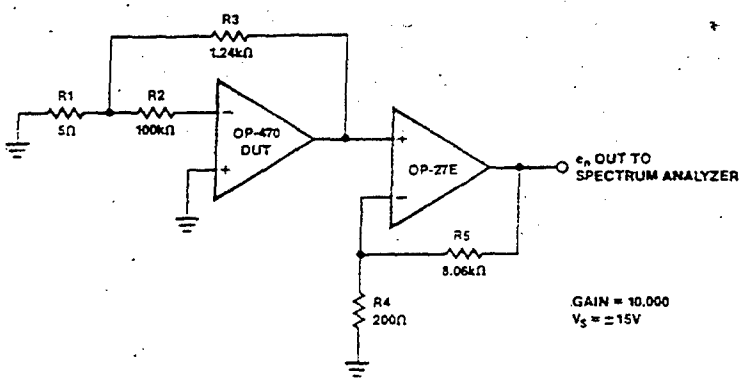


FIGURE 7: Current Noise Density Test Circuit



NOISE MEASUREMENT — CURRENT NOISE DENSITY

The test circuit shown in Figure 7 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G = gain of 10000
R_S = 100kΩ source resistance

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-470 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-470.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 8. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for a load capacitance of up to 1000pF when used with the OP-470.

In applications where the OP-470's inverting or noninverting inputs are driven by a low source impedance (under 100Ω) or connected to ground, if V+ is applied before V−, or when V− is disconnected, excessive parasitic currents will flow. Most

FIGURE 8: Driving Large Capacitive Loads

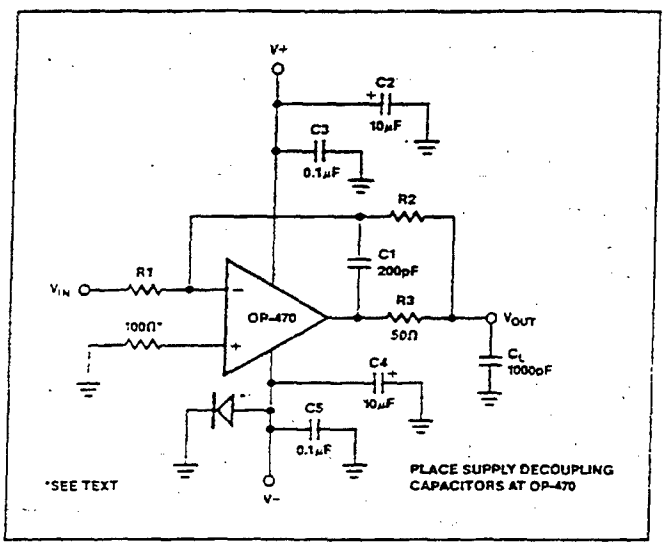
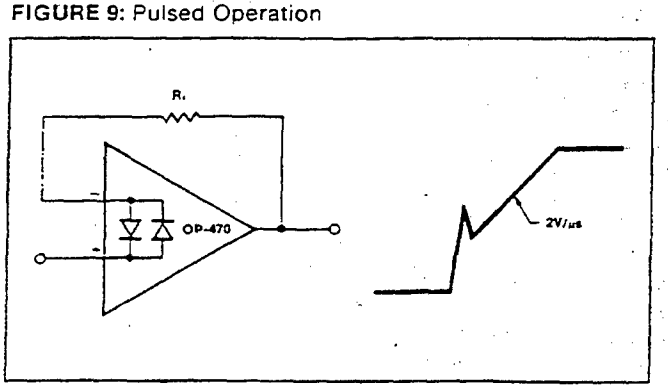


FIGURE 9: Pulsed Operation



plications use dual tracking supplies and with the device ply pins properly bypassed, power-up will not present a blem. A source resistance of at least 100Ω in series with all puts (Figure 8) will limit the parasitic currents to a safe level '- is disconnected. It should be noted that any source stance, even 100Ω, adds noise to the circuit. Where noise equired to be kept at a minimum, a germanium or Schottky de can be used to clamp the V– pin and eliminate the sitic current flow instead of using series limiting resistors. most applications, only one diode clamp is required per rd or system.

TY-GAIN BUFFER APPLICATIONS

en $R_f \leq 100\Omega$ and the input is driven with a fast, large- al pulse (>1V), the output waveform will look as shown in re 9.

ring the fast feedthrough-like portion of the output, the t protection diodes effectively short the output to the t, and a current, limited only by the output short-circuit ection, will be drawn by the signal generator. With $R_f \geq$ 0Ω, the output is capable of handling the current require- ts ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active le and a smooth transition will occur.

en $R_f > 3k\Omega$, a pole created by R_f and the amplifier's input acitance (2pF) creates additional phase shift and reduces se margin. A small capacitor (20 to 50pF) in parallel with elps eliminate this problem.

PLICATIONS

W NOISE AMPLIFIER

mple method of reducing amplifier noise by paralleling lifiers is shown in Figure 10. Amplifier noise, depicted in ure 11, is around 2nV/$\sqrt{Hz}$ @ 1kHz (R.T.I.). Gain for each alleled amplifier and the entire circuit is 1000. The 200Ω stors limit circulating currents and provide an effective put resistance of 50Ω. The amplifier is stable with a 10nF pacitive load and can supply up to 30mA of output drive.

ITAL PANNING CONTROL

ure 12 uses a DAC-8408, a quad 8-bit DAC, to pan a signal tween two channels. The complementary DAC current puts of two of the DAC-8408's four DACs drive current-to- age converters built from a single quad OP-470. The plifiers have complementary outputs with the amplitudes endent upon the digital code applied to the DAC. Figure hows the complementary outputs for a 1kHz input signal digital ramp applied to the DAC data inputs. Distortion of digital panning control is less than 0.01%.

n error due to the mismatching between the internal DAC der resistors and the current-to-voltage feedback resis- tors is eliminated by using feedback resistors internal to the DAC. Of the four DACs available in the DAC-8408, only two, DACs A and C, actually pass a signal. DACs B and D are used to provide the additional feedback resistors needed in the circuit. If the $V_{REF}B$ and $V_{REF}D$ inputs remain unconnected the currrent-to-voltage converters using $R_{FB}B$ and $R_{FB}D$ are unaffected by digital data reaching DACs B and D.

FIGURE 10: Low Noise Amplifier

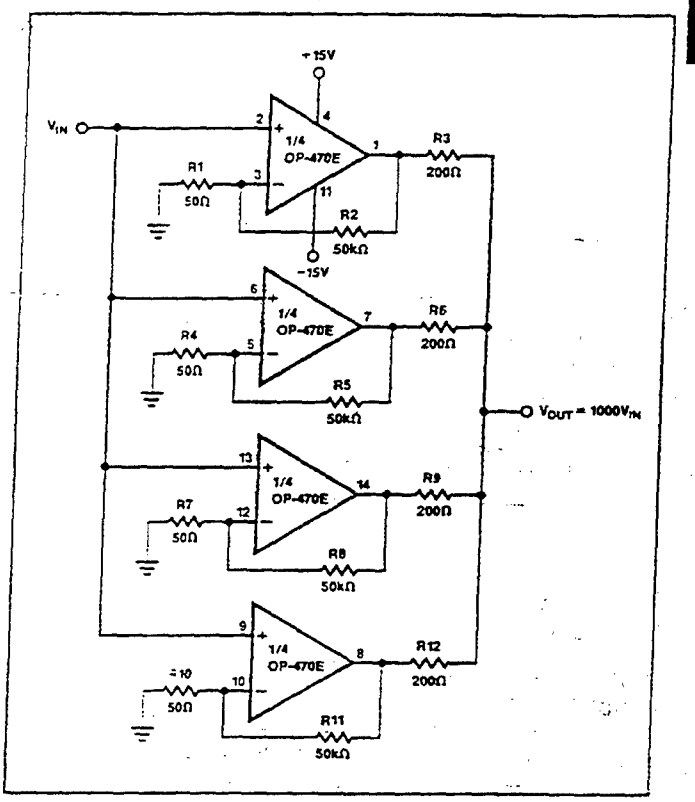


FIGURE 11: Noise Density of Low Noise Amplifier, G = 1000

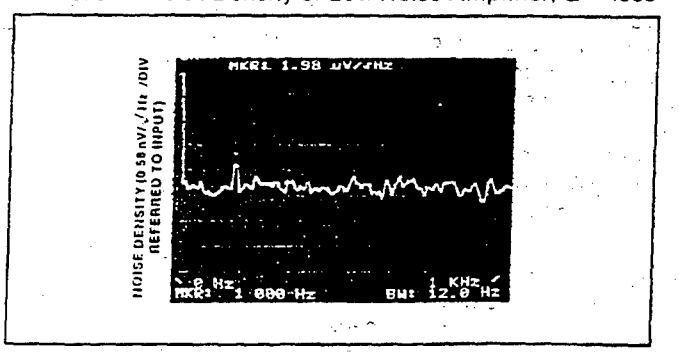


FIGURE 12: Digital Panning Control Circuit

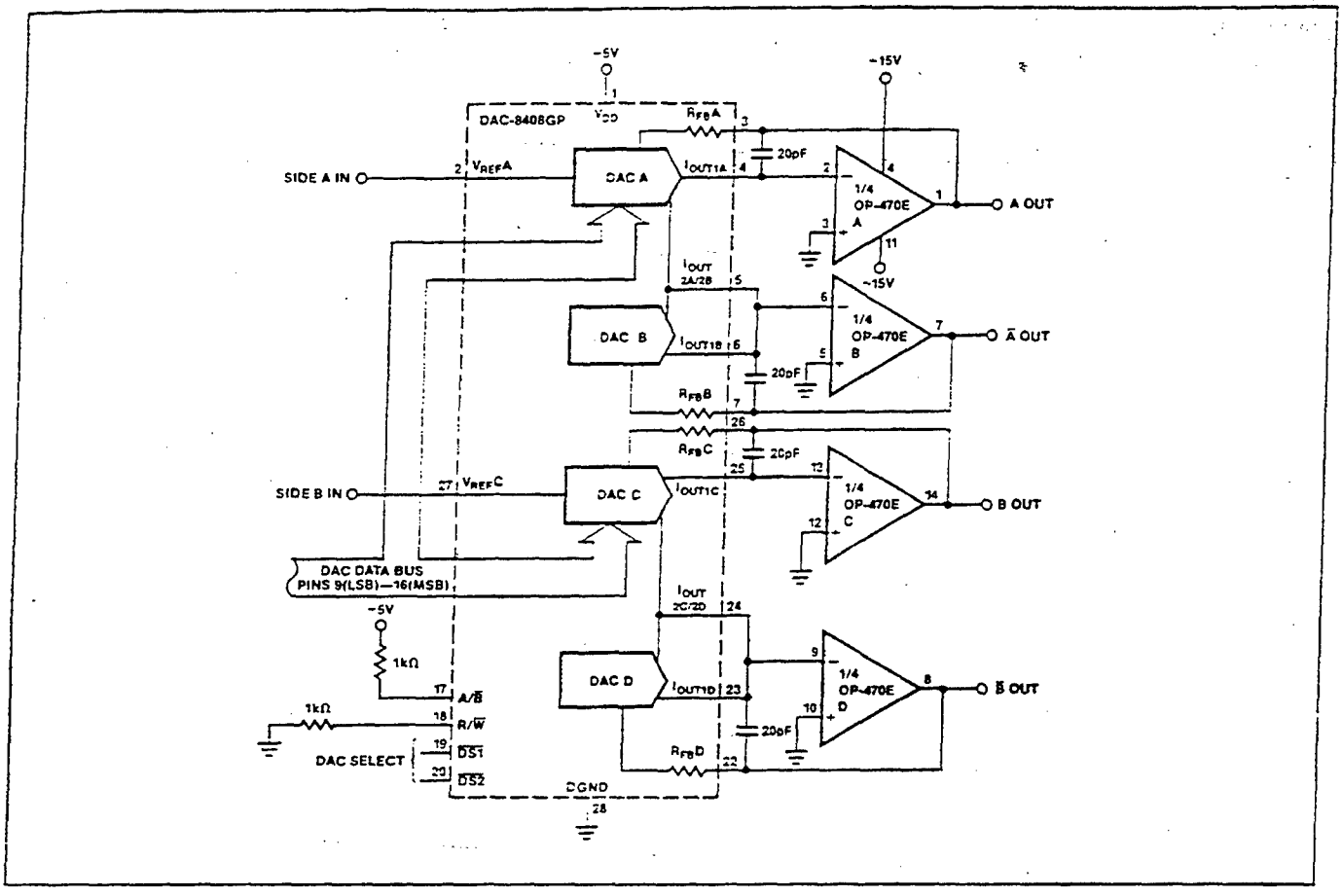


FIGURE 13: Digital Panning Control Output

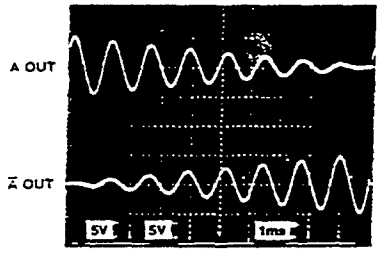
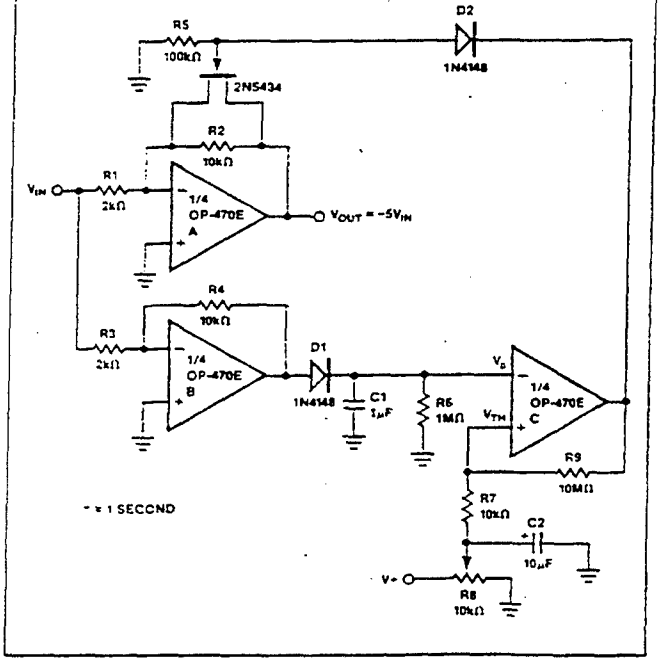


FIGURE 14: Squelch Amplifier



SQUELCH AMPLIFIER

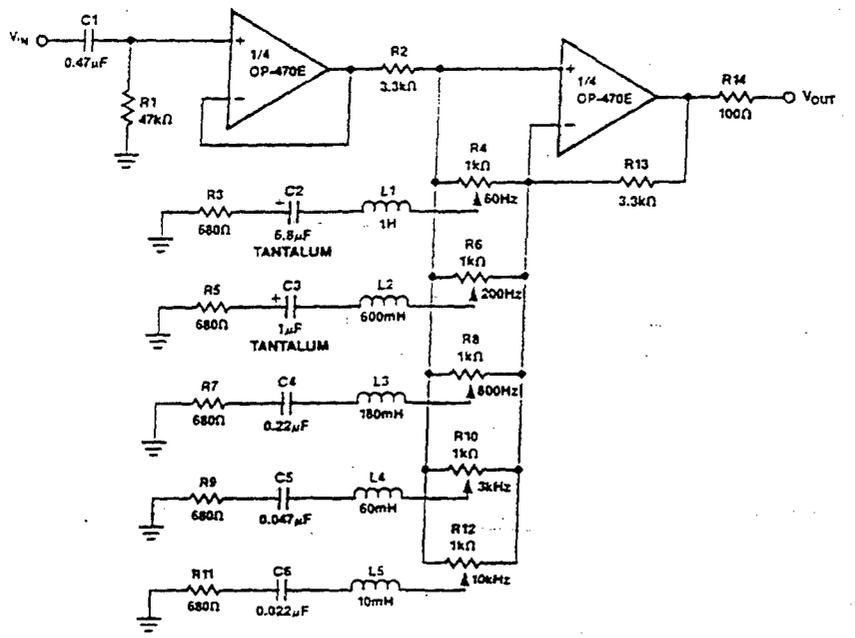
The circuit of Figure 14 is a simple squelch amplifier that uses a FET switch to cut off the output when the input signal falls below a preset limit.

The input signal is sampled by a peak detector with a time constant set by C1 and R6. When the output of the peak detector, V_p, falls below the threshold voltage, V_{TH}, set by R8, the comparator formed by op amp C switches from V− to V+. This drives the gate of the N-channel FET high, turning it ON, reducing the gain of the inverting amplifier formed by op amp A to zero.

E-BAND LOW NOISE STEREO GRAPHIC EQUALIZER

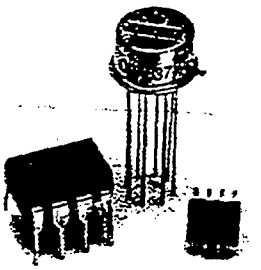
graphic equalizer circuit shown in Figure 15 provides of boost or cut over a 5-band range. Signal-to-noise ratio over a 20kHz bandwidth is better than 100dB referred to a 3V rms input. Larger inductors can be replaced by active inductors but this reduces the signal-to-noise ratio.

RE 15: 5-Band Low Noise Graphic Equalizer



2

BURR-BROWN®



OPA627
OPA637

AVAILABLE IN DIE

Precision High-Speed *Difet*® OPERATIONAL AMPLIFIERS

FEATURES

- VERY LOW NOISE: 4.5nV/√Hz at 10kHz
- FAST SETTLING TIME:
  OPA627—550ns to 0.01%
  OPA637—450ns to 0.01%
- LOW V_{OS}: 100µV max
- LOW DRIFT: 0.8µV/°C max
- LOW I_B: 5pA max
- OPA627: Unity-Gain Stable
- OPA637: Stable in Gain ≥ 5

APPLICATIONS

- PRECISION INSTRUMENTATION
- FAST DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- ACTIVE FILTERS

DESCRIPTION

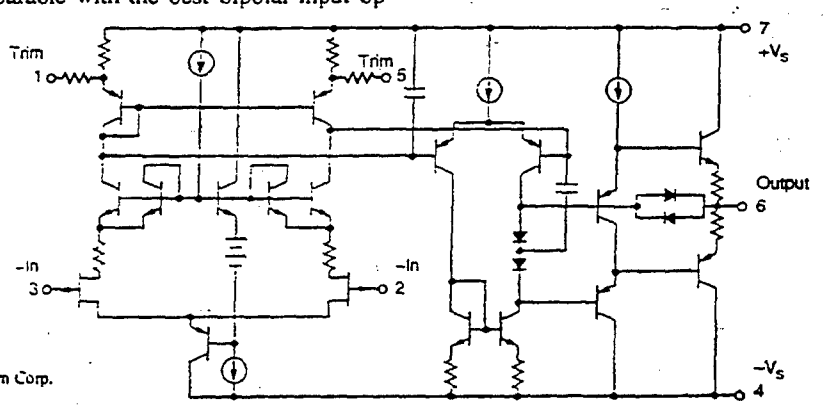
The OPA627 and OPA637 *Difet* operational amplifiers provide a new level of performance in a precision FET op amp. When compared to the popular OPA111 op amp, the OPA627/637 has lower noise, lower offset voltage, and much higher speed. It is useful in a broad range of precision and high speed analog circuitry.

The OPA627/637 is fabricated on a high-speed, dielectrically-isolated complementary NPN/PNP process. It operates over a wide range of power supply voltage—±4.5V to ±18V. Laser-trimmed *Difet* input circuitry provides high accuracy and low-noise performance comparable with the best bipolar-input op amps.

High frequency complementary transistors allow increased circuit bandwidth, attaining dynamic performance not possible with previous precision FET op amps. The OPA627 is unity-gain stable. The OPA637 is stable in gains equal to or greater than five.

Difet fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

The OPA627/637 is available in plastic DIP, SOIC and metal TO-99 packages. Industrial and military temperature range models are available.



Difet®, Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-998E

BURR-BROWN®

SPECIFICATIONS

ELECTRICAL

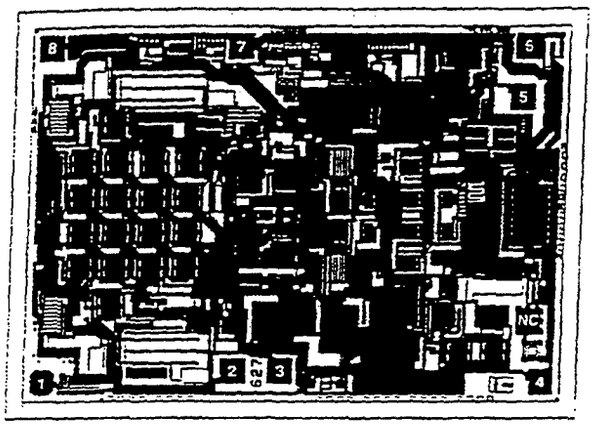
T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	OPA627BM/BP/SM OPA637BM/BP/SM MIN	TYP	MAX	OPA627AM/AP/AU OPA637AM/AP/AU MIN	TYP	MAX	UNITS
OFFSET VOLTAGE [1]								
Input Offset Voltage			40	100		130	250	µV
AP, BP, AU Grades			100	250		280	500	µV
Average Drift			0.4	0.8		1.2	2	µV/°C
AP, BP, AU Grades			0.8	2		2.5		µV/°C
Power Supply Rejection	V_S = ±4.5 to ±18V	106	120		100	116		dB
INPUT BIAS CURRENT [2]								
Input Bias Current	V_{CM} = 0V		1	5		2	10	pA
Over Specified Temperature	V_{CM} = 0V			1			2	nA
SM Grade	V_{CM} = 0V			50				nA
Over Common-Mode Voltage	V_{CM} = ±10V		1			2		pA
Input Offset Current	V_{CM} = 0V		0.5	5		1	10	pA
Over Specified Temperature	V_{CM} = 0V			1			2	nA
SM Grade				50				nA
NOISE								
Input Voltage Noise								
Noise Density: f = 10Hz			15	40		20		nV/√Hz
f = 100Hz			8	20		10		nV/√Hz
f = 1kHz			5.2	8		5.6		nV/√Hz
f = 10kHz			4.5	6		4.8		nV/√Hz
Voltage Noise, BW = 0.1 to 10Hz			0.6	1.6		0.8		µVp-p
Input Bias Current Noise								
Noise Density, f = 100Hz			1.6	2.5		2.5		fA/√Hz
Current Noise, BW = 0.1 to 10Hz			30	60		48		fAp-p
INPUT IMPEDANCE								
Differential			10^{13} || 8			*		Ω || pF
Common-Mode			10^{13} || 7			*		Ω || pF
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±11	±11.5		*	*		V
Over Specified Temperature		±10.5	±11		*	*		V
Common-Mode Rejection	V_{CM} = ±10.5V	106	116		100	110		dB
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±10V, R_L = 1kΩ	112	120		106	116		dB
Over Specified Temperature	V_O = ±10V, R_L = 1kΩ	106	117		100	110		dB
SM Grade	V_O = ±10V, R_L = 1kΩ	100	114					dB
FREQUENCY RESPONSE								
Slew Rate: OPA627	G = −1, 10V Step	40	55		*	*		V/µs
OPA637	G = −4, 10V Step	100	135		*	*		V/µs
Settling Time: OPA627 0.01%	G = −1, 10V Step		550			*		ns
0.1%	G = −1, 10V Step		450			*		ns
OPA637 0.01%	G = −4, 10V Step		450			*		ns
0.1%	G = −4, 10V Step		300			*		ns
Gain-Bandwidth Product: OPA627	G = 1		16			*		MHz
OPA637	G = 10		80			*		MHz
Total Harmonic Distortion + Noise	G = +1, f = 1kHz		0.00003			*		%
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±4.5		±18	*		*	V
Current			±7	±7.5		*	*	mA
OUTPUT								
Voltage Output	R_L = 1kΩ	±11.5	±12.3		*	*		
Over Specified Temperature		±11	±11.5		*	*		V
Current Output	V_O = ±10V		±45			*		mA
Short Circuit Current		±35	+70/−55	±100	*	*	*	mA
Output Impedance, Open-Loop	1MHz		55			*		Ω
TEMPERATURE RANGE								
Specification: AP, BP, AM, BM, AU		−25		+85	*		*	°C
SM		−55		+125				°C
Storage: AM, BM, SM		−60		+150	*		*	°C
AP, BP, AU		−40		+125	*		*	°C
θ_{JA}: AM, BM, SM			200			*		°C/W
AP, BP			100			*		°C/W
AU			160					°C/W

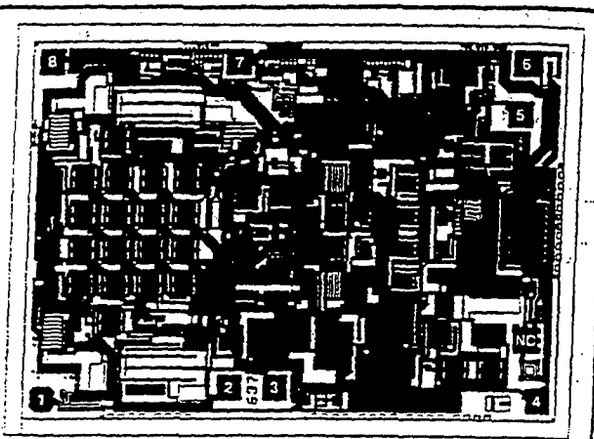
* Specifications same as "B" grade.

NOTES: (1) Offset voltage measured fully warmed-up. (2) High-speed test at T_J = 25°C. See Typical Performance Curves for warmed-up performance.

DICE INFORMATION



OPA627 DIE TOPOGRAPHY



OPA637 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Offset Trim	5	Offset Trim
2	–In	6	Output
3	+In	7	$+V_S$
4	$-V_S$	8	Substrate
		NC	No Connection

Substrate Bias: Dielectrically isolated. See data sheet for connection options.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	117 x 80 ±5	2.97 x 2.03 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Transistor Count		46
Backing:		None

See "DICE PRODUCTS" Appendix C in Burr-Brown Data Book, or contact factory for current information.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA627AP	Plastic DIP	–25°C to +85°C
OPA627BP	Plastic DIP	–25°C to +85°C
OPA627AU	SOIC	–25°C to +85°C
OPA627AM	TO-99 Metal	–25°C to +85°C
OPA627BM	TO-99 Metal	–25°C to +85°C
OPA627SM	TO-99 Metal	–55°C to +125°C
OPA637AP	Plastic DIP	–25°C to +85°C
OPA637BP	Plastic DIP	–25°C to +85°C
OPA637AU	SOIC	–25°C to +85°C
OPA637AM	TO-99 Metal	–25°C to +85°C
OPA637BM	TO-99 Metal	–25°C to +85°C
OPA637SM	TO-99 Metal	–55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

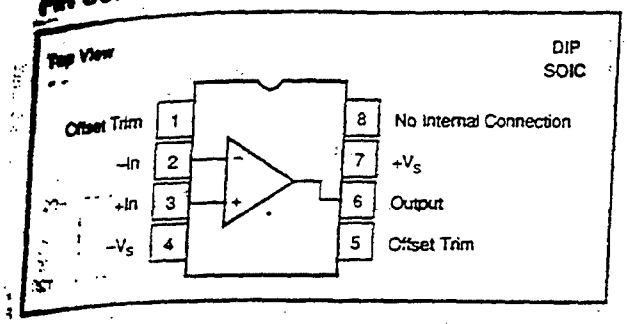
Supply Voltage	±18V
Input Voltage Range	$+V_S$ + 2V to $-V_S$ – 2V
Differential Input Range	Total V_S + 4V
Power Dissipation	1000mW
Operating Temperature	
M Package	–55°C to +125°C
P, U Package	–40°C to +125°C
Storage Temperature	
M Package	–65°C to +150°C
P, U Package	–40°C to +125°C
Junction Temperature	
M Package	+175°C
P, U Package	+150°C
Lead Temperature (soldering, 10s)	+300°C
SOIC (soldering, 3s)	+260°C

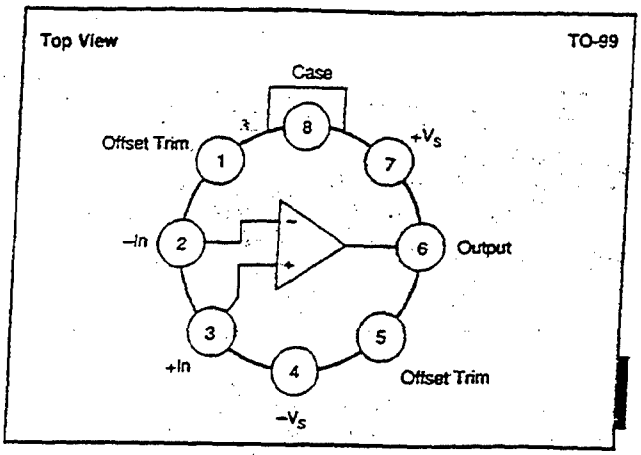
PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA627AP	Plastic DIP	006
OPA627BP	Plastic DIP	006
OPA627AU	SOIC	182
OPA627AM	TO-99 Metal	001
OPA627BM	TO-99 Metal	001
OPA627SM	TO-99 Metal	001
OPA637AP	Plastic DIP	006
OPA637BP	Plastic DIP	006
OPA637AU	SOIC	182
OPA637AM	TO-99 Metal	001
OPA637BM	TO-99 Metal	001
OPA637SM	TO-99 Metal	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN CONFIGURATIONS

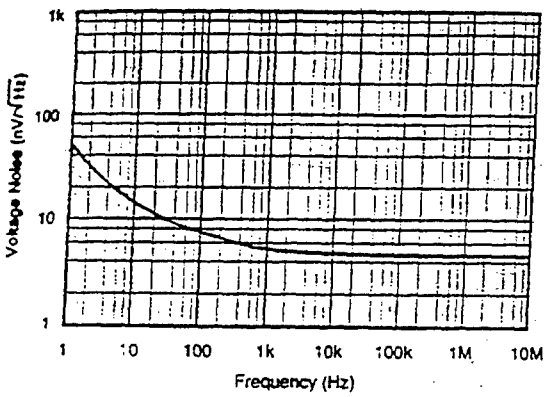




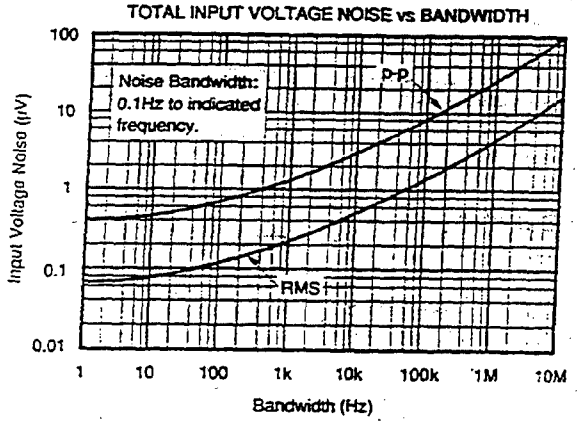
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

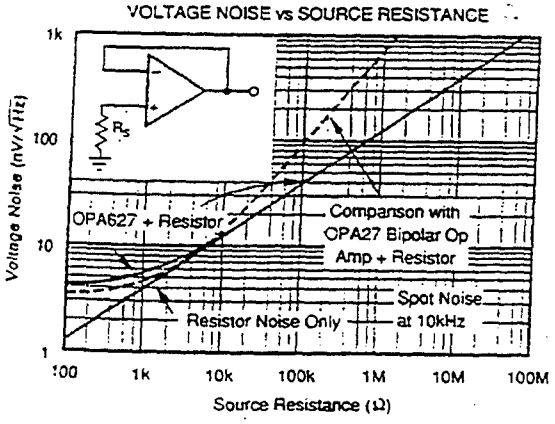
INPUT VOLTAGE NOISE SPECTRAL DENSITY



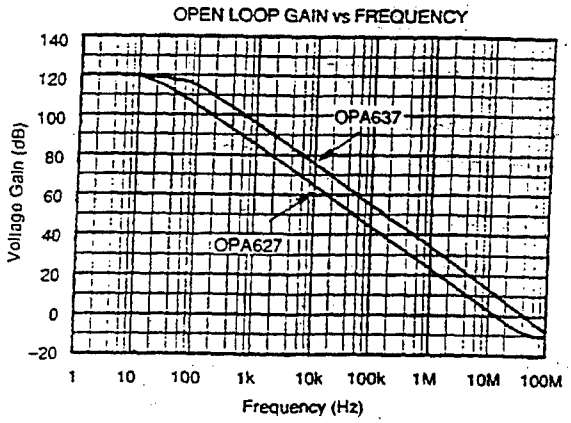
TOTAL INPUT VOLTAGE NOISE vs BANDWIDTH



VOLTAGE NOISE vs SOURCE RESISTANCE



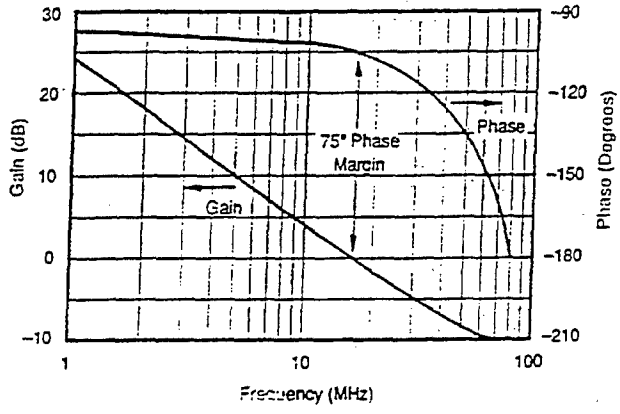
OPEN LOOP GAIN vs FREQUENCY



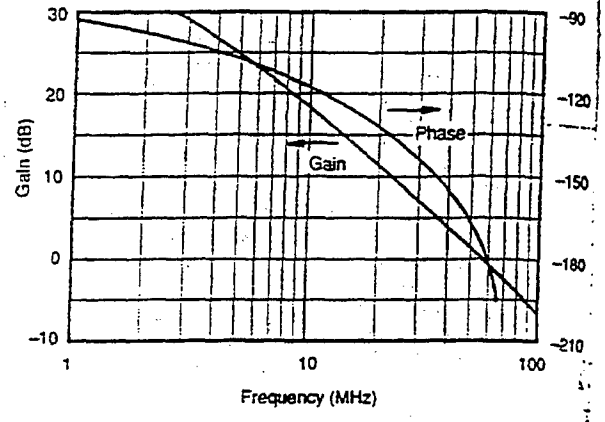
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

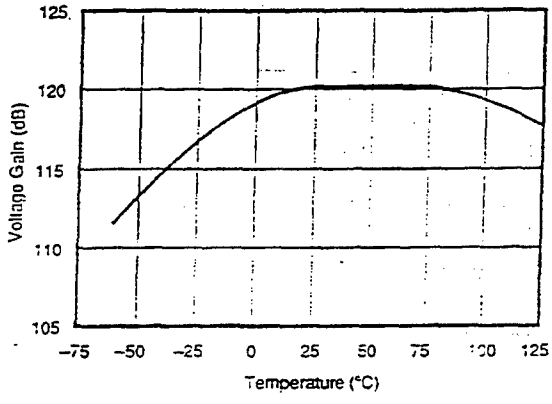
OPA627 GAIN/PHASE vs FREQUENCY



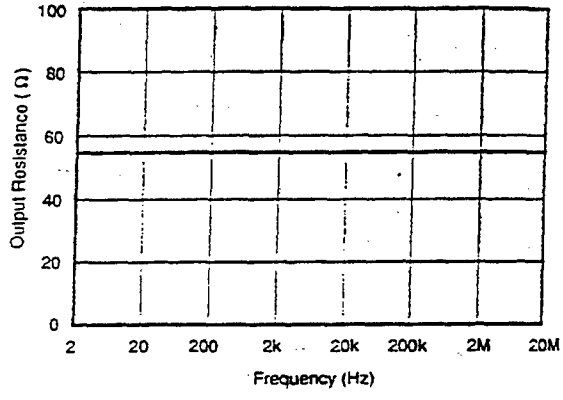
OPA637 GAIN/PHASE vs FREQUENCY



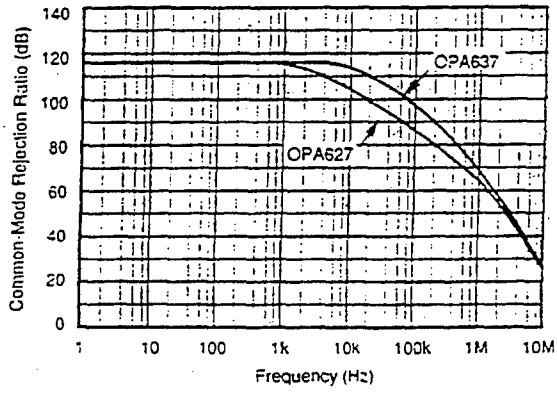
OPEN-LOOP GAIN vs TEMPERATURE



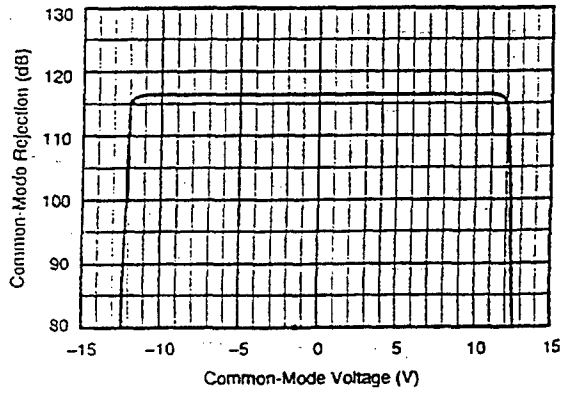
OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY



COMMON-MODE REJECTION vs FREQUENCY



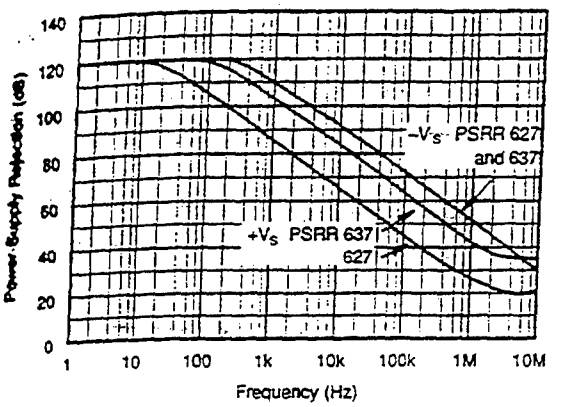
COMMON-MODE REJECTION vs INPUT COMMON MODE VOLTAGE



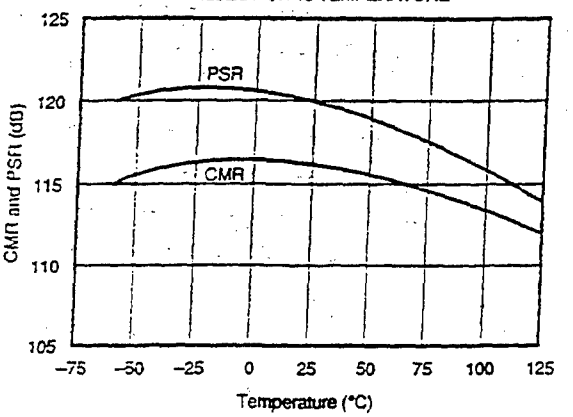
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

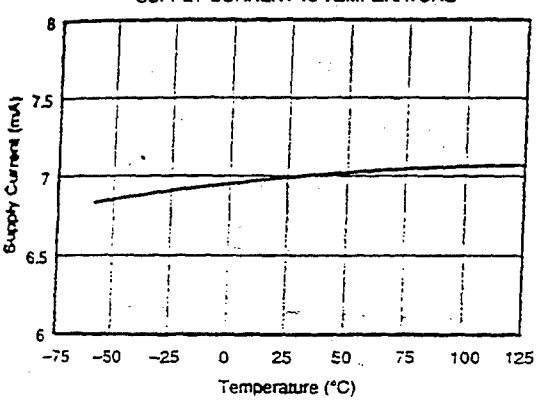
POWER-SUPPLY REJECTION vs FREQUENCY



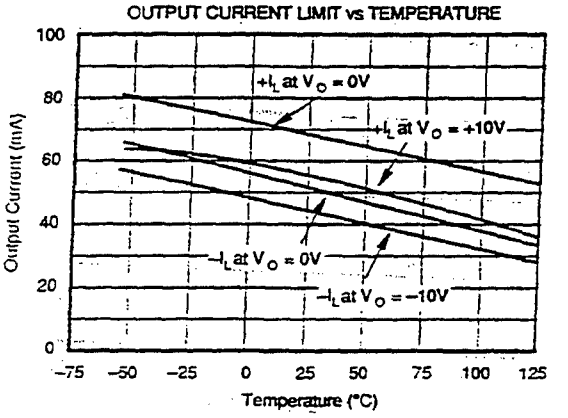
POWER-SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE



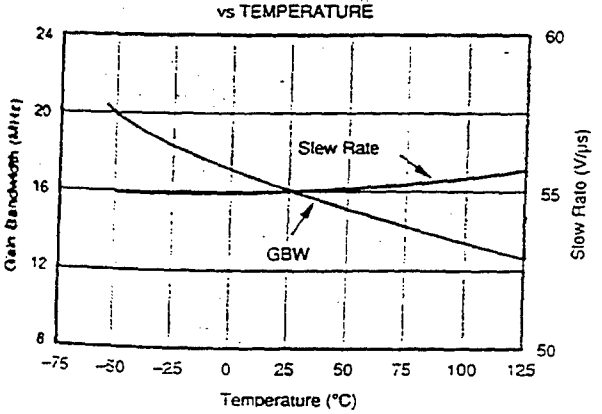
SUPPLY CURRENT vs TEMPERATURE



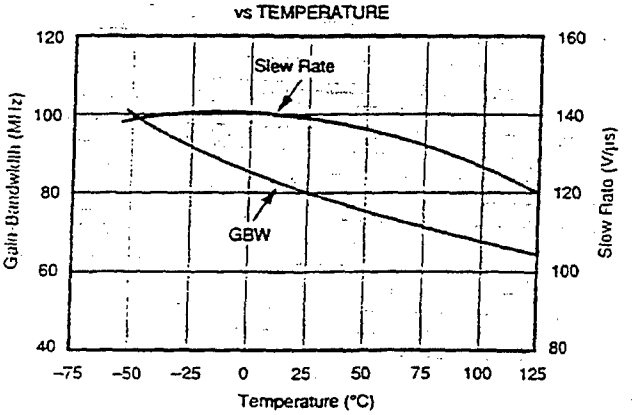
OUTPUT CURRENT LIMIT vs TEMPERATURE



OPA627 GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



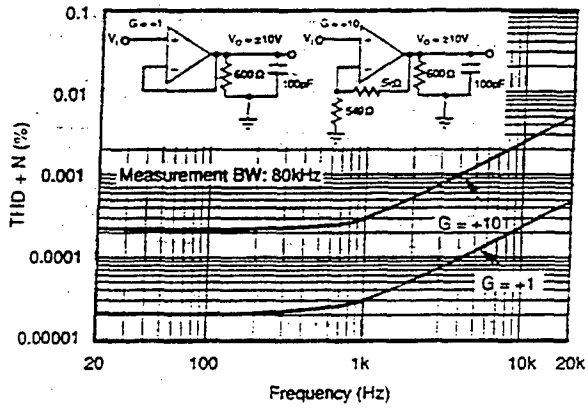
OPA637 GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



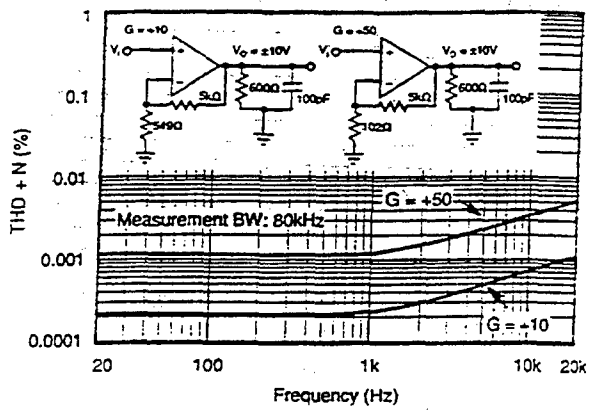
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

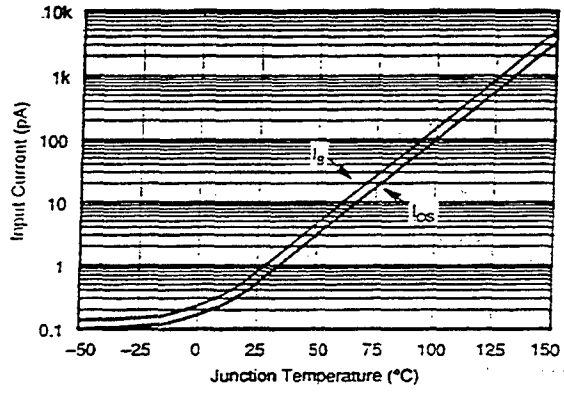
OPA627 TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



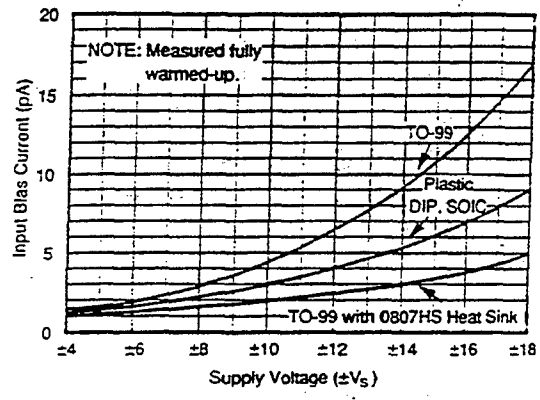
OPA637 TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



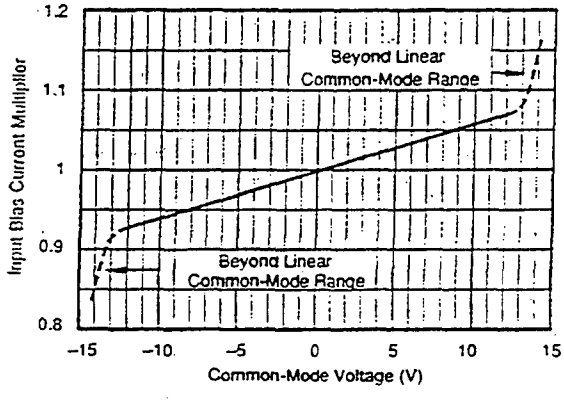
INPUT BIAS AND OFFSET CURRENT vs JUNCTION TEMPERATURE



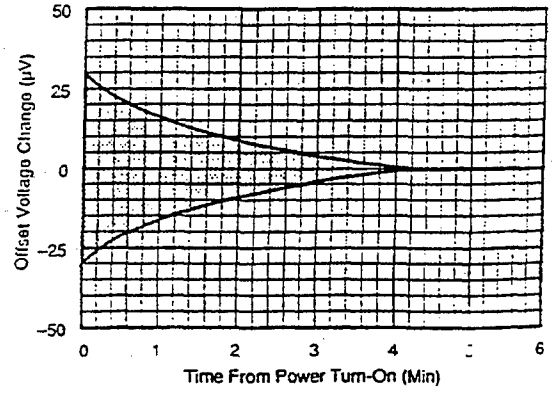
INPUT BIAS CURRENT vs POWER SUPPLY VOLTAGE



INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



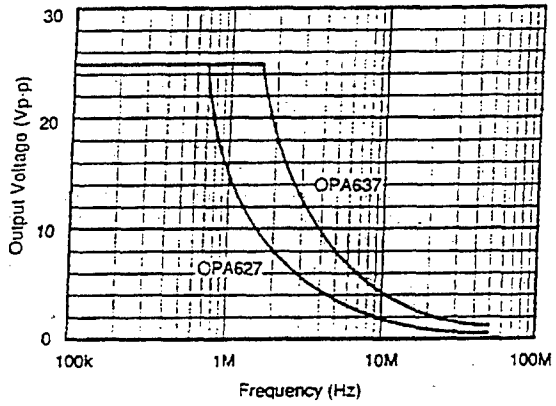
INPUT OFFSET VOLTAGE WARM-UP vs TIME



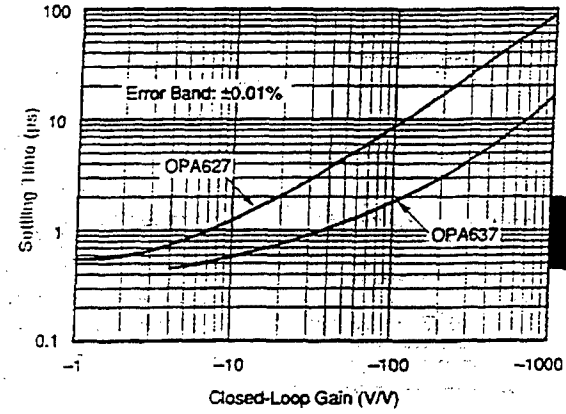
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

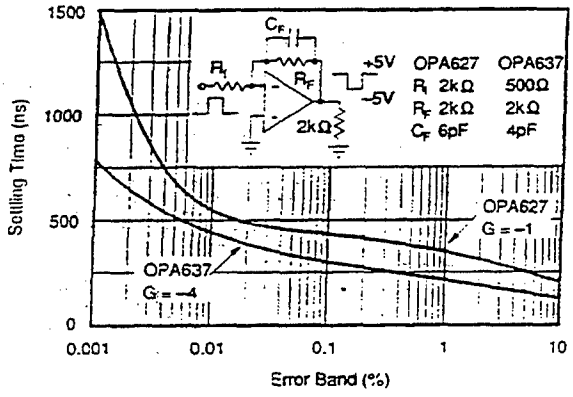
MAX OUTPUT VOLTAGE vs FREQUENCY



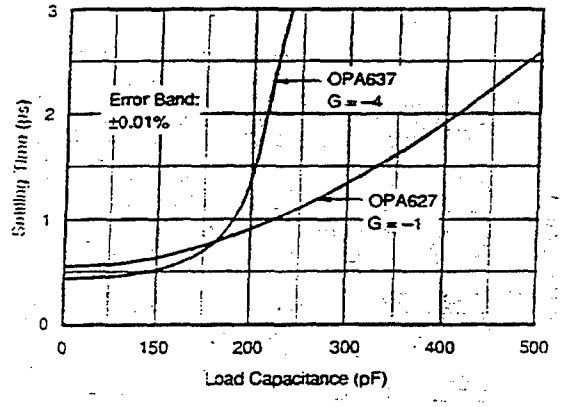
SETTLING TIME vs CLOSED-LOOP GAIN



SETTLING TIME vs ERROR BAND



SETTLING TIME vs LOAD CAPACITANCE



APPLICATIONS INFORMATION

The OPA627 is unity-gain stable. The OPA637 may be used to achieve higher speed and bandwidth in circuits with noise gain greater than five. Noise gain refers to the closed-loop gain of a circuit as if the non-inverting op amp input were being driven. For example, the OPA637 may be used in a non-inverting amplifier with gain greater than five, or an inverting amplifier of gain greater than four.

When choosing between the OPA627 or OPA637, it is important to consider the high frequency noise gain of your circuit configuration. Circuits with a feedback capacitor (Figure 1) place the op amp in unity noise-gain at high frequency. These applications must use the OPA627 for proper stability. An exception is the circuit in Figure 2, where a small feedback capacitance is used to compensate for the input capacitance at the op amp's inverting input. In this case, the closed-loop noise gain remains constant with frequency, so if the closed-loop gain is equal to five or greater, the OPA637 may be used.

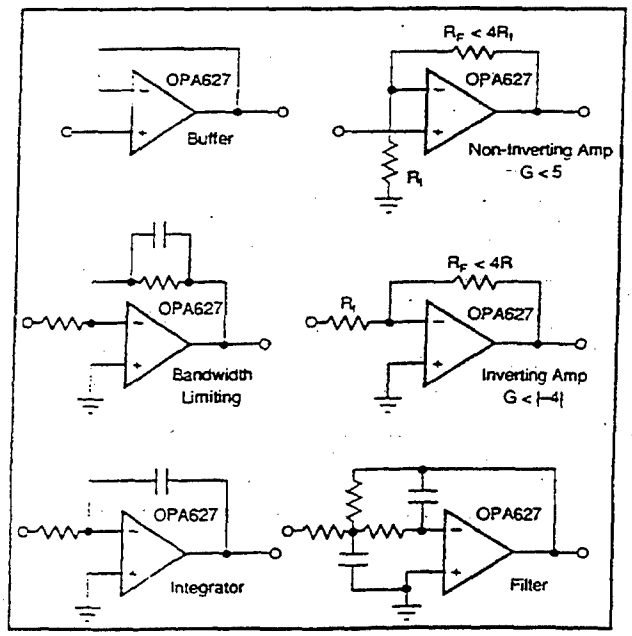


FIGURE 1. Circuits with Noise Gain Less than Five Require the OPA627 for Proper Stability.

OFFSET VOLTAGE ADJUSTMENT

The OPA627/637 is laser-trimmed for low offset voltage and drift, so many circuits will not require external adjustment. Figure 3 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system (such as in later amplification stages or in an A/D converter) because this could introduce excessive temperature drift. Generally, the offset drift will change by approximately 4µV/°C for 1mV of change in the offset voltage due to an offset adjustment (as shown on Figure 3).

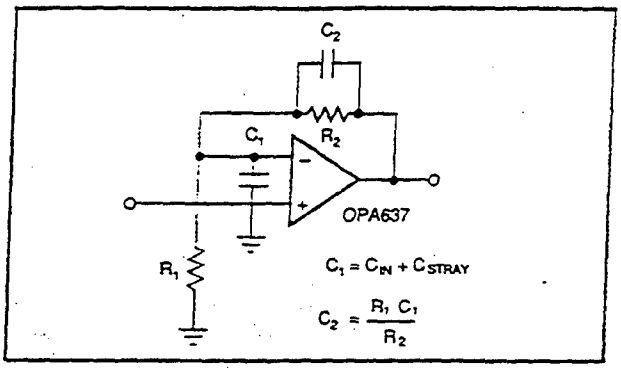


FIGURE 2. Circuits with Noise Gain Equal to or Greater than Five May Use the OPA637.

NOISE PERFORMANCE

Some bipolar op amps may provide lower voltage noise performance, but both voltage noise and bias current noise contribute to the total noise of a system. The OPA627/637 is unique in providing very low voltage noise and very low current noise. This provides optimum noise performance over a wide range of sources, including reactive source impedances. This can be seen in the performance curve showing the noise of a source resistor combined with the noise of an OPA627. Above a 2kΩ source resistance, the op amp contributes little additional noise. Below 1kΩ, op amp noise dominates over the resistor noise, but compares favorably with precision bipolar op amps.

CIRCUIT LAYOUT

As with any high speed, wide bandwidth circuit, careful layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance — especially at the input pins and feedback circuitry.

The case connection (pin 8 of TO-99 metal package only) should be connected to an AC ground for lowest possible pickup of external fields. While DC ground would be the most likely choice, pin 8 could also be connected to either power supply. (The case is not internally connected to the negative power supply as it is with most common op amps.) For lowest possible input bias current, the case may be driven as a guard—see Input Bias Current section. Pin 8 of the plastic DIP and SOIC versions has no internal connection.

Power supply connections should be bypassed with good high frequency capacitors positioned close to the op amp

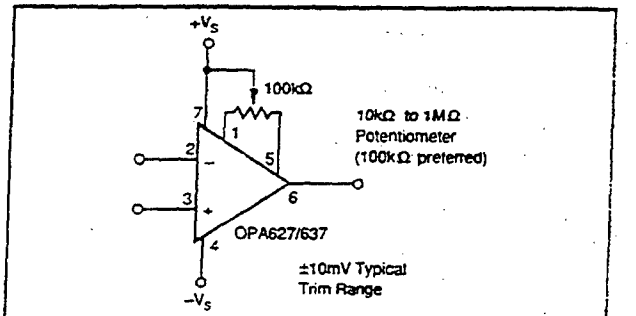


FIGURE 3. Optional Offset Voltage Trim Circuit.

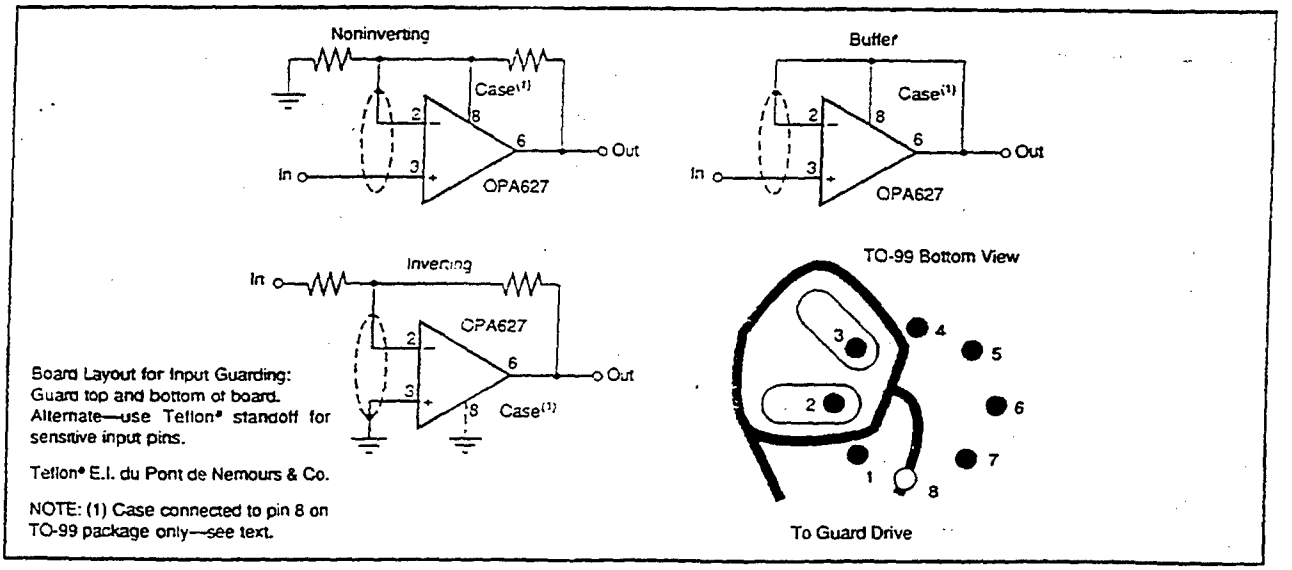


FIGURE 4. Connection of Input Guard for Lowest I_B.

pins. In most cases 0.1µF ceramic capacitors are adequate. The OPA627/637 is capable of high output current (in excess of 45mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as 1µF solid tantalum capacitors may improve dynamic performance in these applications.

INPUT BIAS CURRENT

Difet fabrication of the OPA627/637 provides very low input bias current. Since the gate current of a FET doubles approximately every 10°C, to achieve lowest input bias current, the die temperature should be kept as low as possible. The high speed and therefore higher quiescent current of the OPA627/637 can lead to higher chip temperature. A simple press-on heat sink such as the Burr-Brown model 807HS (TO-99 metal package) can reduce chip temperature by approximately 15°C, lowering the I_B to one-third its warmed-up value. The 807HS heat sink can also reduce low-frequency voltage noise caused by air currents and thermoelectric effects. See the data sheet on the 807HS for details.

Temperature rise in the plastic DIP and SOIC packages can be minimized by soldering the device to the circuit board. Wide copper traces will also help dissipate heat.

The OPA627/637 may also be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using ±5V power supplies reduces power dissipation to one-third of that at ±15V. This reduces the I_B of TO-99 metal package devices to approximately one-fourth the value at ±15V.

Leakage currents between printed circuit board traces can easily exceed the input bias current of the OPA627/637. A circuit board "guard" pattern (Figure 4) reduces leakage effects. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage current will flow harmlessly to the low-impedance node. The case connection (TO-99 metal package only) may also be driven at guard potential to minimize any leakage which might occur from the input pins to the case. The case is not internally connected to $-V_S$.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be removed with cleaning solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at 85°C.

Many FET-input op amps exhibit large changes in input bias current with changes in input voltage. Input stage cascode circuitry makes the input bias current of the OPA627/637 virtually constant with wide common-mode voltage changes. This is ideal for accurate high input-impedance buffer applications.

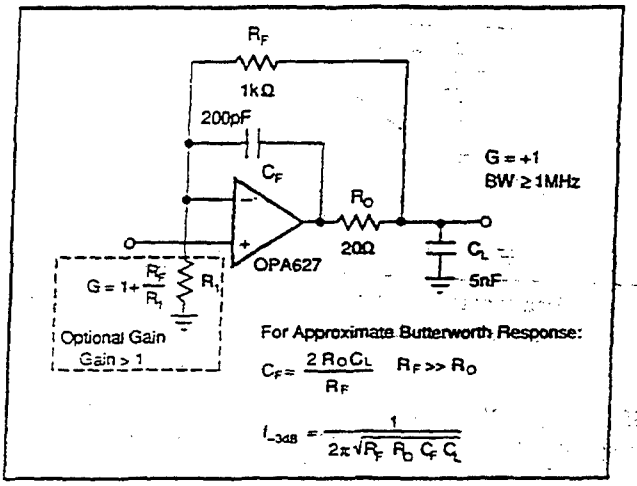


FIGURE 6. Driving Large Capacitive Loads.

PHASE-REVERSAL PROTECTION

The OPA627/637 has internal phase-reversal protection. Many FET-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This is most often encountered in non-inverting circuits when the input is driven below –12V, causing the output to reverse into the positive rail. The input circuitry of the OPA627/637 does not induce phase reversal with excessive common-mode voltage, so the output limits into the appropriate rail.

OUTPUT OVERLOAD

When the inputs to the OPA627/637 are overdriven, the output voltage of the OPA627/637 smoothly limits at approximately 2.5V from the positive and negative power supplies. If driven to the negative swing limit, recovery takes approximately 500ns. When the output is driven into the positive limit, recovery takes approximately 6µs. Output recovery of the OPA627 can be improved using the output clamp circuit shown in Figure 5. Diodes at the inverting input prevent degradation of input bias current.

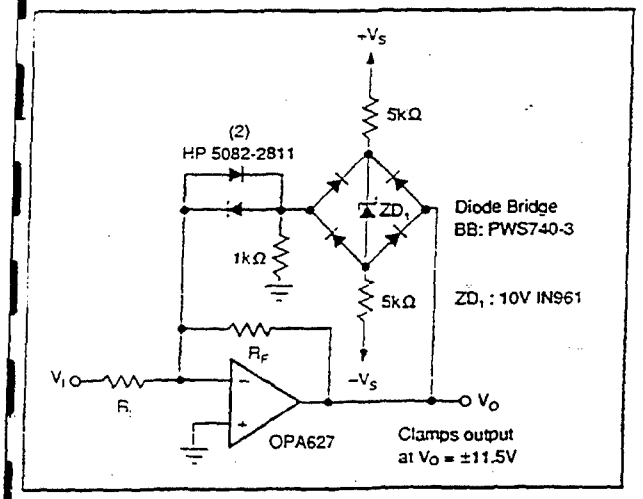


FIGURE 5. Clamp Circuit for Improved Overload Recovery.

CAPACITIVE LOADS

As with any high-speed op amp, best dynamic performance can be achieved by minimizing the capacitive load. Since a load capacitance presents a decreasing impedance at higher frequency, a load capacitance which is easily driven by a slow op amp can cause a high-speed op amp to perform poorly. See the typical curves showing settling times as a function of capacitive load. The lower bandwidth of the OPA627 makes it the better choice for driving large capacitive loads. Figure 6 shows a circuit for driving very large load capacitance. This circuit's two-pole response can also be used to sharply limit system bandwidth. This is often useful in reducing the noise of systems which do not require the full bandwidth of the OPA627.

INPUT PROTECTION

The inputs of the OPA627/637 are protected for voltages between $+V_S + 2V$ and $-V_S - 2V$. If the input voltage can exceed these limits, the amplifier should be protected. The diode clamps shown in Figure 7a will prevent the input voltage from exceeding one forward diode voltage drop beyond the power supplies—well within the safe limits. If the input source can deliver current in excess of the maximum forward current of the protection diodes, use a series resistor, R_S, to limit the current. Be aware that adding resistance to the input will increase noise. The $4nV/\sqrt{Hz}$ theoretical thermal noise of a $1k\Omega$ resistor will add to the $4.5nV/\sqrt{Hz}$ noise of the OPA627/637 (by the square-root of the sum of the squares), producing a total noise of $6nV/\sqrt{Hz}$. Resistors below 100Ω add negligible noise.

Leakage current in the protection diodes can increase the total input bias current of the circuit. The specified maximum leakage current for commonly used diodes such as the 1N4148 is approximately 25nA—more than a thousand times larger than the input bias current of the OPA627/637. Leakage current of these diodes is typically much lower and may be adequate in many applications. Light falling on the junction of the protection diodes can dramatically increase leakage current, so common glass-packaged diodes should be shielded from ambient light. Very low leakage can be achieved by using a diode-connected FET as shown. The 2N4117A is specified at 1pA and its metal case shields the junction from light.

Sometimes input protection is required on I/V converters or inverting amplifiers (Figure 7b). Although in normal operation, the voltage at the summing junction will be near zero (equal to the offset voltage of the amplifier), large input transients may cause this node to exceed 2V beyond the

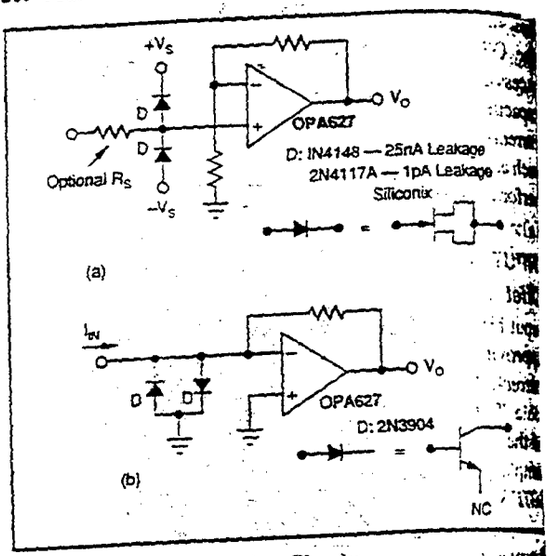


FIGURE 7. Input Protection Circuits.

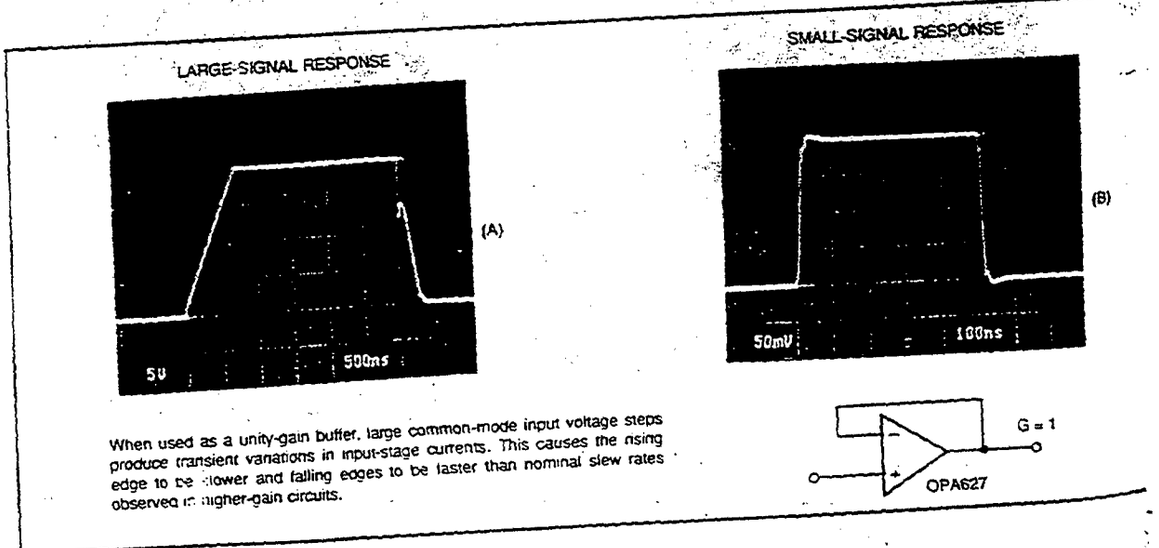


FIGURE 8. OPA627 Dynamic Performance, G = +1.

power supplies. In this case, the summing junction should be protected with diode clamps connected to ground. Even with the the low voltage present at the summing junction, common signal diodes may have excessive leakage current. Since the reverse voltage on these diodes is clamped, a diode-connected signal transistor can be used as an inexpensive low leakage diode, (Figure 7b).

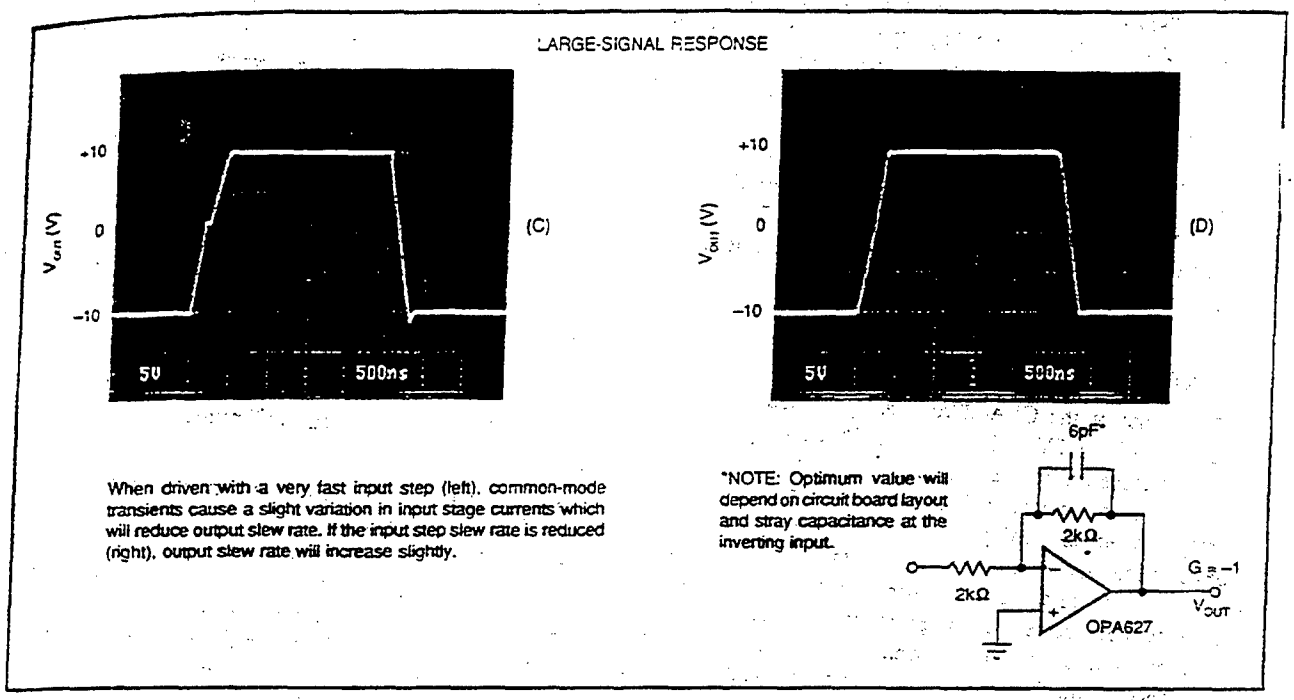


FIGURE 9. OPA627 Dynamic Performance, G = –1.

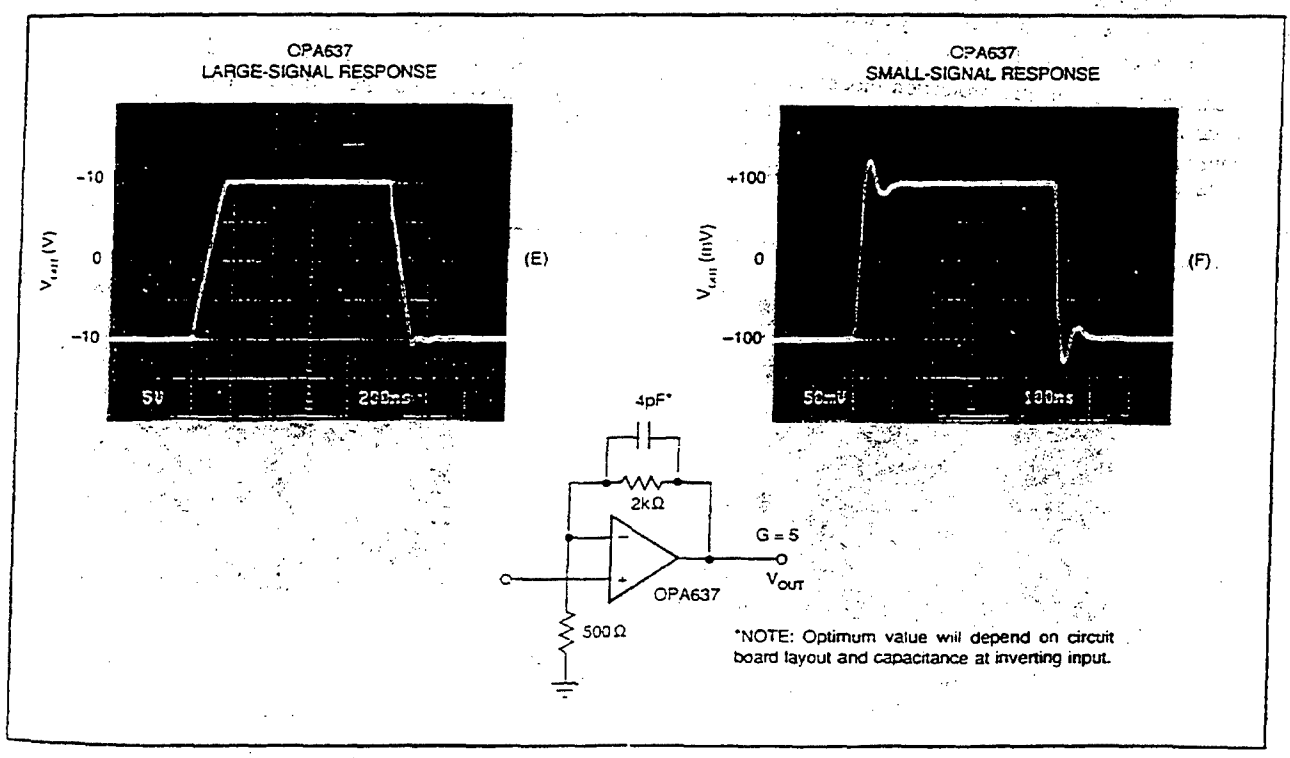
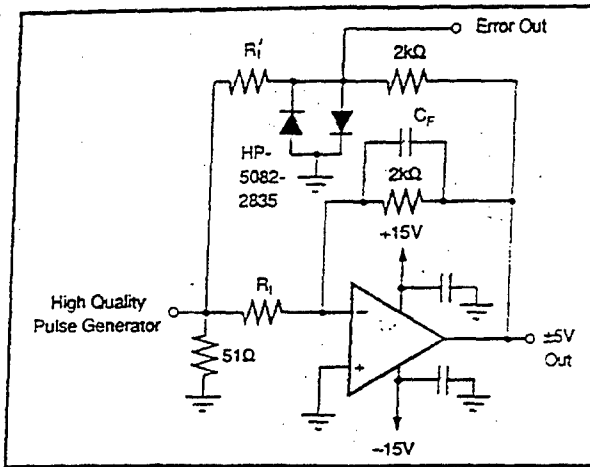


FIGURE 10. OPA637 Dynamic Response, G = 5.



	OPA627	OPA637
R_1, R_2	2kΩ	500Ω
C_F	6pF	4pF
Error Band (0.01%)	±0.5mV	±0.2mV

NOTE: C_F is selected for best settling time performance depending on test fixture layout. Once optimum value is determined, a fixed capacitor may be used.

FIGURE 11. Settling Time and Slew Rate Test Circuit.

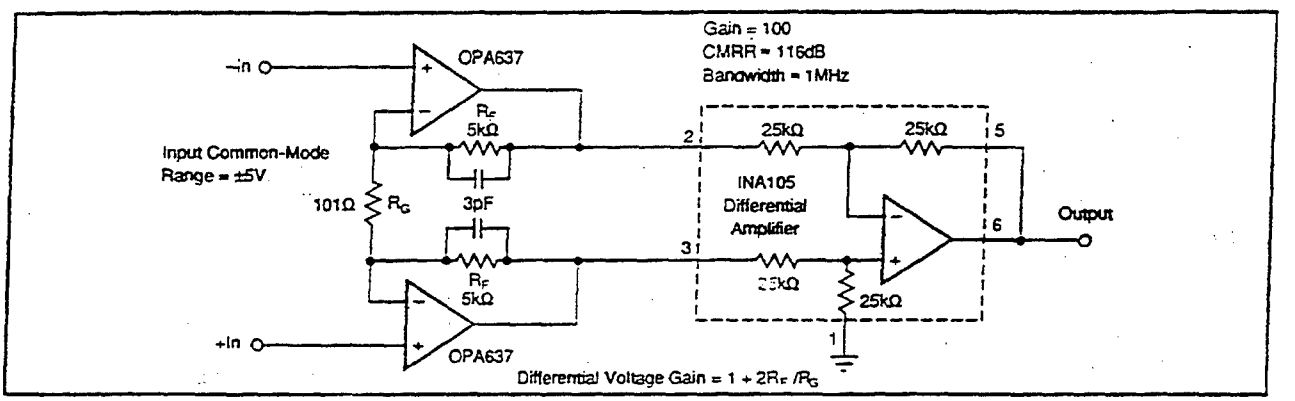


FIGURE 12. High Speed Instrumentation Amplifier. Gain = 100.

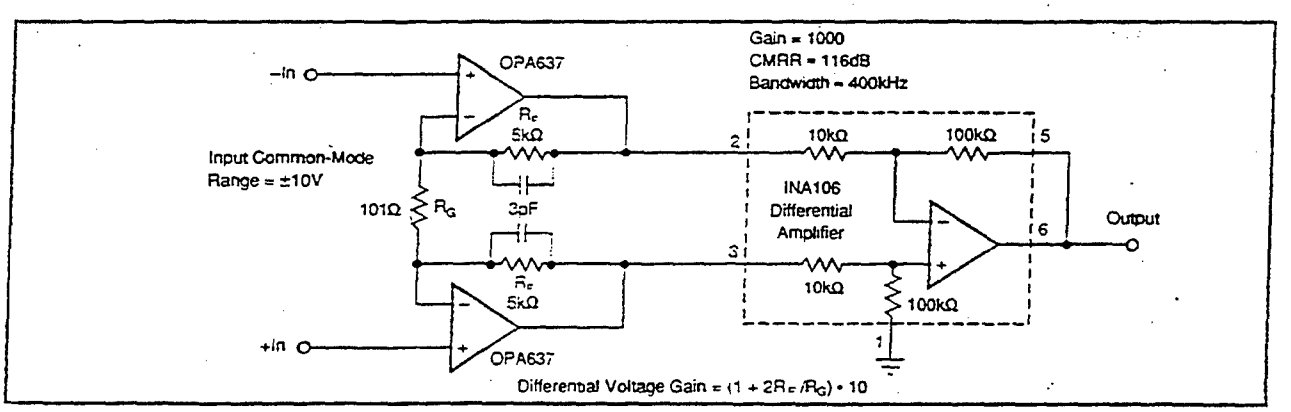
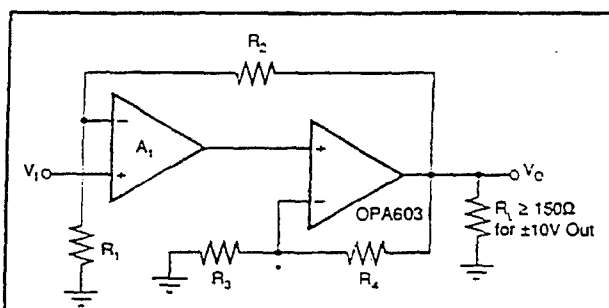


FIGURE 13. High Speed Instrumentation Amplifier. Gain = 1000.



This composite amplifier uses the OPA603 current-feedback op amp to provide extended bandwidth and slew rate at high closed-loop gain. The feedback loop is closed around the composite amp, preserving the precision input characteristics of the OPA627/637. Use separate power supply bypass capacitors for each op amp.

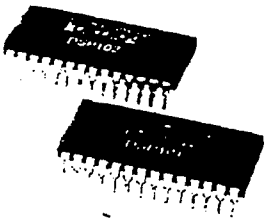
*Minimize capacitance at this node.

GAIN (V/V)	A_1 OP AMP	R_1 (Ω)	R_2 (kΩ)	R_3 (Ω)	R_4 (kΩ)	–3dB (MHz)	SLEW RATE (V/µs)
100	OPA627	50.5[1]	4.99	20	1	15	700
1000	OPA637	49.9	4.99	12	1	11	500

NOTE: (1) Closest 1/2% value.

FIGURE 14. Composite Amplifier for Wide Bandwidth.

BURR-BROWN INT. s.a.
18, avenue Dutartre
B.P. 90
78152 LE CHESNAY CEDEX
TEL : (1) 39.54.35.58
FAX : (1) 39.54.87.03



DSP101
DSP102

DSP-Compatible Sampling Single/Dual ANALOG-TO-DIGITAL CONVERTERS

FEATURES

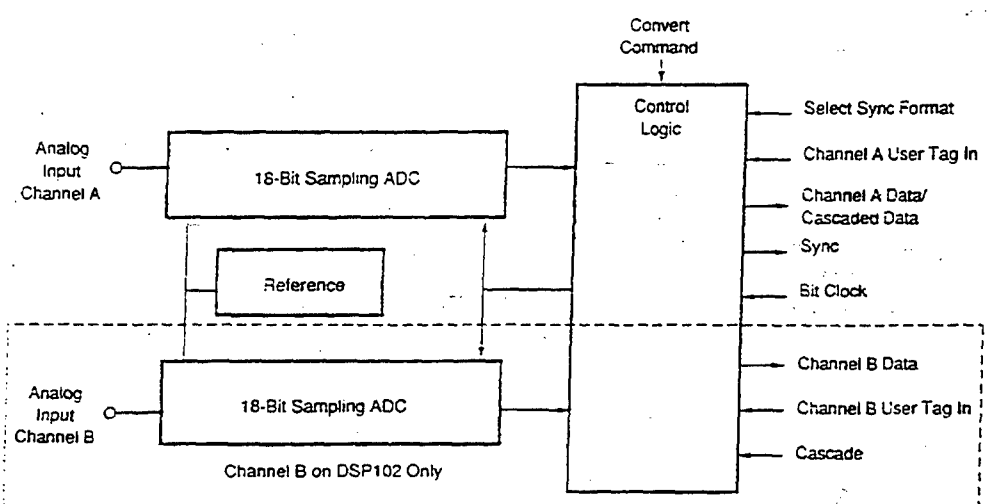
- ZERO-CHIP INTERFACE TO STANDARD DSP ICs: AD, AT&T, MOTOROLA, TI
- SINGLE CHANNEL: DSP101
- DUAL CHANNEL: DSP102
  Two Serial Outputs or Cascade to Single 32-Bit Word
- SAMPLING RATE TO 200kHz
- DYNAMIC SPECIFICATIONS:
  Signal/(Noise + Distortion) = 88dB;
  Spurious-Free Dynamic Range = 94dB;
  THD = –91dB
- SERIAL OUTPUT DATA COMPATIBLE WITH 16-, 24-, AND 32-BIT DSP IC FORMATS

DESCRIPTION

The DSP101 and DSP102 are high performance sampling analog-to-digital converters designed for simplicity of use with modern digital signal processing ICs. Both are complete with all interface logic for use directly with DSP ICs, and provide full sampling and conversion at rates up to 200kHz.

The DSP101 offers a single conversion channel, with 18 bits of serial data output, allowing the user to drive 16-bit, 24-bit, or 32-bit DSP ports. The DSP102 offers two complete conversion channels, with either two full 18-bit output ports, or a mode to cascade two 16-bit conversions into a 32-bit port as one word.

Both the DSP101 and DSP102 are packaged in standard, low-cost 28-pin plastic DIP packages. Each is offered in two performance grades to match application requirements.



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PDS-1068B
Printed in U.S.A. December, 1991

SPECIFICATIONS

ELECTRICAL

T_A = 0°C to 70°C, ±2.75V input signal, sampling frequency (f_S) = 200kHz, $V_A+ = V_D = +5V$, $V_A- = -5V$, 16MHz external clock on OSC1, CLKOUT tied to CLKIN, 8MHz data transfer clock on XCLK, data analysis band-limited to 20kHz, unless otherwise specified.

PARAMETER	CONDITIONS	DSP101JP DSP102JP MIN	DSP101JP DSP102JP TYP	DSP101JP DSP102JP MAX	DSP101KP DSP102KP MIN	DSP101KP DSP102KP TYP	DSP101KP DSP102KP MAX	UNITS
RESOLUTION				18				Bits
ANALOG INPUT								
Voltage Range			±2.75V					V
Impedance			1					kΩ
Capacitance			20					pF
THROUGHPUT SPEED								
Complete Cycle	Acquisition + Conversion			5				µs
Throughput Rate		200						kHz
AC ACCURACY [1]								
Signal to (Noise + Distortion) Ratio	f_{IN} = 1kHz	83	86		86	88		dB[2]
	f_{IN} = 1kHz (–60dB)		32					dB
	f_{IN} = 25kHz		82					dB
Total Harmonic Distortion	f_{IN} = 1kHz		–90	–86		–91	–89	dB
Spurious-Free Dynamic Range	f_{IN} = 1kHz	89	92		92	94		dB
Signal to Noise Ratio (SNR)	f_{IN} = 1kHz	84	88		87	89		dB
DC ACCURACY								
Gain Error				±5				%
Gain Error Mismatch	DSP102 Channels			±2				%
Integral Linearity	±2.75V Input Range		Sufficient to meet AC Accuracy Specifications					
Differential Linearity	±2.75V Input Range		Sufficient to meet AC Accuracy Specifications					
Integral Linearity Error	±0.7V Input Range		±0.003					%
Differential Linearity Error	±0.7V Input Range		±0.002					%
No Missing Codes	±0.7V Input Range		14					Bits
Bipolar Zero Error [3]			±2					mV
Bipolar Zero Mismatch [3]	DSP102 Channels		±2					mV
Power Supply Sensitivity	–5.25V < V_A- < –4.75V		–60					dB
	+4.75V < V_A+, V_D+ < +5.25V		–60					dB
SAMPLING DYNAMICS								
Aperture Delay			30					ns
Aperture Jitter			100					ps,rms
Transient Response			1					µs
Overvoltage Recovery			5					µs
DIGITAL INPUTS								
Logic Levels (Except OSC1)								
V_{IL}	I_{IL} = ±10µA	0		+0.8				V
V_{IH}	I_{IH} = ±10µA	+2.4		+5				V
OSC1 Clock				74HC Compatible				
Frequency				16				MHz
Data Transfer Clock (XCLK)								
Frequency		0.1		12				MHz
Duty Cycle		40	50	60				%
Conversion Clock (CLKIN)								
Frequency		0.5		5.33				MHz
Duty Cycle		25	33	55				%
DIGITAL OUTPUTS								
Format			Serial: MSB first; 16/18-bit and Cascaded 32-bit Mode					
Coding			Binary Two's Complement					
Logic Levels (Except OSC2)								
V_{OL}	I_{SINK} = 4mA	0		+0.4				V
V_{OH}	I_{SOURCE} = 4mA	+2.4		+5				V
OSC2			Can only be used to drive crystal oscillator.					
Conversion Clock (CLKOUT)								
Drive Capability		±2mA						mA
POWER SUPPLIES								
Rated Voltage								
V_A+		+4.75	+5	+5.25				V
V_A-		–5.25	–5	–4.75				V
V_D		+4.75	+5	+5.25				V
Power Consumption	XCLK = OSC1 = 12MHz		250	425				mW
Supply Current	XCLK = OSC1 = 12MHz							
I_A+			30	45				mA
I_A-			–18	–25				mA
I_D			5	15				mA
TEMPERATURE RANGE								
Specification		0		+70				°C
Storage		–65		+125				°C

NOTES: (1) All dynamic specifications are based on 2048-point FFTs, using four-term Blackman-Harris window. (2) All specifications in dB are referred to a full-scale input, ±2.75Vp-p. (3) Adjustable to zero with external potentiometer.

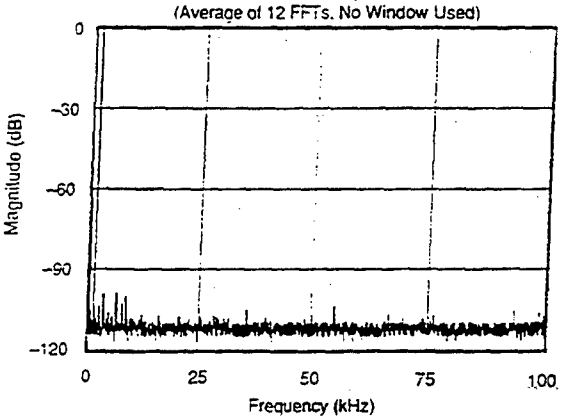
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, $V_A+ = V_D+ = +5V$, $V_A- = V_D- = -5V$, Sampling Frequency f_S = 200kHz; External Clock Input at OSC1 = $80f_S$ = 16MHz, XCLK = $40f_S$ = 8MHz; Using 2048 Point FFT; Data analysis limited to 0 to 20kHz band; Unless otherwise specified.

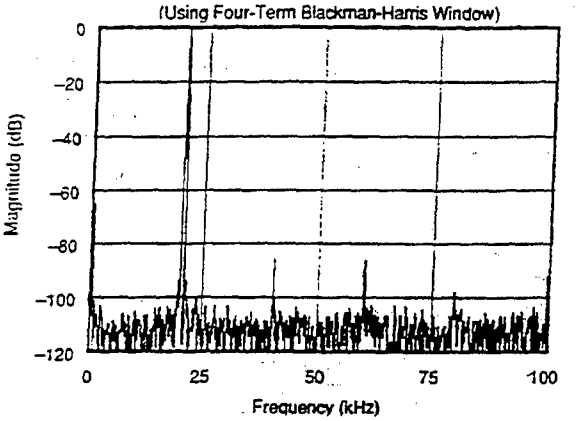
SINAD means Signal-to-(Noise + Distortion) Ratio.
SNR means Signal-to-Noise Ratio excluding harmonics thru the 8th.

THD means Total Harmonic Distortion thru 8th harmonic.
SFDR means Spurious Free Dynamic Range, including harmonics.

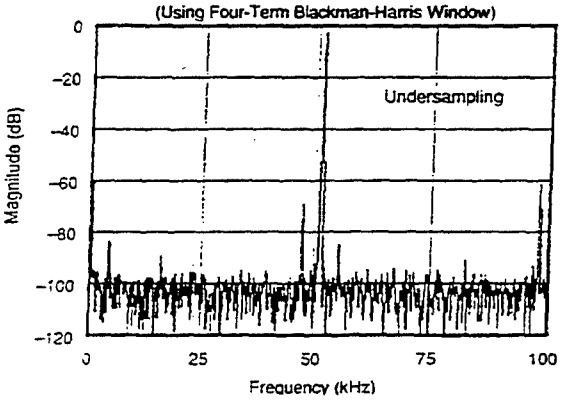
FREQUENCY SPECTRUM of ±2.75V, 1kHz INPUT
(Average of 12 FFTs, No Window Used)



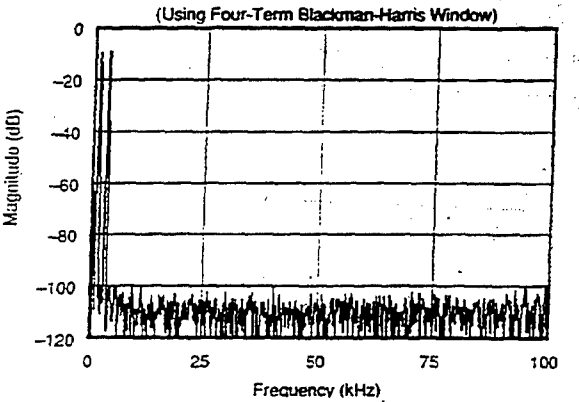
FREQUENCY SPECTRUM of ±2.75V, 20kHz INPUT
(Using Four-Term Blackman-Harris Window)



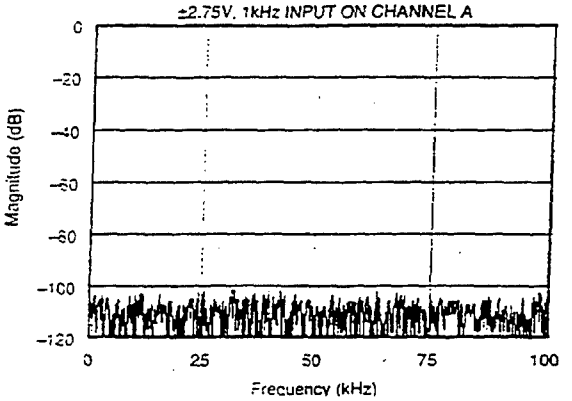
FREQUENCY SPECTRUM of ±2.75V, 451kHz INPUT
(Using Four-Term Blackman-Harris Window)



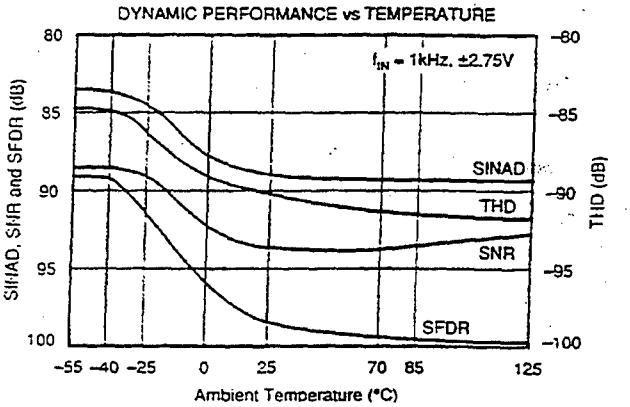
INTERMODULATION DISTORTION WITH 1kHz AND 3kHz INPUTS
(Using Four-Term Blackman-Harris Window)



DSP102 CHANNEL SEPARATION ON CHANNEL B WITH
±2.75V, 1kHz INPUT ON CHANNEL A



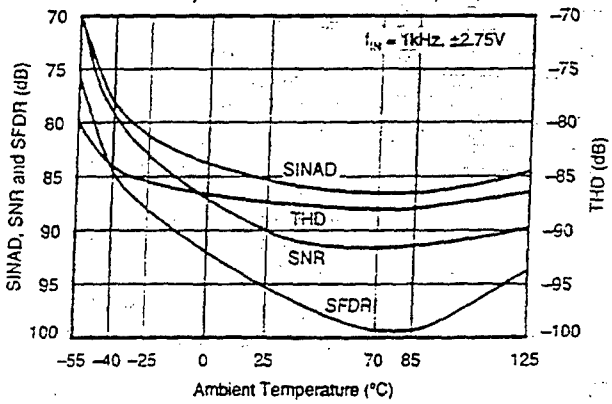
DYNAMIC PERFORMANCE vs TEMPERATURE



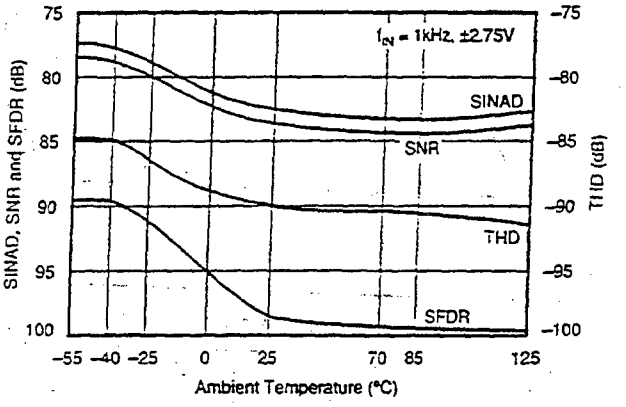
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, $V_A+ = V_D+ = +5V$, $V_A- = V_D- = -5V$, Sampling Frequency f_S = 200kHz; External Clock Input at OSC1 = $80f_S$ = 16MHz, XCLK = $40f_S$ = 8MHz; Using 2048 Point FFT; Data analysis limited to 0 to 20kHz band; Unless otherwise specified.

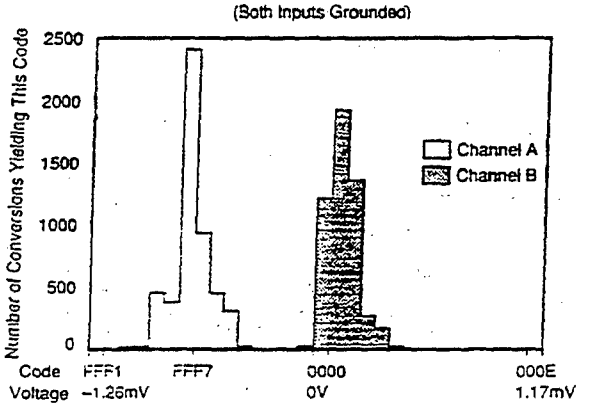
DYNAMIC PERFORMANCE vs TEMPERATURE
(f_S = 180kHz Asychronous to 12.288MHz Crystal Between OSC1 and OSC2)



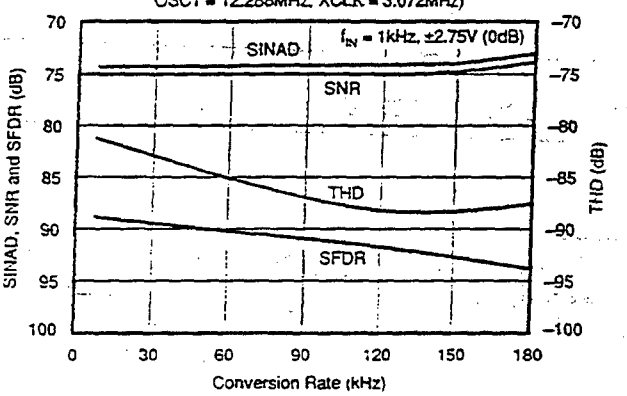
DYNAMIC PERFORMANCE vs TEMPERATURE
(Data Analysis Over Full 0 to 100kHz Band)



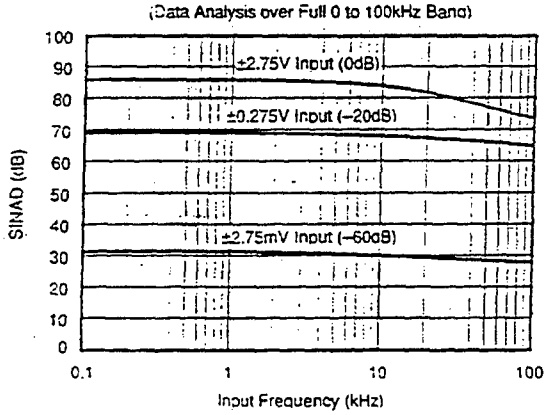
HISTOGRAM OF 5k CONVERSION RESULTS ON DSP102
(Both Inputs Grounded)



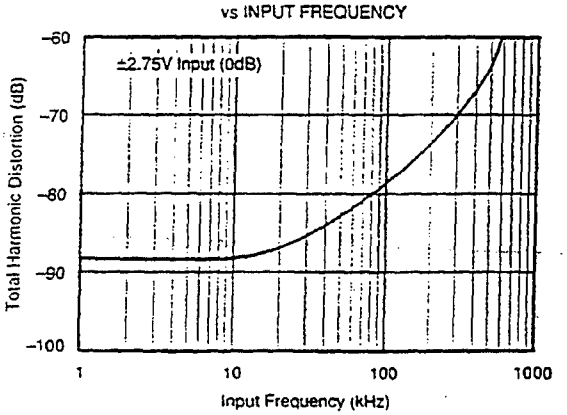
DYNAMIC PERFORMANCE vs CONVERSION RATE
(Data Analysis over Full 0 to $f_S/2$ Band,
OSC1 = 12.288MHz, XCLK = 3.072MHz)



SINAD vs INPUT FREQUENCY
(Data Analysis over Full 0 to 100kHz Band)

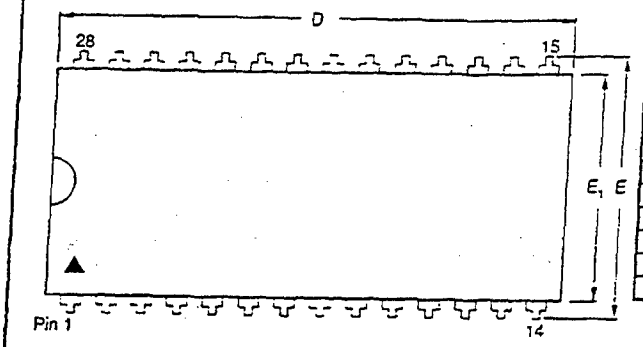


TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY

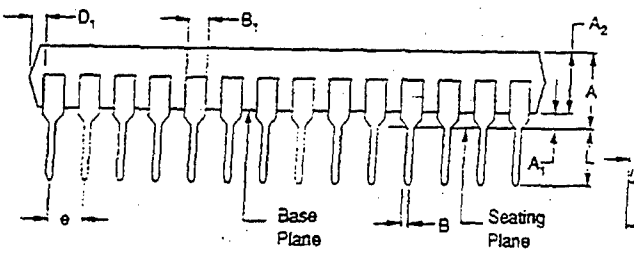


MECHANICAL

P Package — 28-Pin Plastic, Double-Wide DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.250	3.94	6.35
A_1	.015	.070	.381	1.38
A_2	.140	.185	3.57	4.70
B	.014	.022	.356	.559
B_1	.040	.070	1.02	1.78
C	.008	.015	.20	.381
D	1.435	1.480	36.45	37.59
D_1	.040	.100	1.020	2.540
E	.600	.625	15.24	15.88
E_1	.525	.565	13.34	14.35

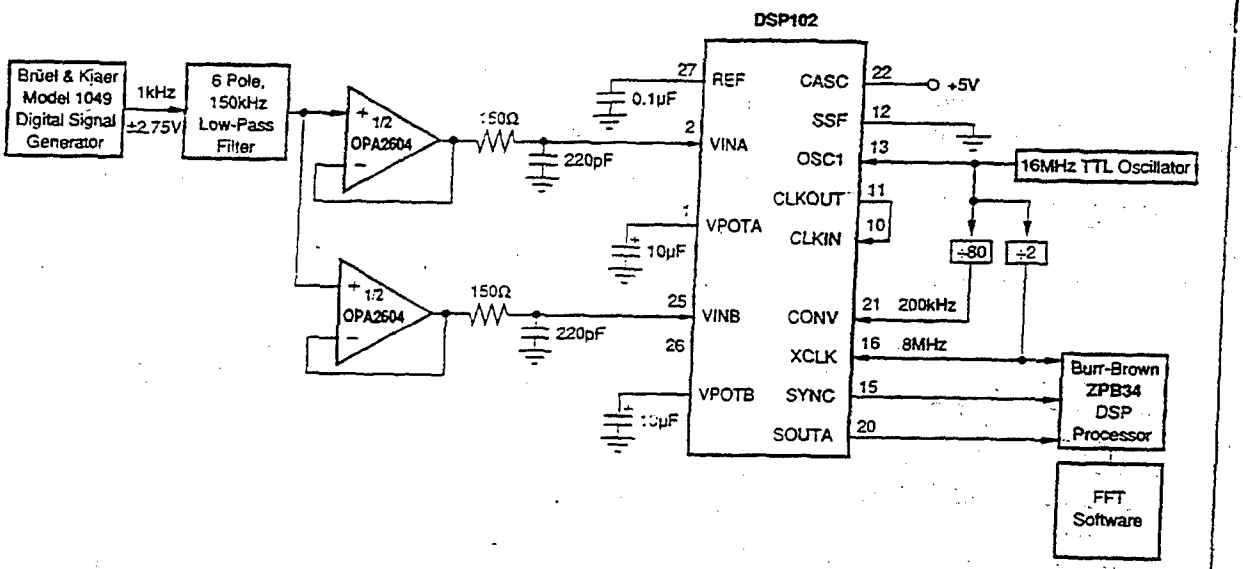


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
e	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	
eB	.600	.700	15.24	17.78
L	.115	.200	2.91	5.08

NOTES:
(1) Not JEDEC Standard.
(2) Controlling dimension: INCH.
(3) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(4) Dimensions A, A_1 and L are measured with package seated in JEDEC Seating Plane Gauge GS-3.
(5) D and E_1 does not include mold flash. Mold flash shall not exceed .010 inches, 0.25mm.
(6) eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

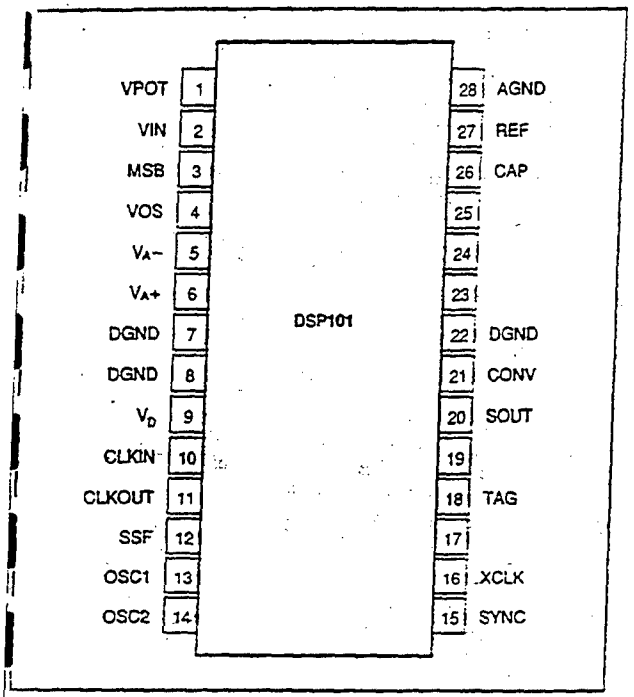
TYPICAL DSP102 FFT SETUP



ABSOLUTE MAXIMUM RATINGS

V_A+ to Analog Common	+7V
V_A- to Analog Common	–7V
V_D to Digital Common	+7V
Analog Common to Digital Common	±1V
Control Inputs to Digital Common	–0.5 to V_D + 0.5V
Analog Input Voltage	±5V
Maximum Junction Temperature	150°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}, Plastic DIP	50°C/W

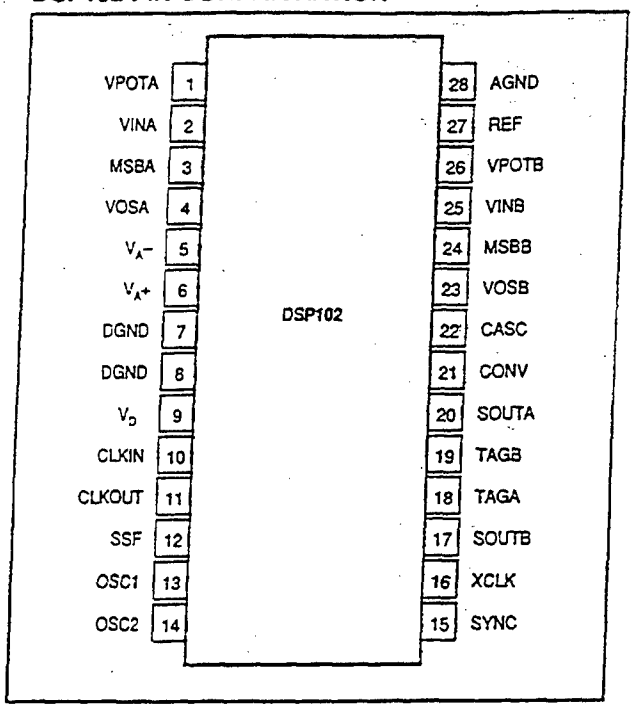
DSP101 PIN CONFIGURATION



DSP101 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	VPOT	Trim Reference Out. 10µF Tantalum to AGND.
2	VIN	Analog In.
3	MSB	MSB Adjust In.
4	VOS	VOS Adjust In.
5	V_A-	–5V Analog Power.
6	V_A+	+5V Analog Power.
7	DGND	Digital Ground.
8	DGND	Digital Ground.
9	V_D	+5V Digital Power.
10	CLKIN	Conversion Clock In.
11	CLKOUT	Conversion Clock Out. Can drive multiple DSP101/DSP102s to synchronize conversion.
12	SSF	Select Synch Format In. If HIGH, SYNC will be active High. If LOW, SYNC will be active Low. See timing diagram (Figure 1).
13	OSC1	Oscillator Point 1 Input/External Clock In. If using external clock, drive with 74HC logic levels. Connect to DGND if not used.
14	OSC2	Oscillator Point 2 Output. Provides drive for crystal oscillator. Make no electrical connection if using external clock.
15	SYNC	Data Synchronization Out. Active High when SSF is HIGH; active Low when SSF is LOW.
16	XCLK	Data Transfer Clock In.
17		No Internal Connection.
18	TAG	User Tag In. Data clocked into this pin is appended to the conversion results on SOUT. See timing diagram (Figure 1).
19		No Internal Connection.
20	SOUT	Serial Data Out. MSB first, Binary Two's Complement format.
21	CONV	Convert Command In. Falling edge puts converter into hold state, initiates conversion, and transmits previous conversion results to DSP IC with appropriate SYNC pulse.
22	DGND	Digital Ground.
23		No Internal Connection.
24		No Internal Connection.
25		No Internal Connection.
26	CAP	Bypass Capacitor. 10µF Tantalum to AGND.
27	REF	Reference Bypass. 0.1µF Ceramic to AGND.
28	AGND	Analog Ground.

DSP102 PIN CONFIGURATION



ORDERING INFORMATION

MODEL	NUMBER OF CHANNELS	SIGNAL-TO-(NOISE + DIST.) RATIO dB min
DSP101JP	1	83
DSP101KP	1	86
DSP102JP	2	83
DSP102KP	2	86

DSP102 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	VPOTA	Channel A Trim Reference Out. 10µF Tantalum to AGND.
2	VINA	Channel A Analog In.
3	MSBA	Channel A MSB Adjust In.
4	VOSA	Channel A VOS Adjust In.
5	V_A-	–5V Analog Power.
6	V_A+	+5V Analog Power.
7	DGND	Digital Ground.
8	DGND	Digital Ground.
9	V_D	+5V Digital Power.
10	CLKIN	Conversion Clock In.
11	CLKOUT	Conversion Clock Out. Can drive multiple DSP101/DSP102s to synchronize conversion.
12	SSF	Select Synch Format In. If HIGH, SYNC will be active High. If LOW, SYNC will be active Low. See timing diagram (Figure 1).
13	OSC1	Oscillator Point 1 Input / External Clock In. If using external clock, drive with 74HC logic levels. Connect to DGND if not used.
14	OSC2	Oscillator Point 2 Output. Provides drive for crystal oscillator. Make no electrical connection if using external clock.
15	SYNC	Data Synchronization Out. Active High when SSF is HIGH; active Low when SSF is LOW.
16	XCLK	Data Transfer Clock In.
17	SOUTB	Channel B Serial Data Out. MSB first, Binary Two's Complement format.
18	TAGA	Channel A User Tag In. Data clocked into this pin is appended to the conversion results of SOUTA. See timing diagram (Figure 1).
19	TAGB	Channel B User Tag In. Data clocked into this pin is appended to the conversion results of SOUTB. See timing diagram (Figure 1).
20	SOUTA	Channel A Serial Data Out. MSB first, Binary Two's Complement format. If CASC is HIGH, 32 bits of data output, with first 16 bits being Channel A data.
21	CONV	Convert Command In. Falling edge puts converter into hold state, initiates conversion, and transmits previous conversion results to DSP IC with appropriate SYNC pulse.
22	CASC	Select Cascade Mode In. If HIGH, DSP102 transmits a 32-bit word on SOUTA, with the first 16 bits being data on Channel A. If LOW, DSP102 transmits data for both channels simultaneously.
23	VOSB	Channel B VOS Adjust In.
24	MSBB	Channel B MSB Adjust In.
25	VINB	Channel B Analog In.
26	VPOTB	Channel B Trim Reference Out. 10µF Tantalum to AGND.
27	REF	Reference Bypass. 0.1µF Ceramic to AGND.
28	AGND	Analog Ground.

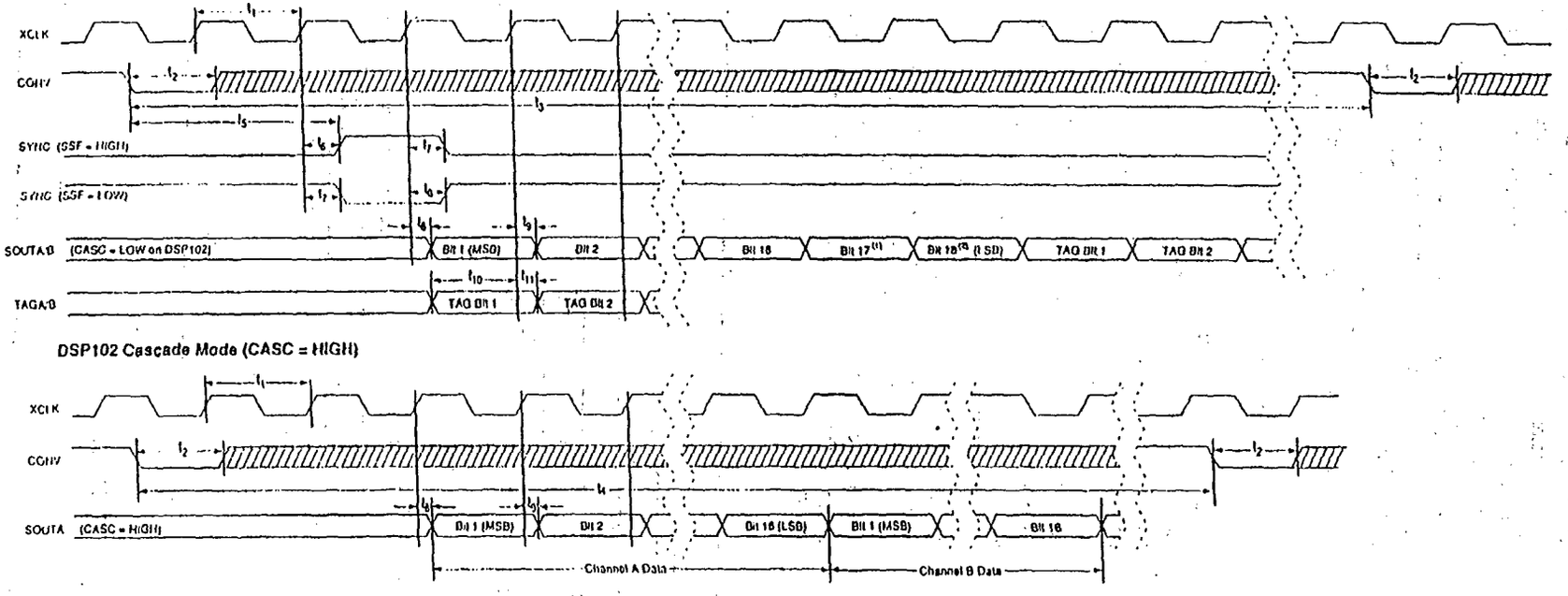
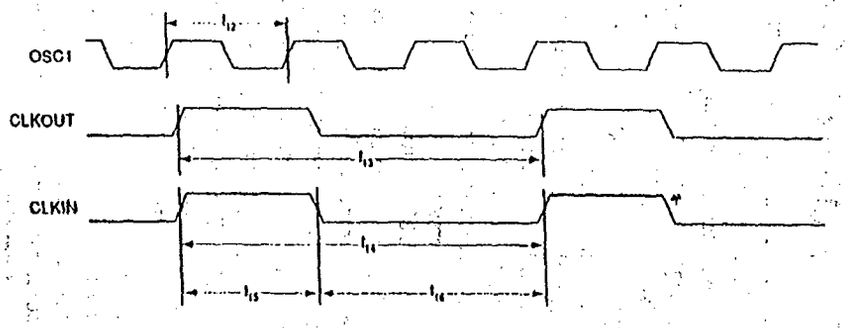


FIGURE 1. DSP101 and DSP102 Timing.

SYMBOL	DESCRIPTION (C_L = 50pF)	MIN	MAX	UNITS
t_1	XCLK period. Duty Cycle 50% ±10%	83		ns
t_2	Convert Command LOW Time	50		ns
t_3	Convert Period (CASC = LOW on DSP102)	24		t_1
t_4	Convert Period (CASC = HIGH on DSP102)	40		t_1
t_5	SYNC Active Delay after Convert Falling Edge	t_1 +40	2 t_1	ns
t_6	SYNC LOW to HIGH Delay from XCLK Rising		15	ns
t_7	SYNC HIGH to LOW Delay from XCLK Rising		15	ns
t_8	SOUTA/B Data Valid Delay from XCLK Rising		15	ns
t_9	SOUTA/B Data Valid After from XCLK Rising	10		ns
t_{10}	TAGA/B Data Setup before XCLK Rising	20		ns
t_{11}	TAGA/B Data Hold after XCLK Rising		0	ns
t_{12}	OSC1 Period.(2) Duty Cycle 50% ± 10%	62	667	ns
t_{13}	CLKOUT Period. Duty Cycle 33% ± 10%	3 t_{12}		ns
t_{14}	CLKIN Period. Duty Cycle 33% ± 20%	186	2000	ns
t_{15}	CLKIN HIGH	62	1050	
t_{16}	CLKIN LOW	84	1340	

Conversion Clock Timing (2)



NOTES: (1) When using a DSP IC in a 16-bit mode, these data bits will be ignored by the processor. (2) f_{OSC1} must be at least 72 times faster than the conversion rate. (t_3, $t_4 \geq 72\ t_{12}$)

THEORY OF OPERATION

The DSP101 and DSP102 are sampling analog-to-digital converters optimized for handling dynamic signals. They have complete logic interface circuitry for ease of use with standard digital signal processing ICs, and transmit data words in a serial stream. The successive approximation conversion architecture is combined with an inherently sampling switched capacitor array to provide maximum user flexibility over sampling and conversion timing.

The DSP101 and DSP102 are pipelined internally. When the user gives a convert command at time (t), two actions are initiated. First, the internal sample/holds are switched to the hold state, and a conversion cycle is initiated. At the same time, the DSP101 or DSP102 transmits a synchronization pulse and starts shifting out the conversion results from the previous convert command at (t-1) using the system bit clock. The data from the conversion at time (t) is shifted out of the converter after the next convert command is received.

Both the DSP101 and the DSP102 are 18-bit A/Ds internally. When the DSP IC is programmed to accept 16-bit word lengths, the processor will ignore the last two data bits transmitted from the DSP101 or DSP102. A Cascade Mode on the DSP102 can be invoked to transmit data for both conversion channels over a single serial line as a 32-bit word. In this mode, the first 16 bits of data transmitted after the Sync pulse contain data from channel A, followed by 16 bits of information from channel B, allowing a single 32-bit word to contain data for both channels.

A unique Tag feature allows additional digital data to be appended to the conversion results, so that a single data word contains conversion results plus other signal information, such as gain settings or multiplexer channel settings in front of the converter.

The DSP101 and DSP102 are high-resolution A/D converters complete with sampling capability and on-board references. They can acquire and convert analog signals at up to a 200kHz sampling rate. Both operate from ±5V supplies, and have full-scale analog input ranges of ±2.75V.

BASIC OPERATION

Figure 2 shows the minimum connections required to operate the DSP101. The falling edge of a convert command on pin 21 puts the internal sampling capacitor array into the hold state. The falling edge on pin 21 also starts the process to initiate a conversion and transmit data from the previous conversion, synchronizing both appropriately to the 10MHz clock input on pin 13. Figure 1 shows the timing relationship between the convert command, the output data, and the synchronization pulse.

In this basic system, the 10MHz clock is used both to generate a 3.33MHz conversion clock and as the data transfer bit clock for outputting data. Per Figure 1, there must be at least 72 clock pulses on pin 13 between convert commands, so that this circuit can sample and convert at up to 138kHz.

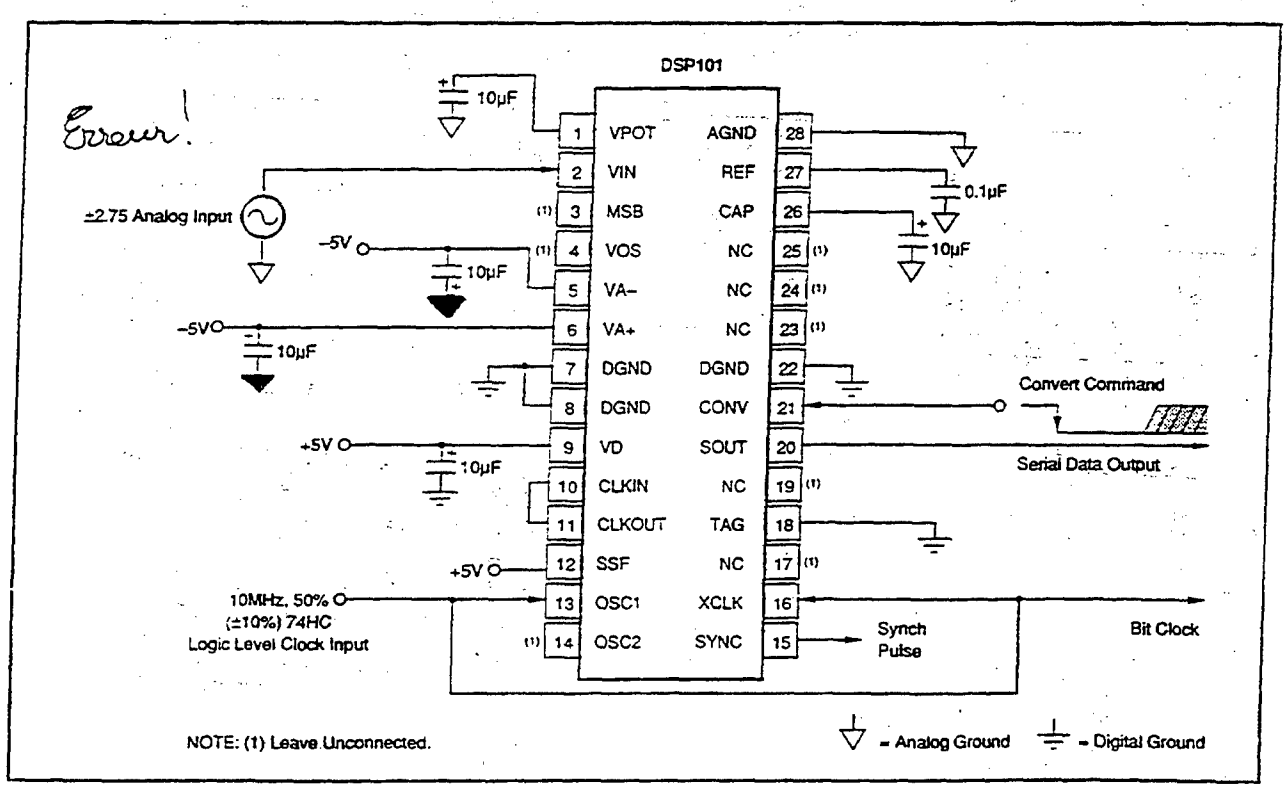


FIGURE 2. DSP101 Basic Operation.

The convert command at pin 21 causes a Sync pulse to be output on pin 15, followed by the data from the previous conversion output on pin 20. The Sync pulse will be HIGH for one bit clock cycle, since pin 12 is tied HIGH. (A LOW Sync pulse will be output on pin 15 if pin 12 is tied LOW.) Data is serially transmitted in an MSB-first data stream, in Binary Two's Complement format. Both the Sync pulse (pin 15) and the data stream (pin 20) are synchronized to the bit clock (at pins 13 and 16), with the timing relationships shown in Figure 1.

After the 18 bits of data from the previous conversion have been transmitted, pin 20 will continue to clock out LOWs until a new convert command restarts the process, since pin 18 (the Tag input) is grounded. If pin 18 is tied HIGH, pin 20 will clock out HIGHs between conversion cycles.

CONVERSION

A falling edge on pin 21 (CONV) puts the internal sampling capacitors in the hold state with minimum aperture jitter, initiates a conversion synchronized to the conversion clock, and outputs the data from the previous conversion with an appropriate Sync pulse. On the DSP102, a single convert command simultaneously samples both channels. The timing relationship between the convert command, Sync and the output data is shown in Figure 1. Both Sync and the output data are synchronized to XCLK, the system bit clock. Following a convert command falling edge, pin 21 must be held LOW at least 50ns.

Convert commands can be sent to the DSP101 and DSP102 completely asynchronous to other clocks in the system. This allows external events to be used to trigger conversions.

From Figure 1, it can be seen that two different clocking conditions must be considered in determining the minimum acceptable time between convert commands. First, there need to be a minimum of 24 XCLK periods between convert commands, to allow internal synchronization and transmission of Sync and the data. (In the Cascade Mode on the DSP102, there need to be at least 40 XCLK periods between convert commands, to allow transmission of the 32-bit data words.) When used with DSP processors programmed for data words longer than 16-bits, the transmission time to the processor may determine the minimum time between convert commands.

The second limitation on convert commands is the requirement that the internal analog-to-digital converter be given enough time to complete a conversion, shift the data to the output register, and acquire a new sample. This condition is met by having a minimum of 24 CLKIN periods between convert commands, or a minimum of 72 clock cycles on OSC1, if it is used to generate the conversion clock (CLKOUT driving CLKIN).

SIGNAL ACQUISITION

After a conversion is completed, the DSP101 or DSP102 will switch back to the sampling mode. With at least 24 CLKIN periods between convert commands, the A/D will have had sufficient time to acquire a new input sample to full rated accuracy.

DATA FORMAT AND INPUT LEVELS

The DSP101 and DSP102 output serial data, MSB first, in Binary Two's Complement format. In the Cascade Mode on the DSP102, the serial data will first contain 16 bits of data for channel A, MSB-first, followed by channel B data, again MSB-first. The analog input levels that generate specific output codes are shown in Table I.

As with all standard A/Ds, the first output transition will occur at an analog input voltage 1/2 LSB above negative full scale (–2.75V + 1/2 LSB) and the last transition will occur 3/2 LSB below positive full scale (+2.75V – 3/2 LSB.) See Figure 3.

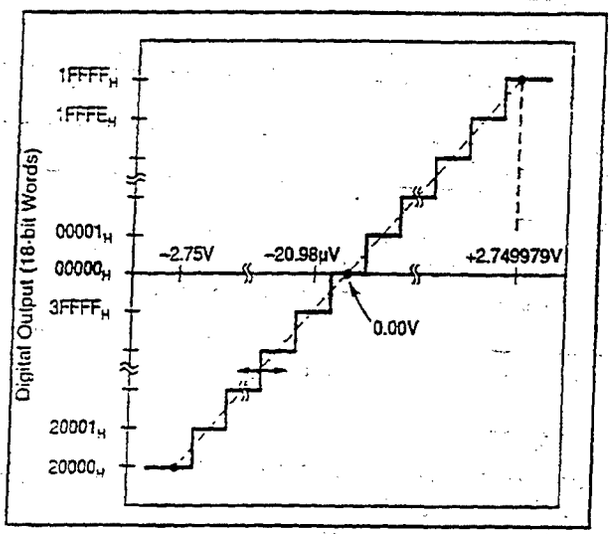


FIGURE 3. Analog Input to Digital Output Diagram.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT (BINARY TWO'S COMPLEMENT) BINARY CODE	16-BIT WORDS (HEX)	18-BIT WORDS (HEX)
Least Significant Bit (LSB = $\frac{5.5V}{2^n}$)				
16-bit Words	84µV			
18-bit Words	21µV			
Input Range	±2.75V			
+ Full Scale (2.75V–1LSB)	+2.749916V +2.749979V	011...111	7FFF	1FFFF
Bipolar Zero (Midscale)	0V	000...000	0000	00000
One LSB below Bipolar Zero	–84µV –21µV	111...111	FFFF	3FFFF
– Full Scale	–2.75V	100...000	8000	20000

TABLE I. Ideal Input Voltage vs Output Code.

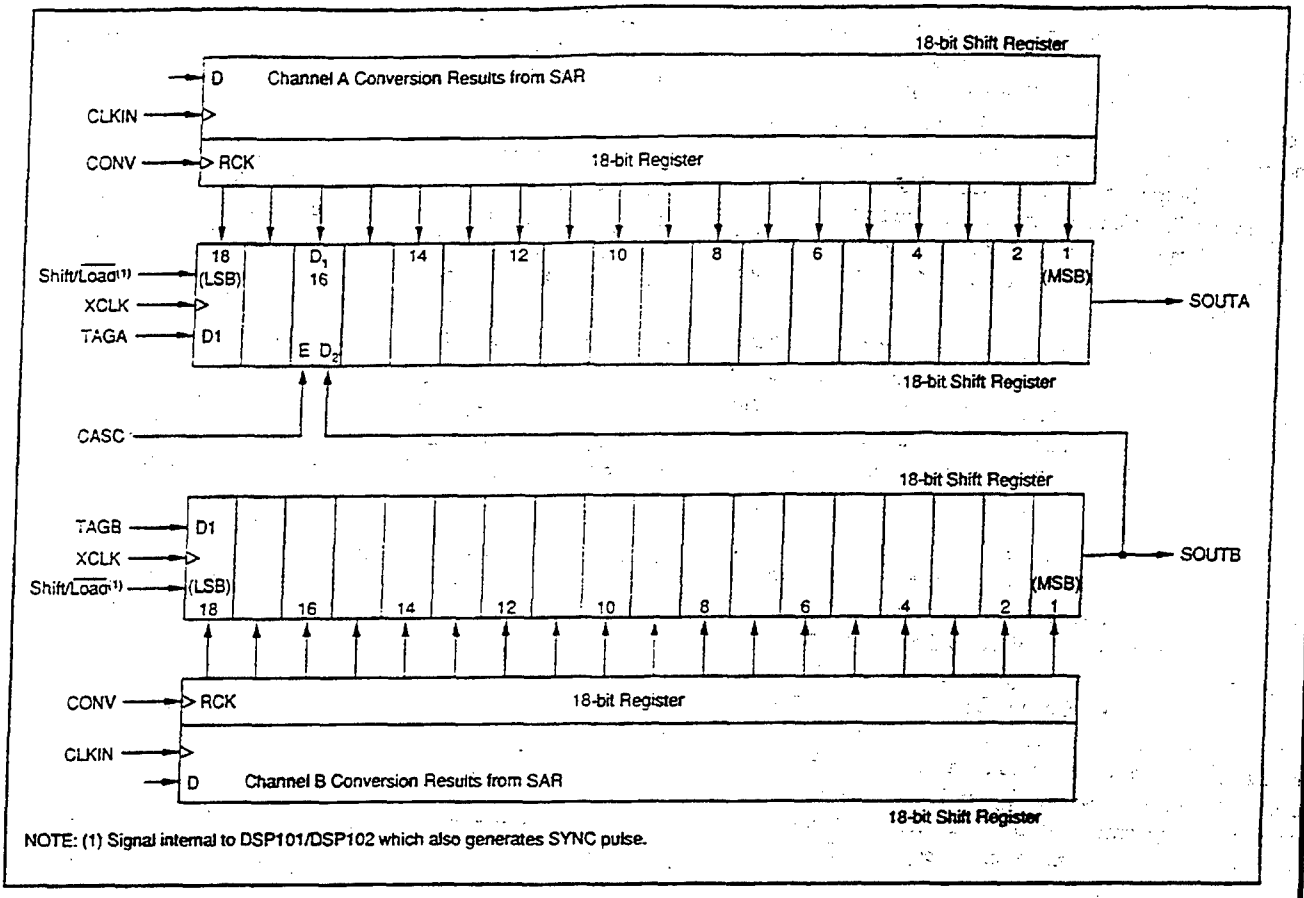


FIGURE 4. Output Structure of DSP102.

DATA TRANSFER

The internal A/Ds generate 18 bits of data, transmitting the data MSB first. When read by a DSP IC programmed to accept 16 bits of data, the first 16 MSB bits of data from the DSP101, or each channel of the DSP102, will be shifted into the processor's input shift register, and the last two least significant bits of data from the A/D will be ignored, although they will still be present on the serial data line. When the DSP processor is programmed to accept words of more than 16-bit length (typically 24-bit or 32-bit), the DSP101 and DSP102 will transmit the full 18-bit conversion results, after which the information input on the TAG input (or TAGA and TAGB on the DSP102) will be appended to the output word. (See Tag Feature below.)

In the Cascade Mode, the DSP102 will first transmit the 16 MSBs from channel A, followed by the full 18-bits from channel B, although DSP processors programmed to accept 32 bits of data will ignore the final two bits of information on Channel B. See the DSP102 Cascade Mode section below for details of the Cascade mode.

DATA SYNCHRONIZATION

A convert command both initiates a conversion and starts the process for transmitting data from the previous conversion. Convert commands can come at any time, completely asynchronous to the conversion clock or the bit clock, and the conversion clock may also be independent of the bit clock. The DSP101 and DSP102 internally synchronize the output data, Sync pulse, and Tag inputs to the bit clock.

While the convert command, conversion clock and bit clock can be asynchronous, system performance is usually enhanced by synchronizing all of them to a system master clock, whenever the application permits. This minimizes changes in digital loads and currents when the critical S/H transition and A/D bit decisions are occurring. Within the DSP101 and DSP102 themselves, running asynchronous convert commands, conversion clocks and bit clocks typically degrades performance only several dB, as shown in the various typical performance curves, but the system board design can easily have more effect.

When a convert command is received, the internal logic generates an appropriate Sync pulse, synchronized to XCLK, as shown in Figure 1. The output Sync pulse will be active High or active Low depending on whether a HIGH or a LOW, respectively, is input at SSF (pin 12).

The convert command also causes the conversion results from the previous conversion to be loaded into the output shift register, synchronous to XCLK. Figure 4 shows the operation of the internal data shift registers on the DSP102. The DSP101 is basically similar, but includes only the top of the figure, showing the SOUTA path.

During the internal successive approximation conversion process, the conversion results are shifted into the input shift registers of the output stage on the DSP102. A new convert command latches that data into the 18-bit parallel latches shown. The internal signal that also generates the Sync pulse, labeled "Shift/Load" in Figure 4, synchronously loads the conversion data into the output shift register on the rising edge of XCLK. The conversion results are then clocked out of the shift register on subsequent rising edges of XCLK.

DATA TRANSFER CLOCK

XCLK is the data transfer clock, or bit clock, for the system, and is an input for the DSP101 or DSP102. This input is TTL- and 74HC-level compatible. The serial data and SYNC outputs are synchronized internally to this clock, with data valid on the rising edge of XCLK, per the timing shown in Figure 1. Data input on pin 18 (TAG) on the DSP101, or on pins 18 and 19 on the DSP102 (TAGA and TAGB), will be clocked into the output shift register on the rising edge of XCLK, as discussed in the Tag Feature section.

CONVERSION CLOCK

The analog-to-digital converter sections in the DSP101 and DSP102 were designed to provide accurate conversions under worst case conditions of supplies, temperatures, etc. In order to achieve a full 200kHz sampling capability, they were designed to use a 33% duty cycle conversion clock (CLKIN on pin 10) as shown in Figure 1. The clock is LOW long enough for internal analog circuitry to settle sufficiently between bit decisions to insure rated accuracy. Bit decisions in the A/D are then made on the rising edge of CLKIN.

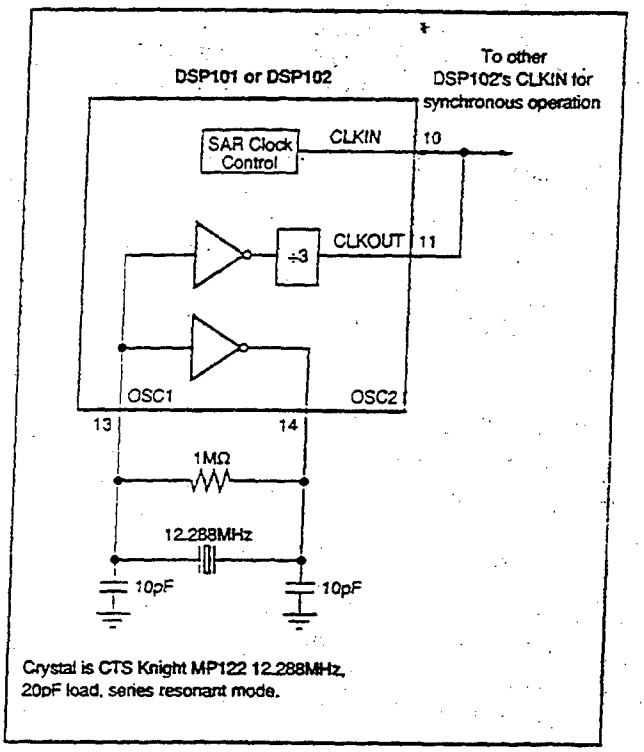


FIGURE 5. DSP101 or DSP102 Conversion Clock Circuit.

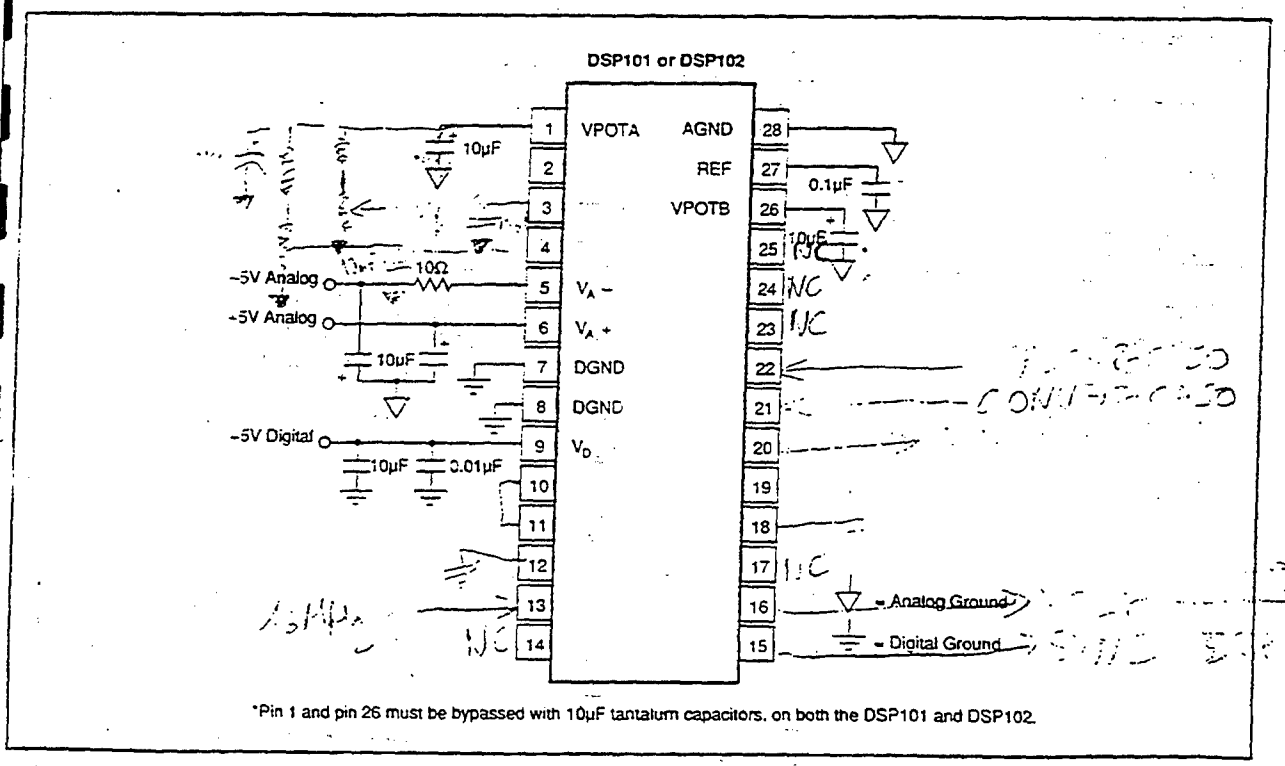


FIGURE 6. DSP101 or DSP102 Power Supply Connections.

When a convert command is received, the DSP101 or DSP102 immediately switches the sampling capacitors to the hold state, and then internally gates the conversion clock to the A/D appropriately. Allowing a minimum of 24 CLKIN pulses between conversions insures that there is sufficient time for complete, accurate conversions, and allows the input sampling capacitor to fully acquire the next sample, regardless of the timing between the convert command and CLKIN.

In most applications, CLKIN (pin 10) can be driven from a 50% duty cycle clock without performance degradation. During characterization of the DSP101 and DSP102, the performance of a number of parts was measured under various conditions with a 4.8MHz, 50% duty cycle input to CLKIN at a full 200kHz conversion rate without noticeable degradation.

OSCILLATOR INPUTS AND CLKOUT

The DSP101 or DSP102 can generate a 33% duty cycle conversion clock output on CLKOUT (pin 11). This is accomplished by dividing by three a clock from either an external 74HC-level clock or from a crystal oscillator. CLKOUT can deliver ±2mA, and can be used to drive multiple DSP101 or DSP102 CLKINs. See Figure 1 for the timing relationship between OSC1 and CLKOUT.

To use an external 74HC-level clock, drive the clock into OSC1 (pin 13), and leave OSC2 (pin 14) unconnected.

To use a crystal oscillator to generate the conversion clock, refer to Figure 5. Connect the oscillator between OSC1 and OSC2. OSC2 provides the drive for the crystal oscillator. This pin cannot be used elsewhere in the system.

If CLKOUT is not used, both it and OSC2 should be left unconnected, and OSC1 should be grounded.

TAG FEATURE

Figure 4 shows the implementation of the TAG feature on the DSP101 and DSP102. When a convert command is received, the internal Shift/Load signal loads conversion result data into the output shift register synchronous to XCLK. Between convert commands, the information input on TAG (on the DSP101) or on TAGA and TAGB (on the DSP102) will be clocked into the output shift register on the rising edges of XCLK. Since this is an 18-bit shift register, the data input on the Tag lines will be output on SOUT (DSP101) or SOUTA and SOUTB (DSP102) delayed by 18 bit clocks.

The Tag Feature can be used in various ways. The Tag inputs can be tied HIGH or LOW to differentiate between two converters in a system. As discussed in the Applications section below, the Tag feature can be used to append to the serial output data word information on multiplexer channel address, or other digital data related to the input signal (such as the setting on a programmable gain amplifier.) Another option would be to daisy-chain multiple DSP101 or DSP102 converters, linking the serial output of one to the Tag input of the next. This can simplify the transmission of data from multiple A/Ds over a single optical isolation channel.

DSP102 CASCADE MODE

If pin 22 (CASC) is tied HIGH, the DSP102 will be in the Cascade Mode. In this mode, when a convert command is received, the DSP102 will transmit a 32-bit data word on pin

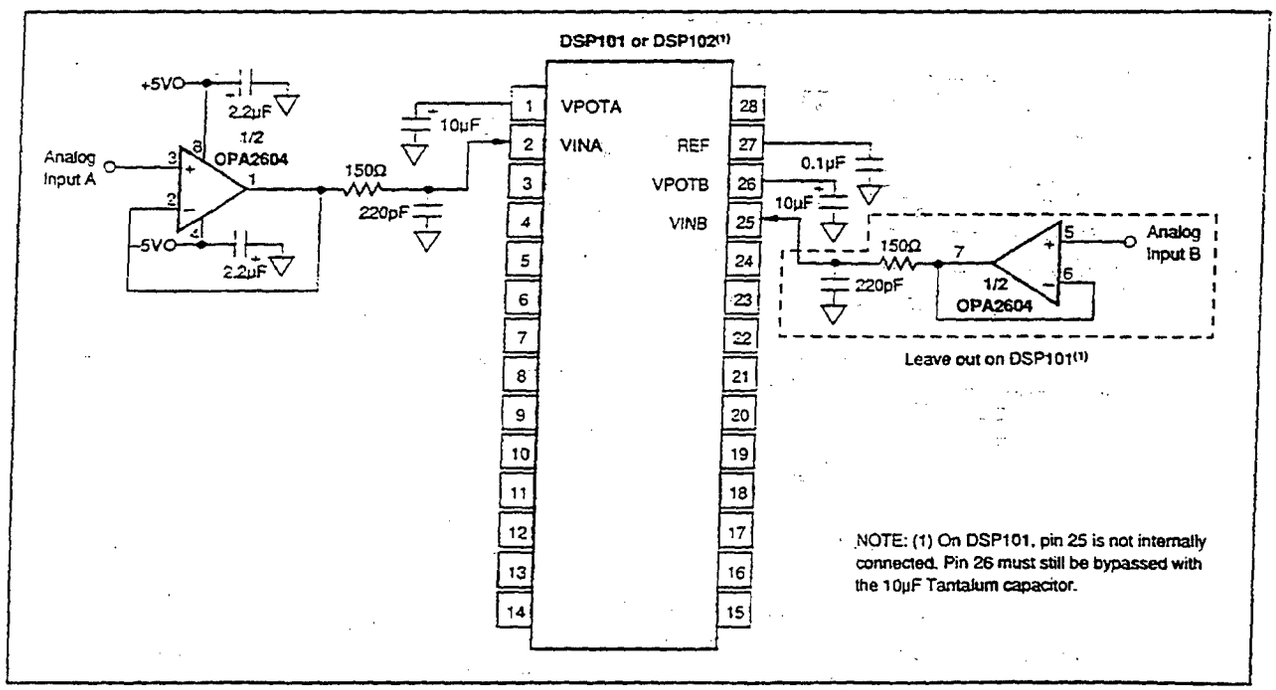


FIGURE 7. DSP101 or DSP102 Input Buffering.

20 (SOUTA) containing data for both input channels in two 16-bit words. Referring to Figure 1, the first 16 bits of data will be the results for channel A, followed by 16 bits of information for channel B. The data will be transferred MSB first. A convert command at time (t) will initiate the transmission of the results of the conversion initiated at time (t – 1).

From the descriptions above of the internal shift registers shown in Figure 4, it can be seen that the DSP102 in the Cascade Mode actually continues to shift out data after the 32nd bit of the data word. The next two bits clocked out will be the last two data bits from the full 18-bit conversion on channel B, after which the information output on SOUTA will be the information clocked into TAGB 35 bit clock cycles earlier.

In the Cascade mode on the DSP102, SOUTB will still output channel B conversion data and tag data as usual.

ANALOG PERFORMANCE

LINEARITY

The DSP101 and DSP102 are optimized for signal processing applications with wide dynamic range requirements. Linearity is trimmed for best performance in the range around 0V, which is critical for handling low amplitude signals. The DSP101 and DSP102 typically have integral and differential non-linearity below ±0.003% in the input range of ±0.7V, with there being no missing codes at the 14-bit level in this range. Over the full ±2.75V input range, the largest non-linearities are centered around the bit #2 transition points at +1.375V and –1.375V levels.

NOISE AND BIPOLAR ZERO ERROR

The equivalent input noise and bipolar zero error of the DSP101 and DSP102 is shown in the typical performance section for both channels on a DSP102. The inputs to both channels were grounded, and the results of 5,000 conversions was recorded. The data shown is binned at the 16-bit level. The noise results from all sources in the circuit, including clocks, reference noise, etc.

In a theoretically ideal converter with no offset and no noise, the results of all 5,000 conversion for each channel would lie in the bin corresponding to bipolar zero, code 0000. The typical DSP101 or DSP102 will have offset errors in the range of 1 to 2mV, and the two channels on the DSP102 will be matched closer than 2mV. The DSP102 shown in the typical performance section has the worst offset, –0.8mV, on channel A, with channel B being less than 1mV different, and the three sigma noise on either channel being less than 250µV.

INPUT BANDWIDTH

From the typical performance curves, it can be seen that there is very little degradation in Signal-to-(Noise + Distortion) for input signals up to 100kHz. The wideband sampling input typically maintains a 60dB Signal-to-(Noise + Distortion) Ratio undersampling 500kHz input signals.

LAYOUT CONSIDERATIONS

Because of the high resolution, linearity and speed of the DSP101 and DSP102, system design problems such as ground path resistance, contact resistance and power supply quality become very important.

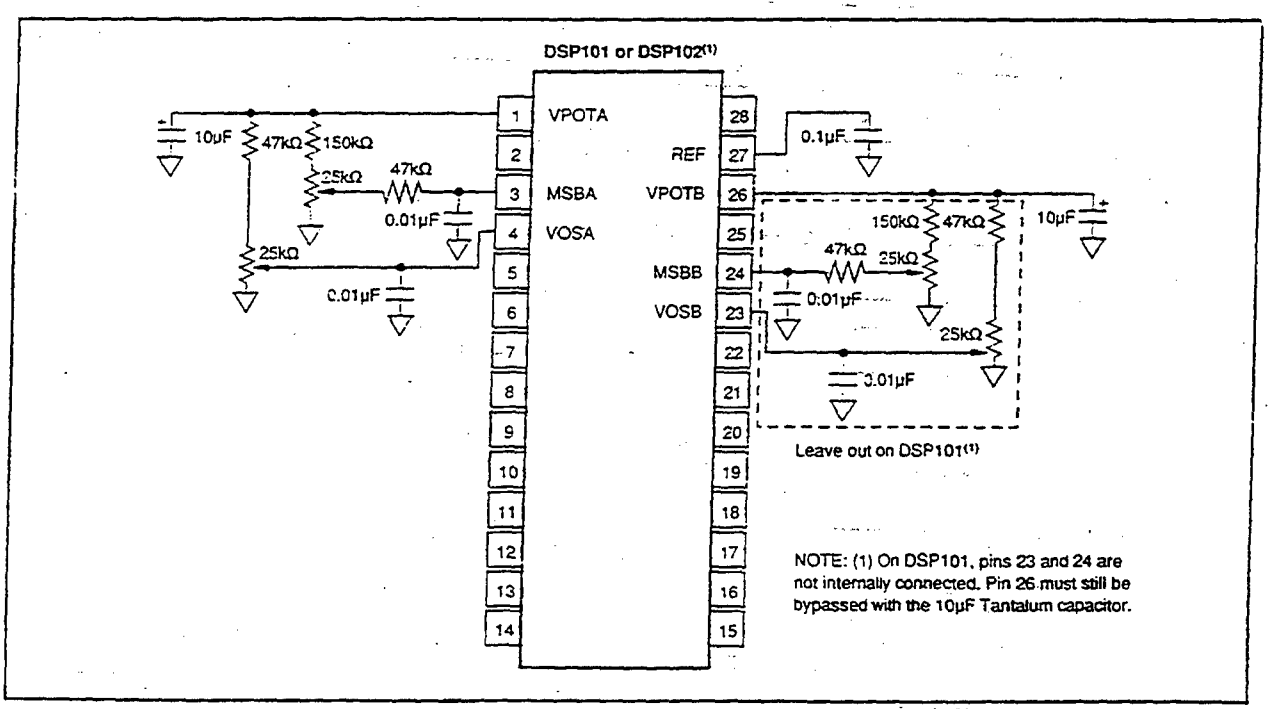


FIGURE 8. DSP101 or DSP102 Optional MSB and Offset Adjust.

Optimal dynamic performance is achieved by soldering the parts directly into boards, to keep the A/Ds as close as possible to ground. The use of sockets will often degrade AC performance. Zero-Insertion-Force sockets are particularly poor because longer lead lengths create inductance.

Short traces on the board, and bypass capacitors as close as possible to the A/D, will further improve dynamic performance.

GROUNDS

To achieve the maximum performance from the DSP101 or DSP102, care should be taken to minimize the effect of changes in current flowing in the system grounds, particularly while bit decisions are being made in the successive approximation converter's comparator. Pin 28 (AGND) on both the DSP101 and the DSP102 is the most critical, and care should be taken to make this pin as close as possible to the same potential as the system analog ground.

Whenever possible, it is strongly recommended that separate analog and digital ground planes be used. With an LSB level of 84µV at the 16-bit level, and one-quarter of that at the 18-bit level, the currents switched in a typical DSP system can easily corrupt the accuracy of the A/Ds unless great care is taken to analyze and design for current flows.

POWER SUPPLY DECOUPLING

All of the supplies should be decoupled to the appropriate grounds using tantalum capacitors in parallel with ceramic capacitors, as shown in Figure 6. For optimum performance of any high resolution A/D, all of the supplies should be as clean as possible. If separate digital and analog supplies are available in a system, care should be taken to insure that the difference between the analog and the digital supplies is not more than 0.5V for more than a few hundred milliseconds, as may occur at power-up.

INPUT SIGNAL CONDITIONING

To avoid introducing distortion, the DSP101 and DSP102 analog inputs must be driven by a source with low impedance over the input bandwidth needed in the application. Op amps such as the NE5532 or Burr-Brown's OPA2604 work well over audio bandwidths. Figure 7 shows an appropriate input driver circuit. The 150Ω and 220pF shown on the input help reduce the dynamic load on the input signal conditioning amp in front of the A/D, since all switched capacitor array architectures exhibit fast changes in input current load as the input sampling switch is opened and closed. These dynamic changes in the load can affect any signal conditioning circuit at the input. Other R and C combinations can be

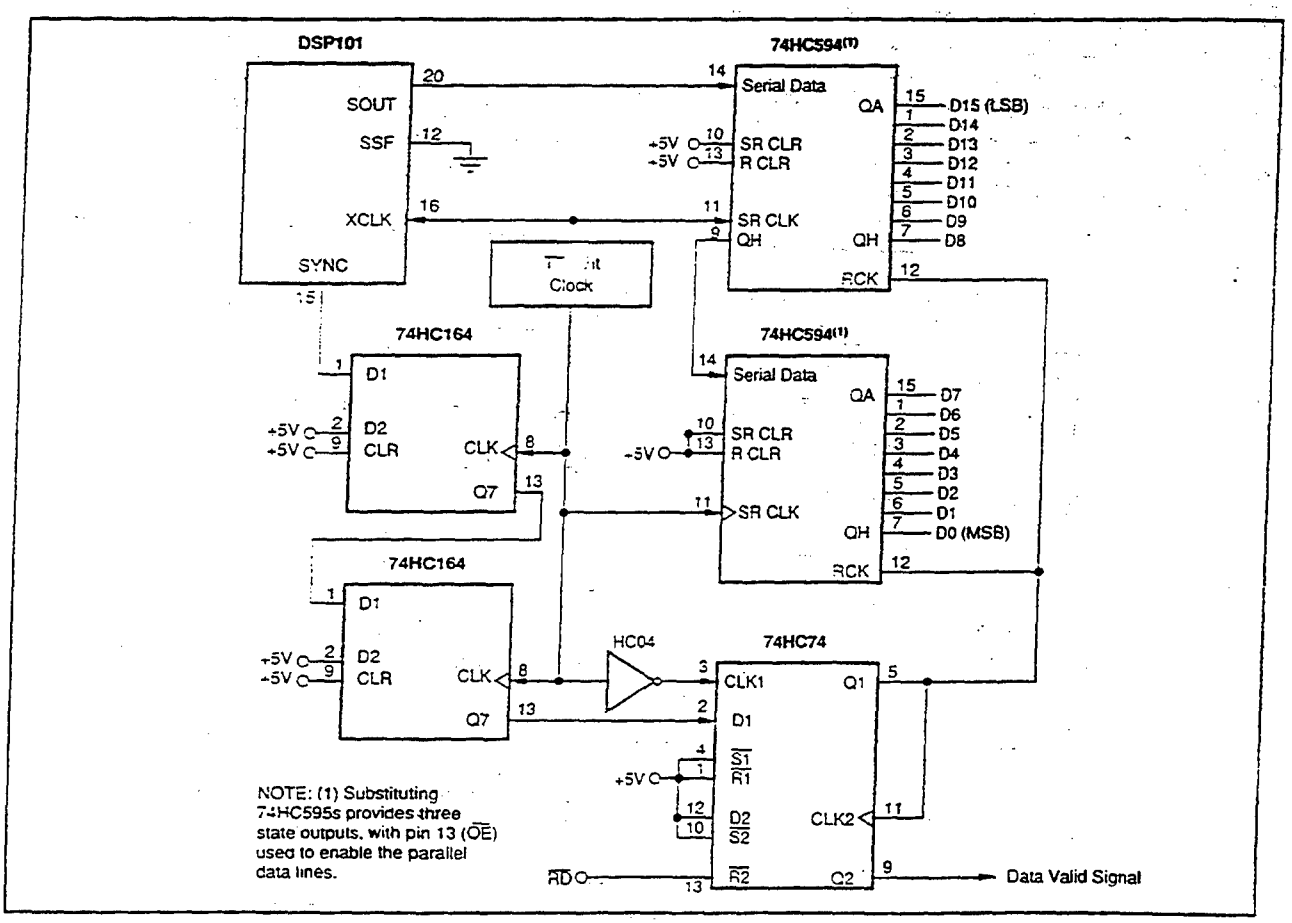


FIGURE 9. Driving a 16-bit Parallel Port from the DSP101.

used, but the resistor should not exceed 200Ω, or the output settling time of the signal conditioning amplifier may be too long.

EXTERNAL ADJUSTMENTS

All of the specifications for the DSP101 and DSP102, plus the typical performance curves, are based on the performance of these A/Ds without external trims. In most applications, external trims are not required.

OFFSET ADJUST

Where required by specific applications, offsets can be adjusted using Figure 8. When not adjusted, VOS (pin 4) on the DSP101, and VOSA (pin 4) and VOSB (pin 23) on the DSP102, should be left open. If these pins are connected to traces on the board, they should be bypassed to ground with 0.01µF capacitors, as close as possible to the A/D.

To trim offset, one alternative is to ground the analog input while converting continually. Then adjust the trimpot (on VOS for the DSP101, on VOSA and VOSB for the DSP102) until the output code is toggling between the codes FFFF and 0000 (Hex) at the 16-bit level (3FFFF and 00000 at the 18-bit level.) This will center the offset at 1/2 LSB below 0V, which is respectively –42µV or –10µV at the 16- and 18-bit levels.

The offset can also be adjusted by providing a sine wave to the A/D input. Using FFT, or even simple averaging of several thousand conversion results at a time, the trimpots can be adjusted until there is no DC offset of the signal.

Grounding the input, or providing the sine wave, as far in front of the A/D as possible allows offset from intervening signal conditioning components to be also corrected by this procedure.

MSB ADJUST

In most applications, adjustment of the Most Significant Bit weight will not be required. When not adjusted, MSB (pin 3) on the DSP101, and MSBA (pin 3) and MSBB (pin 24) on the DSP102, should be left open. If these pins are connected to traces on the board, they should be bypassed to ground with 0.01µF capacitors, as close as possible to the A/D.

MSB (pin 3) on the DSP101, and MSBA (pin 3) and MSBB (pin 24) on the DSP102, are internally connected to a resistor divider network that is used to laser-trim the weight of the MSB capacitor in the CDAC. These pins are nomi-

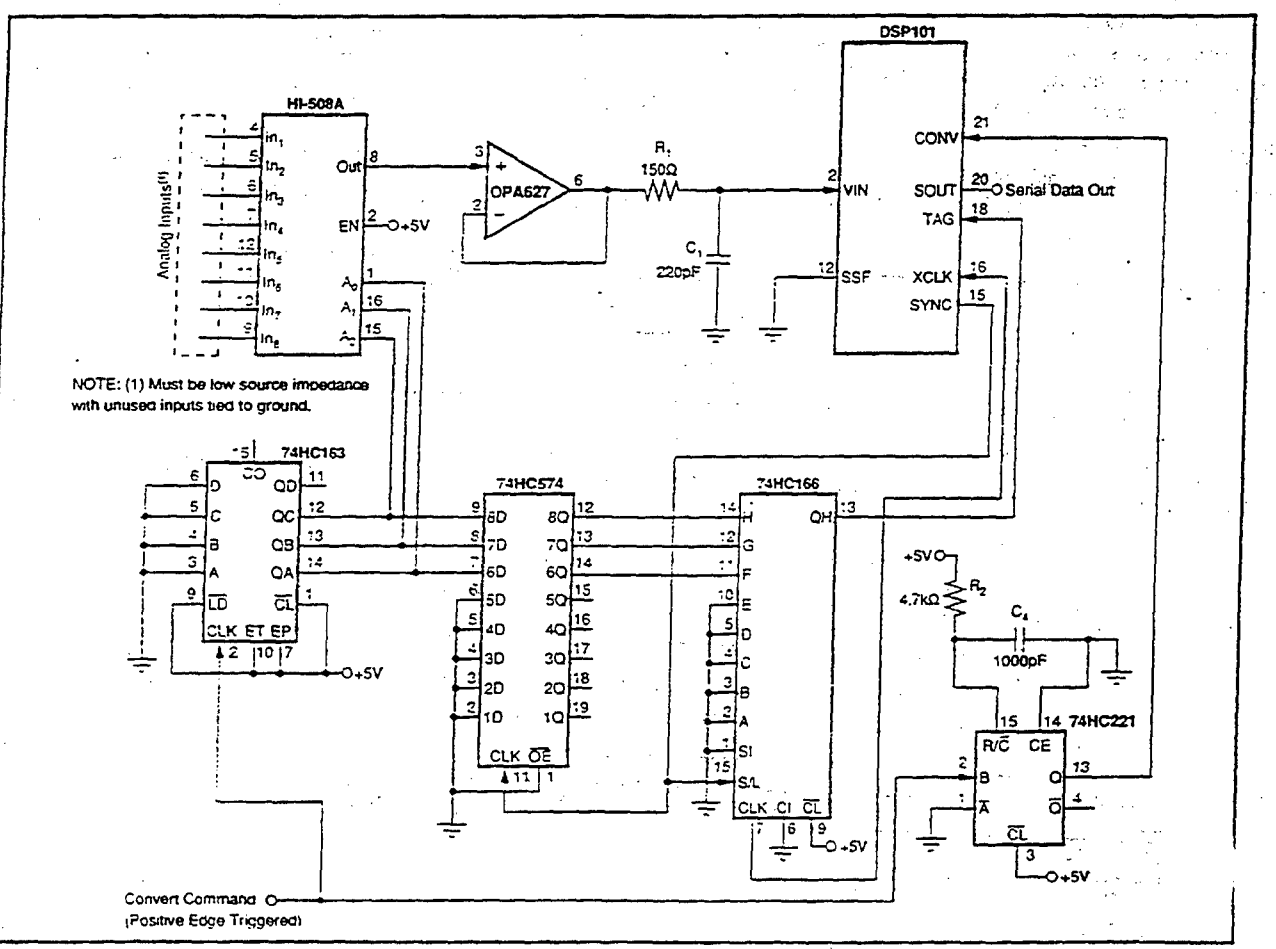


FIGURE 10. A Complete Eight-Channel Analog Input System Using the DSP202 and the HI-508A.

nally at +100mV after laser-trimming during manufacturing. They can handle external inputs up to about one diode drop below ground (–0.6V) before internal clamping circuitry is triggered.

Figure 8 shows an appropriate circuit for adjusting the weight of the most significant bit to minimize differential non-linearity at the critical major-carry transition. To adjust, provide a small amplitude sine wave to the selected A/D input pin while converting continually, and adjust for maximum Signal-to-(Noise + Distortion) ratio, using appropriate signal analysis software.

GAIN ADJUST

If circuit gain needs to be adjusted in hardware, rather than in system software, appropriate trimpots should be included in the analog signal conditioning section in front of the DSP101 or DSP102. No specific gain adjust circuitry is included in the parts.

APPLICATIONS

INTERFACING DSP101 TO PARALLEL PORTS

Figure 9 shows a circuit for converting the serial output data from the DSP101 into 16 bits of parallel data, within the timing constraints of the serial bit-stream from the DSP101. In many applications, this circuit can be easily incorporated into gate arrays or other programmed logic circuits already used in the system, since the extra gate count is not high.

This circuit adds an additional pipeline delay to the conversion data, so that the parallel data from a conversion at time (t) is valid one conversion cycle plus 17 XCLK clocks later (at t+1 plus 17 times XCLK). A convert command at time (t+1) generates a Sync and begins transmitting serial data from SOUT. The serial data is shifted into the 74HC594 shift registers, and Sync is shifted through the 74HC164 shift registers. The Q1 output of the 74HC74 dual D-type flip-flops clocks the conversion data into the output register of the 74HC594s, and triggers a data valid signal on its Q2 output. The user can then read the data at any time before the next conversion is started, and the Read signal will reset the data valid output from Q2.

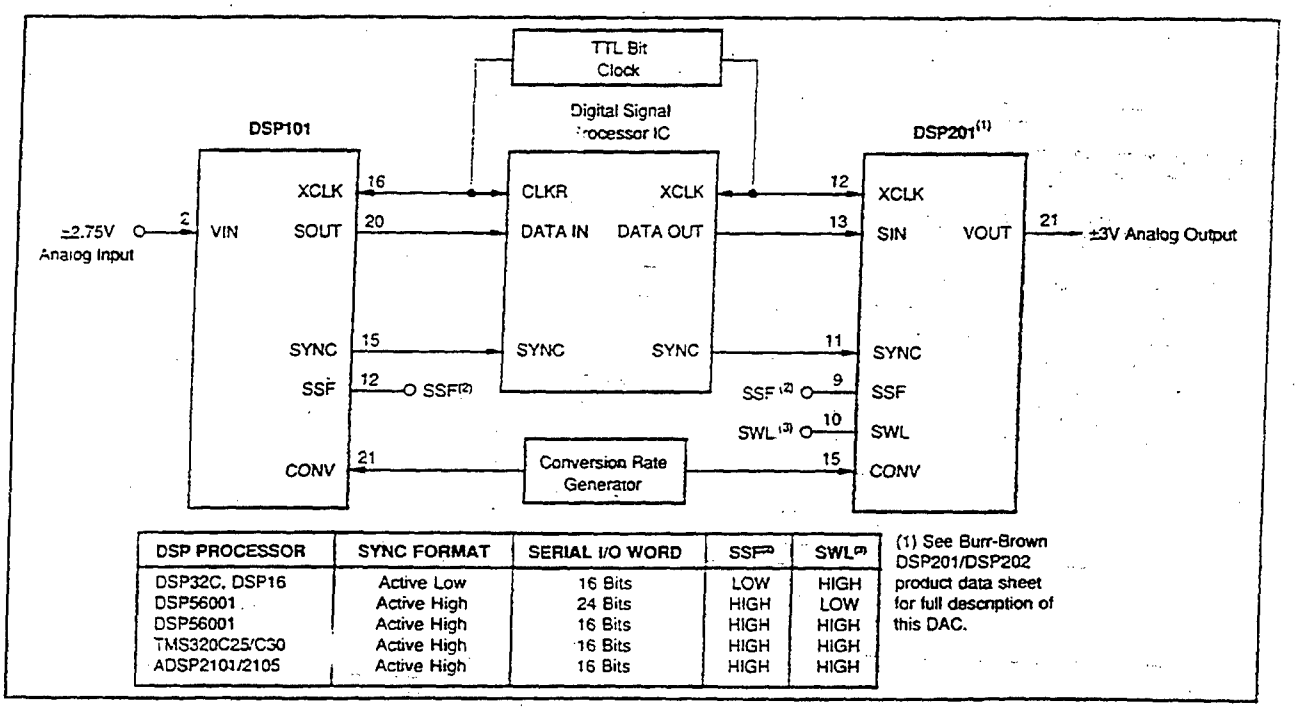
In many systems, galvanic isolation of signals is required. Using opto-couplers on the serial data lines in Figure 9 allows a fully isolated system to be built using a DSP101 and only three couplers across the barrier (for serial data, XCLK and SYNC.)

MULTIPLEXING INPUTS TO THE DSP101

Figure 10 shows a complete circuit for sequentially scanning eight analog input channels with a single DSP101, and using the Tag feature on the DSP101 to append the multiplexer channel address to the serial output conversion results.

The circuit in Figure 10 includes the required digital logic and timing logic. The 74HC163 counter provides the scan sequence to the Burr-Brown HI-508A analog multiplexer. In order to allow the HI-508A enough time to switch to the next channel and settle before the DSP101 begins a conversion, a 74HC221 one-shot introduces a 3µs delay for the DSP101 convert command input.

The Burr-Brown OPA627 provides a low impedance source for the DSP101, buffering it from the output impedance of



DSP PROCESSOR	SYNC FORMAT	SERIAL I/O WORD	SSF(2)	SWL(3)
DSP32C, DSP16	Active Low	16 Bits	LOW	HIGH
DSP56001	Active High	24 Bits	HIGH	LOW
DSP56001	Active High	16 Bits	HIGH	HIGH
TMS320C25/C30	Active High	16 Bits	HIGH	HIGH
ADSP2101/2105	Active High	16 Bits	HIGH	HIGH

(1) See Burr-Brown DSP201/DSP202 product data sheet for full description of this DAC.

FIGURE 11. Analog Input and Analog Output System.

the multiplexer. This unity-gain buffer minimizes distortion, taking full advantage of the resolution and bandwidth of the DSP101.

The 74HC574D register delays the multiplexer address data by one conversion before appending the channel data to the serial conversion results from the DSP101. This attaches the channel address to the correct conversion results. Since the channel scanning shown in Figure 10 is sequential, this delay latch could be left out and software could recognize that the time (t) conversion results have the MUX address from the time (t-1) conversion appended. However, for systems using non-sequential scan lists, this delay latch is essential to maintain the conversion data and channel address integrity.

The 74HC166 synchronous loading shift register loads the channel address tag data into the shift register on the rising edge of the bit clock, in conjunction with the Sync output of the DSP101. The channel address tag data is then clocked into the DSP101 Tag input (pin 18) by the bit clock, while the conversion data is clocked out the other end of the DSP101 shift register (discussed in another section of this data sheet.)

Figure 10 was developed and tested using a Burr-Brown ZPB34 DSP board, which contains an AT&T DSP32C, so that the SYNC output is programmed to be active LOW. The circuit needs to be modified for DSP processors from ADI, TI, and Motorola, which use active HIGH Sync pulses. For these processors, tie SSF (pin 12) on the DSP101 HIGH, and use a 74HC04 hex inverter to invert the Sync signal to the 74HC574 and 74HC166.

The same basic circuit can be duplicated to drive two channels in a DSP102, or can be easily modified for more or less than eight channels of analog input.

USING DSP101 AND DSP102 WITH TEXAS INSTRUMENTS DSP ICS

Figures 11 thru 17 show various ways to use the DSP101 and DSP102 with DSP ICs from the Texas Instruments TMS320Cxx series. For simplicity, all of these circuits are

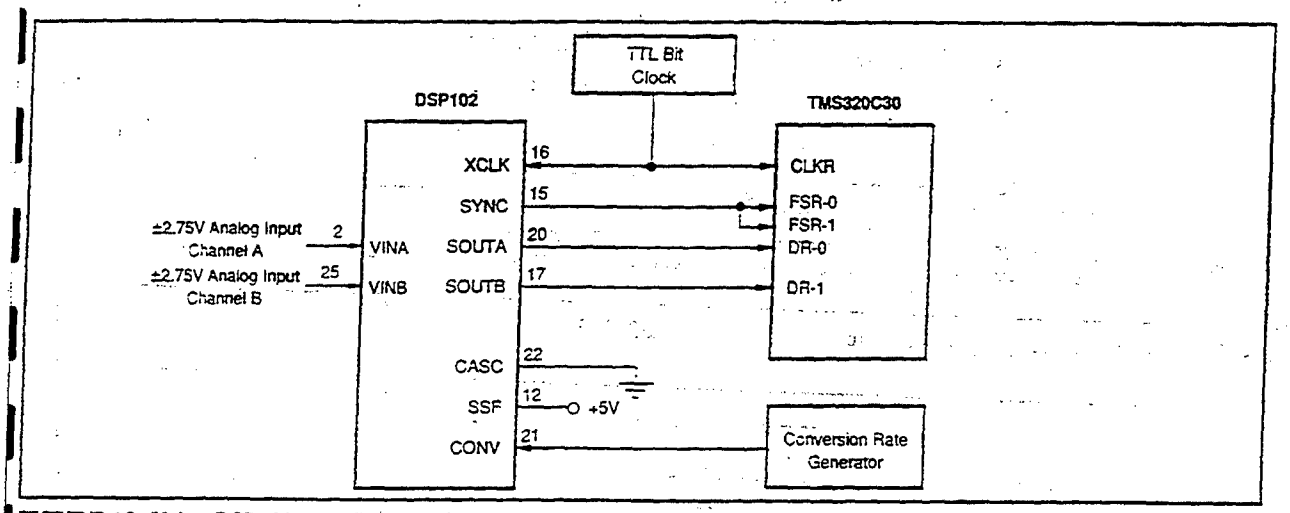


FIGURE 12. Using DSP102 with TMS320C30.

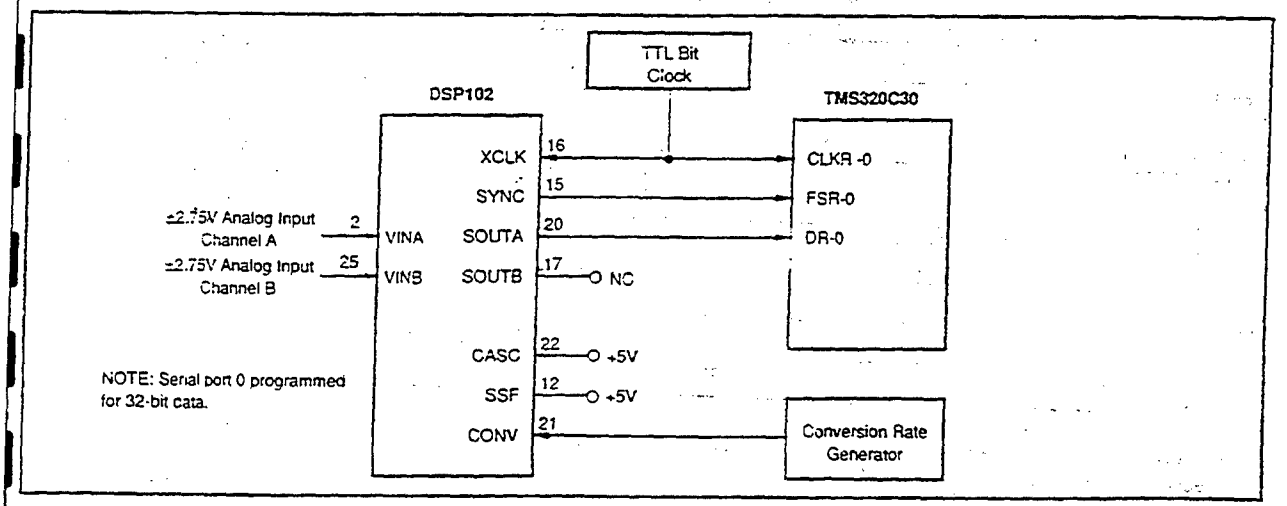
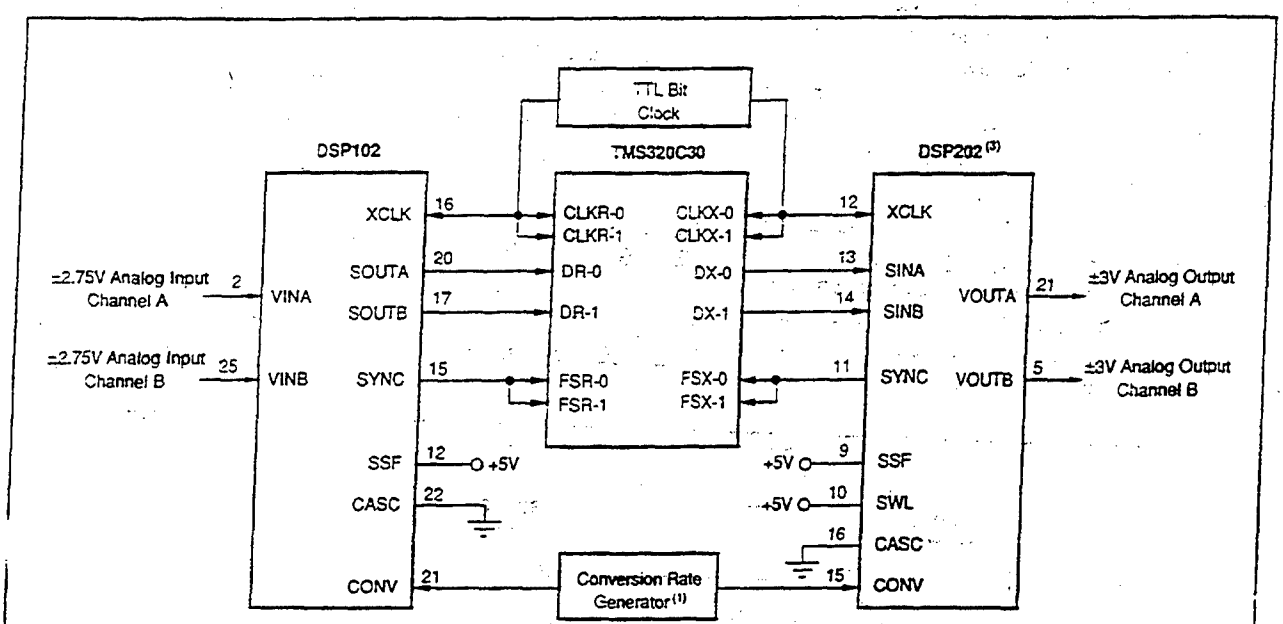


FIGURE 13. Using DSP102 with TMS320C30 in Cascade Mode.

based on using the TME320Cxx in the mode where SSF (Select Synch Format, pin 12) is tied HIGH, so that there is an active High synchronization pulse generated by the DSP101 or DSP102 after receiving a convert command. The synchronization pulse can be changed to active Low simply by making SSF LOW, where appropriate, without changing the basic operation of the A/Ds.

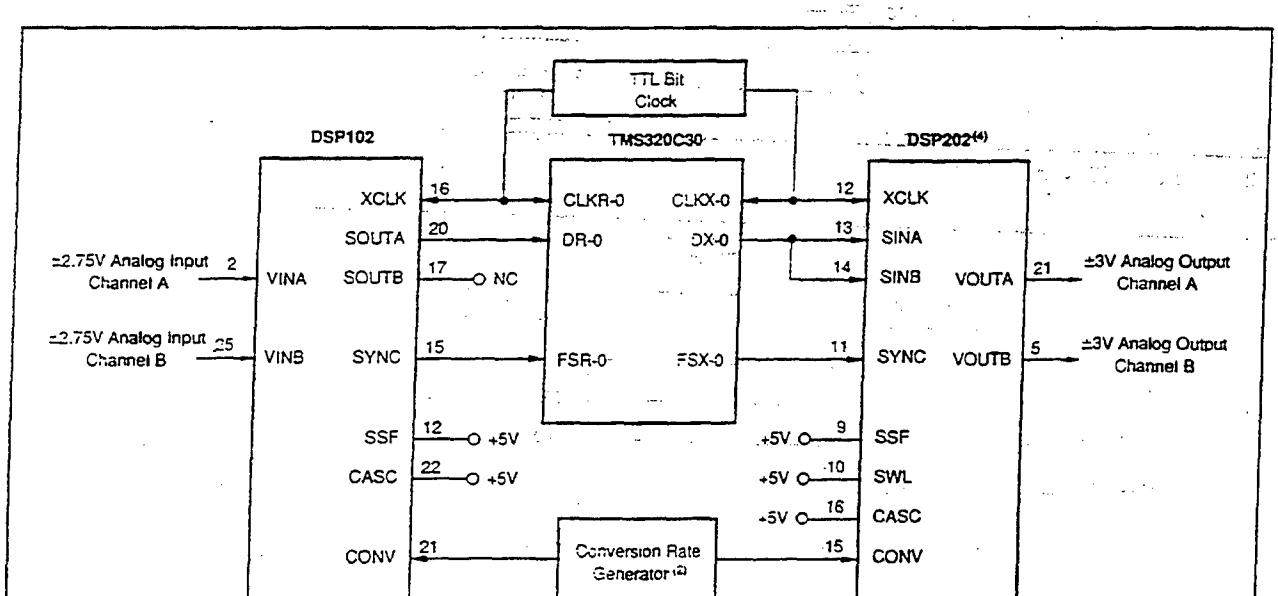
In all cases, the DSP101 and DSP102 will transmit data MSB-first, and the TMS320Cxx needs to be programmed for this.

Figure 11 shows a circuit for using the TMS320C25 or TMS320C30 in a complete analog input and analog output system using the DSP101 along with the Burr-Brown DSP201 D/A.



NOTES: (1) Sample rate on DSP102 and DSP202 may differ. (2) Analog Devices ADSP2101 may be used. SPORT1 and SPORT2 are used for serial MSB first communication. (3) See Burr-Brown DSP201/DSP202 product data sheet for full description of this DAC.

FIGURE 14. Two-Channel Analog Input and Output System with TMS320C30.



NOTES: (1) Program TMS320C30 for 32-bit mode. (2) Sample rate on DSP102 and DSP202 may differ. (3) DSP32C may be used in this mode. (4) See Burr-Brown DSP201/202 product data sheet for full description of this DAC.

FIGURE 15. Two-Channel Analog Input and Output System with TMS320C30 in Cascade Mode.

USING TMS320C31 TO GENERATE ALL CONTROL SIGNALS

Figure 17 shows a circuit for using the TMS320C31 with a DSP102 and a Burr-Brown DSP202 D/A to provide a two channel analog I/O system. The flexibility of the TMS320C31 allows it to generate the data transfer clock (XCLK) and the Convert Command, minimizing additional circuitry and synchronizing the timing signals to the processor's master clock. In this circuit, the DSP102 and DSP202 are used in their Cascade modes, transmitting and receiving two channels of data in a single 32-bit word. (See the Cascade Mode section above.)

Table II shows how to set up the circuit in Figure 17 for a 44.1kHz conversion rate for both channels of the DSP102 A/D and both channels of the DSP202 D/A. Both inputs and outputs will be simultaneously converted.

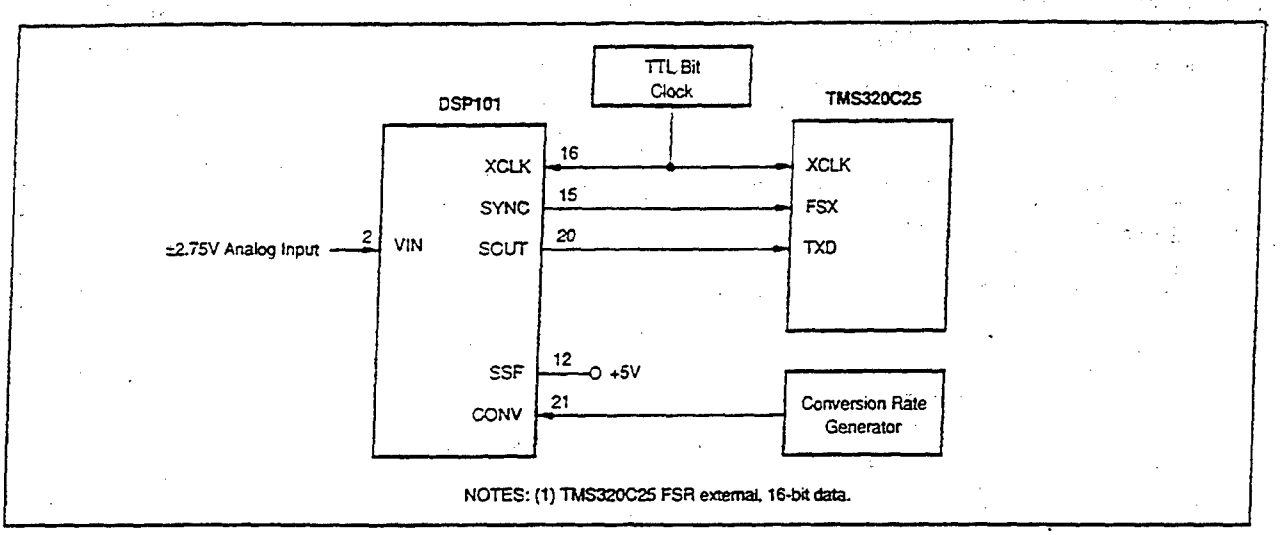


FIGURE 16. Using DSP101 with TMS320C25.

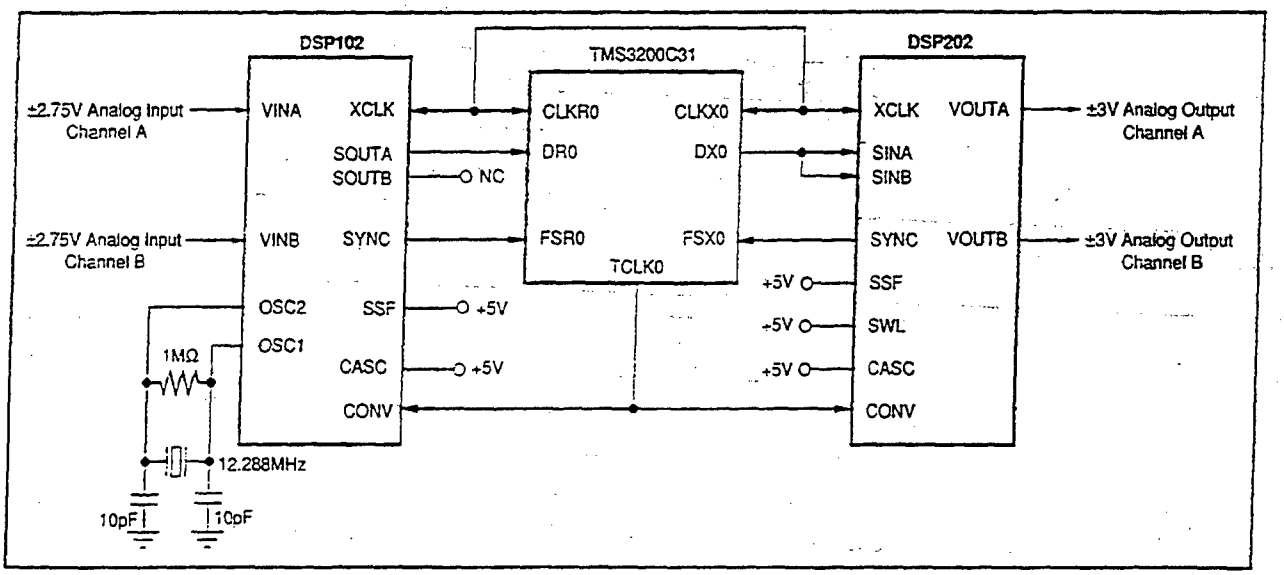


FIGURE 17. Two Channel Analog I/O Using TMS320C31.

SERIAL PORT	
Port Global Control Register	0x0EBC040
FSX/DX/CLKX Port Control Register	0x00000111
FSR/DR/CLKR Port Control Register	0x00000111
Receive/Transmit Timer Control Register	0x0000000F
TIMER	
Timer Global Control Register	0x000002C1
Timer Period Register	0x000000B5
NOTE: Assumes TMS320C31 has 32MHz Master Clock.	

TABLE II. TMS320C31 Register Settings for 44.1kHz Conversion Rate in Figure 17.

USING DSP101 AND DSP102 WITH MOTOROLA DSP ICS

Figure 18 shows how to use the DSP101 with a Motorola DSP56001. Using the DSP102 requires using two DSP56001s. The DSP56001 needs to be programmed to receive data MSB-first with SYNC in the Bit Mode.

SSF (pin 12) needs to be tied HIGH for using either the DSP101 or the DSP102 with DSP56001s. This will cause the DSP101 or DSP102 to transmit an appropriate active High synchronization pulse on SYNC (pin 15) after a convert command is received by the A/D. Timing is shown in Figure 1.

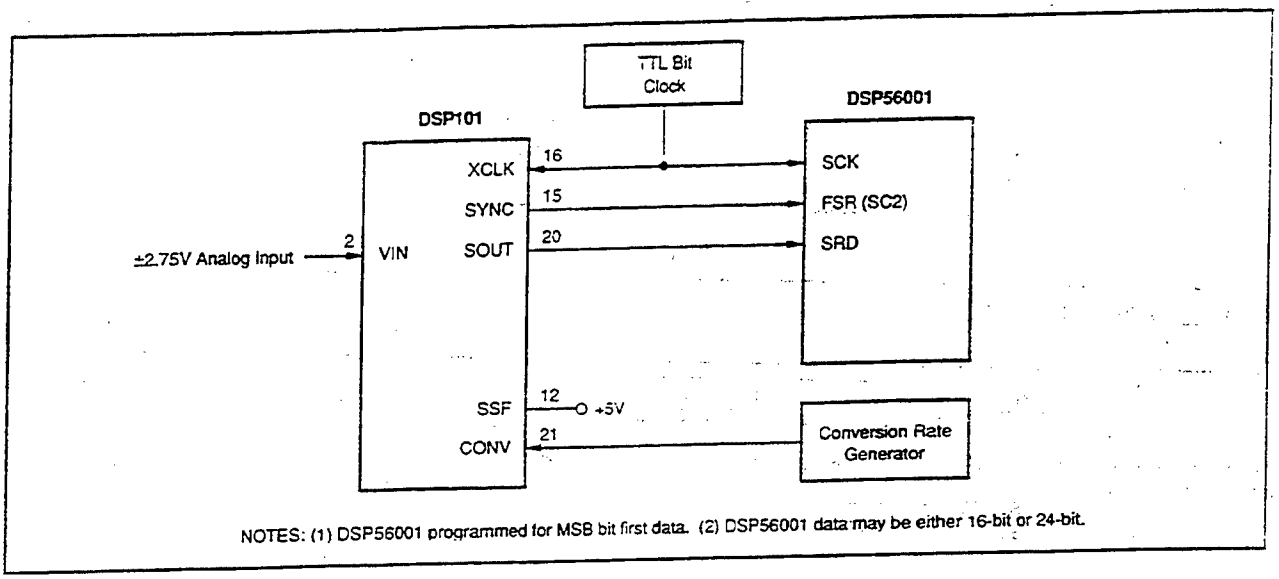
USING DSP101 AND DSP102 WITH AT&T DSP ICS

Figures 11, 19, 20, and 21 show how to use the DSP101 and DSP102 with the DSP16 and DSP32C in different modes. The AT&T processors need to be programmed to accept data MSB-first, and the DSP101 or DSP102 needs to have SSF (pin 12) tied LOW, so that an appropriate active Low synchronization pulse will be transmitted by the A/D after a convert command is received.

Figures 19 and 20 show the DSP32C and DSP16 respectively used with the DSP101 to handle a single analog input channel.

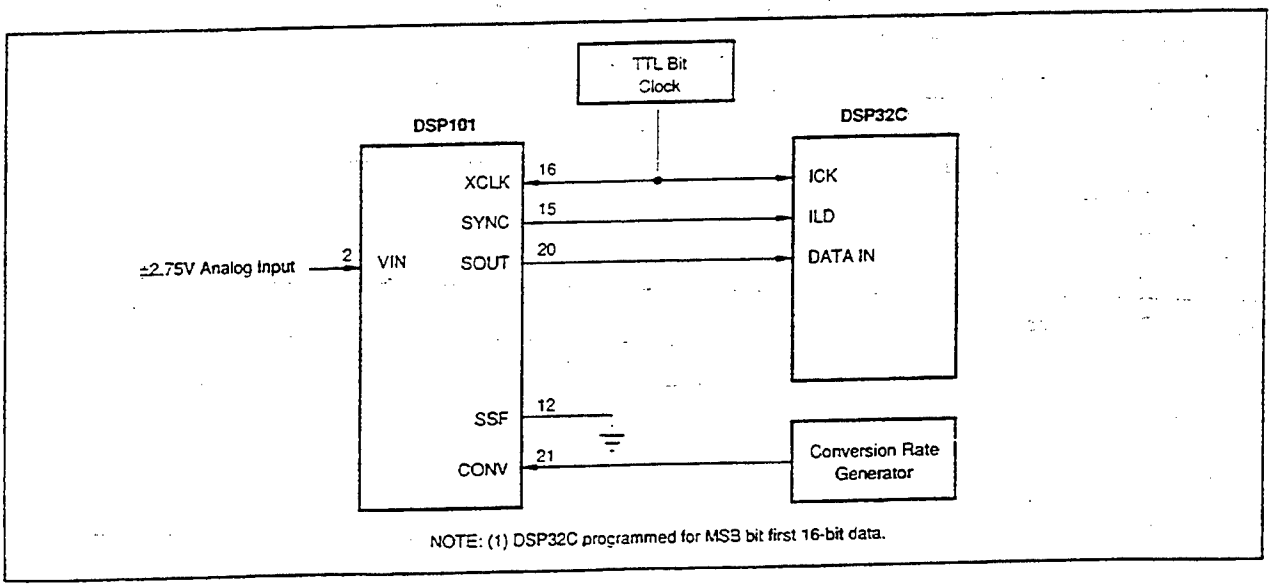
Figure 21 shows how to transmit to a single DSP32C conversion results from both DSP102 channels in a single 32-bit word, using the Cascade mode on the A/D.

Figure 11 indicates how to build a complete analog input and analog output system using a DSP32C or DSP16 with a DSP101 and a Burr-Brown DSP201 D/A.



NOTES: (1) DSP56001 programmed for MSB bit first data. (2) DSP56001 data may be either 16-bit or 24-bit.

FIGURE 18. Using DSP101 with DSP56001.



NOTE: (1) DSP32C programmed for MSB bit first 16-bit data.

FIGURE 19. Using DSP101 with DSP32C.

USING DSP101 AND DSP102 WITH ADI DSP ICS

When using the DSP101 or DSP102 with the fixed-point ADSP21xx series, the processors need to be programmed to receive data MSB-first.

Figure 22 shows how to use the DSP102 with an ADSP2101 to provide a two-channel simultaneous sampling system.

Figure 23 shows the connections required to generate an analog input channel using an ADSP2105 with the DSP101.

The same basic circuit can be used to connect a DSP101 to the ADSP2101.

Figure 11 indicates how to build a complete analog I/O system using either the ADSP2101 or the ADSP2105 with a DSP101 and a Burr-Brown DSP201 D/A.

The two serial ports on the ADSP2101 can also be used with the DSP102 and the Burr-Brown DSP202 D/A to make two complete analog I/O channels, as indicated in footnote 2 of Figure 14.

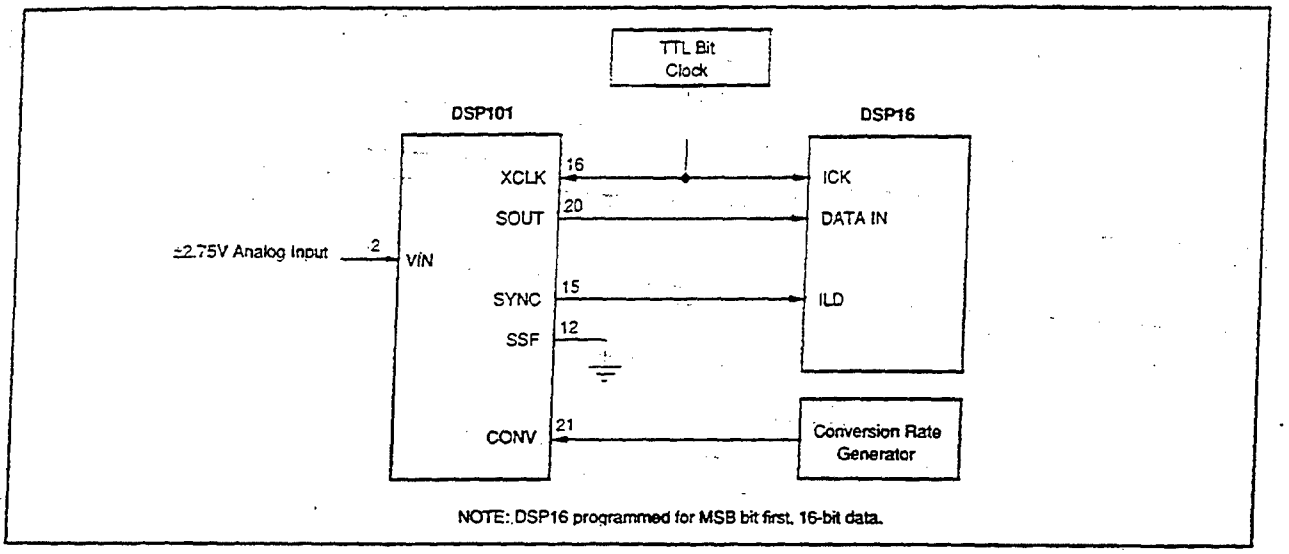


FIGURE 20. Using DSP101 with DSP16.

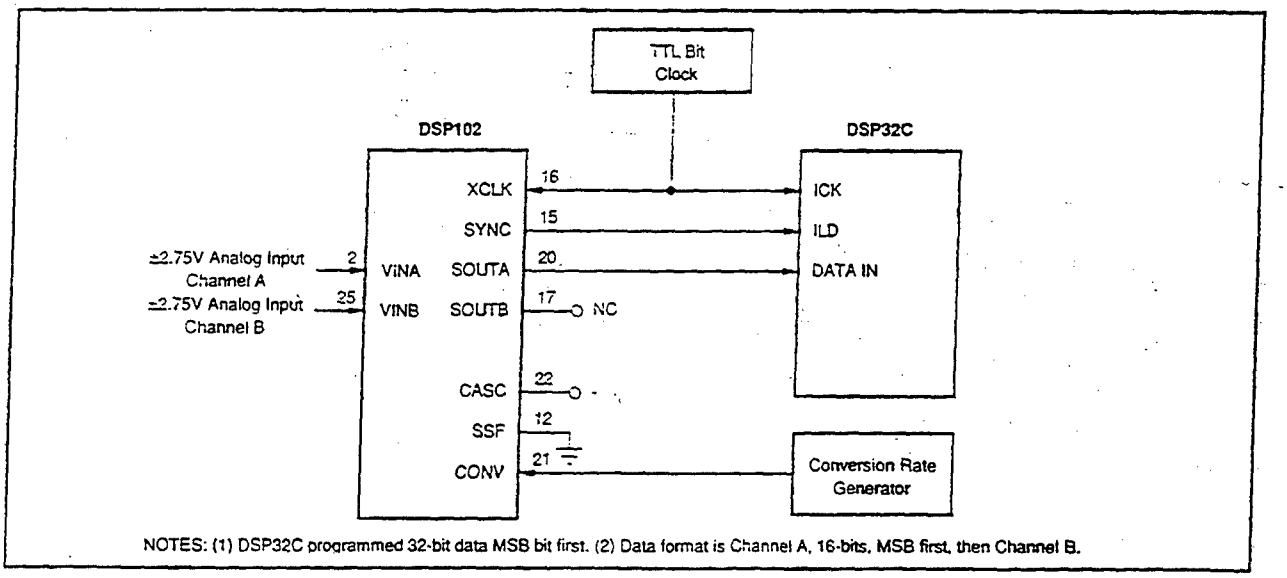


FIGURE 21. Using DSP102 with DSP32C in Cascade Mode.

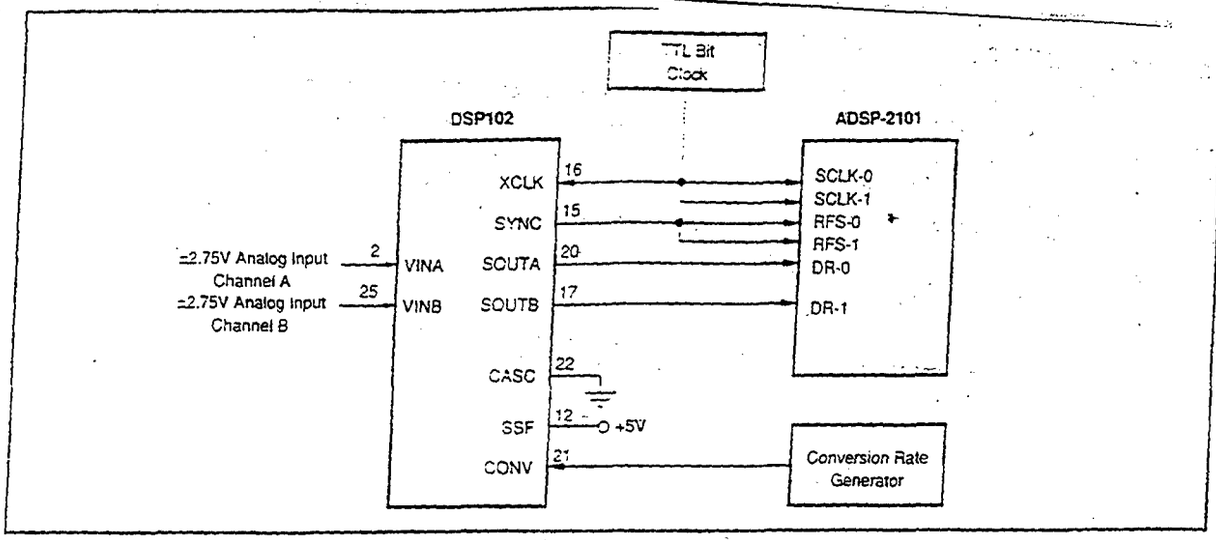


FIGURE 22. Using DSP102 with ADSP-2101.

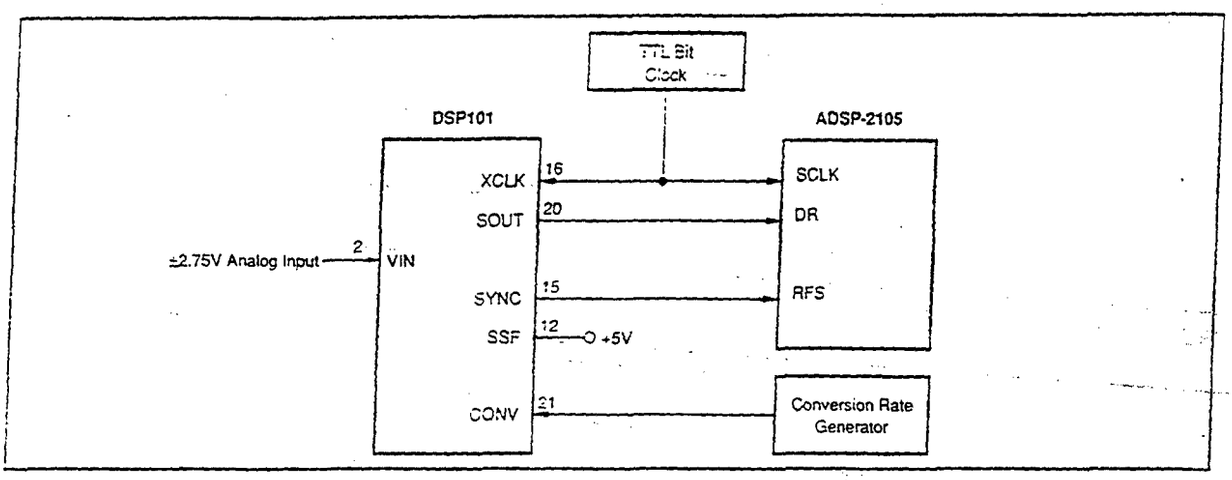


FIGURE 23. Using DSP101 with ADSP-2105.

DEM-DSP102/202 EVALUATION BOARD

An evaluation fixture, the DEM-DSP102/202, is available to simplify evaluation of the DSP101 and DSP102, and the companion digital-to-analog converters, the single DSP201 and dual DSP202. The DEM-DSP102/202 comes complete with a socketed DSP102 and DSP202, a breadboard area, TTL I/O headers and differential line drivers for data transfer options, a complete clocking circuit for the conversion clock and bit clock, and analog filter modules. The board makes it easy to go from design concept to working prototype of a DSP-based system, offering two complete analog I/O channels.

Contact your local Burr-Brown representative for a full data sheet on the DEM-DSP102/202.

CMOS single-chip 8-bit microcontrollers — 83C750/87C750

DESCRIPTION

The Philips 8XC750 offers the advantages of the 80C51 architecture in a small package and at low cost.

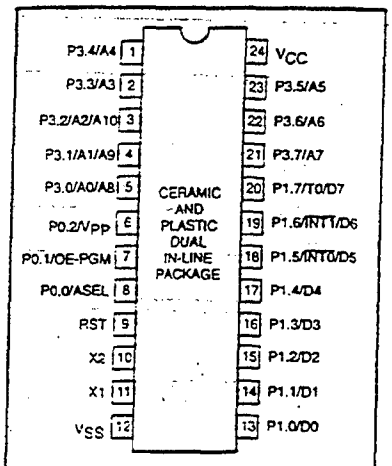
The 8XC750 Microcontroller is fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes CMOS latch-up sensitivity.

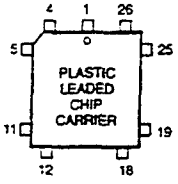
The 87C750 contains a 1k x 8 EPROM, a 64 x 8 RAM, 19 I/O lines, a 16-bit auto-reload counter/timer, a five-source, fixed-priority level interrupt structure and an on-chip oscillator.

FEATURES

- 80C51 based architecture
- Wide oscillator frequency range—up to 40MHz
- Small package sizes
  - 24-pin DIP (300 mil "skinny DIP")
  - 28-pin PLCC
- 87C750 available in erasable quartz lid or one-time programmable plastic packages
- Low power consumption:
  - Normal operation: less than 11mA @ 5V, 12MHz
  - Idle mode
  - Power-down mode
- 1k x 8 EPROM (87C750)
- 64 x 8 RAM
- 16-bit auto reloadable counter/timer
- Boolean processor
- CMOS and TTL compatible
- Well suited for logic replacement, consumer and industrial applications
- LED drive outputs

PIN CONFIGURATIONS





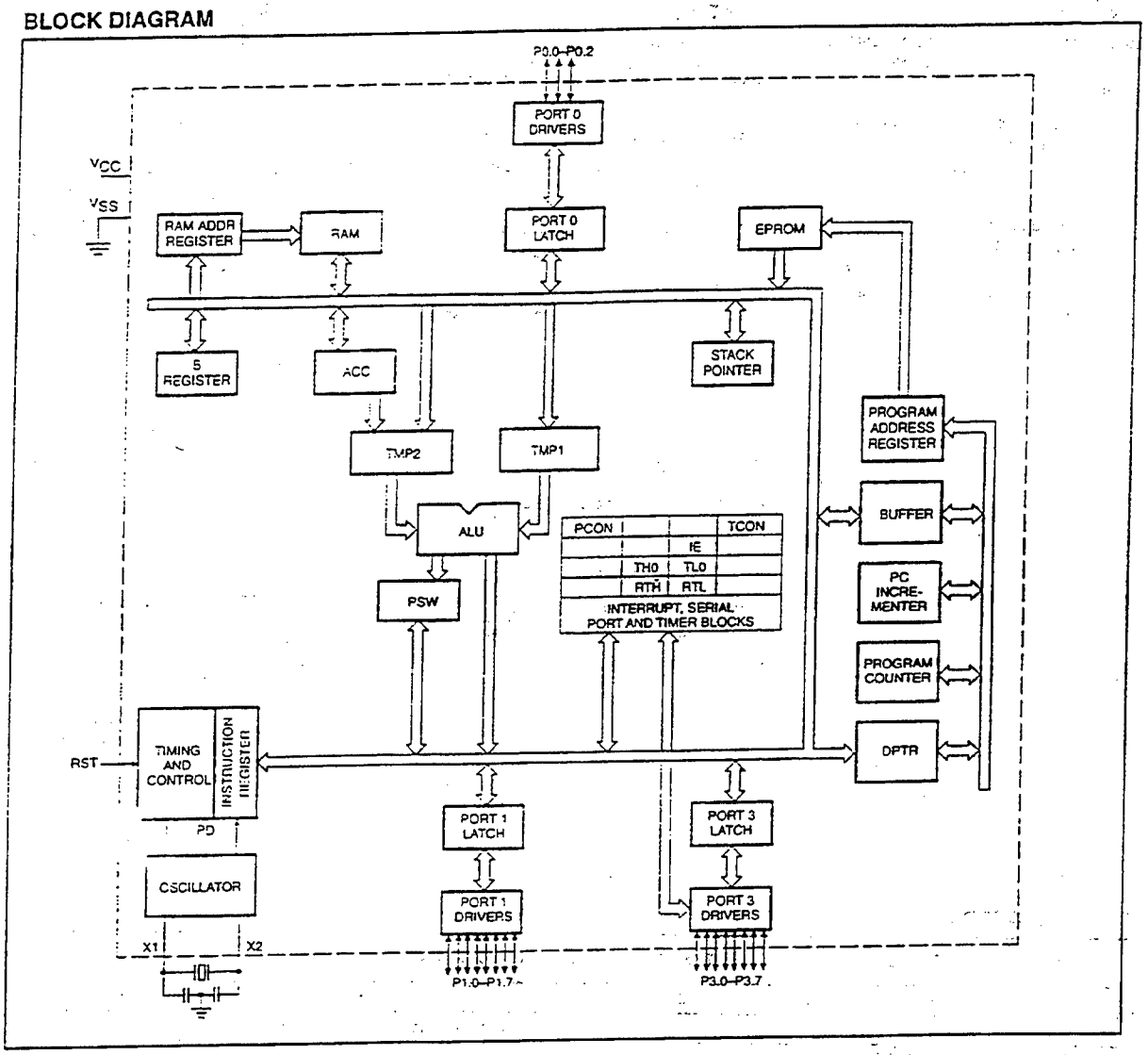
Pin	Function	Pin	Function
1	P3.4/A4	15	P1.0/D0
2	P3.3/A3	16	P1.1/D1
3	P3.2/A2/A10	17	P1.2/D2
4	P3.1/A1/A9	18	P1.3/D3
5	N.C.	19	P1.4/D4
6	P3.0/A0/A8	20	P1.5/INT0/D5
7	P0.2/VPP	21	N.C.
8	P0.1/OE-PGM	22	N.C.
9	P0.0/ASEL	23	P1.6/INT1/D6
10	N.C.	24	P1.7/T0/D7
11	RST	25	P3.7/A7
12	X2	26	P3.6/A6
13	X1	27	P3.5/A5
14	VSS	28	VCC

ORDERING INFORMATION

ROM	EPROM[1]		TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY	DRAWING NUMBER
	P87C750EBF FA	UV	0 to +70, Ceramic Dual In-line Package	3.5 to 16MHz	0586B
	P87C750EFF FA	UV	–40 to +85, Ceramic Dual In-line Package	3.5 to 16MHz	0586B
P83C750EBP N	P87C750EBP N	OTP	0 to +70, Plastic Dual In-line Package	3.5 to 16MHz	0410D
P83C750EFP N	P87C750EFP N	OTP	–40 to +85, Plastic Dual In-line Package	3.5 to 16MHz	0410D
P83C750EBA A	P87C750EBA A	OTP	0 to +70, Plastic Lead Chip Carrier	3.5 to 16MHz	0401F
P83C750EFA A	P87C750EFA A	OTP	–40 to +85, Plastic Lead Chip Carrier	3.5 to 16MHz	0401F
P83C750PBP N	P87C750PBP N	OTP	0 to +70, Plastic Dual In-line Package	3.5 to 40MHz	0410D
P83C750PFP N	P87C750PFP N	OTP	–40 to +85, Plastic Dual In-line Package	3.5 to 40MHz	0410D
P83C750PBA A	P87C750PBA A	OTP	0 to +70, Plastic Lead Chip Carrier	3.5 to 40MHz	0401F
P83C750PFA A	P87C750PFA A	OTP	–40 to +85, Plastic Lead Chip Carrier	3.5 to 40MHz	0401F
	P87C750PBF FA	UV	0 to +70, Ceramic Dual In-line Package	3.5 to 40MHz	0586B
	P87C750PFF FA	UV	–40 to +85, Ceramic Dual In-line Package	3.5 to 40MHz	0586B

NOTE:
1. OTP = One Time Programmable EPROM. UV = UV Erasable EPROM.

BLOCK DIAGRAM



PIN DESCRIPTIONS

MNEMONIC	PIN NO. DIP/ SSOP	PIN NO. LCC	TYPE	NAME AND FUNCTION
V_{SS}	12	14	I	**Circuit Ground Potential**
V_{CC}	24	28	I	**Supply voltage during normal, idle, and power-down operation.**
P0.0-P0.2	8-6	9-7	I/O	**Port 0:** Port 0 is a 3-bit open-drain, bidirectional port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. These pins are driven low if the port register bit is written with a 0. The state of the pin can always be read from the port register by the program. P0.0 and P0.1 are open drain bidirectional I/O pins with the electrical characteristics listed in the tables that follow. While these differ from "standard TTL" characteristics, they are close enough for the pins to still be used as general-purpose I/O. Port 0 also provides alternate functions for programming the EPROM memory as follows:
	6	7	N/A	V_{PP} **(P0.2)** – Programming voltage input.
	7	9	I	**OE/PGM (P0.1)** – Input which specifies verify mode (output enable) or the program mode. OE/PGM = 1 output enabled (verify mode). OE/PGM = 0 program mode.
	8	9	I	**ASEL (P0.0)** – Input which indicates which bits of the EPROM address are applied to port 3. ASEL = 0 low address byte available on port 3. ASEL = 1 high address byte available on port 3 (only the three least significant bits are used).
P1.0-P1.7	13-20	15-20, 23, 24	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 serves to output the addressed EPROM contents in the verify mode and accepts as inputs the value to program into the selected address during the program mode. Port 1 also serves the special function features of the 80C51 family as listed below:
	18	20	I	**$\overline{INT0}$ (P1.5):** External interrupt.
	19	23	I	**$\overline{INT1}$ (P1.6):** External interrupt.
	20	24	I	**T0 (P1.7):** Timer 0 external input.
P3.0-P3.7	5-1, 23-21	4-1, 6, 27-25	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also functions as the address input for the EPROM memory location to be programmed (or verified). The 10-bit address is multiplexed into this port as specified by P0.0/ASEL.
RST	9	11	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on RESET using only an external capacitor to V_{CC}. After the device is reset, a 10-bit serial sequence, sent LSB first, applied to RESET, places the device in the programming state allowing programming address, data and V_{PP} to be applied for programming or verification purposes. The RESET serial sequence must be synchronized with the X1 input.
X1	11	13	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. X1 also serves as the clock to strobe in a serial bit stream into RESET to place the device in the programming state.
X2	10	12	O	**Crystal 2:** Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

X1 and X2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, X1 should be driven while X2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-up, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. the control bits for the reduced power modes are in the special function register PCON.

Table 1. External Pin Status During Idle and Power-Down Modes

MODE	Port 0	Port 1	Port 2
Idle	Data	Data	Data
Power-down	Data	Data	Data

DIFFERENCES BETWEEN THE 8XC750 AND THE 80C51

Program Memory

On the 8XC750, program memory is 1024 bytes long and is not externally expandable, so the 80C51 instructions MOVX, LJMP, and LCALL are not implemented. The only fixed locations in program memory are the addresses at which execution is taken up in response to reset and interrupts, which are as follows:

Event	Program Memory Address
Reset	000
External $\overline{INT0}$	003
Counter/timer 0	00B
External $\overline{INT1}$	013

Counter/Timer Subsystem

The 87C750 has one counter/timer called timer/counter 0. Its operation is similar to mode 2 operation on the 80C51, but is extended to 16 bits with 16 bits of autoload. The controls for this counter are centralized in a single register called TCON.

Interrupt Subsystem – Fixed Priority

The IP register and the 2-level interrupt system of the 80C51 are eliminated. Simultaneous interrupt conditions are resolved by a single-level, fixed priority as follows:

Highest priority: Pin $\overline{INT0}$
Counter/timer flag 0
Pin $\overline{INT1}$

Special Function Register Addresses

Special function registers for the 8XC750 are identical to those of the 80C51, except for the changes listed below:

80C51 special function registers not present in the 8XC750 are TMOD (89), P2 (A0) and IP (B8). The 80C51 registers TH1 and TL1 are replaced with the 87C750 registers RTH and RTL respectively (refer to Table 2).

Table 2. 87C750 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR:	Data pointer (2 bytes)										
DPH	High byte	83H									00H
DPL	Low byte	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*#	Interrupt enable	A8H	EA	–	–	–	–	EX1	ET0	EX0	00H
								S2	S1	S0	
P0*#	Port 0	80H	–	–	–	–	–	–	–	–	xxxxx111B
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	T0	INT1	INT0	–	–	–	–	–	FFH
P3*	Port 3	B0H	B7	B6	B5	B4	B3	B2	B1	B0	FFH
PCON#	Power control	87H	–	–	–	–	–	–	PD	IDL	xxxxxx00B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
SP	Stack pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*#	Timer/counter control	88H	GATE	C/T	TF	TR	IE0	IT0	IE1	IT1	00H
TL#	Timer low byte	8AH									00H
TH#	Timer high byte	8CH									00H
RTL#	Timer low reload	89H									00H
RTH#	Timer high reload	8DH									00H

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.

ABSOLUTE MAXIMUM RATINGS[1, 2]

PARAMETER	RATING	UNIT
Storage temperature range	–65 to +150	°C
Voltage from V_{CC} to V_{SS}	–0.5 to +6.5	V
Voltage from any pin to V_{SS} (except V_{PP})	–0.5 to V_{CC} + 0.5	V
Power dissipation	1.0	W
Voltage on V_{PP} pin to V_{SS}	0 to +13.0	V
Maximum I_{OL} per I/O pin	10	mA

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or −40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V[1]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNIT
V_{IL}	Input low voltage		−0.5	$0.2V_{DD}$−0.1	V
V_{IH}	Input high voltage, except X1, RST		$0.2V_{CC}$+0.9	V_{CC}+0.5	V
V_{IH1}	Input high voltage, X1, RST		$0.7V_{CC}$	V_{CC}+0.5	V
V_{OL}	Output low voltage, ports 1 and 3	I_{OL} = 1.6mA[2]		0.45	V
V_{OL1}	Output low voltage, port 0	I_{OL} = 3.2mA[2]		0.45	V
V_{OH}	Output high voltage, ports 1 and 3	I_{OH} = −60µA I_{OH} = −25µA I_{OH} = −10µA	2.4 $0.75V_{CC}$ $0.9V_{CC}$		V V
C	Capacitance			10	pF
I_{IL}	Logical 0 input current, ports 1 and 3	V_{IN} = 0.45V		−50	µA
I_{TL}	Logical 1 to 0 transition current, ports 1 and 3[3]	V_{IN} = 2V (0 to +70°C) V_{IN} = 2V (−40 to +85°C)		−650 −750	µA µA
I_{LI}	Input leakage current, port 0	0.45 < V_{IN} < V_{CC}		±10	µA
R_{RST}	Internal pull-down resistor		25	175	kΩ
C_{IO}	Pin capacitance	Test freq = 1MHz, T_{amb} = 25°C		10	pF
I_{PD}	Power-down current[4]	V_{CC} = 2 to V_{CC} max		50	µA
V_{PP}	V_{PP} program voltage	V_{SS} = 0V V_{CC} = 5V±10% T_{amb} = 21°C to 27°C	12.5	13.0	V
I_{PP}	Program current	V_{PP} = 13.0V		50	mA
I_{CC}	Supply current (see Figure 2)[5, 6]				

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
2. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA (NOTE: This is 85°C spec.)
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum total I_{OL} for all outputs: 67mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
3. Pins of ports 1 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
4. Power-down I_{CC} is measured with all output pins disconnected; port 0 = V_{CC}; X2, X1 n.c.; RST = V_{SS}.
5. Active I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} − 0.5V; X2 n.c.; RST = port 0 = V_{CC}. I_{CC} will be slightly higher if a crystal oscillator is used.
6. Idle I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} − 0.5V; X2 n.c.; port 0 = V_{CC}; RST = V_{SS}.

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or −40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V[1, 2]

SYMBOL	PARAMETER	VARIABLE CLOCK MIN	VARIABLE CLOCK MAX	MIN	MAX	UNIT
$1/t_{CLCL}$	Oscillator frequency:	3.5	16	3.5	40	MHz
External Clock (Figure 1)						
t_{CHCX}	High time	20		10		ns
t_{CLCX}	Low time	20		10		ns
t_{CLCH}	Rise time		20		20	ns
t_{CHCL}	Fall time		20		20	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
2. Load capacitance for ports = 80pF.

EXPLANATION OF THE AC SYMBOLS

In defining the clock waveform, care must be taken not to exceed the MIN or MAX limits of the AC electrical characteristics table. Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

C – Clock
D – Input data

H – Logic level high
L – Logic level low
Q – Output data
T – Time
V – Valid
X – No longer a valid logic level
Z – Float

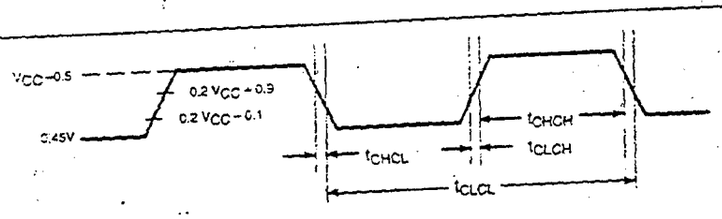


Figure 1. External Clock Drive

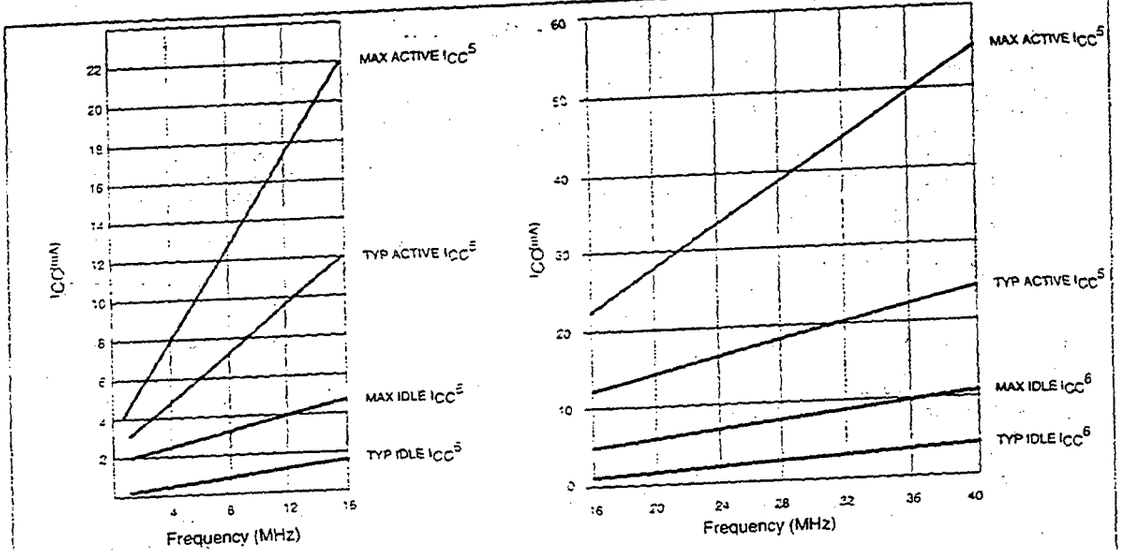


Figure 2. I_{CC} vs. Frequency
Maximum I_{CC} values taken at V_{CC} max and worst case temperature.
Typical I_{CC} values taken at V_{CC} = 5.0V and 25°C.
Notes 5 and 6 refer to DC Electrical Characteristics.

87C750 PROGRAMMING CONSIDERATIONS

EPROM Characteristics

The 87C750 is programmed by using a modified Quick-Pulse Programming algorithm similar to that used for devices such as the 87C451 and 87C51. It differs from these devices in that a serial data stream is used to place the 87C750 in the programming mode.

Figure 3 shows a block diagram of the programming configuration for the 87C750. Port pin P0.2 is used as the programming voltage supply input (V_{PP} signal). Port pin P0.1 is used as the program (PGM/) signal. This pin is used for the 25 programming pulses.

Port 3 is used as the address input for the byte to be programmed and accepts both the high and low components of the eleven bit address. Multiplexing of these address components is performed using the ASEL input. The user should drive the ASEL input high and then drive port 3 with the high order bits of the address. ASEL should remain high for at least 13 clock cycles. ASEL may then be driven low which latches the high order bits of the address internally. the high address should remain on port 3 for at least two clock cycles after ASEL is driven low. Port 3 may then be driven with the low byte of the address. The low address will be internally stable 13 clock cycles later. The address will remain stable provided that the low byte placed on port 3 is held stable and ASEL is kept low. **Note:** ASEL needs to be pulsed high only to change the high byte of the address.

Port 1 is used as a bidirectional data bus during programming and verify operations. During programming mode, it accepts the byte to be programmed. During verify mode, it provides the contents of the EPROM location specified by the address which has been supplied to Port 3.

The XTAL1 pin is the oscillator input and receives the master system clock. This clock should be between 1.2 and 6MHz.

The RESET pin is used to accept the serial data stream that places the 87C750 into various programming modes. This pattern consists of a 10-bit code with the LSB sent first. Each bit is synchronized to the clock input, X1.

Programming Operation

Figures 4 and 5 show the timing diagrams for the program/verify cycle. RESET should initially be held high for at least two machine cycles. P0.1 (PGM/) and P0.2 (V_{PP}) will be at V_{OH} as a result of the RESET operation. At this point, these pins function as normal quasi-bidirectional I/O ports and the programming equipment may pull these lines low. However, prior to sending the 10-bit code on the RESET pin, the programming equipment should drive these pins high (V_{IH}). The RESET pin may now be used as the serial data input for the data stream which places the 87C750 in the programming mode. Data bits are sampled during the clock high time and thus should only change during the time that the clock is low. Following transmission of the last data bit, the RESET pin should be held low.

Next the address information for the location to be programmed is placed on port 3 and ASEL is used to perform the address multiplexing, as previously described. At this time, port 1 functions as an output.

A high voltage V_{PP} level is then applied to the V_{PP} input (P0.2). (This sets Port 1 as an input port). The data to be programmed into the EPROM array is then placed on Port 1. This is followed by a series of programming pulses applied to the PGM/ pin (P0.1). These pulses are created by driving P0.1 low and then high. This pulse is repeated until a total of 25 programming pulses have occurred. At the conclusion of the last pulse, the PGM/ signal should remain high.

The V_{PP} signal may now be driven to the V_{OH} level, placing the 87C750 in the verify mode. (Port 1 is now used as an output port). After four machine cycles (48 clock periods), the contents of the addressed location in the EPROM array will appear on Port 1.

The next programming cycle may now be initiated by placing the address information at the inputs of the multiplexed buffers, driving the V_{PP} pin to the V_{PP} voltage level, providing the byte to be programmed to Port1 and issuing the 25 programming pulses on the PGM/ pin, bringing V_{PP} back down to the V_C level and verifying the byte.

Programming Modes

The 87C750 has four programming features incorporated within its EPROM array. These include the USER EPROM for storage of the application's code; a 16-byte encryption key array and two security bits. Programming and verification of these four elements are selected by a combination of the serial data stream applied to the RESET pin and the voltage levels applied to port pins P0.1 and P0.2. The various combinations are shown in Table 3.

Encryption Key Table

The 87C750 includes a 16-byte EPROM array that is programmable by the end user. The contents of this array can then be used to encrypt the program memory contents during a program memory verify operation. When a program memory verify operation is performed, the contents of the program memory location is XNOR'ed with one of the bytes in the 16-byte encryption table. The resulting data pattern is then provided to port 1 as the verify data. The encryption mechanism can be disable, in essence, by leaving the bytes in the encryption table in their erased state (FFH) since the XNOR product of a bit with a logical one will result in the original bit. The encryption bytes are mapped with the code memory in 16-byte groups. the first byte in code memory will be encrypted with the first byte in the encryption table; the second byte in code memory will be encrypted with the second byte in the encryption table and so forth up to and including the 16the byte. The encryption repeats in 16-byte groups; the 17th byte in the code memory will be encrypted with the first byte in the encryption table, and so forth.

Security Bits

Two security bits, security bit 1 and security bit 2, are provided to limit access to the USER EPROM and encryption key arrays. Security bit 1 is the program inhibit bit, and once programmed performs the following functions:

1. Additional programming of the USER EPROM is inhibited.
2. Additional programming of the encryption key is inhibited.
3. Verification of the encryption key is inhibited.
4. Verification of the USER EPROM and the security bit levels may still be performed.

(If the encryption key array is being used, this security bit should be programmed by the user to prevent unauthorized parties from reprogramming the encryption key to all logical zero bits. Such programming would provide data during a verify cycle that is the logical complement of the USER EPROM contents).

Security bit 2, the verify inhibit bit, prevents verification of both the USER EPROM array and the encryption key arrays. The security bit levels may still be verified.

Programming and Verifying Security Bits

Security bits are programmed employing the same techniques used to program the USER EPROM and KEY arrays using serial data streams and logic levels on port pins indicated in Table 3. When programming either security bit, it is not necessary to provide address or data information to the 87C750 on ports 1 and 3.

Verification occurs in a similar manner using the RESET serial stream shown in Table 3. Port 3 is not required to be driven and the results of the verify operation will appear on ports 1.6 and 1.7.

Ports 1.7 contains the security bit 1 data and is a logical one if programmed and a logical zero if erased. Likewise, P1.6 contains the security bit 2 data and is a logical one if programmed and a logical zero if erased.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Flourless part number 2345-5 or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000µW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Table 3. Implementing Program/Verify Modes

OPERATION	SERIAL CODE	P0.1 (PGM)	P0.2 (V_{PP})
Program user EPROM	296H	–[1]	V_{PP}
Verify user EPROM	296H	V_{IH}	V_{IH}
Program key EPROM	292H	–[1]	V_{PP}
Verify key EPROM	292H	V_{IH}	V_{IH}
Program security bit 1	29AH	–[1]	V_{PP}
Program security bit 2	298H	–[1]	V_{PP}
Verify security bits	29AH	V_{IH}	V_{IH}

NOTE:
1. Pulsed from V_{IH} to V_{IL} and returned to V_{IH}.

EPROM PROGRAMMING AND VERIFICATION

T_{amb} = 21°C to +27°C; V_{CC} = 5V ±10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	MAX	UNIT
$1/t_{CLCL}$	Oscillator/clock frequency	1.2	6	MHz
t_{AVGL}	Address setup to P0.1 (PROG–) low	10µs + $24t_{CLCL}$		
t_{GHAX}	Address hold after P0.1 (PROG–) high	$48t_{CLCL}$		
t_{DVGL}	Data setup to P0.1 (PROG–) low	$38t_{CLCL}$		
t_{DVGL}	Data setup to P0.1 (PROG–) low	$38t_{CLCL}$		
t_{GHDX}	Data hold after P0.1 (PROG–) high	$36t_{CLCL}$		
t_{SHGL}	V_{PP} setup to P0.1 (PROG–) low	10		µs
t_{GHSL}	V_{PP} hold after P0.1 (PROG–)	10		µs
t_{GLGH}	P0.1 (PROG–) width	90	110	µs
t_{AVQV}	V_{PP} low (V_{CC}) to data valid		$48t_{CLCL}$	
t_{GHGL}	P0.1 (PROG–) high to P0.1 (PROG–) low	10		µs
t_{SYNL}	P0.0 (sync pulse) low	$4t_{CLCL}$		
t_{SYNH}	P0.0 (sync pulse) high	$8t_{CLCL}$		
t_{MASEL}	ASEL high time	$13t_{CLCL}$		
t_{MAH_C}	Address hold time	$2t_{CLCL}$		
t_{HASET}	Address setup to ASEL	$13t_{CLCL}$		
t_{ADSTA}	Low address to valid data		$48t_{CLCL}$	

NOTES:
1. Address should be valid at least $24t_{CLCL}$ before the rising edge of P0.2 (V_{PP}).
2. For a pure verify mode, i.e., no program mode in between, t_{AVQV} is $141t_{CLCL}$ maximum.

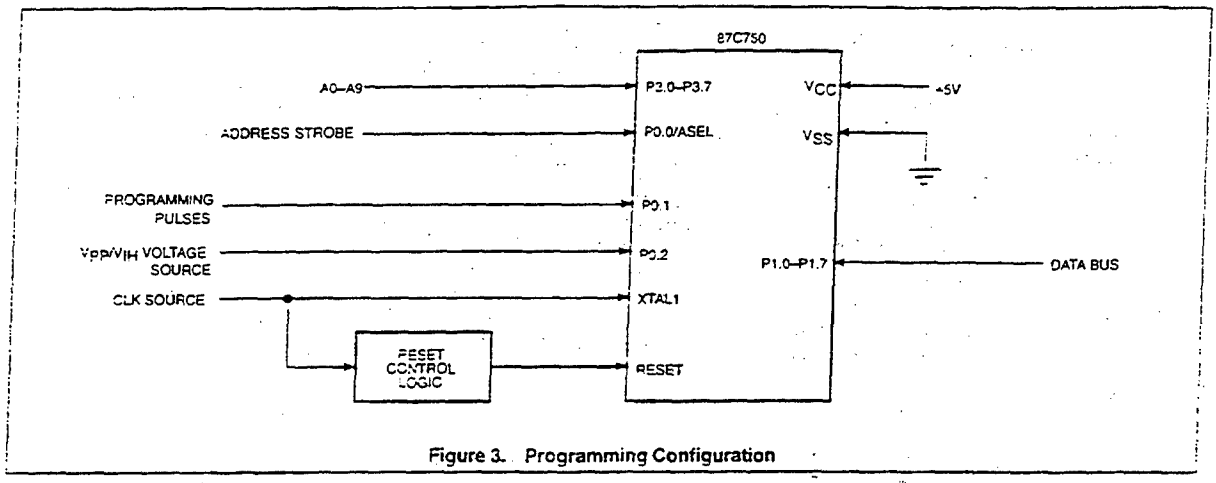


Figure 3. Programming Configuration

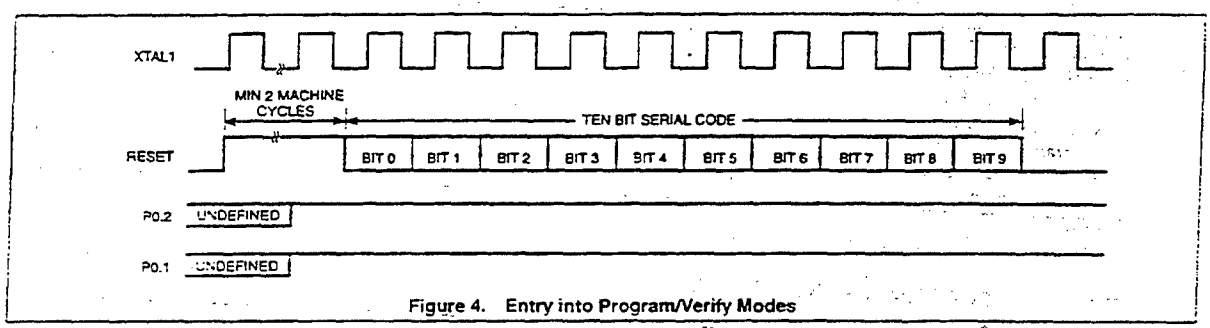


Figure 4. Entry into Program/Verify Modes

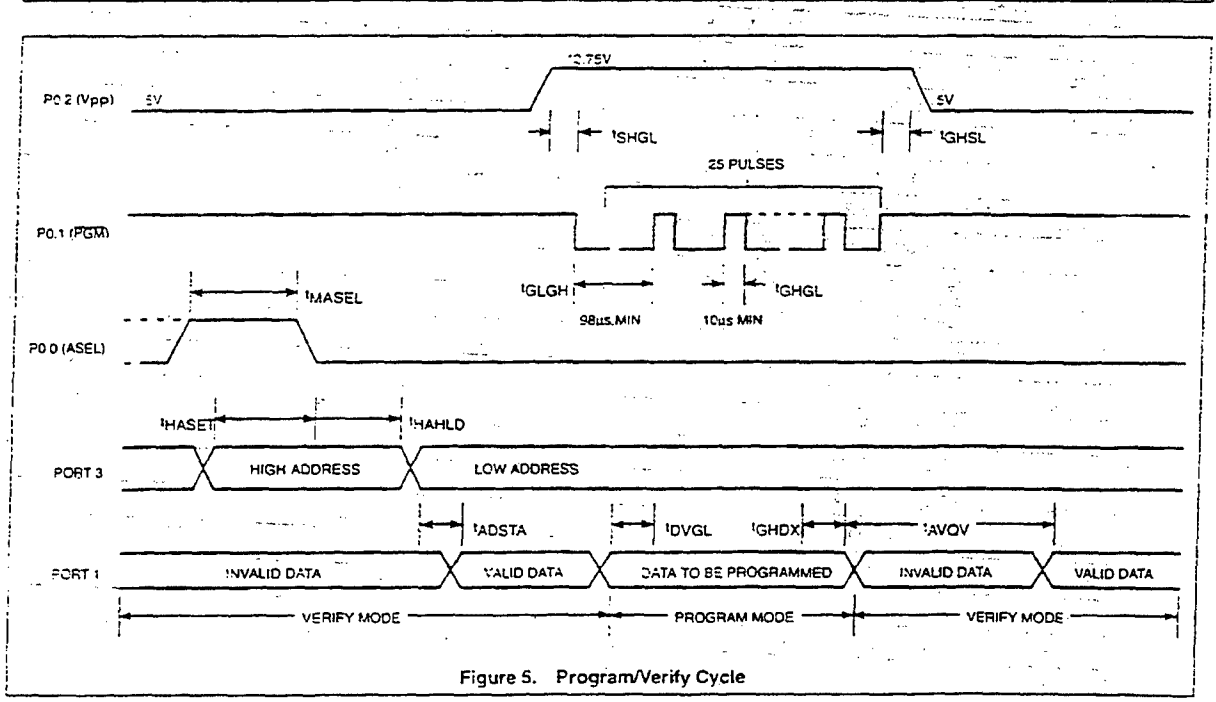


Figure 5. Program/Verify Cycle

80C51 FAMILY INSTRUCTION SET

Table 7. 80C51 Instruction Set Summary

Interrupt Response Time: Refer to Hardware Description Chapter.

Instructions that Affect Flag Settings[1]

Instruction	Flag			Instruction	Flag		
	C	OV	AC		C	OV	AC
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	CPL C,bit	X		
MUL	0	X		ANL C,/bit	X		
DIV	0	X		ANL C,bit	X		
DA	X			ORL C,/bit	X		
RRC	X			MOV C,bit	X		
RLC	X			CJNE	X		
SETB C	1						

[1]Note that operations on SFR byte address 208 or bit addresses 209-215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

Notes on instruction set and addressing modes:

Rn	Register R7-R0 of the currently selected Register Bank.
direct	8-bit internal data location's address. This could be an Internal Data RAM location (0-127) or a SFR [i.e., I/O port, control register, status register, etc. (128-255)].
@Ri	8-bit internal data RAM location (0-255) addressed indirectly through register R1 or R0.
#data	8-bit constant included in the instruction.
#data 16	16-bit constant included in the instruction
addr 16	16-bit destination address. Used by LCALL and LJMP. A branch can be anywhere within the 64k-byte Program Memory address space.
addr 11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2k-byte page of program memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to +127 bytes relative to first byte of the following instruction.
bit	Direct Addressed bit in Internal Data RAM or Special Function Register.

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
ARITHMETIC OPERATIONS				
ADD	A,Rn	Add register to Accumulator	1	12
ADD	A,direct	Add direct byte to Accumulator	2	12
ADD	A,@Ri	Add indirect RAM to Accumulator	1	12
ADD	A,#data	Add immediate data to Accumulator	2	12
ADDC	A,Rn	Add register to Accumulator with carry	1	12
ADDC	A,direct	Add direct byte to Accumulator with carry	2	12
ADDC	A,@Ri	Add indirect RAM to Accumulator with carry	1	12
ADDC	A,#data	Add immediate data to A_{CC} with carry	2	12
SUBB	A,Rn	Subtract Register from A_{CC} with borrow	1	12
SUBB	A,direct	Subtract direct byte from A_{CC} with borrow	2	12
SUBB	A,@Ri	Subtract indirect RAM from A_{CC} with borrow	1	12
SUBB	A,#data	Subtract immediate data from A_{CC} with borrow	2	12
INC	A	Increment Accumulator	1	12
INC	Rn	Increment register	1	12

Table 7. 80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
ARITHMETIC OPERATIONS (Continued)				
INC	direct	Increment direct byte	2	12
INC	@Ri	Increment indirect RAM	1	12
DEC	A	Decrement Accumulator	1	12
DEC	Rn	Decrement Register	1	12
DEC	direct	Decrement direct byte	2	12
DEC	@Ri	Decrement indirect RAM	1	12
INC	DPTR	Increment Data Pointer	1	24
MUL	AB	Multiply A and B	1	48
DIV	AB	Divide A by B	1	48
DA	A	Decimal Adjust Accumulator	1	12
LOGICAL OPERATIONS				
ANL	A,Rn	AND Register to Accumulator	1	12
ANL	A,direct	AND direct byte to Accumulator	2	12
ANL	A,@Ri	AND indirect RAM to Accumulator	1	12
ANL	A,#data	AND immediate data to Accumulator	2	12
ANL	direct,A	AND Accumulator to direct byte	2	12
ANL	direct,#data	AND immediate data to direct byte	3	24
ORL	A,Rn	OR register to Accumulator	1	12
ORL	A,direct	OR direct byte to Accumulator	2	12
ORL	A,@Ri	OR indirect RAM to Accumulator	1	12
ORL	A,#data	OR immediate data to Accumulator	2	12
ORL	direct,A	OR Accumulator to direct byte	2	12
ORL	direct,#data	OR immediate data to direct byte	3	24
XRL	A,Rn	Exclusive-OR register to Accumulator	1	12
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	12
XRL	A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	12
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	12
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	12
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	24
CLR	A	Clear Accumulator	1	12
CPL	A	Complement Accumulator	1	12
RL	A	Rotate Accumulator left	1	12
RLC	A	Rotate Accumulator left through the carry	1	12
RR	A	Rotate Accumulator right	1	12
RRC	A	Rotate Accumulator right through the carry	1	12
SWAP	A	Swap nibbles within the Accumulator	1	12
DATA TRANSFER				
MOV	A,Rn	Move register to Accumulator	1	12
MOV	A,direct	Move direct byte to Accumulator	2	12
MOV	A,@Ri	Move indirect RAM to Accumulator	1	12

Table 7. 80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
DATA TRANSFER (Continued)				
MOV	A,#data	Move immediate data to Accumulator	2	12
MOV	Rn,A	Move Accumulator to register	1	12
MOV	Rn,direct	Move direct byte to register	2	24
MOV	RN,#data	Move immediate data to register	2	12
MOV	direct,A	Move Accumulator to direct byte	2	12
MOV	direct,Rn	Move register to direct byte	2	24
MOV	direct,direct	Move direct byte to direct	3	24
MOV	direct,@Ri	Move indirect RAM to direct byte	2	24
MOV	direct,#data	Move immediate data to direct byte	3	24
MOV	@Ri,A	Move Accumulator to indirect RAM	1	12
MOV	@Ri,direct	Move direct byte to indirect RAM	2	24
MOV	@Ri,#data	Move immediate data to indirect RAM	2	12
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	24
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A_{CC}	1	24
MOVC	A,@A+PC	Move Code byte relative to PC to A_{CC}	1	24
MOVX	A,@Ri	Move external RAM (8-bit addr) to A_{CC}	1	24
MOVX	A,@DPTR	Move external RAM (16-bit addr) to A_{CC}	1	24
MOVX	A,@Ri,A	Move A_{CC} to external RAM (8-bit addr)	1	24
MOVX	@DPTR,A	Move A_{CC} to external RAM (16-bit addr)	1	24
PUSH	direct	Push direct byte onto stack	2	24
POP	direct	Pop direct byte from stack	2	24
XCH	A,Rn	Exchange register with Accumulator	1	12
XCH	A,direct	Exchange direct byte with Accumulator	2	12
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	12
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A_{CC}	1	12
BOOLEAN VARIABLE MANIPULATION				
CLR	C	Clear carry	1	12
CLR	bit	Clear direct bit	2	12
SETB	C	Set carry	1	12
SETB	bit	Set direct bit	2	12
CPL	C	Complement carry	1	12
CPL	bit	Complement direct bit	2	12
ANL	C,bit	AND direct bit to carry	2	24
ANL	C,/bit	AND complement of direct bit to carry	2	24
ORL	C,bit	OR direct bit to carry	2	24
ORL	C,/bit	OR complement of direct bit to carry	2	24
MOV	C,bit	Move direct bit to carry	2	12
MOV	bit,C	Move carry to direct bit	2	24
JC	rel	Jump if carry is set	2	24
JNC	rel	Jump if carry not set	2	24

Table 7. 80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
BOOLEAN VARIABLE MANIPULATION (Continued)				
JB	rel	Jump if direct bit is set	2	24
JNB	rel	Jump if direct bit is not set	2	24
JBC	bit,rel	Jump if direct bit is set and clear bit	3	24
PROGRAM BRANCHING				
ACALL	addr11	Absolute subroutine call	2	24
LCALL	addr16	Long subroutine call	3	24
RET		Return from subroutine	1	24
RETI		Return from interrupt	1	24
AJMP	addr11	Absolute jump	2	24
LJMP	addr16	Long jump	3	24
SJMP	rel	Short jump (relative addr)	2	24
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	24
JZ	rel	Jump if Accumulator is zero	2	24
JNZ	rel	Jump if Accumulator is not zero	2	24
CJNE	A,direct,rel	Compare direct byte to A_{CC} and jump if not equal	3	24
CJNE	A,#data,rel	Compare immediate to A_{CC} and jump if not equal	3	24
CJNE	RN,#data,rel	Compare immediate to register and jump if not equal	3	24
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	24
DJNZ	Rn,rel	Decrement register and jump if not zero	2	24
DJNZ	direct,rel	Decrement direct byte and jump if not zero	3	24
NOP		No operation	1	12

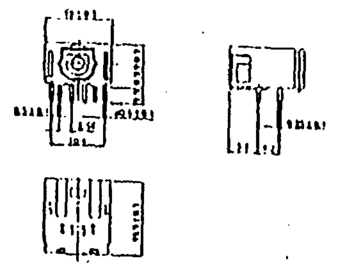
Fiber Optic Transmitting Module
TOTX195

2/15

Fiber Optic Transmitting Module for Simplex Digital signal transmission.

- Data rate : DC to 10 M b/s(NRZ code).
- Transmission distance : Up to 50 m.
- TTL interface.
- LED is driven by Differential circuit.

Unit mm



1 GND
2 Current limitting resistor of LED.
3 Vcc
4 Input
5 Non Connection.
6 Non Connection.

1. Absolute Maximum Ratings. (Ta=25℃)

Item	Symbol	Rating	Unit
Storage Temperature	T_{stg}	-40 to 85	℃
Operating Temperarure	T_{opr}	-40 to 85	℃
Supply Voltage	V_{cc}	-0.5 to 7	V
Input Voltage	V_{IN}	-0.5 to Vcc+0.5	V
Soldering Temperature	T_{sol}	260 (1)	℃

Note (1) Soldering time ≤ 3 seconds.

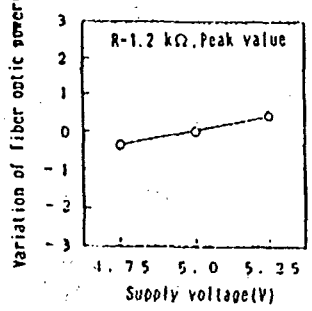
2. Electrical and Optical Characteristics. (Ta=25℃, Vcc=5V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	unit.
Data Rate		NRZ Code (1)	DC	-	10	Mb/s
Transmission Distance		Using APF (2) and TORX194	-	-	50	m
Delay Time(L→H) (3)	t_{pLH}	Using APF and TORX194	-	-	120	ns
Delay Time(H→L) (3)	t_{pHL}	Using APF and TORX194	-	-	120	ns
Pulse Width Distortion (3)	Δtw	Using APF and TORX194 Pulse width 100 ns Repetition 200ns, CL=10pF	-30	-	30	ns
Fiber Output Power	Pf	APF 2m, R=1.2kΩ (4)	-11	-	-6	dBm
Peak Emission Wavelength	λp		-	670	-	nm
Current Consumption	I_{cc}	R= 1.2kΩ	-	35	55	mA
High Level Input Voltage	V_{IH}		2.0	-	-	V
Low Level Input Voltage	V_{IL}		-	-	0.8	V
High Level Input Current	I_{IH}		-	-	20	μA
Low Level Input Current	I_{IL}		-	-	-0.4	mA

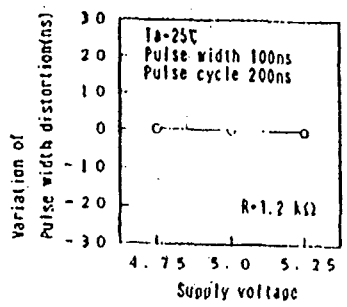
(1) LED is on when input signal is high level, it is off when low level.
(2) All Plastic fiber(980/1000μm) with polished surface.
(3) Between Input of TOTX195 and output of TORX194.
(4) Measure with a standard optical fiber with fiber optic connectors Valued by peak.

Example of Typical Characteristics

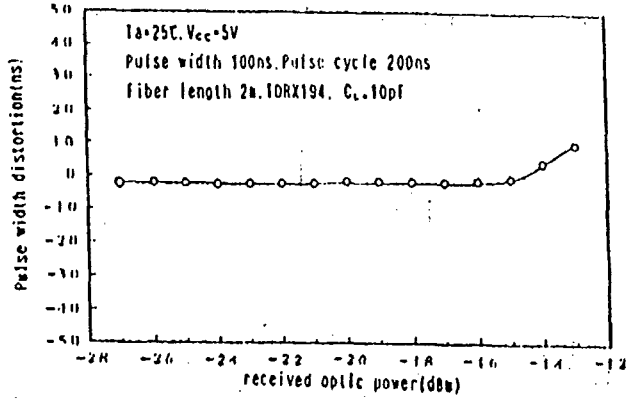
Pf vs. Supply voltage



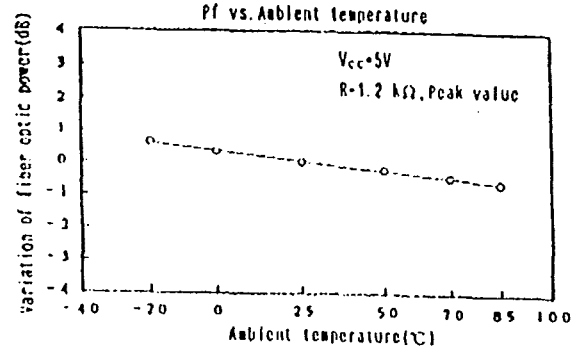
Δtw vs. Supply voltage



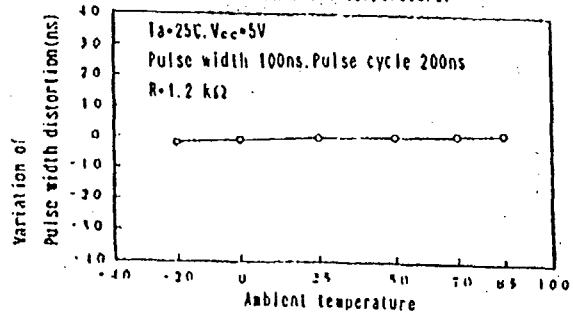
Pulse width distortion vs. Received optic power



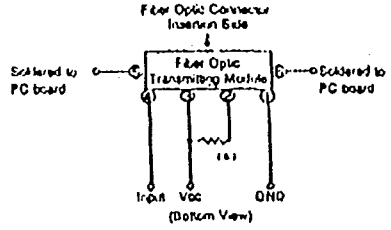
Pf vs. Ambient temperature



Δtw vs. Ambient temperature.



3. Connection Method



Note(*) Select a resistor value as follows:

Transmission Distance (m)	Resistor (Ω)
0.2 to 10	17.8 k
10 to 30	6.2 k
30 to 50	1.2 k

4. Applicable optical fiber with fiber optic connectors.

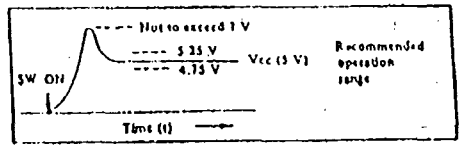
10CP100-**HB, 10CP155-**HB, 10CP100P-**HB, 10CP155P-**HB.

5. Precautions for operation.

(1) The absolute maximum ratings shows the limits, which must not be exceeded even momentarily regardless of the external condition.
Operation beyond the limit of the absolute maximum ratings may cause failure of the device.

(2) Please be sure to solder Pins No. 5 and NO.6 of TOTX195 to PC board.

(3) Power supply voltage.



(4) Do not use acid or alkaline soldering flux cleaner solvent.
Please be careful not inject the solvent into module through the fiber optic connector hole.
If some solvent happens to be injected into the module, wipe off with a cotton ball. The recommended cleaner solvent is thichrolethane.

(5) When not using the module, always provide an attached protective cap to it.

OSHIBA SEMICONDUCTOR
TECHNICAL DATA

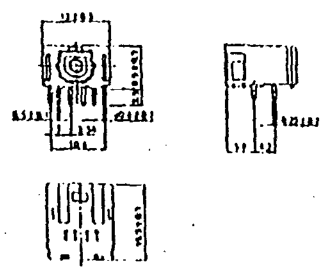
Fiber Optic Receiving Module
TORX194

2/15

Fiber Optic Receiving Module for Simplex Digital signal transmission.

- Data rate : DC to 10 M b/s(NRZ code).
- Transmission distance
  : Up to 50 m(APF).
  : Up to 1000 m(PCF).
- TTL Interface.
- ATC(Automatic Threshold Control) Circuit is used for stabilized output at a wide range of optical power level.

Unit: mm



1 Output
2 GND 1
3 Vcc
4 GND 2
5 Case
6 Case

1. Absolute Maximum Ratings(Ta=25 °C)

Item	Symbol	Rating	Unit
Strage Temperature	T_{stg}	-40 to 85	°C
Operating Temperature	T_{opr}	-40 to 85	°C
Supply Voltage	V_{cc}	-0.5 to 7	V
Low Level Output Current	I_{OL}	20	mA
High Level Output Current	I_{OH}	-1	mA
Soldering Temperature	T_{sol}	260 (1)	°C

Note (1) Soldering time ≦ 3 seconds.

TOSHIBA CORPORATION

TOSHIBA SEMICONDUCTOR
TECHNICAL DATA

TORX194

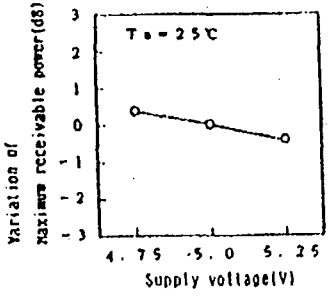
2. Electrical and Optical Characteristics (Ta=25°C, Vcc=5V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Date Date		NRZ code (1)	DC	-	10	Mb/s
Transmission Distance		Using APF (2), TODX195	0.2	-	50	m
		Using PCF (3), TODX194	0.2	-	1000	m
Delay Time(L→H)	t_{pLH}	Fiber length 2m.	-	-	120	ns
Delay Time(H→L)	t_{pHL}	Fiber length 2m.	-	-	120	ns
Pulse Width Distortion (4)	Δtw	Pulse width 100ns, Pulse cycle 200ns, C_L=10pF	-30	-	30	ns
Maximum Receivable Power (5)	P_{MAX}	10Mb/s, APF, TODX195	-14	-	-	dBm
		10Mb/s, PCF, TODX194	-18	-	-	dBm
Minimum Receivable Power (5)	P_{MIN}	10Mb/s, APF, TODX195	-	-	-27	dBm
		10Mb/s, PCF, TODX194	-	-	-29	dBm
Current Consumption	I_{cc}		-	22	40	mA
High Level Output Voltage	V_{OH}		2.7	-	-	V
Low Level Output Voltage	V_{OL}		-	-	0.4	V

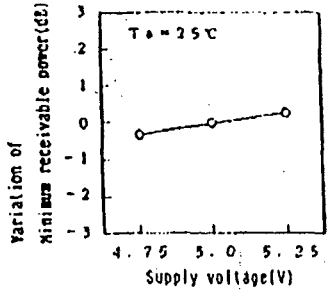
Note (1) The duty factor must be such as kept 25 to 75 %.
High level output when optical flux is received. Low level output when optical flux is not received.
(2) All Plastic fiber (980/1000 μm) with polished surface.
(3) Plastic clad silica fiber (200/300μm) with polished surface.
(4) Between input of a fiber optic transmission module and output of TORX194.
(5) BER ≦ 10^{-9}, valued by peak.

Example of Typical Characteristics

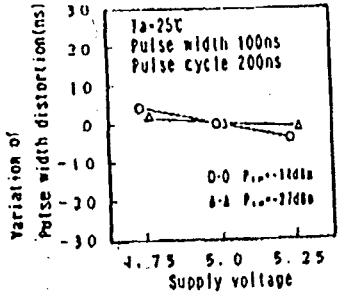
P_{MAX} vs. Supply voltage



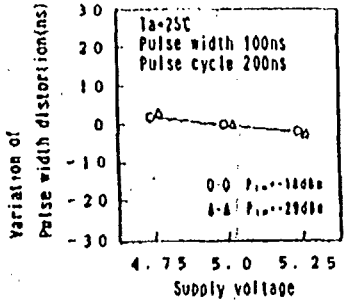
P_{MIN} vs. Supply voltage



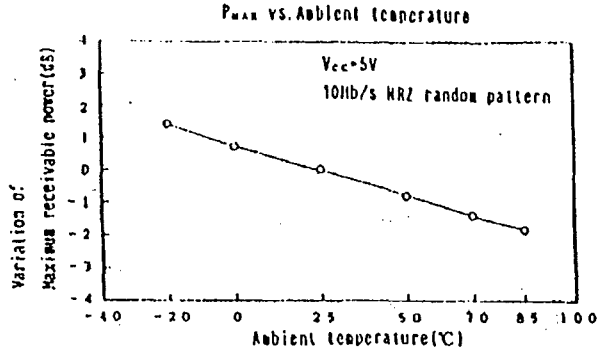
Δtw vs. Supply voltage (APf)



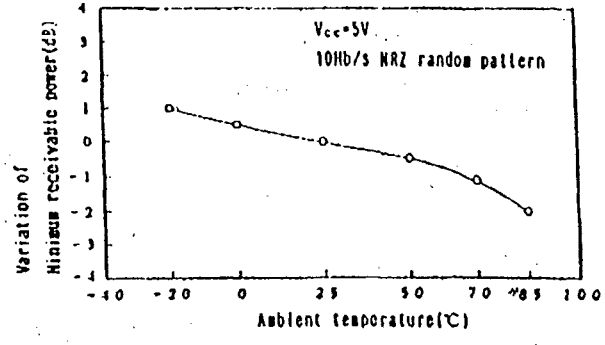
Δtw vs. Supply voltage (PCf)



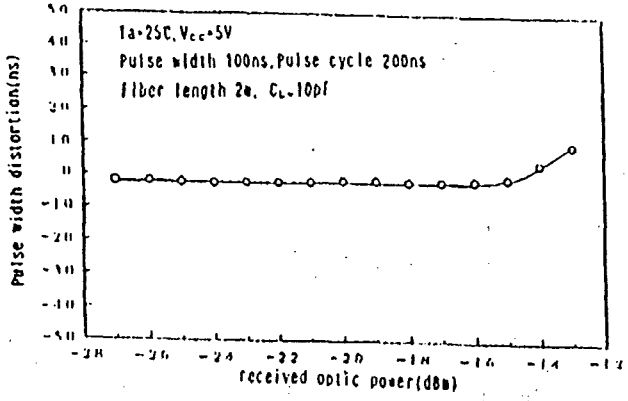
P_{MAX} vs. Ambient temperature



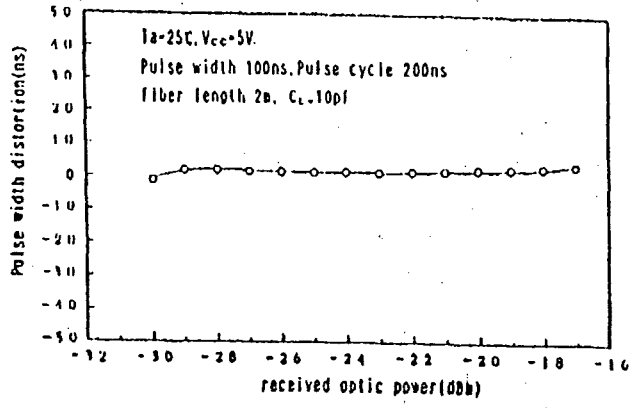
P_{MIN} vs. Ambient temperature



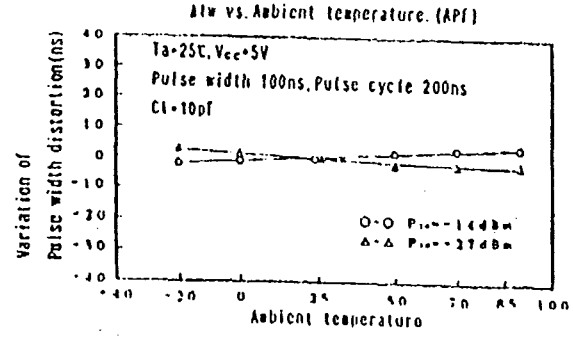
Pulse width distortion vs. Received optic power (APF)



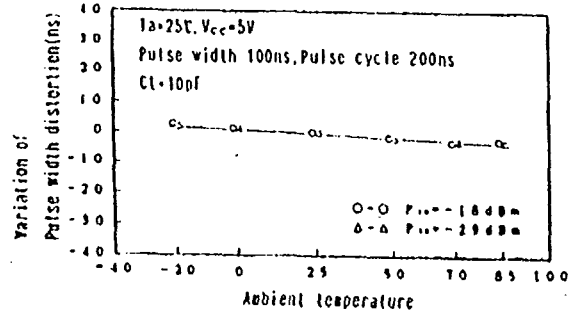
Pulse width distortion vs. Received optic power (PCF)



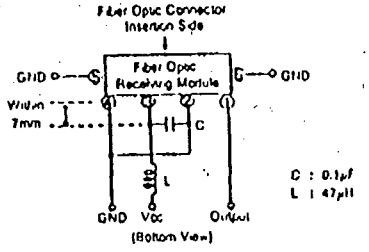
Δtw vs. Ambient temperature. (APF)



Δtw vs. Ambient temperature. (PCF)



3. Connection Method



4. Applicable optic conncal fiber with fiber optic connectors.

TOCP100-••HB, TOCP155-••HB, TOCP100P-••HB, TOCP155P-••HB(APF).
TOCP100Q-••HB, TOCP150Q-••HB, TOCP101Q-••HB, TOCP151Q-••HB, TOCP156Q-••HB
TOCP100X-••HB, TOCP150X-••HB, TOCP101X-••HB, TOCP151X-••HB, TOCP156X-••HB(PCF)

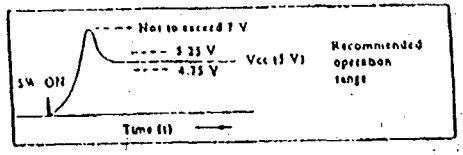
5. Precautions for operation

(1) The absolute maximum ratings show the limits, which must not be exceeded even momentarily regardless of the external condition.
Operation beyond the limit of the absolute maximum rating may cause failure of the device.

(2) Pins No.5 and No.6 of TORX194 are ground pins of housing. The housing is made of conductive plastic for shielding purpose.
Please be sure to ground these pins for efficient shielding.

(3) Additional precaution is necessary to ensure that conductive housing dose not touch other potential patterns.

(4) Power supply voltage



(5) Do not use acid or alkaline soldering flux cleaner solvent.
Please be careful not inject the solvent into module through the fiber optic connector hole.
If some solvent happens to be injected into the module, wipe it off with a cotton ball. The recommended cleaner solvent is thichrolethane.

(6) When not using the module, always provide an attached protective cap to it.

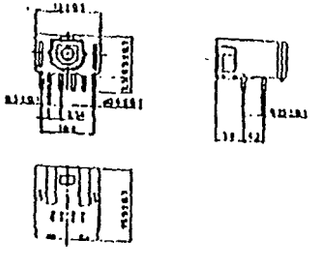
TOSHIBA SEMICONDUCTOR
TECHNICAL DATA

Fiber Optic Receiving Module
TORX194

Unit in mm

Fiber Optic Receiving Module for Simplex Digital signal transmission.

- Data rate : DC to 10 Mb/s(NRZ code).
- Transmission distance
  : Up to 50 m(APF).
  : Up to 1000 m(PCF).
- TTL Interface.
- AIC(Automatic Threshold Control) Circuit is used for stabilized output at a wide range of optical power level.



1	Output
2	GND 1
3	Vcc
4	GND 2
5	Case
6	Case

Zone Cadle Verrat
92315 SEVRES CEDEX
Yannick BAILLY
Tél. : 33 (1) 46 23 24 25
Fax : 33 (1) 45 07 21 91
Télex : 269 746 sous adresse
FR 0/46 TEKELEC

1. Absolute Maximum Ratings(Ta=25 °C)

Item	Symbol	Rating	Unit
Strage Temperature	T_{STG}	-40 to 85	°C
Operating Temperature	T_{OPR}	-40 to 85	°C
Supply Voltage	V_{CC}	-0.5 to 7	V
Low Level Output Current	I_{OL}	20	mA
High Level Output Current	I_{OH}	-1	mA
Soldering Temperature	T_{SOL}	260 (1)	°C

Note (1) Soldering time ≦ 3 seconds.

TOSHIBA CORPORATIO

2. Electrical and Optical Characteristics (Ta=25°C, Vcc=5V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Date Rate		NRZ code(3)	DC	-	10	Mb/s
Transmission Distance		Using APF (3), TOTX195	0.2	-	50	m
		Using PCF (4), TOTX194	0.2	-	1000	m
Delay Time(L→H)	t_{PLH}	Fiber length 2m.	-	-	120	ns
Delay Time(H→L)	t_{PHL}	Fiber length 2m.	-	-	120	ns
Pulse Width Distortion (2)	Δt_W	Pulse width 100ns Pulse cycle 200ns C_L=10pf	-30	-	30	ns
Maximum Receivable Power (5)	P_{MAX}	10Mb/s, APF, TOTX195	-14	-	-	dBm
		10Mb/s, PCF, TOTX194	-18	-	-	dBm
Minimum Receivable Power (6)	P_{MIN}	10Mb/s, APF, TOTX195	-	-	-27	dBm
		10Mb/s, PCF, TOTX194	-	-	-29	dBm
Current Consumption	I_{CC}		-	22	40	mA
High Level Output Voltage	V_{OH}		2.7	-	-	V
Low Level Output Voltage	V_{OL}		-	-	0.4	V

Note (2) The duty factor must be such as kept 25 to 75 %.
High level output when optical flux is received. Low level output when optical flux is not received.
(3) All Plastic Fiber (980/1000 μm) with polished surface.
(4) Plastic clad silica fiber (200/300μm) with polished surface.
(5) Between input of a fiber optic transmission module and output of TORX1
(6) BER ≦ 10^{-9}, valued by peak.

MAXIM

Precision, Quad, SPDT, CMOS Analog Switch

General Description

The MAX333A is a precision, quad, single-pole double-throw (SPDT) analog switch. The four independent switches operate with bipolar supplies ranging from ±4.5V to ±20V, or with a single-ended supply between +10V and +30V. The MAX333A offers low on resistance (less than 35Ω), guaranteed to match within 2Ω between channels and to remain flat over the full analog signal range (Δ3Ω max). It also offers break-before-make switching (10ns typical), with turn-off times less than 145ns and turn-on times less than 175ns. The MAX333A is ideal for portable operation since quiescent current runs less than 1µA with all inputs high or low.

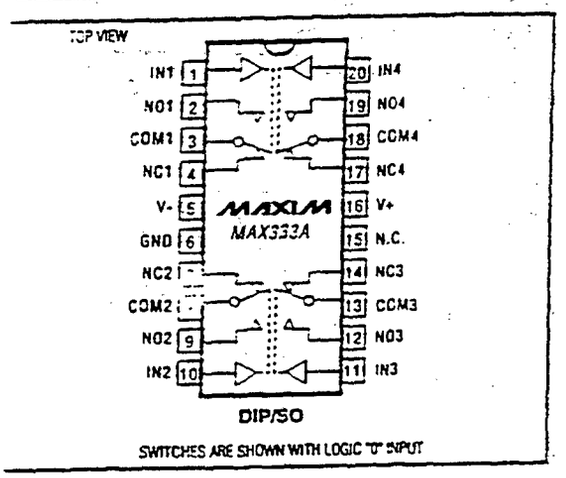
This monolithic, quad switch is fabricated with Maxim's new improved silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), low power consumption (35µW), and electrostatic discharge (ESD) greater than 2000V.

Logic inputs are TTL- and CMOS-compatible and guaranteed over a +0.8V to +2.4V range, regardless of supply voltage. Logic inputs and switched analog signals can range anywhere between the supply voltages without damage. This upgraded part is a replacement for a DG211/DG212 pair when used as a quad SPDT switch, or two DG403 dual SPDT switches.

Applications

Test Equipment
Communications Systems
PBX, PABX
Heads-Up Displays
Portable Instruments

Pin Configuration



Features

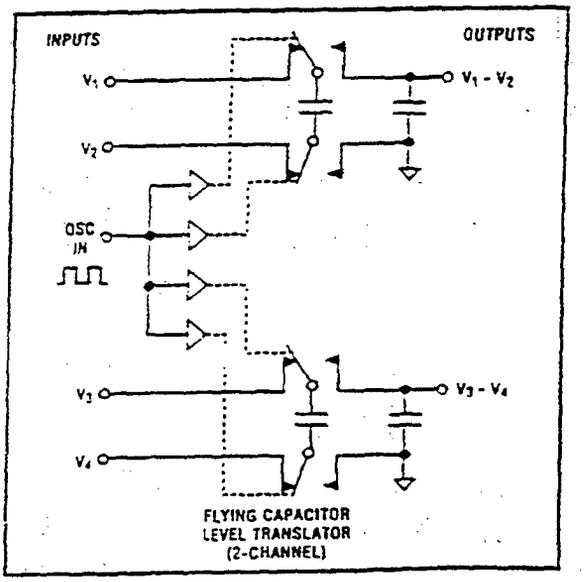
- ♦ **Upgraded Replacement for a DG211/DG212 Pair or Two DG403s**
- ♦ Low On Resistance < 22Ω Typical (35Ω Max)
- ♦ **Guaranteed Matched On Resistance Between Channels < 2Ω**
- ♦ **Guaranteed Flat On Resistance over Full Analog Signal Range Δ3Ω Max**
- ♦ **Guaranteed Charge Injection < 10pC**
- ♦ **Guaranteed Off-Channel Leakage < 6nA at +85°C**
- ♦ ESD Guaranteed > 2000V per Method 3015.7
- ♦ Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ TTL-/CMOS-Logic Compatibility
- ♦ Rail-to-Rail Analog Signal Handling Capability

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX333ACPP	0°C to +70°C	20 Plastic DIP
MAX333ACWP	0°C to +70°C	20 Wide SO
MAX333AC/D	0°C to +70°C	Dice*
MAX333AEPP	-40°C to +85°C	20 Plastic DIP
MAX333AEWP	-40°C to +85°C	20 Wide SO
MAX333AMJP	-55°C to +125°C	20 CERDIP

* *Contact factory for dice specifications.*

Typical Operating Circuit



DG444/445
Monolithic Quad SPST CMOS Analog Switches

Siliconix Incorporated

FEATURES

- ± 15 Volt Input Range
- ON Resistance < 80 Ω
- Fast Switching Action
  - t_{ON} < 160 ns
  - t_{OFF} < 80 ns
- TTL, CMOS Compatible
- DG211/DG212 Upgrades
- ESDS Protection > ± 4000 V

BENEFITS

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Simple Interfacing

APPLICATIONS

- Sample and Hold circuits
- Data Acquisition
- Automatic Test Equipment
- Audio and Video Switching
- Communication Systems
- Battery Operated Systems

DESCRIPTION

The DG444 series of monolithic quad analog switches was designed to provide high speed, low error switching of analog signals. Combining low power (< 35 microwatts) with high speed (t_{ON} < 160 ns), the DG444/445 is ideally suited for upgrading DG211/DG212 sockets. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

To achieve high-voltage ratings and superior switching performance, the DG444 series was built on Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. ON resistance is very flat over the full ±15 V analog range, rivaling JFET performance without the inherent dynamic range limitation.

The two devices in this series are differentiated by the type of switch action as shown in the functional block diagrams for each. Packaging options include the 16-pin plastic and small outline. The performance grade for this series is the Industrial, D suffix (-40 to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

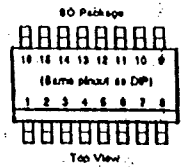
DG444

Four SPST Switches per Package

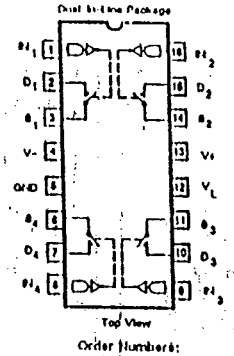
Truth Table

LOGIC	SWITCH
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V



Top View
Order Number: DG444DY



Top View
Order Numbers: DG444DJ

Preliminary

FUNCTIONAL BLOCK DIAGRAM PIN CONFIGURATION

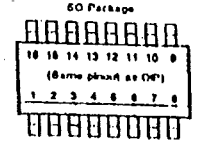
DG445

Four SPST Switches per Package

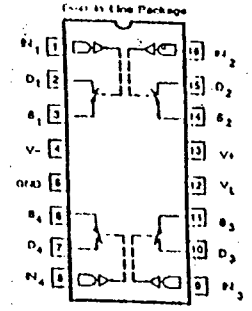
Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V



Top View
Order Number: DG445DY



Top View
Order Numbers: DG445DJ

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-
- V_+ ..... 44 V
- GND ..... 25 V
- V_L ..... (GND -0.3 V) to 44 V
- Digital Inputs V_S, V_D[†] ... (V- minus 2 V) to (V_+ plus 2 V)
  ..... or 30 mA, whichever occurs first
- Current (Any Terminal) continuous ..... 30 mA
- Current (S or D) Pulsed 1 ms, 10% duty ..... 100 mA
- Storage Temperature (D Suffix) ..... -65 to 125°C
- Operating Temperature (D Suffix) ..... -40 to 8

Power Dissipation (Package)*
- 16-Pin Plastic DIP** 450
- 16-Pin SO*** 600

* All leads welded or soldered to PC Board.
** Derate 8 mW/°C above 75°C.
*** Derate 7.6 mW/°C above 75°C.
† Signals on Sx, Dx, or INx exceeding V_+ or V- will b clamped by internal diodes. Limit forward diode current to maximum current ratings.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V_+ = 15 V, V_- = -15 V, V_L = 5 V, GND = 0 V, V_{IN} = 2.4, 0.8 V [e]	LIMITS 1=25°C 2=85°C 3=-40°C		D SUFFIX -40 to 85°C		
			TEMP	TYP[d]	MIN[f]	MAX[f]	UI
SWITCH							
Analog Signal Range[e]	V_{ANALOG}				-15	15	
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = ± 8.5 V; V_+ = 13.5 V, V_- = -13.5 V	1,3 2			80 100	
Switch OFF Leakage Current	$I_{S(OFF)}$	V_+ = 16.5 V, V_- = -16.5 V; V_D = ± 15.5 V, V_S = ± 15.5 V	1 2		-0.25 -20	0.25 20	
	$I_{D(OFF)}$		1 2		-0.25 -20	0.25 20	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_+ = 16.5 V, V_- = -16.5 V; V_S = V_D = ± 15.5 V	1 2		-0.4 -40	0.4 -40	

Preliminary

Siliconix incorporated

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15$ V, $V_- = -15$ V, $V_L = 5$ V, GND = 0 V, $V_{EI} = 2.4, 0.8$ V [e]	LIMITS 1=25°C 2=85°C 3=-40°C		D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	
INPUT							
Input Current with V_{EI} LOW	I_{IL}	V_{EI} Under Test = 0.8 V, All Other = 2.4 V	1,2		-0.6	0.6	µA
Input Current with V_{EI} HIGH	I_{IH}	V_{EI} Under Test = 2.4 V, All Other = 0.8 V	1,2		-0.6	0.6	
DYNAMIC							
Turn-ON Time	t_{ON}	$R_L = 1\ k\Omega$, $C_L = 5$ pF, See Figure 1, $V_S = \pm 10$ V	1			160	ns
Turn-OFF Time	t_{OFF}		1			80	
Charge Injection [e]	Q	$C_L = 10$ nF, $V_S = 0$ V, $V_{gen} = 0$ V, $R_{gen} = 0\ \Omega$	1		-10	10	pC
SUPPLY							
Positive Supply Current	I_+	$V_+ = 16.5$ V, $V_- = -16.5$ V, $V_{EI} = 0$ or 5 V	1 2			1 5	µA
Negative Supply Current	I_-		1 2		-1 -5		
Logic Supply Current	I_L		1 2			1 5	
Ground Current	I_{GND}		1 2		-1 -5		

ELECTRICAL CHARACTERISTICS [a] (UNIPOLAR SUPPLY)

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 12$ V, $V_- = 0$ V, $V_L = 5$ V, GND = 0 V, $V_{EI} = 2.4, 0.8$ V [e]	LIMITS 1=25°C 2=85°C 3=-40°C		D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	
SWITCH							
Analog Signal Range [e]	V_{ANALOG}				0	12	V
Drain-Source ON Resistance	$r_{DS(ON)}$	$I_S = -10$ mA, $V_D = 3$ V, 8 V, $V_+ = 10.8$ V, $V_L = 5.25$ V	1 2,3			160 200	Ω

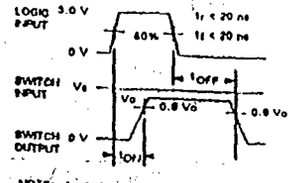
ELECTRICAL CHARACTERISTICS [a] (UNIPOLAR SUPPLY)

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 12$ V, $V_- = 0$ V, $V_L = 5$ V, GND = 0 V, $V_{EI} = 2.4, 0.8$ V [e]	LIMITS 1=25°C 2=85°C 3=-40°C		D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	
DYNAMIC							
Turn-ON Time	t_{ON}	$R_L = 1\ k\Omega$, $C_L = 35$ pF, See Figure 1, $V_S = 8$ V	1			400	ns
Turn-OFF Time	t_{OFF}		1			200	
Charge Injection [e]	Q	$C_L = 10$ nF, $V_L = 5.25$ V, $V_{gen} = 6.6$ V, $R_{gen} = 0\ \Omega$, $V_+ = 13.2$ V	1		-40	40	pC
SUPPLY							
Positive Supply Current	I_+	$V_+ = 13.2$ V, $V_{EI} = 0$ or 5 V	1 2,3			1 5	µA
Negative Supply Current	I_-	$V_{EI} = 0$ or 5 V	1 2,3		-1 -5		
Logic Supply Current	I_L	$V_L = 5.25$ V, $V_{EI} = 0$ or 5 V	1 2,3			1 5	
Ground Current	I_{GND}	$V_{EI} = 0$ or 5 V	1 2,3		-1 -5		

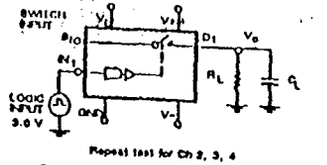
NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{EI} = input voltage to perform proper function.

SWITCHING TIME TEST CIRCUIT

V_O is the steady state output with the switch ON. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

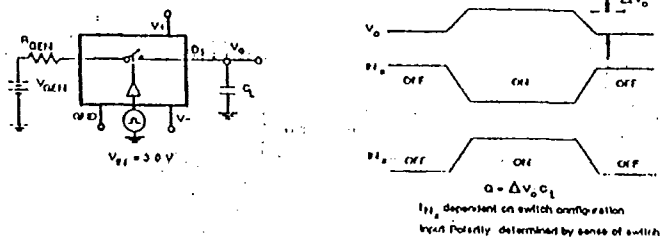


Repeat test for Ch 2, 3, 4

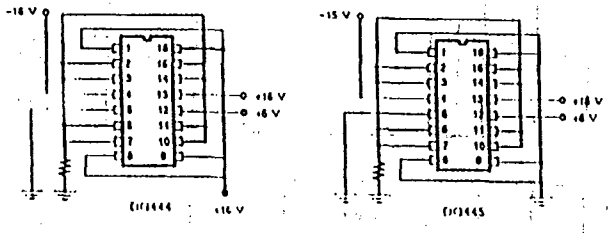
For load conditions, See Electrical Characteristics
C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

CHARGE INJECTION TEST CIRCUIT

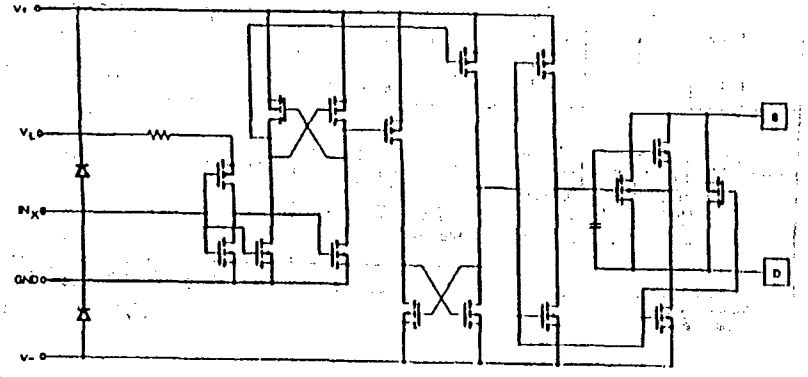


BURN-IN CIRCUITS

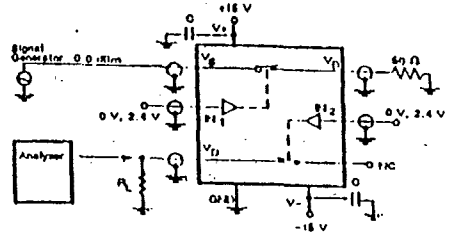


Note: All Resistors are 10 kΩ unless otherwise specified

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

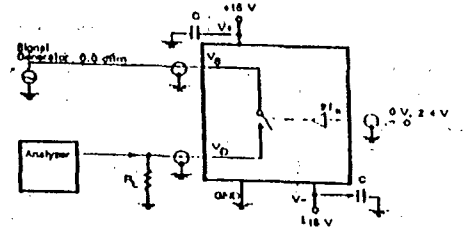


CROSSTALK TEST CIRCUIT



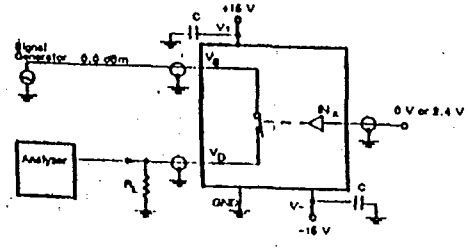
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

OFF ISOLATION TEST CIRCUIT



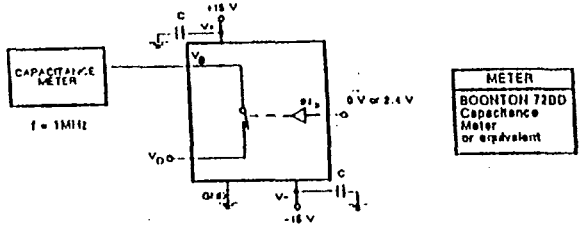
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

INSERTION LOSS TEST CIRCUIT

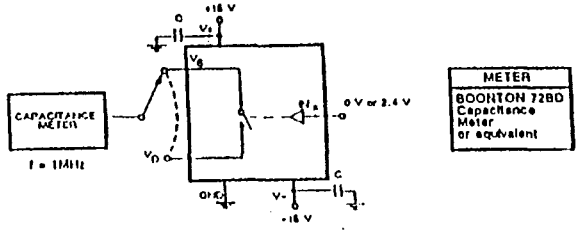


FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

SOURCE + DRAIN ON CAPACITANCE



SOURCE + DRAIN OFF CAPACITANCE



PIN DESCRIPTION

SYMBOL	DESCRIPTION
S	Analog Channel Input or Output
D	Analog Channel Output or Input
IN	Logic Control Input
V+	Positive Supply Voltage
V-	Negative Supply Voltage
GND	Digital Ground
V_L	Logic Supply Voltage

APPLICATIONS

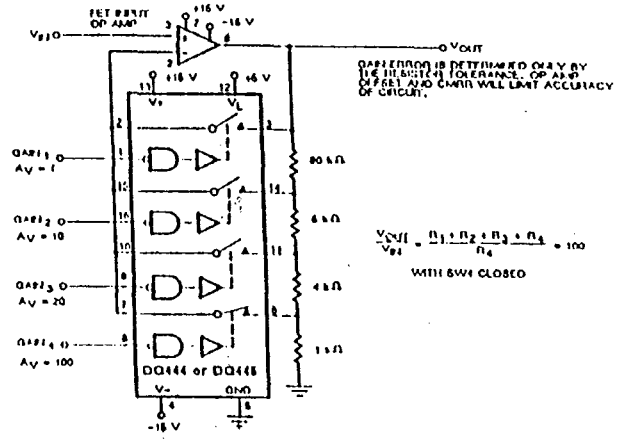


Figure 6. Precision-Weighted Resistor Programmable-Gain Amplifier

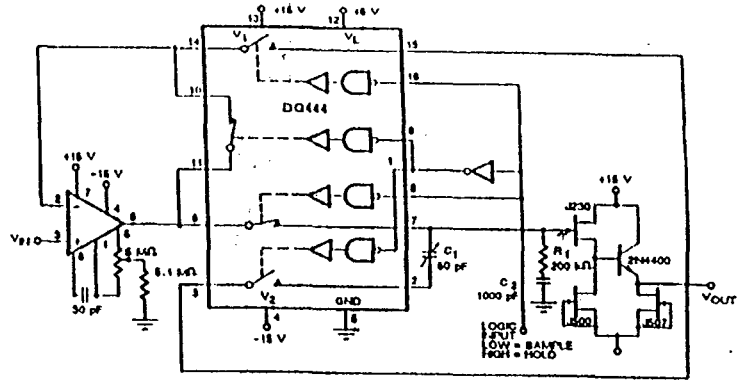
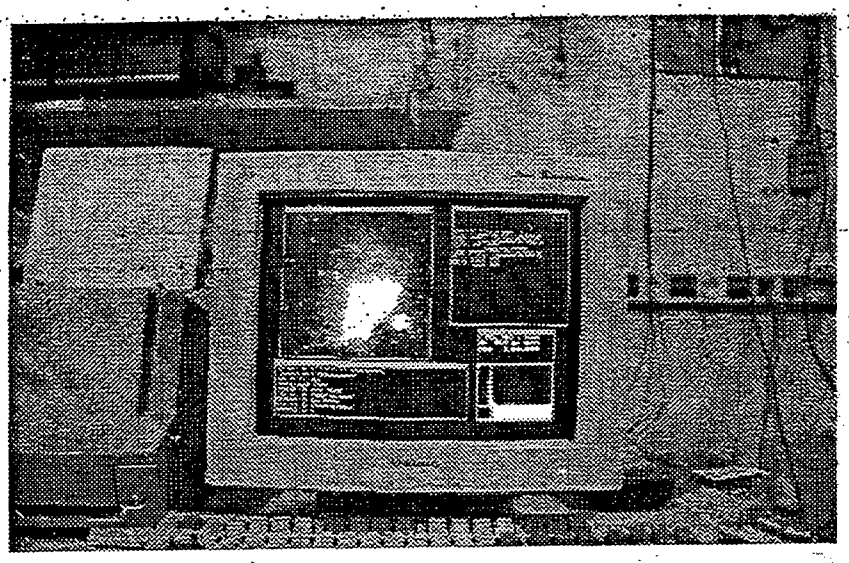


Figure 7. Precision Sample-and-Hold

Appendix 3 : 87C750 based sequencer software

In order to write this software, I used an 8051 public domain assembler which was found on Internet. It can be found at several nodes, including for example at csd4.csd.uwm.edu in the directory /pub/8051. Its author can be reached at markh@csd4.csd.uwm.edu. It seemed to us one of the best packages in its category. The distribution includes a complete documentation on the use of this assembler, and we had no problems what so ever with it.
We also purchased a Ceibo DS750 devlopement system in order to program, simulate and emulate the 87C750.In order to run the camera at the telescope we wrote a data acquisition program, of course not described here which allows to take images, while supporting the standard astronomical image standard FITS. We started to develop this program in 1992 under DOS, using a home made graphical environment. This is now quite old, and a new data acquisition program is being currently written under Windows NT and Visual C++. A typical data acquisition screen is seen above :



Listing of the current sequencer code :

```
;;_____________________________________________________________
;;
;;  CCD sequencer program - V1.0        Version du 28/04/1996
;;        Alain Maury - Herve Viot
;;        December 1994 -> November 1996
;;
;;  This version of the controller program is asynchronous, i.e.
;;  it is not synchronised using the pixel clock coming from the
;;  master board. It is to be used only in single CCD cameras.
;;
;;
;; Always remember to increase the table limit when including
;; new functions in the program
;;
;;
;;  Definition of terms
;;
;;_____________________________________________________________

;; NYI = Not Yet Implemented
;; CDL  = Comment Debug Lines


;;
;;  Definition of the I/O port bits
;;

RECV        equ         P0.0
CLOCK       equ         P0.1
SYNC        equ         P0.2

H1                  equ         P1.0
H2                  equ         P1.1
H3                  equ         P1.2
OSG                 equ         P1.3
RG                  equ         P1.4
CL1                 equ         P1.5        ;; First  clamp, first channel
CL3                 equ         P1.6        ;; Second clamp, first channel
CASC                equ         P1.7

A1                  equ         P3.0
A2                  equ         P3.1
A3                  equ         P3.2
ATGU                equ         P3.3
ATGL                equ         P3.4
CL2                 equ         P3.5
CL4                 equ         P3.6
CONV                equ         P3.7
TRANS               equ         P3.6        ;; Fiber optic emitter


;;
;;  Variables stored in Ram
;;
;;_____________________________________________________________

;; These are preloaded inside the functions
;; or by the serial link at the start of an exposure

seg data at 0

RAM                     equ       30

;; At reset, the stack is at _07_. In order to avoid conflicts between
;; the stack and this memory table, it is shifted as high as possible

C_Ln_1              equ       Ram ;; Current Line Number
C_Ln_2              equ       Ram + 1
```

```
C_Cn_1              equ     Ram + 2    ;; Current Column Number
C_Cn_2              equ     Ram + 3
C_Er_1              equ     Ram + 4    ;; Current Counter erase
C_Er_2              equ     Ram + 5
C_R_1               equ     Ram + 6    ;; Current Column Read
C_R_2               equ     Ram + 7
C_DELAY             equ     Ram + 8    ;; Constant used during vertical delays
C_Id_1              equ     Ram + 9    ;; Delay for vertical inversion
C_Id_2              equ     Ram + 10
Scan_Counter_3      equ     Ram + 11   ;; Scan High   level bit counter
Scan_Counter_2      equ     Ram + 12   ;; Scan Middle level bit counter
Scan_Counter_1      equ     Ram + 13   ;; Scan Low    level bit counter


seg code at 0

;;
;;_____________________________________________________________
;;
;; INITIALISATION ROUTINE
;;
;;     Function which load the ports with their initial values
;;  ( camera at rest ).
;;  It waits also that the data communication port goes low.
;;
;;
;;             Data in  parameters :
;;                                   none
;;
;;             Data out parameters :
;;                                   none
;;
;;      Registers used      :   A  :
;;                              R0 :
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;
;;_____________________________________________________________


Init:

            MOV         IE, #0x00       ;; Interrupts disabled
            MOV         P0, #0x07       ;; Initialise OUTPUT port
                                        ;; P0.0 & 1 as Input
                                        ;; P0.2 as Output = 1
            MOV         P1, #01100011B  ;; CL1, CL3, H1 and H2 high.
            MOV         P3, #10000000B  ;; vertical lines at zero, conv active
low

;; Debug test de la nouvelle carte horloge
;;
;;Debug_Clock:

;;          SETB        H1              ;; H1 High
;;          ACALL       Vt_Tempo
;;          SETB        H2              ;; H1 & H2 High
;;          ACALL       Vt_Tempo
;;          CLR         H1              ;; H2 High
;;          ACALL       Vt_Tempo
;;          CLR         H2              ;; everybody Low
;;          ACALL       Vt_Tempo
;;          AJMP        Debug_Clock

Init1:
```

```
                ACALL       Wait_Zero    ;; Wait the Initialisation of the PC
                                                ;; This high level is
not a command

;;
;;_____________________________________________________________
;;
;; MAIN ROUTINE
;;
;;          Function which waits for a command executes it when it is
;;            recognised - waits another when not recognised.
;;
;;      If A > table_length, AJMP Start,
;;      table length is set in memory to be 9
;;
;;
;;             Data in  parameters :
;;                                   none
;;
;;             Data out parameters :
;;                                   none
;;
;;     Registers used      :   A  : calcul of jump
;;                             R0 :
;;                             R1 :
;;                             R2 : safe of data receive
;;                             R3 :
;;                             R4 :
;;                             R5 :
;;                             R6 :
;;                             R7 :
;;
;;_____________________________________________________________

Start:

                ACALL       Comm            ;; Waiting for a command from the PC
                CLR         C               ;; Clear Carry
                SUBB        A, #0x09        ;; Substract 9 to A
                JC          Calcul_Jump     ;; --> Carry set, correct selection
                AJMP        Start           ;; Else wait a correct command

Calcul_Jump:

                MOV         A, R2           ;; Restore Comm value R2 in A
                RL          A               ;; Each jump is 2 op codes
                                            ;; Acc is now loaded with a code which
                                            ;; should be the mode in which the
                                            ;; camera is going to be used

                MOV         DPTR, #Selection
                JMP         @A+DPTR

Selection:                                  ;; CCD controller command interpreter
                                               ;; Selection table

                AJMP        Init            ;; Transmission error, return to start
                                            ;; Command 0
                AJMP        Stare_Up        ;; Stare exp. without dithered clocking AB
                                            ;; Command 1
                AJMP        Scan            ;; Scan the sky
                                            ;; Command 2
                AJMP        Stare_Ab        ;; Stare exp. with dithered clocking
                                            ;; Command 3
                AJMP        Stare_Bin       ;; Stare exp. with binning reading mode
                                            ;; Command 4
                AJMP        Temp            ;; Transmit some temperature measure
                                            ;; Command 5
                AJMP        Test_Video      ;; Test modeo
                                            ;; Command 6
                AJMP        Test            ;; Continuous CCD readout
```

```
                                        ;; Command 7
            AJMP        Low_Noise       ;; Stare exp. with low noise conversion
                                        ;; Command 8

End_Selection :                         ;; End of the jump, end of the



;;
;;_____________________________________________________________
;;
;; STARE exposure procedure using the upper amplifier
;;
;;
;;          Data in  parameters :
;;                                      none
;;
;;          Data out parameters :
;;                                      none
;;
;;     Registers used      :    A  : Command data received
;;                              R0 :
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;_____________________________________________________________


Stare_Up:

            ACALL       Erase           ;; CCD erase

Stare_Up1:

            ACALL       Comm                ;; Exposure Waiting data PC goes High
            JNZ                 Stare_Up4   ;; Retour sur erreur integration
                                            ;; sans vidage de la cam,ra

Stare_Up2:

            ACALL       Flush               ;; Vidage derniere colonne

Stare_Up3:

            ACALL       Readout_Up          ;; Lecture des pixels

Stare_Up4:

            AJMP        Temp1               ;; This is the optimized end....
                                            ;; with the ouput of the last pixel
                                            ;; and followed with an init routine



;;_____________________________________________________________
;;
;; LOW_NOISE exposure procedure using the upper amplifier
;;
;;          Data in  parameters :
;;                                      none
;;
;;          Data out parameters :
;;                                      none
;;
;;     Registers used      :    A  : Command data received
;;                              R0 :
;;                              R1 :
```

```
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;
;;_____________________________________________________________

Low_Noise:

            ACALL       Erase           ;; Erase of the CCD camera

Low_noise1:

            ACALL       Comm            ;; Exposure Waiting data PC goes High
            JNZ         Stare_Up4       ;; Retour sur erreur integration
                                        ;; sans vidage de la camra

Low_noise2:

            ACALL       Flush           ;; Vidage derniere colonne

Low_noise3:

            ACALL       Nreadout_Up     ;; Lecture des pixels sans bruit

            AJMP        Temp1               ;; This is the optimized end....


;;
;;_____________________________________________________________
;;
;; SCAN Function that read a column of pixels every 66 ms
;;
;;          This time is programmed by the PC
;;
;;
;;            Data in  parameters :
;;                                    none
;;
;;            Data out parameters :
;;                                    none
;;
;;      Registers used      :   A  :
;;                              R0 :
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;
;;_____________________________________________________________


;;
;;xxx
;;  R2 State Value    Data PC     Action
;;
;;         0              0        PC = 0 => PC indique poursuite du Scan
;;         0              1        PC = 1 => PC indique poursuite du Scan
;;                               R2 = 0 => Pas d'indication de data
;;                               Poursuite du cycle

;;         1              0        PC = 0 => PC indique poursuite du Scan
;;         1              1        PC = 1 => PC indique poursuite du Scan
;;                               R2 = 1 => Pas d'indication de data
```

```
;;                                  Arret du cycle

;;          2           0           PC = 0 => PC indique poursuite du Scan
;;          2           1           PC = 1 => PC indique poursuite du Scan
;;                                  R2 = 2 => Pas d'indication de data
;;                                  Poursuite du cycle

;;          3           0           PC = 0 => PC indique poursuite du Scan
;;          3           1           PC = 1 => PC indique poursuite du Scan
;;                                  R2 = 3 => Pas d'indication de data
;;                                  Poursuite du cycle
;;

;;          4           0           PC = 0 => PC indique poursuite du Scan
;;          4           1           PC = 1 => PC indique poursuite du Scan
;;                                  PC = 0 & R2 = 4 => PC pas pres pour
;;                                  reception DATA
;;                                    Attente liberation PC
;;                                  PC = 1 & R2 = 4 => PC pres, indication DATA
;;
;;

;;          5           0           PC = 0 => PC indique poursuite du Scan
;;          5           1           PC = 1 => PC indique arret du Scan
;;                                  R2 = 5 => Test arret Scan
;;                                  PC = 0 & R2 = 5 => PC poursuit Scan
;;                                  PC = 1 & R2 = 5 => PC stop le Scan
;;

Scan:

            SETB    TRANS ;; indicate entrance in Scan mode
            ACALL   Comm  ;; Waiting for Msb waiting counter
            INC     A     ;; A+1 to simplify tempo equation
            MOV     Scan_Counter_3, A ;; Save Msb in R5
            ACALL   Comm              ;; Waiting for Middlesb waiting counter
            INC     A     ;; A+1 to simplify tempo equation
            MOV     Scan_Counter_2, A ;; Save Middlesb in R4
            ACALL   Comm      ;; Waiting for Lsb waiting counter
            INC     A     ;; A+1 to simplify tempo equation
            MOV     Scan_Counter_1, A ;; Save Lsb in R3
            ACALL   Erase

Scan0:

            MOV   R2, #0xFF         ;; Register of the state Scan mode

Scan1_Trans0:

            CLR   TRANS           ;; Indicate data don't be read by PC
            AJMP  Pose_Scan1        ;;

Scan1_Trans1:

            SETB  Trans                 ;; Status of the sequencer = 1
            AJMP  Pose_Scan1        ;;

Pose_Scan1:

            MOV   R5, Scan_Counter_3 ;; Scan High   level bit counter
            MOV   R4, Scan_Counter_2 ;; Scan Middle level bit counter
            MOV   R3, Scan_Counter_1 ;; Scan Low    level bit counter

Pose_Scan2:

            DJNZ  R3, Pose_Scan2  ;; R3 - 1 until R3 = 0
            DJNZ  R4, Pose_Scan2  ;; R4 - 1 until R4 = 0
            DJNZ  R5, Pose_Scan2  ;; R5 - 1 until R5 = 0

Scan2:

            CLR   TRANS       ;; Indicate data must be read by PC
```

```
                INC     R2              ;; State register + 1

Scan3:                                  ;;
                                ;;
                MOV     A, R2           ;; Prepare new state value
                ANL     A, #00000011B   ;; Masque all bits without lowest 2 bits
                XCH     A, R2           ;; Save value in R2 and take old value
                ANL     A, #00000100B   ;; Masque all bits without Bit 2
                RR      A               ;; Shift right Bit 2 to Bit 1
                MOV     C, P0.0         ;; Reading the data of PC
                ADDC    A, #0           ;; ADD. R2 write flag with PC Data
                RL      A               ;; Shift left to table jump
                MOV     DPTR, #Selection_Scan ;; Initialise for table jump
                JMP     @A+DPTR         ;; Jump in the table

Selection_Scan:                 ;; CCD Scan state controler
                                ;; table of state function

                AJMP    Stop_Scan       ;; Stop the Scan mode
                                ;; Command 0
                AJMP    Run_Scan        ;; Follow the Scan mode function
                                ;; Command 1
                AJMP    Stop_Scan       ;; Stop the Scan mode
                                ;; Command 2
                AJMP    Write_Scan          ;; Transfert a colonne of pixels
                                ;; Command 3

Run_Scan:                       ;; Etat 01

                ACALL   Readout_Scan    ;; Reading of the CCD
                AJMP    Scan1_Trans0    ;; ==> Wait a pose time

Stop_Scan:                      ;; Etat 10 & 00


                SETB    Trans               ;; Status of the sequencer = 1
                AJMP    Low_noise3          ;; This is the optimized end....
                                            ;; with the ouput of the image on CCD
                                            ;; that take about 1 mn
                                            ;; and followed with an init routine

Write_Scan:                     ;; Etat 11

                ACALL   Readout_Scan    ;; Reading of the CCD
                AJMP    Scan1_Trans1    ;; ==> Wait a pose time

Readout_Scan:

                MOV     C_Ln_1, #0x01   ;; Sets one pixel to be read
                MOV     C_Ln_2, #0x01   ;;
                MOV     C_R_1 , #0x0A   ;; Vidage 2065 pixels
                MOV     C_R_2 , #0x10   ;;
                AJMP    Nvert_Scan_Up   ;;

;;
;;
;;_____________________________________________________________
;;
;; STARE BIN function wich add pixels in x and y axes
;;
;;          4 Pixels a added in only one pixel
;;      ( We never have used this function actually )
;;
;;
;;              Data in  parameters :
;;                                      none
;;
;;              Data out parameters :
;;                                      none
;;
;;      Registers used      :   A  :
;;                              R0 :
```

```
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;
;;_____________________________________________________________

Stare_Bin:

;;              ACALL       Erase
;;              AJMP        Exposure_Ab


;;
;;_____________________________________________________________
;;
;; STARE AB exposure procedure using the upper amplifier
;;
;;              Stare exposure with anti blooming
;;
;;
;;                Data in  parameters :
;;                                        none
;;
;;                Data out parameters :
;;                                        none
;;
;;       Registers used       :    A  :
;;                                 R0 :
;;                                 R1 :
;;                                 R2 :
;;                                 R3 :
;;                                 R4 :
;;                                 R5 :
;;                                 R6 :
;;                                 R7 :
;;
;;_____________________________________________________________

Stare_Ab:

                ACALL       Erase

Stare_Ab1:

                AJMP        Exposure_Ab         ;; Exposure Waiting data PC goes High
                                                ;; This is the optimized end....
                                                ;; With the read of the CCD
                                                ;; and the ouput of the last pixel
                                                ;; and followed with an init routine


;;
;;_____________________________________________________________
;;
;; TEMP Temperature readout procedure
;;
;;              Function which sets the converter in cascade mode, and
;;       starts a conversion wihch will read the temperature probe
;;       The fisrt data conversion are lost to initialise the
;;       converter, only the data issues of the second conversion
;;              are send to calculate the temperature.
;;
;;
;;                Data in  parameters :
```

```
;;                                      none
;;
;;            Data out parameters :
;;                                      none
;;
;;      Registers used      :   A  :
;;                              R0 : Number of measures
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 : temporisation counter
;;
;;_____________________________________________________________

Temp:

            SETB        Casc        ;; Puts the converter in cascade mode
            ACALL       Mes_Temp    ;; Initialise la mesure de la temperature
            SETB        Trans       ;; On valide la transmission
            ACALL       Comm        ;; Waiting the card ready

Temp1:

            ACALL       Mes_Temp    ;; Temperature readout
            AJMP        Init        ;; this is the end

Mes_Temp:

            MOV             R0 , #60  ;; 60 Measures to be done

Mes_Temp1:

            ACALL       Conv_Low_Noise      ;; Conversion and wait for low noise
            DJNZ        R0, Mes_Temp1   ;; D -> Compteur <> 0, lecture
temperature
            RET                                         ;;



;;
;;_____________________________________________________________
;;
;; TEST reading the CCD continuousl
;;
;;          are send to calculate the temperature.
;;
;;
;;            Data in  parameters :
;;                                  none
;;
;;            Data out parameters :
;;                                  none
;;
;;      Registers used      :   A  :
;;                              R0 : Number of measures
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 : temporisation counter
;;
;;_____________________________________________________________

Test:
```

```
                SETB        Trans           ;; Transmission validated

Test1:

                MOV         C_Ln_1, #0x01   ;; Sets one pixel to be read
                MOV         C_Ln_2, #0x01   ;;
                ACALL       Vert_Stare_Up   ;;
                JB                  Recv, Test1     ;; Test reception end of test
                AJMP        Init            ;; This is the end....



;;_____________________________________________________________
;;
;; Test_Video this permit to generate a video signal
;;     and make a readout conversion with low noise
;;
;;     Notice that : 0x0800 = 08 * 256 = 2048 Number of lines
;;                   0x0810 = 08 * 256 + 16 = 2064 pixels per line
;;
;;          This function transfer the lines and read all the pixels
;;     of each lines.
;;
;;
;;            Data in  parameters :
;;                                    none
;;
;;            Data out parameters :
;;                                    none
;;
;;     Registers used      :   A  :
;;                             R0 :
;;                             R1 :
;;                             R2 :
;;                             R3 :
;;                             R4 :
;;                             R5 :
;;                             R6 :
;;                             R7 :
;;
;;_____________________________________________________________

;;          P1 equal 00000110B at the beginning of this function

Test_Video:

                SETB        Trans           ;; Transmission validated
                ACALL       Comm          ;; Exposure Waiting data PC goes High
                JNZ         Test_Video7   ;; Retour sur erreur integration
                MOV         C_Ln_1, #0x08   ;; Sets the number of lines to be read
                MOV         C_Ln_2, #0x00   ;;
                XRL         P1, #00001101B ;; CL1, CL3, H2, H3 & OSG high.
                ACALL       Long_Tempo1         ;; Video … 5 V + sync. ligne

Test_Video1:

                ORL         P1, #01101000B  ;; Set CL1, CL3 & OSG
                ACALL       Tempo         ;; Waiting input clamp effect
                ANL         P1, #10010111B  ;; Reset CL1, CL3 & OSG
                MOV         A, #0x09        ;; A is used as C_R_1
;;              MOV         C_R_1, #0x09    ;; Number of pixels reset
                MOV         C_R_2, #0x10


Test_Video2:

                NOP
                NOP
                SETB        CL3
                NOP
                NOP
```

```
                CLR         CL3             ;; CL3 Low
                XRL         P1, #00000111B      ;; Change H1 -> H3
                NOP
                NOP
                ACALL       Conv_Low_Noise  ;; Conversion with low noise
                XRL         P1, #00000111B      ;; Change H1 -> H3

Test_Video3:

                DJNZ        C_R_2, Test_Video2
                CJNE        A, #9, Test_Video4
                AJMP        Test_Video5

Test_Video4:

                XRL         P1, #00000011B      ;; Change H3

Test_Video5:

                DJNZ        0E0H, Test_Video2 ;; A - 1

Test_Video6:

                DJNZ        C_Ln_2, Test_Video1
                                                    ;; Redo another line,
for 255 lines
                XRL         P1, #00000011B      ;; Change H3
                DJNZ        C_Ln_1, Test_Video1
                                                    ;; times 8 = 2048 lines

Test_Video7:

                AJMP        Temp1               ;; This is the optimized end...
                                                ;; with the ouput of the last pixel
                                                ;; and followed with an init routine


;;
;;_____________________________________________________________________
;;
;; ERASE sequence, C_Cn ( 3 x 2048 ) vertical transfert
;;
;;          Full erase sequence of the CCD and lines all erased.
;;
;;
;;            Data in  parameters :
;;                                    none
;;
;;            Data out parameters :
;;                                    none
;;
;;     Registers used      :   A  :
;;                             R0 :
;;                             R1 :
;;                             R2 :
;;                             R3 :
;;                             R4 :
;;                             R5 :
;;                             R6 :
;;                             R7 :
;;
;;_____________________________________________________________________

Erase:

                MOV         C_Er_1, #0x24   ;; C_Cn_x are loaded with CE
                MOV         C_Er_2, #0x00   ;; C_Cn_2 = 256

Lp_Eras:
```

```
                ACALL       Vt_Erase

Start_Loop_Erase:

                DJNZ        C_Er_2, Lp_Eras ;; 256 vertical transferts
                DJNZ        C_Er_1, Lp_Eras ;; x 24 = 6144 vertical transfert
                SETB        Trans           ;; On set la trans
                RET



;;
;;_____________________________________________________________________
;;
;; VIDE_HOR erase the horizontal charges during erase sequence
;;
;;          This function erase the charges of the first lines which
;;          can saturate the CCD.
;;
;;
;;            Data in  parameters :
;;                                    none
;;
;;            Data out parameters :
;;                                    none
;;
;;      Registers used      :   A  :
;;                              R0 :
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;
;;_____________________________________________________________________

Vide_Hor:

                MOV         C_Cn_1, #0x1    ;; C_Cn_x are loaded with CE
                MOV         C_Cn_2, #0x10
                AJMP        Trans_Hor           ;;



;;
;;_____________________________________________________________________
;;
;; FLUSH_SEQUENCE , C_Cn ( 3 x 2064 ) horizontal transfer
;;
;;          Notice that : 32 * 256 = 8192 > 3 * 2064 = 6192
;;
;;          This function erase the charges of the first lines before
;;     a readout sequence.
;;          For optimisation this sequence must be follwed by
;;          the Trans_Hor function.
;;
;;
;;            Data in  parameters :
;;                                    none
;;
;;            Data out parameters :
;;                                    none
;;
;;      Registers used      :   A  :
;;                              R0 :
;;                              R1 :
;;                              R2 :
```

```
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;
;;_____________________________________________________________

Flush:
;; C_Ne = 3*2048 = 6144 = 3x0x800 = 0x2400

            MOV         C_Cn_1, #0x20  ;; C_Cn_x are loaded with CE
            MOV         C_Cn_2, #0x00 ;; Poursuite sur Trans_Hor


;;
;;_____________________________________________________________
;;
;; TRANS_HOR horizontal transfer sequence
;;
;;          This function transfer the charges horizontally.
;;
;;
;;            Data in  parameters :
;;                                    none
;;
;;           Data out parameters :
;;                                    none
;;
;;      Registers used      :   A  :
;;                              R0 :
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;
;;_____________________________________________________________

Trans_Hor:

            CLR         H2              ;; 1 H2 low
            NOP
            MOV         P1, #00011101B  ;; 2 H1, H3, OSG, RG high
            MOV         P1, #00001100B  ;; 3 H1 low, RG low
            MOV         P1, #01101110B  ;; 3 H2, CL1 & CL3 high
            NOP
            MOV         P1, #00000010B  ;; 2 H3, CL1 & CL3  OSG low
            SETB        H1              ;; H1 high

Trans_Hor2:

            DJNZ        C_Cn_2, Trans_Hor  ;; 256 vertical transferts
            DJNZ        C_Cn_1, Trans_Hor  ;; x 24 = 6144 vertical transferts
            ORL                 P1, #01100000B
            RET



;;
;;_____________________________________________________________
;;
;; READOUT_UP chip full readout using the upper amplifier
;;
```

```
;;      Notice that : 0x0800 = 08 * 256 = 2048 Number of lines
;;                    0x0810 = 08 * 256 + 16 = 2064 pixels per line
;;
;;          This function transfer the lines and read all the pixels
;;      of each lines.
;;
;;
;;              Data in  parameters :
;;                                      none
;;
;;              Data out parameters :
;;                                      none
;;
;;      Registers used      :   A  :
;;                              R0 :
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;
;;_____________________________________________________________________
;;
;; Note: CL1 must be High at the entrance of this function.
;;
;;
;;
Readout_Up:

            MOV         C_Ln_1, #0x08   ;; Sets the number of lines to be read
            MOV         C_Ln_2, #0x00

Vert_Stare_Up:

            ACALL       Vt_Read         ;; Vertical transfert
            MOV         C_R_2, #0x10

Loop_Hor_Stare_Up1:

            CLR         H2              ;; 1 H2 low
            MOV         P1, #00011101B  ;; 2 H1, H3, OSG, RG high
;;          NOP
            ANL                 P1, #11101110B  ;; 3 H1, RG low
            MOV         P1, #01001110B  ;; 3 H2, CL3 high
;;          SETB        CONV            ;; End of conversion
            NOP
            CLR                 CL3             ;; CL3 Low
            MOV         P1, #00000010B  ;; 2 H3, OSG
            NOP
            CLR         CONV            ;; Start conversion
            NOP
            SETB        CONV            ;; End of conversion
            SETB        H1                      ;; H1 High
            DJNZ        C_R_2, Loop_Hor_Stare_Up1

Loop_Hor_Stare_Up2:

            CLR         H2              ;; 1 H2 low
            MOV         P1, #00011101B  ;; 2 H1, H3, OSG, RG high
;;          NOP
            ANL                 P1, #11101110B  ;; 3 H1, RG low
            MOV         P1, #01001110B  ;; 3 H2, CL3 high
;;          SETB        CONV            ;; End of conversion
            NOP
            CLR          CL3             ;; CL3 Low
            MOV         P1, #00000010B  ;; 2 H3, OSG
            NOP
            CLR         CONV            ;; Start conversion
            NOP
            SETB        CONV            ;; End of conversion
```

```
                SETB        H1                          ;; H1 High
                DJNZ        C_R_2, Loop_Hor_Stare_Up2

Loop_Hor_Stare_Up3:

                CLR         H2              ;; 1 H2 low
                MOV         P1, #00011101B  ;; 2 H1, H3, OSG, RG high
;;              NOP
                ANL          P1, #11101110B  ;; 3 H1, RG low
                MOV         P1, #01001110B  ;; 3 H2, CL3 high
;;              SETB        CONV            ;; End of conversion
                NOP
                CLR          CL3             ;; CL3 Low
                MOV         P1, #00000010B  ;; 2 H3, OSG
                NOP
                CLR         CONV            ;; Start conversion
                NOP
                SETB        CONV            ;; End of conversion
                SETB        H1                          ;; H1 High
                DJNZ        C_R_2, Loop_Hor_Stare_Up3

Loop_Hor_Stare_Up4:

                CLR         H2              ;; 1 H2 low
                MOV         P1, #00011101B  ;; 2 H1, H3, OSG, RG high
;;              NOP
                ANL          P1, #11101110B  ;; 3 H1, RG low
                MOV         P1, #01001110B  ;; 3 H2, CL3 high
;;              SETB        CONV            ;; End of conversion
                NOP
                CLR              CL3             ;; CL3 Low
                MOV         P1, #00000010B  ;; 2 H3, OSG
                NOP
                CLR         CONV            ;; Start conversion
                NOP
                SETB        CONV            ;; End of conversion
                SETB        H1                          ;; H1 High
                DJNZ        C_R_2, Loop_Hor_Stare_Up4

Loop_Hor_Stare_Up5:

                CLR         H2              ;; 1 H2 low
                MOV         P1, #00011101B  ;; 2 H1, H3, OSG, RG high
;;              NOP
                ANL          P1, #11101110B  ;; 3 H1, RG low
                MOV         P1, #01001110B  ;; 3 H2, CL3 high
;;              SETB        CONV            ;; End of conversion
                NOP
                CLR              CL3             ;; CL3 Low
                MOV         P1, #00000010B  ;; 2 H3, OSG
                NOP
                CLR         CONV            ;; Start conversion
                NOP
                SETB        CONV            ;; End of conversion
                SETB        H1                          ;; H1 High
                DJNZ        C_R_2, Loop_Hor_Stare_Up5

Loop_Hor_Stare_Up6:

                CLR         H2              ;; 1 H2 low
                MOV         P1, #00011101B  ;; 2 H1, H3, OSG, RG high
;;              NOP
                ANL              P1, #11101110B  ;; 3 H1, RG low
                MOV         P1, #01001110B  ;; 3 H2, CL3 high
;;              SETB        CONV            ;; End of conversion
                NOP
                CLR              CL3             ;; CL3 Low
                MOV         P1, #00000010B  ;; 2 H3, OSG
                NOP
                CLR         CONV            ;; Start conversion
                NOP
                SETB        CONV            ;; End of conversion
```

```
                SETB        H1                          ;; H1 High
                DJNZ        C_R_2, Loop_Hor_Stare_Up6

Loop_Hor_Stare_Up7:

                CLR         H2              ;; 1 H2 low
                MOV         P1, #00011101B  ;; 2 H1, H3, OSG, RG high
;;              NOP
                ANL                 P1, #11101110B  ;; 3 H1, RG low
                MOV         P1, #01001110B  ;; 3 H2, CL3 high
;;              SETB        CONV            ;; End of conversion
                NOP
                CLR                 CL3             ;; CL3 Low
                MOV         P1, #00000010B  ;; 2 H3, OSG
                NOP
                CLR         CONV            ;; Start conversion
                NOP
                SETB        CONV            ;; End of conversion
                SETB        H1                          ;; H1 High
                DJNZ        C_R_2, Loop_Hor_Stare_Up7

Loop_Hor_Stare_Up8:

                CLR         H2              ;; 1 H2 low
                MOV         P1, #00011101B  ;; 2 H1, H3, OSG, RG high
;;              NOP
                ANL                 P1, #11101110B  ;; 3 H1, RG low
                MOV         P1, #01001110B  ;; 3 H2, CL3 high
;;              SETB        CONV            ;; End of conversion
                NOP
                CLR                 CL3             ;; CL3 Low
                MOV         P1, #00000010B  ;; 2 H3, OSG
                NOP
                CLR         CONV            ;; Start conversion
                NOP
                SETB        CONV            ;; End of conversion
                SETB        H1                          ;; H1 High
                DJNZ        C_R_2, Loop_Hor_Stare_Up8

Loop_Hor_Stare_Up9:

                CLR         H2              ;; 1 H2 low
                MOV         P1, #00011101B  ;; 2 H1, H3, OSG, RG high
;;              NOP
                ANL         P1, #11101110B  ;; 3 H1, RG low
                MOV         P1, #01001110B  ;; 3 H2, CL3 high
;;              SETB        CONV            ;; End of conversion
                NOP
                CLR         CL3             ;; CL3 Low
                MOV         P1, #00000010B  ;; 2 H3, OSG
                NOP
                CLR         CONV            ;; Start conversion
                NOP
                SETB        CONV            ;; End of conversion
                SETB        H1                          ;; H1 High
                DJNZ        C_R_2, Loop_Hor_Stare_Up9

                DJNZ        C_Ln_2, suite1
                AJMP        suite2              ;; Redo another line, for 255 lines

suite1:

                AJMP        Vert_Stare_Up

suite2:

                DJNZ        C_Ln_1, suite1  ;; times 8 = 2048 lines
                RET                         ;; return from subroutine


;;Readout_Up:
;;
```

```
;;            MOV         C_Ln_1, #0x08   ;; Sets the number of lines to be read
;;            MOV         C_Ln_2, #0x00
;;
;;Vert_Stare_Up:
;;
;;            ACALL       Vt_Read         ;; Vertical transfert
;;            MOV         C_R_1, #0x09    ;; Number of pixels reset
;;            MOV         C_R_2, #0x10
;;
;;Loop_Hor_Stare_Up:
;;
;;            CLR         H2              ;; 1 H2 low
;;            MOV         P1, #00011101B  ;; 2 H1, H3, OSG, RG high
;;            ANL          P1, #11101110B  ;; 3 H1, RG low
;;            MOV         P1, #01001110B  ;; 3 H2, CL3 high
;;;;          NOP                         ;;
;;            SETB        CONV            ;; End of conversion
;;            CLR          CL3             ;; CL3 Low
;;            MOV         P1, #00000010B  ;; 2 H3, OSG
;;            CLR         CONV            ;; Start conversion
;;            SETB        H1                      ;; H1 High
;;
;;Start_Loop_Hor_Stare_Up:
;;
;;            DJNZ        C_R_2, Loop_Hor_Stare_Up
;;            DJNZ        C_R_1, Loop_Hor_Stare_Up
;;
;;Start_Loop_Vert_Stare_Up:
;;
;;            DJNZ        C_Ln_2, Vert_Stare_Up
;;                                                ;; Redo another line,
for 255 lines
;;            DJNZ        C_Ln_1, Vert_Stare_Up
;;                                                ;; times 8 = 2048 lines
;;
;;            RET     ;; return from subroutine
;;


;;
;;_____________________________________________________________
;;
;; NREADOUT_UP chip full readout using the upper amplifier
;;  This sequence is the same as NREADOUT_UP but with less noise
;;
;;      Notice that : 0x0800 = 08 * 256 = 2048 Number of lines
;;                    0x0810 = 08 * 256 + 16 = 2064 pixels per line
;;
;;           This function transfer the lines and read all the pixels
;;      of each lines.
;;
;;
;;             Data in  parameters :
;;                                    none
;;
;;             Data out parameters :
;;                                    none
;;
;;      Registers used      :   A  :
;;                              R0 :
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;
;;_____________________________________________________________

Nreadout_Up:
```

```
                MOV         C_Ln_1, #0x08   ;; Sets the number of lines to be read
                MOV         C_Ln_2, #0x00

Nvert_Stare_Up:

                MOV         C_R_1, #0x09    ;; Number of pixels reset
                MOV         C_R_2, #0x10

Nvert_Scan_Up:

                ACALL       Vt_Read         ;; Vertical transfert

Nloop_Hor_Stare_Up:

                CLR         H2              ;; 1 H2 low
                NOP
                MOV         P1, #00011101B  ;; 2 H1, H3, OSG, RG high
                MOV         P1, #00001100B  ;; 3 H1, RG low
                MOV         P1, #01001110B  ;; 3 H2, CL3 high
                NOP
                NOP
                CLR          CL3             ;; CL3 Low
                MOV         P1, #00000010B  ;; 2 H3, OSG
                NOP
                NOP
                ACALL        Conv_Low_Noise  ;; Conversion with low noise
                SETB        H1                          ;; H1 High

Nstart_Loop_Hor_Stare_Up:

                DJNZ        C_R_2, Nloop_Hor_Stare_Up
                DJNZ        C_R_1, Nloop_Hor_Stare_Up

Nstart_Loop_Vert_Stare_Up:

                DJNZ        C_Ln_2, Nvert_Stare_Up
                                                ;; Redo another line, for 255 lines
                DJNZ        C_Ln_1, Nvert_Stare_Up
                                                ;; times 8 = 2048 lines

                RET                         ;; return from subroutine


;;
;;_____________________________________________________________________
;;
;; Conv_Low_Noise function which execute a starting conversion
;;     and wait to make the minimum noise as possible
;;
;;
;;              Data in  parameters :
;;                                      none
;;
;;              Data out parameters :
;;                                      none
;;
;;       Registers used       :   A  :
;;                                R0 :
;;                                R1 :
;;                                R2 :
;;                                R3 :
;;                                R4 :
;;                                R5 :
;;                                R6 :
;;                                R7 :
;;
;;_____________________________________________________________________

Conv_Low_Noise:

                CLR         CONV            ;; Start conversion
```

```
                ACALL       Temp_Less_Noise ;; Temporisation for less noise sequence
                SETB        CONV            ;; End of conversion    *
                RET

;;
;;_____________________________________________________________________
;;
;; VT_ERASE function which execute an vertical transfer
;;

;;
;;     During readout using the upper amplifier, the charges are
;;     transfered in the 2->1->3->2->1->ATGU direction.
;;           ATGL = 0.
;;
;;
;;             Data in  parameters :
;;                                        none
;;
;;             Data out parameters :
;;                                        none
;;
;;      Registers used       :   A  :
;;                               R0 :
;;                               R1 :
;;                               R2 :
;;                               R3 :
;;                               R4 :
;;                               R5 :
;;                               R6 :
;;                               R7 :
;;
;;_____________________________________________________________________

Vt_Erase:

                SETB        A1                  ;; A1 High
                ACALL       Vide_Hor
                SETB        A3                  ;; A1 & A3 High
                ACALL       Vide_Hor
                CLR         A1                  ;; A3 High
                ACALL       Vide_Hor
                SETB        A2                  ;; A2 & A3 High
                ACALL       Vide_Hor
                CLR         A3                  ;; A2 High
                ACALL       Vide_Hor
                CLR         A2                  ;; Every body Low
                RET


;;
;;_____________________________________________________________________
;;
;; VT_READ function which execute an vertical transfer
;;
;;
;;          During readout using the upper amplifier, the charges are
;;     transfered in the 2->1->3->2->1->ATGU direction.
;;           ATGL = 0.
;;
;;
;;             Data in  parameters :
;;                                        none
;;
;;             Data out parameters :
;;                                        none
;;
;;      Registers used       :   A  :
```

```
;;                              R0 :
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;
;;_____________________________________________________________

Vt_Read:

            SETB        CL1             ;; Clamp High
            SETB        A1              ;; A1 High
            ACALL       Vt_Tempo
            SETB        A3              ;; A1 & A3 High
            ACALL       Vt_Tempo
            CLR               A1        ;; A3 High
            ACALL       Vt_Tempo
            SETB        A2              ;; A2 & A3 High
            ACALL       Vt_Tempo
            CLR               A3        ;; A2 High
            ACALL       Vt_Tempo
            CLR         A2              ;; Every body Low
            CLR         CL1             ;; Clamp Low
            RET


;;
;;_____________________________________________________________
;;
;; EXPOSURE_AB exposure with the anti_blooming mode
;;
;;
;;          This function does periodic A1 and A2 inversions while
;;     checking the end flag exposure.
;;          Line inversion frequency = 300 Hz, C_ID = 2300 = 0x08FC
;;
;;
;;            Data in  parameters :
;;                                  none
;;
;;            Data out parameters :
;;                                  none
;;
;;      Registers used      :   A  :
;;                              R0 :
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;
;;_____________________________________________________________

Exposure_Ab:

            ACALL       Vli             ;; Vertical line inversion
            MOV         C_Id_1,#0x09
            MOV         C_Id_2,#0xFC

Delay_Stare_1:

            DJNZ        C_Id_2, Delay_stare_1
            DJNZ        C_Id_1, Delay_stare_1
```

```
                JNB         RECV, Exposure_Ab ;; continue

End_Expo:

;;              AJMP        Stare_Up1     ;; Gestion comm et gestion du vidage
                AJMP        Low_noise1       ;; Gestion comm et gestion du vidage
                            ;; avec faible bruit de lecture


;;
;;_____________________________________________________________
;;
;; Vli vertical line inversion
;;
;;
;;          This function does periodic A1 and A2 for the
;;      anti_blooming mode.
;;
;;
;;            Data in  parameters :
;;                                    none
;;
;;            Data out parameters :
;;                                    none
;;
;;      Registers used      :   A  :
;;                              R0 :
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;
;;_____________________________________________________________

Vli:

            MOV         C, A1           ;; Set carry bit if P3.0 == 1
            ORL          P3, #00000011B  ;; A1 and A2 set high
            ACALL        Vt_Tempo       ;; Waiting routine R7 = 0x30
            MOV         A2,C            ;; A2 is set to A1 former's value.
            CPL         C               ;; Carry bit complement
            MOV         A1,C            ;; A1 is inverted
            RET                         ;; return from subroutine


;;
;;_____________________________________________________________
;;
;; Temp_Less_Noise tempo. to noiseless readout conversion
;;
;;
;;          This function use the tempo function with R7 = 9
;;          to wait a readout pixels time of 5 us.

;;
;;
;;            Data in  parameters :
;;                                    none
;;
;;            Data out parameters :
;;                                    none
;;
;;      Registers used      :   A  :
;;                              R0 :
;;                              R1 :
;;                              R2 :
```

```
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 : Tempo counter
;;
;;_____________________________________________________________

Temp_Less_Noise:
;; Delay during vertical transfert

            MOV          R7, #0x03
            AJMP        Tempo1        ;; Loops three times then exit



;;
;;_____________________________________________________________
;;
;; VT_TEMPO temposisation for the vertical transfer
;;
;;
;;          This function use the tempo function with R7 = 30
;;          without reading the pixels.
;;
;;
;;            Data in  parameters :
;;                                    none
;;
;;            Data out parameters :
;;                                    none
;;
;;      Registers used      :   A  :
;;                              R0 :
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 : Tempo counter
;;
;;_____________________________________________________________

Vt_Tempo:
;; Delay during vertical transfert

            MOV          R7, #0x30
            AJMP        Tempo1        ;; Loops three times then exit


;;_____________________________________________________________
;;
;; TEMPO general temporisation for the sequencer
;;
;;          This function use the tempo function with R7 = FF.
;;
;;
;;            Data in  parameters :
;;                                    none
;;
;;            Data out parameters :
;;                                    none
;;
;;      Registers used      :   A  :
;;                              R0 :
;;                              R1 :
;;                              R2 :
;;                              R3 :
```

```
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 : Tempo counter
;;
;;_____________________________________________________________________


Tempo:
;; Delay during vertical transfert

            MOV          R7, #0xFF
Tempo1:
            DJNZ        R7, Tempo1      ;; Loops three times then exit
            RET
;; return from subroutine



;;
;;_____________________________________________________________________
;;
;; LONG_TEMPO1 general temporisation for the sequencer
;;
;;          This function use the tempo function with R7 = FF.
;;
;;
;;            Data in  parameters :
;;                                    none
;;
;;            Data out parameters :
;;                                    none
;;
;;      Registers used      :   A  :
;;                              R0 :
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 : Tempo counter
;;
;;_____________________________________________________________________


Long_Tempo1:
;; Delay during vertical transfert

            MOV          R6, #0x0A

Long_Tempo2:
;; Delay during vertical transfert

            ACALL        Tempo
            DJNZ        R6, Long_Tempo2 ;; Loops three times then exit
            RET
;; return from subroutine



;;
;;_____________________________________________________________________
;;
;; ERROR general function wich treat the errors
;;
;;
;;          This function must return A = 0 to indicate an error
;;          of transmission or command.
;;          This function is in comments because it take some place
```

```
;;          and it is not useful in the real application.
;;          We can validate it to debug temporarely.
;;
;;
;;            Data in  parameters :
;;                                  none
;;
;;            Data out parameters :
;;                                  none
;;
;;      Registers used      :   A  : Transmission Return code
;;                              R0 :
;;                              R1 :
;;                              R2 : Data received is also 0
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;
;;_____________________________________________________________________

Error:

;;          XRL         P1, #10000000B  ;; D Set P1.7 Indicate an Error
;;          ACALL       TEMPO           ;; D Wait for the visualisation
;;          XRL         P1, #10000000B  ;; D Reset P1.7 after the error
            CLR         A               ;; Data receive is 00
            MOV         R2, A          ;; Sets R2 to 0 initialisation
            RET                       ;;



;;
;;_____________________________________________________________________
;;
;; COMM communication routine with the PC
;;
;;
;; Function which receive commands to the host and permits to
;; run the appropriate routine after a correct reception
;;    This function must be followed by the Wait_Zero function.
;;
;;      Communication between the PC and the sequencer is made
;;      in Pulse Width Modulated mode ( PWM ). Is it a single
;;      wire communication protocol. Bits are transmitted in a
;;      three step process. First communication bit is set,
;;      second it is either set or cleared, depending on whether
;;      the bit is high or low, and finally, the communication
;;      bit is cleared. in order to decode the bit, the program
;;      counts the time when the communication is high and compares
;;      it to the time it is low. If the first is larger than the
;;      second, then the bit is a 1, otherwise it is a zero. Bits
;;      are rotated right in  a storage register, which after 8
;;      bits contains the transmitted byte. It is stored in Acc
;;      before returning.
;;
;;                  _|‾‾|____|‾        This is a zero
;;
;;                  _|‾‾‾‾‾|__|‾       This is a one
;;
;;                   |  |  |  |        The three time intervals
;;                                     taken into consideration
;;
;;      There is a stop bit which is used to end the communication.
;;      In case of transmission error or timeout, the function
;;      jump to the ERROR function that wait data goes low and
;;      return with the falag A = 0 and data received R2 = 0.
;;
```

```
;;              Data in  parameters :
;;                                   none
;;
;;              Data out parameters :
;;                                 none ( Return after the
;;                                        reception of a data or
;;                                        time_out on single level
;;
;;                                 Register A : Data received
;;                                              or 0 if error
;;
;;      Registers used      :    A  : Counter of high data level
;;                               R0 : Counter of low level
;;                               R1 : Counter of bits received
;;                               R2 : Byte received
;;                               R3 :
;;                               R4 :
;;                               R5 :
;;                               R6 :
;;                               R7 :
;;
;;_____________________________________________________________

Comm:
;; Waiting for communication start

;;      XRL         P1, #00000010B  ;; D Indicate waiting start
        MOV         R1, #0x08       ;; Sets R1 to 8 ( bit counter )
                                                    ;; in case of error

Wait_Comm:
;; Wait comm start

        JNB         RECV, Wait_Comm ;; --> While Recv equals zero, wait
                                                          ;; byte
;;      XRL         P1, #00000010B  ;; D Indicate start reception

Start_Comm:
;; Bits are coming !

        CLR         A                   ;; Clear acc. counter high level
        MOV         R0, A           ;; Clear R0 counter low level

Bit_High:                           ;; Recv is now high

        DJNZ        0E0H, Bit_High1 ;; --> Acc -1, test data if != 0
        AJMP        Error           ;; --> Time out high level

Bit_High1:

;;      AJMP        Bit_High        ;; D Test the high level timeout
        JB          RECV, Bit_High  ;; --> Carry is high

Bit_Low:                            ;; Carry just turned low

        DJNZ        R0, Bit_Low1    ;; --> R0 -1, test data if != 0
        AJMP        Error           ;; --> Time out low level

Bit_Low1:

        JNB         RECV, Bit_Low   ;; --> Carry is low

Calculate :                         ;; Carry now high, bit transfered

;;      XRL         P1, #00000100B  ;; D Indicate the end of a bit
        CLR         C               ;; Clear Carry
        SUBB        A, R0           ;; soustract both counts
        MOV         A, R2           ;; R2 ( temp. reception byte ) into acc
        RRC         A               ;; rotate right through carry
        MOV         R2, A           ;; Put back into R2 till next time
        DJNZ        R1, Start_Comm  ;; stop  when 8 bits have been transfered
```

```
Wait_End_Comm:
;; Because of stop bit, it is necessary to
;; wait will Recv goes down

;;      XRL         P1, #00001000B  ;; D Set P1.3 Indicate end comm routine
;;      ACALL       TEMPO           ;; D Wait the visualisation
;;      XRL         P1, #00001000B  ;; D Reset P1.3
;;     AJMP        Wait_Zero       ;; wait till Recv is still low
                                                        ;; And return

;;_____________________________________________________________________
;;
;; WAIT_ZERO function wich wait data reception goes low
;;
;;
;;          This function wait reception data goes low and wait
;;     a time and test another time the reception data.
;;
;;
;;             Data in  parameters :
;;                                   none
;;
;;             Data out parameters :
;;                                   none
;;
;;      Registers used      :   A  :
;;                              R0 :
;;                              R1 :
;;                              R2 :
;;                              R3 :
;;                              R4 :
;;                              R5 :
;;                              R6 :
;;                              R7 :
;;
;;_____________________________________________________________________

Wait_Zero:
;; Wait Code PC goes LOW

      JB          RECV, Wait_Zero ;; --> Recv equals one, wait
      ACALL        Tempo           ;; Temporisation
      JB          RECV, Wait_Zero ;; --> Recv equals one, wait
      RET                         ;; Recv really at 0²
```