AFRL-IF-RS-TR-2002-254
Final Technical Report
September 2002

MODULAR MONOLITHIC MICROELECTROMECHANICAL (MEMS) SYSTEM TECHNOLOGY (M3S)

University of California at Berkeley

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AFRL-IF-RS-TR-2002-254 has been reviewed and is approved for publication.

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 074-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	SEPTEMBER 2002	Final May 97 – Apr 02

4. TITLE AND SUBTITLE
MODULAR MONOLITHIC MICROELECTROMECHANICAL (MEMS) SYSTEM TECHNOLOGY(M3S)

5. FUNDING NUMBERS
C - F30602-97-2-0266
PE - 63739E
PR - E117
TA - 00
WU - 22

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Sponsored Projects Office
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Berkeley California 94720

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Air Force Research Laboratory/IFTC
26 Electronic Parkway
Rome New York 13441-4514

10. SPONSORING / MONITORING AGENCY REPORT NUMBER
AFRL-IF-RS-TR-2002-254

11. SUPPLEMENTARY NOTES

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12a. DISTRIBUTION / AVAILABILITY STATEMENT
APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

12b. DISTRIBUTION CODE

13. ABSTRACT ***(Maximum 200 Words)***

Surface micromachining with monolithic integrated electronic evaluation circuits is an attractive technology for low-cost, highly compact sensors. Unfortunately, past monolithic sensor/circuits processes suffer from technology complexity resulting from the combination of two complex fabrication processes- The complex interactions slow down progress and preclude a straightforward upgrade path when a better circuit process becomes available.

The technology developed here overcomes the disadvantages. By fabricating the mechanical structures first and embedding them in a planarized wafer, it achieves a high degree of separation between the two processes. In fact, the mechanical structures are fabricated by Analog Devices, while a CMOS foundry adds electronic circuits. New circuit options are added by simply sending the wafers to a different foundry.

A full complement of gyroscopes and accelerometers fabricated in the modular process demonstrates the practicality Of the approach. Compared to conventional processes, the sensors benefit from unproved circuits performance and higher integration capability. A 5-V only gyroscope operating at ambient pressure underscores the flexibility of the approach to implement functions that normally require special technologies, such as high voltage transistors or vacuum packaging. 1-he simpler approach greatly reduces cost and should be of value particularly in cost-sensitive applications such as smart ammunition or micro-air-vehicles.

14. SUBJECT TERMS
Microelectromechanical, MEMS, Accelerometers, Gyroscopes, Inertial Navigation

15. NUMBER OF PAGES
29

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

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Summary

This project developed a new surface micromachining process combining an uncompromised polysilicon MEMS module with a standard IC process. The MEMS module features 6μm thick polysilicon, a figure that optimally balances the requirements of high performance sensors, such as gyroscopes, with fabrication complexity. A full complement of inertial sensors covering all six degrees of freedom has been demonstrated. All devices feature on-chip electronic circuits integrated monolithically with the mechanical structures. An in-house (ADI) 3μm BiMOS process as well as a more aggressive 0.8μm foundry CMOS technology are being used.

1. Introduction

We have developed a modular integrated MEMS/circuits technology, M^3S. The modular approach combines sophisticated MEMS processing with a standard, state-of-the-art sub-micron VLSI circuits process. The individual innovations the M3S technology is based on are described below.

Modular technology. The modular approach avoids the complexity of the combined mechanics/circuits technology from escalating and becoming unmanageable. It also allows for more natural evolution from one technology generation to the next. Mechanical devices are fabricated first since they normally require a larger thermal budget. Electronic circuits are added subsequently using a standard VLSI technology. A post-processing step addresses sensor-specific requirements such as structure release and vacuum encapsulation. Since interaction between modules is minimized, they can be developed in parallel and separately optimized.

MEMS-first technology. A state-of-the-art surface-micromachining module with low-stress polysilicon and two or more structural layers is a key feature of the M^3S technology. It is facilitated by fabricating the mechanical devices first and thus eliminating interaction with electronic device characteristics. Before circuit fabrication, the surface micromachined devices are embedded in oxide and the surface of the wafer planarized with chemical-mechanical polishing (CMP). A high temperature anneal significantly reduces the warping of mechanical structures and therefore increases the maximum size of mechanical devices from several hundred micron in BiMEMS to several millimeter in M^3S.

Standard CMOS processing. Electronic devices are added to the planarized wafer using standard VLSI technology. Since no modification of the standard process flow is required, this step can be performed at a foundry. System requirements are the primary consideration in the choice of an appropriate technology. A double poly double metal (DPDM) 0.8μm process fully exploits the aggressive features of the mechanical components. Compared to current 2μm or larger MEMS circuits technologies, the 0.8μm CMOS achieves more than an order-of-magnitude improvement in density, speed, and power dissipation.

MEMS device innovations. New devices exploiting the technology features and the high performance electronic circuits process of M^3S have been designed. A full complement of inertial sensors for monolithic 6-degrees-of-freedom sensing has been developed. Four of these sensors have been integrated on a single chip, demonstrating the high density of the process.

The M^3S (called ModMEMS by ADI) technology and devices fabricated are described in detail below.

2. M^{3}S (MOD MEMS) Process

2. 1 Summary of M3S Process Development:

The Mod MEMS process developed for M3S has been successfully demonstrated by a number of accelerometer and gyro fabrication runs using designs from both ADI and UC Berkeley. The process was initially developed and demonstrated using an ADI internal airbag accelerometer design. The production process used for ADI accelerometers utilizes a 2um poly MEMS layer. In order to expedite the development of Mod MEMS, a standard production accelerometer design was re-designed for the M3S 6um thick poly layer. This thickness was chosen as ADI had also determined it to be an optimum thickness for integrated gyro designs.

Initially two processes were considered for M3S: 1) an upgrade of the Sandia National Labs 2μm integrated MEMS process, and 2) a new epi planarized processed conceived at Analog Devices. Sandia did some initial work to demonstrate the potential to upgrade their process to 6um. However, in the mean time the ADI epi planarized process was adequately developed for prototyping, and was shown to have inherent advantages in planarization, and the ability to eventually implement more than 1 structural layer of poly. The decision was therefore made early in the program to switch all further process development to the Mod MEMS process at ADI.

An abbreviated, conceptual process flow for Mod MEMS is given in figure 1.

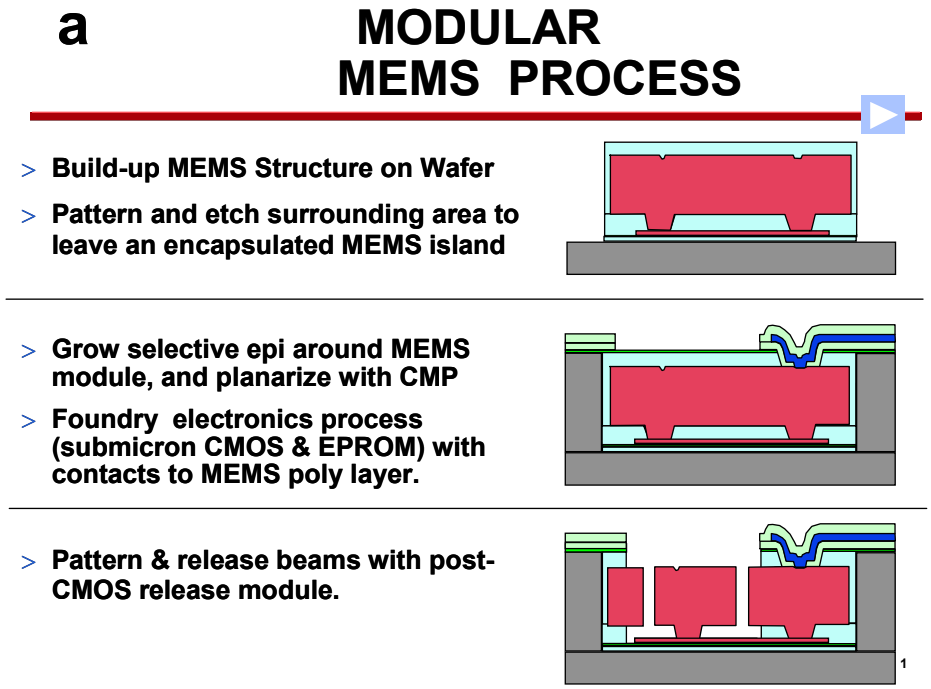


Fig. 1 Mod MEMS Process Flow

The critical unit processes developed for Mod MEMS were:

- Growth of low stress 6µm thick polysilicon
- Growth of an oxide sidewall spacer on the MEMS islands prior to the selective epi step,
- Selective epi which provided good planarization between the very thick MEMS regions and the surrounding Si used for submicron CMOS,
- CMP to both smooth the polysilicon prior to epi, and then complete the planarization of the MEMS area with the surrounding Si to facilitate the subsequent submicron CMOS processing,
- Bosch etching to define 6um poly MEMS structures with vertical sidewalls
- Modification of the ADI proprietary resist pedestal release process for final release of the MEMS structures.

Features of the Mod MEMS process were:

- 0.25µm ground poly with sheet resistance of 50 ohm/sq.
- Oxide isolated poly trench vias to allow contact to isolated ground poly lines
- 6um released structural poly layer with a sheet resistance of 15 ohm/sq, in-plane tensile stress of ~2E7 dyne/cm^2 and low vertical stress gradient with <0.1µm out of plane curvature in a 500um long released beam
- Use of CMP to smooth the 6um poly surface to <1nm RMS roughness.
- Contact process that allowed simple contact of the 6um poly with Al first level metal.

The first demonstration of the process using an ADI internal Bimos process and production 50g airbag accelerometer redesigned for 6um poly is shown in figure 2. The poly was not smoothed by CMP in this initial demonstration.

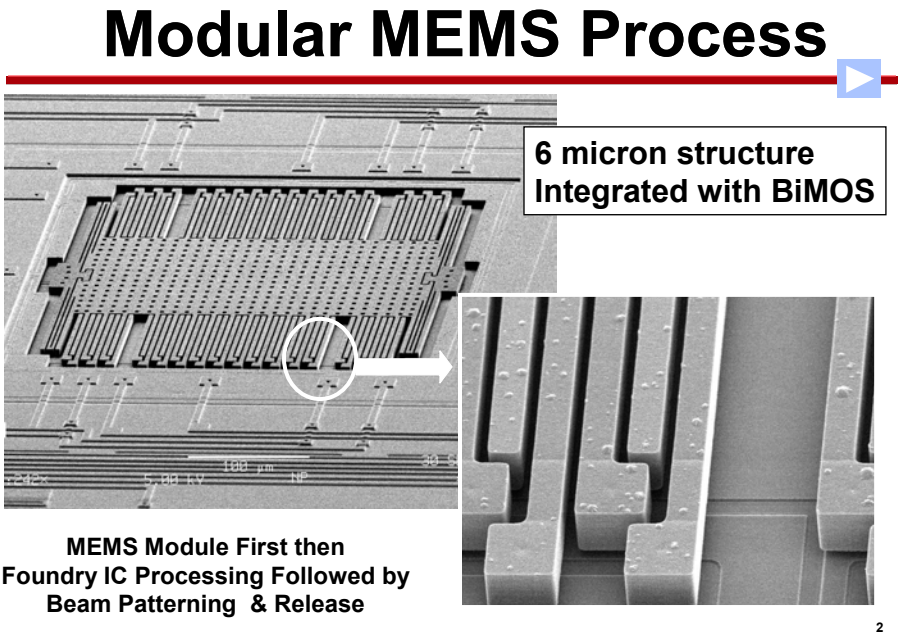


Fig. 2 Mod MEMS with ADI BiMOS

Once the Mod MEMS process module had been developed, the probe yields were quite encouraging on the initial development lots with functional accelerometer yields in excess of 70%. The process was then demonstrated with two UC Berkeley design runs. These designs were run using a 0.8μm CMOS foundry process running at Mitel in Bromont, Quebec in Canada. The CMOS process was not modified at Mitel to run the Mod MEMS wafers. The electrical parameters for the CMOS devices for each run were within normal ranges. For each design iteration a full set of working parts were obtained on the first wafer fabrication run such that additional wafer runs were not required. The electrical results of the M3S design runs are reported in (other sections) of this report.

A Gantt chart for the process development part of the M3S program is given in figure 3:

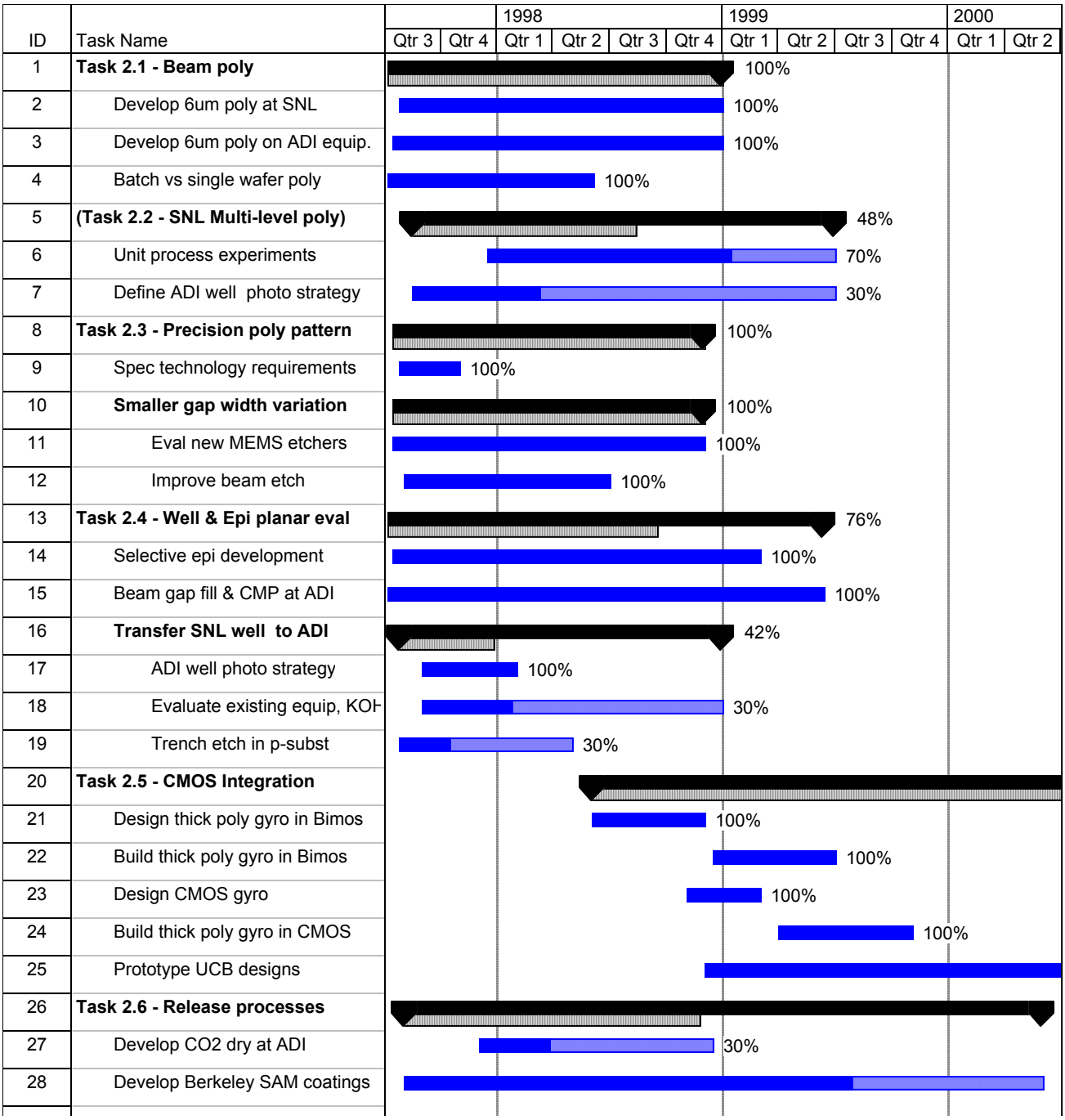


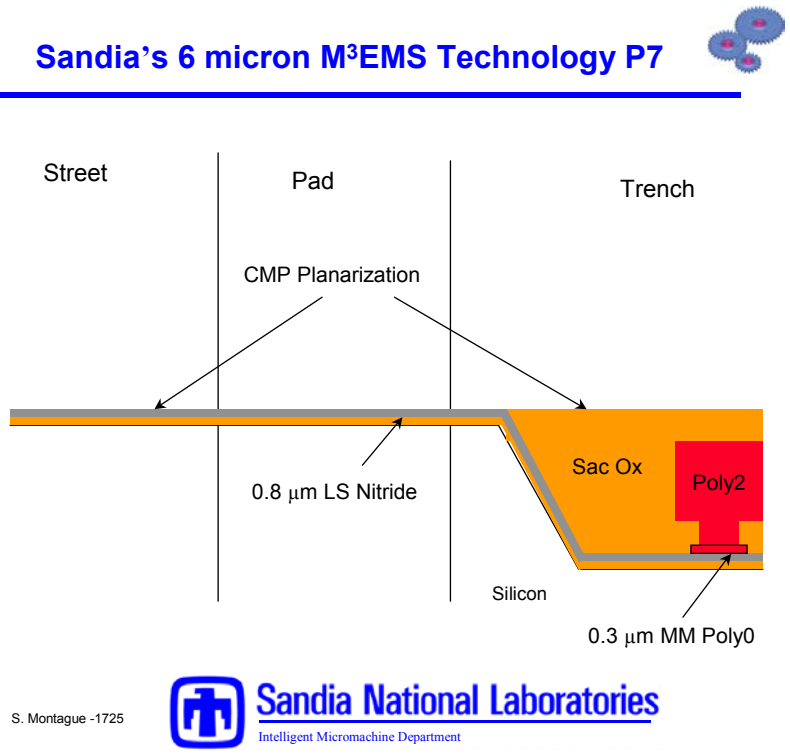
Fig. 3 M3S Process Development Schedule

2. 2 Sandia 6um poly process:

Sandia did demonstration work on their 2um poly integrated MEMS process to determine the feasibility of upgrading it to use a 6um structural MEMS poly layer. A summary of this work is reported in this section. The two main tasks were to: 1) increase the structural poly thickness to 6um with adequately low stress, and demonstrate the

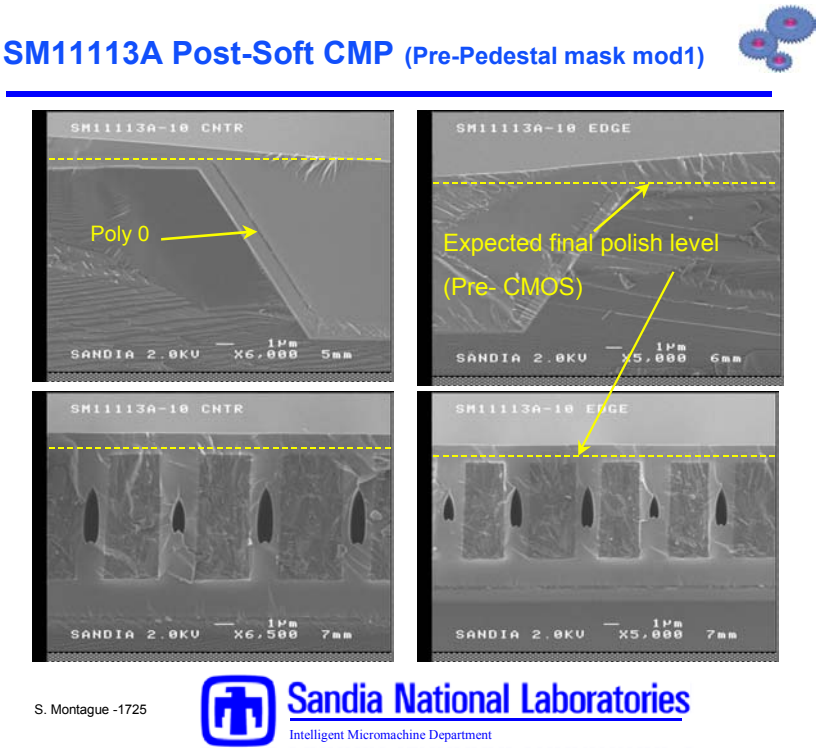
ability to etch it with good sidewall profiles, and 2) create an adequately deep KOH etched well into which a ground poly layer and 6um structural MEMS poly layer could be defined and then planarized with a gap filling oxide, prior to CMOS fabrication.

The Sandia M3EMS process consists of: 1) etching a well in the start Si wafer for the thick MEMS structures, 2) fabricating the MEMS ground and thick structural layer in the well, 3) filling the well and poly gaps with thick oxide, 4) using CMP to planarize the oxide in the well to be coplanar with the surrounding wafer and cap the well for subsequent CMOS processing, 5) CMOS fabrication, 6) open up the well and release the MEMS structures. Figures 4 and 5 depict the process after MEMS poly fabrication, oxide gap fill, and CMP oxide planarization.



Courtesy Sandia National Laboratories, SUMMiT(TM) Technology, www.mems.sandia.gov

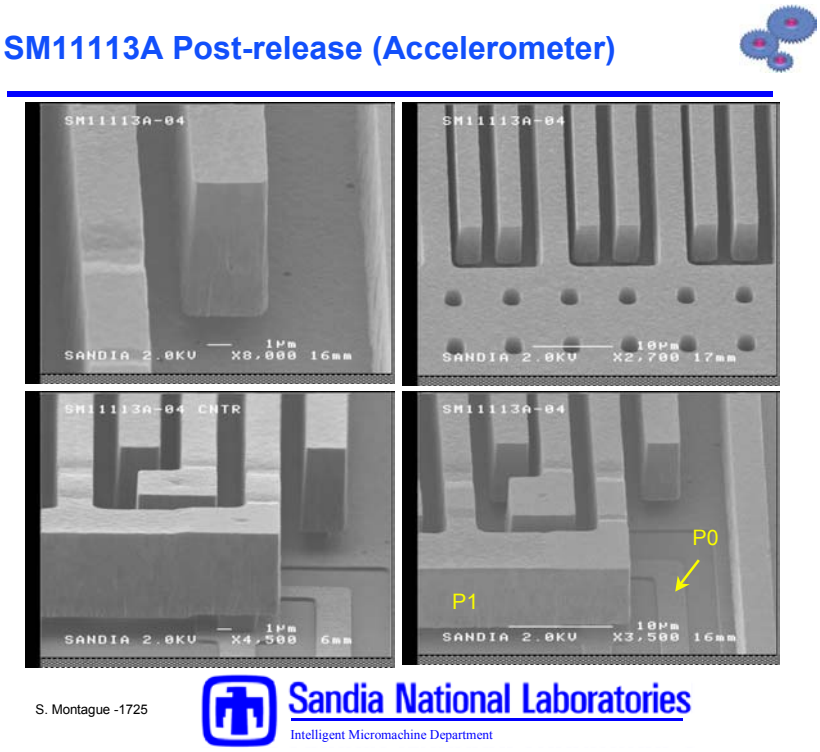
Fig. 4 Sandia Process After MEMS Fabrication, Oxide Fill and CMP



Courtesy Sandia National Laboratories, SUMMiT(TM) Technology, www.mems.sandia.gov

Fig. 5 SEM After MEMS Fabrication, Oxide Fill and CMP

Figure 6 below shows the Sandia process after release of the MEMS structures, which would be done after the CMOS processing is complete.



Courtesy Sandia National Laboratories, SUMMiT(TM) Technology, www.mems.sandia.gov

Fig. 6 SEM of Sandia Process After MEMS Release

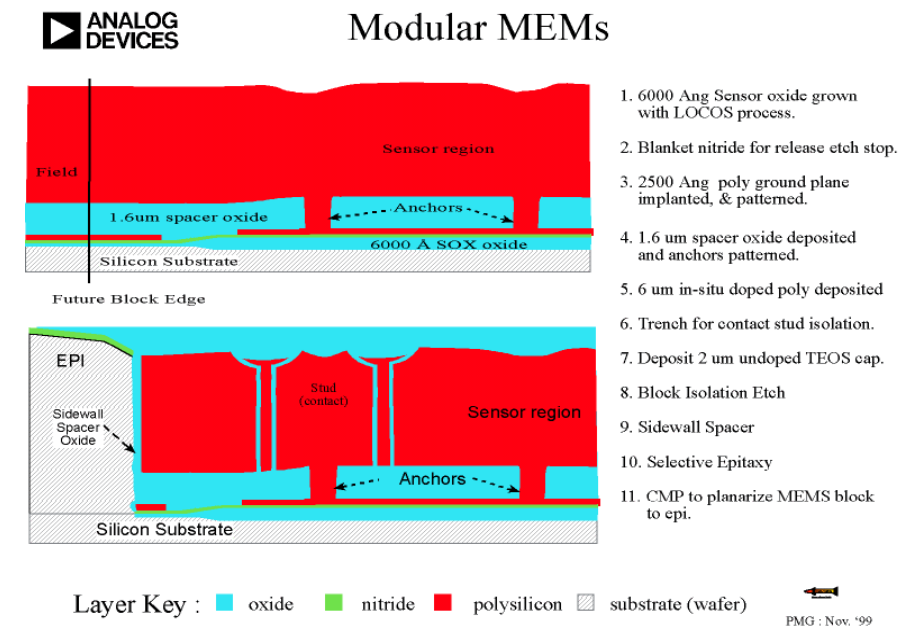
A basic capability was established to fabricate 6um thick MEMS poly structural layers in a planarized module which could be integrated with CMOS. However, several critical process issues were identified at this point which led to the adoption of the ADI epi planarized process:

- Well depth control and Si smoothness in the well after the KOH well etch
- Concern about the use of KOH etching in a CMOS fab.
- Difficulty in obtaining fine line width control of the 1st layer ground poly at the bottom of the well.
- Large spacings were required from the well edge to the MEMS poly in the well due to the variation in photoresist thickness near the well edge, which resulted in a large area penalty.
- There was no ability to CMP oxide over a second structural poly layer in the well, which would preclude the use of two thick structural poly layers which is needed for Z-axis sensing.
- The thick oxide fill and multi-step resist etchback and oxide CMP steps to planarize the well were felt to have serious process control issues. Also the thick oxide fill tool was not readily available at that point.

Based on these concerns, and the excellent progress made in the mean time on the ADI epi planarized MEMS process, it was decided by the second year of the program to focus exclusively on the ADI Mod MEMS process.

2. 3 ADI Mod MEMS process:

A more detailed version of the Mod MEMS process flow is given in figure 7 below.



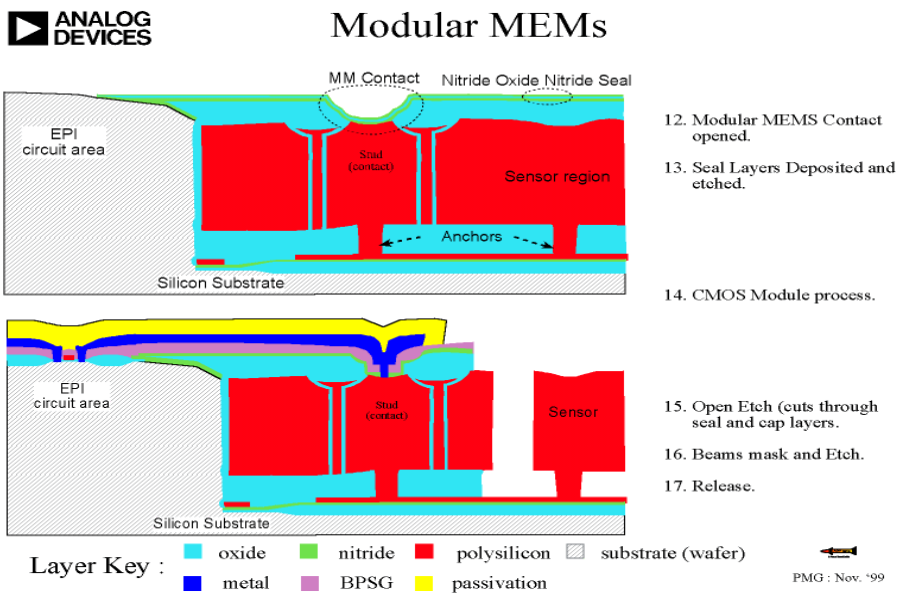


Fig. 7 Mod MEMS Process Flow

2. 4 6μm polysilicon growth, contact trenches, and block sidewall spacer:

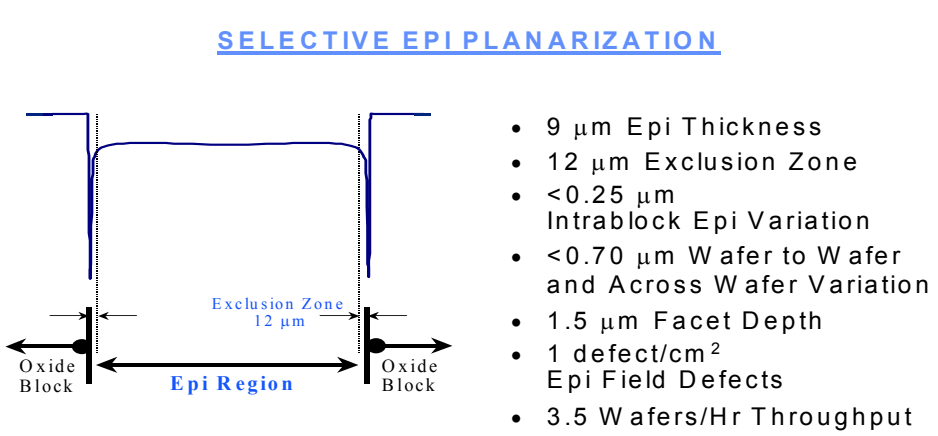
An ASM A400 vertical CVD furnace was used to deposit both the 0.25μm ground poly layer, and the 6μm structural poly layer. In-situ phosphorus doping was used during the 6μm poly growth layer in order to uniformly dope this very thick poly layer. The deposition temperature, gas flows and pressure were carefully balanced to obtain crack free as-deposited poly which was a critical control issue at poly layer thicknesses greater than 5μm. Once the poly was given a 900C anneal or higher the risk of cracking was eliminated. After annealing at 1100C or higher the films were nearly stress free with an in-plane tensile stress of ~2E7 dyne/cm^2, and very low vertical stress gradients as evidenced by out of plane curvature of released 500μm long cantilevered beams of 0.1μm or less. The 6μm poly sheet resistance was 15 ohm/square. The poly surface was quite rough after growth and it was found necessary to perform a brief CMP touch polish to remove this roughness prior to subsequent oxide CMP planarization after the selective epi planarization step. After the poly CMP step the poly surface roughness was reduced from a total range of 8,000A to less than 200A as measured by AFM.

After the 6μm structural poly growth and anneal the next most critical step was the formation of isolation trenches to provide electrical isolation between MEMS regions at different potentials. This involved a deep Si etch through the 6μm poly layer using an Alcatel deep Si Bosch etch tool. We then used a standard Novellus TEOS conformal oxide deposition and oxide etch back to form a trench sidewall spacer. Finally, a poly deposition was used to fill the isolation trench followed by a poly etch back to remove the trench fill poly from the surrounding field. The main process control issue in this isolation trench process was to insure that an adequate overetch margin was used to etch completely through the 6μm MEMS poly to the spacer oxide. Since the poly etch had good selectivity to oxide, and the spacer oxide was thick, this was relatively straightforward. However, in the early development phase special test structures were created to allow hand probing after poly trench fill and etchback to insure that good isolation had been achieved.

After the isolation trenches were completed a 2μm capping oxide and nitride (used as an oxidation barrier) was deposited, and the MEMS structural regions were then separated as isolated blocks by a photoresist mask and etch step. This etch was done to the ground poly which was unpatterned in the field. The field ground poly acted as an etch stop for this step. A thermal oxidation then formed a self-aligned oxide spacer on the block 6μm poly sidewall. Next the oxide formed on the field ground poly and the field ground poly itself were dry etched to the underlying field nitride layer. This nitride, and the block capping nitride were then removed in a hot phosphoric etch. Finally, the thin oxide under the field nitride was dipped off in a brief HF etch. At this point the MEMS poly was encapsulated in oxide and the devices were now ready for selective epi planarization. Several strategies were explored, requiring much time and effort, to provide this block sidewall oxide encapsulation, but this approach finally was chosen as the most robust process.

2. 5 Selective epi planarization:

The next step was the key to providing planarization around the very thick MEMS structures in order to allow integration with submicron CMOS. With the MEMS regions encapsulated in oxide a selective epi process was developed to grow epi around the MEMS block regions up to the top of the block. This epi process was developed in an ASM Epsilon One single wafer LPCVD epi tool. A substantial effort was undertaken to develop this process, but the final process was robust, and highly repeatable. Basically the Si source to Cl gas ratio was varied during growth to achieve good selective epi, and good epi uniformity across the wafer. The ground poly at the edge of the MEMS blocks was actually not covered with a sidewall oxide. However, it turned out that this poly was close enough to the Si substrate field that the substrate epi rapidly overgrew this region, and good epi was obtained all the way up the block sidewall. Due to slow crystal growth planes exposed at the edge of the block, a roughly 1.5μm facet was typically observed at the edge of the MEMS block region. A schematic description and crossection SEM of the epi growth process are shown in figure 8.



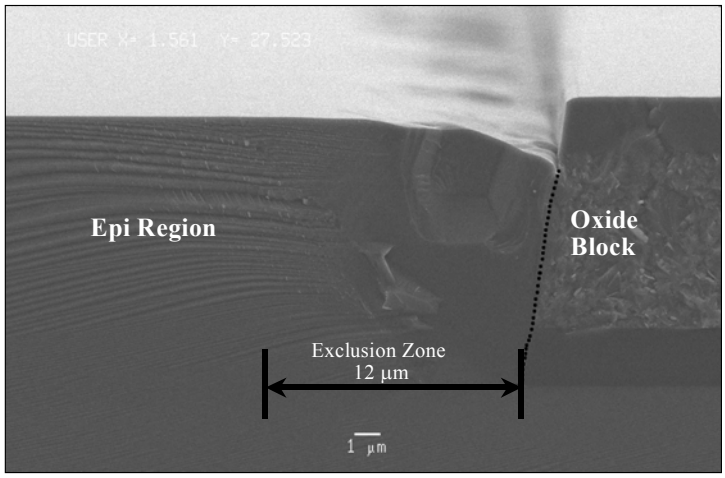


Fig. 8 Selective Epi Planarization Process

Typically 9µm epi was needed to bring the final silicon substrate surface for CMOS processing above the level of the ground poly, spacer oxide, 6µm structural poly, and capping oxide which permitted subsequent CMP planarization and accounted for cumulative variations in the MEMS module layer thicknesses. The 12 um exclusion region in the epi next to the MEMS block was the area where the epi growth rate was lower due to the presence of slow growth crystal planes in this area. The reduced growth rate resulted in an epi facet 1.5µm deep near the block edge. Outside this exclusion region the epi thickness varied by no more than 0.25µm which was considered more than adequate for CMOS stepper photolithography depth of field requirements. The use of selective epi, which requires a higher chlorine gas flow, and process tuning to get good across wafer epi growth uniformity resulted in

relatively slow epi growth rates. However the final wafer throughput of 3.5 wafers per hour was considered adequate for this critical step.

After selective epi, an oxide/nitride/oxide deposition followed by chemical mechanical polishing (CMP) filled the epi facet and finished the MEMS planarization process. The nitride provided a polish stop layer for the oxide CMP process. After CMP the nitride polish stop was removed from the epi field and a large sloped contact area etch was performed to the 6um MEMS poly to provide a contact region where the standard CMOS metal 1 contact process could be performed. Finally a seal nitride layer was deposited and patterned to provide protection to the MEMS region from the subsequent CMOS thick oxidation growth and oxide wet etch steps. A crossection SEM of a MEMS block edge at this step is given in figure 9. The striations in the epi seen next to the block are cleave artifacts. As can be seen here, the final MEMS to field epi transition is highly planarized.

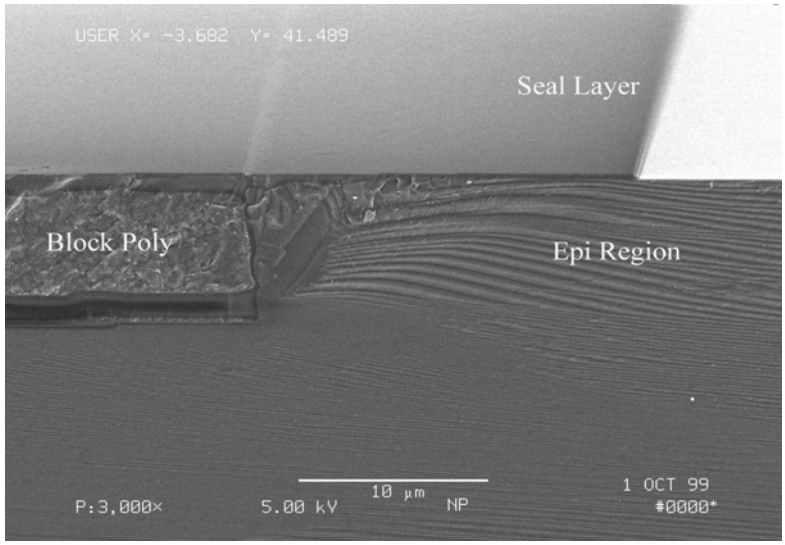


Fig. 9 Mod MEMS after Epi Planarization and Nitride Seal

At this point the wafers were ready for standard IC processing, initially an ADI BiCMOS process was used to demonstrate the process using an automotive accelerometer design (ADI XL76) modified to work with 6µm poly from the design for the standard 2µm poly production process. The first lots with the final Mod MEMS process worked well and soon provided both good wafer probe and final package yields (75% and 95% respectively). We then obtained designs from UC Berkeley designed to use Mod MEMS with 0.8µm CMOS which was obtained from Mitel in Bromont, Quebec in Canada using their standard 0.8µm double level metal CMOS foundry process. Two different design runs were eventually run from UC Berkeley and both resulted in good yields with all viable designs functional on the first pass of each design run.

The two major concerns for IC process integration with Mod MEMS were: 1) providing a MEMS seal layer that would withstand the standard oxidation and HF oxide etch steps, and the LOCOS field oxidation and nitride strip step, and 2) providing good contact between Metal 1 and the MEMS poly using some form of the standard IC contact and metal 1 process. As it turned out a simple multi-layer oxide plus nitride stack provided adequate protection of the beam module, and the large area sloped pre-IC contact area etch to the Mod MEMS contact regions

resulted in no changes to the contact or metal 1 processes for the two target IC processes described above. Furthermore it is believed that even with more advanced W plug contact processes that fairly simple modifications of the pre-IC MEMS contact area could be made which would minimize any required changes to the target CMOS contact process.

2. 6 MEMS beam etch and release

After completion of the foundry IC process through passivation, the MEMS area was opened up and the 6µm MEMS poly layer (beam) was etched and released. A photomask and dry/wet etch opened up the beams area. A resist photomask and Si Bosch etch (using a dep/etch process developed at Bosch for deep MEMS etching) on an Alcatel single wafer system was then used to pattern the 6µm MEMS poly layer. A cross section SEM after beam etch but before resist strip is shown in figure 10.

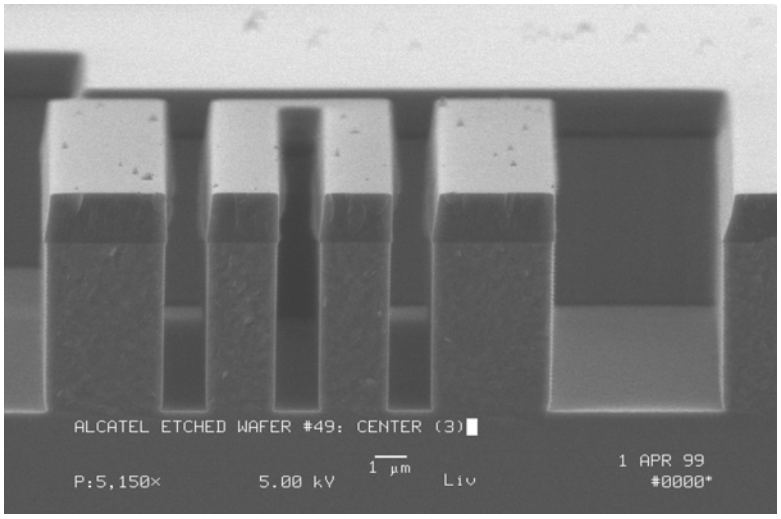


Fig. 10 6um Beam Poly Etch (before Resist Strip)

Finally the beam poly was released using a slight modification of ADI's proprietary photoresist pedestal release process. This process places resist blocks under and between the beam poly which hold the beams in place (i.e. prevent lateral and vertical stiction) during drying after the oxide HF release etch and final spin rinse dry. One additional development required in this process was to modify the beam poly surface condition under the photoresist protecting the field around the beam module during the HF release step. This was necessary to prevent lifting of the resist protecting the field and subsequent attack of the circuitry surrounding the beam module during the long HF release step. Once optimized no resist lifting (blowout) was seen and the surrounding circuit metal was protected. A SEM illustrating the pedestal release process is shown in figure 11, e.g. note the resist blocks in the inset perpendicular to the poly beams which hold the poly in place during drying after HF release.

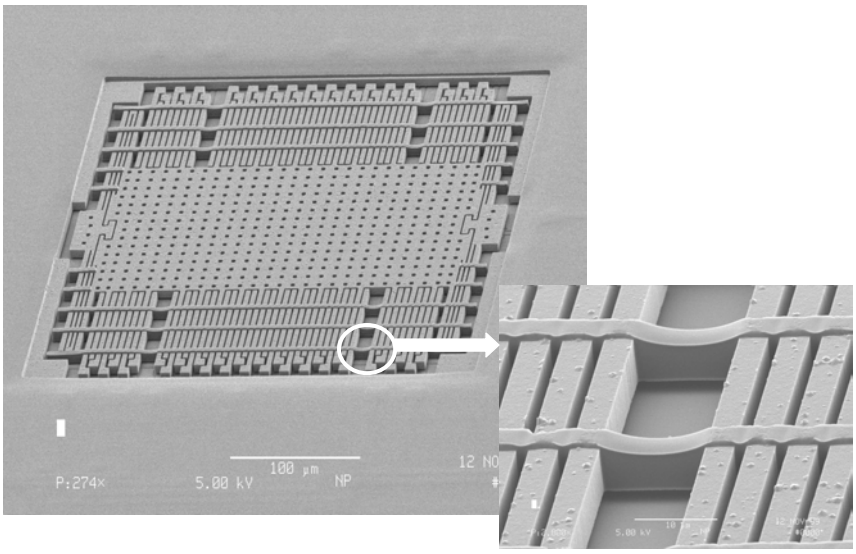


Fig. 11 Resist Pedestal Release Process

After the HF release and spin rinse dry, the wafers are put in a downstream oxygen plasma to remove the resist in order to fully release the beams without stiction. A fully released structure is shown in figure 2 in the summary at the beginning of this section.

This completes the processing of the Mod MEMS wafers. The Mod MEMS die were then diced and packaged using ADI's patented MEMS die soft cap protection and backside sawing process. The assembly yields for the Mod MEMS parts were quite high as described above (~95%) and essentially comparable to our standard production process.

3. M^{3}S Devices

3. 1 Overview:

A full set of inertial sensors has been developed for the M^{3}S process. The structures are described extensively in technical papers and include

- Three-axis accelerometer with on-chip converters [1]
- Z-axis gyroscope [4]
- Vertically driven X/Y gyroscopes [7]
- Resonant output gyroscope [8,9]

Figure 12 shows the layout and an SEM of a chip with two accelerometers and gyroscopes for four degrees-of-freedom (DOF) inertial sensing of linear in-plane acceleration and angular rate about the y- and z-axes. Sensors for the other axes have also been demonstrated in the M^{3}S process and when integrated with the devices shown in Figure 3 provide monolithic full 6 DOF inertial sensing. Such integration is entirely possible with M3S but has not been attempted because of limitations of the assembly tools. (The assembly process needs a tool that is size and pitch-matched to the sensor area of the chip. Only one such tool for a compromise of sensor area has been fabricated).

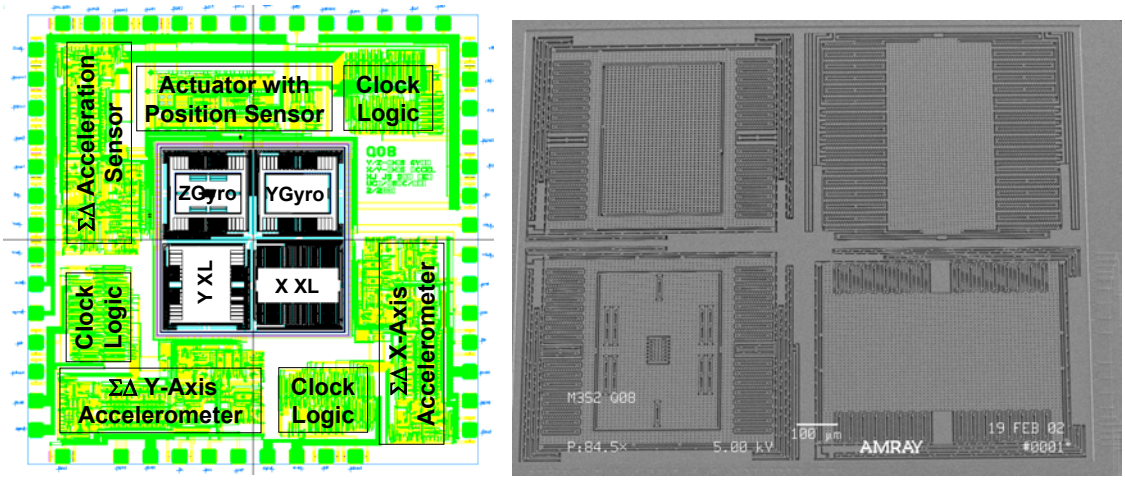


Fig. 12 Layout and SEM of a four degree-of-freedom inertial sensor

Other devices fabricated in M^{3}S include a high resolution electrometer [10] has been fabricated in the M3S process, underscoring the versatility of the technology to address a variety of sensing applications.

Significant effort has also been devoted to improving sense and electrostatic drive circuits for vibratory gyroscopes with new resonant displacement sensors [9], digital force-feedback loops [3], and electrostatic actuation circuits whose range is not limited by the so-called pull-in effect. This circuit and results are described in the section below, "Charge Control of Gap-Closing Actuators".

3. 2 Charge Control of Gap-Closing Actuators

3. 2. 1 Introduction

Gap closing actuators are used in a variety of MEMS applications, such as micromirrors, variable capacitors, accelerometers and gyroscopes. Typical gap-closing actuators are controlled by a constant voltage source. These designs are limited to motion less than 33% of the gap because of an instability known as *voltage-pull-in*. Charge control has been proposed as a technique to avoid *voltage-pull-in* and thus increase the range of motion. Theoretically, it should possible to move across the entire gap. Using the same supply voltage, a charge-controlled actuator can move three times farther than a voltage-controlled actuator.

In this work, we present a charge control circuit and experimental results showing travel greater than 80% of the gap. However, we also show that there is a *charge-pull-in* instability due to parasitic capacitance, and a *tip-in* instability due to torsional modes that can and do drastically reduce the performance of a charge controlled actuator.

Figure 13 shows an ideal gap closing actuator. It consists of one moving electrode and one fixed electrode. The moving electrode is supported by the mechanical suspension, modeled by spring constant k_x. Ideally, the moving electrode is constrained to move only in one direction.

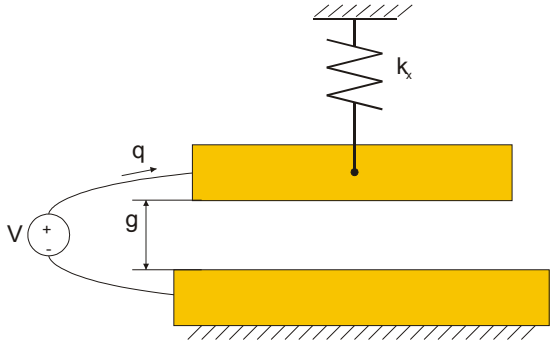


Fig. 13: Ideal gap closing actuator

The charge on the actuator, $q=CV$, where V is the voltage across the actuator, and C is the capacitance of the actuator. The actuator capacitance is modeled as a parallel-plate capacitance plus a parasitic capacitance:

$$C(x) = \frac{C_0}{(1 - x/d)} + C_p ,$$

where $C_0=\varepsilon A/d$ is the nominal parallel-plate capacitance, ε is the permittivity of air, A is the plate area, d is the nominal gap, and C_p is the parasitic capacitance due to fringing fields or wiring capacitance. The electrostatic force acting on the electrodes can be written in terms of either charge or voltage:

$$F_{el} = \frac{C_0 V^2}{2d(1 - x/d)^2} = \frac{C_0 q^2}{2d\left(C_0 + C_p(1 - x/d)\right)^2} .$$

Pull-In

If the voltage across the device is controlled independent of position, the electrostatic force can become much larger than the mechanical restoring force. This effect leads to the voltage-pull-in instability, which occurs at

$$x_{vpi} = \frac{d}{3} .$$

On the other hand, if the charge on the actuator is controlled, the actuator can move farther before becoming unstable.

$$x_{qpi} = \frac{d}{3}\left(1 + \frac{C_0}{C_p}\right)$$

If C_p is smaller than $C_0/2$, the force is relatively insensitive to position, and the actuator can be actuated across the entire gap without instability **[1]**.

3. 2. 2 Electrical Design

To demonstrate charge control, we designed and implemented the switched-capacitor circuit (figure 14) that was originally proposed in **[1]**. This circuit has the advantage over other charge control approaches because it insensitive to top and bottom plate parasitic capacitors, which otherwise would increase C_p and introduce an instability due to charge-pull-in.

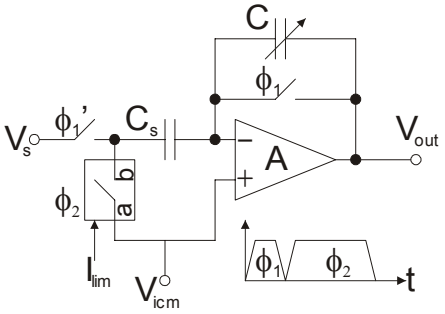


Fig. 14: Charge control circuit. ϕ_1' is a delayed version of ϕ_1.

The circuit has two phase of operation. In phase 1 (ϕ_1), the amplifier is put into unity gain feedback and the actuator, C, is completely discharged. The voltage V_s is sampled onto the input capacitor C_s. In phase 2 (ϕ_2), the charge that was stored on C_s is completely transferred to the actuator. In order to minimize the charge injection from the switches, the feedback switch is opened before the input switch, and the feedback switch is made as small as possible and includes a dummy switch to try to cancel the charge. The injected charge was measured on the order of 10fC or 1% of the full scale.

The charge-control circuit contains a current-limited switch whose schematic is shown in figure 15. In normal operation, V_{icm} is kept at 4.5V while V_{dd} is limited to 5V. When the clock switches from ϕ_1 to ϕ_2, the voltage at the negative terminal of the amplifier could momentarily exceed V_{dd}. This would cause the feedback switch to become forward biased, which would result in a large charge error on the actuator. By limiting the current in the switch, the voltage on capacitor C_s changes slow enough so the amplifier can keep the negative terminal close to V_{icm} and thus prevent forward biasing the feedback switch.

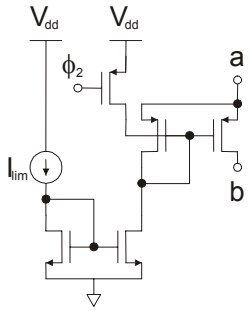


Fig. 15: **Current limited switch**

The amplifier is a two-stage, folded-cascode amplifier. According to reference **[1]** the open-loop gain must be greater than $2Cs/(C_0-2C_p)$. This constraint is easily met for all but the last design which is not charge stable for all deflections because $C_p>C_0/2$.

3. 2. 3 Mechanical Design

Ideally, the gap closing actuator is constrained to a translation mode. However, the mechanical suspension has finite stiffness against rotation, and so it is important to model the actuator as a two degree-of-freedom device (figure 16), which includes the translational mode and torsional mode.

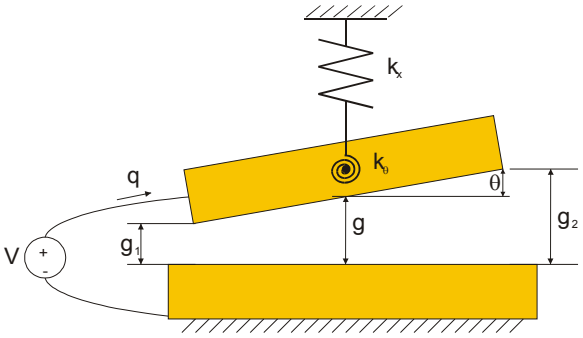


Fig. 16: Gap closing actuator with tipping mode

In this case, the capacitance can be approximated as

$$C(x_1, x_2) = \frac{C_0}{x_1/d - x_2/d} \ln \frac{d - x_2}{d - x_1}.$$

For small angles (i.e. $x_1 \approx x_2$) the capacitance is equal to the ideal model, however, $d^2C/d\theta^2$ is not zero, and it gives rise to a electrostatic, torsional-spring constant,

$$k_{\theta el} = -\frac{C_0 V^2 L_c^2}{12 d^2 (1 - x/d)^3},$$

in addition to the well-known electrostatic, translation-spring constant. The torsional-spring constant is the same regardless of whether the actuator is charge-controlled or voltage-controlled. Thus, if $k_\theta + k_{\theta el} < 0$, the torsional mode becomes unstable and the result is *tip-in*. It can be shown that tip-in will occur at

$$\frac{x_{ti}}{d} = \frac{1}{1 + \frac{k_x L_c^2}{6 k_\theta}}.$$

For a voltage-controlled actuator, the maximum deflection, x_{max}, will be the minimum of x_{ti} and 1/3 of the gap. For typical designs, the tip-in point is greater than 1/3 of the gap so the maximum deflection is 1/3 of the gap. However, it is possible to design an actuator with a low torsional stiffness, so that the actuator will pull-in before 1/3 of the gap. For a charge-controlled actuator, the maximum deflection, x_{max}, will be the minimum of x_{ti} and x_{qpi}.

3. 2. 4 Experiment

Four different parallel-plate actuators have been designed and tested to verify charge control as an effective actuation technique, as well as to verify the existence of the charge pull-in instability and the tip-in instability. A layout image of the chip is shown in figure 17. The chip was fabricated in the Analog Devices MODMEMS process, which includes a 6μm thick structural polysilicon layer along with 0.8μm CMOS electronics.

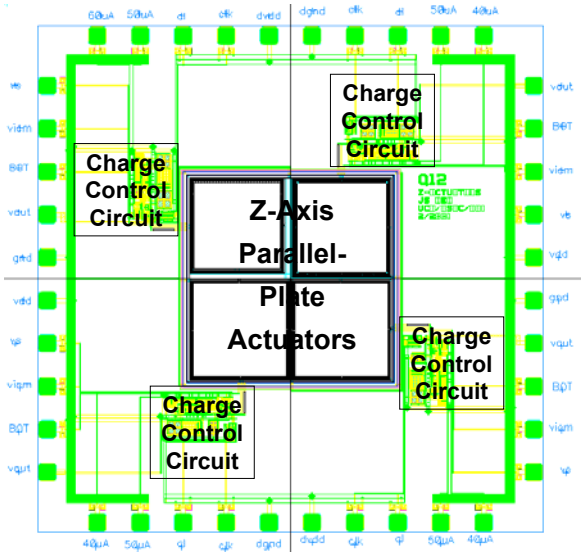


Fig. 17**: Layout image showing all four acuator structures and charge control circuits**

The first three designs have low parasitic capacitance, so that they are not limited by charge pull-in. Design #1, shown in figure 18, purposely has a low torsional stiffness and was designed to tip in at 20% of the gap, regardless of whether the actuator is controlled by voltage or charge. Design #2, shown in figure 19, has a higher torsional stiffness and smaller electrostatic actuator area, in order to reduce the negative torsional-spring constant. It was designed to tip-in at 60% of the gap. Design #3, shown in figure 20, has the smallest actuator area in order to further reduce the negative torsional-spring constant, and improve tip-in to 80% of the gap. The fourth design has the same mechanical design as design #3, and would be expected to tip-in at 80% of the gap. However, the electrical design is different because a parasitic capacitor was intentionally added to cause charge pull-in to occur at 60% of the gap. The design data is shown in Table 1.

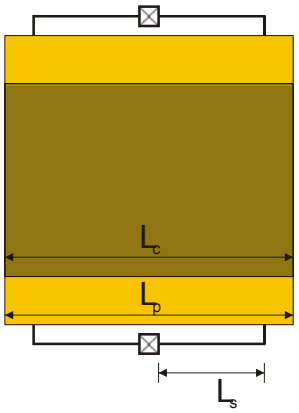


Fig. 18: Actuator design #1

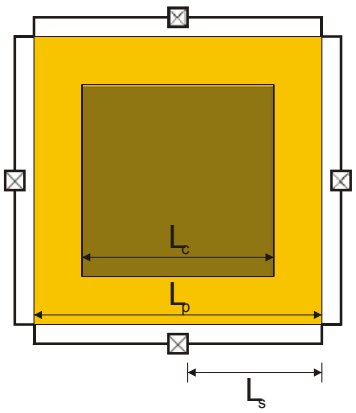


Fig. 19: Actuator design #2

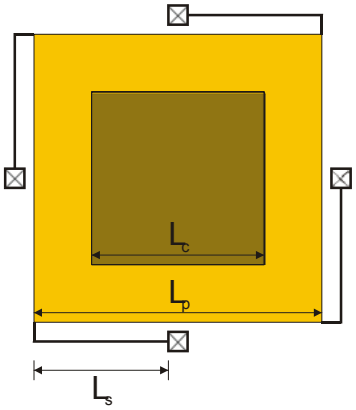


Fig. 20: **Actuator design #3. Actuator #4 has an identical structure but a larger C_p**

Table 1: Actuator Design Parameters

Parameter	Design #1	Design #2	Design #3	Design #3
d (μm)	1.6	1.6	1.6	1.6
k (N/m)	28.7	20.8	7.7	7.7
k_θ (μN m)	0.5	1.4	0.6	0.6
L_s (μm)	205	300	320	320
W_s (μm)	2	2.2	2	2
L_p (μm)	600	611	640	640
L_c (μm)	600	490	268.8	268.8
C_s (pF)	8.5	6	2	2
C_o (pF)	1.99	1.33	0.4	0.4
Cp (pF)	0	0	0	0.4

The amplifier and switches shown in figure 14 were operated on a 100kHz clock. The operation was tested with 60% duty cycle and with 80% duty cycle. Figures 21-24 show the responses of the four different designs to DC

charge control. These figures include 1) the measured root-mean-square values of input voltage V_s and output voltage V_{out}, 2) the extracted deflection versus charge, and 3) curves based on ideal theory that have been fit to the data. The measured and fit parameters are shown in Table 2. As predicted, the Design #1 tips in at 20% of the gap, Design #2 tips in at 60% of the gap, Design #3 tips in at 80% of the gap, and Design #4 pulls-in due to charge at 60% of the gap.

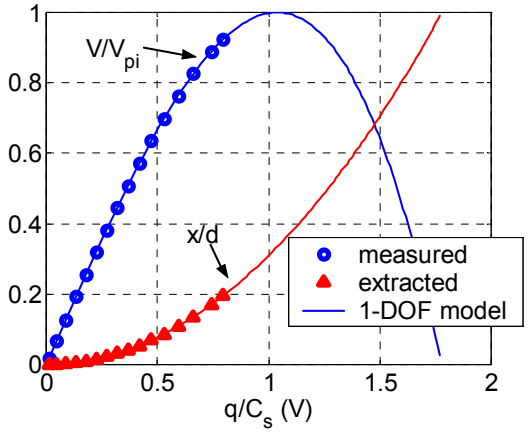


Fig. 21: Normalized position and rms-voltage versus rms-charge for actuator design #1

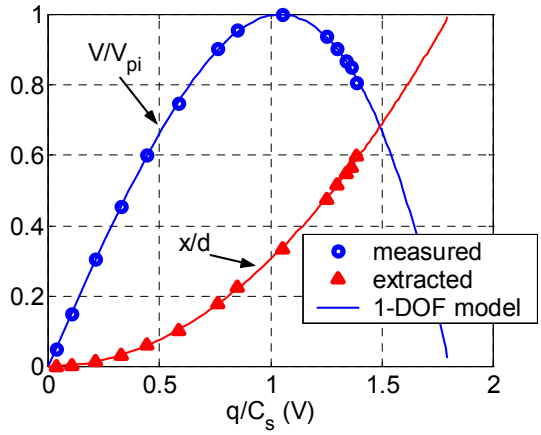


Fig. 22: Normalized position and rms-voltage versus rms-charge for actuator design #2

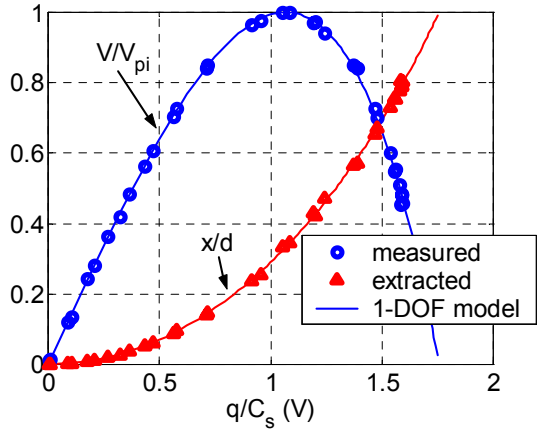


Fig. 23: Normalized position and rms-voltage versus rms-charge for actuator design #3

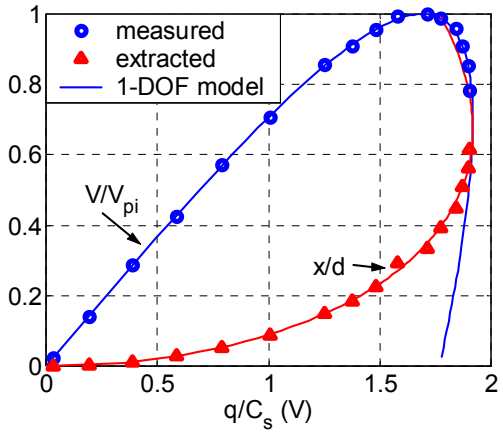


Fig. 24: Normalized position and rms-voltage versus rms-charge for actuator design #4

Table 2: Measured and Fit Actuator Parameters

Parameter	Design #1	Design #2	Design #3	Design #4
V_{pi} (rms)	2.82 (F)	2.97	3.19	3.15
C_s/C_o	4.12	4.28	4.72	4.62
C_p/C_o	0.014	0.004	0.081	0.981
x_{max}	0.196	0.6 (tip)	.805 (tip)	0.615 (q-pi)

3. 2. 5 Conclusion

This work has demonstrated a charge-controlled actuator that deflects up to 80% of the nominal gap. It becomes unstable due to tip-in in which the torsional stiffness is reduced to zero by the electrostatic, torsional-spring constant. We have also verified that parasitic capacitance causes a charge instability.

Future work will focus on new feedback circuit designs to stabilize against charge pull-in as well as tip-in.

4. Conclusions

A modular MEMS/electronics process has been demonstrated. The technology includes a MEMS-first polysilicon surface micromachining module and uses CMP and epitaxy to embed the sensor in the wafer for subsequent processing in a standard IC fab. The viability of this approach has been demonstrated with 0.8μm foundry CMOS and a 3μm BiCMOS technology. No modifications have been made to the MEMS module for these two technologies, underscoring the successful decoupling of the MEMS and circuits processes. Hence the development cycles of MEMS and electronic circuits need not be synchronized, ensuring access to the best process at all times.

The capability of the modular process has been demonstrated with a full complement of accelerometers and gyroscopes covering all 6 degrees of freedom. Up to four sensors have been fabricated on a single die, and more can be incorporated easily by increasing the sensor area. The circuits operate from a single 5-V supply to be compatible with common electronics processes and achieve a level of performance that is commensurate with other surface micromachined devices.

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