

## **I. PROJECT ACTIVITIES REPORT**

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13. ABSTRACT (Maximum 200 words) <p>This report results from a contract tasking Ioffe Institute as follows: The purpose of the proposed project is to develop, fabricate, test, and characterize silicon carbide power semiconductor opening switches operating in the picosecond range of switch time. Special SiC diode structures will be fabricated and investigated, including Junction Recovery Diodes (JRD). The operation of such diodes is founded on the superfast recovery of the junction's blocking ability after switching the device from forward to reverse bias conditions. Our estimations show that the parameters of JRD devices can be substantially improved in case of SiC devices, compared to both Si and GaAs capabilities. We expect i) to increase the speed of switch operation, the specific commutated power, and the operation frequency repetition; ii) to reduce the weight and size of pulse devices; and iii) to achieve better reliability of the devices due to the unique thermal conductivity and radiation hardness of SiC. It is proposed: 1) to carry out detailed theoretical estimations of possible electrical parameters of 4H-polytype SiC based JRDs; this will be based on our extensive past knowledge of and experience with Si based JRDs as well as recent 4H-SiC property data sets, 2) to fabricate appropriate diode structures using commercially available material, 3) to measure and study the diodes' actual switching recovery from the on-state to the off-state in conventional regimes, and to determine the lifetimes and diffusion lengths of minority injected carriers at different injection levels, 4) to study the diodes' operation in the JRD-mode, when the drift mechanism of recovery actually occurs, and to analyze: the kinetics of slow plasma enriched layer dissipation, the kinetics of abrupt current interruption, together with the time dependence of voltage during these processes, the influence of other factors on switching performance, such as the value of blocking voltage, the amplitude and duration of the forward pumping current, and the value of the reverse current, 5) to analyze the effects of the electrical parameters of SiC on JRD-mode switch operation and to consider and evaluate possible material improvements to enhance JRD performance, and 6) to recommend improvements to the material for development of SiC JRD.</p>				
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**Final  
Project Technical Report  
of ISTC 2049p**

**Research and Development  
of Silicon Carbide (SiC) Junction Recovery Diodes  
for Picosecond Range, High Power Opening Switches**  
(From 1 August 2001 to 31 July 2002 for 12 months)

**Igor Vsevolodovich Grekhov  
(Project Manager)  
Ioffe Physico-Technical Institute of Russian Academy of Sciences**

July 2002

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This work was supported financially by European Office of Aero-space Research and Development (EOARD), London as the Partner and performed under the contract to the International Science and Technology Center (ISTC), Moscow

Research and Development of Silicon Carbide (SiC) Junction Recovery Diodes  
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Grekhov Igor Vsevolodovich (Project Manager)  
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The objective of the project is to fabricate, test, and characterize 4H-SiC power semiconductor opening switches (OS) operating in the picosecond range of switch time. Preliminary estimations showed that due to unique properties of silicon carbide parameters of SiC-based pulse power opening switches can be substantially improved, compared to both Si and GaAs capabilities.

Special 4H-SiC diode structures were fabricated and investigated in regimes known for Si-based opening switches such as Inversion Recovery Diodes (IRD). The operation of such diodes is founded on the superfast breaking off the diode reverse current after switching the device from forward to reverse bias conditions.

The following work have been performed in course of the project:

1. calculations of possible parameters of 4H-SiC based OS,
2. fabrication of 4H-SiC diode structures,
3. measurements of static and transient characteristics of the devices,
4. analysis of junction recovery mode of operation.

Some conclusions regarding to possible ways of 4H-SiC material improvement in order to develop high voltage SiC-based OS-devices have been made.

Keywords: Semiconductor Opening switches, High power, Sub-nanosecond operation, Silicon carbide

**The work has been performed by  
the following institutes and partners**

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## 2. Objectives of the Project

The objective of the project is to fabricate, test, and characterize 4H-SiC power semiconductor opening switches (OS) operating in the sub-nanosecond range of switch time. Preliminary estimations showed that due to unique properties of silicon carbide parameters of SiC-based pulse power opening switches can be substantially improved compared to Si capabilities.

## 3. Scope of Work and Technical Approach

Special 4H-SiC diode structures were fabricated and investigated in regimes known for Si-based opening switches such as Inversion Recovery Diodes (IRD). The operation of such diodes is founded on the superfast breaking off the diode reverse current after switching the device from forward to reverse bias conditions.

The following work have been performed in course of the project:

1. calculations of possible parameters of 4H-SiC based OS-devices,
2. fabrication of 4H-SiC diode structures,
3. measurements of static and transient characteristics of the devices fabricated,
4. analysis of junction recovery mode of operation.
5. Some conclusions regarding to possible ways of 4H-SiC material improvement in order to develop high voltage SiC-based OS-devices have been made.

Theoretical estimates of the capabilities of OS-devices in 4H-polytype silicon carbide employ available models of silicon DSRDs and IRDs and the data relevant to the 4H-polytype of SiC. The 4H-modification of silicon carbide is chosen as the polytype with the highest carrier mobility, low dopant activation energies, a high breakdown field and a relatively developed process technology.

To investigate electro-physical properties of 4H-SiC films, appropriate characterization techniques were used such as C-V methods to measure doping profiles, comparative analysis of current-voltage and capacitance-voltage characteristics of junction diodes and Schottky diodes.

When fabricating diode structures, Al-based alloys were used as contact materials to p<sup>+</sup>-emitter layers and nickel metals as contacts to n-substrate regions. Micro profiling techniques to create device structures and patterns were used namely reactive ion-beam etching which allows to achieve a clean etched surface, rather high etch rate of about one micrometer per minute, high etch selectivity referred to the mask material.

Static and dynamics characteristics of the diodes were measured and analysed.

The diode operation in the IRD-mode, when drift mechanism of recovery actual occurs, was investigated by analysis of i) the kinetics of slow plasma enriched layer dissipation, ii) the kinetics of abrupt current interruption, together with the time dependence of voltage during these processes, iii) the influence of other factors on switching performance, such as the value of blocking voltage, the amplitude and duration of the forward pumping current, and the value of the reverse current.

## 4. Summary of Project Technical Report

During 1<sup>st</sup> Quarter the Tasks 1 and 2 have been solved: detailed theoretical estimations of possible electrical parameters of 4H-polytype SiC based OS-devices were carried out; appropriate epi-layered SiC structures have been ordered.

During the 2<sup>nd</sup> Quarter, the work routine has been directed on solving Tasks 2 - 4 of the Project. Mesa-isolated 4H-SiC p<sup>+</sup>n<sub>0</sub>n<sup>+</sup>- and p<sup>+</sup>p<sub>0</sub>n<sup>+</sup>-diode structures and Pd-n<sub>0</sub>n<sup>+</sup> Schottky-diode structures have been fabricated. The diode capacitance-voltage and forward current-voltage characteristics have been measured and analyzed. For p<sup>+</sup>n<sub>0</sub>n<sup>+</sup>-diodes, the transients to the steady-state condition have been studied when the diodes are stressed by a forward current pulse. For both p<sup>+</sup>n<sub>0</sub>n<sup>+</sup>- and p<sup>+</sup>n<sub>0</sub>n<sup>+</sup>-type diodes, comparative studies of the diode reverse current recovery have been made when the diodes are subjected to forward-to-reverse switch. The results obtained showed that the recovery properties of the p<sup>+</sup>n<sub>0</sub>n<sup>+</sup>-diodes drastically differ from those of p<sup>+</sup>p<sub>0</sub>n<sup>+</sup>-type ones. In p<sup>+</sup>n<sub>0</sub>n<sup>+</sup>-type diodes, the blocking ability recovery is governed by rather slow recombination and diffusion processes in the diode base. In contrast, purely drift mechanism of reverse current recovery was found to be responsible for the reverse current recovery in p<sup>+</sup>p<sub>0</sub>n<sup>+</sup>-type diodes. In particular, 4H-SiC p<sup>+</sup>p<sub>0</sub>n<sup>+</sup>-diodes demonstrate the drift recovery mechanism which is similar to that in silicon-based IRDs.

**The very sharp breaking off the reverse current of 1 Amp in a time less than 1 ns was achieved with p<sup>+</sup>p<sub>0</sub>n<sup>+</sup>-type diodes (Fig. 1).**

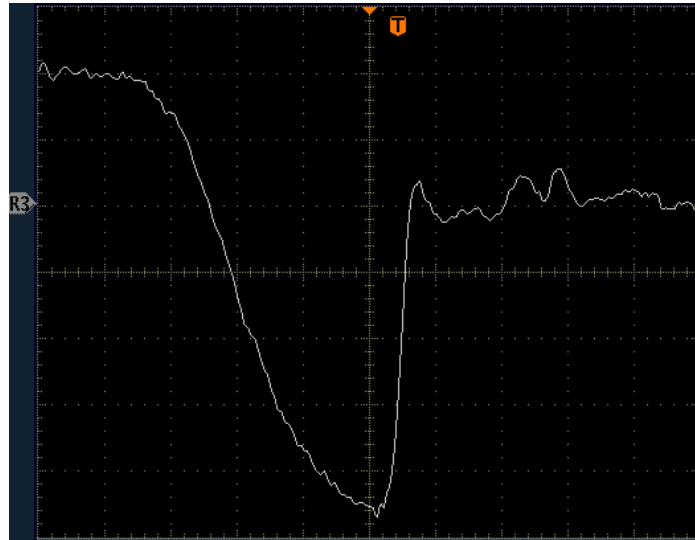


Fig. 1. Current tracing under forward-to-reverse bias switch for 4H-SiC  $p^+p_0n^+$ -diodes. Vertical scale is 0.2 A/div, horizontal scale is 4 ns/div. Forward current is 0.4 A. Zero current level is shown by the R3-marker.

During the 3<sup>rd</sup> Quarter, the work routine has been directed on solving Tasks 4 - 5 of the Project.

Platelets with 4H-SiC  $p^+p_0n^+$ -diode structures to be fabricated during the 2<sup>nd</sup> Quarter were cut into separate chips. Diode chips were placed into empty metal-glass IC packages.

Special electronic pulse generator with inductive energy storing unit was designed and built in which 4H-SiC diode is employed as a fast opening switch for breaking off the reverse current. Optimal regimes of operation of the 4H-SiC diode amounting to the generator were established. With this purpose the influence of the diode blocking voltage, the amplitude and duration of forward pumping pulse and the reverse current on output voltage pulse generation were investigated.

Voltage pulses of 400 V generated with 4H-SiC diode are shown in Fig. 2. As seen, the voltage rise time of about 4 ns. The effect of some reactances on voltage rise time is discussed.

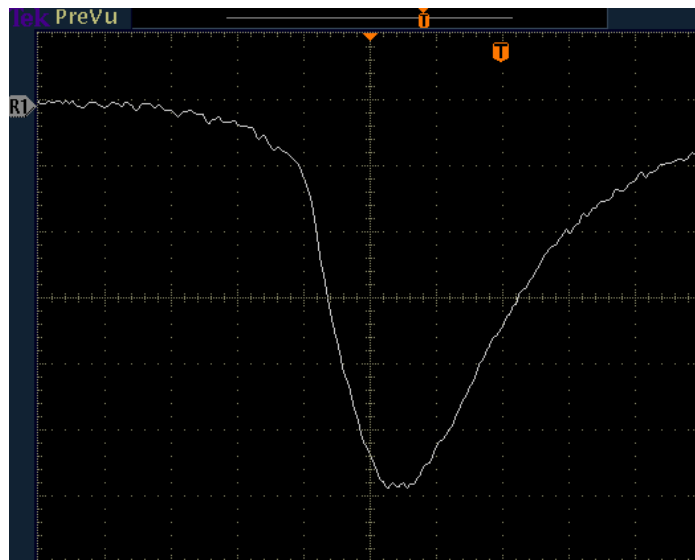


Fig. 2. 400-V voltage pulses generated by the pulse generator with 4H-SiC diode. Vertical scale is 70 V/div, horizontal scale is 4 ns/div. Zero current level is shown by the R1-marker.

During the 4<sup>th</sup> Quarter, real-time voltage pulse generation with our 4H-SiC diodes was shown, on the invitation of the Project Partner, at the International conference AMEREM'2002 (June 3 – 7, 2002, Annapolis, MD). In accordance with Project Work Plan, electronic generator and 10 capsulated 4H-SiC diodes were delivered to J. Gaudet as a contact person at AFL.

Some conclusions regarding to possible ways of 4H-SiC material improvement in order to develop high voltage SiC-based OS-devices have been made.

## 5. **Presentation of project results**

### List of published papers:

1. I. V. Grekhov, P. A. Ivanov, A. O. Konstantinov, and T. P. Samsonova. On the Possibility of Creating a Superfast-Recovery Silicon Carbide Diode. - Techn. Phys. Lett., Vol. 28, N7, pp. 544-546 (2002).

### List of presentations at conferences:

2. Grekhov I.V., Ivanov P.A., Konstantinov A.O. 4H-SiC inverse recovery diodes (IRD) for sub-nanosecond power opening switches. - Abstracts of the AMEREM'2002, June 02-07, 2002, Annapolis, MD, p. 59.
3. Ivanov P.A., Grekhov I.V., Konstantinov A.O., Samsonova T.P. Reverse Current Recovery in 4H-SiC Diodes with n- and p-Base. – To be published in Proc. of the 4rd European Conference on Silicon Carbide and Related Materials – 2002, Lincoping, Sweden, Sept. 2 - 5, 2002 (Trans. Tech. Publ., Switzerland).

## 6. **Cooperation with foreign collaborators (For each collaborator listed in the Work Plan)**

### Exchange of scientific material (information, computer codes and data, samples):

In accordance with Project Work Plan, interim technical reports, together with electronic generator and 10 capsulated 4H-SiC diodes were delivered to J. Gaudet as a contact Partner person at AFL.

### Trips to/from foreign Partner:

Real-time voltage pulse generation with our 4H-SiC diodes was shown, on the invitation of the Project Partner, at the International conference AMEREM'2002 (June 3 – 7, 2002, Annapolis, MD).

## 7. **Cooperation with CIS sub-contractors**

No sub-contractors were involved in the Project

## 8. **Technology Implementation Plan**

### How the project results will be implemented in the future work:

The Project results will be used for creation of the 20-kV pulse generator with voltage rise time ~ 1 ns.

### Perspectives of future developments of the research/technology developed:

Besides DSRD- and IRD-type devices, other types of SiC-based pulse power switches can be created such as avalanche sharpeners. With such devices, high-voltage pulses with several picosecond rise time can be formed.

### Potential commercial application of project results:

The results obtained can be used for manufacturing high-voltage pulse generators operating in sub-nanosecond time interval.

### Patents and copy rights:

At present study the Ioffe team retains know-how on the 4H-SiC pulse OS-devices.



## **II. PROJECT TECHNICAL REPORT**

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Special 4H-SiC diode structures were fabricated and investigated in regimes known for Si-based opening switches such as Inversion Recovery Diodes (IRD). The operation of such diodes is founded on the super-fast breaking off the diode reverse current after switching the device from forward to reverse bias conditions.

The following work have been performed in course of the project:

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## I. Introduction

At present, a task has to be solved in pulse power semiconductor electronics to develop new generation of high voltage switching devices which are able to form voltage pulses as high as 100 kV in a time less than 1 ns. Such super-fast electronic devices can find many applications namely for constructing (i) high effective and reliable pulse power supply for lasers and charged-particle accelerations, (ii) super-precise and ultra broad-band air and underground radar-location equipment, (iii) setups for gas cleaning by means of electrical discharge, (iv) control units for testing broad-band recording and metering circuits, etc.

The only material to be used now for fabrication of super-fast power semiconductor switches is silicon, where as the simplest device of this kind is Si-based Drift Step Recovery Diode (DSRD) [1,2]. The main feature of fast power switches utilizing DSRD-devices is that the high reverse current can be broken off very sharply if certain conditions are accomplished when turning the pn-junction from a forward current to reverse one.

The objective of the project is to fabricate, test, and characterize 4H-SiC power semiconductor opening switches (OS) operating in sub-nanosecond range of switch time. Preliminary estimations showed that due to unique properties of silicon carbide, the parameters of SiC-based pulse power OS can be substantially improved, compared to Si capabilities.

Special 4H-SiC diode structures were fabricated and investigated in regimes known for Si-based OS such as Inversion Recovery Diodes (IRD). The operation of such diodes is founded on the super-fast breaking off the diode reverse current after switching the device from quasi-dc forward bias to reverse bias.

The following work have been performed in course of the project:

1. calculations of possible parameters of 4H-SiC based OS-devices,
2. fabrication of 4H-SiC diode structures,
3. measurements of static and transient characteristics of the devices fabricated,
4. analysis of junction recovery mode of operation,
5. some conclusions regarding to possible ways of 4H-SiC material improvement in order to develop high voltage SiC-based OS-devices have also been made.

Theoretical estimates of the capabilities of OS-devices in 4H-polytype silicon carbide employed available models of silicon ones and the data relevant to the 4H-polytype of SiC. The 4H-modification of silicon carbide is chosen as the polytype with the highest carrier mobility, low dopant activation energies, a high breakdown field and a relatively developed process technology.

Mesa-isolated 4H-SiC  $p^+n_0n^+$ - and  $p^+p_0n^+$ -diode structures and Pd- $n_0n^+$  Schottky-diode structures have been fabricated. When fabricating diode structures, Al-based alloys were used as contact materials to  $p^+$ -emitter layers and nickel metals as contacts to n-substrate regions. Micro profiling techniques to create device structures and patterns were used namely reactive ion-beam etching which allows to achieve a clean etched surface, rather high etch rate of about one micrometer per minute, high etch selectivity referred to the mask material.

To investigate electro-physical properties of 4H-SiC films, appropriate characterization techniques were used such as C-V methods to measure doping profiles, comparative analysis of current-voltage and capacitance-voltage characteristics of junction diodes and Schottky diodes. In particular, the transients to the steady-state condition have been studied for  $p^+n_0n^+$ -diodes, when the diodes are stressed by a forward current pulse. For both  $p^+n_0n^+$ - and  $p^+p_0n^+$ -type diodes, comparative studies of the diode reverse current recovery have been made when the diodes are subjected to forward-to-reverse switch.

The diode operation in IRD-mode, when drift mechanism of recovery actual occurs, was investigated by analysis of i) the kinetics of plasma enriched layer dissipation, ii) the kinetics of abrupt current interruption, together with the time dependence of voltage during these processes, iii) the influence of other factors on switching performance, such as the value of blocking voltage, the amplitude and duration of the forward pumping current, and the value of the reverse current. The results obtained showed that the recovery properties of the  $p^+n_0n^+$ -diodes drastically differ from those of  $p^+p_0n^+$ -type ones. In  $p^+n_0n^+$ -type diodes, the blocking ability recovery is governed by rather slow recombination and diffusion processes in the diode base. In contrast, purely drift mechanism of reverse current recovery was found to be responsible for the reverse current recovery in  $p^+p_0n^+$ -type diodes. In particular, 4H-SiC  $p^+p_0n^+$ -diodes demonstrate the drift recovery mechanism which is similar to that in silicon-based IRD. In 4H-SiC  $p^+p_0n^+$ -diodes, 1-Amp reverse current was found to be broken off in a time less than 1 ns.

Platelets with 4H-SiC  $p^+p_0n^+$ -diode structures were cut into separate chips. Diode chips were placed into empty metal-glass IC packages.

Special electronic pulse generator was designed and built in which 4H-SiC diode is employed as a fast opening switch for breaking off the reverse current. Optimal regimes of operation of the 4H-SiC diode amounting to the generator were established. With this purpose the influence of the diode blocking voltage, the amplitude and duration of forward pumping pulse and the reverse current on output voltage pulse generation was investigated. As a result 400-V pulses with 4 ns rise time are obtained. The effect of some reactances on voltage rise time is discussed.

Real-time voltage pulse generation with our 4H-SiC diodes was shown, on the invitation of the Project Partner, at the International conference AMEREM'2002 (June 3 – 7, 2002, Annapolis, MD). In accordance with Project Work Plan, electronic generator and 10 capsulated 4H-SiC diodes will be delivered to J. Gaudet as a contact person at AFL.

Some conclusions regarding to possible ways of 4H-SiC material improvement in order to develop high voltage SiC-based OS-devices have been made.

## II. Si-based opening switch

Si-based DSRDs are usually made from a gradual  $p^+pnn^+$ -structure (Fig. 1). The forward current is firstly applied to fill the base p- and n-layers by electron-hole plasma (EHP).

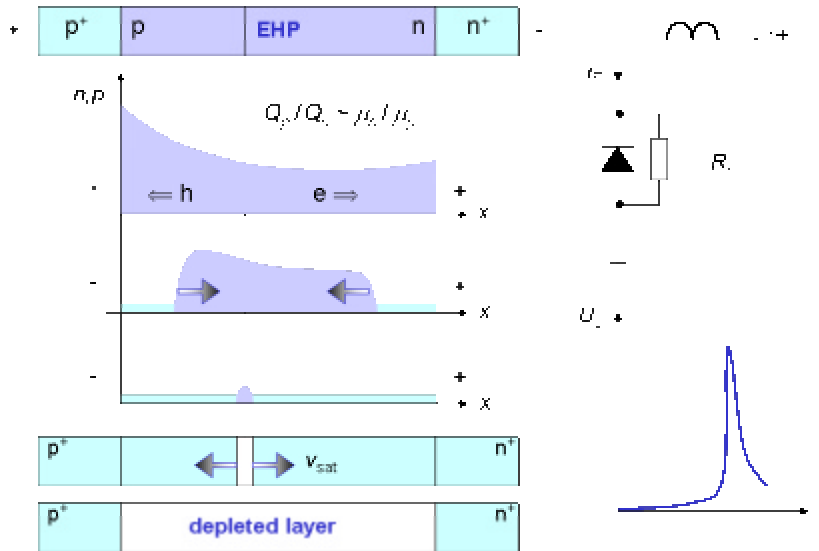


Fig. 1. Si-based gradual DSRD  $p^+pnn^+$ -structure. The distribution of EHP at the end of forward pumping pulse, the motion of EHP wave fronts during sweeping out the excess carriers and the development of DL after collision of EHP wave fronts at the pn-boundary are shown.

Then a reverse current pulse with fast rise time is applied that allows sweeping out the excess electrons and holes away from the base p- and n-layers. During the sweeping-out steep EHP wave fronts are formed which move towards to each other, with the pn-boundary being between the EHP wave fronts. If the wave fronts collide exactly at the pn-boundary then there will be no EHP in the diode after this instant. At a later time, the reverse current can be maintained by majority carriers only: majority electrons and holes move away from the pn-junction in opposite directions, the carrier velocity being equal to saturated velocity  $v_s$ . At this stage the depletion layer (DL) starts to restore and the reverse blocking voltage develops resulting in abrupt breaking off the reverse current (the current falls in a time of several nanoseconds). As a result of this process, the current is passed to a load resistor connected in diode parallel and a fast rising voltage pulse is formed in the load (at a given amplitude of the voltage pulse to be governed by working diode voltage the optimum reverse current may be chosen by adjustment the diode area, background base doping level, and load resistance). If, by contrast, the EHP wave fronts meet each other in a plane that is not coincide with the pn-boundary, the DL is to be restored in presence of some amount of EHP at one of DL's boundary that slows down the current break. To provide for EHP wave fronts to collide exactly at the pn-plane it is necessary that the total amount of EHP in the p-layer is approximately three times higher than that in the n-layer because of corresponding inequality of carrier mobilities (in silicon,  $\mu_n/\mu_p \approx 3$ ). Such a strong non-uniformity in minority carrier distribution is usually provided by applying 0.1 - 0.3  $\mu s$  short pumping forward current pulse.<sup>1</sup>

## III. Potential advances of SiC

<sup>1</sup> If the injection coefficients of both  $p^+p$ - and  $nn^+$ -junctions are unity and the duration of pumping pulse is longer than minority carrier lifetime then the carrier distribution will be asymmetrical because that the ratio of EHP densities at the  $p^+p$ - and  $nn^+$ -boundaries is equal to the ratio of mobilities of carriers which are injected by appropriate junctions [3]. However, owing to decrease in the injection efficiencies with increasing current density  $j_F$  the EHP densities are balanced at  $j_F \sim 100$  A/cm<sup>2</sup>. In this case the required asymmetrical carrier distribution can be created by shortening the forward pumping pulse down to a value that is substantially less than the carrier lifetime.

Wide bandgap semiconductor SiC is promising material for electronic devices owing to its unique electronic properties. The physical and electronic properties of silicon carbide make it the foremost semiconductor material for short wavelength optoelectronic, high temperature, radiation resistant, and high power/high frequency electronic devices. Electronic devices formed in SiC can operate at extremely high temperatures without suffering from intrinsic conduction effects because of the wide energy bandgap. SiC can withstand a voltage gradient over ten times greater than Si or GaAs without undergoing avalanche breakdown. This high breakdown electric field enables the fabrication of very high-voltage, high-power devices such as diodes, power transistors, power thyristors, as well as high power microwave devices. Additionally, it allows the devices to be placed very close together, providing high device packing density for integrated circuits. SiC is an excellent thermal conductor. Heat will flow more readily through SiC than other semiconductor materials. In fact, at room temperature, SiC has a higher thermal conductivity than any metal. This property enables SiC devices to operate at extremely high power levels and still dissipate the large amounts of excess heat generated. SiC devices can operate at high frequencies (RF and microwave) because of the high saturated electron drift velocity of SiC. Collectively, the properties of SiC allow SiC devices to offer tremendous benefits over other available semiconductor devices in a large number of industrial applications.

Potential advantages of SiC-based OS-devices are as follows. Of particular importance are SiC's high electric field strength and high saturation drift velocity, thus allowing smaller and faster devices. It is clear that the time duration of OS-devices recovery is directly proportional to the thickness of DL that corresponds to the static blocking condition and reverse proportional to the DL's expansion velocity:

$$\Delta t_r = \frac{W}{v_s}. \quad (1)$$

At a given diode working voltage, the higher is the critical electrical breakdown field  $E_b$  the lower is the  $W$  value. In silicon carbide the  $E_b$  is about 2 MV/cm [4], i.e. one order of magnitude higher as compared to silicon. In addition, carrier saturated velocity  $v_s$  is  $2 \times 10^7$  cm/s [4], i.e. twice higher as compared to silicon. So, one can expect that the recovery time of SiC-based OS-devices could be at least one order of magnitude shorter as compared to identically rated silicon devices. Besides, higher background doping in the base, higher working temperature, and higher thermal conductivity of SiC allows for SiC-based OS-devices to have much higher working current density at the same diode working voltage.

The main project task is to demonstrate 4H-SiC-based opening switches that can form voltage pulses of approximately 500 V in amplitude, with rise time in the order of 1 ns. Unfortunately, gradual diffusion pn-junctions are hard to be produced in SiC. The reason is that the thermal diffusion coefficients in SiC are very low at temperatures below 2000°C. High quality abrupt pn-junctions in SiC are usually made by epitaxial growth. In course of the task, we fabricated and tested epitaxial 4H-SiC  $p^+n_0n^+$ - and  $p^+p_0n^+$ - diodes. The 4H-polytype is chosen owing its better electronic properties as compared to other SiC polytypes. In particular 4H-SiC has the highest and anisotropic electron mobility and lowest dopant activation energies. It is worth to note that namely 4H-SiC is usually used around the world to produce high voltage bipolar SiC devices - rectifier diodes, thyristors and BJTs [5 - 8].

#### IV. 4H-SiC $p^+n_0n^+$ -diodes

##### 1. Experimental details

Mesa-isolated 4H-SiC epitaxial diodes (Fig. 2a) were fabricated on  $p^+/n_0/n^+$  homoepitaxial layers purchased from IMC (Stockholm, Sweden). Epitaxial growth at IMC was performed by atmospheric-pressure chemical vapor deposition (CVD) in a  $\text{SiH}_4\text{-C}_3\text{H}_8\text{-H}_2$  system. Substrates with 8° off-angles were used to realize homoepitaxy through step-flow growth. The growth temperature was 1500°C, at which a growth rate of about 4  $\mu\text{m/h}$  was obtained. The net donor concentration of 40- $\mu\text{m}$  thick nitrogen (N)-doped  $n_0$ -epilayer was  $(3 - 5) \times 10^{14}$   $\text{cm}^{-3}$ . The Al-acceptor concentration of  $p^+$ -layers and the N-donor concentration of  $n^+$ -layers were designed to be  $10^{19}$  -  $10^{20}$   $\text{cm}^{-3}$ . In order to confine the blocking  $p^+n_0(\text{top})$ -junction, diodes were processed into a mesa structure by reactive ion etching using pure  $\text{SF}_6$  gas with an nickel (Ni) mask. In addition, Pd- $n_0n^+$ -type Schottky diodes were fabricated (Fig. 2b), the top  $p^+$ -layer being preliminary removed from a part of the  $p^+/n_0/n^+$ -type platelet by reactive ion etching in  $\text{SF}_6$ .

Capacitance-voltage (C-V) characteristics of the diodes were measured at a frequency 1 kHz using a capacitance bridge unit E8-2. Forward current-voltage (I-V) characteristics were measured with an I-V tracer unit L2-56.



Recovery processes were studied using an electrical circuit schematically shown in Fig. 3. Forward current pulse was formed by discharge of capacitor  $C_1$  through the loaded diode ( $R_L$  load) when the switch  $S_1$  (Si thyristor) is short-circuited. Then the diode was rapidly switched (using the discharge of capacitor  $C_2$  when the switch  $S_2$  (Si IGBT) was short-circuited after appropriate delay) from the initial forward bias to reverse bias. The reverse current rise time was about 10 ns.

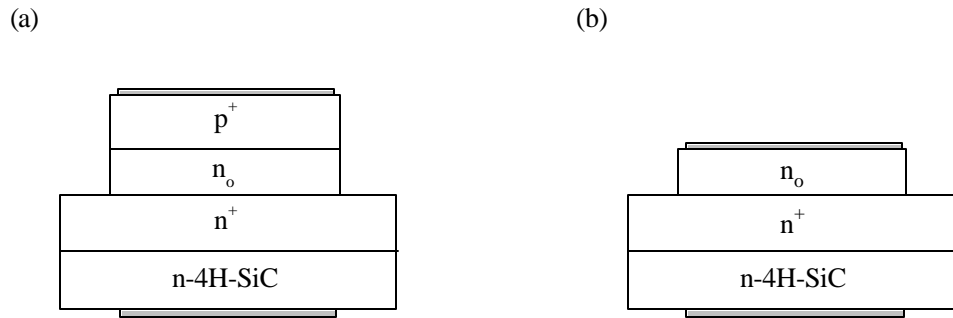


Fig. 2. Mesa-isolated 4H-SiC  $p^+n_0n^+$ -diodes (a) and Pd- $n_0n^+$ -Schottky diodes (b).

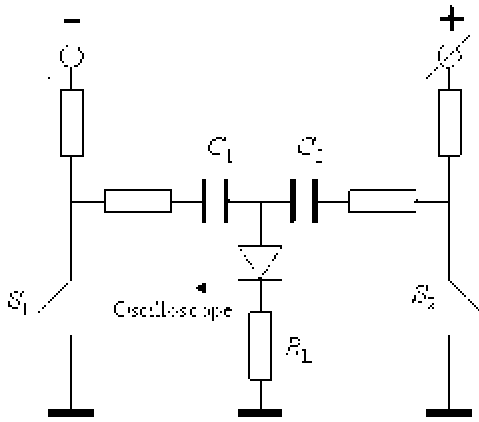


Fig. 3. Electrical circuit to be used for the measurements of transient characteristics of the diodes.

## 2. Results and discussion

Typical C-V characteristic of a  $p^+n_0n^+$ -diode is shown in Fig. 4a, while Fig. 4b depicts calculated doping profile of the  $n_0$ -base.

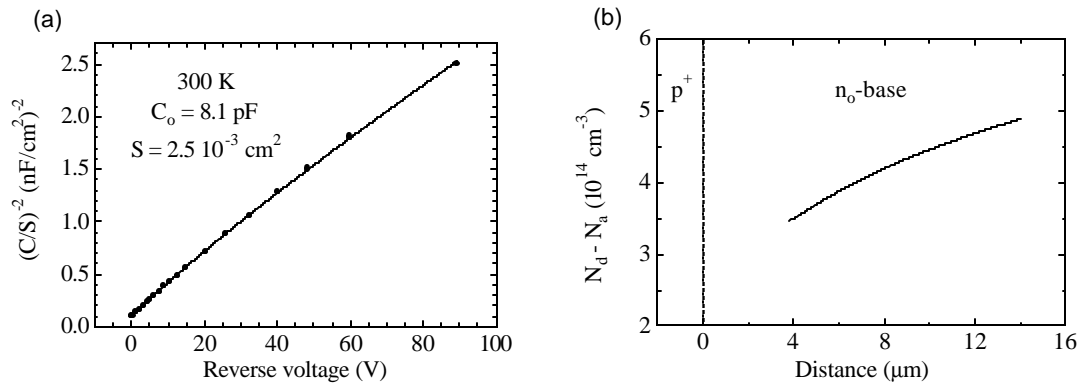


Fig. 4. Capacitance-voltage characteristics of a  $p^+n_0n^+$ -diode (a), doping profile of the  $n_0$ -base.

In the  $p^+n_0n^+$ -diodes, the electron density in the  $n_0$ -base is  $3 \times 10^{14} \text{ cm}^{-3}$  at the metallurgical  $p^+n_0$ -boundary and increases to  $5 \times 10^{14} \text{ cm}^{-3}$  over  $15 \text{ }\mu\text{m}$  away from it toward the base bulk (the total thickness of the  $n_0$ -base is about  $40 \text{ }\mu\text{m}$ ).

Typical I-V characteristics of  $p^+n_0n^+$ -diodes and Schottky-diodes are shown in Fig. 5a and 5b, respectively.

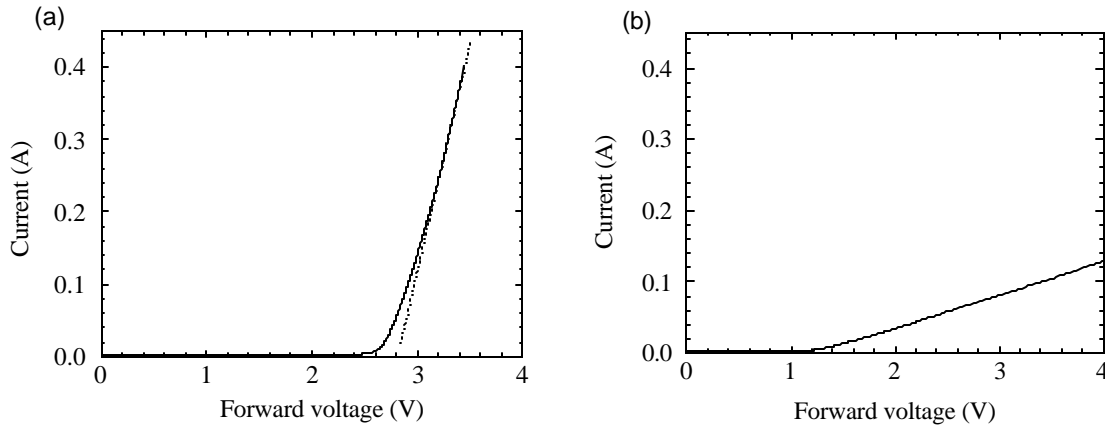


Fig. 5. Current-voltage characteristics of a  $p^+n_0n^+$ -diode (a) and Pd- $n_0n^+$ -type Schottky diode (b).

It can be concluded from Fig. 5a that in  $p^+n_0n^+$ -diodes, rather effective modulation of the  $n_0$ -base by minority carriers is achieved. In fact, the differential resistance of these diodes measured in on-state ( $r_d = 1.7 \text{ }\Omega$ ) is turned out to be approximately 15 times lower than the value to be expected in case of zero modulation. Assuming electron mobility  $\mu_n = 800 \text{ cm}^2/\text{Vs}$  one can calculate the ohmic resistance of the base of  $r_b = W(qn\mu_n)^{-1} = 24 \text{ }\Omega$ . Note that the differential resistance of Schottky diodes (in which no minority carriers arise at any bias conditions) is about  $22 \text{ }\Omega$  in on-state (Fig. 5b) that is very close to the above calculated value.

Figure 6 depicts transient characteristics of  $p^+n_0n^+$ -diodes under stressing the diodes by a pulse forward current. The time dependencies of the voltage drop across the  $p^+n_0n^+$ -diodes during pumping the minority carriers into the base clearly demonstrate the process of accumulation of excess carriers. After applying the forward current pulse, a voltage peak is observed, the maximum value being sufficiently higher than the steady-state one. Such "overshoot" effect is explained as follows. At the instant just after applying the current, the voltage drop is determined by the resistance of non-modulated base. So, the initial voltage drop across the diode is high. As the injected carriers are accumulated in the  $n_0$ -base, the voltage drop falls down to the steady-state value that is determined by the resistance of modulated base. It is worth nothing the following features of the process discussed. First, the time interval of establishing the steady-state grows with rising temperature. This means that the minority carrier lifetime  $\tau$  to be equal approximately to the time interval of establishing the steady-state, grows with increasing temperature. Second, the voltage "overshoot" amplitude also increases with increasing temperature. This very understandable effect results from the decrease of majority carrier (electron) mobility and, subsequently, the increase of resistance of non-modulated base. So, the transient behavior of the  $p^+n_0n^+$ -diodes under stressing by forward current evidences about rather high minority carrier lifetimes (in the average, of several hundreds nanoseconds).

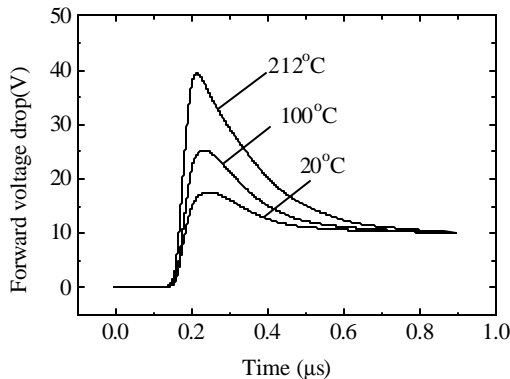


Fig. 6. Time dependencies of voltage drop across a  $p^+n_0n^+$ -diode after applying the forward current pulse of 5.5 A.

Figure 7 presents typical reverse current recovery in  $p^+n_0n^+$ -diodes under a forward-to-reverse bias switch. As it can be seen, diodes exhibit, after reaching the 0.6-Amp reverse current, soft recovery in a time of approximately 16 ns.

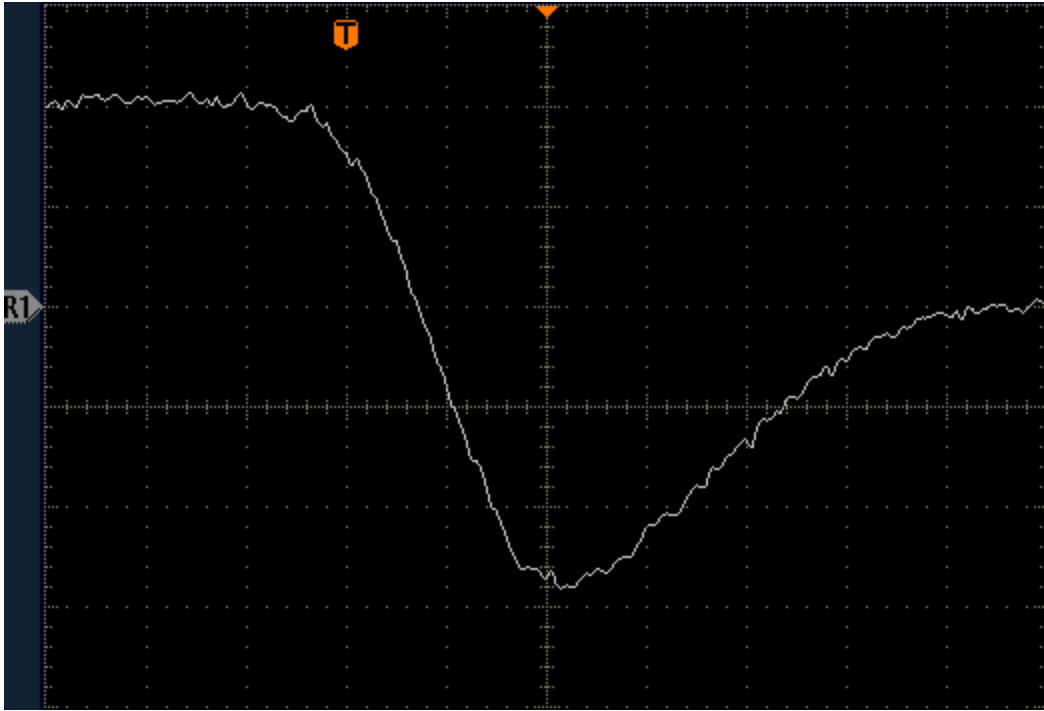


Fig. 7. Current tracing under forward-to-reverse bias switch for  $p^+n_0n^+$ -diodes. Vertical scale is 0.2 A/div, horizontal scale is 4 ns/div. Forward current is 0.4 A. Zero current level is shown by the R1-marker.

At a high reverse current, sweeping out the excess minority carriers from the diode base can be considered as a drift process until the depletion layer starts to restore [3]. It is well known that in 4H-SiC the electron mobility,  $\mu_n$ , is 5 - 7 times higher than the hole one,  $\mu_p$ . Besides, the density of injected electron-hole plasma at the left junction,  $n_l$ , is lowered as compared to that at the right junction,  $n_r$ , (see Fig. 8) due to the presence of a narrow layer at the blocking  $p^+n_0$ -junction, where the minority carrier lifetime  $\tau^*$  is much lower than the  $\tau$  value in the remaining part of the base [9].

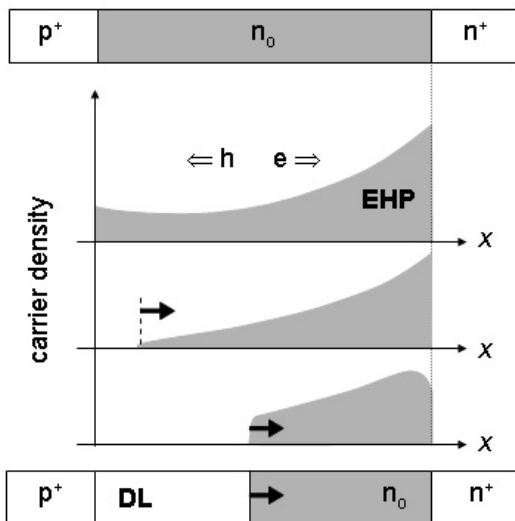


Fig. 8. Qualitative distributions of injected EHP during the recovery process for  $p^+n_0n^+$ -diodes.

For  $p^+n_0n^+$ -diodes, owing to  $\mu_n/n_l \gg \mu_p/n_r$ , the density of EHP at the blocking  $p^+n_0$ -junction rapidly decreases to zero, so that restoration of DL occurs in presence of the EHP. This predetermines soft recovery

behavior (see Fig. 8) that is governed by recombination and diffusion processes in the part of the base (adjoining the  $n^+n_0$ -junction) enriched by excess carriers.

*Conclusion:* in  $p^+n_0n^+$ -type diodes, it is failed to create high density electron-hole plasma layer at the blocking  $p^+n_0$ -junction. So, ultra-fast reverse current breaking off is hard to be realized in diodes of such type.

## V. 4H-SiC $p^+p_0n^+$ -diodes

### 1. Diode design

In order to achieve super-fast operation of devices based on SiC, it is suggested that the base region of  $p_0$ -type conductivity is used instead of  $n_0$ -type one. This allows to have  $p_0n^+$  -junction as blocking one. With lowered injection coefficient of non-blocking  $p^+p_0$ -junction, non-uniform EHP distribution with maximum density at the blocking  $p_0n^+$  -junction can be formed. It is worth nothing that plasma distribution is supposed to be not differ, in principle, for both 4H-SiC  $p^+n_0n^+$ - and  $p^+p_0n^+$ -diodes: compare Figs. 8 and 9, where qualitative EHP distributions during diode recovery are shown). Figure 9 depicts the predictable recovery process. The EHP wave front is formed near the  $p^+p_0$ -junction and moves towards the  $p_0n^+$ -junction with high velocity. Besides, the EHP density at the blocking  $p_0n^+$  junction starts to reduce slow. Certain conditions can be selected providing simultaneous events for the wave front to reach the  $p_0n^+$  junction and for EHP density to become zero here. Then the DL's boundary will move to the left with saturated velocity giving abrupt break of the reverse current.

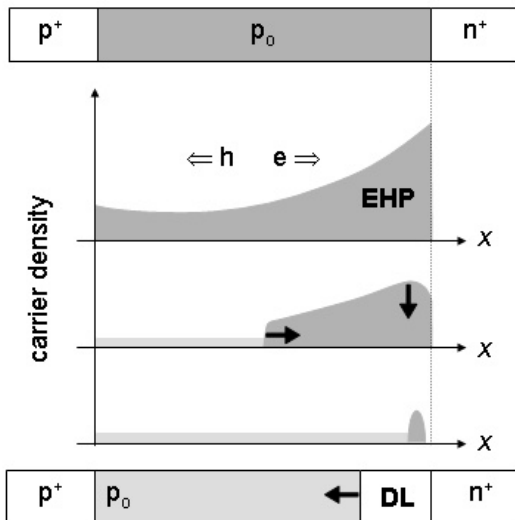


Fig. 9. Qualitative distributions of injected electron-hole plasma (EHP) during the recovery process for  $p^+p_0n^+$ -diodes.

### 2. Experimental details

Mesa-isolated 4H-SiC epitaxial diodes (Fig. 10) were fabricated on  $p^+/p_0/n^+$  homoepitaxial layers purchased from IMC (Stockholm, Sweden). The net acceptor concentration of 12- $\mu\text{m}$  thick aluminum (Al)-doped  $p_0$ -epilayer was  $8 \times 10^{14} \text{ cm}^{-3}$ . The Al-acceptor concentration of  $p^+$ -layers and the N-donor concentration of  $n^+$ -layers were designed to be  $10^{19} - 10^{20} \text{ cm}^{-3}$ .

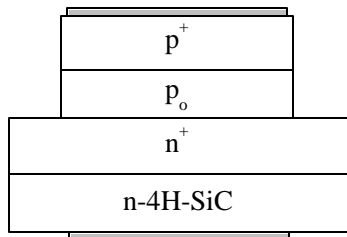


Fig. 10. Mesa-isolated 4H-SiC  $p^+p_0n^+$ -diodes.

### 3. Results and discussion

Typical C-V characteristic of a  $p^+p_0n^+$ -diode is shown in Fig. 11a, while Fig. 11b depicts calculated doping profile of the  $p_0$ -base.

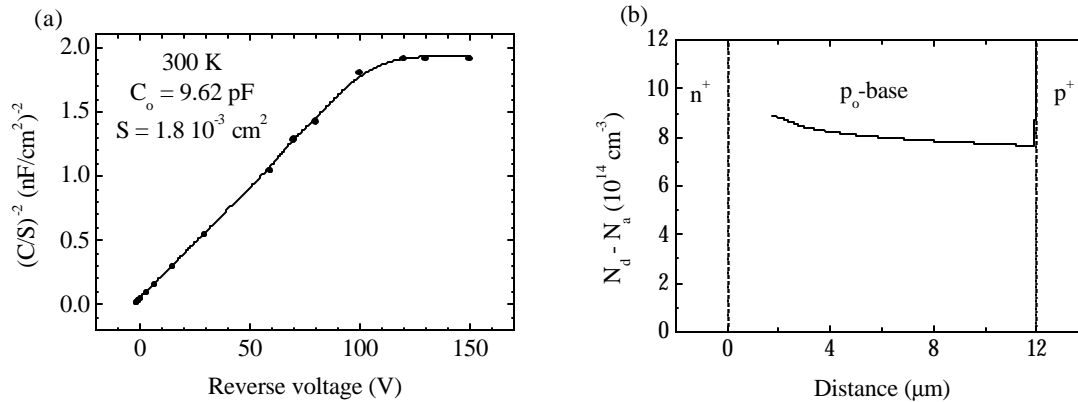


Fig. 11. Capacitance-voltage characteristics of a  $p^+n_0n^+$ -diode (a); doping profile in the  $p_0$ -base (b).

In the  $p^+p_0n^+$ -diodes, the hole density in the  $p_0$ -base slightly decreases as the distance from the  $p_0n^+$ -boundary increases. The average hole density is about  $8 \times 10^{14}$  cm<sup>-3</sup> (the thickness of the  $p_0$ -base layer is 12  $\mu$ m so that the base is fully depleted at a reverse voltage of about 100 V).

Actually, the recovery processes measured in  $p^+p_0n^+$ -diodes was found to be drastically differ from that in  $p^+n_0n^+$ -diodes (Fig. 12).

**At the same forward current and reverse voltage, maximum reverse current is noticeably higher and 1-Amp current is broken off very sharply in a time less than 1 ns.**

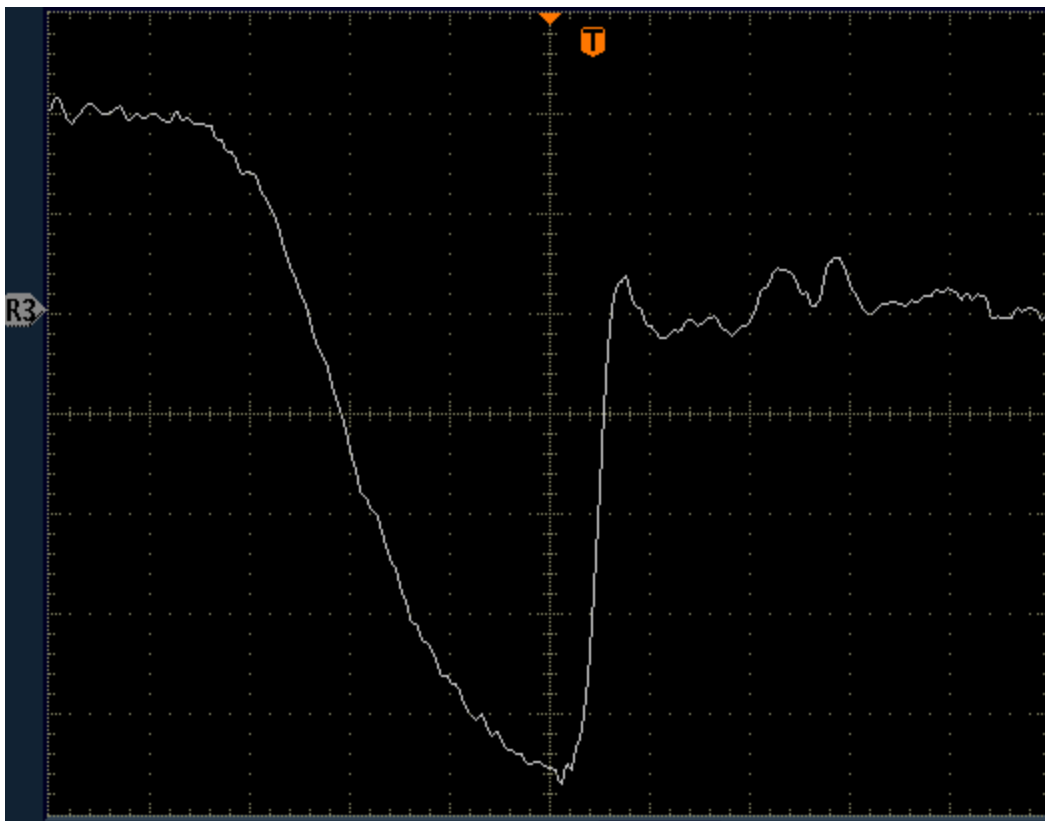


Fig. 12. Current tracing under forward-to-reverse bias switch for  $p^+p_0n^+$ -diodes. Vertical scale is 0.2 A/div, horizontal scale is 4 ns/div. Forward current is 0.4 A. Zero current level is shown by the R3-marker.

Such recovery behavior of the  $p^+p_0n^+$ -diodes evidences that practically all excess carriers are sustained away from the diode base by the instant for DL to start restoration, i.e. recombination and diffusion does not actually affect the recovery process which is governed by purely drift mechanism. Such mechanism under conditions when the carrier pumping is made by quasi-dc current is realized in Si-based  $p^+pnn^+$  IRDs [10,11] in which asymmetrical plasma distribution is formed by lowering, in a special manner, the injection coefficient of the  $nn^+$ -emitter.

As it was described earlier, the active current flowing through the diode during sweeping out the EHP is broken off sharply just after plasma disappearance. Then a displacement current is flowing through the diode due to the removal of the majority carriers from the base. Simultaneously the depleted layer starts to restore. The displacement current decreases in time, in opposite the voltage drop across the restoring depleted layer being increased. The time interval that is needed for the base to be clear of majority carriers can be calculated as

$$\Delta t = qpWS / \bar{i}_R, \quad (2)$$

where  $\bar{i}_R$  is the average reverse current,  $q$  is the electron charge,  $p$  is the carrier density in the base,  $W$  is the base thickness, and  $S$  is the diode area. When testing our 4H-SiC diodes we have found that reverse current of approximately 1 A is broken off most sharply. This current could be achieved after pumping the diode by 0.2 A forward current. With  $p = 8 \times 10^{14} \text{ cm}^{-3}$ ,  $W = 12 \text{ } \mu\text{m}$ ,  $S = 2.2 \times 10^{-3} \text{ cm}^2$  ?  $\bar{i}_R = 0.5$  ? the diode operation speed can be calculated to be about 0.6 ns that coincides well with experimental value.

*Conclusions:* The recovery properties of  $p^+p_0n^+$ -type diodes have been found to be differ from those of  $p^+n_0n^+$ -type ones. In  $p^+n_0n^+$ -type diodes, recombination and diffusion processes predetermine soft recovery behavior in a time of approximately 16 ns. In  $p^+p_0n^+$ -type diodes, purely drift mechanism is responsible, under proper conditions, for the very steep break of reverse current in a time  $\sim 1$  ns. This is due to that the base region of  $p_0$ -type conductivity allows to have  $p_0n^+$ -junction as blocking one. Owing to  $\mu_n/n_1 \gg \mu_p/n_r$ , fast restoration of DL occurs under the condition when there are no minority carriers in the diode base.

## VI. Generation of voltage pulses with $p^+p_0n^+$ -type diodes

### 1. Packaging the 4H-SiC diodes

Platelets with matrixes of 4H-SiC  $p^+p_0n^+$ -diode structures were cut into separate chips with the use of an equipment for laser cutting the crystals. The dimension of a separate chip is  $1.8 \text{ mm} \times 1.8 \text{ mm}$ . Metal-glass cases were used for packaging the chips. The placing of a diode in a case is shown in Fig. 13. Chips were stuck onto the package body by a conductive adhesive containing silver powder. Diode anode and cathode regions were connected to the package stems via ultrasonic welding of Al wires of 50  $\mu\text{m}$  in diameter (three Al pieces were used for each wire bridge). The anode stem (connected to  $p^+$ -region of the diode) is located near the package marker jut. The package covers were stuck to the package base.

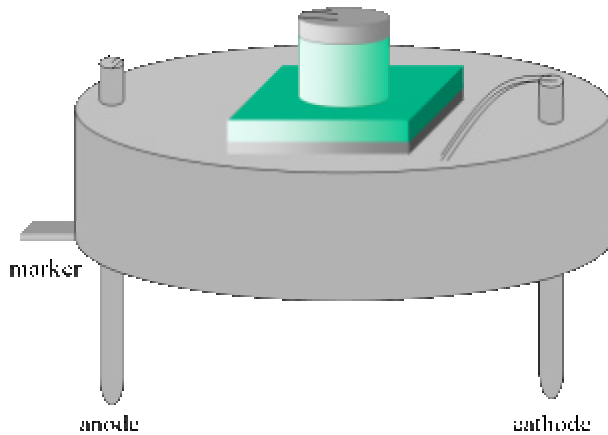


Fig. 13. 4H-SiC diode packaging.

2. Electronic pulse generator (in accordance with the Project Work Plan, electronic generator and 10 capsulated 4H-SiC diodes were delivered to the Partner at AFL).

*Principle circuit of pulse generator.*

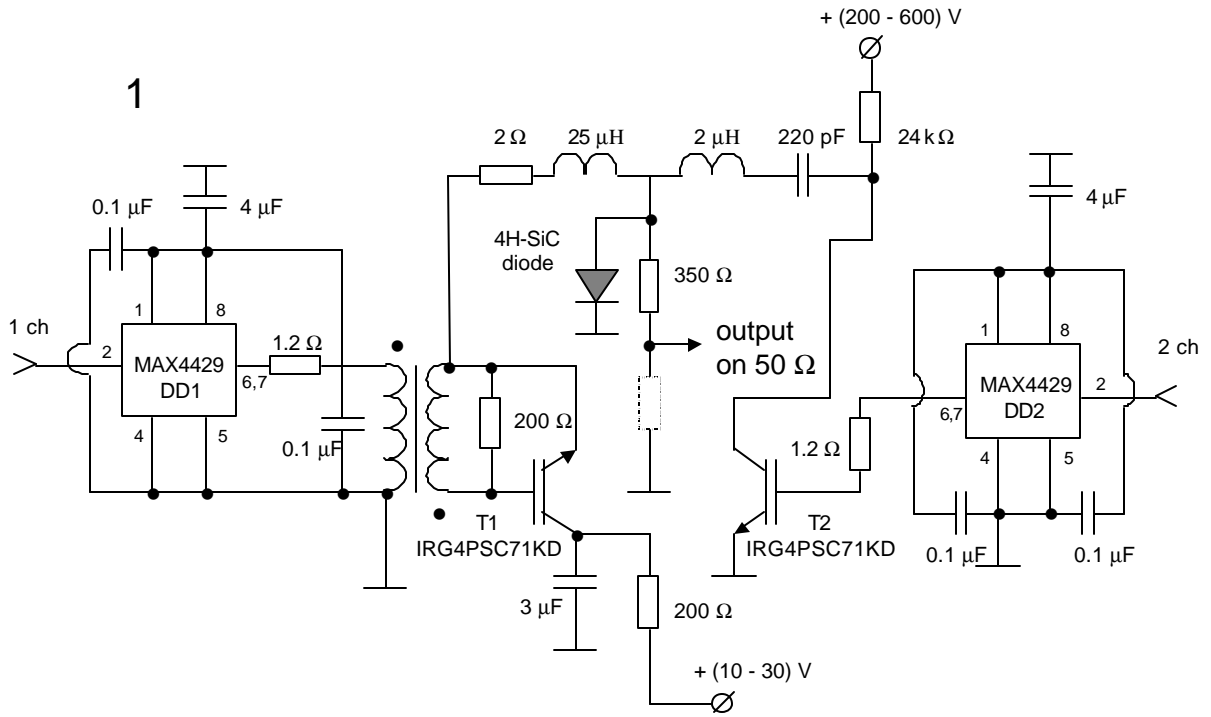


Fig. 14(1). Power part of the pulse generator.

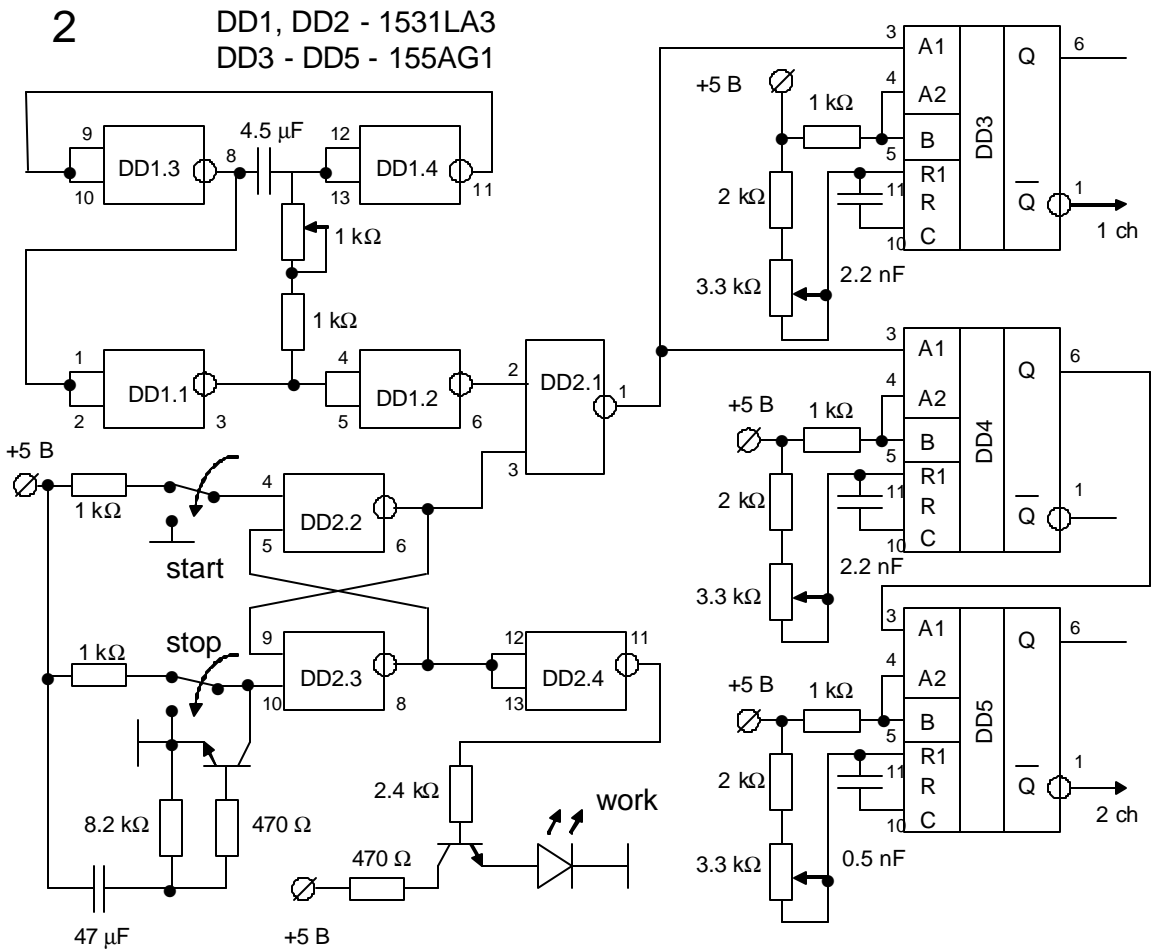


Fig. 14(2). Control circuit for triggering the IGBT-switches in the power part.

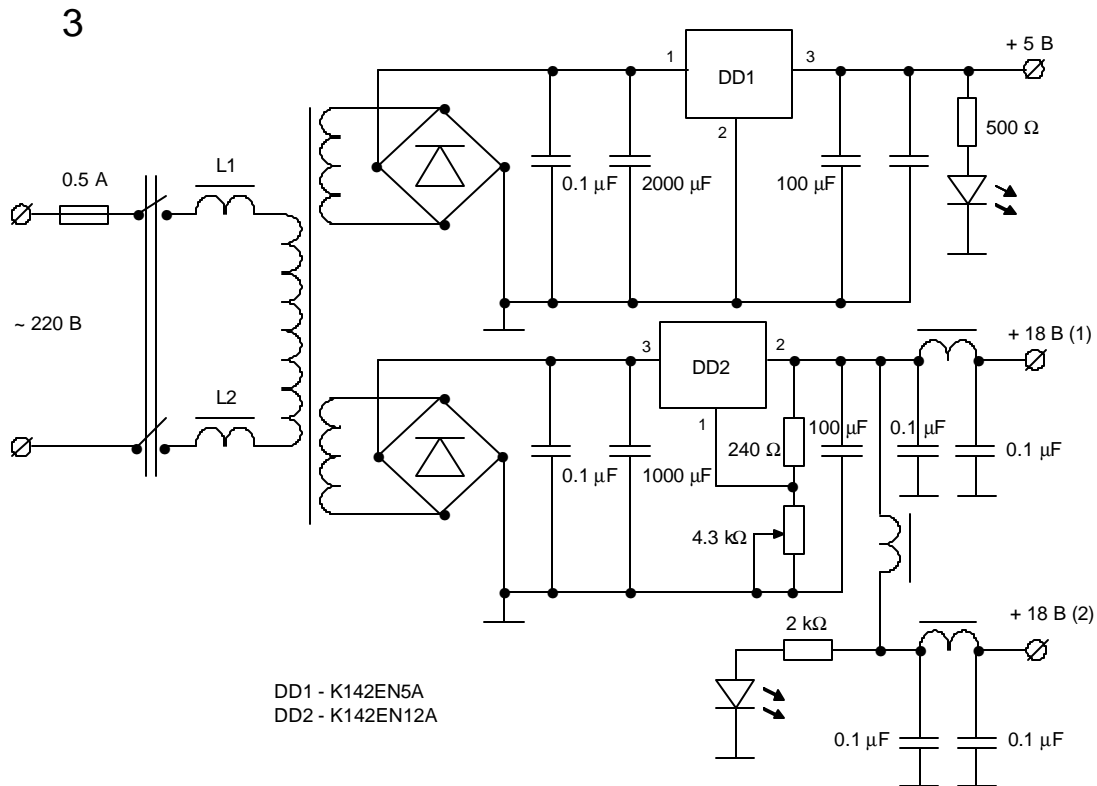




Fig. 14(3). Circuit for making DC supplies for ICs of the control circuit and for IGBT-switch drivers.

We have fabricated pulse power generator with an inductive energy storing unit as described, for example, in Ref. [11].

The power part of the generator (see Fig. 14(1)) includes a circuit for pumping the diode by electron-hole plasma under flowing the forward current and a circuit for sweeping out the plasma by a reverse current.

In the pumping circuit the capacitor 3  $\mu\text{F}$  is charged through the resistor 200  $\Omega$ . The discharge loop contains the IGBT-switch T1 (IRG4PS71KD), separating inductance 25  $\mu\text{H}$  and current limiting resistor 2  $\Omega$ . At the start state, the capacitor 3  $\mu\text{F}$  is charged to 10 – 30 V from a DC current source. After the IGBT-switch T1 is turned on by the driver DD1 (MAX4429) the capacitor 3  $\mu\text{F}$  is discharged through the 4H-SiC diode allowing forward condition. The duration of the forward pumping is of about 1  $\mu\text{s}$  that is enough to achieve steady-state plasma distribution in the diode base. Some change of the forward pulse width can be made by the control circuit (see Fig. 14(2)).

In the sweeping-out circuit the capacitor 220 pF is charged through the resistor 24 k $\Omega$ . The discharge loop contains the IGBT-switch T2 (IRG4PS71KD) and energy storing inductance 2  $\mu\text{H}$ . At the start state, the capacitor 220 pF is charged to 200 – 600 V from a DC current source. When the IGBT-switch T2 is turned on by the driver DD2 (MAX4429), after some delay with respect to triggering the switch T1, the capacitor 220 pF is discharged through the 4H-SiC diode allowing reverse condition. Some change of the delay time can be made by the control circuit (see Fig. 14(2)). During the stage of high reverse conduction, the minority carriers are carrying out from the diode and then the reverse current is broken off sharply. The current is passed to a load resistance 350  $\Omega$  connected in diode parallel. So, high voltage pulse is formed in the load.

The control circuit (see Fig. 14(2)) that controls triggering the IGBT-switches contains 1) the master pulse generator built with logic IC DD1 (the repetition frequency is of about 50 Hz; it can be slightly change by the correcting resistor 1 k $\Omega$ ), 2) the system for starting and terminating the control signals built with logic IC DD2, 3) the maker of triggering pulses to switch IGBT-T1 built with IC DD3 (the pulse width of about 1  $\mu\text{s}$  can be slightly changed by he correcting resistor 3.3 k $\Omega$ ), 4) the maker of the delay for switching the IGBT-T2 built with IC DD4 (the duration of about 1  $\mu\text{s}$  can be slightly changed by the correcting resistor 3.3 k $\Omega$ ), 5) the maker of triggering pulses to switch IGBT-T2 built with IC DD5 (the pulse width of about 1  $\mu\text{s}$  can be slightly changed by the correcting resistor 3.3 k $\Omega$ ).

Circuit shown in Fig. 14(3) is intended for making DC supplies for ICs of the control circuit and for drivers of IGBT-switches. It makes constant-voltage power supply of +5 V (for ICs of the control circuit) and two ones of +18 V (for drivers of IGBT-switches).

*Instruction on starting and shutting down the device.*

Starting:

1. Plug in the device to the AC power supply of 220 V. Two LEDs must be flashed indicating circuit energization by +5 V and +18 V.
2. Plug in the device to the constant-voltage power supplies for pumping and sweeping-out circuits and establish voltages of +20 V and +400 V, respectively.
3. Plug in the generator output to the oscilloscope through an 20 dB attenuator with 50  $\Omega$  input impedance.
4. Push the "start" button.

Shutting down:

1. Disconnect the device and constant-voltage power supplies +20 V and +400 V. Wait some time for the capacitors to be discharged (about ten seconds).
2. Push the "stop" button.
3. Disconnect the device from AC power supply.

### 3. Experimental results and discussion

400-V pulses generated with a 4H-SiC  $\text{p}^+\text{p}_0\text{n}^+$ -diode are shown in Fig. 15. As seen, the voltage rise time of about 4 ns is several times higher as compared with that in Fig. 12 and calculated by Eq. (2).

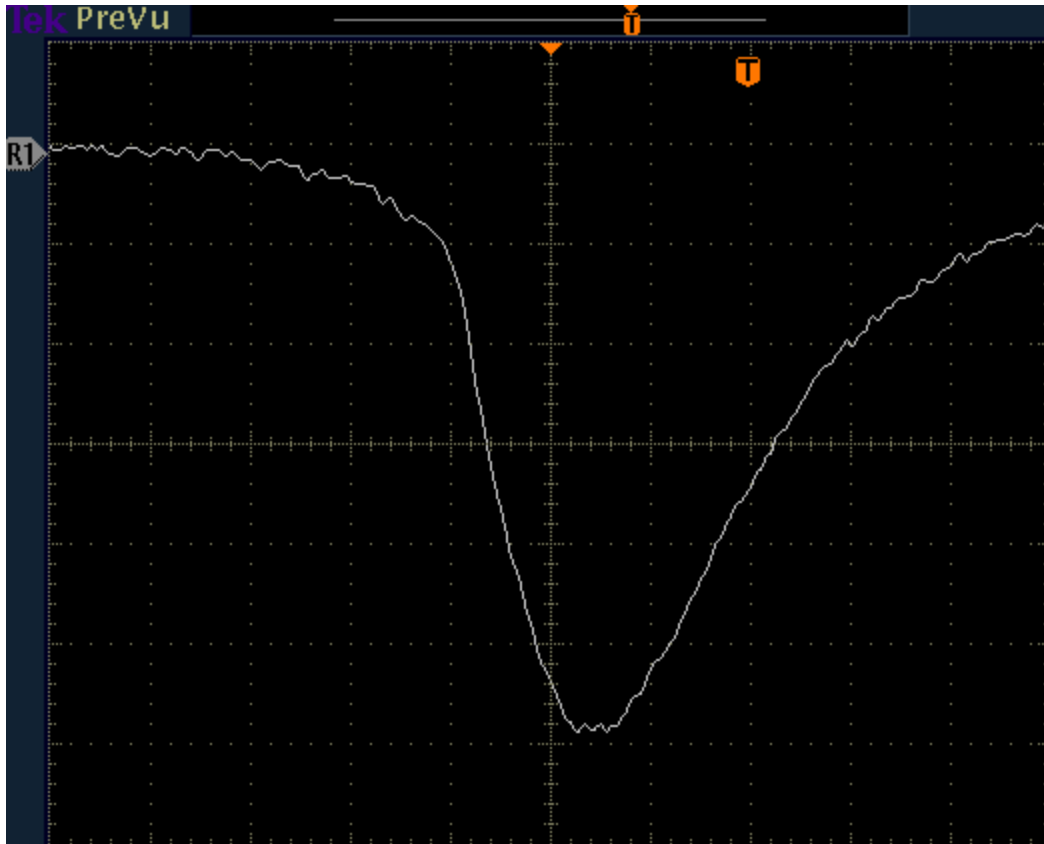


Fig. 15. 400-V pulses generated by the pulse generator with 4H-SiC diode. Vertical scale is 70 V/div, horizontal scale is 4 ns/div. Zero voltage level is shown by the R1-marker.

This can be easily explained if we consider the simple equivalent circuit shown in Fig. 16.

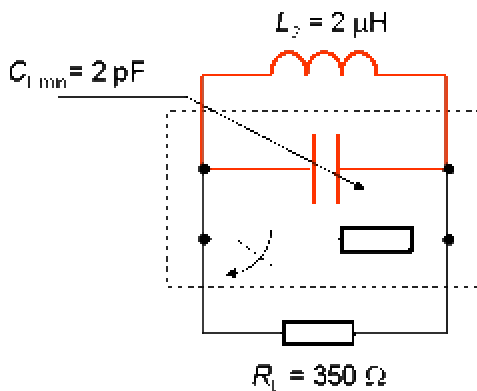


Fig. 16. The equivalent circuit showing the influence of some reactances on generation of the voltage pulses.

The circuit contains some reactances namely energy storing inductance and non-linear 4H-SiC  $p^+p_0n^+$ -diode capacitance. It is clear that the voltage rise time can be determined by the characteristic time of LC-tank shown, with two stages of voltage rise being as follows:

- 1) at the first stage of DL's restoration the diode capacitance is high resulting in comparatively slow voltage rise. But, as voltage increases the capacitance decreases resulting in more and more steep voltage rise;
- 2) at the second stage when the capacitance is saturated at a voltage of about 100 V (see C-V characteristic in Fig. 10a) the voltage rise rate become to be maximum and practically constant one. At this stage, the voltage rises from 100 V to its maximum value of 400 V in a time of about 3 ns. At 100-V voltage the capacitance is about 2 pF. With the storing inductance of 2  $\mu$ H, the calculated voltage rise time can be calculated as a quarter of the oscillation period:

$$\Delta t_{LC} = \frac{T_{LC}}{4} = \frac{P}{2} \sqrt{L_2 C_{Dmin}} = 3.1 \text{ ns} \quad (3)$$

that coincides well with the experimental value.

*Conclusions:* It can be concluded that with 4H-SiC  $p^+p_0n^+$ -layered diodes it is possible to produce IRDs having operation speed less than 1 ns. To realize such devices it is necessary to optimize the device structure namely to increase the base thickness and diode area. The first will allow to reduce the diode capacitance and increase the maximum blocking voltage. The second will allow to increase the reverse current and reduce the storing inductance. As a whole, such optimizations must improve the device operation speed. In particular, in the next Section an estimate of possibility to create 4H-SiC based 100-kV, 1-ns DSRD devices is made.

## VII. Estimate of possibility to create 4H-SiC based 100-kV, 1-ns DSRD-devices

Now we consider in short the possibility to construct 100-kV, 1-ns 4H-SiC opening switches. It seems that only several devices connected in a stack could support 100-kV voltage. IRD-type devices connected in stack are hardly to work properly because of non-identical EHP's distribution under quasi-dc current and, consequently, non-simultaneous breaking off the reverse current. In opposite, DSRD-type devices can be connected in stack because that in case of pumping the diode by short pulses non-steady-state EHP's distribution is less sensitive to individual diode properties.

So, the task is to estimate parameters of 100-kV breakdown voltage ( $V_b$ ), 1-ns operation time ( $\Delta t$ ) 4H-SiC DSRD-stack which has to operate in a circuit with an inductive energy storing unit, with a load resistance of  $100 \Omega$  as an upper load limit.

1. The reverse current,  $i_R$  that has to be broken off is calculated as  $i_R = V_b / R_L = 1 \text{ kA}$ .

2. Let us consider a diode stack containing 5 single DSRD-chips each being able to support 20-kV breakdown voltage  $V_b$ . Then the density of dopants in the diode base can be calculated as

$$N = \frac{\epsilon E_b^2}{2qV_b} \quad (4)$$

where  $\epsilon$  is the dielectric constant. With  $E_b = 2 \text{ MV/cm}$  and  $V_b = 20 \text{ kV}$ , the  $N$  value is calculated to be  $5.5 \times 10^{14} \text{ cm}^{-3}$ . Note that such doping level is achieved in 4H-SiC epilayers grown by CVD without problems [12].

3. The corresponding thickness of the diode base,  $W$  can be calculated as

$$W = \frac{2V_b}{E_b} \quad (5)$$

that is equal to  $200 \mu\text{m}$  in our consideration.

4. The lowest time of flight of majority carriers through the  $200\text{-}\mu\text{m}$  diode base is calculated as

$$\Delta t = \frac{W}{v_s} \quad (6)$$

With  $v_s = 2 \times 10^7 \text{ cm/s}$ , one can calculate  $\Delta t = 1 \text{ ns}$  that meet our requirement to operation speed.

5. The required diode area,  $S$  can be derived from Eq. (2) as

$$S = \frac{\bar{i}_R \Delta t}{qNW} \quad (7)$$

With  $\bar{i}_R = 500 \text{ A}$ , one can calculate  $S = 0.28 \text{ cm}^2$ . As to  $W = 200 \mu\text{m}$  and  $S = 0.28 \text{ cm}^2$ , it is worth nothing that Cree has recently reported characteristics of 20-kV diodes with  $150\text{-}\mu\text{m}$  thick base and 3 mm in diameter (the diode area of about  $0.1 \text{ cm}^2$ ) [13].

6. Let us now to estimate the characteristic time of LC-tank,  $\tau_{LC}$ , in a circuit with inductive energy storing unit. The minimum capacitance of a single diode,  $C_{min}$  is calculated as

$$C_{\min} = \frac{eS}{W} \quad (8)$$

In our consideration,  $C_{\min} = 12.4$  pF. The resulting capacitance of the diode stack will be  $C = C_{\min} / 5 \approx 2.5$  pF.

The value of storing inductance,  $L$  can be calculated from the energy balance,  $Li_R^2 = CV_b^2$ , to be  $L = 25$  nH. With the storing inductance of 25 nH, the calculated voltage rise time can be calculated as a quarter of the oscillation period:

$$\Delta t_{LC} = \frac{T_{LC}}{4} = \frac{P}{2} \sqrt{LC} = 0.2 \text{ ns} \quad (9)$$

that is less than the time of flight calculated by Eq. (6). So, the operation speed will be determined by the time of flight, i.e. about 1 ns.

7. In a DSRD-device, the pumped charge,  $i_F \Delta t_f$  has to be equal to swept out charge,  $\bar{i}_R \Delta t_R$ . If the  $\Delta t_R$  value is limited, for example, by 10 ns, then the pumped (or swept out) charge is calculated to be  $5 \times 10^{-6}$  Cl. On the other hand, if the forward current is limited by a value of 50 A, then the pumping duration,  $\Delta t_f$  should be at least 10 times higher than the  $\Delta t_R$ , i.e. 100 ns. This means that the minority carrier lifetime  $\tau$  must be of about 1  $\mu$ s (the  $\tau$  value should be at least one order of magnitude longer than  $\Delta t_f$  in order to provide no carrier recombination in the base during pumping process). It is a quite reasonable value for modern 4H-SiC diodes grown by CVD (see, for example, Ref. [14]).

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## List of published papers and reports with abstracts

- I I. V. Grekhov, P. A. Ivanov, A. O. Konstantinov, and T. P. Samsonova. On the Possibility of Creating a Superfast-Recovery Silicon Carbide Diode. - Techn. Phys. Lett., Vol. 28, N7, pp. 544-546 (2002).**

Abstract:

The possibility of a superfast (<1 ns) termination of the reverse current during the recovery of a 4H-SiC diode with a  $p^+p_0n^+$  structure is experimentally demonstrated for the first time. It is shown that the recovery process is much like that taking place in inverse-recovery silicon diodes.

## List of presentations at conferences and meetings with abstracts

- II Grekhov I.V., Ivanov P.A., Konstantinov A.O. 4H-SiC inverse recovery diodes (IRD) for sub-nanosecond power opening switches. - Abstracts of the AMEREM'2002, June 02-07, 2002, Annapolis, MD, p. 59.**

Abstract:

4H-SiC  $p^+p_0n^+$ -diodes have been fabricated and tested in a special circuit which allows to form steep high-voltage pulses owing to IRD's ability to break off abruptly the reverse current after forward-to-reverse switch [I.V. Grekhov. *Abstracts of the 11<sup>th</sup> Pulsed Power Conference, Baltimore (USA), 1997, p. 108*]. General rationale for SiC comes from that the maximum voltage rise rate  $(dV/dt)_{\max}$  is limited by the product of the breakdown field and the saturated drift velocity of electrons:  $(dV/dt)_{\max} = E_b v_{\text{sat}}$ . In case of Si IRDs,  $(dV/dt)_{\max} = 2 \times 10^{12}$  V/s, while  $(dV/dt)_{\max} = 6 \times 10^{13}$  V/s in case of 4H-SiC diodes. In particular this means that the voltage rise time in SiC based IRDs can be at least one order of magnitude shorter as compared to Si devices, with the same blocking voltage rating. Besides, higher background doping in the base, higher working temperature, and higher thermal conductivity of SiC allows for SiC IRDs to have much higher current density at the same diode working voltage.

4H-SiC epitaxial diodes were fabricated on  $p^+/p_0/n^+$  homoepitaxial layers grown on heavily-doped n-type substrates purchased from Cree Inc. Epitaxial growth was performed by atmospheric-pressure CVD in a  $\text{SiH}_4\text{-C}_3\text{H}_8\text{-H}_2$  system. The Al-acceptor concentration of  $p^+$ -layers and the N-donor concentration of  $n^+$ -layers were designed to be  $10^{19}$  -  $10^{20}$   $\text{cm}^{-3}$ . The net acceptor concentration of 12- $\mu\text{m}$  thick aluminum (Al)-doped  $p_0$ -epilayers was determined to be  $8 \times 10^{14}$   $\text{cm}^{-3}$  by capacitance-voltage measurements. In order to confine the blocking  $p_0n^+$ -junctions, diodes were processed into a mesa structure with more than 12- $\mu\text{m}$  height by reactive ion etching (RIE) using pure  $\text{SF}_6$  gas. Al-based metallization was employed as ohmic contacts on both top  $p^+$ -layers and back-side n-type substrate, respectively. The diode diameters were designed to be 500  $\mu\text{m}$ .

Quasi steady-state forward current was varied from 2 to 10 A. Just after a diode is rapidly switched from the initial forward bias to a reverse condition, a stage of high reverse current (HRC) can be clearly observed. Then the reverse current is broken off very sharply in a time less than 1 ns. Such recovery mechanism under quasi-dc forward current is realized in Si-based  $p^+pnn^+$ -IRD. In Si IRD, the injection coefficient of the  $n^+$ -emitter is lowered by special manner. So, high density electron-hole (EH) plasma is located mainly at the left of pn-junction. With the ratio  $\mu_n/\mu_p = 3$  in silicon, this allows for the EH-plasma fronts to collide, under a reverse condition, exactly at the pn-junction. In this case, practically all excess carriers are sustained away from the base regions by the instant of finishing the HRC stage, i.e. recombination and diffusion does not actually affect the recovery process which is governed by pure drift mechanism. Owing to poor injection ability of  $p^+$ -emitters in SiC, asymmetrical plasma distribution seems to be realized in 4H-SiC  $p^+p_0n^+$ -diodes, the carrier density at the blocking  $p^+n_0$ -junction being much lower than that at the  $n^+n_0$ -junction. The EH-plasma front on the  $p^+$ -site is moved toward the blocking  $p_0n^+$ -junction with higher velocity as compared to that on the  $n^+$ -site (due to higher electron mobility as compared to hole one). So, the space charge region at the blocking  $p^+n_0$ -junction is not restored until EH-plasma is collided at the blocking junction like in Si-based IRDs. With 4H-SiC  $p^+p_0n^+$ -diodes, the reverse current was found to be broken in a time less than 1 ns allowing to develop a voltage pulse of about 500 V in a 50- $\Omega$  load connected in diode parallel.

- III Ivanov P.A., Grekhov I.V., Konstantinov A.O., Samsonova T.P. Reverse Current Recovery in 4H-SiC Diodes with n- and p-Base. – To be published in Proc. of the 4rd European Conference on Silicon Carbide and Related Materials – 2002, Lincoping, Sweden, Sept. 2 - 5, 2002.**

Abstract:

Mesa-isolated 4H-SiC junction diodes were fabricated on both  $p^+/n_0/n^+$  and  $p^+/p_0/n^+$  homoepitaxial layers by CVD. The net donor concentration of 40- $\mu\text{m}$  thick nitrogen (N)-doped  $n_0$ - and acceptor concentration of 12- $\mu\text{m}$  thick aluminum (Al)-doped  $p_0$ -epilayers were  $(3 - 5) \times 10^{14} \text{ cm}^{-3}$  and  $8 \times 10^{14} \text{ cm}^{-3}$ , respectively. The Al-acceptor concentration of  $p^+$ -layers and the N-donor concentration of  $n^+$ -layers were  $10^{19} - 10^{20} \text{ cm}^{-3}$ .

Transient processes were studied using an electrical circuit schematically shown in Fig. 1. The forward current pulse was formed by the discharge of the capacitor  $C_1$  through the loaded diode ( $R_L$  load) when the switch  $S_1$  (Si thyristor) is short-circuited. Reverse current transients were recorded by a stroboscopic oscilloscope when diodes were rapidly switched (using the discharge of the capacitor  $C_2$  when the switch  $S_2$  (Si IGBT) was short-circuited after appropriate delay) from the initial forward bias of 2 A ( $V_1 = 200 \text{ V}$ ) to reverse bias ( $V_2 = 275 - 500 \text{ V}$ ). The pulse rise time was about 20 ns that is given by operating speed ( $\Delta t_r$ ) of Si IGBT.

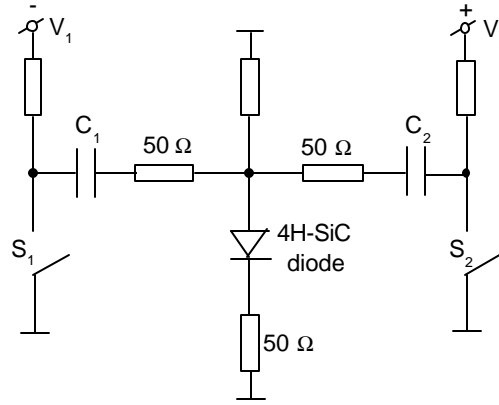


Fig. 1. Electrical circuit to be used for the measurements of transient characteristics of the diodes.

Fig. 2a shows typical reverse current recovery waveforms in  $p^+n_0n^+$ -diodes under a forward-to-reverse bias switch (at  $V_2 = 350 \text{ V}$ ). If the condition  $\Delta t_r \ll \tau$  ( $\tau$  is the carrier lifetime) is satisfied, a finite in time stage of High Reverse Current (HRC) must be observed on the current tracing, the reverse current value and the stage duration being  $I_r = (V_2 - V_1)/3R_L = 1 \text{ A}$  and  $\Delta t_{\text{HRC}} \sim \tau$ .

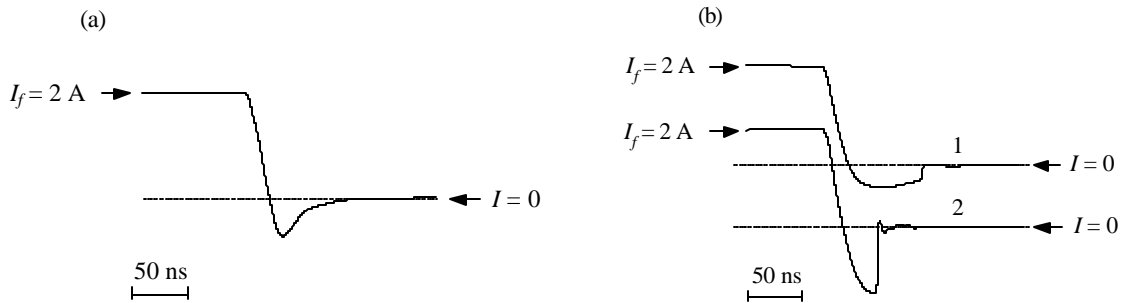


Fig. 2. Current tracing under forward-to-reverse bias switch; (a)  $p^+n_0n^+$ -diodes:  $V_2 = 350 \text{ V}$ ; (b)  $p^+p_0n^+$ -diodes:  $V_2 = 275 \text{ V}$  (1) and  $V_2 = 500 \text{ V}$  (2).

However, no HRC stage was found on the current tracing, with the maximum value of reverse current being lower than 1 A. Besides the reverse current felt down rather slowly in a time of approximately 100 ns. Such transient behavior of the  $p^+n_0n^+$ -diodes under forward-to-reverse switch has been reported elsewhere [1]. The above forward-to-reverse switching features result from the presence of a narrow layer at the blocking  $p^+n_0$ -junction, where the minority carrier lifetime  $\tau^* \ll \Delta t_r$  is much lower than the  $\tau$  value in the remaining part of the base (several hundreds nanoseconds). In such situation the steady-state distribution of injected carriers in the base seems to be asymmetrical (Fig. 3) so that the carrier density at the blocking  $p^+n_0$ -junction remains much lower than that at the  $n^+n_0$ -junction. After the diode switching, the Space Charge Region (SCR) at the blocking

$p^+n_o$ -junction is restored in a short period of time of about  $\tau^*$ . That results in ulterior HRC stage, while the recovery of reverse current is governed by slow recombination and diffusion processes in the part of the base (adjoining the  $n^+n_o$ -junction) enriched by excess carriers.

The recovery processes in  $p^+p_o n^+$ -diodes shown in Fig. 2b at  $V_2 = 275$  and 500 V drastically differ from that in  $p^+n_o n^+$ -diodes.

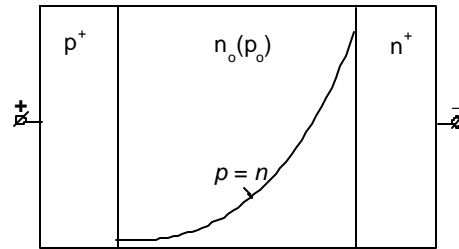


Fig. 3. Qualitative minority carrier distribution in the base of  $p^+n_o n^+$ - and  $p^+p_o n^+$ -type diodes under steady-state forward current.

The HRC stage is clearly observed in Fig. 2b (curve 1) at  $V_2 = 275$  V. The reverse current during the HRC stage equals to the expected value of  $I_r = (V_2 - V_1)/3R_L = 0.5$  ? , with  $\Delta t_{\text{HRC}} \approx 60$  ns. In addition, the reverse current fall time is shorter as compared to that in  $p^+n_o n^+$ -diodes. The maximum reverse current neatly grows with increasing  $V_2$ , with both HRC stage and fall time stage became shorter, so that the reverse current is broken off very sharply in a time of about 1 ns. Such recovery behavior of the  $p^+p_o n^+$ -diodes evidences that practically all excess carriers are sustained away from the base by the instant of finishing the HRC stage, i.e. recombination and diffusion does not actually affect the recovery process which is governed by purely drift mechanism (see, for example, Ref. [2]). Such mechanism under conditions when the carrier pumping is made by quasi-dc current is realized in Si-based  $p^+pnn^+$ -IRD [2]. In Si IRD, the diffusion effects are minimized due to lowering, in a special manner, the injection coefficient of the  $n^+n$ -emitter. With such a method, high density electron-hole plasma is located mainly at the left of pn-junction. Similar situation with asymmetrical plasma distribution seems to be realized in 4H-SiC  $p^+p_o n^+$ -diodes under investigation (see Fig. 3). It is worth nothing that plasma distribution is supposed to be not differ, in principle, for both 4H-SiC  $p^+n_o n^+$ - and  $p^+p_o n^+$ -diodes. But the very different recovery behavior in  $p^+p_o n^+$ -diodes is explained by that the high density plasma layer is located, in contrast to  $p^+n_o n^+$ -diodes, namely at the **blocking** junction. Besides the plasma layer edge on the  $p^+$ -site moves, toward the blocking junction, with higher velocity as compared to that on the  $n^+$ -site (due to higher electron mobility as compared to hole one). It is important feature in order to achieve the plasma disappearance exactly at blocking junction, like in Si IRDs.

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2. I.V. Grekhov. Abstracts of the 11<sup>th</sup> Pulsed Power Conference, Baltimore (USA), 1997, p. 108.

### **III. PROJECT SUMMARY FOR UNRESTRICTED DISTRIBUTION**



ISTC 2049p

**Final  
Project Technical Report  
of ISTC 2049p**

**Research and Development  
of Silicon Carbide (SiC) Junction Recovery Diodes  
for Picosecond Range, High Power Opening Switches**  
(From 1 August 2001 to 31 July 2002 for 12 months)

**Igor Vsevolodovich Grekhov  
(Project Manager)  
Ioffe Physico-Technical Institute of Russian Academy of Sciences**

July 2002

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This work was supported financially by European Office of Aero-space Research and Development (EOARD), London as the Partner and performed under the contract to the International Science and Technology Center (ISTC), Moscow

Research and Development of Silicon Carbide (SiC) Junction Recovery Diodes  
for Picosecond Range, High Power Opening Switches  
(from 1 August 2001 to 31 July 2002 for 12 months)

Grekhov Igor Vsevolodovich (Project Manager)  
Ioffe Physico-Technical Institute of Russian Academy of Sciences

The objective of the project is to fabricate, test, and characterize 4H-SiC power semiconductor opening switches (OS) operating in the sub-nanosecond range of switch time. Preliminary estimations showed that due to unique properties of silicon carbide parameters of SiC-based pulse power opening switches can be substantially improved, compared to both Si and GaAs capabilities.

Special 4H-SiC diode structures were fabricated and investigated in regimes known for Si-based opening switches such as Inversion Recovery Diodes (IRD). The operation of such diodes is founded on the superfast breaking off the diode reverse current after switching the device from forward to reverse bias conditions.

The following work have been performed in course of the project:

1. calculations of possible parameters of 4H-SiC based OS,
2. fabrication of 4H-SiC diode structures,
3. measurements of static and transient characteristics of the devices,
4. analysis of junction recovery mode of operation.

Some conclusions regarding to possible ways of 4H-SiC material improvement in order to develop high voltage SiC-based OS-devices have been made.

Keywords: Semiconductor Opening switches, High power, Sub-nanosecond operation, Silicon carbide

**The work has been performed by  
the following institutes and partners**

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Some conclusions regarding to possible ways of 4H-SiC material improvement in order to develop high voltage SiC-based OS-devices have been made.

4H-SiC epitaxial diodes were fabricated on both  $p^+/n_0/n^+$  and  $p^+/p_0/n^+$  homoepitaxial layers grown on heavily-doped n-type substrates purchased from Cree Inc. Epitaxial growth was performed by atmospheric-pressure chemical vapor deposition (CVD) in a  $\text{SiH}_4\text{-C}_3\text{H}_8\text{-H}_2$  system. Substrates with  $8^\circ$  off-angles were used to realize homoepitaxy through step-flow growth. The growth temperature was  $1500^\circ\text{C}$ , at which a growth rate of about  $4\ \mu\text{m/h}$  was obtained. The net donor concentration of  $40\text{-}\mu\text{m}$  thick nitrogen (N)-doped  $n_0$ - and acceptor concentration of  $12\text{-}\mu\text{m}$  thick aluminium (Al)-doped  $p_0$ -epilayers were determined to be  $(3 - 5)\times 10^{14}\ \text{cm}^{-3}$  and  $8\times 10^{14}\ \text{cm}^{-3}$ , respectively, by capacitance-voltage measurements. The Al-acceptor concentration of a  $1.5\text{-}\mu\text{m}$  thick  $p^+$ -layer and the N-donor concentration of a  $1.5\text{-}\mu\text{m}$  thick  $n^+$ -layer were designed to be  $10^{19}\ \text{cm}^{-3}$  on the order of magnitude. In order to confine the blocking  $p^+n_0(\text{top})$ - or  $p_0n^+(\text{bottom})$ -junctions, diodes were processed into a mesa structure by reactive ion etching using pure  $\text{SF}_6$  gas with an nickel (Ni) mask. Ni-based metallizations were employed as ohmic contacts on both top  $p^+$ -layers and back-side n-type substrate, respectively. Sintering at  $850^\circ\text{C}$  for 10 min was made to form ohmic contact characteristics. The diode diameters were designed to be  $600\ \mu\text{m}$ .

Recovery processes were studied using an electrical circuit schematically shown in Fig. 1. Forward current pulse was formed by discharge of capacitor  $C_1$  through the loaded diode ( $R_L$  load) when the switch  $S_1$  (Si thyristor) is short-circuited. Then the diode was rapidly switched (using the discharge of capacitor  $C_2$  when the switch  $S_2$  (Si IGBT) was short-circuited after appropriate delay) from the initial forward bias to reverse bias. The reverse current rise time was about 10 ns.

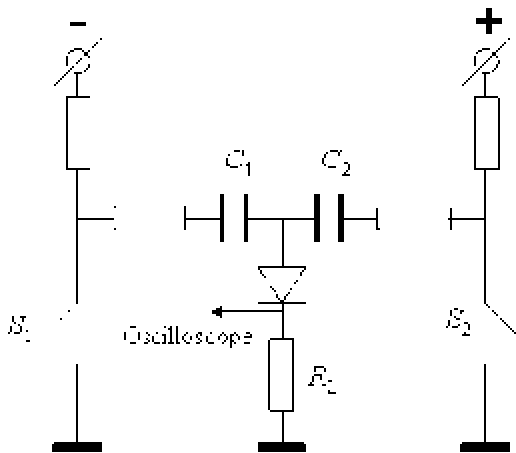


Fig. 1. Electrical circuit used for the measurements of recovery characteristics.

## Results and discussion

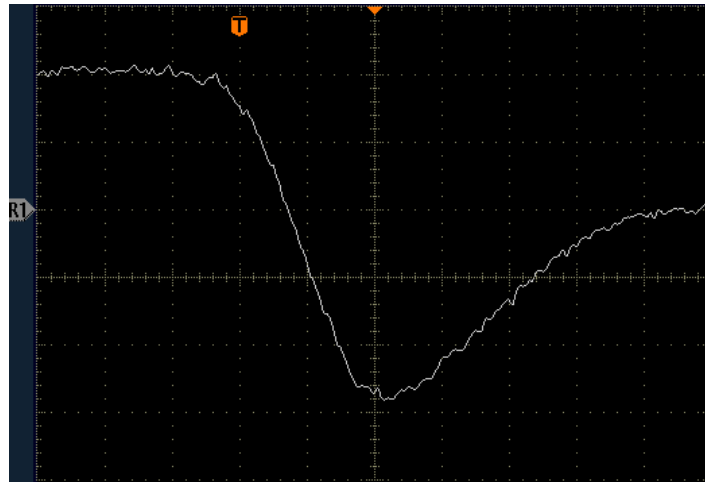
Figure 2a presents typical reverse current recovery in  $p^+n_0n^+$ -diodes under a forward-to-reverse bias switch. As it can be seen, diodes exhibit soft recovery in a time of approximately 16 ns. Figure 2b presents typical reverse current recovery in  $p^+p_0n^+$ -diodes. It drastically differs from that in  $p^+n_0n^+$ -diodes: i) at the same reverse voltage, maximum reverse current is noticeably higher and ii) 1-Amp current is broken off very sharply in a time of approximately 1 ns.

If the reverse current is essentially higher than forward one ( $I_r > I_f$ ), sweeping-out the excess minority carriers from the diode base can be considered as a drift process until the depletion layer (DL) starts to restore [4]. It is well known that in 4H-SiC the electron mobility,  $m_n$ , is 5 - 7 times higher than the hole one,  $m_p$ . Besides, the density of injected electron-hole plasma (EHP) at the left junction,  $n_l$ , is lowered as compared to that at the right junction,  $n_r$ , [5] (it is worth nothing that plasma distribution is supposed to be not differ, in principle, for both 4H-SiC  $p^+n_0n^+$ - and  $p^+p_0n^+$ -diodes: compare Figs. 3a and 3b, where qualitative EHP distributions during diode recovery are shown).

For  $p^+n_0n^+$ -diodes, owing to  $m_n/n_l \gg m_p/n_r$ , the density of EHP at the *blocking*  $p^+n_0$ -junction rapidly decreases to zero, so that restoration of DL occurs in presence of the EHP thus predetermining soft recovery behavior.

For  $p^+p_0n^+$ -diodes, the high density EHP is located, in contrast to  $p^+n_0n^+$ -diodes, at the *blocking*  $p_0n^+$ -junction. The EHP wavefront is formed near non-blocking  $p^+p_0$ -junction and moves towards the  $p_0n^+$ -junction with high velocity. Besides, the EHP density at the blocking  $p_0n^+$ -junction starts to reduce rather slow. Certain conditions can be selected providing simultaneous events for the wavefront to reach the  $p_0n^+$ -junction and for EHP density to become zero here. So, all excess carriers are sustained away from the base by the instant for DL to start restoration. Then the DL boundary will move to the right with saturated velocity giving abrupt break of the reverse current. Such mechanism is known to realize in Si-based inversion recovery diodes [6] which find applications for fabricating high voltage pulse power generators [7].

(a)



(b)

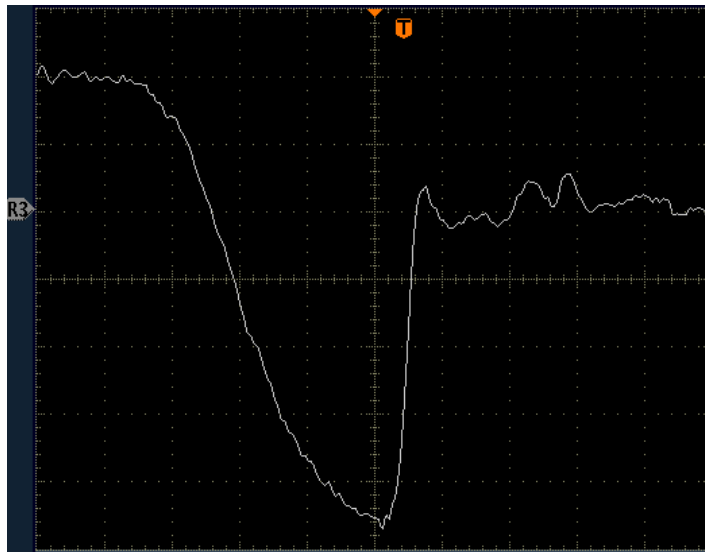


Fig. 2. Current tracings under forward-to-reverse bias switch: (a) -  $p^+n_0n^+$ -diodes, (b) -  $p^+p_0n^+$ -diodes. Vertical scale is 0.2 A/div, horizontal scale is 4 ns/div. Forward current is 0.4 A. Zero current level is shown by R-markers.

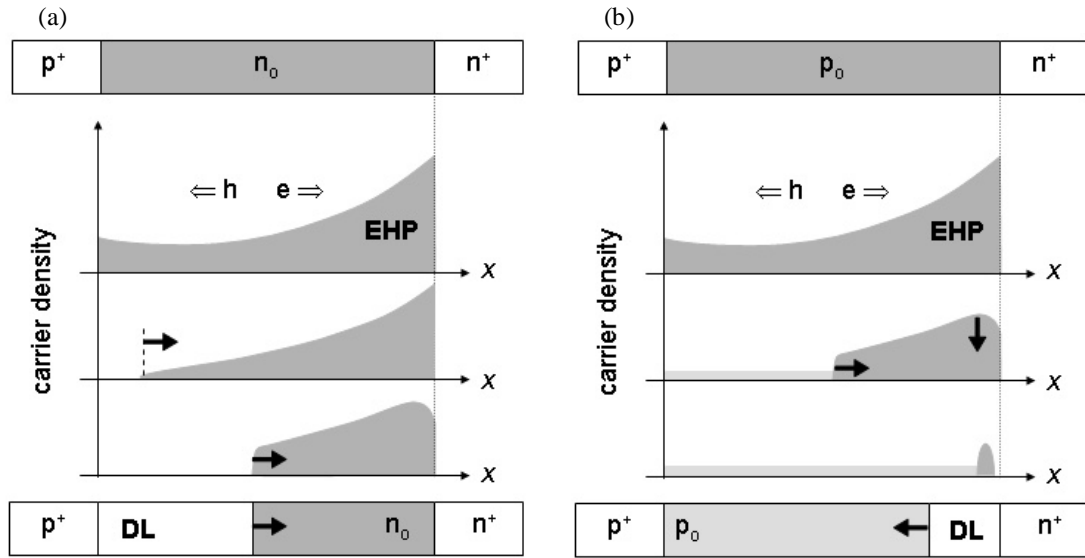


Fig. 3. Qualitative distributions of injected electron-hole plasma (EHP) during the recovery process: (a) -  $p^+n_0n^+$ -diodes, (b) -  $p^+p_0n^+$ -diodes.

So, the recovery properties of  $p^+p_0n^+$ -type diodes are shown to differ from those of  $p^+n_0n^+$ -type ones. In  $p^+n_0n^+$ -type diodes, recombination and diffusion processes predetermine soft recovery behavior in a time of approximately 16 ns. In  $p^+p_0n^+$ -type diodes, purely drift mechanism is responsible, under proper conditions, for the very steep break of reverse current in a time  $\sim 1$  ns. This is due to that the base region of p-type conductivity allows to have  $p_0n^+$ -junction as blocking one. Owing to  $m_h/n_l \gg m_p/n_r$ , fast restoration of DL occurs under a condition when there are no minority carriers in the diode base.

Special electronic pulse generator with inductive energy storing unit was designed and built in which 4H-SiC diode is employed as a fast opening switch for breaking off the reverse current. Optimal regimes of operation of the 4H-SiC diode amounting to the generator were established. With this purpose the influence of the diode blocking voltage, the amplitude and duration of forward pumping pulse and the reverse current on output voltage pulse generation was investigated.

Voltage pulses of 400 V generated with 4H-SiC diode are shown in Fig. 4. As seen, the voltage rise time of about 4 ns. The effect of some reactances on voltage rise time is discussed.

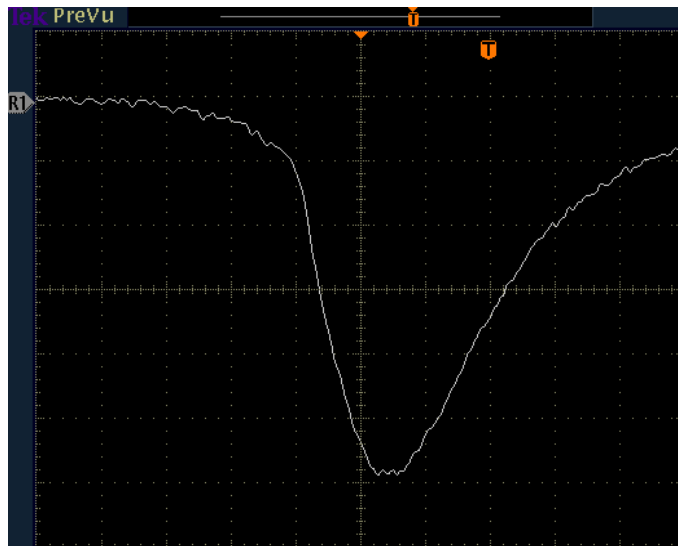


Fig. 4. 400-V voltage pulses generated by the pulse generator with 4H-SiC diode. Vertical scale is 70 V/div, horizontal scale is 4 ns/div. Zero current level is shown by the R1-marker.

## References

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- [6] I.V. Grekhov: Abstracts of the 11<sup>th</sup> Pulsed Power Conference 1997, Baltimore, USA, p. 108
- [7] I. Grekhov and S. Korotkov. Abstracts of the AMEREM'2002, Annapolis MD, USA, p. 58.

### 3. List of publications

- 1. I. V. Grekhov, P. A. Ivanov, A. O. Konstantinov, and T. P. Samsonova. On the Possibility of Creating a Superfast-Recovery Silicon Carbide Diode. - *Techn. Phys. Lett.*, Vol. 28, N7, pp. 544-546 (2002).
- 2. Grekhov I.V., Ivanov P.A., Konstantinov A.O. 4H-SiC inverse recovery diodes (IRD) for sub-nanosecond power opening switches. - Abstracts of the AMEREM'2002, June 02-07, 2002, Annapolis, MD, p. 59.
- 3. Ivanov P.A., Grekhov I.V., Konstantinov A.O., Samsonova T.P. Reverse Current Recovery in 4H-SiC Diodes with n- and p-Base. – To be published in Proc. of the 4rd European Conference on Silicon Carbide and Related Materials – 2002, Lincoping, Sweden, Sept. 2 - 5, 2002 (Trans. Tech. Publ., Switzerland).

### Technology Implementation Plan

1. What marketable results have been achieved or are anticipated?

?	Title of the result possible for utilization	Type of intellectual property	Owner of the results	Intention for utilization	Notes
1	Basic research showing a possibility to create high-voltage pulse power 4H-SiC diodes with improved performance as compared to analogous Si-based devices	Know-how	Ioffe Institute	Creation of the 20-kV pulse generator with voltage rise time ~ 1 ns.	

a) What tasks remain in order to “complete” your Result, meeting the requirements of your target funding sources? How do you propose to meet them and on what timeframe?

i. Describe the current Stage of Development of the project result:

Development stage	Results
Basic Research	At current study of the research, the principal possibility is shown for the 4H-SiC diodes to operate in a DSRD-mode with superfast breaking off the reverse current of high amplitude. Further tasks to be solved for creation high-voltage sub-nanosecond pulse generators are the following: 1) to fabricate diode samples based on the requirements which were worked-out during project implementation, 2) to manufacture pulse generator utilizing the 4H-SiC diodes and test it.

ii. Provide an overview of documentation developed (document type, confidential level, title, number):

1. A scientific paper was published: I. V. Grekhov, P. A. Ivanov, A. O. Konstantinov, and T. P. Samsonova. On the Possibility of Creating a Superfast-Recovery Silicon Carbide Diode. - Techn. Phys. Lett., Vol. 28, N7, pp. 544-546 (2002).

2. Two papers were presented at International conferences: Grekhov I.V., Ivanov P.A., Konstantinov A.O. 4H-SiC inverse recovery diodes (IRD) for sub-nanosecond power opening switches. - Abstracts of the AMEREM'2002, June 02-07, 2002, Annapolis, MD, p. 59; Ivanov P.A., Grekhov I.V., Konstantinov A.O., Samsonova T.P. Reverse Current Recovery in 4H-SiC Diodes with n- and p-Base. – To be published in Proc. of the 4rd European Conference on Silicon Carbide and Related Materials – 2002, Lincoping, Sweden, Sept. 2 - 5, 2002 (Trans. Tech. Publ., Switzerland).

3. Technical documentation on the use of the electronic generator was delivered to J. Gaudet as a contact person at AFL.

b) What is the status of Intellectual Property Rights to your Results?

Type of the rights on IP	Territories, numbers of patent applications and patents	Background or Foreground Rights
Know-how	At present study the Ioffe team retains know-how on the 4H-SiC	



	pulse OS-devices	
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**c) Summarize approximate schedule for activities planned to implement your project results and “graduate” your project team:**

Activity on introduction of results	Attracted partners	Work schedule (starting from...to ...)	Evaluation of estimated expenses
Fabrication of 4H-SiC diodes based on the requirements to be worked-out during project implementation. Manufacturing the 20-kV pulse generator utilizing the 4H-SiC diodes and test it.	IMC (Stockholm, Sweden); AFL (Albuquerque NM, USA); The Three Fox Group (Livermore, USA); "Mega-impulse" Enterprise (with the Ioffe Institute)	Approximately 1 year starting from February 2003 ????	\$35,000

**d) What is your Plan to reach your target industry sector / public-sector organization with your message of sponsorship of your result?**

i. Conferences

At the AMEREM'2002, Annapolis MD, real time device operation was demonstrated for the specialists in pulse power electronics. At the ECSCRM'2002, further plans on growing 4H-SiC epi-structures were discussed with IMC people.

ii. Collaborators

When finishing the work routine on the Project Plan, a special business meeting was organised by J. Gaudet as a representative person with AFL. During discussions J. Gaudet stated that the basic Project Tasks were successfully solved. Both parties came to an agreement that high-voltage sub-nanosecond SiC OS-devices can have marketable properties. So further developments in this field have to be continued

**e) Do you have everything you need at this stage of the project to accomplish your objectives vis a vis your project team's post-project completion sustainability?**

No

**f) What additional services can the ISTC provide that would assist you in reaching your target? For example (note all applicable):**

Assistance identifying target Companies / Organizations.

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### **Private Sector Supplement**

1. What are the possible applications of the technology (product) in the technological process / industry (define)?

The results obtained can be used for manufacturing high-voltage pulse generators operating in sub-nanosecond time interval.

**a) What is the Industry Application Code of the application of your anticipated result (please consult the ISO's Industry Standardization Codes):**

**b) What is the stage in the Technology Process or Cycle to which your anticipated Result relates:**

### **Integrated system**

**c) Please provide brief description of the known technological process (define) and its modifications**

Now Si-based Drift Step Recovery Diode (DSRD) is known as an opening switch to generate short power rise fall pulses in nanosecond range of time. The operation of such diodes is founded on superfast recovery of junction blocking ability after switching the device from forward to reverse bias conditions. The superfast DSRD-mode in a high voltage Si diode is achieved due to the extremely rapid cessation of current which occurs immediately after dissipation of the thin plasma enriched layer that is preliminarily formed near the emitter region by a short pumping current pulse. With the use of Si based JRDs, Ioffe scientists created pulse generators that were able to form 1300 V pulses into a 50 Ohm load, with a voltage rise time of less than 2 ns and a pulse repetition frequency of 100 kHz.

**d) Please describe the possible application(s) of technology (product) in the concrete technological cycle (define):**

Wide bandgap semiconductor material SiC is promising one for constructing superfast DSRDs owing to its unique electronic properties. Of particular importance are its higher electric field strength and higher saturation drift velocity, thus allowing smaller and faster devices. Our estimations show that the parameters of such DSRD devices can be substantially improved in case of SiC devices. As compared to Si we expect: i) to increase the speed of switch operation, the specific commutated power, and the operation frequency repetition; ii) to reduce the weight and size of pulse devices; and iii) to achieve the better reliability of the devices due to the unique thermal conductivity and radiation hardness of SiC.

In DSRD semiconductor structures, maximum voltage rise rate  $(dV/dt)_{\max}$  is limited by the product of the avalanche breakdown field and the saturated drift velocity of electrons:  $(dU/dt)_{\max} = E_{\text{Vsat}}$ . In the case of Si based diodes,  $(dU/dt)_{\max} = 2 \times 10^{12}$  V/s, while  $(dU/dt)_{\max} = 6 \times 10^{13}$  V/s in case of SiC based diodes, i.e. one and half orders of magnitude higher. In particular this means that the voltage rise time in SiC based JRDs can be at least one order of magnitude shorter as compared to Si devices, with the same blocking voltage rating.

**e) Please evaluate technical state of (technological process) in the industrially developed countries and RF. What is the status of technical development of (technological process) in the aforementioned countries (basic, applied research, research & development or industrial introduction.)**

At present, the commercial leader in manufacturing SiC crystals and epilayers is Cree Inc. (USA). At Cree, a wide range of SiC products is commercially offered. With the use of Cree's SiC material practically all classical types of semiconductor devices were created. These devices exhibit SiC's advantages as the wide bandgap material. In particular the following devices have been demonstrated: short wavelength LEDs, UV photo-receivers, power high-voltage switches such as rectifier diodes, different type FETs, BJTs, GTOs, power microwave devices such as MESFETs, IMPATT diodes. In Russia, there is no institutions having industrial equipment for CVD growth of SiC epitaxial films. SiC

research in Russia is supported now by small grants which do not allow for Russian scientists to develop SiC technologies on one's own.

The Ioffe team retains world priority in the field of pulse power semiconductor electronics based on silicon components.

**f) Which of the Companies / enterprises engaging in the (technological process) (ref. point ei above), provide analogous (competing) services products at the same phase in the manufacturing cycle you have identified (point 1b of this supplement):**

To our knowledge, only Ioffe team in Russia deals now with SiC-based pulse power semiconductor devices.

2. What is your "Graduation Strategy" and how is it justifiable?

**a) What is the target market, the size of the market (in units and money), and what market share do you envision capturing with the industrial deployment of your technology?**

Our target market is pulse power semiconductor electronics. Such super-fast electronic devices can find many applications namely for constructing (i) high effective and reliable pulse power supply for lasers and charged-particle accelerations, (ii) super-precise and ultra broad-band air and underground radar-location equipment, (iii) control units for testing broad-band recording and metering circuits, (iv) electronic devices making counteraction for terrorists etc. The market volume for such devices can be estimated as several hundreds millions dollars per year.

**b) How would you characterize your resultant technology:**

Breakthrough (innovative approach / solution to a traditional problem)

**c) How do you envision the commercialization / industry deployment of your anticipated results?**

Distributorship:

Result is production by a business unit (within or outside of) the Institute for manufacturing based upon the technology supported by the sales of product to the Distributor, which resells the product. Distributor usually does not invest in the business unit to establish or upgrade production capabilities.

**d) Which Companies from the above lists would be the most likely candidates for the type of relationship (section c above) appropriate for your Project Team's commercialization of the Technological Result(s):**

"Mega-impulse" Enterprise with Ioffe Institute. This Enterprise is experienced in commercialization of silicon pulse power devices to be developed at the Ioffe Institute.

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**Public Sector Supplement**

**a) What types of Public organizations maintain an interest in the Development of this Technology?**

- R&D-funding organizations for Advancement of Basic / Applied Science

**b) What kinds of Public-sector organizations exist that fund the type of research (technical area) in which you are engaged?**

- Public-funded, non-governmental organizations (such as National Academy of Sciences)

**c) Do you know of other programming / organizations that would be candidates to fund the future development of your research? If yes, which ones?**

CRDF, INTAS, Russian Foundation for Basic Research etc.

**d) Do you know what the eligibility requirements, proposal procedures, and approval timeline / procedures are for this / these organization? If so, what are they?**

Yes

**e) Which Public organizations have you targeted to fund the Research and / or Development of this Technology at your Institute?**

By now, we have not targeted any public organisations.

**f) Do you have everything you need to accomplish your objectives vis a vis your project team's post-project sustainability? Yes / No & explain**

No

**g) What additional services can the ISTC provide that would assist you in reaching your target? For example (note all applicable):**

Assistance identifying target Companies / Organizations.