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TECHNOLOGY SURVEY

Technology Utilization Division

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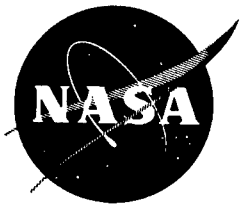
MICROELECTRONICS IN SPACE RESEARCH



NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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MICROELECTRONICS IN SPACE RESEARCH

Prepared under contract for NASA by
RESEARCH TRIANGLE INSTITUTE
Durham, North Carolina

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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Foreword

The Administrator of the National Aeronautics and Space Administration has established a technology utilization program for "the rapid dissemination of information . . . on technological developments . . . which appear to be useful for general industrial application." From a variety of sources, including NASA Research Centers and NASA contractors, space-related technology is collected and screened; and that which has potential industrial use is made generally available. Information from the Nation's space program is thus made available to American industry, including the latest developments in materials, processes, products, techniques, management systems, and analytical and design procedures.

This publication is part of a series intended to provide such technical information. It reviews the status of microelectronics with emphasis on topics of particular importance in space research about which information was available. The Solid State Laboratory of the Research Triangle Institute in Durham, North Carolina, prepared this report.

THE DIRECTOR, *Technology Utilization Division*
National Aeronautics and Space Administration

Preface

The primary purpose of this report is to provide information on the contributions to the microelectronics field which have originated in NASA research programs. Also included is a review of the status of microelectronics in which the limitations of the various technologies are highlighted. Considerable emphasis has been placed on silicon integrated device technology because of its relatively large importance. Microelectronics is defined here as those technologies by which circuit functions are realized in inseparable solid structures which duplicate the behavior of collections of conventional lumped parameter components. This then eliminates from consideration microminiaturization aimed solely at size reduction of components and circuits. Although some of the concepts are original to this report, a preponderance of the material has been obtained from NASA information sources and from the open literature. While it is intended that this report be reasonably comprehensive, the particular research which is described is that for which information was most available. Other equally significant results have probably been generated in other NASA programs.

This report was prepared by the Solid State Laboratory of the Research Triangle Institute, Durham, North Carolina, under Contract NASr-236 with the Office of Technology Utilization and Policy Planning, National Aeronautics and Space Administration, Washington, D.C. The purpose of this contract is to determine, evaluate, and report on NASA's scientific and technological contributions to the field of microelectronics. L. E. Richtmyer, Office of Technology Utilization and Policy Planning, was project director for NASA.

This information was collected and the report written in the period between July 1 and December 31, 1964, by R. M. Burger. Other members of the Solid State Laboratory who contributed directly to the generation of this report are B. M. Berry and L. K. Monteith. The information contained in this report represents the contributions of a large number of people and

organizations and material has been reproduced freely from NASA furnished documents and reports. The open literature has been surveyed for reports on NASA activities and personal contact has been made with the major organizations within NASA who are participating in microelectronics research and development. Of particular help in collecting this information have been the technology utilization officers at the various NASA Research Centers.

CONTENTS

Introduction

The challenge of space research is requiring an expansion of skills in a variety of technologies. The many useful results which emanate from this effort are often obscured by the more glamorous program results and by the usual communication difficulties between working engineers. An additional problem is that of evaluating particular developments. In this report, an attempt is made to gather together activities in microelectronics from the space research effort, to describe the results in terms which may indicate their usefulness to other fields, and to place them in perspective with other developments in microelectronics. While these objectives have not been completely attained, the material herein should be useful and interesting to a variety of people.

Microelectronics is descriptive of those technologies by which electronic circuit functions are fabricated in small solid structures; these can be both reliable and inexpensive. The availability of microelectronic devices allows the electronics engineer to implement many missions which otherwise would not be feasible or which would be done less efficiently. Nowhere will microelectronics have a greater impact than in space research.

It is coincidental that the National Aeronautics and Space Administration was organized in 1958 almost concurrently with the initiation of the strong research and development effort which was to lead to microelectronic devices. The initial impetus for microelectronics came from the military requirements for more reliable systems. Early microelectronics development activities, which were funded primarily by the Air Force, existed in parallel with the early space research programs which necessarily depended upon existing hardware. As space research activities expanded and became more sophisticated, the limitations of existing hardware became more serious. Attention is therefore being focused on the development of new hardware capabilities, particularly in using microelectronics. Almost every NASA center and major contractor is involved in microelectronics efforts; these range from basic material studies to sophisticated applications. All are focused sharply upon the unique requirements of space research, especially that of very long certain life.

Despite the fact that many space requirements are for small numbers of individual parts, the largest user of silicon integrated devices to date has been a space program (the Apollo guidance computer). Under the auspices of NASA some very significant developments of integrated circuits have occurred. It is obvious that NASA is and will continue to be an important customer for microelectronic devices and systems and will set some of the trends in microelectronic device research and development. This should be comparable to the influence of military, telephone system, and computer applications.

There is a strong trend toward introducing microelectronics into space hardware. While integrated silicon devices and thin film devices have already been involved in actual space probes, a large majority of current equipment has been designed with conventional components. Now, however, almost all new equipment is being designed to include microelectronics to some extent. It is obvious that within several years over three-fourths of space electronic systems will contain microelectronic devices and it is only in those particular applications for which microelectronic techniques are not applicable that conventional circuit techniques will be employed.

Microelectronics is classified here into three different technologies: thick film, thin film, and silicon integrated devices. This latter is by far the most important for future applications and is used here as a basis for comparison. A version of thin film technology is being applied by the Bell Telephone Laboratories and IBM is using thick film circuits in a large computer system. For large system applications, decisions made several years in advance determine system design and do not always represent the state-of-the-art for the devices used.

The main purpose of this report is to present the results of completed research. Most of this is in the application of microelectronic devices; therefore, that section of the report is largest. Industries seeking to apply these devices to their own problems will find this applications experience of considerable interest. The second purpose of the report is to review the state-of-the-art of microelectronics in order to put the real and potential accomplishments of NASA in perspective. Since a great deal of literature is already available on microelectronics and its progress, this review only briefly describes the technologies involved and then identifies particular limitations and problems which exist.

This report is divided into five major chapters; the first of these is a review of microelectronics irrespective of NASA studies. The next four chapters describe different categories of NASA activities in microelectronics; technology and techniques for fabricating and evaluating microelectronics devices; actual design and development of devices, i.e., the implementation of specific requirements for space

electronic equipment; reliability which is an important aspect of space research; and applications of microelectronic devices to a variety of equipment. Since telemetry systems are major parts of all space research experiments, a preponderance of the applications reported are concerned with them. It is interesting to note that microelectronic devices are also being used in ground support equipment.

Chapter 1

Review of Microelectronics

In the four years since microelectric devices became available in sample quantities, this technology has progressed rapidly. Today over 180 000 silicon integrated devices are shipped each month and an industrial capacity exists for an order of magnitude increase. Each month the technical literature heralds new devices and techniques. No end appears in sight to the accompanying changes which are revolutionizing traditional concepts of electronics. It is difficult to describe a state-of-the-art for so dynamic a technology.

Microelectronic devices are classified here as thick film, thin film and silicon integrated devices. The first is concerned primarily with circuits prepared by printing patterns of paste or slurry through fine screens onto ceramic substrates and subsequent firing to change their nature, but is broadened to include film prepared by pyrolytic deposition techniques. The second of these is concerned with electronic circuits fabricated primarily by the masked deposition of materials through vacuum evaporation. The silicon integrated device technology is concerned with the realization of electronic circuits in and on single crystal silicon substrates primarily by junction formation. Proponents of film devices may question equating the advent of microelectronics with the introduction of silicon integrated devices; however, silicon technology has provided the stimulus for rapid advance which was lacking in the other techniques and thus justified its use as a reference. There is, in fact, an overriding tendency to compare all other devices to silicon integrated devices.

In the past thin films and silicon structures have been pitted against each other; thick films have also been in the fray. The advent of the new series of IBM computers will maintain for thick films an important place in microelectronics, if for no other reason than the magnitude of IBM's impact on the electronics industry. In most cases, however, reliability and economy of silicon integrated devices make them desirable for the realization of electronic functions. In specialized applications representing extremes of power or frequency other techniques are necessary.

It is very likely that silicon integrated device technology will be married to the film technology. This will be at the subsystem level

but will depend on improved silicon passivation for a practical packaging method. A number of silicon integrated circuits will probably be mounted on a substrate on which film components and interconnection paths will have been formed. Inductors, piezoelectric crystals, and other devices may be compatibly mounted for optimum function realization.

All applications of microelectronics have certain common objectives which must be examined when a choice is made between technologies. For microelectronics, the objectives are given below:

1. Function Realization—While it is obvious that no particular technology will be chosen if it cannot perform the required function, this requirement is sometimes overlooked. For example, a system cannot be fabricated entirely by one technology unless all required functions are realizable by that technology, which is seldom the case.
2. High Reliability—Closely related to cost but overriding it in many space and military applications is reliability. While it is possible that the several technologies will provide structures of equivalent reliability, there is a basic tenet that other things being equal the structure requiring fewer different materials will be more reliable. The silicon structure has advantages in this respect.
3. Low Cost—Many devices are still procured on the basis of cost. This is most important in the nonspace, nonmilitary applications which determine volume production. Devices produced in volume are also most often chosen for the more critical applications in order to take advantage of product stability, production experience, and applications information. The batch production processes of the silicon integrated device technology and availability of standard components have an advantage but highly mechanized volume production of devices by other technologies may become competitive.

These three objectives (low cost, high reliability, function realization) are not exclusive but, in most cases, override all others.

The scope of present applications of microelectronics is not large when compared to their potential. This results primarily from the necessary lead time required to put any new technique such as microelectronics into widespread use. For microelectronic devices in particular, this has been difficult since it has been necessary to discard many of the traditional concepts of system design and to develop new ones. In other cases the necessary device types to warrant a system redesign have not been available and even when they are available, the advantages to be gained from a system redesign do not often

overcome the cost. Thus applications, while appearing to move slowly when examined on the basis of available useful equipment and considering the enthusiasm of most engineers engaged in the microelectronics field, are nevertheless advancing at a rapid pace when the limiting factors are considered. The actual pace can be expected to increase rapidly in the near future particularly in space programs.

In the following sections, each of the separate technologies will be discussed in terms of the necessary processes and the resulting structures and their capabilities; a concluding section compares the three technologies.

THICK FILMS

Thick film structures are prepared by screening and firing or by pyrolytic deposition. They generally contain only conductors, resistors and capacitors. Other components must be added as discrete entities. The substrate is usually a ceramic wafer.

ADVANTAGES AND LIMITATIONS

This technology is not new, but has been in existence for a number of years. In fact, at least one company has been making such units for over twenty years and is now producing over 45 million units/year at costs ranging from under ten cents to three dollars. As with all technologies, however, there are limitations. Most important of these is the inability to provide active components except by individual insertion with attendant high cost and extra connections. There are also the usual limitations upon the value, tolerance and stability of the resistors and capacitors. Attempts have been made to circumvent some of these problems by the development of new materials and new deposition techniques. In pyrolytic deposition, for example, chemical compounds containing the desired materials are thermally decomposed at the substrate over the entire surface; the pattern is then etched or machined into the surface layer.

A big advantage of the thick film technique is its high volume use and relatively low cost. It is also a flexible technique in which a variety of patterns can be achieved with little variation in the process. As long as resistance ratios on the pattern are no more than 5 and capacitors are less than 0.05 μf, thick film circuits can be made very rapidly and even higher resistance ratios (up to 100) can be processed routinely.

The primary limitations on the use of thick film circuits are ones of size and reliability. It can be argued for example that conventional discrete components can be assembled into circuits which are of comparable or less total volume and weight than thick film circuits. At the same time even though the thick film circuits are formed at high

temperatures and are thus relatively stable, it is also true that conventional circuit techniques are quite reliable. Thus the question is raised as to why one should go to thick film circuits if there are not significant improvements in reliability or in volume and weight or in power consumption. The best argument for thick film circuits (and thin film circuits) is the ability to form a number of connections in the process thereby eliminating the troublesome one-at-a-time welded or soldered connections. On the basis of cost vs. incremental improvement in performance, thick films do not have much to offer and to a large extent have been passed over in microelectronic considerations. On the other hand, due to the large commercial utilization of such circuits which includes the recent use by IBM of these techniques in a very large computer program involving ultimately millions of circuits, it is likely that thick films are here to stay, not only in the commercial field but also in space and military systems. For this reason they must be considered as a serious competitor of other microelectronic techniques.

An even more significant possibility is that integrated silicon devices may be placed onto ceramic wafers with thick film components (or possibly thin film ones) which cannot be economically fabricated in the silicon and that such a technique will provide a complete system capability. If, for example, silicon integrated devices and certain high value resistors and coupling capacitors can be placed onto a suitable ceramic substrate as a basic system building block, it is possible to envision a very practical and powerful technology for achieving large electronic systems with a high degree of reliability and with attendant low cost.

SCREEN CIRCUIT PROCESSES

Despite the very large number of screen circuits which have been available on the market for a considerable period of time the exact processes by which these circuits are made are not generally known. This is because the vast majority of the circuits have been used on the consumer or industrial equipment market and their development has not been supported by government funding. As a result, many techniques have been considered proprietary. Nevertheless, the basic processes for making screen circuits are known and only the details of the formulation and the process parameters cannot be given.

Screen circuits ordinarily consist of conductor and resistive layouts in relatively simple patterns. Conductor crossovers are avoided and few capacitors are used. The majority of formulations for conductors are available from chemical companies, particularly Du Pont, and consist primarily of gold, platinum, palladium, silver, or mixtures of these, depending upon the particular requirement. These conductive formulations are fired at temperatures between 600 and 1100° C.

Resistive formulations consist of palladium, silver, carbon, glass frit and other additives designed to achieve specific properties. A new development tailored for high resistance applications includes thallium oxide and glass frit. These resistive formulations can be bought from a number of commercial suppliers. Little information is available on formulations for dielectric coatings, although it is thought that most such coatings consist of glass with additives such as barium titanate to increase the dielectric constant.

With suitable formulations for the screen circuit process, the procedure is as follows. A series of screens is fabricated, with geometries to fulfill the circuit design, for impressing the pastes or slurries upon the ceramic substrate. These screens can be made of silk or stainless steel, the latter being more durable. The mesh size of the screen varies with the application, but generally falls in the range of 150 to 200 mesh. Finer screen sizes result in incomplete circuit patterns since the paste may not extrude through to the ceramic surface. Coarser screens may cause voids in the pattern and have lower resolution. The application of the pastes and slurries is the same as that used by artists in the silk screen process for many years. After application, the pattern on the wafer is air dried, vacuum dried, or gently heated in order to drive out part of the binder. When several different pastes are to be fired, the additional patterns may be put onto the wafer before firing any of them. More often each deposit is fired separately so that the entire process is repeated for each type of paste. The firings usually are in order of decreasing temperature. Both static kiln furnaces and conveyor furnaces are employed, the latter being used in production processing where the wafers are placed on a continuous belt and passed through a suitable temperature profile. Total firing time typically is about 1 hour although the firing temperatures and times vary with the materials employed. Since the films obtained are relatively thick, on the order of one micron, the matching of thermal coefficients of expansion is important. If they are not accurately matched, the deposited film will crack or craze upon removal from the furnace particularly for glass dielectric formulations. Other components such as large capacitors, diodes, and transistors can be directly soldered to the first conductors. The completed screen circuit wafer can be tested and used with pressure type connectors, although soldered connections are more reliable.

A variety of substrates is available, but a high quality alumina is most desirable. In some cases the alumina substrates are overcoated with glass to give a smooth surface and desirable expansion coefficient to the substrate for particular processing requirements.

Many kinds of circuits made by screening are available. One supplier advertises linear and digital circuits, RC networks, audio filters,

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notch filters and other components in almost any standard value and tolerance. In order to achieve this versatility, the components except for the small capacitors and resistors are inserted and in some cases bonded to the ceramic substrate. The form of the substrate varies among manufacturers. In one case the alumina has lead wires directly bonded to it and is packaged in a suitable epoxy. In another case a supplier uses very small circular wafers and assembles them in a TO–5 transistor type can. In other cases the screen circuit is protected only by a film or left uncoated.

PYROLYTIC TECHNIQUES

As noted previously, other methods for depositing thick films exist, the most important of which is the vapor or pyrolytic deposition process. Suitable chemicals are decomposed at the substrate surface and unwanted material is removed in a subsequent step by etching or sandblasting. Vapor sources include metal-organic compounds and metal halides. One of the more common processes uses tin chloride in solution with a catalytic agent. This is sprayed onto a glass covered alumina substrate and decomposes to give a thin oxide coating which is then patterned into film resistors. In this case, conductor patterns can be formed on top of the tin oxide by electroless plating of copper and dielectric patterns made by decomposition of ethylorthosilicate or by glass frit formulations. Components and circuits obtained by these and similar processes are commercially available and comparable to screen circuits. The relative advantages of these two thick film circuit technologies are determined largely by their reliability and cost (in some cases, the performance capabilities may be different). No clear choice now exists.

THIN FILMS

Historically, the development of the thin film technology for the fabrication of electronic circuits somewhat parallels semiconductor technology for it was not until transistors became available that the potential rewards associated with the development of thin film techniques became apparent. The applications which appeared possible for thin films involved the resistors, capacitors and interconnections of electronic circuits. Before the advent of the transistor these portions of the electronic circuits were relatively small, reliable, and inexpensive. The change in this situation caused a large increase in the attention given to thin film techniques.

Much research was performed on ferromagnetic thin films and during the past decade thin film magnetic memories have become available and are being used in computer systems. This however, is a peripheral subject with respect to the present discussion. In this

report thin films are considered only for the fabrication of electronic circuits such as are used in the logic portions of a computer, signal handling circuits and all of the other diverse circuits which include both active and passive components. For these, thin films have been slow to mature, although they are included now in operating equipment. At least three dozen electronic companies have some capability for supplying thin film circuits. These companies range from several small ones specializing in and supplying only thin film circuits, through the larger diversified component and device suppliers, to the large corporations supplying electronic systems.

It is interesting to note that thin film circuit research has encouraged corresponding rapid developments in the vacuum art. Equipment available for vacuum deposition of thin films has progressed from crude bell jars operating at 10^{-6} torr with homemade mask holders to extremely versatile automatic vacuum systems containing extremely complex mask changing apparatus, capable of multiple depositions without breaking the vacuum, and operating to 10^{-10} torr. The commercial availability of such equipment is one very good reason for the existence of the multitude of organizations possessing the equipment and the implied capability for fabricating successful circuits.

ADVANTAGES AND LIMITATIONS

Despite this large developmental effort and equipment investment the application of thin film circuits has been slow. Some of the reasons for this are:

1. Well made thin film circuits with their inserted active components representing the state-of-the-art are smaller than can be achieved by fabrication of circuits with available miniature discrete components.
2. The reliability of thin film composite circuits does not necessarily exceed that of conventional component circuits. There are apparently some unique failure modes associated with thin film circuits on which additional research must be done.
3. To date thin film circuits are, if anything, more expensive than conventional component circuits. These costs are, of course, related to the volume of production but there are some inherent expenses which seem difficult to avoid.
4. It has been stated many times that the key to a rapid expansion of the use of thin film circuits is a thin film active device. Experimental examples of such devices are just appearing from the laboratories, but there are apparently many improvements to be made before these can become competitive.
5. The electronic industry is characterized by a large inertia, i.e., there is a long time between the development of a new technology

and its wide use. It is only now that the industry is adapting itself across the board to the use of transistors. Microelectronics circuits, which are available, are starting to be phased into equipment. This will be a slow process and most effort will be given to that particular technology which offers the most right now in the important criteria of reliability and cost, viz, not thin films, but silicon integrated devices.

What then is the role for thin films in the advancing electronic art? The momentum of the research and development efforts relating to thin films is such that very definite roles for them will be defined, and that they will be widely used. Some of the advantages of thin films are:

1. Thin film circuits do not exhibit spurious interactions any more than do conventional component circuits. For this reason, a one to one extrapolation can be made from conventional components to thin films; the sometimes troublesome interactions characteristic of silicon integrated devices are not present. This results in a bias towards thin film techniques by engineers who are familiar with conventional circuit design and also offers a high frequency circuit capability which has not yet been demonstrated by the silicon technology.
2. Silicon circuits are inherently small and have limited power handling capabilities. When the size increases in order to accommodate higher power, the cost goes up rapidly. In this higher power end of the circuit spectrum, thin films for use as passive components and for interconnections are very practical. High resistance, high power resistors, for example can be made with thin films but not as part of a silicon integrated device.
3. Thin film circuits are believed to be considerably more radiation resistant than are semiconductor integrated circuits. This apparent ability to operate in a radiation environment for longer periods of time than silicon integrated circuits has been a prime justification in thin film circuit development. Despite some doubts as to the accuracy of this reasoning, the requirement for radiation resistant electronics is such as to demand further investigation.
4. Thin film circuits can consist of a multitude of materials, each chosen to be optimum for its particular application. This allows a more complete assortment of component parameter values and circuit types than is possible with silicon. Counter to this, however, is a belief that the addition of new materials to a given electronic structure may introduce new failure modes and may detract from the reliability.

5. Thin films can be deposited upon a silicon substrate and used to improve the capabilities of silicon integrated devices. This adds additional processing steps to the fabrication, increases cost, and perhaps decreases reliability. The hybrid integrated circuit, however, is currently obtaining increasing popularity because of its capability for obtaining certain extreme parameter values impossible in silicon alone.
6. Another hybrid technology involves the deposition on a substrate of thin films for passive components and interconnections, after which silicon integrated circuits are inserted. A favorite method for accomplishing this is to provide ball type electrical connections to the silicon integrated structure, facing it down on a thin film substrate and bonding it by soldering or other appropriate techniques. This approach, in which the best attributes of both the silicon and thin film technology can apparently be used, possesses a large potential.

Each of the points made above for thin films could, perhaps, be made for thick film structures; it is difficult to tell which is better able in a particular case to provide the best answer. Thick film structures might be expected to be more reliable due to the high temperature processes employed in their fabrication but techniques have been developed for many more materials with thin films than with thick films. Also for thick films there is apparently no foreseeable chance to obtain an active device structure; this is not the case with thin films. If size is important, thin films are at present made by techniques which allow higher resolution in the structures.

Most of the comments made above apply to all thin films. However, in the subsequent discussion of the capabilities and fabrication processes it is necessary to separate the two more important of these techniques, i.e., vacuum deposition and the sputtering of tantalum films.

FABRICATION OF VACUUM DEPOSITED THIN FILM CIRCUITS

The equipment for fabricating thin film circuits consists basically of a vacuum system, masks, evaporation sources, and substrate heaters. The complexity of this equipment may vary a great deal ranging from an "oil" pumped, 18-inch bell jar system with mask changers and evaporation sources to a complex in-line system of multiple vacuum chambers which allow substrate transfer from one processing chamber to the next without breaking the vacuum.

Regardless of complexity, the actual processes are basically the same. Given a circuit design, suitable masks are made which define the areas of deposition for the various materials. Translating a circuit into

mask form is not difficult. Objectives in mask design are avoidance of crossovers, minimization of interconnection lengths, minimum area for the desired parameter tolerances, graded power dissipation and a realizable mask geometry. A typical circuit may require four masks: the first for the resistor pattern, the second for bottom capacitor plate, the third for dielectric coating and the final one for top capacitor plates and interconnections. With some processes an additional pattern is needed in order to provide suitable materials for soldering external leads to the circuit. Masks are normally formed by photoetching openings in thin copper-nickel alloy sheets.

The masks are mounted in a changer; while a variety of designs are available, a typical one has a rotary plate on which the masks are mounted and is stepped sequentially in front of the substrate. Positioning is often achieved by aligning suitable holes in the masks with locater pins. Alternative systems involve movement and location of the substrate rather than the mask. The exact mechanism is unimportant, as long as the alignment is close enough for the desired resolution in the deposited pattern. Tolerances of several thousandths of an inch between successive masks are possible.

Source heaters are provided for heating the appropriate materials to evaporation temperatures. There are a variety of designs for sources. Aluminum, a very common material in thin film circuits, is most often evaporated from a stranded tungsten coil filament which is directly heated by passage of current. Silicon monoxide, the most common evaporated dielectric, requires the use of carefully designed evaporation sources which prevent line of sight evaporation from the solid silicon monoxide to the substrate. This is to avoid the ejection of particles from the source to the substrate which causes defects in the films. These sources are normally fabricated from sheets of refractory metal and are heated by passage of large currents. Nickel-chrome alloys, such as Nichrome or Chromel, which are employed for resistors can be evaporated from coiled tungsten wire or by direct passage of current through the alloy wire. A variety of other materials is also employed, each requiring some attention to the design of the evaporation source. Information on sources is available both in the scientific literature and from the suppliers of evaporation sources.

Both alumina and glass substrates are employed for thin films. These substrates are mounted in the vacuum in a suitable holder. It is usually necessary to heat the substrate at various stages of the deposition process, both for cleaning the substrate and for good adhesion of the deposited material. This is accomplished by a suitable resistance heater mounted behind the substrate. Normally the evaporation

sources are mounted at the bottom of the vacuum system, with the substrate at the top. In some of the more advanced systems very high vacuums are possible down to the 10^{-10} torr range and the evaporation sources may be heated by electron beam bombardment.

Normally all depositions are made without breaking the vacuum. This has been found necessary in order to avoid defects in the films brought about by contamination in the air. Dust is a particularly nasty problem. In some cases the adherence of the successive depositions will be poor if there has been exposure to the atmosphere.

With the apparatus described, the deposition of the thin film circuits is a relatively straightforward process. In general, substrates are placed in the holders, the vacuum is obtained, the substrates are heated for cleaning, and the materials evaporated through their respective masks in sequence. The substrates are then removed from the vacuum chamber, tested, resistors adjusted if necessary, active components inserted, lead wires attached, and the circuit encapsulated. Particular processes, of course, differ in detail due to the variety of materials which can be handled in a vacuum evaporation scheme. While Nichrome is popular for thin film resistors, rhenium, titanium, nickel, and other resistive materials have also been vacuum deposited. For dielectric coatings silicon monoxide [1] has bee nused most often but other dielectrics such as magnesium fluoride have also been employed. The silicon monoxide is sometimes oxidized to silicon dioxide during evaporation in order to improve its dielectric properties. Just as with tantalum, as described in the next section, titanium can be anodized to form a dielectric suitable for capacitors. Conductors used include aluminum, silver, copper, and other good metallic conductors.

The parameters of the components which can be obtained by vacuum deposition processes are quoted at various limits by the device suppliers. A typical range of resistance may be quoted at 10 ohms to 1 MΩ by a supplier after which a recommendation is made that resistance values be kept between 500 ohms and 20 kΩ. Vacuum deposited capacitors may be as large as 0.01 μf on a practical size substrate, but some manufacturers even in this range prefer to use attached chip-capacitors with a barium titanate dielectric. The tolerance on these components is a function of their size, typical values being ± 20 percent for untrimmed resistors and ± 10 percent for capacitors. Long term stability of the resistors is quoted as 0.1 percent for resistors and 1 percent for capacitors. The temperature coefficient observed for the materials and processes normally used ranges from ± 50 to ± 1000

[1] The term silicon monoxide is used although the oxide may well not be a stoichiometric compound and the Si : O ratio may vary throughout the layer. The same is true for silicon dioxide.

ppM/°C for resistors up to ±1000 ppM/°C for capacitors. The complexity of the actual circuit and the tolerances which are possible with a particular system determine the substrate size. Single logic stages or amplifiers may be obtained on substrates approximately 0.3 inch square while multiple circuit configurations with over 30 circuits on a substrate have been formed on larger substrates. Normal power ratings for thin film circuits are on the order of a few watts per square inch of the substrate. Resistor and interconnection lines can be as small as 3 mils wide, but a width of 10 mils is more common and gives better results.

The lead wires of inserted active devices may be attached to the thin film substrate by a variety of bonding techniques. Soldering is most common but thermal compression bonding, ultrasonic bonding and welding are also employed. A recent innovation is bonding the active device chip directly to the thin film by small solderable copper ball connections. A variety of encapsulations have been employed for thin films including various epoxies, varnishes, and an overcoating of silicon monoxide. More recently small devices have been supplied in hermetically sealed packages due to problems identified with the other encapsulants.

TANTALUM THIN FILM TECHNIQUES

Since 1959, tantalum thin film circuit technology has been the subject of increasing interest. The advantages of using a tantalum film are high annealing temperature, film stability, anodic adjustability of resistors, and high dielectric strength and dielectric constant of its oxide for capacitor use. Unfortunately, it is not possible to fabricate transistors or diodes on tantalum patterns. However, these devices can usually be mounted directly onto the substrate.

The high melting point of tantalum requires deposition by cathodic sputtering rather than by vacuum evaporation (electron beam heating can be used, but is usually less desirable). The sputtered films adhere better than evaporated films and are more uniform. Sputtering is more economical of material because the deposit is localized but the deposition is difficult to monitor and to mask for geometry control.

Sputtering is a vapor deposition process in which an electrical discharge is set up between two plates in the presence of a low pressure inert gas such as argon. The ionized gas atoms are accelerated by the high electric field to the tantalum cathode and release their kinetic energy, knocking off tantalum atoms (a few of which may become ionized) which are then free to diffuse to the glass substrate on the anode.

In the sputtering process, the vapor deposition chamber is used only to produce thin films. The resistor and capacitor geometry patterns

and circuit layout are done externally by high-resolution photoengraving techniques, which permits the fabrication of high density microcircuits.

For tantalum thin film resistors, a uniform and stable film with a predetermined sheet resistivity must be obtained on the glass or ceramic substrate. Nonuniformity in the resistance of sputtered tantalum films is due to the presence during deposition of temperature gradients and of electric charge on the substrate.

Resistance adjustment and stabilization are obtained by anodic oxidation of the tantalum at temperatures over 350° C. Resistance values are monitored externally during trimming. Adjusted values to within ±3 percent are typical, but values can be trimmed to better than ±0.02 percent where extreme precision is required.

Stabilization of the resistor is obtained by gold doping and oxide formation. A layer of gold with a thickness of about 7 percent of the tantalum is diffused into the tantalum film at a temperature of around 400° C for about 30 minutes. The film obtained has the same resistivity as the original undoped film, but is much more stable and has a temperature coefficient close to zero. A heat treatment for 25 hours at 250° C forms a protective oxide coating thicker than any that could grow during the resistor's lifetime. This oxide cover provides effective protection from the atmosphere and makes further encapsulation unnecessary unless additional mechanical protection is required. Finally, conductive material is deposited over the film and circuit patterns are produced employing standard photoengraving techniques. Conducting lands are usually obtained by depositing gold. A titanium layer between the gold and tantalum creates a more reliable high-strength bond.

Typical resistor characteristics obtained on a 0.31 inch square glass substrate are shown in table I.

TABLE I.—*Typical Resistor Characteristics*

Working sheet resistivity	50–600 ohm/square
Range	10 to 1.5 Megohm
Tolerance	<0.02 to 10 percent
Temperature coefficient	−250 to +50 ppM/°C
Power dissipation	>4.6 watt/cm² of substrate
Noise	0.01 μV (rms)/volt across resistor

In special cases, tantalum thin film resistors can be fabricated to dissipate enough power to thermally-fracture the glass substrates without otherwise failing.

Introducing reactive gases such as nitrogen, oxygen and hydrocarbons into the argon sputtering atmosphere changes the electrical properties and structure of the resulting tantalum film. The intro-

duction of nitrogen to the sputtering chamber affects the specific resistivity of the sputtered film. Between 10^{-6} torr and 4×10^{-5} torr, a 5-fold increase in specific resistivity is noted with a limiting value of 250μ ohm-cm being attained at background pressures greater than 5×10^{-5} torr for 1000 A=0.1 micron films. The temperature coefficient of resistance (TCR) is affected similarly starting at a high value for relatively pure tantalum and decreasing to a negative value of 60 ppM/°C at a nitrogen background pressure of 3×10^{-5} torr. Thus, the consistent fabrication of precision resistors with reproducible parameters is possible by using nitrogen at various background pressures in the sputtering process. However, the exact dependence of the TCR and specific resistivity varies from system to system and extreme care must be taken during the fabrication process. It is necessary to start with a specific resistivity in the film of less than 75μ ohm-cm to attain reproducible electrical properties for the resulting tantalum nitride films.

The precision of thin film capacitors is a function of the uniformity and reproducibility of the thickness of the oxide dielectric and the electrode area. A means to attain the high precision required for microcircuit capacitors is the anodic oxidation of tantalum films. An electrochemical cell consisting of a tantalum anode and a platinum cathode in a heated electrolyte is used to form the oxide dielectric. A potential of 100–150 volts dc applied to the cell for a specified time converts the tantalum metal to a very uniform pentoxide (Ta_2O_5). The oxide thickness is directly proportional to the applied voltage at room temperature and forming constants of 25 A/V are typical. The capacitor characteristics are, therefore, predictable.

A method for improving capacitor yields has been suggested. After the tantalum has been anodized, a layer of aluminum is evaporated over it. This aluminum layer is then removed by etching, with care taken to ensure that the etch does not undercut the glass substrate or destroy the mask. The film is then reanodized to the previous final voltage, and counterelectrodes of aluminum are evaporated to form a capacitor. The area of the counterelectrode determines the final capacitance values. For a specified anodizing potential, capacitance values from 30 to 30 000 pf can be obtained by varying the counterelectrode size. This process is believed to fill in film defects with aluminum oxide.

Table II lists some typical characteristics for capacitors fabricated on 0.2 inch diameter glass substrates.

The range of breakdown voltage is satisfactory for logic circuits operation in which voltages of 10 V or less are applied.

TABLE II.—*Typical Capacitor Parameters*

Capacitance	1.0 μf/in.^{2}
Temperature coefficient	250 ppM/°C
Dissipation factor at 1 kc	<0.01
Breakdown voltage	>25 V

The rapid increase in the dissipation factor with increasing frequency for tantalum thin film capacitors limits their use in high frequency logic circuits. Improvements to extend this frequency limitation are the use of a relatively thick layer of tantalum and the application of a conductive metal underlay, such as aluminum, under the tantalum. Capacitors having a Q of 50 at 5 Mc have been fabricated by underlaying the tantalum film with aluminum and by using thick counterelectrodes of copper.

It has often been stated that one advantage of tantalum thin-film circuitry is the fact that the same metal is used to fabricate the resistors and capacitors, yielding unified technology. However, this advantage is lost, somewhat, by the improved fabrication methods that have come about in tantalum technology. The methods of gold or nitrogen doping and protective anodization employed for resistors are not particularly compatible with thick low-resistivity layers of tantalum or aluminum underlayers used for capacitors. However, tantalum thin-film resistors and capacitors have performed well and both merit further development for future microelectronic circuit use.

SILICON INTEGRATED DEVICES

The development of silicon integrated devices, to electronics, ranks with the inventions of the electronic vacuum-tube and the transistor. Regardless of future trends in microelectronics, silicon integrated devices will play a major role. Less than 5 years after the initial research, thousands of such devices can be found in operating systems and the entire electronic industry is experiencing a reorganization to adjust to the resulting changes. Research on silicon integrated devices started in 1959 and today over twenty companies (the actual number varies from week to week) are offering more than 300 different devices for sale.

ADVANTAGES AND LIMITATIONS

Even the most conservative critic will now concede that in systems requiring digital elements, silicon integrated devices are competitive with conventional circuits and thus should be given first consideration in any new equipment design. For linear or analog circuits, an opti-

mistic statement is that in the near future it will be possible to design and fabricate any function which can now be performed with transistors and which does not require inductance or large values of capacitance. Even for circuits traditionally requiring these functions, in many cases it will be possible to obtain designs in integrated form which circumvent that need. With advancing technology, three trends in silicon integrated devices are evident. The first of these is due to the evolving technology for fabricating a multitude of circuits on a silicon chip rather than one or two as is now the case. The second trend results from using other materials to enhance the silicon integrated circuit. The prime example of this is the development of optoelectronic techniques utilizing gallium arsenide diodes as photon sources. The third trend is toward the functional device wherein the operating solid structure performs electronic functions needed in a system but cannot be broken down into equivalent conventional components. The order given for these three trends is that in which practical results can be expected.

It is useful to examine the reliability, cost, size and power requirements of silicon integrated devices. With respect to reliability no basic limitations have yet been found. As with any new device many early design and production methods turn out to be inadequate. With these eliminated or corrected, however, the life of silicon integrated devices is very long. Systems can be designed so that properly screened devices seem not to fail at all. The silicon integrated 3-input NOR gate being used for the Apollo guidance computer has a failure rate of less than 0.005 percent/1000 hr$=5/10^8$ hr (at 90 percent confidence level) estimated from actual operating use.

The costs of silicon integrated devices cover a wide range. For new devices with significantly enhanced capabilities and available in sample quantities only, the price per unit may be hundreds of dollars, but for high production devices with no demanding specifications, prices are below $3 each in quantity. For high-quality production devices, typical prices range from $20 to $50. This is just an indication that the predicted cost competitiveness of silicon integrated devices is being realized. Most common logic functions can be obtained less expensively in silicon integrated devices than using conventional components. It can be expected that the trend will be toward lower prices for all silicon integrated devices for which a volume market is found.

In discussing microelectronic devices, their size and weight are often compared to those of conventional circuits performing the same function. Integrated silicon devices do offer a very significant reduction in size and weight; in fact, so much so that the emphasis on their size and weight has to a large extent been forgotten. In most commercial,

industrial, and military applications, the size and weight of the system is no longer significantly affected by further size reduction of integrated devices; the input, output and interconnections of these systems are the limiting factors. In space research where size and weight are still extremely important, integrated circuits are being used to good advantage. Equally important, if not more so than size and weight, is the low power requirement of the integrated device. More significant reductions can be obtained in the overall size and weight of a space research experiment by reducing the power requirements of the electronics than by shrinking the device structures.

Power dissipation of silicon integrated devices is between one and several hundred milliwatts per device, dependent upon the function of the device and its design. Both ends of this power spectrum are being pushed by further research and development. For space research and other applications in which power is at a premium, devices which operate at microwatt power levels are needed. The high power end of the spectrum is being pushed because it is necessary to obtain enough power from silicon integrated devices to perform some useful function. The upper limit is set by the ability of the package to remove heat from the integrated device. There is a high power level at which the utility of integrated devices will be less than that of conventional component circuits. Thin film circuits have the ability to operate at higher temperatures and thus have more efficient heat transfer so more power can be handled.

Some of the attributes of silicon integrated devices are listed below. They apply primarily to the monolithic device rather than to the multichip structure which is sometimes also classified as an integrated silicon device.

1. Batch Processing—One important attribute of silicon integrated devices is that up to 400 devices are processed as a unit up to the stage where leads are attached and they are encapsulated. This allows a high degree of process control and device uniformity with relatively low unit cost.
2. Processing Simplicity—The number of processes which are involved in the fabrication of a silicon integrated device is very small when compared to the total number of separate processes required to fabricate the components of the conventional equivalent circuit.
3. Device Diversity—The identical processes can fabricate a variety of integrated devices by variation of the necessary photographic patterns.
4. Materials—In the silicon integrated device a small number of different materials are employed. For example, one class of

devices employs silicon, silicon oxide, aluminum and gold; no other materials are necessary. In other types of integrated devices, additional materials may be employed. They may be other conductors or contacting materials or a resistive metal employed for thin film resistors. Even with these, the number of different materials involved in the integrated device is small. This tends to promote high reliability.

5. Area Factor—The surface area of the single crystal silicon die on which the integrated device is fabricated is very important. It influences yield and thus cost, allowable power dissipation, required power to operate, package size, and functional capability. For a given structure the present lower limit on area may be set by dissipation, current carrying ability, capacitor and resistor parameters, or by resolution limits of the photoengraving process. For low power circuits the latter is most important since for a fixed resolution, the only tradeoffs are between component tolerances and circuit size.
6. Inverted Economics—Because of the greater area required for capacitors and resistors on silicon integrated devices, these components add more cost to the integrated devices than do transistors or diodes. This is the reverse of the situation for circuits designed with vacuum tubes and separate transistors. The inversion of relative cost of the active and passive circuit components will continue to have significant impact upon the design of integrated circuits.

SILICON INTEGRATED DEVICE TECHNOLOGY

The processing technology by which silicon integrated devices are realized varies little from one manufacturer to another. The details are different, however, and these details can be extremely important. In general a new fabrication facility will have a shakedown period before successful devices are produced. This period is spent adjusting processing methods and testing alternative methods to find a successful combination. The only criterion for success is the consistent production of good units. The major steps involved are:

1. substrate preparation
2. photoengraving
3. diffusion
4. oxidation
5. epitaxy
6. chemical processing
7. interconnection, lead attachment, and encapsulation.

Substrate Preparation

The substrate on which silicon integrated devices are formed is a wafer of single crystal silicon which may be between 0.7 and 1.5 inches in diameter. This circular wafer is cut from a single crystal

which is grown either by pulling the crystal from a melt or by the float-zone method. The former is characterized by a lower dislocation density while the latter is more free from dissolved impurities, primarily oxygen. In the usual fabrication facility, silicon wafers are obtained to a specification from a separate group which may or may not be part of the same company. Silicon wafers are difficult to specify because inadequate knowledge is available on what is really needed. Six of the properties which may be specified are

Base material type and impurity.—This is a gross specification indicating whether n- or p-type material is required. The particular impurities which are employed to dope the silicon have normally been boron or phosphorous, but other impurity dopants are available and are employed in particular applications. Although not normally specified, it is desirable that the silicon have a high resistivity before doping in order to minimize compensation effects.

Orientation.—Crystals sliced from a grown ingot normally have a specified crystalline orientation which may be confirmed by X-ray diffraction. The orientation is important for the dicing operation and for wafers on which epitaxial layers will be grown. Wafers with a <100> orientation have cleavage planes at a 90° angle; so when the wafers are scribed with a diamond tool and broken a high yield is obtained. In a <110> orientation the cleavage planes are at 60° angles and the yield is lower. The normal orientation tolerance is 1.5°.

Resistivity.—The resistivity may or may not be an important parameter, depending upon the particular design approach used for the integrated circuit. For epitaxial devices the substrate silicon material is a passive supporting structure, and its resistivity is relatively unimportant. However, if parts of the substrate are used in active structures of the integrated device, the resistivity is very important. The resistivity tolerance is affected not only by the accuracy of the doping and crystal growing procedures but also by the variation of resistivity along a diameter of a circular wafer, which results from temperature gradients existing in the growing process. Wafers with a 20 percent tolerance on the average resistivity can be obtained and a 10 percent tolerance on the variation of resistivity on a single wafer is realizable.

Etch pit count.—When a silicon wafer is etched, in a so-called preferential solution, pits are formed at the sites of crystalline dislocations. The density of these is employed as a measure of the crystal perfection and is sometimes specified. Float-zone crystals are characterized by a large dislocation density (up to 50 000/cm^2) while some

suppliers of pulled crystals claim a zero etch pit count. A specification on pulled crystals of less than 1000 etch pit counts/cm^2 is readily obtainable. The dislocation density is important in its relation to device yield, particularly for epitaxial structures wherein the crystalline imperfections are propagated throughout the epitaxial layer.

Surface finish.—Silicon wafers may be purchased either as-cut from the ingot or with subsequent surface preparation steps already performed. The diamond slicing operation is followed by mechanical lapping and polishing. The final surface employed for the first wafer processing step may be either a mechanically polished surface with a mirror-like finish or a chemically polished surface. When a mechanically polished surface is used, it is assumed that in subsequent processing, the mechanical damage is removed either by oxidation or by gas etching in the epitaxial furnace. The chemically polished surface is not optically flat but is characterized by the so-called lemon peel undulation; this is sufficiently small so as not to interfere with the photoengraving process.

Dimensions.—Specification of dimensions is obvious. If the wafers are obtained with as-cut surfaces, then the thickness should be approximately twice that needed in the device processing in order to allow for polishing and lapping one surface of the wafer. An 8–10 mil thick wafer is used most often. This keeps breakage to a minimum and does not waste material. The diameter of the wafers is not critical unless limited by processing equipment. There is a trend toward wafers of greater than 1 inch diameter in order to have more devices processed on a wafer. The upper limit is set by crystal uniformity and allowed parameter spread.

Wafers with polished surfaces are ready for subsequent processing which will take one of several different paths. If an epitaxial layer is to be provided, the wafers are put into the epitaxial process directly. If dielectric isolation is to be provided then the actual substrate used in device fabrication involves considerably more processing before it is ready for use. If diffusion isolation is to be employed the wafers are put directly into the photoengraving, oxidation and diffusion steps.

The substrate preparation for dielectric isolation is rather complex as noted above. The first step is to etch into one side of the wafer a grid pattern several mils deep. After this the surface is oxidized, then a thick layer of polycrystalline silicon is deposited over the oxide by pyrolytic deposition processing similar to that used in epitaxy. This layer must have sufficient thickness to provide mechanical support for the final structure. After deposition, part of the original silicon wafer material is removed by a combination of mechanical polishing and etching so that a grid pattern of oxide is

exposed on the surface. This surface of the silicon wafer then consists of a large number of single crystal silicon squares completely isolated from each other and from the substrate by the silicon oxide layer. This wafer is then ready for further processing.

Photoengraving

The techniques of photoengraving are necessary for planar processes and interconnections in silicon integrated device technology. The photoengraving masks which give the geometry definition on the silicon wafer are obtainable from commercial organizations or may be made in-house if the necessary equipment is available. This includes high resolution photographic and photoreduction equipment, step and repeat camera, and precision drafting equipment. Using these and the circuit topology layout provided by the design engineer, a series of photographic masks are prepared which define the areas for diffusion, contacts, or for interconnection patterns.

Wafer cleanliness to the point of obsession is extremely important for the photoengraving process but the means for achieving it will not be discussed here. Normally the photoresist is placed on a wafer by an eye dropper or similar dispensing apparatus while the wafer is spinning at high speed on a vacuum chuck. After the photoresist is allowed to air dry, it is usually baked at a low temperature before the printing operation. The patterns are aligned under a microscope. All masks after the first must align with the existing patterns on the wafer to high degrees of accuracy. Commercial apparatus is available which allows this to be done. All photoresist operations up to this step must be performed in yellow red (non-blue) light in order to avoid exposure of the resist. After alignment, the wafer with the mask tightly pressed against its surface is exposed to light with a high ultraviolet content. This changes the polymerization of the resist. The wafers are developed in proprietary developing solutions or xylene and dried. Then the wafers are baked in a vacuum oven in order to harden the remaining resist and improve its acid resistance. This pattern is then etched through the silicon oxide so that a suitable pattern of openings exists through which diffusing impurities will pass. In forming contact or interconnection patterns of metal, it is most common to use a reverse process wherein the unwanted metal is removed from the surface leaving behind the desired pattern. After the resist is used for the etching operation, it is then removed from the surface before subsequent silicon processing. This is a very difficult operation; one method is to heat the wafer in hot sulfuric acid for a short period of time.

The most common resists for the photoengraving operation are Kodak Photoresist (KPR) and Kodak Metal Etch Resist (KMER).

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Other resists are available which have valuable application for particular processes. An example is the AZ resists made by the Shipley Company (popularly known as Positop). Each group uses the one it happens to have the best success with.

The state-of-the-art of photoengraving is such that it is an inexact science. There is much to learn about all the steps required in obtaining patterns with the desired qualities. At the same time it is apparent that photoengraving techniques have been very successful in both the integrated silicon device technology and in the fabrication of silicon transistors. Photoengraving has been proven far superior to other techniques for obtaining close geometry control in very intricate patterns. The main problems associated with photoengraving are that the quality of the resist is variable, the optimum processing steps are poorly defined, better resolutions are desirable, mask making is expensive, and surface preparation and printing techniques need further development. With experience the photoengraving process is gradually coming under better control and if research is performed in some of the specific areas mentioned, it is only a matter of time until improvements are found.

Diffusion

Impurity diffusion is another one of the basic tools of silicon integrated device technology. It consists of a mixture of science and art as do the other basic processes. While mathematical theories describing simple kinds of diffusion are known, the diffusions are performed on the basis of empirically determined methods. As with photoengraving, wide variations may be found in the details of the diffusion processes at different integrated circuit facilities. These variations include the use of different types of impurity sources, different diffusion procedures and different degrees of control. The basic process requires a suitable impurity (dopant) source, almost always either a phosphorus or boron compound. The dopant is transported in vapor form by a carrier gas, usually nitrogen, over the silicon wafers and then discharged. The entire system is contained in a glass or quartz tubing depending on the temperature. The silicon wafers rest on a quartz boat at a thermally flat region of the furnace which is held very precisely at a specified temperature. Diffusion temperatures range from 900° C to 1200° C. Typical impurity sources for phosphorus are phosphorus pentoxide, phosphorus oxychloride, red phosphorus, ammonium phosphate, phosphorus tribromide, and phosphine. For boron, typical impurity sources are boric acid, boron tribromide, methyl borate, boron trichloride, and diborane. The liquid sources, phosphorus oxychloride and boron tribromide, are the most common.

There is some evidence that the gas sources, phosphine (PH_3) and diborane can be used to more advantage.

Diffusion furnaces may be purchased from a number of commercial suppliers. The control of these furnaces and their design has improved a great deal over the last several years. Thermal flat zones held to $\pm 1°$ C or less at a temperature of about 1100° C may be as long as 18 inches. Two zone furnaces are available if required for particular impurity sources. Quartz tubing and quartz boats for holding the wafers during diffusion are commercially available. Flow meters, gas handling equipment and all other necessary accessories for diffusion are well known.

By following any of the prescribed processes, acceptable diffusion results can be obtained. Normally the diffusion parameters are varied by changing the temperature of the furnace. As silicon integrated device technology becomes more sophisticated, a higher degree of control than is now possible will probably be required. Some of the inadequacies which exist in diffusion technology are: (1) agreement between theory and practice is difficult to obtain, (2) data describing diffusion processes vary a great deal between laboratories due to the use of different models, (3) present diffusion operations are largely empirical and many of the second order effects are not understood. For example, the interaction between oxidation and diffusion and data on the dependence of the diffusion coefficients on concentration are not available.

In summary the present techniques of diffusion are sufficiently well developed so as to be no problem for most contemporary silicon integrated devices. However, better control and understanding is desirable in order to make devices which are more exactly alike and whose characteristics can be predicted more accurately.

Oxidation

The ability of the thermally grown oxide on the surface of the silicon wafer to mask against impurity diffusions and to protect the junction from the environment is very important in planar silicon technology and thus to silicon integrated device technology. Everyone who has inspected surfaces covered with these oxides is familiar with the clear interference colors they cause. The clarity of the color, however, exceeds the clarity of our understanding of the properties of the oxide. Examine the requirements for the oxide in the silicon integrated device structure:

1. It is first used as a diffusion mask which process inherently contaminates it with impurity (dopant).
2. It protects silicon junctions which have fringing electric fields on the order of 10^4 V/cm (10^6 V/cm in field effect devices).

3. Oxides are used as substrates for metallic conductors.
4. In some designs the oxide is the dielectric for a capacitor structure.
5. During processing, the oxide surface helps to protect the silicon from mechanical abuse.

With all this the oxide is expected to exhibit negligible conductivity, low dielectric loss, and be thermodynamically and metallurgically compatible with the other materials with which it comes into contact. These requirements are being met and, at the same time, the understanding of charge motion in oxides and other important oxide properties is improving.

Oxides on silicon can be prepared by a variety of techniques, but the three most common oxidizing atmospheres are steam, wet oxygen and dry oxygen—all at high temperatures. Oxides formed by the three processes have different porosity conductivity growth rates and other physical properties. The most common process is steam oxidation which has a higher growth rate at a given temperature.

A typical oxidizing procedure is to place clean silicon wafers with prepared surfaces onto a quartz boat and to insert it into the quartz tube of a furnace. The furnace is very similar to those used for diffusion. A flat zone sufficient to accommodate all of the wafers is desirable. The appropriate environment is provided in the tube before the wafers are inserted. Empirical relationships will give the approximate length of time required to form an oxide of the desired thickness at a given furnace temperature. For most processing the required thickness is on the order of 7000 A=0.7 microns. A carrier gas is not necessary with steam oxidation. Instead a container of very pure water is maintained at or close to its boiling point. The vapor is forced to flow through and out of the open quartz tube.

For most processing purposes the color of the oxide which is obtained in an oxidation process is an accurate enough indication of its thickness. If sufficient care is taken, the oxides when removed from the furnace are clear, uniform in color, and free from imperfections.

Oxides can be made which are adequate for realizing good silicon integrated devices at the present time. They perform very well for diffusion masking, passivation, etc. Inadequacies stem from the fact that in processing silicon integrated devices the proper procedures are largely empirical, and at times these empirical processes fail. When the oxides on the resulting devices degenerate, often for unknown reasons, the production process must be "retuned" until successful structures again result. A failure of a production process may take the form of collector-emitter transistor shorts, leaky junctions, shorts, or similar electrical problems. Some troubles are a result of stored charge in or on the oxide which produces layers of different

conductivity on the surface of the silicon. If these layers are of opposite conductivity type, i.e., inversion layers, device failures can result. Similarly, control of the charge content in surface field-effect transistor structures is essential. Intensive studies of oxide properties which are in progress promise to provide information on space charge effects and charge carrier motion in silicon oxide (in the near future). This knowledge may well provide a new degree of freedom in the design of silicon integrated devices.

Epitaxy

Epitaxy is the descriptive word for that process wherein a thin layer of material is grown in single crystal form on a suitable substrate. While the term may apply to many materials or combinations of materials, here we are only concerned with the growth of silicon single crystal films on single crystal silicon substrates. These epitaxial films may be of opposite conductivity type and different resistivity than that of the substrate on which they are prepared. The ability to grow high quality films of this type has provided an important tool in device fabrication. In silicon integrated devices, better transistor parameters and improved isolation techniques are available through the use of epitaxial films. One may note that if the impurity distributions which determine device behavior are formed completely by diffusion then the impurity densities, as one moves into the silicon from the surface must be rapidly decreasing even when the type of impurity changes. Epitaxial techniques allow variation of impurity profiles such that larger concentrations may be below the surface and lower concentrations near the surface. The most important use of epitaxial films is to provide a very thin active region in which to fabricate silicon integrated devices, and thus to use the substrate silicon only as a mechanical support and "ground" plane.

Epitaxial techniques are diverse. A typical system consists of an induction heater, a quartz tube, a wafer holder or susceptor, and gas handling apparatus. The substrate silicon wafers are heated to approximately 1100° C by heating a susceptor (made of a conducting material) on which the wafers are resting. Different gases flow through the quartz tube in which the substrate wafers and susceptor are placed. First, the silicon wafers may be heated to high temperatures and exposed to hydrogen in order to clean and etch the surface. After cleaning, silicon tetrachloride ($SiCl_4$) is added to the hydrogen carrier gas. At the hot surface of the silicon, a reaction occurs in which the $SiCl_4$ decomposes giving HCl and Si. The silicon deposits on the substrate wafer, and at the temperature of the process, the atoms rearrange themselves into a minimum energy configuration, i.e., a single crystal layer.

Epitaxial techniques are adequate for the fabrication of transistors in silicon integrated devices. Limitations exist primarily with respect to the desire for new applications. For example, it would be useful if epitaxial material could be deposited in small selected regions of the silicon substrate. It would also be useful to make multi-junction structures with epitaxial material and be able to control precisely the impurity distribution in the structure. Other desirable goals would be improved crystalline perfection in the epitaxial layers, and the deposition of silicon epitaxial layers on other than silicon substrates.

Chemical Processing

Chemical processes are vital in fabricating silicon integrated devices; for example, etching of silicon and silicon oxide, cleaning of the silicon surface, cleaning of apparatus used in other processes, and diffusion sources. Not much need be said about these subjects since the procedures used are fairly standard. For silicon etching, hydrochloric acid—nitric acid combinations are employed; for oxide etching, hydrofluoric acid (usually buffered with another chemical) is employed; and a variety of solvents are used for cleaning the silicon surface. Ultrasonic cleaning, vapor degreasing, and other special cleaning and chemical handling techniques are used. The most important aspect of all chemical processing is to obtain chemicals of the highest practical purity. Gases used in diffusion should be dry and free of solid particle content. Deionized water employed throughout chemical processing should have a resistivity in the 10- to 20-megohm-cm range. Suppliers of gases and other chemicals have special high purity grades for use in semiconductor processing.

Some studies have been made of the effect of trace impurities on device performance. It is difficult, however, to draw specific conclusions from these studies. One important contaminant of oxides is sodium ions which may be leached from glass containers or from quartz used in the processing. Heavy metal ions in processing chemicals have been found to stick to the silicon surface and modify its properties. For diffusion sources such as phosphorus pentoxide, the chemical impurity as well as the water content can be very important. In many cases clean areas are provided to remove airborne contamination from the device environment, but these clean areas are very expensive and difficult to maintain at the required level of cleanliness. For this reason, there is a trend toward the use of small enclosures to which the devices are confined during critical operations.

Interconnection, Lead Attachment, and Encapsulation

A typical method for providing contacts, interconnections, and leads to silicon integrated devices is as follows. After the structure within

the silicon is completed, openings are etched in the oxide layer over the silicon for the metallic contacts. Aluminum is then evaporated over the entire surface and removed by photoengraving from all areas except where contact to the silicon is to be made. Then the silicon is heated briefly above the silicon-aluminum eutectic temperature and cooled, providing alloying between the silicon and aluminum. After this, aluminum is again evaporated over the entire surface and removed by photoengraving such that the desired pattern of interconnecting conductors is left on the surface. In this step, relatively large area aluminum pads are provided on the surface of the oxide but at the edges away from the active silicon substrate. Using thermocompression bonding, either with a wedge bonding tool or a ball bonding tool, gold wires are attached to the aluminum and to the feedthroughs for the particular encapsulation being employed. The silicon die is mounted in the encapsulation normally by a gold silicon eutectic bond to a metalized region on a ceramic substrate or by direct bonding to the metal header. Usually TO–5 type transistor headers or especially designed flatpacks are employed for packaging the devices.

Modifications of this basic procedure are becoming more common particularly since the purple plague intermetallic reaction between gold and aluminum has been observed in the lead contact areas. Some manufacturers prefer the all aluminum system wherein aluminum rather than gold wires are bonded to the aluminum pads on the silicon oxide. Others are providing different metallic structures for the interconnections. These may consist of a layer of chromium overcoated with a layer of gold. Flatpacks are Kovar-glass structures or glass-ceramic-Kovar structures both of which can be hermetically sealed and inexpensive. The package sealing is performed in a clean inert gas atmosphere and hermeticity is checked by helium leak detector techniques. At this stage the device is ready for final testing and use.

Summary

The processes which have been outlined here are capable of providing a high yield of good silicon integrated devices. This is evidenced by the fact that a number of manufacturers are using these or similar techniques at the present time. Omitted from the discussion was the fact that numerous tests are performed during the processes for assurance that the product is meeting specifications. For example, when the devices have been completely formed on the silicon substrate and before they have been broken into individual dice for encapsulation, complete electrical testing is performed. The motivation for this is that batch processing is used up to the point where the individual devices are separated and thus the cost per device is relatively low.

However, upon separation the individual operations involved in lead attachment and encapsulation contribute a disproportionately large cost to the device. Thus the testing is for the purpose of weeding out bad units before the final investment is made.

Device yields may run from 1 percent to over 60 percent and, of course, improve with experience in the production facility. Yields in excess of 50 percent are now common for devices which have been in production for at least six months. Devices which are produced in limited quantities and which have particularly complex patterns will normally have yields of less than 10 percent.

MULTICHIP SILICON INTEGRATED DEVICES

An important variation of the monolithic silicon integrated device is the multichip device structure. In this several chips which contain different device structures are bonded to the same substrate or header. In the packaging process jumper wires are bonded between these individual chips as well as to the package leads. The advantages of this technique are:

1. More component versatility is obtained by optimizing the processes by which different devices are obtained on the different chips. For example, transistors may be on one chip, diodes on another and resistors on a third, each formed by certain optimum processing steps.
2. Interaction between the different junction structures is minimized by mounting the chips on insulating substrates. The circuits so obtained display characteristics more closely approximating those of conventional component circuits.
3. Since the actual circuit contained in the package is determined at the assembly point, the multichip integrated circuit technology is very flexible.
4. The yield is improved by pretesting of the individual chips and eliminating those which do not meet specification before assembly into the circuit.

The multichip silicon integrated device technology is another way of assembling circuits but employs components with minimum dimensions and provides a common package for the circuit. Other than that, they have the same advantages and disadvantages as conventional circuit techniques. These include the necessity for providing wired interconnections between the separate chips, the use of a relatively large total number of processes in realizing the components which go into the structure rather than the small number characteristic of the monolithic device, and a higher cost for large production type devices resulting from the assembly and interconnection operations. If multichip structures are formed and interconnected on

ceramic substrates without the necessity for wired interconnections, a major disadvantage is removed but at the cost of forming the appropriate interconnecting pattern on the substrate. In any use of silicon single crystal chips for assembly of circuit functions, it will be of advantage to use monolithic circuit chips when available and individual component chips only when necessary. If this approach is employed, there is of course a question as to whether to form the capacitors and resistors in or on silicon or to use a separate technology for their fabrication. Means for accomplishing this are discussed in other sections of this review.

In summary the multichip silicon integrated circuit is at present an interim packaging technique which provides some but not all of the advantages of the silicon monolithic integrated device.

GENERAL DEVICE CONSIDERATIONS

TESTING OF MICROELECTRONIC DEVICES

Testing methods for microelectronic devices made by the film technologies are analogous to methods used for conventional component circuits. For integrated silicon devices, however, testing has proved to be a problem area for which new concepts have been developed. While individual component structures are tested by probing during fabrication, the prime testing operation on monolithic silicon devices is performed on the complete circuit both before and after encapsulation. The large number of tests which are necessary in order to categorize fully the integrated circuit operation has resulted in this being one of the more expensive and slow parts of the production process. In order to solve this problem, microelectronic device manufacturers have taken the lead in designing automatic test equipment capable of performing a large variety of measurements sequentially. In the design of this apparatus, advantage has been taken of the integrated circuits themselves in order to come up with low cost, high speed testing methods.

The automatic test equipment has solved the device manufacturer's problem by insuring that devices fall within specified limits. Further advances, however, are necessary in order to provide the device user with information sufficient to allow reliable application of devices. Desirable information is statistical distributions of circuit performance, the effect on circuit performance of different application parameters, time variations of circuit performance, and anything else which is necessary for intelligent application of the integrated device. The methods for specifying and testing integrated circuits need reexamination and improvement over techniques now employed.

INTEGRATED CIRCUIT DESIGN THEORY

The design of film microelectronic devices is analogous to conventional circuit design. Silicon integrated devices again present unique problems because of the interactions which exist between components within the structure and because of the deviations of component parameters from the optimum values which are available with separate components. The technology of silicon integrated devices has advanced considerably beyond the ability of present models to explain and predict the phenomena observed. The present models are from transistor theory which was developed to account only for first order phenomena. When applied to integrated silicon structures, the second order phenomena which have not been treated theoretically are often important in determining performance. There is, therefore, a necessity for developing theoretical techniques which supplement the empirical design technique now employed.

LOGIC DEVICES

Logic devices are required to provide gating, level restoring, memory, etc. The realization of these functions in microelectronic devices is based upon conventional circuit design methods. Again in thin film type structures, the conventional circuit design procedures can be carried over on a 1 to 1 basis and any circuit available in conventional components can be realized in the film technology so long as inductors and transformers (both are relatively rare in logic circuits) are not

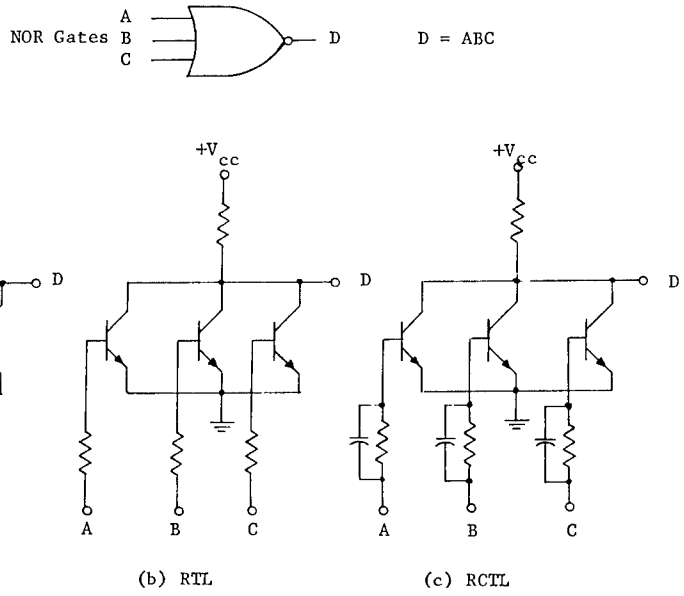
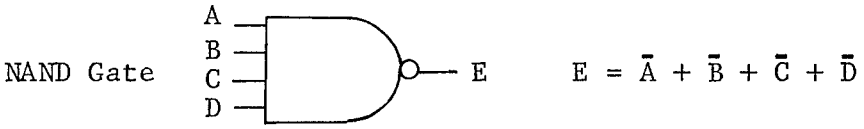


FIGURE 1.—*Direct coupled transistor logic gate circuits.*

required. In the silicon integrated device structures, however, special design considerations must be taken into account. One of these is the inverted economics of the silicon structure; that is, the transistors and diodes are very inexpensive when compared to resistors or capacitors.

The simplest form of logic circuit which is available in integrated form is DCTL or direct coupled transistor logic. The basic circuit configuration of DCTL is shown in figure 1a. Variations of DCTL include resistor-transistor logic (RTL) and resistance-capacitance transistor logic (RCTL) which are shown in figures 1b and 1c. A second form of logic which has been applied in silicon integrated devices is diode transistor logic (DTL). One version of this is shown in figure 2. Other important logic designs are transistor-transistor logic (T^2L) shown in figure 3 and emitter coupled transistor logic (ECTL) which is shown in figure 4. Thus most of the logic devices available can be classified into three major types, viz, DCTL, DTL, and ECTL. Most devices which are available are of the DTL type.



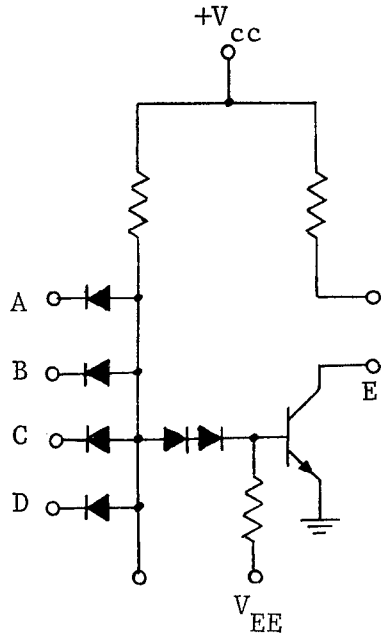
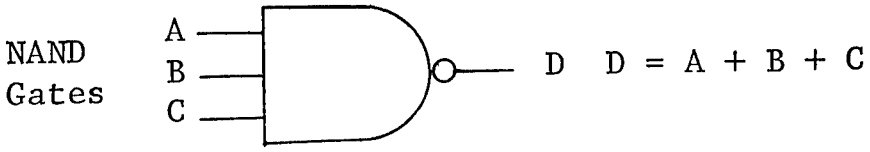


FIGURE 2.—*Diode transistor logic gate.*

The logic circuit configurations are evaluated for various applications on the basis of a small set of significant parameters which include speed, fan-out capability, noise immunity, power dissipation, and required power supply. Table III gives comparative characteristics of several commercial types. Some analysis of these with respect to micropower application is discussed in a later section of this report.



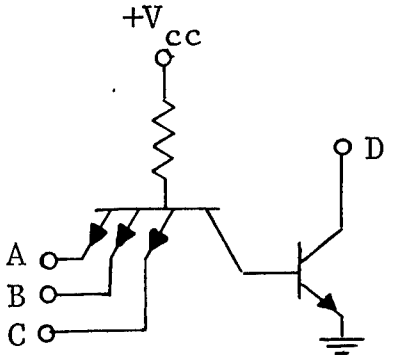


FIGURE 3.—*Transistor-transistor logic gate.*

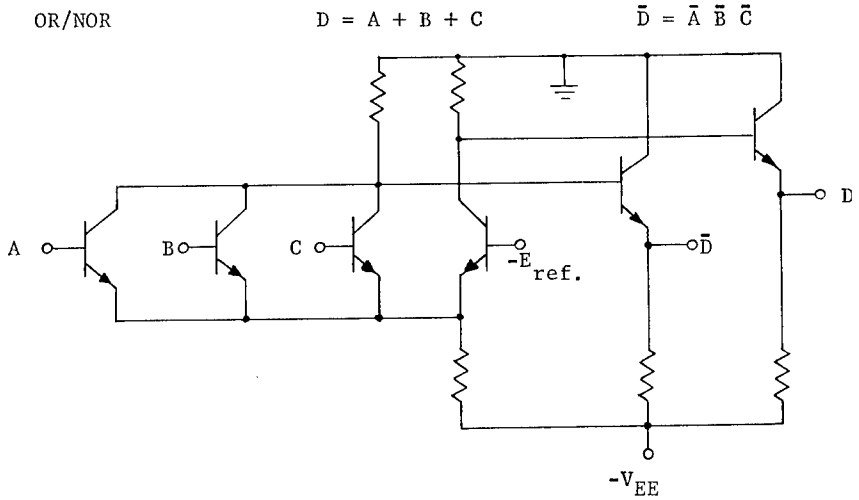


FIGURE 4.—*Emitter coupled transistor logic gate.*

TABLE III.—*Comparison of Several Logic Circuit Types*

Manufacturer type	Speed		Fan out		Noise margin (mV)	Power dissipation single gate (mW)	Operating temperature range (°C)		Supply voltages (volts)
	Gate delay, fan out=3 (nsec)	Binary count (Mc)	Gate	Buffer			Min.	Max.	
Fairchild HSμL900 DCTL	15	10	5	25	250	12	−55 +15	+125 +55	+3
Signetics SE100 DTL	30	10	5	25	500	7	−55	+125	+4 and −2 or 0
Motorola MC300 ECTL	7	30	26	—	320	35	−55	+125	−5. 2 −1. 15
Texas instrument series 51 RCTL	200	0. 8	5	25	—	2	−55	+125	+3
Fairchild MWμL 900 DCTL	50	8	4	30	300	2	−55	+125	+3
Signetics Utilogic	25	8	10	17	1000	5	0	+70	+4. 5
Westinghouse WM 200 DTL	35	11	11	17	550	8	−55	+125	+6
Fairchild 930 DTL	25	10	9	20	700 550	5	−55	+125	+4
Siliconix "A" series DTL	18	10	15	—	900	4	−55	+125	+4
General Microelectronics Multi-logic RTL	40	2. 5	4	30	80	5	−55	+125	+3

LINEAR INTEGRATED CIRCUITS

Because of the smaller market for linear circuits and the more difficult design and fabrication features of these circuits, fewer linear circuits are available in commercial form. Attempts are being made to increase the potential market for particular linear integrated device designs by making them more flexible. Either extra devices are provided in the structures with a variety of possible interconnection patterns or several components are left out of the silicon structure so that flexibility can be achieved by providing different external components.

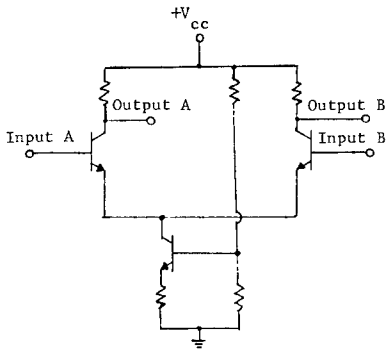
Because dc coupling is easiest in silicon integrated structures, bias point stabilization has been a problem since silicon resistors and junction parameters are highly temperature sensitive. Techniques for avoiding this temperature dependence have been developed by using resistance ratios and compensating junctions which help to avoid shifts with temperature. DC feedback is often used to eliminate resistors and to provide additional stabilization. Differential amplifier stages are employed to improve the stability of single ended amplifiers. In linear structures wide use has been made of the Darlington amplifier connection to provide moderately high input impedances. A few examples of linear integrated silicon amplifiers are shown in figure 5, along with typical operating characteristics. Probably the market for linear circuits will remain less than that for digital types and the price will remain relatively high. At the same time design techniques are advancing to where very good performance is being exhibited; this makes integrated amplifying structures competitive with conventional circuits on the basis of cost and performance. At the same time, integrated linear circuits possess the same advantages of reliability as their digital counterparts.

RELIABILITY

The potential reliability of microelectronic devices has been the primary reason for their development. If one adopts the qualitative definition of reliability as being a measure of one's confidence that the device will perform as intended, then most microelectronic structures are reliable. This is because system designers do have considerable confidence in the performance of microelectronic structures. If one desires quantitative reliability numbers, then the situation is more complex. This is because with the excellent reliability of microelectronic devices, statistics are difficult to accumulate which allow the assignment of realistic reliability numbers. It has been customary to extrapolate from known performance capabilities of transistors made by the same technology in order to be able to quote ballpark reliability figures. At the present time, however, sufficient testing has been performed on certain types of silicon integrated devices to where

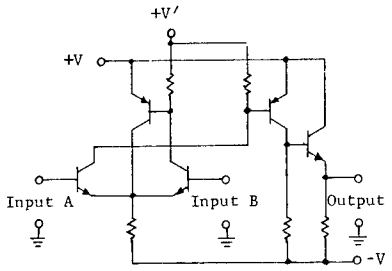
meaningful numbers can be given. One example is given in "Redundancy Made Possible by Microelectronic Devices," Chapter 4.

The most important reliability problem with microelectronic devices is "foolish" failures. In this category fall those defects in the device structure which could be readily avoided if during the design and fabrication of the device no mistakes were made. A majority of the



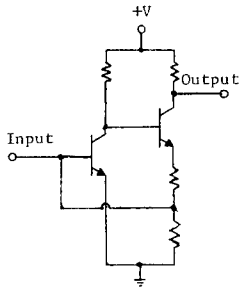
Voltage Gain	145
Input (mv)	5
Input Impedance (kΩ)	2.5
Output Impedance (kΩ)	13
Bandwidth (kc)	900
Supply Voltage (v)	+12

(a) Fairchild μC 109 Differential Amplifier



Open-loop Voltage Gain (db)	62
Common-mode Rejection (db)	60
Bandwidth (kc)	50
Input Impedance (kΩ)	12-100
Output Impedance (Ω)	160
Supply Voltage (v)	10,6,-9

(b) Texas Instruments SN522 Operational Amplifier



Insertion Power Gain at 3 Mc (db)	30
Input Resistance (Ω)	300
Output Resistance (Ω)	200
Input Capacitance (pf)	230
Supply Voltage (v)	+12

(c) Westinghouse WM-1101 RF Amplifier

FIGURE 5.—*Integrated linear circuits.*

observed failures or screening rejects have resulted from carelessness in manufacture. Fortunately, it is this type of mistake that with production experience is easy to eliminate; so those devices which have been in production for a sufficient period of time usually exhibit a minimum number of foolish failures.

The best approach to obtaining reliable devices is to study devices in great detail in order to identify failure causes. If these failure modes are eliminated and screening techniques are adopted which allow the detection of latent failure modes with a minimum of testing, then high reliability can be achieved. Standardization on a relatively few circuit types can obviously be of great assistance here since the testing and evaluation are time consuming and expensive. One version of this testing procedure is that wherein the performance of devices is studied in detail and mathematical models determined which express the performance in terms of those factors which affect it, i.e., equivalent circuits are developed. The equations of the model state the interrelations between the various parameters and predictions can be made to the accuracy of the equations and over the range in which they are applicable.

Conventional reliability techniques have been inadequate for treating high reliability microelectronic devices. Before much can be done with mathematical techniques, some advances in the methodology of reliability are necessary. In the meantime the best approach is probably that which assures good qualitative reliability by elimination of failure modes.

APPLICATIONS

The use of microelectronic devices is increasing rapidly. Most of this increase is represented by silicon integrated devices which are now being sold at a rate greater than 180 000 per month. This use rate will probably increase rapidly in the future. A long list of electronic system applications of microelectronic devices can be given. This list increases weekly and includes such major systems as the IBM 360 computer series which employs thick film type microelectronic circuits, the new RCA Spectra computer line which employs silicon integrated devices, other smaller commercial computing systems, the Minuteman missile program, hearing aids, control systems and a variety of space electronic systems. The percentage of circuit functions which can be fabricated in silicon integrated form at the present time varies from nearly 100 percent for logic circuits of a digital computer to about 50 percent for radar and communication equipment. For those applications not suited to microelectronic devices, conventional components can be employed.

Attempts to convert electronic systems from conventional circuits to microelectronic integrated devices without considerable redesign are of little value. Before redesigning, the technical feasibility of performing the required circuit function and the economics of the integrated circuit design must be determined. Once a decision is made to go to microelectronic devices other factors must be considered. First, what form of microelectronics, film or integrated structures should be used? Usually the silicon integrated structure is desirable because most readily available commercial microelectronic devices are of this type. In using silicon integrated devices decisions are necessary on the type package to be employed, the interconnection methods, and other factors in system design. The cost factor is of course not negligible. It has been estimated that for a small computing system the industrial type silicon integrated devices now offer considerable cost savings over standard transistor circuits. In military systems where higher cost structures must be employed, this saving is not present, but the added cost is justified adequately by the reliability improvement of the equipment. Although size and weight are not important for many applications, in others they are. The value of weight saving has been estimated to be $0.05 per pound for stationary electronics and $20 000 per pound for deep space systems; most applications fall between these extremes.

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Chapter 2

Technology and Techniques

PERSPECTIVE

This chapter is concerned with NASA contributions to the technology and techniques by which microelectronic devices are designed, fabricated and tested. Specific device designs, reliability and applications due to NASA are discussed in subsequent sections. Under this broad classification of technology and techniques, NASA contributions have been relatively small, not because of lack of interest, but because in the formulative years of the space research program it has been necessary to make maximum use of existing electronic devices and techniques. It is only now, when the limits of present available technology are being strained by the demands of space research, that considerable attention is being given to microelectronic devices. As these in turn are employed, NASA interest in improving microelectronic device technology is growing. The work which is described in the following paragraphs represents early evidences of this interest. The rate at which contributions to the technology of microelectronc devices flow from both NASA research centers and from supported research activities is expected to increase rapidly.

Among the most significant aspects of microelectronic technology in NASA is the development of significant internal research and development capabilities. These include the thin film facility at the Manned Spacecraft Center in Houston, the silicon integrated device research and development facility at the Marshall Space Flight Center in Huntsville, the thick film and silicon laboratory facilities at the Langley Research Center, and a silicon integrated device research and development facility at the Goddard Space Flight Center. It is to be expected that research capabilities will be further developed, particularly at the Electronics Research Center, and that internal capabilities of NASA with respect to microelectronic devices will include all variations of such devices and will have considerable impact.

Several of the most interesting contributions to microelectronic device technology are now active NASA supported programs. These include the development of infrared scanning equipment by Raytheon, the acquisition of an electron beam scanning microscope from Westinghouse, and reliability oriented studies. The latter include studies

of failure mechanisms originating in the epitaxial process, material properties, or other of the basic processes; and studies of interconnection techniques. The following sections discuss specific contributions about which sufficient information was available.

THICK FILM CIRCUITS

Thick film circuits are considerably larger than those formed in silicon and must have active devices inserted. Circuits are flexible in fabrication, low cost, and radiation resistant, and have good reliability potential. Long range applications depend on combination with silicon integrated devices for system assembly. Langley Research Center has developed a fabrication facility and has supported both internal and external research activities.

The microelectronics research group at Langley Research Center has been developing thick film or cermet technology as an interim packaging process for space electronic systems. The basic aim of this research has been to eliminate the troublesome interconnections characteristic of conventional electronic circuits. This is done by using screen deposition and high temperature processing to obtain passive components and interconnections. Areas to which particular attention has been given are (1) development of a high resistivity low temperature-coefficient material for the deposition of resistors, (2) development of a compatible material for capacitor dielectrics, (3) the overall thick film circuit deposition process in order to make it more efficient and more flexible for application to space research instrumentation. The results of this effort are operating circuits which have been demonstrated and which will soon be used in space experiments.

CERMET RESISTORS

In the past, in thick film screened circuits, the printed resistor has been of comparatively inferior quality due to the use of carbon base resin inks. These resistors are relatively unstable, particularly when exposed to high humidity and elevated temperatures. More recently, palladium-silver glazes have been developed which are fired at 750° C and result in stable resistors. The resistivity of these compositions is adjusted by varying the proportions of conductive and nonconductive material in the paste. At sheet resistivities of greater than 20 kΩ/square, the resulting resistors are erratic, nonreproducible, nonlinear, and noisy. In addition, resistance values are difficult to reproduce. The objective of one research effort [1] was to develop higher resistivity paste compositions which could be applied by screen printing on a ceramic substrate and fired at approximately 600° C. Prior experience by the contractor on this subject had indicated the desirability of

[1] Speer Carbon Company—Contract NAS1-3155.

using thallium oxide and glass mixtures and the research consisted of an empirical study of process and composition variables using these basic materials.

The basic materials employed were thallium oxide with an average particle size of 0.2 micron and a lead-borosilicate glass frit having an average particle size of 1.5 microns and a softening point of 460° C. Terminations for the resistors were made with platinum-gold paste fired at 930° C. The materials for the resistors are combined and mixed with a temporary binder to give the desired viscosity. A typical paste had the following composition: 9.3 grams of thallium oxide, 20.7 grams of glass frit, 0.46 gram of ethyl cellulose, 10.47 grams of butyl carbonyl, and 2.27 grams of ethyl alcohol. These pastes were printed in appropriate patterns on ceramic substrates using stainless steel screens. All resistors were air dried prior to firing and were approximately one mil thick. They were fired by carrying them through a high temperature furnace on a continuous belt conveyor. The peak temperature during firing was 520° C for most tests. As the weight percentage of thallium oxide in the fired composition was reduced from approximately 60 percent to 25 percent, the sheet resistivity of the resulting patterns increased from below 1 kΩ/square to greater than 1 MΩ/square and was dependent upon the particular type substrate employed as shown in figure 6. When silver termination pads were used, the silver migrated into the resistor element during firing and affected its resistance. This was determined by potential distribution measurements on the resistor pattern. Platinum-gold terminations did not diffuse into the resistor. The variation of resistance values with thallium oxide particle size revealed that the resistivity was approximately inversely proportional to the particle size. The dependence of sheet resistivity on firing temperature was different for alumina and titanate substrates. A complex dependency on firing temperature was obtained, and a definite minimum in sheet resistivity was found between 500 and 600° C firing temperatures. Q–12 glass from Harshaw was the best glass tried although it was modified by adding 10 percent zinc oxide to improve its stability on alumina substrates.

A large number of resistors were tested under several conditions of moisture, overload, temperature, and time. Temperature coefficients were between −247 and −338 ppM/°C. Changes in all tests were under 1 percent. The voltage coefficient of resistance was about 30 ppM/V. Life test data on resistors indicate that the average resistance change at 10 000 hours is 2 percent or less. These results apply to sheet resistivities up to 1 MΩ/square. The stability, TCR and noise index of the compositions can be improved with further research. Additional reliability testing is also desirable.

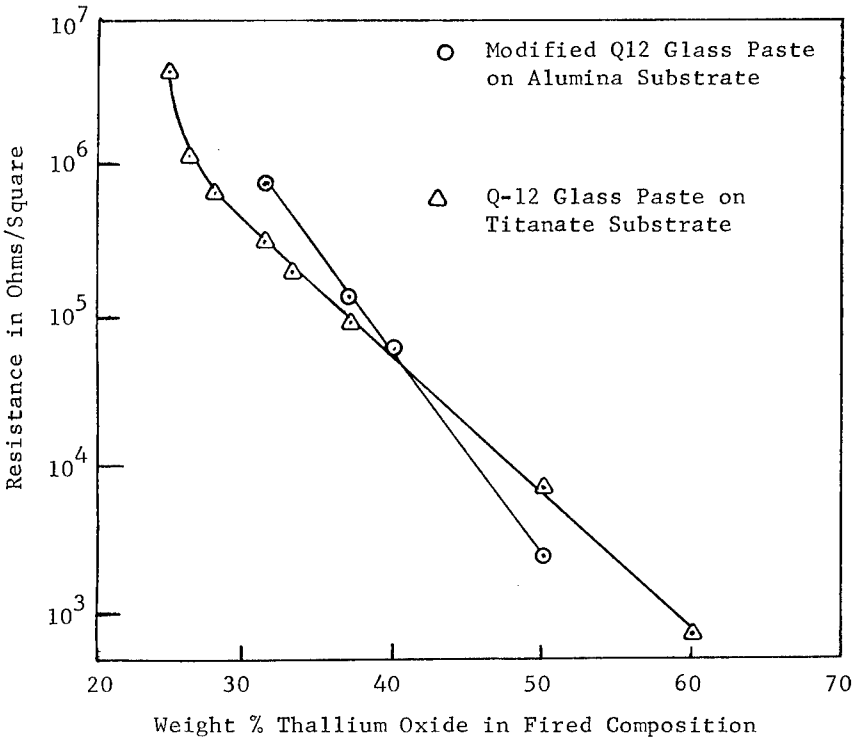


FIGURE 6.—*Variation of sheet resistivity with composition.*

SCREENED DIELECTRIC FORMULATIONS

Screen circuit capacitors are available from several sources. The particular techniques used by the various suppliers, however, have not been revealed and in general have well defined limitations. For this reason an internal NASA project was established to develop dielectric formulations for use with screened microcircuits which could be employed both for capacitors and for insulation between conductors on the substrate.[2] Such a dielectric allows replacement of wire jumpers attached to the substrate and elimination of inserted capacitor chips. The basic problem was to obtain a dielectric material, compatible with the screening process and the microcircuit structure, that becomes a high abrasive-resistant film when fired. Some of the requirements for this dielectric formulation are:

1. It should allow subsequent deposition and firing of a top conductive pattern.

[2] Stermer, Robert L. Jr., "Dielectric Formulations for Use in Processing Screened Ceramic Microcircuit Substrates," 1964 IEEE International Convention Record, Part 9, p. 47.

2. The constituents should be commercially available.
3. The formulation must be screenable, i.e., consist of micron sized particles in an organic binder with a viscosity in the 10^5 centipoise range.
4. The material must fire in a vicinity of 1000° C in order to be compatible with the firing temperature for conductors.
5. The coefficient of thermal expansion of the resultant dielectric film should be compatible with that of alumina which is 6.5×10^{-6}/°C near room temperature and 7.9×10^{-6}/°C at higher temperatures, in order to prevent the creation of large internal stresses in the films.
6. It must be chemically compatible and have good bonding characteristics with the rest of the microcircuit structure.
7. The gas generation should be minimal during firing in order to prevent voids from forming in the film.
8. Its dissipation factor should be less than 0.01 and its dielectric constant should be about 70 for capacitors and around 5 for insulators.

TABLE IV.—*Composition of Thick Film Dielectric for Capacitors.*

High dielectric constant with medium dissipation factor		
Material	Formula	Weight percent
Lead monosilicate	$PbO–0.67\ SiO_2$	65. 0
Barium titanate	$BaO–TiO_2$	22. 5
Lead zirconate titanate	$0.93\ PbO — 0.47\ TiO_2$ $0.07\ SrO — 0.53\ ZrO_2$	10. 0
Calcium stannate	$CaO–SnO_2$	2. 5
		100. 0
Medium dielectric constant with low dissipation factor		
Material		Weight percent
Lead monosilicate		75. 0
Lead zirconate titanate		25. 0
		100. 0

For the capacitor dielectric formulation a ceramic with a high barium titanate content was expected to be required to attain a large dielectric constant. An additional subdivision is possible between high capacitance which can usually tolerate a large dissipation factor and moderate to low capacitance which requires a low dissipation factor. The two recommended formulations are given in table IV and are specifically designed for use with 95 percent alumina substrates and Du Pont gold-platinum conductive material number 7553. The insulator formulation was chosen by a study of 17 commercial glass frit formulations. The best insulator was commercially available as Ferro Corporation frit number 3467. The organic binder used with all of these dielectric formulations was a mixture of butyl cellosolve acetate and ethoxyl T–10. These formulations can be stored in bottles until used.

The thickness of the dielectric film depends upon the viscosity of the formulation and the screen mesh size. In this study a viscosity of 10^5 centipoise and a 165 mesh screen are recommended. A photograph of the screen press which was developed for application of films is shown in figure 7. The distance between the substrate and the screen is 50 mils. Tension of the screen is such that the contact area of the screened substrate is about 4 or 5 thread widths when the squeegee passes over the deposition area. After deposition on the ceramic substrate the wafer is dried in a vacuum of approximately $\frac{1}{10}$ atmosphere for 10 minutes and heated on a hot plate to about 110° C. Firing was in a kiln at approximately 1000° C. The schedule as shown in figure 8 requires rapid heating to the specified temperature and slow cooling, the entire time being about 40 minutes. The resultant capacitor dielectrics were semi-opaque, yellow and had a smooth, uncrazed hard surface.

The top conductor was applied by firing at approximately 20° C lower temperature. It was noted that if subsequent layers (from the bottom conductor under the dielectric to the top conductor) were fired at successively lower temperatures fewer holes were detected in the dielectric.

The insulating or crossover dielectric is screened in the same manner and fired at about 900° C. These crossover dielectrics were clear in appearance after firing and appeared to be of good quality under a microscope.

The resulting properties of the dielectric films are shown in figures 9 and 10. The capacitance was approximately 0.25 μf/inch^2 for the high dielectric constant material and 0.009 μf/inch^2 for the other. The distribution of capacitance values obtained in the process is shown in figure 11 for the high dielectric constant material.

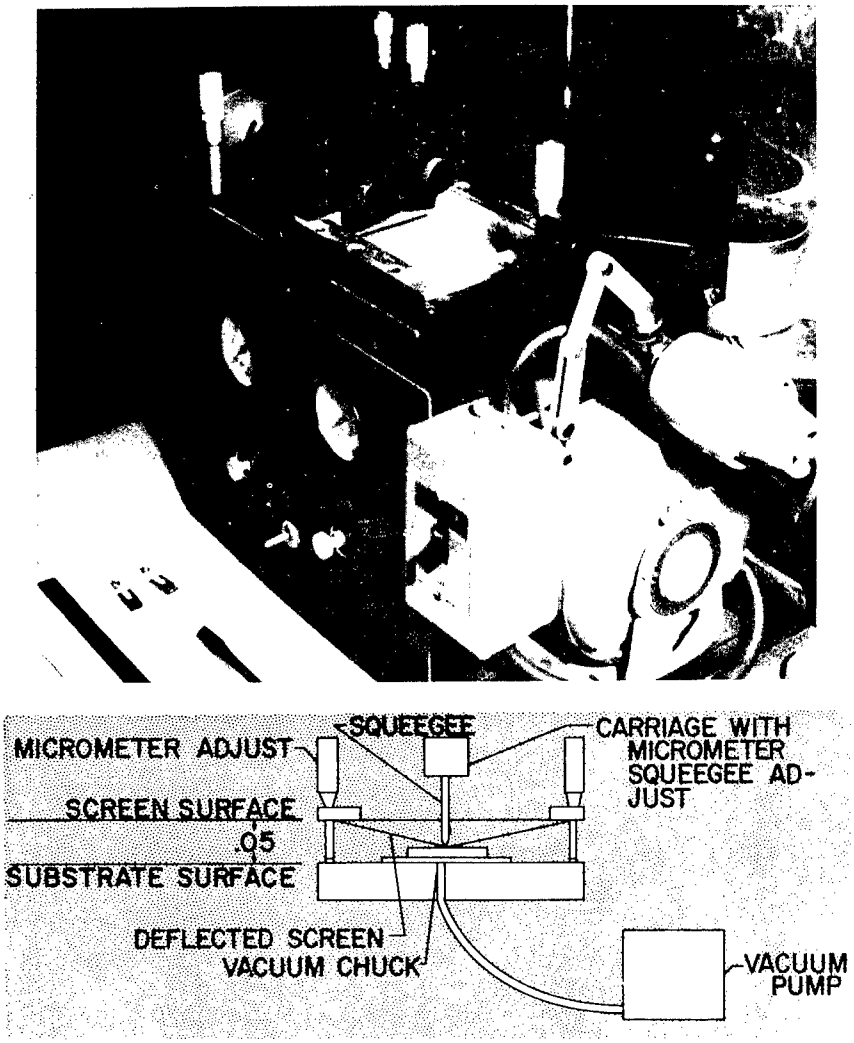


FIGURE 7.—*Screen circuit press. Top: screen press; bottom: block diagram of essential parts of screen press.*

The crossover dielectric was a low-loss minimum-coupling insulator with a stray capacitance between conductors of less than 1 pf/inch^2 at room temperature and a dissipation factor of about 0.006.

Other work is being done in order to perfect methods for firing the dielectrics and conductors at the same time. The principal problem is the emission of gas during firing which detracts from the quality of the films. By inserting the crossover and capacitor dielectrics into the microcircuit structure, about 25 percent of the bonding connections

can be eliminated. The remaining bonding connections are necessary in order to install diodes and transistors. It is desirable that techniques be developed for inserting such components without wire bonds. These dielectric materials are also being investigated for application with compatible resistive films to fabricate distributed parameter networks. The objectives for this particular activity have been met and capacitor and insulator films can be provided routinely by screened film processes.

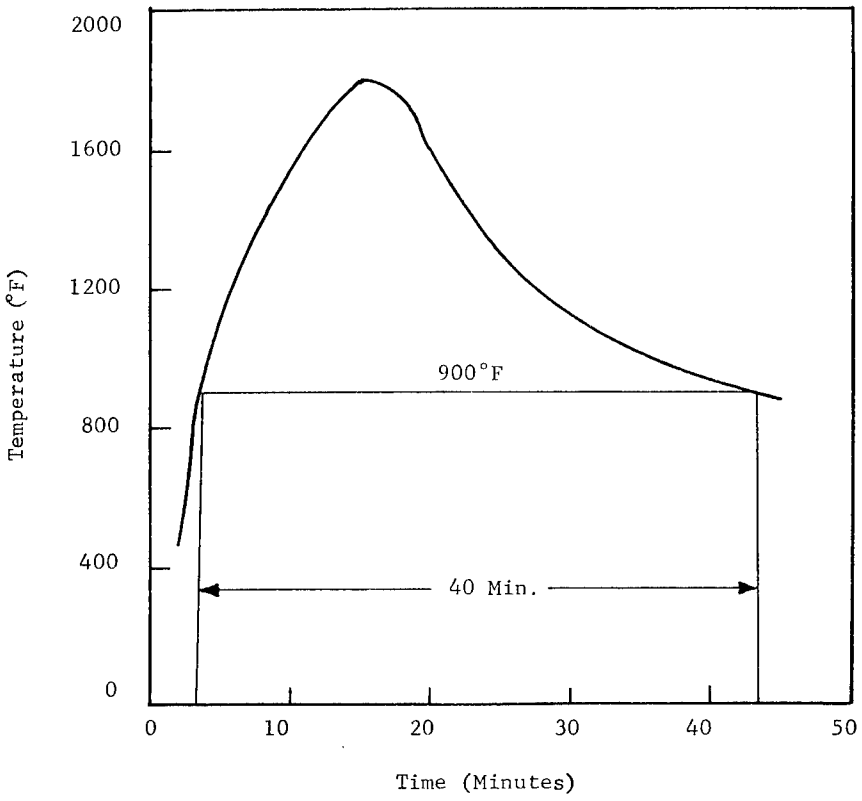
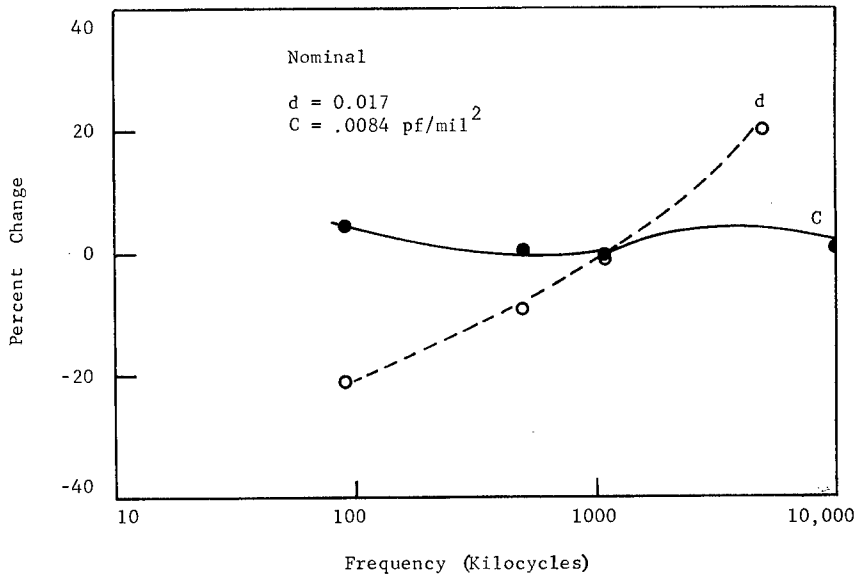


FIGURE 8.—*Firing schedule of capacitor dielectric films.*

Examples of a diode-resistor network and a more complex circuit which were fabricated in the facility at Langley are shown in figure 12.



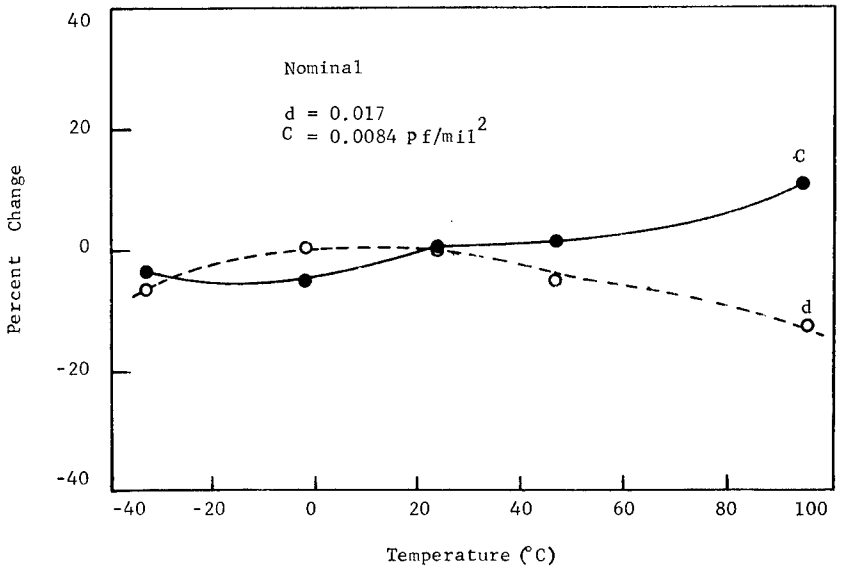
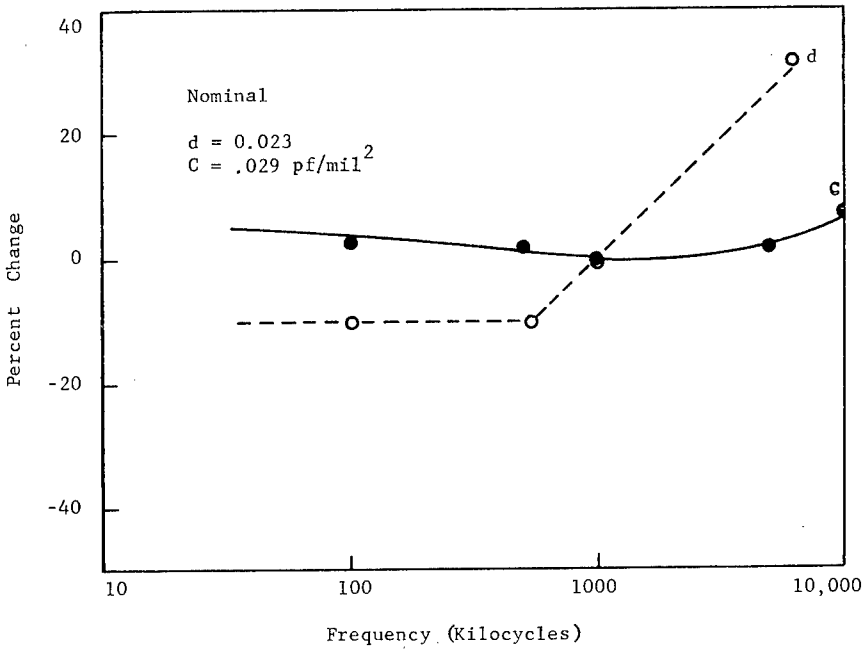


FIGURE 9.—*Properties of low dielectric constant films.*



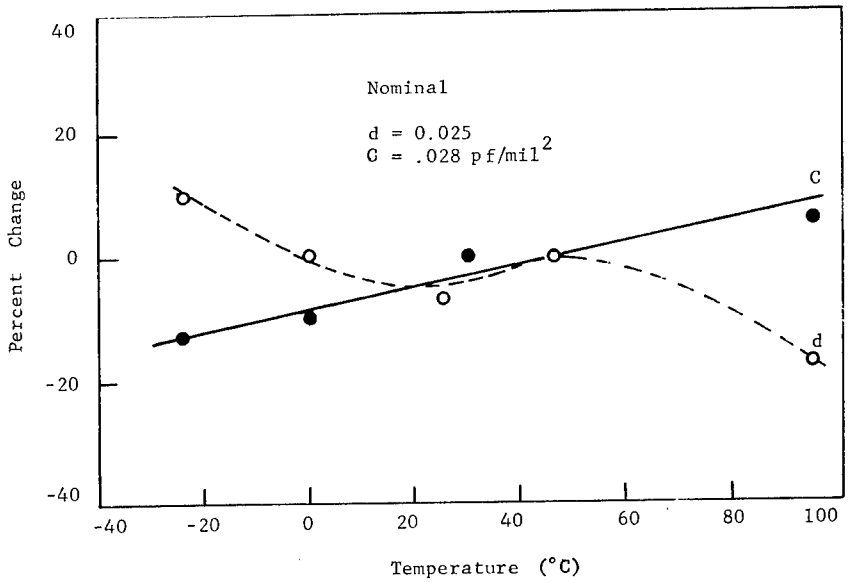


FIGURE 10.—*Properties of high dielectric constant films.*

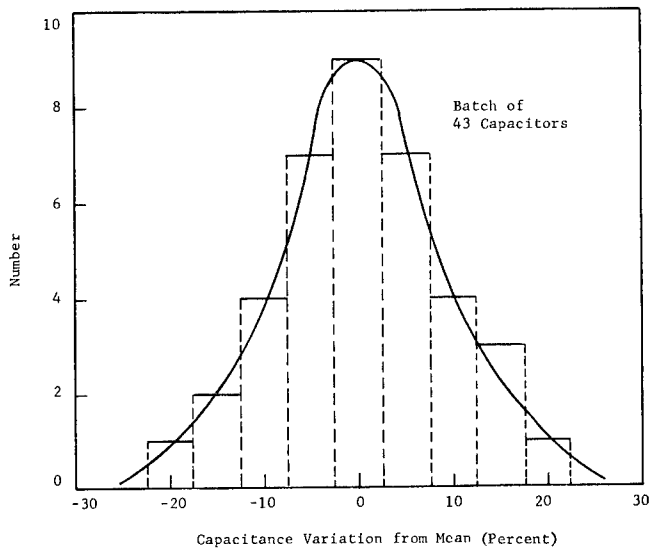


FIGURE 11.—*Distribution of capacitance values for high dielectric constant material.*

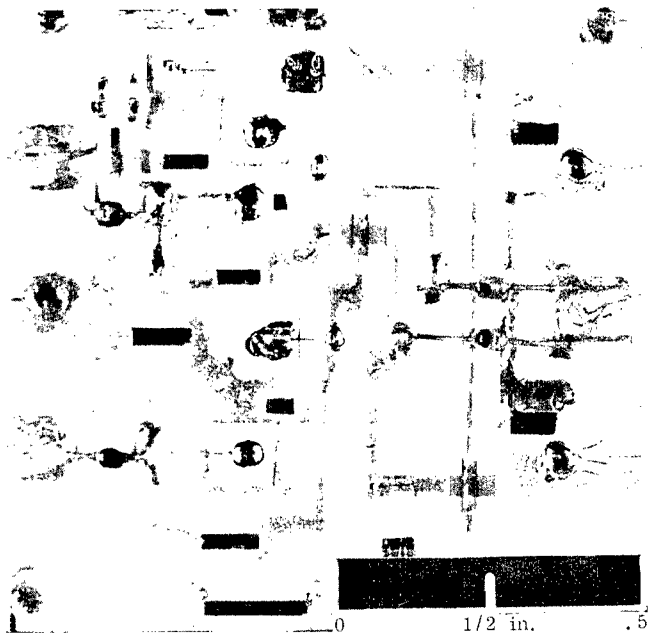


FIGURE 12.—*Examples of Screened circuits. (a)*

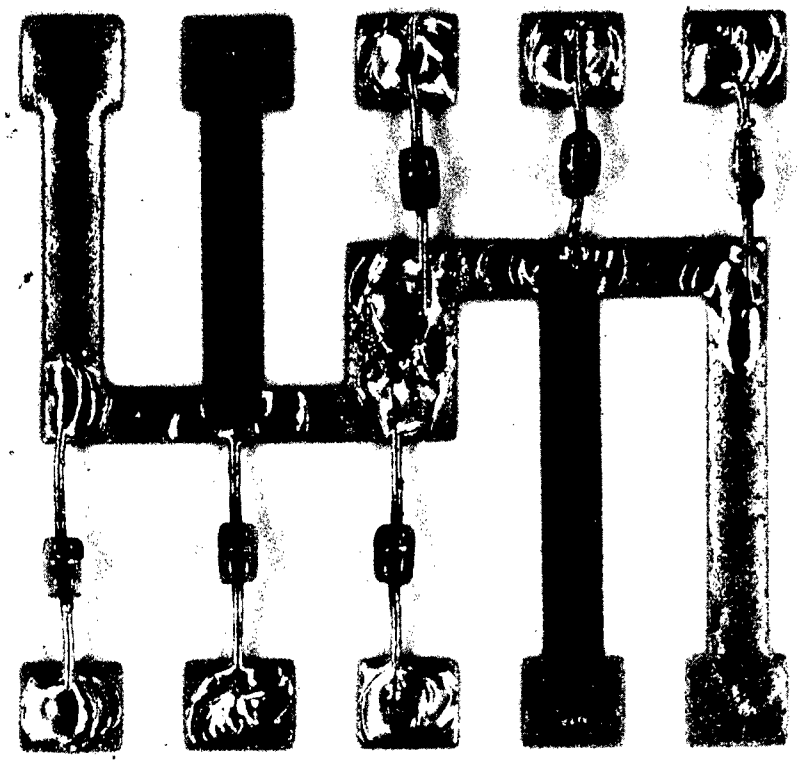


FIGURE 12.—*Concluded.* (*b*).

SINGLE-CRYSTAL SEMICONDUCTOR FILMS [3]

Single crystal films are of potential use for fabricating active thin film devices. At JPL, high quality single crystal films of germanium have been obtained by using an electron beam to produce a small molten region and moving this repetitively over the film area.

An internal research effort at the Jet Propulsion Laboratory has succeeded in growing large area single crystal germanium films by means of microzone melting. In brief, germanium films are prepared by normal evaporation techniques on sapphire substrates and then heated to approximately 850° C (their melting point is 950° C). A small zone of this film is further heated to above the melting temperature by means of an electron beam which is obtained from a modified electron microscope. This electron beam is scanned in a regular grid pattern. During this scanning process, small crystallites of germa-

[3] Maserjian, J., "Single-Crystal Semiconductor Films by Microzone Melting," Jet Propulsion Laboratory Memorandum.

nium which are found at the edge of the molten zone grow in size. Certain preferred crystalline orientations propagate preferentially and, after repeated scans, dominate the morphology of the film. It was determined that the crystalline structure of the sapphire did not contribute to this growth process. The crystalline nature of the films was confirmed by both X-ray and electron diffraction studies. Hall effect measurements were employed to obtain resistivity, carrier concentration, and carrier mobility parameters. A typical film had a resistivity of 0.7 ohm-cm, p-type with a carrier concentration of $5\times10^{15}/cm^3$ and a mobility of 1900 ± 500 $cm^2/Vsec$. The mobility values suggest that the zone-melted film approaches the properties of bulk single crystals. No attempts at making devices from these films have been reported.

The large interest in obtaining active devices compatible with thin film circuits as well as the interest in various aspects of electron beam technology for applications in microelectronics make this research particularly interesting. Similar work is in progress at other laboratories but this is the first report on electron-beam zone-melting crystalline-growth in semiconductor films on passive substrates.

GOLD-FILM THICKNESS DETERMINATION

Measurement of the thickness of thin films is normally performed by tedious optical techniques. An electrical method is described here which gives good agreement with optical methods for thickness of gold films greater than 400 A.

A method of determining the thickness of vacuum-deposited gold films using film resistance and Hall voltage measurements has been studied at the Langley Research Center.

For a given thin isothermal film of thickness t in the x–y plane in the presence of an electric field E_x and magnetic field H_z, the effective electron mean free path, λ_{eff}, can be written as

$$\frac{\lambda_{eff}}{\lambda_0}=\left(\frac{A_H(t)}{A_{H_0}}\right)^{2/3}\frac{\sigma(t)}{\sigma_0}, \tag{1}$$

where λ_0 is the effective mean free path in the bulk material, A_H is the Hall coefficient, σ is the conductivity, and the zero subscripts denote bulk material quantities. The parameters $A_H(t)$ and $\sigma(t)$ are complex functions of the thickness.

If the resistance, R, and the Hall voltage, V_y, for a given current I_x and magnetic flux density B_z, is measured for a section of film of length Y and width X, λ_{eff} can be written as

$$\frac{\lambda_{eff}}{\lambda_0}=\frac{Y}{RX}\frac{1}{\sigma_0}\left(\frac{V_y}{I_xB_z}\frac{1}{A_{H_0}}\right)^{2/3}t^{-1/3} \tag{2}$$

Thus, given the Hall voltage and resistance, thickness of a film can be determined by plotting equation (2) for various values of t and noting the intersection of this curve with the curve plotted from equation (1) as a function of t. This graphical method is equivalent to equating equations (1) and (2) and solving for t.

Using the above method, the thickness of unannealed gold films has been calculated and compared with optical interferometer measurements as shown in table V.

TABLE V.—*Comparison of Film Thickness Determined from Graphical Method with Values Measured with a Multiple Beam Interferometer for Four Gold Films*

Film	Graphical method	Interferometer
A	126 A	182 A
B	295 A	333 A
C	492 A	516 A
D	935 A	920 A

The results are within 5 percent for films with a thickness greater than 400 A. However, for thinner films, greater differences occur, probably due to variations in film structure. The resistance measurements in the unannealed films are particularly susceptible to errors caused by stresses in the film. This work has been described by Leonard and Ramey.[4]

SINGLE-CRYSTAL BERYLLIUM OXIDE (BeO)

Single crystal refractory substrate materials are potentially useful for epitaxial film formation, etc. BeO which has good thermal conductivity is particularly attractive. Small single crystals were grown.

A program was performed by the National Beryllium Corporation for OART, NASA headquarters to develop techniques for the growth of single crystals of beryllium oxide (BeO). The crystals were to be suitable for use in microelectronic applications and their mechanical, thermal and dielectric properties were to be studied.

Single crystals of BeO with hexagonal cross sections and diameters from 50 to 175 mils were grown. Chemical purity of better than 99.9 percent was noted for all crystals with nearly all contamination occurring on the surface.

[4] Leonard, W. F. and Ramey, R. L., "Thin Film Thickness from Theoretical Expressions for Conductivity and Isothermal Hall Effect," Journal of Applied Physics 35, 2963, 1964.

Results of experimental work show that monocrystalline BeO has many physical and mechanical properties which make the material more attractive than the polycrystalline variety. The use of single crystal BeO, preferentially aligned, shows indications of far superior performance for applications as window, filter and controlled energy transfer materials.

HERMETICITY TEST FOR INTEGRATED CIRCUIT FLATPACK

Easy and fast methods for checking hermeticity of integrated circuit packages have been developed.

In testing integrated circuits for the Apollo guidance computer, a number of techniques have been developed which may find wide application. Among these are a hermeticity test for insuring that the flatpacks are leak proof (sometimes they do leak).

One very successful test is to pressurize (150 psig of N_2) a group of flatpacks in a small chamber. Immediately after removal from the chamber, the devices are submerged in alcohol and observed under a microscope. If pin holes exist in the packages small bubble streams are observed to come from them. The use of this technique has succeeded in revealing not only lack of hermeticity in the flatpack but also some gross packaging problems. One example of this is that after pressurizing in the nitrogen chamber several flatpacks have actually been observed to "flip their lids" at normal pressure. These packages not only leaked but were sufficiently fragile so as not to be able to contain the 150 psig.

A second method for leak testing integrated circuit flatpacks is based upon a military standard test. The devices are submerged in hot glycerin and bubble formation is looked for. If the devices are not hermetic, bubbles form at the leak. A more sensitive modification is to take devices directly from a cold chamber at $-65°$ C. At this lower temperature a larger amount of gas will have accumulated in a leaky flatpack and thus it will evolve gas more rapidly when heated.

FLATPACK HOLDER FOR TESTING INTEGRATED CIRCUITS

Convenient flatpack holders for breadboarding integrated circuits have been designed. These allow testing of system concepts without damage to the flatpack leads.

A number of techniques have been devised, usually by the device manufacturer, for the testing and breadboarding of integrated circuits. In the TO–5 can this has presented no particular difficulty since transistor type sockets were readily available even for the ten lead

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configurations. However, the integrated circuit flatpack, which is finding increasing favor for packaging silicon integrated devices, has presented a number of testing problems and in breadboarding systems many of the holders are unreliable. Thus the individual flatpacks must often be soldered or welded into printed circuit boards in order to test system concepts. This technique is destructive since once soldered or welded into the circuit it is difficult to recover the integrated device for use in another system. NASA engineers faced with this particular problem have developed a small holder which is very similar to a door hinge. The flatpack device is placed into the holder, the hinge is closed; positive pressure is insured by two sliding clamps. These holders can be mounted in sockets and wired to provide system functions. The holder is shown in figure 13 and a breadboard system is

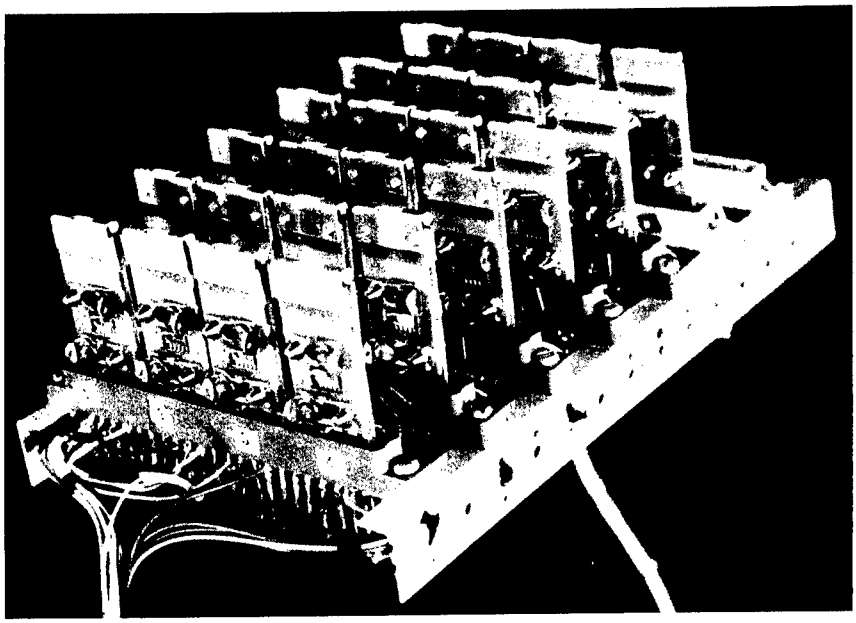


FIGURE 13.—*Flatpack holder for testing and breadboarding.*

shown in figure 14. As can be seen the devices are readily inserted into and removed from these holders without degradation and the holders themselves are relatively simple to construct. The flatpack holders have provided convenient and reliable service for their intended purpose.

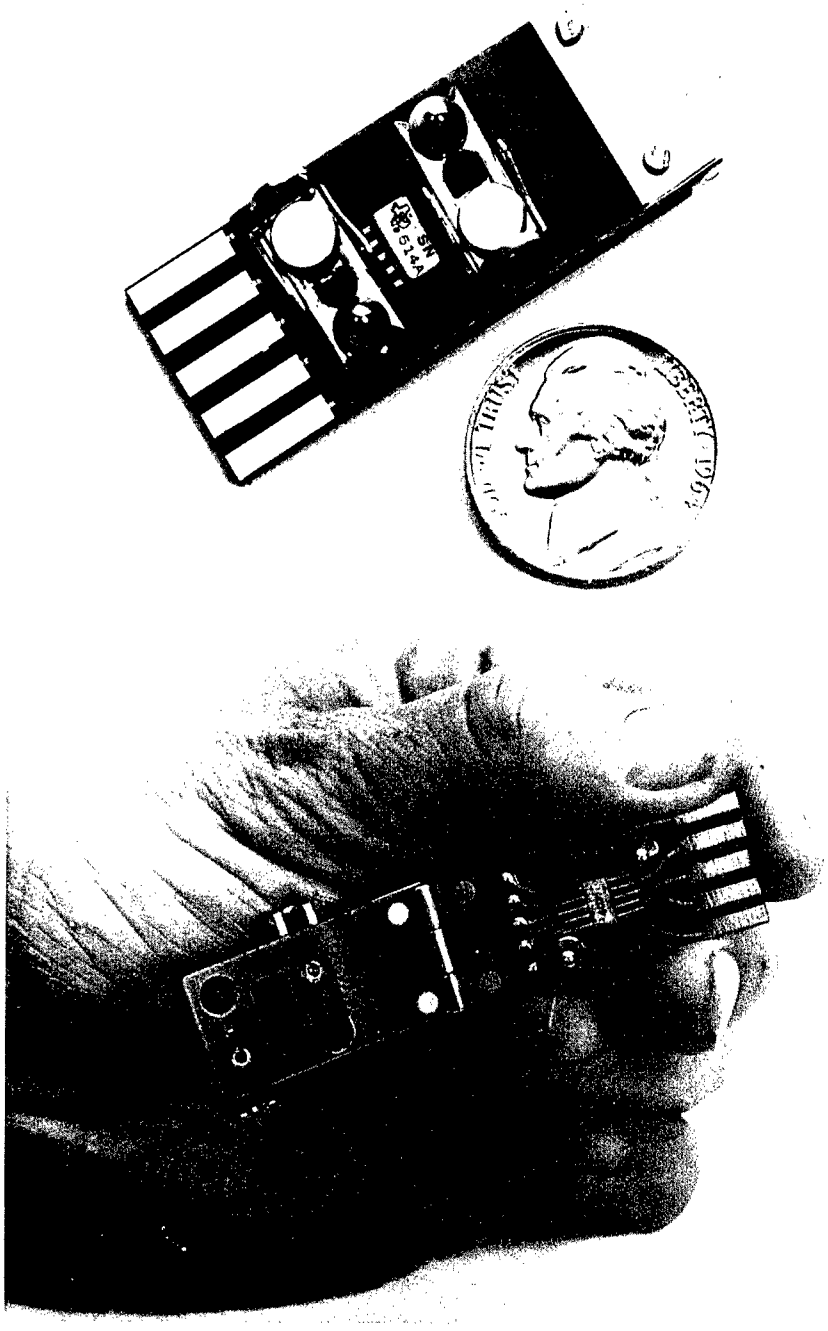


FIGURE 14.—*Breadboard of flatpack system.*

Chapter 3

Device Design and Development

PERSPECTIVE

A number of microelectronic devices have been developed by NASA and some, for which information is available, are discussed in the following sections. Several exihibit excellent temperature stability.

In support of system and equipment development, a number of microelectronic devices have been developed with NASA support. Some of these devices have been designed in NASA laboratories and fabricated by industrial organizations. Others have been designed and developed by microelectronic manufacturers in response to specific NASA requirements and with NASA support, and others have been designed, developed and fabricated within NASA Laboratories. Many of the devices which have been developed with NASA support have applications in areas other than space research and space systems, and are now being marketed for military, commercial and industrial uses.

Numerous microelectronic devices have been developed by or for NASA system suppliers for which descriptive information is not available. The particular items discussed below reflect the ease with which data have been obtainable.

Several of the amplifiers described below are interesting and impressive examples of the monolithic silicon device. Temperature stability, for example, is recognized as a limiting factor in the performance of silicon integrated devices. Yet, in a buffer amplifier discussed below, a gain is exhibited which is constant to within 0.1 percent over a 100° C temperature span. This level of temperature stability is probably greater than that obtainable in transistor type circuits and rivals even that of tube circuits. Good temperature stability is also exhibited by the dc amplifier. The demonstration of an ability to obtain extremely stable linear amplifying devices is one of the more important subjects discussed in this section.

In Chapter 5 of this report, several microelectronic devices are discussed in relation to the system for which they were built. These include the thick film circuits developed at the Langley Research Center, the multichip silicon integrated devices for the OGO data processing system, and the silicon integrated micropower devices being

developed for the record-playback system of the Tiros and Nimbus satellites. In many of the systems applications discussed, device development played an important role. It is only because limited information on these device developments is available that they are not included in this section.

BUFFER AMPLIFIER

A buffer amplifier has been designed and fabricated which exhibits a remarkable degree of temperature stability. It is a good example of how advantage can be taken of certain aspects of silicon monolithic design.

A dc amplifier designed for impedance matching and isolation purposes has been developed for the Goddard Space Flight Center. It was required to have an output impedance of less than 1000 ohms with an input impedance of greater than 10 MΩ. For negative input voltages between 0 and 6.4 V, the voltage gain was to be unity, with a zero signal dc offset voltage of less than 5 mV. This amplifier requires both a positive and negative supply, operates over a frequency range of 0 to 20 kc, and dissipates less than 20 mW of power. A preliminary commercial data sheet has been issued by Westinghouse on this amplifier (WS–119G). It is built with diffused silicon resistors on a single chip of silicon with dimensions of approximately 60 by 90 mils and is packaged in a ¼ by ⅛ inch flatpack with 14 leads.

The purpose of the buffer amplifier is to provide good isolation between the input and output. This is done by making the input resistance very high and the output resistance very low so that loading has a negligible effect on the source. A particular problem with dc amplifiers of this type is the drift in the dc characteristics of the amplifier components such as result from temperature variations. The silicon monolithic construction minimizes this problem because it results in close thermal coupling between the separate component regions. Input and output voltage equalization has also been enhanced by the similarity of input and output junctions provided by the monolithic construction.

The basic circuit for the amplifier is shown in figure 15 where Q_1 and Q_2 are n–p–n transistors with the same emitter resistance, R_1. The output from the collector of Q_1 is fed into the base of p–n–p phase inverting transistor, Q_3. The collector output of Q_3 is the output of the amplifier and is also fed back to the base of Q_2. The base-emitter voltage drops in Q_1 and Q_2 should be equal providing the base currents are equal. The input and output voltages are then identical.

Figure 16 shows a modification of the circuit which further improves the performance. Q_1 and Q_2 have been replaced by Darlington amplifiers to increase the input resistance of the amplifier. The diode,

D_1, has been placed in series with the collector resistance, R_2, in order to offset the base-emitter voltage of Q_3 and also to provide for the same

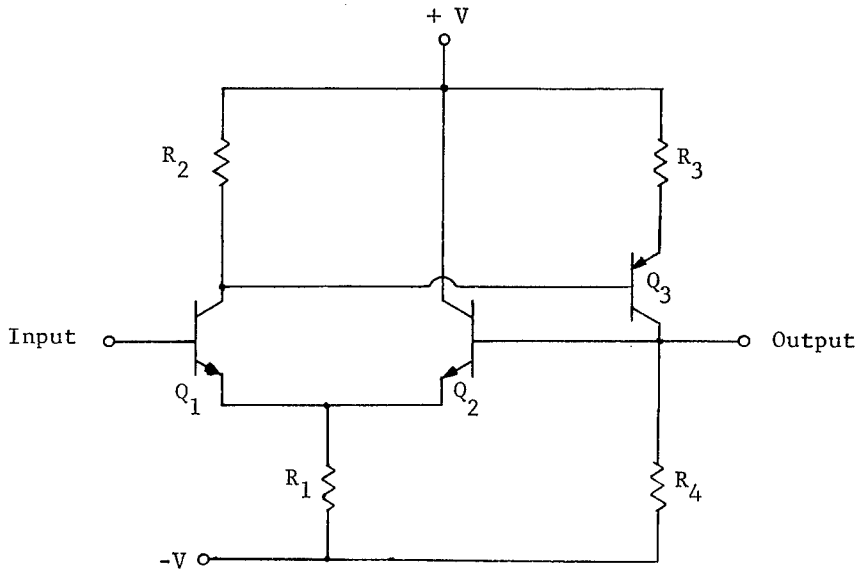


FIGURE 15.—*Basic buffer amplifier circuit.*

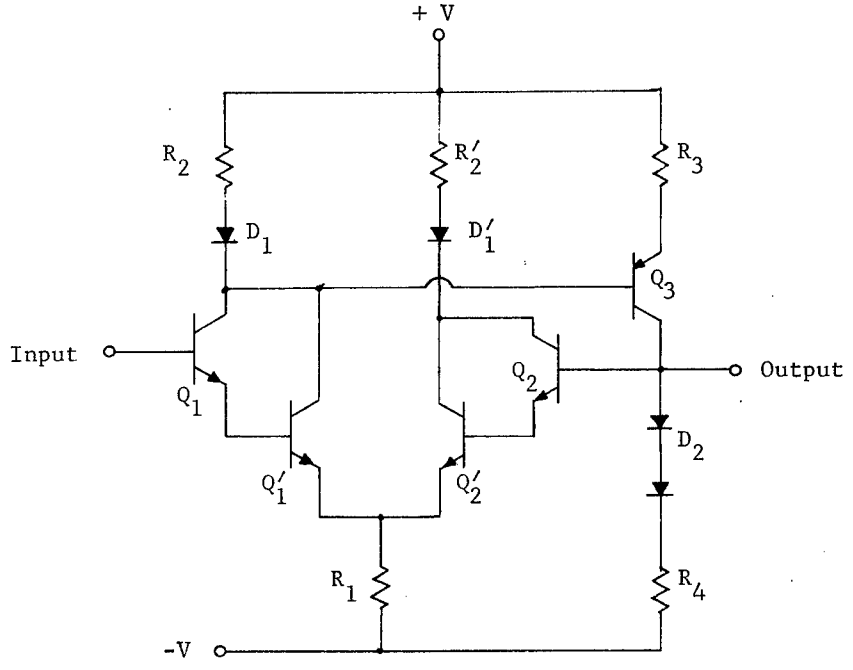


FIGURE 16.—*Improved buffer amplifier.*

temperature dependence of this voltage. The double diode structure, D_2, in series with R_4 is used to provide both voltage compensation and temperature compensation for the equivalent emitter junctions of Q_2 and Q'_2. The dc currents and voltages in the amplifier circuit are by these means carefully balanced in order to achieve identical input and output voltage levels. The input impedance of the amplifier is essentially R_1 multiplied by twice the effective current gain of the input Darlington stage. The output impedance is lower than the value of R_4 because of the negative feedback action of R_1.

The topology of this silicon monolithic amplifier is shown in figure 17. Particular design features include the fabrication of both n–p–n and p–n–p transistors on the same substrate, the use of temperature compensating diodes for both transistor types, an adjustable resistor, and the lateral structure of the p–n–p transistor. In order to allow fabrication of all of these on the common substrate, it is necessary to form epitaxial layers of two different resistivities on the p-type substrate and to perform three diffusions. The first diffusion is deep p-type for the purpose of isolating the respective component regions of the structure; the second diffusion, which is also p-type, forms the diffused resistor regions, the p-type base of the n–p–n transistors, and both the collector and emitter regions of the lateral p–n–p transistor; and the last diffusion, n^+, forms the n–p–n transistor emitter, the n–p–n transistor collector contact, and the p–n–p transistor base contact. In the topology of figure 17 it is seen that the diode D_2 is actually in the form of a Darlington transistor pair with collector and base shorted. This is to provide close temperature compensation of the equivalent Darlington transistor pairs Q_1 and Q_2. Similarly the diodes D_1 and D'_1 are designed to have similar junctions to that of the emitter of the p–n–p transistor with the actual area and peripheral dimensions being proportional to the relative current densities. As shown, the small incremental resistors, R'_4, are for the purpose of adjusting the value of R_4 after preliminary testing of the device. Each incremental resistance is approximately 1000 ohms, allowing adjustment of R_4 total from 38 k to 28 k in 1 k increments. The circular pattern of the lateral p–n–p transistor is noted. In order to provide sufficient gain for this structure, it is provided with an n–p–n transistor to obtain a composite gain of something greater than unity.

An initial performance evaluation showed no significant difference between an amplifier built using deposited thin film resistors and one using diffused silicon resistors. The design met all specifications; however, in initial samples, variations of the offset voltage with temperature were excessive. More careful processing control resulted in higher gain p–n–p transistors and a decrease of the temperature sensitivity of the offset voltage.

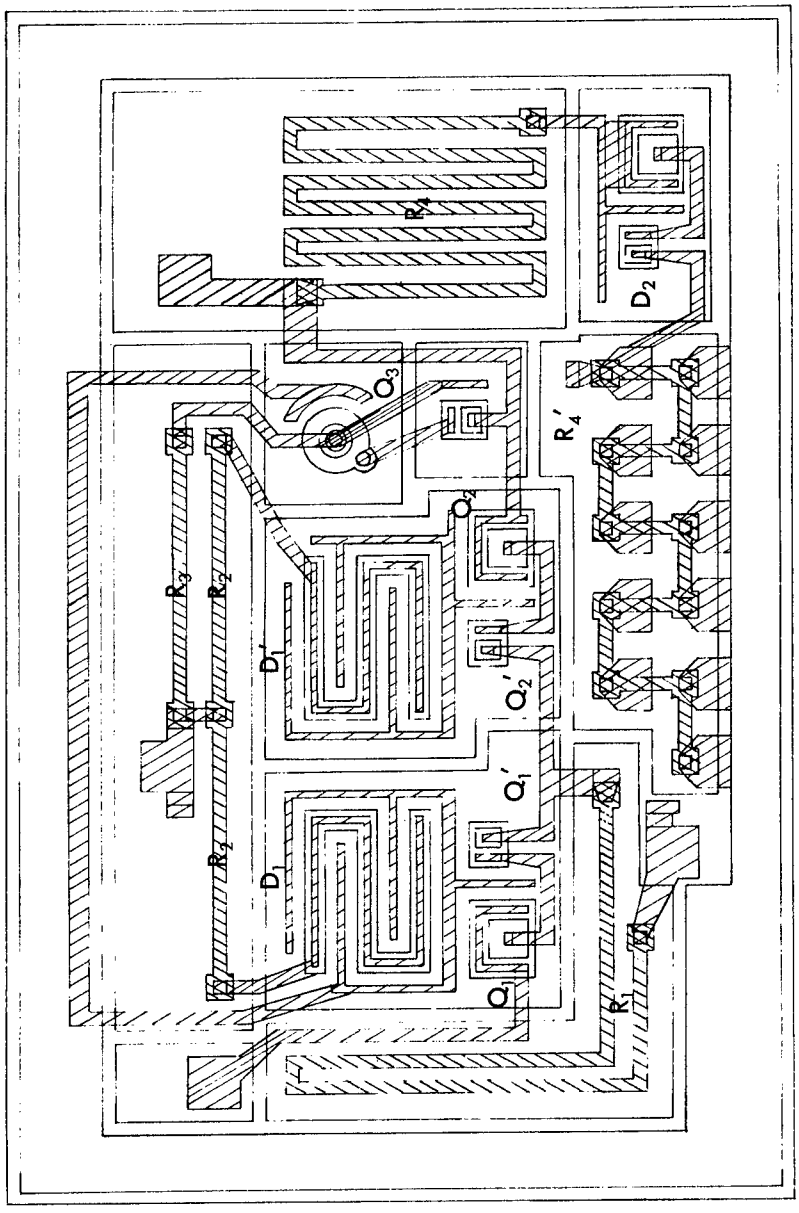


FIGURE 17.—*Topology of buffer amplifier.*

Evaluation of these units shows that objectives have been met. Of 15 delivered units, a typical input impedance was 32 megohms with all units exceeding the required minimum of 10 megohms. The output impedance was typically 300 ohms with all units below the maximum 1000 ohms specification. The offset voltage requirements for the buffer amplifier have essentially been met with the largest offset observed being 6.8 millivolts with an input to the amplifier of 6.4 volts and at an ambient temperature of 90° C. It is expected that this performance will be improved as processing refinements are made.

In summary, a successful buffer amplifier has been designed and fabricated which exhibits a remarkable degree of temperature stability for a dc amplifier. This temperature stability is extremely difficult, if not impossible, to obtain using conventional circuit design techniques and components. This microelectronic device is a good example of how one can take advantage of certain unique aspects of the silicon monolithic design to realize enhanced performance over comparable conventional circuits.

AN INTEGRATED ANALOG SWITCH

This bi-directional switch consists of a single transistor and its drive circuit. The on-off impedance ratio is greater than 10^7 and it provides good isolation between the control and signal voltages which have a common ground.

A bi-directional analog switch designed for the Goddard Space Flight Center has been fabricated into a single monolithic silicon block and encapsulated in a 14 lead $\frac{1}{4}'' \times \frac{1}{8}''$ flatpack.[1] This analog switch is to be used in satellite telemetry systems to time multiplex data. Power dissipation, volume, weight, and reliability are of primary interest. The analog switch met all design objectives except for desired speed and input loading characteristics. The failure to meet all requirements is probably due to limitations in the circuit design.

The electrical circuit of the analog switch is shown in figure 18. Transistor Q_A is the switch, and the remaining components make up the control circuitry that drives Q_A either "ON" or "OFF." Transistor Q_A is the switch and is operated in the inverted mode for a lower offset voltage. When Q_N in figure 18 is driven into saturation by a positive control voltage, the potential at point M is about 0.2 volt and the potential at point N is fixed at about 1.4 volts by the forward biased D_2 and Q_P base-emitter junction. A constant current generator is thus formed by the potential difference between the supply voltage and the voltage at point N divided by resistor R_4. This generator supplies base current to Q_A causing it to turn "ON," and through R_5 swamping out the effect of the $-V$ potential.

[1] Westinghouse Electric Corporation, NASA Contract NAS5-3764.

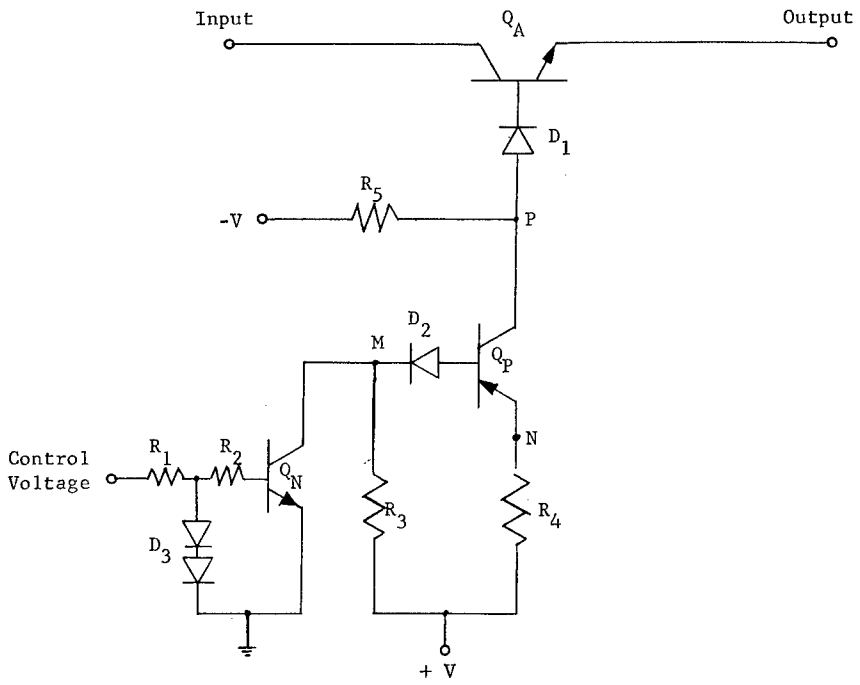


FIGURE 18.—*Analog switch circuit.*

In the absence of a control signal, the collector-emitter circuits of Q_N and, consequently, Q_P are open circuited. Consequently, the negative potential, $-V$, can reverse bias D_1 and the base-emitter junction of Q_A. Diode D_1 reduces the reverse bias applied to Q_A.

The design of this switch provides for controlling the base current in Q_A during the "ON" period such that the switch is just in saturation for a given controlled (collector) current, thus minimizing the opening (storage) time. It also provides for reverse biasing Q_A during the "OFF" period to minimize any current leakage through the open switch.

The analog circuit was designed to meet the following requirements:

1. Offset voltage between output and input less than ± 2 mV over the operating temperature.
2. Analog signal voltage from 0 to -6.4 V from a low impedance source of less than 1 kilohm.
3. A positive control voltage of 4 ± 2 V for the "ON" condition and 0 ± 0.5 V for the "OFF" condition.
4. A control signal frequency from dc to 50 kc.
5. Operating temperature range from $-5°$ C to $+80°$ C and a storage temperature range from $-65°$ C to $+150°$ C.

6. Capability of driving a load of greater than 2 megohms and a shunt capacitance of less than 100 pf.
7. "OFF" impedance greater than 100 megohms.
8. "ON" impedance less than 1000 ohms.
9. Power dissipation less than 5 mW for a 50 percent duty cycle.

Electrical tests given below on the completed analog switch show results close to the design goals.

1. Forward and Reverse Current Gain
   The worst case values of the forward and reverse current gain of Q_A were 50 and 15 respectively. These values are well within the requirements and yield a worst case offset voltage of 1.065 mV.
2. Breakdown Voltage BV_{CEO}.
   The value of the open base collector-to-emitter breakdown voltage BV_{CEO} was about eight volts and is adequate because the signal voltage lies between 0 and -6.4 V.
3. Temperature Effect
   The offset voltage of all switches tested was almost constant over the operating temperature range with a maximum variation of 0.2 mV for a signal voltage of -4 V.
4. "ON" and "OFF" Impedances
   The dynamic "ON" impedance of the gate is about 50 ohms and is practically constant over the temperature range. The dc incremental "OFF" impedance is above 1000 megohms.
5. Loading
   The offset voltage of the signal source is seriously affected by the loading of the analog gate. This is due to the large base current needed to drive the low-offset transistor into deep saturation to insure a low dynamic resistance.
6. Speed
   The turn-on time of six microseconds for the present gate is slower than desired. This is due to the large junction capacitance formed in both the emitter-base and collector-base junctions of the analog gate because of its large junction area. The turn-on time of six microseconds seems reasonable if the capacitance of the emitter-base and collector-base junctions, the stray capacitance and the charging time of the rest of the circuit is considered.
7. Power Dissipation
   The power drain when the gate is "ON" is less than 8 mW and is zero when the gate is "OFF." Therefore, for 50 percent duty cycle operation, the average power dissipation is less than 4 mW.

The analog switch, except for the turn-on time and the loading effect, is successful in obtaining the required performance. The limitations are believed to be due to the problems in the circuit design.

The topology of the analog switch is shown in figure 19 and some details of the unique analog switch transistor structure are shown in figure 20. It is noted that in order to obtain comparable forward and reverse gains in the switching transistor an annular design for the emitter and base was employed. This gives comparable active areas for both the collector junction and emitter junction. On this silicon monolithic structure, a p–n–p transistor was formed using compatible processing techniques. The design of the p–n–p structure is circular with minority carrier transport between the emitter and collector flowing parallel to the surface in contrast to normal transistor design wherein it flows perpendicular to the surface. This lateral transistor design normally exhibits a low grounded emitter current gain, i.e., on the order of one or less, but in applications such as the switch driving circuit where gain is not important the ability to fabricate a p–n–p transistor structure which is compatible with the n–p–n transistors is important for ease of circuit design. Other aspects of the silicon device topology are conventional. Two of the 50×60 mil silicon chip analog switches are packaged in 1 integrated circuit flatpack with 14 leads. A preliminary data sheet, WS–120G, has been issued on this device.

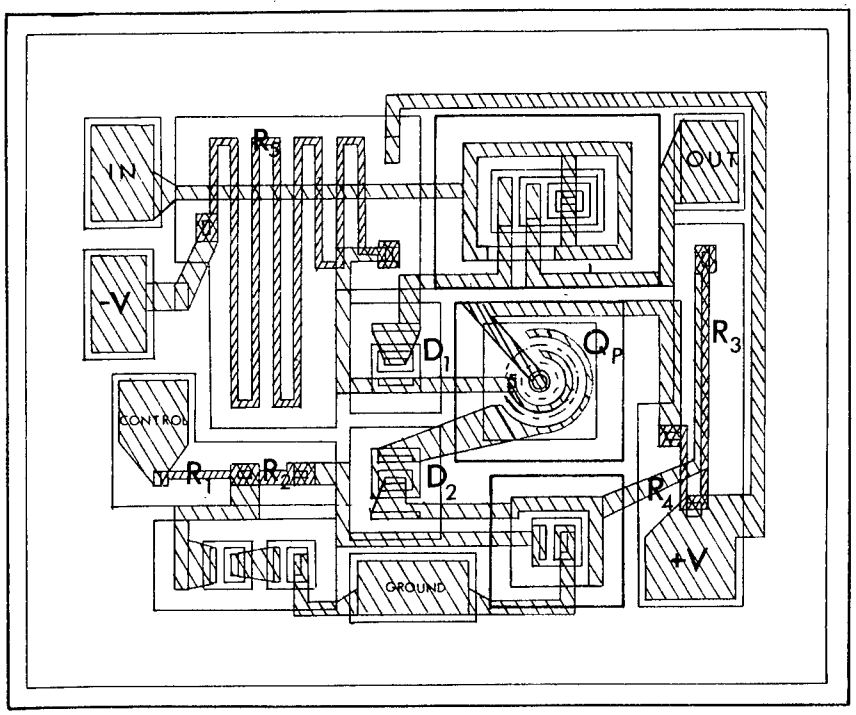


FIGURE 19.—*Topology of analog switch.*

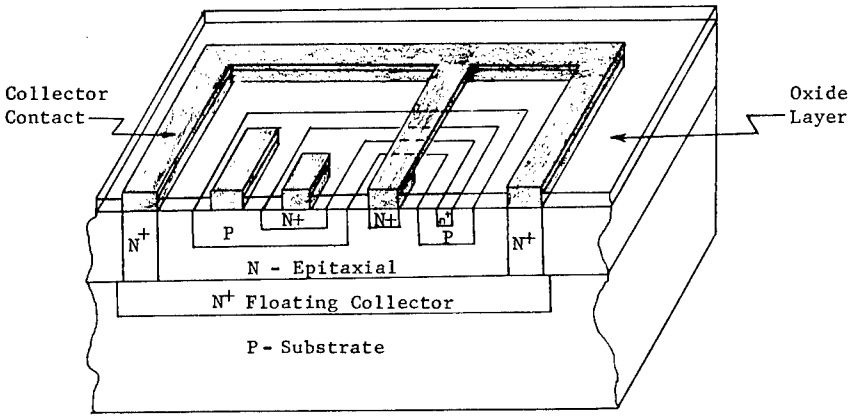


FIGURE 20.—*Analog switch transistor structure.*

The novelty of the analog gate is the bidirectional transistor having a foward common-emitter current gain of 50–100 and a reverse common-emitter current gain of 15–30, achieving a typical offset voltage of 1 mV.

INTEGRATED LOW-LEVEL DC DIFFERENTIAL AMPLIFIER

This integrated silicon dc amplifier has a typical voltage gain increase from 247 to 256 over a temperature span of 100° C. Many applications in medical electronics and other sensing and control systems are believed to exist.

An integrated low-level dc differential amplifier having unique features has been designed by the Langley Research Center.[2] The amplifier was designed to provide a constant voltage gain over a wide temperature range, a high input impedance, and a single-ended dc output voltage. Specific requirements are given in table VI for the monolithic single chip structure. Figure 21 shows the amplifier schematic and figure 22 shows the completed monolithic chip.

Measurements were made of input and output voltage characteristics at four temperatures to determine the voltage gain as a function of temperature using a test circuit with variable source resistances and dc input voltage. A typical voltage gain vs temperature curve for the amplifiers tested is shown in figure 23. There is a gradual increase in gain as the temperature increases. This is caused by the dependence of the open loop voltage gain on the transistor current gain (h_{fe}). An increase in temperature causes h_{fe} to increase, leading to a general increase in the closed loop voltage gain. The variation of the feedback factor, β, with temperature is usually negligible compared to the vari-

[2] This unit was fabricated and tested by Westinghouse Electric Corporation Molecular Electronics Division under NASA contract NAS1–3321.

ation of h_{fe} with temperature. However, the use of thin-film resistors would minimize any variation of β since the temperature coefficient of resistance of thin-film resistors is an order of magnitude less than that of diffused resistors. The thin-film resistances can be deposited on top of the oxide of a semiconductor functional structure.

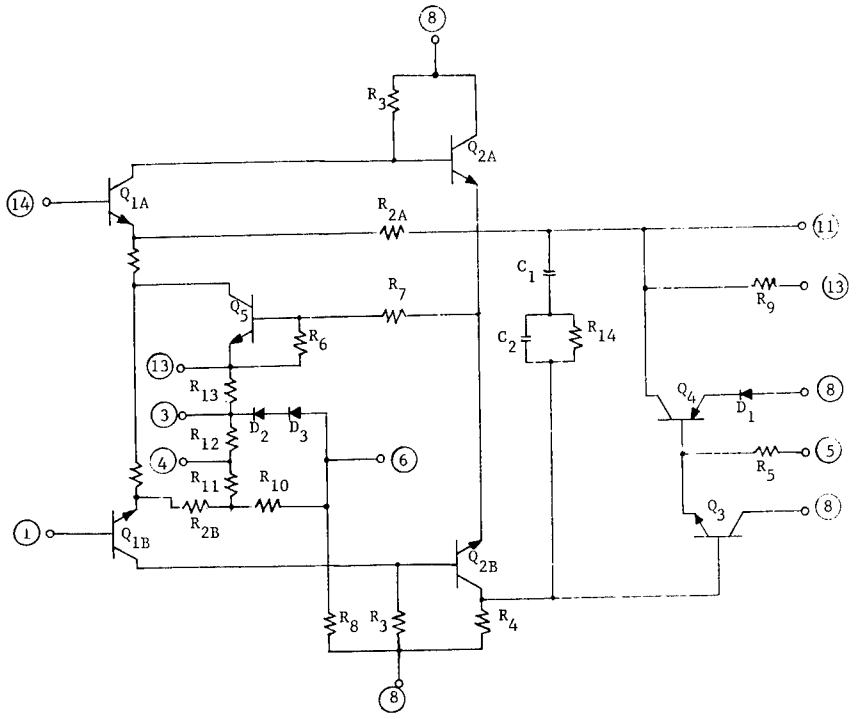
TABLE VI.—*DC Amplifier Specifications*

Differential input range, mV	0 to 20
Output range, V	0 to 5
Gain	250
Gain stability, percent	0.5
Initial offset, V	−0 to 0.5
Zero drift (24 hours), V	±0.2
Linearity, percent	0.1
Input impedance, ohms	150,000
Output impedance, ohms	500
Common-mode rejection:	
DC with no line unbalance	10^5
DC with 200 ohms unbalance	10^4
1000 cycles with no unbalance	10^4
Maximum common-mode voltage, V	±1
Power-supply voltages, V	12; −6
Power-supply variations, percent	±10
Bandwidth (3 db), kc	80
RMS output noise level (input shorted), mV	10
Operating temperature range, ° C	−10 to +85

Design features of the amplifier include:

1. Constant Gain—A nearly constant gain is obtained by using a built-in negative feedback consisting of a voltage divider made of diffused resistors.
2. High Input Impedance—The differential input impedance of this amplifier is obtained with a series negative feedback. The input impedance which is greater than 150 kΩ is larger than that of other integrated differential amplifiers.
3. Single-Ended Zero dc Output Voltage—With no input, a zero dc voltage is obtained at the output terminal by the use of complementary transistors, negative feedback, and matched input transistors. The drift, or offset voltage as referred to the input, is less than 10 μ V/° C in all of the units tested. The complementary p–n–p transistor is fabricated simultaneously with the n–p–n transistor requiring no extra processing steps.
4. Linearity—The improved linearity over previous monolithic units is due to the built-in negative feedback.

The development and fabrication of this differential amplifier represents an improvement over previous integrated units and the amplifier obtained is better than discrete component circuits in many respects.



Pin Connections

1. Input A (Non-inverting)	6. No Connection
3. No Connection	8. Positive Supply Voltage
4. No Connection	13. Negative Supply Voltage
5. Common	14. Input B (Inverting)

FIGURE 21.—*DC amplifier circuit.*

Differential amplifiers, with a basic requirement for matching of transistors and resistors, are nearly ideal for fabrication as a monolithic functional block. The matching of characteristics in the block is insured by the uniformity of temperature in the structure and by the simultaneous fabrication of the complementary component. The ease of matching in the monolith makes it possible for the amplifier to out-perform a discrete component circuit. An oven to maintain a constant temperature and a careful selection of components would be required if the discrete component circuit were to match the monolithic structure in performance.

While the designed amplifier surpasses previous models in performance, the variation of 1.5 percent noted in the voltage gain over the temperature range is larger than had been hoped for. This variation in gain is due to the low open-loop gain, A, the variation of current gain, h_{fe}, with temperature, and to a much lesser extent, the variation

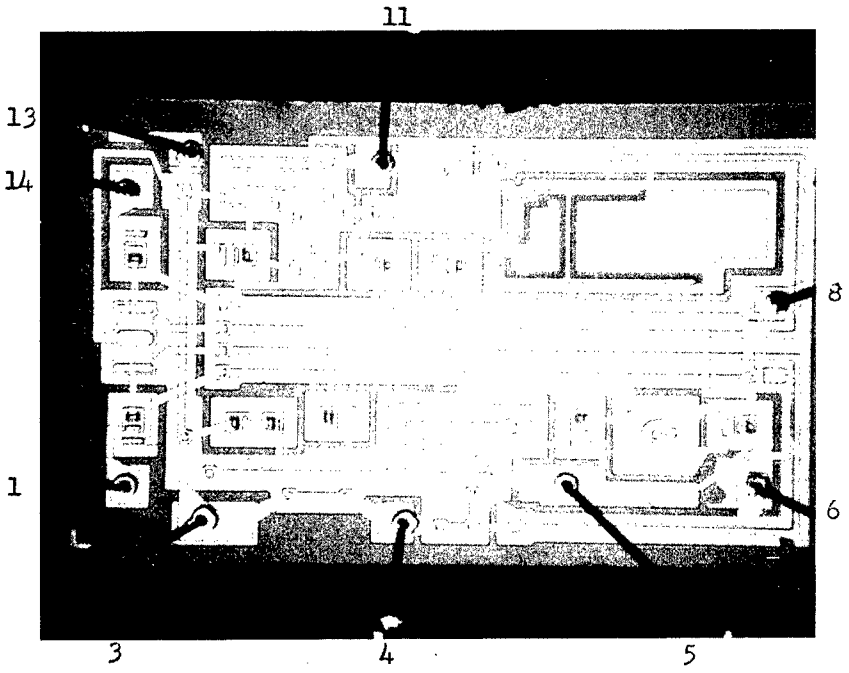


FIGURE 22.—*Differential amplifier chip.*

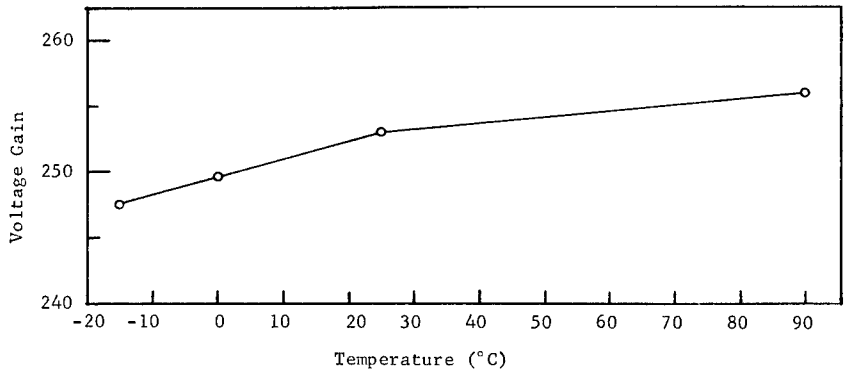


FIGURE 23.—*Temperature dependence of dc amplifier gain.*

in feedback factor, β, with temperature. Any additional investigations to improve the design of this model should concentrate on these areas. The increase of the open loop gain without causing instability and the application of local feedback to individual stages to stabilize the current gain would be particularly significant improvements. Tentative specifications on this amplifier have been issued by Westinghouse as WS 123.

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DC COMPARATOR

This circuit gives an output which is a digital coded representation of the input voltage level to an accuracy of about 2 percent. It therefore functions as a voltage measuring circuit. Applications include A/D conversion for telemetry and other instrumentation systems.

One form of analog to digital conversion for telemetry application utilizes a successive approximation method of conversion. With this method, the unknown voltage representing an analog quantity is compared successively to known voltages in a comparator circuit. If the known voltage exceeds that of the unknown, the circuit produces an output of sufficient amplitude to perform a logic function. Such a comparator circuit was fabricated as a multichip silicon integrated circuit by Motorola for the Langley Research Center for use in an A/D converter. Other portions of the A/D converter are discussed in "Interrogation, Recording and Location (IRL) Subsystem," Chapter 5.

The circuit for the dc comparator is shown in figure 24. The input voltage to the comparator varies between 0 and 5 V, and the known reference voltage for the comparator circuit is generated by a so-called ladder-adder network. The comparator is a differential amplifier which indicates when the ladder-adder voltage is greater than the unknown voltage input. Under these conditions, the comparator produces an output which removes the ladder-adder voltage from the comparator. Successively smaller ladder-adder voltages are compared to the input signal and the sum of all those which are not rejected indicates the magnitude of the input voltage. This is automatically coded for the telemetry system. Using this method it is only necessary to try 6 voltage values in order to determine the input voltage level to within 2 percent of full scale.

In the comparator circuit it is necessary to have two transistors with matched I_{CBO} and V_{BE} parameters. It is also important that these parameters track accurately as the temperature varies. An initial step toward realization of a comparator circuit was obtaining well matched transistors packaged in an integrated circuit flatpack for use in thick film circuits. The later version of the comparator circuit has been fabricated in multichip silicon form by Motorola and packaged in a TO–5 header. Advantage is taken of the versatility of the multichip integrated circuit approach in that both p–n–p and n–p–n transistors are used. Symmetric two-stage dc amplifiers accept the input and reference voltage and a transistor senses when the reference voltage exceeds the input voltage.

The important characteristics of this comparator circuit are as follows. The differential input resistance is 5000 ohms while the common-mode input resistance is 500 000 ohms. In order to obtain an

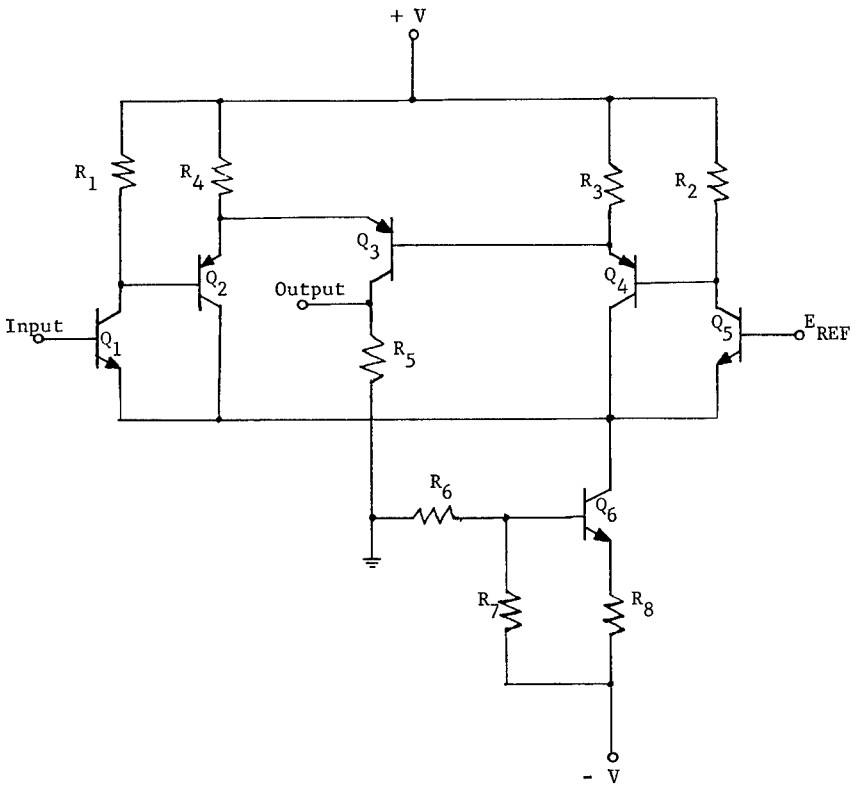


FIGURE 24.—*DC comparator circuit.*

output the reference voltage must exceed the input voltage by an amount which is the sum of an offset voltage and the voltage transition width. The maximum values for these in the circuit developed are 14 millivolts and 5 millivolts respectively. The output resistance of the comparator is in the vicinity of 8000 ohms and the bandwidth is 50 kilocycles. Two power supplies are required, one at about $+9\frac{1}{2}$ V and the other at -3 V. A 6 V output signal is available and the total power dissipation of this device is 30 milliwatts maximum.

The fabrication of this circuit was successful and it is now available as the MC 1514.

INTEGRATED INSTRUMENTATION AMPLIFIER [3]

This amplifier design has been proposed for implementation in silicon integrated form because of its high stable voltage gain independent of parameter values. It has not been fabricated.

[3] Kleinberg, L. L., Goddard Space Flight Center.

A novel design for an integrated instrumentation amplifier has been developed and tested. It is attributed with a very high stable gain which is practically independent of the resistor and transistor parameters included in the structure. The circuit for this amplifier is shown in figure 25. No parameter values are given, but they can be determined by the supply voltage and characteristics of the transistors. This amplifier has a low power consumption and will operate reliably with large variations in the component parameters. Among its applications are use as an electronically controlled variable gain amplifier capable of modulating a carrier.

The design of the amplifier is based upon a large open loop gain with a negative feedback loop. The net voltage gain may be on the order of 2000. In the circuit as shown in figure 25, the output of the amplifier is at the terminal indicated E_o. Feedback voltage is developed across the common emitter resistor R_5, is reduced to a dc level by filtering with capacitor C, and develops a bias train through R_B to the input of the amplifier. Dependent upon the particular frequency for which the amplifier is designed, it may be that capacitor C would be an external component. The rest of the circuit consists of resistors and transistors and should readily be realizable either as a silicon monolithic circuit or by any of the other microelectronic technologies. The unique freedom from specific component parameters would make this amplifier very easy to fabricate. Neglecting frequency considerations it would be expected that the only important considerations are that the transistors have a reasonably high voltage gain.

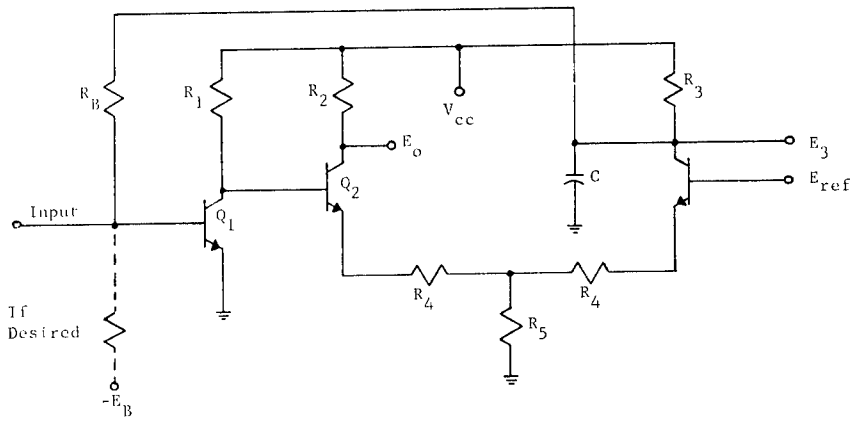


FIGURE 25.—*Proposed integrated instrumentation amplifier circuit.*

STATIC INVERTER PREAMPLIFIER AND POWER AMPLIFIER

Most silicon integrated devices operate at levels below 100 mW. Two device types which are being developed for a power supply application are high power devices delivering 1 A and 10 A respectively. These require different packaging techniques from the low power structures.

A microelectronic preamplifier and power amplifier for use in the static inverter described in Chapter 5 are being developed by Westinghouse for the George C. Marshall Space Flight Center.

The present preamplifier circuit used in the static inverter is shown in figure 26. The circuit diagram and topology for its integrated substitute is shown in figure 27. The input signal for the integrated device is four volts at five milliamperes taken from a TI SN511 solid circuit. The output required to drive the static inverter power amplifier is one ampere over the temperature range −55° C to +125° C. The emitter to collector breakdown voltage of the preamplifier transistors is 9 to 12 Volts. This device is fabricated in one chip of silicon and is packaged in a modified flatpack. Test data on seven of these units given in table VII show that all requirements have been met. A photograph of the package design is shown in figure 28.

The circuit diagram for the integrated power amplifier is shown in figure 29. The diodes indicated are presently being fabricated on separate small silicon chips included in the same package with the rest of the unit. The dc supply for the power amplifier is 28 volts, and an output of 10 amperes is required for a 1 ampere drive. The drop across the transistor is not to exceed 1 volt. The turn-on time is about 6 microseconds, and the storage plus fall time must be less than 20 microseconds. Operating temperature is from −55° C to +150° C. A photograph of this power unit, now under development, is shown in figure 30, together with a proposed package.

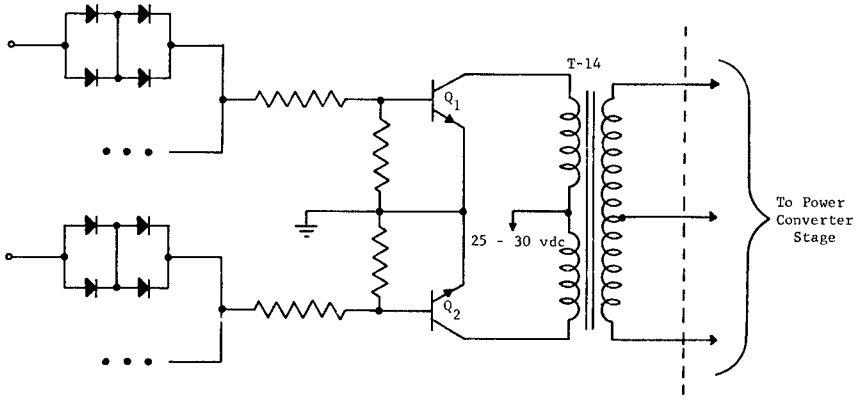
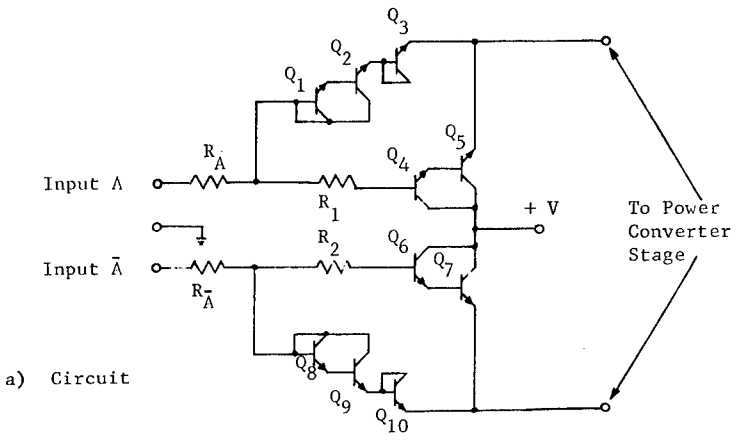
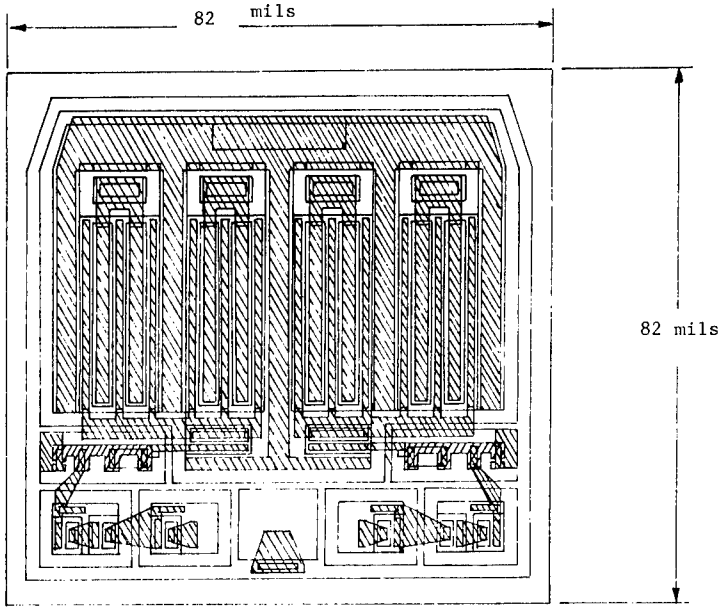


FIGURE 26.—*Conventional preamplifier circuit.*



a) Circuit



b) Topology

FIGURE 27.—*Integrated static inverter preamplifier.*

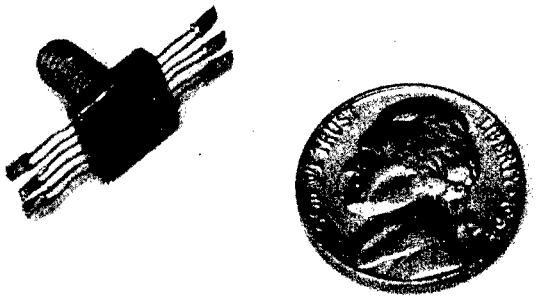


FIGURE 28.—*Proposed preamplifier package.*

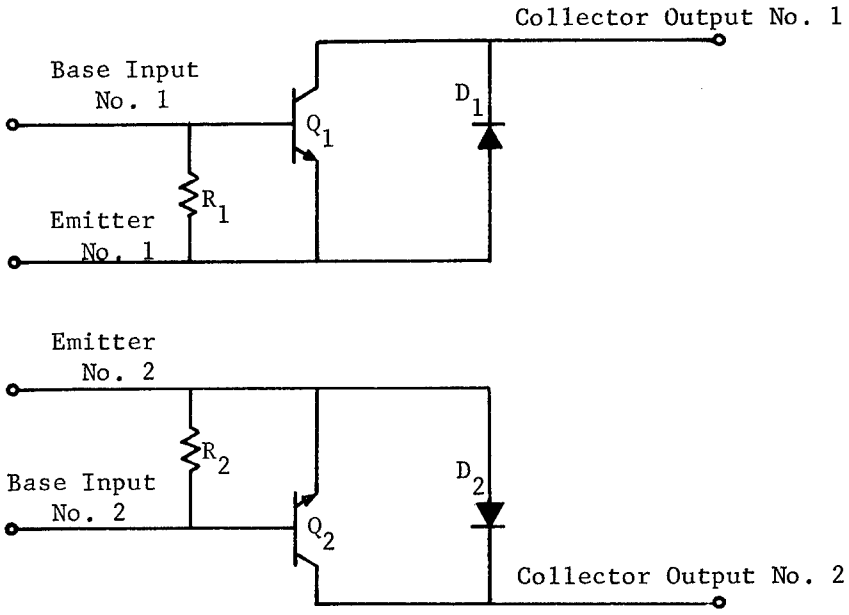


FIGURE 29.—*Circuit of integrated power amplifier.*

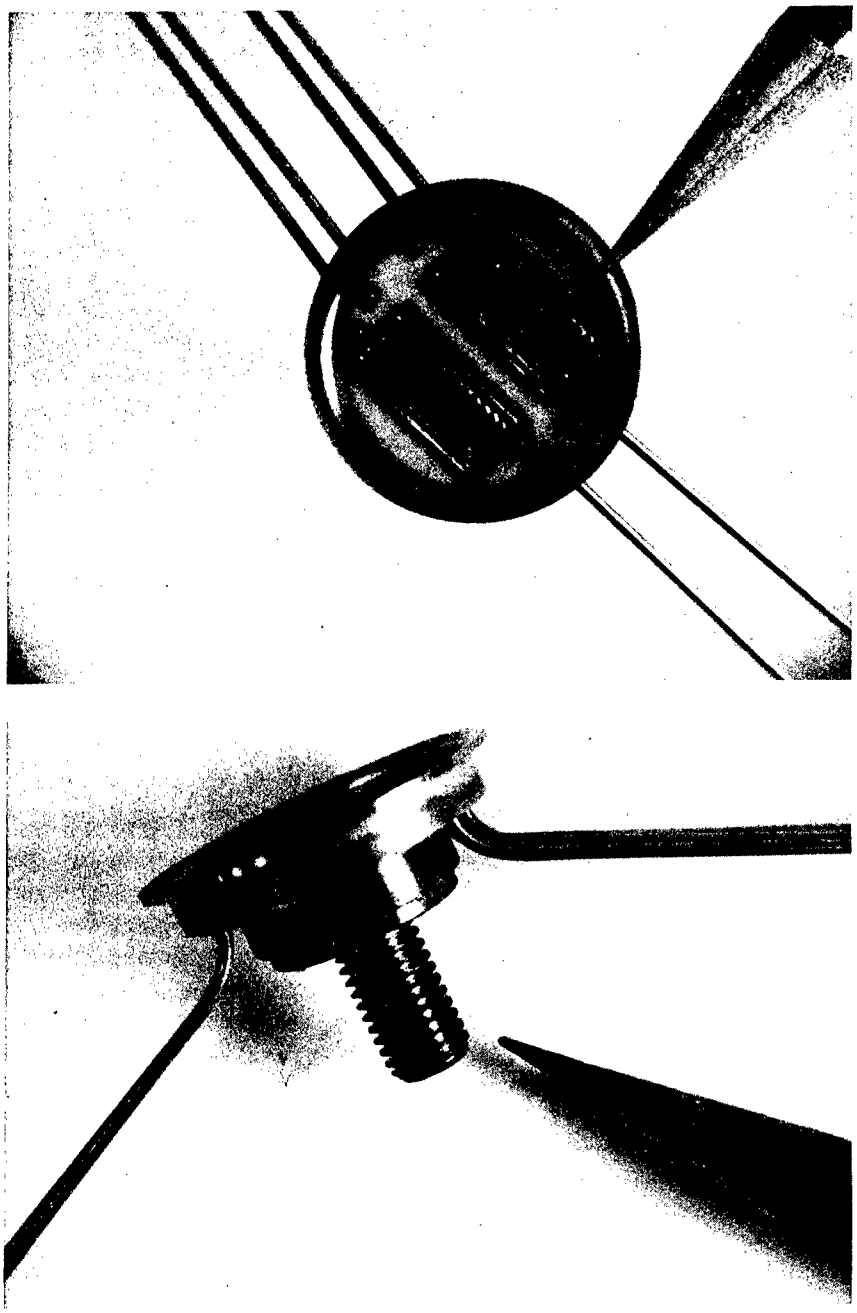


FIGURE 30.—*Dual power amplifier and proposed mounting package.*

TABLE VII.—*Test Data on Preamplifiers*

V_{in}	T (° C)	I_{out} (amp)	t_r (μsec)	t_f (μsec)	No. of measurements
3. 0	25	1. 0–1. 5	. 22–. 28	. 16–. 20	12
3. 0	−55	0. 8–1. 0	. 22–. 32	. 18–. 20	12*
3. 0	125	0. 9	. 22–. 24	. 18–. 20	2
3. 5	25	1. 2–1. 7	. 24–. 34	. 18–. 24	12*
3. 5	−55	0. 9–1. 3	. 22–. 28	. 18–. 20	12
3. 5	125	1. 0	. 24	. 20	2

*Only 3 measurements of time parameters.

INTEGRATED MICROPOWER CIRCUITS

Low power logic circuits are important for space research. This study indicates that, at low speeds, a complementary RDTL logic performs best, with DTL being better at higher speeds.

A study program has been conducted for the Langley Research Center [4] to provide a guide for the design of integrated low power logic circuits. Maximum resistance, propagation time, and power drain at frequencies below 150 kc were studied for the logic circuits considered. This program was initiated because of a lack of knowledge regarding micropower logic circuits and the need for such circuits in spacecraft and other applications where power consumption is of vital importance.

Seven basic logic circuits were studied. They were Direct Coupled Transistor Logic (DCTL), Resistor-Transistor Logic (RTL), Resistor-Diode-Transistor Logic (RDTL), Emitter Coupled Transistor Logic (ECTL), Transistor-Transistor Logic (TTL), Diode-Transistor Logic (DTL), and Complementary RDTL. The power drain capabilities of each circuit were considered as a function of fan-out and fan-in, switching speed, available spacecraft voltages, radiation damage, logic levels and operating temperature.

The comparative performance of each circuit regarding power drain and propagation time was made using worst-case design criteria. The most promising circuits were then tested thoroughly for temperature and load characteristics. The circuit configurations investigated were NAND and NOR gates, a universal flip-flop, and other applications utilizing flip-flops as shift accumulators. Circuits were tested over a temperature range from −55° C to +125° C.

[4] Sperry Semiconductor Division of Sperry Rand Corporation, NASA Contract NAS1–2619.

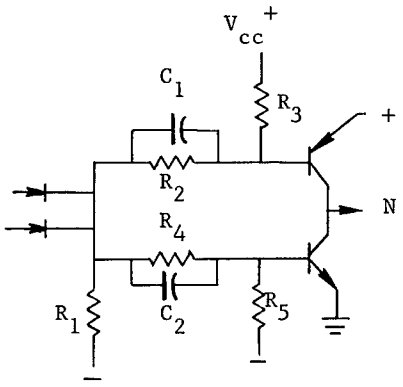
Five gates for each configuration were built and connected in a closed loop to form a ring oscillator. Power drain and propagation time for each oscillator stage were used as the performance parameters. The results obtained easily eliminated RTL, DCTL, and RDTL from further consideration. RTL showed excessive power drain and DCTL was subject to current "hogging." RDTL must be operated at low voltages to obtain acceptable results, making it sensitive to resistor and transistor beta variations. ECTL showed no improvement over DTL, and it is more difficult to design in the gate and flip-flop configuration. Therefore, it was also eliminated from further consideration.

The three circuits investigated in more detail, Complementary RDTL, DTL, and TTL, are shown schematically in figure 31.

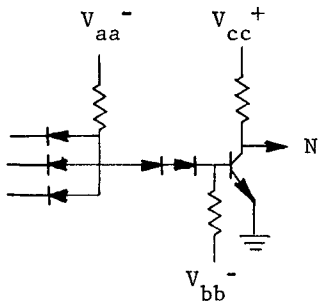
Further investigation showed that the TTL circuits exhibited the most consistent performance characteristics over the temperature range. However, general system performance must be considered in addition to individual circuit performance and the TTL configuration has certain disadvantages. The complementing flip-flop is complex for the TTL circuit, requiring the equivalent of eight gates. Power drain is, consequently, high. This results from the small voltage swing of the gate which prohibits the use of ac steering. TTL is also more noise susceptible than other configurations because of the small turn-off voltage of the transistor base. Noise susceptibility also tends to be increased by the active gating elements because of the lack of a current limiting resistance element. The turn-off voltage decreases with increasing temperature and the gate transistor requires a low offset voltage and a low inverse beta to minimize the turn-off voltage problem and prevent large reductions in base currents. These two requirements are difficult to obtain in the same device. Therefore, it is felt that the advantage of low power drain for TTL is outweighed by the inherent disadvantages in general system use.

Both DTL and Complementary RDTL permit ac coupled flip-flops because of larger output voltage swings. Satisfactory performance for DTL flip-flop operation over the temperature range is attained only by increasing the collector supply voltage, thereby increasing the power gain. NAND and NOR gates are not directly available in the basic DTL configuration. While flip-flops using ac steering are possible, their performance over a wide temperature range is poor.

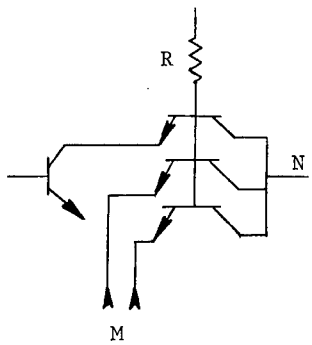
The complementary RDTL configuration has the advantage of permitting NAND and NOR gates to be easily fabricated with similar design and performance characteristics. Additional NAND and NOR gates can be driven simultaneously, permitting greater design flexibility. Speedup of waveform fall time is obtained by transistors



a) CRDTL



b) DTL



c) TTL

FIGURE 31.—*Micropower logic circuit types.*

switching on for each logic level, thereby improving switching speeds. The worst case propagation time is degraded at high temperatures, although not as badly as DTL. Noise immunity is better than in the TTL, and turn off voltage is about half way between the values obtained with DTL and TTL. Complementary pair transistor beta requirements are slightly higher, but are not prohibitive.

The complementary RDTL flip-flop is not as complex as two gates and a considerable reduction in power drain is obtained over the other flip-flops considered. Also, ac set and reset features are possible, and a shift accumulator is available. Considering circuit and system performance, complementary micropower RDTL seems to offer the best performance characteristics. At operating frequencies around 200 kc, DTL begins to gain in performance trade-offs with complementary RDTL and at higher operating frequencies, DTL is probably the better of the two logic circuits.

The state-of-the-art in single-chip integrated circuits is not consistent with the requirements of high beta, low current n–p–n and p–n–p transistors. Multichip circuits are possible and initial plans call for the NAND and NOR gates to be fabricated using a maximum of three chips per gate. The flip-flops will employ a maximum of six chips.

SHORT REPORTS

Additional shorter descriptions of devices and device activities are given in the following paragraphs.

THIN FILM ACTIVE DEVICE RESEARCH

The Office of Advanced Research and Technology of NASA has provided support for research on thin film active devices. This research has been conducted by the Harry Diamond Laboratory, Philco, and General Electric. The objectives of this research have been to develop active thin-film triode devices which depend upon tunneling for gain and to fabricate metal-insulator-metal sandwich structures which operate as tunnel cathodes for electron emission. In these research efforts much has been learned about the technology of preparing structures of these types, and a variety of structures have been characterized. A number of advantages for such structures, if they are practical, can be listed. The research efforts undertaken have also reviewed many limitations upon these devices. Portions of these studies are continuing, and further studies are necessary in order to fully determine practicality.

THIN FILM FLIP-FLOP

As part of the development of the Nimbus and Tiros telemetry systems, a thin film flip-flop was investigated by the Goddard Space Flight Center. The conclusions from this effort are that successful and reliable thin film circuits can be made and interconnected for system application. While this technique does succeed in eliminating a number of soldered or welded interconnections with respect to those necessary in conventional circuitry, it was found that thin film flip-flop circuits are comparable to the best miniature discrete component circuits in size and weight. It was also felt that connection techniques for conventional component circuitry have advanced to the point where the reliability to be gained by the use of thin film techniques is not important. For most applications, it was concluded that silicon integrated devices would be superior to thin film circuits. The exceptions are at the extremes of high power and high frequency and perhaps at the extreme low power end of the spectrum although microwatt silicon integrated devices are being developed. Thin film techniques are, of course, employed in hybrid devices, e.g., thin film resistors and capacitors on silicon substrates. It is also true that the use of a thin film substrate with evaporated components as a wiring board for silicon integrated devices either in packages or in chip form must be given consideration.

DIODE MATRIX

For various information processing systems, a matrix consisting of an x–y grid with a diode across each node of the network is useful. Goddard Space Flight Center has contracted to obtain such a diode matrix with a 16×16 array of diodes. The unique requirement of this fabrication is that all diodes be good, i.e., a wafer must be processed in which there are 256 successful diodes arranged in a square pattern with no failures. In addition to the diodes a series resistor along each x and y line is required. This is an interesting device because it reveals one of the limitations of present semiconductor technology, i.e., there has been considerable difficulty in obtaining a successful diode matrix. The lack of success has been due to an inadequate yield. In very few instances has it been possible to fabricate a monolithic diode matrix with all good diodes.

RADIATION STUDY OF MICROELECTRONIC DEVICES

Under a one-year program sponsored by NASA, scientists at Battelle Memorial Institute are evaluating space radiation effects on semiconductor microcircuits. Approximately 200 circuits produced by various manufacturing processes are being examined in an electron radiation environment provided by a Van de Graaff electron

accelerator. The accelerator directs a beam of electrons at the semiconductor devices, simulating the environment to be found in the outer Van Allen radiation belt. Gates and flip-flops in flatpacks or modified transistor cases will be examined. Selected parameters in the microcircuits will be measured before, during, and after irradiation to determine effects of the electron environment on the devices. Results of the study should provide information useful in utilizing present microcircuits in space, and in the design and manufacture of new ones.

Chapter 4

Reliability of Microelectronic Devices

PERSPECTIVE

One of the most important features of microelectronic devices has been their potential reliability. In almost all NASA applications, this dominates other considerations. Because of the many different organizations participating in space research activities, almost all of whom are employing microelectronic devices, there are a variety of viewpoints on the proper approach to reliability. At one extreme a decision was made to apply devices to a particular electronic system. Good engineering was performed on the system and excellent experience was obtained with the system. No specific reliability studies were made. At the other extreme diverse basic studies are being made of possible failure modes for microelectronic devices in an attempt to remove these failure modes before entrusting deep space probes to their operation. Between these two extremes are attempts to determine in a practical manner how reliable microelectronic devices actually are, to accumulate data on system applications and to determine failure modes and eliminate them. Some of these studies and experiences with microelectronic device reliability are described below. If any conclusion is to be reached from these studies, it should be that microelectronic devices are very reliable, after the initial failure modes, which have been observed for some devices, are eliminated.

RELIABILITY DETERMINATION BY PERFORMANCE STUDIES

Applying empirical techniques to obtain mathematical performance models of microelectronic devices is one approach to reliability prediction and device characterization which looks promising.

Drift or degradation of microelectronic devices is difficult to detect because of their complexity and high stability. Device specifications generally do not include information regarding parameter drift but only state performance measures under conditions that are seldom realized in practice. To realize the full inherent reliability of microelectronic devices, it is important that design engineers have information regarding performance in any specific application and knowledge of any degradation in performance that is likely to occur. The

Langley Research Center has sponsored some research into these specific reliability areas.[1]

One study used a dual NAND–NOR gate (T. I. SN514) as an example. Performance parameter distributions as determined for a sample of these devices in standard test configurations are shown in figure 32. The devices were then placed in logic circuits designed to determine the influence of system parameters on performance, e.g., the loading factor. From these measurements, empirical mathematical models were derived which described these influences. Extension of the models to other parameters such as time and temperature has not yet been accomplished; nor has the time dependence of the performance distribution been determined. The mathematical models are given in table VIII.

In attempting to determine time dependence of the parameter distributions, these devices were stored at 125° C for a total of 56 000 device hours, after which the performances were remeasured. No statistically significant changes could be detected in the parameter distribution. It is expected, however, that accelerated testing will cause variations and that these can then be related to system performance by means of appropriate equations. If the acceleration factors can be evaluated, then it is possible to predict the time dependence of performance (or reliability) for these devices under normal use conditions.

REDUNDANCY MADE POSSIBLE BY MICROELECTRONIC DEVICES

Microelectronic devices make redundancy techniques more practical. Properly applied, redundancy can improve the system reliability.

The Saturn V computer will be employed to guide the Apollo booster from launch to translunar injection. The reliability of this computer is being maximized by use of triple modular redundancy with majority voting circuits at each logic step in the computer's operation. Reliability is improved by this technique because the operation of the computer will not be affected unless failures occur in two modules out of the three in each logic step. Triple modular redundancy was made possible by the use of microelectronic devices. Compared to the Saturn I computer the Saturn V computer is three times faster, has a much larger memory capacity, is only 20 percent heavier and occupies only 40 percent more volume. Its power consumption is 23 percent lower and it is estimated that its failure rate probably has been divided by more than 1000. The particular devices which have allowed this significant improvement in the Saturn V computer are screened circuits on alumina substrates; silicon chips containing

[1] Research Triangle Institute, Contract NAS1–3371.

TABLE VIII.—*Mathematical Models for Performance of Silicon Integrated NAND–NOR Gate (TI SN514)*

	Units	s	R
$\hat{V}_a = 0.20 - 0.50F_o + 1.11V_a^*$	volts	0. 25	0. 93
$V_a^* = 5.70 + 0.000192\ h_{FE} - 0.000178\ R_L - 0.00419\ R_{in}$ $+ 0.00201\ C_{in} + 0.0751\ C_{oe} + 0.00236\ f_\beta$	volts	0. 022	0. 984
$\hat{t}_f = -287.2 + 117.2F_o + 1.18t_f^*$	n sec	73. 33	0. 96
$t_f = 0.1616 + 0.000123\ R_L + 0.0774\ C_{oe} + 0.00285\ f_\beta$	μ sec	0. 0293	0. 925
$\hat{t}_r = -14.8 + 40.0F_o' = 17.4F_i - 8.2F_o + 1.45t_r^*$	n sec	21. 79	0. 94
$t_r^* = 326.05 + 0.175\ h_{FE} - 0.00718\ R_L - 0.538\ R_{in}$ $- 1.71\ C_{in} - 34.69\ C_{oe} - 1.78\ f_\beta - 38.21\ \ln h_{FE}/C_{in}$	n sec	4. 91	0. 746
$\hat{t}_d = 46.2 + 29.9F_o' - 15.3F_i + 14.3F_i' + 3.9F_o$	n sec	18. 93	0. 93
$t_d^* = 153.98 - 3.65\ R_{in} - 23.24\ C_{oe} - 0.575\ f_\beta + 0.0864\ R_{in}$	n sec	2. 64	0. 753
$\hat{t}_s = 1.4 - 2.3F_o' + 2.8F_i + 3.1F_i' + 0.83t_s^*$	n sec	7. 93	0. 57
$t_s^* = 46.87 - 0.0338\ h_{FE} + 0.00578\ R_L - 0.284\ R_{in}$ $- 0.200\ C_{in} - 0.202\ f_\beta$	n sec	2. 285	0. 867

V_a—pulse amplitude
t_r—rise time
t_f—fall time
t_s—storage time
t_d—delay time
s—standard deviation
R—correlation coefficient

$\hat{}$—predicted mean value
*—value of quantity in standard test circuit
F_o, F_i—fan-in and fan-out
F_o', F_i'—fan-in and fan-out of driving stage
h, R_L, R_{in}, C—component parameters in silicon structure

$$1 \leq \frac{F_o}{F_o'} \leq 5 \qquad 1 \leq \frac{F_i}{F_i'} \leq 3$$

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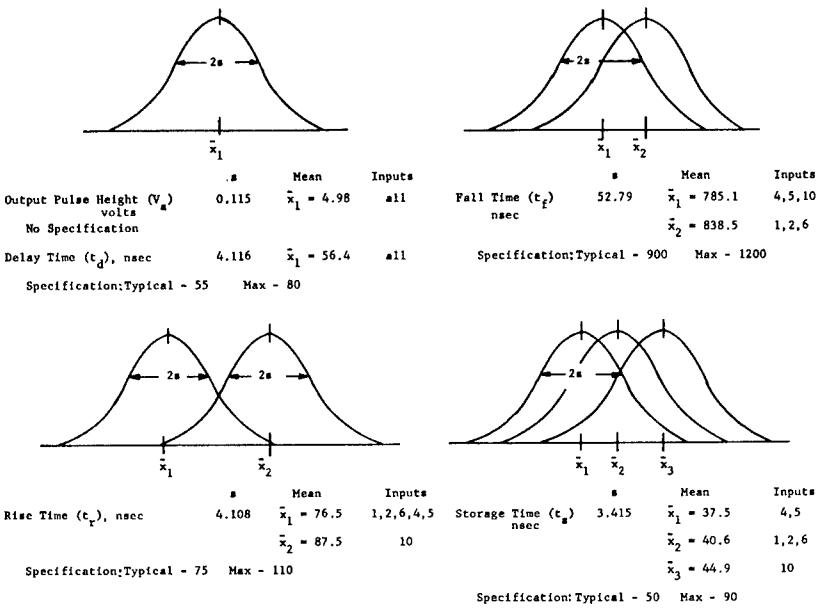


FIGURE 32.—*Performance parameter distributions for NAND–NOR gate.*

the active devices are soldered to the screened circuit. The alumina wafers which are employed for this are 0.3 inches square with the resistors screened on the bottom surface and conductive land patterns provided on the top. Screened edge connections between the top and bottom of the wafer are provided, and metal clips soldered in place are used to connect the wafers to a multi-layer interconnection board. Fifty-four different types of thin film circuits are used in this computing system which, along with its associated data adapter, employs almost 9000 microcircuits. The microcircuits are arranged in groups of about 500 on what are called "pages" in the Saturn V computer. The 500 device "page" is the replacement module.

RELIABILITY WITHOUT REDUNDANCY

Another viewpoint disdains redundancy and concentrates on assuring that the devices themselves are very reliable. This approach requires device standardization and is being used on the Apollo guidance computer. The results look good.

Microelectronic devices can be reliable enough so that redundancy is not needed. This approach has been used in the design of the Apollo guidance computer by the MIT Instrumentation Laboratory. One type of silicon integrated device, a DCTL-NOR gate, is employed as the basic building block. Standardizing on one device allows intensive study of that device and the accumulation of a large amount

of data. After observing the performance of over 200 000 of these integrated circuits, a high level of confidence has been obtained in their performance capabilities. For devices from the best vendor, a failure rate under use conditions of less than 0.005 percent/1000 hrs. at 90 percent confidence was estimated (there were no failures).

In order to insure that the integrated devices being used are good in the first place, elaborate screening techniques have been devised which have succeeded in identifying a number of failure modes. All of the failures observed may be classified as "foolish failures" and are due to poor design or poor quality control. Observed failure modes include:

1. Open bonds due to purple plague caused by poorly controlled thermocompression bonding.
2. Open bonds due to poor aluminum adhesion to the silicon dioxide passivation.
3. Open circuits in the interconnection pattern due to scratches on the device surface or to corrosion of the aluminum conducting path. Corrosion is caused by inadequate cleaning procedures and is accelerated by heat.
4. Cracks in the silicon chip which result from strains induced in the assembly process.
5. Poor layout resulting in excessive spalling of the silicon chip.
6. Poor arrangement of the internal lead wires that provide contact between the silicon chip and the feedthroughs of the package.

The screening tests include mechanical, thermal and power stressing along with visual inspection and studies of electrical characteristics; relatively small samples are used. All of the circuits go through a burn-in test which includes baking, centrifuging and normal operation. Extended life tests are made on large samples of devices from each vendor. Sample size is between 6000 and 18 000 units. The basic simplicity of the particular device helps in providing quick detection and diagnosis of failures during tests. The particular circuit is a DCTL-NOR gate (shown in figure 33) chosen over two years ago on the basis of availability. Even with the development of more sophisticated structures this device is still very attractive due to the large amount of data which has been accumulated on its operation and due to its availability from several sources. For the Apollo guidance computer, this DCTL gate is derated from its 8 V, 100 mW specification to 3 V, 15 mW operation in the computer. The devices employed to date have been encapsulated in the TO–47 type can, but a second generation of this system will use an integrated circuit flatpack containing two gate circuits of the original type. This reduction in the number of encapsulations required for the system will provide additional assurance of reliable operation. Since each of the com-

puters now employs 4000 of the single NOR gate structures, only 2000 integrated circuit packages will be required in the second model.

The success of this particular approach to reliability is demonstrated by the fact that one computer has been in operation for over 2½ years and during this period of time has undergone extensive tests under realistic use conditions. No failures have been observed. Other computers have been in operation for shorter periods of time, again without observation of even one failure. Similar integrated circuits which are used in the ground support equipment but which do not pass as strenuous a screening test have had some failures.

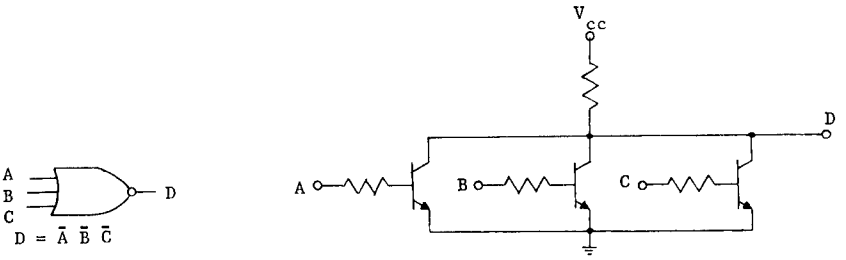


FIGURE 33.—*DCTL-NOR gate.*

INTERCONNECTION RELIABILITY

Assembly and interconnection technology is being studied intensively by NASA. The reliability of interconnections is an important consideration in system reliability particularly with highly reliable microelectronic devices.

One of the more frustrating failure modes observed in practical electronic systems has been that of poor wiring joints. In the past, most of these connections have been made by soldering. More recently welding methods have been investigated in an attempt to find a more reliable process. At the Marshall Space Flight Center, interconnection of microelectronic devices, in particular silicon integrated devices, has been studied. The conclusion is that redundant welded interconnections are more reliable. Redundancy here means that the device lead wire is welded to the circuit board in at least two places. Numbers which have been quoted give the probability of a bad welding connection as 10^{-4}. Redundant welds reduce this probability to 10^{-8} (assuming statistical independence). When one considers that a typical space vehicle has approximately one million electrical connections, it is obvious that high connection reliability is essential. Other factors which have been found to influence the quality of the connection are the shape and time duration of the welding pulse and the nature of the materials between which the weld is being made. For

example, no copper is recommended for the integrated circuit interconnection board; while Kovar and nickel combinations are compatible.

The device attachment and interconnection problem is being studied further. This includes an examination of multilayer circuit boards for use with integrated circuits. These multilayer boards may have as many as 10 layers of conductors.

Interconnection and assembly methods are not only a reliability problem but are also important in cost and weight considerations. The particular solutions being developed for space electronic systems are applicable to all microelectronic systems.

Chapter 5

Applications

PERSPECTIVE

It is in the applications of microelectronic devices that the NASA space research programs have been most active. The first silicon integrated devices entered orbit in 1963 and have operated successfully. A number of systems and equipment containing microelectronic devices are in advanced development and, almost without exception, new designs include a variety of microelectronic devices. Much of the application information being generated can be of value to other users of microlectronic devices.

The particular applications described in the following sections represent primarily those for which information was most accessible. Most of the in-house NASA developments are covered but significant contractor activities have probably been missed since there is no practical means for extracting incidental microelectronics application information from equipment or system suppliers.

INTERPLANETARY MONITORING PLATFORM (IMP) [1]

These first space borne silicon integrated devices have performed without failure despite the lack of a comprehensive reliability program!

The IMP I satellite, launched November 27, 1963, uses TI solid circuits (SN510 and SN514) in its optical aspect computer (for attitude determination). These are the first integrated circuits put into orbit and they have performed satisfactorily since launch.

The integrated circuitry in IMP consists of binary counters, flip-flops, and inhibiting circuits. The diagram of an SN510 used as a binary counter is shown in figure 34. In the early design work, the Goddard Space Flight Center encountered some difficulty in designing a transistorized input circuit. The SN510 counter requires a plus input signal; triggering occurs when the positive signal voltage drops toward ground potential. For reliable triggering, the signal amplitude must be somewhat less than the supply voltage, V_{cc}. The input circuitry that was used in actual flight is shown in figure 35. The voltage divider action of R_1 and R_2 insures that the voltage require-

[1] Bush, E. G., NASA TN D-1758.

ment is met because the input signal voltage at the collector of Q_3 can never exceed $V_{cc}/2$.

The transistors Q_1 and Q_2 and capacitor C_1 in figure 35 produce a positive pulse which drives the input transistor to each counter. The inhibiting circuit at the base of the input transistor stops the count at a time determined by gating signals. Since the collector-to-emitter voltage is about 0.1 V when the transitor is biased on, and since the base-to-emitter voltage of the input transistor is about 0.5 V, an inhibitor of this type is positive in action.

Figure 36 shows a unique type of counter which requires input circuits to both the first and second stages. This counter counts at the input signal rate until signal A is received and then counts at half that rate until cut off by signal B. Since each input transistor of this counter requires two independent inhibiting circuits, a single

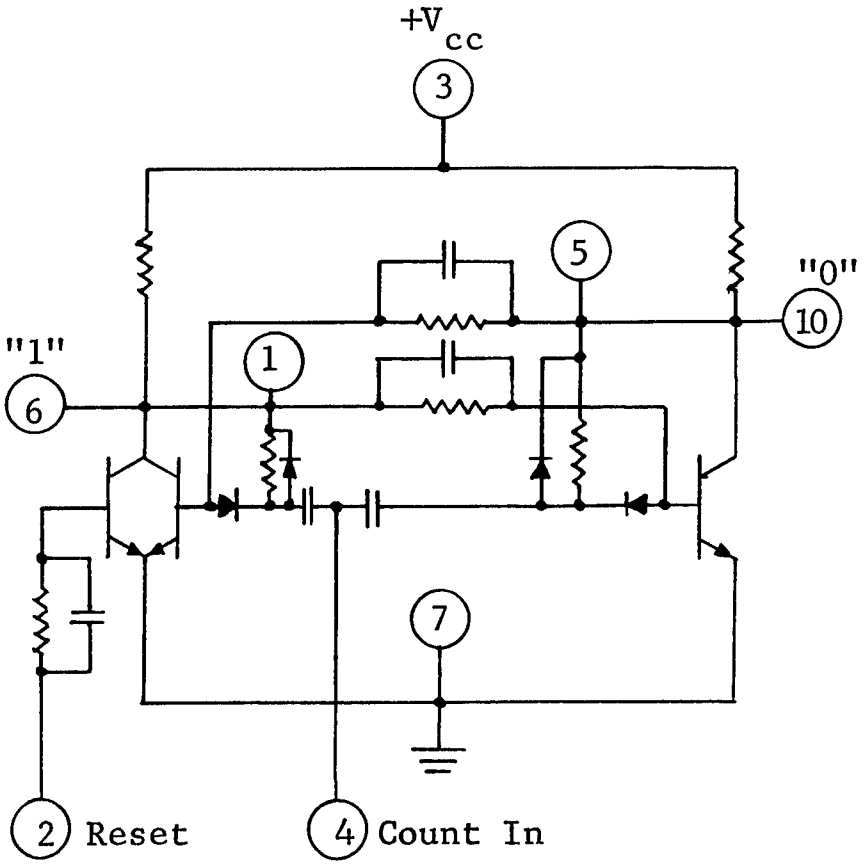


FIGURE 34.—*SN510 solid circuit used as a binary counter.*

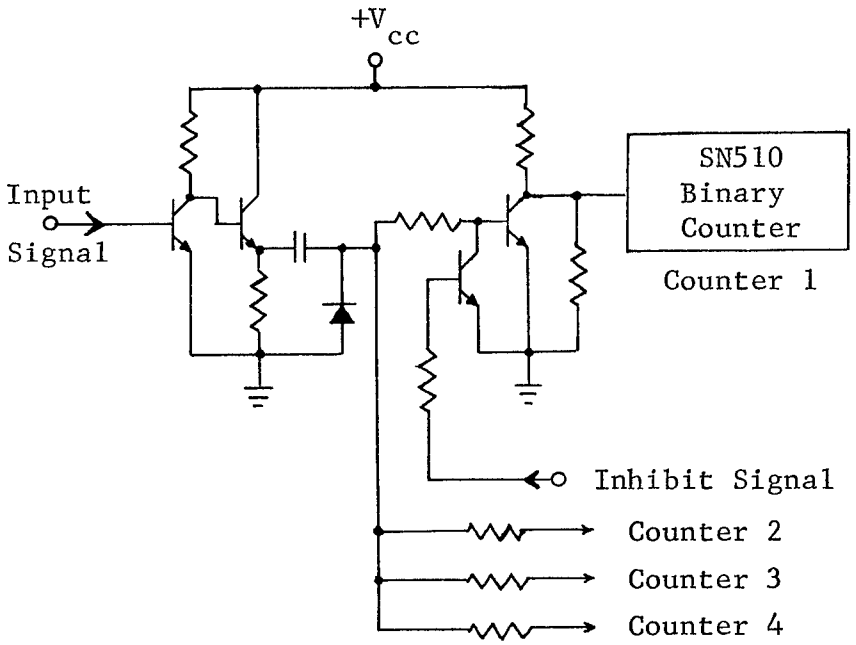
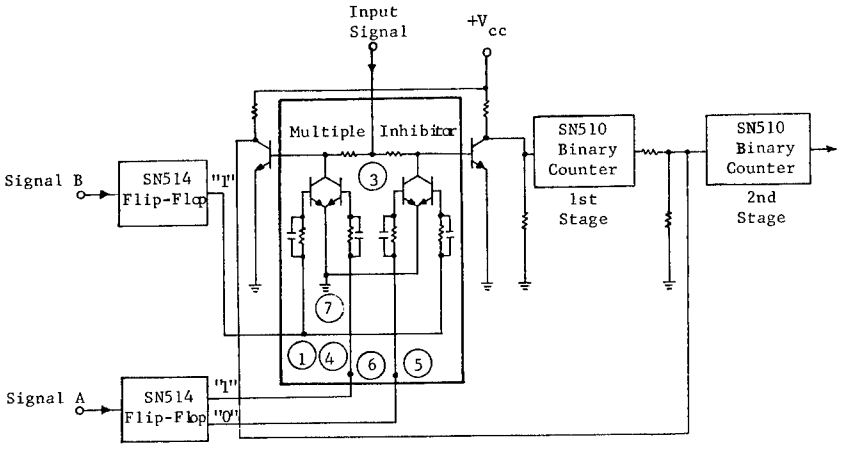


FIGURE 35.—*Input circuit to SN510 binary counters.*



NOTE:
"1" = Ground
"0" = + Voltage

FIGURE 36.—*Full or half speed counter.*

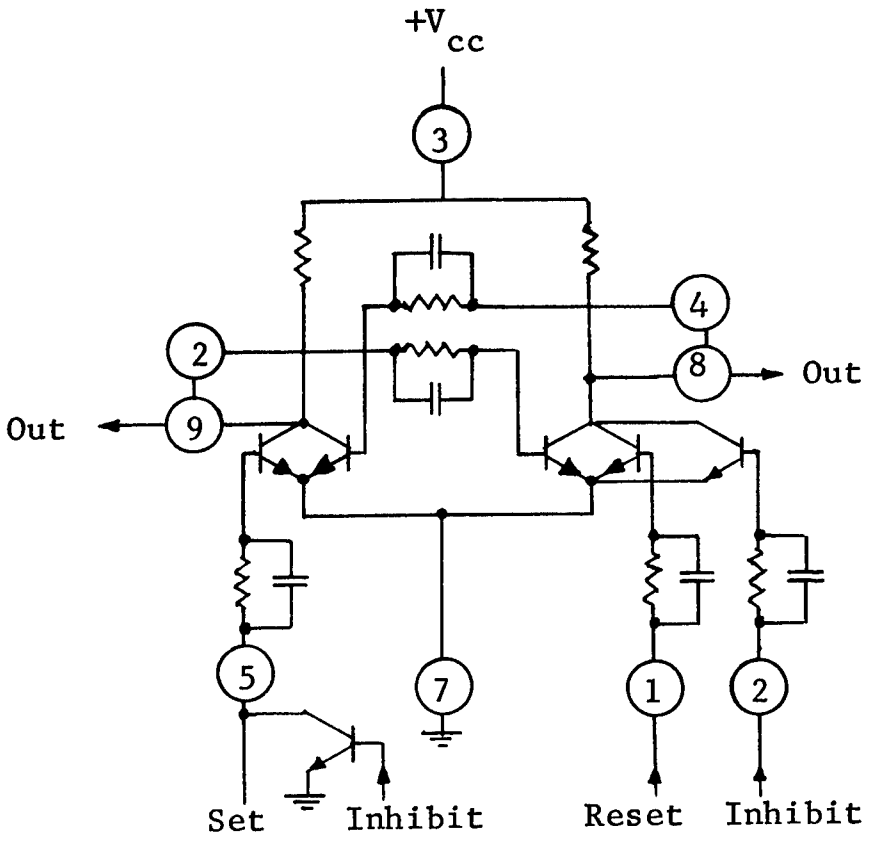


FIGURE 37.—*SN514 solid circuit used as a flip-flop.*

SN514, shown in figure 37, is used to perform this function instead of four transistors.

The SN514 circuit can be set to the "1" or "0" state by applying a positive voltage to terminal 1 or 5, respectively. The external transistor Q_1 can effectively gate or inhibit the set signal. However, the transistor Q_1 can be eliminated and signal inhibition obtained by connecting the inhibiting voltage to terminal 6, if no inhibiting occurs after the flip-flop has been set.

The main disadvantage in using integrated circuits on IMP was found to be their increased power drain compared to conventional transistor circuitry. For example, both the SN510 and the SN514 dissipate 2 mW with a 3 V supply, at 25° C, as compared to 0.5 mW by their complementary-symmetry transistor counterparts. This disadvantage is overcome, however, by a transistor switch which disconnects the supply voltage from all circuits, except one flip-flop and two transistors, for 4/5 of the time of one sequence of the encoder.

This decreases the power drain by 80 percent. The peak power dissipation by the system is about 150 mW.

The solid circuit devices are mounted on submodules as shown in figure 38. These are inserted into Digi-clips on a finished printed circuit card as shown in figure 39. This system can operate with a supply voltage tolerance of ±50 percent from a nominal 3.5 V dc and a tolerance of ±30 percent on the input signal voltage. The operating temperature is from −20° C to +80° C.

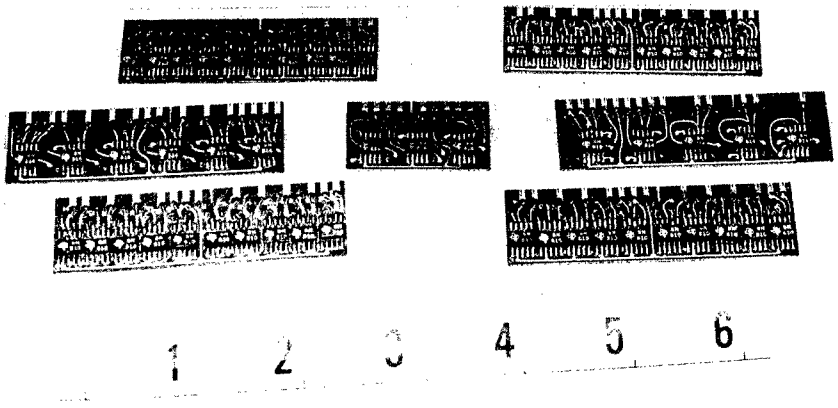


FIGURE 38.—*Modules of the flight model computer card.*

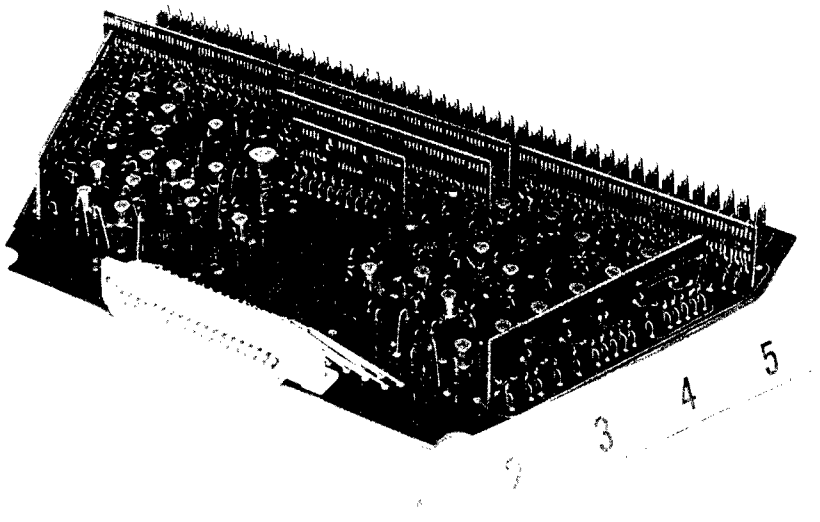


FIGURE 39.—*Flight prototype of optical aspect computer.*

DIGITAL TAPE RECORDER ANALYZER

Test equipment containing 89 silicon integrated devices is described. It is used to count errors in digital recording systems.

The digital tape recorder analyzer is an item of ground support test equipment. The reason for use of integrated circuits here is their proven reliability. Other advantages which may accrue through the use of microelectronic devices are incidental. About ¾ of this test equipment is fabricated from 89 silicon integrated devices of five types. The remaining ¼ consists of conventional solid state circuitry.

The tape recorder analyzer is a test instrument designed to perform error analysis on space borne digital tape recorders. This analyzer is designed specifically to test a 200 ft endless loop, eight channel digital tape recorder which is used on both the Tiros and Nimbus spacecrafts. The design of the test instrument is based upon a parity checking technique. Signals are recorded on six of the tape channels which originate in an internal random code generator, an internal pattern generator, or an external data source. Odd parity is continuously generated during record time by controlling a parity bit with the initial parity checking circuitry and recording a parity bit on the 7th data channel when required to obtain odd parity. Errors in the recording apparatus are indicated on the output by the presence of even imparity between the seven channels. This does not allow for the occurrence of compensating errors but the probability of these is very small. Errors are counted and the sum is displayed on an error count display. On the eighth channel of the recorder a clock signal is recorded. Errors in the phase and missing clock pulses are counted and can be summed with parity errors on the output display. The information desired is the total number of errors which occur in the recording process. Methods are included for observing errors which originate at the splice on the endless tape. These can be subtracted from the total error count.

Because this test instrument is used by a variety of individuals under various conditions, it is designed for ease of operation and maintenance and with substantial mechanical and electronic protection. For example, every power supply and signal input generator to the analyzer is provided with special protection circuits which insure that dangerously high signals are not applied directly to the integrated devices and other circuits. The design is flexible enough to be adaptable to other applications. For example, it would be possible to analyze prerecorded tapes for either even or odd parity.

A more complete description of this apparatus which is an interesting mixture of conventional and microelectronic devices is given in NASA publication G–579N.[2]

[2] J. A. Scivilli, "The Digital Tape Recorder Analyzer," Goddard Space Flight Center, NASA (obtainable from OTS).

RECORD AND PLAYBACK AMPLIFIERS

Multichannel digital tape recorders require record and playback amplifiers on each channel. These amplifiers are being developed in microelectronic form for information storage and retrieval in space research experiments.

Data obtained from various research experiments are converted to digital form by an analog-digital converter and stored on an eight-track digital magnetic-tape recorder. The apparatus described here is designed to store data through a 100 minute orbit and to play back the information on interrogation at a 30 to 1 speedup rate. This requires an input bit rate from dc to 250 bits/sec and an output rate from dc to 7500 bits/sec. The record and playback amplifiers required for this apparatus have been designed in microelectronic form to take advantage of reductions in size, weight, and power consumption and to improve the reliability. A ten channel record and playback system has been designed so that two of the channels are redundant.

The record amplifier is designed to take a high impedance digital signal (0 V and 2 V for a logical "0" and "1") and to have an output sufficient to drive the recording head (3.5 mA and −3.5 mA for the logical "1" and "0"). The microelectronic circuit is shown in figure 40 and the electrical specifications are given in table IX. A field-effect transistor gives a high input impedance and the remainder of the amplifier operates in the saturated switching mode. The output current, determined by resistor R_6 in the power supply voltage, is suf-

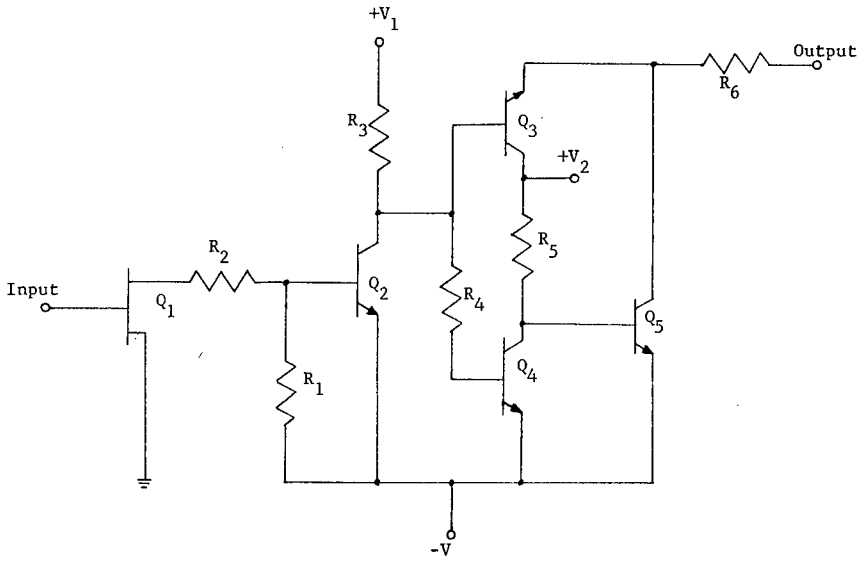


FIGURE 40.—*Circuit for integrated record amplifier.*

ficient to produce a saturating flux in the magnetic tape under all conditions. For 0 V input the field effect transistor Q_1 conducts and transistors Q_2 and Q_5 are saturated while Q_3 and Q_4 are cut off. This gives -3.5 mA with $+3$ volts across R_6. For the "1" input a 2 V or greater signal is applied to the field-effect transistor pinching it off. As a result Q_2 and Q_5 are cut off and Q_3 and Q_4 are in saturation resulting in $+3.5$ mA output to the recorder head. The power dissipation of the amplifier is 22 mW. The record amplifier is fabricated using 3 silicon chips interconnected within a common package. Resistors are formed from thin films deposited on the passivated surface of the silicon in order to obtain large resistance values and better temperature coefficients.

TABLE IX.—*Electrical Specifications for Record Circuit*

V_{in}	0 V maximum for logical "0" +2 V minimum for logical "1"
I_{in}	0 μa for logical "0" 80 μa for logical "1"
I_{head}	3.5 mA ±10% in each direction at all temperatures, and directly proportional to the power supply voltage (±3 V dc)
dc power dissipation	<36 mW at ± 3 V
Operating temperature range	−20° C to +80° C

TABLE X.—*Electrical Specifications for Playback Circuit*

V_{in} (from playback head)	1.2 – 2.4 mV (peak)
Bandwidth	20 – 18 000 cps
Threshold voltage	0.40 mV, + 10%, −30%
V_{out}	0 V for a logical "0" 5.0 V ±20% for a logical "1"
Input impedance	10 k Ω ±10%
Output rise time	< 3 μsec
Output impedance	Enough to produce a rise time < 3 μsec into a 20 k Ω load
Power	± 6 V dc ± 5% — minimum possible current
Bit rate	0 – 7500 bits/sec
Operating temperature range	−20° C to +80° C

The playback circuit must take the 1.2 to 2.4 mV signal from the playback head and give 0 V and 5 V out across a 20 000 ohms load for a logical "0" and "1". The rise time of the output pulses must be 3 microseconds or less and the bit rate is up to 7500 per second. Other specifications are given in table X. Two integrated circuit packages are needed to meet these requirements. The first contains a direct-coupled feedback-stabilized preamplifier with a gain of 52 dbv as shown in figure 41. The gain is set by selecting the value for the

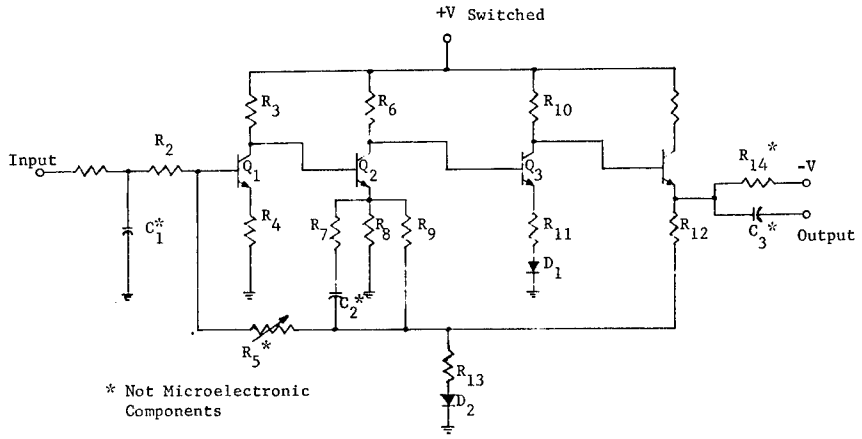
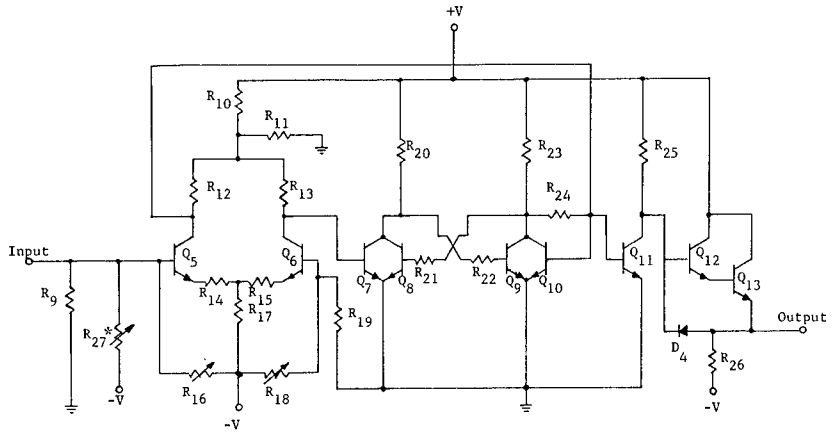


FIGURE 41.—*Circuit for integrated playback preamplifier.*



* This Resistor Is Not Microelectronic

FIGURE 42.—*Circuit for integrated high-level playback amplifier.*

conventional external resistor R_5. The bandpass of the amplifier is 20 cps to 18 kc and is determined by the input RC filter; the total power consumed is 3.7 mW. The output of the preamplifier is used to drive the second stage of the playback circuit shown in figure 42. This consists of a differential amplifier, a flip-flop, an inverter and a Darlington pair. The differential amplifier is a threshold detector which triggers the flip-flop. The total dissipation of this integrated circuit is 12 mW and the positive 5 V output signal which corresponds to the logical "1" is developed at the output. The entire playback amplifier is mounted in 2 flat modules which are combined with the record amplifier on a $1 \times 2 \times \frac{3}{4}$ inch package.

OGO DATA PROCESSOR

This application illustrates circumstances for which multichip silicon integrated circuits were selected. Short development cycle and low cost were prime selection criteria.

The requirements for the digital data processor for the Orbiting Geophysical Observatory (OGO) satellite illustrate an application for multichip integrated circuits. The schedule for the satellite development allows less than one year for delivery of the data processing system. The use of microelectronics was dictated by critical weight requirements in addition to important cost and reliability factors. It was decided that the multichip silicon integrated circuit approach offered the best solution for this system which is under development and scheduled for delivery during the first half of 1965.

The digital data processing system, which is being developed for the Goddard Space Flight Center by the General Instrument Corporation, will consist of approximately 150 integrated circuits. These are arranged into seven identical binary counters, one quasi-floating point counter, a control subsystem and a readout subsystem. Each of the binary counters contains nine flip-flops, the circuit for which is shown in figure 43. The multichip approach allows the use of both p–n–p and n–p–n transistors in this flip-flop. These circuits are put on a ceramic substrate and mounted in a wafer type package similar to those shown in figure 44. A typical flip-flop dissipates on the order of 2 mW and the total system dissipation is less than 370 mW. The

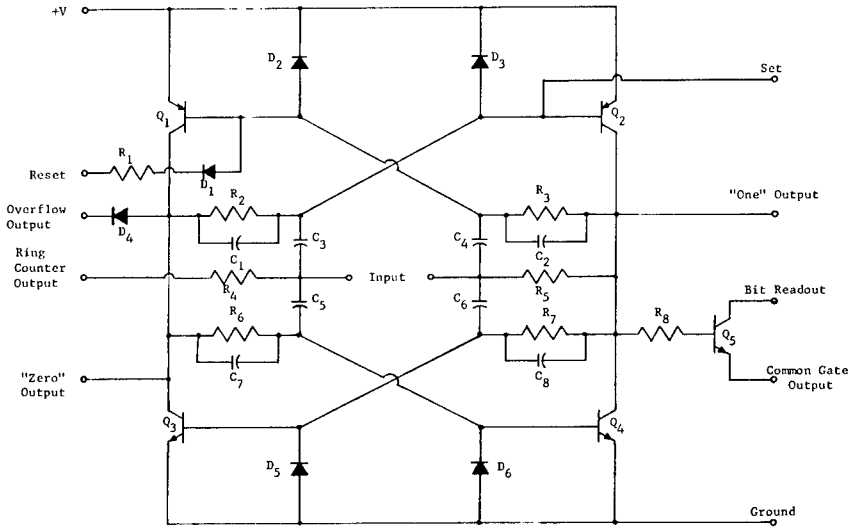


FIGURE 43.—*Circuit for multichip integrated flip-flop using complementary transistors.*

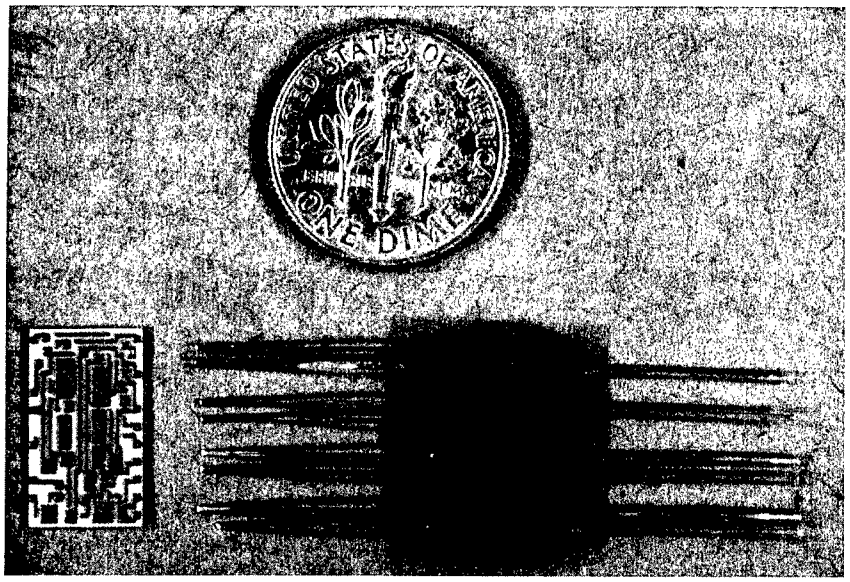


FIGURE 44.—*Multichip integrated silicon circuit.*

completed digital data system will weigh about 0.5 lb and have a volume of 20 in^3.

The function of the system is to take binary data from eight parallel channels and to present accumulated counts to the spacecraft central data system on external command. The major functions therefore are counting, readout-sequencing on demand, and output-data steering. The control subsystem sequences the event count accumulated in the binary registers and permits flexibility in the selection of work and multiplexing rates. The readout subsystem sequences the bits accumulated in each of the eight counters at a rate determined by the central data system of the satellite. Only the counter selected by the control subsystem will present its data for readout. A typical readout may be eight words at nine bits each for a total of 72 bits from the eight counters. The readout bit rate will be up to 200 kc as determined by an external clock.

PROGRAMABLE TIMING CIRCUIT

A timing circuit has been designed making use of a few each of five types of silicon integrated devices. It counts the 1 pps input up to predetermined sums and then produces an output. It has many timing applications but may be too expensive at present.

An interesting useful timing circuit has been developed at the Manned Spacecraft Center in Houston. It uses a combination of five types of integrated circuits from three different manufacturers, mag-

netic shift registers and an Accutron clock. Its function is to give a signal (as indicated by the change in state of an output flip-flop) after each of ten preselected time intervals which occur immediately in sequence. In the present model the flip-flop is used to drive a lamp so that each time interval determines either an ON or OFF period of the lamp. The individual time intervals may be from 1 to 60 sec in 1 sec increments. In the breadboard, the timing sequence is initiated by closure of a mechanical switch but in other applications a starting pulse could be used. Similar timing circuits are expected to have a variety of applications.

In figure 45 a block diagram of the timing circuit is given. In addition to the integrated devices, this circuit uses a number of conventional components. A breadboard of the circuit is shown in figure 46 and a list of major components is in table XI.

The main counter consists of seven SN511 flip-flops and six NOR gates each being ½ of an SN514 dual NOR gate. At the initiation of a timing cycle the flip-flops in the main counter are set by pulses from the magnetic ring counters in order to give the preselected countdown interval. The counters then proceed to count the 1 pulse per second originating in the clock until zero is reached and a pulse appears at the output of the main counter. The counter output pulse changes the state of the output flip-flop and thus that of the output indicating lamp and, in addition, drives the single shot multivibrator, SE160K. The output of the single shot multivibrator changes the states of each of the seven ring counters through the emitter follower and driver circuits. This advancement of the ring counters takes place in a time period short compared to the clock pulse rate, thus resetting the main counter to start a new counting cycle. This sequence is followed continuously with each of the 10 preselected time intervals being generated in sequence.

In order to reprogram the timer the reset button is pushed. This deactivates the clock input to the counter and sets the output flip-flop so that the lamp is off. The new set of time intervals is programed into the magnetic ring counter memory by dialing each in sequence on the switches, placing them in the counters by depression of the enter switch, advancing the ring counters one step by depressing the shift switch, and then inserting the next time interval. After all ten time intervals have been inserted, the timing circuit is again ready to operate following the new program. Operation is initiated by depressing the start switch which unlocks the clock pulse and operation proceeds continuously as described before.

This timing circuit which is described by the designers as a programable photo-timer has application in space research; commercial and industrial applications may be prohibited by the high cost unless there is a decided premium on accuracy and reliability.

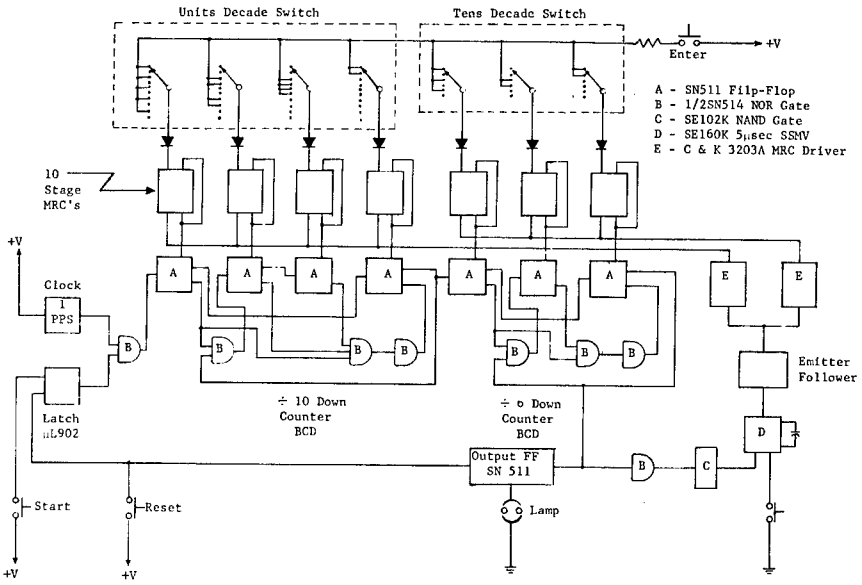


FIGURE 45.—*Block diagram of timing circuit.*

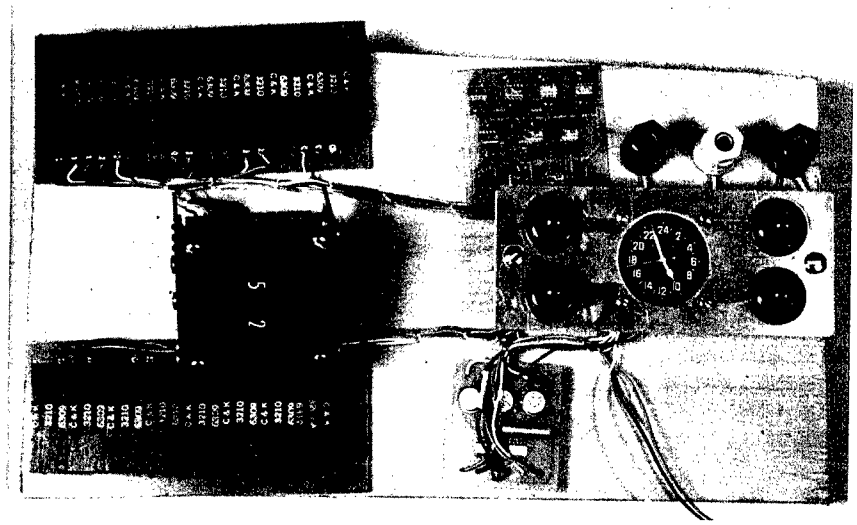


FIGURE 46.—*Breadboard of microelectronic timing circuit.*

TABLE XI.—*Major Parts List for Photo-Timer*

Description	Manufacture and designation	Quantity used
Flip-flop	Texas Instruments SN511	8
Dual NOR gate	Texas Instruments SN514	4
Latch	Fairchild μL902	1
NAND gate	Signetics SE102K	1
Single-shot MV	Signetics SE160K	1
Magnetic shift register	C & K Components 3210	14
MRC driver	C & K Components 3203A	2
Clock	Bulova Accutron	1

STATIC INVERTER

Application of microelectronics to a static inverter promises to improve the system reliability. Similar techniques can be applied to power inversion in many applications.

At present rotating machinery is employed for most power conversion applications in missiles and satellites. Static inverters convert a low dc supply voltage to a higher ac voltage for distribution to spacecraft electronic systems. These static inverters, because of the absence of moving parts, have a greater potential reliability than rotating machinery. Other advantages which have been cited are small size, light weight, high efficiency, and low maintenance. However, these do not offer as high a margin of improvement over rotating machinery as reliability. The introduction of microelectromic structures to static inverter designs is promising to provide an additional reliability improvement over static inverters employing conventional components. The static inverter which is serving as a research vehicle for the application of microelectronics at the George C. Marshall Space Flight Center is a 115 V ac 3-phase, 400 cps unit rated at 250 VA. This general purpose unit could be used as a regulated ac power supply for the guidance and control electronics in a space booster. Unregulated dc input comes from the vehicle primary supply at a nominal level of 28 V dc. The 115 V ac output is regulated to within ±1 V ac at any load from zero to full and with inputs from 25 to 30 V dc. The frequency is precise, and harmonic distortion is minimized. This inverter is built to withstand severe environmental extremes and meet all other spacecraft requirements.

As shown in the block diagram of figure 47, the static inverter is made up of three main sections, a power section, a control section, and a timing section. Inversion from dc to three-phase ac takes place in the power section. Three-phase sinusoidal waveforms are approximated

by combining square waves which have the proper relative amplitude and phase relationships. These square waves are generated from transformer-coupled transistor flip-flops. The required switching sequence is fixed by the timing section.

The timing section which generates all timing signals is the only section using microcircuits in the present model. Its primary function is to provide the gating signals to the power section for controlling the switching sequence of the power converters. It also supplies an ac sequence excitation to a magnetic amplifier in the control section.

A functional block diagram of the timing section is shown in figure 48. Two identical timing channels which operate in standby redundancy increase the reliability of this section. The redundancy is practical because of the use of integrated devices.

The frequency divider is a binary countdown logic circuit consisting of five flip-flop (with emitter follower output) integrated circuits (TI SN511), as shown in figure 49. The operation of this circuit may be understood by assuming that all the flip-flops are preset such that $q=R=0$ and $\bar{q}=S=1$. A positive clock pulse applied to the first flip-flop will charge the internal capacitor and provide for a switching action to occur when the clock pulse again becomes 0. After this flip-flop switches, $q=R=1$, $\bar{q}=S=0$, and the first flip-flop will switch again at the end of the next clock pulse. Since the first flip-flop changes states at the end of each positive input clock pulse, it effectively halves the input clock pulse frequency. As illustrated in figure 49, each stage is connected identically and each stage has a clock pulse input from the preceding stage. Since the output of each stage is half the frequency of the input clock pulse, the outputs of the fourth stage are 2^{-4} or $1/16$ of the clock pulse repetition rate of the input to the first state, i.e., the 76.8 kc input has been reduced to 4.8 kc. As noted there are two output flip-flops; one of these supplies a 4.8 kc signal to the pulse sequence generator while the second is employed as a drive to

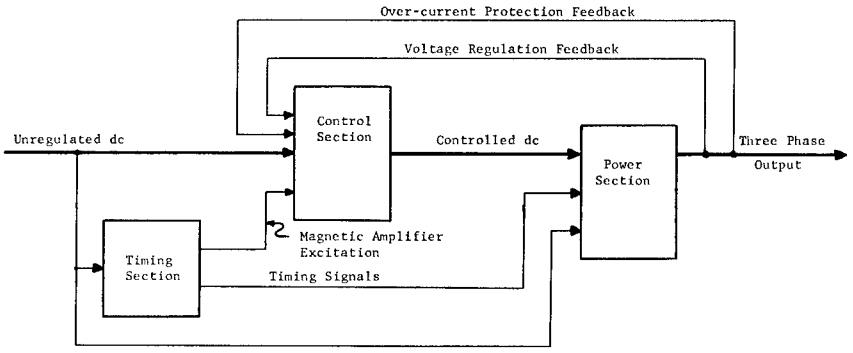


FIGURE 47.—*Block diagram of the static inverter.*

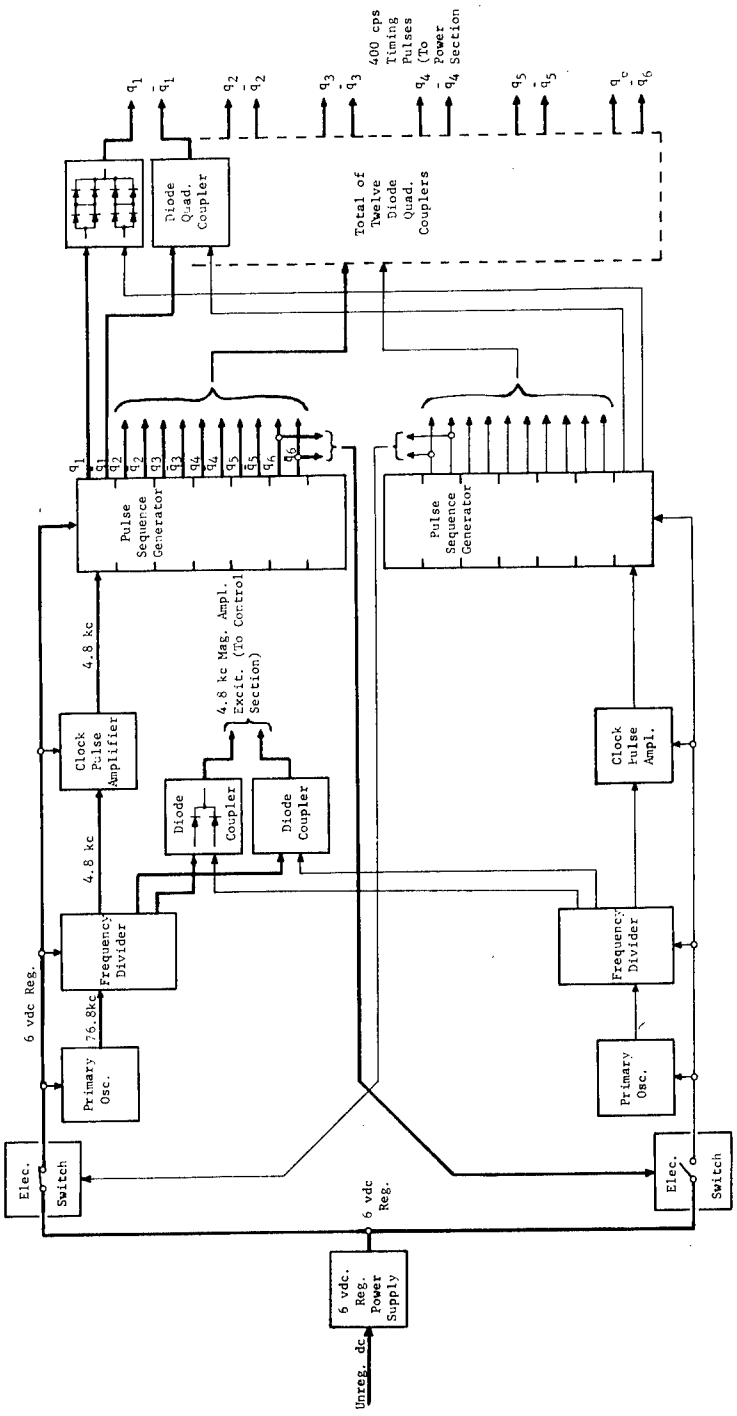


FIGURE 48.—*Timing section block diagram.*

the magnetic amplifier in the feedback control circuit. The clock pulse amplifier improves the shape of the clock pulse supplied to the pulse sequence generator. The pulse sequence generator contains six flip-flop integrated circuits (SN511) and one integrated dual NAND-NOR gate (SN514) arranged in a ring counter as shown in figure 50. Since a positive voltage is here employed as a logic "1", each half of the gate is a NOR circuit. If either input 1, 2 or 6 is a logic "1", then one of the three associated transistors will be turned on and output 8 will be a logic "0". The outputs of each flip-flop are a positive going pulse train and its logical complement. Each flip-flop cycles once for each 12 cycles of the 4.8 kc clock pulse, i.e., at a rate of 400 cycles/sec.

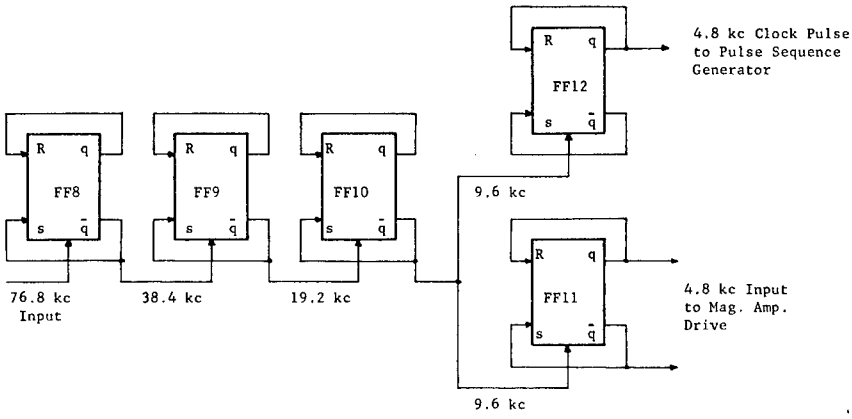
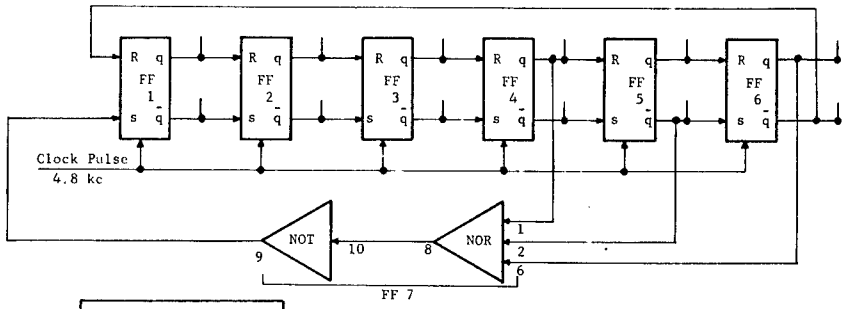


FIGURE 49.—*Frequency countdown circuit.*



Flip-Flop Truth Table

T_n		T_{n+1}	
R	s	q	$\bar{q}$
1	1	q_n	$\bar{q}_n$
1	0	0	1
0	1	1	0
0	0	Indeterminate	

Positive Logic

FIGURE 50.—*Block diagram of the pulse sequence generator.*

Operating models of this static inverter design are in existence and are being studied. Successful operation has been achieved. In addition, new developments are taking place which will provide additional microelectronic structures for application in this inverter type. The two units to which particular attention is being given at this time are the preamplifier and power amplifier in the power section. The integrated version of these units is discussed in "Static Inverter Preamplifer and Power Amplifier," Chapter 3.

GROUND SUPPORT EQUIPMENT

The ground support equipment (GSE) for the Apollo guidance computer includes a large test apparatus which employs microcircuits in its operation. A 3 input DCTL silicon integrated NOR gate, also used in Apollo flight equipment, is employed.

The criteria for the choice of microelectronic devices for ground support equipment—GSE—(in this case the test equipment for the Apollo on-board guidance system computer) [3] are similar in many respects to those for industrial and commercial applications of microelectronics. For this application weight, size, and power consumption are not critical, nor are the reliability demands as stringent because the equipment is repairable. It is, therefore, interesting to consider the reasons for which microelectronic devices were chosen for the test equipment for the Apollo Guidance Computer (AGC).

First of all, two disadvantages are apparent:

1. The size of commercial test equipment, which is part of this system, limits any attempt at miniaturization.
2. The integrated digital circuits have a lower noise threshold than would be obtainable with conventional components.

Offsetting these disadvantages are the assured cost reductions and the lower maintenance which is possible with the use of microelectronics. In addition, techniques for the particular devices employed have been developed for use in the on-board Apollo Guidance Computer, and thus are readily available. In the on-board computer it was decided to use only one type of integrated circuit in order to minimize qualification, testing, and reliability studies. The device chosen is a three-input common emitter, common collector NOR gate using direct coupled transistor logic. The circuit of this unit is shown in figure 51(a) and configurations are shown which allow increased fan-in and fan-out in figures 51(b) and 51(c).

A basic part of the GSE is the AGC Test Set which is used to perform an operational check on the flight computer. The test set consists of three main sections:

[3] Plemenos, F. A., and O'Bryant, D., "Microelectronics Design of Digital GSE," p. 60, NEREM Record, 1964.

1. The Programer and Monitor Section insures that correct information is loaded into the computer and checks computer locations for difficulties. It monitors or indicates different computer outputs and is capable of stopping the computer at various test locations.

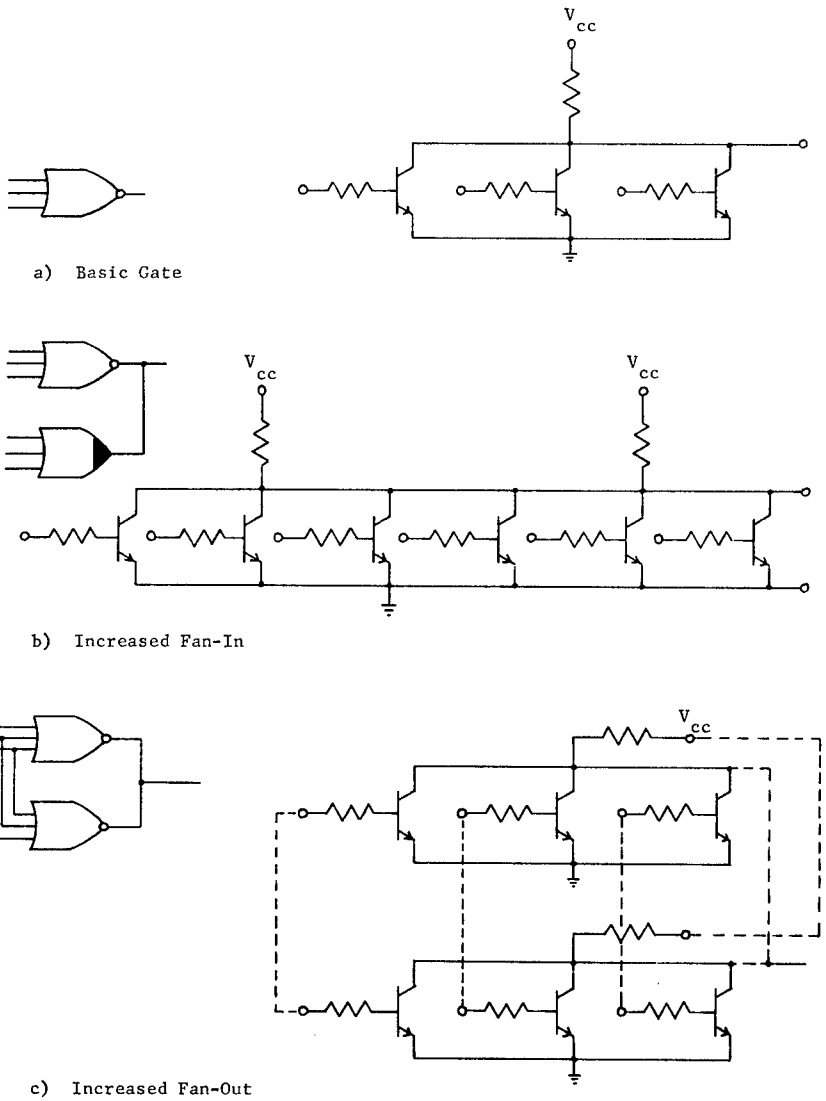


FIGURE 51.—*Methods for increasing fan-in and fan-out of integrated DCTL gate.*

2. The System Interface Section generates signals used in the operational check and checks AGC input and output information.
3. The Self-Test Section makes a complete check of the test set logic and wiring without using any other special test equipment.

The noise problem encountered with the use of microcircuits makes it necessary to keep noise pulses below approximately 0.2 V. Otherwise, the logic units may malfunction as a result of their own internally generated noise. This test set has been successfully designed using the silicon integrated DCTL gates.

THE INTERROGATION, RECORDING, AND LOCATION (IRL) SUBSYSTEM

Nimbus will contain a number of silicon integrated circuits performing a variety of logic functions. Digital system design techniques used here are applicable to other data systems.

The science of meteorology requires the frequent and periodic collection of data pertaining to the surface of the earth and its atmosphere. Many regions are not covered by present data collection programs. Therefore, a system of unmanned observation stations to store or relay data would provide a vital service. Nimbus, a polar orbiting earth oriented satellite, can collect and store data from free-floating or fixed platforms such as buoys, remote weather stations and some types of balloons. A system of this type must be programmable from a ground acquisition and command station (GACS) to enable it to address specific platforms during each orbit. It must receive and store data from each platform and read out the data to the command station at the end of the orbit. Microelectronic devices are being applied to this system on a broad basis.

The IRL system consists of three parts, one on the satellite, one on the observation platform, and one on the GACS. The satellite's data collection package consists of a radio communication and ranging system, a command storage system, and a data storage system. Each observation platform will be equipped with a radio communication system, a telemetry coder to convert sensor measurements to digital form and an address decoder containing the discrete address of the particular platform. The ground acquisition and command station will have a radio communication system, punched tapes to program the satellite-borne IRL subsystem, and a storage system to accept satellite received data.

The modules to be used in each subsystem are listed in table XII. Figure 52 is a block diagram of the IRL subsystem to be used in the satellite as it operates with the observation platform.

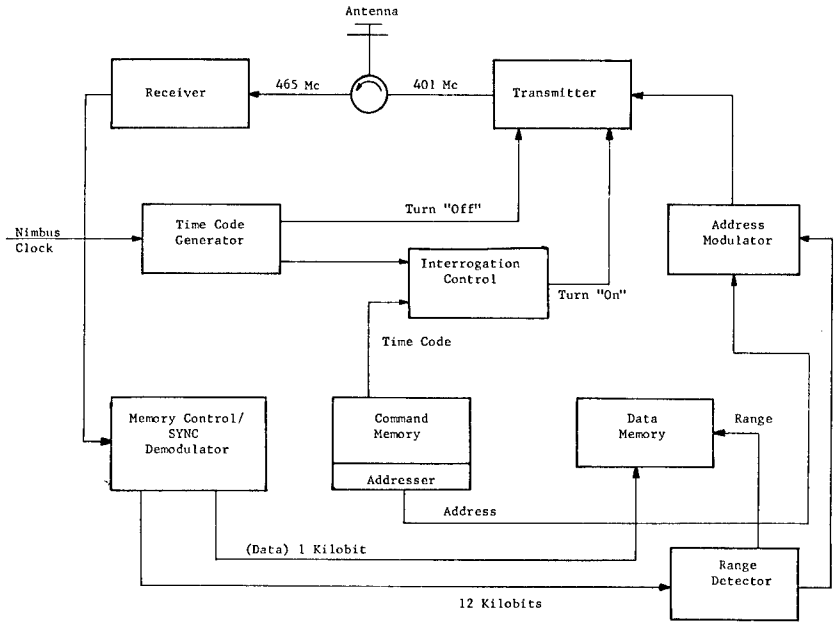


FIGURE 52.—*Block diagram of satellite subsystem operating with observation platform.*

TABLE XII.—*Module Requirements of IRL Subsystems*

Module	Satellite	Platform	GA and CS
Time code generator and detector	X*	-------	-------
Range word generator and modulator	X	-------	-------
Command and data memories	X	-------	X
Address commutator and verifier	X	-------	-------
Address decoder	-------	X	-------
Range detector	X	-------	-------
PCM demodulator and sync. demodulator	X	X	X
Power supply	X	X	X
A/D converter and formatter	X	X	X
Punched tape formatter and control	-------	-------	X
Transmitter frequency (Mc)	400	465	465
Receiver frequency (Mc)	465	400	400
Antenna	-------	X	-------

*The X indicates that the module is used.

The logic for the satellite-borne IRL subsystem is designed using Texas Instruments Series 51, 52, and 53 circuits. The following components are contained in a large standard Nimbus module which is nominally $4 \times 6 \times 6.5$ inches:

1. Time code generator and detector
2. Range word generator and modulator
3. Address commutator and verifier
4. Range detector
5. PCM demodulator and sync. demodulator

The command and data memories will be located in a small standard Nimbus module which is nominally $2 \times 6 \times 6.5$ inches. Each transmitter and its associated diplexer will be contained in a large module; each receiver will be in a small module. The total weight of the satellite-borne subsystem shall not exceed 15 pounds. The logic circuitry for the platform equipment will be in a large module.

Brief descriptions of the components which contain microcircuits are given below:

a. Time Code Generator and Detector—The Time Code Generator and Detector consists of a time code generator and a time code correlator (detector). The time code generator generates signals of 2.5 ± 0.5 V (logical one) and 0 ± 0.3 V (logical zero) as an output to the time code correlator. The correlator then functions to detect a match between the binary code generated and a code from the command memory. If a code match is detected, a logical one turns the transmitter on for a specified time. The time code generator and detector uses 24 flip-flop and 36 logic microcircuits to perform its operation.

b. Range Word Generator and Modulator—This unit produces a digital subcarrier at a bit rate of 12.5 kilobits/sec and synchronizes signals of 1 kc and 80 μsec pulses at a rate of 62.5 pps. Ten flip-flop and 19 logic microcircuits are used in this unit.

c. Address Commutator and Verifier—The address commutator produces an NRZ PCM signal consisting of 16 bits/word. The output from the commutator is put into the verifier allowing an NRZ bit pattern of 16 bits in serial form to be correlated with the code pattern present in the commutator for a test of the matching properties between the two 16 bit words. As an example, a diagram of the verifier (address decoder) is shown in figure 53. An input line designated X_{40} *Received NRZ Address* accepts signal levels of "0" and "1." These levels are sequentially stored in the sixteen bit register. A 1 kc clock input propagates the code pattern in the register. The logical match between each bit is summed in a gate and a test for perfect correlation is made whenever an 80 μsec pulse is present on line X_{43} designated *Regenerated Address sync.* If a perfect match exists in

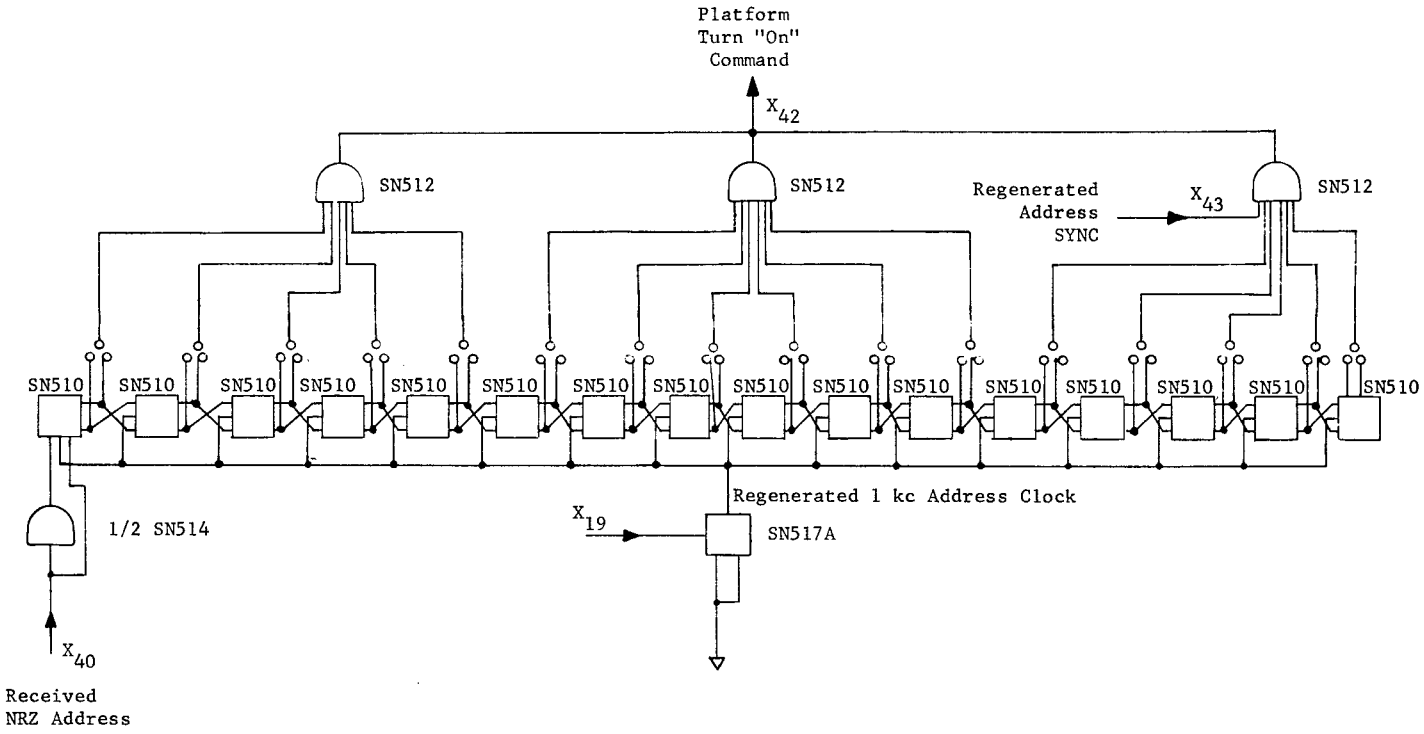


FIGURE 53.—*Block diagram of integrated address decoder.*

the two 16 bit words, a "1" of 80 μsec duration is applied giving the turn "on" command.

d. Range Detector—The range detector computes the round trip propagation time of the communication link between the satellite and the telemetry platform and thus determines the range of the platform. The range accuracy obtained from the time measurement is ± 0.5 km.

e. PCM Demodulator and Synchronizing Demodulator—This unit decodes the received NRZ bit stream, filters it from the noise, and reconstructs the synchronizing waveforms.

f. Transmitter—The transmitter is identical for use on the satellite, the platform, and command station except for frequency. The transmitter frequency is 400 Mc on the satellite and 465 Mc on the platform and command stations.

g. Receiver—The receivers used on the satellite, platform and command station differ only in frequency. The receiver frequency for the satellite is 465 Mc and 400 Mc on the platform and command station.

h. Analog to Digital Converter and Formatter—This unit converts analog signal inputs from the sensors and telemetry points to digital form and arranges these digital signals into a standard form known as a frame.

The IRL subsystem is intended to be used for one year with unattended operation in a space environment. Reliability is, therefore, vital. The IRL satellite-borne subsystem must also meet minimum space and weight requirements. Integrated circuits are ideally suited for these situations and are used whenever possible in the system. A laboratory breadboard of this system has been built and flight models are now being fabricated.

A/D CONVERTERS

Analog-to-digital conversion is an important function in space electronic systems. The several parallel efforts to apply microelectronics to A/D converters are resulting in interesting device developments described in Chapter 2 and in the application experience given below.

A/D CONVERTER FOR REENTRY TEDEMETRY SYSTEM

A microelectronic A/D converter for use in a pulse-code-modulation (PCM) telemetry system is being developed at Langley Research Center to meet weight, size, and reliability requirements. In a PCM system, the amplitude of sampled analog data must be determined and encoded to form a binary word representing its value. An A/D converter is required to achieve this. The electrical requirements of such an A/D converter are given in Table XIII, a block diagram in figure 54.

TABLE XIII.—*Electrical Requirements for Microelectronic Analog-to-Digital Converter*

Conversion rate	10 kilobits/sec
Input range	0 to 5 V
Accuracy	78 m V, 6 bits
Supply voltage	9, 6, and −3 Vdc ± 10%
Power consumption	250 mW
Reference voltage	7.5 V ± 0.05%
Data output level, logic "1"	6 V
Data output level, logic "0"	0 V

The input to the comparator is restricted to the 0-to-5 volt range supplied by a dc amplifier (see "Integrated Low-Level DC Differential Amplifier," Chapter 3).

The ladder adder in the circuit is a precision voltage divider supplied by a highly regulated voltage source and programed by transistor switches. It can provide 64 discrete levels in the 0-to-5 V range. Voltage levels are separated by 78 mV in this 6-bit system. The circuit is being fabricated using thick film techniques and matched transistors in flatpacks.

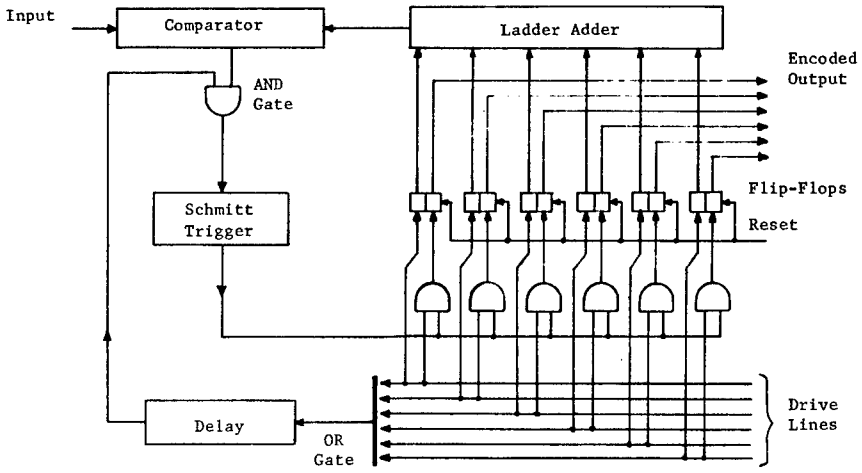


FIGURE 54.—*A/D converter for use in reentry telemetry system.*

The comparator is a difference amplifier. Its primary function is to determine if the voltage supplied by the ladder adder is greater than an unknown voltage representing analog data from the dc amplifier. If the ladder-adder voltage is greater, the comparator will produce an output of sufficient size to perform a logical function. If the unknown voltage is larger, the ladder adder will continue to step up its voltage to the comparator until the ladder-adder voltage is larger

and the required output is produced. The silicon integrated device developed to perform this function is discussed in "DC Comparator," Chapter 3.

The required AND gate, OR gate, flip-flop, and Schmitt trigger circuits are already available in silicon integrated devices.

A/D CONVERTER FOR SLOW-SCAN TELEVISION

A microcircuit A/D converter for use in planetary television experiments has been investigated by the Jet Propulsion Laboratories.

The linear ramp and counter method of conversion was chosen because of its relative simplicity and flexibility. However, ramp converters are not readily adaptable to high-speed operation, and they are susceptible to drift with temperature and supply voltage changes. The latter characteristic, however, can be used to correct for drifts in the television sensor and video amplifiers.

The converter is designed for slow-scan television signals having a frequency range from dc to 1.1 kc. The serial 6-bit PCM output signal is capable of driving a tape recorder or similar device and each 6-bit PCM word defines one of a possible 64 video levels. A block diagram of the converter is shown in figure 55.

A "start" pulse from the programer, together with the clock pulse, sets the gate flip-flop on and begins the generation of a positive going linear sweep in the ramp generator. Also, the gate flip-flop opens the gate between the clock and the scaler. The scaler counts the 160 kc clock pulses until the ramp voltage reaches the video input to the comparator. When the two voltages are equal, the comparator produces an output pulse which changes the state of the set-reset gates in the gate flip-flop. The next clock pulse then resets the gate flip-flop and terminates the gated clock sequence to the scaler. The ramp voltage is also terminated at this time. Closing the gate leaves the scaler

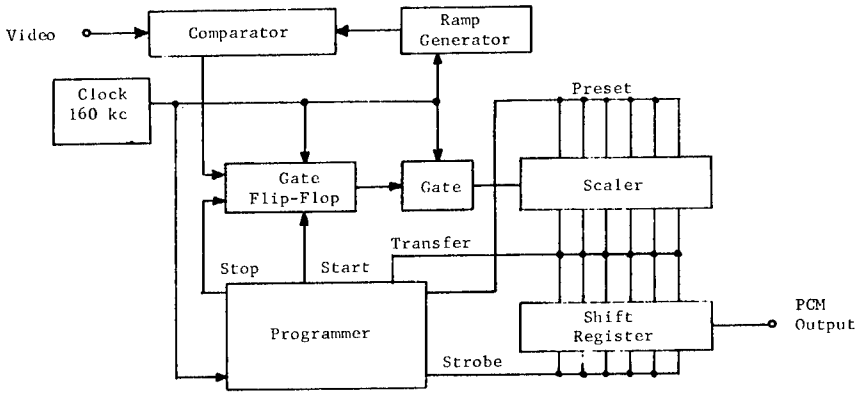


FIGURE 55.—*A/D converter for use in slow-scan television systems.*

with a total count proportional to the amplitude of the video signal. The binary data in the scaler are then transferred to the shift register and coded as a digital PCM output.

The converter was constructed using TI Series 51 solid circuits with the exception of the ramp generator and comparator. These units were constructed using conventional components, but they are now available in microcircuit form.

The performance of the converter over the operating range of $-55°$ C to $+125°$ C was excellent, proving the feasibility of using the ramp conversion method in low speed, low power applications.

SPACECRAFT TELEMETRY AND COMMAND SUBSYSTEMS

A study was performed for NASA headquarters [4] to identify the circuit functions and subsystems in spacecraft which are most likely to benefit from redesign to include microelectronics. Improved reliability and reduced power consumption were the advantages being sought. Attention was given to Nimbus, Syncom A, OGO, OAO, and IMP. The proposed microelectronic designs were compared to the conventional circuits on the basis of weight, size, power, number of interconnections, reliability and cost.

This microelectronics study resulted in the following conclusions most of which apply to low-speed, medium-power integrated circuits, since data available on hybrid and thin-film circuits did not provide sufficient information to assess their reliability for near-term use in spacecraft.

1. A considerable improvement in reliability of portions of spacecraft is not attainable by use of integrated circuits.
2. A ten-fold weight and volume reduction in applicable portions of the subsystems is possible.
3. One-third to two-thirds of the weight and volume of the telemetry and command subsystems can be eliminated through a redesign with microelectronic circuits.
4. Weight reductions, though substantial, represent only a small fraction of total spacecraft weight in spite of the corresponding saving in structure weight.
5. Microelectronic integrated circuits do not by themselves reduce the power consumption of spacecraft circuits.
6. A larger variety of low-power microelectronic circuits suitable for spacecraft use is still needed, such as switches, multiplexers, dual polarity gates and flip-flops.
7. Several common subsystems exist, which can be completely redesigned to permit possible use in several spacecraft.

[4] Arthur D. Little, Inc., Contract NASw–732, May, 1964.

8. Further system redesign is advantageous to implement trade-off possibilities realizable through microelectronics. Thus, one may trade weight reduction for increased power, more integrated circuits for reduced cable and connector wiring, decentralize signal conditioning and switching for increased redundancy and reliability, or reduce power consumption by power commutation with added switching circuits.

SHORT REPORTS

Brief descriptions of additional microelectronics applications are given in the following paragraphs.

RANDOM EVENT COUNTER

A data counting and storage subsystem has been designed by the Langley Research Center[5] for spacecraft applications. The unit records the random occurrence of micrometeoroid impacts and penetrations during flight. The subsystem includes the programing and logic functions required to read out, on command, the stored event counts. It has a storage capacity of 4096 events and the accumulated count can be read out at a maximum rate of around 250 kilobits/sec.

Figure 56 shows a simplified block diagram of the subsystem. The data storage counter which records the random events, will recycle

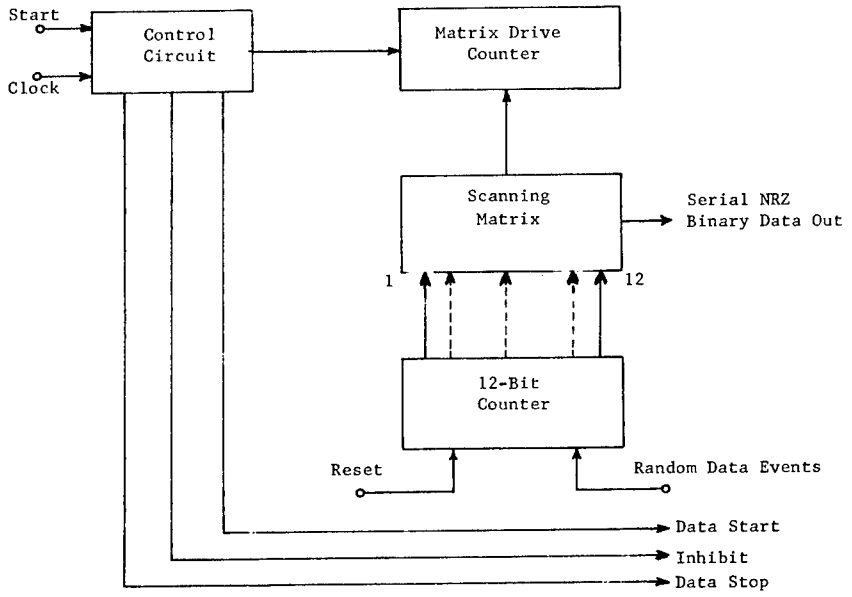


FIGURE 56.—*Block diagram of random event counter.*

[5] This unit fabricated and tested by Texas Instruments Incorporated.

when full and can be reset to zero by a command pulse. The scanner reads the counter in time sequence, on command, producing a non-return-to-zero (NRZ) serial binary data output. The packaged unit contains a total of 45 logic circuits using 35 Texas Instruments Series 51 Solid Circuits. The volume of the package is ½ cubic inch and the weight is ½ ounce. It is encapsulated with a clear epoxy resin and 11 external leads are provided for input and output terminals.

The prototype subsystems passed all tests including shock, vibration, temperature cycling, and simulated orbital flight operation. The system should prove useful in any application requiring the counting of random events.

SYNCHRONOUS PROGRAM CONTROL COUNTER

A 75 state synchronous counter for program control of a simple computer was designed and tested at the Jet Propulsion Laboratory.[6] It employs seven Fairchild J–K flip-flops (μL916) and ten gates (μL908, μL910, μL911). It has a maximum counting rate of about 8 Mc at room temperature. At a fixed clock rate of 10 kc, the counter operates successfully from -50 to $+125°$ C and is insensitive to large variations of clock pulse amplitude and shape. The power consumption of the counter at a supply voltage of 3 V is approximately 0.4 W.

APOLLO GUIDANCE COMPUTER

The reliability information generated in the development of the Apollo guidance computer (AGC) was discussed in Chapter 4 and the ground support equipment for the computer in "Ground Support Equipment," Chapter 5. This project at the Instrumentation Laboratory of M.I.T. and Raytheon is probably the largest user of microcircuits to date. Over 200 000 of the 3 input single NOR gate integrated silicon devices have been tested. Each computer uses 4000 of these gates. An advanced version of this computer will employ 2000 dual gates in integrated circuit flatpacks.

The AGC uses integrated circuits for all computer functions except memory, power supply, and the input-output interface circuits. In the logic no additional components such as resistors and capacitors are used. The basic clock rate of the computer is 1.024 Mc which is derived from a 2.048 Mc crystal-controlled clock.

The power supply is +3 Vdc $\pm$10 percent, the logic "0" is 0 to 0.55 V, and the logic "1" is 0.825 to 3.0 V. The average propagation delay of the gates is 0.25 msec. The maximum dissipation of each gate is about 15 mW.

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[6] "A Microcircuit 75-Counter," J. L. Way, Contract NAS7-100, JPL Technical Report No. 32-645.

Rigid qualification and inspection tests have been formulated both to insure reliability and compatibility between vendors.

APOLLO TV CAMERAS

Two TV cameras are being developed for use on the Apollo mission. One is a 4.2 lb. portable unit which employs silicon digital circuits (Signetics) for the sync and sweep circuits and 19 hybrid devices (silicon chips and film components—Motorola) for the video and linear circuits. The second camera is designed to operate on the lunar surface (-240 to $+260°$ F). Passive temperature control has allowed the use of single chip silicon circuits for the sync and sweep circuits and multichip hybrids in the analog circuits. The design of this camera is completed. Techniques developed on these projects should be directly applicable to commercial and industrial TV equipment.

SPACESUIT TELEMETRY AND COMMUNICATION

A spacesuit telemetry and communication system has been under development at the Manned Spacecraft Center. It combines a duplex mode allowing simultaneous transmission of voice and seven telemetry channels at 300 Mc and a secondary simplex mode for voice only at 260 Mc. The original 5 lb. model of this system was reduced to 1.6 lb. in the most recent cordwood version. It is being used as a test-bed for the development of high frequency thin-film circuits including thin film active devices.

SPACE INSTRUMENTATION DEVELOPMENT

An intensive evaluation of microelectronic techniques for space instrumentation was performed by Electro-Optical Systems Inc. for JPL.[7] Device fabrication techniques were developed and a reliability study was performed. This led to a developmental effort on an A/D converter similar in operating principle to that described in "A/D Converter for Reentry Telemetry System," Chapter 5. It was decided to employ a hybrid approach in which tantalum thin film resistors and capacitors are formed on the oxide coated surface of a silicon wafer in which diodes and transistors are fabricated. This design has been successfully breadboarded and the integrated circuits are being fabricated.

SPACE POWER SUPPLY

A three phase space power supply is being studied for JPL by Westinghouse. In this a small number of integrated circuits count down from a crystal controlled oscillator to provide the timing for a

[7] Contract JPL N–21449.

three phase ac output. A prime objective is to reduce interconnections to a minimum by putting as many circuits as possible on a silicon chip (2 chips for 46 logic elements is a goal). NAND logic is employed.

RANGING CODER

Four parallel development efforts on a ranging coder containing approximately 150 logic elements were sponsored by JPL. The purpose was to compare the performance of different device types as well as to develop the system. The received systems are being tested. Failures observed to date have resulted primarily from cracking of flatpacks.

MULTIPLEXING SWITCH

An n–p–n dual silicon phototransistor, switched by a gallium arsenide photon-emitting diode, is being developed for application in time division multiplexing systems. The photon coupling allows complete isolation between the control and signal paths. "ON" impedances of 20 ohms with a 50 μV offset have been obtained. Breakdown voltages across the switch are greater than 20 V for epitaxial designs.

MISCELLANEOUS

In addition to the applications above, a variety of other microelectronic systems are being developed. For the Saturn program, Marshall Space Flight Center is developing three such systems under contract: Westinghouse a radar altimeter, Martin a control signal processor, and Fairchild a switch selector. An A/D converter which uses the method of successive approximations is being developed for Goddard Space Flight Center by CBS using low power microelectronic techniques similar to those described in "Record and Playback Amplifiers," Chapter 5. Apollo systems which will employ microelectronics for a majority of functions include the digital decoding circuits of the command receiver (Motorola), the stabilization and control system (Honeywell), the fuel gauging system (Giannini Controls), and a PCM telemetry system. A subcontract to Space Technology Laboratories for the guidance computer for the lunar excursion module calls for 20 to 30 computers each of which will use over 1000 microcircuits.

The list can be enlarged to include every space electronic system that is being designed. The advantages to be gained from microelectronics almost make its use mandatory. The vast amount of application information generated by this is important to every user of microelectronics.

Chapter 6

Conclusions

APPLICATION AND DEVELOPMENT OF DEVICES FOR SPACE RESEARCH ARE SIGNIFICANT FACTORS IN THE DEVELOPMENT OF MICROELECTRONICS

In space research, requirements exist for small quantities of special microelectronic devices and for large quantities of standardized devices. The net result is that NASA, through its contractors, has been perhaps the leading user of microelectronic devices and will continue to be among these leaders. This has resulted in the generation of valuable applications experience for all users. NASA support of device development and technology is increasing, particularly for improved reliability. This support has resulted in the development of unique devices which are commercially available.

RAPID DISSEMINATION OF RESULTS MUST BE ENCOURAGED

The size and decentralized organization of NASA complicates the assembly of information on a specialized subject such as microelectronics. Every research center, several headquarters activities, and many contractors are actively producing important results. This information becomes available slowly through normal channels of publication and other dissemination processes. This report has succeeded in gathering together a significant percentage of the existing information, but continuing attention to the information dissemination process is recommended.

DEVICES MUST BE USED PROPERLY

While cost, power dissipation, size and weight are important, reliability is more important for space electronic systems. Microelectronic devices have proven to be very reliable when properly applied. Efforts spent in device evaluation and system design pay off in system performance.

SILICON INTEGRATED DEVICES ARE LEADING OTHER MICROELECTRONICS TYPES—TECHNOLOGIES WILL MERGE

Of the competing microelectronic technologies, all are capable of providing systems superior to those using discrete components since

they provide for batch processing of interconnections and put much of the assembly in the factory where it can be controlled. Silicon integrated devices are holding a lead over film circuits, but the technologies will most likely merge.

DEVICE DEVELOPMENT IS AHEAD OF APPLICATIONS AND THEORY

In reviewing the microelectronics field, an impression is obtained that applications are well behind device capabilities. Device design and fabrication are, in turn, reaching a limit of the current technology. While process improvement will allow new gains, the more significant advances must await the development of better theoretical techniques for understanding and predicting the physical phenomena and for the realization of system functions.

MANY INDUSTRIAL AND COMMERCIAL APPLICATIONS OF MICROELECTRONICS CAN BE STIMULATED BY NASA RESULTS

Almost all improvements in any state-of-the-art will eventually find their way into practical application. It is hoped that this Technology Survey and its successors will help to accelerate the transfer process—especially in respect to the contribution that NASA has made to the overall state-of-the-art.

Bibliography

Much of the information contained in this report is not available in the open literature so references are sparse. In addition to the general references given below, much information can be obtained from trade publications such as "Electronics," "Electronic Design," or "Electronic Industries." References given below which refer to specific sections of this report can be identified by the title.

KEONJIAN, E.: MICROELECTRONICS, Theory, Design, and Fabrication, New York, McGraw-Hill, 1963.

KHAMBATA, A. J.: Introduction to Integrated Semiconductor Circuits, New York, John Wiley and Sons, Inc., 1963.

DUMMER, G. W. A.: Microminiaturization, Proceedings of the AGARD Conference, Oslo, July 24–26, 1961, New York, Pergamon Press, 1962.

STERN, A. P., ed.: Special Issue on Integrated Electronics, Proc. IEEE 52, December 1964, p. 1395.

PARTRIDGE, J.; HANLEY, L. D.; AND HALL, E. C.: Attainable Reliability of Integrated Circuits for Systems Application, (Paper presented at Symposium on Microelectronics and Large Systems, Washington, D.C., November 17–18, 1964).

STERMER, R. L., JR.: Dielectric Formulations for Use in Processing Screened Ceramic Microcircuit Substrates, 1964 IEEE International Convention Record 12, Part 9, March 1964, p. 47.

LEONARD, W. F.; AND RAMEY, R. L.: Thin-Film Thickness from Theoretical Expressions for Conductivity and Isothermal Hall Effect, J. Appl. Phys. 35, October 1964, p. 2963.

GERSTENBERG, D., AND MAYER, E. H.: Properties of Tantalum Sputtered Films, Proceedings 1962 Electronic Components Conference, May 1962, p. 57.

SIKINA, T. V.: High-Density Tantalum-Film Microcircuits, Electronics Reliability and Microminiaturization 1, 1962, pp. 311–319.

MAISSEL, L. I.; HECHT, R. J.; AND SILCOX, N. W.: Techniques for the Fabrication of Low-Cost Tantalum Circuitry, Proceedings 1963 Electronic Components Conference, May 1963, p. 190.

PLEMENOS, F. A.; AND O'BRYANT, D.: Microelectronics Design of Digital GSE, NEREM Record, 1964, p. 60.

RESEARCH TRIANGLE INSTITUTE: Integrated Silicon Device Technology, Volume I—Resistance; by R. P. Donovan, ASD–TDR–63–316, Contract No. AF 33 (657)–10340, Durham, North Carolina, June 1963, AD–408 961.

RESEARCH TRIANGLE INSTITUTE: Integrated Silicon Device Technology, Volume II—Capacitance; by L. K. Monteith, ASD–TDR–63–316, Contract No. AF 33(657)–10340, Durham, North Carolina, October 1963, AD–423 148.

RESEARCH TRIANGLE INSTITUTE: Integrated Silicon Device Technology, Volume III—Photoengraving; by J. J. Wortman, ASD–TDR–63–316, Contract No. AF 33(657)–10340, Durham, North Carolina, January 1964, AD–603 715.

RESEARCH TRIANGLE INSTITUTE: Integrated Silicon Device Technology, Volume IV—Diffusion; by A. M. Smith, ASD–TDR–63–316, Contract No. AF 33(657)–10340, Durham, North Carolina, February 1964, AD–603 716.

RESEARCH TRIANGLE INSTITUTE: Integrated Silicon Device Technology, Volume V—Physical/Electrical Properties of Silicon; by R. A. Evans, ASD–TDR–63–316, Contract No. AF 33(657)–10340, Durham, North Carolina, July 1964, AD–605 558.

GODDARD SPACE FLIGHT CENTER: The Use of Solid Circuits in Satellite Instrumentation; by E. G. Bush, NASA TN D–1758, Greenbelt, Maryland, July 1964.

GODDARD SPACE FLIGHT CENTER: The Digital Tape Recorder Analyzer; by J. A. Sciulli, G–579N, Greenbelt, Maryland.

GODDARD SPACE FLIGHT CENTER: The MRIR–PCM Telemetry System—A Practical Example of Microelectronic Logic Design; by P. M. Feinberg, NASA TN D–2311, Greenbelt, Maryland, July 1964.

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