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According to initially submitted description of the proposed thermal diode for converting heat to electricity, proof of concept can be subdivided into the following three parts:
1. Proving that a semiconductor emitting layer compares favorably in terms of carriers injection with metal emitters both in the thermoelectric or Schottky mode.
2. Verifying limits of diffusive transport in the semiconductor gap in terms of recombination at elevated temperatures.
3. Proving compensation layer capability of blocking thermoelectric back current from the collector.

At this point, we have proved the compensation layer principle and that the recombination in InSb at elevated temperatures does not pose a serious problem. We also proved that semiconductor layer improves efficiency by a factor of four for the same material compared to thermoelectric regime. So far, predictions of the Numerical model developed earlier are sound. We tested energy converters that yielded results competitive with any known thermoelectrics.

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Authors: Peter Hagelstein and Yan Kucherov

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Authors: P. Hagelstein and Y. Kucherov

FINAL REPORT

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EXPERIMENTAL TEST APPARATUS

Test apparatus (see fig. 1) was built from standard mechanical parts used for laser applications. We used Coherent® 600x300 mm^2 stainless steel breadboard as a base. Basic vertical travel of a cold plate was realized with a rod mounting platform (1 foot travel). The cold plate was mounted with an assembly that allowed both precision vertical travel and three axis alignment relative to the hot plate on the bottom. This approach assured parallel plates. The semiconductor based diode is squeezed between the plates and can be damaged if parallelism is not assured. The assembly included a Newport® TSX-1D Translation Stage, Angle Bracket and M-RN-50 Three Axis Rotation Ball and Socket Stage. A water-cooled cold plate was custom machined of copper, polished to optical standards on the contact side and electrochemically coated with 2 microns of silver to prevent oxidation.
The hot plate was custom machined from a copper block for an Ogden Scientific cartridge heater rated to 400W and 1100^{0}C. The hot plate was mounted on a Coherent® Precision Vertical Stage (1" travel) with a Macor™ machined ceramic ring for thermal and electrical insulation. Side thermal insulation was provided by porous zirconia machined ceramic. Hot plate was also coated with 2 microns of silver. Heat flow measuring inserts could be mounted in the hot plate. Inserts were rods made of oxygen- free copper (silver coated) and had holes for thermocouple or RTD temperature sensors.

Overall, the test apparatus allowed 2" of vertical travel with varying precision, down to 1

micron, and up to 25 kilograms of vertical load. Maximum temperature on the sample was 400°C. Both cold and hot side plates had massive (100 mm^2 cross- section) welded fixed current leads. These fixed current leads were bolted to flexible copper (coated with silver) leads and then to a 600A - rated current switch that allowed bolting of custom- made load resistors (10^{-5} ohm to 1 ohm). Measured current path resistance without resistors could be as low as 30 microohms, depending on the thickness of a flexible lead. To prevent materials oxidation, the space between the cold and the hot plates could be constantly vented with argon gas. We used Kapton™ foil to contain the gas. Power to the heater was supplied with a Xantrex 300-3 DC power supply. To measure I-V curves we used Xantrex 7.5-125 DC power supply, that could be connected to the current circuit instead of a load resistor.

For temperature sensors we used a variety of Omega® thermocouples with Omega® DP 41-TC-GN digital readout or Keithley 2001 multimeters. For heat flow measurements we used Omega® RTDs with Keithley 2001 as a readout. Temperature sensors were calibrated with ice and mercury thermometer. In all cases, absolute measurements were better than +/- 0.5°C, and relative measurements approximately +/-0.05°C, which was due to some mismatch of different RTDs at elevated temperatures.

Typical sample thickness was 0.5-1 mm, which makes it difficult to measure temperature directly on the sample by an RTD or thermocouple. For this reason we used an infrared imaging camera by COMPIX®. This NIST- traceable camera allowed 0.1 degree accuracy in the 0-300°C temperature interval. Comparison with RTD measurements on a massive metal plate showed results matching within +/- 1 degree. For IR measurements the sample face had to be coated with a paint having emissivity close to unity in a wide spectral range. We used a thermal paint spray (Rustoleum) recommended by the camera manufacturer. As IR camera makes electrical measurements under argon cover difficult, we made electrical measurements first and IR next (without argon). Over time these measurements do not change much at temperatures below 200°C, suggesting that oxidation goes relatively slow on both samples and contacts and IR data is valid. The IR camera had spatial resolution of approximately 70 microns, which was adequate for our purpose, although there is some room for improvement. IR imaging proved to be very useful for complex samples, e.g., stacks made of different materials as it allows to calibrate interface temperatures measured by IR camera in terms of RTD temperature measured on a hot plate for each particular design. As expected, this calibration is linear. Interface temperatures usually are a little less than calculated, assuming an ideal thermal contact. This difference can be as high as 20 degrees and probably can be explained by the surface thermal resistance due to the phonon mismatch.

Electric measurements were performed with Hewlett Packard 34420 nanovolt / microohm meter which was connected in parallel with the load resistor. The same instrument in a four-wire configuration allowed to measure converter internal resistance with +/- 2 microohm accuracy when hot and cold plates were at the same temperature. Probing voltage at resistance measurements is 3 volts, compared to maximum converter output voltage of 0.1V. It means that, though with smaller accuracy converter resistance could be measured even at elevated temperatures. Typical voltage output was measured in millivolts and HP 34420 readings were compared to readings taken with Keithley 2001or hand- held FLUKE 79 multimeter. In all cases readings were within 0.01mV of each other. Ground loop problems, if any, were checked by

connecting all measuring instruments to a Toshiba 1400XL Plus (3 kW rated) uninterrupted power supply (UPS), which was then disconnected from the mains. No difference was noticed between mains / UPS- mains / stand alone UPS voltage supply to the HP 34420 within 10 microvolt reading. 10 microvolt difference was probably due to the temperature drift on a converter and not on the instrument. Electric current through the circuit was measured by an Amprobe® A-1000 Current transducer (clamp-on). The transducer was calibrated with a Xantrex 7.5-125 power supply and, at currents below 1A, with a Keithley 2001 multimeter. In the current range from 0.5 A to 120 A absolute readings were within 0.1A accuracy. Below 0.5 A readings were not reliable.

SAMPLE PREPARATION

Indium antimonide wafers were purchased from Wafer Technology, LTD (UK); Firebird Corp.(Canada) and Atomergic Chemetals Corp., NY, USA . We used 'Epitaxy-ready-grade' 2" in diameter wafers doped with tellurium and polished on both sides. Wafer thickness varied from 350 microns to 5 millimeters. Tellurium concentration varied from intrinsic to 3×10^{18} cm^{-3} for different wafers. Wafers were cut into pieces with a few square centimeters area and cleaned in alcohol and deionized water ultrasonic bath. Emitter layer was deposited by magnetron sputtering at the University of Utah material science department. High dopant (3×10^{19} and 10^{20} cm^{-3}) concentration InSb sputtering targets were purchased from Super Conductor Materials, Inc., NY, USA. Though 3E19 target works better than 1E20, in each case we were not able to determine crystallinity of the deposited layer. After the deposition samples were cleaved to needed size. Thick wafers (more than 1 mm) had to be cut with a diamond saw to the size and cleaned before the deposition.

Thermal and electric contact interface was formed by In - Ga eutectic. After experimenting with the In/Ga concentration ratio we found out that optimum composition is close to $In_{0.75}Ga_{0.25}$. This composition has a melting point around 35 ^{0}C and can be rubbed on the sample at room temperature. Friction provides sufficient temperature to melt the eutectic and rubbing removes surface oxide layer and contaminants. This composition is also less reactive than liquids with higher Ga concentration. For example, $In_{0.25}Ga_{0.75}$ reacted with InSb at 300^{0}C, but emitter layer was not formed by this reaction, meaning that Ga is a "bad" dopant for InSb in our case.

THERMAL DIODE BASELINE

To make a comparison between different thermal diode designs, we needed a reference point. A reference point does not have to be optimized in terms of diode performance, but must be convenient enough in manufacturing. For example, optimum wafer thickness is close to 2.5 mm, but samples like this are difficult to handle, because they are difficult to cleave and relatively expensive. Thick emitter layers are much more stable in time at elevated temperatures, but deposition of 15000 - 20000Å thick emitters requires few more hours of magnetron sputtering. Varying parameters are:

1. Gap (wafer) dopant concentration

2. Gap thickness
3. Emitter layer dopant concentration
4. Emitter layer thickness.

According to the Numerical Model, optimum gap dopant concentration is 7×10^{17} cm^{-3}. The closest off- the shelf wafer dopant concentration is 1×10^{18} cm^{-3}. We compared experimentally performance of thermal diodes with gap dopant (Te) concentrations of $2x10^{16}$, $3x10^{17}$, $1x10^{18}$ and $2x10^{18}$ cm^{-3}. Other parameters were the same. In accordance with numerical predictions, best output was with $1x10^{18}$ gap dopant concentration and we used it in our baseline samples.

We used 500-micron wafer thickness as they were cheap and readily available.

So far we have failed to create epitaxial emitter layer with $1x10^{20}$ cm^{-3} Te concentration. At best we got a polycrystalline layer with a very low barrier on the interface, resembling ohmic contact in behavior. When we used a sputtering target with $3x10^{19}$ Te concentration, there was some interface barrier between the emitter layer and the gap. We measured this barrier by external I-V curve and saw 30-60 meV barrier at room temperature . Barrier location (on a metal-semiconductor interface or internal) can be disputed, but this situation is better than no barrier at all, and we used this concentration as a baseline. According to the literature, the highest Te concentration ever achieved in a single crystal InSb is between 1.5 and $3x10^{19}$ [1].

Emitter layer thickness did not affect diode performance in a short time frame, i.e. 2-5 minutes at 200 - 250°C. At 400Å emitter layer thickness performance degradation can be seen after 5 minutes at 300°C (emitter layer diffuses away). A 10000Å emitter layer was stable at 300°C to within a fraction of one percent after approximately 6 hours. Assuming that a standard test requires less than 20 minutes at temperatures above 250°C, we compromised on a barrier thickness of 2000Å. It takes only 10 to 15 minutes to deposit such a layer at 180°C.

It is easy to reproduce thermal and electric contact behavior when the sample area is small, because requirements for the hot and cold plate parallelism are not that tight - In-Ga eutectic compensates for some deviations. For this reason we used samples with typical area of 1 - 3 mm^2, though the device allowed to test samples with up to a 1 cm^2 area. The pressure we used to compress our diode samples was estimated by a pressure sensitive film as 1 - 10 MPa. Visible scratches on the sample surface always worked as cleaving seeds, and samples failed under compression.. All scratches had to be avoided. All together our baseline diode had the emitter thickness of 2000Å {Te- $3x10^{19}$}, a gap thickness of 500 microns {Te- $1x10^{18}$}, an area 1-3 mm^2, and In-Ga contacts on both sides. These samples had a repeatable 0.65 $\pm$ 0.05% heat to electricity experimental conversion efficiency at 200°C or 1.2 $\pm$ 0.05% at 300°C (ratio of the electric output to the heat flow through the diode).

COMPENSATION LAYER

The compensation layer was supposed to block back current from the collector. Irrespectively of how this layer is created, its thickness must be larger than the carrier tunneling length in order to avoid an ohmic contact situation. It requires the layer to be thicker than 200-300Å.
We used two different approaches:
1. Deposition of an intrinsic layer of the same semiconductor material as the gap.

2. Ion implantation of p-type impurity to match n-type carrier concentration in the gap.
Both methods have their specific advantages and disadvantages.

Intrinsic layer deposition is cheaper, but it must be thick enough to ensure a long diffusion time of the gap dopant (in our case - Te) into the intrinsic layer. Another problem with this layer is that it must be epitaxial to avoid additional interface barrier that may directly affect carrier transport. Epitaxial layer can be easily achieved by MBE, but this deposition method is inherently expensive and offsets cost advantage. Magnetron sputtering of InSb can also achieve epitaxial layer, but significant efforts must be invested into the substrate and target cleanness etc.

Ion implanted layer is immune to the main gap dopant diffusion because its concentration is the same in implanted region as everywhere else. The problem is the diffusing out of the implanted species. Because of that this layer also must be thick.

We used both methods to prove that compensation layer principle works.

Intrinsic layer: We used InSb sample with the same design as a baseline diode (500 microns thick, $1x10^{18}$ cm^{-3} Te concentration, and the same emitter layer). 400Å of InSb with electron concentration ~ $1x10^{14}cm^{-3}$ were deposited on the collector side of the diode by magnetron sputtering. It was assumed that we had congruent sputtering, i.e. deposited layer had the same composition as a sputtering target. Deposition temperature was 180- 200°C, supposedly enough to achieve epitaxial growth. Tests showed the same performance at 200°C as a baseline diodes, but at 300°C the results consistently showed 1.4 % efficiency, which is 17 % gain over the baseline and outside of the error bar. Possible explanation for this behavior is that at 200°C the deposited layer to some extent blocks the back current, but it also creates an internal barrier that hinders direct current transport. At 300°C due to the temperature dependence, the barrier height it is smaller, and beneficial side of the layer is more pronounced.

Ion implanted layer: The ionization energy of the donors supplied by Te in InSb is 50meV. By accident, ionization energy of acceptors introduced by vacancies in InSb are close to 50meV [3]. This fact creates an opportunity to build a compensation layer by creating vacancy concentration matching the initial Te dopant concentration in InSb. Inert gas ions are well suited for such a task because they are electrically neutral and number of vacancies created by each ion can be large. The number of vacancies is defined by the ion dose per unit area D [ions / cm^2] and the number of vacancies created by a single ion V. V is a function of the ion energy E, or V = V(E). The number of vacancies N(E) = D*V(E). Vacancy concentration C in this case depends on the ion range in the material R, which is also a function of the ion energy: R = R(E). For a given type of ions:

$$C(E) = \frac{D \cdot V(E)}{R(E)} \qquad (1).$$

For a compensated layer C(E) must be equal to the main dopant concentration (n), or

$$D = \frac{n \cdot R(E)}{V(E)} \qquad (2).$$

R(E) and V(E) were modeled using TRIM-91 computer code (Ziegler et al., IBM, 1991) for InSb target and Ar^+ ions. Modeling results are shown in fig. 2 and fig. 3. Using figures 2 and 3 and formula (2) one can define the dose needed to create a compensation layer over a wide range of ion energies in a n-type InSb, doped to concentration (n). We assume that (n) is large enough compared to intrinsic carrier concentration in InSb so that the intrinsic part can be neglected. Ion implantation creates a vacancy concentration profile, which is more pronounced at the last 20-30% of the ion range. In principle this profile can create an additional (unwanted) internal barrier. We decided to address this problem later and use low ion energies so that profile span is smaller than tunneling distance in InSb, which is typically 100-150Å. This situation corresponds to approximately 400Å ion range or 40keV for Ar ion implantation. 400Å is not enough to form a layer stable in terms of vacancy diffusion at elevated temperatures, but it is sufficient to prove the compensation principle for a short time period. Initial $1x10^{18}cm^{-3}$ Te concentration in a baseline diode, is in reality, the average number over the whole grown crystal. Manufacturer's tolerance was sufficiently tight ~10%, but to avoid a dopant concentration variation problem we used a range of doses overlapping +/-50% of the initial value. Baseline diodes were implanted on the collector side at Core Systems, Santa Clara, CA with 40keV Ar ions. Doses were 0.5, 0.75, 1.0 and $1.4x10^{10}cm^{-2}$. Dose accuracy was 5%. Calculated compensation dose was $0.69x10^{10}$ cm^{-2}. Test results for implanted samples at hot plate temperature 200°C are shown in fig. 3. Compared to a non- compensated diode (dose equals zero on the figure) a $0.75x10^{10}$ dose shows 85% performance improvement. This dose was the closest to the calculated dose. At 300°C all the implanted samples showed the same performance as non-implanted samples, suggesting that the vacancies diffused out during the slow temperature rise (approximately 2 hours from 200 to 300°C). Estimated diffusiing out time for vacancies in InSb at 300°C, $1x10^{18}$ cm^{-3} concentration and 400Å layer thickness is ~3-5 minutes. The graph on fig. 4 proves the principle of a compensated diode.The 85% performance improvement is close enough to the predicted by the numerical model factor of two improvement.

GAP THICKNESS OPTIMIZATION FOR THE InSb DIODE

At 300K the reference book numbers for electron recombination length in n-type InSb are 11 ± 1mm. 11 mm is much more than the thermal diode gap thickness and this is not a problem, but at elevated temperatures it can be a problem.

We addressed the problem by experimentally measuring one plate efficiency with the plate thickness as the only changing parameter. We used our baseline diode emitter - 2000Å InSb doped with Te to $3x10^{19}cm^{-3}$, deposited by magnetron sputtering at 180°C. Plates had the same Te- dopant concentration - $1x10^{18}cm^{-3}$. Wafer thicknesses were 360 microns, 0.5mm,1 mm and 5 mm. Samples made out of a 5mm thick wafer could not be cleaved and had to be cut by a diamond saw. Tests results for 300°C emitter temperature and 19°C collector temperature are

shown in fig. 5. Fig. 5 shows that the optimum gap thickness is somewhere between 2 and 3 mm thick. The drop in efficiency at 5 mm thickness is probably due to the carrier recombination.

CONVERTER STACKS

The converter efficiency is the ratio of electric output to the heat flow through the structure. If the hot and cold side temperatures are kept the same, the heat flow at a constant thermal conductivity should decrease linearly with the sample thickness. The e+lectric output within the recombination length should stay the same and scattering mechanisms should impede diffusive carrier transport. At elevated temperatures scattering effects can be as strong as recombination, the difference is that recombination eliminates injected carriers and the corresponding current stops completely. Scattering introduces more resistance but carriers still contribute to the current transport. An interesting situation appears when two or more converter plates are stacked together with an intermediate metal layer. In this case carriers are injected on the hot side of the first plate, migrate to the collector, recombine, and the process repeats itself at lower temperature on the second plate and so forth. The advantage of this design is that recombination in the gap becomes less important, because each gap is relatively thin. Now the current limiting step is the barrier height at lower temperatures. If the barrier height dependence on the temperature for a given material is negative, the current can self adjust and we may have a structure with the same electric output and much lower heat flow, i.e. the efficiency goes up. In the case of a positive barrier height dependence on the temperature, the barrier height can be regulated artificially by varying emitter layer doping. Another positive feature of this structure is that each interface gives an additional thermal resistance, which further reduces the heat flow.

The experiments with stacking of two plates showed a strange effect - electrical output sometimes went up with more than a factor of two drop in the heat flow. Corresponding experimental output I-V curves for one plate and two stacked plates are shown in fig. 6. The difference in the output efficiency is roughly 75% in favor of stacked plates. There are quite a few of ways to explain this behavior, all of them are disputable, so none will be presented here, before an adequate model is developed. An experimental graph of stacked InSb converter efficiency as a function of a number of identical plates is shown in fig. 7. Each plate was 500 microns thick with 10^{18} cm^{-3} Te concentration and 2000Å emitter layer of InSb doped with Te to $3x10^{19}$ cm^{-3} on the hot side of each plate. Interestingly enough, when the plate orientation is lost, the difference in efficiency for a four plates converter is nearly 5 times compared to the oriented situation. The non- oriented situation can be considered as the case of a thermoelectric converter and gives performance comparison. Fig. 6 shows that we are getting diminishing return when the number of plates increases past four. Power density also goes down, dropping approximately to 1 W/cm^2 in a 4-plate configuration. Remembering that plates did not have a compensation layer, which allows another 80% gain in efficiency, these stacks become competitive with the best thermoelectric materials in 300°C temperature region. Temperature dependence of the efficiency for a stack of four plates is shown in fig. 8, efficiency peaks between 300 and 330°C.

CONVERTERS BASED ON $Hg_{1-x}Cd_xTe$ AND RELATED COMPOUNDS

According to the initial theoretical explanation, normalized conductivity (figure of merit for a semiconductor thermionic converter) for HgTe is roughly three times better than the corresponding numbers for InSb. Addition of cadmium makes the figure of merit still higher, in theory up to nearly eight times better than InSb at certain cadmium concentrations and temperatures. Recalculated efficiencies, in this case, can be higher than 40% of an ideal Carnot cycle even without a compensation layer. Building an emitter layer on $Hg_{1-x}Cd_xTe$ (MCT) can be difficult or easy, depending on the method used. According to [2], indium metal reacts with MCT even at room temperature to create a heavily doped (n-type) layer. We used this fact to create an emitter layer. Likewise, a compensation layer can be built by using a reactant that gives acceptor impurity (e.g. copper). Comparison of various emitters with n-type and p-type impurity showed nearly ten times difference in converter performance. We used a sample cut from 0.5 mm thick wafer with basic composition of $Hg_{0.86}Cd_{14}Te$ (from Lockheed - Martin infrared sensors division). This material is not at the optimum Cd concentration, but still 4.5 times better than InSb. One side was coated with a thin $In_{0.75}Ga_{0.25}$ alloy layer, and this sample was tested as a converter. The graph of efficiency in terms of an ideal Carnot cycle versus temperature is shown in fig. 9. Efficiency peaks at approximately 150°C and is significantly higher than any known thermoelectric converter efficiency.

A stack consisting of an InSb plate with a 1 mm thickness and a MCT plate made as described in the previous paragraph allowed to expand the same kind of the ideal Carnot cycle percentage (close to 40%) to 270°C and absolute efficiency close to 17%. The stack performance is shown in fig. 10 and 11. Sandwich interface temperature was calibrated as a function of a hot plate temperature for this particular design using an infrared imaging device. An example of thermal image together with a corresponding temperature profile for the stack mentioned above is shown in fig. 12. The calibration curve obtained in this way is shown in fig. 13. Both plates were not optimized in terms of thickness, composition and no compensation layer was used in this case. In principle, another 10% of an ideal Carnot cycle efficiency are expected when all these features are in place, with operating temperatures up to 300 - 330°C, making it close to the theoretical limit.

MCT is relatively unstable material which loses mercury at elevated temperatures, on top of that, diffusion stability of impurities at elevated temperatures is also questionable. It seems that both of these problems can be solved by depositing a diffusion barrier of Yb metal [4]. The diffusion barrier may allow higher operating temperatures and efficiencies.

We have also tested converters made of HgSe with various emitters. At temperatures higher than 80 - 100°C MCT shows a higher performance, but below 80°C, HgSe reacted with Sn to form an emitter layer wins. Strangely enough, this material does not work with the emitter layer made with In dopant. Preliminary results show promise for high efficiencies at near room temperatures for a converter based on this material.

THERMIONIC REGIME

We have sufficient proof that a compensation layer will be beneficial to the converters performance. On the other hand, for InSb material the difference between a situation with the emitter layer and without is not that pronounced. In most cases this difference is only about 20-

30% in efficiency. There can be many reasons for a small difference, one of them is that we were not able to deposit an epitaxial emitter layer with high dopant concentrations. Different types of carrier injection are possible. It can be thermal excitation over the internal barrier (preferred), excitation over the Shottky barrier on the metal-semiconductor interface, tunnelling and conductance. The last one is the thermoelectric regime. For our design the behavior of a thermoelectric regime has specific features that allow it to discriminate from the carrier injection modes. Typical literature situation is when the output voltage goes up close to linear with the temperature, and the output current flattens out at relatively small temperatures. In a thermionic regime (carrier injection mode) the output voltage V=V(T) curve is also close to linear, but output current should not flatten out over the large temperature range. MCT is a convenient material to check the difference, because the gap is only 60 meV (x=0.14) at room temperature compared to 180 meV for InSb. Temperature dependence of the MCT gap is such that it increases much faster than k_BT and if the Shottky injection was the main mechanism, the output current growth slope (dI/dT) should decrease with the temperature.

We used a $Hg_{0.86}Cd_{0.14}Te$ sample first on a copper substrate (hot side) and than the same sample on the same substrate but with In-Ga layer in between. MCT reacts with Cu after 100°C forming a p-type impurity. It reacts with In-Ga at room temperature to form an n-type impurity and emitter layer. In-Ga forms a little bit better electric contact. Measured sample resistivity at room temperature was 0.0923 ohms compared to 0.1027 ohms for the copper contact. Test results for both cases are shown in fig. 14. Output voltage was the same within 1% over the whole temperature range, below 60°C output currents are the same (within the error bar). As the temperature goes up current flattens out for the Cu-emitter and goes up for the InGa. The difference is nearly four times at 120°C. This behavior effectively proves carrier injection by thermal excitation over the internal barrier and shows that it can be a few times more efficient compared to a thermoelectric mode for the same material.

EMITTER LAYER FOR InSb DIODE

The baseline diode had a gap of InSb doped with tellurium to $1x10^{18}$ cm^{-3} and an emitter layer with 2000Å thickness doped with tellurium to $3x10^{19}$ cm^{-3}. The emitter layer was deposited by magnetron sputtering at 180°C from sintered InSb target. InSb allows congruent deposition, i.e. it does not decompose during the deposition, as known from the literature. This statement is probably not true for Te in InSb. Even if it was true, emitter layer is thin enough for diffusion to be a major effect in Te redistribution. Thin layer provides for high concentration gradient and larger relative concentration profile wash-out in the same time, compared to thicker layers. To understand Te concentration profiles baseline diode was analyzed by time-of-flight secondary ion mass-spectroscopy (SIMS) at Accurel, Inc. Concentration profile is shown in fig. 15. It seems that Te precipitates on the surface and concentration gradient is largest between 500 and 1000Å from the surface. Corresponding barrier should be regarded relative to the electron tunneling length in InSb which is 150-250Å. It means that the barrier is largest where the concentration drop is largest over the same distance. In our case it is approximately one order of magnitude over 250Å. The barrier height $U = k_BT \ln(n^*/n)$, where n^* - higher concentration, n - lower concentration, T - absolute temperature and k_B -Boltzmann's constant. In our case $U \sim 2.3$

k_BT, which is consistent with ~ 60 meV barrier measured by external I-V curve measurements at room temperature. Calculated optimum barrier height is 4-7 kT and we have only marginally suitable barrier.

We tried to build a barrier by different method. 4000Å of pure tellurium were deposited on the same gap InSb material at 180°C. Now Te diffusion creates a layer with high concentration. Apparently this method works better, because a thermal diode with this barrier shows increase in performance nearly 2.5 times compared to the situation with the old emitter. Both output voltage and current are improved.

FUTURE THERMIONIC GAP MATERIALS

Numerical model allows to estimate performance for various materials. Some of the performance curves as a fraction of an ideal Carnot cycle versus temperature are shown in fig. 15. These calculations assume that optimum emitter is formed on the hot side and the cold side is kept at 300 K. At low temperatures Bi shows best performance, but Bi is a semimetal and barrier formation is somewhat problematic, though it can be achieved in principle. Apparently Cd_3As_2 is a material of choice for various applications. It has nearly the same efficiency as MCT (x=0.14) but it is a much more stable and less poisonous material. In principle it can be used up to 880 K, where it has a phase transition. At this temperature, calculated absolute efficiencies could be as high as 33-35% and competitive with internal combustion engines. Unlike InSb and MCT this material is less known and building an emitter layer represents a research project.

High end temperature materials suitable for our approach are basically unexplored. Materials of interest for temperatures higher than 600°C can include rear-earth hexaborides and $C_{1-x}N_x$, which is reported to be a semimetal. Barrier building task can be separated from the efficient gap material, in other words, barrier can be made of semiconductors different from the gap material. If the emitter layer is thin enough, its thermodynamic efficiency is not that important.

Another approach is to engineer a gap material on the basis of metal-insulator or metal-semiconductor nanoparticles. This approach is attractive for many reasons. To name few, conductance activation energy known for these materials can be used as an emitter barrier, elements used in the material can be environmentally friendly, etc.

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Thermionic Sample Test System

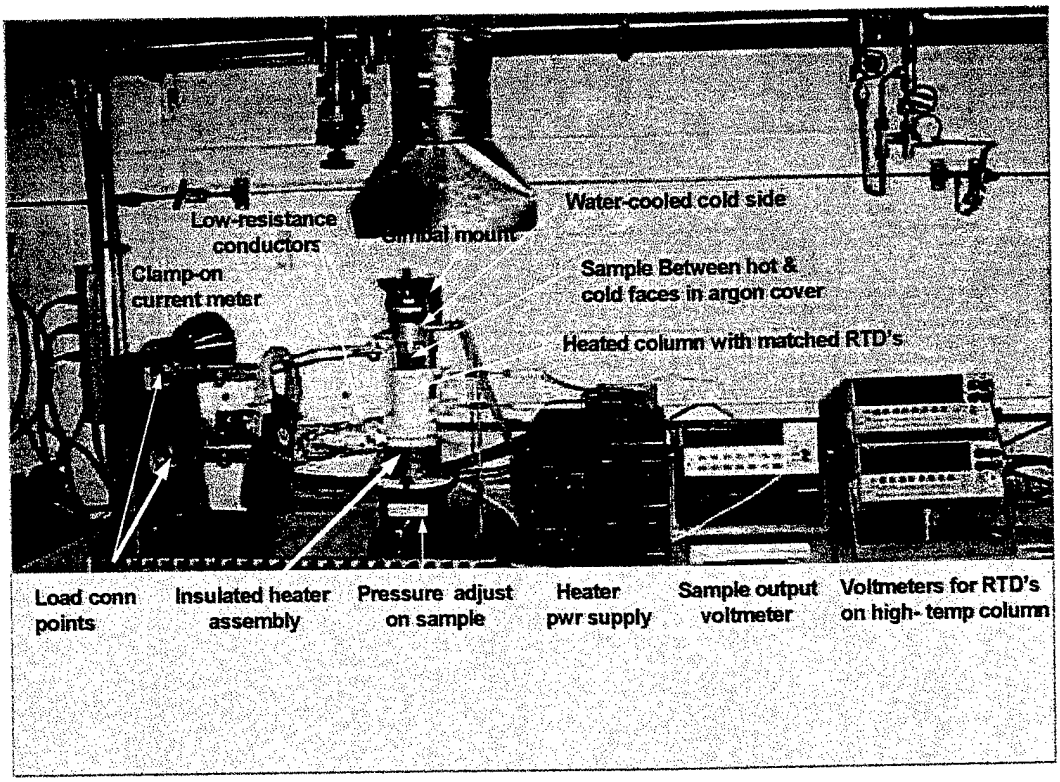


Fig. 1

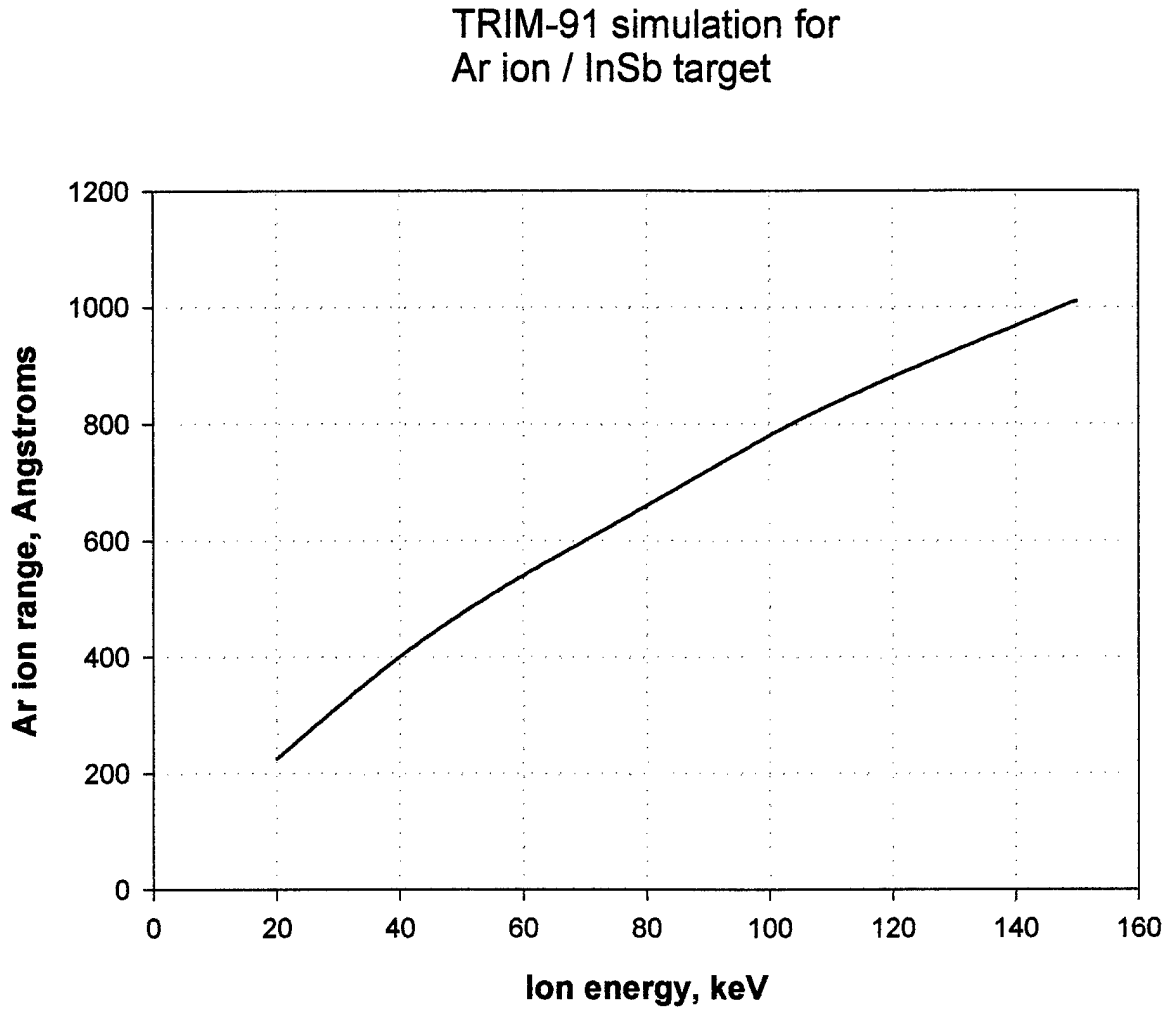

TRIM-91 simulation for
Ar ion / InSb target
Ar ion range, Angstroms
1200
1000
800
600
400
200
0
0
20
40
60
80
100
120
140
160
Ion energy, keV

Fig. 2

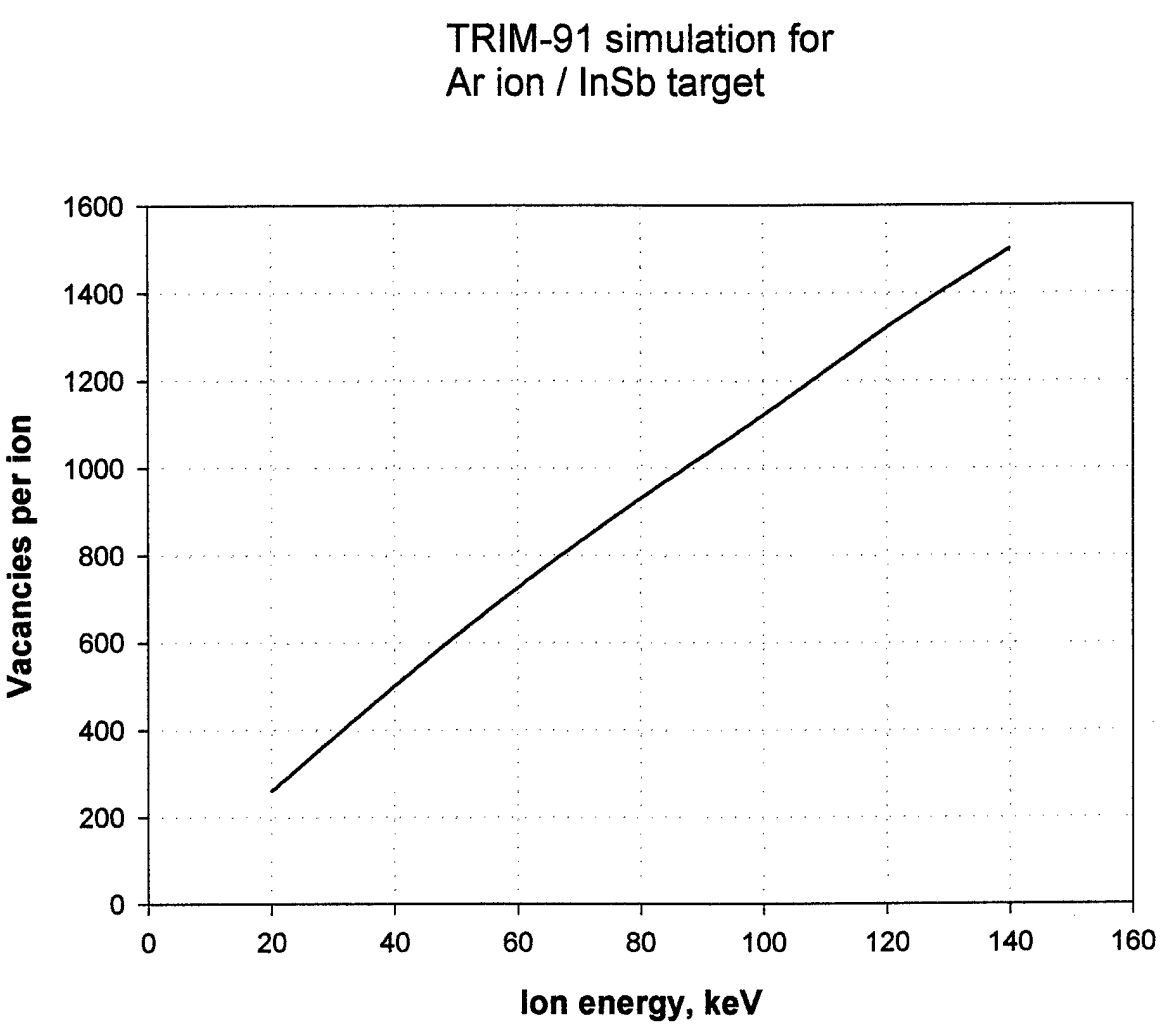

TRIM-91 simulation for
Ar ion / InSb target
Vacancies per ion
1600
1400
1200
1000
800
600
400
200
0
0
20
40
60
80
100
120
140
160
Ion energy, keV

Fig. 3

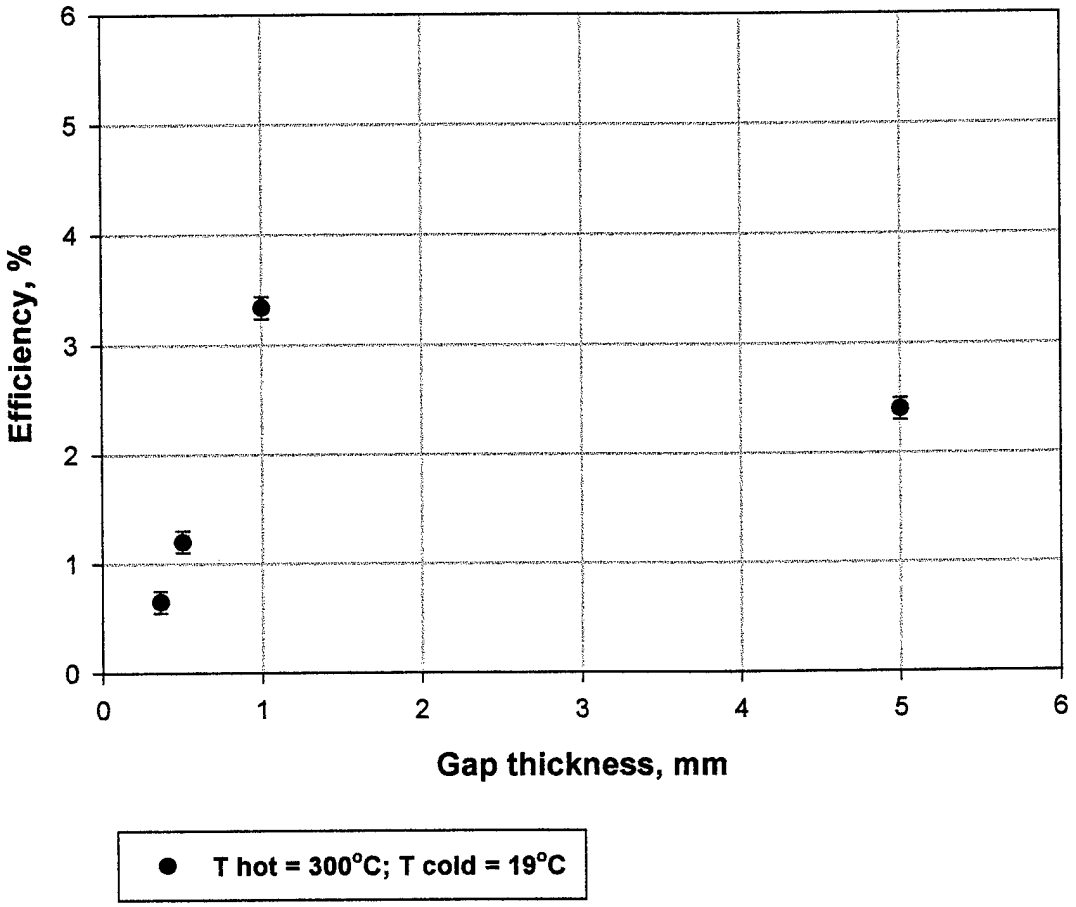

Gap: InSb {Te 1x10^18cm^-3}, 2000A emitter layer
InSb {Te 3x10^19cm^-3}
Efficiency, %
0
1
2
3
4
5
6
Gap thickness, mm
T hot = 300°C; T cold = 19°C

Fig. 4

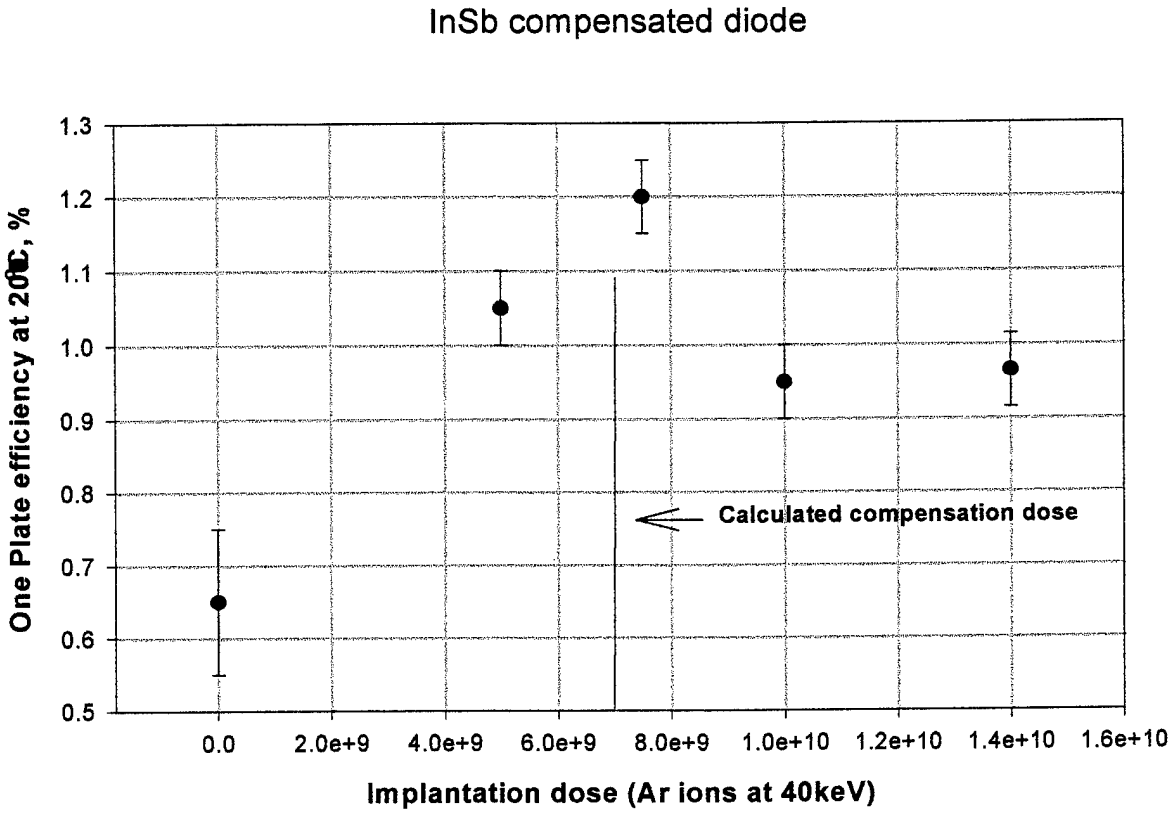

InSb compensated diode
One Plate efficiency at 20K, %
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
Calculated compensation dose
0.0
2.0e+9
4.0e+9
6.0e+9
8.0e+9
1.0e+10
1.2e+10
1.4e+10
1.6e+10
Implantation dose (Ar ions at 40keV)

Fig. 5

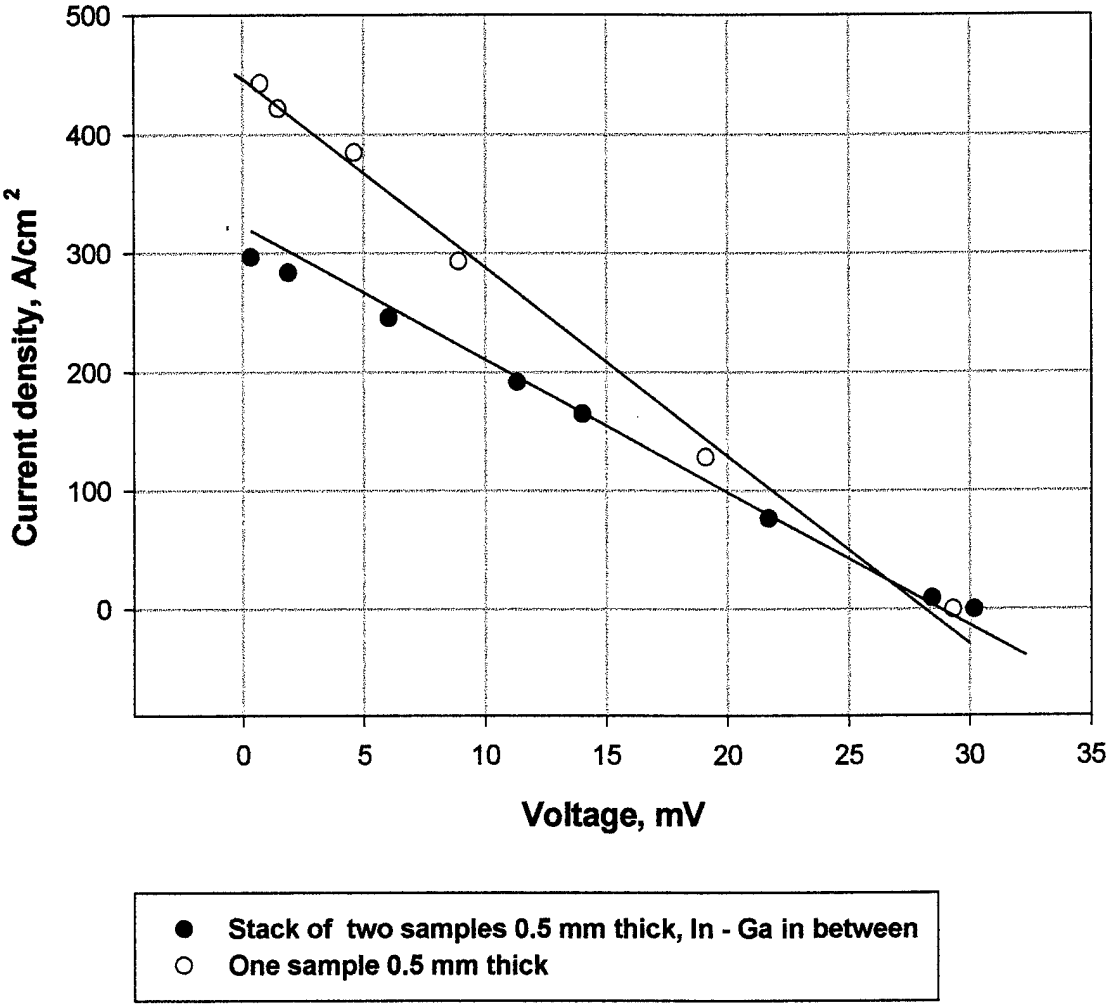

In Sb samples (2000A Te-3x10^19 0n 0.5 mm 1x10^18
T hot = 300^0C, T cold = 11.5^0C; 5/12/2000
Current density, A/cm^2
500
400
300
200
100
0
0
5
10
15
20
25
30
35
Voltage, mV
Stack of two samples 0.5 mm thick, In - Ga in between
One sample 0.5 mm thick

Fig. 6

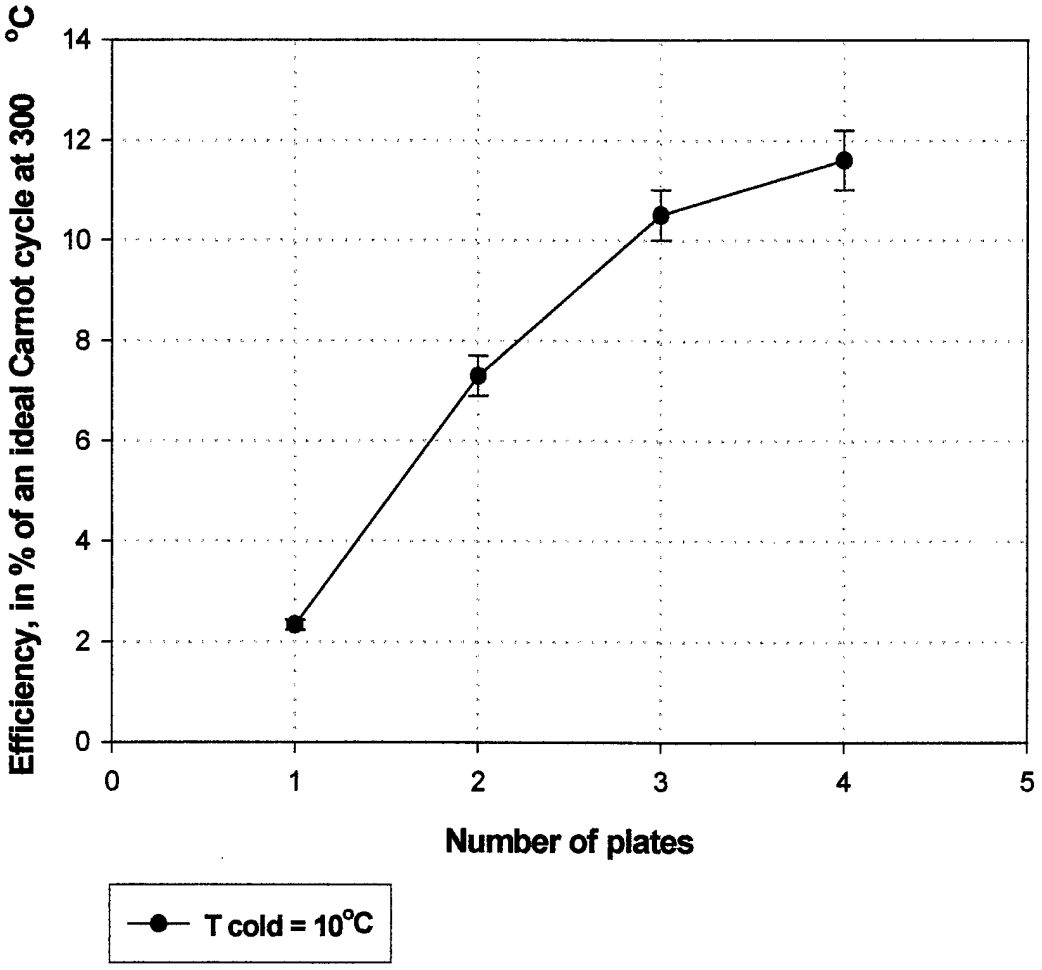

Efficiency, in % of an ideal Carnot cycle at 300 °C
14
12
10
8
6
4
2
0
0
1
2
3
4
5
Number of plates
T cold = 10°C

Fig. 7

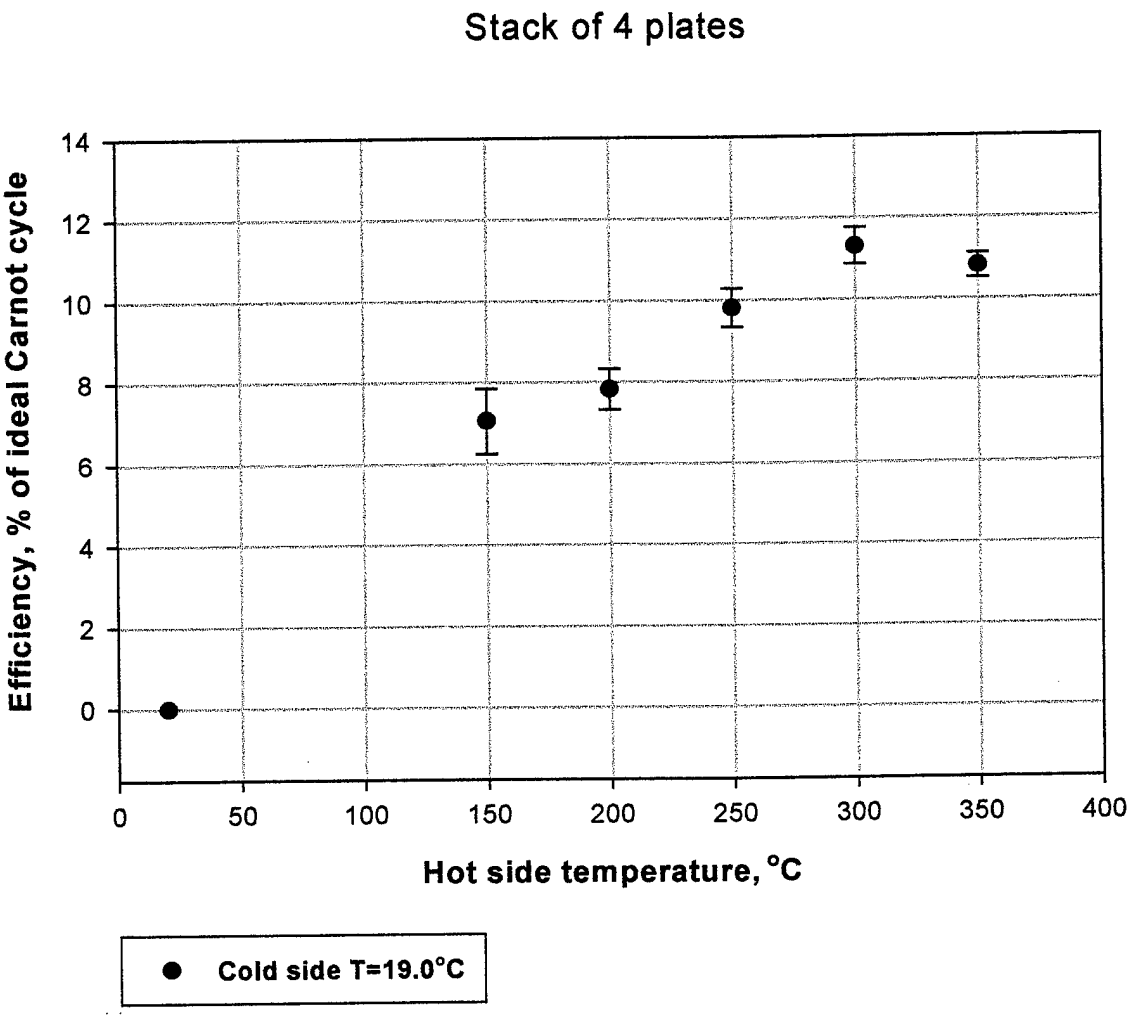

Stack of 4 plates
Efficiency, % of ideal Carnot cycle
14
12
10
8
6
4
2
0
0
50
100
150
200
250
300
350
400
Hot side temperature, °C
Cold side T=19.0°C

Fig. 8

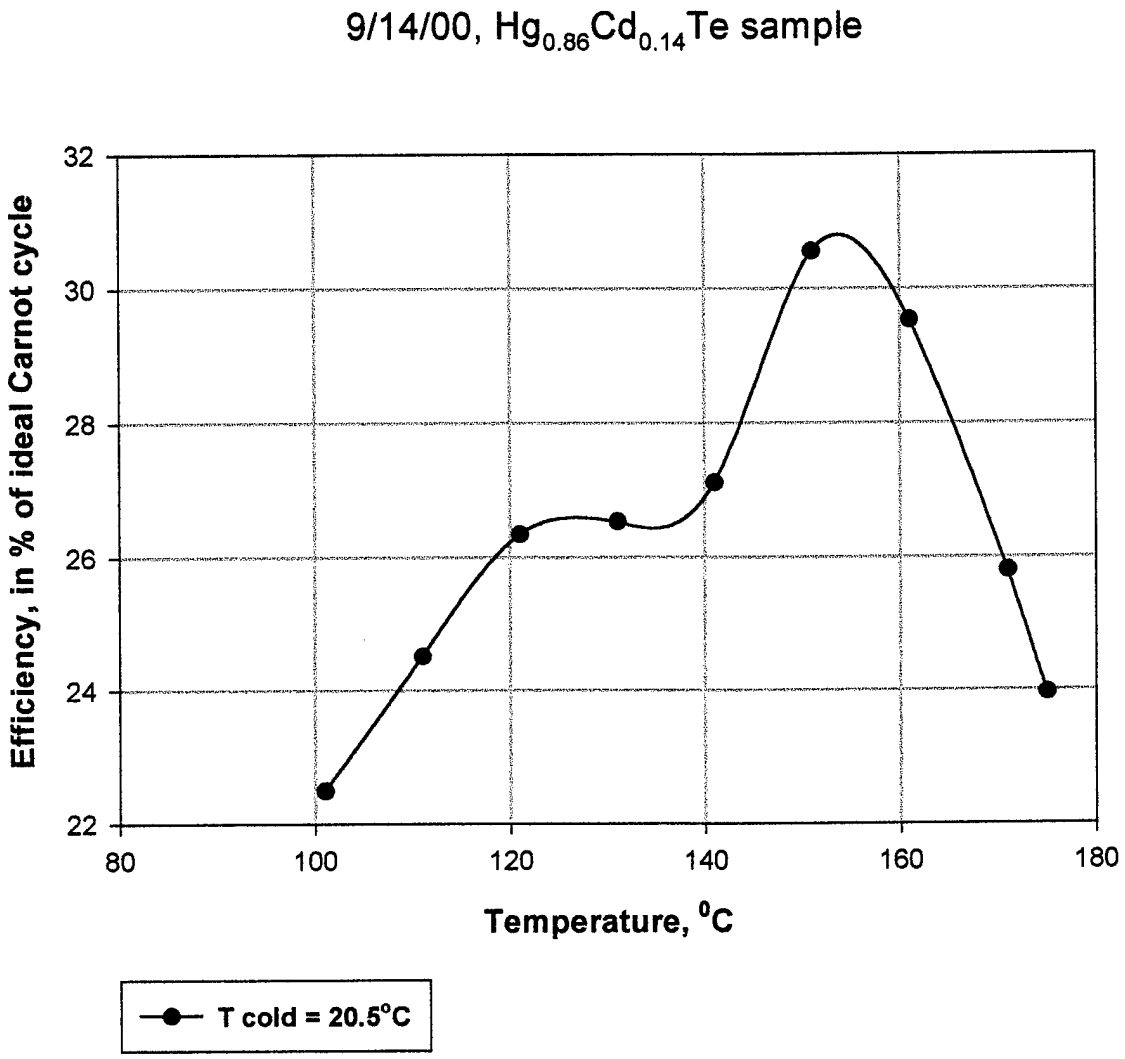

9/14/00, $Hg_{0.86}Cd_{0.14}Te$ sample
Efficiency, in % of ideal Carnot cycle
32
30
28
26
24
22
80
100
120
140
160
180
Temperature, ^0C
T cold = 20.5°C

Fig. 9

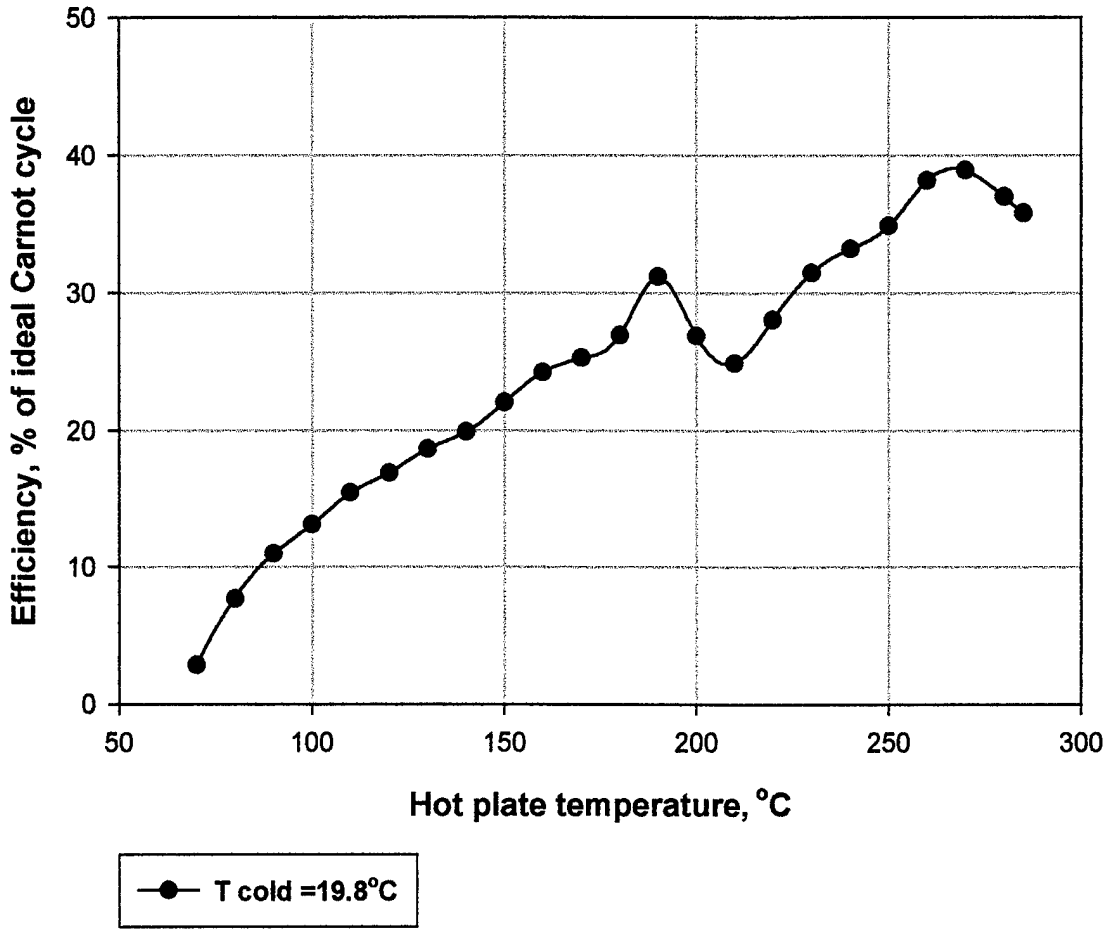

9/27/00 experiment corrected by IR camera
Efficiency, % of ideal Carnot cycle
0
10
20
30
40
50
50
100
150
200
250
300
Hot plate temperature, °C
T cold =19.8°C

Fig. 10

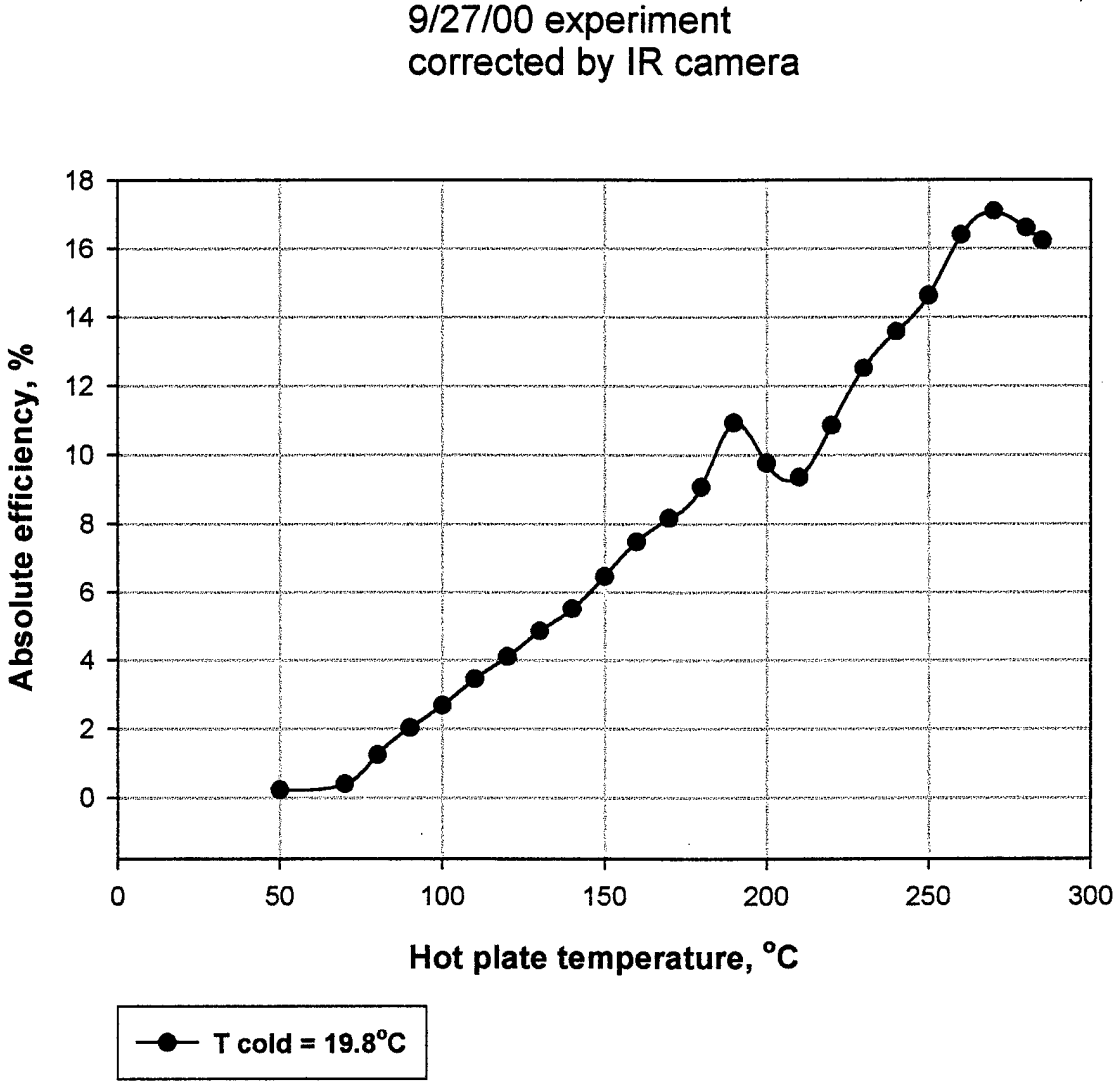
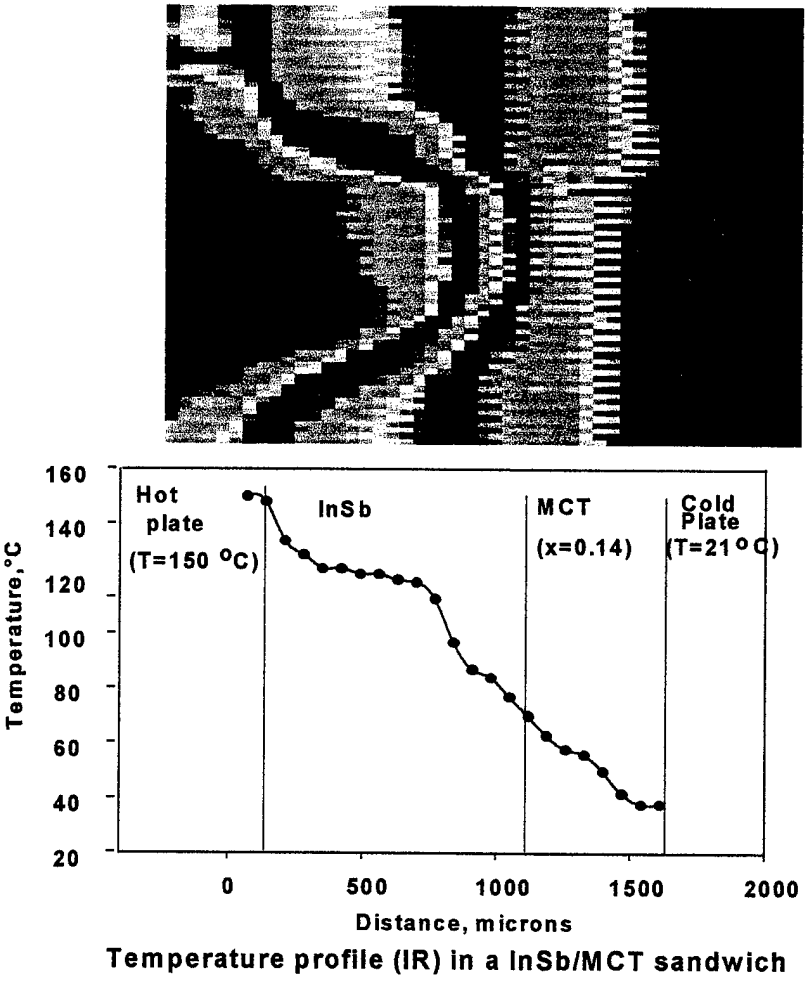

9/27/00 experiment
corrected by IR camera
Absolute efficiency, %
18
16
14
12
10
8
6
4
2
0
0
50
100
150
200
250
300
Hot plate temperature, °C
T cold = 19.8°C

Fig. 11



Temperature profile (IR) in a InSb/MCT sandwich

Fig.12

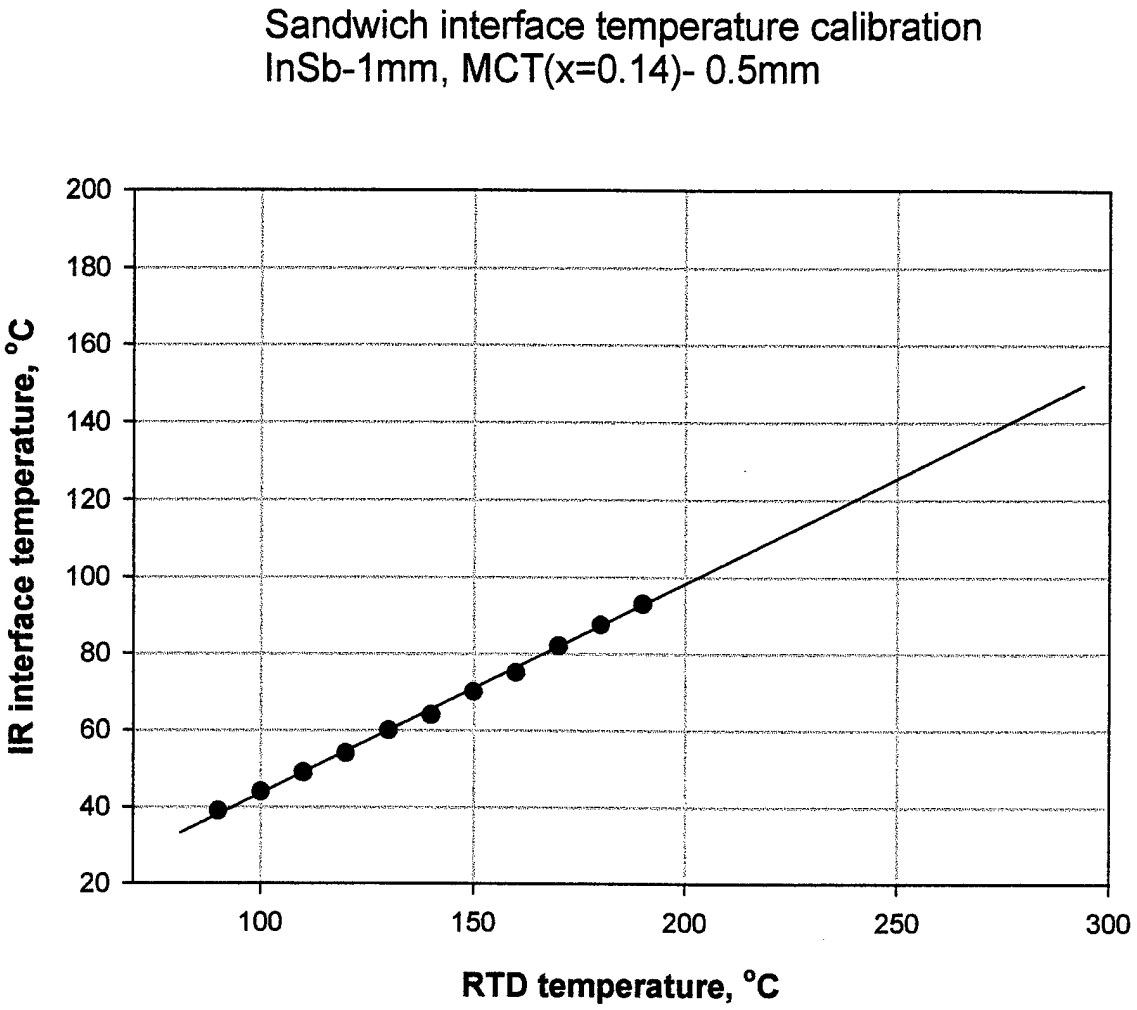
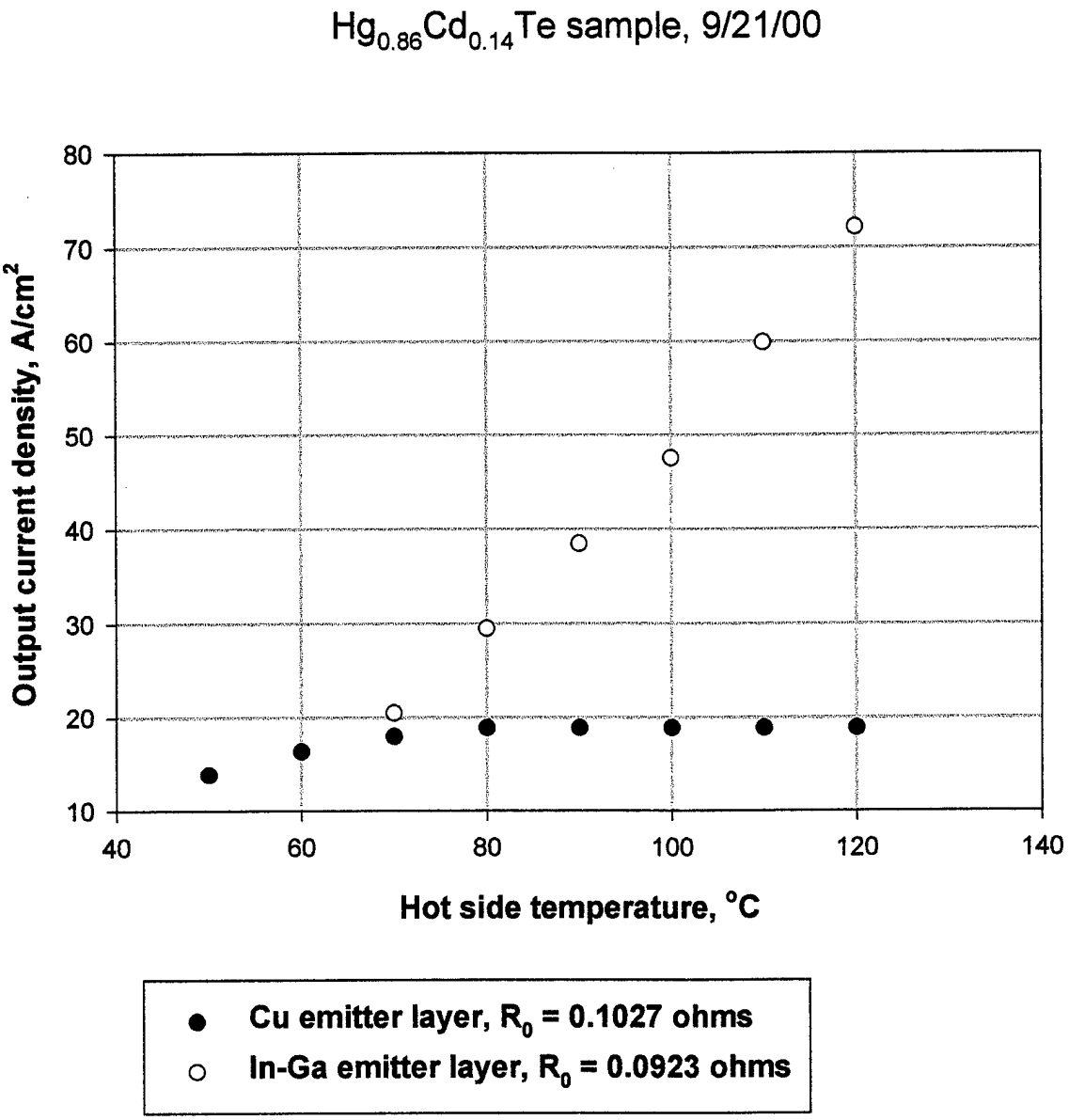

Sandwich interface temperature calibration
InSb-1mm, MCT(x=0.14)- 0.5mm
IR interface temperature, °C
200
180
160
140
120
100
80
60
40
20
100
150
200
250
300
RTD temperature, °C

Fig. 13


$Hg_{0.86}Cd_{0.14}Te$ sample, 9/21/00
Output current density, A/cm^2
80
70
60
50
40
30
20
10
40
60
80
100
120
140
Hot side temperature, °C
Cu emitter layer, R_0 = 0.1027 ohms
In-Ga emitter layer, R_0 = 0.0923 ohms

Fig

Fig. 14

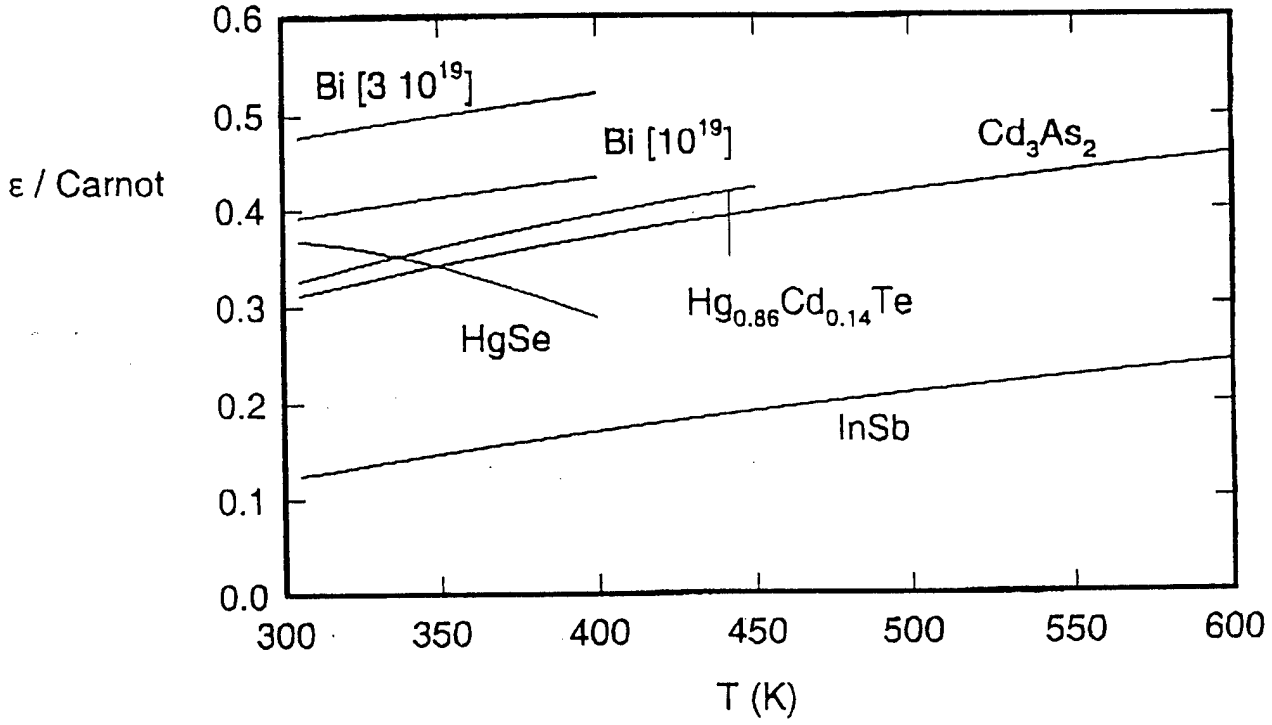

ε / Carnot
0.6
0.5
0.4
0.3
0.2
0.1
0.0
300
350
400
450
500
550
600
T (K)
Bi [3 10^19]
Bi [10^19]
Cd3As2
Hg0.86Cd0.14Te
HgSe
InSb

Fig. 15

Appendix

Abstracted from:

Measurement of the Efficiency of Solid-State Thermionic Converters

Ray Radebaugh, Peter Bradley, Mike Lewis
Physical and Chemical Properties Division
National Institute of Standards and Technology
Boulder, Colorado 80305

CONCLUSIONS

Based on these measurements of InSb samples, we conclude that the results reported by ENECO for this material appear to be correct. The somewhat higher electrical output they achieved appears to be simply a matter of achieving better electrical contact to the sample than what we were able to achieve in the limited time we had available to us. A certain amount of practice is required to achieve these high electrical conductances. Our results for the electrical output were continually increasing as we gain more experience and improved our alignment techniques. Our results are within a factor of two compared with the ENECO measurements whereas the heat flux measurements are in very good agreement with their results. There is the one uncertainty regarding the ratio of electricity and heat flux. Generally a lower current flux would also imply a lower heat flux if the contact had a high electrical resistance. More measurements are required to fully answer that question.