GEORGIA TECH GT–VTF
VLSI DESIGN VERIFICATION DOCUMENT

VLSI DEVELOPMENT REPORT
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GUIDANCE, NAVIGATION AND CONTROL
DIGITAL EMULATION TECHNOLOGY LABORATORY

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COMPUTER ENGINEERING RESEARCH LABORATORY

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Atlanta, Georgia 30332–0540

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INTRODUCTION

There are eleven (11) Georgia Tech VLSI designs (see Table 1) in the AHAT Program. Each of these designs has been produced by Georgia Tech using the Genesil Silicon Compiler. Each design has passed the design verification process at Silicon Compiler Systems / Mentor Graphics and each has been fabricated in a bulk CMOS process (fabrication of certain chips was not complete when this document was released). Each of the Georgia Tech designs listed in Table 1 is being delivered to USASDC and to the Harris Corporation for conversion and fabrication in a rad–hard process. The program under which this work is done is AHAT (Advanced Hardened Avionics Technology). This document includes design information for the Georgia Tech temporal filtering chip, GT–VTF.

Table 1. Georgia Tech Chip Set for AHAT

Design	DV Passed	Tape Delivered	Fabricated	Tested
GT–VFPU/1A	01/17/89	08/03/90	05/19/89	04/04/90
GT–VSNI	01/17/89	05/23/90	04/14/89	04/04/90
GT–VSM8	01/17/89	06/08/90	05/06/89	04/04/90
GT–VCTR	02/08/90	07/12/90	07/13/90	07/27/90
GT–VCLS	01/26/90	07/12/90	07/13/90	07/27/90
GT–VSF	09/12/89	07/19/90	07/13/90	07/27/90
GT–VTHR	12/11/90	02/15/91	03/01/91	03/08/91
GT–VDAG	02/22/91	02/25/91	05/01/91	
GT–VIAG	03/08/91	03/11/91	05/07/91	
GT–VNUC	07/23/91	07/05/91		
GT–VTF	07/24/91	08/01/91		

Table 2. Georgia Tech Documents Sent for AHAT

No.	Document / Software Item	Date Sent
1.	Georgia Tech GT–VFPU : VLSI Design Verification Document	05/15/90
2.	Georgia Tech GT–VSNI : VLSI Design Verification Document	05/23/90
3.	Georgia Tech GT–VSM8 : VLSI Design Verification Document	06/08/90
4.	Georgia Tech GT–VCTR : VLSI Design Verification Document	07/12/90
5.	Georgia Tech GT–VCLS : VLSI Design Verification Document	07/12/90
6.	Georgia Tech GT–VSF : VLSI Design Verification Document	07/19/90
7.	Data Address Generation GT–VDAG : Programming Model Document (v.2)	01/03/91
8.	Instruction Address Generation GT–VIAG : Programming Model Document (v.1)	01/03/91
9.	GT–EP I/O Interface Specification : Note	01/17/91
10.	EP, SNI, SM8 Interconnection Specification : Note (v.1)	01/28/91
11.	Georgia Tech GT–VTHR : VLSI Design Verification Document	02/15/91
12.	Georgia Tech GT–VDAG : VLSI Design Verification Document	02/25/91
13.	Georgia Tech GT–VIAG : VLSI Design Verification Document	03/11/91
14.	GT–FPU Operating Speed Test Document	04/16/91
15.	Staggered Row Focal Plane Array Analysis Document	05/01/91
16.	GT–EP Pascal Compiler : Note (v.1), Source Code, and Program Examples	05/06/91
17.	Instruction Address Generation GT–VIAG : Programming Model Document (v.2)	06/07/91
18.	Georgia Tech GT–VNUC : VLSI Design Verification Document and User Guide	07/05/91

No.	Document / Software Item	Date Sent
19.	EP, SNI, SM8 Interconnection Specification : Processor Design Document (revision to earlier Note sent on 01/28/91)	07/08/91
20.	GT–EP Pascal Compiler : Software User Document (revision to earlier Note sent on 05/06/91)	07/08/91
21.	GT–Seeker/Scene Emulator to GT–GN&C Processor Interface Document	07/19/91
22.	Georgia Tech GT–VTF : VLSI Design Verification Document and User Guide	08/01/91

Table of Content

GT–VTF : Temporal Filter

1.Design Verification Checklist

The DV checklist is attached in Appendix A.

2.Functional Description

This section describes briefly the function of the chip and the modules at core level. First, the organization of all modules of GT–VTF is shown in figure 1. The floorplan of GT–VTF also follows the similar scheme of figure 1, see figure 30.

2.1. Module tfil_1

This module takes signal processing (SP) synchronization information (***begin_row_in, end_row_in, begin_frame_in and end_frame_in***), delay and send them to various locations of GT–VTF to control GT–VTF and the next SP chip(***begin_row_out, end_row_out, begin_frame_out, end_frame_out***) to synchronize SP chips. The schematic for this module is shown in figure 2.

2.2. Module tfil_2

This module generates row and column address (***row_address[9:0] and col_address[9:0]***) and $\overline{CS}$ signals (***mm0_cs[1:0], mm1_cs[3:0]***) for GT–VTF to access its external RAM. The schematic is shown in figure 3.

2.3. Module tfil_3

This module counts four chip clock (***x4_clock***) cycles.. Pulses at every one of these four clock cycles is generated (pulse signals are ***s4_0, s4_1, s4_2, s4_3***) and then, distributes to various modules for controlling purpose. The circuit diagram of **tfil_3** is shown in figure 4.

2.4. Module pre_tfil_4

This module buffers signals ***address[7:0]*** to prevent these signals being the bottleneck that hinders GT–VTF's performance. See figure 5.

2.5. Module tfil_4

This module decodes address commands issue by the host. It also collects GT–VTF parameters that store at various locations of the chip and gives them to the host. If the address requires to read a parameter,

it will simply be output through this module, see figure 6 and 7. In addition, this module also contains manufacturing test logics. Some of the test mode can be activated by toggling the JKFFs in the sub–module **test_ctrl** , see figure 8.

The module **tfil_4** contains three sub–modules: two random logics and one parallel datapath. The detail drawing for these modules are in figure 6, 7 and 8.

2.6. Module tfil_5

This module decodes addresses and sends the resultant signal to the various modules for the executions. The circuit diagram of **tfil_5** is shown in figure 9.

2.7. Module tfil_13

This module contains registers to store ***row_address[9:0]*** and ***col_address[9:0]*** which can be programmed by the host via module **tfil_5**. The schematic of this module is shown in figure 10.

2.8. Module tfil_14

This module is responsible for updating GT–VTF parameters. It produces a signal to release the parameters of the first set of registers to the second set of registers. So, this parameter can be used to filter pixel at the beginning of the next frame. Two updating scheme are in this module: One is to change the parameters (eg. filter coefficients) and reset frames as to assume all the previous states are zero. And the second scheme is to change the parameters but continue to use the previous states which are stored in the external RAM. See figure 11.

2.9. Module stage0

This is the first stage of the second order filter house. this module contains two sets of almost identical processing elements to process the input pixels. It outputs two results: One output is stored in the external external memory for the later feedback and the other will be used as the input for the second stage.

2.9. 1. Module stage0 / load_sigs

Module to determine if the parameter registers in the modules tfil_6 or tfil_7 of stage0 needs to be loaded with the new values. This is achieved by ANDed the load signal with ***address[4]*** signal as shown figure 12.

2.9. 2. Module stage0 / tfil_6

This module contains registers to store A coefficients and outputs shift–truncation bits for the first stage. Two stages of registers are used here to store these parameters. With this scheme the parameters can be updated in one register set and also processing pixel at the other.

Tfil_6 contains 3 parallel datapaths and one random logic block and they ar e show in figure 13, 14, 15 and 16.

2.9. 3. Module stage0 / tfil_7

This module contains registers to store B coefficients and outputs shift bits for the input of the next stage. Since it contains the same structure as **tfil_6**, therefore, only the upper level signal I/O block diagram is shown, figure 17.

2.9. 4. Module stage0 / tfil_8

Multiplication and addtion blocks for calculating intermediate feedback states. The result is a 34 bits signed–magnitude fixed point which will be fed to **tfil_10**. See figure 18.

2.9. 5. Module stage0 / tfil_9

Multiplication and addition blocks for calculating intermediate output for the next stage. The result is a 34 bits signed–magnitude fixed point which will be fed into **tfil_11**. See figure 19.

2.9. 6. Module stage0 / tfil_10

Shifts and truncates the value produced from **tfil_8**. The result will be sent to outside of GT–VTF and store in the external memory for later use. See figure 20.

2.9. 7. Module stage0 / tfil_11

By using the barrel shifter, the output from **tfil_9** is shifted, truncated and then sent to **tfil_16**. See figure 21.

2.9. 8. Module stage0 / tfil_15

This is the input stage for module **stage0**. Input pixels, feedback states and their coefficients are combined here and fed into modules **tfil_8** and **tfil_9** to carry out the arithmetics. See figure 22.

2.9. 9. Module stage0 / tfil_16

This is the output stage for module **stage0**. Output that is produced by B coefficients in **tfil_11** gets to be delayed here for one chip clock cycle and then send out to the next stage for further processing. See figure 23.

2.10. Module stage1

The upper level input and output diagram is shown in figure 24. This module is pretty much the same as **stage0** excepts for the sub–modules:

stage1 / tfil_6	Extra logics for the manufacturing test and notice that tfil_7 has the same construction. See figure 25 and 26.
stage1 / tfil_15	It contains minor difference from **stage0 / tfil_15.** Since the input arrives to stage1 later than to stage0, additional DFFs are used and serve as delay elements. See figure 27.

3.Signal Descriptions

Input and output signals of GT–VTF are described below. All signals are active high except those name start with "***n_***" and not chip select signals ***mm0_cs[1:0]*** and ***mm1_cs[3:0]***. Signals are divided into three groups according to their functionalities and the connections to the external devices: Host, SP chips and external RAM. The wiring diagram for these three groups is shown in figure 28. The

3.1. Host Side

The signals below are connected to the host.

Signal Name	Type	Purpose
n_reset	IN	Reset line.
address	IN	Filter command entry.
data	IN/OUT	Filter parameters input and output.
ods_ids[3:0]	IN	Device select signals from the host.
devices_ready	OUT	Acknowledgement to the host.
oe_n_ie	IN	Signal from the host to indicate host output enable.

3.2. Signal Processing Side

Signals here are used for GT–VTF to communicate with other signal processing chips.

Signal Name	Type	Purpose
pixel_clock in	IN	Pixel clock.
begin_frame_in	IN	Input rows and frames sync. signals.
end_frame_in	IN	
begin_row_in	IN	
end_row_in	IN	
begin_frame_out	OUT	Output rows and frames sync. signals.
begin_row_out	OUT	
end_frame_out	OUT	
end_row_out	OUT	
p_data_in	IN	Pixel data in.
p_data_out	OUT	Pixel data out.

3.3. External Memory Side

These signals control external memories. Signals ***mm0_cs[1:0]*** and ***mm1_cs[3:0]*** are active low because they are not chip select signals.

SIgnal Name	Type	Purpose
state_0[15:0]	IN/OUT	State zero data, stored and recalled.
state_1[15:0]	IN/OUT	State one data, stored and recalled.
row_address[9:0]	OUT	Memory address.
col_address[9:0]	OUT	Memory address.
mm0_csel[1:0]	OUT	Not chip select signal for two memory banks.
mm1_csel[3:0]	OUT	Not chip select signal for four memory banks.
mm1_control	IN	One of the address line for controlling *mm1_csel.*
n_write_en[1:0]	OUT	Not write enable for two sets of RAM memories.

4.Final Notes

The DV tape contains a file named "gtvtf.tar.Z". This file is about 35MB in size, and the database, when uncompressed, is about 247 MB. To restore it, do the following.

1. Go to the location on the destination machine and destination directory and execute "tar xv".
2. After gtvtf.tar.Z has been extracted, type "zcat gtvtf.tar.Z | tar xvf –".

5.Block Diagrams and Schematics

Block diagrams and schematics are included in appendix B.

6.Timing Diagrams

Timing diagrams for GT–VTF are found in the GT–VTF user guide.

7.Pin Description

Wire–Bond Pads/Connector Pins for GT–VTF Chip is shown in figure 29 and 30.

Pin #	Signal Name	Abbrev. Name	Pin Loc.	Pad Type	Timing
1	FALSE		B1	CORNER VSS	
2	p_data_out[0]	PDOUT0	C1	DATA OUT	SB
3	p_data_out[1]	PDOUT1	E1	DATA OUT	SB
5	p_data_out[2]	PDOUT2	F1	DATA OUT	SB
6	p_data_out[3]	PDOUT3	G1	DATA OUT	SB
7	p_data_out[4]	PDOUT4	H1	DATA OUT	SB
8	p_data_out[5]	PDOUT5	G2	DATA OUT	SB
9	TRUE		D2	EDGE VDD	
10	FALSE		E2	EDGE VSS	
11	p_data_out[6]	PDOUT6	F2	DATA OUT	SB
12	p_data_out[7]	PDOUT7	G2	DATA OUT	SB
13	p_data_out[8]	PDOUT8	H2	DATA OUT	SB
14	p_data_out[9]	PDOUT9	D3	DATA OUT	SB
15	p_data_out[10]	PDOUT10	E3	DATA OUT	SB
16	p_data_out[11]	PDOUT11	F3	DATA OUT	SB
17	p_data_out[12]	PDOUT12	G3	DATA OUT	SB
18	p_data_out[13]	PDOUT13	H3	DATA OUT	SB
19	p_data_out[14]	PDOUT14	E4	DATA OUT	SB
20	p_data_out[15]	PDOUT15	F4	DATA OUT	SB
21	p_data_out[16]	PDOUT16	G4	DATA OUT	SB
22	TRUE		H4	EDGE VDD	
23	FALSE		H5	EDGE VSS	
24	state_1[0]	ST1_0	J4	DATA IO	SB,VB
25	state_1[1]	ST1_1	K4	DATA IO	SB,VB
56	state_1[2]	ST1_2	L4	DATA IO	SB,VB
27	state_1[3]	ST1_3	M4	DATA IO	SB,VB
28	state_1[4]	ST1_4	J3	DATA IO	SB,VB
29	state_1[5]	ST1_5	K3	DATA IO	SB,VB
30	state_1[6]	ST1_6	L3	DATA IO	SB,VB
31	state_1[7]	ST1_7	M3	DATA IO	SB,VB
32	state_1[8]	ST1_8	N3	DATA IO	SB,VB
33	state_1[9]	ST1_9	J2	DATA IO	SB,VB
34	state_1[10]	ST1_10	K2	DATA IO	SB,VB
35	state_1[11]	ST1_11	L2	DATA IO	SB,VB
36	state_1[12]	ST1_12	M2	DATA IO	SB,VB
37	TRUE		N2	EDGE VDD	
38	FALSE		P2	EDGE VSS	
39	state_1[13]	ST1_13	J1	DATA IO	SB,VB
40	state_1[14]	ST1_14	K1	DATA IO	SB,VB
41	state_1[15]	ST1_15	L1	DATA IO	SB,VB
42	mm1_csel[0]	N_CS1_0	M1	DATA OUT	SB
43	mm1_control	CS1_CTRL	N1	DATA IN	PROP
44	mm1_csel[2]	N_CS1_2	P1	DATA OUT	SB
45	mm1_csel[1]	N_CS1_1	Q1	DATA OUT	SB

Pin #	Signal Name	Abbrev. Name	Pin Loc.	Pad Type	Timing
46	mm1_csel[3]	N_CS1_3	M5	DATA OUT	SB
47	FALSE		M6	CORNER VSS	
48	mm0_csel[1]	N_CS0_1	M7	DATA OUT	SB
49	mm0_csel[0]	N_CS0_0	Q2	DATA OUT	SB
50	TRUE		Q3	CLK VDD	
51	pixel_clock_in	PCLK_IN	Q4	DATA IN	VB
52	x4_clock	X4_CLK	Q5	CLK	
53	FALSE		Q6	CLK VSS	
54	FALSE		Q7	EDGE VSS	
55	TRUE		P3	CORE VDD	
56	TRUE		P4	EDGE VDD	
57	n_reset	N_RESET	P5	DATA IN	VB
58	n_write_en[0]	N_WR0	P6	DATA OUT	STROBE B
59	begin_row_in	BRI	P7	DATA IN	VB
60	end_row_in	ERI	N4	DATA IN	VB
61	begin_frame_in	BFI	N5	DATA IN	VB
62	end_frame_in	EFI	N6	DATA IN	VB
63	begin_row_out	BRO	N7	DATA OUT	SB
64	end_row_out	ERO	M8	DATA OUT	SB
65	begin_frame_out	BFO	M9	DATA OUT	SB
66	end_frame_out	EFO	M10	DATA OUT	SB
67	row_address[0]	RADDR0	M11	DATA OUT	SB
68	row_address[1]	RADDR1	L8	DATA OUT	SB
70	row_address[2]	RADDR2	N8	DATA OUT	SB
71	FALSE		N9	EDGE VSS	
72	TRUE		N10	EDGE VDD	
73	row_address[3]	RADDR3	N11	DATA OUT	SB
74	row_address[4]	RADDR4	N12	DATA OUT	SB
75	row_address[5]	RADDR5	N13	DATA OUT	SB
76	row_address[6]	RADDR6	P8	DATA OUT	SB
77	row_address[7]	RADDR7	P9	DATA OUT	SB
78	row_address[8]	RADDR8	P10	DATA OUT	SB
79	row_address[9]	RADDR9	P11	DATA OUT	SB
80	col_address[0]	CADDR0	P12	DATA OUT	SB
81	col_address[1]	CADDR1	P13	DATA OUT	SB
82	col_address[2]	CADDR2	P14	DATA OUT	SB
83	col_address[3]	CADDR3	Q8	DATA OUT	SB
84	col_address[4]	CADDR4	Q9	DATA OUT	SB
85	FALSE		Q10	EDGE VSS	
86	TRUE		Q11	EDGE VDD	
87	col_address[5]	CADDR5	Q12	DATA OUT	SB
88	TRUE		Q13	CORE VDD	
89	col_address[7]	CADDR7	Q14	DATA OUT	SB
90	col_address[6]	CADDR6	Q15	DATA OUT	SB
91	col_address[8]	CADDR8	P15	DATA OUT	SB
92	col_address[9]	CADDR9	N15	DATA OUT	SB
93	FALSE		M15	EDGE VSS	
94	n_write_en[1]	N_WR1	L15	DATA OUT	STROBE B

Pin #	Signal Name	Abbrev. Name	Pin Loc.	Pad Type	Timing
95	p_data_in[0]	PDIN0	K15	DATA IN	VB
96	p_data_in[1]	PDIN1	J15	DATA IN	VB
97	p_data_in[2]	PDIN2	H15	DATA IN	VB
98	p_data_in[3]	PDIN3	N14	DATA IN	VB
99	p_data_in[4]	PDIN4	M14	DATA IN	VB
100	p_data_in[5]	PDIN5	L14	DATA IN	VB
101	TRUE		K14	EDGE VDD	
102	FALSE		J14	EDGE VSS	
103	p_data_in[6]	PDIN6	H14	DATA IN	VB
104	p_data_in[7]	PDIN7	M13	DATA IN	VB
105	p_data_in[8]	PDIN8	L13	DATA IN	VB
106	p_data_in[9]	PDIN9	K13	DATA IN	VB
107	p_data_in[10]	PDIN10	J13	DATA IN	VB
108	p_data_in[11]	PDIN11	H13	DATA IN	VB
109	p_data_in[12]	PDIN12	L12	DATA IN	VB
110	p_data_in[13]	PDIN13	K12	DATA IN	VB
111	TRUE		J12	EDGE VDD	
112	FALSE		H12	EDGE VSS	
113	p_data_in[14]	PDIN14	H11	DATA IN	VB
114	p_data_in[15]	PDIN15	G12	DATA IN	VB
115	p_data_in[16]	PDIN16	F12	DATA IN	VB
116	filter_id[0]	FID0	E12	DATA IN	PROP
117	filter_id[1]	FID1	D12	DATA IN	PROP
118	filter_id[2]	FID2	G13	DATA IN	PROP
119	ods_ids[0]	DID0	F13	DATA IN	PROP
120	ods_ids[1]	DID1	E13	DATA IN	PROP
121	ods_ids[2]	DID2	D13	DATA IN	PROP
122	ods_ids[3]	DID3	G14	DATA IN	PROP
123	hrd_dev_id[0]	HDID0	F14	DATA IN	PROP
124	hrd_dev_id[1]	HDID1	F14	DATA IN	PROP
125	hrd_dev_id[2]	HDID2	E14	DATA IN	PROP
126	hrd_dev_id[3]	HDID3	D14	DATA IN	PROP
127	TRUE		G14	EDGE VDD	
128	FALSE		B14	EDGE VSS	
129	data[0]	DATA0	G15	DATA IO	VA,SB
130	data[1]	DATA1	F15	DATA IO	VA,SB
131	data[2]	DATA2	E15	DATA IO	VA,SB
132	data[3]	DATA3	D15	DATA IO	VA,SB
133	data[4]	DATA4	C15	DATA IO	VA,SB
134	data[5]	DATA5	B15	DATA IO	VA,SB
135	device_ready	DR	A15	DATA OUT	SB
136	FALSE		D11	CORNER VSS	
137	oe_n_ie	OE_N_IE	D10	DATA IN	PROP
138	data[6]	DATA6	D9	DATA IO	VA,SB
139	data[7]	DATA7	A14	DATA IO	VA,SB
140	data[8]	DATA8	A13	DATA IO	VA,SB
141	data[9]	DATA9	A12	DATA IO	VA,SB
142	FALSE		A11	CORE VSS	

Pin #	Signal Name	Abbrev. Name	Pin Loc.	Pad Type	Timing
143	TRUE		A10	EDGE VDD	
144	FALSE		A9	EDGE VSS	
145	data[10]	DATA10	B13	DATA IO	VA,SB
146	data[11]	DATA11	B12	DATA IO	VA,SB
147	data[12] 1	DATA12	B11	DATA IO	VA,SB
148	data[13]	DATA13	B10	DATA IO	VA,SB
149	data[14]	DATA14	B9	DATA IO	VA,SB
150	data[15]	DATA15	C12	DATA IO	VA,SB
151	state_0[0]	ST0_0	C11	DATA IO	VB,SB
152	state_0[1]	ST0_1	C10	DATA IO	VB,SB
153	state_0[2]	ST0_2	C9	DATA IO	VB,SB
154	state_0[3]	ST0_	D8	DATA IO	VB,SB
155	TRUE		D7	EDGE VDD	
156	FALSE		D6	EDGE VSS	
157	state_0[4]	ST0_4	D5	DATA IO	VB,SB
158	state_0[5]	ST0_5	E8	DATA IO	VB,SB
160	state_0[6]	ST0_6	C8	DATA IO	VB,SB
161	state_0[7]	ST0_7	C7	DATA IO	VB,SB
162	state_0[8]	ST0_	C6	DATA IO	VB,SB
163	state_0[9]	ST0_9	C5	DATA IO	VB,SB
164	state_0[10]	ST0_10	C4	DATA IO	VB,SB
165	state_0[11]	ST0_11	C3	DATA IO	VB,SB
166	state_0[12]	ST0_12	B8	DATA IO	VB,SB
167	state_0[13]	ST0_13	B7	DATA IO	VB,SB
168	state_0[14]	ST0_14	B6	DATA IO	VB,SB
169	state_0[15]	ST0_15	B5	DATA IO	VB,SB
170	address[0]	ADDR0	B4	DATA IN	VA/VB
171	address[1]	ADDR1	B3	DATA IN	VA/VB
172	address[2]	ADDR2	B2	DATA IN	VA/VB
173	TRUE		A8	EDGE VDD	
174	FALSE		A7	EDGE VSS	
175	FALSE		A6	CORE VSS	
176	address[3]	ADDR3	A5	DATA IN	VA/VB
177	address[4]	ADDR4	A4	DATA IN	VA/VB
178	address[5]	ADDR5	A4	DATA IN	VA/VB
179	address[6]	ADDR6	A2	DATA IN	VA/VB
180	address[7]	ADDR7	A1	DATA IN	VA/VB

8.Key Parameters

```
 ) Key Parameters for Chip /tmp_mnt/nfs/u90/gendv20/wallace/tfil
) ================================================================================
)
) TIME = Thu Jul 18 11:48:35 1991
)
) ROUTE_VERSION = 8.00
) HEIGHT = 417.5 MILS
)     ( = 10604.5 u )
) WIDTH = 420.9 MILS
)     ( = 10690.8 u )
) ROUTED = 1 (0=NO,1=YES)
) TOTAL_WIRE_LENGTH = 844063 MILS
)     ( = 21439200. u )
) CORE_AREA = 138680.0 SQUARE_MILS
)     ( = 89470790.4 u2 )
) PADRING_AREA = 37072.8 SQUARE_MILS
)     ( = 23917888. u2 )
) PAD_AREA = 34117.3 SQUARE_MILS
)     ( = 22011118. u2 )
) ROUTE_AREA = 102015.5 SQUARE_MILS
)     ( = 65816321.1 u2 )
) PERCENT_ROUTING_OF_CORE = 73 %
) PERCENT_ROUTING_OF_CHIP = 58 %
) PERCENT_CORE_OF_CHIP = 78 %
) PERCENT_PADRING_OF_CHIP = 21 %
) PERCENT_PAD_OF_PADRING = 92 %
)
) NETLIST_VERSION = 2.0
) NETLIST_EXISTS = 1 (0=NO,1=YES)
)
) PHASE_A_TIME = 20.7 NANOSECONDS
) PHASE_B_TIME = 20.5 NANOSECONDS
) SYMMETRIC_TIME = 152.1 NANOSECONDS
) NUMBER_OF_TRANSISTORS = 81253
) POWER_DISSIPATION = 926.49 MILLIWATTS_@5V_10MHZ
)
)
) ROUTE_ESTIMATE_LVL = 0
) FLAT_ROUTE = 0 (0=NO,1=YES)
) TECHNOLOGY_NAME = CMOS-2
) PACKAGE_SPECIFIED = 1 (0=NO,1=YES)
) PACKAGE_NAME = CPGA180f
) FABLINE_NAME = HP2_CN10B
) COMPILER_TYPE = GCX
)
) FLOORPLAN_VERSION = 8.1
) BOND_PAD_CNT = 177
) HEIGHT_ESTIMATE = 299.04 MILS
)     ( = 7595.616 u )
) WIDTH_ESTIMATE = 415.27 MILS
)     ( = 10547.85 u )
) FUSED = 1 (0=NO,1=YES)
) FUSION_REQUIRED = 1 (0=NO,1=YES)
) PINOUT = 1 (0=NO,1=YES)
) PINOUT_REQUIRED = 1 (0=NO,1=YES)
) PLACED = 1 (0=NO,1=YES)
) PLACEMENT_REQUIRED = 1 (0=NO,1=YES)
)
)
```

```
) DOWN_BONDS_ALLOWED = 1 (0=NO,1=YES)
) PKG_PIN_COUNT = 180
) PKG_WELL_HEIGHT = 472.00 MILS
)    ( = 11988.80 u )
) PKG_WELL_WIDTH = 472.00 MILS
)    ( = 11988.80 u )
) AREA = 175725.8 SQUARE_MILS
)    ( = 113371257. u2 )
) OBJECT_TYPE = Chip
) AREA_PER_TRANSISTOR = 2.162699 SQUARE_MILS
)    ( = 1395.28690 u2 )
) PHYSICAL_IMPLEMENTATIONS_EXIST = 0 (0=NO,1=YES)
) CHECKPOINTS_EXIST = 0 (0=NO,1=YES)
) CAN_SET_FABLINE = 1 (0=NO,1=YES)
)
) Key Parameter Listing Complete
```

9.PADRING.033

OUTPUT RINGS REPORT Version 1

Noise contribution:(ma/nh) Speed0: 2.50 Speed1: 5.00 Speed2: 8.33 Speed3: 16.66
Limits: Maximum noise level: 100. Unacceptable level: 150

Combined power pads do not supply clean power to the core.
Their use is discouraged

Ring under analysis: VDD

	PAD NAME	EDGE	SPEED	DRIVE TYPE	PAD SUPPLY	COMMENT
WARNING:	mm0_cs[1]	NORTH	1	CMOS	0	EXCESSIVE NOISE LEVEL
	mm0_cs[0]	NORTH	1	CMOS	1	OK
	mm1_cs[3]	NORTH	1	CMOS	1	OK
	mm1_cs[1]	EAST	1	CMOS	1	OK
	mm1_cs[2]	EAST	1	CMOS	1	OK
	mm1_cs[0]	EAST	1	CMOS	1	OK
	state_1[15]	EAST	2	CMOS	1	OK
	state_1[14]	EAST	2	CMOS	1	OK
	state_1[13]	EAST	2	CMOS	1	OK
	edge_vdd_pad[2]	EAST		POWER		
	state_1[12]	EAST	2	CMOS	1	OK
	state_1[11]	EAST	2	CMOS	1	OK
	state_1[10]	EAST	2	CMOS	1	OK
	state_1[9]	EAST	2	CMOS	1	OK
	state_1[8]	EAST	2	CMOS	1	OK
	state_1[6]	EAST	2	CMOS	1	OK
	state_1[7]	EAST	2	CMOS	1	OK
	state_1[4]	EAST	2	CMOS	1	OK
	state_1[5]	EAST	2	CMOS	1	OK
	state_1[2]	EAST	2	CMOS	1	OK
	state_1[3]	EAST	2	CMOS	1	OK
	state_1[0]	EAST	2	CMOS	1	OK
	state_1[1]	EAST	2	CMOS	1	OK
	edge_vdd_pad[1]	EAST		POWER		

p_data_out[16]	EAST	1	CMOS	1	OK
p_data_out[15]	EAST	1	CMOS	1	OK
p_data_out[14]	EAST	1	CMOS	2	OK
p_data_out[13]	EAST	1	CMOS	2	OK
p_data_out[12]	EAST	1	CMOS	2	OK
p_data_out[11]	EAST	1	CMOS	2	OK
p_data_out[10]	EAST	1	CMOS	2	OK
p_data_out[9]	EAST	1	CMOS	2	OK
p_data_out[8]	EAST	1	CMOS	1	OK
p_data_out[7]	EAST	1	CMOS	2	OK
p_data_out[6]	EAST	1	CMOS	2	OK
edge_vdd_pad[0]	EAST		POWER		
p_data_out[5]	EAST	1	CMOS	2	OK
p_data_out[4]	EAST	1	CMOS	2	OK
p_data_out[3]	EAST	1	CMOS	2	OK
p_data_out[2]	EAST	1	CMOS	2	OK
p_data_out[1]	EAST	1	CMOS	2	OK
p_data_out[0]	EAST	1	CMOS	2	OK
edge_vdd_pad[11]	SOUTH		POWER		
state_0[15]	SOUTH	2	CMOS	2	OK
state_0[14]	SOUTH	2	CMOS	2	OK
state_0[13]	SOUTH	2	CMOS	2	OK
state_0[12]	SOUTH	2	CMOS	1	OK
state_0[11]	SOUTH	2	CMOS	1	OK
state_0[10]	SOUTH	2	CMOS	1	OK
state_0[9]	SOUTH	2	CMOS	2	OK
state_0[8]	SOUTH	2	CMOS	1	OK
state_0[7]	SOUTH	2	CMOS	1	OK
state_0[6]	SOUTH	2	CMOS	1	OK
state_0[5]	SOUTH	2	CMOS	1	OK
state_0[4]	SOUTH	2	CMOS	1	OK
edge_vdd_pad[10]	SOUTH		POWER		
state_0[3]	SOUTH	2	CMOS	1	OK
state_0[2]	SOUTH	2	CMOS	2	OK
state_0[1]	SOUTH	2	CMOS	2	OK
state_0[0]	SOUTH	2	CMOS	2	OK
data[15]	SOUTH	1	CMOS	2	OK
data[13]	SOUTH	1	CMOS	2	OK
data[14]	SOUTH	1	CMOS	2	OK
data[11]	SOUTH	1	CMOS	1	OK
data[12]	SOUTH	1	CMOS	1	OK
data[10]	SOUTH	1	CMOS	1	OK
edge_vdd_pad[9]	SOUTH		POWER		
data[8]	SOUTH	1	CMOS	1	OK
data[9]	SOUTH	1	CMOS	4	OK
data[6]	SOUTH	1	CMOS	4	OK
data[7]	SOUTH	1	CMOS	4	OK
dr	WEST	1	CMOS	4	OK
data[5]	WEST	1	CMOS	4	OK
data[4]	WEST	1	CMOS	4	OK
data[3]	WEST	1	CMOS	5	OK
data[2]	WEST	1	CMOS	5	OK
data[1]	WEST	1	CMOS	4	OK
data[0]	WEST	1	CMOS	4	OK
edge_vdd_pad[8]	WEST		POWER		
edge_vdd_pad[7]	WEST		POWER		
edge_vdd_pad[6]	WEST		POWER		
n_wr_en[1]	WEST	1	CMOS	4	OK
col_address[9]	NORTH	1	CMOS	4	OK
col_address[8]	NORTH	1	CMOS	4	OK

```
col_address[6]  NORTH   1  CMOS      4   OK
col_address[7]  NORTH   1  CMOS      4   OK
col_address[5]  NORTH   1  CMOS      4   OK
edge_vdd_pad[5] NORTH      POWER
col_address[4]  NORTH   1  CMOS      6   OK
col_address[3]  NORTH   1  CMOS      6   OK
col_address[2]  NORTH   1  CMOS      6   OK
col_address[1]  NORTH   1  CMOS      6   OK
col_address[0]  NORTH   1  CMOS      3   OK
row_address[9]  NORTH   1  CMOS      3   OK
row_address[8]  NORTH   1  CMOS      3   OK
row_address[7]  NORTH   1  CMOS      3   OK
row_address[6]  NORTH   1  CMOS      3   OK
row_address[5]  NORTH   1  CMOS      3   OK
row_address[4]  NORTH   1  CMOS      2   OK
row_address[3]  NORTH   1  CMOS      2   OK
edge_vdd_pad[4] NORTH      POWER
row_address[2]  NORTH   1  CMOS      2   OK
row_address[1]  NORTH   1  CMOS      2   OK
row_address[0]  NORTH   1  CMOS      2   OK
end_frame_out   NORTH   1  CMOS      2   OK
begin_frame_out NORTH   1  CMOS      2   OK
end_row_out     NORTH   1  CMOS      2   OK
begin_row_out   NORTH   1  CMOS      2   OK
n_wr_en[0]      NORTH   1  CMOS      2   OK
edge_vdd_pad[3] NORTH      POWER

This ring has 6 more VDD pads than it needs
 Ring under analysis: VSS

          PAD NAME        EDGE  SPEED DRIVE PAD     COMMENT
                                      TYPE  SUPPLY
-------------------------------------------------------------------------------

          mm0_cs[1]       NORTH   1  CMOS      1   OK
          mm0_cs[0]       NORTH   1  CMOS      2   OK
          mm1_cs[3]       NORTH   1  CMOS      2   OK
          corner_vss_pad[1NORTH      POWER

          mm1_cs[1]       EAST    1  CMOS      2   OK
          mm1_cs[2]       EAST    1  CMOS      2   OK
          mm1_cs[0]       EAST    1  CMOS      2   OK
          state_1[15]     EAST    2  CMOS      2   OK
          state_1[14]     EAST    2  CMOS      2   OK
          state_1[13]     EAST    2  CMOS      2   OK
          edge_vss_pad[2] EAST       POWER
          state_1[12]     EAST    2  CMOS      2   OK
          state_1[11]     EAST    2  CMOS      2   OK
          state_1[10]     EAST    2  CMOS      2   OK
          state_1[9]      EAST    2  CMOS      2   OK
          state_1[8]      EAST    2  CMOS      2   OK
          state_1[6]      EAST    2  CMOS      1   OK
          state_1[7]      EAST    2  CMOS      1   OK
          state_1[4]      EAST    2  CMOS      1   OK
          state_1[5]      EAST    2  CMOS      1   OK
          state_1[2]      EAST    2  CMOS      1   OK
          state_1[3]      EAST    2  CMOS      1   OK
          state_1[0]      EAST    2  CMOS      1   OK
          state_1[1]      EAST    2  CMOS      1   OK
          edge_vss_pad[1] EAST       POWER
          p_data_out[16]  EAST    1  CMOS      1   OK
          p_data_out[15]  EAST    1  CMOS      1   OK
```

```
p_data_out[14]  EAST    1  CMOS      2   OK
p_data_out[13]  EAST    1  CMOS      2   OK
p_data_out[12]  EAST    1  CMOS      2   OK
p_data_out[11]  EAST    1  CMOS      2   OK
p_data_out[10]  EAST    1  CMOS      2   OK
p_data_out[9]   EAST    1  CMOS      2   OK
p_data_out[8]   EAST    1  CMOS      1   OK
p_data_out[7]   EAST    1  CMOS      3   OK
p_data_out[6]   EAST    1  CMOS      3   OK
edge_vss_pad[0] EAST       POWER
p_data_out[5]   EAST    1  CMOS      3   OK
p_data_out[4]   EAST    1  CMOS      3   OK
p_data_out[3]   EAST    1  CMOS      3   OK
p_data_out[2]   EAST    1  CMOS      3   OK
p_data_out[1]   EAST    1  CMOS      3   OK
p_data_out[0]   EAST    1  CMOS      3   OK
corner_vss_pad[0EAST       POWER

edge_vss_pad[11]SOUTH      POWER
state_0[15]     SOUTH   2  CMOS      3   OK
state_0[14]     SOUTH   2  CMOS      3   OK
state_0[13]     SOUTH   2  CMOS      3   OK
state_0[12]     SOUTH   2  CMOS      2   OK
state_0[11]     SOUTH   2  CMOS      2   OK
state_0[10]     SOUTH   2  CMOS      2   OK
state_0[9]      SOUTH   2  CMOS      3   OK
state_0[8]      SOUTH   2  CMOS      1   OK
state_0[7]      SOUTH   2  CMOS      1   OK
state_0[6]      SOUTH   2  CMOS      1   OK
state_0[5]      SOUTH   2  CMOS      1   OK
state_0[4]      SOUTH   2  CMOS      1   OK
edge_vss_pad[10]SOUTH      POWER
state_0[3]      SOUTH   2  CMOS      2   OK
state_0[2]      SOUTH   2  CMOS      2   OK
state_0[1]      SOUTH   2  CMOS      2   OK
state_0[0]      SOUTH   2  CMOS      2   OK
data[15]        SOUTH   1  CMOS      3   OK
data[13]        SOUTH   1  CMOS      3   OK
data[14]        SOUTH   1  CMOS      3   OK
data[11]        SOUTH   1  CMOS      2   OK
data[12]        SOUTH   1  CMOS      2   OK
edge_vss_pad[9] SOUTH      POWER
data[10]        SOUTH   1  CMOS      2   OK
data[8]         SOUTH   1  CMOS      2   OK
data[9]         SOUTH   1  CMOS      5   OK
data[6]         SOUTH   1  CMOS      6   OK
data[7]         SOUTH   1  CMOS      6   OK
corner_vss_pad[2SOUTH      POWER

dr              WEST    1  CMOS      6   OK
data[5]         WEST    1  CMOS      6   OK
data[4]         WEST    1  CMOS      6   OK
data[3]         WEST    1  CMOS      6   OK
data[2]         WEST    1  CMOS      6   OK
data[1]         WEST    1  CMOS      6   OK
data[0]         WEST    1  CMOS      6   OK
edge_vss_pad[8] WEST       POWER
edge_vss_pad[7] WEST       POWER
edge_vss_pad[6] WEST       POWER
n_wr_en[1]      WEST    1  CMOS      6   OK
edge_vss_pad[12]WEST       POWER
```

```
col_address[9]  NORTH   1  CMOS      6   OK
col_address[8]  NORTH   1  CMOS      6   OK
col_address[6]  NORTH   1  CMOS      5   OK
col_address[7]  NORTH   1  CMOS      5   OK
col_address[5]  NORTH   1  CMOS      5   OK
edge_vss_pad[5] NORTH      POWER
col_address[4]  NORTH   1  CMOS      7   OK
col_address[3]  NORTH   1  CMOS      7   OK
col_address[2]  NORTH   1  CMOS      7   OK
col_address[1]  NORTH   1  CMOS      7   OK
col_address[0]  NORTH   1  CMOS      4   OK
row_address[9]  NORTH   1  CMOS      3   OK
row_address[8]  NORTH   1  CMOS      3   OK
row_address[7]  NORTH   1  CMOS      3   OK
row_address[6]  NORTH   1  CMOS      3   OK
row_address[5]  NORTH   1  CMOS      3   OK
row_address[4]  NORTH   1  CMOS      2   OK
row_address[3]  NORTH   1  CMOS      2   OK
edge_vss_pad[4] NORTH      POWER
row_address[2]  NORTH   1  CMOS      2   OK
row_address[1]  NORTH   1  CMOS      2   OK
row_address[0]  NORTH   1  CMOS      2   OK
end_frame_out   NORTH   1  CMOS      2   OK
begin_frame_out NORTH   1  CMOS      2   OK
end_row_out     NORTH   1  CMOS      2   OK
begin_row_out   NORTH   1  CMOS      2   OK
n_wr_en[0]      NORTH   1  CMOS      2   OK
edge_vss_pad[3] NORTH      POWER
```

```
This ring has 10 more VSS pads than it needs
```

10.Power Dissipation

```
) Total power consumption (5.5V, 0 DegC 50pf/out_pad):
)       DC:         0.00mW [0.00(core)+0.00(ring)]
)       AC@10MHz:   921.10mW [467.71(core)+453.39(ring)]
```

11.Simulation Setup Files

Genesil default setting is used.

12.Timing Setup Files

12.1. hot_cond.040

```
LABEL 4.5 volts, 104 degree
TEMP_VOLT 104 4.50
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK
```

12.2. set_room.040

```
LABEL 5.0 volts, 59 degree
TEMP_VOLT 59 5.00
```

```
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK x4_clock
```

13.Timing Reports

13.1. TYPICAL, 102 deg C, 4.5 V

```
*******************************************************************************
        GENESIL Version v8.1DV_Jul_2_Quark -- Wed Jul 17 10:30:42 1991
Chip: /tmp_mnt/nfs/u90/gendv20/wallace/tfil                    Timing Analyzer
*******************************************************************************
CLOCK REPORT MODE
-------------------------------------------------------------------------------
Fabline: HP2_CN10B                    Corner: TYPICAL
  Junction Temperature:102 deg C      Voltage:4.50v
  External Clock: x4_clock
 Included setup files:
  #0  hot_cond              (4.5 volts, 102 degree)
-------------------------------------------------------------------------------
                          CLOCK TIMES (minimum)
Phase 1 High:    14.1   ns          Phase 2 High:    14.3   ns
           ----------                          ----------
Cycle (from Ph1):    88.2   ns     Cycle (from Ph2):    99.0   ns
                  ----------                          ----------
Minimum Cycle Time:    99.0   ns   Symmetric Cycle Time:     99.0   ns
                    ----------                          ----------
-------------------------------------------------------------------------------
                          CLOCK WORST CASE PATHS
Minimum Phase 1 high time is    14.1   ns set by:
                          ----------
  ** Clock delay: 1.5ns (15.6-14.1)
   Node                          Cumulative Delay      Transition
   stage0/tfil_7/507                  15.6                fall
   stage0/tfil_7/sa0_load             14.8                rise
   stage0/load_sigs/PORT2_EXT1[0]     14.8                rise
   <age0/load_sigs/PORT2_EXT1[0]'     13.6                rise
   stage0/load_sigs/29                13.3                fall
   stage0/load_sigs/BUS_A[0]          13.1                rise
   tfil_5/sb0_load                    13.1                rise
   tfil_5/sb0_load'                   12.3                rise
   tfil_5/39                          12.0                fall
   tfil_5/29                          11.2                rise
   tfil_5/26                           9.5                fall
   tfil_5/tf_sel                       9.1                rise
   tfil_4/tf_sel                       9.1                rise
   tfil_4/tf_sel'                      8.0                rise
   tfil_4/193                          7.8                fall
   tfil_4/218                          5.1                rise
   tfil_4/214                          3.4                fall
   tfil_4/addr[5]                      2.8                rise
   pre_tfil_4/addr2[5]                 2.8                rise
   pre_tfil_4/addr2[5]'                2.7                rise
   pre_tfil_4/34                       2.5                fall
   pre_tfil_4/pre_addr[5]              2.1                rise
   address[5]/addr                     2.1                rise
   address[5]/addr'                    1.1                rise
   address[5]/1                        1.0                fall
   address[5]                          0.0                rise
```

```
Minimum Phase 2 high time is    14.3   ns set by:
                          ----------
  ** Clock delay: 1.9ns (16.2-14.3)
   Node                              Cumulative Delay      Transition
   tfil_4/1786                            16.2               rise
   tfil_4/308                             14.6               fall
   tfil_4/276                             13.9               rise
   tfil_4/190                             12.8               fall
   tfil_4/221                             12.0               rise
   tfil_4/addr[2]                          3.1               fall
   pre_tfil_4/addr2[2]                     3.1               fall
   pre_tfil_4/addr2[2]'                    2.2               fall
   pre_tfil_4/31                           2.0               rise
   pre_tfil_4/pre_addr[2]                  1.2               fall
   address[2]/addr                         1.2               fall
   address[2]/addr'                        0.9               fall
   address[2]/1                            0.7               rise
   address[2]                              0.0               fall

Minimum cycle time (from Ph1) is   88.2    ns set by:
                          ----------
  ** Clock delay: 5.9ns (94.1-88.2)
   Node                              Cumulative Delay      Transition
   stage0/tfil_9/twos/1177                94.1               fall
   stage0/tfil_9/twos/1176                93.8               rise
   *stage0/tfil_9/twos/1178               92.9               rise
   <e0/tfil_9/twos/INTER0_ST2[33]         92.8               fall
   stage0/tfil_9/twos/1172                92.2               rise
   stage0/tfil_9/twos/1171                91.5               fall
   <e0/tfil_9/twos/INTER4_ST2[33]         91.3               fall
   stage0/tfil_9/twos/1196                91.0               rise
   <0/tfil_9/twos/ADDSUB2_OUT[33]         90.3               fall
   stage0/tfil_9/twos/1186                89.9               rise
   stage0/tfil_9/twos/1190                89.0               rise
   stage0/tfil_9/twos/1194                88.5               fall
   stage0/tfil_9/twos/1159                87.8               rise
   stage0/tfil_9/twos/1124                87.1               fall
   stage0/tfil_9/twos/1089                86.5               rise
   stage0/tfil_9/twos/1043                85.7               fall
   stage0/tfil_9/twos/1041                85.0               rise
   <e0/tfil_9/twos/INTER0_IV1[29]         83.8               fall
   stage0/tfil_9/twos/1033                83.3               rise
   stage0/tfil_9/twos/1034                82.5               rise
   stage0/tfil_9/twos/p[29]               82.3               fall
   stage0/tfil_9/p/p[29]                  82.3               fall
   stage0/tfil_9/p/p[29]'                 82.1               fall
   stage0/tfil_9/p/238                    81.8               rise
   <age0/tfil_9/p/ADDSUB1_OUT[14]         81.1               fall
   stage0/tfil_9/p/228                    80.7               rise
   stage0/tfil_9/p/227                    79.6               rise
   stage0/tfil_9/p/237                    79.1               fall
   stage0/tfil_9/p/221                    78.5               rise
   stage0/tfil_9/p/205                    77.8               fall
   stage0/tfil_9/p/189                    77.2               rise
   stage0/tfil_9/p/173                    76.5               fall
   stage0/tfil_9/p/157                    75.8               rise
   stage0/tfil_9/p/141                    75.1               fall
   stage0/tfil_9/p/125                    74.5               rise
   stage0/tfil_9/p/109                    73.8               fall
   stage0/tfil_9/p/93                     73.1               rise
   stage0/tfil_9/p/77                     72.4               fall
   stage0/tfil_9/p/61                     71.8               rise
```

```
   stage0/tfil_9/p/45                  71.1              fall
   stage0/tfil_9/p/29                  70.4              rise
   stage0/tfil_9/p/2                   69.6              fall
   stage0/tfil_9/p/1                   68.9              rise
   stage0/tfil_9/p/BUS_A[0]            67.8              fall
   <age0/tfil_9/product/MS_SUM[0]      67.8              fall
   <ge0/tfil_9/product/MS_SUM[0]'      67.3              fall
   stage0/tfil_9/product/161           67.0              rise
   stage0/tfil_9/product/424           63.6              fall
   stage0/tfil_9/product/393           63.1              rise
   stage0/tfil_9/product/665           60.4              fall
   stage0/tfil_9/product/655           59.9              rise
   stage0/tfil_9/product/924           57.4              fall
   stage0/tfil_9/product/914           57.0              rise
   stage0/tfil_9/product/1184          54.5              fall
   stage0/tfil_9/product/1174          54.0              rise
   stage0/tfil_9/product/1444          51.5              fall
   stage0/tfil_9/product/1434          51.0              rise
   stage0/tfil_9/product/1704          48.5              fall
   stage0/tfil_9/product/1694          48.0              rise
   stage0/tfil_9/product/1964          45.5              fall
   stage0/tfil_9/product/1954          45.0              rise
   stage0/tfil_9/product/2224          42.6              fall
   stage0/tfil_9/product/2214          42.1              rise
   stage0/tfil_9/product/2484          39.6              fall
   stage0/tfil_9/product/2474          39.1              rise
   stage0/tfil_9/product/2744          36.6              fall
   stage0/tfil_9/product/2734          36.1              rise
   stage0/tfil_9/product/3004          33.6              fall
   stage0/tfil_9/product/2994          33.1              rise
   stage0/tfil_9/product/3264          30.6              fall
   stage0/tfil_9/product/3254          30.2              rise
   stage0/tfil_9/product/3420          27.7              fall
   stage0/tfil_9/product/3417          27.2              rise
   stage0/tfil_9/product/3530          26.4              fall
   stage0/tfil_9/product/3525          26.0              rise
   <e0/tfil_9/product/mi0_data[3]      25.4              fall
   stage0/tfil_15/mux_in_0[3]          25.4              fall
   stage0/tfil_15/mux_in_0[3]'         24.6              fall
   stage0/tfil_15/137                  24.3              rise
   stage0/tfil_15/135                  22.9              fall
   stage0/tfil_15/134                  22.6              rise
   stage0/tfil_15/111                  21.5              fall
   stage0/tfil_15/83                   20.6              rise
   stage0/tfil_15/count[0]             11.5              fall
   tfil_1/count[0]                     11.5              fall
   tfil_1/count[0]'                    11.0              fall
   tfil_1/85                           10.8              rise
   tfil_1/86                            9.7              fall
   tfil_1/90                            8.8              rise
   tfil_1/92                            7.4              fall
   tfil_1/635                           7.0              rise
   tfil_1/634                           5.8              fall
   tfil_1/94                            5.5              rise
   tfil_1/192                           5.0              fall
   tfil_1/PHASE_A                       4.4              rise
   x4_clock_pad/PHASE_A                 4.4              rise
   x4_clock                             0.0              rise

Minimum cycle time (from Ph2) is   99.0    ns set by:
                                  ----------

  ** Clock delay: 3.9ns (102.9-99.0)
```

Node	Cumulative Delay	Transition
stage1/tfil_9/twos/1178	102.9	rise
<e1/tfil_9/twos/INTER0_ST2[33]	102.7	fall
stage1/tfil_9/twos/1172	102.1	rise
stage1/tfil_9/twos/1171	101.5	fall
<e1/tfil_9/twos/INTER4_ST2[33]	101.3	fall
stage1/tfil_9/twos/1196	101.0	rise
<1/tfil_9/twos/ADDSUB2_OUT[33]	100.3	fall
stage1/tfil_9/twos/1186	99.8	rise
stage1/tfil_9/twos/1190	98.9	rise
stage1/tfil_9/twos/1194	98.5	fall
stage1/tfil_9/twos/1159	97.8	rise
stage1/tfil_9/twos/1124	97.1	fall
stage1/tfil_9/twos/1089	96.5	rise
stage1/tfil_9/twos/1043	95.7	fall
stage1/tfil_9/twos/1041	94.9	rise
<e1/tfil_9/twos/INTER0_IV1[29]	93.7	fall
stage1/tfil_9/twos/1033	93.3	rise
stage1/tfil_9/twos/1034	92.5	rise
stage1/tfil_9/twos/p[29]	92.2	fall
stage1/tfil_9/p/p[29]	92.2	fall
stage1/tfil_9/p/p[29]'	92.0	fall
stage1/tfil_9/p/238	91.8	rise
<age1/tfil_9/p/ADDSUB1_OUT[14]	91.1	fall
stage1/tfil_9/p/228	90.7	rise
stage1/tfil_9/p/227	89.6	rise
stage1/tfil_9/p/237	89.1	fall
stage1/tfil_9/p/221	88.5	rise
stage1/tfil_9/p/205	87.8	fall
stage1/tfil_9/p/189	87.1	rise
stage1/tfil_9/p/173	86.4	fall
stage1/tfil_9/p/157	85.8	rise
stage1/tfil_9/p/141	85.1	fall
stage1/tfil_9/p/125	84.4	rise
stage1/tfil_9/p/109	83.7	fall
stage1/tfil_9/p/93	83.1	rise
stage1/tfil_9/p/77	82.4	fall
stage1/tfil_9/p/61	81.7	rise
stage1/tfil_9/p/45	81.0	fall
stage1/tfil_9/p/29	80.4	rise
stage1/tfil_9/p/2	79.6	fall
stage1/tfil_9/p/1	78.9	rise
stage1/tfil_9/p/BUS_A[0]	77.7	fall
<age1/tfil_9/product/MS_SUM[0]	77.7	fall
<ge1/tfil_9/product/MS_SUM[0]'	77.2	fall
stage1/tfil_9/product/161	76.9	rise
stage1/tfil_9/product/424	73.6	fall
stage1/tfil_9/product/393	73.1	rise
stage1/tfil_9/product/665	70.4	fall
stage1/tfil_9/product/655	69.9	rise
stage1/tfil_9/product/924	67.4	fall
stage1/tfil_9/product/914	66.9	rise
stage1/tfil_9/product/1184	64.4	fall
stage1/tfil_9/product/1174	64.0	rise
stage1/tfil_9/product/1444	61.5	fall
stage1/tfil_9/product/1434	61.0	rise
stage1/tfil_9/product/1704	58.5	fall
stage1/tfil_9/product/1694	58.0	rise
stage1/tfil_9/product/1964	55.5	fall
stage1/tfil_9/product/1954	55.0	rise
stage1/tfil_9/product/2224	52.5	fall
stage1/tfil_9/product/2214	52.0	rise

```
   stage1/tfil_9/product/2484          49.6              fall
   stage1/tfil_9/product/2474          49.1              rise
   stage1/tfil_9/product/2744          46.6              fall
   stage1/tfil_9/product/2734          46.1              rise
   stage1/tfil_9/product/3004          43.6              fall
   stage1/tfil_9/product/2994          43.1              rise
   stage1/tfil_9/product/3264          40.6              fall
   stage1/tfil_9/product/3254          40.1              rise
   stage1/tfil_9/product/3420          37.6              fall
   stage1/tfil_9/product/3417          37.2              rise
   stage1/tfil_9/product/3530          36.4              fall
   stage1/tfil_9/product/3525          36.0              rise
   <e1/tfil_9/product/mi0_data[3]      35.4              fall
   stage1/tfil_15/mux_in_0[3]          35.4              fall
   stage1/tfil_15/mux_in_0[3]'         34.6              fall
   stage1/tfil_15/102                  34.3              rise
   stage1/tfil_15/80                   33.3              fall
   stage1/tfil_15/130                  30.9              rise
   stage1/tfil_15/150                  30.6              fall
   stage1/tfil_15/81                   30.2              rise
   stage1/tfil_15/88                   25.8              fall
   stage1/tfil_15/137                  22.8              rise
   stage1/tfil_15/output_sel           22.4              fall
   tfil_4/output_sel1                  22.4              fall
   tfil_4/output_sel1'                 21.3              fall
   tfil_4/472                          21.1              rise
   tfil_4/198                          19.1              fall
   tfil_4/1852                         18.6              rise
   *tfil_4/194                         17.0              fall
   tfil_4/195                          16.7              rise
   tfil_4/197                          16.0              fall
   tfil_4/1834                         15.7              rise
   tfil_4/199                          14.1              fall
   tfil_4/205                          13.7              rise
   tfil_4/190                          12.8              fall
   tfil_4/221                          12.0              rise
   tfil_4/addr[2]                       3.1              fall
   pre_tfil_4/addr2[2]                  3.1              fall
   pre_tfil_4/addr2[2]'                 2.2              fall
   pre_tfil_4/31                        2.0              rise
   pre_tfil_4/pre_addr[2]               1.2              fall
   address[2]/addr                      1.2              fall
   address[2]/addr'                     0.9              fall
   address[2]/1                         0.7              rise
   address[2]                           0.0              fall

--------------------------------------------------------------------------------
```

```
********************************************************************************
        GENESIL Version v8.1DV_Jul_2_Quark -- Wed Jul 17 10:30:43 1991
Chip: /tmp_mnt/nfs/u90/gendv20/wallace/tfil                    Timing Analyzer
********************************************************************************
OUTPUT DELAY MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                    Corner: TYPICAL
  Junction Temperature:102 deg C      Voltage:4.50v
  External Clock: x4_clock
 Included setup files:
  #0  hot_cond              (4.5 volts, 102 degree)
--------------------------------------------------------------------------------
                              OUTPUT DELAYS (ns)
Output                    Ph1(r) Delay      Ph2(r) Delay      Loading(pf)
                          Min      Max      Min      Max
begin_frame_out           12.7     15.4     ---      ---      50.00   PATH
begin_row_out             12.7     15.4     ---      ---      50.00   PATH
col_address[0]            11.7     18.8     ---      ---      50.00   PATH
col_address[1]            11.7     18.9     ---      ---      50.00   PATH
col_address[2]            11.8     18.9     ---      ---      50.00   PATH
col_address[3]            11.8     18.9     ---      ---      50.00   PATH
col_address[4]            11.8     18.9     ---      ---      50.00   PATH
col_address[5]            11.8     18.9     ---      ---      50.00   PATH
col_address[6]            12.3     19.3     ---      ---      50.00   PATH
col_address[7]            12.2     19.3     ---      ---      50.00   PATH
col_address[8]            12.2     19.2     ---      ---      50.00   PATH
col_address[9]            12.2     18.5     ---      ---      50.00   PATH
data[0]                   14.3     29.1     14.3     29.1     50.00   PATH
data[10]                  12.9     26.0     12.9     26.0     50.00   PATH
data[11]                  14.1     30.7     14.1     30.7     50.00   PATH
data[12]                  14.0     30.9     14.0     30.9     50.00   PATH
data[13]                  12.9     27.1     12.9     27.1     50.00   PATH
data[14]                  13.0     26.4     13.0     26.4     50.00   PATH
data[15]                  11.2     25.3     11.2     25.3     50.00   PATH
data[1]                   14.5     34.4     14.5     34.4     50.00   PATH
data[2]                   14.5     32.1     14.5     32.1     50.00   PATH
data[3]                   14.5     31.9     14.5     31.9     50.00   PATH
data[4]                   12.7     31.3     12.7     31.3     50.00   PATH
data[5]                   14.4     28.5     14.4     28.5     50.00   PATH
data[6]                   12.2     26.2     12.2     26.2     50.00   PATH
data[7]                   12.7     29.9     12.7     29.9     50.00   PATH
data[8]                   13.8     30.0     13.8     30.0     50.00   PATH
data[9]                   12.8     27.0     12.8     27.0     50.00   PATH
device_ready              13.5     16.4     13.5     16.4     50.00   PATH
end_frame_out             12.7     15.3     ---      ---      50.00   PATH
end_row_out               12.9     15.5     ---      ---      50.00   PATH
mm0_csel[0]               15.6     23.2     ---      ---      50.00   PATH
mm0_csel[1]               15.9     25.1     ---      ---      50.00   PATH
mm1_csel[0]               11.9     25.1     11.9     15.0     50.00   PATH
mm1_csel[1]               13.2     25.1     13.2     13.9     50.00   PATH
mm1_csel[2]               11.8     25.6     11.8     14.9     50.00   PATH
mm1_csel[3]               13.2     25.6     13.2     13.8     50.00   PATH
n_write_en[0]             10.5     10.5     14.0     14.0     50.00   PATH
n_write_en[1]             10.7     10.7     14.4     14.4     50.00   PATH
p_data_out[0]             13.5     16.1     ---      ---      50.00   PATH
p_data_out[10]            13.3     16.0     ---      ---      50.00   PATH
p_data_out[11]            13.3     16.0     ---      ---      50.00   PATH
p_data_out[12]            13.3     16.0     ---      ---      50.00   PATH
p_data_out[13]            13.3     16.0     ---      ---      50.00   PATH
p_data_out[14]            13.3     15.9     ---      ---      50.00   PATH
p_data_out[15]            13.3     16.0     ---      ---      50.00   PATH
p_data_out[16]            12.7     15.4     ---      ---      50.00   PATH
```

p_data_out[1]	13.5	16.1	---	---	50.00	PATH
p_data_out[2]	13.5	16.0	---	---	50.00	PATH
p_data_out[3]	13.5	16.1	---	---	50.00	PATH
p_data_out[4]	13.4	16.0	---	---	50.00	PATH
p_data_out[5]	13.4	16.0	---	---	50.00	PATH
p_data_out[6]	13.4	16.0	---	---	50.00	PATH
p_data_out[7]	13.4	16.0	---	---	50.00	PATH
p_data_out[8]	13.4	16.1	---	---	50.00	PATH
p_data_out[9]	13.3	16.0	---	---	50.00	PATH
row_address[0]	11.6	18.8	---	---	50.00	PATH
row_address[1]	11.6	18.8	---	---	50.00	PATH
row_address[2]	11.6	18.7	---	---	50.00	PATH
row_address[3]	11.6	18.8	---	---	50.00	PATH
row_address[4]	11.7	18.7	---	---	50.00	PATH
row_address[5]	11.7	18.8	---	---	50.00	PATH
row_address[6]	11.8	19.3	---	---	50.00	PATH
row_address[7]	11.8	18.8	---	---	50.00	PATH
row_address[8]	11.8	19.1	---	---	50.00	PATH
row_address[9]	12.0	19.0	---	---	50.00	PATH
state_0[0]	16.4	42.6	---	---	50.00	PATH
state_0[10]	18.0	42.7	---	---	50.00	PATH
state_0[11]	17.9	42.8	---	---	50.00	PATH
state_0[12]	18.2	42.9	---	---	50.00	PATH
state_0[13]	17.6	42.9	---	---	50.00	PATH
state_0[14]	17.0	42.8	---	---	50.00	PATH
state_0[15]	18.3	24.4	---	---	50.00	PATH
state_0[1]	17.7	42.6	---	---	50.00	PATH
state_0[2]	17.5	42.7	---	---	50.00	PATH
state_0[3]	17.3	42.8	---	---	50.00	PATH
state_0[4]	17.1	42.7	---	---	50.00	PATH
state_0[5]	17.5	42.8	---	---	50.00	PATH
state_0[6]	17.5	42.7	---	---	50.00	PATH
state_0[7]	17.8	42.8	---	---	50.00	PATH
state_0[8]	17.1	42.7	---	---	50.00	PATH
state_0[9]	17.7	42.9	---	---	50.00	PATH
state_1[0]	16.1	42.3	---	---	50.00	PATH
state_1[10]	16.9	42.3	---	---	50.00	PATH
state_1[11]	17.1	42.5	---	---	50.00	PATH
state_1[12]	16.9	42.4	---	---	50.00	PATH
state_1[13]	17.3	42.5	---	---	50.00	PATH
state_1[14]	16.9	42.5	---	---	50.00	PATH
state_1[15]	18.3	21.9	---	---	50.00	PATH
state_1[1]	17.3	42.2	---	---	50.00	PATH
state_1[2]	17.3	42.2	---	---	50.00	PATH
state_1[3]	18.3	42.3	---	---	50.00	PATH
state_1[4]	17.2	42.3	---	---	50.00	PATH
state_1[5]	16.3	42.3	---	---	50.00	PATH
state_1[6]	17.4	42.5	---	---	50.00	PATH
state_1[7]	17.1	42.4	---	---	50.00	PATH
state_1[8]	17.6	42.4	---	---	50.00	PATH
state_1[9]	16.5	42.3	---	---	50.00	PATH

```
********************************************************************************
        GENESIL Version v8.1DV_Jul_2_Quark -- Wed Jul 17 10:32:43 1991
Chip: /tmp_mnt/nfs/u90/gendv20/wallace/tfil                    Timing Analyzer
********************************************************************************
SETUP AND HOLD MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                    Corner: TYPICAL
  Junction Temperature:102 deg C      Voltage:4.50v
  External Clock: x4_clock
 Included setup files:
  #0  hot_cond              (4.5 volts, 102 degree)
--------------------------------------------------------------------------------
                      INPUT SETUP AND HOLD TIMES (ns)
Input                   Setup Time          Hold Time
                       Ph1(f)   Ph2(f)     Ph1(f)   Ph2(f)
address[0]               9.3     11.8       -2.4     -5.5      PATH
address[1]               8.3      9.1       -2.6     -3.9      PATH
address[2]              10.1     13.5       -2.5     -3.7      PATH
address[3]               9.2     11.1       -2.6     -3.4      PATH
address[4]               7.1     10.7       -1.7     -3.6      PATH
address[5]              14.8     14.0       -6.9     -2.8      PATH
address[6]              13.4     12.7       -6.3     -2.1      PATH
address[7]              12.6     11.8       -5.4     -3.8      PATH
begin_frame_in           ---      2.5        ---     -0.6      PATH
begin_row_in             ---      2.6        ---     -0.7      PATH
data[0]                 5.5       ---       -3.6      ---      PATH
data[10]                 4.9      ---       -3.1      ---      PATH
data[11]                 5.3      ---       -3.4      ---      PATH
data[12]                 5.1      ---       -3.2      ---      PATH
data[13]                 5.0      ---       -3.1      ---      PATH
data[14]                 4.9      ---       -3.0      ---      PATH
data[15]                 5.1      ---       -3.2      ---      PATH
data[1]                  5.6      ---       -3.7      ---      PATH
data[2]                  5.6      ---       -3.7      ---      PATH
data[3]                  5.5      ---       -3.6      ---      PATH
data[4]                  5.5      ---       -3.6      ---      PATH
data[5]                  5.7      ---       -3.8      ---      PATH
data[6]                  5.8      ---       -3.9      ---      PATH
data[7]                  5.6      ---       -3.7      ---      PATH
data[8]                  5.8      ---       -3.9      ---      PATH
data[9]                  5.6      ---       -3.7      ---      PATH
end_frame_in             ---      2.5        ---     -0.6      PATH
end_row_in               ---      2.5        ---     -0.6      PATH
filter_id[0]            14.2     13.4       -6.1     -2.0      PATH
filter_id[1]            13.2     12.4       -5.9     -1.8      PATH
filter_id[2]            12.2     11.5       -5.1     -3.5      PATH
hrd_dev_id[0]           13.3     12.5       -5.7     -1.6      PATH
hrd_dev_id[1]           13.0     12.2       -5.6     -1.5      PATH
hrd_dev_id[2]           13.6     12.8       -6.7     -2.8      PATH
hrd_dev_id[3]           14.0     13.2       -6.3     -2.2      PATH
mm1_control              ---      ---        ---      ---      PATH
n_reset                  4.8      6.1       -2.0     -0.9      PATH
ods_ids[0]              13.4     12.6       -5.9     -1.8      PATH
ods_ids[1]              13.1     12.3       -5.8     -1.6      PATH
ods_ids[2]              13.8     13.0       -6.9     -3.0      PATH
ods_ids[3]              13.4     12.6       -5.9     -1.7      PATH
oe_n_ie                 10.7     11.5       -3.9     -4.6      PATH
p_data_in[0]             ---      2.7        ---     -0.9      PATH
p_data_in[10]            ---      3.0        ---     -1.1      PATH
p_data_in[11]            ---      2.8        ---     -0.9      PATH
p_data_in[12]            ---      2.8        ---     -0.9      PATH
p_data_in[13]            ---      3.1        ---     -1.2      PATH
```

p_data_in[14]	---	3.1	---	-1.2	PATH
p_data_in[15]	---	3.1	---	-1.2	PATH
p_data_in[16]	---	2.9	---	-1.0	PATH
p_data_in[1]	---	2.8	---	-0.9	PATH
p_data_in[2]	---	2.9	---	-1.0	PATH
p_data_in[3]	---	2.8	---	-0.9	PATH
p_data_in[4]	---	2.8	---	-0.9	PATH
p_data_in[5]	---	2.8	---	-0.9	PATH
p_data_in[6]	---	2.6	---	-0.8	PATH
p_data_in[7]	---	2.6	---	-0.7	PATH
p_data_in[8]	---	3.0	---	-1.1	PATH
p_data_in[9]	---	2.7	---	-0.8	PATH
pixel_clock_in	---	3.2	---	-1.3	PATH
state_0[0]	---	2.9	---	-1.0	PATH
state_0[10]	---	3.3	---	-1.4	PATH
state_0[11]	---	3.3	---	-1.4	PATH
state_0[12]	---	3.3	---	-1.4	PATH
state_0[13]	---	3.3	---	-1.5	PATH
state_0[14]	---	3.4	---	-1.5	PATH
state_0[15]	---	3.5	---	-1.6	PATH
state_0[1]	---	3.0	---	-1.1	PATH
state_0[2]	---	3.0	---	-1.1	PATH
state_0[3]	---	3.0	---	-1.1	PATH
state_0[4]	---	3.1	---	-1.2	PATH
state_0[5]	---	3.2	---	-1.3	PATH
state_0[6]	---	3.1	---	-1.2	PATH
state_0[7]	---	3.2	---	-1.3	PATH
state_0[8]	---	3.1	---	-1.3	PATH
state_0[9]	---	3.2	---	-1.3	PATH
state_1[0]	---	2.7	---	-0.8	PATH
state_1[10]	---	2.8	---	-0.9	PATH
state_1[11]	---	2.8	---	-0.9	PATH
state_1[12]	---	3.0	---	-1.1	PATH
state_1[13]	---	3.1	---	-1.2	PATH
state_1[14]	---	3.1	---	-1.2	PATH
state_1[15]	---	3.1	---	-1.2	PATH
state_1[1]	---	2.7	---	-0.8	PATH
state_1[2]	---	2.8	---	-0.9	PATH
state_1[3]	---	2.7	---	-0.8	PATH
state_1[4]	---	2.9	---	-1.0	PATH
state_1[5]	---	2.8	---	-0.9	PATH
state_1[6]	---	2.9	---	-1.0	PATH
state_1[7]	---	2.9	---	-1.0	PATH
state_1[8]	---	3.0	---	-1.1	PATH
state_1[9]	---	2.8	---	-0.9	PATH

```
********************************************************************************
         GENESIL Version v8.1DV_Jul_2_Quark -- Wed Jul 17 10:32:46 1991
Chip: /tmp_mnt/nfs/u90/gendv20/wallace/tfil                      Timing Analyzer
********************************************************************************
VIOLATION MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: TYPICAL
  Junction Temperature:102 deg C        Voltage:4.50v
  External Clock: x4_clock
 Included setup files:
  #0  hot_cond               (4.5 volts, 102 degree)
--------------------------------------------------------------------------------
                                NO VIOLATIONS
  Hold time check margin: 1.5ns
```

13.2. GUARANTEED, 102 T, 4.5 V

```
********************************************************************************
        GENESIL Version v8.1DV_Jul_2_Quark -- Wed Jul 17 10:37:42 1991
Chip: /tmp_mnt/nfs/u90/gendv20/wallace/tfil                    Timing Analyzer
********************************************************************************
CLOCK REPORT MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: GUARANTEED
  Junction Temperature:102 deg C        Voltage:4.50v
  External Clock: x4_clock
 Included setup files:
  #0  hot_cond              (4.5 volts, 102 degree)
--------------------------------------------------------------------------------
                            CLOCK TIMES (minimum)
Phase 1 High:    20.7   ns          Phase 2 High:    20.5   ns
             ----------                          ----------
Cycle (from Ph1):   135.7   ns      Cycle (from Ph2):   152.1   ns
                   ----------                          ----------
Minimum Cycle Time:   152.1   ns    Symmetric Cycle Time:    152.1   ns
                     ----------                          ----------
--------------------------------------------------------------------------------
                            CLOCK WORST CASE PATHS
Minimum Phase 1 high time is    20.7   ns set by:
                               ----------
  ** Clock delay: 4.6ns (25.3-20.7)
   Node                          Cumulative Delay      Transition
   stage0/tfil_7/507                  25.3               fall
   stage0/tfil_7/sa0_load             24.1               rise
   stage0/load_sigs/PORT2_EXT1[0]     24.1               rise
   <age0/load_sigs/PORT2_EXT1[0]'     22.1               rise
   stage0/load_sigs/29                21.7               fall
   stage0/load_sigs/BUS_A[0]          21.3               rise
   tfil_5/sb0_load                    21.1               rise
   tfil_5/sb0_load'                   19.8               rise
   tfil_5/39                          19.5               fall
   tfil_5/29                          18.1               rise
   tfil_5/26                          15.5               fall
   tfil_5/tf_sel                      14.8               rise
   tfil_4/tf_sel                      14.7               rise
   tfil_4/tf_sel'                     13.0               rise
   tfil_4/193                         12.7               fall
   tfil_4/218                          8.4               rise
   tfil_4/214                          5.6               fall
   tfil_4/addr[5]                      4.6               rise
   pre_tfil_4/addr2[5]                 4.6               rise
   pre_tfil_4/addr2[5]'                4.5               rise
   pre_tfil_4/34                       4.1               fall
   pre_tfil_4/pre_addr[5]              3.6               rise
   address[5]/addr                     3.3               rise
   address[5]/addr'                    1.7               rise
   address[5]/1                        1.5               fall
   address[5]                          0.0               rise

Minimum Phase 2 high time is    20.5   ns set by:
                               ----------
  ** Clock delay: 5.4ns (25.9-20.5)
   Node                          Cumulative Delay      Transition
   tfil_4/1786                        25.9               rise
   tfil_4/308                         23.6               fall
   tfil_4/276                         22.4               rise
   tfil_4/190                         20.5               fall
```

```
   tfil_4/221                          19.4              rise
   tfil_4/addr[2]                       5.4              fall
   pre_tfil_4/addr2[2]                  4.9              fall
   pre_tfil_4/addr2[2]'                 3.5              fall
   pre_tfil_4/31                        3.1              rise
   pre_tfil_4/pre_addr[2]               2.0              fall
   address[2]/addr                      1.9              fall
   address[2]/addr'                     1.4              fall
   address[2]/1                         1.1              rise
   address[2]                           0.0              fall

Minimum cycle time (from Ph1) is  135.7    ns set by:
                                  ----------
  ** Clock delay: 11.1ns (146.8-135.7)
   Node                          Cumulative Delay      Transition
   stage0/tfil_8/twos/1177           146.8                fall
   stage0/tfil_8/twos/1176           146.4                rise
   *stage0/tfil_8/twos/1178          145.1                rise
   <e0/tfil_8/twos/INTER0_ST2[33]    144.7                fall
   stage0/tfil_8/twos/1172           143.8                rise
   stage0/tfil_8/twos/1171           142.8                fall
   <e0/tfil_8/twos/INTER4_ST2[33]    142.5                fall
   stage0/tfil_8/twos/1196           142.1                rise
   <0/tfil_8/twos/ADDSUB2_OUT[33]    140.9                fall
   stage0/tfil_8/twos/1186           140.3                rise
   stage0/tfil_8/twos/1190           138.8                rise
   stage0/tfil_8/twos/1194           138.0                fall
   stage0/tfil_8/twos/1159           137.0                rise
   stage0/tfil_8/twos/1124           135.9                fall
   stage0/tfil_8/twos/1089           134.9                rise
   stage0/tfil_8/twos/1043           133.7                fall
   stage0/tfil_8/twos/1041           132.5                rise
   <e0/tfil_8/twos/INTER0_IV1[29]    130.7                fall
   stage0/tfil_8/twos/1033           130.0                rise
   stage0/tfil_8/twos/1034           128.7                rise
   stage0/tfil_8/twos/p[29]          128.3                fall
   stage0/tfil_8/p/p[29]             128.3                fall
   stage0/tfil_8/p/p[29]'            128.0                fall
   stage0/tfil_8/p/238               127.7                rise
   <age0/tfil_8/p/ADDSUB1_OUT[14]    126.5                fall
   stage0/tfil_8/p/228               125.9                rise
   stage0/tfil_8/p/227               124.1                rise
   stage0/tfil_8/p/237               123.4                fall
   stage0/tfil_8/p/221               122.4                rise
   stage0/tfil_8/p/205               121.3                fall
   stage0/tfil_8/p/189               120.3                rise
   stage0/tfil_8/p/173               119.2                fall
   stage0/tfil_8/p/157               118.2                rise
   stage0/tfil_8/p/141               117.1                fall
   stage0/tfil_8/p/125               116.1                rise
   stage0/tfil_8/p/109               115.0                fall
   stage0/tfil_8/p/93                114.0                rise
   stage0/tfil_8/p/77                112.9                fall
   stage0/tfil_8/p/61                112.0                rise
   stage0/tfil_8/p/45                110.8                fall
   stage0/tfil_8/p/29                109.9                rise
   stage0/tfil_8/p/2                 108.6                fall
   stage0/tfil_8/p/1                 107.5                rise
   stage0/tfil_8/p/BUS_A[0]          105.8                fall
   <age0/tfil_8/product/MS_SUM[0]    105.8                fall
   <ge0/tfil_8/product/MS_SUM[0]'    105.0                fall
   stage0/tfil_8/product/161         104.5                rise
```

stage0/tfil_8/product/424	99.4	fall
stage0/tfil_8/product/393	98.6	rise
stage0/tfil_8/product/665	94.5	fall
stage0/tfil_8/product/655	93.8	rise
stage0/tfil_8/product/924	90.0	fall
stage0/tfil_8/product/914	89.3	rise
stage0/tfil_8/product/1184	85.5	fall
stage0/tfil_8/product/1174	84.7	rise
stage0/tfil_8/product/1444	80.9	fall
stage0/tfil_8/product/1434	80.2	rise
stage0/tfil_8/product/1704	76.4	fall
stage0/tfil_8/product/1694	75.7	rise
stage0/tfil_8/product/1964	71.9	fall
stage0/tfil_8/product/1954	71.2	rise
stage0/tfil_8/product/2224	67.3	fall
stage0/tfil_8/product/2214	66.6	rise
stage0/tfil_8/product/2484	62.8	fall
stage0/tfil_8/product/2474	62.1	rise
stage0/tfil_8/product/2744	58.3	fall
stage0/tfil_8/product/2734	57.6	rise
stage0/tfil_8/product/3004	53.8	fall
stage0/tfil_8/product/2994	53.0	rise
stage0/tfil_8/product/3264	49.2	fall
stage0/tfil_8/product/3254	48.5	rise
stage0/tfil_8/product/3420	44.7	fall
stage0/tfil_8/product/3417	44.1	rise
stage0/tfil_8/product/3530	42.9	fall
stage0/tfil_8/product/3525	42.3	rise
<e0/tfil_8/product/mi0_data[3]	41.3	fall
stage0/tfil_15/mux_in_0[3]	41.2	fall
stage0/tfil_15/mux_in_0[3]'	40.0	fall
stage0/tfil_15/137	39.6	rise
stage0/tfil_15/135	37.4	fall
stage0/tfil_15/134	37.0	rise
stage0/tfil_15/111	35.2	fall
stage0/tfil_15/83	34.0	rise
stage0/tfil_15/count[0]	19.7	fall
tfil_1/count[0]	19.5	fall
tfil_1/count[0]'	18.8	fall
tfil_1/85	18.4	rise
tfil_1/86	16.7	fall
tfil_1/90	15.3	rise
tfil_1/92	13.3	fall
tfil_1/635	12.6	rise
tfil_1/634	10.9	fall
tfil_1/94	10.4	rise
tfil_1/192	9.6	fall
tfil_1/PHASE_A	8.7	rise
x4_clock_pad/PHASE_A	6.8	rise
x4_clock	0.0	rise

Minimum cycle time (from Ph2) is 152.1 ns set by:

** Clock delay: 7.8ns (159.9-152.1)

Node	Cumulative Delay	Transition
stage1/tfil_8/twos/1178	159.9	rise
<e1/tfil_8/twos/INTER0_ST2[33]	159.6	fall
stage1/tfil_8/twos/1172	158.6	rise
stage1/tfil_8/twos/1171	157.6	fall
<e1/tfil_8/twos/INTER4_ST2[33]	157.4	fall
stage1/tfil_8/twos/1196	156.9	rise
<1/tfil_8/twos/ADDSUB2_OUT[33]	155.7	fall

stage1/tfil_8/twos/1186	155.1	rise
stage1/tfil_8/twos/1190	153.6	rise
stage1/tfil_8/twos/1194	152.8	fall
stage1/tfil_8/twos/1159	151.8	rise
stage1/tfil_8/twos/1124	150.7	fall
stage1/tfil_8/twos/1089	149.8	rise
stage1/tfil_8/twos/1054	148.7	fall
stage1/tfil_8/twos/1019	147.7	rise
stage1/tfil_8/twos/984	146.6	fall
stage1/tfil_8/twos/949	145.6	rise
stage1/tfil_8/twos/903	144.3	fall
stage1/tfil_8/twos/901	143.2	rise
<e1/tfil_8/twos/INTER0_IV1[25]	141.4	fall
stage1/tfil_8/twos/893	140.7	rise
stage1/tfil_8/twos/894	139.3	rise
stage1/tfil_8/twos/p[25]	139.0	fall
stage1/tfil_8/p/p[25]	139.0	fall
stage1/tfil_8/p/p[25]'	138.6	fall
stage1/tfil_8/p/174	138.3	rise
<age1/tfil_8/p/ADDSUB1_OUT[10]	137.2	fall
stage1/tfil_8/p/164	136.5	rise
stage1/tfil_8/p/163	134.8	rise
stage1/tfil_8/p/173	134.0	fall
stage1/tfil_8/p/157	133.0	rise
stage1/tfil_8/p/141	131.9	fall
stage1/tfil_8/p/125	131.0	rise
stage1/tfil_8/p/109	129.8	fall
stage1/tfil_8/p/93	128.9	rise
stage1/tfil_8/p/77	127.8	fall
stage1/tfil_8/p/61	126.8	rise
stage1/tfil_8/p/45	125.7	fall
stage1/tfil_8/p/29	124.7	rise
stage1/tfil_8/p/2	123.5	fall
stage1/tfil_8/p/1	122.3	rise
stage1/tfil_8/p/BUS_A[0]	120.6	fall
<age1/tfil_8/product/MS_SUM[0]	120.6	fall
<ge1/tfil_8/product/MS_SUM[0]'	119.8	fall
stage1/tfil_8/product/161	119.4	rise
stage1/tfil_8/product/424	114.2	fall
stage1/tfil_8/product/393	113.5	rise
stage1/tfil_8/product/665	109.3	fall
stage1/tfil_8/product/655	108.6	rise
stage1/tfil_8/product/924	104.8	fall
stage1/tfil_8/product/914	104.1	rise
stage1/tfil_8/product/1184	100.3	fall
stage1/tfil_8/product/1174	99.6	rise
stage1/tfil_8/product/1444	95.7	fall
stage1/tfil_8/product/1434	95.0	rise
stage1/tfil_8/product/1704	91.2	fall
stage1/tfil_8/product/1694	90.5	rise
stage1/tfil_8/product/1964	86.7	fall
stage1/tfil_8/product/1954	86.0	rise
stage1/tfil_8/product/2224	82.2	fall
stage1/tfil_8/product/2214	81.4	rise
stage1/tfil_8/product/2484	77.6	fall
stage1/tfil_8/product/2474	76.9	rise
stage1/tfil_8/product/2744	73.1	fall
stage1/tfil_8/product/2734	72.4	rise
stage1/tfil_8/product/3004	68.6	fall
stage1/tfil_8/product/2994	67.9	rise
stage1/tfil_8/product/3264	64.1	fall
stage1/tfil_8/product/3254	63.3	rise

stage1/tfil_8/product/3420	59.5	fall
stage1/tfil_8/product/3417	58.9	rise
stage1/tfil_8/product/3530	57.7	fall
stage1/tfil_8/product/3525	57.1	rise
<e1/tfil_8/product/mi0_data[3]	56.2	fall
stage1/tfil_15/mux_in_0[3]	56.0	fall
stage1/tfil_15/mux_in_0[3]'	54.8	fall
stage1/tfil_15/102	54.5	rise
stage1/tfil_15/80	52.9	fall
stage1/tfil_15/130	49.3	rise
stage1/tfil_15/150	48.7	fall
stage1/tfil_15/81	48.2	rise
stage1/tfil_15/88	41.3	fall
stage1/tfil_15/137	36.9	rise
stage1/tfil_15/output_sel	36.2	fall
tfil_4/output_sel1	35.2	fall
tfil_4/output_sel1'	33.5	fall
tfil_4/472	33.1	rise
tfil_4/198	30.1	fall
tfil_4/1852	29.4	rise
*tfil_4/194	27.1	fall
tfil_4/195	26.6	rise
tfil_4/197	25.5	fall
tfil_4/1834	25.0	rise
tfil_4/199	22.7	fall
tfil_4/205	22.0	rise
tfil_4/190	20.5	fall
tfil_4/221	19.4	rise
tfil_4/addr[2]	5.4	fall
pre_tfil_4/addr2[2]	4.9	fall
pre_tfil_4/addr2[2]'	3.5	fall
pre_tfil_4/31	3.1	rise
pre_tfil_4/pre_addr[2]	2.0	fall
address[2]/addr	1.9	fall
address[2]/addr'	1.4	fall
address[2]/1	1.1	rise
address[2]	0.0	fall

```
**********************************************************************************
        GENESIL Version v8.1DV_Jul_2_Quark -- Wed Jul 17 10:38:13 1991
Chip: /tmp_mnt/nfs/u90/gendv20/wallace/tfil                    Timing Analyzer
**********************************************************************************
OUTPUT DELAY MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                    Corner: GUARANTEED
  Junction Temperature:102 deg C      Voltage:4.50v
  External Clock: x4_clock
 Included setup files:
  #0  hot_cond              (4.5 volts, 102 degree)
--------------------------------------------------------------------------------
                              OUTPUT DELAYS (ns)
Output                  Ph1(r) Delay      Ph2(r) Delay      Loading(pf)
                        Min      Max      Min      Max
begin_frame_out         20.4     23.8     ---      ---      50.00   PATH
begin_row_out           20.5     23.8     ---      ---      50.00   PATH
col_address[0]          18.8     28.8     ---      ---      50.00   PATH
col_address[1]          18.9     28.9     ---      ---      50.00   PATH
col_address[2]          18.9     29.0     ---      ---      50.00   PATH
col_address[3]          18.9     29.0     ---      ---      50.00   PATH
col_address[4]          18.9     28.8     ---      ---      50.00   PATH
col_address[5]          19.0     29.0     ---      ---      50.00   PATH
col_address[6]          20.1     30.0     ---      ---      50.00   PATH
col_address[7]          20.0     29.8     ---      ---      50.00   PATH
col_address[8]          20.0     29.8     ---      ---      50.00   PATH
col_address[9]          20.1     28.8     ---      ---      50.00   PATH
data[0]                 22.1     45.7     22.1     45.7     50.00   PATH
data[10]                19.5     40.5     19.5     40.5     50.00   PATH
data[11]                20.9     48.3     20.9     48.3     50.00   PATH
data[12]                20.8     48.6     20.8     48.6     50.00   PATH
data[13]                19.7     42.0     19.7     42.0     50.00   PATH
data[14]                19.8     40.9     19.8     40.9     50.00   PATH
data[15]                17.0     38.9     17.0     38.9     50.00   PATH
data[1]                 22.2     55.2     22.2     55.2     50.00   PATH
data[2]                 22.2     51.1     22.2     51.1     50.00   PATH
data[3]                 22.2     50.7     22.2     50.7     50.00   PATH
data[4]                 18.7     49.7     18.7     49.7     50.00   PATH
data[5]                 21.8     44.7     21.8     44.7     50.00   PATH
data[6]                 18.1     41.0     18.1     41.0     50.00   PATH
data[7]                 18.7     47.3     18.7     47.3     50.00   PATH
data[8]                 20.8     47.5     20.8     47.5     50.00   PATH
data[9]                 19.2     42.4     19.2     42.4     50.00   PATH
device_ready            19.4     24.2     19.4     24.2     50.00   PATH
end_frame_out           20.3     23.8     ---      ---      50.00   PATH
end_row_out             20.7     24.0     ---      ---      50.00   PATH
mm0_csel[0]             24.9     36.1     ---      ---      50.00   PATH
mm0_csel[1]             25.3     38.9     ---      ---      50.00   PATH
mm1_csel[0]             17.8     39.0     17.8     21.7     50.00   PATH
mm1_csel[1]             19.6     39.0     19.6     20.2     50.00   PATH
mm1_csel[2]             17.6     39.8     17.6     21.6     50.00   PATH
mm1_csel[3]             19.5     39.7     19.5     20.1     50.00   PATH
n_write_en[0]           17.2     17.2     21.9     21.9     50.00   PATH
n_write_en[1]           17.7     17.7     22.6     22.6     50.00   PATH
p_data_out[0]           21.6     24.8     ---      ---      50.00   PATH
p_data_out[10]          21.2     24.6     ---      ---      50.00   PATH
p_data_out[11]          21.3     24.6     ---      ---      50.00   PATH
p_data_out[12]          21.3     24.6     ---      ---      50.00   PATH
p_data_out[13]          21.3     24.6     ---      ---      50.00   PATH
p_data_out[14]          21.1     24.5     ---      ---      50.00   PATH
p_data_out[15]          21.2     24.6     ---      ---      50.00   PATH
p_data_out[16]          20.2     23.6     ---      ---      50.00   PATH
```

p_data_out[1]	21.6	24.9	---	---	50.00	PATH
p_data_out[2]	21.5	24.8	---	---	50.00	PATH
p_data_out[3]	21.6	24.8	---	---	50.00	PATH
p_data_out[4]	21.5	24.7	---	---	50.00	PATH
p_data_out[5]	21.5	24.7	---	---	50.00	PATH
p_data_out[6]	21.4	24.7	---	---	50.00	PATH
p_data_out[7]	21.3	24.6	---	---	50.00	PATH
p_data_out[8]	21.4	24.8	---	---	50.00	PATH
p_data_out[9]	21.3	24.6	---	---	50.00	PATH
row_address[0]	18.6	28.7	---	---	50.00	PATH
row_address[1]	18.5	28.7	---	---	50.00	PATH
row_address[2]	18.5	28.5	---	---	50.00	PATH
row_address[3]	18.6	28.7	---	---	50.00	PATH
row_address[4]	18.7	28.6	---	---	50.00	PATH
row_address[5]	18.8	28.7	---	---	50.00	PATH
row_address[6]	18.9	29.6	---	---	50.00	PATH
row_address[7]	18.9	28.7	---	---	50.00	PATH
row_address[8]	18.9	29.3	---	---	50.00	PATH
row_address[9]	19.2	29.2	---	---	50.00	PATH
state_0[0]	26.5	67.6	---	---	50.00	PATH
state_0[10]	29.0	67.9	---	---	50.00	PATH
state_0[11]	28.8	68.0	---	---	50.00	PATH
state_0[12]	29.4	68.2	---	---	50.00	PATH
state_0[13]	28.5	68.3	---	---	50.00	PATH
state_0[14]	27.6	68.2	---	---	50.00	PATH
state_0[15]	30.3	39.2	---	---	50.00	PATH
state_0[1]	28.4	67.7	---	---	50.00	PATH
state_0[2]	28.0	67.8	---	---	50.00	PATH
state_0[3]	27.9	68.0	---	---	50.00	PATH
state_0[4]	27.4	67.7	---	---	50.00	PATH
state_0[5]	28.3	68.0	---	---	50.00	PATH
state_0[6]	28.3	67.9	---	---	50.00	PATH
state_0[7]	28.7	68.1	---	---	50.00	PATH
state_0[8]	27.6	67.8	---	---	50.00	PATH
state_0[9]	28.4	68.1	---	---	50.00	PATH
state_1[0]	25.5	66.2	---	---	50.00	PATH
state_1[10]	26.8	66.2	---	---	50.00	PATH
state_1[11]	27.1	66.5	---	---	50.00	PATH
state_1[12]	26.7	66.4	---	---	50.00	PATH
state_1[13]	27.4	66.5	---	---	50.00	PATH
state_1[14]	26.8	66.6	---	---	50.00	PATH
state_1[15]	29.5	33.9	---	---	50.00	PATH
state_1[1]	27.3	66.0	---	---	50.00	PATH
state_1[2]	27.2	66.0	---	---	50.00	PATH
state_1[3]	29.0	66.1	---	---	50.00	PATH
state_1[4]	27.1	66.1	---	---	50.00	PATH
state_1[5]	25.8	66.2	---	---	50.00	PATH
state_1[6]	27.5	66.4	---	---	50.00	PATH
state_1[7]	27.0	66.3	---	---	50.00	PATH
state_1[8]	27.9	66.4	---	---	50.00	PATH
state_1[9]	26.1	66.2	---	---	50.00	PATH

```
********************************************************************************
        GENESIL Version v8.1DV_Jul_2_Quark -- Wed Jul 17 10:40:19 1991
Chip: /tmp_mnt/nfs/u90/gendv20/wallace/tfil                    Timing Analyzer
********************************************************************************
SETUP AND HOLD MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                    Corner: GUARANTEED
  Junction Temperature:102 deg C      Voltage:4.50v
  External Clock: x4_clock
 Included setup files:
  #0  hot_cond              (4.5 volts, 102 degree)
--------------------------------------------------------------------------------
                      INPUT SETUP AND HOLD TIMES (ns)
Input                   Setup Time          Hold Time
                       Ph1(f)   Ph2(f)     Ph1(f)   Ph2(f)
address[0]              13.2     16.8       -4.4     -6.4      PATH
address[1]              11.2     12.1       -3.3     -4.5      PATH
address[2]              14.1     19.4       -3.3     -3.9      PATH
address[3]              12.8     16.1       -3.6     -3.6      PATH
address[4]               9.9     15.4       -0.8     -3.7      PATH
address[5]              21.8     20.5       -9.7     -2.2      PATH
address[6]              19.8     18.5       -8.8     -1.3      PATH
address[7]              18.2     16.9       -7.7     -4.1      PATH
begin_frame_in           ---      1.5        ---      1.3      PATH
begin_row_in             ---      1.6        ---      1.2      PATH
data[0]                  7.7      ---       -3.6      ---      PATH
data[10]                 6.3      ---       -3.0      ---      PATH
data[11]                 7.2      ---       -3.7      ---      PATH
data[12]                 6.7      ---       -3.4      ---      PATH
data[13]                 6.4      ---       -3.1      ---      PATH
data[14]                 6.0      ---       -3.0      ---      PATH
data[15]                 6.4      ---       -3.4      ---      PATH
data[1]                  7.8      ---       -3.8      ---      PATH
data[2]                  7.9      ---       -3.8      ---      PATH
data[3]                  7.7      ---       -3.7      ---      PATH
data[4]                  7.7      ---       -3.7      ---      PATH
data[5]                  8.1      ---       -4.0      ---      PATH
data[6]                  8.7      ---       -4.8      ---      PATH
data[7]                  8.3      ---       -4.4      ---      PATH
data[8]                  8.5      ---       -4.7      ---      PATH
data[9]                  8.3      ---       -4.5      ---      PATH
end_frame_in             ---      1.5        ---      1.4      PATH
end_row_in               ---      1.5        ---      1.3      PATH
filter_id[0]            20.7     19.4       -8.3     -0.8      PATH
filter_id[1]            19.1     17.8       -7.9     -0.4      PATH
filter_id[2]            17.5     16.2       -6.9     -3.4      PATH
hrd_dev_id[0]           19.2     17.9       -7.6     -0.1      PATH
hrd_dev_id[1]           18.8     17.5       -7.5      0.1      PATH
hrd_dev_id[2]           19.8     18.5       -9.4     -2.3      PATH
hrd_dev_id[3]           20.4     19.1       -8.7     -1.2      PATH
mml_control              ---      ---        ---      ---      PATH
n_reset                  5.7      7.7       -1.6      0.3      PATH
ods_ids[0]              19.3     18.0       -7.9     -0.4      PATH
ods_ids[1]              18.8     17.5       -7.7     -0.2      PATH
ods_ids[2]              20.0     18.8       -9.9     -2.7      PATH
ods_ids[3]              19.4     18.1       -7.9     -0.4      PATH
oe_n_ie                 15.3     16.5       -5.5     -5.5      PATH
p_data_in[0]             ---      2.0        ---      0.8      PATH
p_data_in[10]            ---      2.5        ---      0.4      PATH
p_data_in[11]            ---      2.0        ---      0.8      PATH
p_data_in[12]            ---      2.0        ---      0.8      PATH
p_data_in[13]            ---      2.7        ---      0.2      PATH
```

p_data_in[14]	---	2.8	---	0.1	PATH
p_data_in[15]	---	2.8	---	0.1	PATH
p_data_in[16]	---	2.3	---	0.6	PATH
p_data_in[1]	---	2.1	---	0.7	PATH
p_data_in[2]	---	2.2	---	0.6	PATH
p_data_in[3]	---	2.1	---	0.7	PATH
p_data_in[4]	---	2.2	---	0.7	PATH
p_data_in[5]	---	2.2	---	0.7	PATH
p_data_in[6]	---	1.8	---	1.1	PATH
p_data_in[7]	---	1.8	---	1.1	PATH
p_data_in[8]	---	2.5	---	0.4	PATH
p_data_in[9]	---	2.0	---	0.9	PATH
pixel_clock_in	---	2.9	---	-0.1	PATH
state_0[0]	---	2.1	---	0.7	PATH
state_0[10]	---	3.1	---	-0.2	PATH
state_0[11]	---	3.0	---	-0.1	PATH
state_0[12]	---	3.0	---	-0.1	PATH
state_0[13]	---	3.1	---	-0.2	PATH
state_0[14]	---	3.1	---	-0.2	PATH
state_0[15]	---	3.3	---	-0.4	PATH
state_0[1]	---	2.3	---	0.6	PATH
state_0[2]	---	2.4	---	0.5	PATH
state_0[3]	---	2.5	---	0.4	PATH
state_0[4]	---	2.6	---	0.3	PATH
state_0[5]	---	2.7	---	0.2	PATH
state_0[6]	---	2.6	---	0.3	PATH
state_0[7]	---	2.8	---	0.1	PATH
state_0[8]	---	2.7	---	0.2	PATH
state_0[9]	---	2.8	---	0.0	PATH
state_1[0]	---	2.1	---	0.8	PATH
state_1[10]	---	2.3	---	0.6	PATH
state_1[11]	---	2.3	---	0.6	PATH
state_1[12]	---	2.6	---	0.3	PATH
state_1[13]	---	2.8	---	0.1	PATH
state_1[14]	---	2.8	---	0.1	PATH
state_1[15]	---	2.9	---	-0.0	PATH
state_1[1]	---	2.1	---	0.8	PATH
state_1[2]	---	2.3	---	0.5	PATH
state_1[3]	---	2.0	---	0.8	PATH
state_1[4]	---	2.4	---	0.4	PATH
state_1[5]	---	2.3	---	0.6	PATH
state_1[6]	---	2.5	---	0.4	PATH
state_1[7]	---	2.5	---	0.4	PATH
state_1[8]	---	2.6	---	0.2	PATH
state_1[9]	---	2.3	---	0.6	PATH

```
 ********************************************************************************
        GENESIL Version v8.1DV_Jul_2_Quark -- Wed Jul 17 10:40:22 1991
Chip: /tmp_mnt/nfs/u90/gendv20/wallace/tfil                    Timing Analyzer
 ********************************************************************************
VIOLATION MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: GUARANTEED
  Junction Temperature:102 deg C        Voltage:4.50v
  External Clock: x4_clock
 Included setup files:
  #0  hot_cond               (4.5 volts, 102 degree)
--------------------------------------------------------------------------------
                                NO VIOLATIONS
  Hold time check margin: 1.5ns
```

13.3. TYPICAL, 57 T, 5.0 V

```
********************************************************************************
        GENESIL Version v8.1DV_Jul_2_Quark -- Wed Jul 17 10:33:02 1991
Chip: /tmp_mnt/nfs/u90/gendv20/wallace/tfil                    Timing Analyzer
********************************************************************************
CLOCK REPORT MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: TYPICAL
  Junction Temperature:57 deg C         Voltage:5.00v
  External Clock: x4_clock
 Included setup files:
  #0  room_cond              (5.0 volts, 57 degree)
--------------------------------------------------------------------------------
                              CLOCK TIMES (minimum)
Phase 1 High:    11.7   ns             Phase 2 High:    11.7   ns
                 ----------                            ----------
Cycle (from Ph1):    72.6   ns        Cycle (from Ph2):    81.6   ns
                     ----------                          ----------
Minimum Cycle Time:    81.6   ns      Symmetric Cycle Time:     81.6   ns
                       ----------                          ----------
--------------------------------------------------------------------------------
                              CLOCK WORST CASE PATHS
Minimum Phase 1 high time is    11.7   ns set by:
                                ----------
  ** Clock delay: 1.3ns (13.0-11.7)
   Node                              Cumulative Delay      Transition
   stage0/tfil_7/507                      13.0                fall
   stage0/tfil_7/sa0_load                 12.3                rise
   stage0/load_sigs/PORT2_EXT1[0]         12.3                rise
   <age0/load_sigs/PORT2_EXT1[0]'         11.3                rise
   stage0/load_sigs/29                    11.0                fall
   stage0/load_sigs/BUS_A[0]              10.8                rise
   tfil_5/sb0_load                        10.8                rise
   tfil_5/sb0_load'                       10.2                rise
   tfil_5/39                              10.0                fall
   tfil_5/29                               9.3                rise
   tfil_5/26                               7.9                fall
   tfil_5/tf_sel                           7.5                rise
   tfil_4/tf_sel                           7.5                rise
   tfil_4/tf_sel'                          6.7                rise
   tfil_4/193                              6.5                fall
   tfil_4/218                              4.2                rise
   tfil_4/214                              2.8                fall
   tfil_4/addr[5]                          2.3                rise
   pre_tfil_4/addr2[5]                     2.3                rise
   pre_tfil_4/addr2[5]'                    2.2                rise
   pre_tfil_4/34                           2.0                fall
   pre_tfil_4/pre_addr[5]                  1.7                rise
   address[5]/addr                         1.7                rise
   address[5]/addr'                        1.0                rise
   address[5]/1                            0.8                fall
   address[5]                              0.0                rise

Minimum Phase 2 high time is    11.7   ns set by:
                                ----------
  ** Clock delay: 1.6ns (13.3-11.7)
   Node                              Cumulative Delay      Transition
   tfil_4/1786                            13.3                rise
   tfil_4/308                             12.0                fall
   tfil_4/276                             11.4                rise
   tfil_4/190                             10.4                fall
```

```
   tfil_4/221                          9.8              rise
   tfil_4/addr[2]                      2.6              fall
   pre_tfil_4/addr2[2]                 2.6              fall
   pre_tfil_4/addr2[2]'                1.8              fall
   pre_tfil_4/31                       1.6              rise
   pre_tfil_4/pre_addr[2]              1.0              fall
   address[2]/addr                     1.0              fall
   address[2]/addr'                    0.7              fall
   address[2]/1                        0.6              rise
   address[2]                          0.0              fall

Minimum cycle time (from Ph1) is   72.6    ns set by:
                                  ----------
  ** Clock delay: 4.9ns (77.5-72.6)
   Node                          Cumulative Delay      Transition
   stage0/tfil_9/twos/1177            77.5              fall
   stage0/tfil_9/twos/1176            77.3              rise
   *stage0/tfil_9/twos/1178           76.6              rise
   <e0/tfil_9/twos/INTER0_ST2[33]     76.4              fall
   stage0/tfil_9/twos/1172            75.9              rise
   stage0/tfil_9/twos/1171            75.4              fall
   <e0/tfil_9/twos/INTER4_ST2[33]     75.2              fall
   stage0/tfil_9/twos/1196            75.0              rise
   <0/tfil_9/twos/ADDSUB2_OUT[33]     74.4              fall
   stage0/tfil_9/twos/1186            74.0              rise
   stage0/tfil_9/twos/1190            73.3              rise
   stage0/tfil_9/twos/1194            72.9              fall
   stage0/tfil_9/twos/1159            72.3              rise
   stage0/tfil_9/twos/1124            71.7              fall
   stage0/tfil_9/twos/1089            71.2              rise
   stage0/tfil_9/twos/1043            70.6              fall
   stage0/tfil_9/twos/1041            69.9              rise
   <e0/tfil_9/twos/INTER0_IV1[29]     69.0              fall
   stage0/tfil_9/twos/1033            68.6              rise
   stage0/tfil_9/twos/1034            67.9              rise
   stage0/tfil_9/twos/p[29]           67.7              fall
   stage0/tfil_9/p/p[29]              67.7              fall
   stage0/tfil_9/p/p[29]'             67.5              fall
   stage0/tfil_9/p/238                67.3              rise
   <age0/tfil_9/p/ADDSUB1_OUT[14]     66.7              fall
   stage0/tfil_9/p/228                66.4              rise
   stage0/tfil_9/p/227                65.5              rise
   stage0/tfil_9/p/237                65.1              fall
   stage0/tfil_9/p/221                64.6              rise
   stage0/tfil_9/p/205                64.0              fall
   stage0/tfil_9/p/189                63.4              rise
   stage0/tfil_9/p/173                62.9              fall
   stage0/tfil_9/p/157                62.3              rise
   stage0/tfil_9/p/141                61.8              fall
   stage0/tfil_9/p/125                61.2              rise
   stage0/tfil_9/p/109                60.6              fall
   stage0/tfil_9/p/93                 60.1              rise
   stage0/tfil_9/p/77                 59.5              fall
   stage0/tfil_9/p/61                 59.0              rise
   stage0/tfil_9/p/45                 58.4              fall
   stage0/tfil_9/p/29                 57.9              rise
   stage0/tfil_9/p/2                  57.2              fall
   stage0/tfil_9/p/1                  56.6              rise
   stage0/tfil_9/p/BUS_A[0]           55.7              fall
   <age0/tfil_9/product/MS_SUM[0]     55.7              fall
   <ge0/tfil_9/product/MS_SUM[0]'     55.3              fall
   stage0/tfil_9/product/161          55.0              rise
```

```
   stage0/tfil_9/product/424          52.3              fall
   stage0/tfil_9/product/393          51.8              rise
   stage0/tfil_9/product/665          49.7              fall
   stage0/tfil_9/product/655          49.2              rise
   stage0/tfil_9/product/924          47.2              fall
   stage0/tfil_9/product/914          46.8              rise
   stage0/tfil_9/product/1184         44.8              fall
   stage0/tfil_9/product/1174         44.4              rise
   stage0/tfil_9/product/1444         42.3              fall
   stage0/tfil_9/product/1434         41.9              rise
   stage0/tfil_9/product/1704         39.9              fall
   stage0/tfil_9/product/1694         39.5              rise
   stage0/tfil_9/product/1964         37.4              fall
   stage0/tfil_9/product/1954         37.0              rise
   stage0/tfil_9/product/2224         35.0              fall
   stage0/tfil_9/product/2214         34.6              rise
   stage0/tfil_9/product/2484         32.5              fall
   stage0/tfil_9/product/2474         32.1              rise
   stage0/tfil_9/product/2744         30.1              fall
   stage0/tfil_9/product/2734         29.7              rise
   stage0/tfil_9/product/3004         27.6              fall
   stage0/tfil_9/product/2994         27.2              rise
   stage0/tfil_9/product/3264         25.2              fall
   stage0/tfil_9/product/3254         24.8              rise
   stage0/tfil_9/product/3420         22.8              fall
   stage0/tfil_9/product/3417         22.4              rise
   stage0/tfil_9/product/3530         21.7              fall
   stage0/tfil_9/product/3525         21.4              rise
   <e0/tfil_9/product/mi0_data[3]     20.9              fall
   stage0/tfil_15/mux_in_0[3]         20.9              fall
   stage0/tfil_15/mux_in_0[3]'        20.2              fall
   stage0/tfil_15/137                 20.0              rise
   stage0/tfil_15/135                 18.8              fall
   stage0/tfil_15/134                 18.6              rise
   stage0/tfil_15/111                 17.7              fall
   stage0/tfil_15/83                  17.0              rise
   stage0/tfil_15/count[0]             9.5              fall
   tfil_1/count[0]                     9.5              fall
   tfil_1/count[0]'                    9.1              fall
   tfil_1/85                           8.9              rise
   tfil_1/86                           8.0              fall
   tfil_1/90                           7.2              rise
   tfil_1/92                           6.1              fall
   tfil_1/635                          5.7              rise
   tfil_1/634                          4.8              fall
   tfil_1/94                           4.5              rise
   tfil_1/192                          4.1              fall
   tfil_1/PHASE_A                      3.6              rise
   x4_clock_pad/PHASE_A                3.6              rise
   x4_clock                            0.0              rise

Minimum cycle time (from Ph2) is   81.6    ns set by:
                                  ----------
  ** Clock delay: 3.2ns (84.8-81.6)
   Node                          Cumulative Delay      Transition
   stage1/tfil_8/twos/1178            84.8                rise
   <e1/tfil_8/twos/INTER0_ST2[33]     84.7                fall
   stage1/tfil_8/twos/1172            84.1                rise
   stage1/tfil_8/twos/1171            83.6                fall
   <e1/tfil_8/twos/INTER4_ST2[33]     83.5                fall
   stage1/tfil_8/twos/1196            83.2                rise
   <1/tfil_8/twos/ADDSUB2_OUT[33]     82.6                fall
```

stage1/tfil_8/twos/1186	82.3	rise
stage1/tfil_8/twos/1190	81.5	rise
stage1/tfil_8/twos/1194	81.1	fall
stage1/tfil_8/twos/1159	80.6	rise
stage1/tfil_8/twos/1124	80.0	fall
stage1/tfil_8/twos/1089	79.5	rise
stage1/tfil_8/twos/1054	78.9	fall
stage1/tfil_8/twos/1019	78.3	rise
stage1/tfil_8/twos/984	77.8	fall
stage1/tfil_8/twos/949	77.2	rise
stage1/tfil_8/twos/914	76.6	fall
stage1/tfil_8/twos/879	76.1	rise
stage1/tfil_8/twos/844	75.5	fall
stage1/tfil_8/twos/809	75.0	rise
stage1/tfil_8/twos/774	74.4	fall
stage1/tfil_8/twos/739	73.9	rise
stage1/tfil_8/twos/704	73.3	fall
stage1/tfil_8/twos/669	72.7	rise
stage1/tfil_8/twos/623	72.1	fall
stage1/tfil_8/twos/621	71.5	rise
<e1/tfil_8/twos/INTER0_IV1[17]	70.5	fall
stage1/tfil_8/twos/613	70.1	rise
stage1/tfil_8/twos/614	69.4	rise
stage1/tfil_8/twos/p[17]	69.2	fall
stage1/tfil_8/p/p[17]	69.2	fall
stage1/tfil_8/p/p[17]'	69.1	fall
stage1/tfil_8/p/46	68.9	rise
stage1/tfil_8/p/ADDSUB1_OUT[2]	68.3	fall
stage1/tfil_8/p/36	67.9	rise
stage1/tfil_8/p/35	67.0	rise
stage1/tfil_8/p/45	66.7	fall
stage1/tfil_8/p/29	66.1	rise
stage1/tfil_8/p/2	65.5	fall
stage1/tfil_8/p/1	64.8	rise
stage1/tfil_8/p/BUS_A[0]	63.9	fall
<age1/tfil_8/product/MS_SUM[0]	63.9	fall
<ge1/tfil_8/product/MS_SUM[0]'	63.5	fall
stage1/tfil_8/product/161	63.3	rise
stage1/tfil_8/product/424	60.5	fall
stage1/tfil_8/product/393	60.1	rise
stage1/tfil_8/product/665	57.9	fall
stage1/tfil_8/product/655	57.5	rise
stage1/tfil_8/product/924	55.5	fall
stage1/tfil_8/product/914	55.1	rise
stage1/tfil_8/product/1184	53.0	fall
stage1/tfil_8/product/1174	52.6	rise
stage1/tfil_8/product/1444	50.6	fall
stage1/tfil_8/product/1434	50.2	rise
stage1/tfil_8/product/1704	48.1	fall
stage1/tfil_8/product/1694	47.7	rise
stage1/tfil_8/product/1964	45.7	fall
stage1/tfil_8/product/1954	45.3	rise
stage1/tfil_8/product/2224	43.2	fall
stage1/tfil_8/product/2214	42.8	rise
stage1/tfil_8/product/2484	40.8	fall
stage1/tfil_8/product/2474	40.4	rise
stage1/tfil_8/product/2744	38.3	fall
stage1/tfil_8/product/2734	37.9	rise
stage1/tfil_8/product/3004	35.9	fall
stage1/tfil_8/product/2994	35.5	rise
stage1/tfil_8/product/3264	33.5	fall
stage1/tfil_8/product/3254	33.0	rise

stage1/tfil_8/product/3420	31.0	fall
stage1/tfil_8/product/3417	30.6	rise
stage1/tfil_8/product/3530	30.0	fall
stage1/tfil_8/product/3525	29.6	rise
<e1/tfil_8/product/mi0_data[3]	29.2	fall
stage1/tfil_15/mux_in_0[3]	29.2	fall
stage1/tfil_15/mux_in_0[3]'	28.5	fall
stage1/tfil_15/102	28.3	rise
stage1/tfil_15/80	27.5	fall
stage1/tfil_15/130	25.4	rise
stage1/tfil_15/150	25.1	fall
stage1/tfil_15/81	24.8	rise
stage1/tfil_15/88	21.2	fall
stage1/tfil_15/137	18.7	rise
stage1/tfil_15/output_sel	18.4	fall
tfil_4/output_sel1	18.4	fall
tfil_4/output_sel1'	17.5	fall
tfil_4/472	17.3	rise
tfil_4/198	15.7	fall
tfil_4/1852	15.2	rise
*tfil_4/194	14.0	fall
tfil_4/195	13.7	rise
tfil_4/197	13.1	fall
tfil_4/1834	12.8	rise
tfil_4/199	11.6	fall
tfil_4/205	11.2	rise
tfil_4/190	10.4	fall
tfil_4/221	9.8	rise
tfil_4/addr[2]	2.6	fall
pre_tfil_4/addr2[2]	2.6	fall
pre_tfil_4/addr2[2]'	1.8	fall
pre_tfil_4/31	1.6	rise
pre_tfil_4/pre_addr[2]	1.0	fall
address[2]/addr	1.0	fall
address[2]/addr'	0.7	fall
address[2]/1	0.6	rise
address[2]	0.0	fall

```
********************************************************************************
        GENESIL Version v8.1DV_Jul_2_Quark -- Wed Jul 17 10:33:03 1991
Chip: /tmp_mnt/nfs/u90/gendv20/wallace/tfil                    Timing Analyzer
********************************************************************************
OUTPUT DELAY MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                    Corner: TYPICAL
  Junction Temperature:57 deg C       Voltage:5.00v
  External Clock: x4_clock
 Included setup files:
  #0  room_cond              (5.0 volts, 57 degree)
--------------------------------------------------------------------------------
                              OUTPUT DELAYS (ns)
Output                  Ph1(r) Delay      Ph2(r) Delay      Loading(pf)
                        Min      Max      Min      Max
begin_frame_out          10.5     12.6      ---      ---     50.00   PATH
begin_row_out            10.5     12.6      ---      ---     50.00   PATH
col_address[0]            9.7     15.5      ---      ---     50.00   PATH
col_address[1]            9.7     15.5      ---      ---     50.00   PATH
col_address[2]            9.7     15.6      ---      ---     50.00   PATH
col_address[3]            9.7     15.6      ---      ---     50.00   PATH
col_address[4]            9.7     15.5      ---      ---     50.00   PATH
col_address[5]            9.7     15.6      ---      ---     50.00   PATH
col_address[6]           10.1     15.9      ---      ---     50.00   PATH
col_address[7]           10.1     15.8      ---      ---     50.00   PATH
col_address[8]           10.1     15.8      ---      ---     50.00   PATH
col_address[9]           10.1     15.3      ---      ---     50.00   PATH
data[0]                  11.7     23.8     11.7     23.8     50.00   PATH
data[10]                 10.6     21.4     10.6     21.4     50.00   PATH
data[11]                 11.5     25.2     11.5     25.2     50.00   PATH
data[12]                 11.5     25.3     11.5     25.3     50.00   PATH
data[13]                 10.5     22.2     10.5     22.2     50.00   PATH
data[14]                 10.7     21.6     10.7     21.6     50.00   PATH
data[15]                  9.2     20.7      9.2     20.7     50.00   PATH
data[1]                  12.0     28.2     12.0     28.2     50.00   PATH
data[2]                  12.0     26.4     12.0     26.4     50.00   PATH
data[3]                  12.0     26.1     12.0     26.1     50.00   PATH
data[4]                  10.4     25.6     10.4     25.6     50.00   PATH
data[5]                  11.8     23.4     11.8     23.4     50.00   PATH
data[6]                  10.0     21.5     10.0     21.5     50.00   PATH
data[7]                  10.4     24.5     10.4     24.5     50.00   PATH
data[8]                  11.4     24.6     11.4     24.6     50.00   PATH
data[9]                  10.5     22.1     10.5     22.1     50.00   PATH
device_ready             11.1     13.5     11.1     13.5     50.00   PATH
end_frame_out            10.4     12.6      ---      ---     50.00   PATH
end_row_out              10.6     12.7      ---      ---     50.00   PATH
mm0_csel[0]              12.8     19.1      ---      ---     50.00   PATH
mm0_csel[1]              13.1     20.6      ---      ---     50.00   PATH
mm1_csel[0]               9.8     20.6      9.8     12.3     50.00   PATH
mm1_csel[1]              10.9     20.6     10.9     11.5     50.00   PATH
mm1_csel[2]               9.7     21.1      9.7     12.3     50.00   PATH
mm1_csel[3]              10.9     21.1     10.9     11.4     50.00   PATH
n_write_en[0]             8.6      8.6     11.6     11.6     50.00   PATH
n_write_en[1]             8.8      8.8     11.9     11.9     50.00   PATH
p_data_out[0]            11.1     13.2      ---      ---     50.00   PATH
p_data_out[10]           11.0     13.2      ---      ---     50.00   PATH
p_data_out[11]           11.0     13.2      ---      ---     50.00   PATH
p_data_out[12]           11.0     13.1      ---      ---     50.00   PATH
p_data_out[13]           11.0     13.1      ---      ---     50.00   PATH
p_data_out[14]           10.9     13.1      ---      ---     50.00   PATH
p_data_out[15]           11.0     13.1      ---      ---     50.00   PATH
p_data_out[16]           10.5     12.6      ---      ---     50.00   PATH
```

p_data_out[1]	11.1	13.3	---	---	50.00	PATH
p_data_out[2]	11.1	13.2	---	---	50.00	PATH
p_data_out[3]	11.1	13.2	---	---	50.00	PATH
p_data_out[4]	11.1	13.2	---	---	50.00	PATH
p_data_out[5]	11.1	13.2	---	---	50.00	PATH
p_data_out[6]	11.1	13.2	---	---	50.00	PATH
p_data_out[7]	11.0	13.1	---	---	50.00	PATH
p_data_out[8]	11.1	13.2	---	---	50.00	PATH
p_data_out[9]	11.0	13.2	---	---	50.00	PATH
row_address[0]	9.6	15.5	---	---	50.00	PATH
row_address[1]	9.5	15.5	---	---	50.00	PATH
row_address[2]	9.5	15.4	---	---	50.00	PATH
row_address[3]	9.6	15.5	---	---	50.00	PATH
row_address[4]	9.6	15.4	---	---	50.00	PATH
row_address[5]	9.6	15.5	---	---	50.00	PATH
row_address[6]	9.7	15.8	---	---	50.00	PATH
row_address[7]	9.7	15.5	---	---	50.00	PATH
row_address[8]	9.7	15.7	---	---	50.00	PATH
row_address[9]	9.9	15.7	---	---	50.00	PATH
state_0[0]	13.6	35.1	---	---	50.00	PATH
state_0[10]	14.9	35.2	---	---	50.00	PATH
state_0[11]	14.8	35.2	---	---	50.00	PATH
state_0[12]	15.0	35.3	---	---	50.00	PATH
state_0[13]	14.5	35.3	---	---	50.00	PATH
state_0[14]	14.0	35.3	---	---	50.00	PATH
state_0[15]	15.0	20.0	---	---	50.00	PATH
state_0[1]	14.6	35.1	---	---	50.00	PATH
state_0[2]	14.4	35.2	---	---	50.00	PATH
state_0[3]	14.3	35.3	---	---	50.00	PATH
state_0[4]	14.1	35.1	---	---	50.00	PATH
state_0[5]	14.5	35.2	---	---	50.00	PATH
state_0[6]	14.5	35.2	---	---	50.00	PATH
state_0[7]	14.7	35.3	---	---	50.00	PATH
state_0[8]	14.1	35.2	---	---	50.00	PATH
state_0[9]	14.6	35.3	---	---	50.00	PATH
state_1[0]	13.2	34.9	---	---	50.00	PATH
state_1[10]	14.0	34.8	---	---	50.00	PATH
state_1[11]	14.1	35.0	---	---	50.00	PATH
state_1[12]	14.0	34.9	---	---	50.00	PATH
state_1[13]	14.3	35.0	---	---	50.00	PATH
state_1[14]	14.0	35.0	---	---	50.00	PATH
state_1[15]	15.0	18.0	---	---	50.00	PATH
state_1[1]	14.3	34.7	---	---	50.00	PATH
state_1[2]	14.3	34.8	---	---	50.00	PATH
state_1[3]	15.0	34.8	---	---	50.00	PATH
state_1[4]	14.2	34.8	---	---	50.00	PATH
state_1[5]	13.5	34.8	---	---	50.00	PATH
state_1[6]	14.4	35.0	---	---	50.00	PATH
state_1[7]	14.1	34.9	---	---	50.00	PATH
state_1[8]	14.6	34.9	---	---	50.00	PATH
state_1[9]	13.6	34.9	---	---	50.00	PATH

```
**********************************************************************************
        GENESIL Version v8.1DV_Jul_2_Quark -- Wed Jul 17 10:35:14 1991
Chip: /tmp_mnt/nfs/u90/gendv20/wallace/tfil                    Timing Analyzer
**********************************************************************************
SETUP AND HOLD MODE
----------------------------------------------------------------------------------
Fabline: HP2_CN10B                    Corner: TYPICAL
  Junction Temperature:57 deg C       Voltage:5.00v
  External Clock: x4_clock
 Included setup files:
  #0  room_cond              (5.0 volts, 57 degree)
----------------------------------------------------------------------------------
                      INPUT SETUP AND HOLD TIMES (ns)
Input                   Setup Time          Hold Time
                      Ph1(f)   Ph2(f)     Ph1(f)   Ph2(f)
address[0]              7.7      9.8        -2.0     -4.5      PATH
address[1]              6.9      7.5        -2.1     -3.2      PATH
address[2]              8.3     11.1        -2.1     -3.0      PATH
address[3]              7.6      9.1        -2.1     -2.8      PATH
address[4]              5.8      8.9        -1.4     -3.0      PATH
address[5]             12.3     11.6        -5.7     -2.3      PATH
address[6]             11.1     10.5        -5.1     -1.7      PATH
address[7]             10.4      9.8        -4.5     -3.2      PATH
begin_frame_in          ---      2.1         ---     -0.5      PATH
begin_row_in            ---      2.1         ---     -0.6      PATH
data[0]                 4.5      ---        -3.0      ---      PATH
data[10]                4.1      ---        -2.5      ---      PATH
data[11]                4.4      ---        -2.9      ---      PATH
data[12]                4.2      ---        -2.7      ---      PATH
data[13]                4.1      ---        -2.6      ---      PATH
data[14]                4.0      ---        -2.5      ---      PATH
data[15]                4.2      ---        -2.6      ---      PATH
data[1]                 4.6      ---        -3.0      ---      PATH
data[2]                 4.6      ---        -3.1      ---      PATH
data[3]                 4.5      ---        -3.0      ---      PATH
data[4]                 4.5      ---        -3.0      ---      PATH
data[5]                 4.7      ---        -3.1      ---      PATH
data[6]                 4.8      ---        -3.3      ---      PATH
data[7]                 4.6      ---        -3.1      ---      PATH
data[8]                 4.8      ---        -3.2      ---      PATH
data[9]                 4.6      ---        -3.1      ---      PATH
end_frame_in            ---      2.1         ---     -0.5      PATH
end_row_in              ---      2.1         ---     -0.5      PATH
filter_id[0]           11.8     11.1        -5.1     -1.7      PATH
filter_id[1]           10.9     10.3        -4.9     -1.5      PATH
filter_id[2]           10.1      9.5        -4.3     -2.9      PATH
hrd_dev_id[0]          11.0     10.4        -4.7     -1.3      PATH
hrd_dev_id[1]          10.8     10.2        -4.6     -1.2      PATH
hrd_dev_id[2]          11.3     10.6        -5.6     -2.3      PATH
hrd_dev_id[3]          11.6     11.0        -5.2     -1.8      PATH
mml_control             ---      ---         ---      ---      PATH
n_reset                 3.9      5.0        -1.7     -0.7      PATH
ods_ids[0]             11.1     10.4        -4.9     -1.4      PATH
ods_ids[1]             10.8     10.2        -4.8     -1.4      PATH
ods_ids[2]             11.4     10.7        -5.8     -2.5      PATH
ods_ids[3]             11.1     10.5        -4.8     -1.4      PATH
oe_n_ie                 8.8      9.5        -3.2     -3.9      PATH
p_data_in[0]            ---      2.3         ---     -0.7      PATH
p_data_in[10]           ---      2.5         ---     -0.9      PATH
p_data_in[11]           ---      2.3         ---     -0.7      PATH
p_data_in[12]           ---      2.3         ---     -0.7      PATH
p_data_in[13]           ---      2.5         ---     -1.0      PATH
```

p_data_in[14]	---	2.6	---	-1.0	PATH
p_data_in[15]	---	2.6	---	-1.0	PATH
p_data_in[16]	---	2.4	---	-0.9	PATH
p_data_in[1]	---	2.3	---	-0.8	PATH
p_data_in[2]	---	2.4	---	-0.8	PATH
p_data_in[3]	---	2.3	---	-0.8	PATH
p_data_in[4]	---	2.3	---	-0.8	PATH
p_data_in[5]	---	2.4	---	-0.8	PATH
p_data_in[6]	---	2.2	---	-0.6	PATH
p_data_in[7]	---	2.2	---	-0.6	PATH
p_data_in[8]	---	2.5	---	-0.9	PATH
p_data_in[9]	---	2.3	---	-0.7	PATH
pixel_clock_in	---	2.6	---	-1.1	PATH
state_0[0]	---	2.4	---	-0.8	PATH
state_0[10]	---	2.8	---	-1.2	PATH
state_0[11]	---	2.7	---	-1.2	PATH
state_0[12]	---	2.7	---	-1.2	PATH
state_0[13]	---	2.8	---	-1.2	PATH
state_0[14]	---	2.8	---	-1.2	PATH
state_0[15]	---	2.9	---	-1.3	PATH
state_0[1]	---	2.4	---	-0.9	PATH
state_0[2]	---	2.5	---	-0.9	PATH
state_0[3]	---	2.5	---	-1.0	PATH
state_0[4]	---	2.6	---	-1.0	PATH
state_0[5]	---	2.6	---	-1.1	PATH
state_0[6]	---	2.6	---	-1.0	PATH
state_0[7]	---	2.6	---	-1.1	PATH
state_0[8]	---	2.6	---	-1.1	PATH
state_0[9]	---	2.7	---	-1.1	PATH
state_1[0]	---	2.2	---	-0.7	PATH
state_1[10]	---	2.3	---	-0.8	PATH
state_1[11]	---	2.3	---	-0.8	PATH
state_1[12]	---	2.5	---	-0.9	PATH
state_1[13]	---	2.5	---	-1.0	PATH
state_1[14]	---	2.6	---	-1.0	PATH
state_1[15]	---	2.6	---	-1.0	PATH
state_1[1]	---	2.2	---	-0.7	PATH
state_1[2]	---	2.4	---	-0.8	PATH
state_1[3]	---	2.2	---	-0.7	PATH
state_1[4]	---	2.4	---	-0.8	PATH
state_1[5]	---	2.3	---	-0.8	PATH
state_1[6]	---	2.4	---	-0.9	PATH
state_1[7]	---	2.4	---	-0.9	PATH
state_1[8]	---	2.5	---	-0.9	PATH
state_1[9]	---	2.3	---	-0.8	PATH

```
********************************************************************************
        GENESIL Version v8.1DV_Jul_2_Quark -- Wed Jul 17 10:35:17 1991
Chip: /tmp_mnt/nfs/u90/gendv20/wallace/tfil                    Timing Analyzer
********************************************************************************
VIOLATION MODE
--------------------------------------------------------------------------------
Fabline: HP2_CN10B                      Corner: TYPICAL
  Junction Temperature:57 deg C         Voltage:5.00v
  External Clock: x4_clock
 Included setup files:
  #0  room_cond              (5.0 volts, 57 degree)
--------------------------------------------------------------------------------
                                NO VIOLATIONS
  Hold time check margin: 1.5ns
```

Appendix A: DV Checklist

DV CHECKLIST

1. DV CONTROL NUMBER : _____

2. CUSTOMER INFORMATION

Customer Name : Georgia Tech / CERL Chip Name : GT–VTF

Address : 400 Tenth Street FAX : (404) 894–3120

CRB Room 377

Atlanta, GA 30332–0540

Project Manager : Dr. C. O. Alford Phone : (404) 894–2505

Design Engineer : Tsai Chi Huang Phone : (404)894–3484

Andrew Register Phone : (404) 894–2527

Test Engineer : Joseph I. Chamdani Phone : (404) 894–2527

3. SERVICES INFORMATION

xx Design Verification Service only. PO #_____

_____ Prototype Service and Design Verification. PO #_____

_____ 1.8% Maintenance

_____ SCS Test _____ Foundry Test _____ Customer Test

When DV is complete, send verified physical database tape to

Customer Y N Silicon Vendor Y N

4. DV CONTACT : Wallace Wai Phone : (408) 371–2900

5. REGRESSION

5.1. GENESIL Version : 8.0.3

5.2. Name of Session Log from recompile : rebuild.LOG (rebuild.001)

5.3. Include DV regression.CMD : DV_regression.001 (simulation and timing)

5.4. Size of database (MB): 154 Guess ___ Density : 6250 ___ 1600 ___ TK50 ___
Tar xx wbak ___ Apollo Cartridge ___
(compressed) Sun Cartridge xx

6. FUNCTIONAL INFORMATION (check when included)

6.1. Number of Transistors : xx

6.2. Key Parameters : xx Testing ___

6.3. DV pin description : xx Testing ___

6.4. Block Diagram : ___ Testing ___

6.5. Functional Description : xx Testing ___

6.6. Timing Diagrams at Pins : ___ Testing ___

6.7. Annotated Views : xx Testing ___ Annotated Schematics : xx Testing ___

6.8. Chip Text Specification on tape : xx Density: 6250___ 1600___ TK50___
(GT_VTF_spec.012) Apollo Cartridge___
Sun Cartridge xx

7. PHYSICAL INFORMATION

7.1. Fabline Name : HP2_CN10B
Customer–Specific : Y N Fabline GENECAL Directory on tape : Y N
Fabline GENESIL Directory on tape : Y N
Fabline Calibration Status : Production : xx Beta : ___ Alpha : ___
NOTE: If not a production fabline, then approval from SCS is required.

7.2. Plots: (check when included or indicate filename)
Chip Route (D size) : xx Bonding Diagram (B size) : xx
Route Filename : route_d.031 Bonding Filename : bond_b.031

7.3. Die Size : Reported Die Size : 415.7 x 420.9 square–mils
Maximum Acceptable Die Size (+/– 2%) : 435 x 435 square–mils
Minimum Acceptable Die Size (+/– 2%) : 272 x 272 square–mils

7.4. GENESIL Package Name : CPGA180f Spec included? Y N
Cavity/Well Size : 472 mils by 472 mils
Non–GENESIL Supplied Package? Y N Text Spec included on tape? Y N
Vendor Name/Part # : KYOCERA KD–84143A Foundry Approval? Y N

7.5. External Block: none

7.6. LRAM: Y N LROM: Y N LPLA: Y N LogicCompiler Blocks: Y N

7.7. Test Pad (PM Pad) is included? Y N (Required for PS)

7.8. Power Pad : VCC: Core 1 Ring 12 VSS: Core 2 Ring 12

NP protection for nwell pad? Y N

TTL output pads or N Protection for inputs? Y N
If yes, have you received silicon vendor approval? Y N

Error in PADRING.033 (PADRING.DRC)? Y N Hardcopy attached? Y N

ESD requirements _____ Approved by SCS? Y N

8. ELECTRICAL INFORMATION

8.1. Chip Frequency Specified in netlist : 6.67 MHz Target frequency : 6.67 MHz
8.2. Power Dissipation: GENESIL = 0.92 W at 10 MHz Spec = _____ W at ____ MHz
8.3. Operating Voltage: from 4.5 Volts to 5.5 Volts

9. SIMULATION

9.1. Number of Clocking Regimes : 1

	Clock Pad Name	DIV/NO DIV	Ext Clock Name	Int PHASE A/PHASE B Name
1.	x4_clock_pad	NO_DIV	x4_clock	PHASE_A / PHASE_B
2.				
3.				
4.				
5.				

9.2. Simulation Setup Files:
Name : none / default Listings attached : _____
Description : _____
Affected Tests : _____

Name : _____ Listings attached : _____
Description : _____
Affected Tests : _____

Name : _____ Listings attached : _____
Description : _____
Affected Tests : _____

Name : _____ Listings attached : _____
Description : _____
Affected Tests : _____

9.3. Test Vector Set:
Total No. of Vectors : 44,010

NOTE : Test vectors written one phase per vector have a maximum test frequency on the IMS Tester of 10 MHz. Test vectors written one cycle per vector have a maximum test frequency on the IMS Tester of 20 MHz.

1. Name : shift_stg0x_tr.083 No of vectors : 4,496
   Description : Tests barrel shfiters's lower 16 bits at stage0.

   Portions of Chip Tested : Module stage0/tfil_10, stage0/tfil_11

   Pass with GFL model? yes
   Pass with GSL model? yes Use for PS testing? Y N
   Pass Fight Test? yes

2. Name : shift_stg1x_tr.083 No of vectors : 4,496
   Description : Tests barrel shifter's lower 16 bits at stage1.

   Portions of Chip Tested : Module stage1/tfil_10, stage1/tfil_11

   Pass with GFL model? yes
   Pass with GSL model? yes Use for PS testing? Y N
   Pass Fight Test? yes

3. Name : mul_test_tr.083 No of vectors : 4,568
   Description : Tests multipliers and adders.

   Portions of Chip Tested : Module stage0/tfil_8, stage0/tfil_9, stage1/tfil_8, stage1/tfil_9

   Pass with GFL model? yes
   Pass with GSL model? yes Use for PS testing? Y N
   Pass Fight Test? yes

4. Name : shift_upper1x_tr.083 No of vectors : 3,888
   Description : Tests barrel shifters and overflow detections for both stages.

   Portions of Chip Tested : Module stage0/tfil_10, stage0/tfil_11, staage1/tfil_10, stage0/tfil_11

   Pass with GFL model? yes
   Pass with GSL model? yes Use for PS testing? Y N
   Pass Fight Test? yes

5. Name : coeff_tr.083 No of vectors : 1,168
Description : Tests coefficient registers.

Portions of Chip Tested : Module tfil_4, stage0/tfil_6, stage0/tfil_7, stage1/tfil_6, stage1/tfil_7

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test? yes

6. Name : dead_pixel_tr.083 No of vectors : 1,032
Description : Dead pixels input test at the normal filtering mode.

Portions of Chip Tested : All

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test? yes

7. Name : coeff2a_tr.083 No of vectors : 400
Description : Tests coefficient registers in the test mode.

Portions of Chip Tested : Module tfil_4, stage0/tfil_6, stage0/tfil_7, stage1/tfil_6, stage1/tfil_7

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test? yes

8. Name : id_comp_tr.083 No of vectors : 368

Description : Tests device select and filter id select operations.

Portions of Chip Tested : All with emphasis in module tfil_4/para_4

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test? yes

9. Name : cs4_tr.083 No of vectors : 624
Description : Tests different external memory configurations.

Portions of Chip Tested : All with emphasis in module tfil_2

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test? yes

10. Name : atg_gen_tr.083 No of vectors : 470
Description : ATG generated test vectors.

Portions of Chip Tested : All

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test? yes

11. Name : function_tr.083 No of vectors : 12,912
Description : Functionality test of different coefficient sets and frames.

Portions of Chip Tested : All

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test? yes

12. Name : function3_tr.083 No of vectors : 9,591
Description : Functionality test of one low pass filter coefficient set and several frames.

Portions of Chip Tested : All

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test? yes

9.4. IMS Grouping within limitation? Y N (Required for PS only)
9.5. Tester clock frequency = 6.67 MHz
9.6. Signals that must be glitch free: Y N

	Signal Name	Ran GSL with glitch detection feature on?
1.	begin_frame_out	Y N
2.	begin_row_out	Y N
3.	end_frame_out	Y N
4.	end_row_out	Y N
5.	device_ready	Y N
6.	n_write_en[1:0]	Y N
7.		Y N
8.		Y N
9.		Y N

10. TIMING ANALYSIS

10.1. System Environment

Temperature Coefficient: 35 Degrees C / Watt (theta JA)
Operating Temp : from 0 ^{0} C (min) to 70 ^{0} C (max)
Operating Voltage : from 4.5 V (min) to 5.5 V (max)
room junction temp = 25 + (theta JA * Power) = 59 degrees C
maximum junction temp = maximum ambient temp + (theta JA * Power) = 104 degrees C

10.2. Reports (Include the following reports)

(required for PS)* guaranteed corner 5.0V room junc temp		(required for PS)* guaranteed corner min operating V max junction temp		typical corner min operating V max junction temp	
Cycle	: xx	Cycle	: xx	Cycle	: xx
Setup/Hold	: xx	Setup/Hold	: xx	Setup/Hold	: xx
Output Delay	: xx	Output Delay	: xx	Output Delay	: xx
Violation	: xx	Violation	: xx	Violation	: xx

10.3. Timing Setup Files:

Name : hot_cond.040 Listings attached : yes
Temperature : 102 degrees C Voltage : 4.50 V
Description : worst case condition, maximum junction temperature, minimum operating voltage

Name : room_cond.040 Listings attached : yes
Temperature : 57 degrees C Voltage : 5.00 V
Description : nominal condition, room junction temperature, 5.0 V operating voltage

10.4. Critical Boundary Conditions:

List critical paths here or annotate the timing report.
Attach additional pages if needed.

Clock Name : x4 clock pad

	report	limit (+/–5%)	report	limit (+/–5%)
1. Phase 1 High	28.5 ns	75 ns		
2. Phase 2 High	24.2 ns	75 ns		
3. Symmetric Cycle	147.6 ns	150 ns		
4. Minimum Cycle	147.6 ns	150 ns		

Outputs

Signal Name	load (pF)	delay	limit
1. begin_frame_out	50.00	22.8 ns	25 ns
2. begin_row_out	50.00	22.6 ns	25 ns
3. end_frame_out	50.00	22.7 ns	25 ns
4. end_row_out	50.00	22.9 ns	25 ns
5. device_ready	50.00	26.4 ns	30 ns
6. state_0[15:0]	50.00	68.0 ns	68 ns
7. state_1[15:0]	50.00	66.6 ns	68 ns
8. col_address[9:0]	50.00	28.0 ns	28 ns
9. row_address[9:0]	50.00	27.5 ns	28 ns
10. n_write_en[1:0]	50.00	16.7 ns	17 ns
11. mm0_csel[1:0]	50.00	38.1 ns	40 ns
12. mm1_csel[3:0]	50.00	39.1 ns	40 ns

Inputs

Signal Name	setup report / limit	hold report / limit
1.	/	/
2.	/	/
3.	/	/
4.	/	/
5.	/	/
6.	/	/
7.	/	/
8.	/	/
9.	/	/

10.5. Hold Time Violations : none (At 2.0 nsec.)

11. DC CHARACTERISTICS

PARA–METERS	DESCRIPTION	CONDITIONS 0 to 70	CONDITIONS –55 to +125	MIN	MAX
DATA PAD INPUT ONLY					
VIH	Input High Voltage			2.0V	
VIL	Input Low Voltage				0.8V
IIL	Input Leakage	VSS<Vin<VDD	VSS<Vin<VDD	–10uA	10uA
CIN	Input Capacitance				6.0pf
DATA PAD OUTPUT ONLY					
VOH	Output High Voltage	VDD= 4.5V IOH=–2.2	VDD= 4.5V IOH=–2mA	2.4V	
VOL	Output Low Voltage	VDD= 4.5V IOL= 6mA	VDD= 4.5V IOL= 5mA		0.4V
IOZ	Output Leakage current(high Z)	VSS<Vout<VDD	VSS<Vout<VDD	–10uA	10uA
COUT	Output Capacitance				7.0pf
DATA PAD INPUT/OUTPUT					
VOH	Output High Voltage	VDD= 4.5V IOH=–2.2	VDD= 4.5V IOH=–2mA	2.4V	
VOL	Output Low Voltage	VDD= 4.5V IOL= 6mA	VDD= 4.5V IOL= 5mA		0.4V
VIH	Input High Voltage			2.0V	
VIL	Input Low Voltage				0.8V
IOZ	Output leakage current (high Z)	VSS<Vout<VDD	VSS<Vout<VDD	–10uA	10uA
CIO	Input/Output Capacitance				7.0pf
CLOCK PAD					
VIH	Input High Voltage			3.9V	
VIL	Input Low Voltage				0.6V
IIL	Input Leakage	VSS<Vin<VDD	VSS<Vin<VDD	–10uA	10uA
CIN	Input Capacitance				15pf

NOTE: All parameters at a supply voltage of VDD = 5V (+/– 10%).

12. CUSTOMER COMMENTS

Pre–Verification Comments

Test vector file atg_gen_tr.083 needs to have clock signal untoggled when run in GFL simulation.

13. CUSTOMER APPROVAL

The undersigned understands that if any design changes are initiated by the Customer subsequent to this sign–off, the Customer is liable for any charges imposed by Silicon Compiler Systems as agreed to in either the Design Verification Terms & Conditions or the Prototype Services Terms & Conditions. In addition, such changes require the DV process to be started from the beginning, which results in extended DV schedules.

Customer Approval : _____ Date 5 / 30 / 91

Title : Research Assistance

14. SCS APPROVAL

Pre–Verification Comments

SCS Approval : _____ Date ___/___/___

Regional Field Application Consultant

SCS Approval : _____ Date ___/___/___

Technical Support Team Leader