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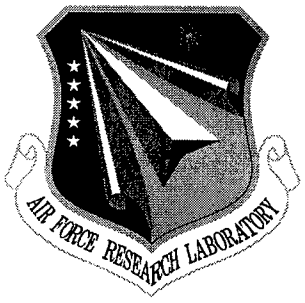

ADVANCED CAD SYSTEM FOR ELECTROMAGNETIC MEMS INTERACTIVE ANALYSIS (ACADEMIA)

Stanford University

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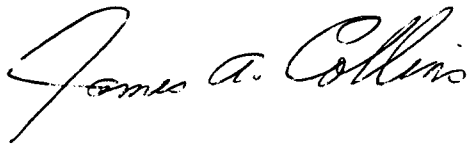
FOR THE DIRECTOR: 

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ADVANCED CAD SYSTEM FOR ELECTROMAGNETIC MEMS INTERACTIVE ANALYSIS

Robert W. Dutton

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13. ABSTRACT *(Maximum 200 words)*

Simulation and modeling of MEMS devices poses a three-fold challenge: a) difficulties in specifying accurate physical models that include process and material dependencies, b) lack of fundamental materials parameters that impact behavior and c) adequate characterization of how the modeling relates final behavior of the devices. A multi-disciplinary team has addressed each of these areas, resulting in significant contributions in all of them. Based on detailed characterizations of a MEMS RF switch, used as a canonical benchmarking structure, accuracy (as well as limitations) of current CAD for MEMS has been quantified. A powerful set of algorithms have been developed for specifying MEMS structures, including extensible capabilities for simulation of processing conditions-especially changes resulting from etching and deposition. A new technique for tensile strength measurements of micro-beams has been developed and provides details of grain-scale effects that contribute to failure. FEM-compatible failure models have been developed using extensive data from aluminum beams. Finally, several new MEMS materials that are compatible with conventional CMOS (backend) processing have been explored. The use of sputtered silicon was tested in the context of circuits fabricated with MEMS structures. Other promising materials that have been investigated for MEMS applications include: iridium, titanium-nitrate, titanium-tungsten, as well as aluminum.

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Table of Contents

List of Figures

List of Tables

1. Executive Summary

Simulation and modeling of MEMS devices poses a three-fold challenge: a) difficulties in specifying accurate physical models that include process- and material-dependencies, b) lack of fundamental materials parameters that impact behavior and c) adequate characterization of how the modeling relates final behavior of the devices. In this project a multi-disciplinary team has addressed each of these areas, resulting in significant contributions in all of them. Based on detailed characterization of a MEMS RF switch, used as a canonical benchmarking structure, accuracy (as well as limitations) of current CAD for MEMS has been quantified. A powerful set of algorithms have been developed for specifying MEMS structures, including extensible capabilities for simulation of processing conditions—especially changes resulting from etching and deposition. A new technique for tensile strength measurements of micro-beams has been developed and provides details of grain-scale effects that contribute to failure. FEM-compatible failure models have been developed using extensive data from aluminum beams. Finally, several new MEMS materials that are compatible with conventional CMOS (backend) processing have been explored. The use of sputtered silicon was tested in the context of circuits fabricated with MEMS structures. Other promising materials that have been investigated for MEMS applications include: iridium, titanium-nitride, titanium-tungsten as well as aluminum.

This report is organized as follows. Section 2 gives an overview of the objectives of the project as well as highlight accomplishments in each of these areas. Sections 3 and 4 provide greater discussion of results in the software development and materials characterization aspects of the work. The majority of the results from this research have appeared in conference and journal papers as well as three PhD theses. Appendix I gives a listing of the publications resulting from this work and Appendix II includes reprinted versions of key papers that support the discussion in the text (as well as those that might be more difficult to find in print or which are not available on the web).

2. Objectives, Approach and Significant Results

2.1 Software Development

A key objective is to develop and demonstrate fully-integrated, FEM-based prototype solver capabilities to model behavior and fabrication process-dependency of MEMS devices. This includes capabilities to consider multi-physics and materials dependencies as well as other process induced factors—for example, geometry effects due to deposition/etching. The overall tool integration strategy was targeted to develop and test key components that overcome limits currently seen to be "bottlenecks" in CAD systems. Application-specific lumped modeling was pursued early on in the project and used to guide the overall direction of the CAD efforts, including improved parameter extraction schemes that cross-link device performance with physical factors such as layout and process dependencies. The approach used here addresses the following information flow and simulation capabilities:

1. Layered access in MEMS specification across levels--layout, process specification, geometry definition, grid and constitutive models
2. Enhanced element technology for discretization of multi-physics systems of equations
3. Unified approach to interface geometry and gridding through use of servers.
4. Demonstration of integrated MEMS simulation capability with internet access to modeling and open interface standards including parameter extraction
5. Prototyping of benchmark canonical RF test structures--both computationally and experimentally--that demonstrate capabilities of models and tools.

The PhD thesis of Edward Chan [1], completed during the course of this project, describes: the validation of a canonical benchmark device (RF switch), characterization of the contact electro-mechanical phenomena, and the design of an electrostatic actuator with an extended range of travel. Included in the thesis are analyses (through simulations) of the effects of: changes in substrate curvature, the influences of stress gradients on fixed-fixed beams, and the importance of considering film coverage in understanding the behavior of composite materials. Rigid-body simulations of the electrostatic actuator with series feedback capacitor, used for extended travel, reveal that tilting always occurs at a spacing of ~60% of the initial gap. This tilting occurs due to asymmetry, but it is unclear why the range does not depend on degree of asymmetry or the size of the series capacitance. One difficulty related to tilting in the electrostatic actuator with extended range of travel is the fact that increasing the feedback or reducing asymmetry cannot mitigate the effect.

Two aspects of the software and design capabilities developed during this research deserve special note and discussion--web-based design of MEMS and accurate modeling of geometry and process-flow information. In the area of web-based design, demonstrations of the final prototype are available through the Stanford TCAD web site [2]. Subsequent to the ending of this contract there has been substantial interest expressed by researchers at the Beckmann Institute at the University of Illinois (Professors Narayan Aluru and Umberto Ravaioli) in continuing efforts in this direction with computational support also coming through NCSA (National Computational Science Alliance) co-located at Illinois. The web-based prototyping environment now includes a more robust interface, remote process tracking to show the status of

submitted jobs, and improvements in the ability to track down errors via the use of error logs. Also demonstrated was an alternative way to view solid models using a Java applet (JGV) developed at the Geometry Center in the University of Minnesota [3]. This complements the use of VRML plug-ins, and provides true platform independence since it requires only a current version of Internet Explorer or Netscape Navigator and no additional plug-ins.

In the areas of geometry modeling and mesh generation, there has been a consolidation of both aspects into an extensible, modeler independent, framework that has been named "Geodesic" [4]. Geodesic is being released in source code form to the MEMS community through the Stanford TCAD web site [2]. The framework is built using the Tcl/Tk language interface to the Visualization Toolkit (VTK) and provides a generic scripting interface layer to the Shapes and Parasolid solid modeler libraries. This interface layer has been designed to provide capabilities independent of the solid modeler kernel being used. It also facilitates extension to other solid modeling kernels (e.g. ACIS). Geodesic can be used as a "black box" geometric-based process simulator for MEMS structures, taking a mask set in CIF format and a process specification in the Composite CAD Process Definition (CCPDS) format and generating solid models which can then be meshed using commercially available tools (e.g. MEGA from SCOREC).

In addition to the geometry-only algorithms suggested by the CCPDS format, Geodesic also provides the ability to incorporate physically-based process simulation using either external simulation programs or through an integrated 2D/3D level set kernel for boundary motion. The significant features of the level set kernel include: a) a modular level set software structure, developed to support interchangeable grid schemes and boundary movement functions; b) general 3D selective etch modeling capabilities; c) a compressed data structure, developed to reduce memory requirements; d) demonstration of techniques for distributing computation on compressed data structure in a heterogeneous computing environment.

2.2 Characterization of MEMS Material Models

The objective of this task is to develop extraction schemes for materials properties using simplified MEMS test structures. In combination with the CAD tools efforts, the physical models (including microstructure) have been evaluated and modified as needed. The scope of material characterization efforts include both standard metal layers (possibly graded as well) and reliability issues such as plastic yield and fatigue. The extraction and validation steps for physical models is a key link with the other two tasks. The approach used in this work builds on the following themes:

1. Mechanical characterization of MEMS materials with dependencies on processing and microstructure.
2. Reliability studies including both fracture and fatigue.
3. Feedback to the constitutive models in the FEM-based modeling task.

This task had two component activities--fatigue modeling (including measurement) and efforts to develop an in situ stress monitoring structure. The fatigue modeling efforts were highly productive in terms of new techniques and quantitative information about this serious reliability

concern for MEMS. The following gives a summary of highlight results, particularly coming from the PhD thesis work of Guido Cornella. The proof-of-concept for in situ stress monitoring was only partially successful; a variety of limitations in process control during fabrication resulted in this aspect of the project being terminated. A summary of limited results for in-situ stress monitoring are given in Section II. The PhD student, Ms Ping Zhang, shifted her thesis topic to further studies in the area of fatigue measurements and modeling. This area is of great ongoing importance to the MEMS field, especially of value to DoD. Currently there is no follow-on support for these studies.

In the PhD thesis by Guido Cornella [5], a new measurement method and design of test structures for fatigue modeling of micron-scale MEMS beams has been developed. Cyclic and static relaxation tests at various strains have been performed for Al micro-beams of different thickness. The results of this study have allowed the construction of stress-strain curves for both cyclic relaxation and static relaxation. These new curves help to infer how the material behaves due to cyclic loading, vis a vis a single application of stress. In addition a post-test sample extraction procedure has been developed which allows the removal of tested, but not fractured microbeams without application of additional loads, allowing one to "freeze" the dislocation arrangement which has evolved throughout testing. Moreover, TEM sample preparation techniques have been developed that allow one to investigate (and illustrate) dislocation states within the tested samples. TEM analysis of cyclically loaded samples reveals the evolution of the dislocation arrangement with the number of loading cycles. At first dislocations interact and entangle; later they form dislocation networks within a grain. Upon further cycling this dislocation network expands and eventually reaches across multiple grains.

Tensile tests on aluminum micro-beams of four different thickness values were performed at strain rates between 7.6x10^-2/s and 7.6x10^-6/s. Strain rate sensitivity has been observed for all film thickness values. Results for small strain rates in the nominally linear-elastic regime (at small strains) deviate considerably from linear elastic behavior. The observed characteristics are well described by anelastic material behavior. Anelastic reloading after stress relaxation experiments supports the anelasticity hypothesis. A two-mechanism model with a fast and a slow relaxation time -corresponding to recoverable grain boundary sliding and dislocation motion - has been developed to explain the observed relaxation behavior in Al thin film samples during monotonic and cyclic loading. The 1D implementation and testing of the model has been performed using ABAQUS; the basic model formulation is also suitable for 2-3D applications.

Iridium thin film samples have been tested under monotonic and cyclic testing conditions. Linear-elastic behavior has been observed up to fracture. Unloading of iridium samples has shown no hysteresis of loading and unloading curves. Fracture stresses of up to 3.5 GPa and fracture strains of up to 0.75% have been measured. A Young's modulus of 490 GPa as compared to the literature value of 528 GPa (7.2% deviation) has been extracted. Cyclic loading experiments of iridium microbeam samples showed small relaxation of the peak stress at the initial strain (around 10%). This initial relaxation cannot be explained by anelasticity since reloading is not observed at the end of the test. The relaxation is more likely due to plastic

deformation. No relaxation of the peak stress was observed for further cyclic testing on the same sample at increased strains.

In addition, alloyed Al beams with about 2% Ti were studied, deposited as 7-ply of Al(0.5micron):Ti(10nm) multilayers and then annealed at 550C for 1hr. It was found from TEM studies that small particles of Al3Ti form along the grain boundaries of Al after the annealing. In montonic tensile testing, the Ti-alloyed beams showed 200MPa of yield strength, which is at least 80% higher than pure Al beams. They also exhibit about 2.5% elongation--much larger than that of pure Al. This alloy effect is potentially of practical importance because one can fabricate much stronger Al beams without substantially sacrificing the conductivity. Relaxation in the pure Al case is much larger than the case of the alloyed samples probably due to precipitation at the grain boundaries which hinders grain boundary motion. Relaxation found in this case is much larger than those previously reported in the case of bulk or thin films on substrates.

2.3 MEMS Device Modeling and Design

Design and implementation of MEMS structures, including materials parameter extraction, were used to test the CAD and physical models based on MEMS devices of interest to DoD. The experimental measurements made with these structures helped to facilitate the critical evaluation of models, physical parameters and overall simulation accuracy of CAD for MEMS devices. The test vehicles from this component of the research also supported canonical benchmarking of both new materials for MEMS and accuracy of Composite CAD in MEMS applications, specifically the RF switch. The approach used in this work builds on the following themes:

1. Design/implementation of test structures for materials characterization.
2. Concurrent building of prototype MEMS application devices (RF switch).
3. Measurement, parameter extraction, and testing of CAD models.

Prototype development, evaluation and documentation of CMOS-compatible MEMS process integration that is capable of exploiting alternative materials (vis a vis standard poly-silicon used in MUMPS) ended up to be the major outcome of this task. The primary materials of interest centered on standard CMOS-oriented materials (i.e. sputtered silicon) but also included alternative, potential break-through materials such as iridium. DoD system-level applications of RF MEMS and initial evaluation of process integration and test structure work were initiated based on collaborations with AFRL (Hanscomb AFB). However, due to lack of funding specifically in that area and loss of personnel from this task (to local start-ups), the detailed DoD application testing portion of the work ended prematurely.

Several criteria must be met in order to create a functional RF MEMS device. These criteria include controllable stress, high electrical conductivity, and mechanical stability. Integration with circuitry may also be important for some applications. The importance of mechanical stability, particularly in regards to strain gradients was highlighted by this work on test structures.

Low stress films were achieved in a variety of materials using DC magnetron sputtering and ion-gun evaporation. In DC magnetron sputtering, stresses were controlled by adjusting the deposition power and working gas pressure. Using this method it was possible to achieve stresses lower than 100 MPa in sputtered aluminum, silicon, titanium, titanium-nitride, and titanium-tungsten. In ion-gun assisted evaporation, a source of charged particles is directed into the flux of atoms coming from the target. This modifies energy and direction of incoming atoms, changing the atomic peening effect at the substrate. Using this method, it was possible to vary the stresses in iridium and platinum.

Due to relatively low mechanical resonant frequencies (< 1 MHz), most electrostatic MEMS do not require high levels of conductivity. RF MEMS, by contrast, have more stringent requirements in this regard. Sputtered aluminum and nickel-molydenum multilayers are much more conductive than titanium and its alloys or silicon. However, nickel-molybdenum multilayers are more difficult to pattern and etch than these other materials and pure aluminum is typically unsuitable because of issues with its mechanical properties.

Aluminum displayed a tendency to warp when released from its sacrificial layer. It was found that the release parameters played a dominant role in this warping and that there were large variations in the radius of curvature of the final structures, even among adjacent devices. Design and process techniques to reduce the impact of released curvatures on electrostatic parallel plate devices were explored and evaluated. Using these techniques, it was possible to successfully release aluminum-based variable capacitors. However, when operated as a switch, the on-off capacitance ratio of these devices was limited by warping in the structure. Pure aluminum also demonstrated strong anelastic behavior [5] which, even if the devices could be made perfectly flat, would result in inconsistent operating voltages when used in an RF switch. Aluminum alloyed with two percent Titanium showed much better behavior in this regard, as discussed in the Section 2.2.

On-chip integration of circuitry with Micro-Electro-Mechanical Systems (MEMS) components is vital to the performance of many types of microsensors. To date, the most common material for integrated surface micromachining has been LPCVD polysilicon, which is deposited and annealed at temperatures that are incompatible with pre-fabricated standard CMOS circuitry. This has required modifications to the CMOS process or fabricating the structural layers before processing the electrical circuitry, resulting in increased complexity. Sputtered silicon, by contrast, can be deposited directly atop CMOS circuitry at very modest temperatures. Although not as conductive as aluminum, silicon has been proven acceptable for a wide variety of applications.

Sputtered silicon microstructures were made using oxide and polyimide sacrificial layers. Films deposited atop oxide were wet-released in buffered HF. It was discovered that sputtered silicon was permeable to buffered HF at film thickness of up to 5 microns. Using this permeability, buried cavities were made in underlying oxide layers. Films deposited above the polyimide were dry-released in an oxygen plasma. The dry-release eliminated the need for critical point drying

normally required to prevent stiction caused by capillary forces during the wet release process. Released curvatures of sputtered silicon cantilevers were more consistent than in aluminum cantilevers. However, the curvatures were dependent on thickness. A model based on surface stresses as the dominant source of the strain gradient in the films was proposed and predicted a released radius of curvature proportional to thickness squared, matching empirical results.

Several additional properties of sputtered silicon films were investigated, including their in-plane stress (< 100 MPa), density (2.24 +/- 0.09 g/cc), surface roughness (3 nm RMS), and electrical resistivity (> 6 Mohm/square). Improvements in the electrical conductivity of completed structures were realized by cladding the sputtered silicon structural layers in symmetric, 50 nm thick layers of titanium-tungsten.

The dry-release sputtered silicon process was integrated with pre-fabricated CMOS transistors and did not change the maximum saturation current by more than 3%; there was no significant difference apparent in subthreshold operation. As a demonstration, the dry-released TiW-clad sputtered silicon process was used to make an electrostatically deflected plate structure with integrated capacitance measurement circuitry, the output of which was correlated to deflection. This work represents the first application of sputtered silicon to integrated MEMS. While not of sufficient conductivity to be used in RF MEMS applications, sputtered silicon is a potential replacement for LPCVD polysilicon and demonstrates the feasibility of integrating CMOS circuitry with sputtered MEMS devices. Further technical details are available in the PhD thesis of Ken Honer [6] as well as the IMECE '99 conference paper [7]. An invention disclosure on the sputtered silicon process has been filed with the Stanford's Office of Tehnology Licensing.

2.4 Technology Transition of Results

The results of this project have been transitioned to others--academic, government and industry--primarily through published work in conferences, journals and PhD theses. In each of the task areas there have been major advances as reflected in three PhD theses to date [1][5][6] and a fourth expected to be completed in 2001 [8].

The software aspects of this project have resulted in two prototypes that have been demonstrated at DARPA contractor meetings and program manager site visits as Stanford University. There also have been a variety of interactions with CAD vendors involved in the Composite CAD program, many of these have directly supported commercial developments--both in terms of providing prototype modules as well as critical benchmarking information. One example of particular significance in the area of standards for the Composite CAD program has been the independent testing (and implementation) of CCPDS as discussed in Section 2.1. This implementation is also included within the Geodesic software prototype that is available through the Stanford TCAD group's web site [2]. There has been a sustained set of interactions with Microcosm (and also Coyote Systems, now merged with Microcosm), especially in the areas of geometric modeling and internet-based MEMS prototyping.

While the main efforts and emphasis to date in technology transition for the software has focused primarily on the Composite CAD vendors, two recent sets of interactions show excellent

prospect for future impact. In Section 2.2 the interactions with Beckmann Institute at the University of Illinois was mentioned. The combination of researchers at Beckmann with interests in MEMS and the computational resources provided through NCSA, offer a very potent option for the ongoing development of interactive MEMS design using a web-based paradigm demonstrated in this project. Professor Narayan Aluru, also active in other DARPA programs in the MEMS area, has expressed interest and willingness to go forward in this area; our Stanford team has offered to assist him both in obtaining our code and collaborative efforts to move further in this research direction.

The second aspect of ongoing technology transition for software results from this work involved the Focus Research Center (FRC) in the area of interconnects, sponsored through MARCO (including a substantial component of DoD funding) and headed by Professor James Meindl of the Georgia Institute of Technology. Specifically, the capabilities that have been developed under this program in terms of the Geodesic prototype are potentially of major use and benefit in modeling interconnections in VLSI. This includes options for 3D integration of heterogeneous, mixed technology capabilities as part of interconnect fabrics. Specifically, the ability of Geodesic to deal with complex geometries that include process and technology dependencies--the goals related to MEMS--turns out to be nearly ideally suited for the applications in interconnect domain. Hence, with strong support and encouragement from Professor Meindl, the Geodesic prototype will be used and further extended under the ongoing MARCO FRC in interconnects.

There have been several interactions in testing advanced RF MEMS structures that can be applied to DoD-oriented applications and that have been leveraged by test structure work and leading edge processing capabilities for MEMS at Stanford. Test device work was carried out in collaboration with the group headed by Captain Rob Reid (AFRL/Hanscomb). As described in Section 2.3, these efforts have been curtailed in scope pending new funding sources. There have also been extensive discussions between Professor Greg Kovacs and staff at Hughes (HRL) to determine feasibility for developing SOS/CMOS to demonstrate that Stanford photovoltaic actuation technology that could be integrated with MEMS. The devices have already been shown to actuate an HRL RF MEMS switch using Stanford microphotovoltaics. Despite the sporadic nature of both AFRL and HRL interactions there have been very real benefits to both groups leveraged through this research program.

2.5 References

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3. Software Development

Authors: Nathan Wilson, Dr. Daniel Yergeau, Prof. Robert W. Dutton.

3.1 A heterogeneous environment for computational prototyping and simulation based design of MEMS

3.1.1 Introduction

Micro-Electro-Mechanical Systems (MEMS) offer dramatic new functional capabilities. Analysis of MEMS is a challenge; the structures are geometrically complicated, electromechanically coupled, and inherently three-dimensional. The multi-domain physics for MEMS includes: electrical, mechanical, and fluidic interactions. Effects of each domain need to be accurately simulated to correctly predict device performance. In addition, IC-based fabrication techniques require the modeling of complex material behavior and processing such as etching, deposition, and thermal processes such as diffusion (and oxidation). The size and aspect ratios of typical MEMS structures differ significantly from those traditionally found in the VLSI community. This spatial stiffness makes it difficult to construct a geometry model using standard process simulation tools.

Several leading authorities in the field believe that design tools are critical to the future and the growth of the MEMS market. For example, Karen W. Markus, director of the MEMS Technology Applications Center at MCNC has stated [1]:

> *MEMS foundries cannot effectively serve their customers without a set of engineering design tools that enable remote, non-expert, users to interface with those foundries. There are no such packages that free the designer from needing a comprehensive understanding of the fabrication process or the nuances of polygon-level layout design.*

In addition, Eric Peeters from Xerox writes [2]:

> *Several microelectromechanical systems have achieved commercial success. The barriers can still be formidable, though, and the path to success is often much different for MEMS than it was for mainstream semiconductors. Maturing software for comprehensive modeling and design will help in the future.*

Stephen Senturia, a leading expert in the field of MEMS simulation commented on the state-of-the art in [3]:

> *Technologies for fabricating a variety of MEMS devices have developed rapidly, but computational tools that allow engineers to quickly design and optimize these micromachines have not kept pace. Inadequate simulation tools force MEMS designers to resort to physical prototyping.*

In the MEMS field, it is becoming widely accepted that representing the 3-D geometry of devices is critical for simulation based design. Many commercial and academic systems for MEMS analysis rely on purely geometric operations to create the structures. Notable examples include MEMCAD, Intellicad, and Solidis [4-8]. While tools exist for creating geometry for the VLSI community, there are unique challenges posed by MEMS. Modeling challenges include the complexity and aspect ratios of typical structures, residual stresses which create initial curvature in ideally flat devices, and effects of the materials used. The typical dimensions of MEM switches (such as fabricated using the MUMPS process) are on the order of several hundred microns in length, a width on the order of 1/10 the length, and thicknesses of only several microns. These dimensions cause significant problems for deposition and etching process simulators such as SPEEDIE [9]. If full 3-D physical process simulations were performed, it would take excessive amounts of computing resources including time and memory that exceed current limitations of software and hardware. In addition, commonly occurring features such as large flat regions do not gain geometric accuracy from 3-D deposition and etching simulation compared to using 1-D or 2-D simulation.

A second issue concerning micro-system simulation is that available commercial tools are designed for a "traditional" computing environment. A traditional computing environment consists of a single user working at a fixed workstation running software locally with licenses tied directly to the given machine (or local cluster of machines). Commercial micro-system design tools were not designed to minimize platform dependence or take advantage of the latest technology (e.g. the internet). The field of MEMS provides an ideal target for internet-based simulation software for the following four important reasons:

1. *Emerging market.* Unlike the automotive and aerospace industries which have been around and utilizing simulation tools for decades, the MEMS market is relatively new and use of simulation in the design process has not yet become deeply entrenched using existing simulation paradigms.
2. *Cost.* The automotive and aerospace industry are driven by a few large companies that can devote significant manpower and financial resources to computational prototyping. In sharp contrast, MEMS is a field driven by smaller firms and universities with more financial constraints.
3. *Size of models.* A typical model for an aircraft involves millions of unknowns (i.e. degrees of freedom). However, many micromechanical devices of interest can be reasonably simulated with tens-of-thousands of degrees of freedom.
4. *Standardized processes.* Due to inherent difficulties in IC fabrication, several popular commercial processes (e.g. MUMPS) currently exist. Since fabrication runs take several months, significant time is lost between runs if one is iteratively designing a prototype. This provides opportunities for "virtual fabrication runs" which can be done using internet-based simulation tools in between fabrication of devices.

This report documents a MEMS computational prototyping system which was developed from the ground up to take full advantage of state-of-the-art technology in computer hardware, software, and the internet. Key design decisions in the software architecture and engineering

tradeoffs of computational efficiency for automation were made to enable internet-based prototyping. After discussing the needs of the typical microsystem developer, an overview of the system is given. Novel methods are documented which utilize existing tools in a computationally efficient method to achieve accurate and practical geometry.

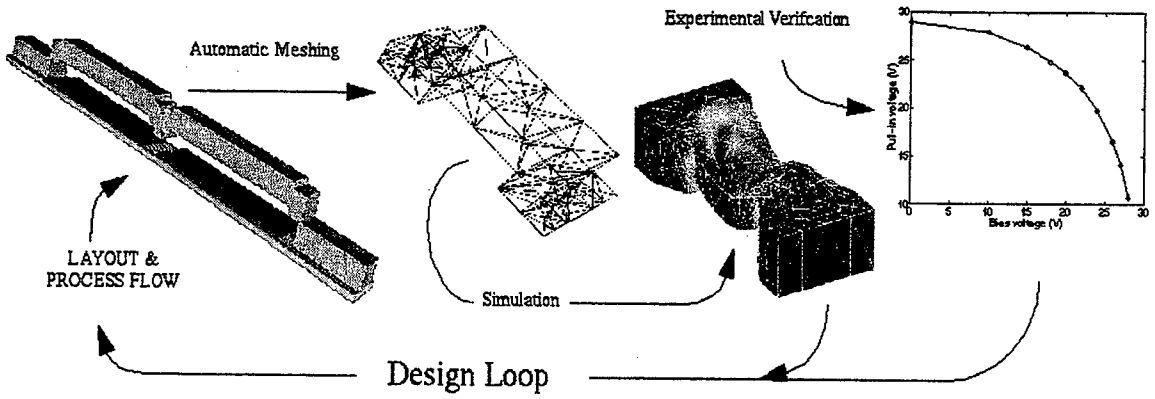


Figure 3-1: Typical design loop for a micro-electro-mechanical switch.

3.1.2 Simulation environment system requirements

The architecture of a software system for microsystem design must take into account the needs and skills of a typical designer. Market research indicates typical MEMS design groups are small, without individuals who are solely dedicated to computer simulation [10]. Here several basic assumptions can be made of the typical designer:

- Mechanical/Electrical engineer with a masters or equivalent work experience
- Minimal background in computer simulation
- Desire to utilize new tools which supply useful and timely feedback on new designs

The potential users are then designers who want to use computer simulation to help guide their development efforts. Under these assumptions, Fig. 3-1 shows a desired iterative design cycle for a RF switch. In general, a simulation based design system for MEMS devices consists of four major components:

1. Geometry Definition
2. Discretization (i.e. mesh generation)
3. Simulation (e.g. coupled electro-mechanical)
4. Visualization (e.g. displacements, charges, stress)

These components need to sufficiently integrated so that information can travel from one module to another without significant user intervention. Two quite different modeling methodologies are being pursued among the MEMS CAD community. The "homogeneous" approach is to develop tightly integrated component simulation tools and design methodology. Alternatively, a "heterogeneous" approach is one that wraps distinctly different end-user software packages to create a "meta" tool. The MEMCAD system is one well known example that uses commercial and other academic tools (ABAQUS, IDEAS, and Fastcap) [4]. The system detailed below relies on using a heterogeneous collection of appropriately chosen external software packages to create a versatile system which provides maximum automation of the model creation and simulation process.

3.1.3 Internet based prototyping of Micro-Electro-Mechanical Systems

This work included a preliminary investigation internet-based simulation of microsystems. It focused on using mainstream, current web-based technology while highlighting possible future directions in relevant internet technology. It proposed a paradigm of automation that limits the information that needs to pass back and forth between a browser-based client and the back-end server. In the present implementation, geometric models are generated from layouts and a process specification, then meshed automatically, and simulated using *hp*-adaptive finite element techniques. The web- and browser-based environment provides file transfer, simulation control, and visualization of simulated results.

3.1.3.1 Client-server overview

The system takes advantage of a client-server paradigm as shown schematically in Fig. 3-2. The yellow boxes (masks/layout, processing flow, boundary conditions, and material properties) indicate the user provided information. The left side of the diagram also indicates the steps that are carried out on the designer's machine (referred to as the "client"). The right side of the figure corresponds to the processes run on the "server." The server can be the same machine as the client, a different machine on the same local network, or a remote machine accessed via the internet, even through a proxy. There are three main steps carried out on the server:

1. *Geometric Modeling*. This step takes the user-defined process flow and masks for the layout and creates a solid model representing the three-dimensional device.
2. *Discretization*. This step automatically breaks the solid model into smaller non-overlapping discrete pieces (called a mesh) needed for simulation.
3. *Simulation*. This step simulates the device using multi-physics Finite Element Analysis techniques to obtain electrical and mechanical characteristics of the structure.

In the overall system, the boxes on the left correspond to computational inexpensive tasks, while the boxes on the right can require significant computational resources. The communication between the left and the right side is transaction oriented (not interactive) and thus can be done efficiently by transmitting small- to medium-sized blocks of data.

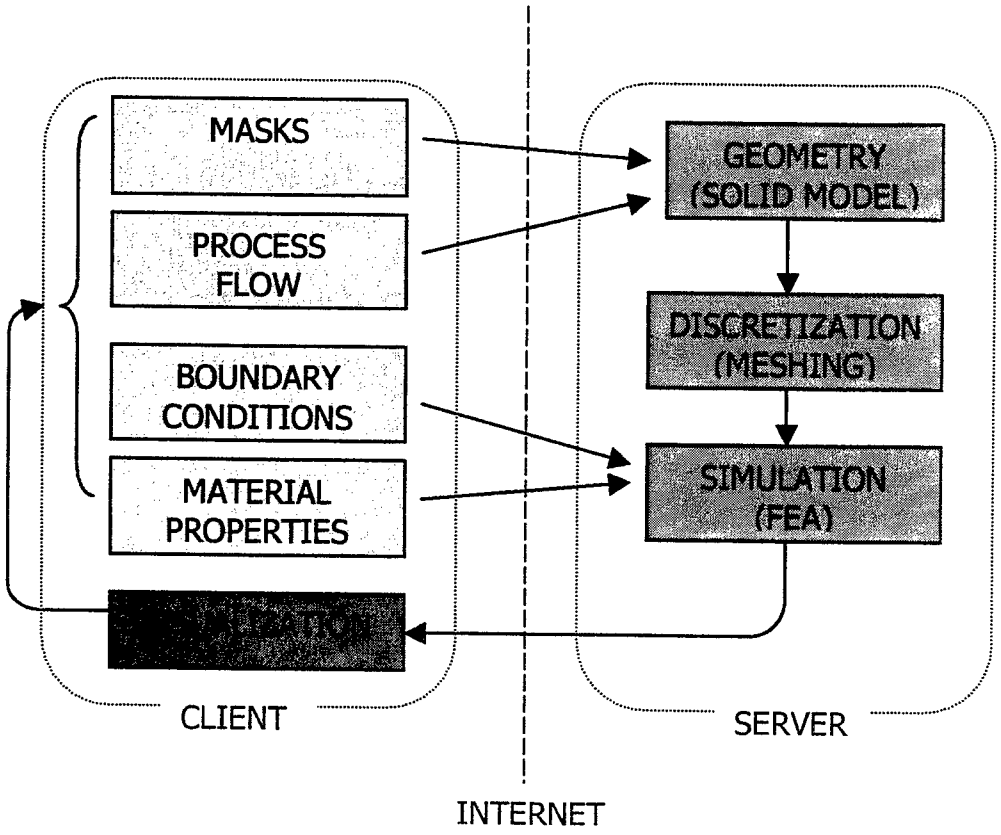


Figure 3-2: Schematic of client-server architecture for internet-based prototyping.

3.1.3.2 Client-server architecture

The client side application is presented through a standard frames-capable web browser as seen in Fig. 3-3. The toolbar on the left allows selection of several submenus, which in turn update the toolbar and/or the main viewing window to guide the user interactively through the process of going from a design to device simulation. Most of the submenus consist of dialogs for information entered directly using standard HTML form objects. The information is transferred using standard HTTP POST/GET methods and server-side CGI scripts. The use of these standard transaction mechanisms permits access to a server across a firewall, provided that an HTTP proxy is available.

As an example transaction, consider the required step of passing the layouts created on the user's local machine to the server for geometric modeling. Typically the masks will be created in a standard layout editor (e.g. L-Edit, Magic, etc.) and exist on the client machine in the form of a text file. The user will then specify the desired filename in a standard HTML form object that uses the HTTP POST method to pass the information to the server. The server receives this information via the HTTP port and runs an appropriate CGI script to create a copy of the file on the server. An identical mechanism can be used to transfer a file containing the fabrication process flow (using the the Composite CAD Process Definition Specification [11]).

The user interface was implemented primarily with standard HTML, instead of Java, for greater portability among browsers and to avoid some of the security restrictions of Java (i.e. Java applets cannot access the local filesystem which would have prohibited uploading of local files containing mask and process flow information). Unfortunately, the transaction-oriented nature of HTTP introduces latencies that are too large for highly interactive use. Tasks such as visualization that require a high level of interactivity or do not map well into a forms-based interface are implemented using Java applets that are downloaded to the browser. Examples of applets utilized in this implementation include an interactive geometry visualization applet (JGV) discussed below and a user friendly applet to create a process flow. The process flow applet uses an HTTP POST method to communicate with the CGI scripts on the server for reasons stated above.

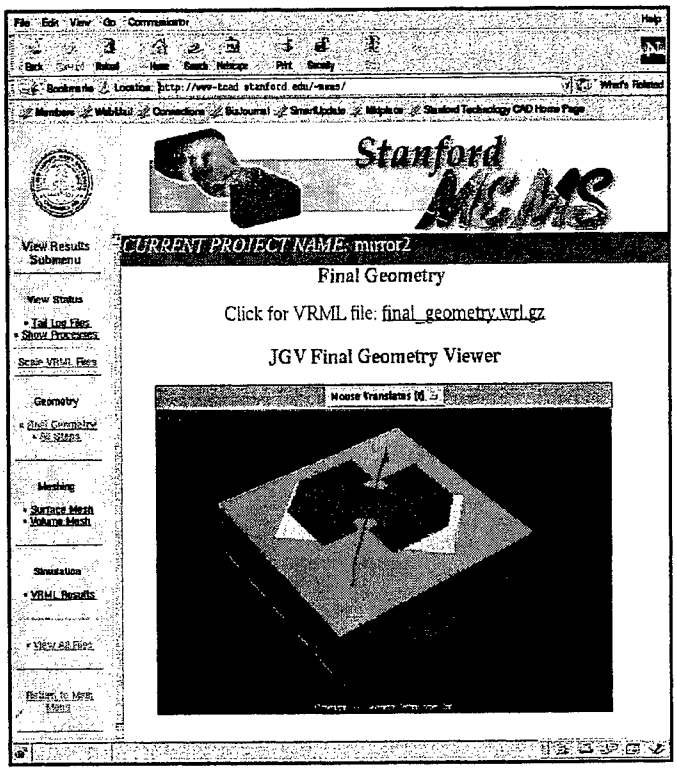


Figure 3-3: User interface (i.e. a web-browser) to web-based MEMS prototyping environment.

Visualization of geometry and simulation results on the local machine is an important step in the design process. Several visualization techniques were tested. First, visualization of the geometry and the surface meshing was achieved using the Virtual Reality Markup Language (VRML) [12]. VRML was one of the first standard file formats proposed for 3-D internet-based visualization. Unfortunately, the standard was never universally adopted and VRML viewers are typically limited to only a subset of the functionality and are not available on all platforms. The VRML standard is no longer being developed, and the Web3D consortium has migrated its

efforts into developing a new extensible 3-D format [13] for internet applications. The second attempt for portable geometry and mesh visualization was to use a visualization package named JGV [14], an applet implemented in pure Java. The viewer was less elaborate than the VRML viewers, but did not require special plugins and is only 100 kilobytes in size, small enough to be transmitted with the geometry over low bandwidth links such as a 56 Kbps modem.

The server side framework is implemented as a collection of PERL and Tcl CGI scripts that manage the transmission and storage of data and control other simulation tools on the server. To organize the information maintained on the server, the idea of a "project" is employed. A project consists of all of the files needed as input (e.g. process flow and masks), the desired output files of the simulation tools (e.g. visualization files), files that maintain the current state of the device (e.g. if mesh generation is completed), and log files (e.g. files detailing the success or failure of a desired operation). Currently this is handled transparently to the user by having the server track the needed files and storing them physically in a single directory for the given project. The client controls the projects via a submenu in the interface that permits the fundamental operations of creating, deleting, renaming, and copying a project. The user is constantly reminded of the current project name since it is clearly displayed in a separate frame of the web-browser (see Fig. 3-3). Since the server tracks the varying states of projects, the user can change between projects or interact with multiple projects via addition windows of the web browser. The main application called by the server scripts, named Geodesic, is detailed in the following section.

3.1.4 Geodesic framework

Geodesic consists of an extensible framework to create MEMS geometry of varying degrees of physical accuracy using multiple geometric simulation techniques. It has an integrated meshing layer that permits automatic tetrahedral mesh generation. In addition, it can create input files automatically for a finite-element code, based on the ProPHLEX finite-element kernel [15], which permits *hp*-adaptive finite element simulation of the coupled electromechanical problem. Fig. 3-4 depicts the architecture of Geodesic. The input to Geodesic consists of a set of masks (defined in a CIF file) and a process flow (specified using the Composite CAD Process Definition Specification [11]). The geometry is then built in a layer by layer fashion by emulating and/or simulating the processing steps used to build the actual device (i.e. "virtual fabrication" or "vfab"). Currently only geometric steps are supported, though these are sufficient for the devices targeted by this contract. When fabrication steps such as implants and diffusions alter the mechanical behavior of the device, they can be approximated by using distinct geometric regions for regions of significantly different doping.

The challenges of integrating diverse tools such as solid modelers and mesh generation software into a unified framework involves tasks of varying computational expense and algorithmic challenge. In addition, in a research setting it is desired to have a tool that permits rapid prototyping and quick testing of new algorithms. For this reason, Geodesic uses Tcl/Tk as a front-end integration environment. Tcl/Tk combines the ease of a powerful scripting language with the ability to imbed C/C++ code for computationally intensive operations. There are four

main modules in Geodesic: the object repository, the solid modeling module, the levelset kernel, and the meshing interface.

3.1.4.1 Object repository

The object repository is a simple hash table of names (character strings) with corresponding object pointers. The repository allows for the basic operations of adding, deleting, listing, and querying of object type. This layer does not know or care about the underlying structure of the objects contained in it, it merely returns the pointers and calls instantiation and deletion methods as required.

3.1.4.2 Solid modeling module

At the heart of geometric modeling is a solid modeler. By wrapping the solid modeling function calls used in generic interface layer, Geodesic can be used with multiple solid modeling kernels. Because these packages inevitably exhibit relative strengths and weaknesses, it is useful to design for a plug-and-play modularity which enables the easy exchange of one implementation for another. This interoperability with multiple kernels is facilitated by designing the system to minimize the number of distinct function calls required to build a geometry. The current implementation can be used with two different commercial solid model kernels (Shapes [16] and Parasolid [17]). So far, only limited results have been achieved using a freely available solid

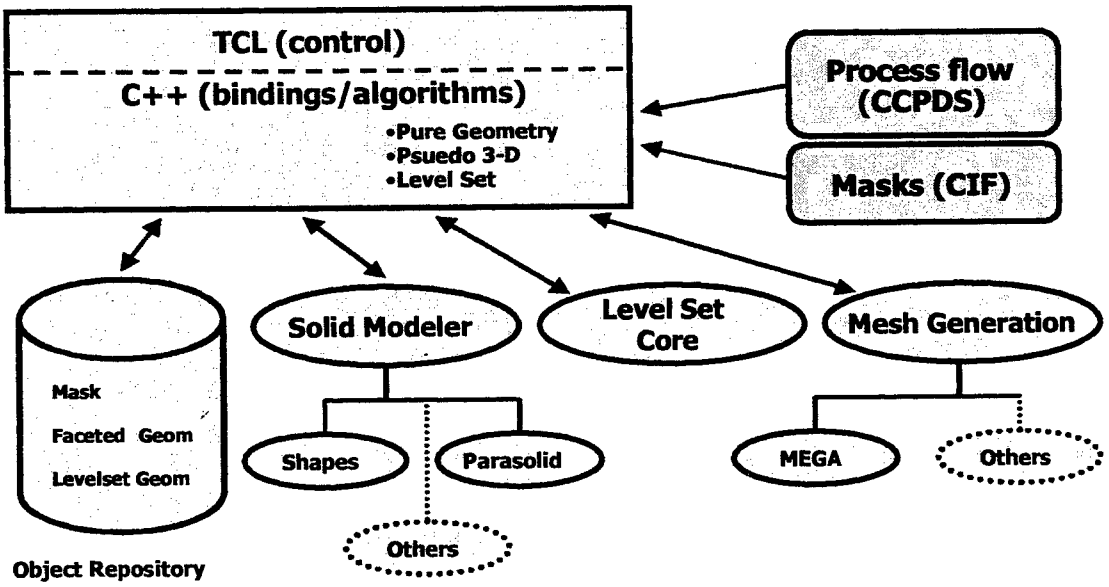


Figure 3-4: Geodesic software architecture.

modeler (IRIT [18]) due to limitations in its internal data representation and capabilities. The extension of Geodesic for use with other solid modelers (e.g. ACIS [19]) should be straight forward.

3.1.4.3 Level set module

Geodesic contains a fully integrated general multi-dimensional level set kernel which can be used for physical process simulation [20]. Briefly, the level set method refers to a mathematical formulation which represents the motion of a propagating curve in the form of a partial differential equation (PDE) which is evolved in time. The equation solves the evolution of a scalar field that implicitly represents the propagating interface. The level set method has many advantages over traditional Lagrangian techniques used to track interfaces (i.e. string methods, marker particle techniques, etc.) in that the method naturally allows for topologic change, and the extension to higher spatial dimensions is straightforward. One of the major difficulties in physical process simulation using the level set method involves defining appropriate physics-capturing velocity functions for different deposition and etching processes. Several cutting-edge techniques are employed in the level set implementation found inside of Geodesic. These include using a compact storage scheme to reduce memory requirements and a technique known in the literature as "narrow-band level set methods" that greatly reduce the computational requirements. The integration of this module with the rest of the Geodesic system enables level set based modeling to be done in conjunction with the other geometric techniques described below.

3.1.4.4 Meshing module

Geodesic also contains a generic meshing layer. In the current implementation, only the MEGA automatic mesh generation package [21] is supported. Its functionality includes "meshing through the thickness," which is useful in the simulation of thin material layers frequently encountered in MEMS. It also possesses special boundary layer meshing capabilities useful in microfluidics. See [22] for details on automatic mesh generation for microsystem simulation.

With the overview of the Geodesic framework complete, more detail is now provided on building geometry appropriate for microsystem simulation. The task of creating the geometry involves the solid modeling module and can involve the level set module as detailed below.

3.2 Creating geometry for the simulation of Micro-Electro-Mechanical Systems

3.2.1 Overview

In the field of microsystems, numerous commercial and academic efforts are underway to develop simulation based design (SBD) systems [4-8]. These systems used assorted methods to generate geometry for MEMS electro-mechanical simulation. All of these systems currently rely purely on geometric operations to create geometry. That is, there is no physical process simulation involved or used in creating the geometry of a micro-mechanical device. These tools commonly refer to their operations as "process emulation," which implies that the user must know certain characteristics of the final geometry. More specifically, the user must at a minimum specify layer thicknesses, etching masks, and a simplified process flow. On the other

hand, process simulation allows the user to specify an input topology and a physics-based model will evolve the geometry based on process specific parameters such as etch rate, selectivity, sticking coefficients, etc. Thus, a user must be able to characterize a processing step and feed the simulator the appropriate parameters, but characteristics of the final geometry are not specified. The interested reader can refer to [23] for a brief history of process simulation and its application.

When one considers utilizing MEMS geometry, there is an important distinction between creating geometry for visualizing the outcome of processing steps and using geometry for simulation. In the case of visualizing the geometry, a design may be curious what his device will actually look like given the masks and processing steps he has specified. Visual inspection may lead to the discovery of design rule violations, obvious design errors such as missing supports, inappropriate layer thicknesses based on prior knowledge of similar devices, etc. In the visualization of the geometry, the retention of small features in a device will have little impact of the ability of the designer to work with it. That is, even the most detailed devices that will be discussed below can comfortably be viewed interactively on a modern PC or workstation. However, in stark contrast, the retention of small features in the geometry which do not impact the global behavior of the device can be extremely computationally costly in simulation. For example, the retention of etch release holes in a device that do not affect the ultimate performance of the device may not be hard to visualize, but may make the mesh generation and the simulation of the device take CPU days instead of CPU hours to perform.

Although the issues are similar in devices for microfluidics and thermally actuated devices, the focus of this work was on generating geometry for the electro-mechanical simulation of microsystems. This is reasonable since there is a large number of devices that perform in this physical domain (e.g. RF switches, comb drives, etc.) and electro-mechanical devices also provide a rich set of devices with varying types of geometry. The goal was to develop a versatile software framework which permits the creation and utilization of varying degrees of topologic complexity and geometric physical accuracy as required for simulation.

3.2.2 Previous and current work in geometric simulation for VLSI & MEMS

Interest in automating 3-D geometry construction, using only mask and process information, for VLSI and MEMS applications has been actively pursued for nearly two decades. One important way to classify these systems is on their implementation. This lumps systems into two basic catagories: those that utilize commercial solid modeling kernels and efforts based on proprietary code to represent solid models. Examples of the latter include OYSTER [24], 3DTOP [25], and MemCel [26]. Efforts using commercial solid modeling kernels include VIP3D [27] and MemBuilder [28] (the current mechanism used to build geometry in the commercial system MEMCAD [4]). Geodesic falls into the first category.

Another important classification of these systems is the underlying representation used to represent the geometry. Geodesic, for example, relies on polyhedral representations of geometry. VIP3D relied on a boundary-representation (bRep) [29], a common model representation used in solid modeling. A bRep solid can contain polygonal faces and a

polyhedra can be directly represented directly in a bRep. The distinguishing characteristic between these two solid model representations, however, is that a bRep includes analytic surfaces such as NURBS and swept surfaces.

3.2.3 Surface representation

An important design decision in Geodesic was to use polyhedra instead of analytic surfaces such as NURBS. The motivation for this was twofold. First, boolean operations on analytic surfaces can be problematic, particularly on the types of surfaces generated by the techniques discussed later. Second, all of the process simulators used in this work required discretized geometry. This would require a translation of the simulation results from polyhedra into more complex analytic representations which can be difficult.

3.2.4 Process emulation vs. process simulation

Often for complicated structures, or depending on the versatility of the processing steps allowed in the package, non-physical process steps must be introduced to be able to create geometry that mimics what is expected. For example, a common processing step in the fabrication of micro-devices is conformal deposition. However, if your geometry engine cannot perform a conformal deposition, you can sometimes emulate this process using deposition, planarization, and etching with additional masks. Two of the examples discussed in section 3.3 highlight the differences between process emulation and simulation. The reactive ion etching example shows that the results of emulation can be implementation specific, while the level set example shows the inability to properly capture rounded corners and the results of select etches using emulation.

3.2.5 Accessibility to algorithms which achieve multiple levels of physical accuracy

Since devices and desired levels of simulation accuracy vary significantly, Geodesic was designed as an integrated environment to permit varying degrees of physical accuracy. It is important, particularly from a designer perspective, to have a single tool capable of generating geometry from the earliest conceptual stage to final production when detailed knowledge of the fabrication processes can be tweaked for higher yield or better reliability. In addition to an efficient and robust method to create geometry using only solid modeling operations, Geodesic provides the capability to smoothly incorporate physically based 2-D and 3-D deposition and etching process simulation results into the geometry. Three key approaches are employed to achieve varying degrees of physical accuracy: a geometric-based deposition algorithm, domain decomposition, and level set process simulation (see 3.1.4.3).

First, an efficient geometric-based deposition algorithm (detailed in [30]) and standard solid modeling operations form the basis of the process emulation capabilities inside of Geodesic. The algorithm provides for surface angle dependent deposition thickness to allow for non-uniform sidewall and step coverage. The algorithm was designed to be independent of the solid modeling kernel used. Additional details can be found in section 3.4. Second, a domain decomposition algorithm (detailed in [31]) was created to improve the overall computational efficiency for building complex geometries for devices requiring process simulation. The device is decomposed (using the etch masks) at each deposition or etching step into regions identified as needing 1-D, 2-D, or 3-D process simulation. Different geometric and physical approaches to

geometry manipulation can be arbitrarily applied among these regions. The domain decomposition algorithm is a critical enabling technology for the level set technique because it drastically reduces the processing power and memory requirements needed to perform process simulation for a realistic size micro-mechanical device. Finally, Geodesic contains a fully integrated general multi-dimensional level set kernel (detailed in [32]) which can be used for process simulation (see also section 3.1.4.3).

3.3 Examples

3.3.1 Overview

Four examples are included in the results section to highlight the versatility and power of the Geodesic framework:

1. Process emulation
2. Extending geodesic
3. Level set process simulation
4. Internet prototyping

First, the canonical rf switch example gives a detailed look at using the CCPDS specification to generate the geometry of a device fabricated using the MUMPS process. The table shows for each processing step the command specified, the resulting geometry, and implementation issues for the given step inside of Geodesic. Several other examples of the same nature are included with the CD-ROM.

The second example highlights the flexibility and extensibility of the Geodesic framework. Although the default geometric etching algorithm is implemented as described in [11], it may be desired to more accurately account for the effects of anisotropic etching. This example highlights one way of implementing process emulation of reactive ion-etching. Many extensions such as this one are possible because process emulation routines are implemented at a script level using lower level primitives in Geodesic.

The third example shows off the capabilities of the 3-D level set kernel. An example of conformal deposition and selective wet etching shows the geometric features that can be captured using process simulation instead of emulation.

Finally, the efforts in internet prototyping are summarized. It is shown that using a standard web-browser with an internet connection geometry of practical interest can be generated on a remote server and displayed on a local machine.

3.3.2 Example of creating the canonical RF switch test device

As part of this contract an extensive analysis was performed of a canonical RF switch test structure (see [33] for details). Fig. 3-5 shows the schematic of the device and several SEMS of the device which was fabricated using the MUMPS process:

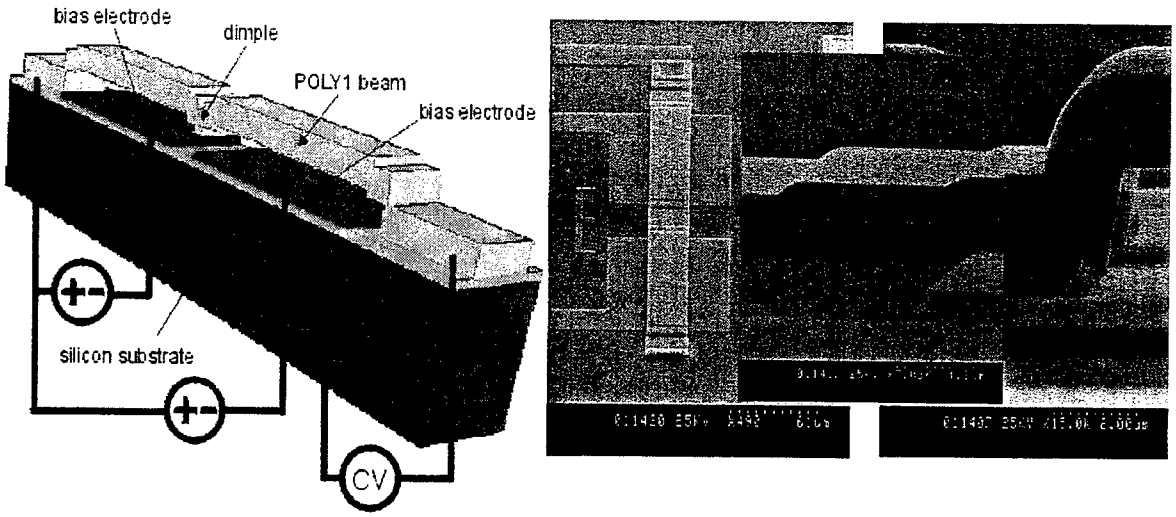


Figure 3-5: Schematic of canonical RF switch and three different SEM views.

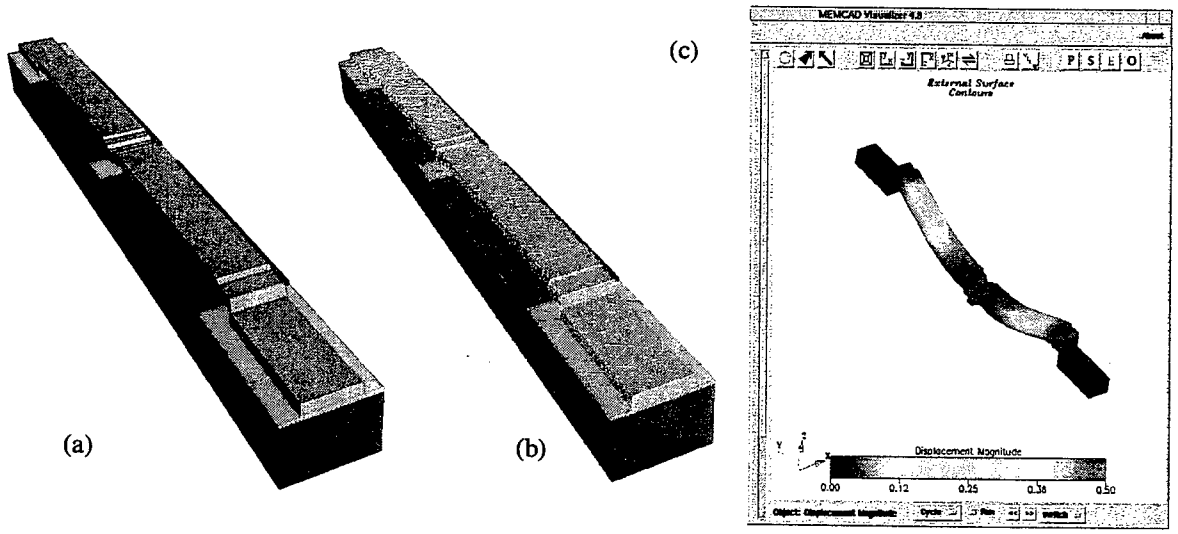


Figure 3-6: Model created using process simulation (a) and meshed (b) in Geodesic and then simulated using MEMCAD (c).

Experimental investigation determined that the sidewalls of the device were not vertical, and that the undercut was occurring during several of the etching processing steps. In addition, simulation results contained in [33] determined that properly capturing these processing effects were critical in calculating the performance of the device. A CCPDS process flow for MUMPS

(similar to that found in [11]) detailed below demonstrates how to build a 3-D solid model representing the switch for electro-mechanical simulation. Fig. 3-6 shows the device created in this example meshed and passed to MEMCAD for electro-mechanical simulation.

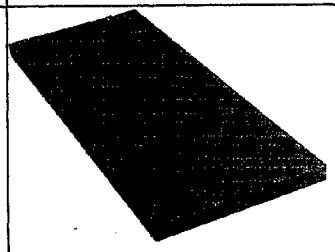
Table 3-1 below shows the processing commands used in conjunction with the CIF file found in Fig. 3-7 to create the geometry of the RF switch.

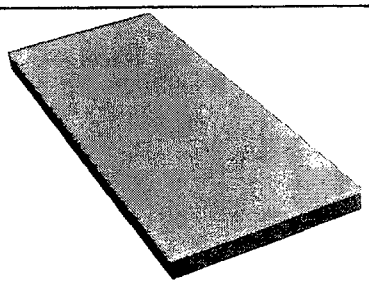
Table 3-1: 12 steps in the process flow for the canonical RF switch. The left column shows the CCPDS command for the given step. The middle column shows the geometry resulting from the given command while the right column discusses important implementation details (*italics* are used for variables while **bold** text is used for actual procedure names found in Geodesic [34]).

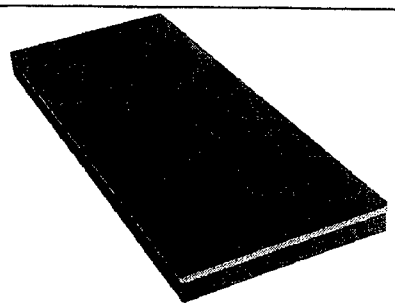
step	CCPDS command	Geometry after Command	Comments

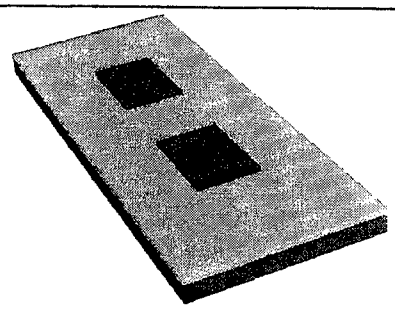
1	ProcessVersion={
	Version="1.0"
	}
			This command specifies the version number of the CCPDS file.

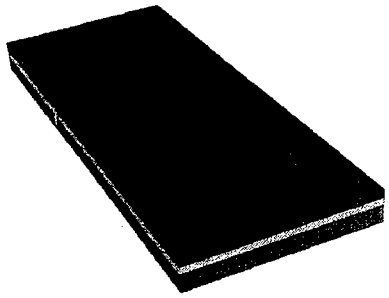
2	ProcessUnit={
	Unit=microns
	}
			This specifies the units to be used throughout the model creation process.

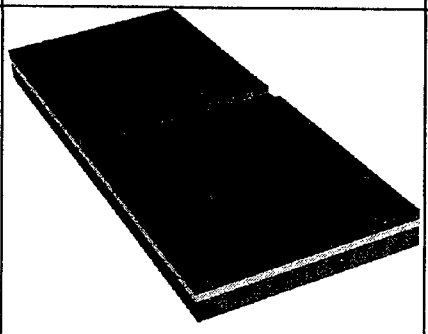
3	Wafer={
	MaskName="GND"
	Thickness=10
	Color=blue
	CIF_filename=masks.cif
	Lambda=1
	}
			Creates a 3-d rectangular solid of *thickness* representing the wafer. It is oriented such that the bottom is in the plane z=0. The *maskName* mask consists of a single CIF box which specifies the center, length, and width of the region of interest.

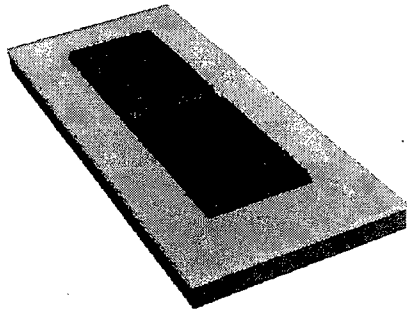
4	Deposit={
	
	DepositType=CONFORMAL
	Face=TOP
	LayerName="Nitride"
	Thickness=0.6
	Scf=c
	Color=green
	}
			Since the device is still planar (no etches have been performed), the deposit routine calls **vfabGeometricDeposit** which creates a rectangular solid of thickness properly oriented in space (with layer *centroid* = *overall_height* + (*thickness* / 2)).

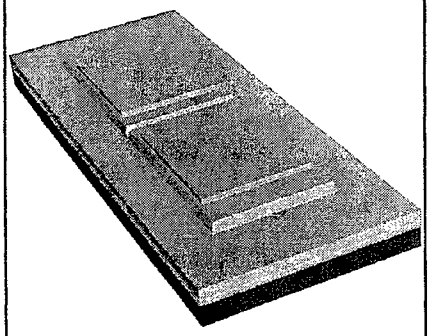
5	Deposit={
	
	DepositType=CONFORMAL
	Face=TOP
	LayerName="Poly0"
	Thickness=0.5
	Scf=c
	Color=red
	}
			This deposit is done the same way as step 4. All conformal depositions are performed this way until an etch is performed. Once an etch is performed, *device_is_planar* is set to FALSE for the rest of the steps (unless a MechanicalPolish or DepositType=FILL is performed).

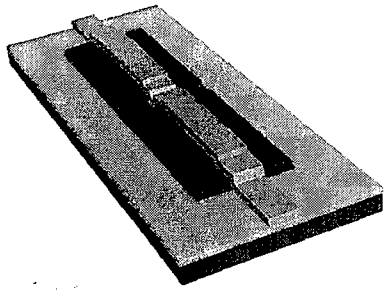
6	Etch={
	EtchType=SURFACE
	Face=TOP
	MaskName="CPZ"
	EtchMask=OUTSIDE
	Depth=3
	Angle=87
	Undercut=0.157
	EtchRemoves="Poly0"
	}
			This etch step causes the variable *device_is_planar* to be set to FALSE. Since this etch involves an undercut and results in angled sidewalls, **vfabAngledEtch** is used. Only the *Poly0* layer is effected by the etch since it appears within the EtchRemoves.

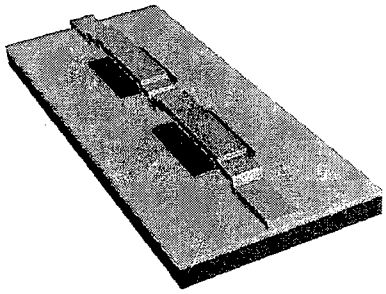
7	Deposit={
	
	DepositType=CONFORMAL
	Face=TOP
	LayerName="ox1"
	Thickness=2
	Scf=.01
	Color=purple
	}
			Since *device_is_planar* is FALSE, we have to use the more general **vfabOffsetDeposit** algorithm which in essence creates the deposited layer by offsetting the original geometry by *thickness* along the surface normals.

8	Etch={
	EtchType=SURFACE
	Face=TOP
	MaskName="DIMP"
	EtchMask=INSIDE
	Depth=1.2
	Angle=75
	Undercut=0.32
	EtchRemoves="ox1"
	}
			This etch uses **vfabAngledEtch**. Note that EtchMask=INSIDE tells the geometry engine to remove the material "underneath" the mask layout. In actual fabrication this corresponds to a negative resist.

9	Etch={
	EtchType=SURFACE
	Face=TOP
	MaskName="MORE"
	EtchMask=OUTSIDE
	Depth=4
	Angle=75
	Undercut=0.32
	EtchRemoves="ox1"
	}
			This etch uses **vfabAngledEtch**. Note that EtchMask=OUTSIDE tells the geometry engine to remove the material from around the mask layout. In actual processing this corresponds to a positive resist.

10	Deposit={
	
	DepositType=CONFORMAL
	Face=TOP
	LayerName="Poly1"
	Thickness=2
	Scf=.01
	Color=deepskyblue
	}
			Again since *device_is_planar* is FALSE we use the general offset algorithm as in step 7. Note that it is very important that small features that would "fill in" such as dimples be removed from the masks by the user in a layout editor before using the offset solid algorithm. The algorithm does not allow for topologic change (you need to use an algorithm such as the level set method for this).

11	Etch={
	EtchType=SURFACE
	Face=TOP
	MaskName="TOP"
	EtchMask=OUTSIDE
	Depth=6
	Angle=90
	Undercut=0
	EtchRemoves="Poly1"
	}
			Since there is no undercut or angle required by this etch, **vfabGeometricEtch** is used. This corresponds to simply extruding the mask in the z-direction by *depth* and subtracting the resulting extruded-solid from the layer (Poly1) specified by the EtchRemoves token.

12	Etch={
	EtchType=SACRIFICIAL
	Face=TOP
	EtchRemoves="ox1"
	}
			The sacrificial etch removes an entire layer from the database. No visibility calculations or the like are performed. This means that completely unphysical processes (such as removing unexposed material) can be performed using this command.

```
(CIF file for canonical_3d.ccpds);
DS 1 1 1;
L GND;
B 60 500 0 0;
L DIMP;
B 100 10 0 0;
L MORE;
B 100 360 0 0;
L CPZ;
B 40 150 0 -90;
B 40 150 0 90;
L TOP;
B 30 500 0 0;
DF;
C 1;
E
```

Figure 3-7: CIF file for canonical test device.

3.3.3 Example of extending Geodesic – Reactive ion etching

In the current implementation of the CCPDS inside of Geodesic, etching is performed by extruding the mask and subtracting the resulting solid from the layers specified by the "EtchRemoves" option. While this emulates some physical processes well, on non-planar geometry it can be a poor approximation. Fig. 3-8 shows a schematic of reactive ion etching. The yellow region on the left represents the material that should be removed by an idealized reactive ion etch of unit depth. The figure on the right shows what occurs using the "vfab" scripts inside of Geodesic to perform the etch. In this case the yellow region represents material which should have been removed but was not.

One of the examples included with the beta release of Geodesic has an example script implementing an idealized reactive-ion etch. The key points of this example are now summarized. We assume we have three given objects:

1. 3-D solid model of a layer named "etchMe" we wish to etch by a unit depth.
2. 2-D polygonal solid of an etch mask named "myMask".
3. 3-D solid named "mems_device" which is the exterior of the entire device.

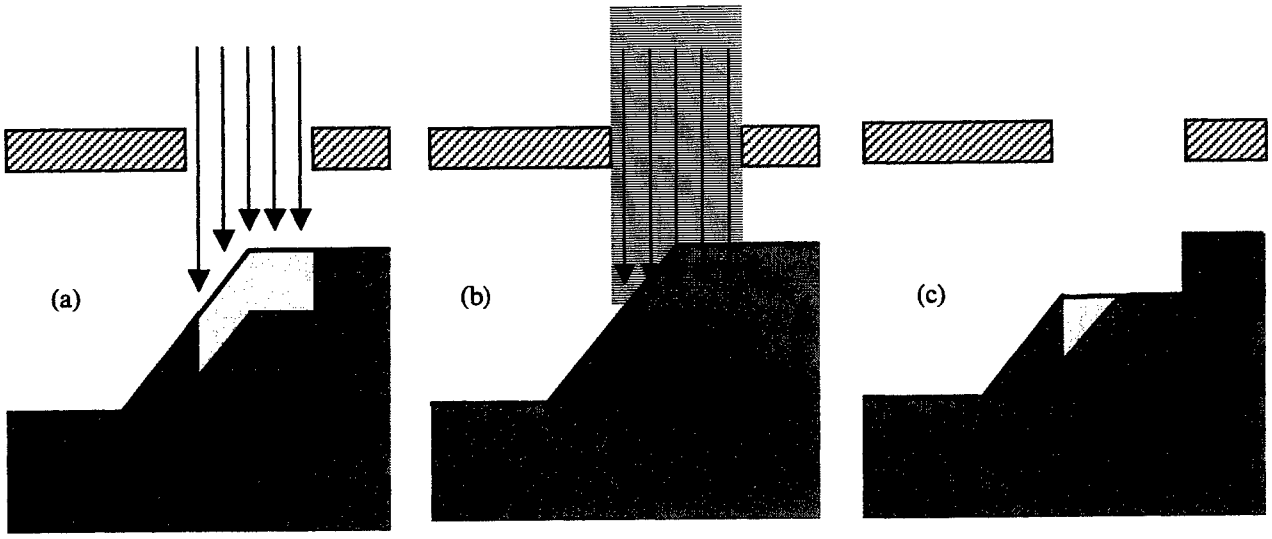


Figure 3-8: The left figure (a) shows in yellow the material which should be removed by an idealized reactive ion etch. The middle figure (b) shows the effective extrusion of the mask by a unit depth, and the right figure (c) shows the material actually removed by the etch simulated using an extruded version of the mask.

A normal idealized etch (Fig. 3-8 b,c) in pseudo-code would be:

```
# extrude the mask in the z-direction by 1 unit
#    note: the 2d-solid mask is in the z=0 plane
solid_extrudeZ –src myMask –dst extruded_mask –dist 1.0

# translate the solid of the extruded mask so that it is
# properly oriented in space
extruded_mask Translate –vec {0 0 (overall_height – deposition_thickess)}
```

8b

```
# now do a boolean subtraction of the etch mask from the layer to be etched
solid_subtract –result tmp –a etchMe –b extruded_mask

# now replace the existing object with the desired result
solid_copy –src tmp –dst etchMe
```

8c

The reactive ion etch involves more steps (see Fig. 3-9):

```
# the offset solid routine works only with polyhedra, so we extract the facets
# from mems_device:
mems_device GetPolyData –result device_polydata                          9a

# note: several Vtk procedures are called at this point to merge coincident points and
# consistently orient the triangles of device_polydata. See the example on the CDROM
# for more details.

# offset the solid for a "negative deposition." That is, we want to move the surfaces
# inward along the surface normal. Since by convention inside of Geodesic the surface
# normals point inwards, we actually specify a positive displacement.
vfab_OffsetSolid –src device_polydata –dst tmp_polydata –offset 1.0      9b

# the output of the offset solid command is a vtkPolyData object, so now we create
# a solid polyhedra
solid_poly3dSolid –result tmp1 –src tmp_polydata –facet Union            9c

# now we subtract the offset solid from the original solid. This effectively leaves us
# with a solid which could be subtracted from the original geometry to do a unit depth
# ion etch over the entire device. However, we only want to etch the area exposed by
# the mask.


# we now want to find the material which should be removed because it is exposed by
# the mask. To do this, we intersect a solid representing the visible area with "tmp1".
solid_extrudeZ –src myMask –dst tmp2 –dist overall_height                9d
solid_intersect –result tmp3 –a tmp1 –b tmp2                             9e

# now do a boolean subtraction of the etch mask from the layer to be etched
solid_subtract –result tmp4 –a etchMe –b tmp3
                                                                         9f
# now replace the existing object with the desired result
solid_copy –src tmp4 –dst etchMe
```

We have then emulated a reactive ion etch as desired, with a resulting geometry pictured in Fig. 3-9f.

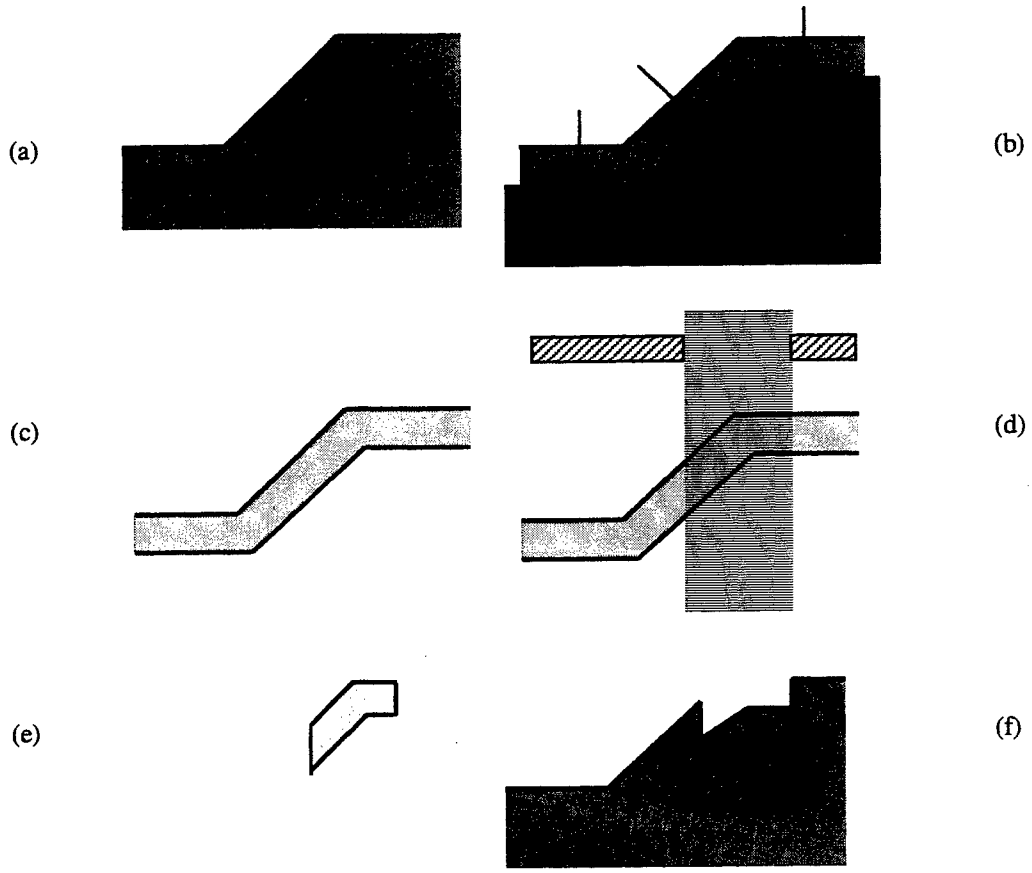


Figure 3-9: Schematic of the 4 step process to emulate a reactive ion etch. (a) shows the original geometry, while (b) shows the offset of the top surface in the direction of the inward normal. (c) shows the result of the Boolean subtraction of the solid created in (b) from the original solid in (a). This layer would corresponds to a reactive-ion etch over the entire surface. (d) shows the intersection of rectangular solids created based on the etch mask to represent the area of the wafer exposed by the etch mask. Finally, the resulting solid from (d) show in (e) is subtracted from (a) to obtain the desired result.

3.3.5 Example using Geodesic level set module: Process simulation

The use of process emulation, and in particular solid modeling based methods to build geometry such as the CCPDS, works for many cases of interest. However, there are practical situations where topologic change can occur (e.g. via or dimple filling) and the "boxy" nature of the methods created using the CCPDS standard are insufficient. In these cases one must utilize more sophisticated techniques to create the desired geometry. One such method is the level set method. There is a rich body of literature on using the level set method with appropriate velocity functions to simulate IC processing steps such as deposition and etching [20].

The level set equation of evolution is:

$$\Phi_t + V\,|\nabla\Phi| = 0$$

where: Φ = scalar function implicitly representing interface (locus where Φ=0)
V = velocity function normal to the propagating interface incorporating physics of deposition/etching

In this example we utilize the level set kernel inside of Geodesic (detailed in [32]) with two velocity functions to simulate wet etching and conformal deposition. In the case of conformal deposition, we assume a constant normal velocity v = 1.0. In the case of etching we assume a velocity function which simulates selective isotropic etching.

Inside of Geodesic, the setup required to simulate conformal deposition and isotropic selective etching is very similar. In the case of deposition, we track the top surface of the device using the scalar field Φ. In etching, on the other hand, we actually track the boundary of the "air" region surrounding the device (i.e. the scalar field Φ implicitly represents the surface of the air region). The reasoning behind the difference is simple. We are only using the zero level set ($\Phi = 0$) to define a material interface, so we can represent only one material with Φ. Since we want the ability to do selective etches on multiple materials, we represent the boundary of the "air" region. In the case of isotropic wet etching, this can be thought of physically as tracking the surface of the etchant.

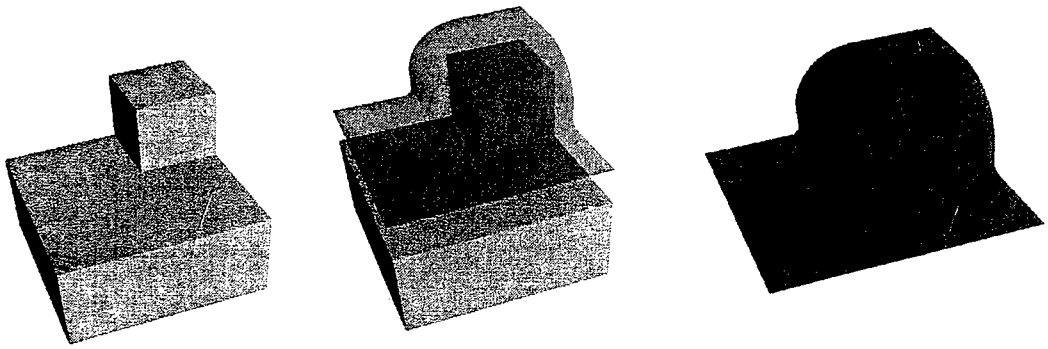
The following pseudo code highlights the important aspects of performing process simulation inside of Geodesic using the level set kernel (the actual scripts are included in the examples with the software distribution):

```
# define the desired deposition thickness / etch depth
thickness = 1.0

# create a solid with a raised center block in the center
solid_box3d -result box1  -dims {...} -ctr {...}
solid_box3d -result box2  -dims {...} -ctr {...}
solid_union -result input_geom -a box1 -b box2

# create air region
solid_box3d -result tmpair  -dims {...} -ctr {...}
solid_subtract -result air -a tmpair -b input_geom

# Set up grid domain
h = {0.500 0.500 0.500}
origin = ...  (lower left hand corner of solution domain)
```

```
dims = ...   (overall extent of simulation domain)

# Instantiate velocity function
#   deposition == constant function (setVConst)
#   etch       == selective etch function (lsetVSelEtch)

if (deposit) {
  velocity = 1.0
  setVConst vfn
  vfn SetV -v $velocity
}

if (etch)  {
 lsetVSelEtch vfn
 vfn SetRate -rate 1.0
 vfn AddRegion -obj box2 -sel 0.1
 vfn AddRegion -obj box1 -sel 1.0
}

# Compute time-step parameters to give desired deposition thickness.
# The level set kernel automatically calculates the maximum allowable time step
# based on the CFL condition.  In this case, since V = constant, we can directly
# calculate the number of times steps the kernel needs to perform to deposit
# the desired amount of material.
numSteps  = ...

# Setup level set core

lsetCore core

core SetTime -simTime -1.0 -cflFactor 1.0
core SetGrid -h $h -dim $dims -origin $origin \
        -type SparseGrid -bandExt {...}
core SetVelocity -vobj vfn
core SetTimers -flag 0

# initialize based on desired process to simulate
if (deposit) {
 core SetSolidSeed -solid input_geom
}

if (etch) {
 core SetSolidSeed -solid air
}
```

```
core Init

# the "lset_for" loop runs the level set simulations for a given number of time
# steps.
set verbose 0
lset_for core $numSteps { } $verbose 1 0

# extract a surface, which either represents the top surface of the new
# material in a deposition or the surface of the "air" region Iin the case of an
# etch.
core ExtractFront -out output_pd -closed 0
```

Fig. 3-10 shows the results of the deposition on a corner, while Fig. 3-11 shows the results of an isotropic etch with materials of two difference selectivities.



(a) (b) (c)

Figure 3-10: A conformal deposition of unit thickness on a corner. (a) original corner, (b) corner with deposition, (c) close up of levelset function.

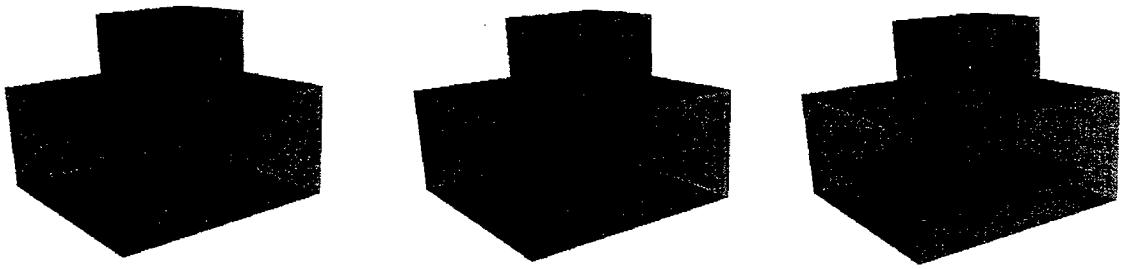


Figure 3-11: Example of a selective corner etch using the integrated 3-D level set kernel in Geodesic. The figure shows three steps in the evolution of the boundary surface, where the red surface indicates the level zero function. As can be seen, the small block on top of the larger block is more resistive to etch.

3.3.6 Examples of internet based prototyping

The proposed client-server architecture for MEMS prototyping discussed in section 3.1.3 is demonstrated with several representative device examples. Fig. 3-12 shows typical electro-mechanical devices such as switches, micromirrors, and combo drives created using the web-based environment (Fig 3-3). In addition, Fig. 3-13 shows a representative mesh of a simple switch and a micromirror. Table 3-2 shows examples of file sizes for the various micro-electro-mechanical devices. Both VRML and OOGL (the file format used by JGV) are ASCII file formats. Most VRML browsers permit the input files to be compressed using the gzip compression algorithm. This greatly reduces the size of the actual file transmitted, as can be seen in Table 3-2. As the table indicates, all of these geometries can be transmitted in a reasonable amount of time even over a 56 Kbps modem (i.e. low bandwidth connection). Also shown are example file sizes for coarse meshes for each of the devices. Note that even though a volume mesh is being generated for each device by the server, only the surface mesh needs to be transmitted back to the client for viewing. These results show great promise for internet-based prototyping of microsystems as an area for future work.

Table 3-2: File size (in bytes) of four example MEMS devices.

Device	Geometry		Surface Mesh	
	VRML*	OOGL	VRML*	OOGL
Dual Electrode Switch	6116	43119	9926	61510
Comb Drive	52257	479440	87137	580514
Torsional Micromirror	4215	28743	11827	149934
Simple Switch	1429	8012	2762	30909

*gzipped file size

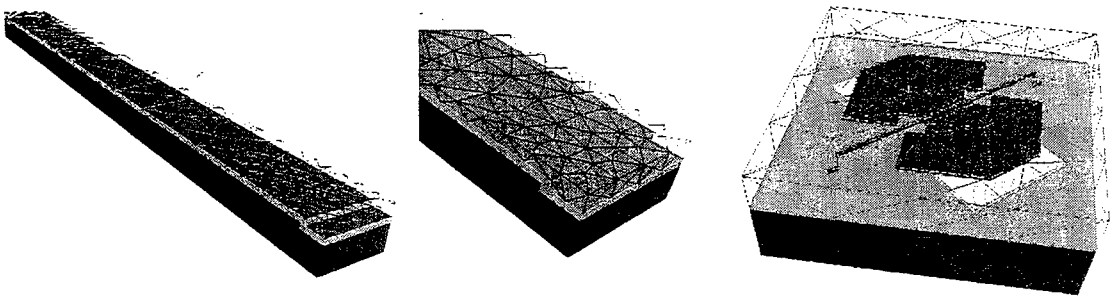
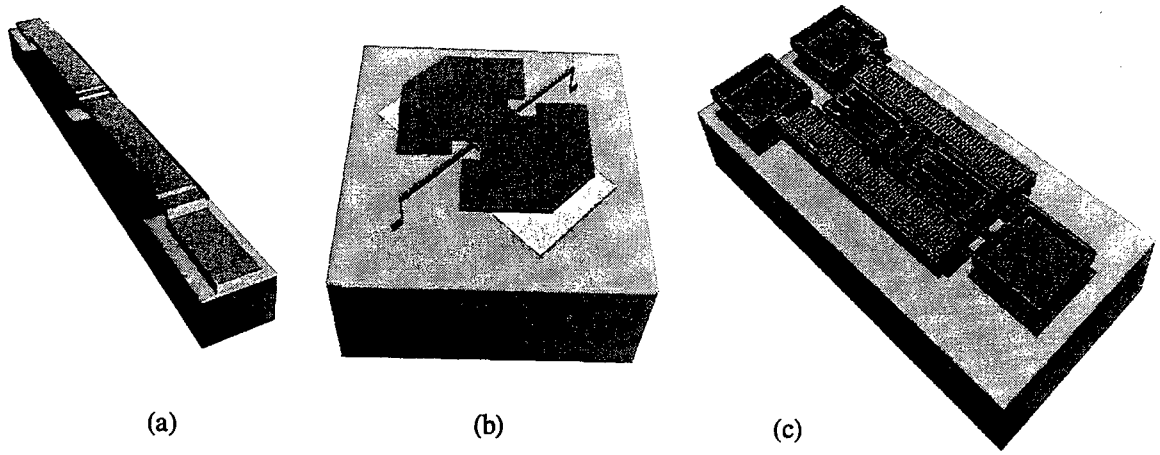


Figure 3-12: Two examples of mesh generation. The simplified switch (a) and the close up of the step up (b) showcase automatic mesh generation with grading. The mesh for the micromirror (c) was also created automatically. Note: All of the meshes are volume meshes with only the exterior surfaces of each layer shown for clarity. In addition, the air region around each device was meshed as indicated.



(a) (b) (c)

Figure 3-13: Three different MEMS geometries created using Geodesic. The switch (a) was created using domain decomposition and process simulation. The micromirror (b) and comb drive (c) were created using the geometric algorithm. Geometries exaggerated in the z-direction for clarity.

3.4 A solid modeler independent implementation of the Composite CAD Process Definition Specification

3.4.1 Introduction

The "Composite CAD Process Definition Specification 1.0" [11] is a proposed standard for MEMS CAD vendors to specify the process flow used to create geometry (i.e. solid models) for simulation. The file format is the product of over a year of interaction of numerous vendors which resulted in a useful format with wide application for microsystems. The standard had several key design objectives. First, it was designed to be an ASCII text file that was "human readable." In addition, the processing steps were to be the most common used in microsystems (with particular focus on process operations which altered the physical geometry). Finally, version 1.0 was designed to be a minimal standard so that maximum compliance across vendors could be achieved.

This section describes the implementation details of the basic standard found in [11]. Here the overview of a solid modeler independent implementation is given. The actual source code can be found on the CD-ROM. The CCPDS format consists of eight commands, which are organized functionally in Table 3-3:

Table 3-3: CCPDS commands organized by functionality

Book-keeping	Process Emulation	Process Macros	Misc
ProcessVersion ProcessUnit	Deposit Etch Mechanical Polish	ImplantDiffuse Grow	Wafer

Each of the four functional categories will be discussed separately. It should be noted that the "basic" CCPDS requires only solid modeling operations to build geometry of interest. While this standard is useful for many applications, section 3.4.4 will close by discussing the limitations and ambiguity in the file format. An import example outside of the current standard is utilizing process simulation to build geometry was seen in section 3.3.

3.4.2 Discussion of commands

3.4.2.1 Book-keeping

These commands are not specific to any particular step in the process flow. They typically should appear first in a given process flow since they effect the meaning of the other commands in the file.

1. ProcessVersion
   This command allows the user to specify the version number of the process flow file. It is useful since it allows for the standard to evolve in the future without invalidating the users existing process flows. In addition, it permits the vendor to determine if the user has imbedded extra information in the file (e.g. extensions).

2. ProcessUnit
   This command allows the user to specify the units to be used in creating the model. All of the operations in the basic standard have been implemented to be dimensionally independent.

3.4.2.2 Miscellaneous

The only miscellaneous command consists of the "Wafer" command. This is an important command that must appear prior to any processing steps in the process flow. The wafer is specified using a box in the CIF file, and is specified such that the "bottom" of the wafer is in the plane z=0. All additional processing steps (e.g. depositions) will take place on the wafer. This allows us to define the "overall height" of the device as the distance from the bottom of the wafer to the maximum z-coordinate in the model.

3.4.2.3 Process macros

Process emulation macros differ in a significant way from the other process emulation commands. Namely, while these commands represent common IC processing steps (e.g. dopant implant and diffusion), the implementation proposed in the standard requires significant approximations and consist of performing a fixed sequence of steps using other commands from the CCPDS. For completeness the major steps involved are listed, but the reader is referred to [11] for the detailed explanation of these macros.

1. Grow

This command is a gross approximation to the growth of thermal oxide on a silicon substrate. It does not predict residual stress or other physical characteristics of this processing step. It consists of the following sequence of fundamental steps:

a. etch silicon that would be converted during the thermal oxidation
b. deposit oxide
c. etch oxide where growth would be inhibited by a nitride mask

2. Implant Diffuse

This command allows the user to create multiple solid regions from an initial layer (e.g. to assign differ material properties to a region of higher doping). It consists of the following sequence of fundamental steps:

a. etch initial layer
b. deposit layer of higher doping
c. etch layer of higher doping

3.4.2.4 Process emulation

The process emulation commands consist of methods to add material (deposition) and remove material (etch, mechanical polish) from a given wafer. Recall that these are process emulation steps in that the user must know the final outcome of the real processing step (e.g. deposition thickness).

There are three types of emulated deposition supported by the CCPDS standard: conformal, snowfall, and fill. We will further subdivide conformal deposition into two categories for implementation purposes: planar and general-topology. Geodesic has an additional physical deposition type that can be invoked to use process simulation. See the results section (Fig. 3-10, 3-11) for a discussion on process simulation using the level set method. Fig. 3-14 shows the organization of the deposition commands. The only CCPDS deposition type not explicitly permitted is "snowfall." This can be integrated in a straight forward manner by adding an anisotropic velocity function which takes into account visibility calculations and sticking coefficients (see [20]). Fig. 3-15 shows graphically the conformal and fill deposition types. The conformal deposition on a non-planar topology relies heavily on the offset solid algorithm detailed in [30].

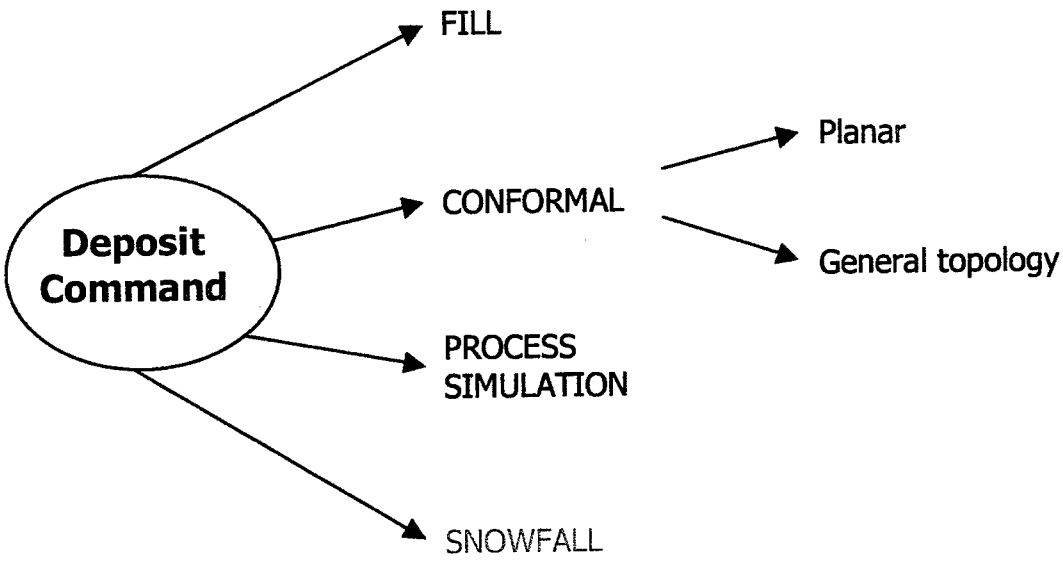


Figure 3-14: Deposit types flow chart.

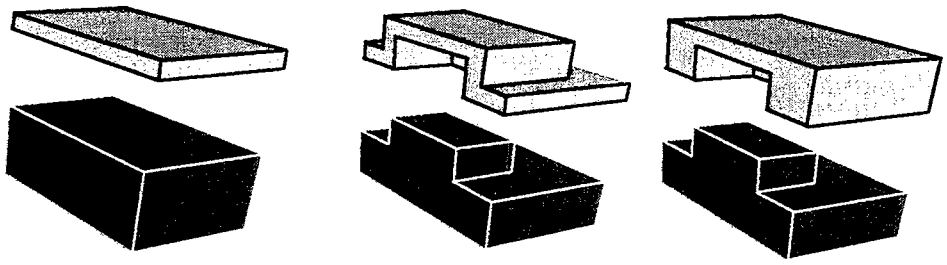


Figure 3-15: Three types of deposition. (a) shows planar deposition, (b) shows conformal deposition, and (c) shows a fill operation.

Fig. 3-16 shows schematically the steps involved in using the offset solid algorithm to perform a conformal deposition. In a preliminary step, all of the current layers and wafer for the device are unioned together simplifying all internal boundaries. This leaves a solid with only exterior walls (i.e. free surfaces) as seen in Fig 3-16 (a). Conceptually, we want to generate a new solid (d) that we can subtract the original geometry (a) from and have the result be the deposited material. This requires four major steps. First, the bottom and sides of the wafer are identified (b) and fixed so they cannot move. This can be thought of as only wanting to deposit material on top of the wafer. Second, infinite planes representing the remaining faces are offset in the direction of the normal by the specified deposition thickness (this can be a function of the normal direction). Third, the vertices of the model are cycled over. At each vertex, the intersection of all infinite planes representing the faces meeting at the vertex is calculated. Assuming the topology of the device doesn't change, these vertices along with the original connectivity define the new geometry shown in (d). The final step consists of doing a boolean subtracting of (a) from (d) to get the desired result.

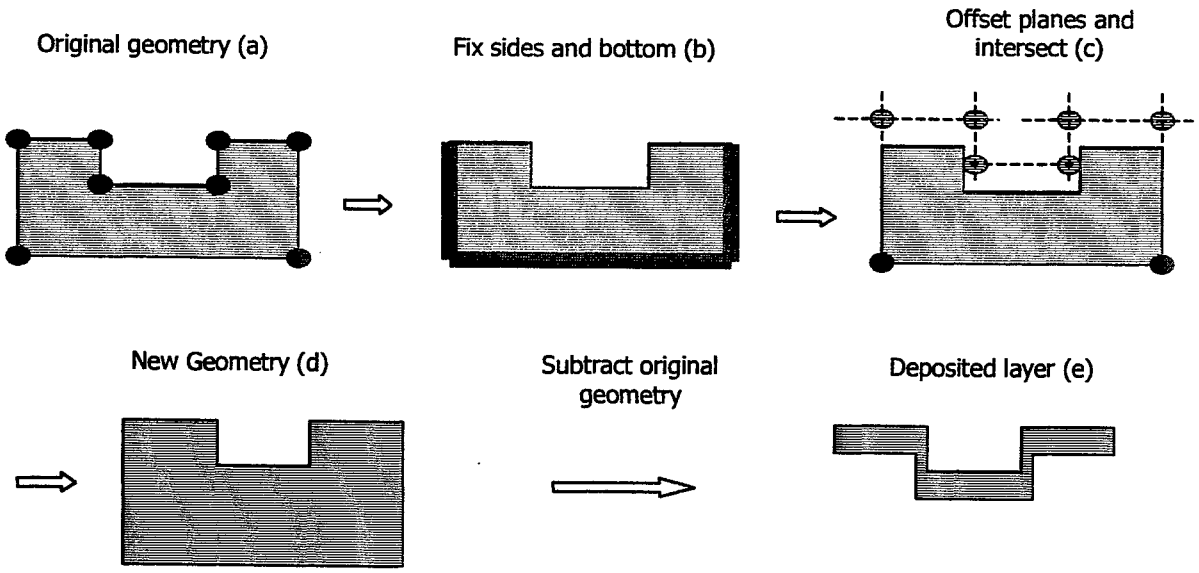


Figure 3-16: Using the offset solid algorithm in Geodesic to generate a conformal deposition. Conceptually, we want to generate a new solid (d) that we can subtract the original geometry (a) from and have the result be the deposited material.

There are three types of etching defined in the CCPDS: Sacrificial, Surface, and Bulk. In addition, Geodesic has an additional type of etching using the level set kernel for physical process simulation. For implementation purposes, we further subdivide surface etching into two categories: ideal, and undercut with angled-sidewalls. The standard also subdivides surface etching into two types: inside and outside. Fig. 3-17 shows the organization of the etch commands.

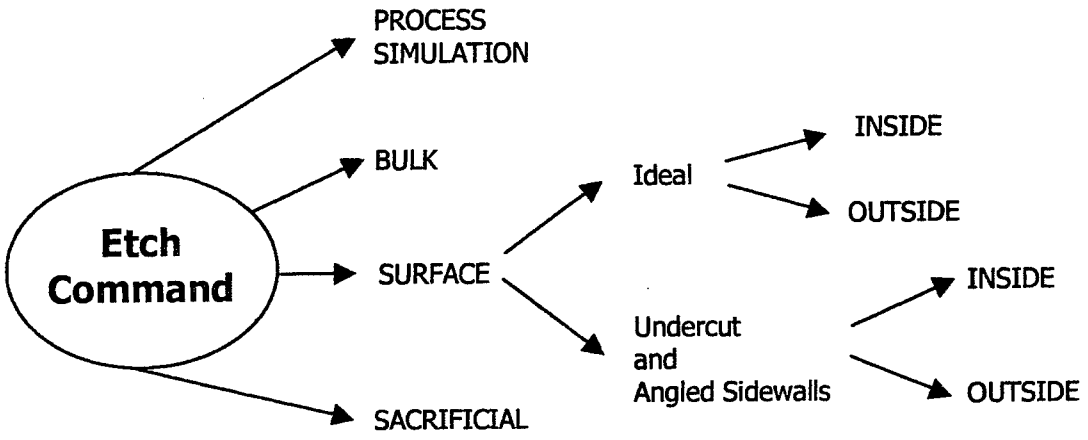


Figure 3-17: Etch types flow chart.

The sacrificial etch represents the release step commonly used in microsytems. In the present implementation, this corresponds to deleting the specified layer of material. This is an approximation that assumes that the material is ideally (i.e. completely) removed, and that the entire sacrificial layer is exposed to etchant. This is not always the case, and special procedures will have to be employed if part of the sacrificial material is to be maintained in the final device geometry.

The case of surface etching with vertical sidewalls and no undercut begins with extruding the mask in the z-direction by appropriate depth of the etch. If "EtchMask=INSIDE" is specified, then this extruded solid is subtracted from each layer specified in the command step. If "EtchMask=OUTSIDE" is specified, then a two step process is required. The first step involves creating a "negative" of the extruded mask solid by subtracting the extruded mask from a rectangular solid the size of the wafer with a thickness of the etch depth. The second step involves subtracting the negative mask solid from each layer specified in the command step.

Performing a surface etch with angled sidewalls and / or undercut is more complicated. The masks are required to consist of non-overlapping simple CIF box objects. The box is then scaled by the undercut value depending on the type of etch performed. Outside etches require the box edges move inward by the specified undercut, while an inside etch requires the box edges move in the outward direction by the specified undercut. Using trigonometry, the image of the box is also calculated at the specified depth of the etch. The end result is eight vertices with a known connectivity which can be used to create a trapezoidal solid. The aggregation of these trapezoidal solids is then used in place of the extruded etch mask, and the process of handling the "EtchMask=INSIDE" and "EtchMask=OUTSIDE" is identical to the vertical wall case. Note that only simple etch masks are handled properly with this implementation. Overcoming this

limitation likely requires performing identical operations as discussed on arbitrary polygonal shapes.

The final type of etching in CCPDS is anistropic bulk etching (i.e. EtchType=BULK). The bulk etching option is a special case of surface etching with angled sidewalls. The first step is to find the minimum bounding box (MBB) of the specified etch mask. Using the resulting MBB as a pseudo mask, a surface etch with a sidewall angle of 54.7 degrees is then performed.

3.4.3 Additional notes on implementation of CCPDS inside of Geodesic

There is a general description of the Geodesic architecture in section 3.1.4 of this report, and it is important to point out additional key aspects relating to the processing of the CCPDS file to create a solid model. In Geodesic, we utilize the scripting language Tcl to process the CCPDS file (which is typically only a few hundred lines of text) while coding the computational intensive commands in C++ with bound Tcl-interpreter commands. The scripts were written in a modeler independent way by using Tcl-bound commands which have modeler implementations "hidden" from the interpreter level. The user can toggle between solid modelers using the "solid_setKernel" command (see [34]), and the scripts remain unaltered. Although we have implemented a more general set of solid modeling commands in our modeler-independent API, Table 3-4 indicates the commands required to implement the basic CCPDS standard. In addition to the "solid_" commands which typically create objects, a SolidModel object has a set of useful methods. Geodesic provides more methods than required to implement the basic CCPDS standard, so Table 3-5 summarizes only the required SolidModel methods to implement the standard.

3.4.4 Limitations of the CCPDS standard

The CCPDS standard has several important limitations. First, it was designed to be a standard that could be implemented using only solid modeling operations as detailed above. However, it is impossible to include the results of detailed process simulation into the final geometry. Second, the standard is predominately written from a 2-D perspective. For example, in surface etching the angle is not clearly defined in the general 3-D setting. Third, it is possible to perform a sequence of depositions and etches which make specifying subsequent steps impossible using just variables such as undercut and angle. Finally, several of the commands are overly simplistic. For example, a sacrificial etch just removes a layer from the model, which can lead to unphysical results if part of the sacrificial layer was not accessible to the etchant.

Table 3-4: Solid modeling commands required to generate geometry*.

	General	Create	Booleans
Basic CCPDS	solid_getKernel solid_setKernel solid_readNative	solid_box2d solid_box3d solid_copy solid_extrudeZ solid_poly3dSolid solid_polyPts	solid_subtract solid_union
Domain Decomposition	*no additional*	solid_poly3dSurface solid_extrude	solid_intersect
Level Set	*no additional*	*no additional*	*no additioal*

*Note that only the first six rows are required for generating geometry for the standard CCPDS, while additional commands are required if domain decomposition or level set simulation is desired.

Table 3-5: Solid model object methods required for model generation

	General	Transforms	Classifications	Labels*
Basic CCPDS	GetClassName GetKernel GetPolyData WriteNative	Translate	*none*	ClearLabel GetLabel GetLabelKeys SetLabel
Domain Decomposition	*no additional*	Rotate Scale	Find Centroid	*no additional*
Level Set	*no additional*	*no additional*	ClassifyPt Distance	*no additional*

although methods to manipulate labels appear in the solid model object, these are equivalent to the more general "repos_*Label" repository label commands.

3.4.5 Summary of CCPDS

In summary, the CCPDS is an extremely useful file format for specifying process flows relevant for MEMS simulation. Although it has some limitations, these can be overcome by providing extensions and clarifications to the basic standard. Unfortunately, the standard has failed to receive widespread adoption by the commercial MEMS CAD vendors, which limits its ultimate practical effectiveness.

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4. Characterization of MEMS Materials Models

Authors: Dr. Guido Cornella, Dr. Hoo-Jeong Lee, Ping Zhang, Prof. John C. Bravman

4.1 Monotonic and Cyclic Testing of Thin Film Materials for RF Switch Application

In MEMS devices, many of the active components exist in the form of free-standing thin films. Such components are constantly in motion under various actuation or stimulation. Understanding the mechanical properties and modeling the mechanical behavior of free-standing thin films is therefore important for the design of MEMS devices, as well as for predicting their mechanical performance and reliability.

The mechanical behavior of a free-standing thin film is expected to be different from that of bulk material or a conventional thin film on a substrate. In a free-standing thin film, the grain size is typically very small and the absence of a substrate leads to both its top and bottom surfaces being unconstrained. These microstructural characteristics may result in unique mechanical properties. Although thin films on substrates have been extensively studied, knowledge of free-standing thin films was not available until the advent of micromachining techniques and is yet to be further explored. We have developed a sample fabrication process which batch produces free-standing thin film samples using micromachining techniques within a cleanroom facility.

Basic materials parameters that are required for mechanical device modeling are, among others, the stress-strain response for monotonic and cyclic loading. We have built a custom-designed micromechanical testing system that is capable of providing accurate stress-strain data for monotonic loading as well as for cyclic loading up to a very large numbers of cycles. In conjunction with a dedicated sample fabrication process, we are able to carry out mechanical testing on a wide range of free-standing thin films of different materials and different geometry. We use Transmission Electron Microscopy (TEM) to reveal the microstructural features of the samples both before and after testing, which facilitates our understanding of the mechanical properties of the thin film materials under investigation.

One particular MEMS application we are trying to simulate through our testing is the operation of an RF switch. We are interested in its one-time switching behavior as well as its cyclic operation in the kHz frequency range, which correspond to monotonic and cyclic loading conditions, respectively. We are also interested in the stress relaxation behavior, important for when the switch is held at the "on" position for an extended amount of time. We have studied pure Al and Al/Ti-alloyed thin film samples and obtained stress-strain responses as well as stress relaxation data from both monotonic and cyclic loading, and have simulated the stress relaxation behavior by anelastic models.

4.1.1 Sample Fabrication

Specimens were fabricated using micromachining techniques at the Stanford Nanofabrication Facility (SNF). The fabrication process makes use of two masks. The front-side mask defines the micro beams; the backside mask defines the silicon windows to be etched away to release the

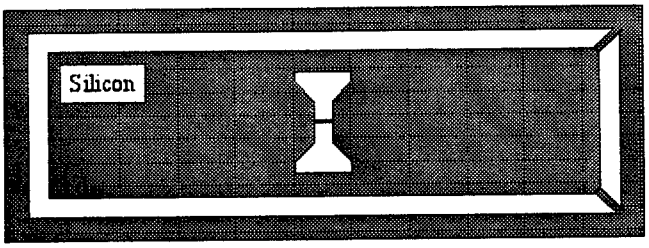

Figure 4-1: Die schematic of a micro beam specimen.

beams. There are 34 dice per wafer, with each die (Fig. 4-1) measuring 8mm×21mm. Each die contains one micro beam (Fig. 4-2), which measures 50μm wide and 500μm long (gauge section), while the thickness varies. For ease of die removal upon completion of the process, a groove about 500μm wide is designed to surround each die. The groove is formed during the silicon backside etch, which leaves the die attached to the remainder of the wafer by only two small silicon support bridges at two corners of the die.

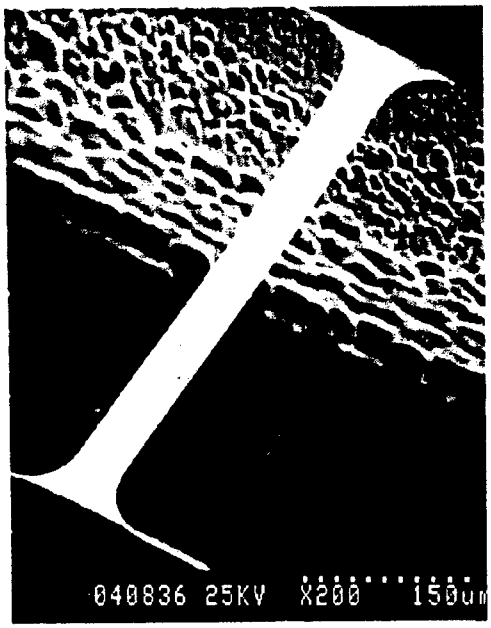

Figure 4-2: SEM micrograph of a free-standing
Al micro beam specimen (prior to testing).

We began the fabrication with (100)-oriented 4-inch silicon wafers. First, 1μm of silicon nitride was deposited by Low Pressure Chemical Vapor Deposition (LPCVD) on both sides of the wafer. Using Photo Resist (PR) to protect the front-side nitride, the backside nitride was removed by a dry etch; the front-side nitride was used later as an etch-stop layer during the silicon bulk etch to release the micro beams from the backside. Next, a metal layer (e.g. Al) was sputter deposited onto the front-side of the wafer, and then patterned with the front-side mask to define the micro beams. Afterwards, a thick layer of PR was put down onto the backside of the wafer

and patterned with the backside mask. This patterned PR acted as an etch mask for the removal of silicon from the backside of the wafer through window regions defined by the backside mask. Silicon was then dry-etched through the wafer thickness (about 500μm) until the front-side LPCVD nitride was reached. Lastly, the nitride was removed by dry etch from the backside, and the micro beams were released.

For the fabrication of the Al/Ti-alloyed micro beams, we previously employed the method of multi-layer metal deposition. For example, to achieve micro beams of 2% of Ti and 2μm in thickness, a 7-ply of 0.5μm-Al/10nm-Ti multi-layer was deposited on the front-side of the wafer during the metal deposition step, followed by subsequent annealing at 550 °C for one hour in a nitrogen atmosphere. We are currently exploring the method of co-sputtering, where metals from the two targets of 100%Al and Al-10%Ti are simultaneously deposited onto the silicon substrate. As we adjust the relative powers of the two targets, ranging from 0.5kW to 8.5kW, we are able to achieve Ti concentrations in the range of 1.5%-5.5%.

4.1.2 Experimental Setup and Procedures

4.1.2.1 Micromechanical Testing System

The heart of the custom-designed micromechanical testing system (Fig. 4-3) is a custom-designed piezo-actuator-driven test rig with a load resolution of ±0.2mN and a displacement resolution of ±10nm. It comprises a piezoelectric actuator with position sensor, a load cell with temperature sensor, a height-adjustable alignment stage, and sample grips that are attached to the piezo-actuator and load cell. The control electronics include a waveform generator, an amplifier, a

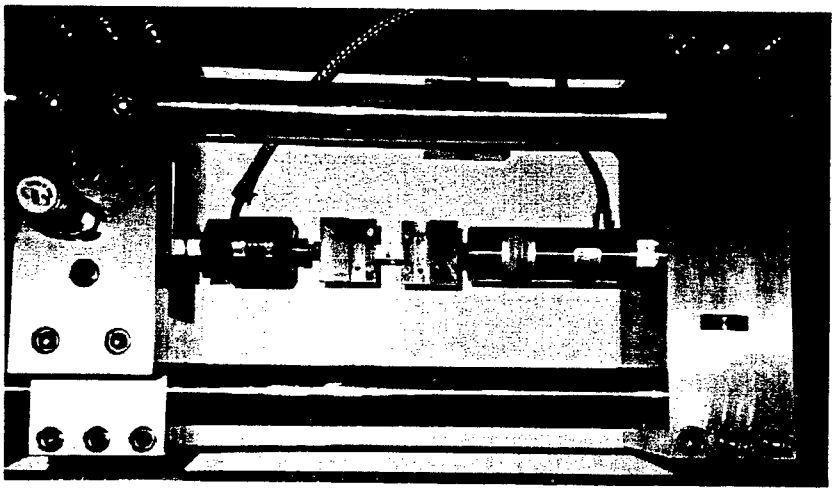

Figure 4-3: Top view of the main components of the custom-designed micromechanical testing system.

closed-loop piezo controller, a signal conditioner and an A/D board located in a control PC. Data acquisition is achieved by LabVIEW software. An optical microscope is mounted directly

overlooking the top of the sample for the purpose of height alignment as well as test monitoring. During testing, the system is kept in a thermally insulating box to eliminate possible effects that could be caused by temperature fluctuations, such as load cell drift or change in thermal expansion coefficients of the components of the system, which could lead to inaccurate measurement of stress or strain.

The load cell has a maximum measurement range of 44.5N and a load resolution of ±0.2mN. The piezo-actuator has a maximum measurement range of 60μm and a displacement resolution of ±10nm. The load to stress conversion is given by

$$Stress = \frac{Load}{Area} \tag{1}$$

where $Area = 50\mu m \times thickness$ is the cross-sectional area of the beam. The displacement to strain conversion is given by

$$Strain = \frac{GaugeDisplacement}{GaugeLength} \tag{2}$$

While we are only interested in the displacement of the gauge section of the specimen, other parts of the system along the stress direction also contribute to the total measured displacement. Strain calibration is done by taking into account the stiffness of the load cell, root section of the specimen, and other compliant parts of the system, in addition to the stiffness of the gauge section of the specimen.

4.1.2.2 Experimental Procedures

Prior to testing, the electronics are energized and left to thermally equilibrate. The load cell is pre-calibrated. The sample stage is adjusted under the optical microscope to eliminate the height difference between the two grips.

The test die is removed from the wafer by gently breaking the two silicon support bridges attached to the die corners, and is then placed on the grips with the beam side facing downward. It is then clamped in place by four screws, two on each side, with care taken to ensure even clamping throughout the process (by monitoring the load response on the LabVIEW screen). Upon securing the die onto the grips, the silicon supports on the two long sides of the die are cut with a hand-held rotary diamond saw. The Al micro beam is now free-standing between the two grips, where one end is attached to the load cell and the other to the piezo. Finally, the system is enclosed in the thermally insulating box and allowed to reach thermal equilibrium before actual testing (The temperature is maintained ±0.5 °C).

Tensile tests are performed by allowing the piezo control voltage to increase (i.e. to elongate the beam) monotonically, while the corresponding load (or stress) response of the beam and hence the stress vs. strain relation is recorded by LabVIEW. For a stress relaxation test, the beam is

quickly loaded to a certain strain first and then held at this constant strain while the resulting load (or stress) change is recorded against time elapsed. For cyclic testing, a triangular waveform is set on the piezo controller in order to cycle the piezo position at a constant displacement rate.

4.1.3 Results and Discussion

In this section, we will not review previously reported results.

4.1.3.1 Tensile Test of Pure Al and Al-2%Ti Micro Beams (2μm thick)

From the stress vs. strain curves (Fig. 4-4) of the pure Al and Al-2%Ti micro beams, we find Young's modulus to be about 60GPa, close to the value of 62GPa for bulk Al. The yield strength at 0.2% strain for the pure Al micro beams is about 120MPa. The yield strength at 0.2% strain for the Al-2%Ti micro beams is about 210MPa, about 75% higher than that of pure Al.

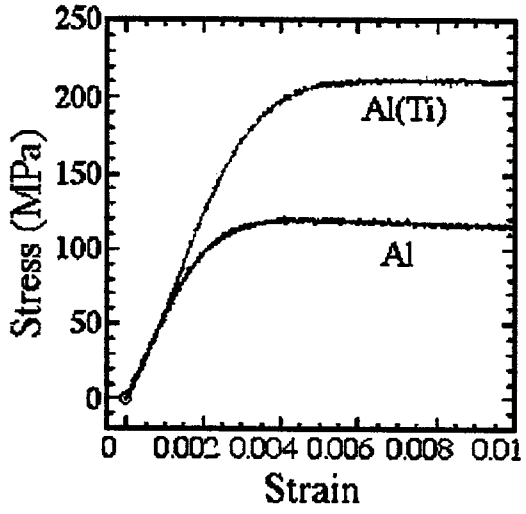

Figure 4-4: Stress vs. Strain curves of pure Al and Al-2%Ti micro beams (2μm thick).

This significant yield strength increase is due to Al_3Ti precipitates that have formed at grain boundaries. As described earlier in the sample preparation section, the multi-layer was annealed after sputter deposition. TEM studies on the cross-section of the Al/Ti multi-layer (Fig. 4-5) before and after the annealing indicate that Ti had reacted with Al to form Al_3Ti precipitates along the Al grain boundaries during the heat treatment. Al_3Ti has a much larger modulus than that of Al. It is known that hard precipitates (in this case, Al_3Ti) can block the motion of dislocations in a soft matrix (in this case, Al), and hence increase the amount of stress required to move these dislocations. In effect, this will result in higher yield strength in the Al-2%Ti micro beams than of those made from pure Al.

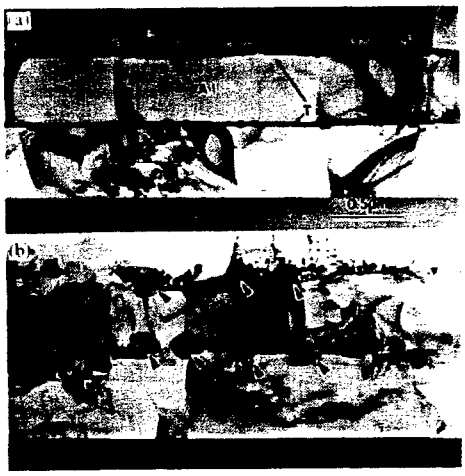

Figure 4-5: TEM cross-sectional view of (a) alternate layers of Ti and Al in the as-deposited Al/Ti multi-layer, (b) Al_3Ti precipitates formed at Al grain boundaries after annealing. (arrows are pointed to the locations of Al_3Ti precipitates)

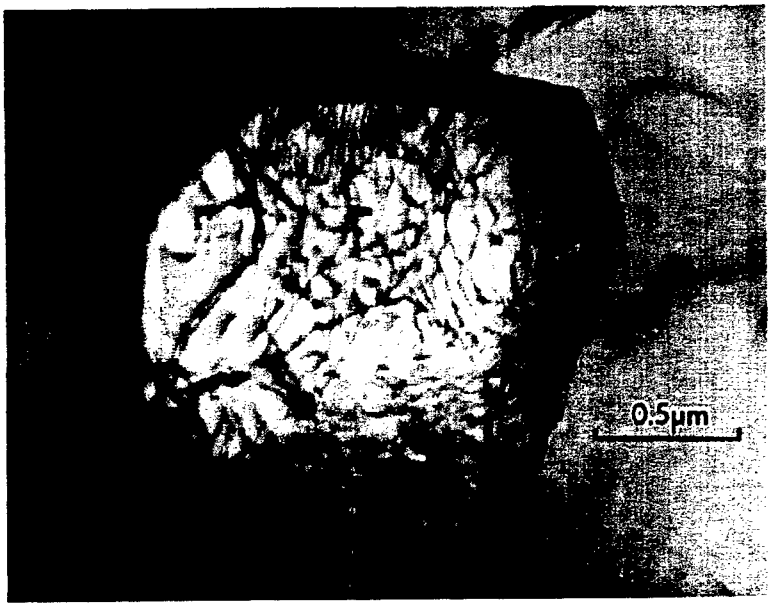

Figure 4-6: TEM bright filed image of a grain in a pure Al micro beam, showing dislocations after 0.4% strain.

Our TEM observation on the tested samples also showed a consistent result. The TEM samples were prepared from pure Al and Al-2%Ti beams after 0.4% strain of deformation. The bright field image of the pure Al sample (Fig. 4-6) under a two-beam condition ($\bar{g} = 111$) reveals many dislocations in the grain that are running rather straight. In the alloyed sample (Fig. 4-7), however, we see a different dislocation pattern, that is, dislocations in the alloyed beams appear

to zigzag or swirl around Al_3Ti precipitates, indicating that their motion was indeed blocked by the presence of the precipitates.

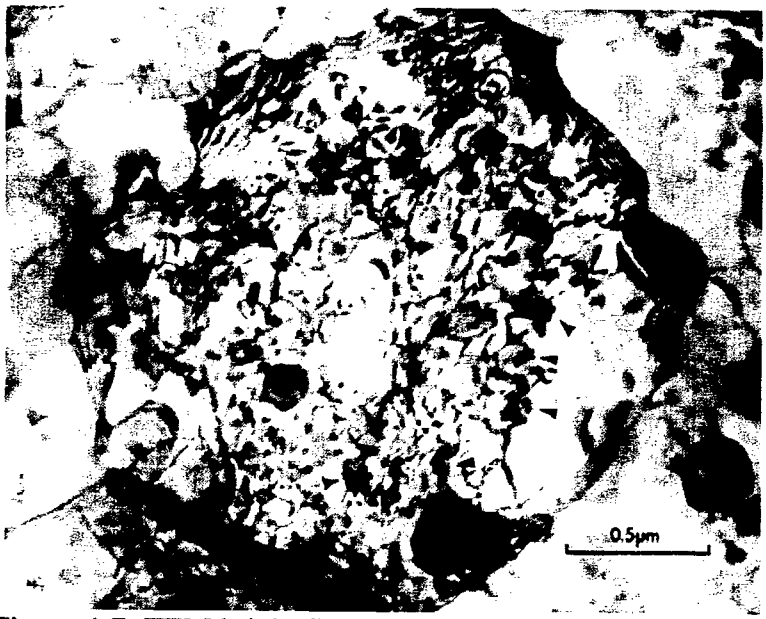

Figure 4-7: TEM bright field image of a grain in an Al-2%Ti micro beam, showing dislocations after 0.4% strain. (arrows are pointed to the locations of Al_3Ti precipitates)

We have therefore demonstrated that we can increase the yield strength of a pure Al free-standing thin film by alloying Al with Ti. In a RF switch application, where both high yield strength and high electrical conductivity are required, choosing Ti as an alloying material for building such MEMS structures offers advantages over pure Al.

4.1.3.2 Stress Relaxation Test of Pure Al and Al-2%Ti Micro Beams (2μm thick)

In stress relaxation tests, using a strain rate of 0.25μm/s, we first quickly loaded the samples to a strain of 1.2×10^{-3}. Then, holding the strain constant at this value, we recorded the corresponding load change for both the pure Al and the Al-2%Ti micro beams (Fig. 4-8).

For the pure Al micro beams, over a relaxation time of about 9min, the stress dropped from 50MPa to 22MPa, corresponding to a 56% relaxation from the original stress. For the Al-2%Ti micro beams, over the same period of relaxation time, the stress dropped from 50MPa to 44MPa, corresponding to a 16% relaxation.

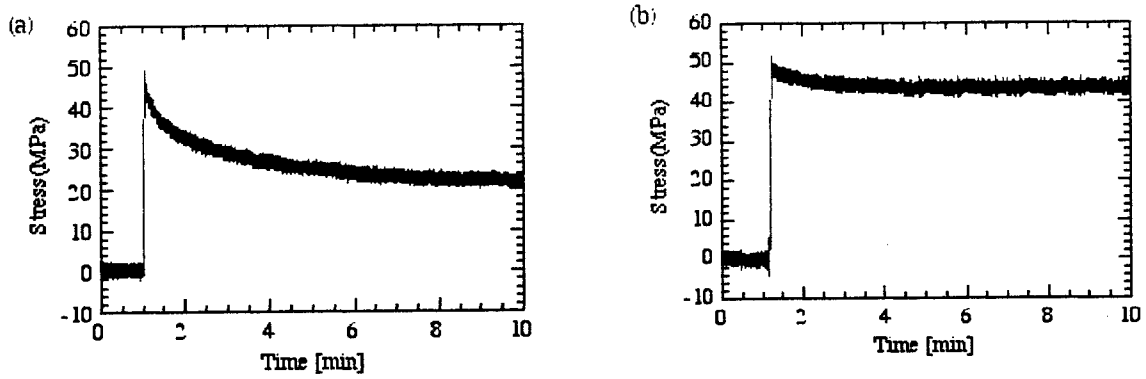

Figure 4-8: Stress relaxation of (a) pure Al, (b) Al-2%Ti micro beams (both 2μm thick).

Stress relaxation has been widely investigated for bulk materials as well as thin films on substrates. Those studies have found that grain boundary sliding is responsible for stress relaxation. However, the amount of stress relaxation from those studies was only a few percent, whereas we found more than 50% for our Al micro beams over the same time period. We have eliminated the possibility of test instrument errors and suggest that grain boundary sliding also accounts for relaxation in free-standing thin films. Qualitatively speaking, we would expect a free-standing thin film to have more grain boundary sliding taking place than a bulk material or a thin film on substrate, again because its top and bottom surfaces are unconstrained. Therefore, the amount of relaxation could be very large compared to bulk, which explains why the pure Al beams exhibit more than 50% of stress relaxation.

In the case of the Al-2%Ti micro beams, we see that the amount of relaxation is significantly less than that of the pure Al. This is probably due to the Al_3Ti precipitates formed at Al grain boundaries that hinder the grain boundary sliding, thereby decreasing the amount of relaxation compared to the pure Al.

Since our stress relaxation tests were carried out in a stress range below 50MPa, i.e. in the elastic regime, we can attribute the stress relaxation to anelasticity. We can, to first order, model the system as being a spring (E_∞) in parallel with a combination of a spring (E) and a dashpot (η) in series. For a constant strain of ε_0, the relaxed stress is a function of time given by:

$$\sigma(t) = \varepsilon_0 \left[E_\infty + E \cdot \exp\left(-\frac{t}{\tau}\right) \right] \qquad (3)$$

$$\text{where } \varepsilon_0 = \frac{\sigma_{initial}}{E_\infty + E} = \frac{\sigma_{final}}{E_\infty}, \text{ and } \tau = \frac{\eta}{E}$$

Since the elastic moduli for our pure Al and Al-2%Ti micro beams are nearly the same value, the difference in relaxation time, τ, is therefore directly related to η, the damping factor. As we can

imagine, because the Al_3Ti precipitates formed at Al grain boundaries, η is larger in value for the Al-2%Ti micro beams. Consequently, the relaxation time, τ, is longer for the Al-2%Ti micro beams, which again explains why the amount of relaxation in the same time period for the pure Al case is larger than for the Al-2%Ti case.

Unfortunately, this simple model could not fit our experimental data very well, and we have therefore proposed a two-Maxwell-element anelastic model, which describes the system as:

$$\sigma(t-t_0)=\varepsilon_0\left[E_\infty+E_1\exp\left(-\frac{t-t_0}{\tau_1}\right)+E_2\exp\left(-\frac{t-t_0}{\tau_2}\right)\right] \qquad (4)$$

$$\text{where } \tau_i=\frac{\eta_i}{E_i}.$$

With this analytical formula, we get a better fit to our experimental data. Our on going study is to investigate different data sets and propose a second mechanism in addition to the grain boundary sliding mechanism.

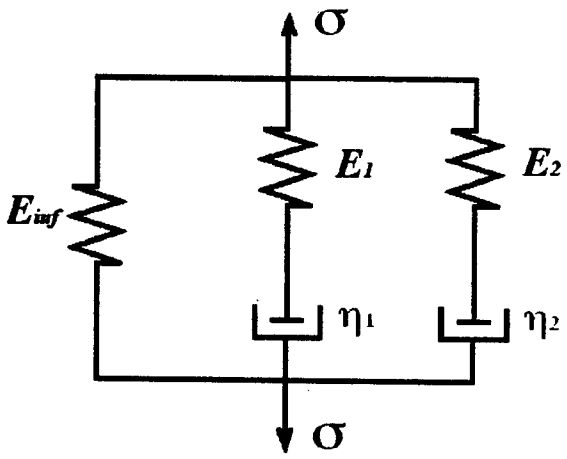

Figure 4-9: Two-Maxwell-element anelastic model.

4.1.3.3 Grain Size Study on Pure Al (2μm thick)

Stress vs. strain curves of pure Al micro beams annealed at different temperatures (Fig. 4-10) show that as annealing temperature increases, yield strength decreases while ductility increases. The heat-treated samples were each annealed for 1hr in a nitrogen ambient. Corresponding TEM micrographs (Fig. 4-11) revealed that grain sizes increase with annealing temperature. Hence, the result agrees with the Hall-Petch theory on conventional, bulk materials.

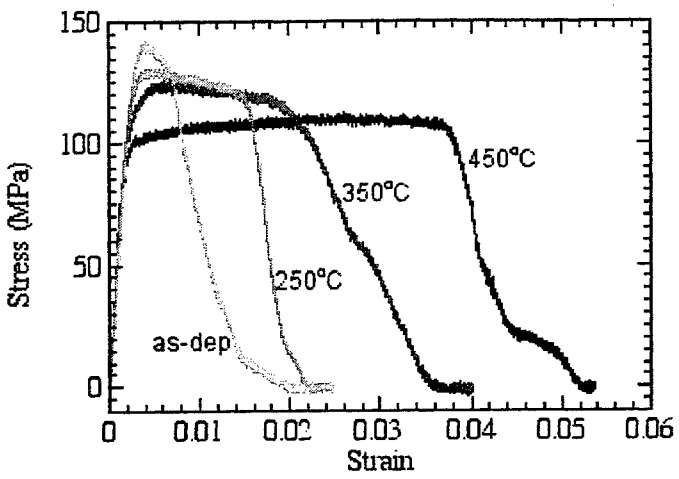

Figure 4-10: Stress vs. strain curves of pure Al micro beams at different annealing temperatures.

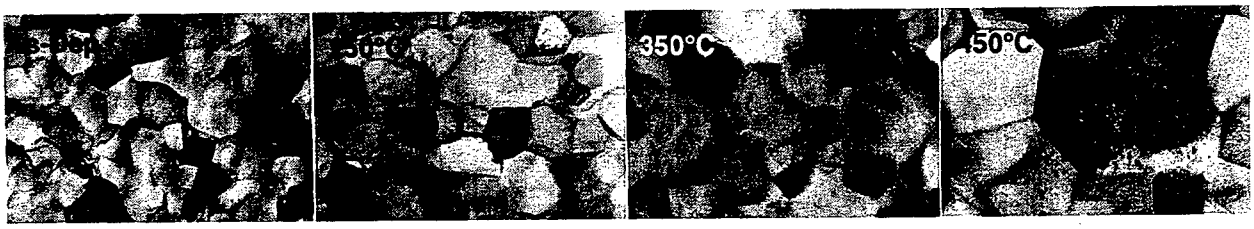

Figure 4-11: TEM micrographs showing grain size increase as increasing annealing temperature.

4.1.3.4 Inhomogeneous Deformation in Pure Al (2μm thick)

TEM studies revealed inhomogeneous deformation (Fig. 4-12) occurring for the as-deposited, 250 °C and 350 °C annealed samples, but not for the 450 °C fully annealed samples. Inhomogeneous deformation occurs in grains larger in sizes from their neighboring grains. Local thinning (i.e. necking) was observed, corresponding to high contrast in TEM images. Dislocation pileup at grain boundaries of the grains that have undergone inhomogeneous deformation was also observed. To circumvent inhomogeneous deformation, which may be undesirable in a RF switch application, we propose fully annealing. Although this will result in a slightly lower yield strength, we can compensate the yield strength decrease by alloying Al with Ti as described earlier.

Figure 4-12: TEM bright field images showing inhomogeneous deformation (local thinning) and dislocation pileup at grain boundaries.

4.1.3.5 Preliminary Results on Al/Ti co-Sputtered Films(1μm thick)

On-going work has been directed at studying Al-Ti co-sputtered thin films of different Ti concentrations and different annealing temperature combinations (Fig. 4-13 and 4-14).

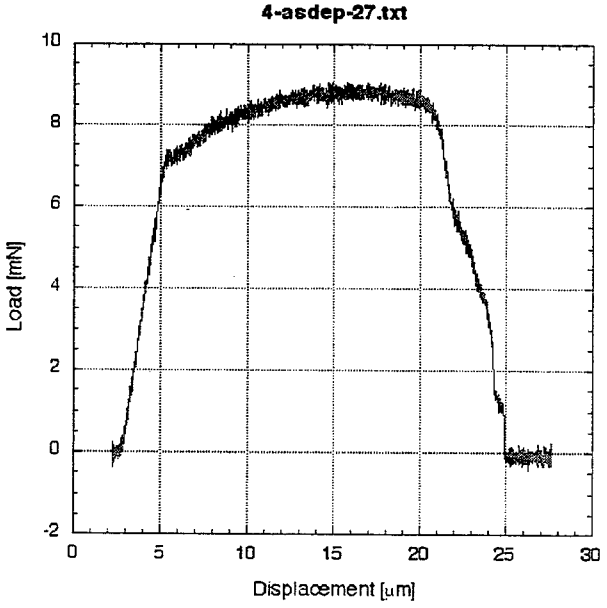

Figure 4-13: Load vs. displacement of Al-1.5%Ti, as-deposited.

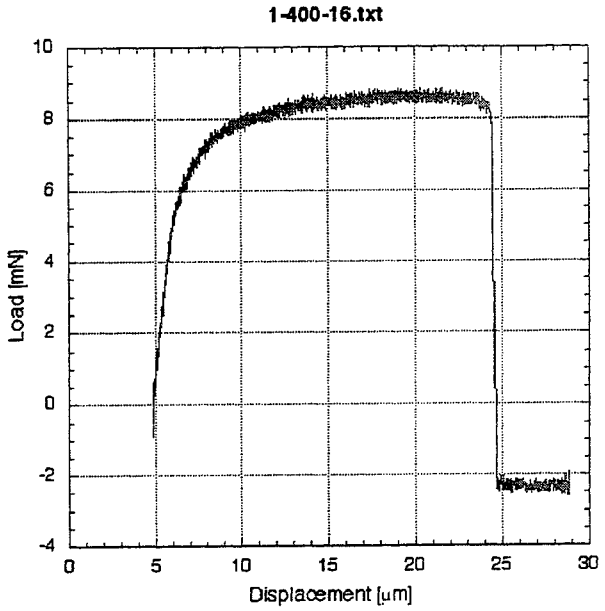

Figure 4-14: Load vs. displacement of Al-1.5%Ti, 400 °C annealed.

4. 2 In-Situ Stress Monitoring

Authors: Ping Zhang, Prof. John C. Bravman

In thin films, especially bi-layer or multi-layer thin films used for MEMS applications, film stress is a key issue to consider. High levels of stress through a film, and stress gradients across a film, may lead to device failure, while stress variations across a wafer may limit the uniformity and/or yield of MEMS devices. While many ex-situ film stress measurement techniques have been developed, in-situ stress monitoring during film deposition remains largely unexplored, especially for films deposited in production-grade equipment. In-situ monitoring will provide valuable information on the evolution and distribution of stress within a film. This should enable deposition conditions to be optimized in order to minimize stress and thus improve device performance.

4.2.1 Tunneling Sensor and Initial Modeling

The in-situ stress monitoring device that we have been developing employs a micromachined tunneling sensor with an external feedback control circuitry (Fig. 4-15). The tunneling sensor comprises of two wafer levels. The top Membrane-Wafer level has a micromachined deflection membrane ($2mm \times 2mm \times 0.5\mu m$) made of low stress silicon nitride, gold coated on its backside to form the membrane-electrode; the thin film of interest is deposited on the front side. The bottom Tip-Wafer level has a micromachined tunneling tip set in the center of a shallow square pit, where the tip and its surroundings are coated with gold to form the tip-electrode and the deflection-electrode.

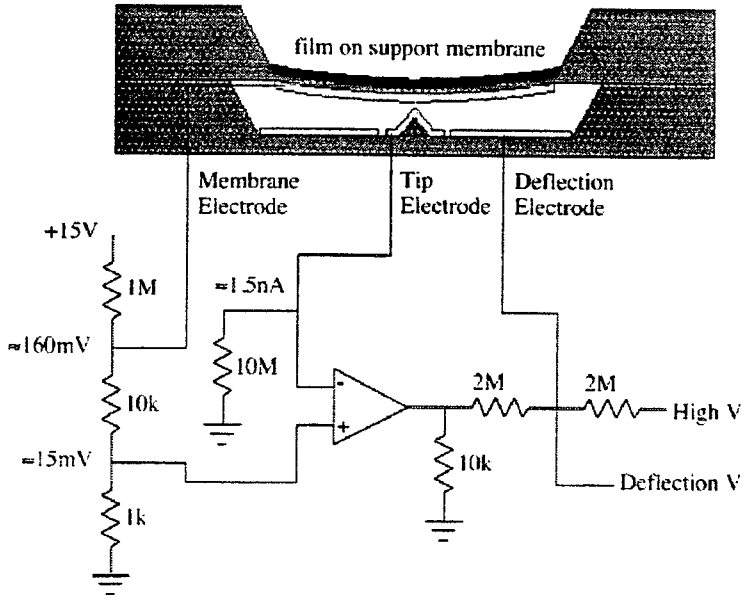

Figure 4-15: Side view schematic of tunneling stress measurement sensor and feedback circuitry.

During stress measurement, the deflection membrane plus thin film of interest is pulled down toward the bottom electrodes by the deflection voltage applied between the membrane-electrode and deflection-electrode. As the tip-to-membrane distance becomes as close as 10Å, significant electron tunneling occurs, corresponding to a tunneling current of about 1.5nA. The feedback control circuit ensures that this current is kept constant, meaning the tip-to-membrane distance is held constant (i.e. a constant center-deflection position). For a change in film stress, the defection voltage will have to change accordingly in order to maintain this tip-to-membrane position. The deflection voltage change is hence related to the film stress change by the following empirical formula:

$$\left(\frac{\varepsilon_0 a^4}{2d^2}\right) V_D^2 = (3.04ta^2h)\sigma + (1.83tEh^3) \qquad (5)$$

where
- V_D = the deflection voltage
- σ = stress
- ε_0 = permittivity of air
- d = distance between the membrane and deflection electrodes
- t = total thickness of the deflection membrane and the deposited thin film
- h = center deflection of the membrane
- a = half the side length of the square membrane
- E = average Young's Modulus

4.2.2 Stress Monitoring Device and Ex-Situ Stress Measurement Results

Ex-situ stress measurements were performed on the stress monitoring devices modified from some Infrared Radiation Detectors, which also employ the tunneling sensor part, but with the Absorber-Wafer level removed. To form the stress monitoring device (Fig. 4-16), the tunneling sensor is wire-bonded and packaged and plugged onto a proto broad built with feedback circuitry.

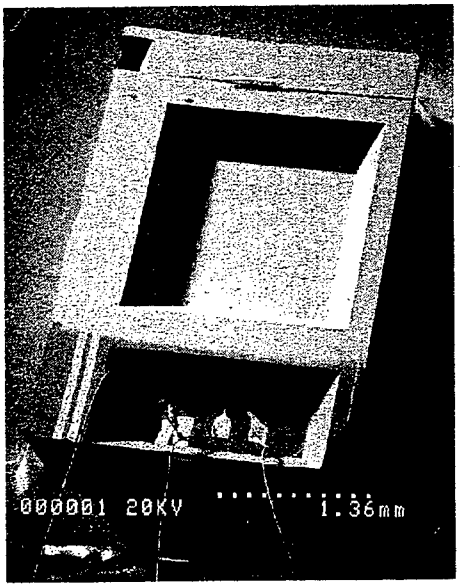

Figure 4-16: Wire-bonded and packaged stress monitoring device.

We sputter deposited Ta onto the deflection membrane and found from tunneling tests that the deflection voltage changed from 48.5V to 59.7V, before and after the Ta deposition. The +11.2V of voltage change corresponds to a stress change of about 0.4GPa, tensile, according to the initial modeling (Fig. 4-17). This stress change agreed with the stress calibrated by Wafer Curvature measurements on blanket Ta films of about 0.5-1GPa.

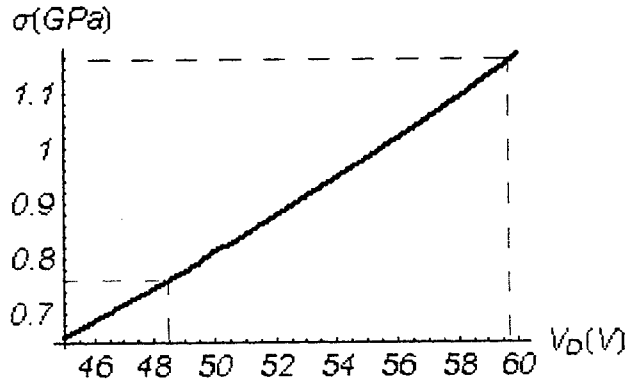

Figure 4-17: Stress vs. deflection voltage curve modeled by equation (5).

4.2.3 Fabrication of Dedicated Stress Monitoring Sensor

The fabrication of dedicated stress monitoring sensors uses a set of 7 masks on two wafer levels. There are 302 dies per wafer batch. Details are described in [5]. Unfortunately, processing issues primarily involving the definition of the tips during wet etch and the wafer-scale bonding and dicing at the end of the processing resulted in almost zero yield. Attempts were made to solve the problems.

4.2.4 ABAQUS Modeling

Using ABAQUS, we have modeled the deflection membrane/film composite behavior under an applied electrostatic force (Fig. 4-18). Both 3D element (C3D20R) and shell elements (S4R5, S4R8, S4R9) were selected, and results from the two were able to converge. Boundary conditions and initial conditions were also taken into account. Simulation data on center deflection vs. deflection voltage (Fig. 4-19), deflection voltage vs. initial stress (Fig. 4-20), and deflection voltage vs. film thickness (Fig. 4-21) were obtained.

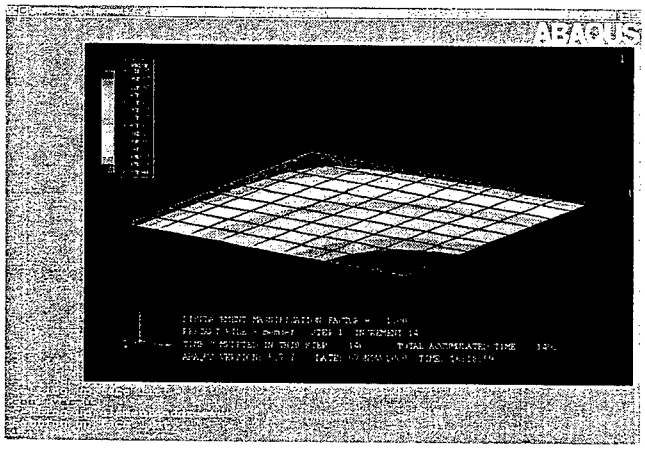

Figure 4-18: ABAQUS modeling of 1/4 membrane, showing center deflection.

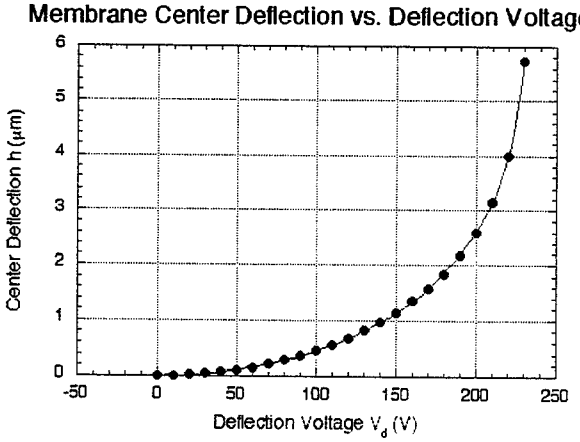

Figure 4-19: ABAQUS modeling result on membrane center deflection vs. deflection voltage (actual sensor).

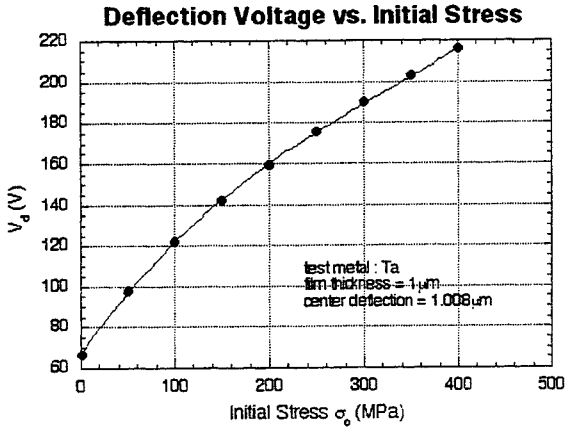

Figure 4-20: ABAQUS modeling result on deflection voltage vs. initial stress (sensor assuming 1μm of center deflection).

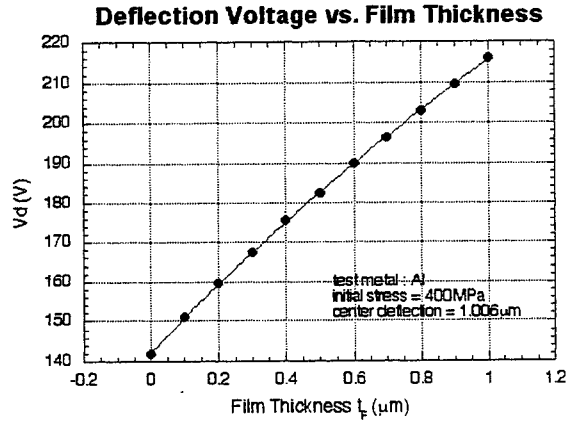

Figure 4-21: ABAQUS modeling result on deflection voltage vs. film thickness(sensor assuming 1μm of center deflection).

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APPENDIX I - LIST OF PUBLICATIONS

PhD Theses:

Edward Keat Leem Chan, "Characterization and Modeling of Electrostatically Actuated Polysilicon Micromechanical Devices," Stanford University PhD Thesis, November, 1999.

Guido Cornella, "Monotonic and Cyclic Testing of Thin Film Materials for MEMS Applications," Stanford University PhD Thesis, July, 1999.

Kenneth Honer, "Surface Micromachining Techniques for Integrated Microsystems," Stanford University PhD Thesis, January, 2001.

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E. K. Chan, K. Garikipati, Z. K. Hsiau, R. W. Dutton, "Characterization of electrostatically-actuated beams through capacitance-voltage measurements and simulations", Modeling and Simulation of Microsystems (MSM), Santa Clara, April 1998, pp. 180-5.

E. K. Chan, R. W. Dutton, "Effects of capacitors, resistors and residual charges on the static and dynamic performance of electrostatically-actuated devices," SPIE Symposium on Design, Test and Microfabrication of MEMS/MOEMS, Paris, March 1999.

E. K. Chan, K. Garikipati, R. W. Dutton, "Complete characterization of electrostatically-actuated beams including effects of multiple discontinuities and buckling," Modeling and Simulation of Microsystems (MSM), Puerto Rico, April 1999.

E. K. Chan, R. W. Dutton, "Effect of surface properties on the effective electrical gap of electrostatically actuated micromechanical devices operating in contact," Modeling and Simulation of Microsystems (MSM), San Diego, March 2000.

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APPENDIX II – REPRINTS OF SELECTED PAPERS

E. K. Chan, R. W. Dutton, "Effects of capacitors, resistors and residual charges on the static and dynamic performance of electrostatically-actuated devices," SPIE Symposium on Design, Test and Microfabrication of MEMS/MOEMS, Paris, March 1999.

E. K. Chan, K. Garikipati, R. W. Dutton, "Complete characterization of electrostatically-actuated beams including effects of multiple discontinuities and buckling," Modeling and Simulation of Microsystems (MSM), Puerto Rico, April 1999.

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Effects of capacitors, resistors and residual charge on the static and dynamic performance of electrostatically-actuated devices

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ABSTRACT

The important practical and realistic design issues of an electrostatic actuator/positioner with full-gap travel are discussed. Analytic expressions and numerical simulations show that parasitic capacitances, and non-uniform deformation in two and three dimensions influence the range of travel of an electrostatic positioner stabilized by the addition of a series capacitor. The effects of residual charge on electrostatically-actuated devices are described. The dynamic stepping characteristics of the positioner under compressible squeeze-film damping and resistive damping are compared. The physical descriptions of devices being fabricated in the MUMPs process are presented along with 3D simulation results that demonstrate viability.

Keywords: electromechanical, full-gap travel, stable, folded capacitor, floating electrode, shielded tether

1. INTRODUCTION

Electrostatically-actuated devices are widely used in microelectromechanical systems as switches [1] and resonators [2], and to extract material properties [3]. A typical device of this nature consists of a movable electrode suspended over a fixed electrode (Fig. 1a). An electric field imposed by applying a voltage between the electrodes actuates the movable electrode towards the fixed electrode. At voltages above a critical voltage known as the "pull-in voltage", the movable electrode collapses onto the fixed electrode. This restricted range of stable travel – about one-third of the initial gap – limits the effectiveness of electrostatic actuators as analog positioners. Several methods to extend the usable range of travel have been proposed such as employing "leveraged bending" [4], closed-loop voltage control [5], and series feedback capacitance [6].

The practical and realistic issues involved in designing a full-gap positioner by adding a capacitor in series with the electrostatic actuator – which is essentially a variable capacitor – to stabilize the actuator are presented in detail in subsequent sections. It is shown that parasitic elements inherent in fabricated devices, and any deviation from ideal 1D behavior limit the stable travel range. Residual charge that can accumulate in dielectrics and electrically-isolated nodes cause a voltage offset in this positioner. The stepping characteristics of this actuator/positioner under compressible squeeze-film damping and resistive damping are compared. Over-stabilization speeds up rise times without increasing settling times. Finally, the physical design of an electrostatic positioner, employing a novel floating electrode, that is currently being fabricated in the MUMPs process (MUMPs) [7] of the Microelectronics Center of North Carolina (MCNC) is described. This device which we call a "folded capacitor" actuator incorporating shielded tethers meets the design requirements for full-gap positioning.

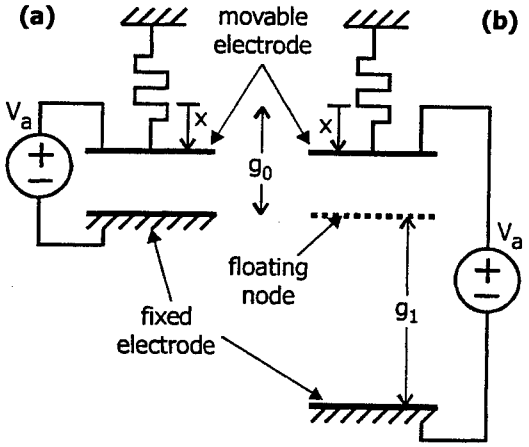

Fig. 1. (a) Schematic representation of conventional electrostatically-actuated device consisting of a movable electrode suspended over a fixed electrode. (b) Schematic representation of electrostatic positioner with series capacitor stabilization. The series capacitor increases the total effective gap between the voltage-driven electrodes. The floating node partitions the gap into the two capacitors -- the actuator and series capacitor..

2. BEHAVIOR OF CONVENTIONAL ACTUATOR

Fig. 1a is a schematic representation of a typical electrostatically-actuated device consisting of a movable top electrode suspended over a fixed bottom electrode. An electrostatic force set up by applying a voltage between the top and bottom electrodes pulls the top electrode towards the bottom. Considering an ideal one-dimensional (1D) system with electrodes of unit area, the equilibrium position of the movable electrode is determined by equating a mechanical restoring force of

$$F_m = -kx \tag{2.1}$$

with an attractive electrostatic force of

$$F_e = \frac{\varepsilon V_a^{\,2}}{2(g_0 - x)^2} \tag{2.2}$$

where k is the mechanical spring constant, x is the displacement of the top electrode, ε is the dielectric permittivity of the region between the electrodes, V_a is the applied voltage, and g_0 is the initial (unactuated) gap between the electrodes. Analytic calculations show that beyond

$$V_a = \sqrt{\frac{8kg_0^{\,3}}{27\varepsilon}} \tag{2.3}$$

corresponding to a displacement of

$$x = \frac{1}{3}g_0 \tag{2.4}$$

there is no equilibrium position for the top electrode, which hence collapses onto the bottom electrode. Therefore, the stable range of travel is limited.

3. SERIES CAPACITOR FEEDBACK

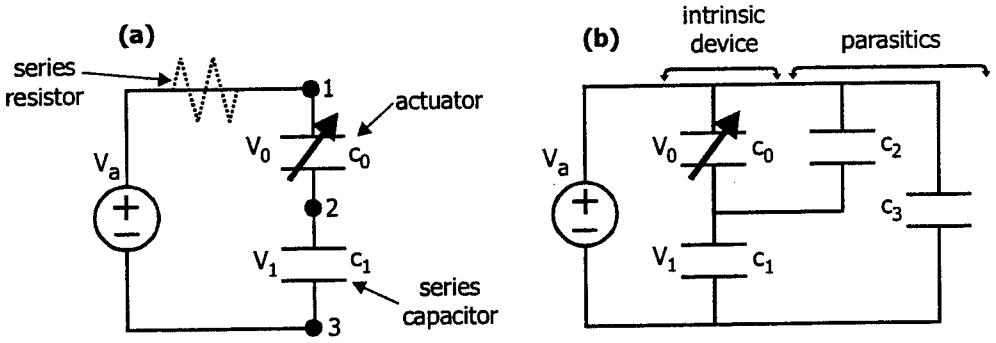

Fig. 2. (a) Circuit diagram of stabilized electrostatic positioner. Voltage across the actuator is determined by the capacitive voltage divider. Series resistor can be included to provide resistive damping. (b) Circuit diagram including parasitic capacitances. Voltage across actuator is given by Eq. 3.4. Capacitor c_3 only affects dynamic performance.

3.1 Ideal behavior

A properly-sized capacitor added in series with the conventional actuator will adjust the actual voltage between the electrodes of the actuator so that the movable electrode can traverse the entire gap stably [6]. The capacitive voltage divider of Fig. 2a suggests that the total applied voltage, V_a, is divided between the actuator and the series capacitor such that

$$V_0 = \frac{c_1}{c_0 + c_1} V_a . \tag{3.1}$$

Since the capacitance of the actuator, c_0, increases as the movable electrode approaches the fixed electrode, the fraction of the applied voltage across the actuator actually decreases as the applied voltage is increased. When the displacement extends beyond one-third of the gap, the rapid increase in capacitance provides the negative feedback necessary to stabilize the actuator so it can traverse the entire gap stably.

This behavior can equivalently and more easily be understood as actuating the movable electrode through the stable range of an actuator with a larger effective initial gap, $g_0 + g_1$, as shown in Fig. 1b. The series capacitor of Fig. 2a serves to increase the total effective gap of the actuator such that the movable electrode moves only through the stable portion of the gap. A floating conductor inserted at the dotted line in Fig. 1b partitions the system into two capacitors in series without disturbing the field distributions. Since the stable range is one-third of the total effective gap, g_1 needs to be at least twice as large as g_0 to achieve stable full-gap travel. In terms of capacitances, this condition is

$$c_1 < \frac{c_0^i}{2} \tag{3.2}$$

where c_0^i is the initial actuator capacitance.

3.2 Effect of parasitics

Fig. 3 shows the cross-section of a typical electrostatically-actuated device fabricated in the MUMPs process. c_0 and c_1 are the intrinsic device capacitances whereas c_{p1}, c_{p2} and c_{p3} are parasitics. c_{p2} and c_{p3} are typically large because the dielectric layer is (electrically) thin. Depending on whether the substrate is grounded or left floating, the parasitic capacitances can be in parallel with either c_0 or c_1. The circuit of Fig. 2a can be generalized to that shown in Fig. 2b where c_1 now includes the parasitics in parallel with it. c_3 is not important to the static solution since it is driven directly by the voltage source, but it will affect dynamic performance.

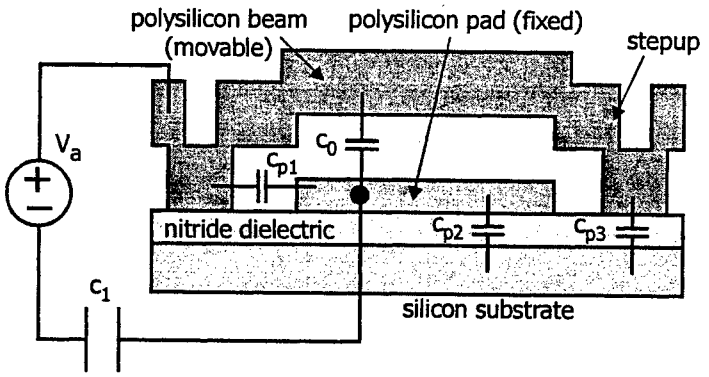

Fig. 3. Profile of typical electrostatically-actuated device fabricated in MUMPs. Parasitic capacitances to the substrate are typically large because the nitride is thin. Displacement is largest at the center of the beam. The length of the fixed bottom pad can be reduced to influence primarily the center portion of the beam thus approaching 1D behavior.

We now derive expressions describing the static behavior of the actuator in the presence of a series feedback capacitor and parasitic capacitors as depicted in Fig. 2b. Let

$$c_0 \propto \frac{1}{g_0 - x},\ c_1 \propto \frac{1}{ng_0} \text{ and } c_2 \propto \frac{1}{mg_0} \tag{3.3}$$

where m and n are positive constants. The voltage across c_0 is determined by the capacitive voltage divider to be

$$\begin{aligned} V_0 &= \frac{c_1}{c_0 + c_1 + c_2} V_a \\ &= \frac{m(g_0 - x)}{(m+n)(g_0 - x) + mng_0} V_a \end{aligned} \tag{3.4}$$

The sum of the electrostatic and mechanical forces gives the total equilibrium force on the movable electrode

$$F_t = -kx + \frac{\varepsilon}{2(g_0 - x)^2}\left[\frac{m(g_0 - x)}{(m+n)(g_0 - x) + mng_0} V_a\right]^2 = 0. \tag{3.5}$$

Differentiating this expression with respect to x to determine the point at which the equilibrium solution becomes unstable gives

$$x_{\max} = \frac{g_0}{3}\frac{m+n+mn}{m+n} \tag{3.6}$$

as the maximum stable displacement of the movable electrode as a function of m and n. In the limit as $m \to \infty$ (no parasitic fixed capacitor in parallel with c_0),

$$x_{\max} \to \frac{g_0}{3}(1+n) \tag{3.7}$$

implying that n should be larger than 2 for full-gap travel ($x_{\max} \to g_0$) as noted previously. As $n \to \infty$ (infinitely small series capacitor for maximum stability),

$$x_{\max} \to \frac{g_0}{3}(1+m) \tag{3.8}$$

implying that c_2 must be no larger than $\frac{c_0^i}{2}$ if full-gap travel is to be achieved. Thus the electrostatic positioner must have well-controlled capacitances and parasitics.

4. DEFORMATION IN TWO-DIMENSIONS

When the beam in Fig. 3 deforms, the displacement of the center portion is largest whereas the portions near the stepup supports hardly move at all. This 2D non-uniform behavior is a subtle but significant source of "parasitic" capacitance, c_2, in parallel with c_0. The 2D beam/capacitor can be modeled as the sum, of two 1D capacitances – a variable capacitor in parallel with a fixed capacitor as shown in Fig. 4. This is expressed as

$$c = c_0 + c_2 \propto \frac{1-q}{g_0 - x} + \frac{q}{g_0} \tag{4.1}$$

where c_0 and c_2 represent the same elements as in Fig. 2b, and q is a proper fraction that increases as x, the center displacement, increases as will be shown later. The larger the value of q, the larger the effect of the parasitic.

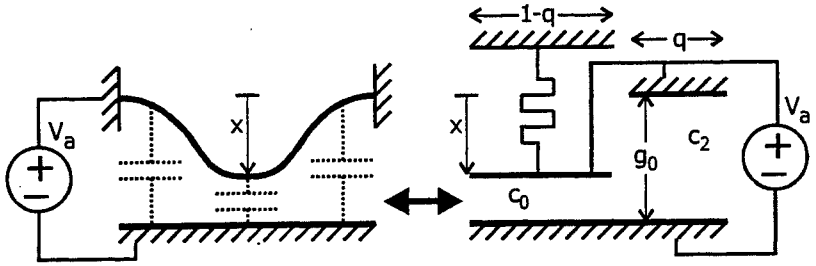

Fig. 4. Ideal 2D electrostatically-actuated beam with its lumped-element representation that is parameterized by the center displacement of the beam, and the fraction "q" of the beam that behaves like a parasitic parallel fixed capacitance.

Fig. 5a shows the normalized simulated capacitances of several 2D 400μm-long electrostatically-actuated beams, with nominal MUMPs thicknesses, as functions of the displacement of the beam center. The coupled electromechanical simulations were performed in Matlab [8]. As shown, the capacitance of a 2D device increases more slowly as a function of center displacement than a 1D device. Numerical experiments show that the normalized capacitance is relatively insensitive to beam length and residual stress. As the fixed bottom electrode on the left-hand side of Fig. 4 is reduced in length (as a percentage of the upper beam length), the 2D device approaches 1D-like behavior because the deformation is more uniform over the more limited center region.

q is computed from the capacitance-displacement curves of Fig. 5a and plotted in Fig. 5b as a function of center displacement, x, and parameterized by bottom electrode length. The shorter the bottom electrode, the more 1D-like the behavior, hence the smaller the value of q. q increases as the displacement increases because the smaller gap amplifies the

effect of non-uniform displacements. Since c_2 must be less than one-half the initial c_0 for full-gap actuation as shown in Section 3, q must satisfy

$$\frac{q}{g_0} < \frac{1-q}{2g_0} \Leftrightarrow q < \frac{1}{3}. \tag{4.2}$$

The displacement at the intersection of the $q = 1/3$ line with the q-displacement curve indicates the maximum achievable stable travel. This assumes that the mechanical restoring force is still linear with displacement, which is not strictly true due to stress-stiffening effects. Nonlinear stress-stiffening actually increases the range of stable travel, even without capacitive stabilization, to about one-half the initial gap, up from the one-third (Eq. 2.4) of the linear case. Thus all the 2D devices shown in Fig. 5b are stable up to about 1μm of deflection. Beyond that, capacitive feedback can stabilize the device up until the increasing displacement causes $q > 1/3$. For example, for the device with a bottom electrode that is 30% of the upper electrode length, capacitive feedback will allow stable travel up to 1.8μm or 90% of the 2μm gap. This, however, assumes an infinitely small series feedback capacitor (see Eq. 3.8) – a larger capacitor will reduce the travel range. Clearly, 2D-like behavior must be avoided.

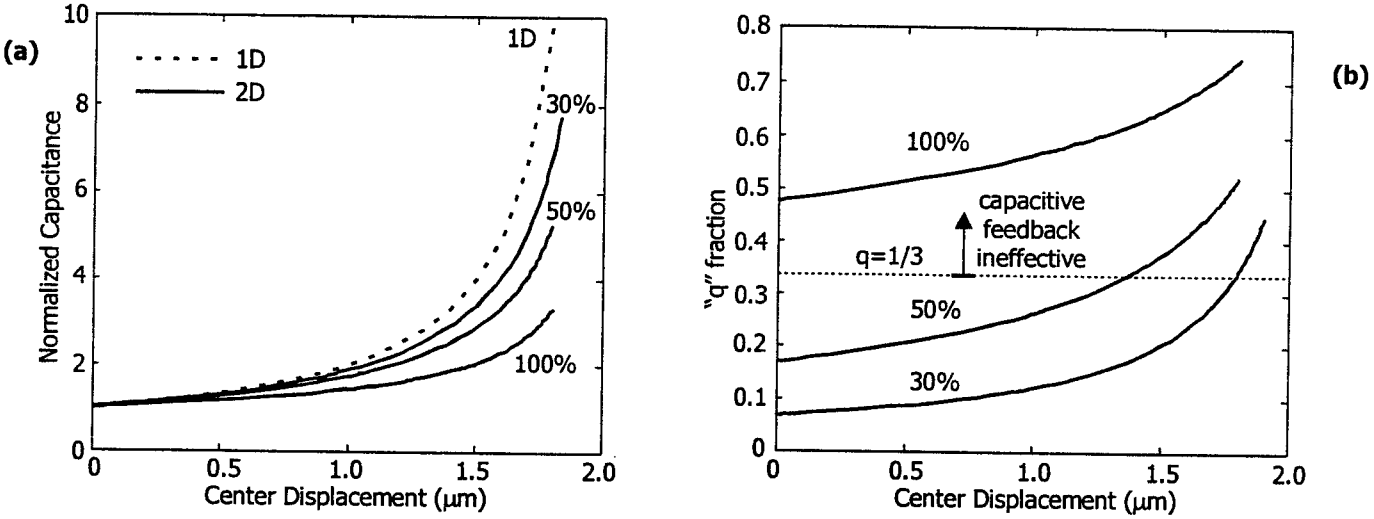

Fig. 5. (a) Normalized simulated capacitances of 2D 400μm-long electrostatically-actuated beams as functions of center displacement and parameterized by bottom electrode length (as a percentage of upper beam length). The increase in capacitance in the 2D case is always less than in 1D. As the fixed bottom electrode length is reduced from 100% of beam length to 30%, the capacitance variation approaches 1D behavior. (b) The fraction "q" of the 2D beam that behaves like a parasitic fixed capacitance in parallel with the variable capacitance. q increases with displacement because the decreasing gap accentuates the effect of non-uniform displacement along the length of the beam. The dotted line where q=1/3 is the boundary above which capacitive feedback is ineffective. Due to stress-stiffening, the center of the 2D beams can move almost 1 μm before pull-in occurs even without capacitive feedback.

Referring back to Fig. 1b, we see that in the 1D case, inserting a floating conductor into the gap at the dotted line does not perturb the electric field lines. When a 2D beam deforms non-uniformly, however, the beam center moves the most, concentrating electrostatic forces near the center. Inserting a floating conductor into the gap in this case will distort the electric field lines since the conductor will enforce a flat, horizontal equipotential which did not previously exist. The series capacitor no longer simply extends the effective gap and thus the effectiveness of capacitive feedback is limited. Designs to maintain 1D-like behavior are discussed in Section 7.

5. RESIDUAL CHARGE

Residual charge can accumulate in electrostatically-actuated devices containing electrically-isolated nodes or dielectric layers. Fig. 6 shows the effect of a sheet of charge inserted between two voltage-driven plates. Both trapped charge in a dielectric layer [3], or net charge on a floating node such as node 2 in Fig. 2a can be modeled by a sheet of charge. According to Gauss' Law, the charge sheet modifies the electric field on each side of the sheet to be

$$E_1 = \frac{V_a - \frac{d_2\rho}{\varepsilon}}{d_1}, \text{ and} \tag{5.1}$$

$$E_2 = \frac{V_a + \frac{(d_1 - d_2)\rho}{\varepsilon}}{d_1} \tag{5.2}$$

where ρ is the areal charge density of the charge sheet. For most electrostatically-actuated devices, the movable electrode is plate 1 in Fig. 6. In this case, the electric field, and hence the electrostatic force, is simply shifted by a voltage offset ($\frac{d_2\rho}{\varepsilon}$ in Eq. 5.1) which scales according to the amount of charge.

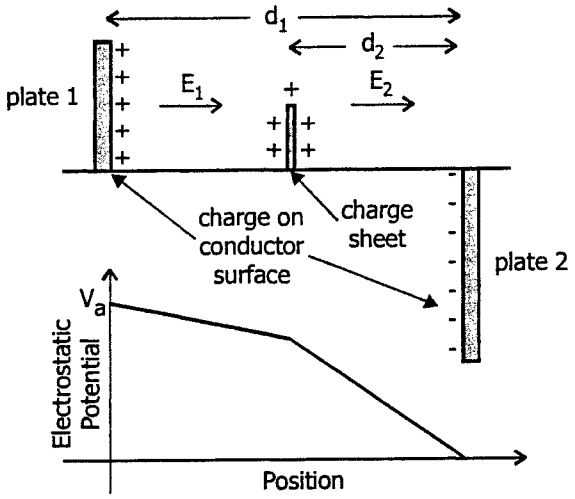

Fig. 6. Effect of residual charge, represented by a sheet of charge, on the electrostatics between two voltage-driven plates. The slope of the electrostatic potential changes abruptly at the position of the charge sheet.

If the electric field on both sides of the charge sheet act on movable electrodes, however, the effect is more complicated. Fig. 7a shows one such configuration where a precharged floating conductor inserted between two voltage-driven plates is free to move. The mechanical restoring force is still given by Eq. 2.1 but the electrostatic force – the product of charge and the average electric field – is now

$$F_e = \rho\left[\frac{V_a}{d_1} - \frac{\rho}{\varepsilon}\left(\frac{d_2 - x}{d_1} - \frac{1}{2}\right)\right]. \tag{5.3}$$

The first thing to note is that unless the floating conductor is precharged, the net electrostatic force on the conductor is zero. Secondly, in contrast to Eq. 2.2, this force is linear with voltage and displacement. By equating the electrostatic and mechanical forces, we find the equilibrium displacement to be

$$x = \frac{\frac{V_a}{d_1} - \frac{\rho}{\varepsilon}\left(\frac{d_2}{d_1} - \frac{1}{2}\right)}{\frac{k}{\rho} - \frac{\rho}{\varepsilon d_1}}. \tag{5.4}$$

Here, the charge scales not just the voltage offset but the displacement axis as well. Since the inverse-square behavior of Eq. 2.2 is absent, there is no abrupt pull-in effect and actuation is always stable, potentially allowing for stable and linear electrostatic actuation. Figs. 7b and 7c are the layout and cross-section of a proposed implementation of this linear actuator being fabricated in MUMPs. The POLY1 floating electrode is suspended by flexible tethers with meanders so that it can move easily within the gap. On the other hand, the POLY2 electrode is designed to be short to minimize its undesired deformation under electrostatic forces. The floating electrode is precharged by briefly connecting it to a voltage source. Like

the capacitively-stabilized actuator, the performance of this actuator is affected by parasitic capacitances. Good isolation of the floating conductor and matching electrode areas is critical for linearity. This, unfortunately, is difficult to achieve in MUMPs.

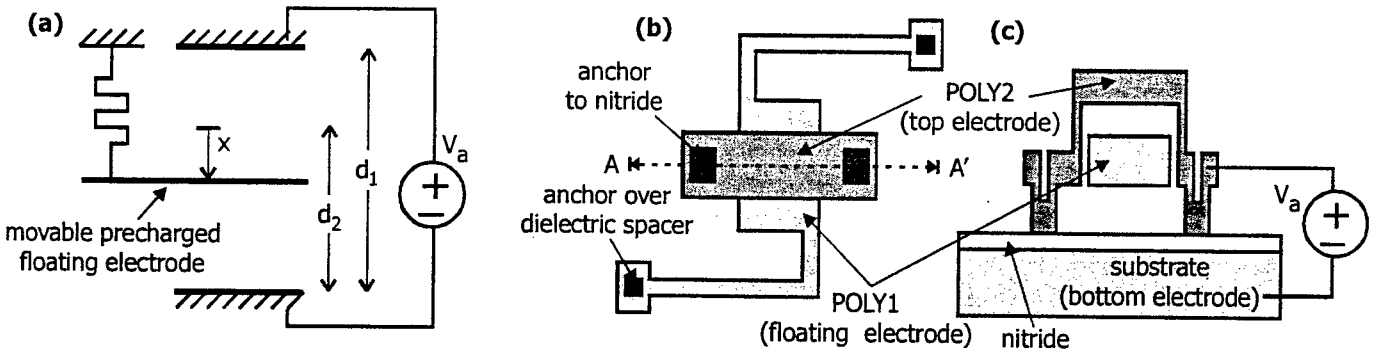

Fig. 7. Linear electrostatic actuator consisting of a movable precharged floating electrode suspended between two voltage-driven electrodes. Displacement is proportional to applied voltage and depends on precharge voltage. (a) Schematic representation. (b) Layout of proposed device being fabricated in MUMPs. The top POLY2 electrode is designed to be short so as not to deform easily. The POLY1 floating electrode, on the other hand, is suspended by flexible tethers so that it can be actuated. (c) Cross-section AA' corresponding to layout (b). Actuation voltage, V_a, is applied between substrate and POLY2 electrode. Precharge voltage is applied briefly to floating electrode.

6. DAMPING

A good positioner or actuator should be well-damped so that rise times are fast, settling times are short, and overshoots are small. The efficacy of the two common damping mechanisms for microelectromechanical devices – resistive damping and compressible squeeze-film damping – on stabilized electrostatic positioners are studied using 1D simulations. The simulation models used here are not calibrated to actual devices but serve to illustrate major damping characteristics. For conventional actuators (see Section 2), the only dynamic responses of interest are pull-in and release times since these devices are usually operated in on/off modes, and involve contact [8]. For analog positioners, however, the dynamic response from one position to another throughout the gap is of interest.

A resistor inserted in series with the voltage source in Fig. 2a will help damp out oscillatory behavior by dissipating energy when current flows. Fig. 8a is an example of the damped step responses of an ideal, 1D, critically-stabilized positioner ($c_1 = \frac{c_0^i}{2}$). The resistor damps out oscillations reasonably well for steps down from $x = 0$, especially for larger steps ($x > 0.5g_0$). The size of the resistor was chosen so that the overshoot for the $x = 0.9g_0$ step would not cause the movable electrode to make contact and possibly stick to the bottom electrode. The resistor performs poorly in damping out the oscillations stepping back up from $x = 0.9g_0$ to $x = 0.15g_0$. In fact, resistive damping alone can never damp out all the oscillations stepping back up all the way to $x = 0$ because the capacitors discharge fully leaving no voltage to drive current through the damping resistor. Hence resistive damping – simple and easy to adjust – is attractive primarily for operating the positioner in the $x > 0.5g_0$ range.

Compressible squeeze-film damping acts whenever the positioner is operated in air. It is more difficult to adjust – damping forces depend on air pressure and the geometry of the device. Fig. 8b shows the performance of the positioner under squeeze-film damping forces modeled by

$$F_d \propto \frac{dx/dt}{(g_0 - x + \lambda)^3} \tag{6.1}$$

where λ is approximately the mean free path for air [9]-[10]. In general, the larger steps (to $x \geq 0.75g_0$) are overdamped, with the approach to $x = 0.9g_0$ being almost asymptotic. This slow approach is probably overestimated by the simulation because Eq. 6.1 neglects the transition from spring-like behavior to incompressible viscous damping at lower actuation speeds. The damping at $x = 0.15g_0$ is generally much better than can be achieved with resistive damping.

Under both resistive and squeeze-film damping, the oscillations are difficult to damp out near $x = 0$. Increasing the damping forces will increase the rise time to $x = 0.9g_0$ significantly, especially for the squeeze-film damping case. Over-stabilizing the positioner i.e. making $c_1 << \frac{c_0^i}{2}$ improves the rise time for the larger steps while leaving settling times and overshoots roughly unchanged as shown in Fig. 8c. Decreasing c_1, to $\frac{c_0^i}{8}$ in this example, provides a more constant electrostatic driving force that is less dependent on the gap, especially as x approaches g_0, thus reducing asymptotic behavior. In the critically-stabilized case, the electrostatic force and the gap are more strongly interdependent and hence both approach static equilibrium asymptotically.

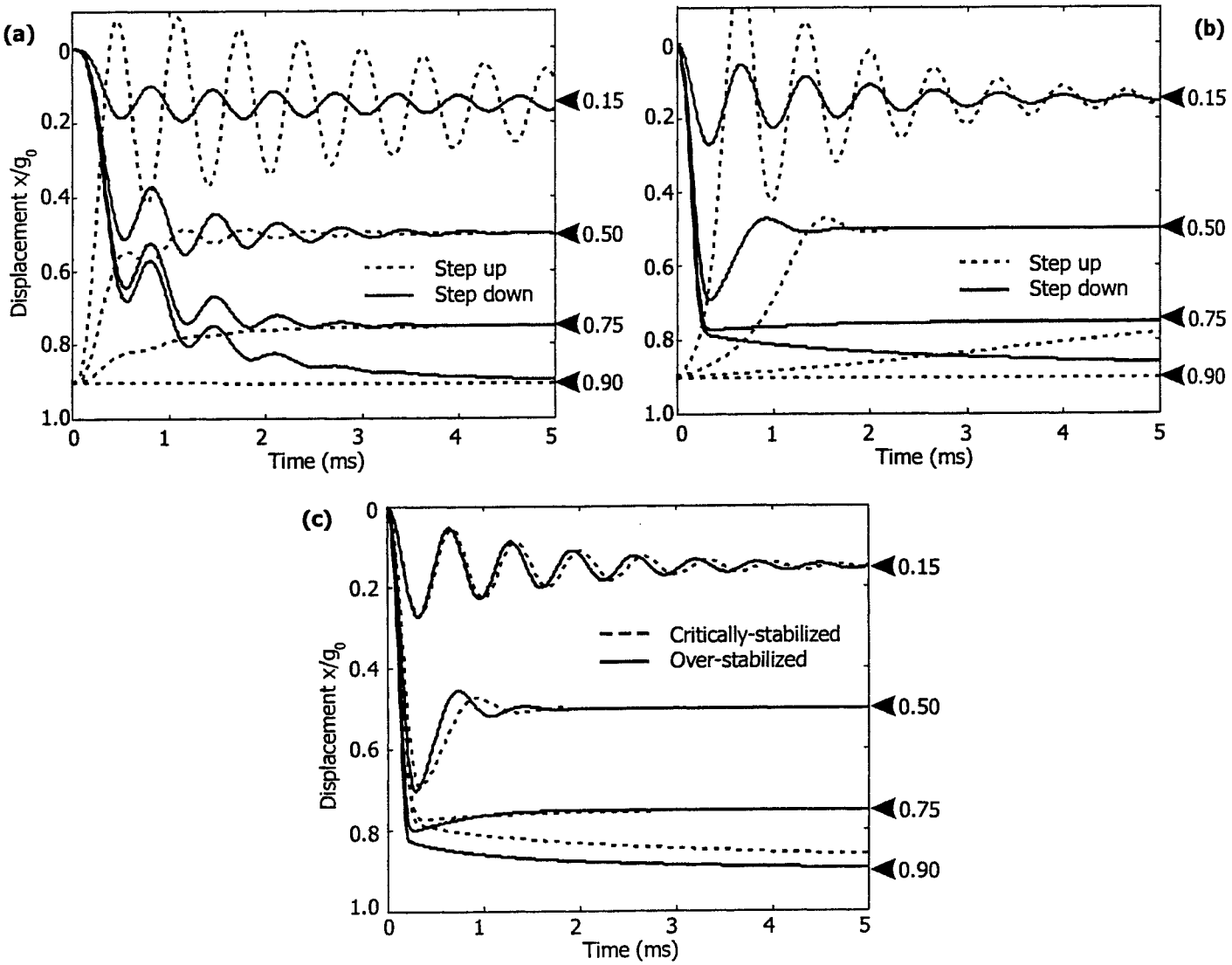

Fig. 8. (a) Step up and step down responses of critically-stabilized positioner under resistive damping. The response is slightly overdamped for steps down to $x>0.5g_0$ but underdamped for steps back up to $x=0.15g_0$. (b) Step up and step down responses of critically-stabilized positioner under compressible squeeze-film damping. The response is severely overdamped for large steps down. The damping at small deflections (near $x=0$) is better than can be achieved using resistive damping. (c) Step down responses of over-stabilized positioner under squeeze-film damping compared to critically-stabilized device. The rise time is faster especially towards $x=0.9g_0$ because the electrostatic force is less dependent on the changing gap. The damping for smaller steps is roughly unchanged.

7. PHYSICAL DESIGN

Fig. 9a shows the straightforward three-conductor-stack implementation of the electrostatic positioner. Fabricating this device would require a dielectric layer many times the thickness of the travel gap to maintain the proper $\frac{c_0^i}{c_1}$ ratio. This device cannot be realized in MUMPs. Figs. 9a to 9d conceptualize the transformation of the initial three-conductor-stack into an equivalent two-layer design more suitable for surface micromachining. First, the floating conductor/node is extended so that the top and bottom voltage-driven electrodes can be moved apart horizontally (Fig. 9b). Then the left-hand side is "folded over" as shown in Fig. 9c. Neglecting fringing fields, the electrostatic forces acting on the movable plate, which is now below the floating electrode, are exactly the same as before. Finally, the mechanical elements on the left-hand side are swapped so that the movable electrode is once again on the top. The movable and fixed portions of the floating electrode are connected electrically. The device of Fig. 9d, which we call a "folded capacitor", is functionally equivalent to the initial design but can now be implemented in MUMPs.

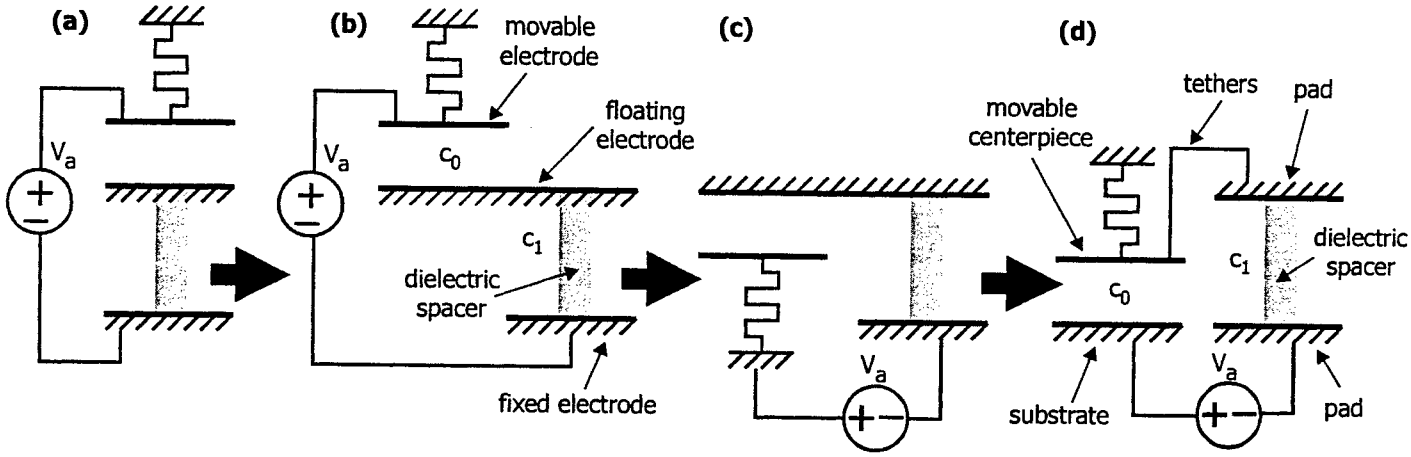

Fig. 9. Transformation of a three-conductor-stack implementation of the electrostatic positioner into a two-layer implementation that is readily fabricated in MUMPs. (a) Original three-conductor vertical stack. Capacitance ratio determined by thickness (gap) ratio. (b) Floating electrode is extended so that fixed and movable electrodes can be separated horizontally. (c) The left-hand side is "folded over" so that the movable electrode is now on the bottom. Electrical connections are all on the bottom. (d) While the electrical connections remain unchanged, the mechanical elements on the left-hand side are swapped so that the movable electrode is once again on the top. This configuration is functionally equivalent to the configuration in (a).

Fig. 10a is the profile of a design currently being fabricated at MCNC. The essential elements are labeled corresponding to Fig. 9d. The device consists of a nominally rigid centerpiece fabricated in POLY1 suspended by POLY2 tethers. A controlled HF etch of the sacrificial PSG creates dielectric spacers which form the capacitor c_1 and electrically-isolate the tethers and centerpiece leaving them floating. c_0 is the capacitance between the centerpiece and silicon substrate. The nitride layer prevents the shorting of the floating conductor to the silicon substrate. The POLY2 tethers are shielded from the substrate by the POLY1 centerpiece thus reducing associated parasitic capacitance. Fig. 10c is the plan view where the tethers have some meander to ensure that most of the deformation as the device is actuated occurs at the tethers leaving the centerpiece as flat as possible, mimicking 1D behavior. The flexures also provide stress relief to prevent buckling. This design, with very small parasitics and nominally flat parts, closely resembles the ideal of Fig. 9d. POLY2 is overlaid on the centerpiece to provide additional stiffness to keep the centerpiece flat. The tethers meet at the center of the POLY1 plate instead of remaining separated so that bending moments at the point of attachment to the centerpiece cancel out.

Designing for the desired $\frac{c_0^i}{c_1}$ ratio simply requires ratioing the area of the POLY1 centerpiece to the area of the POLY1 pads (attached to the PSG spacers) appropriately instead of varying layer thicknesses. The dielectric constant of the c_1 capacitors is some proportionate mixture of the dielectric constants of air and PSG that depends on the duration of the sacrificial etch. Fig. 10b is an alternate design that does not require a controlled HF etch. In this case, the nitride serves as the dielectric spacer (forming c_1) and a POLY0 pad is placed under the centerpiece (forming c_0).

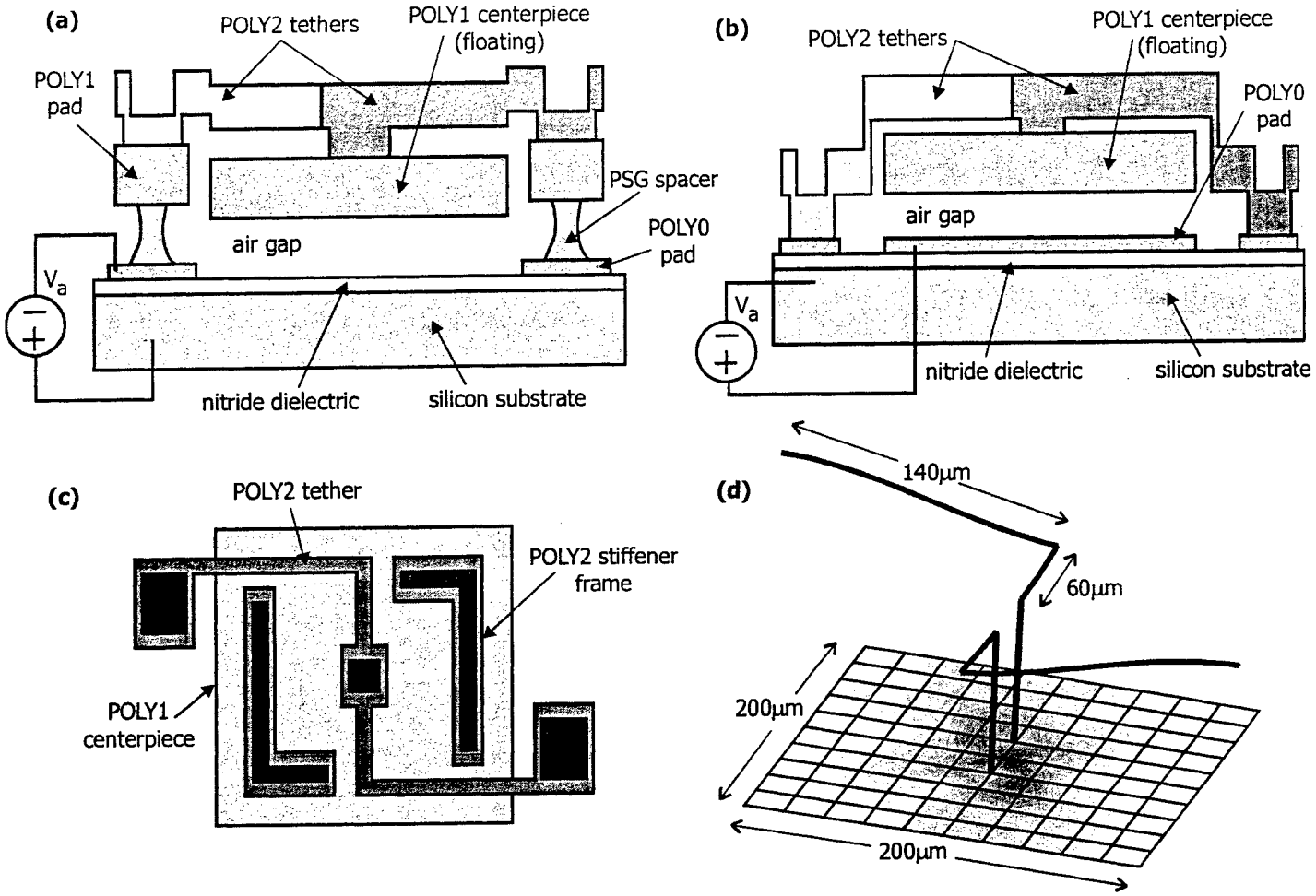

Fig. 10. (a) Profile of electrostatic positioner being fabricated in MUMPs. The device consists of voltage-driven POLY0 pads and silicon substrate, and a POLY1 centerpiece suspended by POLY2 tethers. The tethers are shielded from the substrate by the centerpiece thus minimizing the associated parasitics. The centerpiece and tethers are electrically-isolated by the PSG spacer formed by a controlled HF sacrificial etch. (b) Alternate design that does not require a controlled HF etch. The nitride serves as the dielectric spacer that isolates the tethers and centerpiece. A POLY0 pad now serves as the bottom electrode to which the centerpiece is attracted. (c) Plan view corresponding to profile in (a). Flexures in the tethers ensure that most of the deformation during actuation occurs in the tethers thus leaving the centerpiece relatively flat. The flexures also provide stress-relief to prevent buckling. POLY2 overlaid on the POLY1 centerpiece form a stiffener frame (not shown in the profile) that further ensures that the centerpiece remains flat. (d) 3D simulation in Abaqus using beam elements for the tethers and shell elements for the centerpiece. The stiffener frame was not modeled. At 0.6μm of average deflection, the variation across the centerpiece was less than 2%. Von Mises stress contours are shown on the centerpiece.

Simulation results (Fig. 10d) using Abaqus with electrostatic forces imposed as user-defined loads [11]-[12] show that the design of Figs. 10a and 10c meets the requirements of flatness as detailed in Section 4. At 0.6μm of center displacement, the variation of displacement across the centerpiece is less than 2%. This flatness is desirable for optical applications such as micromechanically-tuned lasers. Decoupling the design of the tethers from the design of the centerpiece also improves the flatness of devices built for leveraged bending [4]. Figs. 11a and 11b show a proposed design that utilizes leveraging of cantilevers with widened actuation pads to position a nominally rigid and flat centerpiece. This also alleviates the need for compressively stressed materials to achieve leveraged bending.

CONCLUSION

A thorough analysis of the various practical issues involved in designing an electrostatic positioner with full-gap travel has been presented. The effects of parasitic capacitances, including the "fixed" capacitance associated with non-uniform 2D deformation, are shown along with two designs that minimize their influence – the "folded capacitor" designs employing floating electrodes suspended by shielded tethers. Residual charge simply causes a voltage shift in the response of this positioner but can be further exploited to create a linear electrostatic actuator utilizing a precharged floating conductor.

Transient damping characteristics can be improved by over-stabilizing the positioner. All devices are currently being fabricated at MCNC and measurements will be presented in an upcoming paper.

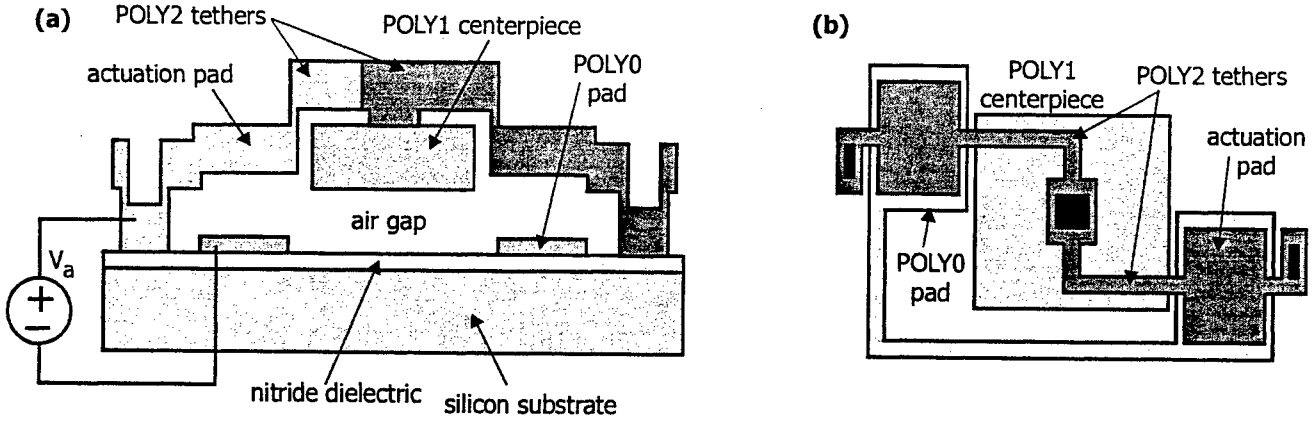

Fig. 11. Electrostatic actuator utilizing "leveraged bending" to achieve full-gap travel exploiting the same tether design as shown in Fig. 10. Decoupling the tether design from the centerpiece allows each element to be optimized separately. The large actuation pads connected to slender beams enhance the effectiveness of leveraging. (a) Profile. (b) Plan view.

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Complete Characterization of Electrostatically-Actuated Beams including Effects of Multiple Discontinuities and Buckling

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ABSTRACT

The entire process of calibrating an electromechanical simulator – identifying relevant parameters, designing and measuring test structures, extracting parameters using detailed electromechanical simulations, and extrapolating the behavior of an actual device – is presented. The simulation model for electrostatically-actuated beams is calibrated to a wide range of electrical and optical test structure measurements and is then used to predict the behavior of more complex dual-bias-electrode structures. Various mechanical discontinuities, and post-buckled pull-in behavior are addressed explicitly. Arbitrary fitting coefficients that limit generality are avoided. The well-characterized behavior of the dual-electrode structures can serve as verification test cases for evaluating coupled electromechanical simulators.

Keywords: *calibration, electromechanical, simulation*

INTRODUCTION

Computer simulation tools need to be thoroughly calibrated to particular fabrication processes in order to produce useful and accurate results. The calibration steps consist of identifying relevant simulation model parameters, designing suitable test structures, extracting parameters using detailed yet fast electromechanical simulations, and finally extrapolating the behavior of an actual complex device. Electrostatically-actuated beams fabricated in the POLY1 layer of MUMPs [2] are considered here. Caution must be exercised whenever simulating different actuation mechanisms or devices with dimensions beyond the range of the calibration. Uniformity of material properties cannot always be extrapolated.

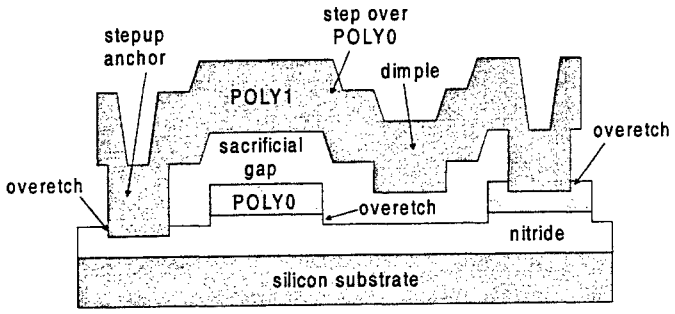

Fig. 1. Profile of typical electrostatically-actuated structure showing discontinuities and effects of overetch.

This simulation-based model consisting of geometrical and material property information precludes the need for rather ad hoc parametric adjustments and simplifying assumptions [3][5]. The model is calibrated to both optical and electrical measurements thus increasing confidence in the extracted parameters. The MUMPs system of materials is first described, highlighting the observed variations among beams of different width, the effects of overetch, and the influences of gold pads. Calibration of flat beams to pull-in voltages (V_{pi}) and buckling amplitudes is explained next. The calibration steps are then repeated for beams with steps over underlying POLY0 pads, and beams with dimples. Finally, the well-characterized Abaqus simulation model is extended to predict the behavior of dual-bias-electrode structures. The extrapolation is very good, verifying the accuracy of the calibration methodology.

MATERIALS SYSTEM

Measurements were made on a single die on the MUMPs27 run unless otherwise noted. The die was supercritically dried after a 2.5 minute HF release to obtain long freestanding beams. Rather than trying to extract parameters in light of run-to-run or even die-to-die variations, the goal of this paper is to come up with very accurate geometric and material properties, and hence to validate a parameter extraction methodology and its underlying coupled electromechanical simulation model.

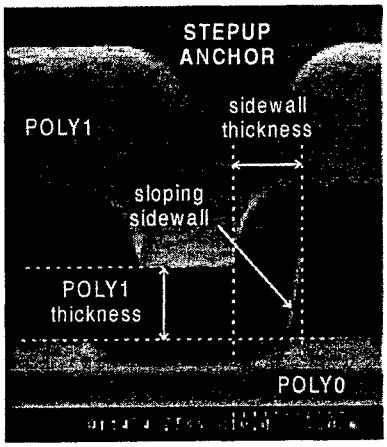

Fig. 2. SEM of stepup anchor showing thickness measurement site, and sidewall geometry.

Fig. 1 of an electrostatically-actuated beam shows steps/discontinuities and overetches. The geometric properties of interest are the thicknesses of layers, and shapes of the stepup anchors and other steps. The electrical thickness of the nitride was determined from capacitance measurements. All thicknesses and height measurements were made using a Zygo NewView 200 interferometer. The thickness of the POLY1 layer was measured at the base of a stepup anchor deposited on

POLY0 as shown in the SEM of Fig. 2. The overetch of about 0.03μm of the underlying POLY0 pad during the ANCHOR1 etch causes the measured thickness to be slightly less than the actual thickness. This discrepancy is offset in part by the overetch of the underside of an actual freestanding beam during the HF release, and by surface roughness which adds to optical thickness measurements but not to structural rigidity. All thicknesses used in subsequent simulations are shown in Table 1.

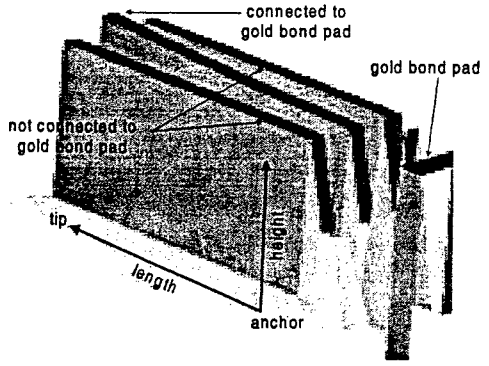

Fig. 3. Interferometric image of three unloaded, freestanding POLY1 cantilevers with similar designs except that the center one is connected to a gold bond pad. The center cantilever curls up more. Interferometric images only show top surfaces therefore the sacrificial gap is not displayed.

The sacrificial gap is determined by subtracting the thickness of the POLY1 layer from the height of an unreleased POLY1-plus-PSG stack deposited on POLY0. POLY0 layers connected to gold bonding pads are about 0.01μm thinner, and have rougher surfaces and hence lower reflectivity than isolated POLY0 layers. This might be due to an electrochemical potential set up by the gold pads that increases the etch rate of the POLY0 layer during the sacrificial HF etch. The influence of a gold pad depends on the amount of exposed surface area of the polysilicon part that it is connected to. This slight etching of the POLY0 layer causes the sacrificial gap in between the nitride and POLY1 to be about 0.01μm less than the gap between the POLY0 and POLY1. Another effect of gold is visible in Fig. 3 which shows that the cantilever connected to a gold pad curls up more than the other two cantilevers.

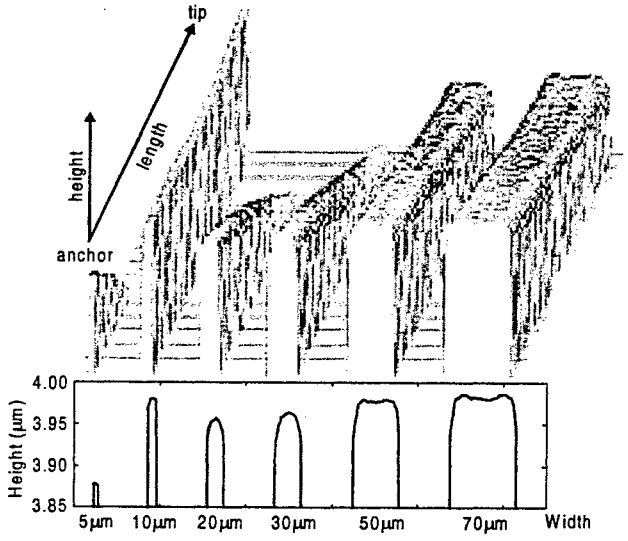

Fig. 4. Interferometric image of the unloaded deflection of released cantilevers of various widths fabricated in MUMPs 25.

The behavior of the beams also shows a dependence on their widths. Fig. 4 shows cantilever beams, all without connections to gold, that curl down with different radii of curvature with the exception of the anomalous 10μm-wide beam which actually curls up. In addition, each of the beams exhibits variations in height along its width as shown in the cross-sectional profile. The top surfaces of the narrower beams (less than 50μm wide) are rounded. It is difficult to determine if this roundedness is due to bending or to uneven etching of the surface. The wider beams show saddle-like height variations with rounded ridges near each edge. It is possible that the two ridges coalesced into one mound in the case of the narrower beams. Since the source of such widthwise variations is unclear, only 30μm-wide beams are used for the calibration to minimize the effects of non-ideal cross-sections while avoiding the saddle-like height variations.

Table 1: Simulation Parameters

Measured Thicknesses (μm)	
POLY0 (with gold)	0.53
POLY0 (without gold)	0.54
POLY1	1.99
Sacrificial PSG	2.16
Nitride (electrical)	0.074
Stepup sidewall	1.80

Extracted Properties	
Initial biaxial stress	7.8 MPa
Young's modulus	135 GPa

CALIBRATION TO FLAT BEAMS

For the best match to simulations, the beams, flat except for the anchor stepups, were designed to be essentially two-dimensional without POLY1 enclosure lips around the anchors [1]. The 2D simulation model in Abaqus™ incorporates overetch, sloping sidewalls and conformal deposition.

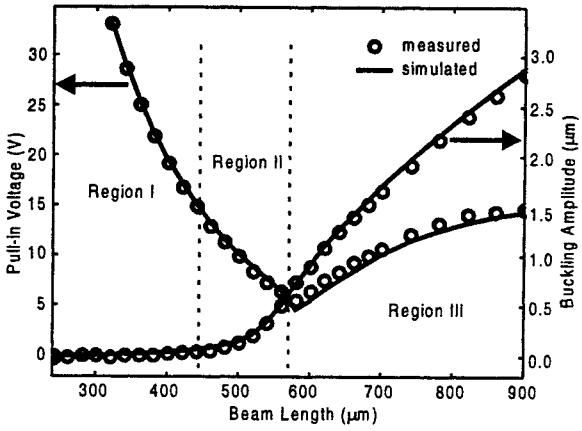

Fig. 5. Pull-in voltages and buckling amplitude of flat beams as functions of beam length. Three regions of pull-in behavior are demarcated.

The beams tend to deform to relieve some initial as-deposited compressive stress. The amplitude of the deflection depends on initial strain, beam length, thickness and boundary

conditions. In contrast to the ideal case where deflection occurs only beyond a threshold buckling beam length, beams with stepup anchors deform even at shorter lengths as shown in Fig 5. The strain parameter can be extracted by fitting Abaqus simulations to the measured buckling amplitudes for various beams. The excellent fit indicates that the other parameters critical to buckling amplitude are as determined from interferometric measurements and SEMs. Measurements of beams with backfilled stepup anchors [7] show that the pressure due to encapsulated PSG in such anchors causes the beams to always deflect downwards instead of upwards, and with larger amplitudes as shown in Fig. 6.

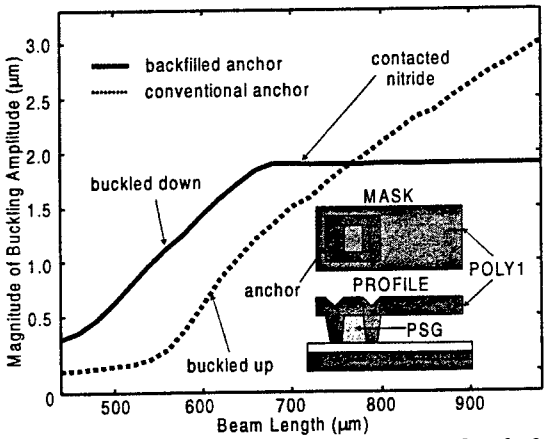

Fig. 6. Measured magnitude of buckling amplitude for beams with backfilled anchors compared to beams with conventional anchors. Beams are from MUMPs 25 run.

Young's modulus can be extracted by fitting simulation results to V_{pi} measurements [3]. An HP 4275A capacitance-voltage (CV) meter was used to apply a bias voltage and to sense the abrupt increase in capacitance at pull-in. The simulation fit is good with the kink at 580μm captured accurately as shown in Fig. 5 although the simulated voltages in Region III are slightly lower than those measured. The three types of pull-in behavior corresponding to the regions in Fig. 5 are shown in Fig. 7. A short beam in Region I will deflect continuously with increasing voltage until the gap decreases to about 1.0μm then snap down to the nitride dielectric. A longer beam in Region II that has an initial buckling displacement deflects continuously then snaps down to a stable state below the zero-displacement position. From

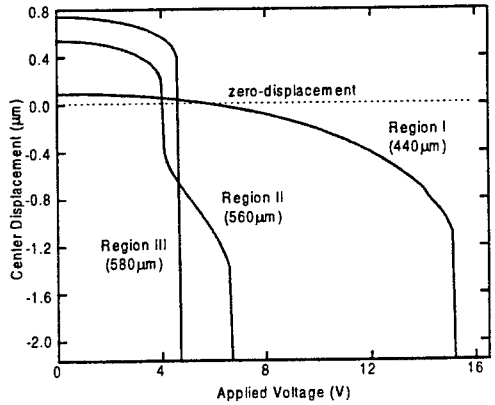

Fig. 7. Three different types of pull-in behavior.

there, it continues to deflect with increasing voltage before finally snapping down again, this time contacting the nitride. This two-step pull-down phenomenon does not occur for longer beams in Region III because there is no stable state below zero-displacement so the beams snap down all the way to the nitride. In contrast to beams in the first two regions, beams exhibiting this third type of behavior have V_{pi}'s that increase with beam length because the buckling amplitude and hence the effective gap increases. Therefore, the V_{pi}'s of these post-buckled beams are more sensitive to initial stress than the V_{pi}'s of shorter beams. Table 1 shows extracted properties.

MULTIPLE DISCONTINUITIES

Beams fabricated out of conformal polysilicon can have dimples, and steps over underlying POLY0. Dimple depth and POLY0 thickness were measured optically then included in the

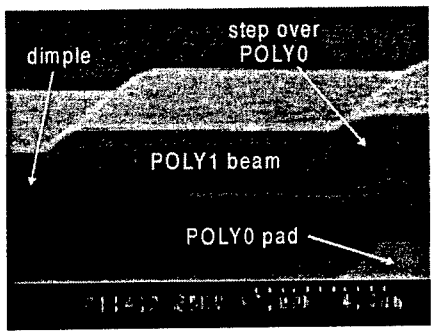

Fig. 8. SEM of step over POLY0 and step into dimple.

Abaqus model using the SEM of Fig. 8 as a guide to the actual shape of the discontinuities. The inset in Fig. 9 shows test structures designed to examine the effects of these discontinuities. Once again, the V_{pi}'s and buckling amplitudes of beams of various lengths were measured. The beams over POLY0 behave quite similarly to flat beams as shown in Fig. 9. The transition in buckling amplitudes from the pre-buckled to the post-buckled states is more gradual and begins earlier due to the increased compliance at the boundaries. The amplitudes are also slightly smaller. On the other hand, beams with dimples

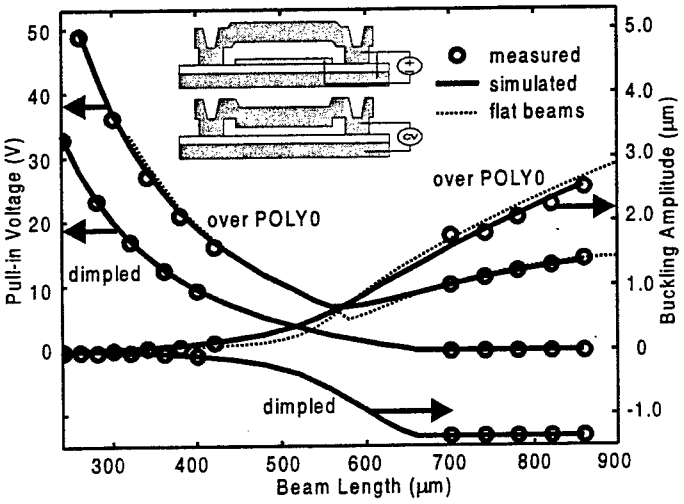

Fig. 9. Pull-in voltages and buckling amplitude as functions of beam length for beams over POLY0 and beams with dimples. Values for flat beams are in dotted lines.

buckle downwards systematically instead of upwards. Therefore, the post-buckled V_{pi}'s do not rise with beam length but instead go to zero once the beams buckle into contact with the nitride. The simulation fits are good indicating that the geometrical model is valid.

DUAL-BIAS-ELECTRODE STRUCTURES

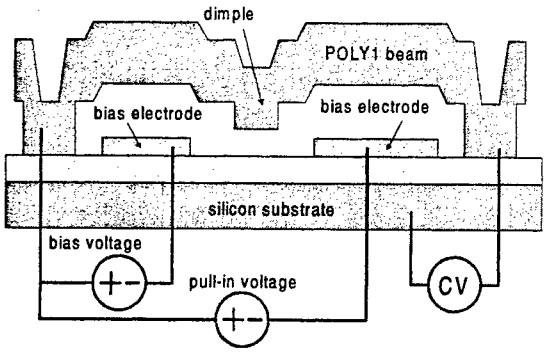

Fig. 10. Profile of dual-bias-electrode structure.

The simulation model characterized in the previous sections is now used to predict the behavior of more complex dual-bias-electrode structures shown in Fig. 10. The measurements of Fig. 11 are of V_{pi} at one electrode as a function of bias voltages (V_{bias}) applied to the other electrode for three different devices. The devices were designed such that pull-in is still abrupt despite the leveraging action. By having two bias electrodes, multiple precise pull-in voltage measurements can be made on a single device. The dimple at the center of the beam prevents conductor-to-conductor contact. Dielectric charging [1] should not affect the behavior of the system. The V_{pi} vs. V_{bias} curves for the devices with left and right electrodes of equal length are symmetric about the $V_{pi} = V_{bias}$ line. By swapping the bias and pull-in connections, the integrity of the devices can be verified by checking for symmetry.

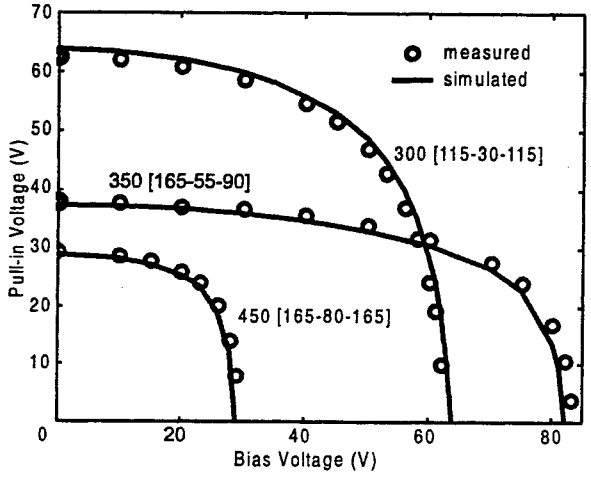

Fig. 11. Pull-in voltage as a function of bias voltage for three dual-bias-electrode structures. The first number in the label is the beam length. In the brackets are the lengths of the pull-in electrode, dimple, and bias electrode.

The extrapolated behavior matches the measurements well. For curves such as these with some segments that are primarily vertical, error norms should be calculated along the directions normal to the curves rather than simply taking the differences between the measured and simulated V_{pi}'s at a particular bias. Using this normal-direction error metric, the simulations match the measured values to within 3%. It has thus been demonstrated that the model parameters in Table 1 along with the measurement data in Fig. 11 can be used as verification test cases to evaluate the accuracy of coupled electromechanical simulators.

CONCLUSIONS

A comprehensive methodology to calibrate a simulation model to the MUMPs process of MCNC has been presented. The limits of the calibration procedure due to width-dependent variations and the effects of gold pads were discussed. The extrapolations of the simulation model to more complex devices were excellent demonstrating the viability of the dual-bias-electrode structures to serve as canonical benchmarks for coupled electromechanical simulators.

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Characterization of Electrostatically-Actuated Beams through Capacitance-Voltage Measurements and Simulations

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ABSTRACT

Detailed 2D electromechanical simulations of electrostatically-actuated beams reveal phenomena not captured by 1D or quasi-2D simulations. The behavior of the beam when in contact with a dielectric layer is studied. Capacitance-voltage measurements are used to extract material properties and explore surface phenomena such as charge accumulation, stiction and surface roughness. Monte Carlo simulations reveal the limits of simulation accuracy due to statistical distributions of input parameters.

Keywords: electrostatically-actuated beams, capacitance-voltage, contact, simulation accuracy

INTRODUCTION

Electrostatically-actuated beams (Fig. 1) are widely used and studied in the MEMS community. Such beams are used as switches and resonators, and for extracting material properties [1,2,3]. Often, rather ad hoc "correction factors" are required to account for behavior not captured by simplified 1D or quasi-2D simulation models. These correction factors are usually specific to the particular process and range of beam dimensions being studied. Simulation results are presented using a more detailed 2D mechanical model which reveals some phenomena neglected by 1D or quasi-2D simulations.

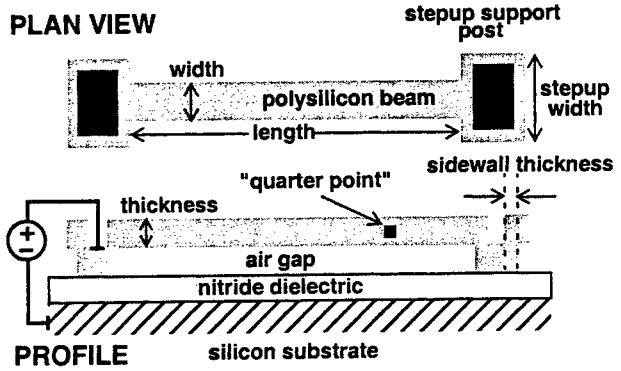

Fig. 1. Electrostatically-actuated beam

The behavior of the system is studied for the case when the beam is in contact with the nitride dielectric that coats the bottom electrode -- a mode of operation important to capacitive microwave switches [4]. Capacitance-voltage (CV) measurements are used to extract material properties and explore surface phenomena such as charge accumulation, stiction and surface roughness.

Monte Carlo simulations reveal the limits of simulation accuracy due to the limited precision of extracted parameters. The distribution of beam pull-in voltages due to process variations is also studied.

SIMULATION MODEL

Fig. 1 shows both a plan view and a profile of a typical electrostatically- actuated beam. Applying a voltage between the beam and silicon substrate causes the beam to deflect downwards. Fig. 2 shows a typical simulation of the capacitance between the top and bottom electrodes as a function of applied voltage with regions numbered corresponding to those in Fig. 3. Fig. 3 is a schematic plot of the total energy of the electromechanical system as a function of voltage and the displacement of a "quarter point" midway between the support post and center of the beam (see Fig. 1). The numbered circles indicate the displacement at equilibrium. As the voltage is increased, the characteristic "pull-in" phenomenon occurs when the barrier between the two minima disappears at the pull-in voltage (V_{pi}) and a portion of the beam comes into contact with the surface of the dielectric. As the voltage continues to increase, more of the beam contacts the dielectric i.e. the beam "zips up". When the applied voltage is decreased, the quarter-point moves away from the surface, i.e. the beam "peels off", but still remains in the same local energy minimum region. Eventually, the barrier between the minima disappears and the entire beam pops off the surface of the dielectric.

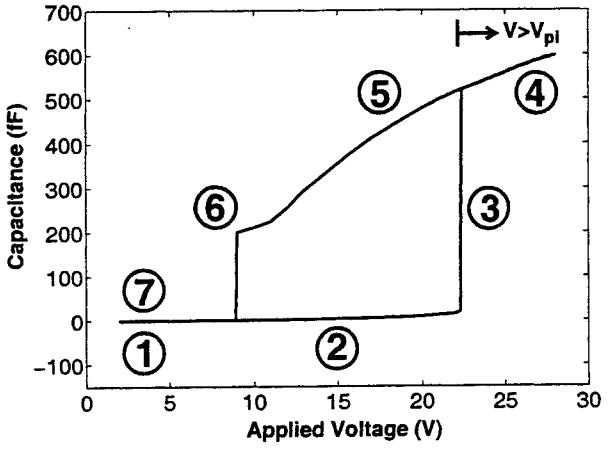

Fig. 2. Typical capacitance-voltage curve

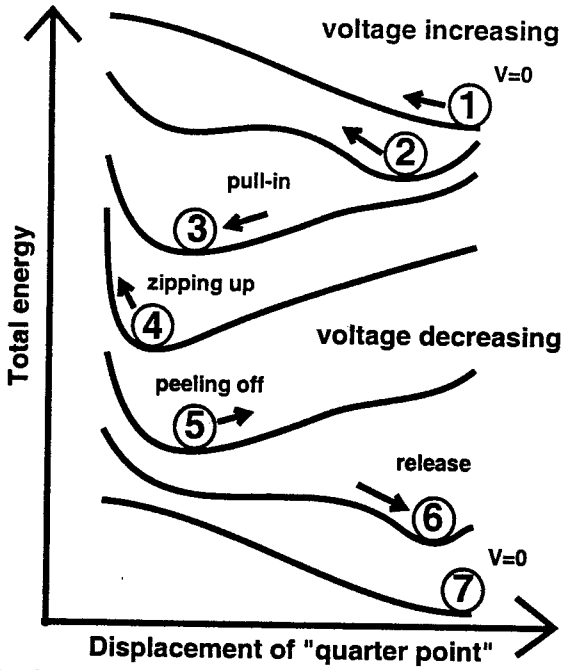

Fig. 3. Total energy of system and equilibrium state as a function of voltage and displacement of "quarter-point"

This electromechanical system is simulated in Abaqus with the electrostatic force applied to the bottom surface of the beam as a user-defined load [5]. The 2D Abaqus simulation provides good mechanical accuracy by automatically including the effects of geometric nonlinearity (or stress stiffening), compliant stepups and contact. The Abaqus model (Fig. 4) uses reduced-integration elements, with plane strain elements for the stepup which adheres to the dielectric surface, and plane stress elements for the beam itself. For the analysis, using 50 quadratic rectangular elements for one-half of the beam provides good accuracy. A correction factor to account for 3D plate-like effects in the beam is included [3].

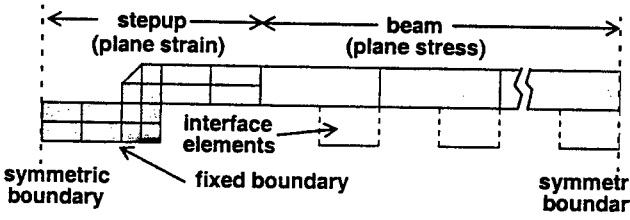

Fig. 4. Mechanical model in Abaqus

To model the electrostatic force, we assume that the beam is made up of many parallel-plate capacitors connected in parallel. This approximation is quite accurate for planar systems, particularly when the gap between electrodes is small as is the case when the beam is in contact with the dielectric. Effects of fringing fields [2] and finite plate thickness are included in our electrostatic force model. Results shown in Fig. 5 using a 2D field solver reveal the amount by which an ideal 30μm-wide capacitor model with infinitely thin plates and no fringing fields underestimates the force between the plates.

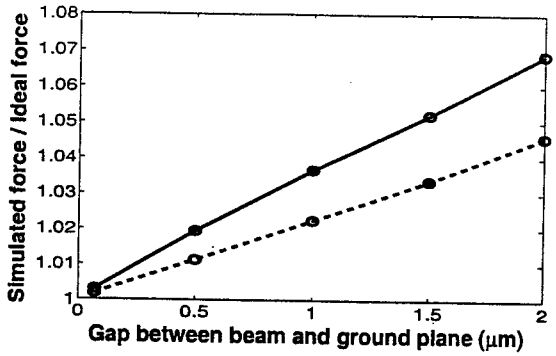

Fig. 5. Simulated electrostatic force on 30μm-wide beam

Fig. 6 compares the accuracy of a 2D Abaqus simulation to a 3D simulation done in IntelliCAD. The IntelliCAD model comprises a 400μm x 30μm beam 2μm thick suspended 2μm above a 0.6μm nitride layer. The ends of the beam are perfectly fixed. The beam is made up of 14 x 2 x 1 quadratic brick elements. The same dimensions, material properties, boundary conditions and discretization sizes are used in the 2D Abaqus simulation. The IntelliCAD model, which consumes over three orders of magnitude more computation time, is just a little stiffer (less than 2%).

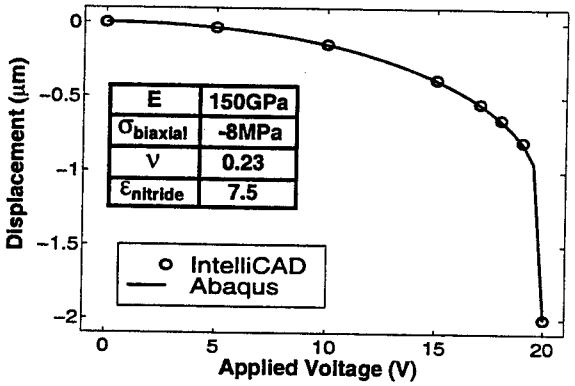

Fig. 6. Comparison between Abaqus model and IntelliCAD

We choose to quantify the residual stress in the system in terms of an expansion coefficient, α. The resultant compressive biaxial residual stress in a uniformly deposited film due to this coefficient is

$$\sigma_{biaxial} = \frac{\alpha E}{1-\upsilon} \qquad (1)$$

where E is the modulus of elasticity and υ is Poisson's ratio. This allows us to gradually ramp the system up to the correct initial stress state before applying an electrostatic load. Incorporating a large residual stress as an initial condition in a single step can result in erroneous simulations -- underestimating the initial bowing or deforming the beam into an incorrect buckling mode.

The average longitudinal initial stress in the beam depends on the length of the beam, the width of the stepup and the sidewall thickness (Fig. 7). The width of the stepup used in 2D simulations should be less than the actual physical width because only the portion of the stepup that is close to the beam interacts with the beam. In general, the stress relaxes more for more compliant stepups and longer beams. However, with the 30μm-wide stepup, the stress actually increases with beam length.

The stiffness of the stepup affects the initial shape of the beam. The interferometric picture (Fig. 8) reveals that beams of the same length can either bow up or down depending on the width of the stepups. A beam with a narrow stepup (90μm) as shown at the top of Fig. 8 bows up whereas beams with wide stepups bow down. The three beams at the bottom of Fig. 8 are part of an array of 10 parallel beams all connected to the same stepup structure. The beam at the edge of the array (second from the top), which has an effectively narrower and hence more compliant stepup, bows up whereas the two lower beams bow down. This effect of stepup widths is verified in simulations and implies that beams connected to the same support posts can influence each other mechanically if their separations are small enough. In some cases, beams which bow up initially do not return to that initial state after going through a pull-in-and-release cycle but remain bowed down.

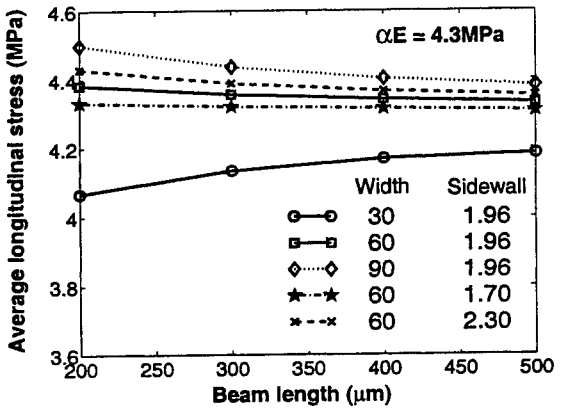

Fig. 7. Average longitudinal stress in beam as a function of stepup geometry and beam length

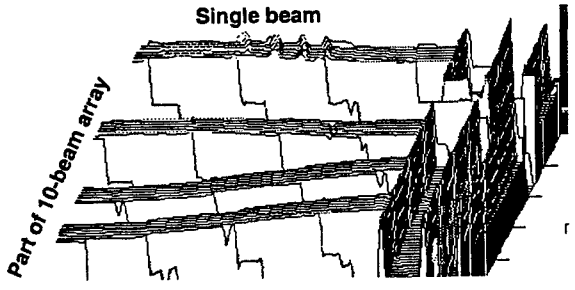

Fig. 8. Interferometric image of 540μm fixed-fixed beams, courtesy of Zygo Corporation

OPTICAL AND MECHANICAL MEASUREMENTS

Fixed-fixed beams and cantilevers of various dimensions were fabricated in the POLY1 polysilicon layer on the MUMPs 22 run. A Zygo interferometer was used to survey the structures and showed that the fixed-fixed beams were flat (less than 0.03μm of bow at the center) up until lengths of 520μm. 600μm beams bowed by 1.06μm. Cantilevers longer than 200μm curled down towards the substrate due to a stress gradient of about 0.4MPa/μm. Cantilevers longer than 290μm touched the nitride.

The thickness of the polysilicon was determined by an interferometric measurement of the thickness of a long polysilicon cantilever that was stuck to the nitride. The gap was determined by subtracting that thickness from the height of a short fixed-fixed beam above the nitride. For verification, a Dektak IIA was used to measure the thickness of a 600μm fixed-fixed beam pushed down by the force of the Dektak stylus, and the height of a 200μm-wide beam which was only partially released. The electrical thickness of the nitride (thickness divided by ε_r) was determined from a capacitance measurement of a polysilicon layer (POLY0) deposited directly on the nitride. This nitride thickness measurement neglects any overetch due to the etching of polysilicon and PSG layers [3]. Furthermore, when the beam comes into contact with the nitride, the surface roughness of the polysilicon effectively adds to the electrical thickness of the nitride because it determines the minimum separation of the two plates of the capacitor.

Table 1 shows the parameters used in simulations. Widths and lengths are assumed as drawn since linewidth resolution is better than 0.1μm [6]. Perfect conformal deposition is assumed, and Poisson's ratio is taken as 0.23.

Table 1. Parameters used in simulations

Poly thickness	Air gap	Nitride thickness	Poisson's ratio	Sidewall thickness	Stepup width
1.96μm	1.94μm	0.068μm	0.23	1.96μm	60μm

ELECTRICAL MEASUREMENTS

V_{pi}'s, voltages at which the capacitances of the systems change abruptly, were measured using an HP4275A capacitance meter with voltage steps of 0.1V. The dice were placed in Gel-Pak™ trays. Measured V_{pi}'s are plotted on a semilog scale in Fig. 9 and lie on a straight line as expected. These measurements were confirmed by using an HP4155A to source a constant 20pA current and observing the voltage of the beam increase as a function of time. At pull-in, the capacitance increases abruptly and the voltage of the beam has to decrease momentarily due to charge conservation. The V_{pi}'s are significantly lower than measurements made on previous MUMPs runs [3] indicating that the polysilicon is more flexible.

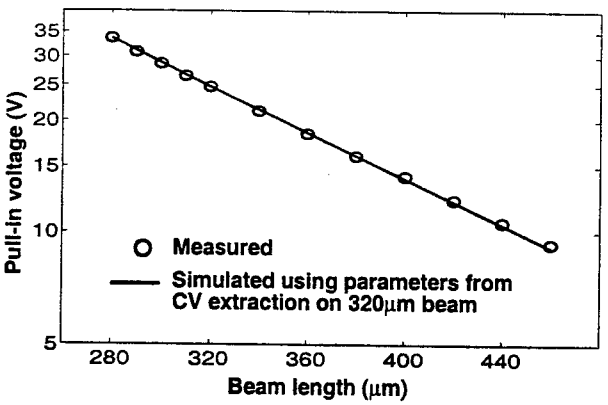

Fig. 9. Pull-in voltages as a function of beam length

Typical CV curves of a fixed-fixed beam and a cantilever are shown in Figs. 10 and 11 respectively. There is a plateau in the peel-off portion of the cantilever CV curve where most of the cantilever snaps off the nitride surface leaving only the tip touching as shown schematically in Fig. 11. This phenomena occurs only for certain cantilever lengths and has been verified in simulations.

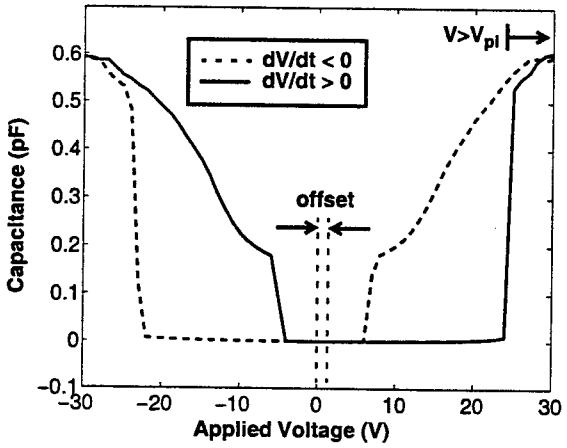

Fig. 10. CV curve of a 340μm fixed-fixed beam

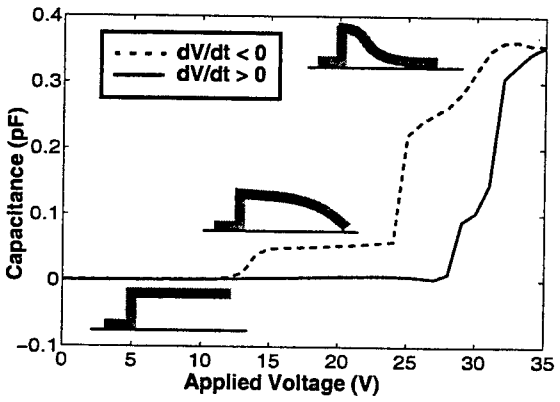

Fig. 11. CV curve of a 130μm cantilever beam

Stiction, which holds back the beam somewhat during peel-off, causes the zip-up and peel-off regions of the CV curves above V_{pi} not to overlap as they would otherwise (compare the regions $V>V_{pi}$ in Figs. 2 and 10). Trapped charge in the nitride shifts the measured V_{pi}'s and offsets the CV measurements along the voltage axis as shown in Fig. 10. Assuming a sheet of nitride charge, the offset voltage is

$$V_{offset} = \frac{xQ_f}{\varepsilon_o \varepsilon_r} \qquad (2)$$

where Q_f is the areal charge density, x is the distance of the charge sheet from the nitride-substrate interface and $\varepsilon_0\varepsilon_r$ is the relative permittivity of the nitride. To quantify this charge, we measured V_{pi}'s by applying both positive and negative voltages. Theoretically, the positive and negative V_{pi}'s should be of the same magnitude since the electrostatic force is proportional to the square of the applied voltage. The measured differences between the magnitudes were less than 0.2V if we waited for more than 5 minutes between measurements. Thus, fixed charge is not a major problem.

Mobile charge, however, seriously distorts the measurements. V_{pi}'s measured in quick succession (less than 1 minute between measurements) are successively lower (magnitudes tending towards zero). This indicates that charge of polarity opposite to that of the voltage applied to the beam is being accumulated with each measurement.

Fig. 12 shows the measured capacitance of a beam as a function of time at a constant applied voltage. This particular 370μm long beam was stuck to the nitride even with no applied voltage, allowing us to measure the decay rate of the capacitance when the applied voltage was removed. The rate of capacitance increase is larger for higher applied voltages. The measurement shown is that using a 100kHz 50mVrms sensing signal but the measurement shows no dependence on signal amplitude or frequency.

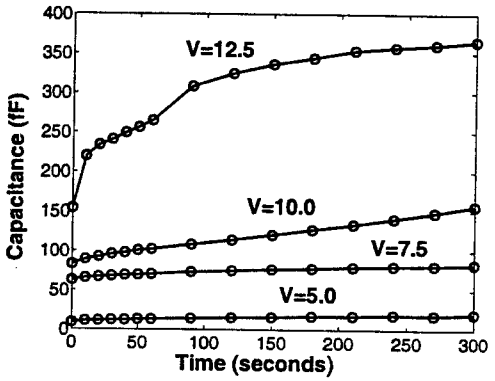

Fig. 12. Capacitance variation with time for various constant applied voltages

These measurements indicate that charge builds up in the system, probably in the nitride or near its surface,

when the beam is in contact with the nitride surface. The polarity of the charge is opposite to that of the beam thus attracting more of the beam into contact and increasing the capacitance of the system. Another source of charging effects could be the movement of charge from the bottom to the top surface of the nitride where it has the largest effect as shown by Eq. 2. The sensitivity of this system to surface charge could be exploited to monitor the movement and buildup of charge in dielectrics in real-time.

In order to avoid charge buildup, especially at high voltages, and to avoid stiction effects, we measure the capacitance of the beam quickly as it is zipping up instead of when it is peeling off. We assume that stiction is a very short ranged force which has no effect until two surfaces are in contact, and therefore does not influence the zipping-up process. While holding the voltage steady at a voltage well below pull-in but still high enough to hold the beam once the beam is in contact with the nitride surface, we induce contact by pushing the beam down with a probe tip. We then ramp up the voltage while measuring capacitance. The measurement takes about 10 seconds and is shown in Fig. 13 for a 320μm beam.

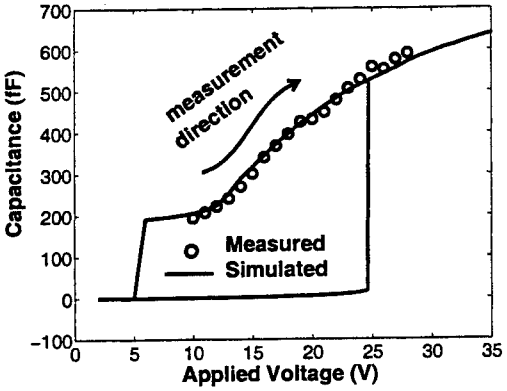

Fig. 13. CV curve of a 320μm beam

MATERIAL PROPERTIES EXTRACTION

With geometrical measurements, V_{pi}'s and CV curves, E and $\sigma_{biaxial}$ can be extracted. Fig. 14 shows contours of $\left|V_{pi}^{measured} - V_{pi}^{simulated}\right|$ in E-$\sigma_{biaxial}$ space of a 320μm fixed- fixed beam. All simulations using E-$\sigma_{biaxial}$ pairs within the narrowest contour (±0.1V) give simulated pull-in voltages within ±0.1V of the measured value. Similar contours can be obtained for a beam of a different length and the region where the ±0.1V contours of the two beams overlap is the region in E-$\sigma_{biaxial}$ space which gives the correct value of V_{pi} for both beams. By overlaying the contours for 320μm and 440μm beams, and assuming a resolution in V_{pi} of ±0.1V, we obtain E=110 ± 2.9GPa and $\sigma_{biaxial}$=-6.0 ± 0.4MPa. The uncertainties in E and $\sigma_{biaxial}$ increase to ±5.2GPa and ±0.8MPa respectively if the V_{pi} resolution is only ±0.2V. The extracted E is low and could be due to a more porous microstructure.

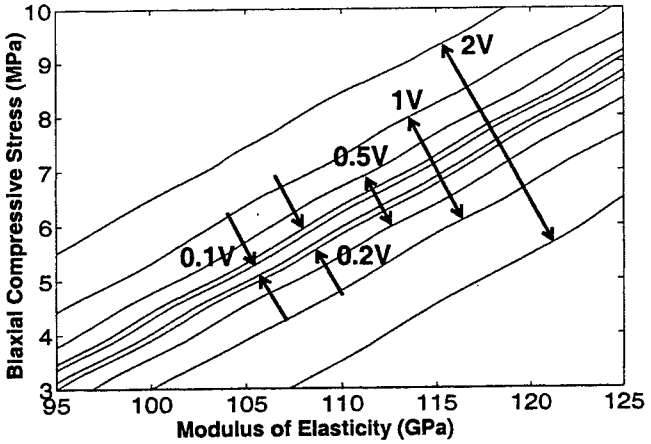

Fig. 14. Contours of V_{pi} resolution for 320μm beam

The RMS difference between measured and simulated capacitances gives another set of contours, shown in Fig.15, for the 320μm beam. These contours are more sensitive to E since the behavior of the beam when in contact with the nitride surface is dominated by bending. By overlaying this set of contours over the V_{pi} contours of Fig. 14, E and $\sigma_{biaxial}$ can be determined from measurements of only one device. Noise in the present capacitance measurements force us to assume RMS errors of at least ±15fF. The extracted parameters are E=112 ± 4.7GPa and $\sigma_{biaxial}$=-6.5 ± 1.0MPa. These values are quite similar to that obtained using the previous method. Fig. 13 compares the measured capacitances to the simulated values.

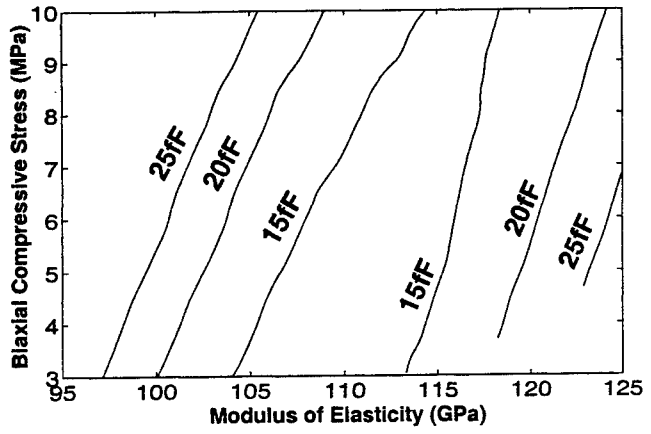

Fig. 15. Contours of RMS difference between measured and simulated capacitance values for 320μm beam

These parameters, extracted from a single device, are used to predict the behavior of beams of different lengths. Fig. 9 compares simulated V_{pi}'s to measured values whereas Fig. 16 compares simulated CV's to

measured curves for various beam lengths. The prediction of V_{pi}'s is reasonable but the CV fit is poor for the 400μm beam. A single set of simulation parameters could not fit all the measured CV curves even if the gap spacing and nitride thickness were varied arbitrarily. Surface roughness of the polysilicon might play a role here -- at the higher voltages used to measure the shorter beams, the roughness at the surface might be compressed so that the separation between the beam and substrate approaches the measured nitride thickness whereas at low voltages, the surface roughness increases the separation. Thus as shown in Fig. 16, the measured capacitances of the 400μm beam are lower than the simulated capacitances at low voltages but approach the simulated values at higher voltages.

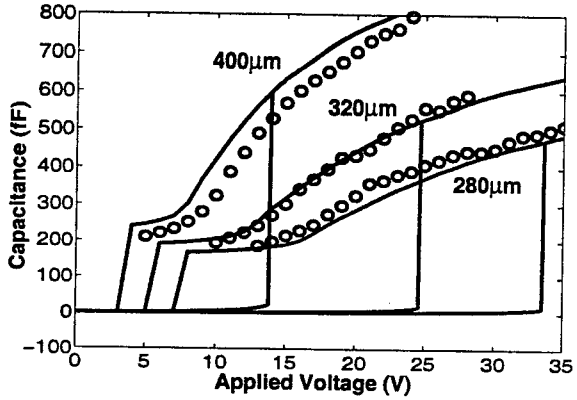

Fig. 16. Measured and simulated CV curves

MONTE CARLO SIMULATIONS

In a complex non-linear system such as this electrostatically-actuated beam, it is difficult to determine the interdependence of various properties and parameters and hence Monte Carlo simulations are required. As a guide for users of MEMS simulation tools, a Monte Carlo simulation on a 320μm beam (measured V_{pi} = 24.7) was performed to obtain bounds on the precision of the simulated V_{pi} assuming finite precision in input parameters as given in Table 2. The resolution of E and $\sigma_{biaxial}$ are that described in the previous section whereas the resolution of the other parameters are assumed from experience with the measurement equipment. A Monte Carlo simulation assuming uniform distributions of the input parameters within their ranges of uncertainty gives a standard deviation in V_{pi} of 0.36V. The distribution of V_{pi}'s is shown in Fig. 17.

Table 2: Precision of input parameters

Polysilicon thickness	Air gap	Nitride thickness	E	$\sigma_{biaxial}$
±0.01μm	±0.01μm	±0.01μm	±3GPa	±0.4MPa

The range of V_{pi}'s due to intra-run variations in process parameters can be determined assuming some reasonable standard deviations in parameters given in Table 3 [3,6]. The resulting standard deviation in V_{pi} is 2.92 V.

Table 3: Standard deviations due to processing variations

Polysilicon thickness	Air gap	Nitride thickness	E	$\sigma_{biaxial}$
0.049μm	0.12μm	0.0024μm	1.9GPa	0.45MPa

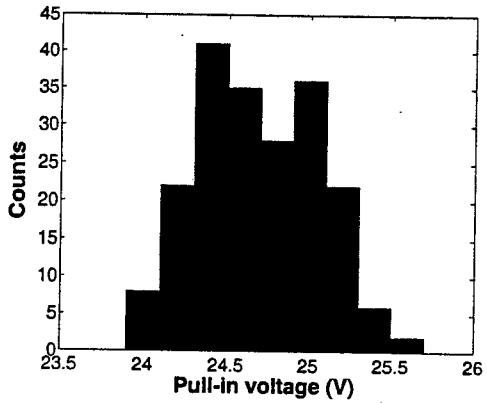

Fig. 17. Distribution of pull-in voltages due to finite precision of simulation parameters

CONCLUSIONS

It is shown that detailed 2D mechanical models, particularly of stepups, reveal phenomena not captured by 1D or quasi-2D simulations. However, 3D simulations are necessary to model plate effects and the stepup supports more accurately. CV measurements of the beam in contact with the nitride surface can potentially be used for calibration if the effects of charge accumulation and surface roughness are mitigated. Currently, a process using a thicker oxide layer as a dielectric is being developed. Interferometric measurements will be used to corroborate the CV measurements and explore 3D effects.

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SPUTTERED SILICON FOR MICROSTRUCTURES AND MICROCAVITIES

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ABSTRACT

Sputtered silicon can be used to make released microstructures at temperatures compatible with prefabricated aluminum-metallized CMOS circuitry. The fabrication sequence is similar to LPCVD polysilicon processes and involves a wet release from an oxide sacrificial layer. This process was used to fabricate a variety of test structures, including cantilevers, combs, and spirals. During release of the structures porosity to HF was observed in films up to 5 μm thick. This porosity resulted in the formation of completely enclosed cavities formed beneath silicon membranes over oxide sacrificial layers, and may have implications for the packaging of released devices. Several properties of the sputtered silicon films were investigated, including their in-plane stress, strain gradient, film density, surface roughness, electrical resistivity, and permeability. The dependency of these properties on deposition power, pressure, and film thickness as well as the effects of low-temperature annealing were also investigated.

INTRODUCTION

Due to its excellent mechanical properties, controllable stress, and reasonable conductivity, polysilicon has been the material of choice for most surface micromachined structures since the early 1980's [1] and has been integrated with on-chip circuitry for almost as long [2]. This integration is vital to the performance of many surface micromachined sensors, since as dimensions decrease, sensitivity often falls off precipitously. The sensitivity of a torsional capacitive accelerometer, for example, scales as the fifth power of the lateral dimension.

Unfortunately, the high deposition and annealing temperatures of LPCVD polysilicon (~580-630 °C and >900 °C, respectively), have required either depositing metal layers after the polysilicon deposition [3] or using refractory metals such as tungsten instead of aluminum [4]. Both approaches increase the overall fabrication complexity and may require re-engineering the CMOS process to accommodate the new thermal budget, metal layers, and/or lithography changes.

Sputtered silicon, by contrast, can be used to make released microstructures atop pre-fabricated, standard aluminum-metallized CMOS. This allows greater flexibility in creating or selecting a circuit process.

Depending upon the application, several properties may be important for the structural layer of a micro-fabricated device. Among these characteristics are average stress, strain gradient, film density, surface roughness and electrical resistivity. Each of these properties is addressed in the sections to follow. Control of stress was achieved without the high temperature anneals of prior work [5]. Additionally, packaging of completed devices is often a concern. Sputtered silicon exhibits porosity to HF that may be useful in forming sealed protective cavities, thus simplifying packaging. The effects of low-temperature anneals on the properties of sputtered silicon were also investigated.

FABRICATION

Sputtered silicon microstructures can be incorporated into process flows that are virtually identical to those used for conventional LPCVD polysilicon micro-structures. Specifically, sputtered silicon films may be deposited atop sacrificial oxide layers and then undercut in buffered HF or PAD etch.

The basic process flow used here is illustrated in Figure 1. The fabrication of the mechanical layers began by depositing the silicon dioxide sacrificial layer. Because of its faster HF etch rate, phosphosilicate glass (PSG) with a phosphorous content of 8% was used instead of undoped low-temperature oxide (LTO). Next, a layer of boron-doped sputtered silicon was deposited. The doping concentration of the target in this study was 40-80 ppm., but much higher concentrations are available. The deposition power and pressure ranged from 1.5 to 2.5 kW and 8 to 14 mTorr, respectively. Deposition rates were between 19 nm, for the 1.5 kW and 14 mTorr case, and 37 nm/min for the 2.5 kW and 8 mTorr case. The deposited thicknesses of the sputtered silicon layers ranged from 0.6 μm to 5.0 μm.

Optional bondpad contacts were formed on some wafers by sputtering and patterning 500 nm of aluminum (Figure 1-a) atop the sputtered silicon. In the case where sputtered silicon microstructures are integrated with CMOS, this aluminum layer would not be necessary, as it would be part of the underlying circuitry. The sputtered silicon was then patterned using an SF_6-C_2ClF_5 plasma (Figure 1-b).

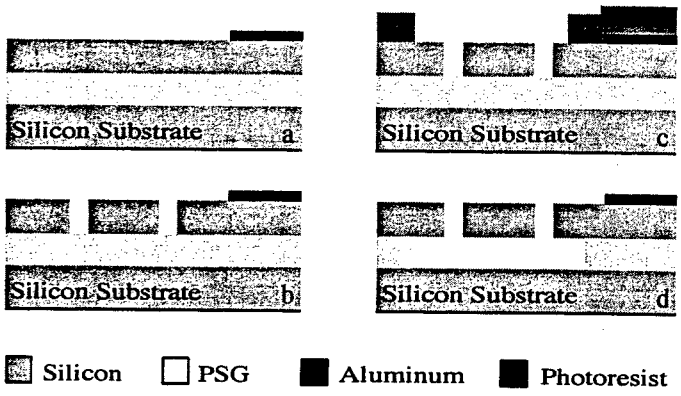

Figure 1: Process flow for sputtered silicon structures: Deposit PSG, sputtered silicon and aluminum layers, and pattern aluminum layer (1-a); Pattern sputtered silicon layer (1-b); anneal wafer at 350 °C and spin on protective resist layer (1-c); release in buffered HF, transfer to isopropyl alcohol and dry using critical point technique (1-d).

The wafers were released in either 20:1 buffered HF, 6:1 buffered HF, or Pad etch (1:1:1,NH_4HF:$HC_2H_3O_2$:H_2O). The latter etchant is more selective to aluminum metallization. A protective layer of photoresist (Figure 1-c) was used to mask areas of the PSG layer that were intended to remain behind after the release, and to protect the bondpads from buffered HF.

During the initial trials, delamination of the protective photoresist resulted in the attack of areas that were intended to remain unreleased. Baking the wafer prior to spinning on the resist, and curing it afterwards at 110 °C as suggested in prior work [6], substantially improved adhesion. However, photoresist adhesion remains an issue for very long etches in HF.

An alternative to photoresist may be found in PECVD carbide, which has been shown to be impervious to HF [7]. It can thus be used as an alternative to the photoresist protective layer in much the same way as LPCVD nitride is used in many LPCVD polysilicon processes [3], but at deposition temperatures compatible with aluminum-metallized CMOS.

Following the HF release (Figure 1-d), the wafers were immersed in acetone and methanol or in isopropyl alcohol. Some wafers were dried using the critical point method [8] while others were allowed to dry in air. Critical point drying helps alleviate problems with capillary forces that cause the released devices to stick to the substrate. After drying, the wafers were cleaved into chip sized samples.

Figure 2 shows an example of a sputtered silicon comb structure fabricated using this technique. The 215 μm long tines are separated from their counterparts by 2 μm. Each tine is 3 μm wide and 2 μm thick. The survivability of the released structure was accidentally demonstrated when the wafer was cleaved directly beneath it.

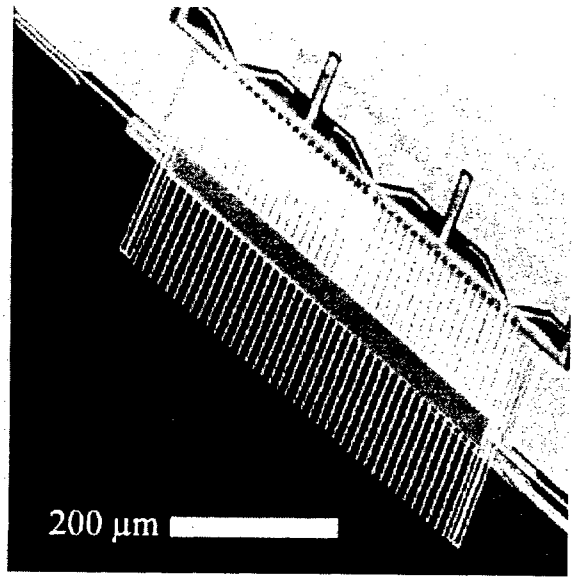

Figure 2: A comb structure fabricated in sputtered silicon. The wafer was cleaved beneath the structure after it was released in buffered HF.

Figure 3 shows an SEM image of spiral support hinges. The plates were protected by photoresist during the HF etch and are not completely released.

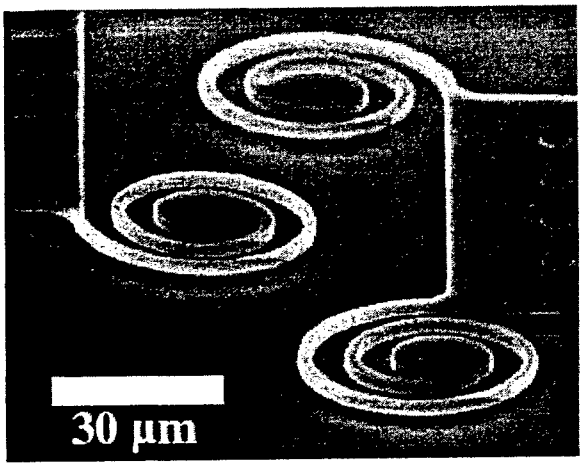

Figure 3: Released spiral support hinges anchored at the plates.

RESULTS AND DISCUSSION

The suitability of sputtered silicon for microstructures depends on several factors, including the ability to control stress, strain gradients, and conductivity. Additional factors may include surface roughness and density.

Average Stresses and Strains

Residual strain is one of the major issues for released surface micromachined structures. If the in-plane residual strains in doubly-supported structures are too compressive, the structures will buckle. This strain level is determined by the Euler buckling criteria for a doubly clamped beam:

$$\varepsilon_{cr} = \frac{\pi^2 t^2}{3l^2} \text{ for compressive strains} \qquad \text{(Eq. 1)}$$

where t is the film thickness and l is the beam length. To control strain, prior work [5] has subjected sputtered silicon to high-temperature (700 to 1000 °C) re-crystallizing anneals, much in the same way that they are used to control strain in LPCVD polysilicon. Unfortunately, these anneals make the approach incompatible with standard aluminum-metallized CMOS processing.

Strains in sputtered silicon were controlled here by adjusting deposition parameters. Table 1 shows the stresses, as measured by wafer curvature, in a set of 1 µm sputtered silicon films, sputtered at two powers and two pressures onto PSG. As can be seen from the table, all films deposited on PSG were tensile, thus avoiding the Euler buckling criteria altogether. In general, increasing the deposition pressure made the stress more tensile.

TABLE 1: Stress of Sputtered Silicon on PSG

Power \ Pressure	8 mTorr	14 mTorr
1.5 kW	97 MPa (Tensile)	106 MPa (Tensile)
2.5 kW	27 MPa (Tensile)	133 MPa (Tensile)

The substrate onto which the films are sputtered also plays a role in film stress. Table 2 shows the stresses in sputtered silicon films deposited on bare silicon at the same time as the samples deposited on PSG, above.

TABLE 2: Stress of Sputtered Silicon on Bare Silicon

Power \ Pressure	8 mTorr	14 mTorr
1.5 kW	34 MPa (Tensile)	141 MPa (Tensile)
2.5 kW	22 MPa (Compr.)	164 MPa (Tensile)

The average stress in many sputtered films has been shown to be a function of thickness [9], and of annealing [5]. Figure 4 shows the stresses in sputtered silicon films of varying thickness, both before and after annealing at 350 °C for 3 hours in forming gas (1:1, H_2:N_2). Each of these films was deposited at 2.0 kW and 9.5 mTorr.

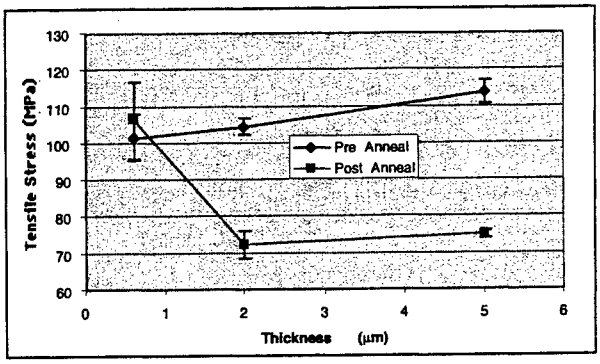

Figure 4: Average stress in sputtered silicon as a function of thickness before and after a 3 hour forming gas anneal at 350 °C. Bars indicate stress values of the two wafers run at each thickness.

The as-deposited stresses were a monotonically increasing function of thickness. After annealing, the stresses in the 2 µm and 5 µm samples became less tensile. The stress in the 0.6 µm samples were not significantly affected by the anneal. Thinner films would be more affected by surface effects or interfacial interactions with the substrate than thicker ones. This may explain why these thinner samples behaved differently than their thicker counterparts.

Strain Gradients

Strain gradients in released films impose important limitations in the overall maximum size of a device. The strain gradients in

the sputtered silicon films examined here were determined by measuring the curvature of released cantilever beams using an interferometric microscope (Zygo, Middlefield, CT.). Figure 5 shows the top surfaces of arrays of released cantilever beams. These structures were released without using the critical point method. In the upper image, the cantilever beams are 2.0 μm thick. The longest beam has been pulled down by capillary forces. In the lower image, the beams are 5.0 μm thick and all beams (up to 260 μm long) are freely released.

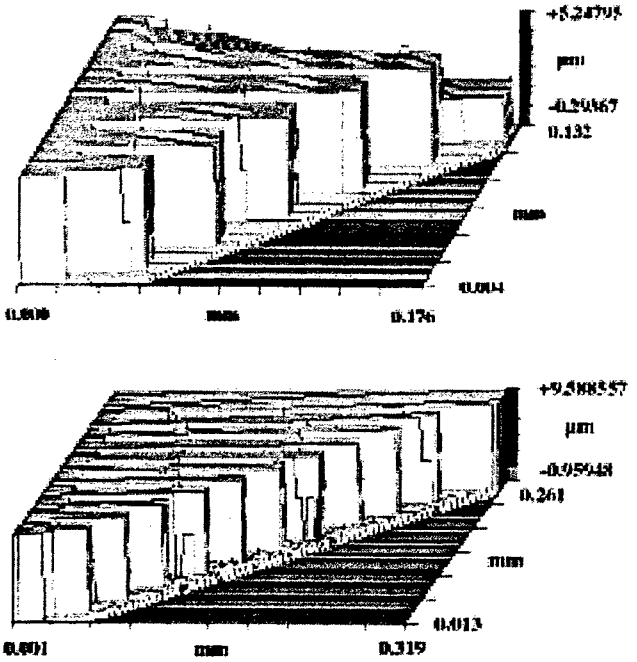

Figure 5: Surface data from an interferometric microscope. In the upper image, the beams are 2.0 microns thick and the longest beam (160 μm) has been pulled down by capillary forces. In the lower image, the beams are 5.0 μm thick and resist being pulled down up to lengths of 260 μm.

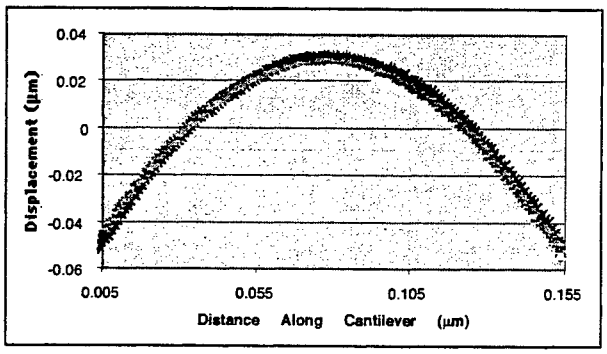

Figure 6: Curvatures of five beams from a single 5.0 μm thick array. The linear slope has been subtracted out of the deflection to only show the curvatures. In this case, the curvature radii average 35.0±0.8 mm.

Curvatures of adjacent beams are shown in Figure 6. Table 3 shows the released curvature radii from samples of varying thickness and the influence of annealing and the releasing etchant. Measurements were taken from at least five beams divided among at least three die sites.

TABLE 3: Released Cantilever Strain Gradients

Film Thickness	As-Deposited Radius of Curvature		350 °C Annealed Radius of Curvature	
0.6 μm	Pad	1.7±0.5 mm	Pad	3.8±0.8 mm
	20:1	2.9±1.0 mm	20:1	6.9±1.3 mm
	6:1	1.8±0.2 mm	6:1	2.5±1.2 mm
2.0 μm	Pad	18±6 mm	Pad	30±2 mm
	20:1	28±6 mm	20:1	-31±6 mm
	6:1	23±3 mm	6:1	29±3 mm
5.0 μm	Pad	27±3 mm	Pad	34±1 mm
	20:1	-30±4 mm	20:1	-112±25 mm
	6:1	47±4 mm	6:1	85±5 mm

For radii much greater than the film thickness, the average strain gradient in the released structures is merely the inverse of the radius of curvature and is seen to decrease with increasing thickness and annealing.

Surface Roughness

The average roughness of a film is an important consideration for bearing and optical surfaces. Figure 7 shows an AFM image of a 2.0 μm thick sample. The RMS roughness over a 1 μm square, is 3.1 nm.

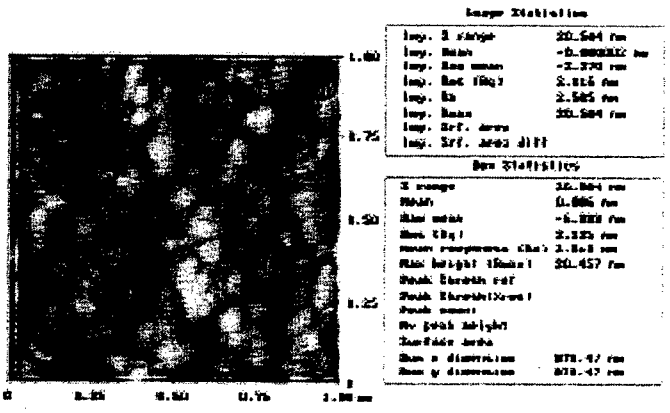

Figure 7: AFM image of an annealed 2.0 μm thick sputtered silicon film on 3.0 μm of PSG. The RMS roughness is 3.1 nm.

Table 4 shows the measured surface roughness of three wafers of varying sputtered silicon thickness, before and after annealing at 350 °C.

TABLE 4: RMS Surface Roughness

Film Thickness	As-Deposited RMS Roughness	350 °C Annealed RMS roughness
0.5 μm	4.2 nm	3.0 nm
2.0 μm	4.9 nm	3.1 nm
5.0 μm	5.9 nm	4.9 nm

Density

The density of the sputtered silicon was determined by measuring the difference between the pre- and post-deposition weights of the wafers. This difference was divided by the volume of the film. To maximize accuracy, the density was calculated using the results from the thickest films (5 μm). Based on the results from eight wafers, the density was determined to be 2.26 ± 0.08 kg-m^{-3}. This is comparable to single crystal silicon, which has a density of 2.33.

Electrical Resistivity

While passive microstructures may not need to be conductive, electrostatic devices require a minimum level of surface conductivity to function properly. That level is determined by the desired speed of operation and the physical dimensions of the device. Based on the Pi model for a distributed RC line, the electrical time constant (τ_{rc}) for a cantilever beam is approximately

$$\tau_{rc} = \frac{r_s \varepsilon_o l^2}{2\delta} \qquad \text{(Eq 2)}$$

where r_s is the sheet resistance, e_o is the permitivity of air, δ is the gap, and l is the length of the cantilever beam. A graph of the sheet resistance required to achieve a given time constant for a cantilever beam based on Eq. 2, is shown in Figure 8.

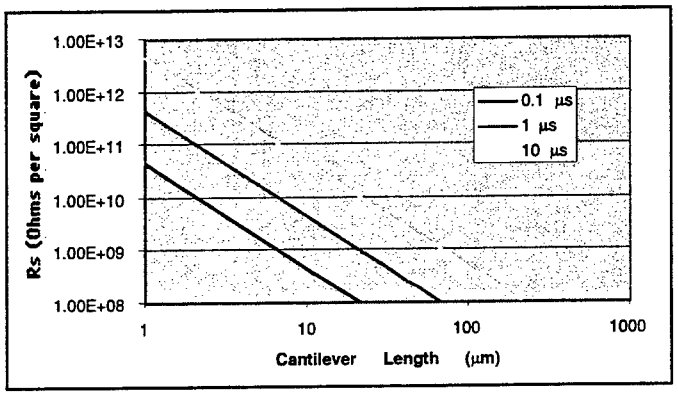

Figure 8: Sheet resistivity required to achieve time constants of 0.1, 1, and 10 μs, as a function of cantilever length.

Table 5 shows the resistivity of sputtered silicon for various film thicknesses. The resistivity was in the 10 MΩ/❑ range for the unannealed samples. After annealing, the resistivity increased significantly. This was confirmed by a separate anneal of a second wafer of each thickness. The mechanism of this increase is not completely understood, but is likely due to hydrogen passivation of intergranular dangling bonds.

TABLE 5: Sheet Resistance of Sputtered Silicon Films.

Film Thickness	As-deposited Resistance	350 °C Annealed Resistance
0.6 μm	50 MΩ/❑	125 GΩ/❑
2.0 μm	20 MΩ/❑	20 GΩ/❑
5.0 μm	7 MΩ/❑	6 GΩ/❑

For the annealed films especially, this level of resistivity would limit the speed of operation for a typically-sized micromechanical structure. When greater conductivity is required, the sputtered silicon can be clad with a thin layer of a film such as TiN, which is both conductive and resistant to HF.

PERMEABILITY

LPCVD polysilicon has been shown to be permeable to HF [10]. The same is true for sputtered silicon. Figure 9 shows an image of a 0.6 μm thick, 1 mm square, silicon membrane that has been pulled down by capillary forces after release in HF.

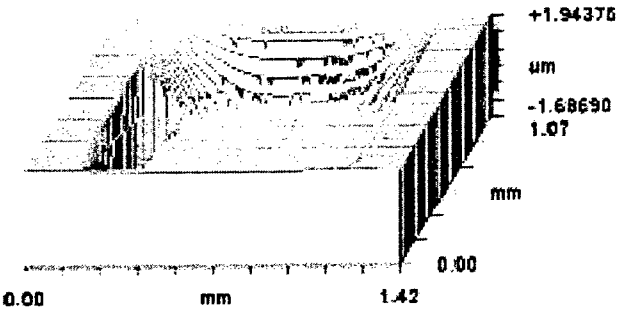

Figure 9: Image generated from interferometer data, showing pull-down of a 0.6 μm thick, 1 mm square, membrane.

During the release, photoresist completely encircled the pulled-down area and there were no lithographically-defined holes in the membrane to allow HF direct access to the underlying PSG. Samples of 0.6 μm, 2.0 μm, and 5.0 μm thicknesses were exposed to 20:1 buffered HF for 55 minutes, 6:1 buffered HF for 15 minutes, or Pad etch for 20 minutes (Pad etch attacks oxide about 20% slower than 6:1 buffered HF).

All samples except the 5 μm film in PAD etch showed evidence of porosity. Pad etch did show porosity in 5 μm

samples that had been etched back to 4 μm prior to release. Figure 10 shows an SEM cross-section of a 2 μm sample after release. The HF attacks the underlying PSG through the grain boundaries of the silicon [10]. Because sputtered films typically deposit columnar grains, it is not surprising that porosity was seen at thicknesses greater than the 0.2 μm demonstrated for LPCVD polysilicon.

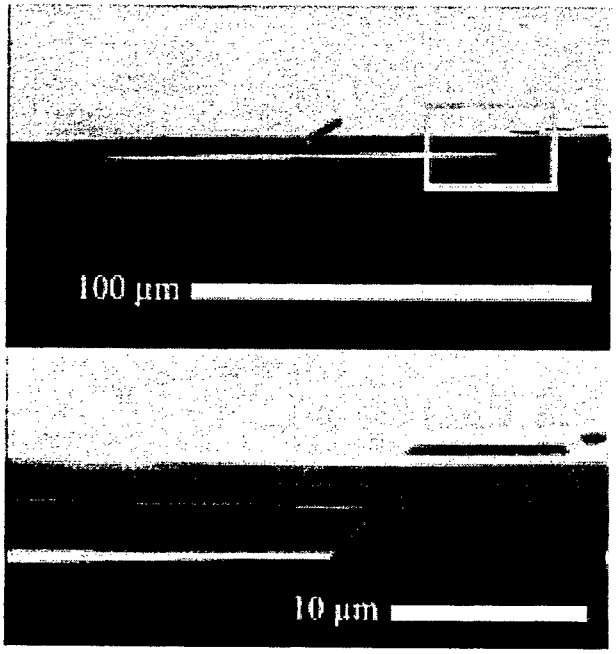

Figure 10: SEM image of a cleaved cavity formed by selectively masking the sputtered silicon with resist and exposing it to 20:1 buffered HF for approximately 1 hour.

During the release, however, several of the membranes were ruptured. This happened less frequently with the 0.6 μm samples, and with samples etched in 20:1 buffered HF. Osmotic pressure during the etch may be responsible for this, as reaction products may have a harder time passing through the sputtered silicon than HF. In any event, weaker solutions of HF should be used when etching thicker membranes.

Using the HF porosity of sputtered silicon, it is thus possible to form sealed cavities or channels by etching in HF and then coating with a nonporous film such as Si_3N_4. Sealing film leakage into the cavity should be minimal, since there need be no lithographically-defined etch holes.

CONCLUSIONS

Sputtered silicon can be used to make released microstructures at temperatures compatible with standard, aluminum-metallized CMOS. By adjusting deposition power and pressure, the stresses in the films can be controlled. Strain gradients in the released films decrease with increasing thickness. The surface roughness, on the other hand increases with increasing thickness. The surface roughness decreases, however, with annealing at 350 °C in forming gas. Annealing at 350 °C increases the resistivity of the sputtered silicon. HF porosity in the sputtered silicon provides an interesting alternative for making filters, microfluidic channels, or sealed cavity devices such as microphones or pressure sensors.

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SPUTTERED SILICON FOR INTEGRATED MEMS APPLICATIONS

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ABSTRACT

This paper describes a new fabrication process for creating electrostatic microstructures that are compatible with prefabricated aluminum-metallized CMOS circuitry. The process uses sputtered silicon to make released microstructures similar to those commonly made using LPCVD polysilicon but does so at much lower temperatures (~350 °C). The low-temperature nature of sputter deposition makes it possible to use polyimide sacrificial layers that can be released in an oxygen plasma. This dry-release process eliminates the need for critical point drying or similar methods. Average strain gradients in released sputtered silicon cantilevers were found to vary with the inverse square of thickness. At a thickness of 5.0 μm, the radius of curvature of released cantilevers was in excess of 80 mm. Improvements in the electrical conductivity of completed structures were realized by cladding the sputtered silicon structural layers in symmetric, 50 nm thick layers of titanium-tungsten. Underlying CMOS transistors showed no more than a 3% increase in their maximum saturation current after mechanical layer processing. As a demonstration of the integratibility of the sputtered silicon process, electrostatically actuated variable-capacitors were fabricated above CMOS capacitance detection circuitry.

INTRODUCTION

Integration is vital to the performance of many types of microsensors, since as dimensions decrease, sensitivity often falls off precipitously. The sensitivity of a torsional capacitive accelerometer, for example, scales as the fifth power of the lateral dimension. Large arrays of transducers also benefit from integration since the number of bondpads and the external circuitry needed to control each device can be reduced through the use of on-chip multiplexers.

LPCVD polysilicon has been the material of choice for most surface micromachined structures since the early 1980's [1] and has been integrated with on-chip circuitry for nearly as long [2]. Unfortunately, the high deposition and annealing temperatures of LPCVD polysilicon (~580-630 °C and >900 °C, respectively), have required either depositing metal layers after the polysilicon structural layers have been deposited in etched pits [3] or using refractory metals such as tungsten instead of aluminum for the circuits [4]. Both approaches increase the overall fabrication complexity and may require re-engineering the CMOS process to accommodate the new thermal budget, metal layers, and/or lithography changes.

In contrast, sputtered silicon can be used to fabricate released microstructures atop standard, aluminum-metallized CMOS at temperatures below 350 °C. By avoiding the temperature extremes of LPCVD polysilicon, greater flexibility is allowed in creating or selecting a circuit process, resulting in potentially significant cost-savings and performance advantages.

Most LPCVD polysilicon processes have used oxide sacrificial layers and wet-releases based hydroflouric acid (HF). Previous high temperature work on sputtered silicon microstructures [5] and our own low-temperature process [6] have followed in a similar vein. Figure 1 shows a sputtered silicon comb fabricated using an oxide sacrificial layer.

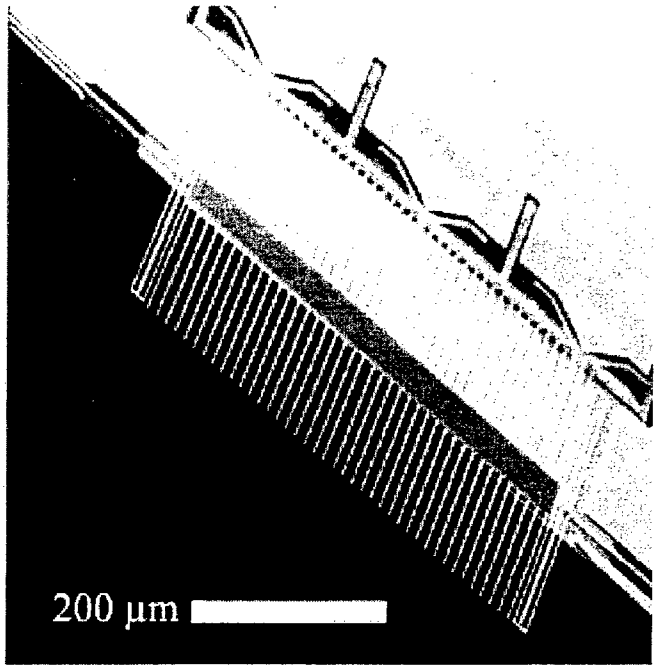

Figure 1: *A comb structure fabricated in sputtered silicon atop silicon dioxide. The wafer was cleaved beneath the structure after it was released in buffered HF.*

Investigating oxide sacrificial layers has led to an interesting discovery. HF porosity in sputtered silicon is evident at thicknesses far in excess of those reported for LPCVD polysilicon [7], making it a potential encapsulating material as well as a structural material. Figure 2 shows a buried cavity formed in an SiO_2 sacrificial layer underneath a 2.0 μm sputtered silicon layer.

One issue of concern is that the attack of the sputtered silicon during exposure to HF may weaken the film structurally. This is in addition to the problems associated with protecting the underlying CMOS during the release and capillary forces that can cause the structure to stick to the substrate if critical point drying [8] or self-assembling monolayers (SAMS) [9] are not used.

However, because sputtered films avoid the temperature excursions of LPCVD polysilicon, they are not only compatible with conventional oxide sacrificial layers, but also with organic sacrificial layers, such as polyimide. These organic layers can be removed in an oxygen plasma, thus avoiding the stiction and selectivity problems associated with wet releases and alleviating the concerns over chemical attack in HF.

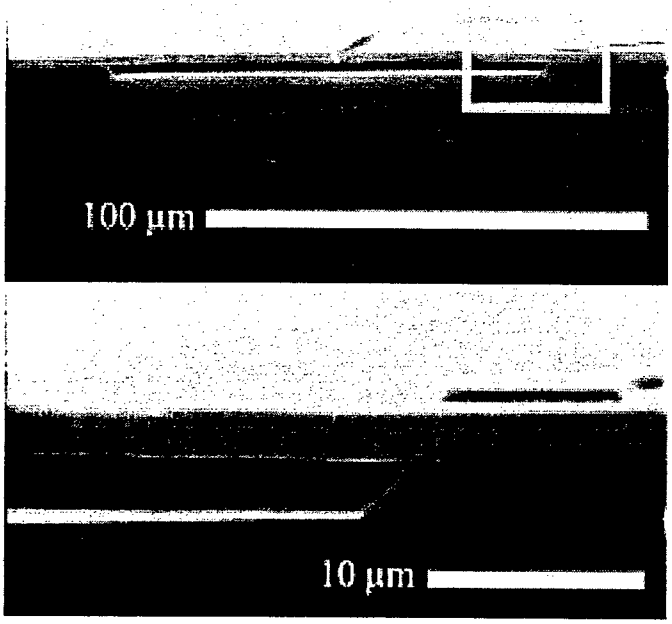

Figure 2: SEM image of a cleaved cavity formed in SiO_2 by selectively masking the top sputtered silicon layer with resist and exposing it to 20:1 buffered HF for approximately 1 hour.

DRY-RELEASED FABRICATION SEQUENCE

The basic process flow is illustrated in Figure 3 and begins with completed and tested CMOS circuitry. For convenience, the second metal layer of the underlying CMOS was used as the lower electrode layer for the mechanical structures. This electrode layer consisted of a bi-layer of 400 nm of aluminum and 100 nm of titanium. The titanium capping layer serves to minimize hillocking during the sacrificial polyimide cure cycle.

After patterning the lower electrode layer (Figure 3-a) and opening contact holes in the titanium over the bondpads, an adhesion promoter (*Dupont PIQ-13 coupler, Willmington, DE.*) was spun on and cured at 350°C for 30 minutes. Dupont PIQ-L100 polyimide resin was chosen for the sacrificial layer because of its low thermal expansion coefficient (3ppm/K) and clean release characteristics. This is in contrast to some other polyimides which, as a result of incorporating adhesion promoters within the resin, often leave behind a visible residue when etched in oxygen plasma. The PIQ-L100 resin was spun on for 30 s at 2200 rpm and cured at 350 °C for 1 hr. These spin parameters produced a polyimide film that was approximately 2.5 µm thick. Thicknesses were established using an optical measurement system (*Nanometrics, Sunnyvale, CA.*) which was calibrated relative to the results from a profilometer (*Veeco, Plainview, NY.*).

The polyimide was then etched back to 2.0 µm in oxygen plasma and coated with 200 nm of aluminum, which served as a hard mask. Etching back the polyimide both improved the adhesion of the aluminum mask and provided more precise control of the sacrificial layer thickness.

After patterning the aluminum mask (Figure 3-b), contact vias were etched in the polyimide using an oxygen plasma. The anisotropy of this etch was increased by reducing the pressure to the minimum practical limit of the plasma etcher (in this case, 100 mTorr). The photoresist used to pattern the aluminum mask was intentionally left in place to provide a more uniform loading during the etch. Care must be taken to avoid overetching the polyimide at this step, since once the resist and the polyimide in bottom of the vias is cleared away, the lateral etch rate increases significantly due to changes in loading.

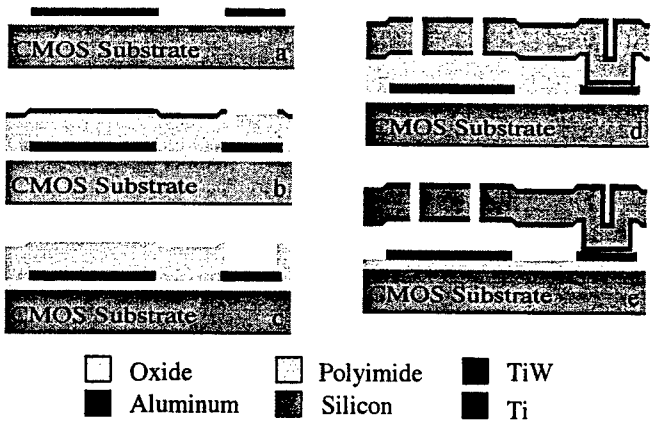

Figure 3: Dry release process flow incorporating conductive TiW cladding: Lower metallization (a); Polyimide sacrificial layer and patterned aluminum hardmask (b); Etched polyimide layer (c); Structural layer (TiW, Si, TiW tri-layer shown) (d); Oxygen plasma release (e).

During the course of the sacrificial via etch, the photoresist mask was etched away, leaving the aluminum mask exposed to the oxygen plasma. The oxidized aluminum mask was then removed by immersing the wafers in 50:1 HF for 10 s followed by a wet aluminum etch (Figure 3-c). This HF dip also helped remove any oxidized titanium from the bottom of the vias.

In order to improve the electrical contacts, the wafers were back sputtered in an argon plasma immediately prior to depositing the structural layer. This structural layer consisted of either 0.6 – 5.0 µm of boron-doped sputtered silicon or a tri-layer of 50 nm of TiW, followed by 2.0 µm of doped sputtered silicon and a second, symmetric, layer of TiW. By making the TiW layers symmetric, thermal bi-morph effects were minimized. Stresses in the films were controlled by varying the power and working gas pressure of the deposition. Films with stress values lower than 100 MPa were routinely obtained.

The TiW layers decrease the electrical resistivity of the resultant film significantly, as can be seen from Table 1.

TABLE 1: Comparison of electrical resistivity

Technology	Resistivity
Unannealed sputtered Si	6-50 x 10^6 Ω/□
Annealed sputtered Si	7-50 x 10^9 Ω/□
Sputtered TiW-Si-TiW	25 Ω/□

The wafers were annealed at 300 °C for 1 hr in a dry nitrogen ambient to sinter the contacts between the mechanical layer and the lower electrode and to stabilize the stresses in the structural layers.

The structural layers were patterned using an SF_6-C_2ClF_5 plasma (Figure 3-d). This chemistry etches both TiW and silicon

so there is no need for separate plasma steps when etching the tri-layer.

Following this etch, the wafers were diced and the individual chips were release in an oxygen plasma. The release etch took approximately 4 hrs to undercut 15 μm at an input power level of 200W and a pressure of 3 Torr (Figure 3-e). Release times could be decreased by using a more aggressive plasma etcher, but circuit damage may become a concern.

STRAIN GRADIENTS

Control of warping in released structures is a major concern during microstructure fabrication. This warping is caused by the presence of residual strain gradients throughout the thickness of the structural layer. The sputtered silicon in this work was not completely free of these strain gradients, as evidenced by the curvature of the released cantilevers in Figure 4. However, the gradients were observed to be a strong function of film thickness, with thicker films having smaller average values for the gradient. At a 5.0 μm film thickness, the average radius of curvature of a cantilever beam was in excess of 80 mm.

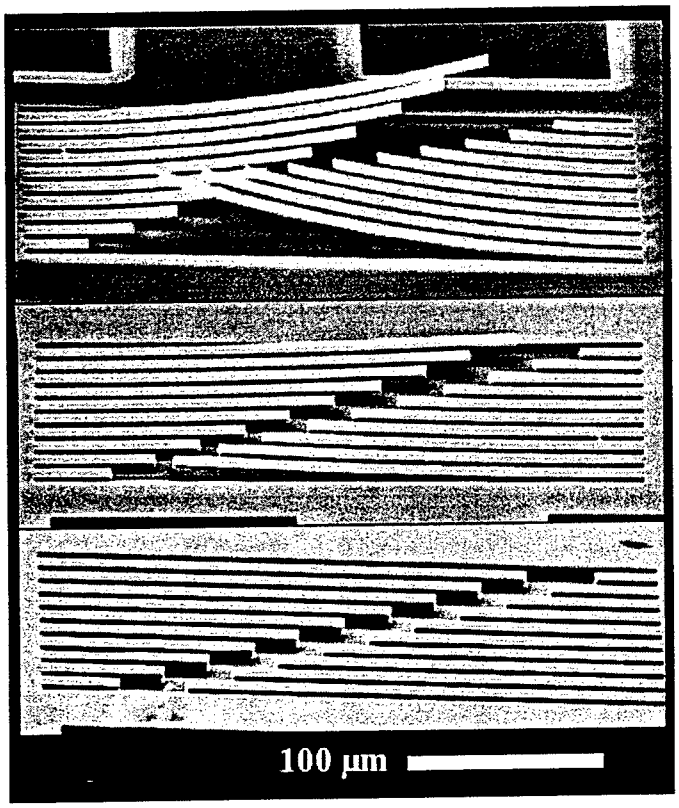

Figure 4: Dry-released pure sputtered silicon cantilever beams. The top set of beams is 0.6 μm thick. The center set is 2.0 μm thick. The bottom set is 5.0 μm thick and has the least curvature. All beams were released in a 1.3 W/cm² oxygen plasma.

Figure 5 shows data from interferometer scans of six cantilever arrays which appears to match a theoretical curve based on surface strains as the dominant contributor to the gradient. The moment caused by these proposed surface strains is proportional the thickness of the film and acts against the stiffness of the cantilevers which is proportional to the cube of thickness. The radius of curvature is thus proportional to the inverse square of the thickness in this model.

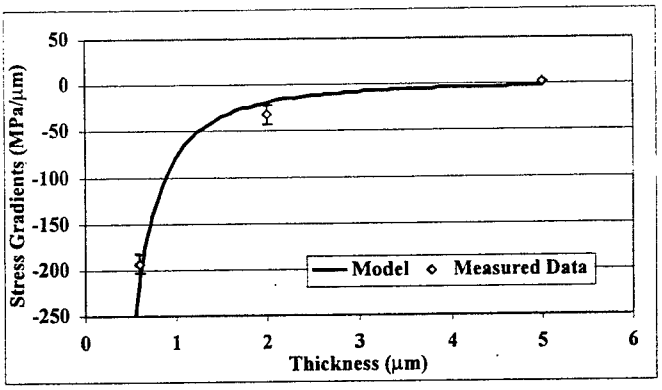

Figure 5: Sputtered silicon stress gradient as a function of thickness for dry-released cantilever beams Each data point represents typical beams from six arrays. Error bars represent two standard deviations. The solid line represents a theoretical curve based on surface effects, which are postulated to dominate the stress gradients in the films.

The TiW layers used to increase the conductivity of the sputtered silicon can also be used to adjust the curvature of the released structures. By adjusting the stress in the top layer to be more compressive, the released structures can be made more convex. Similarly, by making the stress more tensile, the structures can be made more concave.

CMOS COMPATIBILTY

As expected, the post-CMOS fabrication steps have little measurable effect on the underlying CMOS circuitry. Figure 6 shows transistor curves from transistors fabricated at the Stanford University Center for Integrated Systems before and after the mechanical layer processing. Out of the 30 NMOS and PMOS transistors measured, none showed more than a 3% change in maximum saturation current.

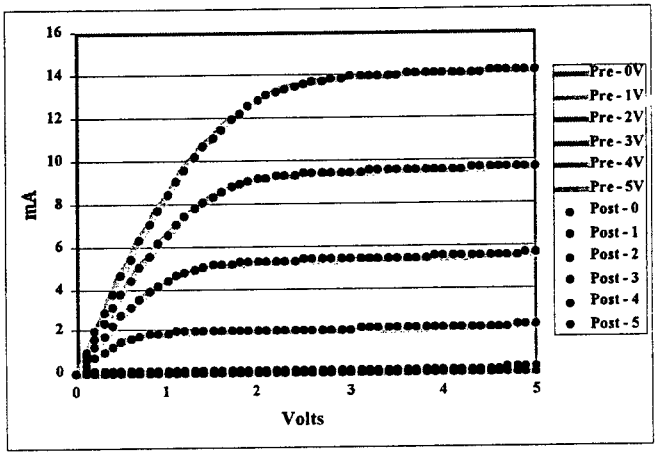

Figure 6: NMOS transistor curves before and after mechanical layer processing. Not more than a 3% increase in maximum saturation current was observed in any of the 30 nmos or pmos transitors tested.

Some of this change can be attributed to sintering of the contacts during the curing and annealing steps since no barrier layers were used between the silicon and the Al-1%Si metallization layers.

INTEGRATED VARIABLE CAPACITOR

As a demonstration of the process, TiW-clad sputtered silicon was used to create variable capacitors with integrated capacitance detection circuitry. This type of device was chosen because most integrated surface micromachined sensors operate using some variation on capacitance detection. Figure 7 shows an optical scan of one such device, an array of 100 μm plates, each suspended by four springs. A simple buffer circuit, with a reset switch to control charging, was used to measure changes in capacitance caused by electrostatically deflecting one set of capacitors. For small deflections, the relationship between deflection, capacitance change, and the output voltage should be linear.

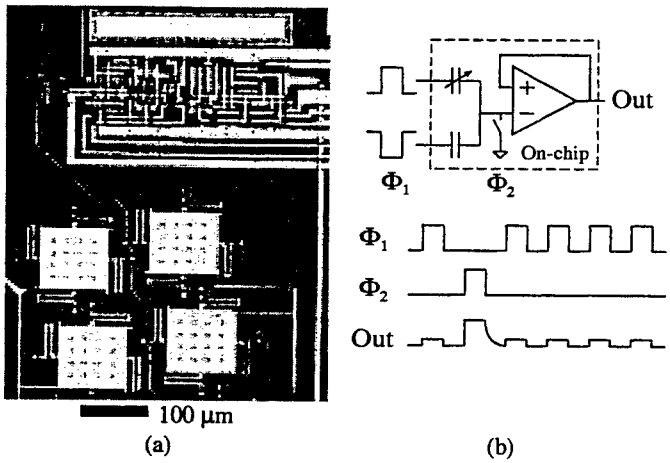

Figure 7: Variable capacitors with integrated detection circuitry. (a) An optical image of the two reference and two variable capacitors next to the capacitance detection circuit. (b) Schematic representation of the capacitance detection scheme.

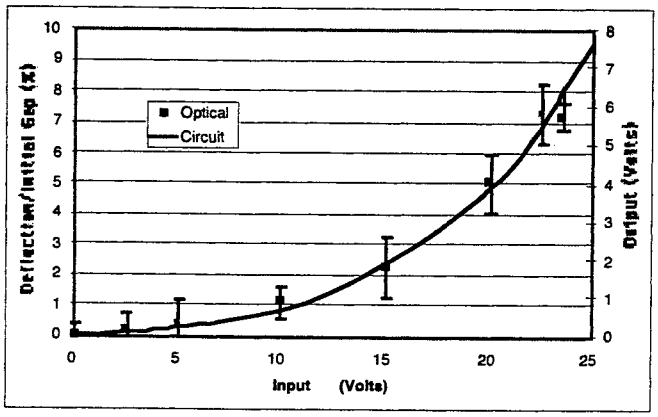

Figure 8: Deflection as a function of voltage for a 100 μm square variable capacitor. The solid line shows the output of on-chip capacitance detection circuitry. The discrete points show the deflection as measured by six scans of an interferometric microscope. Error bars represent the standard deviation.

Figure 8 shows a graph of the amplified output of the capacitance detection circuit and the deflection of the plates, as simultaneously measured by an interferometer. The measured deflection and circuit output correspond to each other, indicating that the circuit is transducing as expected.

CONCLUSIONS

Sputtered silicon is a promising material for integrated microstructures. When clad in TiW, the resistivity is only 25 Ω/ □. The radius of curvature of released structures depends on the film thickness and can be made lower by using thicker films or by tailoring the stress in the TiW cladding layers. Curvature radii in excess of 80 mm were demonstrated with 5.0 μm thick samples. The process does not adversely affect threshold voltage or saturation currents of underlying CMOS transistors. Because the sacrificial layer is removed in an oxygen plasma, there are none of the stiction problems associated with wet-releases. Finally, the TiW-clad sputtered silicon process can be used to make many of the same types of devices currently made using LPCVD polysilicon.

ACKNOWLEDGEMENTS

The authors would like to thank Chris Storment and Elaheh Sigari for their assistance during fabrication. Funding for this work was provided by the DARPA Composite CAD Program (Contract #F30602-96-2-0308-P0001).

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A Novel Method to Utilize Existing TCAD Tools to Build Accurate Geometry Required for MEMS Simulation

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ABSTRACT

This paper details a technique that exploits domain decomposition and utilizes a combination of 1-D, 2-D, and 3-D process simulation to build physically accurate geometry of micro-electro-mechanical systems (MEMS) for simulation. The size and aspect ratios of typical MEMS structures differ significantly from those traditionally found in the VLSI community. This spatial stiffness makes it difficult to construct a geometry model using standard process simulation tools. The domain decomposition technique is an automated process that uses process flow, mask layouts, and a set of heuristics to determine which regions on the wafer require 1-D, 2-D, and 3-D simulation. The appropriate order of simulation is then performed and the results are automatically combined to create a useful geometry which can be used for simulation of behavior.

Keywords: micro-electro-mechanical systems (MEMS), geometry, process simulation.

INTRODUCTION

In the MEMS field, it is becoming widely accepted that representing the 3-D geometry of devices is critical for simulation based design. Many commercial and academic systems for MEMS analysis rely on purely geometric operations to create the structures. Notable examples include MEMCAD, Intellicad, and Solidis [1]. While tools exist for creating geometry for the VLSI community, there are unique challenges posed by MEMS. Modeling challenges include the size (and aspect ratios) of typical structures, residual stresses which create initial curvature in ideally flat devices, and effects of the materials used.

The typical dimensions of MEM switches (such as fabricated using the MUMPS process) are on the order of several hundred microns in length, a width on the order of 1/10 the length, and thicknesses of only several microns. These dimensions cause significant problems for deposition and etching process simulators such as SPEEDIE [2]. If full 3-D simulations are performed, it would take excessive amounts of computing resources including time and memory which exceed current limitations of software and hardware. In addition, due to some of the features of typical devices, much of the device does not gain geometric accuracy from 3-D simulation compared to using 2-D typical cross-sections. This means an intelligent process must be undertaken to reduce the massive amount of data from a complete 3-D simulation to the geometric representation of practical use for device simulation. In this paper a novel method is demonstrated which utilizes existing tools in a computationally efficient method to achieve accurate and practical geometry.

OVERVIEW

The process of building a solid model representing a deposited layer of material has been divided into three basic steps to reduce the computational cost and permit the use of widely available process simulators:

1) Decompose the domain into 1-D, 2-D, and 3-D simulation regions.

2) Perform the appropriate simulations in each region.

3) Combine the resulting simulations together to create a final 3-D solid model.

DOMAIN DECOMPOSITION

Starting with a process flow and the layout masks, a geometry is created using conventional geometric operations. When a more precise representation of a layer (such as a layer of polysilicon to be used as the main structural component for actuation) is desired, the geometry is decomposed into 1-D, 2-D, and 3-D regions of simulation (Fig. 3). Since it would be difficult and computationally intensive to use the 3-D geometry of the device to determine the regions of simulation, the etch masks are used along with knowledge of the process flow. There are four major steps in the domain decomposition algorithm:

1) Create a uniform two-dimensional grid to cover the wafer.
2) Classify each box as a 1-D, 2-D, or 3-D simulation region.
3) "Grow" the classified regions using heuristics.
4) Merging similar adjacent regions.

Step 1 - creating a uniform grid

First, a tensor product (rectangular) grid is created using the deposition thickness (defined as the total thickness of deposition on a flat surface of the current step) rounded up to the nearest integer as the grid size. To be precise, "grid size" actually refers to the height and width of each individual box, and thus the total number of boxes is given by:

$\eta = ceil(l\ w\ /\ ceil(g)^2)$ where: η = total number of boxes (integer), l = length (float), w = width (float), g = grid size

(float), and ceil(x) = function returning the smallest integer not less than x.

Step 2 - classification of each box

The next step is to loop over the η boxes and determine the nature of the simulation required in each box (see Figs. 1 and 2). It is important to note that in the case when multiple etch masks have been used to create the surface topography, a simple superposition of the masks is used. The assumption here is that regions requiring higher dimensional simulation (2-D or 3-D) can only occur within a given distance (which will be called δ) of the edges of the etch masks. Physically, this makes sense because the effects of a feature, e.g. a stepup, will only be felt in the local area of the feature on the wafer and deposition a "reasonable" distance away will be unaffected. Based on numerical experiments and empirical results, δ is assumed to equal to the deposition thickness for the current step. In the case of a wafer that undergoes multiple (repeated) depositions utilizing the domain decomposition technique, δ is the sum total thickness of all of the relevant deposits. It is believed that this is a conservative estimate (i.e. upper bound) of the effects of a given feature and appears to be the case in practice.

Step 3 - growth of 2-D and 3-D regions

The next step in the process is to grow the 2-D and 3-D simulation regions appropriately. The best way to justify this step is by example. Take a hypothetical box from above which contains a corner and has been classified as a 3-D simulation region. Now, assume that the corner occurs at an extrema of the box, such as the lower left hand corner. By the classification procedure in step 2, the box may have as its left neighbor a 1-D box (see Fig. 4). This is incorrect because the assumption was that the feature (i.e. corner) has an effect in a region of influence given by δ. One possible course of action to handle this problem might be to query each 2-D and 3-D box to gain additional information about the exact feature contained within. The drawback is that this would require handling many special cases. A simpler procedure, which was implemented is to create a safety zone around each 2-D and 3-D simulation region.

In general, the etch mask edges may be in arbitrary directions. The current implementation handles only Manhattan style etch masks. Thus, for a 2-D box containing a "vertical" etch mask edge, its adjacent neighbor box to the left and right are converted to 2-D if either were 1-D. For a "horizontal" etch mask edge, its adjacent neighbor box above and below are converted to 2-D if either were 1-D. For 3-D boxes, all eight of the adjacent neighbors are converted to 3-D (see Fig. 4).

Step 4 - Combining adjacent 2-D and 3-D regions

Finally, adjacent boxes of the same order are combined to yield rectangular simulation regions of a given order. For the 1-D and 2-D regions this is a straight forward procedure. In the 3-D case, however, it is more complicated because initially separate 3-D regions might be touching after the growth detailed in step 2. An efficient contour tracing algorithm is used to find the largest possible 3-D region (i.e. bounding box) by combining interacting or nearly interacting 3-D regions (see Fig. 4). The major motivation to have the rectangular 3-D simulation regions is that it greatly simplifies several procedures (such as the pseudo-3D technique described below) without significant cost penalty.

PERFORMING THE SIMULATIONS

For the 1-D regions, the deposition thickness has been user specified in the process flow, and this results in planar surfaces in the 1-D regions. In the 2-D regions, a 2-D process simulator [2] is used to predict the geometry. Surfaces are created by effectively extruding the 2-D profile in the appropriate direction to yield a 3-D surface. For the 3-D regions, two methods are being explored. Currently, we utilize 2-D process simulations to create pseudo 3-D geometry as detailed in [3][4]. Since the size of the area that requires 3-D simulation has been minimized by the domain decomposition, the use of commercial 3-D topography simulators is also being investigated.

RECONSTRUCTION ALGORITHM

After the process simulations have been run to create the geometry, the results have to be recombined to create a continuous deposition surface. Currently, the method implemented is to create a solid from each simulation region and then union (Boolean addition) all of the solids together to create the final 3-D geometry (Figs. 5 and 6). The motivation for the current implementation is its simplicity. However, robustness issues (predominantly with tolerancing) within the solid modeler have increased the need and efforts to search for more alternatives in combining the data. One method which holds great promise being explored is to "sew" the surfaces together thus creating a boundary surface which can be used to create to final solid.

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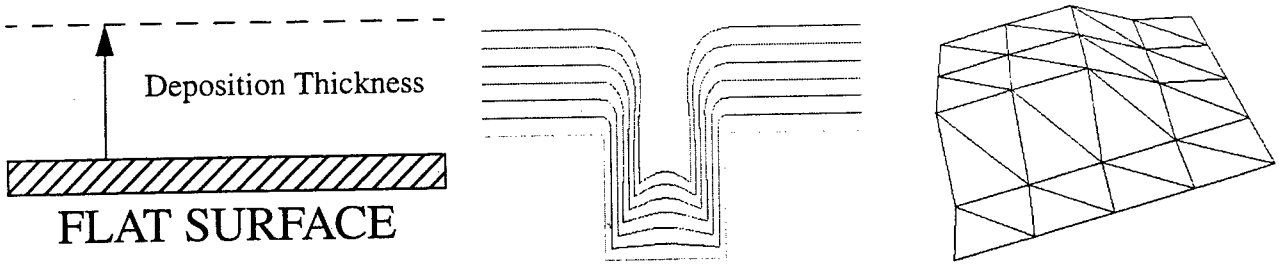

Fig. 1: The definition of process simulation regions. (a) 1-D. (b) 2-D. (c) 3-D. The 1-D regions require only a thickness specification, 2-D regions require SPEEDIE simulation, and 3-D regions need either the pseudo-3D technique or the use of a 3-D process simulation.

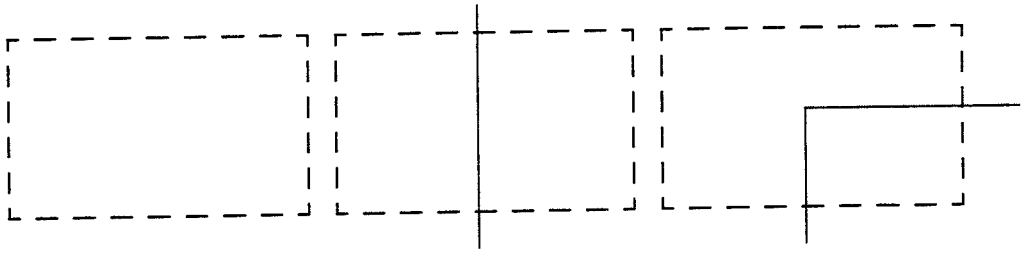

Fig. 2: The 3 possible cases in the domain decomposition of the masks. (a) no line segments inside of the box, indicates a 1-D region. (b) one line segment inside of the box, indicates a 2-D region. (c) two or more line segments indicating a 3-D region.

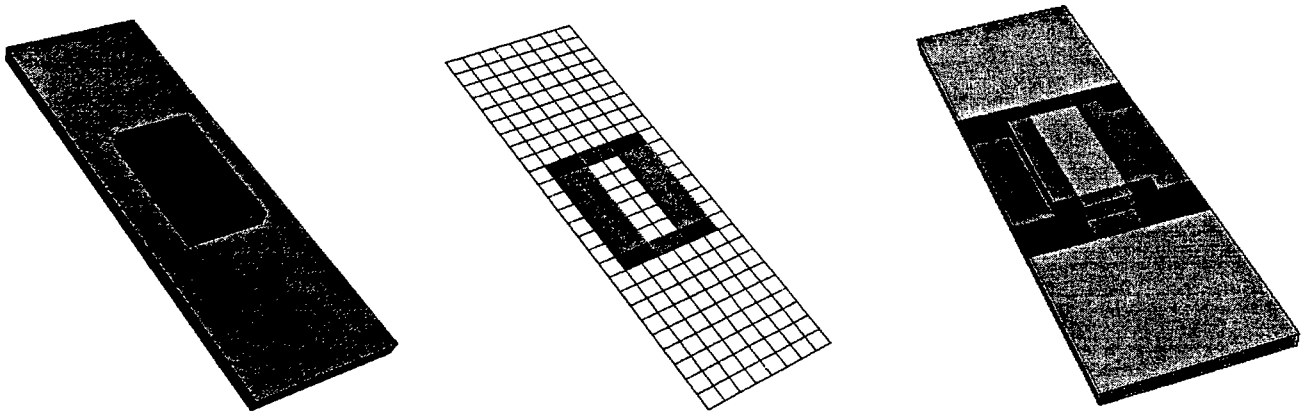

Fig. 3: The domain decomposition of a simple surface. (a) shows the original geometry. (b) domains based on etch masks used to create geometry. (c) the regions of simulation where cyan is 1-D, green is 2-D, and red is the 3-D domains.

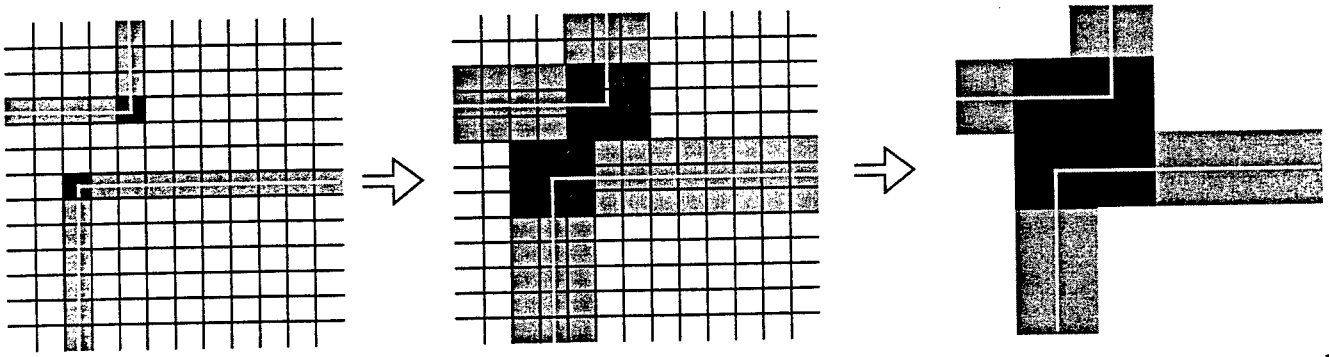

Fig 4. Domain decomposition algorithm. The yellow lines are etch mask edges, 3-D boxes are red, 2-D boxes are green, and the rest are 1-D boxes. (a) On the initial grid, classify the boxes. (b) Grow the 2-D and 3-D boxes. (c) Merge the 2-D boxes and 3-D boxes into 2-D regions and 3-D regions, respectively. The remaining white area is the 1-D region merged region.

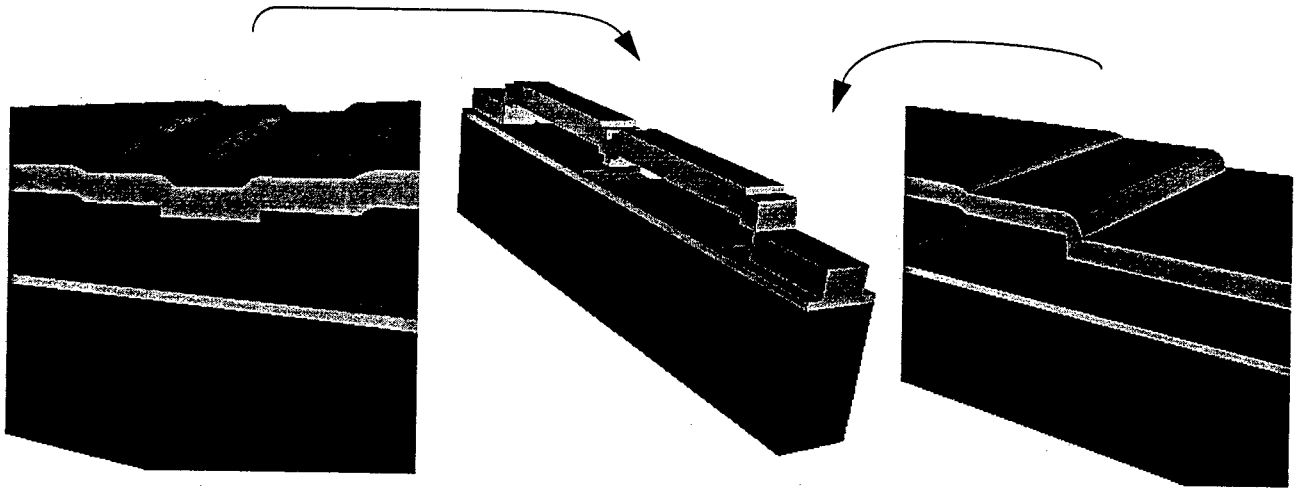

Fig. 5: Two electrode switch built using the domain decomposition technique utilizing a combination of geometric etches and physical depositions. (a) A close-up of the center of the switch. (b) 3-D view of the geometry. (c) The stepup.

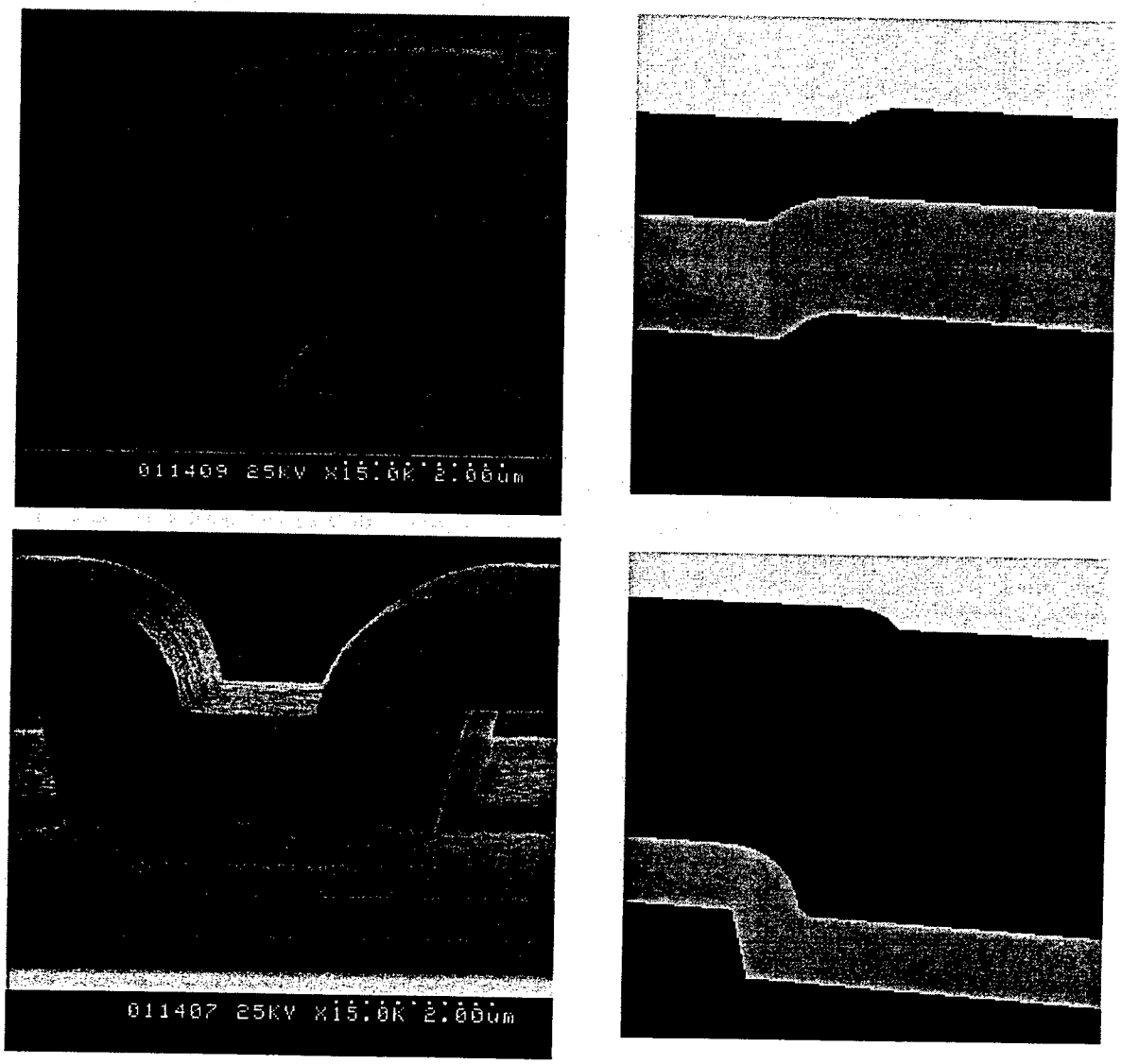

Fig. 6: On the left are two SEMS of an actual switch fabricated in the MUMPS process (see E. K. Chan et. al., MSM99), while on the right are two images of the solid model (see also Fig. 5). Notice the effects of conformal deposition on the final geometry.

GEODESIC: A New and Extensible Geometry Tool and Framework with Application to MEMS

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ABSTRACT

This paper will detail the capabilities of a new geometric modeling tool, called Geodesic, which is being released in source code form to the general community. In addition to providing geometric operations to create geometry useful in MEMS simulation, it uniquely offers a fully integrated 3-D levelset kernel that permits highly accurate physically based deposition and etching simulation.

Keywords: Geometry, MEMS, solid modeling, levelset, TCAD.

1.0 INTRODUCTION

In the field of microsystems, numerous commercial and academic efforts are underway to develop simulation based design (SBD) systems [1]-[5]. Most of these systems consist of closed, proprietary frameworks. This is a disadvantage to the typical designer since it is unlikely that one system can provide all of the desired functionality. In addition, for researchers in the fields of geometric modeling, mesh generation, and numerical simulation, this can complicate and hinder the process of developing new tools.

Interest in automating 3-D geometry construction, using only mask and process information, for VLSI and MEMS applications has been actively pursued for nearly two decades. These efforts can be lumped into two basic catagories: those that utilize commercial solid modeling kernels and efforts based on proprietary code to represent solid models. Examples of the latter include OYSTER [6], 3DTOP [7], and MemCel [8]. Efforts using commercial solid modeling kernels include VIP3D [9] and MemBuilder [10] (the current mechanism used to build geometry in the commercial system MEMCAD [1]). Geodesic falls into this second category.

Geodesic is an effort to increase the interoperability between existing tools by providing an extensible framework for creating geometry suitable for the simulation of MEM devices. Its unique feature set consists of a generic solid modeler interface, user-selectable algorithms for etch and deposition that achieve multiple levels of physical accuracy, and a fully integrated multi-dimensional levelset kernel.

2.0 GEODESIC FRAMEWORK

The input to Geodesic consists of a set of masks (defined in a CIF file) and a process flow (specified using the Composite CAD Process Definition Specification [19]). The geometry is then built in a layer by layer fashion by emulating and/or simulating the processing steps used to build the actual device (i.e. "virtual fabrication"). Currently only geometric steps (e.g. depositions and etches) are supported. Fabrication steps such as implants and diffusions are not modeled within the Geodesic framework.

Figure 1 shows a schematic of the Geodesic architecture. The challenges of integrating diverse tools such as solid modelers and mesh generation software into a unified framework involves tasks of varying computational expense and algorithmic challenge. In addition, in a research setting it is desired to have a tool which permits rapid prototyping and quick testing of new algorithms. For this reason, Geodesic uses Tcl/Tk as a front-end integration environment. Tcl/Tk combines the ease of a powerful scripting language with the ability to imbed C/C++ code for computationally intensive operations. There are four main modules in Geodesic: the object repository, the solid modeling interface, the levelset kernel (section 3.3), and the meshing interface (section 4).

2.1 Object repository

The object repository is a simple hash table of names (character strings) with corresponding object pointers. The repository allows for the basic operations of adding, deleting, listing, and querying of object type. This layer does not know or care about the underlying structure of the objects contained in it, it merely returns the pointers and calls instantiation and deletion methods as required.

2.2 Generic solid modeler interface

At the heart of geometric modeling is a solid modeler. By wrapping the solid modeling function calls used in generic interface layer, Geodesic can be used with multiple solid

modeling kernels. This interoperability with multiple kernels is facilitated by designing the system to minimize the number of distinct function calls required to build a geometry. The current implementation can be used with two different commercial solid model kernels (Shapes [11] and Parasolid [12]). So far, only limited results have been achieved using a freely available solid modeler (IRIT [13]). The extension of Geodesic for use with other solid modelers (e.g. ACIS [14]) should be straight forward.

3.0 ALGORITHMS TO ACHIEVE MULTIPLE LEVELS OF PHYSICAL ACCURACY

State-of-the-art commercial MEMS simulation tools rely on purely geometric operations to create geometry. In addition to an efficient and robust method to create geometry using only solid modeling operations, Geodesic provides the capability to smoothly incorporate physically based 2-D and 3-D deposition and etching process simulation results into the geometry.

3.1 Geometric algorithm

An efficient geometric deposition algorithm has been developed. The algorithm provides for surface angle dependent deposition thickness to allow for non-uniform sidewall and step coverage. The algorithm operates independent of the solid modeler and utilizes standard functionality provided in the Visualization Tool Kit [15]. Briefly, the steps of performing a deposition consist of:

1. Extract a faceted representation of the exterior of the current state of the wafer (this corresponds to creating a vtkPolyData file of the exterior).
2. The vtkPolyData object is then preprocessed by three VTK filters. First, the duplicate points inside of the data file are eliminated (vtkCleanPolyData). Then, all polygons are decomposed into triangles (vtkTriangleFilter). Finally, the facets are consistently oriented (vtkPolyDataNormals).
3. The bottom of the wafer is detected (this is currently done by assuming that the bottom of the wafer lies in plane z=0). The facets corresponding to the bottom and the sides of the wafer are then fixed so deposition only occurs on top of the wafer. The sign of the outward normals is determined by checking the orientation of the bottom facets.
4. For each facet, the position of a corresponding infinite plane is calculated by translating and rotating the plane as a given function of the initial orientation of the facet. In the case of isotropic deposition, this corresponds simply to translating the plane in the outward normal direction by the given deposition thickness.
5. The vertices of the model are then looped over and at each vertex the intersection of the infinite planes meeting at the vertex are calculated. There is additional code to handle the special cases of adjacent coplanar facets and free edges.
6. Once the new vertices are calculated, the topology is copied from the original vtkPolyData object and a new vtkPolyData object is created which corresponds to the exterior of the geometry after the deposition. The

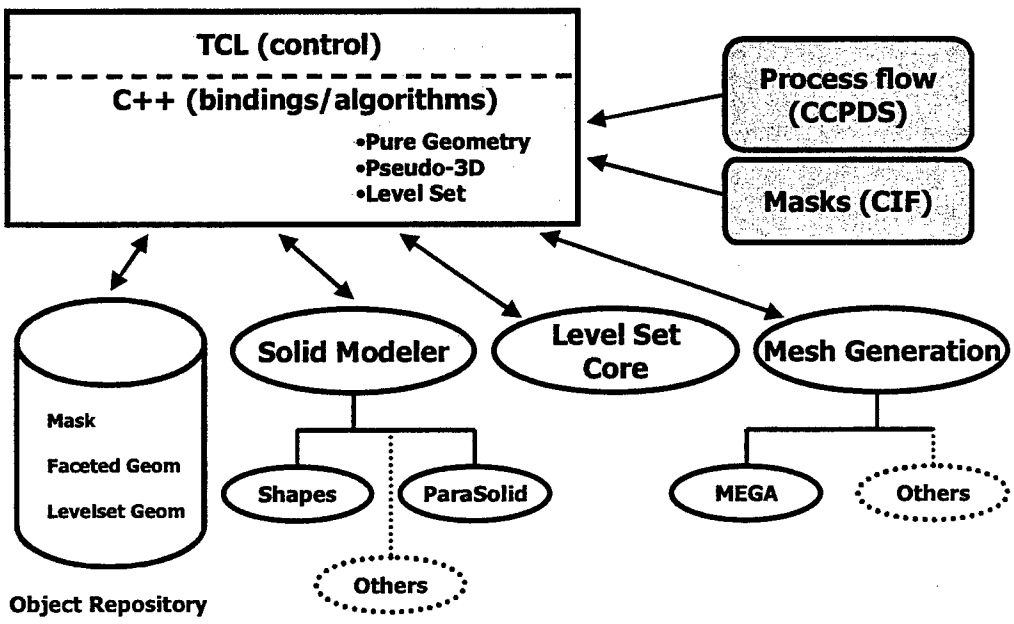

Figure 1: Geodesic Architecture.

vtkPolyData object can then be used to create a solid model.

7. The material deposited for this given step is calculated by subtract the original geometry (step 1) from the final geometry (step 6).

Figure 2 shows a comb drive created using the geometric algorithm to create the conformally deposited layers.

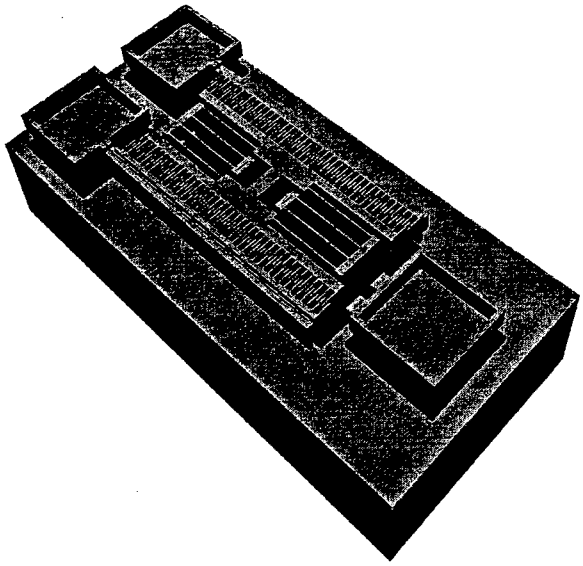

Figure 2: Comb Drive created using geometric operations inside of Geodesic.

3.2 Domain decomposition

To improve the overall efficiency, complex structures are decomposed into regions identified as needing 1-D, 2-D, or 3-D process simulation. Different geometric and physical approaches to geometry manipulation can be arbitrarily applied among these regions. This technique is detailed in [16]. Figure 3 shows a dual electrode switch created using the domain decomposition.

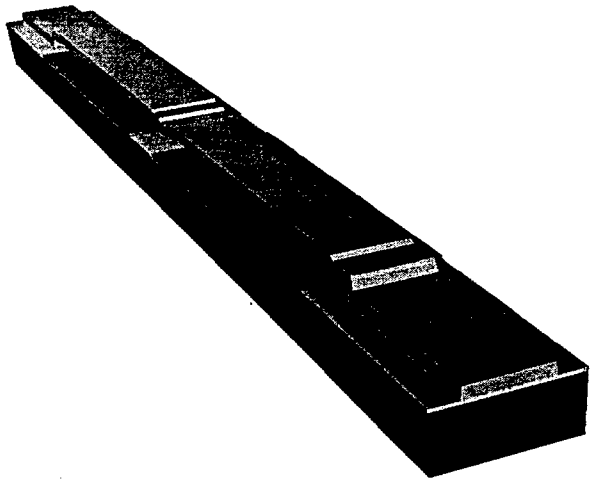

Figure 3: Dual electrode switch created using process using 2-D process simulation, domain decomposition, and geometric operations.

3.3 Levelset process simulation

Geodesic contains a fully integrated general multi-dimensional levelset kernel which can be used for process simulation. The level set method has been shown in [17] to be useful for modeling surface movement in back-end wafer processing. The Geodesic framework incorporates a numerical module for performing 2- and 3-D level set calculations. The integration of this module with the rest of the Geodesic system enables level set based modeling to be done in conjunction with the other geometric techniques described above. Figure 4 shows a two-layer corner structure undergoing material-dependent etching. Dynamic grid reduction techniques based on those described in [17] are used to lower the computational cost of level set calculations.

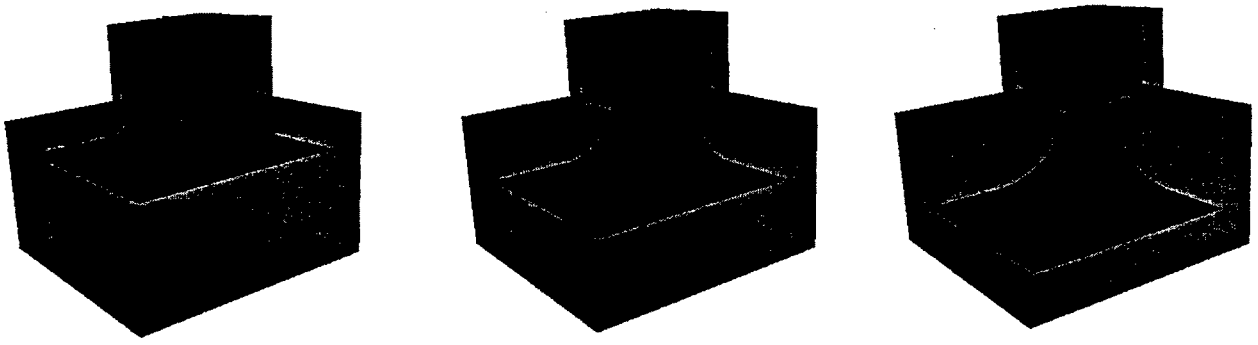

Figure 4: Example of a selective corner etch using the integrated 3-D Levelset kernel in Geodesic. The figure shows three steps in the evolution of the boundary surface, where the red surface indicates the level zero function. As can be seen, the small block on top of the larger block is more resistive to etch.

4.0 MESH GENERATION

Geodesic also contains a generic meshing layer. In the current implementation, only the MEGA automatic mesh generation package [18] is supported. Its functionality includes "meshing through the thickness," which is useful in the simulation of thin material layers frequently encountered in MEMS. It also possesses special boundary layer meshing capabilities useful in microfluidics. Figure 5 shows a coarse mesh of a micromirror, while Figure 6 shows the mesh of a simple switch with refinement near the stepup. Please note, the source code for MEGA will NOT be provided with Geodesic (contact [18] for details about obtaining the SCOREC meshing tools).

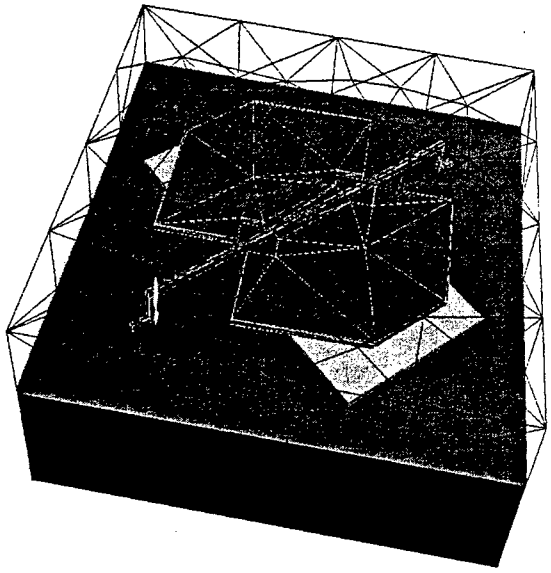

Figure 5: Meshed micromirror.

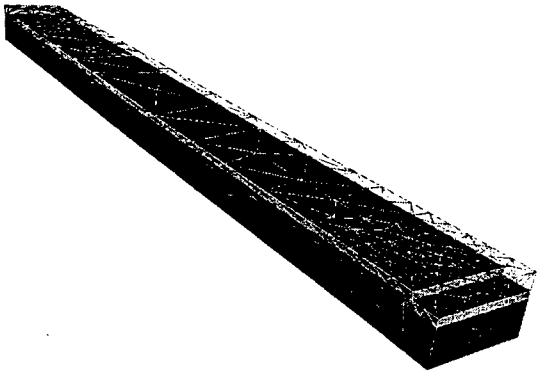

Figure 6: Simple switch with mesh refinement.

FUTURE WORK

Future work on the geometric algorithm will include enhancements that detect and avoid many of the solid modeling related difficulties with small features such as release holes and dimples. Work on levelset performance enhancements is also on-going.

ACKNOWLEDGEMENTS

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