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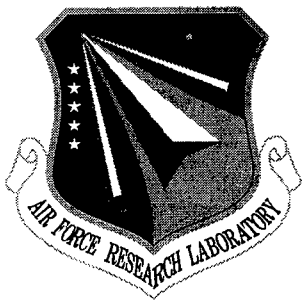

10GBYTE PERSONAL MULTIMEDIA MEMS ROM DATA STORAGE CARD

Kionix, Inc

Sponsored by
Defense Advanced Research Projects Agency
DARPA Order No. E117

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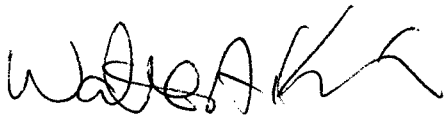

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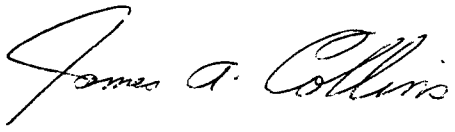

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10GBYTE PERSONAL MULTIMEDIA MEMS ROM DATA STORAGE CARD

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13. ABSTRACT *(Maximum 200 words)*

The goal of this project was to create a two-chip MEMS read-only memory data storage device using single-crystal silicon based actuators. The read head of the ROM is composed of a parallel array of atomic force microscope tips each mounted on a small element size torsional cantilever. An xy microstage containing the data bits is mounted beneath the tips and actuated or scanned, analogous to the rotating magnetic disk for conventional drives. The number of interconnects required for the large displacement stage is minimized, reducing the level of complexity required in the fabrication. Control electronics are needed to drive the stage, sample the small deflections of the torsional cantilever, and buffer the data from the individual probes. The first full storage systems based on MEMS silicon actuators were fabricated, assembled, and tested.

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Project Goals:

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Accomplishments: Jan 1, 1999 - April 11, 2000

- Tested 40kbit and 1Mbit assembled storage elements
- Added large stroke actuator to cantilever design for next generation operation
- Scaled stage design to accommodate 100x storage by burying the actuator beneath the data platform and shielding the cantilevers from resonant tuning

Milestones for the Future Work:

- Fabricate and test 100Mbit prototype using new stage concept and row-column addressing of cantilever arrays
- Integrate massively parallel cantilever array using appropriate partitioning of integrated and discrete electronics
- Perform system reliability studies for long-term tip-surface interactions

- Develop read-write mechanism using magnetic force microscopy and quantized magnetic dots
- Scale the storage system to densities competitive with existing memory technology and provide interface circuitry necessary for common bus interfaces

1. Introduction

This project is part of an ongoing effort at Kionix to provide a two-chip data storage device composed entirely of MEMS actuators. We have spent the majority of the past six months studying the operation of two prototype data storage elements, operating up to four cantilevers in parallel. The total capacity of the elements has increased from 40kbits to 1Mbit by increasing the total number of cantilevers to 44 and reducing the smallest bit size to 250nm.

From feedback obtained during the operation of the storage elements we have developed the next generation 100Mbit system design. Improvements in this iteration include increasing the stroke range of the cantilever using a low frequency actuator, reconfiguring the stage to improve areal efficiency and shielding, and changing the assembly arrangement to ensure hermiticity and ease die singulation.

This final report is a summary of developments during the three years of the contractual effort. We include details on the components and system assembly, as well as system results. Finally, new system designs and a roadmap for the future work is included.

2. Silicon MEMS Fabrication Processes

A significant invention of the three years of the project was to develop a flexible silicon MEMS fabrication technique for fabricating both the cantilever arrays and the two-dimensional (2D) stages. In collaboration with Cornell University, we have developed a beam isolation process that enables two fundamental advancements in silicon MEMS fabrication: multiple contacts for a single released structure (necessary for decoupled stage x and y motion), and the reduction of parasitic capacitance (improving the signal to noise ratio for capacitive measurements and reducing actuator power consumption). Both the cantilever arrays and the stage are fabricated using variations of this technique.

Beam-level isolation is the electrical isolation of individual silicon beam segments from each other or from the substrate silicon. In silicon beam processing based on previous techniques, electrical isolation is normally achieved by coating the structures with metal and using that metal layer for conduction. Multiple paths on a single released structure can be achieved by

coarse patterning of the metal. We have chosen not to use this technique for several reasons. First, the patterning step must be done over an extremely non-planar topology, and is not easily scaled with increasing structure depth. Second, the patterning must often be accomplished on released structures with post-release wet chemistries. This often results in dramatic yield loss.

Therefore, we have chosen to employ the beam-level isolation technique that uses oxide isolation segments incorporated within the beams for electrical isolation at the silicon. Electrical connections are made with a planar metal layer, which contacts the silicon beams to form conduction paths. A schematic of the process we have implemented and tested is shown in Figure 1. First, a trench is etched and filled, later to become the oxide segment within the beam. Second, metal is deposited and patterned to form contacts directly to the silicon. Finally, normal micromechanical processing is resumed to pattern, etch, and release the structure.

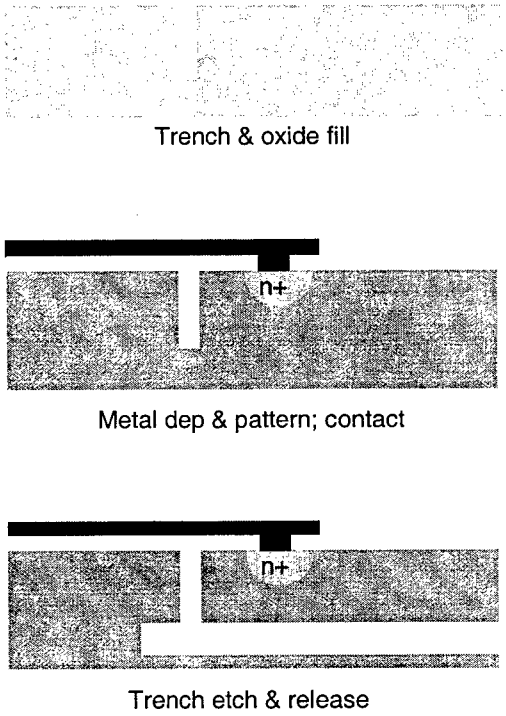

Figure 1. Process schematic for beam-level isolation.

From a fabrication standpoint, the process is mostly self-aligned, since the metal can be aligned to the beams during the structure patterning level. More importantly, the process is planar because all patterning steps occur on a flat topography. One disadvantage is that silicon becomes the primary conductor,

and so the impedance across the device is increased slightly. However, for capacitive devices an important side benefit of the oxide segment is that the parasitic capacitance is reduced to the cross section of a single beam. The predominant process difficulties are ensuring that the trench is filled uniformly, the metal is continuous across the oxide segments, and that no silicon filaments or paths remain to degrade the level of isolation achieved.

It is important to quantify the fabrication processes in experimental measurements of the isolation impedance. We accomplished this task using test structures which were probed using a semiconductor parameter analyzer. One of the test structures is shown in Figure 2, which has conduction from aluminum to silicon beams and back to aluminum. This conduction path is isolated from a second set of ground lines in the silicon, set orthogonal to the first path. A plot of the impedance of the interconnect and the isolation between the two current paths is shown in Figure 3. In this test configuration we obtain in excess of 1 gigaohm of isolation, while maintaining ohmic conduction through the contacts and the silicon beams. The exact magnitude of the leakage current is limited only by the resolution of the parameter analyzer.

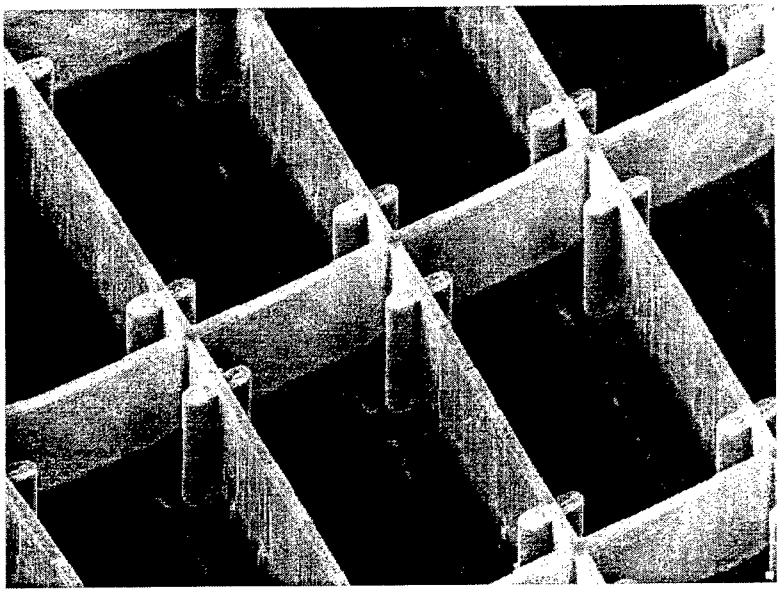

Figure 2. Quantitative test structure for beam-level isolation. Note that the interconnects begin on the aluminum, contact to the silicon beams, and return back to the aluminum to provide isolation from the orthogonal ground lines.

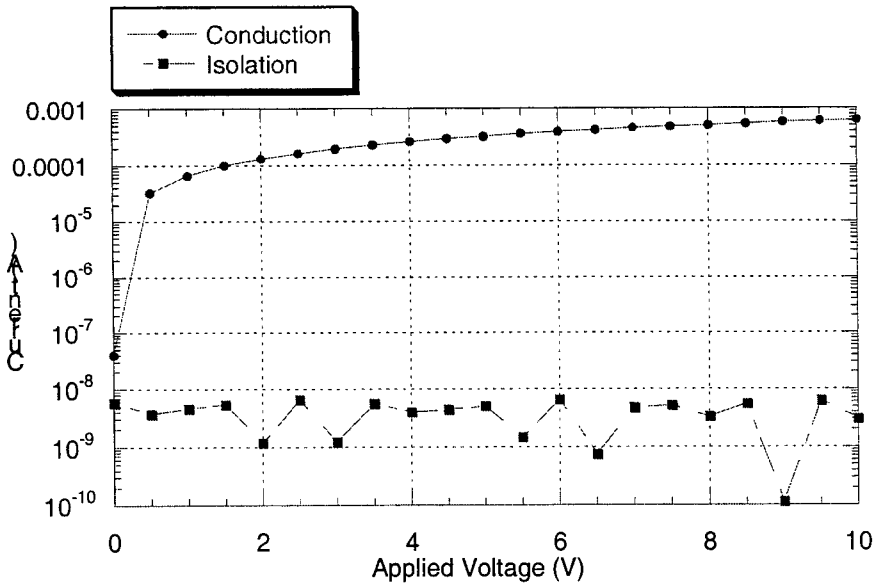

Figure 3. Plot of conduction and isolation impedance for the test structure. Note the measurement resolution is limited by the noise in the parameter analyzer.

As shown in Figure 4, one initial difficulty with the fabrication process was continuity of the metal across the isolation segment. This continuity is related to the void formed during oxide trench fill and etch-back. Initially, many of the conduction paths were broken by this void. However, we eliminated this problem through planarization of the surface using photoresist. The other difficulty encountered during fabrication was the presence of silicon filaments bridging the oxide gap and degrading the isolation. By adjusting the profile of the isolation trench and structure etch, we have completely eliminated filaments leading to vastly improved isolation characteristics.

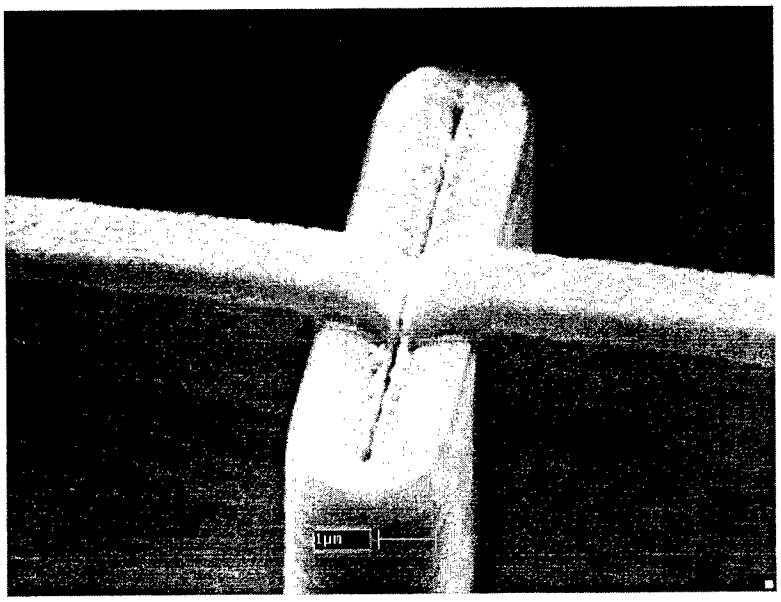

Figure 4. Metal continuity failure across the oxide isolation segment.

In order to provide the large area platform for data encoding, we combined the beam level actuator process with a backside deep RIE step to release a large area platform. The outline for the stage process is shown in Figure 5. By performing beam-level isolation on the frontside and deep RIE from the backside, we are able to release the actuators and the platforms and provide the necessary stage functionality.

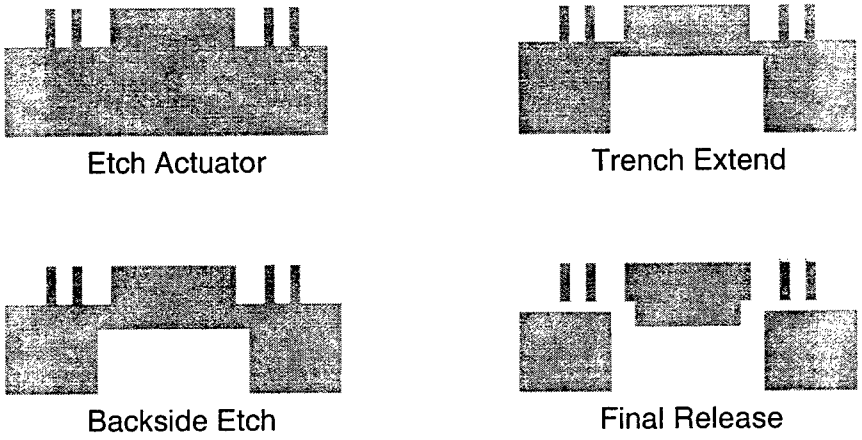

Figure 5. Backside RIE process for releasing large area data platform.

3. 2D Stage Development

Using the backside RIE process enabled us to build functional, decoupled actuators integrated with data platforms. The most difficult aspect of the stage

design then became ensuring a substantial deflection. The target values for deflection were 30-50μm of travel backward and forward in both x and y directions. This amount of deflection enables several percent of the complete device area to be used for storage given the fill factor of the cantilevers.

We began our stage development by testing the limits of conventional folded spring designs. A linear spring constant of 0.25N/m was obtained for a beam width of 1μm and a depth of approximately 20μm using the stage geometry detailed in Figure 6. The springs in this design performed better than anticipated, deflecting approximately 20μm with about 25 actuating volts. The point of instability for the springs, or the maximum obtainable displacement, was not reached due to the presence of beam stops.

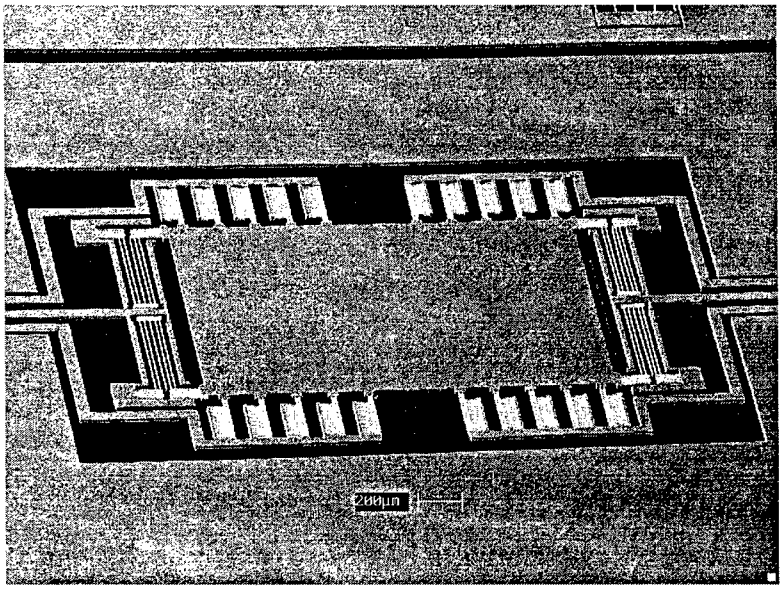

Figure 6. Large deflection data substrate design with folded springs and distributed actuators.

We added a data coding process to this stage design in order to provide storage compatible substrates. Throughout the contract this encoding process consisted of lithography and etch of data features (lines or dots). An example of the coding process is shown in Figure 7, where faint lines are visible in the upper left of the SEM micrograph. This coding process requires only one additional mask to the beam isolation and platform release process.

These initial stages were capable of one-dimensional motion. Besides scaling the structure to two dimensions, the predominant difficulty with the first designs was the vibration susceptibility of the large mass inherent in the data

platform. Many die were lost during back-end dicing and packaging. Consequently, the off-axis stiffness of the springs was insufficient to preclude transverse motion and limit out-of-plane deformations.

The design efforts for 2D stages were focused on providing a robust stage that would be insensitive to vibration and resistant to electrostatic instability. In order to achieve these gains in performance, we used extensive finite element modeling from the ANSYS code, and attempted to meet a 100g vibration specification typical of a hard disk drive.

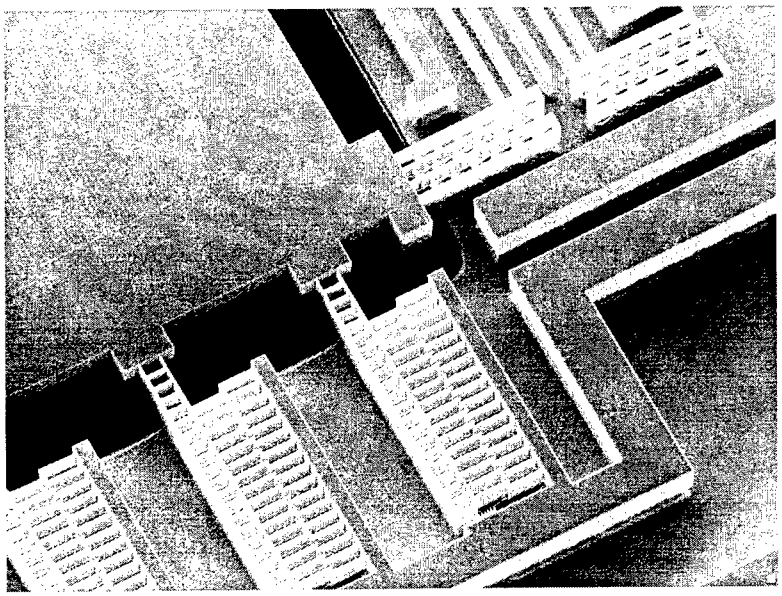

Figure 7. Data patterning on the large deflection stage surface. The 1μm data lines appear in the upper left corner of the micrograph.

In addition to the complete system analysis, the goal of the design study was to provide a full scale deflection of +/-25 microns without electrostatic comb-drive instability. At large deflections the spring designs tend to lose their off-axis stiffness, and become open to catastrophic transverse electrostatic instability. Typical folded spring designs were insufficient to meet the needs of the data stage, and hence distributed springs were designed into the stage. A schematic of a distributed spring design is shown in Figure 8.

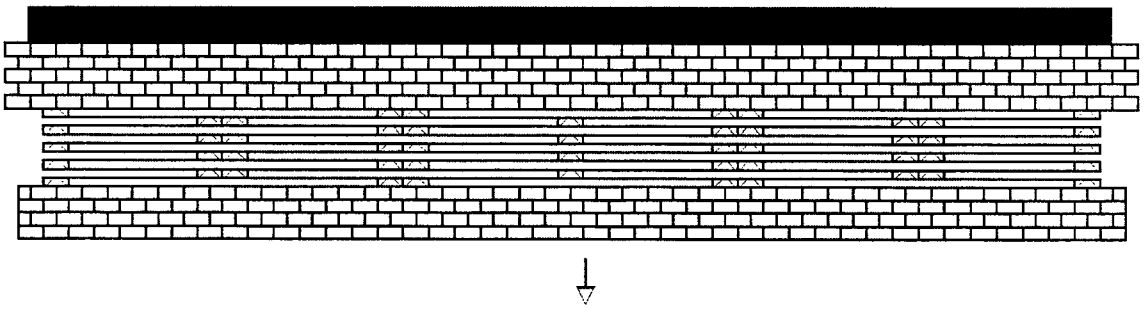

Figure 8. Schematic of a distributed spring for large deflection with high resistance to instability

The predominant figure of merit for all spring designs is the ratio of the transverse axis stiffness to the deflection axis stiffness, or k_y to k_x. A large ratio is better, i.e. the spring will resist off-axis instability longer. Although we could achieve high stiffness ratios for the folded spring designs, the ratio dropped significantly for large deflections. Distributed springs were much more stable over the entire deflection range. The relationship of the stiffness ratio versus deflection is plotted in Figure 9 for both the folded and distributed spring designs. The curves are obtained using deflection analysis from ANSYS.

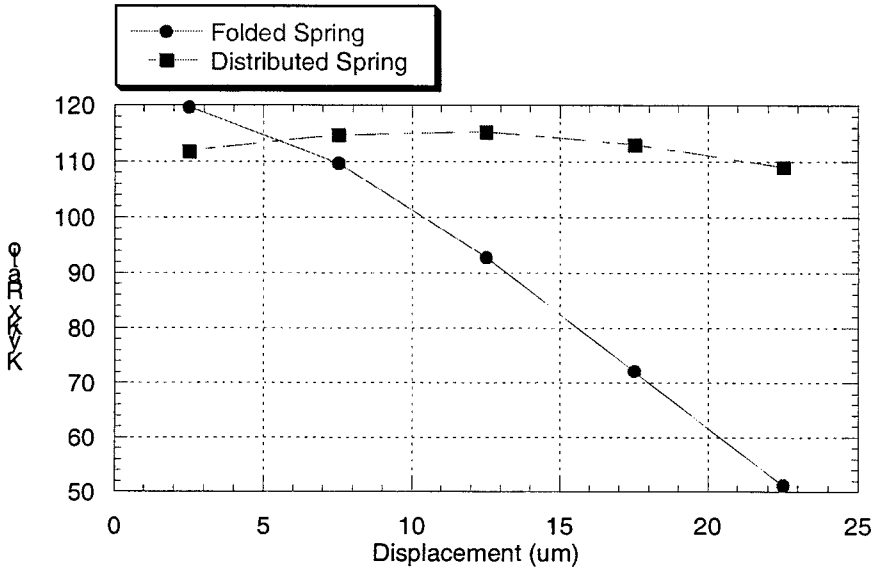

Figure 9. Stiffness ratio plot for distributed spring versus a normal folded spring. Note the stability for the distributed spring design even over large deflections.

The other structural change resulting from the design study was a more conservative approach to the size of the data area. The previous through-wafer devices attempted to maximize the size of the data area, sensible because

efficient use of the die requires a small actuator to data substrate area ratio. However, this high storage area mass directly resulted in poor vibration sensitivity. Therefore, we substantially reduced the effective data area. An example of a completed 2D stage is shown in Figure 10.

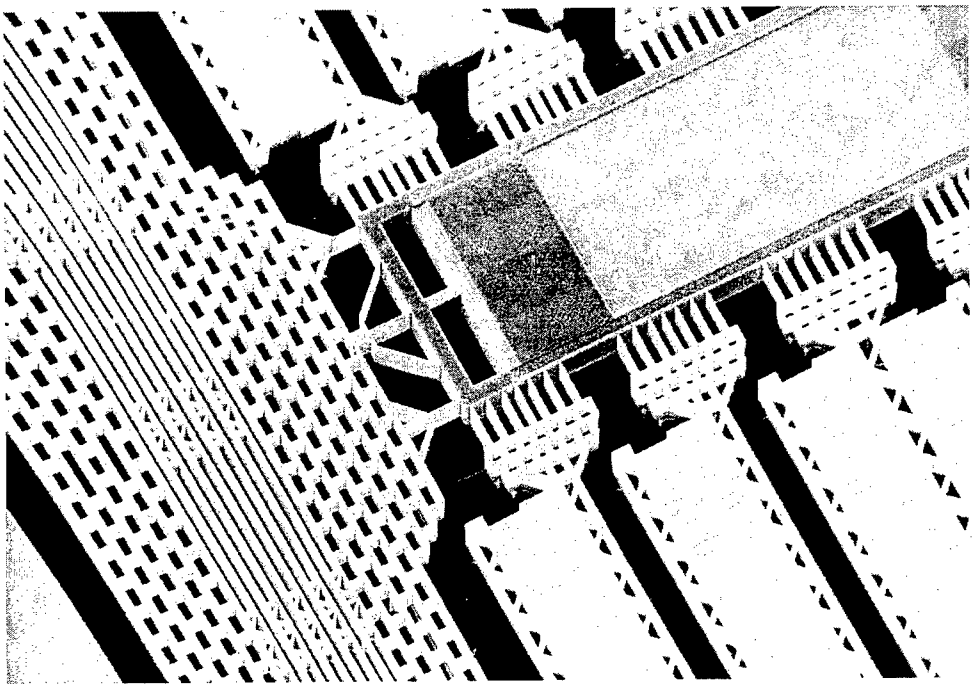

Figure 10. Completed 2D stage showing distributed springs and coded data area.

Three iterations of 2D stages were fabricated during the course of the project. The devices ranged from 200um platform area, accommodating two to six discrete cantilevers, to a stage capable of accepting 44 cantilevers. Characterization of each of the data stages was performed using an atomic force microscope (AFM) to record the data features on the stages during operation.

Driving stages in back and forth in two orthogonal directions requires the use of four separate programmable sources, each with the capability to deliver in excess of approximately 30-50 volts to the capacitive load presented by the electrostatic actuators. We have matched this capability through the use of buffer amplifiers connected to a National Instruments digital-to-analog board. The board has six independent analog outputs and 12 bit resolution. The card was configured to deliver a maximum output level of ten volts. Four analog channels of the D/A board were thus connected to separate 7x voltage buffers, the electrical schematic of which is shown in Figure 11. The circuit is set for an

overall gain of seven, but since the op amp must be kept below saturation, the transistors Q1 and Q2 are required for high voltage amplification. The output resistor is included for protection against accidental shorts in the actuators; since the load is capacitive only, the high output resistance is not an issue. With the exception of an inhibiting circuit on the front end, the rest of the components are for frequency compensation to prevent loop instabilities.

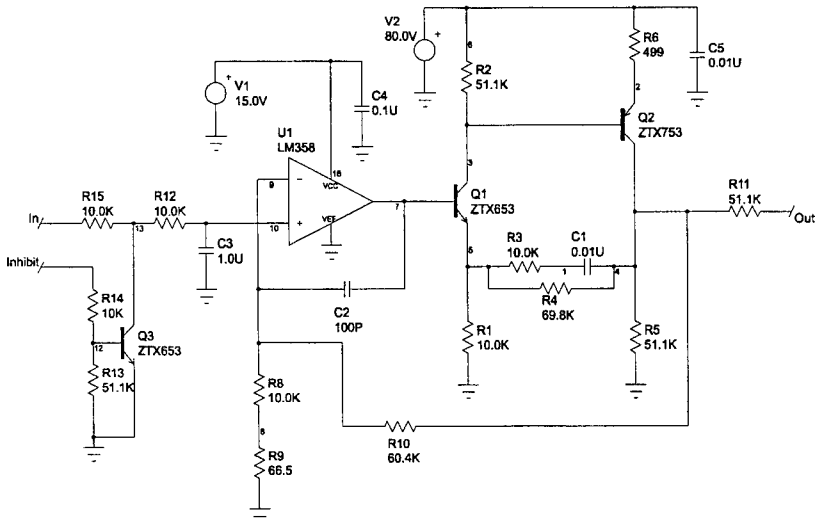

Figure 11. Electrical schematic of the buffer amplifiers, used in conjunction with a D/A board as stage drivers.

Using the software interface provided by the LabVIEW environment, we have been able to drive the stage in arbitrary scanning profiles using the D/A card and buffer amps. The AFM could record the motion by measuring to extreme accuracy the deflection of the stylus. The accuracy of this technique was typically 25nm. A characteristic graph of displacement, this example a large displacement design, is shown in Figure 12. Note that these stages encompass a displacement range of approximately 50μm.

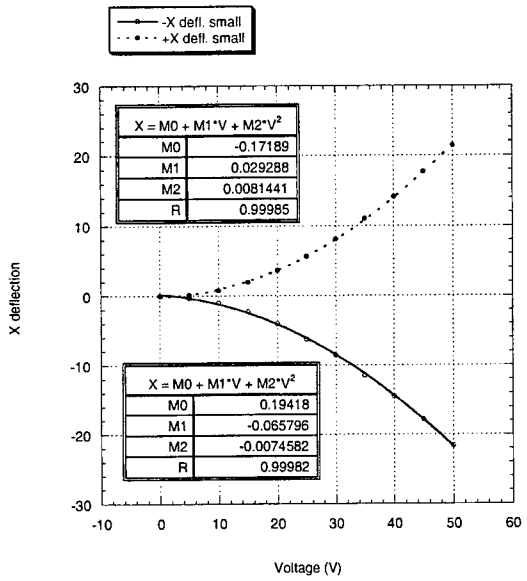

Figure 12. Deflection results of the x-actuators for large displacement stages.

Several peculiarities were found during testing of the data stages. Consistently, the data platforms deflected in the vertical direction (in addition to the preferred lateral directions) when voltage is applied to the drives. This out-of-plane motion is exacerbated at higher stage displacements and is directed down towards the substrate. This motion was confirmed with both AFM and SEM analysis. A quantitative plot of the z-displacement is shown in Figure 13. The motion may be due to the fact that there is some initial bowing of the stage due to its relatively large span. This bowing results in a net levitation (or z) force by the comb actuators during drive.

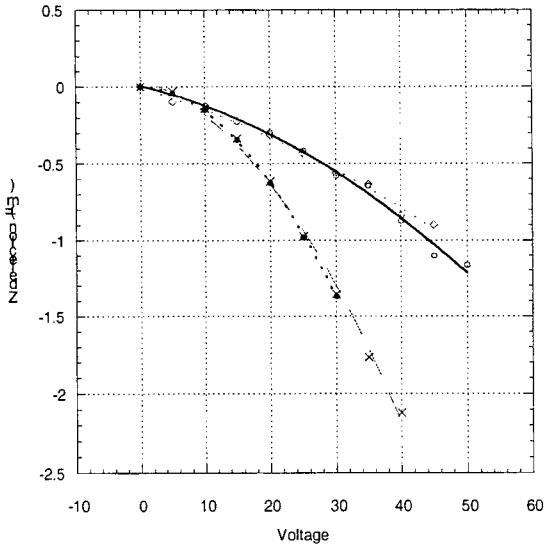

Figure 13. Out-of-plane deflection of stage versus actuation voltage.

Sweeping the stage using the buffer amps and recording data using an AFM gave us clear images of the data patterns on the platform. When the MEMS stage is scanned, a hysteresis effect is present between the forward and reverse scan directions. Figure 14 shows data acquired while the voltage on the stage actuator was ramped up (forward) and down (reverse). In a perfect system, the images would be identical. However, we observe a shift of approximately 1μm in the images, with some streaking occurring at the changes in direction. We believe this hysteresis effect is due to nonlinearity in the flexures caused by the sidewall oxide passivation films.

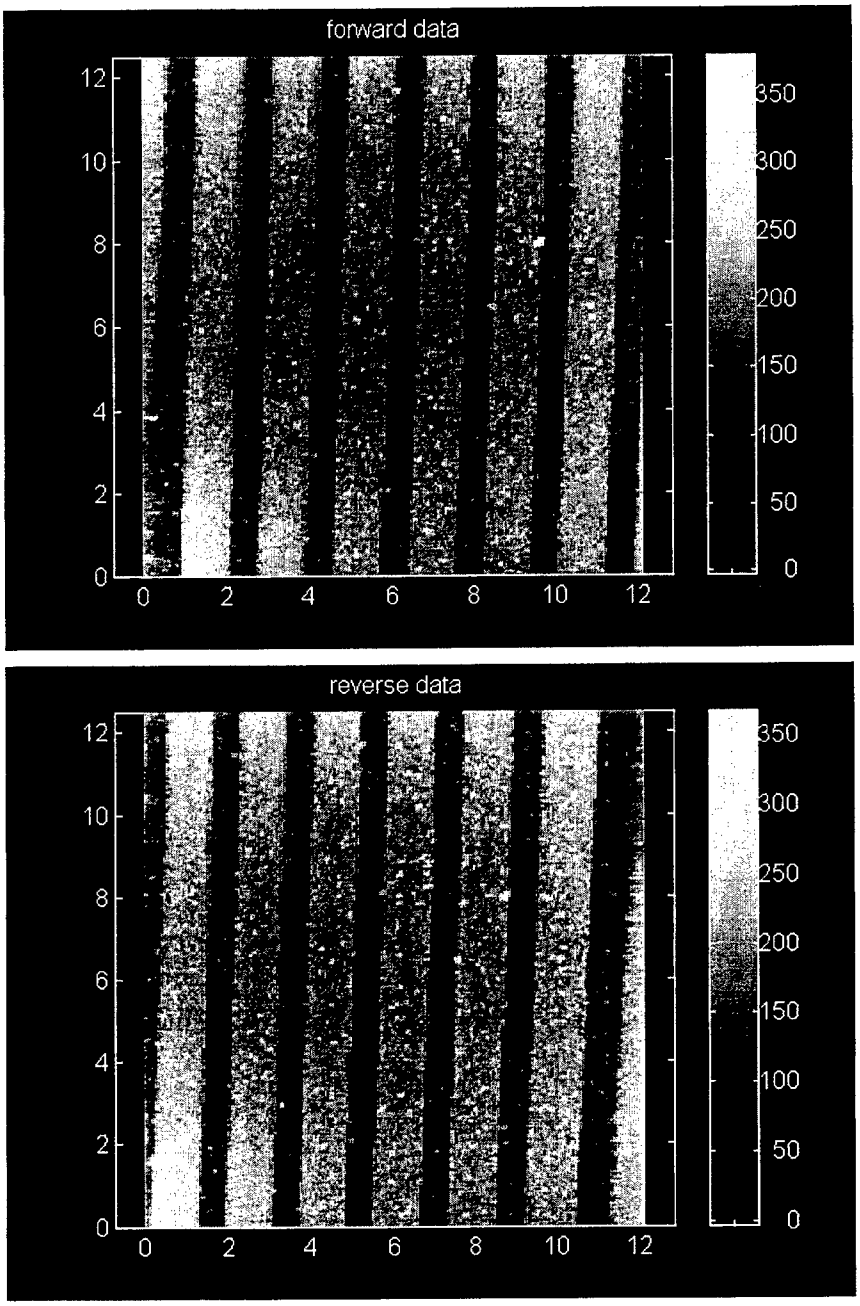

Figure 14. Comparison of forward and reverse scans for the stage. Note the shift in images because of hysteresis. Some streaking is also present at the extents of the scan.

Generally, the stages functioned as designed. Some higher order flexing of the frame generally led to asymmetry of the x and y mechanical stiffnesses, and reduced the onset voltage for electrostatic instability. Performance of the stages in the overall storage system is reviewed in section 5.

4. Cantilever Arrays

Force microscopy is the most flexible method of achieving tip-based data storage. In an AFM, the microscope detects the absolute position of the cantilever on which the tip is mounted or the resonance shifts resulting from dithering of the cantilever. To design a MEMS capacitive cantilever, we carefully analyzed the torque and the resulting capacitance changes generated from two cantilever electrode configurations that could be made with the silicon MEMS process; one with the capacitors composed of the sides of the cantilever beams (sidewall electrode configuration) and the other with the capacitors formed from the metal on the top surface of the beams (interconnect electrode configuration). In both configurations, the cantilever is driven using electric field asymmetries out of the plane of the wafer (levitation actuator).

The total capacitance of the interconnect configuration is less than the sidewall configuration because the overlap area is reduced. The resulting torque generated by this configuration is about one-third that of the normal sidewall case. However, in terms of capacitance changes available for deflection sensing, the two configurations are very similar. Plotted in Figure 15 is a comparison of the changes for both as a function of deflection angle. Since capacitance change is the ultimate figure of merit for the resolution of the sensing circuit, little is lost in the interconnect configuration.

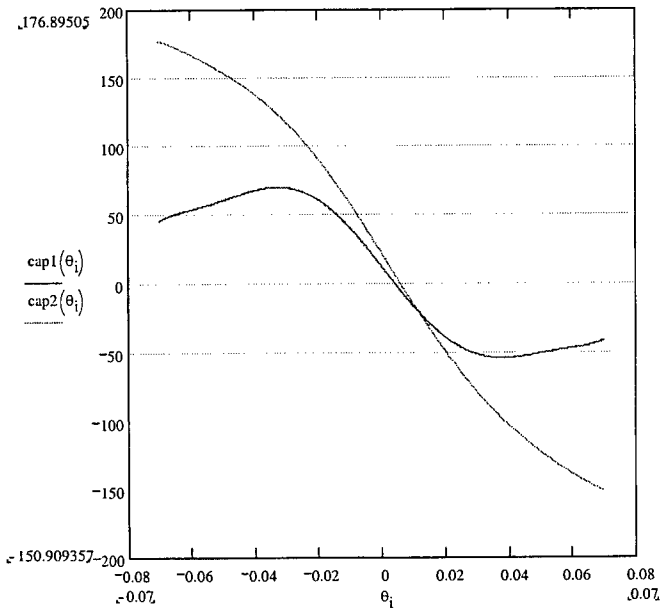

Figure 15. Comparison of the capacitance change for sidewall and interconnect electrode configurations as a function of deflection angle. Both have similar linear regimes.

What is gained, however, is an extraordinary decrease in the complexity of processing. By using the interconnect approach, we can easily fabricate separate drive and sense terminals on the cantilever with a planar metal process rather than with either a patterned, sputtered metal process or the complete beam-level contact sequence. Parasitic reduction is obtained without effort because of a vast reduction in metal coverage area. Additionally, fabrication processes for the tip are more easily integrated with the cantilever process.

Capacitive sensing and transduction of the deflection of the cantilevers is needed to operate in atomic force mode. We developed several variations of non-contact mode AFM for the cantilevers. In each case, the cantilevers are oscillated at its resonant frequency and modulations in amplitude, frequency, or phase are detected to sense presence or lack of a surface feature. Additional requirements for the circuit are that it can be implemented within a silicon integrated circuit, must be reproducible for parallel operation of tips, and must be simple enough to occupy a small chip area. We have spent a significant portion of the project developing discrete and integrated circuit forms of the cantilever circuitry.

At the schematic level, three critical functions are required from the transducing circuit. It must be capable of positioning the tip and cantilever within the optimal tip-surface interaction distance, must regulate the oscillation of the cantilever, and must detect shifts in resonance due to the presence of a data bit. The circuit most commonly used during the project is shown in block form in Figure 16. The cantilever is separated into drive and sense electrodes. A high frequency carrier circuit was used for the sense function, and combined with a low distortion drive signal set to half the resonant frequency. The voltage-squared dependence of the actuator force ensures that the cantilever is excited as desired. By using a low distortion drive signal one avoids interaction between high harmonics and the carrier frequency, which are undesirable. In order to further increase the signal to noise ratio, we chose to operate in tapping mode for the cantilever, relying on high amplitude ac excitation rather than a small amplitude oscillation imposed on a dc offset.

Following the differential amplifier is filtering and a synchronous demodulator to deconvolve the sense capacitance. The results are compared to the drive signal with a phase detector to measure phase shifts. Feedback was not commonly used during the system experiments; often the cantilevers were oscillated with an external source controlled by a LabView interface, thus allowing automated control and imaging of the data bits.

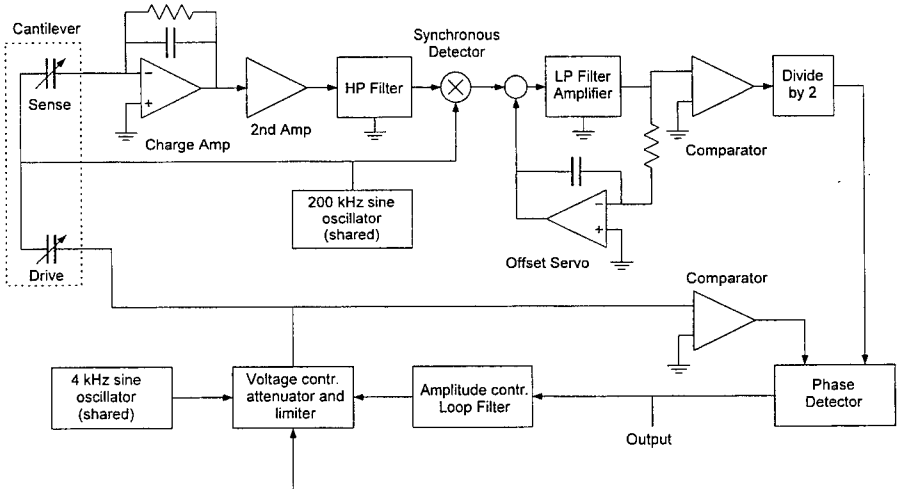

Figure 16. Block diagram for the cantilever frequency detection circuit.

We chose to start with low cantilever resonant frequencies (6-8kHz) and increase the cantilever frequency to 30kHz as we developed the transduction techniques. The lower frequency cantilevers yielded more detection capacitance and greater stroke range and were easier to operate within a system. An SEM

micrograph of one of the fabricated cantilevers is shown in Figure 17. Note that several banks of capacitive electrodes were used to aid in driving and sensing the cantilever motion.

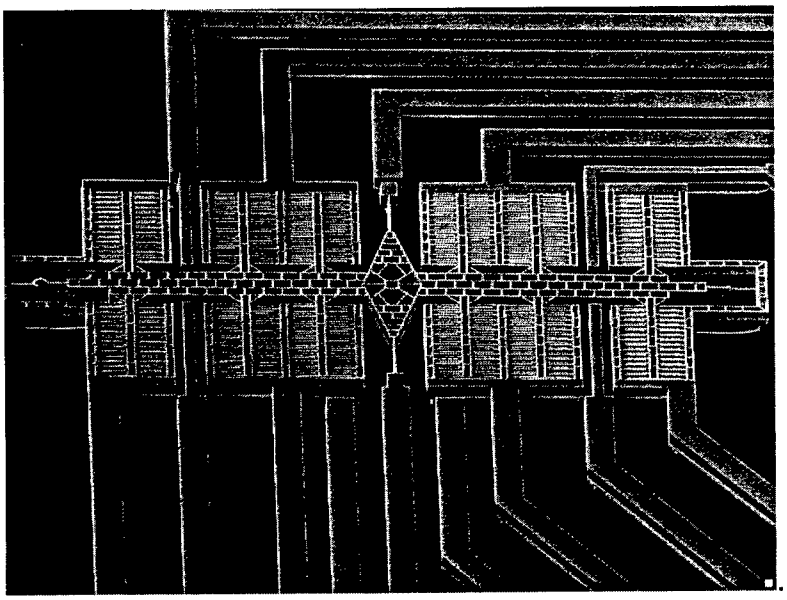

Figure 17. Low frequency cantilever with multiple electrodes for drive and sense.

We first used the cantilever designs in tapping experiments with unpatterned chips. When the cantilever tip impacts a surface, an additional force is imparted to the cantilever. The resulting shift in resonance is usually detected by monitoring changes in phase response. We tested the tapping response two ways. The first was to excite the cantilever in vacuum (2.5 Torr) and to high amplitude until the cantilever oscillations were limited by the substrate floor. The results of this experiment are shown in Figure 18. As soon as a large enough amplitude is achieved, the cantilever clearly hits the substrate floor.

True tapping mode tests were then performed at atmosphere using a commercial AFM. A standard AFM cantilever was used to provide an accurate displacement reference. Piezos were used to approach the AFM cantilever to the MEMS cantilever, which was excited at a constant drive oscillation. The response of the detection circuit is shown in Figure 19. Note that the response is distorted under the presence of tapping, and at any given excitation frequency a phase shift occurs with the onset of tapping. We have detected phase shifts of approximately 15° per each 100nm deviation of the surface at constant excitation. There is some hysteresis present in the phase shifts; after cycling the position of the surface the phase shift may not be identical.

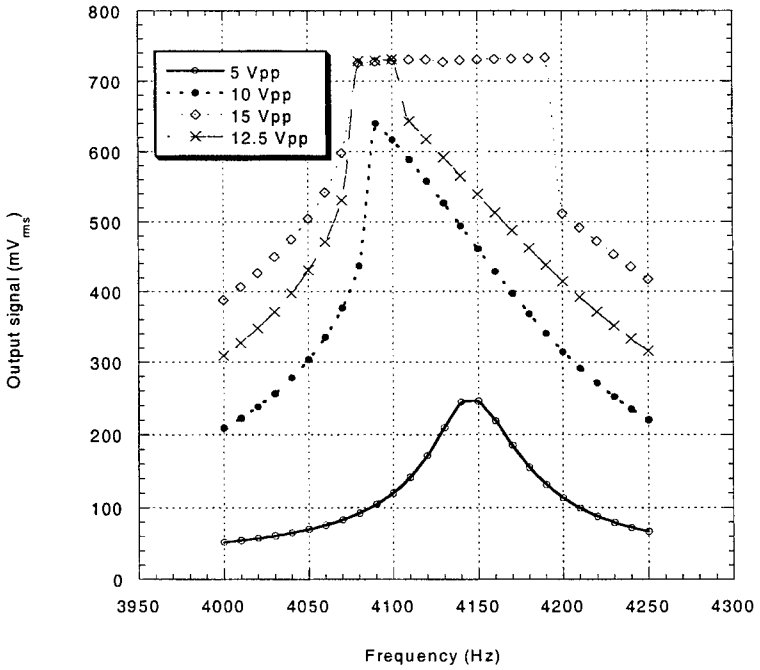

Figure 18. Cantilever response under vacuum as a function of drive voltage.

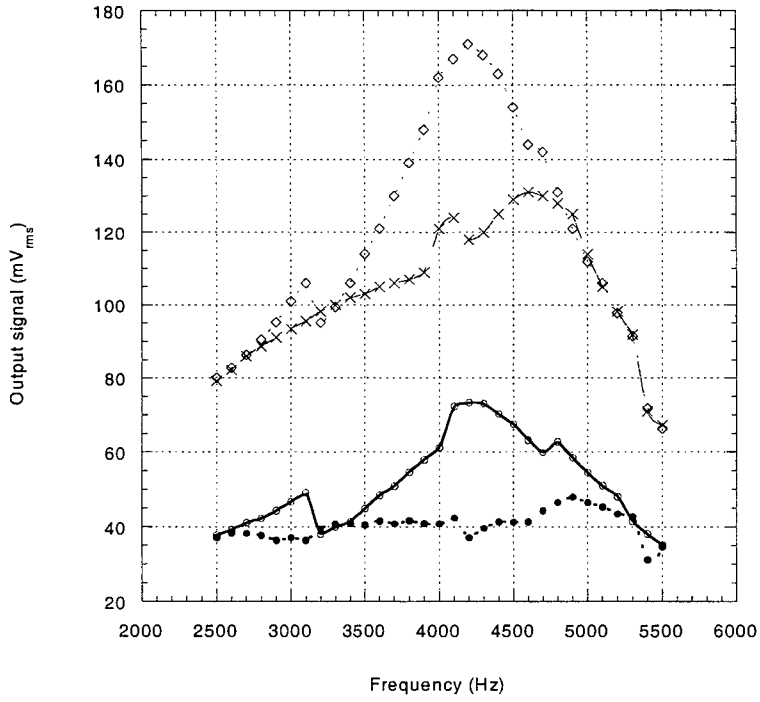

Figure 19. Atmospheric response of cantilever for 20 and 30 volts excitation. Distorted waveforms are a result of tapping.

Given the amplitude and phase response in these simple experiments, we set out to demonstrate the capability of the cantilever during scanning. We performed these experiments in two regimes, constant phase and constant amplitude. First, using external piezos, we scanned a chip with 5μm data line features over the cantilever and recorded the drive amplitude at which abrupt phase change was detected. The results of this experiment are shown in Figure 20. The sample was prepared by etching 5μm lines and spaces into 500nm of silicon dioxide. Note that the lines and spaces are clearly visible in addition to the level shift occurring as a result of sample tilt. The presence of tilt in the sample is not surprising given the separate mounting systems for the two chips.

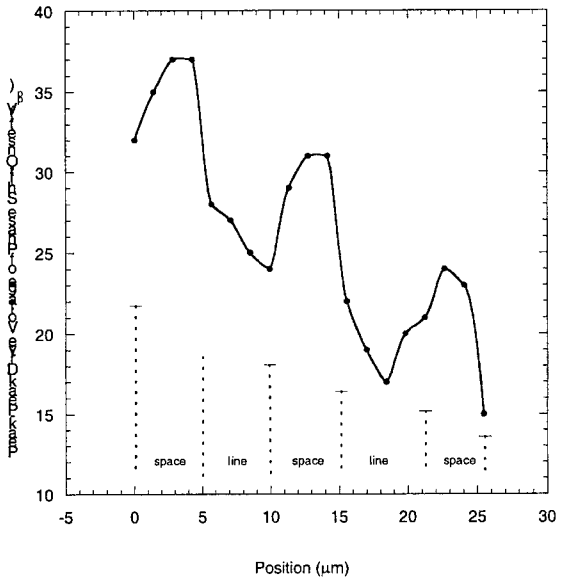

Figure 20. Line scan obtained by varying cantilever amplitude until phase change is recorded.

Using this basic scanning technique, but operating in constant frequency, constant drive amplitude allowed us to perform a 2D scan of the same sample. The output of the circuit, or phase response, was recorded automatically and plotted to provide a full data image. The image results are presented in Figure 21. Again, the lines and spaces are clearly visible, although there is a degree of noise present in the scan. This is again due to tilt of the sample relative to the cantilever.

Occasionally during this scan the substrate would fall out of range of the cantilever motion, and the sample to cantilever spacing would be manually modified to yield output. The regions where the adjustments were necessary are apparent in the horizontal bands of the scan. Although the scan was performed

in the somewhat piecemeal fashion, it proved the viability of the phase measurement.

An important issue raised, however, is the relative positioning of the scanned substrate. In both the line scan and the phase scan, tilt of the sample necessitated amplitude adjustment of the cantilever or positional adjustment of the sample. Some of this lack of planarity was obviously due to the test setup, and the differences in mounting of two distinct samples. Related issues arising in bonding of the system chips are optimum tuning of the separation between the data platform and the cantilever, and providing planarity between the stage and the cantilever over the entire scan range.

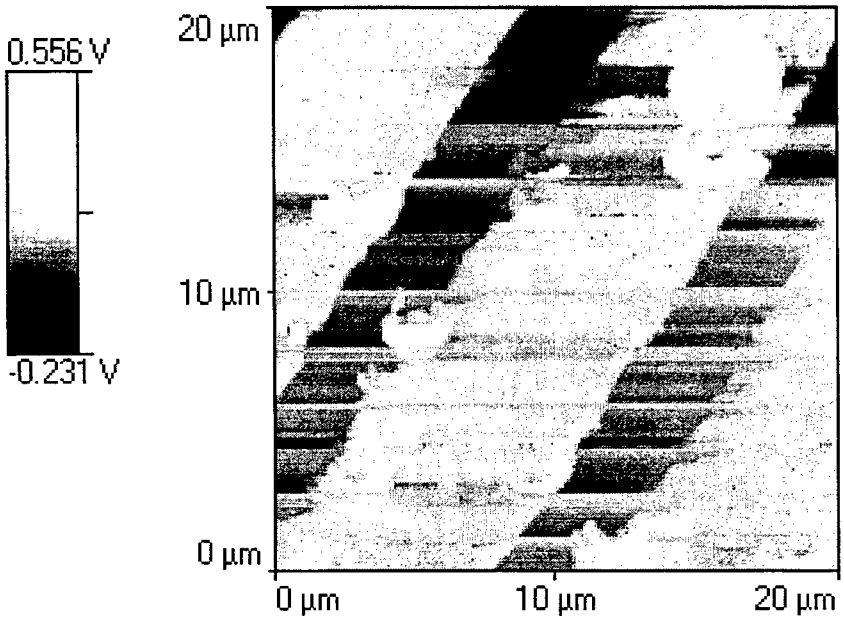

Figure 21. 2D phase scan using constant amplitude excitation.

Over the project, we worked to integrate elements of the cantilever circuit into integrated form, where we could take advantage of the parallelism provided by integrated circuit fabrication. We chose to develop switched capacitor circuitry in a standard 0.5um CMOS process. After three chip iterations, we have developed a complete capacitance detection circuit including front-end charge amplifiers, voltage-controlled oscillator, demodulator, and filtering.

The requirement for full-scale integration of the cantilever circuitry comes from the requirement for parallel operation of many cantilevers to increase the data transfer rate. Also, if each cantilever is addressed separately, an enormous amount of input/output terminals are required for the array. Therefore, several

row-column architectures were investigated as a means to address large numbers of cantilevers. A minimal amount of addressing circuitry, a regime we call small-scale integration, requires that most of the array inputs be tied together for commonality. For example, the supply voltage and ground, carrier, and drive oscillation would be identical for all cantilevers. The output from each cantilever would require a separate output pin for each cantilever. Most of the multiplexing would then be performed off-chip. Increasing the scale of the integration, a sort of medium-scale integration, would allow a row of cantilevers to be operated at the same time. Large-scale integration would require full implementation of circuitry for each cantilever element, probably a requirement for a commercial data storage device.

Each increasing level of addressing requires an increasing level of integration of the cantilever electronics. During the project, we developed an entire capacitance detection interface circuit using the CMOS process line available through the MOSIS foundry service. The capacitance resolution we achieved using switched capacitance architecture was $1aF/Hz^{1/2}$, well within the requirements of cantilever detection. However, we have not to date implemented the high voltage drivers required for cantilever drive, since such an implementation will require a high voltage capability in the fabrication process. Integration of the capacitance detection circuits with the actual cantilevers was also not attempted during the course of the work.

For the final iteration of the ROM, we performed a redesign of the cantilevers to achieve a resonant frequency of about 30kHz. This increase in resonance was accomplished by both reduction in mass and increase in torsional stiffness of the device. The new cantilever frequency allowed us to halve the width of the cantilevers to 150μm, as shown in Figure 22. The control circuitry was modified to accommodate the higher resonant frequency device, and also add a separate transformer circuit to provide higher drive voltages.

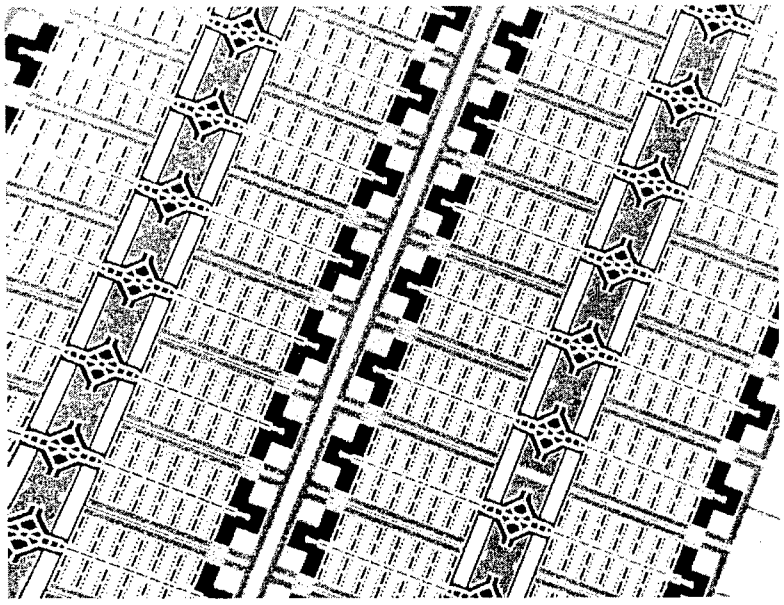

Figure 22. Fabricated 30kHz cantilever array.

The new cantilevers also included improvements in tip processing necessary to achieve a reduction in feature resolution to 250nm. A resist erosion process was used to reduce the lithography pattern for the bits to less than the originally patterned 1μm circle. By isotropic etching of the resist before pattern transfer, we were able to achieve a bit size of less than 200nm. Likewise, it was necessary to improve the fabrication of the probe tip. Previously, sidewall spacers had limited our achievable tip size to about 1μm. In order to surpass this limit, we modified our tip fabrication sequence to fabricate a quarter micron silicon filament encased in oxide to protect the tip during subsequent cantilever definition. The silicon filament is then exposed after release etching by plasma etchback of the oxide. SEM micrographs of the encased silicon probe and the resulting optimal tip shape is shown in Figure 23.

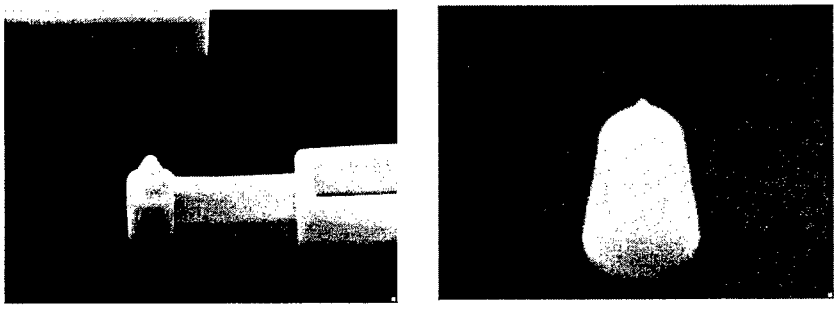

Figure 23. Tip processing for quarter micron probes, including encasing the probe (left) and etchback of oxide protection (right).

5. System Assembly & Operation

The goal of the assembly efforts was to provide a first complete system demonstration, not to optimize the level of storage or emphasize the complete system architecture. The fabricated systems included a version with 24 cantilevers and a version with 44 cantilevers, which address their own sectors of data on the stage. Each of the sensing lines for the cantilevers is pinned out separately, although the drive voltage is shared for each of four sets of six cantilevers. We thus apply the same drive voltage to a line of cantilevers in order to test the uniformity of the cantilever array and the effects of system planarity. The cantilever designs have remained at low frequency (8-30kHz), in order to maximize the stroke distance of the cantilever and allow high signal to noise for topography detection.

Examples from the system fabrication are shown in Figures 24 and 25. Note that the cantilever array is constructed to mount directly to the stage, and the bonding pads match on the two devices. The array of cantilevers rides over the data platforms when bonded. The bonding areas consist of the rectangular regions surrounding the cantilever array and the large trapezoidal areas on either side of the array. The four pads for the stage connect to pad areas on the tip die, and are the portion of the bonding providing a chip to chip conductive interconnect. As mentioned, the cantilevers are split into four groups of six. Each group shares a common ground and drive signal line, meaning each cantilever in a particular group is driven in tandem with five others. The remaining twenty-four pads are the separate sense signals from each individual cantilever. Most importantly, all of the input/output bonding pads are pinned out on the cantilever die for wire bond access.

The stage design was optimized to the system performance. The same actuator design was used to incorporate either 24 or 44 platforms for different cantilever arrays. The large extent of the stage led to several microns of induced bow, and hence z-deflection, across the array which complicated the measurements.

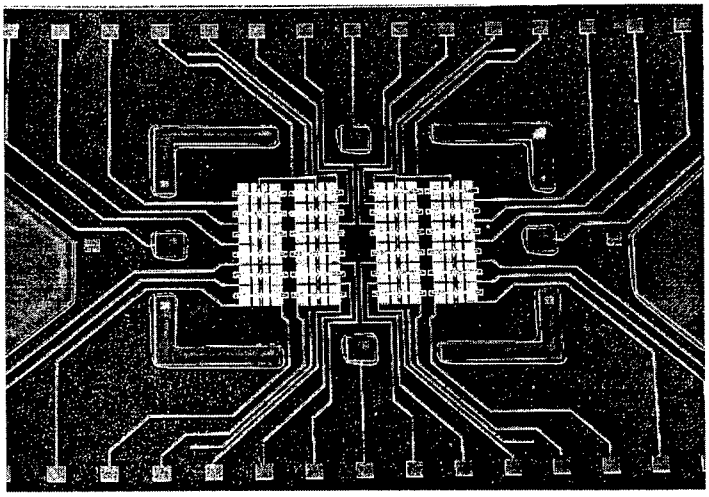

Figure 24. Cantilever array (24 elements) fabricated for the integrated device.

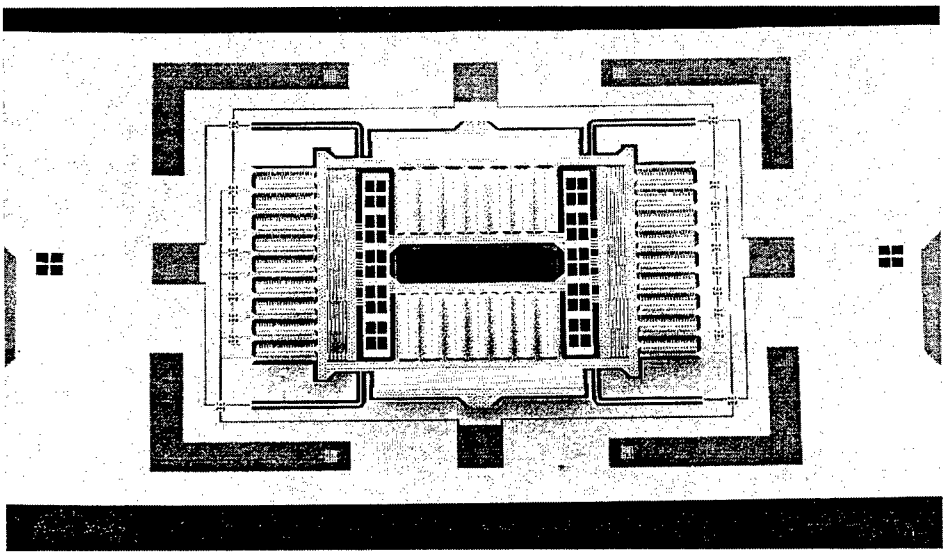

Figure 25. Released stage for the integrated device.

System assembly has proven to be one of the more difficult aspects of the project. Bonding between cantilever chips and stage chips was accomplished with a variety of means. The normal constraint of any bonding process is hermiticity. However, bonding for the storage system also requires a chip-to-chip interconnection and appropriate separation between the cantilevers and stage surface. These interconnects constrain the bonding process to metal solder or eutectics. Wafer level bonding was chosen because of the ability to bond multiple die at tight alignment tolerances, thus controlling the alignment of the cantilevers to micron tolerances.

We originally performed a variety of experiments in order to test eutectic aluminum-silicon, gold-silicon, and aluminum-oxide wafer level bonds. However, none of these eutectic systems provided an acceptably high yield of interconnects, and their wafer bonding capability was limited as well. Because of the importance of the cantilever-stage separation distance in the overall system, we could not implement additive bonding processes (glass frit, adhesive, solder bump) because they provide an unacceptably large separation between functioning chips.

After attempting many aluminum-aluminum bonds, we finally obtained success in our bonding efforts using gold thermocompression bonding. Our bonding parameters for this system are 400°C and 7kN for a 150mm wafer. Careful preparation of the gold surface was found to lead to greater bond strength and better interconnect yields. The gold bonds have survived wafer sawing and separation, indicating that the bond is acceptably strong for the final device.

In order for the gold to be useful as the chip interconnect material, it had to be combined with the aluminum metalization used in the tip and stage processes. Our original attempts at merging the two materials provided low contact yields due to the typical gold-aluminum "purple plague" interaction. However, we relied on previous published work to implement a diffusion barrier system composed of titanium and platinum to form the bonding stack. A schematic of the bonding process is shown in Figure 26. The integrated stage and cantilever device has separate regions for contacts (approximately 250μm) and general bonding areas (much larger in expanse). The titanium and platinum thickness must be carefully tuned to ensure separation of the gold and aluminum yet acceptable conduction of the contact. Our experiments have provided a permanent bond and yield of chip-chip interconnects on the order of 75%. These yields should be improved as the technology matures.

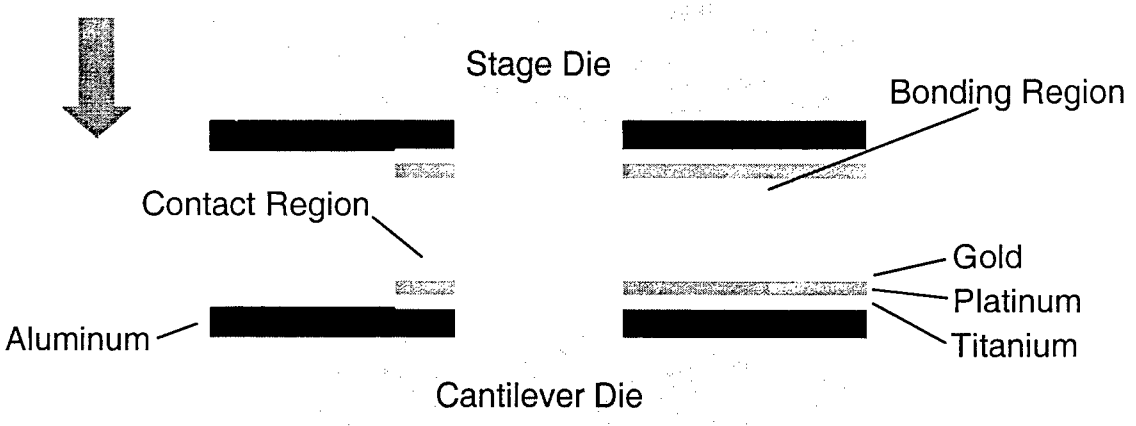

Figure 26. Schematic of wafer level thermocompression bond and interconnect.

Due to process integration concerns, we do not deposit the bonding metal stack during mechanical structure fabrication. The particular integration concern relates to the integrity of the metal during the silicon etches (based on SF_6 chemistries) which define and release the micromechanical structures. Instead, we shadow mask the metals onto the finished wafer during a post-processing evaporation. The shadow mask is made from a kovar sheet, photo-patterned and chemically etched to the dimensions needed for the bonding areas and pads. The flexibility of the kovar fabrication process makes it an ideal material for providing quick-turn shadow masks.

Bonded wafers went through a bond and dice sequence that we developed for the storage element. This scribing process is shown in Figure 27. After the cantilever and stage wafers are bonded, a saw partially cuts through the cantilever wafer. A laser scriber is then used to open channels in the stage wafer to expose the system bond pads. During each cutting process, wafer tape protects the backside of the stages, which contain the through-wafer recesses resulting from the backside of the data platforms.

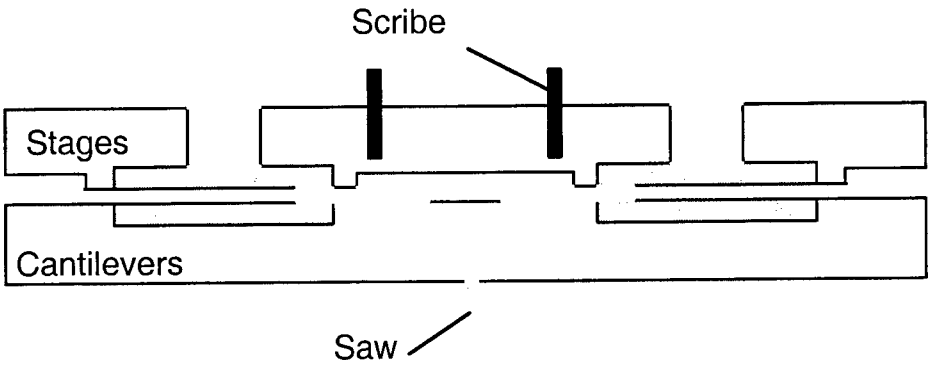

Figure 27. Schematic of the sawing and scribing process to singulate the storage elements.

We have found this singulation process yields mixed results. A large number of particulates are created during the process, and we have discovered water leakage through the seal ring during sawing. The laser scribing also tends to destroy metal leads due to proximity heating. To counteract the yield loss occurring in the sawing and scribing process, most of our experimental results have been obtained by manually clamping the stage die to the cantilever die, which is mounted and wire bonded in a metal package. Since alignment is not critical at this point in the development process, the stage die is positioned manually relative to the cantilever under an optical microscope. Fine adjustment is made with tweezers or probe tips. Once the two chips are aligned, they are clamped using mechanical tabs. With this process, we have obtained good conduction between the two chips without sacrificing sample tilt.

To test the devices after bonding or clamping, we built a series of discrete electronics cards which provide the entire feedback loop for the cantilevers and stage including power distribution, oscillators, phase detectors, and stage drivers. Four separate cantilever channels are available comprising four phase detector boards, four drive boards, a motherboard, and a stage driver board. Front-end charge amplifiers for the four boards are contained within the motherboard where the chip is mounted to minimize noise.

Most of the test results to date have been generated by the 24 cantilever array. The 44 array fabrication has obtained only marginal yield due to insufficient stroke range of the cantilever. Scans of the 2D stage have been made to validate the stage design and baseline the data pattern used for the tests. Figure 28 shows our typical data pattern of uniform 1μm features measured using a

commercial AFM instrument. The bit shape is irregular due to erosion of the original circular feature during actuator definition and release.

Operating the data storage element seeks replication of the data pattern using the assembled stage and cantilever array. During testing we discovered several artifacts that were clouding the images from the system. Because the storage element is assembled, cantilevers are in close proximity to the stage. On cantilevers that were positioned directly above drive voltages or leads, we observed a strong electrostatic tuning effect during scans. The presence of the stage drives actually tune the resonance of the cantilevers, resulting in a phase shift or output from the cantilever circuit. Figure 29 shows the phase output for a cantilever when the x and y actuators on the stage are activated. This particular cantilever is mounted directly above a y stage drive, which correspondingly has the most effect on the output phase signals. Figure 30 is a scan including this effect; although a feature appears, it is actually an artifact of the tuning; the cantilever resonance changes enough to cause the phase detector to flip sign, thereby simulating a phase shift due to a surface feature.

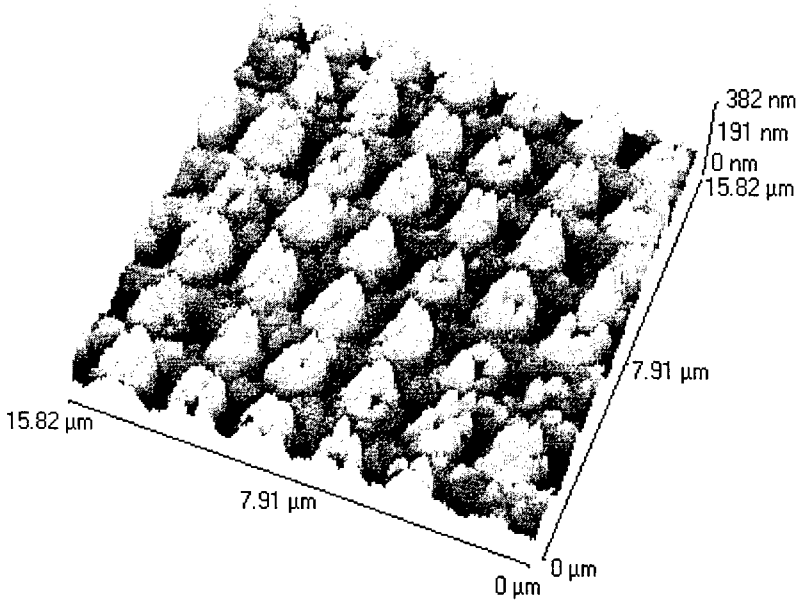

Figure 28. Uniform 1µm data pattern on stage obtained using commercial AFM head.

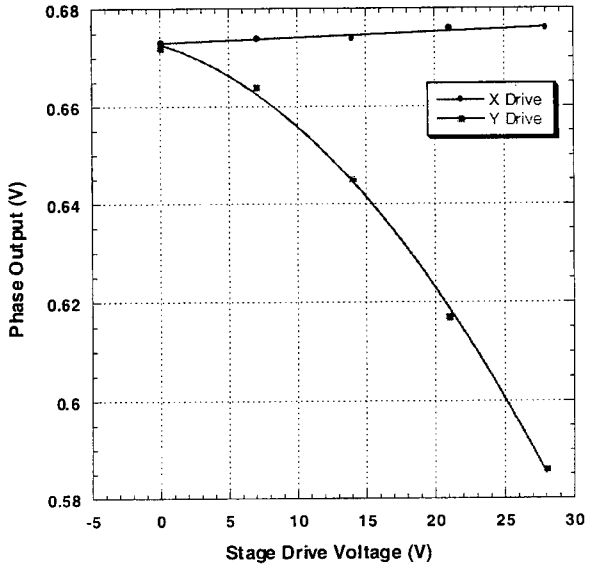

Figure 29. Tuning effect on cantilevers during application of stage drive voltage.

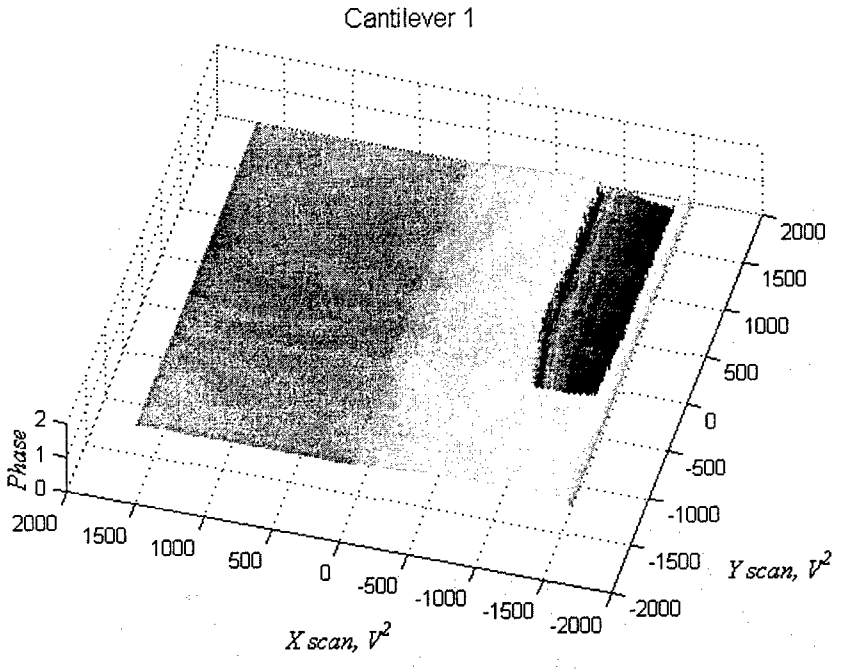

Figure 30. Scan artifact produced by the tuning effect.

Critical for operation of the element is to accurately adjust the tip to stage separation distance. After assembly, we must achieve less than 3μm of separation in order that the cantilever has sufficient stroke to reach the stage. In order to adjust this separation distance, we build a recess into the cantilever wafer so that the tip is located at the proper height. This is a first order

correction to the system; any lack of planarity or levitation in the stage also will affect this separation gap.

Figure 31 is a comparison of two cantilever devices with approximately 1μm of difference in tip recess. The point at which phase output changes from the cantilever reflects the onset of tapping. Large recesses of 5-6μm in the cantilever fabrication are typically necessary to allow the probe tip to touch the data platforms.

Levitation of the stage has been noticed in image scans of the data patterns. Figure 32 is a typical 2D scan we obtain from the system. The faint circular features correspond to the data bits on the platform. For early deflections in the 0 to 2μm range, no image is observed. This is because the data platform is out of range of the cantilever stroke. After approximately 2μm, the stage levitates sufficiently to come within range of the cantilever, at which point imaging occurs.

Figure 33 is a line scan taken from the image in Figure 32. The line scan clearly shows four well defined bits as evidence of the functioning of the device. The tilt in the scan could easily be accounted for using the data recognition algorithms found in conventional storage systems.

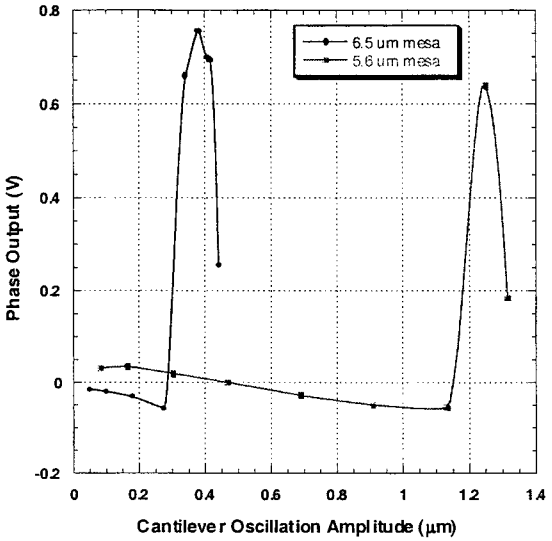

Figure 31. Separation gap between tip and stage is carefully calibrated using recesses in the tip die.

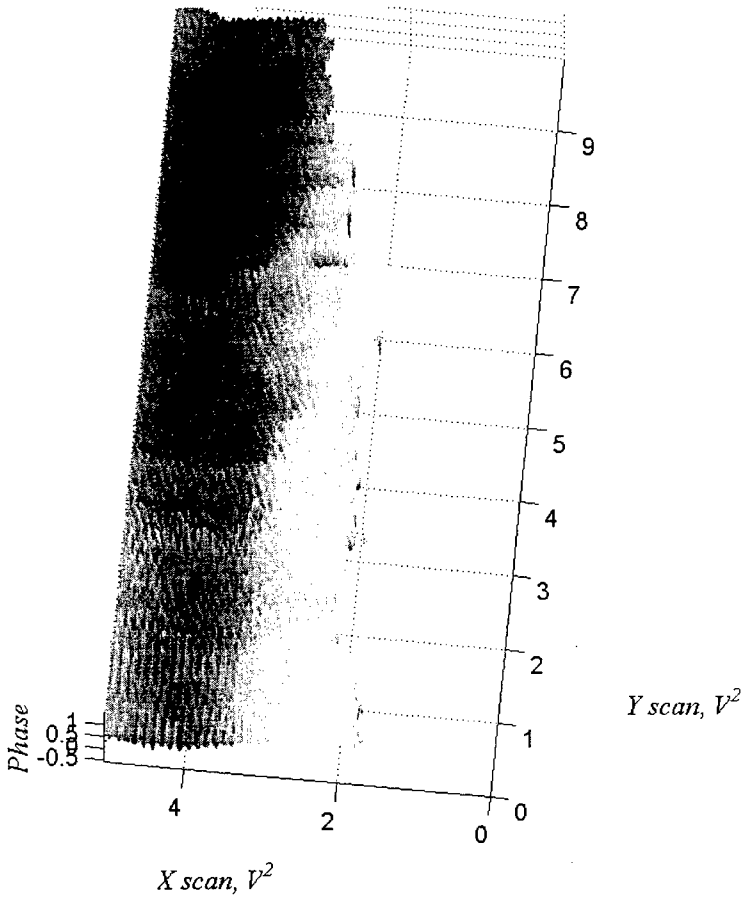

Figure 32. Image produced by storage element replicating data bits as circles in the right half of the image.

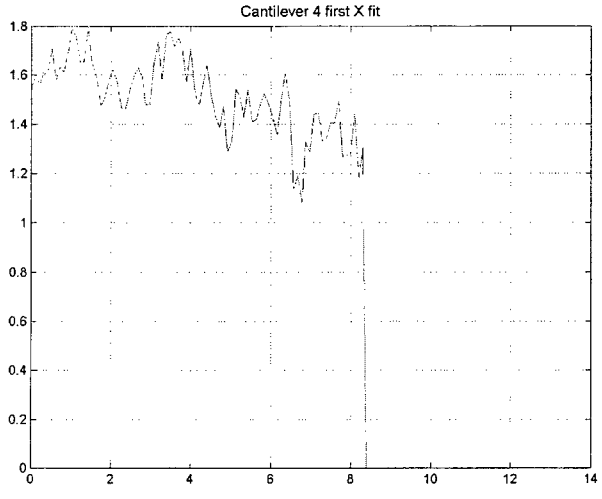

Figure 33. Line scan of Figure 32 clearly showing the phase signal differences or bumps produced by the bits.

6. 100 Mbit System Development

During the project, we attempted to follow the roadmap in Figure 34 for development of the various system iterations. We have completed the design and fabrication iterations for the 24 and 44 cantilever arrays through scaling of the resonance of the cantilever from 8 to 30kHz and reducing the minimum bit size to less than 250nm. The next system iteration of the storage element incorporates a further increase in cantilever resonance (and corresponding reduction in element size) to 100kHz and a reduction in bit size to less than 100nm. More importantly, we also incorporate discrete switching architecture to fabricate a medium array of 100 cantilevers addressed individually. By increasing the scan range of the stage to ±50um, we achieve the same storage (100Mbits) as the roadmap indicates.

Iteration	Date	Cantilever Array	Cantilever Frequency (kHz)	Total Scan Area (μm^2)	Stage Efficiency (%)	Bit Size (μm)	Total Storage Capacity (bits)
Pre-prototype	Jan 99	2x2	8	1,555	0.02	1.00	1.5k
Prototype	Aug 99	4x6	8	36.5k	0.2	1.00	36.5k
Scaling Bit Size	Nov 99	4x11	25	66.8k	0.4	0.25	1M
Switched Cantilevers (end of contract)	Mar 00	25x25	100	950k	2	0.10	100M
Goal: Fully Integrated	Dec 00	100x100	100	25M	≈5	0.05	10G

Figure 34. Scaling roadmap for the storage device iterations.

The increase in the sense frequency (the cantilever resonance) requires us to modify the cantilever circuit by increasing the carrier frequency to 800kHz. This requires complete rework of the oscillator, demodulator, and amplifier design to allow higher frequency operation. More importantly, a switching scheme has been devised to address blocks of cantilevers at one time. The scheme is shown in Figure 35 for a three by three array. The architecture can be scaled easily to a 10x10 system. Note that each cantilever has three capacitors, and are arranged in a matrix. The drive signal to the cantilevers is switched and activates one cantilever is each row. The sense capacitors in each row are shorted together, and hence the charge amplifier for each row processes the signal for the one activated cantilever added with the parasitics from the other cantilevers in the

row. An additional feature of the matrix is a DC voltage which helps to position the active cantilevers.

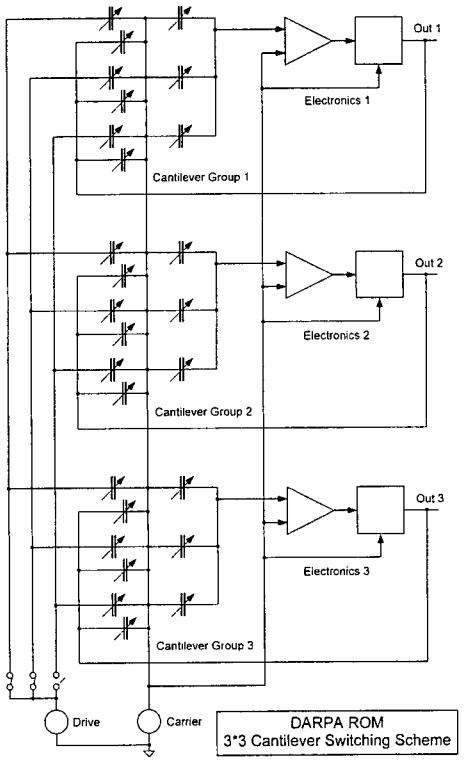

Figure 35. Cantilever switching scheme using discrete components.

The key element to this scheme is how much parasitic capacitance is added by connecting all the sense lines in each row. We have performed a noise analysis on this system using assumptions about the parasitics and lead capacitances from realistic devices. The increase in the noise is minor and can be reduced by increasing the amplitude of the carrier. The resulting signal to noise ratio for the method is acceptable.

Substantive changes have also been introduced to the cantilever and stage mechanical elements in order to provide increased functionality over the previous storage elements. Both the 24 and 44 cantilever system iterations suffered from a number of difficulties which reduced the functional yield and operational stability of the devices. The most difficult problem for the devices was a lack of stroke range of the cantilevers. This was manifested in the inability of many cantilevers to tap the surface, and the inability to tap continuously over a wide stage scan range due to the z-actuation of the stage (the result of stage bow). Both problems are alleviated by increasing the stroke range of the cantilever.

However, the increasing sampling frequency of the cantilevers goes directly against the requirement for increased stroke range. Therefore, we have decided to modify the cantilever structure to include two actuators; one a low frequency, large stroke range frame surrounding a second, high frequency sampling cantilever. A schematic of the new cantilever design is shown in Figure 36. The frame is designed to deflect approximately 10um with low actuation voltage. The actual details of the design, taken from another Kionix product, are proprietary and not reported here. The large stroke range should also be able to account for any planarity variation in the stage, plus nonuniformities in the tip processing that lead to tip height variations across the wafer.

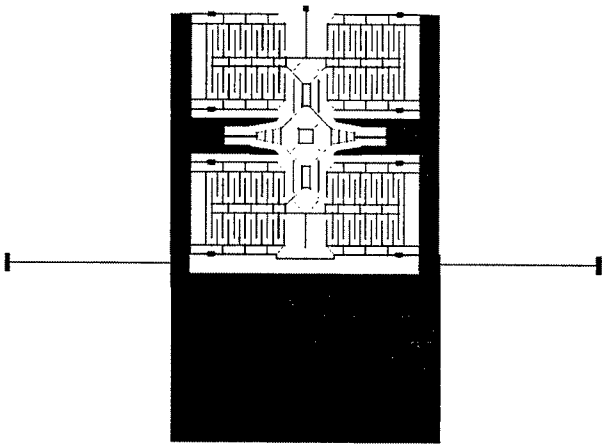

Figure 36. Layout of large stroke range, high sampling frequency cantilever design.

Changing the structure of the cantilever requires a change in the operating mode for the circuitry. However, this new multiple-actuator structure closely mimics the normal operation of a commercial AFM cantilever. Voltage to the large stroke actuator may be used to provide coarse DC control of the cantilever position, as the high frequency cantilever records the onset of tapping. A feedback loop can be constructed where the large stroke actuator voltage is adjusted and becomes the recorded measure of topography. This feedback method is commonly used in both contact and non-contact imaging.

Other improvements have been incorporated into the 100Mbit system design. We also sought to increase the performance of the data stage. Limitations of the previous stages included premature onset of electrostatic instability, tuning of the cantilever resonances, and efficiency of data area. In order to correct these performance characteristics, we incorporated several changes to the stage approach. We included a unique flexure design shown in Figure 37 in order to

further increase actuator deflection without sacrificing electrostatic instability. The flexure is a rigid arm with a pivot point, and is connected to the standard distributed spring design to enhance the deflection of the stage to ±50um. Most importantly, however, we devised a design that buries the actuators beneath the data platform in order to shield the cantilevers from stage drive voltages. This technique also improves the efficiency of the stage to over 2%, allowing a total storage capacity of 100Mbits. A picture of the stage actuator layout is shown in Figure 38.

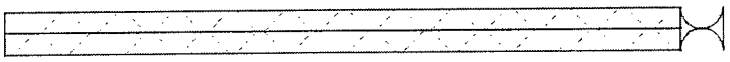

Figure 37. Layout of large stroke range, high sampling frequency cantilever design.

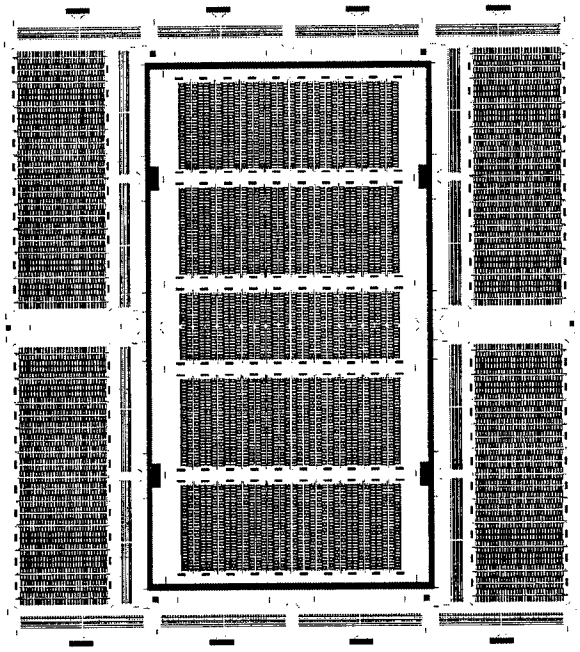

Figure 38. Layout of actuator portion of new data stage.

Shielding the actuators from the cantilevers also allows us to improve the encapsulation methods for the complete system. Currently, we have designed a three-chip stack with data stage, cantilever chip, and lid. By using this method, we can achieve complete alignment and hermiticity before sawing, without the

need for a chip-to-chip interconnect. The current plans call for fabrication of this 100Mbit iteration (stage and cantilevers) for the storage element in 4Q00.

7. Conclusions

During the three years of the project, we have made significant progress toward realizing a MEMS based data storage element. A partial list of the accomplishments is:

- Evolved fundamental plasma micromachining process technology using silicon MEMS with electrical isolation for highly functional actuators
- Incorporated AFM tip and data bit processing for cantilever and stage respectively
- Developed distributed flexure and nested decoupled actuator designs for large 2D stage swept area
- Invented specialized torsional cantilever detection methods for non- and quasi-contact AFM operation
- Implemented gold thermocompression bonding technique to solve chip-to-chip assembly and interconnect issues
- Circuit design, simulation, and construction for stage drivers, cantilever detection, and system integration
- Integrated circuit prototype runs successfully implementing switched capacitor measurement techniques with extremely high precision
- Developed test techniques for discrete cantilever and stage components using commercial AFM
- Demonstration of first industry storage element prototypes with total read-only memory capacity of up to 1Mbit
- Tested cantilever tuning, stage motion artifacts, and sub-micron assembly control in assembled prototypes
- Identified and implemented system scaling necessary to scale storage technology

- Developed 100Mbit stage design using unique flexure and processing flow to increase swept area and reduce imaging nonlinearities
- Added dc offset capability to cantilever using additional degree of freedom to alleviate stroke range difficulties
- Identified and designed interim addressing scheme to reduce pad count for next generation systems
- Provided a sound technology basis for future developments in MEMS based data storage

The most immediate improvement in the functioning of the storage element will be the fabrication of the 100Mbit system. Once the improvements in the construction and functionality of the individual components within the 100Mbit design are incorporated, more consistent operation of the storage device will be obtained. Future work on the storage device will then proceed to include reliability testing of the tip-surface interactions, development of a magnetic read/write mechanism for true erasable storage, and increasing the level of electronics integration. The scaling of the system to a commercial viability will be enabled by the technology developed during the course of this project.

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