REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	30 April 2001	Final Report ; ~~August 1998- June 2000~~ 01 Jun 96 - 31 May 99

4. TITLE AND SUBTITLE
Direct Integration of Ferroelectric LSCO/PNZT Capacitors on Si with Conducting Barrier Layers

5. FUNDING NUMBERS
DAAH04-96-1-0248

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
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8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
U. S. Army Research Office
P.O. Box 12211
Research Triangle Park, NC 27709-2211

10. SPONSORING / MONITORING AGENCY REPORT NUMBER
35845.11-RT-AAS

11. SUPPLEMENTARY NOTES
The views, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy or decision, unless so designated by other documentation.

12 a. DISTRIBUTION / AVAILABILITY STATEMENT	12 b. DISTRIBUTION CODE
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13. ABSTRACT (Maximum 200 words)

: The students (graduate and undergraduate) who were funded by this program, participated in a comprehensive research program that is addressing the materials science issues relevant to the integration of ferroelectric perovskite thin films on silicon substrates for nonvolatile memory applications. These students collaborated with other students, postdocs and guest researchers funded by other sources (both federal as well as industrial) in a "TEAM" environment to address many of the complex issues and in parallel, leveraging the resources invested by the AASERT program. The AASERT funded students worked on two key aspects of the integration problem : (i) growth of ferroelectric PZT (and other derivatives) thin films on poly-Si/Si surfaces using conducting perovskite electrodes : this problem was focused mainly on the materials science of conducting barrier layers ; (ii) reliability studies of the test capacitors fabricated on the aforementioned surfaces. The results of their collaborative efforts have been published in several international journals.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Ferroelectric thin films ; integration on silicon ; reliability testing	18

			16. PRICE CODE
17. SECURITY CLASSIFICATION OR REPORT **UNCLASSIFIED**	18. SECURITY CLASSIFICATION ON THIS PAGE **UNCLASSIFIED**	19. SECURITY CLASSIFICATION OF ABSTRACT **UNCLASSIFIED**	20. LIMITATION OF ABSTRACT **UL**

NSN 7540-01-280-5500

Standard Form 298 (Rev.2-89)
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Sincerely,

FINAL REPORT FOR RESEARCH AGREEMENT NO. DAAH04-96-1-0248
DIRECT INTEGRATION OF LSCO/PNZT FERROELECTRIC CAPACITORS ON Si

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1. Ms. I. Jenkins : Ph.D, June 2000 : Currently with Texas Instruments
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5. Mr. A. Henry, B.S., 1999 (undergraduate intern) : Currently with NRL

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Dr. A. Dhote, Postdoctoral research scientist
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Dr. B. Yang, Ph.D., 1997
Dr. S. Madhukar, Ph.D., 1998
Mr. R. Godfrey, Ph.D. candidate, 2001

PROJECT SUMMARY : This program addressed approaches to integrate thin film $Pb(Zr,Ti)O_3$-based ferroelectric capacitor structures on a filled poly-Si plug, which is a critical requirement for a high-density memory technology. Key materials issues relevant to the development of conducting diffusion barrier layers for integration of these materials on Si wafers are discussed. Specific attention is on the use of conducting perovskite oxide electrodes to contact the ferroelectric thin film. The second part of this program focused on some novel materials that we have investigated for use as diffusion barriers. The principal advantage is that this barrier layer eliminates the use of Pt or Ir, thereby discarding any etching and cost issues associated with the noble materials. A significant portion of the research in

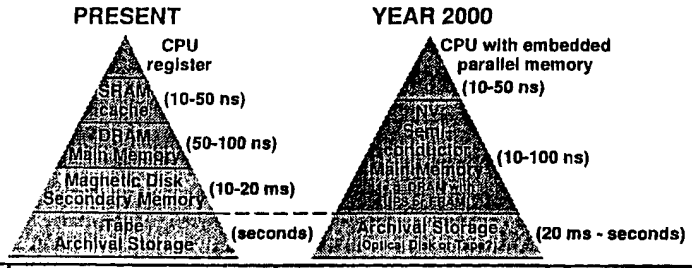
this program was also devoted to understanding the fundamental mechanisms that impact the reliability of the test capacitors.

The students (graduate and undergraduate) who were funded by this program, participated in a comprehensive research program that is addressing the materials science issues relevant to the integration of ferroelectric perovskite thin films on silicon substrates for nonvolatile memory applications. These students collaborated with other students, postdocs and guest researchers funded by other sources (both federal as well as industrial) in a "TEAM" environment to address many of the complex issues and in parallel, leveraging the resources invested by the AASERT program. The AASERT funded students worked on two key aspects of the integration problem : (i) growth of ferroelectric PZT (and other derivatives) thin films on poly-Si/Si surfaces using conducting perovskite electrodes : this problem was focused mainly on the materials science of conducting barrier layers ; (ii) reliability studies of the test capacitors fabricated on the aforementioned surfaces. The results of their collaborative efforts have been published in several international journals, as attached. Also attached are the Ph.D. thesis of Ms. Ingrid Jenkins (a minority student) and the M.S. thesis of Mr. Sadashivan.

INTRODUCTION

The ferroelectric nonvolatile memory technology (NVFRAM) has the potential to take over a large share of the memory market, which was conservatively estimated at about 50-60 billion dollars in 1997 and is expected to possibly double by the next millenium! This raises the obvious question as to what is so unique and valuable about the NVFRAM technology? The answer is shown in the schematic diagram in Figure 1, which compares the current hierarchical architecture of a personal computer to that of a computer of the future. The hierarchical architecture provides a mechanism to interface the very fast microprocessors (CPU) with the reasonably fast random access DRAMS (which are volatile) and finally with the slow but nonvolatile magnetic disk drives. These different sub-systems are interfaced through operating systems thus creating a significant software overhead. Consider for the moment the possibility that one could have a memory element that had all the virtues of the DRAM (i.e., fast, random access, solid state) and the magnetic disk drives (i.e., infinite lifetime and nonvolatile). This would eliminate the entire central section of the hierarchy and would result in a physical architecture. A NVFRAM technology in principle can satisfy all these needs, with the following caveats : (i) the memory should be manufacturable ; (ii) once manufactured it should be reliable ; (iii) once it is reliable, it should be cost-competitive. Each of these caveats is an immense challenge by itself. Researchers worldwide are focusing on all or specific aspects of these caveats, attempting to solve them with the conviction that once all of them are solved a whole new memory technology will emerge. This then formed the backdrop for this program. We focused our attention on key materials issues that we believe will be serious impediments to the development of this technology, if they are not successfully resolved. Specifically we focused on the high-density memory

technology, shown in Figure 2, in which the materials compatibility, interface chemistry and reliability issues are quite stringent [1].



	Virtual Memory Architecture	Physical Memory Architecture	Performance Enhancement
Database access time	10 msec	100 ns	100,000 x
Database bandwidth	3 MBytes / sec	>160 MBytes / sec	50 x
Software overhead	virtual paging file management	essentially none	100 x

Adapted from technical literature of the Ramtron International Corporation (719) 481-7000

FIGURE 1. A schematic comparison of the hierarchical architecture with that of a futuristic physical architecture that will use high speed, solid state random access, nonvolatile memories.

Perovskite or perovskite-like oxides, such as lead zirconate titanate (PZT) and strontium bismuth tantalate (SBT), form a major part of the large family of ferroelectric materials [2]. Among them, although barium titanate is probably the most studied system, the lead-based ferroelectrics and the layered ferroelectrics possess properties that are more interesting from the point of view of nonvolatile memory. We limited ourselves to the lead based ferroelectrics, namely the PZT system and cationically substituted derivatives thereof. Having made this choice, the next step is to make a capacitor on a silicon wafer. Fortunately, this is a well-established architecture used in the DRAM industry and therefore can be easily adopted. Each memory cell consists of one transistor (1T) and one capacitor (1C),

thus leading to the popular 1T-1C nomenclature [3]. The capacitor and transistor are electrically connected to one another, as schematically illustrated in Fig. 2. The figure illustrates the high-density architecture in which the capacitor is located directly on top of the drain of the transistor. In the low-density version the capacitor is laterally displaced with respect to the transistor and electrical connection is established through a metal line. A considerable amount of research and development is currently being focused on the high-density memory technology in which the materials compatibility and interface chemistry issues are quite stringent [1]. Specifically, we focus on the identification and development of conducting diffusion barriers for the high-density memory technology.

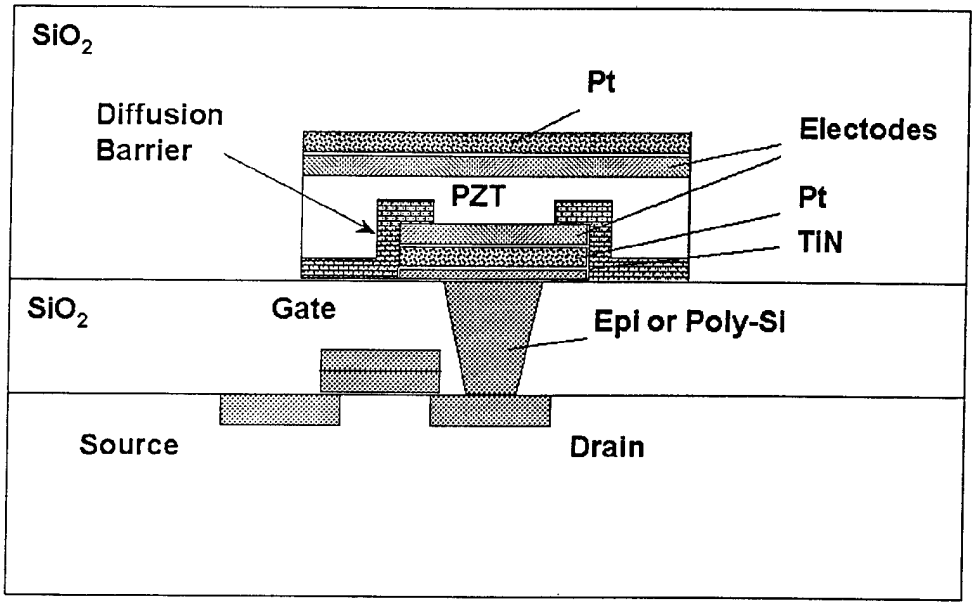


FIGURE 2. Schematic illustration of a high-density, filled poly-Si contact architecture.

A key aspect in the integration on conducting diffusion barrier layers for high-density architectures is that the bottom electrode of the ferroelectric capacitor is in direct electrical contact with the drain of the pass-gate

transistor. This immediately puts drastic materials constraints since oxidation of the poly-Si plug has to be avoided at all costs. Furthermore, Si out-diffusion and lead (or other cationic species) in-diffusion also have to be avoided. Therefore, suitable conducting barrier layers have to be used to prevent any undesirable interface chemistry. Clearly, Pt could be one such material; however it forms a silicide in contact with Si which is Schottky in nature. Therefore, designing conducting barrier layers is an important task that is currently receiving the attention of process engineers and materials scientists in many laboratories. It should be noted that the conducting barrier layer technology is of critical value not only in the FRAM technology but equally valuable in the DRAM technology.

TiN (which is a metallic compound)[4] and other derivatives, in conjunction with Pt or Ir as a multi-layered composite, have emerged as possible conducting barriers. We have been investigating the materials interactions, interface chemistry and structural integrity of (Ti,Al)N / (Pt,Ir) multi-layers as a function of processing conditions. Some general comments regarding the structural integrity are in order. Oxidation of TiN to TiO_2 is accompanied by a volume change (of the order of 60%) and therefore leads to peeling of the layers above the TiN layer and is visible even by optical microscopy. If this can be avoided, then one has to address the second level of problems, namely the possibility of small amounts of oxygen that has diffused through the Pt (or Ir) layer and dissolved in the TiN layer, which leads to an increase in the resistance of this layer. This occurrence is directly related to the crystalline quality of the Pt (or Ir) layer and its thickness. To understand the role of grain boundaries and grain size on the oxidation resistance and ferroelectric properties, we are using both single crystal [001] Si and poly-Si/Si substrates to grow the heterostructures. We have begun this process by first studying epitaxial films, grown on a single crystal [001] Si substrate [5].

Detailed structural and microstructutal investigations have been carried out on such epitaxial heterostructures. Under optimal conditions, we do not observe any lift-off of the layers, thus indicating that the TiN layer is still free of macroscopic oxidation. Transmission electron microscopy studies of cross-sections, Fig. 3, confirm this. An important point to note is that x-ray diffraction studies show no evidence for a pyrochlore phase in the PZT layer. This is one of the most important benefits of using the conducting perovskite layer in the ferroelectric stack. As is always the case, the PZT and PLZT films with LSCO electrodes do not exhibit any fatigue, thus further confirming that fatigue-free PZT-based films can be deposited on a viable conducting barrier layer structure. Similar results were obtained for (Ti,Al)N / Ir composite barrier layers with regards to its structural integrity and the ferroelectric properties of the capacitors.

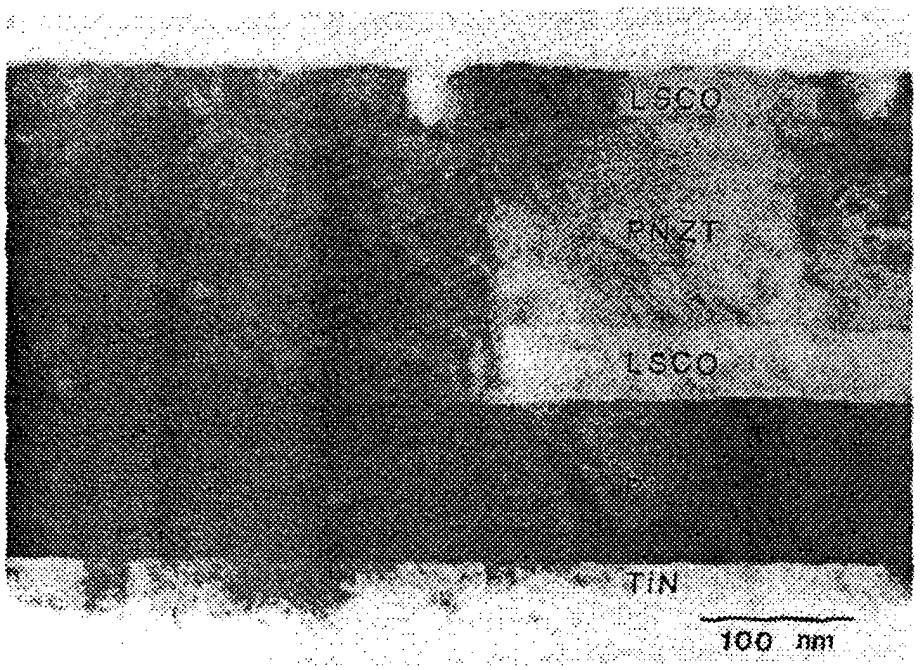


FIGURE 3. A TEM micrograph of epitaxial LSCO/PNZT/LSCO capacitor grown on a Pt/TiN conducting barrier composite on Si.

Some concerns with the use of Pt and Ir composite barrier layers include the difficulty in etching Pt and Ir; cost and availability of these noble metals; and hillocking on their surface when exposed to oxygen. To overcome these problems, we have also been investigating new material systems such as Ti-Al and Ni-Al alloys that would exclude the use of Pt and Ir. These systems were selected based on their ability to form amorphous phases. The philosophy is that eliminating grain boundaries would improve oxidation resistance and retard diffusion of any species through the layers.

Fig. 4 shows a cross-sectional TEM picture of the ferroelectric stack using LSCO electrodes on Ti-Al. As is clear from the image there is no macroscopic reaction between the LSCO electrodes and the ferroelectric, PNZT. Notice that there is no macroscopic reaction between Ti-Al and LSCO or p-Si and Ti-Al. Further, as reported in an earlier study, we observe no discernible oxidation of Ti-Al as evidenced by RBS spectra of the Ti peak before and after fabrication of the ferroelectric capacitor.

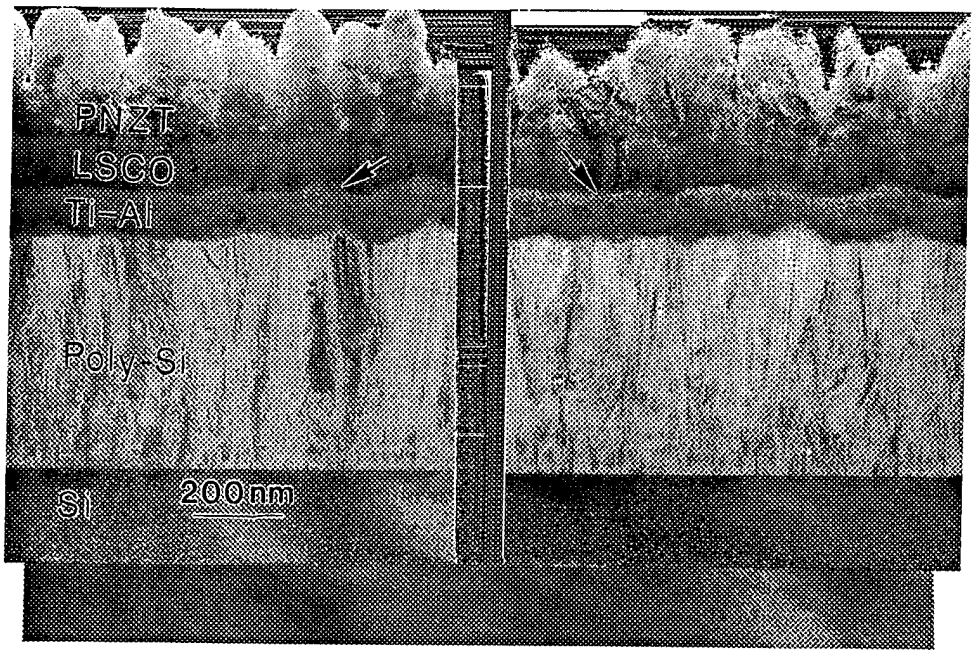


FIGURE 4. A TEM micrograph of a polycrystalline LSCO/PNZT/LSCO capacitor grown on Ti-Al/poly-Si/Si, showing that high quality ferroelectric capacitors can be integrated on Si using such simple conducting barriers.

To further confirm that there is no electrical discontinuity between the poly-Si layer and the bottom electrode of the ferroelectric capacitor, we measured the ferroelectric properties of the capacitors, LSCO/PNZT/LSCO by making contact to the conducting poly-Si layer. Fig. 5(a) plots the hysteresis loops for one such typical capacitor up to 12V. The remanent polarization and the coercive voltage of the ferroelectric capacitor are plotted in Fig. 5(b). The capacitors start to saturate at ~ 7V and have a remanent polarization of ~ 28$\mu C/cm^2$ and coercive voltage of ~ 1V measured at 5V. The resistivity of the capacitors is ~ $8x10^9$ Ωcm and did not change much with increasing voltage, indicating robust capacitors. More importantly, the measurements were done with contact to the poly-Si layer

confirming that there is electrical continuity between that layer and the bottom electrode of the ferroelectric capacitor.

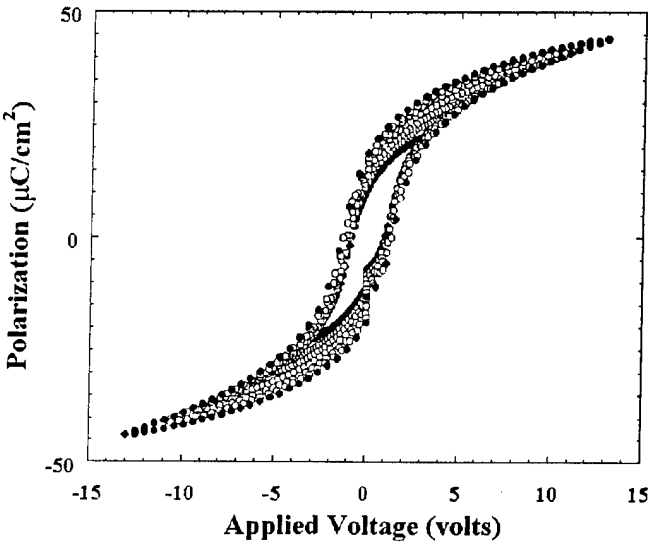


FIGURE 5(a). Hysteresis loops for a typical LSCO/PNZT/LSCO capacitor integrated on Si using Ti-Al conducting diffusion barrier.

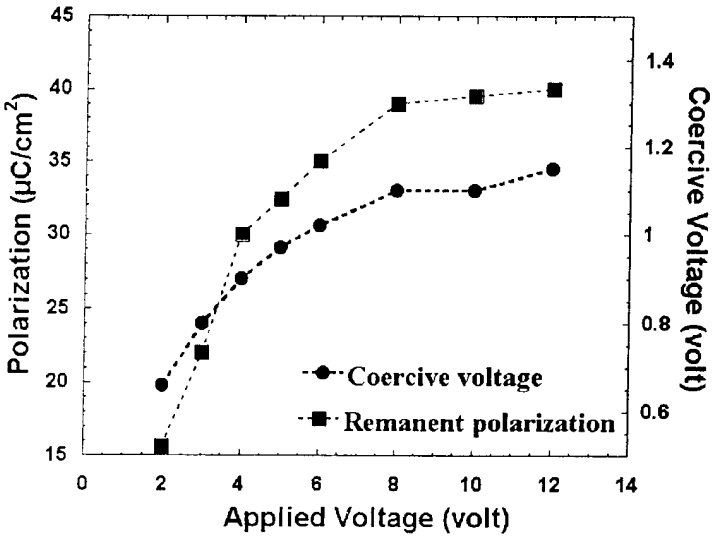


FIGURE 5(b). Remanent polarization and coercive voltage for a typical LSCO/PNZT/LSCO capacitor grown on Ti-Al/poly-Si/Si.

Similarly robust capacitors were also fabricated using SRO electrodes. Fig. 6(a) plots the polarization-voltage curves for a typical SRO/PNZT/SRO capacitor. The remanent polarization and coercive voltage of the capacitor are plotted in Fig. 6(b). Notice that the capacitor starts to saturate at ~ 5V and has a remanent polarization of ~ 31$\mu C/cm^2$ and coercive voltage of ~ 0.7V measured at 5V. The resistivity of the capacitors was ~ 10^{10} Ωcm and did not change much with increasing voltage.

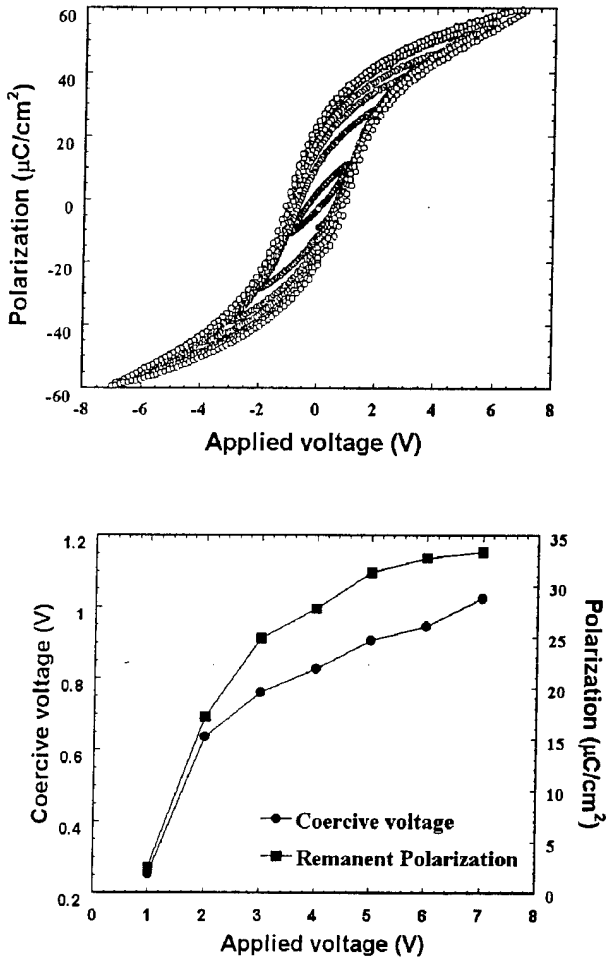


FIGURE 6. Electrical properties of a typical SRO/PNZT/SRO capacitor integrated on Si using Ti-Al conducting diffusion barrier; (a) hysteresis loops; (b) remanent polarization and coercive voltage.

To characterize a ferroelectric capacitor for high-density memory applications, its high-speed pulse polarization response must be measured. Furthermore, this response must be characterized from the point of view of the operation of a memory device. This defines the important properties that need to be measured, i.e. (i) fatigue; (ii) retention; (iii) imprint; (iv) other time dependent degradation phenomena; (v) process damage; (vi) scaling of these properties with the capacitor size (see Ingrid Jenkins Ph.D. thesis). Fig. 7 plots the pulse width dependent polarization of both SRO/PNZT/SRO and LSCO/PNZT/LSCO capacitors from 1μs to 1s at 3V. The remanent polarization values, viz., ~ 15μC/cm^2 at pulse widths of 1μsec and 3V operation certainly merit serious consideration for use in actual high-density memories that will likely function with operating voltage levels in this range [6]. Detailed characterization of the ferroelectric properties of these heterostructures show attractive fatigue, retention and imprint properties, which are discussed in the following sections.

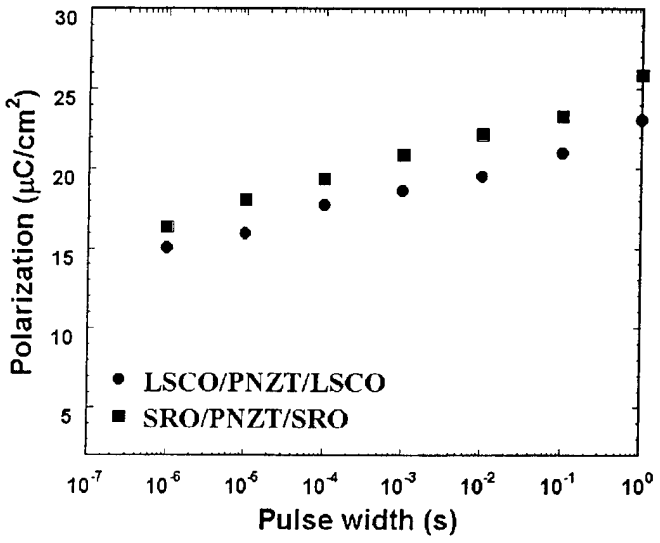


FIGURE 7. Pulse width dependence of remanent polarization for PNZT capacitors with LSCO or SRO electrodes measured by making contact to the poly-Si layer.

Fatigue is the progressive loss of switchable polarization with repeated bipolar cycling. In the hysteresis loop, this manifests itself as a progressive drop of the P_r value. Bipolar fatigue test was performed on both PNZT capacitors with LSCO and SRO electrodes using square pulses of amplitude 5V at 1MHz. Fig. 8 plots the results from such a test that was performed by making contact to the conducting poly-Si layer. The capacitors show a loss of ~ $2\mu C/cm^2$ after 10^{11} cycles. This performance of the capacitor is no surprise and several studies have demonstrated that by using conducting oxide electrodes [7-9] fatigue can be eliminated in PZT capacitors.

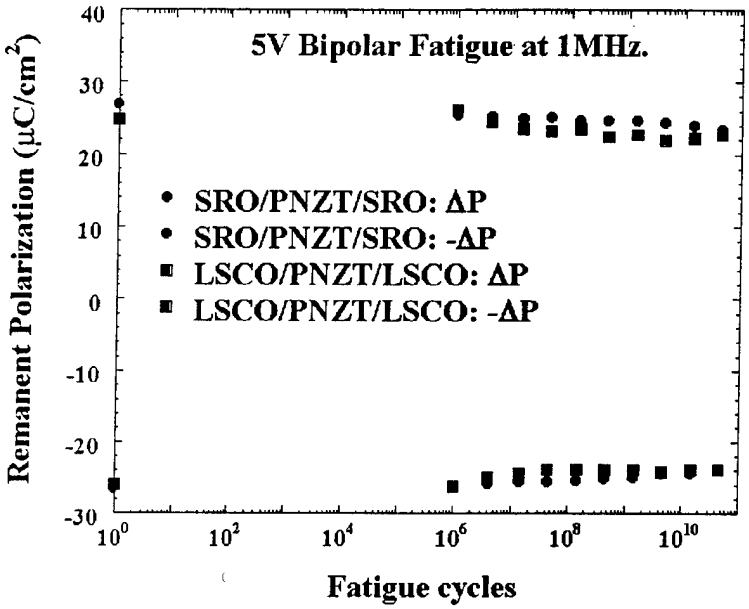


FIGURE 8. Bipolar fatigue for PNZT capacitors with LSCO and SRO electrodes integrated on Si using Ti-Al as a conducting diffusion barrier.

Another fundamental property that is desired in ferroelectric memories is logic state retention [10]. Retention has two components: the first is the ability to retain the polarization state that the capacitor is put into; the second is the ability to distinguish between logic "1" and "0." The

difference in polarization values between these two states (in an actual memory this translates into voltage differences) should be at least $2\mu C/cm^2$. Fig. 9 plots the results from a retention test performed on typical PNZT capacitors with LSCO and SRO electrodes. The capacitors were written with a pulse (pulse width 0.07ms) of negative polarity and amplitude of 5V and read with 5V pulses (pulse width 0.14ms). Both capacitors show attractive retention characteristics from a memory point of view.

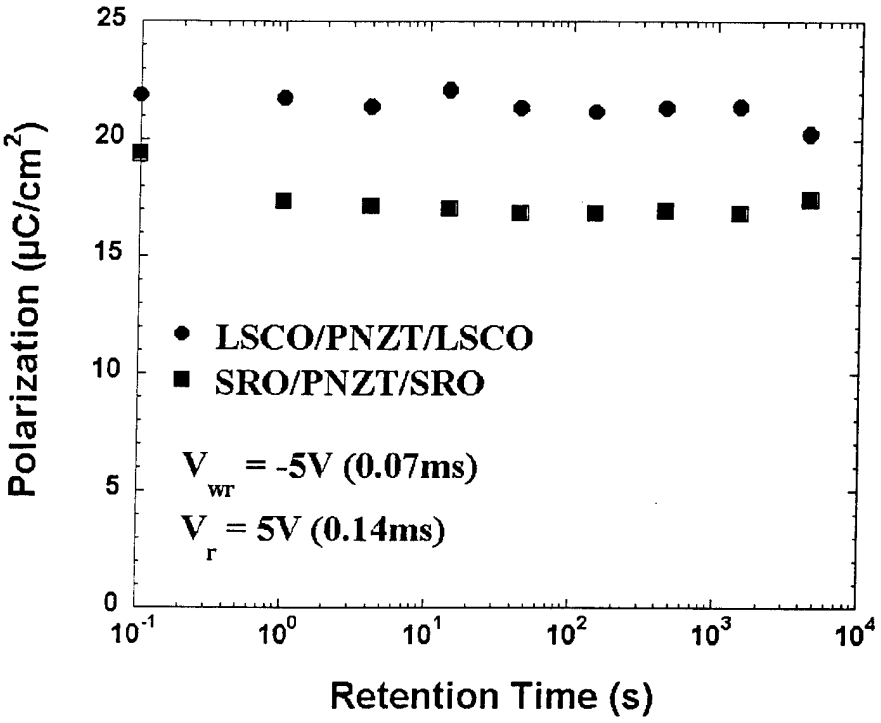


FIGURE 9. Logic state retention for PNZT capacitors with SRO and LSCO electrodes showing good retention characteristics.

Imprint is an issue that is being addressed in great detail by several research groups. In simple terms imprint is the development of an internal field in the capacitor and manifests itself as a progressive shift of the hysteresis loop along the field axis (see Sadashivan M.S. thesis). Why is this important? To put this in perspective, one needs to understand some of the

potential application markets of ferroelectric memories. Among them, the Erasable Programmable Read-Only Memory (EPROM) and the Electrically Erasable Programmable Read-Only Memory (EEPROM) markets are prime targets, since they are also nonvolatile memories, but have limited number of write operations. An EPROM is typically used in a write once and read many times mode. For example, the memory could be programmed into one logic-state, which could subsequently be read a few million times. Since the read process involves the application of a pulse of the same polarity, the storage element will repeatedly see voltage pulses of the same polarity, i.e., it effectively sees a dc field. Translate this to a ferroelectric memory: the ferroelectric capacitor, used under these conditions, will experience repeated unipolar pulses. Under these read conditions, there exists a strong possibility for charged defects in the capacitor to transport across the capacitor, segregate at one of the electrode-ferroelectric interfaces and create an internal field. This internal field shows up in hysteresis measurements as a shift of the loop along the field axis while in pulsed polarization measurements $P^* - |-P^*|$ and $P^\wedge - |-P^\wedge|$ [11]. Imprint failure occurs when one of the coercive fields goes to zero (i.e., one polarization state becomes unstable and reverts to the opposite state). In terms of pulse polarization, this happens when $P^* = |-P^\wedge|$ or $P^\wedge = |-P^*|$. The formation of this internal field can happen with or without the assistance of temperature. In general, tests to study imprint are carried out under two conditions: (i) Static imprint, in which the sample is put into a polarization state and the heated to the desired temperature (for example, 100°C) and held for a fixed period of time (e.g., 1 hour). Imprint stress in this case is purely thermal. (ii) Dynamic imprint in which single-sided pulses (or a dc field) are imposed on the capacitor in addition to the thermal stress. Resistance to the development of such an internal field is an important requirement in ferroelectric memories.

We have performed dynamic imprint tests on LSCO/PNZT/LSCO capacitors and the results are plotted in Fig. 10. The primary experiment

consists of a combined thermal and electrical (i.e., single-sided fatigue) stress profile that is impressed upon the test capacitor. To quantify the effects of test variables on imprint, we use a figure of merit (FOM) based on the relative shift of the hysteresis loop given by [12]:

FOM 1 = [(+Vc,final) + (-Vc,final)] / [(+Vc,initial) - (-Vc,initial)].

In this framework, FOM of +1 or -1 would mean an imprint failure. As is clear from the figure, there is no imprint failure up to 10^9 single side 5V pulses at 180°C. As mentioned earlier, such a combined thermal and electrical stress profile is quite stringent and provides a rigorous measure of the quality of the ferroelectric capacitor. This indicates that the LSCO/PNZT/LSCO capacitors are robust. Similar tests are currently being performed on SRO/PNZT/SRO capacitors and will be publisher elsewhere.

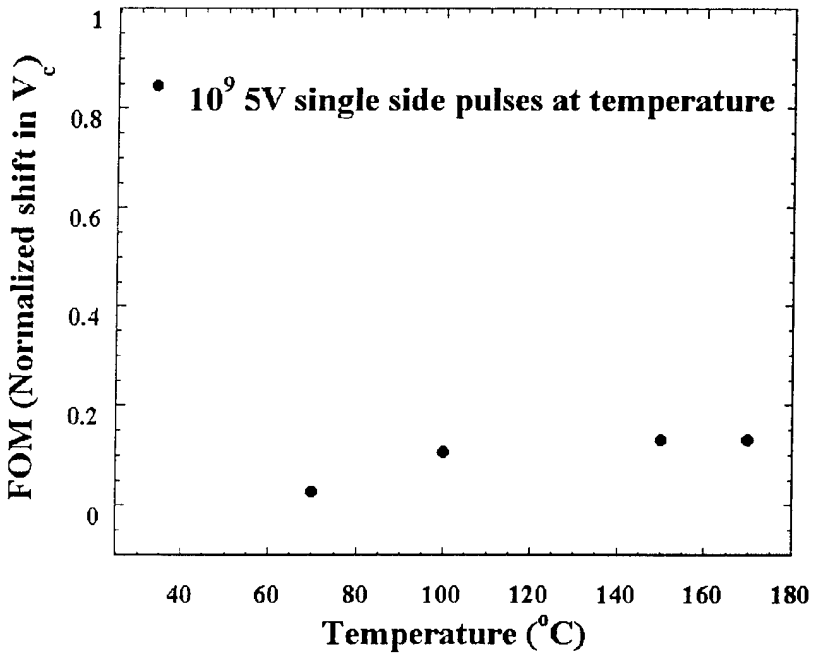


FIGURE 10. Dynamic imprint results for LSCO/PNZT/LSCO capacitors integrated on Si using Ti-Al as a conducting diffusion barrier. Tests were performed by making contact through the poly-Si.

SUMMARY

Ferroelectric thin films for nonvolatile memories are poised for rapid development and production. The past few years have witnessed rapid progress in thin film processing and understanding of the interplay between processing and the fundamental aspects impacting reliability. Specifically, the use of metallic oxide electrodes to alleviate the problems of fatigue and imprint in PZT based ferroelectrics is noteworthy. We have also demonstrated that the ferroelectric capacitors can be deposited on Si wafers with conducting barrier layers enabling direct electrical contact to the drain of the pass-gate transistor. The ferroelectric properties of the test structures, i.e. LSCO/PNZT/LSCO and SRO/PNZT/SRO capacitors hold considerable promise for further development. Future focus should be on processing issues, such as the development of a manufacturable dry etch, reducing process damage and increasing wafer / lot level yield need to be focused on.

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