Final Technical Report

Materials Processing and Device Development to Achieve Integration of Low Defect Density III Nitride Based Radio Frequency

Supported under Grant #N00014-99-1-0971
Office of the Chief of Naval Research
Report for the period 8/1/99 – 4/30/01

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20010508 082

April, 2001

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

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1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	April 30, 2001	Final Technical 8/1/99 - 3/31/2001

4. TITLE AND SUBTITLE

Materials Processing and Device Development to Achieve Integration of Low Defect Density III Nitride Based Radio Frequency

5. FUNDING NUMBERS

6. AUTHOR(S)

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

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8. PERFORMING ORGANIZATION REPORT NUMBER

N00014-99-1-0971

9. SPONSORING/MONITORING AGENCY NAMES(S) AND ADDRESS(ES)

Sponsoring: ONR, Code 312, 800 N. Quincy, Arlington, VA 22217-5660
Monitoring: Administrative Contracting Officer, Regional Office Atlanta
Suite 4R15
100 Alabama Street, NW
Atlanta, GA 30303-3104

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for Public Release; Distribution Unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

Gallium nitride HEMTs were successfully fabricated and tested on silicon substrates. Gallium nitride HEMTs produced on Si substrates had normal current voltage characteristics; however, the transconductance and saturation current density were low. It is believed that this is due to the fact that the GaN epi layers were not optimized on the initial wafer runs. These initial results validate that GaN HEMTs can be produced on low cost silicon substrates and support the position that continued funding in this area will lead to improved performance that may provide a better performance/cost ratio than GaN devices on more expensive substrates such as SiC and sapphire. Other accomplishments include construction and commissioning of a proprietary 100 mm III-Nitride MOVPE system specifically designed to address the uniformity issues required for commercial applications, development of a process route for the growth of GaN on Si(111), demonstration of growth of GaN on 50-mm and 100-mm diameter Si(111) substrates, and the first demonstration of a GaN-based high electron mobility transistor on a 100-mm platform.

14. SUBJECT TERMS

gallium nitride, HEMTs, mesa isolation process, ohmic contacts, mask, epitaxial growth, HFETs, MOVPE, pendeo-epitaxial growth

15. NUMBER OF PAGES

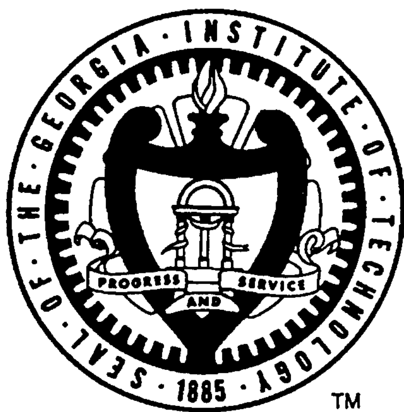
34

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLAS	UNCLAS	UNCLAS	SAR

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std Z39-18



Project A6043 Final Report

Heterogeneous Integration of GaN on Silicon

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March 31, 2001

Final Technical Report for the Period (August 1, 1999 through March 31, 2001)

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Under Contract 1999-1479-01
Prime Contract N00014-99-1-0971

Acknowledgements

The authors extend our thanks to Dr. Davis and his team of researchers at NCSU for the outstanding collaboration and support during this project. We also thank Dr. Kevin Linthicum, Dr. Thomas Gehrke and Dr. Robert Therrien of Nitronex for providing materials and processing support.

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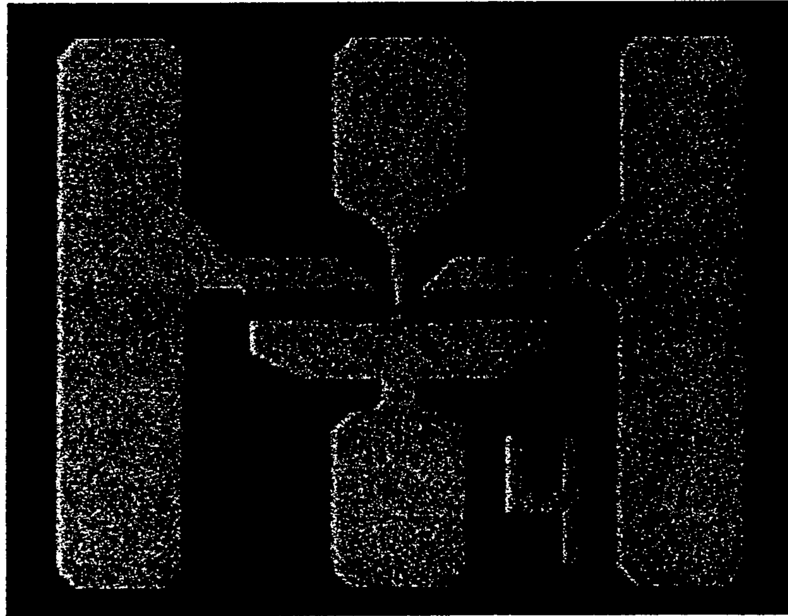
1. Executive Summary

The Georgia Tech Research Institute (GTRI) successfully fabricated and tested GaN HEMTs on silicon substrates. This was the primary objective of the program for the NCSU team. GaN HEMTs produced at GTRI on silicon substrates, had normal current voltage characteristics; however the transconductance and saturation current density were low. GTRI believes that this is due to the fact that the GaN epi layers were not optimized on the initial wafer runs. **These initial results validate that GaN HEMTs can be produced on low cost silicon substrates and support the position that continued funding in this area will lead to improved performance that may provide a better performance/cost ratio than GaN devices on more expensive substrates such as SiC and sapphire.**

GTRI developed and optimized all of the wafer processing steps necessary to make GaN HEMTs and designed a mask set that allowed higher yields and facilitated RF probing more easily than the mask set previously used. GTRI provided the mask set design to Nitronex, a team member. All of the processing steps were refined and fully documented in a "run traveler". Using this run traveler, devices with appropriate physical dimensions were produced and tested. The photograph below shows a one-micron gate length GaN HFET fabricated on a SiC substrate using the process procedures developed on this program. Drain to source spacing of this device is 3.5 microns and on-wafer probing can be used to measure performance. State of the art ohmic contacts were demonstrated. This report summarizes our work and provides detailed results.



GaN HFET Fabricated at GTRI.

2. Materials

GTRI received materials from NCSU and Nitronex. We also purchased three two-inch wafers from Epitronics. Electrical data on the Epitronics' wafers are shown in Table 1. Figure 1 is a diagram of the layer structures grown by Epitronics for this project.

Wafer number	400417E	400418A	400418B
Number of points	55	55	55
Average measurement	505.9 ohm/sq.	508.0 ohm/sq.	518.5 ohm/sq.
Max. value	525.6 ohm/sq.	536.5 ohm/sq.	549.2 ohm/sq.
Min. value	483.8 ohm/sq.	481.4 ohm/sq.	500.3 ohm/sq.
Variation in measurement	8.262 %	10.835 %	9.437 %
Std. deviation from average	11.51 ohm/sq.	11.09 ohm/sq.	11.61 ohm/sq.
Uniformity of wafer	2.27%	2.18%	2.23%

Table 1. Epitronics GaN/Sapphire Wafer Sheet Resistance Statistics.

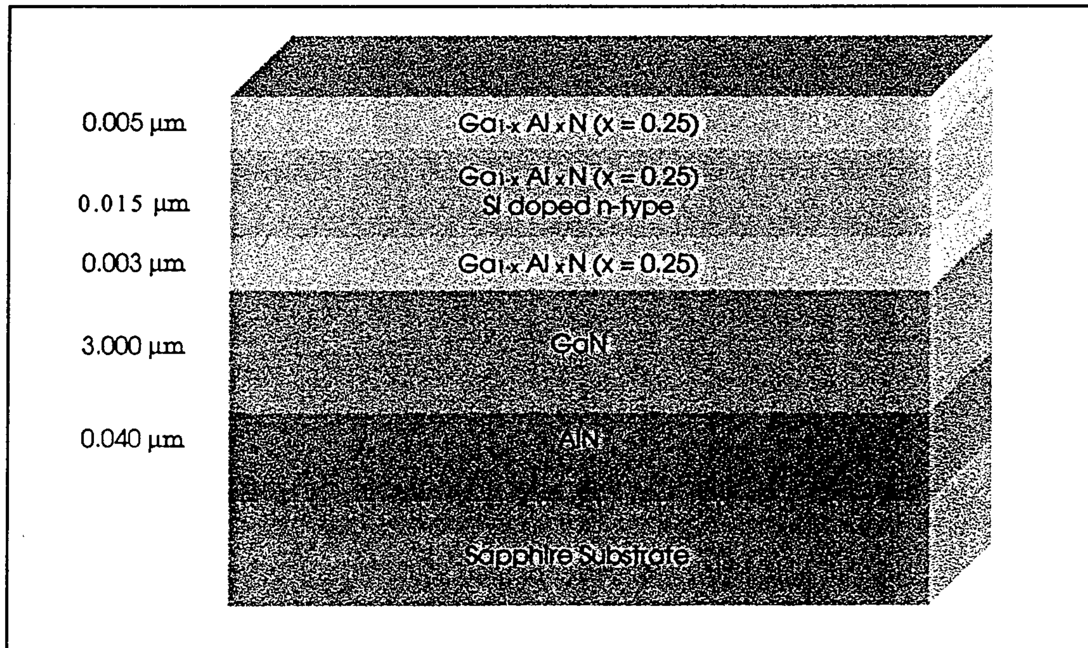


Figure 1. Epitronics Wafer Layer Structure.

3. Process Development

GTRI conducted experiments on various processing steps and processed two GaN pieces along with numerous initial test runs on GaAs to obtain an acceptable parametric performance and to develop a detailed process run traveler. Both GaN pieces processed consisted of a GaN epi-layer structure grown on SiC by NC State. The initial run on GaN Wafer TG-436 produced unacceptable results. GaN Wafer DT-703 contained properly defined structures with correct dimensions.

3.1 Mesa Isolation Process

To create a well-defined mesa structure using RIE, a nickel mask procedure was used as shown in Figure 2.

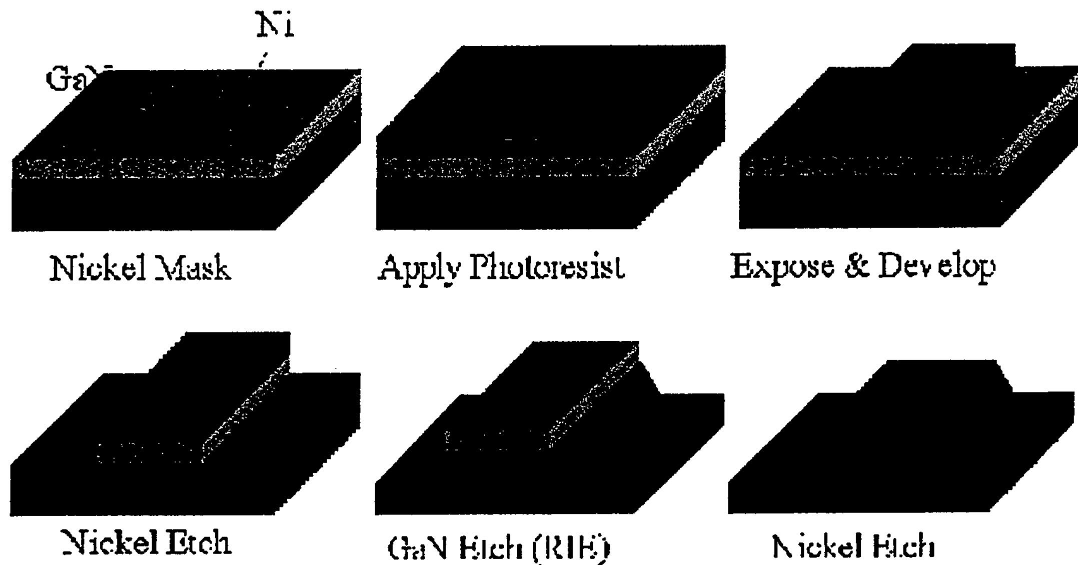
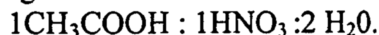


Figure 2. Nickel Mask Procedure for Mesa Isolation.

A layer of 1000 angstroms was deposited onto the GaN piece using e-beam evaporation. Positive photoresist (Shipley 1813) was spun at 5000 rpm's to achieve a PR thickness of 1.1 microns. Exposure time was determined to be best at 6 seconds with an exposure setting of 10 mJ/cm^2.

After developing, the nickel was etched away from exposed areas in the PR using a mixture of acetic acid and nitric acid and DI water. This etchant was used in the following ratio:



$1CH_3COOH : 1HNO_3 : 2\ H_20.$

The nickel pattern protected the GaN active layer during the RIE process. After the GaN was etched with RIE, the nickel was removed using the acetic/nitric acid solution. This created well-defined mesa structures with steep walls and sharp edges (Figure 3).

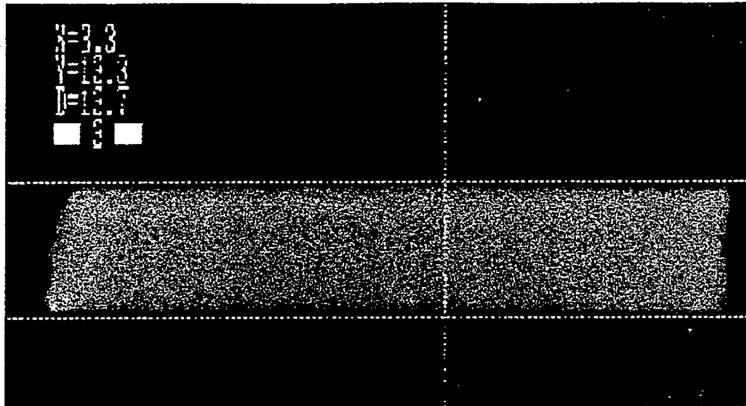


Figure 3. Mesa Structures constructed through RIE.

GTRI found that photoresist not removed before the RIE Etch step will be difficult to remove from the wafer later (Figure 4). An oxygen plasma stripper was the most effective means to remove stubborn PR.

Figure 4. PR adhering to GaN surface after Mesa Etch Procedure.

3.2 Ohmic Contact Process

Positive PR (Shipley 1813) was spun on for a 1.1 micron PR thickness. Through experimentation, an exposure setting 10 mJ/cm^2 for 6 seconds was determined to create acceptable ohmic contact patterns. Proper spacing, between ohmic contacts, was achieved by using the conditions listed above. Figure 5 shows these features.

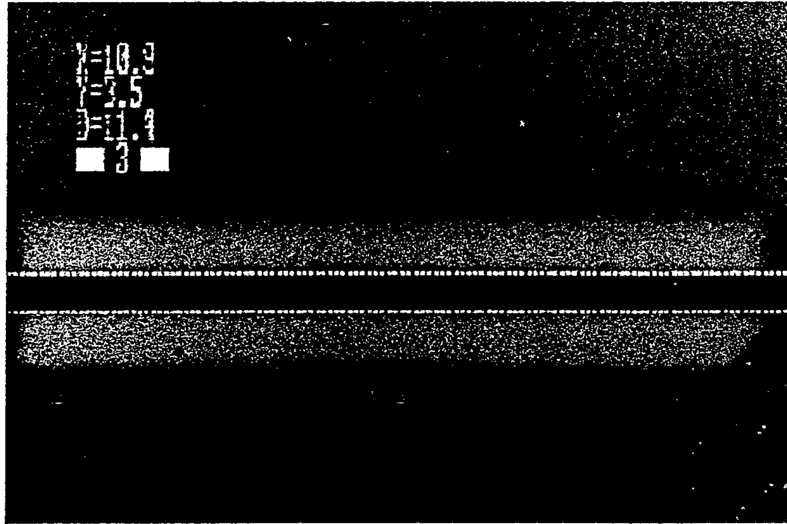


Figure 5. Ohmic Contact Separation of 3.6 Microns.

A five second RIE etch process was used before evaporating the ohmic metals. This roughened the surface and allowed better adhesion of the ohmic metals. Figure 6 is a scanning electron micrograph of a wafer piece after the RIE etch. It is key to note that the photoresist overhang is not damaged and that there is a clean break between the metallization on top of the resist and the metal in the ohmic contact region.

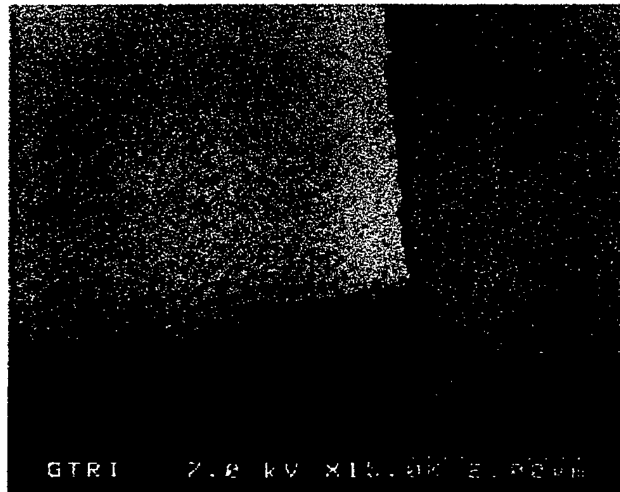


Figure 6. GaN Surface after 5 second RIE Scuff.

The original problem of the ohmic contact deformation during RTP annealing process, shown in Figure 7, was minimized through RTP optimization experiments. These annealing tests took place at the Georgia Tech Microelectronics Research Center, NC State, and Nitronex Corporation.

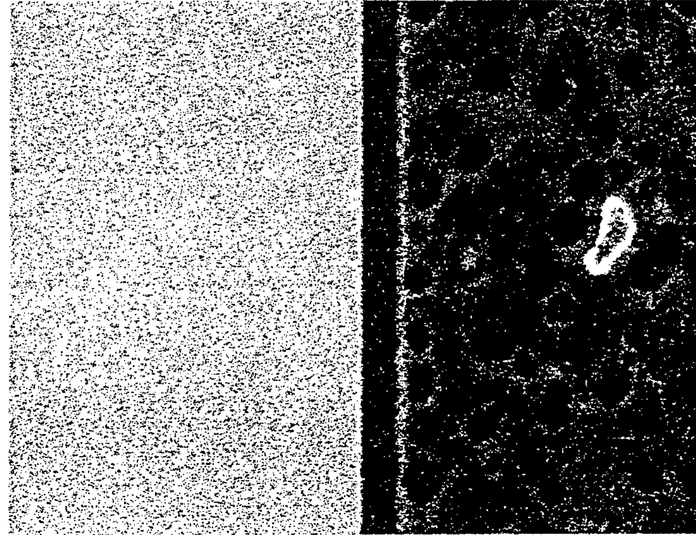


Figure 7. Comparison: Gate Metal shown on Left, Ohmic Metal shown on Right.

Before annealing, the ohmic contacts appeared to have a golden color and were lustrous with sharp edges. After annealing, the metals bubbled and fused together; higher temperatures resulted in more fused appearances. A negligible change in the gate width was observed in the temperature range 800-850°C. Slight protrusions were observed along the edges of the ohmics regardless of the annealing temperature. These protrusions would have a significant effect on gate alignment and performance of the device. They were best minimized between 820-850°C.

Annealing at 850°C for 30s was found to be optimal as it ensured the proper alloying of the metals, the least reduction in gate width, and an overall increase in consistent morphology of the ohmic contacts. The following images show that the ohmic contacts remain intact, the metals have been alloyed properly, and that the contact separation is sufficient for gate placement (Figure 8).

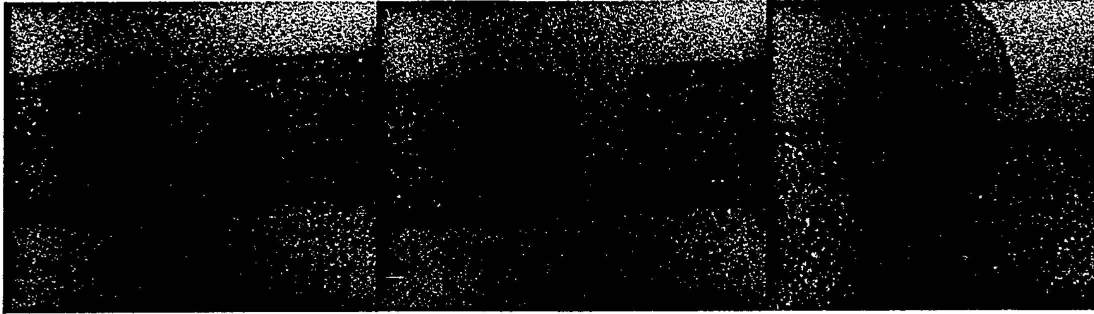


Figure 8. Ohmic Metal Annealed at 850°C for 30 Seconds.

3.3 Gate Process

Positive PR (Shipley S1808) was spun to attain a PR thickness of 0.8 μm. Gate definition and yield were found to be excellent when using an exposure time of 7 seconds, exposure setting of 10 mJ/cm^2, and developing time of 45 seconds (Figure 9). A Ni/Au scheme was placed on the wafer through e-beam evaporation. An adhesion problem was observed when the gate metal would peel on contact with test probes. Ti/Au was experimented with as the gate metal, resulting in good adhesion to the substrate without loss of device performance. Increasing the amount of nickel used from 100 μm to 300 μm in the Ni/Au scheme also allowed better adhesion.

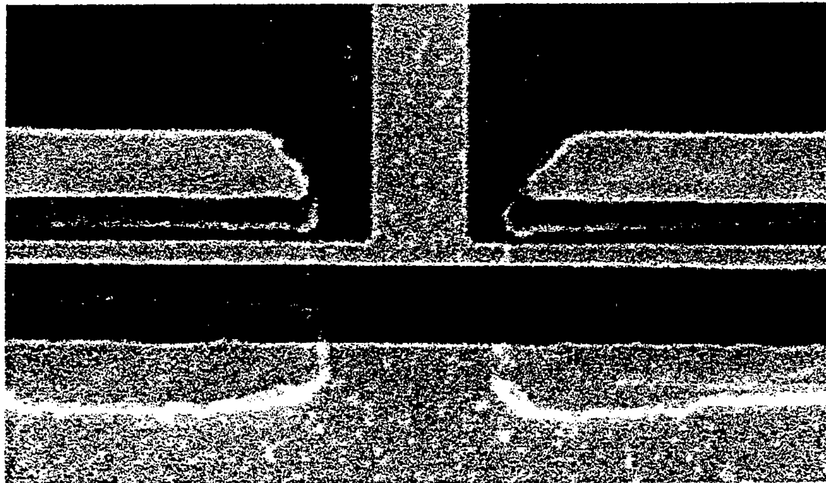


Figure 9. Thin Gate located between Ohmic Contacts.

4. Mask Design

A mask set was designed and created to generate higher yields and ease on-wafer testing. Specifications for the mask design were:

- All devices were to be oriented in the same direction
- All devices, including diagnostic devices, should fit in a uniform unit cell
- All devices will have two sets of three contacts set at specific distances to facilitate test probes.
- Alignment markings will be included in each unit cell.
- The streets (separation between unit cells) were defined to be uniform and wide to accommodate dicing.

The mask design consisted of devices having varying gate widths of 75, 150, and 300 μm. A gate length of 1 μm was uniform on all devices. Diagnostic structures were included on the mask sets. The finished mask set design including diagnostic devices is shown in Figure 10.

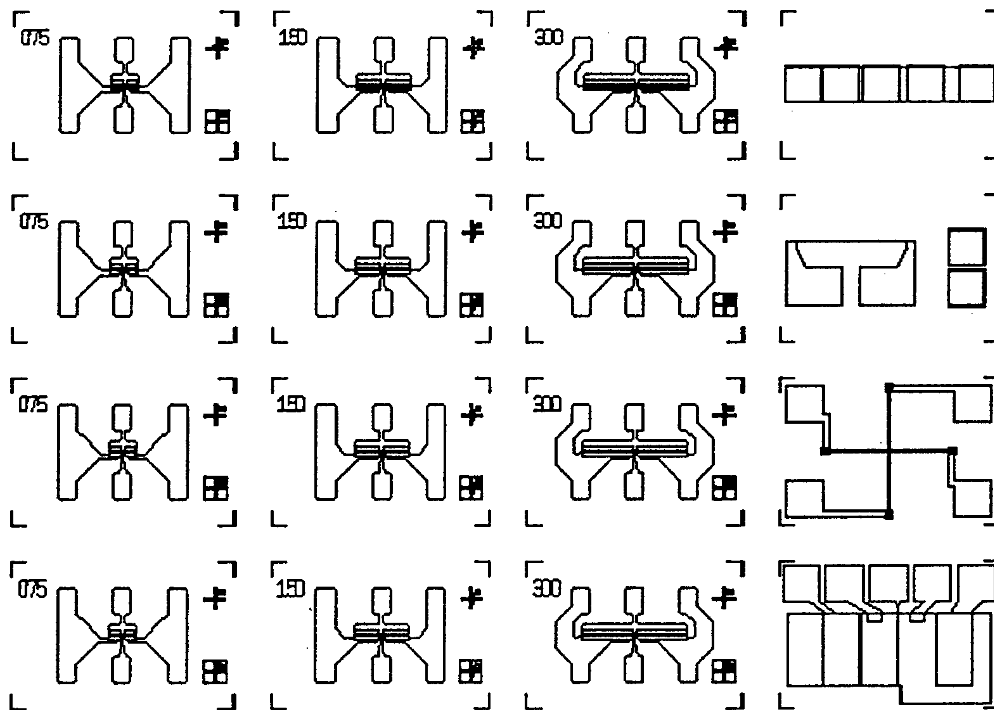
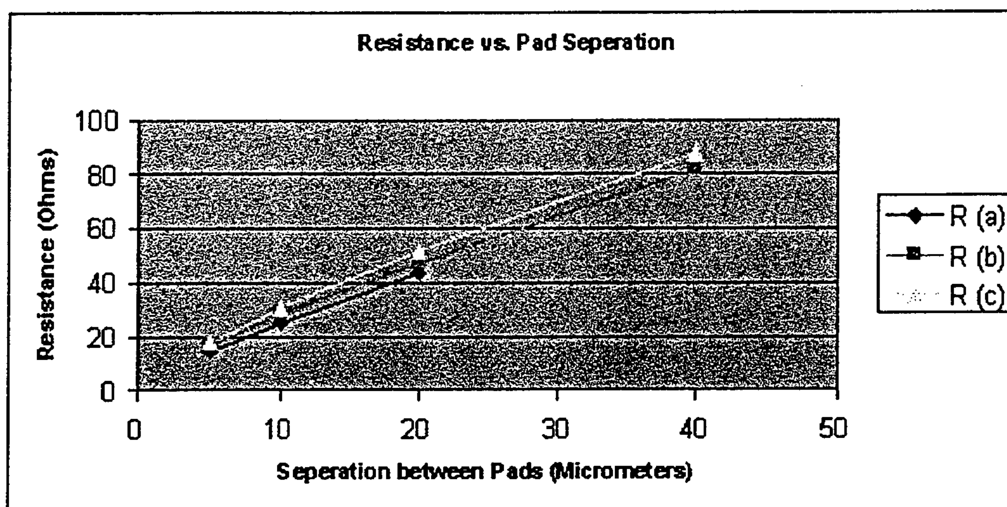


Figure 10. **Mask Set Design with Diagnostic Devices on Right.**

5. Testing Procedures

Device characteristics were obtained using a Tektronix 370A Programmable Curve Tracer along with the File Management Software. Ohmic and Shottky contacts were measured using the procedure presented in the following section.

The GaN wafer design contains diagnostic devices including ohmic resistance test structures. These structures consist of 5 aligned pads separated by distances of 5, 10, 20, and 40 microns. The pads were constructed by overlapping squares of mesa, ohmic metal, and gate metal. Ohmic measurements were taken using a four-probe procedure. Current of 1 mA was forced from one pad to an adjacent pad while measuring the voltage change across pad separation. Resistances were calculated with Ohm's Law and plotted against the respective separations (Table 2).



Distance	R (a)	R (b)	R (c)
5	14.7	16.9	17.9
10	25.1	28.9	30.8
20	43.9	47.7	51.9
40		81.9	87.8

Table 2. Resistance vs. Pad Separation.

The contact resistance, R_C, was calculated for each pair of pads (a). An average value of R_C was determined and used to find the contact resistance in units of ohm-mm (b) and ohm-cm^2 (c). Corresponding equations are given in Figure 11.

(a) $R_C = \left| \frac{R_{ij} l_{jk} - R_{jk} l_{ij}}{2 (l_{ij} - l_{jk})} \right|$ [ohm] — ij refers to distance between pad i and pad j; jk refers to distance between pad j and pad k

(b) $r_C = R_C W$ [ohm-mm] — W refers to pad width in mm

(c) $r_C = R_C(W \times L_t)$ [ohm-cm^2] — W refers to pad width in cm; L_t refers to transfer length in cm.

Figure 11. Equations Used to Determine Contact Resistances.

Pad width was determined to be 0.1mm or .01 cm. The transfer length is the lateral length in the ohmic contacts that current flow is expected to cross. This value L_t was estimated at a typical value of 3.0×10^{-5} cm. Using these values and equations, the contact resistance for the initial test wafer was found in the following forms (Figure 12).

R_C(avg.) = 4.36 ohms
r_C = 0.436 ohm-mm
$r_C = 1.3 \times 10^{-6}$ ohm-cm^2

Figure 12. Contact resistances determined on Initial devices

A characteristic Schottky curve was easily obtained through I-V measurements of a fat FET diagnostic device. The data presented in Figure 13 was taken using a Tektronix 370A Curve Tracer.

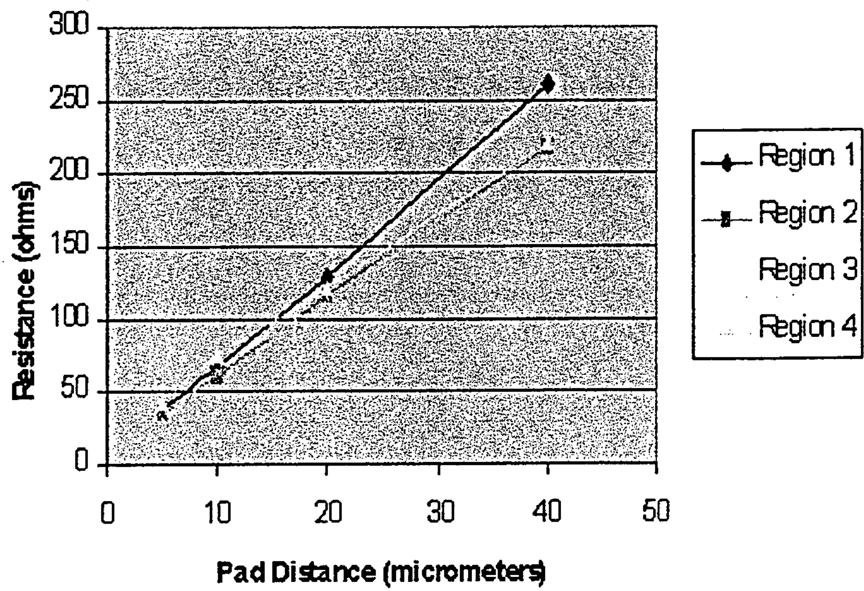
Figure 13. Shottky I-V Characteristics.

6. Results

Four wafers of doped GaN were processed. Three devices had sapphire substrates. A GaN HEMT on SiC/Si was also processed. The characteristics of the GaN MESFETs fabricated on these wafers are shown in Table 3.

Wafer Number	Substrate	Gate Width (mm)	g_m (mS/mm)	IDDS (mA/mm)	Notes
00-700-14(3)	Sapphire	0.075	84	701.3	
		0.150	130	673.3	
		0.300	126	655	
00-700-14(5)	Sapphire	0.075	69.33	318.6	
		0.150	59.33	299.3	
		0.300	55.33	310	
9-12-00 Ti/Au	Sapphire	0.0375	93.33	373.3	Used Ti/Au as gate metal instead of Ni/Au
		0.075	53.33	333.3	
		0.150	53.33	266.6	
HEMT GaN	SiC/Si	0.0375	26.6	21.3	
		0.075	33.3	20	
		0.150	33.3	36.6	

Table 3. Measured Device Characteristics.



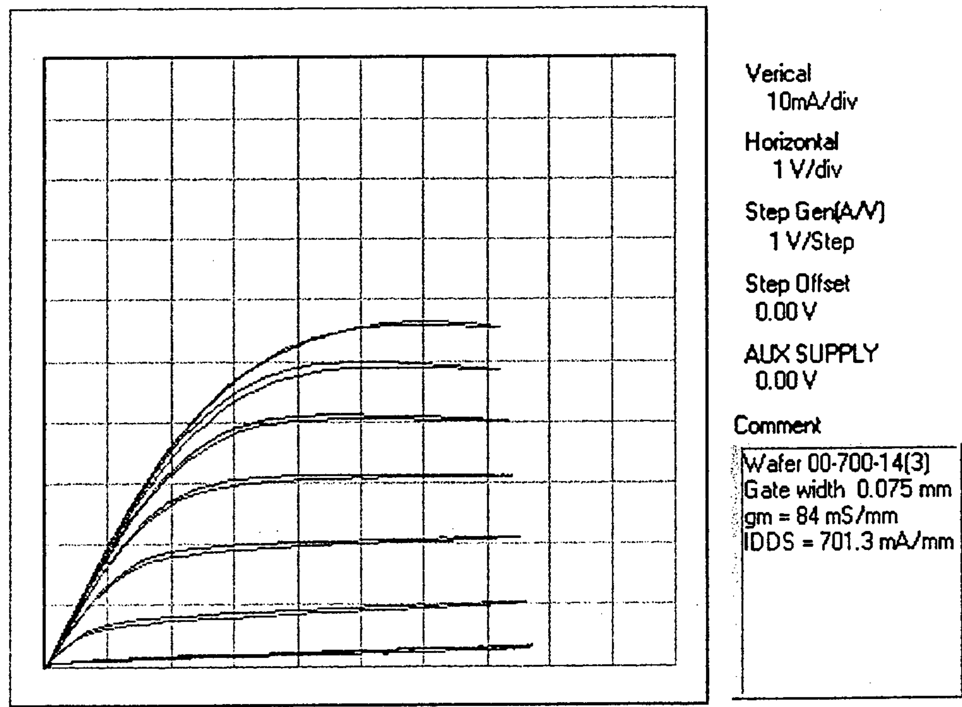
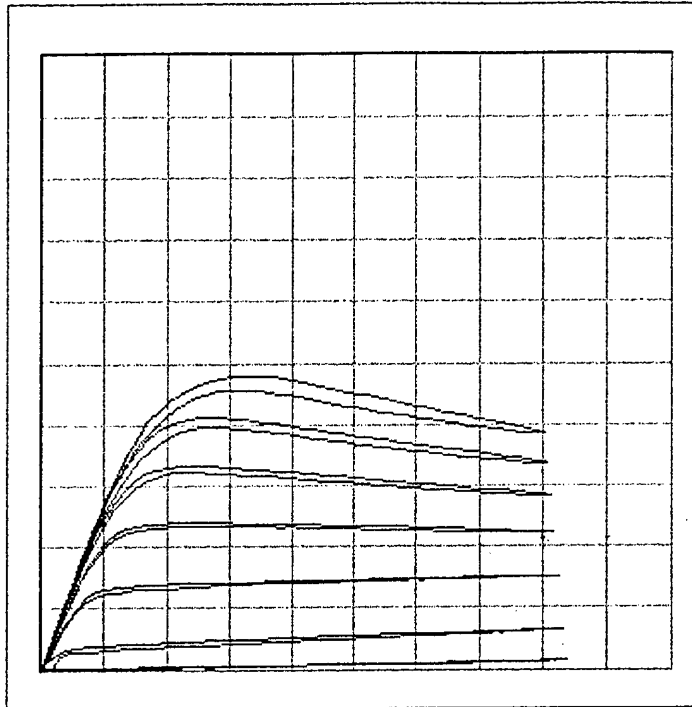
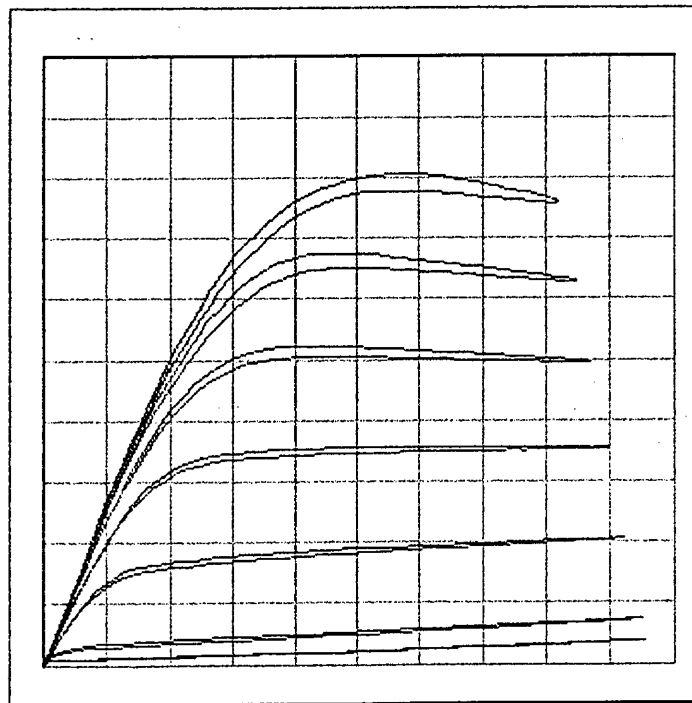


Figure 14. Wafer 00-700-14(3).

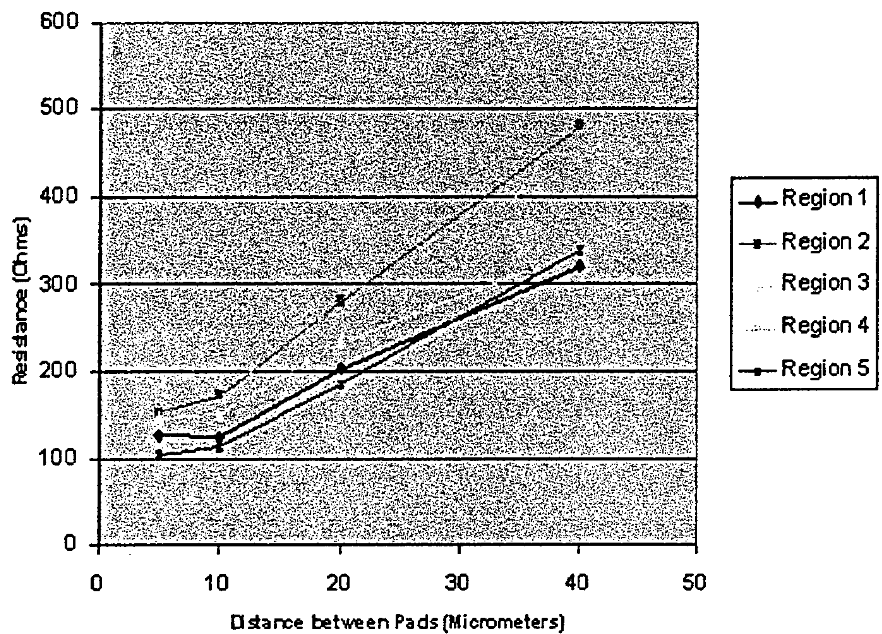


Verical
20mA/div
Horizontal
2 V/div
Step Gen(A/V)
1 V/Step
Step Offset
0.00 V
AUX SUPPLY
0.00 V
Comment
Wafer 00-700-14(3)
Gate width = 0.15 mm
gm = 130 mS/mm
IDDS = 673.3 mA/mm



Verical
20mA/div
Horizontal
1 V/div
Step Gen(A/V)
1 V/Step
Step Offset
0.00 V
AUX SUPPLY
0.00 V
Comment
Wafer 00-700-14(3)
Gate width = 0.3 mm
gm = 126 mS/mm
IDDS = 655 mA/mm

Figure 15. Wafer 00-700-14(3) Continued.



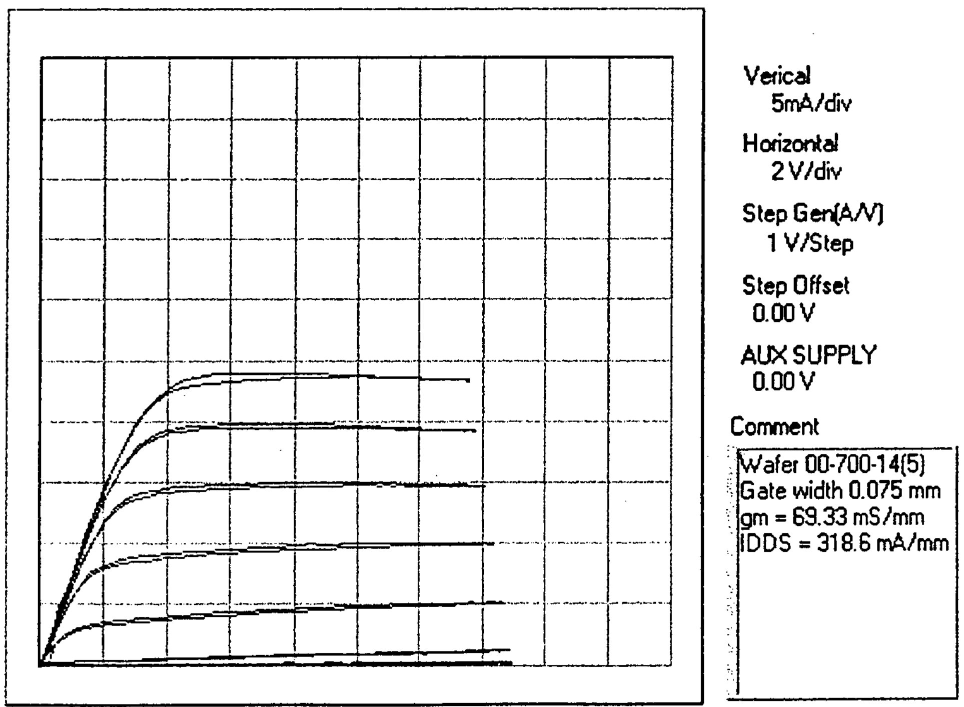
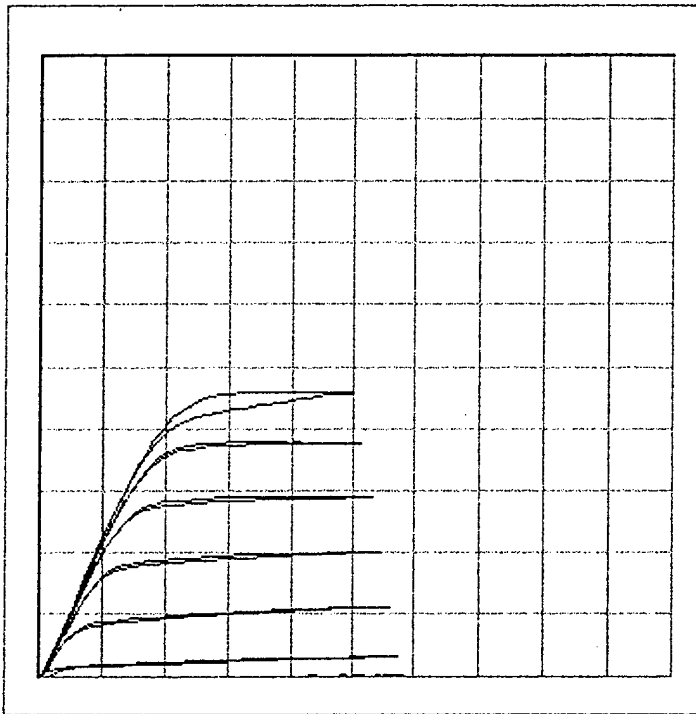
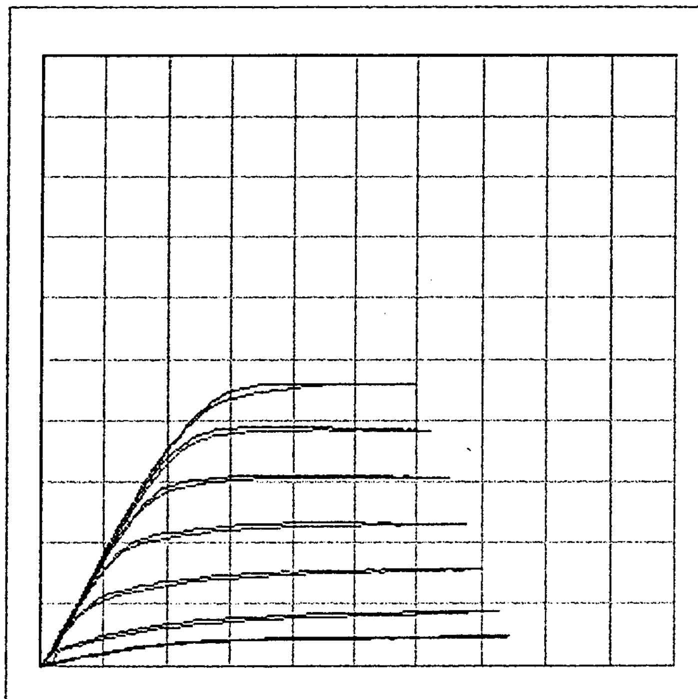


Figure 16. Wafer 00-700-14(5).

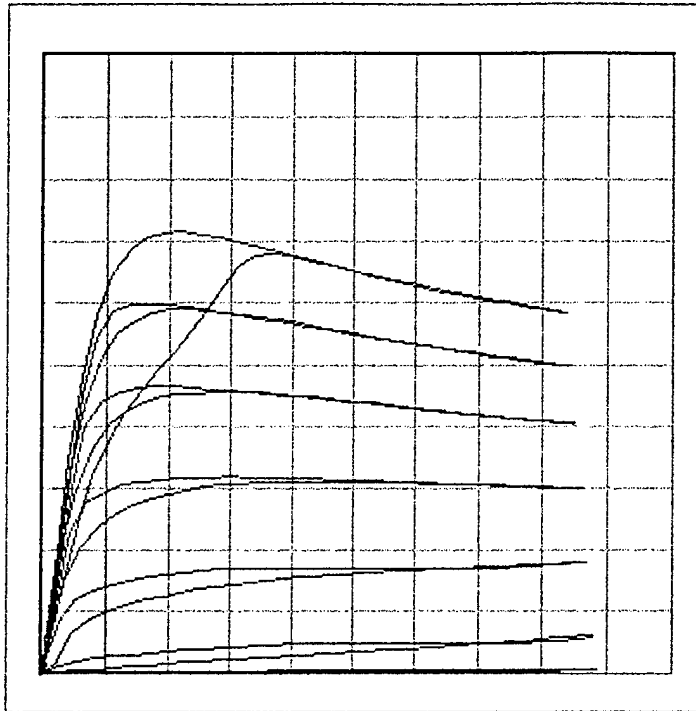


Verical
10mA/div
Horizontal
2 V/div
Step Gen(A/V)
1 V/Step
Step Offset
0.00 V
AUX SUPPLY
0.00 V
Comment
Wafer 00-700-14(5)
Gate width 0.15 mm
gm = 59.33 mS/mm
IDDS = 299.3 mA/mm



Verical
20mA/div
Horizontal
2 V/div
Step Gen(A/V)
1 V/Step
Step Offset
0.00 V
AUX SUPPLY
0.00 V
Comment
Wafer 00-700-14(5)
Gate width = 0.3 mm
gm = 55.33 mS/mm
IDDS = 310 mA/mm

Figure 17. Wafer 00-700-14(5) Continued.



Verical
2mA/div

Horizontal
5 V/div

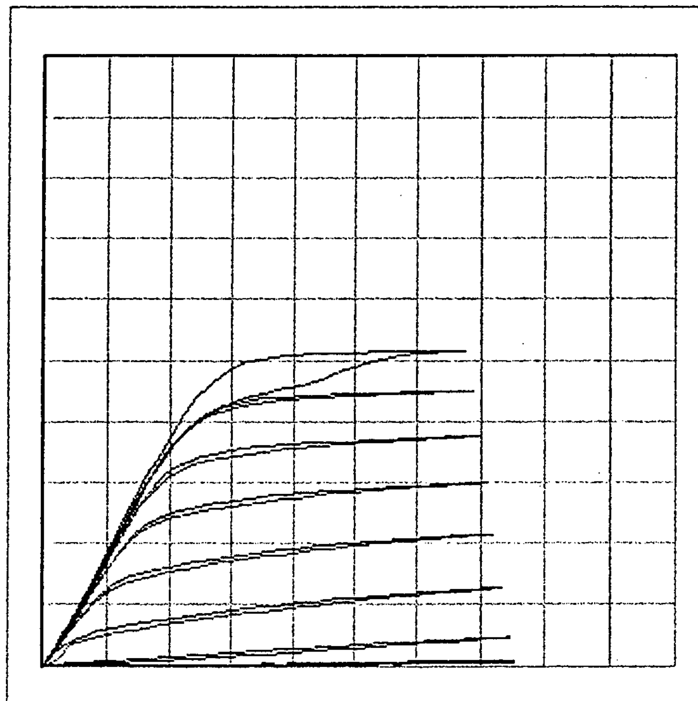
Step Gen(A/V)
1 V/Step

Step Offset
0.00 V

AUX SUPPLY
0.00 V

Comment

Wafer 9-12-00 Ti/Au
Gate width 0.0375mm
gm = 93.33 mS/mm
IDDS = 373.3 mA/mm



Verical
5mA/div

Horizontal
2 V/div

Step Gen(A/V)
1 V/Step

Step Offset
0.00 V

AUX SUPPLY
0.00 V

Comment

Wafer 9-12-00 Ti/Au
Gate width 0.075 mm
gm = 53.33 mS/mm
IDDS = 333.3 mA/mm

Figure 18. Wafer 9-12-00 with Ti/Au Gate Scheme.

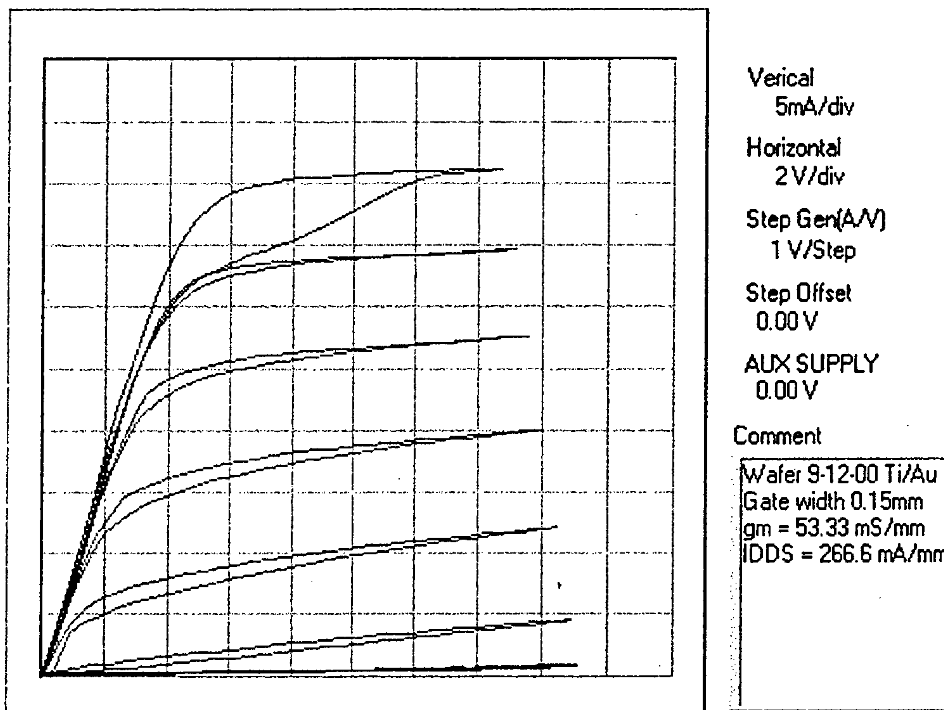
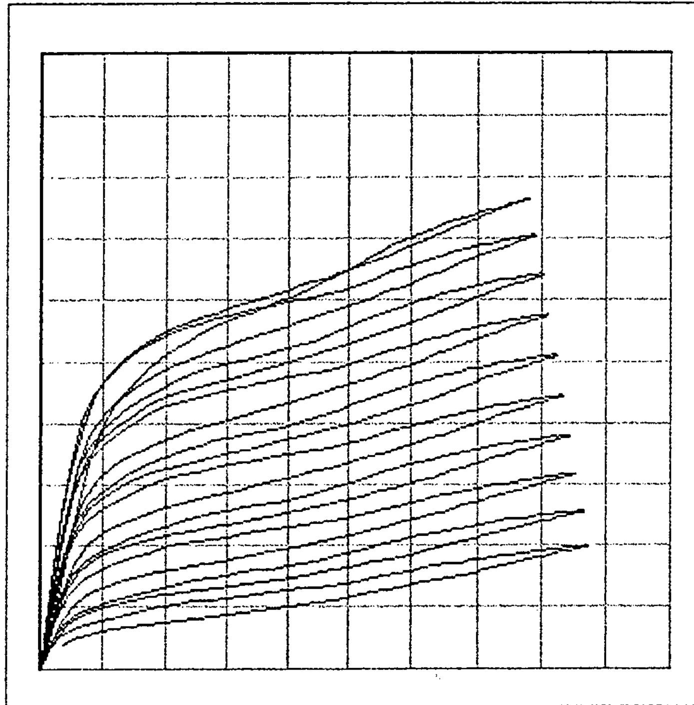


Figure 19. Wafer 9-12-00 with Ti/Au Gate Scheme Continued.



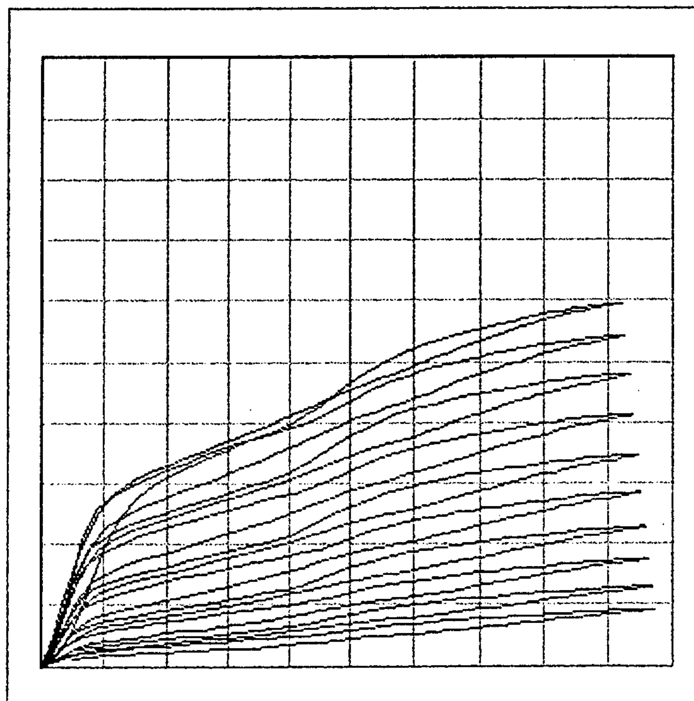


Figure 20. HEMT on Silicon.

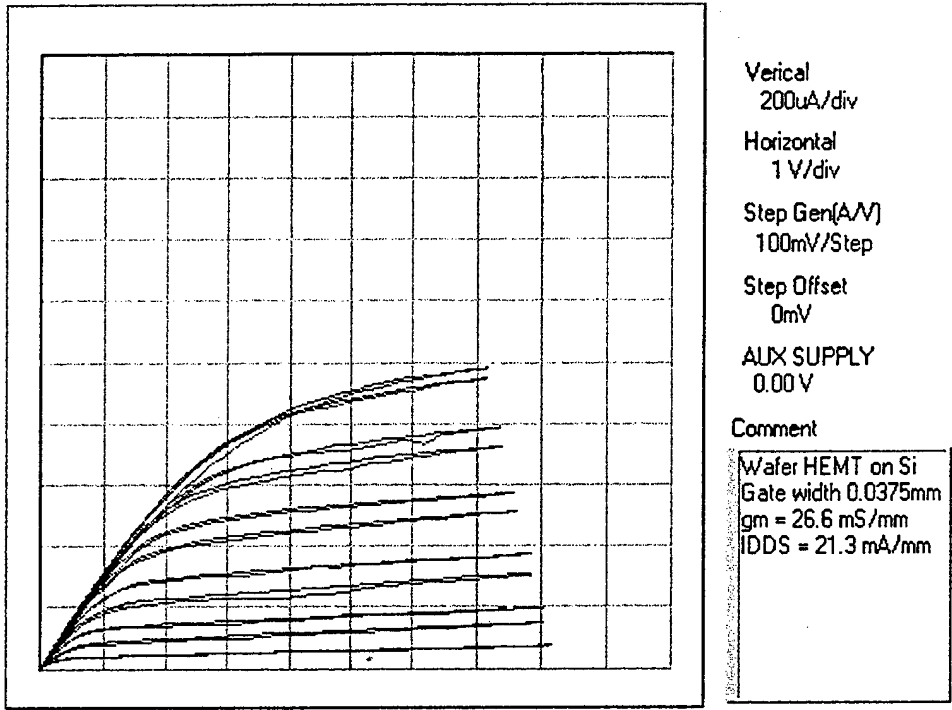


Figure 21. HEMT on Silicon Continued.

7. Substrate Effects

Substrate loss is an important design factor in monolithic circuit implementation. Because of the excellent insulating property of the GaAs substrate, there is no problem associated with the substrate losses in the GaAs-based MMICs. Our material system for GaN HEMTs involves the use of silicon substrates with SiC layer on top. The resistivity of the substrate material and any buffer layers on top affects the losses of transmission lines and passive components (i.e., "Q" of the capacitors and resistors). During the course of this program, we planned to analyze the loss characteristics of the circuits by using available 3-D electromagnetic simulators. We planned to compare these results to measurements made on actually devices using a test masks optimized for GaAs transmission lines. The test masks were designed for 100 mm wafers, which were not availbel in time to conduct this test. We expected to be able to measure the loss per unit length of transmission lines as a function of frequency. Work in this area still needs to be performed.

8. Conclusions

A new heterogeneous materials technology, that combines high performance RF gallium nitride devices and workhorse silicon MOS analog and digital devices on a low cost silicon substrate, is being developed to address limitations associated with hybrid packaging and interconnections. Work completed on this program represents an important first step toward realization of this mixed materials system. GTRI successfully fabricated and tested GaN HEMTs on silicon substrates. GTRI developed its GaN HEMT process on GaN layers that were grown on sapphire substrates. State of the art performance was demonstrated with high transconductance and saturated current approaching 1 A/mm. GaN HEMTs produced at GTRI on silicon substrates, had normal current voltage characteristics; however the transconductance and saturation current density were low. GTRI believes that this is due to the fact that the GaN epi layers were not optimized on the initial wafer runs. **These initial results validate that GaN HEMTs can be produced on low cost silicon substrates and support the position that continued funding in this area will lead to improved performance that may provide a better performance/cost ratio than GaN devices on more expensive substrates such as SiC and sapphire.**

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Nitronex Corporation
Final Technical Report

Heterogeneous Materials and Systems Integration via Selective Growth of Gallium Nitride-based RF components and Silicon Integrated Circuits

Sponsored by

Defense Advanced Research Projects Agency
Microsystems Technology Office

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Reporting Period (August 1,1999 – March 31,2001)

31 March, 2001

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1.0 Summary

The principal goal of the ongoing program is the enhancement of the functionality of silicon by expanding its field of use to include a higher frequency of operation via the integration of silicon-based IC circuits and GaN-based HFETs to produce variable gain amplifiers as the proof of concept of a electronic microsystem. This will be demonstrated by on-chip digital control of the gain of the GaN HFET device using a CMOS gate circuit.

The platform chosen for this initial integration demonstration will be a 100-mm Si(001) substrate that is fully CMOS compatible. The materials stack will be comprised of the following: AlGaN/GaN HFET device material stack, Pendeo-epitaxially grown GaN buffer, an AlN buffer, and a Si(111)/Si (100) SOI wafer with micromachined structures for thermal management.

Nitronex's primary role in this interdisciplinary collaborative research program is the materials integration of heteroepitaxially grown GaN-based epilayers (using a MOVPE deposition technique) with large-area (100mm) silicon (100) wafers. Work accomplished under the time allocated to this project included construction and commissioning of a proprietary 100mm III-Nitride MOVPE system specifically designed to address the uniformity issues required for commercial applications, development of a process route for the growth of GaN on Si(111), demonstration of growth of GaN on 50-mm and 100-mm diameter Si(111) substrates, and the first demonstration of a GaN-based High Electron Mobility Transistor on a 100-mm platform.

2.0 Large Diameter MOVPE Equipment

In developing a reactor for large-diameter epitaxial growth of the III-Nitrides, the most important parameters in obtaining uniform high quality deposition are those related to the gas injection and the uniformity of substrate heating. *These requirements are further exacerbated in the development of the PENDEO^{TM} process, as this lateral growth technique is highly dependent on uniform flow and temperature profiles.* By meeting our own internal uniformity specifications requisite of the pendeo-epitaxial growth technique, we our confident that will be able to achieve 5% uniformity in thickness, composition and doping across the 100-mm wafers.

Wafer carriers are typically heated either by radio frequency (RF) induction or by resistive heating elements. RF heating has the advantage of minimizing the contact between the heating mechanism and process gases. However, uniform heating of large areas by induction is difficult and inefficient. Nitronex's MOVPE system is a vertical reactor with resistive heating capable of deposition on three 50-mm wafers (3 x 2") or a single 100-mm wafer (1 x 4"). The design of this reactor will provide a platform for testing improvements in reactor design that will lead to a reactor for multiple 100-mm wafers (i.e. 3 x 4"). A technical description of Nitronex's vertical reactor design is outlined in the following paragraphs.

2.0.1 *MOVPE System Overview*

The Nitronex 100-mm System (Figure 1) consists of a gas delivery cabinet, reactor chamber cabinet and electronics cabinet. The gas delivery cabinet houses state-of-the-art

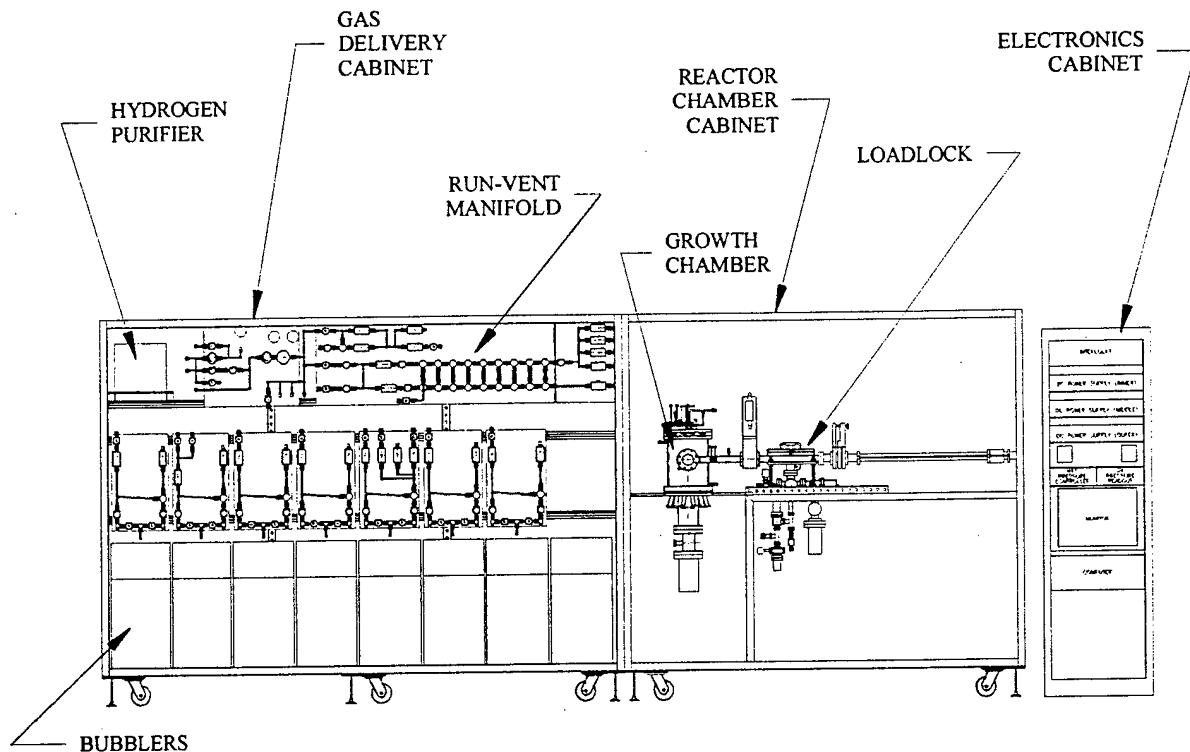

Figure 1. Nitronex MOCVD System Schematic.

purifiers (hydrogen, nitrogen and ammonia), the run-vent manifold and seven alkyl bubblers. The reduced deep volume run-vent manifold is located near to the reactor chamber to minimize the gas line length to the reactor chamber. This design reduces sweep time and contributes to sharper interfaces for multi-layer depositions, especially multiple quantum well structures. The reaction chamber cabinet contains the growth chamber, process pump and load lock. The growth chamber is water-cooled and contains a heated substrate mount (1200°C) with three independently controlled zones, as well as a 1500-rpm substrate rotation capability. The growth chamber is connected to the load lock by a rectangular gate valve. The substrate carrier is transferred between the growth chamber and load lock by a magnetically coupled linear transfer device. The electronics cabinet houses the power supplies, system interlocks and computer control system. The components in all three cabinets have been arranged to allow for ease of maintenance and modification. The most unique aspects involve the multi-zone systems for gas injection and substrate heating.

2.0.2 *Gas Injection*

Having control of the radial concentration of the injected gases is key to obtaining uniform large area deposition. The radial concentration can be controlled by adjusting the geometry of the injection nozzle. However, since multiple injection nozzle geometries must be tried, the fabrication and testing necessary to find the optimum configuration would be time

consuming and expensive. Furthermore, the optimum geometry may be different for different operating temperatures, flows and pressures. We have chosen to use a proprietary design comprised of multiple concentric injection zones (metal-organic alternating with ammonia) with input for each zone controlled by a separate mass flow controller. Such an arrangement allows for precise control of the radial concentration of the process gases during film growth. The use of a curtain gas helps to minimize wall deposition while maintaining uniform flow across the chamber. In addition, the use of the metal-organics and ammonia is more efficient since they are input only across the diameter of the wafer carrier.

2.0.3 *In-Situ Capabilities*

The proprietary gas injector is designed with two optic ports for *in-situ* film deposition analysis. These ports are designed at an incident angle normal to the growth surface to facilitate using interferometry for film thickness measurements and using optical fiber infrared thermometry for substrate temperature measurements.

The commercially available interferometry monitoring system uses spectral reflectance to measure deposition rates, layer thickness, optical constants and uniformity. An integrated silicon photodiode allows for continuous *in-situ* monitoring even at elevated rotation speeds (i.e. 1500 rpm) in either the 1 x 4" or 3 x 2" system configurations. This *in-situ* monitoring tool coupled with our computer control system, described below, will allow for real-time analysis of the growth process.

2.0.4 *Multi-Zone Substrate Heater*

The Nitronex reactor uses a multi-zone resistance heater to insure temperature uniformity across the wafer carrier. With a single zone heater, lower temperatures usually occur near the edge and center support of the wafer carrier. The lower temperatures at the edge are due to the increased gas flow in this region as well as heat loss to the water-cooled reactor wall. Additionally, the center support for the wafer carrier can act as a heat sink leading to reduced temperatures at the center of the carrier. We reduce the heat loss through the center support using a proprietary design to minimize the cross section of the support.

Tungsten and graphite are materials that are commonly used for resistive heating elements. However, both of these materials degrade and become embrittled when exposed to the process gases used in the deposition of GaN. The Nitronex system uses elements made of rhenium, a high temperature refractory metal well suited for use in hydrogen and ammonia environments.

2.0.5 *Computer Control*

The Nitronex 100-mm MOCVD system is fully computer controlled and automated. The in-house designed control software is robust and user-friendly. It can be run in manual mode, automatic (recipe) mode or recipe control with manual override. Recipe control is a must for repeatable process control. Additionally, process and system parameters are stored in a database to facilitate detailed analysis of the process. The backplane of the computer-controlled system is oversized to allow for the implementation of additional mass flow controllers and pneumatically actuated valves should subsequent system modification become necessary.

The optical fiber infrared pyrometer and multi-zone substrate heater power supplies are close-loop controlled. Additional thermocouples are used in balancing the power requirements between the heating zones to insure temperature uniformity across the wafer carrier. With the closed-loop temperature control, in-situ film monitoring system and data acquisition capabilities, Nitronex has the ability to provide real-time process control for nitride growth.

3.0 GaN growth on 50-mm Si(111)

Nitronex has demonstrated the basic steps necessary for single-crystal deposition of 2H-GaN on Si(111). This has been achieved by incorporating the use of a transition layer comprised of a thin 3C-SiC carbonization layer and an aluminum nitride (AlN) buffer layer. Figure 2 is a Scanning Electron Microscopy (SEM) image, performed at NCSU, showing the cross-section of a typical GaN/AlN/3C(SiC(111)/Si(111) materials stack.

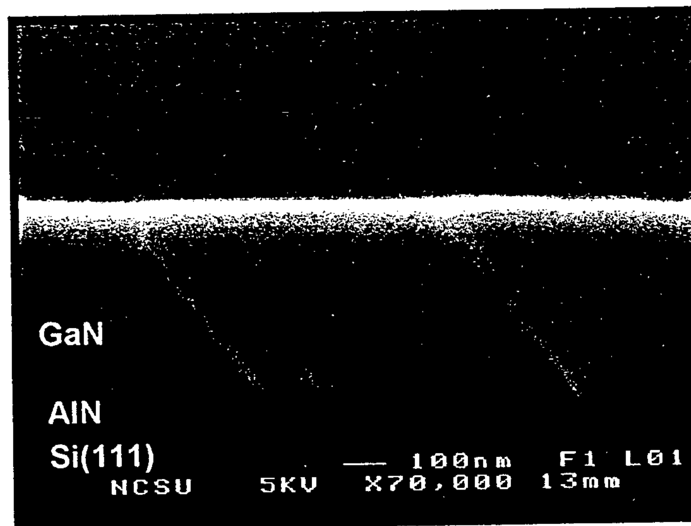

Figure 2. Cross-sectional SEM of GaN/AlN/Si(111) material stack.

Over the last few months, the Nitronex team has continued to refine and optimize the formation of the transition structure. By doing so, we have been able to improve the quality of our GaN epilayers. This is evident by the improvement of our initial GaN layers grown on the AlN/3C-SiC/Si(111) exhibiting typical XRD FWHM values of ~ 1000 arcseconds. Our most recent GaN layers now exhibit typical XRD FWHM values of ~500 arcseconds, indicative of an improved crystal structure. Recent low-temperature (14 K) photoluminescence spectra of these films are comparable to similar GaN layers grown on 6H-SiC as shown in Figure 3.

Nitronex is aggressive pursuing further refinements in the transition layer scheme to further improve the quality of our GaN epilayers and reduce the cracking resulting from the mismatch in coefficients of thermal expansion.

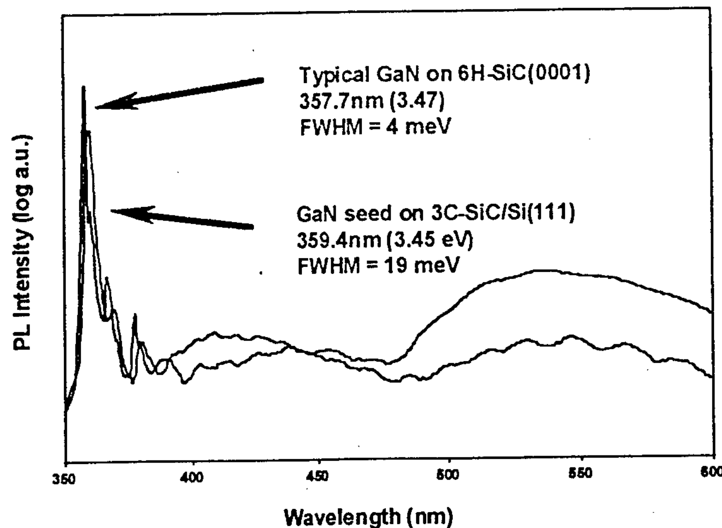

Figure 3. Low-temperature PL spectra of 1μm thick GaN(0001) films grown on AlN/6H-SiC(0001) and AlN/3C-SiC/Si(111).

The GaN epilayer thickness uniformity has been characterized using a Filmetrics F50 spectrometer thin-film mapping system. The variations across the 50-mm samples were measured to be 17.1%, as shown below in Figure 4.

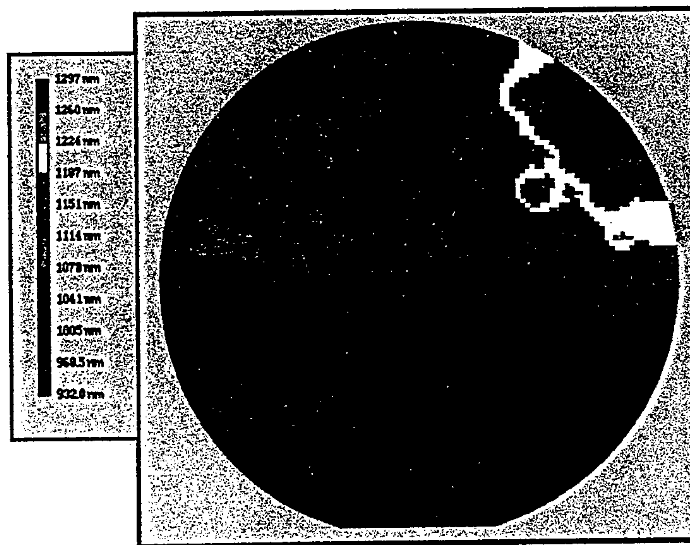

Figure 4. Thickness uniformity of a typical GaN epilayer on 50-mm Si(111).

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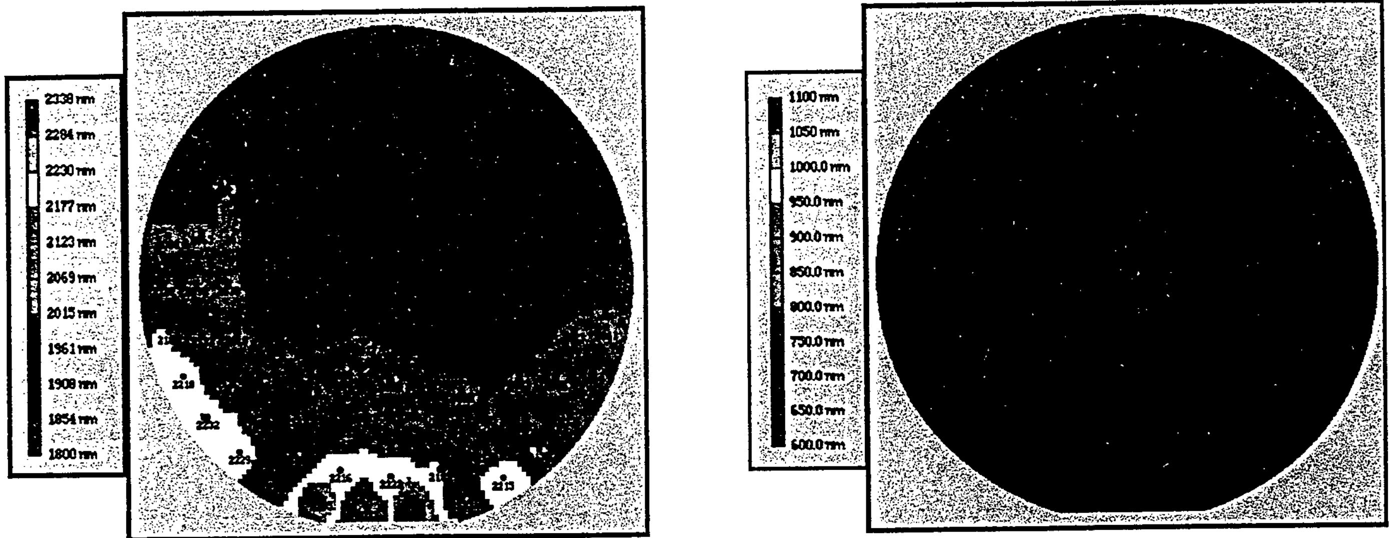
4.0 Scale-up to 100-mm Si(111)

Nitronex, using the facilities at the NCSU Davis Research Labs, achieved initial growth of GaN on 100-mm Si(111) in the Spring of 2000. This process was successfully transferred in-house to Nitronex in July 2000 with improved thickness uniformity across the 100-mm wafers, as shown in Figure 5.



a) NCSU prototype III-Nitride MOVPE
Uniformity ±30.7%

b) Nitronex Custom III-Nitride MOVPE
Uniformity ±10.3%

Figure 5. Thickness uniformity of initial GaN epilayers grown on 100-mm Si(111).

We have also performed Atomic Force Microscopy (AFM) on several of our AlGaN/GaN on silicon HFET structures. Figure 6 shows a typical HFET surface topography of a 25 μm^2 area. The step edge structure of the surface is clearly observed in this phase contrast image. The surface RMS roughness for our GaN-based layers on silicon is on the order of 2-8Å for our optimal stacks. This surface roughness is significantly smoother than values typically reported for GaN grown on sapphire and SiC substrates. We believe that this result is attributed to the use of silicon as the substrate.

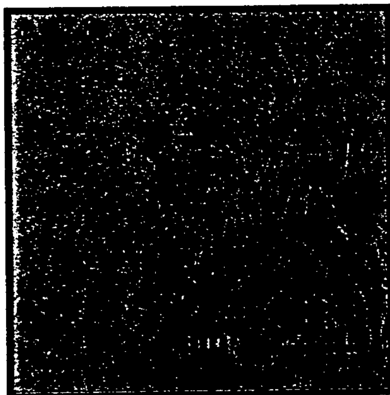


Figure 6. Atomic Force Microscopy of AlGaN/GaN on Silicon material Stack.

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Of the three commonly used platforms upon which the III-Nitride community uses for GaN-based crystal growth (namely, silicon, SiC and sapphire), silicon, by far, has the highest degree of bulk and surface crystallographic perfection. Advantageously, the crystal perfection of the silicon surface is translated into the GaN epitaxial films. Additionally, this leads to the ability to grow materials stacks exhibiting sharper interfaces between any two layers. Since the 2DEG resides 25-50Å below the AlGaN/GaN interface (in the GaN layer), this phenomenon should result in the deposition of HFETs with higher 2DEG mobilities, and partially explains Nitronex's ability to quickly make significant improvements in AlGaN/GaN HEMT structures characterized with mobilities over 1500 cm^2/V s, as reported below.

5.0 2DEG Structures

Several undoped $Al_xGa_{1-x}N$/GaN 2DEG test structures were grown. On-wafer room temperature Hall mobilities from our standard 280Å thick $Al_{0.33}Ga_{0.67}N$ / 1 micron thick GaN HEMT test structures typically exhibit values of >1500 cm^2/V s at ~8.5E12 cm^{-2} sheet electron densities. These typical mobility values are the highest reported for GaN on silicon. We are now in the process of developing silicon-doped material stacks to be incorporated into our current MODFET development. The MODFET structure offers additional degrees of freedom in the overall HFET design over the simpler HEMT. In the HEMT, the sheet carrier density in the 2DEG channel is predominately controlled by the aluminum content in the AlGaN. Typical sheet carrier densities in the range of 0.7–0.9E13cm^{-2} can be achieved by adjusting the Al content from 10 to 40%. However, when the higher Al content HEMT is employed, stringent requirements on the overall thickness of the AlGaN must be adhered to in order to avoid cracking of the epi as well as the occurrence of aging (long term relaxation) in the structure. The addition of the Si-doped donor layer to the structure to form the MODFET allows for more precise control of the sheet carrier density while being able to work in a more reasonable Al content regime. With a Si-doped donor layer, the sheet carrier density can be controlled in the range of 0.7-2.0E13cm^{-2}. This offers increased flexibility in the overall device design. Coupling the advantages of the MODFET structure with the GaN-on-Si process developed at Nitronex, we have achieved mobilities in excess of 1320cm^2/Vs with a sheet carrier density of 1.0E13cm^{-2}.

6.0 Initial Device Fabrication

Nitronex completed commissioning a pilot line clean-room in November 2000. This facility is fully equipped for 100-mm GaN processing. Using this facility, we recently achieved the first demonstration of a GaN-based HEMT on a 100-mm GaN-on-Silicon wafer. Figure 7 shows a typical 100-mm wafer GaN on silicon wafer with the initial HEMT test structures and Figure 8 is a SEM image of one of these devices.

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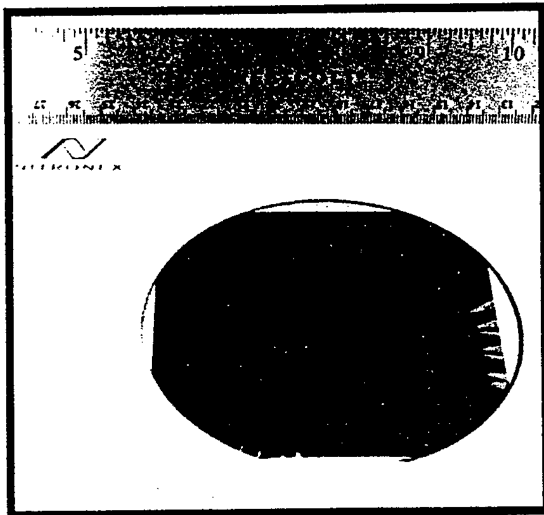

Figure 7. GaN HEMTs of 100-mm Si

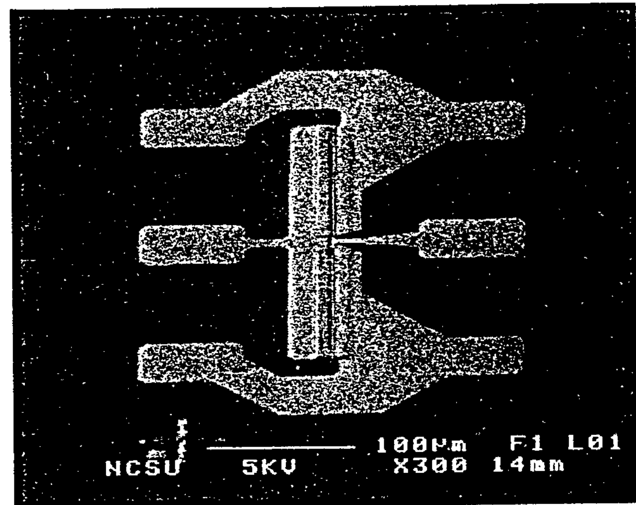

Figure 8. SEM image of HEMT structure

Figure 9 shows the DC characteristics from these initial devices. The gate voltage increments shown in Figure 9 were 0.5 V per division. These transistors show promising characteristics with complete pinch-off and a transconductance of 100 mS/mm with a saturated drain current of 160mA/mm. The on resistance is 10 mW/mm. When devices are fabricated on our more recent MODFET structures on 100mm substrates with mobilities over $1300 cm^2/(v\ s)$ and a channel charge of 1×10^{13} cm^{-2} we expect a dramatic improvement in the I_{Dsat} of these devices. RF power measurements for these devices are forthcoming, as are various improvements to process technologies such as recess etched gates, improved ohmic contact schemes and sub-micron gate technologies.

First GaN HEMT on 4" Si substrate

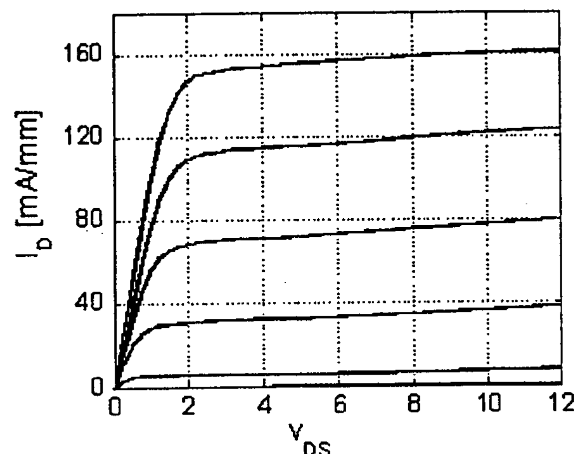

Figure 9. DC-characteristics of initial HEMT structures

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7. Conclusion

Since Nitronex is solely focused on GaN for RF-applications, having achieved the requisite materials requirements, we are now shifting emphasis towards transistor design and fabrication. As such, we are continuing our studies aimed at optimizing the growth of AlGaN thin films, as well as n-type (Si) doped layers of GaN.

Having developed a process route achieving the ability to grow 2-3 micron thick GaN-based epilayers on large-area silicon substrates, Nitronex is now turning its focus from materials development towards device fabrication. During the final months of this effort, Nitronex completed commissioning a pilot line clean-room fully equipped for 100-mm GaN processing and achieved the first demonstration of a GaN-based HEMT on a 100-mm GaN-on-Silicon wafer. These initial transistors show promising characteristics with complete pinch-off and a transconductance of 100 mS/mm with a saturated drain current of 160mA/mm. The on resistance is 10 mW/mm. When devices are fabricated on our more recent MODFET structures on 100mm substrates with mobilities over $1300 cm^2/(v\ s)$ and a channel charge of $1 \times 10^{13}\ cm^{-2}$ we expect a dramatic improvement in the I_{Dsat} of these devices. RF power measurements for these devices are forthcoming, as are various improvements to process technologies such as recess etched gates, improved ohmic contact schemes and sub-micron gate technologies, airbridge fabrication, passivation, and backside processing for thermal design considerations.

Additionally, we have begun the design work on the construction of a multi-large area (3 x 4-inch) MOVPE system for III-Nitride growth. **Once commissioned (scheduled for November of 2001) Nitronex will be capable of GaN-based materials growth on 6"-8" platforms.**

Although Nitronex's immediate commercial interest for GaN-based HEMT devices are focused on providing solutions for the 2.5 and 3G base station applications, we believe the technology developed under this program can provide viable solutions and significant improvements for the requisite output power, linearity, low-noise performance and reliability of the military's future high frequency-high power devices, T/R MMICs and sub-systems, especially when considering the added benefits of growing on a technically mature semiconductor platform available in a large-area, high-quality, readily-obtainable low-cost substrate that silicon offers.

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