Insertion of Diamond into the F-22 EW Array for Improved Thermal Management, Reduced Weight and Increased Reliability

Final Technical Report

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1.0 Summary

Sanders' role on this program was to produce an electronic assembly that would demonstrate the performance benefits gained by incorporating diamond materials into critical electronics assemblies. The power regulator hybrid for the F-22 EW Array electronics was identified as an ideal candidate. The power regulator hybrid provides regulation and distribution of seven discrete voltages to supply RF and analog electronics for the EW array. Power dissipation is over 60 Watts for this assembly, making thermal management a major priority of the design. By inserting diamond substrates, silicon device junction temperatures could in principle be significantly reduced, improving overall reliability of the assembly.

Originally, the diamond based power regulator assembly was planned for insertion into production F-22 assemblies, provided cost and performance targets were met. However, processing issues delayed the availability of suitable diamond substrates during development, and this resulted in delays in completing the demonstration hardware. Ultimately, diamond was therefore not selected as the baseline substrate for the F-22 production design due to timing issues.

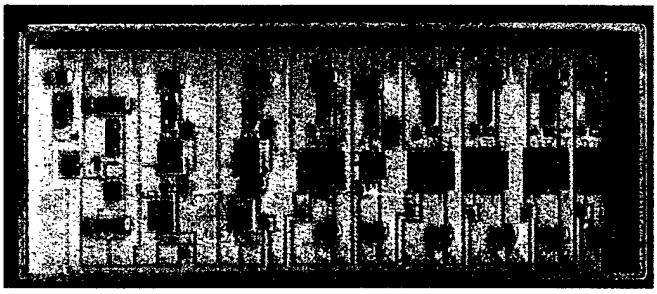


Figure 1 - Photograph of Bonded Copper-Based Power Regulator Baseline Hybrid for F-22 EW Array Electronics

Sanders continues to evaluate cost reduction opportunities on F-22. It is possible that substitution of a diamond-based design for the current baseline power regulator hybrid will be revisited as part of the ongoing evaluation. The major factors that will ultimately determine whether the diamond solution can be implemented include cost of substrates, availability (i.e. the number of suppliers), and performance benefits.

The major accomplishments of this program include:

- Complete redesign of the Power Regulator subassembly for the EW electronics array. This includes the redesign of the Hybrid packages to incorporate diamond substrates.
- Diamond-specific package assembly process techniques including development of ring frame and lead frame brazing to diamond substrates, silicon die attach to diamond and non-hermetic encapsulation.
- Thermal and mechanical stress analyses were completed on hybrid packages.

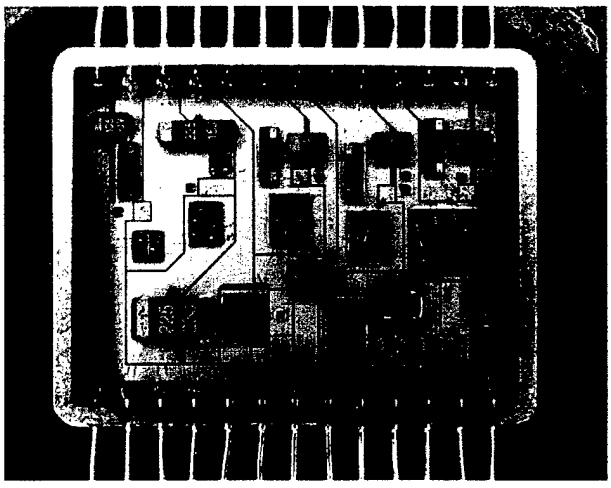


Figure 2. Photograph of New Diamond-Based Hybrid One (HY1) Power Regulator

- Assembly and electrical test of diamond-based hybrids.
- Thermal scan and imaging measurements of diamond-based hybrids.
- Environmental testing including temperature cycling and Y1 acceleration of functional electronics.

This report will show that diamond-based packages have been found to provide significant thermal advantages over more conventional packages types for F-22 Power regulator electronics. Package assembly and component integration require no unusual or expensive techniques. Electrical performance requirements were easily met. Environmental screening revealed no problems during stringent temperature cycling and Y1 acceleration The major remaining challenge is to establish reliable sources of diamond substrates for costs that are similar to BeO, Aluminum Nitride or other competing technologies.

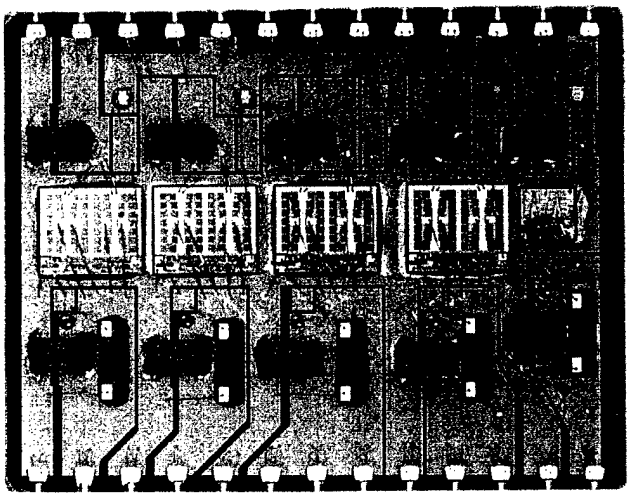


Figure 3. Hybrid Two (HY2) Power Regulator Hybrid

2.0 Program Objectives

All established objectives for this program as outlined in the SOW have been met. In two cases these objectives were modified slightly. The original plan was to assemble the *entire* power regulator*sub-assembly* as the demonstration electronics. Instead, only the hybrids were assembled and tested.

Sanders' effort on this program addressed the following specific objectives:

1. **Design new power regulator sub-assembly for adapting diamond based hybrids**
2. **Develop processes to attach lead and ring frames to diamond substrates**
3. **Develop process for silicon die attach to diamond**
4. **Perform mechanical integrity and thermal analyses to support development of the new design**
5. **Assemble hybrid packages**
6. **Perform electrical and thermal analyses**

3.0 Redesign of Power Regulator Sub-Assembly

3.1 Power Regulator Sub-Assembly

The power regulator sub-assembly was designed prior to this effort as the F-22 Baseline. This nine-channel regulator supplies discrete voltages to RF and analog electronics for the EW array LRU. The basic elements include the Hybrid package (Fig. 1) containing the active electronics, the connectorized printed wiring board (PWB) to route the I/O signals, the thermal core and cold plate required for thermal management. A photograph of the assembly is shown in Fig. 4.

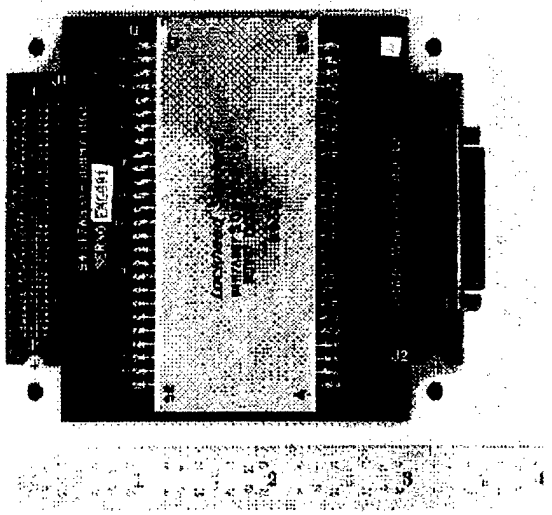


Figure 4. Baseline F-22 Connectorized Power Regulator Sub-Assembly

The Hybrid package includes a Beryllium substrate laminated with a direct bond copper layer. It incorporates an invar ring frame containing the glass-to-metal seals which provide I/O connections to the electronics. The frame is soldered directly to the BeO substrate. The metal lid completes the package by forming a hermetic seal.

The hybrid is attached directly to a BeBeO thermal core using a low impedance epoxy. The core is subsequently attached to the cold plate in a similar fashion. The profile of the baseline construct is shown in Fig. 5.

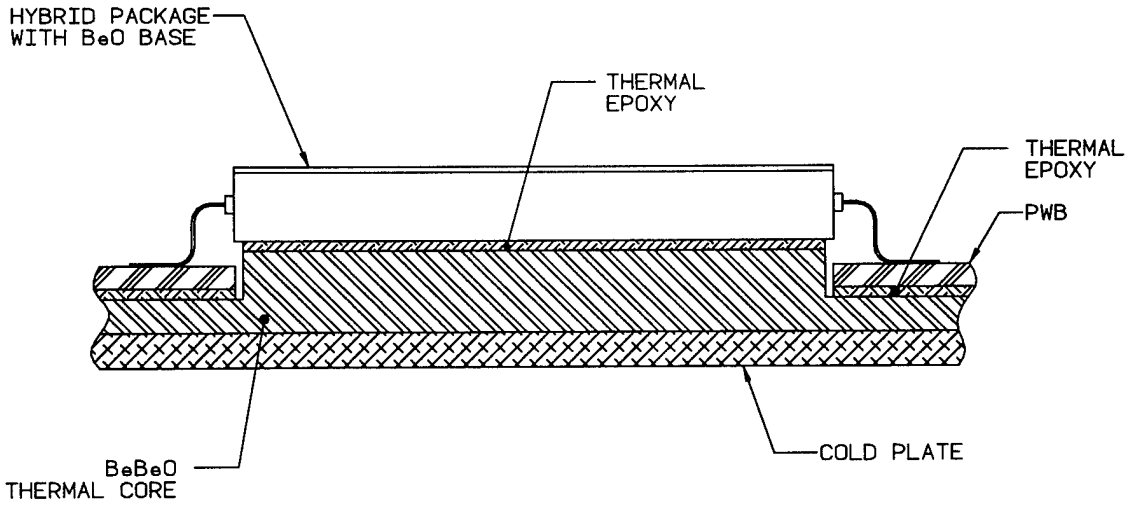


Figure 5. Profile Sketch of F-22 Power Regulator Sub-Assembly

The total power dissipation of the regulator circuits is considerable. When all regulators are operating simultaneously and continuously, worst case dissipation exceeds 68 Watts. Table 1 shows total power dissipation for individual silicon IC voltage regulators.

Thermal analysis shows that silicon die temperatures in this construct are operating with minimal design margin after derating. A modified packaging solution which offers a means to reduce die temperatures (such as utilizing diamond substrates) would have a significant positive impact on the lifetime of the assembly.

Table 1. Power Dissipation

Part No.	Power Dissipation (W)
VR1	7.553
VR2	5.742
VR3	5.018
VR4	5.265
VR8	10.296
VR5	11.670
VR6	0.839
VR7	7.624
VR9	10.699
VR10	3.992
Total Power (W)	68.698

3.2 Diamond-Based Sub-Assembly Redesign of F-22 Baseline to Incorporate Diamond

A major objective of the redesign was to develop a solution that would provide improved thermal performance compared to the baseline while reducing cost for the overall sub-assembly. Several cost-based decisions are evident when examining the sub-assembly layout.

- The electronic circuits were divided into two separate packages: Hybrid 1(HY1) and Hybrid 2 (HY2) shown in Figs. 2 and 3, respectively. This was done to reduce the physical size of the diamond substrates. The concern was maintaining adequate quality over a large area. Achieving the required substrate flatness even over these aspect ratios became a major cause for schedule delays during the program--this is described further in the substrate fabrication description.

- The expensive BeBeO core has been eliminated. The diamond packages are mounted directly to the printed wiring boards (PWB) containing an array of solid-filled thermal vias. These vias provide the low thermal impedance path to the cold plate. Although not as efficient as the BeBeO core, the PWB/thermal via design provides an adequate connection because the diamond substrate provides better lateral spreading of the heat generated by the hybrid. This increases the effective area over which the heat is conducted. Layouts of the redesigned sub-assembly are shown in Figs. 6 and 7.

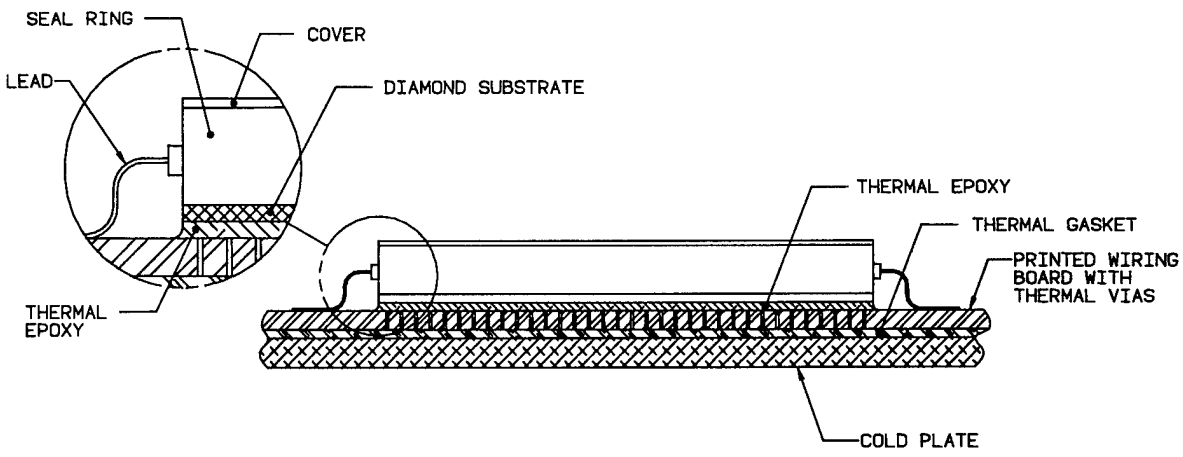


Figure 6. Profile View of Redesign Power Regulator Sub-Assembly

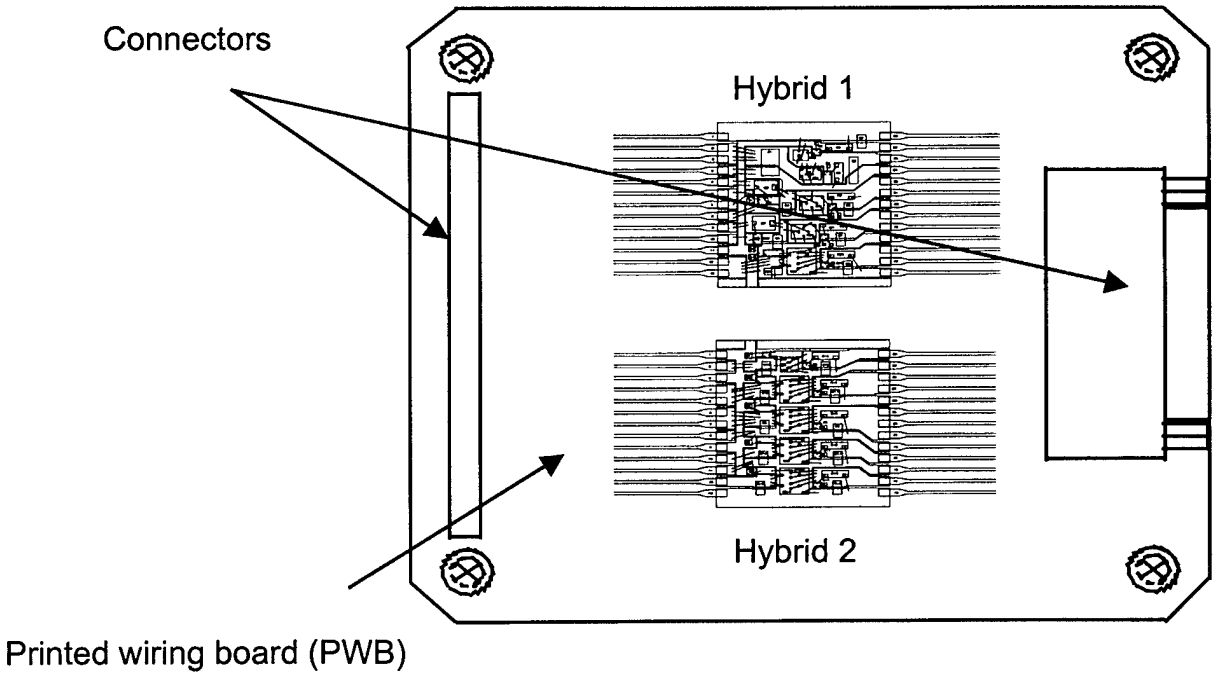


Figure 7. Top view of Redesigned Power Regulator Sub-Assembly

3.3. Preliminary Thermal Analysis

A preliminary thermal analysis was performed to compare maximum transistor junction temperatures on the silicon die for the baseline F-22 module and the diamond-based design.

3.3.1 Analysis of Baseline Design

The current design consists of ten voltage regulators soldered to the BeO substrate using 96% Sn – 4% Ag solder. The BeO substrate is metallized with 0.005" of Direct Bond Copper and bonded to a BeO base package using H-35 epoxy. The package is mounted to a BeBeO thermal core using 740169 epoxy. The assembly is finally dry-mounted to a cold-plate. Figures 8 and 9 show the top and cross section views of the model.

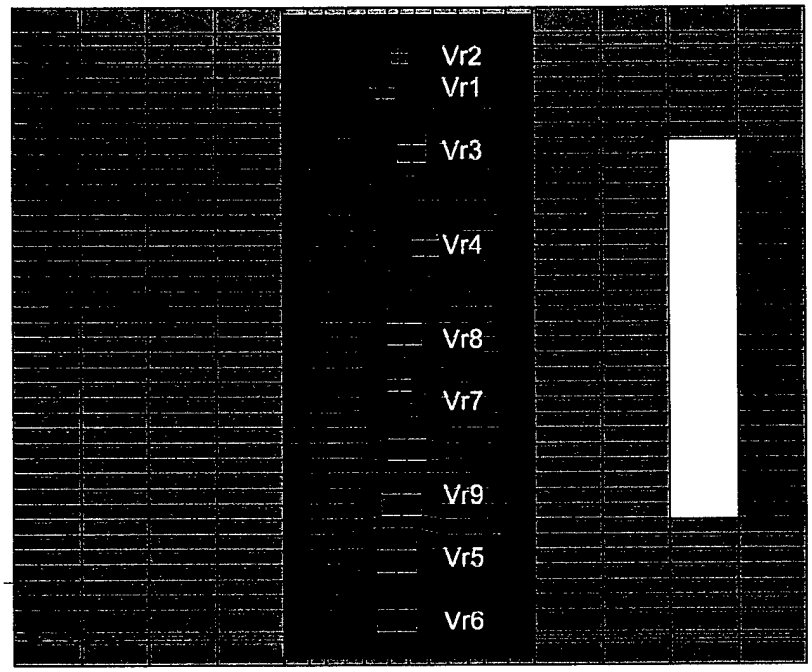


Figure 8. Thermal Analysis Model – Top View

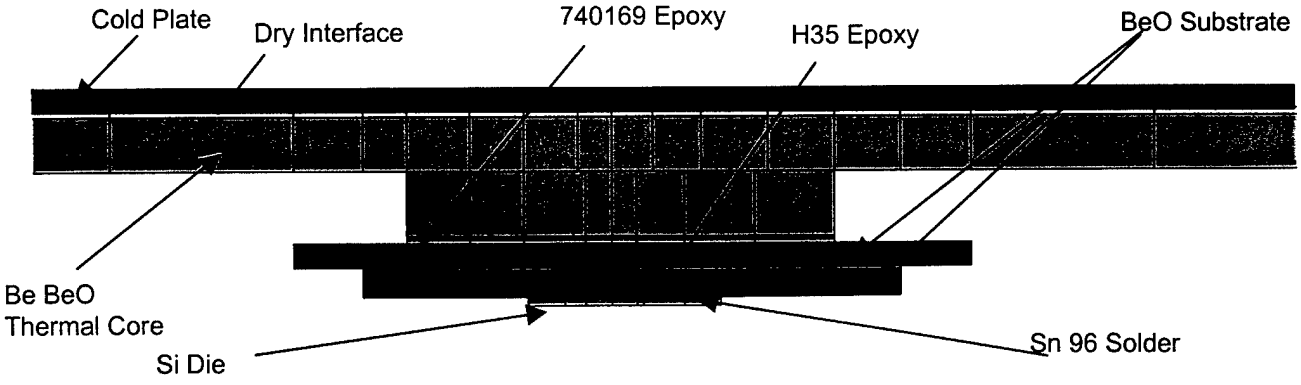


Figure 9. Thermal Analysis Model – Side View

The power dissipation estimates are worst-case values and are listed in Table I. Coefficients of thermal conductivity of the materials are from well-known tables or manufacturers' specifications. These are compiled below in Table 2.

Table 2. Material Properties

Material	Thickness (in)	Thermal Cond. (W/in-°C)
BeBeO	0.04	5.8
BeO	0.195	6.9
H35 epoxy	0.005	0.04
Si Die	0.013	3.7
740169	0.01	0.013
Sn96	0.001	1.99
Copper	0.005	9.93
Dry Mount	-	0.5 W/in^2-°C

The method of analysis was finite element evaluation of the construct. Commercially available software, Thermal Analysis System (TAS), was used to generate the model and predict worst-case temperatures. In order to obtain accurate results for absolute temperature, mesh sizes need to approach the size of the smallest features in the semiconductors where the heat is generated. However, this technique results in lengthy analysis time. Because only a relative comparison of the baseline and diamond-based constructs was required, a mesh was selected to satisfy a compromise between the absolute accuracy and analysis time. The following assumptions and conditions apply to the thermal analysis performed:

- Environment temperature: 70 ° C
- The interface resistance between the thermal core and cold-plate is 0.5 W/in^2 ° C based on a dry mount.
- Conduction is the only mode of heat transfer used in the analysis.
- All regulator circuits are biased simultaneously and operating in a continuous mode.

3.3.2 Results of Baseline Analysis

Table 3 shows the predicted temperatures for all the voltage regulators. The average temperatures on the silicon die surfaces range from 124-136 deg C. The contour plots are shown in Figure 10. Temperatures are consistent with expected power dissipation densities. The legend at the right of the contour map provides the temperature by color.

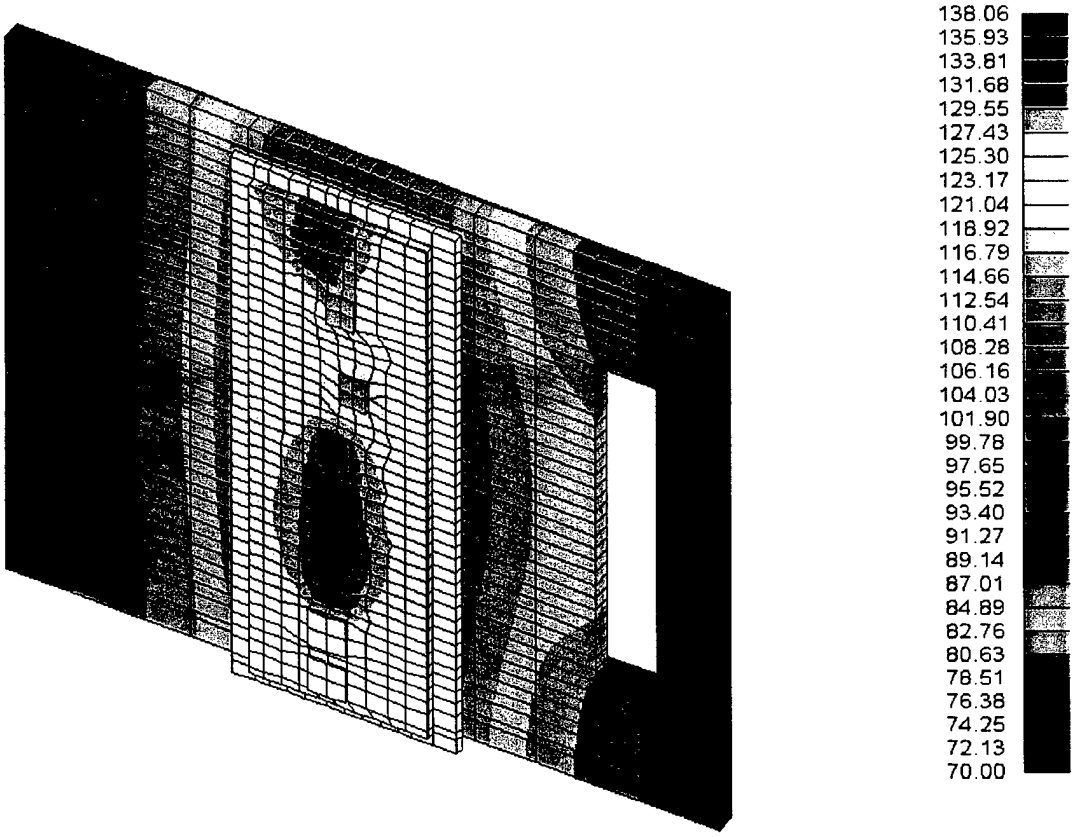


Figure 10. Temperature Contour Plot of Baseline Hybrid Regulator

Table 3. Baseline Junction Temperatures Results from TAS Thermal Analysis

Part No.	Max. Junction Temperature (°C)
VR1	135
VR2	136
VR3	127
VR4	127
VR8	132
VR5	133
VR6	136
VR7	135
VR9	134
VR10	124

3.3.3 Analysis of Diamond-Enhanced Design

Both power regulator hybrids--HY1 and HY2--were modeled using TAS. Each hybrid consists of five high dissipating voltage regulators mounted on a diamond substrate. For the purposes of the analysis, voltage regulators are attached to the diamond substrate using 96%Sn-4%Ag solder. In addition, the hybrid is bonded to a PWB using 704019 epoxy. Figures 11 and 12 show top and profile views of the model.

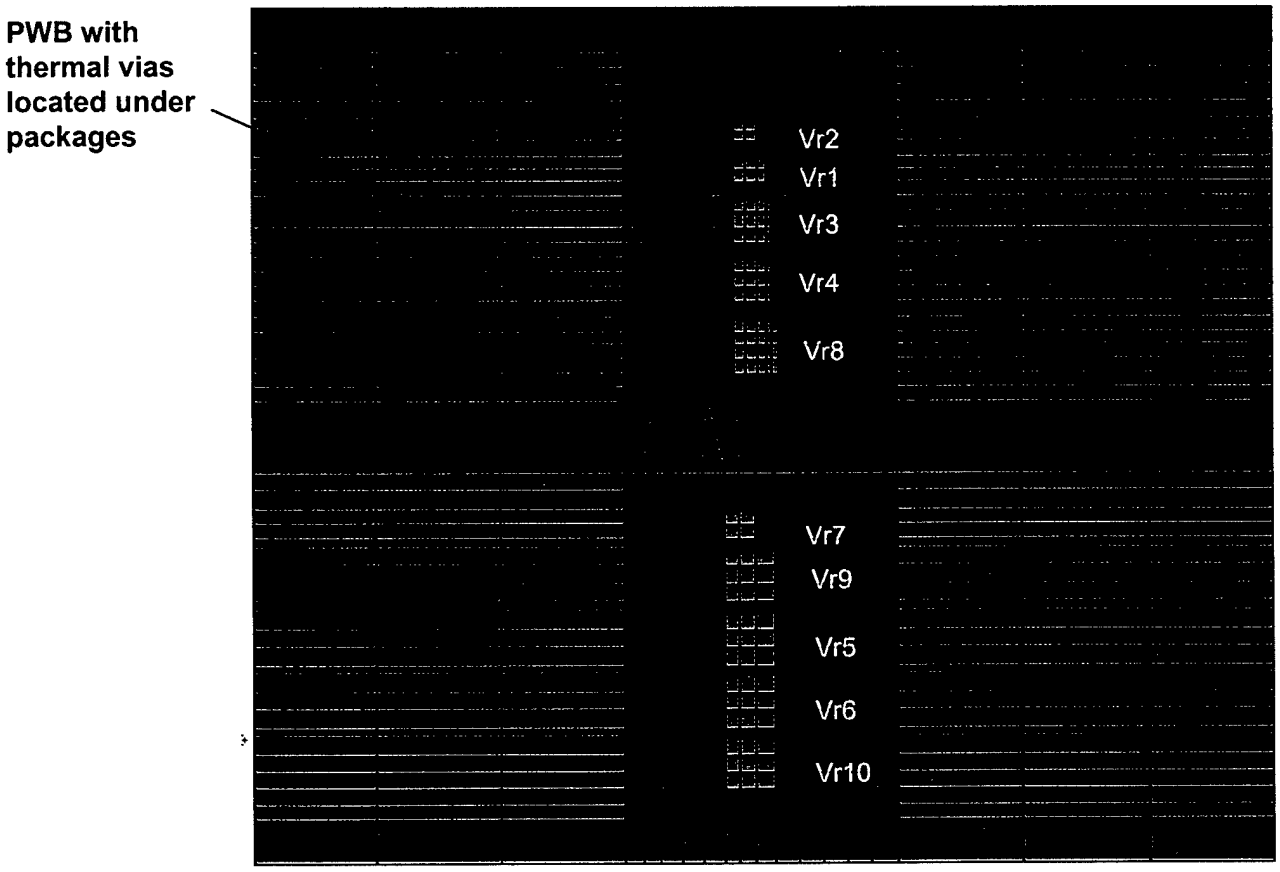


Figure 11. Thermal Analysis of Diamond Enhanced Model (Top View)

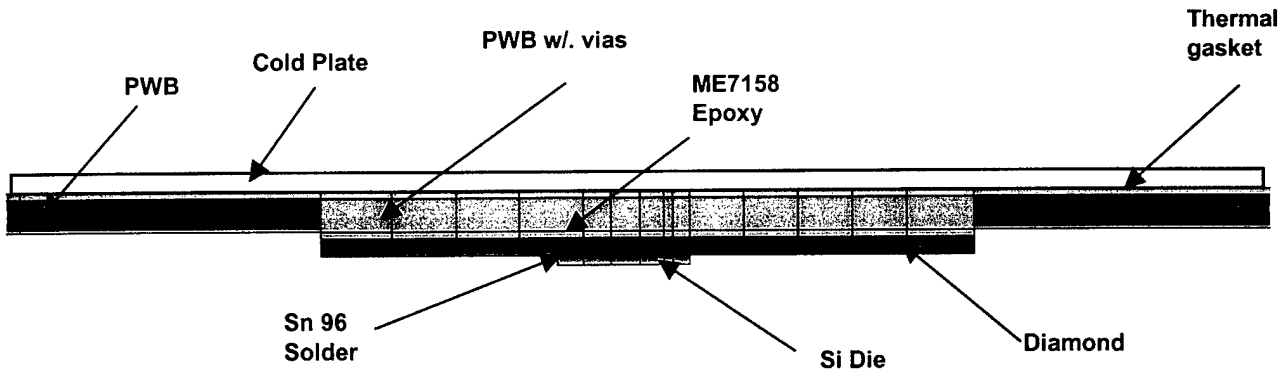


Figure 12. Thermal Analysis Diamond Enhanced Model (Profile View)

A detailed thermal analysis was performed on each power regulator hybrid. Identical to the baseline, a finite element analysis was performed using the Thermal Analysis System (TAS) software to generate the model and predict worst-case temperatures. The thermal conductivity for the PWB with vias was calculated based on 200 vias under each hybrid. Each via is plated with 0.003" of copper. The thermal conductivity was considered for the z-direction only. Table 4 shows the material thickness and coefficients of thermal conductivity used in the model. The following assumptions and conditions apply:

- Environment temperature: 70 ° C
- The interface resistance between the PWB and coldplate was obtained from Chomerics' datasheets (see Appendix C) for gasket Cho-Therm T609. The interface value used in the analysis is 1.5 W/in^2- ° C, which is a conservative number. The data sheets estimate a value of 2 W/in^2- ° C for 100psi of pressure.
- The thermal conductivity of the PWB under each hybrid was calculated based on a total of 200 vias/in^2. Each via is 0.020 in. in diameter and plated with 0.003 in of cooper. The thermal conductivity value used (0.35 W/in- ° C) is also a conservative number. The thermal conductivity is only taken into account in the z-direction.
- Conduction is the only mode of heat transfer used in the analysis.
- The total power dissipation used in the analysis is 68.7W.
- All regulator circuits are biased and operating in a continuous mode.

Table 4. Material Properties – Thermal Analysis

Material	Thickness (in)	Thermal Cond. (W/in-°C)
Diamond	0.02	38
PWB	0.05	0.01
PWB w/ vias	0.05	0.35 (z-direction)
Cho-Therm T609	0.01	1.5 W/in^2-C
ME7158	0.01	0.09
Si Die	0.013	3.7
Sn96	0.002	1.99

3.3.4 Results of Diamond-Enhanced Analysis

The circuit card assembly was mounted to the cold-plate using a thermal gasket Cho-therm T609 interface material. While this is an excellent method to enhance the thermal conduction between these two surfaces, it differs from the analysis performed on the baseline assembly, thereby making it difficult to assess the construct properties by comparison of the silicon die temperatures. Qualitatively, one can examine the difference in average temperatures between the package substrate and the surface of the silicon die. The analysis shows for the diamond enhanced package a 6-7deg ° C improvement in the difference between the temperature at the surface of the die and the substrate. The contour plots of this analysis are shown in Fig. 13.

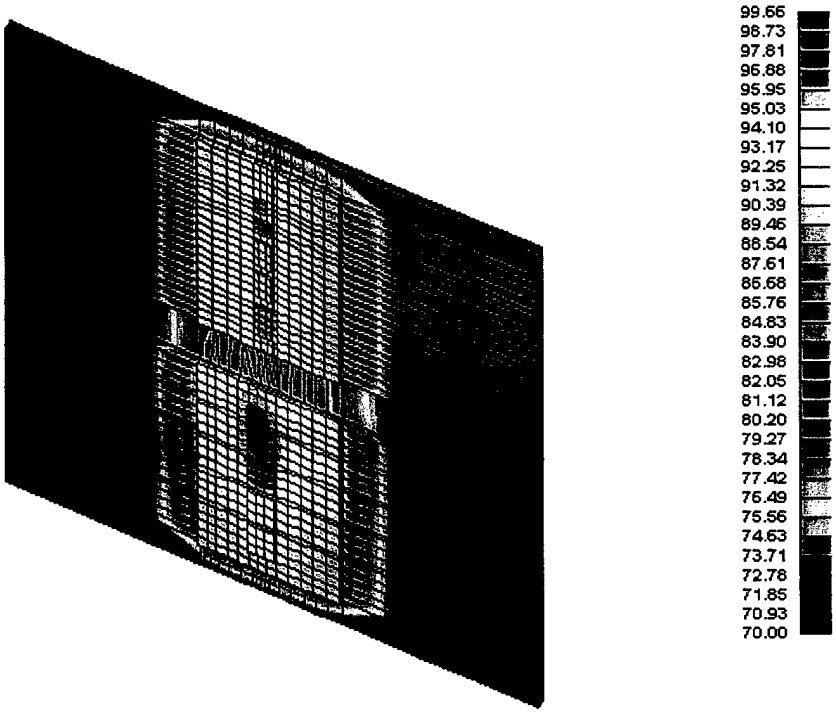


Figure 13. Temperature Contour Plot of Diamond-Enhanced Hybrids Sub-Assembly

3.4 Package Assembly and Process Development

The development of specific assembly techniques and processes was necessary in order to assemble diamond based packages. To support the development effort at Sanders, Astex supplied material from their 2" reactor process. This material was smaller (less area) than the eventual material for the electronic assemblies. However, it was adequate to perform the planned process experiments. (Note: The finished product was to be fabricated on Astex's 12" reactor process.) Planned process experiments included:

- 80Au/20Sn attach of ring and lead frames to diamond substrates.
- Wirebonding
- Silicon die attach
- Non-hermetic encapsulation

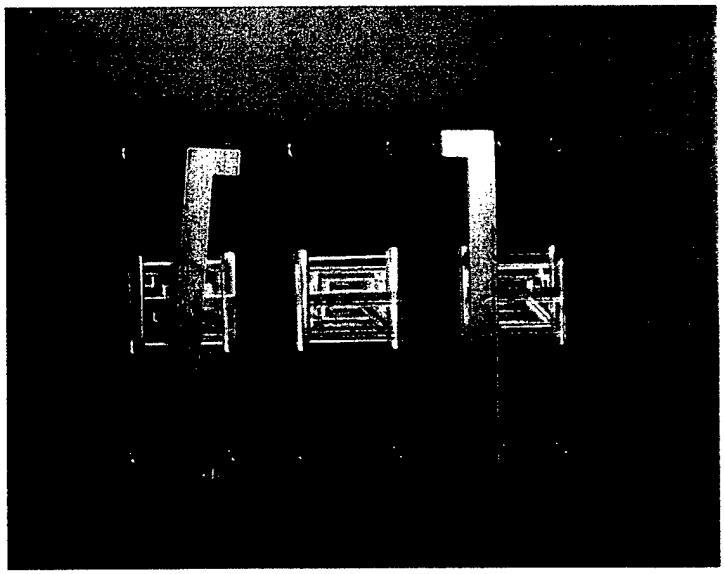


Figure 14. Ring Frame Assembly Fixture

3.4.1 Ring frame attach

To assemble the ring frames, a fixture was designed for use in a high intensity IR oven. The substrate, 80Au/20Sn preform, and ring frame were located into the fixture using bar clamps. The clamps were held in place by variable spring plungers that allowed for pressure adjustment. The fixture was coated in an aluminum oxide to resemble a black body and warm readily when exposed to the IR power source. The fixture is shown in Fig. 14.

Five assemblies were constructed to verify the soldering process. Solder wetting and fill was excellent. Fig. 15 shows an example of the solder wetting and coverage that was achieved for the inside and outside perimeters of the substrate/frame interface. Assemblies underwent temperature cycling (–55 deg C to +125 deg C) and constant acceleration. All assemblies passed hermeticity to 5 X 10^{-8} atm-cc/sec after environmental screening.

3.4.2 Metallization and Wirebonding

Sample substrates were metallized with 200-350Å of TiW, 500-1000Å of Au, 1000-2000Å of Ni, and, finally, with 100-150 micro inches of Au. This is a very common recipe used to metallize many microwave ceramic substrates. Wire bonding required no special processes. Slightly higher bond force was used as compared to alumina ceramic. Pull testing revealed no problems.

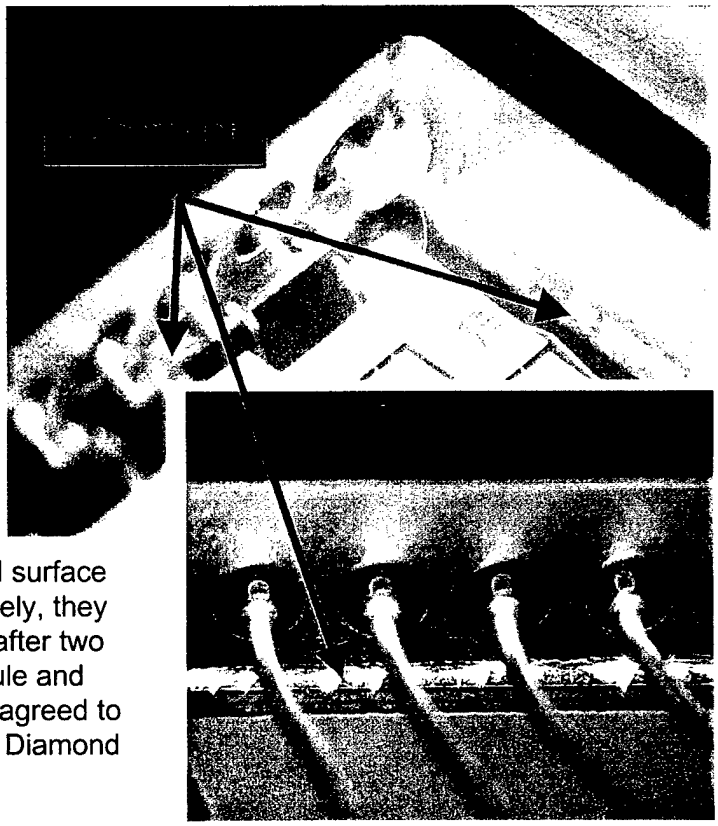


Figure 15. **Example of Solder Fillet at Ring Frame Substrate Interface.**

3.4.3 Diamond Substrate Fabrication

Astex struggled to supply useful substrate material from their 12" process. Observed problems included unacceptable flatness and surface conduction, an undesirable property. Ultimately, they were unsuccessful in delivering the material after two attempts. In the interest of preserving schedule and completing the program, Sanders and Astex agreed to procure substrates from a third party. Norton Diamond Films eventually supplied the material for the component build.

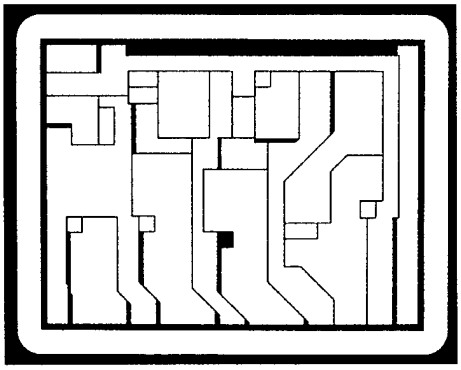


Figure 16. **Plated Diamond Substrate**

The vendor selected to plate the substrates was Film Microelectronics Incorporated (FMI). The same metallization recipe prescribed in Section 3.4.2 was used. FMI had almost no experience plating diamond substrates. After completing patterning, resistance measurements revealed surface conduction in unplated areas that were normally isolated by design. The hypothesis was that the RF plasma cleaning step may cause surface damage, effectively "graphitizing" the surface, making it conductive. The RF plasma exposure was subsequently reduced from 600W of power for 2 min. to 60W for 10sec. This eliminated the problem.

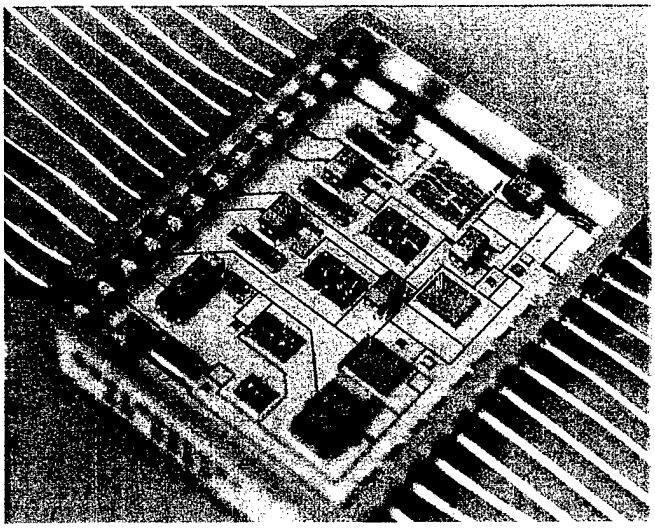


Figure 17. **Hybrid 1 Diamond-Based Power Regulator Assembly**

4.0 Module Integration and Test

4.1 Module Integration

Five packages of each hybrid type were assembled. Photographs of the completed assemblies are shown in Figs. 17 and 18. The silicon die were attached using three attach methods:

- 80Au/20Sn
- 96Sn/4Ag
- H35 Epoxy

Passive components were attached using H35 Silver epoxy. All interconnect wire-bonding was accomplished using 0.7 and 1.0 mil ballbonds. Thermal and mechanical merits of each die attach method were evaluated by X-raying assembled units prior to test. X-ray revealed that 80Au/20Sn attach provided outstanding, void-free results (i.e. <10% voiding). 96Sn/4Ag results were poor--voiding was in excess of 50% in most cases. Later in this report, IR measurement results reveal much higher device junction temperatures in the 96Sn/4Ag samples.

4.2 Hybrid Testing

To perform the electrical testing and thermal image scanning, Hybrid modules needed to be powered and thermally stable. High power dissipations required a special test box. A test box was designed and built that would allow for each of the hybrids to mount directly to a large copper heat sink. DC power is routed from the main supplies to (9) nine individually selectable regulator channels. Output power is dissipated in a resistive load to simulate the array electronics. The box was designed to integrate easily with the thermal imaging test equipment. A photograph of the test stand is shown in Fig. 19. The thermal imaging equipment uses an IR sensor to scan the sample at a selected baseplate temperature. The resolution for this experiment was about 4μ m x 4μ m pixel. This allowed us to measure the average die temperatures.

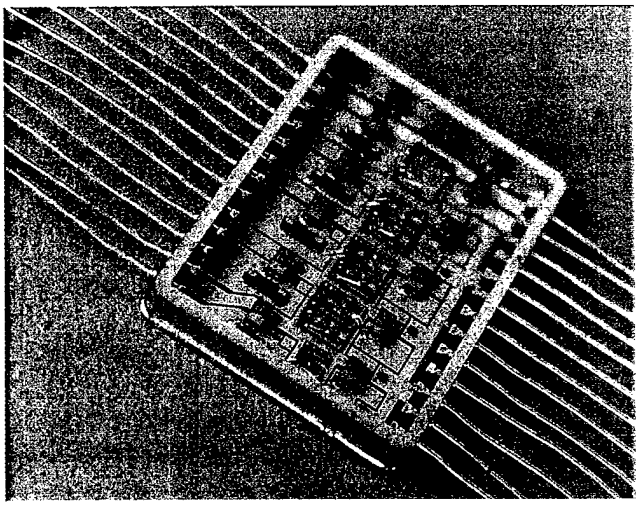


Figure 18. **Hybrid 2 Diamond-Based Power Regulator Assembly**

4.2.1 Electrical Testing

Three (3) units of each type were electrically tested. Trim resistors were adjusted in each unit to meet the design output voltage. Measured results for a typical regulator are shown in Tables 5a and 5b.

Dissipated power, in some cases, is higher than the values used in the preliminary thermal analysis. Tests were conducted in accordance with (IAW) present program demands.

Table 5a. Measured Results from Hybrid 1 Electrical Test.

Regulator	Title	Voltage In	Voltage Out	Voltage Drop	Load Resistor	Load Current	Power Dissipation (Watts)	
VR2	-5 V	-10.01	-4.90	5.11	7.04	0.70	3.56	
VR1	-10 V	-14.90	-10.01	4.89	25.06	0.40	1.95	
VR3	$3.2V_A$	5.75	3.08	2.67	2.01	1.53	4.10	
VR4	$3.2\ V_B$	5.75	3.18	2.58	2.01	1.58	4.07	
VR8	$12\ V_A$	14.74	12.08	2.66	4.03	3.00	7.98	
							21.66	**Total**

Table 5b. Measured Results from Hybrid 2 Electrical Test.

Regulator	Title	Voltage In	Voltage Out	Voltage Drop	Load Resistor	Load Current	Power Dissipation (Watts)	
VR7	9.1 V	14.90	9.00	5.90	5.54	1.63	9.59	
VR9	$12\ V_B$	14.90	11.96	2.94	4.02	2.98	8.76	
VR5	5.5 V	9.07	5.54	3.53	1.35	4.12	14.53	
VR6	$6.5\ V_A$	9.07	6.57	2.50	17.29	0.38	0.95	
VR10	$6.5\ V_B$	9.07	6.54	2.53	4.02	1.63	4.12	
							37.94	**Total**

4.2.2 IR Imaging Test

The hybrid test box was designed to integrate easily with the thermal imaging test equipment. A photograph of the test stand is shown in Fig. 19. The thermal imaging equipment uses an IR sensor to scan the sample at a selected baseplate temperature. The resolution for this experiment was about 4μ m x 4μ m pixel. This allowed measurement of the average die temperatures.

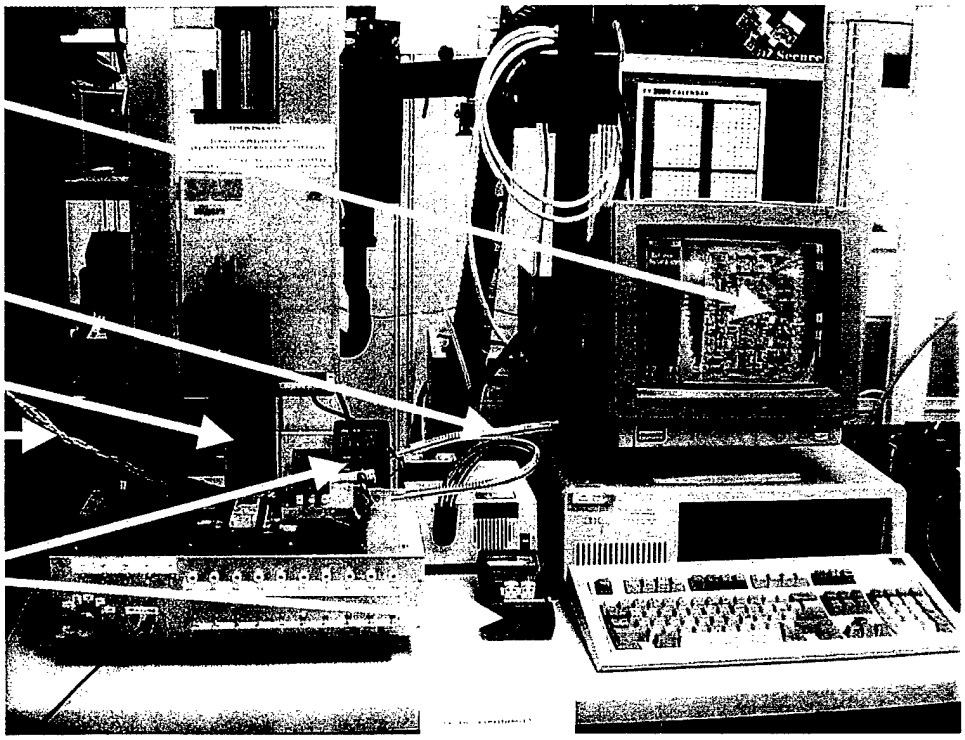
Computer Image of Thermal image of powered Hybrid

Lighting

IR Sensor

Input Power

Multiple Temperature Sensors for Emissivity calibration



Heater

Diamond enhanced hybrid

Copper Heat sink

Selectable Regulator switch

Selectable Input Power switch

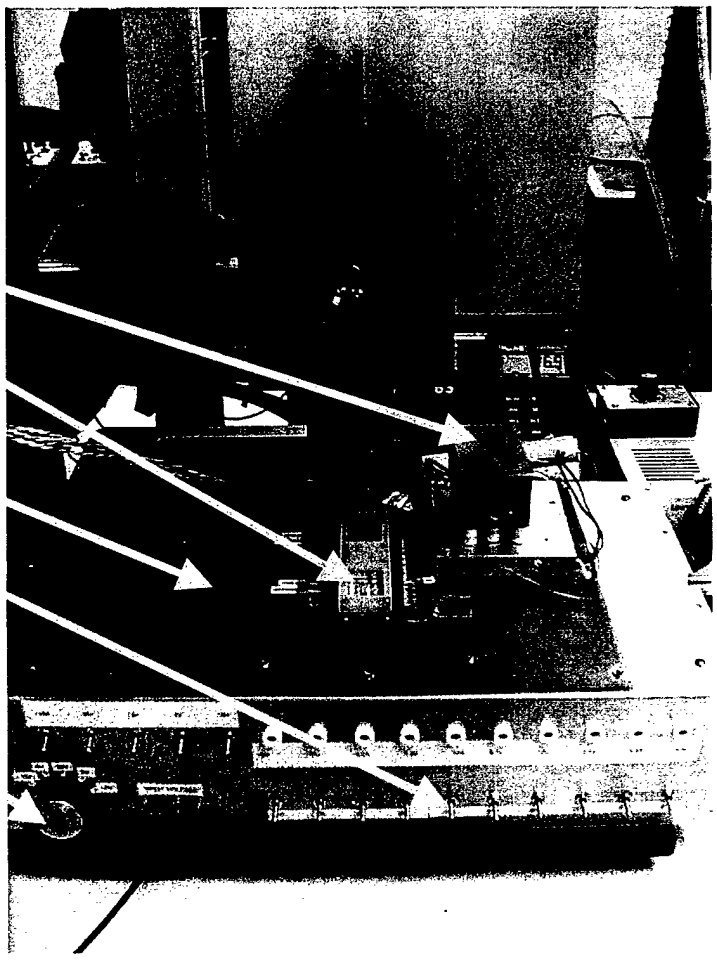


Figure 19. IR Scanning Test Set

5.0 Thermal Analysis

The ability of diamond substrates to conduct heat in the lateral direction is highly beneficial. The effect is to create a large area for transfer of heat across the thermal boundary to the adjacent material or heat sink. As energy in the form of heat, Q, moves away from the transistor and toward the relatively large heat sink, it spreads laterally over an area. The effective heat spreading angle, ϕ, varies as a function of geometry and composition of the construct. If the lower layer is a good thermal conductor, then the spreading will be minimized but greater than zero. If the lower layer happens to be relatively poor, then the spreading will be much greater, but less than 90° lateral spreading. It is in this latter scenario where diamond is particularly useful.

The thermal impedance for a component is dependent on the geometry and the characteristic thermal conductivity of the material and is defined as

$$\theta_{th} = \frac{1}{K_{th}} \frac{T}{A}$$

Diamond substrates do not offer a particular advantage were the packaging stack is thermally optimized. The heat spreading angle is small (small area), as in a diamond based package soldered to a copper heat sink. In this case, the primary advantage comes only from the high thermal conductivity of the diamond. If a less than optimal construct is employed, where the package is attached to a PWB for example, then lateral conduction in the diamond substrate is rapid and the spreading angle of the heat is increased.

The data obtained from measurements could not be compared directly to the baseline packaging, which was included as scope in the original plan. Costs would have been prohibitive, as multiple test stands would have had to be designed and built in addition to sample baseline modules. Instead, diamond-enhanced hybrids would be measured, then models created for the diamond version and baseline. The two constructs would be compared via these models.

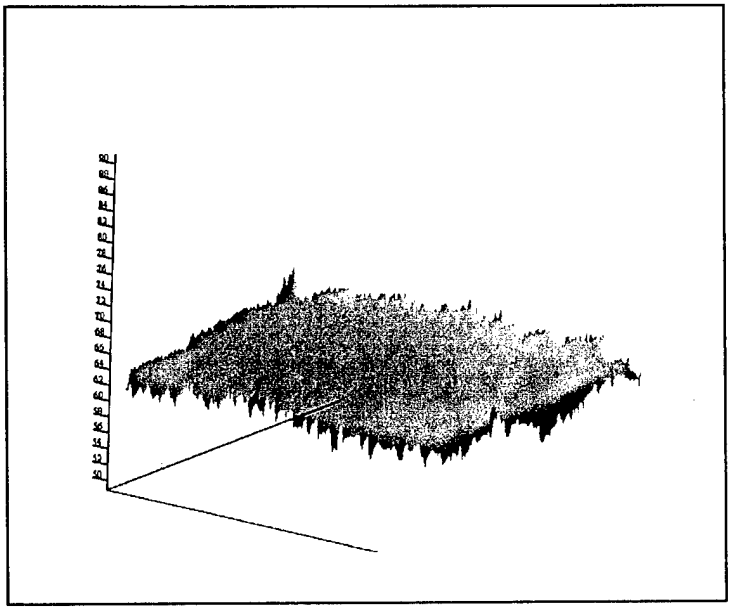


Figure 20. Scanned Temperature Plot of Hybrid 2 with One Sheet of Grafoil™

One experiment devised to evaluate the effectiveness of diamond was to increase the thermal resistance placed between the diamond package and copper heat sink. The interface material was a graphite-based compliant foil (Grafoil™, Union Carbide.). The thermal conductivity is >7 W/cm-K. Sheet thickness is .005".

IR scanning measurements were made where one (1) and three (3) sheets were used. The results of this could then be compared to the baseline package under the same set of conditions.

The first attempt at the experiment yielded confusing results. In fact, the behavior was precisely the opposite of what was expected. The sample with three sheets of Grafoil™ measured lower in temperature than the same package with only one sheet. After careful examination, it was determined that the package had .001"- .003" of bow. It was hypothesized that by adding the additional Grafoil™, the quality of the interface had actually been improved.

The experiment was repeated with different samples and the results were as expected. Figs. 20 and 21 are surface plots of average temperatures across the entire hybrid package area. All regulators were enabled. Die temperatures increased 16 °C, from 74°C, in the case of 1 sheet, to 90°C where 3 sheets were used. These results are modeled and compared to a baseline model later in the thermal analysis section.

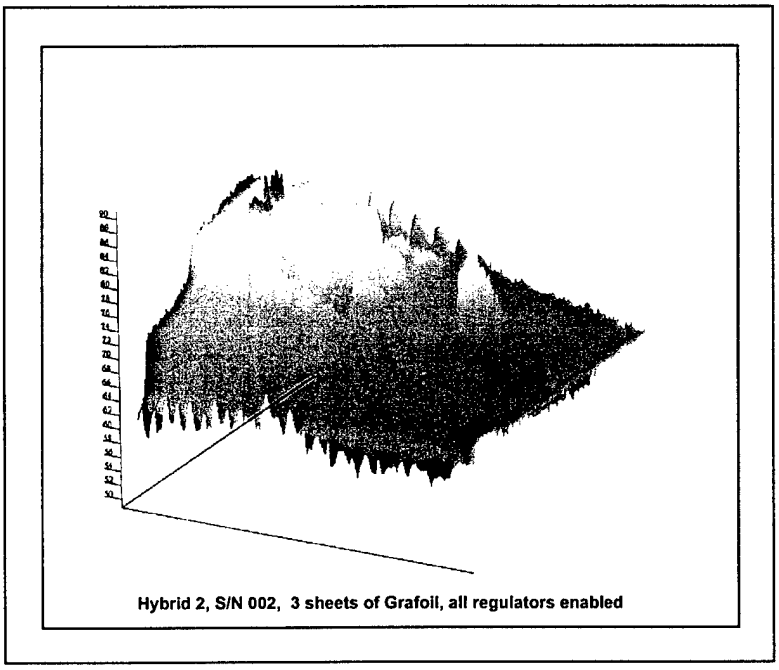


Figure 21. Temperature Plot for Hybrid 2, Three Sheets of Grafoil™

A second experiment was conducted where half the area was removed from the center of the .005" interface layer. By eliminating conduction through the center of the package, all heat transfer must be horizontal in the substrate material, through the Grafoil™ along the edge, and down to the copper heat sink. Again, only conduction is assumed. The experiment is designed as a severe test of the lateral conduction qualities of the substrate material. Fig. 22 is a sketch of the modified Grafoil™ interface.

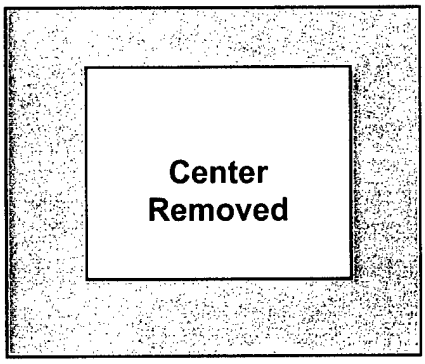


Figure 22. Sketch of 0.005" Thick Grafoil™ Interface, Half Area Removed

The measured results for the diamond-based hybrid are shown in Fig. 23. Again, a surface plot is offered. The average silicon die temperatures are approx. 90°C.

Comparing Figs. 21 and 23, the superior lateral spreading ability is immediately apparent. There is no measurable difference in die temperatures between a near optimal and intentionally degraded thermal interface.

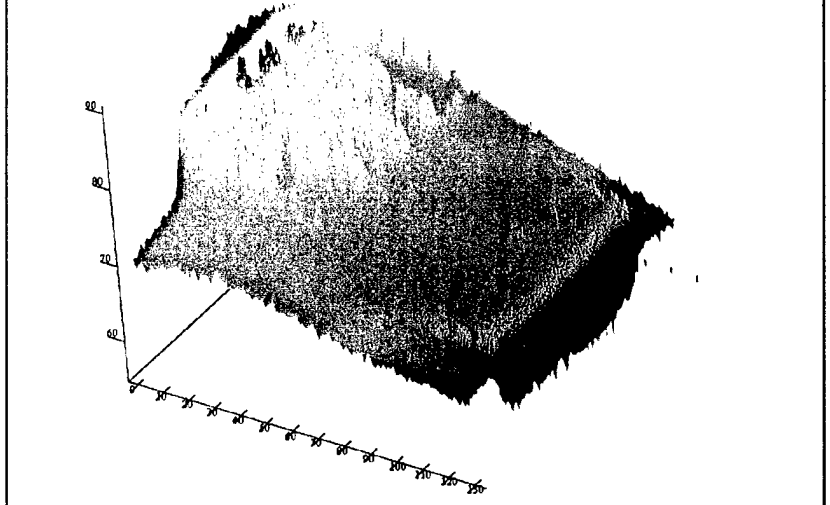


Figure 23. Temperature Plot for Hybrid 2, 50% Grafoil™ Removed

A baseline regulator was not available. Therefore, comparing the thermal images of a baseline regulator and diamond hybrid with an intentionally induced void in the thermal interface was not possible. Thermal analysis software (TAS) was utilized to make this comparison.

Figures 24a and 24b show the finite element analysis of a diamond based Hybrid 1 with one sheet of Grafoil™ and one sheet of Grafoil™ with 50% of the area removed as shown in Fig. 22. The thermal plots show a very small increase, 3°C, in the silicon die temperatures in this extreme case.

The substrate used in the model was then modified to simulate a Hybrid 1 with a BeO substrate. This allows a more direct comparison of the benefits of lateral spreading of diamond in a package with a sub-optimal thermal interface (i.e. voiding).

Figures 25a and 25b show a hypothetical Hybrid 1 with a BeO substrate with the same interfaces as above. In this model, there is a significant increase in the silicon die temperatures, approximately 14°C, and the benefits of diamond are well illustrated.

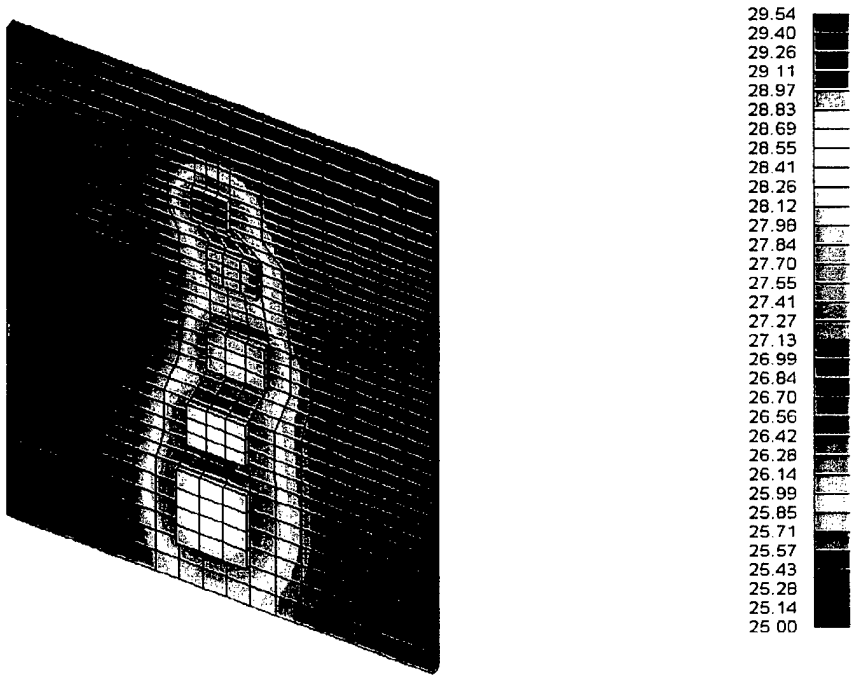


Figure 24a. **Temperature Plot of a Diamond-Based Hybrid 1 with Intact Thermal Interface**

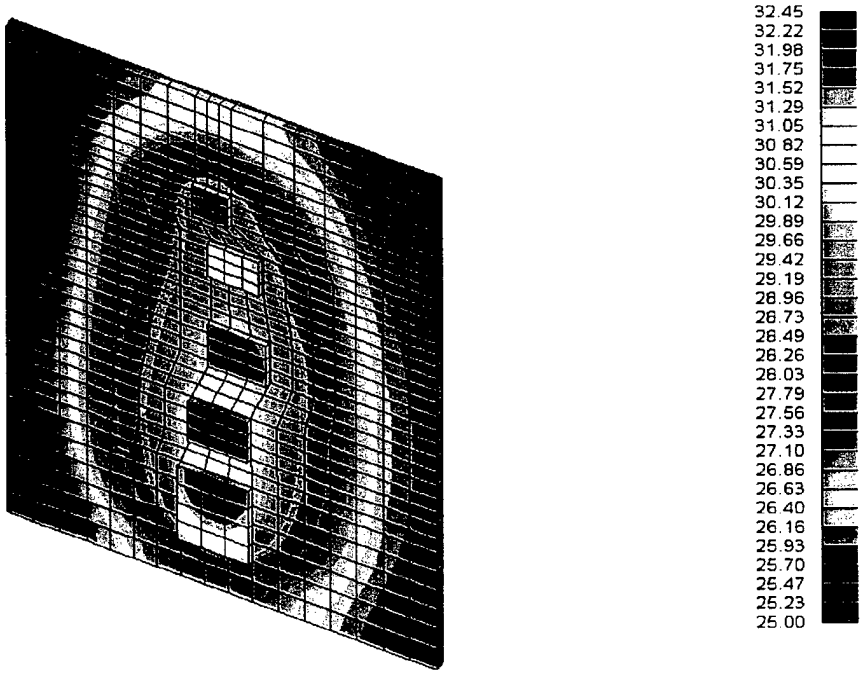


Figure 24b. **Temperature Plot of a Diamond-Based Hybrid 1 with 50% Void in Thermal Interface**

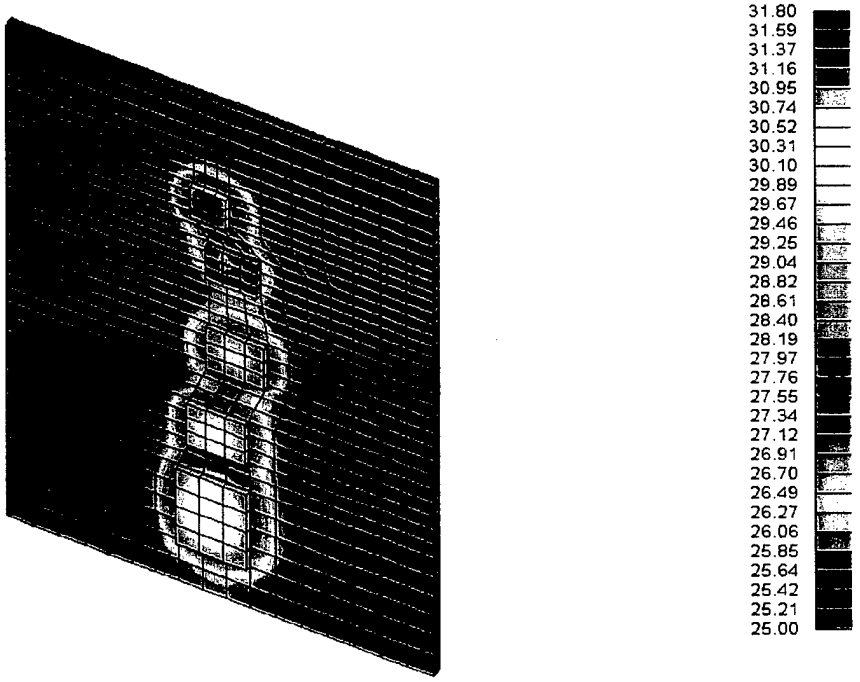


Figure 25a. **Temperature Plot of a BeO-Based Hybrid 1 with Intact Thermal Interface**

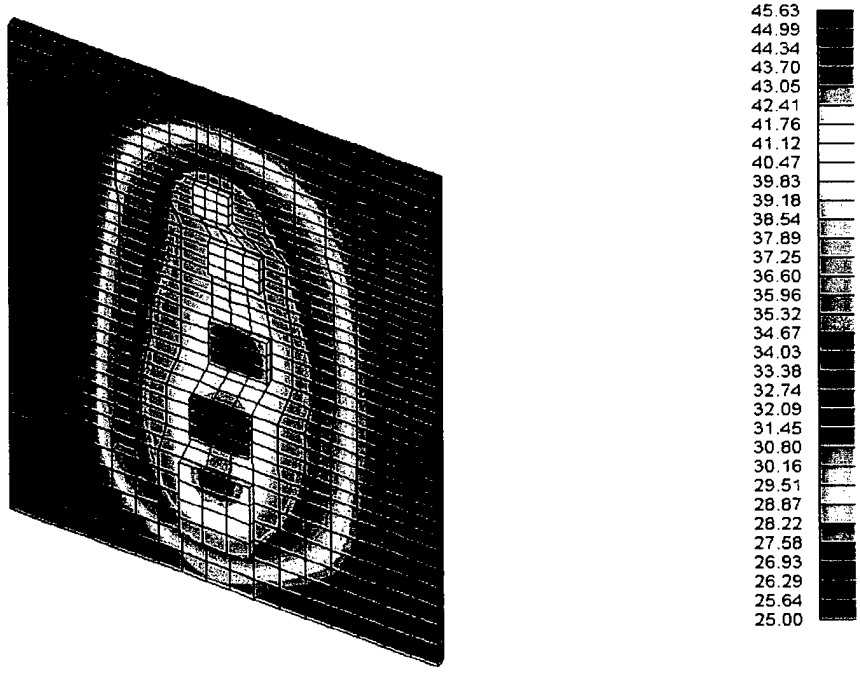


Figure 25b. **Temperature Plot of a BeO-Based Hybrid 1 with 50% Void in Thermal Interface**

6.0 Stress Analysis

6.1 Temperature Cycling

One of each electrically functional Hybrid 1 and Hybrid 2 were selected for temperature cycling in accordance with MIL-STD-883 (Method 1010, Condition B). The units cycled 15 times from -55°C to 125°C with a dwell time of twenty minutes and a transfer time of less than one minute.

6.2 Acceleration Testing.

The Hybrid 1 and Hybrid 2 units that had been subjected to thermal cycling were then subjected to constant acceleration in accordance with MIL-STD-883 (Method 2001). The hydrids were restrained by the housing and accelerated in the Y1 orientation at 5000g for one minute.

6.3 Results of Mechanical and Thermal Stress

No defects attributed to temperature cycling or acceleration were detected. The units were first inspected visually, and then electrical testing was performed. Hybrid 1 was fully functional. Hybrid 2 had one non-functioning regulated output. After careful examination, it was discovered that a bond wire had fused. This mode of bondwire failure could not be caused by the above stresses. This failure was likely induced by shorting a hybrid lead to the test box chassis during testing.