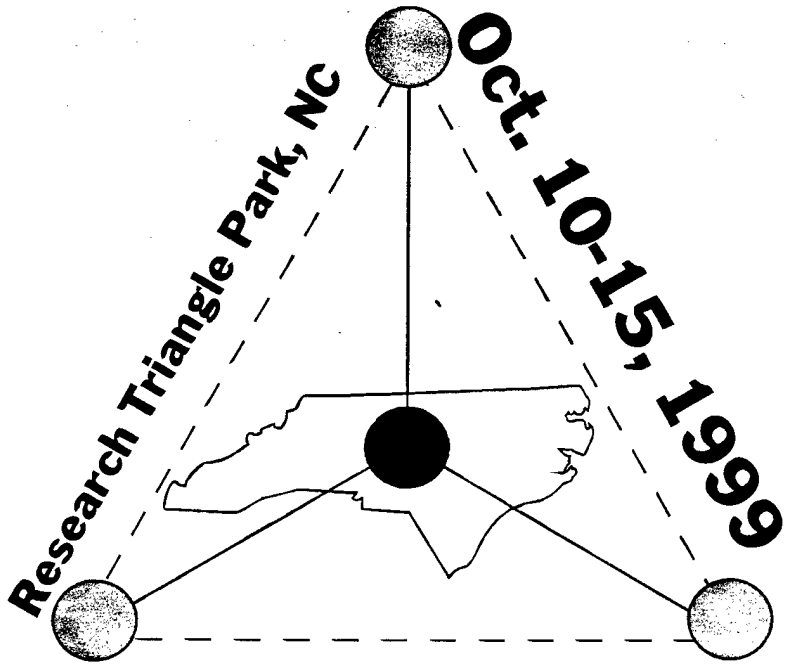
Silicon Carbide and Related Materials - 1999

Part 2



ICSCRM '99

Editors:

Calvin H. Carter, Jr., Robert P. Devaty and Gregory S. Rohrer

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Proceedings of the International Conference on Silicon Carbide and Related Materials - 1999
Research Triangle Park, North Carolina, USA
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Editors:

Calvin H. Carter, Jr., Robert P. Devaty and Gregory S. Rohrer

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Preface

These volumes contain written versions of papers which were presented at the International Conference on Silicon Carbide and Related Materials 1999 (ICSCRM'99), held October 10-15, 1999 in Research Triangle Park, North Carolina. Over 650 participants from 25 countries attended the conference. This attendance was the highest in the conference series to date.

This record attendance and the large number of papers submitted attest to the rapidly increasing interest in wide bandgap semiconductors in both academic and industrial communities. Contained in the two volumes of these proceeding are 401 papers, 19 of which were invited. They document our present understanding of the many topics of interest, such as the growth of bulk crystals, the growth of epitaxial layers, theoretical approaches, materials characterization, device processing and design, fabrication and characterization of electronic and optoelectronic devices, some with outstanding performance.

The success of the conference was due in large part to the labor of many people on the various committees as well as the generous support of four U.S. Government and thirteen industrial sponsors. We wish to thank the students from the University of Pittsburgh (Song Bai, Oleg Shigiltchoff, and Yevgeniy Shishkin) and Carnegie Mellon University (S.-Y. Ha, T. Jang, T. Kuhr, and E. Sanchez) for their hard work in getting the papers organized and reviewed. We also wish to thank the students from the University of South Carolina for helping the session chairpersons and handling the microphones for questions during the conference. Finally, we thank the staff of the North Carolina State University Department of Continuing Education for their hard work in organizing the conference, especially Connie McElroy-Bacon, Cindy Allen and Dee Dee Coon.

The next conference will be held in October, 2001 in Tsukuba, Japan. Prof. S. Yoshida of Saitama University will chair the Organizing Committee, Prof. H. Matsunami of Kyoto University will chair the International Steering Committee and Prof. S. Nakashima of Miyazaki University will chair the Sponsor Committee. We wish the organizers of the next conference much success.

Durham, Pittsburgh, October 1999

Calvin H. Carter, Jr.

Robert P. Devaty

Gregory S. Rohrer

OVERVIEW

PART 1:

PART 2:

Table of Contents

Chapter 2: SiC Epitaxy and Thin Film Growth

2.1 Homoepitaxial Growth

2.2 Heteroepitaxy and Thin Film Growth

Chapter 3: Physical Properties of SiC

3.1 Surfaces and Interfaces

3.2 Structure

3.3 Optical Properties

3.4 Electrical Properties

3.5 Magnetic Resonance

PART 2:

Chapter 4: Processing of SiC

4.1 Polishing

4.2 Doping and Implantation

4.3 Contacts and Etching

4.4 Oxides and Other Dielectrics

4.5 Micromachining

Chapter 5: SiC Devices

5.1 Surveys

5.2 Unipolar Devices

5.3 Bipolar Devices

5.4 Sensors

Chapter 6: Growth of III-Nitrides and Related Materials

Chapter 7: Physical Properties of III-Nitrides

7.1 Surfaces and Interfaces

7.2 Structure

7.3 Optical and Electrical Properties

Chapter 8: III-Nitrides: Processing and Devices

Chapter 4

Processing of SiC

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Physics of SiC Processing

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Keywords: Boron Diffusion, Degradation of SiC MOS Capacitors, Doping by Ion Implantation, Implantation-Induced Defect Centers, Negative-Bias-Temperature Instability

Abstract. Three topics are briefly discussed: 1) The generation of intrinsic-related defect centers by ion implantation. 2) The diffusion mechanism of boron in SiC. 3) The degradation of 6H-SiC MOS capacitors which are operated at temperatures above 600K.

Introduction

The improvement of the crystal quality of 6H- and 4H-SiC wafers, the progress in developing suitable device processes as well as advances in the understanding of the physical properties of this material made it possible to realize electronic devices providing outstanding properties. Nevertheless there are still many open questions left, which have to be solved; a few crucial topics are revealed in the following. Doping by ion implantation is an absolutely necessary technology because of the small diffusion coefficients of most of the dopants; however, this technique requires high annealing temperatures to remove the implantation damage and to electrically activate the dopants. As an unintentional side effect implantation-induced defect centers are generated, which partially survive annealing temperatures up to 1700°C and which may degrade the performance of devices. Among the predominating dopants like nitrogen (N), aluminum (Al), and boron (B) only B diffuses strongly at the annealing temperatures applied. The diffusion mechanisms are still under discussion. With respect to MOS devices several problems arise; one is the channel mobility, which is much lower in 4H-SiC than in 6H-SiC, and another one is the long term stability of interface and oxide properties under certain operation conditions. It is the aim of this paper to contribute a few results to these processing-relevant tasks.

Implantation-induced defect centers

A first problem that arises by implantation of any species into a compound semiconductor like SiC is the disturbance of stoichiometry [1]. As demonstrated in Fig.1, the implantation of a Pearson B profile (dotted curve) at a maximum concentration of $8x10^{19}cm^{-3}$ causes an excess of Si atoms near the surface of approximately $10^{18}cm^{-3}$ (solid curve) because of the heavier mass of the Si atoms and at the trailing edge of the B profile an excess of carbon (C) atoms of the same order of magnitude (dashed curve). This stoichiometric

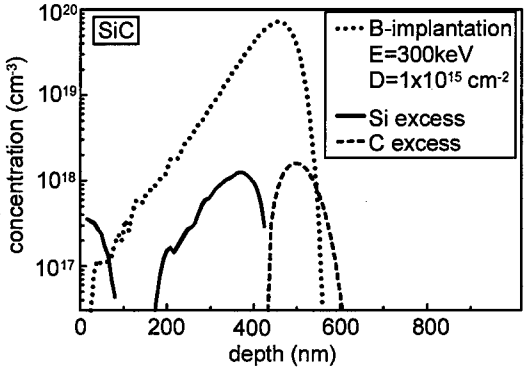

Fig. 1 Distribution of excess Si and excess C caused by implantation of a Pearson B profile (calculated after [2]).

disturbance may affect the diffusion of dopants or lead to an enhanced formation of intrinsic-related defect centers.

In order to test whether the formation of implantation-induced defect centers depends on the mass of the implanted ions, atoms with different masses (hydrogen (H), helium (He), neon (Ne) or argon (Ar)) were implanted. By multiple implantation, box-shaped damage profiles were generated in n-type 6H-SiC epilayers (N doping concentration=$4x10^{15}cm^{-3}$) to a depth of 1.6μm. The individual fluence of the different ion species was determined in such a way that the generated total vacancy concentration (calculated by TRIM_C [2]) resulted in [Vac] = $10^{18}cm^{-3}$. Annealing of the implanted samples was performed at temperatures between 800°C and 1700°C. Deep level transient spectra (DLTS) of two sets of samples annealed at 800°C and 1400°C are displayed in Figs.2(a) and (b), respectively. Subsequent to the anneal at 800°C a series of defect centers is observed as demonstrated in Fig.2(a) (the nomenclature is adopted from the literature; see e.g. [3]); their ionization energies and electron capture cross sections are summarized in Table 1. The generated defect centers are independent of the implanted ion species; however, their concentrations strongly depend on them. The E_1/E_2-, Z_1/Z_2- and RD_5- center reach concentrations between $5x10^{15}cm^{-3}$ and $10^{16}cm^{-3}$. The DLTS spectra taken on samples, which were exposed to an anneal at 1400°C, look similar (see Fig.2(b)), predominantly the E_1/E_2-center survived at a concentration of approximately $10^{15}cm^{-3}$, all the other defects are annealed out, their concentrations are below $10^{14}cm^{-3}$. The E_1/E_2-peak generated in 6H-SiC samples is extremely stable up to temperatures of 1700°C, it is caused by the same defect center like the D_I defect observed in low temperature photoluminescence spectra [4]; the chemical nature and microscopic structure of this defect are still not identified.

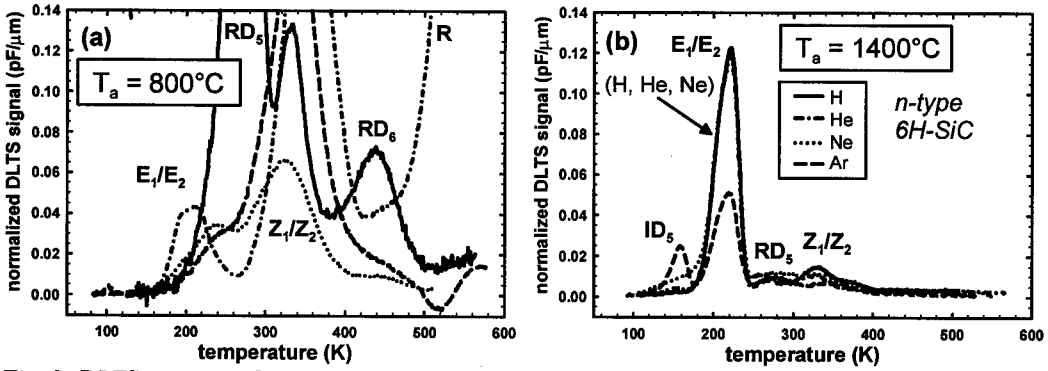

Fig. 2 DLTS spectra taken on n-type 6H-SiC samples, which were implanted with ion species of different masses (H, He, Ne or Ar); (a) annealed at 800°C, (b) annealed at 1400°C.

Table 1. Parameters of defect centers observed in DLTS spectra of n-type 6H-SiC samples, which were implanted with different ion species; ΔE and σ are evaluated for two temperature dependencies of σ: $\sigma \sim T^0$ and $\sigma \sim T^{-2}$;corrsponding deviations are considered by the error.

peak temperature (K) (t_1/t_2 = 1ms / 2ms)	defect center	ionization energy ΔE (eV) $\sigma \sim T^0$ / T^{-2}	capture cross section σ (10^{14} cm^2) $\sigma \sim T^0$ / T^{-2}
154	ID_5	0.3 ± 0.04	5 ± 4
215	E_1/E_2	0.44 ± 0.04	8 ± 2
266	RD_5	0.46 ± 0.05	0.15 ± 0.1
350	Z_1/Z_2	0.67 ± 0.08	6 ± 4
442	RD_6	0.79 ± 0.05	0.12 ± 0.1
570	R	1.26 ± 0.07	7 ± 3

Boron diffusion

At temperatures above 1400°C, implanted B atoms become noticeably mobile in SiC. As a consequence, the shape of implanted B profiles changes drastically and, in addition, outdiffusion of B atoms is observed [6]. The measured B profiles can consistently be simulated on the basis of the kick-out mechanism [7] providing evidence that this mechanism dominates the B diffusion. Because of the fact that B resides at Si lattice sites in SiC [8, 9], Si interstitials (I_{Si}) are necessary to kick B atoms from substitutional lattice sites; at interstitial sites, B atoms become highly mobile. To avoid the kick-out mechanism, the concentration of Si interstitials has to be reduced either by recombination or by binding them in stable complexes. We have tested this diffusion model by coimplantation of C and B as shown in Fig.3(a) (profiles are calculated with TRIM_C); two Pearson C profiles (dotted curves) form the boundary for a box-shaped B profile (solid curve). The as-implanted B profile analyzed by SIMS is revealed in Fig.3(b) (solid curve). Subsequent to an anneal at 1700°C for 3 hours, the measured B SIMS profile has changed its shape. The residual B fluence is still 75% of the implanted fluence and an accumulation of B is observed in the areas of excess C (dotted curves). It is suggested that excess C atoms and Si interstitials form stable complexes like in Si [10]; in this way, Si interstitials are trapped and the B diffusion is blocked.

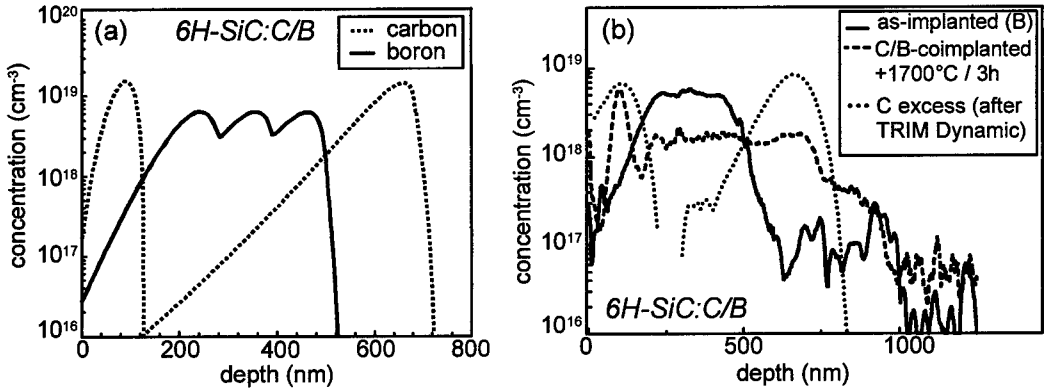

Fig. 3 (a) Coimplanted box-shaped B profile and C boundary profiles (Pearson) as calculated after [5]; (b) measured SIMS B profiles prior to (solid curve) and subsequent to (dashed curve) an anneal at 1700°C for 30min; for comparison, the total generated excess C is calculated after [2] (dotted curve).

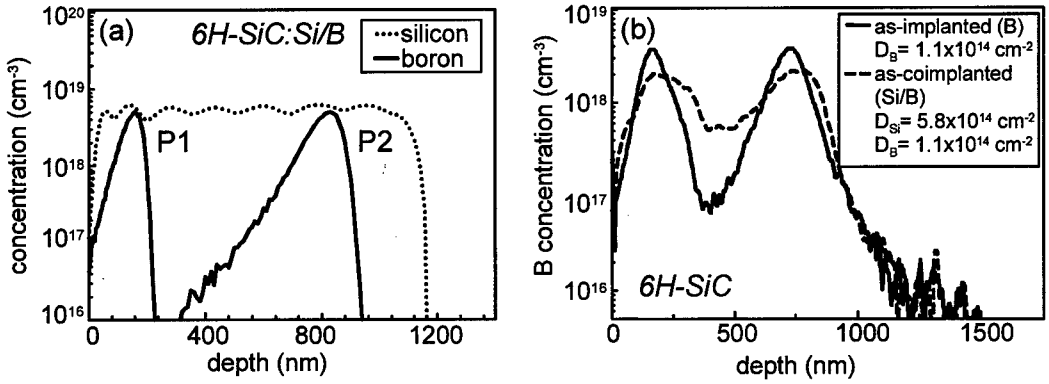

Fig. 4 (a) Pearson B profiles (P1/P2) and box-shaped Si profile as calculated after [5]; (b) measured SIMS profiles of an only B-implanted (profiles P1/P2, solid curve) and a Si/B-coimplanted (dotted curve) 6H-SiC sample as shown in (a).

In order to demonstrate that Si interstitials and e.g. not C vacancies are responsible for the B diffusion, we coimplanted Si/B and tested the diffusion behavior of the implanted Pearson B profiles (P1/P2) (see Fig.4(a)). In the presence of excess Si (Si is implanted first), profiles P1/P2 smear out already during the implantation process without any heat treatment as demonstrated in Fig.4(b) (see dashed curve). The solid curve in Fig.4(b) corresponds to the B SIMS profile measured in a sample, which has only been implanted with B. This B profile shows two sharp peaks, which agree sufficiently well with the implanted Pearson profiles P1/P2. Our experiments clearly support the kick-out mechanism for the B diffusion, which requires Si interstitials.

Degradation of 6H-SiC MOS capacitors operated at elevated temperatures

It has been shown that electron injection under UV illumination [11] and Fowler-Nordheim injection [12] degrades SiC/SiO_2 interfaces. In this section, we report on capacitance-voltage (C-V) investigations of 6H-SiC MOS capacitors, which are operated at temperatures above 600K; it turns out that such heat treatments may lead to an additional formation of charged defect centers at the interface and in the oxide [13].

MOS structures were fabricated on n/p-type 6H-SiC epilayers (Si-face, net concentration: N_N-N_{comp}=2x10^{16}cm^{-3} / N_{Al}-N_{comp}=10^{16}cm^{-3}). The oxide was thermally grown by wet oxidation (T_{ox}=1120°C, t_{ox}=12/24h, d_{ox}=54/110nm). The samples were subsequently exposed to a post-oxidation anneal in Ar at 1120°C for 1h; finally gold contacts were thermally evaporated (Ø=0.7mm).

The measurement sequence is schematically shown in the inset of Fig.5. The sample under investigation is sequentially heated up to a temperature ranging from 550K to 670K in a He ambient. At the degradation temperature, one MOS capacitor on the sample is kept under bias (-20V, oxide field: 1.6MV/cm) for a certain time (2min to 20min, open circles). Then the sample is again cooled down to room temperature and this particular MOS capacitor is analyzed by C-V (full circle). The corresponding C-V characteristics are displayed in Fig.5. With increasing degradation temperature, the C-V characteristics shift to positive voltages indicating that negative charges are generated and trapped in the oxide and/or at the SiC/SiO_2 interface. The degradation of p-type 6H-SiC MOS capacitors results in a fixed positive charge (not shown).

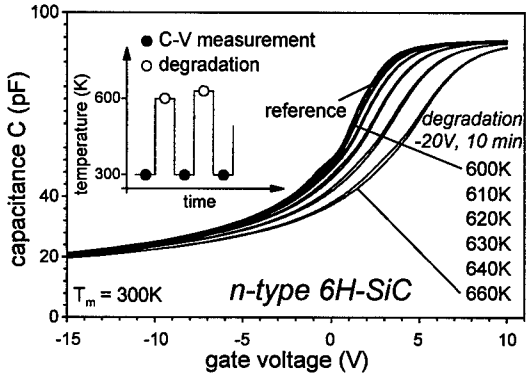

Fig. 5 C-V characteristics of an n-type 6H-SiC MOS capacitor taken each at room temperature T_m subsequent to the degradation process. The degradation was caused under depletion bias of V_i=-20V (oxide field 1.6MV/cm) for 10min at temperatures T_a ranging from 600K to 660K; the measurement sequence is indicated in the inset.

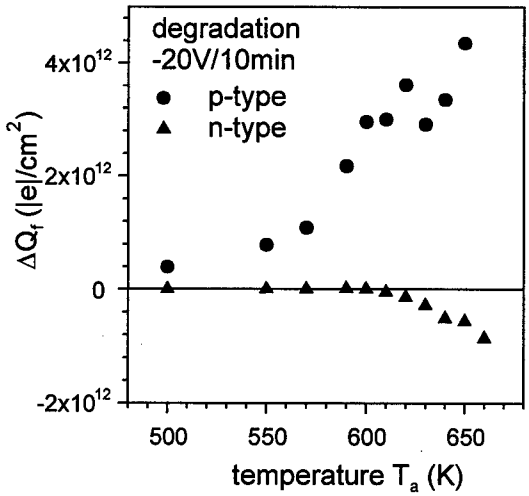

Fig. 6 Additionally generated fixed charge ΔQ_f for an n/p-type 6H-SiC MOS capacitor as a function of T_a for sequentially repeated degradation steps; ΔQ_f is calculated from the change of the flatband voltage.

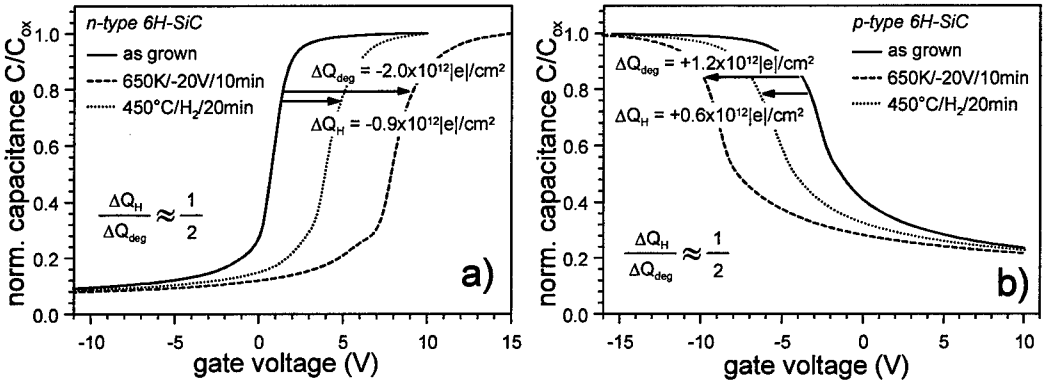

Fig. 7 C-V characteristics for (a) an n-type and (b) a p-type 6H-SiC MOS capacitor. Three experimental situations are revealed: as-grown (solid), degraded (dashed) and hydrogen passivated (dotted). Half of the fixed charge is passivated independent of the sign of the charge (see arrows, $\Delta Q_{deg}/\Delta Q_H$ = fixed charge subsequent to degradation / H-passivation).

Fig.6 reveals the additional (–/+) - fixed charge ΔQ_f generated in an n/p-type MOS capacitor as a function of the degradation temperature T_a. A detectable increase of ΔQ_f starts at $T_a \approx 600K$. It is important to mention that the degradation does not occur in neighboring MOS capacitors, which were not stressed by a negative bias.

In a further step, degraded n/p-type 6H-SiC MOS capacitors were subjected to a hydrogen passivation at 450°C for 20min in a $H_2(5\%)/N_2(95\%)$ ambient. In Fig.7(a), C-V characteristics are taken on an as-grown (solid curve), a degraded (dashed curve) and a hydrogen-passivated (dotted curve) n-type MOS structure; identical measurements taken on a p-type MOS structure are displayed in Fig.7(b). The hydrogen passivation leads to a reduction of approximately half the generated fixed charge independent of its sign: $\Delta Q_H/\Delta Q_{deg} \approx 1/2$. The entire passivation process occurs very quickly; it is completed almost after 2min.

Our experimental results can be explained in the framework of the "negative-bias-temperature instability (NBTI)" model introduced by Blat et al. [14]. These authors stressed n/p-type Si-based MOS capacitors by heat treatments at 600K under negative bias and proved experimentally that the generated concentrations of dangling bonds at the interface and of the fixed positive charge in the oxide are approximately equal; the positive oxide charge was proposed to be due to a hydrogen (water)-related species, because in case the NBTI occurred water had to be present in the oxide. By subsequent hydrogenation, the dangling bonds could completely be passivated while the fixed charge remained unaffected. In case of SiC-based MOS structures, we have to postulate two additional assumptions:

(1) Dangling bonds at the interface of SiC/SiO_2 are energetically deep (their energy position is not known yet); they cannot change their charge state during the voltage sweep and, as a consequence, they contribute to the fixed charge. However, this portion of the fixed charge can be passivated by hydrogen as is demonstrated in Figs.7(a) and (b). The charge

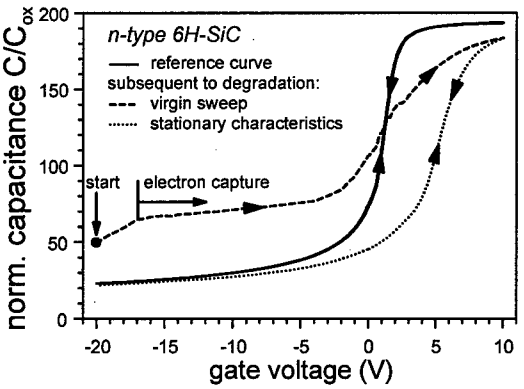

Fig. 8 C-V characteristics of an n-type 6H-SiC MOS capacitor; the solid curve corresponds to the as-grown reference, the virgin curve (dashed) is taken on the degraded MOS capacitor and the dotted curve displays the stationary characteristic.

state of a trivalent Si (≡Si·) depends on the position of the Fermi level; it may be positively ($\equiv Si^+$) charged for p-type SiC or negatively ($\equiv Si^-$) charged for n-type SiC.

(2) The water-related species in the oxide is amphoteric (like dangling bonds at the Si/SiO_2 interface).

These assumptions could experimentally be verified as is demonstrated in Fig.8. The solid C-V curve corresponds to the reference; it is taken on an as-grown n-type MOS capacitor. The dashed branch reveals the virgin curve of the degraded MOS capacitor, which was negatively biased during the ramp down from degradation to room temperature. The measurement was started in deep depletion where no free electrons were available at the interface. First the C-V curve increases steeply at negative bias (≈-20V) indicating a large positive charge. As soon as free electrons are available at the interface ($V_{gate} \geq -17V$), energetically deep dangling bonds as well as fixed oxide states trap electrons and turn to a negative charge state causing a flatter slope of the C-V curve. The dotted characteristic corresponds to the stationary C-V curve of the degraded MOS capacitor, which is stable under the conditions applied. The NBTI model for SiC can be described by the following two equations:

$\equiv Si\text{-}H + X + 2\ holes \Leftrightarrow \equiv Si^+ + Y^+$ and (p-/n-type SiC-MOS capacitors)

$\equiv Si^+ + Y^+ + 4\ electrons \Leftrightarrow \equiv Si^- + Y^-$ (n-type SiC-MOS capacitors)

X, Y are unknown, hydrogen- or water-related species in the oxide.

The NBTI may cause serious reliability problems in SiC MOS devices operated at negative bias and at temperatures above 550K, especially when the oxide is grown under wet conditions [14].

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Polishing and Surface Characterization of SiC Substrates

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Keywords: Annealing, CMP, KOH Etching, Polishing, Substrate Flatness, Surface Roughness

Abstract: We have developed a chemi-mechanical surface preparation process for SiC which produces surface roughness values (Ra) below 5Å and peak-to-valley variations (PV) below 55Å. Non-contact surface profilometry, Atomic Force Microscopy, KOH etching, and Photon Back Scattering techniques have been compared for evaluation of surface finish quality. A short, low temperature KOH etch has been found to be a quick, effective method for revealing the degree of subsurface damage which does not directly correlate with surface roughness.

Introduction

SiC has rapidly gained interest in recent years as a substrate for the fabrication of epitaxial devices based on SiC and III-nitrides. Applications include SiC power switching and microwave devices, as well as nitride-based high intensity, short wavelength LEDs [1, 2] and laser diodes [2]. Epitaxial techniques to produce such devices are driving the need for improvements in substrate surface finish [3, 4]. In this study, we assessed the effect of mechanical and chemi-mechanical surface-finishing techniques on the substrate surface roughness and subsurface damage.

Surface roughness, a key figure-of-merit for substrates with typical Ra values in commercial wafers between 2-6 Å, has been used to guide our chemi-mechnical polishing development activities.

The amount of subsurface damage introduced by the polishing process is much more difficult to determine. Two approaches that have previously been used to assess subsurface damage are Photon Back Scattering (PBS) [5] and Transmission Electron Microscopy (TEM) [4]. Another technique for analyzing residual subsurface damage is KOH etching applying an approach similar to the method used to evaluate subsurface damage in sapphire substrates [6]. With this approach, we have been able to remove an extremely thin layer of substrate material and decorate subsurface polishing damage.

Experimental

We prepared on-axis 6H substrates using the following surface finishing procedure: After slicing of the boules, the substrates were double-side lapped using 9 micron diamond-based slurry to achieve planarity. Subsequently, the substrates were mechanically polished with three successively finer grades of diamond-based slurries from 6 micron to < 1 micron.

In order to reduce surface roughness, some of the substrate surfaces were prepared using mechanical polishing followed by a final chemi-mechanical polishing (CMP) step on a rotating platform. Two CMP approaches were used. Our initial effort focused on a process for CMP of SiC reported in literature [3]. We found that the surface characteristics reported could only be achieved

for off-axis surfaces and by using extremely high force per substrate unit area making this technique impractical for a production process. An alternative CMP process which requires approximately one tenth of the force/area has been developed and used for this study. For comparison, the properties of as-received substrate surfaces from two commercial vendors were evaluated.

Two techniques were used to evaluate the surface roughness during the polishing process. Measurements of average, rms and peak-to-valley roughness were made using a Zygo non-contact surface profilometer having a resolution of 1 Å. For each surface, an array of nine measurements across the substrate was used. These measurements were complemented by Atomic Force Microscopy (AFM) on the same surfaces.

Subsurface damage was assessed using KOH etching in combination with non-contact surface roughness measurements and by photon backscattering (PBS). Controlling the temperature and time of etching allowed for minimal material removal while revealing areas of damage below the surface. PBS measurements provide a semi-quantitative assessment of surface and subsurface damage using an optical backscattering technique [5].

Results and Discussion

Mechanical polishing was initially used to prepare surfaces for on-axis 6H SiC substrates. Typical surface roughness values obtained by mechanical polishing are Ra of 10-12 Å and PV of 200-250 Å. A CMP process [3] using colloidal silica under a high force per unit area reduced surface roughness by approximately a factor of two. However, the high force per unit area did not appear to be suitable for production-scale polishing of on-axis SiC substrates.

Fig. 1 illustrates the significant reduction in surface roughness of CMP finished substrates as measured by non-contact surface profilometry (Ra and PV) over the last nine months. Current Ra values are less than 5 Å, and PV values are less than 50 Å. The improvements were primarily achieved by consecutive optimization and consistent control of the polishing wheel surface (pads versus metallic), the diamond carrier / lubrication agent (water soluble versus oil soluble slurry) and the pH of the solution, the diamond type (polycrystalline versus resin-bonded or single crystalline diamond), the diamond concentration in the slurry, the diamond size distribution (use of very uniform particle size), and to a lesser extent by applied force, temperature, and plate speed. For comparison, the average roughness values for commercially available on-axis 6H substrates from two vendors are shown in Fig. 1.

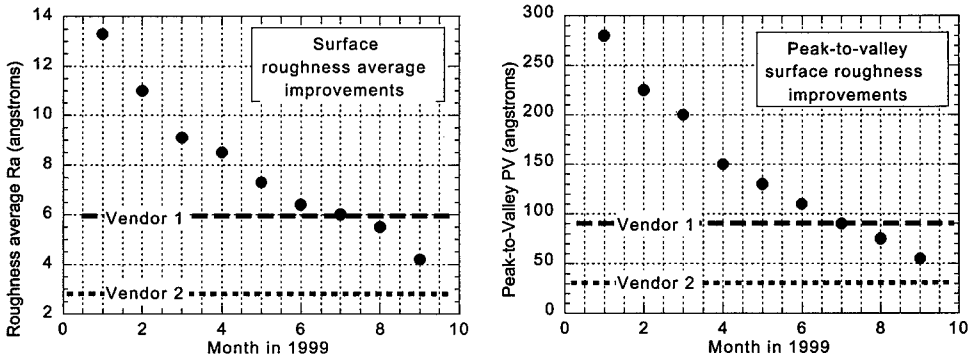


Fig. 1: Chemi-mechanical polishing has rapidly reduced the average surface roughness (Ra) *(left)*, and peak-to-valley (PV) *(right)* of on-axis 6H SiC.

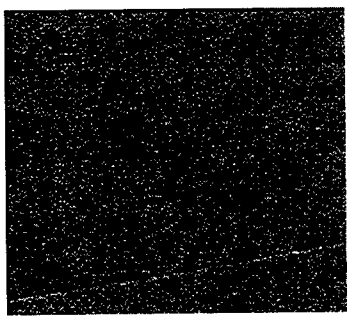
In addition, AFM has been used to evaluate the surface characteristics of SiC substrates. Fig. 2 shows an AFM image of a typical CMP surface and a comparison of AFM and non-contact surface profilometry measurements on the same set of samples. The relative roughness values determined by AFM and non-contact profilometry agree very well, yet the absolute roughness values derived from the AFM measurements are lower than the values determined utilizing a profilometer.

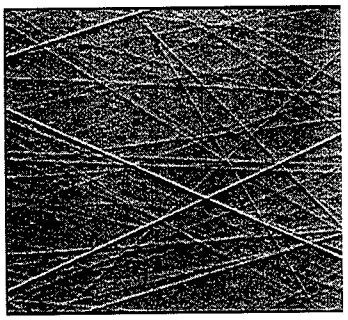
	Ra (Å) determined by Atomic Force Microscopy	Ra (Å) determined by Non-Contact Surface Profilometer
Sample 1	0.61	2.0
Sample 2	4.4	5.8

Fig. 2: AFM image of chemi-mechanical polished surface and a comparison of average surface roughness measurements for non-contact surface profiler and AFM.

In addition to surface roughness, characterization of subsurface damage, which is reported to extend 0.5-1.0 times the diamond particle size into the polished material [4], is required to assess surface finish quality. In our experience, subsurface damage can not be directly correlated to surface roughness measurements.

A KOH etching technique has been used to identify subsurface damage as part of the optimization of our CMP process. For example, Fig. 3(a) shows a profiler image of an as-polished CMP surface (Ra = 2.9 Å, PV = 52 Å) which appears 'scratch-free'. Fig. 3(b) shows the decoration of subsurface scratches in the same surface after KOH etching for 2 min at 390°C. We estimate that on average a layer of less than 0.06 microns thickness was removed by KOH etching under these conditions. Similar decoration of subsurface damage has been observed for commercially available substrates having an initial surface roughness Ra as low as 2 Å. A series of temperature-time etching combinations were evaluated. Fig. 3(c) shows the increase in measured Ra and PV of our CMP substrates after etching as a function of etch time at 390°C.





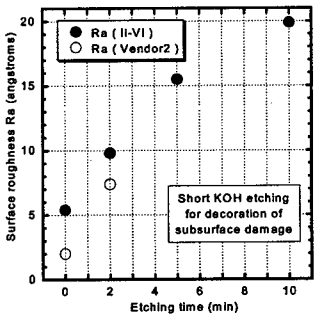


Fig. 3: Non-Contact Profilometer images of on-axis 6H SiC:

(a) surface before etching, Ra = 2.9 Å

(b) surface after 2 min KOH etch at 390°C, Ra = 6.5 Å

(c) Roughness average Ra versus KOH etch time at 390°C

Based on this data we have determined that an etch time of 1-2 minutes at 390°C provides sufficient material removal to decorate subsurface damage. Etching experiments with longer duration or at higher temperature removed layers that were thicker than the subsurface damage layer. This method also tends to decorate structural and crystallographic defects such as micropipes and single Burgers vector screw dislocations making the subsurface damage etch features significantly harder to identify.

PBS has been evaluated as an alternative method for characterization of subsurface damage using the same set of substrates. For example, Table 1 shows PBS intensity (given in units of ppm/steradian), indicating subsurface damage, for an on-axis 6H CMP surface and for commercially available substrates. For comparison, profilometer Ra measurements before and after etching are included in Table 1. The PBS technique indicates there is some backscattering due to surface and subsurface damage in the CMP sample and in one commercial substrate. We found good agreement between PBS and KOH etching for identification of polishing damage.

Table 1. Comparison of KOH etching and PBS techniques for determining subsurface damage.

Sample	PBS Intensity (ppm/steradian)	Ra (as polished) (Å)	Ra (2 min KOH etch) (Å)
II-VI CMP Surface	52	5.8	9.4
Vendor 1 Surface	58	6.0	8.1
Vendor 2 Surface	5	2	7.4

An annealing step of the finished 41 mm wafers at 1200°C for 60 min in argon atmosphere inside a SiC-lined container improved the wafer bow from 19.7 μm before annealing to 0.52 μm after annealing. Ongoing investigations support the idea that this bow reduction by annealing is achieved by a dislocation-related reduction of stress that is induced during the PVT growth process.

Summary

We have rapidly evolved mechanical and chemi-mechanical substrate finishing processes for SiC and produce substrates with surface roughness (Ra < 5Å) which is comparable to those now commercially available. A short, low temperature KOH etch was used to identify residual subsurface polishing damage. Low surface roughness substrates were found to exhibit residual subsurface damage. Annealing of single-side polished substrates was effective for improving flatness and reducing growth- or fabrication-induced stress and bow.

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Comparison of Mechanical and Chemomechanical Polished SiC Wafers Using Photon Backscattering

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Keywords: 4H-SiC, Atomic Force Microscopy, Chemomechanical Polish, Micro Raman, Photon Backscattering, Transmission Electron Microscopy

Abstract: We report a study of subsurface damage in 8° off axis 4H-SiC wafers using Photon Backscattering (PBS) along with atomic force microscopy, transmission electron microscopy and micro-Raman spectroscopy. PBS is a non-distructive subsurface defect detection technique that has been used for evaluation of silicon and gallium arsenide wafers. We have used PBS to evaluate as-received wafers from various suppliers as well as chemomechanical polished wafers. PBS results are compared with TEM, AFM and micro-Raman. As received wafers all show signs of mechanical polishing induced scratches. Chemomechanical polished wafers are scratch free and do not show directional damage typical of mechanical polishing seen in PBS maps of as-received wafers.

Introduction

High quality epitaxial films of silicon carbide and group III nitrides require SiC substrates with defect free surfaces. At present, commercially available wafers are all mechanically polished. A recent study [1,2] has demonstrated that a significant percentage of the defects in epitaxial SiC layers are initiated at surface and subsurface defects on the SiC substrate and not at defects in the bulk of the substrate such as micropipes. Electrically active defects have been reported in the near surface region of SiC wafers as well [3]. Chemomechanical polishing (CMP) has been reported to improve both the surface and subsurface of SiC wafers [4]. While surface defects can usually be observed by optical microscopy and atomic force microscopy (AFM) techniques, subsurface damage is more difficult to detect. Zhou et al. [4] used cross section transmission electron microscopy (XTEM) to demonstrate the removal of subsurface damage with their CMP process. Photon Backscattering (*PBS*®) is a non-distructuve evaluation technique developed by VTI, Inc. which has been shown to be effective in evaluating subsurface damage in silicon and gallium arsenide wafers. We report here on the application of PBS to as-received commercial SiC wafers and to CMP SiC wafers and demonstrate the effectiveness of PBS as a non-distructive evalaution technique for this material. Both as-received and CMP wafers were evaluated with a variety of techniques including AFM, TEM and microRaman scattering, as well as PBS.

Experimental Detais

Bulk wafers of n-type 8° off axis 4H-SiC grown by the physical vapor transport technique were received from three seperate suppliers under the terms of the DARPA High Temperature Electronics Program. After characterziation, selected wafers were given CMP treatment using the collodial silica technique of Zhou et al. [4]. AFM measurements were made on a Digital Instruments Nanoscope III. TEM measurements were made with a JEOL 200 kV machine.

The PBS measurement uses scattered laser light to detect groups of small, crystalline defects just below the polished surface of a semiconductor wafer. The laser is P-polarized and fixed at a 55° angle of incidence. This insures that the majority of the incident light penetrates the surface and scatters from defects below the surface. The scattered light is detected over a very small angle (0.0002 Sr) in the plane of incidence and in the backscatter direction (25°). This minimizes the effect of surface roughness on the scattered light while, at the same time, enhancing the signal from the subsurface defects. Due to the wide bandgap of SiC, the usual 632.8 nm laser probe wavelength could not be used for the PBS experiments. Instead the 325 nm line from a He-Cd UV laser was used with a spot diameter of about 0.4 mm. Under these conditions, the defect detection depth in SiC is 6-7 μm. Two meaurement sequences were done for each wafer to obtain the PBS result. The first involves rotating the plane of incidence through 360° about a fixed spot while plotting the scatter intensity. This is repeated several times at adjacent spots near the center of the wafer and the data used to form a polar plot called a V-MAP. Peaks in the V-MAP indicate defect orientation patterns in the subsurface. The maximum scatter direction is selected from the V-MAP, the plane of incidence aligned in that direction and an X-Y scan of the surface is performed. The resulting area map shows scatter intensity in ppm/Sr versus position and depicts the defect structure in the wafer.

Results

AFM images of an as-received wafer and the same wafer after CMP are shown in fig. 1. Scratches

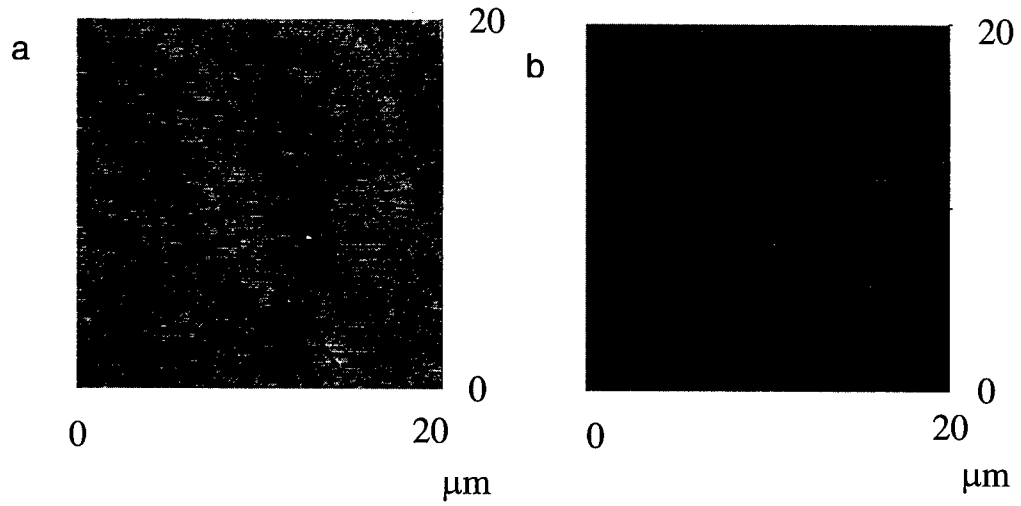

Fig. 1: Atomic Force Microscopy images of an 4H-SiC wafer (a) as-received, and (b) after Chemomechanical polishing

are clearly seen in the as-received wafer. Scratches were seen in all as-received wafers studied regardless of the supplier. The size of the scratches varied amongst the suppliers however. The typical depth and width of the larger scratches in the wafer shown in Fig. 1 are 3.0 and 250 nm respectively. The least damaged wafers as determined by the scratch size were provided by another supplier. Typical maximum scratch dimensions for those wafers were 0.5 and 35 nm. We were unable to observe scratches by AFM after CMP, as seen in fig. 1. TEM studies revealed sursurface damage in the as-received wafers similar to that observed by Zhuo et al. [4]. The damage extended

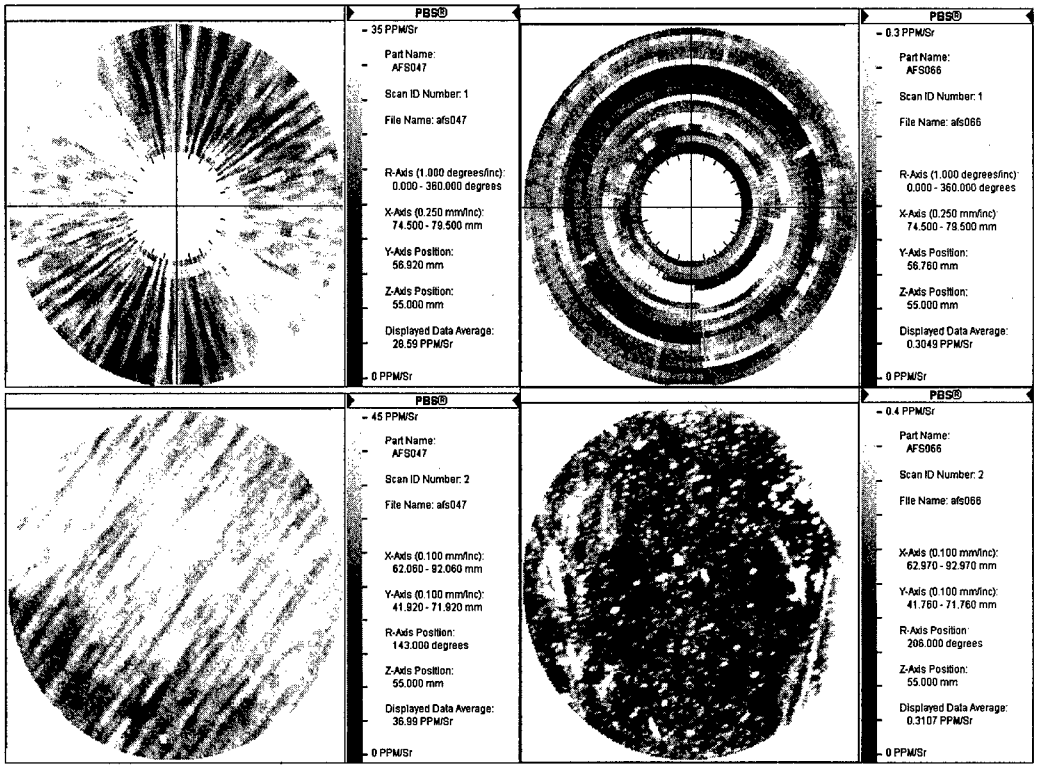

Fig. 2: PBS results for one 4H-SiC wafer. Top left: V-Map, as-received; Top right: V-map, after CMP; Bottom left: area map, as-received; Bottom right: area map, after CMP.

about 20nm below the surface and was not observed after CMP, in agreement with the AFM results. Micro-Raman experiments were perform on as-received and CMP wafers. These experiments suggest that the coupled LO phonon-plasmon mode is frequency upshifted and broadened asymetrically after CMP and the near surface carrier concentration is increased slightly compared to as-received wafers. These results are being investigated further.

The PBS results are shown in Fig. 2. This figure shows gray scale V-MAPs and area maps of the scattered light intensity for the same wafer before and after CMP. The area map for the as-received wafer is plotted on a 0 to 45 ppm/Sr scale and has an average scattered light intensity of 39 ppm/Sr. After CMP the area map average is 0.31 ppm/Sr and is plotted on a 0 to 0.4 ppm/Sr scale. The scattered light had a strong directionality in the as-received wafer but not in the wafer after CMP. This can be seen as the damage trace lines on the area map and the diametrical lines on the V-MAP.

The small scattering areas seen in the CMP wafer are believed to be related to micropipes or other large defects. The micropipe density in this wafer was reported to be less than 10 cm^{-2}. These results are typical of all as-received and CMP wafers studied in that, regardless of the the source, as-received wafers had a streaky pattern suggestive of the much finer scale AFM images with a strong directionality. The scattering intensity did vary amongst the various suppliers, however, and the wafers of the supplier that had the finest scratches as determined by AFM also had the lowest scattered light intensity, with a maximum of about 5 ppm/Sr. Some indication of a scratch-like pattern was seen in some wafers after initial CMP but this disappeared when the CMP was repeated a second time.

Conclusions

All as-received n-type 8° off axis 4H-SiC wafers showed signs of some surface and surface damage when examined with AFM and PBS. In general the most heavily damaged wafers as determined by the size of the scratches seen in AFM had the highest scattered light intensity when studied by PBS. CMP was found to significantly reduce the damage in n-type 8° off axis 4H-SiC wafers. Neither AFM nor PBS detected signs of scratching after CMP. TEM results demonstrate the CMP is effective in removing subsurface damage from these wafers. Micro-Raman results however suggest that the surface is worsened by CMP.

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Damage-Free Surface Modification of Hexagonal Silicon Carbide Wafers

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Keywords: Damage, Etching, Lapping, Polishing, Sub-Surface Damage

Abstract – This paper outlines the general procedures for reducing the total lapping and polishing time for the preparation of silicon carbide wafers. By employing an abbreviated mechanical lapping/polishing process, coupled with chemical etching, the total process machine time has been reduced from 10+ hours to 65 minutes or less. The finished surface quality is comparable to commercially available wafers.

Introduction

The processing of semiconductor silicon carbide (SiC) in some respects parallels the same procedures employed in common silicon wafering. In both cases the wafer is subjected to a lapping or grinding process to planarize the wafer, followed by an etching or rough polishing sequence to remove residual damage. The last step is the so-called finish polish during which the surface roughness is minimized. The similarities between the two processes end with this general description. In the silicon approach lapping, etching, rough polishing, and finish polishing are single step processes optimized to minimize machine time. The silicon carbide approach invariably consists of multi-step lapping and polishing processes which are time consuming and tedious. This project was undertaken to "normalize" the SiC methods and develop a faster and more economical process. Figure I illustrates the basic methods. The first chart is typical of an optimized silicon process and the machine time is actually quite low. The second scheme is the multi-step process used to prepare brittle materials such as silicon carbide. The actual machine time for the multi-step process can vary substantially due to differences in slurry composition, down-force, and other factors, but machine times ranging from 10 to 60 hours are possible when multi-step processes are employed. [1,2] From the outset the machine time for this study never exceeded 10 hours and this is probably the more realistic time of the two extremes.

Procedure

The second chart of Figure I illustrates the typical silicon carbide sequence. The multistep process is long and is more expensive. Optimizing this process involved three key factors. First the quality of the saw cut must be excellent. Excessive sawmarks result in excessive thickness variation and taper, which require excessive lapping time to correct. In this study the wafers were limited to those cut by diamond wire saw. The

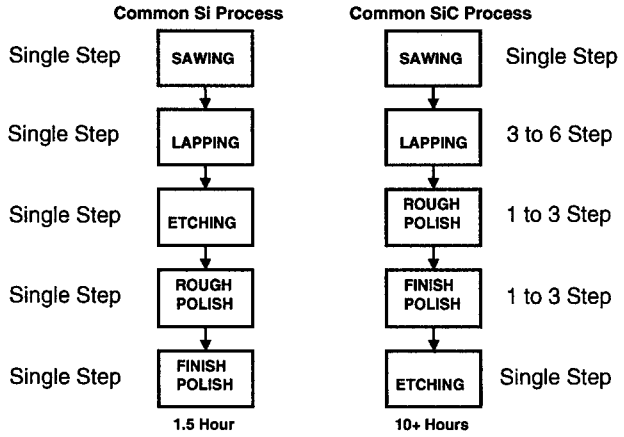


Figure I. A comparison of the two types of lapping/polishing cycles employed in the processing of semiconductors. Note that the machine time for the Si cycle is far shorter than the SiC cycle.

"as-cut" surfaces were essentially flat and artifact free, which reduced the initial lapping time by 75% (+) compared to wafers cut by OD or ID saws. The second factor was the minimization of the number of steps in the multi-cycle processes. The multi-step process described in Figure I varies from lab to lab. The only criteria for success is that each successive step must remove the damage left by the previous step. Data indicates that many of the lapping (grinding) steps were unnecessary if factors such as rotation rate, down-force, and abrasive composition were carefully controlled. Figure II actually suggests the basic approach. The wheel rotation rate can vary from 10 to 300 rpm and the down-force from 2-20 lbs., but these parameters must be consistent from step to step and repeatable from run to run. There are many different combinations of these critical parameters that will achieve the necessary removal for a given cycle time. In this work the procedures were evaluated using a programmable lapping wheel and drive system. It was found that choosing appropriate successive grit sizes while minimizing down-force made it possible to reduce the total number of processing steps.

A third factor is the grit size for the exordium lapping phase. Best results were obtained when the number of steps following the planarization were minimized. As the sequence of steps increases, the flatness is severely degraded. The solution is to make the initial lapping step the only mechanical process to precede the rough polish and employ the smallest grit size that completely removes the saw damage. The advantage is that the rough polishing process can be initiated with a smaller nominal grit size again reducing the number of polishing steps required.

The choices of finish polishing processes are few and the efficiency of many of these methods is questionable. Initial attempts at chemical-mechanical processing show a slow, yet discernable improvement in surface roughness. However, little or no improvement in the sub-surface damage was detected. The best results were obtained with chemical polishing. The approach was essentially that of Jennings [3] with the exception that the etchant was 600°C KOH flux. For brief etch times (less than 3 minutes) the results proved acceptable. The advantage of the approach employed in this work is that the residual

damage layer (the sub-surface damage) is shallow. Measurements tend to be difficult at these levels, but the damage layer is less than 0.12 μm for the smallest grit size employed in the rough polishing step. It is clear that a chemical or chemical-mechanical process need not be perfect as long as it can remove approximately 0.12 μm of SiC in a reasonable period.

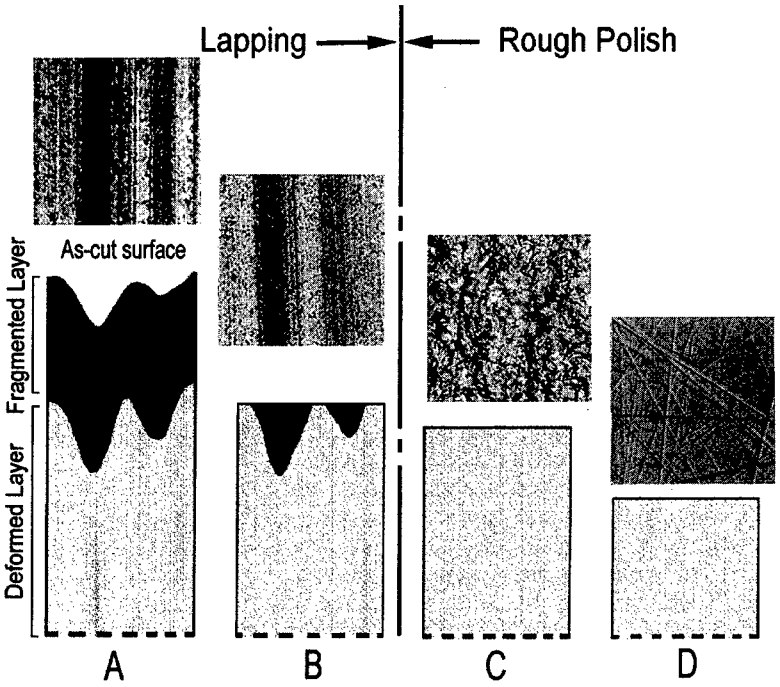


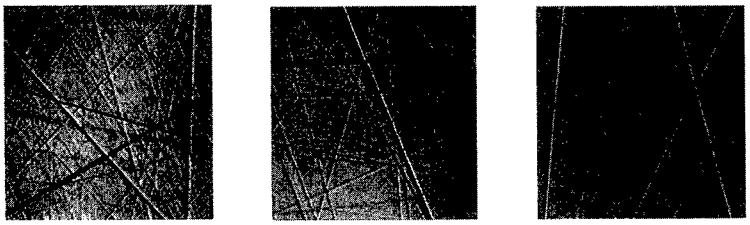
Figure II. Lapping is defined as the process that removes the post-sawing fragmented layer and rough polishing removes the deformed layer left by the sawing and lapping process. Rough-polishing also leaves residual damage that must be removed by finish-polishing or etching.

Results

Overall the time required to bring a SiC wafer from the as-cut state to rough polish was improved significantly by this work. Lapping has been reduced to a single step with machine time ranging from 6.0 to 16 minutes. The rough polishing process in the ideal case was reduced to three steps for a total machine time of 30 minutes. The chemical polish or etching time is very short compared to the mechanical processes and does not significantly affect the total process time. The machine time for a 32 mm diameter wafer with good as-cut quality is approximately 65 minutes. This time essentially doubles for a double-side polished wafer. These numbers do not include mounting, demounting, handling, and the logistics of preparing the machines. This "dead time" or "lag time" depends to an extent on the number of wafers being processed and the mount/demount methods employed. In this laboratory the typical "dead time" for a three to six wafer set

is approximately two hours. This extra 20 to 40 minutes per wafer extends the processing time to approximately three hours.

The quality of the surfaces obtained by this abbreviated approach appears to be comparable to those obtained by commercial suppliers of SiC wafers. The final surface is



Supplier A Supplier B USC

Figure III. A comparison of post rough-polish damage for a USC wafer as compared to the finished surface of some commercial wafers (500X). The surface quality is comparable.

specular with no visible scratches. The surface is flat, and in fact, it is flatter on the global level than many commercially available wafers. The residual subsurface damage appears to be comparable as well. Figure III illustrates the typical scratch density (500X) as seen after a mild molten salt etch of a rough polished surface, compared to some commercial wafer surfaces. The etchant is allowed sufficient time to highlight superficial damage such as scratches but insufficient time to reveal an appreciable number of bulk defects. It should be clear that the post rough polish surface of the USC wafer is similar to the finished surface from other sources.

Conclusion

This work demonstrates that the mechanical processing time necessary to produce a high quality, specular, SiC surface can be reduced substantially. The best approach is to limit the number of lapping (and rough polishing) steps by restricting the initial as-cut quality to a homogeneous, artifact-free surface typical of diamond wire sawing. The lapping process can be initiated with a smaller grit size and the resulting reduction in the depth of damage allows for fewer successive steps prior to the finish-polishing phase. Choosing a combination of final grit size, down-force, and polishing speed minimizes the residual damage and permits the use of slow finish-polishing processes that would not prove viable for deep damage layers. Etching studies have confirmed that the process described here yields results comparable to commercial wafers.

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Nuclear Transmutation Doping of Phosphorus into 6H-SiC

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Keywords: Annealing, Deep Level Analysis, Electrical Characteristics, Nuclear Transmutation Doping, Phosphorus, PL, RBS

Abstract: P-type 6H-SiC has been transmuted to n-type by neutron transmutation. Samples were irradiated by neutrons with the fluence of 10^{17}~10^{19}cm^{-2}, and were annealed at 1400~2000 ℃ for 30min in Ar. In LTPL spectra after 2000 ℃-annealing, free exciton peaks appeared, indicating that good lattice recovery was achieved. *I-V* and *C-V* measurements showed the transmutation from p-type 6H-SiC to n-type. In deep level analyses, there were two electron traps located at E_c–0.51eV and E_c–0.61eV.

1 Introduction

Nuclear transmutation doping (NTD) has been widely utilized in the Si power device field to realize the extremely homogeneous donor concentration in the n^- drift layers [1]. This technology is based on the capture of thermal neutrons by ^{30}Si through the reaction [^{30}Si$(n,\gamma)^{31}$Si], and the subsequent β^- decay forms active ^{31}P (phosphorus) donors. The reason why the extremely homogeneous donor concentration can be produced by this technology is that the neutron absorption cross section of Si is very small. As phosphorus acts as a shallow donor in SiC, the possibility of NTD for SiC has been reported [2]. In this paper, more successful and systematic investigation including effects of very high-temperature annealing and deep level analysis is presented. The feasibility and technological issues of NTD in SiC will be discussed.

2 Experiments

Samples used in this study were 14μm-thick p-type 6H-SiC epitaxial layers with an acceptor concentration of mid 10^{14}cm^{-3} grown on n-type substrates at the authors' group. Samples were irradiated by reactor-neutrons for 8, 24, or 50 hours (named as NTD-8h, NTD-24h, NTD-50h series respectively), in Kyoto University Reactor (KUR), to obtain three different doping concentrations, and were annealed in Ar at temperatures of 1400~2000°C for 30min. The annealing up to 1600 ℃ was carried out in a horizontal cold-wall CVD reactor, and the annealing from 1800 ℃ to 2000 ℃ was done in a sublimation system. Table 1 shows the fluence of neutrons and the resulting doping concentration of phosphorus estimated from the neutron fluence and capture cross section.

Before and after annealing, low-temperature photoluminescence (LTPL), Rutherford backscattering spectroscopy (RBS), *I-V*, *C-V* and deep level analysis were carried out. In electrical measurements, Ni was evaporated as surface Schottky contacts and Ag-paste was used for back side ohmic contacts.

Table 1 Fluences of neutrons and estimated doping concentrations of phosphorus.

Sample	Fluence of thermal neutrons	Fluence of epithermal neutrons (0.5eV~100keV)	Fluence of fast neutrons (> 100keV)	Estimated doping concentration of phosphorus
NTD-8h	$2.3 \times 10^{18}cm^{-2}$	$1.7 \times 10^{17}cm^{-2}$	$1.1 \times 10^{18}cm^{-2}$	$5.0 \times 10^{14}cm^{-3}$
NTD-24h	$7.0 \times 10^{18}cm^{-2}$	$5.1 \times 10^{17}cm^{-2}$	$3.4 \times 10^{18}cm^{-2}$	$1.5 \times 10^{15}cm^{-3}$
NTD-50h	$1.5 \times 10^{19}cm^{-2}$	$1.1 \times 10^{18}cm^{-2}$	$7.0 \times 10^{18}cm^{-2}$	$3.2 \times 10^{15}cm^{-3}$

3 Results and Discussion

Before annealing, RBS and *I-V* measurements were carried out. RBS channeling measurements of as-irradiated NTD-50h revealed that the as-irradiated material has a crystalline structure and not amorphous, in spite of the very high fast-neutron fluence. *I-V* measurements of as-irradiated samples showed an ohmic behavior with a very high resistivity over $10^{10}\Omega$cm, indicating a high density of point defects.

3.1 Low-temperature photoluminescence (LTPL)

Figure 1 shows the LTPL spectra of NTD-50h annealed at different temperatures. All the samples exhibited strong emissions due to vacancy-related "D_I center" as labeled L_1, L_2, and L_3. After annealing at 1600°C, interstitial-related "D_{II} defect" [3] peaks appeared at 420.3nm (2.950eV) and 420.6nm (2.948eV), but these defect emissions became very weak after annealing

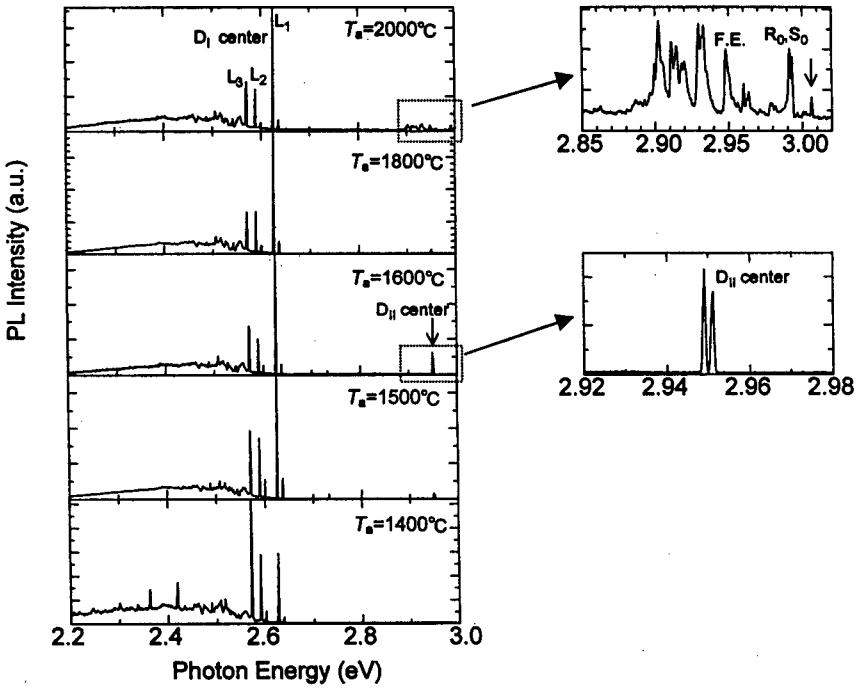

Fig. 1 Photoluminescence spectra at 18K of NTD-50h annealed at different temperatures.

at 1800°C. By increasing annealing temperature up to 2000°C, D_{II} lines disappeared and S_0, R_0 (neutral nitrogen donors bound exciton emission) and free exciton peaks emerged, which is the first observation of free exciton peaks (F.E.) in SiC doped by a neutron transmutation technique. In a previous report [2], the highest annealing temperature was 1850°C, resulting in no significant free exciton peaks observed. The present study suggests that good lattice recovery can be achieved by higher-temperature annealing at 2000°C. And in the LTPL spectra after 2000 ℃-annealing, a small peak (shown by an arrow) appeared at around 412.5nm (3.006eV). Because the energy level of this peak corresponds to that of a neutral phosphorus donor bound exciton emission in phosphorus doped CVD epilayers [5], phosphorus donors are thought to be formed by neutron transmutation.

3.2 *I-V* and *C-V* measurements

Figure 2 represents *C-V* characteristics of as-grown (virgin) and 2000°C-annealed NTD-50h, demonstrating successful conversion from p-type to n-type by NT doping. This conversion was also confirmed by *I-V* measurements. The net donor concentration for the NT-doped sample was determined to be $1.7\times10^{15}cm^{-3}$ with very good uniformity. Since the initial acceptors with a concentration of $8.4\times10^{14}cm^{-3}$ definitely exist as compensating impurities, the real donor concentration will be at least $2.54(1.7+0.84)\times10^{15}cm^{-3}$. This value is 80% of an expected value ($3.2\times10^{15}cm^{-3}$) shown in Table 1.

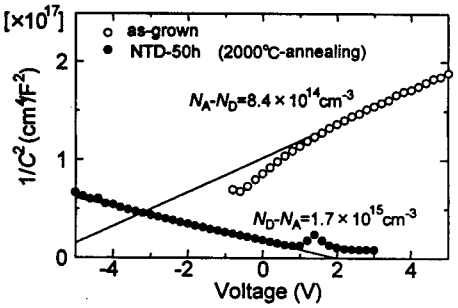

Fig. 2 *C-V* characteristics of as-grown and 2000℃-annealed NTD-50h.

Table 2 summarizes the results of *C-V* measurements. Firstly, for NTD-50h series, annealing at 2000°C yielded much higher donor concentration together with much lower resistivity than annealing at 1800°C. This result shows annealing at 2000 ℃ is very effective. Secondly, it is clear from the transmutation of 1600 ℃-annealed NTD-8h that a lower-temperature annealing process might be enough for samples irradiated with a smaller neutron fluence.

Table 2 Net donor concentrations estimated by *C-V* measurements.

	NTD-8h (cm^{-3})	NTD-24h (cm^{-3})	NTD-50h (cm^{-3})
2000 ℃	2.8×10^{14}(p)→ 4×10^{14}(p)	4.9×10^{14}(p)→ 1.3×10^{14}(n)	8.4×10^{14}(p)→ 1.7×10^{15}(n)
1800 ℃	—	high ρ	5.0×10^{14}(p)→ 1.3×10^{14}(n)
1600 ℃	2.8×10^{14}(p)→ 8×10^{13}(n)	high ρ	high ρ
1500 ℃	—	high ρ	high ρ
1400 ℃	high ρ	high ρ	high ρ

— : sample not available

3.3 Deep level analysis

Figure 3 shows the ICTS (Isothermal Capacitance Transient Spectroscopy) spectra obtained from 2000 ℃-annealed NTD-50h. There are two peaks in the ICTS spectra, and each peak is named as peak1 and 2. Figure 4 shows the Arrhenius plots of τT^2 vs. $1000/T$ for each peak. From Fig. 4, two electron traps are located at E_c–0.51eV and E_c–0.61eV. Because the deeper energy level is nearly equal to the energy level of "Z_1/Z_2 centers", this trap is believed to be the "Z_1/Z_2 centers", which originate from the same point defect as the D_I center [4]. It should be noted that the trap concentrations were estimated to be $1.0\times10^{14}cm^{-3}$ and $4.9\times10^{13}cm^{-3}$

for peak1 (shallow) and peak2 (deep) traps, respectively, being less than 10% of the donor concentration. In deep level analyses of 2000 ℃-annealed NTD-24h, an electron trap is located at E_c–0.61eV and its concentration was determined to be $2.0\times10^{12}cm^{-3}$. But the shallow trap (E_c–0.51eV) was not observed. It was found that this trap concentration of NTD-24h is much smaller than that of NTD-50h, indicating that the trap concentration increases as a neutron fluence is higher. This is the first deep level analysis of NT-doped SiC.

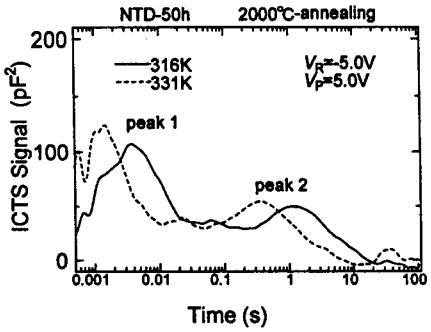

Fig. 3 ICTS spectra of 2000℃-annealed NTD-50h.

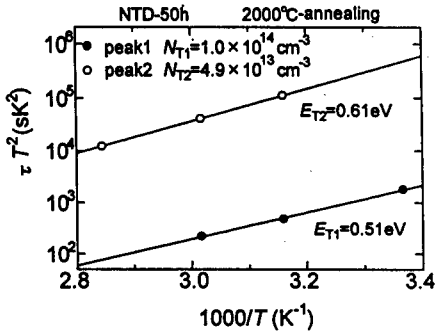

Fig. 4 Arrhenius plots of $\tau\ T^2$ as a function of $1000/T$ obtaind from two peaks.

4 Summary

Characteristics of 6H-SiC irradiated by neutrons were studied. After irradiation of neutrons, considerable damages were generated in samples, but samples have a crystalline structure and not amorphous. After 2000 ℃ annealing, PL spectra showed F.E. peaks and a phosphorus-related peak, indicating good lattice recovery. This is the first observation of free exciton peaks (F.E.) and a phosphorus-related peak in SiC doped by neutron transmutation. *I-V* and *C-V* measurements showed p-type 6H-SiC was transmuted to n-type. In deep level analyses of 2000 ℃-annealed NTD-50h, there were two electron traps located at E_c–0.51eV and E_c–0.61eV. The trap concentrations were $1.0\times10^{14}cm^{-3}$ and $4.9\times10^{13}cm^{-3}$ for shallow and deep traps. In 2000 ℃-annealed NTD-24h, there was one trap, being located at E_c–0.61eV, and its concentration was $2.0\times10^{12}cm^{-3}$. The shallow trap E_c–0.51eV was not observed for NTD-24h.

Acknowledgement

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Radiation Defects and Doping of SiC with Phosphorus by Nuclear Transmutation Doping (NTD)

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Keywords: C-V, Defect, Hall Effect, LTPL, Neutron, Phosphorus

Abstract

We irradiated 4H and 6H SiC samples with various neutron (further: N) fluences of different energetic distributions. Then the samples were sucessively annealed between 600°C and 1850°C and thereafter characterized by Fourier-Transform-Infra-Red-spectroscopy (FTIR), Low-Temperature-Photo-Luminescence (LTPL). Hall-effect, I-V, C-V characteristcs were carried out. It is shown that fast neutrons (FN) produce uppermost defects and samples irradiated with nearby thermal fluences show approximately the same behaviour after annealing at 1500-1650°C as "as-grown" samples. Whereas one has to consider the surface destruction due to annealing processes.

Introduction

Nuclear Transmutation Doping (NTD) is a standard technique in power device fabrication based on silicon [1, 2]. This technique is based on the reaction [$^{30}Si(n,\gamma)\ ^{31}Si \xrightarrow{\beta^-} {}^{31}P$] and thus it is basicly usuable to produce the phosphorous donor levels in SiC, as well. The Phosphorous doping of SiC is characterized after Ion Implantation (6H: [3]). First attempts applying NTD on SiC were made with respect to radiative environments [4]. In the last years it is introduced in SiC research as doping technique [5, 6, 7]. Unfortunuately the electrical characteristics of irradiated samples are heavily influenced by defects which are incorporated by NTD.

Experimental

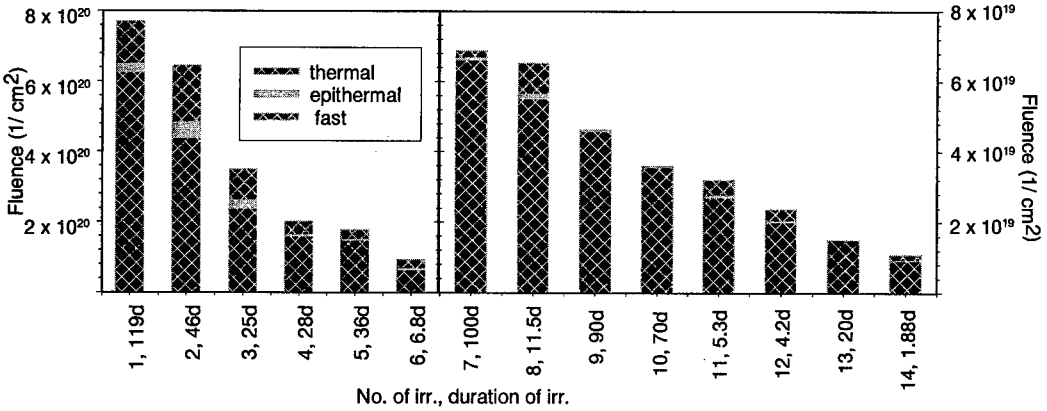
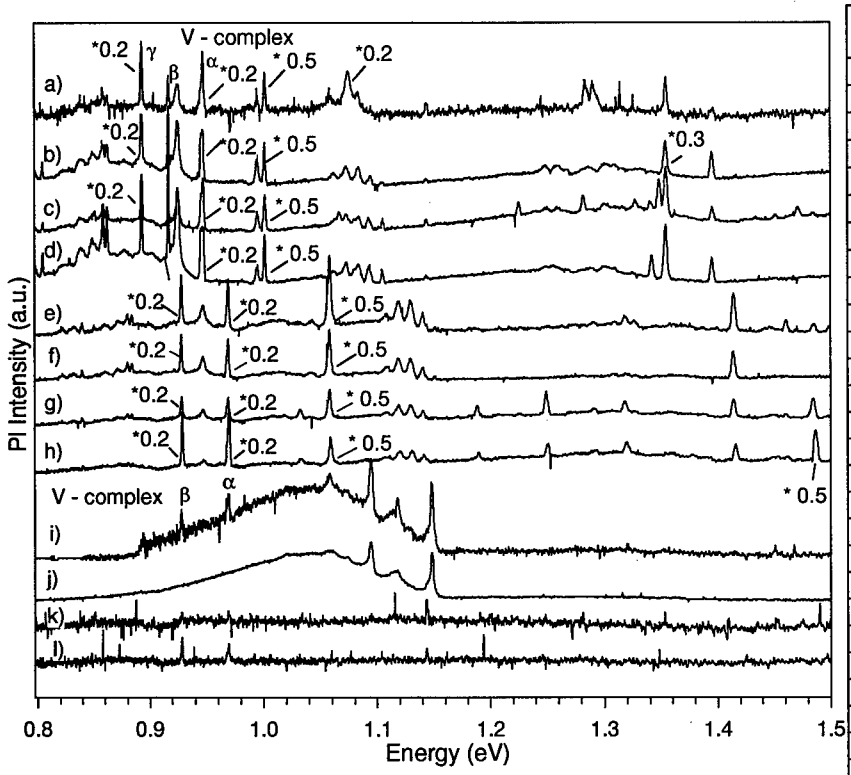


Fig. 1: The neutron fluences are divided in thermal, epithermal and fast parts of each irradiation together with the duration of each.

We irradiated different 4H and 6H epitaxial layers on Cree Substrates both p-type and n-type in different positions of several reactors with Ns of different energy distributions (Fig. 1).



No. of Line	Energy in eV
1	1.500
2	1.490
3	1.486
4	1.484
5	1.471
6	1.462
7	1.415
8	1.396
9	1.355
10	1.342
11	1.340
12	1.327
13	1.325
14	1.323
15	1.320
16	1.294
17	1.290
18	1.284
19	1.282
20	1.251
21	1.226
22	1.190
23	1.148
24	1.144
25	1.141
26	1.130
27	1.120
28	1.118
29	1.109
30	1.108
31	1.105
32	1.094
33	1.084
34	1.075
35	1.073
36	1.061
37	1.059
38	1.058
39	1.042
40	1.033
41	1.001
42	0.994

Fig. 2: on the left side PL spectra in the IR-region are shown: material: a) - d) - p-type 6H, e) - i) - p-type 4H, j) - l) - n-type 4H, c), g) - substrates, others are epilayers, d), f), l), - as-grown, irr. as Fig.1: a) - No. 3, b) - No. 4, c), g), h) - No. 7, e), i), j), k) - No. 13, annealing: h) - 1400°C, e), k) - 1500°C, c), d), f), g) - 1600°C, a), b) - 1700°C, i), j) as irr.. At the right side is a table of the PL-lines and their energies without the $V^{4+/3+}$ - emission and its local modes and phonon lines.

Then we characterized the samples after each ann. step (for detail of sample preparation see [7]). We measured LTPL (for apparative detail: [8]) with two lasers (SHG: second harmonic Ar-Ion laser at 257nm and a HeCd laser at 325nm) for excitation to get different excitation dephts. So one is able to decide whether the signal arises from substrates or from epilayers. The LTPL measurements in the IR region were carried out with the HeCd laser for excitation, a Spex 1681B monochromator and a liquid nitrogen cooled Ge-diode as detektor. FTIR-measurements were carried out with a Nicolet 740 and a Bruker IFS 66v/S spectrometer.

Results

It is for interest to find some global criteria for crystal quality. But most characterization techniques are not useable, or even more, not linear over several decades of defect densities. Therefore we measured the IR-reflection of all samples. The samples with high fluences of FNs applied (Fig. 1, Nos. 1-6) show a big influence of defect concentration on the oscillator damping of the "reststrah-

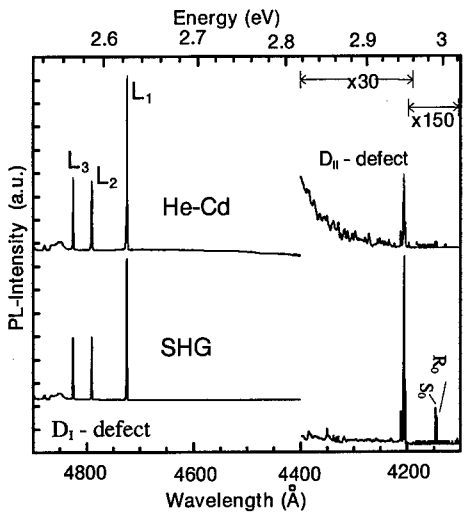


Fig. 3: LTPL of 6H SiC, irr. (Fig. 1, No. 7), ann. at 1600°C, excited with different sources.

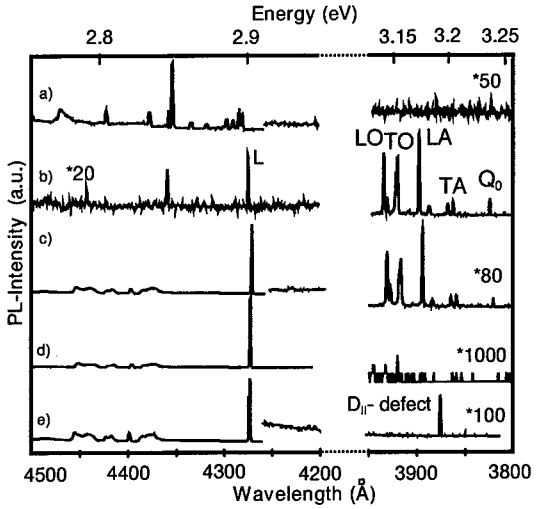


Fig. 4: LTPL-spectra of 4H SiC: a-c) n-type , irr. as Fig. 1, No. 13, a) as irr., b) as-grown, c) ann. at 1650°C; d, e) p-type: d) irr. as Fig. 1, No. 13 ann. at 1650°C, e) irr. as Fig. 1, No. 7, ann. at 1600°C

lenbande". Especially the coupling to the ω_L-frequency becomes weak. Further we carried out LTPL measurements. Here appear different lines and groups of lines depending on the fluences of FN. In the IR-region additional to the well known $V^{4+/3+}$ emission lines [9] various lines appear which are caused due to the NTD and subsequent annealing procedure (Fig. 2). It is conspicious that 4H p-type and n-type samples show quite different emission spectra after annealing, whereas after irradiation they look like twins (Fig. 2i, j). Further all generated lines are emitted from substrates as well, thus we can not present lines which arise from the produced n-type layers. Obvious a complex consisting of 5 lines exists in both 6H (1.05-1.15 eV) and 4H SiC (1.1-1.5 eV) at different energies.

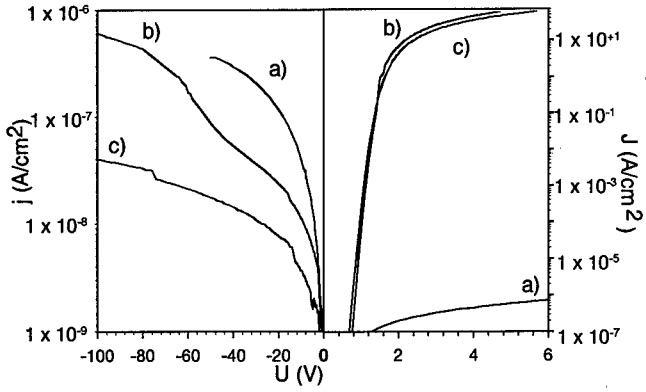


Fig. 5: I-V characteristics of 1mm Schottky contacts on n-type 4H SiC: a) irr. as Fig. 1, No. 13 and ann. at 1300°C, b) irr. as Fig. 1, No. 13 and ann. at 1500°C, c) as-grown

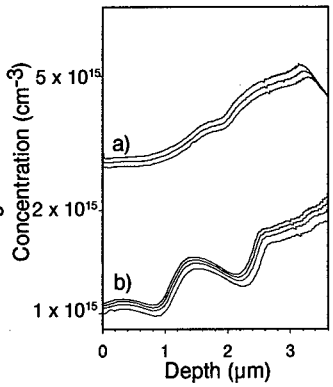


Fig. 6: Concentration-profile of C-V measurements at the contacts as Fig. 5, ann. at 1500°C: a) irr. as Fig. 1, No. 13, b) as-grown

Additional we inspected the visible region with LTPL. After the first irradiations (Fig. 1, Nos. 2, 3, 6) and annealing at approx. 1700°C we got typical emission spectra [7] consisting of D_I and D_{II} defect center [10, 11] as it is known from implanted samples. In Fig. 3 is shown that after irr. (Fig. 1, No. 7) emissions of the nitrogen exciton are visible and here LTPL emissions are detectable after

1000°C ann. whereas after irr. as Fig. 1, Nos. 1-6 these are detectable after 1400°C ann.. Directly after irr. as Fig. 1, No. 13 LTPL is detectable (Fig. 4b, after irr. with electrons: [12]) and this is independent of n-type or p-type. After annealing at 1500°C in n-type (Fig. 4c) the phonon lines ("as-grown": (Fig. 4b)) appear again, whereas in p-type material just the D_{II} defect center is vanished (Fig. 4d,e). We carried out Hall effect measurements after different annealing temperatures, doses (Fig. 1, Nos. 3-7) and energy distributions of N fluences on 4H and 6H SiC. Samples irr. as Fig. 1, Nos. 1-6 show a reduced Hall mobility at low temperatures even after an ann. step at 1700°C. Those samples irr. as Fig. 1, No. 7 show a Hall mobility which is like as-grown. Overall the evaluation of these Hall measurements is restricted in temperature range by the breakthrough of the pn–junctions and the unknown depth of pn-junctions. About 1.5 cm^2 samples of n-type epilayers on n-type 4H substrates were annealed sucessively and prepared with Schottky contacts to prove the ann. procedure. NTD is known to be the most homogeneous doping technique. Thus the depth profil becomes smooth with NTD (Fig. 6) and after annealing at 1300°C the contacts become a "Schottky-like" behaviour, but they become comparable to contacts on as-grown material after annealing at 1500°C (Fig. 5).

Conclusion

With optical and electrical characterization techniques we showed the annealing behaviour of 4H and 6H SiC samples irradiated with N fluences of different energy distributions. The variation of the part of FN by a factor of $9.4x10^4$ shows that even a fraction of 1% of FN dominates the defect generation. Whereas after a fraction of FN of approx. 10^{-4} the samples show almost as-grown behaviour. Most annealing processes destroy the surface of samples and at higher temperatures additional defects are generated. That means that doping with thermal neutrons as such is not expected to affect the device properties in any negative sense. The different annealing behaviour of p-type and n-type samples after similar characteristic as irr. is not necessarilly and only caused by changing fermi level by annealing. But it leads to the conclusion that the whole annealing behaviour varies with different polytypes and p-type or n-type.

Acknowledgement

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Materials Science Forum Vols. 338-342 (2000) pp. 857-860

Relationship between Donor Activation and Defect Annealing in 6H-SiC Hot-Implanted with Phosphorus Ions

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Keywords: Electron Concentration, Hot-Implantation, Positron Annihilation Spectroscopy, Vacancy-Type Defects

Abstract

Phosphorus (P) ion implantation into 6H-SiC at elevated temperatures and subsequent annealing up to 1700 °C has been performed. Relationship between the electrical activation of P atoms and the recovery of defective layers was investigated by Hall effect measurements and positron annihilation spectroscopy. Clustering of vacancy-type defects due to post-implantation annealing is suppressed by implantation at elevated temperatures. The implantation temperature dependence of the carrier concentration in the samples can be interpreted in terms of annealing behavior of residual defects.

1. Introduction

Ion implantation is considered as a key technology for the fabrication of electronic devices based on silicon carbide (SiC). For the electrical activation of implanted impurities, removal of defects by post-implantation annealing is required. Whereas implantation of high concentration of donors or acceptors is necessary to produce low resistivity regions in device structures, amorphous SiC layers subjected to such high dose implantation at room temperature (RT) are hardly recovered by post-implantation annealing[1]. In this case, hot-implantation is known to be effective to avoid amorphization of ion implanted SiC[2]. However, understanding of annealing behavior of defects in high dose implanted SiC is still poor. Recently the structure and annealing behavior of defects in ion implanted SiC have been investigated by positron annihilation spectroscopy (PAS) using slow positrons[1] because this technique is quite sensitive to vacancy-type defects even in thin layers like ion implanted regions.

In order to study the hot-implantation effects on annealing behavior of defects introduced in SiC by high dose implantation, we have performed PAS and Hall effect measurements for 6H-SiC samples implanted with phosphorus (P) at doses around 10^{15}/cm^2 at temperatures up to 1200°C. We discuss the correlation between the recovery of defective region and the electrical activation of implanted P atoms.

2. Experimental

For our PAS experiments, we used n-type 6H-SiC epilayers with a thickness of 4 μm and a net donor concentration of 3×10^{15}/cm^3 (Cree Research Inc.). These samples were implanted with 200 keV-P ions at a dose 1×10^{15}/cm^2 at temperatures between RT and 1200°C. For Hall effect investigations, p-type 6H-SiC epilayers with a thickness of 4 μm and a net acceptor concentration of 5×10^{15}/cm^3 (Cree Research Inc.) were used. In these samples, a four-fold implantation (80, 100, 150 and 200 keV) was conducted to create a box profile of P atoms with a mean concentration of 5×10^{19}/cm^3 and a depth of 0.25 μm. Before implantation, a screen oxide with a thickness of 30 nm was formed on the sample surface by pyrogenic oxidation at 1100 °C to avoid the degradation of the sample surface during hot-implantation. The screen oxide was removed using hydrofluoric acid after implantation. Post-implantation annealing was performed at temperatures up to 1700°C for 20

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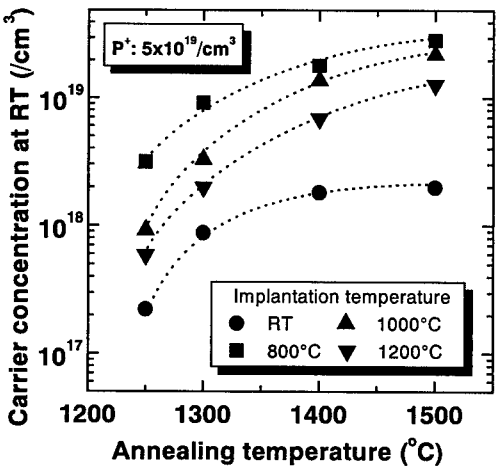

Fig. 1 Annealing temperature dependence of the carrier concentration at RT in 6H-SiC implanted with P^+ at RT, 800, 1000 and 1200 °C.

minutes in Ar atmosphere.

Hall effect measurements of the implanted and subsequently annealed samples were performed at RT using a van der Pauw arrangement[3]. Ohmic electrodes were formed on these samples by the evaporation of aluminum. In PAS experiments, positrons with energies up to 30 keV were implanted into the samples at RT. Energy spectra of annihilation gamma-rays were characterized by the line shape parameter S (S parameter), which was defined as the ratio of the integral of gamma-ray yield in the energy region 511±0.75 keV to the total yield. In this study, a computer code, VEPFIT[4] was used to solve the diffusion equation of positrons. In ion-implanted 6H-SiC samples, the positron sampling region was divided into three or four blocks to analyze the obtained S-E curves. The value of S in each block and at its boundaries were determined by fitting. The S value in the defect free region was fixed to be 0.457 (S_b = 0.457), which corresponds to the value obtained for un-implanted 6H-SiC. Details of the PAS measurement and analysis procedures have been reported in Ref. 1.

3. Results and Discussion

Figure 1 shows the carrier (electron) concentration at RT in the 6H-SiC samples implanted at $5x10^{19}$ /cm^3 at RT, 800°C, 1000°C, or 1200°C and subsequently annealed. The carrier concentration is shown to depend strongly on the implantation temperature. For the sample implanted at RT, the lowest carrier concentration is obtained. In this dose range, an amorphous layer is produced by implantation[2], and such a highly defective layer probably remains even after annealing at 1500°C, which causes poor activation of implanted P atoms. On the other hand, among the hot-implanted samples, the carrier concentration decreases with increasing implantation temperature in the investigated implantation temperature range. The highest concentration of carriers is obtained for the one implanted at 800 °C. This fact can be explained in terms of defects produced during hot-implantation and their annealing behavior, which is discussed later based on the PAS results.

Figure 2 (a) shows the depth profiles of S obtained for the 6H-SiC samples implanted at RT, 800 and 1200 °C. The S values in the shallow and deep defective regions are referred to as $S_{shallow}$ and S_{deep}, respectively, as shown in the figure. The positions of their boundaries are represented as "the interface between the shallow and the deep blocks ($D_{s/d}$)" and "the interface between the deep block and the defect free regions ($D_{d/f}$)". The values of $S_{shallow}$ and $D_{s/d}$ in the RT-implanted sample are estimated to be 0.51 and 180 nm, respectively. The critical energy density for amorphization of SiC due to RT-implantation was reported to be ≈ $2x10^{24}$ eV/cm^3[5]. The damage energy density deposited by P^+-implantation at $1x10^{15}$ /cm^2 in SiC is estimated using TRIM to be higher than $2x10^{24}$ eV/cm^3 in a depth below 200 nm. This depth is close to the value of $D_{s/d}$ obtained for RT-implantation. This result suggests that $D_{s/d}$ in the RT-implanted sample corresponds to the thickness of an amorphous layer (produced by the implantation), and that the obtained $S_{shallow}$ (= 0.51) corresponds to the S parameter for amorphous SiC. Uedono *et al.* reported that the mean size of the open space in an amorphous SiC is estimated to be equal to the size of 2-$V_{si}V_c$ (complex of two divacancies) or 3-$V_{si}V_c$[7]. Since the behavior of positrons in amorphous SiC is not yet fully understood, further investigations are necessary to clarify this point. As for the deep block, S_{deep}/S_b is estimated to be 1.065. For 6H-SiC implanted with 200keV-P^+ at $1x10^{13}$ /cm^2 at RT, the mean size of residual defects after implantation was reported to be $V_{si}V_c$ which exhibited S_{deep}/S_b = 1.062[7].

Thus, it is most probable that vacancy-type defects like $V_{Si}V_C$ are created in the deep block.

On the other hand, no amorphous layer is produced by hot-implantations above 800 °C. In fact, a suppression of amorphization of SiC due to hot-implantation at 400 °C has been reported[8]. The value of $S_{shallow}$ in the 1200 °C-implanted sample is larger than that in the 800 °C-implanted one. The result suggests that larger vacancy clusters are created as implantation temperature is raised. The positions of $D_{d/f}$ and $D_{s/d}$ shift toward the surface by hot-implantation at 800 °C or 1200 °C, which indicates that vacancies migrate toward the surface during hot-implantation. The recombination between vacancies and interstitials could also be an origin of the shift of the damage region. The values of S_{deep} for both the 800 °C- and 1200 °C-implanted samples are almost the same, and they are higher than that for the RT-implanted one. This suggests an increase of the mean size of vacancy clusters or an increase of the vacancy concentration due to the migration of vacancies.

Figure 2 (b) shows the depth profiles of S obtained for the 6H-SiC samples implanted at RT, 800 and 1200 °C after annealing at 1200 °C. Regarding 1200 °C-implantation, the result for as-implanted sample is shown in the figure. $S_{shallow}$ for the RT-implanted sample is much higher than that for the hot-implanted samples. Although the position of $D_{s/d}$ in the RT-implanted sample hardly changes by 1200 °C-annealing, that in the 800 °C-implanted one slightly shifts toward the surface. The value of $S_{shallow}$ for all samples increases, and the position of $D_{d/f}$ in all samples shifts toward the surface by the annealing. This result suggests that the recovery of defective layer occurs from the deep region although the heavily defective region near the surface hardly recovers.

With increasing annealing temperature, the position of $D_{d/f}$ shifts towards the surface, and as a result, the deep block disappears. Figure 2 (c) shows the depth profiles of S obtained for the 6H-SiC samples implanted at RT, 800 and 1200 °C after annealing at 1500 °C. The deep

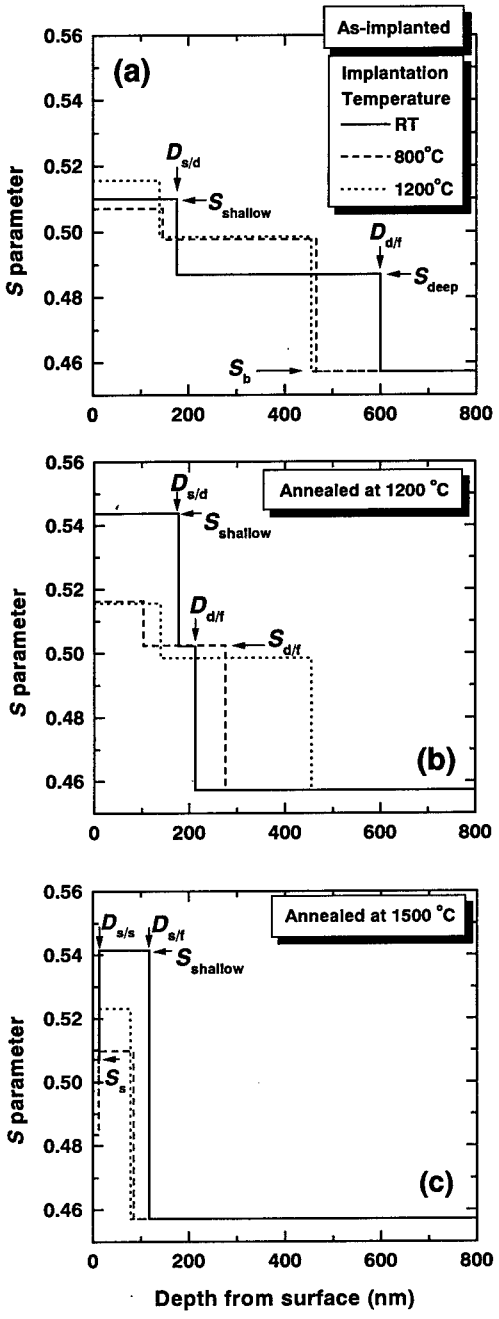

Fig. 2 Depth profiles of S parameter obtained by a fitting of S-E curves for 6H-SiC implanted with P^+ at RT, 800, and 1200 °C (a) before annealing and (b) after annealing at 1200 °C or (c) 1500 °C.

defective region disappears and only the shallow region remains after annealing at 1500 °C (the boundary is referred to as $D_{s/f}$ as shown in the figure). It was found from PAS observations that defects in 6H-SiC implanted with 200 keV-P^+ at $1x10^{13}$ /cm^2 are removed completely by annealing at 1400 °C[7]. Thus, the obtained result for $D_{d/f}$ can be interpreted in terms of the recovery of the deep block from the defect free region. The value of $S_{shallow}$ for the RT-implanted sample is much larger than those for the hot-implanted ones. This result suggests that in the RT-implanted sample larger size and/or higher concentration of vacancy clusters are produced after annealing at 1500 °C. Although the value of $S_{shallow}$ for the sample implanted at 800 °C and subsequently annealed at 1200 °C is almost the same as that for the 1200 °C-implanted one, $S_{shallow}$ for the 1200 °C-implanted one becomes larger than that for the 800 °C-implanted one by annealing at 1500 °C. This suggests that an increase of the mean size of vacancy clusters or/and an increase of the vacancy concentration occurs in the 1200 °C-implanted sample. When the concentration of remaining defects is reduced, the carrier concentration might increase. Vacancy clusters probably incorporate with P atoms. As a result, the carrier concentration might decrease by an increase of the size of vacancy clusters. Thus, the implantation temperature dependence of the carrier concentration in 6H-SiC implanted with high dose P ions can be interpreted in terms of the annealing behavior of residual defects. Further investigations are necessary to clarify the interactions which occur during the annealing between implantation-induced defects and implanted P atoms. For all samples, $D_{s/f}$ still remains around 100 nm from the surface after annealing at 1700 °C although the value of $S_{shallow}$ becomes small. After annealing above 1400 °C, an additional block near the surface ($D_{s/s} \approx 30$ nm) appears and the S value in this block (S_s) is smaller than $S_{shallow}$. Since a change in the S value near the surface was also observed for un-implanted samples after annealing at 1400 °C, this block is thought not to be caused by defects introduced by implantation.

4. Conclusion

Phosphorus ion implantation into 6H-SiC at RT, 800, 1000 and 1200 °C, and subsequent thermal annealing up to 1700 °C were performed to investigate the correlation between the recovery of defective layers and the electrical activation of implanted P atoms. The carrier concentration in the hot-implanted samples is larger than that in the RT-implanted one. The annealing behavior of vacancy-type defects in implanted SiC depends strongly on the implantation temperature. The implantation temperature dependence of the carrier concentration in the samples can be interpreted in terms of annealing behavior of residual defects.

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Hot-Implantation of Phosphorus Ions into 4H-SiC

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Keywords: 4H-SiC, AFM, Hall Effect Measurement, Hot-Implantation, Phosphorus, SIMS

Abstract Ion implantation of phosphorus (P) into 4H-SiC at room temperature and 500°C was investigated. The P profiles simulated with a TRIM (transport of ions in matter) program showed good agreement with experimental results. The sheet resistance (R_S) of implanted layers at both temperatures decreased with increases in the annealing temperature between 1200°C and 1600°C. Also, in the case of the implanted layer at 500°C, a low sheet resistance of 71 Ω/□ was obtained by annealing at 1600°C. Hot-implantation was found to greatly improve the carrier concentration obtained by Hall-effect measurements.

In the case of annealing at 1700°C, the R_S of implanted layers at both temperatures increased sharply. From AFM analysis, it is thought that the increase in R_S is due to the sublimation or evaporation of SiC from the surface of the implanted layer.

1. Introduction

Silicon carbide (SiC) is expected to be a promising material for hard-electronics, owing to its outstanding properties such as wide bandgap, high breakdown field, and high thermal conductivity [1]. In such excellent material, however, for selective doping in device fabrication, ion implantation has been shown to be the only possible means, because the dopant diffusion coefficient in SiC is extremely small even at high temperatures (<1800°C), making diffusion processes very difficult. Hot-implantation has been demonstrated to be effective in reducing implantation-induced damage and in improving electrical activation of implanted ions in SiC [2]. In particular, for n-type doping, P hot-implantation is very notable, because P atoms act as a shallow donor in SiC [3-5].

In this study, we performed hot and high-dose implantation of P ions into 4H-SiC. The electrical characteristics of implanted layers were investigated by Hall-effect measurements. The implanted layers were also characterized by secondary-ion mass spectroscopy (SIMS) and atomic force microscopy (AFM). We discuss the effects of hot and high-dose implantation on the electrical characteristics of implanted layers in connection with surface morphology after activation annealing.

2. Experiments

The phosphorus implantations were performed on commercial (0001) ,Si face ,Al-doped p-epilayers on p^+ 4H-SiC wafers (Cree Research Inc). The nominal thickness and the doping of the p-epilayers were 10 μ m and 5.0 x 10^{15} cm^{-3}, respectively. In the present study, six-fold implantation of phosphorus ions was carried out through a 10 nm oxide layer in order to obtain box profiles. The implant energies and dosages were 250, 200, 150, 100, 70, 40 keV and 2 x 10^{15}, 2 x 10^{15}, 1 x 10^{15}, 1x10^{15}, 5x10^{14}, 5x$10^{14}$$cm^{-2}$, respectively, and samples were kept at room temperature (RT) or an elevated temperature of 500°C, during implantation. For hot-implantation, the samples were set on a resistively heated Ta holder. The typical ion current density was 0.1 to 1 μ A/cm^2. The total

implanted dose was fixed at 7 x 10^{15} cm^{-2}. Post-implantation annealing was carried out in Ar ambient conditions at temperatures between 1200 and 1700°C for 30 min.

The impurity profiles were analyzed by secondary ion mass spectroscopy (SIMS). The electrical properties of the implanted layers were characterized by Hall-effect measurements using the van der Pauw configuration. For ohmic contacts, Ni was evaporated on the surface through a metal mask followed by annealing at 1000°C in Ar. Atomic force microscopy (AFM) was also performed on the samples implanted at RT and 500°C, to evaluate the surface morphology of the material.

1. Results and discussion

Fig.1 shows the P depth profiles for samples as-implanted at 500°C.The implantation was carried out into the surface of the sample with a 7-degree tilt angle between the ion beam direction and c-axis (the <0001> direction). The open squares denote the results obtained by SIMS measurements. On the other hand, the open circles show profiles calculated using a Monte Carlo simulation. Here, the Monte Carlo simulation was performed using a TRIM (transport of ions in matter) program. In the TRIM program, the energy dependence of stopping powers for each element is given as the data base, and the main fitting parameter is the density of SiC. In this study, the value of 3.21 g/cm^3 was employed. The P concentration of box profiles obtained experimentally was about 2 x 10^{20} cm^{-3}.

A Monte Carlo simulation is a powerful technique, which provides more accurate results of the profile calculation. In fact, the simulated profile shows very good agreement with the experimental results, as shown in Fig.1. Some deviation was observed between the simulated and experimental results in the tail region, which may be caused by the channeling of implanted ions, and is difficult to suppress completely in ion implantation into single crystals.

Fig.2 shows the annealing temperature dependence of the sheet resistance (R_S) for the implanted samples at RT and 500°C. The R_S decreases with increasing annealing temperature from 1200°C to 1600°C.

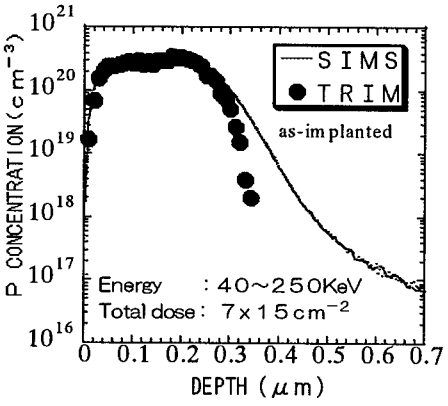


Fig.1 P depth profiles for samples implanted at 500°C at a dose of 7 x 10^{15} cm^{-2}. Open circles denote the results obtained by SIMS. The solid curves show profiles calculated using a TRIM program.

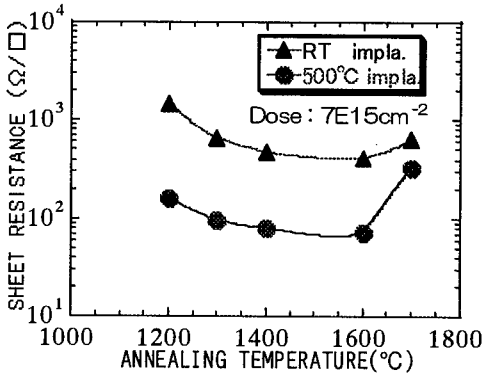


Fig.2. Annealing temperature dependence of sheet resistance of P^+ implanted 4H-SiC layers. P^+ implantation was performed at RT and 500°C with a 7 x 10^{15} cm^{-2} dose.

In the case of 500°C ion-implantation and annealing at 1600°C, an R_S as low as 71 Ω/□ was obtained, which is approximately one-sixth of that of the RT ion-implantation. In addition, it is about one-eighth of that of the nitrogen hot-implantation [7]. On the other hand, the R_S increased with annealing at 1700°C. Therefore, in order to investigate the R_S in more detail, the annealing-temperature dependence of the sheet carrier concentration (Ns), and the mobility (μ) of samples implanted at RT and 500°C, which were obtained by Hall-effect measurements, are shown in Fig.3 and Fig.4. It is clear in the comparison of both Ns results that hot implantation has an advantage over RT implantation for the entire annealing temperature. It was found that the R_S decrease in hot-implantation is mainly due to the Ns improving with increases in the annealing temperature. In the case of annealing at 1700°C, the Ns of both implanted temperatures decreased sharply. On the other hand, the μ of both increased rapidly between 1200°C and 1300°C, shifted almost uniformly between 1300°C and 1600°C, and increased significantly at 1700°C. Here, the reason why the the μ of both implanted temperatures improved rapidly at temperatures higher than 1300°C can be allied to the fact that a kind of vacancy defect vanishes beyond temperatures around 1300°C in 6H-SiC [8].

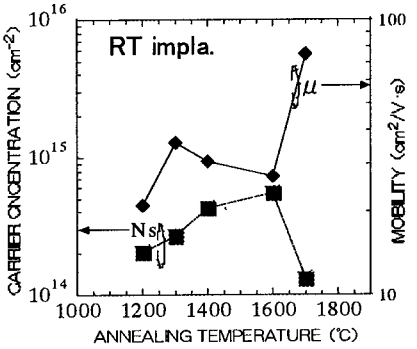


Fig.3. Annealing temperature dependence of sheet carrier concentration and mobility of P^+ implanted 4H-SiC layers. P^+ implantation was performed at RT with a 7 x 10^{15} cm^{-2} dose.

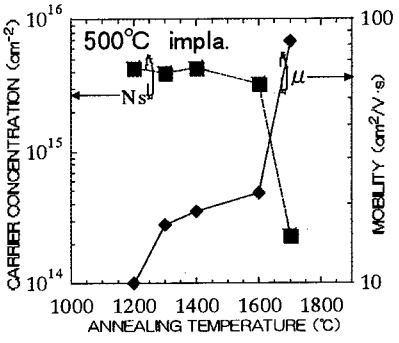
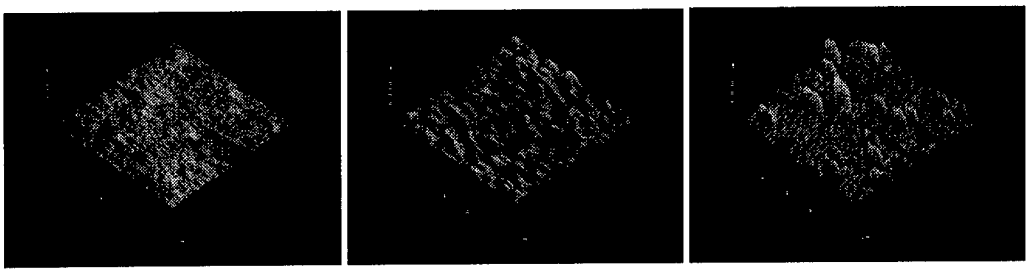


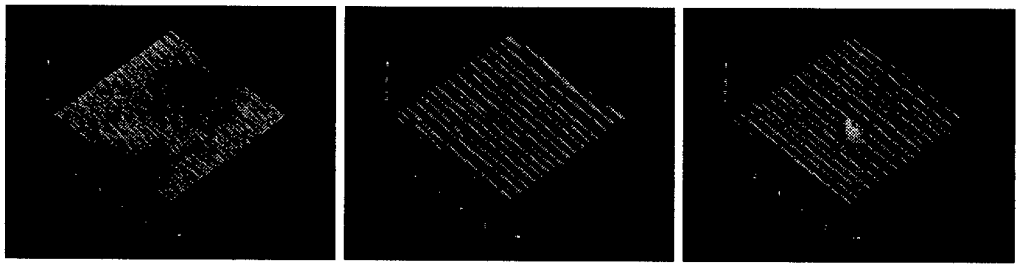
Fig.4. Annealing temperature dependence of sheet carrier concentration and mobility of P^+ implanted 4H-SiC layers. P^+ implantation was performed at 500°C with a 7 x 10^{15} cm^{-2} dose.

Fig.5 and Fig.6 show the surface morphologies of samples implanted at RT and 500°C. For both figures, (a), (b), and (c) show the 10 x 10 μ m ^{2} AFM images of samples with annealing at 1400°C, 1600°C, and 1700°C, respectively. The R_a is the average surface roughness calculated from an observed area of



(a) R_a=1.10 nm (b) R_a=12.1 nm (c) R_a=33.9 nm

Fig.5. 10 x 10 μ m^2 AFM images of P implanted SiC at RT annealed at (a) 1400°C, (b) 1600°C and (c) 1700°C.



(a) R_a=1.51 nm (b) R_a=13.8 nm (c) R_a=14.1 nm

Fig.6. 10 x 10 μ m^2 AFM images of P implanted SiC at 500°C annealed at (a) 1400°C, (b) 1600°C and (c) 1700°C.

10 μ m squares. In both samples implanted at RT and 500°C, the R_a increased with elevation of the annealing temperature. In the case of samples implanted at RT, followed by annealing at 1700°C, the R_a is extremely large, with a value of approximately 34 nm. On the other hand, the R_a of hot-implantation followed by annealing at 1700 °C is sufficiently smaller than those of the RT-implantation. From these AFM analyses, it is thought that the increase in R_S in Fig.2 is due to the sublimation or evaporation of SiC from the surface of the implanted layers, which can be suppressed by hot-implantation. In order to use hot-implantation for device fabrications, further investigations are necessary with regard to surface roughness .

4. Summary

Ion implantation of P ions into 4H-SiC at room temperature and 500°C was investigated. The P profiles simulated with a TRIM program showed good agreement with experimental results. The R_S of implanted layers at both temperatures decreased with increases in the annealing temperature from 1200°C to 1600°C, and in the case of the implanted layer at 500°C, an R_S as low as 71 Ω/□ was obtained by annealing at 1600°C. Hot-implantation was found to improve the carrier concentration by using Hall-effect measurement. From a series of AFM analyses, it is thought that the increase in R_S caused by annealing at 1700°C is due to the sublimation or evaporation of SiC from the surface of the implanted layer, which can be suppressed by hot-implantation. On the basis of the technology reported in this study, phosphorus should become a promising candidate as an n-type dopant in SiC.

Acknowledgements

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Electrical Characteristics and Surface Morphology for Arsenic Ion-Implanted 4H-SiC at High Temperature

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Keywords: Arsenic, Depth Profile, High Temperature Ion-Implantation, Surface Morphology

Abstract: High temperature ion-implantation of arsenic (As^+) into the 4H-silicon carbide (SiC) substrates with high dose of 7×10^{15} cm^{-2} has been investigated as an effective doping technique of n-type dopant for SiC power electron devices fabrication. The R_s as low as 213 Ω/□ is achieved in the sample implanted at 500 °C and annealed at 1600 °C. AFM and SIMS results reveal that the surface roughness of implanted SiC increases with the increasing of post-annealing temperature. This result suggests that the evaporation of Si atoms and As^+ dopants from SiC surface decreases the thickness of As^+ implanted layer and makes effect on R_s of the sample annealed at higher temperature.

1. Introduction

Silicon carbide (SiC) has a potential to yield new devices with functional capabilities that far exceed those based on silicon semiconductor. In order to develop SiC devices such as metal-oxide-semiconductor field-effect transistors (MOSFETs), ion-implantation has been expected as a selective doping technique because the diffusion coefficients for most dopants in SiC are negligible, at temperature below 1800 °C. In particular, ion-implantation at high temperature, which heats up the SiC substrates to high temperature (≧500 °C) during ion-implantation, is very effective method to improve the electrical activation rate of dopants implanted into SiC and to reduce the implantation-induced damage [1]. It was reported that the sheet resistances (R_s) of nitrogen (N^+) and phosphorus (P^+) implanted SiC substrates by high temperature ion-implantation at 500 °C were 546 Ω/□ and 160 Ω/□, respectively [2], [3]. Arsenic is well known as one of n-type dopants in Si device technology, although there are not sufficient reports about arsenic (As^+) ion-implantation into SiC. M.V.Rao et al. reported that the R_s of As^+ implanted SiC with 1.16×10^{14} cm^{-2} dose was 4.1 kΩ/□, which was too high for low on-resistance of power MOSFETs [4].

In this paper, As^+ ion-implantation with high dose at high temperature for the 4H-SiC substrates has been investigated as an effective doping technique for source/drain regions of SiC-MOSFET. Hall effect measurement with van-der Pauw pattern has been carried out. Variations of surface morphology and dopant depth profile caused by high temperature post-annealing have been observed using the atomic force microscopy (AFM) and the secondary ion mass spectroscopy (SIMS), respectively.

2. Experimental procedures

In this study, 4H-SiC(0001) substrates with 8 ° off-angle and a p-type epitaxial layer of Cree Research were used. The effective carrier density of Al in the epitaxial layer was 5×10^{15} cm^{-3}. After the standard RCA cleaning, 10 nm thick oxide films were grown at 1200 °C in dry O_2. Multiple implantations of As^+ and N^+ were carried out through the oxide film at various temperatures in order to form box-shaped profiles with depth of 0.3 μm. The total As^+ and N^+ doses were 7×10^{15} cm^{-2}. The post-annealing was performed in Ar atmosphere at the temperature range between 1200 °C and 1700 °C for 30 min. For measurement of electrical properties using the van-der Pauw pattern, Ni electrodes were formed on the SiC surface by electron beam evaporation and then annealed at 1000 °C for 5 min in order to form the ohmic contact. The surface morphologies of As^+ implanted SiC substrates were observed by AFM and the As^+ dopant depth profiles were measured by SIMS using 14.5 keV Cs^+ primary beam.

3. Results and Discussion

Figure 1 shows that post-annealing temperature dependence of R_s for the samples implanted at various temperatures. The R_s of As^+ implanted samples decreases with the increase of post-annealing temperature from 1200 °C to 1600 °C. The R_s of As^+ implanted samples at temperature ≧ 500 °C is approximately the one order smaller than that of the implanted one at R.T. The R_s as low as 213 Ω/□ is achieved by the 500 °C ion-implantation and 1600 °C post-annealing and is smaller than that of N^+ ion-implantation. A decrease of R_s from R.T. to 500 °C ion-implantation with As^+ dopants is larger than that of N^+ ion-implantation. On the other hand, the R_s of sample annealed at 1700 °C is lager than that of annealed one at 1600 °C. It was reported that the decrease of a sheet carrier concentration with increase of post-annealing temperature was due to out-diffusion of As^+ dopants during post-annealing [4]. It is considered that the dependence of post-annealing temperature on R_s is attributed to the variations of As^+ implanted layer during post-annealing. Thus, the variations of surface morphology of As^+ implanted SiC and of As^+ dopant depth profile were observed using AFM and SIMS, respectively.

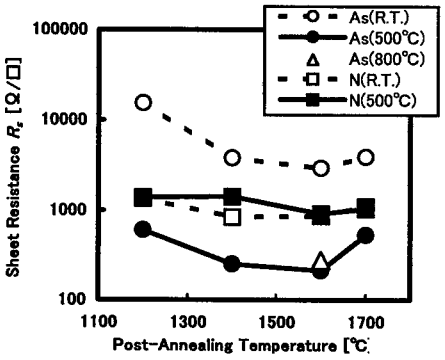

Fig.1 Dependence of the sheet resistances for As^+ and N^+ implanted SiC on post-annealing temperature.

AFM images reveal that the surface morphologies of as-implanted samples at R.T. and 500 °C are very flat and are nearly equal to those of SiC substrates without ion-implantation. However, the surface morphologies become gradually rough as the post-annealing temperature increases. AFM images of As^+ implanted samples at R.T. and 500 °C followed by 1700 °C post-annealing are shown in Fig. 2 (a) and (b), respectively. The AFM images of 10 μm^2 surface area were observed. After post-annealing, R.T. implanted sample has a number of peak-like structures on SiC surface, while surface morphology of sample implanted at 500 °C shows long groove structures running one direction. Both different structures become larger with the increase of the post-annealing temperature. Figure 3 indicates the effect of post-annealing temperature on

the average roughness (R_a) calculated from 10 μm^2 AFM observation area for As^+ implanted SiC. The R_a values increase above 1400 °C post-annealing temperature. The largest increase of R_a is at post-annealing temperature range between 1600 °C and 1700 °C. These structures, as shown in Fig. 2, would be formed by the desorption of Si containing species such as Si, SiC_2 and Si_2C due to the sublimation of SiC surface during high temperature annealing [5]. In general, it is known that the melting point of Si is 1412 °C. The evaporation of Si atoms from the SiC surface could occur around 1400 °C post-annealing. Since the sublimation point of As and melting point of SiAs known as 614 °C and 1113 °C, are much smaller than the melting point of Si. Thus the evaporation of As^+ dopants also may occur during high temperature post-annealing. As a result, the increase of R_s for the samples annealed at 1700 °C is caused by the decrease of As^+ implanted layer thickness because of the excess evaporation of Si atoms and As^+ dopants from the SiC surface during post-annealing. Figure 4 shows As^+ dopant depth profiles of as-implanted samples at (a) 500 °C and (b) R.T. and of samples implanted at (c) 500 °C and (d) R.T. followed by 1600 °C post-annealing using SIMS measurement. The As^+ dopant depth profiles for as-implanted samples, as shown in Fig. 4 (a) and (b), are almost consistent with TRIM simulation. By the post-annealing of 1600 °C, As^+ dopant depth profile of Fig 4 (c) shows a little shift to the surface as compared with Fig. 4 (a). This means that As concentration near the SiC surface of annealed sample is larger than that of the as-implanted sample due to the evaporation of SiC surface layer. As a result, the R_s of the sample implanted at 500 °C and annealed at 1600 °C decreases to 213 Ω/□. On the other hand, it is observed the decreases of As concentration and doping layer thickness in Fig. 4 (d). Furthermore,

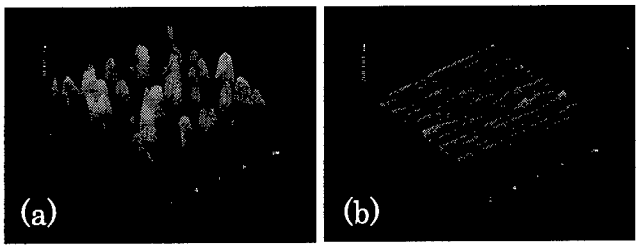

Fig.2 Surface morphologies of (a) R.T. and (b) 500 °C implanted SiC after post-annealing at 1700 °C. z-axis length of image corresponds to 100 nm/div.

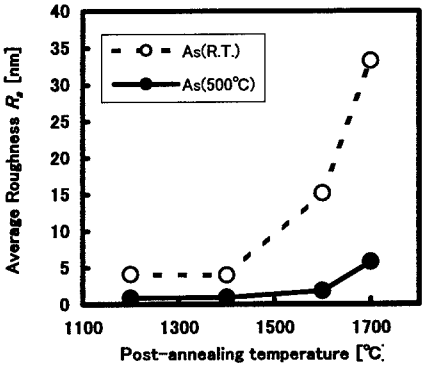

Fig.3 Post-annealing temperature dependence of average roughness (R_a) for As^+ implanted SiC. The R_a was calculated from 10mm□ AFM observation area.

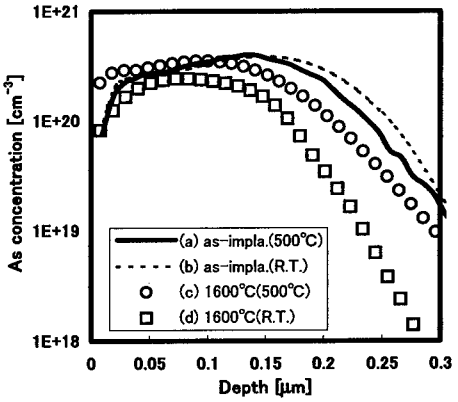

Fig.4 As+ dopant depth profiles of SiC implanted at 500 °C and R.T. without annealing and after annealing of 1600 °C.

comparing Fig. 4 (c) and (d), As concentration near the SiC surface for the sample implanted at R.T. is much smaller than that of the sample implanted at 500 °C. The R_s of the sample implanted at R.T. becomes much larger than that of sample implanted at 500 °C. These different As^+ dopant depth profiles by post-annealing may be caused by the different crystalline of as-implanted layer. M.V.Rao et al. also reported that amorphization of SiC substrates was inhibited by ion-implantation temperature above 500 °C in order to decrease the lattice damage during ion-implantation, especially for high doses [6]. Thus, for the samples implanted at R.T., the evaporation of Si atoms and As^+ dopnants from SiC surface and the out-diffusion of As^+ dopants during post-annealing decrease the implanted depth profile, as a result the R_s becomes larger than that of implanted sample at 500 °C. In addition, this crystalline difference of as-implanted samples results in different surface morphologies of samples by post-annealing, that is, the formation of the peak-like structure for R.T. implantation and the long groove structure for 500 °C implantation. These results indicate that high-temperature ($\geqq$ 500 °C) ion-implantation technique is effective method to improve the electrical properties and surface morphologies of As^+ implanted SiC samples.

4. Conclusion

The As^+ ion-implantation at high temperature with high total dose of 7×10^{15} cm^{-2} into the 4H-SiC substrates has been proved to be an effective doping technique of n-type dopant for SiC devices. The As^+ ion-implantation using 500 °C ion-implantation and 1600 °C post-annealing for 30 min. can achieve R_s as low as 213 $\Omega/\square$. It is observed using AFM and SIMS that the surface roughness occurs due to the evaporation of Si atoms and As^+ dopants from the SiC surface during post-annealing and becomes large with the increase of post-annealing temperature. The depth profile of As^+ dopants for the sample implanted at 500 °C is maintained after post-annealing of 1600 °C, while for R.T. implanted sample the maximum concentration of As decreases due to the out-diffusion of As^+ dopants near the SiC surface during post-annealing. The further decrease of R_s is expected by optimization of ion-implantation and post-annealing conditions such as implantation temperature, post-annealing time and the total dose of dopants.

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Damage Evolution in Al-implanted 4H SiC

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Keywords: Annealing, Channeling, Defect Kinetics, Dose Dependence, Implantation Temperature, RBS, Self-Interstitial, TEM, Vacancy

Abstract The build-up of damage in 4H SiC epitaxial layers implanted with 100 or 180 keV Al ions in the dose range of 10^{13} to 10^{15} cm^{-2} has been studied by transmission electron microscopy (TEM) and Rutherford backscattering spectroscopy in the channeling mode (c-RBS). Implantations have been done at temperatures between room temperature and 800 °C and the samples have been analysed after implantation and after post implant anneals. In as implanted samples channeling results show that a major part of the damage can be avoided already at implantations at 200 °C, but complete removal of damage is not possible even at an implantation temperature of 800 °C. After post implant annealing at typically 1600 °C a distribution of planar faults are seen by TEM. The size is around 10 nm, but increases with increasing annealing temperature.

1. Introduction

For a successful implementation of implantation doping technique in SiC device fabrication it is important to minimize the damage created during the implantation and to optimize the high temperature post implant annealing process to ensure high electrical activation of dopants and removal of residual damage. Several implanted p^+n- and n^+p junctions have already been demonstrated[1-3], but particularly for acceptor dopants the results have been far from ideal. Manufactured diodes often show high leakage currents and premature breakdown under reverse bias and poor and uneven injection during forward bias. These problems are often caused by point defects or larger agglomerates of point defects formed by the implantation process or during the post implant anneal.

Today the implantation and annealing processes in SiC are to a large extent optimized by trial and error since the knowledge of defect kinetics is very limited. Very few of the basic vacancy and interstitial type of point defects created during ion bombardment have been identified and even less is known about their migration and formation energies. This study is done in order to examine how isolated point defects accumulate and damage builds up in the SiC material as the implantation proceeds. We also study the defect kinetics during the post-implant anneal, when the lattice is restored and dopants are positioned at substitutional sites. Ion implantation has been a great success for Si technology and a thourough knowledge of damage build-up and annealing in this material has accumulated over the years. It is therefore useful to make reference to this well documented material when we investigate similar processes in SiC.

Several studies have been conducted during the last years where implantation induced damage build-up in SiC have been monitored by in particular Rutherford backscattering in the channeling mode (c-RBS)[4-6], but also transmission electron microscopy (TEM)[4,5,8,9]. However, most of these investigations have used the 6H polytype and include doses well above amorphization threshold. More important, multiple implantations have been used and ion flux (cm^{-2} s^{-1}) has not been treated systematically. Here we bombard 4H thick, low doped epitaxial layers with lower doses of single energy Al. Furthermore, the flux is kept constant in this investigation, while the implantation temperatures is varied. For the analysis we have also used c-RBS as well as TEM.

2. Experiment

Epitaxial layers, over 10 μm thick, doped with nitrogen in the low 10^{15} cm^{-3} range were grown on 4H n-type Cree substrates at Linköping University[10]. The samples were implanted with Al ions of 100 or 180 keV energy, doses ranging from 10^{13} to 10^{15} cm^{-2}, and at implantation temperatures from room temperature up to 800 °C. The Al flux was kept at 4×10^{11} cm^{-2} s^{-1} during all implantations. Some of the samples were also annealed after the implantation at temperatures from 750 to 2000 °C and for annealing times between 15 minutes and 16 hours. Rutherford backscattering spectroscopy in the channeling mode (c-RBS) and transmission electron microscopy (TEM) were performed on as-implanted samples and after subsequent anneals. Channeling-RBS was done with 2.4 MeV He ions at the Uppsala EN tandem accelerator and TEM was done using a Philips CM 20 UT, equipped with a LaB_6 filament operated at 200 kV. TEM samples were prepared by mechanical grinding and Ar-ion milling with a 4° angle of incidence.

3. Results and Discussion

A full cascade TRIM simulation of a 180 keV Al ion implantation in SiC is shown in Fig. 1 together with the total vacancy distributions for a dose of 6.5×10^{14} cm^{-2}. The vacancy profile peaks at slightly shallower depth compared to the implanted ions since the maximum of the elastic energy deposition occurs at an energy of 10 keV, before the Al ions come to rest. According to the simulation, each Al ion generates on the average 1280 vacancy-interstitial pairs. The TRIM projected range is around 220 nm, which for this ion and energy agrees well with the range measured by SIMS.

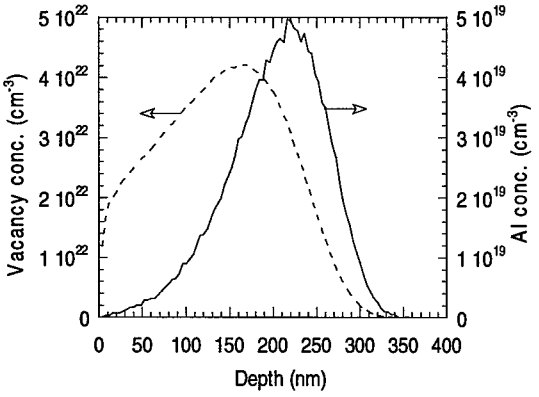

Fig. 1. TRIM simulations of 180 keV Al, 6.5×10^{14} cm^{-2}, implantation of SiC.

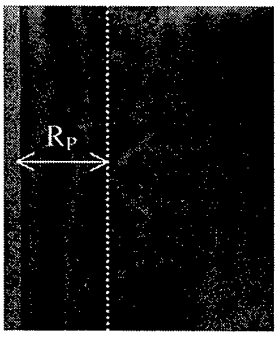

Fig.2. TEM cross section SiC implanted by 180 keV Al, 6.5×10^{14} cm^{-2}, at 700 °C, and annealed at 1700 °C for 30 minutes. Projected range, R_p=220, nm is indicated.

Figure 2 is a TEM cross section, viewed in the <11$\bar{2}$0> direction, of a sample subjected to the same dose and energy of Al ions. The implantation temperature is 700 °C and the sample is annealed at 1700 °C for 30 minutes. Without anneal no sharp contrast can be seen, although the crystalline structure is preserved even for the highest dose. After annealing at typically 1600 °C a number of defects are seen as black dots. They are distributed around the projected range, R_P, although a majority are formed at slightly larger depths. Similar defect structures have previously been reported for boron implanted 6H-SiC[8] and in high resolution TEM they are seen to consist of planar faults of interstitial type residing on basal planes in the crystal. They appear to be circular with varying diameters, although the size increases with annealing temperature. Both the size of the defects and the concentration have roughly the same distributions with a maximum slightly deeper than R_P, as can be seen in Fig. 3. In Fig 3a the average number of planar faults

counted in 100×100 nm^2 areas is plotted as a function of depth and in 3b the average areal size of the defects, is plotted as a function of depth from the sample surface. The statistics is limited, but a rough estimate of the total number of interstitial atoms forming the defects can still be made. For this estimate we make the assumptions that the thickness of the TEM sample is 300 Å and that the atoms in the planar defects have a surface density similar to the SiC lattice. In the region between 200-300 nm we then obtain a concentration of 5×10^{19} cm^{-3} of interstitial atoms bound in the planar faults. Comparing this number with the TRIM data in Fig. 1 it can be concluded that the number of interstitial atoms bound in platelets is three orders of magnitude less than the total generated number of interstitials and roughly similar to the available Al concentration. Since a large part of the Al atoms are positioned at substitutional sites after this annealing temperature[2], it seems likely that the planar faults consist mainly of interstitial carbon or silicon atoms.

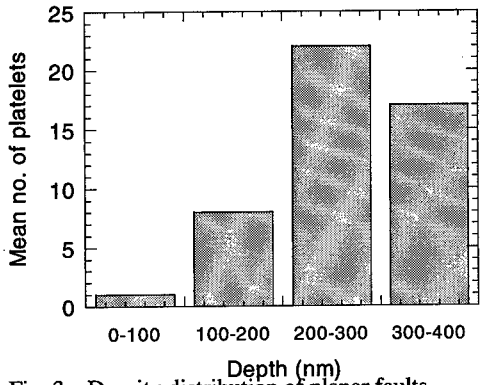

Fig. 3a. Density distribution of planar faults.

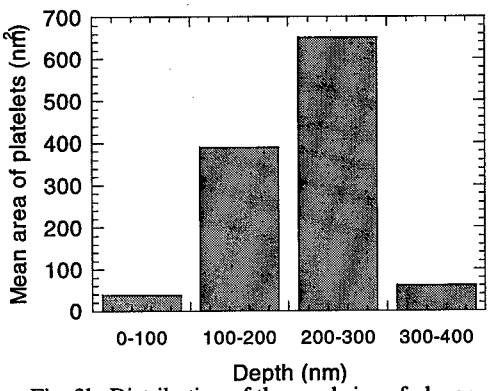

Fig. 3b. Distribution of the areal size of planar faults.

Examples of c-RBS spectra are shown in Fig. 4 for room temperature implants of 100 keV Al at doses ranging from 1×10^{13} to 1×10^{15} cm^{-2}. Already at the lowest dose a deviation from the virgin spectra can be seen. The damage then builds up roughly linearly for increasing doses, starting at the position of the projected range. For the highest dose the backscattered yield is about 80% of the yield at random incidence and the damage extends throughout the implanted layer to the surface. The dependence of implantation temperature is shown in Fig. 5, where the ratio of the random and channeled yield around channel 150 is plotted as a function of implantation temperature, T_{imp}. In Fig. 5 the beneficial effects of hot implantations can be clearly seen and at 800 °C the relative damage levels is almost reduced to the level in an virgin sample. It should also

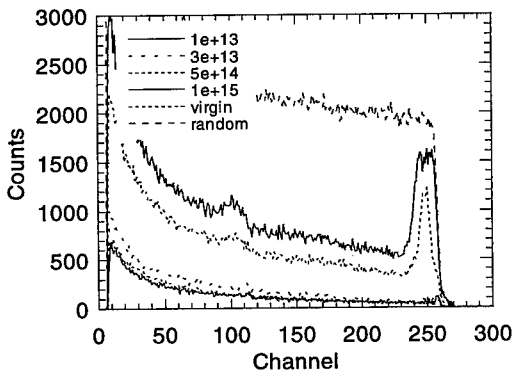

Fig. 4. c-RBS spectra from room temperature implants of 100 keV Al.

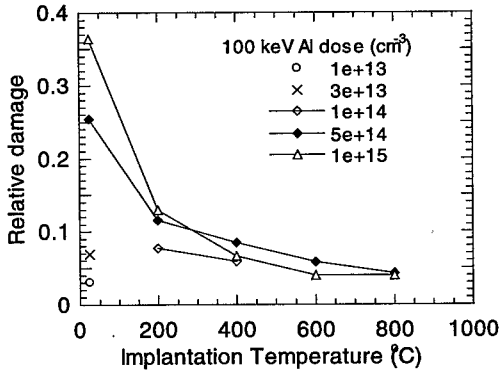

Fig. 5. Relative damage as a function of implantation temperature.

be pointed out that most of the annealing takes place at relatively low temperatures, below 200 °C. From the c-RBS data of higher temperature implantations it is also clear that the damage is distributed more evenly in the penetrated region and also extends to slightly larger depths, than is the case for room temperature implants where the damage is localised to the R_P-region for the same fluence.

Recent investigations[11] of point defects in SiC created by very low fluence ion implantations have shown that the generation of damage, as measured by the concentration of bandgap states, in SiC is much higher than in Si. The fluence used in these experiment was as low as 10^8 cm^{-2} and, if the comparison between Si and SiC is continued with the doses used in the present study, the same relation holds at a dose of 10^{13} cm^{-2}. This is the fluence where damage is first seen in the SiC c-RBS spectra for room temperature implants, while spectra from silicon samples implanted simultaneously with the SiC samples does not deviate from the virgin spectrum at this dose. However, comparing Si and SiC amorphization doses, it seems that Si turns amorphous at a similar or even slightly lower dose than SiC. Thus it appears to be a linear accumulation of damage that eventually lead to amorphization in SiC, while in Si amorphization is reach at some threshold dose.

4. Conclusions

Although diffusion of dopants in SiC requires very high temperatures, a substantial amount of defect motion occurs already for implantations at 200 °C, resulting in a high degree of damage reduction during the implantation. During high temperature post implant anneal self interstitials form planar faults that can be resolved in high resolution TEM. The formation and annealing kinetics of these defects and how they are related to point defect concentrations are the subject of further studies.

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Materials Science Forum Vols. 338-342 (2000) pp. 873-876

Excimer Laser Annealing of Ion-implanted 6H-Silicon Carbide

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Keywords: Electrical Conductivity, Excimer Laser, Ion Implantation, Laser Annealing, Photoluminescence, Rutherford Backscattering

Abstract XeCl excimer laser annealing of ion-implanted 6H-SiC was carried out. Laser annealed SiC was characterized by Rutherford backscattering, secondary ion mass spectroscopy (SIMS), electrical conductivity and photoluminescence. Laser irradiation reduced the χ values and increased electrical conductivity. The activation efficiency of the laser-annealed Al^+ implanted SiC was estimated to be about 0.1%. SIMS results suggest that SiC substrates were not melted by laser irradiation and that the laser annealing effect proceeded in solid phase.

1. Introduction

The ion implantation technique is very important for silicon carbide (SiC) electronic device fabrication, because the impurity diffusion technique cannot be applied to SiC owing to its low impurity diffusion rate.[1] Ion implanted SiC can be activated efficiently by annealing at 1500 °C or more.[2] However, such high-temperature annealing is hardly applicable to oxidized and metallized SiC.

In order to decrease the required and effective annealing temperature of ion-implanted SiC, we tried to achieve a non-thermal annealing process using a pulsed excimer laser of short wavelength. So far, few laser activation of ion-implanted SiC have been reported other than an attempt by Ahmed et al. [3] They reported that both *n*- and *p*-type dopants implanted into SiC were activated by pulsed excimer laser irradiation, which caused melting of the SiC surface for a moment, followed by a substrate seeded epitaxial regrowth.

In this paper, we report the excimer laser irradiation effects of ion-implanted 6H-SiC, characterized by Rutherford backscattering (RBS), secondary ion mass spectroscopy (SIMS), electrical conductivity and photoluminescence (PL).

2. Experimental procedures

N^+ and Al^+ were implanted in *n*-type commercial 6H-SiC substrates at room temperature. Before being placed into a laser annealing apparatus, the ion-implanted SiC substrates were degreased and chemically cleaned in a solution of H_2SO_4:H_2O_2 (1:1) for 5 min. Then, they were etched in a buffered HF solution to remove the native oxide.

Laser annealing was carried out using a laser ablation system, equipped with a 308nm pulsed XeCl excimer laser. The laser output and repetition rate were 130 mJ/pulse and 50 pulses/sec, respectively. The laser beam was not homogenized, and was focused to an area of 3×4 mm^2 by a lens.

The ion-implanted SiC substrate was placed on a target holder, and subsequently evacuated below 1×10^{-6} Torr. During laser beam irradiation, the SiC substrate was kept in a vacuum below 1×10^{-6} Torr, and not intentionally heated or cooled.

RBS analysis was carried out at room temperature using 2 MeV $^4He^+$ and a scattering angle of 100°. When the aligned spectra were measured, He ions were incident along the <0001> azimuth into the SiC substrate. Current-voltage measurements were carried out using vacuum deposited Al/Ti and Ni

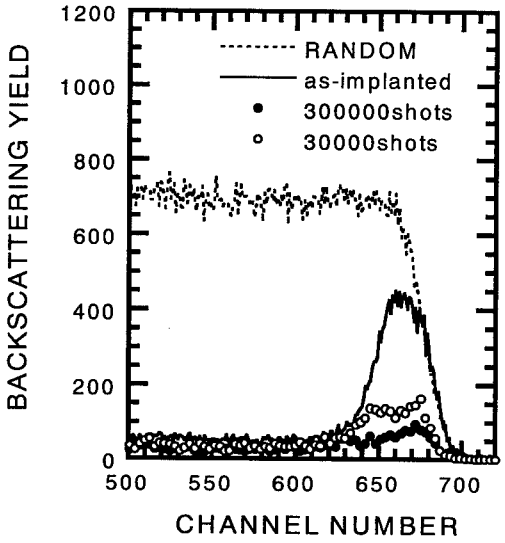


Fig. 1. RBS energy spectra of laser-annealed (○ ●) and as-implanted (—) Al^+ implanted SiC substrates.

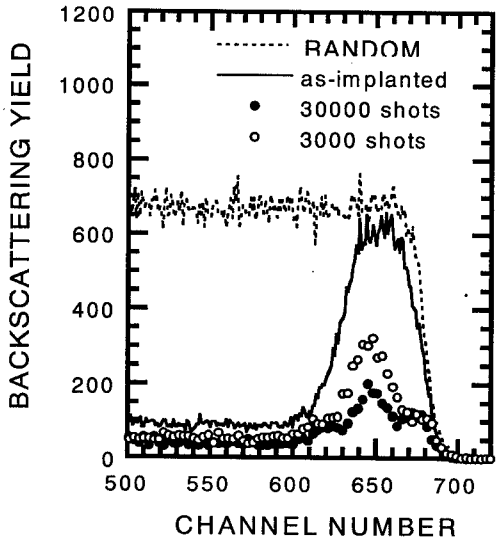


Fig. 2. RBS energy spectra of laser-annealed (○ ●) and as-implanted (—) N^+ implanted SiC substrates.

dots as electrode pairs which were not thermally processed after deposition.

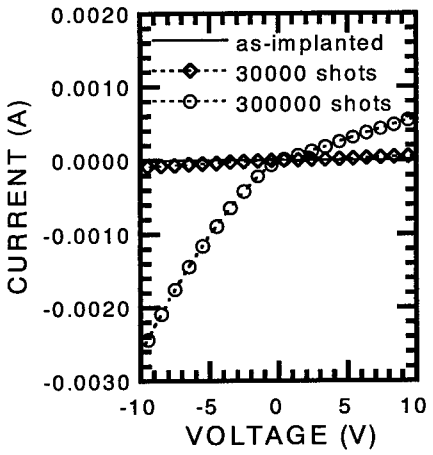
3. Results and discussion

Fig. 1 shows the RBS spectra of as-implanted and laser-annealed SiC substrates. 3×10^{14} cm^{-2} of 30 keV Al^+ were implanted in an *n*-type 6H-SiC substrate. Excimer laser irradiation of 30,000 shots and 300,000 shots were carried out for laser annealing. Channels from 630 to 690 of the RBS spectra corresponded to the Al^+ implanted layer. The χ value of the as-ion-implanted layer was 64%. When 30,000 shots and 300,000 shots of laser irradiation were performed, the χ values of the Al^+ implanted layers were suppressed to 20% and 10%, respectively.

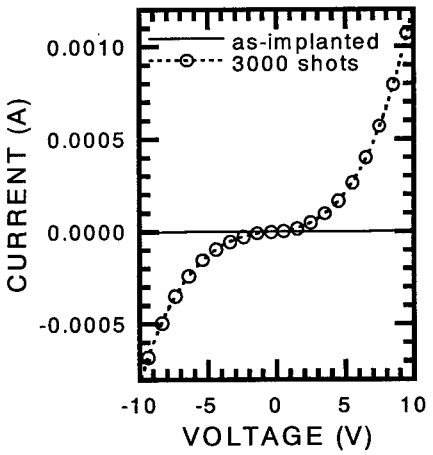
Fig. 2 shows the RBS spectra for the N^+ implanted case. 1×10^{15} cm^{-2} of 30 keV N^+ were implanted in an *n*-type 6H-SiC substrate. Channels from 610 to 690 of the RBS spectra corresponded to the N^+ implanted layer. The χ value of the as-implanted layer was 89%. When 3,000 shots and 30,000 shots of laser irradiation were performed, the χ values of the N^+ implanted layers were suppressed to 44% and 24%, respectively.

Figs. 3 and 4 show the difference between the current-voltage characteristics of the as-implanted and laser-annealed SiC substrates. As seen in Fig. 3, when the Al^+ implanted SiC substrates were annealed by 30,000 shots and 300,000 shots of laser irradiation, the current values at 10V increased from below 10 μA to 100 μA and 2.6mA, respectively. Similarly, the electrical conductivity of the N^+ implanted sample increased by laser irradiation of 3,000 shots, as shown in Fig 4. When 10 V was applied to the N^+ implanted SiC, the current values at 10V increased from below 10 μA to 1.2 mA, after 3,000 shots of laser irradiation.

The activation efficiency of the laser-annealed Al^+ implanted SiC was measured. In order to fabricate a box-shaped profile for Van der Pauu measurement, 6×10^{14} cm^{-2} of 50 keV and 1.3×10^{15} cm^{-2} of 100 keV Al^+ were implanted in an n^--SiC epitaxial layer. The Al atom concentration was estimated to be 1×10^{21} cm^{-3} using the TRIM program. 30,000 shots of laser irradiation were performed. The hole concentration at room temperature was 1.3×10^{18} cm^{-3}. Consequently, the



Figs. 3. Current-voltage characteristics of the as Al-ion-implanted (—) and laser-annealed (◇ ○) SiC substrates. For measurement, as-deposited Al/Ti dots were used as electrodes.



Figs. 4. Current-voltage characteristics of the as N-ion-implanted (—) and laser-annealed (○) SiC substrates. For measurement, as-deposited Ni dots were used as electrodes.

activation efficiency of the laser-annealed Al^+ implanted SiC was about 0.1 %.
These results indicate that XeCl excimer laser irradiation is effective for the electrical activation of ion-implanted impurities as well as the suppression of radiation damages in SiC. In addition, the laser annealing effects mentioned above increase when the number of laser pulses increases.
Figs. 5 and 6 show the Al and N depth profiles of SiC substrates before and after laser annealing

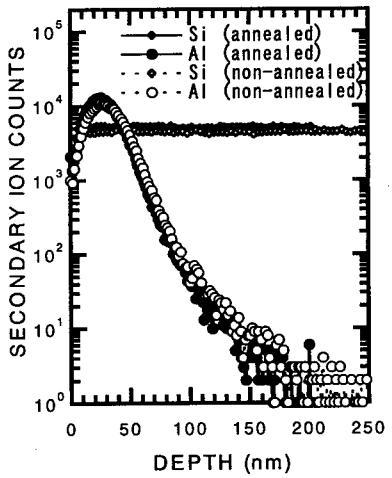


Fig. 5. Al depth profile of 3×10^{14} cm^{-2} of 30 keV Al^+ implanted SiC substrates before (○) and after (●) laser annealing.

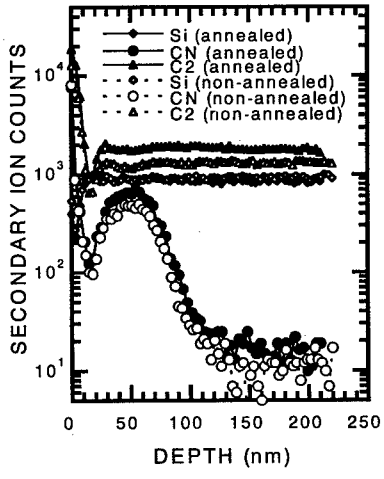


Fig. 6. N depth profile of 1×10^{15} cm^{-2} of 30 keV N^+ implanted SiC substrates before (○) and after (●) laser annealing.

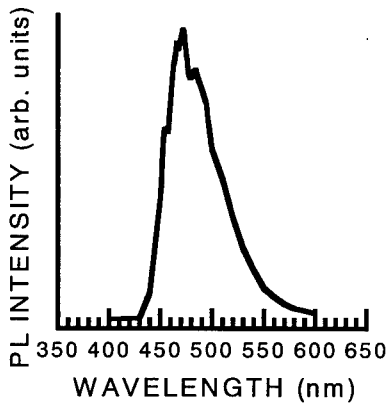


Fig.7. PL spectrum of commercial Al doped epitaxial SiC. Al concentration of the epitaxial layer was 1×10^{16} cm^{-3}

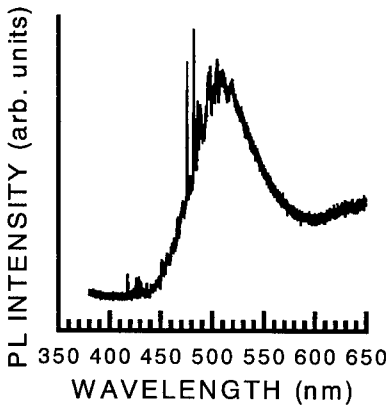


Fig. 8. PL spectrum of laser-annealed SiC. 6×10^{10} cm^{-2} of 50 keV and 1.3×10^{11} cm^{-2} of 100 keV Al^+ were implanted into an n^- SiC epitaxial wafer. The Al atom concentration was estimated to be 1×10^{17} cm^{-3} by TRIM. 30,000 shots of laser irradiation were performed.

obtained by SIMS. In both the Al^+ and N^+ implanted cases, no redistribution due to laser irradiation was observed. These results suggest that, in our experiments, the SiC substrates did not melt and the laser annealing effect proceeded in solid phase. This differs from the results of Ahmed et al., who reported that the activation of implanted atoms in SiC occurred through a melt-regrowth repetition by laser pulse irradiation.

Figs. 7 and 8 show the PL spectra of Al doped epitaxial SiC and laser-annealed SiC. An Al acceptor-N donor pair emission was observed at around 470 nm and 500 nm from the Al doped epitaxial SiC and laser-annealed SiC, respectively. The sharp peaks observed in the laser-annealed SiC are thought to be related to radiation damage. The low-energy shift of the donor-acceptor pair emission from the laser-annealed SiC seems to originate in a wider distance between the neutral donor and the neutral acceptor, and in the dominant non-radiative recombination.

4. Summary

XeCl excimer laser annealing of ion-implanted 6H-SiC was carried out. RBS measurement revealed a suppression of damage in the ion-implanted SiC by laser irradiation. The laser annealing effects, such as the χ value reduction and the rise in electrical conductivity, increase when the number of irradiation laser pulses increases. The activation efficiency of the laser-annealed Al^+ implanted SiC was estimated to be about 0.1%.

SIMS results suggest that the SiC substrates did not melt by laser irradiation and that the laser annealing effect proceeded in solid phase. The low-energy shift of the donor-acceptor pair emission from the laser-annealed SiC suggests a wider distance between the neutral donor and the neutral acceptor, and in the dominant non-radiative recombination.

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Materials Science Forum Vols. 338-342 (2000) pp. 877-880

High Concentration Doping of 6H-SiC by Ion Implantation: Flash versus Furnace Annealing

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Keywords: Aluminum, Annealing, Electrical Activation, Ion Implantation, Nitrogen

Abstract

The electrical properties of high concentration aluminum and nitrogen implanted layers have been investigated after furnace as well as flash lamp annealing. For Al doped layer the electrical efficiency is enhanced using flash lamp annealing. For highest Al concentrations the doped layer shows metal like conductivity. For N doped layers the flash lamp annealing effects no increase of the carrier concentration. Due to the short annealing time only the nitrogen on hexagonal sites is electrically active. Flash lamp annealing produced no extra damage of the vacancy type as proved by Positron Annihilation Spectroscopy.

1. Introduction

The annealing of the implantation induced damage and the relaxation of the SiC lattice is important for attaining a high electrical activation. The electrical efficiency is limited by the temperature dependent solubility of the dopants in the SiC lattice. Furnace annealing is reasonable up to temperatures of about 1800°C because of problems of Si sublimation and carbonization of the SiC surface. Recently, it was shown that using short time annealing techniques, like flash lamp annealing, higher temperatures are available and in the case of aluminum implanted 6H-SiC a higher electrical activation is attained [1].
Using furnace annealing the electrical activation of p- and n-dopants, like aluminum and nitrogen, were investigated up to temperatures of 1750°C. In the case of Al the hole concentration increases with increasing annealing temperature. Dislocation loops are obtained after high temperature annealing [2]. In the case of N implantation the electrical activation increases with increasing annealing temperature [3]. For this dopant an optimum temperature-time regime was found [4].
A few attempts using short time annealing were carried out by several groups. Ahmed et al. [5] used a pulsed eximer laser to anneal Al- and N-implanted layers. They deduced from Spreading Resistance measurements an electrical activation of more than 100 % which points to problems in the interpretation of the measurements. A distinct redistribution of Al and N towards the surface was found. Dzhibuti et al. [6] found by optical transmission measurements that after flash irradiation ($\tau \approx 10$ ms) and halogen lamp annealing ($\tau \approx 10$ s) at about 1100K of B-implanted layers (6×10^{15} cm^{-2}, 50 keV) the defects were annealed. But no electrical measurements were reported. Rapid thermal annealing using halogen lamps (RTA) was employed by Pensl et al. [7] (1200°C, 2 min.) for 6H-SiC and Hirano et al. [8] (1100°C, 10 s) for 3C-SiC. They obtained an enhancement of the carrier concentration after RTA compared to furnace annealing.

In this contribution results concerning the implantation of Al and N into 6H-SiC, the annealing and the electrical activation are briefly presented. Especially, the electrical efficiency of high concentration implanted layers after annealing using different techniques will be discussed.

2. Experimentals

Al- and N-ions were implanted at 400°C (see Ref. [2]) into epitaxially grown 6H-SiC wafers with different energies and doses in order to form a 500 nm thick box-shaped doped layer. The plateau concentration was varied for Al doping between $1x10^{18}$ cm^{-3} and $5x10^{21}$ cm^{-3} and for N doping between $5x10^{17}$ cm^{-3} and $5x10^{20}$ cm^{-3}. The wafers were annealed in argon ambient between 1450°C and 1700°C for 10 min. using an inductively heated furnace. Alternatively, flash lamp annealing was performed at about 2000°C by light irradiation of the wafer back side using an array of xenon lamps with a flash duration of 20 ms [1,9].
The samples were characterized by temperature dependent Hall effect measurements to investigate the electrical properties, SIMS measurements to determine the redistribution of the dopants and XTEM as well as Positron Annihilation Spectroscopy (PAS) to investigate the microstructure after annealing.

3. Results and discussion

3.1 Al-doped layer

In Fig. 1 for Al-implanted 6H-SiC the hole concentration in dependence on the Al plateau concentration is presented. For Al concentrations higher than 10^{20} cm^{-3} a strong increase of the hole concentration with increasing plateau concentration as well as annealing temperatures

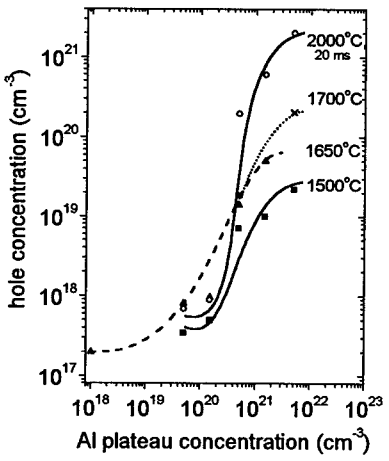

Fig.1: Hole concentration vs mean Al-concentration after annealing at different temperatures (measured at room temperature)

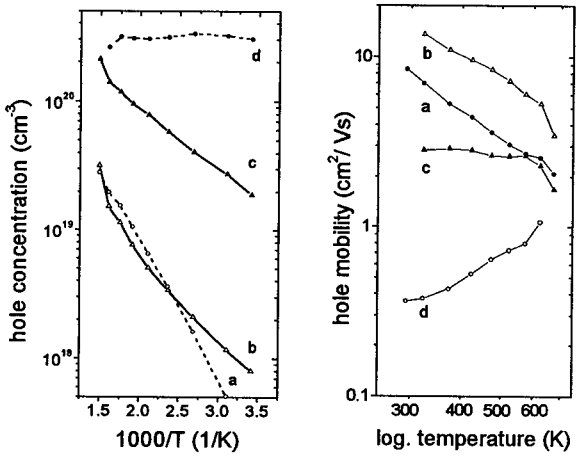

Fig. 2: Hole concentration and mobility vs temperature
$5x10^{19}cm^{-3}$: a-flash; b-furnace
$5x10^{20}cm^{-3}$: d-flash; c-furnace

are observed. For very high Al concentrations a temperature dependent limit of the hole concentration is indicated characterizing the "electrical" solubility of Al in 6H-SiC for the

chosen annealing temperature. After furnace annealing at 1500°C the recovery and the electrical activation is not complete. Dislocation loops from interstitial type were observed by XTEM as well as vacancy complexes by PAS. After annealing at 1650°C only dislocation loops were found. Using flash lamp annealing with the high temperature above the sublimation temperature of Si a further enhancement of the hole concentration is measured. The higher annealing temperature leads to a higher solubility of dopants on the SiC lattice sites. In the case of Al these substitutional atoms are frozen-in during the radiative cooling down because the diffusion of Al in SiC is negligible. Therefore, a higher hole concentration is observed after flash lamp annealing compared to furnace annealing.
In Fig. 2 the hole concentration and mobility in dependence on the measurement temperature are shown for a low and a high Al concentrations after furnace as well as flash lamp annealing. For the low Al concentration the thermally induced conductivity is dominating. For high Al concentration the temperature dependent hole concentration shows a smaller change because the effective ionization energy of Al acceptors decreases as a result of interaction between dopants, clearly shown after the flash lamp annealing. The mobility in dependence on the measurement temperature shows the typical scatter mechanism for the low concentration range. In contrast, for the high concentration range the mobility indicates the transition towards metallic conductivity.
The flash irradiation produces no additional vacavcy-type damage due to quenching effects as proved by PAS. A remarkable Al diffusion was never observed after furnace or flash lamp annealing as revealed by SIMS profiling.

3.2 N-doped layer

In Fig. 3 the carrier concentration and mobility are shown versus the N plateau concentration and different annealing methods, measured at room temperature. After furnace annealing the carrier concentration is enhanced with increasing plateau concentration and annealing temperature. After flash lamp annealing compared to furnace annealing only a lower carrier concentration was measured in spite of the higher annealing temperature. The mobility decreases with increasing N concentration. The highest mobility was measured after flash lamp annealing. Hall effect measurements versus the temperature show that the slope of the mobility curves is approximately constant showing a comparable scattering mechanism for furnace and flash lamp annealing.
SIMS measurements give no evidence of N diffusion during the annealing.
In Fig. 4 the carrier concentration versus the reciprocal temperature is shown after furnace as well as flash lamp annealing. For the furnace annealed samples the typical dependence for n-doped layers is observed [3,10]. The Hall effect analysis by fit of the neutrality equation results in two donor levels of (79 meV) and (128 meV) with a concentration ratio of 1 : 2 which agrees with the ratio of inequivalent hexagonal to cubic lattice sites in the unit cell of the 6H-SiC [10]. On the other hand, the flash lamp annealed sample shows a saturation value in the high temperature range characterizing that all donors are ionized. The analysis of this sample shows only one level of 81 meV.
N atoms occupy hexagonal and cubic lattice sites characterized by different ionization energies. The measured difference regarding the carrier concentration after furnace and flash lamp annealing reflects the ionization probability on the hexagonal and cubic lattice sites. From our results we conclude that the low energetic hexagonal sites will be occupied primarily. In consequence of the short annealing time the occupation of the cubic sites is small. Therefore, the determined ionization energy of 81 meV after flash lamp annealing is characterized by the occupation and electrical effeciency of the hexagonal sites.

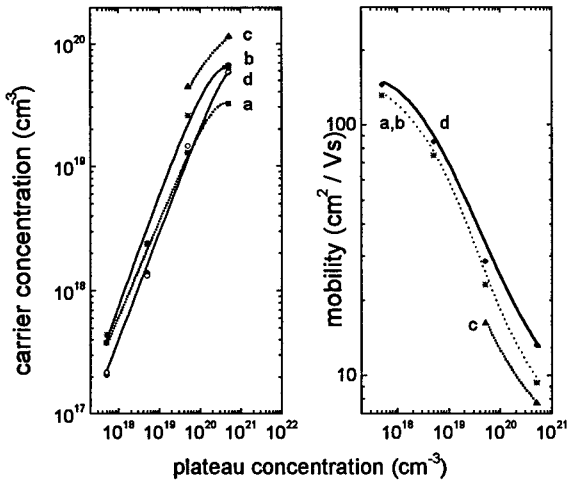

Fig. 3: Carrier concentration and mobility vs N plateau concentration a-1450°C; b-1550°C; c-1650°C, d- flash lamp

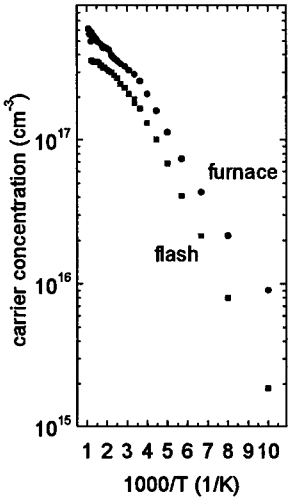

Fig. 4: Carrier concentration vs reciprocal temperatur ($n_{plateau}$=5x10^{17}cm^{-3})

4. Conclusions

The annealing behaviour of Al- and N-implanted 6H-SiC layers was investigated. After flash lamp annealing at about 2000°C for high concentration Al doped layers an enhancement of the carrier concentration is observed in comparison to furnace annealing. For N-implanted layers after flash lamp annealing no higher electrically effective concentration is measured because only the N on hexagonal lattice sites is electrically efficient.
After flash lamp annealing no additional damage compared to furnace annealing and no diffusion of the dopants are observed.

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Consequences of High-Dose, High Temperature Al^+ Implantation in 6H-SiC

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Keywords: Al_4C_3 precipitates, Aluminium implantation in 6H-SiC

Abstract: High doses of 350 keV Al^+ ions were implanted into 6H-SiC single crystals at 500°C. The Al atoms occupy preferentially Si sites in the SiC lattice. The replaced Si atoms seem to be mobile under the given implantation conditions and diffuse out. At higher Al concentrations the SiC matrix is decomposed and Si and Al_4C_3 precipitates are formed. It is found that the Al_4C_3 precipitates have a perfect epitaxial orientation to the SiC matrix. The phase transformation is accompanied by atomic redistribution and strong volume swelling.

Introduction

Silicon carbide (SiC) is a semiconductor, suitable for high temperature and high power applications. Aluminium is a very attractive p-type dopant because of its lower ionization energy. High temperature Al implantation creates defects, which are only partially annihilated by subsequent high temperature annealing [1].

In this paper the incorporation of aluminium into 6H-SiC after high dose, high temperature Al implantation is studied. The formation of aluminium carbide (Al_4C_3) during implantation, in epitaxial relation with the 6H-SiC matrix, is shown. As a byproduct silicon precipitates were also formed. The phase formation was studied by Transmission Electron Microscopy (TEM) and SIMS. The stability of the Al_4C_3 compound during high temperature annealing was investigated.

Experimental procedure

Single crystalline 6H-SiC wafers having (0001) orientation, were implanted with doses of $1x10^{17}$ Al^+ cm^{-2} and $3x10^{17}$ Al^+ cm^{-2} with an energy of 350 keV, at 500°C. According to TRIM calculations maximum Al concentrations of about 5 and 15 %, respectively, can be expected in a depth of 380 nm. Parts of these specimens were subsequently annealed at 1400°C for one hour in argon ambient. The aluminium atomic concentration depth profiles were measured by SIMS.

Results and discussion

After Al implantation with a dose of $3x10^{17}$ cm^{-2}, an extended, highly defected zone was formed. Within this damaged zone a narrow band of large crystalline precipitates were observed around the mean projected ion range of 380 nm. The precipitates have a laminar shape, as shown in Fig.1a. Above and below the precipitated zone a highly defected zone was formed. The dominating defects are stacking faults and segment of dislocations in agreement with [1]. Selected area diffraction patterns (SADP) taken from the precipitated zone reveal that these are Al_4C_3 and Si precipitates, Fig.1b. The SADP taken from an Al_4C_3 precipitate is shown in Fig. 1b. The 0006 6H-SiC reflection is denoted by the letter d, also the row of the $\{0\bar{1}1L\}$ spots of the 6H-SiC is denoted by the arrow A. The extra spots denoted by the letters a,b,c and e corresponds to the 0003, 0006, 0009

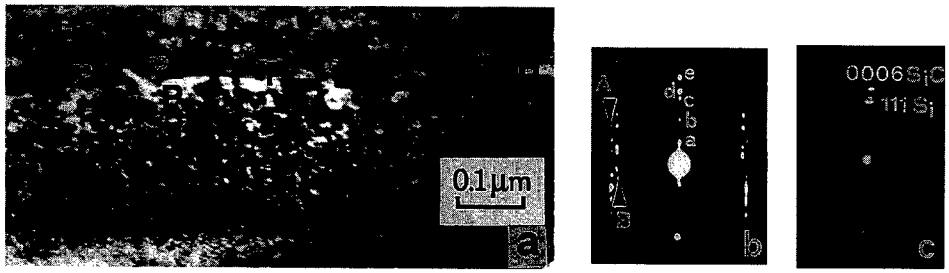


Fig.1 Specimen implanted with dose $3x10^{17}$ Al^+ cm^{-2} a) Cross section TEM micrograph from the implanted area.. Laminar precipitates are evident denoted by the letter P. .b) SADP from an Al_4C_3 precipitate c) SADP from silicon precipitate.

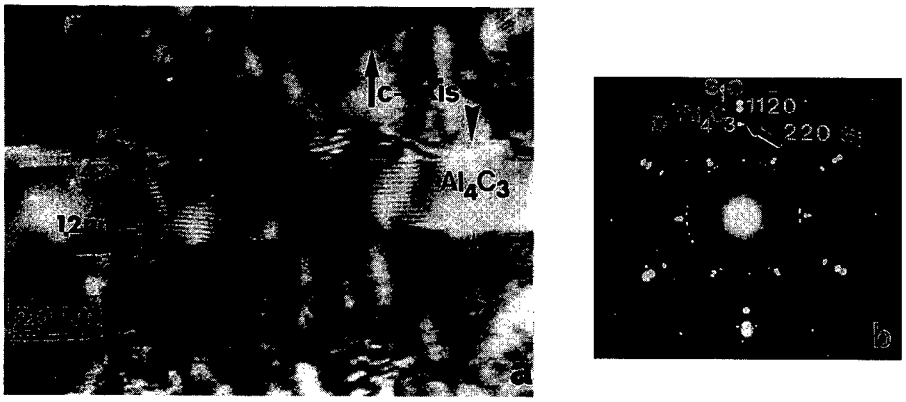


Fig.2 Specimen implanted with dose $3x10^{17}$ Al^+ cm^{-2} a) Cross section TEM micrograph from an Al_4C_3 precipitate. The moiré pattern is evident. b) SADP from the precipitated zone, the electron beam was exactly parallel to the c-axis. The $11\bar{2}0$ spot is double, the outer belongs to the 6H-SiC matrix and the inner spot to the Al_4C_3 precipitates. The 220 spot exited from the Si precipitates is denoted by an arrow.

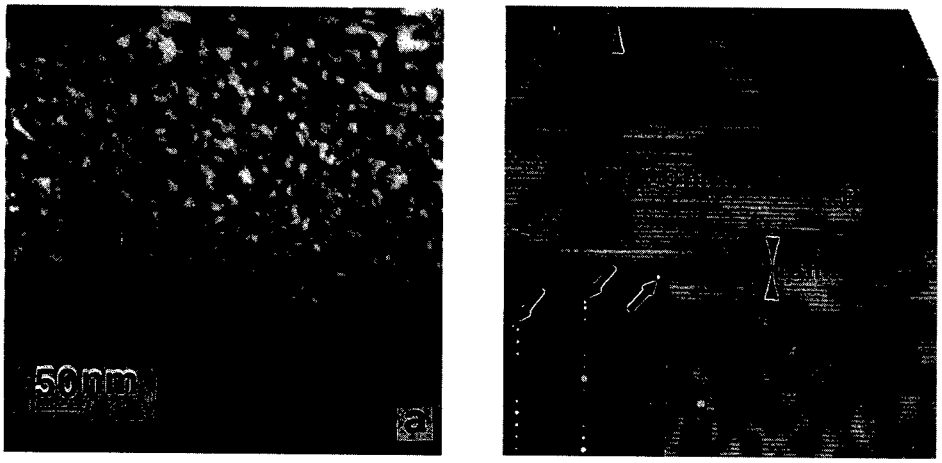


Fig.3 Cross section TEM from the specimen implanted with dose $1x10^{17}$ Al^+ cm^{-2} a) As implanted b) annealed at 1400°C for one hour. The small Al precipitates exhibit moiré pattern due the epitaxial relation with the matrix. Related SADP are shown in the inset. Arrows denote the aluminium spots.

and 00012 Al_4C_3 reflections, the last one, is the most intense spot. Also the row of the spots denoted by the arrow B belongs to the $\{0\bar{1}1L\}$ Al_4C_3 reflections, revealing the epitaxial relation of the Al_4C_3 compound with the 6H-SiC matrix. The Si precipitates are evident from the SADP in Fig.1c. The 111 silicon spot, shown in Fig.1c, is along the c-axis of the 6H-SiC, revealing that the silicon precipitates were formed preferentially according to the orientation relation $[111]_{Si}//[0006]_{SiC}$.

The presence of Al_4C_3 was also confirmed by moiré pattern [2]. These moiré patterns are perpendicular to the c-axis of the 6H-SiC matrix, Fig.2a. The spacing D of the moiré pattern is 1.19 nm. This is very close to the theoretical one (1.18 nm) for the following orientation relation [0001]6H-SiC//[0001]Al_4C_3. The precipitates were further studied by plan view TEM (PVTEM) observations. The characteristic $11\bar{2}0$ and $10\bar{1}0$ type 6H-SiC and Al_4C_3 diffraction spots of the (0001) zone were observed, as shown in Fig.2b. This confirms that the two lattices have the orientation relation, [0001]6H-SiC//[0001]Al_4C_3 also $[11\bar{2}0]$6H-SiC//$[11\bar{2}0]Al_4C_3$. No Al_4C_3 precipitates with other orientations were observed. Most of the Si precipitates are also in epitaxial relation with the 6H-SiC matrix having the orientation relationship [0001]6H-SiC//[111]Si and $[11\bar{2}0]$6H-SiC//[220]Si as shown in Fig.2b. However, about 30% of the Si precipitates are randomly oriented, as the diffraction rings reveal in Fig.2b.

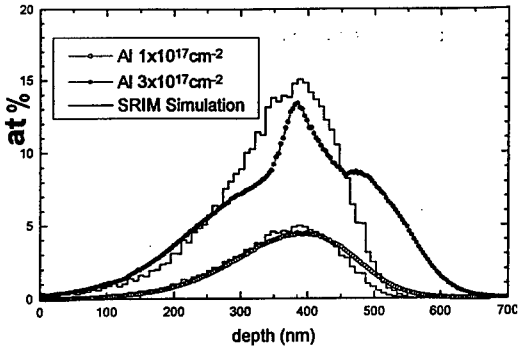
The formation of Al_4C_3 is related with the decomposition of SiC and the release of free Si according the reaction (1) [3].

$$3SiC + 4Al \rightarrow Al_4C_3 + 3Si \qquad (1)$$

A second experiment was performed by implanting aluminium with lower dose, $1x10^{17}Al^+cm^{-2}$, all the other conditions were kept the same. In this case no Al_4C_3 or Si precipitates were observed, only a defected zone was evident, revealing that the implanted aluminium was incorporated in the lattice and in the defects, as shown in Fig.3a.

The Al profiles measured by SIMS are shown in Fig.4. For the lower dose the Al profile is in very good agreement with the result of the Monte-Carlo range simulation SRIM. Clear deviations from the expected ion range profile are evident in Fig.4 for the higher dose. The formation of an Al spike at the depth of about 380 nm is an indication for compound formation in this region. The band of precipitates found in the XTEM analysis is obviously correlated with the Al peak.

Annealing the specimen implanted with a dose $3x10^{17}$ Al^+ cm^{-2} at 1400°C results in the formation of aluminium precipitates with the following epitaxial orientation relationship with the matrix, [0001]6H-SiC//[111]Al and $[11\bar{2}0]$6H-SiC//[220]Al as the related moiré pattern reveal in Fig.5. The related diffraction pattern is shown in the inset of Fig.5. Very few Si precipitates were observed in this case, instead large cavities were formed. It is evident that Al_4C_3 decomposes at high temperatures. The formation of the large Al precipitates in the area where the Al_4C_3 were formed strongly suggests insignificant Al out diffusion. This also suggest that the released carbon reacts with the Si precipitates forming again SiC according to the reverse equation (1). Only very few traces of Al_4C_3 were observed after the annealing. The formation of cavities during the high temperature annealing reveals that for the formation of SiC the diffusing species is the Si. Annealing the implanted specimen ($1x10^{17}$ Al^+ cm^{-2}) at 1400°C results in reduction of the existing defect and the formation of small aluminium precipitates with the same epitaxial orientation with the matrix as shown in Fig.3b. The precipitates now are spherical with a mean diameter of 5nm. No cavities were observed in this case. The formation of aluminium precipitates after Al^+ implantation in 6H-SiC with dose $2x10^{16}cm^{-2}$ at 1400°C, subsequently annealed at 1800°C for 5s, has been reported [1]. It seems that Al_4C_3 is formed above a critical dose. In agreement with previous results it was shown that the Al atoms preferentially occupy Si sites. One reason could be the preferential displacement of Si in the SiC matrix by the Al projectiles because of the higher momentum transfer in the atomic collisions [3]. However, more likely, the main driving force for substituting Si by Al is the higher energy of the Al-C bond compared to the Si-C bond [3,4].



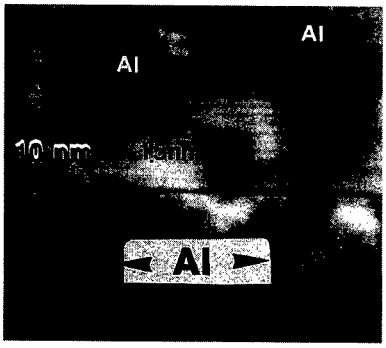


Fig.4 SIMS profiles of aluminium concentration % versus depth of the as implanted specimens.
Fig.5 Cross section TEM micrograph from specimen implanted with dose $3x10^{17}$ Al^{+} cm^{-2} subsequently annealed at 1400°C for one hour. Large laminar Al precipitate corresponding to the maximum Al concentration, as well as spherical Al precipitates at the side band, exhibiting moiré pattern are evident. The related diffraction pattern is shown in the inset.

Conclusions

The energetic preference of Al-C bonds gives the explanation why the doping of SiC with Al is so successful. Silicon substitution by Al occurs already at low temperatures as demonstrated by the implantation experiments at 500°. The strong bonding of Al-C dimers compared to Al-Al and Al-Si is shown to be responsible for the aluminum carbide formation [5,6] Above a critical Al concentration the SiC matrix is decomposed and precipitates of Si and Al_4C_3 are formed. The Al_4C_3 precipitates are plates because the supercritical Al concentration is reached only in a narrow zone around the peak of the implantation profile. Unfortunately, there is only few information about the electrical properties of Al_4C_3. Unlike the most transition metal carbides, which have metallic conduction, [7] Al_4C_3 could be a semiconducting material [7]. Further experiments are in progress in order to study the thermal stability and the electrical properties of the Al_4C_3/Si layers formed by high dose Al implantation into 6H-SiC.

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Materials Science Forum Vols. 338-342 (2000) pp. 885-888

Al and Al/C High Dose Implantation in 4H-SiC

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Keywords: Al and Al/C Implantation, Hall Measurement, pn Junction, Sheet Resistance

Abstract : We report an electrical investigation of high dose Al and Al/C ion-implantation in 4H-SiC. We show that, using a reasonably high temperature annealing (1670°C) for 10 minutes, low resistivity can be obtained. Our best result is ~95 mΩ.cm at 300 K. We also verify the electrical activation enhancement, already reported when using Al and C co-doping. The lowest specific resistance is ~ 2 mΩ.cm^2 for a PN junction realized by Al implantation.

4H SiC is the most promising SiC polytype for manufacturing high-power, high-temperature and high-speed electronic devices with outstanding capabilities [1]. As a consequence, tremendous progress has been made in the crystal growth and device processing technology. Of course some weak points remain. One is a real difficulty to perform efficient p-type selective doping.

Because of the very high temperature needed to perform any (efficient) diffusion of dopants [2], this has to be done by ion-implantation. The doping profile and the final concentration can be independently adjusted but, still, two major problems remain. One is to obtain a reasonable high density of electrical carriers. This is because of the large activation energy of acceptor impurities in 4H-SiC. It ranges from E_A = 191 / 230 meV for aluminum [3 - 5] to E_A = 285 / 390 meV for boron [3, 6, 7]. Since there is no other (shallower) acceptor identified up to now, the direct consequence is that one cannot easily realize a low sheet resistance. The second one comes from the high temperature annealing step (1600°C - 1700°C) which is needed to remove the process induced damage. In many cases, important chemical and morphological surface deterioration occur (like graphitisation and step bunching), which lower the electrical properties.

Recently, very much work has been done to improve on the activation of p-type implanted species in SiC. The activation was optimized for temperature annealing in the range 1600°C to 1700°C for 6H [3, 8 - 9] and 4H [10] polytypes, respectively, but relatively low concentrations of implanted species (< 5x10^{18} atom per cm^3) were used. This resulted in layer resistivity larger than 0.5 Ω.cm. In order to decrease the power losses, for high-power applications like GTO or thyristors, lowest anode and contact resistances are needed. Attempting to solve this problem, a few results on high dose implantation (>10^{16} cm^{-2}) were reported. For 6H-SiC, using C and Al co-doping to increase the activation of Al species, Tone et al. [11,12] achieved a low 0.22 Ω.cm for a targeted Al concentration of 2.10^{21} atom cm^{-3}. However, in this case, the Hall measurement evidenced a non-intrinsic hoping conduction mechanism. Wirth et al. [13] used independently high implantation conditions and flash lamp annealing at 2000°C. They obtained the lowest resistivity ever reported for Al-implanted 6H-SiC (60 mΩ.cm, with a total Al-concentration of 5x10^{20}cm^{-3}). However, similar to the work of Ref.11, they found a metallic-like behavior with a very poor mobility (0.4 cm^{2}V^{-1}s^{-1}). Less results are available for 4H-SiC and, to the best of our knowledge, the

maximum free hole concentration achieved is $2.9x10^{18}cm^{-3}$ for a targeted Al-concentration of $6.5x10^{20}$ cm^{-3} [14]. This corresponds to a (rather poor) resistivity of 0.28 Ω.cm.

In this work we report attempts to perform low resistivity p-type doping in 4H-SiC epilayers by using Al and Al/C ion-implantation. The target material was 4 μm thick epitaxial layers purchased from CREE, with a n^- doping level of 10^{16} cm^{-3}. Using multiple energy implants in the range 30 keV to 180 keV at 650°C, we realized box profile of 220 nm depth with Al concentrations ranging from 10^{19} cm^{-3} to 10^{21} cm^{-3}. Post-implantation anneals were done for 10 min at 1670°C. Because no sufficient latitude exists in the annealing temperature to achieve, at the same time, a high Al activation and a low surface deterioration short time annealing was used. In order to prevent silicon losses, we used a crucible with a SiC source in front of the implanted surface. In these conditions we could maintain a good Si overpressure and limit the sublimation of the surface species. This resulted in a nice surface morphology, evidenced by AFM measurement. For 5μm*5μm square areas, we obtained typical RMS roughness of 0.1 nm after annealing. This has to be compared with the large grooves, 20 nm deep and 500 nm wide, aligned along the $<1\bar{1}00>$ direction which were always present without counter physical vapor transport.

The conduction mechanism was studied by performing Hall measurement in the temperature range 300 K - 750 K. The test features were a conventional Van der Pauw structures, with MESA-etched patterns. Contacts were done using sputtered Al/Ti, followed by a 950°C anneal. In Fig.1 we show the temperature dependence of the resistivity obtained for 6 different samples. Starting from ~ 2 Ω.cm at room temperature, it decreases to ~ 20 mΩ.cm at 750K. Our best result is a fairly low ~95 mΩ.cm at 300 K.

The interesting point is that, under such high dose implantation conditions, the free hole mobility remains intrinsic-like in nature. This is shown in Fig.2. Increasing the temperature from 300 to 700K, we find in both cases of low, intermediate and high implantation doses, the same qualitative behavior. At room temperature, the diffusion mechanism is dose dependent. This is because of scattering by the ionized impurities. At high temperatures remain only the scattering by lattice modes and, in this case, the mobility depends only weakly on the implantation dose. This intrinsic behavior demonstrates unambiguously that, even in the case of our most implanted samples, the conductivity remains semiconductor-like in nature. Since we are close to the theoretical limit expected for the Mott transition in 4H-SiC, this is a very important point to outline. The consequence is that we find an intrinsic free holes mobility of ~ 4 $cm^2V^{-1}s^{-1}$ at 300 K in the most implanted sample. Comparing with the work of Ref.13 on flash-lamp annealing in 6H-SiC, this is about one order of magnitude larger.

Since at 700K the free hole mobility appears sample independent, any change in resistivity must correlate with a change in carrier concentration. Our experimental results show that, decreasing the dose by a factor of 10, the resistivity increases by a factor of 3. This is in very good agreement with simple statistic arguments. Indeed, assuming that most of the compensating species (N_c), come from the initial doping level (N_d) of the epitaxial layers and taking into account the important ionization energy of acceptors, one can easily expect that at ~700K the boundary condition : $N_c \approx N_d << p << N_a$ is fully satisfied. In this case the neutrality equation simplifies and writes :

$$p \approx (\beta N_v N_a)^{\frac{1}{2}} e^{-\frac{Ea}{2kT}} \qquad (1)$$

In this expression β is the degeneracy factor, E_a the activation energy, N_v the effective density of states in the valence band and N_a the concentration of activated acceptor species. Whatever is the dose, introducing an activation coefficient A, the concentration of activated acceptors N_a can be written: $Na = A\,Ct$ where C_t is the targeted concentration. Provided Eq.1 is fully satisfied and A is a constant, p reduces then to :

$$p \approx (A\beta N_V C_t)^{\frac{1}{2}} e^{-\frac{Ea}{2kT}} \quad (2)$$

In other words at high temperatures, in the framework of Eq.2 the free carrier concentration p must scale like the *square root* of the targeted concentration C_t and the resistivity like the *inverse square root* of the C_t. This is exactly what is shown in the insert of Fig.1. The -½ slope indicated as a line is in very good agreement with the experimental datas and confirmed the validity of our hypothesis.

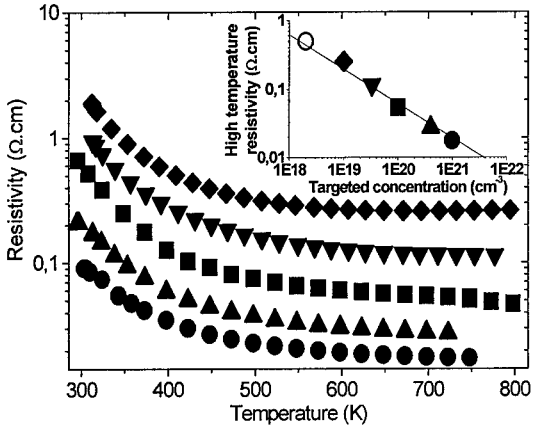

Fig.1: Temperature dependence of resistivity for targeted concentrations (cm^{-3}) :
◆ $1x10^{19}$ ▼ $3.3x10^{19}$ ■ $1x10^{20}$ ▲ $4x10^{20}$ ● $1x10^{21}$
Insert: concentration dependence of the high temperature values.

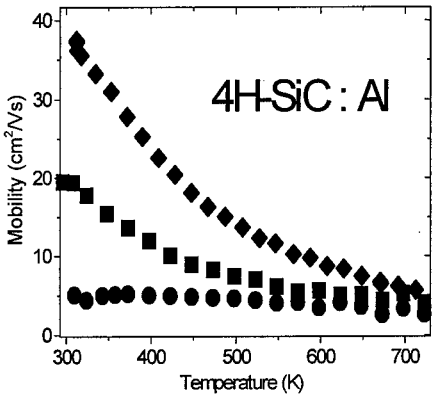

Fig.2: Temperature dependence of mobility for targeted concentrations (cm^{-3}) :
◆ $1x10^{19}$ ■ $1x10^{20}$ ● $1x10^{21}$

From this results it seems that no high concentration of electrically compensating centers was introduced during the implantation / annealing steps. Also, given a process, it seems that the activation coefficient A is reasonably constant. To check this point in further detail we have considered the work of Ref.3, taking similar annealing conditions (a few minutes at 1700°C). We get the result plotted as open symbol in the inset of Fig.1. Despite a large difference in implantation dose and implantation energy (2 MeV in the work of Ref.2 against only 180 keV in this work) this shows that, provided similar annealing conditions are used, similar activation rate is obtained. This makes straightforward the design of any high temperature (p-type) sheet resistivity.

To raise the electrical activation, without changing the process optimized for surface integrity, we have performed Al and C co-implantation using various C/Al concentration ratios. As reported for 6H-SiC [11], we have found evidence of activation enhancement. Indeed, for an Al targeted concentration of 10^{20} cm^{-3}, the room temperature resistivity decreases by a factor of two (from ~0.6 to ~0.31 Ω.cm) when the C/Al concentration ratio increases from zero to one.

Finally, we have produced Mesa-etched p-n junctions. Two typical plots of the characteristics obtained with a $5x10^{15}$ cm^{-2} implantation dose are shown in Figures 3 and 4. Notice that the reverse characteristics exhibits a 200 $nA.cm^{-2}$ leakage current at -200 V (insert) while the breakdown voltage is approximately 400 V. Considering the n^- layer thickness (4μm) and the doping level (10^{16} cm^{-3}) as well as the very simple technology used (without any periphery protection) this is quite a reasonable result. The nice point is that the direct characteristics log $I(V)$ is linear over nine orders of magnitude before entering the high current saturation regime at a forward bias of ~ 2.8 V. The ideality factor is closed to 2, which suggests that recombination in the space charge is the dominant

mechanism. The high current density obtained (typically 100 A/cm^2 for a forward bias of 3V) corresponds with a low specific resistance of 2 mΩ.cm^2. This value was not changed by increasing the implantation dose, demonstrating that the main contribution to the on resistance did not come anymore from the implanted layers.

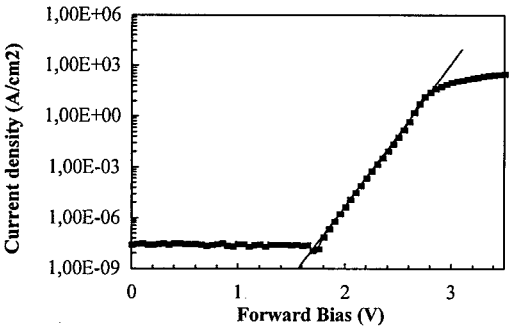

Fig.3 : Forward I-V characteristic for a vertical PN junction diode made by Al implantation at 650°C in n-type 4H SiC.

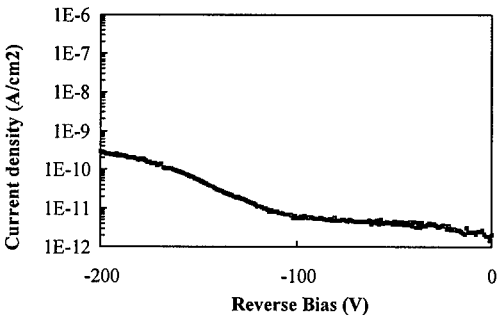

Fig.4 : Reverse I-V characteristic for a vertical PN junction diode made by Al implantation at 650°C in n-type 4H SiC.

To summarize, we have shown that implanting aluminum at high dose and performing a short annealing step at 1670°C can result in a low resistivity. With a targeted concentration of 10^{21} cm^{-3}, we could rich ~ 95 mΩ.cm at room temperature. The nice point is that, for such a high dose, we still maintain an intrinsic conduction mechanism with no evidence of metallic conductivity. Prototype PN junctions realized on such material exhibited low series resistances of ~ 2 mΩ.cm^2.

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Materials Science Forum Vols. 338-342 (2000) pp. 889-892

Channeled Implants in 6H Silicon Carbide

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Keywords: Channeling, Implantation, Monte Carlo Simulations, SIMS

ABSTRACT Implants of MeV ^{11}B, ^{27}Al, and ^{69}Ga into the <0001> channel of 6H-SiC have been performed and concentration versus depth profiles have been obtained utilizing secondary ion mass spectrometry (SIMS). The experiment shows that the deepest channeled Ga ions reach a depth of 6.6 μm, which is 4 times deeper than the projected range of a random angle implantation, while the deepest channeled B ions only exceed the random projected range by 40%. Measurements at several implantation fluences show that implantation induced damage quench the deep channeling at fluences around 2 and 10×10^{13} cm^{-2} for Al and Ga, respectively, while only a minor fluence dependence is found in the B implants at fluences up to 2.6×10^{14} cm^{-2}. The ion mass dependence of these effects is explained by the electronic to nuclear stopping ratios. Monte Carlo simulations of the channeling implants have also been performed and good agreements are found between simulations and experimental data.

INTRODUCTION

Even though samples are normally kept at some "random" direction during ion-implantation in SiC, channeling effects can not be completely avoided and ions steered into high symmetry directions of the crystal can reach deep into the material [1]. Despite of this very little has so far been published about channeling in SiC. In a recent publication, where 1.5 MeV Al^+ ions were implanted parallel to the <0001> axis in 6H-SiC, we showed that the deepest channeled ions reached about 3 times deeper than ions implanted at a random angle [2]. This deep channeling rapidly decreased when the implantation tilt angle was increased, and at a tilt angle of 2° away from the <0001> axis, the implanted profile was equivalent to the random case. In this study we have focused on the dependence of ion mass and implantation fluence on the implantation profiles in samples aligned in the <0001> direction.

EXPERIMENT

Implantations were performed on an *n*-type 6H-SiC epitaxial layer from CREE research, which was carefully cleaned and cut into 8×8 mm^2 pieces. Alignment of the samples with the <0001> axis parallel to the beam was obtained using the Rutherford backscattering setup at the Uppsala University 6 MV tandem accelerator. The 2.4 MeV He^+ beam used in the RBS analysis was turned off as soon as alignment was achieved and the ion beam was then changed to either of the three acceptor ions: $^{11}B^+$, $^{27}Al^+$, or $^{69}Ga^+$. The precision in the alignment was better than 0.1° and the maximum divergence of the ion beam was 0.02°. The beam was focused to a spot on the samples with an approximate diameter of 2 mm and no beam scanning was employed. Due to non-uniform current-density in the beam, the implanted ions were distributed across the sample surface with a higher fluence in the center of the implanted region than at the edge of it. Five implantations were

performed for this study: two samples using 1.5 MeV $^{27}Al^+$ ions to a relative high and low implantation dose, respectively (later referred to as Al_{hi} and Al_{lo}); two samples using 3.0 MeV $^{69}Ga^+$ ions, high and low doses (Ga_{hi} and Ga_{lo}); and one sample using 1.44 MeV $^{11}B^+$ (B_{hi}). A sixth sample (Al_{He}) was implanted with 1.5 MeV $^{27}Al^+$, but the He dose used for alignment was intentionally 7 times larger compared to the other samples. This was done in order to investigate whether the defects induced by the He irradiation affect the subsequent acceptor ion implantation. Since the experimentally obtained distributions from the Al_{lo} and Al_{He} samples were close to identical, it was concluded that the use of He in the alignment had no significant influence on the succeeding implantation.

Acceptor atom concentration as a function of sample depth was determined by secondary ion mass spectrometry measurements (SIMS) utilizing a Cameca IMS 4f microanalyser. A primary sputtering beam of 8 keV $(^{16}O)_2^+$ ions was rastered over an area of 200×200 μm^2 and secondary ions of $^{11}B^+$, $^{27}Al^+$, and $^{69}Ga^+$ were collected from an area 60 μm in diameter, in the center of the sputtered crater. Since the variation of the implanted dose over the 60 μm analyzed area was estimated to be within the experimental accuracy, SIMS analysis could be used to determine the implantation distribution locally, thus providing profiles with varying implantation fluence from each sample. The ^{69}Ga measurements were not straightforward due to a mass interference with the $^{28}Si^{29}Si^{12}C$ molecule in combination with sample charging. This effect made calibration to absolute concentration values less reliable than for the Al and B measurements. The uncertainty in concentration for the Ga-profiles was about a factor of 5, but the relative accuracy of the Ga-curves was, however, better than a factor of 2.

RESULTS AND DISCUSSION

Fig. 1 demonstrates the SIMS profiles for the ^{11}B, ^{27}Al, and ^{69}Ga implanted samples. Starting with the Al_{lo} profile having a fluence of 0.66×10^{12} cm^{-2} (Fig. 1b), a distinct peak in the distribution is found at 1.3 μm. The position of this peak is closely related to the projected range (R_p) of 1.5 MeV Al^+ implanted in a random direction, as reported in Ref. [2] (and does not depend on the implanted fluence). This implies that the ions causing this peak follow a random path from start, or are scattered out of the <0001> channel at an early stage during the first surface oscillations [3] of the channeled beam. This peak will be referred to as the random peak in the remaining of this paper. The Al concentration then decreases slowly, forming a plateau which extends to 3.5 μm, after which the concentration rapidly decreases and reaches the Al-background level at 4.1 μm. This extended, almost box shaped, part of the profile is attributed to axial <0001> channeling and subsequent de-channeling of the implanted ions. The shapes of the Al_{lo} profiles with fluences of 0.66, 2.6, and 11×10^{12} cm^{-2} are close to identical, implying that the previously implanted ions have not significantly affected the crystalline structure of the sample, i.e., the so-called zero dose approximation is still valid. However, at an Al fluence between 11 and 26×10^{12} cm^{-2} a dependence of the preceding implanted ions on the profile shape starts to occur. This can be seen in a gradual saturation of the deepest channeled ions in favor of a new intermediate peak with a position that moves closer to the random peak with increasing fluence. At the highest fluence of 7.1×10^{14} cm^{-2} in the Al_{hi} sample, full saturation of the Al atoms beyond 2.5 μm is reached while the maximum concentration in the intermediate peak has grown substantially higher than the random peak. A qualitative explanation of this process is as follows. In the slowing down process of implanted ions lattice defects are generated which accumulate as the fluence is increased and eventually form a buried damaged layer. The probability that an initially channeled ion will be de-channeled by an implantation induced defect is small at low fluences, but as the fluence gradually increases, more and more channels will contain defects leading to a significant increase of the de-channeling in the buried layer. At some critical defect density (cm^{-2}), roughly on the order of the channel density [4], the fraction of de-channeled ions will be close to unity and, as the implantation proceeds even further, the depth at which this critical density is reached shifts towards the surface.

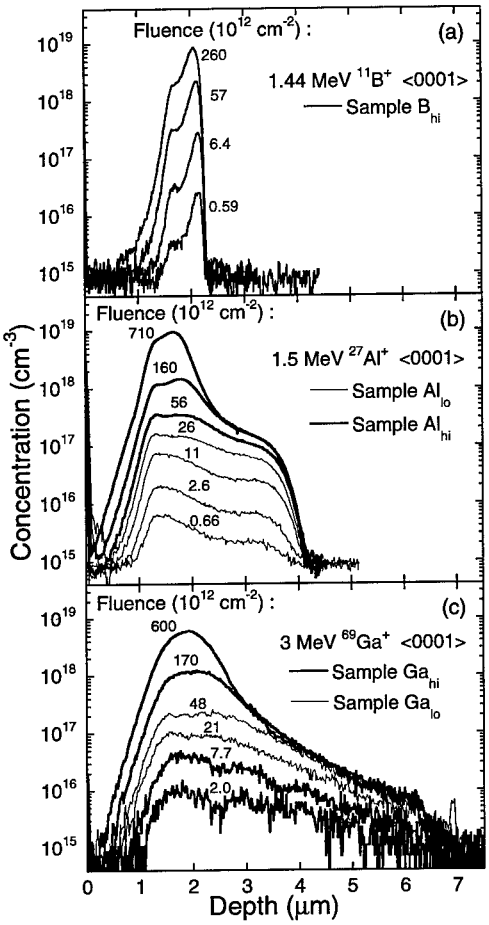

FIG. 1. SIMS profiles of 1.44 MeV $^{11}B^+$ (a), 1.5 MeV $^{27}Al^+$ (b), and 3 MeV $^{69}Ga^+$ (c) implanted in the <0001> axial direction of 6H-SiC at varying fluence. For Al and Ga, a saturation of the deepest channeled ions, in favor of an intermediate peak, is seen at the higher fluences. The shape of the B profiles is on the other hand almost unaffected by the implantation fluence.

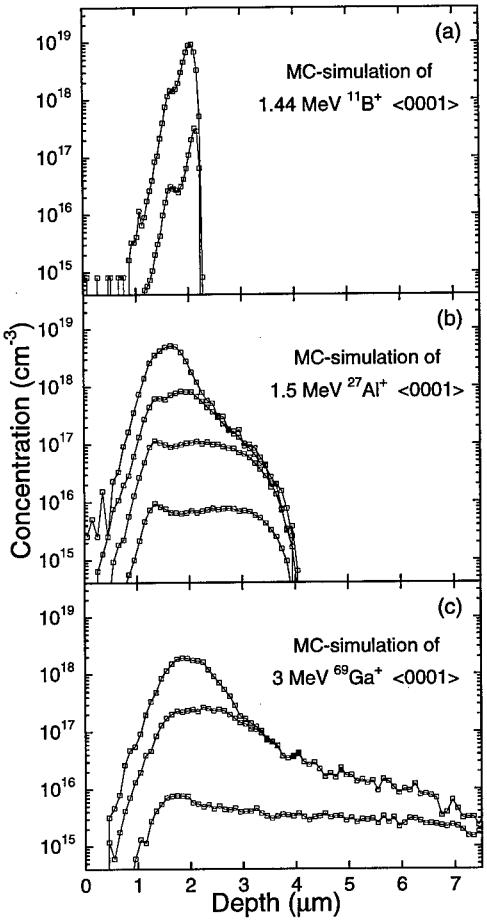

FIG. 2. Monte Carlo simulations of 1.44 MeV $^{11}B^+$ (a), 1.5 MeV $^{27}Al^+$ (b), and 3 MeV $^{69}Ga^+$ (c) implantations in the <0001> axial channeling direction of 6H-SiC. The simulated profiles are in good agreement with the experimental ones in Fig. 1. The fluence dependence was modeled using only one, semi empirical, fitting parameter.

The characteristic features seen in the Al implanted samples, i.e., the random peak and the fluence dependent deep channeled part of the distributions (Fig. 1b), are also found in the B_{hi}, and the Ga_{lo} and Ga_{hi} samples, Figs. 1a and 1c, respectively. When comparing the profiles of the three acceptors, two major trends are found. First, the relation between the range of the deepest channeled ions and the position of the random peak increases dramatically with increasing ion mass. This can be qualitatively understood by considering that a major difference in slowing down a channeled ion compared to an ion with a random trajectory is the absence of close encounter nuclear collisions. In other words, the nuclear stopping power is strongly reduced [3]. Since nuclear stopping only constitutes a very small part of the total stopping for random 1.5 MeV ^{11}B-ions while it is a major part in the case of 3 MeV ^{69}Ga ions [5], it follows that with the reduction of the nuclear stopping, the relative increase in penetration depth will be much larger for channeled Ga- than for B-ions. The second trend seen in Fig. 1 is that the influence of the implanted fluence on the ion distribution has

also a strong dependence on ion species. For Al and Ga a clear transition in the profiles is seen where the concentration of the deepest channeled ions saturates due to an effective defect induced de-channeling. The transition occurs at a lower fluence for Ga than for Al, and is completely absent for B where only a slight shift towards the surface, and a broadening of the channeled peak can be observed for the higher fluences. This is easily explained by the fact that the damage created per ion is larger for a heavy than for a low mass ion having the same energy.

In addition to the experiments, Monte Carlo simulations of the <0001> implantations have been performed using the binary collision approximation (BCA) and the full recoil cascade model [6]. The influence of crystal damage is treated by a statistical approach where the probability that an ion is randomly scattered by a defect is given by: $p = c_a N_d(z)/N_{SiC}$, where $N_d(z)$ is the accumulated point defect concentration at depth z and N_{SiC} is the atomic density of SiC. c_a is a semi empirical parameter which includes any deviation from the used target atom displacement energy threshold (25 eV for both Si and C), recombination and clustering, as well as the scattering efficiency of the point defects. The simulated distributions are plotted in Fig. 2 and are generally in very good agreement with the experimental profiles of Fig. 1. It is noteworthy that the fluence dependence in the implantations can be well reproduced using only one common fitting parameter for all three ions, namely $c_a = 0.5$.

SUMMARY

We have demonstrated the large influence of channeling in the <0001> direction of implanted ^{11}B, ^{27}Al, and ^{69}Ga in 6H-SiC. The experimental data give valuable information both about the electronic stopping power and the damage accumulation during implantation, and can be used for further calibration of ion implantation simulation tools. The presented results also suggest an interesting technological possibility, since the use of aligned implantations would provide deep, box-shaped dopant distributions including a high concentration surface peak, by a single implant only. This type of doping profile is commonly used in power-device applications and is usually accomplished by multiple implantations. Furthermore, Monte Carlo simulations suggest that the concentration of defects generated by an aligned implant is much lower compared to a standard multiple implantation in a random direction.

ACKNOWLEDGEMENTS

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Damage Reduction in Channeled Ion Implanted 6H-SiC

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Keywords: Channeling, Damage, Ion Implantation, Raman, SIMS, Simulation

Abstract: We compare damage effects of "random" (off-axis) and ⟨0001⟩ aligned implants of 1.5 MeV Al into 6H-SiC. Both channeled and random equivalent SIMS profiles have been used to adjust model parameters of the simulator. Depth resolved Raman measurements show that at ion doses below ~$5x10^{14}$ cm^{-2}, the integral damage is reduced by a factor of ~2.5 for the channeled implant. This confirms the corresponding reduction of defect concentrations predicted by simulations.

1. Introduction

The processing of SiC material is complicated because of the high temperature necessary for dopant diffusion. The formation of doped layer is achieved by epitaxial growth process, which do not allow planar selective area doping, essential for integrated circuits and device fabrication. Ion implantation represents the alternative technique to selectively dope SiC devices. However, ion beam irradiation damages the crystalline lattice and many aspects of the damaging process as for example the effects of the ion channeling on the resulting damage level have still to be clarified. Recent investigation [1] on implantation of Al into 6H-SiC indicate noticeable differences in the dopant distribution within the host crystal under random and channeling implant conditions.

The purpose of this contribution is to demonstrate the important reduction in defect concentration that appears in channeled ion implanted 6H-SiC. To this end several samples where implanted at different orientations from channeled ⟨0001⟩ to almost random. The impurity profiles were determined by using secondary ion mass spectroscopy (SIMS). This allows the calibration of the specific ion implantation simulator developed for SiC. The integrated implantation induced damage build up was followed by inelastic light scattering spectroscopy and compared with the reduction of defect concentrations predicted by simulation for channeled implants.

2. Experimental

We used n-type, nitrogen-doped, epitaxial 6H-SiC layer with a net doping concentration of $5x10^{15}$ cm^{-3} and a thickness of 10 μm grown on n^+ type, 3.5° off-axis. After a 380 Å thick sacrificial oxidation the samples were then placed in the Rutherford backscattering (RBS) chamber of a 6MV tandem accelerator. For channeling implants, the <0001> axis of the crystal was determined by performing angular scans, using a 2.4 MeV He^+ beam, around the expected longitudinal angle of 3.5°. The alignment was carried out as fast as possible in order to minimize the damage generated by the He beam. Once the <0001> axis was determined, the source was changed and Al was spot

implanted (ϕ~3 mm), at 1.5 MeV in the corresponding channeling direction. Due to the high energy used for the Al implantation, the critical angle for channeling is small and the channeled part of the profile disappears rapidly with increasing tilt angle. At this energy, near random implantation conditions are reached at relatively low tilt angles (2°).

The non-uniformity of the Al flux across the beam induces higher values of the implanted dose at the center of the implanted zone and lower values near the edge. The SIMS measurements provide almost local profiles since only the secondary ions coming from a circular region with a diameter of 60 μm are counted. By performing SIMS measurements at different points across the spot, it is possible to get three experimental depth profiles from a single implant process, each corresponding to a local implant dose. This is very interesting for channeling studies because the amount of channeling is strongly affected by the implantation dose due to the accumulation of radiation induced defects. In this way we were able to cover a dose range from 1.8×10^{12} cm^{-2} to 4×10^{14} cm^{-2}.

Raman measurements were performed at room temperature using a spectrometer coupled with an metalographic microscope that can be adjusted with an accuracy of 0.2 μm along the optical axis. For backscattering experiments in the (0001) face of 6H-SiC, with an extraordinary refractive index of 2.724 at a wavelength of 514.5 nm, we have estimated using the 100 μm pinhole a confocal depth resolution of ~6 μm.

3. Results and discussion

Fig.1 shows the distortion of the Al profile induced by channeling. The on-axis <0001> implantation is much deeper and wider (at least a factor of three) as compared to the random equivalent implant. The channeled implant at low doses (~3×10^{13} cm^{-2}) displays an almost square shaped Al profile with nearly uniform concentration of 10^{17} cm^{-3}. This plateau extends from the random peak depth located at 1.2 μm, corresponding to Al ions penetrating the crystal near the rows of atoms, to the channeling cut-off at about 4 μm, corresponding to the final stopping depth of well-channeled ions along <0001>. SIMS data have been the tool used to validate the simulation and analyze the different physical parameters that affect the implantation profile of channeled ions. We have found the following: a) The influence of the divergence δ of the implantation beam on the final Al distribution in the host crystal is almost negligible. This is because δ~0.02°, is much lower than the aperture angle of the channel. b) Thermal vibrations rise the stopping power of channeled ions by the atomic lattice. The best experimental fitting has been obtained taking for Si and C, atomic vibration amplitudes that are 20% larger than the ones reported from specific heat measurement [2]. This effective correction accounts for a possible deviation of the vibration amplitude from the experimental value as well as correlation effects of atomic displacements, which have not been considered in the simulation program. c) Although a careful cleaning of the surface has been performed before implantation, a thin layer always remains on the crystal surface. This layer increases nuclear stopping cross-section at the surface and reduces ion channeling. The best compromise has been obtained with an amorphous layer of 50 Å. d) Defects generated by He ions used for the ion beam alignment along the crystallographic c-axis have been estimated for a flux of $^4He^+$ of 2.4 MeV and 2×10^{15} cm^{-2}. The He penetration depth is about 5.75 μm, far away from the maximum depth achieved by Al implants. In the Al implanted zone the calculated Si interstitials concentration generated by the $^4He^+$ ions is almost uniform and reaches a relative value of ~10^{-3}, giving rise to a random collision probability of 10^{-3}. e) Finally, we have also taken into consideration the dechanneling due to defects induced by Al itself. The generation of defects is based on a threshold energy for atomic displacements within the independant full recoil cascades scheme. The random collision probability with previously generated defect is assumed to be proportional to the relative defect concentration in the lattice. In order to account approximately for

the uncertainty on the threshold energy, the possible recombination of point defects and the scattering efficiency of defects, a correction factor has been introduced, which value is 0.5. Taking into account all these parameters in the simulation program we obtain the Al depth profiles shown in Fig. 1. The simulation fits well to experimental SIMS data.
A test to validate the code is to simulate other physical processes in the Al implantation. One of the most interesting for electronic applications is the knowledge of profiles of displaced Si atoms after random and aligned Al implants. The results of simulations are shown in Fig. 2 for the random and aligned implantation specified in Fig. 1. Each implanted Al displaces ~10^3 atoms of Si. Notice that if we normalize calculation results to the same implant dose, the integral damage is reduced by a factor of 1.7 for the channeled implant. This lower defect generation is due to the higher values of impact parameters involved in channeled implants. It should enhance electrical activation during subsequent annealing process.

In order to confirm the reduction of defect concentration predicted by simulation, we have performed Raman measurements. In a previous work [3], it has been shown that the disorder induced changes in the absorption coefficient of the implanted layer can be obtained from the depth profiling of the 966 cm^{-1} LO mode intensity of the undamaged portion of the epilayer using a confocal microprobe set-up. Fig. 3 selects representative Raman spectra from the random and aligned implanted samples. They have been taken, across the surface of the implantation spot, close to the center and midway between the center and the border of the implanted zone. Performing a transversal mapping of the implantation spot we clearly distinguish between two different regions. First, the outside part of the implantation spot, were the implantation doses and the corresponding induced damage is low. Here, the surface region has a low optical absorption and is transparent to the incident laser light which simultaneously probes the damaged layer and the undamaged substrate. At the center of the implantation spot, the optical absorption coefficient increases up to values above $10^4 cm^{-1}$, due to the high damage level induced by the high implantation doses, and the laser light probes only the damaged layer. We have then analyzed the changes in the LO integrated intensity as a function of the Z scan position using the confocal diaphragm. Focusing the incident light well inside the sample volume at the point of maximum fluence of the implantation spot, we obtain for the random implanted sample Raman spectra with almost no background and weak but well defined TO and LO signals. On the contrary, performing the same kind of analysis on channeled implants, we find a progressive weakening of the TO and LO intensities with deepness. This strong optical absorption is related to the presence of a high damaged and absorbing layer provoked by the He ion beam alignment. To eliminate the absorption of this layer we have performed Raman measurements taken at the bottom of the SIMS craters (etch depth > 4 μm). The relative Raman intensity reaches a constant value when the light is focused behind the implanted layer. The associated value of the integral absorption is related to the number of structural defects of absorbing centers in the implantation process [4]. We have compared the absorption evaluated for the random and implanted samples, once the He induced absorption has been subtracted. For an implantation dose of 1x $10^{14} cm^{-2}$, we obtain 1.21 and 0.46 for the random and channeling samples, respectively. For a lower implantation dose of 3x$10^{13} cm^{-2}$, the integrated damage attains 1.05 and 0.38, respectively. In both cases we find that the integrated absorption obtained from the optical parameters is reduced by a factor close to 2.5 for the channeled implant, in fairly good agreement with the integrated damage evaluated from Monte Carlo simulation within the binary collision approximation (MC-BCA).

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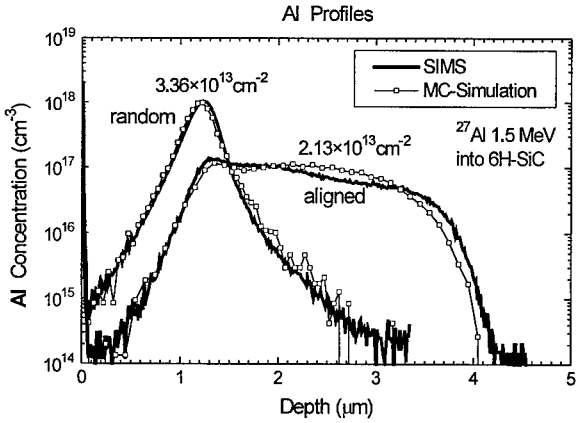

Figure 1: SIMS depth profiles (continuous line) and MC simulations (squares) of aligned and random equivalent implantations of $^{27}Al^{+}$ into 6H-SiC.

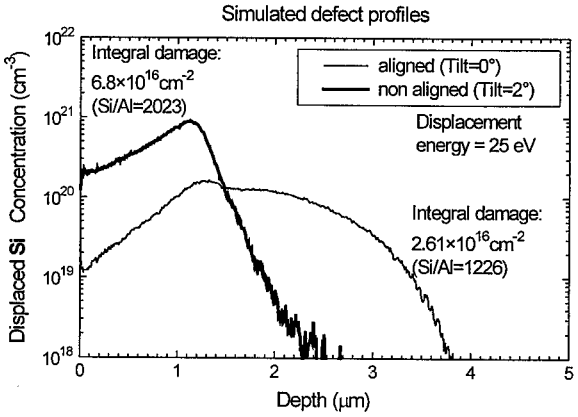

Figure 2: Simulated depth profiles of displaced Si atoms for aligned and random equivalent implantations of $^{27}Al^{+}$ into 6H-SiC.

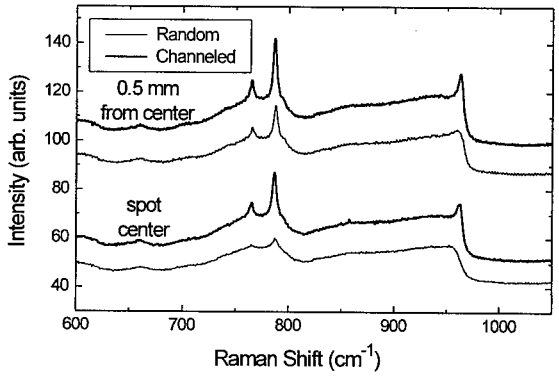

Figure 3: Raman spectra at different radial positions on the random and <0001> channeled implantation spots.

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Ion Beam Induced Nanocrystallization of SiC

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Keywords: Amorphization, Ion Implantation, Recrystallization

Abstract

Ion-beam-induced crystallization (IBIC) was used to produce nanocrystals in the preamorphized region of a 6H-SiC bulk crystal. The precipitation was stimulated by high dose implantation with Al and Si at temperatures between 300 °C and 700 °C. The morphology of the nanocrystalline phase and its dependence on the implantation parameters were investigated by cross-sectional transmission electron microscopy (XTEM). Above a certain threshold dose, randomly oriented grains of 3C-SiC with almost spherical shape and mean diameters ranging from 4 to 25 nm are formed. The recrystallization is completed within a very narrow time window. Therefore, in our experiments the nucleation and growth process could not be observed directly. From the extrapolation of the kinetics of the secondary grain growth to zero time the window of suitable parameters for the observation of nucleation and primary grain growth was estimated. A critical temperature ($T_C \leq 300$ °C) as well as an incubation time ($t_I \geq 300$ s below 700°C) for the beginning of the recrystallization were found.

1. Introduction

Nanocrystalline materials have attracted considerable interest during the last few years. The reduced size of the crystallites causes changes in their optical, mechanical and thermodynamic properties with respect to the bulk material [1]. In the case of silicon carbide, with its low atomic mobilities and high thermal crystallization temperature, it has also been shown that ion implantation can stimulate the crystallization process [2]. In addition to the epitaxial regrowth at the amorphous/crystalline (a/c) interface, the formation of nanocrystals in the amorphous surface layer was found after 300 keV Si^+ implantation at 480 °C. However, there have been no systematic investigations of ion-beam-induced nucleation and grain growth in amorphous SiC up to now. In particular, the critical parameter range for the onset of the crystallization and the kinetics of the process is unknown. Therefore, in this investigation the dependence of the crystallization process on the implantation parameters has been studied.

2. Experimental

Single-crystalline 6H-SiC wafers with 3.5° off-axis (0001) orientation were used as substrate material. To prevent the possible influence of the a/c interface on the recrystallization a 1.8 μm thick amorphous surface layer was generated by 2 MeV Si^+ implantation at room temperature. The crystallization was stimulated by high dose 300 keV implantation of Al (R_P=350 nm) and Si (R_P=308 nm) in a dose range from 3×10^{15} to 3×10^{17} cm^{-2} at temperatures from 300 to 700 °C. The morphology and mean grain sizes of the nanocrystalline phase were investigated by cross-sectional transmission electron microscopy (XTEM).

3. Results and discussion

3.1 Morphology

As demonstrated in Fig. 1, recrystallization is observed in the irradiated regions of the amorphous layer already at an implantation temperature of 300 °C, well below the SiC thermal recrystallization temperature of about 800 °C [3]. It is evident from the halo in the selected-area

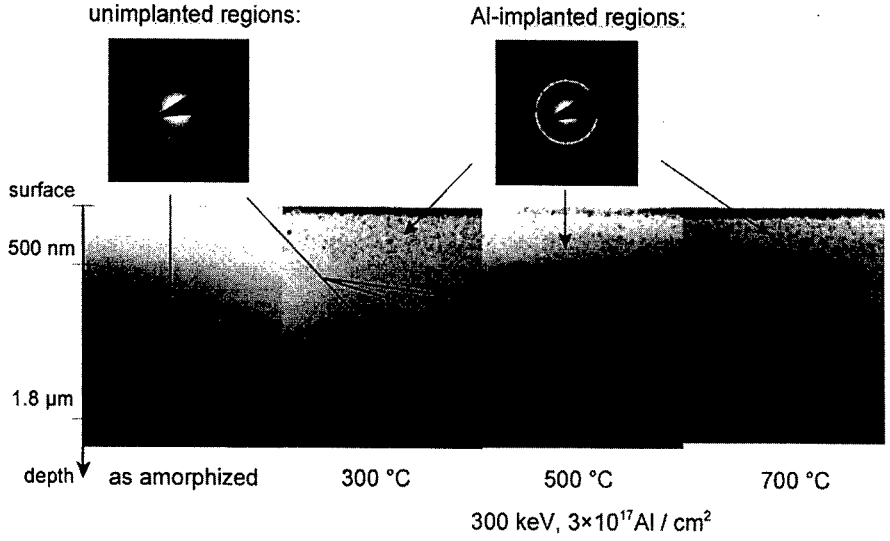

Fig. 1 Cross-sectional TEM micrographs of as-amorphized and Al-implanted a-SiC layers. The corresponding diffraction patterns of the Al-implanted and unimplanted regions are shown above.

diffraction pattern in Fig. 1 that the unimplanted region remains amorphous up to implantation temperatures of 700 °C. This clearly demonstrates that ion beam irradiation strongly enhances the kinetics of the amorphous to polycrystalline phase transition in SiC. After ion-beam-induced crystallization (IBIC), the morphology of the recrystallized material completely differs from that after thermal crystallization [4,5]. Thermal annealing above 800 °C results in a mixture of columns of hexagonal SiC and twinned 3C-SiC regions in the recrystallized layer. After IBIC, SiC grains with almost spherical shape are formed in the implanted regions. The diameter of the grains shown in Fig. 1 ranges from 5 to 20 nm. The rings in the selected-area diffraction pattern (Fig. 1) of the implanted region clearly show the polycrystalline structure of the recrystallized layer. Halo patterns corresponding to amorphous SiC are not observed in this region, indicating that the implanted layer is completely recrystallized. The measured radii of the diffraction rings correspond to the interplanar spacings of the cubic 3C-SiC polytype. Because of the small selected area (⌀=250 nm) of diffraction, the number of contributing particles is relatively small. Therefore, single spots are observed. Their homogeneous distribution over the rings indicates that there is no preferential orientation of the nanocrystals.

3.2 Kinetics

The transformation from the amorphous to the polycrystalline state is a very complex process consisting of three subprocesses. (1) It starts with nucleation which is characterized by a time lag (also called incubation time t_l) and a nucleation rate. In this transformation stage the system is defined by the density of nuclei n and the mean grain size d. (2) In the primary growth process, the nuclei grow with

a certain rate. After the complete transformation of the amorphous material this state is characterized by the mean grain size

$$d_0 = (\frac{6}{\pi} \times \frac{1}{n})^{1/3} . \quad (1)$$

(3) The mean grain size increases by secondary grain growth (ripening) due to grain boundary motion. In the pure thermal case all processes depend on temperature T. However, in the case of IBIC the ion flux j and nuclear damage are additional parameters of the processes. In order to determine the complex kinetics, the observation of isolated grains in the amorphous matrix is necessary. Unfortunately, we only observe either almost completely recrystallized (shown in Fig. 1) or still amorphous layers.

In Fig. 2, the mean grain sizes d of the recrystallized layers are plotted as a function of the implantation time for different temperatures T and ion fluxes j. For a fixed parameter set (ion flux and temperature) only two experimental results are available. Therefore, the data were fitted by linear functions. A consistent description of the data was obtained by the formula

$$d(\Phi,j,T) = 1.3\times10^{-13} cm^2 s \times j \times \exp(\frac{45meV}{kT}) + 3.6\times10^{-3} s^{-1} \times \exp(\frac{-82meV}{kT}) \times \frac{\Phi}{j} \quad (2)$$
$$for\ T>T_C\ ,\ t>t_I\ .$$

The activation energies are much smaller than in the pure thermal case [3]. Since the time for completion of crystallization is much shorter than the implantation time, the first term in Eq. 2 corresponds to the mean grain size d_0. From this value d_0 the grain density n, which is inversely proportional to the nucleation rate can be calculated (Eq. 1). It increases with decreasing ion flux and increasing temperature. This is in agreement with results of ion beam induced nucleation in Si [6, 7]. The second term in Eq. 2 describes the ripening of the grains under ion irradiation. The velocity of this secondary growth increases with temperature. This is in agreement with the results of secondary grain growth in Si and Ge [8]. In most Si experiments the growth rate was found to be a sub-linear function of the ion dose Φ. Such a behavior cannot be excluded from our results, since the linear behavior is only due to the linear fit of the data points.

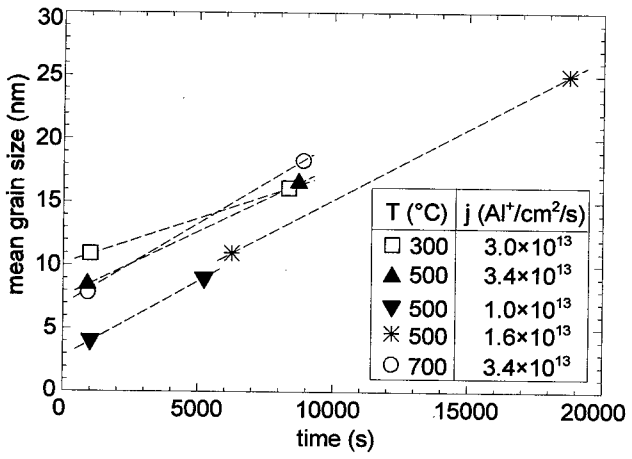

Fig. 2 Dependence of the average grain size of the polycrystalline layers on the time at several temperatures and ion fluxes.

No crystallization was found after implantation of 1×10^{16} Al/cm^{-2} at 500°C although in the case of Si implantation under very similar conditions the layer is completely recrystallized. This is surprising, because there is only a minor difference between the nuclear damage energy profiles for 300 keV Al and Si implantation. The experimental parameters differ only in the used ion fluxes. Because of the higher ion flux, the irradiation time is 300 s for Al irradiation instead of 1000 s for Si. From this result it can be concluded that the incubation time

is longer than 300 s at 500°C. This incubation time decreases with increasing temperature and is reduced to less than 100 s at 700 °C. It is clear that there exists a critical temperature T_C, below which crystallization cannot be achieved. From the IBIEC/IBIIA-transition a very similar critical temperature is known, which increases with increasing ion flux [9, 10]. In our IBIC experiments we found recrystallization for 300 keV Si and Al implantation even at 300°C. This means that the critical temperature should be lower under these irradiation conditions. Our results are in agreement with the critical temperature of amorphization reported in the literature ranging from 130 to 370 °C [10, 11]. Because we did not find isolated grains in our experiment, it was not possible to determine the rates of nucleation and primary grain growth as a function of the implantation parameters. However, our results show that this stage could be achieved at 500°C after implantation times between 300 and 1000s. But at this temperature the grains are always smaller than 4 nm and difficult to observe in XTEM. According to our results, larger grains can be achieved at lower temperatures ($T_C < T < 300$°C) which demands longer implantation times due to the longer time lag.

4. Conclusions

The recrystallization behavior of amorphous SiC layers under high dose implantation with Al and Si was investigated by XTEM. The results show that ion irradiation strongly enhances the recrystallization process in a-SiC already at 300 °C, well below the thermal recrystallization temperature of about 800 °C. Randomly oriented grains of 3C-SiC, with almost spherical shape and mean diameters ranging from 4 to 25 nm, were formed during implantation. It was found that there is only a narrow time window for the observation of nucleation and primary growth. From the extrapolation of the kinetics of the secondary grain growth this time window was estimated.

Acknowledgments

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High Temperature Implant Activation in 4H and 6H-SiC in a Silane Ambient to Reduce Step Bunching

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Keywords: Anneal, Ion Implantation, Silane overpressure

Abstract The mechanical strength of silicon carbide does not permit the use of diffusion as a means to achieve selective doping as required by most electronic devices. While epitaxial layers may be doped during growth, ion implantation is needed to define such regions as drain and source wells, junction isolation regions, etc. While ion implantation has been studied in all of the silicon carbide polytypes, ion activation has resulted in serious crystal damage as these activation processes must be carried out at temperatures on the order of 1600°C. Ion implanted silicon carbide that is annealed in either a vacuum or hydrogen environment usually results in a surface morphology that is highly irregular due to the out diffusion of Si atoms. We have developed and report a successful process of using silicon overpressure, provided by silane in a CVD reactor during the anneal, to prevent the destruction of the silicon carbide surface. This process has proved to be robust and has resulted in complete ion activation at a annealing temperature of 1600°C.

Introduction

Silicon carbide is an ideal semiconductor for high-power and high-temperature applications due to the high level of material stability at elevated temperatures. This high degree of mechanical stability, while it lends itself well to these applications, makes the formation of device structures that require selective area doping difficult. Indeed, SiC is primarily an epitaxial technology where ion implantation is used to selectively dope regions in the epitaxial layer to implement a specific device structure. Although dopant diffusion is the preferred process in silicon technology to achieve selective doping, diffusion rates in SiC are simply too low to permit this approach.

Ion implantation in SiC has been demonstrated to be a suitable means for achieving degenerate doping densities for both p and n-type material with reasonable ion flux [1]. Unfortunately, the high bonding strength of the SiC lattice requires not only that the implant be carried out at elevated temperatures [1] but that the implant anneal be performed in excess of 1600 °C if full doping activation is to be achieved. It is widely believed that the degradation of the silicon carbide material surface after implant annealing is one reason responsible for MOSFET inversion layer carrier mobilities of less than 10 cm^2/V-s in 4H-SiC, a serious problem leading to unacceptable on-state resistances in these power devices [2]. As a consequence, the highest mobility MOSFET devices reported in SiC are either buried channel devices [3] or devices with a low thermal implant activation temperature [4] which also increases the series resistance in the drain and source regions. While the SiC lattice is inherently stable at lower temperatures, Si can out diffuse at elevated temperatures leading to a severe degradation in the surface morphology known as step bunching [5].

Numerous researchers have reported work on annealing SiC with various encapsulants which suppress the out diffusion of Si during the annealing process **[6,7]** but require that the encapsulating material be removed prior to continuing device fabrication.

Ion Implanted 4H-SiC samples

Two sets of samples were investigated during the course of this experimental study. The first was provided by Purdue University and contained an n-type epitaxial layer with a doping density in the mid 10^{15} cm^{-3} range. Samples provided for implant annealing were implanted with both Al and B and were of the 4H and 6H polytype. The second set of samples, the majority of which is discussed here, were composed of a 6 μm n-type epitaxial layer grown by the Emerging Materials Research Lab with a doping density in the mid 10^{15} cm^{-3} range. A single epitaxial layer was grown on 4H-SiC (8° off-axis) and the sample diced into 5 mm squares to permit numerous implant studies to be conducted on epitxial layers of the same doping and thickness. A typical implant Al profile is shown in Fig. 1. Implants were carried out at 700°C through a 110nm Mo mask layer in order to implant the near surface regions of the SiC epilayers. Molybdenum does not react with SiC at the implant temperature, and following implantation, the mask layer was etched away prior to further processing. The AFM photograph in Fig. 2 shows that the surface of the epilayer is somewhat degrade by the implant process. However, bulk crystalline quality is well preserved, as indicated by the ion channeling spectra. These spectra were generated using standard Rutherford backscattering techniques and 2MeV He^{+} ions scattered at 170° to the direction of the incident beam.

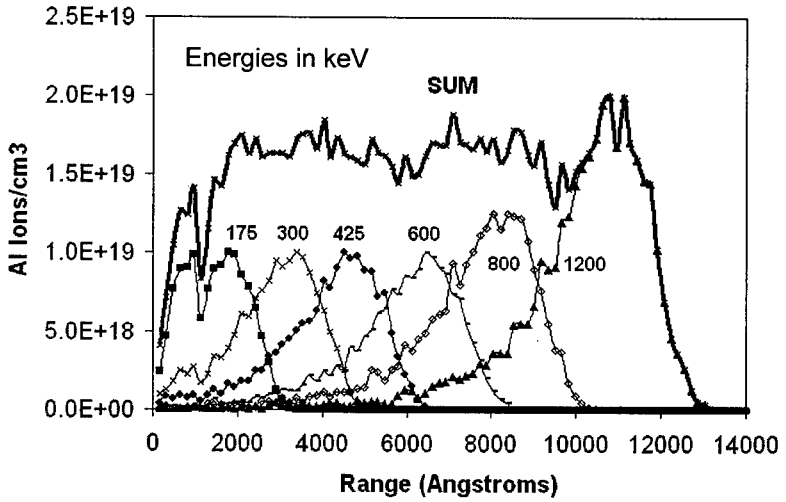

Figure 1 Implant schedule used for the implant anneal studies. Al was implanted at 700°C. Multiple implants starting at 175 keV used to achieve the box profile shown (SUM in fig.).

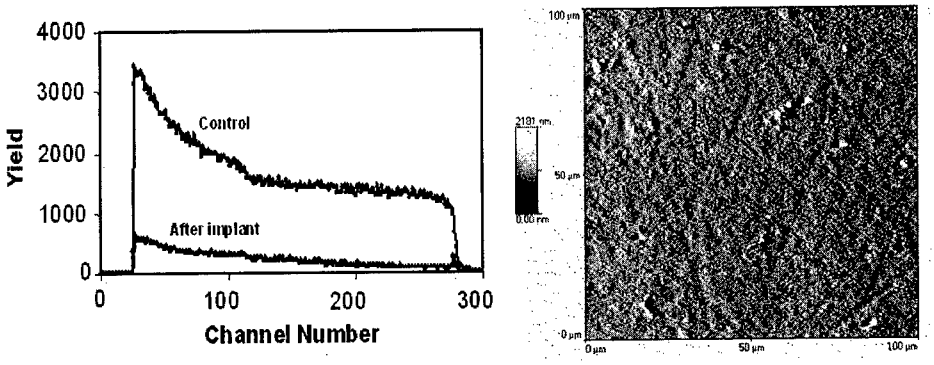

Figure 2 Channeling RBS and AFM data of 4H-SiC implanted with Al at 700°C. Note the crystal quality is degraded due to implant damage, as expected.

Silane Overpressure Annealing Experiments

A silane-based CVD reactor suitable for performing high-temperature anneals in a silicon rich ambient was used for these experiments. Annealing temperatures in excess of 1700 °C are possible by placing the sample to be annealed on a SiC coated graphite susceptor and heating the graphite using an RF induction coil, as has been discussed elsewhere for CVD growth of SiC epitaxial layers [8]. Preliminary experiments were conducted on Al and P implanted samples at 1600 °C at atmospheric pressure and under various silane flow conditions. Both a 3% silane in UHP hydrogen gas flow of 5 to 20 sccm were used to characterize the surface morphology as a function of silane flow. Prior to annealing the material was n-type with a doping density of 4-5E15 cm^{-3}. After annealing the doping density was observed to be in excess of 1E19 cm^{-3} at the surface and was observed to be p-type. Unfortunately the method, using UHP hydrogen, did not result in a repeatable process.

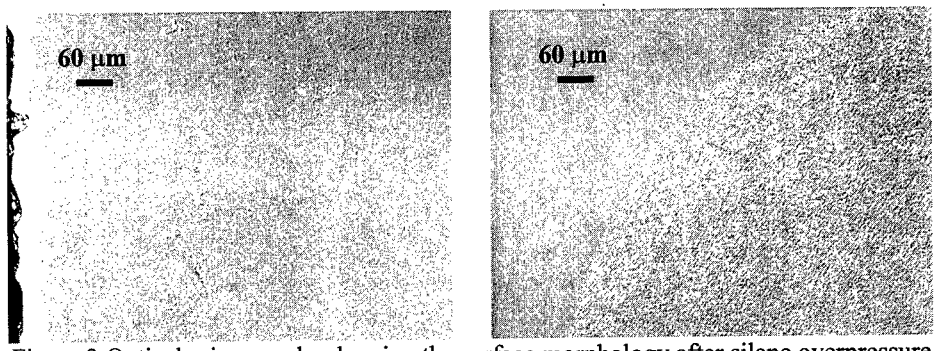

Figure 3 Optical micrographs showing the surface morphology after silane overpressure annealing in SiH_4/H_2. Step bunching was observed to occur on numerous occasions motivating the development of a SIH_4/Ar process.

Since H_2 is known to etch SiC at the temperatures required to anneal the implant, experiments using silane in argon (3% silane in 97% UHP Ar) were conducted and a process schedule established using this process chemistry. Since Ar does not etch SiC the concentration of Si in the reactor during annealing can be varied such that an optimum process is achieved. Figure 4 shows the surface morphology of Al implanted n-type 4H-SiC after annealing. Note that the surface morphology was not affected during the annealing process, indicating that a sufficient overpressure of Si was present during the anneal.

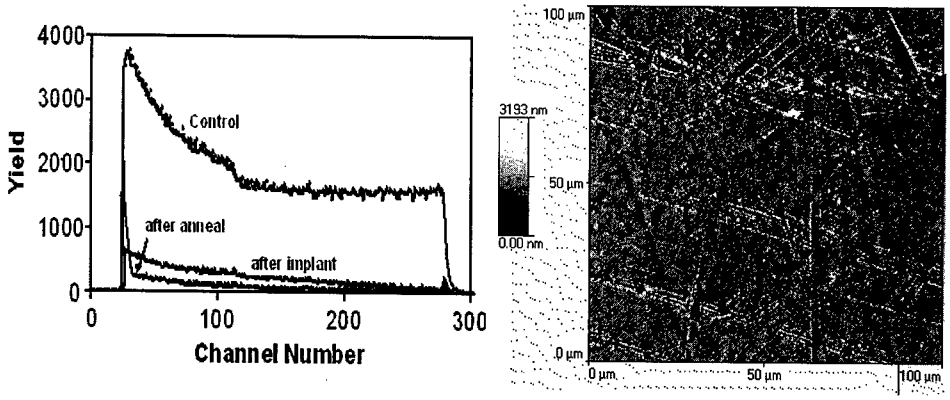

Figure 4 Channeling RBS and AFM data of 4H-SiC annealed using the Silane/Ar process. Note crystal damage from implant has been repaired.

The final process schedule developed during this research is as follows. After a 1 slm UHP Ar flow is established in the reactor, the RF generator is turned on and the susceptor heated to the annealing temperature. The silane in Ar gas flow of 20 sccm is not initiated until a substrate temperature of 1490°C is reached to suppress Si droplet formation. After the annealing temperature of 1600°C is reached the 30 minute anneal is conducted. At this point the reactor is purged of silane by simultaneously turning off the silane in Ar flow (3 slm UHP Ar flow remains on) and the setpoint temperature is reduced to 1400°C. After one minute, the RF generator is turned off and the sample cooled to room temperature under Ar flow.

Summary

Implant anneal experiments were performed to develop a process schedule for silane overpressure annealing of ion implanted SiC. In an effort to develop an optimum process with the smallest number of experiments, the same annealing temperature was used for all the studies conducted (1600 °C). The initial process used available silane in UHP H_2 of varying flow rates. While some success was achieved with this approach, the process proved to be sensitive to annealing conditions and step bunching was observed on most samples after annealing. Since H_2 is known to etch SiC at the temperatures needed to activate the implant, a silane in UHP Ar process was established with the process schedule shown to be robust and provide fully activated implants with no loss of crystal structure. Measurement of the free carrier mobility is now being conducted as well as selective ion implantation which is critical to advanced devices in SiC technology.

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Characterization of Implantation Layer in (1$\bar{1}$00) Oriented 4H- and 6H- SiC

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Keywords: (1$\bar{1}$00)-oriented, Ion-Implantation

Abstract: The polytypic structure of implanted layers in (1$\bar{1}$00)-oriented 4H- and 6H-SiC has been investigated using Rutherford backscattering spectrometry (RBS) combined with channeling technique and cross-sectional transmission electron microscopy (XTEM). The (1$\bar{1}$00) oriented 4H- and 6H-SiC have been implanted with 400 keV Al ions to a dose of 2×10^{15} /cm^2 through a 550 nm thick SiO_2 layer and 400 keV Ga ions to a dose of 5×10^{15} /cm^2 through a 200 nm-thick SiO_2 layer,respectively, at room temperature. In both Al and Ga implanted (1$\bar{1}$00) oriented SiC, the implantation-induced amorphous layer are recrsytallized by annealing above 1500 °C for 30 min, respectively, with good crystalline quality. The XTEM investigation reveals that the amorphous layer in Ga implanted SiC(1$\bar{1}$00) is regrown in accordance with the polytype of substrate

1 Introduction

The wide gap semiconductor SiC has been of great interest as a material for power control and high-speed communication devices because of its high-breakdown field strength and high saturation velocity of the carriers. The ion implantation is an important technique for the fabrication of contact regions in devices since the diffusivity of impurities in SiC is negligibly low below 1800 °C[1].

In (0001)-oriented SiC with a large amount of implantation damage, the post-implantation annealing leads to a regrowth inducing various polytype crystals[2]. The formation of other polytype crystals may be caused from the random rearrangement of atoms at the interface between regrown and residual amorphous layers where the atomic stacking sequence of the original polytype disappears. To prevent the random regrowth of polytype crystals, the implantation process is performed at elevated substrate temperatures.

In this study, we propose the ion implantation to (1$\bar{1}$00)-oriented SiC to preserve the polytypic structure of implanted layer. The atomic stacking sequence of the polytype lies along the <0001> axis on the (1$\bar{1}$00) plane of SiC. In the crystal growth on the (1$\bar{1}$00)-oriented SiC, the polytype of the grown crystal depends on the polytype of the seed[3], whereas in the case of crystal growth of (0001)-oriented SiC, polytypes of SiC tend to mix during the growth even if the growth conditions are optimized[3,4].

It is expected that the crystallographic feature of (1$\bar{1}$00) plane is useful for the preservation of polytypic structure in implantation processes. We show that the implantation-induced amorphous layer of (1$\bar{1}$00)-oriented SiC is recrystallized to the original polytypic structure without the regrowth of other polytype crystals such as 3C.

2 Experiments

The samples used in this study were (1$\bar{1}$00)-oriented 4H-SiC and (1$\bar{1}$00)-oriented 6H-SiC crystals cut from (0001)-oriented crystals grown by the sublimation method. Al ions were implanted into (1$\bar{1}$00)-oriented 4H-SiC through a 550 nm thick SiO_2 layer at an energy of 400 keV and a dose of 2×10^{15} /cm^2. Ga ions were implanted into (1$\bar{1}$00)-oriented 6H-SiC through a 200 nm-thick SiO_2 films at an energy of 400 keV and a dose of 5×10^{15} /cm^2, respectively, at room temperature. The SiO_2 layers were formed to amorphize the surface layer of SiC substrate because the lowest energy of our implanter is 400 keV. The projection range and

standard deviation of ions were estimated to be 550 and 110 nm for the implanted Al ions and 220 and 55 nm for implanted Ga ions, respectively, using a simulation developed by Zeigler et. al[5]. The implanted Al and Ga ions distribute around the interface between SiC and SiO_2. The effective dose of Al and Ga ions to the SiC substrate was estimated to be 1.2×10^{15} and 3.5×10^{15} /cm^2, respectively. The oxide layer was removed by HF acid before the annealing process. To compare the recrystallization process between $(1\bar{1}00)$- and (0001)-oriented crystals, the Ga ion implantation to (0001)-oriented 6H-SiC, which was supplied from Cree Research, was also performed under the same condition.

Annealing of implanted samples was performed at temperatures ranging from 1200 to 1700 °C for 30 min in Ar ambient using an infrared image annealer with a black SiC crucible. In the annealing process, the surface of sample is not protected by a passivation layer beacause the surface of sample contacts to the used SiC crucible. The heating slope was about 75 °C per second. The crystallinity of the implanted layers was evaluated using both Rutherford backscattering spectrometry (RBS) combined with channeling technique and cross-sectional transmission electron microscopy (XTEM) with an electron energy of 200 keV. RBS measurements were carried out using 1.5 MeV $^4He^+$ ions with a scattering angle of 150°. To determine the polytype of the implanted layers, transmission high-energy electron diffraction (THEED) was performed with the incident beam along the $<11\bar{2}0>$ axis using a transmission electron microscopy.

3 Results and Discussion

Figure 1 shows the RBS spectra for Al ion implanted 4H-SiC$(1\bar{1}00)$ samples. The amorphous layer with a thickness of 120 nm was formed in the surface region (spectrum B). The amorphous layer was recrystallized by annealing at 1200 °C (spectrum C). The increase of the yield at 260 channel was observed at a depth corresponding to the end-of-range of implanted Al ions. The end-of-range damage has been often observed in the implanted Si. The end-of-range damage was annealed out by annealing at 1500 °C (spectrum D). For the sample annealed at 1500 °C, the normalized minimum yield (χ_{min}) was estimated to be 8.5 % around 275 channel, while the χ_{min} value for unimplanted sample was about 3.0 %. Figure 2 shows the RBS spectra for Ga ion implanted 6H-SiC$(1\bar{1}00)$ samples. The amorphous region with a thickness of 200 nm was formed at the surface region(spectrum B). As observed for the Al implanted sample, the amorphous region was recrystallized by annealing at 1200 °C. In the sample annealed at 1500 and 1700 °C, the χ_{min} values were estimated to be 8.0 % and 6.8%, respectively. The photograph in figure 2 shows the TEM image of the sample annealed at 1500 °C. There is no secondary defect in the implanted layer. The region from surface to the depth of 100 nm is related to the distribution of the implanted Ga impurities[6]. It has been reported that the implanted Ga impurities redistribute to the surface and then evaporate from the surface accompanied with the improvement of the crystalline quality due to the increase of the annealing temperature[6,7]. For both Al and Ga implanted $(1\bar{1}00)$-oriented SiC, the amorphous region was recrystallized with a good crystalline quality. It is suggested that in the implantation to $(1\bar{1}00)$-oriented SiC, the implantation-induced amorphous region is recrystallized in accordance with the polytype of the substrate.

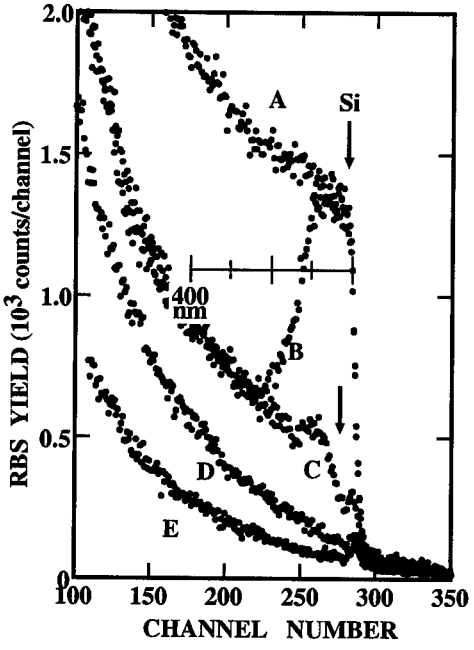

Figure 1: RBS spectra obtained from the Al ion implanted $(1\bar{1}00)$-oriented 4H-SiC. A: random spectrum, B: aligned spectrum for as-implanted sample, C and D: aligned spectra for samples annealed at 1200 and 1500 °C for 30 min, respectively, E: aligned spectrum for unimplanted sample.

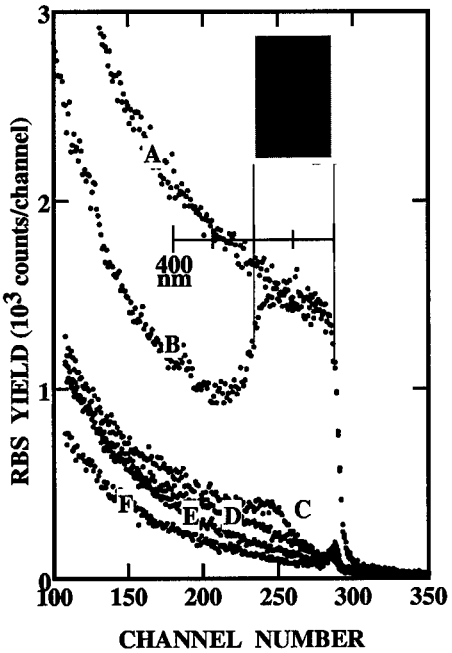

Figure 2: RBS spectra obtained from the Ga ion implanted (1$\bar{1}$00)-oriented 6H-SiC. A: random spectrum, B: aligned spectrum for as-implanted sample, C, D and E: aligned spectra for samples annealed at 1200, 1500, and 1700 °C for 30 min, respectively, F: aligned spectrum for unimplanted sample. The photograph is TEM image obtained from the sample annealed at 1500 °C.

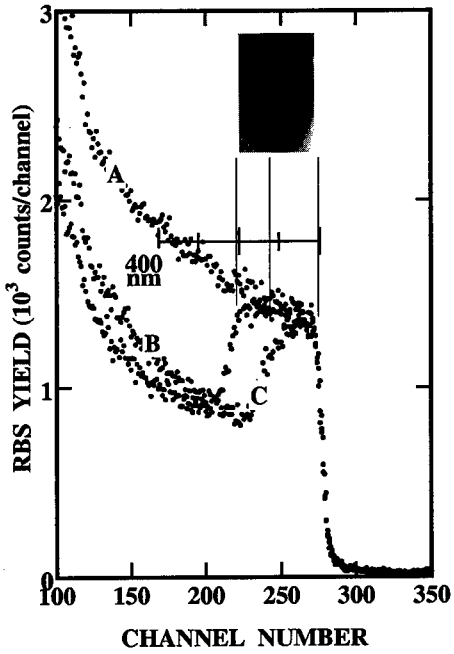

Figure 3: RBS spectra obtained from the Ga ion implanted (0001)-oriented 6H-SiC. A: random spectrum, B: aligned spectrum for as-implanted sample, C: aligned spectra for samples annealed at 1500 °C for 30 min, The photograph is TEM image obtained from the sample annealed at 1500 °C.

The recrystallization process of implanted layers in (1$\bar{1}$00)-oriented SiC is obviously different from that for the implanted layer in (0001)-oriented SiC. Figure 3 shows the RBS spectra for Ga implanted 6H-SiC(0001) samples. In the sample annealed at 1500 °C, a highly defective region with a thickness of 100 nm still remained (spectrum C). The implanted layer contains many secondary defects as shown by TEM observation for the sample annealed at 1500 °C(see photograph in figure 3). As described later, this highly defective region contains the 6H and 3C polytype crystals, which arises from the random arrangement of Si and C atoms during the regrowth. The high aligned yield of this region is due to the direct scattering from the interface between 6H and 3C crystals and other defects in the implanted layer.

The polytypic structure in the implanted layer can be evaluated by THEED with the incident beam along the <11$\bar{2}$0> axis. Figures 4 (a) and (b) show the THEED patterns from implanted and underlying substrate regions, respectively, for the Ga implanted-(1$\bar{1}$00) SiC annealed at 1500 °C. The THEED pattern from the substrate is identified to be 6H-polytype[8]. The THEED pattern from the implanted region is consistent with that from the substrate region. It is concluded that the implanted layer is regrown with the original polytypic structure of 6H. In the (0001)-oriented sample, however, the polytypic structure is not reproduced. Figures 4(c) and (d) show the THEED patterns from implanted and underlying substrate regions, respectively, for the (0001)-oriented SiC annealed at 1500 °C. The THEED pattern from underlying substrate region (Fig. 4(d)) shows the 6H-polytype. The THEED pattern from implanted layer in (0001)-oriented sample consists of the diffraction from twined 3C polytype crystals[8] (A and B in Fig. 4(c)) superimposing on the THEED patterns from the original 6H polytype crystals, as assigned in Fig. 4(c). Furthermore, the diffraction indicated as symbol X

in Fig 4(c) was observed. This diffraction has the plane spacing equivalent to (111) plane in the direction equivalent to (511) plane in "A" 3C-SiC crystal. Therefore, the diffraction referred as symbol "X" is attributed to the twin defect in the zinc-blende structure, that is, 3C-SiC. The twin defect in 3C-SiC has been observed in the 3C-SiC crystal grown by direct carbonization method[9]. The detailed discussion for the THEED patterns will be published elsewhere.

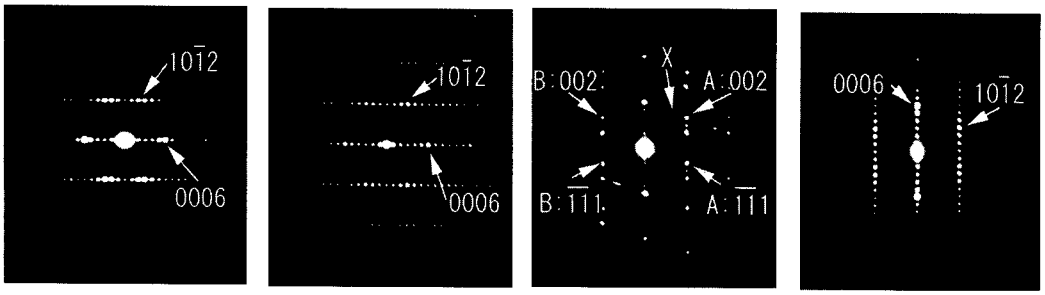

Figure 4: THEED patterns from the implanted layer and the underlying substrate in the sample annealed at 1500 °C. (a) implanted layer and (b) substrate region in $(1\bar{1}00)$-oriented 6H-SiC. (c) implanted layer and (d) substrate region in (0001)-oriented 6H-SiC. In the pattern from implanted layer in (0001)-oriented SiC, the twined 3C-crystals, A and B, are observed.

As described in previous paper[6], in the $(1\bar{1}00)$-oriented SiC, the atomic stacking sequence of the polytype is preserved in the interface between the implantation-induced amorphous layer and the underlying substrate (a/c interface). Therefore, the amorphous layer can recrystallize to the original polytypic structure. However, in the (0001)-oriented SiC the preservation of the polytypic structure at the a/c interface was disturbed by the ion-implantation, resulting in the regrowth of 3C-SiC including twin defect and 6H-SiC. We strongly suggest, therefore, that the implantation to $(1\bar{1}00)$-oriented SiC is useful to fabricate the heavily doped layer by the ion-implantation.

4. Conclusion

In Al and Ga ion implantation to $(1\bar{1}00)$-oriented SiC, the implanted layer was recrystallized in accordance with the polytypic structure of the underlying substrate and contains no detectable secondary defects which can be seen in the implanted 6H-SiC(0001). The regrowth process of amorphous layer strongly depends on the orientation of the substrate, as well as the crystal growth of SiC.

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Electrical and Structural Properties of Al and B Implanted 4H-SiC

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Keywords: Aluminum, Boron, D_1 Center, Di-Vacancy, Hall Effect Measurement, Ion Implantation, Photoluminescence, Positron Annihilation Spectroscopy, Vacancy

Abstract We investigated the electrical and structural properties of aluminum (Al) and boron (B) implanted 4H-SiC by using secondary ion mass spectroscopy (SIMS), low temperature photoluminescence (LTPL), Hall effect measurement and positron annihilation spectroscopy. A strong diffusion was observed for B-implanted samples toward both the inside and the surface by post-annealing at 1700℃ but not for Al-implanted samples. We could see the luminescence at 4272 Å, which was independent of the dopant species and annealing temperatures, originating in the defect, so-called D_1 center, introduced by the implantation and post-annealing process. For Al implantation, a temperature of 1550℃ was enough for the electrical activation of the acceptors from the result of Hall effect measurement. The positron lifetime for both Al and B as-implanted samples (216ps) was in good agreement with the theoretical lifetime of positron localized at a Si-C di-vacancy (214ps). The positron lifetime of post-annealed samples (148, 147, 149ps) located between that of the virgin sample (144ps) and the theoretical lifetime of positron localized at a C vacancy (153ps). We supposed that a defect type of di-interstitial or di-vacancy is dominant for post-annealed samples.

Introduction

Aluminum and boron are the most hopeful p-type dopants for ion implantation in SiC. Although many groups have investigated the electrical and structural properties of the implanted layers with the dopants in SiC until now, many problems, e.g. low activation rate, deep impurity level, the redistribution of the dopants by high temperature annealing, still remain. Especially the electrical property of implanted layer is strongly influenced by the defects introduced by ion implantation. L.Patrick and W.J.Choyke[1] observed the luminescence from the defect produced by ion implantation in 6H-SiC, which was named D_1 center by them. This luminescence is observed independent of the dopants and survives after post-annealing at high temperature (~1700℃). They proposed the di-vacancy model for the D_1 center because of its resistance to high temperature annealing. They observed another luminescence by D_2 center in cubic-SiC [2] which was also independent of the dopants. They proposed the carbon di-interstitial model for the D_2 center. This model is supported by S.G.Sridhara *et al.*[3] for the implantation of various ions in 4H- and 6H-SiC. Subsequently, although many groups have investigated these defects introduced by ion implantation, it is not evident whether these defects directly influence the electrical property of implanted layer. In this paper we will present the relationship between the electrical property of implanted layer and residual defects survived after high temperature annealing by using SIMS, LTPL, Hall effect

measurement and positron annihilation spectroscopy.

Experimental

In this study we used 4H-SiC(0001) wafers with epi-layer (n-type, n~1.0×10^{16}/cm^3, Si-face, 8° off, 10μm thickness) purchased from Cree Research Inc. and cut them into 5×5mm^2 pieces for implantation. To make up the implanted layer as a box profile, we performed the multiple energy implantation in the energy range of 40-400keV for Al and 40-300keV for B with the total dose of 5.0×10^{14}/cm^2 at RT. A thickness of implanted layer is ~6000Å in both cases. The implanted samples were annealed in the furnace at several temperatures (1400℃, 1550℃, 1700℃) for 20minutes in Ar ambient for the electrical activation of dopants. The redistribution of dopants were investigated by SIMS. LTPL measurements were performed at 4.2K by using HeCd (325nm) laser for the excitation source. By using HeCd laser the photoluminescence spectrum include the luminescence from the substrate because of its long penetration depth in 4H-SiC (~4μm). Hall effect measurements were performed in the temperature range of 140K-300K with the van-der Pauw arrangement of Al electrodes. Positron annihilation spectroscopy was performed at room temperature with the energy of 10keV. Positron with this energy penetrates up to 4000Å in 4H-SiC which is shallower than the thickness of the implanted layer.

Results and discussion

Figure 1 and 2 show the redistribution of the dopants by annealing at 1700℃ measured by SIMS for B and Al, respectively. A strong diffusion is observed for B-implanted samples toward both the inside and the surface by post-annealing at 1700℃. Although this strong diffusion was pointed out by several groups[4]-[6], there is no consensus of the mechanism of the diffusion process. Laube *et al.*[6] proposed that B in 4H-SiC diffuses by the kick-out mechanism with the assistance of silicon interstitials in analogy to the B diffusion in Si. On the other hand, there is no strong diffusion for Al-implanted samples incontrast with B-implanted samples although we can see a little out-diffusion. A pile-up of dopants at the surface is observed in both cases, which was confirmed by Troffer *et al.*[4]. But it is not clear wheather these results is quantitatively correct taking the

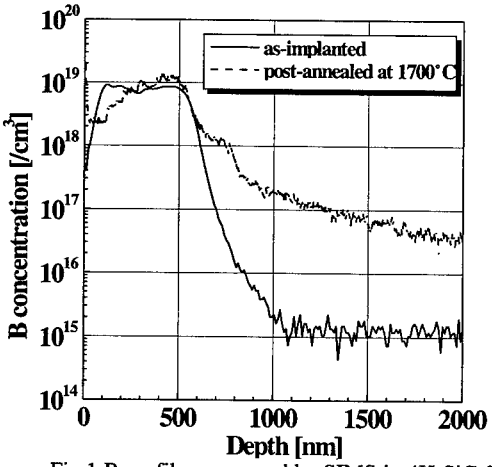

Fig.1 B profiles measured by SIMS in 4H-SiC for as-implanted and after annealing at 1700℃ for 20minutes in Ar ambient.

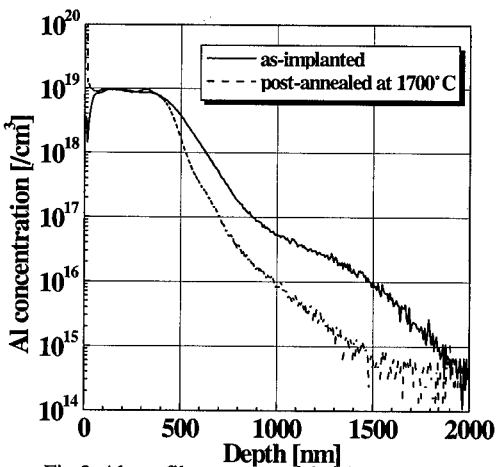

Fig.2 Al profiles measured by SIMS in 4H-SiC for as-implanted and after annealing at 1700℃ for 20minutes in Ar ambient.

insensitiveness of SIMS at surface region. Anyway, we found the big difference of the diffusion process between B and Al in 4H-SiC.

Figure 3 shows LTPL spectra for virgin, Al- and B-implanted 4H-SiC samples subsequent to annealing at 1400, 1550 and 1700 ℃. In wavelength region below 4000Å, we can observe the no-phonon lines of nitrogen–related bound exciton (denoted P_0 and Q_0) and their phonon replicas[7],[8] mainly originating in the substrates in every spectrum due to a long penetration depth of HeCd laser (325nm) in 4H-SiC. In the spectra of Al- and B-implanted samples subsequent to annealing, we can observe very sharp peak at 4272Å and its phonon replicas originating in the defect centers, known as D_1 defect[1], introduced by implantation and annealing at high temperature. We should point out that the intensity of this signal is independent of annealing temperature and, namely, that the density of D_1 defect dose not decrease even after annealing at 1700℃.

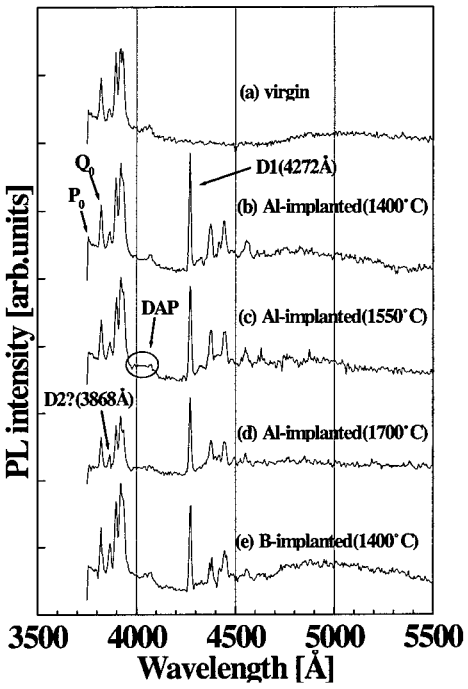

Fig.3 LTPL spectra for virgin and Al-implanted 4H-SiC samples subsequent to annealing at 1400, 1550 and 1700℃.

Figure 4 shows the temperature dependence of free hole concentration for Al-implanted 4H-SiC samples subsequent to annealing at 1400, 1550 and 1700℃. Although there is no great difference in free hole concentration between the cases of annealing at 1550℃ and 1700℃, in the case of annealing at 1400℃, that is less in one order than the cases of annealing at 1550℃ and 1700℃. This result and the fact that the density of D_1 defect is independent of annealing temperature suggest that this defect does not influence the electrical property and, for instance, that D_1 defect does not act as a compensating center that impedes p-type implants.

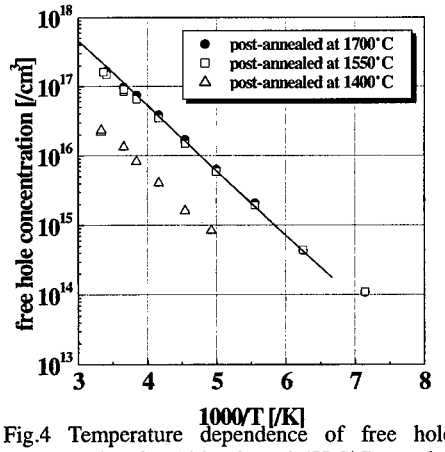

Fig.4 Temperature dependence of free hole concentration for Al-implanted 4H-SiC samples subsequent to annealing at 1400, 1550 and 1700℃.

From the fitting of the neutrality equation to the results of Hall effect measurement, we derived the activation energy of 160-165meV for Al in 4H-SiC, which is rather small in comparison with the result of other group[4]. It is reasonable to suppose that this difference originate in the fact that the mean concentration of Al ($1.0\times10^{19}/cm^3$) in this study is higher than that in their work ($2.0\times10^{18}/cm^3$). In general, the activation energy of dopant become smaller with increasing the doping concentration.

Next, we performed positron annihilation spectroscopy to investigate what kind of defect is dominant in implanted 4H-SiC. Figure 5 shows positron lifetime spectra for virgin and Al-

implanted 4H-SiC samples subsequent to annealing at 1400, 1550 and 1700℃. The positron lifetime in as-implanted sample (216ps) is in good agreement with the theoretical one localized at Si-C di-vacancy (214ps) calculated by Brauer *et al.*[9]. This value is also close to that of 3MeV electron irradiated 6H-SiC studied by Kawasuso et al.[10]. On the other hand, the positron lifetimes in post-annealed samples (148, 147, 149ps) locate between the positron lifetime of virgin sample (144ps) and the theoretical lifetime of positron localized at C vacancy (153ps). Since the positron lifetime for C vacancy (153ps) is quite close to that for virgin sample (144ps), it is hard to be distinguished. However, we think it very dubious that C mono-vacancy survives even after annealing at 1700℃. It is supposed that di-interstitial (C-C or Si-Si) or di-vacancy(C-C or Si-Si), that were proposed in Ref. [1],[2], is dominant for post-annealed samples. To say the least of it, Si mono-vacancy (183ps) or Si-C di-vacancy (214ps) are not dominant for post-annealed samples.

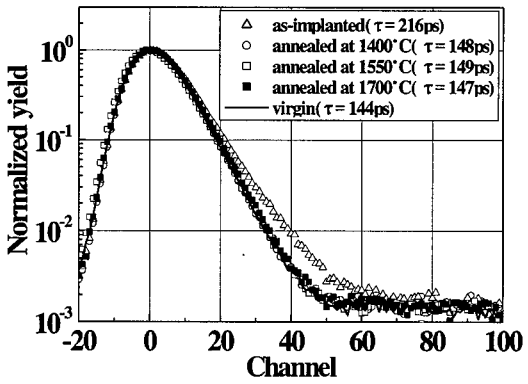

Fig.5 Positron lifetime spectra for virgin and Al - implanted 4H-SiC samples subsequent to annealing at 1400. 1550 and 1700℃.

Summary

In this study, we investigated the relationship between the electrical property and the defect introduced by ion implantation. Although the density of D_1 defect is independent of annealing temperature, the carrier concentration changes drastically between annealing temperature of 1400℃ and 1500℃. This result suggests that D_1 defect does not influence the electrical property, for instance that D_1 defect does not act as a compensating center that impedes p-type implants. From the result of positron annihilation spectroscopy, it is supposed that di-interstitial (C-C or Si-Si) or di-vacancy(C-C or Si-Si), that were proposed in Ref. [1],[2], is dominant for post-annealed samples.

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Secondary Defect Distribution in High Energy Ion Implanted 4H-SiC

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Keywords: Dislocation Loop, Ion Implantation, Secondary Defect, Transmission Electron Microscope

Abstract : The distribution of secondary defects in B^+ or Al^+ implanted 4H-SiC is examined using TEM and SIMS. They distribute from the projected range for low dosage case and from near surface for high dosage case, and they distribute to the depth at the concentration of about 10% of the maximum dopant concentration. These secondary defects are extrinsic dislocation loops and the distribution of them is closely related to that of excess Si and C interstitials formed by implantation.

1. Introduction

Deep pn junction with high blocking voltage and low leakage current is necessary to fabricate vertical type high power devices such as MOSFET and JFET, and for this purpose, high-energy p-type ion implantation process is indispensable [1]. Since the depletion layers extend in both n- and p-type regions when reverse voltage is subjected to the pn-junction, the residual defects in the implanted p-type region exert a bad influence on the reverse properties if they are located inside the depletion layer. This paper describes the distribution and the structure of secondary defects remaining after annealing in high energy B^+ or Al^+ implanted 4H-SiC.

2. Experiments

N-type 4H-SiC wafer with a 10 μ m thick n-type epilayer, obtained from Cree Research Inc., was used for implantation. The donor concentration of epilayer is about $5\times10^{15}cm^{-3}$. Single energy implantations with a energy of 2MeV and multiple energy implantations with energies from 0.5 to 2.0MeV were performed for B^+ and Al^+ at RT through 50nm thick thermally oxidized layer. The implanted dosages are listed in tablel 1. Multiple energy implantations were performed continuously from higher energy conditions. Post-implantation annealings were performed in Ar ambience at 1700℃ for 30min, using RF inductive heated furnace. The heated rate was about 84℃/min. from R.T. to 1700℃.

3. Results and Discussion

Figures 1(a) shows the cross-sectional Transmission Electron Microscope (TEM) image obtained from B^+ implanted at 2MeV and post-annealed epilayer. For as-implanted sample, defect structure was not detected by

Table 1 Ion energies and dosages applied for B^+ or Al^+ implantations

Ion	Energy (MeV)	Total dose (cm^{-2})
B^+	2.0	9.0×10^{13}
B^+	2.0, 1.75, 1.5, 1.3, 1.1, 0.9, 0.7, 0.5	6.0×10^{14}
Al^+	2.0	7.0×10^{13} / 7.0×10^{14}
Al^+	2.0, 1.4, 1.0, 0.7, 0.5	2.6×10^{14} / 2.6×10^{15}

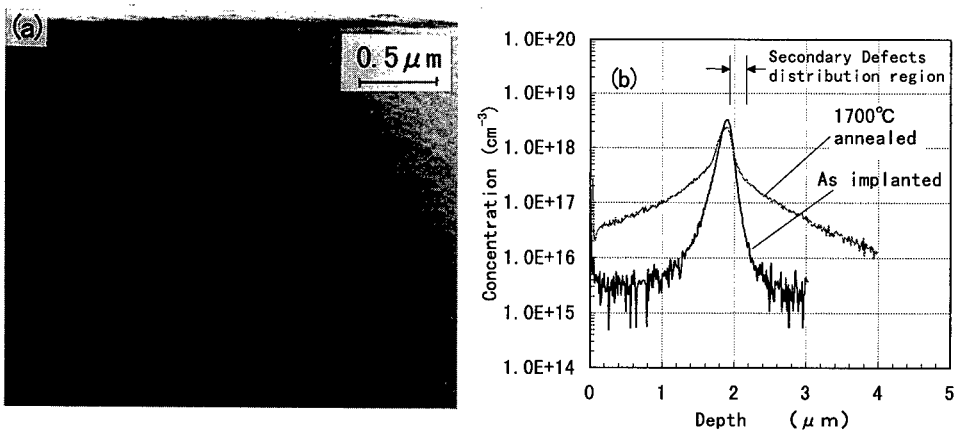

Fig. 1 (a) Cross-sectional TEM image obtained from 2MeV-B^+ implanted 4H-SiC. Dosage is $9.0 \times 10^{13}cm^{-2}$. Observation is along <11$\bar{2}$0> zone axis. (b) SIMS depth profiles of B

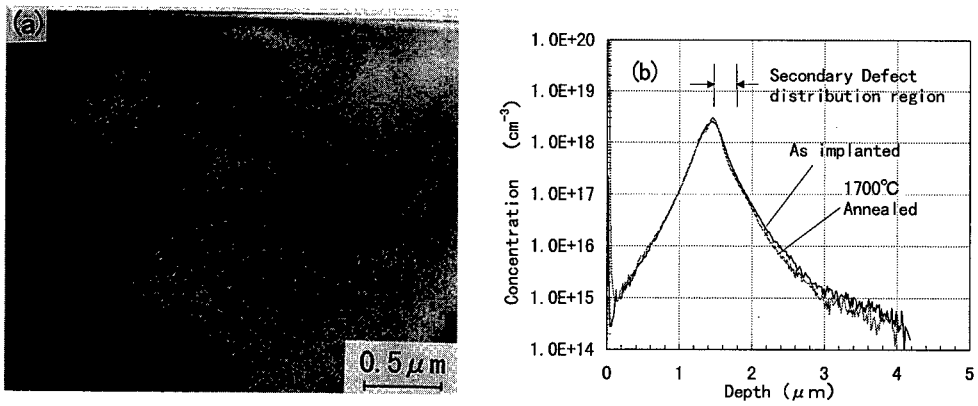

Fig. 2 (a) Cross-sectional TEM image obtained from 2MeV-Al^+ implanted 4H-SiC. Dosage is $7.0 \times 10^{13}cm^{-2}$. Observation is along <11$\bar{2}$0> zone axis. (b) SIMS depth profiles of Al

TEM. After annealing, black dots appear clearly in a belt-like zone, as shown in fig. 1 (a). These secondary defects are distributed between 1.91 μm and 2.15 μm from the surface. Secondary Ion Mass Spectrometry (SIMS) analysis provides B concentration profiles, as shown in figs. 1(b). After annealing, the B profile shows diffusion tails to the surface and bulk. The comparison of the black dots distribution and this B profile for annealed sample reveals that the secondary defects are distributed from near projected range to the depth of the B concentration of $2.5 \times 10^{17}cm^{-3}$, about 10% of maximum dopant concentration. Similar results are obtained for multiple B^+-implanted sample with a dosage of $6.0 \times 10^{14}cm^{-2}$ (dopant concentration of $2\text{-}3 \times 10^{18}cm^{-3}$, not shown) and 2MeV-$Al^+$ implanted sample with a dosage of $7.0 \times 10^{13}cm^{-2}$, as shown in fig. 2. In the case of Al^+ implanted sample, diffusion tails are not observed. The secondary defects are not so clear as that in B^+-implanted sample. They are distributed between 1.44 μm and 1.77 μm from the surface, which is from near projected range to the depth of about 8% of maximum dopant concentration.

Figures 3 shows the cross-sectional TEM image and SIMS profile of 2MeV-Al^+ implanted and post-annealed epilayer. The dosage of this sample is $7.0 \times 10^{14}cm^{-2}$. The secondary defects are distributed in the depth

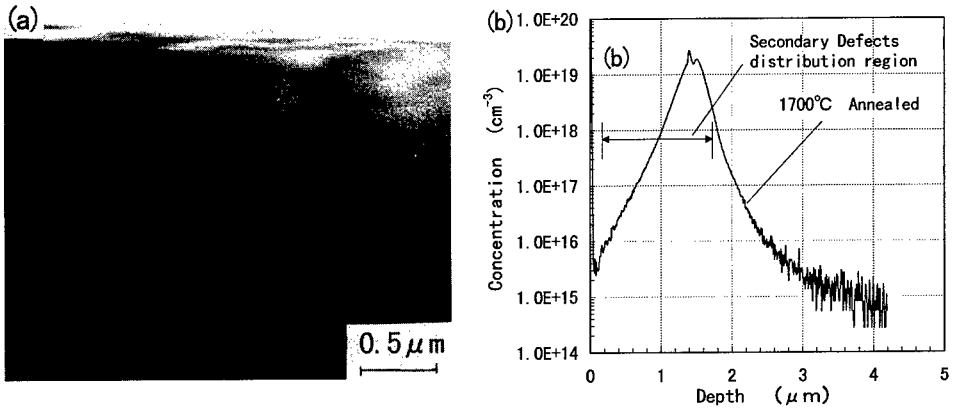

Fig. 3 (a) Cross-sectional TEM image obtained from 2MeV-Al^+ implanted 4H-SiC. Dosage is $7.0\times10^{13}cm^{-2}$. Observation is along <11$\bar{2}$0> zone axis. (b) SIMS depth profile of Al

between 0.1 μm and 1.69 μm, ecpecially densified between 1.22 μm and 1.61 μm. For this sample, the distribution region of secondary defects is from near surface to the Al concentration of $3\times10^{18}cm^{-3}$ (about 11% of maximum dopant concentration). Similar results are obtained for multiple Al^+-implanted sample with a dosage of $2.6\times10^{15}cm^{-2}$ (dopant concentration of $2\text{-}3\times10^{19}cm^{-3}$, not shown).

The structure of secondary defects in high energy ion implantated samples is similar to that in 50-200keV Al^+ implanted sample. Figure 4(a) shows the lattice image of one of the secondary defects observed in multiple Al^+- implanted sample with a dosage of $2.6\times10^{15}cm^{-2}$. When an observation is performed along <11$\bar{2}$0> zone axis of 4H-SiC, a lattice image is characterized by a zigzag pattern of white dots. This zigzag pattern is related to the atomic stacking sequence of Si-C bilayer along <0001> direction, as shown in fig. 4(b). At the center in fig. 4(a), an extra line of white dots parallel to <1$\bar{1}$00> is observed, which means an extra Si-C bilayer is inserted. As a result, the stacking sequence of Si-C bilayer is changed from ABCB'ABCB' (normal sequence) to ABCB'AC'B'CB' (sequence with stacking fault), as shown in fig. 4(b). Consequently, fig. 4(a) shows the cross-section of extrinsic dislocation loop, parallel to {0001} with stacking fault. After implantation, excess Si and C interstitials are formed and the extra Si-C bilayer is generated by agglomeration of these Si and C interstitials during post-annealing. At the upper and lower sides of this extra Si-C bilayer, the crystal lattice may be strained, resulting in the black dots in the low-magnified TEM images.

The size of the secondary defects depends on ion species and dosages. As the dosage is increased, the size of defects grows. This is because that agglomerating interstitials, formed by implantation, are increased with increasing dosage. In the similar dopant concentration, B^+-implanted samples have large size defects compared to Al^+-implanted samples. In the case that dopant concentration is $2\text{-}3\times10^{18}cm^{-3}$, the defect size for B^+-implanted sample is 15-20nm and that for Al^+-implanted sample is 3-5nm. The B diffusion during annealing, as shown in fig. 1(b), is explained by the kick-out mechanism [3], according to

$$I_{Si} + B_S \rightarrow B_I \text{ (mobile)} \quad (I_{Si}: \text{Si interstitial}, B_S: \text{substituted B}, B_I: \text{B interstitial})$$

We speculate that diffused B_I is re-substituted to Si-site and I_{Si} is re-generated through the reaction

$$B_I \rightarrow I_{Si} + B_S$$

and the excess I_{Si} grows extra Si-C bilayer cooperatively with mobile I_C (C interstitial). Supported by the kick-

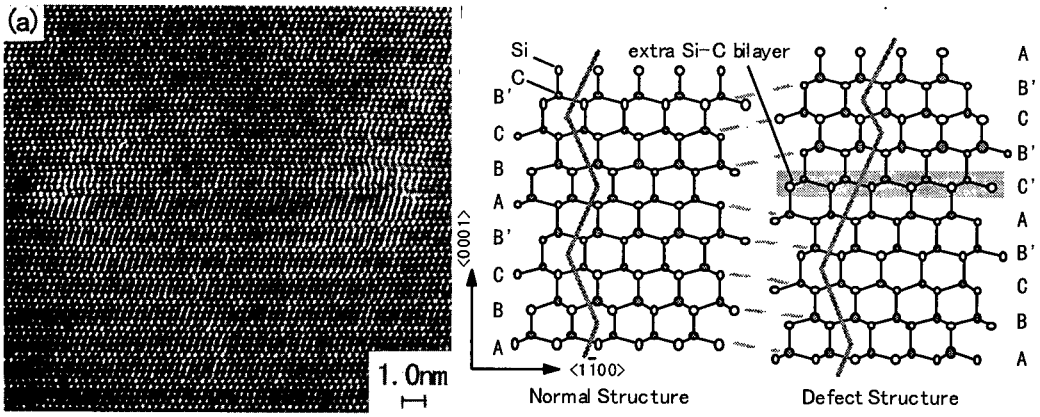

Fig. 4 (a)Lattice image of secondary defect obtained from multiple Al^+-implanted 4H-SiC. Dosage is $2.6\times10^{15}cm^{-2}$. Observation is along <11$\bar{2}$0> zone axis. (b) The model of defect structure. Zigzag patterns of white dots are shown for eye-guide.

out mechanism, agglomerating of I_{Si} and I_C is enhanced in B^+-implanted sample than in Al^+-implanted samples, resulting in the generation of large size extra Si-C bilayer in B^+-implanted sample.

The secondary defects in B^+ or Al^+ implanted 4H-SiC distribute from the depth of projected range for samples with dopant concentrations of $\sim10^{18}cm^{-3}$ and from near the surface for samples with dopant concentrations of $\sim10^{19}cm^{-3}$. Morvan et al. showed there were excess Si and C vacancies near the surface and excess Si and C interstitials in depth for ion implanted 6H-SiC, using simulation technique [4]. The secondary defects distributed in the deeper region are explained by the distribution of interstitials. In the case of high dosage samples, much more point defects are formed near the surface and they may contribute to generate the secondary defects near surface. The reason why the secondary defects distribute to the depth at the concentration of about 10% of the maximum dopant concentration is not clear. Since this result is independent of ion species and dosages, the mechanism can not be explained only by interstitial concentration.

4. Summary

The secondary defects in B^+ or Al^+ implanted 4H-SiC distribute from the projected range for low dosage case and from near surface for high dosage case, and they distribute to the depth at the concentration of about 10% of the maximum dopant concentration. These secondary defects are extrinsic dislocation loops and the distribution of them is closely related to that of excess Si and C interstitials formed by implantation.

Acknowledgements

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Coimplantation Effects of (C and Si)/Ga in 6H-SiC

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Keywords: Carbon, Coimplantation, Gallium, Hall Effect Measurement, RBS-C, Silicon, Site Preference

Abstract. We investigated the effect of coimplantation of gallium(Ga) with carbon(C) and silicon(Si) in 6H-SiC by using Rutherford backscattering spectrometry-channeling(RBS-C) and Hall effect measurement. In the case of coimplantation of Ga with C we could not find the enhancement of the activation rate of acceptors in contrast with the cases of coimplantation of Al/C and B/C. In the case of coimplantation of Ga with Si we found a drastic retrenchment of the activation rate compared with the case of coimplantation of Al/Si and B/Si. We concluded that this result originated in the difference in the site preference between Al, B and Ga.

Introduction

Ion implantation is the most useful technique to control the depth profiles and the doses of the dopants precisely in silicon carbide for the selective area doping. Although many groups have investigated the electrical and structural properties of the implanted layers with the dopants in SiC until now, many problems, e.g. low activation rate, deep impurity level, the redistribution of the dopants by high temperature annealing, still remain. Coimplantation technique was used for Ga/Se implantation in GaAs by Heckingbottom *et al.*[1] for the first time. They confirmed the improvement of the electrical activation rate compared with the Se implantation. This technique is based on the idea of the reduction in the deviation from the stoichiometry introduced by the ion implantation for the compound semiconductor such as GaAs. Recently some studies on the effect of coimplantation of C with the p-type dopants, e.g. Al and B, have been done and the enhancement of the electrical activation rate of acceptors has been reported[2]-[5]. Because Al and B atoms are activated as acceptors on the occasion of residing at Si sites, the number of Al and B atoms occupying Si sites increases by intentionally introducing Si vacancies by coimplantation of C atoms, which leads to the enhancement of the activation rate. The purpose of this study is to investigate the effect of coimplantation of C/Ga or Si/Ga in 6H-SiC by using Hall effect measurement and RBS(Rutherford backscattering Spectrometry)-Channeling.

Experimental

In this study we used 6H-SiC(0001) wafers with epi-layer(n-type, n~1.0×10^{16}/cm^3, Si-face, 3.5° off, 10μm thickness) purchased from Cree Research Inc. and cut them into 5×5mm^2 for implantation. To make up the Ga-implanted layer as a box profile, we performed the multiple energy implantation in the energy range of 40-400keV as shown in Table 1 with the total dose of 5.0×10^{14}/cm^2 at RT and 800℃. In the case of coimplantation, the samples were implanted with C or Si

Energy[kV]	Dose[/cm^2]
400	2.52×10^{14}
300	6.30×10^{13}
200	6.30×10^{13}
150	4.72×10^{13}
100	3.15×10^{13}
70	1.57×10^{13}
50	1.26×10^{13}
40	1.57×10^{13}
total	5.00×10^{14}

Table 1 A schedule of Ga implantation

Energy[kV]	Dose[/cm^2]
120	9.83×10^{13}
100	1.23×10^{14}
80	9.83×10^{13}
60	9.83×10^{13}
40	8.20×10^{13}
total	1.00×10^{15}

Table 2 A schedule of C implantation

Energy[kV]	Dose[/cm^2]
180	2.99×10^{14}
150	2.99×10^{14}
100	1.79×10^{14}
70	1.49×10^{14}
40	7.46×10^{13}
total	1.00×10^{15}

Table 3 A schedule of Si implantation

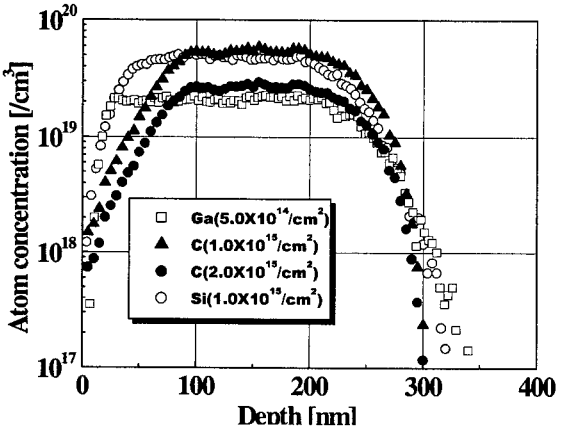

Fig.1 The results of TRIM calculation for depth profile of implanted ions.

with the scattering angle of 105 ° which provides a good depth resolution. Hall effect measurements were performed in the temperature range of 220-330K.

Results and discussion

Figure 2 shows RBS-C spectra for the samples implanted with Ga and coimplanted C/Ga at 800 ℃ after annealing at 1600℃ for 20minutes. The total dose of Ga is 5.0×10^{14}/cm^2 and that of C is 2.0×10^{15}/cm^2. The aligned spectra of Ga implantation and C/Ga coimplantation show the almost same scattering yield as that of virgin sample(not shown here) except the peak at 380 channel which originates in the damages introduced by Ga implantation.

at RT before Ga-implantation with the total dose of 1.0×10^{15}/cm^2 and 2.0×10^{15}/cm^2 with multiple energy implantation to make up box profiles similar to those of Ga-implantation as shown in Table 2 and Table 3. The results of TRIM calculation for depth profile of implanted ions are shown in Fig.1 which suggest that the thickness of implanted layer is ~250nm. The implanted samples were annealed in the furnace at 1600℃ for 20minuites in Ar ambient for the electrical activation of dopants. RBS-C measurements were performed by using 2.0MeV He^+ ion

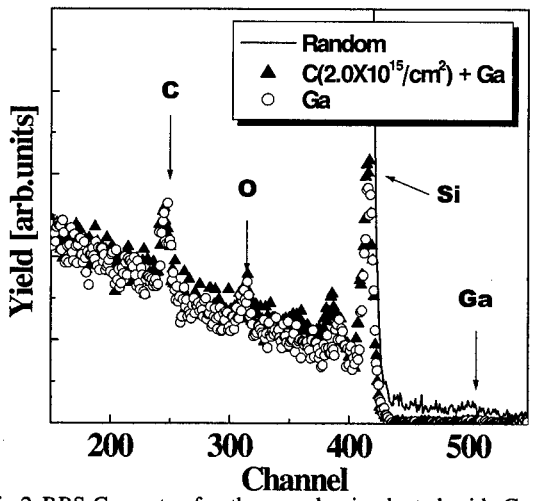

Fig.2 RBS-C spectra for the samples implanted with Ga and coimplanted C/Ga at 800℃. The total doses of Ga is 5.0×10^{14}/cm^2 and C is 2.0×10^{15}/cm^2.

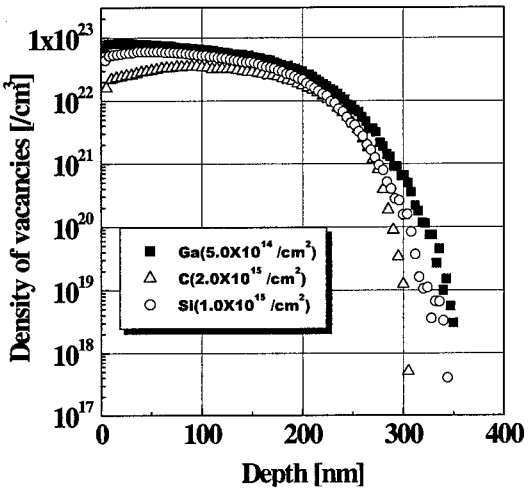

Fig.3 The density of vacancies calculated by TRIM introduced by Ga, C and Si implantation.

In the case of C/Ga coimplantation, we can see the extra peak at 350 channel. We suppose that this peak originates in the damages introduced by C implantation because the distribution of the vacancies formed by C implantation has a peak at deeper region than that of Ga implantation from the results of TRIM as shown in Fig. 3. In the random spectra of both cases, we can see the flat scattering signals from Ga atoms below 500 channel owing to the flat distribution of Ga atoms by multiple energy implantation. On the other hand, we can see very small scattering signals from Ga atoms in the aligned spectra. This result means that the implanted Ga atoms occupy the substitutional positions, but it is not clear which sites(Si site or C site) Ga atoms occupy preferentially from this measurement as described in our previous papers[6],[7]. It is found that through our recent study of EXAFS, which will be published soon, that the implanted Ga atoms occupy the Si site preferentially and act as acceptors.

Figure 4 is the results of Hall effect measurements for Ga implanted(dose = 5.0×10^{14}/cm^2) and C(dose = 1.0, 2.0×10^{15}/cm^2)/Ga coimplanted samples subsequent to annealing at 1600℃ for 20 minutes in Ar ambient. In this result we cannot find the enhancement of the electrical activation rate which is found in the case of C/Al or C/B implantation in SiC by other groups[2]-[4]. Moreover, in

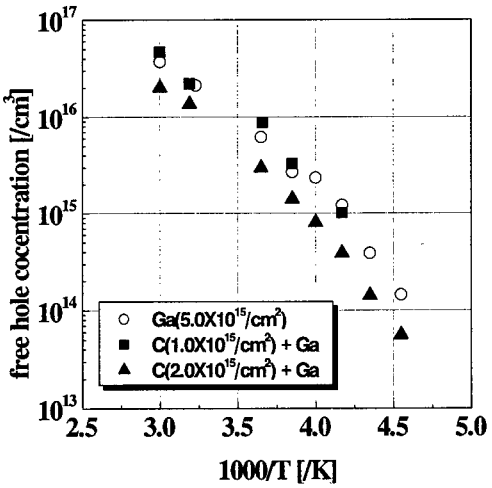

Fig.4 Temperature dependence of free hole concentration in C/Ga coimplanted samples at several doses. Samples were post-annealed at 1600℃ for 20 minutes in Ar ambient.

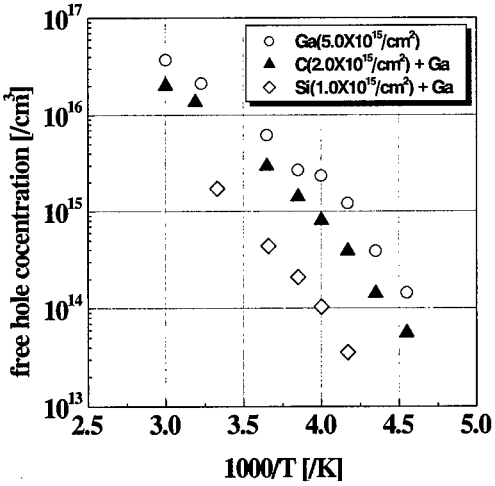

Fig.5 Temperature dependence of free hole concentration in Si/Ga coimplanted samples at several doses. Samples were post-annealed at 1600℃ for 20 minutes in Ar ambient.

the case of Ga coimplantation with C dose of $2.0\times10^{15}/cm^2$(closed triangle) the activation rate is less than that of Ga implantation(opened circle). From the result of Hall effect measurements for C/Al and C/B coimplantation in 4H-SiC studied by Itoh *et al.*[2], we understand that C/B coimplantation is very effective for the enhancement of the electrical activation rate, but C/Al coimplantation is not so effective compared with C/B coimplantation. We suggest that this difference comes from the difference of the site preference of the dopants. Since B essentially prefers to occupy C site rather than Si site because its ionic radius is close to that of C, the incorporation probability of B in Si site is low, which means that the electrical activation rate is essentially low. In the case of B coimplantation with C, the incorporation probability of B in Si site increases due to the existence of excessive C and, consequently, the electrical activation rate is enhanced. Fukumoto also reported[8] that Si site is favorable for B under C-rich condition in cubic SiC from the result of the first-principles calculation. On the other hand, since Al essentially prefers to occupy Si site rather than C site because its ionic radius is close to that of Si, the incorporation probability of Al in Si site is essentially high. So, if excessive C is supplied by coimplantation, the incorporation probability of Al in Si site does not increase so much compared with C/B coimplantation. Since the ionic radius of Ga is much larger than that of B and Al, almost Ga atoms occupy Si sites with or without the existence of excessive C. Consequently there is no difference in hole carrier concentration between Ga implantation and C($1.0\times10^{15}/cm^2$)/Ga coimplantation, on the contrary, it decreases slightly for the C dose of $2.0\times10^{15}/cm^2$ because of the damages by C implantation.

In the case of Si/Ga coimplantation the electrical activation rate considerably decreases in comparison with the Ga implantation(Fig.5) which can be explained by the model that the interstitial Si atoms could interrupt the occupation of Ga atoms in Si sites. This tendency is also seen in the cases of Si/B and Si/Al coimplantation mentioned by Itoh *et al.*[2].

Summary

We have discussed the mechanism of coimplantation of dopants with C and Si. In general, the electrical activation rate of the dopants which act as acceptors by occupying Si sites, eg. B, Al, Ga, is enhanced by coimplantation with C. However, there is a big difference in a rate of enhancement between these dopants because of those site preference. In the case of C/Ga coimplantation there is no effect for the enhancement of electrical activation rate.

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Materials Science Forum Vols. 338-342 (2000) pp. 921-924

Improved Annealing Process for 6H-SiC p^+-n Junction Creation by Al Implantation

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Keywords: Annealing, Electrical Activation, Ion Implantation, RBS/Channeling, SIMS, Surface Stoichiometry

Abstract Five-fold Al implantations at both room temperature (RT) and 300°C ranging from 25 keV to 300 keV with a total fluence of 1.75×10^{15} cm^{-2} have been performed in 6H-SiC epilayers to create p^+-n junctions. The samples have been annealed at 1700°C during 30 mn in an inductively heated furnace especially configured. Surface effects, recrystallization, dopant distribution and electrical activation are investigated by XPS, RBS, SIMS and sheet resistance measurements. For both RT and 300°C-implanted samples, good recrystallization and surface stoichiometry are found as well as no dopant loosing and an interesting electrical activation (46% and 99%, respectively).

Introduction

p^+-n junctions in silicon carbide (SiC) power devices must be realized by ion implantation due to very low diffusion coefficients of dopants in SiC. Its high atomic density and structural crystallinity involve a delicate post-implantation annealing. The implantation temperature, annealing environment, time and temperature of annealing and the heating rate are the essential parameters to reorder the crystal damage induced by ion implantation and to activate the dopants by migrating in SiC lattice sites. Initially, after ion implantation, almost all Al dopants are distributed in interstitial sites, where they are not electrically active.

We utilized a JIPELEC™ rf induction furnace. This technique of annealing has significant advantages such as the very high rising slope in temperature and the very localized zone of heating (the susceptor). But this one implies high temperature variations, vertically in the enclosure and laterally on the surface of the SiC wafers. These temperature gradients may cause an etching of, or a layer deposition on the SiC surface. Moreover, Si is known to volatilize towards 1400°C at one atmosphere pressure, and in lack of a Si supersaturating vapor the carbonization of the surface is inevitable. This paper presents the results of an optimized thermal rf annealing, which avoids these problems.

Experiment

Aluminum, a p-type impurity with a low activation energy (0.20-0.25 eV above the valence band), was chosen to be implanted in a 5×10^{15} cm^{-3} 6H-SiC n-type epilayer purchased from Cree Research. Five implantations were realized at both room temperature (RT) and 300°C with energies ranging from 25 keV to 300 keV, at a total fluence of 1.75×10^{15} cm^{-2}, which correspond in TRIM theoretical simulations to a 4×10^{19} cm^{-3} dopant box profile and a 0.5 µm p^+-n junction depth [Table 1]. Both RT and 300°C implanted samples were annealed during 30 mn at 1700°C in argon atmosphere and silicon partial pressure, in a rf heating furnace. The heating slope was 60°C per second.

The samples were investigated using physico-chemical analysis after each step in dopant incorporation and redistribution. These results were compared to other heating furnace configurations previously published [1-3]. Ion-induced damage in the as-implanted material,

residual damage after post-implantation annealing and SiC recrystallization were evaluated by Rutherford Backscattering Spectrometry in the Channeling mode (RBS/C) technique. The dopant

Energy (keV)	Fluence (cm^{-2})	Rp (nm)	ΔRp (nm)
300	$8x10^{14}$	335	77.9
190	$3.9x10^{14}$	211	56.6
115	$2.8x10^{14}$	127	38.5
60	$1.9x10^{14}$	66	22.8
25	$9x10^{13}$	29	11.0

Table 1: Energy and fluence implantation parameters of experiments, and projected range R_p and standard deviation ΔR_p TRIM simulation results

profiles in the as-implanted and annealed samples were obtained by Secondary Ion Mass Spectroscopy (SIMS) measurements with a 10 keV O_2^+ primary ion beam. Surface stoichiometry of the implanted faces were determined by X-Ray Photoelectron Spectroscopy (XPS), employing AlK_α radiation(1486.7eV). Electrical activation and dopant incorporation in SiC lattice, were inferred from sheet resistance electrical measurements

Results

♦XPS measurements

X-Ray Photoelectron Spectroscopy measurements were undertaken for both RT and 300°C implanted samples on the implanted surface. The XPS results reveal a good surface stoichiometry for the two sample faces, since a yield Si/C=1 was found at 20 nm depth. This shows a non silicon sublimation in spite of our high annealing temperature. We also observe that the energetic shifts reveal a large proportion of C-C/C-H bonds from surface to 8 nm, which must be related to some carbon deposition.

♦RBS/Channeling measurements

After Al RT implantation, the RBS/C spectrum presents an increased backscattering yield, which approaches random value from the surface to a depth of 0.25 μm. This is due to the high fluence used exceeding the critical value at which amorphization of the SiC crystal occurs (about 10^{15} cm^{-3} [4]). For the 300°C implanted samples, the RBS/C spectrum shows a strongly reduced crystalline defect density and no amorphization zone [Figure 1]. The backscattering yield after

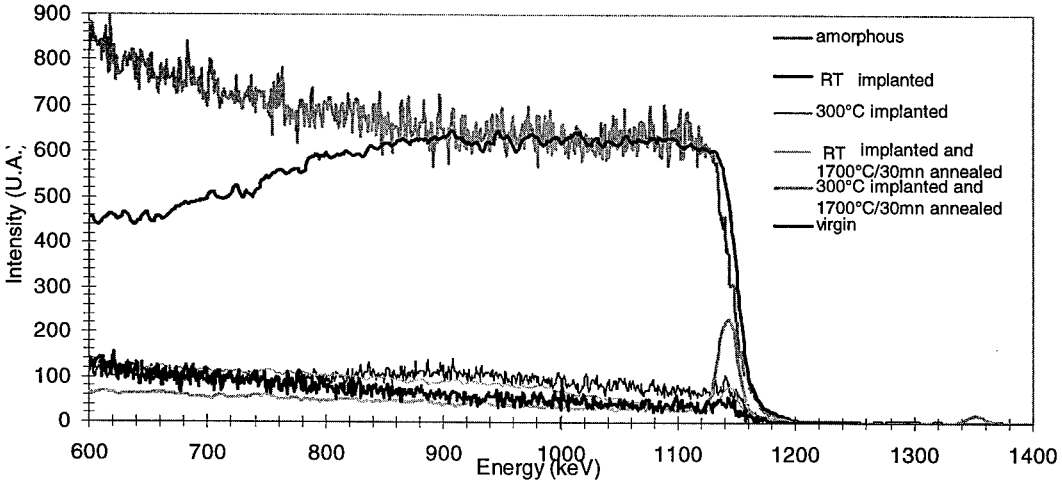

Fig.1 RBS/C signals

annealing is 4.4% for the RT implanted and 4.2% for the 300°C-implanted samples, that proves the sample good crystallinity after annealing for both samples. For the RT-implanted one, a residual damage arising with depth denotes the presence of some extended defects, probably related to the end-of-range defects. The Si signal for the 300°C-sample comes from an XPS analyzed sample, and could be related to Ar^+ sputtering (the 1350-keV peak reveals the Ar presence).

♦SIMS measurements

SIMS profiles of both type-implanted samples agree with the TRIM simulations except the channeled part [Figure 2&3]. For the RT-implanted samples there is a lightly stronger channeling effect. After annealing a fluence of more than 1.6×10^{15} cm^{-2} is found for the RT and 300°C-implanted samples, which denotes no dopant loosing by SiC etching or Al exodiffusion and no layer deposited on implanted surface, in the species and thickness ranges detectable by SIMS. These values compared to other furnace configurations, with other sample ambients, show a clear improvement of our annealing.

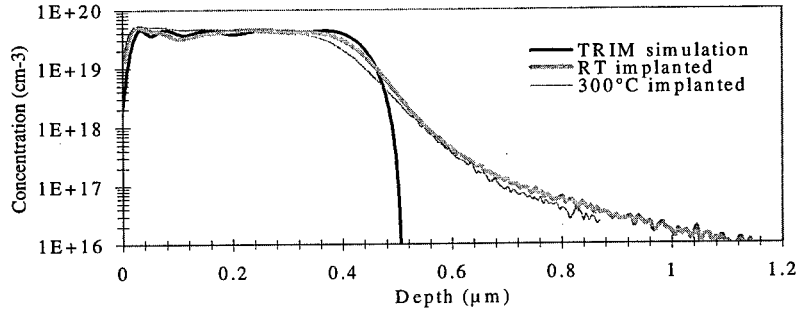

Fig.2 Impurity SIMS profiles before annealing

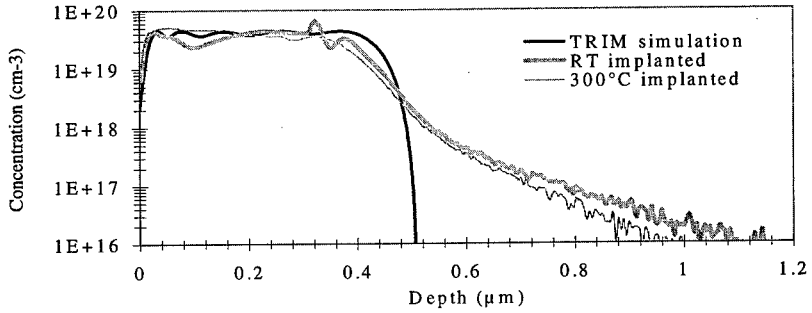

Fig.3 Impurity SIMS profiles after annealing

We can notice that in the case of 300°C-implanted samples a flat profile at 4×10^{19} cm^{-3} is found, like for the as-implanted sample, in contrast with the RT-implanted sample profile where we have some dopant peaks due to the stabilization of Al atoms on end-of-range defects. These defects appear when an amorphous layer is formed. They are localized below the amorphous/crystalline interface and are produced by the coalescence of interstitial impurities into small diameter dislocation loops during the annealing [5].

♦Sheet resistance measurements

A four point probe technique at 25°C was used to measure the sheet resistance of Al implanted layers, in order to determine the electrical active center density. Before four point measurements, 40 nm of the SiC implanted layer was removed from surface by a reactive ion etching (RIE) in SF_6/O_2 plasma, to contact the Al box profile.

For the RT-implanted samples, the measured acceptor activation (incorporation of Al in SiC lattice sites) is in the 35%-46% range, and for the samples implanted at 300°C we find a higher

activation between 48% and 99%. An ionization coefficient of 0.9% for Al dopant and a mobility of 40 $cm^2/V/s$ for hole carriers have been undertaken for calculation.

We can remark disparities in the electrical activation results probably due to the measurements method, the little size of our samples and surface non uniformity. Nevertheless, satisfactory electrical results were obtained, in agreement with post-annealing SiC crystalline quality noticed by physico-chemical analyses.

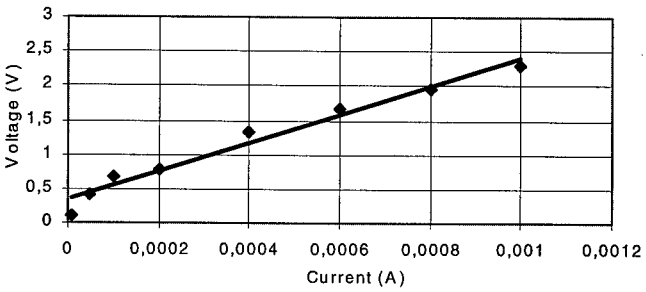

Fig.4 Four point measurements data for a 300°C-implanted sample, R =9.3 kΩ which corresponds to 99% electrical activation

Conclusion

RBS/C measurements reveal that the virgin level is attained after annealing for both RT and 300°C-implantated samples. No great surface carbonization, deposited layer or dopant loosing are found. Elevated implantation temperatures produce higher dopant electrical activation, but the values for RT-implantations remain interesting in the perspective of industrial applications. Additional and various electrical investigations will be carried out on p^+-n diodes and Hall effect structure-tests, which are in fabrication process.

Acknowledgements

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Characteristics of n-p Junction Diodes made by Double-Implantations into SiC

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Keywords: Annealing, Diode, Doping, Ion-Implantation

ABSTRACT: Empirical formulae for range statistics of acceptor ions Al^+ and B^+ in the energy range 50 keV to 4 MeV were developed by fitting the data obtained from the analysis of secondary ion mass spectrometry (SIMS) depth profiles of single energy ion implants. Double implantation technology consisting of deep-range acceptor followed by shallow-range donor implantation was used to fabricate n-p junction diodes in 4H-SiC. Either Al or B was used as the acceptor species and N as the donor species with all implants performed at 700°C and annealed at 1650°C with an AlN encapsulant. The diodes were characterized for their current-voltage (I-V) and capacitance-voltage (C-V) behavior over the temperature range 25°C to 400°C.

Ion implantation is the only feasible selective area doping technique available for making SiC devices. Double implantation technology consisting of deep range acceptor followed by shallow range donor implants is necessary for making complementary field effect transistors and several high power devices such as thyristors and IGBTs. For the junctions to withstand high blocking voltages in high power devices, the lightly doped side of the junction needs to be deep, requiring MeV energy implantation. In this work empirical formulae were developed for the range statistics of acceptor ions Al and B for energies up to 4 MeV. The use of these empirical formulae along with the Pearson IV distribution function [1] predicted the experimental implant profiles better than TRIM. Planar n-p junction diodes were made using successive selective area, multiple energy acceptor and donor implants and characterized for their I-V and C-V behavior.

For this work a series of single energy Al and B ion implants in the range 50 keV to 4 MeV were performed into Si face, 3.5° off-axis, 6H-SiC n-type epilayers with 5 to 10 μm thickness and a doping density of $6x10^{15}$ to $1x10^{16}$ cm^{-3}. Secondary ion mass spectrometery (SIMS) was performed on each single energy ion implanted sample to determine dopant concentration as a function of depth. Range statistics were extracted from the SIMS implant concentration depth profiles. The empirical equations for the range statistics obtained by fitting the experimental data are as follows:

Range of maximum concentration (R_m) = $k_1(E-k_2)^r$ (1)

Mean range (R_p) = $k_3(E-k_4)^s$ (2)

Straggle (ΔR_p) = $k_5(E-k_6)^t$ (3)

Skewness (γ) = $k_7\left[(E-k_8)^u - 1.2\right]$ (4)

Kurtosis (β) = $\dfrac{\left[39\gamma^2+48+6(\gamma^2+4)^{3/2}\right]}{32-\gamma^2}+k_9E+k_{10}$ (5)

Max. concentration / dose (N_m / ϕ) = $k_{11}\left[(E-k_{12})^v + 1\right]$ (6)

Table I. Fitting parameters for equations (1) through (6) determined in this study

	k_1 (μm)	k_2 (MeV)	k_3 (μm)	k_4 (MeV)	k_5 (μm)	k_6 (MeV)
B	1.2	-0.030	1.2	-0.017	0.093	0.046
Al	0.93	0.045	0.91	0.042	0.14	0.048

	k_7	k_8 (MeV)	k_9 (MeV^{-1})	k_{10}	k_{11} (cm^{-1})	k_{12} (MeV)
B	6.8	0.047	0.30	0.96	2.9×10^4	0.037
Al	3.5	0.045	0.24	0.81	1.7×10^4	0.024

	r	s	t	u	v
B	0.76	0.75	0.16	-0.029	-0.24
Al	0.64	0.64	0.26	-0.072	-0.57

Table I gives values of the coefficients in the equations listed above for the two acceptor ions. The Pearson IV fit for the experimental SIMS profile based on the moments obtained from formulas (1) through (6) is shown in Figure 1 for 1 MeV / 3.1×10^{15} cm^{-2} Al implantation and 2 MeV / 2.8×10^{15} cm^{-2} B implantation. Implant profiles predicted by TRIM are also included for comparison. The implant depth profiles generated by the empirical formulae, and Pearson IV model the implant profiles more accurately than TRIM. For the same implant energies implant depth profiles are similar for both 6H- and 4H-material and hence the above empirical formulae hold good for 4H-SiC also.

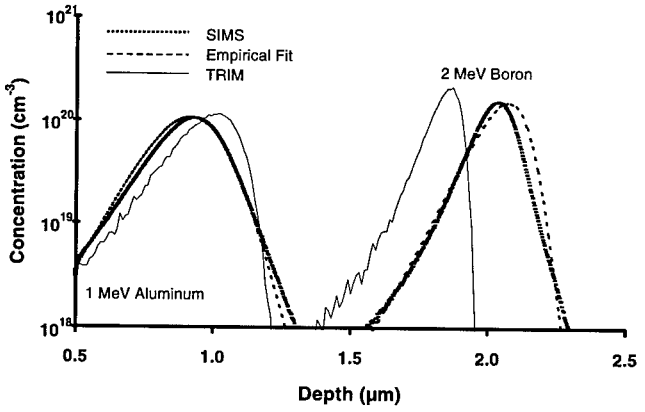

Fig 1 SIMS, Pearson IV fit, and TRIM implant depth profiles for 1 MeV Al and 2 MeV B

Planar, circular n-p junction diodes were fabricated in n-type ($4x10^{15}$ cm^{-3}) 4H-SiC epilayers grown on Si-face, 8° off-axis, n^+ 4H-SiC substrates by multiple-energy box profile Al or B ion implantation followed by shallow box profile N ion implantation. The highest Al ion energy was 1 MeV and the highest B ion energy was 0.7 MeV both yielding a range of ~1 μm. Box profiles of either Al or B implants at a concentration of $1x10^{17}$ cm^{-3} were used. To obtain reliable ohmic contacts, a shallow $1x10^{20}$ cm^{-3} Al implant was also performed for both B and Al implantations in the area where the ohmic contact metals were placed. The acceptor implants were followed by a shallow, multiple-energy N ion implantation with a highest energy of 90 keV to a depth of ~0.2 μm and a concentration of $2x10^{19}$ cm^{-3}. All implants were performed at 700°C using either a thick (2.5 μm) SiO_2 layer or a plated Ni layer with a Si_3N_4 buffer as implant-blocking or mask layers. The diodes were annealed at 1650°C using an AlN encapsulant. Diode passivation was achieved using a 0.4 μm thick SiO_2 layer. No junction termination was used. Ohmic contacts were achieved by e-beam evaporation of Ni or Ti/Al on n- and p-type materials, respectively, and annealing at 1200°C for 3 mins in a vacuum alloying system. The diameter of the diode junction is 245 μm.

Because of space limitations, the I-V characteristics of the $1x10^{17}$ cm^{-3} B-implanted diodes only over the temperature range 25°C to 400°C are shown in Figure 2(a) (forward) and Figure 2(b) (reverse). The ideality factor of the diode measured at room temperature was 2.09, indicating that the dominant current conduction mechanism at low forward bias voltages is due to recombination. The turn-on voltage, defined as the voltage at which the current reaches $1x10^{-4}$ A/cm^2, was 2.3 V at room temperature. With increasing temperature, the I-V characteristics showed two turn on mechanisms, one at voltages less than 1 V and the other at approximately 2 V. The exact reason for this behavior is not known at this time, but may be attributable to SiO_2-SiC interface trapped charges at the surface or some other surface anomaly caused by implantation / annealing processing. This second conduction mechanism has also been observed by other groups in SiC n-p junctions [2, 3, 4]. The forward series resistance, r_s, for the B-implanted diode was 20.8 ohms-cm^2 at room temperature and decreased to 12.9 ohms-

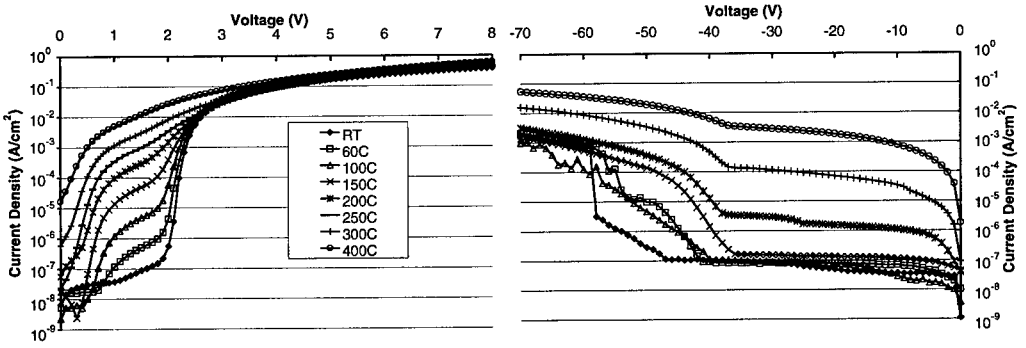

Fig. 2 Forward (a) and reverse (b) I-V characteristics of double (B and N)-implanted 4H-SiC n-p junction diode

cm^2 at 250°C. The r_s value for the Al-implanted diode was 124 ohms-cm^2 at room temperature and decreased to 13.9 ohms-cm^2 at 250°C. The relatively smaller change in r_s for B than Al is consistent with the fact that B is a deeper acceptor than Al and will ionize less with the same increase in temperature. The very high series resistance values for both Al and B implanted diodes in this work probably is due to a combination of the large separation between the n-type doped region and the Ti/Al contact, and the high resistance of the Ti/Al contact to the p-type material. From C-V measurements, the substitutional dopant concentration was $8x10^{16}$ cm^{-3} (~80% implanted dopant) for Al. C-V measurements on a $1x10^{18}$ cm^{-3} B-implanted control sample showed a substitutional B concentration of $2.5x10^{17}$ cm^{-3} (~25% implanted dopant).

The reverse I-V curves for the B-implanted diode over the temperature range of 25°C to 400 °C are shown in Figure 2(b). At room temperature, the B-implanted diode showed an avalanche breakdown at -58V and the Al-implanted diode had an avalanche breakdown at -45V. These low breakdown voltages are due to a small (~0.8μm) p-drift region thickness, which will be swept at a low reverse bias voltage of ~ -20V as suggested by the C-V measurements. The absence of any edge termination also contributed to early breakdown at the periphery of the junction. A room temperature leakage current of $6.5x10^{-8}$ A/cm^2 was observed at a reverse bias of -20V, which increased to $3.3x10^{-7}$ A/cm^2 at 250°C. The Al-implanted diode had a room temperature reverse bias leakage current of $5x10^{-7}$ A/cm^2 at -20V, which increased to $1.8x10^{-2}$ A/cm^2 at 250°C. Two breakdown mechanisms can be seen in the reverse characteristics -- one caused by avalanche and the second probably caused by the same surface phenomenon that caused the early turn on current.

In conclusion, the empirical formulae for the range statistics of the important Al and B acceptors in SiC were developed. Diodes using double implantation technology with reasonable I-V characteristics were demonstrated.

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Materials Science Forum Vols. 338-342 (2000) pp. 929-932

Reactivation of Hydrogen-Passivated Aluminum Acceptors in p-type SiC

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Keywords: Acceptor, Dissociation, Hydrogen, Ion Drift, Passivation

Abstract. The thermal stability of the hydrogen passivation of aluminum acceptors in p-type silicon carbide is investigated by annealing experiments. The passivation is done by low-energy ion implantation. Annealing is done under the influence of the electrical field in a reverse biased Schottky diode. The influence of temperature, p-type doping level, and hydrogen isotope (^{1}H or ^{2}H) on the depth profile of passivated acceptors is investigated. At temperatures around 500 K, Al acceptors become reactivated. In the electrical field, released hydrogen is moving as a positive ion and is able to passivate further acceptors. Without electrical field, the effect is reversible. A qualitative model and an upper limit for the Al-H dissociation energy are given.

Introduction

As in many other semiconductors, hydrogen is known to passivate acceptors in p-type silicon carbide. This passivation may exist already after epitaxial growth (Chemical Vapor Deposition) [1] or may be achieved by intentional incorporation. A systematic study on the spatial extent and the degree of passivation is available for passivation by low-energy implantation of hydrogen only [2]. Using this technique with a kinetic energy of 300 eV per atom, we surprisingly found hydrogen to be mobile already at room temperature because of the drastically reduced defect production compared to plasma treatment or high-energy implantation [3,4]. Both boron as well as aluminum acceptors are passivated effectively. In this work, we are investigating the thermal stability of this acceptor passivation by annealing experiments. To control the balance between dissociation and formation of acceptor-H complexes, we additionally apply an electrical field to remove released hydrogen. Experiments of this type are well known from silicon [5]. For the case of SiC, one of our early experiments is already published [4]. Here, we additionally report on the influence of temperature, p-type doping level, and hydrogen isotopic mass on the time dependence of the acceptor reactivation.

Experiment

The work was done on commercial p-type epitaxial layers (thickness ≈ 5 µm, polytype 4H) on p^+-substrates. The net doping level N_A of the epi-layer is either 6×10^{15} cm^{-3} or 2×10^{17} cm^{-3}. In addition to the intentional dopant Al, boron is present with a typical concentration of 2×10^{15} cm^{-3} [2], i.e. both B and Al determine the electrical properties of the lightly doped layers whereas Al dominates in the more heavily doped material.

The passivation is done by implantation of H_2^+ molecular ions with 600 eV at 680K as described elsewhere [2,3]. After implantation, Schottky contacts (0.5 mm dia.) were prepared by evaporation of Ti on the implanted layers. The depth profiles N(x) of electrically active acceptors were measured by Capacitance-Voltage (CV) profiling. Thermal Admittance Spectroscopy (TAS) was used to investigate the acceptor energy levels and thus to discriminate between B and Al.

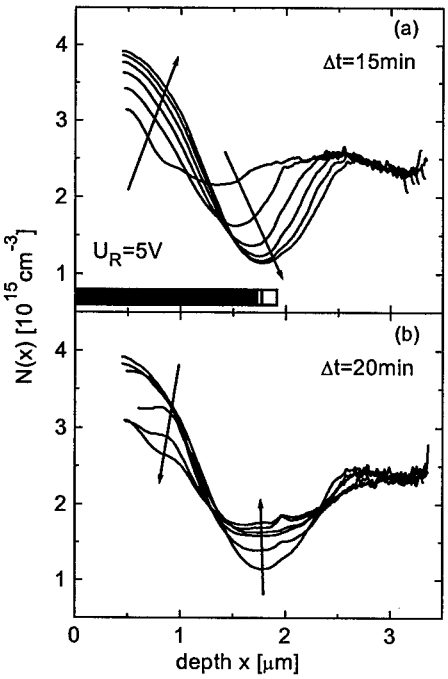

Fig. 1: Depth profiles of electrically active acceptors obtained by CV profiling on ^{1}H-passivated, lightly doped p-type SiC during reverse bias (a) and zero-bias annealing (b) at 510 K. The arrows indicate the sequence of measurements. The time Δt is the duration of each individual annealing step.

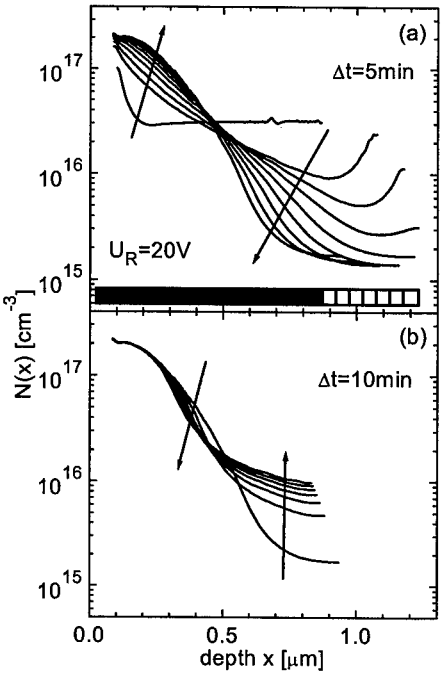

Fig. 2: Similar to Fig. 1, but measured at 490 K on ^{1}H-passivated p-type SiC with a higher aluminum doping level of 2×10^{17} cm^{-3}.

During annealing, the Schottky contacts are used to establish an electrical field by applying a reverse bias U_R at the diode. This procedure is frequently termed 'reverse bias annealing' (RBA). The electrical field gradually decreases with depth and extends up to the width w of the space charge region which is obtained from the capacitance during annealing. The field points into the semiconductor. Even without external bias, there is an intrinsic field due to the zero-bias band bending.

Results

The CV depth profiles N(x) of electrically active acceptors during reverse bias and subsequent zero bias annealing are shown in Figs. 1 and 2 for the lightly and the more heavily doped material, respectively. The spatial extension w of the electrical field is indicated by the bar at the bottom of each figure. It is roughly constant except for RBA at the more heavily doped material (the variation of w during RBA is indicated by the hatched part of the bar). At small depth where the electrical field is strongest, N(x) is increasing during RBA whereas it is decreasing at greater depth. The position of the resulting minimum of N(x) agrees with the extension w of the electrical field as already shown in detail for the lightly doped material by variation of U_R [4]. During subsequent zero bias annealing, the profile changes due to RBA tend to be reversed (Figs. 1b and

2b). The rate of this change is smaller than during RBA.

To investigate the type of acceptor reactivated in the lightly doped material, TAS was measured on Schottky contacts after the RBA sequence (Fig. 3). In an unpassivated reference sample, the two steps in the spectra correspond to Al and B acceptor levels. This identification and the energy levels have already been discussed [3]. After passivation, the step due to B is completely absent and does not reappear after RBA. As already discussed in ref. [3], this means that boron is fully passivated.

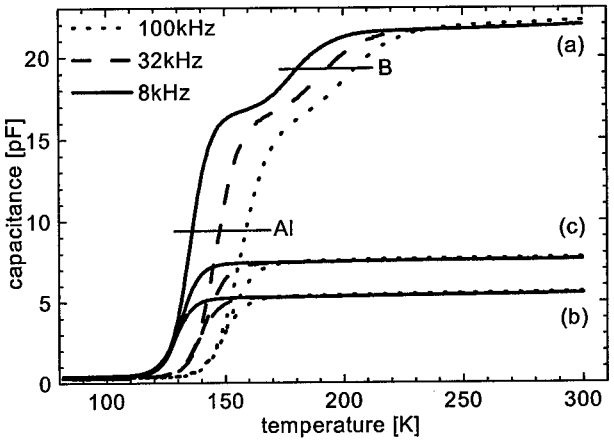

Fig. 3: Thermal admittance spectra (differential capacitance measured with various AC frequencies) at U_R=0 V:
(a) reference, (b) ^{1}H-passivated,
(c) after RBA at 550 K and U_R =20 V.

Discussion

The measured depth profiles clearly demonstrate that acceptors are reactivated at temperatures around 500 K. We interpret this as a dissociation of aluminum-hydrogen complexes. The electric field dependence reveals that the released hydrogen is pushed deeper into the sample by the electric field as expected for a positive ion. Close to the end of the electrical field at the depth w, it passivates further free acceptors and thus reduces N(x) at this depth. Since the electrical field decreases to zero gradually, it is very weak close to the depth w, i.e. the transport of H towards greater depth becomes inefficient at some smaller depth where the ion drift and the reversely directed free diffusion cancel each other. At this depth, the sequentially measured N(x) profiles intersect. With zero reverse bias, the profile changes essentially reflect the diffusion of released hydrogen and its trapping at free acceptors on both sides of the local N(x) minimum (Fig. 1b). The extension of the intrinsic field at zero bias prevents a homogeneous passivation towards small depths. This effect is responsible for the increase of N(x) at the smallest depth in the initial profiles (Fig. 1a, 2a).

Though there is a significant boron concentration present in the lightly doped material, we conclude that the reactivation and passivation observed is due to Al only. This is based on the following facts. The TAS spectra (Fig. 3) demonstrate that no active boron is present after RBA in the temperature range discussed, i.e. B remains fully passivated. In Fig. 1, N(x) saturates at a value of 4×10^{15} cm^{-3} during RBA though the total acceptor concentration in this particular sample is 6×10^{15} cm^{-3} (Fig. 1a). Since about 2/3 of all acceptors are Al in this material [3], this difference agrees well with the statement that Al only, but not B, is reactivated.

To evaluate the reactivation quantitatively, we have investigated the concentration increase c(t) of acceptors during RBA at small depths as a function of annealing time t. The data fit reasonably well to an exponential increase of the type $c(t)=N_i + (N_f - N_i)\times(1 - \exp(-t / \tau))$ where N_i and N_f are the initial and final concentration at fixed depth. The time constants τ resulting from these fits are shown in Fig. 4. There are some clear trends: (i) the reactivation time constant is strongly temperature dependent; though the temperature range investigated is narrow, a thermally activated process is obvious as demonstrated by the straight line in Fig. 4; (ii) there is a significant isotope shift (^{1}H is faster) in the lightly doped material and, at least, an indication of this effect for the

higher doping level; (iii) the reactivation is faster in the heavily doped material.

To interpret these data, we may consider three distinct steps: (1) the dissociation of the Al-H complex, (2) the transport of H to greater depth and (3) the capture of hydrogen by free acceptors. As a first approach, we may assume that process (1) is by far the slowest. In this case, released H is removed immediately, the overall time constant τ is identical to the reciprocal dissociation rate, and the slope of the Arrhenius plot in Fig. 4 directly yields the dissociation energy (1.8 eV). If we reasonably assume that the dissociation rate itself does not depend on the electrical field, this approach, however, does not explain the pronounced doping dependence. To explain it, we propose a significant influence of process (2) on the overall time constant. Since the electrical field is one order of magnitude larger in the RBA experiments on the heavily doped material, a faster process (2) due to the ion drift is to be expected. If process (2), however, has a significant influence on the total time constant, this time constant is larger than the dissociation time constant. Hence, the estimate of 1.8 eV for the dissociation energy derived above, is to be understood as an upper limit. To further understand the reactivation process more quantitatively and to derive e.g. binding energies and diffusion constants, a numerical simulation is being developed, taking into account the depth dependence of concentrations and of the electrical field.

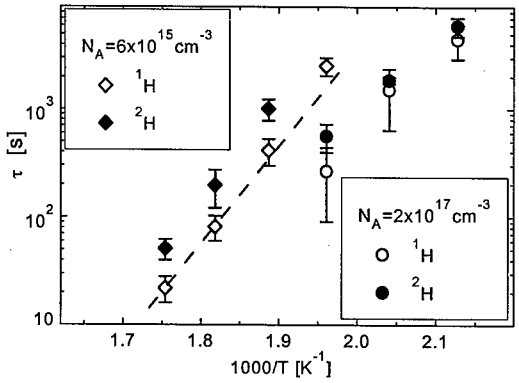

Fig. 4: Reactivation time constants in dependence of RBA temperature for lightly and highly doped material. The dashed line corresponds to an activation energy of 1.8 eV.

Conclusions

A reactivation of H-passivated Al acceptors takes place at temperatures around 500 K. Characteristic profile changes are obtained if the released hydrogen, preferentially existing as a positive ion in p-type SiC, is removed from the acceptors by an electrical field. The characteristic time constant of the reactivation is found to be thermally activated with an activation energy of at most 1.8 eV. According to a simple 3-step model (dissociation, ion drift, and capture), both the dissociation of Al-H complexes as well as the ion drift determine the overall time dependence.

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Materials Science Forum Vols. 338-342 (2000) pp. 933-936

Formation of Passivated Layers in p-Type SiC by Low Energy Ion Implantation of Hydrogen

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Keywords: Acceptor, Diffusion, Hydrogen, Implantation, Passivation, Resistivity

Abstract: The mobility of hydrogen and its passivating effect on acceptors in p-type SiC is investigated. Hydrogen (isotope ^1H or ^2H alternatively) is implanted at temperatures between 300 K and 680 K with low energy (300 eV per atom) in order to minimize implantation damage. The depth profiles of ^2H and of passivated acceptors correspond closely. Up to 500 K, a fully passivated layer with a well defined thickness is formed. Its depth (on the order of 1 micrometer) is investigated as a function of doping level and hydrogen fluence. At higher temperatures, the incorporation drastically increases, but the electrical passivation is partial only. Qualitative explanations are given.

Introduction

In many semiconductors, hydrogen is known to be trapped at defects or impurities and to alter their electrical properties. Shallow levels, in particular, are usually removed from the band gap. In silicon carbide, systematic investigations are still rare. Hydrogen incorporation has been observed after epitaxial growth [1], plasma treatment [2], ion implantation [2, 3] or treatment in hydrogen gas [4]. In most reports, trapping at defects plays a significant role and the process temperatures necessary to induce a detectable mobility of hydrogen are in excess of 900 K. By using low-energy implantation, we have recently shown [5, 6] that hydrogen may be mobile already at room temperature because of the drastic reduction of implantation induced trapping centers. Wherever present, hydrogen passivates acceptors in p-type material. Identical implantations into n-type SiC do neither result in a comparable incorporation nor in a detectable influence on shallow dopants [5]. Consequently, the present work is restricted to p-type material.

We'd like to stress that the range of our implantations is in the order of 10 nm only [5]. The results shown here, however, are measured on a depth scale in the order of micrometers, i.e. they are due to a long-range mobility of hydrogen.

Experiment

Most of the experimental details have already been described in detail [5]. Here, we give a brief summary only: we implant hydrogen (isotope ^1H or ^2H) at temperatures between 300 K and 680 K. In contrast to our earlier work, we additionally use a (Wien-type) mass-filter to select 600 eV H_2^+ molecular ions exclusively. Unless otherwise stated, the fluence is 3×10^{15} atoms/cm^2 . Electrical properties are measured by means of Capacitance-Voltage (CV) profiling (1 MHz) and Thermal Admittance Spectroscopy (TAS) on Schottky diodes. Depth profiles of ^2H and of the acceptors B and Al are measured by Secondary Ion Mass Spectrometry (SIMS). All experiments are done on commercial p-type epitaxial layers (thickness ≈ 5 μm) on p^+-substrates (polytype 4H). The net doping level N_A of the epi-layer is either $(5\text{-}10)\times10^{15}$ cm^{-3} or 2×10^{17} cm^{-3} . In addition to the intentional dopant Al, boron is present with a concentration of $(2\text{-}4)\times10^{15}$ cm^{-3}.

Results

Depth profiles of ^2H and of remaining electrically active acceptors are shown in Fig.1 for samples implantated with ^2H at 300 K, 500 K, and 680 K. Up to 500 K, the depth profiles of ^2H are nearly rectangular-shaped with a maximum concentration close to the virgin acceptor concentration. After implantation, the depth region directly accessible by CV profiling is shifted deeper into the sample compared to the virgin crystal. The shift of the profile data to greater depth means that the zero-bias space charge region of the Schottky contact extends unusually deep into the crystal which in turn means that the concentration of remaining acceptors is very low at small depths. The steep slope of the measured CV profile in Fig. 1b at 1 μm depth somehow indicates this transition, but CV profiling is not expected to give true profiles in the case of very steep gradients. At depths greater than the extension of the hydrogen profile, the net acceptor concentration is not influenced.

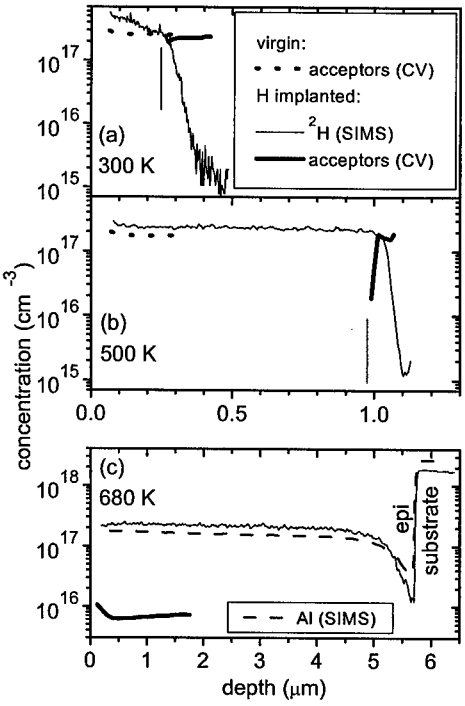

Fig. 1: Depth profiles of ^2H and electrically active acceptors in p-type SiC after ^2H implantation at different temperatures (a-c).

At temperatures above 600 K, the profile shapes are totally different. Fig. 1c reveals a deep incorporation of hydrogen down to the heavily doped substrate, i.e. the total amount of hydrogen incorporated is much larger. The ^2H concentration closely follows the Al acceptor concentration which is inhomogenous close to the epi-substrate interface in these particular samples. The electrical passivation is partial only: the acceptor concentration is reduced by a factor of 25 only and no pronounced depth dependence exists.

Depth profiles of remaining electrically active acceptors after implantation of the isotope ^1H into the same material are shown in Fig. 2. The results are similar: below 500 K, a sharply defined, passivated layer is formed. At 680 K, the whole epitaxial layer is passivated by a factor of 4000. The factor of passivation in the high temperature regime depends on details of implantation conditions and will not be treated here.

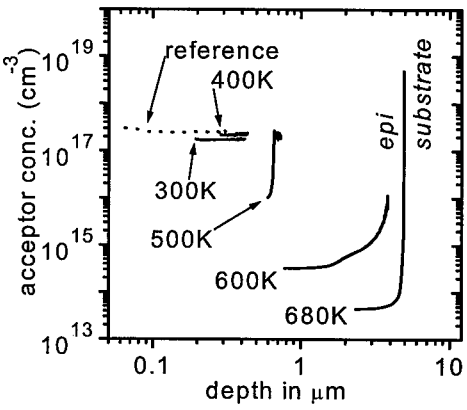

Fig. 2: Depth profiles of remaining accptors in aluminum doped p-type SiC after ^1H implantation at various temperatures.

Similar results, in particular the two characteristic temperature regimes, are also obtained for the lightly doped material. For 300 K and 680 K implantation temperature, some profiles are already shown in Ref. [5] (the gradually

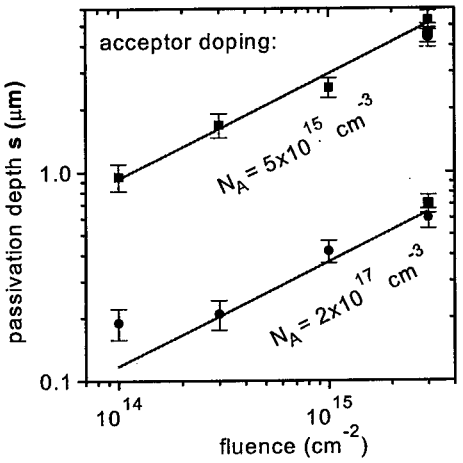

Fig. 3: Depth of the fully passivated layer after ^{1}H implantation at 500 K for two different p-type doping levels.

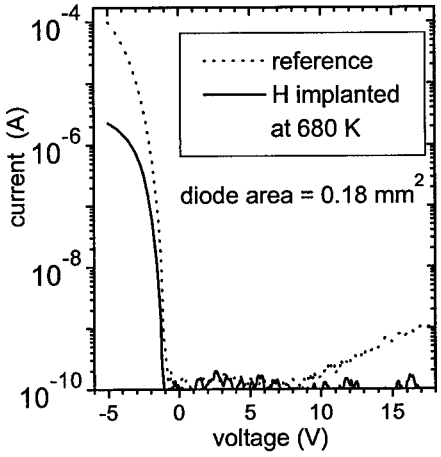

Fig. 4: Current-Voltage Characteristics of a Schottky diode on ^{1}H-passivated p-type SiC with $N_A = 2\times10^{17}$ cm^{-3}.

decreasing profile shown for 465 K in that reference probably is an artefact due to imperfect implantation conditions).

The influence of the implanted H fluence on the thickness of the passivated layer was investigated at 500 K (Fig. 3). Different fluences were realized by keeping the ion beam current constant and varying the implantation time. The thickness of the passivated layer increases sub-linearly with fluence and is larger in the lightly doped material.

The current-voltage (IV) characteristics of the Schottky diode on the sample with the highest degree of passivation (acceptor profile shown in Fig. 2) are shown in Fig. 4. The drastically reduced forward current indicates that the passivated layer is highly resistive. From the differential resistance of the forward IV curve, we estimate a specific resistance in excess of 1 MΩcm of the passivated epitaxial layer.

Discussion

To derive the thickness of the passivated layer, s, from CV-data in the low temperature regime (up to 500 K), we are using a 2-layer-model consisting of a fully passivated layer of thickness s and no passivation beyond. Using Poisson's equation to describe the band bending $\varphi(x)$ below the Schottky contact, this model corresponds to an electrically neutral region with a linear $\varphi(x)$ dependence in the depth region [0; s] and a constant charge density of $-eN_A$ and thus a parabolic $\varphi(x)$ dependence in the region [s; w] where w is the width of the space charge region. By matching both layers to one $\varphi(x)$ function, the depth s of the passivated layer is obtained:

$$s = \sqrt{w^2 - \frac{2\varepsilon U_D}{eN_A}}$$

($\varepsilon = \varepsilon_r \varepsilon_o$ dielectric constant)
(e = elementary charge)

The diffusion voltage U_D of the Schottky diode (1.8 .. 2.1 eV) was taken from an unimplanted reference contact, assuming that the Schottky barrier height is not influenced by H implantation. The depth s determined from CV data by this formula is indicated in Fig. 1 by a vertical line. Within errors (10 %), this depth obtained agrees well with the range of the ^{2}H profile determined by SIMS, thus validating the 2-layer model.

To understand the thickness s as a function of fluence (or implantation time), we are using a

simple model already discussed for silicon by Seager et al. [7]. A rectangular depth profile of H can be understood by assuming a very fast and irreversible trapping of H at acceptors. Free H will immediately be trapped, resulting in the growth of a fully passivated layer. To continue the growth, H has to move through the fully passivated layer to find free acceptors at the interface to the unpassivated layer deeper in the sample. Hence, the flux j of hydrogen through the passivated layer is directly related to the growth rate ds/dt, since all H transported through this layer is trapped at its end: $j = N_A\ ds/dt$. As a driving force of this H flux, we may either assume free diffusion or an ion drift [6] in the intrinsic electrical field due to surface band bending. For both cases, the dependence of the layer thickness s on time and doping level N_A will be the same (i.e. a distinction between these two cases cannot be derived), namely $s(t) \sim (t / N_A)^{1/2}$ [7]. This expectation is well reproduced by the experimental data in Fig. 3: the straight lines reflect a square root function (fluence and implantation time are proportional in our experiments). The vertical offset of the two data sets for different doping levels equals the square root of the doping ratio and thus confirms the $N_A^{-1/2}$ dependence.

The two temperature regimes are understood by the dissociation temperature of Al-H complex of about 500 K [6, 8]. In the low temperature regime, the diffusion of H is determined by an irreversible trapping as discussed above. At higher temperatures, the Al-H complex is no longer permanently stable and there is a dynamic equilibrium between formation and dissociation. Due to the ongoing H supply during implantation, there is still some passivation, but the degree of passivation may be smaller than at low temperatures. We have already shown by TAS [5] that this partial passivation happens at Al acceptors whereas the B-H complex is more stable, i.e. B is fully passivated in the temperature range discussed here.

Conclusions

During low-energy implantation, hydrogen is mobile in SiC already at room temperature and passivates the acceptors B and Al. Up to 500 K, a sharply defined, fully passivated layer is formed. Its thickness as a function of doping level and H fluence is understood qualitatively. At higher temperatures, the Al passivation is no longer stable and, consequently, partial only.

H passivation may be used to produce highly-resistive, 'nearly-intrinsic' SiC in contrast to the known 'semi-insulating' SiC which is produced by compensation. The remaining electrically active acceptor concentration of 10^{14} cm^{-3} or less produced in our experiments is at least one order of magnitude lower than the acceptor concentration in as-grown SiC epi-layers. The thermal stability of this passivation, however, is limited.

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Metal-Contact Enhanced Incorporation of Deuterium in 4H- and 6H-SiC

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Keywords: Deuterium, Diffusion, Secondary Ion Mass Spectrometry

Abstract Deuterium was introduced in p-type SiC from a gas ambient. The samples were partially coated with 200 Å thick metal layer of titanium, nickel, platinum or gold. Heat treatments were performed in the temperature range 500-800 °C during 4 h. Secondary ion mass spectrometry (SIMS) was used to measure the deuterium content after deuterium exposure. The catalytic metal coating is shown to play an important role for introducing deuterium into SiC. Nickel and platinum facilitate hydrogen incorporation in p-type SiC, which may be due to an increased hydrogen concentration at the metal/SiC interface and/or an increase the H^+ ions to H ratio. No in-diffusion of deuterium is observed using titanium although large quantities of deuterium are stored in the titanium film. Furthermore, gold reveals an inert character and does not promote in-diffusion of deuterium.

Introduction

Technologically, the principal interest in hydrogen occurs because of its ability to drastically change the electrical properties of semiconductor devices [1, 2]. Hydrogen can be introduced intentionally or unintentionally during several device processing steps such as, crystal growth, exposure to a plasma, hydrogen containing reagents, annealing steps, and ion implantation. For example, high concentrations of hydrogen have been found in epitaxial grown p-type layers [3].

In this work we have studied the incorporation of deuterium into p-type and n-type 4H- and 6H-SiC from a gas ambient. Metal covers of titanium (Ti), nickel (Ni), platinum (Pt) and gold (Au) have been utilized. Secondary ion mass spectrometry (SIMS) is used to determine concentration versus depth profiles. Deuterium (^{2}H) is employed instead of ordinary hydrogen (^{1}H) to increase the sensitivity of the SIMS measurements by three orders of magnitude.

Experimental

Bulk p–type aluminum doped SiC samples of polytype 4H and 6H with net dopant concentrations of $2.3\text{x}10^{18}$ cm^{-3} (4H) and $1.5\text{x}10^{18}$ cm^{-3} (6H) were mainly used. SIMS measurements showed that the substrates also contained boron to a concentration of $1\text{x}10^{16}$ cm^{-3} and $4\text{x}10^{16}$ cm^{-3}, in the 4H and the 6H samples, respectively. A 200 Å thick metal film of Ti, Ni, Pt or Au were evaporated on one half of the samples. Heat treatments were performed at temperatures ranging from 500 to 800 °C in a gas mixture of deuterium (5%) and nitrogen, with a gas flow of 200 ml per minute. After 4 hours of heat treatment, the samples were removed from the hot zone to a cold region retaining the deuterium/nitrogen flow.

Analysis of the deuterium depth distribution was performed using a Cameca IMS 4f microanalyser. A sputtering beam of 13.5 keV $^{133}Cs^+$ ions was rastered over an area of 200x200 μm^2 and secondary ions of $^2H^-$ were collected from the central region (~60 μm). The erosion rate was typically 5-20 $Å s^{-1}$ as determined by crater depth measurements using an alpha step surface stylus profilometer.

Results and discussion

Fig.1 displays the deuterium depth profiles of the 4H and 6H p-type samples, with and without Pt coating, after heat treatment at 700 °C during 4 h. If deuterium is introduced into p-type SiC it will form complexes with boron and aluminum, where the trapping at 700 °C is primarily caused by boron [4-6]. This trapping is actually necessary to detect the migration of deuterium since free deuterium diffuses at concentration levels well below the SIMS-detection limit. It appears from Fig.1 that the deuterium has diffused into the sample under the platinum coating while measurements outside the metal region only show the ^2H background level. The deuterium concentration follows closely the boron concentration in both the 4H and 6H samples. Since boron is expected to be immobile at these temperatures, this indicates that deuterium-boron pairs are formed in both samples, irrespective of polytype. Similar results are obtained for the p-type 6H-SiC samples heat treated at 600 and 800 °C during 4 hours (Fig.2), while no deuterium is observed at 500°C (not shown). In contrast to the p-type samples, no deuterium is detected in the n-type samples after heat treatment in the temperature range 500 to 800 °C during 4 hours, neither with nor without the Pt coating. This may be due to either slow diffusion of deuterium in n-type material or the lack of trapping centers which facilitate detection.

The catalytic metal coating plays an important role for introducing deuterium into SiC from gas phase as shown for Pt in Fig. 1. To investigate the effect of the type of coating metal, samples were covered with Ti, Ni, Pt or Au and then heat treated at 700 °C for 4 hours (Fig. 3). Ni and Pt layers promote deuterium incorporation in p-type SiC. In the case of Ti and Au, no deuterium is detected in the SiC although a high deuterium concentration is found in the Ti film. The results for Au is in good agreement with a negligible solubility of hydrogen in Au [7].

Hydrogen molecules are decomposed to hydrogen atoms on the Ti, Ni and Pt surface and diffuse into the metal where they can accumulate to high concentrations [7]. Thus, the concentration of hydrogen at the metal/SiC interface will be remarkably higher than the surface concentration at the uncoated region. In the titanium film dihydride will form and it may reduce, even at 700 °C, the amount of free hydrogen available at the Ti/SiC interface [8]. Therefore, Ni and Pt will promote a larger indiffusion of hydrogen than Ti. Here, it should also be pointed out that Pt forms silicides while Ti and Ni can form both silicides and carbides with SiC in the studied temperature range [9].

Finally, the increased deuterium concentration at the interface may not be the only reason for the deuterium diffusion under the metal. In p-type SiC hydrogen is mainly diffusing as a positively charged species [10, 11] and the platinum film may also enhance a transfer from hydrogen atoms (H) to hydrogen ions (H^+). If H^+ is formed, the electrical field introduced by the metal will force the hydrogen into the sample. All metals used in this study form Schottky barrier contacts on p-type SiC, with Ti having the largest barrier height [12].

Summary

Our experiment shows that metal contacts of Ni and Pt on p-type SiC can drastically enhance the probability for incorporation of hydrogen from a gas ambient. Trapping centers are needed to detect the migration of deuterium in annealing experiments using SiC. The deuterium concentration follows closely the boron concentration in both 4H and 6H samples most likely caused by a

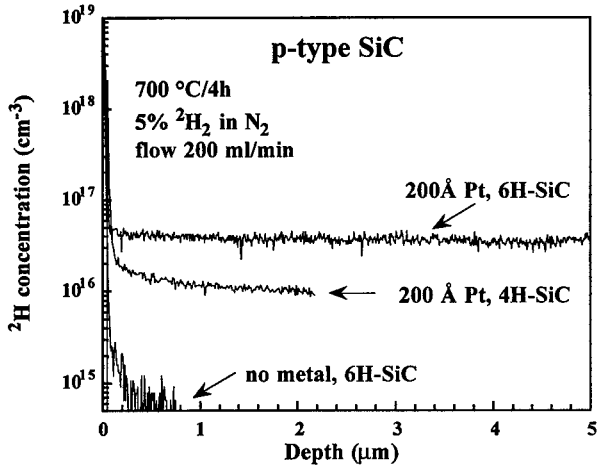

Fig. 1. SIMS measurements of the deuterium concentration versus depth in p-type 4H- and 6H-samples annealed at 700°C for 4 h in a deuterium (5%) and nitrogen ambient (flow 200 ml/min). Three analysis are performed, two on samples which have been coated with a 200 Å thick Pt layer during the anneal and one on an uncoated sample.

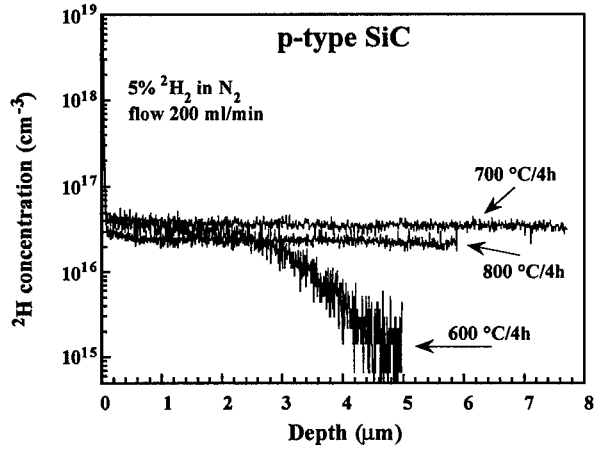

Fig. 2. Deuterium concentration versus depth for three p-type 6H-SiC samples measured by SIMS. The samples were annealed in a deuterium (5%) and nitrogen atmosphere (flow 200 ml/min) for 4 h at 600°C, 700°C and 800°C, respectively. All samples were coated with 200 Å Pt.

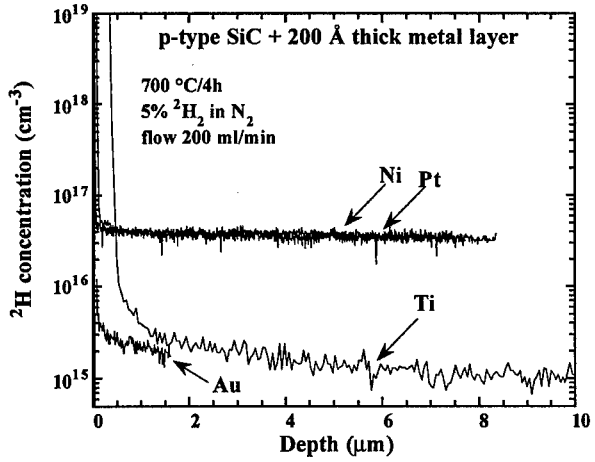

Fig. 3. SIMS measurement of deuterium concentration versus depth in p-type 6H- samples coated with 200 Å of Ti, Ni, Pt or Au. The samples were annealed at 700°C for 4h in a deuterium (5%) and nitrogen ambient (flow 200 ml/min).

formation of boron-deuterium pairs in both polytypes. In n-type material no deuterium is detected after heat treatment at temperatures ranging from 500 to 800 °C for 4 h, neither with nor without Pt coating.

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Transient-Enhanced Diffusion of Boron in SiC

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Keywords: Carbon/Boron-Coimplantation, Kick-Out Mechanism, Outdiffusion, SIMS

Abstract

The redistribution of implanted box-shaped and Pearson B profiles subsequent to annealing steps were studied in 6H-SiC by Secondary Ion Mass Spectrometry. The enhanced diffusion of B can strongly be suppressed by a surplus of carbon. During the annealing process a transient behavior of the B diffusion is observed.

Introduction

Ion implantation into SiC requires annealing steps at high temperatures (T_a up to 1700°C) to remove the lattice damage and to achieve the desired electrical activation of implanted dopants. Unlike implanted aluminum (Al) or nitrogen (N) profiles, which do not show any significant redistribution in SiC subsequent to annealing processes at elevated temperatures [1,2], boron (B), which resides at Si lattice sites in SiC, exhibits strong diffusion at temperatures above 1400°C [3]. In addition, outdiffusion of B occurs, which can lead to a complete depletion of the implanted B profile [4]. The findings obtained for the B diffusion in 4H-SiC reveal distinct analogies to the transient-enhanced diffusion (TED) of B in Si [5]; it was, therefore, proposed that the B diffusion in SiC can also be described in the framework of the kick-out mechanism [4]:

$$B_S + I_{Si} \rightleftarrows B_I \qquad \text{(Eq. 1)}$$

where subscripts S and I denote B atoms residing at substitutional and interstitial lattice sites, respectively; I_{Si} stands for Si interstitials.
In this paper, we have studied the effect of coimplanted carbon (C) on the redistribution of implanted B profiles and the time dependence of the transient-enhanced diffusion behavior of B.

Experimental

Two sets of samples (each consisting of six samples) were cut from an n-type 6H-SiC substrate overgrown by an n-type epitaxial layer ([N] = $7x10^{15}$ cm^{-3}, thickness = 7µm, CREE Research). B and C/B box-shaped profiles to a depth of 0.5µm and of a mean concentration of $5x10^{18}cm^{-3}$ were generated by multiple implantation (sequence: first C implantation followed by B implantation) in samples of set 1 and set 2, respectively (for ion energies and fluences, see Table 1; the implanted profiles are calculated with TRIM-2D). The samples were annealed at 1700°C in Ar ambient and protected in a SiC container; the annealing time t_a was varied between 5min and 180min. The anneals were conducted in a sublimation furnace using a pyrometer for the temperature control. A third set of samples (consisting of sample T1 and T2) was prepared to demonstrate the effect of the C/B coimplantation on Pearson B profiles. Sample T1 was first implanted with a C box-shaped profile to a depth of 1µm and of a mean concentration of $5x10^{18}cm^{-3}$ followed by implantation of

Table 1. Ion energies and fluences used to implant a B and C/B box-shaped profile in samples of set 1 and set 2, respectively (depth=0.5 µm, mean concentration=$5x10^{18}$ cm^{-3}; the implantation parameters are calculated with TRIM-2D)

implanted element	ion energy (keV)	fluence (10^{13} cm^{-2})
C-12	20	2.7
	60	4.1
	120	5.0
	190	5.2
	270	7.0
B-11	20	2.7
	50	4.0
	90	4.9
	140	5.1
	200	7.3

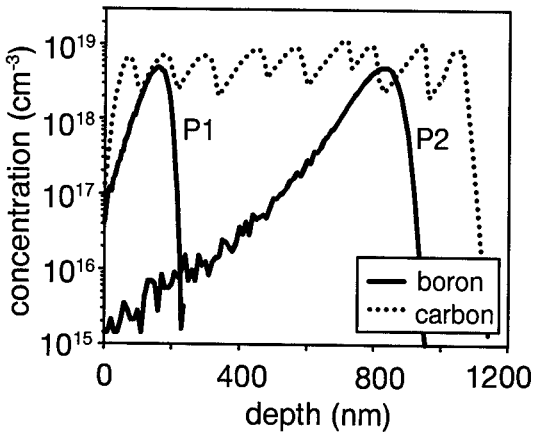

Fig.1 Implanted box-shaped C profile and Pearson B profiles (P1, P2) as used for samples T1/T2.

two Pearson B profiles P1/P2 with parameters: E_1 = 60keV, D_1 = $4x10^{13}cm^{-2}$ / E_2 = 500keV, D_2 = $7x10^{13}cm^{-2}$ (the C/B-coimplanted profiles are plotted in Fig.1). Sample T2 was only implanted with the two Pearson B profiles. Both samples were annealed at 1700°C for 180min under identical conditions as the first two sets of samples. The depth distribution of B was determined with Secondary Ion Mass Spectrometry (SIMS) using an ATOMIKA A-DIDA 3000-30 system (primary ions: 12keV O_2^+). The depth scale was calibrated with a stylus profilometer, the concentration scale for B was obtained from a Relative Sensitivity Factor (RSF) determined in the as-implanted sample.

Experimental results

Fig.2 displays three measured B SIMS profiles: a) The as-implanted B profile (solid curve, see Table 1), which agrees well with the calculated B profile (not shown here). b) The B-implanted profile annealed at 1700°C for 30min (dashed curve, set 1 sample), which shows a diffusion tail into the bulk and a dip in the B concentration in a depth of about 50nm; a pile-up of B is again observed to the surface. The residual B fluence (calculated by integration of the B depth profile) is 45 % of the implanted fluence. c) The B profile of the C/B-coimplanted and annealed (1700°C, 30min) set 2 sample (dotted curve), which reveals a steep trailing edge clearly indicating that the B diffusion is suppressed into the bulk. The shape of the SIMS profile close to the surface is almost identical with the dashed curve; the residual B fluence of 76 %, however, implies that the outdiffusion of B is strongly reduced. In order to study the time dependence of the B outdiffusion in B-implanted and C/B-coimplanted samples, we annealed samples of set 1 and set 2 at 1700°C for different annealing times (5min to 180min).

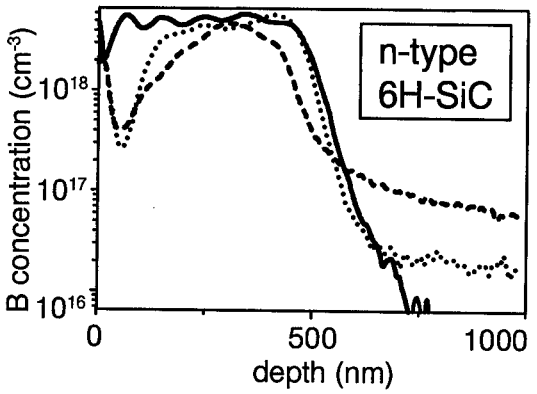

Fig.2 Measured SIMS profiles of B-implanted set 1 sample (solid curve), of B-implanted and annealed (1700°C/30min) set 1 sample (dashed curve), and of C/B coimplanted and annealed (1700°C/30min) set 2 sample (dotted curve).

From the corresponding SIMS profiles, the residual B fluences were determined; they are plotted in Fig.3 as a function of the annealing time t_a. The triangles/circles correspond to the SIMS data measured in set 1/set 2 samples.

Within the first 30min the residual B fluence strongly decreases in both sets of samples; the B fluence of set 2/set 1 samples drops down to $1.6x10^{14}cm^{-2}/0.8x10^{14}cm^{-2}$ demonstrating that an enhanced B diffusion to the surface and at least a partial outdiffusion of B occur during this period. The B outdiffusion in C/B-coimplanted samples is reduced by a factor of approximately 2. For annealing times t_a>30min, both curves run parallel and reveal only a slight decrease of the residual fluence indicating that the outdiffusion is retarded. This behavior is typical for a „transient-enhanced diffusion", which is e.g. also observed for the B diffusion in Si [5].

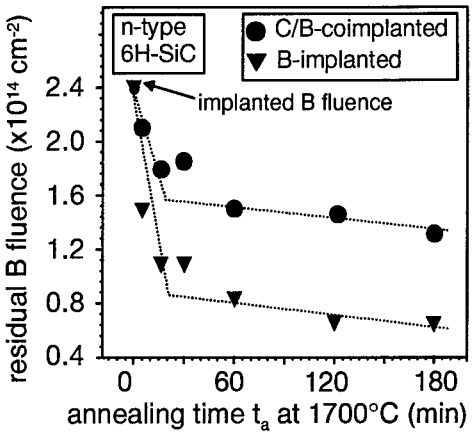

Fig. 3. Residual B fluence as a function of the annealing time t_a; the annealing temperature is 1700°C: Circles/triangles correspond to set 2/set 1 samples.

In order to demonstrate the influence of the surface on the transient-enhanced diffusion of B, we implanted two Pearson B profiles (P1/P2) with differing distance (200nm/800nm) from the surface. The solid curve in Fig.4 reveals the Pearson B profiles determined by SIMS in the as-implanted sample T2. The dashed curve corresponds to the B distribution in sample T2 subsequent to the annealing step. The B profile P1 completely vanished, apparently the B atoms were transported to the surface and evaporated from there (at least partially) during the annealing process; a sharp pile-up of the B concentration is measured close to the surface. The maximum of the deep profile P2 is decreased to a concentration of $10^{18}cm^{-3}$, the width of the profile is symmetrically broadened. The dotted curve shows the B distribution in the C/B-coimplanted sample T1 subsequent to the annealing step. The shallow profile P1 is depleted to a concentration of $4x10^{17}cm^{-3}$. The shape of profile P2 became asymmetric; the position of the maximum is almost unchanged. The trailing flank is still preserved, however, it is slightly moved to the surface. The interesting feature is the broad plateau, which developed on the leading flank of profile P2 in a depth from approx. 300nm to 700nm. B atoms accumulated in this region to a concentration of $9x10^{17}cm^{-3}$; apparently the B diffusion front originating from profile P2 has not yet reached the surface.

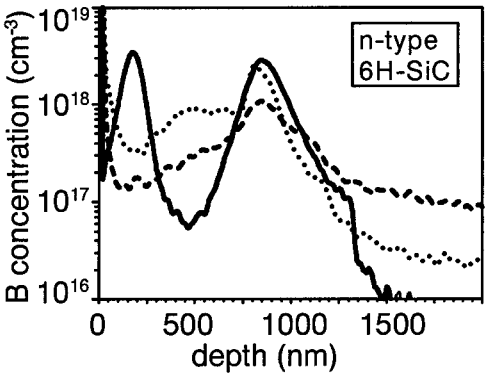

Fig. 4. Measured SIMS profiles of sample T2 prior to (solid curve) and subsequent to (dashed curve) annealing at 1700°C/180min anf of sample T1 subsequent to annealing at 1700°C/180min (dotted curve).

Discussion

At the present, there exists no microscopic or macroscopic model in the literature, which describes the diffusion mechanism of B in SiC. Our proposed diffusion model that aims to explain the observed experimental data is, therefore, speculative and predominantly based on analogies to

the B diffusion in Si. In Ref. 4, it is already proposed that the basic diffusion process of B in SiC is governed by the kick-out mechanism, which requires Si interstitials I_{Si} (see Eq.1). In our implantation experiments, a supersaturation of I_{Si} is generated by the implantation damage and the occupation of Si lattice sites by B atoms. In addition, the implantation forces a disturbance of the stoichiometry caused by the different masses of Si and C. The heavier mass of Si is responsible that an additional surplus of Si atoms is accumulated in a region close to the surface [6,7]. During the annealing process, Si interstitials become highly mobile and are driven to the surface, which enhances the diffusion of B atoms to the surface via the kick-out mechanism (see e.g. plateau (dotted curve) in Fig.4). The surface acts as a sink for both species; Si and B atoms are evaporated during the anneal at elevated temperatures according to their vapor pressure. The enhanced B diffusion is documented in our experiments by the leading edge of the dashed curve in Fig.2 and by the disappearance of profile P1 (dashed curve) in Fig.4. The increase of the B concentration near the surface is still a crucial question, which has to be investigated by further experiments. It seems possible that residual B atoms at the surface are driven in by knock-on collisions with primary ions of the SIMS beam, which may lead to the steep increase of the B concentration near the surface. With increasing annealing time the supersaturation of I_{Si} is reduced retarding the B outdiffusion as demonstrated in Fig.3 (for B diffusion in Si, see [5]). This transient-enhanced diffusion behavior can strongly be suppressed by a surplus of C (in our case by coimplantation of C). We suggest that C-atoms bind Si-interstitials and form stable (I_C-I_{Si})-pairs like in Si. In Si, these dumbbell-like pairs reside at substitutional lattice sites[8]. In SiC, the microscopic structure of these pairs and their lattice position are unknown. All the I_{Si} that are bound to a C atom are no longer enabled to contribute to the B diffusion. The reduced B diffusion is demonstrated by the dotted curves in Figs. 2 and 4 as well as by the data of the residual fluence (circles) in Fig.3. Moreover Scholz et al. [9] predict a remarkable undersaturation of I_{Si} in Si also outside of the C profile; this prediction may explain the steep trailing edges of the dotted curves observed in Figs.2 and 4.

Summary

We have presented SIMS depth profiles, which clearly demonstrate the enhanced diffusion of B in SiC. Coimplantation of C strongly suppresses the B diffusion. It is proposed that the kick-out mechanism dominates the B diffusion. During the annealing step at elevated temperatures, the concentration of I_{Si} is reduced leading to a transient behavior of the B diffusion.

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Materials Science Forum Vols. 338-342 (2000) pp. 945-948

Selective Doping of 6H-SiC by Diffusion of Boron

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Keywords: Cathodoluminescence, Diffusion, Graphite Mask, Photoluminescence, Selective Doping

ABSTRACT: Selective doping of 6H-SiC by diffusion of boron into SiC has been realized at 1800-2100°C using graphite film as a protecting mask. The minimum thickness of graphite film preventing the boron penetration into the substrate was found. Cathodoluminescence measurements as well as an anodic oxidation technique have been employed to identify the local doped regions. A diffused planar *p-n* diode based on the local p-type emitter region was fabricated. The *I-V* characteristic of the formed diode has been measured at room temperature.

1. INTRODUCTION

The 6H-SiC polytype is a promising wide bandgap semiconductor to be used as a substrate material in high-frequency, high-temperature and high-power devices [1]. However, there are still numerous problems in forming planar device structures with selectively doped regions which play an important role in electronic device and IC technology. Presently, in SiC technology, selective doping is realized by ion implantation through a mask followed by a high temperature annealing to reduce the lattice damage. However, incomplete electrical activation of the impurities and shallow with abrupt *p-n* junction formation via ion implantation limit the potential features offered by SiC.

An alternative method of selective doping of SiC is via diffusion. Although the phenomenon of diffusion in SiC has been studied thoroughly, there are limitations in using this process widely in semiconductor device technology [2,3]. Since the dopant atoms in SiC become moveable at temperatures above 1800°C, the high temperature creates additional difficulties for realizing and controlling the process. On the one hand it is necessary to have a high temperature protective mask, and on the other hand it is necessary to create the equilibrium conditions in a crucible to eliminate the sublimation and epitaxial growth during diffusion.

To the best of our knowledge, no studies of high temperature selective diffusion in SiC using graphite mask have been reported to date.

Selective diffusion into 6H-SiC and *p-n* junction diodes fabricated using local doped regions are reported in the present study.

2. EXPERIMENTAL

To prepare the test samples, commercial CREE n-6H-SiC wafers with a 10μm thick nitrogen-doped epilayer with a carrier concentration of $4.1 \times 10^{15} cm^{-3}$ and a n-6H-SiC substrate wafer with background doping concentration of $\sim 10^{18} cm^{-3}$ were used.

In order to realize selective doping into the SiC sample, a graphite film was formed on the surface as a protecting mask. Boron diffusion was carried out in Ar ambient using an induction heating vertical quartz chamber with water-cooled walls. The temperature and time of diffusion varied from 1800 to 2100°C and from 5 to 30 min, respectively. A graphite crucible with a mixture of silicon carbide powder and elemental boron (a source of the doping atoms) was used. The uniform temperature distribution with minimal gradients and equilibrium SiC vapor pressure were created inside the crucible to avoid undesirable evaporation and/or epitaxial growth during diffusion. Since diffusion penetration of the boron atoms takes place at the uncovered backside of the sample as well, the backside diffusion layer was removed by lapping with a diamond paste.

After diffusion, in order to carry out photoluminescence (PL) and cathodoluminescence (CL) measurements, the graphite mask was removed from the samples. A diode structure, as shown in Fig.1, was fabricated using standard photolithography technologies. The SiO_2 provides edge-termination of the diode metal contact. After the deposition of aluminum as a contact to the p-type region and nickel on the backside, the samples were annealed at 600°C in vacuum to form ohmic contacts.

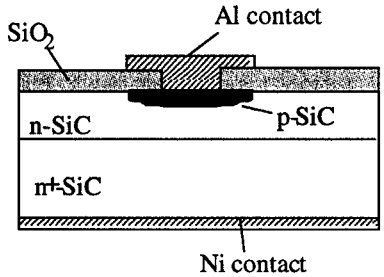

Fig.1. Schematic test structure of the p-n diode

3. RESULTS AND DISCUSSION

To study the protecting properties of the graphite mask, PL measurements were carried out at the surface regions covered by a graphite mask with different thicknesses and at the uncovered region as well. The luminescence was excited by a He-Cd laser providing an UV line at the wavelength λ=325 nm. The total laser power was 52 mW at a spot size of about 20 μm. Fig.2 shows the relative photo-luminescence intensity of samples that previously had been covered by graphite masks with different thicknesses as a function of the wavelength in the range 400-800 nm. The spectra corresponding to a sample with no mask during diffusion and to a sample with no diffusion are included for comparison. The room temperature spectrum (300 K) displays a broad peak with a maximum at λ=572 nm ($h\nu$=2.14 eV). The occurrence of the yellow luminescence is typical for 6H-SiC doped by boron. The lower peak of PL intensity for a sample where diffusion was performed through a 1μm thick mask indicates lower boron concentration in the doped region. Thus, according to these data we could conclude that the minimum graphite mask thickness preventing the boron penetration is ≈2.7 μm.

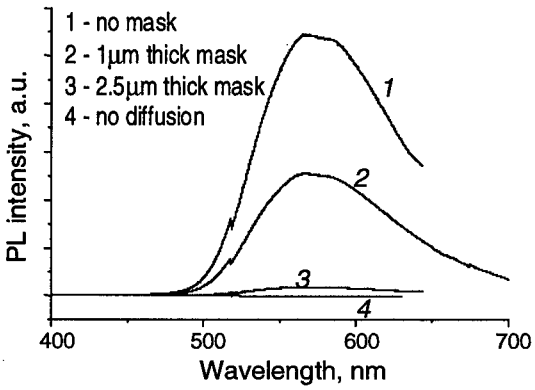

Fig.2. Photoluminescence spectra of 6H-SiC after selective doping by boron at different mask thicknesses

The CL image technique was used to obtain the boron distribution over the surface of the sample. The luminescence was excited by an electron beam of 10 keV energy in order to ensure that the depth of excitation was low. The CL image of the 6H-SiC with local doped regions is shown in Fig.3. This picture clearly confirms that the boron penetration into a SiC substrate takes place only in the areas not covered by the graphite mask. The brighter circles and lines indicate

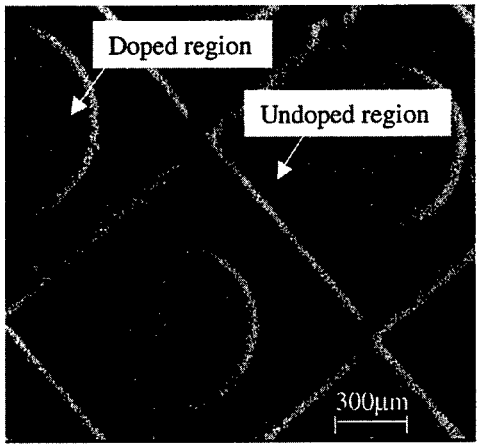

Fig.3. Cathodoluminescence image of doped 6H-SiC by diffusion of boron selectively

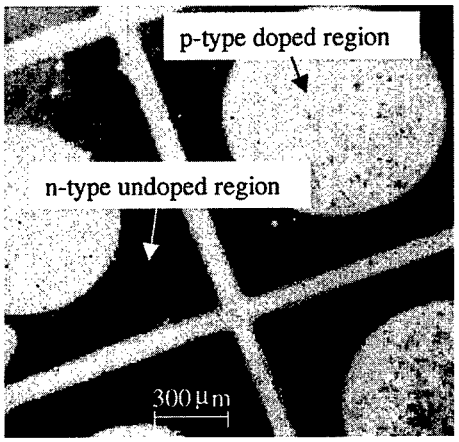

Fig.4. Microphotograph of selectively doped 6H-SiC wafer without epilayer by boron diffusion, after anodic oxidation.

the diffused regions. In addition, the SEM picture was also taken at the same region. But no pattern was observed on the surface. This lack of pattern means that diffusion occurred at equilibrium vapor conditions without the parasitic evaporation or epitaxial growth on the unmasked regions.

Furthermore, the anodic oxidation technique has been used to distinguish regions with different values of conductivity [4]. Due to the different values of current passing through regions with different resistance, the rate of anodic oxidation on those regions is different. This leads to the formation of oxide with different thickness. As a result, a characteristic pattern is formed on the surface. A microphotograph of this oxidized surface is shown in Fig.4. In fact, it is the same pattern which was revealed by the CL image and which corresponds to the applied graphite mask. Note that the CL images can be taken both on wafers with epilayer and without, while it is very difficult to obtain an oxide film on a SiC sample with an epilayer due to its high resistivity.

Simple diffused *p-n* diode structures were fabricated on SiC wafers having a diffused region pattern as shown in Fig.3 and Fig.4. The diameter of the circle windows and the metal contacts were 650 and 350*μm*, respectively. The *I-V* characteristic of the diode presented in Fig.5 shows good rectification properties. The value of breakdown voltage for this diode measured at room temperature was a little greater than 800 V, and the leakage current was $2x10^{-7}$A at 800 V. The forward voltage drop corresponding to 100A/cm^2 is about 12 V. This high value is explained by the relatively high resistance of the p-layer due to the fact that boron in SiC gives two levels in the band-gap energy, resulting in compensation of the n-SiC.

4. CONCLUSION

In summary, selective boron diffusion into 6H-SiC has been realized using a graphite film as the protecting mask. The minimum thickness of graphite film preventing the boron penetration into SiC substrate was about 2.7 μm. Cathodoluminescence measurement as well as anodic oxidation techniques have been used to identify the local doped regions. A diffused planar *p-n* diode based on the local p-type emitter region has been fabricated. The *I-V* characteristic of the formed diode exhibited good rectification properties.

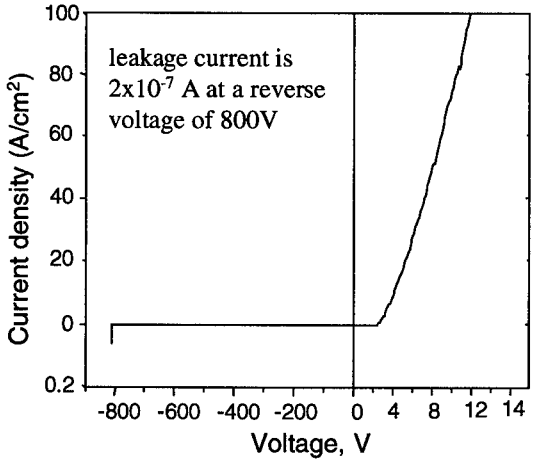

Fig.5. *I-V* characteristic of a diffused p-n diode fabricated in the local doped region.

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Materials Science Forum Vols. 338-342 (2000) pp. 949-952

Ab Initio Study of Intrinsic Point Defects and Dopant-Defect Complexes in SiC: Application to Boron Diffusion

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Keywords: Ab Initio Defect-Energetics, Boron, Defect Complexes, Diffusion, Point Defects

Abstract We apply an *ab initio* method to study intrinsic interstitials, vacancy-antisite complexes, boron interstitials and boron-vacancy complexes in SiC. The electronic and atomic structure as well as the energetics of the defects is calculated. The stability of substitutional boron and aspects of the migration of impurities are discussed.

Introduction

In recent experiments boron-implanted SiC samples were shown to exhibit a transient enhanced diffusion of the dopant [1], which is well known for silicon [2]. The current interpretation of the diffusion mechanism has to rely on the analogy with silicon, as the microscopic understanding of the defect energetics and migration in SiC is lacking. The purpose of the present work is to investigate the relevant point defects and their pair complexes by means of *ab initio* total energy calculations. We present results for intrinsic interstitials, interstitial boron, vacancy-antisite complexes and boron-vacancy complexes. To preserve simplicity, we have restricted the investigation to the cubic 3C-SiC.

Method

In a compound material such as SiC, formation energies of defects depend on the chemical potentials of the constituents μ_C, μ_{Si} as well as on the dopants (boron) chemical potentialμ_B [3]. In a thermodynamical equilibrium $\mu_{SiC} = \mu_C + \mu_{Si}$ holds. We express μ_{Si} as $\Delta\mu_{Si}$, the deviation from the chemical potential of solid silicon. To preserve the stability of SiC, $\Delta\mu_{Si}$ is restricted to values between 0 (Si-rich condition) and $-\Delta H_f$ (C-rich condition), where ΔH_f is the heat of formation of 3C-SiC. The calculations have been performed using the program package FHI96MD [4] within the framework of density functional theory and the local density approximation (LDA) [5]. A supercell of 64 atoms (216 atoms in selected test cases) was used. Smooth norm conserving pseudopotentials of the Troullier-Martin type [6], a plane wave basis of 30 Ry and special k-point sampling are employed.

Intrinsic defects

Interstitials There are several sites which may host interstitials in the SiC lattice: two tetrahedral positions with either carbon or silicon neighbours (C_{TC}, C_{TSi}, Si_{TC}, and Si_{TSi}), hexagonal sites with three silicon and carbon atoms as nearest neighbours (C_{Hex} and Si_{Hex}) and the split interstitials, where two silicon or carbon atoms share one lattice site with the

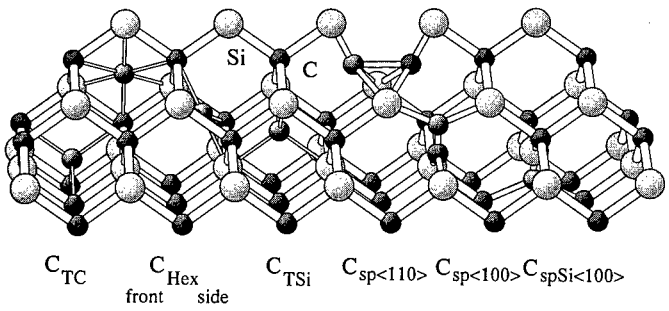

Figure 1: The geometry of different carbon interstitials. The silicon interstitials have corresponding geometry. The interstitials Si_{Hex} and $Si_{spC\langle 100\rangle}$ are unstable.

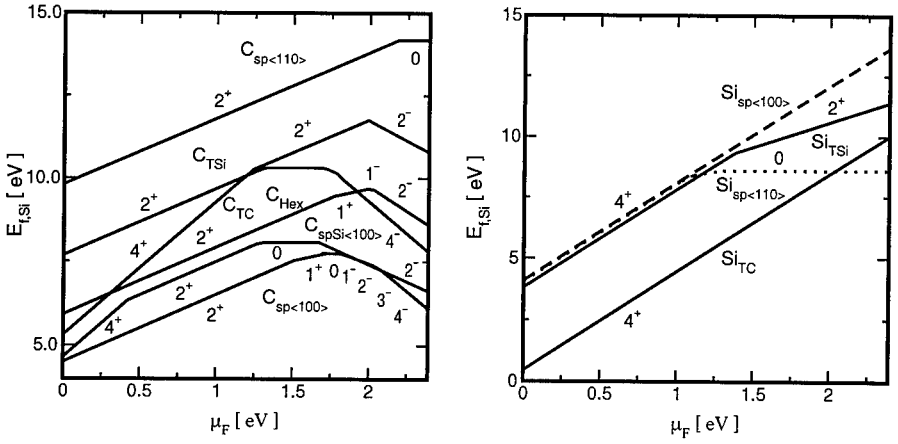

Figure 2: Formation energy $E_{f,Si}$ of the stable carbon and silicon interstitial defects vs. the Fermi-level position μ_F for Si-rich conditions, i.e. $\Delta\mu_{Si} = 0$. The different charge states of the defects are indicated.

axis of the pair being oriented in either $\langle 110\rangle$ or $\langle 100\rangle$ direction ($C_{sp\langle 110\rangle}$, $C_{sp\langle 100\rangle}$, $Si_{sp\langle 110\rangle}$, and $Si_{sp\langle 100\rangle}$) (Fig. 1). The other orientations of the split interstitials were found to be unstable. The mixed split interstitial, consisting of a silicon and carbon atom, is stable only on a silicon site with orientation in the $\langle 100\rangle$ direction ($C_{spSi\langle 100\rangle}$). The Si_{Hex} is unstable. The calculations show, that the lattice relaxation has a substantial effect on the defect formation energies as well as on the electronic structure. Relaxation energies of about 5 eV were found. The effect is substantiated by relaxation of first, second and third nearest neighbours and is well described within the 64 atoms cell as comparison with calculations in 216 atoms cell show. This explains why in earlier calculations [7], which solely included nearest neighbour relaxation, the formation energies of interstitials have been overestimated.

In figure 2 the formation energies of the carbon and silicon interstitials are shown as a function of the Fermi-level position μ_F for Si-rich conditions ($E_{f,Si}$ denotes the formation energy for $\Delta\mu_{Si} = 0$). All interstitial defects predominantly occur in positive charge states. Only the C-interstitials have negative charge states with ionisation levels well above the mid-

gap. The formation energy of Si_{TC} interstitial, which has no levels in the fundamental band gap, is almost 4 eV lower than for the other interstitials of either type. The predominant C-interstitials are the split interstitials $C_{sp\langle 100\rangle}$ and $C_{sp\,Si\langle 100\rangle}$. Intrinsic interstitials in SiC and silicon behave differently in many respects. Especially tetrahedral interstitials are highly charged and the Si_{Hex} is unstable in all possible charge states.

Vacancies The carbon and silicon vacancies in SiC have been recently investigated experimentally as well as theoretically [9]. Here we address two complexes (V_C-C_{Si}) and (V_{Si}-Si_C) formed by a vacancy and an antisite as a nearest neighbour. We find that the (V_{Si}-Si_C)-complex is unstable, making migration of the carbon vacancy by nearest-neighbour hops impossible. However, the (V_C-C_{Si})-complex turns out to be stable. It has two nondegenerate levels within the upper part of the band gap, which derive from a dangling bond located on the C_{Si} antisite. The V_{Si} and the (V_C-C_{Si})-complex form a bistable pair. Under p-type and intrinsic conditions the (V_C-C_{Si})-complex is the ground state while under n-type conditions the Si-vacancy is slightly lower in energy. This indicates that Si-vacancies in non-equilibrium p-type or intrinsic material should largely transform into (V_C-C_{Si})-complexes upon annealing above a suitable temperature.

Boron impurity

Interstitials Similar to intrinsic interstitials, interstitial boron can occupy two different tetrahedral sites (B_{TC} and B_{TSi}) or a hexagonal site (B_{Hex}). The calculations also show that only the split interstitial at a silicon site oriented in the $\langle 110\rangle$ direction is stable ($B_{spSi\langle 110\rangle}$). With respect to the level structure and energetical ordering boron interstitials resemble Si-interstitials with the exception of the hexagonal site, which is unstable for interstitial silicon. Here the behaviour corresponds to the C_{Hex}-interstitial. However, since boron carries one valence electron less than silicon or carbon the charge states of the boron interstitials changes accordingly. The predominant interstitial is B_{TC}.

To access the energetics of boron interstitials we consider the following kick-out reaction of a substitutional boron (B_C and B_{Si}) with an intrinsic interstitial (denoted by C_I and Si_I)

$$B_C^- + C_I^{q+} \rightleftharpoons B_I^{p+} + (q+1-p)\,e^- \quad \text{and} \quad B_{Si}^- + Si_I^{q+} \rightleftharpoons B_I^{p+} + (q+1-p)\,e^- \quad . \qquad (1)$$

From the energetics of this reaction we deduce, that the substitutional boron defects are metastable with respect to a kick-out reaction by intrinsic interstitial defects. In p-type material the energy gain is more pronounced for the kick-out reaction of B_C than for the kick-out reaction of B_{Si} (6 eV compared to 2.5 eV for the most stable configurations). This result contrasts the situation in silicon [8], where substitutional boron together with a silicon interstitial is energetically more favourable than interstitial boron.

Boron-vacancy complexes Substitutional boron with an adjacent vacancy can form two boron-vacancy complexes: ($B_{Si} - V_C$) and ($B_C - V_{Si}$). A nearest-neighbour hop of boron between the two substitutional sites would convert one complex into the other. However, our calculations show that the ($B_{Si} - V_C$)-complex is by 4 eV to 6 eV (n-type and p-type conditions rsp.) more stable than the ($B_C - V_{Si}$)-complex, making a conversion between the two complexes rather improbable. A similar result was also found in recent *ab initio* cluster calculations [10]. As in the case of the kick-out reaction, substitutional boron might be metastable in the presence of vacancies. This is indeed the case. Our calculations show that both boron-vacancy complexes are lower in energy than the corresponding well-separated non-interacting defects.

Discussion

The physics of intrinsic as well as the boron related defects is distinctly different in SiC than in silicon. The most striking difference is that on-site boron is metastable due to interaction with intrinsic interstitials and vacancies. The resulting boron interstitials and boron-vacancy complexes are deep centres. This process should diminish the doping efficiency. However, the recent successful preparation [11] of electrically active boron-doped 4H-SiC suggests that these reactions are kinetically suppressed. This may partly be due to the large migration barriers of the intrinsic defects, and partly because of the formation of more stable intrinsic defect complexes not investigated in this work. In p-type or intrinsic material Si-interstials (Si_{TC}) and carbon-vacancies (V_C) are the most abundant mobile, intrinsic point defects. The equilibrium concentration of both defects are comparable under these conditions. However, under n-type conditions the carbon-vacancy is more abundant as it has a lower formation energy. For the migration barrier of Si-interstitials we can establish a lower bound of 4 eV in p-type material, if we assume that it proceeds between Si_{TC}-sites with the other stable sites involved as intermediate stages. We can exclude a nearest-neighbour mechanism for diffusion of carbon vacancies because the vacancy-antisite complex formed at the first stage of such a mechanism is unstable.

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Beryllium Implantation Doping of Silicon Carbide

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Keywords: 6H-SiC, Annealing, Beryllium, Damage, Doping, Ion Implantation, SIMS

Abstract

Structural properties of beryllium implanted silicon carbide have been investigated by secondary ion mass spectrometry, Rutherford backscattering / channeling, and Raman spectroscopy. Strong redistribution of beryllium has been found after a post-implantation anneal step at temperatures between 1300 °C and 1700 °C. The use of a pre-anneal process at 1000 °C before the high-temperature treatment as well as graphite as a surface encapsulant do not efficiently suppress redistribution of Be in the SiC lattice. The crystalline state of the implanted and annealed material is well recovered after annealing at temperatures above 1400 °C.

Introduction

Silicon carbide (SiC) is currently being explored as a promising material for the next generation of high-temperature, high-frequency, and high-power electronics. The fabrication of electronic devices requires the modification of electronic properties by doping. The low diffusion coefficients of common dopants at temperatures where surface integrity can be maintained preclude the use of thermal diffusion based techniques for this purpose [1]. Thus, ion implantation seems to be the only possible doping method available for SiC. Beryllium (Be) is known to be an acceptor in SiC [2]. High ion ranges and low crystalline damage are advantages of Be implantation which make this technique suitable for generating thick *p*-type layers in SiC. However, there have been few reports on Be doped SiC [2-10]. Although Be was successfully applied to the fabrication of diodes [9,10], much is still unknown about the structural properties of this dopant in the SiC lattice. Therefore, Be implanted SiC is investigated in this work by secondary ion mass spectrometry (SIMS), Rutherford backscattering spectrometry / channeling (RBS/C), and Raman spectroscopy.

Experiment

10 μm thick *n*-type 6H-SiC epitaxial layers ([0001] orientation, off-axis, [n]=1×10^{16} cm^{-3}) grown on *n*-type substrates from Cree Research [11] were used as starting material. A box-shaped profile was produced by multiple energy $^{9}Be^{+}$ implantation at room temperature (RT) using ion doses in the range 6×10^{13} - 2×10^{14} cm^{-2} and energies between 50 and 590 keV. Range distributions were obtained by Monte Carlo (MC) simulations using the TRIM code (SRIM-98, full cascade) [12]. According to these calculations depth and mean Be concentration of the box profile are expected to be 1.1 μm and 1×10^{19} cm^{-3}, respectively. Samples were annealed in flowing argon (Ar) gas for 1 min at temperatures between 1000 °C and 1700 °C using a rapid thermal annealing (RTA) system. The temperature rise and fall rates were about 50 K/s and 30 K/s. Each sample was covered by another SiC crystal to minimize Si evaporation from the surface during RTA. Be depth profiles

were analyzed by SIMS using a CAMECA ims 4f instrument. The recovery of the crystal lattice after RTA was studied using 3 MeV $^4He^+$ RBS/C and Raman spectroscopy.

Results

SIMS measurements were performed on as-implanted and post-implantation annealed samples to study Be depth profiles with respect to their thermal stability. As can be seen in Fig. 1, the near surface tail and the mean concentration of the as-implanted profile are well reproduced by the MC simulations. However, the slope of the tail towards the substrate is lower compared with the TRIM profile. Channeling effects can be responsible for the observed discrepancy, which are not considered in SRIM-98.

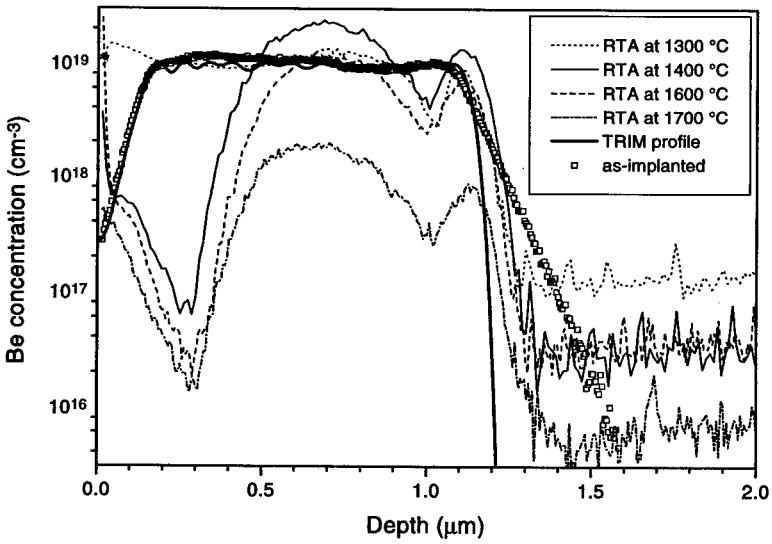

Fig. 1. SIMS ^9Be depth profiles in SiC before and after RTA at the temperatures indicated. A simulated depth profile as obtained by TRIM is shown for comparison.

Strong redistributions were found in the annealed samples. The Be profile is already thermally unstable after a short anneal cycle at 1300 °C. In particular, the heat treatment caused a slight pile-up in the near surface region and in-diffusion into the bulk of the epilayer. Further investigations have shown that the diffusion tail extends to a depth of about 9 μm and may reach even the underlying substrate during annealing at higher temperatures [13]. However, when calculating the integral of the depth profile which is a measure of the retained Be dose, significant lower values compared to the as-implanted distribution were only found above 1400 °C. In particular, 70, 57, and 9 % of the implanted dose was obtained after RTA at 1500 °C, 1600 °C, and 1700 °C, respectively. Since the integrated area under the diffusion tail is always less than 6 % compared to the total area under the as-implanted profile, out-diffusion must be the main reason for the observed Be loss. The strong pile-up at the surface is another indication for out-diffusion.

Evidence for strong redistribution processes during annealing are also the maximum and minimum in the profiles which can be explained in terms of Ostwald ripening [14], i.e., nucleation and growth of Be precipitates caused by a supersaturation of Be in the SiC lattice, especially at lower temperatures, because the solid solubility of Be is lower than the implant concentration [7]. The atomic Be concentration as measured by SIMS decreases at all depths with increasing temperature

(see Fig. 1). This indicates a high Be precipitate formation rate at 1400 °C while a lower rate is anticipated at higher temperatures due to the higher solid solubility. Also, thermally activated diffusion of Be as a competing process can be attributed to this phenomenon.
These findings raise questions about the diffusion mechanism of Be in SiC. If Be diffuses via vacancy sites as proposed in ref. [4], a pre-anneal step before conducting the high-temperature annealing should then suppress diffusion because carbon and silicon vacancies start to anneal out at 150 °C and 750 °C, respectively [15]. Since Be does not noticeably diffuse at 1000 °C [13], a two-step RTA process was performed on one as-implanted sample: a first step conducted at 1000 °C for 5 min followed by a second step at 1600 °C for 1 min. SIMS analysis of this sample revealed a much higher loss of Be compared to the reference sample processed at 1600 °C only (see Fig. 2). In particular, 17 % of the implanted dose remained in the material after the two-step anneal process. Therefore, Be is assumed to diffuse via interstitial rather than vacancies sites. This is corroborated by positron annihilation spectroscopy results indicating that vacancy cluster generated by ion irradiation below the amorphization threshold anneal out at 1400 °C [16]. Hence, their contribution to the redistribution process observed is expected to be negligible.

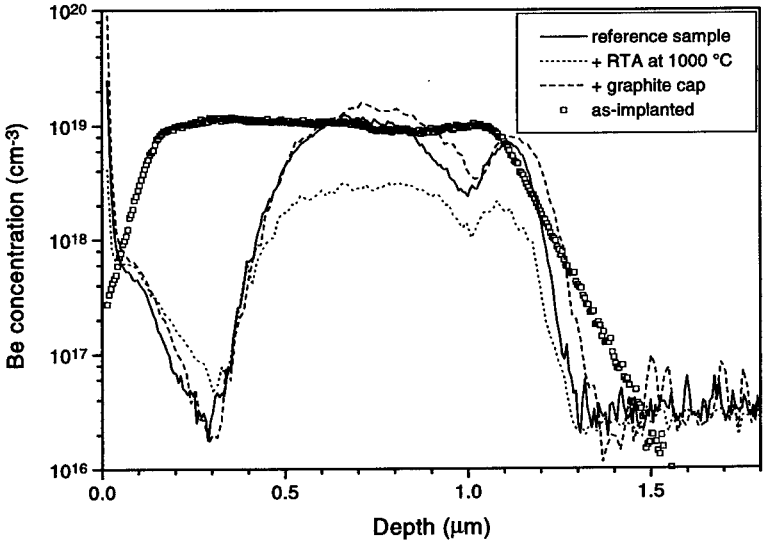

Fig. 2. SIMS Be depth profiles in SiC after annealing at 1600 °C (reference sample), 1000 °C (pre-anneal) + 1600 °C, and 1600 °C using a graphite cap, respectively. The as-implanted profile is also shown for comparison.

Encapsulating the surface before conducting RTA might be another way to suppress out-diffusion of Be. Graphite withstands high temperatures and has a coefficient of thermal expansion close to SiC which are necessary conditions for a suitable encapsulant material. Therefore, an amorphous carbon (a-C) layer containing a high fraction of graphitelike domains (sp^2 bonds) was deposited on another as-implanted sample. It is known that a-C converts to crystalline graphite at temperatures above 1000 °C [17]. As shown in Fig. 2, the encapsulant does not seem to prevent the strong redistribution in the Be profile during annealing. 72 % of the implanted dose remained in the material, which is only a slight improvement compared to the reference sample. This means that out-diffusion cannot be completely suppressed. According to a recent report, AlN as another

encapsulant material also failed to prevent redistribution of boron implants in SiC [18]. Thus, it seems to be difficult to find a suitable encapsulant for this semiconductor.
RBS/C measurements have been performed to evaluate the recovery of the crystal lattice after RTA. The scattering yield in the aligned spectra obtained from samples annealed at temperatures above 1400 °C almost coincides with the yield in the aligned spectrum of the virgin sample at all depths indicating a good lattice quality. Thus, it can be assumed that the crystalline state is well recovered. This is confirmed by Raman spectroscopy results obtained using a confocal microscope system. Neither a broadening nor a shift of the first-order vibrational modes in comparison to virgin material was detected.

Conclusions

Structural properties of Be implanted *n*-type 6H-SiC epitaxial layers were investigated by SIMS, RBS/C, and Raman measurements. Strong redistributions of the implanted profiles accompanied by in and out-diffusion of Be were found after annealing above 1300 °C. The use of a pre-anneal process at 1000 °C as well as graphite as an encapsulant material do not efficiently suppress redistribution of Be in SiC. Finally, the crystalline state is well recovered after RTA at temperatures above 1400 °C.

Acknowledgments

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Materials Science Forum Vols. 338-342 (2000) pp. 957-960

Ion-Channeling Studies of Interfaces and Defect Properties in Silicon Carbide

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Keywords: Amorphization, Defects, Interfaces, Ion Channeling

Abstract

Helium ion channeling has been used in a detailed study of 3C-SiC films on a $Si/SiO_2/Si$ (SIMOX) substrate. The strain-induced angular shift was determined to be $0.16° \pm 0.05°$, indicating a kink between the SiC and Si layers along the <110> axis. Single crystals of 6H-SiC have been irradiated with a variety of ions over a range of fluences. The relative disorder on Si sublattice shows a sigmoidal dependence on dose for all ions. In isochronal and isothermal annealing studies, two distinct recovery stages are identified with activation energies of 0.25 ± 0.1 eV and 1.5 ± 0.3 eV, respectively. Deuterium ion channeling is also applied to simultaneously study accumulated disorder on Si and C sublattices in 6H-SiC crystals irradiated at 100 and 300 K.

Introduction

Silicon carbide (SiC) is an important wide-bandgap semiconductor material with outstanding properties, including high thermal conductivity and stability, high breakdown field, high saturated electron drift velocity, and small capture cross sections for neutrons. Electronic devices based on SiC are recognized as having great potential for applications involving high temperature, high radiation, high power, and high frequency. A fundamental understanding of the accumulation and recovery of irradiation damage in SiC is important both to predicting performance in radiation environments and in using ion-implantation techniques in electronic device fabrication. In this study, Rutherford backscattering spectrometry in channeling conditions (RBS/C) has been used and the results for 3C-SiC films grown on SIMOX substrates and for the 6H-SiC wafers are presented.

Experimental procedures

The thin (nominally, 200 nm) film of 3C-SiC in this study was grown on a SIMOX substrate by the Spire Corporation using conventional CVD methods at a temperature of 1350 °C. The SIMOX structure consists of a top Si layer (nominally, 180 nm thick) with a buried SiO_2 layer (nominally, 123 nm thick) on a Si (100) wafer. The RBS/C measurements along <100>- and <110>-axial directions were carried out using 2.0 MeV He^+ beams at a scattering angle of 150°. The 1.0 mm × 1.0 mm analyzing beams had an angular dispersion of less than 0.05°, as compared to more than 1° FWHM of the angular dip curve under the experimental conditions. Accurate normalization for the incident particle fluence in the RBS/C analysis was achieved by applying a high positive voltage (300 V) to the target in order to suppress the secondary electron emission from the target.

The 6H-SiC single crystal wafers used in this study were obtained from Cree Research, Inc. The irradiation experiments were performed with either 360 keV Ar^+ (incident angle 25° off the surface normal), 550 keV Si^+ ions (30° incident angle), 550 keV C^+ ions (60° incident angle), or 390 keV

He^+ ions (60° incident angle) over a range of ion fluences at low temperatures (between 170 and 190 K). The large incident angles were used to produce near-surface damage that could be analyzed by ion-beam techniques. Profiles of atomic disorder on the Si sublattice were measured *in-situ* using 2.0 MeV He^+ RBS/C along <0001> axial channeling direction. The disorder at the damage peak was obtained from the RBS/C spectra under the assumption of a linear dechanneling approximation from the defects induced in the irradiated crystals.

Isochronal and isothermal annealing procedures were used to study the damage recovery *in situ* using RBS/C. Samples for the thermal annealing studies were irradiated under identical experimental conditions (8.0×10^{14} C^+/cm^2 at 180 K). A sequence of annealing steps were successively carried out isochronally for 20 min each from 220 to 1070 K or isothermally for time intervals of 5 s up to 2400 s at 220, 300, 570 and 870 K, respectively. Channeling measurements after each isochronal or isothermal annealing step were made at temperatures well below the anneal temperature to minimize the defect recombination during data acquisition.

In the deuterium channeling study, ion energy of 0.94 MeV and a scattering or reaction angle of 150° were selected. Because reaction $^{12}C(d,p)^{13}C$ has a large energy release (Q=2.723 MeV), the resulting proton energy is much higher than the deuterium backscattering energy. This condition allows simultaneous measurements of C and Si atoms without spectrum overlap.

Results and discussion

The angular yield profiles around the <110> axis are shown in Fig. 1 for Si in the SiC film, Si layer, and Si substrate, respectively. The dip curves for the Si layer and Si substrate coincide well with each other, but SiC shows an angular shift in the minimum yield position by 0.16° with an accuracy of ±0.05°. However, the corresponding three dip curves for the same specimen around <100> axis are symmetric with minimum yields at the same position [1]. The angular shift is an indication of a superlattice structure at the SiC/Si interface, and their <110> axes are misaligned by ~0.16°. Detailed interpretation about the channeling data can be found elsewhere [1].

The relative disorder on the Si sublattice in 6H-SiC is shown in Fig. 2 as a function of dose for the different irradiation conditions. The disorder shows a sigmoidal dependence on dose for all ions. This dependence is consistent with the defect-stimulated amorphization process suggested for SiC and supported by Molecular Dynamics (MD) simulations. The Ar^+ and Si^+ results are in good agreement; however, there is a shift in the curves to higher doses with decreasing ion mass (damage energy density) for the C^+ and He^+ results. This suggests a higher fraction of defects are lost to simultaneous recombination processes at low damage energies (low ion masses). It is important to note that the relative disorder determined by RBS/C, as shown in Fig. 2, is due to both the accumulation of point defects in the structure (e.g., interstitials) and the formation of amorphous material; consequently, the relative disorder overestimates the actual amorphous fraction, as has been shown previously for SiC [2]. The only possible exception is for the fully disordered or amorphous state, since XTEM results have confirmed that an amorphous layer is present when the dechanneling yield at the damage peak, from RBS/C along <0001>, reaches the random level.

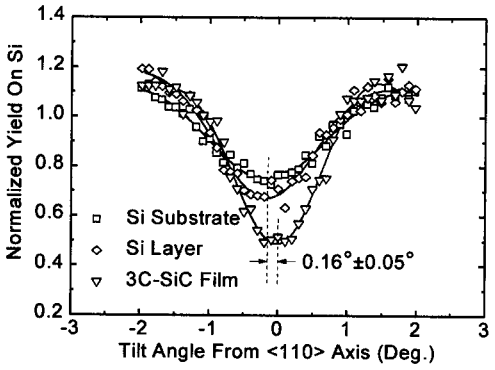

Fig. 1. Angular yield profiles around the inclined <110> axis for the Si element in the thin SiC film, the SiO_2 buried layer, and the Si substrate.

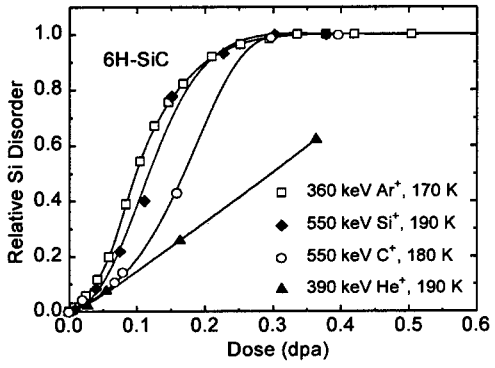

Fig. 2. Relative disorder on the Si sublattice, at the damage peak, as a function of dose in 6H-SiC irradiated with different ions.

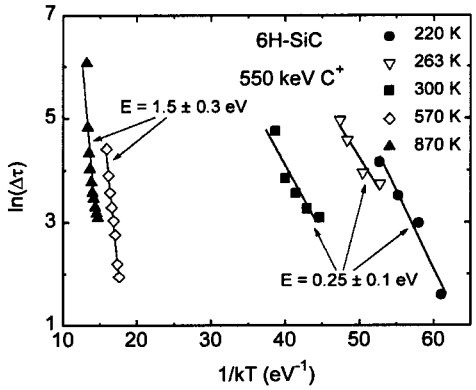

Fig. 3. Arrhenius plot of logarithmic annealing time in isothermal steps versus 1/kT in isochronal annealing.

The migration and annealing of dilute implantation defects, which is of interest in ion implantation technology for electronic device fabrication, has been investigated in 6H-SiC by *in-situ* RBS/C [3]. For low defect concentrations, complete recovery of defects on the Si sublattice can occur below room temperature [4]. The implantation of gas species (H and He) impedes defect recovery processes at low temperatures [5,6]. The results from analysis of isochronal and isothermal annealing data for C^+-implanted 6H-SiC are shown in Fig. 3. Below room temperature, the thermal recovery of defects on the Si sublattice has an activation energy on the order of 0.25 ± 0.1 eV. Defect recovery on the Si sublattice above 570 K has an activation energy on the order of 1.5 ± 0.3 eV, which is in good agreement with results from neutron irradiation studies [7]. These results suggest that there are at least two recovery processes responsible with the observed annealing on the Si sublattice in the investigated temperature range.

The MeV He^+ RBS/C method has become a standard approach for determination of damage profiles in single crystals and has been successfully applied over the years, including the very recent studies on SiC [1,3-6] and GaN [8]. Although this method is convenient to apply to Si sublattice, disorder on C sublattice needs complementary methods for analysis. Instead of using conventional MeV He^+ ions, deuterium ion beams with an energy of 0.94 MeV have been applied to analyze 6H-SiC along the <0001>-axial channeling direction. The simultaneous measurement of the atomic disorder on the Si and C sublattices in 6H-SiC has been performed by analyzing backscattering deuterium ions from the $^{28}Si(d,d)^{28}Si$ elastic scattering and protons from the $^{12}C(d,p)^{13}C$ nuclear reaction, respectively. Results of the accumulated damage on both Si and C sublattices induced at 100 and 300 K are shown in Fig. 4. Solid lines are sigmoidal fits to the data that are consistent with those in Fig. 2. From Fig. 4, the material can be fully amorphized under the He^+ irradiation at 100 K to a dose of ~0.5 dpa. At lower doses,

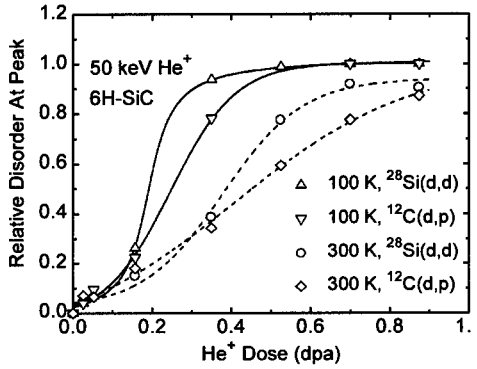

Fig. 4. Relative disorder on Si and C sublattices as a function of dose (dpa) at the damage peak for 50 keV He^+ implanted 6H-SiC at 100 or 300 K. Curves are sigmoidal fits to the data.

disorder on C sublattice appears to be higher than on Si sublattice, indicating a smaller carbon displacement energy. This result is consistent with those from MD simulations [9] and from experimental measurements [10]. At higher doses (above 0.15 dpa for 100 K irradiation and 0.3 dpa for 300 K irradiation), Si disorder becomes higher. This may be due to a higher rate of simultaneous recovery for defects on the C sublattice during irradiation. The results suggest that carbon defects have a lower activation energy for migration and recombination.

Summary

The lattice strain at the 3C-SiC/Si interface has been studied using He^+ channeling method. Radiation damage in 6H-SiC follows a sigmoidal dependence on dose for all ions and temperatures applied. Results show that the fraction of irradiation-induced defects surviving simultaneous recovery processes decreases with decreasing ion mass of the incident ion. Two recovery stages are found on the Si sublattice with activation energies of 0.25 ± 0.1 eV and 1.5 ± 0.3 eV in the temperature range 220 - 870 K. Simultaneous analysis of disorder on both Si and C sublattices in 6H-SiC has been performed using deuterium channeling and nuclear-reaction methods, and results suggest that defects on the C sublattice are slightly more mobile than on the Si sublattice.

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Materials Science Forum Vols. 338-342 (2000) pp. 961-964

Formation of Precipitates in 6H-SiC after Oxygen Implantation and Subsequent Annealing

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Keywords: Extended Defects, Oxygen Implantation, Oxygen Precipitates

Abstract: The structural characteristics of oxygen-implanted 6H-SiC, which was annealed at 1650° and 1900°C were studied by Transmission Electron Microscopy (TEM). Oxygen-related clusters are formed during the annealing The size of the clusters increases and their density decreases by increasing the annealing temperature. Tetrahedral precipitates with a mean size of 5nm are developed after annealing at 1900°C for two hours. The precipitates are apparently amorphous suggesting that SiO_2 is formed. Significant strain is developed around the precipitates, which imposes a displacement vector **R** along the c-axis. The large precipitates punch dislocation loops. The loops are always generated at the edges of the precipitates.

Introduction

Recently it has been shown that oxygen introduced in 6H-SiC by implantation forms two types of oxygen-related centers, shallow donors O_I and O_{II} in the range of (129-360)meV below the conduction band and deep acceptor-like defects near the midgap O_{III}, O_{IV}, O_V [1], similar behavior was observed in 4H-SiC [2] The oxygen-related centers are sensitive to heat treatments resembling the "Thermal Donors" observed in silicon see e.g. ref.[3].

In order to separate damage-induced defects from those related to the chemical bonding of oxygen, implantation of the noble gas neon was also performed with similar profiles as for oxygen. The electrical characterization of these specimens does not result in donor-like or acceptor-like defects [1,2]. The structural characteristics of the clusters and the corresponding defects, which were formed by oxygen implantation and subsequent annealing, were studied by TEM.

Experimental results

For this study n-doped 6H-SiC CREE wafers 3.5° off-axis along the $[11\bar{2}0]$ were used. The net doping concentration N_D - N_A was $1.2x10^{17}cm^{-3}$.One 6H-SiC specimen was oxygen-implanted with a dose of $5x10^{14}$ cm^{-2} and energy of 1200 keV at 300°C, in order to avoid amorphization. One part of the specimen was annealed at 1000°C/2h + 1650°C/2h and a second part at 1000°C/2h + 1900°C/2h.

The second specimen was oxygen-implanted at 100 keV with a dose of $5x10^{15}$ O^+cm^{-2} at 300°C. This implanted sample was annealed at 1000°C/2h + 1650°C/2h. Neon (Ne) was implanted, as a reference, under identical conditions, (100 keV and a dose of $5x10^{15}$ cm^{-2} at 300°C), which results in a similar profile as the oxygen implantation. Subsequently this sample was subjected to the same annealing like the corresponding O-implanted sample. In this way damage-induced defects can be separated from those related to the chemical bonding.

Results and Discussion

1 Low dose oxygen implantation ($5x10^{14}$ cm^{-2}) :

Cross-section TEM (XTEM) observations on this specimen subsequently annealed at 1000°C/2h + 1650°C/2h reveal the formation of small clusters as shown by arrows in the XTEM micrograph in Fig.1a. The mean size of these clusters is estimated to be 2.5nm. The density of the clusters at their maximum concentration is about $10^{16}cm^{-3}$. No other defects were observed in the implanted zone. Specimens annealed at 1000°C/2h + 1900°C/2h show significant coarsening of the clusters with a mean size of 5nm and a density of $10^{15}cm^{-3}$. They are distributed in a zone extended to about 0.5μm at a depth of 1.1μm. The clusters exhibit strong contrast when the operating reflection is parallel to the c-axis, $\mathbf{g}_{0006}$, as shown in Fig.1b. They are invisible for reflections perpendicular to the c-axis, like the reflection $\mathbf{g}_{11\bar{2}0}$, as shown in Fig.1c. The micrograph was taken from the same area confirming that the displacement vector **(R)** of the clusters is parallel to the c-axis. High resolution XTEM (HRXTEM) observations reveal that the largest clusters have triangular shape exhibiting well-defined facets, denoted by letter P in Fig.2a. It is evident that after the coarsening of the clusters we are dealing with precipitates. The smaller clusters have a rather spherical shape denoted by letter N in Fig.2a. One of the triangular precipitates is shown at high magnification in Fig.2b. The 0.25nm periodicity of the (0006) lattice planes is evident. The precipitate is bound by three symmetrical $\{10\bar{1}2\}$ planes, which in projection form an angle 58° with the (0006) lattice planes, as schematically shown in the inset in Fig.2b. This configuration suggests a slightly disturbed tetrahedral precipitate (due to the hexagonal structure) bound by the (0006) and the three symmetrical $\{10\bar{1}2\}$ planes. The $\{10\bar{1}2\}$ and the (0001) 6H-SiC are the lattice planes with the highest density, exhibiting the lowest surface energy. It is evident that the shape is not determined by the precipitate itself, but is the negative image of the 6H-SiC matrix. Significant strain was developed around the precipitates resulting in the bending of the (0006) lattice planes, no particular structure was observed inside the precipitate. The shape of the precipitates in conjunction with the absence of a particular structure confirms their amorphous structure.

Depending on the misfit between the matrix and the precipitate, strain is developed, in the matrix, which increases with the precipitate size. Above a critical size sufficient strain is developed for punching dislocation loops [4], in our case this size was about 8nm. The loops are always generated at the edges of the precipitates as shown in Fig.2a. When a dislocation loop is formed, all the strain is transferred to the loop. The precipitates and the related dislocation loops were also studied by plane view TEM (PVTEM) observations. Under multi beam observation with the electron beam parallel to the c-axis, a high density of circular loops was observed. Each loop is associated with a precipitate at the edge of the loop, as shown in Fig.2c, not all the precipitates punch dislocation loops. The contrast of the defects in Fig.2c is residual, because the reflections of the (0006) section (electron beam perpendicular to the foil) are all perpendicular to the displacement vector **R**, which is parallel to the c-axis and consequently should be invisible..

2 High dose oxygen. implantation ($5x10^{15}cm^{-2}$) annealed at 1000°C/2h + 1650°C/2h.

The defect zone is denoted by letter D in Fig.3a, the defects are small clusters with a density of $4x10^{16}cm^{-2}$ and a mean diameter of 4nm. No Stacking Faults (SFs) were observed in this case. The defect zone was also studied by PVTEM as shown in Fig.3b, small clusters are evident. The corresponding diffraction pattern with electron beam parallel to the c-axis is shown in Fig.3c. Very faint forbidden spots $(10\bar{1}0)$ are denoted by arrows. These are originated from higher order Laue zones due to elongation of the diffraction spots in the reciprocal space [5].

3 High dose Neon implantation ($5x10^{15}$ cm^{-2}) annealed at 1000°C/2h + 1650°C/2h.

The implanted and annealed specimen exhibits a high density of defects, mainly SFs. They are large with a mean diameter of 80nm, as shown in Fig.4a. Neon gas bubbles were preferentially

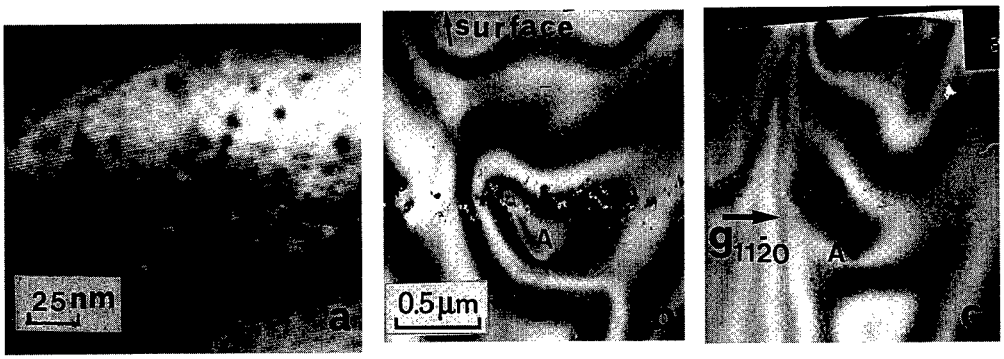

Fig.1 XTEM micrograph from the specimen implanted with oxygen at a dose of $5x10^{14}$ cm^{-2} a) Annealed at 1000°C/2h + 1650°C/2h, small clusters are evident. b) Annealed at 1000°C/2h + 1900°C/2h, operating reflection g_{0006}. c) The same area under operating reflection $g_{11\bar{2}0}$, the clusters are now invisible

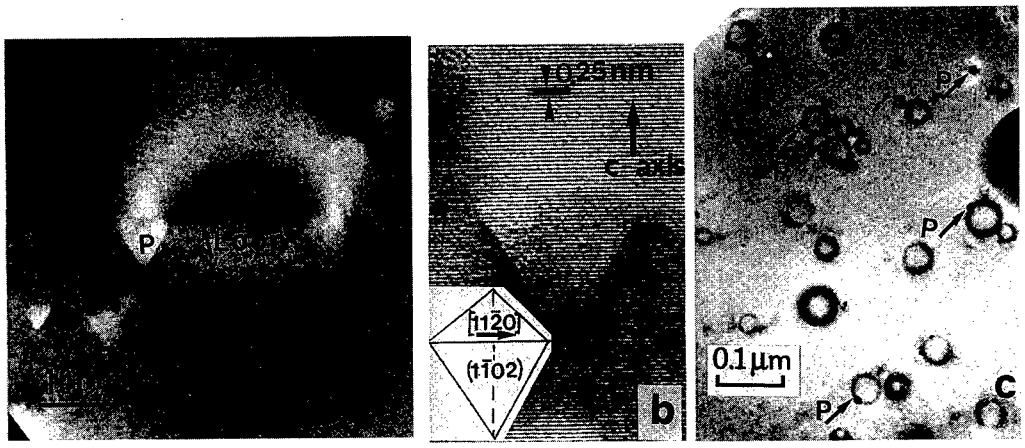

Fig.2 Specimen implanted with oxygen at a dose of $5x10^{14}$ cm^{-2}, subsequently annealed at 1000°C/2h + 1900°C/2h. a) Large clusters exhibiting well-defined facets. b) HRXTEM micrograph from a large cluster. c) PVTEM micrograph, loops associated with precipitates at the edges are evident.

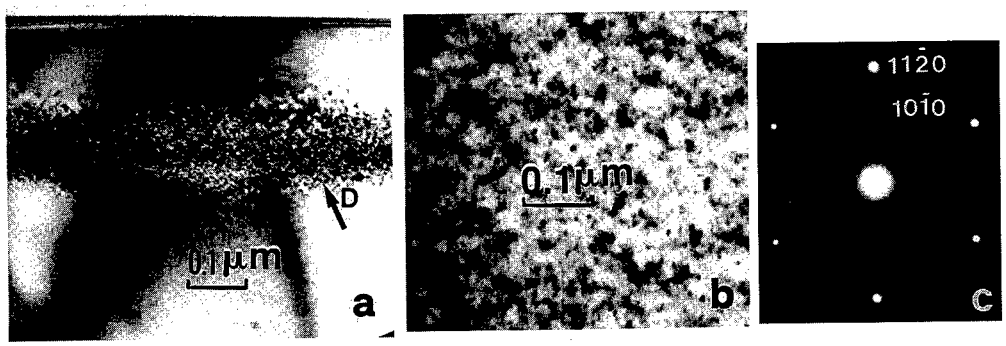

Fig.3 High dose oxygen implantation $5x10^{15}$ cm^{-2} a) XTEM micrograph from a specimen annealed at 1000°C/2h + 1650°C/2h. b) PVTEM micrograph from the same specimen only clusters are observed c) Corresponding diffraction pattern, very faint forbidden $(10\bar{1}0)$ spots are denoted by arrows.

agglomerated during the annealing process at the edges of the SFs. The g_{0006} reflection makes the SFs invisible, as shown in Fig.4b, revealing that they are of the Schockley type. No gas bubbles were observed in the oxygen-implanted specimens. The PVTEM observations from the defect zone reveal a high density of dislocation loops and bubbles. The corresponding diffraction pattern with electron beam parallel to the c-axis is shown in Fig.4c. The forbidden spots are even stronger than the normal diffraction spots of the 0001 section, revealing the high density of overlapping SFs on the basal planes.

Conclusions

It is evident that the implanted O^+ ions apart of the radiation damage, react also with the 6H-SiC resulting in the formation of precipitates. The exact nature of these precipitates is not known. The precipitates are apparently amorphous suggesting that SiO_2 is formed. Further studies are in progress for a better understanding of the oxygen precipitates in 6H-SiC.

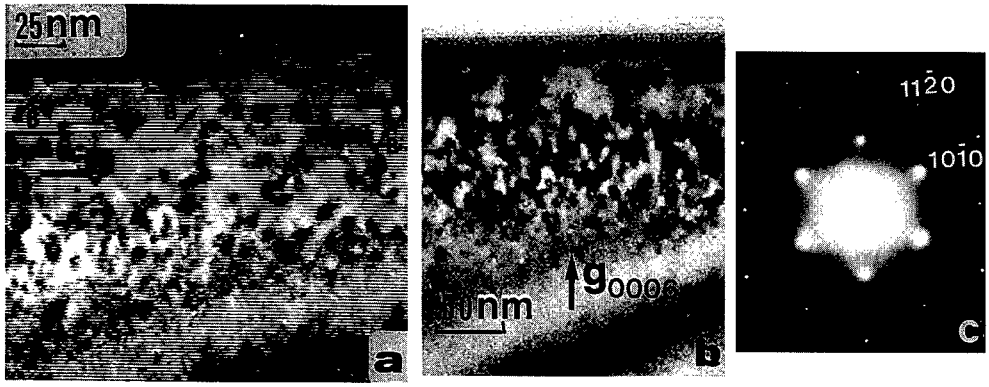

Fig.4 Specimen implanted with Ne with dose $5x10^{15}$ cm^{-2} and subsequently annealed at 1000°C/2h + 1650°C/2h . a) SFs and gas bubbles, which were preferentially agglomerated at the edges of the SFs, denoted by the letter B. b) The SFs are invisible for the g_{0006} reflection.

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Materials Science Forum Vols. 338-342 (2000) pp. 965-968

Microstructural Evolution of Radiation-Induced Defects in Semi-Insulating SiC During Isochronal Annealing

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Keywords: Defects, Irradiation, Positron Annihilation, Semi-Insulating

Abstract. Isochronal annealing and thermal evolution of electron- and proton induced defects in semi-insulating 4H-SiC have been investigated by positron annihilation experiments. Positron lifetime and Doppler broadening measurements were performed to investigate the thermal stability of the radiation induced defects as well as possible clustering mechanisms during the isochronal annealing.

The as-grown samples contain vacancy-type defects. These defects exhibit a positron lifetime of about 248 ps yielding a mean lifetime of 142 ps. The observed lifetimes suggest complexes with divacancy character. The concentration of these defects is in the range of 3×10^{16} cm^{-3}. For the bulk lifetime a value of 138 ps follows.

The mean lifetime shows an increasing dependence on the radiation dose. The grown-in defects are found stable even at 1600 °C. The annealing behaviour for the irradiated semi-insulating sample is quite different from that observed in n- or p-type SiC.

Introduction

Silicon carbide is, because of its unique thermal and electronic properties, a promising semiconductor material for specific applications [1-3]. The nature of many radiation-induced centres, however, has not yet been identified. It is important to apply not only conventional techniques, such as electron spin resonance (ESR) [4, 5], photo-luminescence spectroscopy (PL) [6-8] and deep-level transient spectroscopy (DLTS) [9], but also other methods that allow selective investigation of different types of structural defects. The positron annihilation method is a well-established method to study vacancy-like defects in semiconductors [10]. The data obtained by this method and their correlation with the results of other investigations have demonstrated a great promise of the positron annihilation technique in the diagnostics of structural defects in semiconductor materials.

Electron spin resonance studies on 3C-SiC and 6H-SiC suggest the formation of silicon (V_{Si}) and carbon (V_C) vacancies upon electron irradiation [5, 11] and V_C upon proton irradiation [12]. The silicon vacancy has a negative charge state [11], and it is suggested that after proton irradiation, V_C^0 exists in n-type material and V_C^+ in p-type material [12], while after electron irradiation, V_C^+ was found in n-type samples [13].

On the other hand, very recent positron annihilation experiments on electron-irradiated 6H-SiC show both carbon and silicon vacancies in n-type material, whereas no vacancies were detected in p-type material [14]. After proton irradiation, however, vacancies were detected also in p-type material [15]. To our knowledge there are no published positron studies on semi-insulating SiC.

Experimental Details

The samples used in this study are semi-insulating 4H-SiC single crystal wafers obtained from Cree Research Inc. Four sets of the samples were irradiated either with 2.5 MeV electrons at 77 K to fluences of $1x10^{18}$ cm^{-2} or $1x10^{19}$ cm^{-2}, or with 5 MeV protons at 220 K to fluences of $1x10^{15}$ cm^{-2} or $1x10^{16}$ cm^{-2}, respectively. The 20 min isochronal annealing was done in air from room temperature to 1000 °C and to the higher temperatures in an Ar atmosphere.
Positron lifetime spectroscopy was performed using a spectrometer with a time resolution (FWHM) of 150 ps. The lifetime spectra were numerically analysed using the computer program PFPOSFIT [16] taking into account a source correction due to the contribution of positrons annihilating in the Al foil that supported the positron source. The Doppler-broadening of the 511 keV annihilation line was measured using an intrinsic Ge detector with a resolution (FWHM) of 1.18 keV at 497 keV. The numerical analysis of the spectra was performed by determining the shape parameter S (the ratio between the counts in a central part of the spectrum and the total counts). Both lifetime and Doppler-broadening measurements were performed at room temperature.

Results and Discussion

The results of a two term analysis for the as-grown sample and four electron- or proton irradiated samples are shown in Table 1. From the measured spectra one can calculate the mean lifetime according to $\tau_{mean} = (I_1\tau_1+I_2\tau_2)$, where τ_1 and τ_2 are the fitted lifetimes and I_1 and I_2 are their corresponding intensities. The bulk lifetime τ_b of positrons was calculated from the fit parameters according to the conventional trapping model [17], $\tau_b = (I_1/\tau_1+I_2/\tau_2)^{-1}$, which is of particular importance since it refers to the annihilations from the "perfect" crystalline regions of the sample and hence is a material constant.

Table 1: Lifetime and Doppler-broadening results for the samples investigated: Both the as-grown and the low-temperature irradiated samples were measured at room temperature.

Sample	Treatment	τ_1 [ps] ± 2	τ_2 [ps] ± 15	I_1 [%] ± 1.5	I_2 [%] ± 1.5	τ_{bulk} [ps] ± 2	τ_{mean} [ps] ± 2	S/S_{bulk}
	as-grown	132	248	91.4	8.6	138	142	1
5-9	10^{15} p/cm^2	128	238	49.1	50.9	-	184	1.032
6-7	10^{16} p/cm^2	131	235	38.2	61.8	-	195	1.036
14-15	10^{18} e/cm^2	130	240	67.4	32.6	-	166	1.018
2-3	10^{19} e/cm^2	143	236	31.0	69.0	-	207	1.045

For the as-grown sample the lifetime spectrum is dominated by one lifetime component, τ_1, with an intensity of more than 90 %. This component arises from annihilations in the bulk, whereas the other component associated with the longer τ_2 is due to vacancy clusters. The calculated bulk lifetime of 138 ps is in good agreement with other experimental and theoretical results [14,18-20]. From the two-state trapping model the concentration of these vacancy clusters can be calculated to be in the order of $3x10^{16}$ cm^{-3}. These grown-in defects are stable during annealing up to temperatures of at least 1600 °C.
The changes of the lifetime parameters and the normalized Doppler S parameters after irradiation

with electrons and protons are also shown in Table 1. For all samples we observe a distinct second lifetime component of about 235-240 ps whose intensity increases with the increasing irradiation dose. Both the longer mean and bulk lifetime indicate that we observe complete positron trapping at defects in the crystal.

It is expected that irradiation with electrons or protons induces vacancies, divacancies and vacancy agglomerates. The longer lifetime corresponds to a mixture of the silicon vacancies, divacancies and larger vacancy complexes. Theoretical calculations have indicated a lifetime of 153 ps for the carbon vacancy, 192-194 ps for the silicon vacancy, and 214 ps for the carbon–silicon divacancy [20].

In Fig. 1 the changes of the mean lifetime and the normalized S parameter as a function of annealing temperature for the four samples are shown. For all samples a small annealing stage at about 150 to 200 °C is observable. At this stage the carbon and silicon vacancies can recombine, as was also found in ESR measurements [11]. At the lower radiation doses, there seems to be a plateau in the range from 600 to 900 °C, and after annealing at 1200 °C, both the lifetime and the Doppler parameters have recovered to the values for the as grown 4H-SiC.

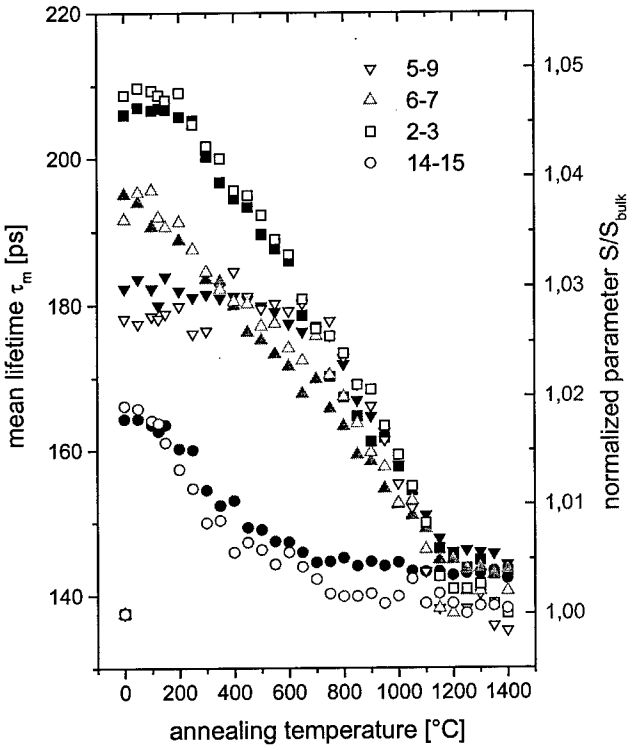

Fig 1: Mean lifetime (solid symbols) and normalized parameter S/S_{bulk} (open symbols) as a function of annealing temperature: ∇ (10^{15} p/cm^2), Δ (10^{16} p/cm^2), O (10^{18} e/cm^2), □ (10^{19} e/cm^2). The values before irradiation are also shown.

The fact that we obtain the same lifetime and S-parameter values after annealing as before irradiation excludes the possibility that a fluence of 10^{16} p/cm^2 or 10^{19} e/cm^2 could lead to amorphization of the sample, since the lifetime as well as the S-parameter values in amorphous regions are quite different from those in the crystalline regions [21].

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Materials Science Forum Vols. 338-342 (2000) pp. 969-972

Vacancy-Type Defects in Proton-Irradiated 6H- and 4H-SiC: A Systematic Study with Positron Annihilation Techniques

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Keywords: Defects, Positron Annihilation, Proton Irradiation

Abstract. Annealing of defects in proton irradiated bulk 6H- and 4H-SiC has been investigated by positron lifetime spectroscopy and Doppler-broadening measurements. The experiments were performed on N-doped (n-type) or Al-doped (p-type) crystals with carrier concentrations $N_D - N_A = 2.0\times10^{17} - 3.2\times10^{18}$ cm^{-3} and $N_A - N_D = 3.8\times10^{18} - 6.2\times10^{18}$ cm^{-3}, respectively, and in semi-insulating samples.
In n-type material the radiation induced defects anneal out in four annealing stages: 150 °C, 350 °C, 750 °C and higher than 1000 °C. The magnitude of the respective annealing stages depends on the proton fluence. In p-type material the increase of the positron parameters after proton irradiation is smaller and a different annealing behaviour is observed after the first annealing stage at about 150 °C. The semi-insulating samples do not show the annealing stage at 1000 °C.

Introduction

Silicon carbide is, because of its unique thermal and electronic properties, a promising semiconductor material for specific applications. A few studies concerning defects have been performed, using photoluminescence (PL) [1-3], electron spin resonance (ESR) [4, 5] and deep-level transient spectroscopy (DLTS) [6]. Several positron investigations of radiation-induced defects have also been carried out in recent years [7-14]. A detailed discussion can be found in [13]. Nevertheless, a systematic study of the behaviour of the radiation-induced defects as a function of doping and radiation fluence is lacking, especially after proton irradiation.

Experimental Details

The samples consisted of ten sets of research grade SiC single crystalline wafers obtained from Cree Research Inc. The doping type, carrier concentrations and irradiation doses are given in Table 1. The temperature of the specimens was kept below 220 K during irradiation. The 20 min isochronal annealing was done in air from room temperature to 1000 °C and in an Ar atmosphere to the highest temperatures.
The positron lifetime and Doppler-broadening measurements were performed at room temperature. Details of the experimental set-up and the analysis procedure as well as the physical background can be found in [13].
From the measured positron lifetime spectra one can calculate the mean lifetime according to $\tau_{mean} = (I_1\tau_1+I_2\tau_2)$, where τ_1 and τ_2 are the fitted lifetimes stemming from annihilations in the bulk (τ_1) and the defect (τ_2) and I_1 and I_2 are their corresponding intensities. From the conventional trapping

model [15], the bulk lifetime $\tau_b = (I_1/\tau_1+I_2/\tau_2)^{-1}$ can be obtained, which is of particular importance since it refers to the annihilations from the "perfect" crystalline regions of the sample and hence is a material constant. Of even greater practical importance is that from this model, the concentration of the defect can be calculated.

Results and Discussion

In Table 1, the results of a two-term analysis of the as-grown samples and after proton irradiation are shown.

Table 1: Lifetime and Doppler-broadening results for the samples investigated: The values shown are for as-grown samples and "as-received" after irradiation.

Sample	Treatment	Doping type and Carrier Concentration [cm^{-3}]	τ_1 [ps] ± 2	τ_2 [ps] ± 15	I_1 [%] ± 1.5	I_2 [%] ± 1.5	τ_{bulk} [ps] ± 2	τ_{mean} [ps] ± 2	S/S_{bulk}
E356	as-grown	n 3.2×10^{18}	136	290	90.2	9.8	143	151	1
	10^{15} p/cm^2		153	247	54.2	45.8	-	196	1.039
S052	as-grown	n 1.8×10^{18}	132	250	72.2	27.8	152	165	1
S052-1	10^{14} p/cm^2		136	239	51.8	48.2	-	186	1.017
S052-2	10^{15} p/cm^2		135	237	53.3	46.7	-	183	1.017
G430	as-grown	n 2.0×10^{17}	136	258	84.8	15.2	147	155	1
G430-1	10^{14} p/cm^2		138	239	58.4	41.6	-	180	1.020
G430-2	10^{15} p/cm^2		142	247	64.5	35.5	-	179	1.020
G430-3	10^{16} p/cm^2		144	242	33.5	66.5	-	209	1.047
E103	as-grown	p 6.2×10^{18}	139	289	95.0	5.0	143	147	1
	10^{16} p/cm^2		137	253	69.0	31.0	-	173	1.027
G346	as grown	p 3.8×10^{18}	137	290	94.4	5.6	141	146	1
	10^{17} p/cm^2		142	240	33.9	66.1	140	207	1.043
F661	as-grown	semi-insulating	132	248	91.4	8.6	138	142	1
F661-1	10^{15} p/cm^2		128	238	49.1	50.9	-	184	1.032
F661-2	10^{16} p/cm^2		131	235	38.2	61.8	-	195	1.036

The lifetime spectra for the as-grown samples are dominated by one lifetime component with an intensity in the 90 % range, stemming from annihilations in the bulk, whereas the longer component is due to vacancy clusters. These defects are formed independent of the growth conditions and are stable during annealing up to temperatures of at least 1600 °C [12].
The calculated bulk lifetimes have values in the range from 138 to 147 ps in good agreement with other experimental and theoretical results [10,14,16]. From the two-state trapping model, a concentration of the vacancy clusters in the range from 2 to 4×10^{16} cm^{-3} can be obtained.
The semi-insulating sample shows the shortest mean lifetime (142 ps), while the n-type samples show the longest (156 ps). The values of the mean lifetime for the p-type samples are about 146 ps.

For sample S052, two defect components can be found, one with a lifetime of 159 ps and the other with 296 ps. The calculation yielded a very high defect concentration, about 4×10^{17} cm^{-3} for the defect with the 159 ps lifetime and about 1×10^{17} cm^{-3} for the 296 ps state [12].

After irradiation we observe for all samples a second lifetime component of about 235-250 ps with increasing intensity, showing that the created defects overwhelm the weak response from the grown-in vacancy clusters. The higher values of the mean lifetime and the calculated bulk lifetime indicate that we observe complete positron trapping in crystal defects. For the Doppler S parameter we also observe an increase after irradiation, with nearly no difference after the lower radiation fluences.

It is to be expected that irradiation with protons induces vacancies, divacancies, and vacancy agglomerates. The longer lifetime originates, therefore, from a mixture of annihilations in the silicon vacancies, divacancies, and even larger vacancy complexes.

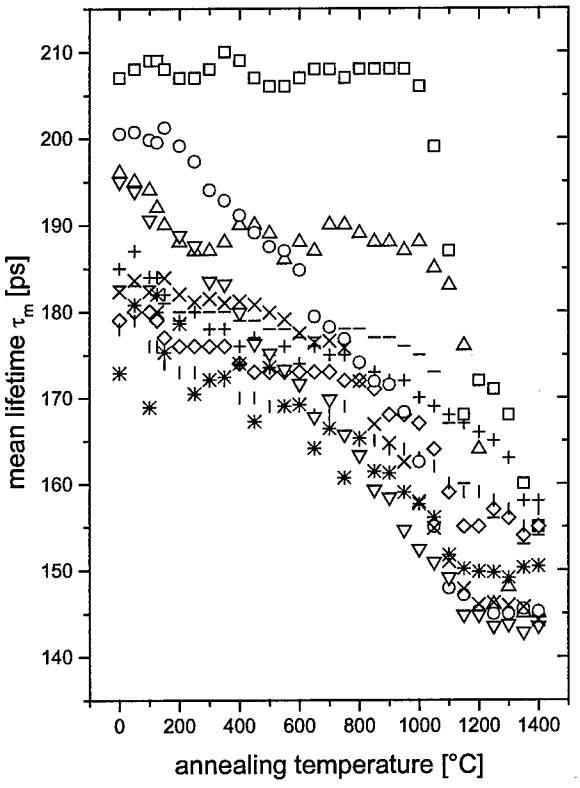

Fig 1: Mean lifetime as a function of annealing temperature: Δ (E356, 10^{15} p/cm^2), + (S052-1, 10^{14} p/cm^2), – (S052-2, 10^{15} p/cm^2), ◊ (G430-1, 10^{14} p/cm^2), | (G430-2, 10^{15} p/cm^2), □ (G430-3, 10^{16} p/cm^2), * (E103, 10^{16} p/cm^2), ○ (G346, 10^{17} p/cm^2), × (F661-1, 10^{15} p/cm^2), ∇ (F661-2, 10^{16} p/cm^2).

Theoretical calculations yield a lifetime of 153 ps for the carbon vacancy, 192-194 ps for the silicon vacancy, and 214 ps for the carbon–silicon divacancy [16].

In Fig. 1 the changes of the mean lifetime as a function of annealing temperature are shown for the different samples.

For the n-type samples there seem to be no differences in the annihilation parameters after proton doses in the range from 10^{14} to 10^{15} cm^{-2}, although there are differences in the annealing behaviour. The irradiation induced defects anneal out in four annealing stages: 150 °C (recombination of vacancies and interstitials), 350 °C (vacancies become mobile), 750 °C, and higher than 1000 °C (vacancy complexes and divacancies anneal out). The magnitude of the respective annealing stages depends on the proton fluence.

For the p-type samples we do not observe any change in the annihilation parameters after irradiation to a fluence of 10^{15} p/cm^2 and only a very small increase in the mean lifetime after a fluence of 10^{16} p/cm^2 (sample G346). For these samples the annealing stages are much less pronounced. It is worth noting that after electron irradiation in p-type material no vacancies were detected [10, 17].

For the semi-insulating sample a similar annealing behaviour as for the p-type sample is observed. The most conspicuous result is the lack of the annealing stage at about 1000 °C.
In summary, we can state that we observe a different annealing behaviour of SiC samples after proton irradiation for differently doped samples. A common feature of all samples is that after annealing at 1400 °C all radiation induced defects have annealed out. Moreover, from Fig. 1 there is evidence that the annealing behaviour depends in a significant manner also on the applied proton doses. Further studies are in progress to quantify this effect.

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Materials Science Forum Vols. 338-342 (2000) pp. 973-976

Deep Centres Appearing in 6H and 4H SiC after Proton Irradiation

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Keywords: Compensation, Deep Centers, DLTS, Irradiation, Protons

Abstract. In the present work the effect of irradiation with 8-MeV protons at doses (D) in the range $1\cdot10^{14}$ - $1\cdot10^{16}$ cm^{-2} on p-n structures and Schottky diodes based on epitaxial 6H and 4H SiC layers was studied. Commercial (CREE) samples and samples fabricated by sublimation epitaxy (SE) in our laboratory were used. Parameters and concentrations of deep centres (DC) were determined by transient capacitance and current spectroscopy. It was shown that proton irradiation may lead to an increase in the initial doping level of 6H-SiC samples. The obtained results are analysed and the properties of radiation-induced defects are discussed.

Introduction. Proton irradiation is commonly used to passivate the periphery of p-n semiconductor structures [1]. Previously, proton irradiation [2] or hydrogen ion implantation [3, 4] have been used to obtain SiC layers semi-insulating at room temperature, however, parameters and concentrations of deep centres formed upon irradiation have not been studied. In other works, parameters of such centres have been investigated [5, 6], but compensation appearing as a result of irradiation was not considered. The aim of the present work was to obtain high-resistivity layers by proton irradiation and to determine parameters of centres responsible for compensation.

Samples. Commercial (CREE) epilayers produced by CVD and layers grown by sublimation epitaxy in our laboratory (SE) [7] were used in the experiments. Net donor concentration (Nd-Na) in the CREE and SE layers before irradiation was $5.5\cdot10^{15}$-$4.5\cdot10^{16}$ cm^{-3} and $(1.1\text{-}7.2)\cdot10^{16}$ cm^{-3} respectively. Schottky diodes were fabricated on the layers by magnetron sputtering of Ni. We also investigated several CREE p-n junctions and p-n junctions produced by sublimation on CREE and Lely method grown substrates. The samples were irradiated at cyclotron MGC-20 with 8-MeV protons. Irradiation with this energy produces defects with uniform distribution in the investigated depth range (<5 μm). Dose of the irradiation was $1\cdot10^{14}$ - $1\cdot10^{16}$ cm^{-2}. In the dose range $1\cdot10^{14}$-$1\cdot10^{15}$ cm^{-2} all samples were successively irradiated with step of $1\cdot10^{14}$ cm^{-2}. The samples were annealed after each irradiation dose for 10 min at 650K for Schottky diodes and at 800K for p-n structures.

Results. In addition to relatively shallow DC (0.2-0.5 eV) whose concentration can be changed by annealing of the samples at 650-800 K, a set of more thermally stable centres were observed in each of the polytypes. In 4H SiC this is the Z1, $RD_{1/2}$, RD_3, RD_4 centres, and in 6H SiC, centres close in parameters to the E_1E_2, Z_1/Z_2, R centres [5, 8] (see the table). The concentrations of these centres increased linearly with the total irradiation dose. Concentrations of DC found in the samples irradiated with dose of $2\cdot10^{14}$ cm^{-2} before annealing are presented in the table. All radiation defects were annealed out completely at temperatures ≥1500 K.

Table. Parameters and concentration of deep centres observed in 6H and 4H SiC after proton irradiation with dose of $2 \cdot 10^{14}$ cm^{-2}

Parameters	6H						4H				
of DC	E_c-0.18	E_1/E_2[5]	RD_5 [5]	Z_1/Z_2[5]	E_c-0.8	R [5,8]	E_c-0.18	Z_1 [5]	RD_1 [5]	RD_3 [5]	RD_4 [5]
E_c-E_0,eV	0.16-0.2	0.36/0.4	0.5	0.7	0.8	1.1-1.22	0.18	0.66-0.7	0.96	1.0	1.5
σ_n, cm^2	$6 \cdot 10^{-17}$	$2 \cdot 10^{-15}$	$5 \cdot 10^{-15}$	$4 \cdot 10^{-15}$	$4 \cdot 10^{-15}$	$2 \cdot 10^{-15}$	$6 \cdot 10^{-15}$	$5 \cdot 10^{-15}$	$5 \cdot 10^{-15}$	$1 \cdot 10^{-16}$	$2 \cdot 10^{-13}$
N, cm^{-3}	$3 \cdot 10^{14}$	$3.3 \cdot 10^{15}$	$2.2 \cdot 10^{15}$	$1.3 \cdot 10^{15}$	$6 \cdot 10^{14}$	$1 \cdot 10^{16}$	$2 \cdot 10^{14}$	$5 \cdot 10^{15}$	$2.5 \cdot 10^{15}$	$2.5 \cdot 10^{15}$	$1.5 \cdot 10^{15}$
T_{ann}, K	< 650	>800	< 650	>800	>800	>800	< 650	>650	>650	>650	>650

C-V characteristics of irradiated samples plotted on C^{-2} – U axes were linear except for several lightly doped CREE samples (Fig.1). Current-voltage characteristics (CVChs) of these structures did not differ significantly from the CVChs of unirradiated structures. The Nd-Na concentration found from the C-V characteristics taken at high temperatures after irradiation exceeded that measured at room temperature (Fig. 2, 3). It was found that the carrier removal rates ($\partial(Nd\text{-}Na)/\partial D$) differ in 4H SiC and 6H SiC by more than an order of magnitude: 10 cm^{-1} for 6H and 250 cm^{-1} for 4H.

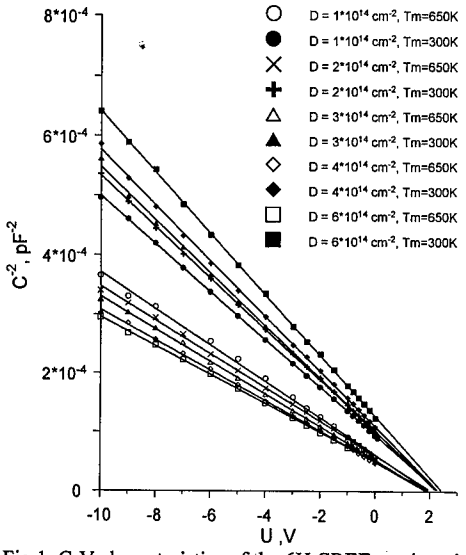

Fig.1. C-V characteristics of the 6H CREE p-n junction irradiated with different doses, measured at 650 K and at room temperature

At the same time forward resistance of some lightly doped CREE Schottky diodes strongly increased after irradiation with dose of $2 \cdot 10^{14}$ cm^{-2}. With increasing temperature, the resistance of these samples falls off exponentially (Figs. 4 and 5). Increasing of the irradiation dose makes higher the resistance activation energy (Ea_R), found from slopes of the straight lines, i.e. the conduction of the layers is determined by successively deeper levels. Irradiation doses of ~$1 \cdot 10^{16}$ cm^{-2} caused degradation of the current-voltage characteristics of all structures under study at room temperature (the forward and reverse CVChs were indistinguishable) [9], and this degradation could not be eliminated by annealing of the samples at temperatures of up to 800 K. At the same time, the CVChs taken on the same p-n structures at 770 K did not differ significantly from the CVChs of unirradiated ones. Schottky diodes irradiated with D = $1 \cdot 10^{16}$ cm^{-2} showed ohmic CVChs at increased temperature. No noticeable difference in radiation hardness and parameters of centres formed was observed between samples prepared by CVD and SE. Most of the centres revealed in the present work have already been known in the literature as radiation-induced or intrinsic defects [10].

Discussion. Measurements of Nd-Na at T~650 K demonstrated that this concentration either increases (6H SiC) or somewhat decreases (4H SiC) upon irradiation. Thus, deep donor levels are formed under our irradiation conditions in addition to acceptor centers, with high concentration of centres still filled with electrons at room temperature appearing in the upper half of the forbidden

gap. In all probability, the acceptor centres lie deeper in the gap (formation of acceptor levels in the lower half of the forbidden gap, i.e., D centres [11], is also possible). As a result, electrons fall down from conduction band or shallow donors to free levels lying deeper in forbidden gap. This lead that the Fermi level at room temperature goes down and the activation energy of resistance E_{aR} increases (Fig. 6). In 6H-SiC, the highest E_{aR} is associated with the R centre characterised by the highest ionisation energy, whose concentration grows most rapidly under irradiation (Fig. 4).

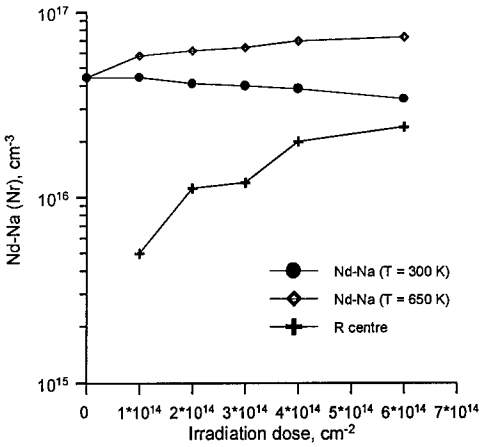

Fig.2. Nd-Na value measured at different temperatures and R centre concentration in the 6H SiC layer vs. the dose of the irradiation

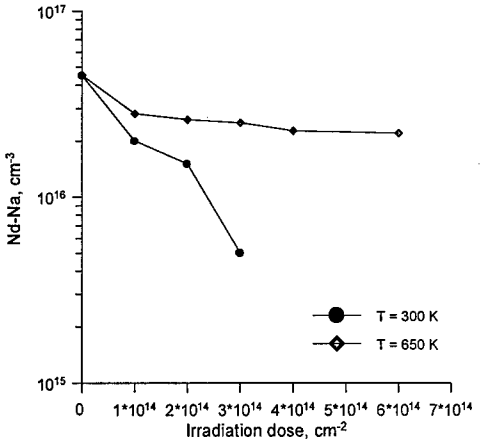

Fig.3. Nd-Na value in 4H SiC layer measured at different temperatures vs. the dose of irradiation

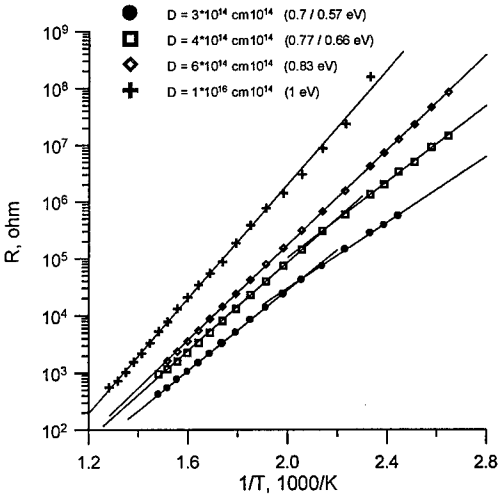

Fig.4. Temperature dependence of the forward resistance of the Schottky diode based on 6H SiC layer irradiated with different doses

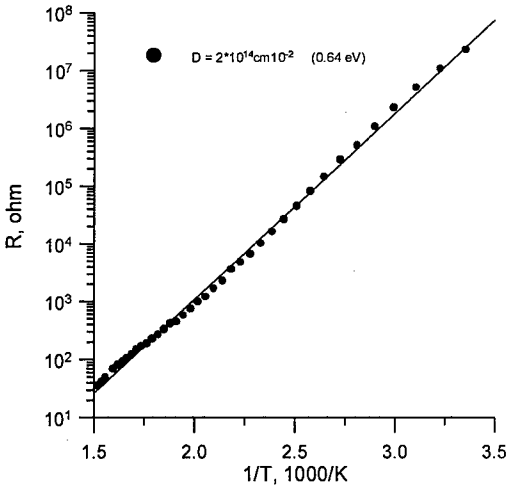

Fig.5. Temperature dependence of the forward resistance of the Schottky diode based on 4H SiC layer irradiated with dose of $2 \cdot 10^{14}$ cm^{-2}

In 4H-SiC, we could obtain E_{aR} = 0.64 eV, which is presumably due to the coincidence of the position of the Fermi level at room temperature and that of the Z1 centre. The presence of deep radiation-induced defects in the given polytype (see the table) allows further increase in E_{aR} with increasing total irradiation dose.

Summary. The results obtained in this work allowed making a somewhat unexpected conclusion: irradiation with 8-MeV protons can increase the 6H SiC doping level. That is, the concentration of donors introduced into this material by irradiation was found to be higher than that of introduced acceptors. The observed growth of the room temperature resistance of the semiconductor can be explained primarily by, so to speak, "depression" of the energy position of the level determining the conductivity of the material, rather than by compensation. Combination of the growing resistance at room temperature and increasing doping level can be considered a specific feature of 6H SiC. From the practical standpoint, semi-insulating SiC layers obtained by irradiation under our experimental conditions are promising for fabrication of devices that are not intended for operation at high temperature, e.g., in radiation detectors or devices with Schottky diodes. The suitability of semi-insulating SiC layers for high temperature electronics is debatable as yet. At the same time, the compensation observed by us in 4H SiC samples (as also the possibility of making higher the activation energy) gives reason to hope that layers of the given polytype, semi-insulating at higher temperatures, could be obtained by selecting the energy and type of charged particles.

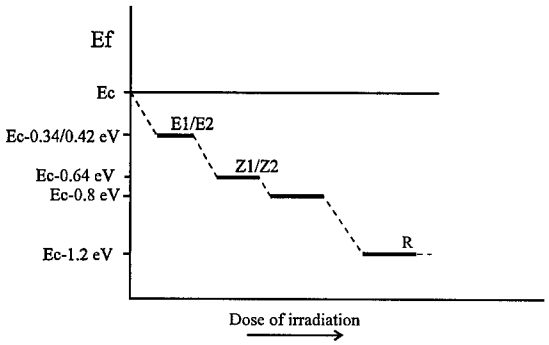

Fig.6. Diagram illustrating dependence of the Fermi level position in the band gap of 6H SiC on the irradiation dose

Acknowledgement.

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Materials Science Forum Vols. 338-342 (2000) pp. 977-980

Radiation-induced Conductivity and Simultaneous Photoconductivity Suppression in 6H-SiC under 17 MeV Proton Irradiation

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Keywords: Carrier Removal, Ion Irradiation, Photoconductivity, Radiation Effects, Radiation-Induced Conductivity

Abstract. Radiation-induced conductivity (RIC) of nitrogen-doped and undoped 6H-SiC has been studied under 17 MeV proton irradiation. The proton irradiation generates defects in the samples, and dark-conductivity (σ_d) decreases because of the carrier removal (CR) due to the defects. A decrease of the σ_d is visible in the undoped sample. Contrary an almost constant σ_d against the irradiation is obtained in the doped sample. The RIC increases in proportion to the proton flux in the doped sample, but a sublinear flux dependence is observed in the undoped sample. Both the differences of the σ_d decrease and of the flux dependence between the doped and the undoped samples are ascribed to a large difference of carrier concentration due to doping. Photoconductivity suppression (PCS) under simultaneous photon/proton irradiation of the undoped 6H-SiC is presented as a characteristic phenomenon under high flux proton irradiation.

Introduction

There has been a great demand for electronic devices usable under strong radiation fields, e.g., in nuclear fusion reactors [1], space satellites [2], etc, which will be more important in the next century. Up to now, we have investigated radiation-resistance of Si-based materials for electronic devices or photo-detectors, and have observed several characteristic phenomena under high fluence/flux irradiation, e.g., the carrier removal (CR) [3], radiation-induced conductivity (RIC) [4] and photoconductivity suppression (PCS) under simultaneous photon/ion irradiation [5]. A high radiation-resistance of SiC has been well established for several decades [6]. However, the characteristic phenomena under high fluence/flux irradiation, e.g., RIC and PCS, have not yet been clarified in 6H-SiC. For applications of SiC devices to the strong radiation fields, understandings of these phenomena are requisite. Although there are some reports on RIC of sintered SiC or fiber-reinforced composites as a structural material for fusion reactors [7], there are few reports on RIC of SiC crystals for semiconductor devices. In this paper, some characteristic phenomena in 6H-SiC under high fluence/flux irradiation, i.e., CR, RIC and PCS, are reported.

Experimental

Samples were fabricated from 6H-SiC wafers of two different types: nitrogen-doped and undoped ones. Both the types of wafers were grown by Nippon Steel Co. [8] using a bulk sublimation method with seed wafers of 6H-SiC {0001}. The undoped samples contain residual nitrogen (N) and boron (B) impurities with concentrations of more than 1×10^{17} cm^{-3} [8], and show *p*-type conduction with carrier concentration of 1.6×10^{14} cm^{-3}. Temperature dependence of dark-conductivity (σ_d) gives a deep activation energy of ~0.3 eV. These results are consistent with the fact that the B impurities are

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dominant acceptors. In the doped wafers, nitrogen gas was fed during the growth, in addition to purified Ar-gas. The doped samples show *n*-type conduction with carrier concentration of 1.5×10^{18} cm^{-3}. Temperature dependence of the σ_d is week, and consistent with the fact that the N impurities are dominant donors. Ohmic electrodes were made by vacuum evaporation of Al and heat treatment in Ar-gas at 1173 K for 30 min.

A 17 MeV proton beam from NRIM cyclotron was used for irradiation. Since the proton range is much larger than the sample thickness 0.4 mm, an irradiated sample is free from hydrogen implantation. The sample was attached to a temperature-stabilized holder in an irradiation chamber, and the sample temperature was kept at 300 K ± 1 K, even under the proton irradiation. For the photoconductivity (PC) measurements, a halogen lamp with a single monochromator (Fig.2) or a Xe-lamp without a monochromator (Fig.4) was used for an excitation source.

Results and Discussion

Conductivity (σ) changes of N-doped and undoped samples, induced by 17 MeV proton irradiation, are shown in Fig.1-(a) and (b), respectively. In the doped sample, the σ increases under the proton irradiation, and decays to the initial value after stopping the irradiation. With increasing the proton flux, an increment of σ becomes larger. In the undoped sample, the σ increases at the beginning of the irradiation, and turns to a gradual decrease. After stopping the irradiation, the σ decays to a much smaller value than before the irradiation. The gradual decrease of σ under irradiation is mainly due to a decrease of dark-conductivity (σ_d), i.e., a base-part of σ. Similar behaviors are observed in crystalline Si [4]. In Si, the increase and the decrease of σ are ascribed, respectively, to the electronic excitation under the proton irradiation, and to the carrier removal due to radiation-induced defects.

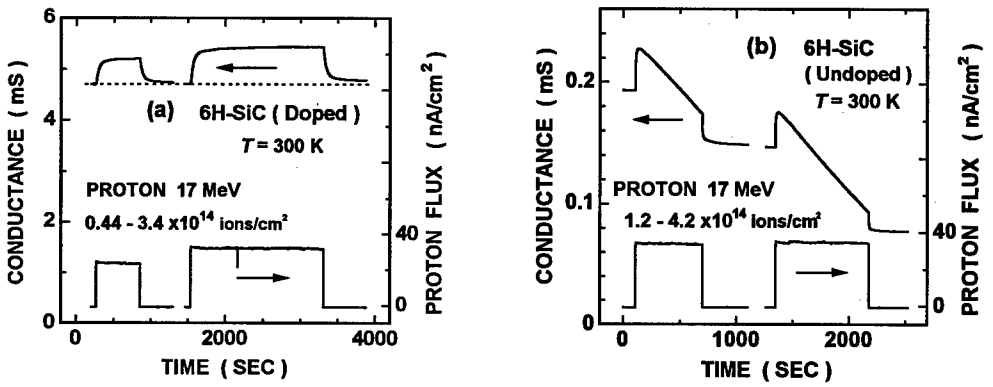

Fig.1 Conductance changes of (a) N-doped and of (b) undoped samples induced by 17 MeV proton irradiation at $T = 300$ K.

Difference of the free carrier density is responsible for the different fluence dependence of σ_d between the doped and the undoped samples. Since phonons are more dominant carrier-scatterers than the radiation-induced defects in this fluence region at $T = 300$ K, the carrier mobility (μ) does not depend on the defect density, i.e., the fluence, in Si [2] and in 6H-SiC. The decrease of σ_d is mainly due to decrease of the carrier density n, i.e., the carrier removal (CR). When deep carrier traps are introduced, free carrier density $n(\phi)$ at fluence ϕ is roughly given as,

$$n(\phi) = n(0) - n_T, \qquad (1)$$

where $n(0)$ and n_T denote free carrier density at $\phi = 0$ and the trap density, respectively. Since the n_T is 10^{15} cm^{-3} at maximum in our experiments, and since $n(0)$ is 1.5×10^{18} cm^{-3} in the doped sample, the carrier density $n(\phi) = n(0) - n_T$ is regarded as a constant $\sim n(0)$ independent of the ϕ. The decrease in $n(\phi)$ becomes pronounced, because $n(0) = 1.6\times10^{14}$ cm^{-3}, comparable to the n_T, in the undoped sample.

Fluence dependences of σ_d, RIC ($\Delta\sigma_B$) and PC ($\Delta\sigma_L$) at $\lambda = 350$ nm are shown in Fig.2. It is noted that σ_d shows the almost linear dependence as in Eq.(1), but the linear dependence is shown as a bent curve in the log-log plot. Although σ_d and $\Delta\sigma_B$ decrease in the undoped sample as exceeding fluence of 10^{14} cm^{-2}, they are almost constant, at least, up to 10^{16} cm^{-2} in the doped sample. Higher stability against the radiation is obtained with the carrier-doping, as also observed in Si [1].

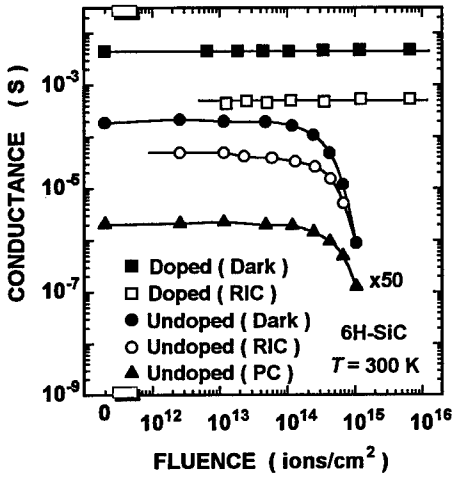

Fig.2 Fluence dependences of radiation-induced conductance, dark-conductance and photoconductance of N-doped and undoped 6H-SiC under 17 MeV proton irradiation.

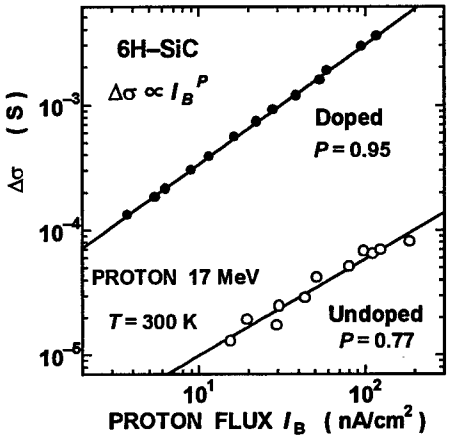

Fig.3 Proton flux dependences of radiation-induced conductance ($\Delta\sigma$) in N-doped and undoped 6H-SiC under 17 MeV proton irradiation.

Proton flux dependence of RIC in the doped and undoped samples is shown in Fig.3. The measurements were quickly carried out so that influences of defect accumulation were negligible. Although the conductance increment ($\Delta\sigma$) is proportional to the flux ($p \sim 1$) in the doped sample, the $\Delta\sigma$ increases sublinearly with the flux ($p = 0.77$) in the undoped sample. Under low flux excitation, minority carriers Δp recombine mainly with the dark-carriers n_o. The largest recombination term in the rate-equations is $n_o\Delta p$, and is in linear to Δp. Under high flux excitation, the minority carriers Δp recombine mainly with the excited carriers Δn. The largest recombination term $\Delta n\Delta p$ is almost quadratic in Δp. A criterion between linear and sub-linear flux dependence is given as follows [9]: When the carrier generation rate G, which is proportional to the proton flux, is smaller (larger) than a constant G_o, a linear (sublinear) dependence occurs, where

$$G_o = (C/4)(n_o + p_o)^2, \qquad (2)$$

and C, n_o and p_o denote the effective recombination coefficient, electron and hole concentration without excitation, respectively. The constant G_o depends on dark-carrier concentration of sample.

The doped sample has much larger G_o than the undoped sample. Under an excitation rate G which satisfies a condition $G_o^{undope} < G < G_o^{dope}$, only the undoped sample shows a sublinear dependence even in the same proton flux region. The condition easily holds because $G_o^{undope} << G_o^{dope}$, i.e., $n_o^{undope} << n_o^{dope}$.

Another phenomenon of concern is the PCS under simultaneous irradiation of 17 MeV protons and near-UV photons. The PCS was recently observed in Si [5], and is considered as a problem for the photo-detection under strong radiation fields. The PC of undoped 6H-SiC is measured using a phase-sensitive detection method. With the simultaneous proton irradiation, the PC is reduced as shown in Fig.4. The suppression becomes stronger, as the proton flux increases. The PCS in 6H-SiC is probably ascribed to the same mechanism in Si [5], i.e., the sublinear dependence of conductance increment $\Delta\sigma(G)$ against the excitation flux G, as shown in Fig.3.

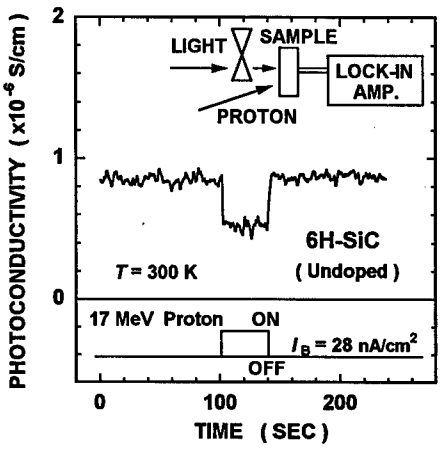

Fig.4 Photoconductivity suppression under simultaneous irradiations of near-UV photons and 17 MeV protons in 6H-SiC, detected by a phase-sensitive method.

Summary

Characteristic phenomena under the high fluence/flux irradiation, i.e., radiation-induced conductivity (RIC), carrier removal (CR) and photoconductivity suppression (PCS) under simultaneous photon/ion irradiation, have been studied in N-doped and undoped 6H-SiC under 17 MeV proton irradiation. The CR, RIC, and possibly PCS, strongly depend on the carrier density of the samples. With the higher carrier density, the higher stability of the RIC and of the dark-conductivity (σ_d) against the radiation is attained. The dependences of the CR, RIC and PCS are similar to those of Si, and similar mechanisms are expected. However, since defect introduction rate of 6H-SiC is much lower than that of Si [6], an N-doped 6H-SiC shows the stabilized σ_d and RIC, up to much higher fluence than doped Si.

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Materials Science Forum Vols. 338-342 (2000) pp. 981-984

Study of Contact Formation by High Temperature Deposition of Ni on SiC

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Keywords: Auger Electron Spectroscopy, Auger Lineshape, Contact Formation, Contacts, Graphite Intercalation, High Temperature Annealing, Hydrogen Etching, Nickel Silicide, Ohmic Contacts

Abstract

We report the observation, by scanning tunneling microscopy (STM), scanning electron microscopy (SEM), Auger electron spectroscopy (AES), and atomic force microscopy (AFM), of island formation on SiC during high temperature deposition and annealing of thin Ni films. Ni films with a nominal thickness of 2.5 monolayers were sputter deposited onto H_2-etched single crystal 6H-SiC (0001) substrates heated to 600°C in an ultrahigh vacuum STM system. After the substrates were annealed to 800-1000°C, island formation was observed by STM. The islands were 0.1-0.5 μm in diameter, ~30 nm high, and separated by ~2 μm from each other, with an exceptionally flat top with a peculiar 'stitched' surface structure. A second type of island, ~1.5 μm in diameter, ~10 nm high, and separated by ~10 μm from each other, was observed by *ex situ* AFM and SEM. Microspot AES showed that the first islands are composed of Ni and C, while the second islands are composed of Ni, C, and Si. AES lineshape studies showed that the carbon in both types of islands is graphitically bound as opposed to the carbon in the substrate which is carbidically bound. From comparisons to literature, we believe that the first islands are a new type of graphite intercalation compound. An indexing of Ni on the top graphite sheets is presented for each anneal temperature.

Introduction

Although Ni deposited at room temperature and annealed to 950°C to form Ni_2Si is the currently favoured ohmic contact to n-type SiC, much of the physics of contact formation is not adequately understood. For example, the fate of the carbon liberated from the SiC during silicide formation, and its effect on contact properties and reliability, is not known. Using transmission electron microscopy it is shown that excess C and voids remain at the interface between bulk SiC and Ni_2Si in newly formed silicide contacts [1]. It seems likely that this will have an effect on the quality of the contact, and that further study is warranted, possibly with the goal of eliminating voids and C inclusions.

This paper is part of a larger study that examined the formation of nickel silicide contacts by sputter depositing Ni films of varying thickness (from sub- to 1000 monolayers) onto 4H- and 6H-SiC substrates at room temperature up to 1000°C. Our primary goal was to ascertain if high temperature deposition of Ni generated improvements over room temperature deposition followed by high temperature annealing by (i) inducing the formation of NiSi and creating a lower impedance contact,

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(ii) lowering the temperature required to form Ni_2Si, or (iii) removing C inclusions and associated voids from the interfacial and bulk regions of Ni_2Si contacts. *In situ* analysis was performed with a combination of reflection high energy electron diffraction (RHEED), low energy electron diffraction (LEED), and/or scanning tunnelling microscopy (STM). Post deposition analysis included microspot and lineshape Auger electron spectroscopy (AES), atomic force microscopy (AFM), and x-ray diffraction (XRD).

In this report, all Ni films were deposited to 2.5 monolayers nominal thickness onto on-axis 6H-SiC substrates heated to 600°C. STM analysis was performed *in situ*, and AES, AFM, and SEM analysis was performed *ex situ*. All SiC substrates were solvent cleaned, H_2 etched [2], and heated to 1000°C in vacuum prior to deposition, and LEED and STM analysis revealed clean ($\sqrt{3} \times \sqrt{3}$) SiC surfaces.

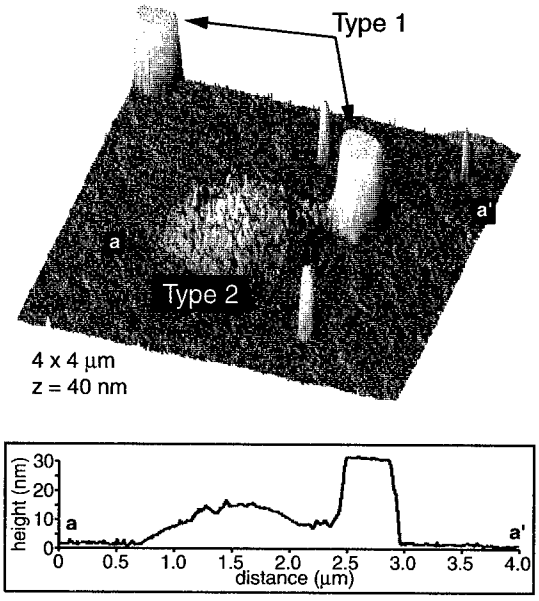


Figure 1 : 4 x 4 μm AFM image showing two large Type 1 islands, one Type 2 island, and three small diameter, possibly Type 1, islands. The profile linescan shows typical shapes of the two island types.

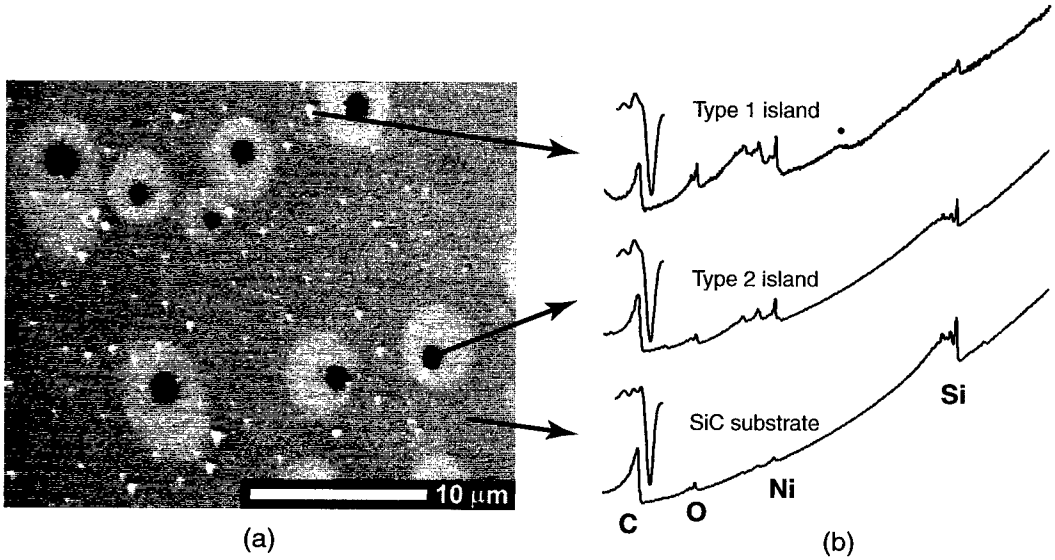


Figure 2 : (a) SEM image of both island types, (b) microspot AES spectra of both island types and a substrate region without islands. Insets above the carbon peaks are first-derivative high energy-resolution scans of the carbon KVV peak at 270 eV. The feature (marked ·) on the top spectrum (Type 1 island) is an artifact from drift compensation.

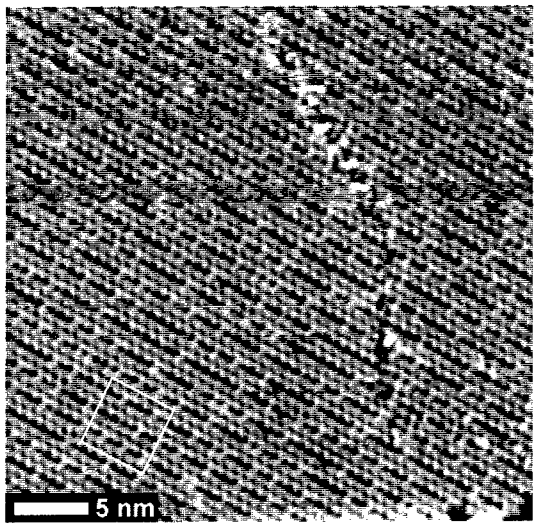
Results and Discussion

At low film thicknesses and intermediate depositions temperatures (between 600 and 800°C), marked differences were observed between films deposited at room temperature and annealed to high temperature vs. films deposited at the same high temperature. Specifically, for films deposited at 600°C onto on-axis 6H substrates, the formation of two types of islands that are randomly distributed across the sample, and with respect to each other, was observed. The first islands (Type 1) are 0.1-0.5 nm in diameter and 30 nm tall, are separated by ~2 μm from each other, and have exceptionally flat tops with a peculiar 'stitched' top surface structure as observed with STM. The second islands (Type 2) are about ~1.5 μm in diameter and ~10 nm tall, and are separated by ~10 μm from each other. These islands are not faceted, and have a rough irregular surface. Both island types are shown in an atomic force microscope image in Figure 1. While Figure 1 shows a Type 1 island in contact with a Type 2 island, in general there was no observed correlation between the locations of the islands.

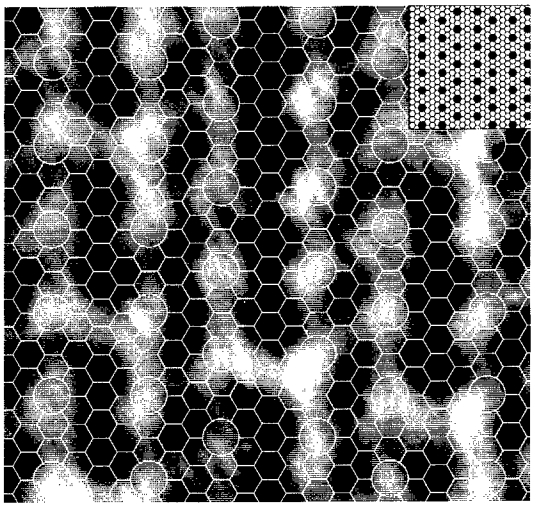
Figure 2a shows a SEM image with representative locations where microspot AES was performed. Multiple scans with AFM and SEM, and comparisons of feature sizes and geometries, were used to determine that the small bright spots observed by SEM are Type 1 islands, and larger dark spots are Type 2 islands. The large bright areas surrounding all Type 2 islands (Fig. 2a) was observed to be a ~1 nm depression by AFM, but was not seen to be chemically different from nearby substrate areas by AES. The source of the strong SEM contrast is under investigation but may be caused by a chemical difference in the first few monolayers of the surface.

Microspot AES has shown that Type 1 islands are composed of Ni and C, while Type 2 islands are composed of Ni, C, and Si (Figure 2b). AES lineshape studies show that the C in both types of islands is graphitically bound as opposed to the carbon in the substrate which is carbidically bound [3].

In situ STM analysis of Type 1 islands revealed a novel surface structure that changed with



(a)



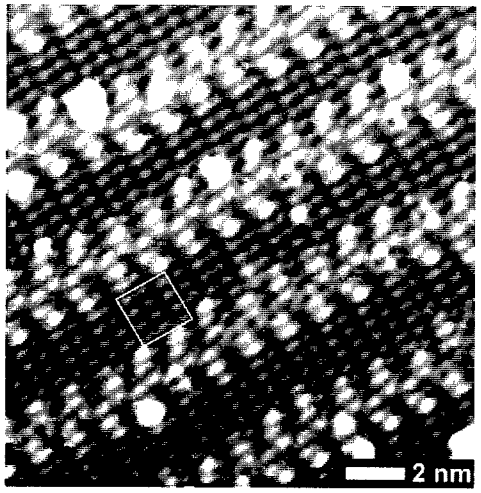
(b)

Figure 3 : (a) STM image of the top of Type 1 island after annealing to 900°C (V_T=2.18V, I=200pA). (b) STM image of marked box from (a) overlaid with proposed Ni on graphite structure. Inset is a schematic of the proposed surface structure - solid circles are Ni atoms, hexagons are the underlying graphite.

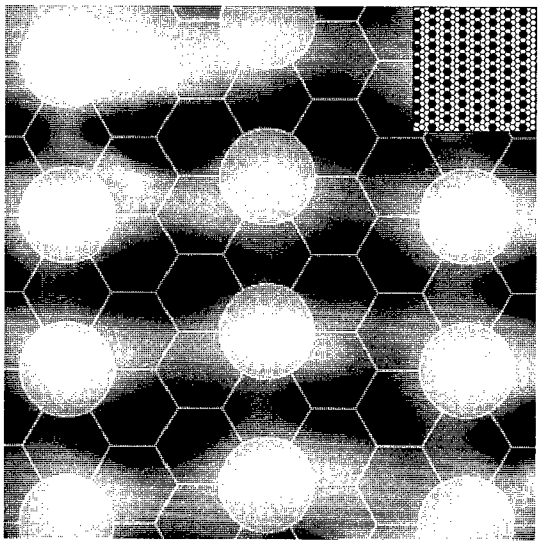
annealing temperature. Figures 3a and 4a show the structures observed after annealing to 900°C and 1000°C respectively. From the STM, SEM, AFM and AES observations, and from comparisons with literature, it is believed that these islands (Type 1) are a type of graphite intercalation compound that has not been previously observed. Graphite intercalation compounds (GICs) [4-7] are compounds formed from alternating sheets of graphite and a second, intercalating, species. The intercalating species, commonly an alkali metal, is arranged in a periodic lattice within the galleries between the graphite sheets. Proposed indexing of Ni on the top graphite sheet, observed by STM, is shown in Figures 3b and 4b. One-dimensional periodic structures are commonly seen by STM of GICs, and are attributed to either intercalant depletion in sub-surface galleries [5,6], or to charge-density wave effects [7].

The nature of the observed Type 2 islands is not fully understood at this time and is the subject of current study.

For other depositions conditions (thicker films, lower deposition temperature, etc.) no island formation was observed, but significant carbon segregation to the surface of the nickel silicide contact layer was found with increased substrate temperature during deposition.



(a)



(b)

Figure 4: (a) STM image of the top of Type 1 island after annealing to 1000°C (V_T=-2.0 V, I=250 pA). (b) STM image of marked box from (a) overlaid with proposed Ni on graphite structure. Inset is a schematic of the proposed surface structure - solid circles are Ni atoms, hexagons are the underlying graphite.

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Ohmic Contact Formation on n-Type 6H-SiC using $NiSi_2$

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Keywords: $NiSi_2$, Ohmic Contacts

Abstract The structural and electrical properties of $NiSi_2$ ohmic contact formed on n-type 6H-SiC have been investigated using Rutherford backscattering spectrometry(RBS), X-ray photoelectron spectrometry(XPS), and I-V characterization. The $NiSi_2$ films on n-type (0001)-oriented SiC substrates with the net doping concentration of 1×10^{18} and 3×10^{16} /cm^3 are formed by annealing the deposited Ni and Si films, whose thicknesses are designed to produce the stoichiometric $NiSi_2$ alloy, at 900 °C for 10 min in Ar+5%H_2 flow. RBS and XPS investigations reveal that the compositon of the formed alloy corresponds to the stoichiometry of $NiSi_2$ and there is no reaction of the deposited film and the substrate. The I-V characterization shows that the formed $NiSi_2$ film is a good ohmic contact for n-type SiC.

Introduction

The wide gap semiconductor SiC is of great interest for the high power control and high-speed communication devices because of the high breakdown field strength and high saturation velocity of the carriers. The ohmic contact is of importance in the electron devises such as metal-oxide-semiconductor (MOS) field effect transistor. Ni metal has been often used as the material for the ohmic electrode on the n-type SiC. The formation of Ni-based electrode requires the high temparature treatment above 1000 °C. The thermal treatment at the high temperature deforms the electrical properties of other components in the electron devices such as MOS structure. It has been reported that Ni_2Si is the only observed phase and C atoms distribute without its compound in the annealed Ni-based electrode layer[1]. The large void has been also observed in the electrode layer[2]. The generation of the void has been connected to the direct reaction of Ni and SiC substrate. To fabricate the SiC electron device with a high performance, the low temperature process and the restriction of the reaction between the electrode materials and the SiC substrate are desired.

In this study, we note that the formation of Ni silicide is an important process in the fabrication of ohmic contact on n-type SiC. In the reaction of Ni film with Si substrate, the congruent phases of Ni_2Si and NiSi are formed at the annealing temperatures at 350 and 750 °C, respectively. $NiSi_2$ alloy, which is the most stable phase in the reaction of Ni and Si, is formed by the treatment above 750 °C[3]. It is expected that the formation of Ni silicide from the deposited Ni and Si films restricts the generations of void and the residual C atoms in the electrode layer. We report at the first time the structural and electrical properties of the $NiSi_2$ alloy formed on the n-type 6H-SiC substrate.

Experiments

Substrates used in this study were (0001)-oriented n-type 6H-SiC, which were provided from Cree Research, with the net doping concentration ($N_d - N_a$) of 1×10^{18} and 3×10^{16} /cm^3. After the standerd cleaning, Si film with a thickness of 90 nm and Ni film with a thickness of 30 nm are deposited on the (0001)Si face of the substrate (Ni/Si/SiC structure) using E-gun evaporation in a vacuum of the order of 10^{-5} Pa. The thicknesses of Si and Ni films were designed to form stoichiometric $NiSi_2$ alloy, assuming that the density of the deposited films is identical to that of the bulk. The $NiSi_2$ layer with a thickness of about 90 nm is expected to be formed after the reaction of the Ni and Si films. The samples were annealed at 800 and 900 °C for 10 min in Ar+5%H_2 flow, respectively. The annealing of sample was carried out using a conventional furnace with a sealed tube to avoid the oxidation of the sample. For comparison, the Ni film with a thickness of 120 nm was deposited on the (0001)Si face of the substrate (Ni/SiC structure) under the same condition described above. The Ni deposited sample was annealed at 1100 °C for 15 min.

The composition of the formed alloy was investigated using Rutherford backscattering spectrometry

(RBS) and X-ray photoelectron spectrometry (XPS). The RBS measurements were carrid out using 1.5 MeV $^4He^+$ ions with a scattering angle of 150°. The XPS analyses were performed using ULVAC PHI 5600 with a Mg Kα line. To obtain the depth profile, the surface layer of the sample was repeatedly removed by an Ar ion sputtering at an ion energy of 5 keV. The I-V characterization was performed using Keithley 2400 source meter combined with a micro-probe equipment at room temperature. The contact resistance was evaluated for the electrode with an area of 0.325×0.325 mm^2 and an interval of 0.325 mm on the SiC substrate with a width of 0.325 mm and a thickness of 0.4 mm.

Results and Discussion

Figures 1(a) and (b) show the RBS spectra taken from the Si and Ni deposited (Ni/Si/SiC) and the Ni deposited (Ni/SiC) samples, respectively. After annealing of Ni/Si/SiC sample at 900 °C for 10 min, the deposited Ni film completely reacts with the deposited Si film. The composition of the formed Ni-Si alloy is estimated to be Ni:Si = 1:2 by a surface approximation method[4]. The estimated composition is consistent with the amount of the deposited Ni and Si atoms on the SiC substrate. The thickness of the film is estimated to be 90 nm from the RBS simulation developed in Hosei Univ. The sharp edge of the Ni signal at the interface in the spectrum indicates that the interface of the Ni silicide and SiC substrate is abrupt after the annealing(see fig 1(a)). It is suggested that the deposition of Ni and Si films corresponding to the stoichiometry of silicide suppresses the reaction of Ni and SiC substrate. On the other hand, for the Ni/SiC samples annealed at 1100 °C for 15 min, the composition of Ni silicide is estimated to be Ni:Si = 2:1(see fig 1(b)). In the Ni/SiC sample the unclear interface is connected to the low quality of the interface morphology as reported in TEM study[2].

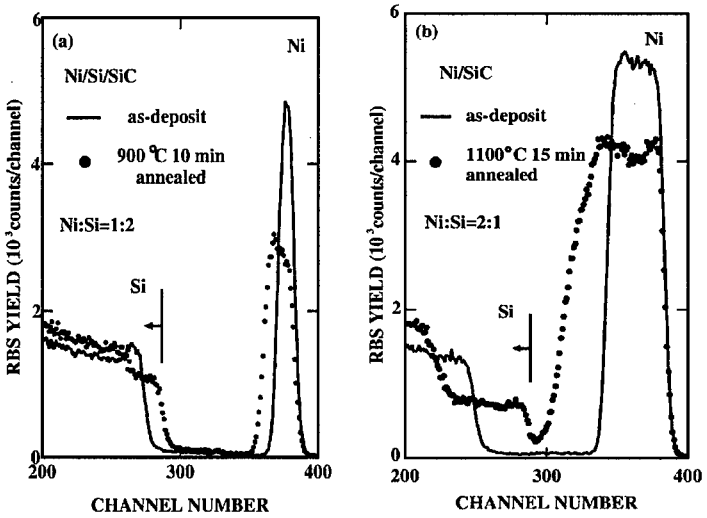

Figure 1 RBS spectra for (a) the Ni/Si/SiC and (b) the Ni/SiC samples before and after annealing. The annealing temperatures for the Ni/Si/SiC and Ni/SiC samples are 900 and 1100 °C, respectively.

Figures 2(a), (b), and (c) show the XPS spectra of Si 2*p*, Ni 2*p*, and C 1*s*, respectively, obtained from the Ni/Si/SiC sample annealed at 900 °C. The spectra in the bottom of these figures show the XPS signals from the top surface layer of the sample. In the spectra at the top layer, the signals of Si 2*p* are attributed to the Si oxides, while the signals from Ni and C atoms can not be detected. The SiO_2 layer may be formed by the oxidation of the excess Si atoms in the formed film. The Si oxide is also observed at the interface between the silicide and the SiC substrate. This Si oxide is originated from the residual oxide on the surface of the SiC substrate which can not be removed by HF acid treatment[5]. The peak energies of Si 2*p* (99.5 eV) and Ni 2*p* (854eV) in the silicide layer are identical to those from $NiSi_2$ layer formed by the reaction of Ni film and Si substrate. No signal from C atoms can be detected in the $NiSi_2$ layer. At the interface, the signals from C atoms are contributed only from those in the SiC substrate. The results from XPS and RBS measurements indicate that the reaction between the $NiSi_2$ alloy and the SiC substrate is restricted by the deposition of Ni and Si films on the substrate.

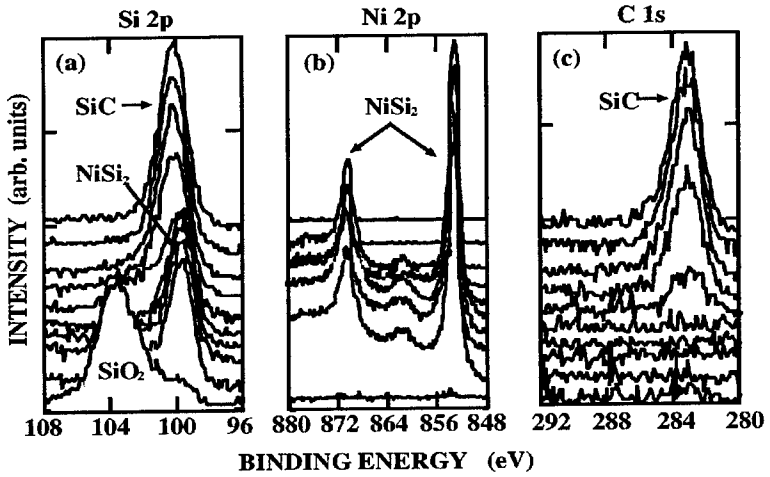

Figure 2 XPS spectra of (a) Si 2*p*, (b) Ni 2*p*, and (c) C 1*s*, from the Ni/Si/SiC sample annealed at 900 °C. The excitation X-ray is a Mg Kα line. The bottom spectra indicate the signals from the top surface layer.

Figure 3(a) shows the I-V characteristics for the $NiSi_2$ contact on the substrate with a doping level of 1 $\times 10^{18}$ /cm^3. The Ni/Si/SiC samples show the good ohmic characteristics for the annealing at 800 and 900 °C. The resistance decreases with the increase of annealing temperature from 800 to 900 °C. The decrease of resistance may be arising form either the crystallinity improvement of $NiSi_2$ layer such as the increase of the grain size or the improvement of the interface morphology. Figure 3(b) shows the plot of resistance vs electrode distance for the Ni/Si/SiC sample annealed at 900 °C. The contact resistance (R_C) is estimated to be 5.5 Ω by extrapolating data to distance = 0. The obtained contact resistance is similar to that for the Ni/SiC sample. The specific contact resistivity is estimated to be 3.9×10^{-3} ohm-cm^2 which corresponds to the schottky barrier height of 0.4 eV in accordance with the thermionic emission model[6,7].

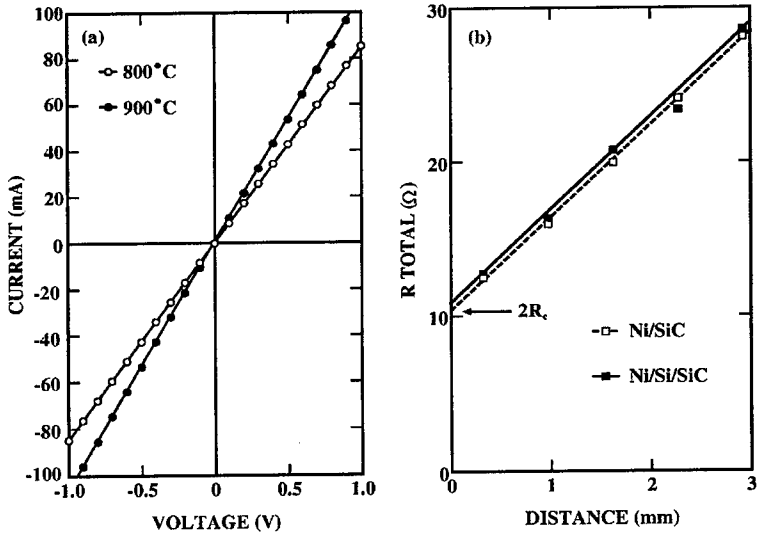

Figure 3 (a) I-V characteristics for the Ni/Si/SiC samples annealed at 800 and 900 °C for 10 min. (b) plot of the resistance vs electrode distance for the Ni/Si/SiC sample annealed at 900 °C for 10 min and the Ni/SiC sample annealed at 1100 °C for 15 min, respectively. The doping concentration of substrate is 1 $\times$ 10^{18} /cm^3.

The ohmic contact based on the thermionic emission model should be available for a low doping concentration. Figure 4(a) and (b) show the results of I-V measurements for the $NiSi_2$ contact annealed at 900 °C for 10 min and Ni contact annealed at 1100 °C for 15 min on the substrate with the doping concentration of 3×10^{16} /cm^3, respectively. Note that the $NiSi_2$ contact shows the ohmic characteristics, while Ni contact shows the schottky-like characteristics. The ohmic properties of $NiSi_2$ contact arises from the abrupt interface between the contact and the substrate. We conclude that the formation of the $NiSi_2$ alloy from the deposited Ni and Si films is able not only to prevent the reaction of Ni with SiC and to lower the process temperature, but also to fabricate the ohmic contact available in the low doping concentration. It is suggested that the thermionic emission is a dominant mechanism in the carrier transportation at the interface of $NiSi_2$ and n-type SiC.

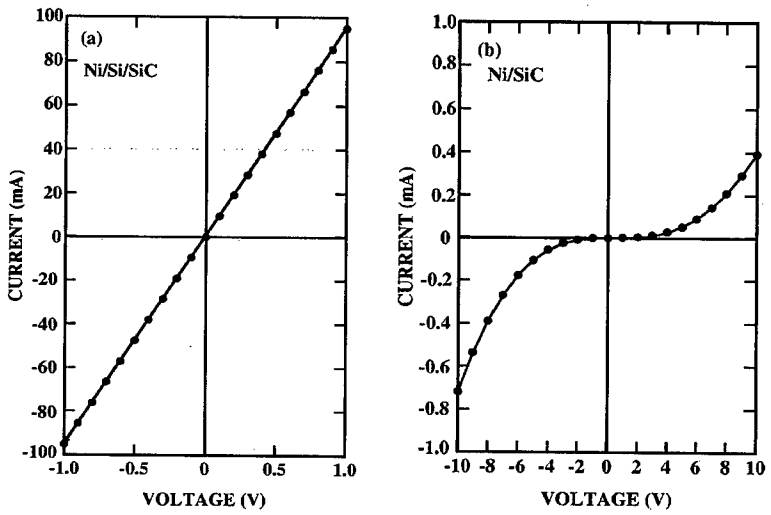

Figure 4 I-V characteristics of (a) the $NiSi_2$ contact annealed at 900 °C for 10 min and (b) the Ni contact annealed at 1100 °C for 10min on the substrate with the doping concentration of 3×10^{16} /cm^3, respectively.

Conclusion

We reported the $NiSi_2$ ohmic contact on n-type SiC formed by annealing the deposited Ni and Si films, whose thicknesses are designed to produce the stoichiometric $NiSi_2$ alloy, at 900 °C for 10 min. The interface between the $NiSi_2$ film and the SiC substrate is much more abrupt than the Ni based contact. The $NiSi_2$ film has the ohmic characteristics for the doping concentration of both 1×10^{18} and 3×10^{16} /cm^3. It was suggested that the thermionic emission is a dominant mechanism in the carrier transportation at the interface of $NiSi_2$ alloy and n-type SiC substrate. The details of the schottky barrier height will be discussed in elsewhere.

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Lowering the Annealing Temperature of Ni/SiC for Ohmic Contacts under N_2 Gas, and Application to a UV Sensor

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Keywords: 6H-SiC, Alloy, Implantation, Junction, n^+p, Ni, Ohmic Contacts, Responsivity, UV Sensor

Abstract. The key technology for a UV sensor is forming a very shallow pn junction and ohmic contacts at this junction. A 6H-SiC UV sensor with high responsivity was realized by introducing nitrogen implantation and lowering the annealing temperature of Ni/SiC for ohmic contacts under N_2 gas. The junction depth of this UV sensor was about 0.1 μm and the responsivity was 187.6 mA/W with a wave length of 290 nm at room temperature. We succeeded in operating this sensor at 700°C.

1. Introduction

Ni is suited for n-type 6H- and 4H-SiC ohmic contacts because it offers a low specific contact resistance [1]. The annealing temperature of Ni/SiC for ohmic contacts is usually about 1000°C. A lower annealing temperature of Ni/SiC is also required for ohmic contacts in order to prevent the Ni on the thin n^+p junction surface of devices, such as a UV sensor, from breaking through to the p region, as the junction depth is as low as 0.2 μm. This is because Ni has a large diffusion constant for SiC [2]. The I-V characteristics of sensor metals must have a perfect linearity to treat a very small current signal. We examined the differences in annealing temperatures for ohmic contacts under Ar and N_2 gases, and succeeded in lowering the annealing temperature of Ni/SiC for ohmic contacts by using the N_2 gas. Then, we used the nitrogen implantation and this method to fabricate a UV sensor.

2. Lowering the annealing temperature of Ni/SiC for ohmic contacts

We compared the annealing temperature of Ni/SiC for ohmic contacts under the annealing gas atmosphere, because there are no reports on this subject to our knowledge. A typical annealing furnace was used with a heater that can be moved for rapid cooling. The sample was placed on a quartz plate. Figures 1 (a) and (b) show the I-V characteristics between Ni contact metals (diameter: 300 μm, pitch: 400 μm) at 1000°C for 5 min under Ar gas and N_2 gas with a flow at 1 l/min, respectively. Ni with a thickness of 4000A was deposited by EB evaporation under the base pressure of 8×10^{-7} Torr onto a 6H-SiC of 0.2 μm thick n-type epilayer doped with 4×10^{17} cm^{-3}. Ohmic contacts

were obtained with the N_2 gas, but not with the Ar gas. The annealing temperature of the ohmic contacts was 1050°C under Ar gas, and 900°C under N_2 gas. The specific contact resistance was 3.8 $\times 10^{-3}$ Ωcm^2 for Ar gas at 1050°C as determined by a four point measurement. Figures 2 (a) and (b) show the AES depth profiles of Ni/SiC alloy layers annealed at 1050°C for 10 min under Ar gas and at 900°C for 5 min under N_2 gas. The AES profile patterns were nearly the same under different temperatures, and the atomic concentration ratio of Ni/Si was about 2.3. This result shows that the annealing temperature of Ni/SiC ohmic contacts for N_2 gas is 900°C and the atomic concentration of C between Ni silicide and SiC increases for both Ar gas and N_2 gas. Figure 3 shows the results of the RBS analysis of Ni/SiC for the Ar and N_2 gas alloys. We confirmed that the composition of Ni silicide at 1000°C was Ni_2Si by comparing our results with the result of J. Crofton et al., and by examining the peak ratio between the Ni silicide to the Si in the Ni silicide of the RBS analysis [3]. The transit layers of Ni silicide and SiC were the same for the Ar and N_2 gas alloys, but with N_2 gas, the thickness of the Ni silicide was a little larger than that for Ar gas. The origin for the differences between the Ni/SiC annealing temperatures may be the oxygen and moisture in the Ar and N_2 gas, as measured at room temperature at the exit of the alloying system; we measured 1.5 ppm and 2.6 ppm for oxygen, and 1.6 ppm and 5.0 ppm for moisture, respectively. Clearly, oxygen and moisture were not the origin of the above phenomenon.

The surfaces of the Ni metals in the Ar and N_2 gas alloys were observed by using SEM. The annealing conditions were at 1000°C for 20 min. For N_2 gas, the grain size of the Ni silicide was smaller than that for Ar gas. In addition, the surface flatness for N_2 gas was better than that for Ar gas. This grain size increased in response to longer annealing and higher temperatures. The difference in the above phenomenon for Ar and N_2 gases is not yet clear; perhaps, the N_2 gas promotes the Ni/SiC

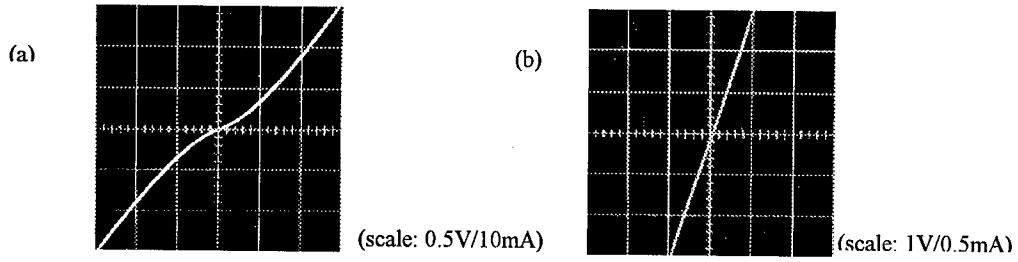


Fig. 1. I-V characteristics of Ni/SiC alloy metals at 1000°C for 5 min: (a) Ar gas, and (b) N_2 gas.

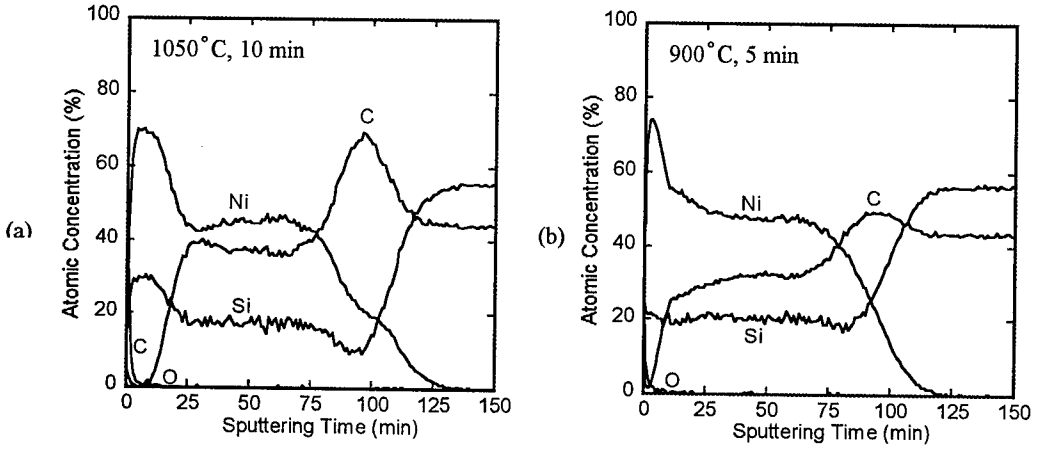


Fig. 2. AES depth profiles of an Ni/SiC alloy layer: (a) Ar gas, and (b) N_2 gas
(Sensitivity factor; Si: C: Ni: O=0.069: 0.128: 0.281: 0.296)

alloy reaction or changes the SiC surface. Otherwise, Ar gas prevents the Ni/SiC alloy reaction.

Next, we examined methods for lowering the Ni annealing temperature with an N^+ implant on an n-type epilayer doped with $1.6x10^{17}$ cm^{-3} in order to increase the surface impurity concentration. To obtain the thinnest possible implanted layer, we used the following conditions: 30 keV for the implant energy, $5x10^{14}$ cm^{-3} for the dose, 7° off for the wafer tilt angle, and 800°C for the implanted temperature. TRIM simulation showed that the ion depth (R_p) was 727A and the maximum doping density was $8.7x10^{19}$ cm^{-3}. The implanted layer was annealed at 1150°C for 10 min under N_2 gas, and 2000A thick Ni was evaporated by EB, and alloyed. Good ohmic contacts were formed at 800°C for N_2 gas, and at 850°C for Ar gas. The Ni annealing temperature under N_2 was about 50°C lower than that under Ar. For a $5x10^{15}$ cm^{-3} dose, the non-annealing contact layers showed nearly ohmic characteristics, but for a $5x10^{14}$ cm^{-3} dose, the characteristics were non-linear. Thus, the high surface concentration clearly leads to a lower Ni/SiC alloy temperature.

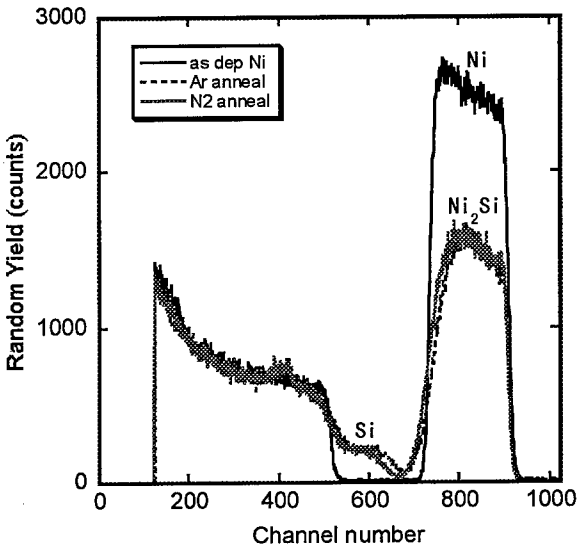


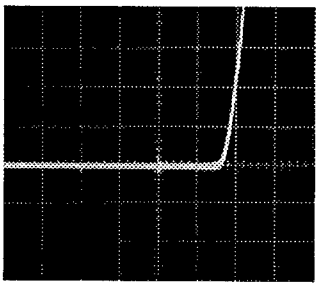
Fig. 3. RBS spectrum of Ni/SiC alloy layer annealed at 1000°C for 5 min.

3. Fabrication of 6H-SiC UV sensors with n^+p junction

With this N_2 gas alloying method, we fabricated a UV sensor, which is blind to visible light, by the process described here: 60 keV as the N^+ implant energy for the thin n^+ layer formation, $4x10^{14}$ cm^{-2} for the dose, 7° off for the wafer tilt angle, and 800°C for the sample temperature in a 3 μm thick p-type epilayer doped with $2.1x10^{16}$ cm^{-3} on a p^+ substrate. After implantation, the sample was annealed at 1150°C for 10 min under N_2 gas. This annealing temperature is equivalent to a typical temperature range for a Si process. R_p and ΔR_p from the TRIM simulation were 982 and 272A, respectively. The junction depth was estimated at about 0.2 μm. The sheet resistance of the implanted layer was 8.9 kΩ/□. From this result, we calculated the conductivity and the carrier concentration as 0.18 Ωcm and $5x10^{17}$ cm^{-3}, respectively. The etching depth of the mesa structure was 0.5 μm with 0.9 mm square for the area as performed by RIE, and Ni was evaporated to a thickness of 2000A with 0.08 mm^2 for the square ring type area. Next, we etched area outside of the Ni metal once more to the desired depth. The junction depth of the active area was about 0.1 μm. After the metal transparency conduction layer was deposited at 100A to achieve the same surface potential, the SiO_2 passivation layer was deposited at 1000A. The Ni alloy was done at 900°C for 1.5 min. After Al was evaporated to 2000A, the Al alloy was done at 850°C for 1.5 min. This sensor has an effective active area of 0.73 mm^2.

Figure 4 shows the I-V characteristics of the fabricated sensor. The built-in voltage from the I-V characteristics of fig. 4 was about 2 V, and the breakdown voltage 250V. The ideality factor (n) from the I-V characteristics and V_b from the $1/C^2$-V characteristics were 2 and 3V, respectively. We confirmed the step junction with these results. Figure 5 shows the responsivity vs. the wave length at room temperature for the device. The maximum value was 187.6 mA/W at 290 nm. This device has a spectrum side peak at 220 nm. This peak is the same as a characteristic of a UV sensor with a deposited SiO_2 film as shown in Cree's data [4]. The I-V characteristics and the responsivity

depended on the implanted energy and the dose. The lower implantation energy increased the responsivity, and the I-V characteristics were leaky below 60 keV for the implantation energy or over 10^{15} cm^{-2} for the dose. In addition, the higher implantation energy decreased the responsivity over 60 keV. We obtained poor responsivity with 100 keV. The best ion implantation condition was 60 keV for the implantation energy and an order of 10^{14} cm^{-2} for the dose. The dark current of this sensor was 200 pA (2.73×10^{-8} A/cm^2) at -10V. This dark current was on an order of 2~3 larger than that of the usual epitaxial junction type sensor [4]. Lastly, we succeeded in operating this sensor at 700°C. The responsivity at 500°C was about two times that at room temperature.



(scale: 1V/5μ A)

Fig. 4. I-V characteristics of UV sensor.

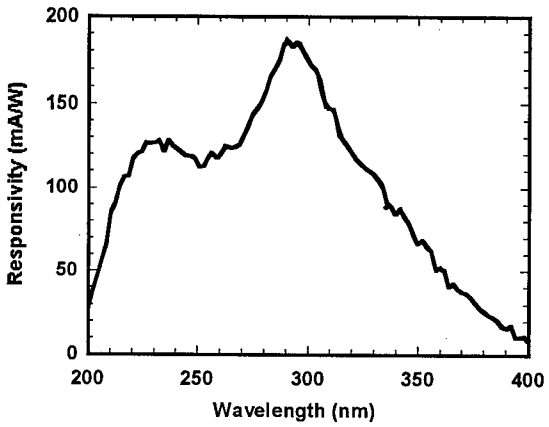


Fig. 5. Responsivity of UV sensor at room temperature.

4. Summary

We examined the differences in the annealing temperatures of Ni/SiC for ohmic contacts under Ar gas and N_2 gas, and found that N_2 gas is better at lowering the annealing temperature. We applied this N_2 gas annealing method to the fabrication of a UV sensor. The Ni contacts were formed at an annealing temperature of 900°C. The responsivity at room temperature for the N^+ implanted UV sensor with an active area of 0.73 mm^2 was 187.6 mA/W at 290 nm. This sensor can be used for a combustion system, a flame detector, a fire alarm, a UV detector, etc.

Acknowledgement

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Materials Science Forum Vols. 338-342 (2000) pp. 993-996

Adhesion and Microstructure of Ni Contacts to 3C-SiC

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Keywords: Adhesion, Interface, Ohmic Contacts, Scratch Test, X-Ray Scattering

Abstract This paper reports on the mictrostructure-adhesion property relationship in Ni/3C-SiC ohmic contacts. The microstructures of the surface and the interface in the Ni/3C-SiC layers annealed at various temperatures were investigated using the X-ray scattering techniques. The adhesion of the Ni on the 3C-SiC surface was examined by the scratch tester in the acoustic emission-frictional force mode. The Ni/SiC layer annealed at 500 ℃ exhibits the highest surface roughness with the lowest interface roughness. The Ni/SiC adhesion force was shown to be decreased with the annealing temperature up to 500 ℃. As the annealing temperature is higher than 500 ℃, the domain size of the $NiSi_2$ silicides is increased with enhancement of crystallinity. The crystallinity enhancement is attributed, presumably, to the low mismatch of lattice constants between the silicide and 3C-SiC.

1. Introduction

The stable adhesion of contacts to the semiconductor surface is an important factor for the reliable device operation. In particular, ohmic contacts connect discrete devices to each other and to external circuits[1, 2]. Most of semiconductor devices are exposed to high temperature and harsh environment during the fabrication process. And the ohmic contacts are required to possess low contact resistance as well as thermal and chemical stability. SiC is potentially known to be an important semiconductor for the application of high power, high frequency, and high temperature electronic devices. Therefore, the reliability of the contacts to SiC surface must be investigated for the realization of the material into a commercial market. In this paper, we report on the formation of Ni ohmic contact to SiC at various annealing temperatures and the microstructure of the Ni/SiC interface using X-ray scattering techniques, rutherford backscattering spectrometry (RBS), and auger electron spectroscopy (AES). In particular, the adhesion force between the Ni ohmic contact and SiC is investigated and are compared with the results from the microstructure analysis. It is the purpose of this paper to This paper reports on the mictrostructure-adhesion relationship in the interface between the Ni ohmic contact and 3C-SiC surface.

2. Experiments

These experiments were performed using an epitaxially grown 3C-SiC wafer with a thickness of 1 μm on 4 °off (100) Si substrate. The 3C-SiC films were grown by a typical chemical vapor deposition (CVD) method and the doping concentration of the epi-layer was measured

to be about $1\times 10^{19}/cm^3$. The surface of the wafer was cleansed in H_2SO_4 : H_2O_2 (4 :1) solution for 10 min. at 120 ℃ for the elimination of any organics, and was dipped into 2 % HF for 10 sec. to etch out possibly deposited oxide on the surface. After the cleansing process, Ni layer with a thickness of 3000 Å was deposited using an e-beam evaporator under a pressure of 10^{-7} torr. The annealing of the samples was performed in a pre-heated tube furnace for 30 min. at different temperatures; 500 ℃, 800 ℃, and 1030 ℃. Oxygen or Argon gas was flown (1.4 l/min) into the furnace during the heating and cooling process. The adhesion force of the Ni contact to the SiC surface was evaluated using a scratch tester (CSEM/REVESR scratch tester) in an acoustic emission-frictional force mode. The Ni/SiC interface was investigated using the X-ray scattering techniques, rutherford backscattering spectrometry (RBS), and auger electron spectroscopy (AES).

3. Results and Discussion

The Ni/SiC layer annealed at 500 ℃ exhibits the highest surface roughness with the lowest interface roughness as is shown in the reflected X-ray beam intensity (Fig. 1 (a)). The Ni/SiC adhesion force was shown to be decreased with the annealing temperature up to 500 ℃. The adhesion force was higher for the samples annealed under the oxygen atmosphere compared to those under argon atmosphere. The results of RUMP simulation suggests that the oxygen atoms were diffused into the interface between the Ni and 3C-SiC while the carbon atoms were accumulated at the interface, which led to the decrease of adhesion. Fig. 1 (b) shows the RBS spectra for the Ni/3C-SiC after annealing at 500 ℃, 800 ℃, and 1030 ℃ under the O_2 atmosphere. Fig. 2 (a) shows the change of adhesion force in the Ni/3C-SiC interface as a function of annealing temperature and Fig. 2 (b) is a micrograph showing the tensile cracking mode after the sample was scratched. It is believed that the strain at the Ni/SiC interface is caused by the formation of silicides[7]. The strain at the interface is increased with the increased volume of silicides. Meanwhile, the strain can be reduced by the formation of $NiSi_2$ at high temperature. As the crystallinity of silicides is improved, the strain is reduced. The reduced strain can improve the adhesion force as is shown in Fig. 2 (a). At the annealing temperatures higher than 500 ℃, the domain size of the $NiSi_2$ silicides is increased with the enhancement of crystallinity. Fig. 3 (a) shows the results of long-scanned X-ray scattering peaks of samples annealed at different temperatures. The as-deposited sample exhibits Ni(111), Ni(200) peaks and SiC(200) peak. The rocking curves for the Ni peaks showed that the Ni layer was deposited onto SiC as powders as is shown in Fig. 3 (b). The SiC (200) peak, meanwhile, exhibits excellent crystallinity with the FWHM (full width half maximum) of 0.734. As the heat treatment temperature is increased to 500 ℃, the intensity of Ni peaks are increased and the FWHM is enhanced. As a result, the domain size of Ni is increased and Ni silicides were formed in the Ni/SiC interface. When the temperature reached as high as 800 ℃, none of the Ni peaks were found any more. It is believed that all Ni phases existed at lower temperatures were used up for the formation of Ni silicides. The FWHM of silicides ($NiSi_2$) formed at 800 ℃ was about 1.1134 and the crystallinity was found out to improve with annealing temperatures (FWHM of 1.026 at 1030 ℃). The enhancement of crystallinity of the silicide is attributed, presumably, to the low mismatch of lattice constants between the silicide(a=5.406 Å) and 3C-SiC(a=4.360 Å).

4. Conclusion

The mictrostructure-adhesion property relationship in the Ni/3C-SiC ohmic contacts was investigated using the X-ray scattering techniques. The adhesion of the Ni on the 3C-SiC surface was examined by the scratch tester in the acoustic emission-frictional force mode. The Ni/SiC layer annealed at 500 ℃ exhibits the highest surface roughness with the lowest interface roughness. The Ni/SiC adhesion force was shown to be decreased with the annealing temperature up to 500 ℃. As the annealing temperature increased higher than 500 ℃, the domain size of the $NiSi_2$ silicides is increased with enhancement of crystallinity. The crystallinity enhancement is attributed, presumably, to the low mismatch of lattice constants between the silicide and 3C-SiC.

Acknowledgment

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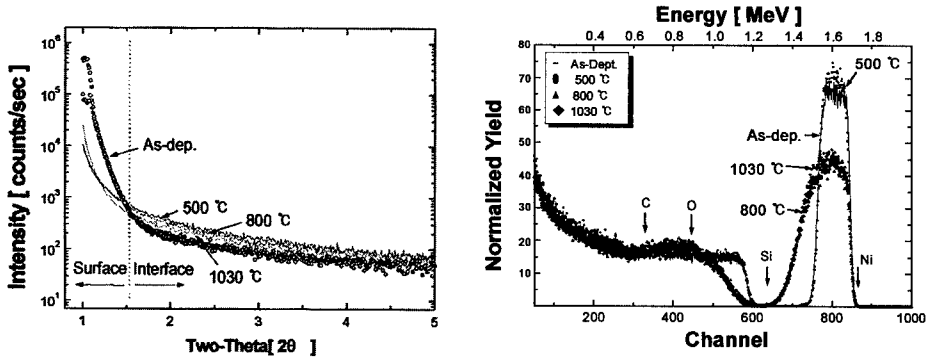
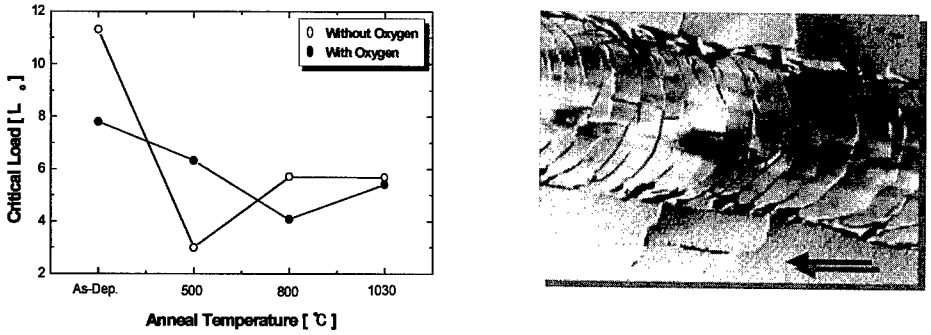


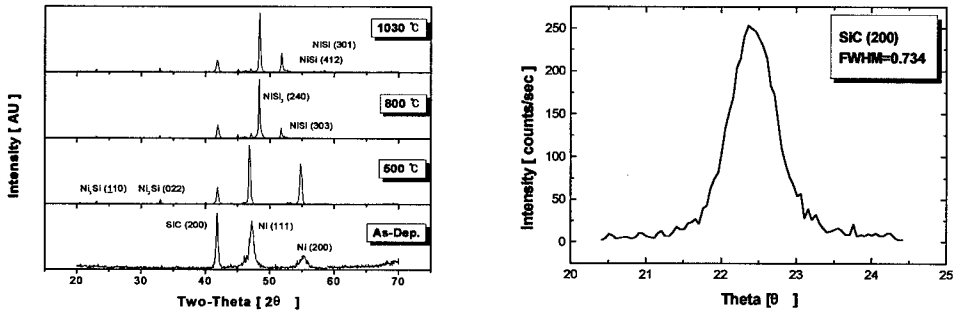
(a) (b)

Fig. 1 Change of the reflectivity after annealing at 500 ℃, 800 ℃, and 1030 ℃ (a) and the RBS spectra for Ni/3C-SiC after annealing in an O_2 Atmosphere (b).



(a) (b)

Fig. 2 Change of the critical load as a function of the annealing temperature (a) and scratch failure mode (tensile cracking) (b).



(a) (b)

Fig. 3 Results of long-scanned X-ray scattering peaks of samples annealed at different temperatures (a) and the rocking curves for the Ni peaks showing that the Ni layer was deposited onto SiC as powders (b).

Materials Science Forum Vols. 338-342 (2000) pp. 997-1000

Low Resistance Ohmic Contacts to n-SiC Using Niobium

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Keywords: Niobium, 'non-reacted' Ohmic Contact, RBS, Specific Contact Resistance, XPS

Abstract: We report the fabrication of high temperature ohmic contacts to n-type 4H- and 6H-SiC. Specific contact resistances (r_c) were measured using the linear transmission line method (LTLM) on epitaxial layers with doping concentrations (N_D) between 9.8×10^{16} cm^{-3} and 1.3×10^{19} cm^{-3}. Average values of r_c were 7.8×10^{-3} Ω-cm^2 for a 6H-epilayer of doping concentration 9.8×10^{16} cm^{-3} and 6.9×10^{-7} Ω-cm^2 for a 4H-epilayer of doping concentration 1.3×10^{19} cm^{-3}. Extensive mixing at the Nb/SiC interface was not observed in Rutherford backscattering (RBS) spectra following anneals at 1100C for 10min or more, and the results of x-ray photoelectron spectroscopy (XPS) measurements indicated that niobium carbide was present in the Nb layer.

Introduction: The need for low resistance ohmic contacts to SiC is critical for high power / high frequency device applications where parasitic resistances must be minimized. For high temperature applications, the contacts must also be stable at or above 300°C. The 4H and 6H polytypes of SiC are currently favored for device applications, and ohmic contacts have been developed for both polytypes [1]. Nickel is widely used to form ohmic contacts for n-SiC, and as an example, specific contact resistances as low as 4×10^{-6} Ω-cm^2 have been reported for a 6H doping concentration of 7×10^{18}cm^{-3} [2]. However, Ni forms an ohmic contact by reacting with the SiC epilayer to form Ni_2Si and carbon after short anneals of several minutes at around 1000°C [2]. This reaction is undesirable for contacts to thin epilayers since Ni and SiC are consumed in the ratio of approximately 1:1 during the formation of Ni_2Si. Herein, we report the fabrication of "non-reacted" Nb ohmic contacts to n-type 4H- and 6H-SiC. Compared to Ni, the Nb layer does not react extensively with the SiC epitaxial layer during contact formation.

Experimental Procedure: Niobium films of approximate thickness 200nm were sputter-deposited on 0.5 μm thick n-epitaxial layers grown on Si-face, off-axis, p-SiC substrates supplied by Cree Research. Details of the cleaning, fabrication and vacuum annealing procedures have been described elsewhere [3]. Patterened samples were prepared for LTLM / van der Pauw / RBS measurements together with 5mm x 5mm broad area samples for XPS analysis.

Results: As-deposited Nb contacts were rectifying. Barrier heights between 1.3 and 1.4eV were measured using C-V and XPS techniques for off-axis, Si-faced 4H samples. Agreement between the two techniques was excellent. Sheet resistances for the Nb films were measured with a four point probe and ranged between 13 and 18Ω/□ for as-deposited films, decreasing to approximately 3Ω/□ after anneals at 1100°C.

Typical RBS spectra (Fig. 1) show that small amounts of Cu are present in the as-deposited and annealed Nb films. Trace amounts of Si are also present throughout several of the as-deposited Nb layers (see channel numbers 250 to 285). The Cu signal appeared for all as-deposited samples and may result from contamination in the Nb sputter target. The Si contamination was likely introduced during sputter deposition and was not present in every sample. Three additional features stand out in Fig. 1(a). (1) A substantial amount of oxygen is present in the samples. (2) Structure appears in the top of the Nb signal - particularly after annealing. (3) A small shoulder (channels 240-260) appears on the Si signal for the annealed sample.

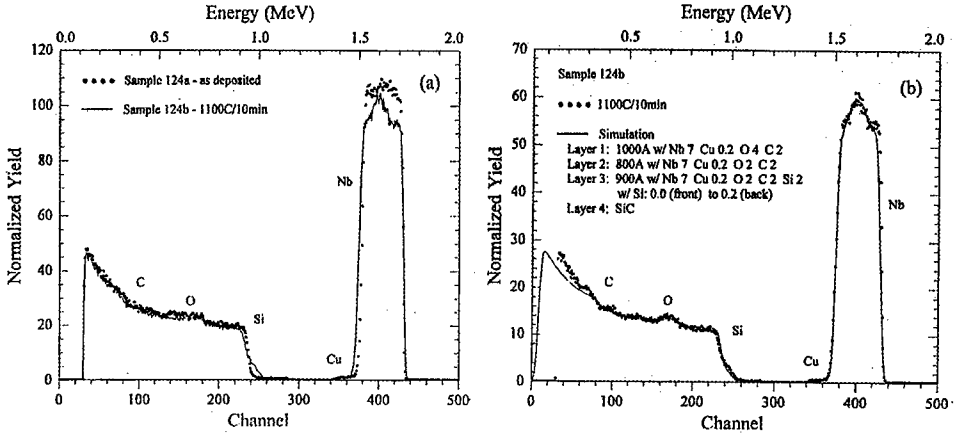

Fig. 1. RBS spectra for Nb/SiC taken with 2MeV He^+ ion scattered at 170°.

Oxygen incorporation during sputter deposition is a problem for the Nb layers. However, the oxygen content at the Nb / SiC interface decreased after annealing [compare oxygen signals between channel numbers 120 and 160 in Fig. 1(a)]. This movement of oxygen is consistent with the changes observed in the top of the Nb signal, and simulation of the RBS spectrum for an annealed sample [Fig. 1(b)] suggests a layered structure for the annealed Nb films. However, the structure in the Nb signal varied substantially from sample to sample, depending on the anneal times at 1100°C. Accordingly, we interpret the RBS simulations only qualitatively.

The small shoulder on the Si signal [Fig. 1(a)] was not observed for anneal times of less than 10min. This shoulder indicates the onset of mixing at the Nb / SiC interface with Si moving out of the SiC towards the surface of the Nb layer. Intermixing appears to start at approximately 10min for 1100°C anneals, and this process may help to remove the oxygen in the Nb film near the interface. However, the movement of Si is not substantial for these anneal conditions, i.e., intermixing is not extensive. Simulations of the carbon content in the annealed Nb films are much less accurate because of the smaller Rutherford scattering cross section for this light element. However, carbon is present in the films and must be included in the simulation in Fig. 1(b) in order to match the measured height of the Nb signal.

X-ray photoelectron spectroscopy depth profiles for as-deposited and annealed samples are shown in Figure 2. Standard Ar+ ion milling was used to generate the XPS depth profiles. Since XPS has inherently low lateral resolution, the possibility exists that a small fraction of the total photoelectron signal originates outside the sputter crater. Auger spectra were recorded periodically during the depth profiles to account for this possibility and to corroborate the formation of various chemical species. However, we cannot completely rule out the possibility that small portions of the C and O XPS signals arise from surface atoms located outside the sputter crater.

Carbon in the Nb films reacts to form NbC_x. The Nb in as-deposited, unannealed Nb films shows partial carbidic character, as indicated by the emergence of fine structure on the low energy side of the C(KLL) 272 eV Auger peak. Annealed Nb films (1100C / 10 min) show strong carbidic characteristics, with well-developed fine structure on the C(KLL) Auger peak and XPS binding energies (BE) in the range expected for NbC_x. The $Nb3d_{5/2}$ feature in the annealed film is located at a BE of 203.3eV, which is within the range measured for stoichiometric NbC (202.8- 203.4eV). Further, the C1s feature has a main peak (63%) at 284.6 eV (C-C and C-H_x) and a smaller component peak (37%) at 282.4eV. This BE is near, but not identical to, the literature value of 281.7eV for stoichiometric NbC [5]. We state that the carbide formed is NbC_x (with $x < 1$) because, to our knowledge, the BE for Nb_2C has not been measured. Therefore, we cannot rule out the existence of Nb_2C. As one approaches the Nb / SiC interface, the C1s peak shifts to 283.4 eV, the BE for SiC. It is difficult to determine the precise chemical species at the Nb / SiC interface (e.g., whether NbC, Nb_2C, or Nb_5Si_3C) by AES and XPS due to the lack of interfacial sharpness after annealing and the presence of oxygen at the interface.

Previous researchers have examined the diffusion path in Nb / SiC couples [6,7]. Feng, et al. [6] found that reaction was initiated at a temperature as low as 843°C. At 1405°C, the initial stage of reaction resulted in the layer sequence Nb / Nb_2C / Nb_5Si_3C / SiC. The same initial stage of reaction was observed

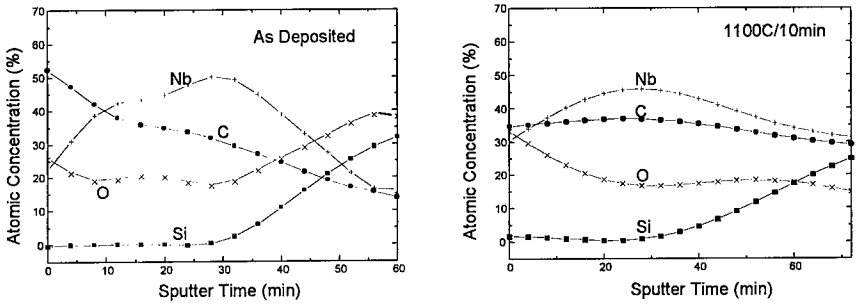

Fig. 2. XPS depth profiles for Nb films on 4H-SiC.

after annealing at 1517°C, but prolonged annealing at 1517°C resulted in the evolution of the complete diffusion path Nb / Nb_2C / NbC / Nb_5Si_3C / NbC / SiC, consistent with the Nb-Si-C phase diagram. It should be kept in mind that the SiC in these samples was polycrystalline and contained a few percent Al_2O_3. On the other hand, AES depth profiles obtained by Joshi, et al. [7] suggest similar results for Nb films sputtered on single crystal SiC substrates and annealed at 900-1100°C. Although precise identity of the phases adjacent to the SiC cannot be confirmed in our study, the formation of the Nb_5Si_3C phase at the contact / SiC interface is consistent with the RBS results discussed above.

Table 1 is a summary of the specific contact resistances measured using the linear transmission line method. Samples with higher doping concentrations were ohmic following anneals at 800C for as little as 1min. However, no attempt was made to determine contact resistance as a function of anneal temperature. The lowest measured specific contact resistance was $< 1 \times 10^{-6}$ Ω-cm^2 for sample #114 which had a doping concentration of 1.3×10^{19} cm^{-3}. Values below 10^{-6} Ω-cm^2 are shown in parentheses in Table 1 to indicate that we generally consider a specific contact resistance of approximately 1×10^{-6} Ω-cm^2 to be the lowest value that can be determined accurately using our LTLM geometry. For comparison, average values of the semiconductor sheet resistance (R_{SH}) are also summarized in Table 1. The TLM values for R_{SH} were determined by averaging the results from four separate TLM measurements. Each vdP value listed for R_{SH} is the average of measurements from three van der Pauw patterns fabricated on reactively ion etched isolation mesas.

Table 1. Results for Specific Contact Resistance Measurements. [a] 6H-SiC [b] 4H-SiC

Sample/ anneal time at 1100°C	N_D (cm^{-3})	Values of r_c (Ω-cm^2) for each TLM No.					Ave R_{SH} (Ω/□)	
		#1	#2	#3	#4	Ave.	vdP	TLM
157[a] /6min	9.8e16	8.1e-4	5.8e-3	1.4e-2	1.1e-2	7.8e-3	32042	66053
112[a] /10min	3.2e17	1.4e-4	1.4e-4			1.4e-4		3446
158[b] /3min	4.8e17	2.2e-4	3.2e-4	5.1e-4	5.0e-4	3.8e-4	1777	1682
113[a] /10min	1.4e18		1.6e-6	5.8e-6	1.6e-6	3.0e-6		1507
129[b] /8min	7.8e18	5.1e-5	1.0e-5			3.1e-5		534
125[b] /8min	> 1e19	1.9e-6	< 1e-6 (3.9e-7)	1.4e-5	2.1e-5	9.4e-6	183	278
114[b] /10min	1.3e19	1.0e-6	1.1e-6	<1e-6 (3.4e-7)	<1e-6 (3.1e-7)	<1e-6 (6.9e-7)		77

Conclusion: Niobium has been used to fabricate ohmic contacts to n-type 4H- and 6H-SiC. The values of the specific contact resistance are comparable to those obtained using Ni and range from approximately 8×10^{-3} to less than 1×10^{-6} Ω-cm^2 for doping concentrations between 9.8×10^{16} and 1.3×10^{19} cm^{-3}. Thermal anneals at 1100°C for up to 10 minutes produced very good ohmic contacts on moderately doped epitaxial layers. No significant (i.e., thick) reaction region was observed at the Nb / SiC interface. This is an

advantage for thin epilayers where silicide layers formed with reactive metals such as Ni might punch through. Ohmic behavior may result from the formation of carbide and silicide phases at the Nb / SiC interface. The results of long-term, high temperature annealing studies (not presented) show that the Nb / SiC ohmic contact is stable at 500°C. The Nb films do contain significant concentrations of oxygen following sputter deposition under moderate high vacuum conditions (10^{-6} Torr), and the films have been observed to oxidize further while in storage prior to annealing for ohmic contact formation. This problem for Nb / SiC can be minimized using UHV deposition techniques and by annealing immediately after deposition. Suitable cap layers may then be applied to the annealed layer.

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A Comparison of Single- and Multi-Layer Ohmic Contacts Based on Tantalum Carbide on n-type and Osmium on p-type Silicon Carbide at Elevated Temperatures

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Keywords: Metal-Semiconductor Interfaces, Ohmic Contacts

Abstract: The thermal stability of TaC ohmic contacts with and without Au, Pt, and W/WC overlayers were investigated on n-type 6H-SiC (0001) substrates. Specific contact resistivities (SCRs) were calculated at temperatures ranging from 20 to 400 °C in air. The TaC contacts with Au overlayers had the minimum SCR at room temperature, which was 1.4 x 10^{-6} Ω cm^2 on SiC with a doping level of 2.3x10^{19} cm^{-3}. The SCRs for both the Au/TaC/SiC (5.3 x 10^{-7} Ω cm^2) and the Pt/TaC/SiC (7.5 x 10^{-7} Ω cm^2) samples decreased with measurement temperature to 200 and 400 °C, respectively, while the latter samples showed reversibility after heating to 400 °C. W/WC/TaC/SiC samples showed the best stability after annealing at 400 °C for 144 hrs in vacuum. Changes in the electrical characteristics were correlated with increases in O incorporation in the contacts as a result of annealing. Investigation of the TaC/SiC interface by transmission electron microscopy indicated that there was little or no reaction between the materials. The Au, Pt and/or W/WC overlayers were required to prevent oxidation of the TaC and Os contacts during elevated temperature measurements. Osmium contacts annealed at 1020 °C for 1 h followed by 1075 °C for 15 min. displayed ohmic behavior on p-type (1 x 10^{19} cm^{-3}) SiC with SCRs of 6.8 x 10^{-4} Ω cm^2.

INTRODUCTION

Silicon carbide is being intensively pursued around the world for high power and high temperature devices because of its wide band gap and other intrinsic properties such as its high bond strength, high electric field strength, and high saturation electron velocity. However, for reliable high temperature devices, electrical contacts that are chemically and microstructurally stable and that have low specific contact resistivities (SCRs) must be developed. While many studies have reported the electrical, chemical, and/or microstructural characteristics of metal-SiC contacts after annealing (typically at temperatures between 400 and 1200 °C), few studies have reported the electrical characteristics of the contacts at elevated operating temperatures [1-3].

In this study both the effects of long term annealing and elevated operating temperatures on TaC/SiC, Au/TaC/SiC, Pt/TaC/SiC, and W/WC/TaC/SiC on n-type and Pt/Os/SiC and Os/SiC on p-type SiC were investigated. The current-voltage characteristics of the contacts were measured in air at temperatures to 400 °C and after long (~150 h) anneals at 400 °C in vacuum (~10^{-5} torr) or Ar.

EXPERIMENTAL PROCEDURE

Nitrogen-doped n-type (2.3 x 10^{19} or 7.8 x 10^{18} cm^{-3}) and Al-doped p-type (1.1 x 10^{19} or 7.0 x 10^{18} cm^{-3}) homoepitaxial layers on 6H-SiC (0001) wafers were grown by Cree Research, Inc.

The substrates were cleaned using acetone and methanol. Thermally grown oxide layers were then removed with 10% HF for 10 min. Samples were rinsed in DI water and dried with N_2.

The substrates were placed in a D.C. magnetron sputtering system with a base pressure of < 3.0×10^{-7} torr and thermally desorbed at 550°C for 10 min. The TaC films were deposited to a thickness of 1600–3200 Å onto the substrates, which were heated to 200 °C. Osmium films were deposited to a thickness of 1000 Å on unheated substrates.

Each sample was photolithographically patterned using two masks consisting of 300 x 50 μm rectangular transmission line model (TLM) pads and rectangular mesa structures. The spacings between rectangular pads were 5, 10, 20, 30 and 50 μm, respectively. The associated processing steps are described elsewhere[4].

The process anneals to produce the ohmic contacts were performed in vacuum (< 5×10^{-6} torr) at 800°C for 1 hour, 900 °C for 15 min., 1000°C for 15 min. or 1075°C for 15 min. Long term anneals at 400 °C were performed in vacuum (~10^{-5} torr) or in Ar. The I-V measurements were performed in air at temperatures between 25 and 400 °C in 100 °C increments. The samples were held at each temperature for an average time of 20 min.

RESULTS

[1] TaC/SiC

The TaC became ohmic after annealing at 800°C for 1 hour. The average SCR for the annealed contacts was 1.08×10^{-4} Ω cm^2 at room temperature. The SCR decreased to a minimum value of 2.1×10^{-5} Ω cm^2 after annealing at 1000 °C for 15 min. All of the remaining contacts discussed in this paper were therefore annealed at 1000 °C for 15 min. to form the ohmic contact.

Increasing the measurement temperature resulted in substantial degradation of the TaC/SiC contacts. This result is attributed to oxidation of the contacts, as correlated with the O level detected from secondary ion mass spectrometry (SIMS) analyses. The O concentration increased by a factor of more than two within the contact layer after heating in air at 400 °C (shown in Ref [4]). The data also indicates growth of an oxide layer at the surface of the contacts, which would increase their resistivity and interfere with the I-V measurements.

Because of the oxidation effects, Au and Pt layers were deposited on the TaC/contacts to serve as protective layers. The SCRs for these samples as a function of measurement temperature are listed in Table 1. The contact resistivity for the Au/TaC/SiC sample decreased to 5.31×10^{-7} Ω cm^2 at 200 °C. However, heating to 300 °C resulted in an increase in the resistivity, while heating to 400 °C caused irreversible degradation of the contacts. It was found that the Au/TaC/SiC samples showed good stability if the measurement temperature was kept between R.T. and 200 °C. In contrast, Pt overlayers resulted in decreasing SCR values to 400 °C. In addition, these contacts showed good reversibility when remeasured at R.T. The decrease in SCR with temperature is attributed to a thermal enhancement of charge carriers across the interface, while the increase (for Au/TaC/SiC) may be associated with a discontinuous overlayer, reaction between the layers, and/or oxidation of the TaC layer via one of the former mechanisms. The possible mechanisms will be subjects of future investigations.

The contacts were also subjected to relatively long anneals at the maximum measurement temperature (400 °C). Table 1 shows that annealing the TaC/SiC contacts for 24–48 h in ultra high purity Ar resulted in an increase in the SCR by nearly a factor of 2. The significantly smaller increase in SCR displayed by TaC/SiC contacts annealed in ~10^{-5} torr vacuum indicates that residual O present during the Ar anneal is associated with the calculated increase in resistivity. To separate the effects of oxidation from the effects of reactions between the material layers, the Au/TaC/SiC and Pt/TaC/SiC samples were annealed in vacuum. The SCR values showed very little increase after annealing for 48 hrs.

	ρ_c vs measurement temperature			ρ_c after annealing at 400 °C (in Ar or vacuum as indicated)				
Sample	Temp. (°C)	Au/TaC/SiC	Pt/TaC/SiC	Time (hour)	TaC/SiC in Ar	TaC/SiC in vac	Au/TaC/SiC in vac.	Pt/TaC/SiC in vac.
ρ_c (Ω cm^2)	R.T.	1.37×10^{-6}	7.38×10^{-6}	0	2.08×10^{-6}	2.08×10^{-6}	1.36×10^{-6}	7.38×10^{-6}
	100	6.95×10^{-7}	2.00×10^{-6}	24	2.32×10^{-6}	2.26×10^{-6}	1.57×10^{-6}	7.81×10^{-6}
	200	5.31×10^{-7}	9.52×10^{-7}	48	3.91×10^{-6}	2.31×10^{-6}	1.60×10^{-6}	8.01×10^{-6}
	300	8.13×10^{-7}	8.45×10^{-7}					
	400	N/A	7.50×10^{-7}					

Table I. Summary of specific contact resistivities (ρ_c) calculated for TaC (3200 Å) / SiC, Au (500 Å) / TaC (3200 Å) / SiC, and Pt (100 Å) / TaC (3200 Å) / SiC. All contacts were annealed at 1000 °C for 15 min. to form the ohmic contacts. The doping concentration in the substrate epilayers was 2×10^{19} cm^{-3}.

The Au/TaC/SiC and Pt/TaC/SiC along with W/WC/TaC/SiC contact schemes on SiC epilayers with lower doping concentrations (7.8×10^{18}cm^{-3}) were subjected to longer anneals (to 144 hrs) at 400 °C. While the Au/TaC and Pt/TaC contacts showed slight increases in SCR with annealing time, the W/WC/TaC contacts yielded a decrease in SCR after annealing for 48 hrs and remained stable after 144 hrs (Fig. 1). The increasing resistivity values of the former contacts may again be associated with slow oxidation of the contacts from the small but finite concentration of O_2 in the vacuum furnace. The reason for the decrease in SCR of the W/WC/TaC contacts is under investigation.

To determine the stability of the TaC/SiC interface, samples were prepared for cross-sectional TEM. The TEM image in Fig. 2 shows that the interface remained smooth after annealing to form the ohmic contact (1000 °C for 15 min.) and that no large-scale reaction occurred. Preliminary investigations of this interface by high resolution TEM also indicate the absence of chemical reactions.

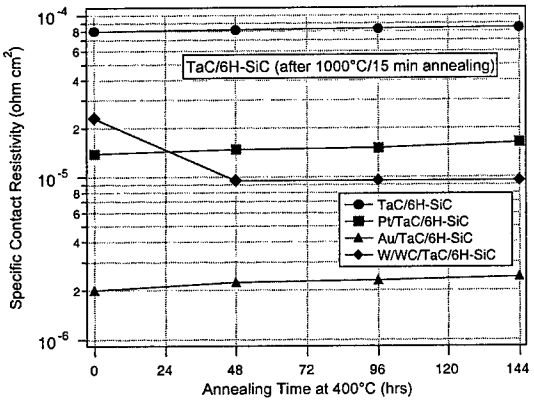

Figure 1. Specific contact resistivity vs. annealing time at 400 °C in vacuum for (1600 Å) TaC / SiC, (100 Å) Pt / (1600 Å) TaC / SiC, and (100 Å) Au / (1600 Å) TaC / SiC. The doping concentration in the n-type SiC epilayer was 7.8×10^{18} cm^{-3}.

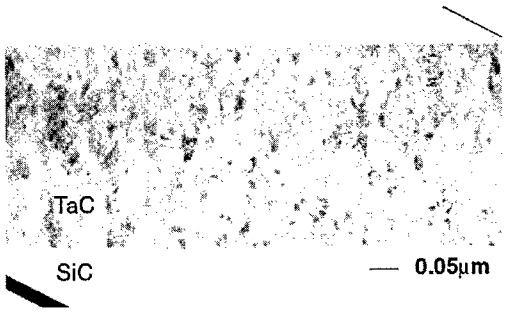

Figure 2. Cross-sectional TEM image of TaC/SiC annealed at 1000 °C for 15 min.

[2] Os/TaC

The Os contacts became ohmic after annealing at 1020°C for 1 hour. A subsequent anneal (1020°C for 15min) resulted in improved ohmic behavior. The average SCR for the contacts was 6.8 x 10^{-4} Ω cm^2 at room temperature. Platinum overlayers were employed to prevent the formation of a volatile Os oxide at elevated temperatures and to achieve better thermal stability.

The TEM images in Fig. 3 and 4 show increasingly rough interfaces with annealing time and give evidence for the formation of new phases through the contact layer. Composition profiles from secondary ion mass spectrometry (SIMS) of annealed Os/SiC contacts revealed that Si and C diffused through the Os layer to form a Si- and C-rich surface layer. The diffusion of Si and C from the SiC to form silicide and C phases is believed to be associated with the observed ohmic behavior.

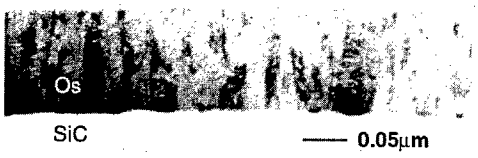

Figure 3. Cross-sectional TEM image of as-deposited Os/SiC.

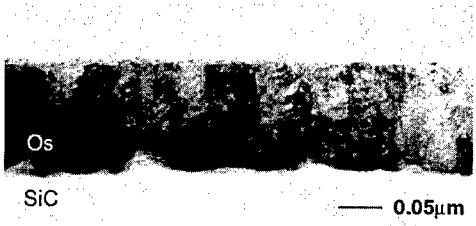

Figure 4. Cross-sectional TEM image of Os/SiC annealed at 1020 °C for 1 hour.

CONCLUSIONS

Contacts with overlayers showed lower SCRs and improved thermal stability in comparison to contacts without overlayers. The TaC/SiC interface displayed little or no reaction after annealing, while the Os/SiC interface displayed significant reaction through the film. In addition to the tendency for reactions between the layers, O was shown to be associated with degradation of the contacts. The present research indicates that interfacial stability between the contact layer and the SiC is but one step in the process for fabricating thermally stable device structures.

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Improved Ohmic Contacts to 6H-SiC by Pulsed Laser Processing

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Keywords: Aluminum, Excimer Laser, Laser Processing, Ohmic Contacts, SiC, Titanium, Tungsten

Abstract. Ohmic contacts to 6H-SiC have been improved in several points such as contact resistivity, surface morphology, depth profiles, and process temperature. Both W/Ti contacts for n-type and Al/Ti contacts for p-type 6H-SiC have been fabricated with excimer pulsed laser irradiation to the metal-deposited substrates at room temperature. Properties of laser-processed contact have exceeded those of the ordinary annealed contacts. Very thin ohmic contact layers with smooth surface morphology have been obtained by this technology.

1. Introduction

Fabrication techniques of low resistive ohmic contact to SiC have been key technologies to realize low-loss SiC power and high frequency devices. Usually, ohmic contacts are made by annealing metal-deposited SiC substrates at high temperature, 700~1000℃ [1]. The contact fabrication method of this kind, however, contains several problems to be solved. For instance, an inter-mixing of metal materials with substrate components Si and C is a serious example, because this resulted in an extensive reaction depth and the deterioration of the surface morphology. In order to avoid this difficulty, we have proposed a new contact fabrication method, a pulsed laser deposition and doping (PLD) process, and succeeded to produce a thin ohmic contact layer with smooth and flat surface, which is essential for maintaining uniform current density [2,3]. In this paper are presented more improved ohmic contact properties on n- and p-type 6H-SiC such as contact resistivity, surface morphology, and depth profiles of contact layers. The contact resistivity was estimated using the linear transmission line method (TLM) [4].

2. Experimental

Samples used in the present experiment are n- and p-type bulk 6H-SiC with net donor and acceptor concentration of $1.5 \times 10^{18} cm^{-3}$, respectively. All the surfaces are (0001) Si face and 3.5° off axis. The samples were degreased in organic solvents and rinsed in deionized water. An oxide of about 30 nm thick was grown in wet oxygen at 1000°C for 30 min and then removed by etching in 10% HF solution. These procedures were repeated twice followed by rinsing in deionized water. Prior to metal deposition the samples were dipped in boiling deionized water to prepare fresh and pinning-controlled SiC surfaces [5].

The contact metal materials consist of double layers of W and Ti for n-type, and Al and Ti for p-type samples. The first thin Ti layer and subsequently the 2nd layer of W (n-type) or Al (p-type) were deposited on the substrate. W-films 10~20 nm thick were deposited with KrF excimer laser ablation from a W-metal pellet in a vacuum of 2×10^{-6} Torr. Typical deposition rate was 0.1 nm/s. The metal-deposited surfaces were irradiated with a KrF excimer pulsed laser (pulse width 20 ns) in a vacuum of $0.5 \sim 2 \times 10^{-6}$ Torr. The properties of contact layers were characterized using current-voltage (I-V) measurements, secondary ion mass spectroscopy (SIMS), and X-ray photoelectron spectroscopy (XPS). In case of I-V measurements of W/Ti contacts, Au was finally deposited on the contacts to prevent from oxidization.

3. Results and discussion

3.1 W/Ti contact

I-V characteristics were measured for several contacts with varying Ti layer thickness (10~30 nm) and constant W layer thickness (approximately 10±5 nm). In general, a larger energy density of the excimer laser

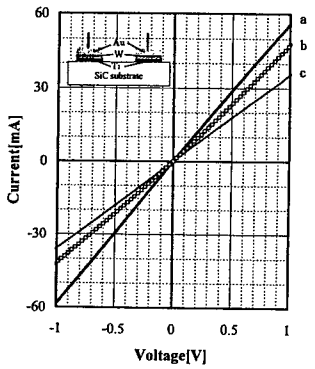

Fig.1 I-V characteristics of PLD-processed W/Ti contacts with constant W layer thickness 10nm;(a) t_{Ti}=30nm, E=2.0J/cm^2, (b) t_{Ti}= 10nm, E=1.5J/cm^2, (c) after annealing of contact (b) at 1000°C, 500s in Ar.

Fig.2 SEM photographs of surfaces of; (a) contact (a), and (b) contact (b) in Fig.1, respectively, and (c) an annealed contact for a reference (at 1000°C, 5min in Ar).

is necessary for obtaining the ohmic behavior, as the increase in the deposited film thickness. However, the increase in the energy density leads to deterioration of the surface morphology. An optimum energy density for a given film thickness should be investigated to realize an ohmic contact with a smooth surface. Hereafter we refer to film thickness and roughness (a peak-to-valley value) as those measured with a profilometer. Fig.1 (a) is I-V characteristics of a contact with W/Ti film 10/30 nm thick irradiated with an energy density of the laser pulse 2.0J/cm^2 (200 shots). The surface roughness is about 100 nm in this case. When the Ti film thickness decreased to approximately 10 nm (±5 nm), 200 shots of laser pulses with 1.5 J/cm^2 are energetically enough to produce an ohmic contact (Fig.1 (b)). It is noticed that reducing both of a Ti film thickness and the laser energy density is effective for a smooth surface morphology of contacts. The roughness of the contact (b) is approximately 10 nm, which is almost the same as that just after deposition.

The scanning electron microscopy (SEM) photographs of the contact (a) and (b) are shown in Fig.2 (a) and (b), respectively, together with a reference one of an annealed contact at 1000°C for 5 min in Ar atmosphere. In Fig.2 (a) small island structures are presented, which seemed to be characteristic Ti compounds (oxide and carbide) formed during a PLD process [6]. In contrast, Fig.2 (b) shows smooth surface morphology. A structure in the figure is due to a scratch with a current probe. It has now been clear that fabrication of an ohmic contact with a smooth surface is successful with a proposed PLD process under proper conditions. Fig.2 (c) shows typical surface morphology observed in annealed contacts containing Ti, the roughness of which is estimated to be about 500 nm. The present annealed contact failed to pass current.

The contact resistivity of the contacts (a) and (b) in Fig.1 was evaluated with the TLM measurements to be 4.3x10^{-5} and 6.7x10^{-5} Ωcm^2, respectively, which is comparable to or smaller than that of Ni contacts to n-type 6H-SiC with a similar net donor concentration [1]. In Fig.1 (c) is also shown an effect of the annealing on the I-V characteristics of the PLD-processed contact (b). The contact was annealed with an Au film capped to prevent from oxidization at 1000°C for 500 s in Ar. The surface roughness increased to 500 nm, but the contact resistivity remained almost unchanged 6.4x10^{-5} Ωcm^2. This result indicates that PLD-processed W/Ti contacts are thermally resistant, although a more reliable thermal test is required for real devices. Since a PLD-processed Ti contact (similarly processed as the contact (b) without W) loses an ohmic property by annealing at 1000°C for 500s in Ar gas, W is essential for the thermal stability of contacts.

SIMS depth profiles of W and Ti of a PLD-processed contact, the same one as that shown in Fig.1 (b), and of as-deposited W/Ti contacts for a reference are shown in Fig.3 (a) and (b), respectively. It is clear that little mixing between W/Ti and the substrate occurs due to PLD process, and a sharp interface is established. Irradiation of 200 shots of 1.5J/cm^2 laser pulses seems to induce a little mixing between W and Ti. Component Si and C (mainly SiC assigned by XPS analysis) observed throughout the metal layer in Fig.3 (a) and (b) probably come from pin holes in thin W and Ti films.

Fig.4 shows the results of XPS analysis on a PLD-processed W/Ti contact with total thickness of about 30 nm. Fig.4 (c) shows depth profiles of calibrated concentration of each component. In Ti rich region

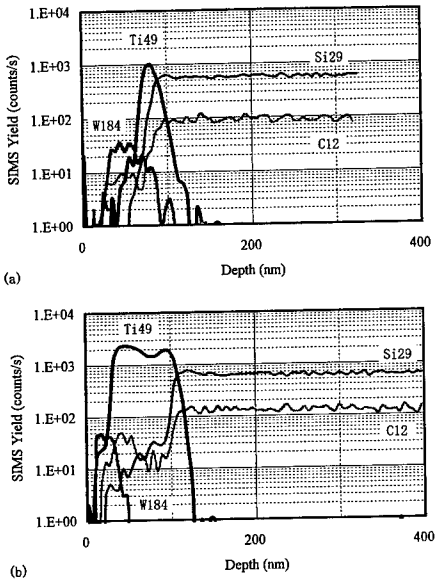

Fig.3 SIMS depth profiles of W, Ti, Si and C in W/Ti contacts; (a) PLD-processed (contact (b) in Fig.1) and (b) as deposited.

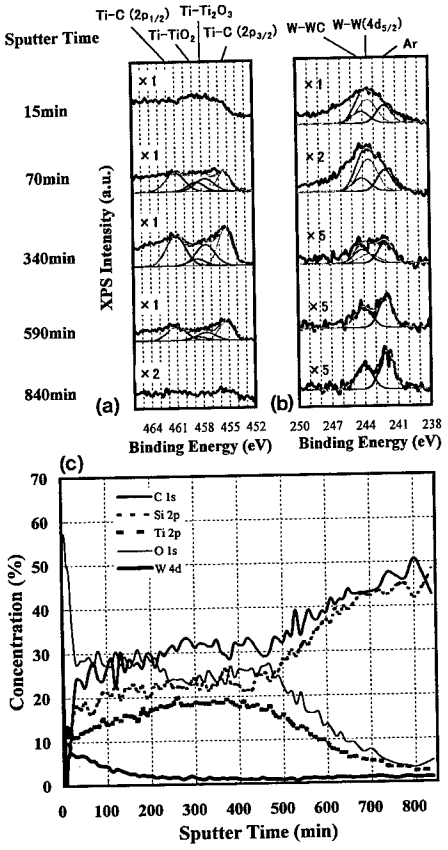

Fig.4 XPS depth profiles of Ti, W, O, Si and C, and Ti2p and W4d spectra as a function of the sputter time in a PLD-processed W/Ti contact.

(sputter time from 70 to 590 min), TiC and Ti oxides are dominant components. Whereas, metallic W dominates in the surface and the interface region between W and Ti (15 to 340 min), and there is a small component of WC throughout the contact layer to the interface with the substrate. A reducing property of Ti, which is effective for deoxidization at the interface between Ti and the substrate, seems to promote forming TiC and WC at the interface. Both of carbides TiC and WC are probably responsible for the ohmic characteristics of the W/Ti contact to n-type 6H-SiC.

3.2 Al/Ti contact

I-V characteristics of the PLD-processed Al/Ti contacts to p-type 6H-SiC, varying Ti film thickness from 10±5 to 30±5 nm against constant Al film thickness (60 nm), are shown in Fig.5. Laser pulses (1.5 J/cm^2, 100 shots) were incident to the top layer of an Al film. The contact (a) (a nominal Ti film thickness t_{Ti}=30 nm) could not pass a current at all. Decreasing t_{Ti} to 10 nm, a good ohmic property was obtained (contact (c)). As shown by a SEM photograph in Fig.6 (a), the PLD process could attain a smooth surface with a peak-to-valley roughness of 10 nm. Fig.5 (d) shows I-V characteristics of a reference Al/Ti contact (Al layer thickness t_{Al}=250 nm and t_{Ti}=30 nm) annealed in Ar gas at 1000°C for 5 min. A SEM photograph of Fig.6 (b) shows the surface morphology of this contact, the roughness of which is estimated to be 50 nm. The contact resistivity of contact (b), (c) and (d) was evaluated to be 2.2×10^{-3}, 1.0×10^{-3} and 7.4×10^{-4} Ωcm^2, respectively, which is comparable to the annealed Al/Ti contacts [1]. Clearly the surface morphology of the PLD-processed contacts is superior to that of annealed contacts. Since a PLD-Ti contact (without Al layer) shows a non-ohmic behavior, and a PLD-Al contact (without Ti layer) shows an ohmic behavior, the ohmic property of the Al/Ti contact should be maintained by the Al layer contacted with the substrate. A highly p-type layer doped with Al is probably responsible for the ohmic property.

Fig.7 shows the SIMS atomic depth profiles of Al, Ti, Si and C in the Al/Ti/p-SiC system; (a) PLD processed, the contact (c) in Fig.5, (b) annealed, the contact (d) in Fig.5, and (c) as deposited contact,

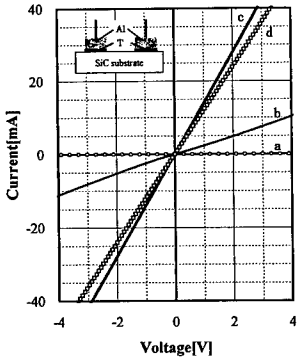

Fig.5 I-V characteristics of PLD-processed Al/Ti contacts with constant Al thickness (60nm); (a) t_{Ti}=30nm, (b) t_{Ti}=15nm, (c) t_{Ti}=10nm. (d) annealed contact for a reference.

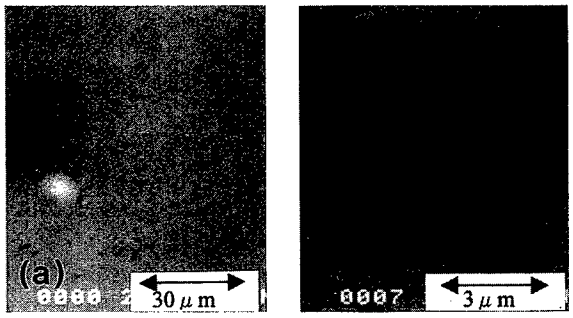

Fig.6 SEM photographs of surfaces of; (a) contact (c) and (b) contact (d) in Fig.5, respectively.

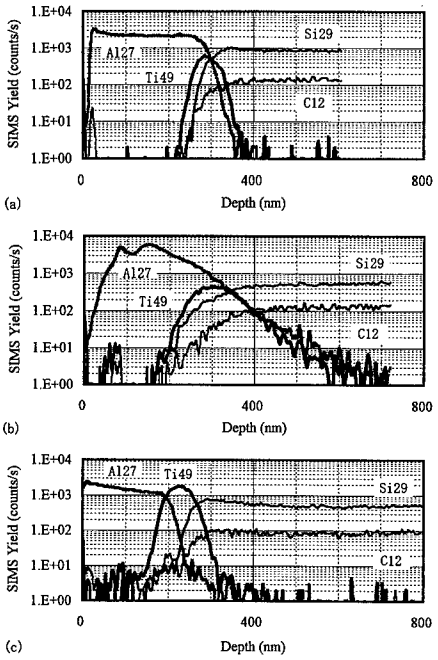

Fig. 7 SIMS depth profiles of Al, Ti, Si and C in Al/Ti contacts; (a) PLD-processed, (b) annealed (1000°C, 5min in Ar) and (c) as deposited.

respectively. Comparing Fig.7 (a) with (c), the PLD process moved the Al layer to the interface region with SiC substrate, and induced mixture of Al and Ti. However, the mixing of Ti layer with the substrate scarcely occurs, and the sharp interface is established as well as the W/Ti contact. In contrast, the annealed contact (Fig.7 (b)) has a deep mixing profile, reflecting the rough surface induced with high temperature annealing (Fig.6 (b)). An intermediate layer of Ti between the Al layer and the substrate increases the adhesion of the Al layer. XPS analysis revealed that the Al layer consisted of mainly metallic Al and a small component of Al oxides, and TiC was formed in the Ti-rich region adjacent to the substrate. The catalytic function of Ti in the interface region seems to help doping of Al reproducibly by PLD process.

4. Conclusion

The PLD process is successful in the following aspects of the contacts to 6H-SiC; (1) to fabricate ohmic contacts with as low contact resistivity as annealed contacts, (2) to reduce interfacial mixture of metals with the substrate component Si and C, (3) to produce a thin contact layer with smooth and flat surface to maintain a uniform current density.

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Al/Si Ohmic Contacts to p-type 4H-SiC for Power Devices

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Keywords: Annealing, Contact Resistivity, Temperature Stability

Abstract

The formation of Al/Si/p-4H SiC ohmic contacts at temperatures as low as 750 °C is reported in this paper. The dependence of electrical properties and contact morphology have been investigated as a function of the annealing regime in the interval 600-700 °C. The lowest contact resistivity of $3.8x10^{-5}$ $\Omega.cm^2$ was obtained at 700 °C annealing, however the most reproducible results were in the low 10^{-4} $\Omega.cm^2$ range. It has been established that the predominate current transport mechanism in the Al/Si/SiC contacts is thermionic-field emission. Atomic force microscopy showed that the addition of Si to the contact layer improves its morphology, and the pitting of annealed Al is not observed. The contacts developed are stable during ageing at 500 °C and at operating temperatures up to 450 °C. After the contacts testing with current density of 10^3 A/cm^2 at temperatures up to 450 °C, their contact resistivity decreases slightly.

Introduction

The 4H polytype of SiC is preferred for device development because of its highest carrier mobility [1]. However, the high Schottky barrier at the metal/p-type 4H-SiC interface due to the high electron affinity (3.3 eV [2]) and wide bandgap (3.2 eV) of 4H-SiC makes it difficult to obtain low resistivity p-type ohmic contacts. Commonly, obtaining a low resistivity is associated with contact annealing at high temperatures (≥900 °C) which might cause changes and distortions of the device structure and contact layer. For that reason, the development of temperature-stable low resistivity-ohmic contacts to p-type SiC annealed at relatively low temperatures is of interest.

Regardless of the fact that during the past years contacts such as Mo, Ti, Ta and Co have been subjected to intense research, Al-based contact systems still belong to the most applicable ohmic contacts to p-type SiC. The Al/Si contact to p-type SiC is appropriate for device production because the solder commonly used in the semiconductor industry consists of an Al+Si alloy. The Al/Si system has not been sufficiently investigated with respect to the dependence of the ohmic properties on the formation regime and also to the thermostability of the contacts formed [3-5].

Experiment

Al/Si/SiC ohmic contacts have been formed on wafers with a 1 μm thick Al-doped epitaxial layer with carrier concentrations of $3x10^{19}$ cm^{-3} and $5x10^{19}$ cm^{-3}. The samples were cleaned in organic solvents and etched in a solution of nitric and hydrofluoric acids (HNO_3:HF:H_2O=1:1.5:30). Mesa etching was performed on the samples intended for electrical measurements and the contact

pads of the test structures were photolithographicaly formed. The samples were then etched in a 10% solution of hydrofluoric acid. Cleaning by an Ar plasma discharge was performed immediately before the metal deposition. The Si and Al layers with the total contact thickness of 150 nm were subsequently sputtered at base pressure of $2.6x10^{-3}$ torr. The excess metal was lifted ultrasonically in acetone to create the test structures. The annealing was carried out in a furnace with resistance heating at temperatures ranging from 600 to 700 °C.

I-V characteristics before and after annealing were measured to check for ohmic behaviour. The contact resistivity ρ_c was determined by the linear transmission-line model (TLM) method [6]. Measurements of I-V characteristics and contact resistivity were carried out on an automated system for measurements at room temperature as well as at temperatures up to 500 °C.

The morphology of the as-deposited and annealed contacts was studied by atomic force microscopy (AFM) on a Nanoscope IIIa microscope using tapping mode.

The temperature stability of the ohmic contacts was investigated by an ageing, temperature-dependence and temperature-current test. The ageing test was performed in N_2 at 500 °C for 100 hours. The temperature-dependence test was carried out in air from room temperature to 450 °C in increments of 50 °C. The temperature was maintained constant with an accuracy ± 1.5 °C during each measurement. With the temperature-current test a current density of 10^3 A/cm^2 was passed for a fixed time through the contacts during the heating. This test was also performed in air up to 450 °C.

Results and discussion

As-deposited Al/Si contacts had I-V characteristics typical of a Schottky barrier which indicates that they form a Schottky contact to p-type SiC. Annealing of the contacts in the interval 600-700 °C produced ohmic properties evident by the linear character of their I-V characteristics.

The experiments showed that anneal of only at 600 °C produced high resistivity ohmic contacts. A strong dependence of contact resistivity on the formation conditions and the substrate doping level was observed with Al/Si/SiC contacts (Fig. 1).

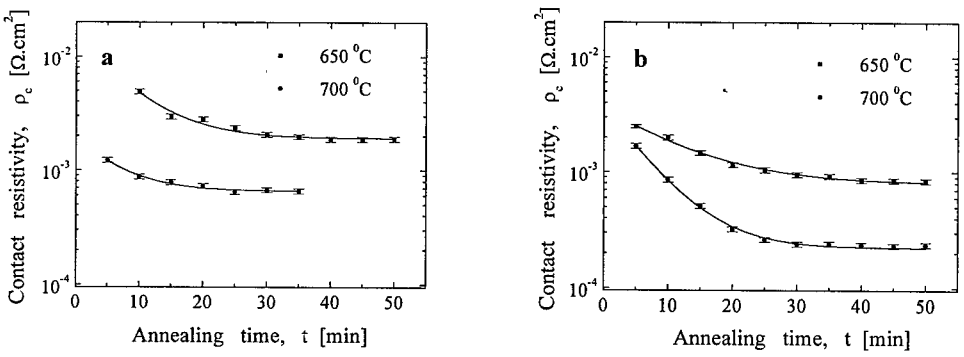

Fig. 1 Dependence of the Al/Si/SiC contact resistivity on the annealing regime with different doping levels of the substrate: (a) $N_A = 3x10^{19}$ cm^{-3}; (b) $N_A = 5x10^{19}$ cm^{-3}.

Obviously, the ohmic properties are formed already at the beginning of the annealing process, but the contact resistivity has relatively high values: $(1\text{-}5)x10^{-3}$ Ω.cm^2. With prolongation of the annealing time, the resistivity decreased. The experiments have shown that within the temperature range investigated Al/Si/SiC contacts with a lowest resistivity of $3.8x10^{-5}$ Ω.cm^2 are formed at an annealing temperature of 700 °C. The reproducibility of the experiments on ohmic contacts formation has been checked by a method based on statistical verification of the hypothesis for reproducibility, where the criterion of Cochran G is compared with its value G_p obtained in the each

experiment performed [7]. The results showed the reproducible contact resistivity of $2.3x10^{-4}$ $\Omega.cm^2$ has been obtained at 700°C annealing temperature (with a probability P=95). Additional annealing at the same temperature did not change the contact resistivity further. Hence, during the time for reaching a minimum contact resistivity, changes in the contact structure occur and a stable interface configuration is formed. As the electric characteristics of the Al/Si/SiC contact exhibit no changes with further prolongation of the annealing time, it could be suggested that the contact layer structure does not change. During the experiments performed, decreasing of the contact resistivity with increasing doping concentration was observed.

The current transport mechanism through the contact is mainly determined by the doping level of the substrate on which it is formed [8]. The doping concentration of $(3\text{-}5)x10^{19}$ cm^{-3} gives a ratio for $kT/E_{oo} \cong 1$, permitting the assumption that the predominating current transport mechanism in Al/Si/SiC ohmic contacts is thermionic-field emission.

The morphology of as-deposited and annealed at 700 °C contacts studied by AFM is presented in figure 2. Both as-deposited and annealed contact layers follow the steps on the epitaxial layer surface of the substrate. This is also evident by the light and dark bands which repeat with a period of 630 nm in the two-dimensional AFM image of the surface.

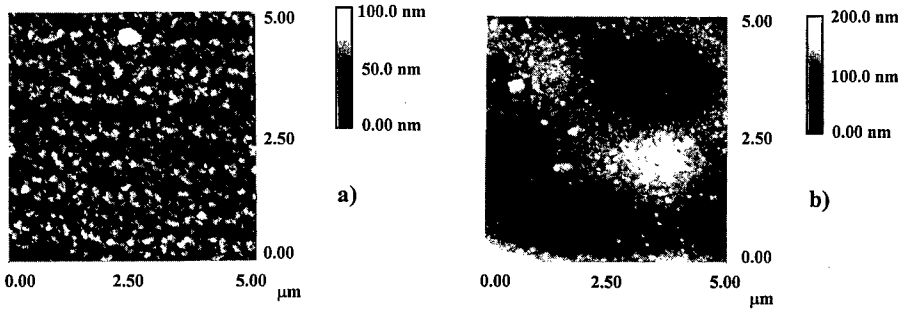

Fig. 2 A two-dimensional AFM image of the surface of (a) as-deposited and (b) annealed (700°C) Al/Si/SiC contact.

The as-deposited contact has a granular structure, with an average feature size of 330 nm. The root-mean-square of the surface roughness is 13 nm. After annealing the Al/Si contact at 700 °C, the substrate surface is uniformly covered by the contact layer and semi-spherical "hills" are formed at some sites. The root-mean-square roughness of the annealed contact increased to 35 nm. The pits characteristic of annealed Al/SiC contacts [3] were not observed, which means that the addition of Si to the contact layer has improved its morphology.

The temperature stability was investigated on an Al/Si/SiC contact formed at 700 °C. The results from the ageing test are presented in figure 3. A contact resistivity of $2.4x10^{-4}$ $\Omega.cm^2$ was measured before the beginning of the test. During the entire ageing time, this value showed no substantial change: a criterion for stable contacts. This result can be ascribed to formation of a stable Al/Si/SiC interface during annealing at 700 °C. As a result, prolonged heating at 500 °C does not lead to changes in contact composition and element distribution on which the ohmic properties depend, and consequently the contact resistivity remains constant.

The behaviour of the Al/Si/SiC contact at operating temperatures up to 450 °C (Fig. 4) has been studied by the temperature dependence test. In a similar manner to the ageing test, no changes in contact resistivity were observed at the temperatures investigated. It should be noted that this stability has been established in experiments carried out in air on contacts without a protective layer.

A temperature-current test has been also performed at temperatures ranging from 25 to 450 °C. A current density of 10^3 A/cm^2 was passed through the contacts for 1 hour at each temperature in the interval investigated (Fig. 4). The contact resistivity did not change up to 150 °C. With higher temperatures, the resistivity smoothly decreased and at 450 °C it had a value of 8.9×10^{-5} Ω.cm^2.

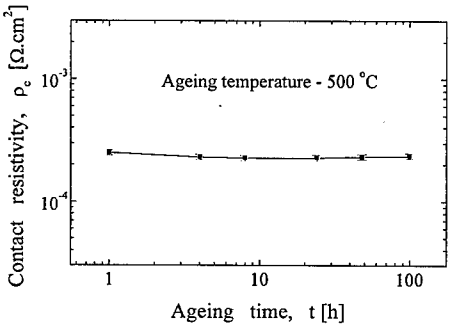

Fig. 3 Resistivity values of the Al/Si/SiC contact at an ageing temperature of 500 °C.

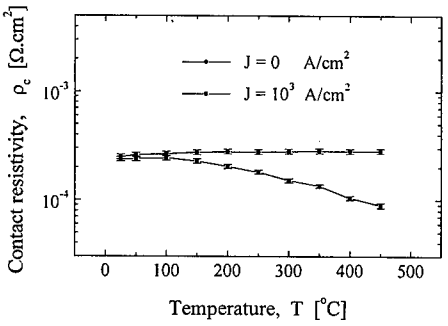

Fig. 4 Resistivity values of the Al/Si/SiC contact at different operating temperatures.

Conclusion

The results of this work show that Al/Si/SiC ohmic contacts to p-type 4H-SiC are formed at temperatures below 750 °C. The morphology of the annealed contacts has been improved by an addition of Si to the contact layer. The contact resistivity depends strongly on the annealing conditions and substrate doping concentration. A reproducible contact resistivity value of 2.3×10^{-4} Ω.cm^2 has been achieved. The lowest contact resistivity of 3.8×10^{-5} Ω.cm^2 has been obtained with insufficient reproducibility.

The Al/Si/SiC contacts formed at an annealing temperature of 700 °C are stable when subjected to the effect of a temperature at 500 °C for a long time or under operating conditions up to 450 °C in air. This temperature stability of the Al/Si/SiC contacts presents a possibility for power device applications.

Acknowledgment

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Searching for Device Processing Compatible Ohmic Contacts to Implanted p-type 4H-SiC

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Keywords: Aluminum, Ohmic Contacts, Palladium, Titanium

ABSTRACT: To search for device processing compatible ohmic contacts to mid-$10^{20}cm^{-3}$ Al+C co-implanted p-type 4H-SiC, Ti and layered Ti, Al and layered Al, Pd and layered Pd metal systems have been studied. Aluminum based contacts give the lowest specific contact resistance with a median value of $4.7x10^{-5}\Omega\cdot cm^2$. However, Al requires a high annealing temperature and is easily oxidized, making it difficult to get a device processing compatible Al contact. Efforts have been made to see if any metal over-layer could be used to solve the problem and the results are reported. Titanium covered by W has high $10^{-4}\Omega\cdot cm^2$ specific contact resistance. When covered by Al, Ti/Al contact gives a better specific contact resistance of $1.4x10^{-4}\ \Omega\cdot cm^2$. But Al tends to get oxidized during annealing in a conventional annealing furnace. Palladium is attractive because of its low annealing temperature and high resistance to oxidation with a reasonably good specific contact resistance of high $10^{-5}\Omega\cdot cm^2$. Pd and layered Pd contacts may be further improved to provide device processing compatible ohmic contacts to p-type 4H-SiC.

INTRODUCTION

SiC is an excellent semiconductor for high power, high temperature devices because of its material properties such as wide bandgap, high breakdown field, high saturation velocity and high thermal conductivity. To utilize its properties in high power devices, formation of good ohmic contact with very low contact resistance can be a critical issue, especially for some types of devices such as IMPATT diodes. Although there are a lot of early papers reporting very good ohmic contact results for p-type 6H-SiC, only a handful reported low resistance contacts to p-type 4H-SiC [1,2,3]. To obtain a good ohmic contact on implanted and buried p-type 4H-SiC compatible with device fabrication with good surface morphology after high temperature annealing, we conducted a set of experiments on the formation of ohmic contacts to p-type 4H-SiC, including: (a) comparison between annealing in a conventional furnace with Ar forming gas and in vacuum with a base pressure in the range of 10^{-6} torr; (b) comparison between samples with and without thermal oxide in proximity with metal contact; (c) comparison among Ti contacts covered by different metals in search of a better surface morphology without contaminating Ti; (d) comparison among Al contacts covered by different metals in search of a better surface morphology without oxidizing Al; (e) comparison among Pd contacts covered by different metals in search of a better surface morphology with minimum surface roughness.

EXPERIMENT

Samples from Cree Research were Si-face 8°-off (0001) 4H-SiC with a thick n-type epilayer doped to $1.1x10^{16}cm^{-3}$. Al-C co-implantation was performed after sample cleaning to obtain a buried p-type layer. The implantation was made to form a buried box profile of 0.1 μm to 0.4 μm into n-type epilayer. Al concentration of mid-$10^{20}cm^{-3}$ after post implantation annealing (1550°C for 30 minutes in Ar) was confirmed by SIMS analysis. After implantation annealing, the samples were cleaned and

mesa etching was performed by inductively coupled plasma (ICP). Then thermal sacrificial oxidation was done at 1100°C for 30 minutes, followed by 5.5 hr to 7 hr thermal passivation oxide. Oxide window for contact metal deposition was formed by ICP etching or BHF wet etching. For comparison purpose, thermal passivation oxide was removed completely by BHF for samples without oxide between patterns. Right before loading into vacuum chamber for contact metal deposition, samples were subjected to ICP cleaning or BHF cleaning for 1 min. Then, linear transmission line model (TLM) patterns were defined either by lift off, wet etching or ICP etching depending on the metal used. The spacing between contact pads are: 2, 4, 6, 8, 10, 15, 20μm. Different annealing conditions have been used and the median values of specific contact resistance are summarized in Table 1, Table 2 and Table 3 for Ti, Al, and Pd based contacts, respectively. Specific contact resistance was determined from the I-V slope at zero bias, which may overestimate the specific contact resistance in case of slightly curved current-voltage characteristics.

RESULTS AND DISCUSSION

1. Ti and layered Ti contacts

Results for Ti based contacts are summarized in Table1. Because Ti is very absorbing, different metal over-layers have been utilized to cover up Ti contacts.

Table 1. Summary of Ti based Ohmic Contacts to p-type 4H-SiC

Layered Contact metal \ Contact annealing condition		950°C 5 min in Ar forming Gas ($\Omega\cdot cm^2$)	1050°C 5min in Ar forming gas ($\Omega\cdot cm^2$)	800°C in Vacuum ($\Omega\cdot cm^2$)
Ti (200nm)	With oxide between patterns	N/A	3.7×10^{-3} (in N_2 forming gas)	N/A
Ti/Al (150nm/100nm)	Without oxide between patterns	1.0×10^{-3}	1.4×10^{-4}	4.3×10^{-4}
	With oxide between patterns	4.0×10^{-4}	Al spill over resulting in invalid data	7.1×10^{-4}
Ti/W (200nm/50nm)	With oxide between patterns	N/A	5.3×10^{-3}	7.7×10^{-4}
Ti/Mo (150nm/100nm)	With oxide between patterns	N/A	1.8×10^{-3}	1.5×10^{-2}

From Table 1, we can see that Ti covered by Al contact gives low $10^{-4}\Omega\cdot cm^2$ specific contact resistance when annealed at 1050°C and without oxide between patterns. Because Al can easily be oxidized or spill over to device passivation oxide, we also used W and Mo to cover up Ti contact. It was found that W-covered Ti contact provided a median value of specific contact resistance of $7.7 \times 10^{-4}\Omega\cdot cm^2$ with an excellent surface morphology after annealing in vacuum at 800°C. Generally speaking, annealing in vacuum at 800°C indeed gave better surface morphology and resulted in less surface Al oxidization than samples annealed in forming gas in conventional furnace. Typical TLM I-V curves for Ti/W samples with proximity oxide annealed in conventional furnace and in vacuum are shown in Fig. 1. As can be seen, annealing in vacuum results in less curved I-V characteristics and lower specific contact resistance.

2. Al and layered Al ohmic contacts

Among the contact metals and layered structures studied in this project, pure Aluminum deposited by thermal evaporation achieved the lowest median specific contact resistance of $4.7 \times 10^{-5}\Omega\cdot cm^2$. This value is obtained when sample without oxide between patterns is annealed in Ar forming gas at 950°C for 5 min. However, Al gets oxidized and forms a surface insulating layer easily during high temperature annealing. High temperature annealing of pure Al often results in spiking into SiC layers, causing substantial anode leakage current if anode p layer is not thick enough. Al also leads

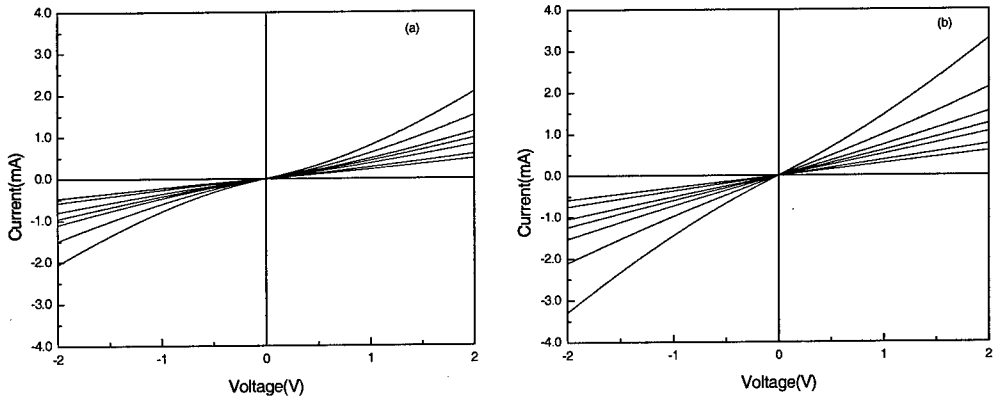

Fig. 1 I-V curves from Ti/W TLM patterns with proximity oxide annealed
(a) in conventional furnace with Ar forming gas at 1050°C, (b) in vacuum at 800°C

to spill over when proximity device passivation oxide is present during high temperature annealing. To search for a device processing compatible Al-based contact, surface insulating layer also needs to be eliminated. For this purpose, Al contacts covered by different metals were studied. The results are shown in Table 2. From Table 2, we can see that for samples annealed at 950°C, Al contact shows the lowest median value of specific contact resistance ρ_c= 4.7 x $10^{-5}\Omega\cdot cm^2$. For samples annealed at 1050°C, proximity oxide results in either invalid data or scattered data due to Al oxidation or Al spill-over onto oxide. Al contacts covered by Pd show 5.7 x $10^{-5}\Omega\cdot cm^2$ with reduced surface insulating layer problem. It should be pointed out, however, that a separate batch of Al/Pd contacts also annealed in pure N_2 did not yield ρ_c in the $10^{-5}\Omega\cdot cm^2$ range, medium value of 8.6 x$10^{-4}\Omega\cdot cm^2$ was found instead as shown in Table 2. The reason is not clear at present. W covering layer results in the most increase in the specific contact resistance.

Table 2. Summary of Al based Ohmic Contacts to p-type 4H-SiC

Layered Contact metal / Contact annealing condition		950°C 5 min in Ar forming Gas* ($\Omega\cdot cm^2$)	1050°C 5min in Ar forming gas* ($\Omega\cdot cm^2$)
Al (400nm)	With oxide between patterns	6.0x 10^{-5}	Scattered data due to Al oxidization
	Without oxide between patterns	6.1 x 10^{-5} 4.7 x 10^{-5}	N/A
Al /Pd (350nm/100nm)	With oxide between patterns	1.4x 10^{-4} (in Ar) 1.2x 10^{-4} (in Ar)	5.7x 10^{-5} (in N_2) 8.6x 10^{-4} (in N_2) 1.4x 10^{-4} (in Ar)
Al /W (350nm/100nm)	With oxide between patterns	N/A	1.5 x 10^{-3}
Al /Ti (350nm/100nm)	With oxide between patterns	N/A	3.3x 10^{-4} (in N_2 forming gas)
	Without oxide between patterns	N/A	8.0 x 10^{-4} (in N_2 forming gas)

*: Samples were annealed in Ar forming gas unless otherwise indicated. Multiple data were obtained from different batches.

3. Pd and layered Pd ohmic contacts

Palladium is highly resistive to oxidation with comparatively low annealing temperature. Pd contacts, however, have quite rough surface [1] after annealing. Thus, Pd contacts covered by three

different metals were studied, including Pd/W, Pd/Au and Pd/Ti. None of the three metals can yield smooth surface. The results are summarized in Table 3. Pd/Au sample gives the lowest median specific contact resistance of $\rho_c = 9.5 \times 10^{-5} \Omega \cdot cm^2$ when annealed in vacuum at 800°C. Also can be seen from Table 3 is that higher temperature annealing has no advantage over lower temperature annealing in terms of specific contact resistance.

Table 3. Summary of Pd based Ohmic Contacts to p-type 4H-SiC

Layered Contact metal \ Contact annealing condition		700°C 25 min N_2 ($\Omega \cdot cm^2$)	800°C 25 min ($\Omega \cdot cm^2$)		950°C 25 min in N_2 ($\Omega \cdot cm^2$)	1050°C 5 min in N_2 ($\Omega \cdot cm^2$)
			In N_2	vacuum		
Pd (110nm-200nm)	With oxide between patterns	N/A	3.8×10^{-4}	N/A	9.6×10^{-4}	7.8×10^{-4}
	Without oxide between patterns	4.0×10^{-4}	5.6×10^{-4}	2.6×10^{-4}	N/A	N/A
Pd/Au (150nm/100nm)	With oxide between patterns	2.6×10^{-4}	5.2×10^{-4}	1.4×10^{-4}	N/A	N/A
	Without oxide between patterns	2.3×10^{-4}	4.3×10^{-4}	9.5×10^{-5}	6.3×10^{-4}	1.1×10^{-3}
Pd/Ti (150nm/100nm)	With oxide between patterns	N/A	4.1×10^{-4}	N/A	5.2×10^{-4}	2.9×10^{-4}
	Without oxide between patterns	N/A	4.0×10^{-4}	N/A	1.3×10^{-3}	6.5×10^{-4}
Pd/W (150nm/100nm)	With oxide between patterns	N/A	4.3×10^{-4}	N/A	6.4×10^{-4}	1.0×10^{-3}

SUMMARY

To identify a device processing compatible ohmic contact to implanted p-type 4H-SiC, Ti and layered Ti, Al and layered Al, Pd and layered Pd metal systems have been studied. Al based contact gives the lowest specific contact resistance with a median value of $4.7 \times 10^{-5} \Omega \cdot cm^2$. However, Al oxidation during high temperature annealing presents a problem for device application. Al/Pd layered contacts yield reduced surface insulating layer with a median specific contact resistance of $5.7 \times 10^{-5} \Omega \cdot cm^2$. Titanium covered by W has a high $10^{-4} \Omega \cdot cm^2$ specific contact resistance. When covered by Al, Ti contacts give a better specific contact resistance of $1.4 \times 10^{-4} \Omega \cdot cm^2$ in comparison to W-covered Ti contacts, but surface insulating layer still presents a challenge. Pd requires a low annealing temperature and has a high resistance to oxidation with reasonably good specific contact resistances. Pd and layered Pd contacts can achieve specific contact resistance of high $10^{-5} \Omega \cdot cm^2$. Further investigation is needed to improve layered Pd contacts for device processing compatible ohmic contacts.

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Structural and Morphological Characterization of Al/Ti-based Ohmic Contacts on p-type 4H-SiC Annealed Under Various Conditions

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Keywords: 4H-SiC, Annealing, Depth Profiling, Ohmic Contacts, p-type

Abstract Structural and morphological characterization of Al/Ti-based contacts to p-type 4H-SiC was performed. Ohmic contacts with low specific contact resistance ($\sim 10^{-4}\Omega\cdot cm^2$) were obtained when cap layers have been used while were completely oxide-free when the annealing was performed under high vacuum conditions the contacts. It was found that use of Ti and Ni in the contact metallizations led to the formation of Ni_2Si/TiC duplex coatings at high temperature annealing.

Introduction

An open issue in the SiC-related technology is the formation of low specific contact resistance ohmic contacts to p-type SiC because of its large band gap and electron affinity. A number of metals and metal-like compositions were tested as contacts to p-doped SiC. The most popular ohmic contacts to p-type 4H-SiC material are the Al/Ti based metallizations [1, 2]. Indeed, the Al-Ti alloy is preferred instead of pure Al due to its higher melting point (1100°C for Al/Ti 90/10 wt.% [3] vs. 660°C for Al) thus, resulting in more thermally stable ohmic contacts. However, aluminum has a high driving force for oxidation and evaporation through the surface of the contact which can deteriorate the quality of the ohmic contact. Thus, it is necessary to use high vacuum conditions and/or protective cap layers to avoid contact oxidation during post deposition anneal. In addition, reproducibility problems occur when the SiC doping does not exceed 1×10^{19} cm^{-3} regardless of the metallization scheme [4].

In order to overcome the above problems in fabricating low resistivity ohmic contacts, we have combined and successfully applied three processing approaches. More precisely, vacuum annealing coupled with metal cap layers (Pd/Ni and Ni/Pt) resulted in non-oxidized contacts independent of the heating method (Rapid Thermal Annealing-RTA, resistive and inductive). In addition, a heavily doped p-type 4H-SiC layer with an aluminum concentration of approximately 1.5×10^{20} cm^{-3} was grown [5, 6] by low temperature Liquid Phase Epitaxy (LTLPE) prior to metal contact deposition. The above approach resulted in reproducible and of low specific contact resistance ($\approx 1\times10^{-4}$ $\Omega\cdot cm^2$) ohmic contacts [4,5]. In this work, we report on their structural and morphological characterization.

Experimental

To fabricate the contacts, the metals were deposited (1) on highly p-doped 4H-SiC epitaxial layers having Al concentration of $1.5\times10^{20}cm^{-3}$ measured by Secondary Ion Mass Spectroscopy (SIMS) (LTLPE layers) [5] and (2) on commercially available p-doped 4H-SiC epitaxial layers having acceptor concentration of $1\times10^{19}cm^{-3}$. The Circular Transmission Line Model (CTLM) pattern was defined by contact UV lithography. Deposition by e-gun evaporation was made at residual pressure $< 4\cdot10^{-7}$Torr.

The initial experiments with single Al/Ti metal contacts, annealed in neutral gas ambient, suffered from the creation of oxides and thus, three different metallizations were investigated as cap layers over the Al/Ti scheme in different annealing environments. The first group of metals (hereby denoted set A) were: Al (50nm) - Ti (100nm) - contact forming layers / Pd (10nm) - Ni (50nm) - covering layers. Ni has been chosen as top layer for subsequent use as a reactive ion etching mask as well as for its well known wetting properties at high temperature annealing while Pd has been incorporated for contact quality improvement and possible diffusion barrier. The second and third set of cap metals (set B and set C) were, Ni/Pt (30nm/100nm) and Pt/Ni (25nm/100nm) in order to avoid more effectively possible problems of oxide formation [4,5]. In the second set Ni was directly on the top of the Al/Ti to enhance its "wetting" effect and thus improve the contact resistance. Finally, in the third set Pt was chosen as diffusion barrier for Ti. Initial annealing experiments were performed by lamps in a commercial Rapid Thermal Annealing (RTA) chamber under flush of forming gas or Ar [4]. In addition to the RTA chamber, two vacuum annealing chambers were used. One (hereby denoted SV chamber) was a quartz chamber pumped by a rotary pump (simple vacuum) and the annealing was performed by inductive heating under a flow of 340 sccm of H_2 resulting in 500 Pa chamber pressure. The other chamber was a diffusion-pumped bell-jar vacuum system (hereby denoted HV chamber) where the annealing was performed by resistive heating in argon ambient at a pressure of 10^{-5} Torr [8]. Reproducible ohmic contacts were obtained only when the annealing was performed in the above two chambers. Therefore, a modification of the RTA chamber (hereby denoted VRTA) was performed permitting the pumping of the chamber down to 10^{-4} Torr during annealing. All the following results concerning RTA annealing correspond to this configuration. Details on the annealing procedure have been reported elsewhere [4, 5].

Auger Electron Spectroscopy (AES) and SIMS depth profiles were performed while X-Ray Diffraction (XRD) is used for phase analysis. Surface morphology was investigated by the Atomic Force Microscopy (AFM) method. The characterization was conducted on the same CTLM patterns which were used for specific contact resistance measurements. This fact resulted in a substantially reduced signal in the case of XRD analysis and increased the inaccuracy in the composition determination by AES and SIMS.

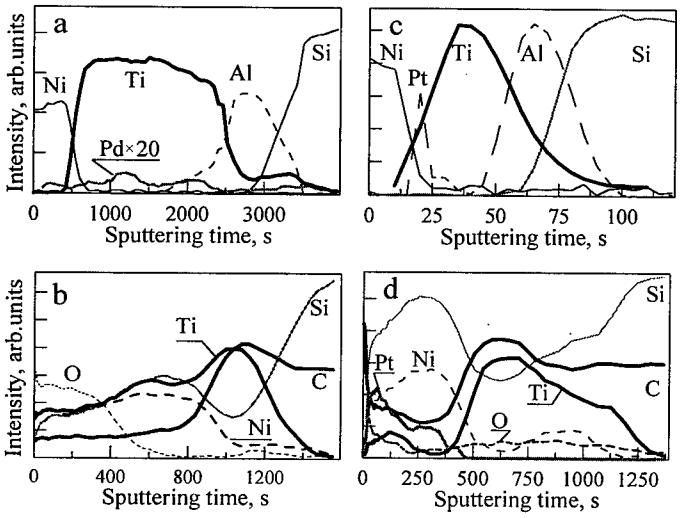

Fig. 1.Contact set A (a) before annealing and (b) annealed in SV chamber at 1150°C for 50 sec; and contact set C (c) before annealing and (d) after VRTA at 1000°C for 120 sec.

Results and discussion.

The first AES results for annealing in neutral gas environment showed evidence of oxidation from the surface to the interface with the SiC [5]. The samples annealed in SV chamber suffered from an oxidation of the top layers while the samples annealed in high vacuum (both in HV and VRTA chambers) were completely oxygen-free. Results are shown in Fig. 1. In the case of the set A, the palladium signal was of the order of the measurements' noise and detected only in the spectra obtained from the samples without annealing.

Its small thickness in combination with the fact that there is a strong interdiffusion between Pd and Ti even at 200°C [7] can explain the above result. Indeed, there is no diffusion between Pd and Ti only in the presence of oxygen [7], since oxygen diffuses through the Pd and forms titanium oxide at the Pd-Ti interface, which plays the role of the diffusion barrier. In our case, deposition of the metals was carried out in high vacuum conditions and therefore in the absence of oxygen. The Pt layer was detected by AES in as deposited samples (Fig. 1c) of the set C, and it is clearly seen that Pt also did not play the role of diffusion barrier at the temperatures of annealing. The AES profiles of annealed samples show also that Ni effectively prevents the oxidation of the metal contact and in any case there was not oxygen at the SiC/metal interface even for SV annealing (Fig, 1b). The AES spectra show the presence of two layers: (1) consisting of carbon and titanium only and detected at the metal-SiC interface; and (2) a layer by nickel and silicon and detected close to the contact's surface.

Al was not detected by the AES analysis of the annealed samples. We have to point out that the Al signal was monitored through its less intensive KLL peak at 1390 eV since the more intense LMM peak (64eV) is overlapped with the LMM peak (89eV) of Si. Nevertheless, we can definitely state that the content of Al in the metal contacts is very low. However, Al presence was clear in the SIMS profile (Fig.2) despite the fact that it was not possible to determine its concentration because the SIMS signal strongly depends on the atomic matrix and does not give the correct atomic concentration at very high concentrations; it is more sensitive and allows the detection of aluminum at low concentrations, down to ~10^{17}cm^{-3}. Another interesting result from the SIMS profile is that part of the Al diffused through Ti towards the surface while another part did not react with Ti but remained in its initial position. There is an evident correlation of the AES profiles shown in Fig. 1 with the SIMS profile concerning the Ti, Si, C and Ni interdiffusion. Both SIMS and AES profiles showed the presence of a TiC layer at the interface between SiC and the metallization.

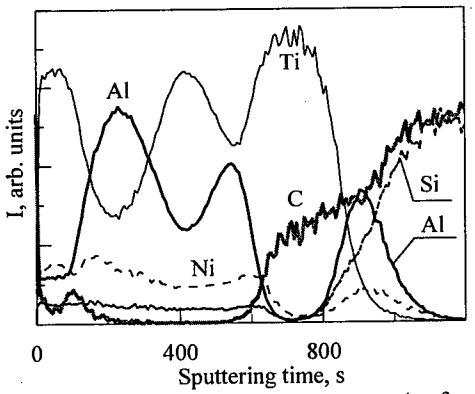

Fig 2. SIMS profile of the contact set A after anneal in SV for 50 sec at 1150°C.

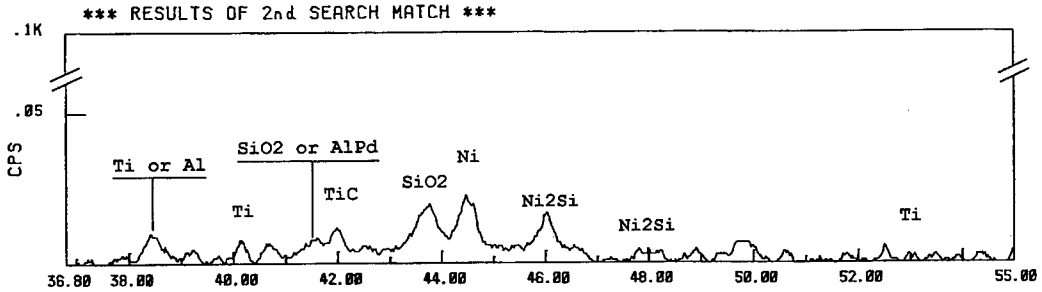

Fig. 3. X-ray phase analysis results for contact set A to LTLPE layer annealed in SV at 1150°C for 50 sec.

Phase analysis of an annealed contact layer was performed by x-ray diffraction. Results are shown in Fig. 3. The first remark is that the signals are very weak reflecting the partial coverage of the SiC surface by the CTLM patterns. The peaks corresponding to pure nickel, Ni_2Si, pure titanium and

AlPd or TiC were detected in the x-ray diffraction pattern. Comparison with AES and SIMS led us to conclude that this last peak corresponds to TiC.

In Fig. 4 the characteristic roughness for the three different cap schemes after annealing is shown. The vacuum annealing conditions did not have any significant effect on the roughness of the surface. The contact of set B cap has the higher roughness (17nm), followed by that of set C (13nm) while set A exhibited the smoother surface with a mean roughness of 9nm. Moreover, the contacts with set C cap layers revealed good adhesion for deposition of Au overlayer and for further thermal compression probably due to the presence of the Pt layer at the surface (see Fig. 1d).

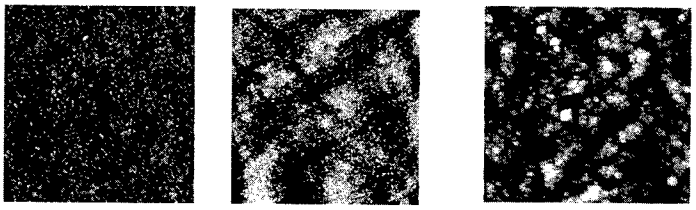

Fig. 4. AFM photos (5μmx5μm with 100nm z-scan) of the annealed surfaces: of the contact with Pd/Ni (set A), with Ni/Pt (set B) and with Pt/Ni (set C) cap layers respectively (from left to right).

Conclusions

Oxide-free Al/Ti-based ohmic contacts on p-type 4H-SiC were obtained only when the annealing was performed under high vacuum conditions. The use of Pd/Ni, Ni/Pt and Pt/Ni cap layers did not prevent the outdiffusion and evaporation of Al. TiC formation was observed at high temperature post deposition annealing. Si outdiffusion and Ni_2Si/TiC duplex formation above the initial Ti layer was evident. This contact fabrication technique could be useful for the fabrication of high frequency and high power switching bipolar 4H-SiC devices, when low series resistance and thermal stability are critical factors for efficient device operation.

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Thermal Stability in Vacuum and in Air of Al/Ni/W Based Ohmic Contacts to p-Type SiC

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Keywords: Ohmic Contacts, Silicon Carbide, Thermal Stability

Abstract: The Al/Ni/W contact demonstrated excellent thermal stability after being aged at 600°C in a high vacuum of $1x10^{-6}$ mmHg for 1022 hours. No degradation in contact resistivity was found after the aging. However, 1 hour aging in air severely degraded the ohmic characteristics of the Al/Ni/W contact. An Al/Ni/W/Mo contact showed ohmic behavior at 300°C in air for 186 hours, while an Al/Ni/W/Au contact displayed good thermal stability at 600°C in air for over 100 hours. In order to avoid the problem of metal oxidation in air and at elevated temperatures, we have proposed and tested a new approach to improving the in-air thermal stability of the Al/Ni/W ohmic contact by adding a top conductive oxide layer to the contact.

1. Introduction

Prototype semiconductor devices based on SiC technology with operating temperature beyond 400°C have shown great potential for commercialization [1]. At least for the present time, the performance of SiC devices is often limited not by the material itself but by the contact performance and the device packaging [2]. At the 4th International High Temperature Electronics Conference we reported the thermal stability of an Al/Ni/W ohmic contact to p-type SiC after being aged at 600°C for 300 hours in high vacuum [3]. In this paper the thermal stability of the Al/Ni/W contact aged in high vacuum up to over 1000 hours is given. Because the high vacuum condition under which the long-term testing was performed does not represent the typical environmental condition the SiC devices operate in, efforts have been made to improve thermal stability in air of ohmic contacts at high temperatures. Processing parameters used in this study are the same as previously reported [3].

2. Thermal Stability in High Vacuum of Al/Ni/W Ohmic Contact

The Al/Ni/W contact demonstrated excellent thermal stability after being aged at 600°C in high vacuum for 1022 hours. No change was found in the current-voltage characteristics after the aging experiment. In fact, the contact resistivity slightly decreased during the 600°C aging as shown in Fig. 1. The chemical depth profiles of Al, Ni, W, O, Si, and C for the Al/Ni/W ohmic contact after aging at 600°C for 1022 hours were determined using Auger Electron Spectroscopy (AES) and are shown in Fig. 2. It was found that the profiles were identical with those for the same contact after the ohmic-forming annealing at 850°C for 5 minutes. No aluminum oxide or any interdiffusion was observed after the long-term 600°C aging process. The formation of thermally stable NiAl and Ni_2Si compounds previously reported explains the high temperature stability of the electrical characteristics of the Al/Ni/W contact.

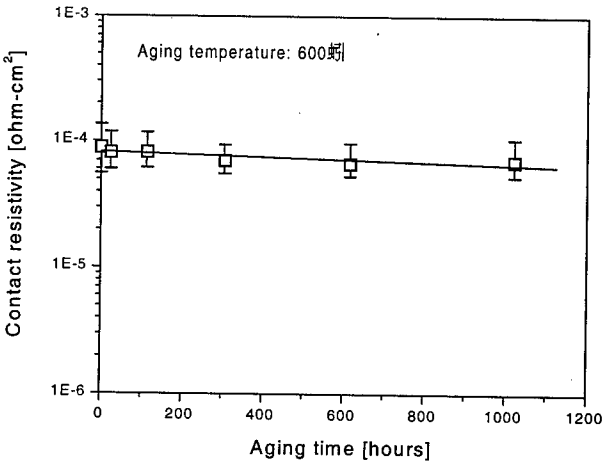

Fig. 1. Contact resistivity versus aging time at 600°C of Al/Ni/W ohmic contact to p-type SiC.

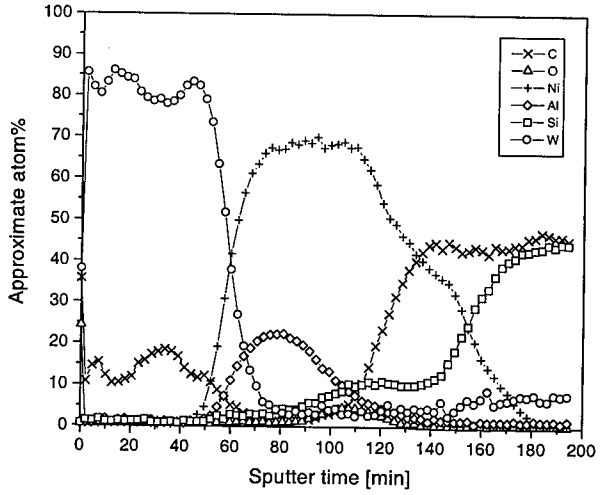

Fig. 2. AES chemical depth profiles of Al, Ni, W, Si, C, and O of Al/Ni/W contact to p-type SiC determined after aging at 600°C for 1022 hours.

3. Air Aging of New Al/Ni/W Based Ohmic Contacts to p-type SiC

The above-mentioned aging experiment was conducted in a high vacuum (10^{-6} mmHg). Because many applications require ohmic contacts that are thermally stable in an ambient atmosphere, the thermal stability of the Al/Ni/W ohmic contact in air was tested and efforts have been made to develop new ohmic contacts that are thermally stable in the air environment. The Al/Ni/W ohmic contact to p-type SiC was aged in air at 600°C for 1 hour. Unfortunately, even such a short duration of air aging severely degraded the ohmic characteristics of the contact. AES chemical depth profiles indicated that after the 1 hour aging, the top W layer was completely oxidized. In addition, oxygen also diffused into the contact inner layer and reacted with Al to form Al_2O_3. In order to improve the ambient stability of the Al/Ni/W contact, Mo or Au were added as a cap layer to the Al/Ni/W contact. The new contacts

were then aged at 300°C in air. This new aging experiment showed that the contact resistivity of the Al/Ni/W/Mo contact gradually deteriorated over time and the I-V curves became non-linear after 186 hours. This is most likely related to the fact that Mo has a very high oxide vapor pressure, so that as the oxide forms at elevated temperatures, it vaporized off the surface, causing a rapid consumption of the metal cap layer. Fig. 3 shows the total resistance of a pair of contact pads for Al/Ni/W/Mo contact versus aging time at 300°C in air. On the other hand, the contact resistivity of the Al/Ni/W/Au contact was almost unchanged during 300°C air aging for 300 hours. Further air aging the same contact at 600°C also produced very good results. The contact has demonstrated good thermal stability up to over 100 hours as shown in Fig. 4. However, the Al/Ni/W/Au contact demonstrates a very poor surface morphology. Because there is no chemical reaction in Au-W and Au-Ni systems, the rough surface in the Al/Ni/W/Au system is the result of a chemical reaction in the Au-Al binary system. In the Au-Al system there are three eutectic reactions at 525, 569, and 650°C, respectively. All these temperatures are far below the annealing temperature that we used to form the ohmic contact (800°C). A reaction between Au and Al occurred even though there are approximately 400 nm of Ni and W layers between them.

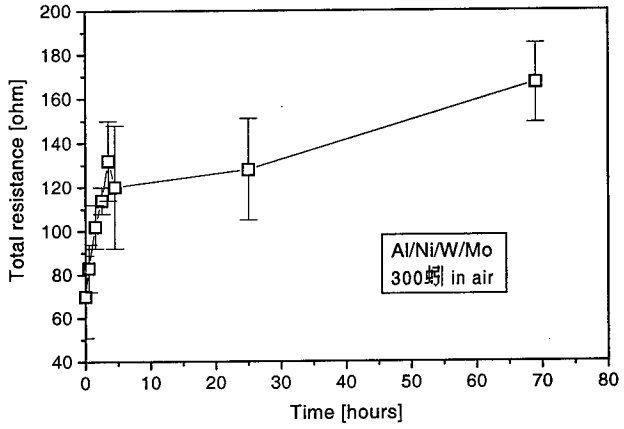

Fig. 3. Contact resistance of Al/Ni/W/Mo contact versus aging time at 300°C in air.

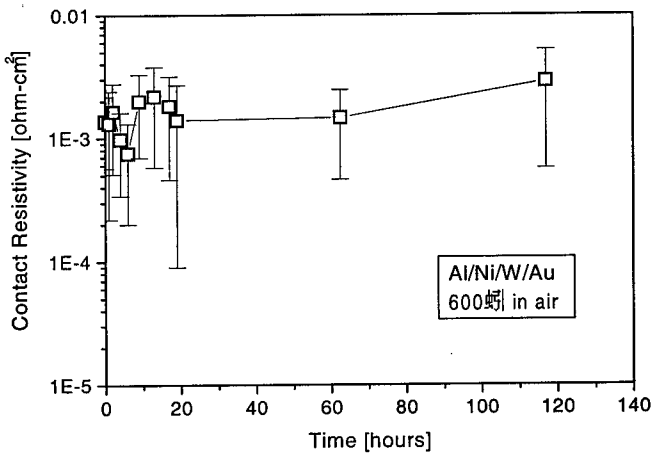

Fig. 4. Contact resistivity versus aging time at 600°C in air for the Al/Ni/W/Au ohmic contact.

4. New Approach to Improving In Air Thermal Stability of Ohmic Contact

In order to avoid the problem of metal oxidation in air at elevated temperatures, we have proposed a new approach to improving the in-air thermal stability of the Al/Ni/W ohmic contact to p-type SiC. That is to add a top conductive oxide layer to the Al/Ni/W contact. We sputtered a thin layer of In_2O_3 (90%)-SnO_2 (10%) (ITO) and tested its electrical property. The ITO layer showed good conductivity in the as-deposited condition. Annealing at 400°C decreased its electrical resistivity and no significant change was found after annealing it at 800°C. The Al/Ni/W/ITO contact to p-type SiC demonstrated ohmic characteristics after being annealed at 800°C for 3 minutes. Preliminary data from the air-aging study of the Al/Ni/W/ITO is shown in Fig. 5.

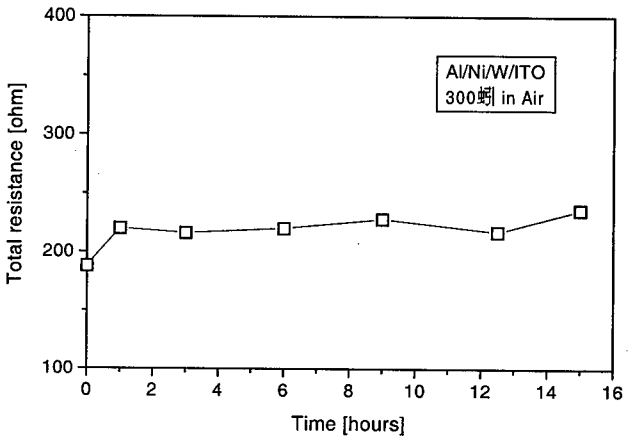

Fig. 5. Contact resistance versus aging time at 300°C in air for the Al/Ni/W/ITO ohmic contact to p-type SiC.

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A UHV Study of Ni/SiC Schottky Barrier and Ohmic Contact Formation

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Keywords: I-V, Ni, Ohmic Contacts, Schottky Barrier, XPS

Abstract: The use of Ni to form metal contacts to SiC has received considerable attention recently for both ohmic and Schottky contact formation. Within this paper, we present results on the formation of Ni/SiC Schottky barriers, for a variety of sample preparations which include a RCA clean, thermal oxide growth and strip and a UHV clean by thermal desorption. An XPS study was performed to examine the chemical interactions occurring at the Ni-SiC interface for sub-monolayer and increasing Ni deposition and as a function of temperature. In addition, a parallel study was performed whereby a thick (35nm) layer of Ni was deposited *in-situ* onto these clean surfaces and patterned into circular diodes. The diodes were then characterised electrically, using an I-V technique and a barrier height of 1.6eV with ideality, n of 1.1 was recorded. Upon annealing the diodes at 500°C the barrier height was seen to increase to 1.73eV in agreement with the XPS results. The work was then extended to diodes formed under HV with no UHV clean. Barrier heights of 1.6eV with idealities of 2 were recorded for both RCA cleaned and oxide stripped samples. However, upon annealing these diodes at 500°C the barrier height was increased to 1.9eV and the ideality improved to match that of the UHV formed diodes.

Introduction

The current immense research interest in SiC for high power device application has been fuelled by its superior material properties, i.e. electric field breakdown, thermal conductivity and wide bandgap, when compared with those of Si[1]. For example, high voltage Schottky rectifiers with breakdown voltages in excess of 2.5KV have recently been reported by Chilukuri and Baliga[2]. However, this result still only amounts to 50% of the ideal breakdown voltage theoretically predicted for the material. It is thus apparent that optimal performance of SiC power devices has yet to be realised and several key fundamental issues associated with the actual formation of the devices have still to be resolved. One crucial issue in particular, is the formation of reproducible high quality metal contacts to SiC.

Nickel has received considerable attention as a suitable metal for both Schottky and ohmic contact formation. As deposited, Ni forms a rectifying contact to SiC with a Schottky barrier height typically in the range of 1.3eV to 1.6eV[3], depending on the sample preparation methods adopted. In order to form an ohmic contact to SiC using Ni, it is necessary to anneal the contact at 950-1000°C for several minutes[4]. This results in the formation of nickel silicide and the electrical conversion of the contact from Schottky to non-rectifying or ohmic. However, whilst the formation of the silicide is seen as a key factor in this process, it has, by itself, been shown to be insufficient in causing the contact to exhibit ohmic behaviour[5].

Within this work we have used the surface science technique of Xray photoelectron spectroscopy (XPS) to examine the dependence of the Ni/SiC Schottky barrier on interface composition, quality and chemical nature. The effect of temperature was also studied. Schottky diodes were formed *in-situ* on ultra-high vacuum (UHV) clean SiC surfaces and their electrical nature assessed as a function of temperature using an *ex-situ* current voltage (I-V) technique. Based

on the knowledge acquired from this ideal case-study, the work was extended to "real" Schottky diodes formed on chemically cleaned surfaces under high vacuum (HV) conditions.

Experimental details

The wafers used for the XPS study were 4H n^+ SiC substrates, doped 2e18cm^{-3} and for the I-V study, n^+ substrates with a 10μm thick epilayer doped 1.2e16cm^{-3}, both supplied by Cree Research Inc. NC, USA. All the samples were subjected to a preliminary chemical clean which consisted of a solvent clean followed by a standard RCA clean.

For the XPS study, two *ex-situ* sample preparations were considered prior to the *in-situ* clean. Following the RCA clean mentioned above, a 400Å dry thermal oxide was grown on one substrate and then etched using concentrated HF acid. Both samples were admitted to UHV and heated gradually to 980°C to remove adsorbates and contaminants from the surface, (the UHV clean). Both samples were seen to exhibit the $\sqrt{3}x\sqrt{3}$ diffraction pattern as observed by LEED, indicative of a clean and ordered surface for 4H SiC[6]. Ni layers of increasing thickness were then deposited. The total thickness deposited was approximately 50Å. After each deposition the samples were scanned using XPS to monitor any chemical or electrical reactions occurring. Finally, the samples were subjected to a series of 10 minute anneals of increasing temperature from 500°C upto 1250°C. After each anneal the samples were scanned to determine the reactions occurring in the conversion from Schottky barrier to ohmic contact.

The epilayer samples used to form Schottky diodes under UHV conditions were subjected to the same ex-situ and in-situ cleaning procedure as the samples used for the XPS study. A single thick layer of Ni was deposited at room temperature. The samples were then removed from UHV and the Ni patterned into circular diodes of 650μm diameter. A thick layer of Ti, deposited by e-beam evaporation under HV, provided the back ohmic contact. This metal has been reported to form an ohmic contact as deposited on SiC[2] and thus enabled the back contact to be formed after the UHV Schottky contact. For comparison however, a sample was prepared where the Ti was deposited prior to forming the UHV Schottky contact. This was therefore annealed to 980°C during the UHV clean procedure. The diodes formed were electrically characterised by I-V measurements, at room temperature, in the dark. The diodes were then annealed and re-measured for comparison with the result of the XPS study.

Results - *ideal surfaces*

A detailed discussion on the results of the XPS Ni deposition and thermal anneal study is beyond the scope of this paper and will appear in a future publication[7]. However, the following important points are of note.

Figure 1 shows the peak shifts occurring for the Si 2p peak as a function of (a) Ni deposition and (b) anneal temperature. This is representative of the trend that occurred for both the RCA-UHV clean and oxide stripped-UHV clean samples during the deposition sequence. In this work, the term peak position refers to the binding energy at which the centroid of the peak occurred. A peak shift of 0.25eV to lower binding energy was measured, indicative of the on-set of band-bending as the Schottky barrier was formed. For the oxide stripped sample, a larger shift was observed, corresponding to *a different Schottky barrier height for*

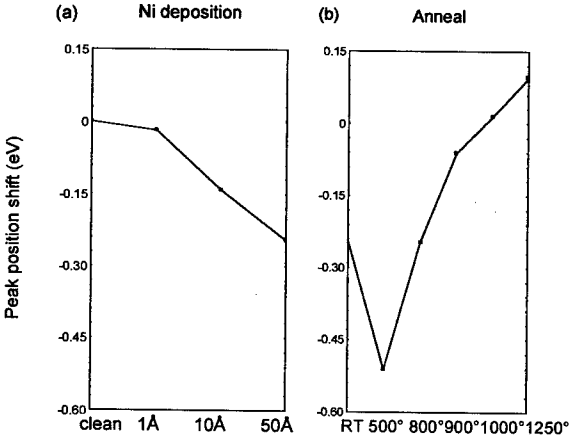

Figure 1. Peak Position shift for Si 2p as a function of (a) Ni coverage and (b) Temperature.

the two sample preparations. Following the 500°C anneal it was seen that the peak position shifted a further 0.26eV to lower binding energy, indicating that *by annealing Ni Schottky diodes at 500°, an increase in Schottky barrier height would be obtained.* As the anneal temperature was increased further the peak shift was seen to decrease back towards higher binding energy. However, *at the temperature at which an ohmic contact is known to form*[4] *(between 950 and 1000°C), the peak position shift of 0.52eV to higher binding energy still corresponded to a Schottky barrier height of over 1eV.* Figure 2 shows the Si 2p and C 1s spectra as a function of anneal temperature for the RCA-UHV cleaned sample. For the Si 2p, it can be seen that after the 500°C anneal a large silicide component had emerged on the lower binding energy side of the spectra. It is known that dissociation of SiC occurs around 500°C with the formation of $Ni_{31}Si_{12}$ and $Ni_{23}Si_2$ phases[8], which change predominantly to Ni_2Si above 700°C and NiSi at 1100°, for the thickness of Ni coverage and anneal time used. For the C 1s spectra the 500°C anneal resulted in a large graphite component which dominated the spectra for the remainder of the anneals. Holloway *et al*[9] has proposed that two methods of ohmic contact formation exist.

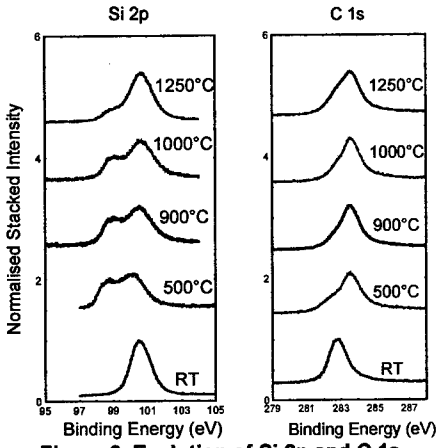

Figure 2. Evolution of Si 2p and C 1s core leves as a function of temperature.

(1) The use of a metal with low workfunction on an unpinned semi-conductor.

(2) The introduction of donors into the near surface region of the semiconductor, thus reducing the width of the Schottky barrier depletion region, enabling current transport to occur across the barrier by the mechanism of thermionic field emission.

As the XPS results show that the high T anneal does not show ohmic behaviour (i.e. a barrier of 1eV), it is likely that donors are introduced near the surface region. One possibility is via the production of Kirkendall voids. The Kirkendall effect[10] states that due to different rates of diffusion (Si diffuses faster in Ni than Ni in Si), Si vacancies will be created in the near surface region of SiC as Ni_2Si forms. However, the fact that Ni_2Si forms at temperatures of 700° and the Ni/SiC contact remains rectifying up to temperatures of 900-1000°C implies that this silicide formation is not solely responsible for the ohmic contact formation. Ni_2Si is a Ni-rich compound. As the temperature is increased further, the silicide phase is said to change to NiSi[8], a more Si-rich compound. It is perhaps the case that the additional Si vacancies act as donor states and play a crucial role in the ohmic contact formation. Such a theory is supported by Noblanc[4] *et al* who tried to reduce the amount of graphite formed at both the interface and free surface during the anneal using solely Ni_2Si as the contact material. Although this did reduce the amount of graphite generated, the specific contact resistance of the ohmic contact formed was an order of magnitude higher than using pure Ni. However, while this result supports the

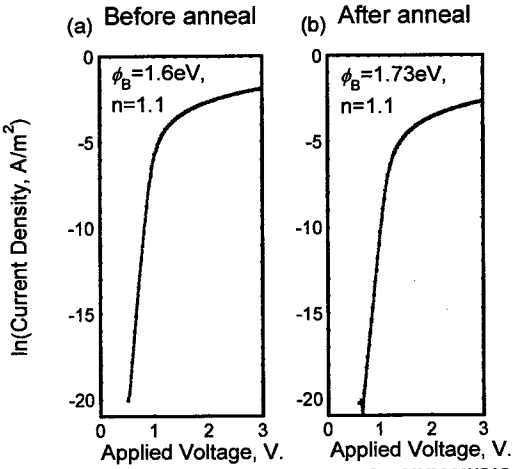

Figure 3. I-V characteristics for UHV Ni/SiC Schottky diodes (a) before and (b) after a 500°C aneal. Annealed Ti was used for the back contact.

silicon vacancy theory, to the authors knowledge there is no proof that Si vacancies will act as donor states. Figure 3 shows forward I-V characteristics for Ni/SiC Schottky diodes formed under UHV conditions for an RCA-UHV cleaned sample (a) before and (b) after a 500°C anneal. The reverse I-V characteristics are not shown due to the values obtained being below the measurement detection level. The back contact used was UHV annealed Ti. The characteristics were fitted using thermionic emission theory[11] and the barrier height and ideality extracted. The results are shown in Table 1(a). In agreement with the results of the XPS study, an increase in Schottky barrier height of 0.13eV was achieved following the 500°C anneal. No improvement in the ideality was seen.

Table 1.	(a) UHV formed diodes	(b) HV formed diodes	
	RCA and UHV clean	RCA clean	Oxide strip
Before anneal	ϕ_B=1.6, n=1.1	ϕ_B=1.6, n=2	ϕ_B=1.6, n=2.2
After anneal	ϕ_B=1.73, n=1.1	ϕ_B=1.9, n=1.1	ϕ_B=1.9, n=1.2

Results - *Real surfaces*

To examine whether the results of the UHV study could be extended to "real" SiC surfaces, Schottky contacts were formed on RCA cleaned and RCA cleaned/oxide stripped epilayers (without the UHV clean) under HV conditions, base pressure, P =$5x10^{-7}$mb. Unannealed Ti was used to provide the back contact. The I-V characteristics were fitted and the Schottky barrier heights and idealities measured are shown in Table 1(b). For both samples a barrier height of 1.6eV was recorded with poor idealities and large series resistance components. Upon annealing the diodes, the barrier heights were seen to increase by 0.3eV to 1.9eV in accordance with the UHV results. This result corresponds to the largest Ni/SiC Schottky barrier height measured to date. In addition, the series resistance term and the idealities both improved to equal those achieved with UHV clean samples.

Conclusion

Within this work we have found that Ni deposited on UHV-clean SiC substrates exhibit different Schottky barrier heights for two different sample preparations. Annealing Schottky diodes at 500°C causes the barrier height to increase by 0.25eV (XPS) and between 0.13 and 0.3eV (I-V). This result holds for both UHV and HV prepared diodes. The anneal was also seen to improve the ideality of the diodes and the Ti ohmic back contact. Based upon the XPS results, a hypothesis of the elemental mechanisms at work in the formation of the Ni/SiC ohmic contact is proposed, based on Si vacancies. However, to substantiate this, further UHV studies are required, the results of which will form the basis of a future publication.

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Fermi Level Pinning and Schottky Barrier Characteristics on Reactively Ion Etched 4H-SiC

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Keywords: Annealing, Barrier Height, Fermi Level Pinning, Ideality, Leakage Current, Nickel, Platinum, Reactive Ion Etching, Schottky Barrier, Titanium

Abstract. The effects of reactively ion etching 4H-SiC epilayers in a CHF_3/O_2 gas mixture on the properties of Pt, Ni, and Ti Schottky barriers subsequently deposited on the etched surfaces are investigated using forward and reverse current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements. Pronounced Fermi level pinning is present on the etched surfaces, and the forward *I-V* characteristics become anomalous. Average *C-V* barrier heights are 1.65, 1.44, and 0.81 V for Pt, Ni, and Ti on unetched material, respectively; and 1.42, 1.40, and 1.29 V, respectively, on etched material without annealing. The *I-V* characteristics are more uniform on etched material, and reverse leakage can be made acceptably low with suitable annealing for all three metals on etched material.

Introduction. Schottky barriers are used in several SiC-based devices, including MESFET's, high voltage rectifiers, and static induction transistors. Electrical properties of Schottky barriers are generally very sensitive to the condition of the surface on which they are formed, and in particular, to the density and energies of interface states. Reactive ion etching (RIE) or other plasma-based processes can produce near-surface damage in many materials, affecting barrier heights, ideality factors, and leakage currents of Schottky barriers subsequently formed on the etched surfaces. Such effects have been investigated only to a limited degree in 4H-SiC [1-4], though they may be important in devices where etching must be performed prior to metallization. Here, we investigate the effects of a particular CHF_3/O_2-based RIE method on Schottky barriers using electrical characterization.

Experimental Methods. Starting material was commercial 2 μm thick 4H-SiC epilayers, doped to N donor concentrations of $1\text{-}2 \times 10^{17}$ cm^{-3}. They were grown on n^+, 0.015 Ω-cm N-doped 4H-SiC Si-face substrates, 35 mm diameter and misoriented by 8° from (0001). Wafers received a modified RCA clean, followed by sacrificial oxidation, which was stripped in buffered oxide etch (BOE). On three wafers, areas where the Schottky metal was to be deposited were first etched in a 15 sccm CHF_3 / 40 sccm O_2 mixture in a Plasmatherm 770 reactive ion etcher to depths of 2300-3400 Å. The process used RF power of 450 W, 70 mTorr pressure, a self-bias voltage of about 0 V (floating substrate), and backside cooling with He gas. The etching process was optimized for smooth morphology. Backside Ni ohmic contacts were then evaporated on all wafers and annealed, then overlayed with Ti/Au. A BOE etch followed by a DI rinse and N_2 blow dry was performed just prior to evaporation of the Schottky metals at a base pressure $\leq 1 \times 10^{-6}$ Torr. Metallization consisted of 500 Å of either Pt, Ni, or Ti, with a 3000 Å Au overlay in each case; each metal was deposited on one etched wafer and on several unetched control wafers or pieces. Diodes were patterned into 1.31×10^{-3} cm^2 areas using lift-off; no high-voltage termination was employed. Some 0.2-1.0 mm diameter diodes were formed instead by shadow masked deposition on material doped around 1×10^{16} cm^{-3}. After initial electrical testing, wafers were quartered and selected pieces were annealed in flowing N_2 for 60 s at either 400, 500, or 600 °C and then re-tested.

Forward and reverse *I-V* characteristics were measured at 297 K using a HP 4145 semiconductor parameter analyzer from 0-2.2 V and from –100 to 0 V. The forward current density (*J*) was fit in every case using a multi-step, nonlinear least-squares algorithm to the equation

$$J = \left[J_{sat,1}\, e^{\left(\frac{q(V - J R_{sp,1})}{n_1 kT}\right)} + J_{sat,2}\, e^{\left(\frac{q(V - J R_{sp,2})}{n_2 kT}\right)} \right] \left(1 - e^{\frac{-qV}{kT}}\right); \quad J_{sat,1} = A^* T^2 e^{-(q\phi_{Bn}/kT)}, \quad (1)$$

where the six fitting parameters are the two saturation currents, $J_{sat,1}$ and $J_{sat,2}$, corresponding ideality factors, n_1 and n_2, and corresponding specific series resistances, $R_{sp,1}$ and $R_{sp,2}$. Also, q is the electronic charge, k is Boltzmann's constant, T is the absolute temperature, A^* = 153 A cm^{-2} K^{-2} is the effective Richardson constant, and ϕ_{Bn} is the barrier height. The first term represents the usual thermionic emission current (generally dominant at high forward bias) and the second, optional term is the "excess" current sometimes observed at low forward bias. The latter term might represent generation-recombination current, but is usually associated in our opinion with current through low barrier-height patches in a nonuniform contact [5]. We recently showed that these patches involve discrete crystal defects visible as dark spots (recombination centers) in electron beam induced current (EBIC) images [6]. The specific on-resistance usually needs to be different for each term to obtain a reasonable fit, consistent with the spreading resistance associated with patches. This model fit well for most diodes on unetched material, but did not work for diodes on etched material, which display anomalous forward *I-V* characteristics. In that case, we fit only to the low current region, and the barrier heights extracted from the fits are of questionable validity. About 500 devices were studied.

The *C-V* characteristics were measured on many of the same devices using a HP 4284A precision LCR meter from –2 to 0 V at frequencies between 10 kHz and 1 MHz (optimized for best quality factor). A least-squares fit to C^{-2} as a function of V yielded the net donor concentration (N_D) and the intercept along the voltage axis, V_i, which is used to find the barrier heights [7], taking the conduction band density-of-states as 1.82 × 10^{19} cm^{-3}. The crucial quality factor was monitored for every diode and was typically >100. The correlation coefficient squared of the fits (R^2) was generally 1.00000, showing excellent linearity and no noise in the data.

Results and Discussion. Forward *I-V* characteristics of typical unannealed "good" devices for each metal on unetched material are shown as curves marked with open symbols in Fig. 1. Many individual devices however showed large excess currents at low bias, as well as higher ideality factors at high current, especially for Pt and Ni. (The ideal current is higher for Ti, so these nonidealities may simply be obscured in that case.) We previously related the nonidealities to discrete crystal defects under the diodes [6]; the good devices should therefore better reflect the intrinsic behavior of the contact. Even relatively good devices still have idealities significantly greater than one on many wafers, however, as reflected in Table 1. We found a pronounced linear correlation between increasing ideality factor (n_1) and decreasing barrier height, which we attributed to nonuniformity arising mainly from discrete crystal defects [6]. The true (defect-free) barrier height can be inferred by extrapolating this relationship to n_1 = 1 (using only data with $n_1 \leq 1.5$); these extrapolated values are listed in Table 1. Values derived from *C-V* measurements are much less affected by localized defects, as that measurement averages over the contact area. (All our *C-V* derived values are actually

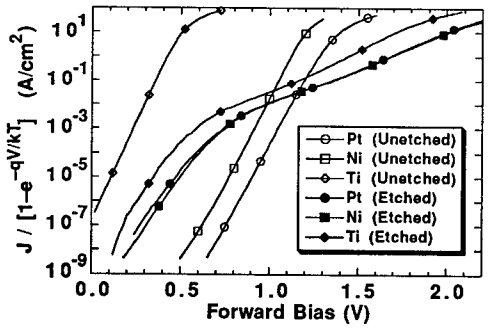

Fig. 1. Typical forward *I-V* data for Schottky diodes on etched, unetched 4H-SiC (no anneals).

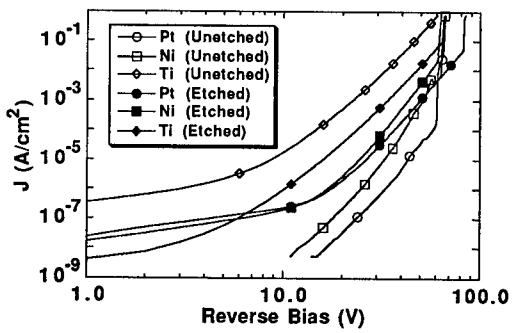

Fig. 2. Typical reverse *I-V* data for Schottky diodes on etched, unetched 4H-SiC (no anneals).

Table 1. Electrical characteristics of Schottky diodes on etched and unetched 4H-SiC.

Metallization	Etch	Anneal temp. (°C)	Barrier Heights (V)			Median Ideality	# of wafers	# of devices	–20 V Leakage (A/cm²)	
			C-V Derived	Average *I-V*	Linearly Extrap. *I-V*				10% quantile	Median
Pt	N	None	1.65 ± 0.02	1.40 ± 0.09	1.66	1.31	4	92	–	–
Ave. ± 1 std. dev. (Range)[a]			(1.60-1.69)	(1.32-1.54)	(1.62-1.71)	(1.13-1.42)			(4.9×10^{-8} - 7.4×10^{-8})	(1.2×10^{-7} - 3.8×10^{-2})
Ni	N	None	1.44 ± 0.01	1.28 ± 0.11	1.44	1.16	5	202	–	–
Ave. ± 1 std. dev. (Range)[a]			(1.40-1.49)	(1.13-1.45)	(1.31-1.54)	(1.06-1.23)			(9.2×10^{-8} - 2.3×10^{-6})	(1.2×10^{-6} - 1.9×10^{-5})
Ti	N	None	0.81 ± 0.03	0.75 ± 0.02	0.77	1.07	5	83	–	–
Ave. ± 1 std. dev. (Range)[a]			(0.63-0.95)	(0.61-0.82)	(0.61-0.86)	(1.03-1.10)			(4.7×10^{-4} - 2.1×10^{-1})	(8.5×10^{-3} - 4.2×10^{-1})
Pt	Y	None	1.42 ± 0.01	0.98 ± 0.11[b]	1.14[b]	1.61	1	39	9.7×10^{-7}	3.2×10^{-6}
Ni	Y	None	1.40 ± 0.03	1.00 ± 0.10[b]	1.14[b]	1.60	1	43	7.0×10^{-7}	2.7×10^{-6}
Ti	Y	None	1.29 ± 0.01	0.92 ± 0.09[b]	1.19[b]	1.43	1	27	1.8×10^{-5}	3.8×10^{-5}
Pt	Y	500	1.38 ± 0.01	1.03 ± 0.03[b]	1.24[b]	1.78	1	5	2.6×10^{-7}	4.4×10^{-7}
Ni	Y	500	1.45 ± 0.03	1.03 ± 0.03[b]	1.17[b]	1.79	1	5	2.9×10^{-7}	5.2×10^{-7}
Ti	Y	500	1.41 ± 0.01	0.99 ± 0.08[b]	—	1.63	1	6	3.2×10^{-7}	4.0×10^{-7}

[a]Average of device averages for each wafer; standard deviation is average of standard deviations on individual wafers; range refers to minimum, maximum average value by wafer (*not* range of individual device values).
[b]Derived from low current portion of anomalous *I-V* characteristic; probably not reliable.

corrected to include image-force lowering, to be directly comparable to *I-V* derived values.) The *C-V* derived barrier heights in Table 1 generally agree very well with the linearly extrapolated *I-V* values, supporting our model of nonuniformity.

The reverse *I-V* characteristics of the same typical devices are similarly shown in Fig. 2 on a log-log scale. (Avalanche breakdown voltages vary substantially from device to device and should not be considered typical.) No model has yet been found which can fully explain the shape of these characteristics, so no fitting has been performed. In evaluating the leakage currents of these devices, it must be emphasized that the material is doped around 10^{17} cm^{-3}. On lighter doped (e.g., 10^{16} cm^{-3}) material, the leakage currents are much lower, and the breakdown voltages are much higher than those described here. Leakage currents are also tabulated in Table 1 at a typical reverse bias of –20 V. We quote observed (wafer-to-wafer) ranges of the median values instead of means, because the latter can be drastically affected by a subset of leaky devices. We also quote the ranges of tenth percentile values (reflective of the best devices on each wafer). It is clear that the lowest leakage currents and highest barrier heights are consistently obtained with Pt rather than Ni in our experiments, in contrast to recent work on sputtered metals by Saxena et al. [8]. Our results agree qualitatively with expectations based on metal work functions (5.65, 5.15, and 4.33 V for Pt, Ni, and Ti, respectively).

The barrier height of Ti on unetched SiC can be markedly increased to ~1.20 V and its leakage drastically reduced to the mid 10^{-7} A/cm^2 range (10th percentile value) by 60 s thermal annealing in the range 400-600 °C, similar to prior work [3]; however, the ideality does not improve. Annealing Ni and Pt has some effect on barrier height, but a major effect in our work is severe degradation in many cases, believed to be related to metal in-diffusion along pre-existing crystal defects. In the Ni case, a partial, nonuniform metallurgical reaction apparently occurs, reducing the *I-V* barrier height to ~0.96 V at 600 °C while actually increasing the *C-V* value slightly. Initial formation of a nickel silicide phase may be responsible [9]. Details of the annealing studies will be described elsewhere.

Diodes on reactively ion etched surfaces display marked changes in forward *I-V* characteristics, as shown by curves marked with closed symbols in Fig. 1. The characteristics are much less sensitive to metal work function than on unetched material. They show apparent barrier heights of 1.29-1.42 V and large idealities of ~1.4-1.6, based on low bias data only. At higher bias, the current is suppressed compared to the unetched case, apparently by nonlinear series resistance possibly involving tunneling through an interfacial layer. Khemka, et al. found similar results for Ni Schottky diodes on 4H-SiC etched with CHF_3/O_2 or CHF_3/CF_4, but not with CF_4/O_2 [1]. Schoen, et al. obtained good *I-V* characteristics on SF_6 etched surfaces [4]. The absence of good overall fits to a thermionic emission model and their poor agreement with *C-V* values render our *I-V* derived

barrier heights very questionable. The C^{-2}-V data still fit well to constant N_D and yield apparently reliable barrier heights (Table 1). Differences in the C-V derived barrier heights correspond well to overall horizontal shifts of the I-V data. Annealing increases the Ti barrier height, as on unetched material. A 600 °C anneal partially recovers the forward conduction of the Ni diodes above 1.2 V but has little effect at lower voltages. This effect is likely related to the nonuniform metallurgical reaction discussed above.

Reverse I-V characteristics are also substantially modified by etching, as seen in Fig. 2. The changes at biases above ~10-15 V are qualitatively consistent with the changes in C-V derived barrier heights. At lower bias, all Ni and Pt diodes on etched material display excess current, whose exponent suggests it is generation current in the depletion regions due to plasma-induced defects. It is largely eliminated by annealing at 400 °C or higher. The –20 V leakage is generally minimized for 500 °C anneals, where it becomes comparable for all three metals on etched material, and is no more than 10× higher than the lowest values on unetched material (see Table 1). Most importantly, the leakage current is more uniform and apparently less sensitive to crystal defects on etched material, especially for Ti diodes (compare median and 10th percentile values in Table 1). The 60 s, 600 °C anneal reduces the leakage slightly for the Ni diodes as it improves their forward conduction.

The C-V derived (most reliable) barrier heights for the three unannealed metals vary with a slope of 0.65 ($R^2 = 0.978$) as a function of metal work function on unetched material, implying some effect of surface states, but no hard pinning. Assuming an interfacial layer thickness of ~5 Å with a relative dielectric constant ≈4 then implies a surface state density around 2.4×10^{13} cm^{-2} eV^{-1}, using standard theory [7]. After etching (but no annealing), the slope is reduced to 0.11 ($R^2 = 0.937$). Relatively strong Fermi level pinning is therefore present. The chemical dependence of the effect, and the zero self bias we used, suggest that the fluorocarbon polymers likely deposited by this etch process [1, 10] contribute to the pinning. While etching may increase surface state density, it is also possible that increased pinning results mainly from increased interfacial layer thickness. Assuming the same surface state density, an interfacial layer thickness of 78 Å could cause the observed pinning, with less required if surface states are also created. Overlayers up to 80 Å have been reported for this type of etching [10]. To our knowledge, this is the first report of processing-induced pinning in SiC.

Conclusions. Reactive ion etching of 4H-SiC in CHF_3/O_2 causes increased Fermi level pinning in Schottky diodes, evident in both forward and reverse I-V characteristics and in C-V derived barrier heights. While forward conduction is degraded, possibly by interfacial fluorocarbon layers, devices on etched material are more uniform. Moreover, with suitable annealing, Ti can replace Ni or Pt on etched material and still maintain good low reverse leakage while benefiting from improved strength and adhesion. Further analytical work is needed to determine the exact causes of the pinning; increased interfacial layer thickness and surface state densities may both play a role.

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Real-Time Assessment of Overlayer Removal on 4H-SiC Surfaces: Techniques and Relevance to Contact Formation

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Keywords: Cleaning, Contact, Spectroscopic Ellipsometry, Surface Preparation, Synchrotron

Abstract: We applied real-time spectroscopic ellipsometric (SE) measurements to assess the removal of overlayer material from 4H-SiC Si- and C-face surfaces in order to investigate the final step of an otherwise standard RCA cleaning regimen commonly used to prepare SiC surfaces for contact formation. The selected treatments (buffered hydrofluoric acid (HF), concentrated HF, dilute HF and 5% HF in Methanol) removed 4 to 40 Å of effective SiO_2 overlayer thickness from these surfaces. We also found that the concentrated HF treatment yielded the best surface, i.e. the most abrupt bulk-to-ambient transition region.

Introduction: For traditional Si technology, both etching residue in the contact windows and damage by contact window etching are thought to cause significant increases in device contact resistance.[1] Similarly for SiC, the challenge has been to prepare smooth, atomically ordered surfaces free of chemical residues. This has proven to be nontrivial and is in fact a major source of irreproducibility in contact performance.[2] For these purposes, the ideal pre-treatment surface would (1) reduce the fixed oxide charge; (2) lower the density of states; (3) passivate, reconstruct, and flatten the surface; and (4) remove any contamination or native oxide. While processes have been developed (e.g. H_2 etching) that come close to meeting these ideal requirements[3], they remain largely infeasible for a production environment. As most practical processing regimens include an RCA-type clean, we use this as the starting point for our investigations. In particular, we investigate the final step of this cleaning regimen, as it varies considerably in the literature.[2,4,5] We found that a final treatment step consisting of concentrated HF yielded a smoother surface and removed more overlayer material for both (0001) and (000-1) surfaces than the other commonly used treatment options, as discussed below.

Experimental Details: Polished (0001) and (000-1) 4H-SiC substrates were processed according to one of the standard surface preparation regimens[5] developed for contact formation—minus the final step, which was assessed in real time with SE. Samples were processed with an RCA clean, prior to a H_2 plasma etch, described elsewhere.[6] They were next[7] subjected to another RCA clean, minus the final step, and then were transferred to the ellipsometer where they were maintained in flowing dry N_2. There the complex reflectance ratios ρ were measured and converted to pseudodielectric functions $\langle\varepsilon\rangle = \langle\varepsilon_1\rangle + i\langle\varepsilon_2\rangle$ via the two-phase (substrate/ambient) model.[8,9] Real-time data were obtained at 5.5 eV and supplemented off-line with $\langle\varepsilon\rangle$ spectra taken over a range of 1.5 to 6.0 eV for optical modeling purposes. Reference $\langle\varepsilon\rangle$ spectra from 1.5 to 6.0 eV were qualified by $\langle\varepsilon\rangle$ spectra obtained from 4 to 10 eV using from the vacuum-ultraviolet ellipsometer at the at BESSY synchrotron radiation source in Berlin.[10]

Three possible final treatment steps were evaluated: (1) Concentrated HF; (2) Dilute HF, specifically 10:1 H_2O:HF; and (3) Buffered HF, specifically 6:1 NH_4F:HF. For comparison we used the real-time approach to develop a fourth option: a sequential application of H_2O, methanol, 5 volume % HF in methanol, with no preliminary RCA clean. All samples were subjected to a final H_2O rinse. Chemical treatments were applied for approximately 3-5s each and the samples were

subsequently blown dry, in addition to being maintained in dry N_2 during all measurements and treatments. Samples were mounted vertically on a vacuum chuck in a windowless cell with a drain at the cell bottom, to prevent accumulation of chemicals, and with an opening on top, to allow the application of wet chemical treatments. This arrangement enables the treatments to be applied while data are being taken.

Theory and Discussion: The general strategy is to measure $\langle\varepsilon\rangle$ at a constant energy above the absorption edge of the material and to monitor its evolution with respect to wet chemical treatments.[8,11] These real-time data reveal: (1) the degree of effectiveness of specific treatments regarding overlayer removal and (2) any evidence of deleterious effects of these treatments, e.g., to surface overlayers, is a weighted average of the dielectric functions of the substrate and overlayer, where "overlayer" may also refer to a microscopically rough termination. For $|\varepsilon_s| >> \varepsilon_a=1$, $\langle\varepsilon\rangle$ is given in the three-phase (substrate / overlayer / ambient) model by[12]

$$\langle\varepsilon\rangle \cong \varepsilon_s + \frac{4\pi i d}{\lambda}\varepsilon_s^{3/2}\left(1-\frac{\varepsilon_o}{\varepsilon_s}\right)\left(1-\frac{1}{\varepsilon_o}\right), \qquad \text{(Eq. 1)}$$

where ε_S, ε_O, and ε_a are the dielectric functions of the substrate, overlayer, and ambient, respectively; d is the layer thickness, and λ is the wavelength of incident light. If $|\varepsilon_S| >> |\varepsilon_o| >> |\varepsilon_a|$, the contribution from ε_o can be neglected, meaning that it is not necessary to know the identity of an overlayer to monitor its removal. However, this places more emphasis on observing chemical reactivity if the identity of an unknown overlayer is to be deduced.

For 4H-SiC in the quartz optics range, we have found that removing an existing overlayer increases $\langle\varepsilon_1\rangle$ and decreases $\langle\varepsilon_2\rangle$. Conversely, treatments having deleterious effects are expected to produce the opposite response. Therefore, the most abrupt surfaces are those for which the above-bandgap values of $\langle\varepsilon_1\rangle$ and $\langle\varepsilon_2\rangle$ are maximized and minimized, respectively. We illustrate this with the results of three-phase (4H-SiC(0001) substrate/ SiO_2 overlayer/ air ambient) model calculations performed on broadband spectra taken at BESSY (Fig. 1) and on narrowband spectra taken after real-time treatments were applied (Fig. 2). In Fig. 1, SiO_2 overlayers in increasing 10 Å increments, for a total of 50 Å of SiO_2, are used to illustrate the dramatic effect of oxide overlayers on the higher-lying optical transitions of the material. And though there is decreased sensitivity to the presence of overlayers below ~6 eV, we can see than an increase in SiO_2 thickness here does indeed result in a decrease in $\langle\varepsilon_1\rangle$ and an increase in $\langle\varepsilon_2\rangle$. Further, the calculations in Fig. 2 confirm this result for energies in the entire quartz optics range and show that there is sufficient sensitivity to

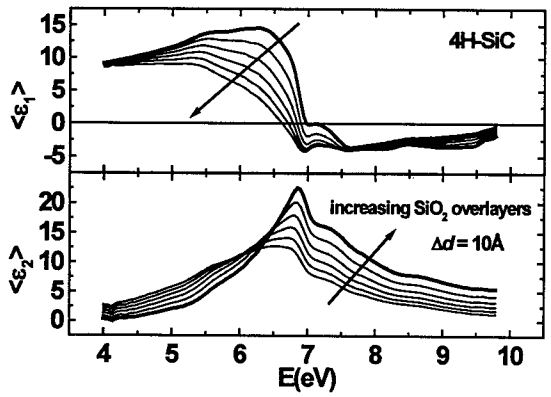

Figure 1. Broadband $\langle\varepsilon\rangle$ spectra (4 to ~10 eV) taken with the vacuum ultra-violet ellipsometer at the BESSY synchrotron radiation source. Data are shown by the heavy solid lines. Lighter lines show the results of three-phase model calculations simulating the effect of a succession of increasing SiO_2 overlayers, where Δd = 10 Å. Arrows show effect of increasing overlayers.

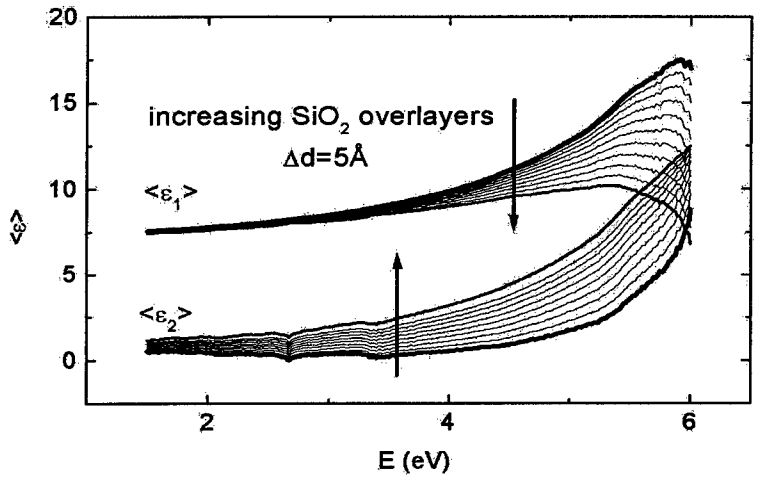

Figure 2. Narrowband (1.5 to 6 eV). Data are shown by the heavy solid lines. Lighter lines show the results of three-phase model calculations simulating the effect of a succession of increasing SiO_2 overlayers, where $\Delta d = 5$ Å. Arrows show effect of increasing overlayers.

the presence of overlayers here to allow for the real-time assessment of overlayer removal. As seen in the figure, $\langle\varepsilon_1\rangle$ and $\langle\varepsilon_2\rangle$ are sufficiently suppressed and elevated that they actually intersect after only 30 Å of oxide overlayer. These fits also aided in the selection of an appropriate energy at which to take data for the real-time treatments, here 5.5 eV.

Results and Conclusions: Both the real-time $\langle\varepsilon\rangle$ data and the off-line $\langle\varepsilon\rangle$ spectra indicated that for both C- and Si-face surfaces the concentrated HF treatment yielded a smoother surface and removed more overlayer material than the dilute or buffered HF solutions. As a case in point, if we model the overlayer as SiO_2, we find for the (0001) surface that the RCA clean deposited 4 Å of material relative to the starting surface, whereas the subsequent concentrated HF treatment removed 11 Å, as seen Table I and Fig. 3. Fits were made over the most sensitive region (indicated) for overlayer removal. In contrast, the buffered HF solution actually degraded the sample surface, in addition to provoking gross surface instabilities. Real-time data showed evidence of rapid adsorbate formation and evaporation upon application of this treatment—on time scales significantly shorter than measurement times of conventional static surface characterization techniques. Such instabilities were more severe and happened on a dramatically faster time scale for the Si-face material. The fourth, entirely real-time treatment removed what appeared to be the greatest amount of material from both types of substrates (15Å and 17Å for the Si- and C-face, respectively), but the real-time data show that approximately half of this material was only organic and inorganic contamination, since it was removed by the initial methanol and H_2O treatment steps.

A summary of the changes in the amounts of overlayer material present on the surfaces that result from the various treatments is given for the two substrate orientations in Table I. Thickness values are expected to vary slightly to account for differences between individual wafers or regions of wafers. Larger relative uncertainties for some treatments indicate that the choice of model should be modified, presumably to account for surface roughness. However, our attempts to refine our models by introducing surface roughness indicated that access to the higher-lying optical transitions would be necessary to obtain a fit with reasonable uncertainties. At the moment, such data are unobtainable, as the ultra-high vacuum requirements of the ellipsometer at BESSY currently

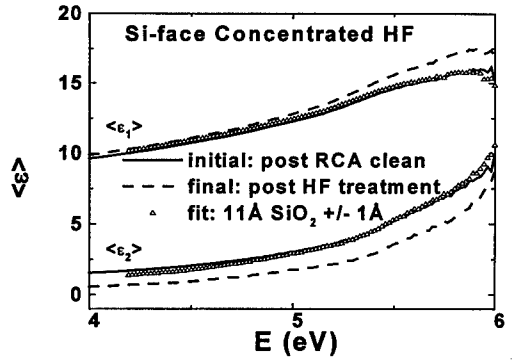

Figure 3. Data (lines) and fit (triangles) for a (0001) [Si-face] SiC sample. Pre-treatment surface is shown by solid lines. Post-concentrated HF treatment is shown by dashed lines. Fit is to pre-treatment surface.

prevent the *in situ* application of wet chemical treatments. Nonetheless, we have sufficient sensitivity in the available spectral range to determine that the most abrupt surfaces on both substrate orientations were achieved with the concentrated HF treatment. More abrupt surface to bulk transition regions mean that there will be fewer defects and recomination centers will be present. Thus it is reasonable to conclude that the "best" surface from the perspective of optical properties will also be a surface with improved electronic properties.[13]

Table I. Changes in overlayer thicknesses in Å that resulted from the RCA and final treatments for (0001) [Si-face] and (000-1) [C-face] SiC. Uncertainties for the Si- and C-face surfaces are ±1 and ±2Å, respectively.

	(0001)		(000-1)	
Treatments:	RCA-[last step]	*in situ* "last step"	RCA-[last step]	*in situ* "last step"
Conc. HF	4	-11	-3	-11
Buff. HF	2	38	17	-4
Dilute HF	-4	-5	-7	-8
5%HF /Meth.	not applicable	-15	not applicable	-17

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Materials Science Forum Vols. 338-342 (2000) pp. 1037-1040

Pre-Growth Treatment of 4H-SiC Substrates by Hydrogen Etching at Low Pressure

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Keywords: Hydrogen Etching, Pressure Dependence, Surface Morphology

ABSTRACT Etch rate and surface morphology of 4H-SiC by hydrogen etching at low pressure and at high temperature are investigated. Smooth and specular pre-growth surface can be obtained by etching at around 20 Torr and at temperatures ranged from 1600 to 1850 °C. Higher etch rate is obtained at low pressures. Protrusions, which have a hexagonal feature, are observed at 2 Torr. Triangular shaped defects extended in the direction of $<1\bar{1}00>$ are also observed at atmospheric pressure.

INTRODUCTION

Epitaxial growth is one of the most important techniques to achieve SiC devices. Quality of an epitaxial layer depends to a great extent on the substrate surface quality. The surface of commercially available SiC substrates contains a lot of scratches, damage layers, and contaminations introduced during wafer polishing process. Etching of SiC with hydrogen [1-4] has been used as one of effective in-situ methods in order to obtain atomically flat and clean surfaces. Surface morphology after hydrogen (or hydrogen contained C_3H_8 or HCl) etching at atmospheric pressure and at temperatures ranged from 1100 to 1620 °C has been investigated [3,4]. Pre-growth treatment at low pressure and at high temperatures is desirable when epitaxial growth is carried out at these conditions. However, it has not been reported yet. In this work, etch rate and surface morphology of hydrogen etched 4H-SiC at low pressure and high temperature are investigated.

EXPERIMENTAL

A vertical CVD reactor, which has a cold-wall quartz tube, was used for etching. SiC substrates on a high purity graphite susceptor (not SiC-coated) were heated by radio-frequency induction. Pd-diffused hydrogen was used for etching. Argon or Ar + H_2 was also used for etching in order to examine the role of hydrogen. The substrates used were 4H-SiC (Si-face, 8° off) from Cree Research, Inc. Before loading into the reactor, the substrates were sequentially cleaned with acetone, dipped in 5%HF, and rinsed in deionised water. Etching was carried out for 30 min. at pressures of 2, 20, 100, and 760 Torr and at the temperature ranged from 1600 to 1850 °C. Temperature was measured with a calibrated pyrometer. The etched surfaces were examined with Nomarski differential interference contrast microscopy (NDIC) and AFM, and etch rates were determinated from the weight loss with microbalance.

RESULTS AND DISCUSSION

Figure 1 shows the relations between etch rate and reciprocal temperature at each pressure. There is an exponential relation between them. The activation energy was determined to be 94 ± 6 kcal/mole at all pressure conditions. Ghoshtagore has discussed decomposition of hexagonal SiC in argon ambient and has determined the activation energy to be 111.4 ± 16.5 kcal/mole [5]. Bartdorf et al. have reported the activation energy for free evaporation of silicon to be 104 kcal/mole [6]. Higher etch rate can be obtained at lower pressures rather than at atmospheric pressure. For

example, etch rate at 20 Torr is several times as high as the etch rate at 760 Torr. This result shows that the damage layer on substrate surface can be eliminated more effectively at lower pressures.

Figure 2 shows NDIC images before (a) and after etching at 2 Torr (b), 20 Torr (c), and 760 Torr (d). One can see a lot of scratches before etching [Fig. 2 (a)], and these are almost eliminated after etching at 20 Torr [Fig. 2 (c)] at the temperature ranged from 1600 to 1850 °C. Protrusions which have a hexagonal feature are observed at 2 Torr [Fig. 2 (b)]. Their size and density increases with increasing temperature. Triangular shaped defects extended in the direction of <1$\bar{1}$00> are also observed at atmospheric pressure [Fig. 2 (d)]. Their size and number of these triangular shaped defect increases with increasing temperature extending in the same <1$\bar{1}$00>

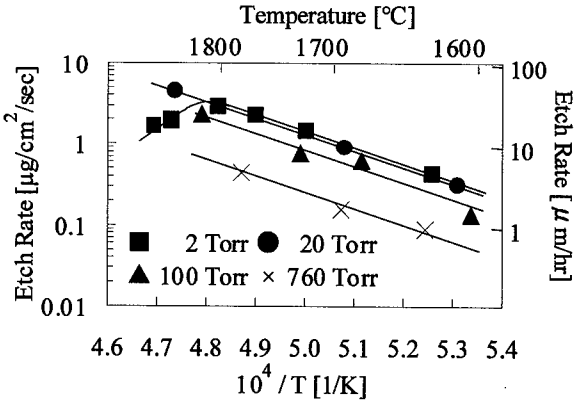

Fig. 1. Relations between etch rate and reciprocal temperature.

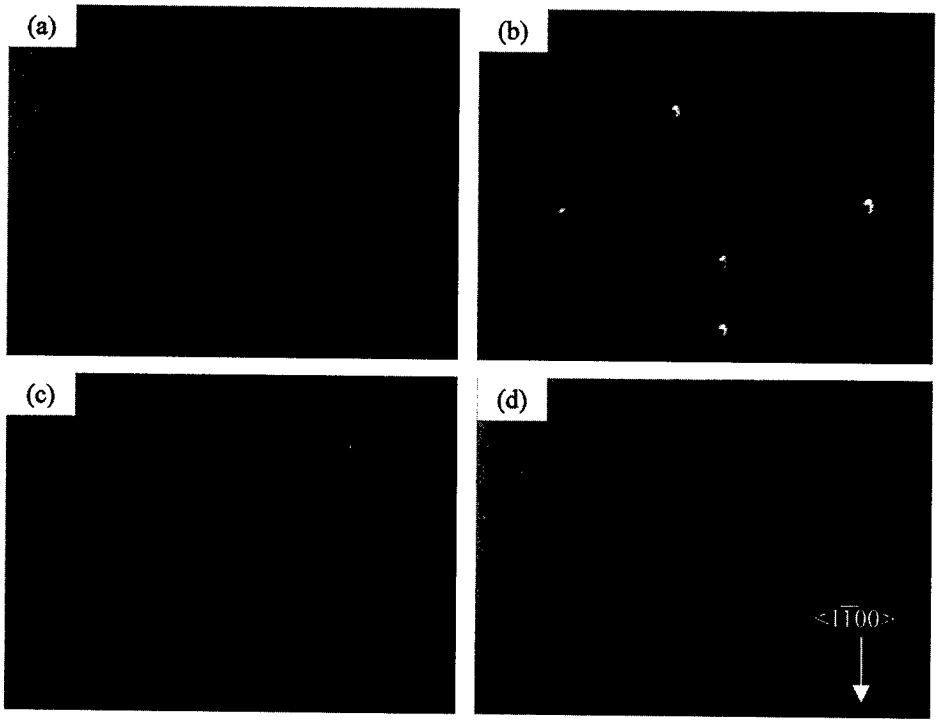

Fig. 2. NDIC images before (a) and after etching at 2 Torr (b), 20 Torr (c), and 760 Torr (d) (at 1700-1730 °C).

direction. These triangular shaped defects and protrusions are not observed at around 20 Torr.

Figure 3 shows AFM images of the same surfaces as in Fig. 2. The height of all the protrusions observed at 2 Torr is almost more than 1 μm. All of the protrusions are deformed in a

direction parallel to <11$\bar{2}$0> (substrate off-direction) [Fig. 3 (b)]. Etched mechanism involving surface steps on the off-substrate seems to influence the deformation of the protrusions. Therefore, the origin of the protrusions is not the flakes from the chamber wall, but may be microscopic re-crystallization or microscopic etching residues. Step like features structures are observed at 20Torr as shown Fig. 3 (c). Fig. 3 (d) shows the edge part of the triangular shaped defect observed at atmospheric pressure [Fig. 2 (d)].

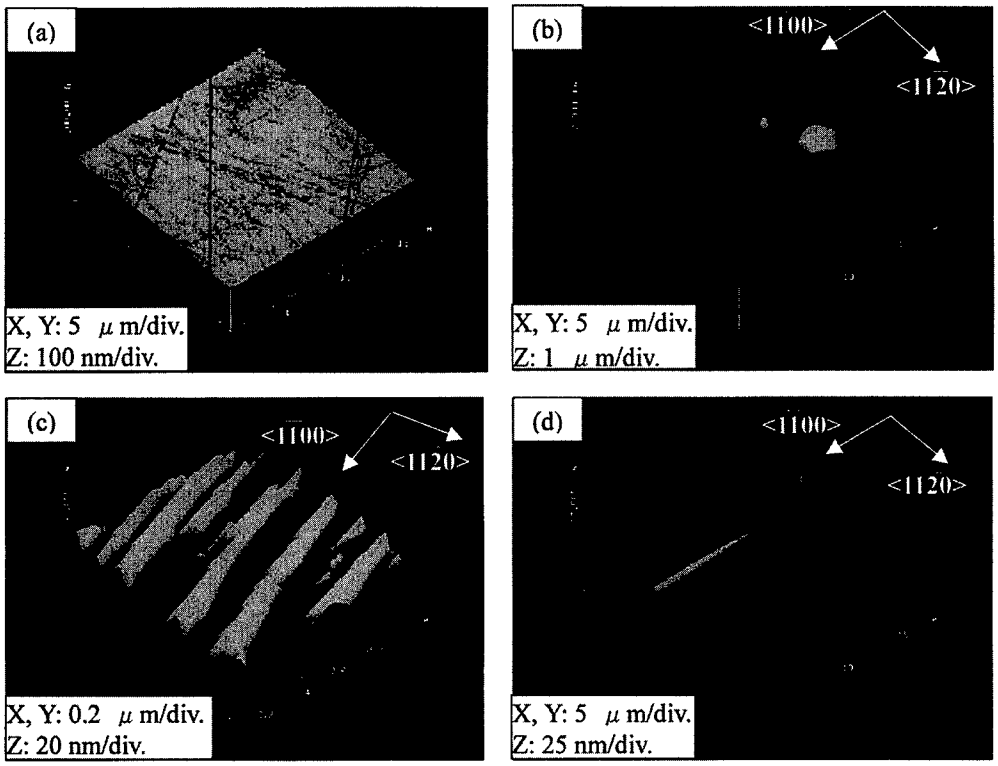

Fig. 3. AFM images before (a) and after etching at 2 Torr (b), 20 Torr (c), and 760 Torr (d) (at 1700-1730 °C).

Etch rate does not depend on H_2 flow rate within the condition of this experiment (Fig. 4). There may be enough amount of hydrogen to react on the surface of the substrate.

Etching in argon ambient was also examined. The etch rate was less than the detection limit of microbalance and was much lower than that of hydrogen etching. Figure 5 shows NDIC images after etching in argon ambient at 20 Torr. The surface after argon etching is rough and is different from that of hydrogen etching. This indicates that hydrogen has an important role in etching reaction and in order to obtain a smooth and

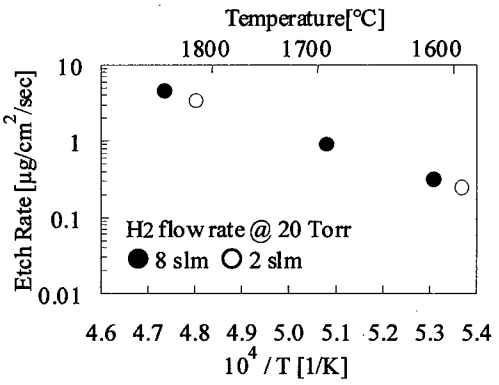

Fig. 4. Etch rate dependence on H_2 flow rate at 20 Torr.

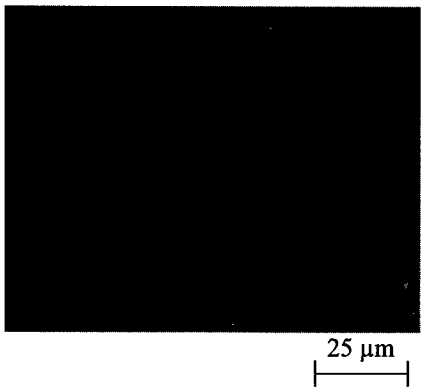

Fig. 5. NDIC images after Ar etching at 20 Torr at 1700 °C.

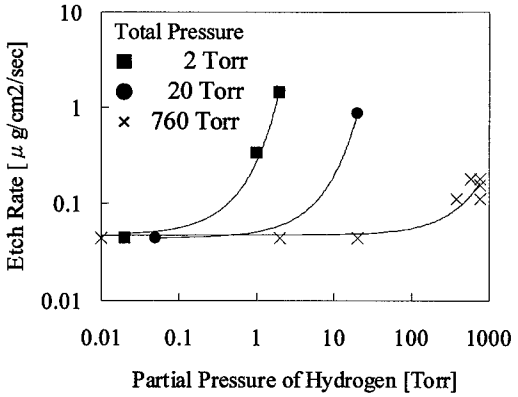

Fig. 6. Etch rate dependence on partial pressure of hydrogen in argon at 1700 °C.

specular surface.

Figure 6 shows the relation between etch rate and partial pressure of hydrogen in the gas mixed with argon and hydrogen. Etch rate is very low in the region of lower partial pressure of hydrogen and increases rapidly with increasing partial pressure. Morphology of the surfaces is rough when etched at low etch rate and low pressure. And it looks like the same morphology as that of argon etching (Fig. 5).

Kumagawa et al. have explained the etching mechanism of SiC by the following three reactions [2].

$$SiC(s) = Si(l) + C(s) \quad (1)$$

$$2C(s) + H_2(g) = C_2H_2(g) \quad (2)$$

$$Si(l) = Si(g) \quad (3)$$

The lower etch rate at low partial pressure of hydrogen may be attributed to the suppression of reaction (2) and to the surface residue of carbon decomposed by the reaction (1). In order to explain the etch rate dependence on total pressure, it is necessary to take into account further the transport mechanism.

SUMMARY

Etch rate and surface morphology of hydrogen etching on 4H-SiC at low pressure and at high temperature have been investigated. Smooth and specular pre-growth surface can be obtained by etching at around 20 Torr and at temperatures ranged from 1600 to 1850 °C. Higher etch rate is obtained at low pressures. The activation energy of hydrogen etching is determined to be 94 ± 6 kcal/mole and does not depend on pressure. Defects such as hexagonal shaped protrusions and triangular shaped defects are observed by etching at 2 Torr and atmospheric pressures, respectively.

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SiC In-Situ Pre-Growth Etching: A Thermodynamic Study

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Keywords: Epitaxy, Etching, Thermodynamic Study

Abstract

A thermodynamic study has been done to understand the impact of the temperature, the pressure and the composition of the gas mixture during SiC pre-growth etching. It is shown that H_2 etching can lead to the formation of a solid silicon phase. Varying the temperature, the formation of this Si phase can be avoided. The influence of added C_3H_8 to H_2 has also been investigated. It is found that the formation of Si droplets can be eliminated. To complete the study, experiments have been performed in a horizontal CVD reactor. The results are in good agreement with the thermodynamic approach. Etch rates have been deduced from infra-red reflectivity measurements.

Introduction

SiC is a promising material for high temperature and high power applications. SiC microelectronic devices are beginning to enjoy more success but are still impeded by insufficient crystal quality. For instance, Schottky diode characteristics are strongly affected by the surface roughness of the epitaxial layer [**1**]. Indeed, SiC surface polishing is not sufficiently mastered to avoid scratches and additional etching has to be done in order to remove these defects. Up to now, neither wet chemical etching at low temperatures, oxidation or reactive ion etching can result in good surface preparation. Most of the time, *in-situ* etching has to be done before epitaxial layer growth.

In this work, a thermodynamic study is made to understand the impact of the temperature, the pressure and the composition of the gas mixture for SiC etching. The results are compared with experiments.

Thermodynamic study

The heterogeneous equilibrium of the Si-C-H system has been determined using the software « mélange / Gémini » [**2**] with thermodynamic data developed by Allendorf [**3,4**] and completed by Aubreton [**5**].

i) H_2 etching

The thermodynamic study of the SiC etching in a H_2 ambiant with T=1685 K and P=1 atm ends in the formation of gaseous species such as CH_4 for the C-containing species and SiH_2, SiH_4, SiH , Si_{gaz} and Si in solid phase for the Si-containing species. By the etching, the quantity of the gaseous C-species formed (mainly CH_4) is three times higher than the gaseous Si-species one. So, there is Si in excess which is condensed at the SiC surface in a solid or liquid phase depending whether the etching temperature is higher or below the Si melting temperature.

The influence of temperature on the created species is shown in Fig.1. At low temperature, the amount of CH_4 produced is high compared to the Si species one : there is a high quantity of

condensed Si. Over 1600 K, the proportion of SiH_2,SiH and Si_{gaz} increases with temperature : the difference between C and Si species created is lowered so that the amount of condensed Si decreased. Over 1750 K there is no more condensed silicon created and as a consequence the etch rate increases. Then, an etching at high temperature should prevent the formation of condensed silicon while increasing the etch rate.

The influence of pressure between 0,1 and 1 atm on a H_2 etching at 1685 K has also been studied. These results are shown in fig 2. At low pressure (0.35 atm) the etching of SiC doesn't lead to condensed silicon because concentration of Si-species and C-species created by the etching are equal. Over 0.35 atm the difference between the amount of C and Si-species formed widens drastically with temperature and condensed silicon appears. On the other hand, at low pressure, the quantity of created species decreases and this means a diminution of the etch rate.

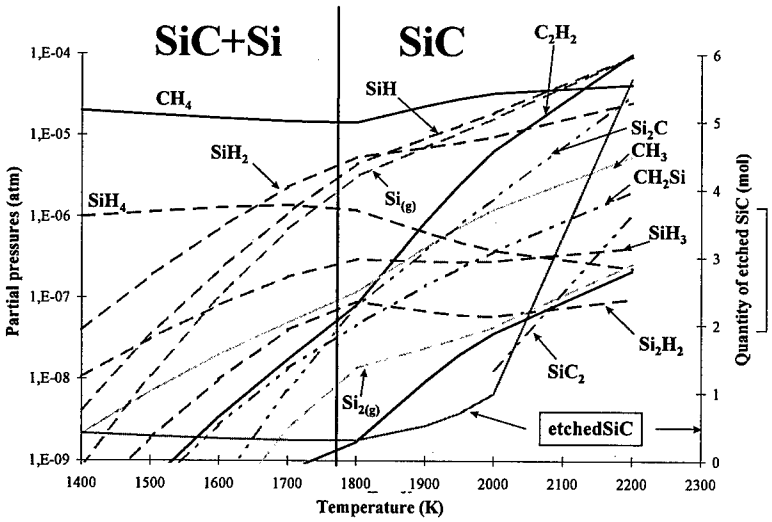

Fig 1. Heterogeneous equilibrium of the SiC - H_2 system under 1 atm. Species created by the etching are represented as a function of the temperature.

ii) $H_2 + C_3H_8$ etching

At 1685 K and 1 atm, the $H_2+C_3H_8$ mixture has been studied. The addition of propane is used to avoid the formation of condensed silicon by limiting the creation of C species by the SiC surface decomposition. On Fig.3, we can see the influence of the quantity of add-propane on the etching (1 atm - 1685K) and the different solid phases formed. We can distinguish three parts :

-Zone I, there is condensed silicon because the « add-CH_4 » concentration is negligible compared to the CH_4 created by the etching. The addition of propane has a weak influence and in this zone the etching is similar to a pure H_2 etching.

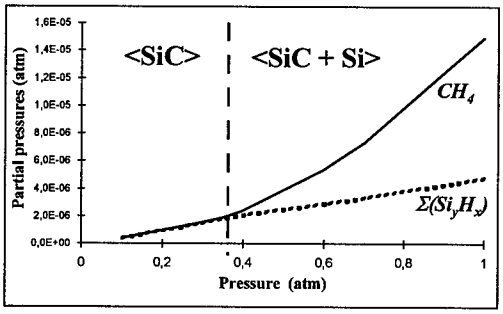

Fig 2. Heterogeneous equilibrium of the SiC - H_2 system at 1685K. Species created by the etching are represented as a function of the pressure.

-Zone II, the increase of the CH_4 partial pressure due to the decomposition of propane involves a diminution of the CH_4 created by the etching. The formation of condensed silicon is prevented but as the C and Si species created by the decomposition of the SiC surface is slowed down, the etch rate is then reduced.

-Zone III, In the third part, the partial pressures of the CH_4 and C_2H_2 saturate, the excess of carbon introduced by the propane is deposited as a solid phase.

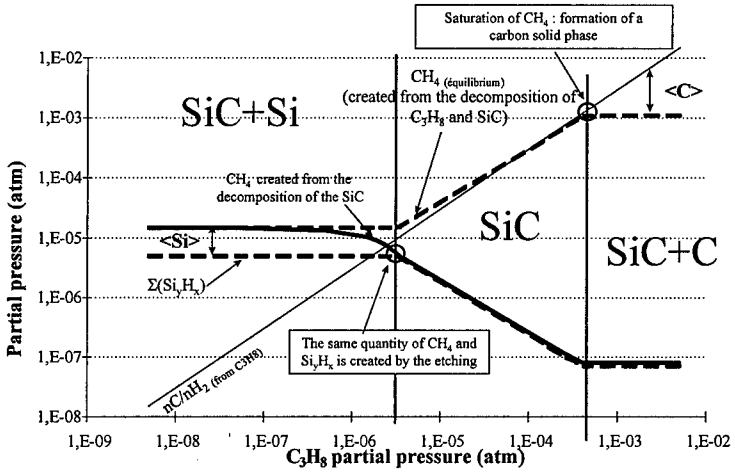

Fig 3. Influence of the quantity of carbon added by the propane on the heterogeneous equilibrium of the SiC-H_2-C_3H_8 system - 1685K and 1 atm.

Experiments

Experiments are done in a horizontal cold wall CVD reactor. SiC coated susceptors are used in order to prevent C-species coming from the graphite susceptor.

i) H_2 etching

The etching of SiC (4H or 6H) at 1700 K, 1 atm and with only H_2 leads to the formation of the defects shown in Fig 4.

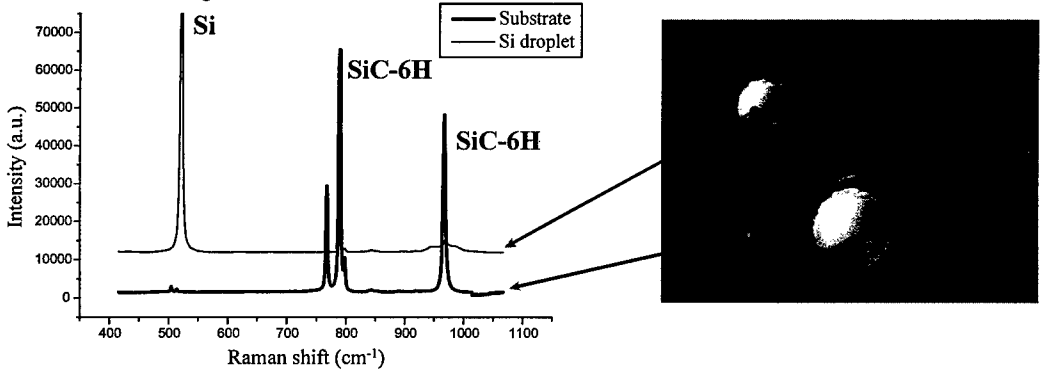

Fig 4. Optical Micrograph of SiC surface etched with H_2 at 1700 K under 1 atm, showing silicon droplets. The Silicon phase is identified by Raman spectroscopy.

These defects are like drops with a 10 microns diameter and are 1 μm high. In a Raman spectra done on this defect, we can see the 521 cm^{-1} band typical of crystalline silicon. Liquid drops induced by the H_2 etching condensed at the SiC surface during the final cooling step of epitaxy.
A probable reaction between the SiC surface and the silicon droplets during their formation creates the circle-shaped defects under the droplets (see fig 4). Their analysis have shown Si- rich SiC regions. When two much droplets are present at the SiC surface they coalesce and crystallize with a dendrite shape. The formation of Si-droplets, circle-shaped defects and dendrites can occur during the same etching step. The density of defects is higher on the edges of the substrate : this might be due to a SiC-coating susceptor contribution and the worse quality of the substrate at the edge [6].
The etch rate has been measured by infra-red reflectivity. H_2 etching at 1700 K under 1 atm removes 80 nm/h (for SiC-4H). This rate is not high enough to remove surface defects such as scratches or pits. SiC etched with H_2 at 1820 K (1 atm) exhibits a surface without Si-droplet (as predicted). At this temperature, the etch rate is also 80 nm/h : between 1700 and 1820 K, the temperature has a weak influence on the etch rate. All these results are in perfect agreement with the thermodynamic approach.

ii) H_2+C_3H_8 etching
We have verified that the use of propane with H_2 avoids the formation of Si-droplets. With the adding of C_3H_8 (0,02 % in H_2), the surface doesn't exhibit any defect and is « mirror-like ». When the C_3H_8 exceeds 0,2 % in H2 , there is a graphitization of the SiC surface. The etch rate of SiC with a H_2 + C_3H_8 (0,02%) mixture was measured to 8 nm/h. As predicted, the use of propane slows down the etching of SiC.
The experimental domain where Si or C deposition is avoided (between 0,02 and 0,2 %) has the limits shifted compared to those found by thermodynamic calculations (between 0,0003 and 0,04 %). This can be easily understood since kinetics, surface reactions, and reactor design are not taken into account.

Conclusion
For the etching of the SiC, thermodynamic calculations and experiments were performed varying the temperature, the pressure and the etching gas .
The H_2 etching leads to the formation of Si-droplets. This can be avoided by reducing the pressure (which decreases the etch rate) , increasing the etching temperature (which increases the etch rate but reduce the susceptor lifetime). Another solution is to add C_3H_8 to the etching gas. Experiments and thermodynamic calculations are in good agreement even though some limits are shifted. Etch rates were measured showing that in situ etching is not sufficient enough to remove the polishing defects. Previously, a material removing has to be done by oxidation or etching step. Taking into consideration those results, the best compromise can be chosen to achieve a high quality etching.

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The Effect of In Situ Surface Treatment on the Growth of 3C-SiC Thin Films on 6H-SiC Substrate - An X-ray Triple Crystal Diffractometry and Synchrotron X-ray Topography Study

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Keywords: 3C-SiC/6H-SiC, In Situ Surface Treatment, Synchrotron X-ray Topography, X-Ray Diffraction

Abstract

The effects of three in-situ pre growth substrate treatments on the quality of 3C-SiC epitaxial films on 6H-SiC(00.1) were evaluated by high resolution x-ray diffraction, synchrotron x-ray topography, atomic force microscopy, and optical microscopy. The Si-face substrates were etched in pure H_2, C_2H_4/H_2, or 0.5% HCl/H_2 mixtures to remove scratches and subsurface polishing damage prior to the 3C-SiC epitaxy by chemical vapor deposition. The dislocation density in the 3C-SiC thin films was estimated from the full width at half maximum (FWHM) of the x-ray diffraction rocking curves for a number of symmetric and asymmetric reflections. Etching in either C_2H_4 in H_2 or HCl in H_2 was more effective at producing smooth substrate surfaces than etching in pure H_2. The 3C-SiC films subsequently deposited on the smooth surfaces had shown a factor of ten reduction in the dislocation density compared to films deposited on substrates without pre growth surface treatments. The smoothest substrate surfaces produced the largest 3C-SiC domains and the lowest defect densities. Synchrotron x-ray topography of selected samples revealed cellular structure of dislocations, low angle grain boundaries and double positioning boundaries in the 3C-SiC films.

Introduction

Silicon carbide is an excellent semiconductor for the fabrication of high power and high frequency devices. Its most distinctive characteristic is its ability to form many different polytypes; structural variations in the stacking sequence of it close-packed basal (00.1) planes, each of which has different energy band gaps and electron mobilities. Control of the polytype is an important issue in the epitaxy of SiC, both to eliminate unintentional polytype inclusions and to intentionally form specific polytype heterojunctions to create band edge discontinuities for device applications. The majority of efforts to control polytype formation in epitaxy has been with 3C-SiC/6H-SiC [1,3].

A major problem with the heteroepitaxy of 3C-SiC on 6H-SiC substrates is the high density of double positioning boundaries (DPBs), thus the key goal of the present research was to determine which pre-growth treatment produces the largest area domains and the lowest defect densities. Powell *et al* [3] showed that nearly pure 6H-SiC epitaxial layers could be achieved on on-axis 6H-SiC substrates by first etching the substrates in a HCl/H_2 mixture at 1375 °C before deposition. By intentionally scratching the etched substrates prior to growth, 3C-SiC epitaxy could be intentionally induced. The 3C-SiC deposited on substrates etched in this manner contained fewer defects compared to 3C-SiC deposited on substrates as received from the manufacturer. Powell *et al* [3] attributed the formation of 3C-SiC to residual subsurface polishing damage in the 6H-SiC wafer. By removing this damage, 6H-SiC became the dominate polytype deposited. Since as-received 6H-SiC substrates typically contain a high density of surface damage, removing scratches and subsurface damage by pre growth etching techniques can have a pronounced effect on the 3C-SiC epitaxial growth domain sizes.

Previous studies on the effect of pre-growth etching on epitaxial layer quality focused on

homoepitaxy, that is, 6H-SiC on off-axis 6H-SiC substrates [4-10]. The present study differs from prior work by concentrating pre-growth etching of on-axis 6H-SiC substrates, with the goal of improving the 3C-SiC epitaxial layer subsequently deposited. The goal is to improve the crystal quality of the 3C-SiC without eliminating its formation altogether.

Experimental

The substrate etching and epitaxial 3C-SiC film growth were carried out in a cold wall horizontal quartz reactor operated at atmospheric pressure. The substrates were heated with a pyrolotic boron nitride coated graphite, resistantly heated susceptor. All films were deposited on silicon-face, 6H-SiC (00.1) substrates at a temperature of approximately 1400°C. The conditions for film deposition were 0.5 sccm SiH_4 and 0.5 sccm C_2H_4 (a C/Si ratio of 2.0) in 6000 sccm H_2 carrier gas. The etching conditions for each sample are summarized in Table 1. The standard in-situ pre growth cleaning procedure was to heat the substrate in 3000 sccm H_2 for 10 minutes (as in the case of sample number one and two); no etching occurs at this temperature. A Blake Industries high resolution triple crystal diffractometer with the $CuK\alpha_1$ was used for the x-ray analysis [11]. The second slit size was 1 mm by 2 mm and the detector was kept wide open. The structure, strain and dislocation density were obtained using a combination of symmetric and asymmetric reflections. The synchrotron radiation topography experiments were carried out at the Stanford Synchrotron Radiation Laboratory, Stanford, CA. The grazing incidence topographs were taken in reflection using monochromatic radiation and selecting a particular wavelength such that the incident radiation makes an angle of 0.5° with the sample surface. Images were recorded in high resolution Kodak SR1 type films for all topographic work.

Results and Discussions

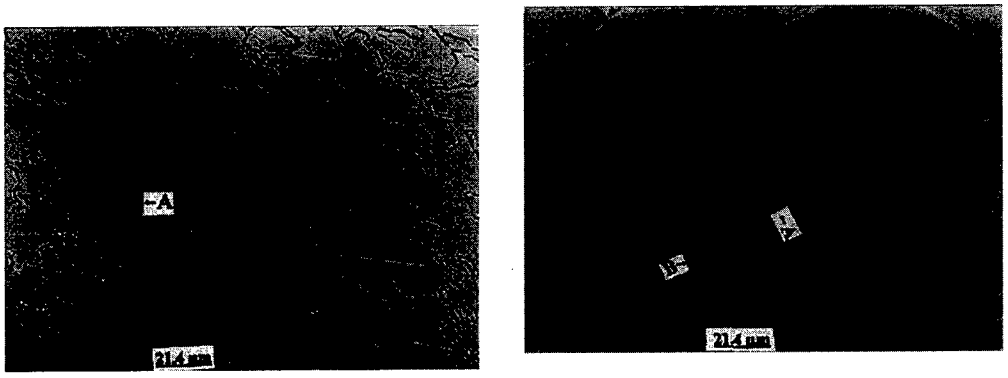
The AFM image of 6H-SiC substrates as-received or etched at 3000 sccm H_2 for 10 minutes on-axis Si-face 6H-SiC substrate shows polishing induced randomly oriented scratches, varying in depth (up to 10 nm) and width (up to 200 nm). However, after in-situ pre growth etching treatment, the scratches began to disappear, and a periodic texture mainly along the $[1\bar{1}.0]$ direction of roughly parallel ridges or terraces are formed. The surface roughness in most cases after etching is below 1 nm. The step heights in etched substrates varied from 0.5 to 1.5 nm which corresponds to two-six SiC bi-atomic layers. Etching in C_2H_4/H_2 and HCl/H_2 produced more regular step and terrace patterns than etching in H_2 alone. The addition of C_2H_4 and HCl into H_2 can also suppress formation of Si droplets.

Table I: Pre-growth etching conditions and roughness in the substrate.

Sample No.	H_2 (sccm)	C_2H_4/H_2	HCL/H_2	Temp.(°C)	Time (mins)	Roughness (nm)
1	3000			1130	10	1.52
2[1]	3000			1130	10	1.52
3	6000			1400	30	0.70
4	6000			1400	30	0.98
5	6000	$2x10^{-5}$		1400	30	0.43
6	6000	$1x10^{-4}$		1400	30	1.74
7	6000		0.5%	1400	10	0.78

[1]substrate research grade

The surface morphologies of the as grown 3C-SiC films were investigated with a Nomarski optical microscope. Typical surface morphologies found were anti-phase domain boundaries, steps, cubic symmetry and stacking faults. As shown in Figures 1 (a) and (b), anti-phase domain boundaries



(a) (b)

Figure 1. Optical microscope photomicrograph from the epitaxial film from selected samples, magnification 700x (a) from the sample number two (cleaned in pure H_2 at low temperature (1130°C)) and (b) from the sample number five (etched in C_2H_4/H_2), (A) anti-phase domain boundaries and (B)stacking faults.

in a C_2H_4/H_2 etched sample are approximately 4.6 times larger as compared to those in the un-etched sample. Triangular defects found in Figure 1 (b) are caused by the nucleation of an initial triangular stacking fault on the (111) plane parallel to the substrate/epilayer interface.[1]

Table II summarizes the results on the full width at half maximum (FWHM) of different symmetric and asymmetric reflections and dislocation density. The FWHM of the rocking curve for the (111) reflection from the film in the sample number seven was only 11 arc sec which was much lower than that from the substrate symmetric reflection. The dislocation density is high in those films which are grown on un-etched substrate and is reduced by etching treatment. C_2H_4/H_2 and HCL/H_2 etchants are more effective than H_2 alone in reducing dislocations. The dislocation density was reduced approximately by a factor of ten when either of these two etchants were used as compared to un-etched sample. Formation of regular terraces might be responsible in reducing defect density.

Figures 2 (a) and (b) shows the synchrotron monochromatic radiation x-ray topography from the substrate and film, respectively, which is typical in all the samples. The defects in the substrate revealed are low angle grain boundaries and cellular structure of dislocations and are continued in the film. The additional defect shown in Figure 2 (b) is double positioning boundary.

Table II: FWHM and dislocation density in 3C-SiC films

Sample No.	FWHM/√π						Dislocation Density
	11.1	22.2	33.3	11.3	22.4	11.5	(X $10^8/cm^2$)
1	67	123	365	270	345	171	1.22
2[1]	88	103	236	114	145	224	1.24
3[2]	80	113	201	57	112	148	1.85
4	33	46	133	89	161		0.94
5	29	89	171	67	137	264	0.34
6	33	46	112	45	89	124	0.15
7	11	46	135	50	104	135	0.19

[1]substrate research grade, [2]with Si droplet

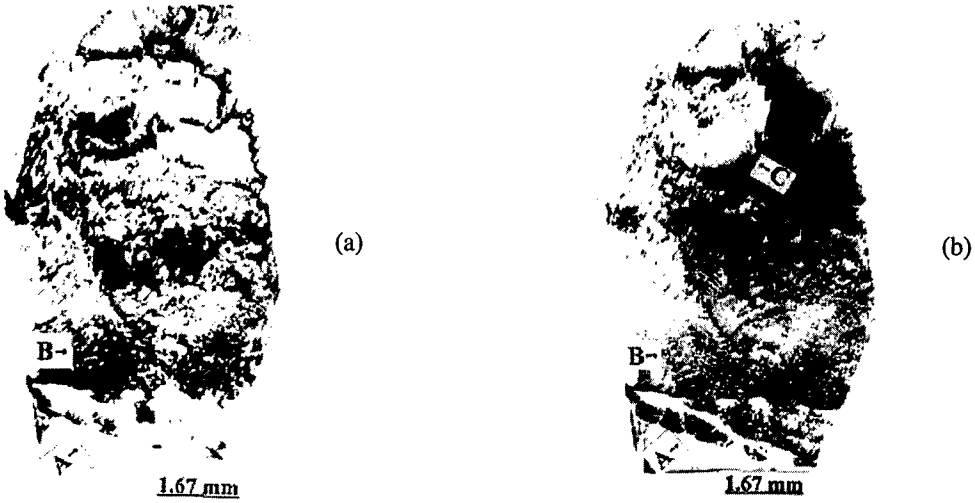


Figure 2. Synchrotron monochromatic x-ray radiation grazing incidence topography in reflection from the sample number one, $\lambda = 1.31$ Å; (a) from the 6H-SiC substrate, (01.10) reflection, and (b) from the 3C- SiC film, (113) reflection, (A) low angle grain boundary, (B) cellular structure of dislocations and (C) double positioning boundary.

Conclusions

AFM, optical microscopy, high resolution x-ray diffractometry and synchrotron x-ray topography were used to investigate the effect of pre growth in-situ surface treatment of the 6H-SiC substrate on the quality of 3C-SiC thin films. The etchants used were either 6000 sccm H_2, or C_2H_4/H_2, or HCL/H_2. The scratches were removed and the surface became smoother after etching as it was shown by AFM. The dislocation density was slightly reduced when H_2 etching was used, whereas it was reduced by a factor of ten when C_2H_4/H_2 or HCL/H_2 etching was used. Formation of smoother substrate surface with regular steps might assist in growing better quality films. Defects as revealed in selected samples by synchrotron x-ray topography were cellular structure of dislocations, low angle grain boundaries and double positioning boundaries.

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Materials Science Forum Vols. 338-342 (2000) pp. 1049-1052

Dry Etching and Metallization Schemes in a GaN/SiC Heterojunction Device Process

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Keywords: Gas Switching, HBT, ICP, RIE

Abstract. Dry etching and metallization schemes are described for a GaN/SiC heterojunction. GaN was reactive ion etched in a chlorine based chemistry (Cl_2/Ar), and an ICP etch was used on 4H-SiC using a fluorine based chemistry (SF_6/Ar/O_2). The etch rates obtained on GaN was above 400 nm/min. High sample temperature from self heating and large dc-bias was the probable cause for the high etch rate. The ICP etch rate on SiC approached 320 nm/min, and the etch selectivity to GaN was >100. The metallization was based on Ti for both n-GaN and p-SiC. TLM and Kelvin structures were used to extract the specific contact resistivity, ρ_C. After a 950 °C anneal in N_2 ρ_C on the GaN samples were below $1 \cdot 10^{-6}$ Ωcm^2 for sputtered contacts in room temperature, and an order of magnitude higher with evaporation. On p-SiC no ohmic behavior was found with a doping of $4 \cdot 10^{18}$ cm^{-3}, but the same contact metallization on highly doped areas (>10^{20} cm^{-3}) showed ohmic behavior with ρ_c below 10^{-4} Ωcm^2.

Introduction

The use of heterojunctions between GaN and SiC in devices are quite unusual. Some results have been reported with heterodiodes (HD) and heterojunction bipolar transistors (HBT) [1-3], but these devices have problems, especially with short life times in p-type SiC and only moderate lattice match between GaN and SiC (~3 %). The lattice match can be improved by using AlGaN since a higher aluminum content improves lattice match and increases the bandgap.

In this work we have developed a process sequence for a GaN/4H-SiC HBT. High density plasma etching used in inductively coupled plasma (ICP) or electron cyclotron resonance (ECR) systems has proven to be efficient when etching SiC and GaN with fluorides and chlorides respectively. In a combined process sequence the etching of SiC in the GaN etch should be minimized and vice versa. Metallization schemes for p-SiC and n-GaN often include high temperature rapid thermal anneals and when combining these schemes problems occur regarding annealing temperature, annealing time, and contact metal.

Experimental

Etching and Ohmic contacts for GaN structures were investigated for both MBE grown GaN and CVD grown AlGaN with an aluminum content of approximately 10 %. The GaN was unintentionally doped with a carrier concentration around $5 \cdot 10^{18}$ cm^{-3}, and the AlGaN was Si doped to approximately $2 \cdot 10^{18}$ cm^{-3}. Both nitrides were grown on a p-type (Al-doped to $4 \cdot 10^{18}$ cm^{-3}) 4H-SiC epi-layer with a 100 Å low temperature grown GaN buffer and a 120 Å AlN layer for GaN and AlGaN respectively. The nitride layers were patterned with photoresist and etched in a diode RIE. The flowrates and gases used were 200 sccm of Cl_2 and 50 sccm of Ar. The process pressure was adjusted to 150 mTorr to reduce the dc-bias, which was around –500 V at 100 W of RF power.

The SiC etch characterization was mainly performed on n-type bulk 4H-SiC purchased from CREE Research, and was patterned with photoresist or Al. An ICP system was used with SF_6 as the reactive fluoride and oxygen or argon were investigated as additional gases. Gas switching between low O_2 or Ar and high O_2 percentage was tested to improve selectivity to the Al mask. In Table 1 the SiC etch parameters are summarized and if nothing else is stated these parameters were used. The etched step heights were measured using a Tencor stylus profilometer and the etched surfaces were inspected by

SEM. Since all equipments used were designed for 4" processing, the samples had to be attached to a 4" silicon wafer using hard baked photoresist. The contact studies were mainly performed on the p-type epi-layer exposed to the GaN etch. An additional contact study was made on a highly doped p-type 4H-SiC epi layer (>10^{20} cm^{-3}). All the samples were dipped in HF prior to metal deposition. The contact anneals were performed in an RTA furnace for 30 s at 950 °C. Contact resistivities and sheet resistances were extracted using TLM and Kelvin measurements at elevated temperatures.

Table 1. Summary of the conditions in the SiC ICP etch.

Parameter	Standard with O_2	Switched (15 s / 7 s)
Chuck power [W]	50	50 / 50
Source power [W]	600	600 / 600
Pressure [mTorr]	5	5
SF_6 [sccm]	21	25 / 5
O_2 [sccm]	9	0 / 25
Ar [sccm]	0	5 / 0

The metallizations were done using both evaporation and sputtering of Ti. The sputtering was performed in a dc magnetron sputter, and the power was 2 kW, temperature 100 °C, argon flow 70 sccm and the pressure 5 mTorr. On GaN 900 Å the Ti deposition was followed by lithography, Ti metal etch (NH_3:H_2O_2 1:3), contact anneal, and on top a fresh ~0.7 µm Ti layer to lower the metal sheet resistance followed by lithography. On the AlGaN sample Ti was first deposited as described above, after this the sputter gas flow was changed to 70 sccm Ar and 50 sccm N_2, the power was reduced to 1 kW, and the temperature set to 150 °C to enable TiN deposition. This step was followed by lithography, Ti metal wet etch and the same contact anneal.

The evaporation was done in an electron beam evaporator with a base pressure of ~10^{-6} Torr and resulted in 1000 Å of Ti on GaN and 4H-SiC. Lithography, Ti wet etch and contact anneal were performed as described above.

Etch results

The nitride investigations were limited due to few samples and limited thickness of layers. However, satisfactory smoothness was achieved with fast etch rates up to 4500 Å/min, which are higher than previously reported for RIE systems [4-6]. This is probably due to self heating of the wafers and samples along with a high dc-bias, unfortunately the temperature can only be roughly estimated between 200 and 300 °C. The photoresist mask was burned and needed to be removed by a strong resist remover (H_2SO_4:H_2O_2 2.5:1). It has been shown that elevated temperatures increase the etch rate in ECR etching of GaN [7], and possibly the temperature dependence is stronger for RIE etching because of the lower Cl^- and Cl^0 density. In [4] a detailed description is given of important physical parameters influencing the etch rate, e.g. boiling point of 201 °C for the residual $GaCl_3$ and the GaN binding energy of 8.92 eV. The boiling point is an indication of the desorption temperature dependence and the binding energy can contribute to the thermal activation of a reaction limited etch process. In [8] the thermal activation of AlN wet etching was 15.45 eV compared to the AlN binding energy of 11.52 eV. The GaN to SiC selectivity was only 4 probably due to the high dc-bias and the strong self heating. However, the selectivity should increase with a more controlled etch process. Studies of Cl_2 ICP etching showed an etch rate of only 200 Å/min and up to 6000 Å/min for SiC and GaN respectively, with similar plasma conditions (i.e. a selectivity of 30) [9, 10].

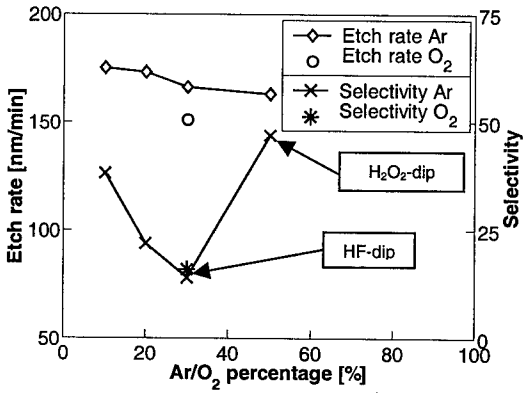

Figure 1. Etch rate and selectivity versus Ar or O_2 percentage.

The role of oxygen is still unclear in SiC etching. In ref. [11] the maximum etch rate was found at 40 % O_2 in a CF_4 plasma. Refs. [12] and [13] showed increased etch rate with decreasing O_2 percentage in SF_6 plasma and using Ar instead of O_2 generally increased the etch rate. In ref. [14] the same correlation with O_2 percentage and little change between Ar and O_2 in NF_3 plasma was reported. The role of oxygen seems to depend on the reactive gas (SF_6, NF_3 or CF_4) and on RF platen (chuck) power. In this study the etch rate was higher with Ar than O_2 by approximately 10 %.

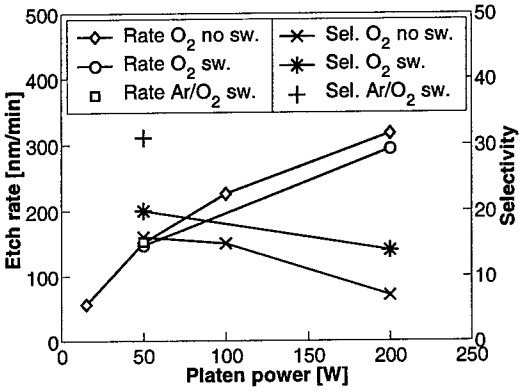

Figure 2. Etch results with switching and w/o switching versus platen power.

Photoresist can almost be ruled out as mask material when etching deeper than 1 µm since the selectivity was below 0.4, and an alternative mask material is needed. Here Al was used because of the well developed deposition and patterning techniques. The role of oxygen in the plasma again enters the scene since Al can oxidize and the selectivity should then increase with O_2 percentage [15], but here an increase in selectivity was in fact found when using Ar instead of O_2. This can be explained by a strong dependence of the selectivity on storage time due to Al oxidation. The highest selectivity, ~50, was observed after Al oxidation in H_2O_2 at room temperature for 5 min. As comparison a sample was etched in 5 % HF for 1 min before etching, here the selectivity was 14. Fig. 1 and Fig. 2 shows the etch rates and selectivity to Al mask versus Ar/O_2 percentage and RF platen power respectively. The SiC etch rate increases almost linear with platen power and the selectivity to the Al mask drops with higher platen powers. To increase selectivity with high O_2 and reasonable etch rate gas switching was tested (used in micro-mechanical processing), where 17 % of O_2 or Ar was switched with 83 % O_2, see Fig. 2.

We expect the same etch characteristics on p-type material [14], and this was also confirmed by etching through a 1 µm p-type 4H-SiC epi-layer where an etch rate difference less than 1 % compared to n-type 4H-SiC was found.

The etched surfaces were smooth and features were sharp, see Fig 3. A tendency for trench effects can be noted however, this effect was not seen on the photoresist samples due to mask erosion. GaN was etched less than 100 Å when etching more than 1 µm SiC (i.e. a selectivity >100).

Contact results

The Ti Ohmic contact to GaN showed low contact resistivities, ρ_C, especially with sputtered Ti. The resistivity of the GaN layer was also low indicating a mobility around 500 cm^2/Vs. The Ti/TiN structure on AlGaN showed higher ρ_C and the epi layer had high resistivity indicating a mobility below 50 cm^2/Vs, see Table 2 for a summary of the results from the TLM measurement. Because of the extra mask step, Kelvin measurement was only done on the n-GaN sample with sputtered Ti, here ρ_C was $1.0 \cdot 10^{-5}$ Ωcm^2. The discrepancy with Table 2 can be explained with a poorly developed passivation technique and will be investigated further.

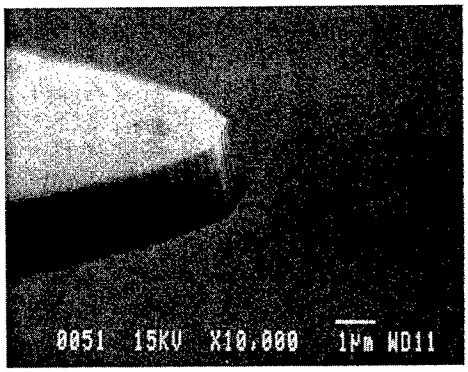

Figure 3. A SEM image of an etched feature. The bright layer is a charged p-type epi layer.

Ti based contacts have shown low ρ_C on p-type SiC but generally with longer Ar anneals and also with Al included in the contact [16-18]. Different

contact materials will only lead to more lithography steps, therefore not crucial to the combined metallization scheme. The annealing temperature, ambient, and time are of greater importance for compatibility with both SiC and GaN. The Ti contact on medium doped material showed rectifying characteristics, but on highly doped material Ohmic contacts were feasible, see the results in Table 2. The temperature dependence of ρ_C for all samples are shown in Fig. 4. The major advantage with the N_2 anneal is the formation of TiN on top, which has interesting properties regarding hardness, chemical stability and thermal stability [19].

Table 2. Summary of the contact resistivities at 25 °C, sp. means sputtered and ev. means evaporated contact.

Sample & contact	doping [cm^{-3}]	ρ_C [Ωcm^2] (TLM)	ρ [Ωcm] (TLM)
n-GaN, sp.	$\sim 5 \cdot 10^{18}$	$2.0 \cdot 10^{-7}$	$3.0 \cdot 10^{-3}$
n-AlGaN, sp.	$\sim 2 \cdot 10^{18}$	$1.3 \cdot 10^{-4}$	0.16
n-GaN, ev.	$\sim 5 \cdot 10^{18}$	$9.4 \cdot 10^{-6}$	$2.5 \cdot 10^{-3}$
p-SiC, ev.	$4 \cdot 10^{18}$	rectifying	
p-SiC, ev.	$>1 \cdot 10^{20}$	$6.0 \cdot 10^{-5}$	$4.2 \cdot 10^{-2}$

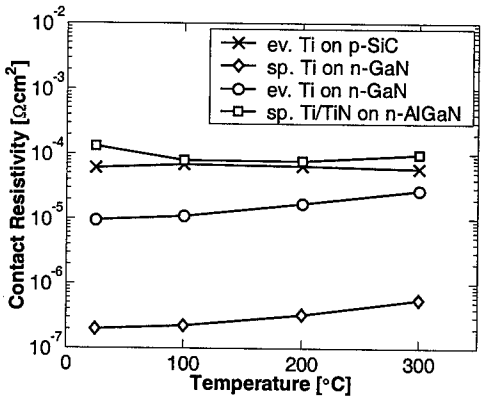

Figure 4. ρ_C versus temperature.

Conclusions

ICP etching in SF_6 of 4H-SiC has been investigated and etch rates up to 320 nm/min were measured. Oxidation of Al enhances the selectivity, and higher selectivities were found using Ar instead of O_2 in the plasma. A switched etch sequence between low and high oxygen percentages improved the Al selectivity. RIE etching in Cl_2 and Ar of GaN showed high etch rate but low etch selectivities over SiC (~4), but this was probably due to strong self heating and high dc-bias. High density plasma etching is believed to improve this selectivity considerably.

Ti contacts annealed in N_2 showed Ohmic characteristics on both GaN and AlGaN, where sputtered Ti on GaN had the lowest ρ_C. The same metallization showed rectifying characteristics on medium doped SiC, but low resistivity Ohmic contacts were achieved using highly doped material.

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Materials Science Forum Vols. 338-342 (2000) pp. 1053-1056

Demonstration of Deep (80μm) RIE Etching of SiC for MEMS and MMIC Applications

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Keywords: Etching, Isolation, Masking, MEMS, RIE

Abstract: For very deep etching of SiC, up to and exceeding 100 μm, which would be required for selected applications, no suitable process has been reported. The ideal process would optimize a combination of fast etch rate, absence of residue, good mask selectivity, sidewall control, and reproducibility. In this work, we compare five SiC etches used in commercial Reactive Ion Etch (RIE) systems with regard to the above criteria, and demonstrate the first 80 μm via etch in SiC using a Ni-alloy mask. The SiC etches examined are residue-free, and possess etch rates ranging from 8 nm/minute up to 235 nm/minute. The etches utilize one or more of the following fluorinated gases: NF_3, SF_6, or CHF_3. Several inorganic and organic mask materials have been evaluated with SiC:mask etch selectivity ranging from 10:1 to 160:1.

I. Introduction

Because of its high bond strength, the etching of SiC has been quite difficult and performed almost exclusively using dry etching techniques. Most techniques have utilized fluorinated gas chemistries in reactive ion etch (RIE), electrocyclotron resonance (ECR) etch, or inductively coupled plasma (ICP) etch systems. Residue free etches have been developed with etch rates from 5 nm/minute up to 350 nm/minute[1,2]. While most research on the etching of SiC has concentrated on etch rate and residue formation, there is no available data on the process development for deep trench or via etching. Deep etches are frequently needed in semiconductor technology for deep trench isolation of power devices, via's in advanced devices, and bulk micro-machining of micro-electromechanical systems (MEMS). Due to the high chemical inertness of SiC, however, most developed etch recipes with reasonable etch rates have low SiC to mask selectivity, which limits the feasibility of deep etching. This work focuses on the characterization of masking material and resultant deep etch development.

II. Experimental Setup

Two RIE systems were used. One system was a Drytek QUAD 480, with four individual etching chambers capable of simultaneous operation. Samples are loaded into an intermediate cassette chamber before entering an etching chamber to allow consecutive etches without having to break vacuum in the active chamber. The separation between RF and ground electrode was set at 2.54 cm, and the RF electrode was aluminum with an area of 161.3cm^2. The second system used was a PlasmaTherm model SL-720, with the SiC wafers loaded on a wafer tray capable of processing one 200 mm or four 50 mm diameter substrates simultaneously. The separation between RF and ground electrode was factory-set at 76 mm in this system. In both systems, all gases are computer-

controlled and fed into the chambers through mass flow controllers. A detailed characterization of our SiC etch process utilizing pure NF_3 plasma in the Drytek QUAD 480, with a discussion of etch rate and residue formation for various etching conditions, is given elsewhere[3]. The optimized chamber pressure and power level for maximum etch rate and minimized residue formation was determined to be 225 mT and 275 W, respectively. An increase in either pressure or power levels results in increased etch rates but at the expense of cleanliness. The self-induced DC bias ranged in value from 35 to 55 V. The NF_3 flow rate was held at a constant 90 standard cubic centimeters per minute (sccm), and was allowed to stabilize in the chamber prior to etching. The processes utilized in the second system (PlasmaTherm SL-720) utilized primarily CHF_3 or SF_6 based chemistries, and details for these processes have also been described elsewhere.[2,4,5] All etching experiments were performed on n-type (N-doped) 4H SiC samples with various doping levels.

III. Experimental Results

Aluminum

Due to its wide availability and high selectivity, aluminum was one of the most commonly used masking materials during initial investigations of SiC RIE etching. However, many researchers reported the development of micropiles on etched samples, caused by back-sputtering of aluminum from the mask, sample electrode, or even the chamber walls onto the etched surface. Al micropile formation can mask sub-micron areas throughout the active etch area and can result in extremely rough etch surface morphology. To reduce the potential for back-sputtering of the mask or electrode material, samples in the DryTek system were mounted on Si wafers to cover the surrounding electrode and the chamber pressure was increased to decrease ionic bombardment of the sample. This has proven effective in eliminating the Al micromasking effect, and etches have been demonstrated with high etch rates, anisotropic sidewalls, and no residue formation[4]. Samples in the Plasma-Therm system used similar techniques to eliminate residue formation.[2]

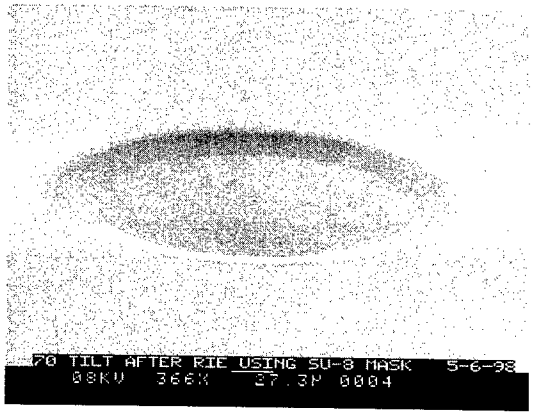

Fig. 1: SEM of a 7 μm deep tapered sidewall etch using a SU-8 photoresist mask.

Photoresist

The potential use of a photoresist mask for SiC is generally not recognized because the chemistry used to etch SiC generally etches photoresist at a high rate. However, thick photoresist films (>100 μm) are routinely used as a masking material in Si MEMs processing, using specially designed photoresist films. To investigate the possibility of using thick photoresist films for SiC trench etching, we utilized negative-tone photoresists, similar to the SU-8 described above, in both RIE systems. In the Drytek system with NF_3, over 10 samples were etched using our standard recipe, with a varying etch time from 5 to 90 minutes. The mask etch rate of ~1.1 μm/min was consistent over all samples. The selectivity, however, was not as high as expected relative to our standard Al mask etch. After photoresist removal, Dektak measurements showed only a 6.75μm deep trench for a 60 minute etch. The etch rate for this etch is 112 nm/min., which is 30% slower than our standard process. SEM characterization on samples etched with NF_3 showed a residue formation at the

bottom of the etched trench. We believe the decrease in etch rate is due to polymer formation from the photoresist mask. Samples masked with thick photoresist evaluated in the PlasmaTherm system with SF_6/O_2 gases exhibited a similar etch selectivity of ~ 0.1, although the etch rate was somewhat slower. Fig. 1 shows results of a 95 minute etch with SF_6/O_2 chemistry utilizing the thick SU-8 photoresist mask, resulting in a residue-free 7 μm deep etch. The lack of residue in the SF_6/O_2 sample clearly shows the effect of the oxygen additive.

ITO

The use of indium-tin-oxide (ITO) as a masking material for SiC RIE and ICP etching has been utilized by researchers as a solution for eliminating micromasking effects.[4] ITO films can be deposited by electron beam evaporation allowing controlled amounts of oxygen into the chamber while depositing the indium-tin alloy, or ITO targets are commercially available for sputter deposition of the film. The plasma etching of ITO is preferred over the use of highly corrosive acids, and is performed using either organic or halide-containing gases such as methane, Cl_2, HCl, HBr, HI, CCl_4, or CF_3Cl. Even with the use of these highly corrosive gasses, slow etch rates of 20-40 nm/min. are commonly reported for various RIE conditions. To evaluate the ITO etch selectivity in NF_3, we sputter deposited 200nm of ITO on silicon and masked the ITO with SiC samples. After etching the samples, the SiC masking samples were removed and the etch rate was determined from the step height. The SiC to ITO etch selectivity was greater than 30 for all of the etches (as shown in Table 2), but the selectivity was the highest in the NF_3 etch. A very low etch rate of 10 nm/min. was found for the samples in the NF_3 etch (selectivity of ~ 160). Since our pure NF_3 recipe does not contain compounds known to form volatile In and Sn compounds, we believe that the slow ITO etch rate is predominantly caused by ionic bombardment under the relatively low DC bias.

Nickel and Nickel Alloys

In the CHF_3 based etch, nickel, gold, and aluminum have all been used successfully as etch masks. For nickel, the SiC to mask selectivity is 30, which is the highest for the three metals investigated. Nickel, however, is a high-stress film that suffers from adhesion problems if the thickness is allowed to become too great. When using a lift-off process, nickel films in excess of 150 nm thick lifted up the photoresist during metal deposition, thus distorting the desired pattern. For 150 nm

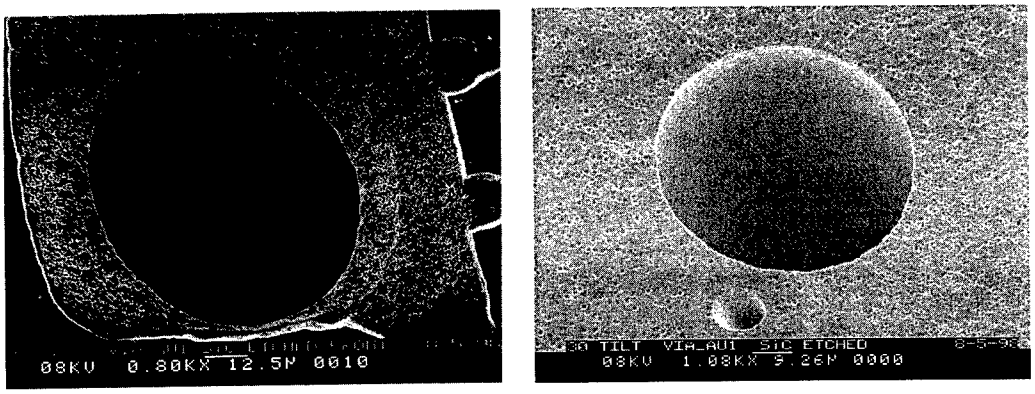

Fig. 2: SEM photograph of an etched via in an 80μm 4H-SiC wafer. The left photograph illustrates the exit point of the etch through the source pad of a device, while the right photograph illustrates the entry point of the via etch on the unpolished wafer backside.

Table 2: Summary of experimental results of SiC RIE etch mask materials.

Mask Material	Selectivity (NF_3)	Selectivity (SF_6/O_2)	Selectivity (CHF_3)
Al	17	-	-
SU-8	0.09-0.1	0.1	-
Ni	25	13	30
ITO	160	40	30

thick films, this limited the total etch depth to 4.5 μm. We found that by using a nickel alloy, rather than pure nickel, we were able to increase the nickel film thickness to nearly 5 μm. This nickel alloy was 98% nickel, with a small concentration of other constituents (magnesium and iron being the largest of the other elements). The mask thickness was increased via selective electroplating which prevented the stress of the film from pulling up the photoresist and distorting the pattern. The etch rate is unchanged from pure nickel, but adhesion problems did remain for thickness' above 5 μm. Using this thick Ni-alloy mask, we have successfully demonstrated a 80 μm deep anisotropic via etch using the pure NF_3 etch recipe. This is the deepest etch reported for SiC, and the first via etch completely through a SiC substrate. The via was etched in less than 6 hours, resulting in an average etch rate 235nm/minute. This etch rate is significantly higher than etch rates observed in shorter time etches (<1hour). It is believed that this increased etch rate is a result of increased substrate temperature, but further investigation of this effect is warranted. SEM pictures of this etch are shown in Fig. 2. Deep etches have also been performed in the CHF_3 based etch, although with much longer etch times. A summary of the mask selectivity for the three etches is contained in Table 2.

Summary

Deep etching of SiC is a critical process step in advanced device fabrication and future SiC MEMs applications. We have experimentally reviewed several potential masking materials (Ni, SU-8, ITO) for the deep RIE etching of SiC using two different commercial RIE systems. The use of thick photoresist masks shows potential for niche applications where sloped sidewalls would be advantageous, but further work is necessary to improve the selectivity while preventing the formation of polymer on the etched surfaces. Indium tin oxide masks have also shown excellent resistance to SiC etches, and are currently being investigated in deep SiC etching experiments. Initial investigations in using ITO as a masking material has shown excellent etch resistance and no signs of micromasking. Finally, we have demonstrated the deepest anisotropic etch reported for SiC, as well as the first via etch, through a 80 μm thick SiC wafer using a Ni-alloy mask. This important proof-of-concept etch is a key technological demonstration for SiC MEMs and SiC MMIC feasibility.

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Materials Science Forum Vols. 338-342 (2000) pp. 1057-1060

Reactive Ion Etching in CF_4 / O_2 Gas Mixtures for Fabricating SiC Devices

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Keywords: Accumulation Mode, MOSFETs, Reactive Ion Etching, RIE Rate, Surface Roughness, XPS

Abstract: CF_4/O_2 mole ratio dependence of the RIE rate of SiC, Si and C reveals the RIE rate of SiC is controlled by the sputtering rate of the constituent C atoms. The chemical reaction, which removes Si atoms from the reaction surface, contributes to flattening the surface. XPS analysis shows light etching (about 0.5nm depth) after the RIE removes residual impurities on the etched surface. An accumulation-mode MOS channel is fabricated by RIE. An effective mobility as high as $100cm^2/Vs$ is obtained, which indicates that a high quality MOS channel is fabricated using RIE in CF_4/O_2 gas mixtures.

1. Introduction

Reactive ion etching (RIE) is a crucial processing technique for the fabrication of SiC devices. Several researchers have investigated RIE of SiC to date [1], however, the etching mechanism and the nature of the etched surfaces are not fully understood. In this paper we investigate the etched surfaces by atomic force microscopy (AFM) and X-ray photoelectron spectroscopy (XPS). The effective mobility of accumulation-mode MOSFET fabricated using RIE is also reported.

2. RIE rate

In this work we used conventional RIE apparatus with parallel electrodes. The RIE in CF_4/O_2 gas mixtures was performed with a total gas flow rate of 50sccm, an O_2 mole ratio varied between 0 and 0.5, a total gas pressure of 0.1Torr and a rf-power between 100 and 300W. Figure 1 shows the RIE rates of 4H-SiC, Si and C (diamond) as a function of the O_2 mole ratio. It is well known that the RIE rate of Si depends strongly on the O_2 mole ratio. This is explained by the O_2 mole ratio dependence of the density of fluorine radicals that react with Si and form volatile species. The RIE rate of SiC increases slightly as the O_2 mole ratio increases. The RIE rate of C has a very weak dependence on the O_2 mole ratio. Although the fluorine radicals and oxygen species vary in density

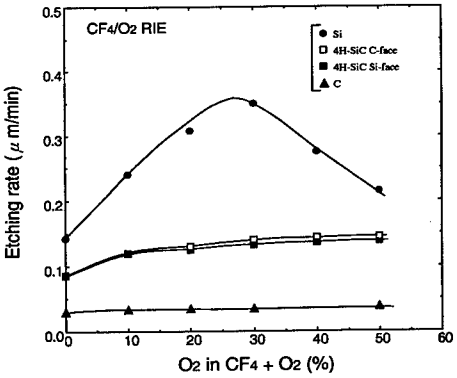

Fig. 1 RIE rates of 4H-SiC, Si and C (diamond) as a function of O_2 mole ratio. A total gas flow rate, a gas pressure and an rf-power are 50sccm, 0.1Torr and 300W. Self-bias voltage is between 580 and 720V.

widely depending on the O_2 mole ratio in the range investigated, the etching rate of diamond is not affected by the O_2 mole ratio. This indicates that the C atoms in the diamond are not removed chemically. The RIE rate of the diamond can be explained by assuming that the etching rate of C is controlled not by a chemical reaction but by a physical reaction, namely sputtering. We speculate that the C atoms in the SiC are removed predominantly by a physical reaction under the RIE conditions investigated. The Si atoms in the SiC are removed both by a chemical reaction and by a physical reaction, so the Si atoms are removed with relative ease. It is considered that the time required to remove the surface Si atoms is much shorter than that required to remove the surface C atoms in the RIE of SiC. We consider that the sputtering of the constituent C atoms in SiC controls the RIE rate of SiC.

3. Characterization of etched surface

The surface roughness of reactive-ion-etched 6H-SiC epiwafers and Si wafers was investigated by AFM. To make clear the effect of etching reactions on surface roughness we also observed the 6H-SiC epiwafer and the Si wafer etched by an Ar ion milling where only a physical reaction takes place. The etch rate by the Ar ion milling process was much smaller than that by the RIE. Figure 2 shows the height profiles of the etched surfaces. The roughness, Ra, of the SiC surface etched by the RIE is 0.25nm. The Ra of the Si surface etched under the identical RIE condition is 0.26nm. No significant difference in surface roughness is observed between reactive-ion-etched SiC and Si. On the other hand the Ra of SiC surface by the Ar ion milling is 0.62nm. This means that the chemical reaction in RIE contributes to flattening the etching surface. To investigate residual impurities we performed XPS analysis of the etched surfaces, the results are shown in Fig. 3. XPS analysis of the as-etched 6H-SiC epiwafer surface reveals that fluorine and

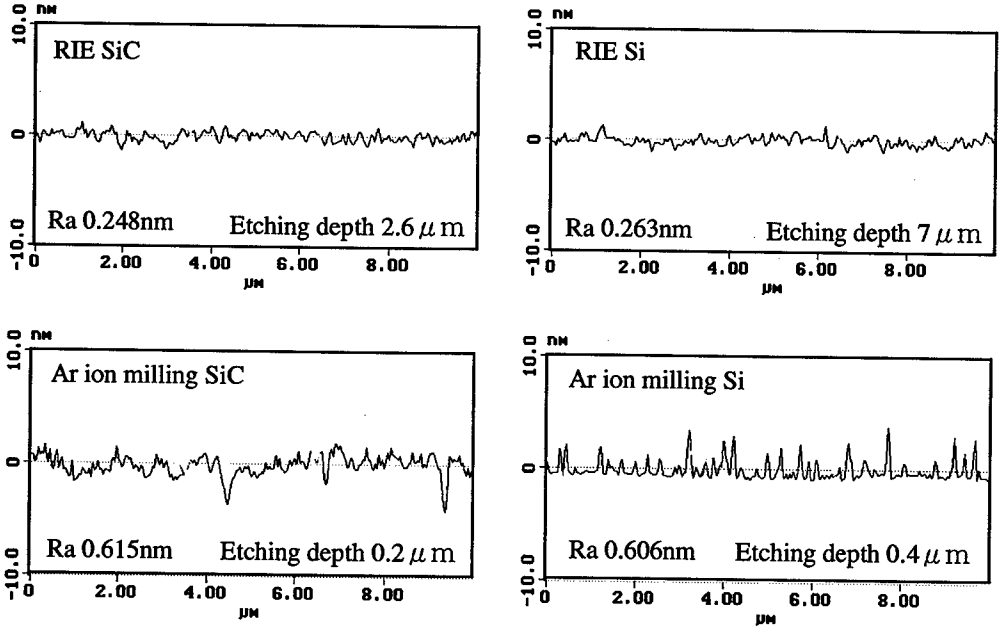

Fig. 2. Height profiles of SiC and Si surfaces etched by RIE and Ar ion milling. RIE condition is CF_4 (40sccm)/O_2 (10sccm) and an RF power of 300W. Ar ion milling condition is acceleration voltage of 600V and beam current of 100mA.

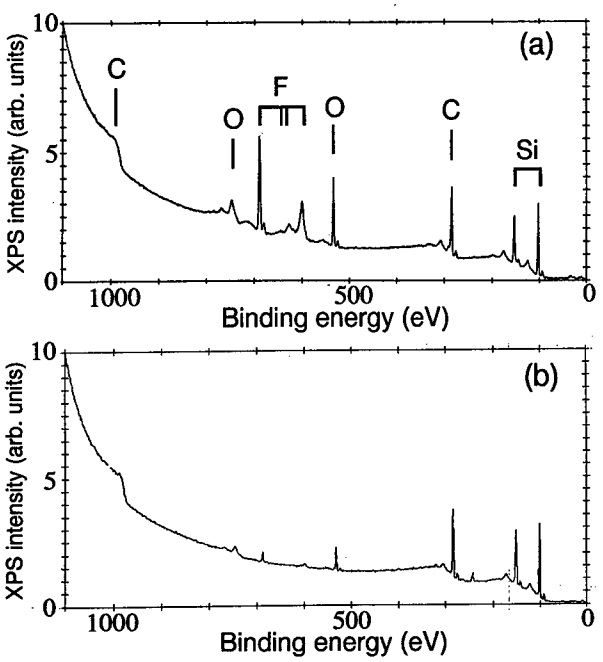

Fig. 3. XPS signals from reactive-ion-etched SiC surface. As-etched surface (a), RIE + light Ar sputtering (0.5nm) (b). By light sputtering signals from O and F species become very low level.

oxygen species remain on the surface. XPS signals from these impurities become very low level after the cleaning of the surface by Ar sputtering (about 0.5nm depth). We suppose that the residual impurities on the RIE surface can be removed easily by light sputtering or by sacrificial oxidation.

4. Accumulation-mode MOSFET

To investigate the effect of the use of the RIE on MOSFET we fabricated accumulation-mode MOSFET [2] (normally-on type) on the reactive-ion-etched surface. For the MOSFET fabrication we used a 4H-SiC epiwafer (n-type epilayer ($1.3\times10^{19}cm^{-3}$, 150nm) / n-type epilayer ($1.0\times10^{17}cm^{-3}$, 260nm) / p-type epilayer ($4.5\times10^{15}cm^{-3}$, 5μm) / n-type substrate ($7.4\times10^{19}cm^{-3}$)) purchased from Cree Research, Inc. First the surface epilayer of 240nm thickness was etched off (remaining n-type epilayer thickness 170nm) except in the source and drain regions by the RIE with an O_2 mole ratio of 0.2 and a rf-power of 300 W. The gate oxide layer was grown by thermal oxidation at 1100℃ for 2h under a wet O_2 condition. This oxidation process formed an oxide layer of 32nm. Next the oxide layer of the source and drain regions was removed by Ar ion milling, and Ni source and drain electrodes were deposited. The electrodes were annealed at about 950℃ to obtain low resistivity

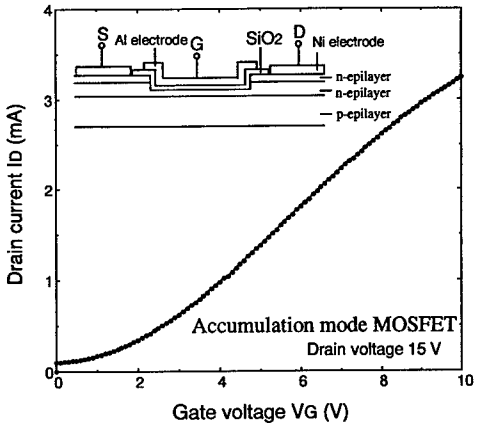

Fig. 4 I_D-V_G characteristics of accumulation-mode MOSFET fabricated using the RIE. The inset shows schematic cross-sectional view of the MOSFET. The gate length and width are 10 and 100 μm.

ohmic contacts. Finally an Al gate electrode was formed using a lift-off technique. The gate length and width were 10 μm and 100 μm, respectively. Figure 4 shows an example of drain current-gate voltage (I_D-V_G) characteristics of the MOSFET measured with the drain voltage of 15V. At this drain voltage the drain current saturates in the gate voltage range measured, thus an accumulation-mode MOSFET operation is observed. We estimated the effective mobility from the slope of $I_D^{1/2}$-V_G curves. In the estimation we subtracted the drain current at the gate voltage of 0V from I_D. High effective mobility between 86-100cm^2/Vs was obtained. The effective mobility is comparable to that of epi-channel MOSFET fabricated with regrowth [3]. It is considered that relatively high quality MOS channel is formed on the reactive-ion-etched SiC surface.

5. Summary

We have investigated RIE of SiC in CF_4/O_2 gas mixtures. RIE rate of SiC, Si and C reveals etching rate of SiC is controlled by the sputtering of constituent C atoms under the RIE conditions investigated. AFM observation of the etched surfaces shows that chemical reaction in RIE contributes to flattening the surface. Residual impurities on the RIE surface are removed by light etching (0.5nm). Effective mobility of the accumulation-mode MOS channel fabricated by the RIE surface is between 86-100cm^2/Vs. The results show that high quality MOS channel is formed on the reactive-ion-etched SiC surface.

Acknowledgement

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Electrochemical C-V Profiling of p-type 6H-SiC

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Keywords: Doping Profile, Electrolytic Etching, Etch Pit

Abstract Capacitance-voltage measurements on p-type 6H-SiC with an HF-based electrolytic solution as Schottky barrier have been performed. The etching behaviour for the two surface polarities is different concerning the etched surface morphology. The doping concentration depth profile was accurately determined for etched depths up to 10μm in the case of the Si-face. Moreover, this method is also useful for etch-pit observation following room temperature etching.

Introduction

Electrolytic dissolution of silicon carbide is the only etching process that may be carried out at room temperature. Several groups have investigated the electrochemical and photoelectrochemical properties of the SiC polytypes but there are very few studies concerning the use of electrochemical etching for determining the carrier concentration profile of SiC epitaxial films [1,2]. Thus, many photoelectrochemical studies were conducted for applications like selective etching for microstructure fabrication, water splitting, porous SiC fabrication and photocatalysis. Nevertheless, the electrochemical profiler is a valuable tool in the characterization of layered structures without depth limitation and it is widely used for the characterization of III-V compounds [3]. In this work, we show that it is possible to employ the electrochemical Capacitance-Voltage profiler for determining the epilayer doping level and thickness of p-type 6H-SiC, with a similar precision as in the case of III-V compounds.

Experimental

The investigated samples were commercially available p-type ($1.7x10^{19}cm^{-3}$ nominal doping) 6H-SiC epitaxial films grown on the Si face of p-type ($3.2x10^{18}cm^{-3}$ nominal doping) 6H-SiC wafers. The nominal thickness of the epilayers was 5μm. Experiments were performed on both the front (epilayer) and back surfaces in order to investigate the effect of the surface orientation. The back surface was polished before the etching experiments.

For our experiments we used a BIORAD PN4200 system and an HF (2% by volume in water) based electrolyte. The pH value of the used electrolytic solution was 1.43. Both e-gun evaporated Al/Ti and annealed in RTA as well as sintered In ohmic contacts were used without observing any important difference in measurements quality. Moreover, the diameter of sealing ring delimiting the area A of the contact between the electrolyte and the surface of the SiC was 1mm.

In all the measurements on the Si-face the dissipation factor had a low value varying from 0.09 to 0.12. Towards this aim, the conditions of measurements were always fixed in order to measure the same value for the serial and parallel capacitance of the electrode with the SiC sample a condition which was easily fulfilled for a measuring frequency of 1kHz. Indeed, the relatively low frequency of 1kHz is appropriate in the case of our highly doped samples for reducing any effect of series resistance. However, in this case, the measurements are more sensitive to surface induced traps.

Therefore, in all cases a preliminary electrochemical etching was performed before the standard profiling in order to remove any surface induced effects.

The doping concentration is calculated through the well-known equation:

$$N = \frac{C^3}{e\varepsilon\varepsilon_o A^2}\left(\frac{\Delta C}{\Delta V}\right)^{-1} \quad (1)$$

where ε=9.72 for SiC and C is the calculated capacitance through the admittance measurement. The flat band potential is also calculated from the equation:

$$\Phi_{FB} = 2C\left(\frac{\Delta C}{\Delta V}\right)^{-1} + V \quad (2)$$

where V is the DC applied bias.

It is well known [3] that etching uniformity is the principal instrumental limit to the depth resolution and that area definition limits the absolute accuracy. For this purpose, we have paid particular attention to the above two parameters and all the etched areas were investigated by Nomarski and Scanning Electron Microscopy (SEM) methods as well as by an alpha-step Tencor profilometer.

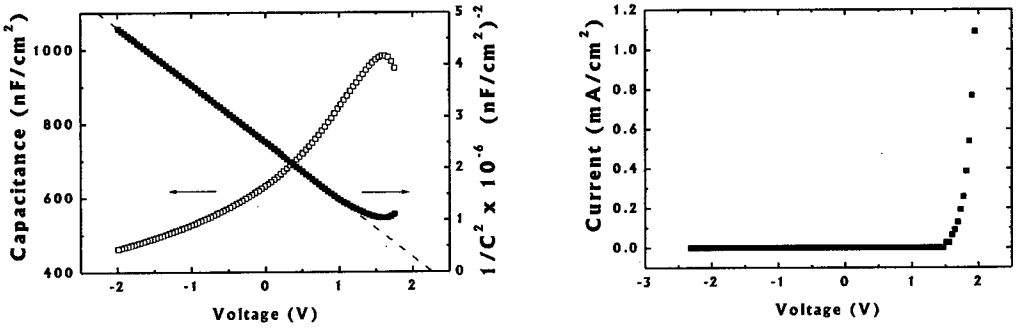
Results and discussion

There is a large difference in the obtained results on Si and C-faces of the investigated samples. In most cases (8 in total of 10 trials), it was not possible to perform a large area etch of the C-face of our samples and only a small ring was etched near to the sealing ring of the electrochemical cell. This often happens when the series resistance is quite high causing preferential etching around the perimeter of the etch hole. A possible explanation in agreement with previous results [2] is that the electrochemical etching with HF-based solutions suffer from sudden stops of the etching process due probably to the formation of a C-rich layer at the interface between the SiC and the electrolyte. However, we haven't observed any etching process stop in the case of the experiments (more than 30) performed on the Si-face even for 10μm etching depths. Experiments of electrolytic etching of the C-face using KOH-based electrolytes are underway to clarify the above issue.

The results reported in the following part are from Si-face experiments unless if it is explicitly mentioned that they relate to C-face etching experiments.

Schottky-Mott plots (e.g. the inverse of the square of electrode's capacitance versus the electrode potential) were linear in all cases for a large potential range and a typical one is shown in Figure 1a with the corresponding plot of the surface capacitance-voltage measurements. No important current (<1 nA) was observed in this range. A periodic check of the doping concentration value determined from the slope of this curve showed a perfect agreement with the results of the C-V profiling (equation 1).

Moreover, the value (2.3eV) of the flat band potential calculated from the intersection with the voltages axis agrees with the corresponding value (2.4eV) calculated through equation 2. This is a clear indication that the junction between the electrolyte and the semiconductor can be modeled as a Schottky diode and thus, used for doping concentration profiling with accuracy. Furthermore, the cathodic dark current (Fig. 1b) has a very low value indicating low leakages and the anodic current becomes important for potential higher than 1.5V.



(a) (b)

Fig. 1. (a) Capacitance versus voltage and inverse of the square of the parallel equivalent capacitance versus voltage (Schottky-Mott plot) of HF-based electrolyte in contact with 6H-SiC epitaxial film. (b) Current-potential dependence for the same as in (a) etching experiment.

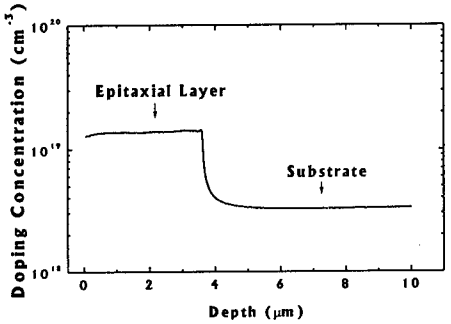
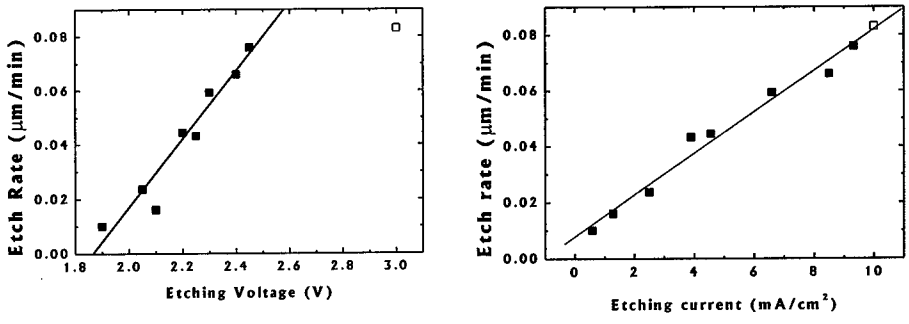


Fig. 2. Typical doping concentration profile with a total etched depth of 10μm.

Fig. 2 shows an etch profile with a total etch depth of 10μm. Note the abrupt interface with the substrate. The measured doping concentrations ($1.4x10^{19}cm^{-3}$ for the epilayer and $3.2x10^{18}cm^{-3}$ for the substrate) agree very well with nominal ones. The only discrepancy with the nominal value is in the measured value of the epilayer thickness (4μm instead of the nominal 5μm) which can be explained by the growth uniformity problems for this grade material.

The variation of the measured, through the profilometer, etch rate with the etching current and the etching voltage is reported on Fig.3.

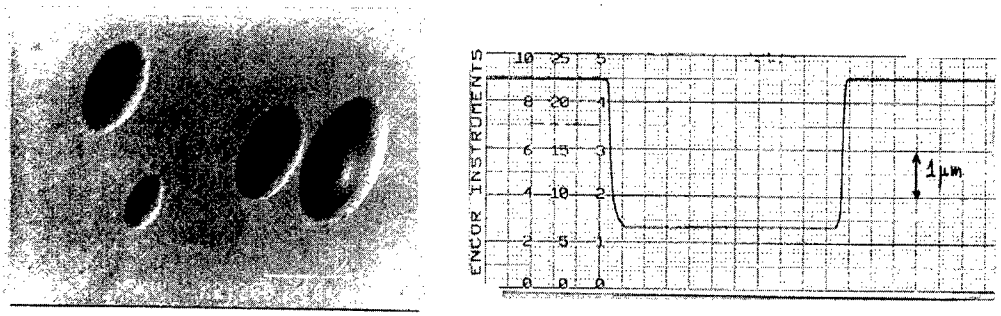


(a) (b)

Fig. 3. Dependence of the etch rate on the applied anodic potential (a) and on the etch current density (b), for both Si (■) and C-face (□) when etching was possible in the latter case.

A clear linear dependence, even for C-face, on the etching current without any saturation etching is obvious from the Fig.3b as expected for electrochemical etching of the same material. The onset of etching occurs at about 1.8V.

A smooth surface, even for etch depths of 10μm, was observed for all the values of etching current showing a large area of optimized etching conditions. To our knowledge, it is the first time that such a study of etched surface morphology in combination with doping profile determination was performed. Fig.4a and 4b show the SEM micrograph of the etched area and the etched trench from the alpha step respectively. The round pits of the Fig. 4a relate to dislocations because they maintain the shape of the pointed bottom and their distribution as etching proceeds [4]. Therefore, electrolytic etching is also useful for room temperature determination of the etch-pit density (EPD).



(a) (b)

Fig. 4. (a) SEM photo and (b) etched trench profile for a p-type 6H-SiC epitaxial film on which electrochemical capacitance-voltage measurement was performed. The dislocations are well decorated in the first case thanks to the etching process.

Conclusions

A common electrochemical set up has been used for etching p-type 6H-SiC epilayers. The doping concentration and the thickness of the epilayers were measured. Smooth etched surfaces have been obtained for etch rates in the range of some μm/hour.

The smoothness of the etched surface and abruptness of the etch walls prove the etching uniformity and the area definition accuracy. For this reason, the measured doping values agree well with the corresponding ones measured by Hg probe analysis and thus, showing, that the electrochemical depth profiling is a worthwhile technique for characterizing the SiC epilayers.

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Electrically Active Traps at the 4H-SiC/SiO_2 Interface Responsible for the Limitation of the Channel Mobility

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Keywords: 4H-SiC, 6H-SiC, Admittance Spectroscopy, MOS, Near-interface Traps

Abstract. A high density of defect states in the SiO_2 near the 4H-SiC/SiO_2 interface ($D_{NIT} > 10^{12}cm^{-2}eV^{-1}$) is observed in 4H-SiC/MOS capacitors in the energy region close to the SiC conduction band. These states are capable of trapping considerable density of electrons from the SiC. The mean activation energy of electron emission from these traps is determined to be ΔE_{NIT} = (200±40)meV. It is likely that the observed near-interface traps are responsible for the reduced electron mobility in the inversion channel of 4H-SiC MOS-FETs.

Introduction

Although the 4H-SiC polytype has superior electronic bulk properties like the high electron mobility and its small anisotropy [1], vital problems arise for this polytype with respect to MOS-based devices (fabricated on wafers with (0001)-orientation) because of the small values of the electron channel mobility (almost one order of magnitude smaller than for the 6H-SiC polytype, see [2]). We have found earlier that there are defect states at Si/SiO_2 and SiC/SiO_2 interfaces which have an energy separation from the conduction band edge of the SiO_2 of $E_C(SiO_2)$-E_{NIT}=2.77 ± 0.05 eV [3, 4]. In the 6H-/4H-SiC polytype, these states are located above/below the conduction band edge. In the case that these states are located in the band gap (4H-SiC), they can reduce the density of electrons in the inversion layer by trapping them; in addition they affect the channel mobility by Coulomb scattering.

In this paper, we present evidence based on capacitance-voltage (C-V) measurements and admittance spectroscopy (AS) for electrically active near-interface states in the band gap of 4H-SiC with an activation energy of (200 ± 40) meV; these states are proposed to be responsible for the reduction of the electron channel mobility. In 6H-SiC MOS devices, such states could not be detected by C-V or AS techniques, but are observable at higher applied electric field in the photon-stimulated electron tunneling experiments [3].

Experimental

For the MOS capacitors, n-type 4H/6H-SiC epilayers doped with nitrogen (N) (N_N-N_{comp} = $2x10^{16}cm^{-3}$) were used. The samples were subjected to a pre-oxidation RCA clean and were subsequently oxidized in dry oxygen at 1120°C for 24h (d_{oxide}(4H) = 124nm; d_{oxide}(6H) = 127nm). Oxidation was followed by a post oxidation anneal in Ar for 1h at the same temperature. MOS capacitors defined by gold electrodes (diameter 0.8mm) were thermally evaporated through a shadow mask and were characterized by C-V and AS investigations in a temperature range from 35K to 300K.

Experimental results

C-V results. In Fig. 1a), two C-V characteristics of a 6H-SiC/MOS capacitor are displayed, which are taken at room temperature (dashed curve) and at 80K (solid curve), respectively. The sweep directions are indicated by arrows. The flatband voltage of curve C(80K) is shifted by $\Delta V_{fb}(AFC) = +1.4V$ with respect to the room temperature curve. This shift is caused by an additional negative charge of $\Delta Q_{AFC} = 2x10^{11}e/cm^2$ resulting from electrons, which occupy deep interface states. At low temperatures, these electrons cannot be emitted into the conduction band during the voltage sweep and act, therefore, as an additional fixed charge (AFC). No hysteresis (<0.05V) is observed between opposite sweep directions.

C-V characteristics of a 4H-SiC/MOS capacitor taken at room temperature (dashed curve) and at 80K (dotted and solid curves), respectively, are shown in Fig. 1b). The characteristics taken at room temperature C(300K) are considered as a reference; C(300K) shows almost no hysteresis (<0.2V). The left dotted curve C(80K,i) corresponds to the initial sweep at 80K starting at deep depletion (-10V); with increasing gate voltage electrons accumulate at the interface (for gate voltages ≥ +2V) and can partially be trapped in deep states leading to a deviation from C(300K). Like in 6H-SiC MOS structures, these electrons are not re-emitted during the voltage sweep. On the way back from accumulation to depletion (sweep rate 0.1V/s) a further shift of the flatband voltage $\Delta V_{fb}(NIT)$ towards positive voltages is observed. $\Delta V_{fb}(NIT)$ is caused by an additional negative charge; this charge is trapped in energetically shallow states (termed: "near-interface traps" (NIT)), because the trapped electrons can completely be emitted during the voltage sweep. Repeated recordings at 80K result in stationary C-V characteristics (see solid curves C(80K)). From the shifts of the flatband voltage $\Delta V_{fb}(AFC) = +6.6V$ and $\Delta V_{fb}(NIT) = 2.8V$ (see Fig. 1b)), a negative charge of $\Delta Q_{AFC} = 1.1x10^{12}e/cm^2$ (trapped in energetically deep states) and $\Delta Q_{NIT} = 0.5x10^{12}e/cm^2$ (trapped in energetically shallow states), respectively, is determined.

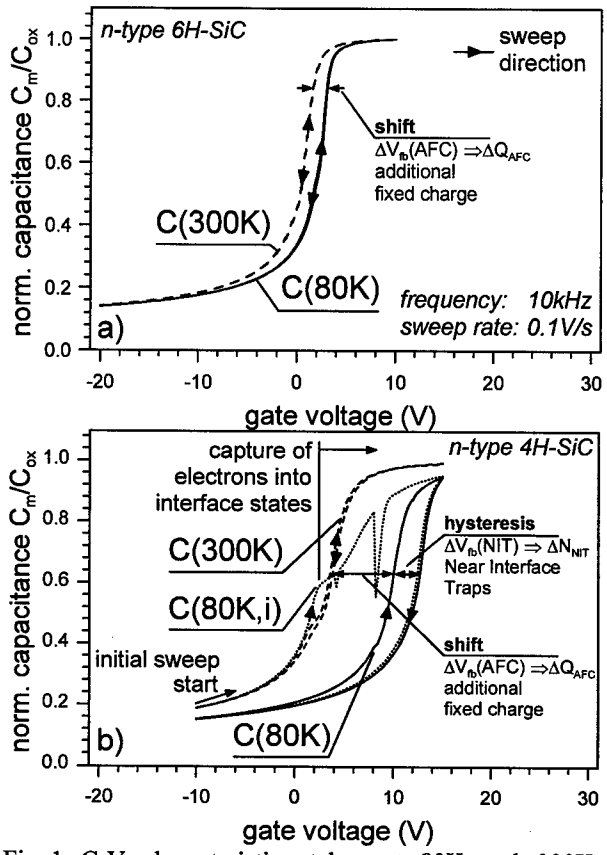

Fig. 1 C-V characteristics taken at 80K and 300K, respectively, on an a) n-type 6H-SiC/MOS capacitor and b) n-type 4H-SiC/MOS capacitor

In Fig. 2, C-V characteristics of a 4H-SiC/MOS capacitor are taken at room temperature (dashed curves), 200K (solid curves), and 80K (dotted curves), respectively. The dependence of the C-V characteristics reflects two features. With increasing temperature (a) $\Delta V_{fb}(AFC)$ decreases meaning that less energetically deep states contribute to the fixed charge (electron emission continues to deeper states) and (b) the hysteresis of C-V characteristics $\Delta V_{fb}(NIT)$ strongly decreases meaning that the density of states, which contributes to the "near-interface states" is reduced. Due to the

increasing temperature two mechanism have to be taken into account: the increase in the thermal emission rate and the band gap narrowing ($\Delta E_{gap}/\Delta$ = -0.38meV/K [5]). As a consequence, the "near-interface states" can no longer keep trapped electrons during the voltage sweep from accumulation towards depletion and a part of the "near-interface states" moves into the conduction band. This observation clearly indicates that near-interface states are located close below the conduction band edge (4H-SiC).

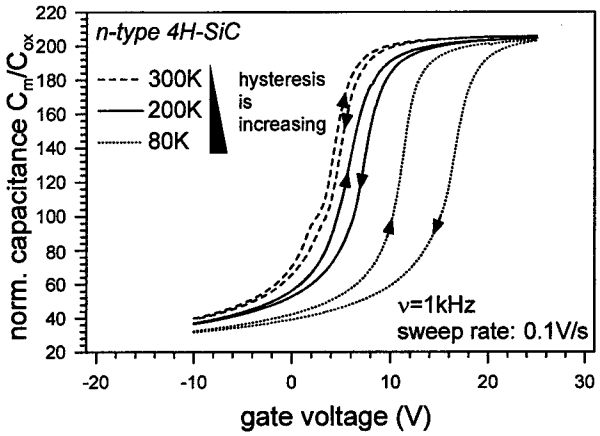

Fig. 2 C-V characteristics taken at 80K, 200K, and 300K, respectively, on an n-type 4H-SiC/MOS capacitor.

Admittance spectroscopy results. The normalized conductance of an n-type 4H-SiC/MOS capacitor under depletion and accumulation bias, respectively, (probe frequency: 100Hz, 1kHz, 10kHz, and 100kHz) is plotted as a function of the temperature in Fig. 3. Under depletion (-15V) two peaks (dashed curves) between 40K and 80K are observed. These peaks are attributed to N donors residing at hexagonal (N(h)) and cubic (N(k)) lattice sites [6]. The conductance signal arises from those N donors, which are located in the space charge region around the intersection point of the Fermi level and the N donor ground state.

Under accumulation electrons are available at the interface providing the possibility to change the charge state of traps, which are located at the interface close to the Fermi level ($E_F \pm kT$). The conductance spectra taken under accumulation (+15V) are depicted by solid curves. Besides the two N donor peaks a broad conductance peak appears in the temperature range from 115K to 185K. An Arrhenius analysis (see inset in Fig. 3) results in a mean activation energy of ΔE_{NIT} = (200±40)meV (assuming: capture cross-section $\sigma \sim T^2$). In 6H-SiC/MOS capacitors, a corresponding set of conductance peaks is not observed, only N donors are monitored (not shown here).

Fig. 4 displays normalized conductance spectra at a fixed probe frequency (ν = 1kHz), however, for different accumulation voltages (+15V up to +30V). With increasing bias, the height of the broad peak strongly decreases and the peak maximum shifts to lower temperatures (indicating that the mean activation energy or capture cross-section is lowered).

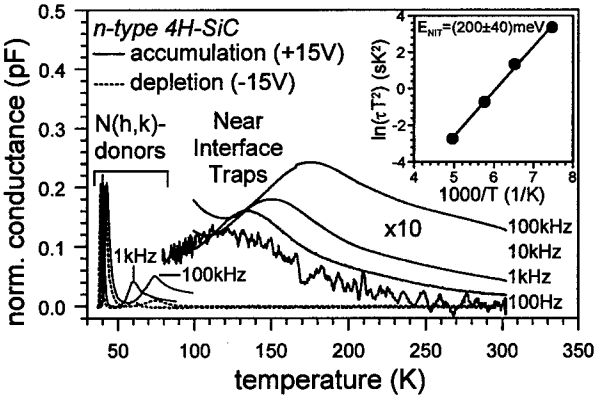

Fig. 3 Conductance spectra of an n-type 4H-SiC/MOS capacitor taken under accumulation (dashed curve) and depletion bias (solid curve). The inset shows an Arrhenius plot for the peak associated with near-interface traps.

Discussion

According to Ref. 3, the near-interface states are energetically ~ 0.1 eV below the conduction band edge of 4H-SiC (at 300K) and are assumed to be located in the oxide about 2nm apart from the interface (for detailed discussion, see [3, 4]). Our C-V results reveal besides deep

traps, which lead to a "fixed" charge, also energetically shallow traps, which are responsible for the hysteresis between voltage sweeps in opposite directions. The width of the hysteresis ΔV_{fb}(NIT) decreases strongly with increasing temperature (80K to 300K). This result is a direct consequence of increased thermal emission rate and the 4H-SiC band gap narrowing (3.3eV to 3.2eV). With decreasing width of the band gap, a considerable portion of near-interface states ($\Delta D_{NIT} = 1x10^{12}cm^{-2}eV^{-1}$) moves energetically above the conduction band edge and can no longer be occupied by electrons.

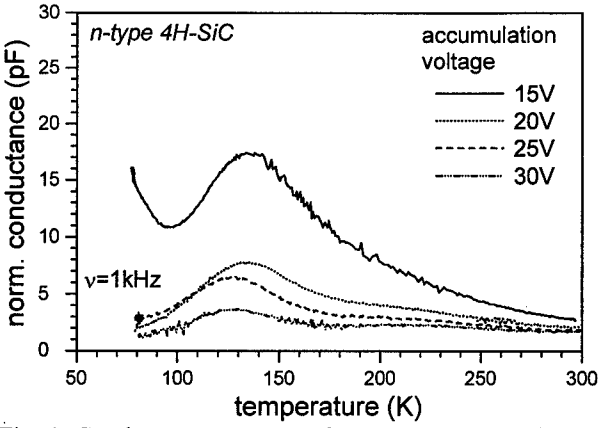

Fig. 4 Conductance spectra of an n-type 4H-SiC/MOS capacitor taken at fixed probe frequency (ν = 1kHz) and different accumulation bias.

The broad peak observed in AS spectra independently confirms the existence of electrically active traps located close below the conduction band gap. The quantitative evaluation of activation energies for near-interface states from the AS spectra seems a somewhat crucial task at the present. We suggest that electrons trapped in near-interface states have to overcome an energy barrier to be released into the conduction band. As a consequence different activation energies have to be considered for the capture and emission process; the determined activation energy of (200±40)meV is, therefore, a mean value for the prevailing process. With increasing accumulation, the conduction band edge approaches the Fermi level E_F at the interface. At this situation, the modulation of the surface potential and hence of the occupation of NITs with electrons by the probe signal is drastically reduced. This fact leads to the observed decrease of the conductance peak height in Fig. 4.

In conclusion, we point out that the observed interface states have a strong influence on the channel electron mobility in 4H-SiC/MOS FETs through additional Coulomb scattering and capture of electrons from the SiC inversion layer. The negative impact of these defects may e.g. be reduced by using SiC polytypes (6H, 15R) with a larger conduction band offset with respect to the oxide.

Acknowledgement. The support of this work by the German Science Foundation (Sonderforschungsbereich 292) is gratefully acknowledged.

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Anomalously High Density of Interface States Near the Conduction Band in SiO_2/4H-SiC MOS Devices

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Keywords: Interface State, Metal-Oxide-Semiconductor (MOS) Devices, Mobility, MOSFETs

Abstract

Process optimized MOSFETs yield mobilities of roughly 25 and 100 cm^2/Vs for 4H- and 6H-SiC respectively. In order to explain these results, we measure the interface state density near the conduction band for both polytypes using the AC conductance technique. The 4H MOS interfaces suffer from greater bandtailing, with D_{IT} exceeding $1x10^{13}$ $ev^{-1}cm^{-2}$. Integrating this D_{IT} profile, we estimate a density of $4x10^{12}$ cm^{-2} interface states lying below the Fermi level at the onset of inversion. According to the Si model, this density of charge at the interface will cause an order of magnitude reduction in mobility due to Coulombic scattering. Also, half of the induced mobile charge will be trapped by these states, thereby reducing the measured mobility by another factor of two. Applying these reductions to the bulk mobility yields expected mobilities that are consistent with measured data.

Introduction

The ability to thermally oxidize silicon carbide (SiC) has led to the development of a variety of SiC MOS devices for integrated circuits and power switching devices. Although significant progress has been made in MOS quality [1], SiC MOSFETs continue to suffer from poor electron inversion layer mobility, especially in the 4H polytype. In extreme cases, the low mobilities can be attributed to step bunching introduced by ion implantation and the high-temperature activation anneals necessary for MOSFET fabrication [2]. In these cases, the inversion channel mobility can be partially recovered by minimizing the total thermal budget (i.e., high temperature processing both before and after oxidation), and mobilities of roughly 25 and 100 cm^2/Vs have been obtained in 4H- and 6H-SiC respectively [3]. However, the question remains as to why the inversion layer mobility is lower in the 4H polytype than in 6H, especially considering that 4H bulk mobilities are quite high.

Schörner et al. [4] have suggested that the anomalously low inversion layer mobility in 4H-SiC could be due to a high density of interface states at energies greater than 2.9 eV above the valence band in all SiC polytypes. In 4H-SiC, most of these states would be located within the bandgap, and would lie below the Fermi level in n-channel MOSFETs under inversion biasing. In narrower bandgap polytypes such as 6H, the same states would lie within the conduction band, and therefore above the Fermi level. If these states are acceptor-like, they would be charged when below the Fermi level (as in 4H) and uncharged when above the Fermi level (as in 6H). When charged, the states could cause significant Coulomb scattering, reducing the inversion layer mobility. In order to investigate this hypothesis, we measured the interface state density (D_{IT}) near the conduction band in both 4H and 6H-SiC using the MOS conductance technique [5].

Experimental

Due to the wide bandgap of SiC, conventional capacitance and conductance measurements provide interface state information only on the majority carrier side of the bandgap. Since most of the MOS studies to date have been performed on p-type SiC, the interface state density in the upper half of the bandgap has been largely unexplored. In order to measure D_{IT} near the conduction band, we fabricate MOS capacitors on n-type 4H- and 6H-SiC. Samples are oxidized together at 1150 °C in wet O_2 followed by an in-situ Ar anneal and a wet reoxidation at 950 °C [1]. Polysilicon is chemical vapor deposited and degenerately doped from a phosphorus spin-on glass driven in at 900 °C. Finally, 450 μm diameter dots are patterned in the polysilicon. For p-type SiC, this process results in fixed charge density Q_F in the mid 10^{11} cm^{-2} and D_{IT} in the low 10^{10} $eV^{-1}cm^{-2}$ range near midgap [6].

Results

Figure 1 shows capacitance-voltage curves for 4H and 6H samples at room temperature. In addition to a slightly thicker oxide, the 4H sample also has a larger flatband shift. Figures 2 and 3 show G_P/ω curves obtained on the 4H and 6H samples using the MOS conductance technique. The 4H-SiC curves are broader (standard deviation ~ 4 as compared to ~ 2.5 for 6H) and much larger in magnitude. D_{IT} opposite the Fermi level at each bias is obtained from the magnitude of G_p/ω at the peak of each curve, and is plotted as a function of energy in Fig. 4. As seen, the 4H sample exhibits an order-of-magnitude higher D_{IT} than the 6H sample near the conduction band. Such a large density of states could conceivably be very effective in scattering inversion electrons, assuming the states are acceptor-like (charged when filled). This anomalously high density of interface states in 4H-SiC is certainly consistent with the hypothesis of Schörner, et al. [4], and may hold the key to the low inversion layer mobility in the 4H polytype of SiC.

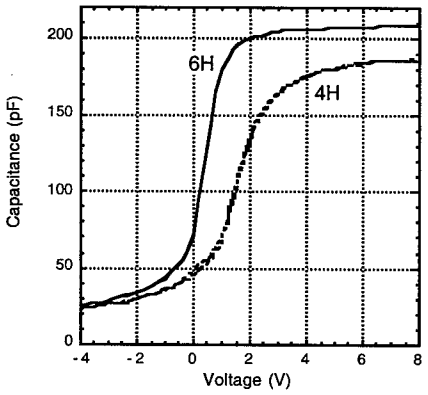

Figure 1. Room temperature capacitance-voltage curves for 4H- and 6H-SiC. Oxide thicknesses are 30.5 (26.4) nm for 4H (6H) samples.

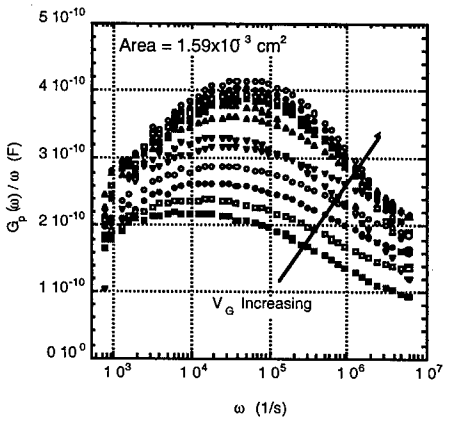

Figure 2. Room temperature G_P/ω curves for 4H-SiC at biases that place the Fermi level near the conduction band. Gate voltage varies from 1.9 to 2.9 V.

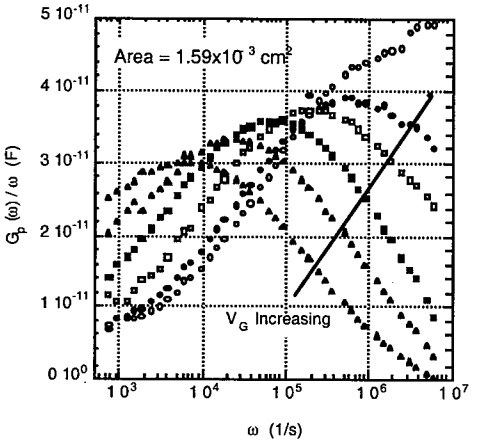

Figure 3. Room temperature G_P/ω curves for 6H-SiC. Gate voltage varies from -0.1 to +0.4 V. Note the difference in vertical scale compared to the data in Fig. 2.

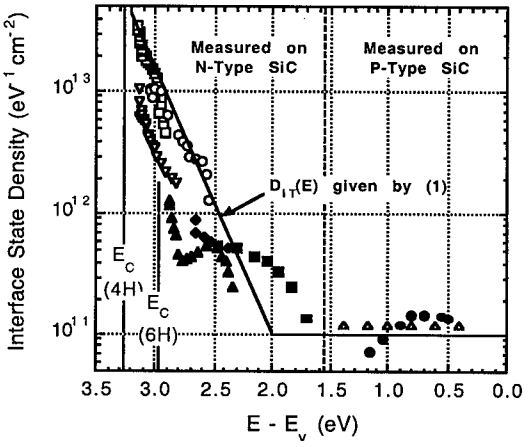

Figure 4. Interface state density on 4H-SiC (open symbols) and 6H-SiC (solid symbols) versus energy. E_C for 4H and 6H are indicated separately.

Discussion

The presence of such a large interface trap density has a two-fold effect on reducing the measured mobility. First of all, as they become charged, they serve as Coulombic scattering centers. To calculate the interface charge, we assume the fixed charge density to be $5x10^{11}$ $eV^{-1}cm^{-2}$ and positively charged. The charge from interface states (all of which are assumed to be acceptor like; i.e., negatively charged when occupied with electrons and neutral when occupied with holes) is derived as follows. A D_{IT} profile is assumed where the density in the upper third of the bandgap has an exponential dependence (shown as the diagonal line in Fig. 4), while the lower two-thirds of the bandgap is assumed to have a uniform D_{IT} of $1x10^{11}$ $eV^{-1}cm^{-2}$ (shown as the horizontal line in Fig. 4):

$$D_{IT}(E) = \begin{cases} 1x10^{11}\ [eV^{-1}cm^{-2}] & (E_V \le E \le E_V + 2eV) \\ 4.55x10^{6}\ [eV^{-1}cm^{-2}] \exp[\,5\,(E - E_V)] & (E_V + 2eV \le E \le E_C) \end{cases} \quad (1)$$

Next, (1) is integrated with respect to energy from the valence band to an energy E in the upper third of the bandgap. For energies $E \ge E_V + 2$ eV (i.e. energies in the upper third of the bandgap), we may write

$$N_{IT}(E) = 2x10^{11}\ [cm^{-2}] + 9.1x10^{5}\ [cm^{-2}] \exp[\,5\,(E - E_V)\,] \quad (2)$$

where N_{IT} is the total number of traps lying energetically between E_V and E. Using E as the Fermi energy, N_{IT} becomes a measure of the total number of charged states (assuming all states are acceptor-like) for a given Fermi level. Figure 5 illustrates how the total interface trapped charge increases as the Fermi level approaches the conduction band. At the onset of inversion ($\phi_S = 2\phi_F$ which occurs at $E-E_V = 3.05$ eV for an epilayer doping of $2x10^{16}$ cm^{-3} at room temperature), $4x10^{12}$ cm^{-2} interface states lie below the Fermi level, and are therefore charged. The mobility reduction due to Coulomb scattering in silicon MOSFETs has been studied by Sun and Plummer [7], and is shown in Fig. 6. According to the silicon model, an interface charge density of $4x10^{12}$ cm^{-2} causes the mobility to be reduced by an order-of-magnitude at the onset of inversion. As the MOSFET is biased deeper into inversion, the Fermi level moves even closer to the conduction band, and the mobility is reduced even further.

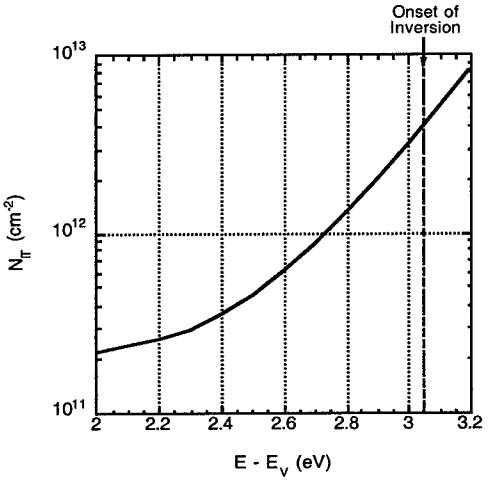

Figure 5. Total number of interface states lying below the Fermi level as a function of Fermi level positioning in 4H-SiC, based on the measured D_{IT} as represented by eqn. (2). At the onset of inversion for a p-type epilayer doped $2x10^{16}$ cm^{-3} (dotted line), $4x10^{12}$ cm^{-2} states lie below the Fermi level.

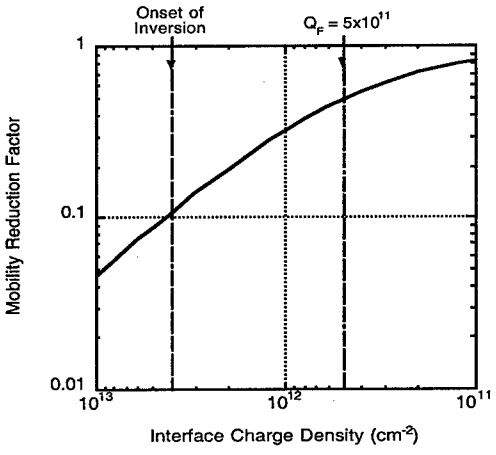

Figure 6. Reduction in inversion layer mobility as a function of interface charge using the silicon model of Sun and Plummer [7] with $N_A = 2x10^{16}$ cm^{-3}. The left-most dotted line shows the mobility reduction expected due to $4x10^{12}$ cm^{-2} charged interface states at the onset of inversion.

In addition to Coulomb scattering, the high density of interface states near the conduction band causes a significant loss of mobile carriers. To prevent overstressing the oxide, the oxide field in a MOSFET must be kept below about 4-5 MV/cm [8]. This results in a maximum induced interface charge density of roughly 10^{13} cm^{-2}. With a total interface trap density of $5x10^{12}$ cm^{-2}, half of the induced charge is trapped in the interface states and unable to conduct. With only half of the inversion charge free to move in the channel, the drain current is reduced by a factor of two. If one invokes a sheet charge model that does not account for the loss of carriers due to trapping, the low drain current is incorrectly associated with low mobility [9]. Hence, the mobility calculated with this premise underestimates the true mobility by a factor of two. The drain current may not only be low due to poor mobility; it may also be low because of a reduction in the mobile electron density.

Summary

Combining the effects described above, we can estimate the inversion layer mobility in the presence of a high density of interface states near the conduction band. Starting with the bulk 4H-SiC electron mobility of about 800 cm^2/Vs, the first calculated reduction is due to surface transport. In silicon MOSFETs, Sun and Plummer [7] show that in the presence of nearly ideal interfaces (i.e., interfaces with very low fixed charge and interface state densities), the surface mobility is roughly 75% of the bulk value [7]. Thus we should be able to obtain mobilities of:

$$\mu_{surface} = \mu_{bulk} \bullet 75\% = 600 \text{ cm}^2 / \text{Vs} \qquad (3)$$

The next mobility reduction is due to Coulomb scattering by interface charges. As shown in Fig. 6, the trapped charge due to interface states at the onset of inversion is around $4x10^{12}$ cm^{-2}. From Fig. 7, this amount of interface charge causes an order-of-magnitude reduction in mobility. Hence, due to Coulomb scattering, the mobility is further reduced to:

$$\mu_{CS} = \mu_{surface} \bullet 10\% = 60 \text{ cm}^2 / \text{Vs} \qquad (4)$$

The final reduction is due to the overestimation of mobile inversion charge. Having lost half of the induced inversion charge to traps, the drain current is reduced by factor of two, which effectively lowers the calculated mobility. Thus our overall mobility estimate is:

$$\mu_{4H-MOS} = \mu_{bulk} \bullet 75\% \bullet 10\% \bullet 50\% = 30 \text{ cm}^2 / \text{Vs} \qquad (5)$$

which is consistent with recently reported inversion layer mobilities on 4H-SiC. As a check, we apply this formulation to the 6H data. The 6H bulk mobility is taken to be 400 cm^2/Vs. Having less of a bandtail effect, the total interface charge for 6H at threshold is on the order of $1x10^{12}$ cm^{-2}. This results in a Coulomb reduction of roughly one-third. Only five percent of the mobile carriers are lost to interface trapping, so we obtain:

$$\mu_{6H-MOS} = \mu_{bulk} \bullet 75\% \bullet 33\% \bullet 95\% = 95 \text{ cm}^2 / \text{Vs} \qquad (6)$$

which is also consistent with recently reported 6H mobilities. We note that this formulation should not be interpreted literally because it is derived from silicon data. Nevertheless, it seems clear that the low inversion layer mobilities in 4H-SiC can be explained by the high density of interface states near the conduction band. These states should therefore be the focus of future MOS research.

Acknowledgements

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Effect of Post-oxidation-annealing in Hydrogen on SiO_2/4H-SiC Interface

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Keywords: Dangling Bond, Hydrogen Annealing, Interface State Density, MOS

Abstract

We have investigated post-oxidation-annealing (POA) effects on thermally grown SiO_2/*n*-type 4H-SiC interface. The flat-band voltage shift ΔV_{FB} and the interface state density D_{it} could be improved by POA both in Ar and H_2. High temperature POA in H_2 above 800°C drastically reduced the D_{it}, it is thought to be a result of the termination of the dangling bonds at the SiO_2/SiC interface by hydrogen atoms.

Introduction

A beneficial feature of SiC processing technology is that SiC can be thermally oxidized to form SiO_2 having superior dielectric properties for MOS applications. Improvement of the thermally grown SiO_2/SiC interface is a critical issue to realize MOSFETs and MOS related devices based on SiC. Wet re-oxidation anneal at low temperatures was reported to reduce the interface state density for *p*-type SiC MOS capacitors [1,2], on the other hand, this method does not improved the *n*-type SiC MOS interface [3]. SiC-ACCUFET, which has the SiO_2/*n*-type SiC interface for a channel region in its device structure, has achieved the low on-resistance [4,5]. The high quality interface is required for further improvement of the device performance. In the case of Si MOS processing, a POA in hydrogen (H_2) ambient gas for SiO_2/Si structure minimizes the D_{it}. An obvious improvement, however, has not been reported on SiO_2/SiC structure [6,7]. In this paper, we report on the effects of POA for SiO_2/*n*-type 4H-SiC interface, especially on those of POA in hydrogen.

Experimental

N-type 4H-SiC(0001) wafer with 4.9μm-thick homoepitaxial layer, purchased from CREE Research Inc., was used in this study. Effective doping density was $1x10^{16}$ cm^{-3}. To insure a clean surface, degreased samples were standard RCA cleaned followed by a sacrificial oxidation. After the sacrificial oxide was etched off in 5% HF, they were thermally oxidized in dry O_2 at 1200°C resulting in 48±3nm-thick oxide. After oxidation, samples were quenched to room temperature. POA was carried out in the flowing gas of Ar or H_2 for 30min. Some samples were dry oxidized

followed by the Ar POA at 1200°C for 30min and also cooled down in Ar at a ramp rate of -5°C /min. Aluminum gate-electrode was deposited on the oxide through a metal mask to form 500μm diameter capacitors. A high-frequency (f=100kHz) and a quasi-static (a voltage ramp rate=0.01V/s) CV measurements were carried out using HP4274 LCR meter and HP4140B pA meter at room temperature. An effective oxide charge density N_{eff} and an interface state density D_{it} was calculated from a flatband-voltage shift ΔV_{FB} of the high-frequency CV curve and high-low CV method, respectively.

Results and Discussion

Figure 1 shows the high-frequency and theoretical CV characteristics for the samples (a) without POA (as-ox.) and with POA in (b) Ar and (c) H_2 at 1000°C. As-ox. sample exhibited the large ΔV_{FB} of 11.8V, the N_{eff} was calculated to be a large value of $-5.0\times10^{12}cm^{-2}$. The ΔV_{FB} is affected by a combination of fixed oxide charge, mobile ions, charged border traps, and charged interface states. The large ΔV_{FB} of as-ox. sample is thought to be originated in the high density charged border traps and interface states occurred by the quenching after oxidation. POA treatment reduced the ΔV_{FB}, the values of N_{eff} were (b) -6.1×10^{11} and (c) $7.1\times10^{11}cm^{-2}$, respectively. The H_2 POA temperature dependence of high-frequency CV characteristics is shown in Fig. 2. The values of N_{eff} are calculated to be -2.2×10^{12} and 6.7×10^{11} cm^{-2} for the 400°C- and 800°C-annealed samples. The sample annealed in H_2 at high temperatures showed a negative ΔV_{FB}. Two possible reasons of the negative ΔV_{FB} are as follows: (i) The interface states were reduced moderately by H_2 POA as discussed later, so that the ΔV_{FB} was mainly determined by the *true* positive fixed oxide charge. (ii) Surplus hydrogen atoms may be trapped in the oxide as H^+ ion because hydrogen concentration in the oxide increased by H_2 POA as described later.

The D_{it} distribution as a function of energy from the conduction band level (Ec-E), calculated using high and low CV method, is shown in Fig. 3. As-ox. sample was higher than

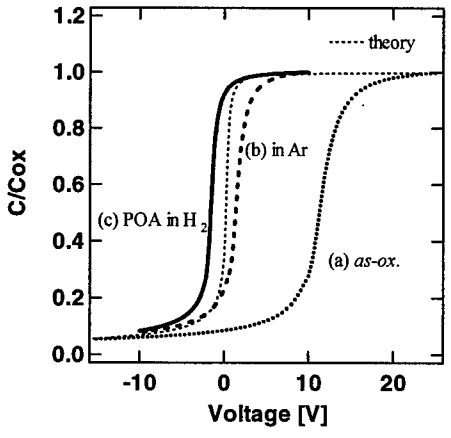

Fig. 1 The effect of POA on the high-frequency CV characteristics measured at room temperature. POA temperature was 1000°C.

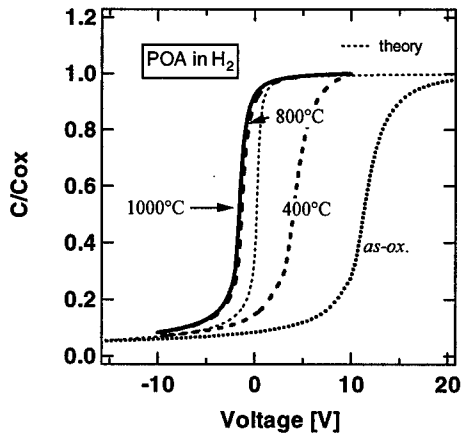

Fig. 2 H_2 POA temperature dependence on high-frequency CV characteristics measured at room temperature.

$10^{12}cm^{-2}eV^{-1}$, POA in Ar (▽) and H_2 (○) at 1000°C reduced not only N_{eff} but also D_{it}. The H_2 annealed samples exhibited smaller values of D_{it} than Ar annealed ones (about 1/3), which indicates that the H_2 POA is more effective than Ar POA for the reduction of D_{it}. The value of D_{it} decreased with increasing H_2 POA temperature, the minimum value of $1x10^{11}cm^{-2}eV^{-1}$ at Ec-E=0.6eV was achieved at the POA temperature above 800°C. The CV properties at an elevated temperature (350°C) was measured for the sample with H_2 POA at 800°C, the value of D_{it} at Ec-E=1.2eV was obtained to be $4x10^{10}cm^{-2}eV^{-1}$.

In order to investigate an influence of the initial oxide and interface quality, the samples with *in-situ* Ar POA were also post-annealed in H_2. The result is shown in Fig.4, the low-temperature annealing of 400°C did not affect the D_{it}. The reason for a little improvement by 400°C POA shown in Fig. 3, is thought to be due to the poor quality of the initial oxide and interface due to the quenching after oxidation. Similar D_{it} distributions were obtained by H_2 POA above 700°C, so we conclude that the POA temperature of 800-1000°C in H_2 is required for effective reduction of D_{it} in dry oxidized SiO_2/*n*-type 4H-SiC interface. In the case of Si MOS structure, the annealing temperature in H_2 is carried out around 400°C. The reason of the requirement of the high-temperature annealing above 800°C has not been clarified yet, it might be related to the termination of C-dangling bonds by hydrogen, because the bond energy of C-H is higher than that of Si-H [8].

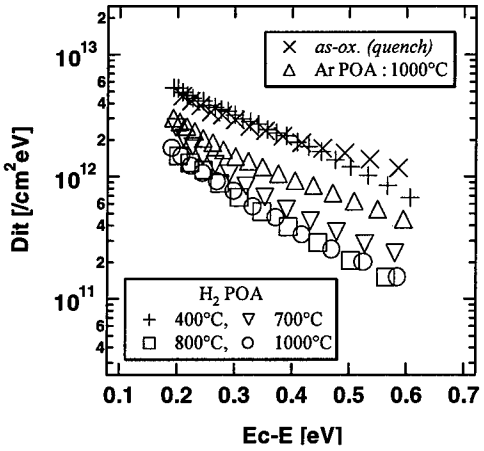

Fig. 3 The effect of POA in Ar and H_2 on the distribution of D_{it} in the energy band gap. The initial oxide (*as-ox.*) was quenched to room temperature after oxidation.

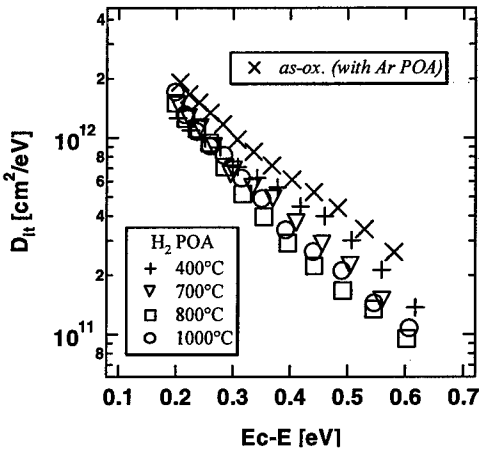

Fig. 4 The H_2 POA temperature dependence on the distribution of D_{it} in the energy band gap. The initial oxide (*as-ox.*) was *in-situ* Ar annealed and cooled down in Ar after oxidation.

Figure 5 shows the quantitative analysis of hydrogen concentration in the SiO_2/SiC structure using SIMS. The samples (a) without POA (as-ox.) and with POA in (b) Ar and (c) H_2 at 1000°C (the same samples shown in Fig. 1). The hydrogen concentration peak at the interface, observed in all samples, seems to be real since the relative sensitivity factor of hydrogen in SiO_2 and SiC are similar. The hydrogen piling up at the interface were observed in the samples without H_2 POA, the hydrogen atoms may come from SiC epitaxial layer (hydrogen concentration is in an

order of $10^{19}cm^{-3}$ as shown in Fig. 5) during oxidation, Ar POA and cooling down. Considered with the results of CV measurements, the sample with larger hydrogen concentration at the interface exhibited lower D_{it}. The Si and/or C dangling bonds at the interface are thought to be terminated by hydrogen atoms, resulting in much lower value of D_{it}.

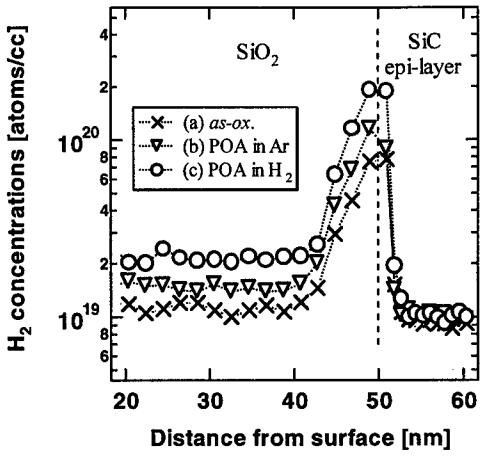

Fig.5 A SIMS analysis for SiO_2/SiC interface. These samples were prepared under the same condition of the ones shown in Fig. 1.

Summary

The effects of POA in H_2 on thermally grown SiO_2/*n*-type 4H-SiC interface have been systematically investigated. A noticeable reduction in D_{it} to a range of $10^{10}cm^{-2}eV^{-1}$ by high-temperature H_2 POA was observed, it is thought to be that the termination of Si and/or C dangling bonds and at the interface by hydrogen atoms. Evaluation of thermal stability of the H_2 POA interface must be performed in order to apply the H_2 POA technique to the device processing.

Acknowledgment

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Process Dependence of Inversion Layer Mobility in 4H-SiC Devices

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Keywords: Field-Effect Mobility, Interface State, MOSFETs, Processing

Abstract. A connection has been established between device processing and field-effect mobility in 4H-SiC MOSFETs. Processing conditions were investigated that reproducibly and predictably yielded mobilities above 40 cm^2/Vs or below 10 cm^2/Vs. A relationship between experimental field-effect mobility and average drift mobility in SiC inversion layers is presented. It is shown that high field-effect mobility is obtained when the interface state density is decreased to a value below the inversion-layer capacitance at the same Fermi energy.

Introduction. The precise nature of surface passivation is not sufficiently well understood to successfully apply the technology directly to semiconductors other than silicon. Although oxide layers can be thermally grown on the surface of silicon carbide, and inversion layers can form in this system, the field-effect mobilities reported for inversion-type SiC MOSFETs vary over as much as several orders of magnitude. Such variation is especially pronounced in 4H-SiC, where the reported mobility values range from <0.1 cm^2/Vs to >100 cm^2/Vs. Recently, Sridevan and Baliga reported an unconventional process for forming gate oxides, which resulted in high inversion layer mobility [1]. The critical process step responsible for the high mobility, however, was not identified. In this work, we have reproducibly achieved inversion layer mobilities as large as 80 cm^2/Vs in 4H-SiC MOSFETs and, furthermore, characterized the dependence of the mobility on device processing. The results are interpreted in terms of the influence of processing conditions on the magnitude and energy distribution of interface state density within the SiC bandgap. In particular, we examine the relationship between the experimentally-determined field-effect mobility and average carrier drift mobility in SiC inversion layers in the presence of charge trapping in surface states.

Device Fabrication. N-channel enhancement-type lateral MOSFETs were fabricated in 10 μm-thick Al-doped epitaxial 4H-SiC layers with $5x10^{15}$ cm^{-3} p-type doping, deposited on heavily-doped p-type 4H-SiC substrates. The wafers were cleaned using RCA clean and sacrificial oxidation. Source and drain regions were formed by double N^+ implantation at 1000 °C through a 1000 Å-thick pad oxide (LTO) and 9000 Å-thick oxide mask. The implant doses and energies were $1x10^{15}$ cm^{-2} at 40 KeV, and $2x10^{15}$ cm^{-2} at 80 KeV. C-V measurements on an MOS capacitor adjacent to a MOSFET confirmed that no implant penetration occurred into the MOSFET channel. After implantation, the oxide was stripped and wafers were divided into five different process splits as outlined in Table 1. A

polysilicon gate was deposited and doped using phosphorus implantation and annealed at 875 °C in nitrogen for 60 minutes. Al-Si contacts were sputtered and patterned using wet etch.

Table1. Post-implantation processing splits.

Steps	Wafer 1	Wafer 2	Wafer 3	Wafer 4	Wafer 5
Strip oxide	✓	✓	✓	✓	✓
Implant activation anneal at 1250 °C *		✓		✓	
Deposit 9000 Å LTO	✓	✓	✓	✓	✓
Strip oxide selectively using photomask					✓
Deposit 1000 Å LTO					✓
Implant activation anneal at 1250 °C *	✓		✓		✓
Wet oxidation at 1100 °C **	✓	✓			✓
Etch 8000 Å in selective areas	✓	✓	✓	✓	
Mobility in Thick Oxide MOSFET (cm^2/Vs)	54	44	9.5	3.2	62
Mobility in Thin Oxide MOSFET (cm^2/Vs)	56	40	3.0	-	73

* The implant activation anneal at 1250 °C was performed in argon ambient for 60 minutes.
** The wet oxidation and ramp down were similar to those described in Ref. 1.

The process splits for wafers 1-4 were chosen to allow selective exposure of the thick LTO to implant activation anneal and wet-oxidation anneal. For example LTO on wafer 1 undergoes both implant activation anneal and wet oxidation anneal, whereas LTO on wafer 4 is not subjected to any anneal. Using a photomask, the gate oxide was etched back to around 1000 Å in selective areas to allow fabrication of thin oxide MOSFETs. On wafer 5 the thinning of gate oxide was done prior to any anneal, and both thick and thin oxides were subjected to implant activation and wet oxidation anneals.

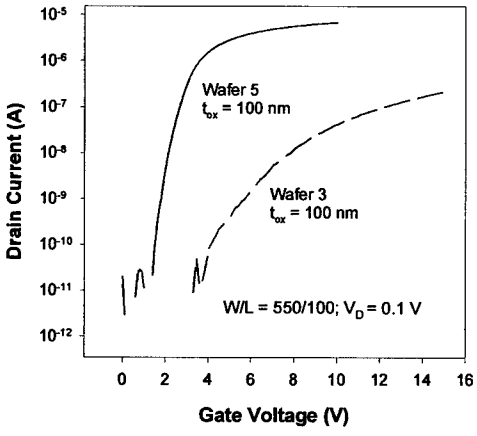

Fig. 1. Drain current – gate voltage characteristics of MOSFETs with high and low mobility.

Results: Field-effect mobility was obtained from the maximum value of transconductance in the linear region of the current-voltage characteristics. The average mobility values, measured on both thick- and thin-oxide MOSFETs, are shown in Table 1. The mobility data are seen to fall into two groups of devices with low and high mobilities. MOSFETs on wafers 3 and 4 have mobilities below 10 cm^2/Vs, whereas the average mobilities on wafers 1, 2, and 5 lie between 40 and 73 cm^2/Vs. The different behavior of the two groups of devices is illustrated in Fig. 1, which shows the transfer characteristics of low and high mobility MOSFETs. The differences in subthreshold slope and drain current are very apparent. Figures 2a and 2b compare the gate-voltage dependence of the transconductance of the two groups of devices. The transconductance of the high-mobility MOSFET

increases more rapidly with the gate voltage, reaches a peak, and decreases with further increase in gate voltage, indicating the presence of heavy inversion. The transconductance of the low-mobility MOSFET increases with the gate voltage much more slowly and does not reach a maximum, indicating that the device is probably in a state of weak inversion even when a large gate voltage is applied. The process step that differentiates the high- and low-mobility devices is the wet-oxidation anneal at 1100 °C and the subsequent ramp-down process. The mobility did not appear to correlate with the oxide thickness or with other processing variables.

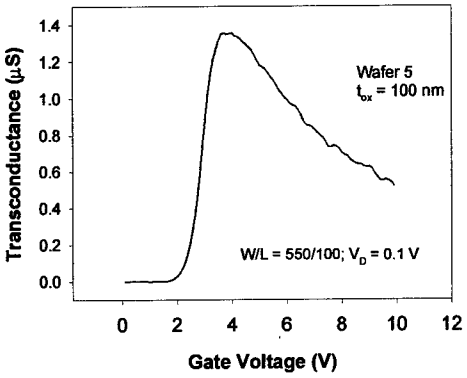

Fig. 2a. Transconductance of a MOSFET with field-effect mobility of 70 cm^2/Vs calculated at V_g = 4 V

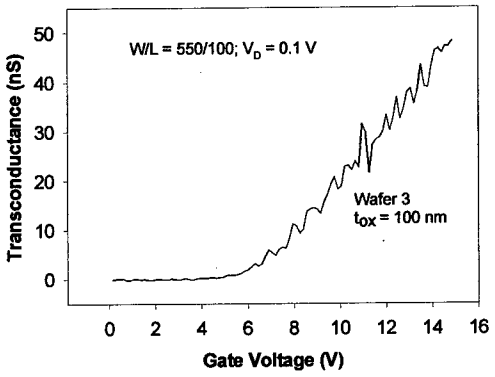

Fig. 2b. Transconductance of a MOSFET with field-effect mobility of 3.0 cm^2/Vs calculated at V_g = 15 V

Discussion. The preceding results can be understood in terms of the effect of processing conditions on the magnitude and energy distribution of interface states within the SiC bandgap. A change δV_G in gate voltage results in a change δQ_t in the charge trapped in interface states and a change δQ_{inv} in inversion charge:

$$\delta V_G = (\delta Q_t + \delta Q_{inv})/C_{ox} \tag{1}$$

while the drain current depends only on the inversion charge:

$$\delta I_D = (W/L)V_D \mu_0 \delta Q_{inv} \tag{2}$$

where μ_0 is the average drift mobility of electrons in the inversion layer, and other symbols have their usual significance. From Eqs. (1) and (2), we obtain

$$\frac{\mu_{fe}}{\mu_0} = \left[1 + \frac{dQ_t/d\Phi_s}{dQ_{inv}/d\Phi_s}\right]^{-1} \approx \left[1 + \frac{q^2 D_{it}}{C_{inv}}\right]^{-1} \tag{3}$$

where D_{it} is the interface state density at a given surface Fermi potential Φ_S, and $C_{inv} = dQ_{inv}/d\Phi_S$ is the differential capacitance of the inversion layer [2].

It can be seen from Eq. (3) that $\mu_{fe} < \mu_0$ as long as the trapped charge increases with the gate voltage, and that $\mu_{fe} \rightarrow \mu_0$ when C_{inv}/q^2 is large relative to D_{it}. One would, therefore, expect the field-

effect mobility to be very low near the threshold, and to increase in strong inversion, where the ratio q^2D_{it}/C_{inv} becomes smaller. However, if the interface state density also increases rapidly near the band edges, as is generally observed in MOS devices, very large gate voltages would be required for the field effect mobility to approach the actual inversion layer mobility. The quantity C_{inv}/q^2 is plotted in Fig. 3 as a function of the Fermi energy (E_c - E_F) at the surface for p-type SiC with doping concentration of 5×10^{15} cm^{-3}. Also plotted in Fig. 3 are interface state density distributions which, in conjunction with the charge-sheet model for SiC [2, 3], were used to fit the $I_D - V_G$ characteristics in Fig. 1. Values 7×10^{11} cm^{-2} and 250 cm^2/Vs were used for the oxide fixed charge Q_f and μ_0 in all calculations. (This last assumption may overestimate the value of D_{it} if μ_0 is lowered by Coulomb scattering by the trapped charges).

The experimental data can be fitted by a density distribution of interface states within the bandgap that increases exponentially toward the band edge [2]:

$$D_{it}(E) = 1\times10^{11} + 1\times10^{14}\exp[-(E_c - E)/\zeta] \quad (4)$$

where ζ is a parameter that characterizes the degree of interfacial disorder. For a perfect interface, $\zeta \rightarrow 0$. The interface state density thus reaches 1×10^{14} cm^{-2}eV^{-1} at the conduction band edge, but the density distribution for the high-mobility sample decays more rapidly away from the band edge. The values of ζ, the trapped charge densities, and inversion layer charge densities at the highest applied gate voltages for wafers 3 and 5 are given in Table II. The differences between the two groups of devices are very apparent. The re-oxidation process apparently lessens the interfacial disorder, thus sharpening the interface state distribution.

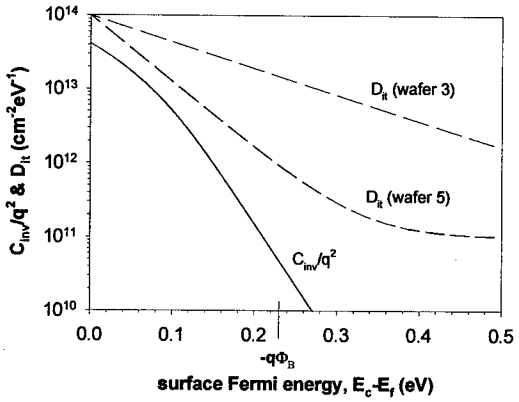

Figure 3 Inversion-layer capacitance C_{inv} and computed D_{it} versus surface Fermi energy. The threshold point ($-q\Phi_B$) is indicated in the figure.

Table II

	Wafer 3	Wafer 5
ζ (eV)	0.12	0.048
Highest μ_{fe} (cm^2/Vs)	9.9	80
Trapped charge (cm^{-2})	2.9×10^{12}	1.4×10^{12}
Inversion charge (cm^{-2})	9.9×10^{9}	4.6×10^{11}

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Controlled Thermal Oxidation of Sacrificial Silicon on 4H-SiC Epilayer

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Keywords: Interface, Oxidation, Sacrificial Silicon

Abstract

This paper reports on the fabrication of a MOS capacitor on n-type 4H-SiC utilizing 30nm of sacrificial Si evaporated onto the Si rich surface of the SiC epilayer sample under UHV conditions. The oxide was thermally grown on the sacrificial Si layer under a wet oxidising ambient with a re-oxidation anneal at 950°C. The oxide was characterised using high frequency C-V measurement with illumination technique and compared to a control sample having no Si layer. The effective net oxide charge, Q_{eff} was calculated to be 4.36×10^{-11} cm^{-2} and 7×10^{-11} cm^{-2} respectively.

Introduction

The use of Silicon Carbide for MOS application is undoubtedly attractive due to the wide band gap of SiC and the ability to grow SiO_2 as a native oxide. However, the quality of thermally grown oxide on Silicon Carbide has always been an issue, hindering the reproducibility of reliable Silicon Carbide based power devices. This is primarily due to the inert properties of SiC material that makes it difficult to yield an oxide of acceptable quality. In addition, a poor SiO_2/SiC interface has been reported possibly related to the presences of carbon [1]. However, recent reports have displayed tremendous progress in achieving thermally grown oxide with an interface state density equivalent to that observed in Silicon technology [2]. Despite this achievement, the reproducibility of the oxide quality is still a barrier due to the carbon induce interface defect. Hence, there is a need to search for alternative methods such as chemical vapor deposition (CVD) or until recently jet vapor deposition (JVD), combining the possibility of applying thermal oxidation on sacrificial Si to avoid such carbon related interface defect. Yet, much of the research work regarding oxidation on sacrificial Silicon produced a lack of promising results. In this work, we take a new look at thermal oxidation of sacrificial Silicon on SiC. This technique focused on the ability to control the oxidising temperature and preventing the diffusion of SiO_2 into the SiC substrate, hence eliminating the possibility of carbon related defects. This approach was carried out focusing on the critical aspects of surface preparation, Si/SiC interface quality and the oxidation conditions.

Experimental Procedure

The MOS capacitor was fabricated on a 10μm thick n-type 4H-SiC epitaxial layer with a doping concentration of 1.1×10^{16} cm^3 obtained from CREE Research Inc. The sample was solvent cleaned and placed in a UHV environment. The sample was heated up to approximately 1000°C to remove contamination present on the surface to yield an atomically clean surface. The sample was allowed to cool down to room temperature after which Silicon was evaporated onto the surface to form a layer approximately 30nm thick at room temperature.

Prior to thermal oxidation process, the sample was extracted from the UHV environment and dipped into BHF to remove the oxide that was formed by the atmospheric exposure. The sample was transferred directly into a 2" wide quartz tube furnace at 700°C under O_2 ambient at a rate of 1l/min. The ramp rate was set to 10°C/min to reach the oxidising temperature of 950°C. Due to the relative lower oxidising temperature of Si in contrast with SiC. By controlling the oxidising temperature at 950°C, we were able to limit the oxidation process to selectively oxidize only the Si layer. Therefore avoiding any involvement with the carbon within the SiC. Further to that we utilized the optimized wet re-oxidation anneal (ROA) condition at 950°C (same as the oxidation condition) for a duration of 3hrs to further improve the SiO_2/SiC interface. Unloading was done at 700°C under an Ar ambient immediately after the ROA. To form the back ohmic contact, Ni was e-beam evaporated and annealed for 5 mins at 975°C under high vacuum (HV) conditions. Finally, to form the gate contacts, Al was evaporated through a shadow mask under HV conditions to form a range of circular contacts of diameter 250-750μm.

A control sample was prepared without the sacrificial Si layer. Prior to oxidation, the sample was solvent and RCA cleaned. The thermal oxide was grown at 1050°C for 4hr to produce an oxide thickness of approximately 200Å. This was followed by ROA at 950°C for 3hrs. The sample was loaded into the furnace at 850°C under pure O_2 (at 1 l/min flow rate) and unloaded at 850°C under Ar ambient immediately after post oxidation anneal. Metalisation of the back ohmic and gate contacts were performed using the same procedure as above.

High frequency C-V measurement was used to extract the electrical characteristic of the sacrificial silicon thermal oxide. This was performed using the HP 4274 impedance analyzer at room temperature with the sample enclosed in a shielded probe station.

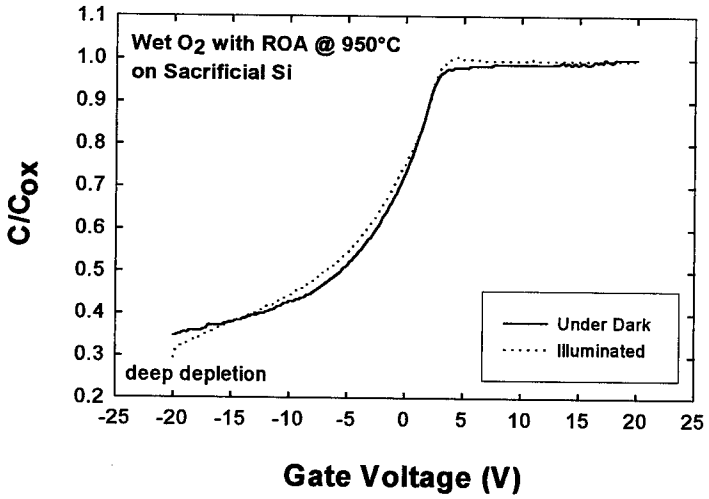

Figure 1. High frequency C-V curve of wet oxidized sacrificial Si thermal oxide on n-type 4H-SiC MOS capacitor measured under dark & illuminated conditions

Results and Discussion

Figure 1 shows the high frequency C-V curves from the wet oxidize sacrificial Si thermal oxide on n-type 4H-SiC epilayer MOS capacitor. The forward sweep from accumulation towards

deep depletion was under dark conditions. This was followed by a reverse sweep from deep depletion back to accumulation under constant illumination of the MOS capacitor with a 100W power tungsten lamp. From the high frequency C-V curve, the oxide thickness was calculated from the accumulation region of the C-V data and was approximately 676Å. This was in agreement with the theoretical thickness expected by oxidising 300Å of Si, which would produce approximately 652Å of final oxide thickness. The flat band voltage shift, ΔV_{fb} was obtained from the high frequency C-V curve corresponding to the C_{fb}, which in this case was determined to be approximately 1.4V. The effective net oxide charge, Q_{eff} was calculated to be $4.36\times 10^{11}cm^{-2}$. This was the best Q_{eff} obtained in our experimental work as compared to previously grown thermal oxide (wet and dry process) on the same 4H-SiC wafer without the use of sacrificial Si.

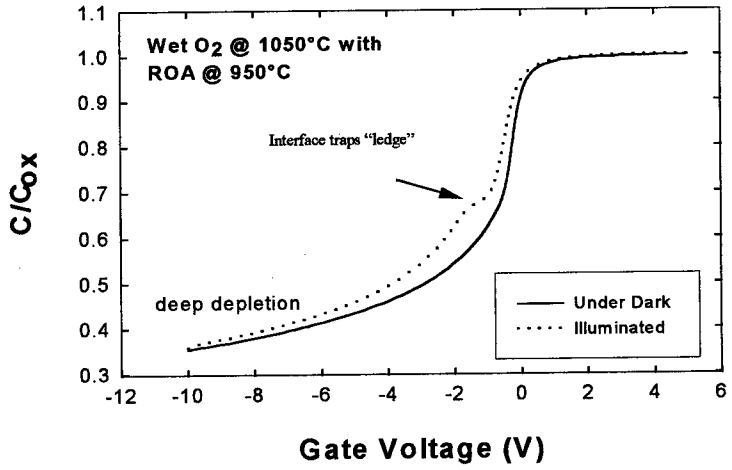

Figure 2. High frequency C-V curve of wet oxidize n-type 4H-SiC MOS capacitor measured under dark & illuminated conditions.

In Figure 1, the C-V hysteresis shows the presence of interface states. However, during the reverse sweep performed under constant illumination no interface traps induced ledge was observed. This was in contrast with the results shown in Figure 2 for the thermally oxidized SiC control sample with no sacrificial Si layer. This corresponds to fewer deep states at the SiO_2/SiC interface on the thermal oxide grown on the sacrificial Si/SiC. The positive flat band shift shows that the oxide is predominantly occupied by negative fixed charges. In contrast, the oxide grown on n-type 4H-SiC without sacrificial Si would normally yield a positive Q_{eff} as shown in Figure 2 that has a Q_{eff} of $7\times 10^{11}cm^{-2}$. These can be related to the oxidation and annealing condition on the thermal oxide [3]. However, in this case both samples shown in Figure 1 and 2 have the same post oxidation annealing condition. Therefore, the difference in the Q_{eff} polarity should be a direct effect from the different source the bulk oxide was grown on under different temperature. From these results despite the difference in the oxide thickness grown on the two samples, the technique utilizing sacrificial Si layer on a UHV environment cleaned SiC surface has displayed its potential of achieving oxide quality of acceptability for MOS technology.

Conclusion

The electrical properties of thermally oxidized SiO_2 on sacrificial Si evaporated on n-type 4H-SiC epilayer have been investigated. The results shows the oxides possessed negative fixed charges in comparison with oxide grown on SiC without the sacrificial Si layer, which possessed

positive fixed charge. Also observed was an improvement in interfacial characteristic not seen on SiO_2/SiC with the latter. Further studies are required to characterise and optimize the potential of oxides grown on sacrificial Si with atomically clean SiC surface.

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Ozone Treament of SiC for Improved Performance of Gas Sensitive Schottky Diodes

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Keywords: Gas Sensors, Ozone Cleaning, SiC Schottky Diodes, Spectroscopic Ellipsometry, Thin Oxide

Abstract

Schottky diodes with catalytic metal gates fabricated on SiC are suitable for sensing of hydrogen containing gases. The device performance, including reproducibility and long term stability, is improved by including an ozone treatment in the device processing. In this investigation, the properties of the oxide layer formed on 4H SiC by such ozone treatment are studied with spectroscopic ellipsometry. It was found that both the oxide thickness and its properties are different compared to those for a native oxide formed without ozone treatment.

Introduction

Catalytic Metal – Insulator – Silicon Carbide (MISiC) devices have potential applications as gas sensitive devices at high temperature and in rough environments, like car exhausts and flue gases [1, 2]. Capacitor devices exhibit very reproducible responses to e.g. hydrogen and hydrocarbons. The physical mechanism is that the flat band voltage of a capacitance shifts to a lower value in presence of reducing gases. The model for the gas sensitivity is based on that hydrogen atoms from molecules decompose on the metal surface and very rapidly diffuse through the metal and form a polarized layer, probably located on the oxide surface underneath the metal [3]. This means that the insulator under the catalytic metal takes active part in the gas response from the MISiC devices. For applications, in e.g. car industry, capacitor devices are not suitable due to the expensive electronic circuitry required. Schottky diodes on the other hand can be operated as gas sensors with very simple electronics. For such diodes, the forward current voltage characteristics change due to reducing gases, and the voltage change at a constant current is used as the sensor signal. Figure 1 shows a schematic view of the geometry of the Schottky diodes used here.

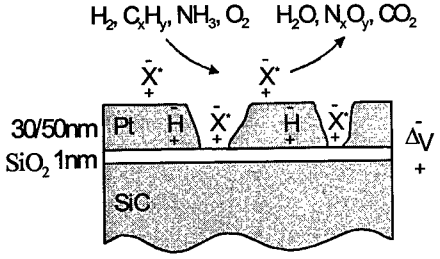

Fig. 1. Schematic picture of a MISiC device with a porous catalytic metal gate. With a porous gate the gas response may have contribution from hydrogen atoms or other polarized species both on the oxide and on the metal. Note the 1 nm oxide which is formed by 10 minutes ozone treatment.

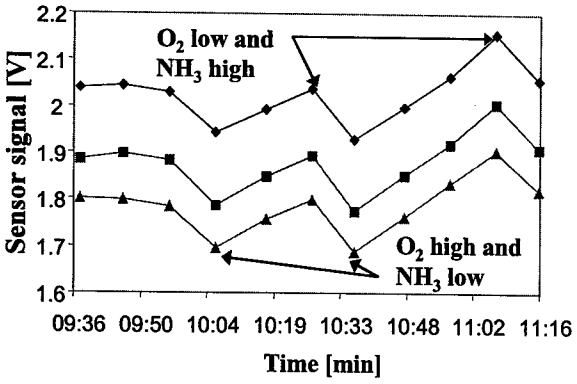

Fig. 2. Measurements in flue gases from a 1 MW boiler by three Schottky diodes with 30 nm Pt gates like in Fig. 1. The sensors are operated at 225°C. The sensor signal is the voltage over the diode at a constant current of 0.1 mA. NH_3, and O_2 are injected at two levels, high and low. At the arrows, the concentrations of injected gases are O_2 low/NH_3 high and O_2 high/NH_3 low, respectively. The experiments were performed in an industrial environment at Vattenfall [2].

The device performance depends not only on design and operating conditions but also on process parameters. A large improvement in sensor performance was obtained when ozone cleaning of the SiC surface was introduced before the catalytic metal was deposited. Ozone treated sensors from the same batch show almost identical gas responses as illustrated in Fig. 2. The properties of ozone treated SiC surfaces have been investigated by Auger spectroscopy [4] and x-ray photoelectron spectroscopy [5]. In this report, we have investigated the influence of the ozone cleaning on the SiC surface employing spectroscopic ellipsometry.

Experimental

The SiC used was of 4H n-type with substrate doping $6.5 \times 10^{18} cm^{-3}$ and with a 10 μm thick n-type epilayer with doping 3.6×10^{15} cm^{-3} on the Si-face. The wafer was oxidized twice as described elsewhere [6]. The oxide was cleaned in H_2SO_4:H_2O_2 (volume ratio 3:1) for 10 min and then removed in 50% HF for 3 min. Ozone treatment was performed in a UV cleaner [7]. In the repeated ozone exposure experiments, the oxide produced by the ozone treatment was removed by cleaning in H_2SO_4:H_2O_2 (volume ratio 3:1) for 10 min and then removed in 50% HF for 1 min. For comparison, similar studies were made on p-type silicon (100) with resistivity 4-10 Ωcm. Optical measurements were performed at four angles of incidence, 60°, 65°, 70° and 75°, in the 0.75-6.5 eV photon energy range (190-1700 nm) using a variable angle spectroscopic ellipsometer of the rotating analyzer type (J. A. Woollam Co., USA). An autoretarder was used for obtaining increased precision. The data were analyzed with the WVASE software (J. A. Woollam Co.) using procedures described by Zollner [8]. In addition to values of the best-fit parameters, the program also provides 90% confidence intervals.

Results

Optical characterization of SiC: In order to accurately determine the thickness of the oxide layers, precise optical constants of the actually used SiC substrate must be determined. These were obtained by measurements performed on a carefully cleaned, etched and finally reoxidized sample employing the methods described above. In Fig. 3, the optical constants of the material in terms of the real and imaginary parts of the dielectric function are shown. Because of the large thickness of the epilayer, the difference in the doping levels between the SiC substrate and the epilayer was not taken into consideration. The absence of interference oscillations in the obtained dielectric function shows that this approximation is valid.

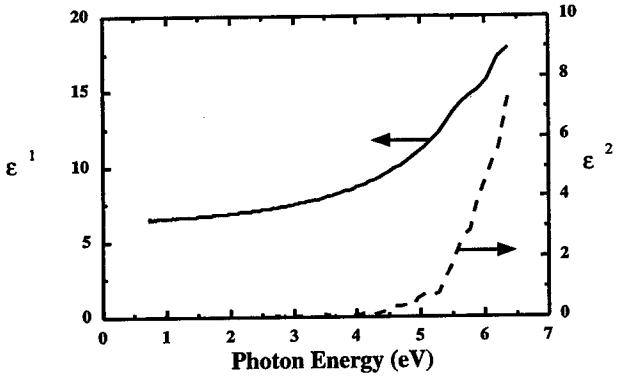

Fig. 3. Real part (solid curve) and imaginary part (dashed curve) of the complex dielectric function $\varepsilon=\varepsilon_1 + i\varepsilon_2$ of 4H SiC used here.

Ozone exposure experiments: A thermally oxidized SiC wafer with an oxide (SiO_2) layer of 127 nm was cleaned and etched in HF prior to the ellipsometric measurements as described above. The analysis showed a surface layer of 0.6 nm (an average of several experiments) that could be modeled either as SiO_2 or surface roughness. Discrimination could not be done due to optical equivalency between a very thin oxide and surface roughness. Cleaning again as above was then followed by 10 minutes of ozone exposure. The ellipsometric analysis resulted in a 1.0 nm layer of SiO_2. In this case, a surface roughness model did not give an equally good fit. The oxide was then removed by etching and the ozone treatment was repeated with very similar result as shown in Table 1. The 90% confidence values for the thicknesses given in Table 1 are ±0.1 nm or smaller. Also without cleaning in H_2O_2 and H_2SO_4, ozone exposure gave an oxide layer of similar thickness. One minute of ozone exposure (after the cleaning step) was tested once resulting in about 0.7 nm oxide.

TABLE 1. Oxide thickness on SiC after ozone treatment.

Time in ozone (min)	Oxide thickness (nm)
10	1.0
10	0.9
10 (no cleaning)	0.9
1	0.7

Silicon studies: For comparison a silicon sample was investigated in the same way. The oxide on the Si sample became thicker, about 1.7 nm, which is expected since an oxide is known to grow faster on Si than on SiC [9]. Even after HF etching, the ellipsometric analysis showed an oxide of about 1 nm. It should be noted that such a layer does not form on SiC under similar circumstances.

Discussion

An ozone treatment during device processing improves the gas sensor performance as evidenced by tests of reproducibility and stability of the sensors [2]. From the results presented here, we see that the interfacial oxide obtained using the ozone procedure is different both in terms of properties and thickness compared to a native oxide formed without ozone. One possible physical explanation for the improvement is that a somewhat thicker oxide has better electrical properties and as a

consequence the electric field distribution at the interface region will be more favorable for gas sensing. The ozone treatment will, at the same time, improve the cleaning of the SiC surface and thereby enhance the quality of the grown oxide. Another possibility is that the actual composition of the oxide is such that surface groups favorable for gas sensing are exposed. Different types of oxides may also lead to differences in electronic surface states at the oxide interfaces influencing the device characteristics. Fixed oxide charges may be of importance as studied by Zetterling et al [10]. They used capacitance-voltage measurements to show that ozone cleaning in combination with forming gas annealing reduce the fixed charge in the oxide. Schottky diode sensors manufactured without ozone cleaning often experienced high instabilities in both the sensor signal and the gas response. A typical behavior after operation for some time at an elevated temperature was a response to hydrogen of several volts in random positive or negative direction. This behavior was investigated by Schmeisser et al by photoelectron spectroscopy [11]. For sensors with a buffer layer of Ta or $TaSi_x$ between Pt and SiC, evidence of nanoparticles of Ta with a thin oxide shell were found. These nanoparticles exhibited dipole moments of up to 8 eV. A thin oxide on the SiC will make the Ta nanoparticles grow much larger and then this extreme dipole moment disappears. The instability of Schottky diodes without ozone cleaning has also been observed for sensors without the buffer layer of Ta or $TaSi_x$. It was suggested, that metal particle contamination might give other metal nanoparticles with oxide shells, that will give instability in the gas response from Schottky diodes without the thin oxide covering the SiC.

Conclusions

Earlier work has shown that the thin oxide formed by ozone treatment is very advantageous for reproducibility and long-term stability of the gas response of MISiC Schottky diode devices. Here we find that ozone cleaning of a SiC surface results in an oxide of about 1 nm thickness as determined by spectroscopic ellipsometry. The optical analysis of the oxide shows that its properties are different from those of a native oxide formed without ozone. These differences are most probably responsible for the improved device performances.

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Reliability and Degradation of Metal-Oxide-Semiconductor Capacitors on 4H- and 6H-Silicon Carbide

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Keywords: Charge Trapping, Degradation, MOS, Reliability

Abstract. Polysilicon gated MOS capacitors with oxide thicknesses between 22 nm and 57 nm were fabricated on *n*-type 4H- and 6H-SiC epitaxial layers with net doping concentrations in the lower 10^{16} cm^{-3} range. The MOS capacitors were characterized by voltage ramping and constant current stress with simultaneous monitoring of the trapped oxide charge. Breakdown field strengths up to 12 MV/cm and charge-to-breakdown values up to 30 C/cm^2 were achieved for the thinnest oxides on 6H-SiC. For the thicker oxides, the charge-to-breakdown is more than 2 orders of magnitude lower. This effect was correlated to impact ionisation in the oxide. The charge monitoring showed that positive charge trapping in oxides on SiC is more pronounced than in oxides on silicon. Furthermore, the positive charge increases significantly for increasing oxide thickness due to impact ionisation.

Introduction

Silicon carbide (SiC) offers the capability to form silicon dioxide (SiO_2) by thermal oxidation analogously to silicon. For thermal oxides on SiC, breakdown field strengths above 10 MV/cm and interface state densities around 10^{12} cm^{-2} have already been achieved [1, 2, 3, 4]. However, concerning the long term reliability of the oxide, a crucial parameter for the commercial use of MOS devices, experimental data are still scarce[5, 6, 8]. In this paper, the long term reliability of polysilicon gated MOS capacitors on 4H- and 6H-SiC is characterized by voltage ramping, constant current stress, and the corresponding values for the breakdown field strength, oxide charge trapping, and charge-to-breakdown (Q_{bd}).

Experimental

The substrates used in this work were *n*-type 8° off-axis 4H-SiC and *n*-type 3.5 ° off-axis 6H-SiC supplied by Cree Research. All 6H-SiC wafers were cut from one single crystal in order to minimize quality fluctuations from wafer to wafer. The *n*-type epitaxial layers were grown homoepitaxially by two different processes types Epi 1 and Epi 2 with significantly different process parameters on the Si face of the wafers by a low pressure chemical vapor deposition process described elsewhere [7]. The net donor concentration was in the lower 10^{16} cm^{-3} range. Poly-silicon gated MOS capacitors with gate areas from 1.7×10^{-4} cm^2 to 9.5×10^{-4} cm^2 and oxide thicknesses from 22 nm to 57 nm (see Table 1) were manufactured with a standard MOS process (for details see reference 8). The gate oxide of the capacitors was formed at 1100 °C by dry thermal oxidation of the epitaxial layers, followed by a 1 hour post oxidation anneal in nitrogen at the same temperature. For comparison, ca-

Table 1, Oxide thicknesses for SiC samples of the different polytypes and epitaxial process types

sample	4H-SiC					6H-SiC				
	Epi 1	Epi 2				Epi 1			Epi 2	without Epi
d_{ox} [nm]	24	22	28	42	57	28	39	56	27	24

pacitors on silicon (Si) with an oxide thickness of 31 nm were co-processed at an oxidation temperature of 1000 °C.

The oxide quality of the MOS capacitors was characterized by voltage ramping and constant current injection, both performed with positive gate voltage. About 40 MOS capacitors were used for each test. After the measurements, all the capacitors on the SiC wafers were etched off and new MOS capacitors were manufactured again on the same wafers with the same process parameters. Since the results of the first examination were reproduced by the second run it was concluded that all the presented results are dominated by the characteristics of the semiconductor material and not by contamination during processing.

During the constant current stress measurements the the gate voltage V_g to maintain the current was measured and recorded. The change of the gate voltage ΔV_g was converted into the change of the trapped oxide charge ΔQ_{ot} by the equation

$$\Delta Q_{ot} = -\Delta V_g \, C_{ox}, \tag{1}$$

where C_{ox} is the oxide capacitance.

Results and Discussion

Voltage Ramping. The breakdown field strength of all capacitors were in the range from 10 MV/cm to 12 MV/cm indicating the so-called intrinsic breakdown. The current densities just before breakdown were in the range from 10^{-2} A/cm^2 to 5×10^{-1} A/cm^2 for the capacitors on SiC and between 2 A/cm^2 and 5 A/cm^2 for the capacitors on Si. We think that this difference is caused by the superior quality of the oxides on Si. Consequently, the constant current injection experiments with all the capacitors had to be done at considerably lower injection current densities than it is possible with capacitors on Si, which are usually tested with current densities up to 5×10^{-1} A/cm^2.

Charge Trapping During Constant Current Stress. Fig.1 shows the trapped oxide charge for the 6H-SiC samples with epitaxial process Epi 1 and the silicon sample as a function of the injected charge with the oxide thickness as parameter. The curves show that much more positive charge is trapped in the oxides on SiC than in the reference oxide on silicon. Furthermore, the curves can be divided into 4 sections corresponding to different trapping mechanisms. In section 1 and 4, these trapping mechanisms are equivalent to those observed in oxides on silicon. In section 2 and 3, the trapping mechanisms are significantly different from those observed for oxides on silicon. An identical behavior was also found for the oxides on 4H-SiC.

In section 1 all curves are nearly identical. Thompson et al. [9] correlated the positive trapped charge in this section with the oxygen vacancy ($(\text{Si-O})_3\equiv\text{Si}\cdot\cdot\text{Si}\equiv(\text{Si-O})_3$). According to Thompson et al. the positive charge is generated by trap-to-band impact ionisation of the valence electrons with hot electrons having energies larger than 7 eV. The valence electrons are pushed into the conduction band of the oxide and a positive charge remains.

At the beginning of section 2, the oxide on silicon starts to be charged negatively. This behavior proceeds until breakdown occurs. In contrast the oxide on SiC continues to be charged positively. The positive charge trapping is independent of the oxide thickness indicating that the charge is mainly trapped near the SiC/SiO_2 interface. If the charge would be trapped equally throughout the oxide volume, a dependence of the trapped charge on the oxide thickness would be the consequence. Furthermore, band-to-band impact ionisation cannot be responsible for the charge build-up since band-to-band impact ionisation occurs about four times more often for an oxide thickness of 56 nm than for an oxide thickness of 24 nm at the used field strength of about 10 MV/cm [10]. The exact mechanism for the charge trapping in section 2 in the oxides on SiC is still an open issue.

In section 3, the positive charge trapping in the oxides on SiC is further accelerated for oxides thicker than 28 nm. A very probable mechanism for this behavior is band-to-band impact ionisation by electrons with energies of around 9 eV. According to DiMaria et al. [11] and Abadeer et al. [12] band-to-band impact ionization starts at an electric field strength of 7 MV/cm for oxides thicker than 30 nm and at an electric field strength of 14 MV/cm for oxides with a thickness of 10 nm. Consistent with this data the MOS capacitors on SiC with oxides thicker than 28 nm are far in the re-

gime of band-to-band impact ionisation since the electric field strength during the constant current stress measurement is about 10 MV/cm. In contrast the sample with the thinnest oxide is tested in a regime where impact ionisation is not dominating and thus the acceleration of the positive charge trapping is not observed. Further measurements with this sample at higher electric field strengths showed that the accelerated positive charge trapping occurs for electric fields of 10.6 MV/cm and higher. These data clearly confirm that the positive charge trapping in section 3 is correlated to impact ionisation of hot electrons with energies around 9 eV. Obviously the oxides on SiC are much more susceptible to charge trapping due to band-to-band impact ionization than oxides on silicon.

In section 4, a negative charge build up occurs for both, the oxide on Si and on SiC. This negative charge can be attributed to electron traps, which are generated by electrons with energies larger than 2 eV [13].

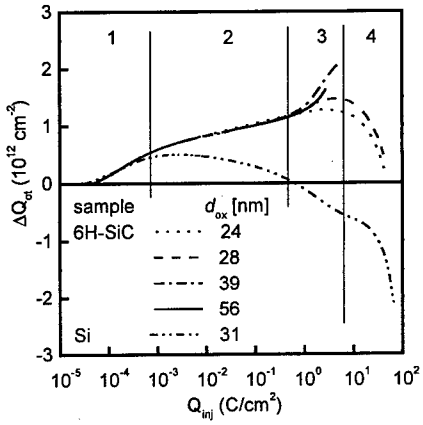

Fig. 1 Change of the trapped oxide charge ΔQ_{ot} of the capacitors on Si and on 6H-SiC with epitaxial process type 1 as a function of the injected charge Q_{inj} with the oxide thickness as a parameter. The injection current density was 1 mA/cm^2.

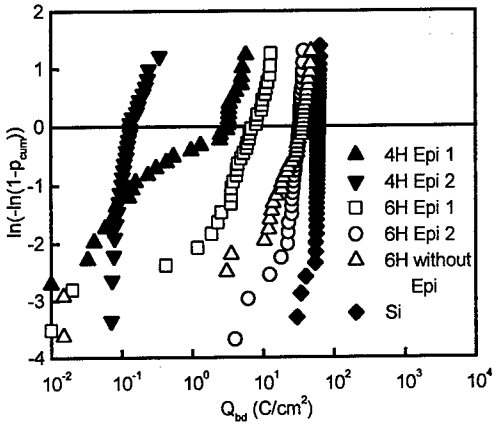

Fig. 2 Weibull-Plot of the charge-to-breakdown. The injection current density was 5 mA/cm^2 with an area of 1.7×10^{-4} cm^2 for the capacitors on SiC and 10 mA/cm^2 with an area of 3×10^{-4} cm^2 for the capacitors on Si. The oxide thickness for 4H Epi 2 and 6H Epi 1 is 28 nm respectively. p_{cum} is the cumulative failure density.

Charge-to-Breakdown. Fig. 2 shows the Weibull-plots of the charge-to-breakdown measured by constant current stress. The comparison of the data for the 6H-SiC samples with Epi 1 and without epitaxial layer reveals that the epitaxial process can create crystal defects in addition to the defects in the substrate. These crystal defects degrade the quality of the grown oxide [14]. The comparison of the data for 6H Epi 2 and the 6H-SiC without epitaxial layer proves that the epitaxial growth can be optimized to achieve results as good as without epitaxial layers. Furthermore, these results compare favorably with the data of the MOS capacitors on Si. On the contrary the MOS capacitors on the 4H-SiC polytype have lower and broader distributed Q_{bd}-values. At this point it is important to remind that the 4H-SiC wafers are cut from different crystals. Unlike the results for the 6H-SiC, the Q_{bd} values for the oxide on Epi 2 are smaller than the Q_{bd} values for the oxide on Epi 1. In general it was observed that the Q_{bd} values for oxides on 4H-SiC wafers from different crystals varied by two orders of magnitude. Two reasons may describe this behavior: first there may be higher density of defects in the 4H-SiC wafers than in the 6H-SiC wafers which varies from wafer to wafer, second the epitaxial process which leads to good results on 6H-SiC induces crystal defects for 4H-SiC. The fraction of the largest Q_{bd}-values for 4H Epi 1, however, demonstrates that the lowering of the Q_{bd} values for the oxides on the 4H-SiC polytype is not a consequence of the polytype itself but a result of a higher density of crystal defects.

Oxide Thickness Dependence of the Oxide Breakdown. Fig. 3 shows the 63% quantile of the charge-to-breakdown for the constant current stress (Q_{bd63}) as a function of the oxide thickness. The data show that the charge-to-breakdown is strongly dependent on the oxide thickness. This phenomenon is much more pronounced for the 4H-SiC samples than for the 6H-SiC samples and it was not possible to

measure the Q_{bd} value for the 57 nm thick oxide on the 4H-SiC sample since the breakdown occurred during the first second of the constant stress, corresponding to a Q_{bd} value lower than 1×10^{-3} C/cm^2. The decrease of the Q_{bd} value with increasing oxide thickness has already been reported for oxides on silicon by DiMaria et al. [8]. DiMaria pointed out that the Q_{bd} values decrease about one order of magnitude if the oxide thickness increases from 10 nm to 40 nm and stay constant up to several 100 nm. This behavior was correlated with the stabilization of the energy distribution of hot electrons with increasing oxide thickness and thus the saturation of the band-to-band impact ionization. The stronger dependence of the Q_{bd} value on the oxide thickness for oxides on SiC may be a result of the higher density of defects in the oxide. An oxide with a high density of defects is obviously more susceptible for changes in the oxide network due to band-to-band impact ionization and the involved charge trapping. This assumption is confirmed by the stronger dependence of the Q_{bd} value on the oxide thickness for the 4H-SiC sample in comparison to the 6H-SiC sample which has a lower density of defects than the 4H-SiC sample.

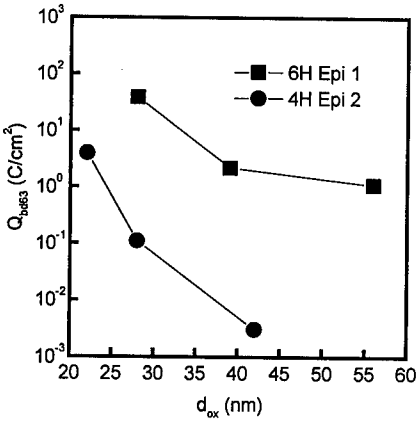

Fig. 3 63% quantile of the charge-to-breakdown for the constant current stress (Q_{bd63}) as a function of the oxide thickness. The gate area and the injection current density during constant current stress were 1.7×10^{-4} cm^2 and 1 mA/cm^2, respectively.

Conclusion

The presented data demonstrate that the long term reliability of thermal oxides on 6H-SiC and on silicon compare favorably for gate areas in the 10^{-4} cm^2 range. Indeed the reliability of the oxide is limited by a relatively high density of defects especially for the 4H-SiC polytype. For 6H-SiC the oxide defects are most probably related with crystal defects originating from the SiC substrate.

The presented data demonstrate the potential of SiC for the use as a semiconductor for commercial MOS devices. For practical MOS devices with larger gate areas, however, the crystal quality has to be improved to achieve a reliability comparable to commercial silicon devices.

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SiC Devices with ONO Stacked Dielectrics

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Keywords: Alternate Dielectric, Interface State, Mobility, MOSFETs, ONO Dielectric, Reliability

Abstract

Significantly improved SiC Metal-Insulator-Semiconductor (MIS) devices have been achieved by using a stacked dielectric consisting of silicon dioxide-silicon nitride-silicon dioxide (ONO). This stacked dielectric was used for both MIS Field Effect Transistors (MISFETs) and simple MIS capacitors, and compared to traditional SiC MOS devices with silicon dioxide: grown thermally and deposited via LPCVD. The devices with the ONO stacked dielectric had higher channel mobilities, lower interface states near the conduction band and longer lifetimes at 350°C at a 15 V gate bias. 4H-SiC buried channel devices had 10X effective channel mobilities of identical devices without the implanted channel.

Introduction

SiC MOSFET devices have been severely limited by issues relating to the insulator and/or its interface: 1) low long-term reliability of the gate insulator with applied field at high (> 300°C) temperature[1] and 2) the low effective surface channel mobility, especially for the 4H polytype. Although SiC can be thermally oxidized to produce SiO_2, improved reliability has been seen using alternative dielectrics to this thermal oxide.[2] There also seems to be a building consensus that interface states, especially near the conduction band, are responsible for low channel mobilities.[3,4]

Channel Mobility

A "fatFET" (250 μm x 250 μm) is the preferred device for extracting effective mobility, as the total resistance will be dominated by channel resistance, and was utilized for all effective surface channel mobility measurements. The first set of 6H-SiC ONO MISFETs had mobilities, determined from the linear regime, slightly higher (43 vs. 36 cm^2/V-s) than those with thermally grown oxide (wet oxidation at 1025°C for 36 hours followed by a 950°C wet re-oxidation). The ONO insulator was created with a 3-step process. First, high quality 10 nm silicon dioxide was grown thermally. Then a 60 nm silicon nitride layer was deposited via LPCVD. This layer was then oxidized in a wet ambient at 950°C for 3 hours to form the top 5-10 nm oxide. The threshold voltages of the ONO devices were approximately 4 V, while the thermal oxide devices were about 3.4 V. The ONO devices had almost 3X higher breakdown voltages and fields than those with thermal oxides.

A second set of ONO and thermally oxidized MISFET devices were measured in both the saturation and linear regimes, to determine the threshold voltage and the effective mobility. One device on each of the 56 die were probed on each wafer and averaged. In addition to the ONO vs. thermal oxide comparison, the devices received different implant activation anneals: 1) 1600°C standard Ar anneal 2) 1600°C anneal with a silicon overpressure and 3) 1700°C anneal with a silicon overpressure. This data is summarized in Table 1.

Table 1. Average mobility (μ) and average threshold voltage (Vt) are compared for both thermal oxides (Th. Ox.) and the ONO layered dielectric, annealed at 1600 or 1700°C, with a silicon over-pressure (OP) or not (Ar).

			Linear		Saturation	
Polytype	Insulator	Anneal	Vt (V)	μ (cm^2/V-s)	Vt (V)	μ (cm^2/V-s)
6H	Th. Ox.	OP 1600	7.3	28.1	6.5	13.7
6H	Th. Ox.	Ar 1600	7.4	25.3	6.5	11.8
6H	Th. Ox.	OP 1700	7.9	24.7	6.8	11.2
6H	ONO	OP 1600	3.0	39.8	2.4	23.1
6H	ONO	Ar 1600	2.9	39.5	2.3	22.7
4H	Th. Ox.	OP 1600	23.1	3.2	21.1	0.3
4H	Th. Ox.	Ar 1600	24.1	3.5	23.0	0.3
4H	Th. Ox.	OP 1700	-	-	23.7	0.2
4H	ONO	OP 1600	9.0	4.7	8.9	1.3
4H	ONO	Ar 1600	9.2	4.6	9.4	1.2

There are no relevant differences between devices with different implant activation anneals, even though these anneals produce substantially different surface roughnesses. The silicon over-pressure produces surfaces that are far less rough, having an average roughness essentially equivalent to that of an as-grown epitaxial layer (0.3 nm), as measured by atomic force microscopy. However, the channel mobilities of devices processed with this anneal were identical to those processed without the silicon over-pressure, which creates a much rougher surface (0.8 nm). This indicates that surface roughness is not the dominant factor for the surface channel mobilities being obtained.

The difference between the thermal oxides and the ONO gate insulators is startling. The difference between 6H and 4H, while pronounced, is consistent with differences typically seen between these two polytypes. Without exception, the ONO devices had dramatically higher mobilities and lower threshold voltages than the devices processed with thermal oxides. This result can be explained by the interface state densities in the upper half of the band-gap.

Interface State Densities

As shown in Fig.1, the shape of the interface state distribution is quite different between ONO and thermal oxides. The interface state densities in the lower half of the band-gap are much lower for thermal oxides, but the ONO has lower densities in the upper half of the band-gap. In addition, the interface state densities are lower at the 6H Fermi level and conduction band than they are for the 4H Fermi level and conduction band. The near-conduction band interface state densities are consistent with the large differences between the effective device mobilities observed, both between insulators and between the 6H and 4H polytypes.

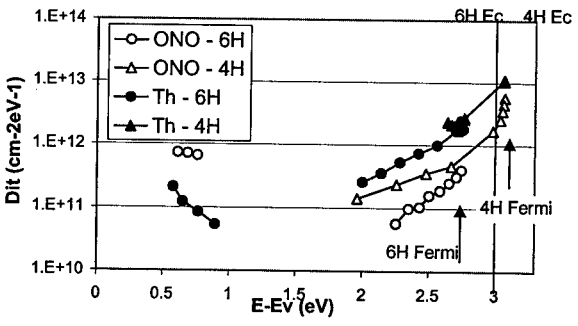

Fig. 1. Interface State Densities across the band-gap. 6H and 4H p-type in the lower half of the band are identical.

Reliability and Projected Lifetime

The ONO MISFET device reliability at high temperature was estimated by applying a gate voltage of +15 V and grounding the source, drain and substrate, and monitoring the gate current until a compliance current of 1 nA (0.25 mA/cm^2) was reached. This test was also performed on MISFETs with thermal oxides (both 1025°C wet and 1100°C dry) and deposited oxides (LPCVD), which all received a 950°C wet re-oxidation anneal. The results are denoted by the large symbols of

Figure 2. The ONO sample was wafer level tested at 350°C for 75 hours without failing. Packaged parts were then tested. However, the temperature of the packaged part was not easily set, and equilibrated closer to 335°C than 350°C. The ONO sample survived 10 days at 335°C before failing, which is a 100X improvement over the next best insulator, LPCVD oxides, and more than 1000X better than the thermal oxides. MOSFETs processed with a dry-wet thermal oxide had 4X the lifetime of those processed with the wet oxidation.

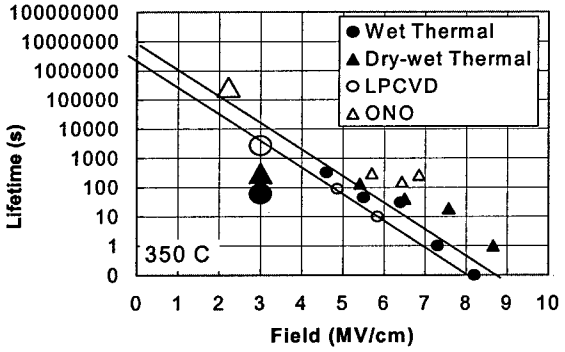

Fig. 2. Estimated lifetimes for capacitors and MISFET devices. Smaller symbols represent capacitors, while larger symbols represent MISFETs.

Time-bias measurements were also made at 350°C on 6H n-type SiC MIS capacitors. N-type SiC was used because it traditionally shows the poorest time dependent dielectric breakdown behavior. The results are also shown in Figure 2, where the measured points are shown by the small symbols, and exponential least squares fits are shown by lines. As before, thermal oxides (both 1025°C wet and 1100°C dry) and deposited oxides (LPCVD), all wet re-oxidized at 950°C were compared to the ONO insulator. Like the MISFETs, capacitors with thermal oxides grown with the "dry-wet" process (1100°C dry for 16 hours followed by a 950°C wet re-oxidation) had higher lifetimes at every field than the wet thermal oxidation. The lifetimes exhibited by the capacitors are low, but are not atypical for thermal oxides on n-type SiC at 350°C.

The MISFETs with the thermal oxides have dramatically reduced lifetimes when compared with the capacitors. This is most likely due to the physical step created at the source and drain regions by the accelerated growth of the ion-implanted regions. This step was reduced with the dry-wet oxidation, as compared with the wet, but was still a significant detractor for device reliability. Since no preferential oxidation takes place with deposited insulators, the deposited oxide and ONO MISFET failed very close to their projected times, but slightly lower. By projecting back to the likely rated operating voltage of 5 V (1 MV/cm), it can be predicted that ONO MISFETs would have a lifetime of almost 6500 hours at 335°C.

Buried Channel Devices

Some of the ONO MISFETs were processed such that the source-drain implant penetrated the implant mask. This is illustrated in Figure 3, where the nitrogen implant is somewhat blocked by the silicon dioxide blocking layer, but some of the implant penetrates through to the channel.

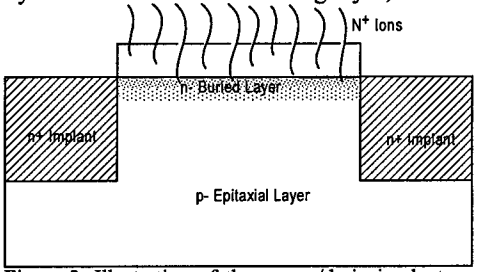

Figure 3. Illustration of the source/drain implant partially penetrating the implant mask, creating a buried channel device.

The devices where the source/drain implant penetrated the implant mask were markedly different than the devices where this did not occur. While the threshold voltage of these devices was 4 V, they had a significant amount of source-drain leakage at V_G=0, as the n- buried layer provided a current path from the source to the drain, around the channel. (The implant was not terminated at the edge of the device. This leakage could be eliminated by applying a +6 V bias to the substrate, which back-depleted the buried layer.

A buried channel ONO 4H-SiC device's IV curves are shown in Figure 4. These current levels are much higher than the current levels seen on the devices where the implant did not penetrate the implant mask. ONO devices without the buried layer, but otherwise processed identically in 4H-SiC had effective mobilities of about 4.7 cm^2/V-s. The buried layer devices had effective mobilities of 36 cm^2/V-s!

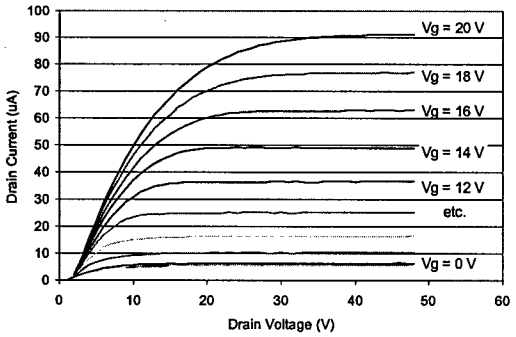

Figure 4. IV curves of a 4H-SiC buried channel MISFET. This device had an ONO insulator, a threshold voltage of 4 V and a mobility of 36 cm^2/V-s. (L_G = 250 μm, W = 250 μm)

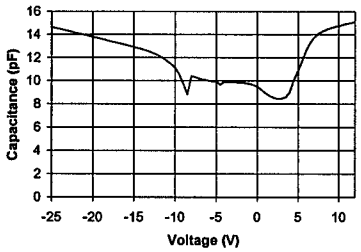

Figure 5. CV curves of a buried channel MISFET. This data indicates that the doping of the buried layer is about $1x10^{16}$ cm^{-3}, and that it extends to a depth of about 250 nm.

To verify that these devices were indeed buried channel devices, a capacitance-voltage sweep was performed. This data, shown in Figure 5, indicates that the device is a buried channel device, and that the n- buried layer is doped approximately $1x10^{16}$ cm^{-3}. The depth, as estimated from the difference in the oxide capacitance and the minimum capacitance, is about 250 nm.

In addition, the high mobility of the buried channel device seems to confirm the theory first offered by T. Ouisse,[5] that there are "pools" of electrons in the inversion layer instead of a continuous sheet. These pools could be created by one or both of the following mechanisms:

1. SiC MOS has very high (2-3 kT/q) surface potential fluctuations. These fluctuations in the local field would be substantial enough to lead to non-inverted areas.
2. Roughness, from step bunching during a high temperature implant activation anneal or from the wafer polish itself, may physically separate the inversion layer.

Unlike a conventional MISFET, the buried channel electrically connects these pools. Therefore the mobility is not limited by the electron's ability to "jump" from pool to pool to cross the channel.

Utilizing a buried channel may be a short-term solution to acceptable mobilities for power MOSFETs. However, because of the lower threshold voltages and the potential for the devices to be normally on, converting to a buried channel MOS structure is not viewed as a long-term solution to the problem of low mobilities in 4H power MOSFETs. The long-term solution is to address the mobility limiting interface states: both decrease interface states near the conduction band, and understand and eliminate the high surface potential fluctuations.

Conclusions

MISFET devices with a stacked Oxide-Nitride-Oxide (ONO) dielectric are substantially improved over devices with either thermally grown or deposited silicon dioxide. Not only do these devices show markedly higher effective surface channel mobilities, but they also exhibit a 100X improvement in device lifetime. The projected lifetime of the ONO MISFETs at 5 V is about 6500 hours at 335°C. ONO MISFETs processed with an implanted buried channel demonstrated a 8X improvement in the effective surface channel mobility, at 36 cm^2/V-s.

Acknowledgements

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The Effect of Si:C Source Ratio on SiO_2/SiC Interface State Density for Nitrogen Doped 4H and 6H-SiC

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Keywords: Interface Trap Density, Polytype, Re-Oxidation Anneal, Si/C Ratio, SiO_2/SiC Interface

Abstract: We report the effect on SiO_2/SiC interface state density near the conduction band of different Si:C ratios (0.12 to 0.55) used during the growth of n-4H and n-6H-SiC epitaxial layers. We also report the effect of a post-growth re-oxidation anneal on the interface state density for both n- and p-4H-SiC. The interface trap density near the conduction band and the effective oxide charge increase with increasing Si:C ratio for both polytypes; however, the n-4H polytype is found to have an order of magnitude higher interface trap density near the conduction band compared to n-6H-SiC. The effective oxide charge is also higher for n-4H polytype. The distribution of interface states for 4H-SiC (measured using n- and p-type material) is asymmetric, with a higher trap density near the conduction band. Post-growth annealing in wet O_2 at 950°C increases the interface trap density near the conduction for n-4H-SiC.

Introduction: Interface traps near the conduction band edge (E_c) affect carrier mobility for n-channel inversion mode SiC MOSFETs. Afanasev, et al. [1] have attributed interface states in SiO_2/SiC structures to the presence of carbon clusters and defects in a near-interfacial sub-oxide layer. Carbon cluster defects should be present following the oxidation of both p- and n-epitaxial layers. Less obvious is whether the near interfacial defects in the oxide layer depend on the dopant type. However, assuming that there is no dopant type dependence, the interface state densities that affect channel mobility for n-channel inversion mode MOSFETs can be studied using C-V techniques applied to oxidized n-epilayers. Schorner, et al. [2] have suggested that the lower channel mobility observed for 4H-SiC (compared to 6H) is the result of a large interface trap density positioned at approximately 2.9 eV above the valence band in both polytypes. The Si:C ratio is often varied to control doping concentration during epitaxial growth [3]. A result of this process is that MOS structures fabricated with epilayers grown using different Si:C ratios may have different concentrations of residual chemical states at the SiO_2/SiC interface. Herein, we report the effect of different Si:C ratios on the interface trap density near the conduction band for n-4H and n-6H-SiC. We also report the effect of a post-growth re-oxidation anneal on the interface state density for n- and p-4H-SiC.

Experimental Procedure: MOS capacitors were fabricated with Mo gates on oxidized, nitrogen doped 4H and 6H epilayers grown with different Si:C ratios [4]. Prior to metal sputter deposition, samples were oxidized at 1100°C in wet O_2 followed by an in-situ Ar anneal. Samples were characterized using simultaneous Hi-Lo C-V techniques at room temperature in order to measure the interface trap density (D_{it}) near the conduction band and the effective oxide

charge (Q_{eff}). For the post-growth re-oxidation anneals, n- and p-4H-SiC samples were re-oxidized at 950°C for 3hr following the Ar anneal. These samples were characterized at both room temperature and at 320°C. For all temperatures, interface state densities are plotted over energy ranges determined using procedures outlined by Cooper [5] for hole emission to the majority carrier band from interface traps in p-SiC. We are currently considering modifications to these procedures that may be necessary for electron emission in n-SiC.

Results: Figure 1 shows doping concentration, effective oxide charge and interface state density near the conduction band as a function of Si:C ratio for n-6H-SiC. The values of D_{it} increase with increasing Si:C ratio and decrease for increasing energy measured relative to the conduction band edge [Fig.1(a)]. The doping concentration and Q_{eff} also increase with increasing the Si:C ratio [Fig. 1(b)]. For the Si:C ratio of 0.25, two doping concentrations are shown – one the result of nitrogen incorporation from the CVD furnace ambient, and a second, higher concentration for which nitrogen was intentionally introduced during growth. Doping concentrations for all other Si:C ratios are the result of ambient background doping. For the same Si:C ratio (0.25), the intentionally doped sample has a higher nitrogen concentration and higher values for D_{it} and Q_{eff}. Wee, et al. [4] have reported that SiC epilayers grown by LPCVD with different silane to propane gas flow ratios had an unreacted C-H overlayer that increased in thickness with increasing propane flow rate. Afanasev, et al. [1] speculate that interface state density may be directly related to carbon clusters at the SiO_2/SiC interface. Our results indicate that D_{it} and Q_{eff} increase with increasing Si:C ratio and depend directly on the nitrogen doping concentration of the epilayer. The manner by which higher doping concentrations and/or residual surface chemical states affect the interface state density is not clear.

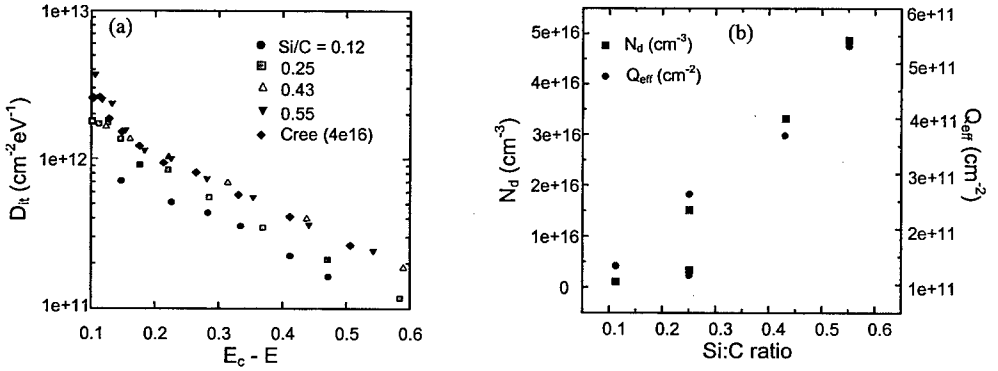

Fig. 1. (a) Interface trap density and (b) effective oxide charge and nitrogen doping concentration as a function of Si:C ratio for n-6H-SiC.

Results for 4H-SiC were similar to results for the 6H-polytype (see Fig. 2). The interface state density and Q_{eff} increase with increasing Si:C ratio. Additionally, for a given Si:C ratio, the measured doping concentration for the 4H-epilayers is slightly lower compared to the 6H-epilayers. We observe that, near the conduction band for a given energy difference E_c-E, D_{it} is an order of magnitude higher and Q_{eff} is about five times higher for 4H-SiC compared to 6H

material *of the same* doping concentration. These observations are consistent with the postulation of Schorner, et al. [2] that both polytypes have a high interface state density located at around 2.8-3.0eV above the valence band edge. For 4H-SiC, these states are located largely within the band gap where they trap conduction band electrons when n-conducting channels are created by inverting lightly doped p-epilayers. However for 6H-SiC, these interface states lie mostly in the conduction band so that charge trapping is much less noticeable for 6H n-inversion layers. The defects near the conduction band are acceptor-like, as indicated by the negative effective oxide charge which is the sum of the true oxide fixed charge and the charge held in interface states and border traps under flat band conditions. As mentioned previously, the presence of interface states has been attributed to excess C and to defects in a thin sub-oxide layer at the interface. The relationship between the doping dependence, excess C and sub-oxide defects is a matter of speculation for us at this time.

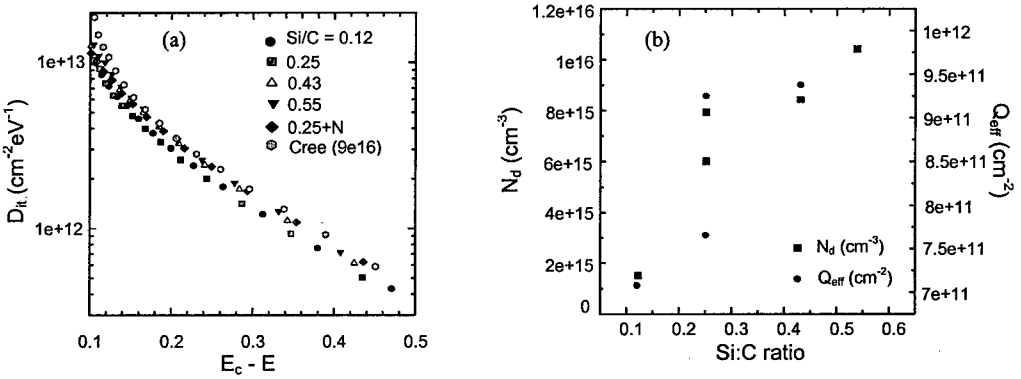

Fig. 2. (a) Interface trap density and (b) effective oxide charge and nitrogen doping concentration as a function of Si:C ratio for n-4H-SiC.

Lipkin, et al. [6] fabricated and characterized MOS capacitors with very low oxide charge and interface trap density using a post-growth, re-oxidation anneal at 950°C. Das, et al. [7] reported similar results using a similar re-oxidation anneal. The re-oxidation anneal reduces the interface state density for p-6H-SiC between mid-gap and the valence band edge. However, the interface traps that affect inversion channel mobility for n-channel MOSFETs are located near the conduction band. Figure 3 shows interface trap density as a function of energy for n- and p-4H-SiC with and without the re-oxidation anneal. The distribution of interface states is asymmetric, and Dit is higher near the conduction band than near the valence band. Following the re-oxidation anneal, the interface density changes very little near the valence band edge, but decreases for energies near mid-gap. This observation is similar to results reported by others [6, 7]. Notice however, that D_{it} near the conduction band increases sharply after the re-oxidation anneal. The interface states near the conduction band are acceptor-like, as indicated by the change in the sign of the effective oxide charge with the location of the Fermi level. Interface states near the valence band are donor-like.

Conclusion: The effects of the Si:C ratio used during epitaxial growth and post-growth re-oxidation annealing on SiO_2/SiC interface state densities have been characterized with simultaneous Hi-Lo C-V measurement techniques. Doping concentration, Q_{eff}, and D_{it} near the conduction band edge were observed to increase with increasing Si:C ratio for both n-4H and n-6H-SiC, indicating that D_{it} and Q_{eff} are directly related to the doping concentration of the epilayer. The 4H-polytype has a larger interface trap density near the conduction band and a higher effective oxide charge compared to 6H-SiC. The distribution of the interface states in the band gap for 4H-SiC is asymmetric, and the nature of states, whether acceptor-like or donor-like, depends on the location in the band gap. The acceptor-like trap density near the conduction band increases after post-growth re-oxidation of n-4H-SiC.

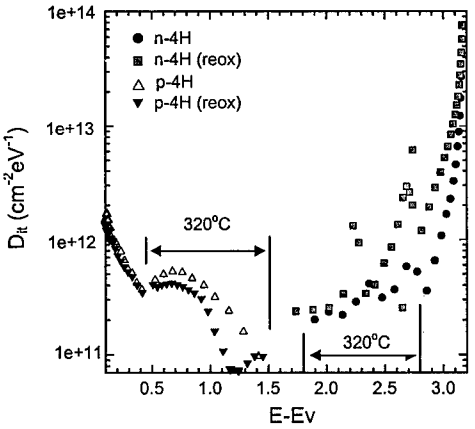

Fig. 3. Interface state density for n- and p-4H-SiC oxidized with and without the post-growth re-oxidation anneal.

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Channel Doped SiC-MOSFETs

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Keywords: Channel Mobility, Interface, Ion Implantation, MOSFETs

Abstract

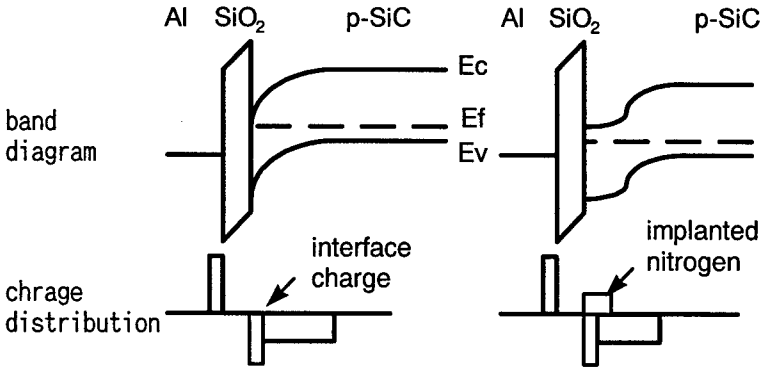
Nitrogen was implanted to compensate the negative charges at the interface of the MOS structure and to suppress the coulomb scattering of electrons and also expected to decrease the acceptor concentration at the interface and to make the electric field weak. We have found that the threshold voltage can be controlled by the nitrogen implantation, and the average channel mobility is improved drastically up to 99cm^2/Vs in 4H-SiC. This result gives a bright to the application of MOS-devices of 4H-SiC. We have found the MOS performance on the C-face can be improved in the same way, although the further optimization of the oxidation condition of the C-face is needed.

Introduction

One of the most important issues for realizing the SiC power MOSFETs is to improve the interface quality between SiC and thermal SiO_2 and to achieve a high inversion mobility. So far, there have been extensive studies to reduce Dit (interface state density) and to increase the channel mobility[1,2,3,4,5]. Still, the channel mobility of 4H-SiC MOSFET is lower than 6H-SiC even though the bulk electron mobility of 4H is higher than that of 6H. On the other hand, it is well known that the C-face (000-1) has a very large Dit and a small channel mobility although C-face has about ten times larger oxidation rate. From the previous study[4,5], we have found a very close correlation between the threshold voltage shift from the ideal value and the channel mobility. This relation predicts that the small threshold shifts will realize a high channel mobility. So, this study is devoted to improve the MOSFET characteristics for both of Si-face of 4H-SiC and C-face of 6H-SiC with the channel doping technique of nitrogen to control the threshold voltage.

Experimental

The Al concentrations of p-type epitaxial wafers of Si-faced 4H-SiC and C-Faced 6H-SiC are 0.7~1.0x10^{16}cm^{-3}. The C-face of 6H-SiC was used to compare with Si-face and not to compare with 4H. The nitrogen was implanted into the MOS-channel region with 50keV at RT. The doses were 5x10^{11}, 2x10^{12}, 8x10^{12} cm^{-2}, The nitrogen concentration of the interface with the dose of 2x10^{12} cm^{-2} is expected equal to the Al concentration of 1.0x10^{16}cm^{-3} in the epitaxial layer. This nitrogen implantation is expected to compensate the negative charges at the interface of the oxide and the semiconductor and to suppress the coulomb scattering of electrons and also expected to decrease the acceptor concentration at the interface and to make the electric field weak. This scheme is shown as the schematic diagrams of charge distributions and band diagrams in Fig. 1. Implanted nitrogen was annealed at 1300°C for 30 minutes in argon gas atmosphere after the nitrogen implantation to the source and drain regions. Gate oxidation was performed at 1100°C for 5 hours in wet oxygen gas for Si-face of 4H-SiC, and at 1100°C for 30minutes in dry oxygen gas for C-face of 6H-SiC. The oxide thicknesses of 4H and 6H-SiC were 36nm and 42nm, respectively. Aluminum was sputtered



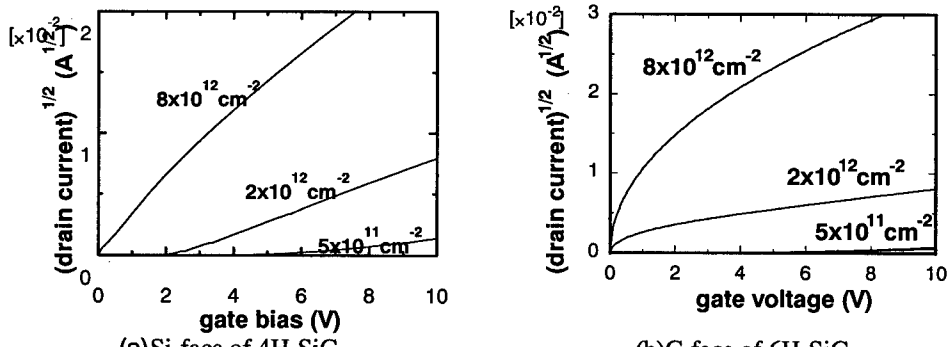
(a) conventional (b)channel doping

Figure 1 band diagrams and charge distributions of SiC-MOSFET of conventional and channel doping types

as a gate metal. The final thermal annealing was done at 450℃ in 10% hydrogen atmosphere after the metalization. The gate length and width are 100 μ m and 150 μ m, respectively.

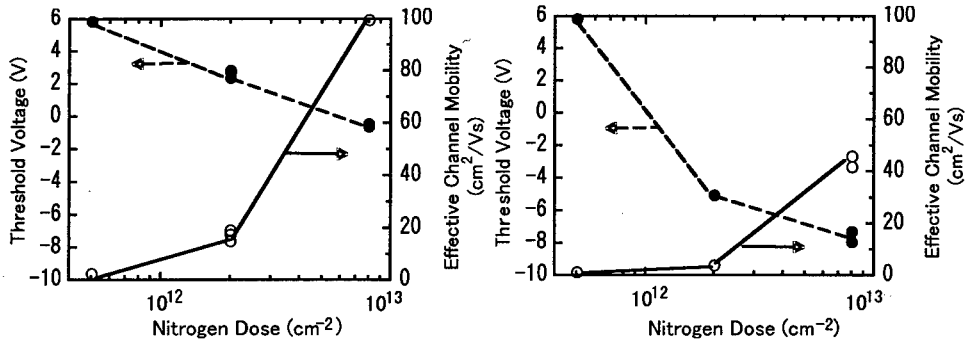
Results and discussions

Fig.2 shows the square-root plots of the drain current with the gate-drain shorted configuration for Si-face of 4H-SiC and C-face of 6H-SiC. The drain current and the gate voltage have the relationship of $\sqrt{I_D} = \sqrt{\mu W C_{ox}/2L}(V_G - V_{TH})$, because the drain current of this configuration is kept in the saturation region. The threshold voltages and the average channel mobilities are extracted from the intercept voltages and the slopes of these plots. The threshold voltages and the average channel mobilities are plotted in fig.3 The negative shift of the threshold voltage with channel dose was larger in C-face of 6H-SiC, and the MOSFET's become depletion mode with the small dose of nitrogen in C-face of 6H-SiC. On the other hand, the threshold voltage for Si-face of 4H-SiC with the dose of $8x10^{12}cm^{-2}$ was only -0.5V. It may be because after the annealing, there exist more residues of the nitrogen atoms in the vicinity of the interface on the C-face than Si-face.



(a)Si-face of 4H-SiC (b)C-face of 6H-SiC

Figure 2 square-root plots of the drain current with the gate-drain shorted configuration



(a)Si-face of 4H-SiC (b)C-face of 6H-SiC

Figure 3 threshold voltage and the average channel mobility vs the dose of the implanted nitrogen into the MOS region at 50keV at RT. The Al concentrations of p-type epitaxial wafers of Si-faced 4H-SiC and C-Faced 6H-SiC are $0.7\sim1.0\times10^{16}cm^{-3}$.

The dose is as low as to compensate the negative charges at the interface of the oxide and the Si-faced 4H-SiC. It is easily seen from fig. 3 that the channel mobility was abruptly increased according to the nitrogen dose, even though the channel mobility is not correct for the depletion mode MOSFETs with this evaluation. The obtained channel mobilities was $99cm^2/Vs$ for Si-face of 4H-SiC with the dose of $8\times10^{12}cm^{-2}$ and $40cm^2/Vs$ for C-face of 6H-SiC with the dose of $8\times10^{12}cm^{-2}$ as shown in fig. 3. It is found that the threshold voltage can be controlled by the nitrogen implantation and the average channel mobility is improved drastically.

The High frequency C-V measurement was done. The gate breakdown voltage of C-faced 6H-SiC is about 10 V. The bias voltage is less than 35 V in our C-V measurement system. These values are too small to make the accumulation condition at the MOS interface of the C-faced 6H-SiC, of which C-V characteristics could not be obtained. The High frequency C-V curves of the Si-faced 4H-SiC are shown fig. 4. The C-V curves shift to the negative bias direction with the increment of the dose content. This tendency corresponds to the compensation by the positive charge. If the n-type region is created, the capacitance will increase in the positive bias region. But this phenomenon is not observed in fig. 4. The C-V curve with the dose of $8\times10^{12}cm^{-2}$ has a large shift to the negative bias direction from the ideal C-V curve without the interface state and fixed charges. This suggests the high frequency C-V characteristics has no good correspondence with the MOSFET characteristics.

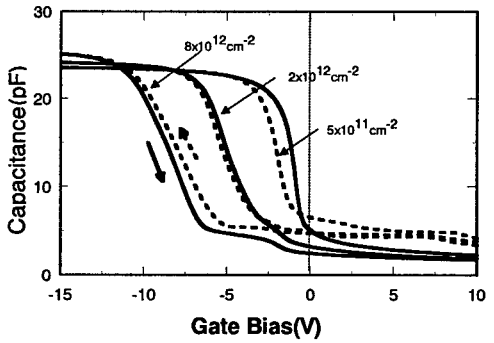


Figure 4 High frequency C-V curves of MOS on the Si-face of 4H-SiC. The doses of nitrogen implanted to the channel are 5×10^{11}, 2×10^{12}, 8×10^{12} cm^{-2} with 50keV at RT.

There has been some reasons that the C-face has not been used for the device fabrication. It is difficult to control the dopant concentration of the epitaxial layer on the C-face, which also has higher Dit than the Si-

face. But the C-face has some merits in the device fabrication. It has a smooth surface without the scratches by polishing and its oxidation rate is as high as silicon to obtain the thick oxide layer. Therefore, if the good MOS performance is realized on the C-face, we can multiply the choices of the SiC device design. We believe that optimizing the oxidation condition of the C-face, the MOS performance can be improved with the channel doping.

Conclusions

We have found that the threshold voltage can be controlled by the nitrogen implantation and the average channel mobility is improved drastically up to 99cm^2/Vs in 4H-SiC. We believe that the MOS performance on the C-face can be improved also with the channel doping if the oxidation condition of the C-face is optimized.

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Anisotropy of Inversion Channel Mobility in 4H- and 6H-SiC MOSFETs on (11$\bar{2}$0) Face

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Keywords: (11$\bar{2}$0) Face, Anisotropy, Electron Trap, Inversion Channel Mobility, MOSFETs, Scattering Mechanisms, Threshold Voltage

Abstract: An anisotropy of inversion channel mobility along ⟨0001⟩ and ⟨1$\bar{1}$00⟩ in the (11$\bar{2}$0) face for 4H- and 6H-SiC MOSFETs was reported. A dramatic improvement of inversion channel mobility was successfully achieved especially in 4H-SiC by using the (11$\bar{2}$0) face compared with the conventional (0001) Si-face. From the temperature dependence of channel mobility, phonon scattering is revealed as a dominant scattering mechanism of electrons in MOSFETs on the (11$\bar{2}$0) face.

1. Introduction

SiC MOSFETs are promising devices for high-power and high-temperature applications. The anisotropy of electron mobility is an important factor for a design of devices. Though the anisotropy of electron mobility in SiC bulk crystals is well known [1,2], the anisotropy of channel mobility in inversion layers has not been reported. In this paper, the anisotropy of channel mobility along ⟨0001⟩ and ⟨1$\bar{1}$00⟩ in MOSFETs fabricated on a (11$\bar{2}$0) face is reported for the first time. In addition, a big problem in the present MOSFETs of a low inversion channel mobility, especially in 4H-SiC, can be conquered by utilizing the (11$\bar{2}$0) face.

2. Experiments

N-channel planar 4H- and 6H-SiC MOSFETs were fabricated on p-type epilayers grown on n-type (11$\bar{2}$0) a-face and p-type (0001) Si-face substrates. The thickness and the acceptor concentration of p-type epilayers (B-doped) were 4μm and 5$\sim$10$\times10^{15}$ cm^{-3}, respectively. The source and drain regions were formed by multiple N^+ ion implantations at room temperature with a total dose of 8×10^{14} cm^{-2} and post-implantation annealing at 1550°C for 30min in Ar. Before gate oxidation, the samples were cleaned by RCA cleaning followed by additional H_2 annealing [3] at 1000°C for 30min. The gate oxidation was performed by wet oxidation at 1100°C for 1h ((11$\bar{2}$0) substrate) or 1150°C for 2h ((0001) substrate) followed by post-oxidation annealing at the oxidation temperature for 30min in Ar, resulting in a thickness of about 40nm. Note that the oxidation rate for the (11$\bar{2}$0) face is 3$\sim$5 times higher than that for the (0001) face [4]. The ohmic contacts for source and drain were Al/Ti alloyed at 600°C for 60min in Ar, and the gate electrode was Al. The channel length(L) and width(W) were 30 and 200μm, respectively.

Two types of MOSFETs, whose current directions were perpendicular each other, were fabricated on the same substrate. MOSFETs on the (11$\bar{2}$0) face have the current directions of ⟨0001⟩ (parallel to c-axis) and ⟨1$\bar{1}$00⟩ (perpendicular to c-axis), and MOSFETs on the (0001) face have the current directions of ⟨1$\bar{1}$00⟩ and ⟨11$\bar{2}$0⟩ (both perpendicular to c-axis). There was little difference in MOSFET performances between the current directions of ⟨1$\bar{1}$00⟩ and ⟨11$\bar{2}$0⟩

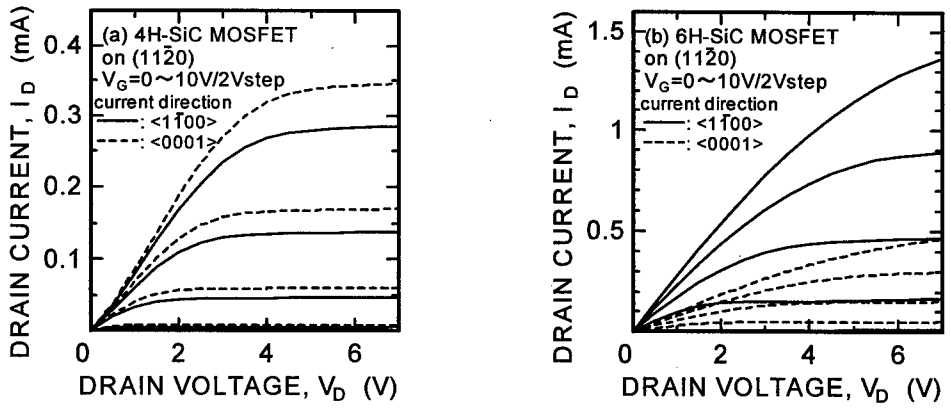

Fig.1: Output characteristics of (a)4H- and (b)6H-SiC MOSFETs fabricated on (11$\bar{2}$0) face.

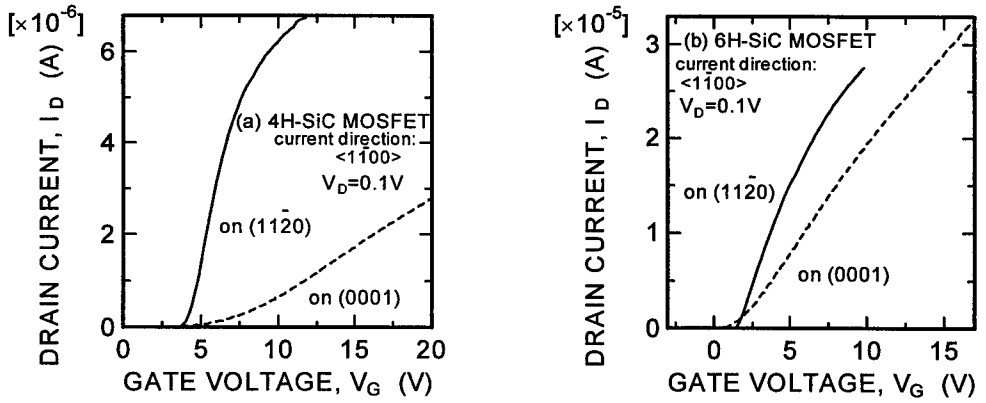

Fig.2: Linear-region transfer characteristics of (a)4H- and (b)6H-SiC MOSFETs with current direction of ⟨1$\bar{1}$00⟩ on (11$\bar{2}$0) and (0001) faces.

on the (0001) substrates.

3. Results and Discussion

Figures 1(a) and 1(b) show typical output characteristics of 4H- and 6H-SiC MOSFETs fabricated on the (11$\bar{2}$0) face. The drain current along ⟨0001⟩ is slightly larger than along ⟨1$\bar{1}$00⟩ in 4H-SiC, whereas that along ⟨1$\bar{1}$00⟩ is almost 3 times larger than along ⟨0001⟩ in 6H-SiC. The difference of drain current caused by the anisotropy of channel mobility was clearly observed.

The linear-region transfer characteristics of MOSFETs fabricated on the (11$\bar{2}$0) and the (0001) faces with the same current direction of ⟨1$\bar{1}$00⟩ are shown in Figs. 2(a) and 2(b). Even along the same current direction, the channel mobility of MOSFETs on the (11$\bar{2}$0) face was higher than that on the (0001) face. Especially in 4H-SiC MOSFETs, a dramatic improvement of channel mobility was achieved by using the (11$\bar{2}$0) face.

The values of channel mobility were determined by three methods: effective mobility ($\mu_{\rm eff}$) from the drain conductance at $V_{\rm D}$=0.1V, low-field mobility (μ_0) from the slope of $I_{\rm D}/g_{\rm m}^{1/2}$-$V_{\rm G}$ plot [5] at $V_{\rm D}$=0.1V ($g_{\rm m}$: transconductance), and saturation mobility ($\mu_{\rm sat}$) from the slope of $I_{\rm D}^{1/2}$-$V_{\rm G}$ plot in the saturation region. The method to obtain μ_0 can eliminate the mobility

Table 1: Average values of channel mobility and threshold voltage.

	4H-SiC			6H-SiC		
substrate	$(11\bar{2}0)$		(0001)	$(11\bar{2}0)$		(0001)
current direction	$\langle 0001 \rangle$	$\langle 1\bar{1}00 \rangle$	$\langle 1\bar{1}00 \rangle$	$\langle 0001 \rangle$	$\langle 1\bar{1}00 \rangle$	$\langle 1\bar{1}00 \rangle$
$\mu_{\rm eff}$ ($\rm cm^2/Vs$)	27.6	28.4	4.93	25.2	72.9	36.3
μ_0 ($\rm cm^2/Vs$)	95.9	81.7	5.59	36.5	115.7	44.8
$\mu_{\rm sat}$ ($\rm cm^2/Vs$)	41.6	36.0	2.03	21.5	62.1	26.3
$V_{\rm T}$ (V)	3.92	4.04	7.78	1.45	1.47	1.48

reduction caused by high gate voltages and source/drain series resistances. The threshold voltage ($V_{\rm T}$) was extracted from the transfer characteristics shown in Fig. 2.

The anisotropy in μ_0 and $\mu_{\rm sat}$ on the $(11\bar{2}0)$ face was clearly observed as shown in Table 1 (linear region: $\mu_{0\langle 1\bar{1}00\rangle}/\mu_{0\langle 0001\rangle}$ was 0.85 for 4H-SiC, 3.17 for 6H-SiC, saturation region: $\mu_{{\rm sat}\langle 1\bar{1}00\rangle}/\mu_{{\rm sat}\langle 0001\rangle}$ was 0.86 for 4H-SiC, 2.88 for 6H-SiC). The small anisotropy in 4H-SiC and large anisotropy in 6H-SiC inversion layers reflect the anisotropy of bulk electron mobility. $\mu_{\rm eff}$s in 4H-SiC MOSFETs fabricated on the $(11\bar{2}0)$ face for the current directions of $\langle 0001 \rangle$ and $\langle 1\bar{1}00 \rangle$ are almost the same due to a poor ohmic contact of source/drain at low drain voltages as observed in Fig. 1(a). A very high channel mobility was obtained in 4H- and 6H-SiC MOSFETs on the $(11\bar{2}0)$ face compared with that on the (0001) face (μ_0=95.9 $\rm cm^2/Vs$ vs. 5.59 $\rm cm^2/Vs$: 17 times higher in 4H-SiC, μ_0=115.7 $\rm cm^2/Vs$ vs. 44.8 $\rm cm^2/Vs$: 2.5 times higher in 6H-SiC).

A high $V_{\rm T}$ observed in 4H-SiC MOSFETs on the (0001) face ($\sim$ 8V) is caused by a lot of negative charges at the MOS interface (both negatively-charged interface states and near-interface traps in SiO_2 [6]). So, low $V_{\rm T}$ ($\sim$ 4V) 4H-SiC MOSFETs on the $(11\bar{2}0)$ face have fewer negative charges, and hence a dramatic improvement of the channel mobility of MOSFETs on the $(11\bar{2}0)$ face can be explained by the reduced scattering of electrons. In 6H-SiC, though almost the same $V_{\rm T}$s were obtained for MOSFETs on both the $(11\bar{2}0)$ and the (0001) faces, a higher channel mobility of 6H-SiC MOSFETs along $\langle 1\bar{1}00 \rangle$ on the $(11\bar{2}0)$ face than on the (0001) face was observed. This indicates that the MOS interfaces on the $(11\bar{2}0)$ face have essentially superior properties than that on the (0001) face. Shenoy *et al.* [4] reported a higher interface state density of 6H-SiC MOS capacitors on the $(11\bar{2}0)$ face than on the (0001) face. More detailed investigation is required for the $SiO_2/SiC(11\bar{2}0)$ interface.

In order to examine the scattering mechanism of electrons in inversion layers, MOSFETs were characterized at various temperatures between 100K and 500K. The temperature dependence of low-field mobility (μ_0) in 4H- and 6H-SiC MOSFETs fabricated on the $(11\bar{2}0)$ and (0001) faces are shown in Figs. 3(a) and 3(b). To the authors' knowledge, a decreasing mobility with increasing temperature above 200K is observed for the first time for 4H-SiC MOSFETs. These characteristics are important to prevent power MOSFETs from break-down due to enhanced drain current at elevated temperatures. 4H-SiC MOSFETs on the (0001) face show an increasing mobility with increasing temperature above 300K as shown in Fig. 3(a), similar to those in the references [7,8]. Though μ_0s in 6H-SiC show negative temperature dependences for both MOSFETs on the $(11\bar{2}0)$ and the (0001) faces, μ_0 on the (0001) face has little temperature dependence. The temperature dependences above 200K of μ_0 on the $(11\bar{2}0)$ face for 4H- and 6H-SiC are $\mu_0 \propto T^{-2.2}$ and $T^{-2.3}$, respectively, which is mainly governed by phonon scattering. However, 4H-SiC MOSFETs fabricated on the (0001) face show a positive temperature dependence of $\mu_0 \propto T^{2.6}$ above 300K. At high temperatures, a lot of electrons captured by acceptor-like interface traps were emitted, and then negative charges at the interface decreased. Thus, the increase of μ_0 at higher temperatures is caused by the reduction of Coulomb

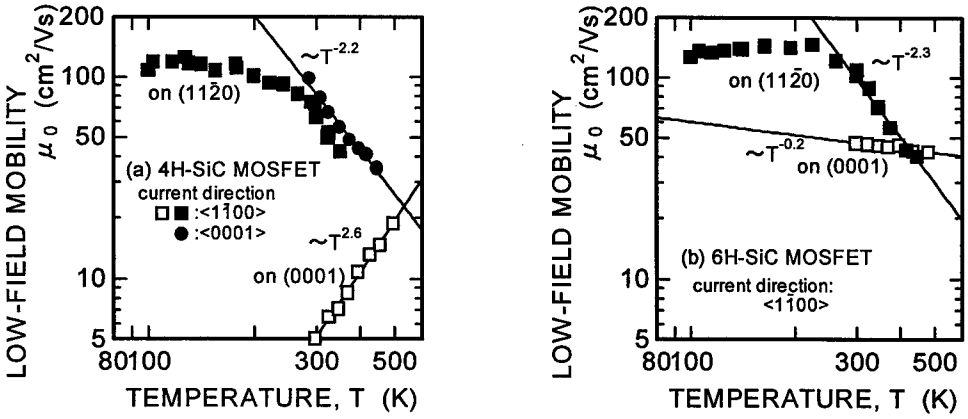

Fig.3: Temperature dependence of low-field mobility (μ_0) in (a)4H- and (b)6H-SiC MOSFETs on (11$\bar{2}$0) and (0001) faces.

scattering. In fact, 4H-SiC MOSFETs on the (0001) face showed a significant reduction of threshold voltages from 8V to 2.7V in the temperature range between 300K and 500K due to the reduction of negative charges at the MOS interface. While the threshold voltage on the (11$\bar{2}$0) face was almost a constant of 4.3V from 300K to 420K.

4. Conclusions

An anisotropy of channel mobility in inversion layers of 4H- and 6H-SiC was reported for the first time. The small and the large anisotropy in 4H- and 6H-SiC reflect the anisotropy in the bulk, respectively. A dramatic improvement of inversion channel mobility was achieved especially in 4H-SiC by utilizing the (11$\bar{2}$0) face compared with the conventional (0001) face. The high channel mobility and its negative temperature dependence of MOSFETs on the (11$\bar{2}$0) face indicate that the (11$\bar{2}$0) face is a suitable orientation for MOS devices.

Acknowledgement

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MOSFET Performance of 4H-, 6H-, and 15R-SiC Processed by Dry and Wet Oxidation

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Keywords: 15R-SiC, Channel Mobility, Interface State, MOSFETs, Near-interface Traps, Polytype, Threshold Voltage

Abstract: Polytype dependence of MOSFET performance in SiC(0001) was investigated. 4H-SiC MOSFETs showed a quite low channel mobility and a high threshold voltage, which seemed to be attributed to a high density of acceptor-like interface states and near-interface traps in SiO_2 near the conduction band edge of 4H-SiC. The threshold voltage of 15R-SiC MOSFETs was almost the same as of 6H-SiC MOSFETs, and the relation of channel mobility between 15R- and 6H-SiC is similar to the bulk mobility (15R-SiC is higher than 6H-SiC), which indicates that the MOS interface properties are comparable for 15R- and 6H-SiC. The oxidation ambient dependence of interface states is also discussed.

1. Introduction

SiC MOSFETs have been recognized as high-speed switching and low-loss power devices. 4H- and 6H-SiC are the most advanced polytypes in wafer fabrication, epitaxial growth, and device processing. However, 4H-SiC MOSFETs have a low inversion channel mobility [1], which brings a higher on-resistance than a theoretically expected value, regardless of a high bulk mobility. Though 6H-SiC MOSFETs show rather high channel mobility [2], 6H-SiC has an essential problem of a low bulk mobility along the c-axis due to a large anisotropy in mobility [3]. 15R-SiC is another choice for power MOSFETs [4] because of a higher electron mobility [5] and smaller anisotropy [3] than 6H-SiC. In addition, a smaller band gap of 15R-SiC avoids the negative influence of near-interface traps [6] located in the energy level between the conduction band edges of 4H- and 6H-SiC. In this paper, the difference of MOSFET performances in 4H-, 6H-, and 15R-SiC is reported. Effects of oxidation ambient (dry or wet) on the MOSFET performance are also discussed.

2. Experiments

N-channel planar MOSFETs were fabricated on B-doped p-type epilayers grown on (0001) Si-face substrates of 4H- and 6H-SiC (p-type, modified Lely) and 15R-SiC (n-type, Lely). The thickness and the acceptor concentration of epilayers were 4μm and $5\sim9\times10^{15}$ cm^{-3}, respectively. The source and drain regions were formed by multiple N^+ ion implantations at room temperature with a total dose of 8×10^{14} cm^{-2}. Post-implantation annealing was carried out at 1550°C for 30min in Ar. After RCA cleaning and H_2 annealing [7] at 1000°C for 30min, the samples were oxidized to form a gate oxide at 1150°C in dry oxygen for 3h or wet oxygen for 2h, resulting in a thickness of about 40nm. Post-oxidation annealing was done in Ar at the oxidation temperature for 30min. The ohmic contacts for source and drain were Al/Ti alloyed at 600°C for 60min in Ar, and the gate electrode was Al. The channel length (L) and width (W) were 30 and 200μm, respectively.

3. Results and Discussion

All MOSFETs showed clearly the linear region and the saturation region in the output

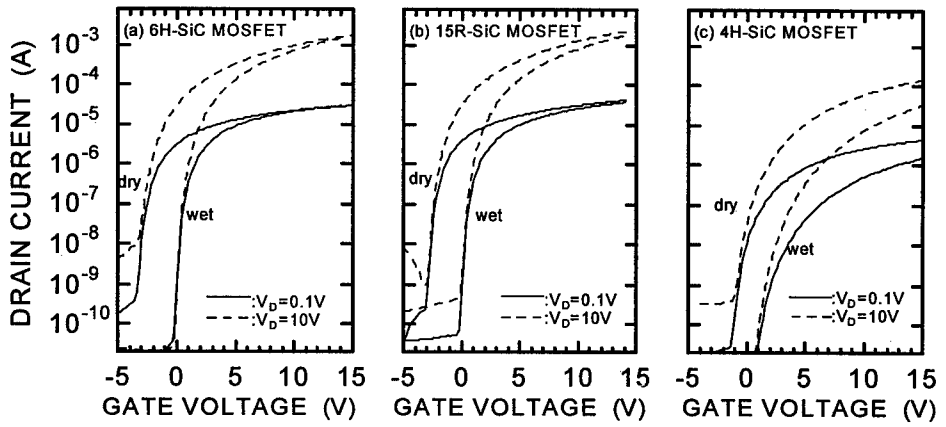

Fig.1: Transfer characteristics (log scale) of (a) 6H-, (b) 15R-, (c) 4H-SiC MOSFETs.

characteristics.

Figure 1 shows the transfer characteristics (log scale) at drain voltages (V_D) of 0.1 and 10V for 6H-, 15R-, and 4H-SiC MOSFETs processed by dry and wet oxidation. Although similar performances were obtained for 6H- and 15R-SiC MOSFETs (Figs.1 (a), (b)), a low drain current (I_D) was observed for 4H-SiC MOSFETs (Fig.1 (c)). The effective mobility (μ_{eff}) and the threshold voltage (V_T) were extracted from the linear-scaled transfer characteristics, shown in Fig.2, in the linear region of $V_D = 0.1$V. The values of the effective mobility and the threshold voltage for all MOSFETs are listed in Table 1. The fixed charge density (Q_f) is calculated from the following equation:

$$Q_f = \frac{C_{ox}}{q}\{V_T - V_T(\text{theory})\}, \quad (1)$$

where C_{ox}, q, and V_T(theory) are the capacitance of the gate oxide, the electronic charge, and theoretical threshold voltage, respectively. The fixed charge density obtained here includes both real fixed charges and carriers (electrons in this case) trapped at interface states. In the case of negative value of Q_f, it means that negative charges exist at the MOS interface.

Table 1: Average values of effective mobility, threshold voltage, and fixed charge density of MOSFETs for different polytypes and oxidation conditions.

oxidation	dry			wet		
polytype	4H	6H	15R	4H	6H	15R
μ_{eff} (cm^2/Vs)	6.27	37.4	47.3	4.96	36.7	49.5
V_T (V)	2.74	−1.44	−1.19	7.91	1.49	1.56
V_T(theory) (V)	0.81	0.83	0.61	1.05	0.54	0.53
Q_f ($\times 10^{11} cm^{-2}$)	−10.1	11.0	9.0	−34.9	−5.8	−5.7

V_T(theory) : theoretical threshold voltage.
Q_f : fixed charge density, includes both real fixed charges and carriers trapped at deep interface states.

As shown in Table 1, 4H-SiC has a quite low channel mobility (5~6cm^2/Vs) and a high positive threshold voltage (3~8V), particularly in wet oxidation samples. So, a large number of negative charges at the 4H-SiC MOS interface (both negatively-charged acceptor-like interface states and near-interface traps [6]) may act as scattering centers and reduce the channel mobility. These interface states and traps are generated more by wet oxidation, resulting in a higher threshold voltage (8V) than that by dry oxidation (3V).

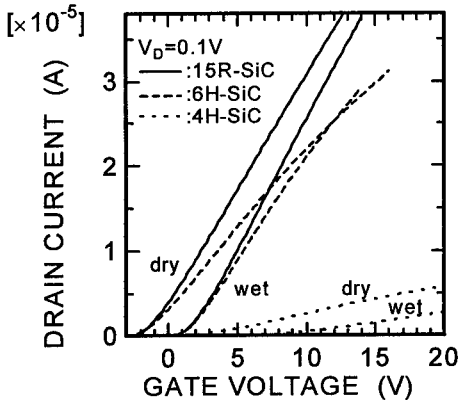

Fig.2: Transfer characteristics (linear scale) for the linear region of 4H-, 6H-, and 15R-SiC MOSFETs.

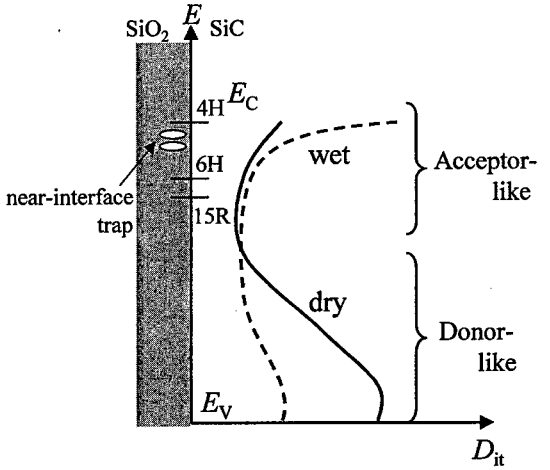

Fig.3: Model for the distribution of SiC MOS interface states.

For 6H- and 15R-SiC, dry oxidation samples have negative threshold voltages owing to positive fixed charges. Especially, p-type 6H-SiC MOS capacitors fabricated simultaneously adjacent to MOSFETs showed a large negative flatband shift (–18V). The main cause of this shift was positively-charged donor-like interface states [8], and some shift was caused by positive fixed charges. Though p-type 15R-SiC MOS capacitors were not characterized in this experiment because of n-type substrate, their characteristics are considered to be similar to 6H-SiC MOS capacitors. Using wet oxidation, a dramatic improvement of flatband shift (–1V) in p-type 6H-SiC MOS capacitors was realized by the reduction of donor-like interface states. However, the channel mobility is almost the same for dry and wet oxidation samples of 6H- (37cm^2/Vs) and 15R-SiC (50cm^2/Vs). Even though a large number of donor-like interface states exist in dry oxidation samples, they are neutralized by injected electrons in the inversion layer from the source region, and so the reduction of donor-like interface states by wet oxidation does not lead to an improvement of channel mobility. A higher channel mobility can be obtained using 15R-SiC compared to 6H-SiC, probably due to a higher bulk mobility [5] and almost the same interface state density. So, 15R-SiC is a promising polytype for power MOSFETs because of the higher bulk and channel mobility and the smaller anisotropy.

Based on the above discussion, a model for SiC MOS interface-states distribution processed by dry and wet oxidation is illustrated in Fig.3. In this model, it is assumed that the interface states in the upper half of the band gap are acceptor-like and those in the lower half of the band gap are donor-like. Under the flat band condition for p-type MOS capacitors, a large part of interface states are above the Fermi level, then the acceptor-like interface states are neutral and the donor-like interface states are positive. So, the p-type MOS capacitors processed by dry oxidation, which have a lot of donor-like interface states in the lower half of the band gap, indicate the large negative flatband shift. The dramatic reduction of negative flatband shift in the p-type MOS capacitors processed by wet oxidation is attributed to reduced donor-like

interface states as illustrated in Fig.3 in the lower half of the band gap. Concerning with the impact of interface states on the channel mobility of MOSFETs, the acceptor-like interface states in the upper half of the band gap, particularly near the conduction band edge for each polytype, are an important factor to determine the value of channel mobility. The extremely low channel mobility of 4H-SiC MOSFETs may be attributed to a high density of acceptor-like interface states near the conduction band edge of 4H-SiC [4], particularly in wet oxidation samples. Furthermore, there exist inherent electron traps in SiO_2 (near-interface traps) [6] between the conduction band edge of 4H- and 6H-SiC. So the 4H-SiC MOS interface has a lot of scattering centers of carriers, which reduce the channel mobility to an extremely low value. In 6H- and 15R-SiC, the acceptor-like interface state density seems to be comparable for dry and wet oxidation samples because of the little effect of the oxidation ambient on the channel mobility.

4. Conclusions

The difference of MOSFET performances in 4H-, 6H-, and 15R-SiC with different gate oxidation ambients (dry or wet) are reported. The distribution of interface states for different polytypes and oxidation ambients are also discussed. MOSFETs fabricated on 4H-SiC showed a low channel mobility in spite of a high electron mobility in the bulk. This fact seems to be due to a high density of acceptor-like interface states near the conduction band edge of 4H-SiC and near-interface traps. More acceptor-like interface states are generated using wet oxidation, which is derived from the higher threshold voltage and lower channel mobility than using dry oxidation. The little difference of threshold voltage in 6H- and 15R-SiC MOSFETs for each oxidation means similar property of the MOS interface for 6H- and 15R-SiC. A higher channel mobility of 15R-SiC than 6H-SiC is due to a higher bulk mobility. In addition to the higher channel and bulk mobility, a small anisotropy of the bulk mobility is desirable, so 15R-SiC is a promising polytype to application for power MOSFETs.

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Interface Trap Profiles Near the Band Edges in 6H-SiC MOSFETs

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Keywords: Capacitance-Voltage Measurements, Interface Trap, Interface Trap Profiles, MOS

Abstract: The interface trap density Dit(E) has been profiled versus energy in the bandgap for 6H-SiC MOS devices. A modified "low-frequency" capacitance-voltage technique is presented which allows trap densities to be independently profiled close to the conduction and valence band edges. Results show that Dit(E) is much higher close to both band edges than the average (midgap) value. These results show that the low transconductance typically reported for n-channel 6H-SiC MOSFETs is caused by trapping of inversion layer electrons at the SiC/SiO_2 interface.

Introduction: There has been considerable recent progress in fabricating high-quality MOS structures on SiC. Reported Dit values are now as low as mid-10^{10} traps/cm^2-eV [1]. However, the best reported inversion layer mobilities for 6H-SiC MOSFETs are typically ~50-100 cm^2/V-s which is considerably less than 50% of the bulk mobility (~300 cm^2/V-s). Recent Hall measurements on MOSFET inversion layers reveal substantial electron trapping at the oxide/SiC interface which is inconsistent with the sample's apparently low average Dit (~1-2x10^{11}) [2]. It has been proposed that poor mobility and high trapping in "low Dit" samples can be explained if Dit increases very rapidly near the conduction band edge [2-5]. In this work, we report capacitance-voltage (C-V) measurements on 6H-SiC which show high Dit near the conduction band (E_c) edge, consistent with this hypothesis.

Experimental "low-frequency" C-V technique: Accurate measurement of Dit in SiC MOS devices can be difficult. Due to the large band-gap of SiC, most interface traps are not in equilibrium with the (changing) applied gate voltage at room temperature. Although equilibrium C-V measurements such as quasi-static C-V used for silicon MOS devices [6] could be performed at ~300°C or higher, we find that Dit in our samples degrades (i.e., increases) when the samples are cycled above ~200°C, preventing this approach. Furthermore, the higher the measurement temperature, the more difficult it is to measure Dit close to the band edges.

In this work, C-V measurements have been obtained on n-channel MOSFETs with n+-source and drain tied to the p-type substrate. The source and drain act as a source of minority carriers (electrons), so that an "effective" low-frequency C-V curve can be obtained. This is similar to quasi-static C-V [6] where a slow dc sweep rate is used, allowing equilibrium to be maintained by thermal generation of minority carriers. Here, the rate-limiting step is electron conduction in the MOS inversion layer (from the source or drain to the center of the MOSFET channel). It is important to recognize that although both free carrier densities (minority and majority carriers) are in equilibrium with the applied dc bias, the occupancy of interface traps far from the band edges is not, since the emission rate for carriers trapped in these states is very long (~10^{16} s for midgap traps at 22°C!). The key to the C-V measurement technique here is that equilibrium of the traps is re-established only in strong accumulation or inversion when the trapped carriers are removed not by emission

(which is slow) but rather by recombination with high densities of free carriers in the accumulation/inversion layers (which is fast). Thus, although the C-V data obtained in these measurements looks like classic low-frequency data, the standard quasi-static analysis cannot be applied, since most traps are not in equilibrium.

Experimental devices and results: Polysilicon gate, n-channel MOSFETs were fabricated using a non-self-aligned process at the Northrop Grumman Corporation. The 6H-SiC starting wafers have a 10 μm thick, lightly doped (~$3x10^{15}$ /cm^3) p-type epi over a heavily doped P+ substrate. After a standard RCA clean, a 32 nm gate oxide was grown wet at 1100°C for 3 hours, followed by a wet re-oxidation at 950°C for 2.5 hours to obtain a lower Dit [1]. Other details of the fabrication process are described elsewhere [7].

The capacitance was measured on large area (W/L=100/100 μm) MOSFETs. A comparison between a theoretical low-frequency C-V curve and experimental data is shown in Fig. 1 (the theoretical curve was arbitrarily centered on the experimental data). As discussed above, all interface traps should be in equilibrium at flatband and inversion. Thus, average Dit can be calculated from $Dit_{av}=C_{ox}\cdot(\Delta V_{fb}+\Delta V_{th})/(q\cdot\Delta E)$, where ΔE is the energy from flatband to inversion, C_{ox} is the oxide capacitance, and $(\Delta V_{fb}+\Delta V_{th})$ is the total voltage difference between experimental and theoretical curves from flatband to inversion. For the device in Fig. 1, $(\Delta V_{fb}+\Delta V_{th})$=1.79 V, ΔE=2.54 eV, and Dit_{av} = $4.8x10^{11}$ traps/cm^2-eV. (Note: for convenience, V_{th} is defined here at the same capacitance value as at flatband. In Fig. 1, this point is about 0.07 eV closer to the conduction band edge than the normal definition of inversion for a MOSFET, $\varphi_s = 2\,\varphi_{bulk}$, but is easier to define experimentally.) The energy range ΔE over which Dit_{av} is measured at a single temperature is shown by the shaded region in Fig. 2.

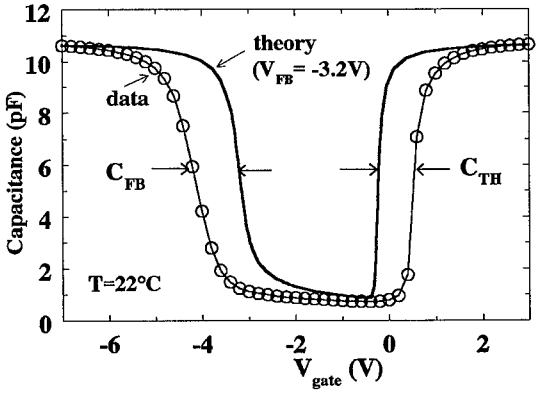

Figure 1. Comparison of theoretical low-frequency C-V with 1 kHz experimental data at 22°C for 6H-SiC MOSFET.

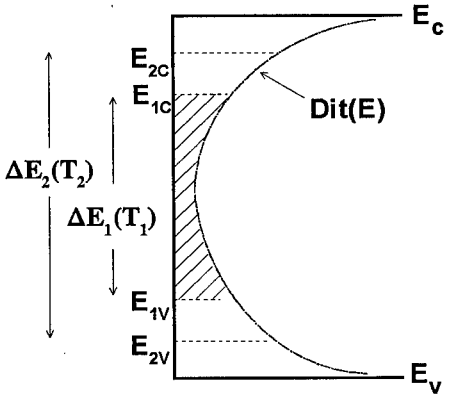

Fig. 2. SiC band diagram showing how Dit(E) is calculated by changing the sample temperature (see text).

A profile of Dit(E) can be obtained by changing the sample temperature, since the energy range ΔE depends on temperature, analogous to the Gray-Brown technique [8]. As shown in Fig. 2, when the temperature is lowered from T_1 to T_2, the Fermi levels at flatband and inversion move towards the valence and conduction bands, respectively. By monitoring the changes in gate voltages at flatband and threshold, it is possible to calculate Dit in the energy ranges (E_{1C}-E_{1V}) and (E_{2C}-E_{2V}). At each temperature, a theoretical low-frequency C-V curve is calculated as in Fig. 1, and then changes in $\Delta V_{fb} + \Delta V_{th}$ in excess of the predicted change are due to the charging of interface traps in those energy ranges.

An example of typical C-V temperature dependence is shown in Fig. 3. This chip was measured using an MDC variable temperature probe station. (Other devices were bonded in 28-pin ceramic DIPs and mounted in a vacuum cryostat capable of 77-600K operation.). The gate voltage required to swing the MOSFET from flatband to inversion decreases at higher temperature because the energy range from flatband to inversion decreases, leading to less charge in the interface traps. Note that the temperature–dependent shifts at flatband and threshold are very roughly the same, indicating that Dit is high near both band edges.

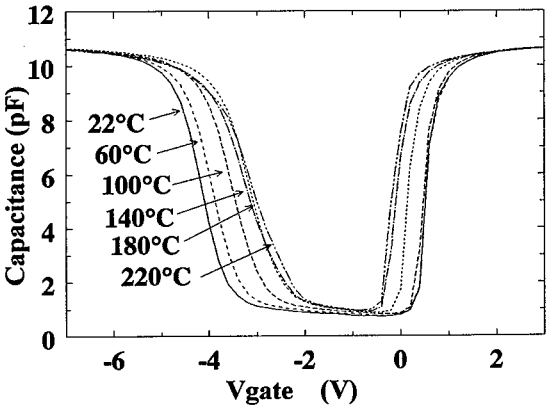

Figure 3. Low-frequency C-V data for the same MOSFET as in Fig. 1 from 19 to 220°C.

Using this analysis technique, Dit(E) profiles for two samples are shown in Fig. 4. Triangle symbols are calculated for the sample in Fig. 3 at 20-220°C; circle symbols are for a second sample measured from –120 to 200°C. Agreement between the two samples is good. Dit(E) is in the mid-10^{12} range at 0.1-0.4 eV from both band edges. This is more than an order of magnitude higher than the *average* mid-gap Dit value (obtained at 200°C), indicated by the dashed line. Qualitatively similar results showing high Dit values near the band edges have been reported previously for 6H-SiC MOS samples [3,4].

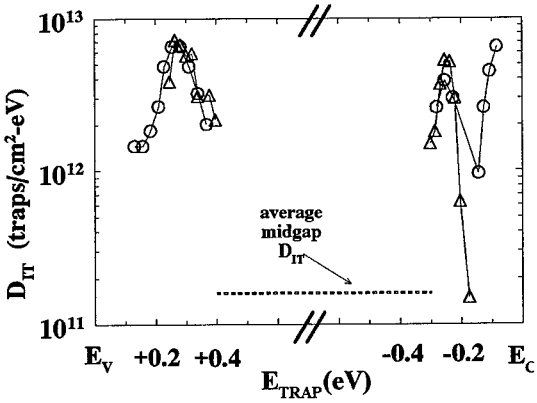

Figure 4. Dit(E) for two different devices from the same wafer. Dit near the band edges (symbols) is much higher than the *average* Dit over the central 2.2eV of the bandgap (dashed line).

In Fig. 4, approximately symmetric Dit peaks are observed at ~0.25 eV above Ev and below Ec in both samples. We speculate that such symmetric peaks could arise from a single amphoteric defect at the 6H-SiC/SiO_2 interface, similar to amphoteric behavior observed for silicon dangling bonds at the Si/SiO_2 interface [9]. We also observe a strong increase in Dit close to the conduction band edge (but not at the valence band edge), which might arise from conduction band tail states. However, it is clearly desirable to have much more data, including from oxides prepared in different ways, before reaching any firm conclusions about the details of these Dit distributions.

It should be recognized that profiling Dit by changing the temperature is a relatively insensitive technique, and therefore can only be used effectively on samples with high Dit. For example, for the samples in Figs. 3-4, a 10°C change in the temperature (at 22°C) causes only a small change in the surface potential at flatband ($\Delta\varphi$ = 8.7 mV), resulting in the discharging of relatively few interface traps. The corresponding change in the gate voltage (ΔV_g) is only ~70 mV. It is therefore very important that other sources of C-V instability, such as ionic contamination of the oxide, etc., be negligible for this analysis to work properly. In order to investigate this possible error source, C-V

curves were compared for forward and reverse sweep directions of the gate voltage. Ionic conduction, or other bias dependent instabilities, should be evident as a C-V shift between the two sweep directions. No such hysteresis is typically apparent either at 20°C (Fig. 5) or 200°C (not shown). Some hysteresis is observed below about -100°C near flatband only, which is believed to be related to freezeout of the dopant in the p-type substrate. We conclude that ionic contamination was not a problem in these samples.

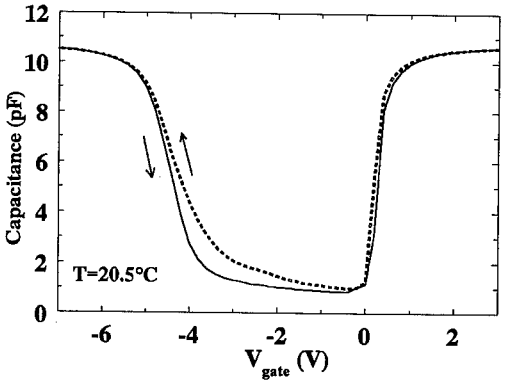

Figure 5. Comparison of C-V data for forward and reverse V_{gate} sweep direction at 20.5°C.

An additional source of error here is the creation of new interface traps during the C-V measurements. An example is shown in Fig. 6 for a sample before and after measurement at 320°C. More traps appear to exist in this sample following cycling to high temperature. Gate bias plays a clear role in this process because no changes in Dit are observed for cycling of unbiased samples to the same temperature. To minimize this effect, the maximum temperature was limited to ~220°C.

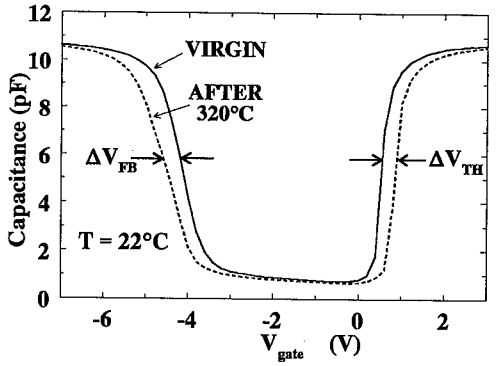

Figure 6. Comparison of C-V data at 22°C before and after C-V measurements at 320°C.

Summary: Dit has been profiled near the band edges using a new low-frequency C-V procedure on large 6H-SiC MOSFETs. This measurement approach has several advantages: it is simple to implement, Dit profiles are obtained near both band edges with a single sample, and it is possible to obtain profiles very close to the band edges. Disadvantages include requiring MOSFETs (as opposed to simpler-to-fabricate MOS capacitors) and a high sensitivity to C-V instabilities. Dit(E) is found to be very high near the conduction and valence band edges (mid-10^{12} traps/cm^2-eV) compared to the average midgap value (low-10^{11} range). This is consistent with strong trapping of inversion layer carriers observed in Hall experiments [2], and it is probably the cause of the low effective mobilities generally reported for SiC MOSFETs.

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Materials Science Forum Vols. 338-342 (2000) pp. 1117-1120

Characterization of SiC MOS Structures using Conductance Spectroscopy and Capacitance Voltage Analysis

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Keywords: Conductance Spectroscopy, CV Analysis, Interface State, Re-Oxidation

Abstract. We find that re-oxidation anneal of thermally grown dry oxides on 6H-SiC results in a significant reduction of the average interface state density. At the same time there are indications that negative charge is formed within the oxide. No significant differences are seen between p- and n-type samples in terms of interface state density or effective oxide charge. We find that re-oxidation using pyrogenic steam has a similar effect on the interface state densities and effective oxide charge as the use of steam produced by boiling water.

Introduction

The use of so called "re-oxidation" anneal to improve the quality of the SiO_2/SiC interface has been investigated recently [1-3]. This method appears to be one of the best ways of obtaining low interface state density at the SiO_2/SiC interface. Re-oxidation consists of a simple heat treatment at 950°C in wet ambient after the oxidation (wet or dry) is formed. The origin of the interface improvement observed is presently unknown but there is a negligible oxidation of SiC at such a low temperature. For some reason most research groups obtain the wet re-oxidizing ambient by bubbling a carrier gas through boiling deionized water instead of using the more conventional pyrogenic steam method for silicon where high purity hydrogen and oxygen gas are intermixed within the furnace to produce water vapor. In this work we compare these two methods of re-oxidation.

Experimental

MOS capacitors were made on commercially available 5 μm 6H-SiC epitaxial layer grown on the Si face of an N or Al doped SiC substrate. The epilayer doping concentration was $1.3x10^{16}$ cm^{-3} for the p-type material and $1.1x10^{16}$ cm^{-3} for the n-type material. The p-type samples were from two wafers from the same ingot while the n-type samples were pieces of the same wafer. Prior to the oxidation, the samples were cleaned using a modified RCA-clean. This clean consists of NH_4OH:H_2O_2:H_2O (1:4:20) at 80°C for 10 min followed by HCl:H_2O_2:H_2O (1:1:6) for 10 minutes at 80°C. The samples are immersed in 2% HF in between the cleaning steps. Thereafter the samples were loaded in at 700°C in oxygen ambient and ramped up to the oxidation temperature. Thermal oxidation was performed at temperatures between 1100 and 1150°C with duration between 4 and 6 hours. The wet oxidation was done using a pyrogenic steam. After the oxidation some samples were annealed for one hour in argon at the oxidation temperature. Thereafter the samples were ramped down in argon to 700°C for unloading, or down to 950°C were re-oxidation was performed in a pyrogenic steam or using water steam (boiling water) with Ar as a carrier gas. The re-oxidation period was 90 min or 180 min. No significant differences were seen between samples receiving different duration of re-oxidation. The samples were thereafter ramped down to 700°C in O_2, Ar or N_2 before unloading. The interface quality of the samples was not sensitive to the ambient gas used in this last process.

The oxide thickness varied between 260 Å and 650 Å depending on the oxidation temperature and conditions (dry or wet). A 0.5 μm thick aluminum layer or a transparent 150 Å thick gold layer was then evaporated on the oxidized side of the samples and lithographically patterned to form capacitors with areas ranging between 10^{-3} -10^{-4} cm^2. High frequency (1 MHz) C-V measurements and conductance spectroscopy were performed using a computer controlled HP4284A LCR meter and a temperature controlled probe station.

Analysis

Estimates of interface state densities and effective fixed charge were done using the photo CV technique at room temperature and conductance spectroscopy at elevated temperatures. Figure 1 shows typical CV curves of an n-type sample containing high density of interface states. The sample is first kept in accumulation in dark conditions for about a minute, then the voltage is swept rapidly (≈ 1 V/s) towards deep depletion. The waiting time in accumulation is to ensure a complete recombination of any minority carriers that are created during the illumination used while contacting the sample. The fast sweep rate towards depletion is to minimize carrier emission from deep interface states during the sweep. Most of the interface states are therefore occupied by a majority carrier at the end of the first sweep. The sample is then illuminated with focused white light for one minute, the light is then turned off and shortly thereafter the bias is swept slowly back towards accumulation. Majority of the interface states are emptied during this illumination period. During the backwards sweep, two processes occur. Firstly, inversion charge is removed from the interface at a certain surface potential (starts at ≈ - 20 volts). In the second process deep interface states recapture electrons from the conduction band which is seen as a small knee or ledge in the CV response (at ≈ - 13 volts). This ledge can be very difficult to resolve from the inversion ledge since the onset of removal of inversion charge and electron capture at interface states can occur at similar gate voltages. However, the interface state ledge can often be seen as a small peak in the parallel conductance data as seen in inset of figure 1. The inset shows the parallel conductance curves measured simultaneously as the capacitance spectra. The large peak close to 0 V is due to emission/capture from interface states that are in thermal equilibrium with the SiC, while the small peak at - 13 volts is due to a response from deep interface traps that are not in thermal equilibrium but capture electrons at a specific value of the surface potential (gate voltage).

The width of the interface state ledge (V_{it}) is a rough measure of the total number of interface states [4,5]. One has, however, to subtract the interface states with energy levels close to the SiC valence and conduction bands of which trapped carriers are able to follow the DC gate voltage. For reasonable capture cross section values ($\sigma \sim 10^{-15}$ cm^2) traps located less than about 0.6 eV away from the SiC band edges emit their charge during the DC bias sweep and do not contribute to the interface state ledge.

The effective fixed charge is in general very difficult to estimate in SiC MOS structures. In n-type samples it is estimated from the difference between the actual flatband voltage and the theoretical value. The assumption is made that most of the interface states are donors thereby not causing a shift of the CV curve during the sweep from accumulation towards depletion. In p-type material, however,

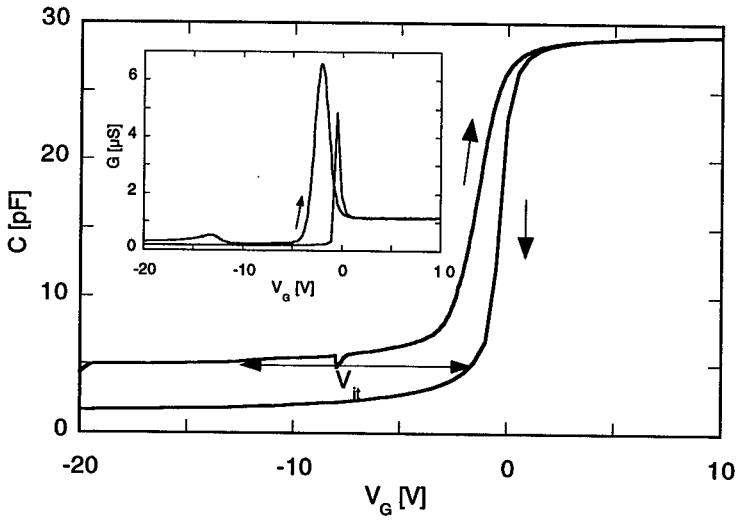

Figure 1. Capacitance voltage curves of an n-type sample after dry oxidation. The inset shows the corresponding parallel conductance curves.

the interface states are mostly empty during the sweep from accumulation towards depletion thereby causing a shift of the CV curve towards negative voltages. This is taken into account when the net effective charge is estimated in p-type samples. The assumption that most of the interface states are of donor type cannot be fully justified here. Other reports suggest that the neutrality level, i.e. the fermilevel at which the net charge of the interface is zero, is located well above midgap but further experiments are needed to verify this hypothesis [6].

The second estimate of the interface state density was obtained using conductance spectroscopy [7]. In this work the sample temperature was varied between room temperature and 200 °C. This temperature range gives an estimate of the interface state density within a narrow region of the bandgap approximately 0.3 - 0.6 eV away from the majority carrier band edge. A great uncertainty factor concerns surface potential fluctuations which complicate the data interpretation considerably [7,8]. Surface potential fluctuations with a standard deviation of typically 70-100 mV are observed as compared to the corresponding value of roughly 30 mV in our silicon MOS reference samples.The conductance values were corrected for series resistance effects as well as the surface potential fluctuations. Typically, a correction for such fluctuations results in an increase of the extracted interface state density by a factor of two to three.

Results and discussion

The first experiment concerned comparing wet and dry oxidation followed by re-oxidation. In short we found that our dry oxides were superior to the wet ones in terms of thermal stability and bias stressing in accumulation. The extracted average interface state densities of dry oxides were generally two times higher than of wet oxides but after the re-oxidation anneal the difference became insignificant.

Due to the instability of our wet oxides we will only detail the results of differently prepared dry oxides. Table I summarizes the extracted data. The interface state density was estimated from both conductance spectroscopy data and photo-CV data when possible. Even though the former method provides interface state density in a narrow region within the bandgap while the latter gives an average value the agreement between these two estimates was within experimental error (± 30 %). The effective oxide charge and the mobile oxide charge was estimated from the CV data. The first thing to note in the table is the insignificant effect of sacrificial oxidation. Secondly there are very small differences between n- and p-type material. The effect of re-oxidation on p- and n-type material is virtually the same in all cases. The re-oxidation anneal reduced the average interface state density in best cases down to the high 10^{11} $cm^{-2}eV^{-1}$ range and both re-oxidation methods give similar results. Figure 2 shows an example of CV curves after dry oxidation compared to samples receiving an additional re-oxidation anneal.

Unfortunately the boiling water introduced mobile charge in the oxide which is not detected in any other samples. An example of this is shown in figure 3. The CV curve is shifted towards negative voltages when sweeping from depletion (inversion) towards accumulation. This shift is fully reproducible and repeated measurements on the same capacitor give identical CV curves. This mobile charge is expected to vanish after careful cleaning of the water boiling apparatus.

Oxide	p-type 6H-SiC		n-type 6H-SiC	
	Q_{fc} [10^{11} cm^{-2}]	D_{it} [10^{11} $cm^{-2}eV^{-1}$]	Q_{fc} [10^{11} cm^{-2}]	D_{it} [10^{11} $cm^{-2}eV^{-1}$]
dry	8	36	1	20
dry+re-ox.	-7	9	-7	9
sacr.+dry	14	50	0	34
sacr.+dry+re-ox.	< 1	9	-10	12
sacr.+dry	4	43	0	33
sacr.+dry+re-ox. (H_2O)	-0.6	6	-10	9

Table I. Extracted parameters for differently prepared dry oxides. The oxides were grown at 1150 °C for a duration of four hours. "sacr." means sacrificial oxidation, i.e. the sample was oxidized twice and the first oxide removed in HF prior to the second oxidation. "re-ox" denotes re-oxidation treatment at 950°C for 3 hours.

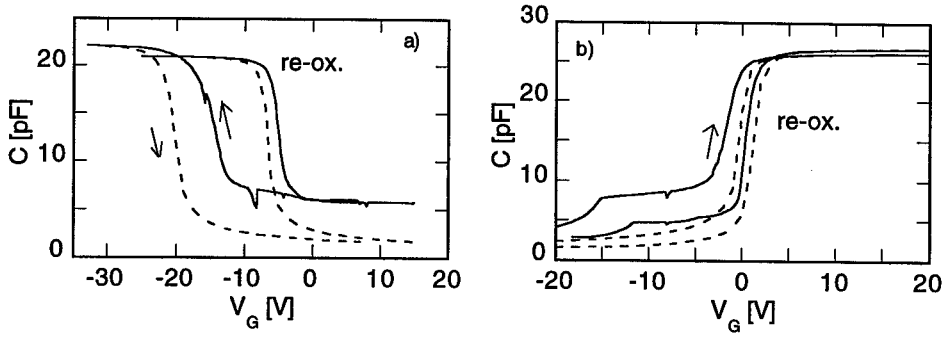

Figure 2. CV data showing the effect of re-oxidation after dry oxidation, a) p-type material, b) n-type material. Samples receiving re-oxidation show a positive flatband shift and a smaller hysteresis as compared to dry oxidation.

Concerning the effective oxide charge it appears as if re-oxidation produces negative charge in the oxide in agreement with recent observations of Yano et al [9]. However, the exact value of the effective fixed charge is highly uncertain since it relies solely on the assumption that all interface states are assumed to be donors. Still the similarities between the extracted data of n-and p-type material suggest that this procedure is a good approximation. If we instead assume equal densities of donors and acceptor states within the bandgap, with donors located in the lower half of the bandgap and acceptors in the upper half, we obtain the same qualitative result as above, i.e. the net oxide charge after re-oxidation still becomes negative, especially in n-type samples. It is also possible that the re-oxidation treatment has different impact on donor and acceptor states thereby changing the density ratio of donor and acceptor states and influencing the extracted effective oxide charge. More spectrocsopic information on the energy distribution and type of interface states is needed to conclude on this matter.

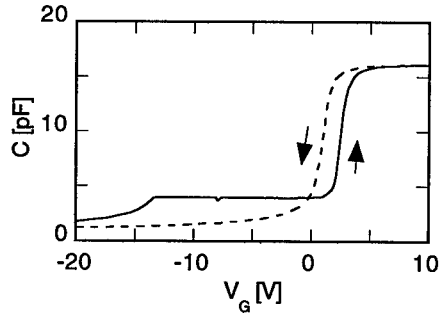

Figure 3. CV curves at room temperature of an n-type sample after dry oxidation and re-oxidation using boiling water. The broken line denotes the first sweep from accumulation to depletion while the solid line is the reverse sweep after illumination for one minute at - 20 V. The shift of the CV curve is fully reversible and is due to mobile charge, presumably sodium. The mobile charge is approximately $8x10^{11}$ cm^{-2} both in n- and p.type samples.

In summary we do not observe any significant differences in oxide quality between n- and p-type samples. The re-oxidation treatment reduces the number of interface states but seems to introduce unwanted negative charge in the oxide.

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Mobility in 6H-SiC n-Channel MOSFETs

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Keywords: Interface Trap, Mobility Degradation Coefficient, MOSFETs, Oxide Charge, Stress Effects

Abstract The effects of process-induced fixed oxide charge and interface-traps, as well as high-temperature stress-induced interface traps, on MOSFET mobility are investigated for *n*-channel 6H-SiC devices with 50-nm gate oxides, both thermally grown and deposited. MOSFET channel mobility in the limit of low interface charge is determined to be 167 cm^2/V-s in the thermal oxides, for an effective vertical field in the inversion layer of 0.14 MV/cm. Also reported for the first time are mobility degradation coefficients for process-induced and stress-induced charge centers in these oxides.

Introduction High-temperature, voltage-controlled silicon carbide (SiC) devices are required for future military and commercial electric-drive applications; e.g., future Army vehicles will require motor drive electronics to operate for 10,000 hours at junction temperatures of 300 °C and above. However, the achievement of high-quality, high-reliability gate oxides and passivation layers for SiC metal-oxide-semiconductor (MOS) devices for use in high-temperature and high-power applications remains elusive. Although several high mobility *n*-channel MOSFETs have been reported [1,2], most SiC MOS devices demonstrated to date exhibit low channel mobilities ($\leq$ 50 cm^2/V-s) [3,4], and the quality of the gate dielectric is largely responsible. We have initiated a study to understand and characterize the effects that oxide charge centers and interface traps have on the device characteristics and how their contributions may vary when the devices are subjected to stresses simulating operating conditions.

SiC Devices In this paper, we investigate 6H-SiC MOSFETs by Cree Research, Inc. [3], using three different oxide processes: wet thermal, dry-wet thermal, and low-pressure chemical vapor deposition (LPCVD). The wet thermal oxide was grown at 1025 °C, followed by a wet 950 °C reoxidation anneal. The dry-wet oxide was grown at 1100 °C in a dry ambient, followed by a wet 950 °C reoxidation anneal with the temperature ramp-down occurring under the wet ambient. The LPCVD oxide was also subjected to a wet 950 °C reoxidation anneal after deposition. All MOSFETs were fabricated using Al-doped epitaxial layers, with acceptor concentration in the mid 10^{15} cm^{-3} range and gate oxides that were nominally 500 Å thick. The source and drain diodes were implanted with nitrogen to 2×10^{20} cm^{-3} and activated with a >1600 °C anneal. The ohmic contact to the source and drain diodes was accomplished using Ni that was sintered, and sputtered Mo was used as the gate metal. The device width and length ranged from 100 to 200 μm and 4 to 8 μm, respectively, with width-to-length ratios of 12.5 to 50 and gate areas of 1×10^{-4} to 8×10^{-4} cm^2.

Experimental We characterized MOSFETs from two test chips from each of the thermal oxide lots and one test chip from the deposited oxide lot at room temperature and subjected a subset of these devices to electrical stress at 300 °C. In doing so, we attempted to investigate the impact of process-induced interface traps and fixed charge centers, as well as stress-induced interface traps on MOSFET mobility. It is important to identify the oxide process that not only provides the highest performance MOSFETs, but also which degrades the least under high-temperature operation. Standard *I-V* characterization techniques, as well as charge pumping were used to determine the mobility dependence on interface charge density. The threshold voltage V_t was extracted from plots of the drain current I_d and transconductance g_m versus gate voltage V_g in the linear region, and the effective mobility was calculated from the drain conductance [5]. Fig. 1 gives

effective mobility (at 25 °C) as a function of V_g-V_t for a MOSFET with a wet thermal oxide gate. All samples included in this study show this type of effective mobility behavior, which is qualitatively similar to the effective mobility dependence on inversion charge (and average vertical field in the inversion layer) reported for Si MOSFETs [6]. (Any samples that appeared to exhibit characteristics of activated transport at room temperature were not included in this study. *I-V* analysis using the methods of Ouisse [7] was employed to investigate this mobility behavior and will be discussed elsewhere.) All subsequent values of effective mobility used in this paper will be calculated for a V_g-V_t of 1.5 V which, for these devices, is associated with a free carrier inversion charge density of 7.2×10^{11} cm^{-2} experiencing an effective vertical field E_{eff} of 0.14 MV/cm. As indicated below, this inversion charge density is only a small fraction (16-29%) of the interface charge for these MOSFETs and, hence, screening effects should be small.

Measurement of Interface Charge The voltage shift of the extracted V_t relative to the theoretical V_t was used to indicate the net oxide charge, which includes the fixed oxide charge and the interface trapped charge. The charge pumping (CP) technique as described in [8,9] was used to measure the interface trap density. The number of fixed charges N_F per unit oxide area was deduced from these two measurements. The interface trap density N_{IT} per unit oxide area was measured using a trapezoidal CP gate signal with a fixed amplitude of 10 V, a frequency of 3.33 kHz, and a duty cycle of 0.25. At room temperature, using these CP parameters, a mean average interface trap density D_{IT} (in cm^{-2} eV^{-1}) is measured over the energy range of 2.2 eV (midgap ± 1.1 eV) and this average is used to estimate the N_{IT} over $2\phi_B$ (2.6 eV). Although a surface potential sweep of 2.6 eV is accomplished during the CP measurement, non-steady-state emission (upon which the CP measurement is based) occurs only over a 2.2-eV energy range. Only at temperatures near – 100 °C can CP measurements be made over the energy range of 2.6 eV. Table 1 gives the average N_{IT} and N_F for the MOSFETs with the three differently processed gate oxides. The variation at one standard deviation is included to demonstrate the range of measured numbers of interface charges. Note that the devices with the dry-wet gate oxides have the lowest number density of interface charge ($N_F + N_{IT}$), as well as the lowest value for N_F, while the devices with wet oxide gates showed the highest $N_F + N_{IT}$ with the highest value of N_{IT}. The devices with the deposited gate oxides had the lowest N_{IT}, but showed the largest value of fixed oxide charge, as might be expected for a deposited oxide. About 70% of the interface charge is contributed by interface traps for the thermal oxides.

Mobility Dependence on Interface Charge Following the analysis originally presented by Sun and Plummer [6] for Si MOSFETs, we use the empirical relationship between effective mobility and interface charge:

$$\mu_{eff} = \frac{\mu_o}{1+\alpha(N_F + N_{IT})}.$$

μ_{eff} is the effective mobility as described earlier, μ_o is the effective mobility in the limit of low interface charge

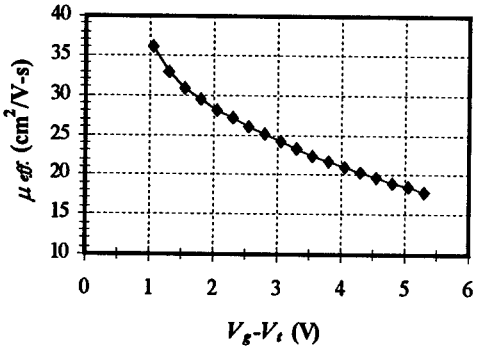

Figure 1. Effective channel mobility vs. V_g-V_t for 6H-SiC n-MOSFET with wet thermal gate oxide.

Table 1. Values of average N_{IT} and N_F with variation at one standard deviation for 6H n-MOSFETs with wet, dry-wet thermal, and LPCVD gate oxides. Values of process-induced α are also included.

Oxide Type	Average N_{IT} (over $2\phi_B$) (x 10^{12} cm^{-2})	Average N_F (x 10^{12} cm^{-2})	Process-Induced α (x 10^{-12} cm^2)
Wet	2.8 ± 0.8	1.6 ± 0.9	1.7
Dry-wet	1.9 ± 0.8	0.6 ± 0.5	
Deposited	1.3 ± 0.1	2.7 ± 1.3	0.55

($N_F + N_{IT} < 10^{10}$ cm^{-2}), and α is the mobility degradation coefficient, which is a combined measure of the effectiveness of Coulomb scattering of the free carrier inversion charge by both the fixed and interface trapped charges. Fig. 2 gives a plot of reciprocal effective mobility (for $V_g - V_t = 1.5$ V) as a function of $N_F + N_{IT}$ for MOSFETs with the three differently processed gate oxides. Linear extrapolation from the data on this chart provides an intercept, which gives μ_o and a slope that yields α (α = slope × μ_o). Good linear fits to the data are given for MOSFETs with wet thermal and deposited oxides, which give correlation coefficients of 0.93 and 0.98, respectively. Values for μ_o of 167 cm^2/V-s and α of 1.7×10^{-12} cm^2 are extracted from the wet thermal oxide data. Although this extracted value of μ_o is at least a factor of four improvement over the mobility values reported here (and is in good agreement with the theoretical work of Joshi [10]), it is significantly lower than the nominal bulk mobility value (400 cm^2/V-s) for the 5×10^{15} cm^{-3} acceptor doping of these devices. If we estimate the maximum channel mobility value for SiC in the limit of low interfacial charge using the data reported by Sun and Plummer [6] for Si MOSFETs (which gives approximately $\mu_o \approx 0.75\ \mu_{BULK}$), we should have a value around 300 cm^2/V-s. Since this value is still considerably higher than the present extrapolated value of 167 cm^2/V-s, we conclude that other effects, such as surface roughness are indeed contributing to the degraded mobility in these state-of-the-art SiC MOSFETs.

We were not able to obtain a fit to the dry-wet thermal data, since it falls over such a narrow range of $N_F + N_{IT}$, but these data points do fall along the linear fit to the wet oxide data quite well. When you consider the data sets for both thermal oxides as one, you cannot distinguish one from the other statistically, which suggests that both oxide types have a similar mobility dependence on interface charge. On the other hand, the deposited oxide mobility behavior is clearly different from that of the thermal oxides. The fit to this data provides a μ_o of 42 cm^2/V-s and an α of 5.5×10^{-13} cm^2. Such a low extracted value of μ_o could indicate that the deposited oxide interface is significantly rougher than that of the thermal oxides. The consumption of the semiconductor surface during the thermal oxidation may provide a smoother interface. The data points for the thermal oxides of Fig. 2 are replotted in Fig. 3, and a curve is fit through these data points according to equation (1). The lowest interface charge for this data set is about 2×10^{12} cm^{-2}, with an associated mobility of 40 cm^2/V-s. Fig. 2 indicates that the interface charge for these thermal oxides would have to be decreased to the mid 10^{11} cm^{-2} (about a factor of four) to increase the channel mobility to values near 100 cm^2/V-s.

Mobility Dependence on Stress-Induced Interface Traps We subjected all three types of MOSFETs to a moderate dc stress (2 MV/cm) at 300 °C for about 4 hours, in order to obtain mobility degradation coefficients α' for stress-induced interface traps. The post-stress changes in the device characteristics were

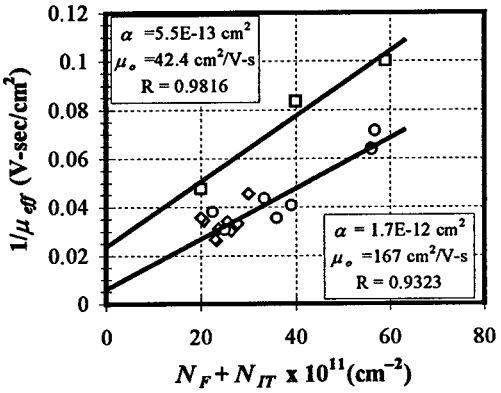

Figure 2. Reciprocal effective channel mobility vs. interface charge for MOSFETs with wet (circle) and dry-wet (diamond) thermal and LPCVD (square) gate oxides. Linear fits for the wet thermal and LPCVD oxide data are given.

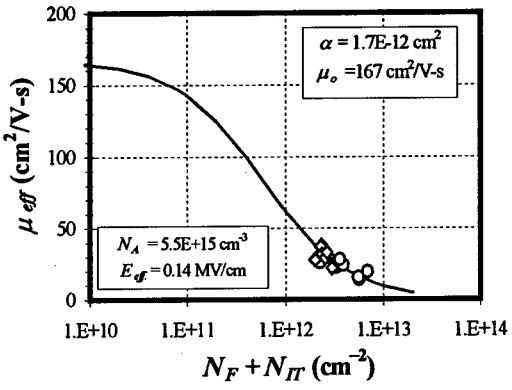

Figure 3. Effective channel mobility vs. interface charge for 6H n-MOSFETs with thermal gate

Table 2. Stress-induced interface trap density, pre- and post-stress channel mobility and the associated stress-induced α_{IT} for 6H n-MOSFETs with thermal and LPCVD gate oxides.

Oxide Type	δN_{IT} (over $2\phi_B$) (x 10^{12} cm^{-2})	μ_{pre} (cm^2/ V-s)	μ_{post} (cm^2/ V-s)	Stress-Induced α' (x 10^{-12} cm^2)
Dry-wet	1.7	28	6	2.1
Wet	1.0	33	14	1.3
Deposited	0.84	22	12	0.94

shown to be consistent with the stress-induced increase in interface traps by a self-consistent analysis, as outlined in Scozzie et al [11], and therefore values of α' were calculated using a relation similar to equation (1), $\mu_{POST} = \mu_{PRE}/(1 + \alpha' \delta N_{IT})$. δN_{IT} is the stress-induced net increase in interface traps over the energy interval of $2\phi_B$ (2.6 eV) in the midgap region and μ_{PRE} and μ_{POST} are the pre- and post-stress room-temperature effective mobilities, respectively. This relation was used by Galloway et al [12], in their investigation of the effects of radiation stress-induced oxide charge centers on the Si MOSFET characteristics. Table 2 gives a summary of one set of stress tests that includes the pre- and post-stress room-temperature measurements of channel mobility, with the corresponding stress-induced increase in interface-trap density and the resulting mobility degradation coefficients for all three types of 6H-SiC MOSFETs. As can be seen from this table, for similar stresses the deposited, wet and dry-wet oxides show increasingly larger amounts of δN_{IT} and the associated increasingly larger values of α'.

Summary We performed an initial investigation of the channel mobility dependence of 6H-SiC MOSFETs on process-induced and stress-induced charge centers for devices with wet thermal, wet-dry thermal, and LPCVD gate oxides. These oxides have average interface charge densities that range from 2.5 to 4.4 x 10^{12} cm^{-2}, with the dry-wet thermal oxide having the lowest charge. About 70% of the total interface charge in these oxides was composed of interface traps. The data analysis we have provided gives an estimate of effective channel mobility in the limit of low interface charge of 167 cm^2/V-s (for E_{eff} = 0.14 MV/cm) for the MOSFETs with wet thermal gate oxides. The data also suggests that the interface charge for these thermal oxides needs to be reduced to mid 10^{11} cm^{-2} in order to increase 6H MOSFET effective mobility values in current state-of-the-art devices from around 40 to 100 cm^2/V-s. Although the devices with dry-wet thermal gate oxides have the lowest interface charge and yield the highest mobilities, the stress data suggests that this oxide damages at a significantly higher rate than the wet thermal or deposited oxides. While the values of stress-induced α' for these devices compare favorably with those published for Si MOSFETs, the process-induced charge effects in SiC MOSFETs appear to be far more significant than those reported for Si devices.

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Effects of Oxidation Conditions on the Concentration of Carbon Dangling Bonds in Oxidized 6H-SiC

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Keywords: Carbon-Related Defects, Dry Heat-Treatment, Electron Paramagnetic Resonance, Thermal Oxidation

Abstract

In a previous study of oxidized 6H-SiC [1], we have used electron paramagnetic resonance (EPR) to observe a defect center that is present in SiC after oxidation and dry heat-treatment. The spectroscopic and annealing characteristics of this center indicate that it is likely a C dangling bond made EPR-active by the release of a hydrogen species during dry heat-treatment. In this study, we examine what effects different oxidation parameters have on the density of centers produced. We find that the termination procedures of the oxidation process have the largest effect on the concentration of centers. In addition, we compare our results with electrical studies preformed by others to examine what, if any, relationship exists between the defect center and electrically active defects.

Introduction

Studies of SiC are motivated by its prospects as a replacement for Si in microelectronic devices that operate at high powers or high temperatures. It is SiC's ability to form a SiO_2 dielectric layer by thermal oxidation that has generated significant interest in a SiC-based high power metal-oxide-semiconductor field-effect transistor (MOSFET). However, the development of the SiC MOSFET has been hindered by high concentrations of electrically active defects such as interface states and oxide charge traps. Unlike interface states in Si-based MOSFETs, which have been attributed at least in part to the interfacial Si dangling bond [2], no physical model for interface states in SiC has been generally accepted.

In a previous study of oxidized 6H-SiC, we have observed a defect center that is present in SiC after oxidation [1]. Dry heat-treating the oxidized sample forms the paramagnetic state of the defect, which can be detected with electron paramagnetic resonance (EPR). Because the defect center is activated by thermal treatments in ambients that eliminate moisture and is passivated in ambients that contain either moisture or H_2, the center appears to be revealed by the release of hydrogen or some hydrogenous species. The spectroscopic and activation characteristics of the center indicate that it is related to C [3-4]. Thus, we have identified the defect as a C-H complex, which becomes a carbon-dangling bond when the passivating hydrogen atom is freed during dry heat-treatment. Hydrofluoric acid etching studies indicate that the center is not located in the SiO_2.

In this investigation, we examine what effects altering the oxidation parameters has on the concentration of centers produced in the samples. Specifically, we have examined the effects of different unloading procedures and oxidation temperatures. These results are compared with the results of electrical studies preformed by others to determine if there is a relationship between this paramagnetic center and electrically active interface states.

Experimental

Our 6H-SiC samples are cut into 0.23 x 1.5 cm^2 strips from a double-side polished, p-type wafer supplied by Cree Research, Inc. We clean the samples by rinsing them in trichlorethane, zylenes, acetone, methanol, and deionized water for 5 min time intervals. Just before oxidation, samples are etched in a 9:1 H_2O:HF (50%) solution.

In our examinations of the effects of the unloading procedure, the oxidations are conducted for 6 hr at 1150 °C in O_2 bubbled through deionized water, which is heated to 95 °C. We have studied five methods of terminating the oxidation:

1. "Fast Pull" in a wet O_2 ambient
2. "Slow Pull" in a wet O_2 ambient
3. "Fast Pull" in a N_2 ambient
4. "Slow Pull" in a N_2 ambient
5. Extended "Reoxidation"

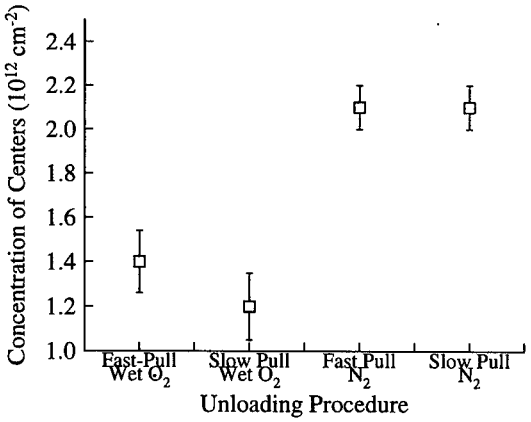

Figure 1: The effect of unloading ambient and procedure on the concentration of centers.

In the "Fast Pull" post-oxidation procedure, the samples are moved to an area of the furnace where the temperature is approximately 940 °C. They remain in this location for 5 min before they are removed from the furnace. In the "Slow Pull" procedure, the temperature of the furnace is reduced at the end of the oxidation to approximately 900 °C over a period of 1 hr, after which the samples are unloaded. The extended "reoxidation" procedure is similar to the "Slow-Pull" removal method in that after oxidation, the temperature of the furnace is reduced to 900 °C. However, the samples remain in the furnace with wet O_2 flowing for either 3 or 10 hr before they are unloaded. Following removal from the furnace, samples are heat-treated in dry (<0.3 ppm H_2O) N_2 for 200 min.

In our studies of the effects of oxidation temperature, we oxidized 4 samples for 6 hr according to the "Fast-Pull" procedure described above. This initial oxidation is necessary to remove damaged material that lies on the cut and polished surfaces of the SiC substrates. Following the initial oxidation, the samples were not dry heat-treated, instead the SiO_2 layer on the samples was stripped by etching in a HF solution. Following this, the samples were oxidized at either 950, 1050, 1150 or 1250 °C for another 6 hr and unloaded from the furnace using the "Fast Pull" technique. Following the second oxidation, the samples were heat-treated in dry N_2 for 200 min.

We examined the samples with EPR at room temperature using a Bruker 200 X-Band spectrometer. All measurements were made with 1 G peak-to-peak modulation amplitude and 1 mW microwave power. The absolute concentration of the center is determined by integrating the EPR spectrum with largest amplitude twice and comparing the result with a known standard. The concentration of the centers that remains in the samples is determined by comparing amplitudes. The error in the figures originates from EPR signal noise.

Results and Discussion

In figure 1, we plot the density of centers measured after dry heat-treatment as a function of the unloading procedure. We observe that removing the samples in a wet O_2 ambient produces the smallest center concentration. The data of figure 1 suggests that unloading the samples using the "Slow Pull" method reduces the center density but not to an amount that is greater than the measurement error. Thus, thermal shock does not appear to alter the concentration of centers. However, we observe that the density of centers is dependent upon the unloading ambient.

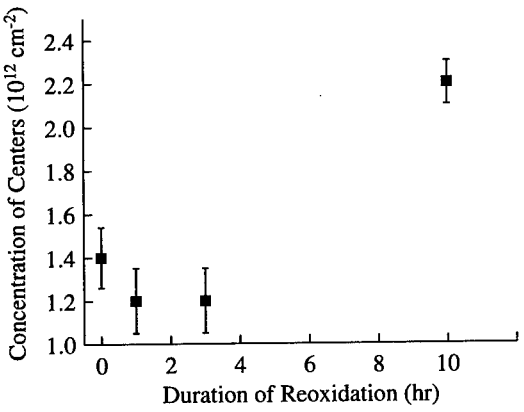

Figure 2: The effect of "reoxidations" of increasing duration on the concentration of centers. The "0" and "1" hr data points are the same as the "Fast Pull" and "Slow Pull" in a wet O_2 ambient points shown in the previous figure.

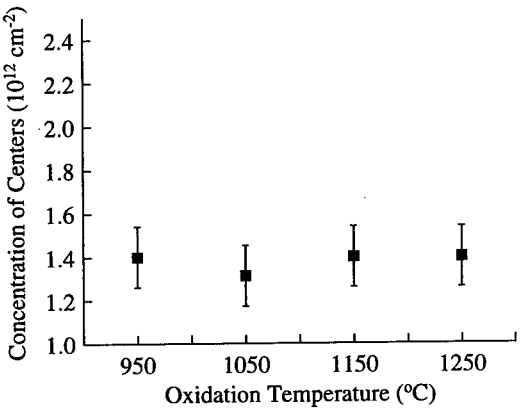

Figure 3: The effect of oxidation temperature on the concentration of centers.

Removing the samples in an oxidizing ambient produces smaller concentrations of centers than unloading the samples in an inert ambient.

Figure 2 shows the effects of reoxidizing the SiC samples. The 0 and 1 hr reoxidation data represent the center densities in the samples whose oxidations were terminated using the "Fast Pull" and "Slow Pull" wet O_2 procedures, respectively. The 3 hr and 10 hr reoxidation data correspond to the concentration of centers in the samples that were oxidized using the extended "reoxidation" method. We find that the sample subjected to the longest reoxidation had the largest concentration of centers. One possible explanation for this is that the defects could arise from a layer of silicon oxycarbide, which some have suggested forms at the SiC/SiO_2 interface [5-6].

In figure 3, we plot the concentration of centers as a function of the oxidation temperature. Each of the samples had approximately the same concentration of centers after dry heat-treatment regardless of the temperature of the oxidation. Thus, during each of the 6 hr oxidations approximately the same number of defects is created. Previous studies of SiC samples that were repeatedly oxidized at 1150 °C showed an increase in the concentration of centers during the early stages of oxidation [7-8]. This was followed by a decrease in the concentration. After oxidation times of eight hours, the density of centers appeared to reach a steady-state amount. In the time dependence study, we presented two alternate models to interpret the data. First, we suggested that the variation in center density with time may be related to the dependence of the C-H precursor formation on the oxidation kinetics. Alternately, the time dependence of the data may simply indicate that the C-H precursors are intrinsic to the SiC and are revealed as the successive oxidations remove more of the outer layers of SiC. Because the oxidation kinetics are expected to be different over the range of temperatures we have examined [9], it is unlikely that each oxidation would produce approximately the same center concentration if the C-H precursors were generated during oxidation. Thus, the precursors are likely hydrogen terminated intrinsic defects that are distributed throughout the SiC. If this is the case, then for these samples, the defect precursors appear to be distributed uniformly throughout the first 500 nm and 100 nm layers of material on the C and Si faces, respectively.

We observe an interesting similarity between the effect of reoxidation on the carbon-center measured in our work and the effect of reoxidation on electrically active defects studied by Lipkin

and Palmour [10]. It is important to note, however, that the processing procedure we use is slightly different from theirs. They incorporate an Ar anneal for 1 hr at the oxidation temperature before removing their samples immediately from the furnace. Our samples receive a similar post-oxidation treatment in our "Slow-Pull" in a N_2 ambient procedure. Lipkin and Palmour observe that reoxidation at 900 °C for 1 to 3 hrs reduces the concentrations of interface states by more than a factor of two as compared to removing the samples directly from the furnace in an Ar ambient. If we compare our "Slow-Pull" N_2 ambient result with our 1 hr and 3 hr reoxidation results, in both cases, we observe almost a factor of two decrease in concentration of centers. Thus, it appears that the C-dangling bond centers may be related to some electrically active defects. However, tandem EPR and electrical measurements using identically prepared samples are necessary to confirm this point.

If our centers are related to electrically active defects, the reoxidation results may indicate that the reoxidation process removes defects that are created during the Ar anneal. Because the anneal is an important processing technique for creating stabile oxides, we would not propose removing this step from the oxidation procedure. Rather, it would be interesting to examine what effect the addition of small concentrations of O_2 to the Ar ambient would have on the density of electrically active defects. It may be possible to eliminate the extra reoxidation step from the oxidation procedure without deteriorating the quality of the interfaces and oxides.

Conclusion

We have studied how the concentration of centers in oxidized 6H-SiC is affected by oxidation parameters including the unloading conditions and the temperature of oxidation. We observe that unloading the samples in an oxidizing ambient rather than an inert ambient reduces the density of centers. The concentration of centers may also be reduced by employing the "Slow Pull" unloading technique; however, the veracity of this effect is unclear due to the inherently large measurement error for this EPR signal. We observed that the center density does not appear to be affected by oxidation temperature. The effect of reoxidation seen in our samples is similar to that observed in studies of electrically active defects. However, proper correlation of our studies with the electrical investigations requires that samples for both EPR and electrical measurements be processed simultaneously.

Acknowledgments

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Effects of Steam Annealing on Electrical Characteristics of 3C-SiC Metal-Oxide-Semiconductor Structures

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Keywords: 3C-SiC, Interface Trap, LP-CVD, MOS, Oxide Layers, Oxide-Trapped Charges, Pyrogenic Oxidation, Steam Annealing

Abstract Annealing in steam at 800°C up to 8 hours was carried out for pyrogenic oxide layers formed on p and n-type cubic type silicon carbide (3C-SiC) epilayers, which were grown on silicon (100) substrates by low-pressure chemical vapor deposition. After the steam annealing, gold was deposited on the oxide layers (SiO_2) to form metal-oxide-semiconductor structures. Simultaneous capacitance-voltage characteristics were measured for these samples to obtain the flat-band voltage (V_{fb}) and the energy profile of interface trap density (D_{it}). The effects of the annealing in steam on the electrical characteristics of the SiO_2/3C-SiC interface are discussed based on a shift of V_{fb} and a change in the energy profile of D_{it}.

1. Introduction

It is considered that cubic type silicon carbide (3C-SiC) is a promising material for integrated circuits with high-performance specifications because it has the highest electron mobility (about 10^3 $cm^2/(Vs)$) among SiC poly-types and its crystal isotropy is of great advantage to designing device structures. Recently, it has been reported that 3C-SiC epilayers with atomically flat surfaces are grown hetero-epitaxially on silicon (Si) (100) substrates by low-pressure chemical vapor deposition (LP-CVD)[1]. This leads us to the fabrication of 3C-SiC metal-oxide-semiconductor (MOS) devices. For the fabrication of MOS devices using 3C-SiC epilayers, it is important to realize the SiO_2/3C-SiC interface with fine electrical properties. In the present study, we have fabricated MOS structures, whose oxide layers were annealed in steam, using p and n-type 3C-SiC epilayers grown by LP-CVD to investigate the influence of annealing in steam after oxidation on the capacitance-voltage (CV) characteristics of the SiO_2/3C-SiC interface.

2. Experiments

The p-type 3C-SiC epilayers were grown on on-axis 3-in. Si (100) wafers by LP-CVD with a vertical reactor using a silane-propane-hydrogen (SiH_4-C_3H_8-H_2) reaction gas system. The growth pressure was 100 Torr. The gas flow rates of SiH_4, C_3H_8 and H_2 were 0.50 sccm, 0.52 sccm and 2.0 slm, respectively. Aluminum (Al) was doped during the growth for achieving the p-type conduction. The growth rate was approximately 1.2 μm/h. The n-type 3C-SiC epilayers were grown by LP-CVD with a horizontal reactor using a SiH_4-C_3H_8-H_2 reaction gas system in Electrotechnical Laboratory. The growth pressure was 10 Torr. The gas flow rates of SiH_4, C_3H_8 and H_2 were 0.80 sccm, 1.44 sccm and 8.0 slm, respectively. Details of the crystal growth have been reported elsewhere [1]. After the crystal growth, the p and n-type epilayers were cut into substrates of 10-mm x 10-mm in square. The substrates were boiled with acetone and sulfuric acid to degrease their surfaces, and then sacrifice oxidation was performed twice. Thereafter, pyrogenic oxidation was carried out at 1100°C for 1 hour to make gate oxide layers of about 40 nm in thickness. At the final stage of the oxidation, annealing in steam was performed at 800°C for 0.50, 2.0 and 8.0 hours. After these processes, gold was deposited on the oxide layers to form gate electrodes of 0.50 mm in

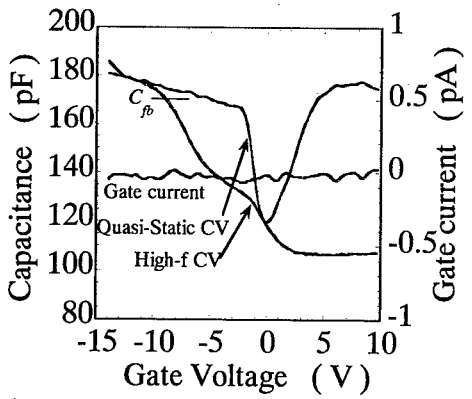

Fig.1 Simultaneous *CV* characteristics of the p-type MOS structure whose oxide layer is not annealed in steam.

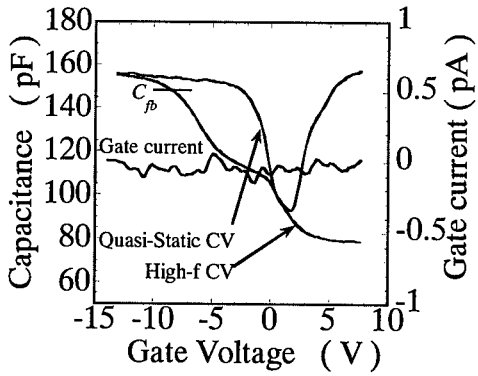

Fig.2 Simultaneous *CV* characteristics for the p-type MOS structure with the oxide layer annealed in steam for 2.0 hours.

diameter. For fabricating an ohmic electrode, the edges of oxide layers were removed with photolithography technique, and Ti/Al or Ni was evaporated on the bared surfaces of the p or n-type epilayers, respectively. The simultaneous *CV* characteristics were measured for the p and n-type 3C-SiC MOS structures to obtain the gate voltage corresponding to flat band condition (V_{fb}) and the energy profile of interface trap density (D_{it}). In the measurements, the MOS structures were illuminated with a low-pressure mercury lamp to induce an inversion layer before sweeping the gate voltage. After the inversion layer was formed, the gate voltage was swept under dark condition at room temperature to acquire *CV* curves.

3. Results

Figure 1 shows the simultaneous *CV* characteristics obtained for the p-type MOS structure whose oxide layer is not annealed in steam. There is a significant difference between the quasi-static and high frequency *CV* curves in the negative gate voltage side, which indicates that a large number of interface traps exist near the edge of the valence band. The value of V_{fb} is obtained to be -9.50 V. Figure 2 shows the simultaneous *CV* characteristics for the p-type MOS structure with the oxide layer annealed in steam for 2.0 hours. Whereas a difference in the two *CV* curves in the negative gate voltage side still exists, V_{fb} increases to –8.50 V by the annealing in steam. The MOS structures with the oxide layers annealed in steam for 0.5 and 8.0 hours are also measured. The value of V_{fb} for the MOS structure with the oxide layer annealed in steam for 0.5 hours is –14.8 V, and that for 2.0 hours is –8.00 V.

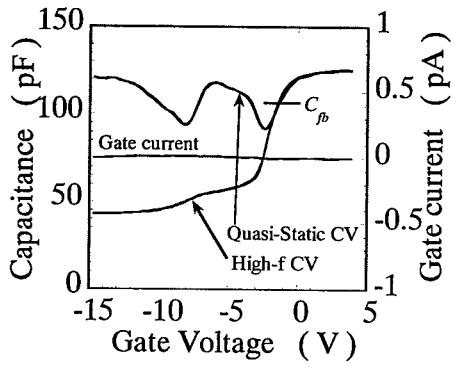

Fig.3 Simultaneous *CV* characteristics of the n-type MOS structure whose oxide laver is not annealed in steam.

Figure 3 shows the simultaneous *CV* characteristics obtained for the n-type MOS structure whose oxide layer is not annealed in steam. A peak is observed around -6 V on the quasi-static *CV* curve, and a ledge is found at –7 V on the high-frequency *CV* curve, which means that a large number of interface traps exist in the middle region of the band gap. The value of V_{fb} is obtained to be –1.30 V. Figure 4 shows the simultaneous *CV* characteristics for the n-type MOS structure with the oxide layer annealed in steam for 2.0 hours. Though the shapes of two *CV* curves do not change significantly by the annealing in steam, V_{fb} increases to +0.24 V. The MOS structures with the oxide layers annealed in steam for 0.5 and 8.0 hours are

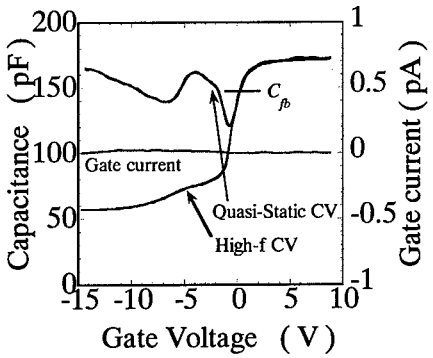

Fig.4 Simultaneous CV characteristics for the n-type MOS structure with gate oxide layer annealed in steam for 2.0 hours.

also measured. The value of V_{fb} for the MOS structure with the oxide layer annealed in steam for 0.5 hours is –1.60 V, and that for 8.0 hours is +0.41 V.

4. Discussion

Gate currents observed during the *CV* measurements (I_q) are shown in Figs.1 to 4. The gate current reflects the displacement of charges induced near the SiO_2/3C-SiC interface of MOS structures by a sweep of the gate voltage. Since I_q obtained does not have any peaks during the sweep of the gate voltage, the sweep speed is considered to be slow enough to neglect the displacement of charges near the interface, i.e., a quasi-static state is achieved in our simultaneous *CV* measurements. The energy profile of D_{it}, therefore, can be derived from the difference between the quasi-static and high frequency *CV* curves.

4.1 Interface trap density

The energy profiles of D_{it} extracted from the simultaneous *CV* curves of p-type MOS structures with oxide layers annealed in steam are shown in Fig.5. The energy profile of D_{it} for the MOS structure before the annealing in steam is also shown in the same figure. For the MOS structure before the annealing in steam, it is found that a large number of interface traps exist near the edges of the conduction and valence bands. Especially, a shoulder of the energy profile is seen around -0.6 eV from the mid-gap. The values of D_{it} are obtained to be (0.8 to 1.3) x10^{13} $eV^{-1}cm^{-2}$ in an energy range between -0.6 to -1.0 eV from the mid-gap. This shoulder is not observed for the *CV* curves of the n-type MOS structures, which is shown in Fig.6. In the p-type MOS structures, Al atoms, which are dopants of p-type epilayers, possibly pile up at the SiO_2/3C-SiC interface by the oxidation. Aluminum acceptors form an energy level of 0.15eV above the valence band edge (-0.95 eV from the mid-gap). Thus, it is likely that Al atoms at the interface have a role for the formation of the interface traps, which form the shoulder of the D_{it} profile at –0.6 eV. On the other hand, the values of D_{it} near the mid-gap are extremely low as compared with those near the both band edges. It is well known that a part of the interface traps in the middle region of the band gap do not have carrier exchange at room temperature. In order to obtain the net number of the interface traps in the middle region of the band gap more precisely, the high temperature *CV* measurements are required.

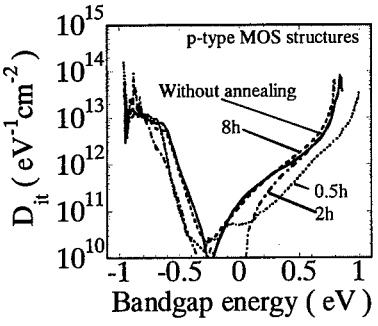

Fig.5 Energy Profiles of D_{it} extracted from simultaneous *CV* characteristics obtained from p-type MOS structures.

By the annealing in steam for 0.5 and 2.0 hours, the total amount of D_{it} is found to decrease. The annealing temperature of 800°C is so low that the significant oxide growth cannot occur at the interface by the annealing within 2.0 hours. It was reported that the annealing in steam at 950°C oxidizes residual carbon atoms near the SiO_2/6H-SiC interface [2]. Taking the fact into account, residual atoms such as carbon and/or Al probably are reduced by the annealing in steam within 2.0 hours. As for the energy profile of D_{it} for the MOS structure annealed in steam for 8.0 hours, no significant decrease is observed compared with that without annealing. This result suggests that the annealing in steam for a long period reproduces the interface traps and oxide-tapped charges in the oxide

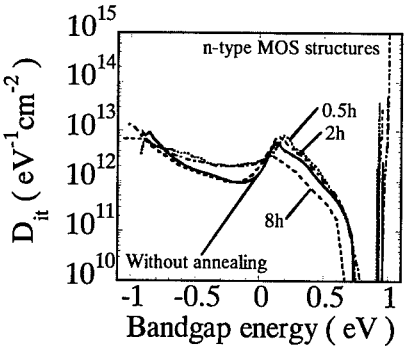

Fig.6 Energy Profiles of D_{it} extracted from simultaneous *CV* characteristics obtained from n-type MOS structures.

layers.

Figure 6 shows the energy profiles of D_{it} extracted from the simultaneous *CV* curves of the n-type MOS structures with oxide layers annealed in steam. Since the high-frequency *CV* curves have a capacitance ledge, the energy profiles of D_{it} in an energy range between –0.6 and +0.6 eV are considered to have an error. In order to get the correct energy profiles near the mid-gap, high temperature *CV* measurements are needed. As seen in Fig.6, no interface traps exist in an energy range between +0.7 and +0.9 eV from the mid-gap. Though the energy profile decreases slightly by the annealing in steam for 8.0 hours, no dramatic change is observed for 0.5 and 2.0 hours. It is considered that the annealing in steam at 800°C does not have any influence on the reduction in the number of interface traps in n-type MOS structures. The annealing in steam at low temperatures (so-called re-oxidation) was reported to reduce residual carbon atoms near the SiO_2/SiC interface [2]. The origin of interface traps in n-type MOS structures might differ from residual carbon atoms at the SiO_2/3C-SiC interface.

4.2 Shift of flat-band voltage

The values of V_{fb} obtained from the high frequency *CV* curves for the MOS structures with and without annealing in steam are summarized in Table.1. In the p-type MOS structures, the annealing in steam for 2 and 8 hours is found to have an increase of V_{fb}. As for the n-type MOS structures, V_{fb} increases with increasing the annealing time. These imply that negative trapped charges increase, or that positive trapped charges decrease near the interface by the annealing in steam. Further investigations are needed to clarify the generation mechanisms of trapped charges in oxide layers near the interface.

Table.1 Flat-band voltages obtained for MOS structures with oxide layers annealed in steam

Annealing time (h)	0(without annealing)	0.5	2.0	8.0
p-type MOS structures: V_{fb} shift (V)	-9.50	-14.8	-8.50	-8.00
n-type MOS structures: V_{fb} shift (V)	-1.30	-1.60	+0.24	+0.41

5. Conclusions

Annealing in steam has been carried out at 800°C up to 8 hours for the oxide layers of MOS structures formed on p and n-type 3C-SiC epilayers. The annealing in steam for 2 hours has reduced the interface traps in the p-type 3C-SiC MOS structures. No significant influence of the annealing in steam is observed on the interface traps in the n-type 3C-SiC MOS structures. The energy profiles of D_{it} obtained for the p-type MOS structures are quite different from those for the n-type ones, which suggests strongly that the origin of interface traps is different between the p and n-type MOS structures.

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Atomic-Scale Engineering of the SiC-SiO_2 Interface

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Keywords: Interface Structure, Interface Trap, Nitrogen, Oxidation

Abstract: We report results from three distinct but related thrusts that aim to elucidate the atomic-scale structure and properties of the SiC-SiO_2 interface. a) First-principles theoretical calculations probe the global bonding arrangements and the local processes during oxidation; b) Z-contrast atomic-resolution transmission electron microscopy and electron-energy-loss spectroscopy provide images and interface spectra, and c) nuclear techniques and electrical measurements are used to profile N at the interface and determine interface trap densities.

Introduction: The native oxide of SiC is SiO_2, but the properties of the SiC-SiO_2 interface fall far short of those of the Si-SiO_2 interface for MOSFET applications. We have initiated a program to investigate the atomic-scale properties of the SiC-SiO_2 interface aiming to identify the causes and possible remedies for the observed behavior. We employ a combination of first-principles calculations, atomic-resolution microscopy, electron-energy-loss spectroscopy, and analytical and electrical measurements as functions of process variation. In this paper we report initial results of these investigations.

Theory: We have pursued first principles calculations (density functional theory, local density approximation for exchange-correlation, pseudopotentials, plane waves) with several objectives.

a) Global bonding arrangements at the interface: Systematic studies of the Si-SiO_2 interface for (001) Si revealed that a totally abrupt interface is possible and energetically preferred. Suboxide bonds (i.e. Si-Si bonds on the oxide side are energetically unfavorable because insertion of an O atom in such a bond generally allows more relaxation to occur via a pivoting action about the O site). In contrast, for SiC-SiO_2, an abrupt interface is not possible for topological reasons. Even in the case of cubic SiC and its (001) surface, the bond lengths are too small to accommodate an abrupt interface. The hexagonal phase is even worse because the surfaces resemble the Si (111) surface [known to have a much rougher interface than (001) surfaces] and the bond lengths are again not suitable. In fact, there is an experimental study [1] that found that depositing a monolayer of O on SiC saturates the bonds in a way that does not allow for the growth of an oxide. Our modeling studies confirm this result and further establish that a substantial interface layer with mixed bonding including Si-Si bonds is absolutely necessary. This result is fully consistent with the EELS data reported below.

b) Atomic-scale processes during oxidation and interface defects: We performed calculations investigating the atomic-scale steps that lead to precipitation of O atoms in the form of SiO_2 particles in SiC [2]. These studies allowed us to deduce several important results about the oxidation of SiC:

i) whereas during Si oxidation, Si interstitials are emitted, during SiC oxidation the emission of either Si or C interstitials is energetically unfavorable. On the other hand, C atoms are removed by being captured by O atoms into CO molecules. The latter are not stable in SiC but are stable and mobile in SiO_2. Thus we have identified the atomic-scale processes that lead to the removal of C in the form of CO, as observed experimentally. We further find that the activation energy for diffusion of CO in SiO_2 is much smaller than that for the diffusion of O_2 in SiO_2 (0.5 eV versus 1.5 eV) so that the rate-limiting step for oxidation is the supply of O or the interface reaction. Similarly, during reoxidation, the rate-limiting step for the possible removal of C precipitates at the interface is again the supply of O. Our calculations further reveal that the oxidation process does not leave dangling bonds. The only likely interface defects are centers involving threefold-coordinated O that are reminiscent of the "thermal donors" in Si [3] and C interstitials from the break-up of departing CO molecules. Both these defects introduce localized energy levels in the upper part of the SiC band gap. We also expect Si-Si bonds at the interface to introduce localized states at both ends of the SiC band gap. Thus, there are several candidates for the observed large densities of interface defects, especially at the edges of the band gap in 4H material.

Microscopy:

Sample preparation: We report investigations of two samples, both oxidized thermally at 1100 °C and one reoxidized at 900 °C. Prior to preparing them for the TEM, the samples were coated with a layer of amorphous silicon (a-Si in Fig. 1 a) for protection. The reoxidized sample showed im-

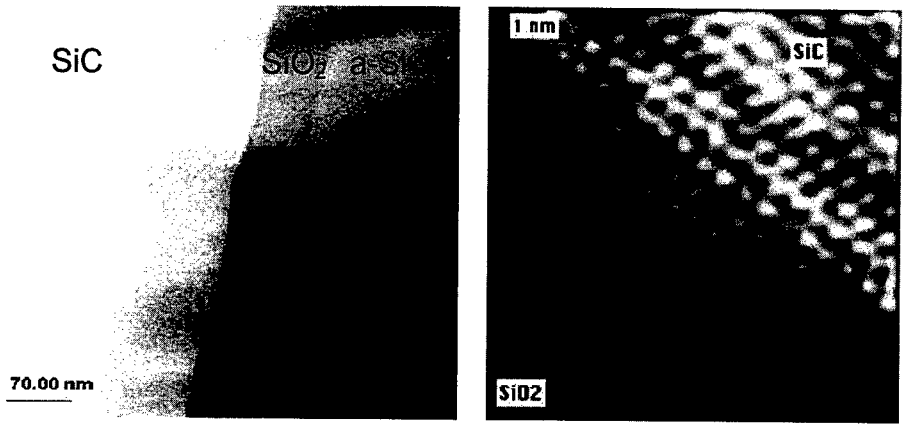

Fig. 1. Z-contrast images of the SiC-SiO_2 interface with a) low and b) atomic resolution. In the reoxidized sample (a) we see a faceting not observed in normally oxidized samples (b). On the atomic scale, both samples reveal a roughness of about one monolayer.

proved electrical properties after the additional heat treatment (see below for details).

Z-contrast images obtained from the reoxidized sample revealed a strong faceting (Fig. 1a). We attribute this faceting to an accumulation of steps originating in the miscut of the SiC-4H substrate. The faceting is not periodic; large plane areas (mostly, but not only, of the (0001) plane) are alternating with areas as shown in Fig. 1a where many facets accumulate. An atomic column resolution investigation of both samples showed a roughness of only about one monolayer.

We also performed electron energy-loss spectroscopy (EELS) on the same samples. The spectra were obtained while the beam (diameter of about 0.3 nm) was scanned along a line across the inter-

face. In Fig. 2 we compare the results of a reoxidized SiC-SiO_2 interface with corresponding data from a (111) Si-SiO_2 interface. In the case of the Si-SiO_2 interface spectrum, the slowly rising onset is attributed to a suboxide layer (SiO_x), namely one or two layers of mixed Si-Si and Si-O-Si bonds. In contrast, for the SiC-SiO_2 interface, a mixed spectrum persists over an interface layer of order 3 nm, suggesting an extended amorphous region whose stoichiometry remains unclear. This result is consistent with the theoretical studies described above. It is notable that, despite the extended mixed phase, the crystalline-amorphous interface has minimal roughness, one to two monolayers, as revealed by the micrograph in Fig. 1b.

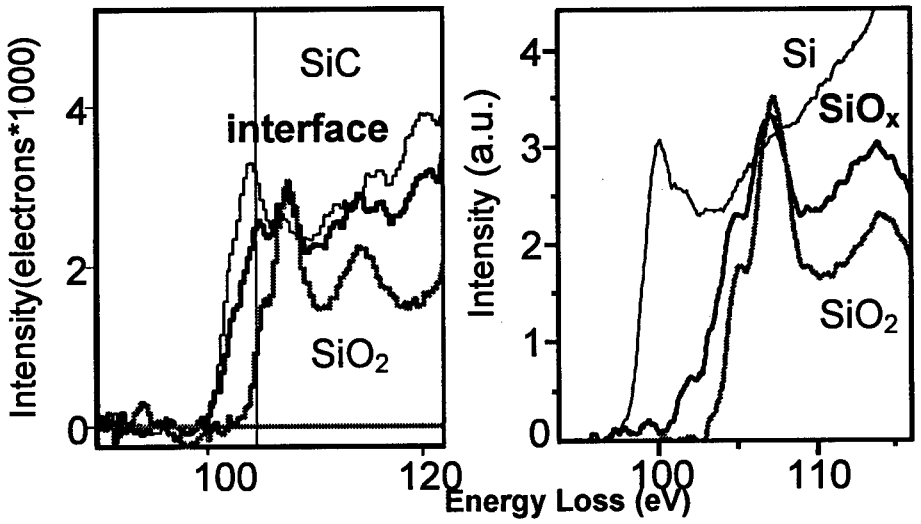

Fig. 2. EELS spectra of Si-$L_{2,3}$ edges from the SiC-SiO_2 interface and the Si-SiO_2 interface. In each case we show the two bulk spectra plus a typical interface spectrum.

Analytical and electrical measurements: Recent experimental work found that incorporation of N in SiC-SiO_2 structures may have a beneficial effect on the interface trap density [4]. We have studied the incorporation of N for oxides grown in (i) N_2O (1100 °C) and (ii) O_2 (1100 °C), subsequently annealed in $^{15}N^{18}O$ (1000 °C). The N_2O grown sample reveals an exceedingly slow growth rate (compared to pure O_2) and a non-stoichiometric oxide. As a result we have concluded that growth in N_2O is not a useful way of incorporating nitrogen into the SiC/SiO_2 structure.

The annealed samples were investigated using isotope-sensitive nuclear techniques to determine the N content and profile. As shown in Fig 1. there is a clear indication of interfacial N, corresponding to ~10^{14} N/cm^2. These values are considerably smaller than the corresponding N accumulation for the Si-SiO_2 system. This is consistent with the fact that the SiC interface is less reactive than the Si interface. Complementary measurements (not shown) of the ^{18}O exchange reaction (from the $^{15}N^{18}O$ annealing gas) with the oxides shows exactly the same reaction rate for both the Si and SiC structure. This is another sensitive demonstration of the fact that the bulk oxides of these two materials are chemically and physically similar, though the interfaces are distinctly different.

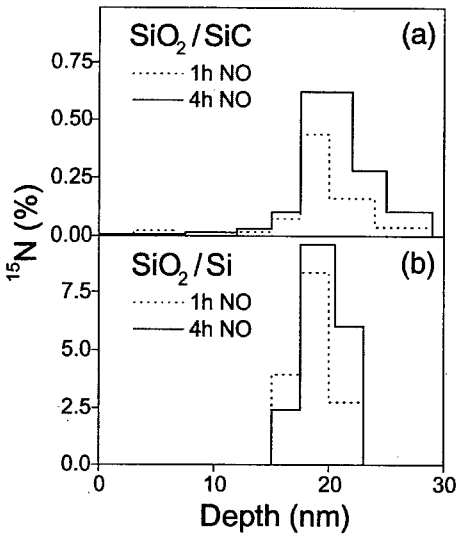

Fig. 3. Concentration profiles of ^{15}N after annealing in 10 mbar of $^{15}N^{18}O$ at 1000 °C for 1 h (dotted) and 4 h (solid). The origin corresponds to the surface, the SiC-SiO_2 interface is at ~30 nm, and the Si-SiO_2 interface is at ~20 nm.

relation of D_{it} with doping suggests that information about states in the upper part of the band gap obtained from n-type material may not be applicable to p-type material. Reoxidation was found to reduce D_{it} in p-type but not in n-type material.

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Electrical measurements have been performed on a series of samples to evaluate the effect of N incorporation both with and without reoxidation. As is well known [5], reoxidation reduces the density of interface traps (D_{it}). We have found that nitridation does not have any effect on D_{it}, with or without reoxidation. Though further reduction of D_{it} would have been desirable, the result that N can be incorporated without an increase in D_{it} is important because N is known to enhance reliability [6].

Finally we report briefly on samples grown epitaxially and oxidized in a furnace. Different ratios of propane to silane were used and the resulting D_{it} in the upper part of the band gap for 6H-SiC is shown in Fig. 4. When the Si/C ratio is small, doping by the ambient N is suppressed and the material is essentially intrinsic. Thus, the observed improvement in Dit may in fact be due to the lower doping. This cor-

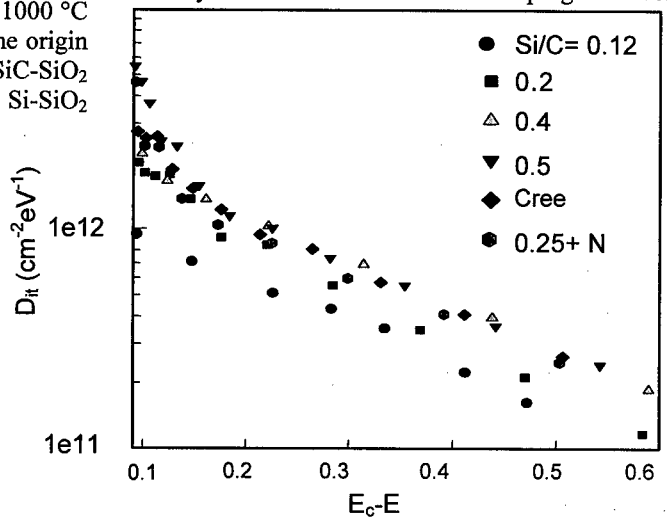

Fig. 4. Interface State Density vs Si/C Ratio for 6H-SiC

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Materials Science Forum Vols. 338-342 (2000) pp. 1137-1140

Comparison of High-Temperature Electrical Characterizations of Pulsed-Laser Deposited AlN on 6H- and 4H-SiC from 25 to 450°C

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Keywords: Aluminium Nitride, Gate Dielectrics, Leakage Mechanism, Passivation Films, Pulsed Laser Deposition, Schottky Emission

Abstract The high-temperature dielectric properties of thin-film aluminum nitride (AlN) that was pulsed-laser deposited (PLD) on heavily doped *n*-type 6H and 4H-SiC substrates are investigated from 25 to 450 °C. Identical, very low leakage current densities ($< 1 \times 10^{-2}$ A/cm^2 at 450 °C for a 2-MV/cm electric field) are reported for both polytypes. The primary high-temperature leakage mechanism appears to be Schottky emission with zero-field barrier heights for 6H and 4H of 1.68 and 1.55 eV, respectively.

Robust high-temperature passivation and gate dielectric materials are required for analog power control devices and embedded digital fault protection circuitry to implement future military and commercial electric-drive applications. These future applications will require dielectric materials that are stable at temperatures up to 350 °C under operating fields of at least 1 MV/cm. Thermally grown and deposited-reoxidized SiO_2 dielectrics are under development, but have not yet been demonstrated to provide stable and reliable MOSFET operation even at a temperature of 300 °C and with a gate field of 1 MV/cm. Therefore, other insulators, especially those with high dielectric constants (resulting in a lower field in the insulator), including aluminum nitride (AlN), are being investigated for high-temperature device applications [1-3].

In this work, the high-temperature bulk dielectric properties of high-quality thin-film AlN that was pulsed-laser deposited (PLD) [4] on heavily doped *n*-type SiC substrates of both 6H and 4H polytypes are investigated from 25 to 450 °C. Previously, we presented a similar study on just the 6H polytype [5]. The capacitors used in this study were fabricated by pulsed-laser depositing 500-nm-thick films of AlN on the highly doped (1×10^{18} cm^{-3}) *n*-type SiC substrates. The SiC substrates were purchased from Cree Research, Inc., as research-grade wafers with the standard polarity (Si face) and orientation (3.5° off-axis for 6H and 8° for 4H). A 200-nm-thick TiN film was pulsed-laser deposited in situ to form the top gate electrodes. A PLD TiN film of similar thickness was grown to form the backside ohmic contact to the SiC substrate.

The band gap of the PLD AlN was determined to be 6.2 eV from optical transmission measurements. X-ray diffraction and Rutherford backscattering analyses showed the AlN film to be well aligned with the lattice planes of the SiC and to have a high degree of crystallinity. The TiN films that were grown on the AlN and on the SiC substrate were also shown to be epitaxial, and the TiN backside layer formed a good ohmic contact to the SiC with a specific resistivity of ~10^{-5} Ω-cm^2. The TiN gate electrodes were patterned using an ion mill that provided six columns with about ten gates each on both the 7 × 6 mm 6H-SiC and the 11 × 5 mm 4H-SiC wafer sections. Each gate measured 200 μm × 200 μm, for an area of 4×10^{-4} cm^2.

Current-voltage (*I-V*), as well as capacitance and conductance, measurements were made as a function of temperature. Because of the high doping level in the SiC, we did not observe any depletion. The capacitances at 25 °C were 5.4 and 5.2 pF for the 6H and 4H samples, respectively, with a maximum variation of ten percent over all the gates, and the capacitor conductances were 0.4 and 0.3 μS, respectively. The capacitances increased by 0.4 pF at 450 °C and decreased to around 5.0 pF upon cooling to 25 °C. *I-V* measurements were made over the voltage range from –20 to +100 V (the maximum voltage for the instrument) which correlate to gate fields of –0.4 to 2 MV/cm for a dielectric thickness of 500 nm. The raw *I-V* data for both samples is shown in Figure 1. The

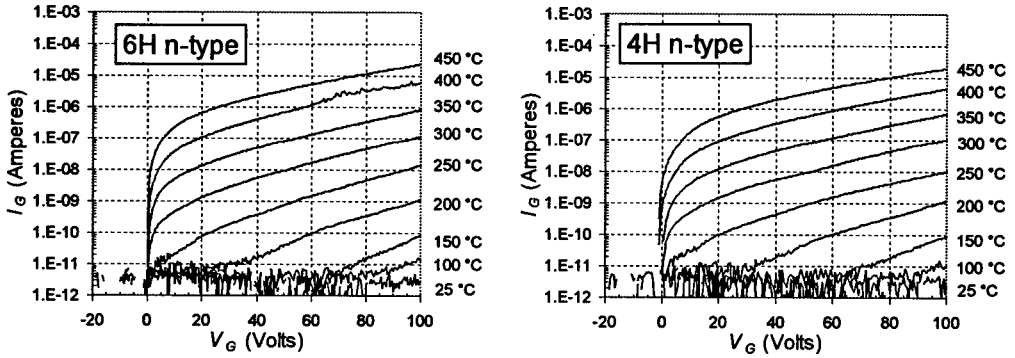

Figure 1. Comparison of current-voltage characteristics for a 6H and 4H PLD AlN capacitor over the temperature range of 25 to 450 °C.

current is seen to monotonically increase with increasing temperature. For temperatures below 250 °C, the measured current for both samples is in the noise at smaller applied biases but comes up with increasing voltage. Current densities for electric fields $\mathcal{E}_i$ of 1 and 2 MV/cm are plotted as a function of $1/T$ for both 6H and 4H samples in Figure 2. In both samples the curves at the two

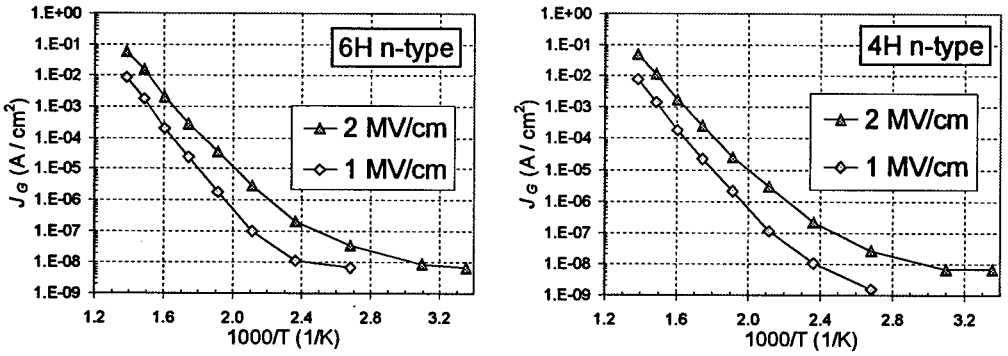

Figure 2. Comparison of 6H and 4H PLD AlN capacitor leakage current density as a function of temperature from 25 to 450 °C (298 to 723 K) for several gate fields.

fields have similar shapes that suggest either Frenkel-Poole or Schottky emission is the rate-limiting leakage mechanism for temperatures above 200 °C (473 K) and that tunneling emission is probably the dominant conduction process for temperatures below 200 °C [5]. The average leakage currents at room temperature are about 1×10^{-8} A/cm^2. The maximum leakage current densities at 450 °C (723 K) for electric fields of 1 and 2 MV/cm are only 8×10^{-3} and 5×10^{-2} A/cm^2, respectively (we previously reported slightly lower current densities on similar 6H samples, 1×10^{-3} and 7×10^{-3} A/cm^2, respectively [5]). These leakage currents are orders of magnitude lower than values that

have been previously reported for thin films of AlN, even though the earlier studies reported *I-V* characteristics at significantly lower temperatures and fields [1-3].

Figure 3 shows a comparison of these current densities. The 6H and 4H PLD AlN values for the 2-MV/cm case, replotted from Figure 2, fall on top of each other. The previously reported 6H PLD AlN results [5] appear in the adjacent curve just below. Tin et al [3] and Zetterling et al [1] both report values only at room temperature for MOCVD AlN. The value of Tin et al is much lower than that of Zetterling et al, probably because the applied field is so much lower: 0.4 versus 2.3 MV/cm. Ouisse et al [2] put AlN down on Si via molecular beam epitaxy (MBE) and although they report current densities up to 300 °C, they only applied 0.3 MV/cm. As a further comparison, results for thermal SiO_2 on p-type 6H-SiC at 2 MV/cm are shown at the bottom of Figure 3 [8].

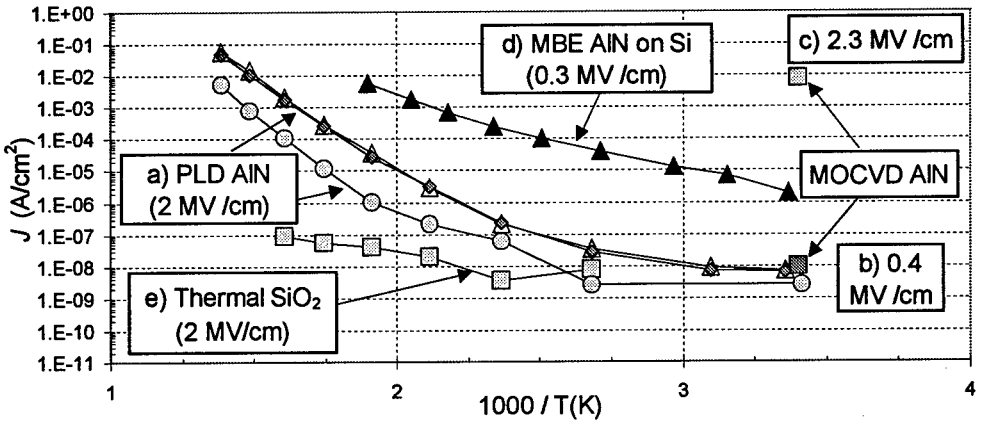

Figure 3. Comparison of dielectric leakage current densities taken from the literature with our recent results. a) PLD AlN on 6H and 4H SiC: upper curves from this work are identical for 6H and 4H, the lower curve is previously reported work on 6H [5]. MOCVD AlN on SiC: b) after Tin et al [3], c) after Zetterling et al [1]. d) MBE AlN on Si, after Ouisse et al [2]. e) Data for thermal SiO_2 on 6H p-type SiC [8].

Figure 4 shows Arrhenius plots for both 6H and 4H samples that were generated using the *I-V* characteristics from Figure 1 for $\mathcal{E}_i$ of 0.25 to 2 MV/cm. The log of the current is plotted versus $1/T$ from 250 to 450 °C (523 to 723 K). The plots are quite linear over this temperature range for all the different fields for both samples. The activation energies, E_a, extracted from the slopes of these lines, are then plotted in Figure 5 as a function of the square root of the PLD AlN electric field $\mathcal{E}_i^{1/2}$. The plots show a very nice linear relationship for both samples, and give extrapolated zero-field E_a values of 1.68 and 1.55 eV for the 6H and 4H samples, respectively. These results are in good agreement with values of the SiC-to-AlN band offsets that have been reported in the literature [6,7]. We conclude from this that Schottky emission at the SiC/AlN interface appears to be the dominant high-temperature leakage mechanism in PLD AlN, at least for fields up to 2 MV/cm. What is especially encouraging is the 0.13-eV difference between the two polytypes. Since the bandgap of 4H is about 0.2 eV greater than 6H, we would expect about 0.1 eV smaller offset in the 4H case. This is indeed what we find!

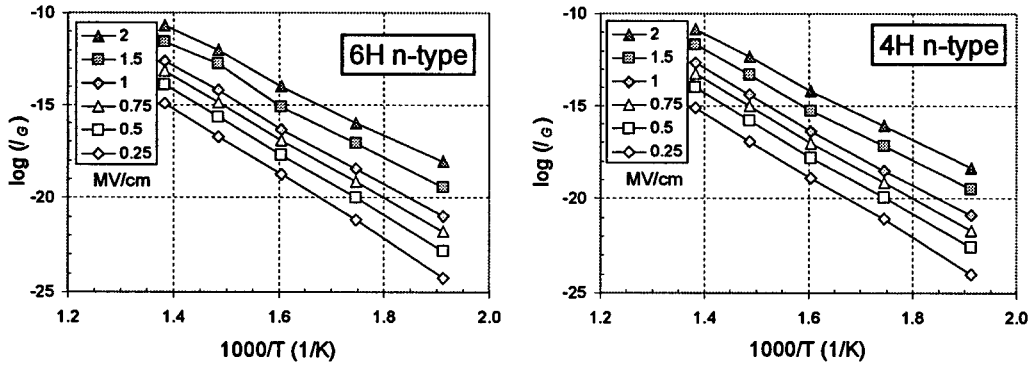

Figure 4. Arrhenius plots for both 6H and 4H PLD AlN capacitor leakage for gate fields of 0.25 to 2 MV/cm.

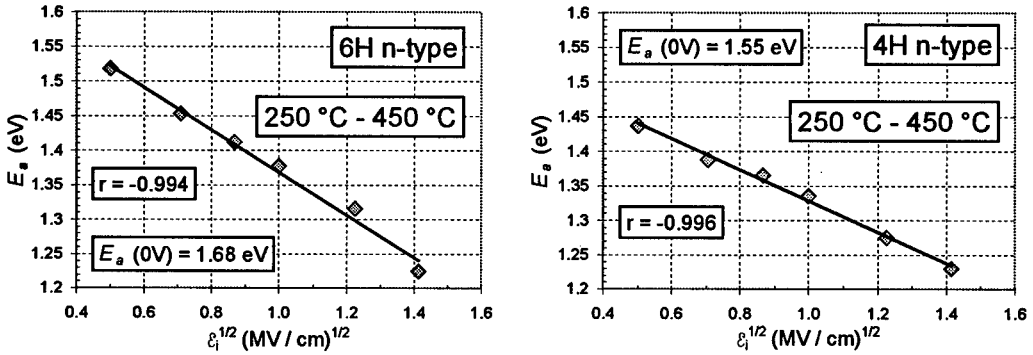

Figure 5. Comparison of plots of activation energy, E_a, as a function of gate field for both 6H and 4H PLD AlN capacitors, which give extracted zero-field E_a values of 1.68 and 1.55 eV, respectively.

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Materials Science Forum Vols. 338-342 (2000) pp. 1141-1144

Molding-based Thin Film Patterning Techniques for SiC Surface Micromachining

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Keywords: MEMS, Micromolding, Polycrystalline SiC, Surface Micromachining

Abstract

Molding-based thin film patterning techniques for polycrystalline SiC using molds made of SiO_2 and polysilicon are presented. The molds are fabricated using conventional SiO_2 and polysilicon deposition and patterning techniques, and are filled with polycrystalline SiC deposited by APCVD. Mechanical polishing is used to expose the molds and planarize the substrate, and wet chemical etchants are used to dissolve the molds. The molding process circumvents the selectivity problems associated with SiC reactive ion etching, and therefore is well-suited for SiC surface micromachining. Examples of surface micromachined devices patterned using micromolding are presented.

Introduction

Compatibility with silicon micromachining in conjunction with outstanding mechanical, electrical, and chemical properties, makes SiC the leading semiconductor for high temperature microelectromechanical systems (MEMS). For device fabrication, reactive ion etching (RIE) is commonly used to pattern SiC films. Unfortunately, SiC etch rates are low relative to Si, and etch selectivities to Si and SiO_2 are poor, making RIE-based device fabrication challenging, especially for surface micromachining processes that use microns-thick SiC structural layers in conjunction with SiO_2 and polysilicon sacrificial layers. In spite of these problems, RIE-based SiC surface micromachining processes have been developed [1,2], and a plasma-based dry etching process with selectivity SiC:SiO_2 of 5:1 has been reported [3], but thus far these processes have not been used to fabricate multilayer devices.

Fabrication

In order to circumvent the problems associated with SiC RIE, we have developed molding-based techniques to pattern SiC films. These techniques, hereafter called micromolding, use patterned polysilicon and SiO_2 films as molds to pattern SiC films. The basic molding process is shown schematically in Fig. 1. The basic process uses patterned SiO_2 films as molds, and Si_3N_4-coated, 100 mm-diameter Si wafers as substrates. Following the deposition of the Si_3N_4 layer by LPCVD, a polysilicon film is deposited on the nitride layer. An LPCVD process involving the decomposition of silane at a pressure of 300 mTorr and a temperature of 615°C is used. The SiO_2 molding layer is then formed by the complete thermal oxidation of the polysilicon film at 1075°C. The molds are then created using conventional photolithography and SiO_2 wet etching.

In this manner, reasonably-thick and thermally-rugged SiO_2 molds can be fabricated on the Si_3N_4 substrate layers.

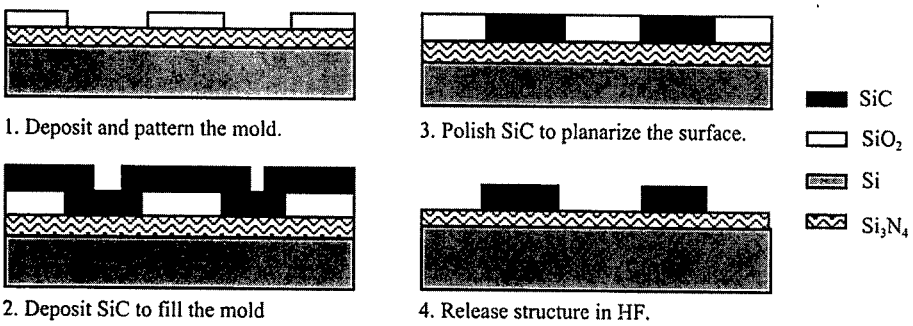

Figure 1. Cross-sectional schematic of the basic micromolding process.

Following mold definition and delineation, the wafer is ready for SiC deposition. Polycrystalline SiC (poly-SiC) films are deposited in a two-step, APCVD process. The deposition process begins with an *in-situ* cleaning of the substrate surface performed in hydrogen at a flow rate of 25 slm for 5 min and at a susceptor temperature of 1000°C. After the *in-situ* cleaning, film growth is initiated by raising the susceptor temperature to 1050°C, and introducing silane and propane into the hydrogen carrier gas flow at rates of 102 sccm and 46 sccm, respectively. For doped SiC films, phosphine is included in the gas mixture at a flow rate of 180 sccm. Using this recipe, poly-SiC films are deposited at a rate of about 1 μm/hr. In order to improve SiC deposition uniformity, wafers were rotated 180 degrees at the midpoint of each deposition run. For a 2.5 μm-thick film, the wafer rotation results in a 2000 Å thickness difference between the top and bottom of each wafer, as compared with a 7000 Å thickness difference without a rotation. The residual stress in the as-deposited poly-SiC films, as determined using the laser-scan wafer curvature technique, is tensile with a magnitude of about 125 MPa for 2.5 μm-thick films.

During film growth, SiC is deposited into and on top of the mold. Mechanical polishing is used to remove the poly-SiC from the top of the oxide mold and to planarize the surface. Two different polishing slurries were investigated for removal rate, selectivity, and uniformity during the development of this process. For relatively rapid removal, a 3 μm-diameter diamond suspension, a normal force of 360 N, polishing pad rotation speed of 150 rpm, and a suspension flow rate less than 10 ml/min is used. The removal rates of planar SiC and SiO_2 films are about 1100 Å/min and 680 Å/min, respectively. For a SiC-based polishing slurry (30 g 3 μm SiC powder in 2000 ml D.I. water) with a flow rate of 200 ml/min, the removal rates of planar SiC and oxide films are about 350 Å/min and 1600 Å/min, respectively. The SiC-to-SiO_2 polishing selectivity using the 3 μm-diameter diamond suspension is 1.6:1, which is surprisingly much higher than the selectivity using the SiC slurry (1:5). The polishing data are summarized in Table 1. Because of the higher selectivity, sharp and clear features resulting from uniform polishing using diamond suspension are produced. Moreover, for the diamond slurry, about 95% of a wafer can be polished without damaging the patterned structures. The SiC slurry, however, results in nonuniform polishing across the wafer, and the complete removal of small SiC features, thus exposing the underlying Si_3N_4 layer. On account of the high removal rate and good

polishing selectivity, the 3 μm-diameter diamond suspension is the preferred polishing material for patterning SiC films using SiO_2 molds. An example of a patterned structure is shown in Fig. 2(a).

Table 1. Polishing selectivity data for the micromolding process.

Polishing Material	Polishing Rate for SiC (Å/min)	Polishing Rate for SiO_2 (Å/min)	Polishing Selectivity of SiC:SiO_2
Diamond Suspension	1100	680	1.6:1
SiC Slurry	350	1600	1:5

In addition to removal rate and selectivity, issues related to stress-induced wafer curvature and SiC film thickness variations make the polishing process challenging. Tensile stresses in the SiC films cause the Si wafers to have a concave shape, which results in more rapid removal of SiC from the edges of a wafer relative to the center. To solve this problem, a thin polymer spacer placed between wafer and wafer carrier was used to reduce the concavity, thus increasing the planarity of the wafer. Also, the spacer reduces the polishing rate in regions where the SiC film is thinnest, thus further increasing the polishing uniformity. About 90% of wafer area can be successfully polished when a spacer is used. After polishing, the SiO_2 mold is simply removed by etching in HF, creating the patterned SiC structure. An optical photograph of a released lateral resonator is shown in Fig. 2(b).

(a) (b)

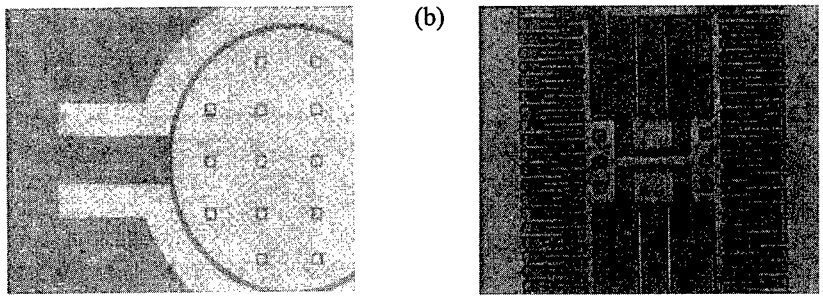

Figure 2: Optical photographs: (a) a patterned SiC pressure sensor, and (b) a released lateral resonantor.

The basic micromolding process has been extended to single-layer and multilayer surface micromachining processes [4,5]. The single-layer surface micromachining process is shown schematically in Fig. 3. The process begins with the growth of a sacrificial SiO_2 layer on a Si wafer. A polysilicon layer is then deposited by LPCVD and patterned to form the mold. Poly-SiC is then deposited by APCVD into and onto the mold. Diamond-based mechanical polishing is then used to planarize the surface and remove the poly-SiC from the top surface of the polysilicon mold. KOH is used to dissolve the polysilicon mold. The patterned SiC structure is then released by dissolving select regions of the sacrificial SiO_2 layer in HF. A SEM micrograph of a surface micromachined lateral resonant structure fabricated in this manner is shown in Fig. 4. By relying on well-characterized polysilicon etch techniques to form the patterns, etch rate and selectivity issues associated with SiC RIE are completely bypassed. The molding process has been extended to fabricate multilevel SiC micromotors by using both SiO_2 and polysilicon molds in alternating fashion. Details concerning the fabrication steps and testing results can be found in [5].

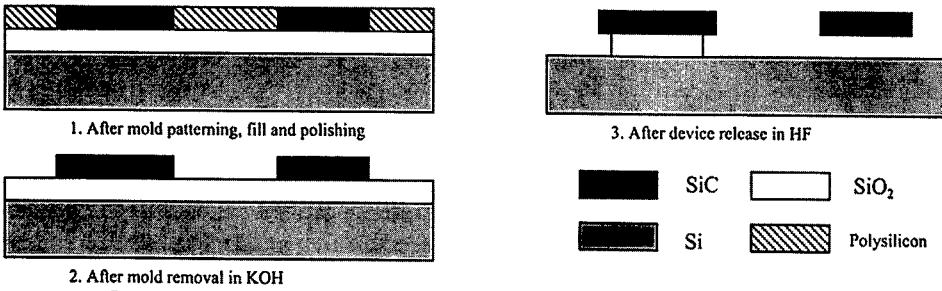

Figure 3. Cross-sectional schematic of a molding-based surface micromachining process for SiC.

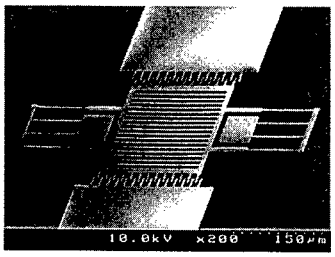

Figure 4. Plan-view SEM of a micromolded SiC lateral resonant structure [4].

Conclusions

Molding techniques for the patterning of Poly-SiC films have been developed. The molding techniques circumvent the problems associated with RIE-based patterning processes, namely selectivity to SiO_2 and polysilicon. The molding process does not bypass the selectivity issue altogether, because mechanical polishing is used to remove SiC from unwanted areas. It was found that diamond-based polishing slurries outperform SiC-based slurries in terms of polishing uniformity, selectivity, and removal rate. Issues pertaining to stress-induced wafer curvature were overcome by the insertion of a thin polymer spacer between the wafer and wafer chuck. The basic molding technique has been extended to single and multilayer surface micromachining processes.

Acknowledgements

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Bulk Micromachining of Polycrystalline SiC Using Si Molds Fabricated by Deep Reactive Ion Etching

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Keywords: DRIE, Micromolding, SiC MEMS, SiC Micromachining

Abstract A method has been developed to fabricate complex, three-dimensional structures out of polycrystalline SiC. Deep Reactive Ion Etching (DRIE) in conjunction with a novel patterning method has been used to make high precision molds from which SiC atomizers were fabricated. A thin film 3C-SiC interface layer between the Si and the thick SiC deposited into the molds was used to ensure a smooth device surface morphology.

Introduction

Bulk micromachining is an integral process technology for the fabrication of Si-based micro-electromechanical systems (MEMS). As SiC replaces Si in the transition to high-temperature MEMS, however, novel etch techniques must be found to maintain device design flexibility. The chemical stability that makes SiC an attractive material for harsh environment sensors renders it impervious to most wet (KOH, EDP) and dry etch chemistries that are the mainstay of Si bulk micromachining. Some success in using photoelectrochemical etching (PEC) for bulk micromachining of SiC has been achieved **[1]**, with etch rates on the order of 2000 A/min. A variety of dry etches have also been examined for SiC **[2]**, with reported etch rates of up to 4500 A/min. However, dry etches tend to exhibit poor mask selectivity, and neither PEC nor dry etching have been practical to date for fabricating complex 3D MEMS structures from SiC.

A novel processing approach is discussed in this paper that provides an alternative to the direct bulk etching of SiC. The approach uses Si molds fabricated by deep reactive ion etching (DRIE) in conjunction with a patented patterning method that allows for the formation of complex, SiC MEMS structures. It should be noted that molding has been used to make macro sized SiC parts using graphite as the sacrificial mold material **[3]**. However, processes like DRIE have yet to be developed for graphite substrates.

DRIE etching has been used to make thick (100+μm) Si structures with a high degree of dimensional precision. The fabrication of molds using the same technology allows for the translation of this precision in the fabrication of thick SiC structures. A SiC atomizer with inlet channels, swirl chamber, outer annulus and exit orifice has been fabricated using this technique.

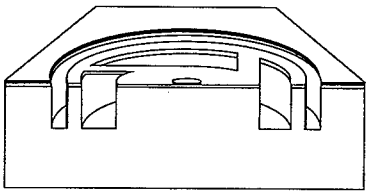
Fabrication

The SiC atomizers fabricated in this work have a thickness of 400 μm with a total diameter of 4318 μm. The Si molds used to make these devices were fabricated from a 500 μm-thick

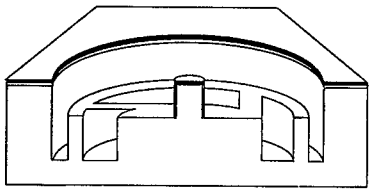
(100) Si substrate using DRIE. The substrate thickness was chosen to allow for an etch depth of 400 μm, equal to the thickness of the final device, without etching through the wafer. The process flow beginning at the first etch, after the first and second etch masks have been patterned, is shown in Fig.1. The novelty of the process lies in the patterning of both the first and second etch step masks before any DRIE etching. This feature overcomes the problem of patterning a substrate for a second etch after the first bulk etch is completed. Conventional photolithography on deep etched substrates is impractical because surface nonplanarities prevent an even coating of the photoresist from being applied to the etched substrate.

The two etch mask materials used to fabricate the mold were thermal oxide and thick photoresist (Shipley AZ 4620). The process begins with a 1 μm growth of silicon dioxide on the substrate. The oxide was patterned for the first etch using a standard photolithographic process. This pattern defined the etch mask for the deepest parts of the mold. The deepest parts of the mold, when filled, form the outer and inner walls of the annulus, as well as the walls of the swirl chamber. The next step required the patterning of the thick photoresist on top of the patterned oxide layer. Notice from the process flow that the resist necessarily exposes more of the underlying substrate than the oxide. This allowed the exposed surfaces during the first etch to continue being etched during the second etch step.

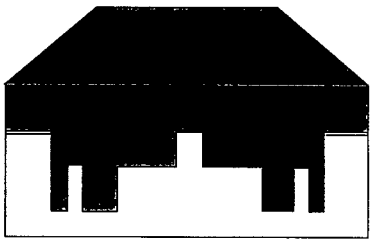
The first etch was then performed to a depth of 275 μm, defining the depth of the annulus, inlet slots, and swirl chamber. After the first etch was completed, the oxide layer was removed using buffered HF, exposing the areas for the second etch defined by the thick photoresist. The second etch was then performed to remove an additional 125 μm of Si, resulting in a maximum mold depth of 400 μm, and a minimum mold depth of 125 μm, with the unetched center post providing the molding for the exit orifice through-hole. The final step for the mold preparation



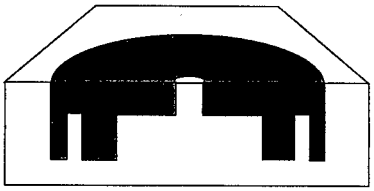
Step1 : First 275 μm deep DRIE etch



Step 2: Removal of oxide mask and second 125 μm DRIE etch



Step 3: Deposit 400μm of SiC



Step 4 : Polish excess SiC and release

Fig. 1: Process flow for SiC atomizer fabrication.

was the removal of the resist using piranha. Using the methodology described above and additional processing steps like Si fusion bonding, more complex molds can also be made.

While the molds were batch fabricated on 4-inch Si substrates, they had to be prepared into 7 x 7 mm^2 dies for the SiC deposition step. This was due to the thermal mismatch effects between SiC and Si which causes excessive warpage and fracturing of large area substrates for thick SiC depositions. The polycrystalline SiC mold filler was deposited in a high-rate atmospheric pressure (AP) CVD reactor to a thickness of 400 μm using methyltrichlorosilane (MTS) at a substrate temperature of 1200°C. A multi-step deposition process was used with the rates varying from 25-50 μm/hr. As the deposition occurred both in the mold and on the field areas, mechanical polishing was required to remove the excess SiC. This was achieved using a two step process. The first step was a non-optimized lapping phase for the rapid removal of SiC using a 15 μm polycrystalline diamond to slow the removal of the SiC, as well as to reduce its surface roughness. Once the SiC was completely removed from the field area, the device was released by dissolving the mold using a KOH solution at 55°C. It should be noted that the mold filler can be any material that can sustain high deposition rates on a Si substrate and withstand the release etchant, and nickel atomizers have also been made using the molding process.

Results and Discussion

An SEM micrograph of the SiC device is shown in Fig. 2. Examination of the SiC atomizer surfaces reveals SiC protrusions from the exit orifice and at various locations in the swirl chamber. These outgrowths are generated during the SiC CVD process, not during mold fabrication, as the surfaces of a typical Si mold are smooth and featureless. It has been reported that depositing SiC at low deposition rates using MTS as the precursor gas results in void formation in the Si substrate **[4]**. It was hypothesized that the irregular SiC device morphology was a consequence of this phenomenon.

Energy Dispersive Spectroscopy (EDS) was performed on the SiC atomizer swirl chamber floor to investigate the outgrowths. This technique was used to eliminate the possibility of contamination leading to the formation of these protrusions. The analysis clearly showed that no contaminants were detected. In an effort to minimize this surface roughness, 3C-SiC thin films were deposited on the mold surfaces prior to the high-rate deposition to produce a void-free interface between the Si and the thick SiC. The thin-film SiC was deposited using a three-step

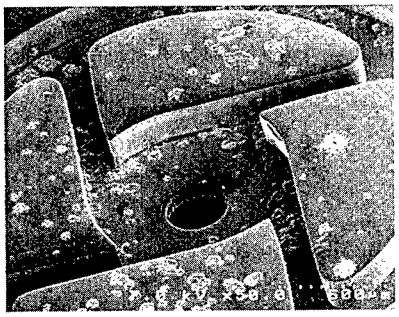


Fig. 2: SEM of a SiC atomizer fabricated without a 3C-SiC interface layer.

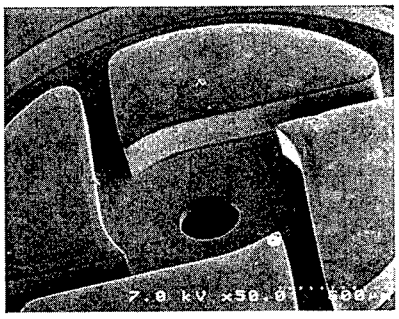


Fig. 3: SEM of a SiC atomizer fabricated with a 3C-SiC interface layer.

deposition process beginning with an *in situ* hydrogen clean, followed by the formation of a carbonization layer, and terminating in the growth step using propane and silane as the reactant gases **[5]**. Using this to deposit 3C-SiC on planar 4-in substrates, we are able to achieve negligibly low void densities (less than 2 voids/cm^2) at the SiC/Si interface. For this work, the interface layer was deposited to a thickness of 1.5 μm. Earlier work has shown, however, that there is a 1 μm film thickness variation from the swirl chamber floor to the top of the swirl chamber wall **[6]**, resulting in a film thickness of 0.5 μm at the swirl chamber floor. The result was a dramatically improved surface morphology, which substantiates the earlier explanation for the roughness of the device surface. The SEM micrograph in Fig. 3 shows a device with using the 3C-SiC thin-film as an interface layer between the Si and the thick SiC.

To investigate the microstructure of the thick SiC deposition, X-ray diffraction (XRD) was performed on a fully released atomizer. To ensure that the device topography and 3C-SiC mold coating had little effect on the diffraction spectrum, the bottom side of the atomizer, which is planar except for the exit orifice, was probed. Peaks from the (111), (200) and (220) 3C-SiC planes were clearly visible, suggesting a random polycrystalline microstructure. No peaks from unreacted Si crystallites or any other impurities were seen. Optically, the atomizers are opaque, with a dark gray appearance, which is consistent with reports by others **[7]** for randomly-oriented thick polycrystalline SiC deposited by MTS on graphite mandrels at 1350°C in a low pressure CVD reactor. The optical appearance is rough on the polished surface, but specular on the molded surfaces, an indication of the fidelity of the DRIE step and the 3C-SiC coating.

Conclusion

Using deep reactive ion etched Si molds, polycrystalline SiC bulk micromachining has been demonstrated. Epitaxial 3C-SiC films used as Si/thick poly-SiC interface buffers have been shown to improve the surface morphology of devices fabricated in this manner. Though mold fabrication is a batch process, the mold filling is performed on small area dies to compensate for thermal mismatch effects. Work still remains to be done before the bulk micromachining of SiC microstructures can be truly considered a batch fabrication process.

Acknowledgments

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Preliminary Investigation of SiC on Silicon for Biomedical Applications

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Keywords: 3C, Biomedical Probe, MEMS, Microelectromechanical, Reactive Ion Etching, RIE, SF_6

Abstract Reactive ion etching experiments were conducted with the intent of constructing a 3C-SiC on silicon heart probe to be used for biomedical applications. Experiments were performed with 3C-SiC as well as 4H-SiC in order to optimize the process for the heart probe construction. The heart probes were patterned on 3C-SiC on silicon to create a hybrid device that would combine the strength and inertness of the 3C-SiC material with the electronic compatibility of Si material to provide a complete probe suitable for reliable and disposable use required by the medical industry.

Introduction

Etching of cubic silicon carbide (3C-SiC) has been reported for a variety of applications including membranes for accelerometers and high-temperature microelectromechanical systems (MEMS) [1,2]. In this new application, heteroepitaxy growth of single crystalline 3C-SiC on silicon is used to form various probe geometries for insertion into hearts for pick-up of electrical signals during cardiac strain. Conventional silicon probes (or needles) used have insufficient material strength to allow sufficient probe integrity [3,4], whereas the superior mechanical strength and hardness of SiC (shown in Table 1) should prove advantageous. Additional advantages of using silicon carbide are anticipated from the high level of inertness of SiC to biological tissue, and from the ability to transmit data electronically or optically from the probe tip to the heart exterior. Continuing to use a silicon substrate could provide long-term benefits in more complex electronics integration, and retaining a higher degree of elasticity than is possible in a silicon carbide homogeneous system. In this work, we report on preliminary investigations into fabricating simple heart probe structures utilizing silicon carbide on silicon, with commercial silicon chips attached to the probes in hybrid fashion.

Table 1: Selected mechanical properties of SiC and Si.

PROPERTY	3C-SiC	4H-SiC	Silicon	6H-SiC
Bandgap (eV)	2.3	3.20	1.12	3.02
Commercial substrate? (dia.)	N	Y (50 mm)	Y (300 mm)	Y (50 mm)
Young's modulus (GPa)	392-448		190 *<111> dir.*	
Mohs hardness	**~ 9**	**~ 9**	**7.0**	**~ 9**
Relative dielectric constant (ε_r)	10.0	10.0	11.7	10.0

SiC Heart Probes

To fabricate the heart probes, cubic silicon carbide is grown on silicon wafers, then patterned for the electrical contacts and mechanical probe structure. Heteroepitaxy of 3C-SiC on Si is achieved in three distinct steps; first the native oxide is removed using a hydrogen in-situ etch, second a carbonization step is performed to form the initial layer of silicon carbide, and third the 3C-SiC film is grown [5,6,7]. After growth of a 6-7 μm silicon carbide film, backside polycrystalline 3C-SiC

was removed via mechanical polishing. The heart probe processing uses a two mask process for the hybrid device. Metal contacts are first patterned for bonding of commercially available silicon small-outline transistor (SOT) packages or discrete die for signal amplification. Metal traces for conduction from the probe tip (for signal pick-up) to the die for (signal amplification) are also made during this step. The second mask level deposits selective metal protection for etching of the physical heart probe structures. Approximately 4 kÅ of aluminum was deposited using D.C. sputtering to be used as the mask for reactive ion etching. For the heart probe etch, the 3C-SiC etch rate (in SF_6 : He) was 491 Å/min, while the silicon etch rate was 1333 Å/min and the aluminum etch rate was 13 Å/min, yielding excellent selectivity. Etch development details are reported below. Unlike typical SiC MEMS applications, where freestanding SiC membranes are desired, this application requires the patterning and etching of the 3C-SiC and underlying silicon as one component. As is seen in Figure 1, a smooth, anisotropic sidewall is obtained on the 3C-SiC film, while the underlying Si has a large amount of undercutting, and very poor surface morphology. Future work will require optimizing a single etch process for 3C-SiC and Si anisotropic etching, or developing an etch stop so that the etch process can be quickly modified upon reaching the Si.

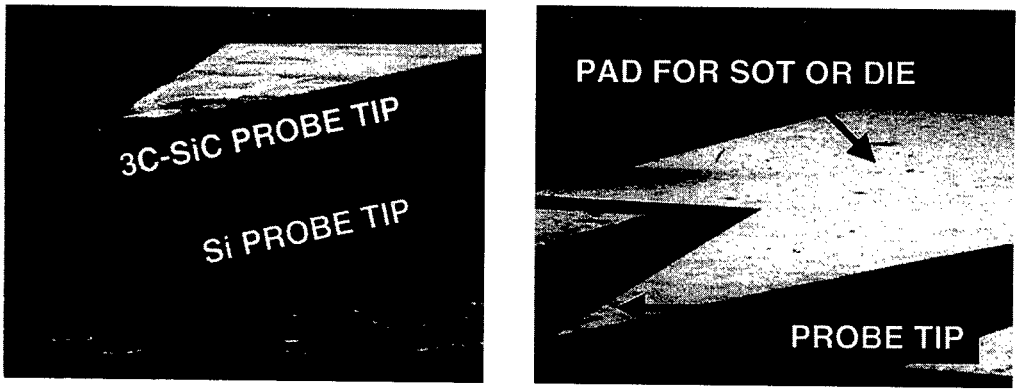


Figure 1: SEM micrographs of 3c-SiC on silicon heart probe tip at a) high-power (2.4 kX) magnification and b) low-power (40 X) magnification. Note the significant undercutting of the silicon in a).

SiC Etch Development for Heart Probe Applications

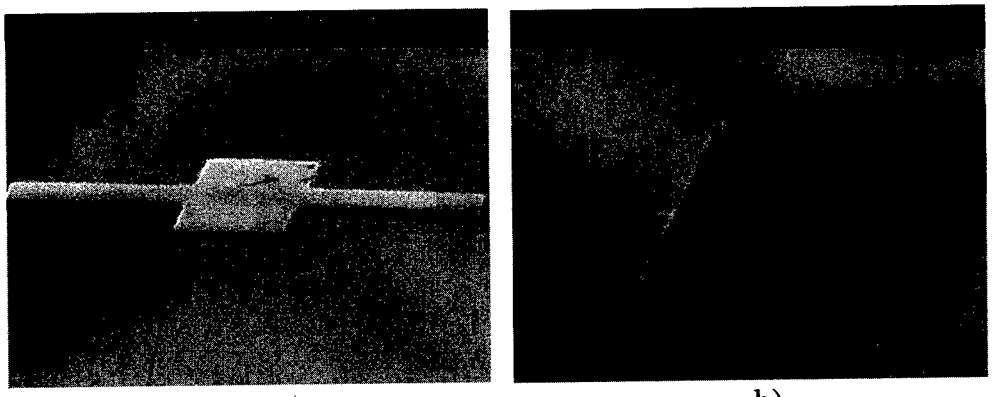
3C-SiC Baseline Etch Process

The RIE was performed on a parallel plate plasma system with variable electrode-to-sample spacing, similar to that reported in [8]. This system operates at 13.56 MHz using a SF_6:He (5:10 sccm) plasma for 3C-SiC etching. A baseline etch recipe developed for 3C-SiC was 210 mT with a RF power of 10 W, which yields an average power density of 0.906 W/cm^2 normalized to the electrode area. The etch rate was 491 Å/minute for this baseline process. In this configuration, an electrode spacing of 2.5 cm was used with the electrodes having a diameter ratio of 1.33, with the powered electrode made from molybdenum, and the grounded electrode manufactured from aluminum. This is an inverted electrode configuration, with the powered electrode on the bottom (holding the sample) and the grounded electrode on the top, thereby reducing the etch residue normally left on the sample during the RIE process.

4H-SiC Baseline Etch Process

The system and procedures used for the 4H-SiC etch process are similar to those used for the 3C-SiC process, except for the plasma composition. For the 3C-SiC etch process a combination of SF_6

and He was used, while the 4H-SiC process was optimized using SF_6 and O_2. Also, instead of using an aluminum mask as was done with 3C-SiC, for 4H-SiC a nickel mask was used to improve mask selectivity. This same system was used to develop a baseline etch process with an RF power of 10 W (power density of 0.906 W/cm^2) at 13.56 MHz, and using a SF_6:O_2 (5:10 sccm) plasma at 180 mT. The etch rate for this baseline process was 240 Å/minute. The electrode spacing in this process is also set to 2.5 cm, and produces a clean, smooth surface morphology, as is seen in Figure 2.



a) b)

Figure 2: SEM micrographs of 4H-SiC test etch at a) low-power magnification (1.42 kX) and b) high-power (10 kX) magnification. Note the excellent surface morphology and nearly vertical sidewall etch. Grooves in sidewall are a result of the photolithography process.

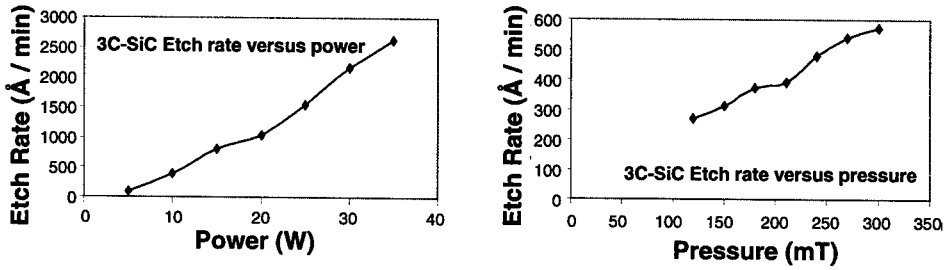
Etch Development

To optimize the etch process for the heart probe, modifications are clearly necessary. For the 3C-SiC etch process, higher etch rates will be required depending upon the thickness of 3C-SiC films. Much thicker (up to 40 μm) 3C-SiC films may be required to provide the overall probe rigidity and strength necessary to maintain probe integrity. For an all SiC heart probe in 4H-SiC, which would offer integrated rather than hybrid electronics sensing, amplification, and processing, the etch could be even deeper (up to 100 mm) similar to that required for via development in microwave applications [9]. Etch experiments were performed on both 3C-SiC and 4H-SiC at various RF power settings (5 to 35 watts), various pressures (100 to 300 mT) to evaluate mask integrity, surface morphology, and etch rate. When an optimum power density was realized for a set pressure, the pressure was then varied about that optimum power density. All experiments were performed with a constant gas ratio of SF_6:O_2 ; 5:10 sccm for 4H-SiC and SF_6:He ; 5:10 sccm for 3C-SiC. The etch selectivity of 4H-SiC to nickel was greater than 20 for all etch recipes, even at the highest power level of 35 W (3.171 W/cm^2). The etch selectivity of the 3C-SiC to aluminum was greater than 40 for the baseline process, and greater than 10 for the highest power level of 35 W. As can be seen in Figure 3, the peak etch rate for 4H-SiC was 1400 Å/minute, which is very comparable to peak RIE rates reported for 4H-SiC using pure NF_3 [10]. The 3C-SiC etch rates reached nearly 3000 Å/minute, which is one of the highest etch rates for RIE of single crystalline 3C-SiC we have seen reported [11]. It should be noted that, unlike many 3C-SiC MEMS applications, this 3C-SiC is single crystalline material which generally has a slower etch rate than amorphous or polycrystalline 3C-SiC [12].

Summary

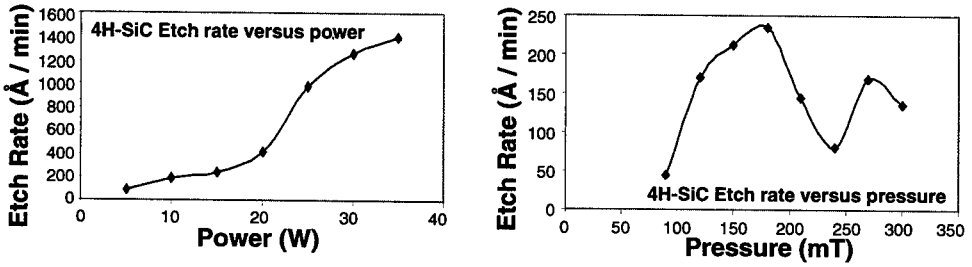
We have reported on preliminary optimization work for developing suitable etch processes of 3C-SiC and 4H-SiC necessary to fabricate self-consistent biomedical probes. These probes will have advantages over traditional silicon-based probes in terms of mechanical strength, and the ability to

sense both electrical and optical signals within the organic tissue. Specific etch requirements needed for probe fabrication include a very high etch rate, smooth surface morphology, and good mask selectivity for both polytypes. We have obtained maximum etch rates of over 2500 Å/minute in single crystalline 3C-SiC, and approximately 1400 Å/minute in 4H-SiC. Both of these etch rates are quite high when comparing to previously published RIE rates [11]. Surface morphology and mask selectivity was adequate for the etches examined here, but maintaining both morphology and selectivity while increasing the etch rate, will require further research.



a) b)

Figure 3: 3C-SiC etch rates a) versus power with pressure at 100 mT and b) versus pressure with power at 10 W.



a) b)

Figure 4: 4H-SiC etch rates a) versus power with pressure at 100 mT and b) versus pressure with power at 10 W.

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Chapter 5

SiC Devices

Materials Science Forum Vols. 338-342 (2000) pp. 1155-1160

SiC and GaN High-Voltage Power Switching Devices

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Keywords: GaN, SiC, Switching Devices

ABSTRACT

The present status of high-voltage SiC and GaN power semiconductor switching devices is reviewed. The choice and design of several key device structures are discussed. The performance expectations of the major two- and three-terminal unipolar and bipolar devices in SiC and GaN are presented and compared. The progress in high-voltage power device experimental demonstration is reviewed. The material and process technology issues that need to be addressed for device commercialization are discussed.

INTRODUCTION

Silicon has long been the dominant semiconductor of choice for high-voltage power switching device applications [1,2]. However, recently, wide bandgap semiconductors, particularly SiC and GaN, have attracted much attention because they are projected to have much better performance than silicon, particularly at breakdown voltages above 1000V. The superior physical properties of these semiconductors offer a lower intrinsic carrier concentration (10 to 35 orders of magnitude), a higher electric breakdown field (4-20 times), a higher thermal conductivity (3-13 times), a larger saturated electron drift velocity (2-2.5 times), when compared to silicon (See Table I). Also, interestingly, unlike silicon, the hole ionization coefficient (α_p) is larger in SiC and GaN than the electron coefficient (α_n).

Among the three SiC polytypes (3C, 6H and 4H) with available bulk commercial wafers and/or epi layers, 4H-SiC has become the polytype of choice because it has higher carrier mobility and more isotropic nature of its properties when compared to 6H-SiC. Commercial bulk GaN substrates are not yet available, so most of commercial GaN films (2H-GaN only) are grown heteroepitaxially either on sapphire or 6H-SiC substrates.

The potentials of SiC and GaN power switching devices were clearly demonstrated several years ago with the calculated unipolar and bipolar figures of merit (Table II). In this paper, we will comparatively examine SiC (particularly the 4H polytype) and 2H-GaN for power electronics applications. The electrical performance of two- and three-terminal devices expected will be presented. The recent experimental demonstrations of power switching devices in these two semiconductors will be reviewed. Also, the outstanding material and processing issues that need to be overcome for device commercialization will be pointed out.

DEVICE CHOICES AND STRUCTURES

Both two- and three-terminal devices are needed to construct basic power circuit units, such as a half-bridge circuit. While SiC power rectifiers strongly resemble those of silicon, GaN rectifiers are either quasi-vertical (Fig. 1) or lateral when they are grown on insulating substrates like sapphire. High-voltage Schottky

rectifiers offer fast switching speed but suffer from high on-state voltage drop and on-resistance because mostly majority carriers participate in its forward conduction. By contrast, the pin junction rectifier has low forward drop and high current capability due to conductivity modulation, but has slow reverse recovery characteristics due to minority carrier storage. SiC has an edge over GaN in bipolar devices due to its indirect bandgap and hence longer minority carrier lifetimes. To combine the best features of these two rectifiers, hybrid rectifier structures, such as the Junction Barrier Schottky (JBS), Merged Pin/Schottky (MPS) and MOS Barrier Schottky (MBS) rectifiers have been proposed and have been demonstrated in silicon [2]. Also, whereas the crossover voltage between Si Schottky and junction rectifiers is about 100V, primarily due to the excessive reverse leakage current of the Schottky rectifier at elevated temperatures. We estimate the practical upper reverse blocking voltage limit for 4H-SiC Schottky rectifiers is about 2000V.

UMOS in SiC is popular since the p-body layer is formed by epitaxy due to slow diffusion of most dopants but several groups have used ion implantation to demonstrate DMOS devices in 6H- and 4H-SiC. However, care must be taken to avoid high electric field at the trench corners of the UMOS as well as under the gate oxide in the JFET region of the DMOS. Compared to GaAs, GaN MIS structures appear to be much easier to implement. Also, since GaN is most often grown on electrically insulating sapphire substrates, lateral device structures as well as quasi-vertical devices are most relevant. However, if GaN is grown on heavily doped SiC substrates, vertical power device structures are also possible. Another important device concern that needs to be addressed is the high electric field in the gate insulator (usually SiO_2) due to the high SiC and GaN avalanche field. Conventional power MOS structures (UMOS and DMOS) would lead to an oxide field of 3 to 7.5×10^6 V/cm, leading to potential device reliability problems. Besides, because of their much higher bandgaps, both SiC and GaN MOS would be more susceptible to hot electron problem, particularly at elevated temperatures, because of their much smaller potential barriers at the oxide/semiconductor interface (<2.7eV vs. 3.15eV in Si). To minimize the hot electron problem and improve channel electron mobility, accumulation mode MOSFET's have also been explored.

Besides the conventional GTO, the UMOS devices include the power MOSFET, IGBT and MOS-Controlled Thyristor (MCT). The most popular silicon power bipolar transistor is the IGBT, in which a MOSFET is connected to the base of a bipolar transistor in a Darlington configuration. In the on-state, the n-channel IGBT can be considered as an n-channel MOSFET driving a wide-base pnp bipolar transistor. In silicon, the n-channel MOSFET has a better transconductance than the p-channel one due to a higher electron mobility and the pnp is more rugged and less susceptible to second breakdown than the npn due to a larger electron ionization coefficient. Hence, the n-channel IGBT has a larger safe-operating area than and is preferred over the p-channel one. The n-channel MGT (**M**OS-**G**ated **T**ransistor), which can be fabricated in the same IGBT process and has been demonstrated in silicon, has an n-channel MOSFET driving a narrow-base high-voltage npn transistor. On one hand, this device has more current non-uniformity and less conductivity modulation in the on state when compared to the IGBT. On the other, it does not have a four-layer parasitic thyristor and has an optional n-channel turn-off MOSFET. In addition, the hole ionization coefficient is larger than the electron coefficient in SiC and, thus, the npn is now more rugged than the pnp. Furthermore, the MGT uses an n+ substrate, which can be doped heavier than the p+ substrate for the n-channel IGBT. In light of these considerations, it is worth considering both the MGT and the IGBT for SiC power devices[3].

The unipolar and bipolar figures of merit in Table II compare silicon devices with the wide bandgap ones. However, for each semiconductor, dependent on its bandgap, there is a crossover in voltage rating above which bipolar devices are preferred over unipolar ones due to the reduced drift-layer resistance from conductivity modulation of bipolar carrier injection. For silicon, this voltage is about 300V whereas, for SiC and GaN, it is about 3000V. Also, with increasing operating temperature, this cross-over voltage is expected to decrease since the ON-resistance of unipolar devices varies inversely as the second power of temperature while the turn-on voltage decreases and carrier lifetimes increase. In addition, in SiC, electrons also have a higher mobility but have a lower impact ionization capability than holes. These considerations lead to the inclusion of a p-channel IGBT in SiC.

DEVICE DESIGN AND PERFORMANCE

(a) Breakdown Voltage -

We have approximated the SiC ionization coefficients by a single ionization coefficient and obtained the ideal breakdown voltage (BV_{pp}) and depletion layer width at breakdown (W_{pp}) as a function of background doping as shown in Fig. 2 for 6H- and 4H-SiC. The analytical calculations have been corroborated well with numerical simulations and experimental results. Similar calculations have been performed on 2H-GaN. High-voltage open-base bipolar transistor (BV_{CEO}) design depends primarily on minority carrier lifetime and $BV_{CEO} \propto (1 - \alpha_0)^{1/n}$, where α_0 is the common-base current gain, n is 4 for npn and 6 for pnp transistors in silicon. For 4H-SiC, we have found that n is 13 for npn and 3 for pnp. Hence, unlike silicon, the SiC npn transistor has much better open-base breakdown characteristic than the pnp counterpart. Proper termination must also be designed and processed to minimize the effect of junction curvature on the BV to realize the optimal blocking voltage of a power switch. Termination structures that have been utilized include implanted Junction Termination Extension (JTE), three-step termination, floating field rings, and mesa-isolation. Among these, JTE is the most flexible and easiest to optimize while the three-step termination and mesa-isolation are most compatible with the trench UMOS processes.

(b) Static Characteristics -

Fig. 3 illustrates the $R_{ON,sp}$ vs. BV relationship calculated for n-type Schottky rectifiers on silicon, 6H-SiC and 4H-SiC. At low values of BV (< 500V for SiC), the substrate resistance dominates the specific on-resistance. When the BV exceeds 1000V, the drift resistance starts to be the main limiting factor and the increase in R_d is a direct consequence of the increase in drift layer thickness and reduction in drift layer doping. We have also included recent published experimental results [4] in Fig. 3. As seen in Fig. 4, experimental SiC Schottky rectifiers have achieved significant improvement over Si counterparts, but they are still not yet at performance levels expected from the theoretical predictions. The highest reverse blocking voltage reported so far for a 4H-SiC Schottky rectifier is about 5000V. By contrast, experimental GaN rectifiers [5] only approach the performance limit for Si devices at present and BV < 1000V.

SiC MOSFETs have demonstrated lower on-resistance than that of silicon devices (Figure 5). At room temperature, the 5000V IGBT and GTO have a lower forward drop than the power MOSFET only at current densities exceeding 100 A/cm^2. However, at higher temperatures, both the GTO and the IGBT are superior and the difference between the GTO and IGBT is small. Because a p-channel IGBT has an n+ substrate, which can be readily heavily doped, it is also included for forward I-V comparison with the n-channel IGBT and MGT. At room temperature, both the n-MGT and p-IGBT have better I-V characteristics than the n-IGBT. However, at 400°C, the n-channel IGBT is clearly superior to either the p-IGBT or n-MGT. Experimentally, both n- and p-channel IGBT's have been demonstrated in either 6H- or 4H-SiC up to 800V but the forward drop is still far from optimal. Symmetric and asymmetric 4H-SiC gate-controlled thyristors reported have breakdown voltages up to 1000V and current-handling capabilities up to 6A.

(c) Switching Times -

Unipolar devices switch very fast (~ 1ns). By contrast, minority carrier storage, bipolar devices, like the IGBT and GTO, slows down the turn-on and turn-off times. However, SiC IGBT's and GTO's are significantly faster than the silicon counterparts of the same voltage rating due to a much reduced drift layer. While the turn-off time of the MGT remains almost constant with increasing lifetime, that of the IGBT increases from 50 ns to 0.14 μs when the lifetime increases from 5 to 25 μs. The reason for the weak dependence of turn-off time on carrier lifetime in the MGT is due to the availability of a turn-off gate [6].

(d) Safe-Operating-Area -

To quantitatively assess the device operating margin, safe-operating-area (SOA) maps are often used. In silicon, the RBSOA of n-channel IGBT is much larger than the p-channel one due to the larger electron impact ionization coefficient (α_n). However, in 6H- and 4H-SiC, since the hole impact ionization coefficient

is larger the electron one, the RBSOA is larger for a p-channel IGBT. The RBSOA of an MCT is much smaller than that of the IGBT due to a higher degree of conductivity modulation and the tendency for filamentation [6]. GaN bipolar transistors are expected to have similar trends.

MATERIAL AND PROCESSING CHALLENGES

For high voltage devices, total epitaxial layer thickness of at least up to 30 μm with acceptable surface flatness and doping uniformity and minimum compensation is needed. To minimize parasitic substrate resistance and maximum carrier concentration, a doping of 10^{19} cm^{-3} would be desired. Such a high doping level seems to be difficult with p+ substrates. A micropipe density of less than $1/cm^2$ is needed to realize devices of current ratings larger than 100A with reasonable yield. Other structural defects, such as elementary screw dislocations, appear to correlate with excessive leakage current in 4H-SiC pn junctions [7]. Bulk GaN substrates would allow vertical homojunction power devices unless heteroepitaxial growth of GaN over SiC substrates yields high-quality material and low resistances.

The MOS interfacial parameters of thermally grown oxide on SiC continue to improve but the correlation between surface state densities with inversion layer mobility is weak. The improvement of inversion layer mobility is the biggest obstacle for power MOS device development in 4H-SiC and 15R polytype seems to be better in this regard [8]. No inversion mode MISFETs has been reported for GaN. Recent advances in n-type implantation yield sheet resistance values approaching those in silicon (< 100 Ω/square) but p-type implanted layers still have too high a sheet resistance (> 5 KΩ/square). N- and p-type Ohmic contacts with low contact resistivities (< 10^{-6} Ω-cm^2) are necessary to fully exploit the intrinsic device performance enhancement offered by SiC. Also, it would be desirable to use the same contact metallization to both n- and p-type contacts so as to minimize the pitch in UMOS and DMOS unit cells, but more process development is needed to achieve this.

SUMMARY

We have reviewed the present status of SiC and GaN power devices for high-voltage power electronics applications. In particular, we have presented the choice and design of device structures, expected device performance, recent experimental demonstrations, material and processing challenges of SiC and GaN power devices. Commercial SiC power devices are starting to be available.

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Table I: Physical properties of important semiconductors for high-voltage power devices.

Material	E_g eV	n_i cm^{-3}	ε_r	μ_n $cm^2/V \cdot s$	E_c $10^6 V/cm$	v_{sat} $10^7 cm/s$	λ $W/cm \cdot K$	*Direct Indirect*
Si	1.1	1.5×10^{10}	11.8	1350	0.3	1.0	1.5	I
Ge	0.66	2.4×10^{13}	16.0	3900	0.1	0.5	0.6	I
GaAs	1.4	1.8×10^{6}	12.8	8500	0.4	2.0	0.5	D
GaP	2.3	7.7×10^{-1}	11.1	350	1.3	1.4	0.8	I
InN	1.86	$\sim 10^3$	9.6	3000	1.0	2.5	-	D
3C-GaN	**3.27**	**8×10^{-9}***	**9.9**	**1000**	**1**	**2.5**	**1.3***	**D**
2H-GaN	**3.39**	**1.9×10^{-10}**	**9.0**	**900**	**3.3**	**2.5**	**1.3**	**D**
3C-SiC	**2.2**	**6.9**	**9.6**	**900**	**1.2**	**2.0**	**4.5**	**I**
4H-SiC	**3.26**	**8.2×10^{-9}**	**10**	**720[a] 650[c]**	**2.0**	**2.0**	**4.5**	**I**
6H-SiC	**3.0**	**2.3×10^{-6}**	**9.7**	**370[a] 50[c]**	**2.4**	**2.0**	**4.5**	**I**
Diamond	5.45	1.6×10^{-27}	5.5	1900	5.6	2.7	20	I
BN	6.0	1.5×10^{-31}	7.1	5	10	1.0*	13	I
AlN	6.1	$\sim 10^{-31}$	8.7	1100	11.7	1.8	2.5	D

Note: *a* — mobility along a-axis, *c* — mobility along c axis, *— estimate.

Table II: Normalized unipolar figures of merit of important semiconductors for high-voltage power devices.

Material	λ	JM $(E_c v_{sat}/\pi)^2$	MJM λ*JM	KM $\lambda(v_{sat}/\varepsilon_r)^{1/2}$	Q_{F1} $\lambda\sigma_A$	Q_{F2} $\lambda\sigma_A E_c$	BM (Q_{F3}) $\varepsilon_r \mu E_c^3$	BHFM μE_c^2
Si	1	1	1	1	1	1	1	1
Ge	0.4	0.03	0.012	0.20	0.06	0.02	0.2	0.3
GaAs	0.33	7.1	2.4	0.45	5.2	6.9	15.6	10.8
GaP	0.53	37	20	0.7	10	40	16	5
InN	-	58	-	-	-	-	46	19
3C-GaN	**0.87**	**685**	**595**	**1.5**	**20**	**67**	**23**	**8.2**
2H-GaN	**0.87**	**760**	**655**	**1.6**	**560**	**6220**	**650**	**77.8**
3C-SiC	**3**	**65**	**195**	**1.6**	**100**	**400**	**33.4**	**10.3**
4H-SiC	**3**	**180**	**540**	**4.61**	**390**	**2580**	**130**	**22.9**
6H-SiC	**3**	**260**	**780**	**4.68**	**330**	**2670**	**110**	**16.9**
Diamond	13.3	2540	33800	32.1	54860	1024000	4110	470
BN	8.7	1100	9700	11	715	23800	83	4
AlN	1.7	5120	8700	21	52890	2059000	31700	1100

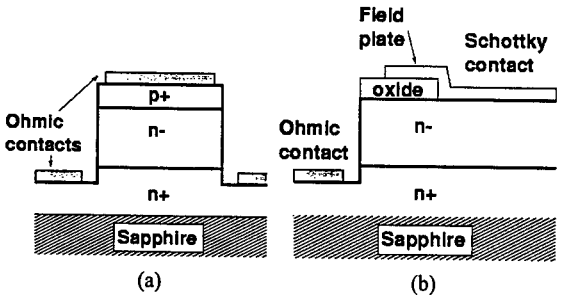

Fig. 1 Schematic cross-sections of (a)p-n junction and (b)Schottky quási-vertical power rectifier structures that can be implemented in GaN on sapphire substrates.

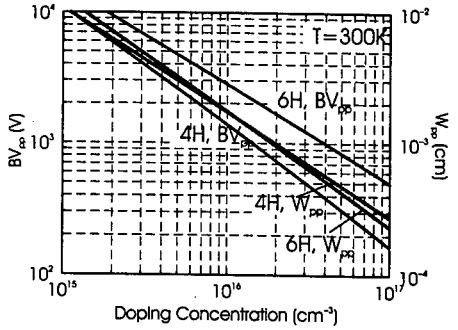

Fig. 2 Breakdown voltage of parallel-plane, one-sided abrupt junction (BV_{pp}) and its depletion layer width at breakdown (W_{pp}) of 6H- and 4H-SiC at 300K.

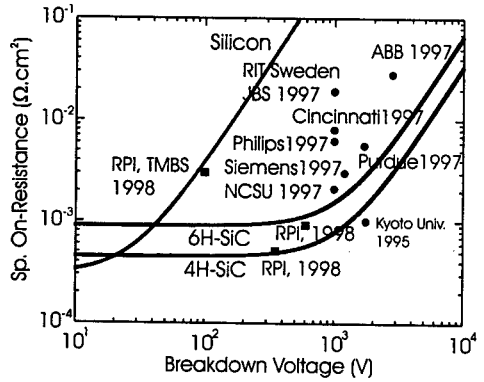

Fig. 3 Specific on-resistance vs. breakdown voltage for various Schottky rectifiers on SiC. Experimental results and analytical calculations at 100 A/cm^2 and 300 K.

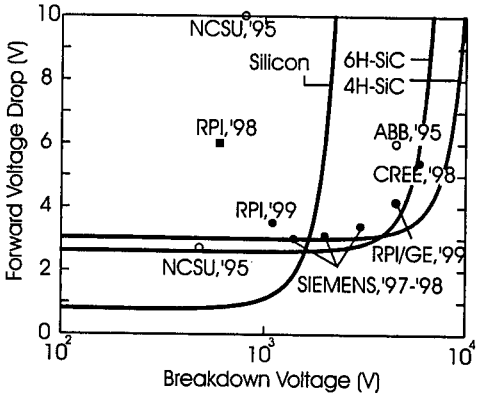

Fig. 4 Forward voltage drop vs. breakdown voltage for various pin junction rectifiers on 4H-SiC. Experimental results and analytical calculations at 100 A/cm^2, with $\tau_{n0} = 0.1$ s and $\tau_{n0} = 10\tau_{p0}$.

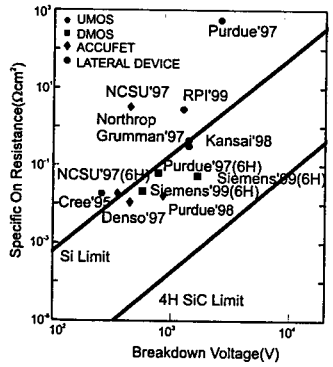

Fig. 5 Specific on-resistance vs. breakdown voltage for various MOSFET structures on SiC, including intrinsic material limits for Si and 4H-SiC.

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Electrical Impact of SiC Structural Crystal Defects on High Electric Field Devices

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Keywords: Avalanche Breakdown, Crystal Defect, Diode, Epilayer Growth Pits, Micropipe, Microplasmas, pn Junction, Rectifiers, Reliability, Safe Operating Area, Schottky Diodes, Screw Dislocation

Abstract: Commercial epilayers are known to contain a variety of crystallographic imperfections, including micropipes, closed core screw dislocations, low-angle boundaries, basal plane dislocations, heteropolytypic inclusions, and non-ideal surface features like step bunching and pits. This paper reviews the limited present understanding of the operational impact of various crystal defects on SiC electrical devices. Aside from micropipes and triangular inclusions whose densities have been shrinking towards manageably small values in recent years, many of these defects appear to have little adverse operational and/or yield impact on SiC-based sensors, high-frequency RF, and signal conditioning electronics. However high-power switching devices used in power management and distribution circuits have historically (in silicon experience) demanded the highest material quality for prolonged safe operation, and are thus more susceptible to operational reliability problems that arise from electrical property nonuniformities likely to occur at extended crystal defects. A particular emphasis is placed on the impact of closed-core screw dislocations on high-power switching devices, because these difficult to observe defects are present in densities of thousands per cm^2 in commercial SiC epilayers, and their reduction to acceptable levels seems the most problematic at the present time.

Introduction: As illustrated by the invited paper of Dudley [1] at this conference, SiC wafers and epilayers contain a variety of crystallographic structural imperfections. The degree to which each kind of crystal defect impacts a given device is quite application-specific, strongly dependent on a combination of both the electrical operating requirements and the physical layout of each particular SiC device structure. Almost all useful semiconductor electronic devices require rectifying junctions in order to function properly. The fundamental properties of transistors (i.e., gain, voltage and current ratings, operating speeds, etc.), be they unipolar (MESFET, JFET, MOSFET, etc.), bipolar (BJT, Thyristor, GTO, etc.), or hybrid (IGBT, etc.) depend largely on the fundamental conduction and/or blocking characteristics of Schottky and/or pn junctions within the transistor device structure. Therefore, the primary failure mode addressed in this work is the loss or degradation of 2-terminal junction rectifying characteristics, particularly at high electric fields (on the order of megavolts per cm) where SiC is expected to operate with the largest benefits over conventional silicon and GaAs electronics in high-power applications. Only commercially available slightly-off (0001) wafer orientations are considered, as other potential wafer orientations have not yielded advantageous high-field device results to date. While not addressed in this paper, there are likely to be other application-specific consequences of crystal imperfections beyond degradation of junction rectifying properties.

Crystal Defects: Most envisioned SiC devices are fabricated so that their electrically active regions reside entirely within homoepilayers grown on top of mass-produced 6H- and 4H-SiC wafers cut and polished a few degrees off the (0001) crystallographic surface. Therefore, the defects contained in these epilayers are of greatest interest to electrical device and circuit manufacturers. Figure 1 schematically depicts some of the SiC epilayer defects that could impact electrical device performance, including micropipes, closed-core screw dislocations, small growth pits, and triangular inclusions. Other defects not pictured in Figure 1 include basal plane dislocations, edge dislocations, low-angle boundaries, and carrot and comet-tail defects [2-4]. It is important to note that the vast network of basal plane dislocation loops found in the commercial PVT-grown bulk wafers are not found in subsequently grown epilayers [5], so that homoepitaxial 6H and 4H devices automatically contain significantly fewer crystal defects than similar devices fabricated directly in bulk wafers.

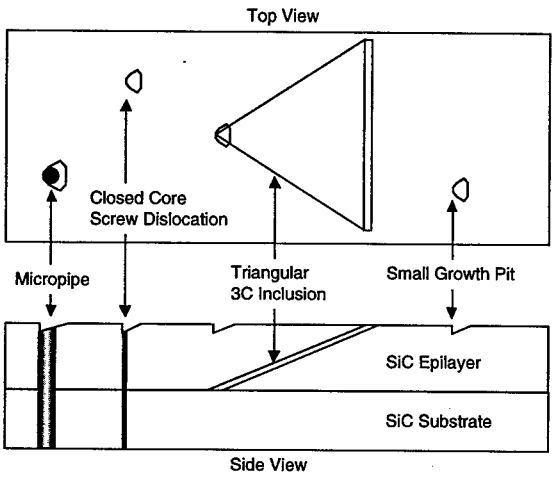

Figure 1: Some common SiC epilayer defects that impact high-field device properties.

The density of each specific defect determines the size and numerical yield of devices that hit or miss each defect. It is also important to consider the root causes of each defect and whether or not certain kinds of defects will be greatly reduced in density in the near future as crystal growth processes improve. The reported densities of some of the various defects in commercial epilayers are summarized in the first two columns of Table I.

Epitaxial Growth Defects: SiC Schottky-based rectifiers offer large benefits to high-power systems because their unipolar conduction enables much faster high-voltage switching that will enable shrinking of power system passives as well as increased power converter efficiency. The quality and smoothness of the semiconductor surface is well-known to critically control the electrical properties of rectifying Schottky diode junctions, especially since peak electric fields occur near the metal-semiconductor interface while current is exponentially controlled by the metal-semiconductor potential barrier [6]. The presence of non-smooth surface features routinely observed by atomic force microscopy on SiC epilayer surfaces could perturb the local electric field and thermionic carrier emission properties, which could result in locally increased current under both forward and reverse. Previous works have forcefully argued that SiC Schottky diode I-V properties are controlled by small localized surface defects that have a lower effective Schottky barrier height [7-9]. However, conclusive links between specific types of SiC surface defects and specific non-ideal Schottky I-V properties remain to be experimentally proven.

It is plausible that pn junction devices are perhaps less-affected by SiC surface defects, primarily due to the fact that the peak electric field and current conduction mechanisms (primarily recombination) occur at the metallurgical junction buried within the semiconductor. However, pn junction forward and/or reverse characteristics can be expected to track with surface imperfections in those cases where the surface defect arises due to an extended defect that actually runs through the thickness of the epilayer to intersect the metallurgical pn junction. Such behavior has been observed by Kimoto for 3C triangular inclusions, which were found to greatly increase leakage

Table 1: Selected Properties of SiC Epilayer Extended Structural Defects in High-Field Devices

SiC Epilayer Defect [References]	Density (#/cm^2)	Observed Defect Sources	Observed Impact on High-Field Junction	Summary Comments (see text)
Micropipe Hollow Core Screw Dislocation [1, 4, 11, 13]	< 30 (commercial) < 1 (best)	Substrate micropipes that propagate into epilayer.	> 50% breakdown voltage reduction. Microplasmas. Increased leakage currents.	Densities improving to where they may not be present in most ~ 1 cm^2 power devices in a few years.
Closed Core Screw Dislocation [1, 10, 14-16, 18]	~ 3000 to ~ 10000	Substrate screw dislocations that propagate into epilayer.	~10-30 % breakdown voltage reduction. Softened breakdown Microplasmas. Carrier lifetime reduction.	**Densities slowly improving, but will be present and affect ~ 1 cm^2 sized power devices for many years .**
Triangular 3C Inclusions [2-4, 10]	< 5	Wafer preparation & epitaxial growth process.	> 50% breakdown voltage reduction. Increased leakage currents.	Densities improving to where they may not be present in most ~ 1 cm^2 power devices in a few years.
Carrots & Comet Tails [2-4]	< 5	Undetermined.	Some increase in pn junction leakage. Non-smooth surface seems likely to impact Schottky rectifying properties.	Densities improving to where these may not be present in most ~ 1 cm^2 power devices in a few years.
Small Growth Pits [2, 3, 9, 18]	> 3000	Closed core screw dislocations. Wafer preparation & epitaxial growth.	Non-smooth surface seems likely to impact Schottky rectifying properties.	Densities improving, but closed-core screw dislocation density may represent a limiting floor for these defects.

current and decrease breakdown voltage for kV-class epitaxial pn junction diodes [3]. Kimoto also observed an increase in reverse leakage current due to carrot/comet tail defects.

The X-ray studies of Si et. al. [10] found no evidence that epilayer triangular inclusions nucleated at substrate screw dislocations. Powell et. al. [2] demonstrated that many morphological imperfections in the as-grown SiC epilayer surface are greatly impacted by surface polish as well as epitaxial growth initiation process. Off-axis polish angle has been increased to successfully reduce 3C triangular inclusions in 4H-SiC epilayers [10]. Thus, while by no means trivial, it appears that defects arising from pre-epitaxial and epitaxial growth processing should become less important as these processes are optimized. Since present-day densities of triangular inclusions and carrot/comet tail defects are already less than 5 per cm^2 in commercial epiwafers [4], it appears that ~ 1 cm^2 power devices free of these particular defects could be manufacturable within a few years.

Micropipes (Hollow Core Screw Dislocations): SiC screw dislocations are well-known to originate in commercial 6H- and 4H-SiC wafers and propagate parallel to the crystallographic c-axis through the entire thickness of standard homoepilayers grown by CVD. As discussed by Dudley [1], screw dislocations with large Burgers vectors form hollow cores and are thus referred to as tubular voids or micropipes. Micropipes are well documented to cause premature reverse failure in high-field SiC devices [3,11,12]. However, SiC electronics designed to operate all internal device junctions at relatively low electric fields are least affected by crystal defects. SiC pn junction diodes, FET's and integrated circuits have all demonstrated an ability to function despite the

presence of micropipes running through key rectifying junctions as long as junction fields are kept to a small percentage of the theoretical SiC breakdown field. Steady improvements in SiC wafer quality has reduced SiC wafer micropipe densities from several hundreds per cm^2 in 1993 to less than 1 per cm^2 in 1998 in the best reported wafers [13], so that micropipe-free power devices on the order of 1 cm^2 area rated for 100's of amps on-state current would become feasible in the near term if other non-micropipe defects turn out to be harmless or are eliminated.

Closed Core Screw Dislocations: When the Burgers vector of an SiC screw dislocation is small enough, hollow core formation is avoided [1,14]. Nevertheless, the closed core screw dislocation possesses many properties similar to micropipes, starting with a propensity to undesirably propagate through bulk crystals and epilayers [1,5,15,16]. These defects are present in average densities on the order of several thousands (best) to around ten thousand per cm^2 in commercial wafers [1]. Because they have not declined in density over time as fast as micropipes, it would appear that all devices manufactured on mass-produced wafers whose active areas exceed ~ 1 mm^2 will contain these defects for the forseeable future.

While not as detrimental to device characteristics as micropipes, experimental evidence is emerging that closed core screw dislocations somewhat negatively impact the electrical properties of high-field SiC junctions. Much of the evidence is indirect largely because screw dislocations cannot be observed by conventional microscopic methods, and must instead be non-destructively observed in devices by X-ray topographic mapping. Unfortunately, few SiC device studies have sufficiently tracked device performance as a function of closed core screw dislocations. One study that did use X-ray topography to map closed core screw dislocations demonstrated that elementary screw dislocations are somewhat detrimental to the reverse leakage and breakdown properties of low-voltage (< 250 V) 4H-SiC p^+n diodes [15,16]. Examples of remarkably similar observations of increased reverse leakage, soft breakdown, and/or microplasmas not associated with micropipes are independently reported in the literature [12,17], even though none of these works carried out X-ray mapping to conclusively ascertain the presence of screw dislocations within their devices. The impact of closed core screw dislocations on higher voltage (> 1 kV) junctions and bipolar gain devices remains to be ascertained, as do physical mechanisms and models for the exact electrical behavior of these dislocations.

The work of Schnabel et. al. reported at this conference [18], in which a combination of Electron Beam Induced Current (EBIC) measurements were correlated with X-ray screw dislocation mapping and surface growth pit mapping, reveals two important observations regarding screw dislocations in SiC. First, all closed core screw dislocations mapped by X-ray were found to have clear EBIC signatures indicating a local reduction in the minority carrier lifetime in the immediate vicinity of the defect. This observation experimentally confirms previous suggestions that closed core screw dislocations were responsible for some (but clearly not all) of the defects observed in earlier SiC Schottky EBIC studies [7,8]. This also re-raises the possibility that closed core screw dislocations were responsible for destructive Schottky diode failure and localized negative temperature coefficient of breakdown observed in [8], which are clearly undesirable properties for high-power rectifier usefulness and reliability. The second important finding of [18] is that all closed core screw dislocations mapped by X-ray resulted in a corresponding small growth pit on the as-grown epilayer. This suggests that epilayer process improvements may not be able to reduce small growth pit densities below bulk wafer screw dislocation densities.

It is worth noting that some non-conventional epitaxial growth techniques have been attempted to prevent the propagation of micropipes and screw dislocations through SiC epilayers [19,20]. While these approaches seem to physically close and cover up micropipes, there has been little demonstrated performance improvement in high-field devices fabricated in the resulting material prior to this conference. Further studies into alternative growth approaches that reduce epilayer

screw dislocations seem warranted, but proof of feasibility must be demonstrated by greatly improved large-area high-field SiC diode performance.

High Power Devices & Circuits: As pointed out by Fazi et. al. [21], crystal defects are clearly much more harmful to devices that operate junctions at high electric fields (i.e., power devices), especially when the crystal defects perpendicularly cross the high-field metallurgical junction boundaries as is the case with screw dislocations on commercial SiC epiwafers. Steady reductions in SiC micropipe densities have enabled initial prototype DC demonstrations of high current SiC diodes in the neighborhood of 100 A. It is important to note, however, that most high-current SiC power devices reported to date are significantly derated, in that the experimentally demonstrated blocking voltages are usually significantly less than the theoretical blocking voltages calculated from epilayer doping and thickness. Similarly, the highest reported blocking voltage SiC devices (> 7 kV) have to date been very small-area (~ 10^{-4} cm^2, small enough to be free of closed core screw dislocations) with low on-state current rating well under 1 A. If micropipes are the only defect limiting SiC high power devices, much better experimental results combining optimum (i.e., near theoretical) high voltage and high current in a single large-area device should be obtainable.

Independent studies of micropipe-free pn high-voltage rectifiers have documented a clear trend that yield and standoff voltage decrease significantly as device area increases beyond ~ 5 x 10^{-4} cm^2 on any given SiC diode wafer [3,22,23]. Depending upon selection of specific yield criteria (i.e., the reverse voltage and leakage current used to define a "good" device), the defect densities extracted from these studies are on the order of thousands per cm^2. While these extracted densities are more consistent with close core screw dislocation and small growth pit densities than other known SiC defects, additional evidence that links specific defects to device degradation is clearly needed.

While SiC devices promise some of the largest operational benefits to electric power conversion and motor-drive systems, these circuits also impose the harshest operational stresses on semiconductor switches. Solid-state devices in modern day power conversion circuits are often subjected to demanding overvoltage, overcurrent, dI/dt, and/or dV/dt stresses not found in other applications, which they must withstand without damage or degradation in order for the system to function reliably. Thus, it is possible that non-micropipe SiC crystal defects, which appear relatively benign when subjected to conventional DC characterization methods and used in less-demanding applications, could cause device/system failure when operated in demanding high-power circuits, as historically is the case with silicon-based power devices whose design specifications today are still governed by safe operating area (SOA) reliability considerations. In silicon power electronics experience, undesired nonuniformities in semiconductor properties across the high field region of a power device (sometimes caused by crystal dislocation defects and/or undesired impurity clusters) have historically led to reliability problems (i.e., reduced SOA) in demanding high-power systems, with higher voltage devices being most susceptible to failure [24].

SiC has strong material property advantages that should make it inherently more durable to electrothermal stresses that govern SOA than silicon, such as higher thermal conductivity, higher melting temperature, lower impurity diffusion, etc. It is therefore quite possible that SiC-based high power devices may be able to much-better tolerate the presence of localized currents and crystal defects than silicon power devices. Previous works indicate this is the case for properly fabricated SiC pn junction diodes with voltage ratings of less than 600 V [25-27]. When subjected to reverse-breakdown avalanche energy testing, no significant difference was noted between devices with and without closed-core screw dislocations, apparently due to the fact that space-charge effects restrict the breakdown power density and temperatures at the dislocation-related microplasmas [27]. As of this writing, however, no high power SiC rectifier (V_R > 1 kV, I_{ON} > 10 A) has demonstrated reverse avalanche breakdown energy ratings (normalized to device anode area) significantly (> 2X) above silicon, even though most SiC rectifiers are expected operate in circuits at much higher (> 2X)

power densities than silicon. Most experimental observations of poor SiC breakdown energy appear attributable to edge-related breakdown and other non-optimum device processing issues. However, because microplasma power density and thermal stresses could increase with device blocking voltage, closed core screw dislocations presently cannot be ruled out as a possible cause of low avalanche energy in larger-area kV-class SiC rectifiers. Clearly, more work to better understand the electrophysical properties and SOA ramifications of closed core screw dislocations is warranted.

Conclusion: Because present-day commercial SiC wafers and epilayers contain plenty of non-micropipe crystal defects in densities as high as thousands per cm^2, virtually all multi-amp SiC high voltage devices manufactured in the near term seem guaranteed to contain electrical nonuniformities that could potentially impact SiC high-power device operation. It is therefore critical to understand the impact of these various non-micropipe defects (particularly closed core screw dislocations) on the SOA of various SiC power device structures, as understanding of device SOA is necessary for design of reliable high-power circuits. Significant changes in high-power circuit topologies and device derating and paralleling practices may be required if closed core screw dislocation defects are found to greatly reduce the SOA of SiC-based power devices.

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Performance and Reliability Issues of SiC-Schottky Diodes

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Keywords: Electrical Properties, Failure Mechanisms, Overcurrent Limitations, Reliability, Schottky Diodes

Abstract. The aim of this study is to evaluate the performance of packaged SiC-Schottky diodes under overcurrent conditions and to determine the long term stability and reliability of these devices. For this purpose we used standard test procedures like long term high temperature reverse bias testing and multiple temperature cycling. Contrary to the excellent switching behavior, the SiC-Schottky diodes showed a limited overcurrent capability compared to typical ultrafast Si pn diodes. Destruction of 1 mm^2 devices occurred at $I > 120$ A (10 µs pulse) and $I > 20$ A (10 ms pulse). The corresponding failure mechanisms will be explained. The long term stability of the packaged SiC-Schottky diodes under reverse bias testing conditions was found to be excellent, i. e. no failure occurred during the 1000 h reliability testing of several hundred of these diodes.

Introduction

Silicon Carbide (SiC) Schottky diodes as unipolar devices offer unique ultrafast switching behavior making them extremely attractive for applications requiring blocking voltages ranging from 300 V to 3000 V and switching frequencies higher than 50 kHz. For blocking voltages less than 300 V there is a choice of other unipolar diodes like Si or GaAs Schottky diodes. Above 3000 V most likely SiC-bipolar diodes will be the option with the best overall performance due to their significantly lower leakage current together with a weaker temperature dependence of this property compared to Schottky diodes.

So far, many groups reported on the manufacturing technology and the rectifying behavior of Schottky diodes (for example see [1,2]). On the other hand, information about the reliability of such devices regarding the long term stability, peak current capability, and thermal stress tolerance is still rare. It is the aim of this study to present experimental results on these reliability issues and to show the advantages and disadvantages of SiC Schottky diodes in comparison to classical Si pin diodes.

Experimental

Our Schottky diodes were manufactured on n-type 4H-SiC substrates (micropipe density < 30 cm^{-2}). The n^- epitaxial layers were grown in a multi wafer epi system in our laboratory [3] with doping concentrations of 7 to 8×10^{15} cm^{-3}, and thicknesses of 8 to 9 µm. The diodes are equipped with an Al-implanted bipolar edge termination as described by Mitlehner et al. [4] to prevent premature breakdown due to electrical field crowding at the edge of the Schottky metal. The implanted ions have been activated by a subsequent annealing step at 1500 °C. Ti was used as Schottky metal and Ni (annealed at 980 °C) served as ohmic contact on the rear side of the wafer. Both contact metalisations have been reinforced by a solderable and bondable multiple layer metalisation. The active areas of the Schottky diodes investigated in this study are 1 and 1.5 mm^2, respectively. After a polyimid passivation the diodes were packaged in a standard TO220 housing. Fig. 1 shows a schematic of the diode structure and a packaged diode.

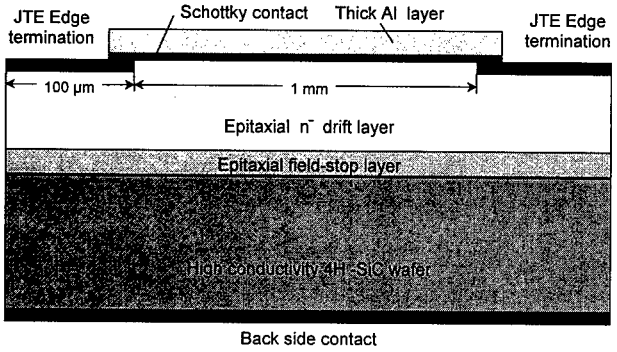

Fig. 1:
Schematic of our SiC Schottky diodes and photography of a packaged diode.

Results

Current-Voltage Characteristics and Yield. The SiC-Schottky diodes build in this study are dedicated to 600 V applications. According to this a reverse leakage current density of 20 $\mu A/mm^2$ was set as yield criterion. To be able to distinct between material related and technology related failures a pretest was done immediately after the epi growth. For this purpose Schottky contacts have been defined on the wafer with the same mask as used for the complete devices but without any edge termination and rear contact. With these simple test structures the rectifying behavior was tested at 100 V. At this voltage level most of the micropipes already cause a reverse failure and a material related yield Y_0 can be derived. For the wafers used in this work this Y_0 value typically was in the range between 60 and 80 % for an active device area of 1.5 mm^2.
The yield of finished devices Y_1 is between 50% and 75%, and the ratio Y_1/Y_0 which is a measure for the yield of the substrate independent process technology is about 90 % in our laboratory. A representative leakage current and yield distribution for the finished device structures on the wafer is displayed in Fig. 2.

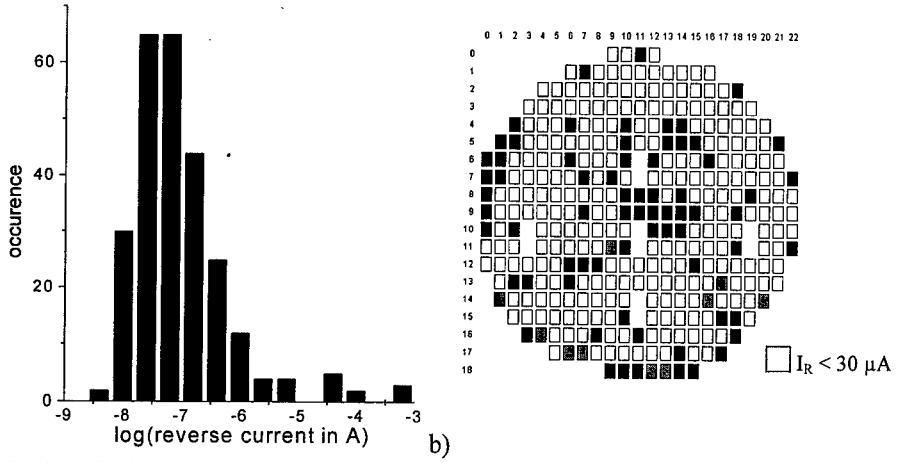

Fig 2: a) Typical leakage current distribution measured on fully processed Schottky diodes on a 35 mm diameter wafer before die sawing and packaging
b) Yield distribution on the wafer. The black and dark gray dies show breakdown or excess leakage current, respectively. The dark cluster in the center of this specific wafer corresponds to a big defective area, visible by the naked eye.

From room temperature (RT) to 275 °C we observed an average increase of the leakage current of packaged devices by a factor of 50. This is much less than expected for current generation only by thermionic emission, but may be explained by a significant contribution of current caused by field emission.

In forward direction (packaged diodes) a differential on-resistance of 0.095 ±0.007 Ω was derived at RT. The barrier of the Schottky metal determined by the forward I/V characteristics is 1.25 to 1.30 eV with an ideality factor between 1.02 and 1.06. This leads to a typical forward voltage drop of 1.5 to 1.6 V at a current of 6 A (400 A/cm^2) at RT. At 275 °C this forward voltage rises to 3.0 to 3.4 V for the same current. From the I/V curves we derived a thermal reduction of the voltage drop across the Schottky junction of 0.3 V and an increase of the total differential resistivity by a factor of 4.5 in this temperature range. This can be well explained with the published data on the temperature dependence of the electron mobility in low doped SiC epitaxial layers ($\mu \approx T^{-(2.0 \text{ to } 2.5)}$, e. g. [5]). The strong temperature dependence of the conductivity is a characteristic feature of unipolar devices, where the T-dependence of the mobility, in contrast to bipolar devices, is the dominating effect.

Switching behavior. As already reported by several other groups [6,7,8] SiC-Schottky diodes show only capacitive switching losses. To be able to carry out a reasonable measurement of the dynamic properties we used 10 diodes (1.5 mm^2 each) in parallel. By this means we derived a Q_{rr} value for a single diode of less than 0.025 µC (switched off from I=4 A to a reverse voltage of 300 V).

Overcurrent stability. In many diode applications short time peak currents may occur occasionally or regularly under certain operating conditions (e. g. capacitor charging). For Si pn diodes the peak current capability is a fixed part of the specification and usually reaches about 2 orders of magnitude higher values than the rated current of the device. On the opposite, there is very little expertise in the literature [9] about this property for SiC diodes.
With a constant forward voltage in the range of 35-75 V applied to our diodes for 10 µs, a current response as displayed in Fig. 3 can be observed : The current reaches a peak value of up to 140 A (1.5 mm^2 diode area; 120 A for 1 mm^2) immediately after the voltage is switched on. After this the current drops significantly towards the end of the voltage pulse. Such pulses have been repeated up to 10^5 times (one second delay from pulse to pulse) without destruction of the device. Contrary, forward voltages in excess of 75 V cause a destruction of the device, mostly during the first pulse. Failure analysis showed, that the destruction occurred in the edge area. Together with the fact, that the critical forward voltage level closely corresponds to the voltage value where the p-type edge termination area is expected to be completely depleted by the field of the Schottky contact, we conclude, that the destruction is caused by an extremely high current density occurring in the edge area after this complete depletion.

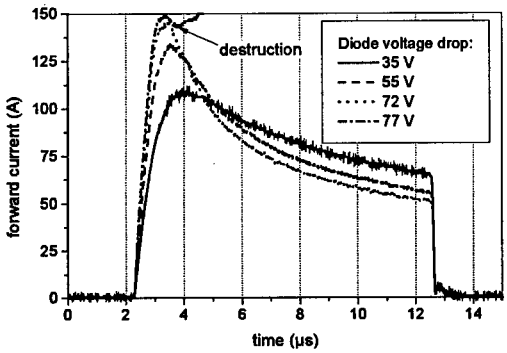

Fig. 3: Current as a function of time for a SiC Schottky diode (10 µs constant forward voltage pulse).

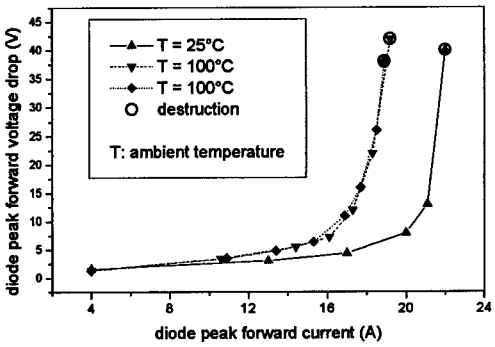

Fig. 4: Peak current vs. peak forward voltage (sine voltage half wave with 10 ms length).

The drastic drop of the current in Fig. 3 is caused by the dissipation of the electrical power in the chip and the strong temperature dependence of the differential on-resistivity of such unipolar devices as described above. From this one can expect a general limitation of the peak current tolerance of SiC Schottky diodes especially for longer lasting current pulses due to a thermal runaway. This was confirmed by other experiments where a voltage sine half wave with 10 ms duration was applied to the Schottky diodes (1 mm^2

active area). The maximum forward current vs. the peak voltage of the sine half wave is given in Fig. 4. Obviously there is a strict limitation of the maximum possible current for the device, depending only on die temperature and voltage pulse length. The positive feedback between dissipated power in the device and increase of resistivity by temperature finally leads to a thermal destruction of the device (melt down of the metalisation). This is a completely different behavior compared to Si pn diodes and has to be taken into account when considering specific applications for such Schottky diodes.

Standard reliability tests. To prove the long term stability of the diodes under high thermal and electrical stress the following tests have been carried out for more than 100 devices for each test:

1. Thermal cycling up to 400°C (without package) ⇒no failure
2. Cycling between –55 and 150°C (1000 times) ⇒no failure
3. high temperature reverse bias testing (150°C, -600V, 1000 h) ⇒no failure (see Fig. 5)
4. high humidity high temperature reverse bias testing (85°C, 85% r. h. , - 80 V, 1000 h) ⇒no failure

These results are very encouraging, because they illustrate that the SiC Schottky diode together with our chosen packaging and passivation scheme is highly stable. On the other hand, as also displayed in Fig. 5, the leakage current shows a significant scatter from one measurement to the next. Even with this scatter, the current values at the end of the test stay below our failure selection criterion of 30 µA for this device type. Nevertheless it will be necessary to understand and reduce this fluctuations in the future.

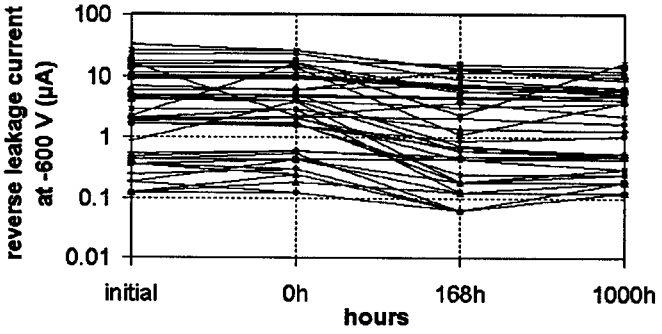

Fig. 5:
Results of high temperature reverse bias testing (150°C, -600 V, 1000h). Between "initial" and "0h" 100 temperature cycles from -55°C to +150°C have been carried out.

Acknowledgement

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Materials Science Forum Vols. 338-342 (2000) pp. 1171-1174

Designing, Physical Simulation and Fabrication of High-Voltage (3.85 kV) 4H-SiC Schottky Rectifiers processed on Hot-Wall and Chimney CVD Films

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Keywords: High-Power Device, Physical Simulations, Schottky Diodes

Abstract: Physical simulation, fabrication and characterization of high-voltage Ni/4H-SiC Schottky rectifiers are studied. We demonstrate a blocking voltage of 3.85 kV by utilizing a 43 μm thick low doped 4H-SiC epilayer in vertical hot-wall Chimney CVD reactor. A high breakdown voltage of 3.56 kV was achieved on a layer grown by conventional hot-wall CVD reactor. The reverse leakage current on CVD sample was as low as 5×10^{-6} A cm^{-2} at 3.5 kV just before the breakdown

Introduction

4H-SiC is considered to be a promising material for high power switching device applications due to its several advantages properties arising from its physical parameters [1]. A simple simulation predicts that high voltage SiC Schottky rectifiers with fast switching and negligible switching loss can realized, revolutionizing in the power device area [2]. In this paper, the physical simulation, fabrication and characterization of high blocking voltage (>3.8 kV) Ni/4H-SiC Schottky rectifiers are presented. Simulations were used to provide insight into the current flow of the diodes and where breakdown first occurs.

Device designing and simulations

Drift-diffusion simulations were performed in order to optimize the device structure using a commercial program Medici, from Avant Corporation. We utilized the most recently published model parameters for 4H-SiC to obtain the closest agreement with the experimental data. The simulations use an anisotropic, field-dependent and doping-dependent mobility. For low-field mobility, the Arora model was used, where the high field mobility is determined with a Caughey-Thomas expression. The simulation also considers incomplete ionization of the donors, bandgap and effective density of state temperature dependence, variations in the intrinsic concentration due to high doping, concentration dependent lifetime, Shockley-Read-Hall and Auger recombination, impact ionization and tunneling, anisotropic permitivity and lattice heating. Physical simulations predict fast switching and negligible switching loss in high voltage 4H-SiC Schottky rectifiers. Thermionic emission and thermionic field emission were shown to be the dominant current transport mechanisms. In addition to this, surface leakage and defects related leakage also occur in real devices.

Device fabrication and characterization

In the diode fabrication we utilized 27-56 μm thick low-doped n-type 4H-SiC-epitaxial layers. These layers were grown using either a horizontal hot-wall chemical vapor deposition (CVD)

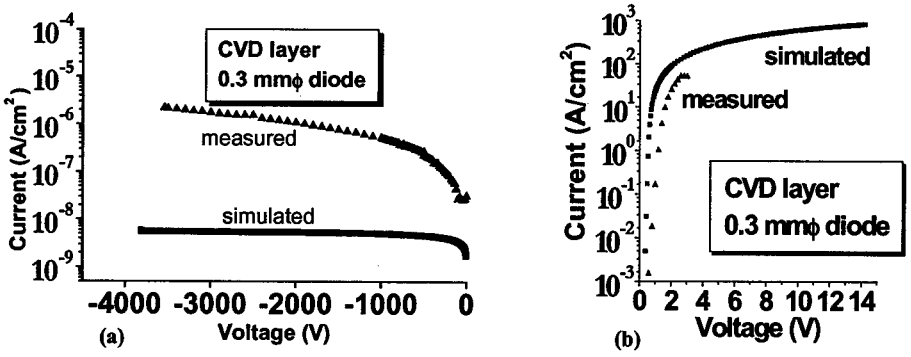

Fig.1 Semilogrithmic plot of current density-voltage characteristics for a simulated and experimentally measured diodes a) in reverse and b) in forward direction.

reactor at 1550 °C or high temperature CVD Chimney technique around ~1780 °C on n-type 8° off 4H-SiC(0001) substrates [3-4]. The Chimney CVD technique is very attractive because thick 40-56 μm layers were grown with increased growth rates of 20-30 μm h^{-1}, which are of interest for thick epilayers used in power devices. By hot-wall CVD epilayers were grown to a thickness of 27 and 35 μm. By Chimney CVD, samples were grown to a thickness 40-44 μm.

The diode structure consists of backside ohmic and front Schottky contact. A metal overlap onto an oxide (SiO_2) layer was utilized as an edge termination. A 2.5 μm thick oxide layer was formed by the combination of dry oxidation and plasma CVD processes. Ni was employed both for ohmic and Schottky contact. Backside contact was annealed at 1000 °C for obtaining an ohmic behavior. Circular diodes of diameters 0.1, 0.3, 0.5 and 1.0 mm were patterned using standard photolithography. Finally a 50-nm thick Au caplayer was deposited on Ni Schottky contact.

Current-Voltage (I-V) characteristics to 1 kV were measured using Keithley 237 source measure unit and breakdown measurement was performed using a 5 kV Bertan power supply together with Kiethley 237. Capacitance-Voltage measurement was performed with HP-4284 LCR meter at a probing frequency of 1 MHz.

Results and discussion

The doping concentrations calculated by $1/C^2$-V plot, measured on 1 mmϕ diode were 7 x 10^{14} and 2 x 10^{15} cm^{-3} for hot wall CVD layers of thickness 27 and 35 μm respectively. The doping concentrations of Chimney CVD samples were in the range of 3–7 x 10^{14} cm^{-3}. The doping was found to increase gradually from one end to other for a 35-mm long substrate piece along the gas flow direction during the growth. The $1/C^2$ *vs* V plot yielded a built-in voltage between 1.3-1.4 V from which barrier heights were estimated to be 1.63, 1.67 for CVD and 1.7 eV for Chimney CVD grown samples respectively.

Figure 1 shows a semi-log plot of current-density *vs* voltage characteristic from both a simulated and measured diode. The measurement results were obtained from a 0.3 mmϕ diode fabricated on a 27 μm thick CVD layer of doping 7 x 10^{14} cm^{-3}. Experimentally the diode blocked a maximum voltage of 3.56 kV, while physical simulations predicted that the breakdown voltage by impact ionization with image force barrier lowering should be 3.85 kV. This experimentally observed breakdown was more than 90% of the voltage obtained by simulations indicating that the MOS field

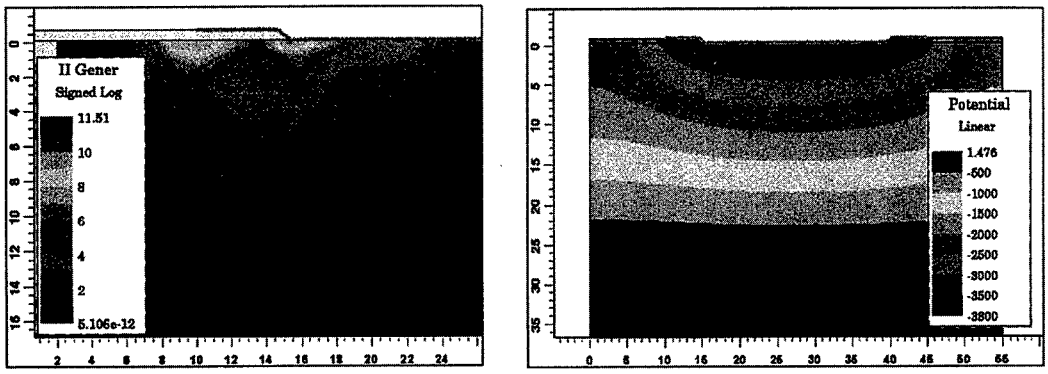

Fig. 2 Simulated picture of the diode a) showing contours of impact ionization at –3800 V b) showing uniform potential distribution at –3800 V.

plate edge termination is active. Figure 2 shows simulated pictures of the diode obtained at 3.80 kV just before the breakdown. Fig. 2a indicates that the impact ionization started at the Ni and SiC edge of the diode, and not under the oxide layer. Figure 2b shows the electric potential at the same bias point indicating an equal distribution without electric field crowding at the periphery of diode. Experimentally a similar feature was observed for the diode, which reached such high breakdown voltage. The second CVD grown sample of thickness 35 μm and doping 2 x 10^{15} cm^{-3} also reached to its breakdown at 3.6 kV.

The reverse leakage current density measured at 1, 2 and 3 kV was 5.2 x 10^{-7}, 1.0 x 10^{-6} and 1.7 x 10^{-6} A cm^{-2} respectively, while the simulated values with image force barrier lowering at the same bias points were in the 10^{-9} A cm^{-2} range. Even though the measured leakage current was three orders of magnitude higher than the simulation (Fig. 1a), however, this value is four orders of magnitude lower than what has been reported earlier [5]. The measured reverse leakage current density just before the breakdown was 5 x 10^{-6} A cm^{-2} and a sharp breakdown was observed.

Fig. 1b depicts the semilogrithmic plots of current-density *vs* voltage characteristics in forward direction both obtained from simulated and measured diode. In the forward direction, I-V curves follow a thermionic emission equation. Theoretically the CVD grown diode should conduct 100 A cm^{-2} at a voltage drop of 2.2 V (Fig. 1b). However, in the calculations, a 100 μm substrate thickness and an ohmic contact resistivity value of 1 x 10^{-6} Ω cm^{-2} was used. The experimentally measured voltage drop on a 0.3 mmϕ diode at a forward current density of 50 A cm^{-2} was 2.5 V (Fig. 1b). The voltage drop at a current density of 100 A cm^{-2} was 3.9 V, which is almost double compared to the value obtained theoretically. The difference could be either due to a poor ohmic contact or presence of a thin interfacial layer between the Schottky metal and semiconductor. The ideality factor was calculated from the initial part of the forward characteristics and a best value was obtained to be 1.05, while the average value was around 1.10. Some diodes that blocked over 3 kV also showed ideality factor as high as 2.0, the reason for this variation is not understood yet. Barrier height calculated by I-V was found to be between 1.2-1.4 eV which is about 0.2-0.4 eV lower than the value obtained by C-V for almost all the measured diodes. This difference could be attributed to the static and effective barrier heights of Ni-4H-SiC Schottky diodes.

I-V measurements were also performed at elevated temperatures to 550 K on a 0.5 mmϕ diode, both in the forward and reverse directions until 1 kV was reached (Fig.3). This shows an increase in the reverse leakage current and an increase in the forward voltage drop. The effective barrier heights as measured by I-V, increased by 0.2 eV with temperature, while the static barrier height assessed by the C-V technique remained the same, a similar behavior was reported in the literature for SiC Schottky diode [6].

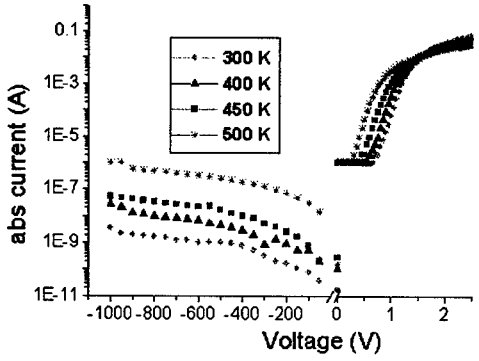

Fig.3 I-V characterstics of 0.5 mmϕ diode measured at different temperature.

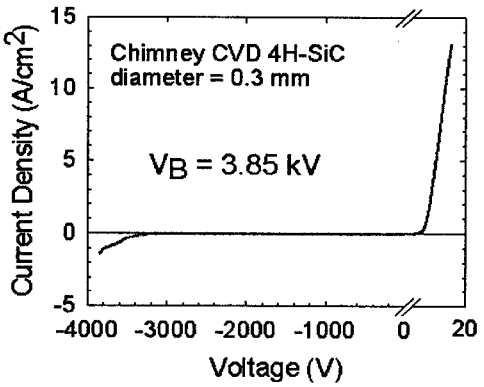

Fig.4 I-V characteristics measured on a 0.3 mmϕ diode processed on Chimney CVD films.

Figure 4 shows current-density *vs* voltage characteristics measured on a 0.3-mmϕ diode made on the layers grown by Chimney CVD. The diode has a breakdown of higher than 3.85 kV. Large diode of 1.0 mmϕ also blocked 2.8 kV. This experimentally obtained breakdown voltage is about 60% of the ideal parallel-plane breakdown voltage without image force barrier lowering. This sample also exhibited extremely low reverse current density of 1.8×10^{-7} A cm^{-2} at 2.2 kV, lower than for any material reported earlier. In the forward direction a voltage drop of 4.4 V was obtained for a current density of 100 A cm^{-2}.

Conclusion

High-voltage Ni/4H-SiC Schottky diodes have been simulated and were fabricated on thick epilayers grown in hot-wall and Chimney CVD reactors. By utilizing a 27 μm thick epilayer, a breakdown voltage of 3.56 kV was achieved which is more than 90% of the theoretical breakdown value. The diode also exhibited extremely low reverse leakage current and an avalanche breakdown was observed for the first time instead of a soft breakdown. Simulation results help us how to design the diode and where the breakdown starts to occur. A record breakdown of 3.85 kV was obtained on a 43 μm-thick 4H-SiC epilayer grown at 20 μm/h rate using Chimney CVD.

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Materials Science Forum Vols. 338-342 (2000) pp. 1175-1178

Influence of Epitaxial Growth and Substrate Induced Defects on the Breakdown of High-voltage 4H-SiC Schottky Diodes

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Keywords: Dislocation, Epitaxial Defects, Schottky Diodes

Abstract: The influence of morphological and structural defects on high-voltage 4H-SiC Schottky diodes was studied. Micropipes were found as severely limiting the breakdown voltage of 4H-SiC power devices, where as carrot-like defects did not influence the value of breakdown voltage. The screw dislocation density as determined by X-ray topography analysis under the active area of the diode was also found to directly affect the breakdown voltage value. Only diodes with low density of screw dislocations and free from micropipes could block 2 kV or higher.

Introduction

Among wide-bandgap semiconductors silicon carbide has reached the highest maturity in terms of reasonable size and thickness of bulk and epi layer growth technologies. Several small-area prototype SiC power devices e.g. junction P-i-N and Schottky diode with record blocking voltage of 6 and 4 kV respectively and 2.8 kV MOSFETs have been fabricated and tested successfully [1-3]. Still, deficiencies in the material quality may increase the time-gap needed to transpose such prototype into field demonstrations. SiC wafers containing high density of crystallographic defects cause premature breakdown in high voltage devices. The *micropipes*, which are voids caused by e.g. giant screw dislocations, are well documented in the literature as severely affecting the power device [4]. A second type of defect, which is found occasionally in some wafers are *inclusions* of either some other polytypes than 4H or other phases such as graphite. Triangular shaped inclusions grown in chemical vapor deposition (CVD) layers are sometimes 3C-SiC [5]. Polishing and etching related defects such as scratches are also considered as surface defect, which could affect the epilayer quality [6]. SiC wafers also contain a high density of screw and edge dislocations, typically in the range of several thousands per square centimeter. When an epitaxial layer is grown by CVD, most of the substrate defects are expected to propagate into the growing film and additional defects may also be introduced or revealed. These are for example "*Carrot*" shaped ditches aligned along the step flow direction with a length around 250 μm for a film thickness of 40 μm (8° off-axis). The origin of this defect in the epi-layer may be related to a perfect screw dislocation pinned at the wafer surface during growth [6]. The dislocation will dissociate into two

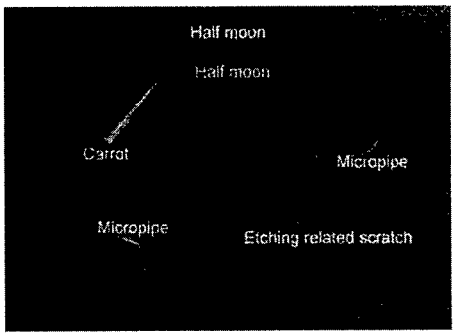

Fig. 1 Morphological defects image 4H-SiC surface obtained by a Nomarski micorscopy.

partials, which will propagate in the basal plane and thus form partial ledges in the film. Any topographical defect on the substrate will disturb the step flow growth of the epitaxial layer. Such obstructions often resemble *half moons* when they are over grown. Crystallites of SiC that has been nucleated elsewhere and then been "falling" down on the growing surface is termed as *down fall*. The shape of some common defects in the substrate and those, which are formed during the epitaxial growth, are illustrated in Fig.1.

Of the various defects, micropipes have been the most studied and are now known to cause premature breakdown failure [7-9]. However, now the micropipes defect densities have steadily been reduced below 1 cm^{-2}. The focus naturally shifts towards other defects such as screw dislocations because of their non-terminating nature of overgrown epilayer, and their densities in the order of thousands per square centimeter have been reported even for epi-layers thickness > 80 μm. Recent studies showed that p-i-n diodes containing screw dislocations exhibit higher pre-breakdown reverse current, display softer breakdown thresholds, and led to the formation of localized filamentary micro channels [10-13]. This study was performed on relatively highly doped (~10^{17} cm^{-3}) and thin epilayer (4 μm) and thus in low breakdown regimes. The morphological defects like carrots and their effect on breakdown can be enhanced when the epi-layer thickness is higher (>20 μm) [10]. In this paper we present our investigations on the premature reverse breakdown of high-voltage Schottky diodes placed on selected defects. In an ideal 4H-SiC Schottky diode, the reverse leakage current is caused by the barrier height which is typically 1 – 1.6 eV and at high electric field regime the image force barrier lowering is more than 0.2 eV. Thus, a slight change in the barrier height due to interface and surface related defects could significantly enhance the reverse leakage current, alter the ionization coefficient and thus lead to pre-avalanche breakdown.

Experiment

Diodes were processed on a low-doped (5 x 10^{15} cm^{-3}), 25 μm-thick, hot-wall CVD grown epi-layer by direct writing technique on top of morphological defects as well as at the defect free areas. Nickel was employed both as ohmic and Schottky contact and a metal overlap onto oxide layer was utilized for edge termination to avoid electric field crowding at the periphery. The diodes were circular shaped, with diameter 1.0 and 0.5 mm. The details of the processing steps and diode structures are described in Ref. [2]. Electrical measurements were carried out with a 2 kV Tektronix curve tracer in SF_6 environment to prevent sparking. A total of 250 diodes were processed on the wafer and analyzed in terms of their breakdown voltage. Theoretically the breakdown voltage due to impact ionization using image force barrier lowering could be around 2.8 kV.

X-ray topographies were taken in the reflection geometry using the Lang's method and Kα Cu laboratory radiation source. Two types of asymmetric reflections were employed, the $(1\bar{1}.8)$ and the (10.10) reflections, respectively, with penetrations depths of the order of 12 and 24 μm. The topographs were taken from the epilayer face after oxidation and diode patterning. The circular diode patterns

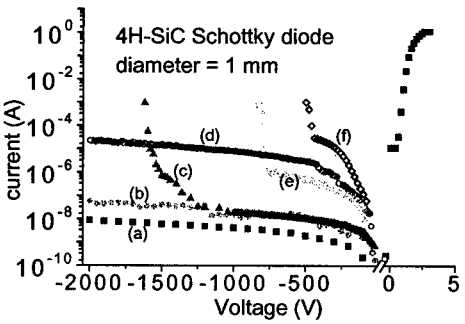

Fig. 2 Semilog plot of current-voltage characterstics of (a) best diode on the chip containing dislocation density around 950 cm^{-2} (b) around 1200 cm^{-2} (c) density between 1500-1650 cm^{-2} (d) diode with a carrot (e) and (f) diodes contain micropipes

could be made visible from the geometrical contrast of the 200-nm-high oxide wall (Figure 3), while screw dislocations are imaged as dots of varying size, relating to their Burger's vector magnitude [14]. Epitaxial defects such as carrots could also be imaged as high contrast stripes, providing, together with micropipes, a post process confirmation of the optical microscope map used for the diode patterning.

Result and discussion

Since micropipes are considered in earlier reports to be performance-limiting defects [7,8], a large number of diodes (120 out of 250) were placed on top of at least one or a combination of micropipes of different diameters. None of the diodes placed over micropipes blocked 2 kV. All of these diodes reached to their breakdown at voltages below 1 kV as shown in Fig.2. Only 27 diodes reached to their breakdown in the voltage range of 500 - 1000 V. A glowing microplasma was observed around the large dimension micropipes when viewed through the microscope. A similar result has been reported in the literature where 80% of the p-i-n diodes (area ~ 1 mm^2) failed below 500 V [7]. The diodes placed on bunch of micropipes and other defects like inclusions of triangles showed a soft breakdown at 100 V and reach absolute reverse leakage current of 1 mA, (a value defined for breakdown in the present study).

Carrot defects (Fig.1) were not found to be harmful to the absolute value of the breakdown voltage in disagreement with an earlier report [10]. Diodes placed on top of such defects sustained high voltage (2 kV in the present measurements). Four diodes were processed on different sizes of carrots. Three of them sustained 2 kV with a degradation of the reverse current. One of the diodes contained two parallel carrots separated by 40 μm from each other reached to its breakdown at 1.8 kV.

Diodes were placed at the morphological defect free areas in order to study the effect of screw dislocations on the reverse current and breakdown. Only 20% of the diodes (21 out of 97) sustained to high voltage of above or equal to 2 kV. Sixteen diodes reached their breakdown between 1.5 - 2.0 kV, 24 diodes reached their breakdown between 500 -1000 V, 23 diodes were failed at or below 500 V. In order to investigate the effect of screw dislocations, X-ray reflection topography analysis was performed on one half of the wafer. The image showed a non homogeneous distribution of screw dislocations. Very high densities of screw dislocations (>2 x 10^4 cm^{-2}) were sometimes observed in regions where several of micropipes were located. It was seen that those diodes that have a low reverse breakdown voltage contain a higher density of dislocations in the active area compared to those which blocked 2 kV or higher. This result is in agreement with Neudeck et.al [12-13] who showed that the pn-diodes containing elementary screw dislocations exhibited 5-35% reduction in breakdown voltage. Dislocations are assumed to create additional states within the bandgap due to atomic strain and internal stress. Trapping of carriers by these states can significantly enhance the electric field locally. Since the ionization rates are nonlinearly dependent on electric field, such changes can dramatically alter the ionization coefficient (α_n, α_p), hence enhance the reverse current, and resulting in breakdown. Moreover, carriers would also prefer to channel by those dislocations that run closest to that direction in which the net current flows in the device [15]. Figure 3a and b shows X-ray reflection topographic images of the two diodes that contain screw dislocations density around 10^4 and 10^3 cm^{-2} respectively. The screw dislocation densities in the active area of the diodes are plotted with their respective breakdown voltage in Fig. 4. It can be seen from this

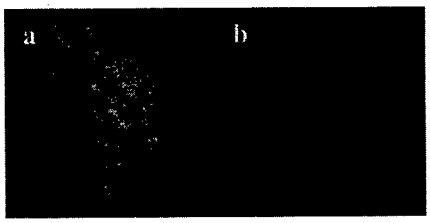

Fig. 3 Reflection X-ray topography image of the Schottky diode showing a) high density of screw dislocations b) diode with low density of screw dislocations corresponding to the I-V curve (a) in Fig. 2

figure that the diodes containing a dislocation density higher than 2000 cm^{-2} reached their breakdown at 400 - 1000 volts.

Diodes with breakdown above 1500 volts contained a dislocation density less than 2000 cm^{-2}. The best value was 950 cm^{-2} and this particular diode exhibited extremely low reverse leakage current as shown in Fig. 2.

In summary, except carrots, all other defects (micropipes, downfalls, triangles and other inclusions) are severely affecting the reverse performance of SiC devices. None of the Schottky diodes placed on micropipes could stand reverse voltage higher than 1000 V. X-ray reflection topography study showed that the local density of screw dislocations also play an important role in the performance of high-voltage SiC devices. This study showed that wafers having areas with screw dislocation density < 1000 cm^{-2} may be desirable for power device application.

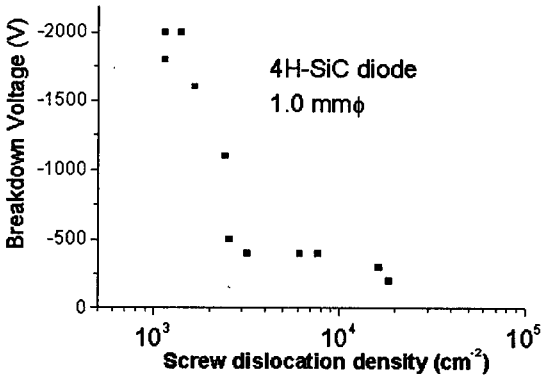

Fig. 4 Semilogrithmic plot of screw dislocation density *vs* breakdown voltage of Schottky diode.

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Materials Science Forum Vols. 338-342 (2000) pp. 1179-1182

A 2.8kV, Forward Drop JBS Diode with Low Leakage

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Keywords: JBS Rectifier, Junction Barrier Schottky, Power Rectifier

Abstract

High voltage Schottky-, Junction Barrier Schottky (JBS)- and PiN-diodes with an implanted JTE termination have been fabricated on the same 4H-SiC wafer. Blocking voltages of 2.5-2.8kV were reached for JBS and PiN diodes while the Schottky diodes reach about 2.0kV. It is shown that the JBS design increases the blocking voltage effectively compared to the Schottky device with less than 10% increase in on-state static lossses. Also, a comparison of static losses to a PiN diode gives a decrease of 40% for the JBS. The leakage current is also lowered by two decades compared to the Schottky device at its blocking voltage. Temperature measurements show that the low leakage current is maintained up to at least 225 °C.

Introduction

The JBS device is a promising rectifier for the medium voltage range since it combines a low forward voltage drop of a Schottky diode with a blocking mechanism similar to that of a PiN diode. The static losses can be much lower than for a PiN as long as the unipolar on-resistance is low enough and the leakage current is lower than for a Schottky diode by keeping the high electric field away from the Schottky contact. Demonstration of JBS devices in 4H-SiC up to 1kV have been reported previously [1,2].

The JBS diode [3,4] is a Schottky structure with a p^+n junction grid integrated into its drift region. In forward conduction the current flows unipolar through the multiple conductive channels under the Schottky contact with a voltage drop determined by the Schottky barrier. In reverse blocking mode the p^+n junctions become reverse biased and the depletion layers spread into the channel and pinch off the Schottky barrier. After pinch-off a potential barrier is formed which limits the electric field at the Schottky contact while the drift region supports further increase in voltage. The spacing between the p^+ regions should be so designed that pinch-off is reached before the electric field at the Schottky contact rises to the point where excessive leakage currents occur due to tunneling currents [5]. Lowering of the leakage current without too much increase in on-resistance can be obtained for the JBS if an optimized p+ grid design is used. This paper presents 4H-SiC JBS diodes in comparison to Schottky and PiN diodes for on-state and reverse blocking as a function of temperature.

Design and experimental

A schematic cross section of the JBS structure is shown in Fig. 1. The p^+n junction grid is characterized by the width of the p^+ regions (**W**) and spacing in between (**S**), i.e., the Schottky area region. These parameters are together with the Schottky barrier and the epilayer doping the

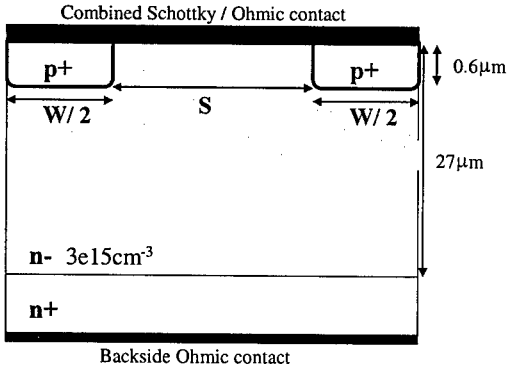

Fig. 1 Schematic cross section (light grey indicates extending depletion region under reverse bias)

Drawn grid design		*% Schottky area*
W	*S*	*S/(S+W)*
3μm	3 μm	50%
3μm	6 μm	67%
3μm	9 μm	75%
3μm	12 μm	80%
6μm	6 μm	50%
6μm	12 μm	67 %
6μm	18 μm	75%

Table 1 Grid design used in the experiment

important design parameters for the tradeoff in forward drop and leakage current. The resulting effective Schottky area should be maximized without too wide grid spacing. To investigate this a striped grid geometry (see Fig. 2) was designed with two different p^+ widths : 3μm or 6μm. The spacing in between is varied so that the active Schottky area ranges from 50% to 80% according to Table 1.

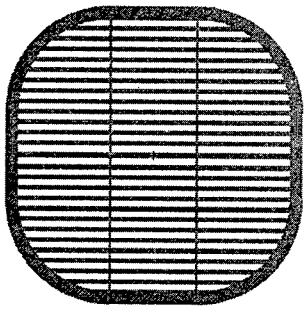

Fig. 2 P^+ grid layout for JBS

JBS and reference Schottky and PiN diodes were processed on the same 4H-SiC n-type substrate with 27μm thick n-epi with a doping of $3e15cm^{-3}$. The epi thickness and doping should give a blocking voltage of 2.7-3.0kV if a critical electric field of 2.0MV/cm is assumed. The theoretical on-resistance of the epi layer is $7m\Omega cm^2$ if an electron mobility of $880cm^2/Vs$ is used [6].The layout contained both JTE- and unterminated devices for device sizes ranging from 20mA up to 1A device currents. After etching alignment marks the JBS grid and PiN emitter were ion implanted with boron and aluminum to a profile depth of 0.6μm. After that a two zone JTE was implanted with different masks and then an implantation anneal was carried out at 1700 °C. The next steps were oxide surface passivation and contact holes patterning. For the backside contact nickel was deposited and annealed at 950 °C and for the frontside Schottky contact (and combined Ohmic contact) titanium was chosen as metal. A 500 °C anneal in vacuum was done to improve the Schottky contact interface while knowing that this anneal would be insufficient for a low resistance Ohmic contact on the implanted areas. After anneal the leakage current was reduced by a factor of 3 for the Schottky diodes and the diode current range, with an ideality factor ≈1.1, increased two decades.

Results and discussion

In Fig. 3 the forward current-voltage characteristics is shown in a) semi-log b) linear scale for a Schottky diode and different JBS designs. The PiN diode is not shown since it has high forward drop due to the insufficient anneal (6-7V at $100A/cm^2$). To calculate the current density the total contact area including both Schottky and p^+ grid areas is used. Typical forward voltage drops for the Schottky diodes are 1.8V. The JBS device with 50% Schottky region has a voltage drop of 2.0V at $100A/cm^2$ with an on-resistance of 7.5 $m\Omega cm^2$. For JBS diodes with increased Schottky

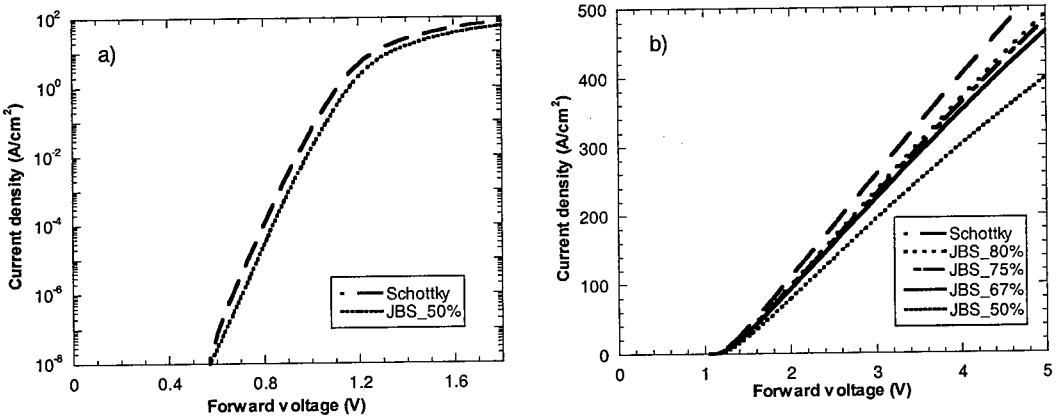

Fig. 3 Forward characteristics of JBS diodes with different grid designs in comparison with a Schottky diode a) semi-log plot of sublinear current b) linear plot of high current characteristics

area the on-resistance decreases to a value of 6.2mΩcm^2 for the 80% JBS device. The Schottky contact voltage drop is characterised by a barrier height of 1.4eV, and an ideality factor of 1.1.

The reverse characteristics up to –500V is shown in Fig. 4. At –500V even the widest spacing of 18μm should be pinched off. It is clear that the leakage current is reduced by the use of a p^+ grid. In Fig. 5 the –500V leakage current versus forward drop at 100A/cm^2 is presented for the different JBS designs, both at 30 °C and 125 °C. For the same Schottky area percentage the forward voltage drop is higher for the design with p^+ width of 3μm than the design with 6μm. This is believed to be a current crowding effect which gives self-heating effects. This is supported by the fact that the effect is even more pronounced for higher temperature, see 125 °C in Fig. 5.

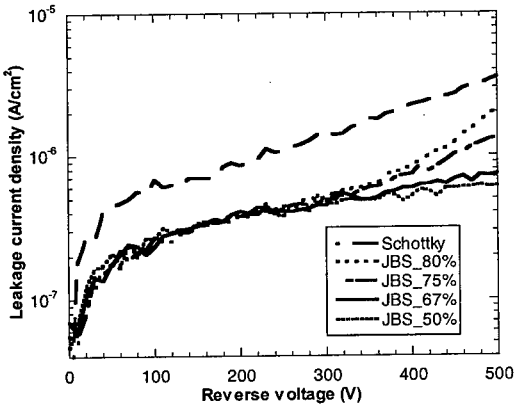

Fig. 4 Reverse characteristics to –500 V of JBS diodes with different grid designs in comparison with a Schottky diode.

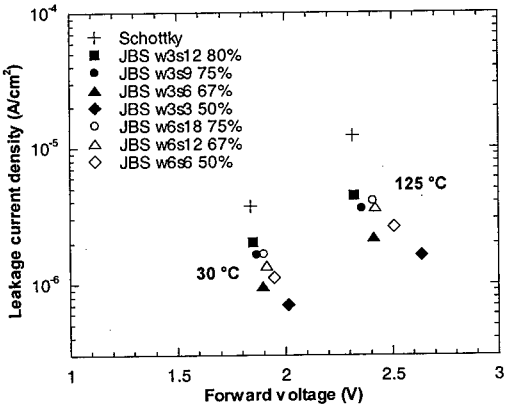

Fig. 5 Leakage current at –500 V versus forward voltage drop at 100 A/cm2 for 30 °C and 125 °C.

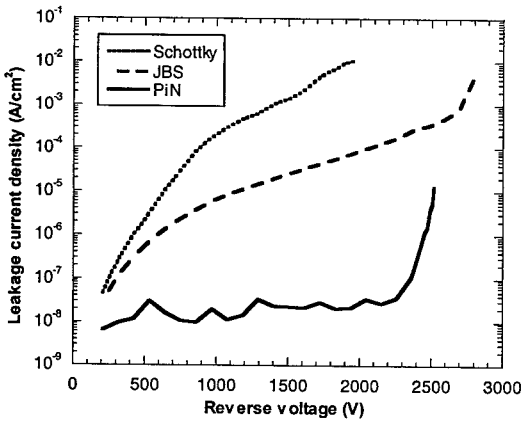

Fig. 6 Reverse characteristics of a 2.8 kV JBS diode at 30 °C compared to a PiN and Schottky diode.

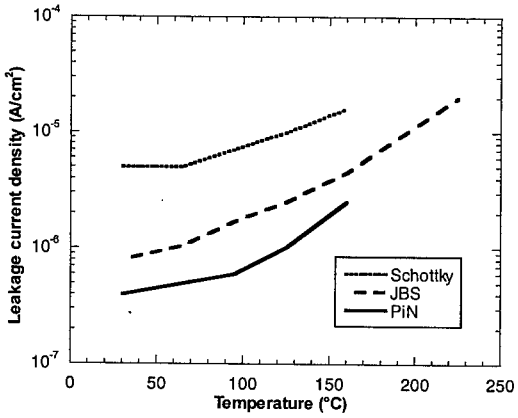

Fig. 7 Temperature dependence for reverse leakage current at –500 V.

Typical blocking characteristics is shown in Fig. 6 for a Schottky, JBS and PiN diode. No Schottky device blocked more than 2kV while several JBS devices blocked 2.5-2.8kV with two decades reduction in leakage current at 2kV compared to the Schottky device. These breakdown voltages are in the theoretical limit of the epi thickness and doping used. Measurements of the leakage current at –500V for different temperatures show that the low leakage current is maintained up to at least 225 °C, see Fig. 7.

Conclusions

Junction Barrier Schottky diodes have been demonstrated with a blocking voltage of 2.8kV and a forward drop of less than 2V at 100A/cm^2. It is shown that the JBS design increases the blocking voltage effectively compared to a Schottky device and that the static losses are 40% lower than for a theoretical PiN diode.

Acknowledgements

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Materials Science Forum Vols. 338-342 (2000) pp. 1183-1186

3.6 kV 4H-SiC JBS Diodes with Low RonS

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Keywords: Junction Barrier Controlled Schottky Diode, pn Diode, Schottky Diodes, Static Induction

Abstract

The new high voltage Junction Barrier controlled Schottky (JBS) diode has been fabricated using 4H-SiC. This diode has some field reduction regions in the active area of a Schottky barrier diode (SBD). These regions can reduce the electric field at the Schottky barrier in the reverse blocking state, and can reduce the leakage current. By adopting the proper SBD metal, fine patterning and optimized structures, we succeeded in improving the trade-off between the blocking voltage (BV) and the specific on-resistance, and realized the highest BV, an excellent low leakage current, and the top level of specific on-resistance. BV at the reverse leakage current density of $10mA/cm^2$, leakage current density at 3kV, and specific on-resistance was 3.6kV, $2mA/cm^2$, and $43m\Omega cm^2$ respectively.

1. Introduction

SiC is expected to enable the realization of power semiconductor devices with performance superior to that of Si power semiconductor devices because of their superior electrical and physical properties. In order to realize the next generation of large capacity power conversion, SiC devices with higher voltage, higher speed and lower loss are desired. Especially, free-wheeling diodes with fast recovery characteristics are expected. By using SiC, high voltage SBDs with fast recovery characteristics and low on-state loss can be expected. Several groups have fabricated 4H-SiC SBD with high voltages of 1.7-3.0kV[1,2], but their leakage currents were very large over the voltage of 1.5kV. To reduce the leakage currents drastically, SiC JBS and MPS (Merged pn/Schottky) diodes were developed [3,4]. In these diodes, electric field reduction regions in the active area of a SBD were formed. These regions can reduce the electric field at the Schottky barrier in the reverse blocking state by using Static Induction phenomena, and can reduce the leakage current. But the BVs of reported JBS and MPS were low (about 1kV), and the trade-off between BV and the specific on-resistance was not good. In this paper, we report improvement of the trade-off and successful realization of the highest BV and good on-state characteristics.

2. Experimental details

A cross-sectional view of a JBS is shown in Fig.1. JBSs were fabricated using 4H-SiC n-type wafers with 30μm and 50μm epitaxial layers from Cree Research Inc. The donor concentration of the epitaxial layer is 1.3-1.8x$10^{15}$$cm^{-3}$. B^+ implanted p regions with a striped pattern are formed in the active area at the period of 10μm. These p regions are expected to reduce the maximum electric field at the Schottky barrier by static induction effect in order to realize high BV and low leakage current. The widths of p regions of fabricated JBSs described as Lp in Fig.1 are 5μm, 7μm and 8μm. Ls is the spacing between the p regions in the active area, and this region acts as a channel region. As the edge-termination to realize high BV, p^+ regions are formed by B^+ implantation. Ni is employed as the SBD metal to realize high BV because it has a higher work function. For comparison with JBSs, SBDs and pn diodes were fabricated. All diodes are 0.3mm x 0.3mm in size.

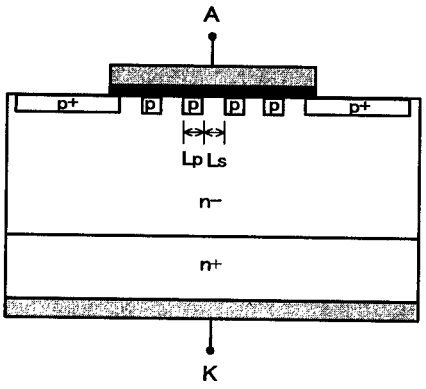

Fig.1: Schematic cross-section of a fabricated JBS.

3. Results and discussion

Fig.2 shows the backward characteristics of diodes with 30μm epi-layer depending on the ratio of the p region in the active area described as Rp. By increasing Rp, the reverse leakage current is reduced. In JBSs (0.5<Rp<1) the leakage current is reduced by more than one order compared with SBD described as Rp=0. P regions formed in the active area can reduce the maximum electric field at the Schottky barrier effectively. The larger Rp is, the larger BV of a JBS at the same leakage current is. Fig.3 shows their forward characteristics. In case of Rp of 0.5, excellent forward characteristics are realized although it is a little bit worse compared with that of SBD. The ideality factors of SBD and JBS (Rp=0.5) are 1.08 and 1.09 respectively. Both JBS(Rp=0.7) and JBS(Rp=0.8) have large built-in potential.
It seems that lightly doped p-type regions are partially or totally formed by the diffusion of B to the surface of the channel region and these regions cause a potential barrier.

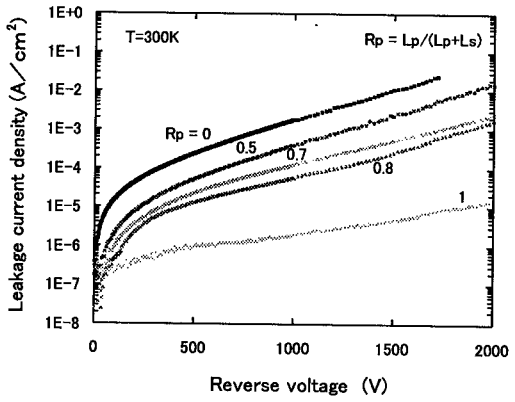

Fig.2: Backward I-V characteristics of a SBD, JBS and pn diode with 30μm epi layer.

Fig.4 shows the dependence of the BV at 10mA/cm^2 and the on-state voltage at 100A/cm^2 on Rp regarding diodes with 30μm epi-layer. By increasing Rp, BVs are higher, and on-state voltages are higher, too. From such relationships, Rp of about 0.5 is suitable for BV and the on-state voltage. Therefore, in diodes with 50μm epi-layer, Rp of 0.5 is adopted. Fig.5 shows its backward and forward characteristics. The backward characteristics are excellent and BV of 3.6kV is achieved. This voltage is a new record among unipolar devices. The leakage current is very low. At 3kV, the reverse leakage current density is 2mA/cm^2 and very low compared with that of SBD (about 2A/cm^2 [2]). The reverse characteristics have been observed without any deterioration repeatedly. Furthermore, low specific on-resistance of 43mΩcm^2 is obtained. On-state voltage at 100A/cm^2 is 6.0V and the ideality factor is 1.24.

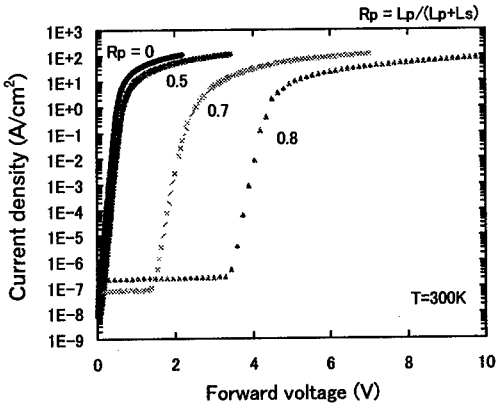

Fig.3: Forward I-V characteristics of a SBD and JBSs with 30μm epi-layer.

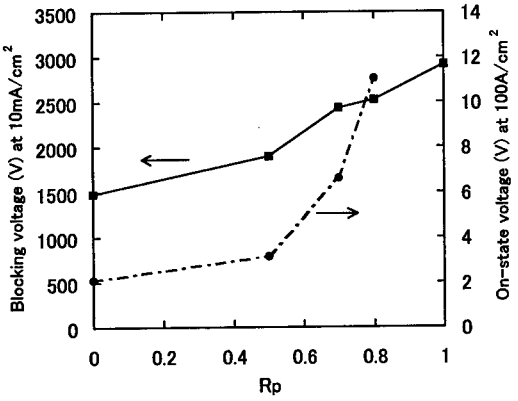

Fig.4: Blocking voltage and on-state voltage depending on the ratio of the p-type region in the active area of a SBD, JBSs and a pn diode with 30μm epi layer.

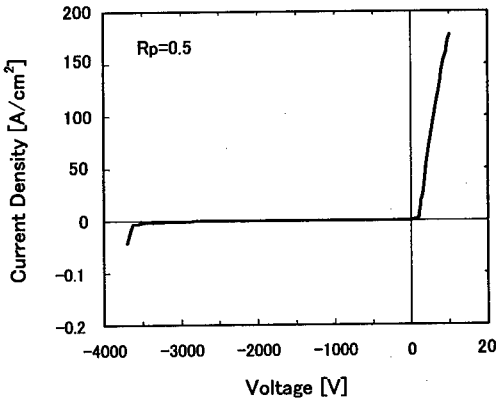

Fig.5: Forward and backward characteristics of a JBS with 50μm epi-layer.

Fig.6 shows the trade-off between BV and the specific on-resistance. BVs of the fabricated JBSs are plotted at the leakage current density of 10mA/cm^2. The trade-off of the fabricated JBS is superior to that of the previous JBS[3] and is nearly the same as those of Kyoto University's[1] and Linköping University's[2]. JBS in this work has the highest BV among unipolar devices and the smallest reverse leakage current density at more than 2kV.

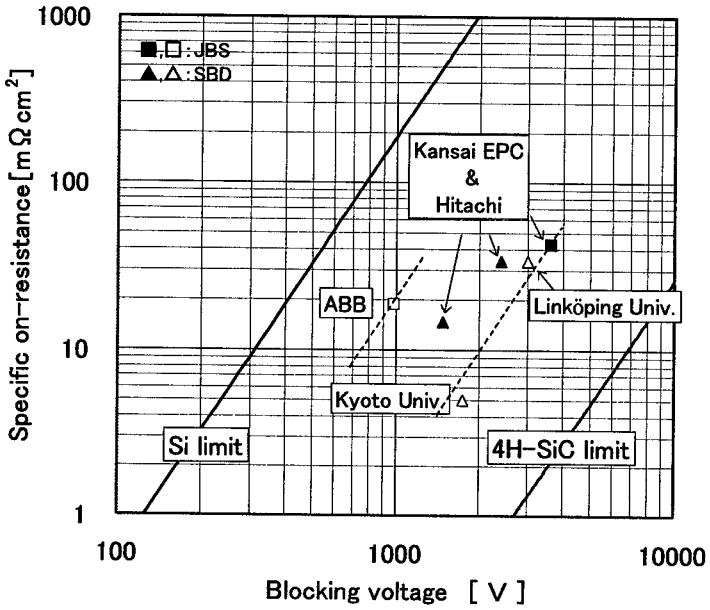

Fig.6: Relationships between specific on-resistances and blocking voltages of SBDs and JBSs.
(this work's data[■: JBS,▲: SBD], reported data [□: JBS,△: SBD])

4. Conclusion

Junction Barrier controlled Schottky (JBS) diodes were fabricated using 4H-SiC and the new BV record of 3.6kV was achieved. P regions formed in the active area of a JBS could improve the trade-off between BV and the specific on-resistance. The specific on-resistance was 43mΩcm^2. In backward characteristics, the reverse leakage current density was very low and was 2mA/cm^2 even at 3kV.

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Materials Science Forum Vols. 338-342 (2000) pp. 1187-1190

Fabrication and Testing of 1,000V-60A 4H-SiC MPS Diodes in an Inductive Half-Bridge Circuit

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Keywords: Inductive Half-Bridge Switching, MPS Diode, Power Diode

Abstract: 4H-SiC merged PiN/Schottky-barrier (MPS) diodes have been modeled and fabricated. DC *I-V* characterization has been done at RT and 255°C. The MPS diodes have shown greatly reduced reverse leakage current density, characteristic of PiN diodes, and unipolar forward properties, characteristic of Schottky-barrier diodes. AC switching in an inductive half-bridge circuit has also been performed to over 60 A.

Introduction: SiC Schottky-barrier diodes (SBDs) are attractive devices for high power switching because of their low conduction and switching losses. However, their leakage current density J_R can be high, especially under high temperatures, largely due to Schottky interface tunnelling and barrier lowering as a result of high electric field in SiC SBDs. One undesirable way to reduce J_R is to design the drift layer with a doping concentration lower than required for a given blocking voltage, which leads to a lower forward current density or a larger forward voltage drop. SiC PN diodes have much lower J_R in comparison to SiC SBDs but their forward turn-on voltage is much larger than that of SiC SBDs and Si PiN diodes. Hence, SiC PiN diodes are attractive only for very high-voltage applications or for high-temperature applications. By merging PN diode and SBD monolithically, as first proposed by Wilamowski [1] for Si and demonstrated by R. Held *et al.* for SiC for 1A-500V switching [2], an MPS diode is formed in such a way that keeps the advantages of both low forward voltage drops of SBDs and low J_R of PN diodes. Besides, as a quasi-unipolar device, when operating in the sub-on-state of the merged PiN structure, the MPS diode is fast and

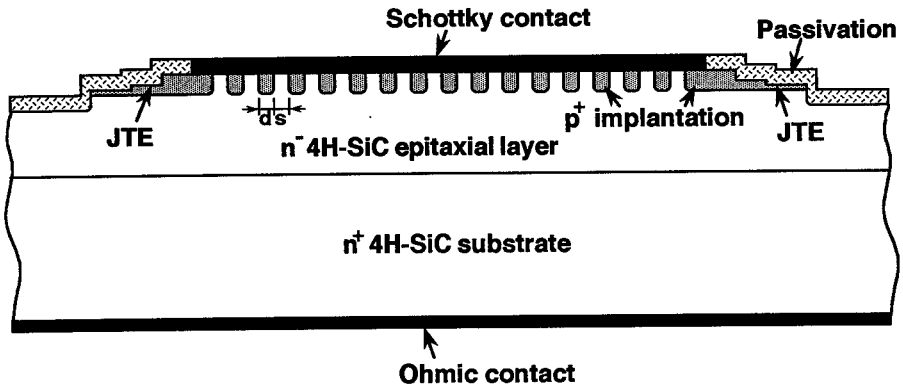

Fig. 1. Cross-sectional view of a fabricated MPS diode.

the associated switching loss is low. As a result of the low J_R dictated by the merged PN-junction reverse characteristics, SiC MPS diodes can also be operated at higher temperatures in comparison to SiC SBDs. This paper reports our first trial in demonstrating 4H-SiC MPS diodes for inductive half-bridge switching applications.

Device Fabrication: Fig. 1 shows the cross-sectional view of a SiC MPS diode with modified junction extension termination (JTE). The 4H-SiC epitaxial wafer purchased from Cree Research, Inc. has a drift layer thickness of 13 μm with a doping concentration of 9.7×10^{15} cm^{-3}. The design of the drift layer was based on an assumed breakdown field strength of 2.4 MV/cm, which would lead to a blocking voltage of 1,580 V, larger than our target of 1,000 V, with a corresponding depletion width of 13 μm. This lower-than-ideal field strength was assumed because large area SiC power devices tend to show substantially reduced field strength. MPS diodes with different p^+ spacings of 1.5, 2, 3, and 4 μm have been modeled and fabricated. Computer modeling results show that over 1,000-V blocking can be achieved if pn junctions close to 1 μm in depth can be formed by ion implantation. For comparison purpose, SBDs and PN diodes with identical designs of the modified JTE have also been included so that each fabrication would produce all three types of diodes on the same chip. Multiple-energy implantation was done to form a box profile of low 10^{18} cm^{-3} of Al and a p^+n-junction depth near 1 μm. Previously established post-implantation annealing conditions [3] were used to activated the Al acceptors. After activation annealing, edge termination was done using modified JTE etched by inductively-coupled plasma, followed by both thermal oxidation and LPCVD SiO_2 deposition for surface passivation. Ni was used both as substrate ohmic contact and front Schottky contact. Al or Au overlayers were then deposited to facilitate 125 μm × 25 μm ribbon bonding.

Characterization: Fig. 2(a) shows the RT and 255°C DC *I-V* curves for a packaged MPS diode with a total diode area of 1.77 mm × 1.77 mm. It is seen that the MPS diode carries a high total current, 13.5 A at 3 V or 19.5 A at 4 V (R_{on} = 6.4 mΩcm^2), while maintaining a low reverse leakage current of less than 10^{-4} A at 1,000 V. The OFF-state power loss is therefore only 0.1 W, even for operation up to 255°C. Fig. 2(b) shows the RT and 255°C DC *I-V* curves for another packaged MPS diode with a total diode area of 3 mm × 3 mm. It is seen that this MPS diode is capable of conducting a DC current of 33 A (366 A/cm^2) at 2.9 V with a reverse leakage current of 1.03×10^{-5} A at 700 V, making the OFF-state power loss negligible when utilized in a 700-V power system.

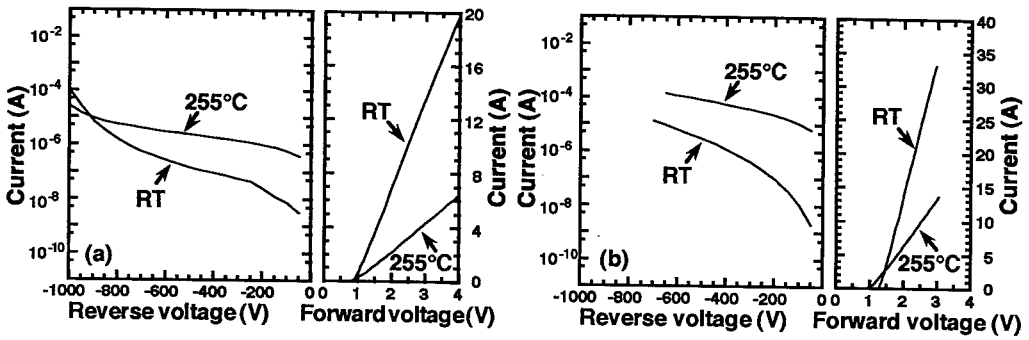

Fig. 2. Room temperature and 255°C DC *I-V* characteristics of (a) a packaged 4H-SiC MPS diode with a total diode area of 1.77 mm × 1.77 mm and (b) a packaged 4H-SiC MPS diode with a total area of 3 mm × 3 mm.

The extrapolated current would be 57 A at 4 V. At 255°C, the total forward current is reduced to 14 A at 3.0 V, which is believed to be largely due to the reduction in electron mobility at high temperature. If the current decrease at 255°C is totally attributed to the temperature dependence of carrier mobility, i.e., $\mu_n \propto T^{-n}$, Fig.2(b) data would suggest an n value equal to 1.44, which is within the expected range. The reverse leakage current is also seen to increase, but is still low enough to be neglected in terms of the resultant power losses in the OFF-state.

Fig. 3(a) shows a comparison of room-temperature reverse leakage current densities for a SBD, a PN diode, and an MPS diode all of 1-mm diameter fabricated on the same chip, as well as SBD data taken from the most recent SBD paper [4]. It is seen that at 500-V reverse bias, our SBD has a J_R of 2×10^{-3} A/cm^2, similar to the results of [4] at 500 V. (The factor of 10 difference is believed to be largely due to our use of a lower drift-layer doping density of 9.7×10^{15} cm^{-3} in comparison to the 1.6×10^{16} cm^{-3} doping density used in [4].) This result suggests that our Schottky-interface quality was largely preserved during the MPS-diode fabrication which included a high-temperature annealing. In comparison to the SBDs, however, the MPS diode shows a substantially lower J_R of 1×10^{-7} A/cm^2 at -500 V, 10,000 times lower in comparison to that of SBD. Even at -1,000 V, J_R is only 2×10^{-4} A/cm^2, corresponding to an OFF-state power loss of only 0.2 W/cm^2. The PN diode (PND) reverse leakage current density is also shown for comparison purpose. It is seen that the MPS has maintained a reverse characteristic similar to that of PND. Fig. 3(b) shows the comparison of reverse leakage current densities for our SBD, MPS and PND as well as the SBD data from [4] all measured at 255°C. Again, the MPS diode shows a much lower reverse leakage current density in comparison to that of SBDs. Note that there is only a very small increase in the reverse leakage current density at -1,000 V, a characteristic very similar to that of the PND shown in the same figure.

Packaged MPS diodes have been evaluated in an inductive half-bridge circuit resembling the inductive motor-control inverter circuit as shown in Fig. 4(a) where Si IGBTs and PiN diode have been used except the upper FWD, which is a 4H-SiC MPS diode. An inductor of L = 1,000 μH was used. Fig. 4(b) shows the switching current and voltage waveforms for an MPS diode with a switched current up to 65 A. Fig. 5 shows the detail of a turn-off switching for the MPS diode biased at -700 V. The switching loss is 1.21 mJ with Q_{rr} equal to 0.985 μC and i_{rr} equal to 3.8 A. Further investigation is underway to minimize packaging related parasitic inductance so that a

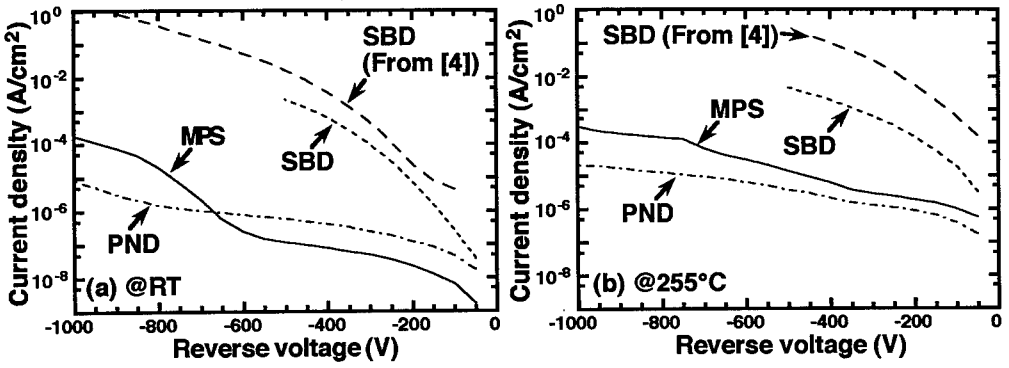

Fig. 3. Comparison of room temperature (a) and 255°C (b) reverse leakage current densities for a SBD, a PN diode, and an MPS diode, all of 1-mm diameter, fabricated on the same chip, as well as SBD data taken from the most recent SBD paper [4].

comparison can be made between the hybrid package of SiC-MPS diode/Si-IGBT and the Si-PiN/Si-IGBT commercial module in terms of switching losses and storage charges.

Acknowledgment: This work was supported in part by TACOM through an SBIR program managed by Dr. T. Burke.

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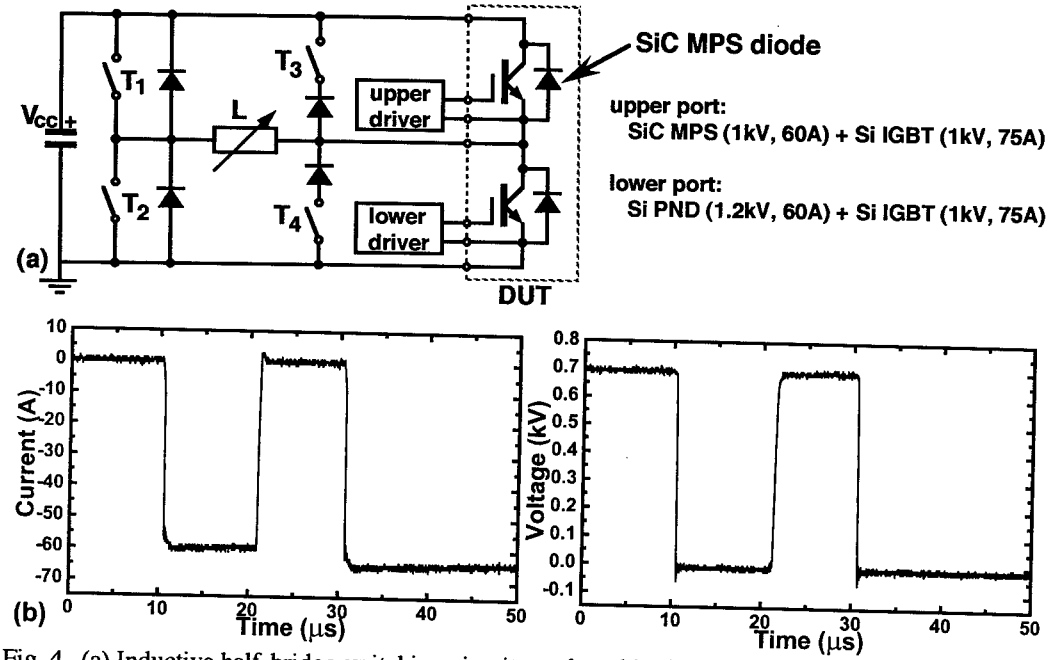

Fig. 4. (a) Inductive half-bridge switching circuit employed in the measurements; (b) the switching current and voltage waveforms for an MPS diode with a switched current up to 65 A.

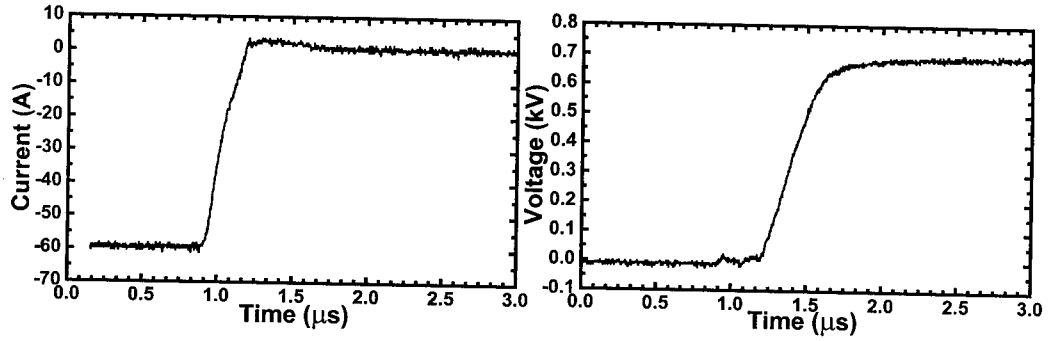

Fig. 5. Detailed 4H-SiC MPS diode turn-off waveforms in the inductive half-bridge circuit showing a switching loss of 1.21 mJ and a Q_{rr} of 0.99 μC.

Materials Science Forum Vols. 338-342 (2000) pp. 1191-1194

Large Contact Ti/4H-SiC Schottky Diodes Fabricated Using Standard Silicon Processing Techniques

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Keywords: Silicon Processing Techniques, Ti Schottky Contact

Abstract: This paper presents electrical characteristics of Ti/4H-SiC Schottky diodes utilizing the same fabrication abilities (procedures, equipment, personnel) used in a silicon fabrication process line. The characterization study includes forward and reverse I-V temperature characteristics together with C-V frequency characteristics. The effect of the temperature and the impact of a post metalization anneal was also investigated. Pre-fabricated surface morphology characterization was also undertaken.

I. Introduction

An important issue for Silicon Carbide processing is the compatibility with standard silicon processing techniques ; the ultimate goal being the transfer of the SiC technology to the existing silicon production line . In this paper, we present results on SiC Schottky diodes fabricated with the minimal number of processing steps required, utilizing standard silicon processing facilities provided in a typical Si process production fab. The electrical characteristics and operational parameters of fabricated diodes are presented. Temperature dependence and the influence of post metalization anneal are also studied. A brief discussion regarding the problems related to the process is given.

II. Experimental Procedure

Commercially available 4H-SiC n type (~5.10^{15} cm^{-3}) 10 μm epi-layer from CREE Research were used in this study Following a solvent clean and later "RCA" cleaning step [1], a PECVD oxide passivation layer was deposited, since the use of such an oxide is very simple from a processing point of view. Titanium was magnetron sputtered on two SiC wafers to a nominal thickness of 2000 Å, to improve probe contact 5000 Å of Al/1%Si was deposited. Large Schottky contacts (2100 x 2100 μm^2) previously designed for Si MPS rectifiers were formed by wet etch definition. No alignment mark were used wherefore the 10 μm metal overlap initially designed could not be ensured. A back ohmic contact was formed by 1 μm of magnetron sputtered Al/1%Si. A 30 min anneal at 500 °C in N_2 flow was performed at the end of the process on one wafer for comparison. Forward and reverse (I-V) characteristics were measured for the Ti Schottky rectifiers, in air by directly probing individual Schottky rectifiers using an HP 4156 parameter analyzer. High voltage reverse I-V characteristics were measured using a computer controlled high-voltage Keithley 75 and were measured at different temperatures using a heated stage. Capacitance-voltage measurements analysis were also performed.

III. Initial Material Characterisation

Surface morphology characterisation was undertaken using a Topometrix Explorer™ AFM operating in non-contact mode using commercially available Si tips to determine large scale surface topography. Images revealed a number of different structures on the wafer, the most predominant

feature being a "nanoisland" like defect (Figure 1) with a typical density of 10-50 per μm^{-2}, 15-50 nm in height and approximate radius of 0.1-0.3 μm.

Identical defects have previously been reported in similar work [2]. It is understood that these "nanoislands" are considered to be small silicon crystallite condensates formed during final stage in epitaxy [3] may be detrimental to devices operation, especially in reverse bias. The standard RCA cleaning process does not eliminate such defects, consequently complications may arise during either oxidation or metalisation processing steps, decreasing the quality of the metal/SiC interface, thus producing poor electrical characteristics.

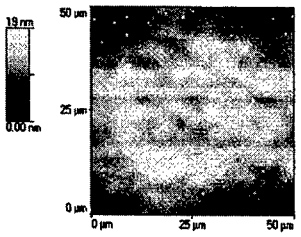

Figure 1 : AFM topography illustrating typical nanoisland defects distributed on as received 4H-SiC epilayer surface.

IV. Measured Forward and Reverse Characteristics

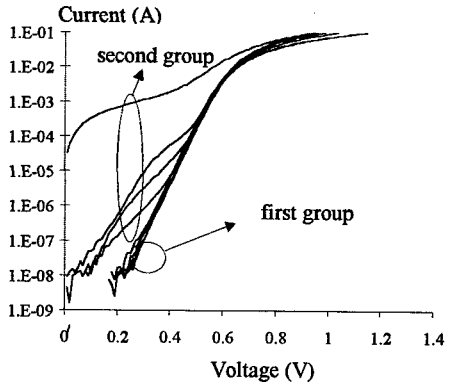

Figure 2 : Forward I-V characteristics of Ti/4H-SiC diodes

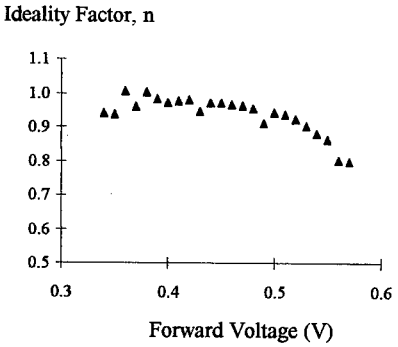

Figure 3 : Ideality profile for one representative device of group 1

Figure 2 shows measured forward I-V characteristics of Ti/4H-SiC Schottky rectifiers at room temperature. We can distinguish primarily two groups of devices. Group one rectifiers showed good agreement with the thermionic current model. An average SBH of 1.04 +- 0.04 V was measured on these devices and an ideality factor near unity for group 1 devices in the limited range of voltage (~0.35-0.55V) were measured (Figure 3). Best devices belonging to group one exhibit a value of 13.4 ohm.cm^2 in terms of specific on-resistance. Group 2 devices show typically a "Two SBH" characteristic profile, this behaviour has been previously reported on Ti Schottky diodes [3] and may be related to defects observed in the section II of this paper. Breakdown voltage values measured for group 1 devices range between 150 and 400 V at room temperature. At -100V, the devices show low leakage current densities, ~ 1 x 10^{-7} A/cm^2 (Figure 4). These results are consistent with previous studies without edge termination. Group 2 devices displayed comparatively poor electrical characteristics, i.e. low breakdown voltage and high leakage

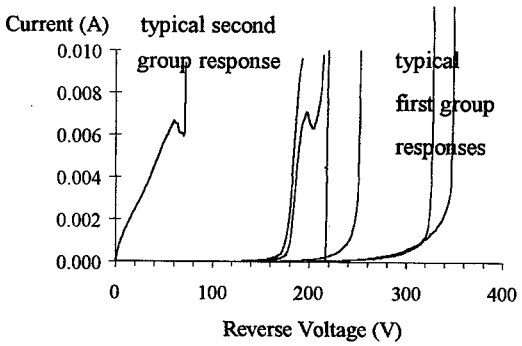

Figure 4 : Reverse I-V characteristics at room temperature for the both group of devices.

current with group 1 devices. All devices which exhibit a non-ideal forward behavior additionally display poor reverse electrical characteristics. At this stage, it is difficult to ascertain whether there exists such a correlation between forward and reverse characteristics. Moreover, in recent studies performed on "two SBH" behaviour, reverse characteristics are not shown [4].

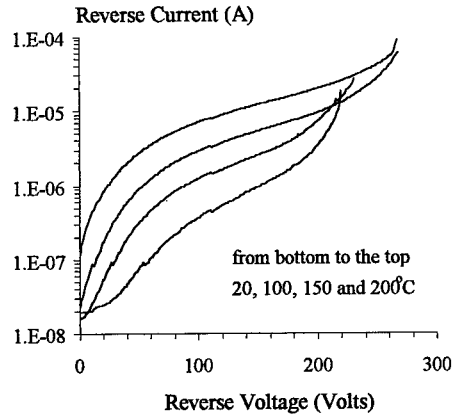

Figure 5 : Influence of the temperature on the reverse characteristic of a Ti/4H-SiC diode of the group 1.

IV. Influence of the Temperature and the Anneal

Group one devices show increased reverse saturation current with increasing temperature, representative for devices dominated by thermionic emission. The on-resistance shows an increasing trend with increasing temperature in agreement with previously reported studies [5,6]. Figure 5 shows that breakdown voltage increases with temperature as expected due to the decrease of the ionization coefficients. Temperature effects for group 2 devices were not examined, given the increase of reverse saturation current.

A post process 500°C N_2 anneal produced consistent effects on device parameters. Group 2 devices showed significantly improved reverse characteristics and leakage current after the anneal (figure 6). Group 1 devices with low leakage current before anneal also decrease by a factor of 100 at -100V. An increase in barrier heights was observed as expected [6], however, the ideality factor and the on-resistance showed a substantial increase. The impact of the anneal is beneficial, except in terms of on-resistance. This could be due to pre-metal clean deficiency and/or the sputtering process procedure.

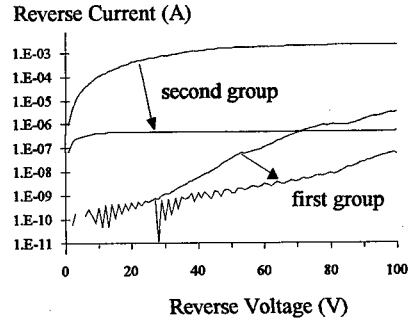

Figure 6 : Improvement of reverse characteristics between 0 and -100V of one device of each group after the anneal.

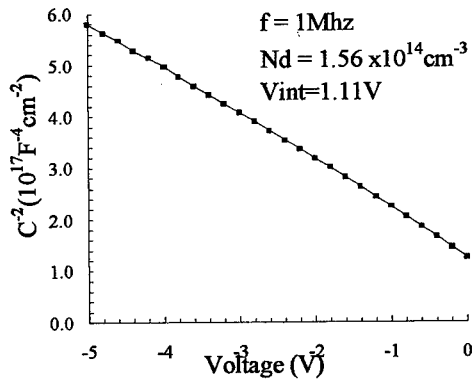

Figure 7 : $1/C^2$ vs. Reverse bias plot for Ti/4H-SiC of the group one device.

V. C(V) measurements

C(V) measurements were performed on devices of group one devices in order to confirm the extracted barrier height value as well as the doping level of the epi-layer (Figure 7). Measurements were found to vary with frequency which may be due to the high series resistance observed. Barrier heights deduced at 1Mhz are consistent with previous studies [5]. Donor concentration was found from the slope of the plot to be ~ 2.10^{14} cm^{-3} differing from the documented value given by CREE Research

(~5.10^{15}cm-3). However, this difference could be consistent with the fact that the specific on-resistance is 10 times higher that expected. and this fact induces an earlier roll-off in comparison with previous studies on similar device [4,6]. Consequently, group one devices have approximately six decades of linearity at room temperature with typical current density of only 4.23 A/cm^2 at 1.3 V.

VI. Problems related to the use of a standard silicon process production fab.

Even with such a basic process i.e. a two mask set, many problems were encountered during the fabrication process particularly mechanical handling issues related to the small size of the SiC wafer. The process line used is typically designed for 4 inch silicon wafers and required extensive modification to accommodate small samples, e.g. design of specific holder for the metal magnetron sputter machine, adaptation of the mask aligner and batch holder. Often, these adaptations increase the risk of damaging SiC wafers used.

Problems also arise given the restriction on SiC test wafers due to the high financial cost involved, this means that the procedure of testing different possible recipes (short-loop) is severely restricted. Short-loop procedures used for 4 inch Si wafers also differ from SiC processing such as oxidation and metal reliability which can reduce the reliability of SiC processing.

Moreover, the process engineers inherently think in terms of silicon technology. This fact does not facilitate good process management, especially since one engineer is generally specialized for a particular step of process. Finally, the test conditions of the devices were not optimized for this kind of material and some substantial adaptation are required before to use a daily test lab equipment.

VII. Conclusion

In a long-term objective of transfer technology, the principal aim of this study was to fabricate a two mask process 4H-SiC Schottky rectifiers closely following classical silicon processing procedures and materials through a typical Si production fab. This study shows that standard silicon IC processing techniques including cleaning, sputtering, PECVD and furnace anneals could be use in producing Ti/4H-SiC Schottky for power applications. However, even if the process done was theoretically simple a strong effort in terms of equipment modification, personnel adaptation and parallel electrical investigative work is required in order to achieve good quality devices

Acknowledgments

The authors want to strongly thank the managers Brendan O'Neill and Julie Donnely of the NMRC silicon fabrication group for their support.

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Optical Beam Induced Current Analysis of High-Voltage 4H-SiC Schottky Rectifiers

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Keywords: KOH Etching, Leakage Current, OBIC Images, Schottky Rectifiers

Abstract The optical beam induced current(OBIC) analysis of 4H-SiC Schottky rectifiers is presented. Many bright spots in OBIC images are observed beneath Schottky electrodes with high reverse leakage currents more than 10^{-5}A/cm^2 at -400V. Forward current density-voltage characteristics are measured, the Schottky rectifiers with high leakage currents show forward excess currents at low voltage level. The excess current is considered to be due to the lower Schottky barrier height at the bright spots of OBIC. It appears that the bright spots of OBIC are not due to the screw dislocations, because the relationship between the bright spots of OBIC and etch pits by molten KOH etching can not be obtained. Finally, the origin of the bright spots of OBIC is considered.

Introduction

Recently, it has been required to reduce on-resistance in power devices. Since the on-resistance becomes close to the theoretical limits in silicon power devices, new materials with the properties superior to silicon have been expected. 4H-SiC is one of the promising materials because of its high critical electric field of 3×10^6V/cm which is one order of magnitude higher than that of silicon. 4H-SiC Schottky rectifiers are expected as substitutions for silicon pin diodes because of the lower reverse recovery currents with same breakdown voltage[1]. However, the leakage current density of each Schottky rectifier was distributed over a wide range from 10^{-7}A/cm^2 to more than 0.1A/cm^2 in our measurement. Since higher leakage currents result in the power loss, it has been desired to control the reverse leakage current close to the theoretical value.

In this paper, fabrication and characterization of high-voltage 4H-SiC Schottky rectifiers with guard ring structures are presented. Optical beam induced current (OBIC) analysis, surface observation and current density-voltage measurements are performed to investigate the cause of the high leakage currents.

Device fabrication and measurement techniques

The cross sectional structure of a Schottky rectifier is shown in Fig.1. 8°off angled n-type 4H-SiC wafers were supplied by Cree Research. At first, guard rings were formed by Al^+ or B^+ implantation. Then backside Ni ohmic contact with a circular window was formed. During backside OBIC measurements, laser beam was irradiated through this window. Finally, Ni Schottky metal was sputtered on (0001)Si face cleaned by sacrificed oxidation and BHF etching. The wafer was annealed at 200°C for 5 minutes.

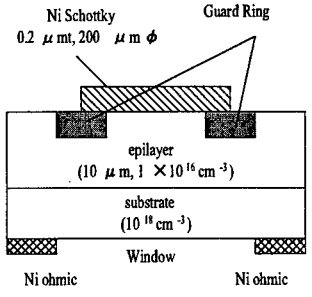

Fig.1 The cross sectional structure of a Schottky rectifier.

Current density-voltage characteristics of Schottky

rectifiers were measured by HP4142B modular DC source / monitor at room temperature. OBIC measurements were performed by a digital OBIC scanner, JEOL DOB-13, with a digital scanning laser microscope, JDLM-6601. Molten KOH etching was carried out at 500°C for 2 minutes to visualize the surface defects. The surface was observed by optical microscopy and scanning electron microscopy(SEM).

The principle and the measurement system of OBIC

When a scanning laser beam is irradiated the semiconductor, of which the bandgap energy is lower than that of laser, electron-hole(e-h) pairs are generated. When the electric field is not applied, e-h pairs disappear by the recombination process within Debye length. If electric field is generated by the depletion layer and defects, electrons and holes in that region drift each direction. This drift current can be detected as OBIC signals.

The OBIC measurement system is schematically shown in Fig.2. He-Ne laser (632.8nm(1.96eV), 0.6mW) is used as excitation light. Although the energy of the laser is lower than the bandgap energy of 4H-SiC(3.25eV), OBIC images could be obtained. Electrons may be excited to the conduction band via the deep level in the bandgap. Very low minimum detective value of the OBIC amplifier (40pA) may also contribute to successful OBIC images.

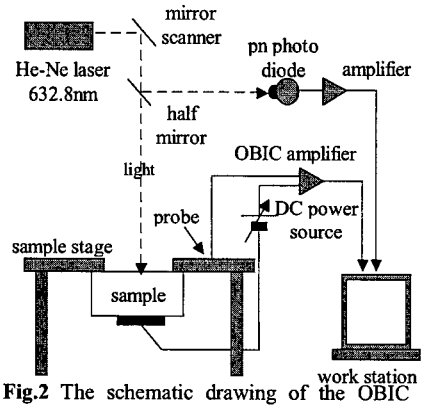

Fig.2 The schematic drawing of the OBIC measurement system.

All OBIC measurements were performed at zero bias. At zero bias, the width of the depletion layer spreads about 0.5 μ m from the metal-semiconductor interface. At the magnification of 1800, the focused beam diameter and the depth of the focus were 0.1 μ m and 0.27 μ m, respectively. The focus position can be moved with a step of 0.1 μ m.

Results and discussion

OBIC images are shown in Fig.3(a),(b). A laser beam was irradiated on (0001)Si face. Since the laser beam was blocked by the Schottky electrodes, OBIC signals could not be obtained in the dark circular regions in Fig.3(a),(b). The bright lines in the dark circular regions are the scratches by the probe. The large bright circumferences show the edge of the guard rings. A bright spot pointed in Fig.3(a) was observed in the guard ring, and this electrode showed a high leakage current density. On the contrary, the rectifier with a low leakage current had no bright spots in the guard ring as shown in Fig.3(b). However, even if there are no bright spots in the guard ring, some Schottky electrodes showed high leakage current density. In these cases, bright spots were considered to be hidden by the Schottky electrodes.

In Fig.3(a),(b), bright and dark regions in the guard ring could be seen on the right and left side of the Schottky electrode, respectively. During reverse current density-voltage measure-

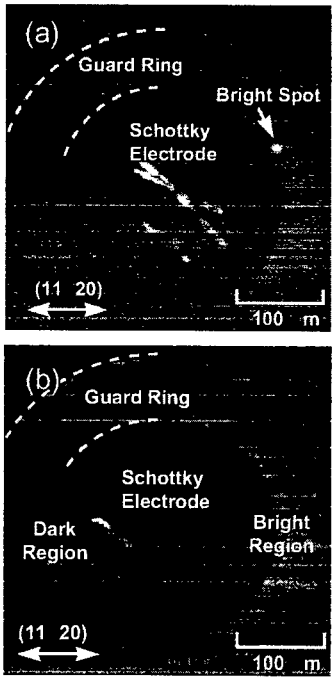

Fig.3 The OBIC images on (0001) Si face. An electrode with a high leakage current(a), an electrode with a low leakage current(b).

ments, the sparkling points by the avalanche breakdown were observed along the edge of the guard ring in the range of high reverse voltage. First the sparkling points generated on the left side of the Schottky electrode, where corresponded to the dark region in OBIC images, then they spread gradually to the right with the increase of applied voltage. This phenomenon was independent of the probe position in the electrode, the direction of the wafer, device structures and the device position in the wafer, however, the mechanism has not been clarified.

In order to obtain OBIC images beneath the Schottky electrodes, the laser beam was irradiated through the backside of the wafer. OBIC images from the backside are shown in Fig.4(a),(b). Many bright spots were observed beneath the electrodes with high leakage currents, while no bright spots were observed beneath the electrodes with low leakage currents. From this fact, it appears that the reverse leakage currents flow at the bright spots in OBIC images when the leakage current is high. There were 10 to 100 bright spots in the high leakage 10^{-2}A/cm^2 (at -400V) electrodes. The OBIC signals of the bright spots were strongest at the metal-semiconductor interface, and the intensity gradually reduced as the focus position is moved from the interface into the bulk. Therefore, the bright spots are probably located at the metal-semiconductor interface.

After the OBIC measurements, the Ni Schottky metal was removed and the wafers were etched in molten KOH. The OBIC image and the optical microscopic photograph of the same area after KOH etching are shown in Fig.5(a),(b). Several etch pits due to the screw dislocations appeared in Fig5(b). However, there was no relationship between the bright spots in OBIC images and the etch pits. This result may be justified by the report which mentioned that the reverse leakage current did not increase even if there are some screw dislocations within the pn diode[2]. Further investigation of the surface has been done by SEM to find other defects related to the bright spots, however, any defects could not be recognized as yet.

Current density-voltage characteristics of Schottky rectifiers with a low and a high leakage current are shown in Fig.6. There is an excess current at low forward voltage level when the leakage current is high,

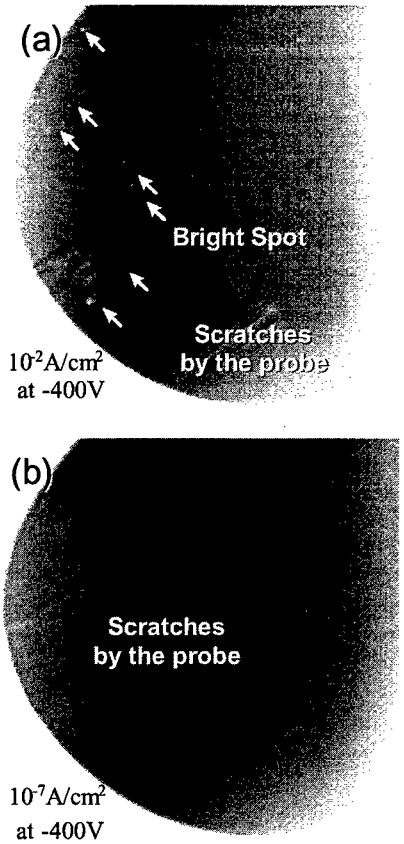

Fig.4 The OBIC images from the backside of the wafer. The electrode with a high leakage current(a), the electrode with a low leakage current(b).

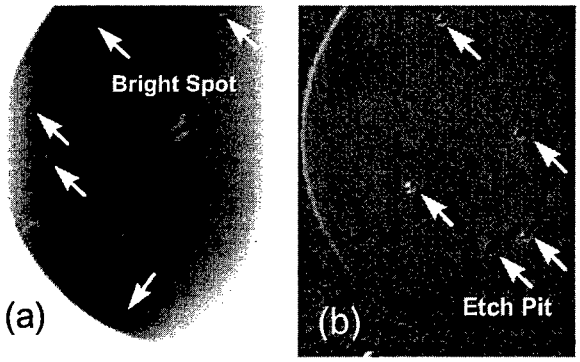

Fig.5 The correlation between the OBIC image(a) and the photograph by optical microscopy in the same area(b).

whereas no forward excess current has appeared in the case of a low reverse leakage current electrode. The forward excess current at low voltage level increased with the rise of the reverse leakage current. This excess current has been discussed in many reports, and they attributed the forward excess current to partial reduction of Schottky barrier height within the electrode[3][4].

Since the electrodes with high leakage currents had the bright spots of OBIC and showed the lower Schottky barrier height suggested by the forward excess currents, it appears that the Schottky barrier height reduction, which causes the high leakage current, occurs at the bright spots of OBIC. However, the causes of the bright spots of OBIC and the low Schottky barrier height have not been clarified yet. Since the bright spots of OBIC were located near the interface of the Schottky contact, these phenomena may be explained by the disorder of the SiC surface. If there is the disorder of the SiC surface, the interface state density will be high. Then more excited carriers will generate via the interface state level during OBIC measurements and result in the bright spots of OBIC. The high interface state density will also cause the Fermi level pinning. Since Ni Schottky metal has a high metal work function of 5.2eV, the Schottky barrier height will be reduced by the Fermi level pinning.

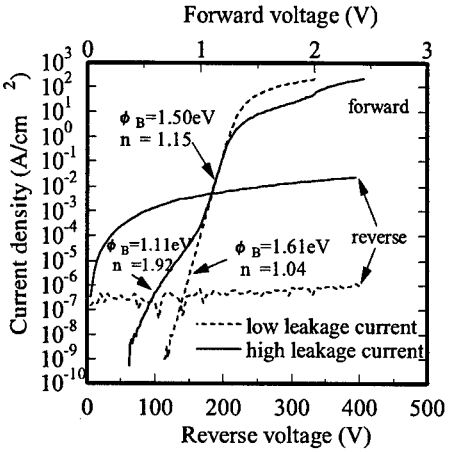

Fig.6 Current density-voltage characteristics of Schottky rectifiers with a low leakage current and a high leakage current.

Conclusions

The cause of high leakage currents was investigated. The OBIC images of the metal-semiconductor interface revealed that there were many bright spots within the Schottky electrodes with high leakage currents. The excess forward current at low voltage level could be obtained in the Schottky electrodes with high leakage currents. It is considered that there is barrier height reduction at the bright spots of OBIC. However, there was no correlation between the bright spots of OBIC and etch pits generated after KOH etching.

Acknowledgments

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Effect of Plasma Etching and Sacrificial Oxidation on 4H-SiC Schottky Barrier Diodes

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Keywords: Electrical Characterisation, Reactive Ion Etching, Sacrificial Oxidation, Schottky Barrier Diode, XPS

Abstract: In devices such as recess gate MESFETs and in SITs, the Schottky gate is formed on a plasma etched surface. The quality of this interface is crucial to the performance of these devices. This study considers sacrificial oxidation as a post-etch, pre-metallisation treatment for SiC Schottky diodes. Current-voltage and X-ray Photoelectron Spectroscopy measurements are used to determine the effect of two different sacrificial oxidation methods on plasma etched and unetched n-type 4H-SiC.

Introduction: The electrical performance of a Schottky barrier diode strongly depends on the quality of the metal contact-semiconductor interface, which in turn largely depends on the preparation of the semiconductor before metallisation[1]. Surface roughness, contaminants or the presence of an interfacial oxide can lead to the creation of electrically active defects, increased contact resistivity, barrier height lowering and poor contact adhesion[2].

The preparation of the material surface is a major issue in SiC devices such as recess gate MESFETs and in static induction transistors (SITs) where the Schottky diode is formed on an etched surface[3]. Plasma etching, (also referred to as reactive ion etching, RIE) has the advantage of high etch rate and high degree of etching anisotropy[4]. However, conventional plasma etching can result in surface contamination, carbon rich and rough surfaces which are detrimental to the electrical characteristics of the diodes[5]. The extent of this etch induced damage can be minimised by altering the parameters of the etch [4] or by altering the source of excitation [6, 7]. An alternative method to reduce etch induced damage is to improve the surface of the material after etching using sacrificial oxidation [8]. Sacrificial oxidation has shown an improvement in both diode ideality and the surface roughness of both the etched and unetched material[9].

This study compares two sacrificial oxidation methods on reactive ion etched and unetched n-type 4H-SiC. The surface treatments discussed are a HF etched thermally oxidised surface, a HF etched densified deposited oxide and a standard solvent clean for reference. X-ray photoelectron spectroscopy (XPS) was used to determine the chemical composition of the surface and current-voltage (I-V) characteristics of Ni Schottky diodes deposited on these surfaces are presented.

Experimental Procedure: Two sets of samples were simultaneously prepared for this study. The first set of samples was fabricated for electrical characterisation using an n-type epitaxial wafer (N_D=2.1x10^{17}cm^{-3}, 5μm thick). The second set of samples was prepared using a bulk n-type (N_D=6.5x10^{18}cm^{-3}) 4H-SiC wafer and was to be used for XPS of the prepared surfaces, with back contact and Schottky gate processing omitted. It was deemed an unnecessary expense to use epitaxial material for materials characterisation.
The epitaxial wafer was cut into sections and then each section was half-masked using thick resist. The samples were then mounted on Si carrier wafers using high temperature wax and reactive ion etched for 60 minutes using CF_4. This resulted in the removal of approximately 0.5μm of SiC from the unmasked areas of the samples. The samples were removed from the carrier wafers and cleaned in trichloroethane, warm acetone, and warm propan-2-ol. One section was thermally oxidised in a steam ambient and the oxide on the back face was removed in dilute HF. 1000Å of Ni was deposited on the highly doped backside of all the epitaxial wafer

sections and was vacuum alloyed at 1000°C to form a large area Ohmic contact. The processing schedule for each sample is summarised below:

Table 1. Summary of preparation treatments used.

SAMPLE	SET 1 Samples for Electrical Characterisation	SET 2 Samples for XPS
1	RIE (half masked), Ni Ohmic deposition/anneal, solvent/water clean.	RIE, solvent/water clean.
2	RIE (half masked), 1100°C 12hour wet oxidation, 10:1 water:HF back oxide strip, Ni Ohmic deposition/anneal, 10:1 water:HF front oxide strip,	RIE (half masked), 1100°C 12hour wet oxidation, 10:1 water:HF oxide strip,
3	RIE (half masked), deposit 0.5μm PECVD oxide, back oxide strip, Ni Ohmic deposition/anneal, 10:1 water:HF oxide strip.	RIE (half masked), deposit 0.5μm PECVD oxide,1000°C 60 sec anneal in vacuum, 10:1 water:HF oxide strip.

The samples prepared for electrical characterisation were then patterned using standard photolithography and 1000Å of Ni was deposited using an electron beam evaporator to form Schottky contacts. I-V and C-V measurements were used to characterise the samples.

XPS Results: XPS was used to determine the surface chemical composition of the as-received epitaxial wafer and processed bulk wafers. This was performed at take-off angles of 15° and 75° to the surface normal, giving different X-ray penetration depths and hence surface sensitivities. Results are given in Table 2. The ratio of the 75° to the 15° XPS peak areas gave a measure of relative depth, the higher the value, the larger the surface contribution. The surface elemental composition, expressed as atomic % of each species within the exponential decay depth sampled by XPS at 15°, was calculated by applying published relative sensitivity factors[10].

Table 2. XPS results for the three surface preparations after RIE etching

Layer	**Species**	**Epitaxial wafer**		**(1) RIE Etched**		**(2) SacOx**		**(3) SacDepOx**	
		Atomic %	**Ratio 75°/15°**	**Atomic %**	**Ratio 75°/15°**	**Atomic %**	**Ratio 75°/15°**	**Atomic %**	**Ratio 75°/15°**
Surface contamination layer	F_B	-	-	12	0.8	-	-	-	-
	C_F	-	-	2	2.9	-	-	-	-
	C_C	9	1.5	4	2.4	11	1.0	16	1.4
Oxide layer	**O**	8	1.1	9	0.6	10	0.9	11	0.6
	Si_O	-	-	5	0.3	-	-	-	-
	F_A	0.5	1.0	5	0.3	-	-	0.5	0.6
SiC substrate	Si_C	44	0.5	25	0.3	38	0.5	32	0.2
	C_{Si}	39	0.4	36	0.2	41	0.4	40	0.1

The identified XPS peaks have been assigned to particular chemical species by comparison with published binding energies and chemical shifts[11], with the table arranged in rough order of increasing depth. On sample (1), fluorine was observed at 2 binding energies of 685.4 (F_A) and 687.2 (F_B) eV. F_B was assigned to a surface fluorocarbon species and F_A was possibly underlying oxyfluoride (SiOF). Several C_{1S} peaks were identified. The 282.4eV peak could be clearly assigned to C in SiC (C_{Si}), whereas the peak at 283.7-284.6eV could have many origins (C-C, C-O, Si-C-O) and is simply labelled C_C. Strongly shifted peaks at 287.7-292.5eV were assigned to fluorocarbon (C_F). Two Si_{2p} peaks were resolved. That at 100.4eV was assigned to Si in SiC (Si_C) with a shifted peak at 101.7 to 102.7eV corresponding to increasing Si-O coordination number (Si_O). Only a single O_{1s} peak was observed, at 532eV.

Results from the epitaxial wafer are consistent with a thin surface oxide and some overlying carbonaceous contamination. RIE treatment (sample (1)) produced a fluorocarbon contamination layer which survived solvent cleaning, but was completely removed by oxidising or thermal treatments in the SacOx and SacDepOx procedures. Surface oxygen and carbon levels remaining after both SacOx and SacDepOx processes ((2) and (3)) could be due to incomplete removal of surface oxide and contamination by wet etching, and/or to accumulation during delays in transfer to the XPS system. In the case of the SacDepOx, trace surface nitrogen was also detected, presumably associated with the use of N_2 and N_2O in the PECVD growth chamber.

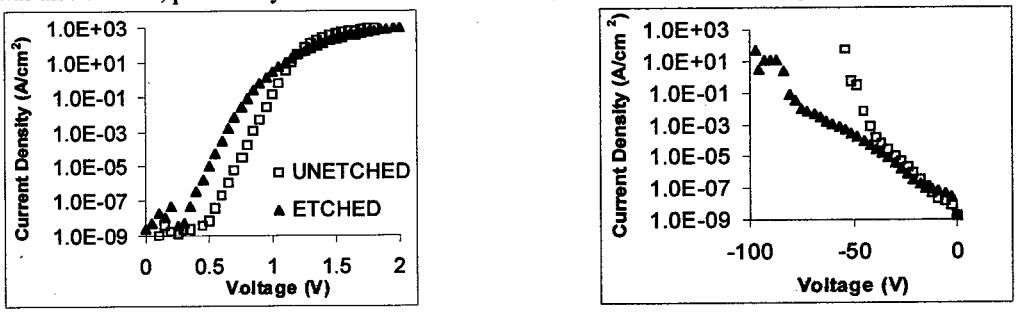

Fig 1: Forward and Reverse I-V Characteristics of diodes fabricated on sample (1).

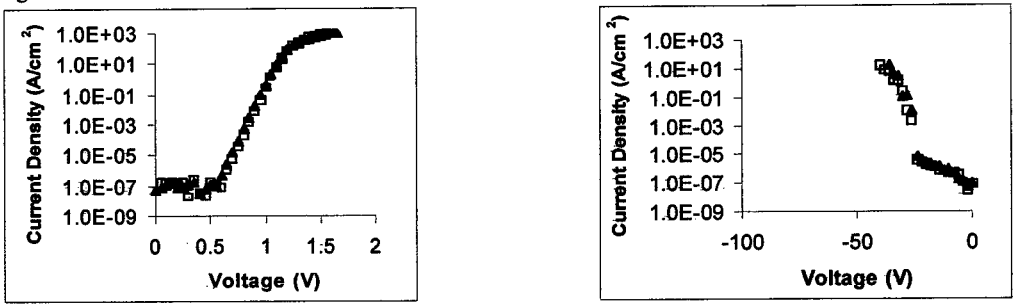

Fig 2: Forward and Reverse I-V Characteristics of diodes fabricated on sample (2) after the removal of thermally grown oxide.

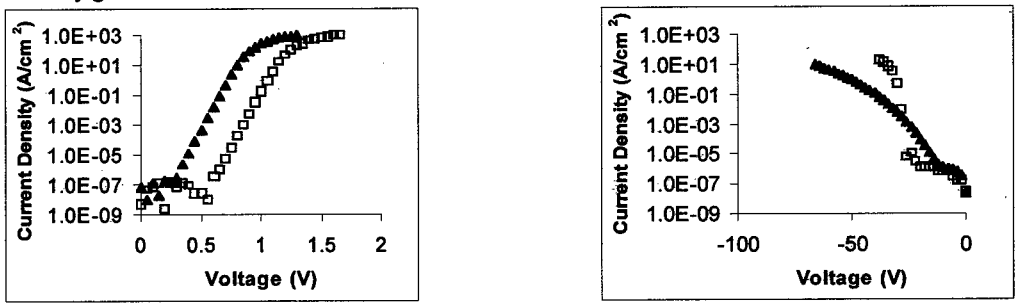

Fig 3: Forward and Reverse I-V Characteristics of diodes fabricated on the sample (3) after the removal of densified deposited oxide.

Electrical Results: Fig 1 depicts the forward characteristics of a typical diode fabricated on the RIE etched and unetched areas of the reference sample. Diodes fabricated on the unetched area of the sample all showed good ideality and low series resistance, but there was a variation in barrier height (Φ) between 1.54 and 1.78eV across the sample. This indicates the presence of an inhomogeneous contamination layer, which was not removed by the chemical clean. By contrast, there was very little variation from diode to diode across the etched section of the sample. However, these RIE etched diodes were less than ideal, with a strong curvature indicating a distribution in barrier heights over a length scale much smaller than the contact size. This localised variation in barrier height could be caused by the fluorocarbon contamination layer and/or underlying etch damage. Diodes fabricated on the etched area of the sample resulted in higher breakdown voltages (-80V) than those fabricated on the unetched area (-40V). In the lower reverse voltage region (0 to –15V) of the etched area I-V chracteristics, resistive behaviour is observed. This suggests the etch damage serves as a quasi-edge termination in the same way as Ar implantation. [12]

Diodes fabricated after sacrificial thermal oxidation on both unetched and etched material resulted in high ideality forward I-V characteristics with little variation in barrier height (1.49eV) across the wafer (Figure 2). However, both the unetched and etched area diodes showed sudden breakdown. This was probably due to the absence of any device termination. This process essentially completely removed the RIE etch damage and also removed any surface contamination on the as received wafers.

Figure 3 shows the forward and reverse characteristics of unetched and etched material after removal of densified deposited oxide. There was a striking difference in barrier height between the unetched (Φ= 1.46-1.6eV) and etched (Φ= 1.2eV) areas of the sample, with both areas showing good ideality. The unetched area showed some variation in barrier height across the sample, which was absent in the etched region. The reverse leakage current of diodes on the etched area of this sample was correspondingly higher, reflecting the lower barrier height. Like etched area diodes on reference sample 1, etched area diodes on sample 3 exhibited higher breakdown voltages, and resistive behaviour in the lower reverse voltage region.

All barrier heights obtained using I-V characteristics were confirmed by C-V measurements.

Conclusions: In this study, two treatments to remove surface damage and contamination following reactive ion etching have been assessed with XPS and Schottky diodes measurements. RIE left a fluorocarbon layer, which was not removed by simple chemical cleans and resulted in degraded diode ideality. The use of a sacrificial oxidation removed all trace of the fluorocarbon and produced near ideal diode behaviour suggesting complete damage removal. Interestingly, an annealed and stripped deposited oxide, which did not consume any of the surface SiC layer, dramatically improved the diode ideality on the etched area albeit with a reduced barrier height.

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4H-SiC Device Scaling Development on Repaired Micropipe Substrates

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Keywords: Defect, Diode, Epitaxy, LPE, Micropipe, Scaling, Schottky

Abstract. The impact of SiC Liquid-Phase Epitaxy (LPE) on improving the breakdown behavior of Schottky diodes is examined. This technique, which is know to fill in large area open core screw dislocation defects known as micropipes, has not been examined for its impact on other, smaller closed core screw dislocations, which are known to limit the scaling of large area SiC power devices. After statistical analysis of breakdown voltages on 83 *small-area* diodes (chosen so that defects other than micropipes would be primary yield limiters), distributed on both a control and LPE treated samples, no significant difference in breakdown voltage is observed.

Introduction. A major obstacle to commercial insertion of silicon carbide device technology into power electronics is the presence of hollow-core defects, known as micropipes, in the substrate material. Although considerable progress has been made to reduce the commercially-available micropipe density to less than 30 cm^{-2}, continuing presence of these defects is believed to be one limiting factor in large-area device development. Additionally, the presence of large numbers of closed-core screw dislocations, dislocation defects and other defects contribute to poor scaling of SiC power devices [1]. A process to reduce the micropipe density by filling the defects with SiC and covering the repaired material with a LPE layer has been developed at TDI, Inc. [2-5]. Large area Schottky diode device performance on SiC epi layers grown using Chemical Vapor Deposition (CVD) on both conventional and repaired substrates have also been reported [6]. One result of these early experiments was a significant improvement in the surface morphology (reduction of step-bunching in the CVD layer) of the as-received reduced micropipe substrate material. More recently, a transmission electron microscopy (TEM) investigation of TDI's micropipe reduction method with CVD epi has suggested that few dislocations may be generated at the LPE/CVD interface [7]. Although preliminary work indicates that the TDI process could improve device-scaling performance, this comparison was based upon a very limited sample size and, until now, no quantitative assessment of the device performance on these improved substrates has been performed. Here we statistically compare small-area (< 200 μm diameter) Schottky diode breakdown characteristics on micropipe repaired and conventional substrates, similar to data reported elsewhere [8].

Device Fabrication. A 4H-SiC substrate (Cree, 0001, 8° off-axis, n^+) was obtained along with a LPE processed wafer from TDI. Both wafers were placed in the CVD reactor and a 6 μm thick n-type epi layer was grown. The epi growth was conducted at a growth temperature of 1535°C with a silicon to carbon ratio (Si/C) equal to 0.3 for a duration of 3 hours to yield a thickness of approximately 6 μm (see Fig. 1). Samples were mechanically back-side polished to remove unwanted material grown during the CVD. Sputtered back-side nickel ohmic contacts were formed by tube annealing the contact for 20 minutes at 800°C in argon. Next, Schottky contacts were

formed using standard lift-off processing by spinning 3.2 μm of Microposit positive S1800 resist, exposing the pattern on a K. Suss MJB-3 aligner and developing. After thermally evaporating 800 Å of Ni, the pattern was lifted off using an acetone/methanol liftoff sequence. The anode radius ranged from 25 to 100 μm, as denoted by R in the cross-section shown in Figure 1. To permit top-side CV characterization, an ohmic annular cathode ring was deposited with an anode-to-cathode spacing W of either 10 or 15 μm. Measurements were then made using a curve tracer (Tektronix 577 or 371) to screen for blocking voltage (defined nominally at 50 μA of reverse current) in Fluorinert™, and doping density was extracted from CV measurements.

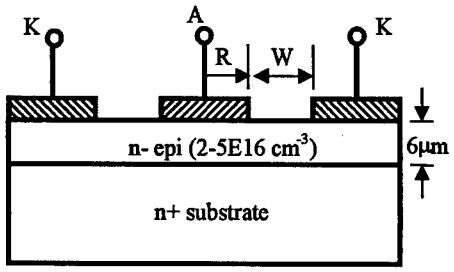

Figure 1: Device cross-section of 4H-SiC Schottky diodes fabricated on conventional 4H-SiC substrates and micropipe-repaired 4H-SiC substrates. Backside cathode contact (K) not shown.

Device Characterization. Dopant density extraction was very important to verify that the dopant density was uniform over each sample, and that samples being compared had the same dopant concentrations. The figure on the left (typical of our CVD reactor's uniformity) in Figure 2 illustrates dopant density of a sample doped at 2-3 x 10^{16} cm^{-3}. Note that the left and right portions of the sample had non-uniform dopant concentrations, which increased with depth. This sample, along with an identically doped micropipe repaired sample, were examined in terms of top-to-top breakdown, and the results from a limited set indicated that micropipe-repaired sample exhibited higher average breakdown, prompting the need for a more detailed comparison examining vertical Schottky barrier diode breakdown performance.

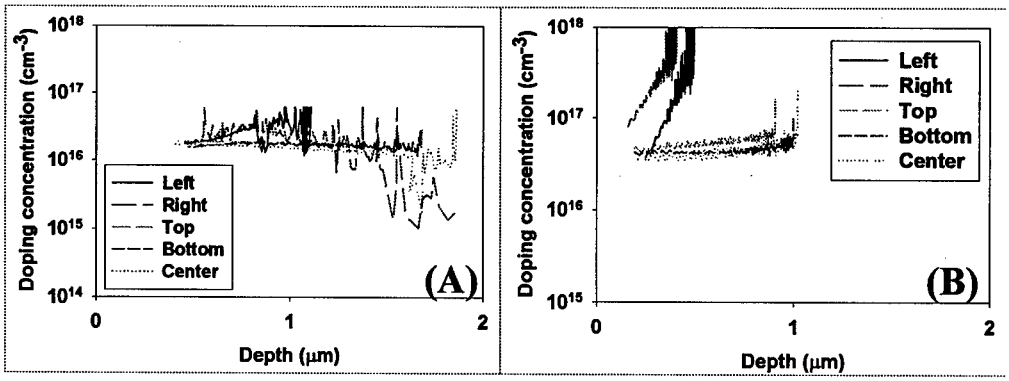

Figure 2: CV extracted dopant uniformity. Although dopant control was non-uniform near the left and right edges of the samples, the dopant control was extremely uniform over the majority of the sample. Both samples were approximately 20 mm x 20 mm while sample A is the control and B is the LPE repaired sample.

The graph on the right in Figure 2 shows typical dopant concentrations of both control and micropipe repaired diode samples which were compared more extensively in terms of vertical diode breakdown behavior. Note that the dopant concentration over the vast majority of this sample is very constant at 5 x 10^{16} cm^{-3}. Again, the left and right edge (in only the outside 3 mm) of the sample had non-uniform dopant control, and those diodes were not measured.

The distribution of vertical breakdown voltage was very similar for both the control and micropipe-repaired sample, as shown in Figure 3. The maximum breakdown voltage obtained for these samples was 150 V. For these Schottky diodes with a $5x10^{16}$ cm^{-3} doped, 6 μm thick blocking layer, this represented a maximum field of approximately 1.65 MV/cm or about 50% of the theoretical breakdown strength of SiC. Considering the diodes were unpassivated and unterminated, this is a very reasonable peak blocking voltage. A total of 42 diodes on the micropipe-repaired sample and 41 diodes on the control sample were examined with diameters ranging from 50 μm to 200 μm. The relatively small diameter diodes were chosen so that defects other than micropipes would be primary yield limiters since smaller defects nucleate from the process. The distribution plotted in Figure 3 represents data from all 83 diodes of various diameter. Although the average was slightly higher on the micropipe repaired sample, the statistical difference between it and the control was minimal.

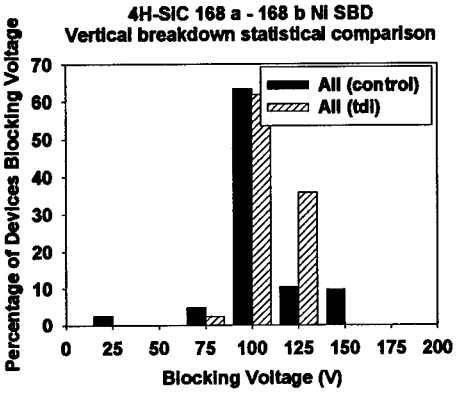

Figure 3: Comparison of statistical yield of Schottky diodes (all sizes) sorted for breakdown for control and micropipe-repaired (tdi) samples.

In Figure 4, the statistical distribution of diode breakdown is shown for all five diode sizes (radii of 25, 37.5, 50, 75, and 100 μm). Again, no significant statistical difference is observed for any of the distinct diode diameters. This information is summarized in Table 1, where one can observe that except for a smaller standard deviation, there is no clear difference in blocking voltage on the micropipe repaired sample as compared to the control. In fact, the average blocking voltage for each diameter falls within the standard deviation of the other sample so that no statistical advantage from either sample can be observed.

Table 1: Summary of diode breakdown statistics for control and repaired samples.

Diode Radius	25μm	37.5μm	50μm	75μm	100μm
Avg. Breakdown (control)	108.8	98	100	90	78.5
Avg. Breakdown (repaired)	***99.6***	***96***	***97***	***104***	***101***
Standard deviation (control)	17.9	14.8	22.6	11.0	34.2
Standard deviation (repaired)	***14.6***	***12.9***	***9.0***	***11.9***	***9.3***
Sample size (control)	8	10	10	6	7
Sample size (repaired)	***11***	***10***	***9***	***5***	***7***

Conclusions. We have previously reported on the effects of diode performance on micropipe-repaired substrates using LPE. In the past we have found that this technique does fill in the large open-core screw dislocation (micropipes) and that CVD also improves the surface morphology as compared to the LPE surface as verified by AFM [6,7]. However, in terms of impacting the smaller line defects, (shown to impact breakdown behavior in small-area diodes [1]), no significant improvement is observed by using the LPE repaired substrates. Thus, while LPE remains a useful technique for filling micropipes, its ability to improve small-area diode blocking voltages is not statistically significant. The LPE effects on large diameter diodes remains to be investigated.

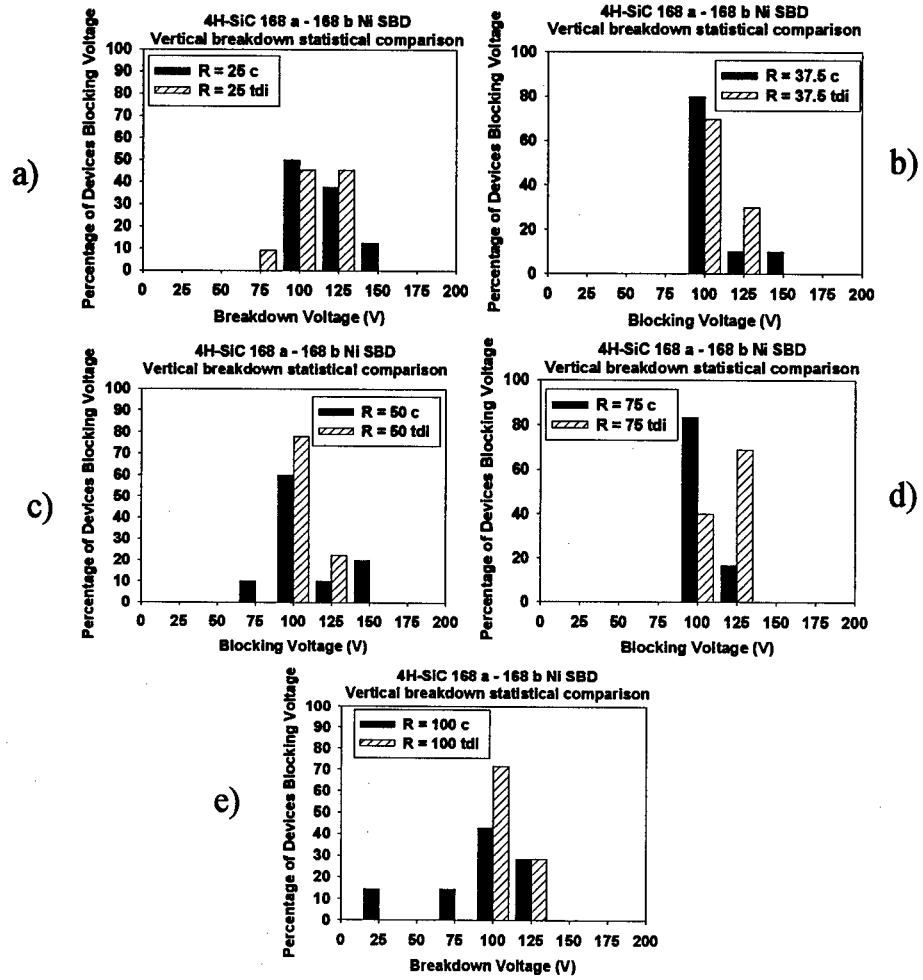

Figure 4: Breakdown voltage distribution of small-area (radii = 25, 37.5, 50, 75, and 100 mm shown in parts a) - e), respectively) 4H-SiC Schottky diodes fabricated on conventional (control) and micropipe-repaired (tdi) substrates.

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Design and Characterization of a SiC Schottky Diode Mixer

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Keywords: DC, High-Level Mixer, RF Measurements, Schottky Diodes, Singly Balanced Mixer

Abstract

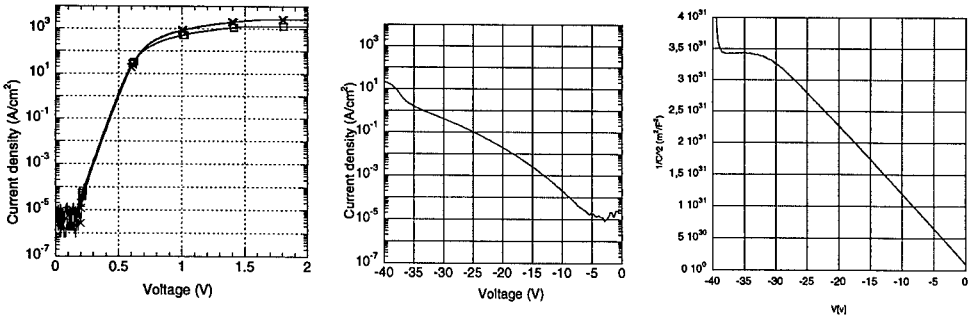
In this paper we present the work on a single balanced mixer with 4H-SiC Schottky diodes. DC and RF measurements are given for the circuit. The circuit gave a minimum conversion loss of 6.7 dB at 10 to 15 dBm LO input power. The conversion loss was below 10 dB for 0.7 to 1.4 GHz for a LO input power of 15 dBm.

Introduction

Mixers are used in various communication and radar systems to generate an intermediate frequency signal by mixing the incoming RF-signal with a local oscillator signal. This may be done with different non-linear devices such as FETs and diodes. SiC diodes are promising candidates as such a device partly because of its high power handling capacity resulting in better intermodulation performance [1].

Diode fabrication and measurements

The Schottky diode structure is as follows: on top of the 4H-n^{++}-type substrate, a highly doped buffer layer is grown, followed by a n-type epilayer. The doping concentration for the *n* drift is $3.1 \cdot 10^{17}$ cm^{-3}, and the buffer has a doping of $8 \cdot 10^{18}$ cm^{-3} and finally the substrate has a doping of $1.1 \cdot 10^{19}$ cm^{-3}. The drift and buffer layer is 0.38 μm and 0.5 μm thick. Substrate thickness is 340 μm. Mesas are etched by Ion Beam Etching. Schottky barriers are formed by evaporation of Ti-. A backside contact was formed by Ni-evaporation and annealing at 950 C for 5 min. in an Ar:H_2 atmosphere. The backside was finally gold plated. The capacitance and IV measurements are shown in fig. 1. IV measurements gave a barrierheight of ϕ_{Bn}=0.88 eV, a J_0 of $5 \cdot 10^{-8}$ A/cm^2 and an ideality factor of η<1.2. The CV-measured V_{bi} was 0.97 V and N_D was measured to be $2.7 \cdot 10^{17}$ cm^{-3}. This gives ϕ^0_{Bn}=1.08 eV and the drift epilayer donor doping to be $3.1 \cdot 10^{17}$ cm^{-3}. The large difference of barrier heights between IV and CV measurements has been noted previously by others [2].



(a) (b) (c)

Fig. 1. Forward (a) and reversed (b) Current-Voltage characteristics for the diode. Capacitance-Voltage characteristics for the reversed biased diode (c). The C_{j0} for these diodes were approximately 11.7 pF for a radius of 50 μm.

Mixer design

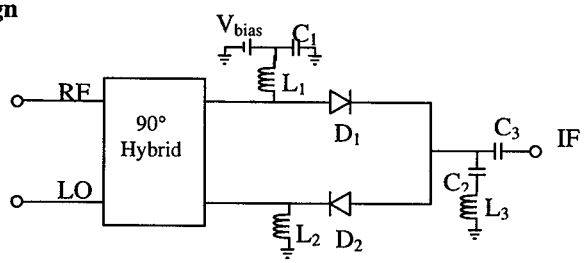


Fig. 2. The topology of the mixer.

The mixer has the topology shown in fig 2. It was designed using HP Microwave Design System for the non-linear simulations, using the non-linear model extracted from measurements. The mixer is a singly balanced mixer. It consists of two mixers combined with a 90°-hybrid. The RF and LO are applied to one pair of mutually isolated ports. The diodes are connected to the ports such that their polarities are opposite.

Mixer characterization and results

The mixer was fabricated on a duroid-substrate mounted on a copperplate. Chip capacitors and inductors were soldered to the substrate. The diodes were diced and soldered to an alumina-

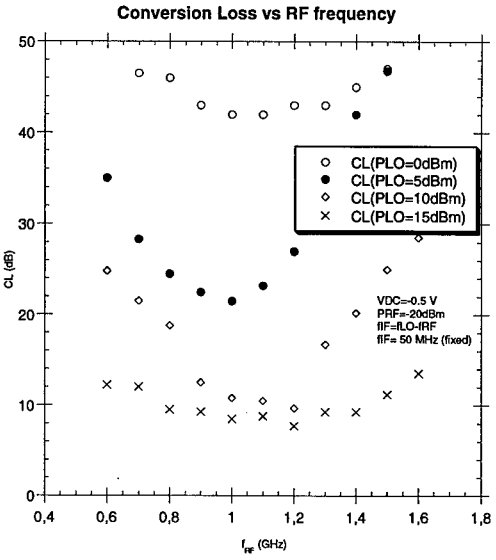


Fig. 3. Conversion loss versus frequency.

carrier. The carriers were then glued to the substrate and ribbon-soldered to the circuit. SMA-contacts were used for the RF, LO, IF and DC connections.

The mixer has been characterized regarding DC bias, RF bandwidth, LO saturation, conversion loss, and compression. It had a conversion loss of 6.7 dB at a RF of 1.15 GHz, IF of 50 MHz and a LO-power of 10 to 15 dBm. This is to our knowledge the best-reported conversion loss for a SiC diode mixer (12 dB CL in ref[1]).

Fig.3 shows the conversion loss versus frequency and gives the RF bandwidth for this mixer. The bandwidth increases with high LO power and with 15 dBm LO power it has a conversion loss below 10 dB for frequencies between 700 MHz and 1.40 GHz.

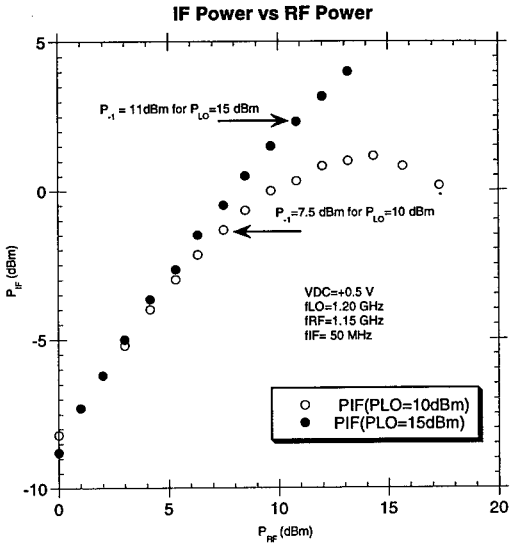


Fig. 4. Conversion loss versus LO power.

Fig. 4 shows the bias dependence of the mixer circuit. The bias was applied according to the circuit schematics in fig. 2. For lower bias (-0.5 at best) it was possible to get the lowest conversion loss. However for high simultaneous RF input power the circuit started to self-bias. For a positive bias of 0.5 V, self-biasing was not an issue, but a higher conversion loss could not be avoided. From the figure it can also be seen that the conversion loss abruptly increases for the lower biases when lowering the input LO power. Thus lower bias demands a higher LO input power. This comes from the fact that the LO amplitude is not reaching the voltage levels necessary for the mixer-diodes to operate in their non-linear voltage range (0.2-0.7 V approx.) from figure 1.

Figure 5 shows the output IF power versus input RF power for the DC bias of 0.5V. The 1 dB compression points referred to the input are 11 dBm (RF) at a LO power of 15 dBm and 7.5 dBm

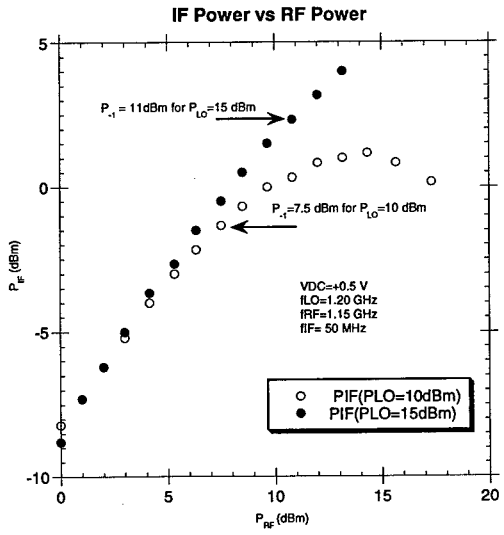


Fig. 5. IF power vs. RF power

(RF) at a LO power of 10 dBm.

Conclusions

A single balanced mixer has been designed, measured and characterized based on SiC Schottky diodes manufactured in our lab. RF characterization shows a very good conversion loss of only 6.7 dB at best, and less than 10 dB for frequencies between 0.7 and 1.4 GHz when a LO power of 15 dBm was used. These diodes which initially were intended for higher frequencies and thus only have Schottky contacts with a diameter of 50 microns, are still capable of handling 21 dBm input LO power which makes them suitable for high-level mixers even at these low frequencies. SiC Schottky diodes are very interesting for front-end mixing because of their high input power capability and temperature endurance.

Acknowledgments

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Materials Science Forum Vols. 338-342 (2000) pp. 1211-1214

Breakdown Voltage Improvement of 4H-SiC Schottky Diodes by a Thin Surface Implant

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Keywords: 4H-SiC, Breakdown Voltage, Leakage Current, Schottky Rectifiers

Abstract. In this paper we present a technique to improve the blocking capability of p-type 4H-SiC Schottky rectifiers by use of a shallow surface implant. Devices with near-ideal breakdown voltage as high as 900 V have been obtained with only 4 μm thick drift layer, corresponding to a critical breakdown field of $\sim 3\times10^6$ V/cm. Not only does the breakdown voltage improve, the reverse leakage current is also significantly lowered. However, the forward voltage of the diodes with surface implants are slightly higher.

1. Introduction

Superior intrinsic material properties such as avalanche electric breakdown field, large bandgap and high thermal conductivity make silicon carbide (SiC) a strong candidate for high-voltage, high-frequency and high temperature semiconductor devices. Current state-of-the-art SiC Schottky rectifiers have achieved blocking capability as high as 4 kV [1]. However, as a direct consequence of their ability to sustain high electric fields, high-voltage SiC Schottky rectifiers show high levels of reverse leakage current due to image force-induced barrier lowering and corner field enhancement [2],[3]. This results in high off-state power losses. In this paper, we will describe a technique to improve on the reverse leakage current and blocking capability of 4H-SiC Schottky rectifiers via a thin surface implant. Devices with nearly ideal breakdown voltage have been obtained with only a 4μm drift layer.

The energy band diagrams for an p-type semiconductor having a surface layer containing either acceptors or donors is shown in Fig. 1. The metal-semiconductor interface has an ideal barrier height of Φ_B (energy band c). The presence of heavily doped layer with acceptor impurities (energy band b) increase the surface field. The width of the barrier is reduced which facilitates carrier tunneling (as indicated in Fig.1), thereby reducing the effective barrier height. On the other hand, the presence of surface layer with donor impurities (energy band c) can increase the effective barrier height to majority carriers [4]. Due to the opposite conductivity of the surface layer, electric field at the surface is decreased. Beyond a threshold charge in the surface layer at which the surface electric field is zero, the surface field reverses sign and the peak electric field is within the bulk. A potential maximum occurs within the surface layer which increases the barrier height. Therefore, not only the electric field at the semiconductor surface is decreased in the case of barrier raising, but peak electric field point occurs in the bulk of the semiconductor. The Schottky barrier lowering effect is reduced and the reverse characteristics of the device improved.

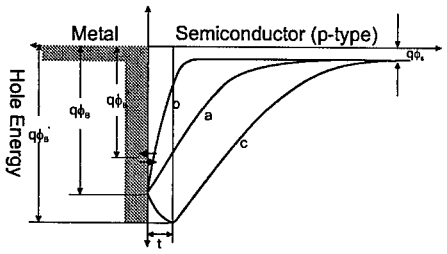

Figure 1: Schematic of conduction band edge for a Schottky barrier with or without a surface implant layer. t is the thickness of the surface implant layer.

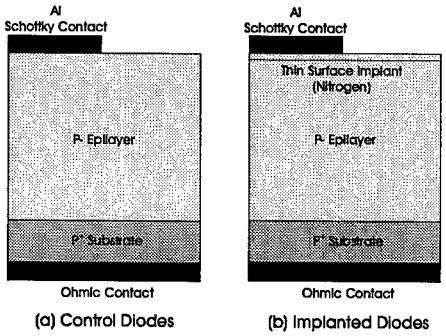

Figure 2: Schematic of the cross-section of the p-type Schottky devices fabricated in this work.

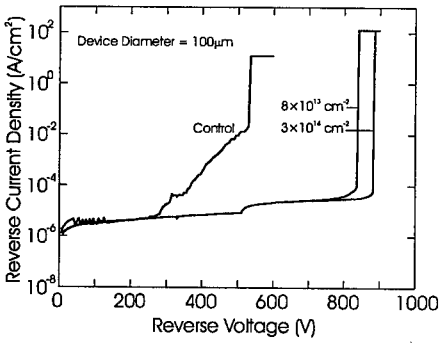

Figure 3: Reverse log(J)-V characteristics of 100 μm diameter diodes at room temperature.

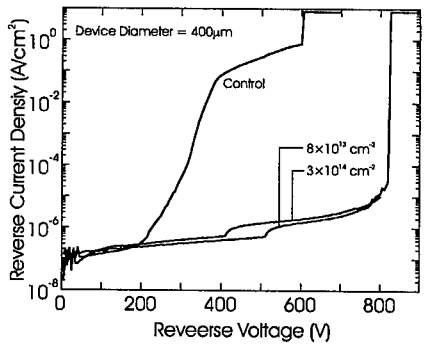

Figure 4: Reverse log(J)-V characteristics of 400 μm diameter diodes at room temperature.

2. Device Fabrication

The samples utilized for the experiments were p on p^+, 8° off-axis, Si face, (0001) 4H-SiC wafers purchased from CREE Research. The thickness and the doping of the p-type epi-layer were 4.0 μm and 1.8×10^{16} cm^{-3}, respectively. One of the three types of samples was a control (sample A), while the other two samples (samples B and C) underwent implantation with two different dosages. A 50 nm thick PTEOS oxide was deposited on samples B and C which was then annealed at 1100°C in wet oxidizing ambient for 3 hrs followed by re-oxidation at 950°C for 1 hr. This resulted in a net oxide thickness of about 65-70 nm on the two samples. Sample B and C were then blanket-implanted with nitrogen (n-type dopant in SiC) with dose/energy of 8×10^{13} cm^{-2}/25 KeV and 3×10^{14} cm^{-2}/25 KeV, respectively. Following implantations samples B and C were annealed at 1100°C in argon for 1 hr. Oxide was then stripped from the two samples in wet buffered oxide etch. The thickness of the resultant implanted layer was ascertained to be about 25-30 nm from SUPREM simulations. Backside ohmic contact was formed by alloyed Al/Ni/Al (100/100/10 nm). Al was then deposited on the front side through a shadow mask to form Schottky diodes with diameters from 100-400 μm (Fig. 2).

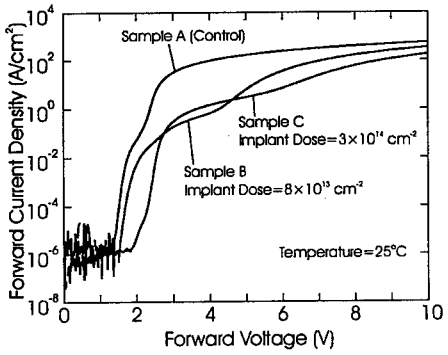

Figure 5: Forward log(J)-V characteristics of 100 μm diameter diodes at room temperature.

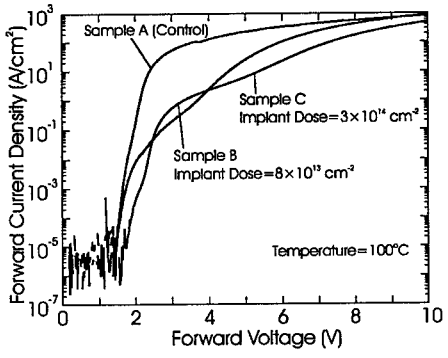

Figure 6: Forward log(J)-V characteristics of 100 μm diameter diodes at 100°C .

3. Results and Discussion

Typical reverse leakage current characteristics of p-type 4H-SiC Schottky diode with 100μm diameter are shown in Fig. 3. A breakdown voltage of about 530V is observed on the control diodes with the reverse leakage current density showing significant increase near 275V typical of SiC Schottky rectifiers [1],[2],[3]. Diodes with surface implants show significant improvement in the breakdown voltage. Devices with 8×10^{13} cm^{-2} surface nitrogen implant indicate a breakdown voltage of about 830V whereas, devices with 3×10^{14} cm^{-2} dose nitrogen implant show slightly higher breakdown voltage of about 900V. The implanted devices also show better leakage current density than the control devices. Unlike control diodes, the leakage current density in implanted diodes does not show significant increase and stays within the same order of magnitude until breakdown. The room temperature leakage current density at a reverse bias of 200V is observed to be about 3×10^{-6} A/cm^2 for all three device types. At a reverse bias of 500V, however, the implanted devices showed leakage current density of about 1×10^{-5} A/cm^2 compared to about 9×10^{-3} A/cm^2 measured on the control diodes.

Devices with larger area did not show significant deviation in characteristics, indicating similar breakdown voltages as shown by reverse characteristics of 400μm diameter diodes in Fig. 4. Device with surface implants achieved lower leakage current and higher breakdown voltage than control devices even at high temperatures.

Fig. 5 shows the measured forward characteristics of the devices at room temperature. Implanted devices indicate higher forward voltage drops which a direct consequence of increased barrier height. At 100 A/cm^2 control diodes showed a forward voltage drop of 4.1V which increased to about 7-9V for the implanted diodes depending on implant dose. Control devices had a minimum ideality factor of 1.4 and a barrier height of 1.74 eV as extracted from the low current exponential region of the characteristics, which increased for the implanted diodes as given in Table 1. Such high values of ideality factor and barrier height indicate significant deviation from ideal thermionic emission theory. Nevertheless, these results show significant improvement over previously reported p-Schottky diodes on 4H-SiC [5]. Forward log(J)-V-T measurements have also been performed to analyze the device performance at higher temperature. As indicated in Fig 6 diodes indicated similar characteristics at high temperatures as well. Specific on-resistance of the control diodes was found to be about $\sim$13 mΩ.cm^2 as compared to 11 and 16 mΩ.cm^2 obtained from low and high dose implanted diodes, respectively.

Table 1: Measured parameters of the fabricated p-type Schottky at room temperature.

Sample	Implant Dosage	Breakdown Voltage (BV)	Reverse Leakage Current Density at 500V (J_R)	Forward Drop at 100 A/cm^2 (V_F)	Barrier height (Φ_B)	Ideality Factor (n)
	(cm^{-2})	(Volts)	(A/cm^2)	(Volts)	(eV)	
Sample A	Control	530	9.1×10^{-3}	4.1	1.74	1.41
Sample B	N, 8×10^{13}	830	1.5×10^{-5}	7.2	1.82	1.45
Sample C	N, 3×10^{14}	895	1.8×10^{-5}	8.8	2.0	1.75

A forward bias of greater than 100 A/cm^2 in all these device was accompanied by a visible electroluminescence of blue color with implanted diodes showing brighter emission. This kind of light emission has previously been observed in Au-SiC Schottky devices [6]. This emission is believed to be generated by highly energetic carriers impinging on the metal from the semiconductors, typically in Schottky devices with high barrier height.

The breakdown voltage reported in this work is the highest reported for a p-type Schottky diode on any polytype of SiC. Previous reported high breakdown voltage on a p-type 4H-SiC Schottky diode is 600V, achieved on devices with argon implanted edge terminations [5]. The improvement in leakage current is due to the lowering of the surface electric field as described earlier. The breakdown voltage of control diodes will be affected by surface conditions and edge field enhancement. In implanted diodes, on the other hand, the surface conditions will be less effective as the peak electric field point if pushed into the bulk of the semiconductor. Also blanket surface implant acts as junction termination thereby alleviating corner field enhancement. A first order calculation of the critical field, assuming that the device breakdown is not limited by corner field enhancement, indicated a value of about 2.7-2.9$\times10^6$ V/cm for the implanted devices.

4. Summary

High-Voltage Schottky rectifiers have excessively high reverse leakage current at high reverse bias due to significant barrier lowering. We have demonstrated a simple technique to improve the leakage current of Schottky devices by employing a thin surface layer implant. The breakdown voltage of the implanted device is also shown to improve dramatically. However, this improvement comes with a penalty in forward voltage drop.

Acknowledgment

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Materials Science Forum Vols. 338-342 (2000) pp. 1215-1218

DC and Pulse Characterizations of (600V) 6H-SiC Schottky Diode Breakdown

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Keywords: 1-µs Pulse Breakdown Voltage, 6H-SiC Reliability, DC Breakdown Voltage

Abstract : Both transient and DC breakdown characteristics of 6H-SiC Schottky diodes have been measured. The data show large discrepancies between the set of tested devices. Most devices withstand a maximum voltage under transient voltage pulses above DC Breakdown. On the other hand some parts have premature failures with a 75 % derating. This set of data is representative of both the quality of the material and the structure of the device (electric field control edge).

I. Introduction

SiC power devices should allow higher power ratings and should supersede silicon in many high power electronic applications [1-2]. However, before this happens, SiC power devices must exhibit reliability as good as silicon based power devices. Silicon based power devices present large Safe Operating Area (SOA) and large immunity to overvoltage stresses because they are free of defects and they get a Positive Temperature Coefficient of Breakdown Voltage (PTCBV) [3-4]. In the case of SiC based devices, it has been shown that both a high density of micropipes (10^2 cm^{-2}) and of elementary screw dislocations (10^4 cm^{-2}) [5] could induce premature breakdown point. These defects are very detrimental for breakdown behavior of SiC power devices. This paper examines the DC and pulse reverse bias characteristics of middle range voltage (600V) 6H-SiC schottky diodes free of micropipes.

II. Experimental Details

A. 6H-SiC Schottky Barrier Diodes

6H-SiC schottky diodes are manufactured at CEA-LETI. A 6 µm n-doped layer is grown on commercial n+-SiC wafers from CREE (N_d=2x10^{18} cm^{-3}). Square diode mesas are processed by plasma etching (RIE). Contacts are obtained by Ti-deposition and junction edge terminations are made with Al-implantation to limit the increase of the electric field at edge of the contact as shown in Figure 1 [6]. Epilayer doping (N_d=2x10^{16} cm^{-3}) and schottky barrier height (ϕ_b=0.7 eV) are calculated from a high frequency (1MHz) C(V) measurement [7]. From these data, we are able to calculate the theoretical critical electric field E_{cr}, the breakdown voltage V_{br} and the thermoionic reverse leakage current density J_s [8], all these values are summarized in Table 1.

Table 1 : Main Schottky Barrier Diode features

N_d	ϕ_b	E_{cr}	V_{br}	J_s
3×10^{16} cm^{-3}	0.7 eV	2.7 MV/cm	850 V	1.8×10^{-5} A/cm^2

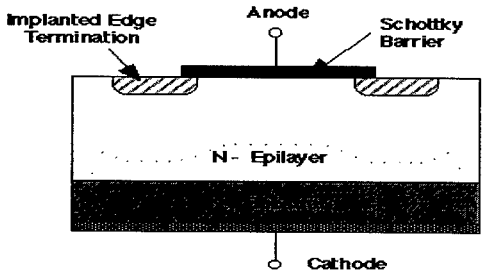

Figure 1 : Schematic cross section of an implant edge terminated Schottky Barrier Diode in 6H-SiC.

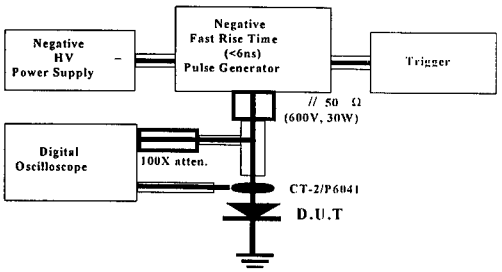

Figure 2 : Fast rise time 1μs-pulse testing circuit.

In this study, we have performed measurements on three sets of schottky barrier diodes with an active area of respectively 8×10^{-5} cm², 84×10^{-5} cm² and 240×10^{-5} cm². For each area, more than three devices have been tested.

Due to the crystal defect densities observed on commercial SiC wafers and due to the area of the present diodes, theoretically our devices should be free of micropipes. Nevertheless they could present some elementary screw dislocations.

B. Measurement settings

DC reverse bias $I_r(V_r)$ characteristics are measured with a HP4142-3A high voltage power supply (1000V, 10mA). In order to avoid any damage of the samples during DC measurement, we limit the reverse current density J_r by setting a current compliance of 1A/cm².

On the other hand, diodes are submitted to single 1μs-pulses with increasing amplitude up to 700 V. The pulse measurement circuit is schematically illustrated in Figure 2. During pulses, both voltage and current transient responses are monitored and recorded on a digital oscilloscope. The current probe used in this work is a commercial Tektronix CT-2 device. The high voltage is monitored with a 50Ω bias Te. After each pulse, DC reverse characteristic is checked.

III. Results and Discussion

A. DC Measurements

In a first step, we have determined the conduction behavior of our device as a function of reverse voltage. As illustrated in Figure 3, the reverse bias response of the different sets is well fitted by the thermoionic emission theory with the image force lowering (straight curves). But for the three sets, the parameters extracted from the fit are much higher than the theoretical values calculated from the Table 1 as represented in the Figure 3 by the dashed curve. This discrepancy can be explained by the non uniformity of the Schottky barrier height, Bathnagar et al. [9] relate this non uniformity to the presence of defects as elementary screw dislocations.

Furthermore, we have determined the breakdown voltage V_{br} of each sample. First of all, measurements have been made up to 10 A/cm². For this high value of reverse current density, a high increase in the reverse current happens but it leads to the destruction of our device. To forbid any catastrophic degradation, reverse current compliance is set to about 1 A/cm². Then, V_{br} is defined for the maximum reverse current density accessible without any degradation as previously explained. From the first destructive experiments, we can evaluate that we under estimate the breakdown voltage of about 10 %. For this current value, diodes present a breakdown voltage ranging from 250V to 500V depending on the quality of the characterized samples as illustrated in Figure 4. These experimental values are lower (between 40% to 60%) than the theoretical breakdown voltage calculated in Table 1. This discrepancy could be related to either the lack of

efficiency of the implant edge termination or the presence of elementary screw dislocations. Furthermore as illustrated in Figure 4, experimental breakdown voltages are dependent on the diode area with an increasing average value as a function of the decreasing area. These results could be related to the defect density in the material.

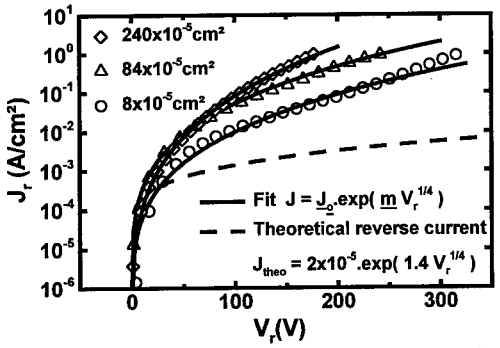

Figure 3 : Schottky barrier diode DC current density as a function of reverse bias V_r.

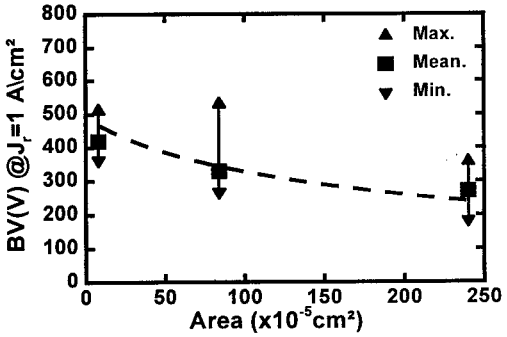

Figure 4 : DC Breakdown voltage as a function of diode area.

B. Transient measurements

In this section, we present results from pulse measurements. Figure 5 illustrates typical response of SiC diode during a 1-µs electric pulse. As expected from DC characterization, no detectable conduction current is measured for pulse voltage up to the DC breakdown voltage. Above this voltage, the reverse current density becomes significant (J >1 A/cm^2) and increases with the pulse magnitude (see Figure 6). This increase of current could be related to the limited efficiency of the implant termination edge. This limitation can not be reached in the case of DC measurements since very high voltage leads to device failure.

For 85 % of the tested devices, the highest pulse voltage without any catastrophic breakdown should exceed the DC breakdown voltage by 10 % up to 100 % as illustrated in Figure 7. This first set of data is consistent with expected behavior of device under transient solicitations where the breakdown voltage performance is increased when pulse duration is decreased [10]. However, comparison with data obtained on silicon devices shows that the improvement of the breakdown voltage as a function of pulse duration could be as high as three to ten times the DC breakdown voltage [10]. This discrepancy could be explained either in terms of implant edge termination efficiency as discussed previously or in terms of SiC material quality.

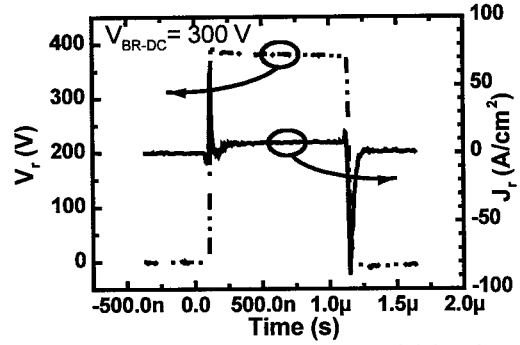

Figure 5 : Transient reverse voltage (straight) and current (dash) of a 84x10^{-5} cm² diode presenting a DC breakdown voltage of $V_{BR\text{-}DC}$ = 300V.

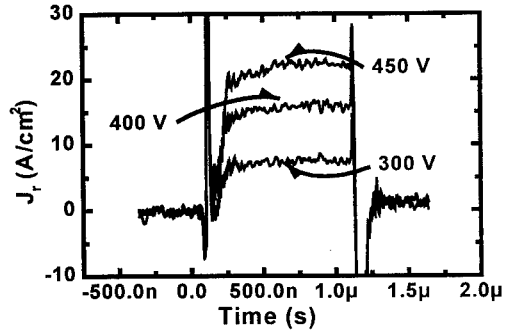

Figure 6 : Reverse current density J_r for several pulsed voltages of a 84x10^{-5}cm² diode presenting a DC breakdown voltage $V_{BR\text{-}DC}$ = 300V.

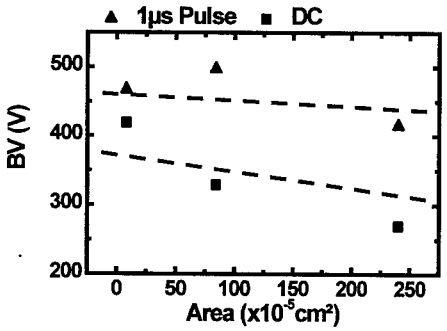

Figure 7 : Breakdown voltages under DC and Dynamics measurements.

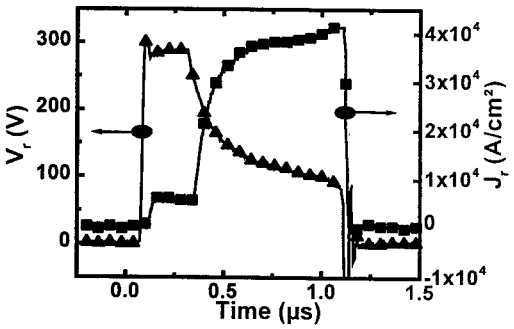

Figure 8 : Pulse measurement of a 84×10^{-5} cm² diode with a BV_{DC}=450 V.

On the other hand, 15 % of the tested diodes present a quite different response under pulse measurement. Surprisingly, pulse breakdown voltages are lower than DC breakdown value, down to 75% of the DC breakdown voltage. This type of behavior is illustrated in Figure 8. During the first 20 ns the diode withstands the 300 V reverse bias, then the reverse current increases up to 5000 A/cm² and the reverse bias falls down (about 10 volts). This voltage drop is observed during the next 200 ns before voltage collapses drastically and current reaches the maximum output current of the pulse generator that is synonymous of diode failure. This reduction can be explained by the presence of elementary screw dislocations as previously reported [4,11]. In spite of this behavior, during the first 200 ns the diode presents a positive temperature coefficient of breakdown voltage (the voltage increases while the current decreases) as silicon based devices and it is encouraging.

IV Conclusion

We have tested 6H-SiC 600V Schottky Barrier Diodes under both transient and DC conditions. Two different behaviors are reported. For 85% of the parts the pulsed mode of operation results in a maximum voltage above the DC breakdown. On the other hand 15% of the parts suffers from premature failures. This ~ 75% derating of the breakdown voltage is related to crystaline defects of the material. Compared to previous data, these results show an improvement in material quality. Nevertheless this problem still limits the maximum achievable yields for high volume industrial production.

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Materials Science Forum Vols. 338-342 (2000) pp. 1219-1222

6H-SiC Schottky Barrier Diodes with Nearly Ideal Breakdown Voltage

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KW: Contact Annealing, Ideal Electrical Characteristics, Oxide Ramp Profile, Schottky Diodes

Abstract - A simple edge termination based on oxide ramp profile around the Schottky contact is used on Ni Schottky rectifier fabricated on a $2.7x10^{16}cm^{-3}$ n-type 6H-SiC epilayer. Three anneals of the Schottky contacts were experimented. The diodes annealed at 900 °C showed excellent reverse characteristics with a nearly ideal breakdown at about 800V. Forward characteristics follow thermionic emission theory with ideality factor nearly one.

1. INTRODUCTION

SiC Schottky rectifiers are a promising technology after the potential for low forward drop (smaller than 2V at $100A/cm^2$), high breakdown voltage (up to 5kV) and fast switching speed with no reverse recovery current [1-3]. The SiC Schottky rectifiers offer substantial performance benefits in high voltage and high temperature operation over Si and GaAs Schottky rectifiers. Si and GaAs Schottky structures are severely limited only for systems operating below 200 V and 600V respectively, by low critical field of these materials. An other restriction for these semiconductors is relativity low value and small range of the Schottky barrier height variation. Therefore, Si and GaAs Schottky contacts lead to a substantial increase in reverse leakage current at elevated temperatures, and dissipate more power.

The excellent material characteristics of SiC like large breakdown electric field (one order of magnitude higher than silicon), high electron saturated velocity and high thermal conductivity makes it a very promising semiconductor for high voltage applications, which reduced power losses. SiC Schottky rectifiers have been shown to have a strong dependence of Schottky barrier height on metal work function [3].

In the case of high voltage devices, the edge termination plays a crucial role in achieving the parallel plane breakdown voltage. Two and three – dimensional field crowding of non edge terminated devices increases the electric field at the contact edge well above the parallel plane electric field. The *mesa* edge termination has been demonstrated to provide a nearly ideal breakdown voltage for SiC *pn* junctions. However, this approach is unattractive because the *mesa* surface is difficult to passivate [1-2]. Various planar edge termination, such as floating metal rings, *p*-type guard rings, highly resistive surface regions formed by boron implanted or by porous SiC, dual metal trench, have been explored for SiC power devices [1-3].

We had previously proposed a simple planar edge termination technique with which nearly ideal plane parallel breakdown is achieved [4-5]. This technique is based upon creation of a field plate overlapping on oxide ramp etching at the Schottky contact periphery, and it was successfully tested on Si power devices [5]. A 6H-SiC Schottky barrier structure with this termination has been simulated using MEDICI program [4]. The simulations showed that a parallel plane electric field and a volume breakdown voltage are obtained for the oxide ramp smaller than 5° and an oxide thickness of at least 1μm, respectively [4]. Although the termination with oxide ramp profile can be used with any high voltage SiC device, experimental confirmation is demonstrated for Ni/*n*-type 6H-SiC Schottky barrier diodes (SBD) in this contribution.

2. EXPERIMENTAL PROCEDURE

The basic device structure of the oxide ramp profile SBD is presented in Fig. 1. As a starting material, we used n^+ 6H-SiC Lely substrate with 5μm thick epitaxial *n* layer doped to $2.7x10^{16}$ cm^{-3} grown by sublimation method at IOFFE. Multiple oxide layers, undoped (LPCVD), phosphorous 8% doped and undoped (CVD) having a total thickness of x_o=1.1μm, were grown on the epilayer. Circular contact windows (320 μm diameter) in oxide were defined using a shadow mask. In order to obtain an oxide ramp profile a P-etch solution was used for oxide over-etching. The angle of the ramp was measured to be smaller than 4° (Fig. 1). Before metallization, the contact window was cleaned using RCA method. After this cleaning procedure, 5000 Å thick nickel was evaporated. High vacuum annealing at three temperatures (800°C, 900°C and 1000°C) for 2 min. were performed to form Schottky barrier contact. E-gun evaporation of nickel was also done (before Schottky contact) on the heavily doped backside substrate and annealed at 1100°C to obtain an ohmic contact.

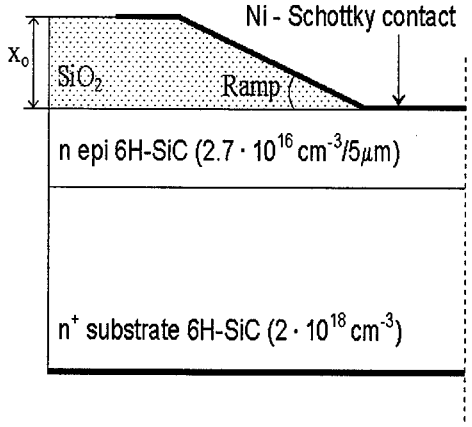

Fig. 1. Schematic cross section of the Schottky barrier diode with the Oxide ramp profile.

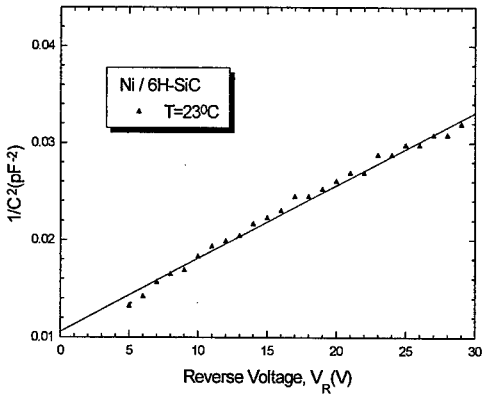

Fig. 2. Typical $C^{-2} - V_R$ curve measured on a sample annealed at 800°C.

3. ELECTRICAL CHARACTERISTICS. DISCUSSIONS.

Fig. 2 shows a typical capacitance versus reverse voltage characteristic measured on a Schottky barrier diode with oxide ramp profile. The C^{-2}-V curve is well fitted with a linear characteristic, confirming a uniform doping of the epitaxial layer. A $3x10^{16}cm^{-3}$ concentration obtained from the slope of this linear characteristic (Fig. 2) is in good agreement with the measurements made on the epitaxial layer (Fig. 1).

Figs. 3-4 present the reverse characteristics of the Ni/6H-SiC SBD. At the room temperature, the two different samples annealed at 800°C and 900°C exhibited a sharp breakdown at an average value of 600V and 800V, respectively (Fig. 3). The breakdown is not destructive. MEDICI simulations shown that for mentioned values of x_o and RAMP (Chapter 2) an ideal plane parallel breakdown voltage of 800V is achieved. Simulations of leakage currents have not been performed. A dramatic degradation in breakdown voltage is resulted after annealing at 1000 °C. Reverse leakage current increases rapidly with the increasing of the reverse bias (Fig. 3). This results of the formation of an ohmic contact at the interface. A sharp reduction in breakdown voltage is also observed when measuring temperature is increased up to 125°C for annealed samples at 800°C (Fig. 4.). The decreasing in the breakdown voltage can be partially attributed to the negative temperature coefficient of the breakdown electric field reported for 6H-SiC.

The reverse leakage current density is very low with a weak dependence on voltage for V_R>100V after an annealing at 800-900°C (Fig. 3). The magnitude of this current predicted by thermionic emission is much lower than experimental values of reverse leakage current (Figs.3-4).

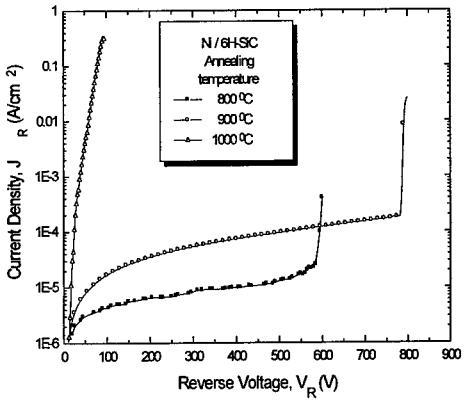

Fig. 3. The room temperature reverse Characteristics of SBD sample annealed at different temperatures.

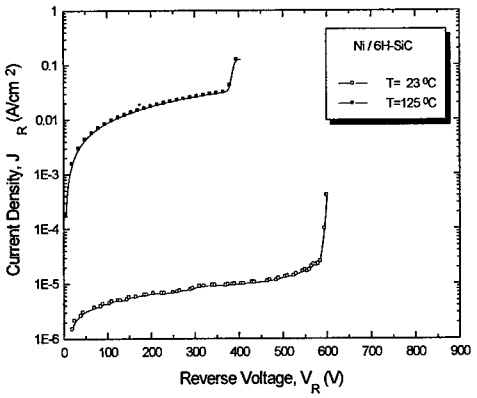

Fig. 4. The J_R-V_R characteristics measured at two temperatures on a sample annealed at 800 °C.

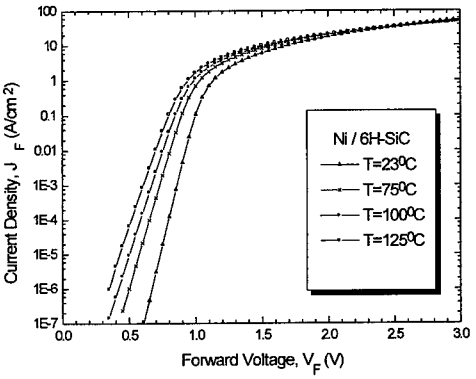

Fig. 5. The J_F–V_F characteristics measured at different temperatures on SBD with oxide ramp profile.

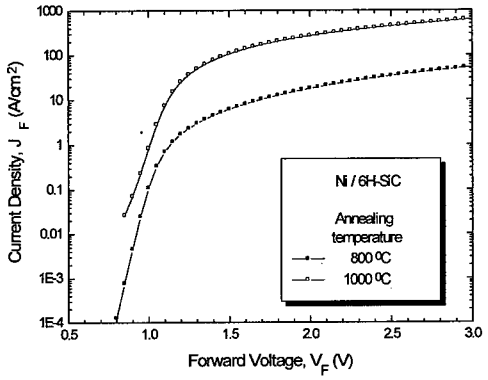

Fig. 6. The annealing temperature influence on $J_F - V_F$ curves of SBD with oxide ramp profile.

The typical measured J_F-V_F characteristics of a Schottky barrier diode with oxide ramp profile are shown in Figs. 5-6. Analysis of 800°C annealed sample (Fig. 5) revealed that the current conduction mechanism follows the thermionic emission theory for at least six orders of magnitude into low current density levels. However, at higher levels, the series resistance comes into effect and this contributes to an additional voltage drop across the diode. The forward voltage drop is

$$V_F=(nkT/q)ln(J_F/A^*T^2)+ \Phi_{Bn}+R_{on}J_F,$$

where k is the Boltzman's constant, T is the temperature and A^* is the Richardson's constant.

The ideality factor (n), Schottky barrier height (Φ_{Bn}) and the specific on resistance (R_{on}) values extracted from the J_F-V_F measurements are given in Table 1. The values of Φ_{Bn} and n remained invariant (within measurements errors) with temperature and indicate a high quality of the Schottky contact.

The elevated values of the specific on-resistance (Table 1) explain the high forward voltage drop at 100A/cm^2 current density for sample annealed at 800 °C (Fig. 4.). The on–resistance shows an increasing trend with increasing temperature (Table 1).

Table 1. Parameters of Ni/6H-SiC SBD annealed at 800 °C.

T(°C)	Φ_{Bn}(V)	n	R_{on}(mΩcm^2)
23	1.39	1.02	18
75	1.35	1.02	24.1
100	1.35	1.08	27.3
125	1.34	1.05	30.2

This is in accordance with reported Schottky rectifier on-resistance temperature dependence [1]. From the data of the Table 1, R_{on} was found to increase mònotonically with $T^{1.8}$ in agreement with the previous reported variations of $T^{1.6}$, $T^{2.0}$ and $T^{2.4}$ [1-3].

A useful figure of merit for rectifiers is the ON/OFF current ratio, which combines the current-carrying capability in forward bias with the leakage current in reverse bias [3]. The Ni/6H-SiC with an oxide ramp profile, annealed at 800^{0}C, has yielded ON/OFF current ratio between 10^4 (at 1V/-500V) and 10^6 (2V/-500V) at room temperature. In order to achieve a high current density at much lower forward voltage it is necessary to strengthen Schottky contact annealing. Fig. 6 shows typical forward characteristics measured at room temperature on the SBD with oxide ramp profile annealed at 800 °C and 1000 °C, respectively.

The voltage drop at high current density of 100 A/cm^2 is smaller of 1.5V after an annealing at 1000°C (Fig. 6). After this annealing a soft reverse current voltage curve and a very low breakdown voltage (<100V), has been achieved (Fig. 2). The ON/OFF current ratio also decreases.

4. CONCLUSIONS

A simple termination of the planar Schottky barrier structure was experimented and successfully tested for Ni/6H-SiC power diodes. The technique is based on oxide etching under small angles around the Schottky contact window. The MEDICI simulations showed that for smaller than 5° angles and oxide thickness over 1μm a parallel plan electric field vectors and an ideal volume breakdown are achieved. The simulation results. were experimentally checked on a Ni/6H-SiC Schottky barrier diode with about 4° ramp oxide profile and a 1.1μm oxide thickness.

Reverse characteristics showed near-ideal parallel plane breakdown at a voltage of 800V and very low leakage current after vacuum annealing of Schottky contact at 900°C for 2 min. A remarkable weak reverse current-voltage dependence for V_R>100V has been obtained. The forward characteristics of the Ni/6H-SiC SBD agreed very well thermoionic emission theory. The 800°C vacuum annealing led to devices with ideality factors near one and specific on resistance higher than theoretical value due to ohmic backside contact. By increasing the annealing temperature to 1000°C, the R_{on} is reduced but dramatic degradation of the breakdown voltage is observed.

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Lateral Current Spreading in SiC Schottky Diodes Using Field-Plate Edge Termination

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Keywords: Current Spreading, Edge Termination, Field-Plate, Forward Current Density, Schottky Diodes

Abstract

Increase in the forward current density in SiC Schottky diodes with field-plate edge termination is reported for the first time. The forward current density for a given forward bias is 2-3 times higher and the reverse breakdown voltage is ~ 2 times higher for Schottky diodes with field-plate edge termination as compared to unterminated Schottky diodes with a similar Schottky contact area. A possible model to explain the higher forward current density in Schottky diodes with edge termination is proposed based on the formation of an accumulation layer underneath the oxide layer resulting in lateral current spreading under forward bias.

Introduction

Edge termination techniques such as guard rings, field-plate (by metal overlap over an oxide layer), MESA, etc. are generally adopted for high voltage devices, in order to relieve the electric field enhancement around the contact periphery and thus obtain near ideal planar breakdown voltages [1,2]. The field-plate edge termination technique is probably the most commonly used technique due to its simple processing and effectiveness. While there are several publications [3,4] that describe the improvement in reverse breakdown voltage of Schottky diodes using field-plate edge termination, to the best of our knowledge, there is no work reported on the influence of the metal overlap edge termination on the forward characteristics of Schottky diodes. In this paper, we compare the forward J-V characteristics of P-type 6H-SiC Schottky diodes with and without edge termination to study lateral current spreading which results in a higher forward current density.

Experiment

Schottky diodes were fabricated on a p-type 6H-SiC wafer from Cree Research (substrate doping ~ $1.6\times10^{18}cm^{-3}$) with a 10 μm thick epilayer of ~ $6\times10^{15}cm^{-3}$ doping concentration. The 30-mm diameter wafer was cut into 8mm x 8mm square pieces to obtain several samples for experiments. The samples used in this experiment were selected from among that cut from the center of the wafer so as to assure relatively uniform material parameters. All samples were subjected to an oxidation etch (after ~ 2 hrs. of wet oxidation) and cleaned by the RCA procedure prior to diode fabrication. While unterminated Schottky diodes of 150 μm diameter [Fig. 1 (a)] were fabricated following conventional photolithographic process, Schottky diodes with oxide layer (field-plate) edge termination were fabricated based on a depo-conversion oxidation technique discussed in detail elsewhere [5,6]. After the fabrication of the diodes, their forward and reverse I-V characteristics were measured using a D.C voltage source (*Kiethley 237 High Voltage SMU*).

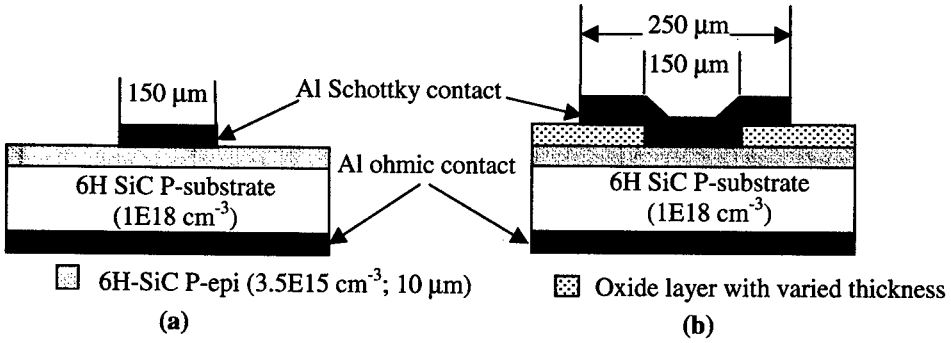

Fig.1. Cross section of Al/6H-SiC Schottky diode (a) without edge termination, and (b) with oxide edge termination.

Results and Discussion

(a) Forward J-V characteristics

In Fig. 2, the forward J-V characteristics of a P type 6H SiC Schottky diode without edge termination is compared to the J-V characteristics of a Schottky diode with an ~ 6000 Å thick oxide layer edge termination.

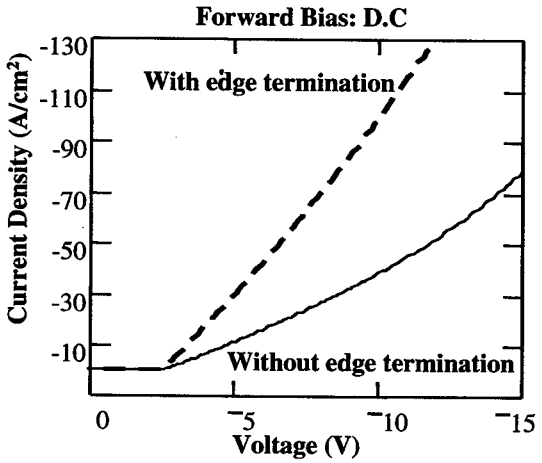

Fig. 2: Typical forward current density vs voltage (J-V) characteristics of a P type 6H-SiC Schottky diode with and without edge termination under D.C excitation.

It is clear from the above figure that the forward current density of Schottky diodes with ~6000 Å thick oxide edge termination is 2-3 times higher than that for un-terminated diodes. Hence for a given forward current, the forward voltage drop (V_F) is smaller for the diodes with edge termination compared to the diodes without edge termination. For example, at a current density of 50 A/cm^2 the forward voltage drop was V_F ~ -11.7 V for the diodes without edge termination, while it was V_F ~ - 6.5 V for the diodes with edge termination. The high forward voltage drop in these p-type SiC Schottky diodes can be attributed to the large series resistance ($R_{s,sp}$) of the epilayer and the substrate due to the low doping concentration and the large ionization energy of the dopant atom (Al) in SiC [7].

(b) Simulation of forward characteristics by ATLAS

The higher forward current density through the diode with edge termination is attributed to the formation of a low resistivity accumulation layer within the semiconductor. Under forward bias conditions, when a negative potential is applied to the Schottky contact, holes in the P-type epitaxial layer can accumulate at the semiconductor-oxide interface of the MOS structure surrounding the Schottky contact. Depending on the applied bias and the oxide thickness the concentration of majority carriers (holes) in this accumulation layer can be 2-3 times higher than the background dopant concentration. Since this low resistivity accumulation layer is in communication with the Schottky contact edge, it acts like a virtual contact increasing the effective current conduction area causing lateral current spreading as evident from the current density plot obtained using the ATLAS software from Silvaco, Fig. 3.

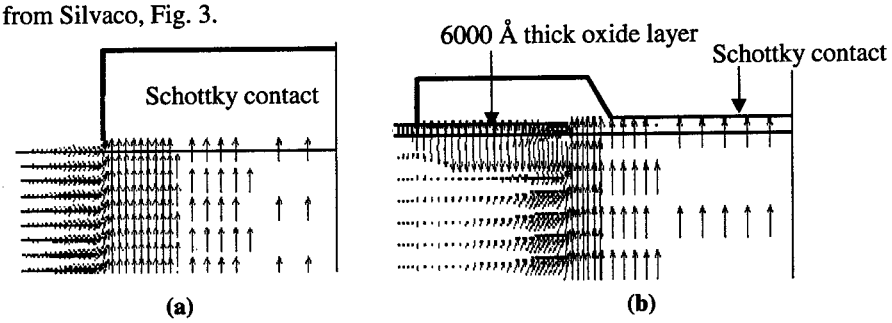

Fig. 3: Forward current density plot through a Al/SiC Schottky diode (a) without edge termination, and (b) with thick oxide edge termination, using ATLAS device modeling software.

The lower series resistance due to increased conduction area and the improvement in the current flow pattern with less current crowding at the Schottky contact periphery, will lead to higher forward currents and lower forward voltage drops in Schottky diodes with oxide edge termination. Simulation of forward J-V characteristics of the above un-terminated and oxide edge terminated Schottky diodes using ATLAS software confirms our hypothesis that lateral current spreading indeed results in higher forward currents (Fig. 4).

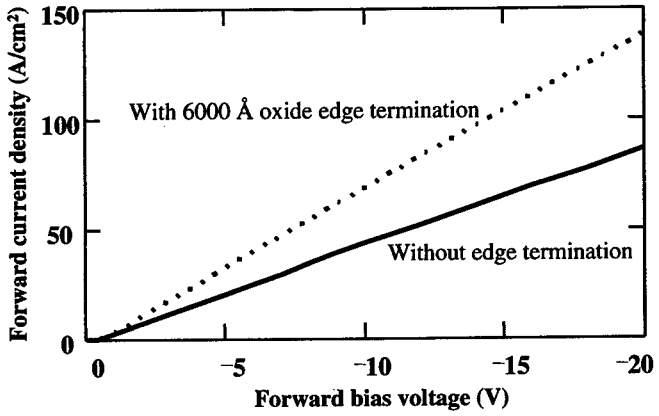

Fig. 4: Simulated J-V characteristics during forward bias of un-terminated and oxide edge terminated P-type 6H SiC Schottky diodes using ATLAS.

(b) Reverse J-V characteristics

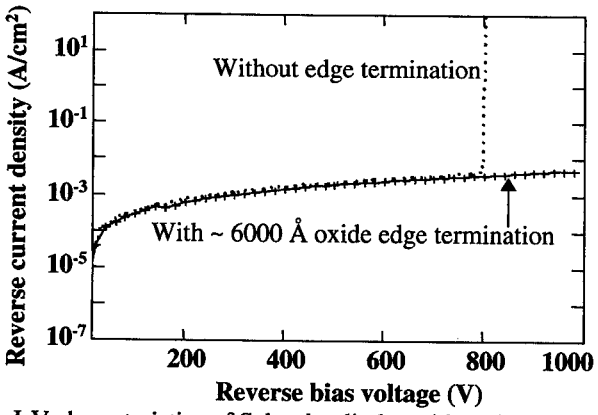

Fig. 5: Reverse J-V characteristics of Schottky diodes with and without edge termination.

In Fig. 5 the reverse J-V characteristics of an un-terminated P type 6H SiC Schottky diode is compared to that of a Schottky diode with a ~ 6000Å thick oxide layer edge termination. It is observed that the reverse breakdown voltage of Schottky diodes with edge termination is clearly larger than that of diodes without edge termination. Thus it is evident that the improvement in the forward J-V characteristics due to field-plate edge termination (Fig.2) does not compromise the generally expected increase in the reverse breakdown voltage due to field relief at Schottky contact periphery [6].

Conclusions

DC current-voltage (I-V) measurements on Schottky diodes with and without field-plate edge termination indicate that the oxide layer used for edge termination improves both the forward and reverse electrical characteristics. While other edge termination techniques such as guard rings, ion-implantation and MESA etching can also yield high reverse breakdown voltage [8], the formation of the accumulation layer under the oxide layer and the consequent increase in the forward current density is obtained only with a field-plate edge termination using metal-overlap over oxide layer.

Acknowledgements

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Characterization of Schottky Contact on p-type 6H-SiC

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Keywords: Barrier Height, Ideality Factor, Schottky Contacts

Abstract Schottky barrier height and other contact parameters of various materials (Al, Au, and Cu) on p-type 6H-SiC have been measured by using I-V and C-V techniques. The measured barrier heights were between 1.18eV and 2.87eV depending on the metal and measurement techniques used. Interfacial layers of different properties are assumed to be present, which result in different barrier heights measured by different techniques.

Introduction

Alpha (6H)-SiC is one of the most important polytype of this kind of semiconductor family and the progress has been made on this type of material. Schottky contacts have important effects on a variety of electronic and optoelectronic devices[1]. In this work, the electrical properties of different metal (Al, Au, and Cu) contacts to p-type 6H-SiC (0001) have been studied and the key parameters of the Schottky contacts have been measured by using I-V and C-V methods.

Experimental Methods

Schottky contacts were formed on commercially available p-type 6H-SiC wafers from Cree Research (research grade). The doping level was $\cong 8 \times 10^{17}$ cm^{-3}. In order to remove a surface natural oxide layer, SiC substrates were immersed in HF solution immediately before metal deposition. Au/Ge alloy was evaporated on the reverse side of the substrate to obtain a ohmic electrode. Au , Al or Cu was evaporated to form a Schottky electrode. The forward current-voltage characteristics measured at room temperatures leads to quantitative determination of Schottky diode parameters such as the Schottky barrier height and the ideality factor.

Results and Discussion

Figure 1 shows forward current-voltage characteristics for the fabricated Schottky contacts. Ideality factor and barrier height were estimated from linear portions in Fig. 1. The values are listed in Table 1. Figure 2 represents capacitance-voltage characteristics for the Schottky contacts of the same samples as that used in the I-V measurements. The frequency used in C-V measurement was 100kHz. The $(1/C)^2$-V plots show straight lines. The impurity concentration was determined from the slope of the line. The values are approximately $1.82\sim9.14\times10^{15}$ cm^{-3}, and are different from the data on the catalog. This may be because the quality of the substrate is "research grade". Table 1 shows ideality factor and barrier height calculated from Figs.1 and 2. The ideality factor was nearly equal to ideal value for Au and Cu, but fairly large for Al. For Al, the barrier height calculated from current-voltage characteristics was quite different from that calculated from capacitance-voltage characteristics. All barrier heights calculated from capacitance-voltage characteristics were higher than that measured from current-voltage characteristics.

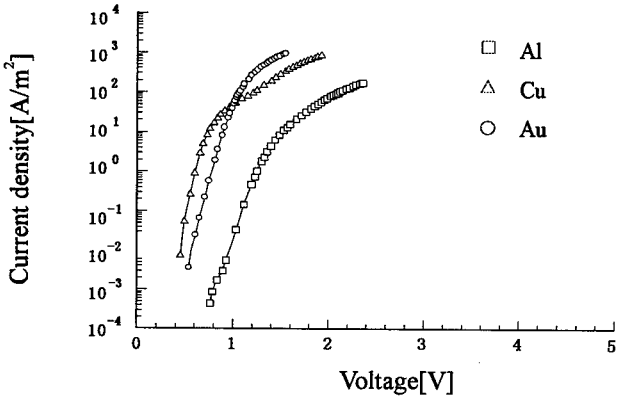


Fig. 1. Current-voltage characteristics of fabricated Schottky contacts

Table 1 : Ideality factor and barrier height

Metal	Ideality factor	Barrier height (I-V) [eV]	Barrier height (C-V) [eV]
Al	2.18	1.23	2.87
Cu	1.01	1.22	1.39
Au	1.51	1.18	1.45

The relation between barrier height and metal work function was not apparent in this work as shown

in Table 1. The device performance seemed to be determined by the property of the surface layer. The barrier height for Al probably indicates the presence of an additional oxide interfacial layer. Chemical composition near the interface was estimated by XPS measurement. Figure 3 shows the depth profile of atoms in the metal electrode. Oxygen was detected in Al/SiC contact shown in Fig. 3 (a). Evaporated Al atoms reacted with residual oxygen to form the oxidized layer, because the background pressure was about $2x10^{-5}$ Torr. No oxygen was detected in Au/SiC and Cu/SiC contact. Large n value seems to be caused from an oxidized layer near the interface. The presence of the oxidized layer also seems to result in the large diffusion potential of Al/SiC contact.

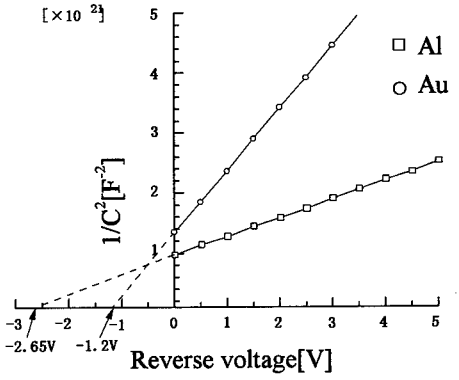
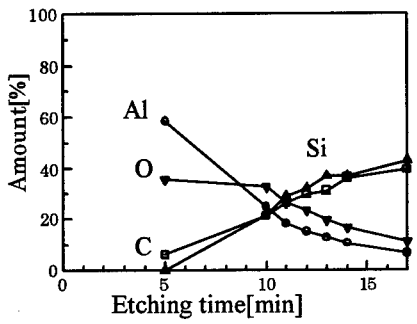
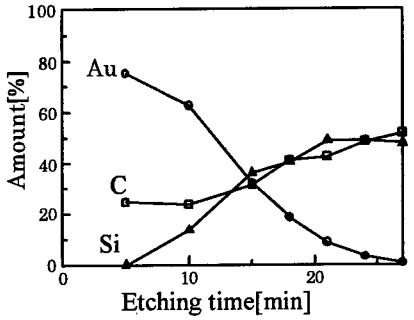


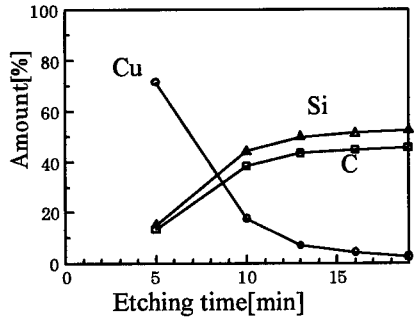
Fig. 2. Capacitance-voltage characteristics measured at 100kHz



(a) Al/SiC contact



(b) Au/SiC contact



(c) Cu/SiC contact

Fig. 3. Depth profile of atoms

Conclusions

The electrical properties of Al, Au, and Cu contact to p-type 6H-SiC have been characterized by means of I-V and C-V measurements and the key parameter of the Schottky contacts have been determined. The barrier height determined from I-V measurement was 1.23, 1.22 and 1.18 for Al/SiC, Cu/SiC and Au/SiC contact, respectively. An oxide layer was detected in Al/SiC contact by XPS measurement. Large n value of Al/SiC contact seems to be caused from an oxidized layer near the interface.

This work has been funded in part by Grant-in Aid for Scientific Research (C).

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Computer Simulation of p-type SiC Schottky Diode using ATLAS

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Keywords: ATLAS, Breakdown, Edge Termination, Field-Plate, Schottky Diodes

Abstract: The forward and reverse bias current density (J) vs voltage (V) characteristics of a P-type 6H SiC Schottky diode was simulated using ATLAS device modeling software from SILVACO. Based on the simulation results, the reverse breakdown voltage of a P-type 6H SiC Schottky diode with a 7000 Å thick oxide layer field plate edge termination was predicted. The measured J–V characteristics indicate a close match between experimental and simulation results, confirming the accuracy of the model.

Introduction

Most of the commercially available device modeling tools are tailored for Si device modeling by incorporating key material parameters and empirical or theoretical descriptions of significant phenomena relating to Si. On the other hand, mathematical modeling of SiC devices is still in the developmental stage; not all phenomena are completely understood and some important parameters have not been measured. Due to significant differences in certain key parameters, such as the intrinsic carrier concentration between Si ($n_i \sim 10^{10}$ cm^{-3}) and SiC ($n_i < 10^{-6}$ cm^{-3}), some of the techniques developed for simulation of Si devices may not be appropriate for devices made from SiC. In this context, we describe a modeling philosophy based on combining experimental results with traditional physics-based modeling to create a semi-empirical model that gives a good match between experimental and simulation results of P-type SiC Schottky diodes.

Modeling Approach

Due to the inherent complexities in predicting the nature of the metal-semiconductor Schottky contact [1], our approach in modeling the SiC Schottky diode was to avoid trying to model the barrier directly. Instead, we chose to adjust two of the modeling parameters so that the calculated J-V characteristics would match the measured J-V characteristics of the device.

Since ATLAS treats the metal contact as a boundary condition for solving the Poisson's equation during the simulation of a Schottky contact, we chose the work function of the metal contact, ϕ_m, as the first adjustable parameter. In ATLAS, the barrier height ϕ_b is determined from ϕ_m using Eq. 1 given below:

$$\phi_b = \chi_s + \frac{E_g}{q} - \phi_m \qquad (1)$$

where, χ_s is electron affinity; and E_g is bandgap of semiconductor.

The non-ideal barrier height ϕ_b* observed in real devices is introduced into the model by replacing ϕ_m with an effective value ϕ_m*, which produces the proper barrier height and reverse saturation current to match the experimental results. The correct value of ϕ_m* was found from the

reverse saturation current density J_{ss}, obtained from the measured reverse J-V characteristics by extrapolating a ln(J) vs V plot to V=0. The intercept of this line is ln(J_{ss}), from which ϕ_b* and ϕ_m* is computed. This process results in a good fit between the simulated and actual J-V characteristics.

In order to simulate the breakdown phenomena we enabled the Selberherrs model in ATLAS for determining the electron-hole pair generation rate by impact ionization. According to the Selberherrs model the electric field dependence of the electron/hole ionization rates is given by [2]:

$$\alpha_{n,p} = A_{n,p} \exp\left[-\left(\frac{b_{n,p}}{E}\right)^{m_{n,p}}\right] \qquad (2)$$

Where E is the electric field strength across the depletion region, A_n, A_p, b_n, b_p, m_n, m_p are constants. While the values of A_n, A_p, b_n, m_n and m_p were not changed from the default values in ATLAS, the value of the ionization coefficient b_p was adjusted until a good match was obtained between the experimental and the simulated J-V characteristics (upto reverse breakdown) for an un-terminated diode. The breakdown voltage of a Schottky diode with a 7000 Å thick oxide edge termination was predicted by simulating the J-V characteristics using the optimized ϕ_m and b_p values.

Results

High voltage Schottky diodes were fabricated on a P-type 6H-SiC wafer from Cree Research (substrate doping ~ 1.6×10^{18}cm^{-3}) with a 10 µm thick epilayer of ~ 1×10^{16}cm^{-3} doping concentration. The Schottky contacts were formed by Al deposition by thermal evaporation in high vacuum (<10^{-5} Torr). Both un-terminated Schottky diodes and diodes with a thick oxide (~ 7000 Å) edge termination were fabricated and their forward and reverse I-V characteristics were measured using a Kiethley 237 High Voltage Source Measure Unit.

(a) *Barrier height (ϕ_b) adjustment*

For preliminary simulations using ATLAS, the work function for the Al Schottky contact was set to the default value of ϕ_m = *4.1 eV*, corresponding to a barrier height of ϕ_b ~ *3.0 eV*. As seen from Fig. 1(a), the simulation of an un-terminated SiC Schottky diode using this ϕ_b value did not match the J-V characteristics from experimental measurements. The simulated current density in the reverse regime was several orders of magnitude below the actual values.

To improve the agreement between the simulation and the actual device, an *apparent barrier height ϕ_b**, was calculated from the experimental J-V characteristics considering a reverse saturation current density of J_{ss} ~ 2.5 x 10^{-5} A/cm^2.

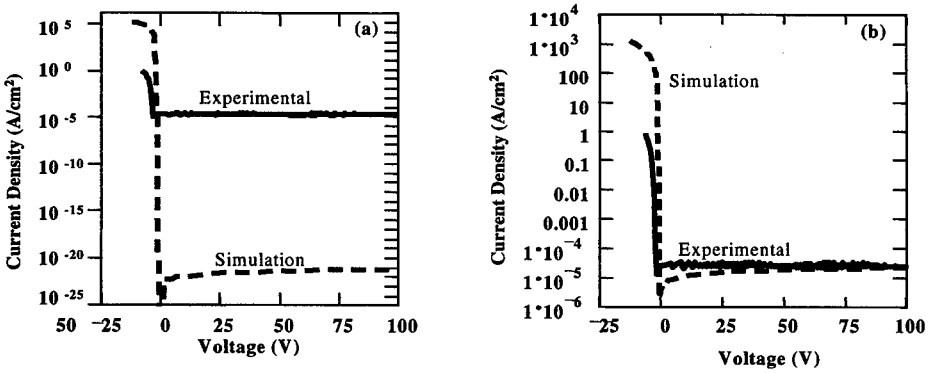

Fig.1: Comparison of simulated and measured J-V Characteristics of an un-terminated P-type 6H SiC Schottky Diode, (a) obtained using the default value of Al work function giving ϕ_b ~ 3 eV; (b) using a corrected value of Al work function giving ϕ_b* = 0.7 eV.

The extracted value of $\phi_b^* = 0.7$ eV was used to calculate the effective metal work function $\phi_m^* = 6.4$ eV, that was used to set the boundary conditions in ATLAS for a new simulation. The simulated J-V characteristics of an un-terminated P-type 6H SiC Schottky diode, after changing the metal work function to $\phi_m^* = 6.4$ eV, is shown in Fig. 1(b). The simulated and actual reverse characteristics now show good agreement. The reverse saturation current densities were relatively close, 2.3×10^{-5} A/cm^2 for the simulation versus a measured value of 2.5×10^{-5} A/cm^2.

(b) *Adjustment of* b_p

After obtaining a good match between the simulated and experimental reverse saturation current densities, the b_p value over a region extending from the SiC surface to a depth of ~ 1 μm was adjusted to obtain a good match between the simulated and experimental breakdown voltages of an un-terminated diode. It was observed that the breakdown voltage decreases progressively with decrease in b_p and for b_p ~ 9.3 MV/cm, the simulated breakdown voltage (V_b = 480 V) matches closely with the experimentally measured value of approximately 500 V for an un-terminated Schottky diode. Now the reverse breakdown characteristics of a P-type 6H SiC Schottky diode with a 7000 Å thick oxide edge termination was simulated using $\phi_b^* = 0.7$eV and $b_p = 9.3$ MV/cm. In Fig. 2 the simulated and experimental results are compared for both un-terminated and terminated Schottky diodes. It is noteworthy that though the simulations were calibrated using the un-terminated diode, the simulated breakdown voltage V_{sim} ~ 1130 V (predicted value) for the diode with edge termination, compares reasonably well with the measured (DC) value of V_{exp} ~ 1060 V.

Discussion

As evident from Fig. 2, the introduction of a field-plate surrounding the Schottky contact periphery significantly improves the reverse breakdown voltage of the P-type SiC Schottky diode [3]. The simulation results using ATLAS indicate that the improvement in the breakdown voltage is primarily due to the field relief at the Schottky contact periphery provided by the field plate, by shifting the high field region into the oxide near the edge of the metal-overlap.

The comparison of electric field values at the Schottky contact periphery for the un-terminated and terminated Schottky diodes, shown in Fig. 3 (a), indicates that the field plate results in ~35% reduction in the peak electric field. Since the avalanche breakdown voltage is extremely sensitive to the electric field value, the above field reduction is sufficient to increase the breakdown voltage for the terminated diodes. Moreover, while the location of the high field region is within the semiconductor near the Schottky contact edge in the case of un-terminated Schottky diodes, the high field region is located in the oxide layer near the edge of the metal-overlap in the case of the terminated diodes, Fig. 3 (b,c).

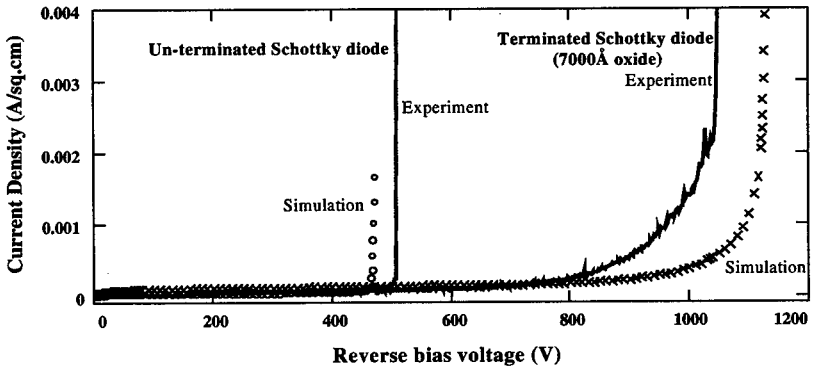

Fig. 2: Comparison of simulated and experimentally observed reverse breakdown characteristics for un-terminated and oxide edge terminated P-type 6H SiC Schottky diodes.

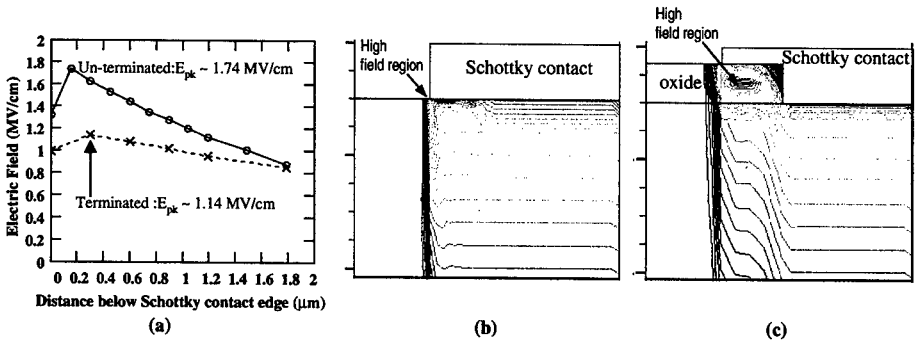

Fig. 3: (a) Comparison of electric field values at the Schottky contact periphery of a P-type 6H SiC Schottky diode without edge termination and with a 7000 Å thick oxide edge termination, at 400 V reverse bias; and, location of the high field regions in (b) un-terminated, and (c) terminated Schottky diodes.

The influence of the field-plate on the breakdown voltage was observed to be dependent on the extent of metal-overlap over the oxide layer. As seen from Fig. 4, the breakdown voltage increases progressively with increase in the overlap until the overlap is approximately equal to the epi-layer thickness. An overlap greater than the epi-layer thickness does not result in any significant improvement in the breakdown voltage.

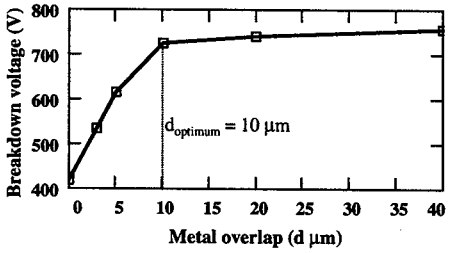

Fig.4: Dependence of reverse breakdown voltage on metal overlap distance (d) for a P-type 6H SiC Schottky diode with 7000 Å thick oxide edge termination (epi-layer thickness = 10μm).

Conclusions

Simulation of J-V characteristics of un-terminated and oxide edge terminated P-type 6H SiC Schottky diodes using ATLAS indicates significant improvement in the reverse breakdown voltage due to field relief at the Schottky contact periphery. A good match between experimental and simulated J-V characteristics was obtained by adjusting the barrier height (ϕ_b) and critical field parameter (b_p) values. In order to obtain a high reverse breakdown voltage the optimum metal overlap for the field-plate was found to be approximately equal to the epitaxial layer thickness.

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Schottky Barrier Characteristics of 3C-SiC Epilayers Grown by Low Pressure Chemical Vapor Deposition

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Keywords: 3C-SiC, LPCVD, Schottky Barrier Characteristics

ABSTRACT. We have developed a low pressure chemical vapor deposition (LPCVD) method and successfully obtained layers with atomically flat surfaces. We fabricated Schottky barrier structures using these epilayers and investigated the junction properties by measuring current-voltage (I-V) characteristics. We obtained excellent Schottky barrier junctions with the ideality factor of 1.11 and the reverse breakdown voltages of 240 V, which is two orders of magnitude higher compared with that of atmospheric pressure CVD (APCVD) epilayers.

1. INTRODUCTION

Silicon carbide (SiC) is a promising semiconductor for high power, high frequency and high temperature electronic devices due to its excellent physical and chemical properties. SiC has many polytypes. Among them, 3C-SiC has some advantages compared with other SiC polytypes, such as the highest mobility and ease in designing devices because of its isotropic physical properties. We have studied the 3C-SiC heteroepitaxial growth on Si substrates using atmospheric pressure chemical vapor deposition (APCVD) method. However, the epilayers grown by APCVD have many protrusions on the surfaces and poor surface morphology as shown in Fig. 1 (a). Therefore, APCVD 3C-SiC epilayers could not realize practical Schottky barrier diodes with high reverse breakdown voltages, which was no more than several voltages [1]. This can partly be attributed to the rough surfaces of APCVD epilayer as displayed in Fig. 1 (a). To overcome the problems of 3C-SiC epilayers grown by APCVD method, we have tried to grow SiC by low pressure CVD (LPCVD), and successfully obtained atomically flat surfaces without protrusions as shown in Fig 1 (b) [2]. Moreover, the obtained epilayers were antiphase domain (APD) free and the etch pit densities were in the order of 10^4 cm^{-2}, which is 4 order of magnitude smaller than those of APCVD epilayers [3]. In this report, we study the characteristics of the Schottky barrier diodes fabricated on the LPCVD epilayers and show the great improvement in the junction characteristics.

2. EXPERIMENTS

3C-SiC single crystal films were epitaxially grown on n type on-axis Si (001) substrates of 61 $\times$76 mm^2 by LPCVD using a silane-propane-hydrogen reaction gas system. The details of the growth have been described elsewhere [2]. The unintentionally doped epilayers show n-type conduction. We used 3C-SiC epilayers of over 10 μm thickness, because epilayers with single

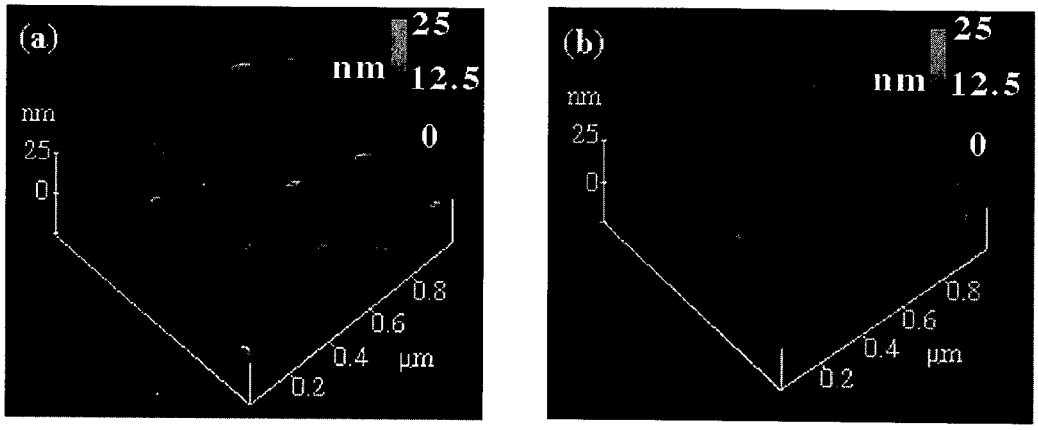

Fig. 1. Atomic force microscope (AFM) images showing surface morphologies of the 3C-SiC epilayers grown by : (a) APCVD; (b) LPCVD.

domain can be obtained for more than 5 μm thick growth of SiC on Si by LPCVD method despite using on-axis Si substrates [3]. Before the Schottky-electrode fabrication, the epilayers were oxidized at 1100 °C to make oxide layers of 50 nm in thickness and the oxide layers were subsequently etched by HF solution. Then, the epilayers were soaked in 20% K_2CO_3 at 80 °C for 2 hours to remove defect layers, and were dipped in diluted HCl for 10 min to neutralize a residual base. Schottky electrodes of Au or Ni thin films with 0.1-0.2 mm in diameter and 50 nm in thickness were produced on the 3C-SiC surfaces by vacuum evaporation. Ohmic electrodes were formed on the back surfaces of n-type Si substrates by vacuum evaporation of Al. The current-voltage (I-V) characteristics of the Schottky barrier contacts were measured using a curve tracer and a pA-meter/DC-voltage- source (HP 4140B) at room temperature. The capacitance-voltage (C-V) measurement was carried out at frequency of 1 MHz using a C-meter (HP 4280A).

3. RESULTS and DISCUSSION

An example of the voltage dependence of the Au/n-type 3C-SiC diode capacitance is shown in Fig. 2. It can be seen in the figure that the plots of $1/c^2$ against voltage are almost on a linear line, and thus the depth profile of the carrier concentration calculated from the plots in Fig. 2 is uniform. The value of the carrier concentration was about 5.0×10^{15} cm^{-3}. The barrier height can be obtained from the expression

$$\Phi_B = V_i + \xi + k_BT/q - \Delta\Phi$$

where V_i is the intercept of the extrapolated $1/C^2$ vs V curve with the voltage axis, ξ the difference between the conduction-band edge and the Fermi level, k_bT the thermal energy and $\Delta\Phi$ the image force lowering of the Schottky barrier. The value of V_i we obtained was 1.11 V. At room

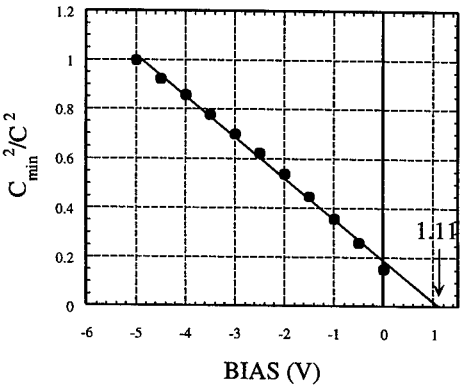

Fig. 2. Capacitance-Voltage characteristics of a reverse biased Au/3C-SiC Schottky barrier contact.

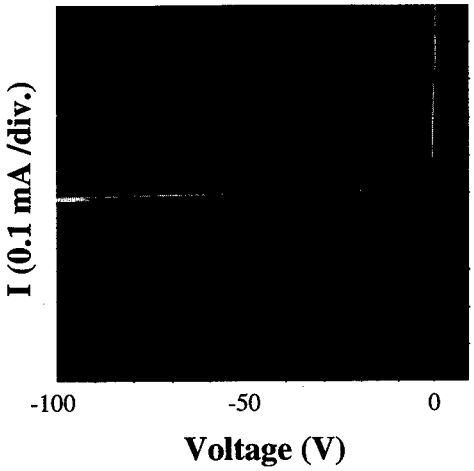

Fig. 3. Current-Voltage characteristic of a Ni/3C-SiC Schottky barrier diode.

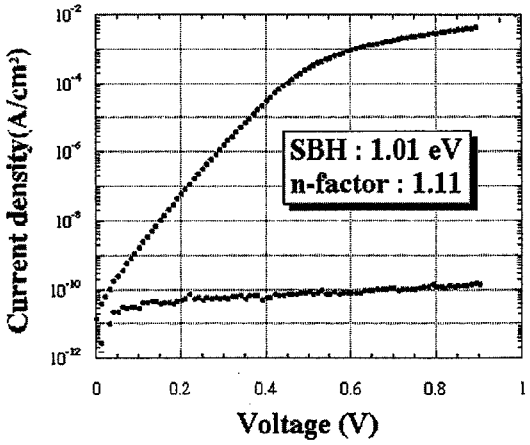

Fig. 4. Current density-voltage characteristic of an Au/3C-SiC Schottky barrier contact.

temperature, the values of ξ, k_BT/q and $\Delta\Phi$ were calculated to be 0.17, 0.03 and 0.03, respectively, based on a carrier concentration obtained from the slope in Fig. 2. Therefore, the barrier height calculated from C-V measurement was 1.28 V.

Figure 3 shows a typical current-voltage (I-V) characteristic of a Ni/n-type 3C-SiC diode. The diode was exhibited good I-V characteristics with a high reverse-biased curve. The reverse breakdown voltages were in the range of 200-240 V for the Ni electrode case and 140-180 V for the Au electrode case. These value are the highest among those reported in Schottky barrier diodes of 3C-SiC hetero-epilayers grown on Si (001) [4,5], and two orders of magnitude higher compared with those of APCVD epilayers [1].

The logarithmic plot of current density against applied voltage for an Au / n-type 3C-SiC diode is shown in Fig. 4. The forward I-V characteristic of Schottky diodes is generally described with the well known equation,

$$I = A^* S T^2 \exp(-q\Phi_B/k_BT) \{\exp(qV/nk_BT) - 1\}$$

from the thermionic emission theory, where S is the contact area, A* the Richardson constant, Φ_B barrier height and n the ideality factor. We calculated the ideality factor and the barrier height from Fig. 3 using this equation. The forward characteristic showed over 5 decades of linearity with an ideality factor of 1.11. The barrier height was determined from the forward I-V plots to be 1.01 eV. Figure 5 shows AFM image of LPCVD epilayers having enlarged vertical axis compared with that of Fig. 1(b). The root-mean-square roughness was 0.153 nm, which exhibits that the surface of LPCVD epilayer is atomically flat. These results indicate that the improvement of surface morphology as shown in Fig. 1 and 5 is effective

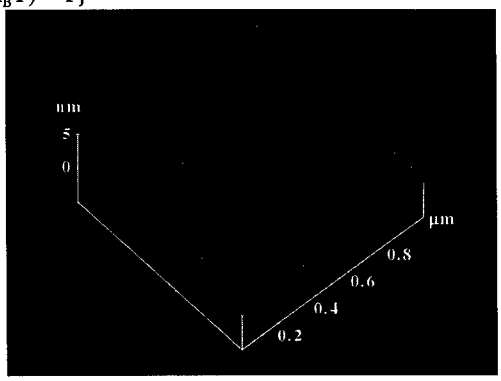

Fig. 5. Atomic force microscope (AFM) images showing surface morphologies of the 3C-SiC epilayers grown by LPCVD. The root-mean-square roughness was 0.153 nm.

to improve Schottky barrier junction characteristic.

However, the reverse leakage current density was in the order of 10^{-1} A/cm^2 at reverse bias of 100 V. Regarding the reverse breakdown voltages, the values of about 200 V are one order of magnitude smaller than 6H and 4H Schottky diodes. Though we obtained APD free and atomically flat epilayers by LPCVD method, those epilayers contained many macro steps [2, 3]. Bahng *et al.* have reported that multi twin bands along {111} faces exist in these steps [6]. Moreover, the density of etch pit which is thought to originate from the stacking faults and the dislocations [7] was still at 10^4 cm^{-2} order. It has pointed out that the stacking faults affect strongly on the reverse current properties of Schottky barrier junction. Twin bands are also considered to affect those. We used the electrodes of 0.1 mm in diameter. In this size, the defect free area can not be obtained for the epilayers with the defect density of 10^4 cm^{-2}. Therefore, it is seemed that the large leakage current and the low break down voltage are due to the high densities of stacking faults and twin bands in the epilayers.

4. CONCLUSION

We have successfully obtained 3C-SiC heteroepitaxial layers with atomically flat surfaces using LPCVD method and fabricated Schottky barrier diodes using the epilayers and showed the reverse break down voltage of 240V and the ideality factor of 1.11. These results indicate the great improvement in the junction properties compared with those using APCVD epilayers.

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Characterization of Au Schottky Contacts on p-type 3C-SiC Grown by Low Pressure Chemical Vapor Deposition

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Keywords: 3C-SiC, Low Pressure CVD, p-Type, Schottky Barrier Height, Schottky Contacts

Abstract: Gold (Au) Schottky barrier contacts have been fabricated on p-type 3C-SiC films, which were epitaxially grown on Si substrates by low pressure chemical vapor deposition (LPCVD) method. The Schottky barrier height was experimentally obtained by current-voltage, capacitance-voltage and x-ray photoemission spectroscopy measurements to be 1.12 ± 0.12 eV, 1.11 ± 0.18 eV and 1.40 ± 0.15 eV.

1 Introduction

Silicon carbide (SiC) is considered a suitable material for high frequency, high power, high temperature and radiation resistant devices. For the development of Schottky-based SiC devices such as high voltage and high frequency rectifiers, it is important to fabricate Schottky contacts with quite good electrical characteristics. Recently, the electrical characteristics of Schottky contacts on hexagonal type SiC have been studied by many researchers[1]. Concerning Schottky contacts on cubic type SiC (3C-SiC), excellent rectifying characteristics using n-type crystals have been reported[1-3]. However, there are only a few reports regarding Schottky contacts on p-type 3C-SiC[4, 5].

In the present study, we have grown high quality p-type 3C-SiC epilayers by low pressure chemical vapor deposition (LPCVD) and fabricated Au Schottky contacts on the p-type 3C-SiC. The electrical characteristics of the Schottky contacts have been investigated.

2 Experiments

Heteroepitaxial growth of p-type 3C-SiC films were performed on 3-inch Si (001) substrates by LPCVD. A vertical quartz reactor with a water-cooled cold wall was used in our CVD apparatus. The gases of SiH_4 and C_3H_8 were used as source gases, and H_2 refined by a purifier was used as a carrier gas. Prior to the growth, Si substrates were carbonized with C_3H_8 at 1300°C and 100 Torr for 5 minutes. After the carbonization, the growth of 3C-SiC films were carried out at the gas flow rates of H_2, SiH_4 and C_3H_8 were 2.0 slm, 0.50 sccm and 0.52 to 0.55 sccm, respectively, where the growth temperature and the reactor pressure were 1300°C and 100 Torr, respectively. During the growth, Al impurities were doped using a chemical reaction of Alumina and graphite. As a result, we have grown p-type 3C-SiC epilayers with thicknesses of 7, 12 and 18 μm. Details of the growth procedures have been described elsewhere[6]. The carrier concentration and the Hall mobility of holes in the epilayers were obtained to be (1 to 5) x 10^{16} cm^{-3} and 10 to 30 cm^2/Vs, respectively, by Hall effect measurements at room temperature (RT).

Prior to the formation of Schottky contacts, the surface of 3C-SiC film was degreased in ethanol and etched in sequence with 1% HF for 5 min, 40 % K_2CO_3 at 85°C for 120 min, 10% HCl for 5 min and 5% HF for 5 min[3]. After these processes, Au was deposited on the epilayer surface at RT

to form gate electrodes. The diameter and the thickness of gate electrodes were 200 μm and 100 nm, respectively, for electrical measurements. For fabricating the ohmic contacts, Ti was deposited on the sample surface near the gate electrodes. Thereafter, Al was deposited on the Ti contacts to avoid the oxidation of Ti contacts. An Al electrode was also fabricated on the backside of the Si substrate to make an ohmic contact. The Schottky contacts on p-type 3C-SiC were characterized by current-voltage (*I-V*), capacitance-voltage (*C-V*) and x-ray photoemission spectroscopy (XPS) measurements. For XPS measurements, Au with a thickness of 20Å was deposited on the whole surface of 3C-SiC samples.

3 Results and discussion

Figure 1 shows a typical *I-V* characteristic for the Au/p-type 3C-SiC Schottky contacts. The thickness of this 3C-SiC film is 7 μm. A rectifying characteristic is clearly observed in this figure. In the positive voltage side, the soft breakdown occurs around 10 V and the breakdown takes place at 26 V. The leakage current at 26 V is approximately 2.7 μA, which is much smaller than those reported previously [4, 5]. This implies that high quality of Au Schottky contacts is achieved. The turn on voltage is about -1V.

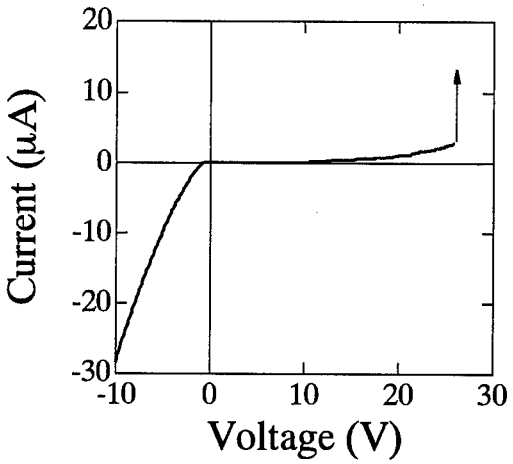

Fig. 1 *I-V* characteristic for Au/p-type 3C-SiC Schottky contacts.

Figure 2 shows a semilogarithmic plot of current density (J) versus forward voltage (V). The barrier height (ϕ_B) of Au Schottky contacts and the ideal factor (n) can be derived from a linear part of the log(J)-V curve. Here, the current density in the linear part is given by following equation;

$$J = J_s \exp(qV / nk_BT), \quad (1)$$

where J_S is the saturation current density, k_B Boltzmann's constant, and T absolute temperature. From a fitting using Eq. (1) to the *J-V* data in a forward voltage range from 0.3 to 0.7 V, n is estimated to be 1.24. This value is comparable with those reported for the Au Schottky contacts on 6H- and 4H-SiC[1]. The value of J_S is also estimated to be $9.7\text{x}10^{-14}$ A/cm^2 from the J value at the intersection between the Y-axis (V=0) and the fitting line.

The barrier height (ϕ_B) of Schottky contact is related to the saturation current density (J_S) by

$$\phi_B = k_BT / q\ln(A^*T^2 / J_s), \quad (2)$$

where $A^*=(m^*/m_0)A$, and m^* and A are the effective hole mass and Richardson constant, respectively. In this analysis, we employ $m^*=0.8m_0$[7]. The Schottky barrier height of this

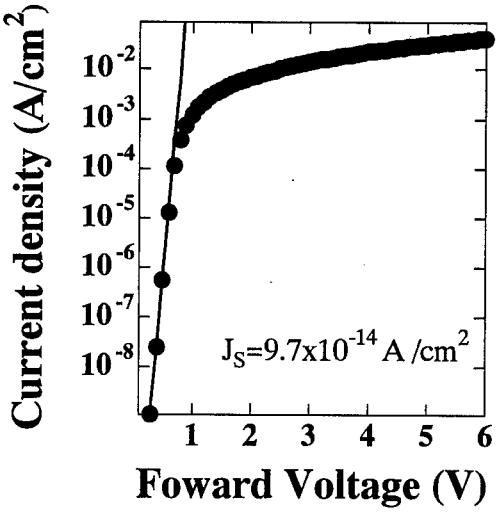

Fig 2 Semilogarithmic plot of current density versus forward voltage for Au/p-type 3C-SiC Schottky contact. The solid line represents the fitting result obtained using Eq. (1).

sample is estimated to be 1.19 eV.

We have measured *I-V* characteristics for various Au/p-type 3C-SiC Schottky contacts. The maximum breakdown voltage is obtained to be 42 V for the 18 μm thick 3C-SiC. The average value of the barrier height for Au/p-type 3C-SiC Schottky contacts is derived to be 1.12 ± 0.12 eV.

The barrier height of Schottky contacts can be also determined by *C-V* measurements. Figure 3 shows an example of *C-V* curves for the Au/p-type 3C-SiC Schottky contacts. In this figure, the plot is almost linear in a bias voltage range from -1.5 V to -0.7 V, but deviates from the linear relationship at bias voltages higher than - 0.7 V. This deviation can be explained by the assumption that the space charge remains at the metal/semiconductor interface. At bias voltages lower than -1.5 V, the capacitance could not be measured owing to a large leakage current. From the linear part of the data in Fig. 3, the net acceptor concentration in this sample is obtained to be about 5.0 x 10^{17} cm^{-3}. This value agrees well with that estimated from the carrier concentration obtained by Hall effect measurements and the ionization energy of Al acceptor in 3C-SiC (160meV)[8].

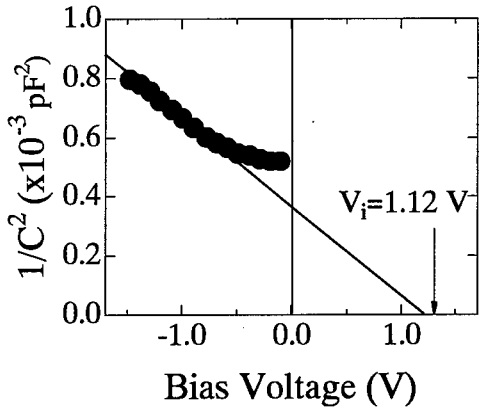

Fig. 3 *C-V* characteristics of a reverse-biased Au/p-type 3C-SiC Schottky diode. The sold line represents the liner curve fitted between -1.5 V and -0.7 V.

The barrier height is expressed as[3]

$$\phi_B = V_i + \zeta + k_B T / e - \Delta\phi, \qquad (3)$$

where V_i is the intercept voltage of the extrapolated $1/C^2$ vs V curve obtained by the *C-V* curve. The value of ζ is the energy difference between the Fermi level and the edge of the valence band, and $\Delta\phi$ the image force lowering of the barrier height at the interface. The value of V_i for this sample is 1.12 V. Therefore, the barrier height estimated from the *C-V* data in Fig. 3 is 1.14 eV. We have also measured *C-V* characteristics for various Au/p-type 3C-SiC Schottky contacts, and obtained the barrier height of 1.11 ± 0.18 eV. This value is in good agreement with that obtained from the *I-V* measurements.

Figure 4 shows the C1s core level peaks of XPS spectra of SiC observed from before and after deposition of Au. The relationship among the C1s binding energy measured with XPS (E_{C1s}), the interface Fermi energy (E^i_F) and the barrier height (ϕ_B) is shown in the inset. For p-type semiconductors, E^i_F is equal to ϕ_B. Thus ϕ_B is expressed as[9]

$$\phi_B = E^i_F = E_{C1s} - (E^*_{C1s} - E_v), \qquad (4)$$

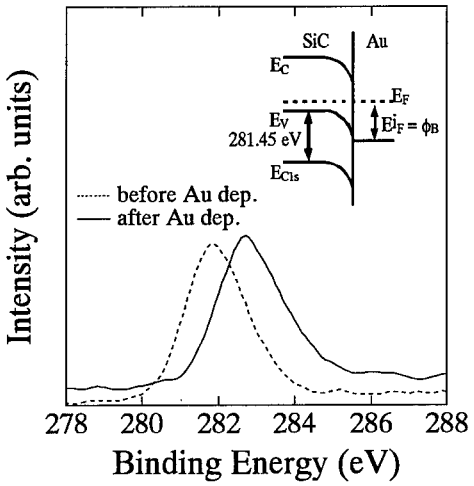

Fig. 4 XPS C1s core level spectra for the 3C-SiC surface. The solid and dotted lines represent the spectra obtained before and after deposition of thin Au, respectively. The inset shows the relationship between ϕ_B and C1s binding energy.

where E^*_{C1s} and E_v represent the C1s and the valence band edge binding energy in 3C-SiC before Au deposition. Therefore, $(E^*_{C1s}-E_v)$ is the C1s to valence band edge binding energy difference in 3C-SiC. Since the value of $(E^*_{C1s}-E_v)$ is a bulk material constant, we use the value of 281.45 eV reported previously for $(E^*_{C1s}-E_v)$[9]. In Fig. 4, the C1s core level peak shifts to 282.7 eV by the Au deposition because the band bending is caused by the formation of Au Schottky barrier. The Schottky barrier height of the Au/p-type 3C-SiC is estimated to be 1.25 eV using Eq. (4). This value is close to the ϕ_B values obtained from the *I-V* and *C-V* measurements. We have performed XPS measurements for the various Au/p-type 3C-SiC Schottky contacts. The barrier height is estimated to be 1.40 ± 0.15 eV.

The barrier height of Au/n-type 3C-SiC was reported to be 1.15 ± 0.15 eV[3]. The energy band gap of 3C-SiC at RT is 2.2 eV. The difference between these values is 1.05 ± 0.15 eV, which agrees well with the ϕ_B values obtained by *I-V*, *C-V* and XPS measurements. This fact indicates that the obtained ϕ_B values are reasonable for the barrier height of Au Schottky contacts on p-type 3C-SiC, and that the crystal quality of LPCVD grown p-type epilayers is high enough to form Schottky contacts.

4 Summary

We have grown p-type 3C-SiC epilayers by LPCVD and characterized Au Schottky contacts on the p-type epilayers. Excellent *I-V* characteristics are obtained for the Au Schottky contacts. The maximum breakdown voltage and the best ideal factor are 42 V and 1.24, respectively. The barrier heights of 1.12 ± 0.12 eV, 1.11 ± 0.16 eV and 1.40 ± 0.15 eV are estimated from the *I-V*, *C-V* and XPS measurements, respectively. These values are reasonable for the barrier height of Au Schottky contacts on p-type 3C-SiC. The obtained results indicate excellent quality of p-type 3C-SiC is grown by LPCVD.

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Static and Dynamic Characteristics of 4H-SiC JFETs Designed for Different Blocking Categories

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Keywords: Device Simulation, JFET, Mobility, Switching Characteristics, Temperature Dependence

Abstract

In this work vertical 4H-SiC power JFETs are presented. The structure consists of two parts, a first, thick epitaxial layer supporting the desired breakdown voltage and a thin head region implemented in a second epitaxial layer on top of the first one, responsible for controlling the device. Sample sets have been fabricated with blocking voltages from 600V, 1200V to 1800V and an active area of 2,3mm². The devices exhibit stable avalanche breakdown and are rugged under short circuit conditions in the order of several milliseconds. Due to the unipolar conduction mechanism, high switching speeds can be achieved. The temperature dependence of the on-resistance can be modeled on the basis of the temperature dependence of the electron mobility and follows a $R_{on} \sim T^{2,58}$ relation. The experimentally obtained results fit well to previous simulations.

Introduction

Various figures of merit, see e.g. [1], propose a large potential for Silicon carbide power switching devices in the medium and high voltage range particularly for power MOSFETs. These considerations are based mainly on silicon carbide's outstanding physical properties like, for instance, its high electric breakdown field. Especially the 4H-SiC polytype with its high and nearly isotropic electron mobility seems to be the material of choice for fast, low loss SiC MOSFETs suited for switching application between 600 and 1800V which is the voltage range used in state of the art driving applications. Today's experience with MOSFETs, however, shows that particularly for 4H-SiC such devices suffer from extremely low inversion layer mobilities so that the on-resistance of vertical 4H-SiC power MOSFETs is by orders of magnitude higher than theoretically predicted [2]. By means of other polytypes with smaller bandgaps, acceptable inversion layer mobilities can be achieved [2]. These polytypes, however, are either not available or their electron mobility is to small. Nevertheless, for power semiconductor devices with no surface channel like a vertical JFET, the device parameters become very attractive especially for 4H-SiC. The following work presents a vertical power JFET structure for different blocking voltages together with its static behavior at different temperatures as well as corresponding dynamic characteristics.

Device Concepts, Simulation and Technology

Fig. 1 shows a cross section of a half cell of our vertical JFET. The substrate material is n-type 4H-SiC from Cree with a specific resistivity between 16 and 20mΩcm. A first n-type epitaxial layer was grown onto the substrate by LPCVD [3]. A buried p-layer was implanted selectively into the first epitaxial layer. Then, a second layer of 2µm was grown forming the so-called head of the structure. At the top of the layer, the p-gate was implanted with aluminum. Several subsequent lithographic, dry etching and implantation steps for the source region and the electric connection of the buried layer defined the final layout shown in Fig. 1a). After annealing the implantations at

around 1700°C, nickel based contacts were deposited at the top (gate and source areas) and at the bottom (drain contact) of the wafers. In this type of device, the buried p-layer was electrically connected to the source resulting in a low Miller capacitance. The contacts were annealed at about 1000°C. An insulating oxide layer of 400nm was deposited via PECVD and opened in the gate pad and source area. Subsequently, an aluminum metallization of 3µm serving as a bond area was evaporated and patterned. The complete device consisted of 1452 parallel cells resulting in an active area of 2,3mm^2.

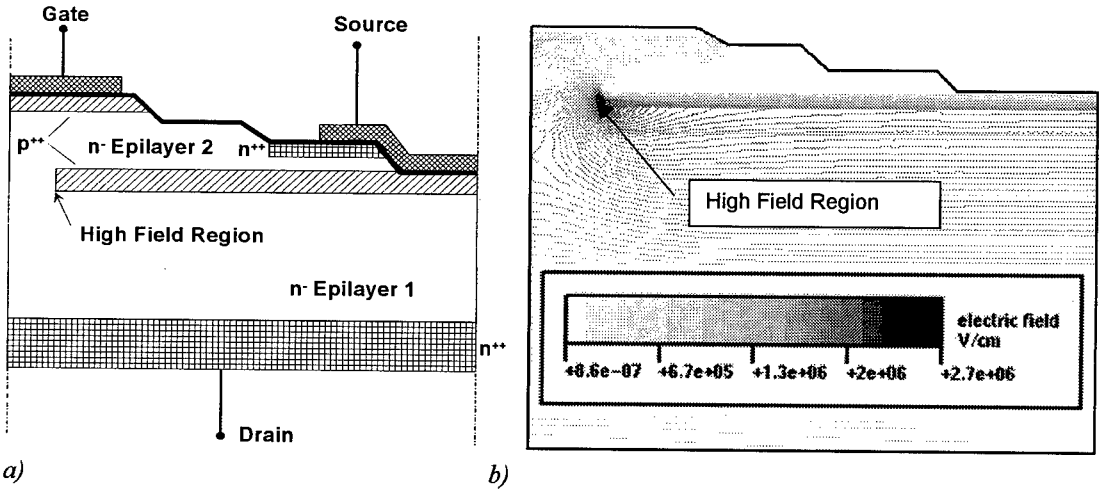

Fig. 1: a) cross section and b) simulated electric field distribution prior to breakdown for a vertical 4H-SiC VJFET

Doping and the thickness of the first epitaxial layer were adjusted according to the desired breakdown voltage; the parameters for epilayer 2 were the same for all blocking categories. It should be mentioned here that the data for the first epitaxial layer were gained from intensive simulation work (carried out with a DESSIS ISE ® [4]) since the breakdown of the structure is a two dimensional phenomenon and starts at the edge of the buried p-layer (see Fig.1b). Table 1 summarizes the parameters for the epilayers used for the three different devices.

Parameter /V_{BD}	$N_{D\,Epi1}$ (cm^{-3})	Thickness Epi $_1$ (µm)	$N_{D\,Epi2}$ (cm^{-3})	Thickness Epi $_2$ (µm)
600V	$1{,}2 \times 10^{16}$	9	$1{,}5 \times 10^{16}$	2
1200V	5×10^{15}	14	$1{,}5 \times 10^{16}$	2
1800V	3×10^{15}	23	$1{,}5 \times 10^{16}$	2

Table 1: Parameters for the epitaxial layers used in this work

Static characteristics at room temperature and at elevated temperatures

Fig. 2 shows the static behavior of JFETs with 600V, 1200V and 1800V blocking voltage. The forward characteristic shows that the on-resistance can be adjusted nearly independent of the blocking voltage. This behavior is due to the fact that in the conduction mode the voltage drop primarily occurs in the head region which is the same for all blocking categories. The specific on-resistance at room temperature ranges from 21.5 mΩcm² for the 600V device to 24.5 mΩcm² for the 1800V sample.

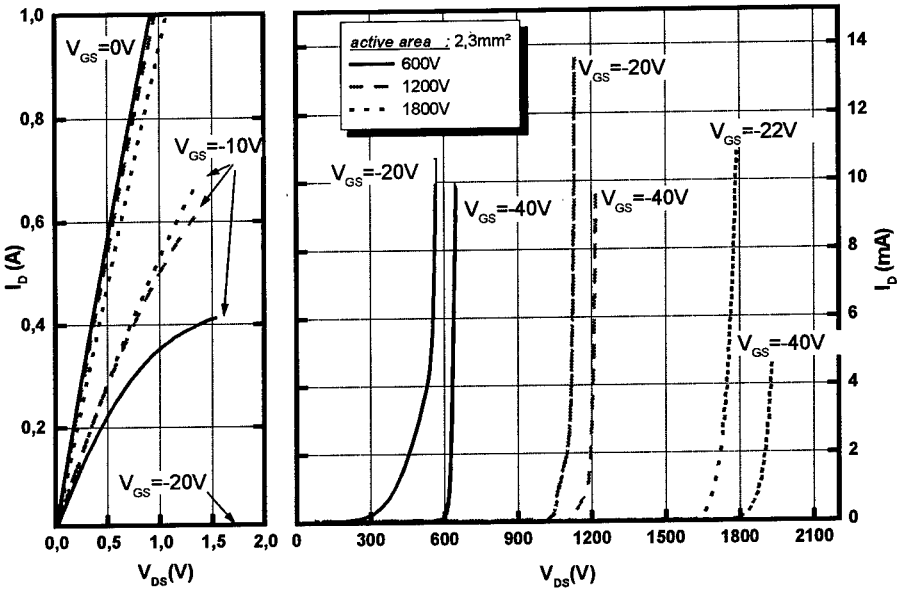

Figure 2: Static characteristic of VJFETs for 600V, 1200V and 1800V blocking voltage

In the blocking mode, the devices exhibit avalanche behavior with a current rating of more than 0.4 A/cm² corresponding to a power dissipation of about 500 W/cm² for, e.g, the 1200 V device. For increasing temperatures, the on-resistance increases as well like shown in Fig.3a.
Since the current through the device is governed by majority carriers, the temperature dependence

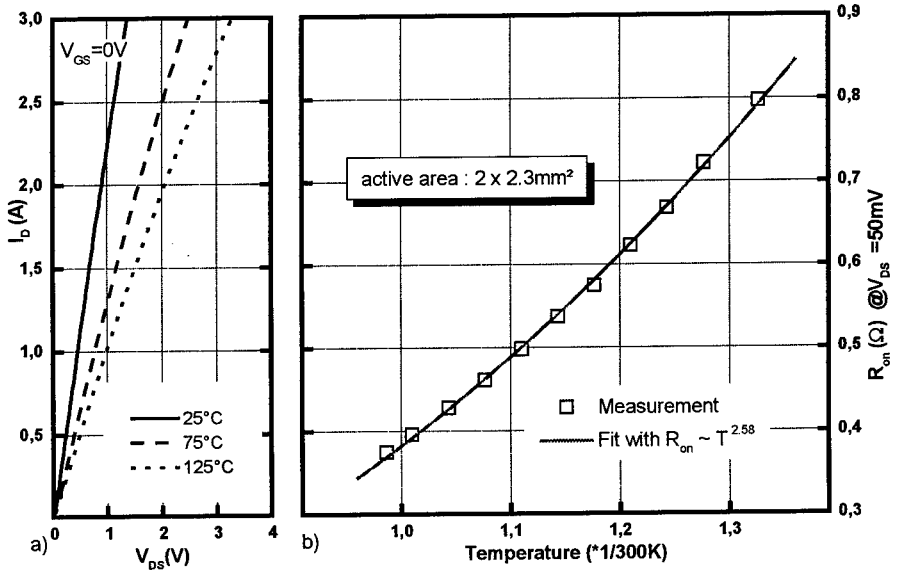

Fig.3 : Temperature dependence of a) the on-characteristic at V_{GS}=0V and b) the on-resistance at V_{DS}=50mV for two parallel connected VJFETs (blocking class 1200V)

of the on-resistance is given by the temperature dependence of the reciprocal electron mobility. The latter was modeled by means of the familiar Caughey and Thomas formula [5] (eq. 1)

$$\mu = \mu_{min} + \frac{\mu^{\delta}}{1+\left(\frac{N_D+N_A}{N^{\mu}}\right)^{\gamma}}\left(\frac{T}{300K}\right)^{\alpha} \quad (1)$$

with μ_{min} = 0 cm²/Vs, $N^{\mu} = 1.94\text{x}10^{17}\text{cm}^{-3}$, μ^{δ}= 947 cm²/Vs and γ = 0.61 [6]. A fitting of the data from Fig. 3b results in a value of α = -2.58. Such a behavior indicates that the mobility is not only influenced by phonon scattering but most probably by ionized impurity scattering as well.

Switching Characteristics and Short Circuit Behavior

The switching behavior of the device has been already thoroughly discussed previously [7] by analyzing switching tests in a cascode arrangement with a low voltage silicon MOSFET similar to the configuration described by Baliga [1]. The cascode was part of a chopper circuit with inductive load and a gate resistance of 10Ω. It could be shown that due to the connection of the buried p-layer to the source contact, the switching is considerably enhanced compared with a configuration where both p-layers act as gate [7]. However, during switch-off of the devices presented in reference [7], a tail current remained lasting approximately 300ns after an initial rapid decrease of the drain current to about 40% of its maximum within 30ns. This is supposed to be due to the triode like output characteristic of the samples analyzed in the previous work. The devices presented here exhibit a pentode like low voltage output characteristic and show even faster switch off lasting only 100ns without any significant tail behavior.

In short circuit tests, a sinusoidial signal of 50Hz with a peak voltage of 600V was applied while switching the cascode directly onto the short circuit (pulses of varying duration to the MOSFET gate). The configuration is able to works under short circuit conditions without failure up to several milliseconds. This ruggedness is caused by the self limiting behavior of the JFET what is primarily due to self heating. Such a behavior is in contrast to a corresponding MOSFET or IGBT characteristic and enables easier implementation in critical systems.

Summary

Based upon a novel vertical JFET structure, the fabrication of switching devices for different blocking voltages from 600V to 1800V with nearly identical specific on-resistances ranging from 20 to 24 mΩcm² was demonstrated. The devices operate in the ampere regime, show a very fast switching behavior and are rugged under short circuit conditions. The temperature dependence of the devices was successfully described by a temperature dependence of the electron mobility. All results fit well to previous numerical simulations.

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Power Density Comparison between Microwave Power MESFET's Processed on Conductive and Semi-Insulating Wafer

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Keywords: MESFET, Microwave, Semi-Insulating Substrate

Abstract : MESFET's have been processed either on conductive and semi-insulating wafers. After packaging of the dies, load-pull measurements have been performed at 1 and 2 GHz on various gate periphery transistors. A decrease of the power density with gate periphery has been observed. Besides, a maximum value of 2.5W/mm has been obtained with transistors processed on S.I substrate while 4W/mm has been measured on conductive wafer. A shape change of the dc I-V characteristics has been shown when high biasing which results in a decrease of the rf sweep power. We think that a high density of deep traps inside the S.I wafers are responsible for such a phenomenon.

Introduction

In the past, the first worldwide published results concerning microwave power MESFET's have been obtained with devices processed on conductive wafers. Some of them were impressive, showing that output power can reach 3.4W per mm of gate width in CW conditions [1]. Unfortunately, these performances were obtained on small transistors with gate periphery smaller than 1mm, leading to low output power values. On larger transistors, smaller performances were expected because of the large parasitic losses, mainly due to the huge capacitances generated by connection pads and lines that make a good impedance matching very difficult.

The way to avoid such a drawback consist of processing devices on high resistive or semi-insulating substrates. Such wafers have become commercially available and, in the past two years, most of the MESFET related papers dealt with transistors processed on this kind of substrates. It has been shown that the small signal rf-behavior of the transistors has been very significantly improved [2]. Power rf characterizations are also performed on-wafer or on packaged transistors, depending on their gate periphery and the heat power to be dissipated during the measurements. One of the latest published paper show that very high power density (up to 4.6W/mm of gate width) can be reached on transistors processed on semi-insulating wafer but on very short gate width (<1mm) [3]. On large transistors, a very impressive result has been announced about one year ago with an output power of 80W under CW conditions at 3GHz (ECSCRM 98, Montpellier, France). All the details of this performance are now available and show that a 48 mm gate periphery transistor has been used, meaning that the power density per unit of gate width (often called linear power density in the text) is around 1.67W/mm [3]. Such a result is another cornerstone establishing the huge capability of rf Silicon Carbide transistors. It also shows that commercial applications using this kind of devices should now come soon. But, even if such a linear power density is more than three

times higher than what is obtained from the Silicon LDMOS transistor - probably the closest competitor - we should wonder why such a strong decrease is noticed between small and large transistor performances.

In the last few months, we have been processing semi-insulating wafers and made various gate periphery MESFET's (between 2 and 6 mm per die). The dies have been packaged either in single or multi-chip packaging and load-pull characterization have been performed at 1 and 2GHz. A trend between linear power density and gate periphery has been evidenced and is reported in this paper. A comparison has been made with transistors processed on conductive wafers and the various behaviors have been qualitatively explained measuring the DC I-V characteristics of the transistors. A schematic explanation is proposed to explain the reduce power density measured on transistors processed on semi-insulating wafers.

Transistor fabrication

All the electrical characterization presented in this paper has been obtained on MESFET's processed on one of the following epi-structures :

- structure A : S.I. substrate / n-active layer / n+-cap layer (no buffer layer between S.I substrate and active layer)
- structure B : n+ substrate / p-buffer layer / n-active layer / n+-cap layer .

The details of the fabrication sequence have been given previously [4]. The channel is designed to pinch-off between -13V and -18V and the drain-source saturation current is in the 250 to 350 mA/mm range.

Some of the dies have been packaged using a special test carrier with input and output 50Ω micro-strip lines. A single chip is soldered in this case and this package will be referred as Test Carrier (TC) in the text. Another kind of package is also used and will be referred as Silicon Like Package (SLP). Single or multi-chip packaging is performed using this "standard" power package. A maximum of 6 dies has been put in the same package in order to increase the output power. The power measurements are performed between 1 and 2GHz under CW conditions.

Power results

1- Single chip on TC at 2GHz

The load-pull characterizations have been performed at various quiescent bias points in order to find the best compromise between maximum output power (Pout) and maximum power added efficiency (PAE). The total gate periphery of the various transistors that have been measured is function of finger number (8, 16 and 24) and finger width (150 and 250µm). The highest output power density (2.5W/mm) has been obtained with a 2mm gate periphery made of 8 fingers of 250µm width. The following values have been measured : Pout = 37dBm, PAE = 38% and Gain = 8.4dB at the quiescent bias point : Vdsq = 80V, Vgsq = -10V, Idsq = 140mA. All the other measurements that have been performed with higher gate peripheries transistors (2.4, 3.6 and 6mm) have given significantly lower density per unit of gate width (between 1.5 and 1.8W/mm), even at higher quiescent drain-source voltage (up to 100V).

Transistors from structure B has been characterized in very close conditions. Because of the use of conductive wafer, smaller transistor yield simpler transistor matching. That is why 1mm gate periphery transistors have been measured. The following results have been obtained : Pout = 36dBm (4W), PAE = 32% and Gain = 8dB at the quiescent bias point : Vdsq = 65V, Vgsq = -10V, Idsq = 160mA.

2- Multi-chips in SLP at 1GHz

In order to increase the output power values of the transistors, multi-chip packaging has been performed with structure A chips. Two, four and six chips have been soldered in the same package and peripheries up to 36mm have been obtained. Power density values between 1.4 and 0.95W/mm have been measured showing a clear power density decrease versus gate periphery (Fig. 1). The following results have been obtained with a 6 chips transistors (total gate periphery : 36mm) : Pout = 45.4dBm (34.4W), PAE = 28% and Gain = 8.2dB at the quiescent bias point : Vdsq = 70V, Vgsq = -10.4V, Idsq = 1.4A.

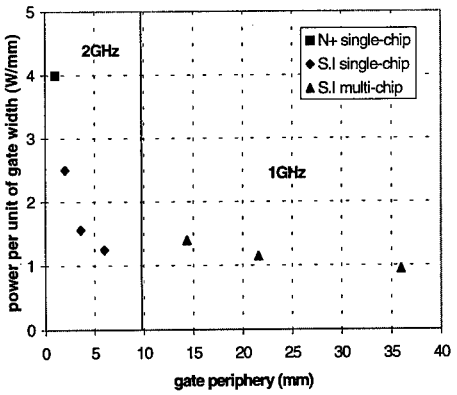

Fig.1 : power per unit of gate width on various gate periphery transistors processed on N+ and S.I wafers

Discussion : evidence of trapping phenomena

When comparing the two results obtained on single chip on TC at 2GHz, we can notice that the quiescent bias current values are very close while periphery of the transistor from structure A is twice. So, the difference in power density can originate from this difference in quiescent current. When trying to increase the quiescent bias current on structure A transistors, we have noticed a decrease in output power while gain values are unchanged. As a consequence, a large decrease in PAE is observed. Besides, when measuring the same transistor (multi-chips in SLP) several times and especially when biasing at high voltage, a decrease of the rf power has been noticed. After a long rest (several days) or after annealing at 300°C for few minutes, the initial properties are recovered.

We have previously presented evidences of trapping phenomena on devices processed on semi-insulating wafers [4, 5]. We believe that these phenomena are responsible for the lower power density than expected. We have observed a change in the shape of the DC I-V set of characteristics and specially a strong increase of the knee voltage after a high voltage biasing, whatever the gate periphery, leading to a decrease of the RF power sweep (Fig. 2). The location of the quiescent bias point stay unchanged even after several measurements. We believe that high trap density in the semi-insulating substrates are responsible for this discrepancy. SIMS analysis on semi-insulating wafers have shown a Nitrogen residual level of $2.10^{17}cm^{-3}$. Even if the way to make substrate semi-insulating is not precisely known, a high compensation ratio is necessary to achieve semi-insulating properties including a high concentration of deep levels. These levels can act as traps and, when filled by electrons, can create a backside depletion layer at the substrate-active layer interface, additional depletion responsible for the drain current decrease and on-resistance increase.

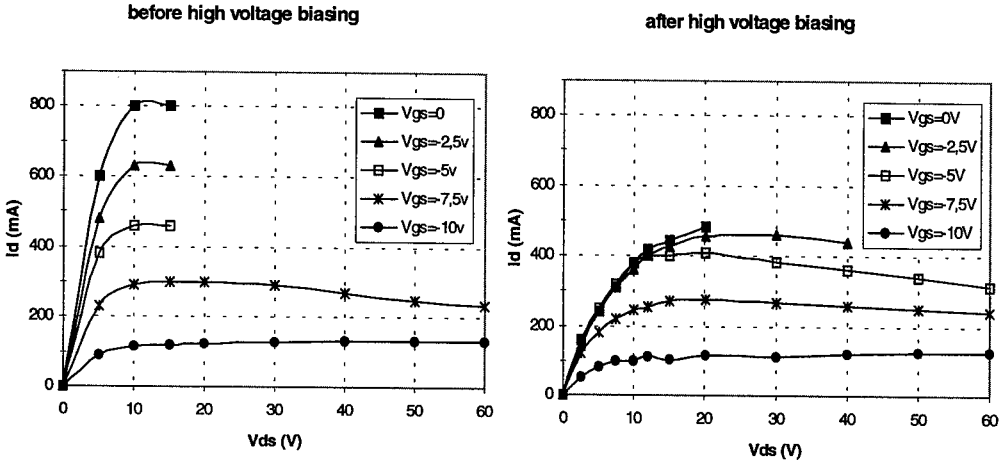

Fig. 2 : DC characteristics of a structure A transistor before and after high voltage biasing. No such change is observed on structure B transistor

Conclusion

Trapping phenomena have been evidenced on various gate periphery transistors processed on semi-insulating substrate with a buffer-less structure. These phenomena are responsible for variations of the shape of DC set of I-V characteristics when high biasing is performed. Power behavior limitations has also been evidenced. It has been impossible to get more than 2.5W/mm out of a 2mm gate periphery transistor while 4W/mm is reach on conductive wafer. A trend, showing a decrease of the linear power density versus gate periphery, has been evidenced. Because of the location of the traps, inside the S.I substrate, we point out that an efficient buffer layer between the substrate and the active layer has to be added in order to prevent the injection of carriers into the substrate. By this way, we hope to reach the promising linear power densities (around 4W/mm) which are targeted and make Silicon Carbide a really promising material for RF microwave power transistors.

Acknowledgments : this work was supported by EEC (TELSIC ESPRIT Program) and French Defense Administration (DGA)

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Surface Induced Instabilities in 4H-SiC Microwave MESFETs

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Keywords: MESFET, Microwave Power, Surface Traps

Abstract
Mesa isolated 4-H SiC microwave MESFETs showed a relaxation in drain current following application of operating bias on a timescale of seconds. It is shown that this was associated with charging of the exposed surface between the gate and the source and drain contacts, and that this impacted CW performance. Pulse operation of the devices nevertheless gave good power performance of 2.5W/mm at 2GHz.

Introduction

Highly encouraging microwave power results have been reported for SiC MESFETs [1, 2], however, as yet there has been little public discussion of the device non-idealities which normally result from the use of a new material system. Noblanc [3] has reported a gradual reduction in drain current following application of bias, which was tentatively ascribed to trapping in the vicinity of the buffer/substrate. Here we describe work on a qualitatively similar phenomenon which we show was due to charging of the exposed SiC surface between the gate and the source and drain. Similar effects are well known in GaAs MESFETs [4]. We illustrate the effect of the instability on the device current-voltage (IV) and radio frequency performance.

Device Fabrication

Conventional mesa isolated MESFETs were fabricated on both conducting and semi-insulating 4H-SiC substrates using a combination of optical and electron-beam lithography[5]. The three layer epitaxy was purchased from Cree Research and had a heavily doped ($\sim 10^{19}cm^{-3}$) contact layer, a nominal channel doping of $2.4x10^{17}cm^{-3}$ of etched thickness 0.2-0.35μm thickness and a lightly doped p buffer layer of thickness 5μm and 0.5μm for the conducting and insulating substrates respectively. For a gate length of 0.7μm, breakdown voltages >100V have been achieved with f_T~8GHz and f_{max}~20GHz when probed on-wafer continuous wave (CW). No passivation layer was included on any of the devices reported here.

Drain Current Instability

The device performance was found to be strongly dependent on the measurement technique and previous measurement history. Figure 1 shows a particularly dramatic example of the effect of different pulse conditions on the IV characteristic of a 200μm wide device. For a slow ramp measurement, a fairly conventional drain IV characteristic was observed. When the device characteristic was measured by pulsing both drain and gate bias from 0V to each measurement

point, the drain current saturation became far less pronounced. However, when the quiescent point was set to a V_{DS} of 24V and V_{GS} of –7V, the drain current collapsed and the knee voltage increased dramatically. In a similar way, the presence or absence of illumination could change the device characteristic. Indeed, all our devices on both conducting and insulating substrates have shown this effect with varying magnitude and time constant.

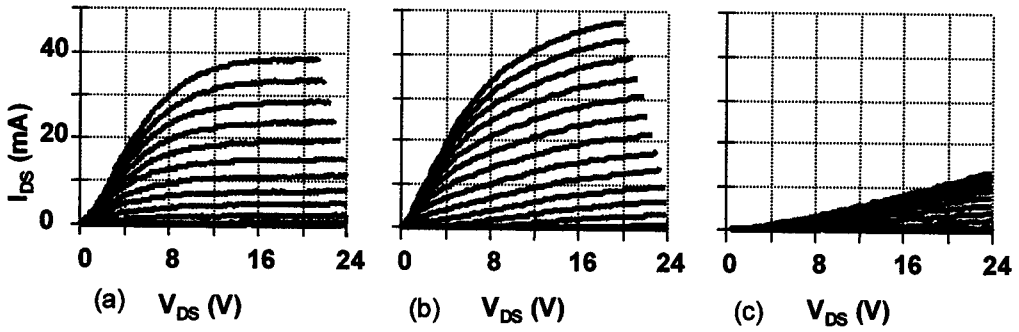

Figure 1. (a) Slow sweep, (b) pulse IV from V_{DS}=0V, V_{GS}=0V, (c) pulse IV from V_{DS}=24V, V_{GS}=-7V. 200/0.7μm MESFET with -1V per gate step starting at +1V, pulse length was 0.5μs and duty cycle 0.1%. (Av13,20E2)

It appeared that this instability was not a simple bulk trapping effect. In devices fabricated on conducting substrates, a substrate bias could be applied which allowed the channel to be pinched off from below. Following a step change in the substrate bias on large area MESFETs (150x100μm), the channel current changed rapidly and showed little relaxation in the current after the step. Hence it appeared that there were insignificant numbers of deep levels at the buffer/channel interface. Similarly the Schottky diode gate could be eliminated as a direct source of trapping since the same large area MESFETs showed insignificant drain current or gate capacitance relaxation following step changes in gate or drain bias. These measurements do not preclude field induced trapping/de-trapping in the bulk in the short-channel devices but certainly suggest that the bulk is not dominant.

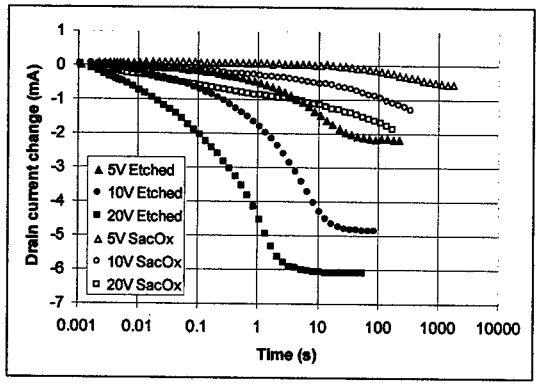

Figure 2. 100/2μm SI substrate MESFETs. Current change following indicated drain voltage step (V_{GS}=0V). I_{dss0} 350mA/mm for Etched, 430mA/mm for SacOx. (Bul14,21V, Por18,17V)

Figure 2 shows clear evidence for the surface sensitivity of the effect. The drain current relaxation following application of the indicated drain bias with gate earthed has been plotted for two devices fabricated on the same wafer, but with different surface processing. The two variants were an unpassivated device where recess etch damage was not removed (Etched), and a device where oxidation and strip was used to remove the etch damage (SacOx), but no further passivation was applied. Drain current relaxation was observed in both linear and saturation regimes, with the

relaxation occurring faster at increased drain bias. The process was not simply characterised by a single time constant with considerable dispersion being observed. The surface sensitivity was very clear with SacOx slowing the current relaxation by at least two orders of magnitude and reducing the magnitude of the effect considerably. The observation of the effect in the linear regime also tends to rule out field induced de-trapping of bulk traps.

Our measurements suggest that a surface depletion layer of typically ~0.1μm was normally present at the ungated surface in the absence of any bias, representing a surface charge of ~$2x10^{12}cm^{-2}$. This depletion layer was inferred from a combination of Hall measurements on ungated van der Pauw structures and device conductance and capacitance measurements on large area transistors. A substrate bias was used on the conducting substrate devices to find the fraction of donors which were activated, since this had to be accurately accounted for. The activation was measured by comparing the change in free carrier number density (from Hall), with the change in net donor numbers (from the large area device pinch-off voltage), as the substrate bias and hence conducting channel thickness was varied. Typically only 60-75% of the donor atoms were found to be activated at room temperature, which was confirmed from temperature dependent Hall measurements [6].

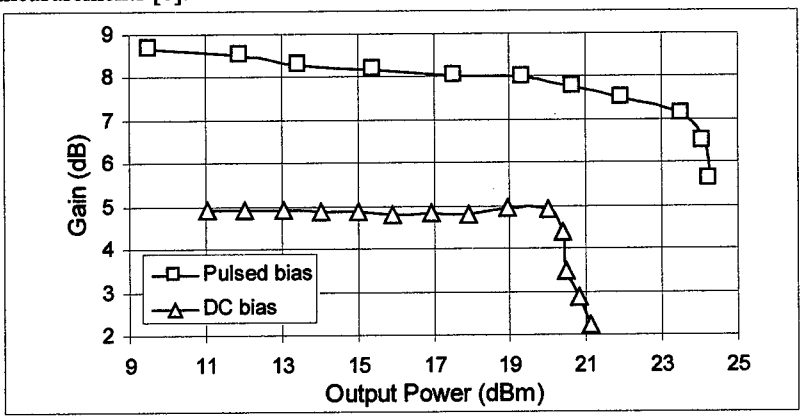

Figure 3. Static and pulsed power measurement for a 200/0.7μm MESFET. V_{DS}=60V, V_{GS}=-6V, I_D=30mA, 2GHz, 450ns DC pulse length. (Eng17,19C)

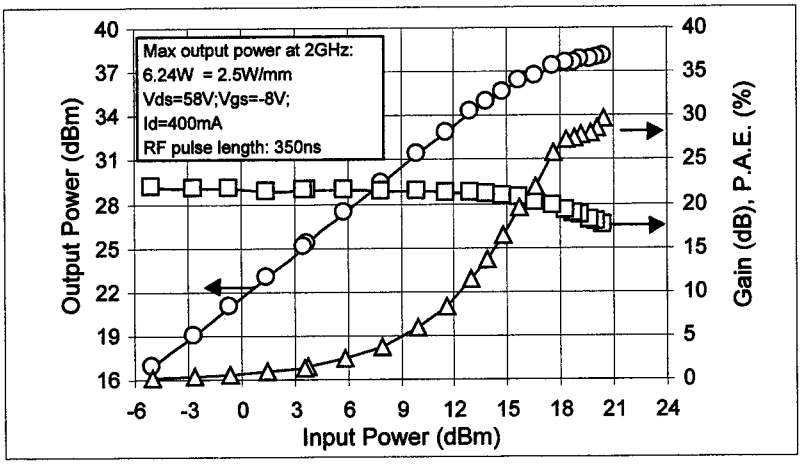

Figure 4. Pulse power from a 10 finger, 2.5mm wide MESFET, DC pulse length 450ns, duty cycle 1%. (Av14,14)

The overall effect of the current instability was that the device RF performance was degraded at CW, with the details being subtly dependent on the particular device geometry. Figure 3 shows the difference between pulsed and static measurement of the RF gain for one particular 200μm wide device. In this case, pulsed measurement gave an extra 3dB of gain and power. However, good power results were achieved for pulsed operation, with >6W demonstrated with 3dB gain compression (see figure 4).

Discussion and Conclusions

The presence of a surface depletion region in the ungated region showed that there are surface traps which can store charge and which in principle can change state and so modulate the channel current. The most likely model which accounts for the observations is that charge can transport across the ungated surface between the gate and the source and drain under the influence of the lateral electric field. This additional surface charge will change the surface depletion width and so modulate the channel width. Charge flowing into the gate-source region will increase the source resistance giving an increase in the knee voltage, a reduction in the channel current and thus a reduction in RF gain. Gate charge spilling onto the drain side of the gate will result in the saturated drift region extending further towards the drain. Figure 1c shows this in operation, where the applied gate and drain biases resulted in a strong reduction in channel current and an increase in knee voltage.

It is clear that effective passivation of the surface is essential to reduce the density of surface states and hence control the channel modulation allowing CW operation. However, even in the absence of passivation, useful pulse power operation can be achieved.

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Characterization of SiC MESFETs on Conducting Substrates

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Keywords: Capacitive Loss, f_{max}, f_t, MESFET

Abstract. Silicon Carbide MESFETs were fabricated on n-doped substrates (N_d $4x10^{18}cm^{-3}$), utilizing 15 μm low doped epi layers (N_d mid $10^{15}cm^{-3}$ range) for reduction of capacitive losses. An f_{max} of 31 GHz and an extrinsic f_t of 7.8 GHz for a gate length of 0.4 μm were achieved. The pad capacitances for the gate and drain contacts of the devices were 2-3 times the values of devices made on semi-insulating substrates.

Introduction

Silicon Carbide MESFETs for microwave operation are usually made on semi-insulating substrates in order to reduce capacitive losses [1]. This makes operation at higher frequency possible compared to MESFETs made on standard, conducting substrates [2]. Semi-insulating SiC substrates are less developed than normal n- and p-type doped substrates and are also very expensive. A method to use standard, conducting substrates for SiC MESFETs would therefore be desirable. In this work, we have fabricated MESFETs on standard n-type substrates. Thick low doped epi-layers were used to reduce the capacitive losses.

Fabrication

Low doped p^- epi layers were grown on n^+ substrates (doping $4x10^{18}cm^{-3}$) to a thickness of 15 μm. The layers were unintentionally doped to the mid $10^{15}cm^{-3}$ range. The active layer was formed by nitrogen implantation (N_d $1.5x10^{17}cm^{-3}$), and a top n^+ layer for ohmic contact formation, doped to $10^{19}cm^{-3}$, was grown by CVD.

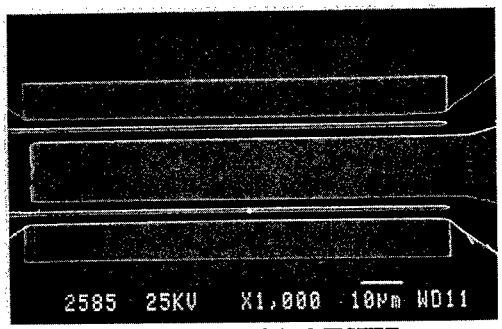

Fig. 1. SEM micrograph of the MESFET gate area.

MESFETs with two parallel gates (Fig. 1.) were fabricated on this structure. The fabrication process includes recess etching, ohmic contact formation, definition of gates using electron beam lithography, device isolation and definition of the pads. No air bridge technology was used. The gate length was varied from 0.4 μm to 2.6 μm. The drift region length was 1.5 μm - 2.5 μm. The gate width was 200 μm.

Characterization

DC characterization of the MESFET devices showed a low threshold voltage between –1 and –3 Volts and an on-state current of 40-60 mA/mm, as seen in Fig 2. A low threshold voltage could be related to a lower than expected electrically active nitrogen concentration in the channel layer. The transconductance g_m (20 mS/mm) and the on-state current do not show a pronounced dependence on the gate length, in contrast with theoretical predictions for an ideal MESFET. This indicates a considerable source resistance. The breakdown voltage measured in the off state was >100V (Fig. 4.).

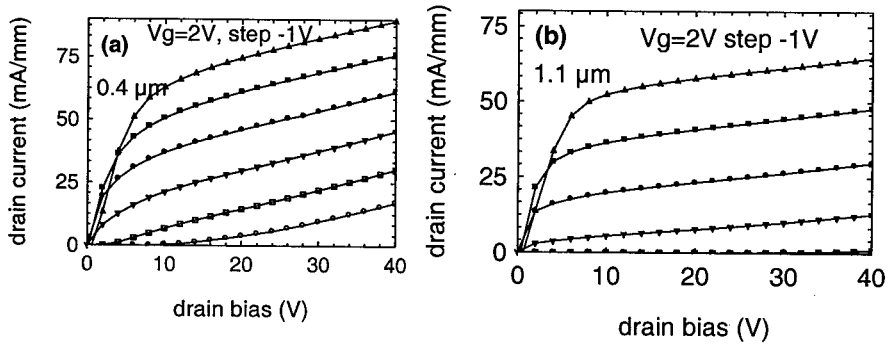

Fig. 2. DC characteristics of MESFETs. Channel width is 0.2 mm, the gate length is 0.4 µm (a) and 1.1 µm (b).

The maximum frequency of oscillation, f_{max}, and the transit frequency, f_t, were measured for transistors with different gate lengths (Fig. 3.). The best value is f_{max} = 31 GHz and an extrinsic f_t = 7.8 GHz for a gate length of 0.4 µm. The increase in f_{max} and f_t is small for a gate length below 0.8 µm, indicating other limiting factors, possibly the capacitive loss to the conducting substrate and output conductance.

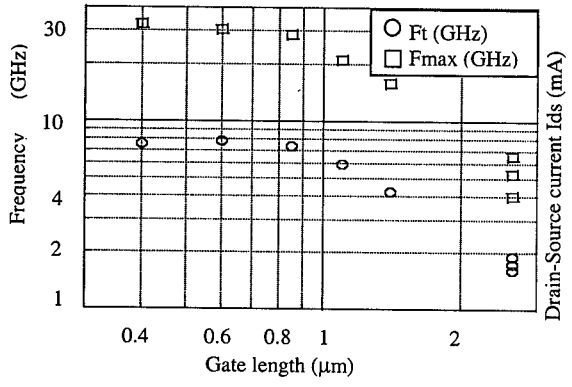

Fig.3. MESFET frequency response vs. gate length.

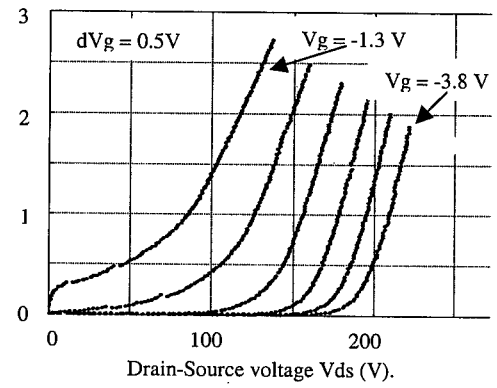

Fig. 4. Breakdown voltage measurements for a MESFET with 2.6 µm gate length.

Load-pull measurements were performed on a device with 0.6 µm gate length and 200 µm total channel width (Fig.5.). The measurement frequency was 2 GHz and a source-drain voltage of 50 V

was used. The maximum power density was slightly below 100 mW/mm. This low power density could be due to resistive parasitics as seen in the low on state current. A measurement at 40 V source-drain bias gave 2 dBm lower maximum power density.

One transistor with a gate length of 0.5 μm was compared to a similar device fabricated on a MESFET structure grown on a semi-insulating substrate (by Cree Inc). The device on semi-insulating material had an f_{max} = 39 GHz and f_t = 8.1 GHz, compared to the values for the device on normal material of f_{max} = 31 GHz and f_t = 7.5 GHz. Modeling [3] of the devices gave pad capacitances for the gate and drain contacts of the device on normal material of 2-3 times the values for the device on semi-insulating substrate. This can explain the difference in frequency response between the devices. For more data on this comparison, see [3].

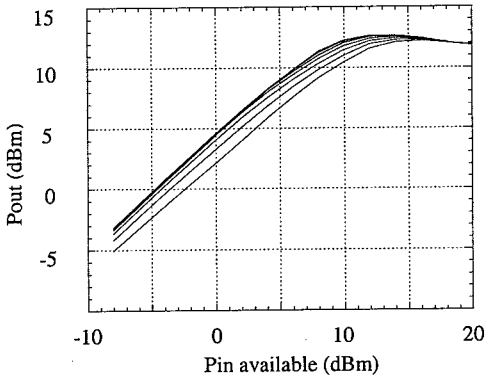

Fig. 5. Output power vs. input power at 2 GHz for a device with 200 μm channel width and 0.6 μm gate length. The gate DC bias was varied from -2 V (lower curve) to +1 V (upper curve).

Simulations

The MESFET operation was simulated using the 2-dimensional MEDICI software[4]. The actual doping profile is uncertain. Calibration experiments have shown the corresponding dose ratio to be around 55%, which was used in simulation. The source resistance was varied to obtain the best fit to experimental data. Plotted in Figure 6a and 6b are the results for the simulation assuming a zero source resistance. As seen from the plot, the simulation assuming a zero source resistance shows a much stronger dependence of the on-state current on the gate length than what is experimentally observed. The possibility of applying a large positive bias to the gate also cannot be explained for this model. A better agreement with experiment is obtained assuming a source resistance of 20 Ohms/mm, as is seen from Figures 6c and 6d. The reason could be related to incomplete annealing of implantation damage in the channel region. Another possibility is trench formation at the edge of the masking layer, which could occur upon reactive ion etching of the n^+ and the channel regions. Such a trenching could decrease the active channel thickness in the regions adjacent to the source.

Experimental and simulated curve families clearly illustrate the significance of short-channel effects in silicon carbide MESFETs (Fig 2, 6). The devices with longer channels have near-classical MESFET characteristics with clearly defined saturation and turn-off regions. By contrast, the drain current of short-gate MESFETs does not have a good saturation of the drain current, it considerably increased with the increase of the drain voltage. Off-state short-channel devices can be turned on applying an additional gate bias.

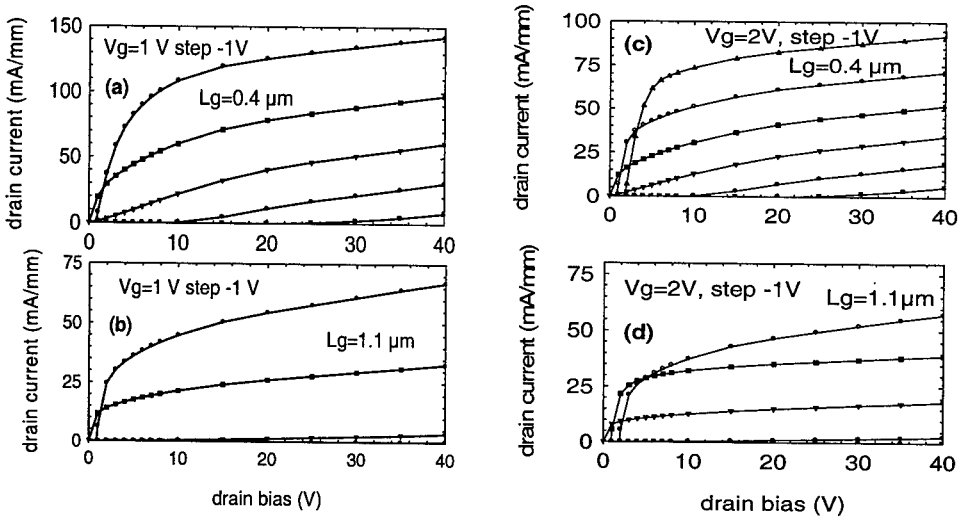

Fig. 6. Simulated curve families of implanted-channel microwave MESFETs. Gate length is 0.4 μm (a,c) and 1.1 μm (b,d). The source resistance in the simulation is 0 Ohms/mm (a,b) and 20 Ohms/mm (c,d).

Discussion

We have looked at the possibility to use standard SiC substrates for MESFETs by using thick, low doped epi layers in order to reduce capacitive losses. The results are encouraging, with frequency response not far from what was achieved on devices of similar design made on semi-insulating substrates. The power density was low, but we believe this is caused by resistive losses due to inadequate doping or activation of the active layer. The simulation results support this theory. This problem could thus be solved in a future batch. We believe the frequency response for these devices could be good enough for microwave devices in the lower frequency range, e.g. for cellular phone base stations.

Acknowledgement

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Fabrication, Characterization, and Modeling of SiC MESFETs

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Keywords: DC, Equivalent Circuit, Load-Pull, MESFET, Modeling, Noise, Silicon Carbide, S-Parameter

Abstract

In this paper we present the work on of submicron gate length SiC MESFET´s performed at Chalmers University. A process for fabrication of air-bridged multi-finger high power Silicon Carbide MESFETs has been developed. Measurement results as well as small signal. and noise modeling for two different batches are presented. Drift Diffusion simulations have been used to understand the physical processes in the MESFET.

1. Introduction

The combination of several advantageous material properties such as high thermal conductivity, high breakdown field and high saturation velocity makes Silicon Carbide (SiC) a very promising material for high power microwave MESFET amplifiers. SiC MESFET could have a wide range of applications in mobile radio base stations, microwave ovens, microwave lighting, phased array radars and various electronic warfare systems.

2. Transistor Processing

All processes necessary to produce large SiC MESFETs with air-bridges have developed. The transistor fabrication process consists of five optical lithography steps and one electron beam lithography step. The sequence is mesa, recess, thermal oxidization, dielectric deposition and etching, ohmic contact formation, gate (EBL), pad deposition, and air-bridge formation. The mesa and recess steps use Reactive Ion Etching with a CF_4/O_2 gas mixture. Ohmic contacts are formed by annealing nickel at 950°C with a Rapid Thermal Anneal (RTA) furnace and the resulting ohmic contact resistance is 0.5-0.6 Ω·mm. The gate contact consists of a multi-layered metal structure (Ti/Pt/Au). The Schottky barrier height of the gate is 0.9 eV.

The MESFETs are processed on a three-layer homoepitaxial structure on semi-insulating 4H-Silicon Carbide from Cree Research. The layer structure is from the top: 0.15 µm n-type cap layer $N_D=1\cdot10^{19}$ cm^{-3}, 0.5 µm n-type channel layer $N_D=3\cdot10^{17}$ cm^{-3}, and 0.5 µm p-type bufferlayer $N_A=5\cdot10^{15}$ cm^{-3}. The channel thickness under the gate of the component is 0.35 µm. The gate length is 0.5 µm and gate to source spacing is 0.5 µm and gate to drain spacing is 1.0 µm.

The multi-finger devices have more than two gatefingers and thus require air-bridges. The new designs are processed with and without sidegating (grounding the buffer layer), with different number of gatefingers, and different gate to gate spacings to investigate the effect of these parameters. Air bridges are formed from pure gold. The gate length (L_G) is 0.5 um and gate to source spacing (L_{GD}) is 0.5 um and gate to drain spacing (L_{GS}) is 1.0 um. Figure 1 shows a SEM photograph of a multi-finger SiC MESFET.

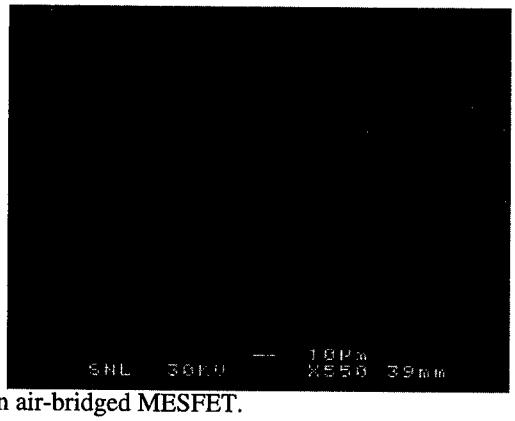


Fig. 1: A SEM picture of an air-bridged MESFET.

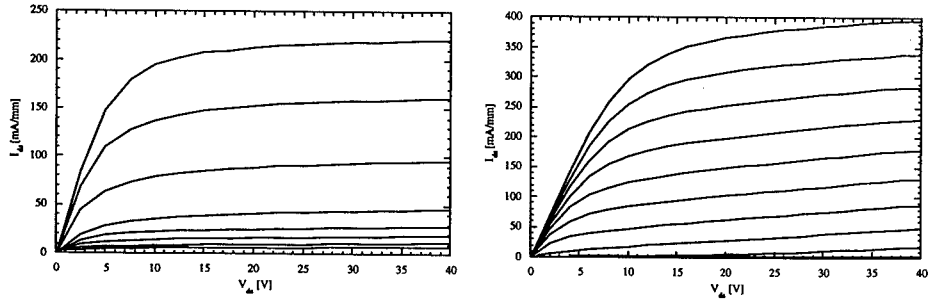
3. Simulations by Physical Modeling

Numerical drift-diffusion simulations have been performed to optimize the proposed device structure using Medici from Avant Corporation [1]. We used the most recently published model parameters for 4H-SiC to obtain the close agreement with the experimental data. The simulator uses an anisotropic, field dependent and doping dependent mobility. It also considers incomplete ionization of the donors and an advanced band structure. The effects of an increased lattice temperature were also included.
The breakdown voltage and the power density of the device were calculated for different doping concentrations and thicknesses of the channel layer. The thickness and the doping of the p-type buffer layer was selected with respect to the doping of the channel layer. The Schottky gate was recessed to a finite depth to achieve an optimum breakdown voltage. The breakdown occurs as an avalanche at the gate junction. Further increase in the channel doping decreases the breakdown voltage due to an increase in the field at the gate for the same applied drain bias.

4. Characterization and Results

In this section we present the characterization and the results of two different batches (hereafter named Run#1 and Run#2) of MESFETs fabricated on the same material.

4.1. DC-measurements



(a) (b)

Fig. 2: Drain characteristics, I_{DS} vs. V_{DS} for SiC MESFET Run#1 (a) and Run#2 (b). Traces are, from the top, measured for V_{GS}= 0, -2,..., -14V (a) and V_{GS}=0, -2,..., -20V (b).

The DC-characteristics were measured using a HP4145 semiconductor parameter analyzer (fig. 2). The DC transconductance, g_m, and the saturation drain current, I_{dss}, for Run#1 (Run#2) is 30 (23) mS/mm and 220 (390) mA/mm, respectively. The on-state drain-gate breakdown, V_{bdg}, is ≈105 V for Run#1 (Not measured yet for Run#2). The higher current and lower transconductance for Run#2 indicate a

more shallow recess etching. Notice that we have much better pinch-off characteristics in Run#2 (the last two curves for V_{gs}=-18 and –20 V are not visible in figure 2).

4.2. High Frequency and Noise Measurements and Modeling

Noise- and s-parameters were simultaneously measured using a noise test set connected to a VNA (HP8510). The drain currents were 20, 40 and 60 % of I_{dss} and the drain voltages were 10, 20, 30 and 40 V. Noise and s-parameters were measured between 2-26 GHz. S-parameters were also measured at other biases and higher frequencies, which are used in the extraction of the equivalent circuit. The maximum frequency of oscillation, f_{max}, for the SiC MESFET was 39 (37) GHz, the extrinsic transit frequency, f_T, was 8.1 (8.0) GHz, and the intrinsic f_T was 11 (12) GHz for Run#1 (Run#2).

A standard FET equivalent circuit was used to model the small signal characteristics of the SiC MESFETs (fig. 6). It was not possible to use coldFET and forward biased gate coldFET to extract the parasitics. R_g, R_s and R_d were extracted from DC-measurements using HP4145 Semiconductor Parameter Analyzer. R_g was set to one third of the end-to-end resistance of the gate fingers. R_s and R_d were measured using a gate-probe method. The parasitic capacitors and inductors associated with the probe pads were determined using optimization with HP MDS. Once the parasitics were determined the closed form expressions in [2] could be used to extract the intrinsic equivalent circuit parameters. The validity of parasitic parameters were checked by ensuring frequency independent intrinsic parameters. The resulting equivalent circuit parameters for Run#1 are listed in table I.

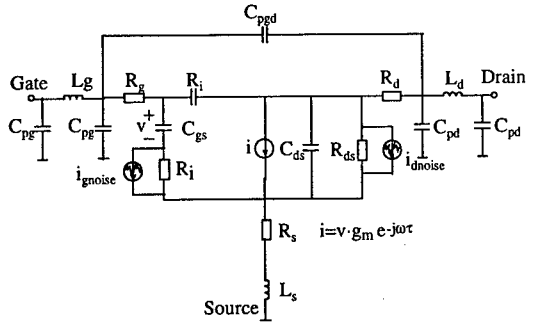


Fig. 3: Small signal equivalent circuit

Table 1. Equivalent circuit parameters

Parameter	Value	Unit
Cpg	11	fF
Lg	32	pH
Rg	2.4	Ohm
Cpd	6.5	fF
Ld	33	pH
Rd	55	Ohm
Ls	1.0	pH
Rs	20	Ohm
Cpgd	5.0	fF
Cgs	59	fF
Ri	53	Ohm
Cgd	3.7	fF
Cds	5.4	fF
Rds	2800	Ohm
gm	4.2	mS
t	4.3	ps

The Pospieszalski-method [3] was used to model the noise parameters for Run#1. The noise source parameters were extracted both by optimization and direct extraction[4]. The two methods gave the same result and very good correspondences were achieved (fig. 4). The minimum noise figure was measured to be 2.7 dB [5] with an associated gain (G_{ass}) of 12dB at 3 GHz.

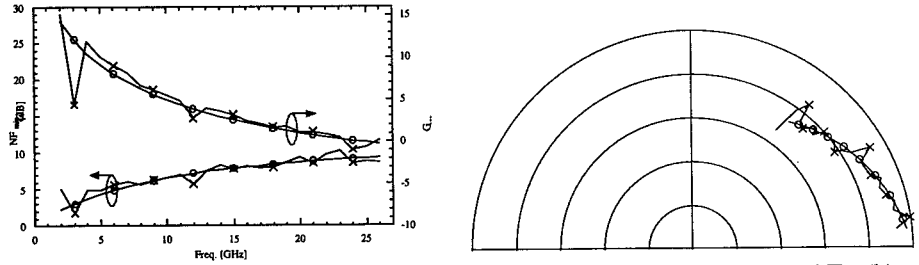
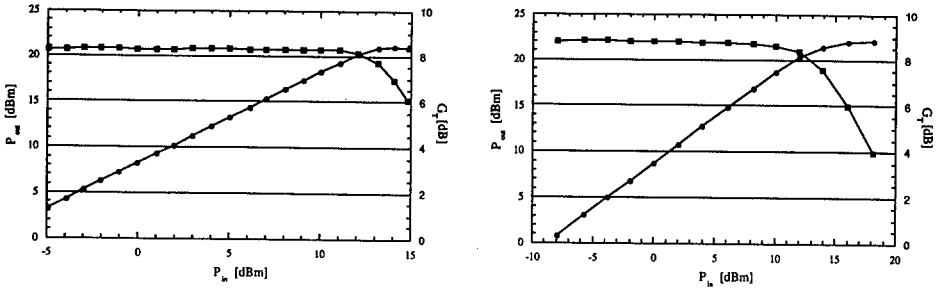


Fig. 4: Measure and modeled noise parameters for Run#1: NF_{min} and R_n (a), and Γ_{opt} (b)

4.4. Load-Pull Measurements

The output power of the MESFETs were measured with a Maury Load Pull system. The output power was 0.4 (1.6) W/mm for Run#1 (Run#2) in Class A. Better pinch-off characteristics and •-contacts partly explain the higher output power for Run#2.



(a) (b)

Fig. 5: Output power and gain vs. input power. for Run#1 (a) and Run#2. The gate width is 400 μm and 100 μm in (a) and (b), respectively.

5. Discussion and Conclusions

We have in Run#2 improved the output power by improving pinch-off characteristics. To further improve the power performance of our devices we will investigate other material structures. Physical simulations indicate that by changing the buffer thickness and doping higher output power is achievable. We will also work on reducing the parasitic resistances by decreasing source-drain distance and using double recess. This will also improve noise performance. The frequency performance will be improved by increasing the transconductance. This may be achieved by increasing the aspect ratio, which will also improve output conductance. Air-bridgedSiC MESFETs are currently being manufactured. These devices have a total gate width up to 12.8 mm.

Acknowledgments

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Physical Simulations on the Operation of 4H-SiC Microwave Power Transistors

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Keywords: MESFET, Microwave Power Transistor, Simulation

Abstract Physical drift and diffusion simulations were performed in order to optimise the device structure of and to understand the relevant physical processes in 4H-SiC microwave power MESFETs. The doping and thickness of the channel and buffer layers were optimised. The maximum drain current was above 300 mA/mm. The optimum power performance was modelled using both DC and RF analysis. The cut-off and the maximum frequency of oscillation for a device with a gate length 0.5 μm were 13 and 45 GHz respectively. The maximum achievable gain was above 10 dB up to 26 GHz. The Self-heating due to current flow in the device was modelled and the channel temperature was as high as 636 K at a drain bias of 130 V.

Introduction

The combination of several advantageous material properties such as high thermal conductivity, high electric breakdown field and high saturation velocity makes silicon-carbide (SiC) a promising material for high power microwave transistors. Theoretical calculations indicate that SiC metal-semiconductor field effect transistors (MESFETs) could have output power densities a factor of 5-10 higher than those of standard technologies [1]. SiC MESFET amplifiers with output powers in the range 10-1000W between 1 and 20 GHz could have a wide range of applications in mobile radio base stations, microwave ovens, phased array radars and various electronic warfare systems. In this paper we present simulation results for 4H-SiC MESFETs and an analysis of DC and RF performance and the self-heating due to current flow.

Transistor simulations

In this paper we present results from numerical drift-diffusion simulations using a commercial program, Medici, from Avant Corporation [2]. We have utilised the most recently published model parameters for 4H-SiC to obtain the closest agreement with experimental data. The simulations use an anisotropic, field dependent and doping dependent mobility. For low field mobility the Arora model is used [3]. The high field mobility was modelled with a Caughey-Thomas expression [4]. The simulation also considers incomplete ionisation of the donors, the temperature dependence of the bandgap and the effective density of states, variations in the intrinsic concentration due to heavy doping, a concentration dependent lifetime, Shockley-Read-Hall and Auger recombination, impact ionisation and tunnelling, the anisotropic permittivity and lattice heating. The semi-insulating substrate was modelled as a compensation-doped semiconductor with a high density of deep level impurities.

Structure optimisation

Figure 1 shows the basic device structure which consists of a semi-insulating substrate, a p-type buffer layer, an n-type channel and an n^+ contact layer. The gatelength was 0.5 μm, the gate to source spacing was 0.5 μm and the gate to drain spacing was 1.0 μm. The breakdown voltage and the DC power density of the device were calculated for different doping concentrations and thicknesses of the channel layer. The Schottky gate was recessed to a finite depth to achieve an optimum breakdown voltage.

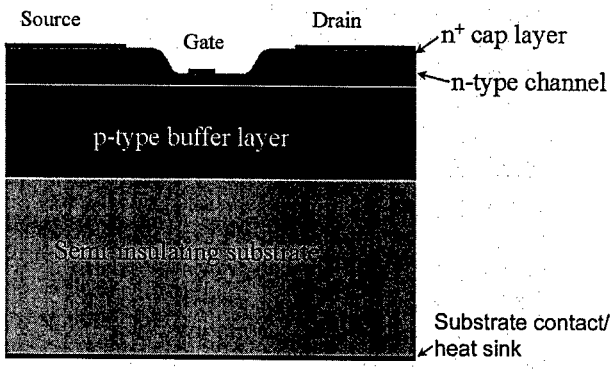

Fig. 1. MESFET structure used in the simulations

Buffer layer. While keeping the channel layer at a constant doping and thickness, the p-type buffer layer thickness and doping were varied in order to maximise the drain current while still being able to pinch off the device for a certain gate bias. Our simulations show that the properties of the semi-insulating substrate strongly affects the transistor performance when the buffer layer is too thin and low doped. On the other hand, the use of a thick, highly doped buffer layer reduces the drain current significantly. Figure 2 is showing plots of simulated drain current as a function of drain to source bias for certain gate voltages. The channel thickness and doping was kept at 0.25 μm and 1.9×10^{17} cm^{-3} respectively. The results for a buffer thickness of 2 μm and a doping of 1×10^{17} cm^{-3} is shown in Fig. 2 (a). The device was pinched off but the drain current was reduced to 140 mA/mm at $V_g = 0$ V and $V_{ds} = 90$ V. The performance of an optimised structure with buffer thickness and doping of 2 μm and 5×10^{16} cm^{-3} respectively is displayed in Fig. 2 (b). The drain current at $V_g = 0$ V and $V_{ds} = 90$ V was >200 mA/mm and the channel was pinched off at $V_g = -8$ V.

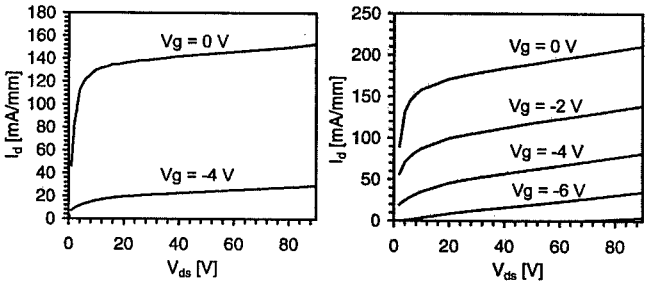

Fig. 2. Drain characteristics for a 0.25 μm thick channel with 1.9×10^{17} cm^{-3} doping and (a) 2 μm thick buffer with 1×10^{17} cm^{-3} doping, $V_g = 0, -4$ V (b) 2 μm thick buffer with 5×10^{16} cm^{-3} doping, $V_g = 0, -2, -4, -6, -8$ V.

Channel layer. The doping of the channel layer directly affects the drain current and breakdown voltage and thus the power density of the transistor. When varying the channel doping one must be aware that it affects other important device characteristics such as the channel mobility. It also affects the buffer thickness and doping which are required to be able to control the current flow. Figure 3 shows the variations in drain currents with channel doping when the buffer was kept at a thickness of 2 μm and a doping of 1×10^{17} cm^{-3}. The drain characteristics shown in Fig. 3a, b and c corresponds to three device structures where the channel thickness was kept at 0.25 μm and the doping was set to 2×10^{17}, 3×10^{17} and 4×10^{17} cm^{-3} respectively. The drain current at $V_g = 0$ V and $V_{ds} = 90$ V was 150 mA/mm for the transistor with the 2×10^{17} cm^{-3} doping and the device was pinched off at $V_g = -8$ V (Fig.3a). When the channel doping was increased to 3×10^{17} cm^{-3} the maximum drain current was above 300 mA/mm at $V_g = 0$ V and the device was pinched off at

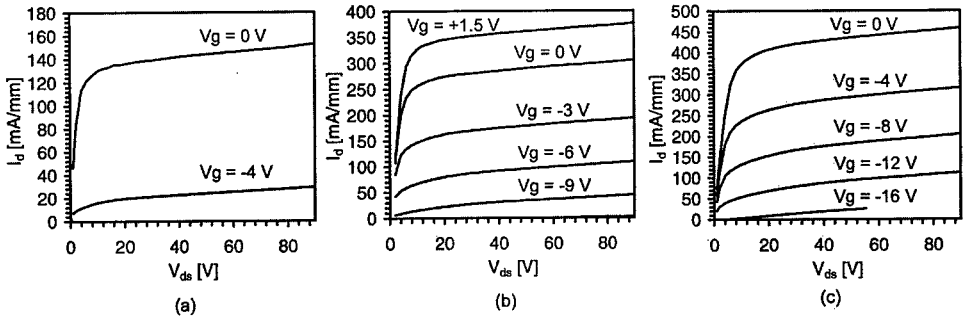

Fig. 3. Drain characteristics for a FET with a 2 μm thick buffer with 2×10^{17} cm^{-3} doping and a 0.25 μm thick channel with (a) 2×10^{17} cm^{-3} doping, V_g= 0, -4, -8V (b) 3×10^{17} cm^{-3} doping, V_g= 1.5, 0, -3, -6, -9, -12V (c) 4×10^{17} cm^{-3} doping, V_g= 0, -4, -8, -12, -16V.

V_g = -12 V (Fig. 3 b). By further increasing the channel doping to 4×10^{17} cm^{-3}, the maximum drain current was increased to 450 mA/mm at the same drain and gate biases, but the device suffered breakdown at a drain voltage of 55 V when V_g = -16 V before it was completely pinched off (Fig. 3c).

Based on the above simulations, we selected a device structure for further simulations that had a channel thickness and doping of 0.25 μm and 2.2×10^{17} cm^{-3} respectively and a buffer with a thickness and doping of 1.5 μm and 5×10^{16} cm^{-3} respectively. In the simulations the channel was pinched off at a gate voltage of -9 V. The saturation drain current was above 300 mA/mm and the breakdown occurred above 130 V as an avalanche at the Schottky gate. Further increase in the channel doping decreases the breakdown voltage due to an increase in the electric field at the gate for a constant applied drain bias.

Small signal RF analysis

The small signal high-frequency operation of the device was modelled from 100 MHz to 50 GHz. The cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}) were obtained from the calculated s-parameters and were also calculated from capacitance data. The f_T values obtained by the two different methods used were almost identical (12.5 and 12.6 GHz respectively). The results obtained for the short circuit current gain (h_{21}), the maximum stable gain (MSG) and the maximum available gain (MAG) as a function of operating frequency at a drain bias of 90 V are plotted in Fig. 4. Note that the achievable gain is above 10 dB up to 26 GHz.

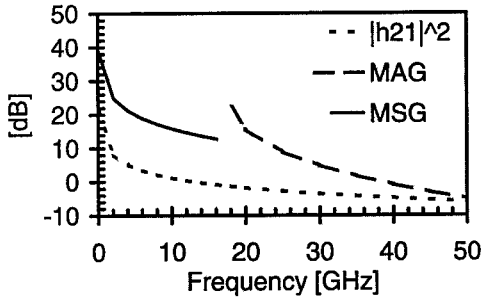

Fig. 4. Frequency response of the short-circuit current gain, the maximum stable gain and the maximum available gain for the transistor.

Lattice heating

SiC is especially attractive for power devices due to its high thermal conductivity. We have simulated the self-heating in the lattice generated by the current in the channel region and the heat flow down to the substrate which was considered a heat sink. In the calculations we used a thickness

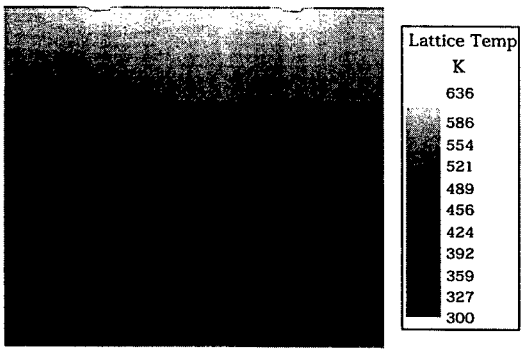

Fig. 5. Simulated lattice heat image of the device with two gates and 50 μm-thick semi-insulating substrate at a drain voltage of 130 V

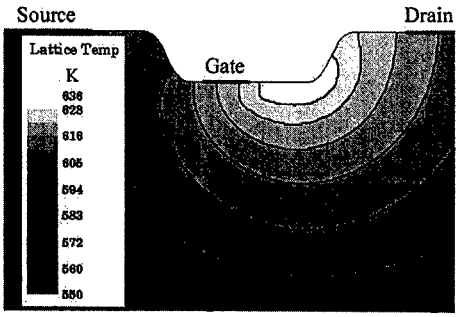

Fig. 5b Close-up of the hot region in the transistor. Contours showing temperature from 550 K and above.

of 50 μm for the semi-insulating substrate. The bottom electrode was defined as a perfect heat sink and held at 300 K. The thermal conductivity value was set to 4.9 W/cmK in the transistor layers while we used a value of 3.3 W/cmK for the semi-insulating substrate [5]. To simulate a unit cell of a power transistor we used a structure with two gates, two sources and a common drain as shown in Fig. 5a. We used a gate to gate spacing of 15 μm, which we believe is a likely value in a real multi-finger device. No temperature dependence of the thermal conductivity has been included in this simulation. The highest temperature observed was 636 K when V_g = +2 V and V_{ds} = 130 V. This occurred at the corner of the recess between the gate and the drain as can be seen in Fig. 5b. Using the selected geometry and including the thermal effects the drain current was simulated and the results are shown in Fig. 6. A significant decrease in drain current due to heating was observed only when the gate bias was +2 V. This dramatic decrease of the drain current with drain voltage was not observed for lower gate biases.

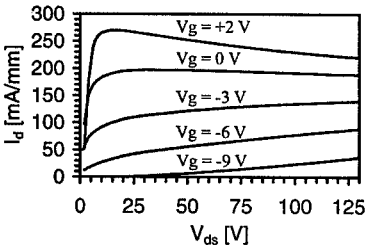

Fig. 6 Drain current simulation including heating effects for the device shown in Fig. 5.

Conclusion

Simulations showed that the selection of buffer layer doping and thickness affects the transistors drain characteristics significantly. The semi-insulating substrate properties strongly affect the transistor performance if the buffer layer is too thin and low doped. On the other hand, the use of a thick, highly doped buffer layer reduces the drain current significantly. Using a channel doping higher than 4 x 10^{17} cm^{-3} reduces the breakdown voltage of the transistor. When operating at a drain voltage of 130 V and gate bias of +2V, the temperature in the channel region can reach 636 K for a device with a 50 μm thick semi-insulating substrate connected to a perfect heat sink.

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Properties of Transmission Lines on Various SiC Substrates

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Keywords: Coplanar Waveguides, Microwave Characterization, Modelisation, Multilayer SiC Substrate

Abstract

This paper presents characteristics of microwave transmission in coplanar waveguides (CPW's) on various Silicon carbide substrates. Propagation constant and characteristic impedance measurements were performed at frequencies ranging from 0.1 to 10 GHz. A quasi-TEM equivalent circuit model was developed from the available process parameters, which takes into account the effects of electromagnetic fields in CPW structures.

1. Introduction

Silicon Carbide (SiC) devices are reported to be very promising for microwave power applications. Besides, the possibility of using semi-insulating substrates now enables a substantial performance improvement in the microwave domain for passive and active devices [1]. Furthermore, coplanar waveguides have a strong interest in the monolithic integration of microwave circuits. The modeling of SiC interconnects will be rapidly necessary for efficient circuit simulation. This paper presents an equivalent circuit model and analytical formulae to analyze the properties of coplanar transmission lines realized at LETI-CEA on various substrates.

2. Samples and experiment

Coplanar waveguides (CPW) with a longitudinal length L = 5,5 mm were fabricated on three multilayer substrates, each one being composed of bulk SiC, epitaxial (SiC P) and high thermal oxide (HTO) layers. A cross section of the test structure is given in fig.1 and the characteristics of the three samples are listed in table 1. The metal line is composed of 0.06 µm, 0.04 µm and 0.8 µm thick Ti, TiN and Cu layers respectively. It should be noted that the metal lines are obtained by chemical etching and thus exhibit a trapezoidal form. W and S values are taken as indicated in fig.1.

Structure	Substrate doping level	P-type buffer layer thickness (µm)	P-type buffer layer doping level (cm^{-3})
A	4H-SiC, $\rho>10^5\Omega.cm$	1	3.5×10^{15}
B	N-type 4H-SiC $N_D=1.2\times10^{18}$ cm^{-3}	4	6×10^{15}
C	P-type 6H-SiC $N_A=1.5\times10^{18}$ cm^{-3}	4	9.5×10^{15}

Table 1.Technological features corresponding to the three different multilayer substrates

S parameter measurements were performed over the frequency range f=100MHz-10GHz using a cascade Microtech probe station and HP 8510B network analyser, after a SOLT calibration procedure. Then the complex propagation constant γ and characteristic impedance Z_c of the line are derived using the standard form of the solution of the Telegrapher's equations [2] :

$$\gamma = \alpha + j\beta = \frac{1}{L}\ln(A \pm \sqrt{A^2 - 1}) \quad (1)$$

with $$A = \frac{(1 - S_{11})(1 + S_{22}) - S_{21}S_{12}}{2S_{12}} \quad (2)$$

and $$Z_c = 50\sqrt{\frac{(1 + S_{11})(1 + S_{22}) - S_{21}S_{12}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}} \quad (3)$$

where α and β are the attenuation and phase constants of the line respectively.

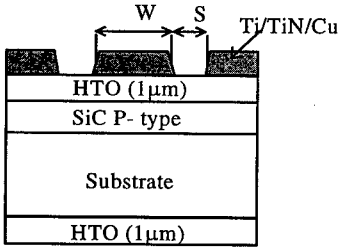

Fig.1 : Coplanar waveguide schematic cross section. W=25 µm, S=13.3 µm. The substrate thickness is about 300 µm, HTO meaning High Thermal Oxide

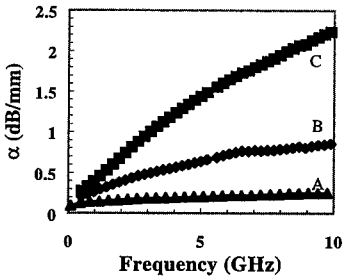

Fig.2 : Attenuation constant α (dB/mm), extracted from S-parameter measurement, for the structures A, B, C described in table 1.

3. Results

3.1 Comparison between the three different structures.

From the extracted γ values, we derived the attenuation constant α in dB/mm. α is plotted for structures A, B and C in fig.2. As can be seen in this figure, for structure C (6H-SiC substrate), α is very high at 10 GHz, approaching 2,5 dB/mm. This is mainly due to the currents flowing in the conductive SiC substrate. The loss in structure B (4H-SiC conducting substrate) is reasonable since it reaches 0,8 dB/mm at 10 GHz, but performance is greatly enhanced in structure A, because the losses in the semi-insulating substrate are drastically reduced.

Besides, it is interesting to compare the SiC semi-insulating substrate with GaAs materials. We have simulated a transmission line on a semi-insulating GaAs substrate with the same line geometry. A typical resistivity value used for this material is 10^7 Ω.cm, and its permittivity is around 12,5. If we compare this with a SiC substrate (same resistivity), we find that SiC has a better performance than its GaAs counterpart, due to its lower permittivity value ($\varepsilon r_{(4H\text{-}SiC)}$**=10**).

3.2 Quasi static model

Hasegawa *et al.* [3] have demonstrated the existence of three fundamental modes of propagation : "quasi-TEM mode", "skin effect mode" and "slow wave mode". For high conductivity values, the substrate acts as an imperfect ground plane, which leads to a skin effect mode. For intermediate values of substrate resistivity, the slow wave mode propagates in the low frequency area. Actually, the quasi static analysis has been conducted on high resistivity material only, since, for such a substrate, the quasi TEM mode propagates at high frequencies (>1 GHz).

We considered a classical R,L,C,G model (fig.4) where $R_s+jL_s\omega=\gamma Z_c$ and $G_{sub}+jC_d\omega=\gamma/Z_c$. R_s represents the total series resistance, L_s the longitudinal inductance, C_d the dielectric capacitance and G_{sub} the substrate conductance per unit length. R_s, L_s, C_d and G_{sub} are extracted from the γ and Z_c values.

In the quasi static approach, L_s is generally expressed as [4] :

$$L_s = \frac{1}{4c^2\varepsilon_0 F} f_c \qquad (4)$$

where c is the light velocity and F is a geometric empirical factor given by :

$$F = \begin{cases} \dfrac{\ln\left[2\dfrac{(1+\sqrt{k})}{(1-\sqrt{k})}\right]}{\pi} & \text{if } 0.707 \le k \le 1 \\ \dfrac{\pi}{\ln\left[2\dfrac{(1+\sqrt{k'})}{(1-\sqrt{k'})}\right]} & \text{if } 0 \le k \le 0.707 \end{cases} \qquad (5)$$

Where $k = \dfrac{W}{W+2S}$ and $k' = \sqrt{1-k^2}$

For this model, G_{sub} and C_d are commonly approximated by :

$$G_{sub} = 2\sigma_{SiC}F \text{ and } C_d = 2\varepsilon_{SiC}\varepsilon_0 F f_c \qquad (6)$$

It should be noted that, in this paper, L_s and C_d are corrected by the same factor f_c, very close to 1 (1.05). The introduction of this factor is required by the trapezoidal form of the metal and its thickness, since the above equation assumes infinitesimally thin metallic strip conductor and ground planes [5].

Besides, the substrate conductivity is assumed to be less than 10^{-3} S/m. However, this value is difficult to evaluate accurately, especially at high frequencies. Furthermore, the buffer layer is doped at $3{,}5.10^{15}$ cm^{-3} which approximately corresponds to a 3.1 S/m conductivity. Then, the conductivity used in this model is more than 10^{-3} S/m ($3{,}2.10^{-2}$ S/m), and corresponds to an equivalent conductivity for our multilayer substrate.

We consider the series resistance R_s as the sum of two components [6] : $R_s = R_m+R_l$. R_m is a resistance representing metal losses and R_l the influence of the substrate. R_m takes into account the skin effect in the given metal and the corresponding skin depth is defined by :

$$\delta_m = \frac{1}{\sqrt{\pi f \mu \sigma_m}}. \qquad (7)$$

This expression is defined for an conductor of infinite thickness with conductivity σ_m. In our case the metal thickness is equal to t = 0.9 µm. This problem has been dealt with in ref.[2] in the microstrip case, where the skin effect occurs underneath and on the side of the conductor. But for coplanar waveguides, the skin effect current occurs mainly on the conductor sides as field lines extend to the ground planes. R_m is given by [7] :

$$R_m = \frac{1}{2\sigma_m\delta_m t\left[1-\exp\left(\dfrac{-W}{\delta_m}\right)\right]\left(1+\dfrac{W}{t}\right)} \qquad (8)$$

The factor (1+W/t) represents fringing effects as indicated in fig.3

R_l depends linearly on frequency and is given by [6] :

$$R_l = \frac{1}{2}\sigma_{SiC}\mu_0\omega \qquad (9)$$

The substrate conductivity value is the same as that used for the G_{sub} calculation. It should be noted that the R_s value includes the contribution of the contact resistance of the probes to metallic pads. We have experimentally extracted it and then included it in the model.

3.3 Comparison of model with experiment

Using equation (4)-(9), the equivalent line parameters per unit length, (R,L,C,G) have been computed as described in section 3.2, and compared with the measured values. Fig. (4), (5), (6) indicate that experimental variations of R,L,C,G, α and Z_c versus frequency are in good agreement with our model.

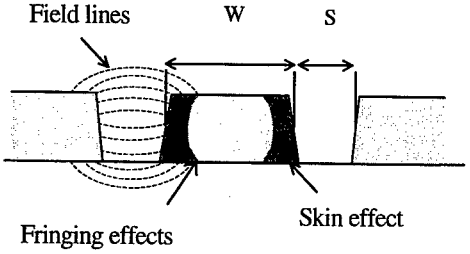

Fig.3 : Field lines and skin effect in the conductor in the case of coplanar waveguide.

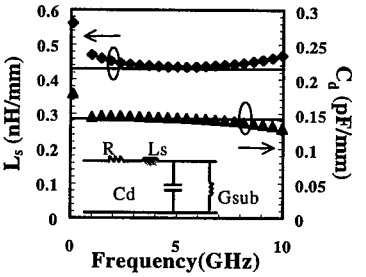

Fig.4 : Measured (data points) and modeled (solid lines) C_d (pF/mm) and L_s (nH/mm)

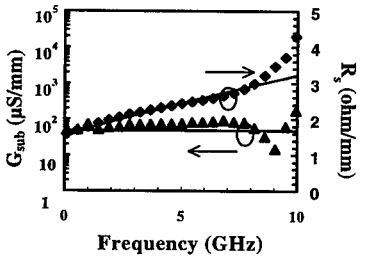

Fig.5 : Measured and model series resistance R_s (ohm/mm) and conductance G_{sub} (µS/mm)

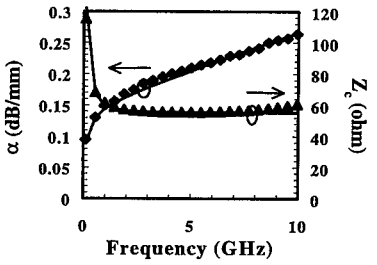

Fig.6 : Measured and modeled attenuation constant α (dB/mm) and characteristic impedance Z_c (ohm)

Then, ε_{reff} and tanδ are calculated from γ , G_{sub} and C_d parameters. The value of ε_{reff} at high frequencies corroborates the quasi-TEM mode, since $\varepsilon_{reff} = (\varepsilon_{r(4H\text{-}SiC)}+1)/2=5.5$ [4], and $\tan\delta = G_{sub}/(C_d\omega)$ reaches 2.8×10^{-3} at 8 GHz and more.

Conclusion

SiC coplanar waveguides on various substrates have been investigated. The attenuation constant extraction shows that combining semi-insulating SiC substrates and copper metallisation results in enhanced performance in term of microwave losses. A classical R, L, C, G model has been used to model the transmission lines on semi-insulating SiC. The calculated line parameters are in a very good agreement with measured values, which proves that SiC structures can be modeled with a standard approach.

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High Temperature, High Current, 4H-SiC Accu-DMOSFET

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Keywords: Accumulation Layer, High Power, High Temperature, MOSFET

Abstract

Planar 4H-SiC Accu-DMOSFETs have been designed, fabricated and characterized, and the highest reported current (>1 Amp) for this type of device was achieved at both room temperature and 350°C. The highest breakdown voltage obtained on a 1200 mΩ-cm^2 device was 904 V. The specific on-resistance obtained on another 439 V device was measured to be 90 mΩ-cm^2 and the accumulation layer mobility is estimated to be in the 5 to 8 cm^2/V-sec range. The temperature variation of on-resistance, channel mobility and threshold voltage is also presented.

Introduction

Power devices made with Silicon Carbide (SiC) are expected to show great performance advantages as compared to those made with other semiconductors. This is primarily because SiC has a high breakdown electric field (2-4x10^6 V/cm), and a high electron mobility [1]. A high breakdown electric field allows the design of SiC power devices with thinner and higher doped voltage blocking layers. Since it can be difficult to diffuse impurities in SiC, a UMOSFET offers a simple way to fabricate a MOSFET. While 560 V, 2 A UMOSFETs have been demonstrated at Cree [2], it suffers from a fundamental oxide breakdown concern at the gate trench bottom. A double-diffused DMOSFET offers good high temperature reliability because the p+ base regions shield the gate oxide from high electric fields during reverse bias operation. In 4H-SiC, a DMOSFET utilizing an accumulation channel layer is expected to show a lower on-resistance as compared to a conventional, inversion channel DMOSFET [3]. This paper describes the design, fabrication and experimental characterization of such a device, called an Accu-DMOSFET.

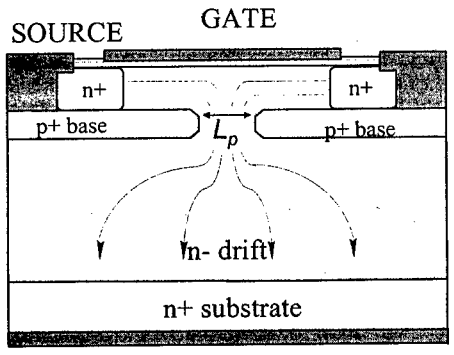

Figure 1: The Accu-DMOSFET structure.

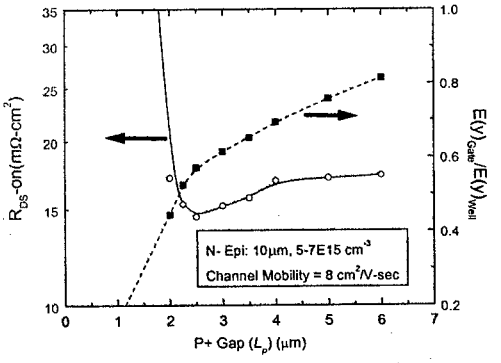

Figure 2: Simulated specific on-resistance and electric field reduction at SiO_2-SiC interface.

The cross-section of the Accu-DMOSFET structure is shown in Figure 1. In this structure, a thin n-type region is formed below the MOS gate by using a buried p^+ implanted layer. The thickness and doping of this n^- layer is chosen such that it is completely depleted by the built-in potentials of the p^+/n^- junction and the MOS gate at zero bias, resulting in a normally-off device. When a positive gate bias is applied, an accumulation channel (of electrons) is created at the SiO_2/SiC interface. As in the case of silicon, SiC should also show higher accumulation mobility as compared to inversion layer mobility, resulting in a lower on-resistance than an inversion-mode device. The fabrication of an Accu-DMOSFET is fairly straightforward and it offers robust performance under a wide operating temperature range.

Design of Accu-DMOSFET

A 12 μm n^- epitaxial layer with a doping of 5-7E15 was grown on an n^+ 4H-SiC substrate. The buried p^+ layer was located between 0.3 μm and 0.7 μm from the surface. To obtain reasonable reliability for a device, the electric field in the SiO_2 must be restricted to below 3 MV/cm. The Accu-DMOSFET achieves this by suppressing the peak electric field from the SiC-SiO_2 surface, to below the p^+ base region. The influence of p^+ base region spacing (L_p) on the surface electric field is evident from the results of 2-D device simulations, shown in Figure 2 (right scale). The ratio of electric field at the SiO_2-SiC interface to the bottom of the p^+ base region (peak electric field) shows that the electric field at the SiO_2-SiC interface reduces monotonically as L_p is reduced from 6 μm to 1 μm, particularly for L_p values below 2.5 μm.

The dominant sources of on-resistance in this device are: the channel resistance of the accumulation layer; the "JFET resistance" between the adjacent p^+ regions; and the drift resistance of the low doped, voltage blocking layer. Simulation results of Figure 2 (left scale) show that a distinct minima exists for specific on-resistance ($R_{ds.on}$) as L_p is changed from 1 μm to 6 μm. This is because a trade-off exists between the JFET region resistance and the channel resistance. An increase in L_p results in an increase in unit cell pitch, which increases the channel resistance per unit area. On the other hand, as L_p is reduced below 2.5 μm, a dramatic increase in the JFET region resistance occurs because of a reduced current carrying width between adjacent p^+ base regions. Relatively low accumulation channel mobility (μ_{acc}) of 8 cm^2/V-sec was used in these simulations because this is the value obtained in our first attempt to fabricate this device. Two different L_p designs were fabricated on this first batch of devices - 2 μm and 6 μm to observe the effect of this parameter on the performance of this device. A mesa edge termination was chosen for this design because of its reliability from the past devices processed at Cree. Devices were laid out with channels both parallel and perpendicular to the wafer flat. The two device sizes fabricated were 0.7 mm×0.7 mm and 1.5 mm×1.5 mm, with a cell pitch of 16 μm.

Device Fabrication

First, buried p^+ layer was ion implanted at high temperature, followed by the ion implantation of the n^+ source region at high temperature. A high temperature implant anneal step was then performed to activate the implanted species. Another mask was used to expose the buried p^+ layer by reactive ion etching so that the p^+ base layer could be electrically connected with the source region. A deep RIE etch was then performed to form the mesa edge termination. A thick oxide layer (>2 μm) was then deposited via LPCVD on the wafers to passivate the surface of the termination region. After etching the thick oxide from the active area, a thinner gate dielectric (800 Å) was deposited via LPCVD and annealed. Windows in the oxide were etched and the emitter metal contacts were deposited. Nickel contacts were used for the n^+ source ohmics and shorts to the implanted p^+ base region. Ni was also blanket deposited on the back of the devices forming the drain contacts. After the contacts were annealed, gold overlayers were deposited on top of all of the contacts to obtain a low bus resistance.

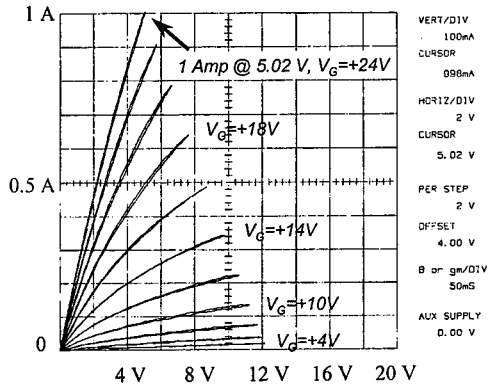

Figure 3: A current of 1 A at gate bias of +24 V obtained on a 1.5mm×1.5mm 4H-SiC Accu-DMOSFET.

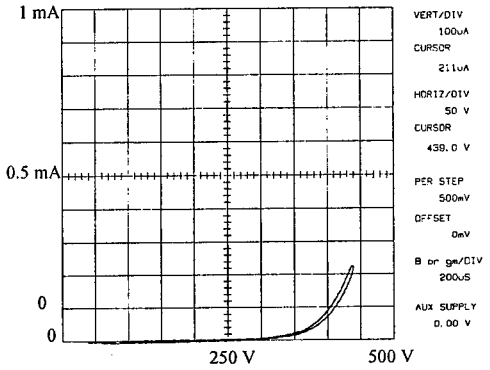

Figure 4: Forward blocking characteristics of high current 0.7mm×0.7mm 4H-SiC Accu-DMOSFET at gate bias of 0V.

Experimental results

Figure 3 shows the room temperature forward I-V characteristics of the highest current 4H-SiC Accu-DMOSFET fabricated to date. The $R_{ds.on}$ obtained on this device is about 90 mΩ-cm^2 and μ_{acc} is estimated to be 5 cm^2/V-sec. This device exhibited no drift in I-V characteristics with time and no gate-source leakage current up to a relatively high gate bias of +40 V. The threshold voltage on this device was about +2 V, but there was a 35 μA residual drain current at zero gate bias and drain bias of +10 V. This device showed excessive leakage at only 141 V drain bias. This device was formed with L_p=2 μm and channel current flow was 0° with respect to the wafer flat. On smaller (0.7mm×0.7mm) devices fabricated on the same wafer, a low on-state specific on-resistance of only 92 mΩ-cm^2 at a +20 V gate bias was obtained. The blocking voltage obtained on this device was 439 V as shown in Figure 4. The highest breakdown voltage obtained on an Accu-DMOSFET was 904 V, but it had an $R_{ds.on}$ of 1200 mΩ-cm^2 at V_G=40 V, and a threshold voltage of +24 V. Test structures on the wafer show that source contact resistance was 5x10^{-5} Ω-cm^2 and the n$^+$ sheet resistance was 525 Ω/sq.

High temperature characteristics

Figure 5 shows the on-state I-V characteristics of a >1 Amp Accu-DMOSFET at 350°C. Attempts to operate at higher temperatures led to failure of these devices. The threshold voltage

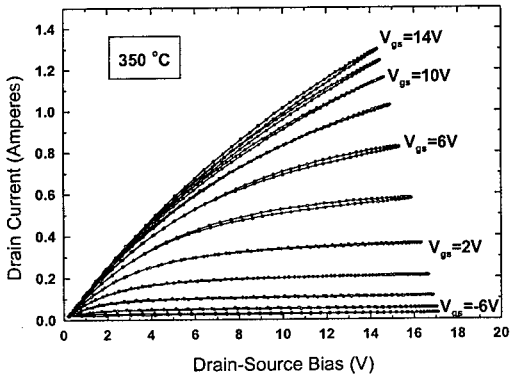

Figure 5: A high temperature >1 Amp 4H-SiC Accu-DMOSFET with an active area of 0.02 cm^2.

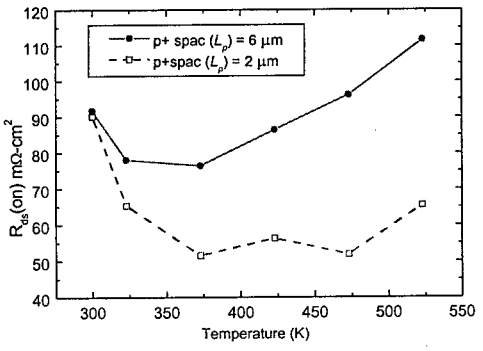

Figure 6: R_{ds}(on) vs. Temperature plot of 0.0032 cm^2 4H-SiC Accu-DMOSFETs at a constant V_G-V_T=20 V.

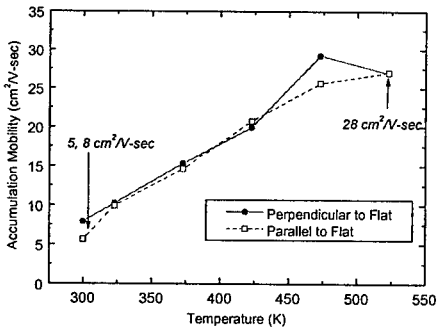

Figure 7: Measured accumulation channel mobility (μ_{acc}) from room temperature to 300°C.

decreases steadily with an increase in temperature and was –6 V at 350°C. The variation of specific on-resistance with temperature at a V_G-V_T of +20 V and drain-source bias of 1 V is shown in Figure 6 for two different values of L_p. The $R_{ds.on}$ of the device with a 6 μm p- well spacing was found to be 90.1 mΩ-cm² at room temperature, which decreases to 51.5 mΩ-cm² at 150°C, and then increases with the temperature. The device with a 2 μm p-well spacing exhibits a similar trend, but with a smaller increase in $R_{ds.on}$ beyond 150°C. The decrease of $R_{ds.on}$ for temperatures up to 150°C is due to an increase of the MOS channel mobility with temperature, and the increase in $R_{ds.on}$ above 150°C is due to an increase in the bulk (JFET and drift region) resistance because of the decreasing bulk electron mobility. Since the JFET resistance of the L_p =2 μm device is larger than that of a L_p=6 μm device, its resistance increases more sharply beyond 150°C. The bulk resistance monitored using a vertical Schottky test structure, shows a monotonic increase from 27 mΩ-cm² at room temperature to 60 mΩ-cm² at 300°C. The measured μ_{acc} in directions perpendicular and parallel to the wafer flat, using a test structure, shows an increase in this temperature range for both directions. At room temperature, μ_{acc} parallel to the flat was measured to be 7.88 cm²/V-s, which is approximately 40% greater than that in the perpendicular direction (5.62 cm²/V-s), as shown in Figure 7. However, this difference disappears at higher temperatures and the effective μ_{acc} increases to 27.0 cm²/V-s at 300°C. The measured leakage current level is around 1.5 mA for 2 μm p-well pitch devices and around 500 μA for 6 μm p-well pitch devices. The leakage current was found to be relatively independent of temperature and could be further reduced by applying a larger negative bias to the gate. This indicates that channel leakage rather than the pn junction or the oxide leakage dominates. Therefore, further optimization is required in the gate oxide processing and implant activation in order to reduce the leakage current and stabilize the threshold voltages.

Conclusions

Planar 4H-SiC Accu-DMOSFETs were designed, fabricated and characterized, and the highest reported current (> 1 Amp) for this type of device was achieved. The highest breakdown voltage was 904 V. The specific on-resistance obtained for a 0.7mm×0.7mm device blocking 439 V was about 90 mΩ-cm². These devices were operated up to a maximum temperature of 350°C. Many layout designs were analyzed and the highest room temperature accumulation layer mobility observed was about 8 cm²/V-sec for gate fingers parallel to the flat. However, the variation of accumulation mobility with orientation was negligible at higher operating temperature. Further optimization of the accumulation mobility, edge termination and gate dielectrics is required.

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4H-SiC Self-Aligned Implant-Diffused Structure for Power DMOSFETs

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Keywords: Diffusion, DMOSFET, Implantation, Power Devices

Abstract

In this paper we report the first self-aligned vertical implant-diffused (VID) and lateral implant – diffused (LID) MOSFET test structures in 4H-SiC by using the differing diffusivities of implanted boron and nitrogen in silicon carbide. Boron diffusion was studied with and without nitrogen co-implants. The optimal diffusion conditions resulted in a 1 μm lateral diffusion width. A blocking voltage of 300 V was achieved in these test structures with a blocking layer thickness of only about 2 μm.

Introduction

Because of the high performance, reliability of design, and the relative ease in fabrication obtained by using diffusion to form a self-aligned gate, the self-aligned DMOS structure is the most common power MOSFET design produced in the Si industry. The reason this structure has classically not been considered for SiC MOSFETs was because of the extreme temperatures required for obtaining significant dopant diffusion in SiC. At these temperatures, severe degradation of the SiC surface can occur, resulting in step bunching and silicon evaporation.

All SiC DMOSFETs reported to date have utilized a double implanted MOS (DIMOS) [1-3] structure instead of the conventional, less expensive, diffused MOS (DMOS) structure with a self-aligned channel. The DIMOS structure requires separate implant masks for the formation of the source and channel regions. In addition, these devices have demonstrated relatively low channel mobility, a possibly due to damage imparted to the channel by the implantation process. Unlike Si, it is difficult to fully remove this implant damage in SiC. This damage can degrade the mobility severely through the implanted regions.

Thus, a diffused DMOSFET should have substantial fabrication and performance advantages over the DIMOS device. The first step in pursuing such a device is to understand and control the dopant diffusion. Boron was chosen as the dopant species because it acts as a p-type dopant in SiC, and diffuses more easily than Al, the other common p-type dopant in SiC.

Dopant Diffusion

The diffusivity of implanted boron and nitrogen in 4H-SiC at different implantation conditions (same depth of B and N; B deeper then N; B shallower then N; different order and temperature during implants) and annealing conditions (temperature range of 1500 – 1700°C for 5 - 30 minutes) was measured via SIMS. The most relevant profiles are shown in Figs. 1 and 2.

Fig.1a. shows the diffusion in the "tail" region of the implanted B (90 keV, 2.0×10^{14} cm^{-2}) during a 1700°C anneal for 30 minutes. The boron diffused in this region at anneal temperatures in excess of 1500°C, and did not vary significantly for anneal temperatures between 1500°C and 1700°C. It was found that boron diffuses during the first few minutes of the anneal with an effective diffusion coefficient of 2×10^{-12} cm^2/sec, and then is fairly stable.

The same boron diffusivity was observed in this "tail" region when the B (90 keV, 2.0×10^{14} cm^{-2}) was co-implanted with N (150 keV, 1.8×10^{14} cm^{-2}). However, the boron diffusion concentration starts at 1×10^{17} cm^{-3}, instead of the 1×10^{18} cm^{-3} observed without the co-implants. This implies

that nitrogen co-implants can be used for control of the boron diffusivity in the "tail" region.

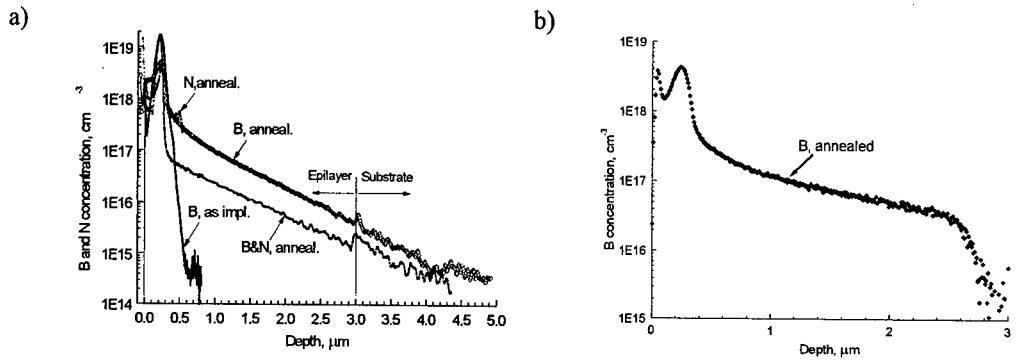

Figure 1. SIMS data for B implants into 4H-SiC before and after annealing at 1700°C for 30 minutes. a) with and without N co-implants along the (0001) axis; b) along the (11$\bar{2}$0) axis.

Fig. 1b demonstrates that the diffusion of implanted B (90 keV, 2.0×10^{14} cm^{-2}) depends on the crystal orientation. Diffusion along the (11$\bar{2}$0) axis is lower than in the (0001) axis. For the DMOSFET, diffusion in the lateral direction will be along the (11$\bar{2}$0) and (1$\bar{1}$00) axes. This lateral diffusion does not demonstrate the long tail observed in the vertical diffusion.

Diffusion of boron towards the surface is important for two reasons: 1) the boron can evaporate from the surface, dramatically reducing the amount available for diffusion into the channel region, which would be the lateral direction of a DMOSFET and 2) the boron can compensate the co-implanted nitrogen, increasing the source resistance.

Fig. 2 shows the B diffusion in the near-surface region. Fig. 2a illustrates the effect of anneal temperature on the boron distribution using 1500, 1600, and 1700°C anneals for 10 minutes. These samples were implanted at room temperature (RT) by B^+ (180 keV, 4×10^{15} cm^{-2}) and co-implanted with N^+ (25 keV, 1.5×10^{14} cm^{-2} and 60 keV, 2.5×10^{14} cm^{-2}). As shown on Fig.2a, implanting N^+ after B^+ reduces the evaporation of boron through the surface during anneals up to 1600°C. At 1700°C, the B significantly diffuses towards the surface.

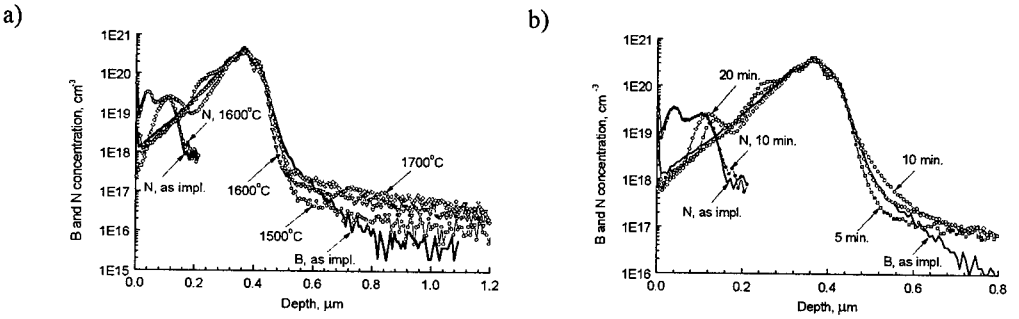

Fig. 2. B and N distributions as measured via SIMS after annealing at a) at 1500°C, 1600°C, or 1700°C for 10 minutes and b) at 1600°C for 5, 10 or 20 minutes.

In Fig. 2b, the B does not diffuse towards the surface during the 1600°C anneal for 5 or 10 minutes, but does during the 20 minute anneal. Although not illustrated in these figures, B annealed without the N co-implants diffuses towards the surface with a concentration level of about 1×10^{19} cm^{-2} and evaporates.

The diffusion of nitrogen in SiC was negligible and can be used as a reference for identifying etching or growing processes during an anneal. As reported by T. Troffer et. al. [5], a boron peak within 40 nm of the surface was measured. However, this peak can be the result of a growing process during an anneal in the prescense of SiC vapor, as identified by using the N peak as a

reference or "marker" as shown on Fig.1a near the surface.

DMOS Device

DMOS test structures and FETs were fabricated with 3 μm thick epilayers (N_d-N_a= 2.2E15 cm^{-3}) on n-type substrates (N_d-N_a= 3E18 cm^{-3}) by using B^+ (180 keV, 4E15 cm^{-2}) and N^+ (25 and 60 keV with 1.5 and 2.5E14 cm^{-2}, respectively) implants into the same well at room temperature and anneals in the temperature range of 1500 – 1700 °C for 5 - 30 minutes. The cross section and top view of the DMOSFET are shown in Figure 2. The source-drain spacing varied from 0.5 to 30 μm. The gate oxide was 25 nm thick.

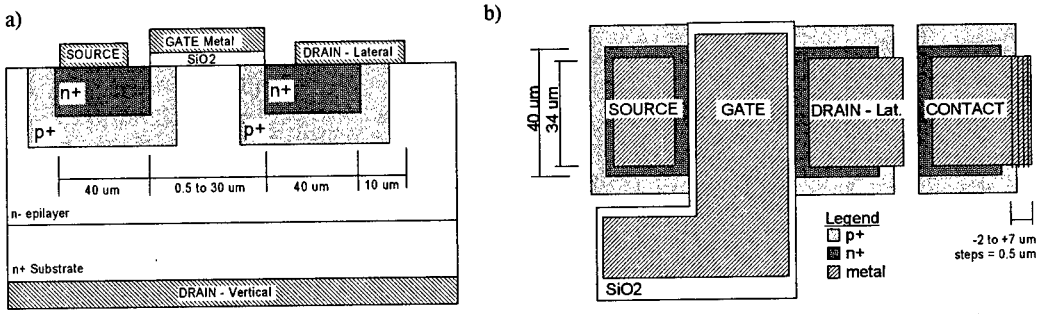

Fig.3. a.) Cross-sectional and b.) top-view of the test structure design for a vertical and lateral 4H-SiC n-channel implant diffused DMOSFET.

An example of one of the designs for this DMOSFET test structure is shown in Fig. 3, in both a cross-sectional and planar-view, with some of the critical dimensions. Two different structures for two different measurement techniques were designed in order to accurately determine the lateral boron diffusion distance. The first design consisted of a combined vertical and lateral MOSFET structure. Referring to Fig. 3, the first test structure consists of the Source, Gate, Drain-Lat (lateral) and Drain-Vert (vertical) regions. By incrementally narrowing the Source-to-Drain_Lat spacing, the test structure is transformed from a vertical MOSFET to a lateral MOSFET. Initially, with a Source-Drain_Lat spacing of 30 μm, the Source and Drain_Vert nodes act as the source and drain, respectively, of a vertical MOSFET. The diffused p-type boron region acts as the channel of the n-channel MOSFET.

As the Drain_Lat region is moved closer to the Source region, at some point the two p-type boron regions merge, creating a channel between the Source and the Drain_Lat regions; hence a lateral MOSFET device. As shown in the figure, the Drain_Lat contact overlaps the n^+ and p^- regions of the drain, creating a substrate tie-down for the lateral device. By characterizing the 4-terminal device (3 top + bottom) and noting at which Source-Drain_Lat spacing the transition was made from a vertical to a lateral MOSFET, the boron diffusion distance could be determined. The maximum spacing was 30 μm and the minimum was 0.5 μm, with 0.1 increments in between these values for each reticle.

The second method for verifying the boron diffusion distance can be seen in Fig. 3b. A 2-terminal device is formed between the n-type region (labeled Contact) and the Drain_Vert region. The contact is incrementally stretched from the n-type nitrogen region, across the p-type boron region, and eventually to the n- epilayer. Initially, the Contact is fully enclosed by the n-type nitrogen region, creating an NPN transistor where the n-type nitrogen implant is the emitter, the diffused p-type boron region is the floating base, and the n-epilayer is the collector. Because there are back-to-back diodes, no current can be measured vertically through the chip. As the edge of the contact is stretched across the nitrogen-boron junction, the emitter and base regions are shorted together, yielding a diode between Contact and Drain_Vert, and the pn junction I-V characteristics can be observed. Finally, as the edge of the contact is stretched past the diffused boron region, the emitter, base and collector of the NPN device are shorted together, creating a resistive short between Contact and Drain_Vert. By characterizing the 2-terminal device and noting at which contact-overlap spacing the transition was made from a diode to a resistor, the boron diffusion distance could be determined.

The channel length was determined to be about 1.0 μm (thus the lateral boron diffusion length in excess of nitrogen diffusion was about 1.0 μm). The annealing condition that yielded this result was

the 1600 °C, 10 minute anneal. Other annealing conditions resulted in less diffusion or lower activation of boron in the channel region. The 1 μm lateral diffusion of the implanted B was in agreement with the distances measured on test samples with SIMS.

The DMOSFETs had a p-type channel surface concentration of about 2.5×10^{18} cm^{-3}, determined by the relatively high threshold voltage of $V_G = +6V$ and the gate oxide thickness of 25 nm. Figure 4a demonstrates the standard MOSFET characteristics that were observed, with excellent current saturation, indicating that there were no short-channel effects. The on-current at $V_G = +18$ V was

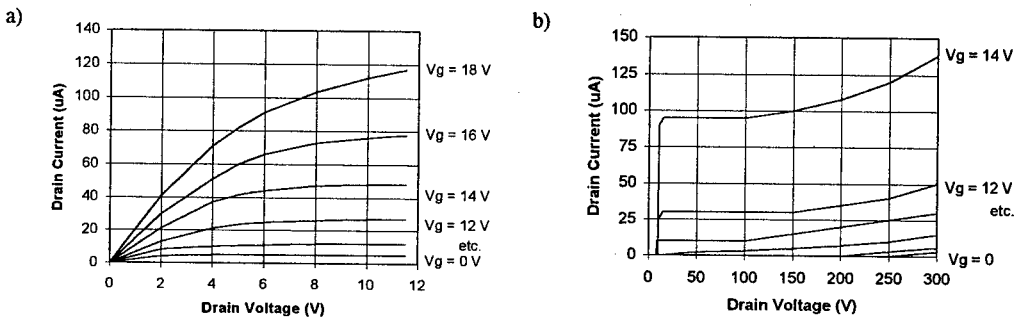

Fig.4. I-V characteristics of self-aligned 4H-SiC DMOS test structures produced by room temperature B^+ and N^+ implantation and annealed at 1600°C for 10 minutes at a) low drain voltage and b) high drain voltage, showing 300 V blocking voltage for an approximate blocking layer thickness of <2μm (W = 80 μm, L_G = 1 μm).

about 1.5 mA/mm of gate periphery. The channel mobility derived from the I-V characteristics and the gate length that was measured for this diffused 4H-SiC vertical test structure was $\mu_n = 0.6$ cm^2/V-sec, at a gate bias of 18 V (12 V above the threshold voltage). The best channel mobility in lateral DMOS structure was $\mu_n = 1.5$ cm^2/V-sec. This value is quite low, but is not a typical for lateral MOSFETs in 4H-SiC. It has been proposed that the very low channel mobilities in 4H-SiC are due to a high density of interface states near the conduction band [4,6].

The highest blocking voltage achieved on these devices was 300 V, as shown in Figure 4b. This is despite the fact that the n^- blocking layer, after the boron was diffused, was probably less than 2 μm thick, and there was no high voltage edge termination on these devices.

Conclusions

The gate control and excellent blocking voltage of these DMOSFETs demonstrate for the first time that a DMOS technology in SiC may be a viable alternative to the DIMOS and UMOS structures. The feasibility has been demonstrated for developing a self-aligned DMOS technology in SiC that can achieve high voltage operation with greatly reduced fabrication costs. However, the low channel mobilities for these 4H-SiC devices indicates that further research is needed.

Acknowledgements

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Materials Science Forum Vols. 338-342 (2000) pp. 1279-1282

Nitrogen vs. Phosphorus as Implant Species for High-Voltage Lateral RESURF MOSFETs on 4H-SiC

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Keywords: 4H-SiC, MOSFET, Nitrogen, Phosphorus, RESURF

Abstract

A comparison of nitrogen vs. phosphorus as implant species for source/drain and RESURF region in high-voltage lateral RESURF MOSFETs in 4H-SiC indicates that phosphorus is good for source/drain implants and nitrogen is preferred for the RESURF region due to the better activation for low doses at low implant anneal temperatures. RESURF MOSFETs with blocking voltages in excess of 1200V have been obtained with a specific on-resistance of $4\Omega.cm^2$.

1. Introduction

Owing to high critical electric breakdown field and large energy gap, SiC has been established as the most promising candidate for high-voltage power semiconductor devices. Lateral high-voltage devices are ideal for the integration of logic circuits in power IC's. 2.6kV lateral MOSFETs have recently been fabricated on semi-insulating 4H-SiC[1]. The on-resistance of lateral devices can be reduced by the REduced SURface Field (RESURF) principle[2]. Lateral RESURF MOSFETs have been demonstrated in 4H-SiC[3] and 6H-SiC[4]. The activated charge in the RESURF region is a critical parameter for the RESURF MOSFET. In this paper, the performance of devices fabricated with nitrogen and phosphorus as source/drain and RESURF region implants activated at 1200°C and 1600°C is compared.

2. MOSFET Fabrication

The 4H-SiC wafers used for the fabrication of the lateral RESURF MOSFETs had a p-type epitaxial thickness and doping of 10 μm and 4×10^{15} cm^{-3} respectively. Table 1 shows the process splits, gate oxide thickness and the implantation scheme chosen for the fabrication. The fabrication information for sample N1 is described in detail elsewhere[5]and that of the other samples in Table 1 is similar. The optimum dose for the RESURF region was estimated from 2-D simulations to be $\sim1\times10^{13}$ cm^{-2} (Fig. 1). Samples N1 and N2 were implanted with nitrogen with a source/drain and RESURF dose of 3×10^{15} cm^{-2} and 5×10^{13} cm^{-2} respectively. Samples P1 and P2 were fabricated with phosphorus as the implant for source/drain (dose: $4\times10^{15}cm^{-2}$) and the RESURF region (dose: $2\times10^{13}cm^{-2}$). Sample P1 and N1 were annealed at 1200°C for 60 min in argon and the samples P2 and N2 were annealed at 1600°C for 10 min in argon. The schematic of cross-section of the lateral RESURF MOSFET fabricated is shown in Fig. 2.

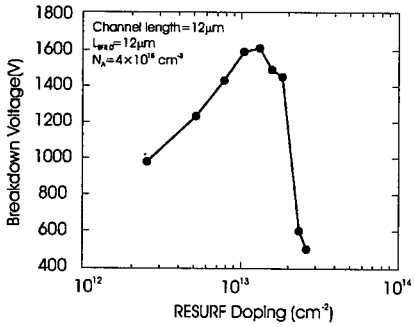

Fig. 1: Breakdown voltage vs. RESURF region doping for 4H-SiC

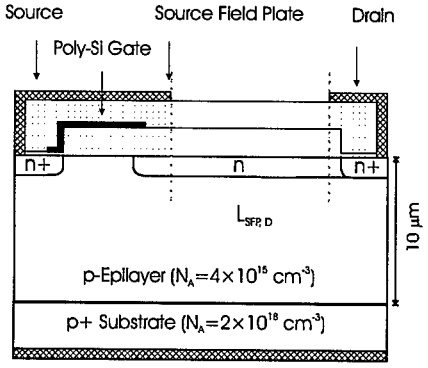

Fig. 2: Crossectional view of lateral RESURF MOSFET in 4H-SiC

3. Results and Discussion

Experimental results were obtained on self-enclosed circular geometry RESURF and non-RESURF MOSFETs with width of 600μm, channel lengths of 4 and 6μm. The RESURF MOSFETs had a source-field-plate-to-drain spacing($L_{SFP,D}$) of 0, 4, 8, and 12μm. The I_D-V_D characteristics for a RESURF device with L_{ch}=6μm and $L_{SFP,D}$ = 12μm is shown in Fig. 3. Room temperature breakdown voltage of 1230V with a specific on-resistance ($R_{on,sp.}$) of 4 Ω.cm^2 was obtained for this device. The total on-resistance of a lateral RESURF MOSFET consists of contributions from the source/drain contact, n$^+$ source/drain regions, channel and the RESURF region. An estimate of the on-resistance contributions for this device, shown in table 2 indicates that 90% of the on-resistance is due to the channel resistance, due to the very low inversion layer mobility in these devices($\sim$ 0.1-2 cm^2/V.s).

The breakdown voltage vs. $L_{SFP,D}$ for L_{ch}=4 and 6μm is shown in figure ??. The breakdown voltage increases linearly with increase in $L_{SFP,D}$ and does not depend on the L_{ch}. The breakdown voltage measurement on non-RESURF MOSFETs indicates that the channel region supports $\sim$50V.

RESURF MOSFETs with implantation anneals performed at 1600°C were also fabricated (sample N2). These devices had a poor breakdown voltage (<100V) because of the high RESURF charge due to better activation of implants at 1600°C. The low breakdown could also possibly be due to the surface roughness due to the high temperature anneal. The on-resistance of this device was similar to the sample N1. RESURF MOSFETs were also fabricated using phosphorus as the source/drain and RESURF region implant species. Phosphorus has been shown to be an ideal

Table 1: Process Split and Implantation Scheme for lateral RESURF MOSFET

Sample	Gate Oxide Thickness(nm)	N$^+$ Implant	RESURF Implant	Implant Anneal Temperature (°C)	Breakdown Voltage ($L_{SFP,D}$=12μm)
N1	900	N	N	1200	1230
N2	300	N	N	1600	<100
P1	100	P	P	1200	1100
P2	100	P	P	1600	<100

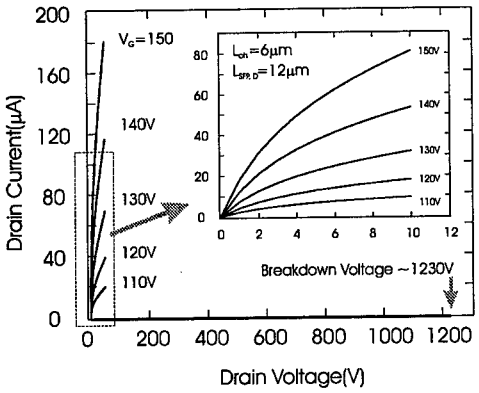

Fig. 3: Drain characteristics of a RESURF MOSFET with $L_{SFP,D}$=12μm, L_{ch}=6μm on sample N1

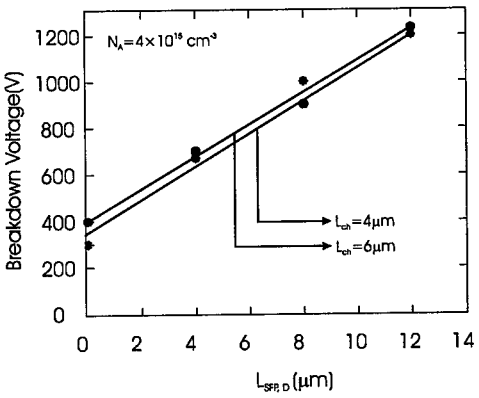

Fig. 4: Experimental breakdown voltage vs. $L_{SFP,D}$ for L_{ch}=4 and 6μm on sample N1

candidate as a heavily doped n-type implant species in 4H-SiC having a sheet resistance as low as 160Ω/sq and 250Ω/sq after 1600°C and 1200°C implant anneal temperatures respectively[6]. These values are much lower than that obtained with nitrogen ($3\times10^3\Omega$/sq and $1.3\times10^4\Omega$/sq after 1600°C and 1200°C anneals). The specific contact resistvity obtained with phosphorus ($\sim 10^{-4}\Omega.cm^2$)was an order of magnitude lower than the contact resistivity obtained with nitrogen.

Samples P1 and P2 were fabricated with phosphorus as the implant species for both source/drain and RESURF region and were annealed at 1200°C and 1600°C respectively. Sample P1 exhibited a high breakdown voltage (~1100V for $L_{SFP,D}$=12μm)(Fig. 5) but a high specific on-resistance. The high specific on-resistance for sample P1 is due to the large RESURF region resistance; this is supported by the low specific on-resistance of non-RESURF MOSFETs ($3.7\Omega.cm^2$) on the same wafer indicating that the on-resistance is not dominated by channel resistance. A sheet resistance and specific contact resistance of 850Ω/sq. and $1\times10^{-4}\Omega.cm^2$ was obtained on these devices. The high RESURF region resistance is due to the poor activation of the low dose phosphorus implants at 1200°C implant activation anneal. Sample P2 exhibited a poor breakdown voltage due to the non-optimum RESURF charge but had a low specific on-resistance ($R_{on,sp.}$=0.45Ω cm^2 for $L_{SFP,D}$=12μm, L_{ch}=6μm)(Fig. 6).It has been reported that high implant activation anneal temperatures roughens the SiC surface, thereby degrading the inversion layer mobility[7]. Since high inversion layer mobility is required in order to reduce the channel resistance contribution to the on-resistance, low implant activation anneal temperatures are desired.

Table 2: Estimated On-Resistance Contributions

	R_{ch}	R_{RESURF}	R_{source}	R_{drain}
R(Ω)	1.3×10^4	1.1×10^3	195	230
Specific On-resistance Contributions(%)	90	8	1	1

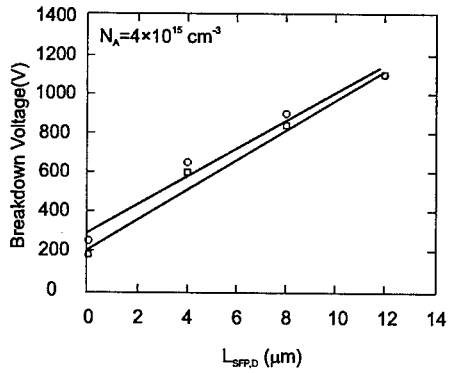

Fig. 5: Experimental breakdown voltage vs. $L_{SFP,D}$ for L_{ch}=4 and 6μm on sample P1

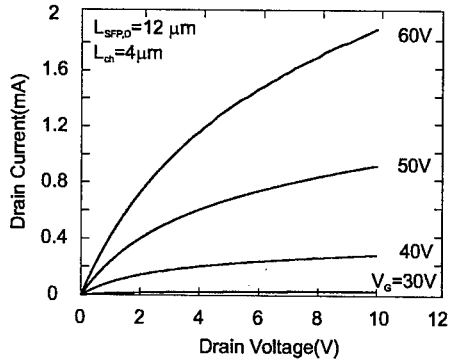

Fig. 6: Drain characteristics of a RESURF MOSFET with $L_{SFP,D}$=12μm, L_{ch}=6μm on sample P2

4. Conclusion

Lateral RESURF MOSFETs were fabricated in 4H-SiC using nitrogen and phosphorus as implants for source/drain and RESURF region and implant anneal temperatures of 1200°C and 1600°C. The devices annealed at 1600°C do not exhibit high breakdown voltage, while devices annealed at 1200°C exhibited high breakdown voltage. The RESURF MOSFETs using nitrogen as the implant species and annealed at 1200°C exhibited a specific on-resistance of 4Ω.cm^2 while devices with phosphorus as the RESURF implant had a high on-resistance. Thus, we recommend phosphorus for the source/drain and nitrogen for the RESURF region implant. Currently, we are fabricating RESURF MOSFETs with phosphorus source/drain and nitrogen as the RESURF region implant.

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Materials Science Forum Vols. 338-342 (2000) pp. 1283-1286

Effect of Off-Angle from Si (0001) Surface and Polytype on Surface Morphology of SiC and C-V Characteristics of SiC MOS Structures

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Keywords: C-V Characteristics, MOS Structure, Off-Angle, Polytype, Surface Morphology

Abstract

We have investigated the relationship between the surface morphologies of 3.5° and 8° off-angled 6H-SiC (0001) and 8° off-angled 4H-SiC (0001) substrates and the C-V characteristics of SiC MOS structures. C-V characteristics and atomic force microscopy (AFM) observations revealed that the D_{it} and the step height increased with increasing the off-angle. It is considered that these contribute to origins of low channel mobility for 4H-SiC MOSFETs.

Introduction

6H- or 4H-SiC substrates are expected to be higher temperature, higher power, and higher frequency devices for the next generation because of higher electric field breakdown strength, higher saturated electron velocity, and higher thermal conductivity than Si power devices. Power metal-oxide-semiconductor field-effect transistors (MOSFETs) are superior to bipolar transistors due to their fast switching speeds and small switching losses. Therefore, power MOSFETs are considered to be one of a promising target for power SiC devices. Many researchers have studied SiC MOSFETs [1]-[3]. The channel mobility of 4H-SiC MOSFETs are reported to be lower than those of 6H-SiC MOSFETs although the mobility of 4H-SiC estimated from the Hall measurements is higher than that of 6H-SiC [4],[5]. This is a large problem for practical use of 4H-SiC MOSFETs. Usually, 6H-SiC and 4H-SiC MOSFETs is fabricated on 3.5° and 8° off-angled SiC (0001) substrates, respectively. It can be thought that the off-angle affects the surface morphology and the interface state density (D_{it}).

In this paper, we have investigated the effect of off-angle from Si(0001) surface and polytype on surface morphology of SiC and capacitance-voltage (C-V) characteristics of SiC MOS structures.

Experimental

3.5° and 8° off-angled 6H-SiC (0001) and 8° off-angled 4H-SiC (0001) substrates with n-type epitaxial layer were purchased from Cree Research. The 8° off-angled 6H-SiC (0001) substrate was specially fabricated for this study. After the standard RCA cleaning, sacrificial oxide films were grown in dry O_2, and then were removed by 5% HF solution, and surface morphology was observed using atomic force microscopy (AFM). 50nm thick gate oxide films were thermally grown at 1200 °C in dry O_2. We have reported that H_2 annealing reduced the D_{it} of 4H-SiC MOS structures[6],[7], so samples were annealed in H_2 at 1000 °C for 30 min after the oxidation. Ar was also used for comparison of the annealing effect. Aluminum was evaporated on the top and the back of the sample for gate electrodes and ohmic contacts, respectively. C-V measurements were performed using HP 4274 LCR meter and HP 4140B pA meter in a shielded dark box at room temperature.

Results and Discussion

1. C-V characteristics

Figure 1 shows high-frequency (solid lines, f=100kHz) and quasi-static C-V (dotted lines, sweep rate=0.01V/s) characteristics of 3.5° and 8° off-angled 6H-SiC, and 8° off-angled 4H-SiC MOS structures, and ideal one (dashed line). The ΔV_{fb} of SiC MOS structures with various polytypes, off-angles and annealing gases are summarized in Table 1. The C-V characteristics of 3.5° off-angled 6H-SiC MOS structure with Ar annealing is very closed to the ideal one, and the ΔV_{fb} is –0.1V. The ΔV_{fb} after H_2 annealing is –5.1V. The ΔV_{fb} of the 8° off-angled 6H-SiC MOS structure with Ar and H_2 annealing are -0.2V and –7.7V, respectively. The effect of H_2 annealing on ΔV_{fb} is different even for the same polytype although the ΔV_{fb} of 6H-SiC MOS structure with Ar annealing is independent of the off-angle, and exhibits almost the same value. On the other hand, the ΔV_{fb} of 8° off-angled 4H-SiC MOS structures with Ar and H_2 annealing are 2.1V and –1.2V, respectively. The ΔV_{fb} of 8° off-angled 6H- SiC MOS structure is quite different as compared to that of the same off-angled 4H-SiC MOS structure. The ΔV_{fb} after H_2 annealing is determined uniquely by neither the polytype nor the off-angle, which means that SiO_2/SiC interfaces are different even in the same polytype and the off-angle. The difference between high-frequency capacitance and quasi-static capacitance at the same voltage corresponds to D_{it}. The capacitance difference near the accumulation voltage in 4H-SiC MOS structure is larger than that of the 3.5° off-angled 6H-SiC MOS structure. This means that the D_{it} near the conduction band of 4H-SiC MOS structure is lager than that of the 3.5° off-angled 6H-SiC MOS structure. Figure 2 shows the D_{it} distribution in the band-gap of the 3.5° off-angled 6H- SiC MOS structures with Ar and H_2 annealing, and the 8° off-angled 6H- and 4H-SiC MOS structures with H_2 annealing, which was estimated using high-low C-V method. The D_{it} is obtained from Eq. (1),

$$D_{it} = q^{-1} ((C_q^{-1} - C_{ox}^{-1})^{-1} - (C_h^{-1} - C_{ox}^{-1})^{-1}). \quad (1)$$

where q is the electronic charge, C_{ox} is the oxide capacitance, C_q is the quasi-static capacitance, and C_h is the high-frequency capacitance, respectively [8]. The D_{it} is underestimated at E_c-E above approximately 0.6eV because the measurement is performed at room temperature [9], [10].

The D_{it} of the 3.5° off-angled 6H-SiC MOS structures with H_2 annealing is smaller than that of the 3.5° off-angled 6H-SiC MOS structures with Ar annealing. Therefore, it is confirmed that H_2 annealing also reduced the Dit of 6H-SiC MOS structures. The D_{it} at E_c-E ≤ 0.58 eV in band-gap of 3.5° off-angled 6H-SiC MOS structures with H_2 annealing is much smaller than that of 8° off-angled 4H-SiC MOS structures. In 6H-SiC MOS structures, the D_{it} of 8° off-angle is higher than that of 3.5° off-angle. These results imply that the D_{it} increases as the off-angle steepens.

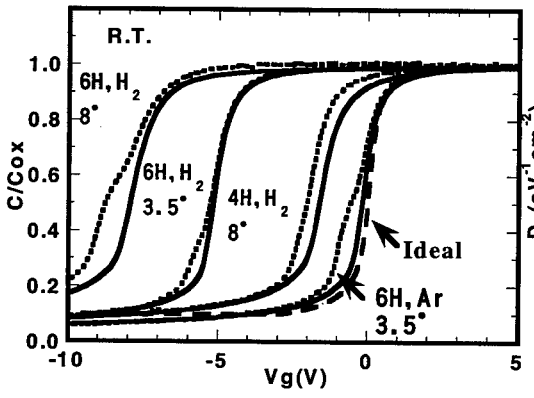

Fig.1 C-V characteristics of SiC MOS structures.

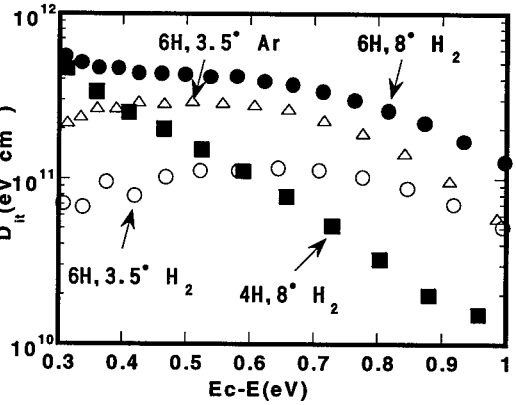

Fig.2 D_{it} distribution in band-gap.

Table 1. ΔV_{fb} of SiC MOS structures with various polytypes, off-angle, and annealing gas.

	6H(3.5°off-angled)	6H(8° off-angled)	4H(8°off-angled)
Ar	-0.1 V	-0.2V	2.1V
H_2	-5.1V	-7.7V	-1.2V

2. Surface Morphology

Figures 3-(a), (b) and (c) show 3 dimensional AFM images (10μm□) of 3.5° and 8° off-angled 6H-SiC (0001), 8° off-angled 4H-SiC (0001) surfaces, respectively. The Ra of (a) is a little smaller than those of (b) and (c). Kimoto et al. reported that there are microsteps with various terrace width and step height on the SiC surface [11]. In order to observe microsteps, 2 dimensional differential AFM images (Fig.4-(a), (b) and(c)) and height profiles (Fig. 5) of local region (1μm□) for the SiC surface were measured. The straight lines due to step edges are observed in Fig.4-(a), (b) and(c). Those on 8° off-angled 4H-SiC (0001) surfaces are the most clear among three samples, which means that the change of height profiles is the steepest. The average step heights of 3.5°off-angled 6H-SiC surface, 8° off-angled 6H- and 4H-SiC surface estimated from the height profiles are 0.3nm, 0.5nm and 0.6nm, respectively. The step heights of 8° off-angled 4H- and 6H-SiC (0001) surfaces are approximately 2 times larger than that of 3.5° off-angled 6H-SiC (0001) surfaces. Furthermore, the amount of dangling-bonds for Si or C atoms become large at the higher off-angled SiC substrates because the summation of the step height at step edges increases as the off-angle increases, resulting in high D_{it} in 8° off-angled 4H-and 6H-SiC MOS structures. It is considered that this high D_{it} and large step height contribute to the lower channel mobility of 4H-SiC MOSFETs than that of 6H-SiC MOSFETs.

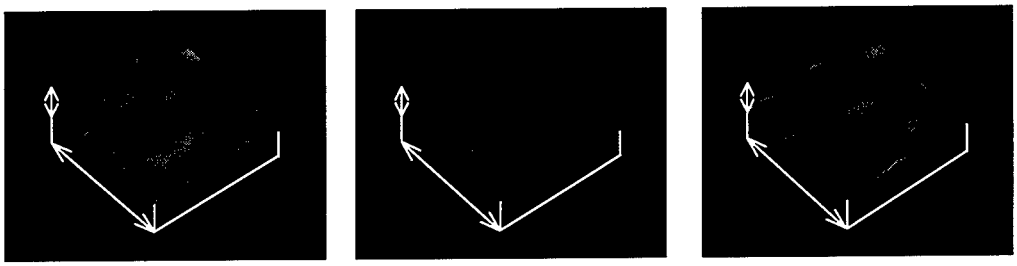

Fig. 3 3-D AFM images (10μm□)of 3.5° off-angled 6H-SiC (0001) surface, and 8° off-angled 6H- and 4H-SiC (0001) surface.
X: 10μm /division, Z: 20nm/division
(a) 6H (3.5° off-angled, Ra=0.42nm) (b) 6H (8° off-angled, Ra=0.58nm) (c) 4H (8° off-angled, Ra=0.47nm)

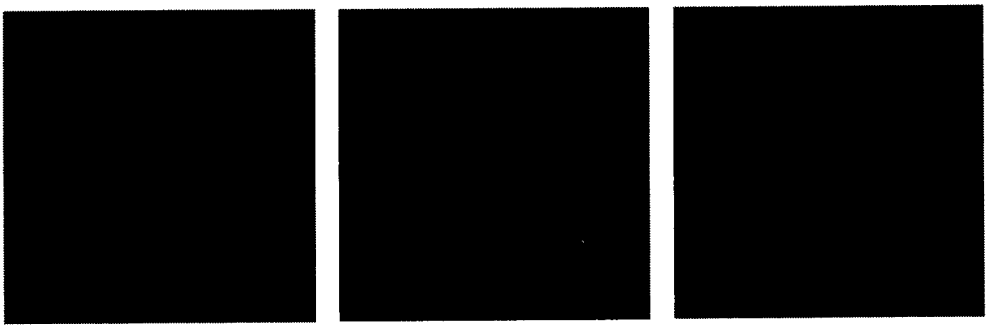

Fig. 4 2-D differential AFM images (1μm□) of 3.5° off-angled 6H-SiC (0001) and 8° off-angled 6H- and 4H-SiC (0001) surface.
(a) 6H (3.5° off-angle) (b) 6H (8° off-angled) (c) 4H (8° off-angled)

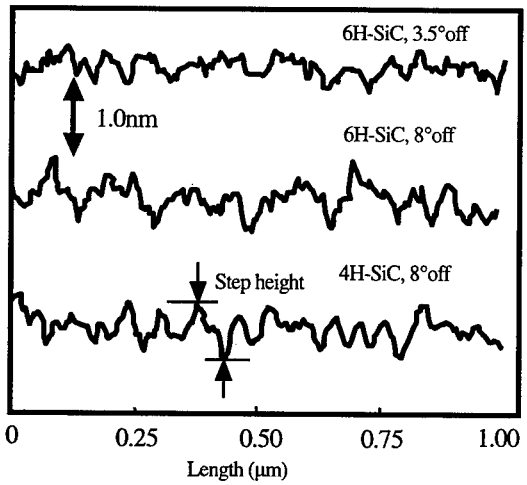

Fig. 5 Height profiles of 3.5° and 8° off-angled 6H-SiC (0001) and 8° off-angled 4H-SiC (0001) surface.

Conclusion

We have investigated the relationship between the surface morphology of 3.5° and 8° off-angled 6H-SiC (0001) and 8° off-angled 4H-SiC (0001) substrate and the C-V characteristics of MOS structures fabricated on these SiC substrates with H_2 and Ar annealing. H_2 annealing reduced drastically the D_{it} as compared to Ar annealing. This technique is very available for accumulation type SiC MOSFETs because they have n-type MOS interfaces. The D_{it} and step height increase with increasing the off-angle. These are considered to contribute to the origin of low channel mobility for 4H-SiC MOSFETs.

Acknowledgement

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Accumulation-Mode SiC Power MOSFET Design Issues

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Keywords: Accumulation Mode, Breakdown Voltage, Edge Termination, MOSFET, Simulation

Abstract

Issues relating to the design of accumulation-mode SiC power MOSFET's which utilize a lateral accumulation channel for MOS gate control and a vertical drift region to support large blocking voltage are investigated using MEDICI device simulation. An optimized device design is expected to have an R_{ON} = 0.04 ohm-cm^2 with a breakdown voltage of 700 V for a drift layer doping of 2 x 10^{16} cm^{-3}. A buried guard ring, edge termination is necessary to achieve the desired high breakdown voltage.

Introduction

SiC MOSFET's have received significant attention because of the performance advantage in terms of lower specific on-resistance, higher breakdown voltage, and higher operating temperature that they promise over comparable Si MOSFET's. Although their demonstrated performance is somewhat superior to Si MOSFET's, their potential performance advantage is even greater [1]. Many of the SiC MOSFET's demonstrated to date [2-5] have used conventional silicon power device designs and therefore do not take full advantage of SiC. On the other hand, an accumulation-mode SiC MOSFET with a lateral channel and a vertical drift region has the potential to better utilize the material advantages offered by SiC technology [6]. The lateral accumulation channel offers lower resistance because the accumulation layer mobility is significantly higher than the inversion layer mobility in SiC. Moreover the lateral channel and vertical drift region structure, when designed properly, can shield the gate oxide from the high electric field in the drift region. In order to better understand the design tradeoffs involved in designing this accumulation-mode SiC MOSFET, two-dimensional device simulations were performed using MEDICI. Material parameters of 4H-SiC are used in the simulation [7]. In cases in which the 4H-SiC material parameters are unknown, values of 6H-SiC are used [8]. The importance of providing a buried edge termination is also discussed.

MOSFET Cell Structure

The cross section of the SiC accumulation-mode MOSFET structure along with the design parameters is shown in Figure 1. Due to the symmetry of the device structure, only half of the cell is shown. In this structure, a buried P^+ layer separates the thin N accumulation channel and the thicker N drift region. The electric current flows laterally in the accumulation channel from the source and then vertically towards the drain contact through the opening between the P^+ buried layers. The P^+ buried layer divides the device into two regions. The region below the buried layer is the drift region which supports most of the applied voltage under reverse bias conditions. This region determines the device performance in the off-state. The channel region above the buried layer determines the device performance in the forward bias condition. The two regions are connected by the opening in the P^+ buried layer. The opening in the P^+ buried layer is called the JFET region. It will be shown later that this opening in the P^+ buried layer is the key design parameter to optimize the device performance for both forward and reverse bias conditions.

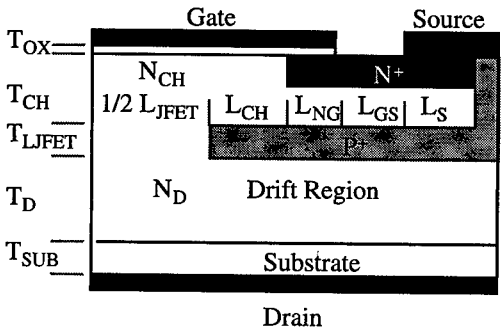

Fig. 1 Cross section of SiC accumulation-mode MOSFET showing all design parameters. Because of the symmetry of the cell design, only half of the cell is shown.

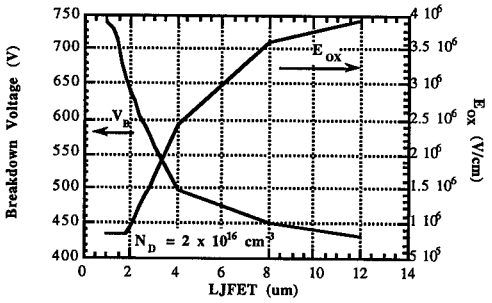

Fig. 2 Effect of L_{JFET} on breakdown voltage and oxide field with $N_D = 2 \times 10^{16}$ cm^{-3}.

The nominal device dimensions used in the MEDICI simulations were: L_S = 3 μm, L_{GS} = 0.9 μm, L_{NG} = 0.7 μm, L_{CH} = 1.3 μm, and L_{JFET} = 2.0 μm. However, L_{JFET} was varied from 1 μm to 12 μm in order to optimize this parameter in terms gate oxide field and device on-resistance. The vertical device dimensions were: T_{OX} = 800 Å, T_{CH} = 0.6 μm, T_{JFET} = 0.5 μm, and T_D = 10 μm. The device doping densities were: $N^+ = P^+ = 1 \times 10^{20}$ cm^{-3}, $N_{CH} = 1 \times 10^{16}$ cm^{-3}, and N_D = 1 or 2 x 10^{16} cm^{-3}. The channel mobility was chosen to be 90 cm^2/V-sec.

MOSFET Cell Design Parameters

As mentioned previously, the most important design parameter in this MOSFET is the size of L_{JFET} because this dimension affects the gate oxide field, device breakdown voltage, and device on-resistance. The effect of L_{JFET} on the gate oxide field and device breakdown voltage with $N_D = 2 \times 10^{16}$ cm^{-3} is shown in Figure 2. As L_{JFET} is increased from 1 μm to 12 μm, the gate oxide field increases from less than 1 x 10^6 V/cm to greater than 3 x 10^6 V/cm. The device breakdown voltage decreases from above 750 V to below 450 V for the same increase in L_{JFET}. The electric field in the SiC remains relatively constant at ≈ 3 x 10^6 V/cm over this range of L_{JFET}. The optimum value for L_{JFET} is near 2 μm because of the need to maximize device breakdown voltage and minimize gate oxide field. Minimization of the gate oxide field will increase device reliability.

Another important design parameter is the device threshold voltage which is plotted versus the channel doping N_{CH} in Figure 3. N_{CH} also affects the device on-resistance R_{ON} which is also shown in Figure 3. The optimum device will have a minimum on-resistance, but since a normally-off MOSFET is preferred, N_{CH} cannot be too large. A good tradeoff between these two requirements

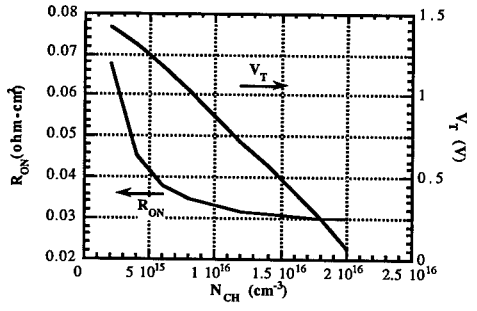

Fig. 3 R_{ON} and V_T versus channel doping.

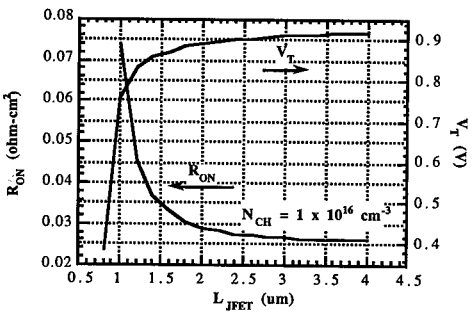

Fig. 4 R_{ON} and V_T versus L_{JFET}.

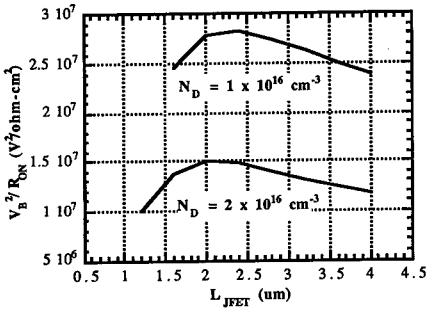

Fig. 5 V_B^2/R_{ON} versus L_{JFET}.

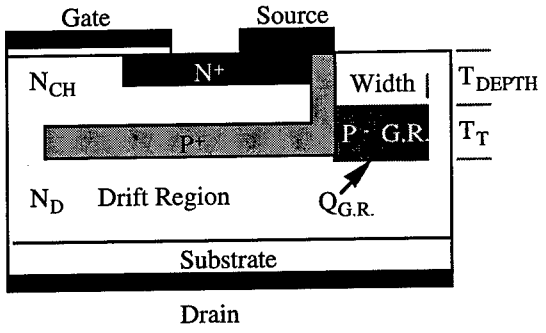

Fig. 6 Cross section of buried guard ring structure showing all design parameters.

can be achieved with N_{CH} = 1 x 10^{16} cm^{-3} which yields a threshold voltage of about +1 V and a relatively low on-resistance 0.03 ohm-cm^2. It should be mentioned that the resistance of the SiC substrate and the source and drain contact resistances have not been included in this on-resistance calculation. Adding these resistances will increase the on-resistance by no more than a few mohm-cm^2. The effect of L_{JFET} on threshold voltage and on-resistance is shown in Figure 4. The on-resistance increases rapidly for L_{JFET} less than 2 μm because of the small opening through which the device current must flow, and therefore from these consideration, L_{JFET} = 2 μm again appears to be an optimum value.

A figure of merit for power devices [9] V_B^2/R_{ON} is shown in Figure 5 versus L_{JFET} for N_D = 1 x 10^{16} cm^{-3} and 2 x 10^{16} cm^{-3}. As L_{JFET} is increased from 1 μm to 4 μm, V_B^2/R_{ON} increases and then decreases peaking for values of L_{JFET} between 2 μm and 2.5 μm. V_B^2/R_{ON} is lower at smaller L_{JFET} because of higher R_{ON}, as shown in Figure 4, and is lower at larger L_{JFET} because of the lower breakdown voltage, as shown in Figure 2. Therefore from a variety of perspectives (Figures 2,4, & 5), L_{JFET} ≈ 2 μm appears to be optimum.

Edge Termination Structure

All switch-mode power devices require some type of edge termination in order to achieve maximum performance. By using artificial boundary conditions, the previous simulations only applied to the power MOSFET cell. However in a complete device the high electric fields at the perimeter of the device must be properly terminated so as not to degrade the breakdown voltage of the MOSFET cells. A guard ring edge termination structure [9] was selected for this accumulation-mode MOSFET because of its compatibility with the MOSFET structure. Normally guard rings are placed at the surface of the device, but this approach proved unsuccessful with the accumulation-mode MOSFET. Instead the guard ring had to be buried below the wafer surface at approximately the same depth as the P^+ layer (Figure 6).

Guard Ring Design Parameters

The important design parameters (Figure 6) for the guard ring are: T_{DEPTH}, T_T, $Q_{G.R.}$, and Width. All of these parameters were investigated using MEDICI simulations. The effect of guard ring depth T_{DEPTH} and thickness T_T is shown in Figure 7. The thickness of guard ring has little affect on the breakdown voltage, but the bottom of the guard ring must be deeper than that of the P^+ layer in order to be effective in achieving high breakdown voltage. Therefore with T_{CH} = 0.6 μm and T_{JFET} = 0.5 μm (Figure 1), a 0.6 μm thick guard ring needs to have a depth of at least 0.6 μm, as shown in Figure 7. The charge density of the guard ring $Q_{G.R.}$ is very important in achieving maximum breakdown voltage (Figure 8). The optimum charge density is 2-3 x 10^{13} cm^{-2}. The width of the guard ring needs to be at least 25 μm so as not to degrade breakdown voltage. At exterior corners of the MOSFET the guard ring may need to be even wider.

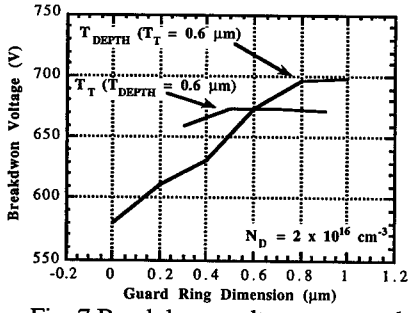

Fig. 7 Breakdown voltage vs. guard ring dimensions T_{DEPTH} and T_T.

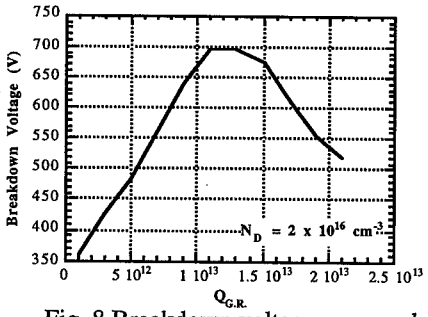

Fig. 8 Breakdown voltage vs. guard ring charge density $Q_{G.R.}$.

Conclusions

MEDICI device simulations were used to optimize the design of an accumulation-mode SiC MOSFET with a lateral channel and a vertical drift region. The optimum design value for L_{JFET} was 2 μm which yielded the best compromise between gate oxide field, breakdown voltage, and on-resistance. $L_{JFET} \approx 2$ μm also maximized the power device figure of merit V_B^2/R_{ON} for drift layers doped between 1-2 x 10^{16} cm^{-3}. For the edge termination to be effective, it must be buried in the SiC slightly deeper than the P^+ buried layer.

Acknowledgements

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Progress Towards a Manufacturable SiC Mixed Analog-Digital Integrated Circuit Technology[+]

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Keywords: Chopper Stabilized, Gain, MOSFET, Operational Amplifier, Yield

Abstract

A silicon carbide (SiC) operational amplifier has been successfully demonstrated. Using n channel depletion mode MOSFETs, these devices have shown open loop gains higher than 45 dB, a unity gain bandwidth of 2.5 MHz, and a dynamic range of 84 dB. Close control of the doping and thickness of the deposited epitaxial layers and the use of analytical modeling to predict device properties have led to the successful fabrication of this SiC device. With a functional yield of 25%, this work indicates the feasibility of large area, complex SiC device manufacturing.

Introduction

The development of Analog-Digital SiC integrated circuits (IC) for high temperature control and sensor applications has focused on the use of n channel depletion mode MOSFETs. The reasons for the use of depletion mode devices are: 1) the inability to control the characteristics of n channel inversion mode MOSFETs caused by unresolved MOS interface problems, and 2) extremely short time dependent dielectric breakdown (TDDB) of the gate oxides with positive gate bias [1-3].

Depletion mode devices do not possess these problems since: 1) accumulation to depletion MOS interface characteristics using n type SiC are reproducible; 2) channel electrons flow below the surface resulting in higher mobilities {80-100 cm^2/V-sec for 6H and 50 for 4H} with the "correct" temperature dependence; and 3) the TDDB with negative gate bias is extremely long even at elevated temperatures [1-3]. However, a disadvantage is the "tight" requirements placed on the doping and thickness of the SiC epitaxial layers required to maintain a narrow "turn-off" threshold voltage window so as to result in good circuit performance and yield with margin for low backgate bias voltages and prevention of minority carrier inversion.

SiC MOSFET Modeling and Testing

A theoretical model was developed for predicting the MOSFET threshold voltages, V_{th}, this being the pinch-off voltage for the buried conducting channel. The backgate

[+]supported by Wright Labs - Turbine Engine Division Contract F33615-94-C-2417 Contract Monitor - Stephen J. Przybylko

bias voltage is determined by the doping of the underlying epilayer. A sensitivity analysis was performed to find the optimal starting specifications for the SiC substrates to ensure a MOSFET threshold of between –6 V to –2 V. The substrates and epilayers were then fabricated by Cree Research.

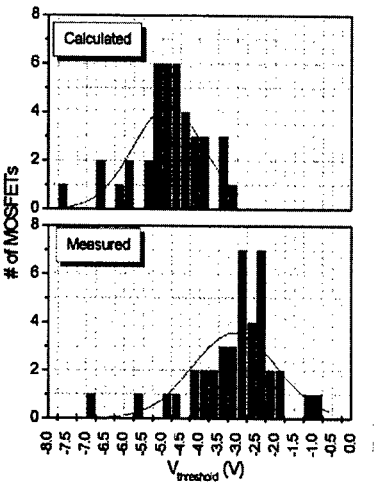

Figure 1. The calculated and measured threshold voltages from one lot of SiC MOSFETs. The epi layer thickness and doping concentrations were extracted from C(V) analysis and used as inputs in the modeling equations. Note the shift of almost +2V from the predicted threshold voltages and the measured values.

MOS C(V) profile analysis was performed on the as-received SiC substrates. These parameters were then inserted back into the model to calculate the predicted V_{th} of MOSFETs located at various positions across the substrates. Device MOSFET threshold voltages were measured and show a shift of +1 to +2 V from the theoretical predictions as can be seen from the two histograms in Figure 1. Important to note is that 88% all of the measured threshold voltages are found to be in the –6V to –2V range as needed for optimized circuit performance, and the threshold voltages have been reproduced from lot to lot.

Chopper Stabilized Operational Amplifier

Employing chopper stabilization in the amplifier decreases the effective offset drift and flicker noise by modulation to the chopped rate, which is outside the signal bandwidth.

A chopper stabilized operational amplifier circuit (opamp) was designed which incorporates both analog and digital circuitry. The circuit was designed using depletion mode NMOS transistors, n-epitaxial resistors, and poly to n-epi capacitors. A block diagram of the circuit is shown in Figure 2.

The ring oscillator and divide-by-two counter, which generate the clocks to operate the chopping switches, were implemented using buffered FET logic (BFL). BFL circuits provide the level shifting necessary for cascading static depletion mode logic. A silicon carbide BFL inverter is shown in Figure 3. The threshold voltage for the input to the inverter is negative with respect to ground. The output of the simple first stage depletion mode inverter is between ground and VDD. In order for the inverter to drive another logic gate, it requires a level shifting second stage. A source follower biased with current source and a voltage dropping resistor form the level shifting second stage.

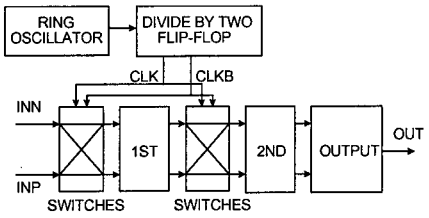

Figure 2. Chopper stabilized opamp diagram.

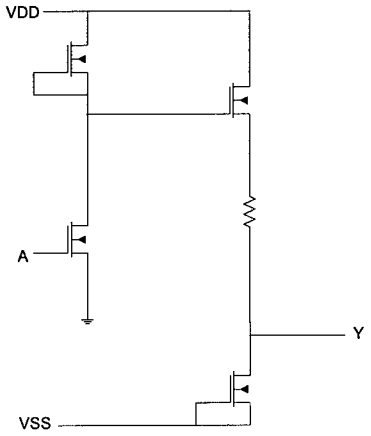

Figure 3. Silicon carbide BFL inverter.

dynamic range of approximately 84dB.

The opamp circuit is shown in Figure 4. The circuit has two stages, each with a gain of approximately 10, and an output buffer stage. Chopping switches surrounding the first stage modulate the offset voltage of the input pair to the chopping clock frequency. The offset of the second stage differential pair is reduced by the first stage gain when referred to the amplifier input.

The circuit was fabricated in an NMOS depletion mode technology, and a photograph of the integrated circuit is shown in Figure 5. The circuit contains 109 transistors and 17 resistors. The chip dimensions are 2600μm x 3300μm, and the circuit had a functional yield of 25%. The minimum channel length is 5μm.

The open loop gain, which is a measure of the ultimate accuracy of the amplifier, was greater than 45dB (see Table 1). Open loop gain of this magnitude provides accuracy of better than one percent. The gain-bandwidth product is a measure of the settling behavior of the amplifier. A unity gain bandwidth of 2.5MHz was measured, which allows the amplifier to be used with signal bandwidths in the hundreds of kilohertz and suitable for many sensor applications. The noise was measured to be 63μV in a 100KHz bandwidth allowing a

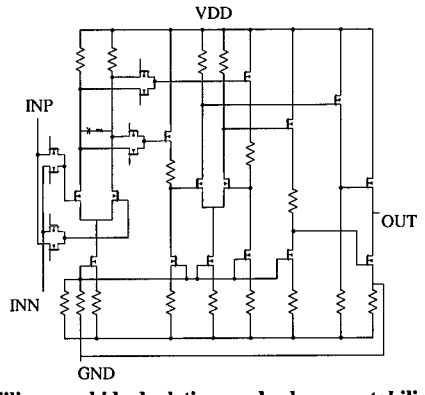

Figure 4. Silicon carbide depletion mode chopper stabilized opamp.

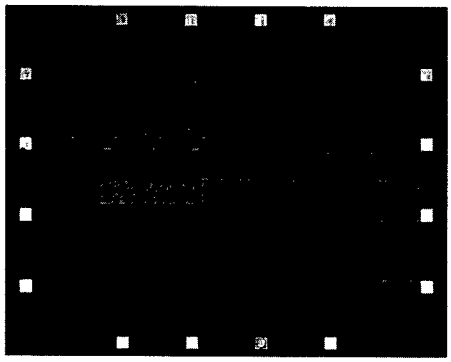

Figure 5. Die photograph of the chopper stabilized silicon carbide opamp.

SiC Op-Amp Characterization Summary and Future Research

Previous studies have shown that the MOS TDDB MTF is more than 50 years at 350°C with negative gate bias [1]. This study adds the factor that predictable and reproducible MOSFET characteristics are possible and in turn complex SiC MOSFET ICs can be leaves one remaining barrier: drift caused by "slow" electron trapping which has also been a problem with other depletion mode FETs (e.g. JFETs) [1]. This is thought to be produced by contamination of the n channel layer; this cause is being actively investigated using various analytical material techniques such as SIMS analysis and MOS C(V) characteristics. Hopefully this last barrier will be overcome soon.

Table 1. Important opamp properties.

Dimensions	2600 μm x 3300 μm
Functional yield	25%
Open loop gain	>45 dB
Unity gain bandwidth	2.5 MHz
Dynamic range	84 dB

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Rugged Power MOSFETs in 6H-SiC with Blocking Capability up to 1800V

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Keywords: Avalanche Breakdown, Power MOSFETs, Switching Characteristics

Abstract

This paper presents the static and dynamic characteristics of 1800V 6H-SiC vertical power MOSFETs. These devices exhibit an on-resistance of 46mΩcm^2 at room temperature and a steady state current rating of 0.4A at a power dissipation of 160W/cm^2. The forward blocking mode is characterized by a stable avalanche breakdown with a current rating of 20mA/cm^2. This robust and stable avalanche breakdown could be further improved to a current rating of 2A/cm^2 by optimizing the doping profiles. The dynamic behavior of the 1800V MOSFETs proves to be controllable in all switching states and is also stable at higher temperatures. Particularly the devices withstand a short circuit for 85µs with a maximum overload current of 2.7A at 300V DC supply voltage.

Introduction

Silicon carbide has been projected to exhibit a significantly better performance for high voltage switching devices than silicon. For vertical power **M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistors (MOSFETs) this potential has been successfully exploited in the past: In recent years devices with blocking voltages well above 1kV were realized in conjunction with a specific on-resistance distinctly below the values achievable with silicon /1,2,3,4/. Many of these MOSFETs, however, suffer from two deficiencies: Firstly they are susceptible to destructive failure at the maximum blocking voltage even at nearly no power dissipation. Secondly in most cases the active area of the devices is quite small and consequently the absolute current rating is limited. The largest SiC MOSFET reported up to now, is to our knowledge a 450V UMOSFET with an active area of about 1mm^2 /5/. Robust blocking performance and high current rating, however, are basic requirements for power MOSFETs appropriate for commercial switching applications.

Device Concept and Fabrication

The cross section of one cell of our MOSFET is sketched in Fig.1. The cell has a square layout in order to achieve a higher channel length per active area compared to the stripe geometry used in reference /3/. The cell structure of Fig.1 is similar to the well known double-diffused MOSFET cell of silicon power MOSFETs. This structure, however, is formed by three separate ion implantation processes because of the negligible impurity diffusion in SiC and consequently this MOSFET is called TI^{2}MOSFET (**T**riple **I**on-**I**mplanted MOSFET). The n$^+$-source as well as the p-well are heavily doped box-profiles. The p-base

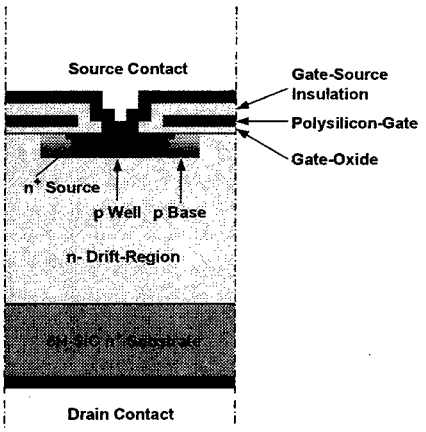

Fig.1 Schematic cross section of the TI^{2}MOSFET square cell.

determining the channel length is doped with a retrograde profile which has a low surface concentration in the region of the inversion channel. For achieving the full blocking capability of the MOSFET the active area is laterally terminated by a so called planar junction termination extension /6,7/.

As substrate material the 6H polytype of SiC is selected despite of its relatively low bulk mobility parallel to the c-axis. This is done because we verified a drastically higher inversion layer mobility for this polytype compared to the 4H polytype. A detailed analysis of the inversion layer mobility for different SiC polytypes /8/ revealed furthermore that the 15R polytype would be the best choice for SiC power MOSFETs. However this polytype is not yet available on commercial scale.

The fabrication of the TI^{2}MOSFETs started with the growth of an n-type epilayer on the 6H-SiC substrates (Cree Res. Inc. Durham, N.C.) by a low pressure chemical vapor deposition process /9/. The thickness and doping level of the epitaxial layers was adjusted to the intended blocking capability. Thereafter the three ion implantation steps were completed. Firstly the p-wells were created by aluminum implantation (box profile with peak concentration of $2x10^{18}cm^{-3}$). Secondly the n^+ source was formed by a high dose implantation of nitrogen and finally the p-base was generated by a second 400nm deep aluminum implantation with a surface concentration of $7x10^{16}cm^{-3}$ and a peak concentration of $1x10^{18}cm^{-3}$ in the depth. These implantations were annealed at a temperature of about 1700°C. The gate oxide was grown by a combination of dry and wet thermal oxidation at 1100°C. Subsequently the polysilicon gate was deposited and doped with phosphorous. The polysilicon grid was insulated from the source metallization by a 200nm thick silicon oxide layer. After annealing the source and drain contacts at around 1000°C the source and drain metallization as well as the gate contact were finally formed by a 2µm thick aluminum layer ensuring safe operation up to several ampere.

Experimental Results and Discussion

Static Characteristics

Fig. 2 shows the static low and high voltage I-V family of a 1800V TI^{2}MOSFET monitored by a curve tracer (Tektronix 370A). The device is normally off and has a threshold voltage of 4.8V. In the on-state the device can be driven up to 1A. At V_{GS}=10V (E_{ox}=2.8MV/cm) the specific on-resistance at low current levels is 46mΩcm^2. A detailed analysis of the corresponding transfer

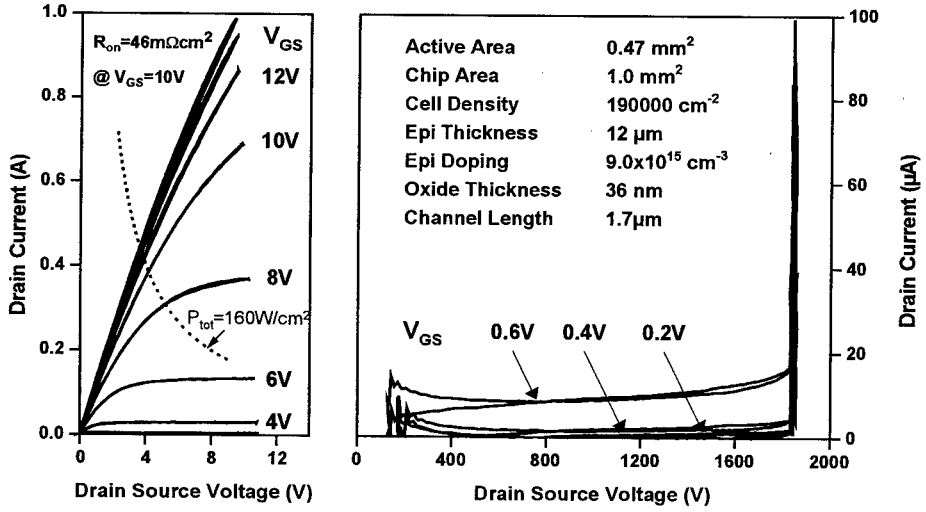

Fig.2 Low and high voltage I-V family of a 1800V 6H-SiC TI^{2}MOSFET at room temperature. For the measurement of the forward blocking characteristic the device was immersed in Fluorinert™ oil.

characteristic according to the method described in /10/ revealed that 36% of this on-resistance stem from the channel resistance. Furthermore, this analysis revealed a low field mobility of about 15cm^2/Vs for the MOSFET channel. This value is in good agreement with the data reported in /11/ where a strong decrease of the channel mobility with increasing base doping level was found. Consequently, higher inversion layer mobilities could be realized only by a lower base doping level which would adversely affect the blocking capability of the device.

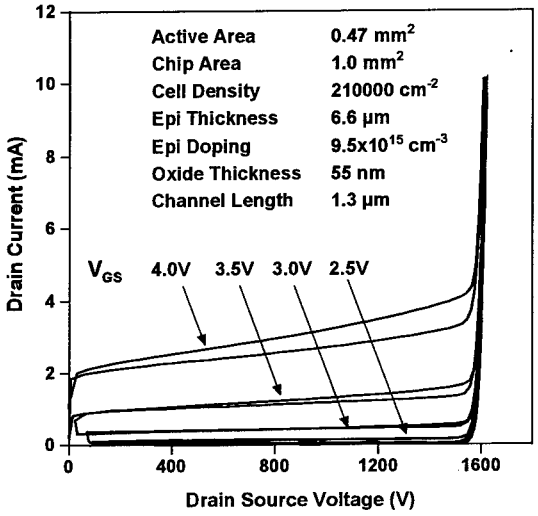

Fig.3 High voltage I-V family of a 1600V 6H-SiC TI^{2}MOSFET at room temperature immersed in Fluorinert^{TM} oil.

Allowing a DC power density of 160W/cm^2, a value typical for large area Si-devices and standard packaging technique, the TI^{2}MOSFET of Fig.2 can be driven continuously with 0.4A at V_{GS}=10V. In the forward blocking mode the device withstands voltages up to 1800V and is characterized by a stable avalanche breakdown. This avalanche breakdown can be powered up to 0.1mA corresponding to 20mA/cm^2.

The ruggedness of this avalanche breakdown could be further enhanced by tuning the technology and optimizing the doping profiles. This is demonstrated in Fig. 3 for a 1600V TI^{2}MOSFET which exhibits a current rating of 10mA in the avalanche mode corresponding to a current density of 2A/cm^2 referred to the active area and a power density of 1.6kW/cm^2 referred to the total chip area. In this avalanche mode no latch up phenomena are observed and the device exhibits a white luminescence emerging from the border of the device.

Dynamic Characteristics

The static current rating of 0.4A of the presented TI^{2}MOSFETs offers the chance to study their switching performance. In order to characterize the turn-on and the turn-off behavior as close as possible to typical inverter applications, e.g. motor-drives we used a chopper circuit which is described in detail in reference /4/.

The switching behavior of the TI^{2}MOSFETs will be characterized by a typical turn-off transient at room temperature with a series resistance (R_G) of 1kΩ in the gate drive circuit. Fig.4 shows the gate source voltage (V_{GS}), the drain source voltage (V_{DS}) as well as the drain current (I_D) as a function of time. The graph starts with the MOSFET operating in the linear on-state regime at V_{GS}=12V. At time t=0 the gate driver is set

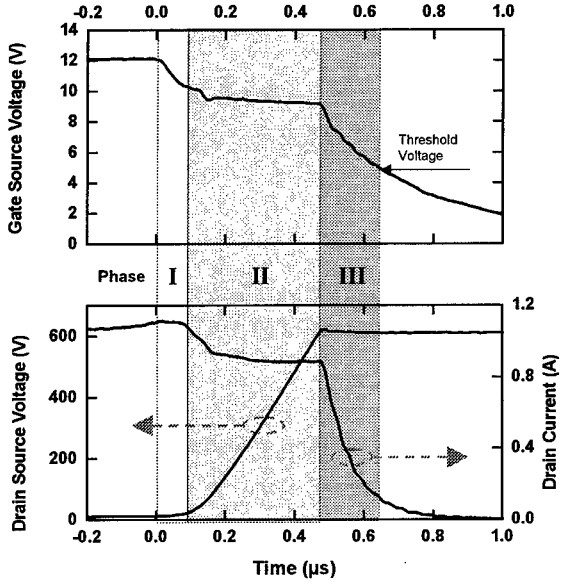

Fig.4 Turn-off period of a 1800V 6H-SiC TI^{2}MOSFET at a load voltage of 600V.

to zero. The subsequent turn-off transient can be divided in three distinct periods. In the first period I_D and V_{DS} remain constant while V_{GS} drops to the Miller plateau of V_{GS}=9.2V. In the second period V_{DS} starts to increase, driving the MOSFET into saturation, while V_{GS} remains clamped charging the Miller capacitance of about 5pF with a gate current $I_G=V_{GS}/R_G$=9.2mA. The unfamiliar drop of I_D by about 0.1A at the beginning of this period does not originate from the MOSFET but is caused by charging the parasitic capacitance (≈5pF) of the inductive load. This drop in drain current depends on the switching speed which is controlled by R_G. Finally in the third period V_{GS} drops exponentially and I_D follows until the threshold voltage is reached and the MOSFET is turned off. The overall turn-off delay for the 1A load current and 600V DC supply voltage is 650ns for R_G=1kΩ. The turn-off delay shortens to 250ns by reducing the gate resistance to 125Ω thus demonstrating that the switching behavior of the MOSFET is controllable. In addition, the switching transient proved to be stable up to temperatures of 125°C, an important feature for the commercial application of MOSFETs.
The short circuit strength of the TI^{2}MOSFETs has been tested with a DC supply voltage of 300V. In this test the MOSFET withstood short circuit for approximately 85µs. During this time the current through the inductive load of 4mH raised up to 2.7A and the supply voltage settled at 300V. The corresponding energy dissipated in the device is 36mWs.

Conclusions

The normally off 6H-SiC vertical power MOSFETs presented in this paper exhibit in the conducting mode a current rating in the ampere regime and in the blocking mode a stable avalanche breakdown. The dynamic behavior of these devices exhibits a turn-on and turn-off behavior typical for power MOSFETs which is controllable in all switching states. In addition the MOSFETs are robust against short circuit, short time overloading and show no latch up phenomena. Thus, the MOSFETs prove to be capable of handling high voltages and high currents simultaneously, under static as well as dynamic conditions. Due to their high energy absorption during avalanche breakdown and their short circuit strength these SiC power MOSFETs deserve to be called rugged.

Acknowledgment

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Influence of Post-Oxidation Annealing on Electrical Characteristics in 6H-SiC MOSFETs

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Keywords: Channel Mobility, Field Effect Transistors, Metal-Oxide-Semiconductor, Post-Oxidation Annealing, Threshold Voltage

Abstract

Enhancement-type *n*-channel metal-oxide-semiconductor field effect transistors (MOSFETs) have been fabricated on p-type 6H-SiC epitaxial films. The gate oxide in the MOSFETs was annealed in steam or dry hydrogen (H_2) up to 1000 °C to investigate the influence of post-oxidation annealing on the electrical characteristics of the MOSFETs. The channel mobility is found to increase by both annealing methods. The optimum annealing temperature is obtained to be 800 °C for steam annealing and 700 °C for annealing in H_2.

1. Introduction

Silicon Carbide (SiC) is considered a promising candidate for high-power and high-frequency devices. Besides, since SiC has strong radiation resistance[1], it is also expected for electronic devices used in radiation environments such as space and nuclear reactors. For the application of SiC to devices with metal-oxide-semiconductor (MOS) structures, it is important to optimize their fabrication processes. Especially, the improvement of the interface between gate oxide and SiC is required for raising channel mobility in SiC MOS field effect transistors (FETs). Interface traps in SiC MOS structures have been studied using capacitance-voltage (*C-V*) measurements by many researchers[2,3]. Lipkin *et al.*[3] reported that *C-V* characteristics of 6H-SiC MOS structures are improved by post-oxidation annealing at 950°C in a wet oxidizing ambient. Fukuda *et al.*[4] reported that defects in the interface between SiO_2 and n-type 4H-SiC are reduced by annealing in hydrogen (H_2) at 1000 °C. However, the influence of post-oxidation annealing on channel mobility and threshold voltage in SiC MOS FETs has not yet been fully understood.

In this study, we have performed steam and H_2 annealing for gate oxide in 6H-SiC MOSFETs, and demonstrated that the electrical characteristics in SiC MOSFETs are improved by post-oxidation annealing in steam and by annealing in H_2.

2. Experiments

The MOSFETs used in this study were fabricated on p-type 6H-SiC epitaxial films with a thickness of 4 μm grown on 6H-SiC substrates (3.5° off, Si-face). The net acceptor concentration of the epitaxial films ranged from $5x10^{15}$ to $1x10^{16}$ /cm^3. The gate length x width of the MOSFETs was 10 x 200 μm^2. The source and drain were formed by phosphorus (P) or nitrogen (N) ion implantation at 800 °C and subsequent annealing at 1500 °C for 20 min in Ar atmosphere. The gate oxide was fabricated at 1100 °C for 1 hour in steam (pyrogenic condition; H_2:O_2 =1:1). Steam-annealing for the gate oxide was performed at 700 °C to 1000 °C for 30 min in the same atmosphere as the oxidation process. The samples were rapidly cooled to room temperature (RT) after the annealing. As for H_2 annealing, the samples were annealed at 400 °C to 900 °C for 30min in dry H_2 at a pressure of 20 Torr. The thickness of the gate oxide after annealing was determined by *C-V*

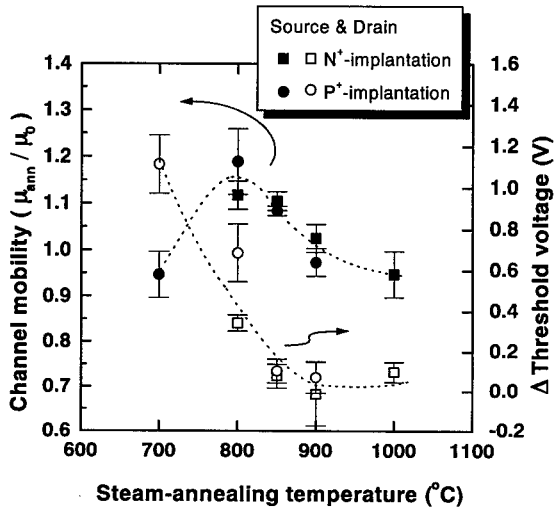

Fig. 1 Dependence of channel mobility (closed symbols) and threshold voltage (open symbols) on temperature of steam-annealing for 6H-SiC MOSFETs. Squares and circles indicate the results for the MOSFETs in which source and drain were formed using N^+- and P^+-implantations, respectively. The left-hand ordinate represents the channel mobilities in the MOSFETs after the steam annealing (μ_{ann}) normalized by that in the sample without annealing (μ_0), i.e., μ_{ann}/μ_0. The shift of V_T upon the steam annealing (ΔV_T) is also plotted.

measurements. After the post-oxidation annealing, aluminum electrodes were formed using lift-off technique. The electrical characteristics of the MOSFETs were measured under the dark condition at RT.

3. Results and Discussion

Figure 1 shows the dependence of channel mobility (closed symbols) and threshold voltage (open symbols) on steam-annealing temperature for 6H-SiC MOSFETs. Squares and circles indicate the results for the MOSFETs of which source and drain were formed by using N^+- and P^+-implantations, respectively. The channel mobility was derived from drain current (I_D) -drain voltage (V_D) curves in the linear region. The right-hand ordinate in the figure represents the channel mobilities in the MOSFETs fabricated with steam annealing (μ_{ann}) normalized by that in the MOSFETs without annealing (μ_0), μ_{ann}/μ_0. The threshold voltage (V_T) was determined as the value at the intersection between the gate voltage (V_G) axis and the line extrapolated from the curve of the square root of I_D versus V_G in the saturation region. The shift of V_T upon steam annealing (ΔV_T) is plotted in the figure. The highest mobility is obtained for the samples annealed at 800 °C. The channel mobility in these MOSFETs is 52.2 cm^2/Vs, which is about 1.2 times as high as that in the sample without annealing. No significant change in V_T is observed in an annealing temperature range between 900 and 1000 °C, and V_T increases with decreasing annealing temperature below 900 °C.

I_D-V_G curves in the subthreshold region for the MOSFETs fabricated with steam annealing were measured. The results are shown in Fig. 2. The source and drain of these MOSFETs were formed by using P^+-implantation. The voltage marked with a cross on each curve corresponds to V_T. A potential of 10 V was applied between the source and drain during the measurements. The subthreshold curve shifts toward the positive gate voltage side without any change in the inclination of the curve by the steam-annealing at 800 °C. On the other hand, the inclination of the subthreshold curve is changed by the steam-annealing at 700 °C. According to McWholtor and Winokur[5], the subthreshold current curves are affected by the generation or reduction of oxide-trapped charges and interface traps. The generation of oxide-trapped charges simply translates an entire subthreshold curve, because the contribution of oxide-trapped charges to the shift of V_T is independent of gate bias. Since interface traps interact with carriers in semiconductor, the inclination of subthreshold curves is changed by the generation of interface traps. For 6H-SiC, interface traps located near the middle region of the band gap behave just like oxide-trapped charges because they release charges with extremely long time constant[6]. Taking account of the fact that a large negative flat band shift was observed for p-type 6H-SiC MOS capacitors[2], the obtained result suggests strongly that positively charged oxide-trapped charges and/or interface traps located near the middle gap region decrease by steam-annealing at 800 °C. On the other hand, interface traps located near the band

edge region are probably generated by the steam-annealing at 700 °C. For the MOSFETs steam-annealed below 600 °C, no significant difference in subthreshold curves with that for no-annealed MOSFETs was observed (the result is not shown in this paper).

It was reported that carbon compounds, which probably degrade channel mobility, reside in oxide near the interface of SiO_2/SiC after oxidation[7]. The increase of channel mobility due to the steam-annealing can be interpreted by the speculation that the number of residual carbon compounds decreases by the reactions between carbon and oxygen-related species during the annealing. The reaction rate probably increases with increasing annealing temperature. The steam annealing at high temperatures above 800 °C could give rise to further oxidation of SiC, which leads to the production of additional carbon compounds. The formation of carbon compounds is enhanced when steam annealing temperature is raised. It is most likely that competition between the reduction and formation of carbon compounds during steam annealing causes the annealing temperature dependence of channel mobility shown in Fig. 1.

Figure 3 shows the dependence of μ_{ann}/μ_0 (circles) and ΔV_T (squares) on temperature of H_2-annealing for 6H-SiC MOSFETs of which source and drain were formed by using P^+-implantation. By the H_2-annealing above 700 °C, the channel mobility increases in comparison with that in the sample fabricated without annealing. The highest mobility is obtained for the sample annealed at 700 °C. The channel mobility in this MOSFET is 51.8 cm^2/Vs, which is about 1.2 times as high as that in the one without annealing. After annealing at 400 °C, no significant increase of mobility is observed. No significant difference in V_T is observed between 400 °C- and no-annealing, and V_T shifts toward the negative voltage side with increasing

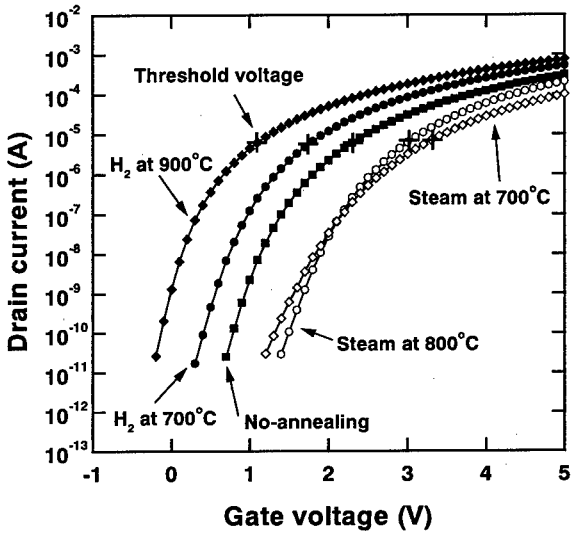

Fig. 2 Subthreshold current curves for the steam- and H_2-annealed MOSFETs. The voltage marked with a cross on each curve corresponds to V_T. A potential of 10 V was applied between the source and drain. The result for no-annealed MOSFET is also shown for comparison.

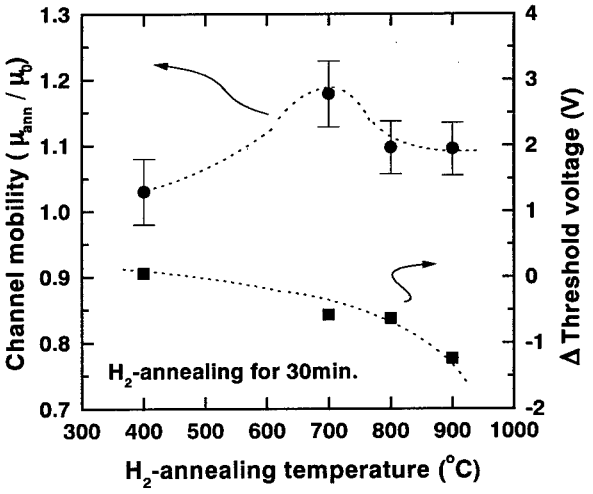

Fig. 3 Dependence of μ_{ann}/μ_0 (circles) and ΔV_T (squares) on temperature of H_2-annealing for 6H-SiC MOSFETs.

annealing temperature. The subthreshold curve shifts toward the negative gate voltage side without any change in the inclination of the curve with increasing H_2-annealing temperature, as shown in Fig. 2. Thus, the shift of V_T due to H_2-annealing indicates an increase of positively charged oxide-trapped charges and/or interface traps located near the middle region of the band gap. It is unlikely that such oxide-trapped charges and/or interface traps generated by H_2-annealing reduce channel mobility. Taking account of the fact that the shift of V_T by H_2-annealing differs from that by steam-annealing, it is most probable that mechanisms of the post-oxidation annealing effects on the electrical characteristics of MOSFETs are different between H_2- and steam-annealings. To clarify this point, further investigations are necessary.

4. Conclusions

Enhancement-type n-channel MOSFETs with gate oxide annealed in steam or dry H_2 up to 1000 °C were fabricated on 6H-SiC to investigate the influence of the post-oxidation annealing on channel mobility and threshold voltage. The channel mobility is found to be improved by steam-annealing as well as H_2-annealing after oxidation. The threshold voltage is also affected by such post-oxidation annealings. As for steam-annealing, the MOSFET annealed at 800 °C shows the highest channel mobility 52.2 cm^2/Vs, which is approximately 1.2 times as high as that in no-annealed MOSFET. As for H_2-annealing, the channel mobility in MOSFETs increases by the annealing above 700 °C in comparison with that in no-annealed MOSFET, and the highest value of 51.8 cm^2/Vs is obtained in the MOSFET annealed at 700 °C.

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Effect of Boron Implantation on 6H-SiC N-MOSFET Interface Properties

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Keywords: Carrier Mobility, Dielectrics, MOSFET, Switching

Abstract: MOS gated devices performances are mainly dependent on the dielectric/semiconductor interface characteristics. We have evaluated the different performances of 6H-SiC N-MOSFET structure for testing the feasibility of power VDMOS. We have observed the influence of growing the gate oxide on an implanted region, resulting in a decrease of the effective channel mobility. This effect is maintained at high temperature. We have also checked the switching capability of the MOSFET. The difference in the on-state losses is also observed.

1. Introduction

MOS gated devices are currently the main elements used in Silicon microelectronic for circuit fabrication. These types of structure could be also very attractive for SiC. High temperature SiC CMOS and high voltage SiC VDMOS and IGBT are for example devices with an important potential of applications. The key point of this type of technology rely in the quality and reliability of the gate oxide, which have been shown to be lower for SiC than for Si [1-3]. SiC planar MOS-Gated Power devices and low signal MOSFET structures processing require to implement a P-well using implantation technique. Consequently, gate oxide interface properties can be modified when compared with optimised MOS structure on epitaxial P-layer. In this paper, we compare the electrical properties of MOSFET devices made on a P-type substrate with and without Boron implantation in order to evaluate the effective mobility degradation due to the boron implantation. We show that the inclusion of boron impurities at the interface, resulting of an implantation process to form the P-body of a DIMOS for example, have a negative impact on the channel mobility.

2. Devices fabrication

The starting material is a Lely modified 6H P-type 2e17 cm^{-3} Al doped substrate. A multiple Boron implantation was locally performed through a mask. The implantation parameters have been determined by means of simulation [4]: energies 20, 35, 60, 100 and 150 keV and doses 10^{13}, $1.5x10^{13}$, $2.25x10^{13}$, $3.2x10^{13}$ and $5x10^{13}$ cm^{-2}, were used, respectively. The total implanted dose corresponds to a chemical doping level of $3x10^{18}$ cm^{-3}. This last value and the P-substrate doping were chosen to be compatible with the P-well doping of power MOS devices. After Nitrogen implantation for source and drain formation, a RTA annealing was performed at 1500°C during 30 minutes. This annealing was shown not to be enough for complete Boron activation but sufficient for implantation defects removal (observed from RBS measurements) and for Nitrogen activation. Sublimation of Silicon from the surface is also mainly avoided at this temperature. The gate oxide was grown at 1100°C in wet ambient,

followed by an annealing in Ar at 1100°C and a wet reoxidation at 950°C. This process was previously optimised [5] with a study on MOS capacitors. The gate metal was deposited just after the oxidation step. The process was completed in order to obtain N-channel MOSFETs on Boron implanted (BI) and non-implanted (BNI) regions using nickel as metal for contacts. The width of the MOSFET is fixed (150μm) and the channel length is varied from 5 to 24μm.

3. Experimental results

Electrical static measurements have been performed in order to extract MOSFET's parameters. In Fig. 1 we can appreciate the I-V characteristics of an 8/150μm MOSFET for different gate voltages. Due to the thickness of the gate oxide, we have observed that gate voltages higher than 16V are not recommended in order to maintain the oxide reliability. A small rectifying effect is observed at low voltage due to the non-ideal contact.

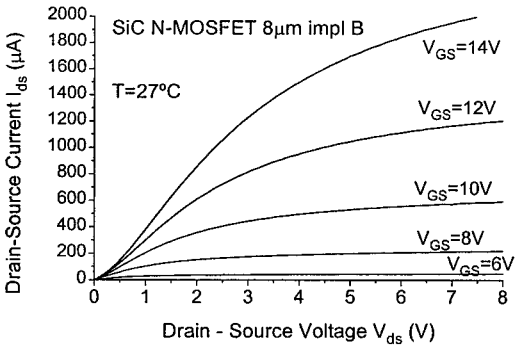


Fig. 1: Experimental output characteristics Boron Implanted (BI) MOSFET with channel length L=8μm

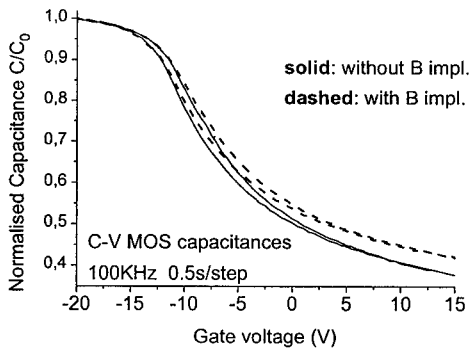
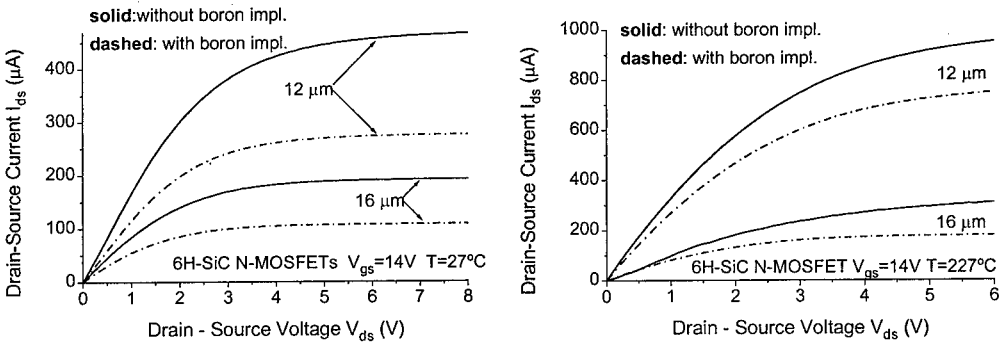


Fig.2: Normalised C-V characteristics for MOS capacitance build on Boron implanted (dashed) and non-implanted (solid) layer.

There is a difference of 0.4V to 0.6V between measured threshold voltages of BI and BNI MOSFETs. This difference can be due to a different doping level at the surface due to the boron activation and to different fixed charge quantity at the interface. In order to evaluate the interface quality, MOS capacitors made on BI and BNI regions have also been fabricated on the same wafer. C-V measurements made on these MOS capacitors are shown in Fig. 2. We can see that there is a small hysteresis and no bumps or ledges usually observed in MOS capacitors on P-type SiC. This figure shows that the difference in threshold voltage can be attributed to a slightly lower flat band shift and to the higher active doping of the BI MOS interface. We obtain a factor of 1.4 between the surface doping extracted from these measurements. It demonstrates that the implanted Boron has been partially activated. The extracted gate oxide thickness is 420Å. The difference in the slope of the C-V curves also indicates a larger quantity of interface traps in the BI MOS capacitances.

The I-V output characteristics show (Fig. 3a) that the BNI MOSFET has a higher output current than the BI MOSFET for a given gate voltage. This difference is not exclusively due to the different threshold voltages but also to the lower carrier mobility in the channel of the BI structure. For the 12μm channel length MOSFET, extracted carrier mobilities (from transconductance measurements) are 12 and 17 cm^2/Vs for BI and BNI MOSFETs,

respectively. A maximum carrier mobility of 20 cm^2/Vs is obtained for the 8μm MOSFET. These low mobility values are partially due to the high doping of the semiconductor surface. The effective channel mobility has been shown to decrease when the doping at the interface is increased as indicated in [6]. The difference in output characteristics between BNI and BI MOSFETs is still existing at higher working temperature as can be seen in figure 3(b).



(a) (b)

Fig. 3: Output current of Boron implanted (dot) and non implanted (line) MOSFET with channel length L=12μm and L=16μm. Gate voltage is 14V. (a) at 27°C and (b) at 227°C

The current levels increase at higher temperature (Fig. 4) due to the thermal activation at the highly disordered interface. The extracted effective carrier mobility in the channel increases by a factor of 1.75 between 27°C and 270°C at V_{gs}=15V for the boron implanted 16μm channel length MOSFET. A similar factor (between 1.7 and 2.1) is also observed for the MOSFETs with other channel lengths.

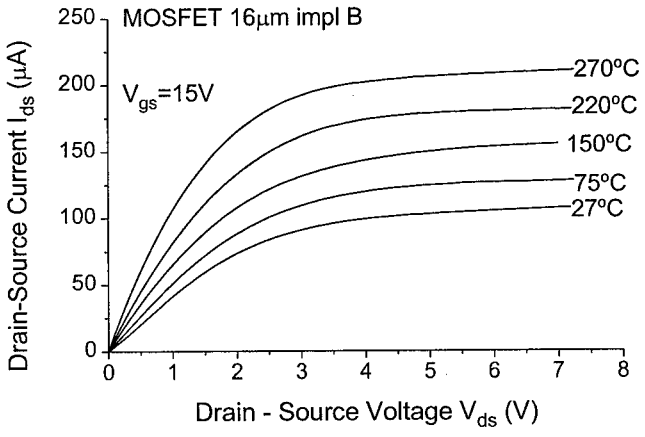


Fig. 4: Experimental I-V curve at Vgs=15V of Boron Implanted MOSFET with channel length L=16μm for temperatures from 27°C to 270°C.

We performed dynamic measurements on resistive load in order to confirm the switching capability of the MOSFET (Fig. 5). The supply voltage is 10V and the gate voltage is switched between 0V and 15V. Both devices exhibit a standard switching waveform with a perfect gate signal indicating no leakage in the gate during switching. We can appreciate the lower on-state losses obtained with the BNI device (Fig. 5(a)) due to the lower on-resistance. It reflects the higher effective mobility in the BNI device even in dynamic mode. In our experiments, switching times are limited by the circuit parasitic capacitors. However, we can conclude that power MOS switches can be fabricated starting from this MOS technology.

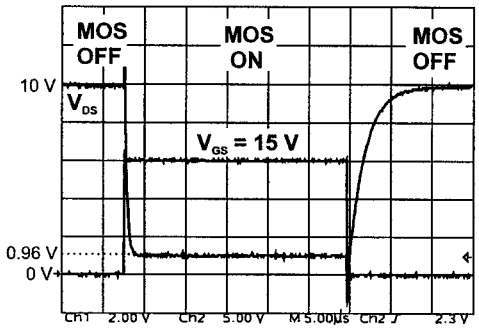


Fig. 5(a): Gate and Drain voltage of BNI MOSFET (12µm) during switching on a resistive load. The resulting on-state voltage is 0.96V and the MOSFET is in the linear mode.

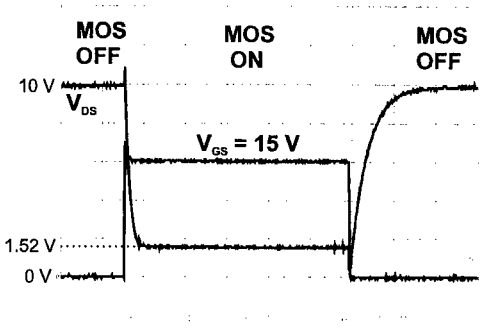


Fig. 5(b): Gate and Drain voltage of BI MOSFET (12µm) during switching on a resistive load. The resulting on-state voltage is 1.52V and the MOSFET is in the linear mode.

4. Conclusion

MOSFET devices in SiC usually exhibit low effective carrier mobility in the channel in comparison with Si. Many physical processes are involved to explain this phenomena. We have shown that one of these processes is related to the implantation process used to form the P-well of MOS devices. Even using a low implantation dose and a high temperature annealing to remove the defects, there is a decrease of the carriers mobility resulting in a lower output current. This lower output current is also observed with switching measurements.

Acknowledgement

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Investigation of Lateral RESURF, 6H-SiC MOSFETs

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Keywords: Interface Trap, LDMOS, Mobility, Power MOSFETs, RESURF

Abstract: We report on theoretical and experimental investigations of 600 V, lateral RESURF, 6H-SiC MOSFETs. The 2 dimensional device simulations show that the breakdown voltage of this class of devices is limited by the peak electric field in the oxide, which should be kept below 3 MV/cm for long-term reliability. The devices made on 6H-SiC substrates show 600 V breakdown, which was limited by the breakdown of the gate oxide. In order to reduce the electric field in the gate oxide, we show that it is necessary to reduce the doping of the lateral drift layer. This results in excessive specific on-resistance, which is dominated by the resistance of the drift layer. The inversion layer electron mobility of 50-60 $cm^2/V{\cdot}s$ was obtained on experimental devices. Large area devices (560 μm x 1700 μm) had a specific on-resistance of 57 $mohm{\cdot}cm^2$.

Introduction: Both vertical and lateral power MOSFETs in 6H- and 4H-SiC have been reported [1-6]. The overall goal is to develop a MOS process technology in SiC having a gate insulator with a high quality SiC/SiO_2 interface, high electron inversion layer mobility, low interface trap density, appropriate lateral drift layer, good contacts, and high conductivity of the source and drain regions. These requirements are often conflicting. For example, the high temperature required for activation of various implants can lead to surface roughness resulting in poor inversion layer electron mobility. In our previous work [7], the source/drain and drift layer implants were activated at 1200°C which caused insufficient activation, very high sheet resistance of the source/drain regions and poor mobility in the drift region due to the residual implant damage. In this work, we have activated the implants at 1400°C resulting in much improved activation, lower sheet resistances, theoretical mobility in the drift layer while retaining the high inversion layer electron mobility of 50-60 $cm^2/V{\cdot}s$.

Device Structure: Two different SiC high voltage lateral MOSFET designs are shown in Figs 1-2.

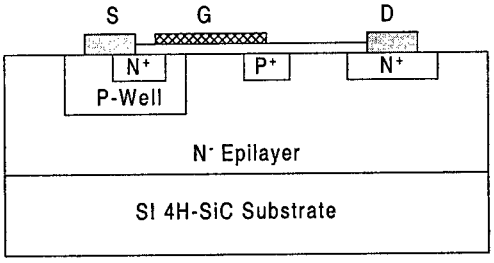

Fig. 1 The conventional LDMOS structure as reported by Purdue University [6].

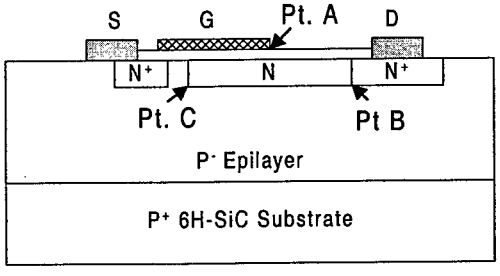

Fig. 2 The LDMOS structure used in this work.

The drawings in Figs 1-2 are oversimplified and do not show field oxide etc. The structure in Fig. 1 was first reported by Purdue Univ.[6]. This structure employs a gate oxide grown on the surface of

a p-well which has to be implanted. A major drawback of this scheme is that it requires >1400°C anneal to activate the boron or aluminum implants. Such a high temperature results in surface roughness leading to poor inversion layer electron mobility. Currently, techniques of reducing the so-called "step-bunching" during implant-activation are being investigated. The second structure avoids the p-well entirely and utilizes the p-epitaxial layer with good surface quality. The implanted n-drift layer can be fully activated at 1400°C in 6H-SiC.

Two Dimensional Device Simulations: The structure shown in Fig. 2 was simulated using the 2D device simulator from Siborg Systems Inc. The x-component of the electric field in SiC, $E_x(SiC)$, along the line BC in Fig. 2 and the y-component of the electric field in SiO_2, $E_y(SiO_2)$, along the gate electrode/SiO_2 interface are shown in Fig. 3 with drain biased at 600 V. The doping of the 0.5 μm thick drift layer was $1x10^{17}$ cm^{-3} and the length was 15 μm. The p-type channel doping was 10^{16} cm^{-3}. Clearly, the field in the oxide peaked at the edge of the polysilicon gate electrode overlapping the n^- drift layer (point A in Fig. 2) and has exceeded 3 MV/cm for a drain voltage of only 600 V. This is a direct result of the fact that $E_y(SiO_2)$ is 2.5x (ratio of dielectric constants of SiC and SiO_2) of $E_y(SiC)$. It should be noted that this problem does not arise in silicon devices, as the maximum breakdown field in Si is 0.4 MV/cm, which limits the electric field in oxide to 1.2 MV/cm. In order to overcome this problem, the doping density in the drift layer can be selectively reduced under the gate electrode. In practice, this is costly because it causes the FET resistance to increase. We have done simulations by uniformly reducing the doping density in the drift layer. The results are shown in Fig. 4. As expected, $E_y(SiO_2)$ at point A reduces and $E_x(SiC)$ at point B increases with reductions in the drift layer doping at a constant drain bias of 600 V. For drift layer doping above 10^{17} cm^{-3}, the E_x (SiC) peaks at point C instead of point B as expected.

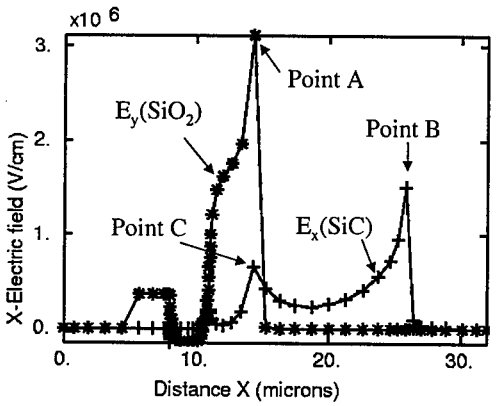

Fig. 3 2D device simulation results of the structure shown in Fig. 2. The drift layer was 15 μm long, 0.5 μm thick, and doped at $1x10^{17}$ cm^{-3}. The gate and source were grounded and the drain was biased at 600 V. The locations of points A, B and C are shown in Fig. 2.

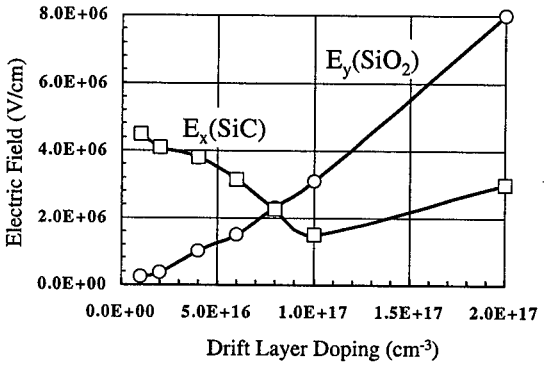

Fig. 4 The variation of $E_y(SiO_2)$ at point A and $E_x(SiC)$ at points B or C with drift layer doping. The reduction of the drift layer doping reduces $E_y(SiO_2)$ but increases $E_x(SiC)$ at point B. The drift layer doping of $1x10^{17}$ cm^{-3} seems to be optimal.

The reduction in the drift layer doping, of course, leads to increase in the specific on-resistance of the MOSFET as shown in Fig. 5. These results are calculated assuming parameters similar to those given in Table 1. The gate voltage was fixed at 10 V. From these simulation results, it is clear that the optimum doping for the drift layer which keeps the peak field in the oxide at or below 3 MV/cm is about $1x10^{17}$ cm^{-3}. Higher doping will cause the oxide to breakdown at point A. Lower doping will cause SiC to breakdown at point B. The total specific resistance for the optimal doping is 38 mohm·cm^2, 50% of which is in the drift layer and the remaining 50% is in the inversion layer.

Device Fabrication: We have implemented the structure shown in Fig. 2 on p^+ 6H-SiC substrates with 10 μm of p-epitaxial layer doped at $1x10^{16}$ cm^{-3}. The device parameters are listed in Table 1. The source, drain and the lateral drift regions were implanted with nitrogen to a depth of 0.5 μm and activated in argon at 1400°C for 30 minutes. The implanted dose in the drift region was $3.75x10^{12}$ cm^{-2} and resulted in a sheet resistance of 6180 ohm/sq. This corresponds to a bulk electron mobility of 270 $cm^2/V{\cdot}s$ along the a-axis, and demonstrates that the 1400°C anneal is sufficient for activation of N implants. At the same time, the temperature is low enough to avoid "step-bunching" on the SiC surface which can drastically reduce the inversion layer electron mobility. The 31 nm thick gate oxide was grown wet at 1100°C for 3 hours and then re-oxidized wet at 950°C for 90 min to obtain a low interface trap density [8]. A thick ~ 7 kÅ field oxide was formed during the same oxidation step by complete oxidation of an un-doped polysilicon layer. A 3.5 kÅ thick layer of polysilicon was deposited and doped with phosphorus at 900°C for the gate electrode. The ohmic contacts to the n^+ source and drain regions were formed by depositing 800Å of nickel annealed at 800°C for 150 s.

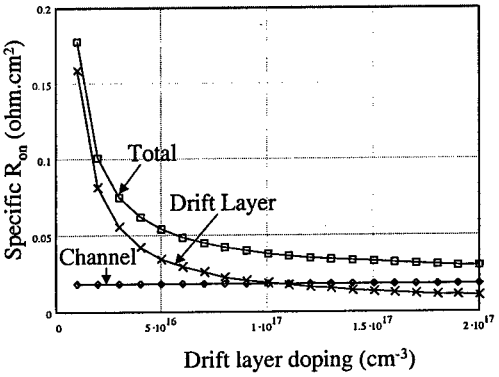

Fig. 5 The calculations of the channel and drift layer components of the specific on resistance for 6H-SiC LDMOS. The device parameters were similar to those shown in Table 1. The gate voltage was fixed at 10 V.

Table 1 Device parameters of the fabricated 6H-SiC LDMOSFET

P epilayer doping (cm^{-3}), thickness (μm)	$1x10^{16}$, 10
Drift layer implanted dose (cm^{-2})	$3.75x10^{12}$
Sheet resistance of the drift layer (ohm/sq)	6180
Sheet resistance of n^+ source/drain (ohm/sq)	695
Contact resistance to n^+ source/drain ($ohm{\cdot}cm^2$)	$1.05x10^{-5}$
Gate oxide thickness (Å)	310
Channel length (μm), drift layer length (μm)	3, 15
Inversion layer electron mobility ($cm^2/V{\cdot}s$)	50-60

Experimental Results: The enclosed RESURF MOSFETs were fabricated with two different drift region lengths (10 and 15 μm) and three different gate lengths (3, 5, and 10 μm). The I-V characteristics for the FET with 10 μm gate length and 15 μm drift region are shown in Fig. 6. This FET broke down at 650 V at point A in Fig. 2. The inversion layer electron mobility (extracted from the long gate length devices without the RESURF region) was 50-60 $cm^2/V{\cdot}s$. A large device with channel length of 3 μm, total periphery of 3 cm and drift length of 10 μm was measured (Fig 7). The measured on-resistance at a gate voltage of 10 V was 57 $mohm{\cdot}cm^2$ (compared to the calculated value of 48 $mohm{\cdot}cm^2$ shown in Fig. 5 corresponding to the drift layer doping of $7.5x10^{16}cm^{-3}$ in the fabricated devices). Of the total series resistance, the dominant source of resistance, 69%, was in the drift layer. ***The gate voltage of 10 V is very reasonable from the standpoint of long-term reliability of the gate oxide.*** The large area inter-digitated devices broke down at around 400-450 V.

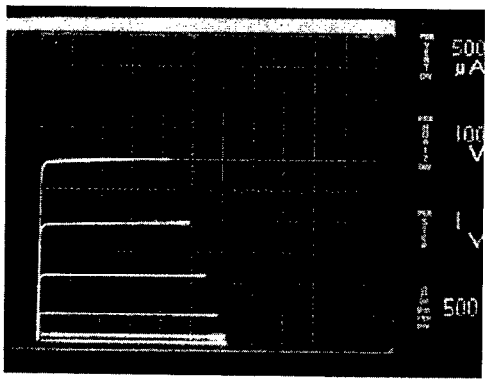

Fig. 6 The I-V characteristics of an enclosed LDMOS with L=10 μm, L_{drift}=15 μm. The gate voltage is from 0 to +5 V.

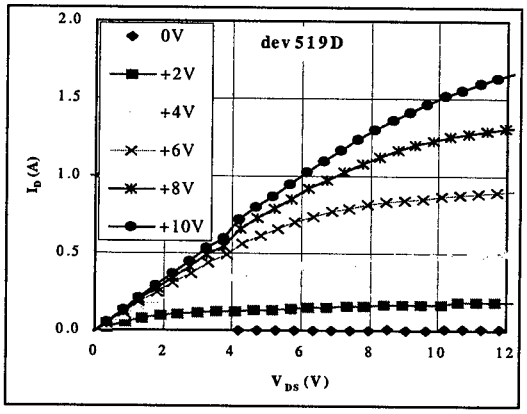

Fig. 7 The forward I-V characteristics of a large area device with L = 3 μm, W = 3 cm, L_{drift} = 10 μm. The active area was 560 μm x 1700 μm.

Summary: Lateral high voltage 6H-SiC MOSFETs have been successfully fabricated using 1400°C implant anneal in Ar ambient. The MOS inversion layer mobility is high enough (50-60 $cm^2/V{\cdot}s$) so that the FET resistance is limited by the resistance of the implanted drift layer, and not the MOS channel resistance, as desired. The measured specific on-resistance is 57 $mohm{\cdot}cm^2$ consistent with the drift layer sheet resistance (6180 ohm/sq). Future work should focus on obtaining higher breakdown voltages consistent with the drift layer design. This may involve optimization of the structure shown in Fig. 1 which has an extra P^+ implant to shield the gate oxide from the high fields.

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Highly Durable SiC nMISFET's at 450°C

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Keywords: High-Temperature Electronics, Jet Vapor Deposition, ONO Dielectric, Reliability

Abstract

Enhancement-mode nMISFET's fabricated on 6H-SiC substrates exhibit remarkable reliability and durability at high temperatures. These devices incorporate ONO (oxide-nitride-oxide) gate dielectrics made by the JVD (Jet-Vapor Deposition) method. Projected operating lifetimes of over 200 years under an oxide field of 3 MV/cm, and over 10 years under a field of 3.6MV/cm, have been demonstrated at 450 °C. These values are believed to far exceed the best data reported to date.

Introduction

It is well known that SiC is an attractive semiconductor for high-temperature and high-power applications. However, problems related to high gate leakage currents and poor gate dielectric integrity at high temperatures are also well known [1-4], especially for N-channel MOSFET's fabricated on p-type SiC substrates. For example, the best lifetime data for N-channel SiC MOSFET's in the open literature are in the neighborhood of only a few days under an oxide field of 3MV/cm at an operating temperature of 350°C [4], although that is already 100 times longer than the prior state-of-the-art. It is obvious that such short operating lifetimes pose severe limitations on the usefulness of SiC CMOS devices. It will be shown in this paper that the observed short lifetimes at high temperatures are not intrinsic to SiC NMOS technology, and can be substantially lengthened by the use of a suitable gate dielectric. More specifically, it will be shown that, by the use of an ONO (oxide-nitride-oxide) dielectric stack made by the JVD (Jet Vapor Deposition) method [5], a projected lifetime of over 200 years can be realized for a N-channel SiC MISFET operated under an oxide field of 3 MV/cm at a temperature of 450°C.

Device Fabrication

Non-self-aligned nMISFET's (W/L=250/50 μm, 250/200 μm) were fabricated on p/p+ 6H-SiC with the p-type epi-layer doped to ~2.7×10^{16}/cm^2 and the p^+ substrate doped to ~ 2.87×10^{18}/cm^2. Nitrogen ions, ranging from 20 keV to 360 keV, were implanted at room temperature to form the source/drain. The post-implant anneal was done at 1400 °C for 15 min in Ar ambient at 1 atm, with the samples encased in a SiC crucible to minimize Si evaporation. Both the field oxide and the gate oxide were made by JVD with a structure of silicon oxide-silicon nitride-

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silicon oxide (ONO) stack. The equivalent oxide thickness (EOT), calculated from the measured dielectric capacitance by assuming a dielectric constant of SiO_2 (3.9), is 140 nm and 28 nm for the field oxide and the gate oxide, respectively. The physical thickness is 10nm-20nm-10nm for the ONO stack gate dielectric. After deposition, the sample was annealed in N_2 at 900°C (1 hour for the field dielectric and 30 minutes for the gate dielectric), and then in water vapor for 1 hour at 950°C. Thermally evaporated aluminum was used as the electrodes for all 4 terminals of the MOSFET's: source, drain, gate and substrate. After the metallization, the sample was annealed in N_2 for 30 min and in water vapor for another 30 min, both at 400°C.

Time Dependent Dielectric Breakdown

Reliability of the fabricated devices was tested by constant-voltage stress in partial vacuum (10 mTorr) at 450 °C. A series of gate voltages (corresponding to oxide fields >5.71 MV/cm) were applied to a set of identical nMISFET, with the source, drain and substrate grounded. A device was considered to have "failed" when its gate current reached 0.25 mA/cm^2. Figure 1 shows a lifetime plot for the above experiment, where one can see that the projected lifetime reaches 280 years at 3MV/cm. Alternatively, this plot suggests that one can operate a device without failure for 10 years under an gate oxide field of 3.64MV/cm at 450 °C.

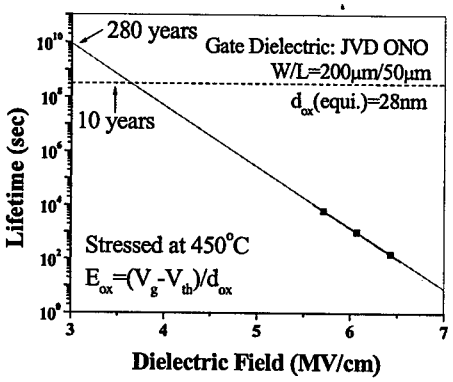

Fig.1 Intrinsic lifetime projection of SiC n-MISFETs measured at 450°C.

In fact, even after the device has failed the stress test, it typically still functions very well as exemplified by its slightly changed I_d-V_d characteristics (Fig.2a) compared to those before stress (see Fig.2b). It should be noted that the high-field and high temperature stress used in this study has caused a steady shift of the threshold voltage to a total of about 1V, due to electron injection and trapping in the dielectric. Such a shift is relatively small compared to those reported by others [4].

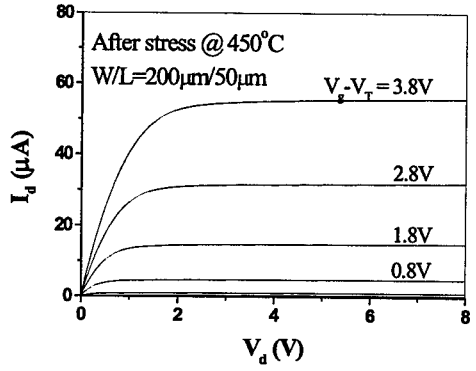

Fig. 2 (a) I_d-V_d characteristics of a nMISFETs measured at 450°C after stress at 6.07MV/cm for 1011sec.

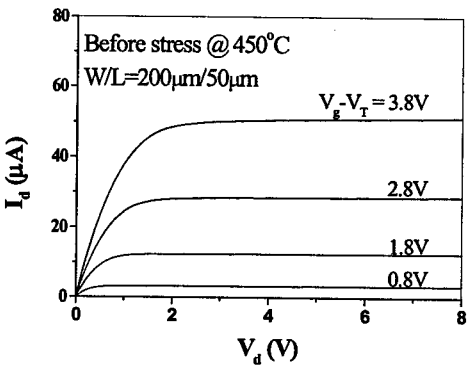

Fig. 2 (b) I_d-V_d characteristics of the above nMISFETs measured at 450°C before stress.

The high reliability of the SiC nMISFET's is attributable to the robust JVD dielectric [5,6], as well as its low gate leakage current at high fields and high temperatures. The use of the JVD ONO stack apparently also avoids the problem associated with electric field enhancement effect at the edges of the implanted source and drain regions.

An example of the low gate leakage current at 450 °C is shown in Fig. 4. With the source, drain and substrate grounded, the leakage current through the JVD ONO stack is very low even under high fields (e.g. 5×10^{-7}A/cm^2@6.5MV/cm). The J-E characteristics in the high-field region follow Fowler-Nordheim tunneling model, which can account for the very weak temperature dependence reported previously [6]. It should be noted that the flat current plateau for oxide fields below 4MV/cm is actually displacement current caused by the finite voltage ramping rate, and the actual gate leakage current should go down exponentially with lowering oxide field.

Conclusion

By the use of a JVD ONO stack gate dielectric, one can greatly improve the reliability of N-channel enhancement-mode SiC MISFETs at high electric fields and high temperatures. Projected lifetimes of such devices are in excess of 200 years under an oxide field of 3MV/cm at an operating temperature of 450 °C. At the same temperature, a 10-year projected operating lifetime can be realized for oxide fields as high as 3.6 MV/cm. These results clearly suggest that it is possible to fabricate highly reliable and durable high-temperature SiC CMOS transistors by the use of an appropriate gate dielectric.

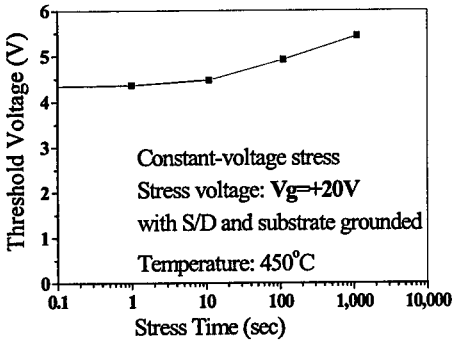

Fig3. Threshold voltage shift during the stress at 6.07MV/cm in 450°C

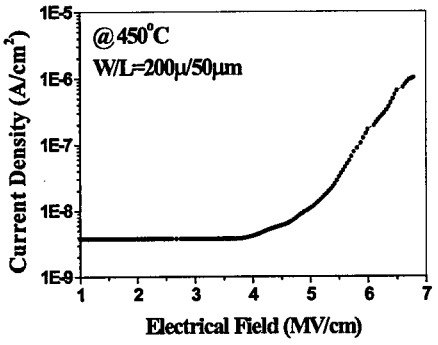

Fig.4. Leakage current under different gate electrical field at 450°C

Acknowledgment

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SiC MISFETs with MBE-grown AlN Gate Dielectric

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Keywords: Aluminium Nitride (AlN), Gate Dielectrics, High Temperature, MBE, MISFET

Abstract. Metal-Insulator-Semiconductor Field Effect Transistors (MISFETs) with ion implanted source and drain junctions have been made in 6H silicon carbide (SiC). Aluminum nitride (AlN) was used as the insulating gate dielectric, and was grown using molecular beam epitaxy (MBE). Gate controlled transistor operation was shown with an inversion layer mobility of 10-20 cm^2 / Vs. However, due to relaxation of the AlN film, the gate leakage was excessive, which precluded a thorough investigation of the transistor characteristics. This paper describes the manufacturing process and current voltage characteristics, and an improved process sequence is also proposed.

Introduction

Silicon carbide (SiC) has several materials properties which makes it of great interest for device applications. High breakdown voltage devices are possible due to the wide energy bandgap, and high frequency and high power devices due to the high saturated velocity and low dielectric constant. The wide bandgap and high thermal conductivity should also allow high temperature operation. Applications for high temperature electronics are many, and a low cost alternative using integrated circuits with MOSFETs in SiC would be a preferable technology due to the possibility of scaling [1]. However, this may be limited by reliability issues when using silicon dioxide as gate dielectric at high temperatures [2,3]. Aluminum nitride (AlN) promises an alternative high temperature stable dielectric for use in high temperature SiC MISFETs [4], and recent advances in nitride processing is presented in [5]. In this paper we investigate MBE-grown AlN as a gate dielectric for SiC MISFETs using a four mask layer process [6].

Experimental

The starting material was silicon face 6H SiC with a 4 μm thick low-doped (10^{16} cm^{-3}) p-type epitaxial layer from CREE Inc. The AlN film was grown by molecular beam epitaxy using a Perkin-Elmer 470 MBE-system. Prior to growth the surface was thermally oxidized, and the oxide was stripped using a 10:1 HF solution for 10 minutes immediately before loading. In the chamber the sample was desorbed for 30 minutes at 800 °C. Using a substrate temperature of 1000 °C, and ammonia as nitrogen source, 2.5 hours growth yielded an AlN thickness of 150 nm. Atomic force microscopy (AFM) showed the films to be smooth after growth (roughness on the order of 1 nm), with few visible defects. Originally the samples were intended for MIS capacitor structures, therefore the AlN film was grown prior to source/drain (S/D) formation.

The transistor process uses four mask steps: alignment marks, S/D implant, contact holes and S/D contacts, and gate contact. The alignment marks were etched using RIE with CF_4 and an aluminum etch mask. The same aluminum layer (after another lithographic step) was also used as mask during ion implantation of nitrogen at room temperature for n+ doping of the S/D, with

energies and doses of 80, 120, and 180 keV and 2.5, 3, and 5.5 x 10^{14} cm^{-2} respectively. The implant anneal was performed at 1400 °C, with the AlN film as a cap layer preventing SiC surface damage. Advantageous for processing is that contact holes can be wet etched in the AlN using photoresist developer (containing diluted NaOH) [7]. However, after the high temperature anneal the etch rate was not constant over the sample. Hence the source and drain contact holes were not completely etched in all parts of the wafer and low yield resulted. A liftoff step was used to make 200 nm thick titanium/aluminum source and drain contacts, which were alloyed at 600 °C. Finally, the gate was made using liftoff by evaporating aluminum (100 nm). A top view of the finished device is shown in Fig. 1, and a cross section in Fig. 2. The experimental devices were not self-aligned, since a rather large total gate length was used, overlapping the source and drain regions with about 10 μm. The S/D spacing used was 10 or 30 μm.

After the high temperature activation anneal, it was noted that the AlN film had relaxed. This is not surprising, since the AlN film was as thick as 150 nm, which is over the critical thickness considering the 1 % lattice mismatch between AlN and SiC. The triangular dislocation patterns can be seen in Fig. 1. A better process solution may be to grow the AlN film after the S/D ion implant activation anneal has been performed. This would lead to the same cross section as in Fig. 2, but higher anneal temperatures could be used without damaging the AlN insulating properties.

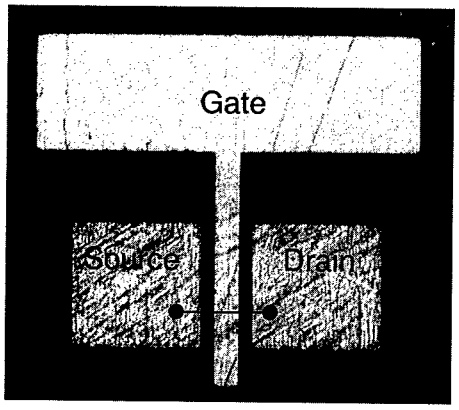

Fig. 1. Top view of AlN-SiC MISFET with 10 x 200 μm gate. (The line indicates the position of the cross section in Fig. 2.)

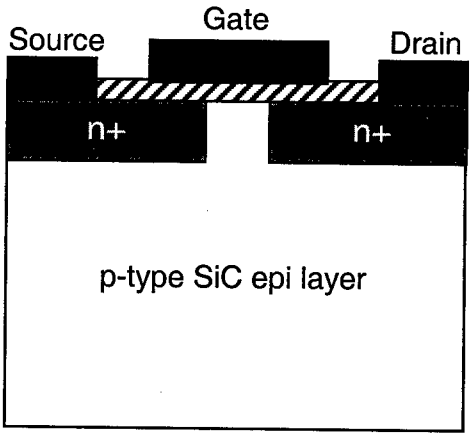

Fig. 2. Cross section of AlN-SiC MISFET in the gate region. Note the gate-to-drain overlap which causes leakage.

Results

Room temperature IV-measurements showed that the AlN films were very leaky, and therefore the measurement voltage had to be limited to 5 V. Also due to the high leakage in accumulation, high frequency capacitance voltage measurements could not be made over the entire range. The flatband voltage shift was not excessive (less than a few volts). Fig. 3 shows the drain characteristics at room temperature for gate voltages between 0 and 5 V, in steps of 0.5 V. (Note that the drain voltage in all measurements was stepped in 0.1 V steps, so the legend symbols do not represent data points). The same data is shown in a magnified view in Fig. 4. Three types of behavior is visible in the two figures: For drain voltages less than the gate voltage, a large leakage current (several mA) flows from the gate to the drain (negative drain current). For drain voltages much larger than the gate voltage, a leakage current flows from the drain to the gate (positive drain current).

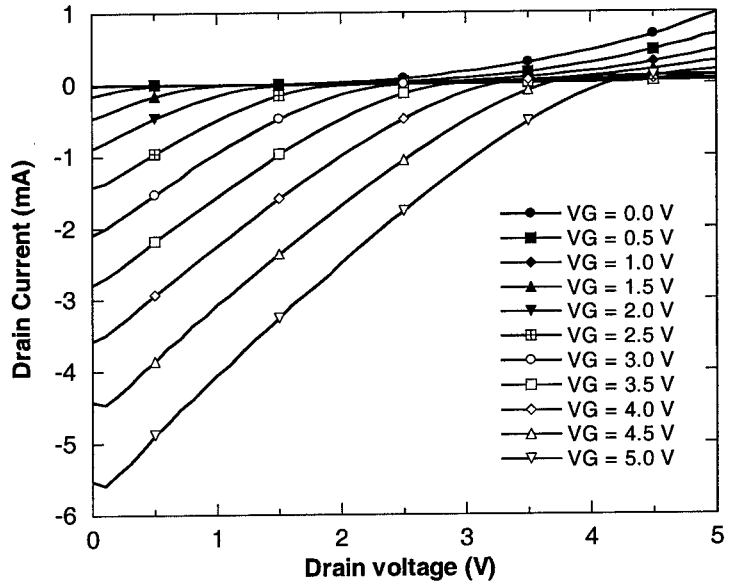

Fig. 3. IV characteristics at room temperature of an AlN-SiC MISFET with a gate length 10 μm. (NOTE: Drain voltage was varied in 0.1 V steps, so legend symbols do not represent data points.)

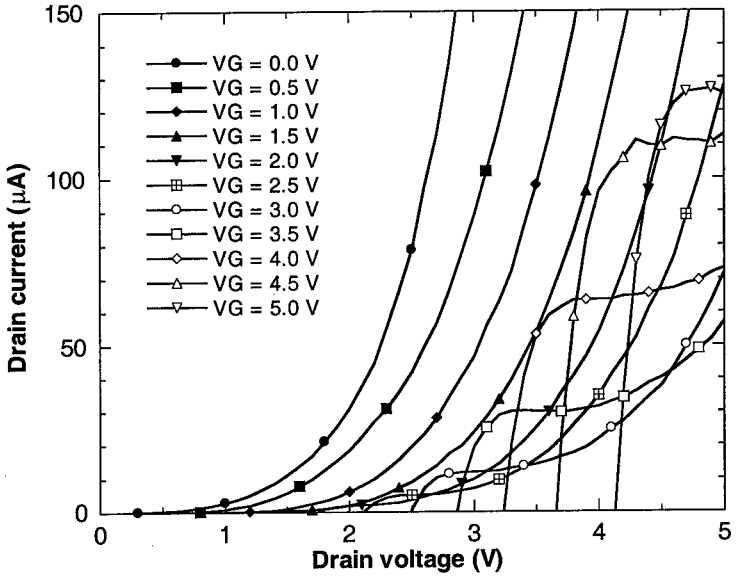

Fig. 4. Magnified view of Fig. 3. Saturated drain current is seen for gate voltages > 2 V. (NOTE: Drain voltage was varied in 0.1 V steps, so legend symbols do not represent data points.)

However, in the region where the drain voltage is only slightly larger than the gate voltage, AND the gate voltage is larger than about 2 V, we can see saturated drain current in the range of 100 μA, see mainly Fig. 4. This we interpret as evidence of gate controlled transistor operation for gate voltages between 2 and 5 V, since a leakage current can not be constant. Judging from the onset of

the saturated drain current flow, the threshold voltage for the device is around 2 V. Due to the high leakage, the drain characteristic is clearly distorted, evidenced by the overlapping current curves for increasing gate voltages. The linear region expected for low drain voltages is not present due to the leakage from gate to drain, similar to what is seen for silicon MOSFETs with ultra-thin gate oxides. Therefore the transconductance and the mobility can not be judged from the slope of the drain characteristic in the low field region, and have to be extracted for higher drain voltages in the range 3 to 5 V. The transconductance for the shown device is around 0.3 mS / mm gate length, and the inversion channel mobility is on the order of 10-20 cm^2 / Vs (at a drain voltage of around 4 V).

The gate current is high, and consists mainly of leakage current to the source, which means that for each gate voltage it is constant and equal to the drain current a drain voltage of 0 V. The substrate current was also monitored, but was found to be at least 6 orders of magnitude less than any of the terminal currents.

Summary

To our knowledge, this is the first SiC-AlN MISFET manufactured. Although the AlN film proved to be leaky, the demonstration of gate controlled transistor operation shows the promise of future devices. If the AlN leakage can be controlled by using a different process sequence, a new promising technology for high temperature integrated circuits is possible.

Acknowledgements

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Steady-State and Transient Forward Current-Voltage Characteristics of 5.5 kV 4H-Silicon Carbide Diodes at High and Superhigh Current Densities

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Keywords: Diffusion Length, Emitter Injection Coefficient, Lifetime, Rectifier Diode

Abstract. Steady-state and transient forward current-voltage characteristics of 5.5 kV p^+nn^+ 4H-SiC rectifier diodes have been measured up to a current density j = 55 kA/cm^2. The steady-state data are compared with calculations in the framework of a model, in which the emitter injection coefficient decreases with increasing current density. At a low injection level, the hole diffusion length and lifetime are estimated to be about 2 μm and 15 ns, respectively, whereas at a high injection level, these parameters are found to be 6 - 10 μm and 0.14 - 0.4 μs, respectively. The calculated and experimental results agree well within the wide range of current densities, 10 A/cm^2 < j < 4 kA/cm^2. At j > 5 kA/cm^2, the experimental values of residual voltage drop are lower than the calculated ones. In the range 5 kA/cm^2 < j < 20 kA/cm^2, the minimal value of differential resistance is found to be 0.15 mΩ·cm^2. At j > 25 kA/cm^2, the resistance increases with increasing current density manifesting the contribution of other non-linear mechanisms to the formation of steady-state current-voltage characteristic. The possible role of Auger recombination is discussed.

Introduction

Recently, 4H-SiC diodes with a blocking voltage as high as 4.5 kV (the width of the blocking n-base W_n = 45 μm) [1] and 3.4 kV (W_n = 30 μm [2]) have been successfully demonstrated. High-voltage SiC diodes are expected to show faster switching and lower residual voltage drops at high current densities in comparison with those of identically rated Si diodes. However, current-voltage (*I-V*) characteristics of high-voltage SiC diodes at high current densities have not been investigated by now. In this work the forward *I-V* characteristics of 5.5 kV 4H-SiC p^+nn^+ diodes have been measured up to a current density of 55 kA/cm^2. The results obtained are compared with calculations in the framework of a model [3] in which the emitter injection coefficient decreases with increasing current density.

Experimental details and theoretical approach

The p^+nn^+ 4H-SiC diodes under investigation had the 1.5 μm thick p^+-emitter and 85 μm thick n-base layers. The background doping of the n-base is equal to N_d = (7-10)×10^{14} cm^{-3}. Structures with diameter of 100 μm were fabricated on the n-type substrate with the doping level of 5×10^{19} cm^{-3}. *I-V* characteristics were measured up to the current density of 55 kA/cm^2, using a pulse generator (with rise time of 30 ns). The kinetics of current and voltage rise were recorded simultaneously. The hole diffusion length at low injection level, L_{pl} was measured by photoresponse technique. The hole lifetime at high injection level, τ_{ph} was estimated from the kinetics of current and voltage rise time.

It is known that at high current densities, forward voltage drop across a diode is determined by several non-linear processes, such as electron-hole scattering, Auger recombination, and

dependence of emitter efficiency on current density. However, for SiC devices, these processes are practically not studied until now. To describe the experimental results, we used a theoretical model [3] which takes into account the non-ideality of the p^+-emitter and base modulation. The flat profile of the doping in the base and abrupt p^+-n and n^+-n junctions were assumed. The voltage drop on the base was calculated by the numerical integration using the analytically obtained carrier distribution along the base. Instead of the saturation current density j_s used as the fitting parameter in that model a new fitting parameter a was introduced in [4]: $a = j_s(L/qDn_i)^2$, where q is the electron charge, $D = [2b/(b+1)]D_p$ is the ambipolar diffusion coefficient, D_p is the hole diffusion coefficient, $L = (D\tau_{ph})^{1/2}$, $b = \mu_n/\mu_p$ (μ_n and μ_p are the electron and hole mobilities), and n_i is the concentration of intrinsic carriers. Within the temperature interval of 300-600 K a varies (1.5-2)-fold. Physical limitations on a can be established as follows:

$$0 < a < \left[qN_d \left(\frac{2b}{b+1} \right)^{1/2} \left(\frac{D_p}{\tau_{ph}} \right)^{1/2} \right]^{-1}. \qquad (1)$$

Results and discussion

Fig. 1 presents the time dependencies of current and voltage during the turn-on process.

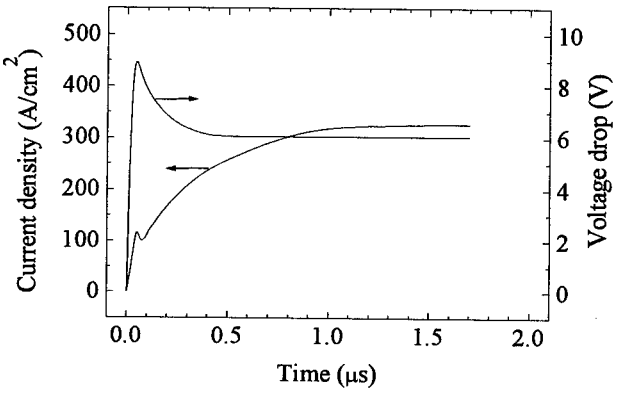

Fig. 1. Time dependencies of current and voltage during the forward turn-on process. Steady-state current density and residual voltage drop are 350 A/cm^2 and 6.2 V, respectively.

It is seen that the characteristic transit time τ_T is about 0.3 μs. Although there is no precision technique for extracting the hole lifetime τ_p from such transient characteristics, it is clear from simple physical reasons that $\tau_p \sim \tau_T$ [5]. The current density through the p^+n junction which corresponds to a transition from the low to high injection level can be estimated as 0.5 A/cm^2. Thus, the dependencies shown in Fig.1 correspond to a high injection level, and the lifetime τ_p estimated from transient characteristics is the hole lifetime at high injection level, τ_{ph}.

The hole lifetime at a low injection level, τ_{pl} was estimated by the photoresponse technique. The dependence of photocurrent versus space charge region thickness has given a diffusion length $L_{pl} = 1.9$ μm. Taking $D_p = 2.6$ cm^2/s, we calculate the hole lifetime $\tau_{pl} = L^2_{pl}/D_p = 14$ ns. Note that $\tau_{pl} << \tau_{ph}$.

Experimental *I-V* characteristics of a 4H-SiC diode and the results of theoretical calculations are shown in Figs. 2-3. Dashed line in Fig. 2 represents result of calculation at a diffusion length $L = (D\tau_{pl})^{1/2} = L_p(D/D_p)^{1/2} = (4/3)L_p = 2.5$ μm, where $L_p = 1.9$ μm is the hole diffusion length measured by the photoresponse technique. The value of a was assumed to be zero ($a = 0$, "ideal emitter"). It is seen that the calculated and experimental results differ qualitatively. Indeed, the ratio $W_n/L = 33$ is

too large to provide the observed base modulation. Solid line in Fig. 2 represents calculation at $a = 0.08$ cm^2/A and $L = 12$ μm ($\tau_{ph} = 0.3$ μs). (With $b = 8$, $N_d = 10^{15}$ cm^{-3}, $D_p = 2.6$ cm^2/s, and $\tau_{ph} = 0.3$ μs, the a value lies (see Eq. 1) in the range $0 < a < 1.6$ cm^2/A.)

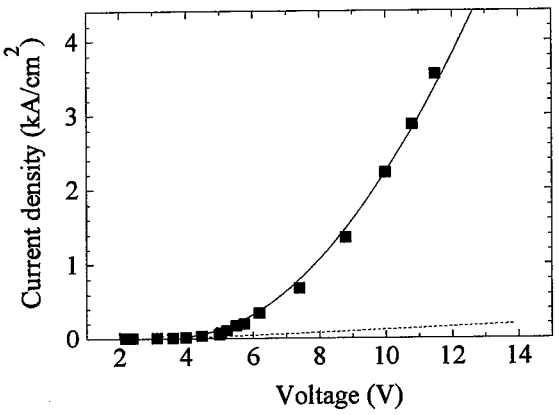

Fig. 2. Current-voltage characteristics of a 5.5 kV 4H-SiC diode up to $j \approx 4$ kA/cm^2. Points are experimental data. Dashed line is the result of simulation with $a = 0$ and $L_p = 1.9$ μm. Solid line is the result of simulation with $a = 0.08$ cm^2/A and $L_p = 9$ μm.

The value $a = 0.08$ cm^2/A corresponds to the injection coefficient $\gamma = 0.95$. Note that j_s is about 3×10^{-47} A/cm^2 at the given parameters and $a = 0.08$ cm^2/A. It is seen from Fig. 2 that there is a good agreement between experimental and calculated results in a very wide current density region 10 A/cm^2 $< j <$ 4 kA/cm^2.

At $j > 5$ kA/cm^2, a strong discrepancy is observed between experimental data and results of simulation (Fig. 3).

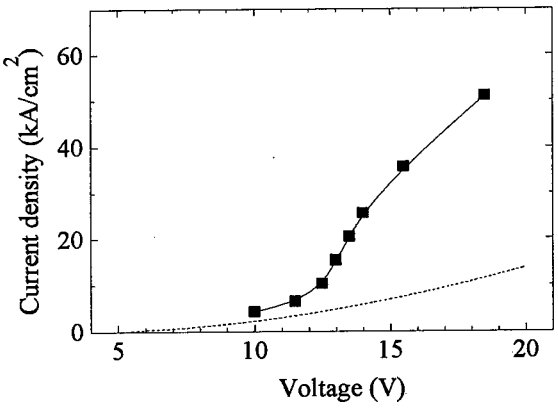

Fig. 3. Current-voltage characteristics of a 5.5 kV 4H-SiC diode up to $j \sim 55$ kA/cm^2. Solid line is the experimental data. Dashed line is the result of simulation with $a = 0.08$ cm^2/A and $L_p = 9$ μm.

The current increases much more steeply with increasing bias than it is predicted by the model. Such a behavior may be only due to a sharp increase of the minority carrier lifetime τ_{ph} from 0.3 μs to 3.2 μs. Such an increase of the lifetime can be explained by that the main recombination trap which controls the lifetime in the base is filled at very high hole concentrations, and the corresponding recombination channel is saturated. The other effect which can contribute to the observed effect is as following. The simple estimations show that the self-heating of the diode at the end of the pulse at

$j = 60$ kA/cm^2 and voltage drop $V = 20$ V achieves $\Delta T \approx 100$°C. When junction temperature rises, deep p-type dopants in the p$^+$-emitter get ionized, and higher injection efficiency can be achieved.

It can be seen in Fig. 3 that at $j > 25$ kA/cm^2 the differential resistance R_d increases with increasing j. It is well known that a decrease of the emitter injection coefficient with increasing current density can not explain such an effect. In the framework of the model under consideration, R_d is saturated at high current density. For the parameters discussed, the calculated R_d value is saturated at $j > 40$ kA/cm^2 and remains unchanged up to $j = 200$ kA/cm^2.

Hence, we may conclude that the effect is determined by one of the non-linear mechanisms, electron-hole scattering or Auger recombination. Parameters of electron-hole scattering for SiC are not known until now. The Auger recombination coefficient $C = 8\times10^{-31}$ cm^{6}s^{-1} was recently estimated for 4H-SiC using time resolved free carrier absorption technique [6]. The lifetime τ_A of excess carriers, related to Auger recombination, can be calculated as $\tau_A = 1/Cp^2$. It can be seen that τ_A must be equal to the carrier lifetime due to trap recombination at $p = (1/\tau_{ph}C)^{1/2}$. Assuming $\tau_{ph} = 0.3$ μs, we find that $\tau_A = \tau_{ph}$ at $p \approx 2\times10^{18}$ cm^{-3}. However, as mentioned above, τ_{ph} is about 3.2 μs at very high injection level. For such a value of τ_{ph}, the condition $\tau_A = \tau_{ph}$ is satisfied at $p \approx 6\times10^{17}$ cm^{-3}. This hole concentration is reached at the p$^+$n boundary at $j = 25$ kA/cm^2. In this case, the effect of Auger recombination must be very important.

Conclusion

Forward current-voltage characteristics of 5.5 kV 4H-SiC p$^+$n rectifier diodes have been experimentally investigated in a wide current density range. The hole lifetimes at low and high injection levels have been estimated of 15 ns and 300 ns, respectively. Experimental results at current densities ranging from 10 A/cm^2 to 4 kA/cm^2 coincide well with calculations in the framework of a model taking into account the decrease of the emitter injection coefficient with increasing current density. To explain the experimental results at current densities above 5 kA/cm^2, it should be assumed that the trap with very different capture cross sections for electrons and holes contributes significantly to the process of recombination. An increase of the differential resistance at current densities above 25 kA/cm^2 has been observed experimentally. The estimations show that Auger recombination in the base may be responsible for this effect.

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Current Voltage Characteristics of High-Voltage 4H Silicon Carbide Diodes

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Keywords: Contact Resistance, Electroluminescence, Excess Current, High Voltage, IV Characteristics, JBS, Leakage Current, pn Diode, Schottky, Shunt, TLM

Abstract: High-voltage 4H silicon carbide diodes with breakdown voltages above 3500V were processed and characterized by using different techniques. Measurement results of the electrical properties of p^+–ν–n and Schottky high-voltage diodes are presented. The achieved Schottky barrier height at room temperature was estimated to be $\Phi_b = 1.17\,\mathrm{eV}$ from IV measurements. The p^+–ν–n diodes showed negligible leakage current densities of $J_r \leq 0.5\,\mu\mathrm{A\,cm^{-2}}$ at 1000V reverse bias. We also present a simple model to quantitatively characterize excess currents observed under low forward biases in different diode structures.

Introduction

The inherent properties of silicon carbide have attracted much attention during the last decade for the application in high temperature and high frequency power electronic devices. So far however the commercialization of such devices has been delayed due to major difficulties in the production of the necessary high quality material and the need of new or modified process technology compared to the standard silicon mainstream.

In this paper we describe the electrical characteristics of high voltage diodes based on thick low-doped n-type epitaxial layers of the 4H silicon carbide polytype. The investigated diodes include implanted pn junctions, Schottky junctions and combined junction barrier Schottky (JBS) rectifiers [1]. It is our goal to gain understanding of the role of different defects on the electrical properties of power devices made out of this material.

Experimental Details

Various types of diodes were manufactured on one half of a commercial 35 mm 4H SiC wafer (manufactured by Cree, n-type, $1.1 \cdot 10^{19}\,\mathrm{cm^{-3}}$) with a subsequently grown CVD epitaxial layer (grown at Linköping University, n-type, $1.6 \cdot 10^{15}\,\mathrm{cm^{-3}}$, thickness 35 μm). The pn junctions and field rings around some diodes [1] were formed by a deep ($\approx 1\,\mu$m) boron and a more shallow aluminum coimplantation through a single mask layer (SiO_2). The implantation damage was removed and the implanted species were activated by a high temperature anneal at 1700 °C. A combined metallization layer was applied to serve a) as an ohmic contact to the p-type implanted areas, b) as a Schottky contact to the n-type epitaxial layer and c) to form terminating fieldplates and guard rings on top of the isolating field oxide. First a 200 nm layer of titanium was deposited by e-beam evaporation, followed by a 400 nm layer of aluminum. During the following anneal for 2 min at 600 °C some alloying between the metal layers and the silicon carbide surface was observed while the contact resistance of the ohmic contacts to the p-type implanted areas decreased by a factor of two to finally $\leq 10^{-2}\,\Omega\,\mathrm{cm^2}$ as determined by linear TLM measurements at room temperature [2]. The metal layer was patterned by standard lift-off technique with negative photoresist. A large area backside ohmic contact was processed by e-beam evaporation of nickel.

Electrical measurements were performed using a modified *Rucker & Kolls* model 260 probe station, a *Keithley* 237 high-voltage source-measure-unit (SMU) for high resolution measurements (with a four point probe) under forward and reverse (< 1100V) bias and a *Bertan* 225-10R 10 kV supply for high-voltage measurements under reverse bias. To avoid sparking in air and to reduce surface leakage currents the sample was immersed in dielectric silicone fluid (*Dow Corning* DC550) during high voltage measurements. CCD micrographs were taken

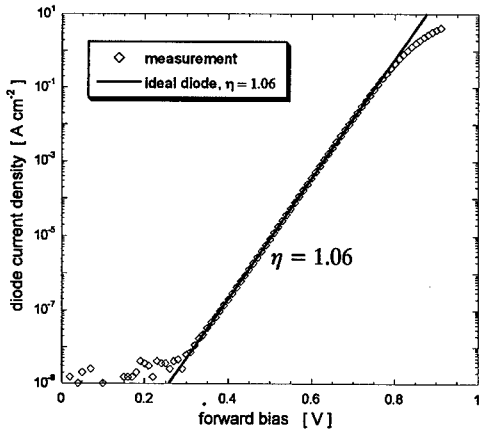

Figure 1: *Typical IV characteristic of a processed Schottky diode. The measured ideality factor is* $\eta = 1.06$ *and thus allows for the extraction of a Schottky barrier height of* $\Phi_b = 1.17\,\mathrm{eV}$ *from the IV measurement data at room temperature. For current densities of* $J \geq 1\mathrm{A\,cm^{-2}}$ *the voltage drop across the diode is increased partially due to the influence of contact and substrate series resistances.*

with a *Hamamatsu* C4880 CCD camera attached to a *Nikon* microscope in order to correlate electroluminescent light emission from the junction areas to non ideal features in the electrical characteristics of the diodes.

Results and Discussion

a) Schottky diodes

Figure 1 shows a typical forward IV characteristic of a Schottky diode. The ideality factor of these Schottky diodes was $\eta \leqq 1.1$ and therefore allows for the thermionic emission theory to be applied to explain carrier transport over the Schottky barrier.

$$J = J_s \left(e^{qV/k_BT} - 1\right) = A^*T^2 e^{\Phi_b/k_BT} \left(e^{qV/k_BT} - 1\right) \quad \text{with } A^* = \frac{4\pi\, e\, m^* k_B^2}{h^3} \qquad (1)$$

Assuming an effective Richardson constant for silicon carbide of $A^* = 120\mathrm{A\,cm^{-2}\,K^{-2}}$ (as calculated for an effective electron mass $m^* = m_0$) [3, 4] we can extract a Schottky barrier height at room temperature of $\Phi_b = 1.17\,\mathrm{eV}$ from the measured saturation current density of $J_s = 7{\cdot}10^{-14}\mathrm{A\,cm^{-2}}$. This is in good agreement to results obtained by Raghunathan et.al. using titanium on 4H silicon carbide [5]. An error of a factor 2 in the assumption of the Richardson constant A^* would change this value for the barrier height Φ_b by less than $\pm 0.02\,\mathrm{eV}$, which justifies the use of our approximation of the effective electron mass m^*.

b) pn diodes

The analysis of 28 similar pn diodes distributed over the processed area of the wafer ($2\,\mathrm{cm^2}$) does not show any significant variations in the electrical properties in spite of expected variations in the thickness, doping and carrier lifetime of the epitaxial layer. Most of the smaller size pn diodes (diameter $\leqq 200\,\mu\mathrm{m}$) exhibit a forward IV characteristic with two distinct regions with different mechanisms dominating the current transport. The ideality factors of $\eta_1 = 2$ and $\eta_2 = 1.2$, respectively as shown in fig. 2.

However, a significant number of diodes deviate from the above described behavior by showing a feature in their forward IV characteristics which has been described as an excess current in the literature [6, 7]. In order to explain the nature of this excess current we propose a model in which a second diode with a significantly higher saturation current serves as a shunt parallel to the main junction under low applied forward biases. A similar model was used by Defives et. al. to explain IV characteristics of silicon carbide Schottky diodes [8]. The forward voltage drop V of a non-ideal pn diode can be approximated as a function of the forward current I :

$$V = \frac{\eta k_B T}{q} \ln\left(\frac{I}{I_s}\right) + IR_S \qquad (2)$$

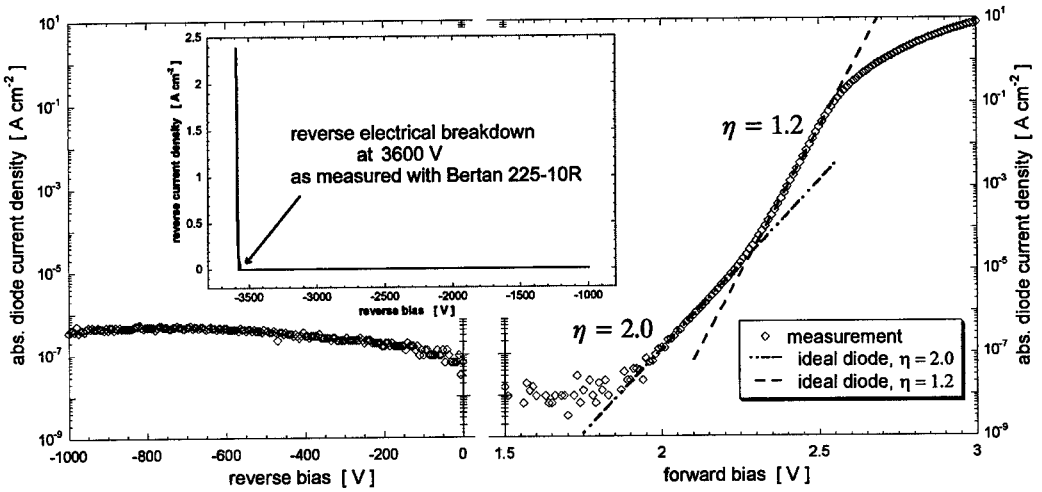

Figure 2: *Measured forward and reverse IV characteristic of a typical pn diode with 200 μm diameter and protected by an isolated metal guard ring. The measurement was performed in air using the Keithley 237 SMU and the data was plotted on a semilogarithmic scale. Under forward bias, two regions with ideality factors $\eta_1 = 2.0$ and $\eta_2 = 1.2$, are distinguishable. The inset shows the electrical breakdown at 3600V measured with a Bertan 225-10R high-voltage supply, the sample being submerged under silicone fluid.*

where η is the ideality factor of the junction, I_s is the dark or saturation current, k_B is the Boltzmann factor, q is the elementary charge, T the junction temperature and R_S is the series resistance (first order) of the diode. By parallel coupling of two independent diodes with different parameters (I_s, R_S, η and I'_s, R'_S, η' respectively), the current through this network for a given forward bias is the sum of the individual currents $I_{\text{total}}(V) = I(V) + I'(V)$.

The analysis of the experimental data using this model reveals a series resistance typically five to six orders of magnitude higher for the shunting diode than for the main junction. Together with the analysis of CCD micrographs taken under forward bias which show hot spots of significantly increased electroluminescence we suggest that this high resistance is due to the high spreading resistance of small current paths through the diodes related to crystallographic defects.

The magnitude of these excess currents has been observed to increase after the diode has been exposed to high reverse biases while it returns to its initial value after being forward biased for some time at a current density of $J \geq 5\text{A}\,\text{cm}^{-2}$ as shown in fig. 3. We observed a similar decrease while heating the diodes for 65 hours at 250 °C in an argon atmosphere, indicating the possible influence of trapped charges in deep states in the bandgap of the silicon carbide material as described by Ramungul and Chow for the influence on current controlled negative resistances [9].

Under reverse bias above approximately 1000V, bright spots of electroluminescence occurred outside the junction area of a number of metallized pn diodes. This kind of spots was also visible underneath the p-implanted anode region in pn diodes without metallization at positions which often correlate to positions of increased electroluminescence under forward bias (see also [10]). Together with an increasing leakage current these spots indicate the onset of microplasmatic breakdown as reported earlier [10,11].

Conclusions

Electrical and electro-optical measurement methods have been applied to characterize the properties of silicon carbide high-voltage diodes. The correlation of results obtained by these supplementary techniques leads to a more concise understanding of the role of the different types of crystallographic defects found in state-of-the-art silicon carbide material (substrates

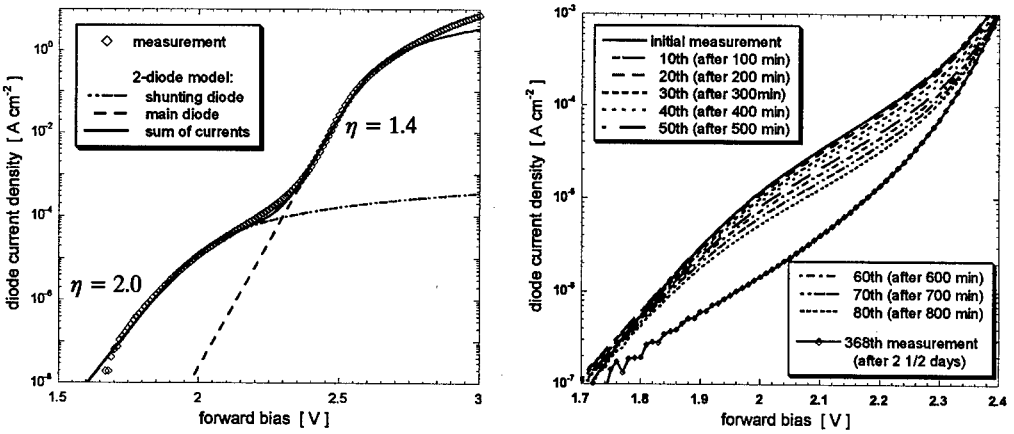

Figure 3: *Measured IV characteristics of a pn diode showing an excess current for low forward biases. The left image shows the fit of the measured data in the proposed two-diode model with parameters* $J_s = 1.6 \cdot 10^{-32}\mathrm{A\,cm^{-2}}$, $\eta = 1.4$, $R_S = 0.1\,\Omega\mathrm{cm}^2$ *for the main junction and* $J_s' = 4.4 \cdot 10^{-20}\mathrm{A\,cm^{-2}}$, $\eta' = 2.0$, $R_S' = 1000\,\Omega\mathrm{cm}^2$ *for the shunting diode. The right image shows the decrease of the excess current during repeated measurements. The original diode characteristic w/o excess current is reached again after 2 1/2 days of measurements.*

and epitaxial layers) on the electrical characteristics of high voltage devices. In the processing of high-voltage diodes presented in this paper, high breakdown voltages and low leakage currents have been achieved in spite of defects most likely to be present in these diodes. A model has been introduced to quantitatively describe the so-called "excess currents" for low forward biases which are observed on a number of different types of diodes.

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Materials Science Forum Vols. 338-342 (2000) pp. 1327-1330

Dynamic Avalanche and Trapped Charge in 4H-SiC Diodes

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Keywords: Carrier Traps, Dynamic Avalanche, Impact Ionization, Reverse Recovery

Abstract. A dynamically reduced breakdown voltage from more than 2 kV under static conditions to 300 V during reverse recovery was measured for 4H-SiC p^+nn^+ diodes. Device simulation indicates that deep hole-trapping donors in the n-base, close the pn junction, could explain the dynamically reduced breakdown voltage. Hole traps situated 0.66 eV above the valence band were found in the diode n-base by DLTS measurements.

1. Introduction

4H-SiC has due to its wide bandgap very attractive properties for high voltage and high temperature applications. The high critical field strength of 4H-SiC enables the design of high voltage diodes with about ten times shorter n-base width than comparable Si diodes. The shorter n-base reduces the series resistance and the reverse recovery current, the latter by reducing the stored charge during forward conduction. Another predicted advantage of SiC compared to Si is a much higher onset level of dynamic avalanche during reverse recovery [1]. This higher avalanche onset level is explained by the higher n-base doping of SiC diodes, which means that the hole mobile charge at high reverse current densities has a smaller influence on the electric field. Reverse recovery has been studied by for instance refs. [2, 3], but the high predicted onset level of dynamic avalanche has to the authors knowledge not been reached. In this work, a substantial avalanche was found at low voltages of about 300 V during reverse recovery for Boron-implanted p^+nn^+ diodes, which had a static breakdown voltage of more than 2 kV. The commonly described dynamic avalanche [1] which results from electric field enhancement by a current controlled hole mobile charge cannot explain this large difference between static and dynamic breakdown voltage. It has therefore been investigated by device simulation how a positive trapped charge resulting from hole capture by deep donors may temporarily increase the electric field during reverse recovery. These device simulations could qualitatively reproduce the measured avalanche. Hole traps situated 0.66 eV above the valence band were found in the n-base of the experimentally studied diodes using DLTS measurements. Ion implantation in combination with diffusion is a probable source of the hole traps [4]. The importance of carrier trapping in deep levels for the transient behavior of SiC devices have previously been pointed out by refs. [5-7].

Reverse recovery measurements

A special optical measurement technique described in ref. [3], was used to obtain reverse recovery in the bulk diode region. A carrier plasma is created in the diode n-base with a fast (5 ns) laser pulse, which enters through a centrally located 0.3 mm diameter hole in the anode metallization. The laser pulse arrives in open-circuit conditions and a following rapid application of a high reverse voltage produces reverse recovery in the optically excited region. The laser pulse creates an estimated carrier concentration of approximately $1*10^{18}$ cm^{-3} to achieve reverse recovery with high current densities. The experimentally studied diodes are test diodes of a process similar to ref. [8]. The n-epilayer is about 35 μm wide with a doping concentration of approximately $1*10^{15}$ cm^{-3}. The

p^+ region was formed by Boron-implantation, followed by high-temperature annealing. The circular diodes, which have an active area of 0.5 mm^2 (800 μm diameter) could block a reverse voltage of 2 kV with a small leakage current under static conditions.

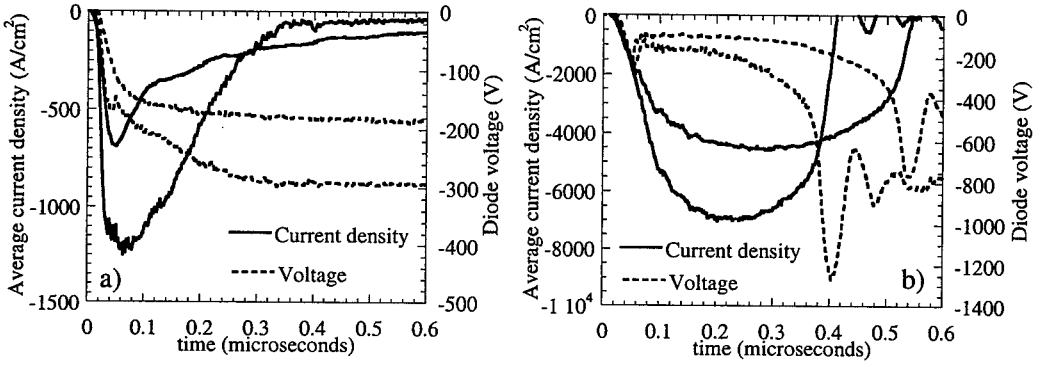

Fig. 1 Optical reverse recovery measurements for blocking voltages 200 and 300 V (a) and 500 and 800 V (b). Current density (solid line), diode voltage (dashed line).

Fig. 1a shows reverse recovery measurements for blocking voltages 200 and 300 V. The large increase of the integrated reverse current and the reduced dV/dt in the 300 V measurement are clear indications of avalanche multiplication. This avalanche becomes more pronounced for the reverse voltages 500 V and 800 V in Fig. 1b where the reverse voltage falls for a short period and dV/dt is strongly reduced as the current density increases to peak values of several thousands A/cm^2. The Fig. 1 measurements are averaged from ten pulses, to suppress oscillations which appeared above the avalanche threshold. Avalanche did not occur as the diode was reverse-biased 2 μs after the laser pulse (when the carrier plasma had essentially recombined) or if the laser intensity was reduced with about 95 %.

Device simulation and carrier traps

The optical experiment was simulated using the drift-diffusion-based software tool TMA Medici [9], with a simple SPICE model of the switching circuit. The set of physical models for simulating 4H-SiC was taken from ref. [1]. Fig. 2 shows a simulation of the optical experiment for 1200 V blocking voltage with and without impact ionization included in the simulation models. The difference between the simulations indicates that the onset of dynamic avalanche should occur at around 5-6 MW/cm^2 (about 8000 A/cm^2 and 700 V) during reverse recovery. In ref. [3], optical reverse recovery measurements resulted in no dynamic avalanche for a similar 4H-SiC p^+nn^+ diode with a peak power density of about 1200 kW/cm^2 for a blocking voltage of about 1000 V. The onset of avalanche in the Fig. 1 measurements did however occur already at about 250 kW/cm^2 (1250 A/cm^2 and 200 V), which is only about 5 % of the peak power dissipation in Fig. 2. The high static breakdown voltage (>2 kV)

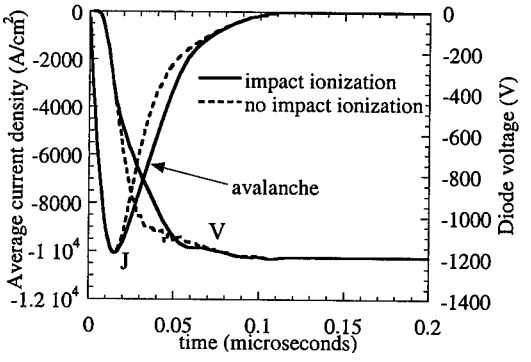

Fig. 2 Simulated optical reverse recovery for blocking voltage 1200 V. Impact ionization included (solid line), excluded (dashed line).

of the diodes indicates that the measured avalanche during reverse recovery is not caused by a reduced critical field strength of the material. To look for an alternative explanation to the measured avalanche, device simulations were performed to examine how deep hole traps would affect the electric field distribution during reverse recovery. The influence of carrier trapping in deep levels on the failure limit of 4H-SiC diodes has previously been examined by refs. [5, 6]. Carrier trapping was also studied in high-dose electron irradiated Si diodes in ref. [10], where a temporarily reduced breakdown voltage resulted from hole-trapping in deep donor levels during reverse recovery.

Hole traps situated (0.66 $\pm$0.06) eV above the valence band were found in DLTS measurements for the experimentally studied diodes. The trap concentration could however not be measured since the DLTS signal could not be saturated, i.e. all traps could not be filled. The charge state of the traps is not clear since it is not determined by DLTS and both acceptor and donor hole traps have been reported close to the measured trap energy [4]. Device simulations including carrier traps were performed with a hole trap level at the measured energy level 0.66 eV above the valence band. The trap level was assumed to be a donor, i.e. it becomes neutral after hole emission [11]. A hole capture cross-section $\sigma_p=1*10^{-14}$ cm^2 was used, according to DLTS measurements for the D-center in 6H-SiC [12]. A trap profile with a peak concentration of $3*10^{16}$ cm^{-3} at the pn-junction and a linear decay extending 4 μm into the n-base was assumed in simulation. This assumption is arbitrary but not unreasonable since it has been proposed that high concentrations of deep traps, exceeding the activated doping concentration can form in a Boron diffusion tail [4]. Fig. 3 displays simulation results with and without the described hole trap distribution for otherwise identical p^+nn^+ diodes. Without the traps (a), the diode reaches the blocking voltage fast and the peak electric field in the 800 V simulation reaches about $8*10^5$ V/cm, which is below the onset of avalanche. With traps (b), the peak electric field in the 300 V simulation becomes more than $1.2*10^6$ V/cm and avalanche results in a slow current decay. A substantially reduced voltage rise-time for increasing voltages in the measurements (see Fig. 1) is in qualitative agreement with the simulations with traps in Fig. 3b, and this effect is not obtained without traps in Fig. 3a. The high trap concentration close to the pn junction also results in a very low local carrier lifetime (in the nanoseconds range) which explains why the peak reverse current becomes lower with traps than without traps (see Fig. 3). Fig. 4 illustrates the electric field enhancement which results from trapped holes during reverse recovery at t=0.080 μs in the 300 V simulation in Fig. 3b. The hole traps in the n-base are empty and neutrally charged before the laser pulse arrives. The laser pulse creates a carrier plasma in the n-base region, and the traps capture holes and become positively charged. As the diode is reverse-biased, the holes remain trapped since thermal emission of electrons from the valence band to the trap level 0.66 eV above should have a time constant of about one second for a capture cross-section $\sigma_p=1*10^{-14}$ cm^2.

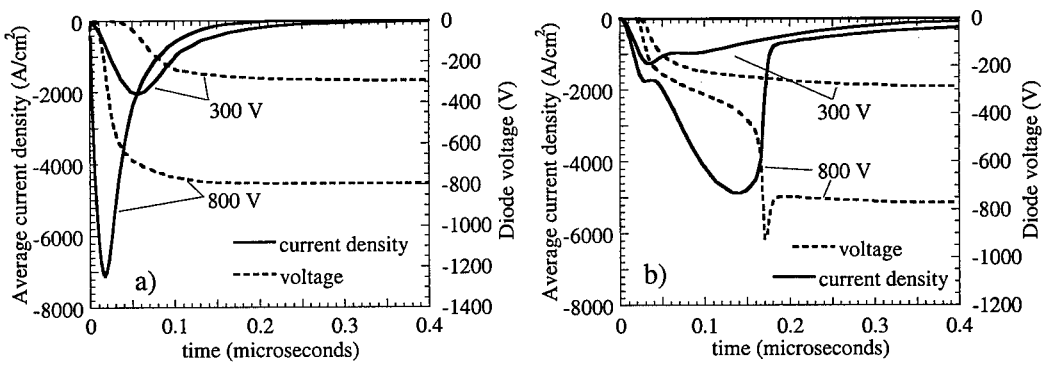

Fig. 3 Simulated reverse recovery for 300 and 800 V. a) Diode without traps, b) with hole traps.

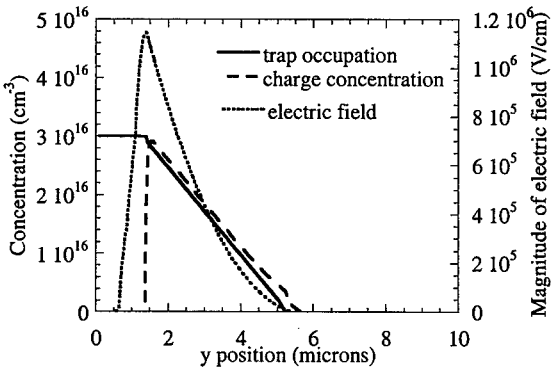

Fig. 4 Trap occupation (solid line), charge concentration (dashed line) and local electric field (dotted line) in the pn-junction region at t=0.080 μs in the Fig. 3b 300 V simulation.

Thermal emission is therefore presumably much too slow to keep up with the change in bias conditions, in analogy with results for the shallower Boron acceptor level in ref. [7]. The hole traps effectively control the space charge and peak electric field since the peak concentration of trapped hole charge becomes about 30 times higher than the n-base doping level (see Fig. 4). Deep hole traps which become positively charged after hole capture is thus a possible explanation for the large difference between static and dynamic breakdown voltage in this work. The proposed avalanche mechanism is in analogy with recent observations for Si power diodes [10]. To obtain the described electric field enhancement (see Fig. 4), the trap has to be a donor, i.e. positively charged with a hole. According to simulations, the traps release their holes by electron capture from the conduction band after the carrier plasma in the n-base has recombined. Electron capture is therefore a likely explanation why the avalanche current eventually decays (see Figs. 1b and 3b) and why no avalanche was observed as the diode was reverse-biased after the plasma had recombined (2 μs after the laser pulse).

Summary

A large difference in breakdown voltage between more than 2 kV under static conditions and 300 V during reverse recovery was measured for 4H-SiC p^+nn^+ diodes. Electric field enhancement by a current controlled hole mobile charge is according to simulations, not sufficient to explain this large dynamic reduction of the breakdown voltage. Simulations indicate, on the other hand, that hole-trapping by deep donors could explain the measured avalanche during reverse recovery. Hole traps situated 0.66 eV above the valence band was found in the diode n-base, close to the pn junction, in DLTS measurements. In summary, the results in this work indicate that hole traps which are deep donors can significantly enhance the local electric field during reverse recovery and thus dynamically reduce the breakdown voltage of 4H-SiC p^+nn^+ diodes.

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Materials Science Forum Vols. 338-342 (2000) pp. 1331-1334

Comparison of Nitrogen and Phosphorus Implanted, Planar, High-Voltage 4H-SiC Junction Rectifiers

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Keywords: 4H-SiC, Diode, Junction Rectifiers, Nitrogen, Phosphorus

Abstract. High-voltage $n^+/p/p^+$ junction rectifiers have been fabricated on 4H-SiC using nitrogen and phosphorus as n^+ implants. The performance of the devices, fabricated with varying junction termination extension (JTE) species and post-implant anneal temperatures, were compared. Diodes with breakdown voltage as high as 1300V were obtained using a 10μm epitaxial layer. The best forward forward characteristics were obtained on the phosphorus implanted diodes annealed at 1600°C (forward voltage ~5V at 100A/cm^2). The leakage currents on the phosphorus implanted diodes were slightly higher than the nitrogen implanted diodes (due to damage caused by the heavier phosphorus).

1. Introduction

Silicon carbide (SiC)-based semiconductor devices are attractive for high-voltage, high-temperature and/or radiation resistant electronics. Ion-implantation is expected to have more impact in SiC technology due to extremely low diffusivity of dopants in SiC even at high temperatures. While nitrogen implanted junction rectifiers have been reported in 6H-SiC [1, 2] and phosphorus implanted junction rectifiers have been reported in 4H-SiC [3], there are few reports on the comparison of nitrogen and phosphorus implants and junction rectifiers on 4H-SiC[4][5]. In this paper, we report our study on nitrogen implanted high-voltage planar junction rectifiers and their comparison with phosphorus implanted devices in 4H-SiC. Devices were fabricated by varying the implantation species (N vs. P), post-implant anneal temperature (1200° and 1600°C) and junction termination extension (JTE) implant species (N vs. P). Breakdown voltage as high as 1300V has been obtained with a 10μm epitaxial layer.

2. Device Fabrication

The circular junction diodes (140μm diameter) were fabricated on commercial p/p^+, (0001), 8° off-axis 4H-SiC wafers . The thickness and doping of the epitaxial layer and the substrate are 10μm : 4×10^{15} cm^{-3} and 370μm : 1.4×10^{18} cm^{-3}, respectively. The n^+ layer was formed by implantation through a thin oxide layer at 650°C using nitrogen (dose: 3×10^{15} cm^{-2}) or phosphorus (dose: 4×10^{15} cm^{-2}). Junction termination extension was formed by implanting nitrogen (dose: 5×10^{13} cm^{-2}) or phosphorus (dose: 2×10^{13} cm^{-2}) in a similar process to the n^+ implantation. All the implants were annealed simultaneously in argon at 1200°C or 1600°C (Table 1). Samples NN1200 and PP1200 were annealed at 1200°C for 1 hr in argon whereas samples NN1600 and PP1600 were annealed at 1600°C for 10 min. Al/Ni/Al was used to contact the front and backside of the samples and annealed at 1000°C in argon for 2 min. Ti/Mo/Au was used as the final contacting metallization. A schematic of these devices is shown in Fig. 1.

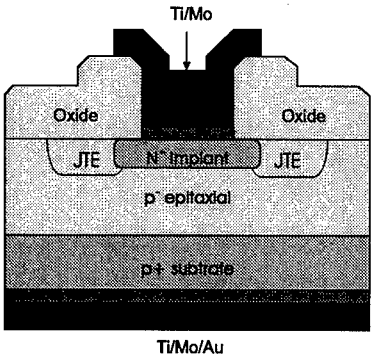

Figure 1: Crossection of fabricated n-type implanted planar junction rectifiers

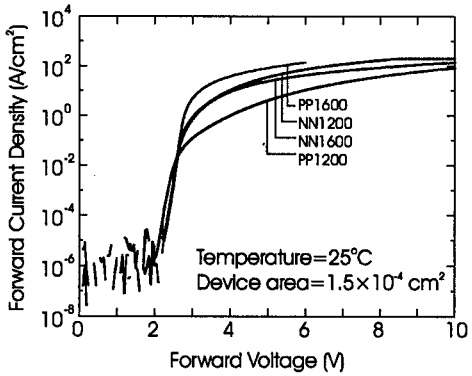

Figure 2: Forward characteristics of different implanted diodes at room temperature

Table 1: Measured parameters of fabricated junction rectifiers at room temperature.

Sample	N^+ Implant	JTE Implant	Implant Anneal	Breakdown Voltage	Leakage Current Density at 200V	Forward Drop at 100 A/cm^2	n	E_A
				(Volts)	(A/cm^2)	(Volts)		(eV)
NN1600	Nitrogen	Nitrogen	1600°C	350	5.21	8.7	1.83	1.76
NN1200	Nitrogen	Nitrogen	1200°C	1300	3.16	6.5	1.76	1.72
PP1600	Phosphorus	Phosphorus	1600°C	450	5.28	5.0	1.40	2.28
PP1200	Phosphorus	Phosphorus	1200°C	1100	6.88	10.7	1.89	1.55
PN1200	Phosphorus	Nitrogen	1200°C	900	3.88	-	-	-

3. Results and Discussion

Fig. 2 shows the forward log(J)-V characteristics for these diodes at room temperature. The phosphorus implanted diodes (PP1600) annealed at 1600°C exhibited a typical forward voltage drop of 5 V at 100 A/cm^2 as compared to 10.7 V obtained on diodes annealed at 1200°C . Though a significant portion of the voltage (~1.1 V) is dropped across the highly resistive p^+ substrate, the higher voltage drop in PP1200 diodes indicates insufficient conductivity modulation of the drift region. The forward voltage drop obtained on the PP1600 is comparable to the value obtained in [3]. The forward characteristics of the PP1600 show two distinct exponential regions, the first at low current levels, characterized by n~2 where conduction is controlled by the recombination via a single recombination level in accordance with the classic SNS model. The second region, at slightly higher current level, has an ideality factor of ~1.4 and current transport is controlled by recombination via multiple level as described by Khemka *et al.*[3]. The activation energy (E_A) in the second region is determined to be 2.28 eV, in agreement with the multiple level model.

On the other hand, nitrogen implanted diodes, (samples NN1200 and NN1600) showed a somewhat higher forward voltage drop of 6.5 V and 8.7 V, respectively. The ideality factor for both these diodes were ~1.8 with a thermal activation energy of 1.7 eV indicative of single level (SNS) recombination dominated current. Forward voltage drop on these diodes decreases with increase with temperature as indicated by the forward log(J)-V characteristics at 100°C in Figure 3. At 100 A/cm^2, diodes on samples NN1600 and PP1600 achieved a forward voltage drop of 6.5 and 4.4 V, respectively at 100°C . These results indicate that phosphorus n^+ implanations when activated at higher

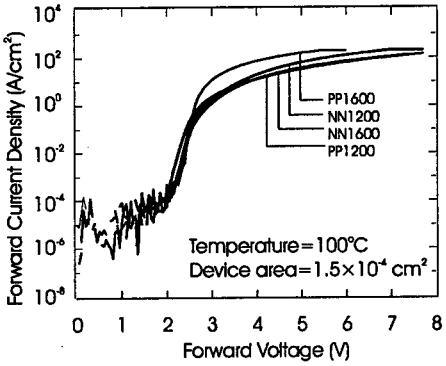

Figure 3: Forward characteristics of different implanted diodes at 100°C .

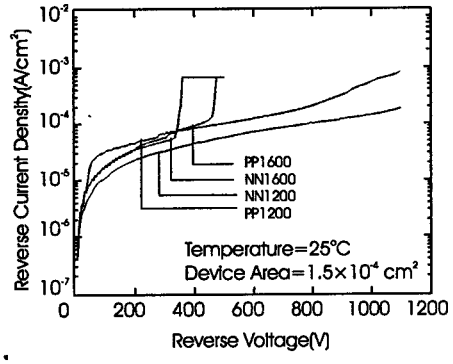

Figure 4: Reverse characteristics of different implanted diodes at room temperature.

temperature yields junction rectifiers with better forward characteristics.

The room temperature reverse characteristics is plotted for the diodes in Fig. 4. The PP1200 and NN1200 devices could block voltage in excess of 1100V with breakdown voltage reaching as high as 1300V on NN1200 devices. The breakdown voltage on the PP1200 device was facilitated by the damage-induced high resistivity of the termination implant whereas, on the NN1200 device, the high breakdown was due to proper JTE activation.

The blocking voltages of the diodes annealed at 1600°C were significantly lower (~350-450V). The low breakdown voltages in these diodes is due to the higher than optimum JTE dose due to the better activation at the 1600°C implantation anneal. The devices without JTE indicated a breakdown voltage of ~450 V on all the samples. Though the sample PP1600 exhibited a low forward voltage drop, the leakage current in these devices is high (5.28nA at 200V). The reverse leakage is seen to increase with an increase in temperature (Fig 5).The reverse leakage current was observed to vary as $I \propto V$ which is attributed to the resisitive leakage path due to the damage caused by the n^+ and JTE implantations around the periphery of the device.

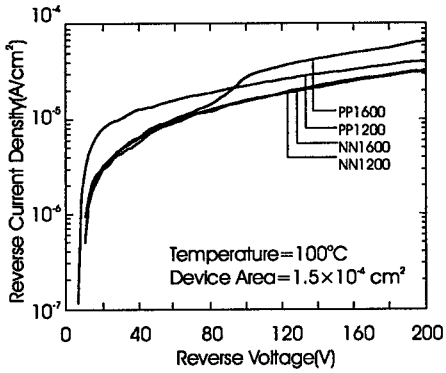

Figure 5: Reverse characteristics of different implanted diodes at 100°C .

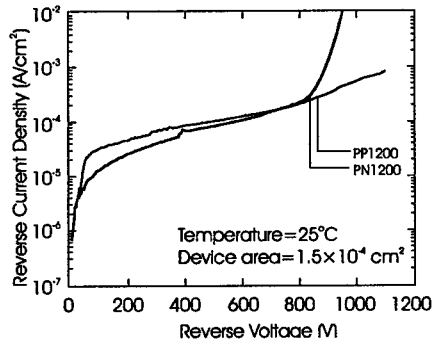

Figure 6: Reverse characteristics of phosphorus implanted diodes with nitrogen and phosphorus implanted JTE.

The high leakage current of the devices with the phosphorus implants is attributed to the damage

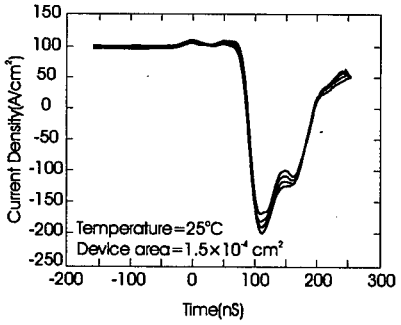

Figure 7: Reverse recovery switching transient for waveforms measured at room temperature.

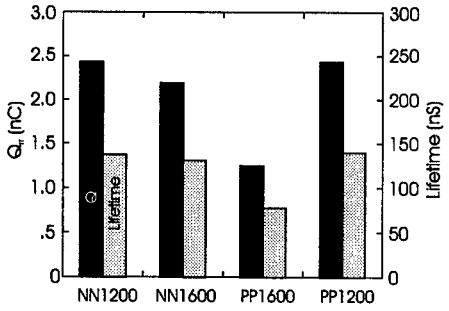

Figure 8: Histogram comparing the reverse recovery charge Q_{rr} and the high level lifetime (τ_h).

caused by the heavier phosphorus. This is supported by the lower leakage currents on sample PN1200 (with nitrogen JTE) compared to the sample PP1200 (phosphorus JTE) (Fig. 6).

Switching measurements were performed on the diodes using a custom built test circuit to extract the high level lifetime. The diodes were switched off from a on-state current density of 100 A/cm^2 with current ramp rate of 1×10^4A/cm^2.μs as indicated in Fig. 7. A snappy current recovery process is seen, typical of n^+ implanted junction rectifiers[6][7]. Extraction of lifetime using the algorithm presented in [8] indicated a typical lifetime of about 100 nS. This value is similar to other previously reported lifetime numbers on SiC implanted junction rectifiers [3]. No significant difference in the lifetime was observed in diodes on different samples as illustrated by Fig. 8. Typical value of the reverse recovery charge was ~1.5-2.5 nC.

4. Summary

High-voltage, planar junction rectifiers have been fabricated on 4H-SiC using nitrogen and phosphorus as n^+ implants. Phosphorus implanted diodes annealed at 1600°C exhibited the lowest on-state voltage drop of 5 V at 100 A/cm^2. Diodes annealed at 1200°C exhibited high breakdown voltage (~1300 V for sample NN1200), while the diodes annealed at 1600°C exhibited poor breakdown voltage (~350-450V). At low implant anneal temperature, the activation of nitrogen JTE is better than the phosphorus JTE. The leakage current density on the phosphorus implanted diodes exhibited high leakage current compared to the nitrogen implanted diodes due to the damage caused by the heavier phosphorus. Switching measurements were performed on these diodes and the reverse recovery charge and high level lifetime were extracted.

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Materials Science Forum Vols. 338-342 (2000) pp. 1335-1338

Dynamic and Steady-State Description of Incomplete Ionization in 4H-SiC Power Diodes under Turn-Off

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Keywords: Beyond SRH, Dynamic Trapping, Incomplete Ionization, Power Devices, SRH

Abstract. Transient simulations of a 4H-SiC 3kV p^+-n^--n^+ power diode have been performed using the drift-diffusion approximation. An additional equation has been added to describe the time evolution of the dopant gap level occupation. In this way, we accomplish a more general dynamic description of donor and acceptor occupation than the conventional steady-state model (i.e. merely including incomplete ionization in the case of relatively large ionization energies). The influence of variations in the donor and acceptor ionization energies has been studied as well as the effects of different sets of carrier capture coefficients characterizing these dopant levels. For the device under study (a pin diode), our calculations show that the turn-off process depends mainly on the donor energy position and less on the acceptor energy position. As a consequence, we show that a donor-type defect which is in the n-region and which is deeper than Nitrogen donor, can give rise to a turn-off behaviour which, for a proper description, needs the more accurate dynamic donor occupation model.

Introduction

In SiC the activation energy for dopants is rather large, resulting in a large amount of dopants not being ionized at room temperature (incomplete ionization). Therefore, it is expected that these dopants may give rise to a complex behaviour in the device, e.g., the turn-off process may be delayed due to a slow release of carriers, or the impact ionization process may be enhanced [1]. For these reasons it is important to get an insight into the behaviour of such dopants under switching. We have used the Medici program [2] to simulate the reverse recovery of a 4H-SiC 3kV power diode making use of two models: a general (dynamic) model which is an extension of the Shockley-Read-Hall (SRH) theory [3], and the conventional steady-state model (see more below). The physical models and parameters (*i.e.*, mobility models etc) in the simulation program for the 4H-SiC diode are the same as the ones used in Bakowski et al.[4].

Physical Models, Parameters and Device Description

The main idea of the dynamical model is to regard dopant atoms as electron or hole traps. This means that they can capture and emit electrons (or holes), depending on their positions in the band gap and on the values of the capture and emission coefficients. In the case of donors, the charge is zero if the traps are occupied, while it is positive after emitting one electron. Thus, one can write down an equation for the rate of change of the trapped charge concentration n_t with respect to time :

$$\frac{\partial n_t}{\partial t} = C_n(N_t - n_t)n - E_n n_t - C_p p n_t + E_p(N_t - n_t)\,. \qquad (1)$$

Here, N_t is the total concentration of traps, n is the electron concentration in the conduction band and p is the hole concentration in the valence band, C_n (C_p) denote the electron (hole) capture coefficients and E_n (E_p) the electron (hole) emission coefficients. The latter have been calculated at equilibrium (Shockley 1952 [3]) and are related to the capture coefficients.

Let us consider the steady state solution of Eq.1. We assume that the steady-state concentration for electrons and holes can be written as a Boltzmann distributions using the quasi-Fermi potentials. In the case of donors (*i.e.*, $C_p = E_p = 0$) this leads to the familiar Fermi-Dirac distribution function for the filled states:

$$n_t = N_t \left(1 + \frac{1}{g} e^{\frac{E_D - E_F}{kT}} \right)^{-1} . \qquad (2)$$

where g is the degeneracy factor, E_D and E_F are, respectively, the donor energy and the quasi-Fermi energy. This is the steady-state model, which is equivalent to the assumption that all the dopants are in steady-state at every stage of the transient. If, instead, the dopant atoms do not reach the steady state condition at once, we need to describe their time evolution making use of Eq. 1. This is achieved in the dynamical approach, which is a full generalization of the SRH model to transient conditions. In order to fully describe the process, the model also requires the carrier continuity equations:

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \bullet \mathbf{J}_n - n C_n (N_t - n_t) + E_n n_t + (G - R) . \qquad (3)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \bullet \mathbf{J}_p - p C_p n_t + E_p (N_t - n_t) + (G - R) . \qquad (4)$$

for electrons and holes, respectively, and the Poisson equation

$$\nabla \bullet \mathbf{E} = \frac{q}{\varepsilon} (p - n + N_t - n_t) . \qquad (5)$$

where J_n (J_p) is the electron (hole) flux, G (R) the rate of generation (recombination) of electron-hole pairs, $\boldsymbol{E}$ is the electric field and q and ε are the electron charge and the semiconductor permittivity respectively.

The different outcomes from the two models described above, i.e., the steady-state model and the dynamic model, have been studied. The simulations were carried out for a 4H-SiC p^+-n^--n^+ diode with dopant densities 10^{19}, 10^{15} and 10^{18} cm^{-3} and the widths 1.4, 31 and 270 μm, for the p^+, n^- and n^+ regions, respectively.

Three different kinds of dopants were alternatively used as acceptors in the p^+ region (anode), namely Al, Ga, and B. The acceptor ionization energies were assumed to be 0.191, 0.267 and 0.326 eV, respectively (these values have been chosen as representative for the large spectrum of values found in the literature [5]). In all cases, nitrogen has been used as a dopant in the n-type regions. The donor energy levels were set to 52 and 91.8 meV, since nitrogen shows two different donor levels [5]. The simulations have been carried out using three different values for the capture coefficients $C_p = C_n = 10^{-7}$, 10^{-9} and 10^{-11} $cm^3 s^{-1}$ [5,6], both for donors and for acceptors.

In the middle of the gap we placed a SRH recombination center having hole and electron lifetimes of 0.1 μs and 0.5 μs [7,8], respectively. Two different initial current densities (100 A/cm^2 and 1000 A/cm^2) have been studied. Initially, the diode is forward biased and then it is switched to a 800 volts reverse bias.

Simulation Results

When we change the acceptor energy from 0.191 eV to 0.326 eV, while keeping the N donor levels fixed, the two models give rise to the same transient behaviour, irrespective of which set of capture coefficients is used. In fact, the motion of the depletion edge in the n-region seems not to be affected by the rate of release of the trapped charge by the acceptors. Therefore the two models predict the same rate at which the carrier plasma is removed, and thus the same turn-off I/V characteristic and electric field evolution.

Next we will investigate what will happen if we in addition to the N donors have donor-like defects in the n-region with energies deeper into the band gap than N. In order to explore this situation, a new energy state has been added at 0.3 eV below the conduction band. The N concentration is now 30% of the total doping concentration, ensuring that the forward current of the device is not considerably reduced, and the deep donor concentration has been chosen to 70% of the total donor concentration. Moreover, the capture coefficients have been put equal to 10^{-11} cm^3s^{-1} with Al as the acceptor impurity on the p^+-side. In this case a faster recovery was obtained in the dynamic model (see Fig. 1).

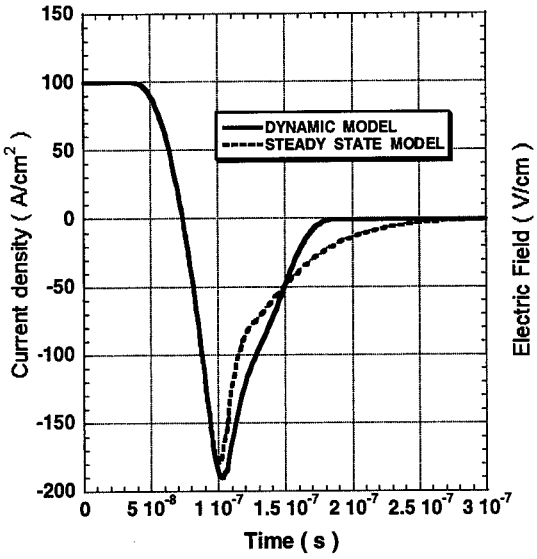

Fig. 1: Recovery curve for a donor energy at $E_D = 0.3$ eV and Al as acceptor

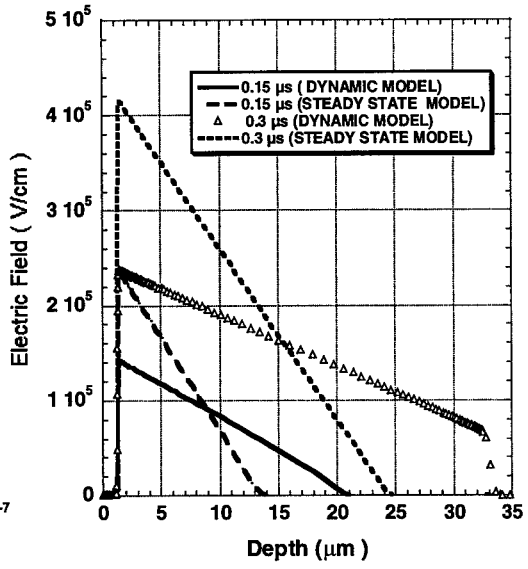

Fig. 2: Profiles of the electric field (same case as in Fig. 1)

The electric field profiles at t = 0.15 µs and t = 0.3 µs are shown in Fig. 2. As one can see, according to the dynamic model the depletion region edge is moving at a higher speed compared to the steady-state case. When the reverse recovery time (i.e. the time needed to turn off the current in the device) is shorter than the time needed for the donors to emit their electrons (as measured by the inverse of the donor emission rate), the trapped charge in the depletion region gives rise to an effective doping, which is lower than in the steady-state case. Due to this lower doping, the depletion region on the n-side becomes larger (see Fig.2) than in the steady-state model. Therefore, in the dynamic model the carrier plasma is removed faster, and, as a result, a different (faster) recovery occurs. In the case that the emission coefficient is high relative to the reverse recovery

time, the donors are fast enough to follow the recovery curve, and both models predict approximately the same result. In particular, we have found that for a capture coefficient of 10^{-11} cm^3s^{-1} the electrons are trapped in the donor states, as can be clearly seen in Fig. 3 for t = 0.3 μs, while for a value of 10^{-7} cm^3s^{-1} they follow indeed the recovery curve.

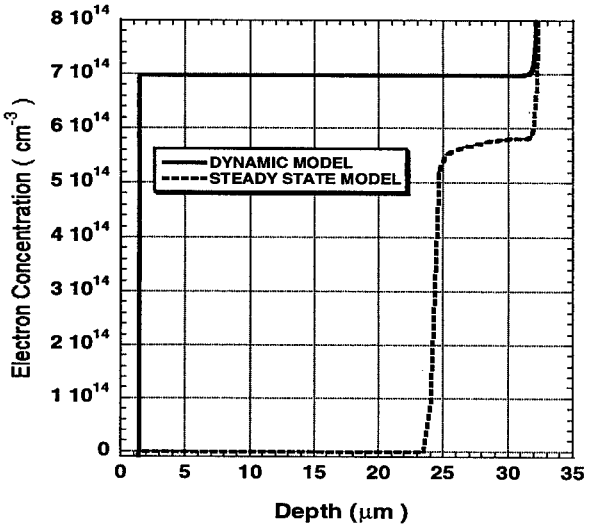

Fig. 3: Electron occupation in the 0.3 eV donor level at t = 0.3 μs.

Then we can conclude that the dynamic model and the steady-state model are equivalent in the description of the particular *ideal* diode investigated, irrespective of the choice of acceptor dopants in the p^+ region considered here, the set of capture coefficients, and the current densities at which the recovery starts. But it has also been demonstrated that a donor-like defect which is deeper than N (e.g., at 0.3 eV below the conduction band) and which has suitable electron capture properties, can give rise to a turn-off behaviour which is not well-described by the steady-state model, but which requires the more accurate dynamic model used here.

Furthermore, according to the steady-state model, the maximum value of the electric field in the depletion zone is twice as large as in the dynamic case. This can obviously have direct importance for the modelling of avalanche: in this case the steady-state model could have predicted avalanche break-down, while the more accurate dynamic model would not.

Acknowledgement
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Simulation and Fabrication of High-Voltage 4H-SiC Diodes with Multiple Floating Guard Ring Termination

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Keywords: Breakdown, Diode, Edge Termination, Guard Rings, MEDICI, Simulation

Abstract: In this work, we have demonstrated the use of a commercial simulation package to design and predict the breakdown of SiC diodes with multiple floating guard ring termination. The accuracy and predictability of the simulations were verified with the fabrication of 4H-SiC Schottky and aluminum implanted pn diodes using floating guard ring termination. The measured breakdown voltages, ranging from 580V with no termination to over 1300V with four floating rings, showed excellent correlation to initial simulation predictions.

I. Introduction

Silicon Carbide has received a substantial increase in research interest over the past few years as a base material system for future high-power semiconductor devices. 4H-SiC is particularly attractive for power devices due to its wide band gap, high mobility, excellent thermal conductivity, and high critical field strength. Because of their simple structure and potential system performance increase, SiC pn and Schottky diodes are rapidly becoming a commercially viable technology. Several researchers have shown the potential for high-voltage SiC pn and Schottky diodes with significantly reduced on-resistance and switching times compared to Si devices [1,2], and will result in increased system switching speed and reduced power loss.

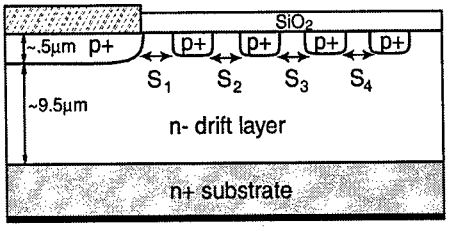

Fig. 1: Schematic of an implanted pn diode with guard ring termination.

As with Si technology, edge termination for SiC power devices is a critical design issue to achieve maximum breakdown voltage and thus optimum on-resistance. Several different edge termination methods for pn junction termination have been investigated; field plate extensions, junction termination extensions (JTE), and high-resistivity implanted layers. These methods either require additional processing steps, or have unresolved reliability issues. The floating guard ring structure (Fig. 1) is a proven edge termination method in high-voltage silicon technology, but has not been investigated thoroughly as a technique for SiC power device termination. This is most likely due to the difficulty of floating guard ring design and the shortcomings in using silicon based simulation tools for SiC device design. In order to investigate floating guard ring structures for SiC devices, we have used the MEDICI simulator [3] to develop an optimum SiC four guard ring design, and have fabricated SiC Schottky and implanted pn diodes with floating guard ring termination to verify our approach.

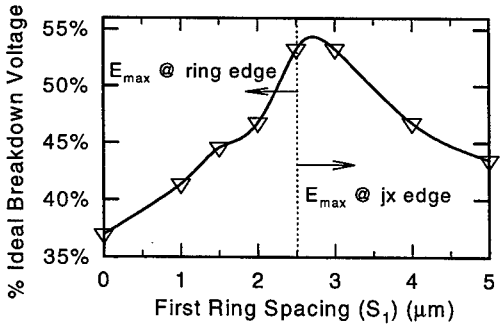

Fig. 2: Simulated increase in breakdown voltage as a function of the first guard ring spacing.

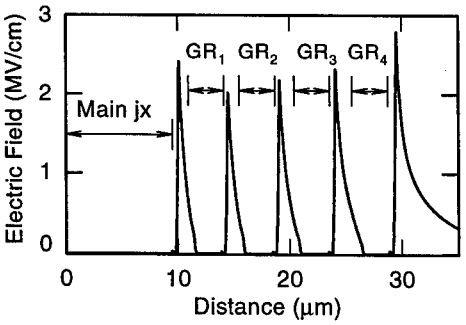

Fig. 3: Simulated electric field profile for an optimized four guard ring structure (V_A=1200V).

II. Simulations

Numerical simulations with floating structures are extremely complex, with results being strongly coupled to solution method and grid conditioning [4]. To accurately simulate the breakdown of a circular junction with floating junctions, the simulator must be able to solve for the independent quasi-Fermi potentials of the floating rings as they are allowed to vary with the surrounding potential distribution. In addition, the 3-dimensional field crowding effects at junction edges can play a significant role in the determination of the junction breakdown voltage and must be included for accurate results. To include these effects in the design of our guard ring structures, we have used the MEDICI simulator to predict the breakdown of SiC pn junctions with floating guard rings. Simulations involved solutions to Poisson's equation and both carrier continuity equations, with impact ionization coefficients extracted from the most recent experimental results in the literature [5].

To determine optimum guard ring spacing, the simulations involved an iterative process by which a single ring was optimized, then additional rings added, and re-optimized. Fig. 2 illustrates the dependence of the breakdown voltage on the spacing for a single guard ring. For a single ring, the optimum junction-to-ring spacing (S_1) to maintain the peak electric field at the guard ring is 2.5μm. An increase in S_1 shifts the peak field to the edge of the main junction, resulting in a lower breakdown voltage. If S_1 is decreased, the peak electric field is still maintained at the ring edge, but the electric field shielding effect is diminished and the breakdown voltage is lowered. For all simulations, the electric field was examined to determine maximum breakdown while maintaining the peak electric field at the outermost ring. The potential and electric field distributions of an optimized four-ring structure are shown in Fig. 3 and Fig. 4, respectively. The optimized profile corresponds to a 10μm epitaxial layer with N_D=1x10$^{15}cm^{-3}$, S_1=1.5μm, S_2=1.5μm, S_3=2μm, and S_4=2.5μm. These simulations predict a breakdown voltage of 85% of the ideal 1-D parallel-plane breakdown (1600V) for this structure with four optimized rings.

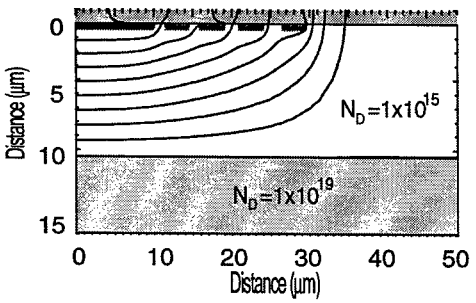

Fig. 4: Simulated potential contours for an optimized four guard ring structure.

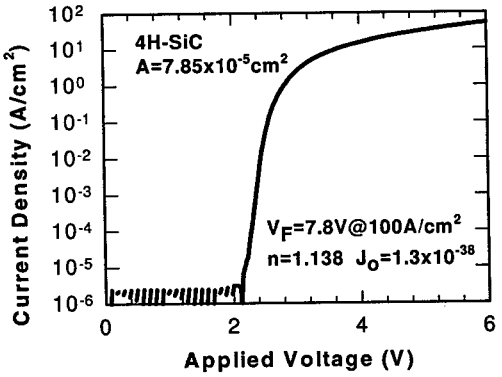

Fig. 5: Typical forward I-V characteristics of an aluminum implanted 4H-SiC pn diode with AlTi ohmic contacts.

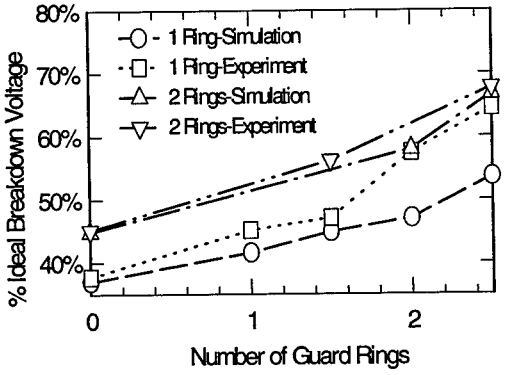

Fig. 6: Simulated and measured breakdown of diodes with 1 and 2 guard rings, with outermost ring spacing as a variable.

III. Fabrication

To verify our simulations, implanted pn diodes were fabricated on high quality n^+ Cree wafers. The n-type epi-layers were grown at Auburn University by chemical vapor deposition at 1500°C on 5mm x 5mm square pieces of n^+-doped 8° off-axis 4H-SiC substrates obtained from Cree Research Inc. The thickness of the epi-layers was approximately 10μm with a carrier concentration of $5x10^{15}$ cm^{-3} obtained by CV profiling. The p^+ main junction and guard rings were formed by multiple Al implants ranging from 50keV-260keV at 700°C. Selective area implantation was performed through a Mo mask patterned by a liftoff procedure. Implant activation and damage annealing was performed at 1700°C for 10min. After implant activation, the samples were cleaned, a short surface RIE was performed to remove any remaining residue, and a high-quality thermal oxide was grown as a passivation layer. Circular p-type ohmic contact areas were opened with a BOE through a window created by standard lithography. A thin layer of AlTi was then sputtered and patterned by liftoff prior to the contact anneal at 1050°C for 2 min. Ti Schottky contacts were formed with the same liftoff procedure, with an additional 5 minute in-situ ion-gun clean before Ti evaporation.

V. Experimental Results

A typical forward current-voltage characteristic for a 100μm aluminum implanted pn diode is shown in Fig. 5. The forward voltage drop was measured to be 7.8V at $100A/cm^2$. The relatively high on-resistance is due to an insufficient aluminum activation anneal and consequently high p-type ohmic contact resistance. As predicted by simulation, the experimental results for the diodes with implanted guard rings showed a significant improvement in breakdown voltage over those without edge termination. Measurements were made using a Tektronix 371 curve tracer in conjunction with a HP Picoammeter, with the samples immersed in a

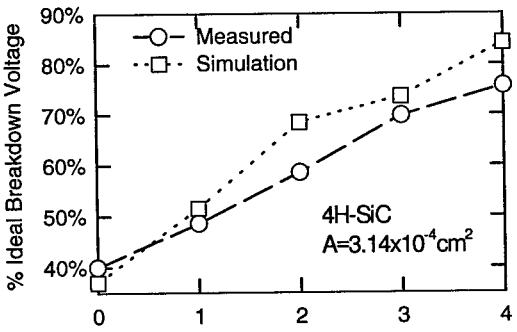

Fig. 7: The correlation between measured and simulated breakdown voltages for pn diodes with an increasing number of floating guard rings.

Flourinert™ solution. Fig. 6 shows the simulated and measured breakdown voltage for 100μm diodes with one and two guard rings, with the outermost guard ring spacing as the independent variable. It is clearly seen that the exact guard ring spacing can have a large effect on the measured breakdown value.

Fig. 7 shows the simulated and measured improvement in breakdown voltage for an increasing number of guard-rings, with the measured breakdown voltage normalized to the ideal parallel plane value. Diodes with 200μm diameter exhibited an increase in breakdown voltage from an average of 580V with no termination, to over 1200V with four optimized guard rings. The largest measured breakdown voltage, plotted in Fig. 8, was over 1300V for a 100μm diode with multiple guard rings. Breakdown was not catastrophic for the diodes tested, but a certain degree of breakdown walkout was observed on diodes with multiple guard rings. We believe this could be due to a charging of the oxide at the high electric field peaks near the guard ring edges, thus causing an increased spreading of the depletion layer.

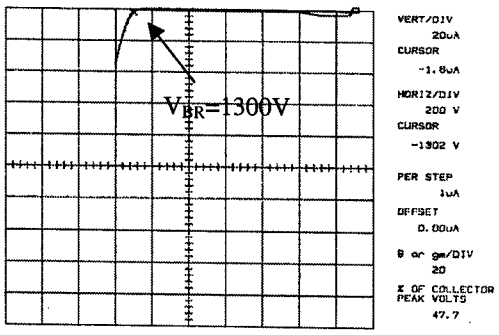

Fig. 8: Output plot of a Textronix 371 curve tracer showing the reverse breakdown characteristics for a 100μm SiC pn diode.

VI. Summary

High-voltage SiC Schottky and implanted pn diodes with multiple floating guard ring termination, designed by numerical simulation, were successfully fabricated with breakdown values in excess of 1300V. The ability to include multiple floating guard rings into a wide range of power devices with little or no additional process steps, makes this method of edge termination very attractive for SiC devices. The good agreement between the simulation results and the measured improvement in breakdown voltages of both pn and Schottky SiC diodes demonstrates the feasibility of floating guard ring predictive simulation and design of SiC edge termination.

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Transient Characterization of SiC P-N Diode

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Keywords: Buck-Converter, Hard Switching, p-n Diodes, Reliability, ZVS Switching

ABSTRACT: Silicon carbide is emerging as a superior material for semiconductor devices for applications that require high power operation at high temperature, radiation and chemically harsh environments. Besides the material properties of wide band-gap, high breakdown electric field, good thermal conductivity and carrier saturation velocity, SiC devices have been observed to display other useful properties that make them suitable for high current applications. This is especially true for bipolar devices where SiC can be used at high frequencies prohibited for silicon devices by large carrier storage and the consequent switching losses. SiC p-n diodes display a much reduced reverse recovery charge than silicon p-n diodes. Only a slight variation with forward current and temperature further improve their advantages. From this standpoint, the performance of the SiC diodes in applications that subject them to transient stresses must be studied.

INTRODUCTION:

Silicon carbide is being viewed as a potential material for use in high voltage and high current applications for harsh environments. Ordinary silicon devices fail to perform in their desired mode of operation under such conditions. Silicon carbide has the advantages of wide band-gap, high breakdown electric field, thermal conductivity and high electron saturation velocity besides being mechanically the second hardest substance. SiC devices have also been known to be better than silicon devices for high frequency operation. This is primarily due to their high electron saturation velocity, electrical and thermal conductivity, which gives a high frequency-power product [4]. For high power applications, positive temperature coefficient of breakdown voltage is necessary to withstand instantaneous glitches in applied voltage. Numerous reports on negative temperature coefficient of SiC breakdown are only recently being refuted by reports on positive coefficient [1,2]. Abnormal behavior in breakdown performance of the defective devices is observed in static as well as transient conditions. It has been observed that premature device breakdown may occur under high-speed pulse testing [3]. Such behavior is undesirable since diodes in power electronic circuits frequently experience rapid changes in voltage and current. Considering the above-mentioned performance of SiC devices, there is a need to evaluate the device performance not only individually but also at a system level. This paper reports such a study conducted on 4H-SiC p-n diodes used in switching power converters. Hard switching and ZVS topologies for a simple buck converter were utilized to test the operation of the SiC diodes. A reliability issue regarding use of SiC devices in stressful switching applications was identified. Silicon carbide (4H-SiC) P-N diodes fabricated at the NASA Glenn Research Center were used in this study. The mesa-type diodes were of square cross section and had dimensions of 0.09 cm x 0.09 cm as shown in Fig. 1.

The detailed structure of the diodes and the extraction procedure used is described elsewhere [5, 6]. The drift region doping extracted from C-V measurements (10 kHz to 1 MHz) corresponded to an ideal breakdown voltage around 100 V. The observed breakdown around 65 V was attributed to presence of closed core screw dislocations in the diode structure [4]. The diode was current rated based on the forward current measured for a forward voltage drop of 5 V. Accordingly the diode was rated at 1 A.

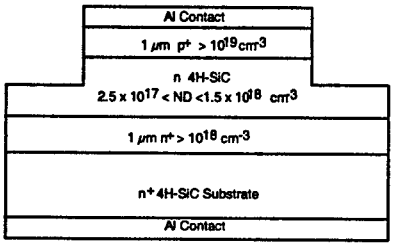

Fig. 1 Structure of the diodes under test

Transient measurements:

The diode described above was tested in simple buck DC-DC converter as a current freewheeling diode. The main purpose of this characterization was to evaluate the performance of the diode in a switched application as compared to a commercially used silicon device. Effects of hard switching and resonant zero voltage switching (ZVS) of the main switching device on the freewheeling diode were also studied. The two circuits are shown in Fig. 2 and Fig. 3 respectively.

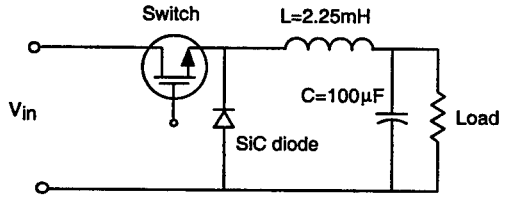

Fig. 2 Hard switching buck converter

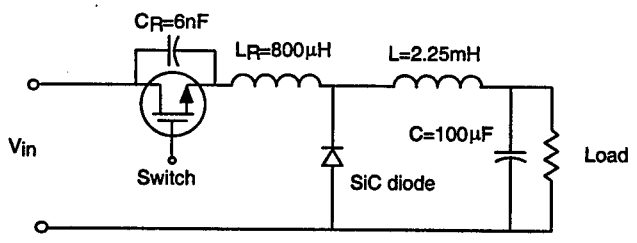

Fig. 3 ZVS switching buck converter

The detailed operation of these circuits is given in [7]. In the hard switching buck converter, the switch turns on with the diode conducting the freewheeling inductor current. This subjects the diode to a reverse recovery stress, every time the main switch is turned on. The severity of this stress depends upon the current level at which the converter is operating and the input voltage V_{in}. The ZVS topology is usually associated with a high current stress for the diode during the circuit

resonance but the reverse recovery stress is greatly reduced. Thus the two circuits impose different stresses on the diode.

Table 1. SiC diode hard switching measurements at 50°C

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Vdiode(on) (V)	Power loss Diode (W)	Rout (Ω)
50.7	0.15	28.75	0.23	4.5	0.6	125
50.8	0.176	28.4	0.28	5.0	0.75	100
50.9	0.225	28.13	0.37	5.2	0.93	75

Table 2. SiC diode hard switching measurements at 100°C

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Vdiode(on) (V)	Power loss Diode (W)	Rout (Ω)
60.2	0.3	34.64	0.462	5.3	1.41	125
60.5	0.23	34.81	0.348	5.2	1.138	100
60.4	0.19	35.33	0.283	5.1	1.02	75

Table 3. SiC diode zero voltage switching measurements at 50°C

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Vdiode(on) (V)	Power loss Diode (W)	Rout (Ω)
50.2	0.097	20.68	0.165	4.4	0.48	125
50.2	0.106	18.24	0.182	4.6	0.52	100
50.4	0.111	16.04	0.214	4.6	0.56	75

Table 4. SiC diode zero voltage switching measurements at 100°C

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Vdiode(on) (V)	Power loss Diode (W)	Rout (Ω)
50.2	0.096	20.5	0.164	4.4	0.5	125
50.1	0.103	18.25	0.182	4.6	0.52	100
50.1	0.105	15.79	0.21	4.7	0.65	75

For the actual measurements, the switch was driven by a square wave at a frequency of 54 kHz with a duty cycle of 60%. Performance of the converter was observed for variations in the load resistance, input voltage and temperature. The results are tabulated in the Tables 1-4.

Discussion and results:

The diode was known to have a very negligible reverse recovery transient [6]. As expected the switching losses were negligibly small as compared to the conduction power loss. This was primarily due to the high value of the on-state voltage drop across the diode. The diode resistance also was observed to play a conspicuous role from the increase of the diode drop with current. This also reflected on the power loss of the diode, which increased noticeably with increasing current. Earlier static I-V and reverse recovery measurements on this diode [6] had suggested a dominant recombination current rather than diffusion current, through the diode. Thus increase in the minority carrier lifetime with temperature led to increase in the measured diode power loss. This was much more prominent in the hard-switching converter.

The reverse recovery measurements described in [6] that were performed on this diode had the diode undergoing reverse recovery at a very low frequency around 500 Hz. At currents lower than half the rated current, the reliability of the diode was not a concern. However from the observations of the diode behavior in the converter operating at 50 kHz show that such might not be the case at higher frequencies. After operating the diode in the hard switching converter at around 0.5 A output current (and hence peak diode current), the diode suddenly stopped conducting in the forward direction for forward voltages as much as 25 V. The diode however showed the reverse I-V curve similar to the one observed before the converter testing was done. Furthermore after the diode was reverse biased with a reverse current greater than about 50 μA, it showed a small current in forward direction which decayed rapidly with time. This forward current tendency was observable later for larger reverse currents only. Finally the diode did not conduct at all in the forward direction at all even after reverse biasing it for larger currents and longer times. This phenomenon could be due to presence of trap levels in the drift region of the diode which get filled up in the forward bias and empty under reverse bias conditions.

Conclusion:

A 4-H SiC diode was tested in a simple buck converter with hard switching and zero voltage switching topologies. The diode was observed to have negligible switching power loss due to a smaller reverse recovery waveform. The power loss in the diode was instead dominated by the conduction power loss due to high on-state voltage drop. A distinct increase in power loss with increasing diode current as well as increasing temperature is observed. For hard switching operation at higher switching frequencies, the diode reliability is jeopardized. This is reflected as a loss of diode conduction in the forward conduction. The exact reason for this was not known but could be attributed to filling up and emptying of trap levels in the drift region.

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Formation of Deep pn Junctions by MeV Al- and B-ion Implantations into 4H-SiC and Reverse Characteristics

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Keywords: Electrical Activation, Ion Implantation, pn Junction Diode

Abstract: To form deep ($\geq 2\mu$m) p-well regions for several-kV SiC power devices, MeV ion implantation of Al and B into 4H-SiC has been systematically investigated. The 3μm-deep box profiles were formed through MeV Al^+- and B^+-implantation, and the electrical activation was investigated. The activation ratio of Al was larger than that of B, and each activation ratio was improved with C^+ co-implantaion. Pn junction diodes were fabricated by MeV Al^+- and B^+-implantations. The B^+-implanted diodes showed better reverse characteristics than the Al^+-implanted diodes.

1 Introduction

Silicon carbide (SiC) is an attractive semiconductor for high-power and high-temperature devices because of its wide bandgap, high breakdown field and high thermal conductivity. As selective doping techniques, ion implantation and diffusion techniques are generally used in Si device processes. In the case of SiC, the diffusion coefficients of impurities are very low, and so high temperature (more than 1800 ℃) is required to use a diffusion technique for SiC. But there is no proper material as a diffusion mask to resist such a high temperature. Therefore, ion implantation is a key technology as selective doping for SiC.

To realize several-kV (or higher) SiC power devices such as vertical DIMOSFETs and IGBTs, the formation of deep ($\geq 2\mu$m) p-well regions becomes a critical issue. For this purpose, high-energy (MeV) Al- and B-ion implantations will be the most promising approach, on which very few investigations have been reported. In this paper, MeV ion implantation of Al and B into 4H-SiC is systematically investigated. Because of the present motivation, we focus on the electrical activation of implanted ions and the reverse characteristics of fabricated pn junctions.

2 Experiments

N-type 4H-SiC epilayers with a donor concentration of $7\sim10\times10^{14}$cm^{-3} grown at the authors' group were used in this study. Al or B ions were implanted at room temperature. Post-implantation annealing was performed at 1500~1600°C for 30min in Ar ambience.

Pn junction diodes were fabricated by implantation of Al, B to n-type epilayers (13μm, 8×10^{14}cm^{-3}). The profile of ion implantation was a 3μm-deep box profile and the total doses of Al, B were 1.0×10^{14}cm^{-2} and 3.0×10^{14}cm^{-2}, respectively. The annealing temperature and time were 1600 ℃ and 30min. The structure of diodes was mesa-shaped which was formed by

Reactive Ion Etching (RIE). The diodes had SiO_2 (about 50nm) for passivation and Al/Ti and Ni electrodes for p- and n-type layers (alloyed at 800 ℃).

3 Results and discussion

3.1 Electrical activation

To design deep box profiles, the projected range (R_p) and straggle (ΔR_p) of MeV Al^+ implantation for SiC, systematic data of which had not been available, were obtained through single-energy implantations and subsequent SIMS measurements. Figure 1 shows the R_p and ΔR_p for various implantation energies (E). In fitting these data, the following equations were obtained.

$$R_p = 0.31E + 0.73\exp(-0.30/E) \quad [\mu m], \tag{1}$$

$$\Delta R_p = 0.13\exp(-0.61/E) + 0.048 \quad [\mu m]. \tag{2}$$

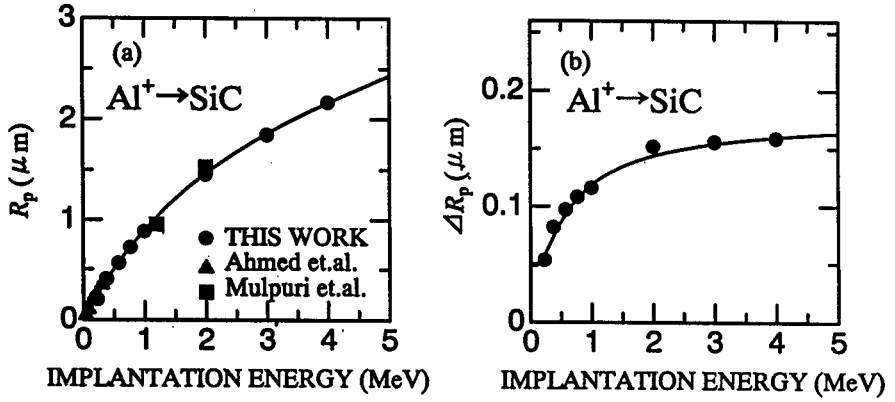


Fig.1 Al^+ implantation for (a) projected range (R_p) and (b) straggle (ΔR_p).

Based on these basic data, we succeeded in the formation of 3μm-deep box profiles with Al^+ (50keV~6.2MeV) implantation. For B^+ implantation, it is reported that the actual profiles differ only 10% from TRIM simulation [1]. The 3μm-deep box profiles with B^+ (30keV~3.4MeV) implantation were designed by using TRIM. The total dose of $3.0\times10^{14}cm^{-2}$ resulted in the average Al or B atom concentration of $1.0\times10^{18}cm^{-3}$. To enhance the electrical activation, "co-implantation" of C^+ [2] was also investigated.

The net acceptor concentration was determined from C-V measurements for a Ni(as-depo.)/SiC Schottky structure formed on the implanted layer. Table 1 summarizes the electrical activation ratios for different implantation and annealing conditions. For Al^+ implantation, an electrical activation ratio of 32% was obtained by annealing at 1600°C, and was improved up to 46% by C^+ co-implantation. In the case of B^+ implantation, the electrical activation was greatly improved by C^+ co-implantation. However, the activation ratio was still low, approximately 10%, making the B^+-implanted layers more resistive compared to the Al^+-implanted layers.

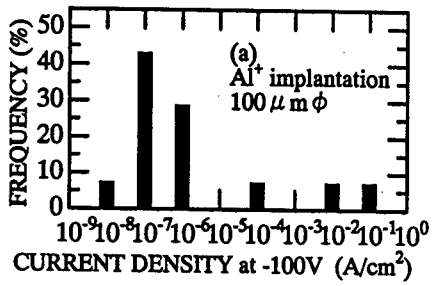
Table.1 The condition of ion implantation and annealing, and the electrical activation ratio.

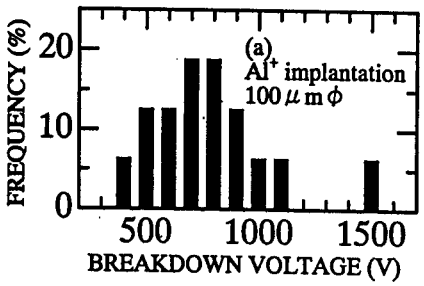
Al^+ dose (cm^{-2})	C^+ dose (cm^{-2})	T_{anneal}	N_a-N_d (cm^{-3})	activation ratio	effect of co-impla
$3.0x10^{14}$	—	1500℃	$< 5x10^{14}$	< 0.1%	—
$3.0x10^{14}$	—	1600℃	$3.2x10^{17}$	32%	—
$3.0x10^{14}$	$1.5x10^{14}$	1600℃	$4.6x10^{17}$	46%	x1.5
$3.0x10^{14}$	$3.0x10^{14}$	1600℃	$4.5x10^{17}$	45%	x1.5
B^+ dose (cm^{-2})	C^+ dose (cm^{-2})	T_{anneal}	N_a-N_d (cm^{-3})	activation ratio	effect of co-impla
$3.0x10^{14}$	—	1500℃	$2.7x10^{16}$	2.7%	—
$3.0x10^{14}$	—	1600℃	$2.2x10^{16}$	2.2%	—
$3.0x10^{14}$	$1.5x10^{14}$	1500℃	$4.2x10^{16}$	4.2%	x1.6
$3.0x10^{14}$	$1.5x10^{14}$	1600℃	$1.0x10^{17}$	10%	x4.5
$3.0x10^{14}$	$3.0x10^{14}$	1500℃	$9.8x10^{16}$	9.8%	x3.6
$3.0x10^{14}$	$3.0x10^{14}$	1600℃	$9.8x10^{16}$	9.8%	x4.5

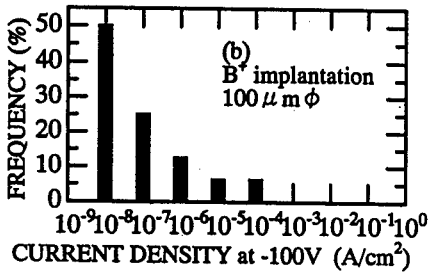
3.2 pn junction diodes

The 3μm-deep pn junction was formed through MeV Al^+- and B^+-implantations into 13μm thick n-type 4H-SiC epilayers with an implanted impurity concentration of $3\sim10\times10^{17}cm^{-3}$. After annealing at 1600°C, samples were processed into mesa structures with SiO_2 passivation. Detailed *C-V* analyses of the diodes revealed the existence of "*i*-layers" at the junction interface. The *i*-layer was thicker for B^+-implanted junctions (0.5μm) than for Al^+-implanted junctions (0.1μm), probably due to the pronounced in-diffusion of B atoms.

A few tens of 100$\mu m\phi$ diodes without visible surface defects were selected for each implantation condition, and were tested under a high-voltage reverse-biased condition, which is crucial for DIMOSFET blocking performance. Figure 2 shows the histograms of leakage current density at -100V for (a) Al^+- and (b) B^+-implanted diodes, demonstrating that B^+-implanted diodes exhibit much lower leakage with tight distribution. Although the maximum breakdown voltage obtained exceeded 1500V, regardless of implanted species, B^+-implanted diodes showed significantly higher breakdown voltages as shown in Fig.3. The average breakdown voltage was 830V for Al^+- and 1230V for B^+-implanted diodes, suggesting a large difference which cannot be explained by the difference in the *i*-layer thickness mentioned above. From preliminary Isothermal Capacitance Transient Spectroscopy (ICTS) measurements, concentrations of deep levels were $10^{13}cm^{-3}$ and $10^{12}cm^{-3}$ for Al^+-, B^+-implanted diodes, respectively. So, MeV Al^+ implantation at room temperature may introduce more traps and some kind of harmful defects near the junction interface. Though C^+ co-implanted diodes for Al^+-, B^+-implantations were also investigated, the impact of C^+ co-implantation on diode performance was very small. Thus, B^+ implantation is preferable to form deep junctions (or p-well) with a high blocking voltage.







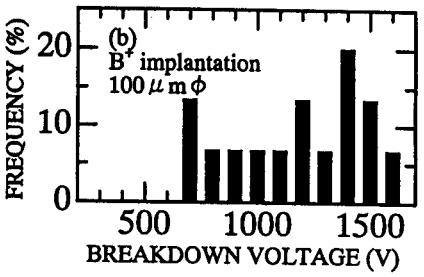


Fig.2 Histograms of leakage curernt density at -100V for (a) Al^+- and (b)B^+-implanted diodes.

Fig.3 Histograms of breakdown voltage for (a)Al^+- and (b)B^+-implanted diodes.

4 Conclusion

MeV Al^+- and B^+-implantation into 4H-SiC epilayers has been investigated. The implantation-energy dependence of the projected range and straggle were established for MeV Al^+ implantation. In 1600 ℃ annealing, the activation ratio of implanted species was 32% and 2.2% for Al^+- and B^+-implantations, respectively. With C^+ co-implantation, the Al activation ratio was improved up to 46%, which was 1.5 times larger than without C^+ co-implantation, and the B activation ratio was 10%, which was 5 times larger than without co-implantation. The B^+-implanted diodes had the smaller leakage current density than Al^+-implanted diodes. The maximum breakdown voltage was more than 1500V in both Al^+-, B^+-implanted diodes, but the average breakdown voltage of B^+-implanted diodes was higher than Al^+-implanted diodes. Deep level concentrations of deep were $10^{13}cm^{-3}$ and $10^{12}cm^{-3}$ for Al^+- and B^+-implanted diodes, respectively, indicating that the damage by ion implantation is smaller in MeV B^+ implantation than MeV Al^+ implantation.

Acknowledgement

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Defect Modeling and Simulation of 4-H SiC P-N Diode

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Keywords: 2-D Simulations, "Defect" Diode, Forward I-V Characteristics, Modeling, p-n Diodes

Abstract: Silicon carbide is seen as a potent material for high power, high temperature and harsh environment applications. However the commercial use of SiC devices is greatly restricted by the immature process technology and wafer quality deficiencies. While the most degrading micropipe defects have been significantly reduced in number, other defect types like the closed core screw dislocations continue to contaminate SiC devices in large quantities. The effects of these defects on the quality and performance of SiC devices is under study. This paper models the presence of embedded structural defects in SiC PN junction diodes. The defects are presented as parallel diodes to the "ideal" ones with areas correspondingly reduced. "Defect" diodes are shown to turn on earlier to the "ideal" ones giving an anomalous bump in the initial part of forward I-V curves.

I. Introduction: Silicon carbide semiconductor electronic devices are being developed for extreme conditions of high temperature, high power and/or high radiation where ordinary silicon based semiconductor devices fail to perform in their desired operational mode. With all its advantages, the extensive use of SiC is limited by the underdeveloped crystal growth and device fabrication technology. Processed SiC wafers contain too many structural defects to be used successfully in many applications, especially those requiring both high currents and voltages. The commonly observed and most harmful micropipe defects have been reduced to a typical value of a few hundreds per square cm with values less than 30/ cm^2 being marketed commercially. By and large, micropipes are expected to be sufficiently reduced within the next few years. The more densely (but not as easily) observed defects are the closed core screw dislocation defects that are in the order of 5000-10,000 per square cm [1]. While not nearly as detrimental to device performance as micropipes, the operational impact of these defects in various devices and circuits is not clearly known. It is the attempt of this paper to characterize and model 4H-SiC P-N diodes with localized structural defects such as open and closed core screw dislocations and 3-C epilayer inclusions. A reasonably accurate approximation is proposed in which the defect is modeled as a separate smaller area "defect" diode parallel to the "ideal" one. An overall diode model ("ideal" and "defect" diodes combined) is arrived at after extensive static characterization. The "ideal" and "defect" diodes are simulated in a 2D finite element simulator and the combined static characteristics matched with the measured ones. It is shown that the defects can indeed be modeled to the first order as very small area diodes parallel diodes to the "ideal" one and having varying physical and material properties depending upon the defect type. While the defect types are not firmly identified physically, the reflections of the presence of these "defect" diodes are shown in the electrical characteristics of the total structure.

II. Diode Structure and Static Measurements: Silicon Carbide diodes (4H-SiC) fabricated by the NASA Lewis Lab were used for study. The diodes were of square cross-section and had dimensions of 0.09 cm x 0.09 cm. The mesa-type diodes had a drift region of width 4μm and the doping density 6e17 cm^{-3}. Aluminum contacts were provided at the anode and cathode. The detailed structure and fabrication is described elsewhere [1, 9]. Doping of the drift region was extracted from measured C-V characteristics. Static characterization for I-V curves was done using a series resistance setup with an accurate voltage source. For higher voltage levels, a high power Sony-Tektronix curve tracer 371A was used. High frequency (10kHz to 1MHz) capacitance measurements were performed using a typical setup with an HP L-C-R meter. Variations in the static characteristics with temperature were studied using a hot plate.

The "ideal" breakdown voltage for tested devices was estimated to be of the order of 100V from the extracted dopings. Presence of defects is known to have a degrading effect on breakdown voltage [1]. Thus checking for non-idealities in the breakdown voltage or reverse I-V curves was used as a primary means for determining the integrity of the diodes. The measurements showed a maximum breakdown voltage of 83V and a minimum of 30V. The reverse I-V curves are discussed in more detail elsewhere [8]. Diodes showing breakdown voltages above 60V were chosen for further analysis and the rest of them discarded as not operational.

The extracted drift region doping from measured C-V curves comes out to be about 6e17/cm^3. Since C-V curves are expected to be the least affected by small-area defects, they would give an accurate picture of the "ideal" diode regions and doping. I-V curves would represent the presence of defects to a high degree of sensitivity, the forward current being exponentially dependent on voltage. The measured curves are shown in Fig. 1. Two distinct types of forward I-V curves were observed:

In the first one, the curve follows a normal, expected trend, rising from about 2.4V and showing series resistance limitation around 2.8V. Testing of another similar diode however gives a curve that shows an early current rise, starting from about 1.6V and till around 2V forward bias where the current is limited. This flat in the current proceeds up to 2.5V after which the curve rises again. This second rise exactly follows the I-V curve of the first diode.

Such an anomalous behavior was observed in case of Schottky diodes [2] and the phenomenon was attributed to activation of two different Schottky barrier levels at different voltages. The first activation gave the initial part of the I-V curve while at higher voltages, the second higher level is overcome leading to the second rise or "bump" in the curve. A similar though not the same variation was observed in [3] and was explained as due to current controlled negative resistance (CCNR) where low lifetimes in the drift region were said to result in single carrier injection. The change from single to double carrier injection regime caused a sudden decrease in resistance giving a snapback effect.

In this paper, the cause of the anomalous forward I-V behavior is proposed to be defects that can be modeled by small-area diodes of different physical characteristics, parallel to the "ideal" diodes. The initial high current region is then due to the turn-on of one of the "defect" diodes having a smaller effective turn-on voltage. The current rises through this "defect" diode with increasing applied voltage and until it becomes limited by the high series resistance corresponding to very small effective area of the "defect" diode. As the applied voltage further increases the current of the parallel "ideal" diode with higher turn-on voltage becomes significant. When the current through the "ideal" diode exceeds that through the "defect" diode, the second current rise is observed. The location of the rise on the current axis depends upon the effective series resistance of the "defect" diode relative to the current of the "ideal" diode. The "ideal" diode is assumed to have the theoretical band-gap of 3-3.2eV and doping density as extracted from the measured C-V curves. The area used for scaling the "ideal" diode current density in Section III modeling is the actual physical area of the diode. The "defect" diode is assumed to represent a

structural embedded closed core screw dislocation defect. Knowing the commonly observed sizes of SiC epilayer defects, the effective area of the diode is estimated to be much less than 1% of the total diode area [1].

Rise in temperature should increase the diode current densities for both the diodes. Since the current through the larger (ideal) diode scales by a larger area than the smaller (defect) diode, the "ideal" diode I-V is expected to shift left at higher temperatures more than the "defect" diode I-V. This should reduce the prominence of the bump in the combined ("defect" and "ideal") diode I-V. The measurements at high temperature indeed show such a trend as shown in Figs. 1-2. The "ideal" portion of the I-V curve shifts left and up at a higher rate than the "defect" portion due to its larger area causing more increase in the current with temperature. This in effect begins to smooth out the bump in the high temperature I-V in Fig. 1 relative to the room temp I-V, similar to the observations in [2] for Schottky diodes.

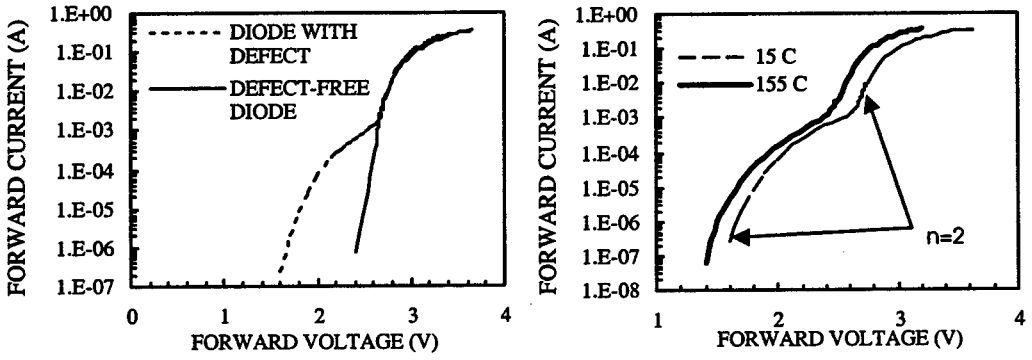

Fig. 1 Measured forward I-V curves for diodes under test

III 2-D Simulations: As described earlier, both the "ideal" and "defect" parts of the SiC diode structure were simulated in the 2-D finite element simulator Atlas-Pisces manufactured by Silvaco Corporation. Each diode (i.e. the "defect" diode and the "ideal" diode) was simulated separately using different values of physical parameters. The "ideal" diode structure was prepared with the end regions doped to 1e19/cm^3. The drift region density was chosen to be that extracted from the capacitance-voltage measurements. The variation of the drift region doping was varied to fit the measured C-V curves.

For the forward I-V simulations, the physical and material parameters of the "defect" diode band-gap, series resistance and area were varied so that the I-V curves were matched for the initial rising part. Since it is observed that the "defect" diode has a smaller effective turn-on voltage, it is expected to have some combination of smaller band-gap and greatly enhanced recombination. For the "ideal" diodes, dopings extracted from C-V measurements were used in structures for simulations. Carrier lifetimes required for matching the I-V curves were extracted from reverse recovery measurements [8]. A good match was obtained for forward I-V curves as shown in Fig. 2. A band-gap of 2eV was estimated for the "defect" diodes and 3.1eV for the "ideal" bulk diodes from the simulations. While admittedly inconsistent with very recent measurements indicating reduced minority carrier lifetimes at closed core screw dislocation defects [9], the same values of minority carrier lifetimes were used for the simulated "ideal" and "defect" diode structures. Only band-gap reduction was used for modeling the "defect" diodes at this time in order to maintain simplicity of the model. For the "ideal" diode, the physical area was known to be 0.81e-2 cm^2. The physical area estimated for the "defect" diodes from the fitting of these simulations to measured data was 4.3e-6 cm^2. Thus the area of the defect diodes came to about 2000 times less than the

area of the "ideal" diode. The series resistance values for the "ideal" and "defect" diodes estimated from the simulations come out to be 1.4 Ω and 1.4 kΩ respectively. The higher resistance for the defect diode is consistent with its much lower physical area. For simulations performed at higher temperatures, the I-V curves showed a good match by additionally reducing the series resistance slightly, which would be consistent with increased ionization of partially frozen-out dopants in the quasi-neutral regions of the epilayer and substrate. The I-V curves showed an n=2 ideality slope indicating that recombination current, not diffusion current, was the dominant forward conduction mechanism for both the "defect" and "defect-free" parts of the diode.

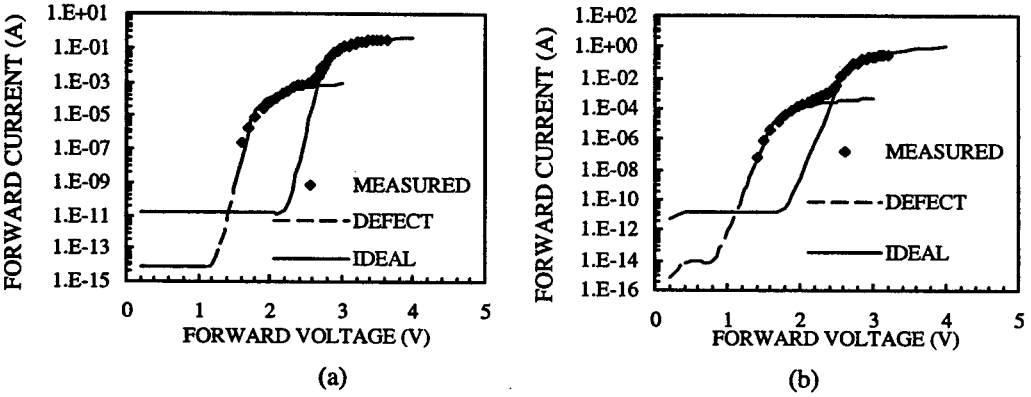

Fig. 2 Measured and simulated forward I-V curves at (a) 55° C and (b) 155° C

V Conclusion: Low voltage 4H-SiC diodes were characterized for static performance. Anomalous I-V curves were observed and attributed to presence of very small area structural defects which are well-known to exist in SiC. The net structure was modeled to first order by a parallel combination of "ideal" and "defect" diodes. The forward I-V curves were shown to turn on for lower voltages by the defects in the device structure, giving an initial high current. A good correlation was obtained between the simulated and measured I-V curves of the parallel combination for different temperatures.

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Materials Science Forum Vols. 338-342 (2000) pp. 1355-1358

6H-SiC Diodes with Cellular Structure to Avoid Micropipe Effects

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Keywords: Cellular Structure, Encapsulation Technique, Mesa pn Diode, Micropipe

Abstract - A cellular structure to avoid micropipe effects of 6H-SiC power devices is discussed. Using a matrix structure with 0.16mm^2 cell area pn mesa diode medium power (600V breakdown voltage and 1A at forward voltage of 5V) has been fabricated and tested. A especially technique to separate and to connect the good cells has been used.

1. INTRODUCTION

The inherent physical properties of silicon carbide (SiC) are extremely well suited for power / high temperature devices. These include a higher breakdown field (more than ten times that of Si) which permits much smaller drift regions (i. e., much lower drift region resistances), a higher thermal conductivity (more than three times that of Si) that permits better heat dissipation, and a wide bandgap energy (2.9eV for 6H-SiC) that enables higher junction operating temperatures [1]. While small-area high voltage (1-5kV) SiC devices are being prototyped and tested, the high density of crystallographic defects in SiC wafers prohibits the attainment of SiC devices with very high operating currents (>50A) that are commonly obtainable in silicon-based high-power electronics [1-2].

Micropipes are well documented as the most harmful defect to 4H- and 6H-SiC power device performance. Micropipes are hollow-core screw dislocations formed during the SiC wafer sublimation growth process. The diameters of the micropipes can vary depending on the growth conditions and formation mechanism but are typically 0.5-10μm in diameter. Both hollow-core (micropipes) and non-hollow-core screw dislocations and associated crystal lattice stress are replicated in subsequently grown SiC epilayers [1].

A correlation of yield and chip size with micropipe density indicates that these defects have to be eliminated for fabrication of large area power devices. Our experiments made on the mesa 6H-SiC *pn* diode with different areas showed there is a "critical device area" of 10^{-3} - $2x10^{-3}$cm^2 to get a good yield [3]. If defects detrimental to high voltage SiC devices are uniformly distributed, the density of the device-killing defects can be estimated to be 500 - 10^3cm^{-2}, given as the inverse of the "critical device area". This density is much higher than a typical micropipe density of 50-100 cm^{-2} observed in commercial production grade SiC wafers [2].

High current devices (1-100A) have a large active area that must withstand electric fields. To realize large area devices with reduced micropipe effect influence a cellular device structure is discussed in this contribution. More cells should be parallel connected to improve current capability. The proposed cellular structure is tested on 6H-SiC *pn* power diodes.

2. DEVICE FABRICATION

Double epitaxial mesa insulated 6H-SiC *pn* junctions with multicell matrix structures were defined in order to eliminate substrate major defects.

The diodes were fabricated on n^+ 6H-SiC Lely modified substrate, doped with nitrogen and fabricated at Compozit Ltd., Moscow. A *n*-type layer (base) ranging in doping from $4x10^{15}cm^{-3}$ to $2x10^{17}cm^{-3}$ with a thickness of about 5μm, followed by a 2μm Al-high doped p^+-type layer were grown by sublimation epitaxy on the substrate at the Ioffe Institute, St. Petersburg.

Mesa groves for cells and diodes separation was performed by CF_4 reactive ion etching (RIE) to a depth of 7μm using a metal mask. Fig. 1 presents a mesa etched 6H-SiC pn junction SEM micrograph. After a 2μm depth etching using Al mask, a smooth semiconductor surface is observed at the bottom of the sample. On the contrary, the etched wall shows some sharp unregulated strips.

To passivate the mesa etched surface some oxidation methods (APCVD, LPCVD, etc.) and different oxide thickness were tested. A thick SiO_2 layer of 1.5μm deposited by LPCVD-TEOS was found to be optimal. This oxide (which is very conformal) fills the micropipes up to 3μm diameter and eliminates the short-circuit which could appear during the post metallization annealing. The contact window in SiO_2 is made with a minimum over etching. On the p^+ layer, the ohmic contact is obtained with sequential evaporation of Al, Ti and Al, having about 2000Å each layer. Ni (5000Å) was employed to form a large area backside contact on the substrate. Ohmic contact with a resistivity of 3- $5x10^{-5}\Omega cm^2$ for Ni backside contact and $2x10^{-4}$ - $2x10^{-2}\Omega cm^2$ for Al/Ti front side contact were obtained after a 1100°C / 2 min. thermal annealing. Finally, the metallization was completed on the top and backside with other Al (2μm) and Ni (5000Å) layers, respectively. The quality of the successive fabrication steps was evaluated all along the diode processing.

To realize large area devices with reduced micropipe effect influence a cellular device structure was designed. More cells should be paralleled to improve current capability. Our statistical analysis (obtained by breakdown voltage measurements on different area devices [3]) showed an optimum area of $400x400\mu m^2$ for the elementary cell and 9 cells for one diode structure. An especially designed method for power SiC device encapsulation has been used for mounting diodes. This technique is illustrated in Fig. 2.

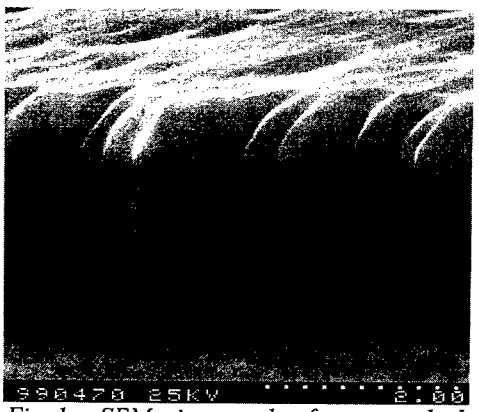

Fig. 1. SEM micrograph of mesa etched sample.

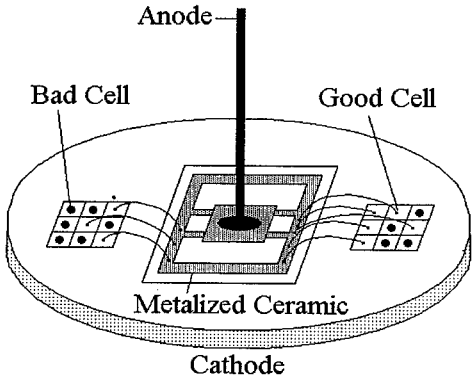

Fig. 2. Packaging method for cellular encapsulated pn power diode.

Characterization of 6H-SiC substrate and epilayers were made using Raman Scattering and Reflectivity Infrared Spectroscopy [4]. Complementary reflectivity measurements on Compozit substrate show a slightly deviation from ideal case observed on the Cree substrate materials [4].

A doping substrate level around $2x10^{18}cm^{-3}$ was determined from the reflectivity measurements. The Raman spectra on the *n* and p^+ epilayer show that a 13% and 10% maximum difference integrated intensity are reached, respectively. This indicates a higher homogeneity of the epilayers as compared with the substrate [4].

3. ELECTRICAL CHARACTERISTICS

Current-voltage curves measured on the wafer are shown in Figs.3-4. Under forward bias, the current-voltage dependence is exponential due to recombination and diffusion currents (Fig. 3). At high injection levels, the series resistance role is dominant. Measurements made on single and multiple paralleled cells showed: (i) the cells numbers influence occurs at low forward injection levels only, where the recombination current is dominant (Fig. 3); (ii) the reverse current is proportional with the connected cells area (Fig. 4).

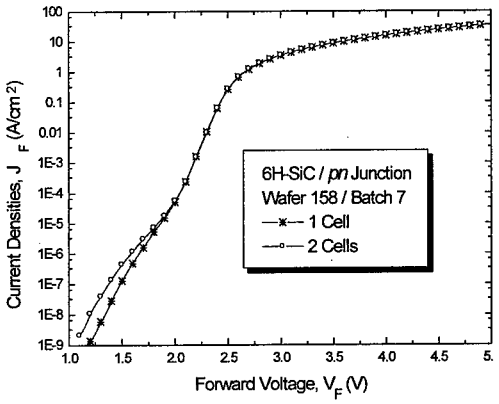

Fig. 3. Forward J_F - V_F characteristics measured on one cell and two parallel connected cells, respectively.

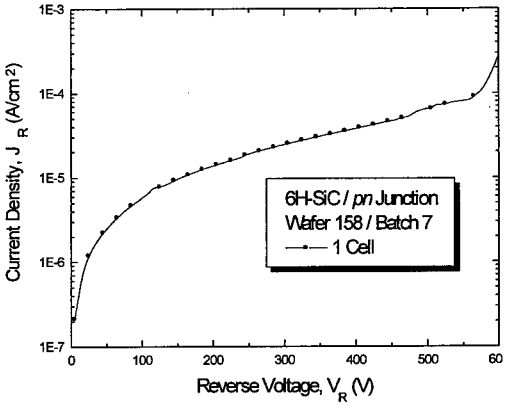

Fig. 4. Typical reverse characteristics of a cell.

Measurements at room temperature on the encapsulated diodes have been performed (Figs. 5-8). The forward current density is mainly invariant with the connected cells (Fig. 5). With temperature increase the forward current density increase too (Fig. 6). The reverse current density has puzzling depends on cells number of the diode (Fig. 7). The reverse current level is larger than simple theoretical predictions by many orders of magnitude; and probably the leakage current is a surface current.

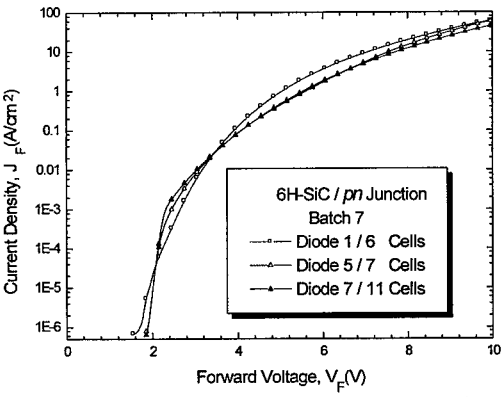

Fig. 5. Forward characteristics measured a room temperature on some diode from batch 7.

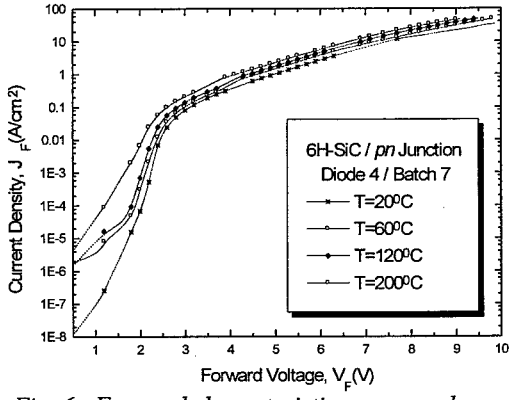

Fig. 6. Forward characteristics measured on a diode with 15 cells from batch 7.

Morphological defects observed on the grown surface [1] and the shape of the mesa etched surface (Fig. 1) cause the increase in leakage current and a strong dependence on the voltage (Fig. 7).

An average of 600V breakdown voltage was measured on diodes from batch 7.The high specific on resistance of the structures from batch 7 fully explains the large voltage drop of 10V at 100A/cm^2 (Figs. 5-6). For comparison, the typical forward characteristic of a diode from batch 5 is presented in Fig. 8. The smaller specific on-resistance of the above batch structures lead to a low voltage drop about of 5V at 100A/cm^2.

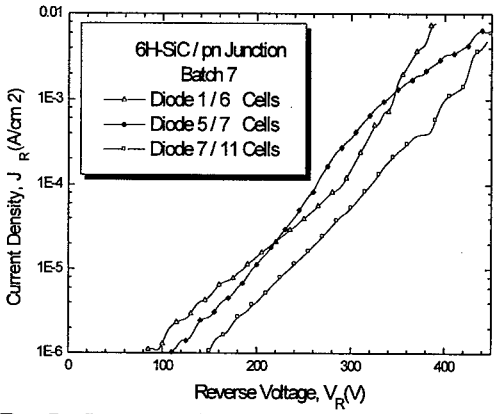

Fig. 7. Reverse characteristics measured o the same diodes as in Fig.5.

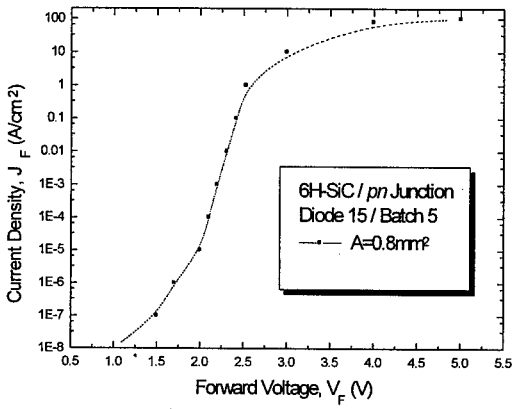

Fig. 8. Typical forward curves measured at room temperature on a diode from batch 5.

5. CONCLUSIONS

A cellular structure to avoid the micropipe effects in 6H-SiC large area devices has been proposed. *pn* diodes with a matrix structure having 0.16mm^2 cell area has been fabricated and tested. An originally technique to separate and to package the good cells from the matrix has been found.

Optical investigations by Raman spectroscopy showed the epilayers and the substrates used in experiments have a good homogeneity and structural quality similar with the Cree samples. SEM micrograph evinced sharp strips on vertical 6H-SiC walls after the mesa etching.

Current voltage characteristics measured up to 200^{0}C on wafer structures and encapsulated diodes showed a 600V breakdown voltage and 1A at a forward voltage smaller than 5V. Large leakage current and soft reverse characteristics are attributed to other defects than the well known micropipes.

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A Closed-Form Analytical Solution of 6H-SiC Punch-Through Junction Breakdown Voltages

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Keywords: 6H-SiC, Breakdown Voltage, Punch-Through

Abstract

In this paper, a closed-form analytical solution of 6H-SiC Punch-Through junction breakdown voltages is presented and verified. It is shown that to obtain a minimum base region specific on-state resistance for 6H-SiC unipolar power devices, a value of $\beta \cong 0.6$ ($\beta = V_{RT}/V_{PT}$) is required. The results can also be used to design soft recovery PiN diodes.

1. Introduction

High voltage diodes are needed for various power electronic applications such as motor control and power transmission systems. Several 6H-SiC PiN diodes have been demonstrated [1-2]. Diode reverse recovery and turn-off failure were also investigated [3].

A punch-through structure is often utilised when designing a bipolar device to reduce the drift region specific on-resistance. An analytical expression for the Si based critical electric field parallel-plane junction has been derived [4], which introduces significant error, especially when the epitaxial-layer thickness becomes thin. Numerical calculations of a punch-through parallel-plane junction based on ionization rates is time-consuming. Recently, a closed-form analytical expression for the silicon PT limited breakdown voltage based on ionization integration was reported [5]. The purpose of this paper is to present an analytical solution of 6H-SiC junction punch-through breakdown voltage which can be used to readily calculate 6H-SiC punch-through junction breakdown voltages. The accuracy of the analytical solution is verified by comparison with numerical simulation results. The solution is also employed to derive the minimum base region specific on-state resistance and design soft recovery 6H-SiC punch-through diodes.

2. An analytical solution for 6H-SiC Punch-Through Junction Breakdown Voltage

By defining a parameter $\beta = V_{RT}/V_{PT}$ (V_{RT} is the reach-through voltage, the voltage when the depletion layer just extends to the i/N+ junction; V_{PT} is the junction PT junction breakdown voltage), the following equations apply when diode reach-through and avalanche breakdown occur respectively, provided the P^+/N^- junction is an abrupt junction:

$$\frac{1}{2}\frac{qNw^2}{\epsilon_s} = \beta V_{PT} \tag{1}$$

$$E_{crit} w - \frac{1}{2}\frac{qNw^2}{\epsilon_s} = V_{PT} \tag{2}$$

where: E_{crit} the critical electric field; w the drift region width; N the drift region doping; ϵ_s the dielectric constant.

Combining Eqns. (1) and (2) generates a critical electric field expression:

$$E_{crit}=\frac{1+\beta}{\sqrt{\frac{2\beta\epsilon_s}{qN}}}V_{PT}^{0.5} \tag{3}$$

While breakdown occurs, assuming the axis origin is at the P^+/N^- junction, the electric field in the drift region is described by:

$$E(x)=E_{crit}-\frac{qN}{\epsilon_s}x \tag{4}$$

An approximate form of ionization rates α_n and α_p is $\alpha_{eff}=\alpha_n=\alpha_p=aE^b$, where a and b are parameters reflecting the properties of semiconductor materials. Using this expression and solving the breakdown condition $\int_0^w \alpha_{eff}dx=1$, an expression for the base width w in terms of base doping N is derived:

$$w=\frac{2\beta}{[(1+\beta)^{b+1}-(1-\beta)^{b+1}]^{\frac{1}{b+1}}}\left(\frac{b+1}{a}\right)^{\frac{1}{b+1}}\left(\frac{\epsilon_s}{q}\right)^{\frac{b}{b+1}}N^{-\frac{b}{b+1}} \tag{5}$$

Equation (5) is an general expression and can be applied to devices fabricated with many semiconductors by adjusting a and b. For 6H-SiC, by fitting to numerical simulation results using the ionization rate expressions [6], a and b are 1.256×10^{41} and 7 respectively. From Equation (5), an approximation solution of β ($0<\beta\le1$) is obtained:

$$\beta=1.221-\sqrt{1.525-1.502c} \tag{6}$$

with $c=7.72\times10^{-12}wN^{\frac{7}{8}}$.

Hence, given a base width w and doping N, the punch-through junction breakdown voltage V_{PT} is computed from Equation (6) and $V_{PT}=V_{RT}/\beta$ (for $V_{RT}=\frac{1}{2}\frac{qN}{\epsilon_s}w^2$).

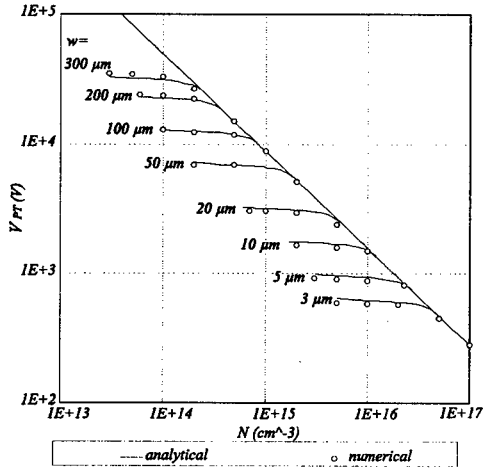

Figure 1. 6H-SiC junction PT limited breakdown voltages

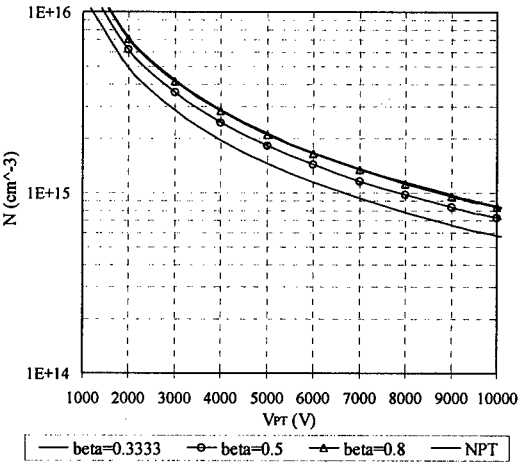

Figure 2. (a)

To verify the accuracy of Equation (6), numerical simulation results are compared with analytical results in Figure 1. The results correspond well with the numerical simulation results. The same procedure can also be applied for deriving PT junction breakdown voltages fabricated with other semiconductors, including 4H-SiC and 3C-SiC.

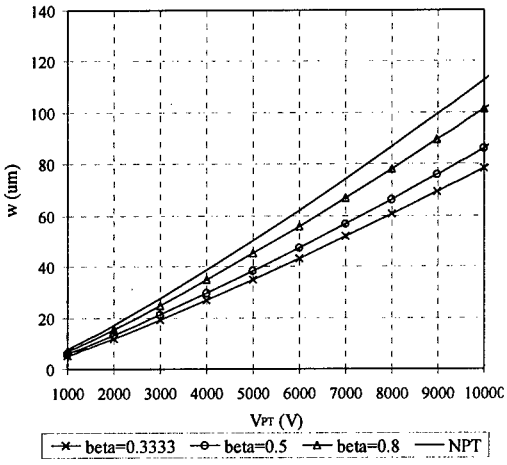

Figure 2 (b)

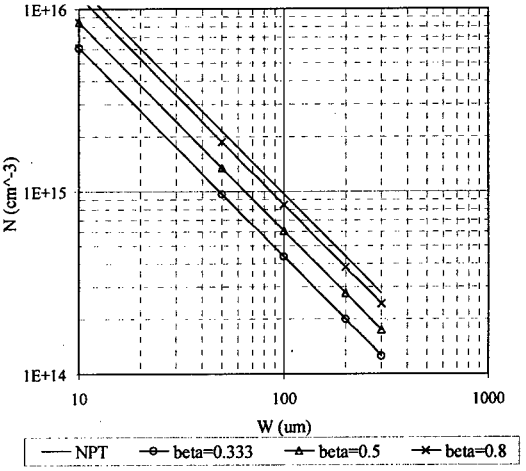

Figure 2 (c)

Figure 2. 6H-SiC junction base region (a) doping, (b) width, against voltage rating and (c) doping against width

To design a 6H-SiC punch-through junction with a specific V_{PT} and β, the following expressions for N and w apply:

$$N=4.6\times10^{20}\frac{\beta}{(1+7\beta^2+7\beta^4+\beta^6)^{\frac{1}{3}}}V_{PT}^{-\frac{4}{3}} \tag{7}$$

$$w=1.524\times10^{-7}(1+7\beta^2+7\beta^4+\beta^6)^{\frac{1}{6}}V_{PT}^{\frac{7}{6}} \tag{8}$$

For a NPT junction, Equations (7) and (8) are simplified by setting β to 1 (also plotted in Figure 1):

$$N_{NPT}=1.826\times10^{20}V_{NPT}^{-\frac{4}{3}} \qquad w_{NPT}=2.42\times10^{-7}V_{NPT}^{\frac{7}{6}} \tag{9}$$

In Figure 2, the base region doping level and width with β=0.33, 0.5 and 0.8 for a 6H-SiC punch-through junction are compared with those for 6H-SiC NPT structures (β=1).

3. Minimum Base Region Specific On-State Resistance

When designing power unipolar punch-through devices like MOSFETs and SBDs, it is customary to minimize the base region specific on-state resistance, $\frac{w}{q\mu N}$, the primary contributor to the on-state resistance in power unipolar devices. For a fixed breakdown voltage, neglecting the slight difference in carrier mobilities in punch-through and non punch-through devices, the ratio of punch-through device base region $R_{on,sp}$ to NPT device base $R_{on,sp}$ is described by:

$$f(\beta)=\frac{R_{on,sp,PT}}{R_{on,sp,NPT}}=\frac{wN_{NPT}}{w_{NPT}N}=\frac{0.25\sqrt{1+7\beta^2+7\beta^4+\beta^6}}{\beta} \tag{10}$$

The definition of β is as above ($\beta=V_{RT}/V_{PT}$). In the range $0<\beta\leq1$, a minimum value of $f(\beta)=0.78$ occurs at β=0.60. Therefore, to design a device with a minimum base region specific on-state resistance, a value of $\beta\cong0.6$ would be used.

4. Soft-recovery design of 6H-SiC PiN diodes

It is customary to minimise the drift region width so that the injected charge during the on-state can be reduced greatly in punch-through bipolar devices compared to non punch-through devices. However, this does not apply to PiN diodes. The most important issue when designing a PiN diode is to avoid snap recovery, that is, the diode reverse current changes abruptly during the reverse recovery. When the depletion layer reaches the i/N+ junction, most stored charge has been swept out of the drift region or diminished via recombination. A rapid change of the diode current occurs at that moment. Generally, V_{RT} is designed to be equal to the DC link voltage, which is 50 to 80% of the diode breakdown voltage V_{PT}.

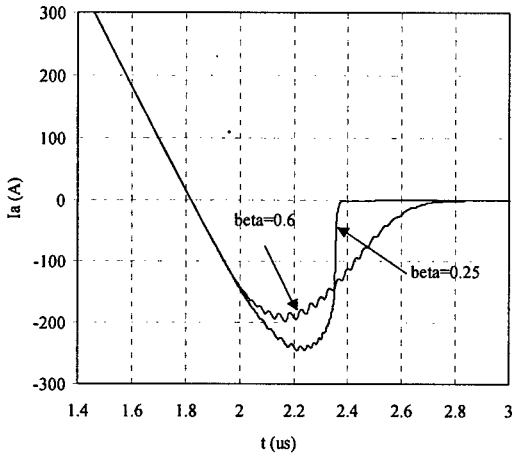

Figure 3. 6H-SiC PiN diode reverse recovery current waveforms

Numerical simulations are performed to compare the reverse recovery behaviours of two 5 kV 6H-SiC PiN diodes, which are designed using Eqs. (7-8) with β of 0.25 and 0.6 respectively. The devices are switched from an on-state current of 1.5 kA to blocking a cathode voltage of 2.5 kV. An RC snubber circuit is paralleled with the diode. The di/dt is 833 A/μs and the junction temperature is 500 K. As shown in Figure 3, the diode with β of 0.6 shows a favoured soft recovery characteristic. In comparison, the diode with β of 0.25 exhibits a snap recovery behaviour and the voltage rises an extra 1.3 kV. The snap can cause a large voltage spike due to the existence of parasitic inductances and even catastrophic destruction of other circuit components.

5. Conclusion

In this paper, a closed-form analytical solution of 6H-SiC Punch-Through junction breakdown voltages has been derived. The results fit well with numerical simulation results. It was found that to obtain a minimum base region specific on-state resistance, a value of $\beta \cong 0.6$ ($\beta = V_{RT}/V_{PT}$) is required. The solution has also been employed to design a soft recovery PiN diode.

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Study of the Breakdown Voltage of Protected or Non-Protected 6H-SiC Bipolar Diodes by OBIC Characterisation

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Keywords: Breakdown, Diode, JTE, OBIC, Peripheral Protection

ABSTRACT The OBIC (Optical Beam Induced Current) method and its application to study SiC implanted diodes protected or not by JTE are presented in this paper. These measurements associated to the simulation results illustrate the effects of the periphery emitter doping profile on the electric field distribution and give information concerning the operation of the Boron implanted JTE on the breakdown voltage.

1. INTRODUCTION

Silicon carbide presents electrical properties suitable for many applications especially for high power devices. In addition to the semiconductor's high critical electric field, the breakdown voltage depends on the protection used for the junction termination. The JTE (Junction Termination Extension) technique is a potentially efficient protection to prevent premature breakdown for high voltage SiC devices. The OBIC (Optical Beam Induced Current) technique is a powerful method to investigate the electric field distribution in periphery of high voltage planar diodes and to study the operation of the junction termination [1]-[3]. This work presents electrical and OBIC characterisation results obtained from experimental 6H-SiC bipolar diodes protected or not by Boron implanted JTE and compared to the simulation results with ISE simulation software.

2. EXPERIMENTS

2.1 Device structures

The p^+nn^+ diodes are realised on a n^+-type 6H-SiC substrate doped at 3×10^{18} cm^{-3}. Five successive implantations of Aluminum at 300 °C (at energies ranging from 25 keV up to 300 keV) into the n-type epilayer (thickness = 10 µm, doping level = 3×10^{15} cm^{-3} confirmed by C-V measurement) create the emitter (depth = 0.5 µm, target-doping level = 4×10^{19} cm^{-3}). JTE (depth = 0.7 µm, target-doping level = 2×10^{17} cm^{-3}) is realised by 11 Boron implantations realised at 300°C. The samples were annealed at 1700 °C during 30 minutes [4], and metallized for anode and cathode ohmic contacting at the end. No passivation layer covers the semiconductor surface. We have tested two types of diodes: D1 diodes without JTE, D2 diodes protected by JTE (Fig.1). OBIC and electrical characterisations have been performed on these devices.

2.2 OBIC Setup and method

Fig. 2 shows the experimental setup that we use to perform OBIC measurements. An Ar^{++} laser produces an UV beam at different wavelengths (from 363.8 nm to 300 nm) which is focused on the sample and modulated at 70 Hz by a chopper. A lock-in amplifier detects the local variation of the photocurrent induced by the 3.3 µm incident light spot on the reverse biased device. A computer controls 2 stepper motors to ensure the horizontal moving of the device under test and records current measurements as a function of the light spot position.

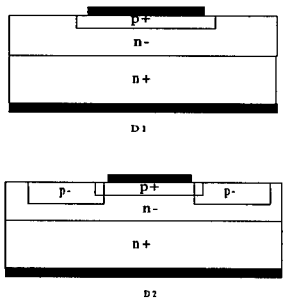

Fig. 1 : P^+NN^+ diodes.

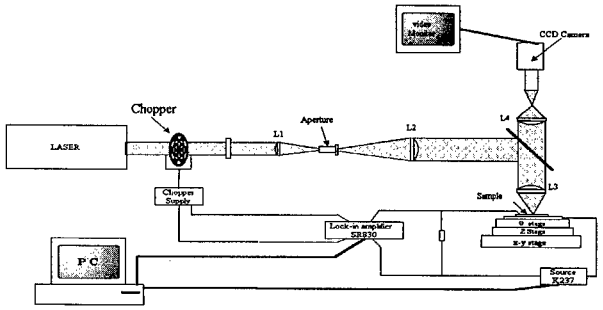

Fig. 2 : OBIC setup.

3. RESULTS AND DISCUSSION

3.1 I-V characteristics and breakdown voltage

Breakdown voltage measurements were made in 2 different ambients (air and silicone oil) at room temperature. Though a quite wide range of breakdown values (Tab. 1) is obtained, we can first note the influence of the ambient nature. Breakdown voltages are slightly better in the higher dielectric strength ambient (oil). That indicates that the breakdown takes place in the ambient, confirmed by the arc occurrences observed between the edge of the p^+n junction SCR and the anode contacting probe (well visible during tests in oil). Moreover, contrary to air-testing, the results in the oil indicate a JTE presence effect, allowing the observation of Vbr values up to 1700 V for D2 protected devices (Theoretical breakdown value = 1640 V). Besides, all experimental breakdown voltages for D1 diodes are higher than the expected value (360 V) obtained by simulation, taking into account a box profile shape of p^+ emitter and the ionisation coefficients given by Konstantinov et al. [5]. Moreover we observe that the highest voltage sustaining structures often exhibit elevated voltage drop under high forward current. Fig. 3 presents 2 typical kinds of forward characteristics at room temperature. The different reverse characteristics present the same non linear behaviour, with typically $J_r = 1\times10^{-6}$ A/cm^2 at $V_r = -600$ V at 300 K. Among the possible explanations of such inhomogeneous results is the p^+ doping profile, as confirmed by the different Al impurity profiles over the wafer obtained from SIMS measurements (Fig. 4). The different Al profiles are due to the surface etching during post-implantation annealing. The use of OBIC measurements is aimed at completing the analysis by studying the influence of the emitter doping profile and the surface charges on the electric field distribution at the device periphery.

Ambient	Air	Oil
Breakdown voltage for D1	400 V – 1100 V	700 V – 1200 V
Breakdown voltage for D2	600 V – 1100 V	600 V – 1700 V

Tab.1: Values of breakdown voltage in different ambients.

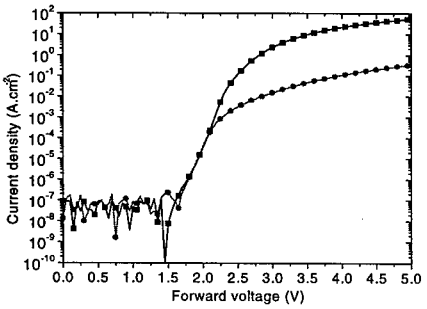

Fig. 3: Two typical forward characteristics at 300 K

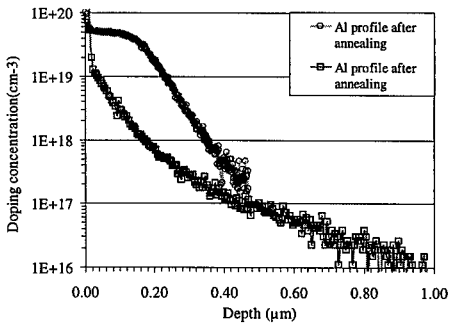

Fig. 4: Two different SIMS Al profiles at different places on the wafer

3.2 OBIC Measurements

Fig. 5 shows the OBIC signals simulated and measured on 2 non protected D1 samples along one half diameter line at λ =333.6 nm or λ =351.1 nm, corresponding respectively to light penetration lengths of 5 µm and 10 µm in 6H-SiC, with a spot diameter of 3.3 µm and an optic power density of 1 W/cm^2. For simulation, the p^+ emitter profile has a constant doping level of 4×10^{19} cm^{-3} up to 0.35 µm depth; and we neglected any surface charge density.

Fig. 5a shows D1 experimental results exhibiting the same behaviour as the simulated ones presented on Fig. 5b. A constant photocurrent is induced when the UV spot scans the emitter region, non-covered by the anode metal. This current increases with the voltage due to the space charge region (SCR) spreading. Moving towards the structure periphery an OBIC peak occurs at the edge of the p^+n junction SCR, which grows with increasing voltage. This peak is caused by the local carrier multiplication (essentially holes multiplication) produced by the high electric field at the p^+n junction. Outside the SCR, the current decreases exponentially due to photogenerated hole diffusion (L_p = 4 µm for the simulation and 9 µm for the measurements). The laterally non abrupt Al concentration profile, the L_p value, and the spot diameter uncertainty, can explain the wider experimental OBIC signals compared to the simulated ones. The fact that we do not detect any OBIC signal far outside the diode at low voltage, indicates no significant presence of surface charges. So the higher experimental breakdown values for D1 (compared with the simulation) may not be explained by the effect of surface charges.

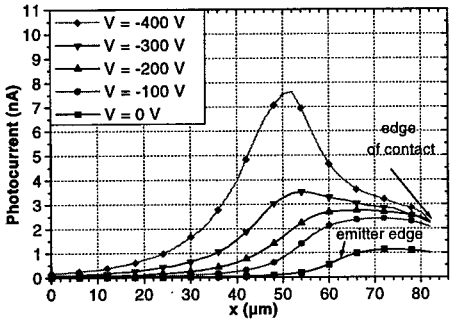

Fig. 5a: OBIC signal on D1 at λ = 333.6 nm

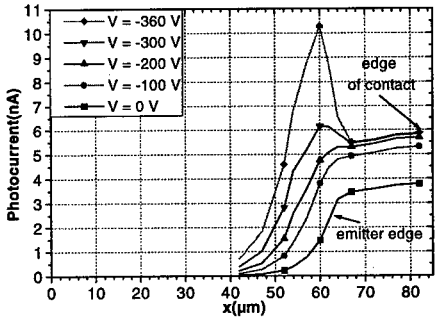

Fig. 5b: OBIC simulation at λ = 333.6 nm

Fig. 5c shows a second type of experimental behaviour. In that case, the photocurrent increases with applied voltage and saturates when the epilayer is totally (depleted width = 10 µm depleted at V_r = - 280 V). But no peak arises at the periphery. This result means that the electric field distribution at the junction periphery is different. That can be explained by the periphery emitter doping profile. In fact for experimental acceptor doping profiles as presented on Fig. 4, the simulation results show that lower electric fields are obtained for a given reverse bias as compared with the theoretical Al profile case.

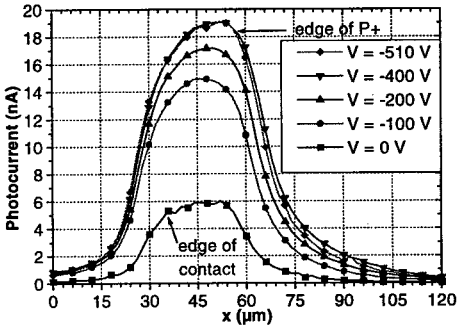

Fig. 5c: OBIC signal on D1 at λ = 351.1 nm

We expose the OBIC measurements obtained from JTE D2 diodes on Fig. 6, using semi-logarithmic scales. Fig. 6 allows to observe 3 distinct zones in the OBIC signal obtained at the periphery of the anode contact. First we recognise the OBIC signal due to the p^+ region, as for D1 diodes. Then the photocurrent decreases versus the distance from the emitter region edge. At this position, OBIC signal is due to the extension of SCR on both sides of the JTE pn junction. The presence of a peak at the emitter edge reveals a total depletion of the JTE near p^+ region. The third zone on Fig.6 corresponds to the external side of JTE. For the reported reverse biases, the SCR extension in the n-type epilayer remains weak, leading to small current. Such a behaviour requires a low doped JTE region. Fig.7 shows the simulated equipotential line repartition in a structure assuming a 1×10^{16} cm^{-3} doped JTE with a 1.4 µm deep gradual junction, in agreement with the effective Boron profiles checked by SIMS analysis. Such a too low doping level of the JTE protection allows to explain the weak difference in breakdown voltages between D1 and D2 diodes.

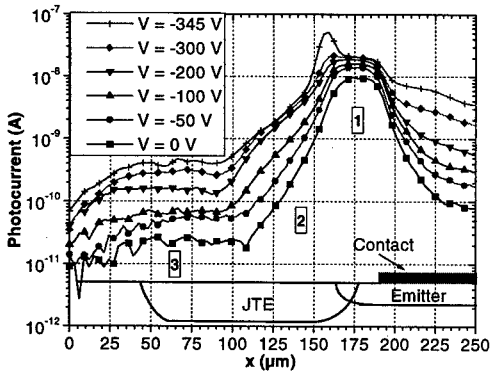

Fig. 6: D2 OBIC measurement at λ = 351.1 nm with Popt = 1.5 W /cm²(semi-logarithmic scale)

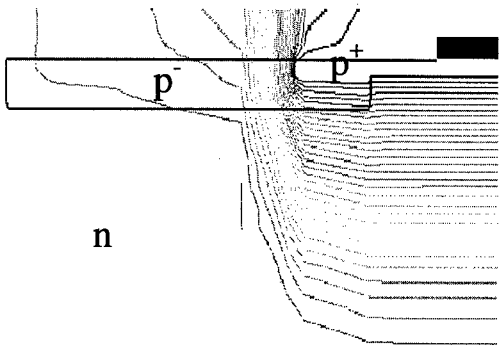

Fig. 7: ISE simulation of equipotential repartition for a diode with JTE at reverse bias voltage of 450 V

4. CONCLUSION

This paper shows that the OBIC measurements performed on our planar 6H-SiC bipolar diodes, combined with the electrical characterisations and the simulations, allow to analyse the device behaviour under reverse biases. The examination of both experimental and simulated OBIC signal versus the position of the localised photogeneration zone can give information concerning the place of the breakdown region, the effect of the junction doping profiles (emitter or JTE) and the presence of surface charges. From the presented results, the effective operation of the Boron doped JTE protection and the reasons for its poor efficiency could be evidenced.

Acknowledgements : This work was supported by GIRCEP group and Schneider Electric Research Center. We are grateful to C. Dubois from LPM- Insa Lyon for SIMS measurement performance.

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Materials Science Forum Vols. 338-342 (2000) pp. 1367-1370

Al/C/B Co-Implanted High-Voltage 4H-SiC PiN Junction Rectifiers

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Keywords: High-Level Lifetime, High-Voltage Power Device, Pin Rectifier, Reverse Recovery

Abstract: We investigate the static and dynamic characteristics of implanted anode high-voltage 4H-SiC pin junction rectifiers. The epitaxially grown drift layer has a thickness of 40 μm and a blocking voltage of 4.5 kV is measured with a leakage current of $1x10^{-4}$ A/cm^2. An average forward drop of 4.7 V for 300 μm x 300 μm devices and 5.0 V for 800 μm x 800 μm devices is measured at 100 A/cm^2 and 25°C. A minimum ideality factor of 1.2 is determined. Reverse recovery measurements indicate a high-level lifetime of at least 20 ns at room temperature and 90 ns at 250°C.

1. Introduction

Because of its excellent physical properties, SiC offers the promise of high-voltage, fast-switching power rectifiers with low forward voltage drop. Significant activities in developing SiC power devices have taken place in the last few years and several high-voltage epi-grown and implanted 4H-SiC junction rectifiers have been successfully demonstrated [1-5]. High-voltage power rectifiers made from SiC offer higher operating temperature, lower switching losses, and lower forward drop compared to silicon devices. Silicon rectifiers are constrained to operation below 10 kV while SiC rectifiers are anticipated to operate as high as 50 kV due to the larger critical electric field of SiC. This paper presents the static and dynamic electrical characteristics of 4.5 kV implanted anode 4H-SiC pin junction rectifiers.

2. Device Structure and Fabrication

The structure of the fabricated pin junction rectifier is shown in Fig. 1, where a 40 μm lightly doped ($1x10^{-15}$ cm^{-3}) n-type epitaxial layer has been grown on an n$^+$ 4H-SiC substrate. An ideal parallel plane breakdown voltage of 6.4 kV is calculated for this drift layer. The p$^+$ anode has been formed by multiple implants of aluminum, carbon, and boron, similar to those used for 1.1 kV junction rectifiers that utilize a deep boron implant for optimal junction leakage and a shallow aluminum/carbon implant for emitter injection and ohmic contact [4]. Boron was implanted with energies ranging from 25 to 300 keV at 650°C with a total dose of $3.3x10^{14}$ cm^{-2} resulting in a junction depth of 0.7 μm. Aluminum and carbon were implanted to a depth of 0.2 μm with energies of 30 - 180 keV and 20 - 120 keV, respectively at 800°C, each with a dose of $3.6x10^{15}$ cm^{-2} for a concentration of $2x10^{20}$ cm^{-3}. A three zone boron implanted junction termination extension (JTE) has been used as the termination for these devices with implanted dose of $1.9x10^{13}$ cm^{-2}, $1.2x10^{13}$ cm^{-2} and $6.6x10^{12}$ cm^{-2} from the inner zone to the outer zone. A nitrogen implanted n$^+$ field stop provides isolation from adjacent devices. The planar structure of these devices eliminates the need for trench isolation as required in epitaxially grown junctions. Square anode sizes of 300 μm, 800 μm, and 4000 μm are fabricated.

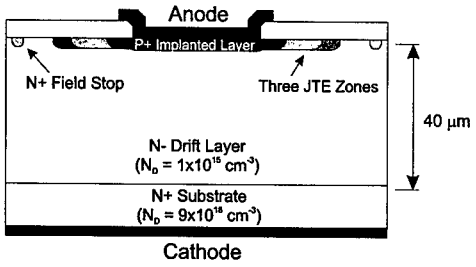

Fig. 1. Cross-section of implanted anode 4H-SiC pin junction rectifier.

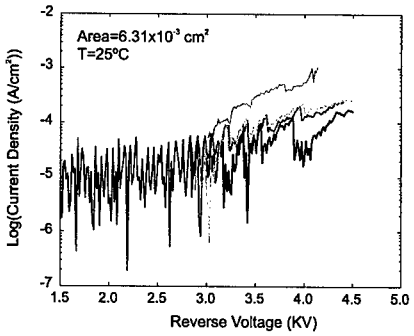

Fig. 2. Reverse blocking voltage of 800 μm x 800 μm devices at 25°C.

3. Electrical Characteristics

The reverse blocking characteristics for several 800 μm x 800 μm devices at 25°C are shown in Fig. 2 up to 4.5 kV where leakage currents are on the order of 10^{-4} A/cm^2. The leakage current is below the measurement limit at moderate reverse voltage at room temperature.

The forward characteristics of these devices have been measured up to 250°C. Fig. 3 shows the log(current) versus voltage characteristics of a 300 μm x 300 μm device at various temperatures. One noticeable feature of these characteristics is the rapid increase in forward voltage drop above 1 A/cm^2. This current density is below the level where high-level injection or series resistance can influence the forward characteristics so some other mechanism must be proposed. The ideality factor can be used to identify the current mechanisms of a junction rectifier. An ideality factor of 1 indicates diffusion limited current while an ideality factor of 2 indicates recombination limited current. Intermediate values of the ideality factor indicate that both recombination and diffusion currents are present due to a combination of deep and shallow levels. The ideality factor extracted from the forward characteristics of Fig. 3 is shown in Fig. 4 at 25°C. At low currents, the current mechanism consists of both diffusion and recombination. Between 10^{-5} and 10^{-4} A/cm^2 the recombination current mechanism dominates. Above 10^{-4} A/cm^2 the current becomes increasingly dominated by the diffusion mechanism where a minimum ideality factor of 1.2 is measured. The ideality factor rises rapidly above 10^{-1} A/cm^2 and may be attributed to single carrier injection if the ambipolar diffusion length is much less than one half the drift layer thickness [6].

The distribution of room temperature on-state voltage drop at 100 A/cm^2 indicates an average voltage drop of 4.68 +/- 0.29 V for the 300 μm devices and 4.96 +/- 0.20 V for the 800 μm devices. The forward characteristics of a typical 800 μm x 800 μm device plotted on a linear scale are shown in Fig. 5 up to 250°C. The on-state voltage decreases significantly at elevated

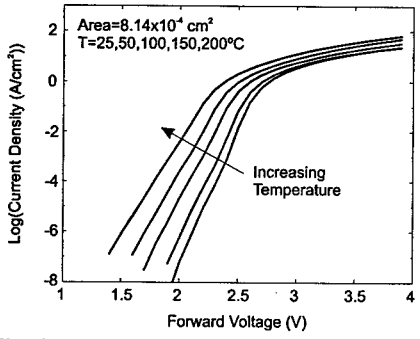

Fig. 3. Forward log(current) versus voltage characteristics of a 300 μm x 300 μm device.

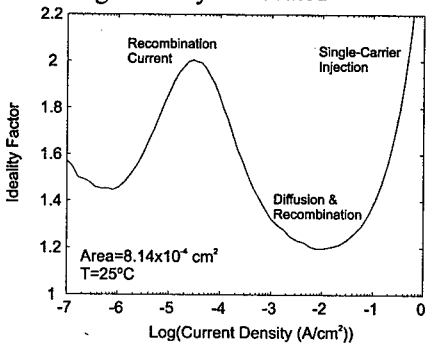

Fig. 4. Ideality factor extracted from Fig. 3 at 25°C.

temperatures. The actual junction voltage drop can be determined by subtracting the voltage drop contributed by the parasitic series resistance. Table 1 lists the measured voltage drop and the corrected value (after accounting for series resistance) at a current density of 100 A/cm^2. The series resistance is mainly due to the p-contact resistance, measured from 4-terminal Kelvin contact test structures, and the substrate resistance as determined from simulations using TMA Medici. For comparison, the simulated forward voltage drop at 100 A/cm^2 for a junction with an ambipolar lifetime of 1.2 μs is also shown. The corrected forward voltage drop is 1.3 V larger than simulated at 25°C but only 0.5 V larger at 250°C indicating an increase in lifetime with temperature. The high-level lifetime is estimated by comparing the measured and simulated forward voltage drop at 100 A/cm^2. Fig. 6 shows the simulated forward voltage drop as a function of ambipolar lifetime at 300K. The measured voltage drop of 4.4 V indicates a high-level lifetime of ~ 40 ns.

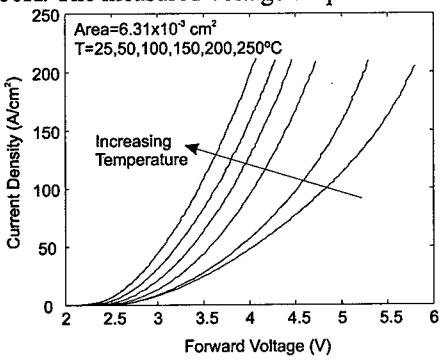

Fig. 5. Forward current voltage characteristics of a typical 800 μm x 800 μm device.

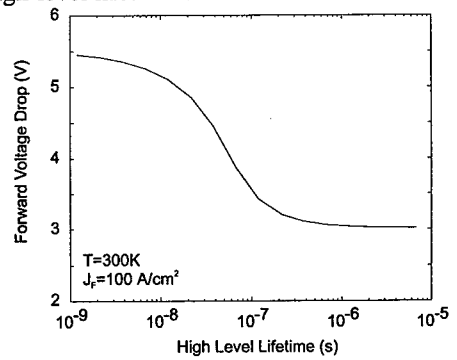

Fig. 6. Simulated forward voltage drop versus high level lifetime at 100 A/cm^2.

Table 1. Forward voltage drop versus temperature at 100 A/cm^2 for device of Fig. 5.

T (°C)	V_F (V)	$R_{pcontact}$ (mΩcm^2)	$R_{substrate}$ (mΩcm^2)	Corrected V_F (V)	Simulated V_F* (V)
25	4.83	2.19	2.11	4.40	3.15
50	4.52	1.78	2.02	4.14	3.09
100	4.04	1.20	1.95	3.73	2.98
150	3.81	0.77	1.76	3.56	2.87
200	3.63	0.59	1.74	3.40	2.78
250	3.45	0.50	1.72	3.23	2.69

*Simulated with τ_n=1.0 μs, τ_p=0.2 μs, μ_n=480 and μ_p=60 cm^2/Vs

Reverse recovery measurements have been performed to measure the high-level lifetime for these junctions[7]. In Fig. 7, reverse recovery characteristics of the SiC pin rectifier of Fig. 5 are compared with those of a commercial silicon pin rectifier with a drift layer of approximately 50 μm. The extracted high-level lifetime (τ_{HL}) and reverse recovery charge (Q_{rr}) are listed in Table 2. For the SiC rectifier, a reverse recovery charge of 2.8 nC and a lifetime of 21 ns are measured at 25°C, while in the Si rectifier, a much larger high-level lifetime and reverse recovery charge are measured. The increase of carrier lifetime with temperature is consistent with optically determined lifetime measurements versus temperature [8]. Also, the reverse recovery characteristics shown in Fig. 7(a) indicate a rapidly decaying component and a slowly decaying component, most noticeable at higher temperatures. Compared to the 800 μm x 800 μm devices, the high-level lifetime measured on the 300 μm x 300 μm devices is found to be smaller indicating the presence of perimeter recombination effects as described by Neudeck [9] and Kimoto, et al. [10].

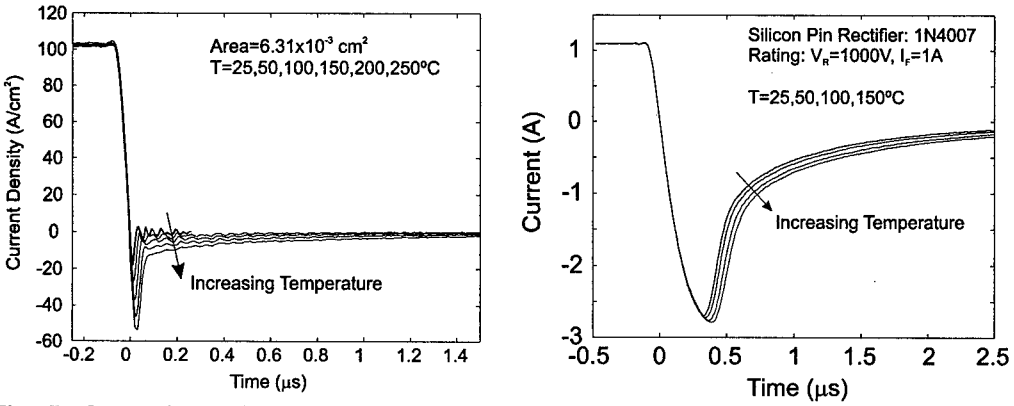

Fig. 7. Comparison of reverse recovery characteristics of (a) 4H-SiC pin rectifier and (b) commercial silicon rectifier, both measured with a reverse voltage of -50 V.

Table 2. Extracted parameters from reverse recovery measurements of Fig. 7.

T (°C)	4H-SiC pin t_{HL} (ns)	4H-SiC pin Q_{rr} (nC)	Si pin t_{HL} (μs)	Si pin Q_{rr} (μC)
25	21.3	2.76	2.20	1.58
50	25.4	3.71	2.31	1.68
100	32.6	5.54	2.44	1.82
150	50.8	10.4	2.57	1.94
200	69.0	17.6	-	-
250	86.0	24.0	-	-

4. Summary

The electrical characteristics of implanted anode high-voltage 4H-SiC pin junction rectifiers have been discussed. A reverse blocking voltage of up to 4.5 kV is measured with a leakage current of $1x10^{-4}$ A/cm^2 at room temperature. The forward voltage drop for a typical 800 μm square device at 100 A/cm^2 is measured to be 4.8 V at 25°C and falls to 3.5 V at 250°C. A minimum ideality factor of 1.2 is measured on the 800 μm x 800 μm devices. The ideality factor rises rapidly above 0.1 A/cm^2 and is attributed to single carrier injection as a result of the thick drift layer and low carrier lifetime. Reverse recovery measurements indicate increasing lifetime with temperature where a high-level lifetime of 21 ns is measured at 25°C and 86 ns at 250°C.

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Materials Science Forum Vols. 338-342 (2000) pp. 1371-1374

6.2kV 4H-SiC pin Diode with Low Forward Voltage Drop

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Keywords: High Blocking Voltage, Mesa JTE, Reverse Recovery Time, SiC Pin Diode, V_F

Abstract

A pin diode with improved termination named mesa JTE has been developed and a new record high blocking voltage of 6.2kV and a low V_F of 4.7V at 100A/cm^2 have been achieved. The diode developed has a short trr of 28.5ns and an excellent trade-off between the blocking voltage and V_F superior to the trade-off of the commercialized Si pin diodes.

1. Introduction

SiC is expected to enable the realization of power semiconductor devices with performance superior to that of Si power semiconductor devices because of their excellent electrical and physical properties. On the other hand, bipolar devices can achieve lower power dissipation than unipolar devices in high voltage application areas due to its conductivity modulation effect. But, because of larger bandgap, shorter lifetime and larger p contact resistance of SiC, it has been difficult to reduce the forward voltage drop (V_F) of SiC bipolar devices to below that of Si bipolar devices in spite of several R&D efforts [1-4]. By improving the quality of the epitaxial layers and the structures of the junction terminations, we succeeded in improving the trade-off between V_F and the blocking voltage of the SiC bipolar pin diode. This paper reports on a high voltage pin diode with a new record high blocking voltage of 6.2 kV and a low V_F of 4.7 V at 100A/cm^2, exceeding the trade-off of the commercialized Si pin diodes for the first time.

2. Device Structure and Simulation

Fig.1 shows the high voltage pin diode with the improved termination, mesa JTE (Junction Termination Extension). The diode is a punch-through type and is fabricated by using 4H-SiC wafers with n- epitaxial layers of about 50μm in thickness and 1x10^{15}cm^{-3} donor concentration. The p+ layer is also formed by epitaxial deposition, because the pn junction formed

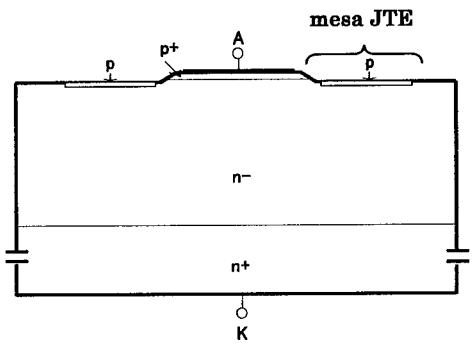

Fig. 1 Cross-sectional view of 6.2 kV diode with shallow mesa JTE.

by ion implantation typically has poor forward characteristics as compared with that formed by epitaxial growth. Conversely, since good forward characteristics are not indispensable for the JTE, it is formed by using ion implantation after shallow mesa etching of the p+ epi-layer, and therefore, it is named mesa JTE. The depth of the mesa is about 2 μm and that of the p+ layer is about 1.5 μm. The pn junction is an abrupt junction and impurity concentration of the p+ layer is $1x10^{18}cm^{-3}$.

Fig.2 shows simulated relationships between the blocking voltage and the mesa angle of mesa JTE. The definition of the mesa angle θ is shown in the inset of Fig.2. The simulator is ISE TCAD, which was also used in designs of 1.4kV 4H-UMOSFET [5]. The surface of the mesa JTE is covered with a thick oxide film so that the blocking voltage is limited by electric field concentrations in SiC and not in SiO_2. The surface charge density is $1.0x10^{11}cm^{-2}$. As the mesa angle becomes large, the blocking voltage becomes higher to a maximum of 80 degrees and then begins to decrease. In the cross-section shown in Fig.1, or the inset of Fig.2, the electric fields concentrate at both pn junctions close to the bevel surface of the mesa, site a, and at the edge of JTE of the chip edge side, site b. The electric field of the latter is constant and independent from the mesa angle. On the other hand, the electric field of the former becomes high as the mesa angle becomes large, and is larger than that of the latter at each mesa angle. Therefore, the blocking voltage is limited by the electric field at site a and the mesa angle of 80 degrees is suitable to achieve the maximum blocking voltage, which is 6,640V.

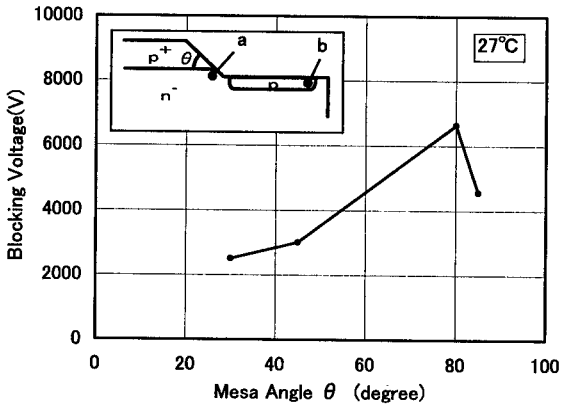

Fig. 2 Simulated relationships between blocking voltage and mesa angle.

Fig.3 shows simulated relationships between blocking voltage and the p layer impurity concentration of mesa JTE, which has an impurity profile of box type. As the impurity concentration becomes high, the blocking voltage becomes high and reaches maximum at $2.5 x10^{17}cm^{-3}$ before it drops. On the other hand, as the impurity concentration

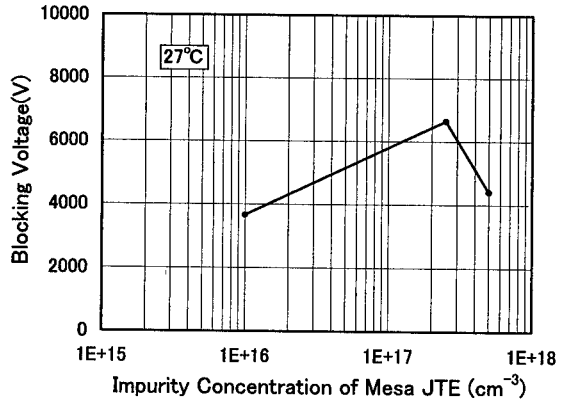

Fig.3 Simulated relationships between blocking voltage and impurity concentration of mesa JTE.

increases, the electric field at site a becomes lower but that at site b becomes higher. The former is larger than the latter at impurity concentrations of less than 2.5 $x10^{17}cm^{-3}$ and limits the blocking voltage, but the latter becomes larger than the former at more than 2.5 $x10^{17}cm^{-3}$ and limits the blocking voltage. To achieve the maximum blocking voltage, the impurity concentration should be about $2.5x10^{17}cm^{-3}$.

The dependence of blocking voltage on other parameters has also been simulated, and the device structure has been optimized.

3. Device Fabrication and Characterization

The diodes with an optimized structure were designed and fabricated. The design of the diode's active area is a circle, and two diameters, 200 μm and 500 μm, were fabricated. Fig.4 shows the reverse and forward characteristics of the fabricated pin diode with the shallow mesa JTE and the active area of 200 μm in diameter. A blocking voltage of 6.2kV was achieved. This is the highest blocking voltage reported to date for SiC devices. The leakage current at 6.2kV is $1.5x10^{-5}cm^{-3}$, and the diode shows rapid avalanche breakdown over 6.2kV. Since the mesa angle of the fabricated diode is about 75 degrees, the achieved blocking voltage of 6.2 kV fits the simulated result shown in Fig.2. The V_F is 4.7 V at $100A/cm^2$, and the differential on resistance (dV/dI) beyond the build-in voltage is $7.4m\Omega cm^2$, which is very small and therefore indicates sufficient conductivity modulation.

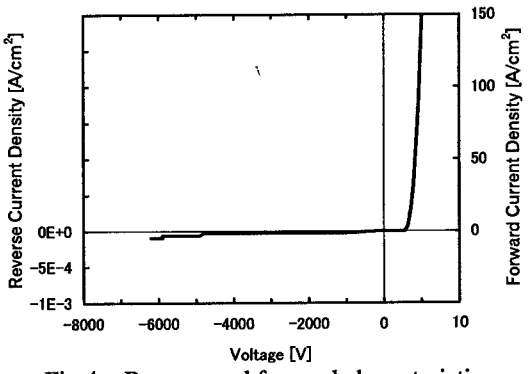

Fig.4 Reverse and forward characteristics of 6.2 kV diode with shallow mesa JTE.

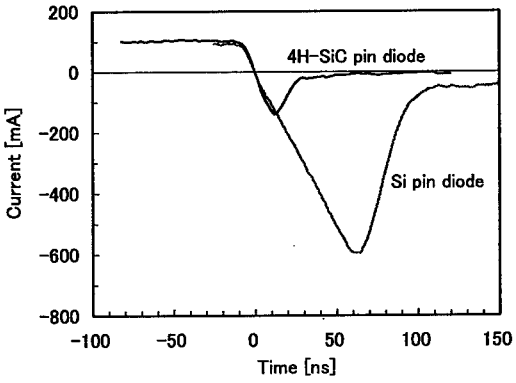

Fig.5 Turn-off waveform of fabricated 6.2kV SiC pin diode and 400V Si pin diode.

Dynamic measurements of the fabricated SiC diode have been performed in a chopper circuit switched by a conventional Si MOSFET. The turn-off performance is determined with a current ramp of dI/dt =17A/μs to a reverse voltage of 30V. Fig.5 shows turn-off waveforms of the fabricated diode. The reverse recovery time trr is 28.5ns. The reverse recovery current density is $70A/cm^2$, and the reverse recovery charge Qrr is 2.0nC. Fig.5 also shows turn-off waveforms of a high speed Si diode rated for 400V (Hitachi's U06E); its trr, Jrr and Qrr are 96.1ns, $299A/cm^2$ and 28nC, respectively. In spite of the fact that the SiC diode is more than 10 times higher

voltage (6.2 kV), very high speed turn-off performances can be achieved as compared with the Si diode of a low rating blocking voltage.

Fig.6 shows the trade-off curves between the blocking voltage and V_F at 100A/cm^2 regarding the reported SiC diodes [1-4], Si pn diodes commercialized in Japan and SiC diode in this work. In the case of both a SiC schottky diode (SiC-SBD) and a Si pn diode, the V_F becomes remarkably large at a blocking voltage of more than 1.8kV and 3kV, respectively, because the resistance of the n^- drift layers becomes more dominant than the schottky barrier height and the build-in potential of the pn junction. However, such a tendency is not clear in the case of the SiC-pn diode because of data scattering. The V_F of the SiC-pn diode is higher than that of the SiC-SBD at less than 2kV, but becomes lower than that of the SiC-SBD at more than 2kV. Furthermore, the V_F of the reported SiC-pn diodes seems to be higher than that of the Si-pn diode at less than 8 kV. However, the SiC-pn diode in this work has smaller V_F than that of the Si-pn diode at even 6.2kV, and has a trade-off between the blocking voltage and V_F superior to that of the Si-pn diode. The trade-off seems to be still more improved by decreasing the p contact resistance, which limits V_F of the SiC-pn diode in this work.

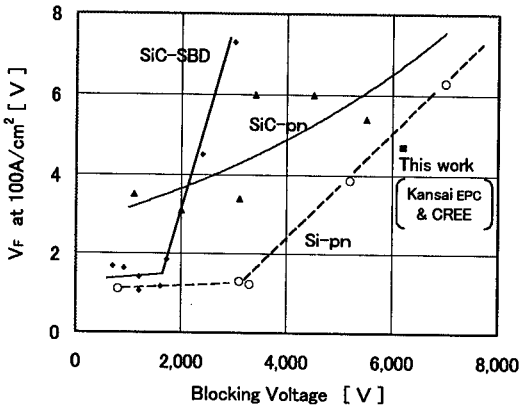

Fig.6 Trade-off between blocking Voltage and VF of diodes.
(◆ : reported SiC-SBD ▲ : reported SiC-pn
■: SiC-pn in this work ○:Si-pn)

4. Conclusions

The SiC pin diode with improved termination, mesa JTE, has been developed. The suitable mesa angle and impurity concentration of mesa JTE for achievement of high blocking voltages have been simulated to be 80 degrees and 2.5 x10^{17}cm^{-3}, respectively. The developed diode has a new record high blocking voltage of 6.2 kV, a low V_F of 4.7 V at 100A/cm^2, and a short trr of 28.5ns. Additionally, it has an excellent trade-off between the blocking voltage and V_F superior to the trade-off of the commercialized Si pin diodes.

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Materials Science Forum Vols. 338-342 (2000) pp. 1375-1378

Theoretical and Experimental Study of 4H-SiC Junction Edge Termination

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Keywords: Diode, Epitaxial Guard Ring, GTO, Modified Junction Termination Extension

Abstract This paper focuses on the study of 4H-SiC junction edge termination by way of numerical simulation using ISE-TCAD software. A modified junction termination extension, which uses a single step ion implantation and multiple dry etches, is presented. Simulation results show that near ideal breakdown voltage can be reached by a practical two-step dry etch. The breakdown voltages of our pin diodes with a 13μm-thick $9.7\times10^{15}cm^{-3}$-doped base, a two-step MJTE of etched depths of 0.4μm and 0.44μm and 0.7μm-deep $2.0\times10^{18}cm^{-3}$-doped junction, achieve 1680V, which approaches 96% of the breakdown voltage of corresponding ideal parallel junction. Guard rings formed by an epitaxial layer instead of ion implantation for GTO edge termination is studied. Devices with these two protection techniques are fabricated and the experimental results are reported.

Introduction In recent years, silicon carbide (SiC) has received increased attention as a material for use in high-temperature high power devices due to its superior properties such as high thermal conductivity, high breakdown field, wide bandgap and high saturated electron drift velocity [1]. For a power device, one of its most important characteristics is the high reverse blocking voltage. In general, the breakdown will occur at the edges of the junction due to the electric field crowding at the edges of the junction. Field crowding makes the reverse blocking voltage much smaller than that of the ideal parallel-plane junction. Hence, the protection of the junction edge becomes an important issue in the design of SiC power devices. Several techniques, such as MESA, floating guard rings, junction termination extension (JTE), and field plate have been studied for junction protection in SiC technology [2]. The present paper focuses on the design and optimization of floating guard rings and JTE. A modified JTE and an epitaxial floating guard ring are presented. To understand how these methods affect the breakdown voltage and to optimize the design using these methods, we have performed simulation using ISE, Inc.'s DESSIS SiC module. All of the simulations are done at 300K. The edge-termination of the fabricated devices in the experiment has been optimized by way of simulation.

Modified Junction Termination Extension (MJTE) Multi-step and multi-zone implantation with two or three different doses has been used successfully in the fabrication of planar implanted 4H-SiC pin diodes. It may be desirable, however, to create the p^+ anode or the p region in a merged pin Schottchy barrier diode (MPS) and the p layer for JTE purpose by a single step ion implantation. This is possible if an accurately controlled amount of acceptor charges near the surface is removed by dry etch [3]. Except for epitaxial layers, however, it is very difficult to achieve such high degree accuracy required for JTE to be effective because of

the uncertainty in the exact acceptor activation efficiency in SiC and the possible redistribution of acceptors after high temperature annealing. Hence, it is highly desirable that an MJTE such as the one shown in Fig.1 along with more realistic doping profile of Fig.2 determined by SIMS studies be investigated so that a more practical procedure can be developed for the fabrication of planar single-step implanted SiC pin and MPS diodes. Fig.3 shows the breakdown voltage as a function of the etch depth. For a given junction doping profile, the etched depth is the main parameter affecting the breakdown voltage. From Fig.3, it is seen that near ideal breakdown voltage (approaching 99% of the breakdown of corresponding ideal parallel-plane junction) can be reached by a practical two-step dry etch. Fig.4 shows the high

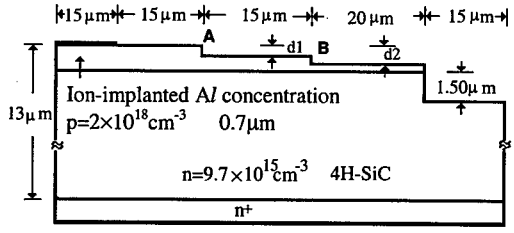

Fig.1 The structure and dimensions of the pin diode with two-step MJTE

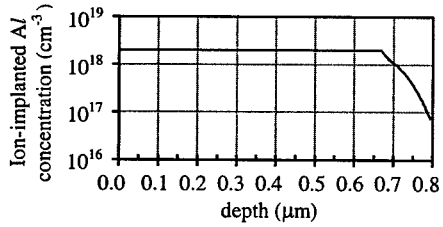

Fig.2 The ion-implanted Al concentration profile in the main junction of the pin diode shown in Fig.1.

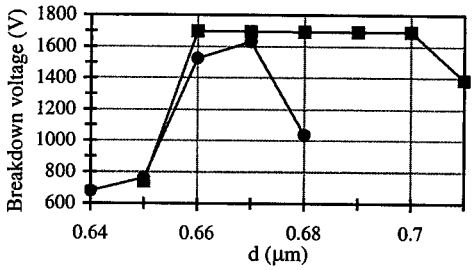

Fig.3 The breakdown voltage of pin diodes shown in Fig.1 as a function of the etch depth. • d1=d2=d ■ d1=0.64μm, d2=d

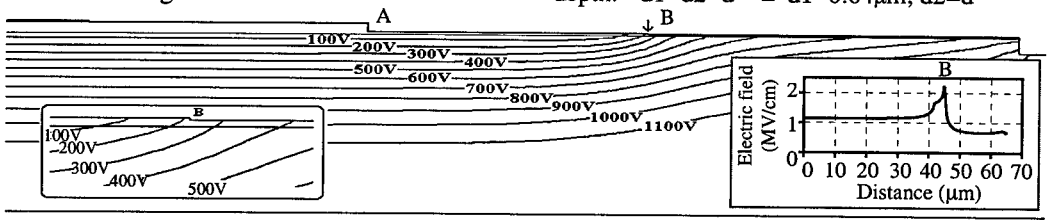

Fig.4 The electric potential distribution at 1200V reverse bias. The electric field at 0.7μm under the main junction surface of the diode is shown in the insert (2). The dimension and doping of the diode is shown in Fig.1. d1=0.64μm d2=0.68μm

efficiency of MJTE in spreading the equipotential lines near the edge of the junction. This technique can also be used practically in the fabrication of Schottky and MPS diodes. We have fabricated 4H-SiC MPS diodes and pin diodes protected by MJTE. The breakdown voltages reach 1267V for our pin diodes, which have a 13μm-thick $9.3\times10^{15}cm^{-3}$ -doped base, a one-step MJTE with etch depth of d1=d2=0.14μm and 0.35μm-deep $2.0\times10^{18}cm^{-3}$ -doped junction. This voltage approaches 84% of the maximum breakdown voltage obtained by simulation for corresponding diodes with one-step MJTE. And the breakdown voltages of our 1mm diameter pin diodes, which have exactly the structure and cross sectional view of Fig.1 with the two-step MJTE etch depths of d1=0.4μm and d2=0.44μm, reach 1680V as shown in Fig.5, which approaches 96% of the breakdown voltage of the corresponding ideal parallel junction. Note that the simulated breakdown voltage for this device is low, only 620V (shown in Fig.5, with 100% implantation activation efficiency). This may be due to the uncertainties in implantation

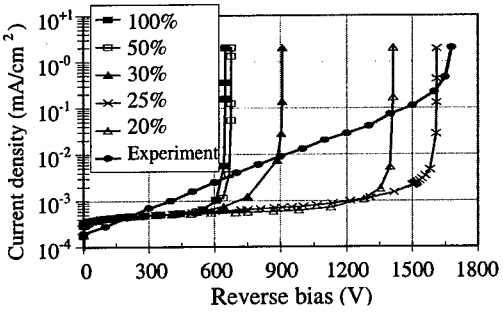

Fig.5 Reverse J-V curve of pin diode shown in Fig.1 at different implantation activation efficiency with d1=0.4μm, d2=0.44 μm.

Table 1. The breakdown voltage of 30μm-thick $1.5\times10^{15}cm^{-3}$-doped pin diodes with 12 guard rings

Diode	Ring Spacing (μm)	Experiment Ir(μA)/Vbr(V)	Simulation Vbr (V)
1	2.0	0.9/1440	1300
2	2.5	-	2000
3	3.0	9.8/2047	2760
4	3.5	-	2258
5	5.0	1.8/1150	1300
6	7.0	1.3/850	1030
		Ring width (μm)	
7	3.0	3.0	2596
8	3.0	4.0	2633
9	3.0	6.0	2714
10	3.0	8.0	2760

Note: Ir is the reverse current at Vbr.

activation efficiency in our diodes as well as the assumption of zero surface charge. The experimental J-V curve and simulated J-V curves for the pin diodes of Fig.1 with d1=0.4μm and d2=0.44μm and different assumptions on the implantation activation efficiencies are shown in Fig.5. It is clearly seen the implantation activation efficiency has a great effect on the breakdown voltage.

Floating Guard Rings Ion implantation guard rings can be used to provide effective edge termination as shown by simulation in Fig.6 and Fig.7 for a p^+in diode with a 30μm-thick and $1.5\times10^{15}cm^{-3}$-doped base and 12 rings of 8μm wide, 0.8μm deep and 3μm apart. It is a very challenging process in reality, however, especially when used in SiC GTO fabrication. We have fabricated floating guard rings terminated pin diodes. The experimental results and simulation results are summarized in Table 1. The discrepancies between experimental results and simulation results are most likely due to the effects of surface charge. From Table 1, it can be seen that the breakdown voltage is sensitive to ring spacing, but not to ring width, as expected.
A much easier approach for terminating the blocking pn junction in a GTO is to etch the n-type epitaxial layer in the GTO to form epitaxial guard rings (EGRs). As shown in Fig.8, the EGRs can be formed by a single dry etch which generally leads to a surface quality much superior in comparison to implanted guard ring surfaces. Computer modeling has been done for the GTO shown in Fig.8 with a uniformly distributed oxide charge of $3\times10^{11}cm^{-3}$ assumed in the LPCVD oxide. The model result shows a breakdown voltage of 1760V. We have also fabricated GTOs

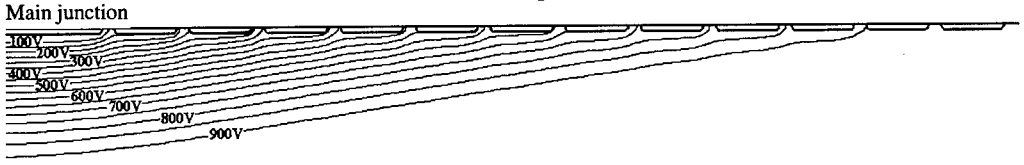

Fig.6 The potential distribution in the diode with 12 guard rings at 1000V

with the same cross sectional view and doping concentrations as shown in Fig.8 by using 12 EGRs, a maximum blocking voltage of 1200V has been measured. To qualify the dependence of breakdown voltage of EGR-terminated pn junctions, a detailed simulation has been done for a 13μm-thick, $p^-=5\times10^{15}cm^{-3}$ np^- diode. Fig.9 shows the equipotential lines of the np^- junction with EGRs and without EGRs, indicating effective edge termination. The simulation results are presented in Table 2. 67% of the breakdown voltage of the ideal parallel plane junction can be

reached by this technique assuming zero surface charge density. The breakdown voltage is sensitive to ring space, but not to ring width. The simulation results show that EGR is as effective as implanted guard ring for GTO edge termination, but EGRs are easier to form with high surface quality.

Conclusion Simulation results show that MJTE and EGR are effective technique for the protection of the junction edge of high power SiC devices. The experimental results confirm this point and also show they are more practical procedures in the fabrication of high power SiC devices. However, the influence of MJTE and EGR is not so clear, many uncertainties such as the implantation activation efficiency, the exact value of critical electric field and the epitaxial layer parameters make simulation results different from experimental results, more experiments are needed to optimize the design of MJTE and EGR.

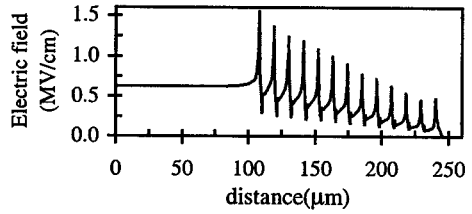

Fig.7 The electric field distribution beneath the surface of the diode with 12 guard rings at 1000V.

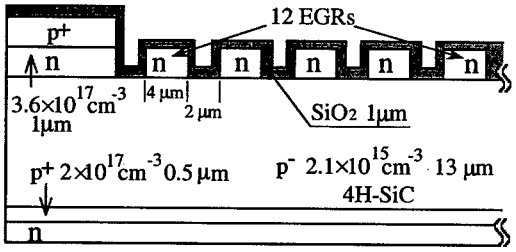

Fig.8 Schematic cross sectional view of 4H-SiC GTO with the EGRs.

Table 2. The breakdown voltage of 13μm-thick and $5\times10^{15}cm^{-3}$-doped np^- 4H-SiC diodes with 15 epitaxial guard rings. The depth of n region=1μm.

Diode	Ring Spacing (μm)	Ring Width (μm)	Simulation Vbr(V)
Ideal parallel-plane diode			2268
Without EGRs			417
1	1.0	4	852
2	0.75	4	1207
3	0.5	4	1515
4	0.5	2	1402
5	0.5	4	1515
6	0.5	6	1513

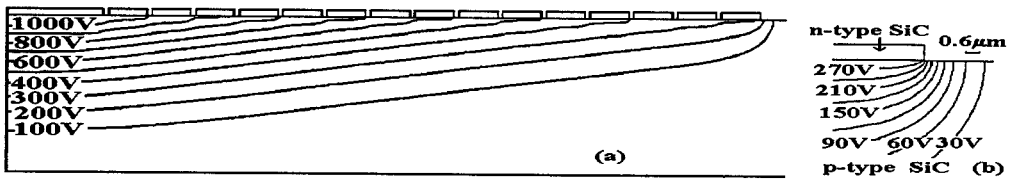

Fig.9 The potential distribution in a 13μm-thick and $5\times10^{15}cm^{-3}$-doped np^- diode.
(a) With 15 EGRs under 1148V reverse bias. Ring spacing=0.5μm, ring width=4μm.
(b) Without EGRs under 300V reverse bias.

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Materials Science Forum Vols. 338-342 (2000) pp. 1379-1382

Monte Carlo Simulation of 4H-SiC IMPATT Diodes

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Keywords: Electron-Hole Transport, Impact Ionization, Millimeter Wave Generation

Abstract The electron-hole transport including impact ionization and millimeter wave power generation in 4H-SiC has been studied by the Monte Carlo Particle technique. The model of 4H-SiC consists of three electron and two hole bands. The millimeter wave power generation is investigated in p^+-n-n^--n^+ 4H-SiC IMPATT diodes operating in parallel resonant circuit. It will be shown that 4H-SiC offers the potential to generate millimeter wave power over several watts at around 200 GHz.

Introduction

It is well known that at a given frequency the microwave output power of an IMPATT diode is proportional to the square of the product of semiconductor critical field and carrier saturation velocity. It is also well known that heat generation and dissipation in IMPATT diodes can severely limit the performance of IMPATT diodes. SiC is, therefore, an ideal semiconductor for IMPATT diodes because SiC offers (i) a 10 times higher critical field, (ii) a 2 times higher carrier saturation velocity, and (iii) a 3 times higher thermal conductivity, in comparison to that of Si. These properties can lead to high performance IMPATT diodes for microwave and millimeter wave applications. Because of the uncertainty in the high field drift velocity and other quantities needed for the modeling of IMPATT diodes using drift-diffusion approach, the Monte Carlo Particle (MCP) simulation becomes very attractive, as it requires no assumptions of field and time (which becomes important at millimeter wave frequencies) dependencies of diffusion coefficients drift velocities, ionization coefficients, and other average quantities. Moreover, the nonlocal field effects which are possible at millimeter wave frequencies are naturally accounted for in MCP simulation. The input parameters for MCP simulations are the band structure of material and carrier scattering rates by phonons and impurities. Most of these parameters can be found in recent publications [1,2,3,4]. In this paper, we present the first attempt to investigate the millimeter wave power generation in 4H-SiC IMPATT diode using a standard parallel resonant circuit.

4H-SiC IMPATT diode model

The 4H-SiC band structure for holes and electrons is taken from [1]. Electron band structure consists of three nonparabolic bands: first, second, and third with the nonparabolicities of 0.323, 0.45, and 0.2 eV^{-1}, respectively. The energy gaps between first and second bands and between first and third bands are 0.122 and 2eV, respectively. The effective masses along x, y and z-axes (z-axis assumed to be in parallel with the 4H-SiC principal c-axis) are (0.31; 0.57; 0.28), (0.71; 0.78; 0.16), and (2.0; 0.5; 0.2) for first, second, and third bands, respectively. Structural

anisotropy is included in the model. Electron scattering by acoustic phonons, polar optical phonons, zero and first order intervalley phonons, and ionized impurities is also included. For the interband transitions and scattering between equivalent valleys, the zero and first order phonon and interaction potentials are assumed to be the same for each band. The phonon energies and interaction potentials are taken from [3]. Impurity scattering is accounted for using Ridley's third body exclusion theory. The hole band structure consists of two parabolic bands, the first and the third bands with an energy gap of 0.1eV between the bands. The effective masses in directions perpendicular and parallel to the c-axis are (0.59; 1.56) and (1.49; 0.21) for the first and the third bands, respectively. The second band is not accounted for in the simulation because the effective masses of the second band are equal to that of the first band and the gap between the bands is only a few meV[1]. The hole scattering by acoustic phonons, polar optical phonons and ionized impurities is taken into account. The scattering parameters are set the same as for electrons. Additionally, nonpolar optical scattering is introduced with interaction potential of 3.5×10^{9}eV, which is close to that for 3C-SiC[4]. The interband transitions due to the acoustic, polar and nonpolar optical scattering are also accounted for. The impact ionization is accounted for by using Keldysh formula [5] with the threshold energy equal to 1.25 times of 4H-SiC band gap. This formula has one dimensionless fitting parameter P, which measures the softness of the threshold. The best fit to experimentally measured [6] impact ionization coefficient α_p for holes gives the softness P_h=0.0025 (see Fig. 1). For electrons we set P_e=1.3, which gives lower value of α_n than for holes in view of the experimental fact that carrier multiplication in 4H-SiC in the direction parallel with c-axis is hole initiated. The electron lifetime is chosen to be τ_{n0} = 40ns and the hole lifetime is determined by the relation of $\tau_{n0} = 5\tau_{p0}$ often used for silicon. The Auger recombination coefficient is assumed to be the same for electrons and holes and is set to be C_n

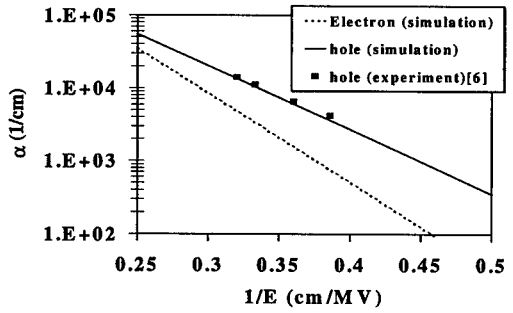

Fig.1 The electron and hole impact ionization coefficient dependencies on electric field in 4H-SiC in direction parallel to c-axis.

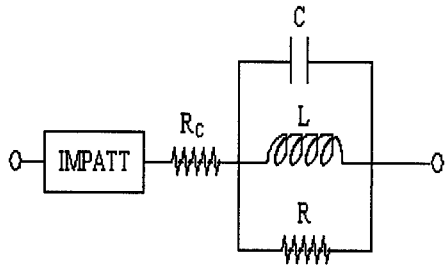

Fig.2 Circuit used in the MCP simulation. R_c (=ρ/area) represents the anode contact resistance.

$=C_p=10^{-28}$cm^6/s. Millimeter wave power generation in a parallel resonant circuit is performed by MCP simulation through the simultaneous solutions of coupled Boltzmann, Poisson and circuit equations. The simulated IMPATT diode has a hi-lo structure of p^+-n-n^--n^+ with the corresponding dimensions of 0.020-0.08-0.17-0.015 μm where n = 5×10^{18}cm^{-3}, n^- =10^{16}cm^{-3}, and the crossectional area is 1000 μm^2. Specific contact resistance to the anode is set to be either ρ=10^{-6}Ωcm^2 or ρ=10^{-5}Ωcm^2. In the simulations, the IMPATT diode is connected with the circuit elements as shown in Fig.2. The circuit parameters for power generation at 200GHz are capacitance C = 3.01pF, inductance L = 0.2 pH, load resistance R = 50Ω. The contact resistance is accounted for in the circuit as a resistor R_c. In all the calculations field is applied in parallel with c-axis of 4H-SiC. The simulations are performed at 300 K temperature. The number of simulated particles, depending on the case, varies between 5000 and 40000. The time step in all cases is 0.5fs. Such a short time step is needed for the correct account of the possible plasma

effects in highly doped cathode and anode regions and of the carrier multiplication due to impact ionization, especially at the avalanche breakdown conditions.

Results and discussion

The simulated impact ionization coefficient dependencies on electric field in 4H-SiC are shown in Fig. 1. A good agreement with the experimental data on hole impact ionization coefficient is obtained. The electron drift velocity (see Fig.3, solid line) at 400 kV/cm has a maximum of 1.83×10^7cm/s which coincides with Monte Carlo simulations using two-band model [2]. The hole saturation velocity from our model is equal to 0.84×10^7cm/s (see Fig. 3, dashed line). Carrier energy dependencies on field are presented in Fig. 4. The hole energy due to a heavy

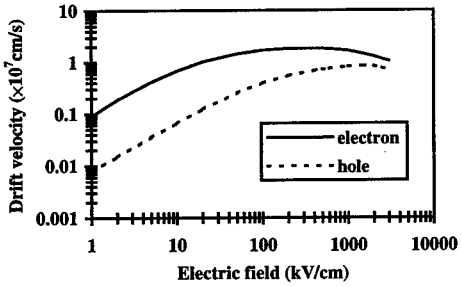

Fig.3 Simulated electron (solid line) and hole (dashed line) drift velocity dependencies on electric field in 4H-SiC in direction parallel with c-axis

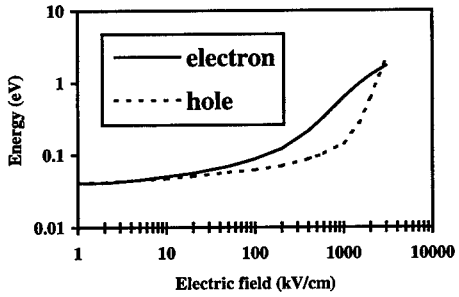

Fig.4 Simulated electron (solid line) and hole (dashed line) energy dependencies on electric field in 4H-SiC in direction parallel with c-axis

mass in the first band increases very slowly with the field. The fast rise of hole energy starts over the fields of 1 MV/cm, when the third band with much lower hole mass in c-directions becomes considerably populated. The electron energy dependence on field is close to that of two-band model [2]. The IMPATT diode simulation results for different specific contact resistance are presented in Figs. 5 and 6.

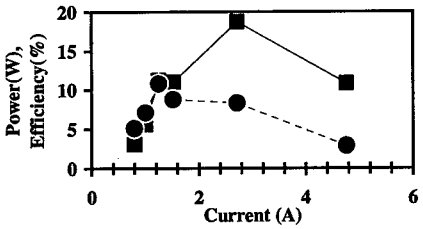

Fig.5 The generated power (solid line) and efficiency (dashed line) dependencies on current in IMPATT diode operating in parallel resonant circuit at 200GHz. The diode anode specific contact resistance is assumed to be $10^{-6}\Omega cm^2$

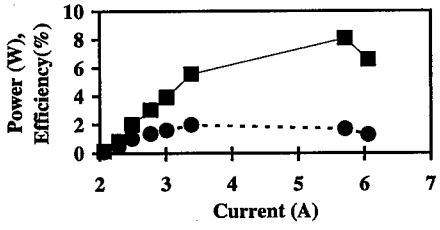

Fig.6 The generated power (solid line) and efficiency (dashed line) dependencies on current in IMPATT diode operating in parallel resonant circuit at 200GHz. The diode anode specific contact resistance is assumed to be$10^{-5}\Omega cm^2$

In Fig.5 the generated power (solid line) and conversion efficiency (dashed line) are plotted as a functions of current for an anode specific contact resistance of $\rho=10^{-6}\Omega cm^2$. The data points in Fig.5 correspond to the IMPATT diode DC-biased from 72 to 77V with a step of 1 V from low current point to high current point. At the power peak of 18 W the amplitude of voltage oscillations on the 50Ω load resistance becomes strongly modulated due to the resonance between circuit and IMPATT diode characteristic frequencies. After this point power and efficiency decreases with increasing current. The resonance effect is more pronounced in Fig.6

where a larger specific contact resistance of $\rho=10^{-5}\Omega cm^2$ is used. In this case the IMPATT diode bias is changed from 78 to 85 V with a step of 1 V from point to point. The voltage oscillations on load resistance are nearly harmonic at the low currents before the resonance point at 5.8A. At high currents beyond the resonance point the oscillations become modulated and noisy. With the low contact resistance, a high power of 11W with an efficiency of 10% at 200GHz can be generated in harmonic oscillation region (See Fig.5). The increased contact resistance considerably reduces efficiency and power. Nevertheless, at $\rho=10^{-5}\Omega cm^2$, it is still possible to get more than 5W power with 2% efficiency in harmonic oscillation region (see Fig.6). Because of the uncertainty in electron ionization coefficient, the same IMPATT diode in the same circuit is also simulated by neglecting the electron impact ionization so that the effect of electron ionization coefficient can be determined. The generation threshold voltage is found to increase by 50%, while the other power generation parameters show much less changes. Further work is underway to quantify the effects of electron impact ionization.

Conclusions

4H-SiC model with three electron bands and two hole bands has been developed for Monte-Carlo simulation of high field transport in 4H-SiC. The model is validated by comparison with the most recent experimental hole impact ionization coefficients and with full-band Monte-Carlo simulation results. The 4H-SiC IMPATT diode simulation shows the high potential of this material for 200GHz frequency millimeter wave power generations. The simulated diode can deliver 11W power with 10% efficiency if the specific contact resistance ρ is equal to $10^{-6}\Omega cm^2$, and 5W power with 2% efficiency for $\rho=10^{-5}\Omega cm^2$.

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Materials Science Forum Vols. 338-342 (2000) pp. 1383-1386

Demonstration of High Performance Visible-Blind 4H-SiC Avalanche Photodiodes

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Keywords: Avalanche Photodiodes, Photoresponsivity, Response Speed, UV Detectors, Visible-Blind

Abstract 4H-SiC visible-blind reach-through avalanche photodiodes (RAPDs) are designed and fabricated with mesa edge termination and thermal oxide passivation techniques. The devices show a "hard" avalanche breakdown with a positive temperature coefficient, a wide spectral range (285nm to 360nm) with higher than 100A/W photoresponsivity, and a peak photoresponsivity of 738A/W at 320nm. The visible-blind rejection ratio, defined as the maximum responsivity divided by the responsivity at 400nm, has a maximum value of about 2500 at 93.9V reverse bias. The APD photoresponse speed is studied and a fall time of 4.0ns is measured.

Introduction

Visible-blind detectors are highly desired over other non-visible-blind detectors in applications such as UV astronomy, flame sensors and missle detection systems. Avalanche photodiodes (APDs) are the only semiconductor photo-detectors that can provide both high gain and high speed. However, they may also give a high noise figure due to the random nature of the avalanche process. It is well known that the noise figure can be minimized with either a very large or very small k, defined as the ratio of hole/electron ionization rates. Among the semiconductors suitable for the visible-blind or near visible-blind ultra-violet (UV) detection, SiC is the only one which has a very large k [1]. In contrast, GaN has a k value very close to unity, just like other III-V compound semiconductors [2]. Therefore, SiC has an unmatched advantage for hole-initiating APD application over GaN.

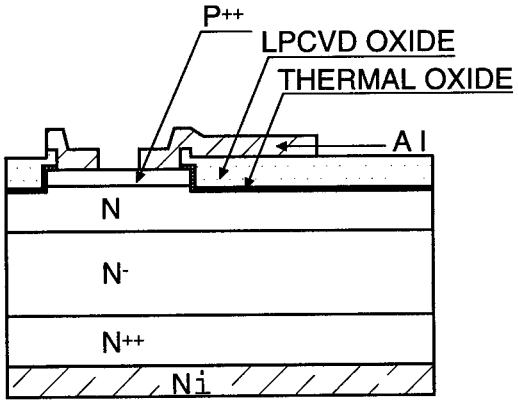

Figure 1 The cross-sectional view of 4H-SiC RAPD

The first 4H-SiC APD has been demonstrated with a maximum responsivity of 106A/W in deep avalanche [3]. In this paper, we will present the design, fabrication, and characterization of the 4H-SiC APDs and also report the latest results. It will be shown that the maximum photoresponsivity as high as 738A/W can be obtained and the visible-blind rejection ratio as high as about 2500 can be achieved. Besides, the response speed is studied and a fall time of 4.0ns will be reported.

Device Design and Fabrication

An n^+ substrate based, hole-initiating p^+-n-n^--n^+ RAPD device structure is chosen in order to have both a relative thin multiplication layer and a wide photon absorption region. The layers from the top to bottom in the p^+-n-n^--n^+ RAPD structure are designed respectively for the purpose of p^+ ohmic contact formation, multiplication, photon absorption and n^+ ohmic contact (See Fig.1). The critical parameters for the p^+-n-n^--n^+ 4H-SiC RAPDs are the doping concentrations and thicknesses of the n and n^- layers. One design objective of the n^- layer is to make this layer totally depleted at the desired RAPD operating voltage so that the n^- layer can become active in sweeping photo generated carriers. Therefore, its doping concentration should be as low as possible. Another design objective is to control the RAPD's operating voltage to be within 100V. There is obviously a trade-off in the maximum achievable photo response and the operating voltage because a thinner n^- layer leads to a lower photo absorption. Considering the maximization of the photoresponse at around 320nm and the voltage limitation in the RAPD operation, the n layer is designed to be 0.4μm in thickness and $5x10^{17}/cm^3$ doped. The n^- layer is designed to be 1μm and doped as lightly as possible. The thickness of p^+ layer is designed to be 0.4μm. 4H-SiC wafers with the designed structure were purchased from Cree Research, Inc. The actual n layer doping concentrations for two different wafers are $5.4x10^{17}/cm^3$ and $5.7x10^{17}/cm^3$.

To fabricate the 4H-SiC RAPDs, a 0.6μm deep mesa was first etched by the inductively coupled plasmas (ICP), followed by a one-minute *in situ* "cleaning" at a substrate dc bias of -50V as described in Ref. [4]. A 50nm oxide was then grown by wet thermal oxidation at 1100°C for 4 hours, followed by 1μm LPCVD SiO_2 deposited at 900°C. After that, oxide windows were opened to reach the p^+ layer and 100nm aluminum and 100nm titanium were sputtered on the p^+ side and defined by the standard lift-off technique. Next, the aluminum at the center of the mesa was etched to form optical windows and 200nm nickel was sputtered on the back. Both p-type and n-type ohmic contacts were annealed at 1050°C for 10 minutes in N_2 forming gas. Finally, 300nm Al overlayer was sputtered and wire bonding patterns were formed by photolithography. RAPDs with four different sizes were fabricated. The sizes of the devices are $35x35\mu m^2$, $60x60\mu m^2$, $85x85\mu m^2$ and $100x100\mu m^2$, and the corresponding optical windows are $17x17\mu m^2$, $32x32\mu m^2$, $57x57\mu m^2$, and $62x62\mu m^2$, respectively.

The I-V properties of RAPDs fabricated on two different wafers are tested. The breakdown voltages for $5.4x10^{17}/cm^3$ and $5.7x10^{17}/cm^3$ doped wafers are 93V and 78V, respectively. They are in good agreements with theoretical prediction [5].

The temperature-dependent I-V characteristics of 4H-SiC RAPD are measured up to 257°C as shown in Fig.2, and a positive temperature coefficient of breakdown voltage of 0.016V/°C is observed, which is a strong evidence that a uniform avalanche breakdown has been realized.

Characterization of 4H-SiC APD

The photo response spectra of RAPDs are measured by a computer controlled system, which consists of a power source with 150W UV enhanced Xe lamp, a monochromator with a 2400g/mm grating blazed at 240nm and optimized for 200nm to 450nm wavelength region, an optical chopper, a UV microscope objective with a spot size smaller than 50μm, an XYZ translator, a current pre-amplifier, a power supply for the RAPD, and a lock-in amplifier. The power of the UV light illuminating on the RAPDs is calibrated by a UV-enhanced Si photodiode detector calibrated from 200nm to 1000nm.

The best photoresponsivity results are obtained on the RAPDs fabricated on $5.4x10^{17}/cm^3$ n-doped wafer with a device size of $35x35\mu m^2$ and an optical window of $17x17\mu m^2$. The photoresponsivity spectra at different reverse biases are shown in Fig.3. It is clearly seen that the photoresponsivity increases from about the order of 10^{-3}A/W to the order of 10^2A/W as the bias increases from 0V to 94.6V. The photoresponsivity at 94.6V has a maximum of 738A/W at 320nm,

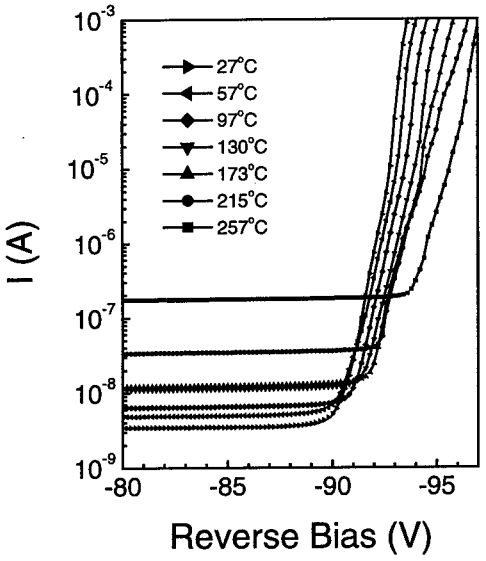

Figure 2 Temperature-dependent I-V characteristics of 4H-SiC RAPDs

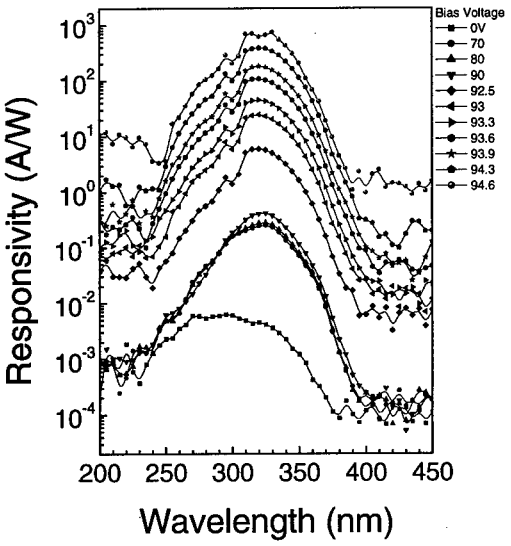

Figure 3 Photoresponsivities measured at different reverse biases

which is more than three orders of magnitude higher than that of conventional 6H-SiC p-i-n photodiodes [6] and GaN p-i-n photodiodes [7]. The high response spectra are wide, ranging from 285 to 360nm with responsivities higher than 100A/W.

The maximum responsivity vs. bias voltage is shown in Fig.4. At 0V bias, the maximum photoresponsivity is about $6x10^{-3}$ A/W. It is about 0.2A/W at 70V and is doubled at 90V. However, at 94.6V, the maximum photoresponsivity increases by three orders of magnitude as a result of the avalanche multiplication.

The visible-blind rejection ratio is evaluated by dividing the maximum photoresponsivity and the photoresponsivity at 400nm. The maximum rejection ratio is as high as about 2500, which is

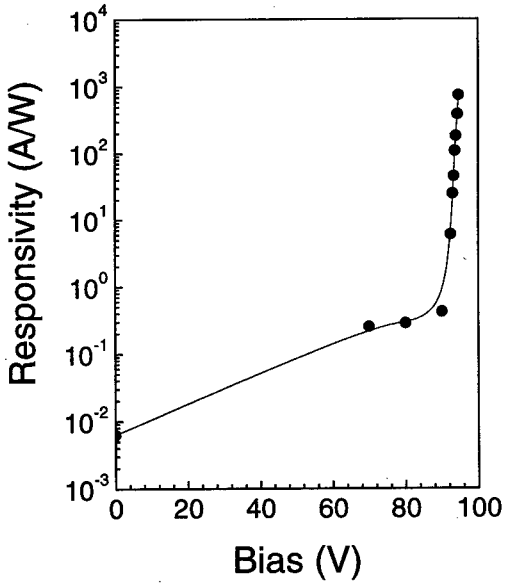

Figure 4 The maximum photoresponsivity vs. reverse biases

much larger than the same rejection ratio obtained from 6H-SiC p-i-n diode, which is only about 30 [6], and that from GaN p-i-n diode of about 1000 [7], even though bandgap of GaN is larger than that of SiC.

RAPDs from the second wafer doped $5.7x10^{17}/cm^3$ are wire-bonded for detector speed measurements. RAPDs from this wafer typically have an avlanche breakdown voltage around 78V. Fig.5 shows the temporal response measured from a typical RAPD reverse biased at 77V. It is seen that the RAPD has a very quick response and the fall time is only 4ns. This is the fastest response ever reported for visible-blind UV detectors.

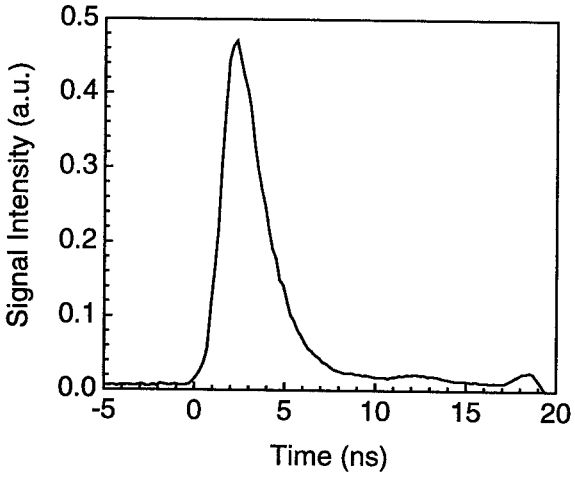

Figure 5 Temporal response of 4H-SiC APD reverse biased at 77V

Summary

In summary, we have demonstrated greatly improved 4H-SiC RAPDs. Photoresponsivity as high as 738VA/W at λ=320nm has been achieved. It has been shown that 4H-SiC RAPDs have excellent visible-blind rejection ratios with a maximum of about 2500 at 93.9V reverse bias. 4H-SiC RAPDs have also shown a high speed response. The fall time is measured to be in the range of around 4ns, the fastest ever reported for visible-blind UV photodiodes. Furthermore, SiC APDs show their potential to work at temperatures up to 257°C.

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Materials Science Forum Vols. 338-342 (2000) pp. 1387-1390

2600 V, 12 A, 4H-SiC, Asymmetrical Gate Turn Off (GTO) Thyristor Development

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Keywords: GTO, High Temperature, JTE, Power Devices, Switch, Thyristors

Abstract: We report on a 2 mm diameter, 4H-SiC, asymmetrical Gate Turn Off (GTO) Thyristor with a blocking voltage of 2600 V and a forward current of 12 A – the highest reported power handling capability of 31 kW for a single device in SiC. Furthermore, the 1 mm diameter devices showed a forward blocking voltage of 3100 V. The 5-epilayer structure utilized a blocking layer that was 50 μm thick, p-type, doped at about 7-9x10^{14} cm^{-3}. The devices were terminated with a single zone Junction Termination Extension (JTE) region formed by ion-implantation of nitrogen at 650°C. The devices required less than 10 mA gate current to turn-on when blocking 2000 V between anode and cathode.

Introduction: The first symmetrical (blocking in both directions) SiC Thyristors were demonstrated by Cree [1]. These early devices blocked 700 V with a rated current of 6 A at a forward drop of 3.9 V – an impressive result. The devices were made on n^+ 4H-SiC substrates resulting in an npnp structure which is inverse of the conventional pnpn structure used in the silicon technology. This is necessary in SiC because the resistance of the p^+ substrates is very high. Subsequently, other researchers have built on this early work and have produced asymmetrical (blocking in only one direction) npnp devices [2-5]. The limitations on epilayer thickness and the device footprint have generally limited these results to 1000 V and several Amps. In this work, we report on asymmetrical GTO thyristors with 2600 V forward blocking and up to 12 A of forward current from a single 2-mm diameter cell. We have also demonstrated a forward blocking voltage of 3100 V in a 1 mm diameter cell. The forward blocking voltage has been increased by increasing the blocking layer thickness to 50 μm. Despite the high thickness of the blocking layer, the thyristors turn on with relatively low gate current (10 mA) and with a relatively low forward drop of 6.5 V indicating that the ambipolar life-time under high level injection condition in the thick blocking layer is of the order of 1-2 μs.

Silicon Thyristors and GTO's are currently used in only very high power applications where silicon IGBT's are not available. However, the recent development of a hybrid MOSFET Turn-Off Thyristor (MTO™) has been very successful in medium power applications requiring switching of >4000 V and >100 A [6]. The hybrid MTO™ consists of a silicon GTO and several MOSFET chips attached to the periphery of the GTO between the gate and the cathode terminals of the GTO. The MOSFETs are used to help turn-off the GTO after it has been turned-on. This approach overcomes the issue of a large gate drive required to turn the GTO off. The advantage of the hybrid approach lies in the fact that the high power GTO and the low power MOSFET can be independently optimized and separately processed. The separate processes can have much higher yield as compared to the integrated approach.

Device Structure: Fig. 1 shows a simplified cross-section of the device. The five epilayers were grown at Cree on 8° off-axis 4H-SiC, n-type, 15 mils thick, substrates with a resistivity of 0.020 ohm•cm. The first two n and p type buffer layers are typically a few microns thick, doped such that the injection efficiency of the np junction is high. The purpose of the p buffer layer (second layer) is to block the spread of the depletion region under forward blocking thus making the device asymmetrical. The third p^- layer is about 50 microns thick, doped at 7-9x10^{14} cm^{-3}, designed to work in punch-through mode under forward blocking. This layer is fully depleted at about 2000 V forward blocking voltage. The fourth layer (n) is designed to prevent punch-through under forward blocking. The topmost p^+ layer serves to inject holes when the anode-gate junction is forward biased. In order to turn-on this structure, it is very important to get a good injection efficiency in the top and bottom junction. The bottom n^+p junction (J_3) will always have a good electron injection efficiency because the p-buffer is partially ionized at room temperature. However, the top p^+n junction (J_1) can have low hole injection efficiency because the p^+ layer is only 2% ionized at room temperature with an acceptor doping of 1x10^{19} cm^{-3}. Thus, it is very important to grow the p^+ layer with a very high concentration of acceptors.

The n-type Junction Termination Extension (JTE) region is created by implanting nitrogen at 650°C to a total dose of about 8x10^{12} cm^{-2}. The gate and cathode contacts are formed by sintered nickel. Finally, the inter-digitated fingers are connected using 2 μm of gold. A photo-micrograph of a 2 mm diameter involute structure is shown in Fig. 2.

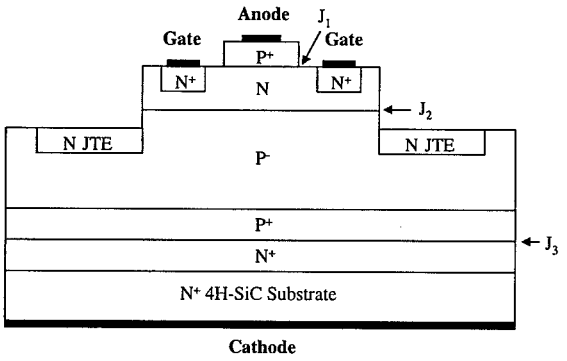

Fig. 1 Schematic cross-section of the asymmetrical SiC GTO Thyristor. The p^- blocking layer is 50 μm thick.

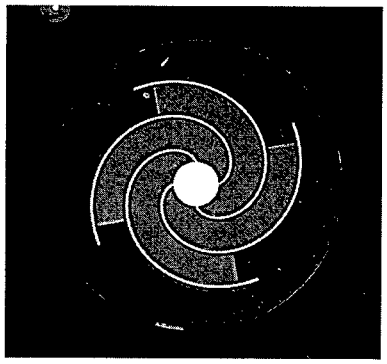

Fig. 2 Photo-micrograph of a 2 mm involute thyristor. The anode area is approximately 0.0167 cm^2 (~ 50% of the total cathode area).

The reverse blocking capability is minimal (~ 50 V) due to the presence of the p^+ buffer layer at junction J_3. It turns out that the typical PWM inverter systems need only asymmetrical switches. It is much easier to fabricate such devices as only one blocking junction (J_1) needs to be properly terminated. In our design, this junction is terminated by using a floating n-type JTE region. This enables the multi-cell approach on the same SiC wafer as small cells can be individually terminated.

Experimental Results: The 2-mm involute thyristors were immersed in Fluorinert with the anode grounded and the gate terminal floating. A negative voltage was applied to the cathode to determine the blocking voltage. The trace from the Tektronix 371 curve tracer is shown in Fig. 3 indicating that the forward blocking voltage is at least 2600 V. The device can be turned on by forward biasing the anode to gate junction. Fig. 4 shows the on-wafer probe measurements of the forward characteristics at room temperature for this device. To reduce the probe resistance, four probes to the anode were used. The device shows a forward current of 12 A at a forward voltage drop of 6.5

V. This results in a total power capability of about 31 kW. In order to further reduce the contribution to the forward drop from the probes and wiring, the measurements will need to be repeated on a packaged device.

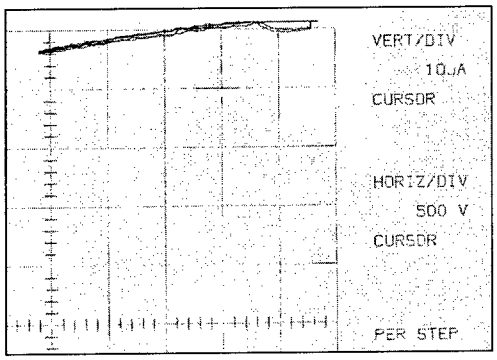

Fig. 3 The 2600 V forward blocking voltage of the 2-mm thyristor measured at room temperature in Fluorinert. The negative voltage was applied to the cathode while the anode was grounded with gate floating.

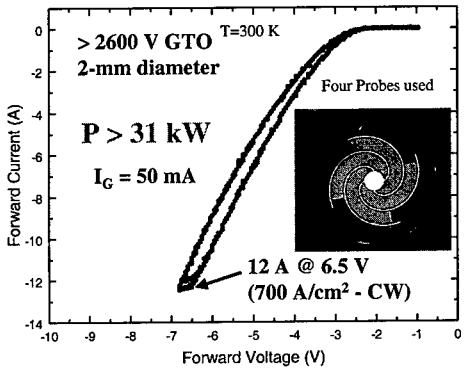

Fig. 4 The on-wafer probe measurements of the forward characteristics of the 2-mm thyristor measured at room temperature. The anode was grounded; the gate was forward biased to inject 50 mA with the cathode biased between 0 to – 6.5 V.

Fig. 5 shows a forward blocking voltage of 3100 V for a 1 mm circular device. The measurement was also taken in Fluorinert. This voltage is currently limited by the capability of the Tektronix 371 curve tracer. The variation of the breakover voltage with gate current for the larger 2 mm diameter device is shown in Fig. 6. It shows that less than 10 mA gate current is needed to turn on the device when it is blocking more than 2000 V. The holding current is between 80 to 100 mA. Fig. 7 shows the on-wafer probe measurements on the 2-mm diameter device as a function of temperature. During this measurement, a gate current of 50 mA was flowing through the forward biased anode-gate junction. The current density has been calculated based on the anode area, which is about 50% of the total cathode area. The reduction of forward drop with increasing temperature for a fixed current density is as expected.

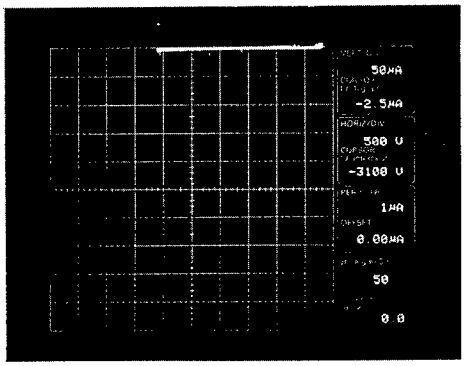

Fig. 5 The 3100 V forward blocking voltage of a 1-mm diameter thyristor measured at room temperature in Fluorinert. The negative voltage was applied to the cathode while the anode was grounded with gate floating.

Conclusions: 4H-SiC, 2 mm diameter, asymmetrical GTO's have been designed, fabricated and tested with blocking voltages up to 2600 V and forward current of 12 A at a forward voltage drop of 6.5 V resulting in the highest reported power handling capability of 31 kW for a single device in SiC. Furthermore, the 1 mm diameter devices blocked 3100 V. These devices utilized a p-type, 50 μm thick blocking layer, grown at CREE. Despite the high thickness of the blocking layer, the thyristors turn on with relatively low gate current (10 mA) and with a relatively low forward drop of 6.5 V indicating that the ambipolar life-time under high level injection condition in the thick

blocking layer is of the order of 1-2 μs. The devices were evaluated up to 300° without any degradation.

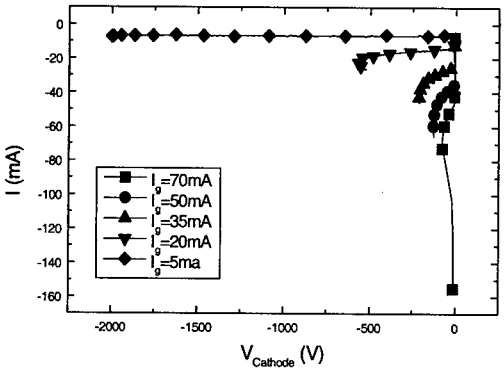

Fig. 6 The turn-on behavior of the 2 mm thyristor. The holding current is about 100 mA (6 A/cm^2)

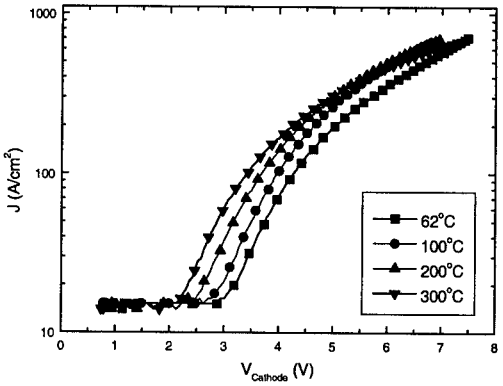

Fig. 7 The on-wafer probe measurements of current density (*wrt.* anode area) vs. the forward drop of the 2-mm thyristor at different temperatures. The maximum current density of about 700 A/cm^2 corresponds to 12 A.

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Factors Influencing the Design and Performance of 4H-SiC GTO Thyristors

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Keywords: Bipolar Junction Transistor, Current Gain, GTO Thyristor, Power Switching Device

Abstract: We investigate the static and dynamic performance of 4H-SiC GTO thyristors made on epitaxial layers grown on n+ substrates. The forward voltage drop is found to be 4.5 - 5 V measured at 100 A/cm^2 and 200°C and a forward blocking voltage of up to 1100 V is measured. A large forward drop at room temperature (12-15 V) is attributed to incomplete ionization and bandgap narrowing in the p+ anode. The transistor current gains inherent to the GTO thyristor are measured as functions of current and temperature. The fabricated devices show large turn-on gain and small turn-off gain, consistent with the comparable npn and pnp transistor current gains.

1. Introduction

Thyristors made from SiC have been pursued over the last several years because of the potential for lower forward drop, faster switching, higher blocking voltage, and higher operating temperature compared to silicon based thyristors [1-5]. Large-area, high-current handling thyristors have been achieved in silicon because of the availability of uniformly doped, ultra low defect material [6]. The continued improvement in silicon carbide material quality suggests that similar current handling capability will be possible in silicon carbide in the near future. This paper reports on the static and dynamic electrical characteristics of 4H-SiC GTO thyristors recently fabricated in the first phase of a project that aims to demonstrate high-voltage power devices capable of high-temperature operation. The fabricated devices show forward blocking voltages of up to 1100 V and typical on-state voltage drop at 100 A/cm^2 of 4.5–5 V at 200°C. GTO thyristor switching performance and transistor current gains are also measured as functions of temperature and current.

2. Device Fabrication

The structure of the fabricated GTO thyristor is shown in Fig. 1 where four epitaxial layers are grown on an n+ 4H-SiC substrate. The 12 μm p-type drift layer and the punchthrough buffer provide asymmetric blocking capability with a calculated parallel plane breakdown voltage of ~ 2200 V. The punchthrough buffer reduces the non-uniformity of the electric field in the drift layer and prevents punchthrough breakdown allowing higher blocking capability. The actual forward blocking capability of the GTO is limited by open-base breakdown and field crowding at the device edge. A three-zone junction termination extension (JTE) and a p+ field stop provide termination for these devices.

Two geometries are used to fabricate 800 μm, 1200 μm, and 2400 μm diameter devices. The concentric geometry shown in Fig. 2 incorporates concentrically arranged anode segments to increase the anode-gate periphery to allow for device turn-off. The involute geometry shown in Fig. 3 utilizes involute anode and gate fingers with constant anode to gate spacing along the segment. This geometry is expected to yield more uniform current spreading at turn-on but slower turn-off performance relative to the concentric design [7]. Both involute and concentric devices have anode segment widths of 20 μm.

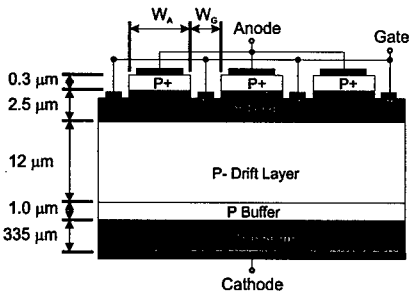

Fig. 1. Device cross-section of the fabricated GTO thyristor.

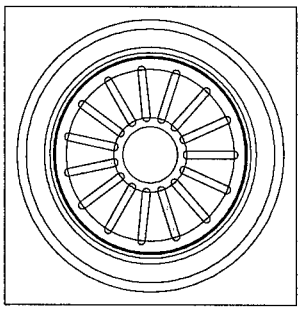

Fig. 2. Concentric GTO pattern (800 μm diameter).

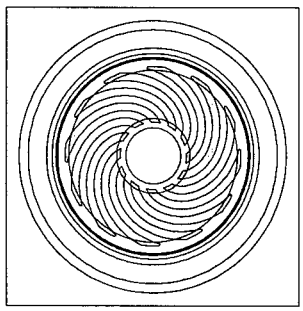

Fig. 3. Involute GTO pattern (800 μm diameter).

3. Electrical Characteristics

Measured forward characteristics of an 800 μm device are shown in Fig. 4 at 150 and 200°C. The simulated on-state voltage drop for these GTO thyristors at 100 A/cm^2 and 200°C is found to be 2.9 V when an ambipolar lifetime of 0.12 μs is assumed. Parasitic resistance has not been included in the simulations but must be accounted for when comparing measured and simulated results. The characteristics after subtracting the voltage drop due to the parasitic resistance are also shown in Fig. 4. The corrected forward voltage drop at 100 A/cm^2 is found to be 4.80 V at 150°C and 4.55 V at 200°C. There is an additional 1.5 - 2 V drop that is not accounted for by the parasitic resistance and may be caused by poor injection efficiency of the p+ anode or low conductivity modulation of the drift layer. At room temperature, these GTO's show large gate trigger currents (100-150 mA) and large on-state voltage drop (12-15 V). At higher temperatures, the carrier lifetime increases and acceptor ionization in the p+ anode increases allowing the device to turn on at moderate current levels (a gate trigger current of 2mA is measured at 250°C).

The reverse blocking characteristics of these devices have been measured up to 200°C and show leakage currents of ~ 10^{-6} A/cm^2 up to the blocking voltage. Characteristics for an 800 μm device are shown in Fig. 5 where a blocking voltage of 1000 V is achieved with low leakage current. For this measurement, the anode and gate are shorted and the current density is normalized to the area of the blocking junction. At 200°C, the leakage current increases by a factor of 3 and remains below 10^{-5} A/cm^2 until breakdown, two orders of magnitude lower than in previously reported GTO's[5]. The 800 μm devices show a blocking voltage of up to 1100 V, whereas the 1200 μm devices show a maximum blocking voltage of 600 V. The maximum blocking capability of a GTO thyristor may be limited by open-base breakdown, edge termination or defects. In these

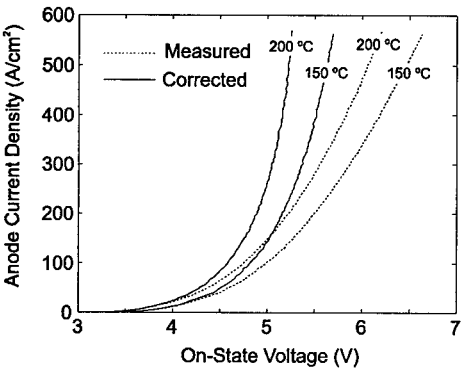

Fig. 4. GTO thyristor on-state characteristics. characteristics (anode area: 4.58x10^{-4} cm^2).

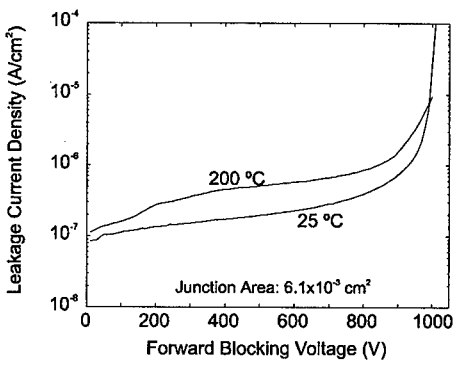

Fig. 5. GTO thyristor forward blocking characteristics (anode area: 4.58x10^{-4} cm^2).

thyristors, the current-voltage characteristic under forward blocking conditions do not show snap-back up to 200°C indicating that the breakdown voltage is limited either by the edge termination or defects.

To characterize device yield, the blocking voltage of the anode-gate junction has been measured for the 800 and 1200 μm devices. This blocking voltage must be sufficiently large to allow device turn-off under gate control. For a random sample of 50 devices of each size, the smaller devices show significantly higher yield compared to the 1200 μm devices. If devices with anode-gate blocking voltage above 10 V are considered as working devices, the yield for the 800 μm devices is 65 percent while the yield is only 19 percent for the 1200 μm devices. The lower yield of the larger devices is consistent with the larger number of defects present over the larger area.

The switching setup shown in Fig. 6 is used to investigate the switching performance of these devices. Figs. 7 and 8 show the resistive turn-on and turn-off characteristics of an 800 μm concentric GTO thyristor at 125°C having an anode finger width of 20 μm. These characteristics are taken at an anode current density of 200 A/cm^2. The turn-on characteristics show a delay time of 280 ns and a rise-time of 350 ns at a turn-on gain of 4. For this device, the current spreading phase is approximately 150 ns. The turn-off characteristics of Fig. 8 show a storage-phase of 85 ns and a fall-time of 200 ns at a turn-off gain of 2.4. The recombination tail for this device is estimated to be 350 ns. A maximum turn-off gain of 3.6 and maximum turn-on gain of 10 are measured at 200 A/cm^2 and 125°C.

GTO thyristor operation is dependent on the behavior of the constituent bipolar junction transistors. In particular, the common-base current gain of each transistor impacts GTO thyristor holding current, blocking voltage, and switching behavior. GTO performance is optimized when the gain of the upper pnp transistor is large and the gain of lower npn transistor is small. The measured npn and pnp transistor current gains are shown in Figs. 9 and 10 as functions of temperature and collector current. In both cases, the collector-emitter voltage was held constant at 25 V. A ~25 percent increase in the current gains was measured at a collector-emitter voltage of 100V. The wide-base npn transistor is shown to be strongly influenced by injection level where the dc current gain is very low below 0.1 A/cm^2 and rises rapidly at higher currents. The ac current

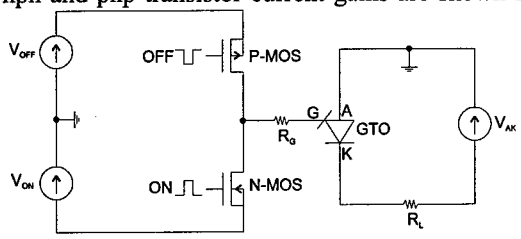

Fig. 6. Setup to measure GTO switching performance.

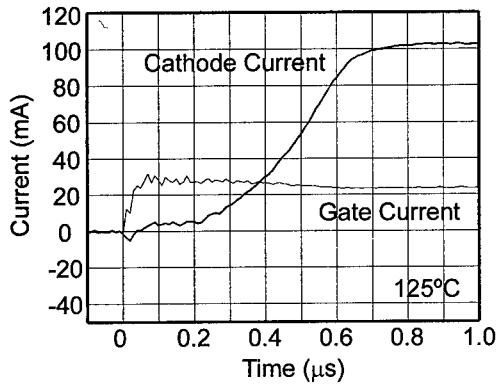

Fig. 7. Measured turn-on characteristic of concentric GTO of Fig. 2.

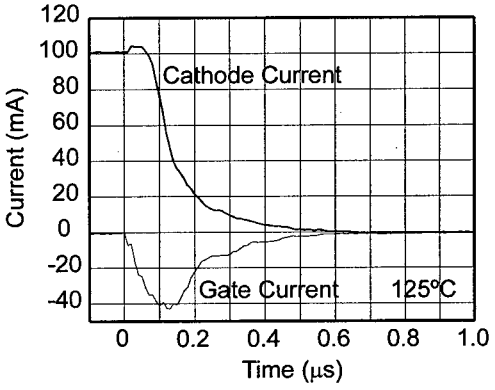

Fig. 8. Measured turn-off characteristic of concentric GTO of Fig. 2.

gain shows similar current dependence. Above 0.1 A/cm^2 the current gain increases noticeably with temperature reflecting the increase of carrier lifetime with temperature in the p-base. For the pnp transistor, there is smaller current dependence on current gain as shown in Fig. 10. Here, the current gain increases rapidly with temperature because of effects of thermal ionization and bandgap narrowing in the p+ anode. It should be noted that the current gains of each transistor are of comparable magnitude which leads to poor turn-off gain. Also, the sum of the ac current gains of the transistors must be larger than 1 to turn on the thyristor. The sum of the individually measured ac current gains do not exceed 1 up to 175°C however thyristor latching is observed at temperatures as low as 25°C. This discrepancy may result from current crowding below the emitter in the non-interdigitated transistor test structure, while no such current crowding takes place in the interdigitated GTO thyristor structure.

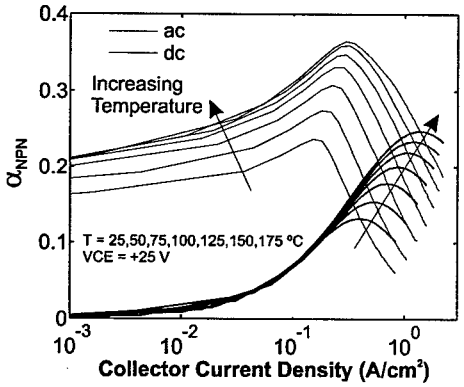

Fig. 9. Common-base current gain measured on NPN transistor test structure.

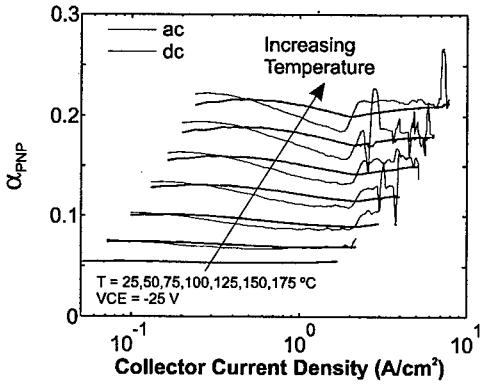

Fig. 10. Common-base current gain measured on PNP transistor test structure.

4. Conclusion

GTO thyristors fabricated on 4H-SiC have been electrically characterized at temperatures up to 200°C. The forward on-state voltage has been found to be higher than expected (4.8 V) compared to simulations (2.9 V). The large voltage drop is attributed to series resistance and low p+ anode emitter injection efficiency. The gate triggering current decreases from 150 mA at 25°C to 2 mA at 250°C. A forward blocking voltage of up to 1100 V has been measured and leakage currents are below 10^{-5} A/cm^2 at 200°C. Switching measurements showed a turn-on rise-time of 350 ns and a turn-off fall-time of 200 ns.

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Materials Science Forum Vols. 338-342 (2000) pp. 1395-1398

4H-SiC Gate Turn-Off Thyristor Designs for Very High Power Control

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Keywords: Gate Turn-Off Thyristor, Power Conditioning

Abstract Measurements indicate that in power conditioning circuits using SiC gate turn-off (GTO) thyristors, conduction losses can be reduced by injection of a portion of the load current through an electrode connected to the base regions so that it encounters only two back-to-back *p-n* junctions. Simulations of SiC GTO thyristors indicate that the maximum voltage blocked can be increased and the turn-off time reduced by an increase in the thickness of the *p*-type buffer layer (*p*+ base region). These simulations also show that it is permissible to have the drift region *n*-type whether the gates are on an *n*-base or a *p*-base. This option is desirable because high-quality thick *n*-type epilayers are easier to grow than *p*-type epilayers.

Introduction

Excellent SiC gate turn-off (GTO) thyristor characteristics have been demonstrated for structures that were designed based on concepts developed over the last four decades to optimize silicon GTO thyristors. These structures have exhibited less than 100-ns switching speeds [1], 1000-V blocking, switching of 5000 A/cm^2 [2], and switching of 10 A when paralleled [3]. For implementation in high-performance reduced-size power-conditioning circuits, devices should be developed that do not destructively fail until performing well beyond the limits of silicon. Concerns have been raised about the 3-V on-state anode-cathode voltage drop, which may limit the maximum current that can be controlled by an SiC GTO thyristor [4]. Unfortunately, increasing the size of devices to handle more current has led to lower breakdown voltages, while increasing the number of devices in parallel could lead to nonuniform switching and increase the cost of manufacturing. Furthermore, the commercial availability of high-quality thick *p*-type epi-layers for blocking in the multikilovolt range is an issue.

However, solutions to these issues are within reach. In this paper we discuss new device structures for handling higher powers, presenting both measurements and simulation results. We demonstrate the capability of SiC GTO thyristors to handle higher powers by a new way of operation. To expand on this new concept we present simulation results showing switching characteristics. We also discuss the benefits of increasing the thickness of the *p*-type buffer layer and demonstrate the benefit of using an *n*-type drift region.

Procedure

We first demonstrate that gate turn-off does occur when part of the load current is injected at the gate electrode on a SiC GTO thyristor fabricated in our lab [5]. In this case, we investigated a three terminal SiC GTO thyristor in which a portion of the load current entered at the anode in series with a 43-Ω resistor, and the rest entered at the gate contact in series with a 1638-Ω resistor. A 700-Ω load was present. A Keithley 220 current source provided the ±3-mA gate drive signal to switch the thyristor on and off. The on-state currents were measured in the center of a 3-ms time interval

between the turn-on and turn-off pulses. Our aim here is only to indicate that this mode of operation is possible. To optimize the performance at maximum power levels the device structure should be properly modified and much lower resistors should be used in series with the contacts.

To separate the behavior of the gate control current from the load current injected at the base, we also investigated four-terminal devices as shown in figure 1. The contact connected to an inner base in series with resistor R_A is referred to as the subbase contact. Simulations were done on the four possible permutations of gate and subbase contacted structures; we discuss results for all four cases but show characteristics only for the two cases in figure 1. Mixed mode drift-diffusion model simulations were done with Silvaco's Atlas/Blaze software. We used models with SiC material parameters to account for incomplete ionization of impurities, concentration dependent mobility, SRH and Auger recombination, and impact ionization. We provide details about these models elsewhere [6]. The device had region thicknesses of 1, 1, 8, 1 and 4 μm for the top-most to bottom regions, and corresponding dopant concentrations $N_A = 1 \times 10^{19}$, $N_D = 3 \times 10^{17}$, $N_A = 1 \times 10^{15}$, $N_A = 5 \times 10^{18}$ and $N_D = 5 \times 10^{18}$ cm^{-3}. The circuit consisted of $R_A = 400\ \Omega$, $R_B = 50\ \Omega$, and $R_L = 6000\ \Omega$. The structure is 30 μm wide and 1000 μm long so that the total current density being turned off from the on state is 65 A/cm^2. We focus on the structure in figure 1(a) to investigate the effect of changing R_A and R_B.

We investigated the influence of *p*-type buffer layer thickness on switching losses by simulations of transient turn-off with structures having the following dimensions: (*p*-type drift region: *p*-type buffer layer) (6:5), (6:3), (8:5), and (8 μm: 3 μm). All other region thicknesses and dopant concentrations were as given above. To compare the performance of a structure with a p-type drift region with that of a structure with an *n*-type drift region, turn-off simulations were done with the device structure described in the previous paragraph, but in one case we replaced the drift region's acceptors with an equal number of donors with the proper ionization energy. Finally, we calculated the maximum voltage blocked in a structure with an *n*-type drift region for a structure having anode and *n*-type base region thicknesses of 2 μm each, and dopant concentrations of $N_A = 5 \times 10^{19}$ and $N_D = 3 \times 10^{17}$ cm^{-3}. For these calculations, the concentration and thickness of the *n*-type drift region and *p*-type buffer layers were varied.

Results and discussion

Figure 2 presents results of measurements made on a 4H-SiC GTO thyristor, demonstrating (for various on-state voltages) that some of the current passing through the load can be injected into the thyristor at its gate contact (I_G), while the rest passes through from anode to cathode (I_A). These results indicate that for this unoptimized device, the ratio of the load current entering the gate to that entering the anode (after the GTO thyristor is switched on and before the turn-off gate pulse is applied) is 38 percent at an on-state anode-cathode voltage drop (V_{AK}) of 4.75 V, dropping to 22 percent at $V_{AK} = 5.45$ V. The gate-to-cathode voltage drop in some cases was measured to be less than 0.1 V. The current exiting at the cathode contact was measured to be the sum of the currents entering at the anode and gate contacts.

For the two cases in figure 1, the transient turn-off curves are presented in figure 3. In its on state, the voltage drop V_{SBK} (subbase to cathode) is 0.054 and 0.059 while V_{AK} is 2.95 and 2.96, for cases (a) and (b) respectively. Switching losses are perhaps more important, and thus frequency dependence needs to be compared. The ratio of the total load current that sees the larger V_{AK} compared to that which sees the smaller total voltage drop is 1.258 for case (a) and 1.254 for case (b). Gate turn-off performance was also demonstrated in cases in which the subbase contact was placed on the *p*-type buffer layer, and a portion of the load current flowed from the anode to this subbase contact through just two back-to-back *p-n* junctions. When the subbase and the gate are on

the same layer, such as in case 1(a), the gate current does not go to zero until the gate drive circuit's current is turned off (around 8 μs in fig. 3(a)). This is because after the load current has switched off (but before the gate drive has switched off), there will be current flow in the circuit formed by V_G, R_G, R_A, R_B, and the *n*-base region that the gate is connected to. However, when the gate drive is connected to one region and the subbase contact is on another region, as in case 1(b), the gate drive current will turn off as soon as the load current is switched off. In all cases where the gate drive (V_G and R_G) is connected directly to the *p*-type buffer layer, the turn-off gain is higher than when the gate drive is connected to the *n*-type gated base. In the structure in figure 1(a), decreasing R_A or increasing R_B improves the turn-off gain. Moving the gate or subbase contacts laterally away from the main *p-n-p-n* region slightly increases the switching time. The separation of the injected load current at the gate from the gate drive as indicated in figure 1, and/or improved gate drive isolation techniques should resonably protect the gate drive from the very high load currents.

Simulations indicated that a thicker *p*-type buffer layer does reduce the turn-off times. Storage/fall times in nanoseconds for a structure with (drift region : *p*-type buffer region) thickness in μm are 630/297 (8:3), 474/330 (8:5), 572/287 (6:3), and 441 ns/325 ns (6 μm:5 μm). In other investigations we found that using a thick *n*-type drift region would result in performance that is at the very least comparable to that obtained with a *p*-type drift region. Comparing switching characteristics, simulations indicate storage/fall times of 979/390 ns when the drift region is *p*-type and 1268/231 ns when it is *n*-type. Steady-state simulation results indicate that for the case analyzed here, the maximum voltage blocked in the off state is similar, whether the drift region is *p*-type or *n*-type. Increasing the *p*-buffer region thickness increases the maximum voltage blocked, as shown in Figure 4 for an *n*-type drift region structure.

Conclusions

We have discussed, with measurement and simulation results, methods of reducing losses and increasing the amount of current that can be controlled in power conditioning circuits. These methods involve injecting a portion of the load current into a contact connected to one of the inner base layers so that it encounters only two back-to-back *p-n* junctions. The rest of the load current would pass as usual directly from anode to cathode. The entire current flowing through the load is controllable by the gate turn-off mechanism. This approach suggests a way of increasing the current that can be controlled in the device without increasing the area of the device. This technique will benefit greatly devices with a high on-state resistance (such as structures with very thick drift regions), because it allows them to operate at a lower voltage and lower current point on their *I-V* curves. Simulation results also indicate that the maximum voltage blocked can be increased and the turn-off time reduced by an increase in the *p*-type buffer layer (*p*+ base region) thickness. It is permissible to have the drift region *n*-type whether the gates are on an *n*-base or a *p*-base in a SiC GTO thyristor.

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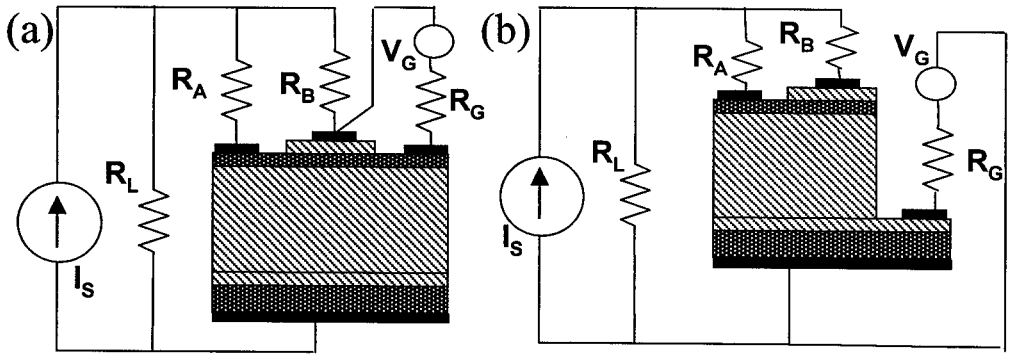
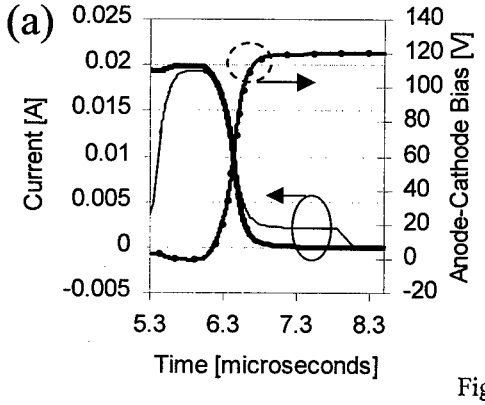


Figure 1. Circuit diagram showing resistors R_B, and R_A. Dark shaded regions are donor doped, and light shaded regions are acceptor doped. R_L is the load resistor and R_G is the gate drive resistor. From top to bottom of this structure the regions are 1) anode, 2) *n*-type base, 3) drift region, 4) *p*-type buffer layer, and 5) cathode region.



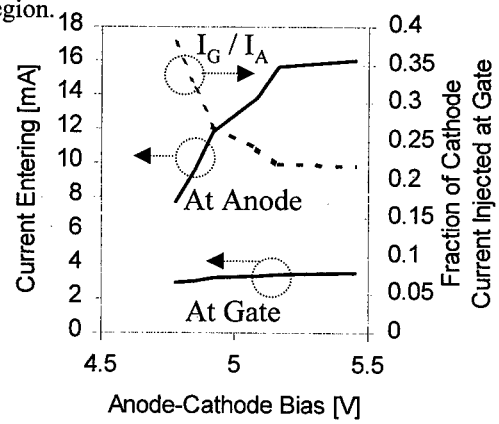


Figure 2. Measured load currents entering SiC GTO thyristor in its on state with gate trigger pulse off.

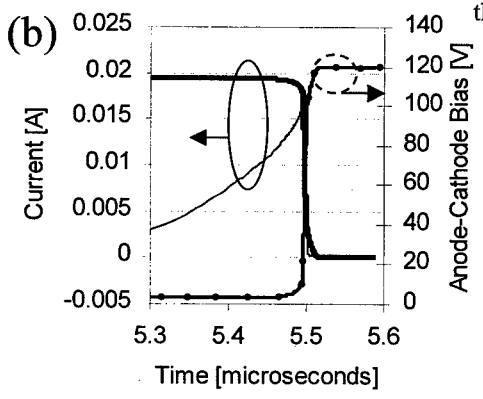


Figure 3. Simulation results for the structures with corresponding letters in figure 1. Shown are total current being switched (thick solid line), gate drive current (thin line) and. anode-cathode voltage drop (line with dots).

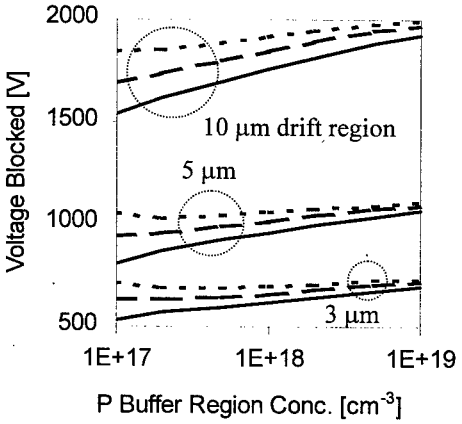


Figure 4. Simulated maximum voltage blocked for a structure with an *n*-gated base / *n*-drift region / *p*-buffer layer. *p*-buffer region thicknesses are, 1 (solid line), 2 (long dash), and 4 μm (short dash).

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Fabrication and Characterization of 4H-SiC GTOs and Diodes

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Keywords: Edge Termination, GTO, Guard Rings, PiN Diode

Abstract: 4H-SiC GTOs and P^+iN diodes have been fabricated and characterized. Mesa termination and floating guard ring termination have been used for the fabrication of GTOs with 7μm $7.2x10^{15}cm^{-3}$ doped p-blocking layer and 13μm $2.1x10^{15}cm^{-3}$ p-blocking layer, respectively. Characterization results will be reported. Switching measurements at high temperatures will also be reported which allows the determination of minority carrier lifetime and its temperature dependence in the p-base region of the GTO. For planar P^+iN diode fabrication, single zone implantation into a 30μm $1x10^{15}cm^{-3}$ doped n-type epilayer along with three-step JTE etching have been performed.

Introduction: SiC's potential for high power, high temperature and high speed applications have been clearly demonstrated over the past 10 years. Among many possible high power devices, the thyristor and gate turn-off (GTO) thyristor are attractive because they can handle very high power and do not require gate insulator which may present a long term reliability problem. GTOs with several hundred to a thousand volt forward blocking have been demonstrated, such as the asymmetrical 700V-2.5A ($688A/cm^2$) GTO[1]. 4H-SiC thyristors of 900V-2A and 700V-6A have also been reported [2]. Very high current density 4H-SiC GTOs capable of over 800-V fabricated with direct mesa termination by inductively-coupled plasma etch have shown robust performance [3]. In the area of diode development, P^+iN diodes have shown great potential for very high voltage applications. In this paper, we report on the fabrication and characterization of both 4H-SiC GTOs and P^+iN diodes.

GTO and P^+iN Diode Fabrication: The interdigitated anode and gate structures were employed for GTOs. Both multi-anode and single anode finger GTOs were designed and fabricated. Fig.1 shows the cross sectional view of a single anode 4H-SiC GTO developed under this project. The anode dimension was designed to be $4x10^{-5}$ cm^{-3}. The gate to anode spacing was 4 μm. The key to achieving high blocking voltage is in the edge termination. Instead of etching off the 1μm n-base layer and creating n^+ guard rings by implantation into the p^--base region, the n-base layer was implanted together with the gate contact region by nitrogen to form a 0.3 μm n^+ layer doped uniformly to $1x10^{19}cm^{-3}$. Nitrogen activation annealing was done at 1,550C for 30 min. By selective etching the implanted n-base region by 1.1 μm, 12 floating guard rings designed to be 4 μm wide and 2 μm apart were formed. Computer modeling showed that the floating guard rings along with the thin layer thermal passivation oxide and the thick 1 μm LPCVD oxide could reduce the field crowding and lead to a blocking voltage around 1,200V, if the amount of positive charge in the LPCVD oxide is assumed to be $3x10^{11}cm^{-2}$. Ni was used for n-type ohmic contact and Ti/Al bilayer was used for p-type ohmic contact. Both contacts were annealed at 1050°C for 5 min in Ar forming gas. GTOs with a 7μm p-blocking layer doped $7.2x10^{15}cm^{-3}$ and a 1 μm n-base layer doped $6x10^{17}cm^{-3}$ have also been fabricated in the same way but with deep mesa etching for edge

termination without using the floating guard rings. The starting material used in the fabrication of 1.4 mm diameter P^+iN diodes with the cross section view shown in Fig. 2(b) was a 4H-SiC wafer purchased from Cree Research, Inc. with a 30μm $1x10^{15}cm^{-3}$ doped n^- epilayer on n^+ substrate. Multiple energy and dose C+Al co-implantation was done to create the doping profile shown in Fig.2(a). The lower concentration implantation deeper into the epilayer was for the purpose of forming the main pn junction and multi-step JTE by dry etching. The heavy doping near the surface was for the formation of ohmic contacts. Implanted samples were annealed at 1,550°C for 30 min in a graphite crucible with SiC powder to prevent surface deterioration during annealing. After mesa etching of 3.7μm for isolating individual devices on the same wafer and following the JTE etching, 30 nm thermal passivation oxide and 1 μm LPCVD oxide were grown. Ni was sputtered on the substrate and annealed at 1050°C for 5 min in Ar forming gas to form ohmic contact. Anode contact windows of either 1mm or 0.3mm in the oxide were opened by wet etching and Al metal was then deposited by thermal evaporation and defined by standard lift-off process. Al contact was annealed at 950°C for 5min in Ar forming gas. The cross sectional view of the P^+iN diode is shown in Fig.2(b).

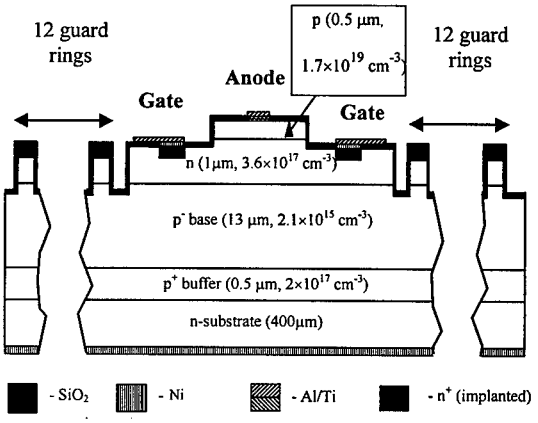

Fig.1: Cross sectional view of 4H-SiC GTOs with floating guard rings formed by n-base layer.

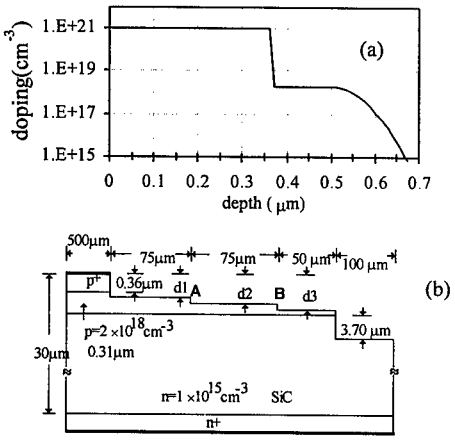

Fig.2: (a) Doping profile created by ion implantation assuming 100% activation efficiency; (b) cross sectional view of a planar implanted 4H-SiC P^+iN diode with three-step JTE.

Results and Discussion: Before performing device characterization, TLM patterns fabricated along with the device were utilized first to evaluate the specific contact resistances. Ni ohmic contacts on GTO gates were largely in the mid 10^{-6} ohm-cm^2 while Ti/Al contacts were scattered with the best in the mid 10^{-4} ohm-cm^2. DC blocking capability was then mapped and many devices were able to block over 1,000V. Fig.3(a) shows the forward current vs. blocking voltage for a 13 μm GTO that blocked the maximum voltage of 1,200V. The measurement was done by immersing the GTO in Fluorinet™. The DC I-V curve for a 13μm GTO that blocked 800V is shown in Fig.3(b). It is seen that by increasing the applied voltage, the gate current required to turn on the GTO is reduced from 1.4mA to 0.4mA. The self turn-on of this particular GTO is at 800V. The forward current density was limited to 1,250A/cm^2 by a load resistor. Turn-on and turn-off controls of the GTOs were also confirmed up to an anode current density as high as 4,000 A/cm^2. The 7 μm blocking layer GTO with direct mesa edge termination showed a maximum blocking voltage of slightly over 800V. Because the mesa terminated GTOs were much more robust in switching performance at high temperature, they were wire-bonded for high current density and high temperature switching

measurements. Fig.4(a) shows the turn-on voltage waveforms measured under different ambient temperatures. It is seen that turn-on time reduced as ambient temperature is increased, most likely due to the improved common base current gain of the top p^+n transistor when the top p^+ layer ionization efficiency is increased with increased temperature. Fig.4(b) shows the turn-off current waveforms at different ambient temperature. Note that the cathode current of over 300 mA for such a small area device could cause substantial heating of the anode p^+n junction. It is seen that the turn-off time increases with increasing temperature. By best fitting to the exponential decay of I_K in Fig. 4(b), electron carrier lifetime has been determined as a function of temperature as shown in Fig. 4(b). It is seen that the minority electron lifetime increases as a function of temperature from 52ns at 100C ambient temperature to 124 ns at 200C ambient temperature.

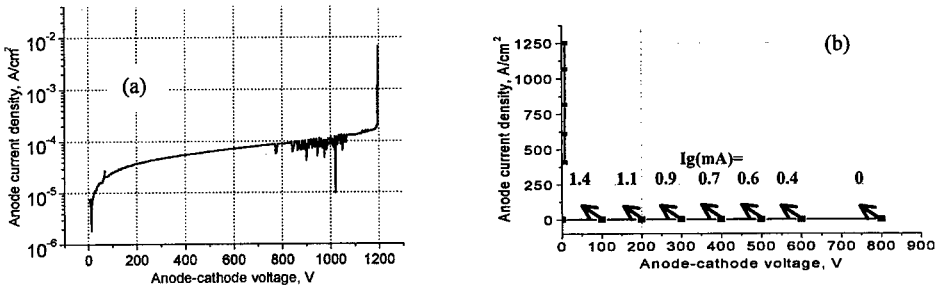

Fig.3(a) Forward I-V curve of a GTO showing up to 1,200V blocking; and (b) Gate turn-on control for an 800V GTO.

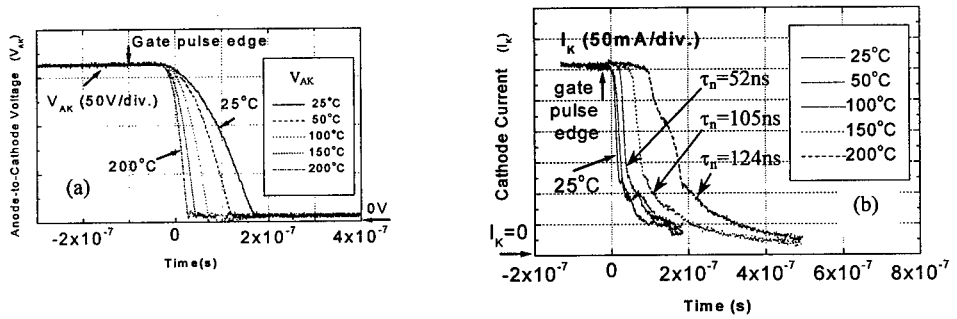

Fig.4 GTO turn-on (a) and turn-off (b) waveforms for the 7 μm blocking layer GTO.

Planar implanted P^+iN diodes have also been carefully measured. The best P^+iN diodes in terms of low leakage current and high blocking voltage (up to 5000V) have etching depth of d_1=0.25, d_2=0.27, and d_3=0.29μm (including SiC consumed by oxidation). Fig. 5 summarizes the measured results for a fabricated P^+iN diode chip. The measurement was done up to 3,000V and many diodes showed leakage currents as low as 10^{-7}~10^{-9}A at 3000V. Wafer level forward I-V measurement for a single cell has been done up to 5A at both RT and 200°C (Fig. 5(c)), which represents a current density near 637A/cm^2 at a forward volatge drop of 4.5V (at 200°C), and the reverse I-V (Fig. 5(b)) curve measured at RT showed a leakage current of $1x10^{-8}$A at 4000V and a leakage current of $1x10^{-6}$A at 5000V. A packaged 22-cell P^+iN diode has been measured up to a total current of 100A with a forward voltage drop of 9.4V as shown in Fig. 5(c). The packaged SiC diode has been successfully tested in a half-bridge inductively-loaded inverter circuit. A large percent of the 9.4V drop was due to the packaging because the anode specific contact resistance is in the range of $3.9x10^{-4}$ to $5.6x10^{-4}\Omega cm^2$ as determined by TLM pattern measurements. It should be pointed out that the demonstrated 5000V blocking voltage corresponds to a critical field as high as 1.97 MV/cm

for the $1x10^{15}$ doped drift layer of 29.3μm as shown in Fig. 2(b). The maximum blocking voltage of P^+iN diode of Fig. 2(b) with three-step JTE was simulated by using ISE Inc's DESSIS SiC module. Based on the cross sectional view shown in Fig.2(b) and the implantation profile shown in Fig.2(a) and assuming 100% activation efficiency, the maximum possible breakdown voltage is found to be 5,000V, in a good agreement with our experimental results, suggesting that three-step JTE is a very effective way for edge termination.

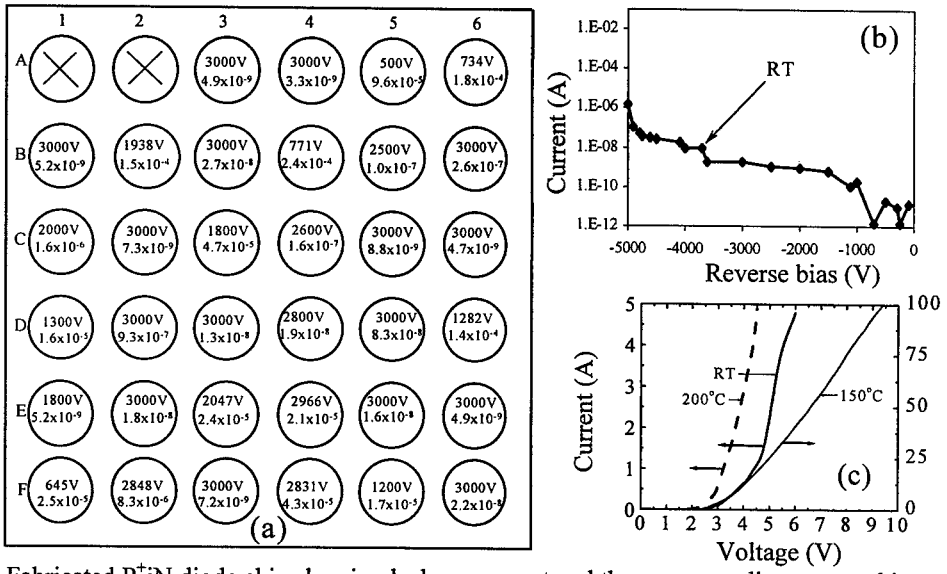

Fig.5 Fabricated P^+iN diode chip showing leakage current and the corresponding reverse bias voltage (a), reverse I-V curve at RT (b), and forward I-V curves (c) for a single cell at RT and 200°C and a 22-cell diode at 150°C.

Conclusion: Floating guard rings based on the n-base layer in a GTO structure has been utilized successfully for 4H-SiC GTO edge termination. Maximum blocking voltage up to 1,200V was realized for the GTO with a blocking layer thickness equal to 13μm. This approach is much more attractive than creating floating guard rings by implantation into p^- base layer. Mesa terminated 7μm blocking layer GTOs showed robust performance at both high current density and high temperatures. Switching measurements under different ambient temperatures show that the turn-on time shortens while turn-off time increases when ambient temperature is increased. Planar Al+C co-implanted 5000V 4H-SiC P^+iN diodes have been fabricated by using 29.3μm, $1x10^{15}cm^{-3}$ doped drift layer, reaching a critical field of 1.97MV/cm. A current density up to $637A/cm^2$ at 4.5V has been achieved for the P^+iN diode at 200°C. A packaged 22-cell P^+iN diode has been measured up to 100A.

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100 kHz Operation of SiC Junction Controlled Thyristor (JCT) Switches used in an All-SiC PWM Inverter

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Keywords: Controller, Converter, Diode, Drive, Gate Turn-Off Thyristor, GTO, Inverter, JCT, JFET, Junction Controlled Thyristor, Motor, Pulse Width Modulated, PWM

Abstract

This paper reports the first demonstration of a SiC switch operating at 100 kHz under hard driven, clamped inductive switching conditions. The switch, consisting of a SiC Junction Controlled Thyristors (JCT) and SiC free-wheeling diodes, was tested up to 150 V/0.8 A (=207 A/cm^2). The turn-off energy per cycle was 4.5 μJ, corresponding to a total switching loss of ~0.45 W (~116 W/cm^2) @ 100 kHz. Turn-on losses were <10 % of the turn-off losses. Snappy diode recovery of ~15 ns resulted in peak transient current enhancement of 3.5x. A first estimate is made for expected power loss of practical SiC switches with modest device ratings.

Introduction

Recent demonstrations of multi-amp and multi-kilovolt diodes [1,2,3] and power switches [1,4,5,6] have encouraged the insertion of SiC components in fundamental power device circuits, such as inverter switches, in order to study their performance characteristics. Such examinations are being conducted concurrently with investigations of scale-up and yield of individual devices. [1,7,8] The maximum operating frequency of a switch is an important device parameter in these investigations because of the desire to reduce the size, weight and cost of passive elements in power systems. Conduction and switching device losses ultimately determine this frequency for a given circuit topology and device package (thermal management approach). Several groups are presently examining the loss and efficiency improvements of inverters containing silicon switches and SiC fly-back Schottky and p-i-n diodes. [9,10] However, it is generally accepted that a significant increase in switching frequency will require the insertion of SiC switches.

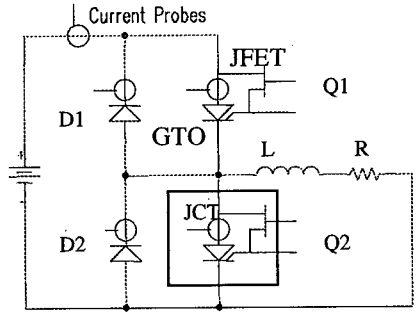

Figure 1: Schematic diagram of the circuit used to measure the characteristics of SiC diodes and JCT switches.

To date, limited experimental data is available on the switching characteristics of SiC devices, especially under the inductive loading conditions typically seen in inverter applications. [11] This paper, therefore, explores the performance of SiC switches as a first step in developing adequate models and estimates of the frequency capabilities of SiC devices for a given packaging approach. A JCT switch [12] is used for these studies since these devices have the all the elements of a high power

switch: (1) voltage-controlled turn-off to eliminate high current gate drive requirements of Gate Turn-Off thyristors (GTOs), (2) conductivity modulation to handle large currents and (3) high temperature capability. [1,13] Moreover, these devices have already been used to demonstrate an all-SiC 3-phase, Pulse Width Modulated Inverter (PWM-I). [1]

Experimental details

Tests were performed on a single phase of a 3-phase PWM-I, packaged and wire bonded on a custom designed Direct Bonded Copper (DBC) substrate containing on-package current probes mounted in the diode and GTO anode paths (see Figure 1). Each switch consisted of 4 parallel GTOs with blocking voltages up to 400 V and maximum turn-off capability of ~750 A/cm^2. The GTOs were capable of conducting 2 A @ 500 A/cm^2. Up to 36 small area JFETs were connected in parallel to yield > 1.8 A @ V_{DS} (=$V_{GA, GTO}$) = 2 V and V_{GS} = +2 V. The fly-back diode was composed of four 400 μm and two 600 μm diameter diodes blocking > 500 V and conducting 2 A @ 500 A/cm^2. All devices were made of 4H-SiC material. Characteristics of diodes & GTOs are given elsewhere.[1] Individual devices did not have snubbers and were, therefore, hard driven. However, the circuit did employ a DC bus capacitor.

Results

Conduction losses of the switch can be determined from the I-V characteristics shown in Figure 2. A maximum loss of 3.36 W (~870 W/cm^2) was measured at a current density of 207 A/cm^2. A large on-state dissipation is expected for SiC because of the 3.28 eV band gap energy. However, these values are higher than the ~2.7 V @ 500 A/cm^2 at 390 C that we have previously demonstrated using a more optimized structure. This corresponds to on-state dissipation in the range of 1350 ~W/cm^2 without accounting for heat spreading effects. Operation at 100-200 A/cm^2 should limit this dissipation to ~200-500 W/cm^2 with still lower values obtained by thinning the wafer to reduce substrate resistances.

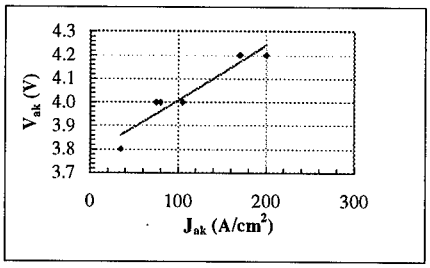

Figure 2: On-state I-V characteristics of a packaged SiC GTO switch as determined from pulsed measurements.

Switching losses are best characterized by E_{on} and E_{off}, the turn-on and turn-off energy loss per switching cycle, respectively. The power loss is then determined by the equation: $P_{sw} = f * (E_{on} +$

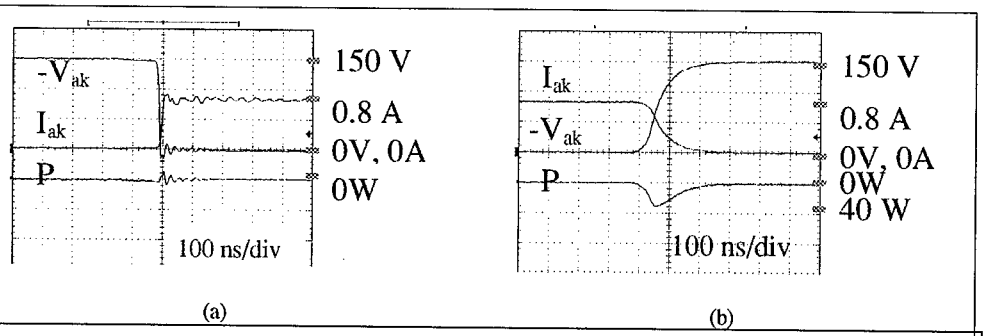

Figure 3: (a) Turn-on and (b) turn-off current, voltage and power waveforms for a JCT switch operating at 148 V/0.83 A (=207 A/cm^2) under resistive loading conditions. The voltage scale is inverted for display purposes.

E_{off}), where and f is the operating frequency. Figure 3 illustrates switching characteristics of the JCT under resistive loading conditions. Measured turn-on delay times decreased with increasing gain ($g=I_k/I_g$, where I_k and I_g are the GTO cathode and gate currents, respectively) from 400 ns (g=11) to 70 ns (g=2.2). Switching tests were performed with turn-on gains between 3 and 9. The GTO current had 13 ns rise and 130 ns fall time. Device dV/dt and dI/dt ratings were 1800 V/μs and 70 A/μs, respectively. It is obvious from the figure that turn-off losses far exceed turn-on losses (<10%) under typical operating current densities (>100 A/cm^2).

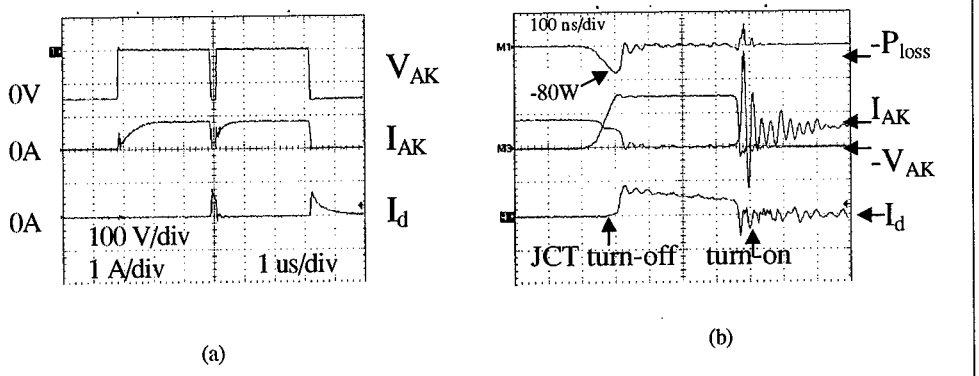

Figure 4: (a) Double pulse waveform and (b) expanded view of the 400 ns interval between the two pulses for a JCT switch operating at 148 V/0.84 A (=207 A/cm^2) under clamped, inductive loading conditions. The current and voltage scales in (a) and (b) are the same. The voltage trace in (b) has been inverted for display purposes.

Figure 4a illustrates typical switching waveforms under hard driven, clamped inductive switching conditions. Referring to Figure 1, JCT Q1 is seen to turn-on inductively with the first pulse, with diode D2 remaining off during the pulse. At the end of this pulse, D2 turns-on, clamping the voltage across Q1 and providing a conduction current of ~80 % of that in Q1 to the inductive load as Q1 turns off. The onset of the second pulse turns JCT Q1 on again, this time with an additional current spike due to reverse recovery of diode D2. Diode D2 is seen to turn-on at the end of the second pulse, with the current decaying as the energy in the diode/inductor load loop is dissipated by the series resistor. A magnification of the interval between the two pulses, shown in Figure 4b, reveals an oscillation during turn-on which combines with a snappy ~15 ns diode recovery spike to cause the current in Q1 to rise to ~3.5x its steady state value. The oscillation, most likely due to coupling between the DC bus capacitor and package inductance, should be eliminated in future packages by placing the capacitor closer to the switch. Nevertheless, the additional current is a further, unwanted, stress on Q1. Thus, diode snappiness, a result of either implant damage or surface recombination in the small devices used, will need to be

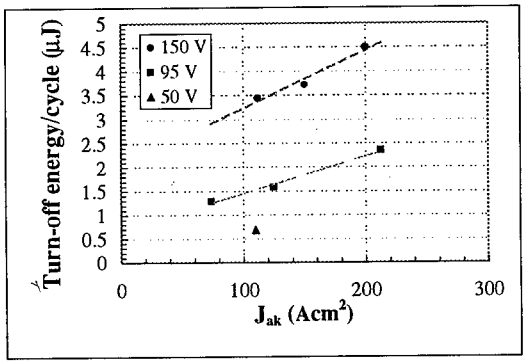

Figure 5: Plot of turn-off energy verses switch current for the JCT under inductive loading conditions.

monitored and addressed if still present in larger area devices. Turn-off losses again dominate losses.

Data similar to that shown above has been used to determine the switching losses in the JCT (see Figure 5). As one can see, the energy loss has a linear dependence on conduction current and super-linear dependence on voltage. Figure 6 illustrates the operation of a JCT switch at 100 kHz under 50% duty cycle under ambient cooling conditions. From Figure 5, one can determine a switching loss of 0.24 W (~60 W/cm^2) under test conditions, lower than expected conduction losses even from more ideal devices. Extrapolating these results to practical device structures (1-2 kV) operating at 100 kHz, one obtains a rough estimate for the total power losses of ~1.0-1.5 kW/cm^2, at the high end of present packaging capabilities, suggesting the need to focus on thermal management issues.

Conclusions

SiC switches are shown to be capable of 100 kHz operation under hard driven, clamped inductive conditions. Turn-off energy, determined for typical current densities over a range of voltages illustrates the increased importance of on-state dissipation for these devices relative to silicon-based switches, as expected. The results provide experimental confirmation of the expected increase in maximum operating frequency of SiC power switching devices. Extrapolation of the results suggests the need for improved thermal management to obtain similar performance in practical devices.

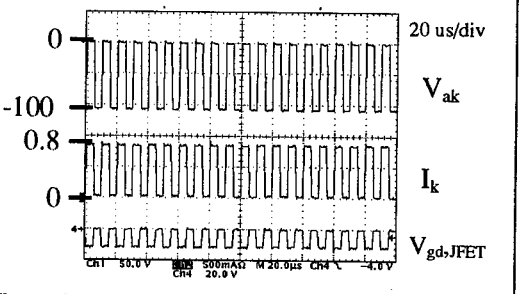

Figure 6: Voltage (100 V) and current (0.75 A @ ~200 A/cm^2) waveforms of a SiC JCT operating at 100 kHz.

Acknowledgements

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SiC-Power Rectifiers

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Keywords: Rectifiers, Schottky Diodes, SiC Power Devices, Switching

Abstract This contribution will focus on recent progress in Merged-PN/Schottky-Diodes (MPS) or 'Junction Barrier Schottky-Diodes' (JBS) [2] based on 4H-SiC first published on the ICSCIII-N'97 [1] conference. We will present measurements on large area 600V-SiC-Schottky-diodes which are able to handle more than 50 A. The switching behavior of these SiC-diodes is drastically improved in comparison to Si-diodes. The IGBT turn-on characteristic at 50 A will be demonstrated with a single SiC-Schottky-diode chip as the free wheeling diode.

Introduction Silicon Carbide (SiC) has the potential to replace Silicon based bipolar devices in the market of high power electronics. SiC-Schottky-diodes will pave the way to improved power electronics in traction and auxiliary converters. The power losses within those converter systems will be drastically decreased and the cooling effort will also be strongly reduced. These new converters will be for the benefit of electric cars like hybrid or fuel cell vehicles (600V-devices). For higher power requirements (e.g. busses) 1200V-devices will be used.

Experimental We use n-type 4H-SiC-substrates with about 10 μm thick epitaxial layers supplied by CREE Research Inc.. The Schottky-barrier of our MPS-diodes is formed by Titanium followed by a multi-layer metallization for packaging requirements. The achievable breakdown voltage was optimized by a suitable edge termination scheme including a p-type guard ring and an n-type channel stopper as well as a high field stable passivation layer. The n- and p-type regions are performed by ion implantations [3] (Al, N) followed by an activation step at 1700 °C.
For measurement purposes the devices are soldered in a TO-254 cases and contacted by wire bonding. The switching behavior of diodes and IBGTs are examined in a DC-Chopper circuit (low inductive setup) with an inductive load. The combination of Si-diode with Si-IGBT and SiC-diode with Si-IGBT is compared. The measurements are performed by using commercially available power blocks consisting of Si-pn-diodes and Si-IGBTs [4].

Results The outstanding behavior of high voltage, unipolar SiC-Schottky devices is demonstrated in Fig.1. The switching losses of a SiC-Schottky-diode in comparison to a fast Si-diode are drastically reduced. The area under the zero line (Q_{rr}) is a measure of the amount of switching losses of the diodes. The measurement was performed at 300 V and 20 A. Additionally, the observable reverse recovery current peak of the Si-diode can be neglected for a SiC-Schottky-diode. Hence also EMC problems are reduced. In traction converters for electric cars 400 A modules are needed meaning that the area of a single SiC-diode chip must be increased for current ratings in the tens of amps order. The quality progress of the SiC material and the epitaxial layers on the one hand and the improvement of the device design on the other hand made it possible to fabricate diodes with active areas of 16 mm^2 for current ratings in excess of 50 A. In Fig.2 first results for real power diodes performed in 4H-SiC are

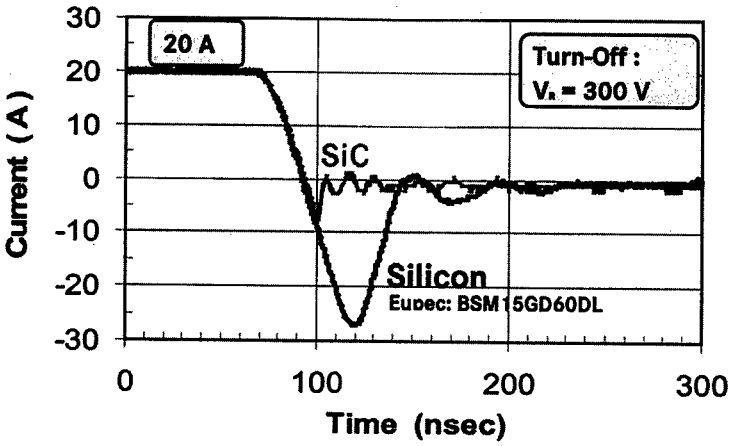

Fig. 1: Comparison of the switching behavior of a 600V- Si- and SiC-diode.

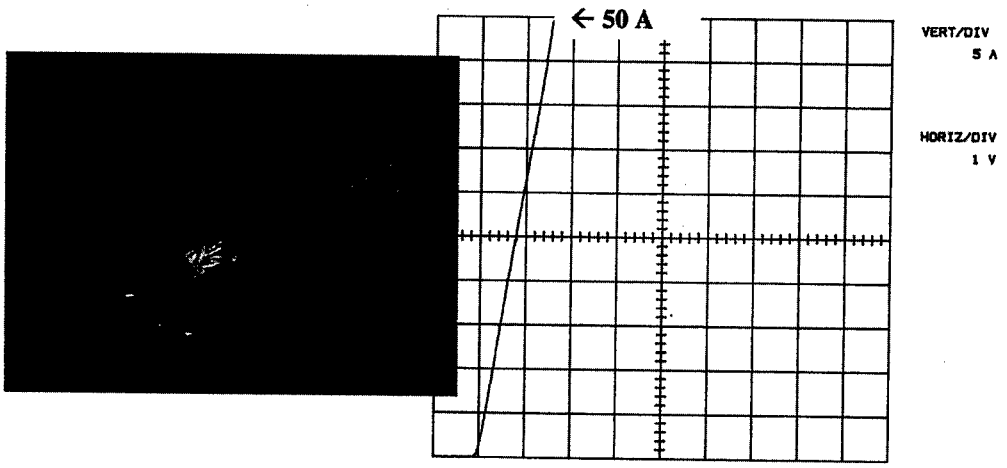

Fig. 2: Photograph of a single Schottky-diode chip packaged in a TO-254 case and forward current characteristic of the diode.

shown. The I-V forward characteristic of such a large area SiC-Schottky-diode is depicted exhibiting 50 A and a slope of r_d=34 mΩ. The main obstacle of the large area SiC-diodes are the various defects of the raw material (e.g. micro pipes, epitaxial defects, particles and dislocations). Depending on the kind and density of defects the devices are not always destroyed but exhibit an increased defect induced leakage current. In consequence, the yield of good large area devices is relatively poor. However, with the reduction of the defect density over the last years by Cree Research we can also see a corresponding improvement of device performance making larger areas up to 16 mm^2 (active area) possible.

Concerning the reverse leakage characteristic of SiC-Schottky diodes nearly defect free devices with smaller areas demonstrate what will be possible also for large area devices if defect density is further reduced.

In Fig. 3 the temperature dependence up to 225°C of the reverse current of 600V-type SiC-Schottky-diodes is depicted. Even for high temperatures an stable avalanche breakdown behavior can be deduced and the leakage current remains very small. Thus, the SiC-Schottky-diodes can also be used at elevated operating temperatures. While good and stable static

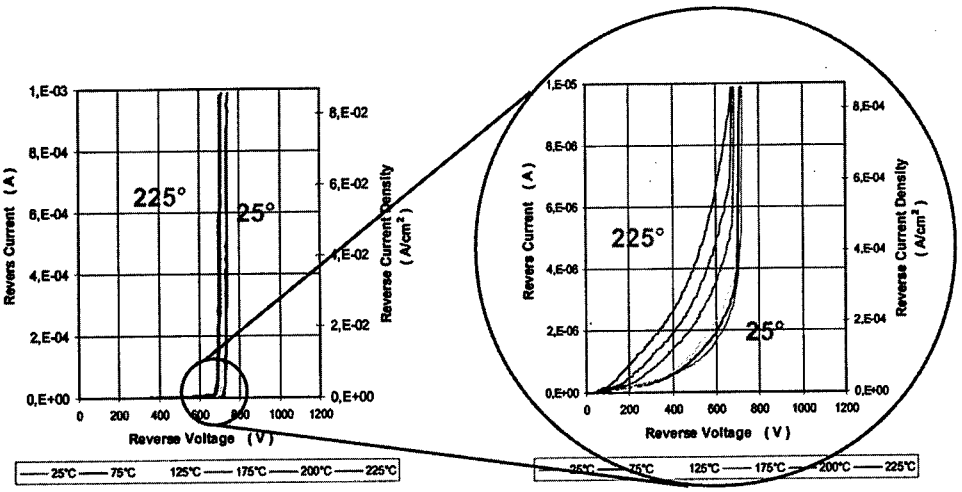

Fig. 3 Measured reverse I-V-curves for RT. and 225 °C.

device characteristics are indispensible, our main objective is the analysis of the switching characteristic of converter module sub-systems composed of a diode (SiC or Si, for comparison) and an Si-IGBT. In Fig.4 the switching behavior of the Si-IGBT (at turn off) and the Si-diode (left-hand side) in comparison with the substitution by a SiC-Schottky diode at 125 °C can be seen. In the case of the Si-diode, the reverse recovery current peak of the diode must also pass the IGBT which results in a current peak of the IGBT.

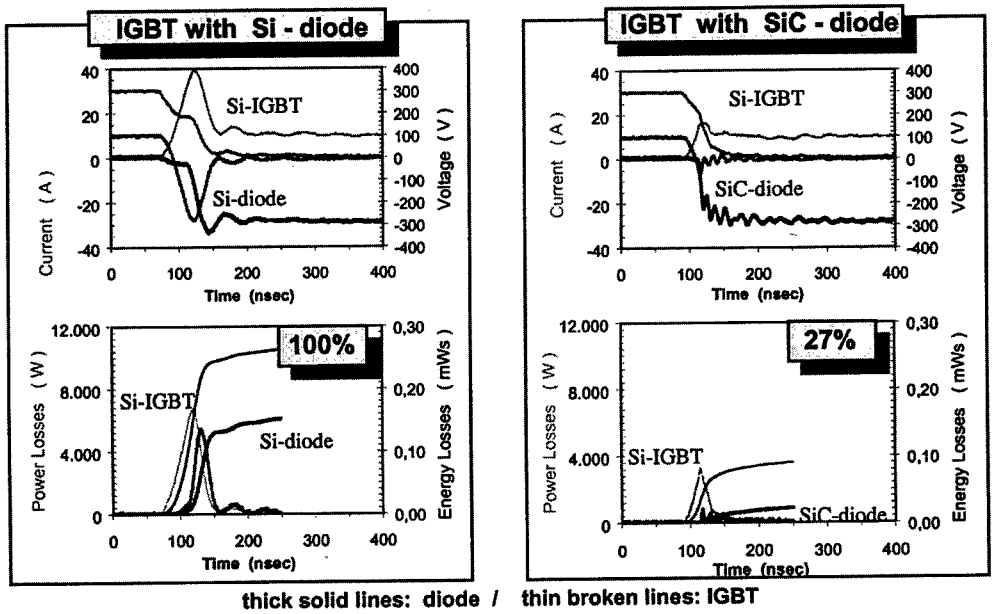

Fig.4: Switching behavior at 125 °C (10A, 300V).
Left: Si-diode + Si-IGBT. Right: SiC-diode + Si-IGBT

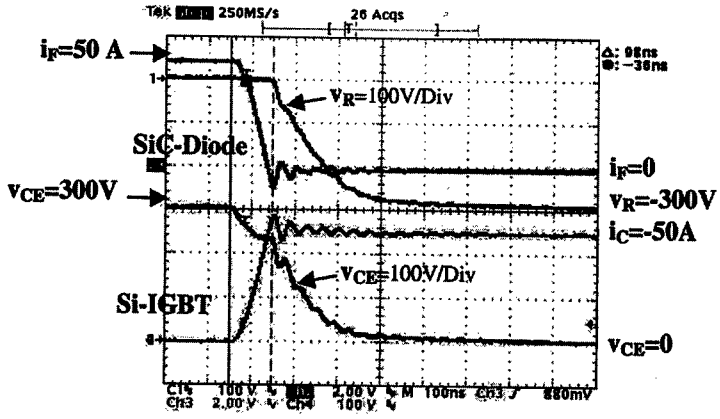

Fig. 5: Switching behavior of a 16mm^2 SiC-diode in a chopper circuit (1200V-devices) at 125°C. (Plot from Tektronix TDS 754C four channel digitizing oscilloscope).

In the case of the SiC-diode, no reverse current peak occurs and therefore also the switching losses in the IGBT are decreased. From these investigations the benefit in terms of power losses by substituting simply the bipolar Si-diode by an unipolar SiC-diode in conjunction with an Si-IGBT can be deduced. In the example shown above the resulting turn-on power loss saving amounts to about 70%.
The switching behavior of a single large area (16 mm^2) SiC-Schottky-diode at 50 A, 300 V and 125°C is demonstrated in Fig. 5. These are exact the switching specs in a traction converter of a fuel cell vehicle exhibiting a typical operating voltage range of 300 V and 200 A (consisting of 600 V, 50 A devices). For the auxiliary converters 20 – 30 A SiC-diodes are sufficient. The SiC-diode technology is on its way to jump in real converter demonstrations within zero emmision cars or hybrid cars for auxiliary converters as well as traction converters.

Summary We have demonstrated the feasibility of 600 V, 50 A SiC-Schottky-diodes for new converter modules which exhibit drastically reduced power losses and are suitable for high temperature applications. SiC has the potential to penetrate into converter modules used for electric cars. They are ready for real tests at different electric motors in auxiliary and traction converters exhibiting a reduced volume and weight as well as a higher efficiency. The electric vehicles will thus practice a higher performance.
Further improvements concerning efficiency and reduction of volume of the converters will occur when SiC-power-MOSFETs are available. This will lead to highly compact converter systems.

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Comparison of 5 kV 4H-SiC N-Channel and P-Channel IGBTs

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Keywords: Incomplete Ionization, SiC N-Channel IGBT, SiC P-Channel IGBT

Abstract

In this paper, the performance of 5 kV SiC P-channel and N-channel IGBTs is investigated and compared. Unlike their Si counterparts, the 4H-SiC N-channel TIGBT is not suitable for applications at 300 K-400 K and the P-channel IGBT is a better choice because of the relatively larger ionization gradients of acceptors than donors in SiC, although elevating the operating temperature improves the N-channel IGBT performance significantly.

1. Introduction

The vast majority of Si IGBTs have an N-channel because electron mobility is higher than that of holes for silicon. However, in this paper, it will be shown that some unique characteristics of SiC will make the P-channel IGBT comparable to its N-channel counterpart.

Performance investigations of SiC IGBTs have been carried out using numerical simulation [1-3]. A 200V fully planar, 6H-SiC TIGBT has also been demonstrated [4]. All the devices have an N-channel structure. Because of the relatively high ionization energy of dopants required in SiC and ionization gradients decrease with doping level, most impurity atoms are not ionized in highly doped regions. The ionization gradient of dopants in a P type SiC region is much lower than that in an N type SiC region since the ionization energy of acceptors is larger than donors. Hence, devices with a P^+ substrate exhibit larger specific on-state resistance than those with an N^+ substrate. For bipolar devices, incomplete ionization also induces lower injection efficiency, hence poorer on-state characteristics. As shown in Figure 2 of [4], the current handling ability of the TIGBT at 250°C is 10 times better than at 25°C because the ionization gradient of dopants increases with temperature. Therefore, the incomplete ionization effect has a more severe impact on the performance of N-channel IGBTs (with a P^+ substrate) than P-channel IGBTs (with a N^+ substrate). Also, the channel carrier mobility and the drift region carrier mobility in N-channel IGBTs are higher than in P-channel IGBTs, indicating smaller channel and drift region specific on-state resistances. Therefore, it is worthwhile investigating the feasibility of a P-channel IGBT in SiC.

2. SiC N-channel and P-channel IGBT comparison

In this paper, the performance of 5 kV 4H-SiC N-channel IGBTs and P-channel IGBTs with various base lifetimes and at different temperatures are investigated and compared by employing numerical simulations. P^+ polysilicon and N^+ polysilicon are employed as the gate materials respectively. Both devices have a substrate thickness of 300 μm, which is doped at 5×10^{19} cm^{-3}. The channel length is 2μm. The IGBTs have a trench gate structure. A buffer layer is used, therefore the devices have punch-through structures. Appropriate physical models and material parameters are chosen to obtain realistic results. The N-channel IGBT channel electron mobility is set as 100 cm^2/Vs at 300K, with V_{gs}=15V and V_{ds}=0.1V. The same material parameters of the inversion layer mobility

model to simulate the N-channel IGBTs are utilized for the P-channel IGBTs. All device breakdown voltages are measured at 800K.

For the same carrier lifetime and forward blocking voltage, the P-channel IGBT drift region width is larger and doping is lower than in N-channel IGBTs. The IGBT forward blocking voltage is determined by the open-base breakdown voltage of the integrated transistor, which is pertinent to the gain of the parasitic base/drift/substrate transistor. The current gain of the P-channel IGBT parasitic transistor is intrinsically higher than the N-channel IGBT parasitic transistor because the former is a NPN transistor whilst the latter is a PNP transistor. So the P-channel IGBT is prone to breakdown at a lower forward voltage than the N-channel IGBT for the same structure. To achieve the same blocking voltage capability, a longer drift region and a lower doping level is required for the P-channel IGBT. Along with the lower mobility of majority carriers (holes) in the P-channel IGBT, its performance is projected to be poorer than N-channel counterparts. However, as will now be shown, when considering incomplete ionization of dopants in SiC, P-channel IGBTs offer better current handling ability at room temperature.

Figure 1 shows the temperature dependence of on-state voltage $|V_{on}|$ at 100 A/cm^2 of 5 kV SiC P-channel IGBTs and N-channel IGBTs with different lifetimes. The gate voltage amplitude is 15 V. The on-state voltages of the SiC N-channel IGBTs at 300K are more than 9 V, even with a 1 μs lifetime. By investigating the carrier distribution inside the device, it is found that at room temperature only a small quantity of minority carriers are injected into the drift region. Increasing the lifetime to 10 μs, the on-state voltage is decreased to 5.8 V. The on-state voltages are in the range of 4 to 5 V at 600 K because of the increased ionization gradient, hence improved injection efficiency at high temperature. Generally, the current handling ability of a SiC N-channel IGBT is improved with increased temperature and carrier lifetime. Its drift region modulated resistance depends largely on the injection efficiency, i.e., N^+ substrate doping and P buffer doping. Its sensitivity to carrier lifetime is less. However, this sensitivity will increase with voltage rating.

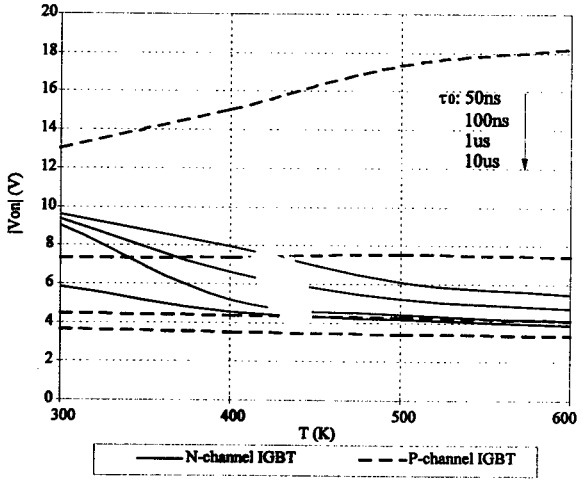

Figure 1. On-state voltages at 100A/cm^2 versus temperature

In contrast, it is more complicated for the P-channel IGBT. The ionization gradient of dopants in the P-channel IGBT substrate is larger than that in the N-channel IGBT substrate, thus, even at room temperature, a reasonable on-state voltage is observed. Increasing the lifetime to 10 μs does not substantially improve the device on-state performance. The on-state voltage of the P-channel IGBT changes rapidly with carrier lifetime, but only slightly with temperature, except with a 50 ns lifetime. The majority carriers of the P-channel IGBT drift region are holes, which exhibit lower mobility than electrons, resulting in larger intrinsic drift region resistance than for the N-channel IGBT. Thus, the carrier lifetime has a more significant impact on the performance of the P-channel IGBT than on the N-channel IGBT for the same voltage rating. With a lifetime of 50ns, few minority carriers are injected into the drift region at all temperatures, resulting in a relatively high on-state voltage. Several factors which influence the device performance change with temperature:

(1) The ionization gradient of dopants in the substrate - the higher ratio the activated dopants, the

higher the injection efficiency;
(2) The ionization gradient of dopants in the buffer - the higher ratio the activated dopants, the lower the injection efficiency;
(3) The mobilities of carriers - which degrade with temperature and
(4) The carrier lifetime - which increases with temperature.
With lifetimes from 10 μs to 100 ns, these effects counteract each other, hence the on-state voltages are steady. With a lifetime of 50 ns, the effects of the buffer and drift region mobilities are more significant than others, thus an increase in on-state voltage is observed.

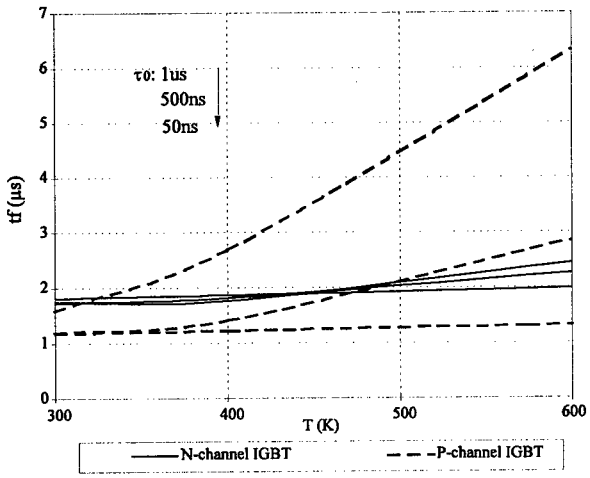

Figure 2. 1.2 kA 4H-SiC IGBT collector current fall time at switch-off versus temperature

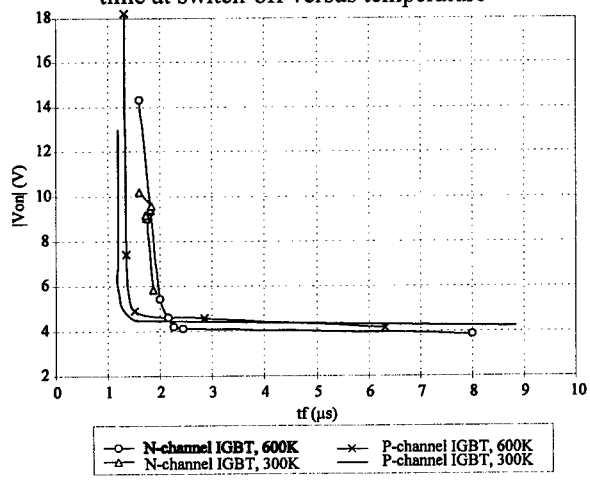

Figure 3. 4H-SiC IGBT trade-off curves

The IGBT temperature dependence of collector current fall time at switch-off with a resistivity load is plotted in Figure 2. The on-state current is 1.2 kA and the DC link voltage is 2.5 kV. The switching speed of N-channel IGBTs only changes slightly with temperature and carrier lifetime. The switching speed of the P-channel IGBT with a lifetime of 1 μs or 500 ns decreases quickly with temperature. With a lifetime of 50 ns, there are few excess carriers stored in the drift region at all temperatures, hence device switch-off speed is constant.

When switching off the devices, after the gate voltage drops below the threshold voltage, the channel current is cut off. The channel current is a significant part of the on-state current in the N-channel IGBT. In contrast, the channel current, comprising holes in P-channel IGBTs, is much less than the electron current at the N base/P^- drift region junction. In addition, for the same breakdown capability, the P-channel IGBT drift region width is larger than in the N-channel IGBT. Thus, generally N-channel IGBTs are faster than P-channel IGBTs.

A device with a higher carrier lifetime has better current handling ability, but slower switching speed. It is useful to plot trade-off curves between on-state voltage and switching speed in order to observe device structure requirements. The device trade-off curves between t_f and $|V_{on}|$ are shown in Figure 3.

The trade-off curve for N-channel IGBTs at 300 K is not smooth because a higher lifetime produces a lower blocking voltage and thicker drift region width, together with a low injection efficiency. Therefore, an N-channel IGBT with a higher lifetime does not necessarily exhibit a lower

on-state voltage. Even increasing the lifetime to 10 μs, N-channel IGBTs still have a steady switching speed. Obviously, P-channel IGBTs are a better choice at room temperature because they exhibit lower on-state voltages and a faster switching speed. At 600K, at the best trade-off point, P-channel IGBTs have a faster switching speed while N-channel IGBTs have a lower on-state voltage. Hence, generally, the P-channel IGBT is suitable for fast-switching devices and the N-channel IGBT is suitable for devices with low on-state voltages at elevated temperature. The specific application will determine the device type preference.

3. Conclusion

The performance of 5 kV 4H-SiC P-channel TIGBTs and N-channel TIGBTs have been investigated and compared using a 2-D numerical simulator. Due to the relatively larger ionization gradients of acceptors than donors in SiC, the 4H-SiC N-channel TIGBT is not suitable for applications at 300 K-400 K and the P-channel IGBT is a better choice. At elevated temperature, 4H-SiC N-channel IGBT performance is greatly improved. At high temperature, from the trade-off curves between switching speed and current handling ability, it is clear that P-channel IGBTs have a faster switching speed whilst N-channel IGBTs exhibt a lower on-state voltage at the respective best trade-off points.

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Design and Simulations of 5000V MOS-Gated Bipolar Transistor (MGT) on 4H-SiC

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Keywords: FBSOA, IGBT, MOS-Gated Bipolar Transistor, RBSOA

ABSTRACT A novel Bipolar Transistor structure – the MOS-Gated Bipolar Transistor (MGT) is designed and studied for the first time on 4H-SiC. Simulations are performed and the device characteristics are compared with the Insulated-Gate Bipolar Transistor (IGBT). An on-state voltage drop similar to that of the IGBT is observed, but the new device exhibits superior Forward Bias Safe Operating Area (FBSOA) and Reverse Bias Safe Operating Area (RBSOA) when compared to IGBT. The turn-off MOSFET makes the turn-off much faster and independent of carrier lifetime.

INTRODUCTION

SiC has been predicted to have better performance than Si for high-voltage power applications. Conventional Insulated-Gate Bipolar Transistors (IGBTs) have previously been fabricated and demonstrated in both 6H and 4H-SiC [1,2,3]. Although the IGBT has advantages over MOSFET for high voltage applications, SiC IGBTs suffer from the presence of parasitic thyristor and trade-off between the Safe Operating Area (SOA) and channel mobility because the *npn* transistor has a better SOA than the *pnp* [4].

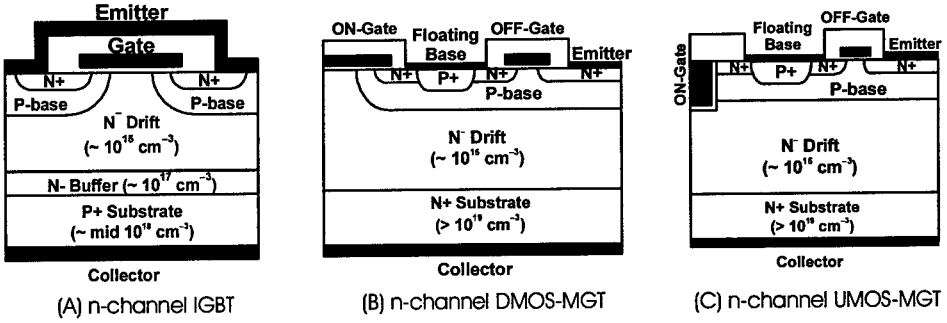


Fig. 1: Schematic cross-sections of n-channel IGBT, DMOS-MGT and UMOS-MGT

In order to integrate both the high mobility n-channel and the *npn* transistor in one structure, and to alleviate the problem of thyristor latch-up often faced by IGBT, a novel MOS-gated bipolar transistor structure, which has been previously demonstrated in silicon [5], is explored and studied by numerical simulations. This structure exhibits good on-state and reverse blocking characteristics as well as wider FBSOA and RBSOA. In addition, it is devoid of the latch-up phenomenon of the IGBT.

DEVICE STRUCTURES

Schematic cross-sections of both n-channel DMOS-MGT, UMOS-MGT and n-channel IGBT are shown in Fig. 1. The n-channel MGT is essentially an n-channel MOSFET driving an *npn* bipolar transistor. DMOS-MGT and UMOS-MGT differ in whether the turn-on gate is a DMOSFET or a UMOSFET. There is an optional n-channel turn-off MOSFET integrated in the structure. For SiC, the MGT has the optimum device structure due to the higher transconductance of n-channel MOSFET over p-channel and the higher current gain and BV_{CEO} of *npn* than the *pnp* counterpart [4]. The *npn* is more rugged than the *pnp* in SiC because the hole ionization coefficient is larger than the electron coefficient. Since the MGT does not have a four-layer parasitic thyristor, a better forward bias SOA is expected. Furthermore, the MGT uses n+ substrate, which can be doped heavier than the p+ substrate for the n-channel IGBT in SiC.

The fabrication process for the DMOS-MGT closely resembles the one used to fabricate a regular DMOSFET and IGBT which is a planar process. UMOS MGT is superior in its smaller cell size and easy processing with the use of epi grown P-Base but will suffer from low channel mobility and low breakdown voltage due to the higher electric field at the trench corner. DMOS MGT can solve these problems by adding a deep P-Base implantation.

SIMULATION RESULTS AND DISCUSSIONS

Numerical simulations have been used for the device performance projection. The material parameters and their variations with temperature used in these simulations have been carefully assessed and extracted from available experimental data. These include impact ionization coefficients, band gap energy, carrier mobility and dopant energy levels.

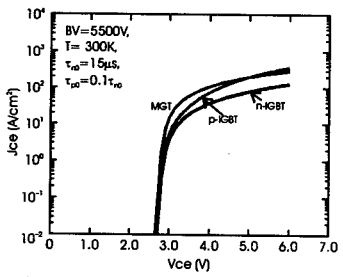
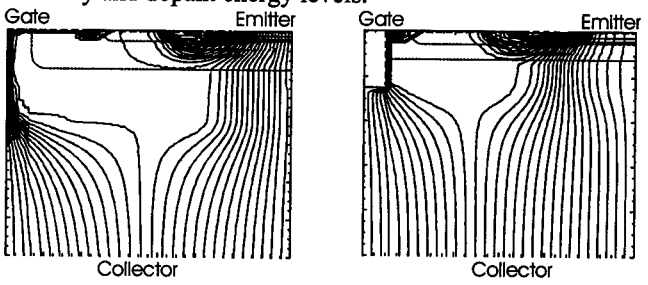


Fig. 2: Forward I-V Characteristics of 5000V UMOS n-IGBT, p-IGBT, and MGT in 4H-SiC



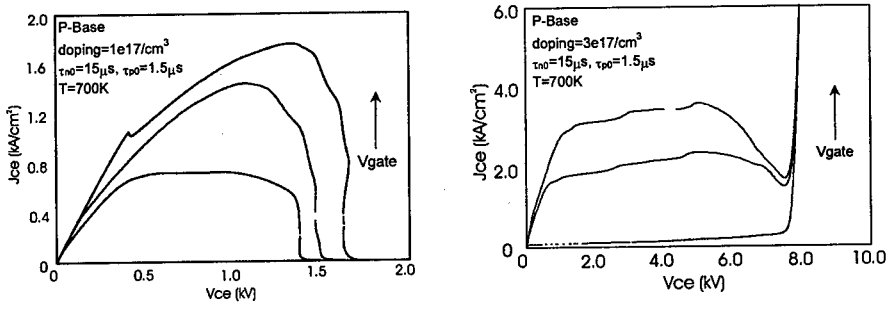
(A) DMOS-MGT (B) UMOS-MGT

Fig. 3: Current flow lines for 5000V MGT at J=100A/cm^2, Gate bias=15V

Calculated forward I-V characteristics of the 5000V SiC n-channel MGT are shown in Fig. 2 together with those of the 5000V n- and p-channel IGBTs. At room temperature, the forward drop of the MGT is similar to both that of the n- and p-IGBT. In addition, simulation shows similar forward voltage drop of the MGT when electron lifetime varies from 15μs to 0.15μs. The current flow lines of the 5000V DMOS and UMOS MGTs are compared in Fig. 3. The collector current of the MGT is composed of the current of the MOSFET and the current of the bipolar transistor.

An interesting current self-limiting effect is observed when low P-base doping is used. For a 2μm thick P-base with a doping of 1×10^{17} cm^{-3}, most of the P-base is depleted after a certain applied collector bias. In this case, the feeding path of the base current is cut off, leading to a decrease of the collector current (Fig. 4A). Although this special feature can serve as a protection in the on-state or over-current conditions, in the off-state, the base punchthrough will degrade the

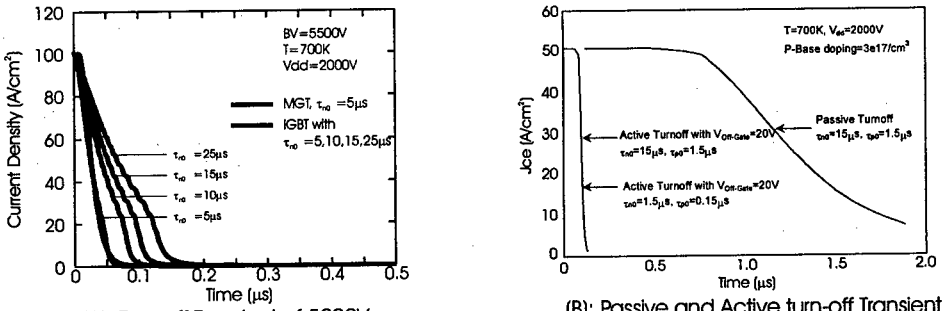
breakdown voltage. Therefore, it is important to choose a P-base doping concentration and thickness to make sure that the avalanche breakdown and the punchthrough of the base region happen at the same time. Fig. 4B also shows the forward bias SOA of MGT when using an optimal P-base doping of 3×10^{17} cm^{-3}. The forward bias SOA of MGT is superior to IGBT mainly because there is no parasitic thyristor and therefore no latch-up action is observed.



(A) Current self-limiting effect for 5000V SiC MGT with low p-base doping.

(B) Forward-bias SOA of 5000V SiC MGT

Fig. 4: Forward-bias SOA of 5000V SiC MGT with different P-Base doping



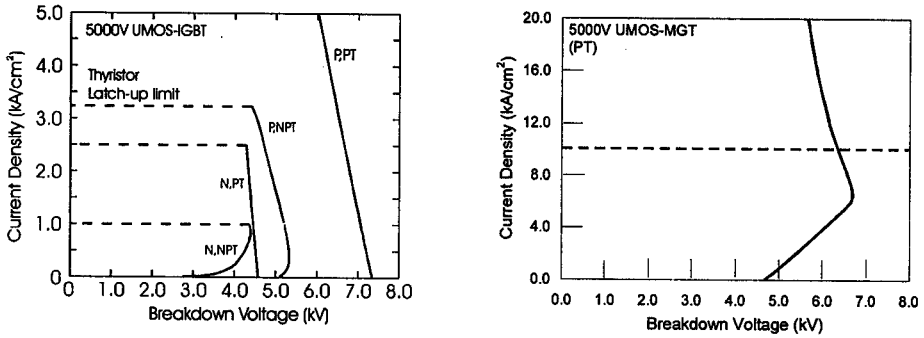
(A): Turn-off Transient of 5000V SiC IGBTs and MGT at 700K

(B): Passive and Active turn-off Transient of 5000V SiC MGT at 700K

Fig. 5: Turn-off Transients of 4H-SiC MGT and IGBT

Fig. 5 shows the turn-off transients for the n-channel MGT and IGBT. Unlike the IGBT, the MGT turn-off characteristics are not necessarily open base and can be controlled by an integrated turn-off MOSFET. During passive turn-off, the electron and hole plasma is extracted from the drift region. In the active mode, the minority carriers are extracted out of the device through the turn-off MOSFET channel. Hence the primary mechanism of the active turn-off is not recombination, and the turn-off is much faster and almost independent of carrier lifetime. Also shown in Fig. 5B are the simulated active turn-off with different lifetimes and the passive turn-off.

A significant improvement in the reverse-bias SOA is observed for the MGT. Comparing with the IGBT, the main bipolar transistor of the MGT has a narrow-base, lightly doped collector structure. Due to the Kirk Effect, when the collector current increases, the electrons that flow into the drift region will change the profile of the electric field in the collector, hence the maximum sustainable collector voltage increases. This effect results in the increase of the breakdown voltage with increasing current density in part of the MGT RBSOA shown in Fig. 6. It shows clearly the wider RBSOA of the MGT compared with that of the IGBT.



(A) RBSOA of n- and p-channel IGBT (B) RBSOA of MGT

Fig. 6: Reverse-bias SOA of 5000V SiC IGBT and MGT

Devices with the DMOS-MGT structure and 5000V blocking voltage have been designed and are under fabrication. The typical layout of the device is shown in Fig. 7. It is expected that the actual device performance will depend to a large extend on the channel mobility of the driving MOSFET as well as the gain of the bipolar transistor.

SUMMARY

A novel high-voltage MOS-Gated Bipolar transistor structure is examined in detail for 4H-SiC. Its characteristics have been compared with those of the IGBT structures. The fabrication of the MGT is compatible with that of the DMOSFET or UMOSFET. Based upon numerical simulations, it has been demonstrated that the device gives good performance in on-state, reverse blocking, RBSOA, FBSOA and turn-off transient.

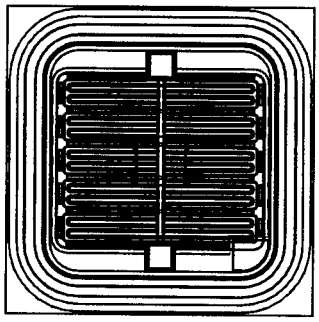


Fig. 7: Layout of 5000V SiC DMOS-MGT

ACKNOWLEDGEMENT

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TCAD Evaluation of Double Implanted 4H-SiC Power Bipolar Transistors

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Keywords: 4H-SiC, Bipolar Transistor, Simulation

Abstract

In this paper, a double implanted vertical npvn 4H-SiC power bipolar transistor (BJT) is studied using TCAD simulation. The choice of physical models employed in the simulations is shown to markedly affect critical device characteristics such as current gain. Incomplete ionisation of acceptors in the base region is shown to result in dramatically increased gain at room temperature but a reduced current drive capability, which is caused by emitter current crowding. The effects of band-gap narrowing and lifetime variations are also studied. The simulations demonstrate that a SiC power BJT should indeed be a viable device but that much work needs to be done to improve the accuracy of physical models, and for implanted SiC in particular, before reliable predictions can be made.

1. Introduction

SiC is an attractive candidate for manufacturing power switching devices operating at high temperature, high voltage and high current density because of its wide band-gap, high thermal conductivity and high breakdown electric field strength. Although much progress has been made in many areas of device technology, the development of a controlled, normally-off, switching device has been hampered by poor MOSFET performance. This is particularly the case with the 4H polytype, which is preferred for vertical switching devices on account of its higher on-axis mobility. Alternative majority carrier switching device technologies, such as the ACCUFET [1] and SIT, have been proposed but they demand non-trivial processing with very high tolerances to achieve acceptable performance. Bipolar switching devices, such as thyristors, and combinations of devices such as a GTO thyristor-JFET, on the other hand have been demonstrated effectively at high current levels [2]. The humble power bipolar junction transistor (BJT) has, however, received little attention, in spite of the fact it was the backbone of Si technology for many years. It is, therefore, the purpose of this paper to present a simulation based evaluation of the SiC power BJT.

2. Theory

The npvn bipolar transistor relies on a wide lightly doped collector to act as the main voltage blocking region with the base region acting as the other half of the voltage supporting structure. At breakdown, under idealised conditions, the electric field at the base-collector junction approaches the critical field, E_c, for SiC. To prevent punch through of the base region, the base doping level, N_A, and base width, W_b, must be chosen such that:

$$qN_AW_b > \varepsilon E_c \qquad \text{(Equ. 1)}$$

Thus in SiC, where the critical field is high, a relatively high level of base charge is required.

A simplified expression for the gain of a BJT may be obtained if it is assumed that the minority carrier diffusion lengths in the emitter and base are large compared to the physical length of these

regions. The base transport factor may thus be assumed close to unity and the expression for the common emitter current gain is well approximated by:

$$hfe \approx \frac{\gamma}{1-\gamma} \approx \frac{n_{b0} D_{bn} W_e}{p_{e0} D_{ep} W_b} \qquad \text{(Equ. 2)}$$

where γ is the emitter efficiency, n_{b0} is the equilibrium electron concentration in the base, p_{e0} is the equilibrium hole concentration in the emitter and W_e is the emitter depth.

The requirement for a relatively large base charge (roughly 10 times that expected in Si) does not auger well for SiC since increases in base width and/or increases in base doping will tend to suppress gain. Values for the diffusion coefficients D_{bn} and D_{ep} might also be expected to be lower than in Si reducing the expected gain still further. Given that typical Si power BJT gains are of the order of 10, it might be expected that a SiC power BJT would yield a very low gain and would, therefore, be of little practical interest. This, however, ignores the different ionisation energies associated with typical donor and acceptor species in SiC. For boron, the dominant acceptor level lies some 300meV above the valence band, resulting in just 0.4% of dopants being ionised under equilibrium conditions at room temperature (implanted acceptor concentration of $10^{18}cm^{-3}$, see Figure 1). For nitrogen, there are donor levels at 52meV and 92meV below the conduction band edge, giving around 16% electrical activation at room temperature under equilibrium conditions (donor concentration of $10^{19}cm^{-3}$ implanted in $10^{18}cm^{-3}$ B-doped p-well). The difference between the degree of ionisation in the base and emitter regions means that the ratio of equilibrium minority carrier concentrations (n_{b0}/p_{b0} in Equation 2) will be some 40 times higher than predicted by considering all dopants to be ionised.

In general, the degree of ionisation depends on the position of the quasi-fermi levels for electrons (holes) relative to the donor (acceptor) level. In equilibrium and under conditions of carrier injection (forward bias) the quasi-fermi level for the majority carrier will be pushed close to the dopant level leading to reduced ionisation as described above. In depletion (reverse bias) the quasi fermi level for the majority carrier is forced towards the centre of the band-gap resulting in complete ionisation of dopants.

3. Simulation

The active device was based on a 10μm epitaxial layer doped n-type $10^{16}cm^{-3}$, which forms the wide lightly doped collector region. The base region was boron-doped by ion implantation to a depth of 0.37μm at a nominal level of $10^{18}cm^{-3}$ whilst the emitter was nitrogen-doped by ion implantation to a depth of 0.2μm at a nominal level of $10^{19}cm^{-3}$. The emitter stripe width and emitter stripe spacing were both set at 10μm.

TCAD simulations were performed, using MEDICI [3], to obtain the current gain and I-V characteristics using a variety of physical models at a range of lattice temperatures. The principal physical models employed in the simulation were: an analytical model of the doping dependent carrier mobility for low electric field (ANM), doping dependent carrier lifetime (DDL), band-gap narrowing (BGN) and incomplete ionisation of dopants (INC). For the ANM model, the parameters were taken from experimentally verified results in [4]. In the case of the DDL model, electron lifetimes were taken from [5,6] while the hole lifetime was assumed to be one fifth of the electron lifetime. Note that little or no data has been published on the lifetime of carriers in implanted regions so a wide range of lifetime values was employed. The parameters for the BGN model were taken from the classical model [7]:

$$\Delta E_g = \frac{3q^2}{16\pi\varepsilon_s}\left(\frac{q^2 N_E}{\varepsilon_s kT}\right)^{1/2} \qquad \text{(Equ. 3)}$$

For the INC model, parameters are GCB=2/GVB=4 for the degeneracy factor, and EAB=0.3eV/EDB=0.07eV for ionisation energy, for boron /nitrogen dopants respectively.

4. Discussion and Results

Figure 2 shows the effect of various physical models on the simulated common emitter current gain of the transistor at constant Vce. Mid-range gains of 40, 3000, 3.1 and 250 were determined for the ANM/DDL, ANM/DDL/INC, ANM/DDL/BGN and ANM/DDL/BGN/INC model combinations respectively. The gain in the case of the ANM/DDL model may be compared with the simplified analytical expression of Equation 2, which yields a value of 50. Introduction of the BGN model results in a significant reduction in gain, primarily due to an increase in the equilibrium minority hole concentration, p_{e0} in the heavily doped emitter, which is more increase than n_{b0} in the base (see Equation 2).

Incomplete ionisation (INC model) is most significant in the base region because of deep boron acceptor level of 300meV, and results in a significant reduction in the base hole concentration (Figure 3). In effect, the forward biased base-emitter junction behaves as if the base doping level were relatively low (~$10^{16}cm^{-3}$ at 300K), whilst the behaviour of the reverse biased base-collector junction is unaffected by the INC model and reflects the implanted acceptor level of $10^{18}cm^{-3}$. The quantity of active base charge may thus be much less than the base depletion charge, which is determined by the critical electric flux for SiC (Equation 1). This low level of active base charge increases the base sheet resistance, leading to emitter crowding and a fall in gain at high current densities (Figure 2). A further consequence of incomplete ionisation is the appearance of a negative temperature coefficient in the gain characteristic (Figure 4) at moderate current densities (up to $500A/cm^2$). This could be used to good effect in parallel connections where current sharing is often a problem. Finally, studies of the effect of carrier lifetime on current gain (Figure 5) show that the proposed BJT is tolerant of the reduced lifetimes expected in annealed, implanted regions. Figure 6 shows the simulated transfer characteristics of the bipolar transistor at 300K.

5. Conclusions

An evaluation of a 4H-SiC, double implanted power bipolar transistor has been presented. TCAD based simulations have shown the importance of the choice of physical models on critical device characteristics such as common emitter current gain. Band-gap narrowing effects in the emitter region are shown to decrease gain by a factor of nearly 10 at 300K. Conversely, incomplete ionisation of dopants is shown to yield almost a 100 fold increase in gain at 300K. However, this gain falls rapidly at higher current densities due to emitter current crowding. At higher temperatures, the increased degree of ionisation results in reduced gain at moderate current densities and increased gain at high current densities. Together, these studies indicate that design strategies for the SiC BJT will be significantly different to those used for equivalent Si devices. In particular, the dual nature of regions doped with deep-level impurities raises some interesting possibilities and is worthy of further investigation. It is also clear that much work needs to be done to determine accurate models for physical effects such as band-gap narrowing and for lifetime and mobility in implanted regions before TCAD simulations of SiC bipolar devices can be used to make accurate predictive assessments.

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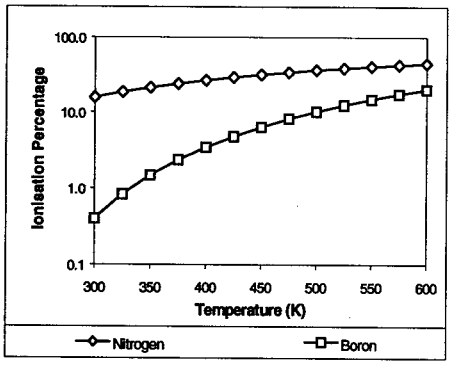

Fig.1: Ionisation percentage of dopants vs. Temperature

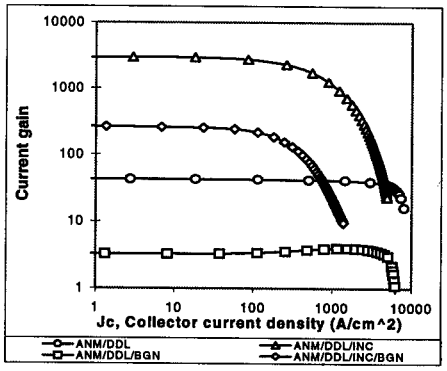

Fig.2: Gain vs. Jc with varying Model at 300K, Vce=5V

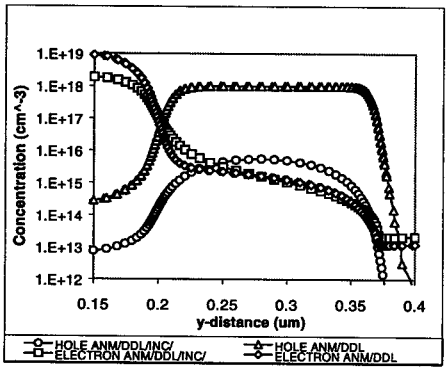

Fig.3: Hole and Electron distribution in Base at 300K, Vce=5V, Jc=100A/cm^2

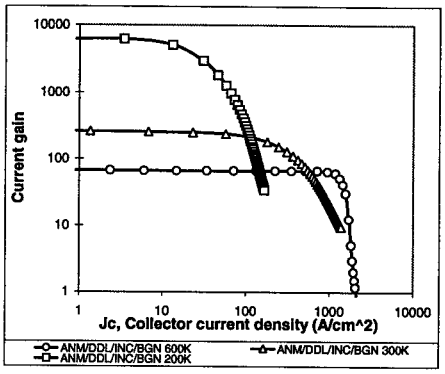

Fig.4: Gain vs. Jc with varying Temperature at Vce=5V

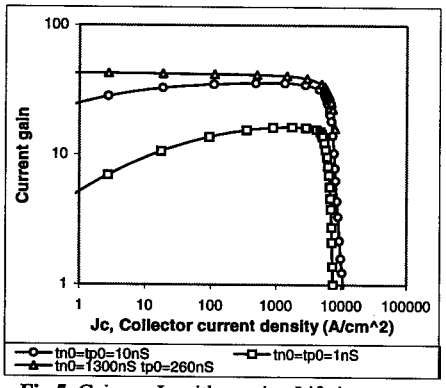

Fig.5: Gain vs. Jc with varying Lifetime at 300K, ANM/DDL

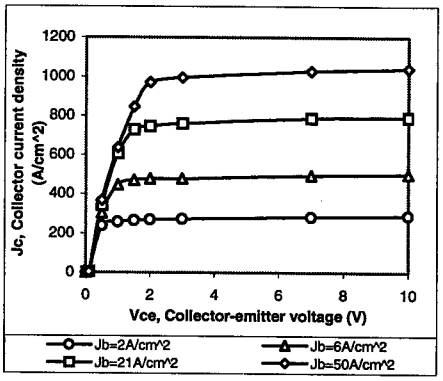

Fig.6: Jc vs. Vce with varying Jb at 300K, ANM/DDL/INC/BGN

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Operation of a 2500V 150A Si-IGBT / SiC Diode Module

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Keywords: High Current Switching, High Voltage Switching, Large Area Devices, PiN Diode, Power Modules

Abstract. Large area 4H SiC PIN diodes (20mm^2 and 40mm^2) for high power applications were manufactured and assembled in a classical high power press pack module. This module consists of four 2500V Si-IGBT chips and four antiparallel connected 2500V SiC diodes. Such modules are operated in application circuits with nominal conditions of 800V$_{dc}$ and 150A peak current. Diode switching losses are reduced to 4% of the Silicon reference. Compared to small diodes, large device chips show a high spread in leakage current density and often a reduced static blocking voltage. However, excellent transient switching characteristics can be maintained.

Introduction

High power applications, such as motor drive systems and HVDC transmission systems use voltage source converters. Such converters using inductively loaded switching are often limited thermally, where in addition in the second application also the cost of energy cannot be ignored. Loss reduction is therefore a prime objective. SiC devices have the potential to impact this converter technology fundamentally. However, such systems are often in the MW or even >100MW range and require devices with a large active area. This paper focuses on large area SiC PIN diodes and their properties under application condition. Even with large SiC diodes, parallel connection of several chips is necessary to reach the >100A current level. At this point, the active device area with a sufficient yield is still limited by material related deficiencies.

Fabrication

On 35mm 4H SiC wafers from CREE, a hot-wall CVD EPI layer of 30 – 40um thickness with a n-type doping in the low 10^{15}cm^{-3} range is grown [1]. Depending on the assumed critical field strength for this low doping, a theoretical blocking voltage of about 3000 - 3500V is expected. These wafers are then characterized with an optical microscope to identify a variety of defects. Visible defects such as 'micro-pipes', 'carrots', 'triangles', etc. have been reported to negatively affect the device performance to varying degrees [2, 3]. Individual for each wafer, large area diode chips of 20mm^2 and 40mm^2 are then placed in these defect free areas as shown in Fig. 1. The remaining

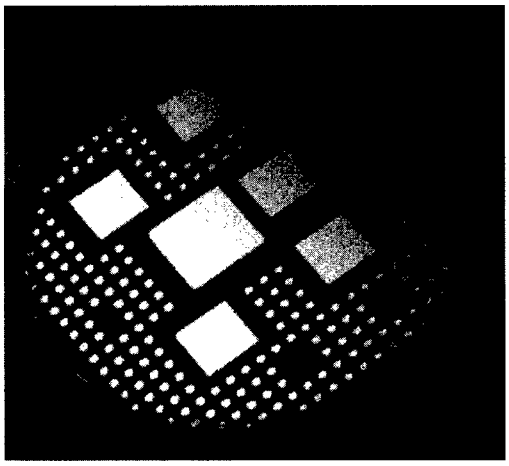

Figure 1 Typical wafer with 20 and 40mm^2 area diodes for power modules. The small diodes serve as reference devices.

area is used for small (0.5mm^2) monitoring devices. For patterning, a Direct Laser Write system is used. The implanted anode uses a multi energy Al-B profile, annealed at 1700°C, to combine optimal injection properties with good low leakage blocking. The devices are terminated using an implanted multi-zone junction termination extension with an oxide surface passivation layer. The details of the design and the process were described previously [4].

Characterization

Figure 2 shows the conduction characteristic of a 20mm^2-diode chip. At 100A/cm^2 the forward voltage V_f is 3.4V. This is in good agreement with the value of the surrounding small diodes provided the thermal measurement conditions are kept identical. This V_f shows a negative temperature coefficient of α_T~-1.1mV/K (at 100A/cm^2). This α_T has an appreciable variation over the wafer (up to -5mV/K have been observed) and varies also with current density. These effects are commonly attributed to a varying density or nature of recombination centers in the n-base layer.

For low forward currents a slight increase of V_f is observed for larger diodes. As this is not a transient effect due to the pulsed measurement, a non-uniform current distribution is likely present at the on-set of injection. The optical picture in Fig. 3 of a special diode test structure confirms this. Distinct areas, likely related to changing substrate properties, do indeed exhibit a retarded on-set of injection. These effects become less noticeable as the current density is increased.

In the subthreshold regime, large devices have often a wider ideality~1 range than small diodes, presumably due to diminished perimeter effects. However, excess recombination current at very low voltages (marked "A" in Fig. 2) may also be present. Such diodes show higher leakage current in reverse and inferior blocking.

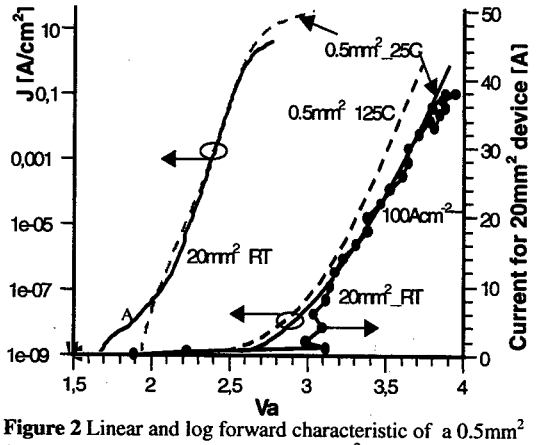

Figure 2 Linear and log forward characteristic of a 0.5mm^2 (current density scale right) and a 20mm^2 diode (•) at 25°C. The 0.5mm^2 diode is also shown at 125°C.

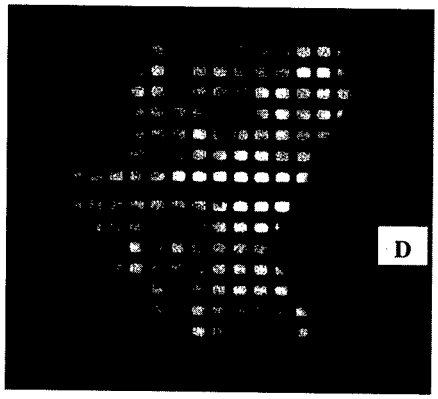

Figure 3 Optical emission of test-structure diode (0.8mmx 0.8mm) with windows in anode metallization. At 5A/cm^2 a clearly defined region has a lower current

Simulations indicate that non-uniform distribution of a variety of reported impurity or defect related traps in the bandgap [5] could explain the above phenomena (variation V_f, α_T, retarded injection) by affecting the recombination in the n-base. Except for the affected low forward current recombination, these trap centers must be located throughout the n-base. Potentially, crystal imperfections or remaining impurities in the EPI and substrate cause these electrically active defects.

Figure 4 shows the reverse characteristic of two small and two 20mm^2 diodes. These samples show good blocking (avalanche ~ 3kV), however, the leakage current density varies widely. While most small diodes have low leakage up to avalanche (small-1), others show increases in

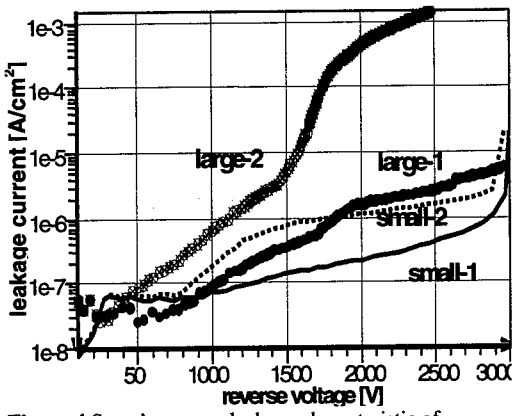

Figure 4 Sample reverse leakage characteristic of 0.5mm^2 and 20mm^2 diodes at 25°C.

leakage currents similar to reported dislocation related conduction (small-2) [6]. On the other hand, at currently reported dislocation densities, the (large-1) device probably contains several 100 to 1000 dislocations in the active area, while showing only slightly higher leakage current density than good small devices. Conversely, device (large-2), shows almost unacceptable high leakage while still reaching 2500V blocking. As no visible EPI defects are present in the compared devices, other material imperfections must be responsible for these variations. However, these remaining defects cause varying electrical consequences, as otherwise the shown devices would be unlikely according to [6]. The detailed properties of the defects causing this leakage remain unknown and their elimination unsolved.

Static and dynamic module operation

For dynamic operation with inductive load switching and proper thermal converter conditions, power modules are assembled. Classical Si press packaging technology is used for this. Four 2.5kV IGBTs (4x1cm^2) are assembled together with four 40mm^2 SiC diodes chips. The diodes for one module are parameter matched with respect to forward voltage and its temperature coefficient. A good thermal coupling between the chips was ensured by soldering the chips in close proximity (Fig. 5). The current sharing between the diode chips is tested by mounting thermocouples on all SiC chips. An inhomogeneous current distribution due to the decreasing forward voltage with increasing temperature would lead to uneven heating of the chips. In Figure 6 the temperature is plotted versus time, as the current in the module is gradually increased from 25, 50 to 75A/cm^2. This Figure demonstrates that the diodes maintain an equal temperature distribution indicating stable current sharing over the entire load range.

Dynamic testing of these SiC diode modules was carried out. A circuit corresponding to one phase leg of a converter is used. The measurement in Fig. 7 shows the SiC diode turn-off at a

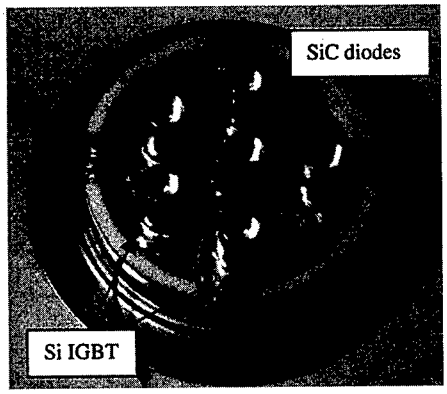

Figure 5 Standard presspack module combining Si-IGBT and SiC pin diodes.

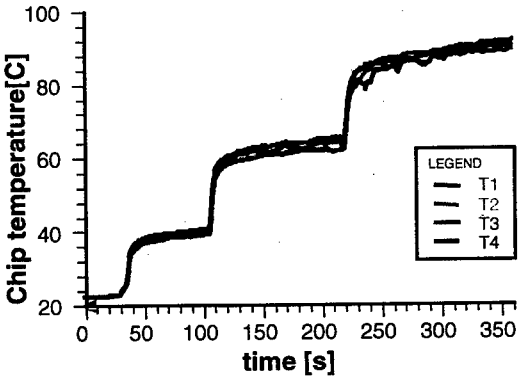

Figure 6 Chip temperature of the four parallel connected SiC PIN diodes indicating uniform current sharing as 40, 80, and 120A is passed through the module.

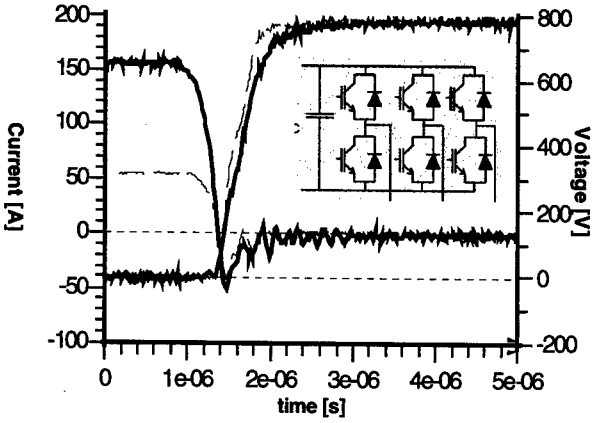

Figure 7 Transient operation of Si-SiC module. V-t and I-t curves for a diode turn-off at 800V, 150A (solid lines), and 55A (thin lines) at Tj=125°C. Inset: converter configuration for switching.

current of 150A. The DC link voltage is set to 800V. The temperature of the chips was 125°C. The reverse recovery charge for 150A is 13.5µC and for 55A 8µC, respectively. This is about factor three (rsp. 2) higher than the expected depletion layer charge, indicating that carrier plasma is removed during the recovery and that higher currents indeed increases the base modulation as expected. At room temperature (trace not shown), the recovery charge is on the order of the depletion charge, indicating that all plasma charge recombines during the relatively slow turn-off (~400ns from full forward current). This strong increase in the plasma level at higher operating temperatures can explain the decreased series resistance of the diode at higher temperatures. Via device simulations, the effect is attributed mainly to a n-base carrier lifetime increase and only a slightly higher injection due to improved dopant ionization in the p-anode. Note, that these transient traces reflect operating conditions, but are significantly lower than the maximum current voltage conditions for destructive failure.

The benefits of SiC in power applications are mainly the semiconductor loss reductions for high voltage components and a higher operating temperature. A module with silicon diodes for identical rating and switching conditions (at 75°C) leads to 70mJ for this event, while the presented SiC module causes merely a loss of 3.7mJ. Hence, the recovery charge and the switching losses of the module with the SiC diodes are less than 4% compared to Si. This confirms experimentally the high loss savings due to the use of SiC components.

Summary

High power modules with SiC diodes have been shown feasible to ratings relevant for power electronic application. Paralleling of diode chips is demonstrated to achieve >100A ratings. Diode switching losses are reduced to 4% compared to equivalent silicon diodes. However, crystal defects such as dislocations and impurities within the active region of large devices affect both forward and reverse characteristic adversely. The most severe limitation for ~1cm^2 chips is the large variation in leakage current. Nevertheless, excellent dynamic switching can be maintained.

Acknowledgement

The authors benefited from valuable discussions and contributions from U. Lindefelt, B. Breitholz, H. Bleichner and A. Galeckas as well as the entire ABB SCRIPT technology team.

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Materials Science Forum Vols. 338-342 (2000) pp. 1427-1430

High-Power P-Channel UMOS IGBT's in 6H-SiC for High Temperature Operation

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Keywords: High Power, High Temperature, Insulated Gate Bipolar Transistor, P-Channel

Abstract

P-channel UMOS IGBTs in 6H Silicon Carbide were fabricated and characterized for temperatures ranging from room temperature to 400°C. These devices exhibited much higher reliability at high temperature than typically observed for SiC n-channel MOSFETs. A blocking voltage of 400 V was measured for a 0.02 cm^2 device at room temperature. Differential specific on-resistance ($R_{on,sp}$) at V_g = -30 V and V_{CE} = -5 V is measured to be 431 mΩ-cm^2 at room temperature, which decreases to 80 mΩ-cm^2 at 400°C. A collector current of 2.0 A was measured at 400°C for a 0.02 cm^2 IGBT.

Introduction

Insulated Gate Bipolar Transistors (IGBTs) [1] offer an excellent combination of high blocking voltage, low on-state voltage drop, reasonable switching speed, I-V safe operating area and MOS gate control. In silicon carbide (SiC), N-channel IGBTs [2] are not attractive because low resistivity p-type substrates are not presently available in SiC. P-channel UMOS IGBTs in 4H-SiC [3] utilizing low resistivity n-type substrates were reported previously. However these devices had poor room temperature on-state characteristics due to non-ideal p-type ohmic contacts and a high threshold voltage for the PMOSFETs. In this paper, we present high power, high temperature (2.0 Amp. at 400°C) p-channel UMOS IGBTs in SiC, using the 6H polytype in order to obtain a lower PMOS threshold voltage and improved p-type ohmic contacts. The use of the 6H polytype is detrimental to a vertical unipolar device because resistance in the drift region is the dominant contributor to the on-resistance ($R_{DS,on}$) due to the very poor vertical electron mobility for 6H-SiC (85 cm^2/V-sec) as compared with that of 4H-SiC (~900 cm^2/V-sec) [4]. However, this problem is not nearly as severe in the case of a bipolar device such as an IGBT, which relies on a significant level of conductivity modulation for on-state current conduction.

Device Fabrication

The epitaxial structure used for this device includes a 3 μm thick, $1x10^{17}cm^{-3}$ doped p-type buffer layer grown over an n^+ 6H-SiC substrate, followed by a thick low doped (15 μm, $5x10^{15}cm^{-3}$) p-type voltage blocking layer, an n-type emitter (2 μm, $2x10^{17}cm^{-3}$) and a highly doped (0.7 μm, $1x10^{20}cm^{-3}$) p+ layer as shown in Figure 1. The p+ epilayer was RIE etched to isolate the p+ emitter regions, followed by a nitrogen ion implant to form the body contact regions. The devices were then mesa isolated using RIE etch. The edge termination was performed using junction termination extension (JTE) nitrogen implantations. An implant activation was then performed at 1650°C. The gate trenches were formed by reactive ion etching after implant activation. An 800 Å thick oxide layer was then deposited by LPCVD, which was densified in wet O_2 at 950°C for 3 hours to reduce the surface state density [5]. Molybdenum was sputtered immediately after the densification of the oxide to form the gate electrode, and nickel was deposited for both p-type and n-type ohmic

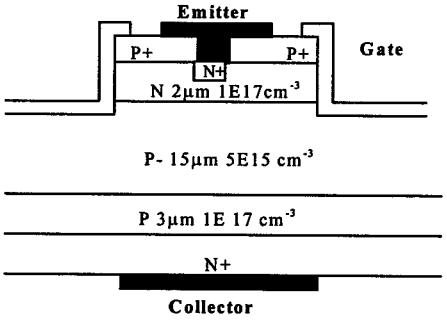

Figure 1. P-channel UMOS IGBT in SiC

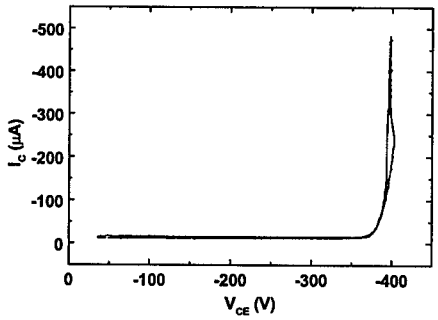

Figure 2. Blocking Characteristics of a 0.02 cm^2 6H-SiC IGBT.

contacts. After the ohmic contact anneals, a 1.5 μm thick Ti/Pt/Au layer was deposited as an overlayer. The unit cell pitch of the resulting device was 16 μm and the channel packing density in the active area was 1290 cm/cm^2.

Experimental Results and Discussion

Characterization of the IGBTs was performed on a high temperature probe station using a Tektronix 370A curve tracer. Breakdown voltage measurements were performed by covering the device in Fluorinert^{TM}. Figure 2 shows the blocking characteristics of a 6H-SiC IGBT with an area of 0.02 cm^2. The device exhibited a non-destructive breakdown at voltages up to 400 V, which is below the blocking capability of the p- drift region. This is possibly due to a rough surface caused by RIE etching during the mesa isolation processing step, resulting in premature breakdown of the blocking pn junction in the JTE region. Figure 3 and 4 show the on-state characteristics of a 6H-SiC IGBT at room temperature. A collector current of 1.4 A was measured at V_g = -40 V and V_{CE} = -14 V. Figure 4 shows the behavior of this device at low collector and gate biases. The device exhibited low current, MOSFET-like characteristics for drain biases lower than –2.6 V due to leakage currents at the bottom large area pn junction. For drain biases greater than –2.6 V, the injecting junction turned on and normal IGBT characteristics were observed. This junction leakage can be modeled as a parallel resistor to the injecting pn junction. Therefore a certain amount of current (in this case, approximately 1 mA) is necessary to turn on the pn junction. Figure 4 depicts that the I-V curve with a gate bias of –17 V does not show IGBT characteristics because the collector current

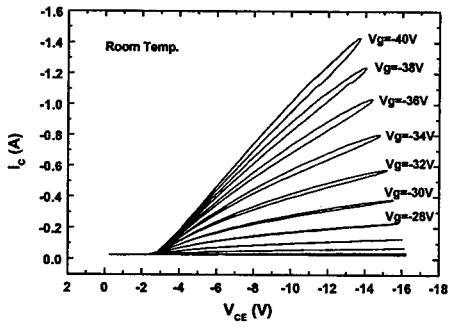

Figure 3. On-state characteristics of a 0.02 cm^2 6H-SiC IGBT at room temperature.

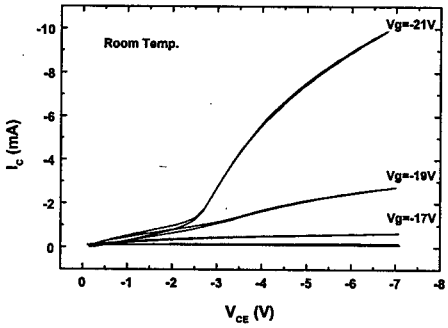

Figure 4. On-state characteristics of a 0.02 cm^2 6H-SiC IGBT at low drain and gate biases.

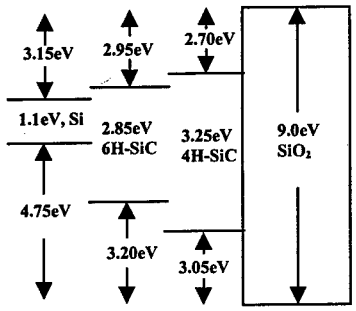

Figure 5. The energy band of 6H-SiC and 4H-SiC with respect to SiO_2 [6].

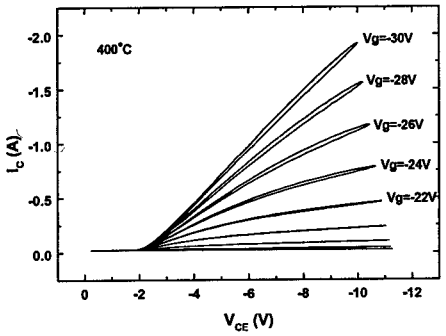

Figure 6. On-state characteristics of a 0.02 cm^2 6H-SiC IGBT at 400°C, with on-current of 2 Amps.

is always lower than –1 mA, and therefore fails to turn on the injecting bottom pn junction. This phenomenon is not observed when the whole structure is mesa isolated, as demonstrated in previous designs [3].

PMOS devices in 6H-SiC have a barrier against Fowler-Nordheim tunneling of 3.20 eV, which is greater than those of other MOS structures currently available in silicon carbide (2.95 eV for NMOS in 6H-SiC, 2.70 eV for NMOS in 4H-SiC, 3.05 eV for PMOS in 4H-SiC) [6]. The combination of the higher resistance to hole injection into the oxide and the exceptional stability of pn junctions in 6H-SiC enables operation of these p-channel IGBTs in 6H-SiC at temperatures up to 400°C. The on-state I-V characteristics of a 6H-SiC IGBT with an area of 0.02 cm^2 at 400°C is shown in Figure 6. This device demonstrated a collector current of 2.0 A at a V_g of –30 V and a V_{CE} of –10 V, which corresponds to 100 A/cm^2. To examine the effect of temperature on the device, the collector current was measured at a fixed gate bias of –30 V for temperatures ranging from room temperature to 400°C (Figure 7). The values of differential specific on-resistance were extracted from these curves at V_{CE} = -5 V and plotted as a function of temperature in Figure 8. The value of differential specific on-resistance ($R_{on.sp}$) decreased dramatically from 431 mΩ-cm^2 at room temperature to 80 mΩ-cm^2 at 400°C (Figure 8). This decrease is believed to be due to the combination of improvement of p-type emitter contact resistance, shift of PMOS threshold voltage toward zero, an increase of the PMOS channel mobility, and an increase of the current gain of the NPN transistor. The PMOS threshold shift and improvement of the bipolar current gain with

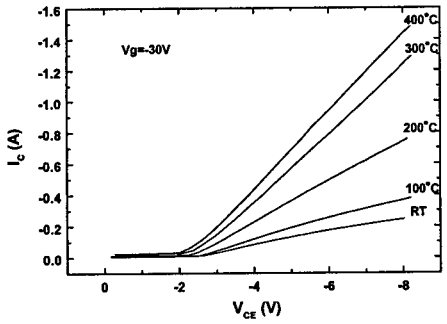

Figure 7. IV characteristics of a 0.02 cm^2 6H-SiC IGBT at temperatures ranging from room temperature to 400°C (V_g=-30V).

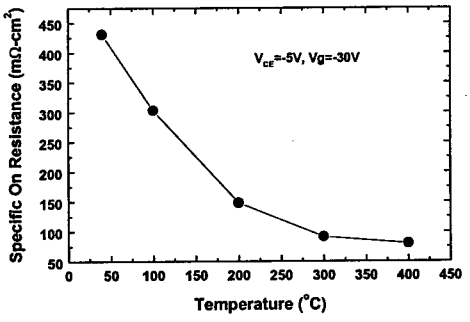

Figure 8. Differential specific on-resistance as a function of temperature at V_{CE}=-5V and V_g=-30V.

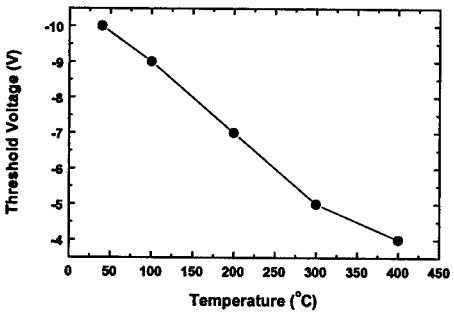

Figure 9. Threshold voltage of a 6H-SiC IGBT as a function of temperature.

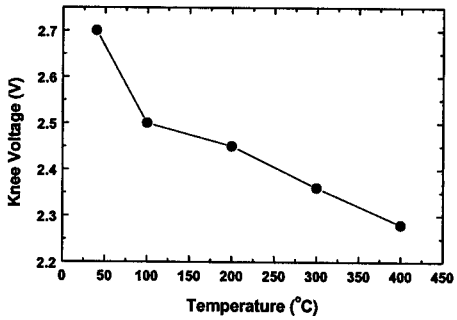

Figure 10. Knee voltage for a 6H-SiC IGBT as a function of temperature

temperature are believed to be the dominant causes for this increase. The PMOS threshold voltage (V_t), which is defined as the gate bias at which the IGBT starts flowing more than 20 μA of collector current at a fixed collector bias (V_{CE} = -5 V), is plotted as a function of temperature in Figure 9. V_t shifted from –10 V at room temperature to –4 V at 400°C. This is primarily caused by the change in trapped charge in the MOS interface states due to the shift of the Fermi level toward midgap with increasing temperature. The knee voltage, which is defined as the magnitude of V_{CE} at which the device starts showing an increase of I_C with respect to V_{CE} greater than 833 mV/dec at a fixed gate bias (V_g = -30 V), is plotted in Figure 10 as a function of temperature. The knee voltage shifts from 2.7 V at room temperature to 2.28 V at 400°C, or about -1.13 mV/°C.

Summary

P-channel UMOS IGBTs in 6H-SiC were fabricated and characterized at temperatures from room temperature up to 400°C. The 6H-SiC IGBT with an area of 0.02 cm^2 demonstrated a blocking voltage of 400V at room temperature in Fluorinert. A differential $R_{on,sp}$ of 431 mΩ-cm^2 at V_g = -30 V and V_{CE} = -5 V was measured at room temperature, which decreased to 80 mΩ-cm^2 at 400°C. The main causes of this decrease are the shift in the PMOS threshold voltage toward zero and enhanced current gain of the wide base NPN transistor at elevated temperatures. The IGBT demonstrated a high collector current of 2.0 A at 400°C (100 A/cm^2).

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Materials Science Forum Vols. 338-342 (2000) pp. 1431-1434

High Temperature 4H-SiC FET for Gas Sensing Applications

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Keywords: Device Function, Gas Sensors, High Temperature, MOSFET

Abstract

A gas sensitive silicon carbide MOSFET device for use at high temperatures has been developed and fabricated. Intermediately doped source and drain extension regions were employed to improve the device stability. The gas sensitivity was attained by the use of catalytic gate metals, $TaSi_x$ and platinum. MOSFET operation was confirmed up to a temperature of 700°C, and gas response up to 775°C. Two-dimensional numerical device simulations were performed to analyze the device operation.

Introduction

Silicon carbide (SiC) is an ideal material for the production of high temperature devices that need to function in aggressive environments. It is eminently suitable for use as a hydrocarbon gas sensor for combustion engine monitoring. To date, only SiC Schottky diodes and MOS capacitors have been investigated in this capacity [1]. A MOSFET should produce a gas sensor with better performance, but to date no MOSFET devices have been reported which function for extended periods at temperatures higher than 500°C [2]. This paper describes the design and production of a SiC MOSFET intended for operation as a hydrocarbon gas sensor at 600°C and above.

Device Design

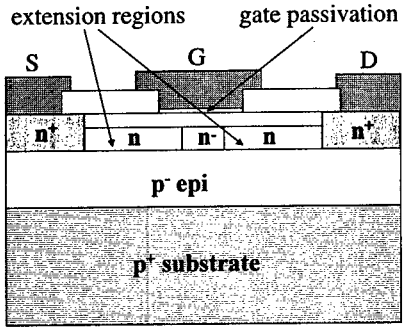

Figure 1. MOSFET sensor design

The cross section of the FET is shown in Fig.1. It is able to function as a gas sensor by the application of a catalytic gate metal. It has previously been shown that it is necessary to have an oxide layer, preferably relatively thick, under the catalytic metal in order for it to function as a gas sensor [3]. However, a common failure mechanism of FET devices at increased temperatures is failure of the gate oxide [4]. It is clear that a high quality oxide is required. It has been observed that damage caused by ion implantation can degrade the oxide quality [5]. Source and drain regions created by high implantation doses therefore lead to the production of poor quality oxide at the point where the gate oxide overlaps these regions. In our design, extension regions to the source and drain were created by a medium-dose single-energy implantation, which minimizes surface damage and enables the oxide which overlaps these regions to be of higher quality. The single-dose implantation also removes the

main channel region away from the surface and its associated effects. A single-energy implantation into the channel region permits adjustment of the threshold voltage. A threshold voltage around 0V was desired in order to minimize the required gate bias, thus creating minimum stress on the oxide and prolonging the device lifetime.

Fabrication

The devices were processed on 4H-SiC, as its wider band-gap promotes improved high-temperature performance. Source and drain regions were fabricated by multiple-energy nitrogen ion implantations at 500°C into epitaxial p-type material on a p-type 4H-SiC substrate. The implantation doses and energies were chosen so as to obtain a box-like nitrogen concentration of around 10^{20} cm^{-3}. The extension regions and the channel region received single-energy nitrogen ion implantations, 5×10^{18} cm^{-3} in the source and drain extensions, and 1 - 2×10^{17} cm^{-3} in the channel region. Two different doses into the channel region were investigated, and for comparison, some devices did not receive any channel implantation. The wafers were annealed at 1700°C to activate the nitrogen and to remove the implantation damage. The field passivation upon which the contact pads lay consisted of a stack of thermal silicon dioxide, LPCVD silicon oxide and LPCVD silicon nitride. The gate dielectric consisted of 50 nm thermal silicon dioxide, with a thin (30 nm) silicon nitride layer on the top to act as protection during the subsequent ohmic contact formation. C-V measurements on test wafers showed that the presence of the nitride layer did not affect the quality of the gate dielectric. The interface state density was calculated to be 3×10^{11} $cm^{-2}eV^{-1}$. Ohmic contacts to the source and drain regions, and to the backside of the wafer, were formed by sintering 100 nm nickel at 950°C. The catalytic gate metal consisted of 10 nm tantalum silicide plus 100 nm platinum. This catalytic metal stack has previously been developed by the centre of excellence, S-SENCE, at Linköping University, Sweden [1]. A similar but thicker metal stack was used to form contact pads.

Characterization

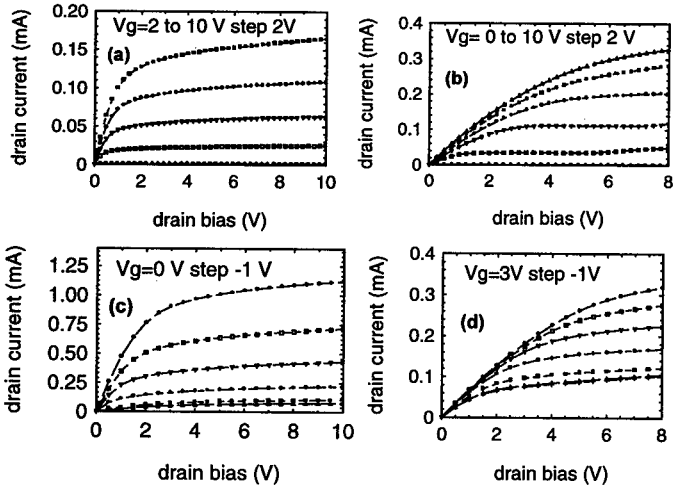

Figure 2. FET characteristics at room temperature and 600°C
(a) 20°C (b) 600°C (low-dose implantation)
(c) 20°C (d) 600°C (high-dose implantation)

Device characterization was carried out in the temperature range 20 – 700°C. It was observed that those devices that received the lower channel implantation dose were "normally off" at room temperature with a threshold voltage of about 2V. Those that received the higher dose were "normally on" at room temperature. All implanted-channel devices showed a well-behaved turn-on and turn-off up to 600°C. At higher temperatures, the normally-off devices showed instabilities, but the normally-on devices were operable up to 700°C. The common-source curve families at room temperature and at 600°C are plotted in Fig.2. The MOSFETs with no channel implant were found to have very high threshold voltages (above 10 Volts) and low drain currents. The corresponding inversion-layer electron mobility was below 1 cm^2/Vs at room temperature, but this increased to approximately 10 cm^2/Vs at 200 - 300°C.

Simulation

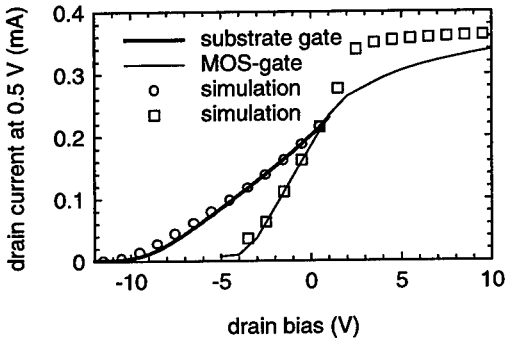

Figure 3. Simulated and experimental curves.

Simulation of device operation with MOS gate control and with substrate control was carried out using 2-dimensional MEDICI software. Both simulated and experimental curves are shown in Fig.3. It is seen that a good fit is obtained between simulation and experiment, except for the case of high positive bias on the MOS gate. According to the simulation the drain current should abruptly saturate as soon as the inversion channel is formed because the inversion-channel mobility is much lower than the bulk value. The experimental curves however show that the drain current continues to increase with the gate voltage. This might be caused by large fluctuations of the Fermi level at the oxide interface, a phenomenon which has previously been reported in the literature [6].

Gas Response

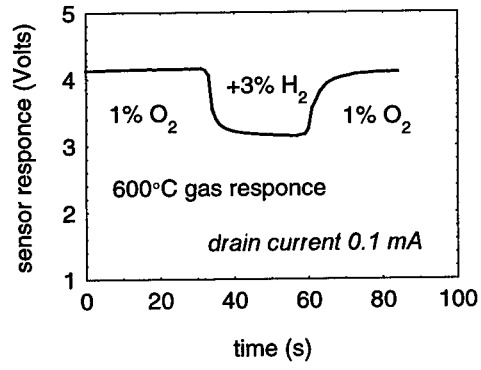

Figure 4. MOSFET sensor response

The implanted-channel MOS devices fabricated in this study were found to show a strong gas response up to a maximum temperature of 775°C. Fig.4 shows an example of the response of these devices to an intermittent flow of hydrogen- and oxygen-rich gas. The response is defined as the drain voltage required to maintain a constant current through the device. During the measurement, the gate was shorted to the drain, and the substrate was held at the same potential as the source.

Simulation shows that the introduction of a hydrocarbon-rich ambient effectively decreases the gate metal workfunction by approximately 1 eV and thus causes the drain current to increase (at a constant drain voltage). This is in agreement with expectations based on earlier results for Schottky diode and MOS capacitor gas sensors [1, 3].

More details of the gas sensor properties of these silicon carbide MOSFET devices is presented in a parallel publication by the S-SENCE group, Linköping University, Sweden [7].

High-Temperature Stability

The gas response of the MOSFET sensors was monitored as a function of time in intermittent flows of hydrogen- and oxygen- rich gas mixtures. At 500°C, the devices operated for more than 24 hours without any significant change in the sensor signal. However, at 600°C, although they operated for more than 15 hours without failure, the voltage required to maintain a constant current through the devices steadily increased with time. At 775°C, the devices failed within 10 minutes.

At 775°C, disruption of the narrowest metal lines was observed after failure [7]. This was probably caused by catalytic etching of the metal by the hydrogen and oxygen gases. This effect also occurs at lower temperatures, but increases with increasing temperature.

Further tests at 600°C in air showed that the device stability is strongly dependent on the MOS-gate bias. At an elevated gate bias the drain current slowly decreased over a few hours. However at lower gate bias, the devices showed stable operation for several hours without failure. The gate leakage current remained at a low value throughout all measurements. This indicates that the device failure mode in air is not related to failure of the contacts or to gate oxide breakdown, but is probably related to threshold voltage instability due to charge injection.

The stability of the ohmic contacts used in these devices has been investigated in a separate study. The results of this study are reported in a late news publication[8].

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High Temperature Gas Sensors Based on Catalytic Metal Field Effect Transistors

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Keywords: Catalytic Metal, Gas Sensors, High Temperature, MOSFET

Abstract
Catalytic metal insulator silicon carbide field effect devices, MISiCFET, have been developed as gas sensitive devices. They functioned in a corrosive atmosphere of hydrogen / oxygen alternating pulses up to 775°C. At 600°C some devices operated with full gas response to hydrogen for 17 hours. Below a temperature of 500°C the gas response of the devices was very stable with no base line drift for several days. MISiC Schottky diodes have been used for cylinder specific monitoring of an engine and exhausts and flue gas diagnosis. The MISiCFET devices will increase the number of possible applications for FET gas sensor devices.

Introduction

It has previously been shown that catalytic metal insulator silicon carbide, MISiC sensors, based on capacitor devices can be operated up to 1000°C. Even at this temperature (for a short time), the flat band voltage of the devices changes to a lower value in a reducing atmosphere as compared to an oxidising atmosphere [1]. MISiC Schottky devices with catalytic metal contacts have shown a similar response in their IV characteristics to a change between oxidising and reducing atmospheres [2]. The speed of response was investigated for the Schottky devices and shown to be in the order of a few milliseconds [3]. Accordingly cylinder specific monitoring of exhaust gases was demonstrated [4]. Furthermore, the Schottky diode sensors have been tested for exhaust and flue gas diagnosis [5,6]. The advantage of the Schottky diodes, as compared to the capacitor devices, is the simple electronic circuitry required for operation of the sensors. The disadvantage is the lower temperature stability of the Schottky diodes. The MISiC diodes fail at about 750°C and one reason for that can be intermixing of materials at the metal - silicon carbide interface. The introduction of a thin insulator under the catalytic metal, 1nm of SiO_2 created by ozone exposure [7], significantly increased the reproducibility of the Schottky diode gas sensors. However, their temperature stability was not improved. Field effect transistors with a catalytic metal gate combine the advantage of high temperature stability, since these devices have a thick oxide like the capacitors, with simple electronic circuitry like the diodes. In this paper we present for the first time results from MISiC transistor devices with platinum gates that respond to an alternating hydrogen / oxygen atmosphere at temperatures above 650°C.

Experimental

Catalytic Metal Insulator Silicon Carbide Field Effect Transistors, MISiCFETs, were designed and processed by ACREO (formerly IMC), Kista, Sweden. The devices were processed in 4H SiC, as described elsewhere [8]. The cross section of the FET is shown in Fig. 1. The channel region was implanted with a single-energy nitrogen ion dose. Two different doses were investigated. The FETs with the lower dose were subsequently found to be "normally off" while the higher dose produced

"normally on" devices. The channel width is 200 μm and the channel length is 2 μm. The gate areas had a finger shaped design of 1-,3-, or 10-fingers, and each finger has catalytic metal over an area of 20 x 210 μm. The gate dielectric consists of 50 nm thermally grown SiO_2 with a 30 nm LPCVD silicon nitride on top. The metal stack on the gate consisted of 10 nm $TaSi_x$ and 100 nm Pt and was deposited by magnetron sputtering. The layout connected the gate and drain together. This created a "two terminal" device, which produced diode-like I-V characteristics. The sensors were gold bonded and glued to ceramic substrates that could be heated. The substrates were mounted with an air gap to 16 pin holders. The IV curves of a normally off device was recorded in different gas ambients, see Fig.2. The sensor signal is the voltage at a constant current of 0.1 mA, and the difference between the signal in e.g. oxygen and hydrogen is the gas response [3]. Gases, of 99.99 % pureness or better, were supplied from a gas mixing system. The total gas flow was 200 ml/min.

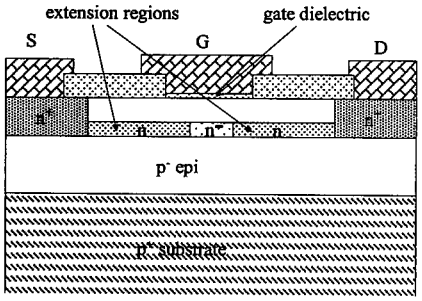

Fig. 1. Cross section of the MISiCFET device design.

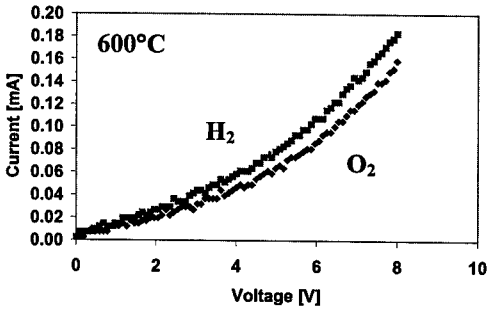

Fig. 2. The IV characteristics in $1\%O_2/N_2$ and $3\%H_2/1\%O_2/N_2$, respectively, at 600°C for a 4H SiC MOSFET. This normally off device has a layout, where gate and drain are connected together.

Results

In this first device design both normally off and normally on FET transistors were produced. About 4-5 V lower gate /drain voltage was needed for the normally on devices, compared to the normally off devices, to maintain a constant current of 0.1 mA between source and drain. Most of the tests were performed on the normally off devices and will be reported here. Three different gate-finger structures were tested, with 1-, 3-, and 10-fingers, respectively. There was no large difference between structures with different numbers of gate-fingers. The device characteristics were very similar at room temperature for devices from the same batch and the same processing scheme. The sensors showed larger differences when the temperature was raised. The combination of gate metals used for high temperature operation [4], demands an activation procedure before full gas response is achieved. The activation was performed in an alternating gas ambient of $3\%H_2/1\%O_2/N_2$ (30s) and $1\%O_2/N_2$ (60 s), respectively. About three hours at 550°C performed the necessary activation here. This alternating hydrogen / oxygen atmosphere was also used to simulate corrosive conditions during the testing of the MISiCFET devices. The response to hydrogen is defined as the difference in sensor signal in the oxygen and hydrogen atmosphere, see insert in Fig. 3.

At temperatures below 500°C, the lifetime of the tested components was very good. Sensor devices have been running in the lab in the simulated corrosive atmosphere for several days without any special baseline drift or decrease of the gas response. Figure 3 shows a 3-finger gate MISiCFET device operated at 500°C. There is no baseline drift and a very stable gas response during 24 hours of operation. Instability in the gas response is seen during the first hours of operation, but the origin

of this is not known. Three 10-finger gate sensors were operated for 17 hours with full gas response at a temperature of 600°C. The baseline showed some drift to higher voltages during this operation.

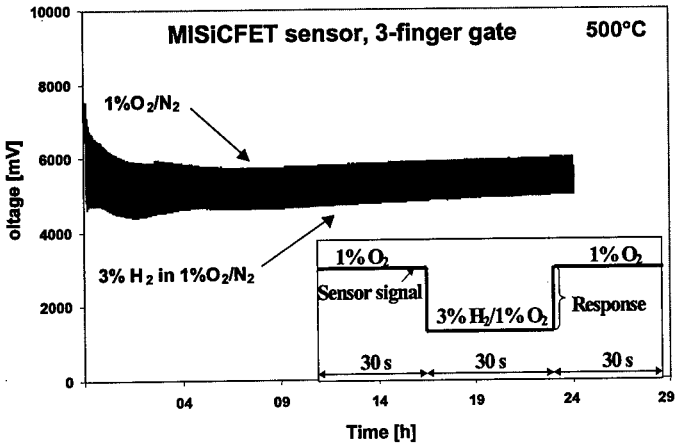

Fig. 3. The sensor signal at 500°C for a 3-finger gate "normally off" device. Carrier gas,1% O_2 in N_2. Insert: Schematic of the gas exposure sequence and the sensor signal.

Figure 4 shows two 1-finger gate sensors operated at 650°C. A small drift towards lower voltages is now recognised, as well as some instability in the pulse response. The highest possible operation temperature was investigated and shown to be 775°C. All sensors failed after less than 10 min at this temperature. A microscope inspection revealed disruption of the narrowest lines in the sensor gate metal pattern to be the reason for failure. The metal had evaporated, probably due to catalytic etching in hydrogen and oxygen at this high temperature [9]. This means that a different design might increase the temperature stability. The testing of the devices also showed that a lower gate bias increased the device lifetime, in accordance with earlier results [10]. As shown in measurements on three terminal devices [8], the gate leakage current remained low throughout the measurements, indicating that the threshold voltage instability is due to charge injection.

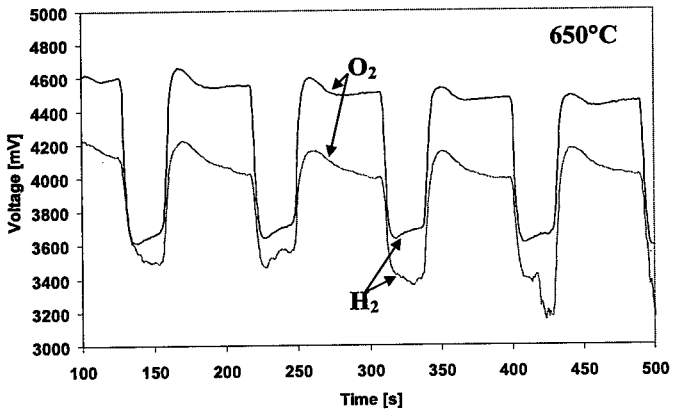

Fig. 4. The sensor signal for two devices that are 3-finger "normally off". The gas ambient is changed between 1%O_2/N_2 (60 s) and 3%H_2/1%O_2/N_2 (30s), respectively.

Summary
Catalytic metal insulator SiC transistor devices operated as gas sensors are demonstrated for the first time. These devices have the potential to combine the good high temperature stability properties of capacitors with the simple electronics of Schottky diodes. It was possible to run the sensors at 600°C for 17 hours in pulses of hydrogen and oxygen. Definite failure occurred at 775°C, due to disruption of narrow lines in the gate metal pattern. A new design might increase the high temperature performance. The sensors are good candidates for applications at high temperature and in aggressive environments.

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SiC-Based Gas Sensor Development

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Keywords: Electronic Nose, Emission, Gas, High Temperature, Hydrocarbon, Packaging, Sensor

Abstract: Silicon carbide based Schottky diode gas sensors are being developed for applications such as emission measurements and leak detection. The effects of the geometry of the tin oxide film in a Pd/SnO_2/SiC structure will be discussed as well as improvements in packaging SiC-based sensors. It is concluded that there is considerable versatility in the formation of SiC-based Schottky diode gas sensing structures which will potentially allow the fabrication of a SiC-based gas sensor array for a variety of gases and temperatures.

1.0 Introduction

Silicon carbide-based gas sensors are of considerable interest since they can be operated at high temperatures and detect gases, such as hydrocarbons (C_xH_y) and nitrogen oxides (NO_x), which are of interest in various applications such as emission monitoring and leak detection. Our development of SiC-based gas sensors has centered on investigations of gas sensitive Schottky diodes. The major advantage of a Schottky diode in gas sensing applications is its high sensitivity. While a simple palladium (Pd) on SiC (Pd/SiC) Schottky diode structure has the advantage of high sensitivity, these sensors drift with extended heating at high (400° C) temperature [1]. Efforts are underway to stabilize the Schottky sensor structure for long-term, high temperature operation [2].

One approach incorporates chemically reactive materials such as metal oxides into a SiC-based metal-insulator-semiconductor (MIS) Schottky diode structure. Unlike Si-based electronics, SiC-based devices can be operated at high enough temperatures for these materials, e.g. tin oxide (SnO_2), to be reactive to C_xH_y and NO_x. This results in a metal-reactive insulator-semiconductor (MRIS) gas sensor structure. Potential advantages of this structure include increased sensor sensitivity and stability. Varying the reactive insulator composition can vary sensor selectivity to various gas species. We previously demonstrated this structure with SnO_2 as the reactive insulator and compared the reactive insulator sensor response to that of a Pd/SiC structure on the same chip (Figure 1a) [2]. The MRIS sensor showed improved stability and different response than the Pd/SiC sensor.

This approach, combined with metal-alloys directly on SiC [2], potentially yields wide flexibility in the design and operational capabilities of SiC-based gas sensing Schottky diodes. Various reactive oxides and metal alloys can be combined within the Schottky diode structure to tailor the diode response to specific applications. Work is on-going to develop a high temperature electronic nose consisting of an array of appropriately tailored gas sensors based on SiC and other materials [3]. However, this work depends on the ability to package these sensors for the appropriate operating conditions. This paper discusses our on-going development of SiC-based gas sensors. First, the effect of the geometry of the insulator on the MRIS sensor behavior was studied. Second, a prototype sensor package allowing high temperature operation of the sensor in ambient conditions will be discussed.

2.0 Device Fabrication and Testing

The SiC-based sensors are fabricated from chips with a 4-5 μm thick alpha-SiC epilayer grown by chemical vapor deposition on a commercially available off-axis alpha-SiC substrate. A backside contact is achieved by sputtering aluminum onto the bottom of the wafer. The MRIS sensor investigated in this work is shown schematically in Figure 1b. A thin layer of approximately 50 angstroms (Å) of SnO_2 is sputter deposited onto half of the as-grown SiC epilayer surface (layer SnO_2 configuration). On both halves of the wafer, open circular patterns of 200 µm diameter were formed using photoresist. The SnO_2 layer half (left half of Figure 1b) of the wafer was then covered masking off the circular photoresist patterns; on the other half of the wafer 50 Å SnO_2 contacts (diode SnO_2 configuration) were formed by sputter deposition using the same parameters as the first SnO_2 deposition. The layer side was then uncovered and circular palladium (Pd) contacts approximately 400 angstroms (Å) thick were formed on both sides by sputter deposition and the subsequent lift-off. Thus, the SnO_2 is deposited completely across the surface (layered configuration on the left half of Figure 1b) on roughly half the chip while on the other half SnO_2 is deposited only beneath the Pd contact (diode configuration surface on the right half of Figure 1b). The difference between the two sides of the chip is the geometry of the SnO_2 layer beneath the Pd. This is in contrast to the previous tests (Figure 1a) where half the chip had the SnO_2 layer beneath the Pd and the other half had no SnO_2 at all beneath the Pd.

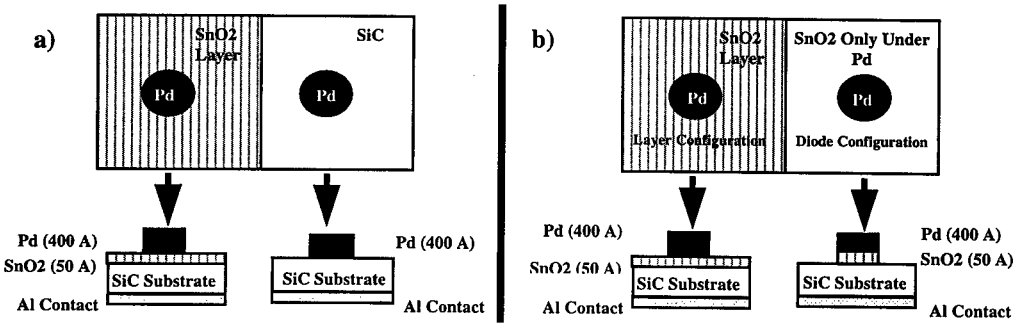

Figure 1: A schematic drawing of the test structures for: a) the MRIS approach which compared a Pd/SiC diode to a $Pd/SnO_2/SiC$ diode. (Ref. 2) b) the effect of the reactive insulator (SnO_2) geometry on the sensor behavior of a $Pd/SnO_2/SiC$ diode.

The gas sensor testing facility and sample connections have been described elsewhere [1]. The sample rested on a hot stage whose temperature is controlled from room temperature to 425°C. Current-time (I-t) measurements were taken to characterize the diode response as a function of time during exposure to a variety of gases, and current-voltage (I-V) measurements were taken to characterize the diode's electronic properties in a given environment. The forward voltage at which the current is measured is chosen to maximize diode response and minimize series resistance effects.

3.0 Results and Discussion

3.1 Effects of Reactive Insulator Geometry

Heating the structures in Figure 1b at 350°C for extended periods has shown a difference in behavior between the layer configuration sensors and diode configuration sensors (Figure 2). Both sensors are first exposed to air (10 minutes), nitrogen plus 10% oxygen (15 minutes), nitrogen plus 10% oxygen and 2500 ppm hydrogen, denoted as H_2 mix, (15 minutes), followed by nitrogen plus 10% oxygen (5 minutes) and air (10 minutes). The diode configuration sensor has nearly no response to H_2 at this concentration while the layer configuration sensor has a significant response. Comparison of the I-V curves of the two configurations is shown in Figure 3. The layer configuration sensor shows exponential behavior at low voltages and series resistance behavior at higher volt-

ages. An increase in the current for a given voltage is noted upon exposure to H_2 for this sensor. However, the diode's H_2 sensitivity is less than that noted for the previously investigated $Pd/SnO_2/SiC$ sensor with a layer SnO_2 configuration [2].

The diode configuration sensor shows complicated behavior as a function of voltage. In air, exponential I-V behavior is noted below 0.4 V. The slope of the exponential changes near 0.4 V and remains nearly constant from 0.4 to 2.5 V. The sensor does not respond to H_2 at this concentration below 1.5 V, while between from 1.5 to 2.5 volts a small response to H_2 is noted. Above 2.5 V, series resistance behavior is noted in both the air and H_2 mix curves. This sensor does not have the standard Schottky diode characteristics noted in Pd/SiC diodes previously investigated [1]. In contrast to the results of reference 2, the layer configuration sensor exhibits more standard Schottky diode behavior. Thus, the diode configuration sensor behavior is obviously different than that of the layer configuration sensor. These results suggest that the geometry of the reactive insulator, i.e. whether the SnO_2 covers the whole region around the sensor or just underneath the diode, affects the behavior of the sensor. The underlying reason for the effect will be investigated in future studies.

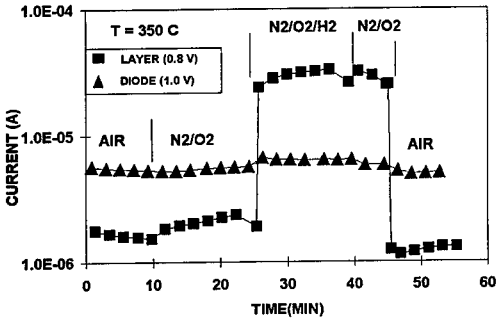

Fig.2. The forward current vs time at 350°C upon exposure to H_2 mix of the layer configuration sensor and diode configuration sensor.

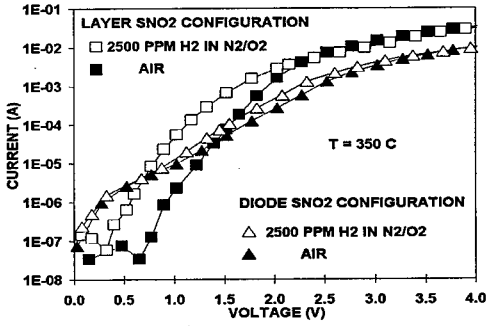

Fig.3. The logarithmic I-V curve at 350°C in air and in the H_2 mix of the layer configuration sensor and diode configuration sensor.

These results have some similarities to those seen when comparing the Pd/SiC sensor to that of the $Pd/SnO_2/SiC$ layer configuration sensor in reference 2. In both cases, increased sensitivity to H_2 is noted for sensors in the layer configuration compared to sensors without the layer. In summary, the diode sensitivity and stability is improved when the SnO_2 layer covers half the chip compared to that of a sensor where a SnO_2 layer does not extend beyond the boundary of the Pd contact.

The difference between the SnO_2 layer configuration sensors discussed in this work (diode 1) and in reference 2 (diode 2) is of interest. Both sensors show exponential behavior followed by series resistance behavior at higher voltages (not shown). The low voltage behavior in air of both diodes is shown in Figure 4 in a linear current scale. At lower voltages, diode 2 shows a linear I-V curve (shunt resistive behavior) until at least 0.6 V. The slope of the I-V curve gives an effective resistance of near $2*10^6$ Ω which is a value consistent with the resistance of a thin SnO_2 film. Above 0.9 V, diode 1 exhibits exponential behavior. In contrast, the I-V curve of diode 2 shows noise current below 0.8 V while above 0.8 V exponential behavior is observed. Thus, the most significant difference in the behavior of the two diodes is the shunt resistance behavior at lower voltages. These results suggest that differences in the deposition of a SnO_2 film can affect the sensor response even if the geometry of the film is the same. Possible differences in the SnO_2 film deposition parameters include thickness of the film and stoichiometry of the SnO_2.

3.2 Sensor Packaging

The ability to package a sensor for a given environment is of fundamental importance to its eventual application. One difficulty with operating sensors which function at higher temperatures than ambient is that a considerable amount of power (order of several watts) may be necessary to

properly heat the sensor. For example, temperatures above 300-400°C will likely be necessary to optimally measure gases such propylene and methane [1]. The heat power demand to achieve such temperatures may limit sensor use in some applications. Thus, the development of appropriate sensor packaging technology is necessary. Figure 5 shows the schematic of a prototype sensor package incorporating a Pd/SiC based sensor, temperature detector, and heater. The sensor resides on a micromachined diaphragm structure; this diaphragm structure minimizes the thermal mass and decreases the amount of power necessary to heat the sensor to appropriate temperatures. It also allows heating of the sensor with minimal heating of the adjoining package components. Temperatures up to 600°C have been achieved with a heater power of near 1 W. Further, at approximately 500°C, the packaged Pd/SiC sensor with a built-in heater has measured 5000 ppm of H_2, ethylene, and methane in N_2 (not shown). The methane signal has a longer response time than that of H_2 and ethylene, but has the same general shape of I-t curve. This is in contrast to the results at lower temperatures where the methane response was fundamentally different than the sensor response to H_2 and propylene [1]. However, as would be expected, degradation of the sensor response occurs with continued high temperature operation. This type of packaging can also be used for a variety of other sensors which would constitute the high temperature electronic nose.

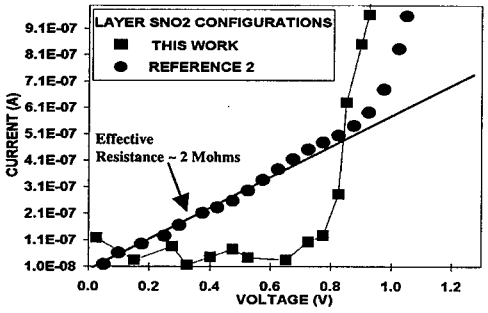

Fig. 4. The I-V curve in air on a linear current scale at 350°C of the Pd/SnO_2/SiC diode in this work and in reference 2.

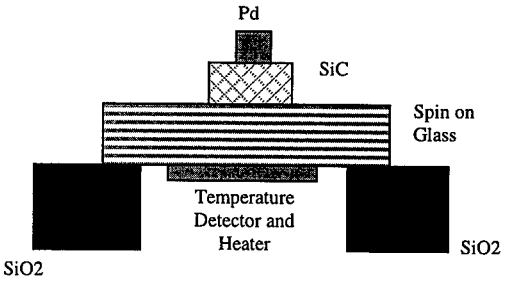

Fig. 5. Schematic drawing of sensor package for SiC-based devices.

4.0 Conclusions and Future Plans

The MRIS diode structure shows a dependence on the geometry of the insulator. Further studies with other diode geometries, reactive insulators, and processing conditions are planned. Integration of MRIS and metal alloy-SiC sensors together into an appropriate sensor package is also planned. By integrating SiC-based sensors with various structures into a sensor array, the sensor array can be tailored to meet the detection needs of a range of gas sensing applications.

5.0 Acknowledgments

The authors would like to acknowledge the contributions of Dr. J. F. Lei, Dr. G. Fralick, Dr. R. Okojie, F. DeAngelo, and Dr. D. Larkin of NASA Glenn and C. Salupo of Cortez III/NASA Glenn.
Send correspondences to G. Hunter, E-mail: ghunter@grc.nasa.gov

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Materials Science Forum Vols. 338-342 (2000) pp. 1443-1446

Fabrication of SiC Hydrogen Sensor by Pd-Implantation

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Keywords: Hydrogen Sensors, Ion Implantation

Abstract. Silicon carbide, a semiconductor, is used to fabricate an efficient high temperature hydrogen sensor. When a palladium coating is applied on the exposed surface of silicon carbide, the chemical reaction between palladium and hydrogen produces a detectable change in the surface chemical potential. Rather than applying an external palladium film we have implanted palladium ions into the silicon face of 6H, n-type SiC samples at the ion energies of 130 keV and 70 keV and various fluences at 500°C. Then each sample was exposed to low levels of hydrogen and its response measured by monitoring the current through the sample, with respect to time. The results obtained are presented in this paper.

Introduction

In the past few years has been an increasing interest in the field of gas sensors that can operate in harsh environments such as hot engine control for aerospace and automobile applications, or process gas monitoring. The requirement of operating in high temperature environments brought silicon carbide into attention, for its **remarkable** properties. Because of its outstanding thermal stability, silicon carbide, that is a ceramic material with a wide bandgap and low intrinsic carrier concentration, can operate as a semiconductor potentially up to 1000°C [1, 2]. The presence of a catalytic metal such as palladium onto (or into) silicon carbide results into a Schottky diode behavior. The gas changes the space charge region surrounding the metal clusters, which in turn affect the conductivity of the crystal. This change in conductivity is measured and can be correlated to surface concentrations of catalyst and to the concentration of the sampled gas in the environment.

Experiment

For this study of the response of silicon carbide sensors to gases, rather than depositing palladium onto the surface of silicon carbide as on [3], we implanted it into the silicon face of 6H, n-type (nitrogen doped), 3.5° off-axis orientation, silicon carbide samples provided by Cree Research Inc. The samples were implanted at 500°C, with Pd ions to fluences between 3×10^{14} at/cm^2 and 3.2×10^{16} at/cm^2, and implantation energies of 70 keV and 130 keV. The implantation energies were chosen by using the SRIM code [4], in order to get high surface concentrations of Pd ions.

The current measurements were done using a Keithley model 595 IV/CV meter interfaced to a computer, for several temperatures near 23, 70, 145, 215°C in a closed gas environment. The voltages applied were +/- 1V. The temperature was also monitored in order to correct for current fluctuations due to temperature changes. For this experiment, air was cycled with an H_2-Ar gas mixture with 4% hydrogen, and the cycles were chosen to be 2 minutes in length (a compromise between the signal rise time and the length for a complete measurement). A drawing of the experimental setup is shown in Fig. 1. The metallic contacts were made out of guilt copper, and the insulator was thick Teflon, so that the capacitance with the bottom side of the aluminum enclosure (connected to the common ground as a Faraday cage) was negligible.

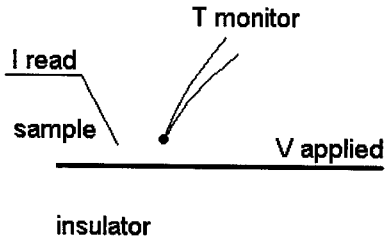

Figure 1. Schematic view of the setup.

Results

Figures 2 through 7 show that at room temperature (23°C) the current increases in the presence of the 4% H_2 in the H_2-Ar mixture, for all of the SiC implanted samples. When the H_2–Ar environment is replaced by air, the current reverts to its initial value. At higher substrate temperature, the difference between the current read-out for H_2–Ar ambient and air ambient decreases as we approach about 60°C to 84°C where it becomes zero. Continuing increasing the temperature, one can clearly see from these figures that the current at presence of H_2–Ar gas becomes definitely smaller than when air is present. For figure 7 the temperature value at which the current inversion appears is somewhere in the 140°C region (for negative voltage applied). For comparison, measurements performed on blank SiC samples revealed no current fluctuation with the gas change for any temperature in the range 23°C - 240°C. Our implanted sensor at high temperatures shows an opposite behavior in the current while exposed to hydrogen, relative to sensors reported in the literature [3, 5, 6] for SiC with palladium deposited on the surface. There, the current in the presence of hydrogen is more for every temperature level, and reverts to the initial value when air is supplied instead of hydrogen.
Similar behavior was observed for both positive and negative voltage applied (the currents for the negative voltage are shown in the graphs in absolute values). For absolute voltages above 1.2 V, the p-n junction breaks down, and no more sensing behavior can be observed.

Conclusions

From the results that we have so far, we could not observe a clear dependence of the current according to the level of implantation dose, or energy. However, one can say that the current for samples #2 (low fluence) is smaller than that of the sample #8 (high fluence, same high energy), but the order is reversed for samples implanted at lower energy and similar fluences. Further measurements with a better remote controlled experimental setup are underway at this time, in order to obtain a precise behavior.

Acknowledgements

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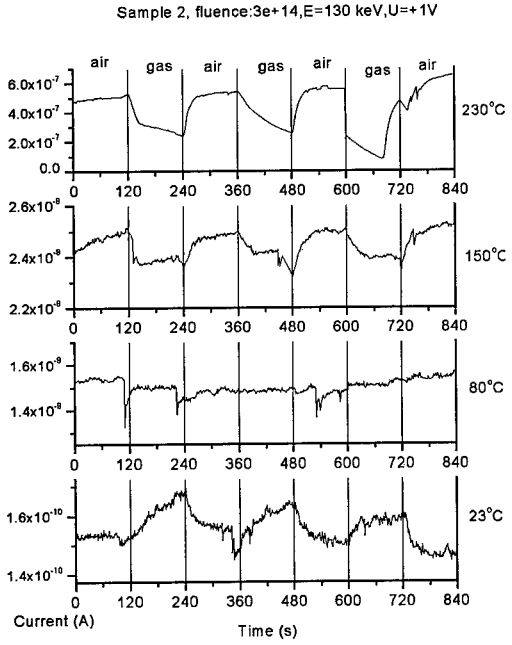
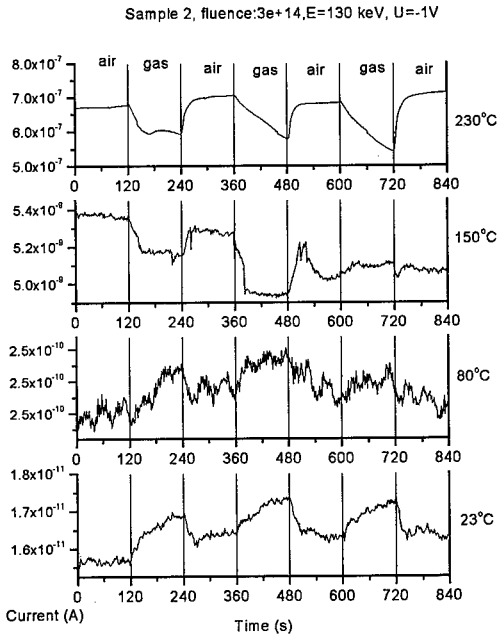


Figure 2



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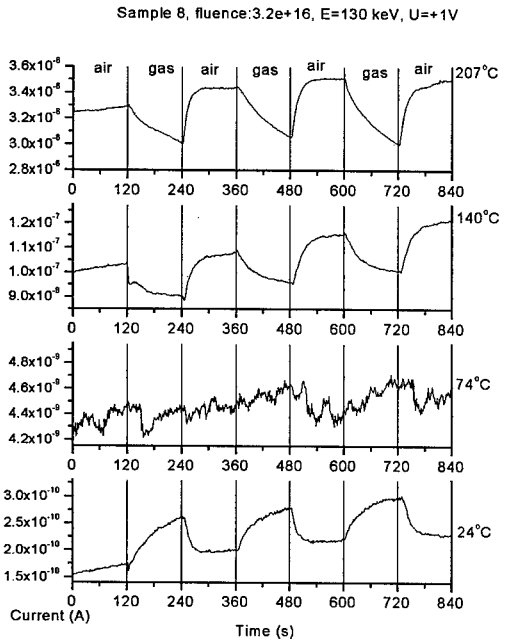

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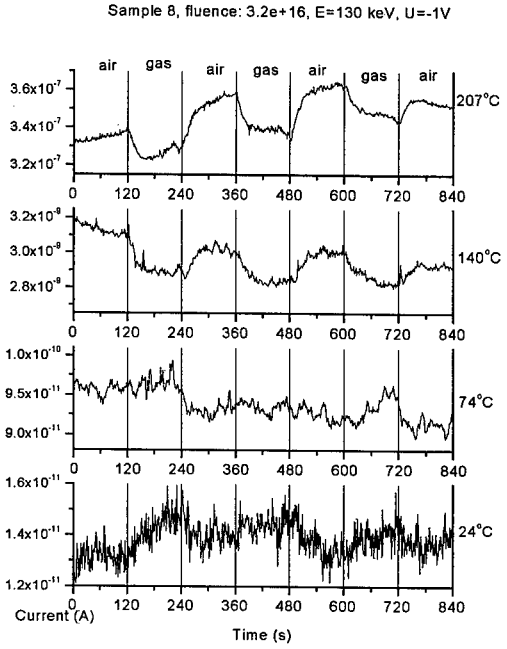

Figure 5

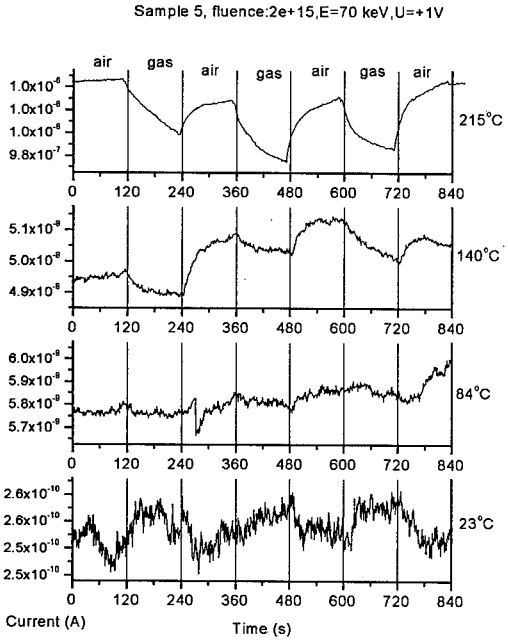

Figure 6

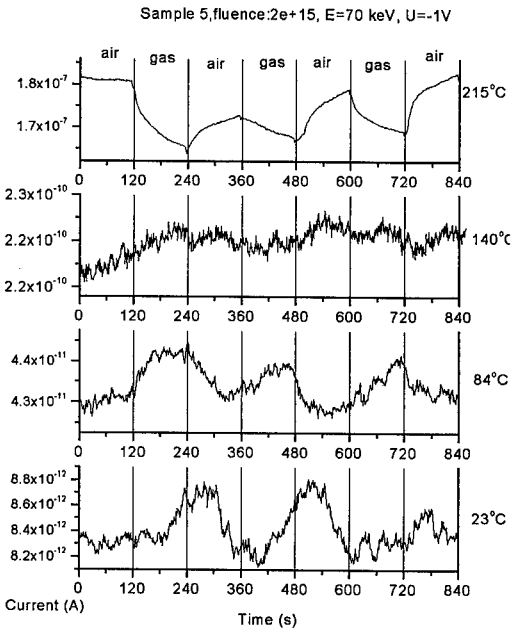

Figure 7

Materials Science Forum Vols. 338-342 (2000) pp. 1447-1450

Epitaxial 6H-SiC Layers as Detectors of Nuclear Particles

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Keywords: Alpha Particles Spectroscopy, Amplitude Spectrum, Diffusion Length, Energy of Electron-Hole Pair Formation, Nonuniformity of Lifetime, Sublimation Epitaxy

Abstract. Schottky diodes based on n-n^+ 6H-SiC epitaxial layers grown by sublimation epitaxy were used for registration of alpha particles ^{244}Cm . Specific features of nonequilibrium charge transfer were studied in regimes of total and partial structure depletion. A relationship was revealed between film characteristics and the dependence of the signal amplitude and the shape of the amplitude spectrum on diode bias.

Introduction. Application of SiC as a detector media of nuclear radiation arises from its wide energy bandgap and high radiation persistence. As a consequence detectors capable for working at high temperatures and radiation fields [1,2]. One of the perspective of SiC detectors is spectroscopy of charge particles. As shown in [3], the sublimation technique gives 6H-SiC layers with concentration of uncompensated impurities N^+_D-$N^-_A \approx 10^{15}$ cm^{-3} and hole diffusion length $L_0 \approx 2$-3 μm. These values seem to be sufficient for using the layers as ion detectors. The high fields of electric breakdown, characteristic of SiC, allow creating a space-charge region (SCR) as wide as tens of micrometers. The low concentration of nonradiative recombination centers ensures carrier lifetimes sufficiently high for effective transport.

Experimental. The Schottky diodes were fabricated by magnetron sputtering of Ni onto the surface of 6H-SiC layers. The barrier diameter was 600-1200 μm. Structures manufactured by CREE Co. (USA) were used for some methodological measurements. In contrast to the case of complete particle deceleration in the SCR, the thickness on n-type films was always smaller than the particle path length. The average signal amplitude and also the shape and full-width-at-half-maximum (FWHM) of the spectrum were inspected. The analyzer scale was calibrated using a Si-detector. Also, current-voltage and capacitance-voltage characteristics were taken. The following SiC parameters were evaluated: average energy of electron-hole pair formation ε, hole diffusion length L_0, nonuniformity of lifetime $\Delta\tau/\tau_0$ in the base of the structure, and lifetimes of carriers until their capture during drift in the SCR.

Results. The dependence of the signal amplitude on bias voltage U (Fig.1) exhibits characteristic regions of steep rise and slow growth with signal saturation (E_{sat}). This corresponds to, respectively, U values before and after total depletion of the

structure. The E_{sat} region is used to find ε. The energy E_{abs} absorbed in the film is determined by TRIM software [4] and the proportion $E_{abs}/\varepsilon=E_{sat}/\varepsilon_{Si}$ is used, where ε_{Si}=3.62 eV. For SiC films, ε≤7 eV.

The diffusion length L_0 is found from the signal deficit $\lambda=1-E/E_{abs}$. In [5] the generation density was examined as uniform and stationary; for a linear dependence of the generation density on the coordinate, G(x)=1+bx [6], we have:

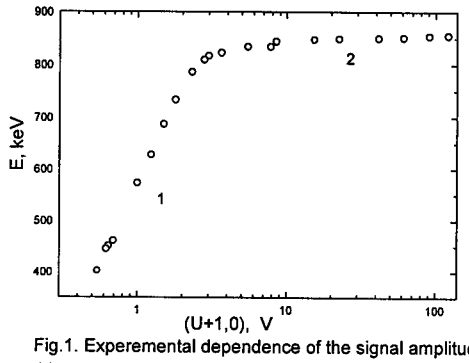

Fig.1. Experemental dependence of the signal amplitude on bias voltage on detector 1 - before, 2 - after total depletion

$$\lambda = \frac{\int_{W}^{h} G(x-W)\,[1-\exp(W-x)/L_0]\,d(x-W)}{h\,(1+bh/2)} \qquad (1)$$

where W is the SCR boundary found from capacitance measurements and h is the film thickness. Further fitting is done with respect to two parameters, L_0 and h (Fig.2). L_0 values for holes were found experimentally to be in the range from 2.4 to 0.6 μm, depending on impurity concentration in the films. Shape of the amplitude spectrum from alpha particles ^{244}Cm (E = 5.77 MeV) is used to find nonuniformity of lifetime

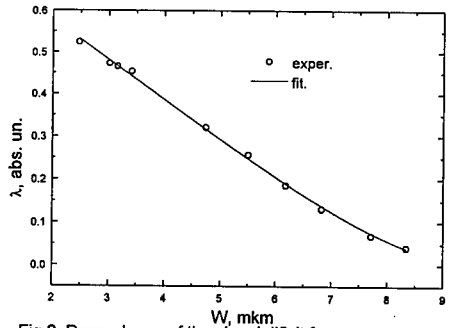

Fig.2. Dependence of the signal dificit from space - charge region boundary

in the base of the structure. The signal due to each particle reflects transport conditions in a volume ~10 μm^3; therefore, chaotic incidence of particles reveals the statistics of the lifetime τ over the detector area. The spectrum was calculated for diffusion of holes in the base, using the identity (see [7]) $dN/dq=(dN/d\tau)(d\tau/dq)$, where dN is the number of pulses in the interval dq, and q values are normalized to introduced charge. Under assumption that $dN/d\tau$ is a Gauss function with dispersion

$\sigma=\Delta\tau/2.35$ and generation is uniform with depth, the following system was obtained for dN/dq=f(q):

$$dN/dq = (\tau/\tau_0)^{1/2} \exp[-(\tau/\tau_0 -1)^2 /0.362\ (\Delta\tau/\tau_0)^2] \quad (2)$$
$$q = (W+L_0\sqrt{\tau/\tau_0}) / h$$

The parameters of the spectra are W/h, L_0 /h, $\Delta\tau/\tau_0$, with W/h only shifting the peak position and nonuniformity of τ, on the contrary, governing only FWHM. L_0 and h affect the spectrum as a whole. The modification of spectrum for three value $\Delta\tau/\tau_0$ are shown in Fig. 3. Plotting the FWHM value against L_0/h revealed the following simple relatio

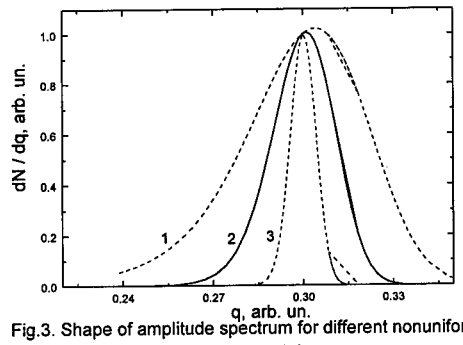

Fig.3. Shape of amplitude spectrum for different nonuniformity of lifetime; $\Delta\tau/\tau_0$: 1 - 1, 2 - 0.5, 3 - 0.2

$$(q_2 - q_1) = 0.48\ (\Delta\tau/\tau_0)\ (L_0/h) \quad (3)$$

It is significant that the values $\Delta\tau/\tau_0$=20-60% found for SiC films correspond to the average level of "detector" Si. Drift charge transfer is used to find the capture time. The signal generated upon structure depletion was calculated for the case of weak capture and generation linearly increasing into the detector. Formulas were obtained relating the signal deficit to drift displacem ent τ. The calculated data agree satisfactorily with. experiment for hole capture at τ=35 ns.

Discussion and conclusion. The experiments have shown that low concentrations uncompensated impurities and deep centres in n-type SiC layers provides the sufficient values of W and τ to create of nuclear particle detectors. In so far as the thickness on n-type films was smaller than the particle path length, the geometry of experiment was distinguished from the traditional geometry with complete particle deceleration in the region of electrical field of detectors. Specific features of nonequilibrium charge transfer were studied in regimes of total and partial structure depletion by comparison the calculate and experimental data. As shown from analysis dependence of signal amplitude and shape of amplitude spectrum on Schottky diode bias, it is possible determine characteristic of material is responsible for transport of carriers.

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Chapter 6

Growth of III-Nitrides and Related Materials

Materials Science Forum Vols. 338-342 (2000) pp. 1453-1458

GaN Quantum Dots on Sapphire and Si Substrates

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Keywords: Molecular Beam Epitaxy, Photoluminescence, Polarization, Quantum Dots, Stark Effect

Abstract: GaN dots have been grown on c-plane sapphire and (111) Si substrates by reactive molecular beam epitaxy. A new method involving two-dimensional growth followed by a controlled annealing during which dots were formed was employed. Due to localization and large dot density, relatively high luminescence efficiencies were obtained on both substrates. Single layer dots were used for AFM analysis whereas 30 layer dots were used for photoluminescence experiments. AlN layers, some too thick for mechanical interaction between stacks, and some thin enough for vertical coupling were used. Strong polarization effects lead to a sizeable red shift, which depends on the size of the dots.

Introduction

Gallium nitride and its alloys with InN and AlN have recently emerged as important semiconductor materials with applications to yellow, green, blue and ultraviolet portions of the spectrum as emitters and detectors, and as high power/temperature electronics.[1-6]

Nitride-based light emitting diodes (LEDs) with lifetimes approaching 100,000 hours (extrapolated) and brightness near 70 lm/W in the green have been obtained. These LEDs are already being used in full color displays, moving signs, traffic lights, instrumentation panels in automobiles and aircraft, airport runways, railway signals, flashlights, underwater lights. The technology is in the process of being extended to standard illumination under the name " Solid State Lighting" (SSL). SSL is expected to result in substantial energy savings by as much as a factor of six compared to standard tungsten bulbs. Along similar lines, blue lasers are being explored as the read and write light source for increased data storage density for the next generation of digital video disks (DVDs). Already, the room temperature CW operation in excess of 10,000 hours has been reported. To be versatile, this level of lifetime with a power level of about 20 mW at 60 C is required. The present device lifetimes under these more stringent operating conditions are near 400 hours which is a long way from the needed 10,000 hours.

The large bandgap of GaN with its large dielectric breakdown field, coupled with excellent transport properties of electrons and good thermal conductivity, are well suited for high power electronic devices.[7] Already, high power modulation doped field effect transistors (MODFETs) [8] with a record power density of about 10 W/mm in small devices, and a total power of 8 W in large devices have been achieved.[9] In addition to high power, and high frequency operation, applications

include amplifiers that operate at high temperature and other unfriendly environments, and low cost compact amplifiers for earthbound and space applications.[7]

When used as UV sensors in jet engines, automobiles, and coal burning furnaces (boilers), GaN-based devices will allow optimal fuel efficiency and control of effluents for a cleaner environment.[10-12] Again, this is a direct result of the large bandgaps accessible by nitrides, as well as their robust character. GaN/$Al_xGa_{1-x}N$ UV pin detectors have demonstrated sensitivities of ~0.20 A/W and speed of response of well below a nanosecond.

By necessity, GaN is predominantly grown on foreign substrates such as sapphire and the film growth proceeds in twisted and tilted columns. The case on other substrates is to a first approximation similar since none of them is lattice matched. Additional complications, which truly exacerbate the situation, involve InGaN, which forms clusters leading to sizable compositional inhomogeneities. Ironically, somehow the compositional inhomogeneities appear to give rise to efficient light emission. It is well known by now that In free active layers do not lead to efficient emission[13].

It is commonly accepted that In rich regions are of higher quality and that combined with localization these are the regions that dominate the radiative recombination processes. Regions with lower In concentrations would be transparent to the radiation produced by In rich regions providing that the bandtailing effects are not severe.[5] Active layers formed of dots can tolerate lattice mismatch. The idea is that the layer or layers of quantum dots will decouple the active layers to be studied from the substrate or buffer layer and, thus reduce number of extended and point defects. This application of QDs is novel. In addition to the important device applications, having truly high quality material without extended and point defects - since dots nucleate at extended defects and the dot density is much higher than the defect density - is important.

In the same vein is that proposed by Gérard et al[14] for reducing the degradation of internal quantum yield. These authors point out that once the carriers are captured by QDs, they become strongly localized and their migration toward nonradiative recombination centers is made difficult. Furthermore, the increased localization gives rise to increased radiative recombination rates. Growth of GaN self-assembled QDs on AlGaN, with the aid a sub- to monolayer Si layer, which are then covered by AlGaN has been reported by Tanaka et al., and Shen et al.[15,16] Other approaches have been reported by Widmann et al.[17,18] and Damilano et al.[19] who used AlN wetting layers which provide a larger lattice mismatch to GaN than AlGaN, and in turn provide the impetus for a 3-D growth. In addition, the surface topology of AlN is smoother which removes the surface features from being the nucleation sites for dots. Dots have been demonstrated on 6H-SiC[20,21] and sapphire (0001).[17,18] Blue-light emission has been reported from such QD structures.[18,] By changing the size of the quantum dots, one can in fact tune the color of the emission.[19]

Experimental

GaN dots discussed here were grown on either (111) Si substrates or c-plane sapphire substrates by reactive molecular beam epitaxy using ammonia as the nitrogen source. Si substrates underwent by now a standard RCA-like chemical etch, which involves several steps of oxidization followed by oxide removal. The last step before loading into the MBE system is a hydrogenation process

which attaches H to dangling bonds. Hydrogen desorbs rather easily in vacuum at temperatures above about 400 C. This combined with a short ammonia exposure at 850 C leads to a well defined (7x7) RHEED pattern indicative of a clean surface. Following a monolayer deposition of Al at a somewhat lower temperature, and nitridation of the Al layer, a nominally 0.3 μm thick AlN layer at 900 C followed by an AlGaN or a GaN layer was grown. This was then followed by the deposition of a sufficiently thick AlN layer that is presumed relaxed.

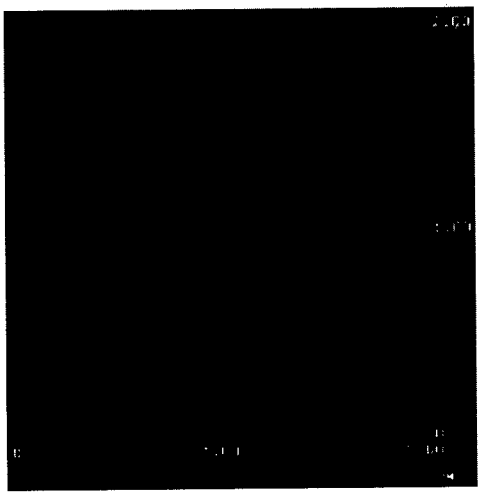

Fig. 1. AFM image of a c-plane sapphire prepared for smoothness. Atomically flat surface is clearly visible. Atomic step heights are about 0.15 nm, which represent the only roughness in the image. The diagonal lines from down-left to up-right are due the artifact of AFM.

Quantum dots were formed by growing a GaN layer having a thickness, which allows it to maintain its coherency with the AlN lattice in a fashion similar to that reported in reference 19. The ensuing short thermal annealing step causes the dots to form. The initial thickness and the length of the annealing cycle determine the particular size of the dots. In the case of sapphire substrates, the process is somewhat similar except that the substrate is prepared in a manner to lead to atomically smooth surfaces as shown in Fig. 1.

The rest of the growth particulars are similar to those on Si substrates. Since the purpose of the dots is to disconnect the strong tie between the buffer and dots, the choice of the substrate is not really that critical for optical quality which is what makes this approach attractive.

In the absence of a surface topology driven process, the dots nucleate at dislocations that propagate to the surface, i.e. the surface of AlN in the above examples. The key for quality is then to obtain a dot density that is substantially larger than the dislocation density. The goal then should be to reduce the dislocation density below 10^8 cm^{-2} and increase the dot density above 10^{11} cm^{-2}. This would simply mean that less than one out of every 1000 dots would contain extended defects. Fig. 2 shows an AFM image of a single layer high density GaN Qdots produced in our laboratory in a manner discussed above. Based on our work with quantum wells, we anticipate that size effects (blue shift) will dominate for dot sizes below about 2 monolayers, and polarization effects(red shift) above this size[22].

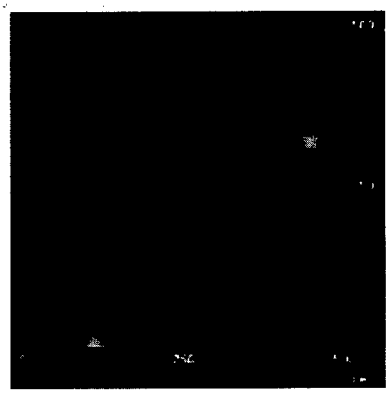

Fig. 2. AFM image of a single layer high density GaN Qdots produced in our laboratory. Note the high density of dots.

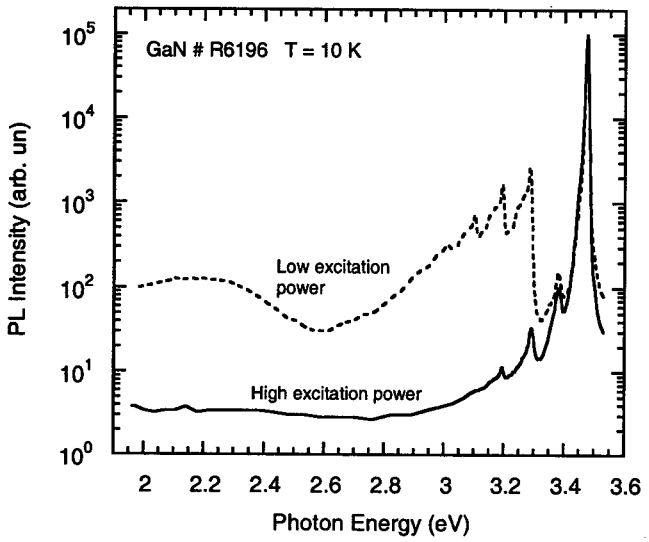

Fig. 3. PL spectrum from the GaN sample at 10 K for two excitation intensities. The emission lines near the band edge are due to the donor bound exciton and its phonon replicas. Some extrinsic processes are apparent in the low excitation case.

For reference purposes, shown in Fig. 3 is the PL spectrum from a 2 μm thick GaN layer on sapphire. Both the results from unfocussed low intensity (0.1 W cm^{-2}), and focused high intensity (100 W cm^{-2}) excitation conditions are displayed in a log scale. The lack of extrinsic transitions in the focussed beam case is noteworthy. However, the unfocussed case indicates the presence of some extrinsic transitions. The peaks near the band edge are the bound to donor exciton transition and its phonon replicas.

Preliminary experiments using the aforementioned dot formation method, but with manual control of the shutters during growth, have been very successful as evidenced by the photoluminescence data of Fig. 4.

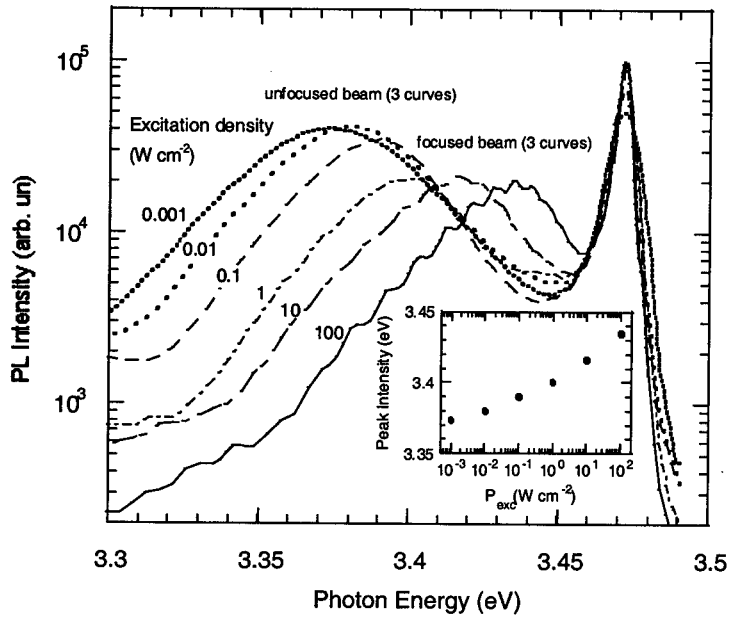

Fig. 4. Photoluminescence spectra at 10 K of a 30 layer stacked GaN QD as a function of excitation intensity. The 3.47 eV and lower energy transitions are due to the GaN buffer layer and GaN dots, respectively.

The PL data are from a stack of 30 dot layers. With manual shutter control, the reproducibility of the dot size from one dot layer to the next is not very good which is the case in runs on sapphire substrates in our case. The runs on Si substrates were performed in a different system with computer controlled shutters, which ensured identical deposition time for each layer of the quantum dot stack.

The cumulative PL data from two dot structures on Si and sapphire substrates are shown in Fig. 5. Owing to the automatic shutter control involving the sample on Si, the linewidth is narrower than that on sapphire. This is a mechanical problem and can be remedied. An interesting feature of these layers is their high quantum efficiency exceeding that for the bulk layers by a factor over 5. This is to be expected as the dot layers are of higher quality and carrier confinement favors radiative recombination.

In conclusion, quantum dot layers with as many as 30 vertical stacks have been grown with reactive molecular beam epitaxy on sapphire and Si substrates. PL measurements indicate the expected enhancement of the quantum efficiency as compared to the bulk layers. Single dot layers investigated by AFM indicate high dot concentration estimated to be much larger the extended defect concentration. The emission energy underwent varying degrees of red shift due to the dominance of the polarization effects.

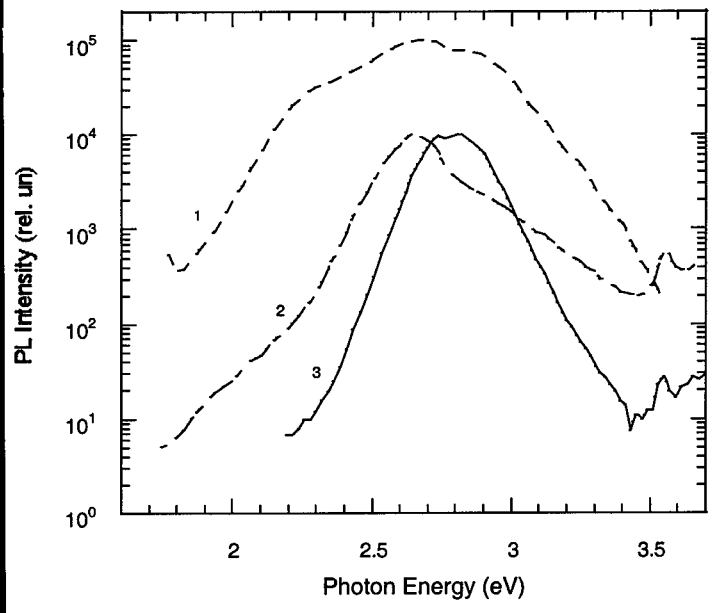

Fig. 5. PL of 30 stack Qdot samples on sapphire (1) and Si (2,3) substrates. The one on sapphire was with manual shutter control during growth, which is responsible for broadened emission. Excitation intensities are 0.1 W cm^{-2} for curves 1 and 2, and 100 W cm^{-2}.

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Achievement of MBE-Grown GaN Heteroepitaxial Layer with (0001) Ga-Polarity and Improved Quality by In Exposure

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Keywords: CAICISS, GaN, In Exposure, MBE, Polarity

Abstract We achieved the amazing improvements of the structural and electrical properties of GaN heteroepitaxial layers grown by molecular beam epitaxy on sapphire substrate. The improvements were carried out by the controlling of the lattice polarity due to exposure to a small amount of In flux during GaN epiaxial growth. The lattice polarities of GaN samples were confirmed by Coaxial Impact Collision Ion Scattering Spectroscopy (CAICISS) technique. By the structural and electrical evaluation of the GaN epitaxial samples, it is clarified that (0001) Ga-polarity GaN is superior compared with (000-1) N-polarity GaN. Hall measurement revealed that more than one order higher mobility of Ga-polarity layers compared with N-polarity layers. These results give the advances in the growth of high quality nitride films by MBE for device applications.

1. Introduction

GaN has been recently recognized as attractive materials for optoelectronic devices operating in the blue/UV region and electronic devices capable of operating under high power, high-frequency and high-temperature conditions. Until now, GaN crystals have been usually grown on sapphire and SiC substrates heteroepitaxially. GaN layers grown on non-polar substrates have two kinds of the lattice polarities, which are (0001) Ga-polarity and (000-1) N-polarity. It is well accepted that GaN films grown by metal-organic chemical vapor deposition (MOCVD) exhibit Ga-polarity. On the other hand, it is assumed that GaN epitaxial layers grown by conventional MBE show N-polarity, however the detailed occurrence of the polarities for MBE layers are not satisfactorily clarified. Smith *et al.*[1] investigated the correlation between the surface reconstruction structures after growth and the NaOH etching features for two kinds of MBE-grown layers on sapphire substrate; heteroepitaxial ones assumed to have N-polarity, and homoepitaxial ones on CVD-grown layers showing Ga-polarity. They insisted that Ga-polarity layers show (2×2) and (5×5) reconstruction patterns and the resistance for the etching. However, in regards to the polarity itself, no direct confirmations were indicated.

In this study, we achieved GaN epitaxial layers having Ga-polarity by In exposure during the MBE growth using radio-frequency (RF) nitrogen plasma. We clarified the correlation between the lattice polarity and surface reconstruction directly by using Coaxial Impact Collision Ion Scattering Spectroscopy (CAICISS), which can analyze the atomic arrangement of materials with high sensitivity owing to the focusing and shadowing effects for several keV ions. Moreover, we found out the better characteristics of Ga-polarity epitaxial layers in terms of X-ray diffraction (XRD) and electron mobility.

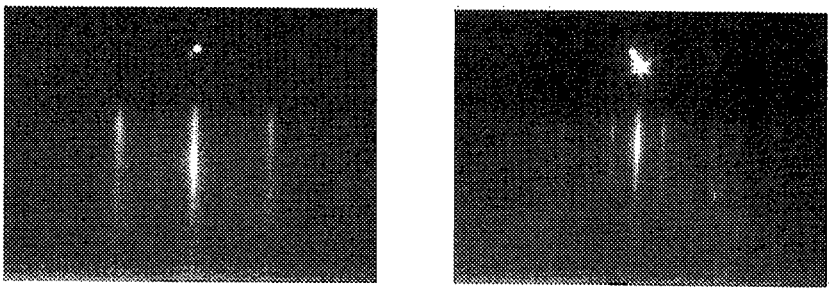
2. Experiment

GaN epitaxial layers were grown on sapphire substrates by RF-plasma assisted MBE. We fabricated two kinds of GaN heteroepitaxial layers. One is that with In exposure during epitaxial growth (denoted sample A), and the other is that without In exposure (denoted sample B). The

epitaxial layers were grown commonly at 700°C on low temperature GaN buffer layer grown at 300°C on nitrided sapphire substrate. Sample A was exposed to In flux for several seconds intermittently at 640°C only at the initial growth stage. The In flux intensity was 1.7×10^{-7} Torr, which is about 1/5 as low as the Ga flux intensity. Considering the In flux intensity and the growth temperature, the incorporation of In into the epilayers are negligible, and the formation of InGaN were observed by neither XRD nor PL in fact. Total thickness of each samples is 2.5 μm. Growing surfaces of epilayers were monitored by reflection high-energy electron diffraction (RHEED) in-situ. During growth, (1×1) RHEED patterns were observed both for samples A and B. We investigated the lattice polarities of the epitaxial layers by CAICISS technique. He^+ ion was employed as an incident beam, and the incident polar angle dependence was examined. In order to evaluate the structural and electrical properties of GaN samples, XRD and Hall effect measurements ware carried out, respectively.

3. Results and Discussion

Figure 1 shows the RHEED reconstruction patterns with decreasing the substrate temperature after growth. In Fig. 1, (2×2) patterns were observed for sample A, and (3×3) patterns were observed for sample B at 300°C. In addition, we investigated NaOH-etching properties of sample A and B as was done by Smith *et al.*[1] Although sample A was hardly etched by NaOH, sample B was etched with showing rough surface morphology. From these results, samples A and B are thought to correspond to the heteroepitaxial and homoepitaxial samples in Smith's report, respectively.



(a) Sample A with In exposure

(b) Sample B without In exposure

Fig. 1 RHEED reconstruction patterns after growth at 300°C

Figure 2 shows the polar angle dependence of Ga CAICISS signals for GaN layers showing (2×2) and (3×3) reconstruction, respectively. According to the simulation results, figure 2(a) exhibits the specific feature of Ga-polarity;[2] sharp single-peak at 18° and 40°. On the contrary, the specific features of N-polarity are seen in Fig. 2 (b), which are the wide double-peaks at 14° and 24°, intensity decreasing at 44° and intensity increasing at 50°. This CAICISS result clearly indicated that samples A and B have Ga-polarity and N-polarity, respectively. Thus, the correlation between the RHEED reconstruction, NaOH etching feature and the lattice polarity of GaN epitaxial layers were clearly established. The details of the mechanism of Ga-polarity occurrence with In exposure will be in the future publication.

Figure 3 shows the XRD rocking-curve profiles of sample A and B. XRD rocking-curve widths for sample A and B were 0.2461° and 0.4546°, respectively. XRD width of sample A is about half compared with that with sample B. Omega-2theta scan results showed narrow (0002) peaks as

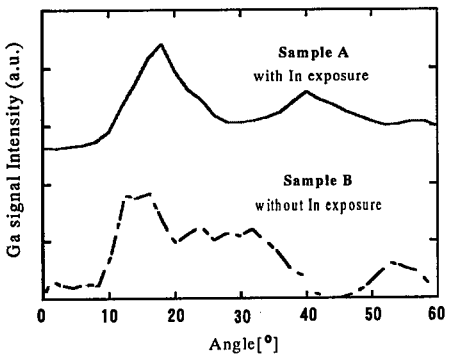


Fig. 2 Polar angle dependence of Ga CAICISS signal

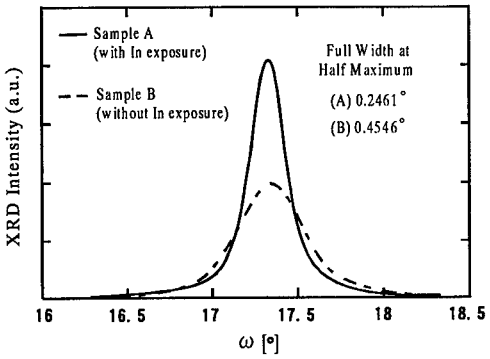
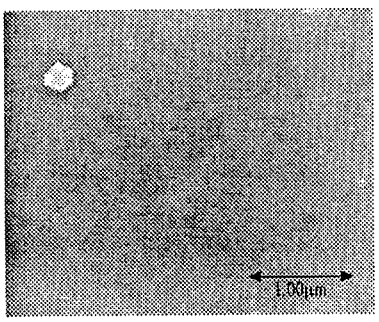
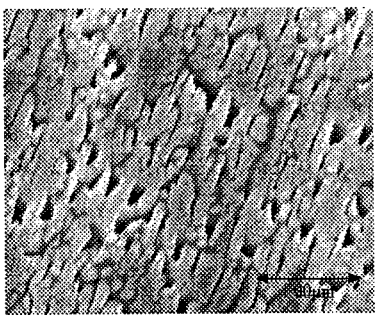


Fig. 3 XRD rocking-curve for (0002) diffraction

small as 60 arcsec in ω, and almost no significant difference was observed between the two samples. The flat and smooth surface of Ga-polarity layer was also confirmed by scanning electron microscope (SEM) observation. Figures 4 (a) and (b) show the SEM images of the two kinds of epitaxial layers after etching. As shown in Fig. 4(a), sample A has flat and smooth surface morphology. On the contrary, many grain boundaries exist on the surface of sample B as shown in Fig. 4(b). Hall effect measurements revealed more than one order higher mobility (275 cm^2/V s) of Ga-polarity layers compared with N-polarity layers. Much higher mobility can be expected by optimizing the growth condition. From the XRD results, the enlargement of grain saize is suggested, which means the reduction of grain boundaries. This consideration for structural properties can explain the mobility improvement, because grain boundaries may work as scattering centers for electrons. By the evaluations above, the quality of sample A, with In exposure, is superior to that of sample B. As reported by Shen et al.,[3] In-doping effect in epitaxial layers may be considered as one of the reasons of this improvement. However, in our study, a small amount of In flux is exposed to the samples only for a few minutes. Therefore, it is considered that the effect of In exposure is to control the lattice polarity for the growth. The structural and electrical qualities of GaN layers can be improved by the growth mode showing Ga-polarity in MBE.



(a) Sample A with In exposure



(b) Sample B without In exposure

Fig. 4 SEM images of the two kinds of epitaxial layers after etching

4. Conclusion

In conclusion, we clarified the correlation between the lattice polarity and surface reconstruction for hexagonal GaN epitaxial layers on sapphire directly by CACISS. We have found that the achievement of Ga-polarity much contributes to the improvements of the quality of MBE-grown samples. The Ga-polarity can be realized even in MBE growth by the exposure of a small amount of In flux.

The growth under Ga-polarity mode gives higher quality to GaN epilayers for device applications even in MBE.

Acknowledgement

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Crack-Free, Single-Crystal GaN Grown on 100 mm Diameter Silicon

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Keywords: Buffer Layers, Epitaxy, PL Spectra, TEM Images, Threading Dislocations, X-Ray Diffraction

Abstract

We have grown GaN epilayers, with a thickness of 1.3 to 1.4 μm, on 100 mm diameter Si(111) substrates. The GaN films were grown by using buffer layers consisting of 3C-SiC and 2H-AlN. The GaN films were flat and smooth without noticeable micro-cracks but had slip lines. The x-ray diffraction and electron diffraction analyses showed that each of the buffer layers and the GaN film were single-crystals. The room temperature PL showed that the FWHM was as low as 35.5 meV, the narrowest for all reported GaN/Si films grown by blanket MOCVD.

Introduction

GaN epilayers have been grown on 6H-SiC, sapphire, and silicon substrates. The GaN epilayers grown on 6H-SiC and sapphire have been utilized for fabricating short-wavelength optical emitting devices and high-frequency and high-power electronic devices. The growth of GaN on Si is highly desirable for the Si-based electronic industry since large diameter Si substrates are readily available and the GaN devices fabricated in a Si wafer fab will be low cost. The epitaxy of GaN on Si is considerably more difficult than that on 6H-SiC or sapphire substrates. This is due to the fact that the dominant polytype of GaN is a hexagonal (2H) structure while the Si substrate is diamond-cubic structure. In addition, GaN can hardly nucleate on a Si substrate since the silicon substrate can be quickly passivated by the nitrogen that is decomposed from a nitrogen-source gas such as ammonia needed for the GaN deposition. Conversely, the Si substrate surface can react rapidly with Ga to form Ga-Si alloys when a Ga-rich composition in the gas reactants is used for the GaN growth. Additional issue includes a high film stress resulting from mismatches in lattice parameters and differences in thermal expansion coefficients between the epilayers and the Si substrate. In this paper is we demonstrate the growth of 100 mm diameter GaN films by using AlN/3C-SiC as buffer layers on the Si(111) substrates to overcome some of the aforementioned issues.

Experimental Procedures

A modified Aixtron AIX200/4 CVD reactor was used for the epitaxy. A GaN film and buffer layers consisting of 3C-SiC and 2H-AlN were deposited in-situ on a 100 mm diameter Si(111) substrate. The deposition steps for a 3C-SiC buffer layer included carbonization and epitaxy. The carbonization was carried out by introducing propane at room temperature, rapidly heating up to 1100 °C, and then maintaining this temperature for 4 minutes. The carbonization step converts the Si surface to 3C-SiC by the reaction of Si with the carbon deposited from the propane. The epitaxy was then carried out at the same temperature by introducing trimethylsilane into the reactor. Approximately 0.2 μm of 3C-SiC was grown. This was followed by the growth of an AlN buffer layer using trimethylaluminum and NH_3 at 1140 °C. The thickness of the AlN buffer is approximately 0.1 μm. Finally, the GaN film was grown on top of the AlN using trimethylgallium and NH_3 at 1050 °C or 1020 °C. Thickness of the GaN films ranged from 1.3 to 1.4 μms.

Hydrogen was used as a carrying gas for the growth of all three layers. The pressure was kept constant at 100 mbar. Separately, we had obtained 3C-SiC buffer layers deposited on 1" diameter Si(111) substrates. The 3C-SiC buffer layers were deposited from the direct reaction of propane and silane (without the carbonization step). The 3C-SiC films prepared by this method were also single-crystal. To study if the GaN films would be affected by using the differently prepared 3C-SiC buffer layers, we made a consecutive growth of AlN (0.2 μm) and GaN (1.4 μm) films simultaneously on these substrates. The substrates made of direct deposited 3C-SiC included four different thickness (500Å, 1000Å, 2000Å and 3000Å). The substrate made from carbonization was prepared using the same procedure as described earlier.

Results

The grown films consisting of the GaN(1.4 μm)/AlN (0.1 μm) stack were severely cracked when they were deposited on the 3C-SiC buffer layers prepared by direct reaction. The degrees of the film crack seemed to be independent of the 3C-SiC layer thickness. However, the films were not cracked with a film thickness up to 1.4 μm when they were deposited on 3C-SiC formed via a carbonization step. Thus, the results presented in the followings are only for the GaN/AlN films deposited on such 3C-SiC.

The surfaces of the grown GaN films were fair specular and exhibited 7 to 10 concentric color fringes within 100 mm diameter. A few widely spaced slip lines were visible to the naked eye and with a microscope. Figure 1 is a photomicrograph that shows the "surface" feature of a 1.4 μm thick film. A high density of dark spots can be seen. They are likely resulting from voids underneath the 3C-SiC/Si interface. The voids are the characteristic defects resulting from the surface conversion of Si to 3C-SiC [1].

The SiC and AlN buffer layers prior to the GaN deposition were analyzed by X-ray diffraction (XRD) and were found to be single-crystal as shown in Figures 2 and 3 respectively. An in-situ deposited film stack consisting of GaN/AlN/3C-SiC was also analyzed by XRD and is shown in Figure 4. It shows that only (0002) and (0004) planes of GaN and AlN are present without any other plane in the diffraction pattern. This diffraction pattern shows that a <0001> axis of the GaN and AlN films is parallel to the [111] axis of the Si. The crystal perfection of the GaN films was analyzed by the x-ray double-crystal diffraction method. The full-widths at half-maximum (FWHM) of the GaN(0002) peak were in the range of 534 to 539 arc-sec. This is slightly better than 570 arc-seconds obtained from a 2.1 μm thick GaN film deposited on sapphire grown with the same reactor.

We have analyzed the in-plane (a- and b-axes) crystallographic relationships between the epilayers and the Si substrate by using selected area electron diffraction (SAED). Figure 5 shows a cross-sectional TEM image of the GaN/AlN/3C-SiC film stack for the analysis. The SAEDs were taken separately from a spot at Si, SiC, and the GaN/AlN interface. The SAED patterns showed that each buffer layer and GaN were single-crystals with sharp diffraction spots. Analyses of the electron diffraction patterns showed the crystallographic relationships between the hexagonal GaN or AlN and diamond-cubic 3C-SiC or Si as followings: GaN[0002]//AlN[0002]//3C-SiC[111]//Si[111] in the c-axis, and GaN[1-100]//AlN[1-100]//3C-SiC[211]//Si[211] in the a-axis. From the stereographic projections of a Si(111) and a hexagonal (0002) it can be visualized that the aforementioned a-axis relationship is equivalent to GaN[11-20]//AlN[11-20]//3C-SiC[01-1]//Si[01-1].

We have investigated the crystallographic defects and microstructure of the buffer layers using the TEM. The results showed that the 3C-SiC and AlN films were crystallographically well aligned. A high magnification TEM image confirms the absence of a grain structure in both layers. The interfaces between the 3C-SiC and AlN, as well as the top surface of AlN, are fairly flat and smooth. The predominant defects in these two layers were threading dislocations. The dislocations are also the predominant defects in the GaN layers. Figure 5 shows that the threading dislocations are propagating vertically from the GaN/AlN interface to the top surface. The threading dislocation densities were found to be in the range of $3x10^{10}/cm^2$ to $9x10^{10}/cm^2$.

The depth profiles of the Ga, Al, Si and C concentrations were analyzed by secondary ion mass spectrometer (SIMS). We have found that the thickness of the GaN layer varied as high as 40%

within the wafers when we had a poor epitaxial layer spot at the center of the wafer. The abruptness of the GaN/AlN interface was also varied with the measurement locations in the wafers. Extended inter-diffusions of Al and Ga across the GaN/AlN were seen at the poor epitaxial layer spot.

The photoluminescence (PL) spectra were taken at room temperature (RT). The FWHMs of the band edge emission measured at RT were in the range of 35.5 to 40.5 meV. Figure 6 shows the room temperature PL spectrum taken from a 1.4 μm GaN film grown on Si(111) and shows FWHM of 35.5 meV. This spectrum also shows very low intensity of yellow emission at 2.17 eV.

Discussion and summary

The success for growing a highly lattice mismatched epilayer, such as GaN on Si, seems to depend on selection of a suitable buffer layer or buffer layers. We chose 3C-SiC as a first buffer layer for separating the Si surface from reaction with Ga and nitrogen. The lattice constant of 3C-SiC(02-2) is 1.54Å and is not far apart from the lattice constants of 1.59Å for GaN(11-20) and 1.56Å for AlN(11-20). Thus, the epitaxy of GaN(11-20) and AlN(11-20) should be easier on 3C-SiC(02-2), than on Si(02-2) that has a lattice constant of 1.92 Å.

Two different methods were used for growing 3C-SiC on Si. The GaN/AlN films deposited on the 3C-SiC with carbonization had few micro-cracks. This is likely due to the fact that a 3C-SiC film produced by carbonization always contains voids on the top of the Si substrate. The voids may facilitate the Si top surface to act as a compliant layer to alleviate the film stresses resulting from mismatches in thermal expansion coefficients and lattice mismatches between the films and substrate.

The GaN film quality evaluated by photoluminescence showed that the FWHMs of the band edge emission measured at room temperature were in the range of 35.5 to 40.5 meV. The earlier reported lowest FWHM was 62.5 meV [2]. Other reported values were 90 meV [3], 100-150 meV [4], and 74 meV [5]. The low FWHM values in our films may likely attribute to the high-degree of crystallographic alignment of the buffer layers and to layers without a gain structure.

The high spatial variations of the GaN layer thickness and the diffused GaN/AlN interfaces at some regions of the films could be the results of substrate temperature non-uniformity and a non-optimized growth process. A non-even surface roughness of the films could also contribute to the measurement uncertainty of depth profiles by SIMS.

Conclusion

We have grown single-crystal, GaN films on 100 mm diameter Si(111) substrates using AlN/3C-SiC as buffer layers. A key step in growing crack-free films seems to rely on how the 3C-SiC buffers layer were prepared. The 3C-SiC prepared by carbonization resulted in better GaN films than that without the carbonization step. To our knowledge the films grown by this work showed the narrowest FWHM PLs for reported GaN grown on Si by blanket MOCVD.

Acknowledgements

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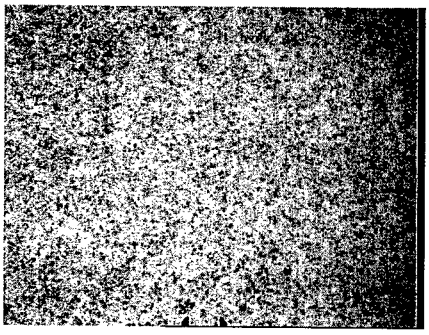

Fig. 1. A photomicrograph of a 1.4 μm thick GaN film (the scale=30 μm).

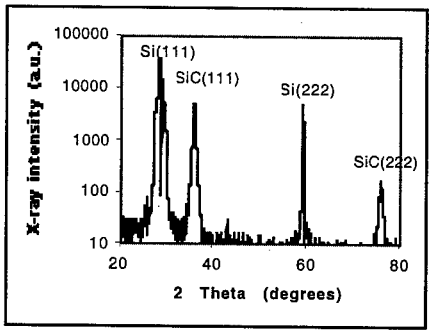

Fig.2. X-ray diffraction of a 3C-SiC buffer layer.

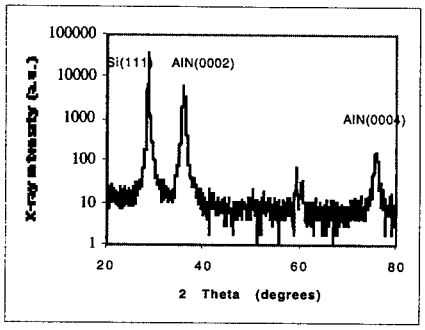

Fig.3. X-ray diffraction of an AlN buffer layer.

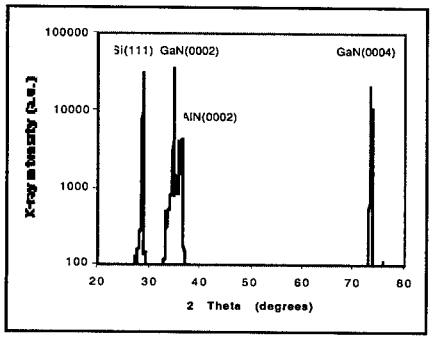

Fig.4. X-ray diffraction of a GaN/AlN/SiC film stack.

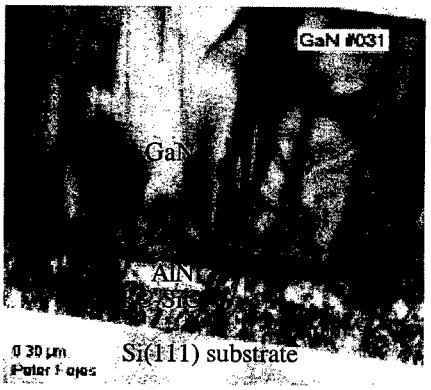

Fig. 5. A cross-sectional TEM of a GaN film deposited on AlN/3C-SiC/Si.

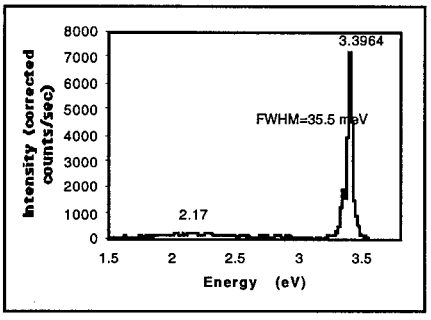

Fig. 6. A PL spectrum taken at room temperature for a 1.4 μm thick GaN on Si(111).

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3C-SiC Pseudosubstrates for the Growth of Cubic GaN

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Keywords: AFM, FTIR, Raman, RHEED, SOI

Abstract : We report on the successful growth of 3C-SiC/Si and 3C-SiC/SOI heterostructures for the growth of cubic GaN films. Raman results provided moreover direct evidence of the compliant character of the SOI substrate. We show that the GaN surface roughness depends drastically both on the starting SiC surface and its structural quality. Rheed oscillations patterns of β-GaN grown on thick 3C-SiC epilayers with smooth surfaces were observed.

1. Introduction

GaN, AlN and related alloys are ideal materials for applications to UV/blue emitters and high temperatures, high-power electronics devices [1]. Due to the lack of high quality GaN bulk substrates, the growth of this material is carried out by heteroepitaxy. Zinc blende GaN is very attractive from a practical point of view, though it is know to be metastable phase and therefore, it is extremely sensitive to the growth parameters. Many attempts with different substrates have been made in order to obtain good quality β-GaN epilayers. If one considers Si and SiC materials, the most common cubic substrate, SiC seems to be the more suitable due to the relatively low lattice mismatch (3.5%) and the small thermal expansion coefficient difference between β-GaN and β-SiC. Besides, it has been reported that the use of SOI substrates improve the quality of 3C-SiC epilayer [2]. In this work, we report on the structural and morphological characterizations of β-GaN and β-SiC films in the β-GaN/SiC/Si and β-GaN/SiC/SOI heterostructures. The morphologies of 3C-SiC/Si and 3C-SiC/SOI pseudosubstrates were characterized by Nomarski optical microscopy and atomic force microscopy (AFM). Raman and IR spectroscopies were carried out in order to compare the quality of 3C-SiC films grown on SOI substrates and on Si substrates and to characterize GaN films.

2. Results and discussion

2.1 Growth and characterization of 3C-SiC fims on Si and SOI substrates

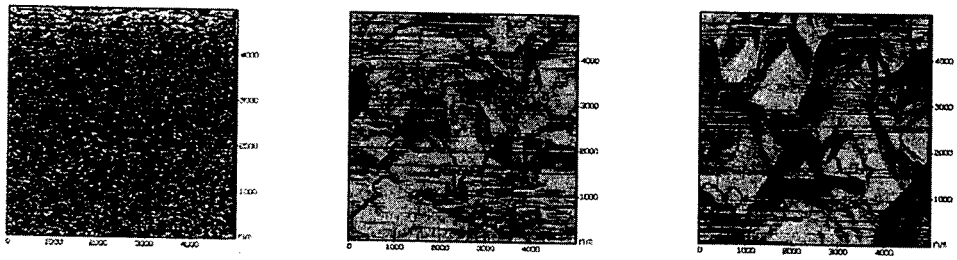
3C-SiC films were heteroepitaxially grown on Si(100) and on UNIBOND® SOI (Silicon-On-Insulator) substrates (SOL: 205 nm / BOX: 200 nm), by atmospheric pressure CVD. A vertical reactor with a 70 mm inside diameter was used. The substrates were placed on a rf heated graphite susceptor. The growth process involved three steps as follows: the samples were heated at 1000°C in a H_2 ambient during 5 minutes, for in situ cleaning. Then Si (or SOI) substrates were carbonized at 1150°C for 10 min under 10 sccm of C_3H_8 and 10 slm of H_2. Finally, CVD growth of SiC was carried out at 1350°C using 0.8 sccm of SiH_4, and 0.9 sccm of C_3H_8 and 10

slm of H_2. Three series of 3C-SiC epilayers were prepared resulting in 1-2 nm-, 1μm- and 3 μm-thick 3C-SiC films (resp. A, B and C samples). The growth conditions for all samples are summarized in Table 1.

	Thickness	Growth conditions
A samples	1-2 nm	- Si (or SOI) carbonization
B samples	1 μm	- Si (or SOI) carbonization - CVD growth for 20 min
C samples	3 μm	- Si (or SOI) carbonization-CVD growth for 1 hour

Table 1. Growth parameters for A, B and C 3C-SiC/Si (or SOI) pseudosubstrates

Figure 1 shows AFM images of A, B and C samples for a 5000 x 5000 nm scan. A samples presented a very good surface morphology characterized by an AFM surface roughness (root mean square or RMS) of 0.25 nm. No surface defects have been found on these films. For B samples (resp. C samples), the surface roughness was typically about 2.8 nm (resp. 3,2 nm).



(a) (b) (c)

Fig. 1. AFM images of (a) A sample, (b) B samples and (c) C samples. (scan 5000 x 5000 nm^2)

X-ray diffraction made on B and C samples indicated a good cristallinity of the 3C-SiC films for both samples. The full weight half maximum (FWHM) of the SiC(200) 2θ peak was 195 arcsec for B samples and 135 arcsec for C samples.

FTIR reflectance spectroscopy was performed at room temperature before and after growth of the GaN films on type C samples deposited either on Si(100) wafers or on SOI (100) substrates. The spectra showed no contribution of free carriers, indicating that the residual effective doping level was well below 10^{17} cm^{-3} in both the nominally undoped 3C-SiC and β-GaN layers. This upper limit was confirmed by Raman backscattering spectra excited with the 514.5 nm (2.41 eV) line of an Ar^+ laser under the microscope of a DILOR apparatus. Raman results provided moreover direct evidence of the compliant character of the SOI substrate : as shown in fig. 2, for two 3C-SiC samples (type C) deposited in the same batch on different substrates, the 3C-SiC film grown on Si(100) yielded the zone-center TO phonon peak near 796 cm^{-1} [3] at a higher frequency (ie was under a stronger compressive stress) than the 3C-SiC layer grown on the sacrificial (100) silicon overlayer of the SOI pseudosubstrate. We attribute this residual stress to the fact that the thermal expansion coefficient of Si is higher than that of 3C-SiC. As expected from such thermoelastic considerations, a much weaker shift in the opposite direction was observed in fig. 2 between the TO phonon frequencies (near 520 cm^{-1}) of the two types of silicon substrates. The spectra of this figure confirmed that in the case of SOI a significant mechanical decoupling between the Si substrate and the thin silicon overlayer subsisted after growth at high temperatures of a crystal with a lower lattice expansion coefficient.

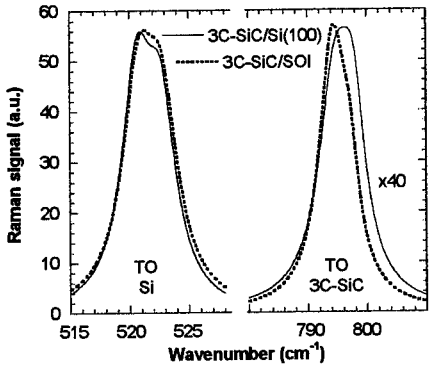


Fig.2. Raman spectra in the TO mode region of Si (left) and SiC (right) of 3μm-thick 3C-SiC samples depositedin the same batch (# 184) on silicon or silicon-on-insulator.

2.2 Growth and characterization of GaN/SiC/Si and GaN/SiC/SOI films

The growth of β-GaN, AlN and alloys was carried out by Molecular Beam Epitaxy (MBE) on A, B and C samples, at temperatures in the range of 600-700 °C. After standard preparation (i.e. degreasing in trichloroethylene, acetone and methanol, and etching in HF), the 3C-SiC/Si pseudosubstrates were introduced into the UHV chamber. Systematically, outgassing was carried out at 750 °C. Under such conditions, the SiC surface was reconstructed (5x1). Before deposition of the nitride films, a 0.5-μm GaN undoped buffer layer was deposited at 700 °C and at low growth rate of ~ 0.3 monolayers (ML)/s. A 2D-growth mode was observed soon after the deposition of the buffer film. On A substrates, only polycrystalline GaN is obtained. For B substrates, 3D GaN spots are superimposed on the streaky RHEED pattern after deposition of 300 ML of GaN (see Fig.3a). By contrast on C substrates, only a streaky RHEED pattern was obtained (see Fig.3b) and RHEED intensity oscillations along the [110] azimuth (see inset in Fig.3b) for β-GaN and its ternary alloys with Al could be obtained.

(a) (b)

Fig.3. RHEED pattern of β-GaN surface take during the growth of GaN layers on SiC substrates of 1 μm (a) and 3 μm (b).

It allowed us to determine the growth conditions as a function of Ga cell temperature, and N flux. Two regimes clearly appear: in the first one, corresponding to the low Ga temperature range, one observes an increase of the growth rate proportional to the Ga flux. Then, this regime corresponds to Ga-limited, N-rich growth. Note however that in this regime, the GaN growth front is rough and tends to form facets. In such a case inclusions of hexagonal phase were found in the layers by Raman spectroscopy. In contrast, for higher Ga temperatures, the GaN growth rate is constant whatever the Ga flux, indicating that the growth occurs under N-limited Ga rich conditions. In this regime one observes a 2D-growth mode, but a Ga excess eventually leads to the formation of Ga droplets. Therefore the stoichiometry conditions have to be carefully adjusted to optimize the structural quality of the layers. Raman spectroscopy was performed on GaN/SiC/Si and GaN/SiC/SOI films. After substraction of the intense TO peak associated to the silicon substrate, a careful analysis of the resulting spectra enabled us also to compare the phase purity and structural quality of such β-GaN

and 3C-SiC (type C) films. Fig 4 shows that close to the 552 cm^{-1} peak of the TO phonon of β-GaN, layers grown on thick SiC films deposited on SOI substrates yielded a secondary Raman peak around 567 cm^{-1} attributed to the E_2 mode of a parasitic hexagonal α-GaN phase, in contrast to the weak shoulder which appeared for the classical GaN/SiC/Si structure. According to previous estimates [4], the spectra shown in fig 5 correspond to local hexagonal phase volume fractions of 0.15 % (resp 0.5 %) in the case of the SOI substrate (resp Si(100) wafer), and the frequency of the TO peak was lower in films containing a lower hexagonal volume fraction [4]. The occurrence of the unwanted hexagonal phase in the epitaxial GaN samples was not in our experience systematically correlated to that of hexagonal polytypes in the 3C-SiC underlayer, as indicated by specific [3] example of such disordered 6H polytypism can be seen in the Raman spectra of fig. 5 for the film grown on a SOI pseudosubstrate. It is not clear at present that the poorer structural quality of such films will hinder their application to β-GaN/3C-SiC devices, in view of the reasonable quality of the active β-GaN epitaxial layer and of the advantages of a compliant substrate for many applications.

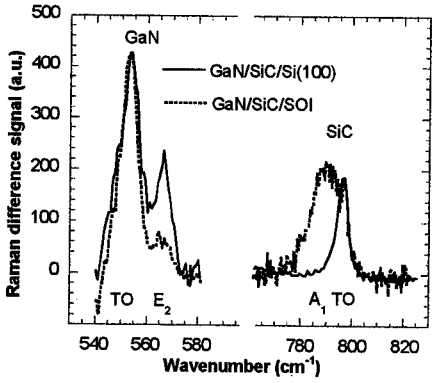


Fig.4 Micro-Raman spectra of GaN/3C-SiC structures deposited on silicon or on silicon-on-insulator substrates.

3. Conclusion

3C-SiC films grown Si and SOI substrates were used as pseudosubstrates for the growth of cubic GaN. Raman results show a lower stress of SiC films grown on SOI substrates to compare to Si substrates indicating a compliant effect of SOI structure. The RHEED patterns along the [110] azimuth obtained from GaN grown on thick SiC substrates indicate a 2D growth mode of single crystalline β-GaN films.

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Lateral- and Pendeo-Epitaxial Growth and Defect Reduction in GaN Thin Films

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Keywords: Inductively Coupled Etching, Lateral Epitaxial Overgrowth, LEO, MOVPE, Pendeo-Epitaxy, Scanning Electron Microscopy, Silicon Nitride Mask, Thin Film Morphology

Abstract

Monocrystalline discrete and coalesced films of lateral- and pendeo-epitaxial GaN layers originating from stripes deposited within windows contained in SiO_2 masks or from side walls of seed structures topped with silicon nitride masks have been grown via organometallic vapor phase deposition using on-axis GaN/AlN/6H-SiC(0001) substrates. Scanning and transmission electron microscopies and atomic force microscopy revealed (1) coalescence of the laterally growing layers, (2) a low density of dislocations in the overgrown regions, and (3) an RMS roughness of the $(11\bar{2}0)$ sidewall plane of the pendeo-epitaxial structures of approximately 0.100 nm.

Introduction

It has been a necessity for investigators in the III-nitride community to grow films of GaN and related nitride materials using heteroepitaxial growth routes because of the dearth of bulk substrates of these materials. This results in films containing dislocation densities of 10^8-10^{10} cm^{-2} because of the mismatches in both the lattice parameters and the coefficients of thermal expansion between the buffer layer and the film and/or the buffer layer and the substrate. These high concentrations of dislocations may also limit the performance of devices.

Several groups [see e.g., Refs. 1-9], including the present authors, have conducted research regarding selective area growth (SAG) and lateral epitaxial overgrowth (LEO) techniques for GaN deposition, specifically to reduce significantly the dislocation density. Increased emphasis in this research topic was fueled in part by the announcement by Nakamura, et al. [10-12] of the dramatic increase in projected lifetime of their GaN- based blue light-emitting laser diodes fabricated on LEO material. Using these approaches, researchers have been able to grow GaN films containing dislocation densities of $\approx 10^5$ cm^{-2} in the areas of overgrowth. However, to benefit from this reduction in defects, the placement of devices incorporating LEO technology is limited and confined to regions on the final GaN device layer that are located on the overgrown regions.

Recently we have pioneered a new approach to selective epitaxy of GaN layers, namely, pendeo- (from the Latin: to *hang* or be *suspended*) epitaxy (PE) [13-18] as a promising new process route for growth of a single, continuous, large area layer or a discrete platform of this material. This technique incorporates mechanisms of growth exploited by the conventional LEO process by using an amorphous mask to prevent vertical propagation of threading dislocations; however, it extends beyond the conventional LEO approach to employ the substrate itself as a *pseudo-mask*. This unconventional approach differs from LEO in that growth does not initiate through open windows on the (0001) surface of the GaN seed layer; instead, it is forced to selectively begin on the sidewalls of a tailored microstructure comprised of forms previously etched into this seed layer. Continuation of the pendeo-epitaxial growth of a GaN layer until coalescence over and between these forms results in a complete layer of low defect-density material.

The following sections describe the experimental parameters necessary to achieve GaN films via LEO and PE. The microstructural evidence obtained for the resulting films is also described, discussed and summarized.

Experimental Procedures

The LEO of GaN(0001) films has been achieved via metallorganic vapor phase epitaxial (MOVPE) deposition on an underlying 1 μm thick GaN seed layer previously deposited on a 100 nm thick AlN buffer layer/6H-SiC(0001) substrate heterostructure. The GaN seed layer was exposed through windows etched in an overlying, 100 nm thick SiO_2 mask deposited using low pressure chemical vapor deposition at 410°C. The etched mask contained 3μm and 5μm wide striped openings, spaced parallel at distances ranging from 3 to 40μm. The patterned samples were dipped in a 50% buffered HCl solution to remove surface contamination. The lateral overgrowth was achieved at 1000 -1100°C and 45 Torr. The deposited GaN grew vertically to the top of the mask and then both laterally over the mask and vertically until the lateral growth fronts from many different windows coalesced and formed a continuous layer. Additional details of the growth experiments are presented in Refs. [7, 8, and 19].

Each pendeo-epitaxial GaN film was deposited using the same equipment, essentially the same growth parameters and a similar initial GaN/AlN/6H-SiC(0001) heterostructure as employed in the LEO studies. However, as noted in the Introduction and as described below, the etched microstructure used in the PE technique is essentially the inverse of that employed in the LEO technique. A 100 nm silicon nitride growth mask was deposited on each GaN seed layer via plasma enhanced chemical vapor deposition. A 150 nm nickel etch mask was subsequently deposited using e-beam evaporation. Patterning of the nickel mask layer was achieved using standard photolithography techniques followed by dipping in HNO_3 for approximately five minutes. The samples were subsequently cleaned by consecutive dips in trichloroethylene, acetone, methanol, and HCl for five minutes each and blown dry with nitrogen. The seed-forms used in this study were raised rectangular stripes oriented along the $<1\bar{1}00>$ direction. This provided a parallel sequence of GaN sidewalls with nominally $(11\bar{2}0)$ faces. This microstructure was fabricated via removal of portions of the nickel etch mask via sputtering and by inductively coupled plasma (ICP) etching of portions of the silicon nitride growth mask, the GaN seed layer, the AlN buffer layer and the near-surface regions of the 6H-SiC substrate. This resulted in the removal of all III- nitride material from the areas between the sidewalls of the forms. This step was critical to the success of the PE growth. Seed form widths of 2 and 3 μms coupled with separation distances of 3 and 7 μms, respectively, were employed. The remaining nickel mask protecting the seed structures during the ICP etching process was removed using HNO_3. Immediately prior to pendeo-epitaxial growth, the patterned samples were dipped in a 50% HCl solution to remove the surface contaminants from the walls of the underlying GaN seed structures.

Results and Discussion

Continuous 5 μm thick GaN layers were obtained via LEO, as shown in Figure 1. Atomic force microscopy revealed an RMS roughness of the surfaces of the pit-free overgrown layers of 0.25 nm which is similar to the RMS roughness values obtained for the underlying GaN films. Each black spot in the overgrown GaN layer shown in Figure 1 (a) is a void that forms when two growth fronts coalesce.

A cross-sectional TEM micrograph showing a typical laterally overgrown GaN layer is presented in Figure 2. Threading dislocations, originating from the GaN/AlN buffer layer interface, propagate to the top surface of the regrown GaN layer within the window regions of the mask. By contrast, there were no observable threading dislocations in the overgrown layer. A few dislocations formed parallel to the (0001) plane via the extension of the vertical threading dislocations after a 90° bend in the regrown region. These dislocations did not subsequently propagate to the surface.

The pendeo-epitaxial phenomenon is made possible by taking advantage of growth mechanisms identified by Zheleva et.al. [13] in the conventional LEO technique, and by using two additional key steps, namely, the initiation of growth from a GaN face other than the (0001) and the

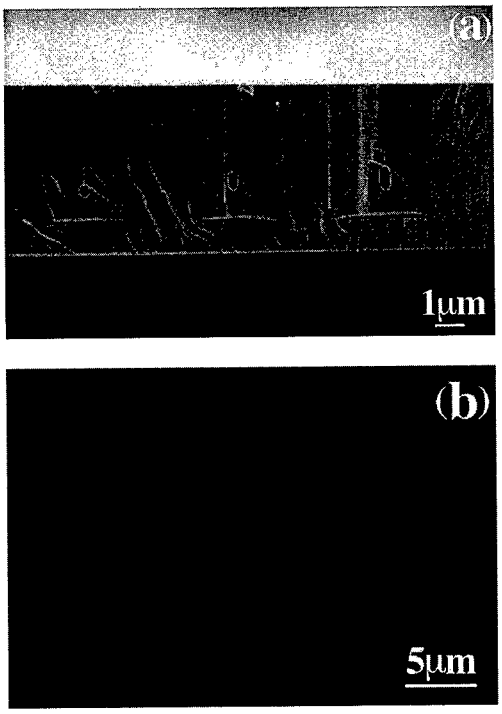

Figure 1. (a) Cross-section and (b) surface SEM micrographs of the coalesced GaN layer grown on 3 μm wide and 3 μm spaced stripe openings oriented along <1$\bar{1}$00>.

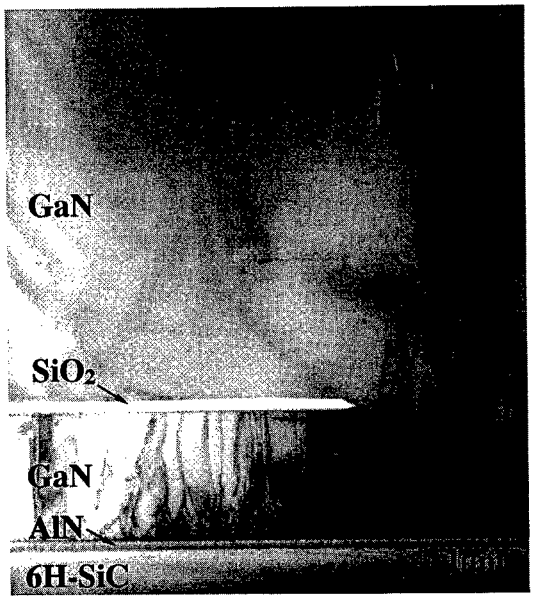

Figure 2. Cross-section TEM micrograph of a laterally overgrown GaN layer on a SiO_2 mask.

use of the 6H-SiC substrate as a mask. By capping the seed-forms with a growth mask, as shown schematically in Figure 3a, the GaN was forced to grow initially and selectively only on the GaN sidewalls. Common to conventional LEO, no growth occurred on the silicon nitride mask covering the seed forms. Deposition also did not occur on the exposed SiC surface areas at the higher growth temperatures employed to enhance lateral growth. The Ga- and N-containing species more likely either diffused along the surface or evaporated (rather than having sufficient time to form GaN nuclei) from both the silicon nitride mask and the silicon carbide substrate. The pronounced effect of this is shown in Figure 3b wherein the newly deposited GaN has grown truly suspended from the sidewalls of the GaN seed structure. Vertical growth of GaN occurred from the advancing (0001) face of the laterally growing GaN.

Extension of the vertical growth to a height greater than the silicon nitride mask allowed conventional LEO-type growth and eventual coalescence over the silicon nitride mask covering the seed structure, as shown in Figure. 4. A cross-sectional TEM micrograph showing a typical PE growth structure is shown in Figure 5. Threading dislocations extending into the GaN seed structure and originating from the GaN/AlN and AlN/SiC interfaces are clearly visible.

The silicon nitride mask acted as a barrier to the further vertical propagation of these defects into the laterally overgrown PE film. Since the newly deposited GaN is suspended above the SiC substrate, there are no defects associated with the mismatches in lattice parameters between GaN and AlN and between AlN and SiC. Analysis of the GaN seed/GaN PE interface revealed evidence of threading dislocations or stacking faults within the (0001) planes. As in the case of LEO, there is a significant reduction in the defect density in the regrown areas.

The continuation of the PE growth results in coalescence with adjacent growth fronts and the formation of a continuous layer of GaN with a smooth surface, as observed in Figure 6. This also results in the practical elimination of all dislocations stemming from the heteroepitaxial growth of GaN/AlN on SiC. Clearly visible in Figure 6(a) are the voids that form when adjacent growth fronts coalesce. Optimization of the PE growth technique should eliminate these undesirable defects.

Summary

Continuous GaN films having very low dislocation densities have been achieved via lateral epitaxial growth and coalescence of GaN homoepitaxial stripes over SiO_2 masks. Pendeo-epitaxy has been developed as an alternative and more universal and simple approach of growing uniformly low-defect density thin films over the entire surface of a substrate. In particular, we have demonstrated the growth of both discrete structures and coalesced GaN films using PE on etched GaN seed layers previously grown on AlN/6H-SiC substrates.

Acknowledgements

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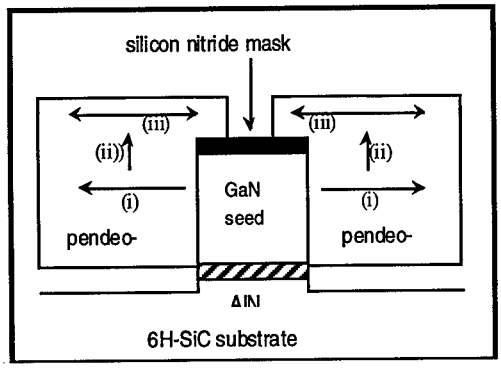

Figure 3a. Schematic of pendeo-epitaxial growth from GaN sidewalls and over a silicon nitride mask.

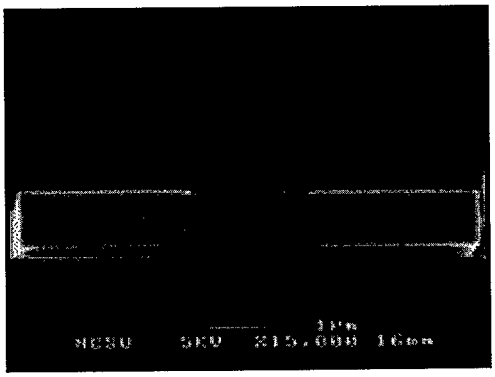

Figure 3b. Cross-sectional SEM of a GaN pendeo-epitaxial growth structure with limited vertical growth from the seed sidewalls and no growth on the seed mask.

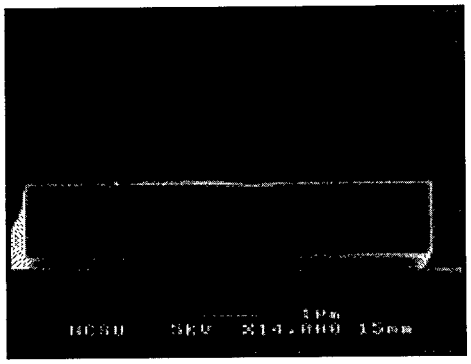

Figure 4. Cross-sectional SEM of a GaN/AlGaN pendeo-epitaxial growth structure showing coalescence over the seed mask.

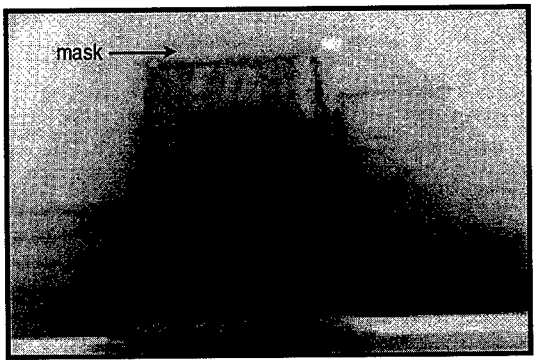

Figure 5. Cross-sectional TEM of a GaN pendeo-epitaxial structure showing confinement of threading dislocation under the seed mask, and a reduction of defects in the regrown areas.

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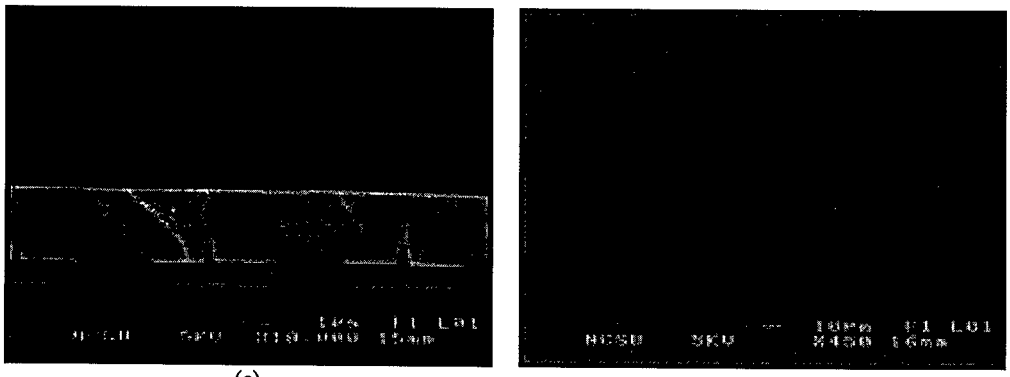

(a) (b)

Figure 6. Micrographs taken via (a) cross-sectional SEM and (b) plan-view SEM of pendeo-epitaxial growth of a GaN layer with coalescence over and between the seed forms.

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Pendeoepitaxy of GaN and InGaN LEDs on SiC

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Keywords: Epitaxy, Gallium Nitride, LEDs, Silicon Carbide

Abstract

Pendeoepitaxy of GaN on GaN grown on 6H-SiC (0001) substrates with a conductive buffer layer has been studied. Transmission electron microscopy (TEM) revealed a significant reduction in dislocations in PE epilayers. Some dislocations, which are parallel to (0001) plane, were observed in PE epilayers. Scanning electron microscopy (SEM) and atomic force microscopy (AFM) were also utilized to characterize the PE epilayers. InGaN quantum well LEDs have been fabricated with different indium compositions that emit from 450 to 625 nm.

Introduction

Gallium nitride films grown on sapphire or SiC substrates contain a high density of dislocations (10^8 - 10^{10}/cm^2) due to the lattice mismatches between epilayers and substrates. To reduce the dislocation density in the GaN epilayers, many researchers have studied lateral epitaxial overgrowth (LEO) [1-4] and Pendeoepitaxy (PE) [5-7]. Both methods have been proven very effective to reduce dislocation density in GaN epilayers. In this research, we studied Pendeoepitaxy of GaN on GaN grown on 6H-SiC (0001) substrates with a conductive buffer layer. Transmission electron microscopy (TEM) revealed a significant reduction in dislocations in PE epilayers. Some dislocations, which are parallel to (0001) plane, were observed in PE epilayers. Scanning electron microscopy (SEM) and atomic force microscopy (AFM) were also utilized to characterize the PE epilayers.

Experiment

Both Pendeo GaN layers and underlying GaN seed layers were grown in a MOCVD system. GaN seed layers were grown on n-type 6H-SiC (0001) substrates with a conductive buffer layer. Total thickness of the seed layers is about 1.3 μm. Photoresist was used as a mask for etching GaN seed layers to form 5, 10 μm wide GaN stripe patterns oriented along $<1\bar{1}00>$ and $<11\bar{2}0>$ directions. Etching was extended into the SiC substrate to ensure removal of all of the GaN and conductive buffer layer. The space between two parallel GaN stripes was from 3 to 25 μm. After removing photoresist, the wafers with GaN seed stripes were loaded into MOCVD

reactor for Pendeo growth. The growth of GaN starts from the top and side walls of the GaN stripe as shown schematically in Figure 1. SEM (JEOL 6100) was used to study the dependence of Pendeo lateral growth rate and facets on the sidewalls on the growth temperature and stripe orientations. TEM (TOPCON 002B, 200 kV) and AFM (Digital Instrument Nano-Scope) were also utilized to characterize defect structure and surface morphology of the Pendeo epilayers.

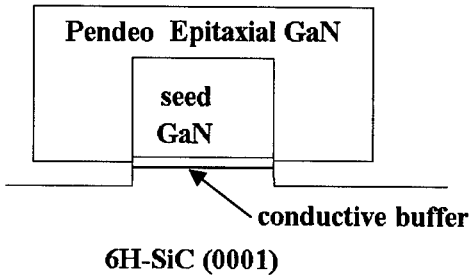
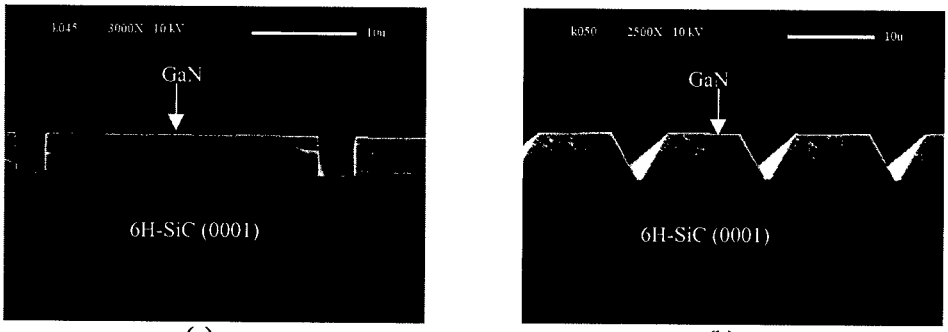


Figure 1. Schematic diagram of Pendeoepitaxy.

Results and Discussion

The cross-sectional SEM images in Figure 2a and 2b show the dependence of Pendeoepitaxy on stripe orientation. This PE sample was grown at 1080 °C. Fast lateral growth (5.8 μm/hr) was obtained on the <$1\bar{1}00$> GaN stripe (Fig. 2a). This PE GaN is suspended from the SiC substrate with (0001) top facet and ($11\bar{2}0$) side facets. The gap between the SiC substrate and PE GaN is in the range of a few hundreds to a few thousands angstroms. No deposits were found on the exposed SiC area. In contrast, very little lateral growth was observed on the <$11\bar{2}0$> GaN stripe (Fig. 2b). In this case, the (0001) facet is on top and ($1\bar{1}01$) facets on both



(a) (b)

Figure 2. Cross-sectional SEM images of (a) PE GaN on a <$1\bar{1}00$> GaN stripe; (b) PE GaN on a <$11\bar{2}0$> GaN stripe.

sides. When growth temperature was decreased to 1035 °C, $(11\bar{2}2)$ side facets were observed on $<1\bar{1}00>$ stripes as shown in Figure 3. The vertical and lateral growth rates at the growth temperatures of 1080 °C and 1035 °C are summarized in Table 1.

Table 1. Dependence of PE growth rates* on growth temperature

Growth Temperature	Vertical G. R.**	Lateral G. R.	Ratio (L.G.R/V.G.R)***
degree C	μm/hr	μm/hr	
1035	3.1	3.7	1.2
1080	1.6	5.8	3.6

* Stripe orientation: $<1\bar{1}00>$; GaN stripe width: 7 μm; SiC open window: 25 μm.
** G.R.: growth rate; *** L.G.R.: lateral growth rate; V.G.R.: vertical growth rate.

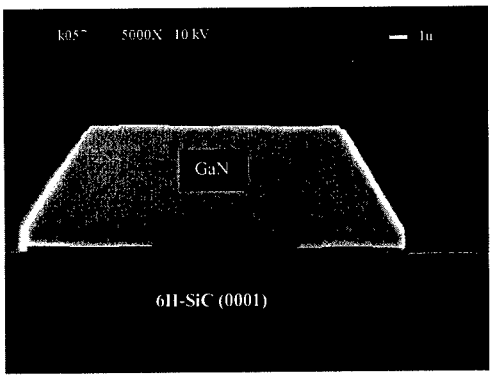


Figure 3. Cross-sectional SEM image of PE GaN on a $<1\bar{1}00>$ GaN stripe grown at 1035 °C.

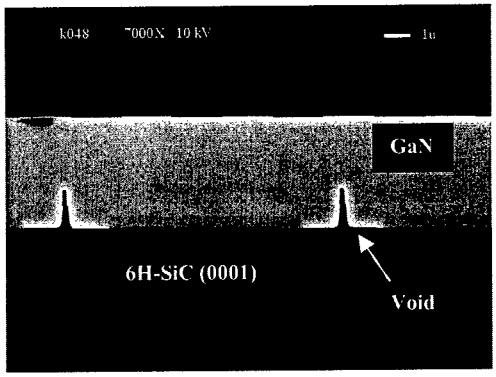


Figure 4. Cross-sectional SEM image of coalesced PE GaN on $<1\bar{1}00>$ GaN stripes grown at 1080 °C.

When two adjacent PE GaN layers coalesce, a continuous GaN layer with "⊥" shaped voids were obtained as shown in Figure 4. The vertical portion of the void probably is likely due to the lack of gas supply. When two laterally grown layers grow very close to each other, it becomes more and more difficult for source gases and byproducts of the source gases to diffuse in and out of the small gap. Finally, the top portions merge first and left a void behind.

A cross-sectional TEM image of PE on a $<1\bar{1}00>$ GaN stripe is shown in Figure 5. The threading dislocation density is very high in the GaN seed stripe area. Threading dislocations originated from the interface of the SiC and conductive buffer layer and extended into the GaN seed layer. They propagated further to the top of the GaN layer grown during PE. However, the threading dislocations were confined in the seed stripe area. There were no dislocations generated at the interface of the GaN seed layer and PE GaN layer. A significant reduction in dislocation density was achieved in the suspended laterally grown layer. The dislocations observed in the laterally

grown layer are mainly in the bottom portion. They are parallel to the basal plane and do not extended into the top portion. These results are similar to that in Ref. 5 and 6.

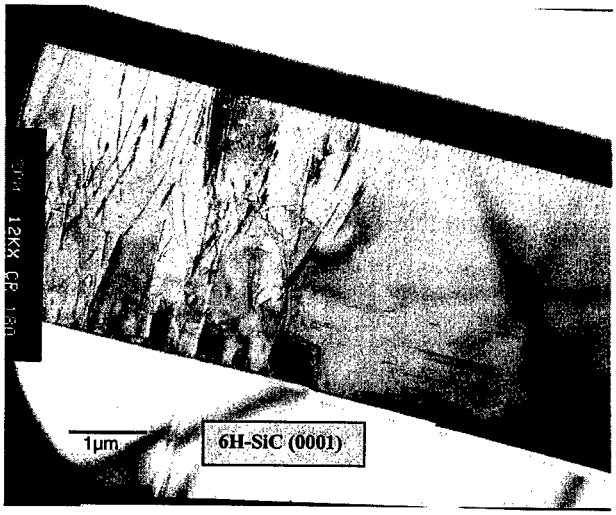


Figure 5. Cross-sectional TEM image of PE GaN on a <$1\bar{1}00$> GaN stripe.

The GaN grown on the seed stripe has very different surface morphology from that of laterally grown layer as revealed via AFM (Figure 6). The sample is a PE GaN grown on a <$1\bar{1}00$> GaN stripe. The middle region of the AFM image is the seed stripe area. Spiral growth features indicate the existence of many dislocations in this region. By contrast, suspended Pendeo epilayers

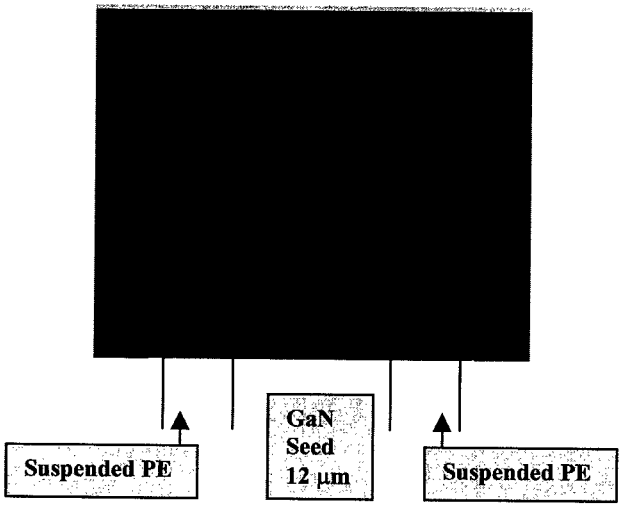
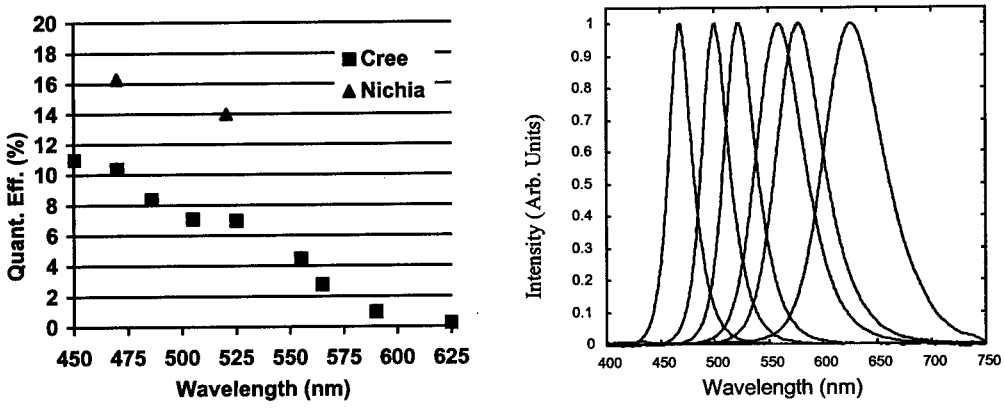


Figure 6. AFM image of the surface morphology of a PE GaN on a <$1\bar{1}00$> GaN stripe.

have a very smooth surface. Ongoing work is in progress to refine PE growth conditions and to grow laser and LED structures on the high quality laterally grown layers.

InGaN LEDs

InGaN QW LEDs have been fabricated on n-type SiC substrates using standard conductive buffer layers. Figure 7a shows the quantum efficiency as a function of wavelength. The devices were operated at 20 mA. For comparison, two points for Nichia quantum well devices grown on sapphire substrates are shown. A maximum quantum efficiency of 11% has been obtained for Cree devices having a dominant wavelength of 450 nm. The 450 nm devices are used in white light LEDs that employ converting phosphor coatings. The 470 and 525 nm devices are used for large area full color displays. The 505 nm devices are used in green traffic signals. Figure 7b shows normalized spectra for six different Cree LEDs at 20 mA. The peak emission wavelength shifts longer with increasing indium with decreasing efficiency. Peak emission wavelengths have been obtained out to 625 nm with an efficiency of 0.3%.



(a) (b)

Figure 7. (a) Quantum Efficiency as a function of dominant wavelength for InGaN LEDs and (b) select LED spectra obtained at 20 mA.

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Comparison of Different Epitaxial Lateral Overgrowth GaN Structures using SiO_2 and Tungsten Mask by Cathodoluminescence Microscopy and Micro-Raman Spectroscopy

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ABSTRACT

Epitaxial lateral overgrown GaN structures, oriented along different crystallographic directions (<11$\underline{2}$0> and <1$\underline{1}$00>), using different mask materials (SiO_2 and W), were comprehensively characterized by cathodoluminescence (CL) microscopy and micro-Raman spectroscopy. CL microscopy directly visualizes the significant differences between the overgrown areas on top of the SiO_2-mask and the coherently grown regions between the SiO_2-stripes in quantitative correlation with micro-Raman spectroscopy mapping the local strain and free carrier concentration. The overgrown GaN shows a partial strain relaxation and a high carrier concentration strongly broadens the luminescence. A strong impurity incorporation is evidenced in the coalescence regions. In contrast, the local luminescence from the areas of coherent (0001) growth is dominated by narrow excitonic emission, demonstrating its superior crystalline quality.

The technique of Epitaxial Lateral Overgrowth (ELO) to the group-III nitrides has been proven successful in significantly reducing the concentration of threading dislocations emanating from the underlying buffer layer. The ELO approach consists of masking parts of the defective crystalline substrate GaN "seed" layer with an amorphous layer so that the dislocations are prevented from propagating into the overlayer during subsequent regrowth. Furthermore, it was reported that the impurities are unintentional incorporated in the lateral overgrown GaN and the biaxial strain and defect concentration are reduced on the top of the mask.

The SiO_2-masked ELOG samples consist of a AlN-buffer layer, followed by a 3 μm thick GaN-epilayer grown by metal organic vapor phase epitaxy (MOVPE) on (0001) sapphire and subsequently structured using 120 nm thick SiO_2 stripes parallel oriented in <11$\underline{2}$0> or in <1$\underline{1}$00> direction. The width of the windows and masks are 10 μm each. The selective lateral overgrowth was achieved with 50 μm thick hydride vapor phase epitaxy (HVPE) GaN deposited on the underlying MOVPE GaN layer through the windows in the SiO_2 mask [1]. ELO of GaN using a tungsten mask was performed by atmospheric HVPE and MOCVD. On (0001) sapphire a low temperature GaN buffer was grown, followed by a 5 μm thick MOCVD layer. On the top of the MOCVD GaN a 120 nm thick tungsten film was deposited by RF sputtering at room temperature. Conventional photolithography and wet chemical etching with H_2O_2 lead to 10 μm wide tungsten stripes with 10 μm spacing. Stripe orientations along <11$\underline{2}$0> and <1$\underline{1}$00> were used. Finally, epitaxial lateral overgrowth of the tungsten stripe pattern was achieved by HVPE [4,5].

The low-temperature (5 K) CL measurements were performed in a fully computer-controlled modified scanning electron microscope. In the CL imaging mode the focused electron beam is scanned over the area of interest (256 x 200 pixels) and *a complete CL spectrum is recorded at each pixel.* The resulting 3-dimensional

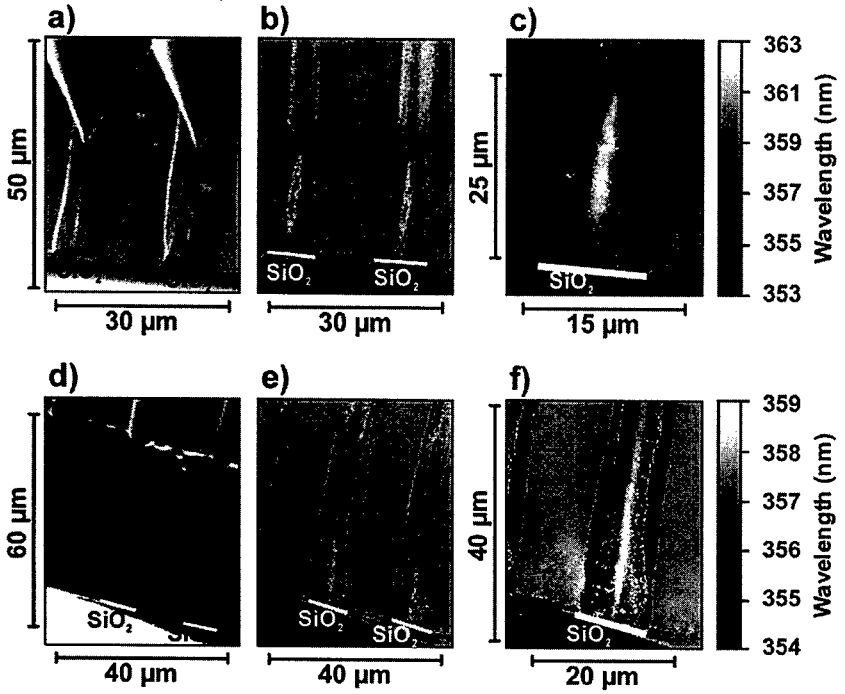

Fig. 1: SEM image, CLWI and magnified CLWI of the SiO_2 masked samples: <11$\underline{2}$0> orientation in the upper row and <1$\underline{1}$00> orientation in the bottom row

data set $I_{CL}(x,y,\lambda)$ is evaluated *ex situ* to produce local spectra, sets of monochromatic CL images, as well as CL wavelength images (CLWI) mapping the emission wavelength of the local maximum CL intensity at each sampling point [1]. A spatial resolution of 40 nm can be achieved. The µ-Raman measurements were carried out with spatial resolution better then 1 µm using a confocal micro optic and the 515.4 nm line of an Ar^+-Kr^+ mixed-gas laser for excitation [1].

Cross sectional CL mappings are presented in Fig. 1 for both SiO_2-masked samples. The scanning electron microscope (SEM) images of the resulting ELOG structures depicted in Fig. 1a and Fig. 1d demonstrate the strikingly different overgrowth schemes: While for the SiO_2 mask in <11$\underline{2}$0>-direction (Fig. 1a), the HVPE layer is terminated by sharply defined <1$\underline{1}$01>-facets, an almost smooth lateral overgrowths results for the mask in <1$\underline{1}$00>-orientation (Fig. 1d).

The CLWI in Fig. 1b visualizes three different growth regions: the GaN buffer layer, the overgrown region above the SiO_2 and the area of coherent growth between the SiO_2 pattern. In contrast to the spectral position of (D^0,X) in completely relaxed GaN (357.2 nm) the buffer layer shows a blue-shifted (D^0,X) emission at 356.4 nm according to a compressive biaxial stress of 0.8 GPa. In the coherently grown region a monochromatic triangle of almost homogeneous emission at 358 nm is visible evolving in the center between the SiO_2 stripes (Fig. 1b). The overgrowth region (CLWI with higher magnification in Fig 1c) is dominated by a blue-shifted emission around 356 nm and is very inhomogeneous showing stripe-like patterns in c-direction. Strongly red shifted, extrinsic CL (362 nm) dominates the very center of the overgrowth region, i.e. the ELO coalescence area. At the outer edges of the SiO_2 stripes a strong blue-shift (354 nm) is obtained. Areas with no CL intensity are masked out in black in the CLWIs.

The lower row of Fig. 1 (d-f) depicts the results for sample with SiO_2-pattern along <1$\underline{1}$00>. Again the three different growth regions can be separated. However, here the coherently grown region forms a uniform rectangle proceeding now up to the surface. The blue-shifted overgrowth region is even more inhomogeneous

than for sample with SiO_2 pattern along <11$\bar{2}$0>. Again the coalescence area is marked by strongly red shifted, extrinsic luminescence in the center of the overgrowth region. A strongly blue shifted emission arises from the edges of the SiO_2 stripes due to local compressive strain.

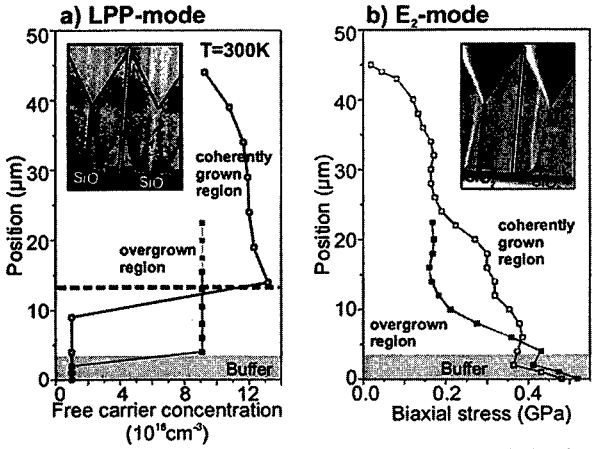

Fig. 2: µ-Raman linescans: gray line (coherently grown region) and black line (overgrown region), a) Free carrier concentration determined from the LPP-mode and b) biaxial (compressive) stress calculated from the E_2-Raman-mode.

In order to understand the spatial dependence of the luminescence we performed µ-Raman scattering-experiments in the same region where the CL microscopy was carried out. By measuring the E_2 mode we detected the local strain distribution. The free carrier concentration was determined by the position of the LO phonon-plasmon (LPP) modes [1]. Fig. 2 shows the results of different µ-Raman linescans: two different scans are marked by a gray and a black line, respectively, in the CLWI (inset of Fig. 2a) and in the SEM image (inset of Fig. 2b). The free carrier concentration in the overgrown region jumps to a value of about $9x10^{18}$ cm^{-3} outside the buffer layer and remains nearly constant up to the surface. This results from a strong impurity incorporation in the overgrown area. The free carrier concentration in the coherently grown region starts at a level below our detection limit of about $1.0x10^{18}$ cm^{-3}. At a distance of 14 µm from the substrate interface a jump occurs to a high value of $1.3x\cdot10^{19}$ cm^{-3}. In comparison with the CLWI we obtain this increase of the carrier concentration at the end of the coherently grown region (at the top of the triangle, compare Fig. 1b). In the coherently grown region we find a lower carrier concentration due to less structural defects. In Fig. 4b the biaxial stress determined by the shift of the E_2 mode is depicted. The compressive stress in the coherently grown region decreases continuously from a value of 0.5 GPa in the buffer layer with increasing distance from the substrate and is fully relaxed at the surface. The compressive stress in the overgrown region on the top of SiO_2 relaxes much faster than in the coherently grown region. At 10 µm from the interface the stress reduction stops.

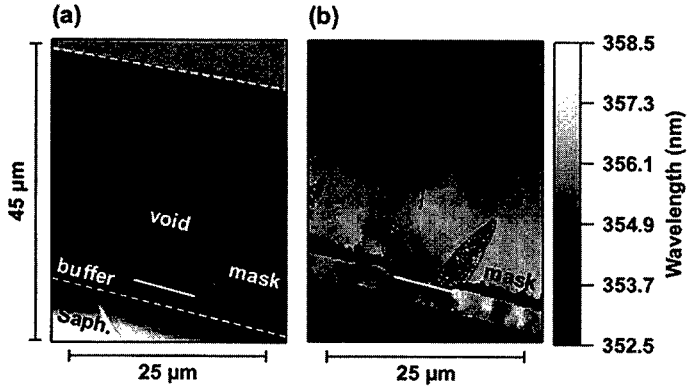

Fig. 3: SEM image, CLWI of the ELO sample with the tungsten mask along <11$\bar{2}$0>

For the purpose of comparison, CL measurements were performed on ELO samples using tungsten mask. In Fig. 3a a cross-sectional SEM image of a sample with a W mask orientated along <11$\underline{2}$0> is depicted. The SEM image proves a smooth sample surface but huge voids appear directly above the W stripes. The strongly varying local CL emission wavelength is mapped in the corresponding CLWI in Fig. 3b. As in the case of the SiO_2 masked samples, the strongest fluctuations of the emission wavelength occur above the tungsten mask. In contrast to the spectral position of (D^0,X) in completely relaxed GaN (357.2 nm) this overgrown region above the W stripes is dominated by a weak, blue-shifted and broad emission around 355 nm. In cross-section this area of blue-shifted emission always exhibits a typical form (rabbit ear structure) which obviously differs from the specific structures of the overgrown region found for the SiO_2 masked samples. Its size is self-limited by the coalescence of the <11$\underline{0}$1> facets above the W masks (Fig. 4).

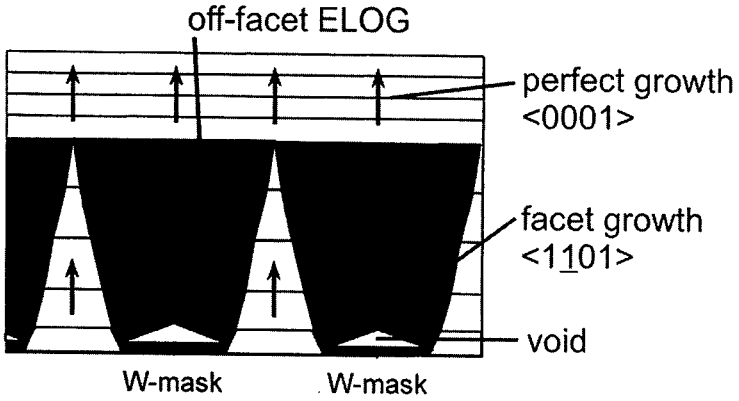

Fig. 4: Growth model

In the coherently grown region evolving in the center between the W stripes only sharp excitonic lines are visible. After 15 µm distance to the substrate facet growth stops and only perfect <0001> growth occurs both between and above the tungsten stripes. Accordingly, at the sample surface no influence of the mask position is detected in the luminescence, showing the main excitonic line at 357 nm.

Epitaxial lateral overgrowth GaN structures with SiO_2 and W mask orientated along <11$\underline{2}$0> and <1$\underline{1}$00> were characterized and regions of different growth regimes were identified. In all ELO structures the coherently grown region shows perfect excitonic CL, i.e. crystallographic quality. In the ELO sample with SiO_2 stripes in <11$\underline{2}$0> direction the coherently grown area forms a sharply defined triangle in the middle of the structure. This pattern orientation shows a strong <1$\underline{1}$01> facetting in the surfaces morphology. In the sample with pattern along <1$\underline{1}$00> the coherently grown region forms a rectangle of sharp excitonic luminescence up to the surface indicating perfect crystallographic quality and low carrier concentration in perfect agreement with µ-Raman results. Always the overgrown region is dominated by a blue shifted broad CL emission.

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Materials Science Forum Vols. 338-342 (2000) pp. 1487-1490

High Quality GaN on Si(111) using $(AlN/GaN)_x$ Superlattice and Maskless ELO

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Keywords: AFM, MOVPE, Photoluminescence, TEM

Abstract

In this work we present a novel growth method to obtain high structural quality GaN films on Si(111) by low pressure Metalorganic Vapour Phase Epitaxy (LP-MOVPE). Epitaxy by Lateral Overgrowth (ELO) is achieved starting from self organised islands on a GaN template layer, obtained after a growth mode change induced by an *in-situ* treatment of the template under silane (SiH_4). Their density and size are controlled by the silicon treatment and growth temperature. An overgrowth initiated from such islands leads to a drastic improvement of the material quality, as determined by X-ray diffraction (XRD), atomic force microscope (AFM) and photoluminescence (PL). The full width at half maximum (FWHM) on the (0002) line of GaN in rocking curve scan is as low as 525 arcsec. The dislocations density in the sample, evaluated by AFM and transmission electron microscope is in the low 10^9 cm^{-2} range. The 10K PL spectra is dominated by neutral donor bound exciton at 3.453eV with a FWHM of 11meV.

Introduction

Recently, the growth of high quality GaN materials has raised great interest for the development of optoelectronics in the visible and UV range. Si(111) is an attractive substrate for the growth of wurtzite GaN because of its low price, large scale and high perfection. Si can also be easily etched in order to realise self supported GaN crystals. The possibility of growing GaN films on silicon substrates is complicated by the large differences in their lattice parameters and thermal dilatation coefficients. However, many efforts have been done to overpass these problems. High quality GaN thin layers have been grown using different buffer structures like AlAs [1], SiC [2,3] or AlN thin layers [4,5]. Meanwhile the structural and optical properties of such layers are still poor in regard to the one deposited on sapphire and 6H-SiC substrates. Recently, the quality of GaN crystal grown on sapphire was improved via epitaxial lateral overgrowth (ELO) [6,7,8,9]. During ELO process, the growth of GaN is carried out through windows opened in a mask deposited onto a GaN template. Defects reduction occurs in the laterally grown crystal. Mask-less GaN ELO can also be performed on self organised islands [10]. Such islands are generated after a high temperature *in-situ* SiH_4 treatment of the template.

The aim of this work is to demonstrate the efficiency of this process for the growth of high quality GaN on Si(111) substrates. The GaN thin layers were characterised by X-Ray diffraction (XRD), Atomic Force Microscopy (AFM), Transmission Electron Microscopy (TEM) and Photoluminescence.

Growth process and results

Growths were performed in a horizontal low pressure MOVPE reactor. triMethylAluminium (TMA), triMethylGalium (TMG) and ammonia (NH_3) were used as precursors and pure hydrogen was chosen as carrier gas. The growths were carried out on Si (111) on-axis substrates at 100mbar total pressure. The substrates were oxidised in H_2O_2:H_2SO_4 (1:3) and etched in HF (1/10) solutions, then rinsed in deionised water before introduction into the reactor chamber. The starting point is the realisation of a buffer structure for the subsequent growth of GaN. The optimised structure consists in a 20nm AlN layer deposited at 1060°C with 10µMole.mn^{-1} TMA and 1.5slm NH_3. The GaN is subsequently grown at 1060°C with 30µMole.mn^{-1} TMG and 2slm NH_3.The structural quality of the resulting GaN thin layer is then satisfactory (sample A). In particular, the full width at half maximum (FWHM) on the (0002) line of GaN in rocking curve scan is 690 arcsec, which is one of the lowest values reported. But the GaN layer is in high tensile biaxial strain, as evidenced by photoluminescence (PL) and reflectivity (table 1) [1]. The critical thickness measured for crack free layers is only around 400nm. A second approach used a strained superlattice consisting in 5 periods of 200nm thick AlN and GaN layers in order to reduce this strain (sample B). The efficiency of the superlattice was demonstrated by a large shift of the excitons to higher energies observed on the PL and reflectivity spectra [11]. Layers are crack free for a thickness up to 900nm. The superlattice was used as template for the growth of mask-less GaN ELO. Self organised islands were then grown on a $(AlN/GaN)_5$ buffer followed by lateral overgrowth until complete coalescence as described in Fig. 1 (sample C). The 3D growth mode is induced by an *in-situ* surface treatment of the template at high temperature by SiH_4. The full description of the process is given elsewhere [10]. The FWHM on the (0002) line of GaN in rocking curve scan is as low as 525 arcsec. This is the best value ever reported for thin wurtzite GaN layers grown on Si(111).

Sample structure	I_2 (eV)	A+B (eV)	C (eV)	Rocking curve (0002)
A: AlN 20nm, GaN 400nm	3.449	3.456	-	690 arcsec
B: $(AlN/GaN)_5$, GaN 900nm	3.457	3.461	3.477	630 arcsec
C: $(AlN/GaN)_5$, islands, GaN 1.5µm	3.453	3.458	3.474	525 arcsec

Table 1 : samples specifications

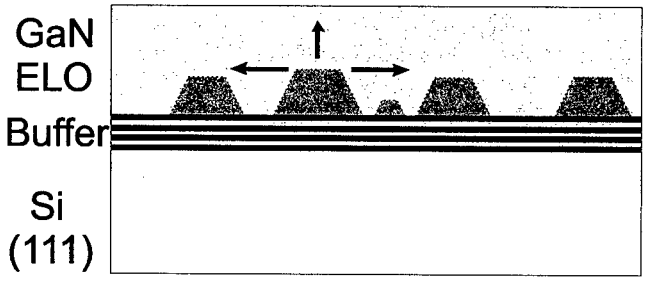

Figure 1 : schematic drawing of the mask-less ELO process

Morphology of the GaN samples

The samples were studied by AFM in tapping mode. The typical morphologies of the GaN samples grown on AlN buffer layer (A), on a $(AlN/GaN)_5$ superlattice (B) and via mask-less ELO (C) are shown for comparison in fig. 2. For all photographs, the vertical scale is 3nm. The surfaces of all films are quite smooth and present terraces separated by 2-3Å high steps. This corresponds to a GaN bi-layer (2.6Å). The surface morphology of both samples A and B are similar and present dislocations density in the 10^{10} cm^{-2} range organised along the terraces. Sample C presents a similar morphology to that observed for MOVPE samples grown on sapphire on a 3D GaN buffer layer [12]. In particular the larger pits joining two surface steps are attributed to mixed (Burgers vector $b = \frac{1}{3}\langle 11\bar{2}3\rangle$) or pure screw ($b = \langle 0001\rangle$) dislocations. The overall density of dislocation measured by AFM is 1.6 x 10^9 cm^{-2}. These measurements are consistent with TEM observations.

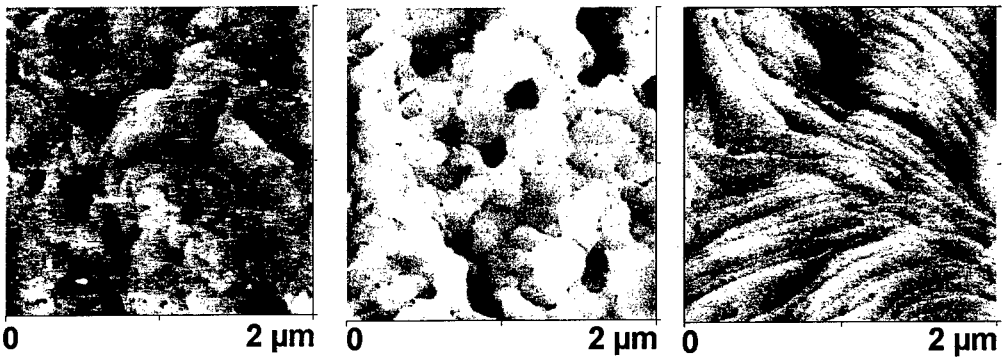

Figure 2 : surface morphology of the GaN samples recorded in tapping mode AFM.

Optical properties of the samples

The samples were assessed by low temperature (10K) photoluminescence (PL) and reflectivity. The excitation source for PL was a 10mW HeCd laser (325nm). The spectra of samples A,B and C are shown in fig. 3. The PL band edge is dominated by donor bound exciton I_2 for all of the samples. Free excitons A and C are also visible for samples A and B as checked by reflectivity [10]. The possible diffusion of Si in sample C is assumed to be responsible of the high intensity of I_2 for this sample. The FWHM of the dominating line is 15meV for samples A and B and only 11meV for sample C. Notably, the signal of donor-acceptor pairs (DAP) for this sample is very weak.

Conclusion

The efficiency of the mask-less ELO process for the growth of GaN thin layers on Si(111) was demonstrated. Both structural and optical properties are improved when a 3D mode is used as a starting point of the growth.

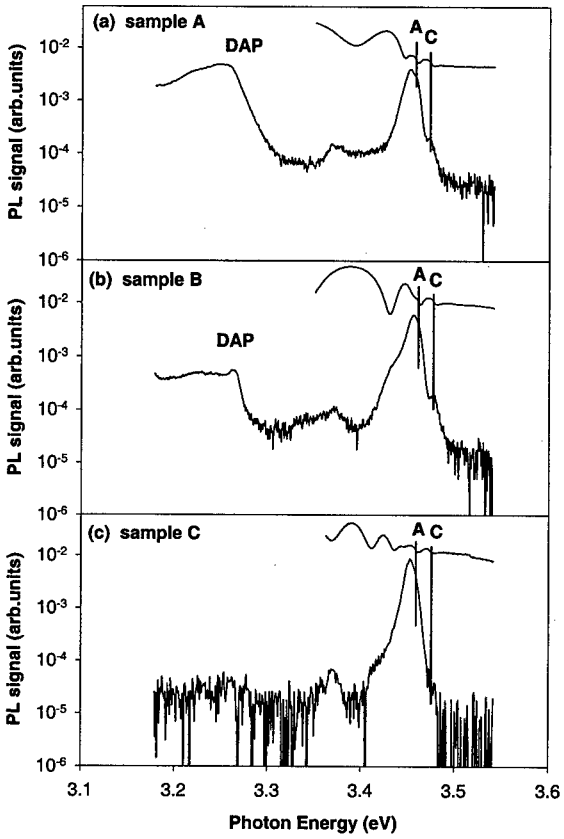

Figure 3: Optical properties of the GaN samples: 10K photoluminescence and reflectivity.

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Materials Science Forum Vols. 338-342 (2000) pp. 1491-1494

Pendeo-Epitaxy™ Process for Aluminum Gallium Nitride Thin Films on Silicon Carbide Substrates via Metalorganic Chemical Vapor Deposition

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Keywords: $Al_xGa_{1-x}N$, Auger Spectroscopy, Lateral Growth, Pendeo-Epitaxy, Selective Growth, Substrate Engineering

Abstract

Pendeo-epitaxial growth of $Al_xGa_{1-x}N$ thin films has been achieved on stripes etched in a GaN seed layer on 6H-SiC(0001) substrates using metallorganic vapor phase epitaxy. Fully coalesced thin films have been characterized for a comparison study with conventional grown $Al_xGa_{1-x}N$ thin films using scanning electron microscopy, X-ray diffraction, and high resolution scanning Auger microprobe. A FWHM of 794 arcsec has been measured for pendeo-epitaxially grown $Al_{10}Ga_{90}N$ films, which is comparable to conventional grown films on 2H-AlN/6H-SiC substrate. A variation of 1% in the atomic Al content of $Al_{10}Ga_{90}N$ thin films related to the microstructure has been measured.

Introduction

A recent topic in III-Nitride research has been selective area growth combined with lateral epitaxial overgrowth (LEO) and the application of this tandem process for reduction of the dislocation density of GaN films by several orders of magnitude in the overgrown areas. A new form of selective and lateral growth, namely 'pendeo (from the Latin: to *hang* or be *suspended*) - epitaxy' (PE) has been recently pioneered in our group [1-6], to achieve large area growth of III-N films having a continuous low dislocation density over the entire surface. The studies have primarily concentrated on the growth and characterization of GaN films and more recently on $Al_xGa_{1-x}N$ films. This process route is based on the growth of the III-N material from a side wall of a seed structure and the ability to stop lateral propagation of vertically oriented defects.

In this paper we report the growth and characterization of $Al_xGa_{1-x}N$ thin films via pendeo-epitaxy and a comparison with conventionally grown $Al_xGa_{1-x}N$ thin films.

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Experimental Procedure

Films of $Al_xGa_{1-x}N(0001)$ have been grown via pendeo-epitaxy on a 0.5 μm thick GaN(0001) seed layer grown on a high temperature, 100 nm thick AlN buffer layer previously deposited on a 6H-SiC(0001) substrate. All layers were grown using a cold-wall, vertical pancake style, RF-inductively heated metalorganic vapor phase epitaxy (MOVPE) system. The AlN buffer layers and the hexagonal GaN seed layers were each grown within the susceptor temperature ranges of 1080°C-1120°C and 980°C-1020°C, respectively, at a total pressure of 45 Torr. Triethylaluminum, triethylgallium, and NH_3 precursors were used in combination with a H_2 diluent. If employed, a 100 nm thick silicon nitride layer was used as a growth mask for blocking the continued threading dislocations during the pendeo-epitaxial growth stage. The processing of the GaN seed layer for pendeo-epitaxial growth is explained in detail in Ref. [1]. Following these processing steps, the samples were degreased and cleaned prior loading them into the MOVPE chamber. The pendeo-epitaxial growth of the $Al_xGa_{1-x}N$ layers was achieved within the susceptor temperature range of 1080-1120°C. $Al_xGa_{1-x}N$ layers having an atomic Al content of approximately 10% were grown by introducing triethylaluminum into the growth chamber.

A JEOL 6400 FE scanning electron microscope (SEM) and a Philips X'Pert MRD X-ray diffractometer were employed for microstructural analysis. A JEOL JAMP-30 high resolution scanning auger microprobe was utilized for measurements of the Al content of the as grown $Al_xGa_{1-x}N$ layers. The atomic Al content was calculated in comparing the intensity ratios of the Al and Ga signals.

Results and Discussion

In the first phase of this research, seed structures of 2 μm wide and 3 μm spaced elongated GaN stripes, covered with a silicon nitride mask to prevent vertical propagation of threading dislocations, were employed. Figure 1 shows a cross-sectional scanning electron micrograph of a single GaN seed stripe from which lateral growth of $Al_{10}Ga_{90}N$ occurred. The rough surface of the $Al_{10}Ga_{90}N$ film above the silicon nitride mask indicates that the $Al_{10}Ga_{90}N$ nucleated on the silicon nitride rather than overgrowing it. Based on this result a different seed structure was developed having a smaller width of the GaN seed stripes to reduce the area from which the threading dislocations can propagate into the regrown film and without the silicon nitride growth mask.

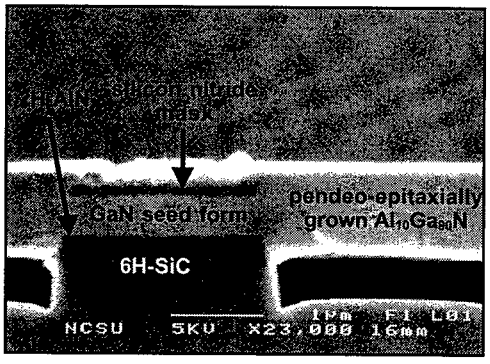

Figure 1. Cross-sectional scanning electron micrograph of a pendeo-epitaxially grown $Al_{10}Ga_{90}N$ film showing the results of nucleation of the solid solution on the silicon nitride mask covering the GaN stripe.

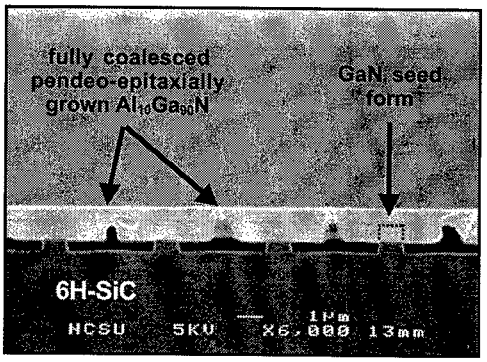

Figure 2. Cross-sectional scanning electron micrograph of a pendeo-epitaxial $Al_{10}Ga_{90}N$ film grown from and over several unmasked GaN seed stripes.

The seed stripes were 1 μm wide and spaced 4μm apart, as shown in the cross-sectional scanning electron micrograph of a pendeo-epitaxial grown $Al_{10}Ga_{90}N$ film in Figure 2. The film was fully coalesced and possessed a smooth surface morphology. The cross-sectional scanning electron micrograph shows no indications of boundaries in the regions of coalescence or cracking in the film. The size and shape of the original GaN seed stripes from which the $Al_{10}Ga_{90}N$ films were grown is also schematically indicated in this Figure. The threading dislocation propagation of the later films was studied using transmission electron microscopy (TEM).

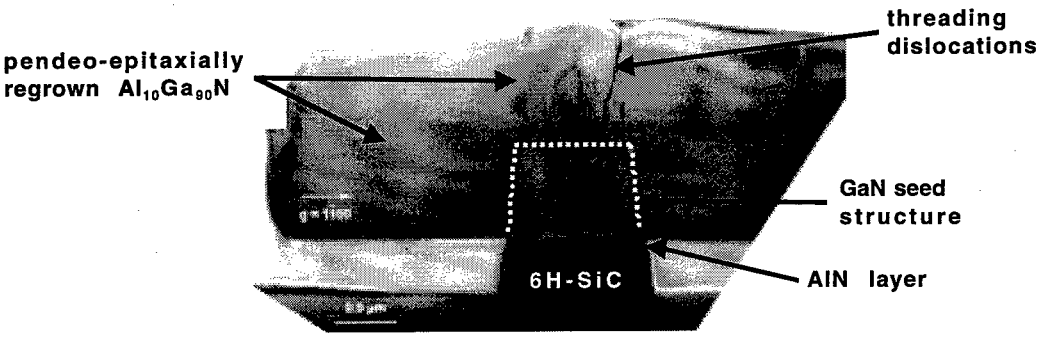

Figure 3. Transmission electron micrograph of pendeo-epitaxial grown $Al_{10}Ga_{90}N$. The threading dislocations do not propagate laterally from the GaN seed form into the regrown $Al_{10}Ga_{90}N$.

As shown in the transmission electron micrograph of Figure 3, the threading dislocations of the GaN seed form do not propagate laterally into the pendeo-epitaxially regrown $Al_{10}Ga_{90}N$ region. Due to the reduced width of the seed form, the amount of dislocations propagating vertically during regrowth is reduced. Growing the $Al_{10}Ga_{90}N$ film out vertically reduced further the threading dislocation density caused by the annihilation effect of opposite oriented dislocations.

The $Al_{10}Ga_{90}N$ films shown in Figure 2 have been characterized and compared to $Al_{10}Ga_{90}N$ films conventionally grown on 6H-SiC substrates. Figure 4(a) shows an X-ray diffraction (XRD) omega-scan of a 600 nm thick $Al_{10}Ga_{90}N$ film grown on a 100 nm thick high-temperature AlN buffer layer. The FWHM is 708 arcsec. In comparison, Figure 4(b) shows an omega-scan of a 2 μm thick pendeo-epitaxial grown $Al_{10}Ga_{90}N$ film, grown from GaN stripes. The FWHM is 794 arcsec, which is comparable to the conventionally grown film.

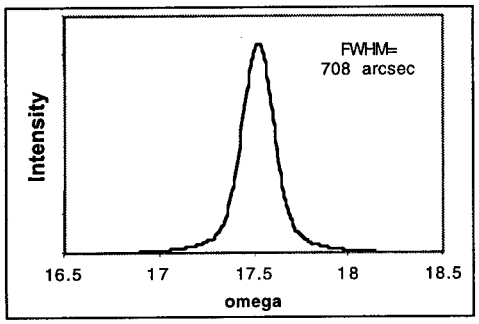

Figure 4(a). XRD omega-scan of a 600 nm thick $Al_{10}Ga_{90}N$ film grown on a 100 nm thick high-temperature AlN buffer layer on a 6H-SiC wafer.

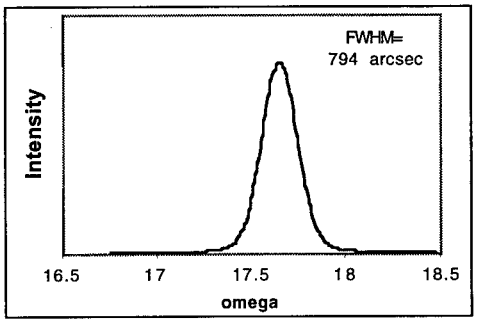

Figure 4(b). XRD omega-scan of 2 μm thick pendeo-epitaxial grown $Al_{10}Ga_{90}N$ film, grown GaN seed forms on a 6H-SiC wafer.

The atomic concentration of the Al in different areas of the pendeo-epitaxially grown $Al_{10}Ga_{90}N$ films was determined via high resolution scanning Auger electron spectroscopy using a beam size of ≈ 500 nm. An average Al content of 8.7% was measured in the surface regions above the GaN seed structures. In contrast, an average Al content of 9.7% was measured in the surface of the coalesced regions between the seed forms. The 1% difference cannot be explained at this point. A possible correlation to the dislocation density is part of the ongoing studies. The sampling depth of Auger electrons is on the order of several atomic monolayers, which eliminates any contributions of the GaN seed stripes to the measurement.

Summary

Pendeo-epitaxial growth of $Al_{10}Ga_{90}N$ has been achieved on GaN seed forms (stripes) on 6H-SiC(0001) substrates. The use of a silicon nitride growth mask atop the GaN stripes results in both nucleation and growth of the $Al_xGa_{1-x}N$ rather than coalescence, and a rougher surface relative to the portions of the film between the stripes. An XRD FWHM of 794 arcsec was measured, which is comparable to that of conventionally grown $Al_{10}Ga_{90}N$ films on 2H-AlN/6H-SiC substrates. A variation in the atomic Al content across the film surface of about 1% has been measured with values of 8.7% and 9.7% above the GaN stripes and within the coalesced regions, respectively. The reason for this variation is not known at this point and is the subject of ongoing studies.

Acknowledgement

The authors express their appreciation to Cree Research, Inc. for supplying the SiC wafers. This work was supported by the Office of Naval Research under the contracts N00014-96-1-0765 and N00014-98-1-0384 (C. Wood, technical monitor) and N00014-98-1-0654 (J. Zolper, technical monitor).

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Reduction of Defects on GaN and AlGaN by In-Doping in Metalorganic Vapor Phase Epitaxy

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Keywords: Crack, Dislocation, In-Doping, XRC

Abstract

In-doping to GaN and AlGaN was performed at 1000°C by supplying trimethylindium (TMI). Concentrations of the In atoms in epitaxial layers were 10^{18}~10^{19} cm^{-3}. GaN layers with and without the In-doping were characterized by molten KOH etching, photoluminescence (PL) and X-ray rocking curve (XRC) observations. Reduction of etch pit density by the In-doping was observed and narrowing of the full width at half maximum (FWHM) of PL and XRC spectra was also observed. These result indicate that dislocations in the growth layer are reduced. Narrowing of FWHM of XRC was also observed for AlGaN with the In-doping. Moreover, suppression of cracks on the AlGaN layer was observed by the In-doping. These results were attributed to relaxation of tensile stress in the AlGaN layer by the In-doping.

Introduction

It is widely recognized that GaN on a sapphire substrate contains a number of edge and screw dislocations and some efforts for the defect reduction have been demonstrated[1,2]. Recently, the isoelectronic In-doping effect have been reported for the GaN growth by metalorganic vapor phase epitaxy (MOVPE) [3] . In ref. 3, improvement of the GaN crystal quality by incorporation of small amount of In atoms has been observed. Similar effect has been reported for the GaN growth by molecular beam epitaxy (MBE) [4]. Surface flatness has been improved by adding the In flax during the growth by MBE. This effect was attributed to the surfactant effect of the In atoms. These methods have been applied to only GaN. However, we think that the In-doping method is more attractive for the AlGaN growth on GaN rather than the GaN growth. The atomic size of the In atom is larger than Ga and, consequently, the stress in AlGaN caused by lattice mismatch will be relaxed by incorporating In atoms to AlGaN. In this report, we show the effect of the In-doping to GaN and AlGaN.

Experimental

GaN was grown on a c-face sapphire substrate at 1000°C by atmospheric MOVPE. InN layer deposited at 600°C was used as a buffer layer[5]. Typical thickness of the GaN layers was 2μm. The In doping was made by adding trimethylindium (TMI) to the precursors for GaN, i.e., trimethylgallium (TMG) and ammonia (NH3), of which flow rates were 36μmol/min and 4slm, respectively . $Al_xGa_{1-x}N$ (x=0.08, 0.1) was grown on a GaN layer which was grown without In-doping and the typical thickness of the AlGaN was 1μm. Aluminum precursor was trimethylaluminum (TMA) and the AlGaN layers were grown at 1000°C. For n-type doping, monomethylsilane(MMSi) was used as Si precursor [6].

Results and discussion

We measured the In concentration in AlGaN by secondary ion mass spectroscopy (SIMS) . Figure1 shows the In distribution profile of continuously grown three AlGaN layers with different TMI flow rates. The measured In concentrations were 4×10^{18} and 8×10^{18} cm^{-3} for the TMI flow rates of 40 and 80μmol/min, respectively. This result indicates that the In-doping was possible at the temperature of 1000°C though the In solubility is very low at this temperature.

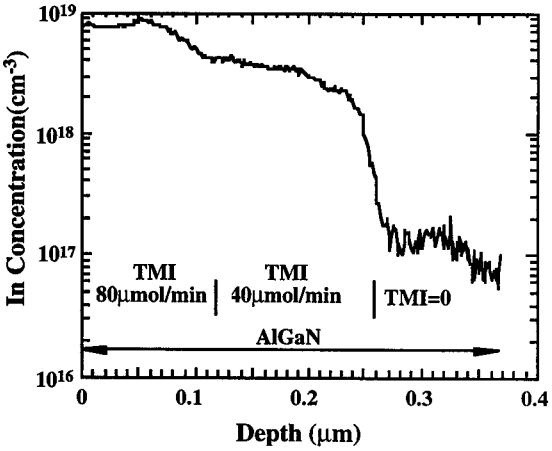


Fig.1 In depth profile In continuously grown AlGaN with differet TMI flow rate.

The GaN layers with and without the In-doping were characterized by etch pit observation using molten KOH at 350°C for 3 minute. Large (>1μm) and small (<0.5μm) etch pits, of which shapes were hexagonal pyramid, were observed on the surfaces[7]. The microscope observation showed that the density of the large size etch pits was drastically reduced by the In-doping and the total etch pit density of GaN with the In-doping was about half of that of GaN without the In-doping. We have observed that the etch pit density of the large pits was independent on the GaN epilayer thickness. Origin of the large etch pit is thought as a nanopipe and the origin of the small pit is screw dislocations[8]. Therefore, these results indicate the In-doping is effective for the reduction of screw dislocations.

Photoluminescence (PL) of undope GaN layers with and without In-doping were observed at 77K. Figure 2 shows the dependence of the full width at half maximum (FWHM) on TMI flow rate. The FWHMs of GaN with the In-doping were narrower than that of the GaN without the In-

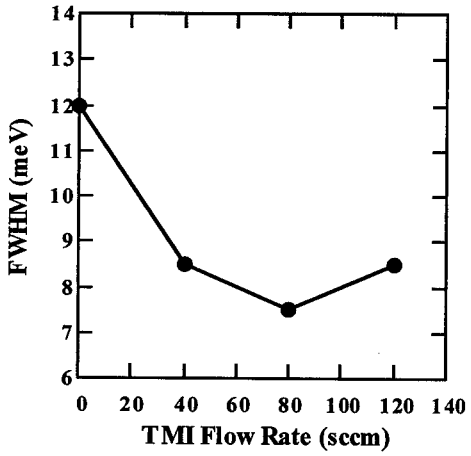


Fig.2 Dpendence of FWHM of GaN PL spectra on TMI flow rate.

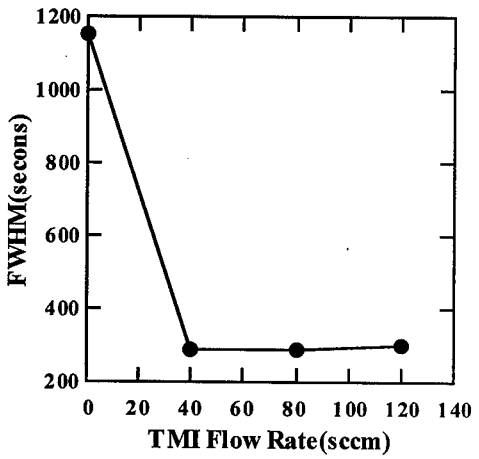


Fig.3 Dpendence of FWHM of GaN XRC on TMI flow rate.

doping. However, the values of the FWHM of the GaN with the In-doping are almost same values. This shows that the In-doping effect is saturated at the TMI flow rates of this experiment. We have also characterized GaN layers by ω-mode X-ray rocking curve (XRC) of the symmetric diffraction of (0004). GaN films have mosaic structure. The fluctuation of the columns of the mosaic was divided into tilting and twisting. The ω-mode XRC characterizes the tilting. Figure 3 shows the dependence of FWHMs of XRC on the TMI flow rates. The dependence is similar to the PL spectra. Therefore, Fig.3 indicates that the fluctuation of the tilting is reduced by In-doping. As the tilting of the columns induce screw dislocations[9], this result supported by the reduction of the etch pit density, that is the reduction of screw dislocations.

For the AlGaN layers, we also measured the ω-mode XRC. Figure 4 shows the dependence of FWHMs of XRC for undope and Si-doped AlGaN on the TMI flow rate. Both undope and Si-doped AlGaN have similar dependence and show the dependence in contrast with GaN. Figure 4 shows that the narrowing effect dose not saturate at these TMI flow rates. AlGaN on GaN is under tensile stress because the lattice constant of AlGaN is smaller than that of GaN. As atomic size of In is larger than those of Ga and Al, In incorporation to AlGaN will relax the tensile stress. Moreover, the AlGaN layers were grown on GaN without the In-doping. Therefore, dislocations are transmitted from GaN layer. We think that Fig.4 shows the relaxation effect of In atoms rather than reduction of dislocations.

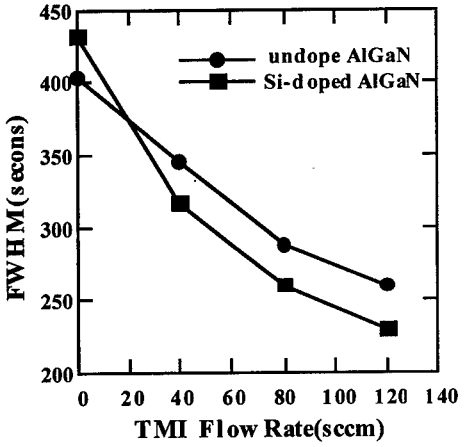
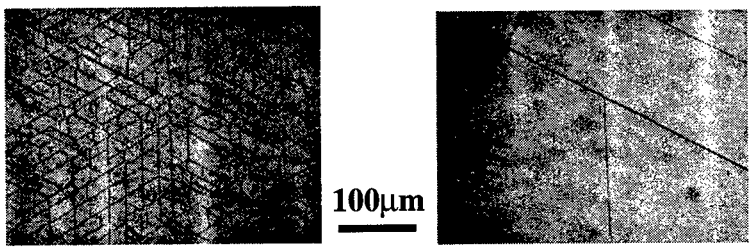


Fig.4 Dpendenccce of FWHM of AlGaN XRC on TMI flow rates.

Crack formation is observed in an AlGaN epitaxial layer on GaN when the thickness is in excess of the critical thickness which depends on the Al content. In this experiment, cracks were observed on the AlGaN surfaces of which Al content was 10%. However, the crack density was different between AlGaN layers with and without the In-doping. Figure 5 shows the photographs of the $Al_{0.1}Ga_{0.9}N$ surfaces, of which thickness is about 1μm, observed with a Nomarski microscope. It



(a) (b)

Fig. 5 Photographs of the surfaces of Al0.1Ga0.9N (a) without and (b) with the In-doping.

can be seen that the crack density of AlGaN with the In-doping is lower than that of AlGaN without the In-doping. This result directly indicates that the In-doping relaxes of the tensile stress in AlGaN and supports the result of Fig.4.

Conclusion

The In-doping of GaN and AlGaN was performed at 1000°C and the doping levels of 10^{18}~10^{19} cm^{-3} were obtained. GaN layers with and without the In-doping were characterized by molten KOH etching, photoluminescence (PL) and X-ray rocking curve (XRC) observations. These results indicate that the small amount of In atoms in GaN is effective for the reduction of the dislocations. Narrowing of FWHM of XRC was observed for AlGaN with In-doping. Suppression of cracks on the AlGaN layer were also observed. These results were attributed to relaxation of the tensile stress in the AlGaN layer by the In-doping rather than reduction of dislocations like GaN.

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Comparison of AlGaN and GaN Grown on Various Substrates: Step Flow Growth on $LiGaO_2$ at Low Growth Temperature

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Keywords: Atomic Force Microscopy, Dislocation, $LiGaO_2$, Polarity, Rf-Plasma Nitrogen Source, Step Flow Growth, Surface Morphology, X-Ray Diffraction

Abstract

AlGaN/GaN heterostructures were grown on $LiGaO_2$ (LGO), sapphire, and hydride vapor phase epitaxy (HVPE) grown GaN substrates. Structural properties and surface morphology of each film was compared. LGO substrates produced the lowest FWHM values for both symmetric <00.4> and asymmetric <10.5> reflections. The films grown on LGO substrate also showed the best morphology. The small lattice mismatch of LGO to nitrides and Ga-polarity of grown films could be the primary reason for the smoother surface of AlGaN/GaN structure on LGO substrates. In developing the HFET structure on the LGO substrate, we have observed step flow growth in a structure with 300 Å thick $Al_{0.25}Ga_{0.75}N$ on 2.4 μm thick GaN, which is very similar to the films grown by MOCVD. A high III/V flux ratio during growth and recently improved polishing of LGO substrates may have aided in promoting two dimensional step flow growth.

There has been rapid progress in the growth of AlGaN/GaN heterostructures required for hetero structure field effect transistors (HFET). Of particular importance is the ability to produce a good heterojunction interface and low defect density AlGaN. Conventional substrates for the growth of GaN-based HFET structures are sapphire or SiC. $LiGaO_2$ (LGO) has been considered as an alternative substrate for the growth of nitrides and shows promise due to the relatively small lattice-mismatch between LGO and GaN [1-7]. Recently, we reported the first demonstration of a two-dimensional electron gas (2DEG) produced at an AlGaN /GaN heterostructure on LGO. We observed a 2DEG mobility of 731 cm^2/Vs at room temperature and 2166 cm^2/Vs at 77 K [8]. The interface roughness, 6.6 nm RMS, (inferred from surface measurements by AFM) was relatively high for this structure. Thus, a key to continued improvement of GaN on LGO relates to improved interface quality and surface morphology.

Herein, we present the effects of various substrates on the growth of AlGaN and GaN layers as produced by molecular beam epitaxy (MBE) with an rf-plasma nitrogen source at relatively low growth temperature. The flexibility of utilizing low growth temperature is very important for devices in controlling interface quality, defect density, and dopant placement and activity. AlGaN/GaN heterostructures were grown on LGO, sapphire, and hydride vapor phase epitaxy grown GaN (HVPE-GaN) substrates. Here, we focus on the comparison of the material quality of AlGaN layers.

These films were grown in a Riber 32 MBE system equipped with a radio frequency plasma nitrogen source manufactured by Oxford Applied Research (CARS-25). GaN layers were first grown on each substrate and AlGaN layers were grown on top of the GaN layers. The thickness of all the GaN layer on each substrate is 1 μm. The thicknesses of the AlGaN layer grown on the 1 μm GaN layers for each substrate are 3400 Å for LGO, 2300 Å for HVPE-GaN substrate, and 2300 Å for sapphire. The HVPE grown substrate consisted of an 18 μm thick GaN film on sapphire. All of these structures were grown at substrate temperature of 700 °C with a growth rate of approximately 0.45 μm/h. Nitrogen pressure was 3.2×10^{-5} Torr and rf-power was 500 W. Prior to GaN growth on LGO, a 200 Å GaN

buffer was grown with a low growth rate after 2 minute exposure to nitrogen plasma at 700 °C. In the same way, the sapphire was nitridized for 10 minutes at 800 °C and a GaN buffer was grown with the same condition used for LGO. On the HVPE-GaN substrate, growth was initiated without nitridation or a buffer layer. The structural quality and surface morphology were characterized by double crystal x-ray diffraction and atomic force microscopy (AFM).

The double crystal x-ray diffraction, <00.4> reflection full width at half maximum (FWHM) of the AlGaN layers was 243 arcsec, 449 arcsec, 478 arcsec for films grown on the LGO, HVPE grown GaN substrate, and sapphire, respectively. The asymmetric <10.5> reflection FWHM and the Al composition of the AlGaN layer for each sample are listed in Table 1. LGO substrate produced the lowest FWHM values for both symmetric <00.4> and asymmetric <10.5> reflections, which implies better structural quality under these growth conditions.

Utilizing etching experiments with a NaOH solution, we determined the crystal polarity of GaN films. According to the results of Seelmann-Eggerbert, *et al.* [9], the surface of GaN with Ga-polarity is inert to KOH or NaOH solutions, while the surface of N-polar GaN is not. After a three hour dip in the NaOH solution, the GaN grown on sapphire was etched 3000 Å and the surface became hazy. This indicates that the GaN grown on sapphire substrate is N-polar or consists of mixture of Ga-polar and N-polar regions. GaN grown on the cation (Li, Ga) terminated surface of LGO was inert to the NaOH solution. The LGO substrate used for this study contained a small region with an anion (Oxygen) terminated face. The surface of the GaN in this region was etched. This result implies that GaN grown on LGO does conserve the polarity of the LGO substrate. Similarly, the GaN substrate grown by HVPE showed Ga-polarity and the MBE-grown GaN on top of this substrate had the same polarity. It has been shown that Ga-polar material is necessary for the producing a two dimensional electron gas by polarization effects at the AlGaN/GaN interface [10].

For the HFET application, obtaining a smooth interface is very important, since a rough AlGaN/GaN interface can reduce the channel carrier mobility and velocity. We assume that by observing the thin AlGaN surface, the interface quality of AlGaN/GaN heterostructure can be inferred. AFM images of each sample are shown in Fig. 1. The surface of the AlGaN/GaN layer grown on sapphire is rough and grainy indicating three dimensional growth. The film grown on the HVPE-GaN substrate also resulted in rough surface morphology. However, this surface contained larger areas of smooth regions disconnected by pits. In terms of the surface smoothness and the density of pits, the film grown on LGO substrate showed the best morphology.

The grainy three-dimensional growth of GaN on sapphire substrate may, in part, be related to the large lattice mismatch of sapphire to GaN. Nitrogen polarity or multi-polarity of AlGaN and GaN can also result in three-dimensional growth [11]. For this experiment we also cannot rule out the effects of non-optimum nitridization of the substrate prior to growth. The AlGaN/GaN sample on the HVPE GaN buffer showed a smoother surface than growth on sapphire. However, this surface was not as smooth as that on LGO despite the fact that both grew with a Ga-polarity. Thus, some other factor, such as a smaller lattice-mismatch, appears to enhance the factors that yield a more two-dimensional growth. In developing the HFET structure on the LGO substrate with more refined efforts, we have observed step flow growth in a structure with 300 Å thick $Al_{0.25}Ga_{0.75}N$ on 2.4 μm thick GaN that was grown at 650 °C (See Fig. 2.). This is a lower growth temperature than for the sample described above and shown in Fig. 1 (a). The ratio of group III and V fluxes was larger (14 % increase of Ga flux with the same nitrogen flux) than that used for the growth of structure of Fig. 1 (a) and small Ga droplets were observed on the surface after growth. We utilized a LGO polishing process developed by Georgia Tech to remove surface defects frequently observed on the vendor-supplied substrates. The improved surface morphology for this sample resulted from the enhancement of two dimensional growth which is related to increased flux of column III elements [12,13]. The polished, smoother surface of starting substrate may have contributed to promoting Ga migration on the growing surface. Step flow growth can occur in the case of MOCVD growth at very high temperatures (above 1000 °C) [14]. The typical growth mode for high III/V ratio with MBE is reported to show spiral patterns around dislocation cores [12,15]. As can be seen in Fig. 2, our observations are more similar to the films grown by MOCVD [14]. The hexagonal pit hole in Fig. 2 (a) is assumed to be a nano-pipe with a diameter of approximately 120 nm.

The tiny pit holes in Fig. 2 (a) are dislocation cores. The calculated dislocation density from these surface features is 5×10^8 cm^{-2} which agrees well with our previous TEM analysis [16]. This dislocation density is comparable to high quality MOCVD grown GaN on sapphire.

Fig. 3 shows the result of structural characterization of this film as determined by x-ray diffraction. The FWHM for GaN for symmetric <00.4> and asymmetric <10.5> reflections are 114 arcsec and 203 arcsec, respectively. Extracting FWHM values from the very thin AlGaN layer was difficult because of the weak signal intensity. The small asymmetric value reflects the low dislocation density of this structure on LGO.

In conclusion, we observed improvements in the structural quality and surface morphology of AlGaN/GaN heterostructures grown on LGO. We believe these relate to the small lattice mismatch of LGO to nitrides and the Ga-polarity of nitrides grown on the cation face of LGO substrate, which is favorable not only for a smooth surface but also for producing a 2DEG from polarization effects. These are promising features of the LGO substrate for the development of AlGaN/GaN based HFETs.

By increasing the III/V flux ratio and by using custom polished LGO substrates with smoother surfaces, two dimensional step flow growth was observed with low dislocation densities.

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Units : arcsec

Substrates	GaN <00.4>	GaN <10.5>	AlGaN <00.4>	AlGaN <10.5>	Composition
$LiGaO_2$	185 ± 2	361 ± 7	243 ± 2	397 ± 40	$Al_{0.26}Ga_{0.74}N$
HVPE GaN on Al_2O_3	291 ± 1	250 ± 17	449 ± 1	~ 850*	$Al_{0.22}Ga_{0.78}N$
Al_2O_3	586 ± 5	430 ± 14	478 ± 31	503 ± 295 **	$Al_{0.25}Ga_{0.75}N$

* Due to extremely low intensity signal, fit to the AlGaN peak on the HVPE GaN material is only an estimate.
**Low intensity peaks led to larger errors.

Table 1 Double crystal X-ray rocking curve FWHM data on various substrates.

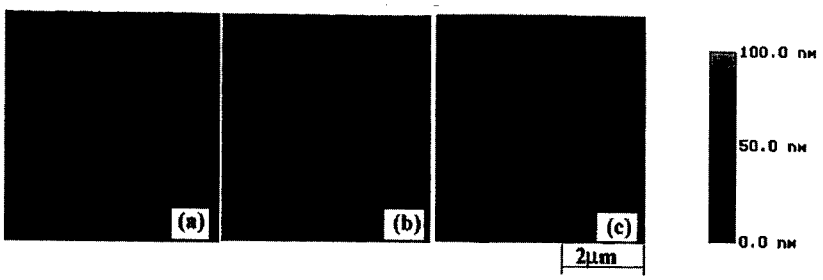

Fig. 1 AFM images (5 μm × 5 μm) of AlGaN/GaN layers on (a) LGO, (b) HVPE grown GaN, and (c) sapphire.

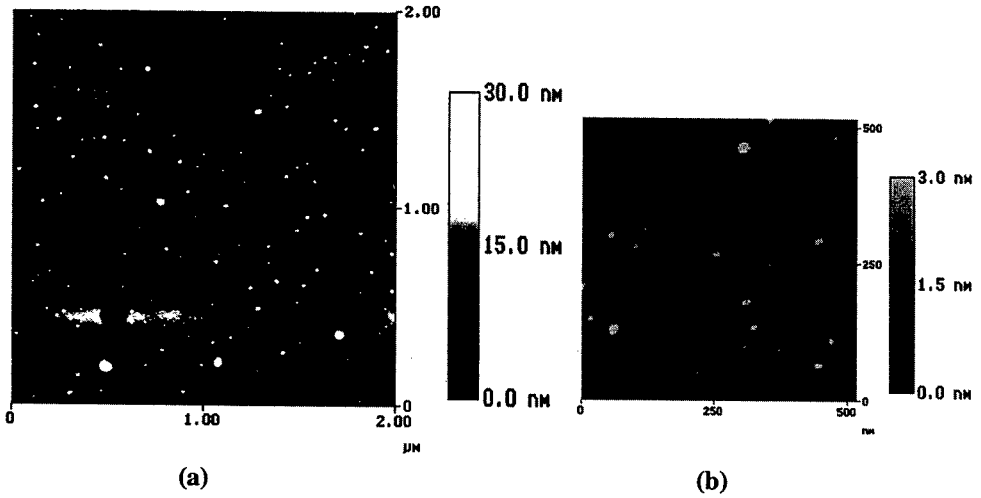

Fig. 2 AFM images of AlGaN/GaN surface showing step flow growth for (a) 2 μm × 2 μm size scan, and (b) 516 nm × 516 nm size scan.

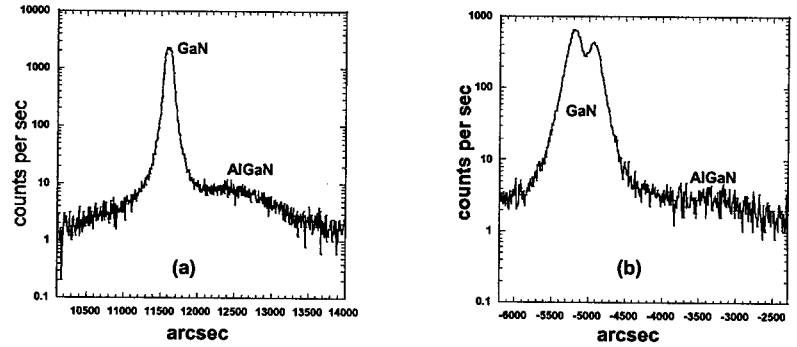

Fig. 3 X-ray rocking curve of AlGaN/GaN structure grown on LGO with step flow growth; (a) Symmetric <00.4> reflection with FWHM of 114 arcsec for GaN, (b) Asymmetric <10.5> refection with FWHM of 203 arcsec for GaN. The double peaks for (b) result from different wavelengths from the X-ray source (Kα1 and Kα2 contributions).

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Pulsed Laser Deposition: A Novel Growth Technique for Wide-Bandgap Semiconductor Research

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Keywords: AlN Encapsulation, AlN High Temperature Dielectrics, Ga-Al-N Alloys, Ohmic Contacts, Pulsed Laser Deposition, Thyristors, TiN

Abstract: The present work describes a novel, relatively simple and efficient technique of pulsed laser deposition (PLD) for rapid prototyping of thin films and multilayer heterostructures of wide-bandgap semiconductors and related materials. In this method, a KrF-pulsed excimer laser is used for ablation of polycrystalline, stoichiometric targets of wide-bandgap materials. Upon laser absorption by the target surface, a strong plasma plume is produced, which then condenses onto the substrate, which is kept at a suitable distance from the target surface. We have optimized the processing parameters, such as laser fluence, substrate temperature, background gas pressure, target to substrate distance, and pulse repetition rate, for the growth of high-quality thin films and heterostructures of AlN, GaN, and their alloys. Application of this technique in the fabrication of high-quality AlN thin films for SiC encapsulation, low-leakage AlN dielectric layers, and epitaxial TiN ohmic contacts for high-temperature SiC-based thyristors is discussed.

Introduction: Wide band gap (WBG) semiconductor materials, such as AlN, GaN, AlGaN, and SiC, have tremendous potential in a number of areas such as high-temperature electronics, high-power electronics, UV detectors, and emitters. A variety of thin film deposition techniques have been playing a dominating role in the advances of the wide band gap technologies. Here, we discuss the use of a relatively simple technique, namely, pulsed laser deposition (PLD)[1], for the fabrication of thin films of AlN, GaN, AlGaN and their alloys. In this technique, a high power pulsed laser was used for the evaporation or ablation of the wide band gap materials. Due to a strong laser coupling with the material, and laser-material interaction, the evaporated species have higher kinetic energy (~100 eV) as compared to that in conventional evaporation techniques. The laser-material interaction process also controls the composition of the target material, which is interesting in the context of fabrication of alloys and multicomponent systems. Due to simplicity and rapid prototyping in the fabrication of thin films, PLD can be useful to study the growth, doping, heterostructures, and alloys of GaN and related materials. In this paper, we highlight the growth and characterization of Al-Ga-N films, and the application of the laser-deposited AlN films for the development of high-temperature SiC based thyristors.

Experimental: The schematic for PLD is shown in Fig. 1. A KrF excimer laser ($\lambda = 248$ nm, $\tau =$ 25 ns) was used for the ablation of a polycrystalline, stoichiometric AlN and GaN targets (99.99 purity) at an energy density of ~1 J/cm^2. The NH_3 background gas pressure was varied from 10^{-6} to 10^{-3} Torr. The deposition rate and the film thickness were controlled by the pulse repetition rate (5 to 10 Hz) and total deposition time (30 to 60 min.). The PLD films were characterized by four-circle x-ray diffraction (XRD), atomic force microscopy (AFM), UV-visible spectroscopy,

photoluminescence spectroscopy (PL), cathodoluminescence spectroscopy (CL), Rutherford backscattering spectrometry (RBS) and ion channeling, transmission electron microscopy (TEM), and electrical transport measurements.

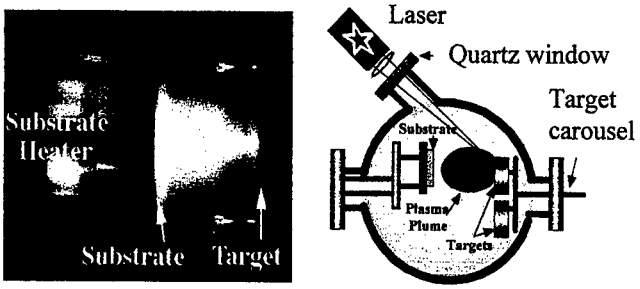

Figure 1. Schematic of the laser induced plasma plume from GaN target (left) the PLD (right).

Epitaxial growth and characterization of AlN, GaN, and AlGaN alloys: The crucial parameters in the PLD of epitaxial films are the deposition temperature, background gas pressure, target-to-substrate distance, laser fluence, and pulse repetition rate. We have studied the dependence of these parameters on the crystalline quality, surface morphology, and the optical and electrical properties of the III-V nitride films [1]. We found that GaN and AlN grew epitaxially on sapphire at a substrate temperature as low as 600 °C. However, the crystalline quality of these films improved with an increase in the substrate temperature. High-quality epitaxy was obtained when the films were grown under a background NH_3 gas pressure of $5x10^{-5}$ Torr and a substrate temperature of 750 to 850 °C. The XRD θ–2θ angular scans of a 2000-5000 Å thick film clearly show only a {000*l*} family of the planes of wurtzite-AlN and GaN with full-width-at-half-maximum (FWHM) of the rocking curve (ω) for the (0002) peak of about 5 to 7 arc-minutes. The quantitative analysis of the crystalline quality, composition, and interface structure of the III-V nitride films was carried out by RBS and ion-channeling techniques. The ratio of the RBS yield with the He^+ beam incident along [0001] (channeled) to that of a random direction, respectively, (χ_{min}), reflects the epitaxial quality of the film. Figures 2 (a) and (b) show the aligned and random backscattering spectra for the AlN and GaN films. The χ_{min} near the surface region of the films is ~3%, indicating a high degree of crystallinity. It should be noted that some exist dislocations always exist close to the interface, due to a large lattice mismatch between the film and the substrate. Our channeling results (aligned spectra) clearly indicate an increase of the χ_{min}, up to ~10 to 12% near the interface region, suggesting dislocation density of $10^{10}/cm^2$ near the interface. We also observed a band edge emission in PL, as well as CL, for PLD GaN films, the emission lines due to the recombination of excitons bound to neutral donors, transitions from donor-acceptor impurities, and the yellow band. The FWHM of the free exciton peak is 45 meV at 80K. All films grown at 750 to 850 °C were shiny, and the surface roughness as measured by AFM for the GaN and AlN was ~20 nm and 5 to 8 nm, respectively. The electrical resistivity at room-temperature for ~0.5-μm-thick GaN film was ~10^{-2} to 10^3 Ω-cm, the mobility was 25 to 90 $cm^2V^{-1}s^{-1}$, and the carrier concentration was 5 x 10^{16} to 6 x 10^{19} cm^{-3}.

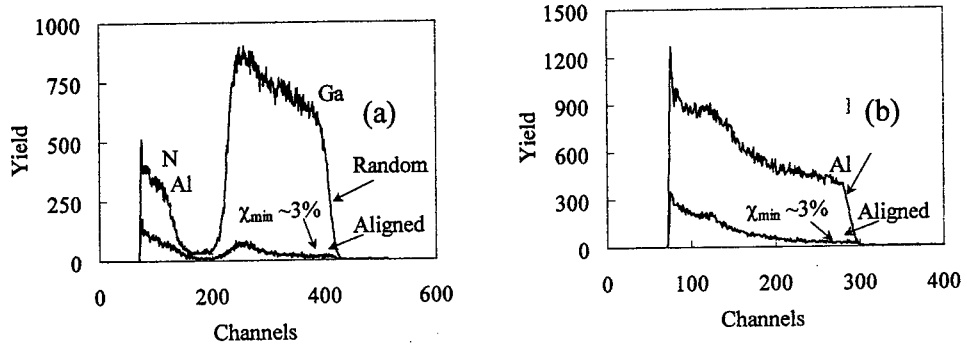

Figure 2. Random and aligned RBS spectra of epitaxial (a) AlN and (b) GaN thin films grown by PLD.

The AlGaN alloys were also fabricated successfully using PLD. In this case, computer-controlled automated multilayer deposition assembly (manufactured by Neocera, Inc.) was used in order to switch the targets periodically at the laser ablation sight. Prior to the growth of alloys, an individual deposition rate per pulse for GaN and AlN was determined. Using the predetermined growth rates, the number of pulses required to ablate GaN and AlN to form one monolayer of an alloy with given composition was calculated and used for the experiments, and each iteration was executed anywhere from 800 to 1000 times, depending on the desired thickness of the film. Figure 3 (i) and (ii) shows XRD patterns and UV-visible spectroscopy, respectively, for the AlN, GaN, and AlGaN alloys of varying composition. The alloys reported here had laser pulse ratio on GaN to AlN target of 10:20, 10:40, and 15:20, which produce alloys of $Ga_{0.45}Al_{0.55}N$ [curves (b)], $Ga_{0.6}Al_{0.4}N$ [curves (c)], and $Ga_{0.7}Al_{0.3}N$ [curve (d)], respectively. The XRD patterns and UV-Visible spectroscopy confirmed the formation of alloys. The films displayed ~ 70 to 80% optical transmission in the near-visible range. The E_g was determined by a linear fit of the square of the absorption coefficient, as a function of the $h\nu$ near the band edge. The results of composition versus E_g are shown in the inset of Fig. 3(ii).

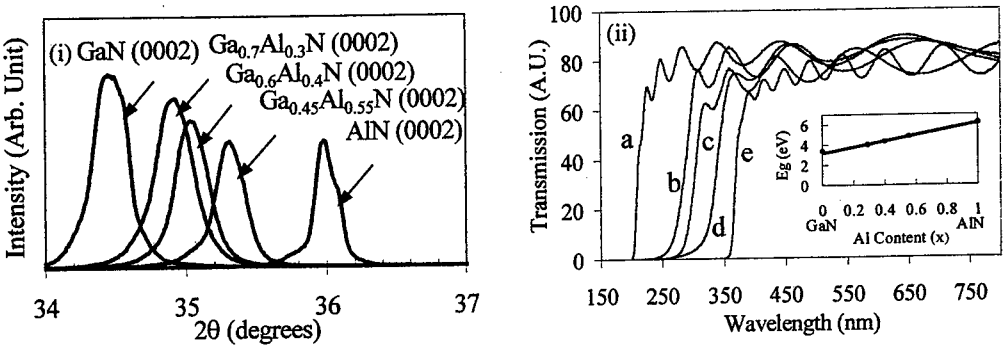

Figure 3. XRD (i) and UV-visible spectroscopy (ii) of PLD GaAlN alloys

AlN/SiC heterostructures and devices: Thin films of AlN seem to be promising as a dielectric, as compared to SiO_2 for metal-insulator-semiconductor (MIS) structures. The advantage of AN AlN/SiC materials system is the small lattice mismatch between AlN and SiC. Our major objective is to develop and fabricate thyristors based on SiC, with integration of other wide band gap materials suitable for high-temperature operation (300-500 °C). In this context, we have studied the suitability of the PLD technique for the fabrication of AlN thin films for encapsulation, passivation, and dielectrics on SiC.

Epitaxial TiN/AlN/SiC MIS capacitors with gate areas of $4x10^{-4}$ cm^2 were fabricated using PLD, and high-temperature current-voltage (*I-V*) characteristics were studied up to 450 °C. We measured leakage current densities of around 10^{-8} A/cm^2 at room temperature and of around 10^{-3} A/cm^2 at 450 °C under 2 MV/cm field, as shown in Fig. 4. Complete electrical characterization and analysis of the dielectric properties of the PLD AlN films is discussed in another submission to this conference [2].

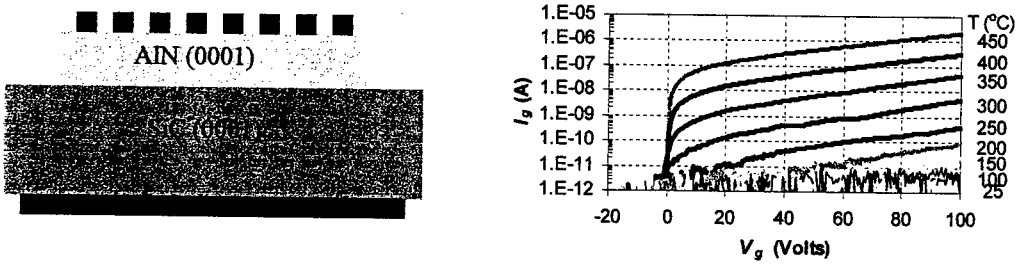

Figure 4. Schematics (left) and I-V characteristics (right) of PLD TiN/AlN/SiC MIS capacitors.

Conclusion: We show that high-quality thin films of AlN, GaN, and their alloys can be fabricated by PLD at substrate temperatures (750 to 850 °C) which are lower than those employed in (MOCVD) (1000 to 1100 °C), an alternative growth method. These films show a high degree of crystallinity and good optical properties. Epitaxial AlN thin films grown by PLD are shown to be excellent for dielectric application for SiC thyristors. PLD is also used successfully for epitaxial growth of AlGaN alloys and TiN ohmic contacts. Thus, the PLD technique producing optoelectronic-grade wide bandgap thin films and heterostructures can be useful for further studies, such as growth, doping, alloying, tailoring optoelectronic properties, and integration of WBG materials.

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Investigation into the Film Growth of AlN on SiC by Low Pressure Chemical Vapour Deposition

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Keywords: Chemical Vapor Deposition, Sublimation, Surface Etching

Abstract

Aluminium nitride layers were grown by Low Pressure Chemical Vapour Deposition on off-cut 6H-SiC and 4H-SiC substrates, implanted or with an epilayer. Samples were annealed at the temperature of 1600°C or 1650°C. Depending of annealing temperature and nature of the substrate, the AlN layers were partially removed and the SiC substrates etched. AlN layers and SiC surfaces were characterized by X-ray diffraction and Scanning Electron Microscopy before and after annealing.

Introduction

AlN has been considered to be a good alternative to silicon dioxide and to serve as a dielectric for a gate oxide in SiC MOS devices [1-3]. The interest for pursuing AlN arises from the close lattice match between AlN and SiC which is 1% in the (0001) plane and also from the compatibility of other material properties. In addition, an AlN film could be an effective diffusion barrier for an SiC wafer during substrate annealing and protects the SiC surface during the high temperatures (1400-1700°C) dopant activation step [4]. Jones et al. [5] proved that the performance of AlN used as an encapsulant is effective up to 1600°C for 15 min.
In this study, aluminium nitride layers deposited on SiC substrates by Low Pressure Chemical Vapour Deposition (LPCVD) are characterized. The annealing effects on the surface morphology and the structure of AlN layers and SiC substrates are also investigated.

Experimental procedure

Table 1 describes the investigated samples and their preparations. The substrates used were 4° off-axis toward <11-20> 6H-SiC and 4H-SiC crystals manufactured by Cree Research Inc.. Two 6H-SiC crystals were implanted by aluminium (samples *I* and *III*). Two epilayers on a 6H-SiC (sample *II*) and a 4H-SiC crystals (sample *IV*). were also utilized. Before deposition, the substrates were annealed at 850°C under hydrogen to remove oxides. Aluminium nitride depositions were carried out using a vertically configurated, cold wall, low pressure chemical vapour deposition reactor. Precursors for the growth were ammonia (NH_3), hydrogen (H_2) and aluminium chlorides formed in situ by the reaction of chlorine on aluminium chips. Argon was used as a carrier gas. The samples were quickly heated (ramp time around 5 minutes) to the growth temperature of 850 °C. Pressure was fixed to a value lower than 10 torr.

Sample	Substrate	Implantation and epitaxy	AlN deposition	Annealing temperature
I	6H-SiC	Al implanted 2200Å	10 min, 532 Pa	1650 °C
II	6H-SiC	6H epilayer		1650 °C
III	6H-SiC	Al implanted 2200Å		1600 °C
IV	4H-SiC	4H epilayer		1600 °C

Table 1: Samples and experimental procedures.

The experimental parameters, gas flow rates, temperature (800 or 850°C), pressure (532 to 1330 Pa) and deposition time from 10 to 40 min were investigated on different Si and SiC substrates to optimize the process. The optimal deposition time and pressure were found to be 10 min and 532 Pa, respectively.
SEM was employed to evaluate the morphology of the samples. The thickness was determined using SEM and FTIR spectroscopy. Structures were characterized by X-ray diffraction techniques. Composition measurements were obtained by electron microprobe analysis. Annealings were carried out in a resistive furnace at 1600°C or 1650°C under an argon atmospheric pressure for 5 minutes.

Sample characterisation

The as-deposited layers are optically homogeneous with a 0.5 µm layer thickness. Chlorine content is below 1 %. The surfaces, observed by SEM, are very smooth and homogeneous.

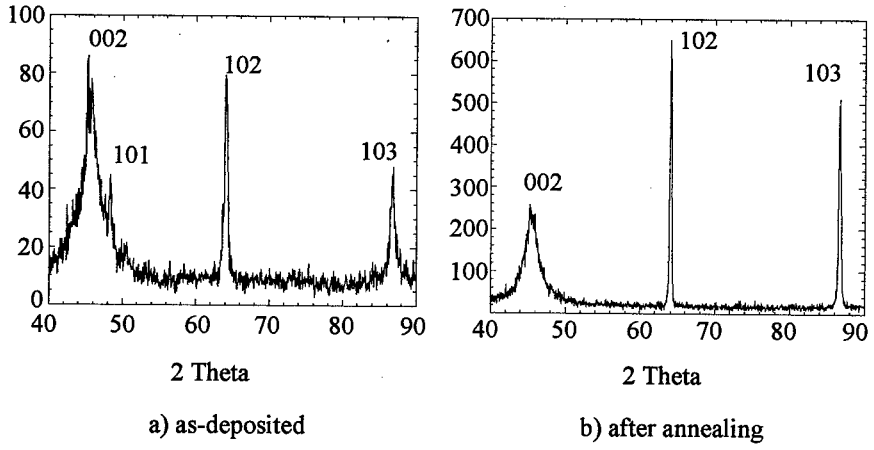
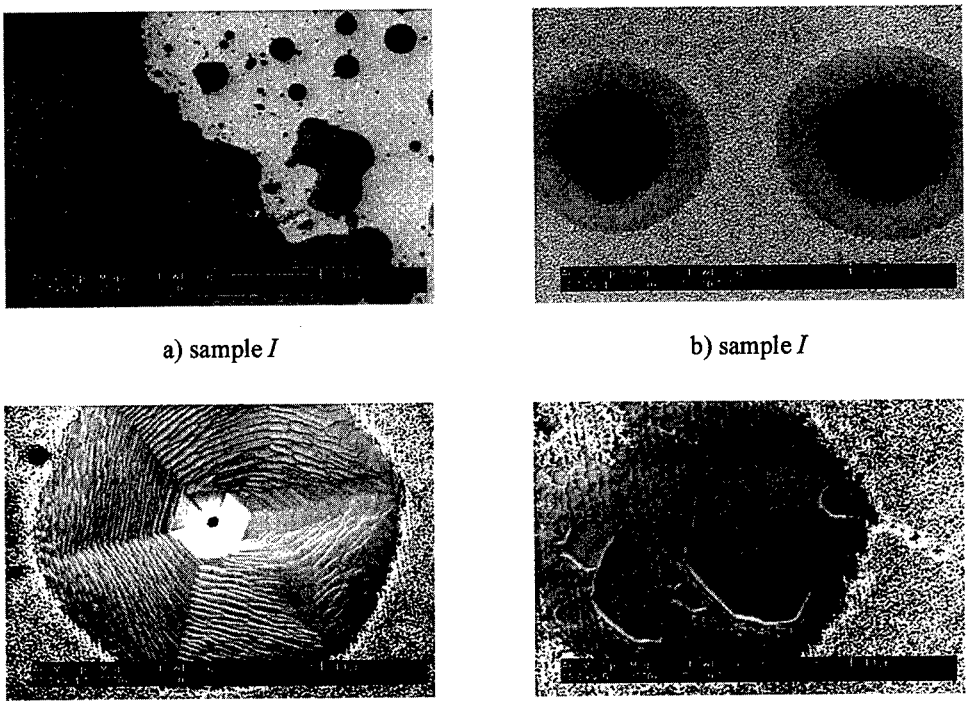


Fig. 1: Sample *III* θ-2θ X-ray diffraction spectra before and after annealing (KαFe)

Fig. 1a shows a θ-2θ X-ray diffraction spectrum of an as-deposited AlN film. The 101, 102 and 103 reflections are narrow and the 002 reflection is very large. The 100 and 110 reflections are not observed as it would be for a perfect powder. It means that the layer is

textured but it is not an epilayer. It was not possible to complete the analysis of the 002 reflection with a 4° off-axis diffraction vector because of the presence of a strong SiC peak. After annealing , it has been shown with optical microscopy that the AlN layer on the sample *II* had vanished. On the samples *I* and *IV*, the layer was partially removed (~80 % remained) whereas the film on the sample *III* seems to be homogeneous. The X-ray diffraction spectrum of the sample *III* (Fig. 1b) shows that its texture has not changed. The 102 and 103 reflections became higher and narrower which corresponds to a well crystallised layer. The X-ray diffraction spectra of the samples *I* and *IV* show non identified reflections in addition to the AlN-related peaks.



a) sample *I* b) sample *I*

c) sample *IV* d) sample *IV*

Figure 2: SEM micrographs after annealing

Fig. 2 shows several SEM images of the annealed samples *I* and *IV*. In the sample *I*, AlN layer (white area on Fig. 2a) presents a granular surface but is partially removed near the sample border (grey area). In this region, AlN film was sublimated and the substrate was etched. Fig. 2b shows regular shaped holes in the SiC substrate with an approximately 3 μm depth. The etching figures are hexagonal craters with small steps on the edge. The bottom, flat and inclined toward [110] direction is probably the (001) face. Similar holes have been observed in sample *IV* , some of these exhibit etching figures of micropipes as shown on figure 2c. When the AlN layer is entirely removed, the SiC surface is step etched (Fig. 2d). Similar observations are found for the sample *II* . The AlN film of sample *III* is granular without any degradation of the film and substrate (similar to the white area on Fig2).

Summary and Discussion

AlN thin films have been deposited by LPCVD starting from $AlCl_3$, NH_3 and H_2 films on two types of SiC substrates, implanted and with a SiC epilayer. They are highly textured but do not form perfect epilayers. The systems layer/substrate were annealed at 1600°C and 1650°C during 5 minutes, under argon atmosphere. For both temperatures, it was found that the AlN/epilayers SiC samples are degraded and much more etched than the other samples.
The temperature of 1600°C appears to be the limit for the use of AlN films as an encapsulant in order to avoid a degradation of the SiC substrates or epilayers during post implantation annealing. This temperature limit seems to be related to the thermal decomposition and sublimation of AlN in the tested annealing conditions.
An atmosphere of nitrogen during annealing may be a possible solution to increase this temperature limit to a value suitable for a perfect activation of the dopants.

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AlN Epitaxial Films Grown by ECR Plasma Assisted Metalorganic Chemical Vapor Deposition under Controlled Plasma Conditions in Afterglow Region

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Keywords: AlN, Electron Cyclotron Resonance Plasma, Epitaxial Growth, Mirror Field, MOCVD

Abstract: Wurtzite-type aluminum nitride (w-AlN) films were epitaxially grown on sapphire substrates by electron-cyclotron-resonance plasma assisted metalorganic chemical vapor deposition (ECRMOCVD) using trimethylalminum (TMA) and ammonia (NH_3) as source gases under a mirror field condition in a growth chamber. Under small gas feed ratios of N source to Al source (NH_3/TMA) at epitaxial growth process, the proportion of non-epitaxial domains became large. In order to obtain AlN epitaxial films having excellent crystallinity and surface morphology on c-plane of sapphire substrates, thermal nitridation, the growth of buffer layer around 600°C prior to the epitaxial growth, and the epitaxial growth under high NH_3/TMA gas feed ratios were required.

1. INTRODUCTION

W-AlN is a wide band-gap semiconductor (Eg=6.2eV at 300 K), and is considered to be a very promising opto-electronic material for applications such as light-emitting diodes and lasers in the deep ultraviolet region [1, 2]. By alloying AlN with GaN, which has a complete solid solubility, it is possible to tune the energy gap between 3.39 and 6.2 eV [3]. AlN is a good candidate for the insulated gate of GaN devices due to its high thermal conductivity (2W/cmK), electrical insulation and heat-resistant properties [4]. AlN is also used as a buffer layer for the GaN based lasers fabricated on sapphire substrate [5]. Therefore, the detailed investigation of epitaxial growth of AlN on sapphire is very important subject even now. Nitridation process of substrate surface [6], low temperature growth of buffer layer [7] prior to the epitaxial growth have been reported to play important roles in improving the crystallinity and the surface morphology of AlN epitaxial films.

The experimental conditions of nitridation, buffer layer growth, and epitaxial layer growth can be widely varied by using ECRMOCVD method, because stable nitrogen source gases such as N_2 and NH_3 are able to be easily decomposed at low temperatures [8]. The ECRMOCVD method using NH_3 also has some effects on the improvement of crystallinity and morphology and on the relaxation of stress by reactive species such as hydrogen radicals. In the present study, w-AlN was grown on sapphire substrates in an afterglow plasma region of ECR plasma controlled by a magnetic coil around the growth chamber. In addition to the study on the epitaxial growth conditions, the investigations about the influence of surface nitridation and buffer layer growth on the film properties were carried out. Nitridation process was carried out using both thermal and plasma energies.

2. EXPERIMENTAL

The ECR plasma CVD apparatus used in this study is comprised of an ECR plasma chamber, a growth chamber, a microwave circuit, a gas supplying system and an evacuating system. In addition to the two magnetic coils around the plasma chamber for the ECR field, a magnetic sub-coil was wrapped around the growth chamber. Details concerning the structure of the apparatus used in the present study have been reported in a previous paper [9]. The magnetic field gradient

from the plasma chamber to the growth chamber was controlled by the current flow in the sub-coil. The mirror and cusp fields were obtained by the sub-coil current flows in the same ($I_{sc}>0$) and opposite ($I_{sc}<0$) directions to the magnetic coils of the ECR field.

Variations in space potential and floating potential at 10 mm from the substrate surface in the growth chamber as a function of the sub-coil currents measured by a Langmuir probe were measured [9]. Under positive sub-coil currents, the space potential and floating potential decreased. Under low plasma space potential, the degradation of the crystal structure of the epitaxial films is believed to be suppressed, due to the depression of the impingement of positive ions with high energy. Therefore, the plasma nitridation, the growth of low-temperature buffer layer and the epitaxial growth were performed under a mirror field condition (I_{sc}=40 A).

Figure 1 shows the time chart of AlN growth process. AlN growth was carried out via the following five processes. (a) Sapphire substrates were thermally cleaned in H_2 gas flow at 1050°C for 10 min (t_{TC}). (b) The substrate surface was nitrided with NH_3 gas at 1050°C for 10 min (t_N). In addition to thermal nitridation, plasma nitridation was also carried out at the same substrate temperature. (c) A low-temperature (LT) buffer layer was grown using V/III ratio of 520 at various substrate temperatures (t_{LTG}). (d) The nitridation layer and LT buffer layer were annealed at 1150°C for 30 min in an atmosphere of NH_3 gas (t_{AN}). (e) AlN epitaxial films were grown at 1150°C using various V/III ratios (t_G). The growth conditions of w-AlN are as follows: substrate sapphire (0001), background pressure $1x10^{-6}$ Torr, pressure during the whole process 2mTorr, NH_3 gas flow rate 15 sccm, incident microwave power 340 W. The obtained AlN films were characterized by an atomic force microscopy (Digital Instruments, NanoScope III) and by an X-ray diffractometer (Rigaku, RAD-IIIA).

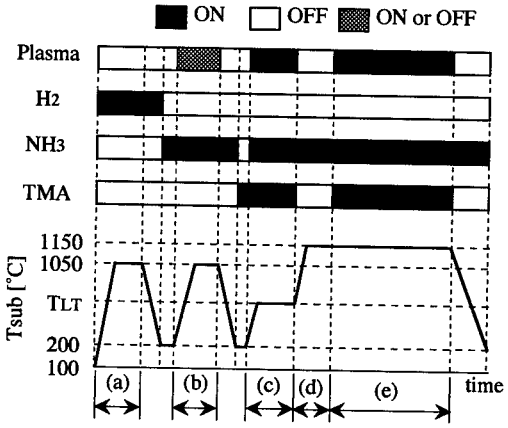


Fig. 1 Time chart of the growth process. The growth temperature of LT buffer layers was extensively varied in the experiment.

3. RESULTS AND DISCUSSION

The crystallinity of w-AlN films and their crystal orientation were improved by the nitridation prior to the film growth. Figure 2 shows the X-ray diffraction spectra of AlN epitaxial films grown after various nitridation processes. The diffraction peaks from (10-10) and (10-11) planes, together with large peak from (0002), were observed for AlN film grown without nitridation in the measurement of θ-2θ scan, as shown in Fig. 2. The appearance of the (10-10) and (10-11) diffraction peaks indicates the existence of the domains whose c-axis is parallel to the substrate surface and those including stacking faults. In contrast, only a diffraction peak from the (0002) basal plane was observed for the AlN film grown after thermal or plasma nitridation. From the values of full

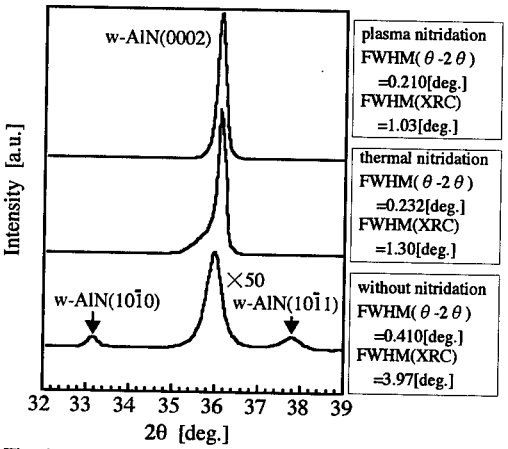
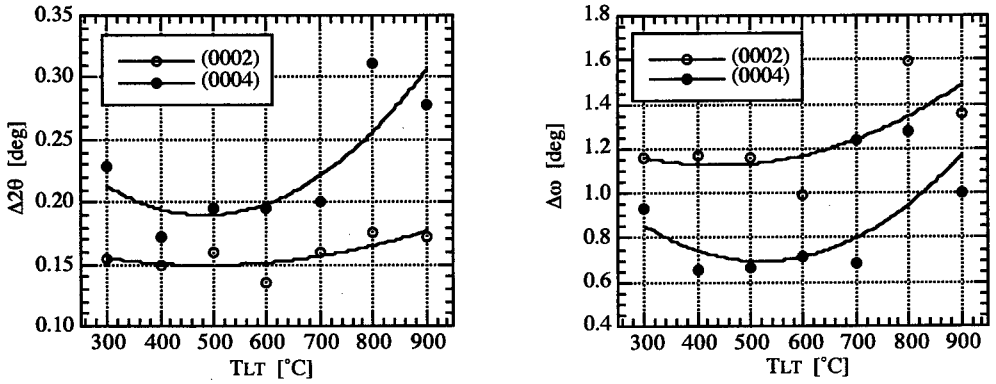


Fig. 2 X-ray diffraction spectra of AlN films grown after various nitridation processes.

width at half maximum (FWHM) of θ-2θ scan and ω-rocking curve, which are somewhat poor values compared to the other report [10], AlN films having better crystallinity and crystal orientation were found to be grown after thermal or plasma nitridation.

Figure 3 shows the dependence of the FWHM values of (0002) and (0004) diffraction peaks of θ-2θ scan and of ω-rocking curve on the growth temperature of LT buffer layer. Growth conditions except for the buffer layer growth such as nitridation, annealing, and the epitaxial growth were the same. From the figure, the growth around 600°C was best for the growth of AlN with excellent crystallinity and crystal orientation. When the temperature of LT buffer layer growth is lower than 400°C, the integrated diffraction intensity ratio between (0002) and (10-10)+(10-11) of buffer layer, ($I_{0002}/[I_{10\text{-}10}+I_{10\text{-}11}]$), became on the order of 10. This implies that the non-epitaxial domains increased up to a few tens percent by the lowering of the growth temperature. The crystal orientation of these domains could not be restored during the annealing process. In case of the buffer layer growth at around 600°C, on the other hand, the integrated diffraction intensity ratio became larger than 10^3. The non-epitaxial domains further decreased when LT buffer layer was grown at higher temperatures (>700°C). However, AlN layer grown just on the nitridation layer at high temperatures is considered to be constituted of mosaic-like crystal domains having small variations of crystal orientation. Therefore, the FWHM values of X-ray diffraction spectra of AlN epitaxial films on the buffer layer grown at high temperatures became large due to some scattering of crystal orientation.



(a) θ-2θ scan (b) ω-rocking curve

Fig. 3 Dependence of the FWHM values of X-ray diffraction peak of θ-2θ scan and of ω-rocking curve on the growth temperature of LT buffer layer.

The non-epitaxial domains became large, when V /III (NH_3/TMA) gas feed ratio at the epitaxial growth was lower, as shown in Fig. 4. Therefore, the growth of non-epitaxial domains is considered to be enhanced by the excessive supply of TMA. The plasma nitridation, growth of LT buffer layer at around 600°C, thermal annealing and the epitaxial growth with high V/III ratio were the best process to reduce the non-epitaxial domains and to improve the crystallinity and crystal orientation of AlN films. Using LPMOCVD growth without ECR plasma, the non-epitaxial domains became large compared to those grown with ECR plasma at the same V/III ratio.

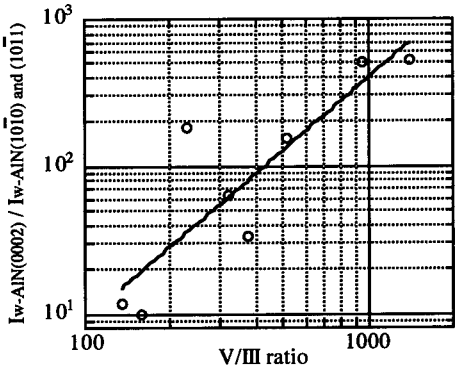
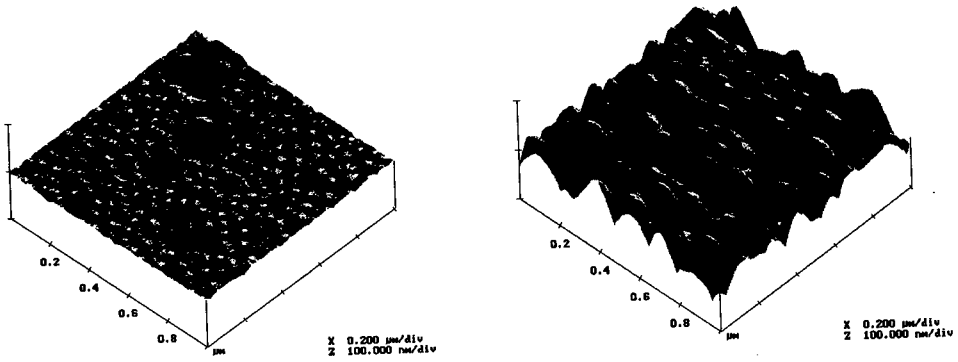


Fig. 4 Dependence of the ratios of integrated diffraction intensity $I(0002) / [I(10\bar{1}0)+I(10\bar{1}1)]$ of w-AlN films on the gas feed ratio NH3/TMA

From the results of the comparison between plasma nitridation and thermal nitridation, nitridation process influences not only on the crystallinity of w-AlN epitaxial films but also on morphology of them. Two-dimensional (2D) growth was enhanced when AlN was grown on sapphire substrate after thermal nitridation processes, as shown in Fig. 5. On the other hand, the crystallization was drastically enhanced when AlN was grown after plasma nitridation process mentioned above. However, three-dimensional (3D) island growth was enhanced by plasma nitridation.



(a) 1×1μm (Ra=2.832nm) (b) 1×1μm (Ra=12.062nm)

Fig. 5 AFM images of AlN films grown on Al2O3. (a) thermal nitridation (b) plasma nitridation before AlN film growth. V/Ⅲ=520 during LT buffer layer growth, V/Ⅲ=320 during epitaxial growth.

4. CONCLUSION

W-AlN films were epitaxially grown on sapphire substrates by ECRMOCVD method using TMA and NH_3 as source gases under a mirror field condition. Nitridation using NH_3 plasma prior to the epitaxial growth improved the crystallinity of AlN films. The growth of buffer layer at about 600°C and thermal annealing at high temperature was more favorable for the growth of AlN epitaxial films with excellent crystallinity and crystal orientation. Under large gas feed ratio (NH_3/TMA) at epitaxial growth process, the proportion of the non-epitaxial domains decreased. In order to obtain the AlN epitaxial films with excellent crystallinity and surface morphology, thermal nitridation, the growth of buffer layer at about 600°C prior to the epitaxial growth, and the epitaxial growth under high NH_3/TMA gas feed ratio were required.

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Silicon Carbide Substrates for Epitaxial Growth of Aluminium Nitride by Chloride-Transport Process

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Keywords: Chloride-Transport Process, Defect Formation, Nitrided Stainless Steel, Sublimation Growth

Abstract: SiC wafers are used as substrates for III-V nitrides growth. 6H- and 4H-SiC boules were grown by the Modified Lely method elaborated at the St.-Petersburg Electrotechnical University. Formation of stress and misoriented areas in SiC crystals has been investigated. The chloride-transport process was employed for the growth of AlN on SiC substrates using an open (p=1 atm) horizontal silica multichannel reactor. High-perfect single crystalline AlN layers were deposited at the growth temperatures above 1150 C and growth rate about 0.1...0.5 μm/min. Single crystalline layers of AlN on large SiC substrates with misoriented areas have been successfully obtained.

Introduction

SiC wafers are used as substrates for III-V nitrides growth. Silicon carbide has the basal plane lattice constant closest to that of AlN and should be considered as the best substrate material. Because of thermal and lattice mismatches between sapphire and AlN more higher than SiC and AlN, it is necessary to grow a thick epitaxial layer to obtain reasonable quality material. One of the problems to obtain high quality SiC wafers is the presence of slightly misoriented (less than 1 degree) comparatively large areas in the silicon carbide boules which can limit operation of the devices based upon such material. The aim of the present work is to investigate influence of misoriented areas in SiC substrates on epitaxial growth of aluminium nitride layers.

Experiments and Results.

The silicon carbide basically oriented substrate of 6H, 4H polytypes as well as (10.0) cut of 6H-SiC polytype with diameter 25 - 50 mm were used for epitaxial nitride growth. The 6H- and 4H-SiC crystals 25-50 mm in diameter were grown by sublimation method elaborated at the St.-Petersburg Electrotechnical University [1, 2,]. Samples have been investigated using X-ray diffractometry and X-ray topography (Berg-Barrett and Lang methods) for observation of misoriented areas in the wafers. Etching in molten KOH was employed for selective etching and revealing of dislocations including those that are forming low angle boundaries of the misoriented areas.

The influence of the growth conditions and crystal enlargement on the formation of misoriented areas and dislocations has been investigated. The main reasons of the misoriented areas formation are: reproduction of such areas from the substrate and formation of the misoriented areas under enlargement of crystal when growth of marginal areas occurs over polycrystalline material grown

on graphite. Additional reason is stress formed in the marginal areas due to the nonuniform distribution of temperature in the boule.

Reproduction of misoriented areas from the substrate. In all cases we observed reproduction of the misoriented areas from the substrate to the growing crystal. But depending on growth conditions the structure of the substrate can be completely reproduced in the crystal or the misorientation of the areas can be diminished. For diminishing the formation of misoriented areas we used growth in the conditions when the growth rate was limited by diffusion mass transfer from source material to substrate. For this purpose we used growth at higher temperature and under higher inert gas pressure. At the same time in the case that the misorientation of the areas in substrate is higher than several angle minutes it is hard to avoid reproduction of such defect in the overgrown crystal.

The results obtained gave a possibility to diminish formation of misoriented areas in SiC crystals. X-ray topography image of a 40 mm in diameter 6H-SiC substrate sliced along (0001) plane from the boule is shown in Fig. 1. Formation of misoriented areas was prevented for crystals with

Fig.1 X-ray Berg-Barrett topography of SiC substrate.

diameters up to 30 mm. For crystals 30-50 mm in diameter misoriented areas in the peripheral parts of the boule were observed. For most cases misorientation did not exceed 1' and several angle minutes for crystals up to 35 mm and 35-50 mm in diameter, respectively.

These SiC wafers were used for epitaxial nitride growth. The first stage of pre-growth substrate treatment consisted on high-temperature annealing – etching in hydrogen in order to reduce deep damage and remove defect material from the surface. The next stage was necessary to smooth the surface relief after the hydrogen treatment, by polishing in liquid etching.

The chloride-transport process was employed for the growth of AlN using an open (p=1 atm) horizontal silica multichannel reactor [3,4]. The precursors were Al, HCl and NH_3. Ultra-pure argon was used as a carrier gas. Chlorination of metallic aluminium by gaseous HCl was carried out directly in separate reactor channel as the first stage of the epitaxial process.

Optimum CVD reactor design should meet two requirements:
(i) requirement of layer uniformity, both axial and lateral one;
(ii) minimum gas residence times to achieve sufficient interface abruptness.

As known, aluminum nitride chemical vapor deposition by chloride hydride technique in hot-wall reactor is frequently accompanied by homogeneous chemical reaction of AlN formation in gas phase volume. This process can be observed visually as milk-colored regions in gas usually near the walls and was employed by us as natural visualization in order to study an effect of basic technique parameters such as gas injection technique, mass flow rates, temperature profile etc. on flow patterns.

Axial uniformity is affected by a number of factors primarily by gas flow reagent exhaustion due to both homogeneous and heterogeneous chemical reactions of AlN synthesis and, probably, irreversible destruction of ammonia. Homogeneous reaction can lead to rapid depletion of gas mixture. In addition, growing particles can fall onto the substrate and can be captured by the epitaxial layer.

Quasi steady-state aerosol structure was observed for relatively low temperatures (about 800°C on the wall). Temperature enhancement causes turbulation and partial destruction of aerosol pattern. For higher temperatures (above 950°C) one can see that the space aerosol region in gas flow is separated from the walls by a thin dark region. Because the high linear gas flow velocities were used (30..150 cm per sec) the temperatures on the reactor walls are much more than ones of gas flow nucleus thus leading to great cross-cut temperature gradients. As a result, "homogeneous" particles are removed from the walls due to thermophoretic phenomenon. Thickness of dark region being arised is of some millimeters varying as a function of the growth temperature and gas flow velocity. Therefore, inclusion of particles into the epitaxial layer can be prevented provided high gas velocities and undeveloped structure of temperature profile of gas flow.

Aerosol intensity may be minimized on the whole reducing either $NH_3/AlCl_3$ partial pressure ratio or growth temperature. At the same time temperature decreasing is undesirable because high growth temperatures (> 1150°C) are necessary to achieve an acceptable structural perfection of AlN epitaxial layers.

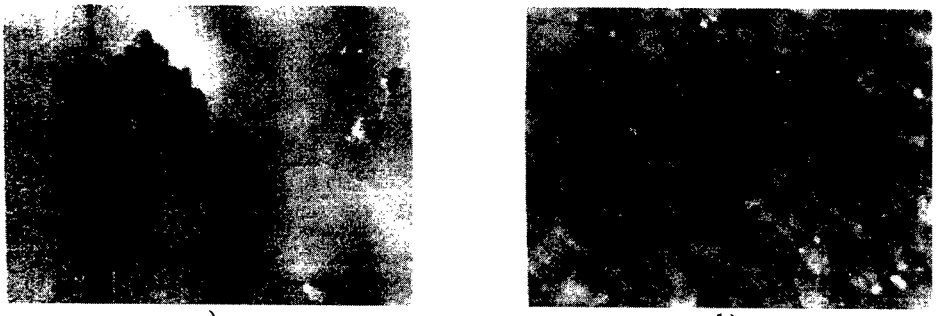
To clear effects of homogeneous reactions and ammonia dissociation powder products condensed onto reactor walls near an outlet of reactor have been studied by X-ray diffraction techniques. Ammonia chloride was identified always even if very small gas velocities and ammonia partial pressures were used being indicative of that the ammonia destruction in gas phase is impeded kinetically although resolved thermodynamically and an effect of ammonia destruction in gas flow on axial fall of growth rate downstream the reactor is negligible. Aluminum oxynitride was also detected.

Lateral uniformity is determined mainly by the method of gas reagent injection into the growth chamber. Various nozzle injection techniques for NH_3 and $AlCl_3$ have been tested. Nevertheless, the best results, i.e. improved area uniformity and structural perfection of epitaxial layers were obtained only when chlorides and ammonia were mixed in the special reactor chamber at 773 – 1073 K. The higher mixing temperature caused an intensive depletion of reaction flow because of nitride deposition immediately in the mixing chamber; lower temperatures led to condensation of by - products such as $AlCl_3 \cdot NH_3$ etc. Finally, homogeneous gaseous flow of $AlCl_3$ and NH_3 was introduced into the epitaxial growth reactor chamber via quasi porous plug injector.

To minimize gas residence times any laminar vortices should be eliminated. Natural convection vortices were observed in gas space and were strongly pronounced for larger values $Sp = Gr/Re^2$ where Gr – Grashof number, Re – Reynolds, Sp – Sparrow number. Such a flow is not uniform,

and the gas residence time is increased. At the same time increasing the gas flow velocity was rather uneffective because led to increasing not only Re but partly also Gr. The contribution of thermal convection was suppressed mainly by decreasing the height of growth chamber down to 8..10 mm and also by advanced construction of the injector arranged at the inlet of the growth chamber.

AlN layers were grown at 1173 – 1473 K. Typical values for growth rate and thickness were 0.1...1.0 μm/min and 1...10 μm, correspondingly. High-perfect single crystalline AlN layers were deposited at the growth temperatures above 1150 C and growth rate about 0.1...0.5 μm/min (Fig.2a). The lower growth temperatures led to considerable deterioration of structures perfection caused by arising misoriented crystallites, the surface morphology being clearly defined by a number of great hillocks (Fig.2b).



a) b)

Fig.2. AlN layers on silicon carbide substrates: a) 15R-SiC substrate, T=1100°C, growth rate of 0.37 μm/min, X 6000; b) 6H-SiC substrate, T=1000°C, growth rate of 0.46 μm/min, X 6000.

AlN epitaxial layers have wurtzite structure whatever substrate polytype and polarity were used. Layers with thickness of more than 2...3 μm as a rule tend to numerous cracking or even peeling off. Deposition of fibre texture AlN layers can be achieved at the considerably lower temperatures, no more than 950 C, the X-ray full width at half-maximum (FWHM) being about 1...2 ° (Cu K_α radiation, 0002AlN). Smooth texture layers of AlN were obtained on all substrates used including (10.0) 6H-SiC cut. Microcracking and sometimes peeling of AlN layers were typical features for silicon carbide substrates of (0001) orientation but never observed for single crystalline or texture AlN grown on (10.0) silicon carbide. Misoriented areas in the substrates have no any considerable effect on crystal perfection of AlN epitaxial layers.

Conclusion

Thus, high-perfect single crystalline layers of AlN on large SiC substrates have been successfully obtained. Silicon carbide wafer with misoriented areas of several angle minutes have not essential influence on quality of aluminum nitride epi-layers.

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Low-Energy-Ion-Assisted Reactive Sputter Deposition of Epitaxial AlN Thin Films on 6H-SiC

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Keywords: 6H-SiC, AlN, Cathodoluminescence, Epitaxial, Sputtering, TEM, XRD

Abstract

Epitaxial wurzite-structure AlN thin films have been grown on 6H-SiC substrates by ultra-high-vacuum (UHV) low-energy-ion-assisted reactive dc magnetron sputtering. The quality of epitaxial AlN films is significantly improved by low-energy ion assistance (E_i = 17-27 eV), during reactive magnetron sputter growth on vicinal (3.5 °) 6H-SiC. The ion-assisted growth results in an increased surface mobility, which promotes domain boundary annihilation and epitaxial growth. This results in lateral expansion of column width. Thus, AlN films with domains as large as 40 nm at the interface to 6H-SiC can be realized. At film thickness above 100 nm, the column width expands to 100 nm. The crystal quality of the films is very good with low background impurities (O: 3.5x10 ^{18}cm^{-3}).

The wide-band gap wurtzite aluminum nitride (AlN) is an important candidate material for many electronic applications, for example as dielectric in SiC-based device technology and as cathode material in field emission devices .[1] AlN is also used as a buffer layer for GaN epitaxial growth.[2,3] However, the use of AlN as a semiconductor or dielectric is hindered by the difficulties preparing high-quality material. The most common structural defects in state-of-the-art epitaxial AlN films are domain boundaries, which often are attributed to unit cell mismatch at substrate steps .[4] Furthermore, it is difficult to achieve low background impurity concentration. In this work, we show that the quality of epitaxial AlN films is significantly improved by low-energy-ion-assisted (17-27 eV) reactive magnetron sputter growth on 6H-SiC substrates in ultra-high-vacuum (UHV).

The AlN films were grown on quarters of 35 mm-diameter vicinal (3.5 °) 6H-SiC (0001) research grade wafers from CREE Research Inc. The substrates were prepared by a chemical cleaning procedure with a subsequent annealing in hydrogen atmosphere before transfer into the UHV sputtering system with a background pressure below 5x10 $^{-9}$ Torr. Subsequently, the substrates were heated to the growth temperature of 1000 °C. Prior to growth, an *in-situ* reflection high-energy electron diffraction (RHEED) pattern of a $(\sqrt{3} \times \sqrt{3})$R30 reconstructed surface was obtained, known to represent a clean and smooth surface of 6H-SiC with step heights of one unit cell. [5] A 75mm-diameter aluminum disk (99.999% pure) was used as a sputtering target in an atmosphere of purified nitrogen gas (99.999999%) kept at 10 mTorr. Ion-assisted growth was achieved by applying a constant negative substrate bias, V_S, to extract ions from the nearby plasma, during the growth. The maximum energy of arriving ions to the growing film, E_i , is given by the difference between V_S and the plasma potential, V_P ($|E_i| = |V_S - V_P|$ eV).[6] From plasma probe

measurements, the plasma potential at the substrate was determined to be 2 V and the substrate floating potential was –8 V. The ion-to- AlN arrival rate ratio was calculated to be 4 ions/molecule. A deposition rate of 0.05 nm/s was obtained, as measured from the films that were grown with incident ion energy, E_i = 2 eV.

The microstructure of the AlN films and the AlN/6H-SiC interfaces were studied using cross-sectional high-resolution transmission electron microscopy (HREM) in a Philips CM 20UT electron microscope. Films grown to thicknesses between 100-200 nm exhibited a reduced density of domains as well as an increased rate of annihilation of the domains when using E_i in the range of 17-27 eV. This is demonstrated in Fig. 1(a) and (b) where the micrographs are taken from samples which were grown at E_i = 2 eV and 27 eV, respectively. For AlN films grown with E_i = 2 eV, an abrupt interface was obtained between the AlN and the 6H-SiC substrate. This AlN film has a columnar-like structure with a narrow column width of approximately 2-4 nm at their bases.[7] This can be expected from kinetically limited growth of AlN due to low surface mobility at the used growth temperature of 1000°C.

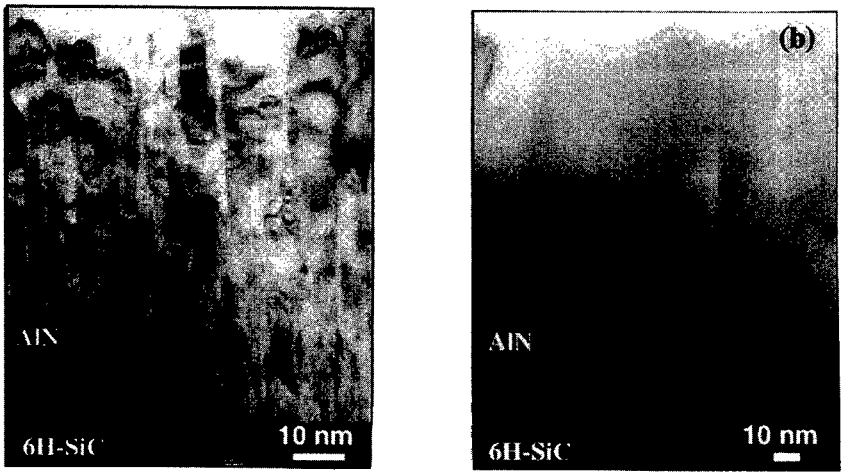

Fig. 1. (a) Cross-sectional TEM of AlN thin film, grown with E_i = 2 eV and **(b)** using a low ion-assistance of E_i = 27 eV, respectively. Please notice that these images are not of the same magnification.

The AlN film grown with low-energy ion assistance, however, shows an increased domain size (see Fig. 1(b)). The appearance of columnar domain boundaries was observed at the first few nanometers from the interface. The domain width increased from 38-42 nm near the interface, to 75-135 nm at 100 nm film thickness. Domain boundary annihilation during the growth has thus resulted in a significant expansion of AlN domain width compared to films which were grown at E_i = 2 eV. This indicates that low-energy ions enhanced adatom mobility, which suppress the domain formation and promote domain boundary annihilation. However, large facets at the surface of the films can also be seen in Fig.1(b) as a further evidence of this effect. Increasing E_i >52 eV yielded initial growth of amorphous AlN with a thickness of a few nanometers and a sharp interface to SiC. Subsequently a continuous microstructure evolution to polycrystalline structure was observed. This result can be expected for ion bombardment during film growth with

energies sufficient for re-sputtering and displacive collisions of atoms such that re-nucleation may take place.[8]

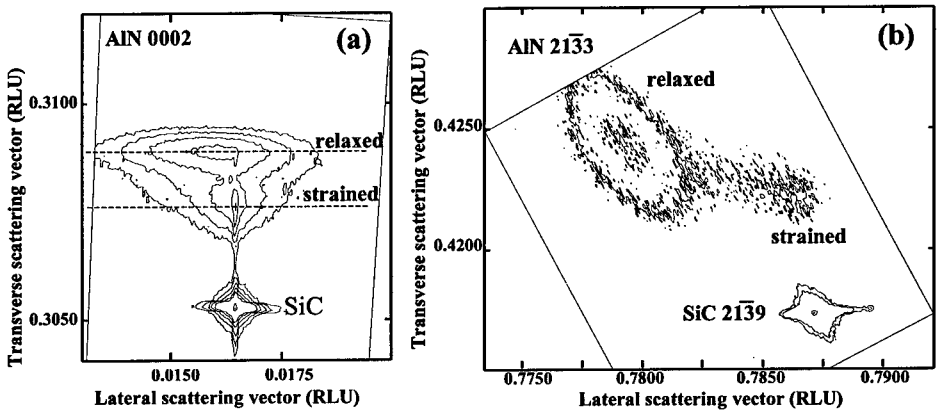

Fig. 2. (a) The 0002 and **(b)** 21$\bar{3}$3 reciprocal space maps (RSM) of an 200-nm-thick AlN film, grown at E_i = 17 eV , shows the strained epitaxial layer and the relaxed layer of the AlN film on 6H-SiC substrate.

Reciprocal space mapping (RSM) was performed by using high-resolution x-ray diffraction (HRXRD) in a Philips X'pert MRD. As shown in Fig.2 (a) and (b), the RSMs of an 200-nm-thick AlN film grown at E_i = 17 eV showed that a domain of strained layer epitaxial AlN was formed together with a relaxed domain when the low-energy ions were used. The in-plane lattice mismatch of the strained AlN with respect to the lattice parameters of 6H-SiC substrate,[9] was 0.3% (relaxed lattice mismatch = 0.9%) and the FWHM of the HRXRD 0002 rocking curve was 60 arcsec indicating a very high structural order in that domain (the FWHM of the relaxed domain was 1800 arcsec). Using higher ion energy than 17 eV, the films were faulted fully relaxed.

Atomic force microscopy (AFM), using a Digital Instrument Nanoscope IIIa was used to characterize the surface morphology of the films. The root-mean-square (RMS) surface roughness was found to increase abruptly from 1.3 to 8.7 nm when the ion energy was increased from 2 to 17 eV and then drop continuously to 2.1 nm as the energy was increased further. Simultaneously, the surface feature size followed the same trend in agreement with the HREM results.

The use of UHV conditions, very pure target and sputtering gas is to keep the impurity concentration levels of the films as low as possible. The results from the secondary ion mass spectroscope (SIMS) have showed that 1000 °C is the optimum growth temperature for our system.[7] The concentration levels of Si, C and O in the AlN films were $1x10^{17}$, $1.3x10^{18}$ and $3.5x10^{18}$ cm^{-3}, respectively, as measured by a CAMECA IMS6F instrument.

The quality of the AlN material is also reflected in strong near-band edge emissions in cathodoluminescence (CL) spectra, which were obtained using an Oxford Research Instrument CL system. In Fig.3, the CL spectra obtained at different temperatures are shown. Two strong peaks of near-band edge emissions can be observed at 6.02 eV and 5.85 eV at 4.7 K. The peak at 5.85 eV disappears as the temperature is increased above 100 K.

As the temperature is increased further, the peak at 6.02 eV shifts to 5.96 eV. These peaks have previously been observed in material grown by metal organic chemical vapor deposition (MOCVD).[10] Although their origin are still not clear, their appearance is taken to indicate a high semiconductor quality AlN material. The peaks at 4.77 eV and 3.76 eV have been reported as defect related peaks in the material ,[10, 11] which corresponds to the result from SIMS.

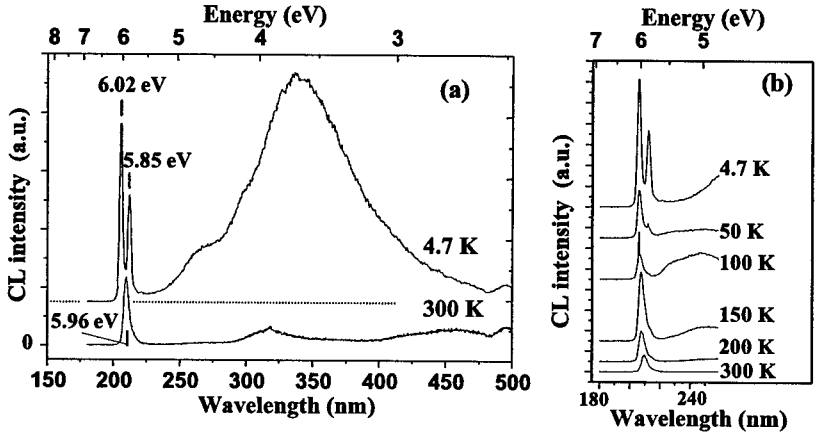

Fig. 3 (a) CL spectra from AlN film on 6H-SiC, grown with low-energy ion assistance (E_i=17 eV) shows 2 near-band edge emissions at 4.7 K and **(b)** the temperature dependent of the emission peak at 5.85 eV (at 4.7 K).

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Pulsed Laser Deposition of Oriented Aluminum Nitride Thin Films and Their Application

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Keywords: Optical Wave Guide, Pulsed Laser Deposition, Surface Acoustic Waves

Abstract. Pulsed laser deposition was applied to prepare aluminum nitride films of up to 1250 nm thickness onto c- or r- cut sapphire substrates with (00.1) or (11.0) orientation, respectively. X-ray diffraction goniometry revealed a preferential in-plane alignment of the AlN crystals. First experiments on several potential applications are presented where orientation dependent properties of AlN are significant. A r.f. delay line based on surface acoustic waves in AlN(11.0) generated along the AlN c-axis was fabricated. Silicon carbide films were grown on AlN predeposited sapphire substrates. Optical wave guiding was demonstrated in an AlN film.

Introduction

Aluminum nitride in the wurtzite crystal structure is a material of great technological interest due to its exceptional properties. Most of the research on AlN film deposition is focussed on AlN(00.1). In general, however, crystals may be oriented in any arbitrary direction in space. For films the variety of crystal orientations is limited by the differences in growth rate and reactivity of the crystal faces. Here, we concentrate on two special cases of AlN orientation. The first one is AlN(00.1) with its c-axis perpendicular to the surface, the second one is AlN(11.0) with its c-axis parallel to the surface.
Due to the wurtzite crystal structure the AlN(00.1) film surface exhibits a sixfold rotational symmetry resulting in isotropic elastic, piezoelectric and optical properties for all directions parallel to the surface. The AlN(11.0) surface symmetry includes two perpendicular mirror planes. On the film surface the elastic, piezoelectric and optical properties are dependent on the direction. The optical axis of the positive uni-axial AlN crystal is parallel to the surface resulting in anisotropic light propagation (birefringence) in the film.
AlN with its high sound velocities of up to 6000 m/s is a potential material for surface acoustic wave (SAW) applications [1]. The orientation dependent elastic properties of the surface are relevant for instance for the excitation of SAW by interdigital transducers. AlN might serve as substrate for epitaxial growth of SiC since it has similar lattice constants and crystal symmetries as the hexagonal polytypes of silicon carbide (SiC). The orientation dependent symmetry and surface energy may influence the growth mode and crystal orientation of the epilayer. For optical applications, AlN seems to be interesting because of its large band gap of 6.2 eV [2] and high nonlinearities [3,4]. For thin films a standard optical device is a waveguide.

Experimental

The films were prepared in a standard PLD system which was previously described [5]. A KrF excimer laser (Lambda Physik 315i, 248 nm, 25 ns, 50 Hz) with 150 - 250 mJ pulse energy was focussed (approx. 2 J/cm^2) onto rotating targets in a stainless steel vacuum chamber with 10^{-6} mbar

base pressure. The AlN films were deposited on sapphire substrates in 2×10^{-5} mbar ammonia (NH_3) from a sintered AlN target whereas SiC films were deposited in high vacuum from a polycrystalline SiC sinter target on AlN predeposited sapphire. The substrates were placed 5 cm in front of the target. A substrate temperature of 800°C was measured by a pyrometer. Deposition rates of approximately 50 nm/min for AlN and 30 nm/min for SiC were achieved.
The crystallographic orientation of the films was determined by X-ray diffraction with a *Philips X'Pert* diffractometer equipped with an Eulerian cradle using Cu-K_α line radiation. The film thickness was measured by a profilomter (*Tencor P-10*).
SAW device fabrication and electrical measurements were performed at the *Paul-Drude-Institute Berlin*. Interdigital transducers (IDT) were prepared by a photolithographic process. 700 aluminum finger pairs of 0.7 µm width and 60 nm thickness were assembled in a split finger configuration for the IDTs. The periodicity of the finger pairs of 5.6 µm is equivalent to the wavelength of the acoustic waves excited in the IDT's resonance. A transmission electron microscope (*JEOL* 300 keV) was applied to investigate cross-section samples (at the *University of Jena*). Optical properties of the AlN films were investigated by UV-VIS absorption spectroscopy (*AVIV 14DS*) and spectral ellipsometry (*Sentech SE 800*). Optical wave guiding in AlN was demonstrated by m-line spectroscopy at the *Fraunhofer Institut für Optik und Feinmechanik Jena.*

Results

The orientation of the AlN films depends on the sapphire substrate cut as previously examined in detail [6]. On c-cut sapphire AlN(00.1) film growth is observed with an in-plane alignment of $AlN[2\bar{1}\bar{1}0]\|Al_2O_3[10\bar{1}0]$. Due to a very pronouced columnar growth of the AlN film in the (00.1) direction the film surface appears relatively rough. For 1000 nm thick AlN films a r.m.s. roughness of more than 10 nm was determined. On r-cut sapphire AlN films grow in (11.0) orientation. The in-plane alignment is $AlN[0001]\|Al_2O_3[0\bar{1}11]$. For this AlN orientation very smooth films with a r.m.s. roughness of 1.2 nm were grown up to a thickness of 1250 nm.

Surface Acoustic Wave Application. A rf delay line was fabricated from a 1200 nm thick AlN(11.0) film on r-cut sapphire. The interdigital structures on top of the AlN film were aligned in such a way that the direction of surface acoustic wave generation coincided with the c-axis direction AlN[0001] of the film. The surface acoustic waves are excited only due to the piezoelectricity of the AlN film since sapphire is not piezoelectric. Films as AlN(11.0) with its c-axis parallel to the film surface are beneficial for SAW excitation by planar IDT configurations since the piezoelectricity of AlN is highest in c-axis direction. The electrical transfer function of a r.f. delay line based on the described configuration is shown in fig. 1.

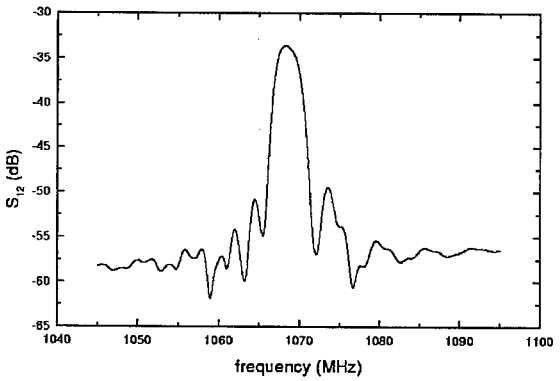

Figure 1:
Response function of a r.f. delay line based on SAW in AlN.
The centre frequency of the pass-band is 1.068 GHz.

The centre frequency is 1.068 GHz. The low peak transmission is due to limitations of the lithographic process on the small sample and misoriented AlN crystallites. From the centre frequency and the periodicity of the interdigital transducers a phase velocity of 5980 m/s is derived for the surface acoustic wave. This value agrees well with results of other groups [7]. For the bare substrate the velocity of the generalized Rayleigh wave in this direction is 6087 m/s [8], thus the AlN film appears to decrease the velocity in addition to providing the electro-mechanical coupling. However, deviations in the orientation of the propagation direction, that lead to a reduction of the substrate velocity, can not be excluded and have to be further investigated.

Application as Substrate for Silicon Carbide Deposition. AlN(00.1) and AlN(11.0) films were used as substrate for silicon carbide deposition. Due to the different surface properties and crystal orientations of the AlN films there is a distinct variation of SiC film properties. On AlN(00.1) the silicon carbide surface appears rough whereas on AlN(11.0) the SiC is smooth. For both substrate orientations the SiC films are polycrystalline with some degree of preferential orientation according to selective area electron diffraction patterns. The exact crystallographic alignment, especially of SiC grains close to the SiC/AlN interface need more detailed investigations.

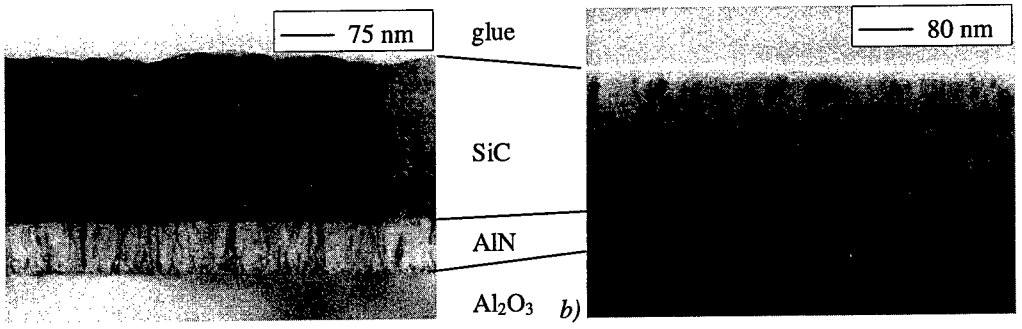

Figure 2: TEM cross section micrographs of 60 nm AlN and 200 nm SiC on sapphire substrates. The films were simultaneously deposited.
a) SiC on AlN(00.1) on c-cut sapphire b) SiC on AlN(11.0) on r-cut sapphire

Optical Characterization and Application. The AlN film are transparent with only interference fringes visible at the film edges due to inhomogeneities in thickness. There is no significant variation of the optical transparency with the AlN crystal orientation. The band gap of 5.8 eV (213 nm) was determined by UV-VIS absorption spectroscopy. It appears to be slightly smaller than the commonly referred AlN band gap of 6.2 eV [2]. The reason for this difference is not yet fully understood, it might be explained by strain in the crystals. Spectral ellipsometry in the wavelength range of 250 nm to 800 nm was performed to investigate the optical properties of AlN more thoroughly. For wavelengths larger than 300 nm the absorption of AlN was below the detection limit of k = 0.001. The dispersion relation of AlN was determined according to Cauchy's formula.

$$n^2(\lambda) = 4.046 + \frac{3.1 \cdot 10^4\ \mathrm{nm}^2}{\lambda^2} + \frac{2.8 \cdot 10^9\ \mathrm{nm}^4}{\lambda^4}$$

Since the refractive index of AlN is larger than that of sapphire the AlN films may serve as optical wave guide with internal total reflection. In a 1250 nm thick AlN(11.0) film on r-cut sapphire optical wave guiding was investigated by m-line spectroscopy with a He-Ne laser (632.8 nm).

	$TE_{\parallel}$	$TM_{\parallel}$	$TE_{\perp}$	$TM_{\perp}$
n_0	2.0591	2.0670	2.0926	2.0774
n_1	2.0194	2.0262	2.0528	2.0355
n_2	1.9539	1.9590	1.9907	1.9667
n_3	1.8623	1.8600	1.8996	1.8719
n_4	1.7530	1.7550	1.7785	1.7685
n_f	2.072	2.080	2.1052	2.0907
t_f	1226 nm	1265 nm	1231 nm	1264 nm

Table 1:
Refractive indices n_i of the five guided modes in a AlN(11.0) wave guide on r-sapphire (n=1,753) at 632.8 nm
TE, TM: transversal electrical or transversal magnetic polarisation
$\parallel, \perp$: direction of light propagation with respect to the optical axis of AlN
n_f, t_f: refractive index and thickness of the AlN film

Five guided modes were detected parallel and perpendicular to the optical axis (c-axis). The birefringent effect in the positive uni-axial AlN can be seen from the high refractive indices of the $TE_{\perp}$ mode (extraordinary refractive index) in comparison to the other states of polarisation and propagation direction. The propagation losses of the laser light in the wave guide are rather high with approximately 10 dB/cm. This might be due to scattering and absorption at grain boundaries of AlN crystallites. For experiments to investigate the nonlinear optical properties the propagation losses in the wave guide need to be reduced.

Summary and Concluding Remarks

It was shown that pulsed laser deposition is a capable technique to prepare AlN thin films of distinct orientation. Especially AlN(11.0) were found to be beneficial for SAW excitation by planar IDT structures and deposition of smooth SiC films. Furthermore, optical wave guiding in an AlN(11.0) was demonstrated. The birefringence effect in AlN was observed in the optical wave guide.

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State of Art of c-BN Growth Physics: Substrate Effect

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Keywords: c-BN Phase Control, Choice of Substrate, Heteroepitaxy

Abstract Modern growth techniques are currently carried out to elaborate the cubic phase of BN films. However, c-BN growth optimization is still a question under debate. Up to now a variety of substrates has been tested and an optimized choice still remain to be found. In this work, we discuss the existing data on c-BN content in BN films in function of substrate hardness and film/substrate lattice parameter mismatch and we identify, within the framework of the elasticity theory, an elastic constant-related material feature which enlightens substrate effects in c-BN growth processes.

Introduction

Boron Nitride can form different crystalline structures showing quite different material properties: an hexagonal sp^2-bonded phase (h-BN), a cubic sp^3-bonded phase (c-BN), a wurtzitic sp^3-bonded phase (w-BN) and a rhomboedric sp^2-bonded phase (r-BN). c-BN has many excellent properties, e.g. extreme hardness, high thermal conductivity, high electrical insulation, chemical stability and excellent semiconductor properties (wide band gap III-V semiconductor). It is transparent from near ultraviolet to infrared and it can be easily n and p type doped. c-BN is very attractive for thin film applications such as cutting tools, acousto-opto-electronic devices, high power and high temperature electronic applications. Although Physical Vapor Deposition (PVD) methods [1] can produce BN films that consist almost entirely of c-BN, an obstacle for these applications is cracking and loss of adhesion of deposited c-BN films and their high level of stress. Recent works [2] seem to resolve this difficulty by using high deposition temperatures ($T \cong 1000°C$) which disqualify a lot of substrates. Consequently, a better understanding of growth and nucleation mechanisms of c-BN, including substrate influence, needs to be developed.

The deposition conditions necessary for c-BN growth are well known. First, it needs a sufficient temperature, a reliable control of N/B stoechiometry and an important ion bombardement. Last results indicate that c-BN growth needs less ion energy than c-BN nucleation [3]. In ref. [4] it has been established that the momentum transferred into the growing film by the bombarding ions is the single parameter which controls the formation of c-BN. This demonstrates that ion bombardement during film growth is a critical parameter in forming c-BN thin films. Several models try to describe ion-induced formation of c-BN, such as sputter model [5], thermal spike model [6], stress model [7] and subplantation model [8]. However, none of these models give a comprehensive representation of c-BN formation. Especially substrate effects, which have been analyzed in ref. [9] in terms of substrate hardness and which are not included in these models, show the trend that more harder is the substrate much higher is the film c-BN content.

The microstructure of BN films, observed by a number of group using different growth techniques, always consists of a succession of a-BN, h-BN and c-BN layers. The intermediate a-BN and h-BN layers generally affect the quality of the BN-film/substrate interface. The aim of this work is to reach a better understanding of substrate influence on c-BN content in BN films and then to use this parameter to improve the film/substrate interface quality. In what follows, we present the

state of art of c-BN films elaborated on several substrates and we discuss the results in function of substrate hardness, lattice mismatch and substrate elastic constants.

Effect of substrate hardness

Although most of c-BN film growth is made on silicon substrates, several other substrates have been already used. The literature indicates that high c-BN fraction (>85 %) is obtained on hard substrates like diamond [10,11], 3c-SiC [9], Si [3] whereas generally medium and low c-BN fraction is obtained on soft substrates like metallic (20 to 70 %) substrates (Ni, Cu, Al) [11,12] and ionic- bonded (10%) substrates (KBr, KI) [10]. As we will see, the results show the tendency that the leading parameters for c-BN formation may be physical properties of the substrate and his surface , like hardness [12] and roughness [10] rather than lattice parameter matching between c-BN and substrates. As for example, c-BN content on Si and 3c-SiC substrates (up to 90%) are higher than on Cu substrate (≈ 60%) while Cu lattice mismatch is 0.05 %, lower than Si (40 %) and 3c-SiC (18 %).

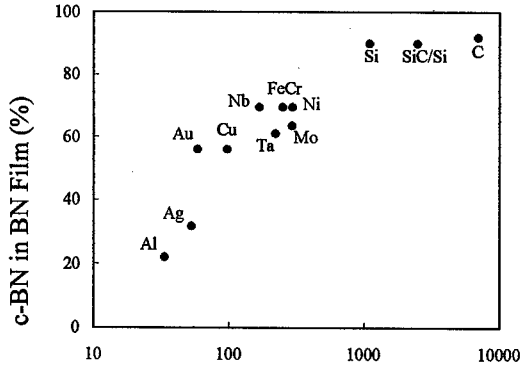

Fig. 1 c-BN content vs substrate hardness

On Fig.1 we represent the variation of c-BN content in BN films grown on different substrates in function of measured substrate hardness, where metallic or ionic or covalent/ionic bonds contribute to the substrate lattice stability. This illustration of substrate effect, widely cited in the literature, shows the trend towards an increase of c-BN content when substrate hardness increases. The position of the point corresponding to C (harder than c-BN) substrate shows that substrate hardness effect does not tell us the whole story because of the saturation effect in c-BN content for three substrates, namely Si, SiC/Si and C characterized by very different hardness.

Effect of substrate misfit

Let us now discuss the effect of standard lattice parameter mismatch f on c-BN composition. f may be defined by the following equation:

$$f=2(a_F-a_S)/(a_F+a_S) \qquad (1)$$

where a_S and a_F are respectively the lattice parameters of substrate and film. Except for Si substrate and to a certain extent for SiC, the tendency is that c-BN content increases when f decreases. The misfit corresponding to Si is in fact half way between ionic (KBr, KI) and metallic (Al, Ag, Au, Mo..) substrates whereas Si, as a substrate, gives a high c-BN content. With C and Si substrates, we have two opposite configurations: low positive misfit for C (substrate in extension) and high negative misfit for Si (substrate in compression), whereas c-BN contents are rather similar.

Effect of substrate effective elastic constants

When lattice parameter mismatch between overlayer and substrate host materials exists, interface strains are created. For overlayer thickness beyond the critical thickness, interface dislocations can become more favored from the viewpoint of defect energy formation. By a mechanism similar to that leading to phase transformations under the effect of hydrostatic pressure, epitaxial strains created by constraining a material lattice to match the lattice of a substrate material can induce phase transformations. A theory based on total energy calculations [13] of solids and using second order continuum elasticity theory [14] has clearly demonstrated the occurrence of epitaxy-induced phase transformations: energy reduction due to overgrowth lattice relaxation in the growth direction is calculated using elestic constants. This is to say that elastic constants and related

material features must play a vital role in epitaxy-induced processes as we demonstrate that the variation of c-BN content in BN films grown on different substrates can be understood on the basis of elasticity theory. Let us then consider the equations of the elasticity theory [14] which relate strain to lattice dynamics features, as we have for cubic crystals:

$$\frac{\partial^2 u}{\partial t^2} = \frac{C_{11}}{\rho}\frac{\partial e_{xx}}{\partial x} + \frac{C_{12}}{\rho}\left(\frac{\partial e_{yy}}{\partial x} + \frac{\partial e_{zz}}{\partial x}\right) + \frac{C_{44}}{\rho}\left(\frac{\partial e_{xy}}{\partial y} + \frac{\partial e_{zx}}{\partial z}\right) \qquad (2)$$

where u is the x component of the displacement, ρ is the density, the C_{ij} are the elastic constants, and the $e_{\sigma\sigma'}$ are the strain components ($\sigma,\sigma'=x,y,z$). Similar equations for y and z directions can be deduced from Eqn. 2. The left hand side of this equation is proportional to ω^2, the square of the angular frequency ω. Because of this feature, these equations may be considered as the signatures of a strain-dynamics correlation via an elastic constants factor $f(C_{ij})$ which represents a linear combination of elastic constants. For each interface configuration, i.e. for a specific growth plane, the dynamics equations involve effective elastic constants $f(C_{ij})$. In cubic crystals, $f(C_{ij})$ are given below respectively for the [100], [110] and [111] principal directions [14]:

$f(C_{ij})=C_{11}$ (a), $f(C_{ij})=C_{11}+C_{12}+2C_{44}$ (b), $f(C_{ij})=C_{11}+2C_{12}+4C_{44}$ (c) (3)

The elasticity theory has been successfully applied to several heterosystems to investigate heterointerface optimization and results related to IV-IV, III-V, II-VI and IV-VI-materials-based heterointerfaces have been already published [15-18].

We have calculated for several substrates used to grow BN films the value of the ratio $R=[f(Cij)]_{c\text{-}BN}/[f(C_{ij})]_{substrate}$. The results of c-BN content in BN film are depicted on Fig. 2 in function of the average of R for the directions [100], [110] and [111]. These results demonstrate that the c-BN content in BN films increases when R decreases: high values of R means that the effective elastic constants of the substrate are lower than c-BN ones while low values of R correspond to substrates characterized by effective elastic constants comparable to c-BN ones. Among all considered substrates, only Si and Nb show a deviation. The issue of such a finding is that we have now identified one material intrinsic feature which enables a straightforward representation of c-BN content data. This approach is complementary to the measured substrate hardness approach, although it only requires the knowledge of the elastic constants. The experimental conditions prevailing in the determination of elastic constants by methods based on the use of ultrasonic waves with wavelength of the order of $\sim 10^{-2}$ cm are such that a large part of the material is probed (non-local material features). One interesting implication of the previous analysis in terms of R is that we can predict, for a given substrate, the c-BN content of the deposited BN film. Such kind of information can be useful for growth process.

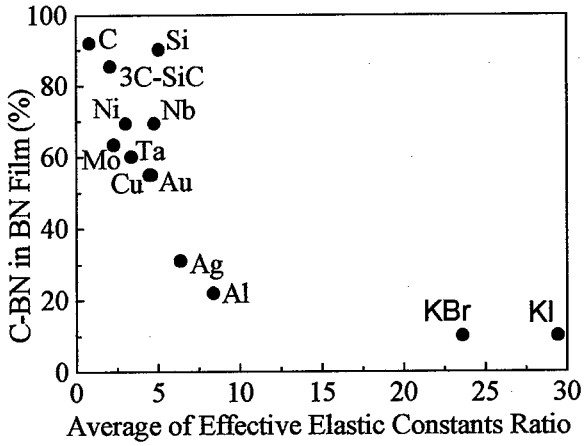

Fig. 2 Variation of c-BN content in function of R average

Conclusion

We discuss the state of art of c-BN growth on several substrates as regards to the variation of c-BN content in BN film in function of various substrate features as substrate hardness, lattice

parameter misfit and substrate effective elastic constants. For Si, 3c-SiC/Si and C substrates, Fig. 1 shows a saturation effect of c-BN content (~ 90%). This indicates that considerations only based on substrate hardness can not be the only comprehensive strategy for optimizing substrate choice. The effect of substrate lattice misfit f shows that when decreasing f, BN films with an increasing c-BN content can be elaborated. However, Si and 3c-SiC substrates do not follow this rule: BN films deposited on these two substrates (misfit respectively equal to 40 % and 18 %) contain a high percentage of c-BN phase. The strategy of optimizing substrate choice based on substrate misfit is not totally conclusive. Eventually, we demonstrate that an analysis in terms of substrate effective elastic constants gives a reliable approach to predict c-BN content, at least consistent with c-BN content data for metallic, ionic and covalent/ionic substrates. We have demonstrated the success of a strategy based on the elasticity theory for other compounds and results have been published elsewhere [15-18] (IV-IV, III-V, II-VI and IV-VI-materials-based heterointerfaces where the atomic density was included). But in the case of BN, only stress factors do matter.

Up to now, c-BN growth experiments do not show a successful evidence for the elaboration of c-BN films. The data shown in Figs. 1 and 2 demonstrate that the substrate choice is a vital key. A possible physical explanation for substrate influence on films c-BN content could be their property to absorb or reflect a part of the energy induced by ion bombardment. One objective of this work is to propose a strategy aiming at making such a choice. Within this strategy, we show that SiC may be a good substrate-candidate for growing c-BN and an optimized choice of a buffer layer still has to be made. This route is also widely investigated for other nitrides, e. g., GaN.

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Chapter 7

Physical Properties of III-Nitrides

Materials Science Forum Vols. 338-342 (2000) pp. 1533-1536

Adsorption and Desorption of Hydrogen on Ga-rich GaN(0001)

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Keywords: Deuterium, HREELS, TPD

Abstract

Hydrogen adsorption and desorption from GaN(0001) was studied using high resolution electron energy loss spectroscopy (HREELS), energy loss spectroscopy (ELS), low energy electron diffraction (LEED), Auger electron spectroscopy (AES), and temperature programmed desorption (TPD). HREELS loss peaks produced by atomic hydrogen were observed at 2580, 3280, and 3980 cm^{-1} and are attributed to Ga-H bonds. Heating the surface to 380°C completely removes the absorbate vibrational peaks. TPD confirms that the disappearance of Ga-H feature in HREEL spectra is due to recombinative desorption of hydrogen. Overall, this work demonstrates that the recombinative desorption of hydrogen from surface Ga sites occurs over the range of 250 to 500°C.

Introduction

A complete understanding of the growth process requires an understanding of relevant surface reactions. Previous research has shown that the reaction of hydrogen on the GaN surface alters growth and processing. Hydrogen affects growth rate and film quality both in MBE [1] and MOCVD [2,3]. Yu *et al.* reported that atomic hydrogen had an evident effect for GaN rich growth in MBE process. On the MOCVD growth side, Koleske *et al.* showed the GaN

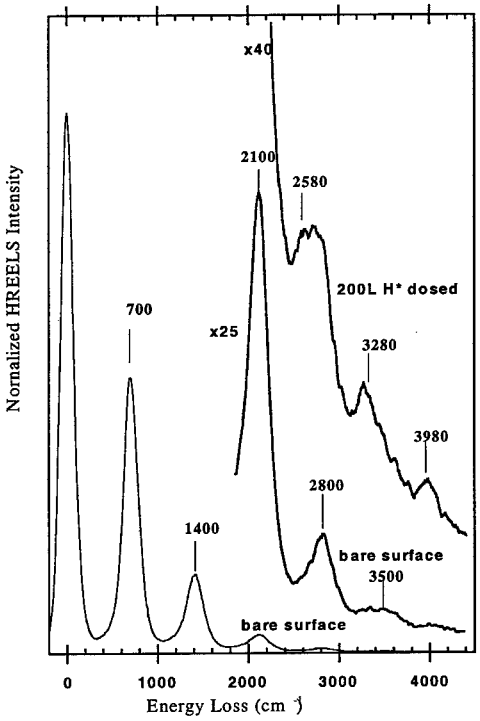

Figure 1. High Resolution Electron Energy Loss Spectra of sputtered and annealed surface and hydrogen saturated surface. The multiple loss of 700 cm^{-1} and peaks at 2580,3280,3980cm^{-1} are combination of Ga-H bonds plus FK phonon.

decomposition rate is accelerated as the hydrogen pressure increased above 100 Torr for temperature ranging from 850 - 1050 °C [3]. Han *et al.* reported that during the low temperature deposition of a GaN buffer layer the nuclei morphology evolution is strongly affected by H_2. Hydrogen has also been reported to affect doping efficiency and etch rates. Nakamura *et al.* conclude that the atomic hydrogen produced by NH_3 dissociation at 400 °C is related to the hole compensation mechanism [4]. A study by Pearton *et al.* showed that the etching rate is significantly faster when hydrogen is present in the etching chemistry [5].

Experiments

The GaN sample was grown by MOCVD at the Naval Research Laboratory and is 5 mm wide x 12 mm long [6]. The GaN film was grown on a-plane sapphire which was heated to 1180 °C for 10 minutes followed by the growth of a low temperature 250 Å thick AlN layer at 600 °C. The AlN layer was ramped under NH_3 to a temperature of 1040 °C for the growth of the GaN film. The GaN film was grown using TMGa and NH_3 with H_2 as a carrier gas. It is silicon doped with a carrier concentration of 2 x 10^{17} cm^{-3} and mobility of 400 cm^2/Vs. The polarity of the film is not known. The sample was rinsed by acetone then isopropyl alcohol before insertion into UHV. *In situ* cleaning was performed by sputtering with ~25 $\mu A/cm^2$ of 1 keV nitrogen ions for 5 minutes followed by annealing at 900 °C for 5 minutes.

Results and discussion

After sputtering and annealing, the LEED pattern shows a well-ordered but faceted surface and AES confirms surface cleanliness.

HREELS, a surface sensitive vibrational spectroscopy using low energy (6 eV) electrons, was used to characterize clean and hydrogen-exposed GaN(0001). The HREEL spectrum of the clean surface showed only the Fuchs-Kliewer (FK) phonon at a loss energy of 700 cm^{-1} and multiple losses at 1400, 2100, 2800, and 3500 cm^{-1} (Fig.1). HREELS shows that molecular hydrogen does not react with GaN(0001), but atomic H readily adsorbs [7,8,9]. Atomic hydrogen production was accomplished by passing molecular hydrogen over a W filament heated to 1500 °C. Following exposure of the clean GaN surface with H atoms, HREEL spectra show adsorbate loss peaks at 2580, 3280, and 3980 cm^{-1}

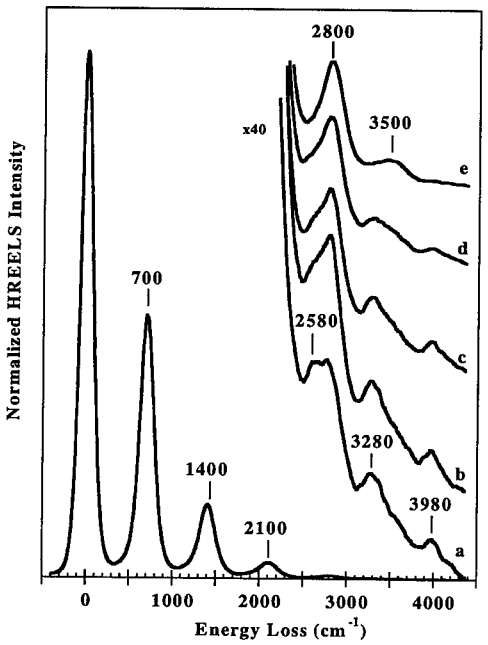

Figure 2. High resolution electron energy loss spectra of a) hydrogen-saturated GaN(0001) and following brief heating to b) 160 °C, c) 260 °C, d) 330 °C, and e) 380 °C. Peaked at 2580, 3280, and 3980 cm^{-1} are assigned to combinations of a Ga-H stretch and a one, two, and three Fuchs-Kliewer phonons, respectively.

(Fig. 1). These loss peaks reach maximum intensity after exposure to ~50 L of H_2 in the presence of a heated W filament, where 1 L = 1 x 10^{-6} Torr·sec. An exposure of 200 L was used in these experiments to assure maximum coverage was obtained and the surface treated in this way will be referred to as the hydrogen-saturated surface. In addition to loss peaks at 2580, 3280, and 3980 cm^{-1}, the Ga-H stretching vibration at 1880 cm^{-1} becomes evident when the HREEL spectrum is deconvoluted to remove the phonon multiple-loss peaks (not shown). Upon dosing with deuterium, the Ga-D bending mode is observed at 400 cm^{-1} but no vibrational peaks due to N-D surface species are observed. The Ga-D stretching vibration expected near 1350 cm^{-1} was not observed presumably due to interference from the second FK phonon peak at 1400 cm^{-1}. We therefore assign the 2580, 3280, and 3980 cm^{-1} peaks to combination modes of the Ga-H stretch and FK phonon(s) [7]. Since only Ga-H (Ga-D) and not N-H (N-D) vibrations are observed, we conclude that the surface is Ga-terminated.

To characterize hydrogen thermal desorption, vibrational spectra were acquired after briefly heating the hydrogen-saturated surface to 160 °C, 260 °C, 330 °C and 380 °C (Fig. 2). The sample was sputtered, annealed, and hydrogen-exposed before each desorption experiment. Heating to 160 °C produced no change in the HREEL spectrum. However, briefly heating to 260 °C caused a small decrease in the intensity of the Ga-H related peaks. Heating to 330 °C resulted in a much larger decrease in the intensity of the Ga-H vibrations and heating to 380 °C completely removed them as shown in Fig.2. We interpret these data to indicate that hydrogen desorbs from the surface beginning near 260 °C and occurs rapidly at a temperature of 380 °C.

To confirm the decrease of these peaks is due to desorption and not dissolution into the bulk, TPD experiments were also performed. In order to avoid the confounding effects of background hydrogen, deuterium (D_2) was used to model the surface interaction with hydrogen. The deuterium-saturated (200 L) surface was linearly heated from 150 °C to 600 °C with a uniform heating rate of 2 °C/sec and desorbed products were detected with the mass spectrometer. D_2 and HD were observed as desorption products. While the desorbing D_2 is due to recombination of surface D atoms, desorbing HD may result from either unintentional H atom exposure during D exposure from background H_2 or the recombination of subsurface H with surface D. Figure 3 shows the desorption curve

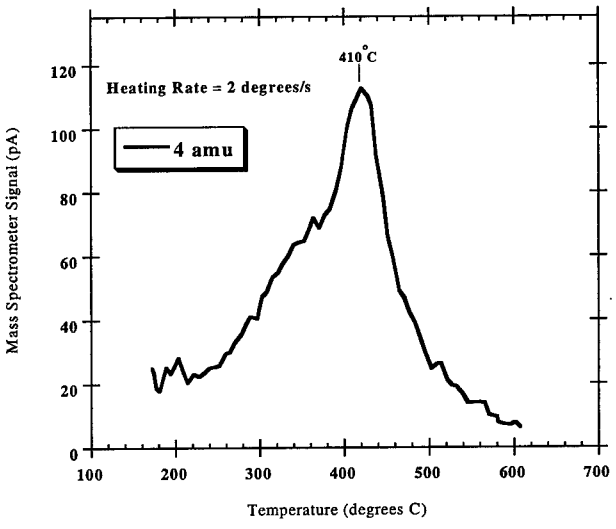

Figure 3 Temperature Programmed Desorption curve of D_2 from D-saturated GaN(0001). Surface was heated from 150°C to 600°C with uniform rate of 2°C/sec. The background was removed by linear fitting. Desorption starts from ~260°C to 500°C and peaked ~410°C.

for D_2 after removal of the background. A single desorption peak is observed showing thermal desorption of deuterium starting at ~250 °C and peaking at ~410 °C. No ND_x (x=1,2,3) signal was observed above the background over this temperature range. This range of desorption temperatures agrees with that observed for the disappearance of surface Ga-H as seen by HREELS This result confirms that the loss of surface hydrogen is due to recombination and desorption.

Sung *et al.* reported that N-H terminated GaN(000 $\bar{1}$) showed desorption of hydrogen-related species such as H_2, NH_2 beginning at about 850 °C [10]. In our experiment no N-H bond on the surfaces were detected and no N-H desorption were observed. Chiang *et al.* and Shekhar and Jensen have shown that hydrogen desorption from Ga-rich polycrystalline GaN and GaN(0001) occured around 300 °C [8, 9]. In both experiments, desorption from Ga-sites was suggested. Our work demonstrates that Ga-H surface species result from the reaction of GaN with hydrogen atoms and that Ga-H decomposes resulting in recombinative desorption of hydrogen between 250 to 500 °C.

Conclusion

Using HREELS we have shown that that hydrogen bonds only to Ga-sites and that the surface is Ga-terminated. We also observe that surface hydrogen is removed beginning near 260 °C and rapidly at a temperature of 380 °C. TPD shows that surface deuterium recombinatively desorbs between 250 to 500 °C. Therefore, we have demonstrated that surface hydrogen atoms recombine and desorb from Ga-sites on the GaN surface near 400 °C.

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Extremely Efficient Electron Stimulated Desorption of Hydrogen from GaN(0001)

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Keywords: Electron Energy Loss Spectroscopy, Electron Stimulated Desorption, Hydrogen

Abstract

Electron-stimulated desorption (ESD) of hydrogen from GaN(0001) has been observed and characterized using electron-energy-loss spectroscopy. Saturation exposure to atomic hydrogen produces a decrease in the intensity of energy loss peaks at 3.5 and 6.6 eV and an increase in the intensity of loss peaks at 11.7 and 18 eV. Bombardment with 90 eV electrons produces a reversal of the hydrogen-induced changes at 3.5, 6.6, and 11.7 eV. The increased intensity at 18 eV is almost unchanged by electron exposure. We conclude that the reversal of changes at 3.5, 6.6, and 11.7 eV is due to electron-stimulated desorption of hydrogen from Ga sites while the loss peak at 18 eV may be due to bulk hydrogen and not affected by 90 eV electrons. Cross sections for removal of H and D are found to be 2×10^{-17} and 7×10^{-18} cm^2, respectively. The large cross section and small isotope effect for ESD of hydrogen from GaN indicates the participation of a long-lived excited electronic state.

Introduction

To achieve high etch rates and anisotropy during etching of GaN, high temperatures, reactive chemicals, and/or high ion energies are required [1]. The use of electron or photon stimulated processes for etching may be one method to avoid the use of reactive chemicals, damage produced by high ion energies, and materials limitations imposed by high temperatures. For example, Gillis et al. have reported that GaN can be etched by low energy electron bombardment in an hydrogen atmosphere by a technique called low energy electron-enhanced etching (LE4) [2]. It is a low-damage dry etching technique which uses 1-15 eV electrons and a reactive species (H) to achieve etch rates of 200 Å/min, avoids ion beam damage and gives anisotropic pattern transfer. The mechanism of LE4 etching in an H plasma remains to be explained. Electron stimulated processing also has the advantage of being spatially selective making possible the production of patterned surfaces without masking. Electron beam patterning of hydrogen-saturated Si surfaces has been achieved without masking using a scanning tunneling microscope [3-5]. We have used high resolution electron energy loss spectroscopy (HREELS), energy loss spectroscopy (ELS), low energy electron diffraction (LEED), and Auger electron spectroscopy (AES) to examine the adsorption and electron stimulated desorption (ESD) of hydrogen on GaN(0001).

Results and Discussion

The GaN sample was grown by MOCVD at the Naval Research Laboratory on a-plane sapphire. It is silicon doped with a carrier concentration of 2×10^{17} cm^{-3} and mobility of 400 cm^2/Vs. In-situ cleaning was performed by a procedure of sputtering with 1 keV Nitrogen ions and annealing in UHV at 900 °C. LEED of the sputtered and annealed surface indicated a 1 x 1 surface structure with evidence of facetting. HREELS, which characterizes surface vibrations by measuring energy loss of scattered, low-energy (6 eV) electrons, was used to determine local bonding. We have recently reported the results of a HREELS study which shows that molecular hydrogen does not react with the GaN(0001) while atomic hydrogen exposure results in the formation of surface Ga-H [6]. No surface N-H was found and it was concluded the surface is Ga-terminated.

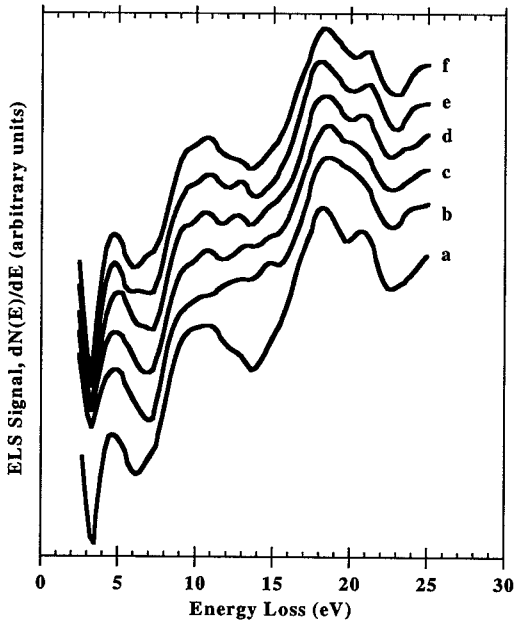

Fig. 1. First derivative electron energy loss spectra (dEN(E)/dE) of a) sputtered and annealed GaN(0001) and successive spectra of the H-saturated GaN(0001) following electron exposures of b) 0 electrons/cm^2 (0 min.), c) 1.9 x 10^{16} electrons/cm^2 (1 min.), d) 7.6 x 10^{16} electrons/cm^2 (4 min.), e) 1.5 x 10^{17} electrons/cm^2 (8 min.), and f) 3.8 x 10^{17} electrons/cm^2 (20 min.). In each case, the electron exposure and time given in parentheses correspond to the start of the spectrum.

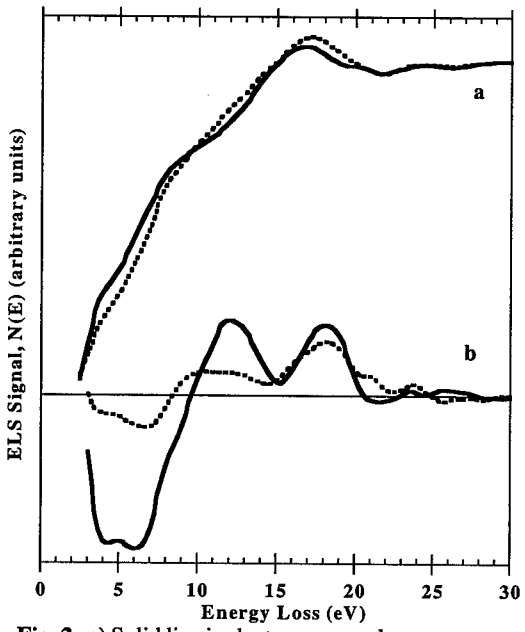

Fig. 2. a) Solid line is electron energy loss spectrum (N(E)) from clean GaN(0001) and the dotted line is the first spectrum following saturation hydrogen exposure (dotted line). b) Solid line is the difference between N(E) from the hydrogenated surface and N(E) from the clean surface. Dotted line is the difference between N(E) from the hydrogenated surface following 20 min. of electron exposure and N(E) from the clean surface.

ELS, which measures the energy loss of 90 eV electrons to electronic excitations of the surface, was used to characterize the electronic structure of both the clean and hydrogen-exposed GaN surface. After molecular hydrogen exposure, ELS shows no difference to that of the clean surface. In contrast, ELS following H atom exposure shows significant changes. Figure 1 shows the first-derivative ELS (d(EN(E))/dE) after sputtering and annealing, and after 200 L of H* exposure followed by various amounts of electron bombardment. For each spectrum, electron beam bombardment time and electron exposure at the beginning of each spectrum is given. The spectrum of the clean surface (Fig. 1a) is similar to previously reported clean GaN(0001)-(1x1) spectra [8,9,10]. There are considerable changes to clean surface following 200 L H* exposure as seen in Fig. 1b which have previously been described [9]. The double peak centered near 20 eV merges into a single peak and a leveling of the entire region from 9 to 15 eV is also seen, with an elimination of the peak between 9 and 11 eV and the dip between 13 and 15 eV.

With continued electron bombardment substantial changes to the H-saturated surface are observed. What is apparent is that most of the change in the ELS spectrum occurs within the first 8 min. of electron bombardment. After 20 min., the ELS spectrum appears similar to the one acquired from the clean surface. The broad single peak of the 0 minute spectrum centered near 20 eV emerges as a double peak following electron exposure. A reversal of leveling of the entire region from 9 to 15 eV is also seen, with a dip reappearing between 13 and 15 eV.

In order to understand and quantify the changes induced in the energy loss spectrum by electron exposure, we present N(E) spectra of the clean and hydrogenated GaN(0001). Figure 2a shows the N(E) energy loss spectra for the clean (solid line) and 200 L H* exposed (dotted line) GaN(0001). Figure 2b (solid line) is their difference, N(E) from the hydrogen-saturated surface minus N(E) from

the clean surface. From this difference we see that H adsorption produces a decrease in the intensity at 3.5 and 6.6 eV and an increase in the intensity at 11.7 and 18.1 eV. The loss peak at 3.5 eV has been assigned to the bandgap transition. H adsorption has been observed in photoemission to affect occupied states lying 1 and 6 eV below the valence band maximum [7,8]. We believe the energy loss peaks at 6.6 and 11.7 eV are transitions from these filled states to an empty state ~ 2 eV above the conduction band minimum[9]. Since HREELS of H/GaN(0001) showed that only Ga-H species were produced by H exposure[6], the hydrogen-induced changes in ELS were attributed to formation of Ga-H [9].

Figure 2b (dashed line) shows the difference of N(E) from the hydrogenated surface following 20 min. of electron exposure and N(E) from the clean surface. From this difference curve we see that electron exposure has substantially reversed the changes at 3.5, 6.6, and 11.7 eV produced by H exposure. We attribute the reversal of hydrogen-induced changes in ELS following electron exposure to ESD of hydrogen. Since electron exposure reverses changes produced by Ga-H formation, we suggest that electron-induced dissociation of the Ga-H bond is occurring. However, we can not rule out the removal of surface Ga. The loss peak at 18 eV is much less affected by electron bombardment than peaks at 3.5, 6.6, and 11.7 eV. A volume plasmon has been predicted at 18.5 eV from optical data [10]. In earlier work we made no definitive assignment of this peak since formation of surface Ga-H would not be expected to affect the volume plasmon [9]. The lack of response of the 18 eV peak to electron exposures which substantially reverse other hydrogen-induced changes suggests that it is not associated with surface Ga-H but with subsurface or bulk hydrogen.

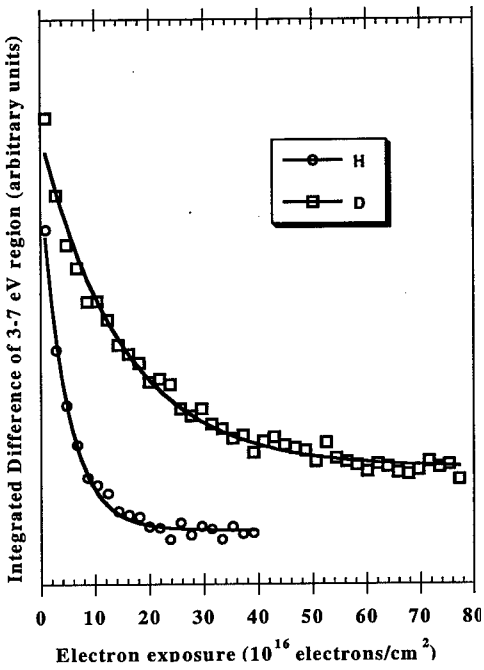

Fig. 3. Integral of the difference between N(E) from the hydrogenated (deuterated) surface following various electron exposures and N(E) from the clean surface vs. electron exposure.

Similar to the curves shown in Fig. 2b, we construct difference curves by subtracting the N(E) energy loss spectrum of the clean surface from the N(E) spectra after various electron exposures of the hydrogen-saturated surface. To quantify the desorption process, we plot the integral of the difference from 3 to 7 eV vs. the electron exposure as shown in Fig. 3. The points are fit to an exponential of the type $f(x)=A+Be^{-(\sigma x)}$ where σ is the desorption cross section (cm^2) and x is electron exposure (electrons/cm^2). The cross section for the ESD of H determined by this fit is 2 x 10^{-17} cm^2, while the ESD of deuterium shows a cross section of 7 x 10^{-18} cm^2, a factor of ~3 lower than for H.

The cross section for the ESD of hydrogen from GaN(0001) is 20 to 6000 times greater than reported on Si surfaces (Table I).

TABLE I. Comparison of desorption cross-sections from semiconductors.

Adsorbate	Substrate	Beam energy	Cross section (cm^2)	Reference
H / D	GaN(0001)	90	2.4 x 10^{-17} / 8.6 x 10^{-18}	This work,11
H / D	Si(100)	7-12	4 x 10^{-21} / 8 x 10^{-23}	13,12
H	Si(100)	7-30	3 x 10^{-20}	14
H	Si(100)	25-200	1 x 10^{-19} - 1.4 x 10^{-18}	15
D	Si(111)	16-500	<1 x 10^{-21} - 1.3 x 10^{-20}	16

On GaN the cross section for ESD of D is ~3 times smaller than for H, while on Si(100) the ESD of D is ~50 times less than for H [10]. Assuming the ESD of H from GaN(0001) occurs through an electronically excited state, as in the Menzel-Gomer-Redhead (MGR) model, the presence of a large cross section and small isotope effect would indicate slow quenching of the excited electronic state. In general, long-lived surface electronic excitations would result in enhanced efficiencies for electron- or photon-stimulated processes. This extremely fast ESD of H also has consequences for electron spectroscopies (LEED & ELS) of H/GaN. In essence, the H is removed from GaN(0001) more quickly than many electron spectroscopies can be performed.

Conclusion

We have used surface-sensitive electron spectroscopies to examine and quantify electron beam effects on the hydrogenated GaN(0001) surface. Atomic hydrogen exposure produces changes in the energy loss spectrum, decreases in intensity at 3.5 and 6.6 eV and increases in intensity at 11.7 and 18 eV. Electron bombardment of the hydrogen-saturated surface substantially reverses the changes at 3.5, 6.6, and 11.7 eV, restoring an energy loss spectrum similar that of the clean surface. We conclude that electron-stimulated desorption of hydrogen from surface Ga-H is responsible for these reversals. The increased intensity at 18 eV is not reversed by electron bombardment. We conclude that this feature is due to a volume plasmon and that hydrogen is being introduced into the subsurface or bulk. A very large cross section for ESD of H of 2×10^{-17} cm^2 was found with a reduction of ~3 for the ESD of D to 7×10^{-18} cm^2. These results suggest the participation of a long-lived surface electronic excitation leading to desorption.

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The Reaction of Oxygen with GaN(0001)

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Keywords: Adsorption, Energy Loss Spectroscopy, Surface

Abstract

The interaction of oxygen with GaN(0001) at room temperature is investigated using low energy electron diffraction (LEED), Auger electron spectroscopy (AES), electron energy loss spectroscopy (ELS), and high resolution electron energy loss spectroscopy (HREELS). Both ELS and HREELS are consistent with reaction of oxygen with surface Ga. LEED shows no surface reconstruction produced by oxygen adsorption. AES reveals a plateau in adsorbed oxygen coverage above ~200 L of exposure to molecular oxygen (1 L = 10^{-6} Torr*s). However, ELS continues to show changes in surface electronic structure to ~1000 L of O_2.

Introduction

In addition to optoelectronic applications, GaN and other Group III Nitrides also exhibit properties appropriate for their use in high frequency, high power, and high temperature transistors. The properties of these devices are affected by oxygen in several ways. One of these effects is the production of parasitic resistances and capacitances. The losses produced are more significant at higher power and frequency and have a significant impact on device performance [1]. The presence of oxygen has been seen to alter the properties of metal contacts on GaN. Bermudez recently reported differences between Schottky barrier heights for metals deposited on atomically clean and wet-chemically cleaned GaN surfaces [2]. Smith *et al.* report a marked increase in contact resistance for Al on n-GaN after heating to 500 °C which caused the formation of an aluminum oxynitride layer

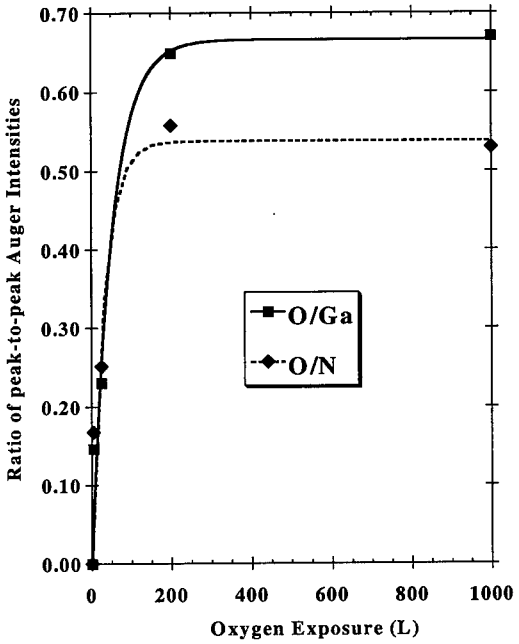

Figure 1. Ratios of Auger Electron Spectroscopy peak-to-peak heights for O(KLL)/Ga(LMM) and O(KLL)/N(KVV) signals vs. oxygen exposure at room temperature.

[3]. Reaction with oxygen also results in surface passivation. Adsorption of oxygen reduces surface band-bending compared with the clean surface, but not by as much as oxidation by wet-chemical cleaning [4]. Reaction with oxygen can result in growth of a thick oxide, but only at high temperatures [5]. Incorporation of oxygen into the bulk affects electrical properties. Pankove *et al.* have used oxygen doping to compensate Mg and improve photodetector performance [6].

The work reported here follows an extensive series of experiments on the reaction of hydrogen with GaN(0001) [7-10]. In that work it was found that the nitrogen-sputtered and annealed surface was Ga-terminated and was not reactive to molecular hydrogen. However, atomic hydrogen readily adsorbed forming surface Ga-H.

Experimental Details

This work was performed in a three-chamber stainless-steel UHV system with a base pressure of 2×10^{-10} Torr. Details of the UHV system and sample mount have previously been described [7]. The GaN sample was grown by MOCVD at the Naval Research Laboratory and is 5 mm wide x 12 mm long [11]. The GaN film was grown on a-plane sapphire which was heated to 1180 °C for 10 minutes followed by the growth of a low temperature 250 Å thick AlN layer at 600 °C. The AlN layer was ramped under NH_3 to a temperature of 1040 °C for the growth of the GaN film. The GaN film was grown using TMGa and NH_3 with H_2 as a carrier gas. It is silicon doped with a carrier concentration of 2×10^{17} cm^{-3} and mobility of 400 cm^2/Vs. The sample was rinsed with acetone then isopropyl alcohol before insertion into UHV. *In situ* sample cleaning was performed by a procedure of bombardment with 1 keV nitrogen ions and annealing in UHV at 900°C .

Results and Discussion

For sputtered and annealed GaN(0001), low energy electron diffraction (LEED) exhibited a low-background 1x1 pattern with satellites spots at some energies indicating that the surface was well-ordered but facetted. Auger electron spectroscopy (AES) was used to verify sample cleanliness. In earlier work, it was shown that this surface is Ga-terminated and exposure to hydrogen atoms produces only Ga-H surface species [7].

Oxygen exposure was performed with the sample at room temperature and facing away from the chamber ion gauge using research purity oxygen. Exposure of the surface to O_2 results in an increase in the LEED background intensity indicating a disordering of the surface. No surface reconstructions were observed after room temperature exposure. Figure 1 shows the O(KLL) to Ga(LMM) and O(KLL) to N(KVV) peak-to-peak height ratios as a function of oxygen exposure. These ratios are not corrected for sensitivity and were

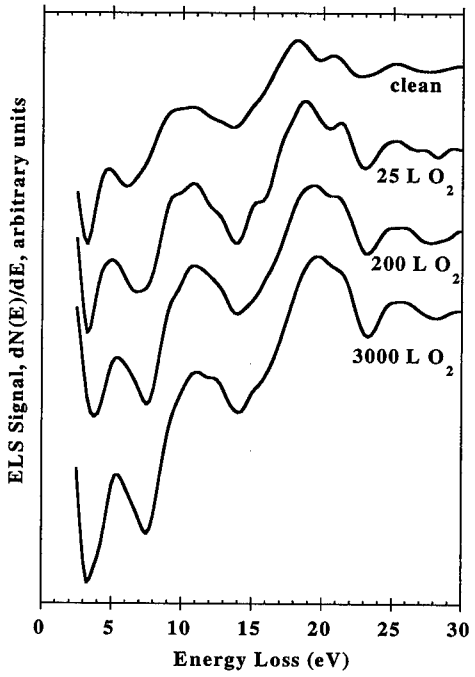

Figure 2. First derivative electron energy loss spectra of clean GaN(0001) and following various oxygen exposures at room temperature.

collected using a retarding field analyzer (dN(E)/dE) and not the more common cylindrical mirror analyzer (dEN(E)/dE). Oxygen exposure produced an increasing O(KLL) signal in AES with a maximum oxygen signal observed after ~200 L O_2 exposure (1 L = 10^{-6} Torr s), as shown in Fig. 1. Saturation is observed near 200 L in both the O(KLL) to Ga(LMM) and O(KLL) to N(KVV) ratios. A determination of the oxygen coverage in monolayers would require an assumption of the structure of the facetted GaN surface. Although it has been determined that this surface is Ga-terminated, the structure of the surface and near surface are not known. For this reason, we have not converted AES intensities into oxygen coverage. Surface electronic structure was characterized by electron energy loss spectroscopy (ELS) using 90 eV electrons. First derivative ELS of the clean and oxygen-exposed surface are shown in Fig. 2. The most dramatic change produced by oxygen adsorption is near 20 eV loss energy. The double peak seen on the clean spectrum merges nearly to a single peak after exposure to 200 L of O_2. Some additional merging is observed for larger exposures. A shift to higher loss energy is also observed for the feature near 5 eV.

Although ELS is usually collected and presented as derviative spectra (dN(E)/dE), nondifferentiated data (N(E)) is usually more useful for analysis and assignment. Fig. 3 shows N(E) electron energy loss spectra for bare GaN(0001) and after exposure to 200 and 3000 L of O_2. Also shown are the difference of oxygen exposed N(E) spectra from that of the bare surface. These subtractions reveal that oxygen produces a reduction in the ELS intensity at loss energies of 3.5 and 6 eV, as well as a large increase near 18 eV. The same changes, but to a smaller magnitude, were previously observed from the reaction of atomic hydrogen and formation of surface Ga-H [8]. The changes observed here are consistent with the reaction of both oxygen and hydrogen with surface Ga dangling bonds. Also seen from these data is that considerable changes to the electronic structure occur at exposures larger than 200 L, the exposure where the coverage plateaus as measured by AES intensity ratios. Additional changes to the surface electronic structure implies that adsorption is still occuring after 200 L. The lack of an increase in AES O(KLL) signal may be due to changes in excitation cross-sections or excape depths caused by changes in structure.

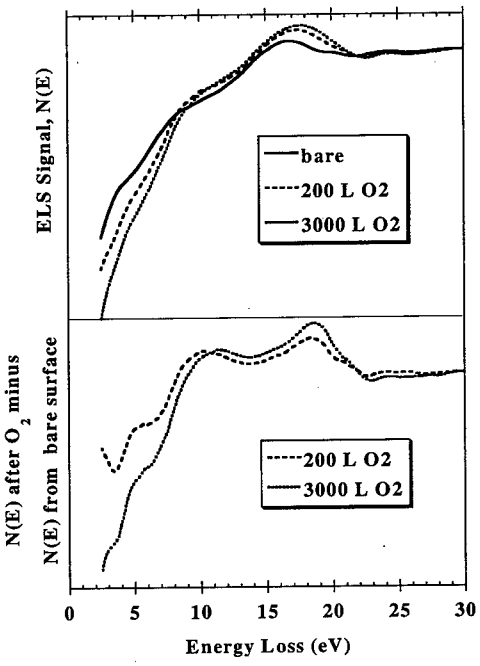

Figure 3. Shown above is the nondifferentiated energy loss spectra, N(E), from bare and oxygen-exposed GaN(0001) surfaces. Below is the difference between N(E) from the oxygenated and the bare surfaces.

Surface atomic structure was characterized by high resolution electron energy loss spectroscopy (HREELS), a surface sensitive vibrational spectroscopy. HREELS of clean GaN(0001) shows intense loss peaks at 700, 1400, 2100, 2800, and 3500 cm^{-1} due to surface optical phonons or Fuchs-Kliewer (FK) phonons. Following oxygen exposures up to 200 L, no adsorbate vibrational features are resolved from Fuchs-Kliewer phonon

losses. Oxygen exposure produced assymetric FK phonon losses with increased intensity on the higher energy loss side as has also been reported by Tsuruoka *et al.* and attributed to formation of a gallium oxide or oxynitride [12]. A HREELS peak at 690 cm^{-1} observed on oxygen-exposed CoGa(001) has been attributed to a Ga-O vibration [13]. Since Ga-O vibrations on other surfaces have been observed near 700 cm^{-1}, a Ga-O mode on GaN would be expected to be difficult to resolve from the fundamental Fuchs-Kliewer. Therefore the lack of any resolved vibrational peaks on GaN after oxygen adsorption is not inconsistent with the formation of Ga-O bonds.

Conclusion

Overall, molecular oxygen is observed to react with GaN(0001) at room temperature saturating after ~200 L of O_2 exposure according to AES but producing changes in electronic structure to exposures of ~1000 L of O_2. Both electronic structure and vibrational data are consistent with adsorption of oxygen on Ga sites and the formation of Ga-O bonds.

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Observation of Cubic GaN/AlN Heterointerface Formation by RHEED in Plasma-Assisted Molecular Beam Epitaxy

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Keywords: Cubic III Nitrides, Heterointerface, Lattice Relaxation, RHEED

Abstract The formation of cubic GaN on AlN and cubic AlN on GaN heterointerfaces, and their lattice relaxation were observed by in-situ RHEED technique. The behavior of lattice relaxation was found to be different between these two cases, and the critical thickness of the overlayers in these heterostructures was estimated to be around 150Å, which is quite large compared with the report for corresponding hexagonal crystals.

Introduction

The study of hexagonal group III nitrides has recently made a great progress aiming at the development of short wavelength optical devices and high-frequency high-power devices. Stimulated by this situation, much attention has been also paid to another crystallographic phase of III nitrides, i.e., cubic zincblende nitrides. Because of its higher crystallographic symmetry and the availability of low-cost large-area substrates, cubic nitrides are expected to have several advantages for device application, such as low carrier scattering, high doping efficiency, etc. From the viewpoint of device structure using heterostructures, cubic AlN, InN and their alloys are also important, besides cubic GaN. Due to their metastable nature, the growth of pure cubic nitrides is quite difficult, and the quality of cubic epilayers has been so far inferior to that of hexagonal nitrides. However, the recent development of molecular beam epitaxy (MBE) and chemical vapor deposition (CVD) techniques has enabled the great improvement of layer quality of cubic III nitrides [1].

We have grown high-quality cubic GaN epilayers [2], and recently achieved the growth of cubic $Al_xGa_{1-x}N$ epilayers in the whole Al compositional region by gas source MBE technique using radio frequency (RF)-N_2 plasma as a N source and 3C-SiC substrates with appropriate growth initiation techniques [3, 4]. For the device application of cubic nitride heterostructures, detailed investigation of heterointerface formation is strongly desired, such as lattice relaxation, characterization of interface flatness, etc. So far, there has been little information on the heterointerface formation of III nitrides. In the present study, we investigated the formation process of cubic GaN/AlN heterointerfaces by reflection high electron energy diffraction (RHEED) technique. Based on the observed diffraction patterns, we discuss the growing surface feature and the lattice relaxation during the heterointerface formation, in relation to their difference from the cases of corresponding hexagonal epilayers.

Experiments

The MBE growth of cubic AlN and GaN layers was done on CVD-grown 3C-SiC(001)

epilayers by using metallic III-group element sources and an RF-N_2 plasma source (SVT model-4.5). The N_2 flow rate and the plasma power were 1-2 sccm and 300-400W, respectively. The typical growth temperature was 700-750°C. The growth rates of epilayers were around 400nm/h for both cubic AlN and cubic GaN layers. The detailed growth procedure has been described elsewhere [3, 4]. AlN layers were used as a buffer layer just above the substrate. Care was taken to achieve the stoichiometric III/V ratio condition. Growing surfaces of cubic GaN and AlN epilayers on thick and relaxed cubic AlN and GaN layers were observed, respectively, by in-situ reflection high energy electron diffraction (RHEED) technique. The diffraction patterns were monitored by a CCD camera and diffraction intensity profiles were analyzed with the lapse of growing time.

Results and Discussion

RHEED patterns from cubic AlN and GaN epilayer surfaces with sufficient flatness are shown in Figs.1a) and 1e). It was confirmed that they shows (2x1) and (4x1) reconstruction structures, respectively. The (4x1) structure was also observed for an $Al_{0.2}Ga_{0.8}N$ epilayer. These clear reconstruction and streak features indicate the excellent flatness of the epilayers.

In the case of cubic GaN on cubic AlN heterointerface, the initial (2x1) streak pattern was maintained for a while after starting the deposition of GaN layers. In a short time, extra spots having a different interval from the initial streaks in the RHEED pattern appeared. Then, the newly appearing spots became brighter suddenly and the initial streaks disappeared. After that, the spots changed to streaks gradually as the GaN deposition proceeded. The RHEED patterns for this sequence is shown in Fig.1. The horizontal RHEED intensity profiles near the newly appearing spots in this sequence are shown in Fig.2. The position and width of (10) peak in Fig.2 are plotted against the elapsing time in Fig.3, and a sudden change is clearly seen at the elapsing time denoted by the arrow. This change is attributed to the lattice relaxation, and the growth mode changes from 2D to 3D manners at this point.

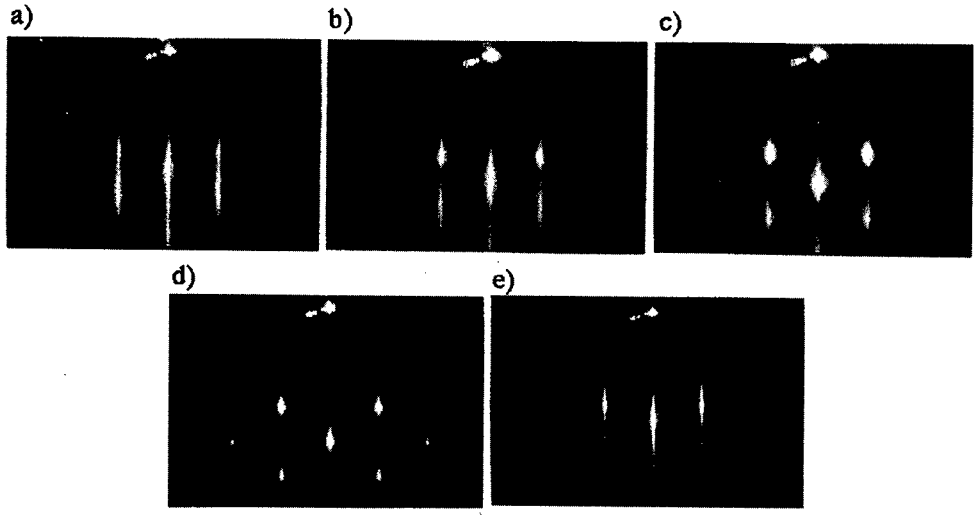

Fig.1 RHEED patterns from the growing surfaces during the cubic GaN/AlN heterointerface formation, a) initial AlN surface, showing (2x1) structure, b) 2 min after starting the deposition of GaN, c) 3 min after starting the deposition of GaN, d) 4 min after starting the deposition of GaN, and e) final GaN surface, showing (4x1) structure.

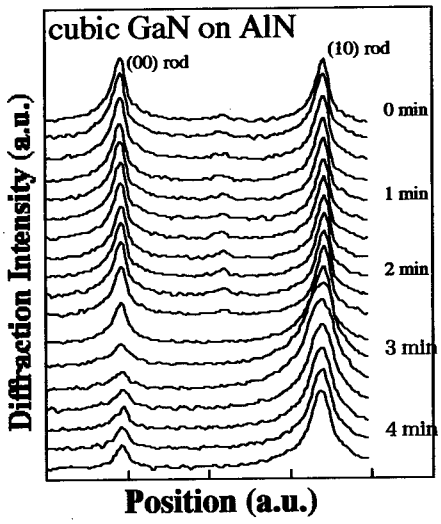

Fig.2 Horizontal RHHED intensity profiles in course of cubic GaN deposition on cubic AlN layers.

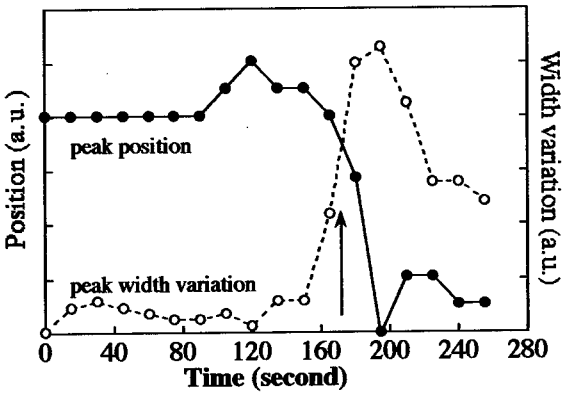

Fig.3 Position and width variation of the (10) diffraction peaks in Fig.2 against the elapsed time after starting the deposition of GaN layers.

From the change in Fig.2, the critical thickness of plastic relaxation for cubic GaN on cubic AlN is estimated to be 150Å, considering the growth rate in the present experiment. This value was quite large compared with the report for corresponding hexagonal crystal [5]. Similar sudden change was observed in the vertical profiles for the vicinity of the initial streaks. By comparing the diffraction streak intervals of the initial and final patterns, we found the lattice constant of cubic AlN to be 4.38Å, for the first time. This value agrees well with the lattice constant estimated from the same bond length as hexagonal AlN.

The case of cubic AlN on cubic GaN heterointerface exhibited a quite different behavior. Fig. 4 shows the sequence of RHEED patterns during the cubic AlN on GaN heterointerface formation. The variation of RHEED patterns due to the lattice relaxation is not so distinct as cubic GaN on AlN heterointerface. Around 170 seconds after the start of AlN deposition, extra diffraction spots having the interval corresponding to cubic AlN appeared. It is noted that AlN thickness where the extra spots appear is almost equal to the critical thickness of cubic GaN on AlN. However, the streak feature of the pattern was essentially maintained even several minutes after the start of AlN deposition. The interval of these streaks gradually changed to the one for the newly appearing AlN spots.

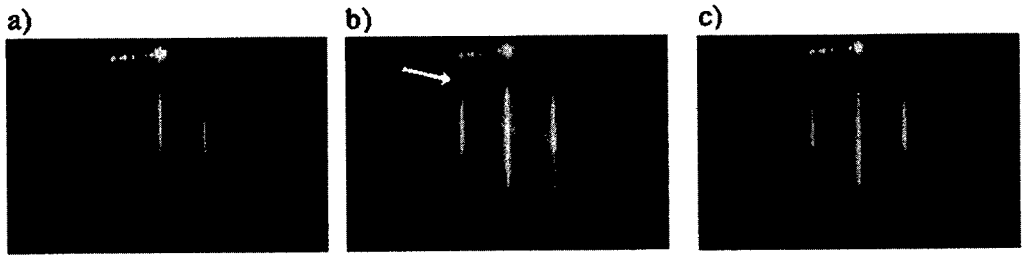

Fig.4 RHEED patterns from the growing surfaces during the cubic AlN/GaN heterointerface formation, a) 1 min after starting the deposition of AlN, b) 7 min after starting the deposition of AlN, and c) 14 min after starting the deposition of AlN. Extra spots corresponding to AlN are indicated by the arrow in b).

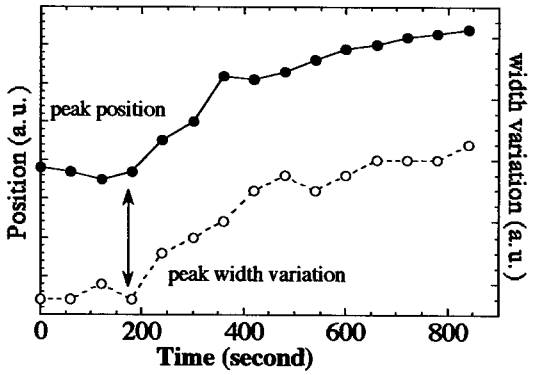

Fig.5 Position and width variation of the (10) diffraction streak against the elapsed time after starting the deposition of AlN layers for cubic AlN/GaN heterointerface.

The position and width for the streaks are plotted against the elapsed time in Fig.5. These results mean that the main relaxation occurs elastically, and some part of the relaxation is by the plastic one due to the dislocation introduction, which results in the occurrence of extra diffraction spots.

Comparing our results with the previous report for corresponding hexagonal crystal on sapphire [5], the general features are similar to each other. However, the initial sudden change of lattice constant for AlN on GaN interface, and a quite small critical thickness for GaN on AlN interface, etc. were not observed in our experiment. These differences may be explained by the different situation concerning dislocation density, which is caused by the lattice mismatch between epilayers and substrates.

Summary

We observed the cubic GaN/AlN and AlN/GaN heterointerface formation by RHEED, and analyzed their lattice relaxation and lattice constant precisely from the intensity profiles. It was found that the relaxation occurs plastically and results in the growth mode change from 2D to 3D for cubic GaN/AlN. For cubic AlN/GaN, the relaxation was found to occur elastically. The critical thickness of the overlayers in these heterostructures was estimated to be around 150Å.

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Analysis of Dislocation Densities and Nanopipe Formation in MBE-grown AlN-Layers

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Keywords: AFM, Nanopipes, RBS/Channeling, SiC Substrates, Spiral Growth, XRD

Abstract: To study the influence of the growth parameters on structural properties and crystal quality epitaxial layers of aluminum nitride were grown on Si-terminated SiC- and sapphire substrates (0001) by varying substrate temperature, growth rate, and III/V ratio in a RF-plasma enhanced MBE-system. A detailed analysis of dislocations was performed by RBS channeling and X-ray diffraction measurements and was compared with TEM results obtained on cross sectional and plan view samples. The annihilation of threading dislocations during the growth process was observed by RBS-channeling depending on the type of substrate and the growth mechanism. Lowest dislocation densities are obtained for 2D-growth on SiC substrate in the range of $2 \cdot 10^8$ cm^{-2}. The reduction of the growth temperature from 1000°C to 900°C lead to an increase of the dislocation density by about an order of magnitude and in the case of 2D growth we observed for the first time in MBE grown AlN-layers the formation of regularly shaped nanopipes located within a screw dislocation. The spirals are composed by monoatomic steps surrounding nanopipes with diameters of 10 – 60 nm. Their formation is discussed according to the Frank theory resulting in a ratio of surface free energy to shear modulus of about $3 \cdot 10^{-3}$ nm.

Introduction: For the development of semiconductor UV detectors epitaxial layers of aluminum nitride (AlN) were grown on sapphire and silicon carbide (SiC) substrates using plasma enhanced molecular beam epitaxy. Due to the large band gap of 6.2 eV these layers offer a wide field of applications ranging from optical UV filters and insulating layers to optoelectronic devices like LED's, Laser diodes or detectors [1]. In addition, the thermal stability of the materials allows to fabricate high temperature devices. A basic problem for device fabrication is the usually high dislocation density of the layers in the range of up to several 10^{10} cm^{-2}. It is shown in reference [2] that the free carrier concentration and their mobility are affected seriously by the dislocation density. For the applicability of these layers a sufficient material quality is necessary, particularly with respect to crystal quality, impurities and appropriate doping. A 2D epitaxial growth along monoatomic steps is suitable to obtain high crystal quality. Recent experiments could reduce the dislocation density for GaN down to about 10^6 cm^{-2} [3, 4] using the lateral epitaxial overgrowth technique (LEO). But those layers still show a regular pattern of high and low dislocation densities. To reduce the amount of threading dislocations (TD) homogeneously their formation process and the corresponding growth conditions have to be studied in detail. Some results are reported for the growth of GaN [5] but only little has been published for the growth of AlN.

Experimental: The AlN-layers were grown by molecular beam epitaxy (MBE) on (0001) 6H-SiC substrates oriented 3.5° off axis towards [11$\bar{2}$0] in a Riber P32 machine equipped with gallium and aluminum effusion cells. Nitrogen radicals were produced by the Oxford Applied Research CARS25 RF-Plasma source. The nitrogen beam equivalent pressure (BEP) was varied between $2.1 \cdot 10^{-6}$ hPa and $1.9 \cdot 10^{-5}$ hPa corresponding to a flow rate of 0.1sccm and 0.7sccm, respectively. RF-power was kept at 440W. The substrate temperature was varied between 900° and 1050°C for the growth of AlN. Substrates were degassed at 1050°C until the streaky 1x1 reflection high energy electron diffraction (RHEED) pattern of the Si-terminated surface was observed. AFM

measurements were performed in situ with an Omicron UHV-STM/AFM system connected to the MBE and ex situ with a Digital Instruments Nanoscope III. The full width at half maximum (FWHM) of XRD-rocking curves was obtained from ω-scans of the AlN (0002) reflex using a four crystal x-ray diffractometer with Cu-K_α radiation and dislocation densities were calculated from this following the method of Ayers [6]. The thickness of the layers was determined by Rutherford backscattering (RBS) and transmission electron microscopy (TEM).

Fig. 1: Cross-sectional TEM image of an AlN layer grown on SiC substrate. The interface shows high dislocation density in the range of about 10^{11} cm^{-2}. Within the AlN layer the density of threading dislocations is reduced to $1{\cdot}10^{9}$ cm^{-2}. (evaluated from TEM plan view images)

Influence of growth parameters: The formation of TD was followed by TEM, RBS-channeling and by XRD-rocking curves. A transition from 2D to 3D growth was observed for very high and for low V/III-ratios resulting in an increase of FWHM of the XRD-rocking curves [7]. The observed increase corresponds to a rise of the amount of TD of more than two orders of magnitude compared to the best values of about $2{\cdot}10^{8}$ cm^{-2} in the case of stoichiometric, 2D grown layers on SiC. The 2D/3D transition is traced back to a reduced surface mobility of Al for the nitrogen terminated surface. For both, SiC and sapphire substrates, cross-sectional TEM images show high dislocation densities of about several 10^{11} cm^{-2} at the interface to the substrate of the 2D grown AlN layers (fig. 1). During the growth process this amount is reduced due to annihilation of the defects whose Burger's vectors are reasonably tilted with respect to the growth direction. The amount of the tilt of Burger's vectors depends strongly on the type of substrate and the growth conditions indicated by different annihilation rates of the defects. Fig. 2 shows depth profiles of TD density obtained by RBS-channeling. In the case of 2D grown films on SiC a high annihilation rate of TD emerges close to the interface while the rate is decreased for 3D grown layers and even more for layers nucleated on sapphire. But in all cases there seems to appear a second, much slower annihilation process which is attributed to TD with Burger's vectors directed close to the growth direction.

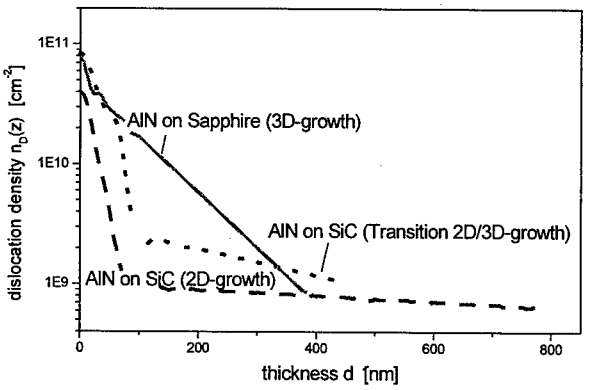

Fig. 2: Profiles of the dislocation density in dependence on the thickness of the epitaxial layer measured by RBS-channeling. Thickness values starting at the substrate interface.

The defect density is also influenced by the growth temperature of the layers. A decrease from 1000°C to 900°C increases the defect density by a factor of about 5 (fig. 3). The observed offset between the values obtained from XRD and from RBS-channeling of about an order of magnitude is related to the fact that RBS-channeling is only sensitive to

defects with Burger's vectors showing a suitable tilt to the measured lattice channels oriented in the (0001) direction. XRD-rocking curves are sensitive to all kind of defects and result therefore a higher defect density. Additionally, it must be remarked, that the results may not only be determined by TD but also by a tension induced into the lattice by deep grooves observed for growth temperatures below 950°C.

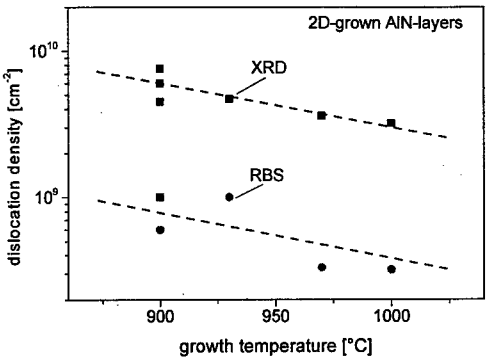

Fig. 3: Variation of the threading dislocation density with growth temperature. Complementary results from XRD-rocking curves and RBS-channeling measurements.

Formation of hollow core screw dislocations: While at temperatures above 1000°C 2D step flow growth is observed, the AFM image (fig. 4) shows growth spirals with a density of $2 \cdot 10^7$ cm^{-2} at substrate temperatures below 970°C for AlN layer (> 2 µm) on sapphire composed by monoatomic steps. Step heights of about 0.25nm (see line scan in fig. 4) are observed which fits the value of c/2 = 0.258nm for bulk AlN [8]. Some of those growth spirals exhibit nanopipes in the center with diameters in the range from 16 nm to 50 nm. These hollow core screw dislocations showed Burger's vectors in the range of 2c to 5c determined by counting the amount and height of the steps originated in the center of a spiral. An analysis according to Frank's theory [9] results a ratio of free surface energy to shear modulus $\gamma/\mu = (3 \pm 1) \cdot 10^{-3}$ nm from the slope of the plot of the nanopore radius r versus the square of the Burger's vector b following the equation $r = (\mu b^2)/(8\pi^2\gamma)$ (fig. 5). Different sets of data points in figure 5 refer to different AFM tips, which influence the result on the pore diameter while γ/μ stays in the same range. The result is in good agreement with values obtained for GaN ($\gamma/\mu = 1 \cdot 10^{-3}$ nm [10]) and for SiC ($\gamma/\mu = 1.5 \cdot 10^{-3}$ nm [11]) but is one

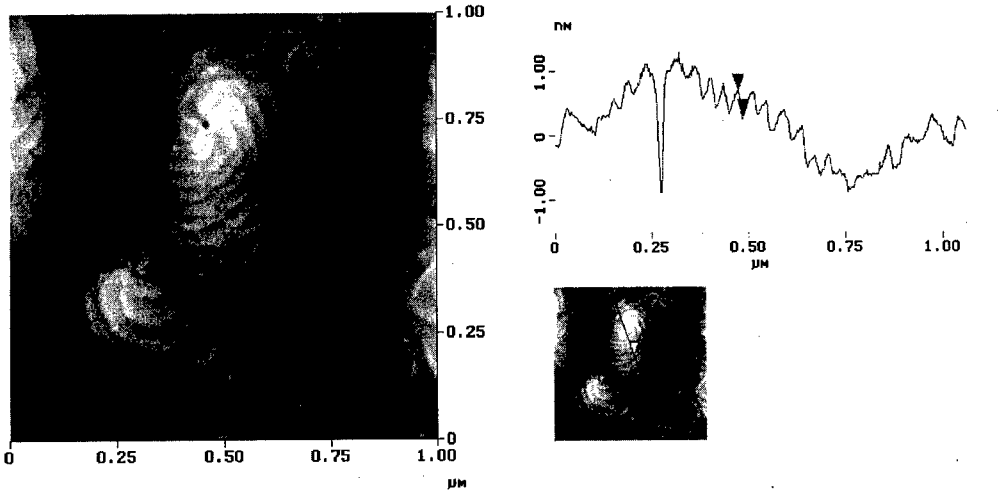

Fig. 4: AFM height image of an MBE grown AlN layer with growth spirals on (0001) sapphire substrate (1 µm x 1 µm). The spirals are composed by monoatomic steps surrounding nanopipes with diameters of 10 – 60 nm. On the right hand side a line scan is shown exhibiting monoatomic steps of the growth spiral (arrows).

order of magnitude below the theoretical value of $\gamma/\mu = 1 \cdot 10^{-2}$ nm. There may be two reasons for this deviation. The first one is due to the uncertainty of the AFM measurement. But this does not hold for the results for GaN and SiC which are also supposed to have one order of magnitude higher γ/μ values. More reasonably a portion of edge type dislocation has to be taken into account.

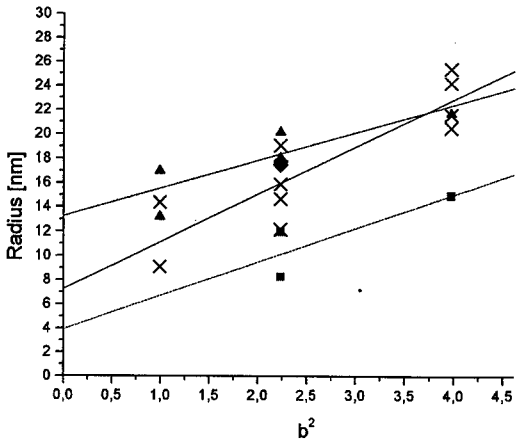

Fig. 5: Radius of the nanopipes versus the square of the Burger's vector b according to Frank's equation. Different data sets correspond to different AFM-tips.

Conclusions: The density of TD was analyzed with respect to layer thickness, V/III-ratio and growth temperature. The annihilation of defects was influenced by the type of substrate and the growth mechanism (2D/3D) due to the formation of defects with differently oriented Burger's vectors. Higher dislocation densities were found at lower substrate temperatures. A transition from 2D step flow to 2D spiral growth is observed for substrate temperatures below 970 °C. In some cases growth spirals were observed with nanopipes of the type of hollow core screw dislocations. The formation follows Frank's theory resulting a γ/μ of about $3 \cdot 10^{-3}$ nm in accordance with the results for GaN and SiC. The deviation from the theoretical value of about one order of magnitude is related to the contribution of edge type dislocations involved in the formation of the pores.

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Correlation between Optical and Structural Properties of Thick GaN Films Grown by Direct Reaction of Ga and NH_3

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Keywords: Growth, Metallic Ga, Optical Properties, Structural Properties, Thick GaN

Abstract : Thick GaN films were grown on sapphire by the direct reaction of metallic Ga and ammonia in a conventional RF induction heated chemical vapor deposition reactor. The crystal and optical qualities of the thick GaN was evaluated as functions of the distance between sapphire substrate and Ga source, growth temperature and time with X-ray diffraction (XRD) and photoluminescence (PL) measurements. For thick GaN grown at the position of 3.5 cm away from the Ga source, the FWHM of (0002) peak in XRD curve was about 684 arcsec, which is comparable to the previously reported values. The growth rate of the thick GaN film was about 18 ㎛/h. Deep level yellow luminescence had a close relation to $(10\bar{1}0)$ and $(10\bar{1}1)$ planes developed in the growth of GaN.

1. Introduction

The recent realization of efficiently bright blue, green, and yellow light emitting diodes and laser diodes using InGaN and GaN has stimulated tremendous scientific interest in the physical properties of the III-nitride materials [1]. For the device applications, considerable investigations for the growth of high quality III-nitrides have been carried out in the past several years. But the development of a suitable substrate material on which lattice-matched III-nitride epilayers can be grown is the most serious issue to solve in the near future.

Among various substrates which have been intensively examined for growing high quality GaN, bulk GaN crystals seems to be the most attractive and suitable substrate. But the size of bulk GaN crystals grown so far are still too small to be used as substrates [2]. Another promising substrate is the thick GaN film. Currently, three-types of growth methods for thick GaN are under development. They are (1) hydride vapor phase epitaxy (HVPE) [3], (2) sublimation of amorphous GaN powders [4], and (3) the direct reaction of metallic Ga with NH_3 using high temperature vapor phase epitaxy [5].

In this work, we grew thick GaN films on sapphire by the direct reaction of metallic Ga and ammonia in a chemical vapor deposition (CVD) reactor. We have grown thick GaN films at various growth conditions and attempted to correlate the structural and optical properties of thick GaN films.

2. Experiment

Thick GaN was grown using a modification of the horizontal CVD reactor as described in our previous report [6]. The cylindrical susceptor made in four parts from high purity graphite coated with SiC was heated inductively by a solid state RF generator (15kW) operating at a frequency around 100 kHz using a solenoid coil. Figure 1 shows the schematic diagram of the susceptor.

Metallic Ga (0.1 g) was placed in a hole dug on the lower part of the graphite susceptor and a chemically treated 10 × 7 mm c-sapphire substrate was mounted a few centimeters apart from the Ga source on the same plane, as shown in Fig. 1. After cleaning the sapphire surface with H_2 at 540℃ for 10 min, NH_3 was introduced into the reactor with a flow rate of 500 sccm and thick GaN thin films began to grow at a growth temperature. The growth of thick GaN films was carried out at 0.8 torr with 500 sccm of NH_3 flow, varying the distance between the Ga source and sapphire substrate (1.5 - 3.5 cm), growth temperature (1030 - 1150℃), and ime (20 – 60 min).

XRD and Raman spectroscopy were employed to investigate the structural properties of thick GaN films. The surface and cross-sectional morphologies were examined using a scanning electron microscope (SEM).

Optical properties of the thick GaN were determined using photoluminescence (PL) excited with 325 nm line of a He-Cd laser.

3. Results and discussion

Figure 2 shows XRD patterns for thick GaN films grown on a sapphire surface positioned at 1.5 (P_1), 2.5 (P_2), and 3.5 (P_3) cm away from the Ga source, respectively. For GaN films grown at P_1 and P_2, XRD spectra exhibit a sharp peak of wurtzite GaN(0002) at 2θ = 34.35° with blunt peaks for GaN($10\bar{1}1$) and GaN(0004) at 2θ = 36.75 and 72.85°, respectively [Fig. 2 (a) and (b)]. However, the XRD spectrum for GaN grown at P_3 shows diffraction only from the c-plane of GaN and the sapphire substrate [Fig. 2(c)]. The uncorrected FWHM ofthe(0002) peak is about 0.191° (corresponding to about 684 arcsec). This value is comparable to the previously reported data [4,5]. Although not illustrated in his paper, the Raman spectrum for the GaN film exhibited the high film exhibited the high frequency E_2 mode at 568 cm^{-1}, also indicating the growth of wurzite GaN crystal mainly in the c-direction. A SEM photograph for the surface and cross-section of the GaN film grown for 20 min at the condition of Fig. 2(c) shows that thick GaN film grows with a columnar structure and the thickness of the film is about 6 ㎛, corresponding to a growth rate of 18 ㎛/h [Fig. 3].

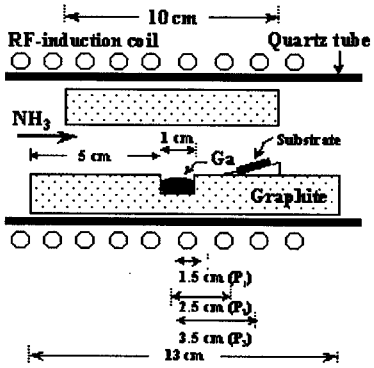


Figure 1. Schematic diagram of RF - induction heated CVD reactor for the growth of thick GaN by the direct reaction method

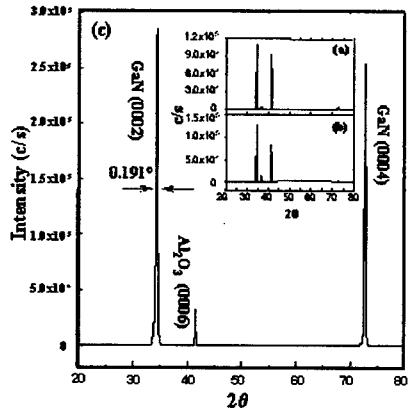


Figure 2. XRD spectra for thick GaN grown as a function of the distance between the Ga source and the sapphire substrate: (a) 1.5 cm, (b) 2.5 cm, (c) 3.5 cm.

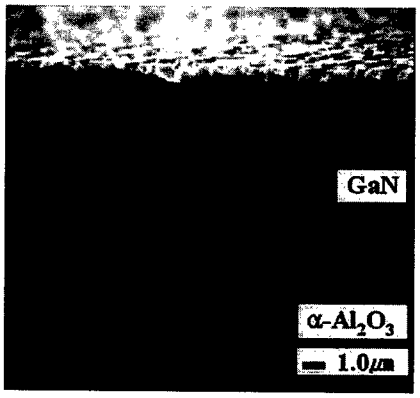


Figure 3. A Cross-sectional SEM photograph for thick GaN grown for 20 min at (a) 1070℃.

Room temperature PL spectrum for GaN film grown at P_1 exhibits both deep level yellow (YL) and band edge (BE) emissions at peak energies of 2.246 and 3.398 eV, respectively, [see Fig. 4(a)]. For GaN films grown at P_2 and P_3, however, strong band edge emissions were observed at the energy positions of 3.358 and 3.414 eV, respectively, while a deep level yellow emission was greatly suppressed as shown in Fig. 4(b) and (c). This means that optical properties of the GaN thick films are greatly dependent on the distance of the substrate from the Ga source.

In this system, the growth may be influenced by the vapor pressure of liquid Ga, the temperature profile in the graphite susceptor, and the flow pattern of NH_3 in the reactor. At a constant flow rate of NH_3 (500 sccm), pressure(0.8 torr), and Ga amount, the temperature gradient in the graphite susceptor impacts significantly the amount of Ga transferred to the trate surface since the adsorption coefficient of gaseous Ga

will decrease with an increase in the surface temperature. We measured temperatures at positions of 0, 1.5, 2.5, and 3.5 cm from the center and observed the decrease of the temperature along the axial direction of the graphite from the Ga source to the edge due to the heating property of graphite with RF-induction. After the growth, we also found that the amount of deposited solid-products increased from the center to the edge of the graphite susceptor. Considering that the amount of Ga adsorbed on the reacting surface increases with the axial distance of the graphite boat from the center to the edge, we can speculate that Ga-deficient GaN film may grow at P_1, while stoichiometric GaN film grows at P_3. This seems why Fig. 4 showed a deep level yellow luminescence light dominantly emitted from GaN grown at P_1, while the band edge emission prevailed in GaN grown at P_2 and P_3. Our experimental observations indirectly support the previous reports that the Ga vacancy is related to the origin of the yellow luminescence emitted from GaN [7]. Nishida et al. have also observed the similar variation of the PL spectrum from the YL to the BE with the structural change when decreasing H_2 carrier flow rate. in a two-flow horizontal MOVPE reactor [8].

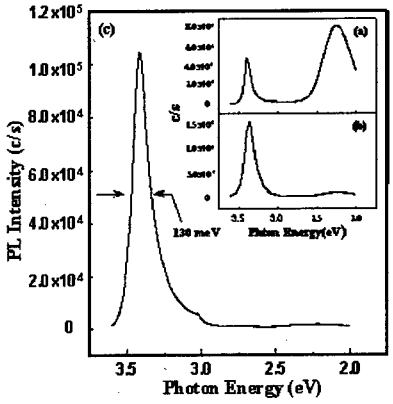
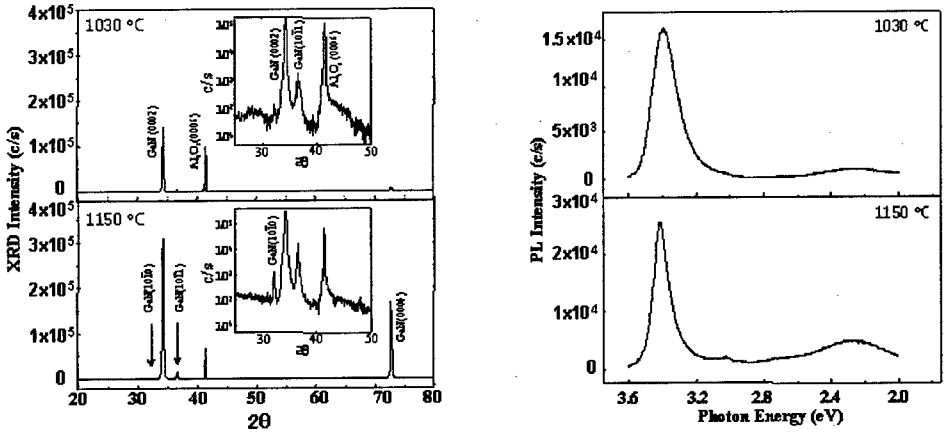


Figure 4. PL spectra for thick GaN grown as a function of the distance between the Ga source and the sapphire substrate : (a) 1.5 cm, (b) 2.5 cm, (c) 3.5 cm.

For thick GaN films grown at 3.5 cm away from Ga source for 60 min, varying the growth temperature of 1030 ~ 1150℃, XRD spectra of Fig. 5(a) showed that all the films grew predominantly along the c-plane of GaN and sapphire, but some weak peaks corresponding to $(10\bar{1}0)$ and $(10\bar{1}1)$ refractions at 2θ =32.2 and 36.7 °, respectively, appeared from the samples. The intensity of the smaller peaks was significantly influenced by the growth temperatures. The growth of the GaN films along $[10\bar{1}0]$ and $[10\bar{1}1]$ directions is mainly due to misoriented structures. It has been reported that the growth of misoriented structures is significantly affected by GaN growth condition and surface preparation condition of substrates [9].

PL spectra of the GaN films were measured at room temperature (see Fig. 5(b)) and correlated with the results of XRD spectra. Figure 6 depicts the intensity variation of (1010) and (1011) peaks and that of YL.



(a) (b)

Figure 5. (a) XRD and (b) PL spectra for thick GaN grown for 60 min with 500 sccm NH_3 at 1030℃ and 1150℃.

For an accurate comparison the intensities of XRD peaks were normalized to that of the (0002) peak, and the YL intensity was normalized to that of band edge luminescence. The intensity of XRD peaks varies in the

similar way with that of the YL. This means that the growth of GaN with $(10\bar{1}0)$ and $(10\bar{1}1)$ structures enhances the evolution of the YL. SEM images for the thick GaN films grown at 1150℃ also showed that the film involved many misoriented defects and micrometer sized grain structures.

Many research groups have studied theoretically and experimentally the structural properties of $(10\bar{1}0)$ and $(10\bar{1}1)$ planes and some of them have attempted to correlate the structures with the optical properties of GaN [10, 11]. When summarizing their experimental and theoretical studies, it seems that the origin of YL has a direct relation to extended defects, native defects, and impurities included in the GaN films. From our consistent observation on the correlation between the YL and the structures of $(10\bar{1}0)$ and $(10\bar{1}1)$ planes, we speculate that the emission of YL is mainly due to the formation of deep gap state in the band gap by Ga vacancy and impurities trapped at domain boundary with $(10\bar{1}0)$ and $(10\bar{1}1)$ atomic facets. Similar behavior was also observed from the correlation between XRD and PL peak intensities for thick GaN films grown for different times.

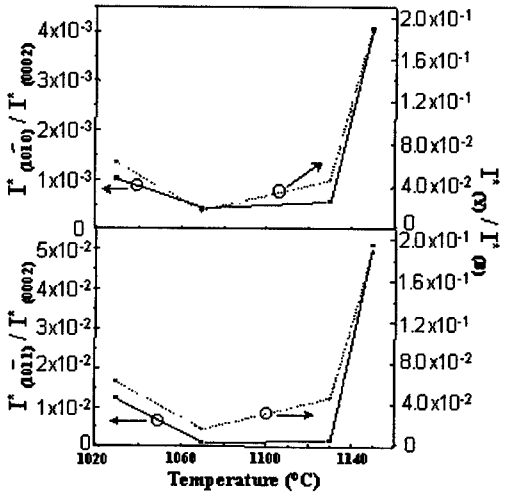


Figure 6.The integrated peak intensity ratio of YL to BL and of $(10\bar{1}0)$ and of $(10\bar{1}1)$ to (0002) as a function of the growth temperature.

4. Conclusion

Wurzite GaN thick film was grown on sapphire substrate at 0.8 torr and 500 sccm NH_3 by the direct reaction of metallic Ga (0.1 g) in a conventional CVD reactor as function of the distance of the substrate from the Ga sourc, growth temperature, and time. X-ray diffraction (XRD) and photoluminescence (PL) measurements for these GaN films revealed that the structural and optical properties of the films were significantly influenced by the distance of sapphire substrate from Ga source, the growth temperature and time. Our experimental observations showed that the YL had a close relation to $(10\bar{1}0)$ and $(10\bar{1}1)$ planes developed in the GaN growth. It was speculated that the YL emits from the deep gap state formed in the band gap by Ga vacancy and impurities trapped at domain boundary with $(10\bar{1}0)$ and $(10\bar{1}1)$ atomic facets.

Acknowledgement.

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Improved Electron Emission from Defective Diamond Film Deposited by CVD Method

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Abstract Influence of the defects in the diamond films on electron emission has been studied by using electron spin resonance (ESR) method. The defect density in the diamond film increased up to a order of 10^{18} spins/cm^3 when the CH_4 concentration was increased at 5 %. When the defect density in the diamond film is sufficiently high, electrons are efficiently supplied to the diamond surface from the back of the diamond film through defect-induced energy band by a hopping conduction. Therefore, the emission current at the applied electric field of 8 V/μm increased up to $1x10^2$ μA/cm^2 with increasing the defect density.

1. Introduction

The diamond film deposited by chemical vapor deposition (CVD) method has unique properties such as wide band gap, high electron and hole mobility etc. One of the applications of the diamond film is an electron emitter, because hydrogen-terminated (as-grown) diamond surface has negative electron affinity (NEA) [1-3]. For the diamond electron emitter with vacuum-diamond-Si substrate (electrode) system, the electrons in Si substrate are injected into the diamond film through the diamond/Si interface. On the other hand, the electrons at the diamond surface are easily emitted from its surface due to the NEA. However, it is difficult to transport electrons from the back of the diamond film to the surface as the diamond film is a high resistance material. One of the electron transportation mechanisms is the hopping conduction through the defect-induced energy bands. Therefore, defects in the diamond film affect the emission characteristics such as emission current and threshold electric field. [4,5]

In this paper, we will discuss influence of the defect on electron emission from a defective diamond film by using ESR method.

2. Experiments

The diamond film with thickness of 4 μm was deposited by hot filament type CVD method from CH_4 and H_2 gases. The CH_4 concentration in H_2 was varied from 0.5 to 5 %. The emission current was measured in a vacuum of ~$1x10^{-6}$ torr. The cathode area of the diamond film and distance between the cathode and the anode were 25 mm^2 and 200 μm, respectively. To investigate the defect structures, the ESR measurement was performed using X-band spectrometer at room temperature.

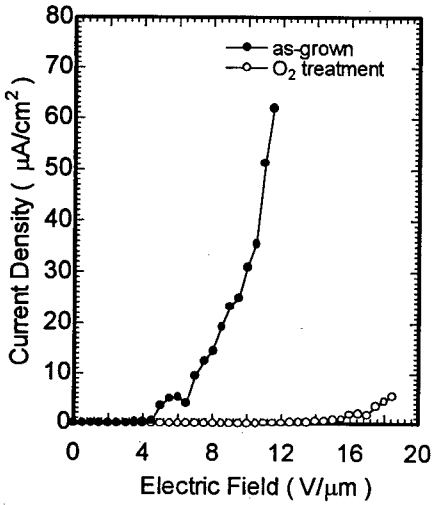

Fig. 1 The electron emission as a function of the electric field for the as-grown and the oxidized diamond films

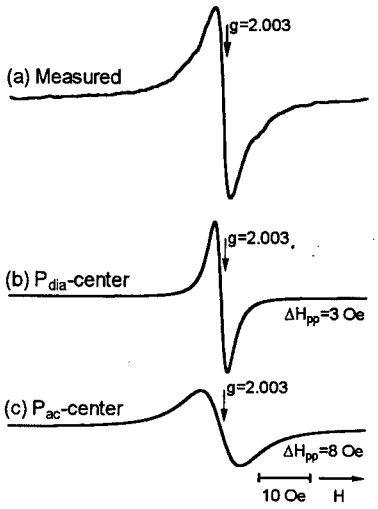

Fig. 2 (a) the ESR signal observed for the diamond film, (b) the P_{dia}-center and (c) the P_{ac}-center

3. Results and Discussion

Fig. 1 shows the emission current as a function of the applied electric field for the diamond films deposited at the CH_4 concentration of 1 %. The as-grown diamond film exhibits efficient field emission with low threshold electric field of 4 V/μm. The current density at 12 V/μm was 63 μA/cm^2. When thermal treatment was carried out in oxygen atmosphere at 600 °C for 10 min in order to oxidize the diamond surface, the emission current was decreased up to $1x10^{-1}$ μA/cm^2 along with an increase in the threshold electric field.

Fig. 2 (a) shows the typical ESR signal for the diamond film deposited at the CH_4 concentration of 1 %. The ESR signal has a Lorenzian line shape with g=2.003 and ΔH_{PP}=3 Oe and has a tail at its foot. This ESR signal for the diamond film was composed of two kinds of ESR centers as shown in Fig. 2 (a) and (b). [6,7] One is narrow Lorenzian line with g=2.003, ΔH_{PP}=3 Oe and the other is broad one with g=2.003, ΔH_{PP}=8 Oe. The natural and the synthetic diamonds exhibit ESR signal with g=2.0023 - 2.0027 and ΔH_{PP}=3.0 - 6.0 Oe. [8-10] Walters *at al.* [11] reported that the mechanically damaged surface region on colorless diamond powder has an ESR signal with 2.0027 and ΔH_{PP}=5.5 Oe. They suggested that this ESR signal is attributed to broken bonds of carbon. The observation of the ESR with a narrow ΔH_{PP} implies the formation of well crystallized diamond [12]. On the other hand, amorphous carbon films exhibit a broad ESR line with 2.0027, ΔH_{PP}=6 - 12 Oe. [13] Therefore, the deconvoluted narrow ESR center originates from carbon dangling bonds in the diamond (P_{dia}-center) and the broad one originates from carbon dangling bonds in the non-diamond phase carbon (P_{ac}-center). The correlation between these ESR centers and resistance on the diamond film has been reported in the references [6,7].

Fig. 3 (a) and (b) show the changes in the emission current and in the threshold electric field with an increase in the CH_4 concentration, respectively. The emission current density at

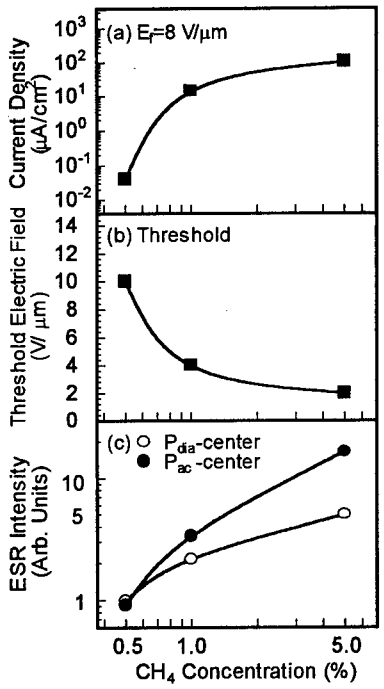

Fig. 3 (a) the current density, (b) the threshold electric field and (c) the ESR intensity as a function of CH_4 concentration.

8 V/μm increased from $4x10^{-2}$ to $1x10^{2}$ μA/cm^2 with an increase in the CH_4 concentration from 0.5 to 5 %. On the other hand, the threshold electric field is deduced from 10 to 2 V/μm with an increase in the CH_4 concentration. Fig. 3 (c) also shows the change in the spin densities of the ESR centers as a function of the CH_4 concentration. These spin densities was increased by 5 and 18 times for the P_{dia}- and the P_{ac}-centers, respectivly with an increase in the CH_4 concentration from 0.5 to 5 %. The spin densities of each ESR centers in the diamond film deposited at 5 % are $1.2x10^{18}$ and $4x10^{18}$ spins/cm^3, respectively.

The electron affinities of the as-grown (hydrogen-terminated) and the oxidized diamond surfaces are negative and positive, respectively. [14] The electrons are efficiently emitted from the diamond surface with a negative electron affinity. Therefore, the emission current from the as-grown diamond film is higher than that of the thermally oxidized diamond film. This result indicates that the hydrogen termination to the diamond surface plays an important role for efficient electron emission. However, the efficiency of electron emission is governed by the defect structures in the diamond film in addition to the specimens of the diamond surface.

The undoped diamond films have high resistivity, as the band gap of a diamond is high (5.5 eV). Hence there is no electron, that could be excited in conduction band in the diamond film at room temperature. Therefore, it is difficult to transport the electrons from the back of the diamond film to the diamond surface. However, the diamond film deposited by the CVD method exhibits low resistivity. [15] On the other hand, the ESR results in this study exhibit that the dense defects with spin densities of the 10^{17} - 10^{18} spins/cm^3 exist in the diamond films. These high

density defects create the additional (defect-induced) energy band(s) within the band gap of the diamond film. When the defect-induced energy bands are sufficiently dense, the hopping conduction of carrier dominates in the diamond film and the resistivity of the diamond film decreases. The resistivity ($6x10^5$ Ω-cm) of the diamond film deposited at the CH_4 concentration of 5 % was lowed by two orders than that of the diamond films deposited at 0.5 %. [14] Therefore, the high-density electron emission was obtained from the defective diamond film deposited at 5%, because electrons are efficiently supplied from the back of the diamond film to the surface through the defect-induced energy band(s) by hopping conduction.

4. Summary

The as-grown (hydrogen-terminated) diamond film exhibits high-density electron emission compared to the oxygen-terminated one. The emission current density was dependent on the defect density in the diamond film in addition to the terminated specimen of its surface. The efficient electron emission was obtained for the defective diamond film deposited at high CH_4 concentration of 5 %, as electrons are supplied to the diamond surface through the defect-induced energy band(s) by the hopping conduction.

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Theory of Impurities and Defects in III-Nitrides: Vacancies in GaN and Related Materials

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Abstract We review a theoretical approach for studying defects and impurities in wide-band-gap semiconductors, focusing on mechanisms that limit doping. Among native defects, vacancies play a prominent role. They cause compensation, and also give rise to luminescence bands. The behavior of gallium and nitrogen vacancies in GaN is compared with cation and anion vacancies in other wide-band-gap semiconductors, including ZnO.

1. Introduction

The III-nitride semiconductors are widely recognized as excellent materials for a wide range of electronic and optoelectronic devices, including light emitters, detectors, and transistors for high-temperature, high-power, and high-frequency applications. The ability to control doping is crucial for all of these applications; wide-band-gap semiconductors such as GaN have long suffered from lack of control of p-type and/or n-type doping. In this paper we discuss how a theoretical approach for native defects and dopant impurities, combined with state-of-the-art first-principles calculations, can be used to understand the various factors that govern doping.

Among the various types of native point defects, only *vacancies* are low enough in energy to form in significant concentrations. Nitrogen vacancies are *not* responsible for the n-type conductivity of as-grown GaN; however, they do act as donors and compensate p-type GaN. We will discuss similarities and differences with anion vacancies in other III-V and II-VI compounds, including ZnO. Gallium vacancies act as acceptors and form a source of compensation in n-type GaN. Furthermore, we have proposed the gallium vacancy to be the source of the "yellow luminescence". Again, we will draw comparisons with other wide-band-gap semiconductors, including ZnO, where we suggest Zn vacancies to be the cause of the "green luminescence".

Section 2 contains a brief description of the theoretical approach. In Section 3 we will discuss results for anion vacancies: V_{N} in the nitrides, and V_{O} in ZnO. Section 4 contains our results for cation vacancies : V_{Ga} or V_{Al} in the nitrides, and V_{Zn} in the II-VI compounds.

2. Theoretical approach

The key parameters in our approach are obtained from first-principles calculations that do not require any adjustable parameters nor any input from experiment. The computations are founded on density-functional theory, using a supercell geometry and soft pseudopotentials. Details of the computational approach can be found in Refs. [1] and [2].

A key quantity describing the behavior of defects and impurities is their *formation energy*, E^f. The formation energy determines the equilibrium concentration of impurities or native defects according to the expression $c = N_{\text{sites}} \exp(-E^f/k_B T)$, where N_{sites} is the number of sites the defect or impurity can be incorporated on, k_B the Boltzmann constant, and T the temperature. It is clear that defects with a *high* formation energy will occur in *low* concentrations.

The formation energy is not a constant but depends on the growth conditions. For example, the formation energy of an oxygen donor is determined by the relative abundance of O, Ga, and N atoms, as expressed by the chemical potentials μ_{O}, μ_{Ga} and μ_{N}, respectively. If the O donor is charged (as is expected when it has donated its electron), the formation energy depends further on the Fermi level (E_F), which acts as a reservoir for electrons. Forming a substitutional O donor requires the removal of one N atom and the addition of one O atom:

$$E^f(\text{GaN:O}_\text{N}^q) = E_{\text{tot}}(\text{GaN:O}_\text{N}^q) - \mu_{\text{O}} + \mu_{\text{N}} + qE_F \qquad (1)$$

where $E_{\text{tot}}(\text{GaN:O}_\text{N}^q)$ is the total energy derived from a calculation for substitutional O, and q is the charge state of the O donor. E_F is the Fermi level. Similar expressions apply to other impurities and to the various native defects. We refer to Refs. [1] and [3] for a more complete discussion of formation energies and their dependence on chemical potentials.

The Fermi level E_F is not an independent parameter, but is determined by the condition of charge neutrality. However, it is informative to plot formation energies as a function of E_F in order to examine the behavior of defects and impurities when the doping level changes. Results relevant for the present discussion are depicted in Figure 1. For ease of presentation, we have set the chemical potentials equal to fixed values; however, a general case can always be addressed by referring back to Eq. (1). The fixed values we have chosen correspond to Ga-rich conditions [$\mu_{\text{Ga}} = \mu_{\text{Ga(bulk)}}$], and to maximum incorporation of the various impurities, with solubilities determined by equilibrium with Ga_2O_3, Si_3N_4, and Mg_2N_3. For each defect we only show the line segment corresponding to the charge state that gives rise to the lowest energy at a particular value of E_F. The change in slope of the lines therefore represents a change in the charge state of the defect [see Eq. (1)], and the Fermi-level position at which this change occurs corresponds to a transition level that can be experimentally measured.

3. Anion vacancies

3.1 Nitrogen vacancies in GaN

Our first-principles results for native defects show that self-interstitials and antisites are high-energy defects in GaN, and are thus unlikely to occur [1, 4]. Nitrogen vacancies (V_{N}) behave as donors, as seen in Fig. 1: the formation energy of V_{N} exhibits a slope of +1 [see Eq. (1)]. The formation energy of V_{N} is very high in n-type material; V_{N} are therefore unlikely to form in n-type GaN, and hence they cannot be responsible for n-type conductivity.

We have proposed that unintentional impurities such as oxygen and silicon are the actual cause of the observed unintentional n-type doping [5]. Figure 1 shows that O and Si are shallow donors with formation energies much lower than V_{N}; they will therefore readily incorporate during growth. Support for this assignment has come from SIMS studies [6] as well as from high-pressure studies [7]. The latter have shown that oxygen (but not Si) behaves as a DX center in GaN under pressure [8], in agreement with theoretical predictions [9].

Figure 1 shows that the formation energy of V_{N} is significantly lowered in p-type GaN, making it a likely compensating center in case of acceptor doping. Compensation by V_{N} is suppressed when hydrogen is present [10], i.e., in growth techniques such as MOCVD or HVPE. Figure 1 also shows that V_{N} can occur in a 3+ as well as a + charge state, with a transition level within

0.5 eV of the top of the valence band. V_N may therefore be responsible [11, 12] for the blue lines commonly observed by photoluminescence in Mg-doped GaN [13, 14, 15, 16].

Nitrogen vacancies may also be responsible for the persistent photoconductivity effects that have often been observed in *p*-type GaN [13]. The +/3+ transition of V_N is characterized by a large lattice relaxation [4]. Such large differences in relaxation are usually indicative of metastability, which can produce persistent photoconductivity. Here the metastability is associated with the different position of the A_1 state near the valence band in the 1+ and 3+ charge states; this state is occupied with two electrons the 1+ charge state, and empty for the 3+ charge state. The 2+ charge state is always higher in energy than either 1+ or 3+, and thus thermodynamically never stable; this is characteristic of a so-called "negative-*U* defect".

Finally, we note that the appearance and disappearance of photoluminescence (PL) lines during post-growth annealing of Mg-doped layers grown by MOCVD [17, 18] may be related to the interactions of H with V_N. Complexes between hydrogen and nitrogen vacancies can form during growth [12]; the calculated binding energy of the $(V_N\text{-H})^{2+}$ complex, expressed with respect to interstitial H^+, is 1.56 eV. Dissociation of this complex, producing isolated nitrogen vacancies, may explain the behavior of PL lines during annealing for acceptor activation.

3.2 Nitrogen vacancies in AlGaN

The behavior of V_N in AlN is qualitatively very similar to GaN [19]. However, the +/3+ level occurs at a higher position in the band gap in the case of AlN (around 1 eV, consistent with a roughly constant position of this deep level across the GaN/AlN interface, assuming a valence-band offset of 0.7 eV). Because the formation energy decreases much faster with decreasing E_F in the 3+ charge state, V_N becomes much more favorable for low Fermi-level positions in AlN.

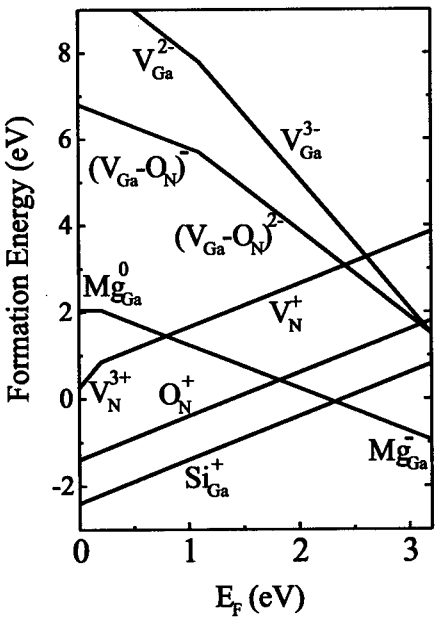

Figure 1: Formation energy *vs.* Fermi energy for important native defects and impurities in GaN. The zero of E_F is located at the top of the valence band, and Ga-rich conditions are assumed.

3.3 Anion vacancies in other compounds

Anion vacancies in compound semiconductors tend to behave as donors, and thus compensate *p*-type material. The negative-*U* character and large lattice relaxation have also been observed for the As vacancy in GaAs [20]. One may wonder why V_N in GaN behaves as a shallow donor, while V_{As} in GaAs only gives rise to deep levels. The explanation lies in the significantly smaller lattice constant of GaN. When an anion vacancy is formed, four deep levels are introduced in the band gap which arise from the four dangling bonds on the neighboring cations. In the neutral charge state, three electrons need to be accommodated in these levels (since each Ga dangling bond contributes 3/4 electron). In GaAs, the Ga neighbors are far enough apart to only weakly interact; but in GaN, the Ga atoms are much closer together, and their strong interaction leads to a large splitting of the defect levels [1]: three states (occupied with one electron) are pushed above the conduction-band minimum (giving rise to the shallow-donor character), while the symmetric A_1 state, occupied with two electrons, is pushed close to the valence band.

The negative-U behavior is also observed for anion vacancies in II-VI compounds, e.g., for the Se vacancy in ZnSe [21]. Here, however, each dangling bond on the neighboring Zn atoms only contributes 1/2 electron, leading to a total of two electrons to be accommodated in the defect levels; both of these are accommodated in the A_1 state. This picture immediately makes clear why the oxygen vacancy in ZnO does not behave as a shallow donor, contrary to what has often been assumed. Recent first-principles calculations [22] have indeed shown that V_O has a 2+/0 transition level deep in the band gap. Again, the 1+ charge state is unstable, characteristic of a negative-U center.

4. Cation vacancies

4.1 Gallium vacancies in GaN

Figure 1 shows that gallium vacancies (V_{Ga}^{3-}) have relatively low formation energies in highly doped n-type material; they could therefore act as compensating centers. Yi and Wessels [23] found evidence of compensation by a triply charged defect in Se-doped GaN.

We have proposed that gallium vacancies are responsible for the "yellow luminescence" (YL) in GaN, a broad luminescence band centered around 2.2 eV [24]. The most direct evidence for involvement of Ga vacancies in YL was provided by positron annihilation measurements [25], showing that the concentration of V_{Ga} correlates with the intensity of the YL. Here we briefly review other evidence supporting the assignment of the YL to V_{Ga}; further references to experiment can be found in Ref. [26].

Position of the defect level. Figure 1 shows that the Ga vacancy has a deep level (the 2-/3- transition level) about 1.1 eV above the valence band. Transitions between the conduction band (or shallow donors) and this deep level therefore exhibit the correct energy to explain the YL. Various experiments have linked the YL with a deep level located about 1 eV above the valence band [27, 28]. In addition, the calculated pressure dependence of this level is also consistent with experiment [27]. It is noteworthy that the absorption corresponding to this defect level occurs at a significantly higher energy than the emission; in photoluminescence excitation a broad absorption peak around 2.8 eV was observed [29].

n-type *vs.* p-type. The formation energy of V_{Ga}^{3-} shown in Fig. 1 indicates that the defect will mostly form in n-type material. Experiments have indeed indicated a suppression of the YL in p-type material [30].

Complexing with donor impurities. Figure 1 shows that the formation energy of V_{Ga}-O_N complexes is lower than that of the isolated V_{Ga}. We therefore expect an increase in the YL when oxygen is present. The YL intensity indeed increases in the neighborhood of the interface with a sapphire substrate [29], where the oxygen concentration is also known to be higher [6].

4.2 Cation vacancies in AlGaN

The formation energy of cation vacancies in AlN is lower than in GaN [19]; these vacancies thus form an increasingly important source of compensation in $Al_xGa_{1-x}N$ alloys with higher x. This compensation mechanism competes with DX-center formation [9]: oxygen becomes a deep level (and effectively behaves as an acceptor) when $x > 0.3$. Whether Si forms a DX level at high x is still controversial; if it does not, then compensation by cation vacancies will be the dominant compensation mechanism in the absence of oxygen.

As might be expected, the 2-/3- transition level also shifts higher in the band gap in AlN [31], in agreement with the observed "violet luminescence" [32].

4.3 Role of cation vacancies in diffusion

Phase separation in InGaN quantum wells has been a topic of intense debate. McCluskey *et al.* [33] observed that $In_{0.27}Ga_{0.73}N$ quantum wells exhibited significant phase separation after annealing at 950°C for 8 hours. A broad optical absorption peak around 2.65 eV was found in the annealed material. This peak is reminiscent of the absorption found in Ref. [29] in samples with strong YL, which we attributed to Ga vacancies. We interpret the peak observed in Ref. [33] as evidence for the presence of cation vacancies, which are mediating the diffusion process leading to phase separation.

4.4 Cation vacancies in II-VI compounds

Metal vacancies and their complexes with donor impurities (the so called *SA* (self-activated) centers) are well known in II-VI compounds (e.g., ZnS, ZnSe); similar to cation vacancies in III-nitrides, they act as compensating centers in n-type material. These defects also exhibit features which are strikingly similar to the YL: recombination between a shallow donor-like state and a deep acceptor state, and a broad luminescence band of Gaussian shape [34, 35].

Our calculations for ZnO [22] show that V_{Zn} behaves as an acceptor with a 1-/2- level occurring around 0.8 eV above the valence band. Transitions from electrons in the conduction band to the V_{Zn} level may therefore be responsible for the "'green luminescence" which is frequently observed in ZnO, and is centered between 2.4 and 2.5 eV [36].

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Materials Science Forum Vols. 338-342 (2000) pp. 1567-1570

Nonabrupt Interface Related Exciton Energy Shifts in $GaN/Al_xGa_{1-x}N$ Quantum Dots

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Keywords: Energy Level Shifts, Excitons in $GaN/Al_x\ Ga_{1-x}N$ Quantum Dots, Nonabrupt Interface

Abstract The existence of smooth interfaces was observed to change considerably the confined carriers energy levels and exciton energies in $GaN/Al_xGa_{1-x}N$ quantum dots. The results were obtained within the framework of the effective–mass theory. It was observed a shift of the ground-state exciton energy about 27 meV if a 10 Å wide smooth interface exists in a $GaN/Al_{0.3}Ga_{0.7}N$ dot with 50 Å of radius. This is a realistic case considering that interface widths are actually about this magnitude.

Introduction In the search for better performance of group III nitrides light emitting devices, a lower threshold current density can be achieved through a dimensional decrease of the active layer structure. Synthesis and optical properties of GaN quantum dots (QDs) were reported in the last three years, and the observation of their quantum confined states was possible [1-6]. A striking feature of the GaN QDs photoluminescense spectra is the increase of the inhomogeneous broadening with the reduction of the mean QDs size, an effect which was found to be a combination of a blueshift from the confinement-induced shift of the electronic energy levels, and a redshift from the increased Coulomb energy induced by a compression of the exciton Bohr radius [6]. However, the spectrum of an individual GaN dot investigated by Petersson *et al.* [7] using cathodoluminescense and scanning electron microscopy suggested that the major contribution of the increased photoluminescense half-width is not related to the radius variation between different dots but is intrinsic to each dot. The interface is intrinsic to each dot, and a thickness around 10 Å should be adopted in the calculations because it is comparable to the dot-size fluctuations. Hence, it is expected that nonabrupt interface related effects is a plausible mechanism contributing effectively to the broadening of the luminescense spectra, as well as to the shift of the excitons and confined carriers energy levels. As a matter of fact, the high-resolution transmission electron microscopy of Arlery *et al.* [8] allowed a quantitative characterization of GaN quantum-dot structures in AlN, evidencing the intermixing between GaN and AlN materials in the dots.

The purpose of this work is to present preliminar results on how the existence of nonabrupt interfaces can change the carriers energy levels and the ground-state confined exciton energy in $GaN/Al_xGa_{1-x}N$ quantum dots. It is shown that nonabrupt interface related size fluctuation effects can contribute significantly to the observed photoluminescense broadening [6], as well as to the blue or red shifts of the carriers energy levels depending on the nonabrupt interface localization in respect to the sharp confinement picture.

The Nonabrupt Interface Related Energy Shifts $GaN/Al_xGa_{1-x}N$ QD interfaces are considered to change both in width (W) and in position (α), being localized between R-αW and R + (1-α)W, where R is the dot radius and α the interface localization, whose values are in the interval [0,1]. In this scheme, the interface related dot-size fluctuations on the carriers energy levels and ground-state confined exciton energy can be depicted in a α-W space diagram [9], from which the nonabrupt interface related photoluminescense broadening can be inferred. The description of the interface region is an adaptation to the zero dimensional case of the scheme that Wang, Farias, and Freire

have recently proposed to study interface-related exciton-energy blueshift in $GaN/Al_xGa_{1-x}N$ two dimensional quantum wells [10]. The smooth confinement potential follows from the assumption that the spatial variation of the aluminum molar fraction y(r) changes linearly from zero when $r \leq R-\alpha W$ to x when $r > R + (1-\alpha)W$ in the $GaN-Al_xGa_{1-x}N$ QD interface [9,10].

The two lowest *1s*- and *2p*-like carriers (electron and heavy-hole) energy levels are calculated by solving Schrödinger-like equations with position dependent effective mass in spherical coordinates through a generalization of the multistep method proposed by Ando and Itoh [11]. The confined exciton energy is obtained following a variational and/or an effective potential approach [12]. Numerical calculations are performed for $GaN/Al_{0.3}Ga_{0.7}N$ QDs in the wurtzite phase - see ref. [8] to find the GaN,AlN gap energies and electron and heavy-hole effective masses in the Γ point at low temperatures. The results are obtained for the case $\alpha=1$, which means that the smooth interface is located totally inside the QD, e.g. the smooth interface begins at R-W and ends at the R, the radius that the dot has within the abrupt interface picture.

The interface related blueshift of the confined ground state and first-excited electron energy level is depicted in the top and the bottom of Fig. 1, respectively. It is stronger in the case of small QDs, and increases when the interface becomes wider as a consequence of the reduction of the mean confinement width for the electron. Comparing the left and right panels in Fig. 1, one can observe that the role of the smooth interface is more important in the case of the first-excited state than in the ground state. It is important to remark that interfaces wider than ~ 16 Å in a 50 Å wurtzite $GaN/Al_{0.3}Ga_{0.7}N$ QD can preclude the existence of the first-excited electron energy level. Consequently, even at low temperatures confined excited-state excitons should not exist if the actual smooth interfaces are wider enough. The interface width enhancement due to annealing, for example, should contribute to the disappearance of peaks in the photoluminescense spectra which are related to confined excited-states.

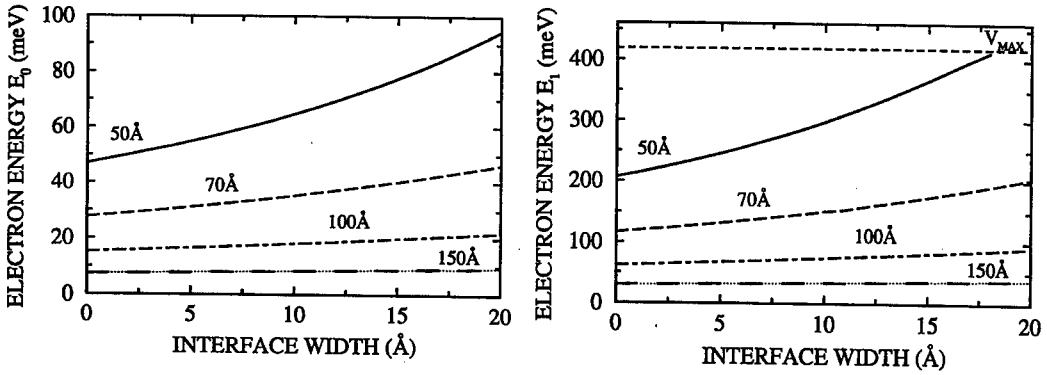

Figure 1 Ground (left panel) and first-excited (right panel) electron energy dependence on the interface width of $GaN/Al_{0.3}Ga_{0.7}N$ QD with radius of 50 Å, 70 Å, 100 Å, and 150 Å calculated considering $\alpha=1$. V_{MAX} is the depth of the electron confinement well in the $GaN/Al_{0.3}Ga_{0.7}N$ QDs.

Figure 2 depicts the confined ground state (left panel) and first-excited (right panel) heavy-hole energy blueshift due to the smooth interface. The interface effect on the confined heavy-hole energy is less strong than in the confined electron energy case since the confinement potential depth of the former is smaller than that of the later. However, due to the effective-mass value, an interface width a little smaller (~ 14 Å) can preclude the first-excited heavy-hole energy level in a 50 Å wurtzite $GaN/Al_{0.3}Ga_{0.7}N$ QD.

The dependence of the confined ground-state exciton energy on the $GaN/Al_{0.3}Ga_{0.7}N$ QD radius with 0 Å (triangles), 5 Å (small dashed), 10 Å (dotted dashed), 15 Å (long dashed), and 20 Å (solid) wide interfaces is depicted in Fig. 3. Although the smooth interface effect on the ground-state exciton binding energy E_b related to the electron-heavy-hole interaction is small (few meV)

[14], the interface related ground-state exciton energy blueshift $\Delta E=E_{exc}(W,\alpha)-E_{exc}(W=0\ \text{Å})$ is very strong. In the inset of Fig. 3, it is shown that a smooth interface of only 10 Å (15 Å) can shift the ground-state exciton energy in a 50 Å $GaN/Al_{0.3}Ga_{0.7}N$ QD by as much as ~ 27 meV (~ 45 meV). This shows that smooth interface related effects in small $GaN/Al_xGa_{1-x}N$ QDs are considerably stronger than in similar $GaAs/Al_xGa_{1-x}As$ QDs [9].

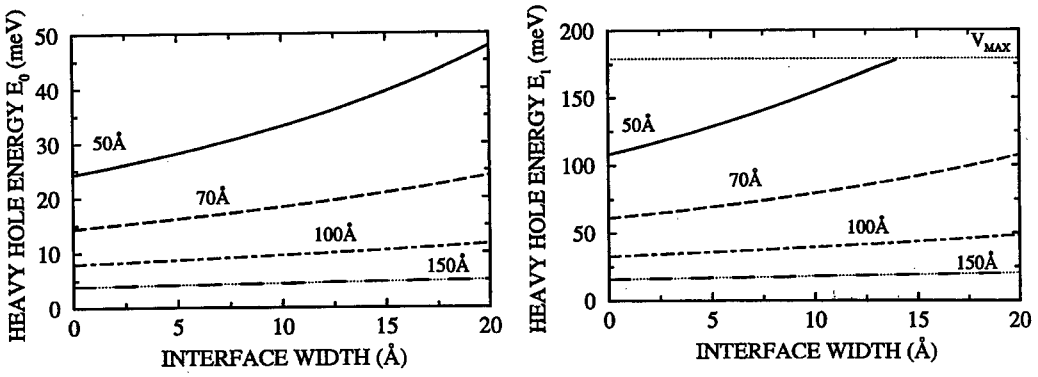

Figure 2 Ground (left panel) and first-excited (right) heavy-hole energy dependence on the interface width of $GaN/Al_{0.3}Ga_{0.7}N$ QDs with radius 50 Å, 70 Å, 100 Å, and 150 Å calculated considering $\alpha=1$.

When $\alpha=0$ the smooth interface is located totally outside the originally sharp QD, e.g. the smooth interface begins at R and ends at the R+W. In this case, when the interface becomes wider the mean confinement width for the carriers increases, generating redshifts of the confinement carriers energy levels and of the ground-state exciton energy, but whose absolute values are smaller (~ 40%) than those of the blueshifts [12]. According the interface related dot-size fluctuations, the energy of the photoluminescense peak due to confined excitons depends not only on the dot radius, but also on the interface width W and localization α. Considering α varying in the range [0,1] and the existence of a 10 Å smooth interface, the peak of the photoluminescense spectrum related to the ground-state confined exciton in 50 Å $GaN/Al_{0.3}Ga_{0.7}N$ QDs should occur in the range [$E_{exc}(W=0)$-16 meV, $E_{exc}(W=0)$+27 meV]. Consequently, a rough estimate of the nonabrupt interface related broadening of the photoluminescense spectra is of the order of 40 meV.

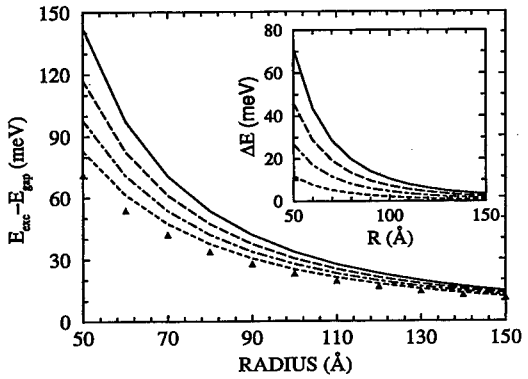

Figure 3 The dependence of the confined ground-state exciton energy on the radius of $GaN/Al_{0.3}Ga_{0.7}N$ QDs with smooth interfaces 0 Å (triangles), 5 Å (small dashed), 10 Å (dotted dashed), 15 Å (long dashed), and 20 Å (solid) wide. The inset shows ground-state exciton energy blueshift $\Delta E=E_{exc}(W,\alpha)-E_{exc}(W=0\ \text{Å})$ related to each interface. $\alpha=1$ and E_{gap} is the GaN gap energy.

A drawback of this work is that the strong internal electric-fields occuring in (Al,Ga)N/GaN structures were not considered [13], whose origin was ascribed predominantly to spontaneous polarization effects rather than a piezoelectric effect in the GaN confinement material. Recently, an enormous (500 meV) redshift of the photoluminescense peak from GaN self-assembled quantum dots was assigned to internal electric-fields [14].

Conclusions The results presented in this work allow to conclude that nonabrupt interface effects must be considered for a better understanding of the optical properties of $GaN/Al_xGa_{1-x}N$ QDs. The interface related broadening of the photoluminescense spectra can be as important as the size fluctuation broadening. Further work is in progress to compare polarization and interface effects in $GaN/Al_xGa_{1-x}N$ quantum wells and dots, and to explore the α-W space diagram as an efficient way to furnish information concerning the interface related broadening of the photoluminescense spectra in $GaN/Al_{0.3}Ga_{0.7}N$ QDs.

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Materials Science Forum Vols. 338-342 (2000) pp. 1571-1574

Radiative Recombination in InGaN/GaN Multiple Quantum Wells

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Keywords: InGaN MQW, Photoluminescence, Surface Roughness, Time-Resolved

Abstract. Optical spectra were studied for several sets of InGaN/GaN multiple quantum well samples, grown with MOCVD at different conditions. One set of samples was prepared with the InGaN layers grown at 700 C, and the GaN barriers at 1000 C, another set was grown under conditions 780 C and 1000 C, respectively. A third set of samples was grown at 820 C for both barrier and well material. These sets of samples show fairly different spectral properties, the two former have rather broad single peak spectra, while the latter shows multiple peak spectra. The piezoelectric field is important in governing the recombination properties, as is also the localization potentials, in particular for the lower InGaN growth temperatures. For the 820 C samples we suspect that a surface roughness affects the center QWs causing additional PL transitions.

Introduction

In_xGaN_{1-x}/GaN multiple quantum well (MQW) structures provide an important active medium for the violet III-Nitride lasers [1]. Consequently the recombination processes in these structures are of considerable interest. It has recently been claimed that the broad spontaneous photoluminescence (PL) emission spectra in these structures are due to an inhomogeneously broadened envelope of excitonic emissions from "quantum dots" (QDs) [2]. These QDs are supposed to consist of regions of a size 3-5 nm having a bandgap much lower than the alloy matrix, due to segregation of In during growth [2]. Other recent work points towards the importance of the piezoelectric field as the dominant mechanism governing the electronic energy levels and the recombination processes in these QW structures [3,4]. In this work we report on a study of the recombination dynamics in $In_{0.15}Ga_{0.85}N$ MQWs over the temperature range 2 - 300 K. The PL emission properties of samples grown at different growth temperatures for the InGaN layers has been studied in detail. The QD exciton model in the specific form of Ref. 2 is not confirmed in our samples, although clearly carrier localization is important. Multi-peak PL spectra as reported in Ref 2 are only observed in samples where the GaN barriers are grown at low temperatures (820 C). The piezoelectric (PZ) field has a strong effect on the recombination, but potential fluctuations are also strong, even for low InGaN growth temperatures (like 700 C).

Category	A	B	C
Barrier GaN			
Width	6.0 nm	6.0 nm	4.6 /6.8/9.4/14
Tg °C	1000	1000	820
Well InGaN			
x	0.15	0.15	0.15
Width	3.0 nm	3.0 nm	2.3/3.4/4.7/7.0
Tg °C	700	780	820
Periods	5	5	9/6/5/3

Table 1. Description of structure and growth conditions for the studied samples in the three different categories.

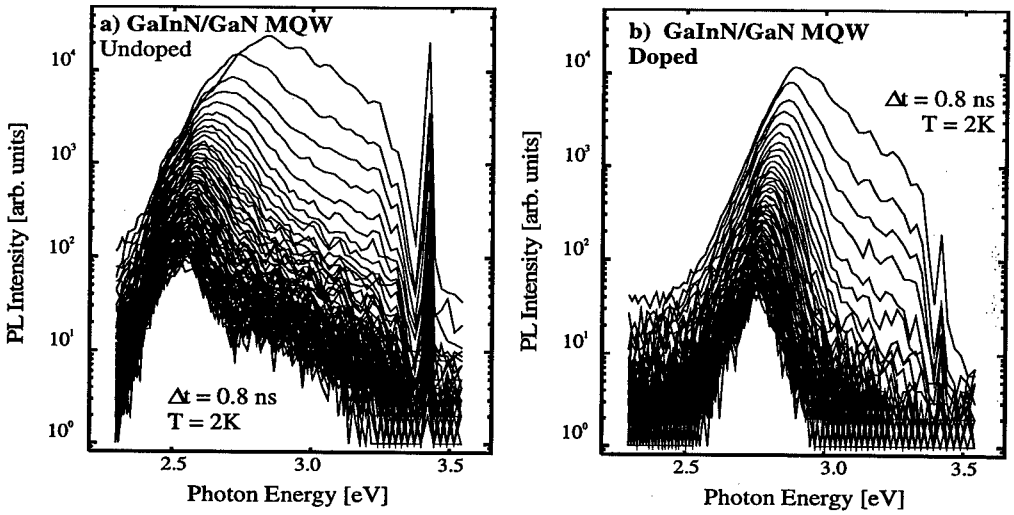

Figure 1. Low temperature time resolved photoluminescence spectra of two different InGaN/GaN MQW structures, where the sample in a) is nominally undoped while the sample in b) is doped with Si in the QW. The time delay between each successive spectra is 0.8 ns.

Samples and experimental procedures

For two sets of samples the $In_xGa_{1-x}N$ MQWs comprising 5 nominally identical QWs were grown with MOCVD with an In fraction x about 0.15. The QW thickness was 3.0 nm, with a GaN barrier thickness of 6.0 nm, (see Table 1). The detailed growth procedures have been described elsewhere [5]. The GaN barriers were grown at high temperatures (about 1000 C), while the growth temperature of the InGaN layers was lower, 700 C for one set (A), 780 C for the other (B). In a third set of samples C the growth temperature was 820 C for both InGaN QWs and GaN barriers. For the C samples the barrier width was also twice the well width, but several samples with different well widths were studied. The In composition x for the C samples was x = 0.12.

The spectral PL experiments discussed here involve continuous wave (cw) laser excitation, as well as more advanced transient studies. In the former case we have access to an upconverted cw argon laser (FRED) emitting at 244 nm, together with a 0.32-m monochromator, and a UV-sensitive CCD detector. In both cases we use He cryostats for variable temperature experiments from 2 K to 300 K. For the transient PL measurements we had several UV laser systems available, tunable both above and below the GaN bandgap. For detection we employ photon counting techniques for the time domain 100 ps to 4 μs, and a streak camera for the faster time domain 15 ps to 2 ns.

Timeresolved PL spectra for the MQW samples.

In Fig. 1 we show time-resolved PL spectra for two category A samples at 2 K, one nominally undoped, and the other Si-doped in the QW. The unperturbed QW exciton energy in these samples is about 3.05 eV [6], but the PL peak energy is much lower for both samples. The trend with time delay after pulsed excitation is a clear shift towards lower energy, which can be explained both by the piezoelectric (PZ) field [3,4] and by the presence of rather strong potential fluctuations. The PZ field is expected to be of the order 1 MV/cm in these QWs [3], and will be partly screened by the presence of carriers, both photoexcited and those from doping. The carriers will also screen the potential fluctuations, however, in particular for potentials of short range (of the order 10 nm) [7]. Therefore the detailed modeling of the recombination involves carrier (or exciton) recombination in a skewed potential due to the PZ field, and at the same time hopping of carriers (or excitons) occurs

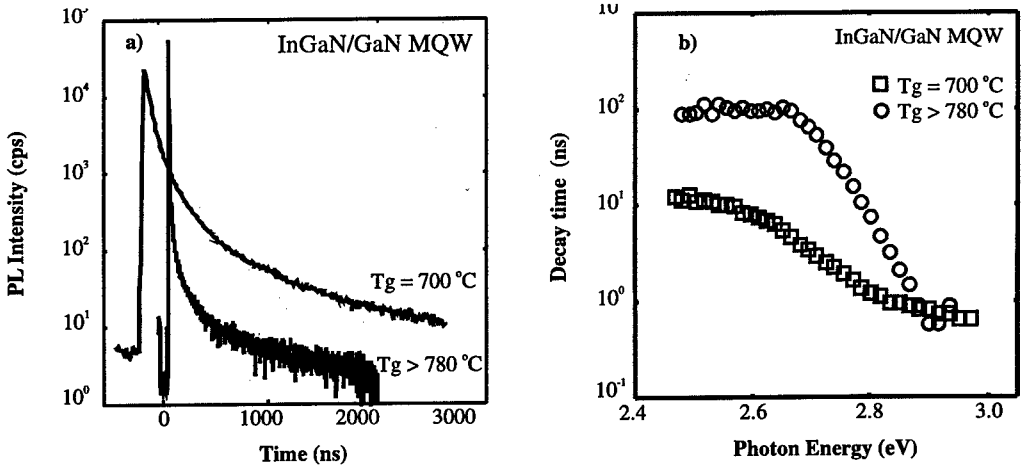

Figure 2. **a)** Typical decay curves at 2.0 K for the main emission from two different samples, with InGaN layers grown at 700 °C and 780 °C, respectively. The decays are non-exponential for both samples. **b)** shows the decay time, defined as the 1/e value of the intensity, as a function of emission wavelength for the two different samples.

between localization potentials of different depth and range. The screening is a dynamic process after an excitation pulse, and the potential (both locally and across the structure) will therefore vary with time during a time-resolved experiment. We shall therefore here only have a qualitative discussion of the processes.

From Fig. 1 is clear that there is a substantial downshift in photon energy of the PL peak with delay time after the excitation pulse, consistent with both the decrease in screening of the PZ field and with a contribution from a hopping process before recombination. In Fig 1 (b) the spectra for the Si-doped sample shows a much higher peak photon energy, mainly attributed to a rather efficient screening of short range localization potentials, since at this doping level the contribution to screening of the PZ field by the donors is small [8]. The conclusion is that the influence of localization potentials and the PZ field on the peak position is of a similar order; while the unscreened PZ field should downshift the peak by about 0.4 eV (Fig 1 (a)), the localization potentials seem to be of a typical size of 0.2 eV, as evidenced also by the rather large linewidth (> 0.1 eV in these samples).

For the category B samples (which were undoped) the PL spectra are quite similar to Fig. 1 (a), with a slightly narrower linewidth. The decay of the PL after the excitation pulse is strongly nonexponential across the entire emission profile, see Fig, 2 (a) for a comparison between the A and B samples. A longer decay time with time delay is expected, due to the increasing PZ field with time. Also, there is a range of lifetimes in the recombination via localization potentials, contributing to this decay shape. For the purpose of comparing different samples the 1/e decay time was recorded for different samples. As shown in Fig 2 (b), this decay time at 2 K varies between 20 ns and 150 ns among samples in category A and B. These are the radiative decay times. The value is most easily understood in terms of a recombination process between separately localized electrons and holes, suggesting an efficient impact ionization process of the excitons during the initial relaxation when free carriers are also present [7]. Strongly localized excitons could also have a long radiative lifetime, however.

The properties of the category C samples seem to be different, however. As seen in Fig. 3 (a,b) the principal PL peak in these samples is typically rather narrow (< 0.1 eV halfwidth, probably of excitonic origin), but there are strong additional peaks at lower photon energy. Part but not all of this structure could be due to interference effects. The different peaks have a different decay time, as

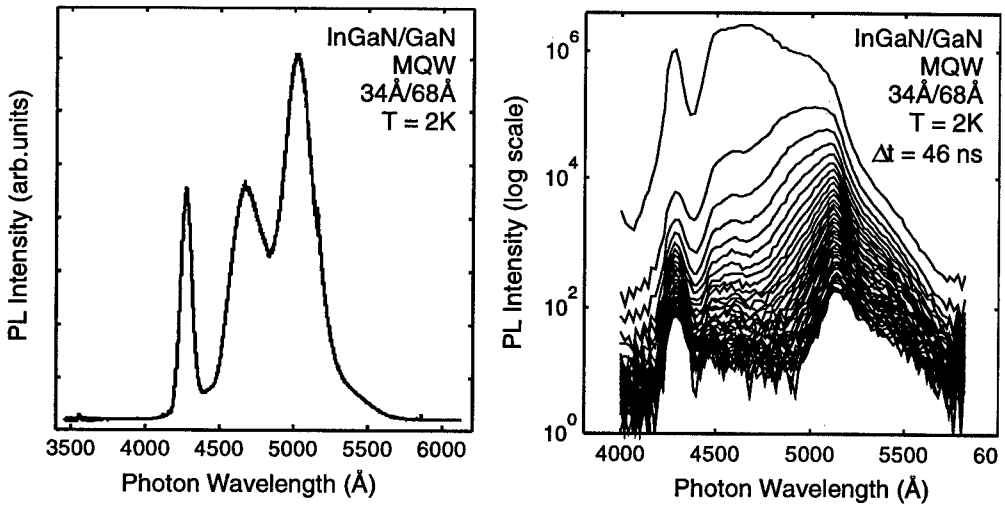

Figure 3. Photoluminescence spectra at 2.0K obtained using CW laser excitation, from a MQW InGaN/GaN sample grown at 820 °C. b) Time delayed spectra for the same sample. Each spectra is measured with a successive time delay of 46 ns after the excitation.

shown in the time-resolved spectra of Fig. 3 (b). The decay is generally faster than for the corresponding samples in category A and B. A typical 1/e decay time for the principal line is about 10 ns, which is shorter than from the samples in Fig 2, which also had a narrower well width. This value could be reasonable for localized excitons in this system; here the localization potentials are shallower, as evidenced by the narrower linewidth.

The additional PL peaks at lower photon energy are only seen in the samples where the GaN barriers have been grown at the same low temperatures as the InGaN layers (i e 820 C). Inspection of these samples with TEM reveals that the surface of the sample is quite rough, due to the development of V-groove defects in the QW stack, for all samples. This means that the inner QWs in the MQW set are normal while the outermost QWs, close to the surface, are strongly affected by the distortion of the structure caused by these defects. This is presumably the reason for the presence of the lower energy PL peaks, which are then related to strongly perturbed QWs close to the surface.

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Materials Science Forum Vols. 338-342 (2000) pp. 1575-1578

Impact of Epitaxial Lateral Overgrowth on the Recombination Dynamics in GaN Determined by Time Resolved Micro-Photoluminescence Spectroscopy

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Keywords: ELOG, Excitonic Luminescence, Micro-Raman Spectroscopy, Time-Resolved Micro-PL

Abstract

Epitaxial laterally overgrown GaN (ELOG) structures are microscopically characterized using cathodoluminescence (CL), micro-Raman spectroscopy and time-resolved micro-photoluminescence. Two ELOG samples consisting of a 3 μm thick GaN buffer layer on (0001) sapphire masked with SiO_2 stripes parallel to <1$\underline{1}$00> and <11$\underline{2}$0> direction, respectively, were investigated. Beside their technological relevance ELOG samples are a superior subject of investigations due to internal gradients in strain and free carrier concentration. To study the influence of the different lateral growth mechanisms on the optical properties of the GaN in the coherently grown and in the overgrown region, we correlate the temporal behavior of the near band gap luminescence with the local free carrier concentration as determined by Raman-spectroscopy. As a result we observe distinct differences in the decay times of the near band gap luminescence for the two different samples as well as for different regions within one sample. The near band gap emission changes from excitonic luminescence to band-to-band recombination depending on the distance from the interface as evidenced by micro-photoluminescence. Beside these drastic changes we also observe a change in decay times in the region of excitonic emission correlated with the donor concentration which leads to a different influence of the coulomb screening effect.

The group-III Nitrides and its related ternary alloys have been growing to the most promising material for light emitting diodes and laser diodes in the UV and blue spectral range [1]. Recently, laser diodes with an estimated lifetime of more than 10 000 hours were reported and are now available commercially [2]. To achieve such lifetimes necessary for commercial application the introduction of the epitaxial lateral overgrowth (ELO) technique was claimed to be effective. This method has already been applied successfully in reducing dislocation density by at least 3-4 orders of magnitude compared to that of bulk GaN (approx. 10^{10} cm^{-2}) [3,4]. It was shown that lateral overgrowth of GaN leads to a direct improvement of quality of the InGaN multi-quantum well structures due to the elimination of dislocations [5].

The ELOG samples investigated here are schematically depicted in Fig. 1a and 1b. A 3 μm thick GaN layer was grown by metalorganic vapor phase epitaxy (MOVPE) on a (0001) sapphire substrate and patterned with 120 nm thick SiO_2 masks parallel to the <1$\underline{1}$00> (sample A) and <11$\underline{2}$0> (sample B) direction. The width of the openings and the stripes are 10 μm each. This structure was subsequently

overgrown with a 50 μm thick GaN layer deposited by hydride vapor phase epitaxy (HVPE) through the windows in the SiO_2 masks on the underlying MOVPE GaN layer. Details of growth are given elsewhere [6].

The setup for the micro-PL and cathodoluminescence experiments are described in Ref. 7 and 8, respectively. The micro-PL measurements having a spatial resolution better than 600 nm were carried out in backscattering geometry using a glass fiber. The photoluminescence signal was analyzed in a 0.35 m subtractive double spectrometer and detected by a microchannel plate photomultiplier. For time resolved measurements a single photon counting setup was used with a 50 ps FWHM response to the laser pulse. Employing convolution techniques the overall time resolution is enhanced to 15 ps. A frequency-doubled dye laser pumped by a Nd:YAG was used for excitation.

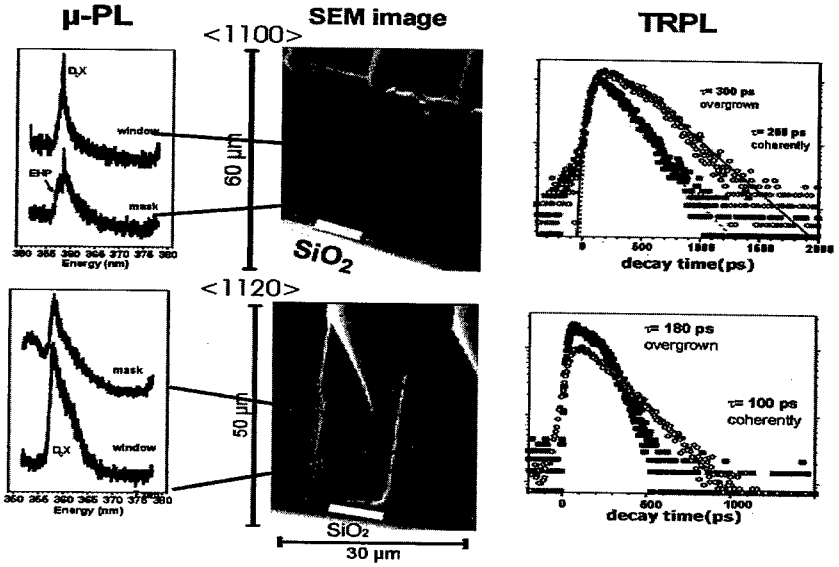

Fig. 1: Comparison of micro-PL, the SEM pictures and transients taken at the different areas, i.e. the coherently grown region and the overgrown region of the ELOG samples A (<1100>) and B (<1120>)

In Fig. 1 two cross-section SEM images are shown. We distinguish between the coherently grown and the overgrown regions, i.e. window and mask region, respectively. The micro-PL spectra for the different areas are shown on the left hand side of the Fig. 1. The changes in linewidth and energy are clearly observable. From these measurements and CL results it was found, that the coherently grown region of sample A exhibits a uniform monochromatic rectangle up to the surface where a sharp excitonic luminescence at 358.6 nm dominates the spectra, whereas for sample B a triangle of excitonic luminescence of approximately 10 μm in height is formed. In the area on top of the SiO_2 masks, i.e. in the coalescence region, the luminescence is strongly redshifted, indicating the strong impact of defect mediated effects. For a more detailed discussion of the CL results refer to Ref. 9 and 10. On the left hand side of the Fig.1 we present results of time-resolved micro-photoluminescence for the two different regions of both samples.

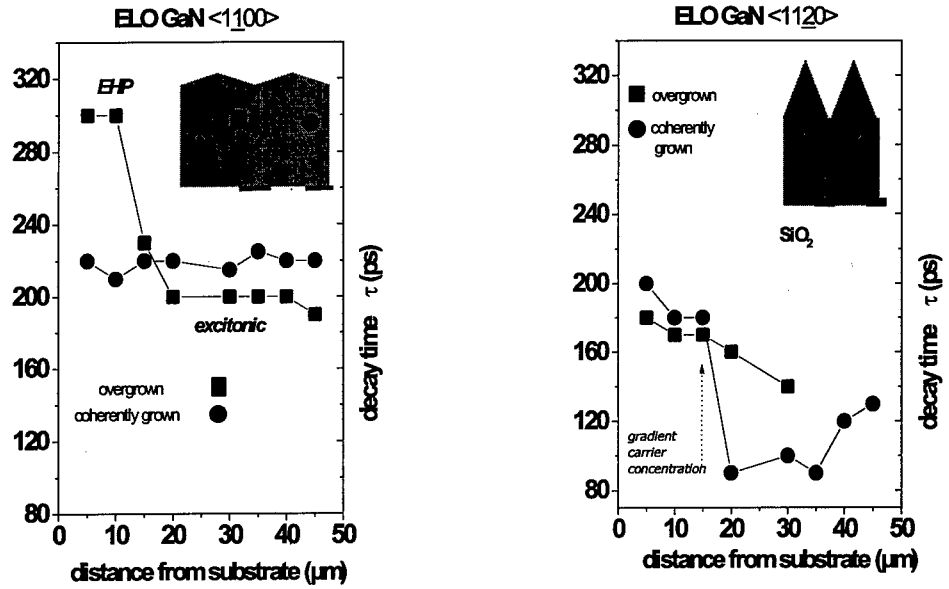

Fig. 2 : Results of the micro-TRPL in dependence on the distance from the substrate for sample A (right hand side) and sample B (left hand side)

The results of the time-dependent PL measurements are collected in Fig.2 for the sample A and sample B, respectively. In Fig. 2 the decay time of the near band gap emission are shown as function of the distance from the substrate interface. The decay time of the excitonic luminescence in the coherently grown region (solid circles) remains constant at 220 ps within the experimental accuracy. In this region the free electron concentration is below the detection limit of our method and all data points are set to $1x10^{18}$ cm^{-3} [10]. In the overgrown region of sample A the time constants (solid squares) are almost constant with decreasing distance from the substrate but sharply increased from 200 ps to 300 ps at 10 μm above the masks. In the same region a jump in free carrier concentration from $9x10^{18}$ cm^{-3} to $1.4x10^{19}$ cm^{-3} occurs. Therefore the temporal behavior can be understood, if assuming that the high free carrier concentration causes a change from excitonic to non-$\underline{k}$-conserving band-to-band recombination. As known from highly doped wide-gap semiconductors as CdS:In, a sharp increase to longer decay constants is observed above the Mott-density [11]. This is because the band-to-band transition probability is smaller than the exciton transition probability, though slower decay times are expected.
The recombination dynamics of sample B is summarized in the upper part of Fig. 3. In the overgrown region the decay time is slightly increased from 140 to 180 ps as one approaches the substrate interface. Above the masks the transient is composed of the dynamics of band-to-band transitions and excitonic processes. The influence of band-to-band processes is reduced with distance from the masks and the faster excitonic processes dominate the decay. The free carrier concentration remains constant at $9x10^{18}$ cm^{-3} in this region.
In the coherently grown region the decay time is reduced from 130 ps near the surface to 90 ps at 20 μm from the substrate with decreasing distance from the substrate. At 15 μm from the substrate a sharp increase to time constants of 200 ps is observed. This can be explained by an increased number of incorporated impurities, changing the free carrier concentration from $9x10^{18}$ cm^{-3} to $1.3x10^{19}$ cm^{-3} when moving towards the substrate. As explained by Rashba and Gurgenishvili [12] the average distance of impurity centers compared to the exciton-impurity complex is reduced, since the number of impurities

is increased. Thus, the higher the impurity concentration, the greater the Coulomb screening on the donor-exciton binding energy. The effective binding energy is lowered and so is the radiative decay time, but the bound exciton complex still exists. This drastically changes at 15 μm from the substrates. The sharp increase in time constant is linked to a drop off in free carrier concentration from $1.3x10^{19}$ to $1x10^{18}$ cm^{-1}, obtained by micro-Raman experiments at this point, within the experimental accuracy.

Summarizing our results, we microscopically characterized two ELO GaN samples with different orientations of the SiO_2 masks in a comprehensive manner. From our findings we identified the different growth regimes: the coherently grown region of sample A (masks along <1$\underline{1}$00>) shows perfect excitonic micro-luminescence, i.e. high crystallographic quality and low carrier concentration up to the surface. This is confirmed by long decay times of 220 ps which are almost unchanged along the cross section. In the ELOG sample B we observe a sharp decrease of the decay times from 180 ps to 90 ps above the low impurity region which corresponds to the heights of the triangle in the CL image in Fig.1d. Above this point the declining impurity concentration leads to a reduced exciton screening and longer time constants.

The drastic change of the time constant at 10 μm from the substrate interface in the overgrown region of sample A is explained by a change in the origin of the recombination from excitonic to band-to-band recombination. The influence of many-particle processes accounts for the carrier dynamics in the overgrown region of the <11$\underline{2}$0> sample as well.

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Structured Ultrafast Carrier Drift Velocity in Photoexcited Zincblende GaN

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Keywords: Photoexcited Zincblende GaN, Structured Overshoot, Ultrafast Transport Transient

Abstract A theoretical study is performed on the ultrafast transient transport properties of photoexcited carriers in zincblende GaN subjected to electric fields up to 120 kV/cm. Depending on the photoexcitation degree, the subpicosecond electron and heavy-hole drift velocity evolution towards the steady state presents maxima and minima, *e.g.* a structured transient. Since nonequilibrium phonon effects are not included, the structured ultrafast carrier drift velocity is explained through the crossover of the evolution curves for the transport and momentum relaxation times, whose definition is based on the nonequilibrium variables used to describe the system.

Introduction Nitride based semiconductors (GaN, AlN, InN and their alloys) are attracting considerable attention due to the blue light emission properties of their heterostructures. However, there is still a lack of studies concerning GaN (the confinement material in most cases) bulk properties. High-field transport investigations addressed mainly steady-state phenomena [1-11], and only recently the transient regime begun to be studied [12-14]. Basic research on the ultrafast transport transient of hot GaN carriers is of relevance since the overshoot effect could be a relevant factor for technological applications in the sub-micron device domain. Overshoot effects were shown to be present during the drift velocity transient stage of electrons in GaN, AlN, and InN initially subjected to equilibrium conditions [12-14].

The study of photoexcited carriers in nitride based semiconductors can furnish informations on both their carrier and phonon dynamics properties, which are important to a better deviced design [15-16]. In this work, it is addressed an analysis of the ultrafast transport properties of photoexcited carriers in zincblende GaN subjected to electric fields up to 120 kV/cm.

Transport Transient in Photoexcited Zincblende GaN A zincblende GaN sample, where a concentration n of electron-hole pairs is created by an intense pulse of laser light, is considered. The photoexcited carriers are far from equilibrium with the lattice, but become thermalized between themselves by Coulomb interaction after a fraction of picosecond. A constant electric field E is applied to the sample accelerating the carriers, which at the same time relax energy and momentum to the phonon field. The sample is in contact with a thermal reservoir at temperature T_o. The optical phonons are heated up in scattering events involving Fröhlich and potential deformation interactions with the carriers, but the acoustical phonons are only slight warmed up.

The following variables are choosed for the description of the nonequilibrium thermodynamic state of the system: the reciprocal of the carriers quasi-temperature [$\beta_c(t)$], of the

optical longitudinal and transversal phonons [$\beta_{LO}(t)$ and $\beta_{TO}(t)$, respectively], and of the acoustic phonons [$\beta_A(t)$] (which is taken as a constant equal to $1/T_B$), the variables $-\beta_c(t)\mu_e(t)$ and $-\beta_c(t)\mu_h(t)$ ($\mu_{e(h)}$ is the electron (hole) chemical potential), and $-\beta_c(t)v_e(t)$ and $-\beta_c(t)v_h(t)$ ($v_{e(h)}$ is the electron (hole) drift velocity). The nonlinear coupled set of integro-differential generalized transport equations that govern the time-evolution of these eight nonequilibrium thermodynamic variables follows from the nonlinear quantum kinetic theory which is based on a nonequilibrium statistical ensemble algorithm [18], and the Markovian approximation is used [19].

The equations for the carriers drift velocities can be transformed into the following equivalent integral equation [20]:

$$|v_a(t)| = (e/m_a)\tau_a(t)E \quad , \tag{1}$$

where a=e or h for electron or hole, respectively. It has a non-linear Drude-type form with an instantaneous relaxation time for transport given by

$$\tau_a(t) = e^{-\psi_a(t)} \int_0^t dt \; e^{\psi_a(t')} \quad , \tag{2}$$

where $\psi_a(t) = \int_0 dt' \gamma_a(t')$, and $\gamma_a(t)$ is the reciprocal of the instantaneous relaxation time of the carriers linear momentum resulting from collisions with phonons, that depends on the quasi-temperature and drift velocity of the hot carriers.

Maxima and minima of the drift velocity in its transient regime should be observable depending on the evolution of the nonequilibrium macroscopic state of the photoexcited carriers in zincblende GaN. In fact, at a time, say t_{ex}, v(t) has an extremal value, it follows that $\tau_a(t_{ex}) = 1/\gamma_a(t_{ex})$, and the extremum is a maximum or a minimum if the second derivative $-(e/m_a)E\tau_a(t_{ex})d[\gamma_a(t)]/dt|_{t_{ex}}$ is negative or positive, respectively. Consequently, the following criterion can be stated [20]: for a zincblende GaN sample arbitrarily away from equilibrium and in the presence of an electric field, a maximum (minimum) in the carriers drift velocity occurs whenever there exist a crossover of the evolution curves for transport time, $\tau_a(t)$, and momentum relaxation time, $1/\gamma_a(t)$, and the latter is decreasing (increasing) at the crossover.

The Structured Ultrafast Carrier Drift Velocity To have an idea on the conditions necessary for the existence of a structured ultrafast carrier drift velocity in photoexcited zincblende GaN at the lattice temperature T_B=300 K, the calculations were performed considering the case of photoinjected carriers with a concentration 1.0×10^{18} cm^{-3}, with an excess energy of 1.2 eV (to avoid intervalley scattering) per pair gained in photon absorption processes. After Coulomb thermalization, the initial carriers temperature $T_c(0)$= 4640 K. The zincblende GaN parameters used in the numerical solution of the coupled quantum transport equations are those of a recent investigation of the hot electron dynamics in zincblende and wurtzite GaN [21].

The left and central panels of Fig. 1 display, respectively, the evolution of electron and hole drift velocities. After a transient roughly of the order of half picosecond, a steady state sets in. During the transient, it can be noticed the predicted behavior of the maxima and minima existence, with one of the maxima corresponding to a velocity drift hole overshoot for fields larger than roughly 20 kV/cm. The right panel shows the evolution of the nonequilibrium temperature of the carriers, describing a very rapid process of relaxation of energy to the lattice. Only at very high fields a weak structure in its evolution can be discerned.

It is important to remark that, since nonequilibrium phonon effects are not taken into account [22], the structured ultrafast carrier drift velocity in photoexcited zincblende GaN is explained in this work uniquely through the crossover of the evolution curves for the transport and

momentum relaxation times, whose definition is based on the nonequilibrium variables used to describe the system.

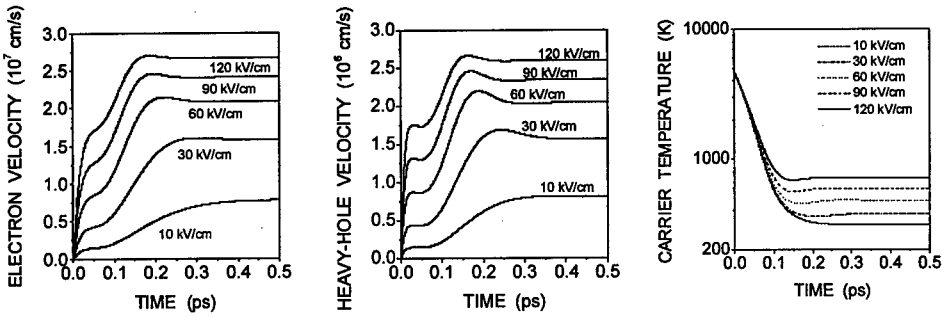

Fig. 1 Time evolution of the electron drift velocity (left panel), heavy-hole drift velocity (central panel), and electron temperature (right panel) in photoexcited zincblende GaN.

Final Remarks A drawback of our assumptions is that a transient transport period in the half picosecond scale requires that the carriers Coulomb thermalization should have followed in the tem-fold femtosecond scale. Thus, in GaN (and also in the others nitride compounds) the strong polar interaction (Frölich's carrier-phonon interaction) leads to relaxation times for the carriers excess energy out of the equilibrium comparable with the one resulting from the carier-carrier Coulomb interaction. This means that one must include as basic macroscopic quantities the population of the carriers in the different band-energy states, and to carry out the joint calculation of relaxation effects due to carrier-carrier Coulomb interaction and carrier-phonons interaction. Further work is in progress to derive the corresponding theory and numerical calculations [23].

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Characterization of Thick GaN Layers Using Guided Optical Waves

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Keywords: Guided Optical Mode, Layer Thickness, Prism-Coupling Method, Refractive Index

Abstract. The propagation of guided optical modes in comparatively thin and thick GaN layer-on-sapphire substrate structures has been experimentally studied. The thickness and ordinary and extraordinary refractive indices of GaN layers were extracted from the comparison of the measured effective refractive indices of the modes with the solutions of characteristic equation for a planar optical waveguide.

The propagation of guided optical waves in GaN layers can be employed as a tool for determining important layer parameters. Measurements of effective refractive indices of guided optical modes enable us to evaluate simultaneously the thickness and the refractive index of the layer. Moreover, from the analysis of guided modes spectra, the homogeneity of refractive index along layer thickness can be estimated. Most of the studies of guided optical modes in GaN layer-on-substrate structures have been performed for layer thicknesses not exceeding 1-2 μm [1,2]. In the present report, we investigate the guided optical waves propagation in thick (near 6 μm) GaN layer-on-sapphire substrate structures and compare the results with those obtained in structures with thinner (close to 1 μm) layers.

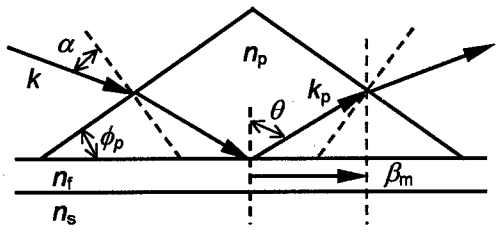


Fig.1. Geometry of n_m measurements. k and $k_p = n_p k$ are wave numbers of light wave in free space and prism material, respectively; $\beta_m = n_m k$ is propagation constant of guided optical mode.

The GaN layers were grown by low pressure MOCVD on (0001) sapphire substrates. Two samples, G2 and G3, with *i*-GaN layers of different thicknesses as well sample G4 with Si:GaN layer has been investigated. The effective refractive indices of guided optical modes were measured by the prism-coupling method [3] as shown in Fig. 1. Coupling the light of He-Ne laser into GaN layer using a GaP prism excited the guided optical modes. Phase matching conditions, necessary for excitation of a particular mode, were satisfied by rotating the sample on the goniometer, which enabled to perform high precision angle measurements. Observing the mode pattern on the screen at the prism output indicated the excitation of the mode. The effective refractive indices of guided modes are found from the expression

$$n_m = \sin\alpha_m \cos\phi_p \pm \left(n_p^2 - \sin^2\alpha_m\right)^{1/2} \sin\phi_p \ , \qquad (1)$$

where α_m is the incidence angle for given mode, ϕ_p is the prism angle, and n_p is the refractive index of prism material. In our experiment, at the optical wavelength 632.8 nm, the value of the latter was 3.305. The plus sign in Eq.1 corresponds to the case shown in Fig.1, and the minus sign is for the case of light incidence at the opposite side of the normal to the prism-air interface. Two sets of modes with different polarization, TE and TM, have been studied. The values of effective refractive indices measured in two samples, G2 and G3, are plotted as a function of mode order number, m, in Fig.2. Waveguiding GaN layer in sample G2 as well as in G4 supported several TE and TM modes, whereas the layer in sample G3 supported numerous modes. Difference in numbers of modes observed clearly indicates the considerable difference in layer thicknesses. Though several highest modes were hard to distinguish, the values of their effective refractive indices could be reconstructed by using the polynomial approximation for the experimental $n_m(m)$ dependence. These values are marked in Fig. 2 by crosses or stars. As our analysis showed, however, their accounting for or neglecting had no significant influence on the results obtained.

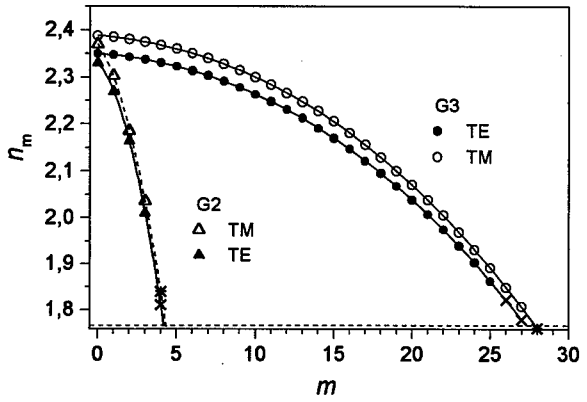


Fig.2. Effective refractive indices of guided optical modes versus mode order. Dots represent experimental values; lines, polynomial approximations of measured dependences. Extrapolated values are shown by crosses for TE, and by stars for TM modes. Abscissa corresponds to extraordinary refractive index of sapphire substrate, and horizontal dashed line shows its ordinary index.

Using the measured values of effective refractive indices, the parameters of GaN film, thickness and refractive index, could be evaluated. The thickness of step-like waveguide can be expressed from the characteristic equation for guided modes as a function of the refractive index of film material, n_f , and the effective refractive index of guided mode, n_m :

$$d = \frac{\lambda}{2\pi\left(n_f^2 - n_m^2\right)^{1/2}}\left\{m\pi + \arctan\left[\left(\frac{n_f}{n_s}\right)^{\gamma}\left(\frac{n_m^2 - n_s^2}{n_f^2 - n_m^2}\right)^{1/2}\right] + \arctan\left[n_f^{\gamma}\left(\frac{n_m^2 - 1}{n_f^2 - n_m^2}\right)^{1/2}\right]\right\} \qquad (2)$$

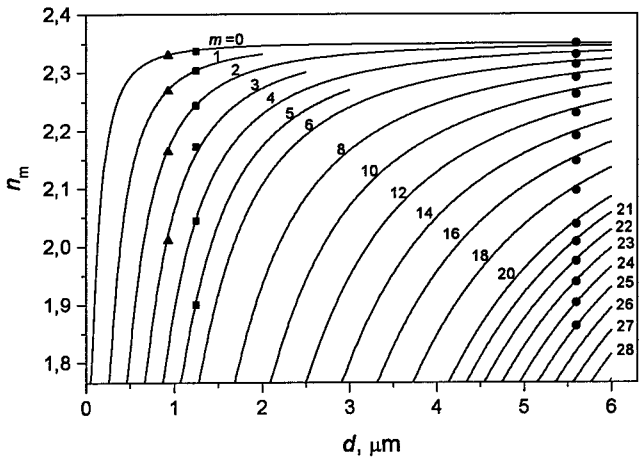
where γ=0 for TE modes, and γ=2 for TM modes, λ is the optical wavelength in a free space, m is the guided mode order, and n_s is the refractive index of the substrate material. The latter is the ordinary refractive index of sapphire, n_o=1.7661, for TE modes and the extraordinary one, n_e=1.7580, for TM. The calculations of d are performed for all layer modes by substituting adjustable parameter n_f, which is increased in steps starting from the value slightly exceeding the highest value of the mode index (zeroth-order). If the n_f value is chosen properly, the same thickness value should be obtained for any mode. In reality, however, due to measurement errors and possible deviations of the refractive index profile from ideal steps, a certain dispersion of thickness values corresponding to different modes at the same n_f appears. The spread in the results is characterized by the root-mean-square deviation

$$\sigma = \left[\frac{1}{M}\sum_{m=0}^{M-1}\left(d_m - \langle d\rangle\right)^2\right]^{1/2}, \qquad (3)$$

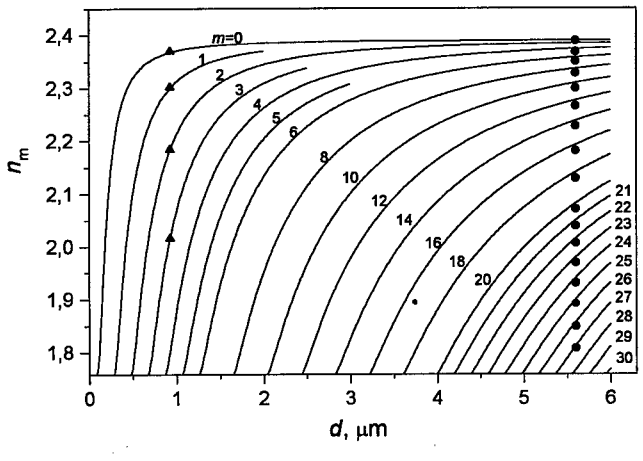
where d_m is the thickness value obtained for the m-th mode, the mean value of the thickness is

$$\langle d \rangle = \frac{1}{M} \sum_{m=0}^{M-1} d_m \ , \tag{4}$$

and M is the total number of modes. The calculation procedure is performed to find n_f corresponding to a minimum value of σ. This value of refractive index and corresponding mean thickness value stand for the searched parameters of the layer. The results obtained for samples used in our experiment are given in Table 1. Only data for TE modes were available for sample G4. For optical axis of GaN oriented normal to the substrate surface, n_f for TE modes is the ordinary index, n_o=2.35, and for TM it is the extraordinary refractive index n_o=2.39. These values, obtained in our experiment, are in a good agreement with the values for GaN films given in [1, 4]. Lower values of the refractive indices were reported in [5].



a



b

Fig.3. Dependences of effective refractive indices of guided optical TE (a) and TM (b) modes on layer thickness. Solid curves for TE modes are calculated with n_f =2.35 and for TM modes with n_f =2.39. Dots represent experimental values, measured in samples G2 (triangles), G3 (circles), and G4 (squares). Numbers at the curves indicate mode order. To not overload the figure, some of the calculated and measured in sample G3 modes are omitted.

Provided the refractive index of layer material is determined, one is able to calculate, using Eq.2, the dependence of the effective refractive index on the layer thickness, $n_m(d)$, for an arbitrary mode. The sets of dispersion curves for TE and TM modes are plotted in Fig.3. The experimentally measured values of the effective refractive indices at relevant depths are also depicted for comparison. In the thinner samples, the agreement for all the modes is very good, indicating the high optical homogeneity of the layers. This could be expected from low values of the RMS deviation obtained (see Table 1). In fact, instead of the described above procedure, any pair of modes is sufficient to evaluate layer parameters

Table 1. Parameters of GaN layers evaluated by RMS deviation minimization procedure

Sample	Number of modes M		Refractive index n_f		Thickness, μm $\langle d \rangle$		Root-mean-square deviation, % σ	
	TE	TM	TE	TM	TE	TM	TE	TM
G2	5	5	2.3496	2.3920	0.92	0.93	0.19	1.32
G3	28	29	2.3504	2.3890	5.36	5.33	4.87	5.34
G4	6	-	2.3478	-	1.26	-	1.62	-

by solving a system of two equations of type Eq.2 with unknowns n_f and d. In contrast, for the thickest sample G3, small discrepancies between measured and calculated values are observed. First, to fit better the dispersion curves, the argument d for the measured set of n_m values had to be chosen 5.6 μm, a somewhat larger value than those given in Table 1. Moreover, so there is no full coincidence between measured points and calculated curves for some of the modes. The relatively large value of the thickness RMS deviation, σ, for this sample is caused not by the enhanced measurement inaccuracy, but rather by the differences in thicknesses "seen" by different modes. This implies that the profile of refractive index in the layer G3 is not an ideal step, even though the deviations should not be very significant. The real profile can be reconstructed by the inverse Wentzel-Kramer-Brillouin (IWKB) procedure [6] what is, however, out of the scope of the present paper and will be addressed in future work.

In conclusion, we have measured by the prism-coupling technique the effective refractive indices of guided optical modes propagating in GaN layer-on-sapphire substrate structures with different layer thicknesses. The thickness and ordinary and extraordinary refractive indices of GaN layers at wavelength 632.8 nm were evaluated from the solutions of characteristic equation for a planar optical waveguide. The obtained results are in satisfactory agreement with the step-like profile model. However, some small discrepancies are observed in 5.6-μm thick sample, which are attributed to the refractive index inhomogeneity along the layer thickness.

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Polarization Memory in Band Edge Luminescence From Free Standing Gallium Nitride

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Keywords: Deformation, Edge Emission, Polarized Light

Abstract

The effect of memory to linear polarization of exciting light was observed in samples of free-standing gallium nitride for the first time. The effect is interpreted as the result of site-selected excitation of luminescence by polarized light in small regions, deformed in various directions in plane of the sample.

Introduction

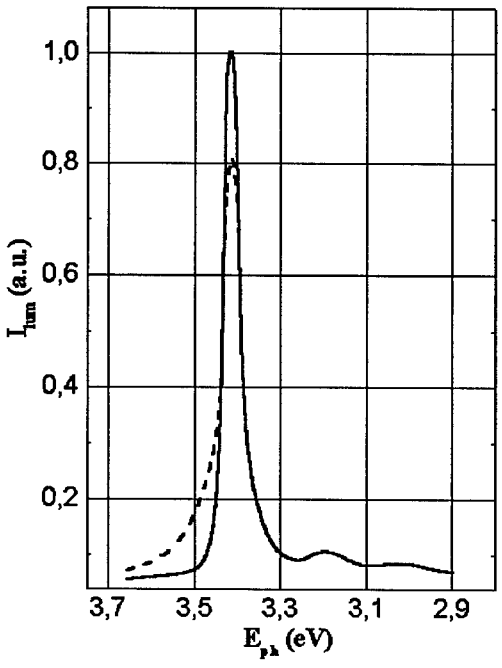
Polarization memory is interesting physical phenomenon, observed in various solid state materials. The effect manifests itself as the dependence of luminescence polarization on the polarization of exciting light. First discovered in ruby, the effect was studied then in various materials, especially in semiconductors. The most known in this field is so called optical orientation effect: circular polarization of luminescence from isotropic materials as the result of circular polarized excitation [1]. The effect has evident physical nature – it is the result of angular momentum conservation of oriented photons. Memory to linear polarization also was observed in so called "hot luminescence" from various semiconductors [2]. Quite recently memory to linear polarization was found in porous silicon, and was explained in assumption of luminescence from asymmetric crystallites [3]. In all the cases above only the dependence of luminescence polarization degree on the polarization of excitation were observed, but any changes in spectra were not found.

Samples and Experiment

The samples for present investigation were free-standing GaN layers, initially grown on sapphire by chlorine gas epitaxy. The free-standing samples had thickness about 0,4 mm ; initial surface of GaN layer was covered by hexagonal microprisms.

Experiments were carried out with the light beam parallel to C_6 axes of material, so the samples and experimental conditions were isotropic in plane, normal to light beam. Luminescence was excited by pulse N_2 laser with the energy of light quanta 3,69 eV . Spectra were registrated separately for parallel and crossed orientation of analyzer and polarizer. This procedure make it possible not only to measure the degree of polarity, but also to study the spectral details. The observed luminescence spectra of samples under study were typical for hexagonal GaN: at 77 K main band 3,45 eV, and a week band near 3,27 eV were observed. 3,45 eV band is the band edge luminescence, and contains the components of different nature; and 3,27 eV band is usually attributed to recombination through the level of residual acceptor.

Results



The effect of polarization memory was observed on a band 3,45 eV at 77 K ; it was absent at room temperature. The effect manifests itself as the dependence of the band profile in luminescence spectra on the correlation of linear polarization directions for excitation and luminescence light.

When the linear polarizer in the exciting beam and linear analyzer in luminescence were crossed, the band in luminescence spectra was nearly symmetric. The form of the band was not Gaussian, it had a broad background (30meV at level 0,1 from maximum), that can be considered as the evidence of essential inhomogeneous broadening. Another band profile was observed with the polarizer and analyzer aligned parallel. In the last case the high energy side of the band became much narrower (up to 3-5 meV at level 0,1 of maximum). Together with the narrowing of the high energy side, some increase of luminescence intensity in band maximum was observed, so that integral luminescence intensity remains approximately the same (see figure). At the same time the intensity and the form of low energy side of the luminescence band remained unchanged.

The authors are not aware about similar effects in any other materials or about any effect of memory to polarization of exciting light in gallium nitride.

Discussion

Let us consider the mechanisms, that can be responsible for the effect observed. The microscopic nature of the effect can not be similar to that of optical orientation or optical alignment effects [2-4]. According to existing models, the linear polarization of luminescence can appear as the result of recombination of the carriers with the total angular momentum value more then $2\pi/h$. As far as gallium nitride has simple electronic band with spin value ½ , the linear polarization of luminescence only can be due to polarization of holes. But, taking in consideration that the excitation in experiment was about 250 meV higher than the observed luminescence, and the high efficiency of momentum relaxation for the holes (or excitons) in the acts of scattering, the initial direction of hole momentum must be relaxed to the moment of the recombination.

The qualitative explanation of the effect can be done in terms of inhomogeneous broadening. According to that, broad background of band in spectra is the result of recombination of holes in some defect regions. Most probably, in our case the cause of the deviation of component position from the center of the band is a deformation. Similar effects are well known for GaN, e.g.[4]. At the same time, due to low difference in energy, we can consider, that components in the wings of the band are of the same nature, as in the band's maximum. The disappearing of high energy side of band together with increase of intensity in maximum means, that excitations from the regions with increased gap energy value migrate to the main, non-deformed material. In frame of this approach unchanged low energy side of the band has evident reason – carriers can not migrate into the main material along the direction of increase of band gap energy. The absence of the effect at room temperature is easy to explain also: the room temperature if high enough for the excitations to get the regions with 30 meV band gap higher, then the main material. As a result, the luminescence from high energy wing can be observed at 300 K.

Necessary to note, that only the considerations on inhomogeneous broadening were used to get the explanation of effect at this stage and no any model assumptions about the sample were made.

The role of light polarization in effect is still to be explained. Let take into account the fact, that used FS GaN consist from microscopic single crystal grains. The grains are known to be deformed in plane of the sample (normally to C6 axis of GaN). As the light beam in experiment is directed along C6, the local deformation of material is the main factor of asymmetry in optical phenomenon in our experiments. Probability of optical transition for most anisotropic materials is much higher, when the electrical vector of the light is normal to the direction of main optical axis. Another words, detection of liner polarized light of luminescence means, that we detect luminescence from the regions with the direction of deformation normal to the electrical vector in detected light. So, in experiment with parallel polarizer and analyzer one detects light

mostly from the same regions, where excitation takes place. Disappearance of high energy side of band in experiment with parallel polarizer and analyzer means, that migration of excitation occur between points of the sample with the same direction of deformation It can happen inside the same crystal grain (domain).

When the polarizer and analyzer were crossed, the decrease of high energy side was not observed. According to our model, it is to mean, that migration of carrier (or excitation) between regions, deformed in different direction, is much weaker, that in previous case – between regions with parallel direction of deformation. This is because the migration between regions with different direction of deformation must include a part of a pass through some kind of boundary regions, with non-uniform deformation. The boundary region should contain higher density of defects, and so the migration through it must be suppressed or at least must be much weaker.

Conclusions

As a result: the effect of polarization memory in photoluminescence of gallium nitride was observed for the first time. It was found, that the profile of luminescence band depends on the correlation between polarization of excitation and luminescence light. The effect differs qualitatively from the known cases of the polarization memory in other semiconductor materials. One can expect, that the new effect will be informative about the details of relaxation processes in GaN. The future investigations will finely clarify the nature of the effect.

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Enhancement of UV-Sensitivity in GaN / GaAs Heterostructures by Si-Doping

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Keywords: Deep Levels, GaN/GaAs-Heterostructure, UV Detectors

Abstract.
Cubic GaN layers prepared by radio frequency plasma assisted molecular beam epitaxy on semiinsulating GaAs (100) substrate were investigated. Si doped n-type GaN films with electron concentrations varying between 10^{14} and 10^{19} cm^{-3} were analyzed. The Si-doping was performed by varying the Si-effusion cell temperatures. In the DC-photocurrent spectra an incorporation of a Si-related shallow donor level of about E_C-35meV was found. The responsivity of the cubic GaN layers enhances with increasing Si-doping, which could be explained by a space charge model. In addition, a higher Si-doping causes an increase of both the time constant of the persistent photocurrent and the deep defect-to-band transitions in the optical admittance spectroscopy.

1. Introduction:

The direct wide gap material GaN is successfully used for optoelectronic devices like high responsivity visible blind UV- detectors [1] light emitting diodes and lasers. Because of their superior radiation hardness, high temperature resistance and high band gap, this material is suitable for operation under extreme conditions and high irradiation fluxes. Applications of these devices in communication, UV imaging, solar monitoring and flame detection have been suggested [2]. Further the spectral region of detection of GaAs or Si- devices can be extended to the UV-region by GaN useful for UV-VIS detectors or solar cells.
The detection properties of cubic GaN deposited on substrates such as GaAs are not well investigated up to now. Especially, the influence of the GaAs-substrate and the quality of the cubic GaN layer on the static (responsivity of the DC-photocurrent) and the dynamic (frequency dependent photocurrent, persistent photocurrent) detection parameters is hardly analyzed. In this paper we investigate the DC- and AC-photocurrent of cubic GaN layers on semiinsulating GaAs substrates in the ultraviolet spectral region as a function of the Si doping level. The results are compared with optical admittance spectroscopy (OAS) measurements, where optical transitions between defects and the corresponding bands are monitored.

2. Experimental details:

Cubic GaN (c-GaN) layers were grown by rf-plasma assisted molecular beam epitaxy (MBE) on semi-insulating GaAs (001)-substrates. N-type doping of the c-GaN was achieved by varying the temperature of the Si-effusion cell between 750 and 1100°C. The resulted carrier concentrations varied from 10^{14} to $10^{19}cm^{-3}$ and was determined by Hall-Effect measurements. Al-layers annealed at 500°C in nitrogen gas and Pt-layer sputtered by a magnetron were used for ohmic contact and Schottky contact on GaN, respectively. The ohmic contact on GaAs was realized by a NiGeAu-layer annealed at 500°C in nitrogen atmosphere. To perform measurements in coplanar contact arrangement both contacts on the GaN-layer were used.
The DC-photoconductivity was detected by a high resistance meter. The spectral responsivity measurements were performed with an UV-VIS grating monochromator and a 75 W Xenon lamp. It was defined by the ratio of the difference of the current under illumination and in the dark, and the incident light power. The samples were illuminated from the GaN-side. A thermopile and a calibrated UV enhanced Si-detector were used for

the determination of the incident light power which is 3.3 μWmm^{-2} at a wavelength of 300 nm. For the measurements of the persistent photoconductivity (PPC) a shutter was introduced into the optical path and the the illumination time was adjusted to 600s. The light power at 350 nm was 5.7 μWmm^{-2} and the time resolution was 100 ms. The time constant of the PPC decay was determined by a stretched exponential function as described in [3]. Optical admittance spectroscopy (OAS) was measured using a HP4284A High precision LCR meter and an UV-VIS-IR grating monochromator. For details of the experimental technique see references [4] and [5].

3. Results and discussion:

The spectral DC-responsivity of the Si-doped c-GaN layers (Fig. 1, top) shows an increase between 250nm and 380nm with increasing Si-concentration (see Fig. 1, bottom left). Furthermore, the peak position shifts to higher energies E_G-E_{peak} with increasing doping level (see Fig. 1, bottom right). At 300K a band gap energy E_G of 3.237eV is used for c-GaN [6]. Taking into account, that this peak is caused by a superposition of various transitions between the bands and defect levels we conclude that the Si doping introduces a shallow donor level of about 35meV below the conduction band. This transition dominates the NBG-peak at higher Si-concentrations. Such values of donor binding energies in cubic n-type GaN are consistent with results of photoluminescence measurements on c-GaN by LIU et al. [7] (55meV) and AS et al. [8] (25meV).

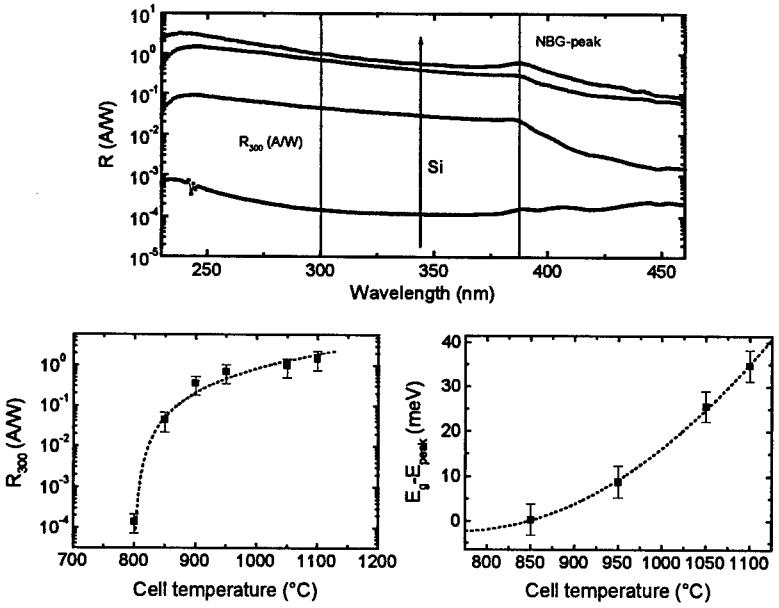

Fig. 1: Spectral dependent responsivity of different Si doped cubic GaN samples (top), the responsivity at 300nm R_{300} as a function of the Si effusion cell temperature (bottom, left) and shift of the difference in energy of the band gap E_G and near band gap (NBG) peak E_{peak} with increasing effusion cell temperature (bottom, right). The spectral dependent responsivity increases dramatically with increasing doping level (bottom, left) showing a saturation at a cell temperature above 900°C.

We assume that the responsivity of the GaAs-substrate is constant within the error limits for all samples. Thus, the increase of the responsivity in the UV-region can be explained by a change of the responsivity in the GaN-layer. One possible explanation for the rising responsivity with increasing doping could be a decrease of

the concentration of deep levels. However, OAS investigations shown in Fig. 2 indicate an increase of the OAS signal above 450nm. These transitions are caused by deep defects at about 2.4..2.8eV (blue band) and at 1.6..2.1eV (yellow band) (the defects in cubic GaN are discussed in detail in [9]). Thus, the concentration of deep levels is higher in the sample with higher Si-concentration and therefore a decrease of the responsivity is expected, which is in opposite to the behavior observed in Fig. 1.

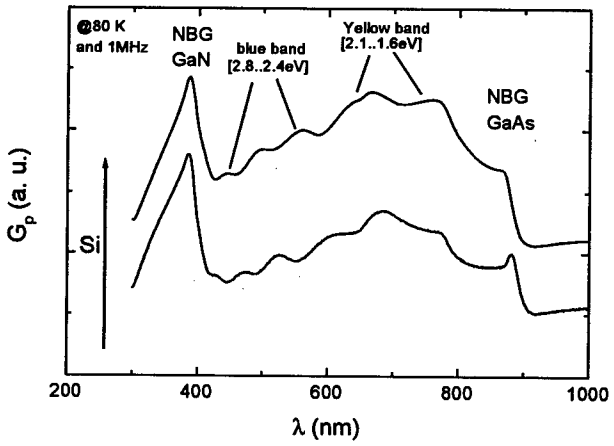

Fig. 2: OAS-spectra of cubic GaN layers with different Si doping levels

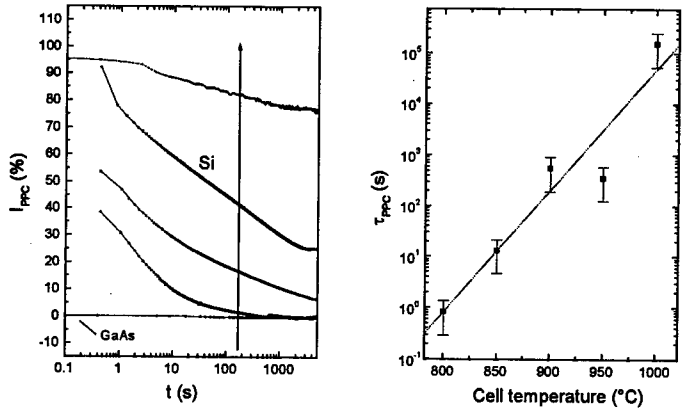

Fig. 3: The normalized PPC-decay of different Si-doped GaN layers and the time constant determined by fitting the PPC decay with an stretched exponential function; the semiinsulating GaAs shows no PPC-effect.

Recently, in Si doped hexagonal GaN and AlGaN another explanation was found for the large doping dependence of the responsivity [10], [11]. Instead of changing the free carrier concentration by photoexcitation a strong variation of space charge regions (SCR) was proposed. Such space charge regions may exist at the GaN surface, at the GaN/GaAs interface, at grain boundaries or around charged dislocation lines. Both photoexcitation and doping can strongly decrease these depletion widths, resulting in an increased conductive volume in the GaN layer and therefore in an increased current flow. Especially for highly doped samples a small change in the cross sectional area leads to a large change in the responsivity. Therefore, we

think that this model is also appropriate to the cubic GaN case. The investigated samples also show a persistent photocurrent (PPC) effect. With increasing Si-doping level the PPC rises slower and the time constant determined by the stretched exponential fit increases (see Fig. 3). This behavior is in contrast to the effects observed in [10] and [12]. In these papers an increase of the doping level leads to a decrease of the PPC effect. The origin of our results can be explained by additional deep levels with low emission rates unintentionally introduced by the Si doping. To ascertain this, additional OAS measurements were made (see Fig. 2). With increasing Si cell temperature additional traps especially in the region of the yellow band were introduced. This traps enlarge the time constant τ of persistent photo conductivity showing again the correlation between the defects of the yellow band and the PPC effect [12], [13], [14].

4. Conclusions:

The photoconductivity behavior of MBE grown n-type cubic GaN-layers on semi-insulating GaAs (001)-substrates was investigated. By changing the Si-effusion cell temperature samples with free electron concentrations between 10^{14} to 10^{19} cm^{-3} were realized. In the DC-photocurrent spectra a shallow donor defect state with a transition energy in the range of about E_C-35 meV. A huge increase of the UV-responsivity of the c-GaN layers with rising Si-doping was observed. OAS measurements excluded that this responsivity improvement was due to a reduction of deep levels. In contrast they showed an increase of the concentration of deep levels with increasing Si concentration. Therefore, only a space charge model was appropriate to explain the UV-responsivity dependence. The increase of the deep defect concentration further results in a longer time constant of the observed persistent photoconductivity with increasing Si concentration.

Acknowledgments

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Materials Science Forum Vols. 338-342 (2000) pp. 1595-1598

Resonant Raman Scattering and the Emission Process in Zincblende-$In_xGa_{1-x}N$

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Keywords: Photoluminescence in c-InGaN, Quantum Dots in c-InGaN, Raman Scattering in c-InGaN

Abstract Resonant Raman Scattering (RRS), and selectively excited photoluminescence (PL), spectra were obtained for cubic c–$In_xGa_{1-x}N$ with x = 0.07, x = 0.19 and x = 0.33. The emission of blue and green light observed at room temperature and T = 30 K, is attributed here to quantum confinement effects due to the self–formation of quantum dots of c–InGaN. The average In content within the dots, $\overline{x}$, was measured directly by a selective resonant enhancement of the Raman scattering. The values for $\overline{x}$ were found to be the same for all samples. This method allowed also the detection of an important composition inhomogeneity of the dots.

Introduction The hexagonal h–$InGaN$ active layers in the Nichia's devices were shown to grow as two dimensional arrays of isotropic, self–formed Quantum Dots (QDs) or dot–like structures that make up just a few percent of the total layer volume.[1] In spite of this low coverage, the dots dominate the emission process due to their efficient trapping of excitons. The binding energy of the excitons, enhanced by quantum size effects, is considered as the key process for achieving low–threshold laser diodes.[2] Furthermore, when the QD size is well designed bi–exciton lasing is also possible.[3] The gain enhancement effect due to bi–excitons should relax the requirements for size homogeneity and coverage of QDs, which means that laser action might be observed even in the case of large size distribution and low dot–density.[3] Experimental data on a large number of h–$InGaN$ diodes and epilayers, lead to a model that attributes the luminescence almost exclusively to QDs.[4] On the other hand, giant piezoelectric effects were proposed to dominate the emission process for larger h–GaN QDs grown on h–AlN .[5] This was found not to be the case, even for the largest h–GaN dots for which the dominating process in emission is the confinement effect.[6] While the h–$InGaN$ optical emission mechanism is a subject of on–going discussion in the literature the c–$InGaN$ has been only sporadically investigated.[7,8] The understanding of the emission, the precursor of laser action, requires further investigation, mainly in the particular case of c–$InGaN$ that is believed to possess potential advantages for the fabrication of InGaN–based devices.

In the present work we investigate the nature of the photoluminescence peak appearing at lower energies than the energy gaps of c–$In_xGa_{1-x}N$ layers. Pursuing this task, resonant Raman scattering experiments using several excitation lines in the blue–green region in order to tune the electronic levels, were carried out. This procedure allowed us to observe a selective resonant enhancement of an extra–peak appearing in between the TO and LO phonon frequencies of the alloy. The occurrence of this resonance shows that the scattering of the extra–phonon is

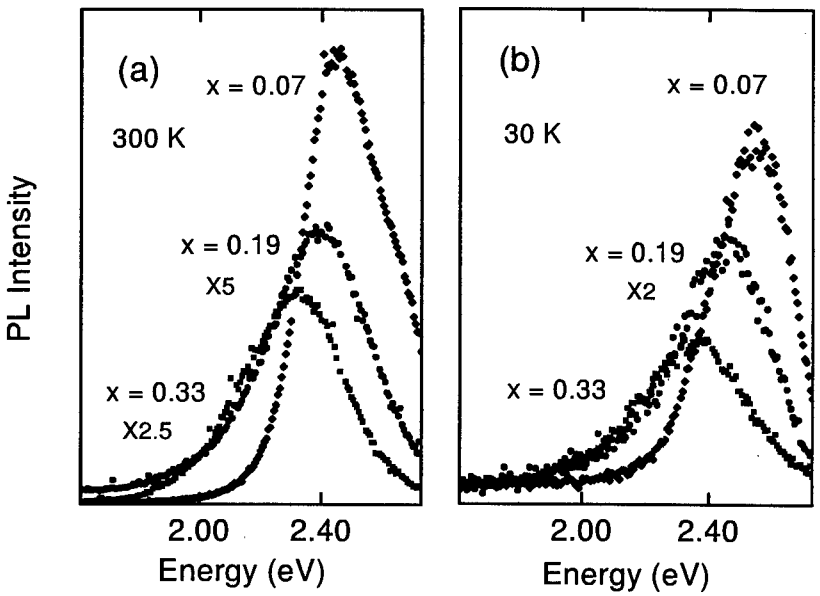

Figure 1: PL spectra of c–$In_xGa_{1-x}N$ excited with $\lambda = 441.6\ nm$ (a) at RT; (b) at T = 30 K.

also a property of the quantum dots that dominates light emission in c–$InGaN$. The phonon frequency variations were used to estimate the fluctuation in In concentration of the dots.

Experimental The InGaN layers were grown by Molecular Beam Epitaxy (MBE), on (001)–GaAs/GaN buffer layer kept at temperatures in the range of 600 °C – 680 °C. The PL measurements were carried out at room temperature (RT) and T = 30 K, with standard photomultiplier detection, and using the line 441.6 nm of a HeCd laser for excitation. The Raman scattering measurements were performed at RT with the Jobin–Yvon T64000 microRaman system. Several different lines of an Ar^+ and a Kr^+ laser were used in order to achieve resonance.

Results and discussion The photoluminescence spectra obtained at room temperature (RT), and at T = 30 K are shown in Fig. 1(a) and 1(b), respectively, for three different samples. At room temperature (30 K) a redshift of the peak energy position of 142 meV (197 meV) can be observed as the In content, x, increase from 0.07 to 0.33. The linewidth of the emission peak is the same for both samples with higher x ($\overline{\Gamma} \sim 325\ meV$), but significantly smaller for the sample with x = 0.07 ($\overline{\Gamma} \sim 262\ meV$). The intensity increases with the decrease of In molar fraction, the strongest peak, observed for x = 0.07, being about 5 times stronger than those observed for higher x at RT, and twice as higher at T = 30 K. Similar emission peaks were observed neither for GaN nor InN using the same experimental procedure. The emission energies were observed to fall far below the gap energies of the alloy to be attributed to a band–to–band transition.[9] In c–GaN a defect related process has been observed at 2.4 eV by cathodoluminescence at low excitation densities.[10] However, luminescence of this transition is totally suppressed at low temperatures. Therefore, impurity related process is ruled out, due to the weak temperature dependence of the observed PL–lines. Besides, as piezoelectric fields do not exists in c–$InGaN$, the emission is analyzed here exclusively in terms of quantum confinement effects. The confinement is due to the self–formation of quantum dots as a consequence of the immiscibility of InN in GaN.[9] The average size of the dots was estimated by using the effective masses of InN, in the lack of measured values for those of c–InGaN.

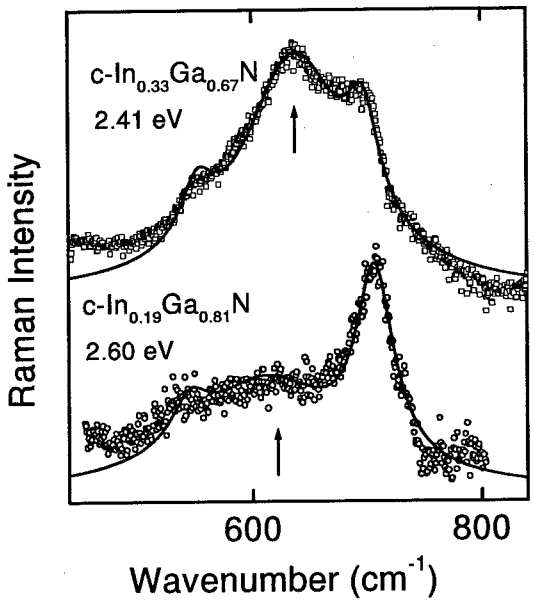

Figure 2: Resonant Raman spectra for c–InGaN, for several In content. The solid lines are fittings to Lorentzian lineshapes.

A model for spherical quantum dots together with the confinement energies determined here, yields an average dot size value of $\overline{r} \sim 3$ nm. To help this analysis a selective Resonant Raman Scattering experiment was performed using several excitation lines in the blue–green region to tune the electronic levels from which emission takes place. This procedure allowed us to observe a selective resonant enhancement of an extra–peak, in between the frequencies of the TO and LO phonons of the bulk c–$In_xGa_{1-x}N$. Figure 2 shows the Raman spectra for two different samples, with the out–going beam in close coincidence with the corresponding emission energy. The spectra, after background subtraction, consist of three peaks. The additional band, marked by arrows in Fig. 2, is broad and enhances just in the blue–green region. For excitation outside this region it disappears. The occurrence of this resonance shows that the scattering of the extra–phonon is, actually, a property of the quantum dots causing the low energy emission. For large QDs the quantum dot vibration energy is not affected by quantum confinement.[11] Therefore, the frequency of the QD phonon is related to the In concentration and the changes in this frequency are a measure of In fluctuations, exclusively. The measurements of the average concentration and compositional fluctuations in the QDs relied on the composition dependence of the LO–mode for bulk c–InGaN.[12,13] As a result, the average value, $\overline{x}$, was found to be the same, within the large fluctuation observed, for the dots formed in the samples with higher In concentration, x = 0.33 and x = 0.19. The detailed procedure gave $\overline{x} = 0.76 \pm 0.06$ ($\overline{x} = 0.72 \pm 0.09$) for the concentration within the dots of the sample c–$In_{0.33}Ga_{0.67}N$ (c–$In_{0.19}Ga_{0.81}N$). For the c–$In_{0.07}Ga_{0.93}N$ layer, the resonant peak was too weak probably due to a small scattering volume. In fact, the QD Raman peak was observed to be much stronger for x = 0.33 than for x = 0.19. Our results are thus consistent with a segregated phase spatially confined to nanoparticles. The quantum confinement to the dimension of nanoparticles of c–$In_{\overline{x}}Ga_{1-\overline{x}}N$, with radii increasing with $\overline{x}$ explains the observed shifts to lower emission energies. Because there is practically no difference in $\overline{x}$, the emission energy displacement can be attributed to the confinement effects mainly. Hence, the observed redshift

in energy is due to the different confined electronic levels rather than differences in bulk gap energies. The contribution of dots with different sizes causes the PL linewidth to be larger than expected for a recombination process involving a single electronic state. The distribution of sizes is caused by the fluctuation on $\overline{x}$ which was revealed by the RRS measurements. The important fact that the strongest PL peak was observed for the layer with lower In concentration suggests that the emission efficiency is inversely proportional to the dot size. This is true even for the lowest density of dots (for the lowest x), as inferred from the RRS experiments.

Conclusions PL spectra at RT and T = 30 K were obtained for three c–$In_xGa_{1-x}N$ samples with different In concentration. The analysis of the spectra shows that the emission is from self–formed quantum dots. RRS experiments helped this interpretation yielding the average In content within the dots. The results indicate a higher PL efficiency for lower quantum sizes even in the case of the lower QDs density.

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Materials Science Forum Vols. 338-342 (2000) pp. 1599-1602

A Comparison of Aluminum Nitride Freely Nucleated and Seeded on 6H-Silicon Carbide

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Keywords: Bulk Crystal Growth, Cathodoluminescence, Raman Spectroscopy, X-Ray Topography

Abstract The crystal quality, vibrational and luminescence properties of AlN crystals prepared by the sublimation-recondensation method with free nucleation on the crucible walls or seeded growth on 6H-SiC wafers were compared. Freely nucleated needles and platelets exhibited near-band-edge cathodoluminescence, narrow Raman peak widths, and a relatively low dislocation density as revealed by synchrotron white-beam x-ray topography. In contrast, thick films deposited on on-axis, (0001) 6H-silicon carbide wafers exhibited luminescence only at 3.5 eV, had much broader Raman peak widths, and a mosaic crystal structure.

Introduction

Aluminum nitride, a wurtzite structure wide band gap (6.2 eV) semiconductor, is a good candidate substrate for GaN epitaxial films due to its relatively small lattice constant mismatch along the a-axis (-3.5%), good thermal stability (melting point >2500 °C), high resistivity, and similar coefficients of thermal expansion [1]. Bulk crystals are grown by the sublimation-recondensation technique, most successfully developed by Slack and McNelly [2] in the mid-1970's, and further advanced more recently by Balkas *et al* [3] and Tanaka *et al* [4]. In this technique, a temperature gradient is established to decompose the polycrystalline or powder source via the reaction AlN = Al(v) + ½ N_2 in a hot sublimation zone, and the vapors are recondensed (driving the reaction in the reverse direction) as single crystals, in the cooler recondensation zone. Previous researchers have either freely nucleated the crystals on the crucible walls [2,4] or on a 6H-SiC seed crystal to better control the crystal orientation [3]. The present study was undertaken to compare the crystal quality, vibrational and luminescence properties of the AlN crystals nucleated by these two different techniques.

Sample Growth

Crystals were grown in a resistively heated furnace using tungsten wire mesh heating elements. The growth ambient was pure nitrogen, maintained at pressures between 4.0×10^4 Pa and 1.11×10^5 Pa. Pure AlN sintered into a solid form was used as a source. The source and the growing crystals were contained in a cylindrical shaped pyrolytic boron nitride crucible. The freely nucleated crystals were formed on the crucible walls, subliming from a source temperature held between 2000 °C and 2200 °C. The temperature of the recondensation zone was roughly 150 °C lower. For seeded growth, silicon-face, on-axis (0001) 6H-SiC crystals roughly 2.0 cm^2 were employed. AlN growth on 6H-SiC was limited to a seed temperature of 1750 °C or lower, to reduce the decomposition of the SiC substrate. Typically, runs were 20 hours in duration.

Materials Analysis

Raman spectra of the samples were excited by the 514.53 nm line of an Ar^+ laser. Raman spectra line widths were determined by curve-fitting to a sum of Gaussian lineshapes. The instrumental linewidth of the Raman spectrometer is 3.5 cm^{-1} to 4.0 cm^{-1}. The incident laser light was plane-polarized and the polarization of the scattered light was analyzed. The Raman scattering geometries are described by the Porto notation, for example x(zz)y, where the symbols outside the parentheses (xy in the example) refer to the propagation directions of the incident and scattered light, the symbols inside the parentheses refer to the polarizations of the incident and scattered light, z refers to the crystal (0001) direction, and x,y are orthogonal to (0001). In our experiments, the incident propagation direction was neither parallel nor perpendicular to (0001), thus the experimental geometries are described by a "mixed" notation, for example x(zz)x + x(zz)y. CL spectra of the samples were obtained in a scanning electron microscope with incident electron energy of 20 keV at a temperature of T=12 K. Synchrotron white beam x-ray topographs (SWBXT) of AlN both freely-nucleated and on the 6H-SiC substrates were taken in both Laue transmission and reflection modes at the Stanford Synchrotron Radiation Laboratory, Stanford, CA. Double crystal x-ray rocking curves of the AlN/6H-SiC samples were taken at WSU.

Results and Discussion

The freely nucleated samples produced included needles up to 4 mm in length and 0.5 mm in diameter, and thin platelets up to 2 mm x 2 mm. The majority of freely nucleated samples were needle shaped, with the longitudinal axis oriented in the <0001> crystallographic direction. Occasionally, the needles had hexagonal cross-sections; more frequently, the cross-sections were incompletely formed hexagons with deep striations running along the length of the crystal. The freely nucleated samples were either colorless or slightly amber colored, possibly a consequence of residual oxygen incorporation.

On bare 6H-SiC, the AlN nucleated as islands, forming spiral patterns, suggesting that growth was enhanced at screw dislocations present in the SiC substrate. In some cases, the AlN islands would not completely coalesce, even with a relatively large c-axis growth rate. Despite undertaking growth at a low temperature (1750 °C), some decomposition of the SiC substrate occurred, and was most rapid at the micropipes. The AlN films were frequently cracked, probably as a consequence of the small difference between the thermal expansion coefficients of AlN and SiC, combined with the large temperature span (about 1800 °C) of the sublimation growth process. The characterization reported below was on a continuous AlN film approximately 100 μm thick.

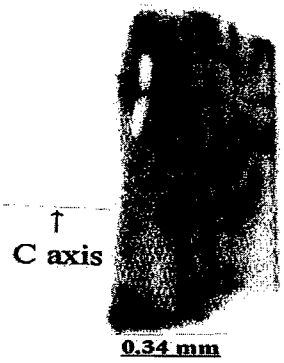

Figure 1 Synchrotron white beam x-ray topograph in Laue transmission mode from an AlN single crystal needle, diffraction vector g = -246, wavelength = 0.0298 nm.

Both needles and platelets were single crystal, with the wurtzite structure, as confirmed by the Laue transmission and back reflection synchrotron x-ray pattern, and contained regions of lower amounts of defects mixed with regions of low angle grain boundaries. Figure 1 shows a SWBXT of an AlN needle in Laue transmission mode. The low transmission parts of the topograph (white regions) shows relatively lower amounts of defects while the curved black lines are low angle grain boundaries. The grains are elongated along the c-axis and the length of individual grains varies between 0.1 mm to 1.0 mm. Unfortunately, due to the small size of the needles and platelets, x-ray rocking curves could not be taken from these samples. The x-ray double crystal rocking curves for the AlN films on 6H-SiC indicated a mosaic structure with multiple grains and a full width at half maximum from an individual AlN (0002) peak of 150 arc sec.

Five of the six Raman allowed modes of AlN were observed (Figure 2(a)) in the needle shaped samples, and identified by reference to a previous Raman study of single crystal AlN [5]. The observed modes, ordered by increasing wavenumber, were: E_2 at 247 cm^{-1}, strongest for x(yy)x + z(xx)y geometry; A_1(TO) at 609 cm^{-1} to 612 cm^{-1}, strongest for x(zz)x + x(zz)y geometry; E_2 at 656 cm^{-1}, strongest for x(yy)x + z(xx)y geometry; E_1(TO) at 669 cm^{-1}, strongest for x(yy)x + z(xx)y geometry; and E_1(LO) at 909 cm^{-1} to 912 cm^{-1}, strongest for x(zy)x + x(zx)y geometry. A distinct A_1(LO) peak, predicted at ~890 cm^{-1}, was not observed, but that mode is allowed only in z(xx)z geometry which was not accessed in our experiments. The mode frequencies were consistently lower, by 2 cm^{-1} to 7 cm^{-1}, for our sample than reported by McNeil [5]. The reason for the discrepancy is not known; one possible cause is a difference in the concentration of oxygen or other impurities.

For the AlN on 6H-SiC, the observed modes, were (Figure 2(b)): E_2 at approximately 247 cm^{-1}, A_1(TO) at 601 cm^{-1} to 603 cm^{-1}, E_2 at 654 to 657 cm^{-1}, a broad peak, possibly E_1(TO) at 647 cm^{-1} to 657 cm^{-1}, and a peak at 893 cm^{-1} to 898 cm^{-1}, which is likely a superposition of E_1(LO) and A_1(LO) lines, unresolved due to the broadening of each of these lines. The FWHM of the high-frequency peak (tentatively identified as $E_1(LO)+A_1(LO)$) in the AlN/6H-SiC films is much wider (29 cm^{-1}) than the FWHM of the E_1(LO) peak in the freely nucleated crystals (7 cm^{-1} to 8 cm^{-1}). The E_2 modes at 247 cm^{-1} and 656 cm^{-1} do not show any shift of the peak position between the freely-nucleated crystals and the

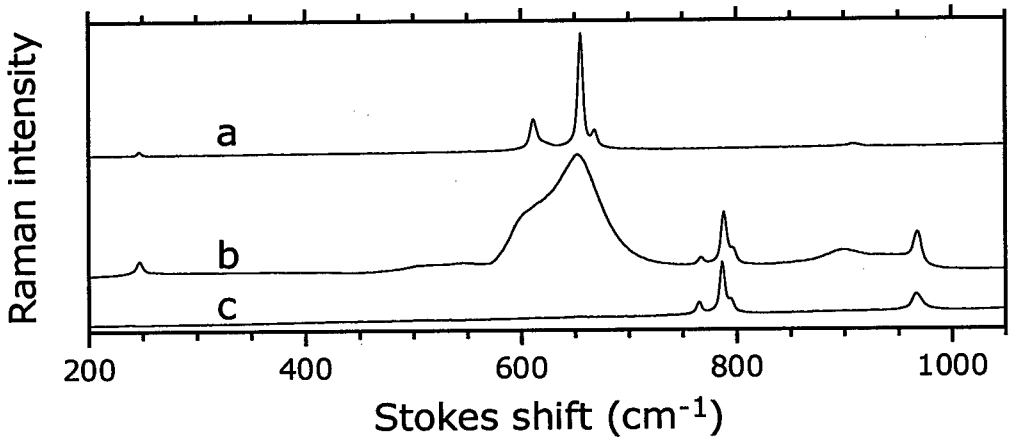

Figure 2. Raman scattering spectra of AlN from (a) a freely nucleated AlN crystal, (b) a thick film seeded on a 6H-SiC(0001) substrate, and (c) a bare 6H-SiC(0001) substrate. [Raman lines common to spectra (b) and (c) clearly originate from the substrate.]

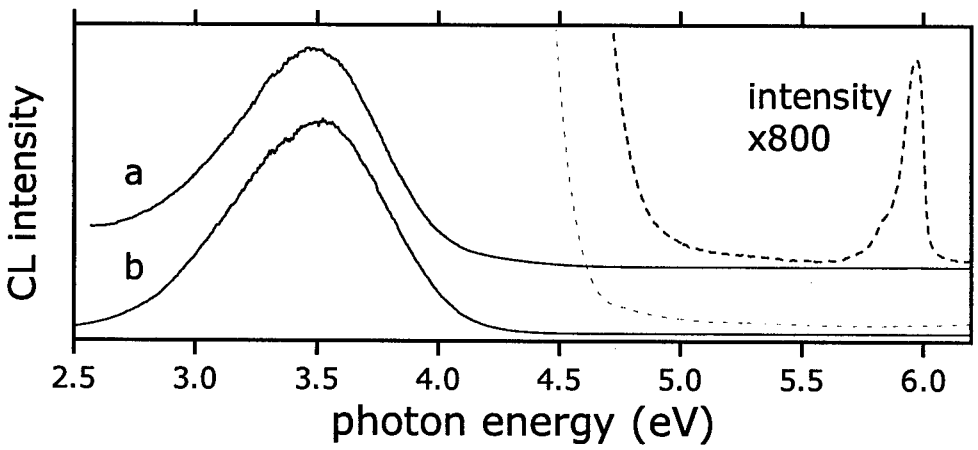

Figure 3. Cathodoluminescence spectra from AlN (a) a freely-nucleated AlN crystal, and (b) a thick film seeded on a 6H-SiC substrate.

thick films, and are also broadened less in comparison to the other modes. The E_2 modes are thus apparently less sensitive to the imperfections that cause the peak shift and broadening in the thick films. Our narrowest E_2(654 cm^{-1}) FWHM was 12 cm^{-1}, compared to value of 7.0 cm^{-1} reported by Balkas *et al* [3] for AlN/6H-SiC, and 2.2 cm^{-1} reported by McNeil and French for a bulk crystal [5].

Two overlapping near-band-edge CL peaks were observed in the freely nucleated samples: a higher energy peak located at 5.92 eV to 5.96 eV (FWHM 0.07 eV to 0.10 eV) and a lower energy peak at 5.84 eV to 5.90 eV (FWHM 0.14 eV to 0.18 eV) (Figure 3(a)). We tentatively attribute these peaks to excitons bound to impurities or point defects. A much more intense CL peak is located at 3.5 eV, with a full width of 0.7 eV. Previous researchers have proposed that the broad 3.5 eV peak is due to a combination of oxygen, nitrogen vacancies, interstitial aluminum, and point defects. The AlN/6H-SiC film does not show the exciton peak, only the peak at 3.5 eV (Figure 3(b)).

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Low Frequency Noise in n-GaN with High Electron Mobility

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Keywords: 1/f Noise, Band-to-Band, Low-Frequency Noise, Sapphire Substrate

Abstract. Low frequency noise in n-type gallium nitride (GaN) grown on sapphire with 300 K electron mobility of 790 cm^2/Vs has been studied. The noise spectra have the form of 1/f noise with a Hooge parameter α of approximately 10^{-2}. This value of α is two orders of magnitude smaller than that observed before in n-GaN. The obtained results show that the level of flicker noise in GaN, just like that in GaAs and Si, strongly depends on the structural perfection of the material. The effects of band-to-band illumination on the low-frequency noise show that 1/f noise in GaN might be caused by the occupancy fluctuations of the tail states near the band edges. This mechanism of 1/f noise is similar to that in GaAs and Si.

Introduction

Gallium nitride has an excellent potential for high temperature, high frequency, and high power microwave applications (see, for example [1-3]). The level of the low-frequency noise is one of the most important parameters, which determines whether the devices are suitable for microwave and optical communication systems. First estimates of the low-frequency noise level in n-GaN were made using visible-blind GaN *p-n* junction photodetectors [4,5]. The estimated α value was very high ($\alpha \approx 3$). The results obtained for n-GaN resistors confirmed these data [6,7].

One might suggest several possible reasons for such large 1/f-noise level. The level of the 1/f noise is much higher for a semiconductor material with imperfections. Among other factors, high dislocation density strongly increases the level of 1/f noise in certain cases [8,9]. The measured dislocation density in GaN samples grown on sapphire is of the order of 10^9-10^{10} cm^{-2}. On the other hand, theory [10] predicts that the level of 1/f noise should be proportional to the density of the tail states near the band edges. The density-of-states in the conduction band tail in GaN is much higher than that for Si and GaAs (see, for example [11]).

For the samples used in [6,7], the electron mobility μ_n was approximately 60 cm^2/Vs and was practically temperature independent in the range between 77 K and 400 K. Here we report on the results of the measurements of the low frequency noise in the samples grown on sapphire substrates with μ_n = 790 cm^2/Vs at 300 K, and with the temperature dependence $\mu_n(T)$ close to that predicted by theory [12].

Experimental details

The 20-μm thick sample was grown by hydride vapor phase epitaxy on sapphire. Sputtered ZnO was used as a buffer layer between the sapphire and GaN. Except for a highly defective interface region of a few thousand angstroms thickness, the sample was of very high quality, with the Hall mobility of 790 cm^2/Vs at 300K, and Hall electron concentration of 1.3×10^{17} cm^{-3}.
Ti (540 A)-Al (1920 A) contacts were deposited on the surface of the film and annealed at a temperature of 550 °C for 2 min.

Low-frequency noise was measured between contacts 1 and 2, and 1 and 1' (see Fig. 1) in the dark and under band-to-band illumination. Current-voltage characteristics measured between the contacts were linear and symmetrical with an accuracy of approximately 1%. Resistance R_{12} between contacts 1 and 2 was equal to 9.85 Ohm; resistance R_{11}, between the contacts 1 and 1' was equal to 30.2 Ohm.

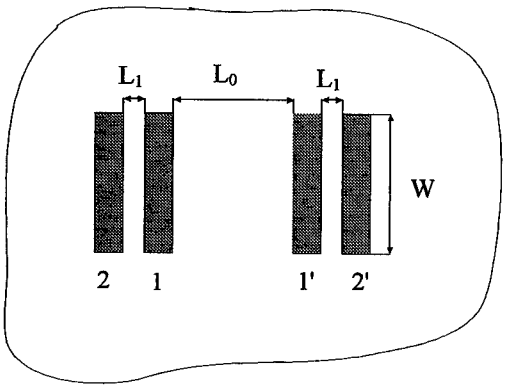

Fig. 1 Top view of the sample geometry. L_0 = 1100 μm, L_1 = 80 μm, W = 250 μm, the thickness of the film t = 20 μm.

Results and discussion

Fig. 2 shows the frequency dependencies of the noise relative spectral density measured between the contacts 1 and 2. In the dark (Curve 1), the noise is typical 1/f (flicker) noise.

The flicker noise level in different materials is frequently characterized by the dimensionless Hooge parameter, α [13]:

$$\alpha = \frac{S_V}{V_o^2} fN, \qquad (1)$$

where N is the total number of electrons contributing to noise, f is the frequency, V_o is the voltage drop across the region contributing to noise. The region contributing to noise is the region with the large electric field, since

$$S_V = \frac{\alpha\sigma^2}{fn}\int F^4 dv \qquad (2)$$

where σ is conductivity, n is the electron concentration, and F is the electric field. (see reference [13].) We estimate that the largest electric field is actually under the contacts in the region extending into the contact up to approximately the transfer length $L_T = \sqrt{r_c / R_{ch}}$, where r_c is the contact resistance (~10^{-5} Ωcm^2) and R_{ch} is the sheet resistance ($R_{ch}\approx30$ Ω). Using this dimension we crudely estimated α ~ 0.01.

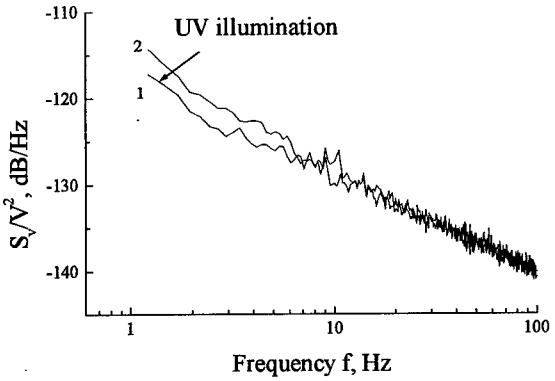

Fig. 2 Frequency dependencies of the current noise relative spectral density S_V/V^2 in the dark (Curve 1) and under band-to-band illumination (Curve 2) measured between contacts 1 and 2.

Curve 2 in Fig. 2 presents the results under band-to-band illumination with an incandescent lamp. At a given illumination intensity, the photoconductivity $\sigma/\sigma_0 \approx 2\times10^{-2}$. The effect of the illumination is relatively weak. However the qualitative effect is quite similar to that for Si and GaAs [15]. The illumination has no effect at higher frequencies and increases the noise at relatively low frequencies.

Fig. 3 shows the frequency dependencies of the noise relative spectral density measured between the contacts 1 and 1'.

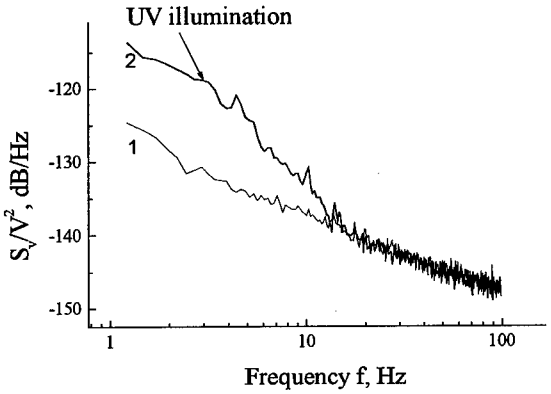

Fig.3 Frequency dependencies of the current noise relative spectral density S_V/V^2 in the dark and under band-to-band illumination measured between contacts 1 and 1'.

The curve measured in the dark (Curve 1) has the form of 1/f noise (flicker) noise. Comparing Curves 1 in Figs. 2 and 3 one can see that the difference in the level of the dark noise is rather small for these two very different electrode configurations. The noise measured between contacts 1 and 1' should be considerably less than that between contacts 1 and 2. It is clear that the total number of the conduction electrons involved is substantially smaller for the case represented in Fig 2 (contacts 1 and 2) compared to that shown in Fig. 3 (contacts 1 and 1'). Therefore the noise measured between contacts 1 and 1' should be at least 20 dB less than that between contacts 1 and 2. However, the measured difference in the noise levels is only ≈ 7 dB (compare Curves 1 in Figs. 2 and 3). Once again, these results demonstrate that relatively small regions close to the surface contacts disproportionally contribute to the noise.

Curve 2 in Fig. 3 represents the results under band-to-band illumination. At a given illumination intensity, the photoconductivity $\sigma/\sigma_0 \approx 5\times10^{-3}$. Despite the fact that this photoconductivity is less than that for the case represented in Fig. 2, the effect of the band-to-band illumination is much stronger. Such an effect of band-to-band illumination on the 1/f noise was

analyzed in detail for Si samples in reference [16] using the model of 1/f noise developed in Ref. [10] (see the inset in Fig. 3).

The comparison of the observed effect of band-to-band illumination on the low-frequency noise (see Fig. 3) with the theory (see the inset) shows that the nature of the 1/f noise in GaN should be similar to that in GaAs and Si. The 1/f noise is caused by the fluctuations of the occupancy of the tail states near the band edges.

Acknowledgment.

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Chapter 8

III-Nitrides: Processing and Devices

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Role of Alloy Fluctuations in InGaN-Based LEDs and Laser Diodes

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Keywords: Dislocation, Laser Diode, Lateral Overgrowth, LEDs, Lifetime

Abstract

UV/blue/green InGaN and GaN single-quantum-well structure light-emitting diodes (LEDs) were grown on epitaxially laterally overgrown GaN (ELOG) and sapphire substrates. The external quantum efficiency (EQE) of the UV InGaN LED on ELOG was much higher than that on sapphire only at high-current operation. At low-current operation, both LEDs had the same EQE. When the active layer was GaN, EQE of the LED on sapphire was much lower than that on ELOG even at low- and high-current operations due to the lack of localized energy states formed by alloy composition fluctuations. In order to improve the lifetime of laser diode (LD), ELOG had to be used because the operating current density of the LD is much higher than that of LED. A violet InGaN multi-quantum-well/GaN/AlGaN separate-confinement-heterostructure LD with an emission wavelength of 410 nm was grown on ELOG substrate. The LDs with cleaved mirror facets showed an output power as high as 40 mW under room-temperature continuous-wave (CW) operation. The stable fundamental transverse mode was observed at an output power of up to 40 mW. The estimated lifetime of the LDs at a constant output power of 30 mW was more than 500 hours under CW operation at an ambient temperature of 60℃.

1. Introduction

Recently, there has been much interest in light-emitting diodes (LEDs), which emit from ultraviolet (UV) to red wavelengths, and are fabricated from III-V nitride compound semiconductors. Major developments in wide-band-gap III-V nitride semiconductors have recently led to the commercial production of high-efficiency UV/blue/green/amber/white LEDs and violet laser diodes (LDs) [1-6]. All of these light-emitting devices use an InGaN active layer instead of a GaN active layer because of the difficulty in fabricating highly efficient light-emitting devices using a GaN active layer [7]. Several groups recently reported that the dislocations are nonradiative recombination centers in GaN and InGaN [8,9]. In InGaN, however, the role of dislocations has not yet been clarified. Highly efficient blue/green InGaN quantum-well structure (QW) LEDs have been fabricated directly on a sapphire substrate in spite of a high dislocation density of 1-10 x $10^{10}/cm^2$ originating from a large lattice mismatch between GaN and the sapphire substrate [1-6]. Due to the high efficiency of the LEDs grown on sapphire substrates, the dislocations in InGaN do not appear to work effectively as nonradiative recombination centers [10]. Epitaxially laterally overgrown GaN (ELOG) on sapphire was developed recently to reduce the number of threading dislocations in GaN epitaxial layers [11-13]. Using the ELOG, the number of threading dislocations was reduced significantly to almost zero in the GaN grown on SiO_2 stripe mask [12,13]. The blue InGaN single-quantum-well (SQW) structure LEDs were fabricated on the ELOG to study the role of dislocations [14]. The output power of blue LEDs grown on the ELOG was almost the same as that grown directly on sapphire substrate [14]. To explain the high efficiency of InGaN-based LEDs in spite of a large number of dislocations, localized energy states formed by alloy composition

fluctuations of the InGaN layer were proposed [7,15]. In order to study the role of dislocations in InGaN and GaN layers further, UV/blue/green InGaN and GaN SQW structure LEDs were fabricated on ELOG and sapphire substrates. Also, InGaN muti-quantum-well (MQW)/GaN/AlGaN separate confinement heterostructure (SCH) LDs were grown on the ELOG.

2. UV/blue/green InGaN and GaN LEDs grown on ELOG

III-V nitride films were grown using the two-flow metal-organic chemical vapor deposition (MOCVD) method, the details of which have been described previously [1]. First, selective growth of GaN was performed on a 2-μm-thick GaN layer grown on a (0001) C-face sapphire substrate. The 0.1-μm-thick silicon dioxide (SiO_2) mask was patterned to form 4-μm-wide stripe windows with a periodicity of 12 μm in the GaN <1-100> direction. Following the 15-μm-thick GaN growth on the SiO_2 mask pattern, the coalescence of the selectively grown GaN enabled the formation of a flat GaN surface over the entire substrate. This coalesced GaN was designated the ELOG. We examined the defect density by plan-view transmission electron microscopy (TEM) observation of the surface of ELOG substrates. The number of dislocations on the SiO_2 mask area was almost zero, and that on the window area was approximately $2x10^7/cm^2$[16]. This ELOG was the same as that used to fabricate blue SQW LEDs previously [14]. After obtaining a 15-μm-thick ELOG substrate, UV InGaN and GaN LEDs were grown on the substrate [3,5]. The LED structure consists of a 1.5-μm-thick undoped GaN layer, a 2.4-μm-thick n-type GaN:Si layer, a 0.2-μm-thick undoped GaN layer (current spreading layer), a 400-Å-thick n-type AlGaN:Si, a 50-Å-thick undoped InGaN or GaN active layer, a 600-Å-thick p-type $Al_{0.2}Ga_{0.8}N$:Mg layer and a 0.1-μm-thick p-type GaN:Mg layer. This structure of the LEDs is almost the same as that of previous UV InGaN LEDs [3,5]. The In composition of the InGaN well layer was nearly zero for UV LEDs. For comparison, the same structure of LEDs was grown directly on sapphire substrate. Fabrication of LED chips (350 μm x350 μm) was accomplished as follows. The surface of the p-type GaN layer was partially etched until the n-type GaN layer was exposed. Next, a Ni/Au contact was evaporated onto the p-type GaN layer and a Ti/Al contact onto the n-type GaN layer. The characteristics of the LEDs were measured under a direct current (DC) at room temperature.

Figure 1 shows the emission spectra of UV InGaN LEDs on ELOG at various currents at RT. The emission spectra of UV InGaN LEDs on sapphire were almost the same of those on ELOG. The peak wavelength of both LEDs is around 380 nm. The large spectrum width is mainly due to alloy composition fluctuation in the InGaN well layer [17,18]. This means that the degree of the fluctuation is the same in both LEDs in spite of a large difference in the TD density. Thus, the alloy composition fluctuations are not related to the TDs. In both spectra, a small blue shift is observed due to the band-filling effect of the localized energy states formed by alloy composition fluctuation [17,18]. However, the degree of blue shift is relatively small due to the small alloy composition fluctuations that resulted from the small In mole fraction in the InGaN well layer. The ELOG and GaN on sapphire had average dislocation densities of $7x10^6/cm^2$ and $1x10^{10}/cm^2$, respectively. Here, the average dislocation density of the ELOG on sapphire was obtained by dividing the dislocation density of $2x10^7/cm^2$ on the window region by the ratio of (stripe periodicity of 12 μm)/ (window width of 4 μm) because the dislocation density

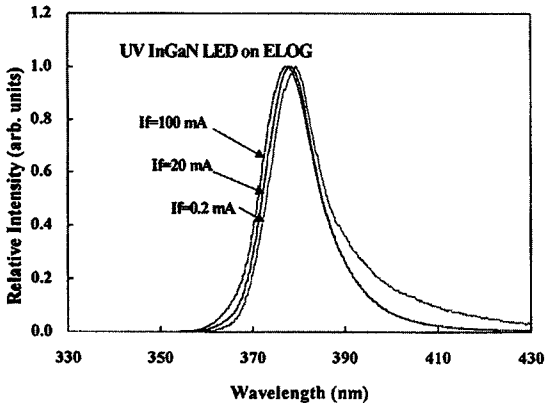

Fig. 1. Emission spectra of UV InGaN LEDs on ELOG substrate at various forward currents at

on the SiO_2 stripe region was almost zero. The size of LED chip is as large as 350 μm x 350 μm. Each LED chip includes many window and SiO_2 stripe regions. Therefore, we used an average dislocation density for the ELOG on sapphire.

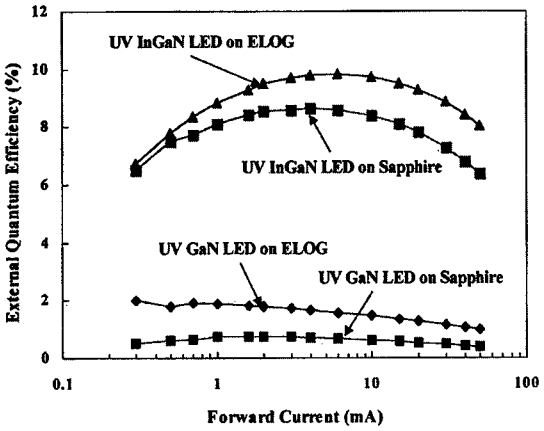

Fig. 2. EQE of UV InGaN and GaN LEDs as a function of forward current.

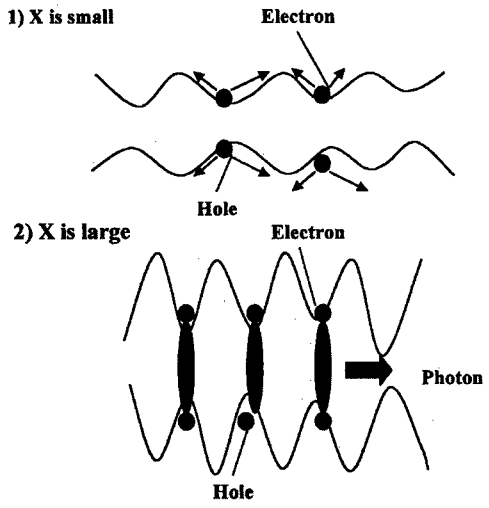

Fig. 3. Model of localized energy states formed by alloy composition fluctuations. (a) When the degree of alloy composition fluctuations is small, carriers easily overflow the localized states with increasing the current. (a) When the degree of alloy composition fluctuations is large, carriers are still confined even at high current operation.

Figure 2 shows the external quantum efficiency (EQE) of UV InGaN and GaN LEDs as a function of forward current. From this figure, the EQE of UV InGaN LED on sapphire is almost the same as that on ELOG at low currents below 0.4 mA. Thus, the carriers are easily captured to localized energy states formed by alloy composition fluctuation at low currents, and radiatively recombine before they are captured by nonradiative recombination centers formed by a large number of dislocations [7]. With increasing current, some carriers can overflow from the localized energy states due to a small alloy composition fluctuation of UV InGaN LEDs, and reach nonradiative recombination centers. As a result, the efficiency of UV InGaN LEDs on sapphire decreases at high currents. By reducing the dislocation density using ELOG, UV InGaN LEDs can emit a stronger output power even at high currents. On the other hand, the EQE of UV GaN LED on sapphire is lower than that on ELOG even at low currents because there are no localized energy states formed by alloy composition fluctuation. It is only by reducing the dislocation density, can the EQE of UV GaN LEDs be increased using ELOG, as shown in Fig. 2 [7]. Recently, many groups have reported that the quantum-confined Stark effect (QCSE) resulting from the piezoelectric field due to strain determines the emission mechanism of InGaN or GaN-based LEDs [19-22]. This field, if sufficiently strong, will induce a spatial separation of the electron and hole wave functions in the well. Then, the wave function overlap decreases and the interband recombination rate is reduced. It is difficult to explain the results in Fig. 2 by QCSE [7]. UV InGaN LEDs on sapphire and ELOG have the same efficiency at low currents. However, the efficiency of UV GaN LED on sapphire is much lower than that on ELOG even at low currents. Considering the strain in the well layer, QCSE should almost be the same for all of these LEDs. Thus, it is difficult to explain these

differences in the behavior of UV InGaN and GaN LEDs using QCSE [7]. These results can be explained only by the localized energy states formed by alloy composition fluctuation as mentioned above, and not by QCSE.

At a forward current of 20 mA, The EQE is the highest at a wavelength in the blue region with an EQE of 11.6% due to a large number of deep localized energy states formed by large alloy composition fluctuations. At the wavelength in the blue and green regions, there was no difference in EQE between LEDs on ELOG and sapphire despite a large difference in the dislocation density between them [14]. However, UV LEDs exhibit a different behavior: EQE becomes much lower when the LED was fabricated on sapphire due to a large number of dislocations. When the emission wavelength of UV LEDs with an active layer of GaN is 360 nm, the EQE of GaN LED on ELOG is two times higher than that on sapphire. These results are explained only using the localized energy states formed by alloy composition fluctuations in the InGaN well layer, as mentioned in Figs. 2. When the emission wavelength is shorter than 370 nm, EQE decreases dramatically, due mainly to the self-absorption of p- and n-GaN contact layers. Figure 3 shows the schematic model of localized energy states formed by alloy composition fluctuations in the InGaN well layer.

3. Violet InGaN-MQW/GaN/AlGaN SCH LDs

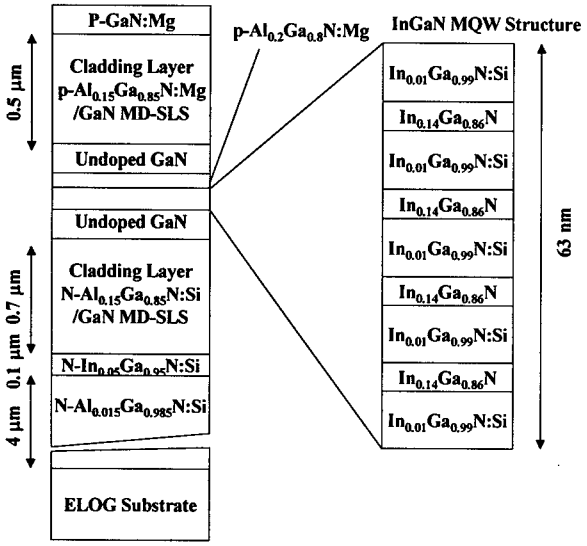

Fig. 4. Structure of InGaN-MQW/GaN/AlGaN SCH LDs

Even if InGaN active layers are used for LEDs and LDs, with increasing current, some carriers can overflow from the localized energy states due to a small alloy composition fluctuation of UV InGaN LEDs and LDs, and reach nonradiative recombination centers, as mentioned above. As a result, the efficiency of UV InGaN LEDs and LDs on sapphire decreases at high current operation. Especially, the operating current density of the LDs (2-5 kA/cm^2) is much (more than 10 times) higher than that of LEDs (0.04 kA/cm^2). Thus, under laser operation, many carriers can overflow from the localized energy states, and reach nonradiative recombination centers formed by a large number of TDs when the LDs were fabricated directly on sapphire substrate [7]. Through this nonradiative recombination of the carriers, the internal loss of the cavity of the LDs is increased, and the thershold current density of the LDs is increased [7]. As a result, the lifetime of the LDs was shortened to around 300 hours [23]. Thus, only by reducing the dislocation density using ELOG, InGaN-based LDs can lengthen a lifetime by reducing the threshold current density [7].

On the above-mentioned ELOG substrate, the laser structure was grown as shown in Fig. 4. The details of the InGaN-MQW/GaN/AlGaN SCH laser structure are described in other papers [1,6]. The surface of the p-type GaN layer was partially etched until the n-type GaN layer and p-type $Al_{0.15}Ga_{0.85}N$/GaN MD-SLS cladding layer were exposed to form the ridge-geometry LDs. The stripe width was 2 μm. The cavity length was 600 μm. The region of the ridge-geometry LD of 2 μm x 600 μm was formed on the laterally overgrown region of the GaN on SiO_2 stripe-shaped mask. A laser cavity was formed by cleaving the facets along the {1-100} face of the LD grown on the

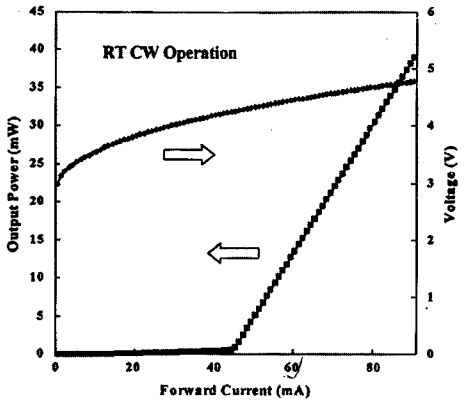

Fig. 5. Typical L-I and V-I characteristics of InGaN-MQW/GaN/AlGaN SCH LDs measured under CW operation at RT.

ELOG. A facet coating consisting of two pairs of quarter-wave TiO_2/SiO_2 dielectric multilayers was formed on one side of the facets. The output power of the LD was measured from an uncoated facet. The electrical characteristics of the LDs fabricated in this way were measured under a direct current (DC).

Figure 5 shows the voltage-current (V-I) characteristics and the light output power per uncoated cleaved facet of the LD as a function of the forward DC current (L-I) at RT [6]. No stimulated emission was observed up to a threshold current of 43 mA, which corresponds to a threshold current density of 3.6 kA/cm^2. The threshold voltage was 4.3 V. The output power of the LDs was as high as 40 mW at an operating current of 90 mA. At an output power of up to 40 mW, no kink was observed in the L-I curve because the transverse mode was stable at a fundamental transverse mode with a small ridge width of 2 μm. The slope efficiency was as high as 1.0 W/A. The emission spectra of the LDs were measured under RT-CW, as shown in Fig.6. At output powers of 3 mW and 10 mW, single-mode laser emissions were observed at wavelengths of 408.1 nm and 408.2 nm. At output powers of 30 mW and 50 mW, multimode laser emissions were observed at wavelengths of 408.7 nm and 409.1 nm.

Figure 7 shows the results of a lifetime test of CW-operated LDs carried out at an ambient temperature of 60°C, in which the operating current is shown as a function of time under a constant

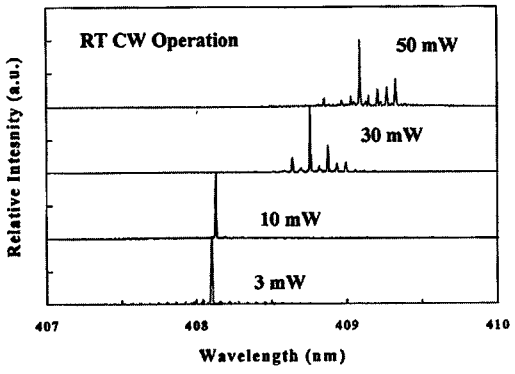

Fig. 6. Laser emission spectra measured under RT-CW operation at output powers of 3 mW, 10 mW, 30 mW and 50 mW.

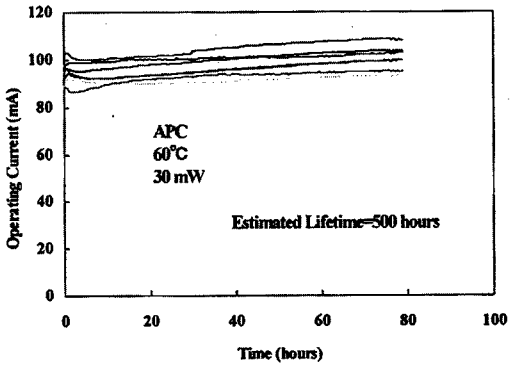

Fig. 7. Operating current of InGaN-MQW/GaN/AlGaN SCH LDs as a function of time under a constant output power of 30 mW at an ambient temperature of 60°C controlled

output power of 30 mW controlled using an autopower controller (APC). After 78 hours of operation, only small degradation was observed. The degradation speed was defined to be dI/dt (mA/40 hours), where I is the operating current of the LDs and t is the time. Using this degradation speed, the estimated lifetime was determined to be the time when the operating current became 1.5 times the initial operating current of the LDs. The lifetime was estimated to be more than 500 hours under these conditions.

4. Conclusions

UV/blue/green InGaN and GaN LEDs were grown on ELOG and sapphire substrates. When the emission wavelength of InGaN LEDs was shorter than 380 nm, EQE of the InGaN LED on ELOG was much higher than that on sapphire at high current operation. At low current operation, both LEDs had the same EQE. When the active layer was GaN, EQE of the LED on sapphire was relatively low even at low and high current operations due to the lack of localized energy states formed by alloy composition fluctuation. When the emission wavelength was in the blue and green regions, EQE was almost the same between LEDs on ELOG and sapphire due to a large number of deep localized energy states formed by large alloy composition fluctuations. Thus, under operating conditions of laser diodes, carriers injected into InGaN well layers easily overflow from the localized energy states, and reach nonradiative recombination centers formed by a large number of TDs. Thus, in order to improve the lifetime of the LD, the TD had to be reduced using ELOG substrate. InGaN-MQW/GaN/AlGaN SCH LDs were fabricated on the ELOG. The LDs with cleaved mirror facets showed an output power as high as 40 mW under RT-CW operation with a stable fundamental transverse mode. The lifetime of the LDs at a constant output power of 30 mW was approximately 500 hours under CW operation at an ambient temperature of 60°C. High power LDs with an output power of 30 mW and a lifetime of 3,000 hours would be available soon because the progress of the improvement of the lifetime is so fast.

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Materials Science Forum Vols. 338-342 (2000) pp. 1615-1618

Influence of Annealing Conditions on Dopant Activation of Si^+ and Mg^+ Implanted GaN

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Keywords: Activation, Annealing, Capping, Encapsulation, Ion Implantation, Photoluminescence, Rutherford Backscattering Spectrometry

Abstract

This report reflects the results of heat treatment under various conditions on as-grown and ion implanted GaN. The PL spectrums of as-grown GaN and GaN with 400 Å AlN cap were almost identical. This fact allows us to use PL analysis without AlN stripping. As-grown GaN and ion implanted with Mg^+ and Si^+ crystals were annealed at 1300 °C for 10 minutes in three different conditions: in flowing argon gas; in flowing ultra high purity nitrogen; and in a quartz capsule sealed with nitrogen gas. The results of PL, RBS, SEM and TEM analysis show an advantage of GaN high temperature annealing in quartz capsules with nitrogen ambient as compared to annealing in argon and nitrogen gas flow. Encapsulation with nitrogen overpressure prevents the decomposition of the GaN crystal and the AlN capping film, and allows one to achieve optical activation of implanted Mg and Si after 1300°C annealing.

Introduction

GaN can be doped during growth, by ion implantation, ion implantation at elevated temperature [1-3], by recoil atom implantation, and by neutron transmutation [4]. Ion implantation is widely used in microelectronics technology and attracts the attention of many researches trying to achieve the desired GaN doping, but this process is still under development. Annealing at temperatures higher than 1100 °C is required to recover radiation damage in ion implanted GaN. The high temperature processing of this material should be conducted with extreme care of GaN's surface stoichiometry: substantial nitrogen outdiffusion from the surface of GaN in a vacuum starts at about 800-900°C [5]. In order to avoid GaN decomposition, various methods can be used, such as annealing with polycrystalline AlN cap, at high nitrogen pressure, and other conditions. In the work presented, we studied the influence of annealing ambient on to the optical and structural properties of as-grown and ion implanted GaN crystals.

Experiment

Highly resistive GaN films were grown by MOCVD on 6H-SiC (0001) with an AlN buffer layer. The details of the growth process and films parameters are discussed elsewhere [6]. RBS measurements for the as -deposited GaN resulted in χ_{min} (ratio of aligned to random yield) less than 3%.

GaN samples were implanted with 80 keV Mg^+ /or 100 keV Si^+ with doses of $5x10^{14}$ cm^{-2}. The ion energies were calculated using TRIM code to achieve an ion projected range of ~70nm. As-implanted samples were analyzed with RBS and PL. Before annealing all samples were capped by 400 Å of AlN film grown by MOCVD at 1100 °C. The 16 K PL spectra were excited with 8 mW HeCd laser (325 nm).

As-grown and ion implanted GaN samples were annealed in a conventional furnace at 1300 °C in three different conditions: first, in flowing argon gas; second, in flowing nitrogen; and third, in a sealed quartz capsule with 1 to 2 Torr pressure of nitrogen for 10 minutes. Annealed samples were characterized with PL, SEM, TEM, RBS.

Results and discussions

Fig. 1 represents the photoluminescence spectra taken at 16 K from GaN samples. AlN capping did not significantly affect PL measurements, except some change in the intensity of the "yellow" band emission region. The full widths at half maxima (FWHM) of the band-edge emission lines showed a slight decrease after annealing in the capsule from 11.3 meV to 10.5 meV. The FWHM of the "yellow" band also decreased from 338 meV to 300 meV. PL data for AlN capped GaN and annealed in a capsule, revealed a noticeable rise of the peak-to-peak ratio of intensities of the "yellow" band to the band-edge lines: after 1300 °C annealing, the peak-to-peak ratio dropped nearly 35%.

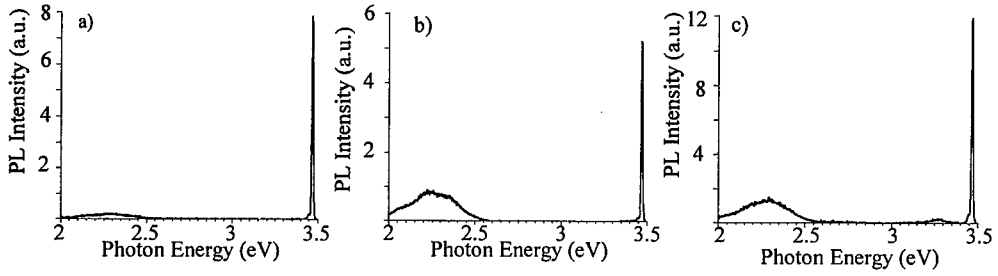

Figure 1. PL spectra (16 K) for: a) as-grown GaN; b) GaN capped with AlN; c) GaN capped with 400 Å AlN and annealed at 1300°C for 10 min in quartz capsule with nitrogen pressure of 2 Torr.

Annealing of ion implanted GaN samples in flowing argon (or nitrogen) at 1300 °C for 10 min. resulted in partial or complete degradation of both the AlN cap and underlying GaN film. The 2.7 eV luminescence peak was present for all the annealed samples annealed. Analysis of the samples by SEM and RBS (see Fig.2) confirmed partial to complete decomposition of the AlN cap and underlying GaN after annealing in flowing argon as well as flowing nitrogen.

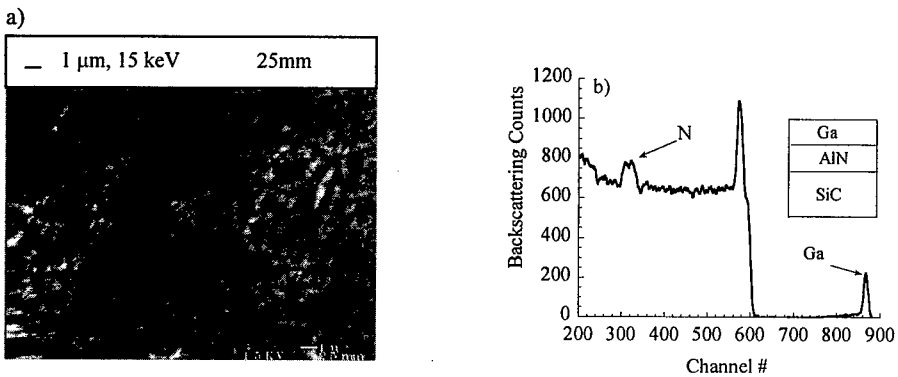

Figure 2. GaN implanted with 80 keV Mg^+, capped with AlN, and annealed at 1300 °C for 10 min. in flowing argon, nitrogen, or in a quartz capsule with less than 1 Torr of nitrogen gas pressure: a) SEM image of GaN annealed in flowing argon, b) RBS spectrum (random).

RBS analysis (Fig. 2b) confirmed degradation of the AlN cap layer and underlying GaN film of samples annealed in flowing argon, nitrogen, or in a quartz capsule with less than 1 Torr of nitrogen gas pressure at 1300 °C for 10 min. The SEM image of this type of sample is shown in Fig. 2a.
Selected Mg (or Si) implanted AlN samples were annealed in a conventional furnace at 1200 °C for 2 hrs. in flowing argon. The PL spectra from Mg^+ implanted sample showed a dominating peak at 3.47 eV (FWHM=14.6 meV), and DA phonon replicas at 3.27 eV, 3.17 eV, and 3.08 eV, and finally a "yellow" band at around 2.23 eV. Similar PL results on Mg implanted GaN films were reported elsewhere [7].
Other Mg^+ implanted GaN samples were sealed in a quartz capsule with 2 Torr of nitrogen gas pressure and annealed at 1300 °C for 10 min. The PL spectra indicated significant changes: the "yellow" band intensity has become almost 50% lower than D-A peaks (see Fig.3a). The consecutive separation between these peaks is about 91 meV due to the coupling of phonons to the transition to the donor-acceptor pair recombination peak of 3.27 eV. As a result of annealing Si^+ implanted GaN, the peak at 64 meV from the band-edge appeared (Fig. 3b). This peak is most likely related to the dopant activation. At the same time, the "yellow" band is relatively higher in intensity. This high intensity can be a result of a higher concentration of radiation defects caused by Si, which atomic mass is higher compared to that of Mg. The SEM image shown in Fig.3c also reveals substantially better surface features of the AlN cap in comparison to other annealing conditions. The RBS analysis indicated the presence of unaffected AlN cap (Fig. 3d).

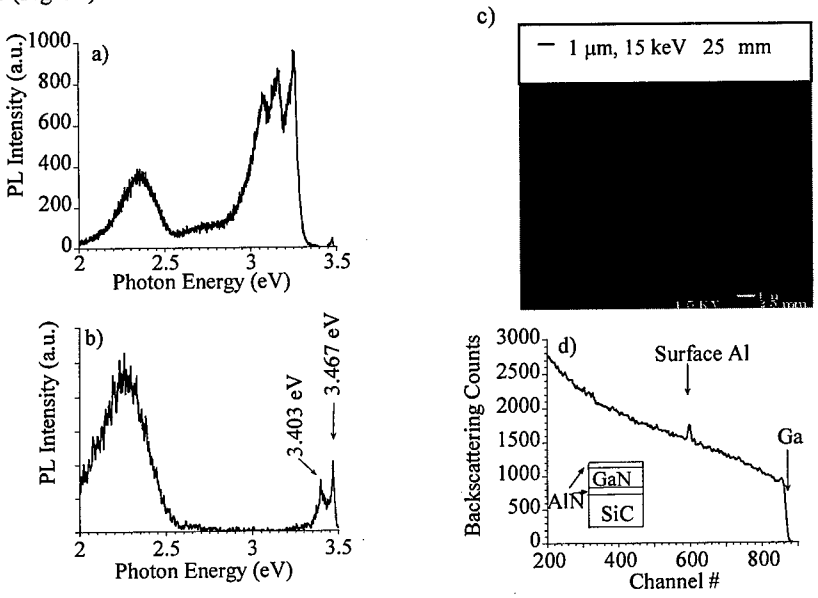

Figure 3. GaN implanted with 80 keV Mg after annealing in quartz capsule at 1300 °C for 10 min. under 2 Torr of nitrogen pressure: a) PL spectrum of Mg^+ implant, b)PL spectrum of Si^+ implant, c) SEM image of Mg^+ implant, d) RBS spectra of Mg^+ implanted.

In order to distinguish the role of radiation damage and the presence of implanted impurities 140 keV Ar^+ ions were implanted with the same range as the implanted Mg^+ and Si^+ ions. The annealing recovered the band edge peak, but the "yellow" emission in the Ar^+ implanted sample remained strong even after 1300°C anneal in capsule. Therefore PL peaks in the near band–edge region in the case of Mg^+ or Si^+ implantations are caused not by radiation defects, but by the presence of implanted dopants (Mg or Si).

The non damaged AlN capping film and GaN crystal, after this type of annealing, can be seen in TEM image in Fig. 4.

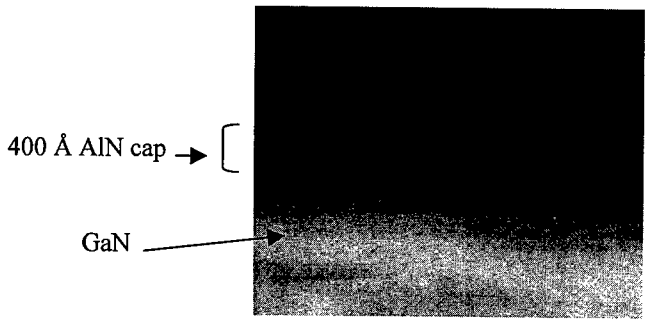

Figure 4. TEM image for the implanted GaN film, covered with AlN and annealed at 1300°C for 10 min under 2 Torr pressure of nitrogen.

Conclusions

The results of the PL, RBS, SEM and TEM analysis show an advantage of GaN high temperature (1300°C) annealing in quartz capsules with nitrogen ambient, as compared with annealing in argon and nitrogen gas flow. The 2.7 eV luminescence peak has been observed in samples with partial to complete decomposition of the AlN cap and underlying GaN, after annealing in flowing argon as well as flowing nitrogen, and this peak cannot be related to dopant activation.

Encapsulation with nitrogen overpressure prevents the decomposition of the GaN crystal and the AlN capping film, and allows one to achieve optical activation of the implanted Mg and Si after 1300°C annealing. PL measurements at 16 K of GaN samples implanted with Mg and annealed in a capsule showed three relatively strong peaks at 211, 303, and 395 meV from the band-edge emission. The relative intensity of the "yellow" band emission is several times lower in the case of annealing in a sealed capsule as compared to that in open anneals in flowing argon or nitrogen. As a result of annealing Si^+ implanted GaN, the peak at 64 meV from the band-edge appeared. This peak is most likely related to dopant activation.

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Materials Science Forum Vols. 338-342 (2000) pp. 1619-1622

Ohmic Contact Formation on Silicon-doped Gallium Nitride Epilayers by Low Temperature Annealing

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Keywords: Low Temperature Annealing, n-GaN, Ohmic Contacts, Ti/Al

Abstract

Ohmic contacts have been fabricated on Si doped n-GaN using Ti/Al by low temperature annealing. Contact resistivity values of 8.6×10^{-6} ohm-cm^2 were obtained for 3.67×10^{18} cm^{-3} doped samples after annealing at 500°C. SIMS analysis showed that Al diffused through the Ti layer after annealing. As a result Al low work function metal to n-GaN may have resulted in good ohmic contact. Photoluminescence (PL) showed that there was no degradation in the epilayer quality of the film annealed at this temperature for 25 min.

Introduction

The III-V nitrides have long been viewed as a promising material system for optical device applications between the visible and UV wavelength spectra; and also for various high temperature, high power and high frequency electronic devices, due to their direct, wide-band gap [1,2].

In order to realize GaN devices with good performance, it is essential to have high quality ohmic contacts to this wide bandgap material. In most of the work that has been carried out on ohmic contacts to GaN, high temperature annealing has been performed in order to achieve low specific contact resistivity [3,4]. This process is, however, often not desirable, especially in heterostructure devices. Furthermore, in most published reports [3,5-7], the GaN samples were unintentionally doped, yet having carrier concentrations of the order of 10^{17} cm^{-3} or more. This is an indication of a significant number of defects, such as nitrogen vacancies, which may have aided the ohmic contact formation. In other instances, GaN surfaces have been etched by RIE prior to metallization [4], which might have modified the surface and contributed to the ohmic contact formation.

In the present work, low temperature annealing at 500°C has been used to achieve good ohmic contacts on two Si-doped GaN samples. Furthermore, the degradation or enhancement in the epilayer, while annealing for contact studies has been observed through the PL measurements.

Experimental

A GaN buffer was first grown on the sapphire substrate at a temperature of 550°C to a nominal thickness of 300 Å. The temperature was then raised to1050°C for the growth of the n-GaN with V/III ratio in the range of 3000. The reactor pressure was maintained at 200 Torr. Silicon doping was carried out by flowing silane. The bulk carrier concentrations of the samples were 1.08×10^{18} cm^{-3} and 3.67×10^{18} cm^{-3} with room temperature Hall mobility of 328 and 234 cm^2/V-s respectively. The contact resistance was obtained using the TLM method. The structures used for the TLM measurements were fabricated by first patterning the GaN with 55x400 μm mesas. The patterns were etched using a Plasma-Therm 770(ICP/RIE) system, with a mixture of BCl_3/Cl_2 gases. For metallization, the GaN samples were first cleaned with organic solvents. Contact pads were patterned on the mesas with spacing between pads of 2, 4, 6, 8, 10 and 15 μm. Then, prior to

loading the sample into an e-beam evaporator the samples were dipped in HCl:H_2O(1:1) for 3 min, rinsed in DI water and blown dry with N_2 gas. The evaporator chamber was pumped down to a base pressure of ~10^{-6} Torr before metal deposition. The bilayer contact consisted of ~15 nm Ti deposited directly on GaN, followed by ~110 nm of Al. A conventional lift-off technique was used to define the pattern on the metallized samples. The metal contacts on n-GaN were furnace annealed in a N_2 ambient. Current-voltage characteristics and contact resistances were measured using an HP4156A semiconductor analyzer. All measurements were conducted at room temperature. A Cameca ims 6f secondary ion mass spectrometer with 3.0 keV Cs^+ beam was used for the SIMS analyses.

Results and discussions

The linear I-V characteristics of as-deposited and annealed contacts on samples with doping levels of $1.05x10^{18}$ cm^{-3} and $3.67x10^{18}$ cm^{-3} are shown in Figures 1 and 2 respectively.

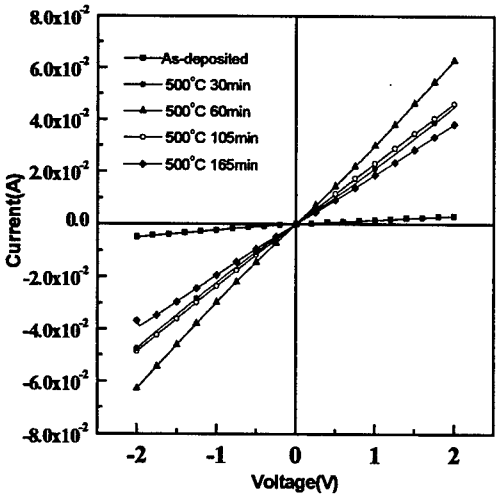

Figure 1: Typical I-V characteristics for Ti/Al on n-GaN ($1.08x10^{18}$ cm^{-3}).

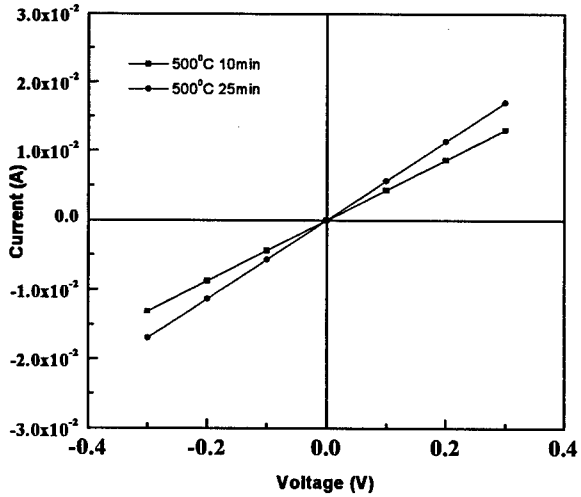

Figure 2: Typical I-V characteristics for Ti/Al on n-GaN ($3.67x10^{18}$ cm^{-3}).

Table-I: Specific contact resistivities calculated for different annealing conditions.

Concentration (cm^{-3})	Temperature (°C)	Time(min)	ρ_c (ohm-cm^2)
$1.05x10^{18}$	500	30	$4.65x10^{-5}$
		60	$4.49x10^{-5}$
		105	$5.33x10^{-5}$
$3.67x10^{18}$	500	10	$1.55x10^{-5}$
		25	**$8.63x10^{-6}$**

The specific contact resistivity values were calculated from the measured resistance vs contact spacing data using the TLM method and are listed in Table-I.

It can be seen that for the contacts on GaN with $1.05x10^{18}$ cm^{-3} carrier concentration and annealed for 60min, ρ_c reaches a minimum of $4.49x10^{-5}$ Ω-cm^2. Increasing the annealing time further degrades the contacts. This may be attributed to the formation of an insulating Al_xO_y layer on the surface of the Al for higher annealing time [3]. As a result measurement of the contact resistance at the GaN interface became more difficult and caused the contact resistance to be artificially high. The lowest

specific contact resistivity of 8.63×10^{-6} Ω-cm^2 was obtained after annealing at 500°C for 25 min on the 3.67×10^{18} cm^{-3} sample. This value is the lowest specific contact resistivity for GaN in the open literature for contacts annealed in N_2 ambient. Lee et al. [5] have reported a specific contact resistivity of 1.2×10^{-8} Ω-cm^2 for Ti/Al contacts annealed at 500°C for 60 min. However, this was for an unintentionally doped GaN having a high electron concentration of 1×10^{19} cm^{-3}.

The reason for ohmic contact formation for n-GaN in the Ti/Al metal system is generally explained as either due to TiN formation or AlN formation as follows:

(1) The chemical reaction at the Ti/GaN interface would form a thin layer of TiN. This is a semi-metal and has a work function of 3.74 eV[8], hence satisfying the condition for low work function metal to form ohmic contact to n-GaN. The N was depleted at the surface of GaN to form TiN. This in turn converts the surface of the n-GaN to be heavily doped enabling the tunneling current at the interface to be responsible for ohmic contact formation [9].

(2) Luther et al. [10] have proposed that Al, which is a low work function metal (4.28 eV), diffuses through Ti during annealing and reaches the n-GaN surface. The Al then reacts with the surface of the GaN to form a thin AlN layer at the interface. This process resulted in N vacancies, which yields a heavily doped interface, resulting in a tunneling current responsible for the ohmic contact formation.

From the literature it should be observed that TiN formation at the Ti/GaN interface occured only at a reaction temperature greater than 600°C [11-12].

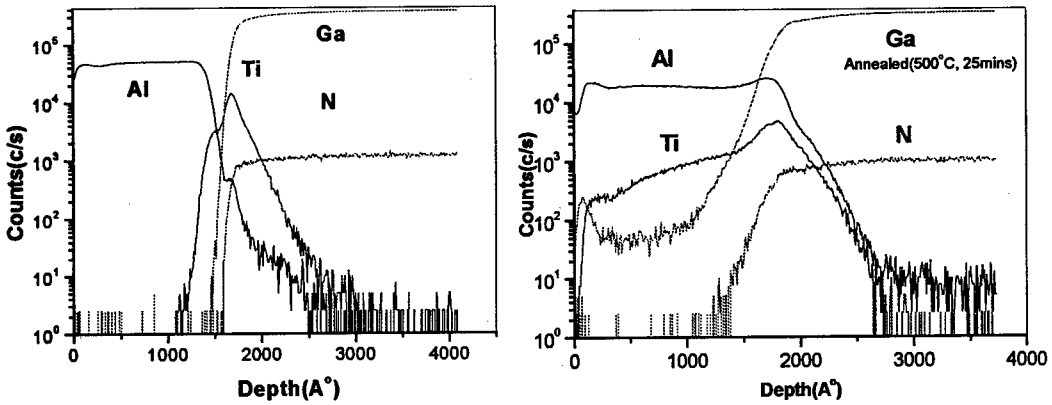

Figure 3: SIMS depth profiles for as-deposited (left panel) and annealed (right panel) Ti/Al contacts on Si doped n-GaN.

In our case, since the annealing temperature was only 500°C, reaction may not have occurred to facilitate in the ohmic contact formation. Figure 3 shows the results of SIMS analysis for the as-deposited and annealed samples. This reveals that for the annealed sample the Al has diffused through the thin Ti(~15 nm) layer to the GaN surface. Thus, either Al as a low work function metal or complex ternary or quarternary Ga, Ti, and Al nitrides compounds with low-barrier heights material to n-GaN, could have resulted in the formation of ohmic contacts with low specific contact resistivity. This same phenomenon has also been observed for Pd/Al metallization scheme, where the Pd interlayer thickness is 12.5 nm[7].

Room temperature photoluminescence spectra were measured with a He-Cd laser as the excitation source (325 nm, ≈10 mW) to observe any detrimental effect on the annealed samples from the optoelectronics device point of view.

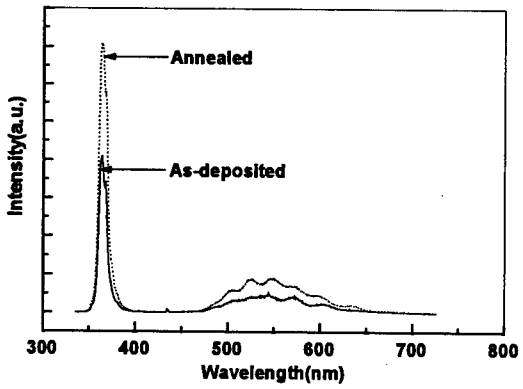

Figure 4. shows the typical PL spectra for the n=3.65x10^{18} cm^{-3} GaN for both non-annealed and annealed cases. It is interesting to note that the intensity of the band-edge emission of the furnace annealed sample (500°C, 25 min) shows a marked increase compared to the as-deposited sample. This shows that the post metallization anneal has not degraded the material. On the contrary, it has improved the crystalline quality of the GaN epitaxial layer.

Figure 4: Typical PL spectra for the 3.67x10^{18} cm^{-3} doped sample.

Conclusion

Specific contact resistivities as low as 8.63x10^{-6} Ω-cm^2 have been achieved on n-typed, intentionally doped GaN epilayers using Ti/Al annealed at a low temperature of 500°C. The annealed samples at this temperature also show that there is no degradation in band-edge PL intensity and thus, no degradation of the epilayer quality

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Materials Science Forum Vols. 338-342 (2000) pp. 1623-1626

Time-Resolved Photoluminescence Measurements of InGaN Light-Emitting Diodes

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Keywords: Carrier Diffusion, Disorder, Time-Resolved Photoluminescence

Abstract We have used time-resolved photoluminescence (TRPL), with 400 nm (3.1 eV) excitation, to examine $In_xGa_{1-x}N$/GaN light-emitting diodes (LEDs) before the final stages of processing at room temperature (RT). We have found dramatic differences in the time-resolved kinetics between dim, bright and super bright LED devices. The lifetime of the emission for dim LEDs is quite short, 110 ± 20 ps at photoluminescence (PL) maximum, and the kinetics are not dependent upon wavelength. This lifetime is short compared to bright and super bright LEDs, which we have examined under similar conditions. The kinetics of bright and super bright LEDs are clearly wavelength dependent, highly non-exponential, and are on the nanosecond time scale (lifetimes are in order of 1 ns for bright and 10 ns for super bright LED at the PL max). The non-exponential PL kinetics can be described by a stretched exponential function, indicating significant disorder in the material. Typical values for β, the streching coefficient are 0.45 – 0.6 for bright LEDs, at the PL maxima at RT.

We have also used TRPL, applying 267 nm (4.65 eV) excitation, to examine carrier diffusion from the p-type GaN layer into the InGaN/GaN multiple quantum wells. The carrier diffusion occurs on the 3-5 ns timescale and can be measured using the risetime of the InGaN emission, the extracted value for diffusion constant is 0.9 cm^2/sec (μ= 35 cm^2/Vs). This value of the mobility is consistent with Hall measurements.

Introduction

Recently there has been world-wide interest in the use of nitride semiconductors (e.g., GaN, InN, and AlN) for opto-electronic devices such as lasers and light-emitting diodes. The large changes in physical properties such as band gap, crystal structure, phonon energy, and electronegativity difference between GaN and GaAs, demonstrate that nitride semiconductors are fundamentally distinct from traditional III-V semiconductors. In spite of the impressive progress made in recent years [1] in the development of LEDs and lasers, significant work needs to be done in terms of the optimization of device performance. In order to achieve this goal, the physics underlying the operation of these devices must be better understood. Furthermore, new diagnostic techniques for the characterization of materials and devices will greatly aid in the long-term commercialization of this technology.

It has been recognized that under typical growth conditions there is a positive enthalpy for indium mixing in GaN. Electron microscopy and cathodoluminescence of InGaN has demonstrated the existence of nanometer and micron scale regions of high indium concentration [2]. It has been hypothesized that the nanoscale regions of high indium concentration are critical to LED operation [1]. We have previously used time-resolved photoluminescence to investigate indium concentration fluctuations, in InGaN/GaN multiple quantum wells and LEDs. In this paper we discuss the result of time-resolved photoluminescence obtained from a set of LEDs with different quantum efficiency.

Carrier diffusion has been investigated in many systems using time-resolved photoluminescence by the application of markers or graded multiple quantum wells. A quantitative understanding of carrier diffusion is critical to the modeling and optimization of InGaN LEDs. In this paper we discuss the use of time-resolved photoluminescence to investigate carrier diffusion in InGaN LEDs at room temperature. We note that in this case, no modifications need to be made to the InGaN LED structure in order to use this technique. Furthermore, this technique is nondestructive and noncontact.

Experiment

The light emitting diodes were grown by metal organic chemical vapor deposition at EMCORE Corp. The average indium mole fraction was about 11 %. LEDs consist of ten layers of $In_{0.11}Ga_{0.89}N$, each 35 Å thick, and nine layers of GaN, each 45 Å thick. The whole structure was on c-plane sapphire with 3 microns of unintentionally doped (n-type $5x10^{16}/cm^3$) GaN as a substrate. The LEDs studied in this work were grown under slightly different conditions, leading to large changes in brightness. After final processing, the electroluminescence from samples was in order of 100 μW, 400 μW and ≥ 2 mW. Based on the electroluminescence efficiency we divide samples in three groups dim, bright, and super bright LEDs.

An amplified and doubled Ti-sapphire laser from Coherent Corporation operating at 250 kHz was used. TRPL measurements were performed with a Hamamatsu streak camera (model C5680). The excitation pulse was at 400 nm (3.10 eV) for TRPL, and the excitation for diffusion measurements was produced by third harmonic generation (267 nm) with a frequency tripler from UNIWAVE Technologies. The excitation power was adjusted by calibrated neutral density filters. The typical response time was 60 ps and was determined by electrical jitter in the triggering electronics. The laser power used was 1.6 mW, 2.56 $\mu J/cm^2$.

Results and discussion

Time-resolved PL data for dim, bright and super bright LED are shown in Fig.1. The lifetime of the emission for dim LED is quite short, 110 ± 20 ps at PL maximum, and the kinetics are not dependent upon wavelength. The short lifetime and low PL intensity of dim LED are due to fast non-radiative recombination processes, which are dominant in this case. This lifetime is short compared to bright and super bright LEDs, which we have examined under similar conditions. The kinetics of bright and super bright LEDs are clearly wavelength dependent, highly non-exponential, and are on the nanosecond time scale. The lifetimes are on the order of 1 ns for bright and 10 ns for super bright LED at the PL max. Such long times are consistent with carrier localization in regions of high indium concentration.

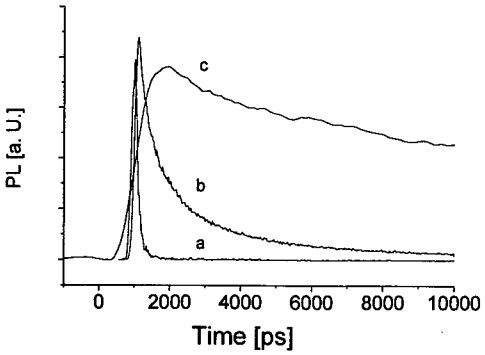

Fig. 1: TRPL from a) dim, b) bright and c) super bright LED.

The non-exponential PL kinetics of bright and super bright LEDs, can be described by a stretched exponential function, Eq.1, where β is between 0 and 1 and I(t) is the PL intensity as a function of time.

$$I(t) = I_0 \exp(-(\frac{t}{\tau})^{\beta}) \qquad \text{Eq. 1}$$

There is growing evidence from our group [3] and others [4-5] that stretched exponential decays correctly describe the PL decays from InGaN under a variety of conditions. Stretched exponential decays are consistent with disorder. By analogy with previous simulations of localized excited states in other semiconductors, the wavelength dependences of β and τ, Fig. 2, imply that excited state migration is important in InGaN LEDs. Temperature dependence measurements (not shown) suggested that the potential fluctuations associated with the disorder (75 meV), are much bigger than RT thermal energy (25 meV). This result implies that the excited states are heavily localized in the LED.

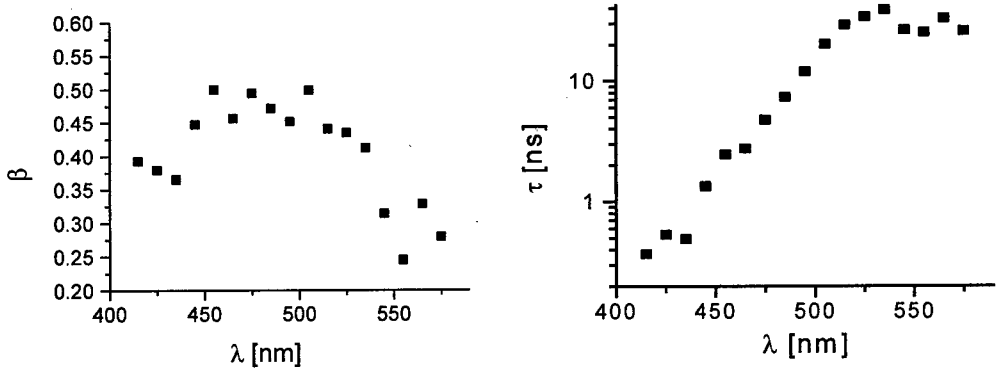

Fig. 2: Analysis of the TRPL from super bright LED. The stretched exponential lifetime is observed to dramatically increase as the emission wavelength is varied from 420 to 500 nm. The PL maximum is at 480 nm.

Figure 2 clearly demonstrates that the stretched exponential lifetime is strongly dependent upon wavelength or emission energy. The data can be successfully fit to an exponential dependence of τ on emission energy.

$$I(t) \approx \exp(-\frac{\hbar\omega}{E_0}) \qquad \text{Eq. 2}$$

For the superbright LED, E_0 was found to be 570 meV, which is much greater than the thermal energy. Similar results were obtained for bright and super bright several LEDs. It can be shown that equation 2 is consistent with a tunneling mechanism [6]. We conclude that the carriers produced in the TRPL experiments migrate between different indium quantum dots by a tunneling mechanism. By using a simple model, the average tunneling distance can be estimated to be approximately 20 Å [6]. Therefore the TRPL data confirms the existence and importance of nanometer scale indium alloy fluctuations on the operation of super bright LEDs.

The PL decays, using 267 nm (4.65 eV) excitation, show the delayed rise in the InGaN emission, Fig. 3. The emission has a risetime of 3-5 ns. Similar results are obtained with bright blue LEDs. Carrier diffusion can be described by solution of a diffusion equation with an additional term to account for recombination. The extracted diffusion constants are 0.9 cm^2/sec, and are in good agreement with the known hole mobilities of typical p-type doped GaN [7].

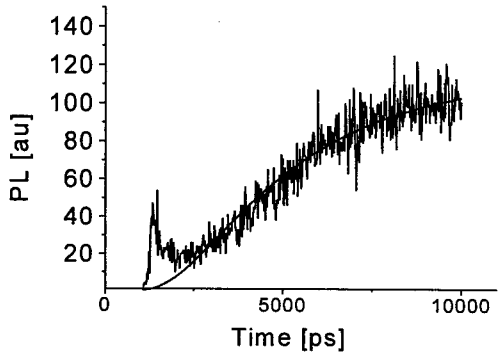

Fig. 3 The slow rise time in the PL is due to the diffusion of carriers from the p-type GaN layer into the InGaN MQW. Diffusion constant is obtained using a simple diffusion model. D = 0.9 cm^2/sec; μ = 35 cm^2/V-sec.

Conclusions

In summary we have used TRPL to examine wafers of InGaN LEDs before the final stages of processing. We have found that in the bright and super-bright LED examined, PL lifetimes at room temperature were on the nanosecond timescale. The PL kinetics were strongly dependent upon the emission wavelength and were well described by a stretched exponential. Both observations are strong experimental evidence for the importance of disorder in actual light emitting diodes. An analysis of the data based on this hypothesis confirms the existence and importance of nanometer scale indium alloy fluctuations on the operation of superbright LEDs.

In addition, we have used time-resolved photoluminescence to investigate carrier diffusion in InGaN/GaN light-emitting diodes. Carrier diffusion is observed on the nanosecond time scale at room temperature in the p-type GaN layer over the InGaN multi quantum layer (MQW) structure. This is consistent with known values for the diffusion coefficient in typical p-type GaN samples.

Acknowledgement

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GaN PIN Photodiodes Grown on Sapphire and SiC Substrates

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Keywords: Dislocation Density, Photodiodes, Substrate Effect

Abstract

GaN PIN photodiodes were grown on both sapphire and SiC substrates to directly compare the device performance. In this paper the growth, fabrication, and characterization of these devices are described. The GaN photodiodes on sapphire have significantly higher dark current densities than similar devices grown on SiC. This reduction in dark current is attributed to a reduction in dislocation density for GaN grown on SiC as compared to sapphire. Characteristics of AlGaN PIN photodiodes grown on sapphire are also described.

Introduction

Visible-blind UV photodetectors have a number of applications including missile detection, flame sensing, and solar UV monitoring. The III-V nitrides are ideal for UV applications due to their wide bandgaps, making detectors transparent to visible and infrared radiation. There have been several studies of GaN photodiodes on sapphire [1,2] but the effects of the substrate on device performance have not been directly investigated. The crystal quality can be considerably affected by the substrate choice for nitride growth, as demonstrated by variations in the x-ray diffraction width or dislocation density of material grown on various substrates. Similarly, the buffer layer used on a given substrate can also significantly impact the material quality of subsequently grown nitride layers, resulting in a variation of material quality grown on the same substrate. Consequently, the substrate and buffer layer effect on device performance could be substantial and affect not only GaN photodetectors but also other GaN-based devices such as high-speed transistors, light emitting diodes (LEDs), and lasers. This effect has already been demonstrated for GaN photoconductive detectors [3]. In this paper, improved device performance is demonstrated for GaN photodiodes grown on SiC compared to devices grown on sapphire.

The dislocation density of GaN layers grown by metal-organic vapor phase epitaxy (MOVPE) on heteroepitaxial substrates such as sapphire and SiC is determined by the lattice mismatch, nucleation technique, and GaN layer thickness. Typical dislocation densities for GaN on sapphire are 10^9 to 10^{10} cm^{-2} due to the substantial lattice mismatch between the two materials (13.8%).

We investigated the use of SiC substrates which enable a reduction in the dislocation density compared to sapphire due to a closer lattice match to GaN (3.4%). Here, we describe and compare the material characteristics and operation of similar GaN PIN photodiodes grown by MOVPE on sapphire and SiC. In addition, AlGaN PIN photodiodes with low aluminum composition grown on sapphire are also described.

Materials Growth and Device Fabrication

The two different substrates used in this study were (0001) sapphire and n-type (0001) 4H-SiC. The GaN layers were grown by MOVPE with an appropriate nucleation layer on each substrate. The epitaxial device layers on the sapphire substrate consisted of 1 μm undoped GaN, 1 μm n-type GaN, 0.5 μm undoped GaN, and 0.2 μm p-type GaN. The epitaxial layers on SiC are similar: 0.5 μm undoped GaN, 1 μm n-type GaN, 0.5 μm undoped GaN, and 0.3 μm p-type GaN. Double crystal x-ray diffraction full-width-at-half-maximum (FWHM) results for these layers were 780 and 226 arcsec on sapphire and SiC substrates, respectively. In general, based on previous TEM measurements, the dislocation density of our material grown on SiC is approximately an order of magnitude lower than similar layers grown on sapphire. Also, the material grown on SiC is smoother than that grown on sapphire by optical inspection in a Nomarski microscope. The 5% AlGaN PIN structure is also a homojunction device with AlGaN n- and p-type contact layers. This structure was similar to the GaN PIN on sapphire but with a 0.25 μm undoped AlGaN layer for the i-layer and a 0.25 μm p-type layer.

Portions of these epitaxial wafers were fabricated into PIN photodiodes. Chlorine-based reactive ion etching was performed to etch through the p-type and undoped GaN layers and expose the underlying n-type GaN. Ohmic contacts were evaporated and patterned by lift-off photolithography. Detectors were fabricated with mesa diameters of 250, 500, and 750 μm. The p-type contact was a single dot, 80 μm in diameter and the n-type contact was a ring around the device mesa. A schematic of a GaN PIN photodiode is shown in Fig. 1.

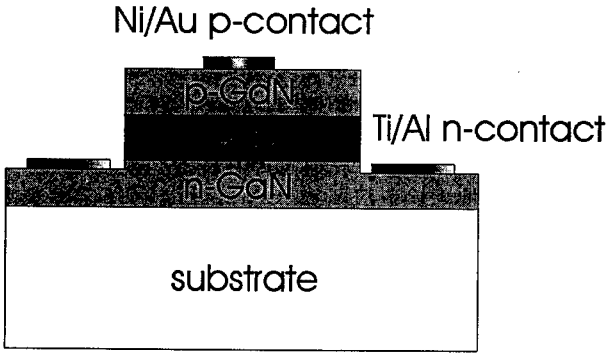

Figure 1. Schematic of a GaN PIN photodiode.

Results

Figure 2 shows the responsivity as a function of wavelength for representative devices from each sample. The GaN photodiodes on sapphire consistently showed higher responsivity than the other samples, which we attribute to a thinner p-type layer on this sample. The strong peak and more rapid decrease in responsivity with decreasing wavelength of the other two samples is indicative of photodiodes with a thicker p-type layer. Devices with more comparable structures are being fabricated for a direct comparison and results will be presented.

The electrical characteristics of the photodiodes indicate a substantial decrease in the dark current of devices grown on SiC as compared to sapphire. Shown in Figure 3 is the dark current density as a function of reverse bias. The dark current density at a reverse bias of 10 V is 1100 and 13 nA/cm^2 for devices on sapphire and SiC, respectively. The 5% AlGaN photodiodes demonstrate very similar dark current densities to the GaN photodiodes with a dark current of 1800 nA/cm^2 at 10 V. This is despite the fact that the i-layer for the AlGaN PINs is half the thickness of the GaN PINs. The almost two orders of magnitude reduction in dark current is attributed to the improved material quality for GaN grown on SiC as compared to sapphire. It is anticipated that further reduction in the dislocation density of the GaN and AlGaN material will result in considerably lower dark current photodiodes such as those recently reported by Parish *et al.* using lateral epitaxial overgrowth [4].

Acknowledgement

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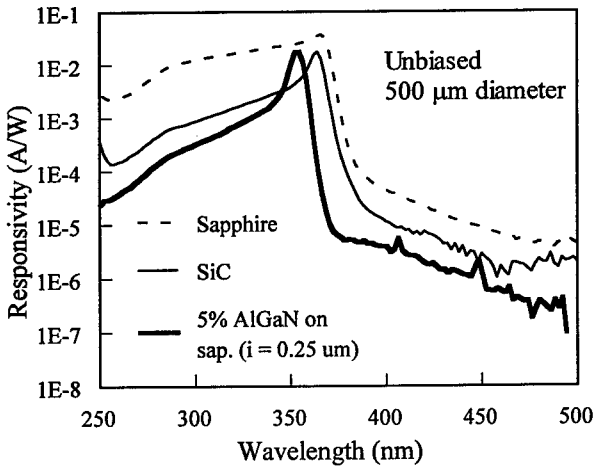

Figure 2. Responsivity as a function of wavelength for representative 500 μm diameter GaN PIN photodiodes with 0.5 μm i-layers grown on sapphire or SiC substrates. Also shown is a representative 5% AlGaN PIN photodiode with 0.25 μm i-layer grown on sapphire.

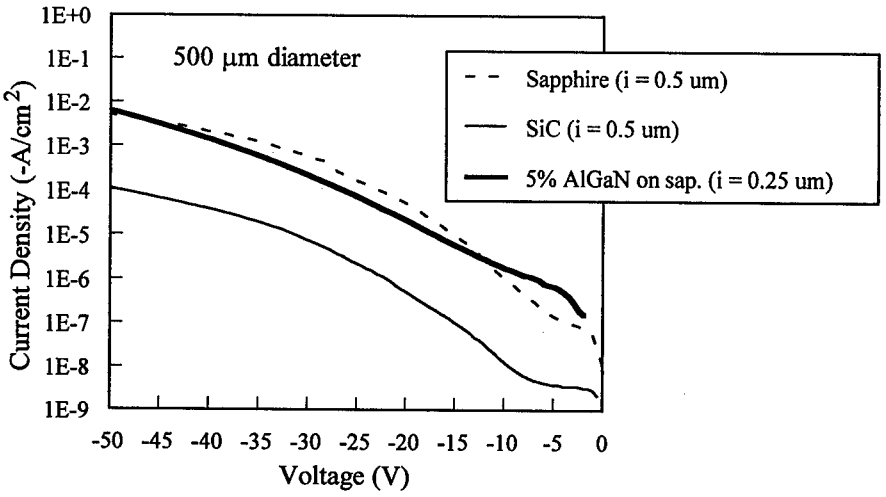

Figure 3. Dark current density as a function of reverse bias for representative GaN PIN photodiodes with 0.5 μm i-layers grown on sapphire or SiC substrates. Also shown is a representative 5% AlGaN PIN photodiode with 0.25 μm i-layer grown on sapphire.

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Temperature Dependent Performance of GaN Schottky Diode Rectifiers

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Keywords: Breakdown Voltage, Schottky Diodes, Temperature Dependence

Abstract GaN Schottky diode rectifiers with reverse breakdown (V_{RB}) > 2 kV were fabricated on epitaxial layers grown on sapphire substrates. The temperature dependence of V_{RB} and forward turn-on voltage (V_F) were measured. The V_{RB} values display a negative temperature coefficient (-0.92 $V \cdot K^{-1}$ for 25-50 °C; -0.17 $V \cdot K^{-1}$ for 50-150 °C), indicative of surface- or defect-assisted breakdown. The V_F values decrease with increasing temperature. The room temperature breakdown voltage is approximately a factor of three lower than the theoretical maximum expected based on avalanche breakdown, and the current performance of GaN rectifiers is comparable to that of Si at the same on-resistance.

Introduction

Wide bandgap semiconductors such as SiC and GaN offer many advantages for fabrication of diode rectifiers, including high breakdown voltages and operating temperatures [1-3]. Schottky diodes are employed as high-voltage rectifiers in power switching applications. To suppress voltage transients when current is switched to inductive loads such as electric motors, these diodes are placed across the switching transistors. The advantage of simple metal-semiconductor diodes relative to p-n junction diodes is the faster turn-off because of the absence of minority carrier storage effects and lower power dissipation during switching .

In this paper we report on the temperature dependence of reverse breakdown voltage (V_{RB}) and forward turn-on voltage (V_F) in GaN diodes fabricated on thick (3-12 μm total) GaN layers grown by Metal Organic Chemical Vapor Deposition (MOCVD). We find that both V_{RB} and V_F decrease with increasing measurement temperature.

Experimental

The GaN samples were grown by MOCVD on c-plane sapphire in two different systems using ammonia (NH_3) and trimethylgallium (TMG) as the precursors. In one case 3-11 μm thick undoped GaN layers were grown on top of a 1 μm thick n^+ GaN region, while in the other case 3 μm of high resistivity GaN was grown on a 300 Å thick novel buffer layer. The 4-12 μm thick structures were used for fabrication of vertically-depleting diodes, while the 3 μm thick structure was found to deplete laterally. In the former devices, a mesa down to the n^+ region was formed by Cl_2/Ar Inductively Coupled Plasma etching under low-damage conditions, while

in the latter devices selective-area n^+ ohmic contact regions were formed by Si^+ implantation followed by annealing at 1125 °C. Ohmic contacts were formed by lift-off of Pt/Au. The ohmic contacts were annealed at 750 °C for 20 secs prior to deposition of the Pt/Au.

Results and Discussion

Figure 1 shows some typical data for the temperature dependence of V_{RB} in the diodes fabricated on 4μm thick active layers. Clearly the V_{RB} decreases with temperature, i.e. there is a negative temperature coefficient. If impact ionization were the cause of breakdown, we would expect a positive temperature coefficient. There have been reports of positive temperature coefficients for V_{RB} in various GaN devices, including heterostructure field effect transistors, p^+pn^+ diodes and p-i-n diodes [4-6]. The fact that in our diodes the V_{RB} decreases with increasing temperature indicates that a possible mechanism is defect-assisted tunnelling through surface or defect states.

Figure 2 shows the temperature dependence of V_{RB} in our diodes. The breakdown voltage decreases with increasing measurement temperature, but the decrease is not linear. The temperature coefficient is $-0.92\ V{\cdot}K^{-1}$ in the range 25-50 °C and $-0.17\ V{\cdot}K^{-1}$ in the range 50-150 °C. In a simplistic picture, the breakdown voltage scales with the fourth power of the bandgap. The bandgap of GaN has a negative temperature coefficient, variously reported between 0.39-0.67 $meV{\cdot}K^{-1}$ [7-8]. Therefore, V_{RB} would decrease with increasing temperature in this model, which assumes no surface breakdown.

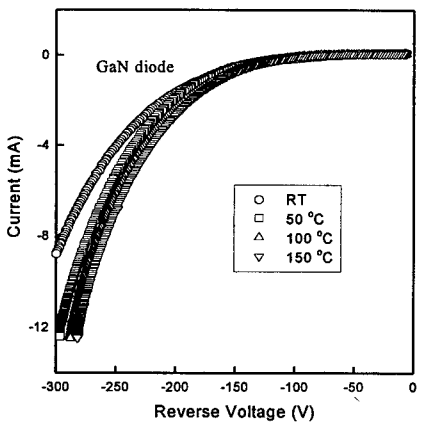

Figure 1. Reverse I-V characteristics from a 4 μm thick active layer diodes taken at different measurement temperatures.

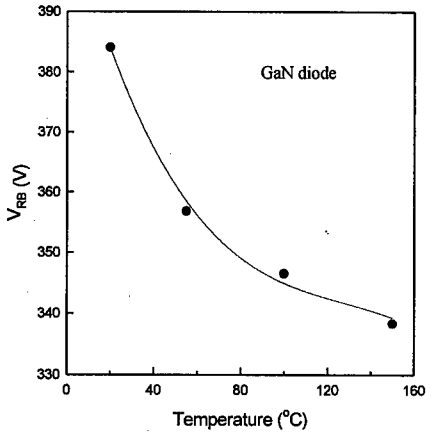

Figure 2. Temperature dependence of V_{RB} in vertical GaN Schottky diodes with 4 μm thick active regions.

Our results from this diode showed that the forward turn-on voltage decreased from 3 V at 25 °C with increasing temperature as $\exp(\frac{1}{T})$, where T is the absolute temperature of the sample. The turn-on voltages observed are still well above the theoretical values, and the specific on-resistances are essentially comparable to those of perfect Si devices, indicating there is more work to be done on both the ohmic and rectifying contacts for this material.

We obtained V_{RB} values of ~550 V and >2 kV for the 11μm thick active layer vertical diodes and 3 μm thick lateral devices, respectively, at 25 °C. To place these results in context, Figure 3 shows theoretical plots of V_{RB} versus depletion layer thickness and doping for hexagonal GaN, along with experimentally determined values. Note that for most of the diodes reported to date the breakdown voltages are approximately a factor of 3 lower than the theoretical values. This is likely due to a combination of the high dislocation densities and relatively high compensation levels in state-of-the-art GaN grown on sapphire. However, the 3 μm thick diode reported in this work has a V_{RB} well above the theoretical value. This suggests that the depletion is lateral in the device, and that V_{RB} would depend on the contact separation.

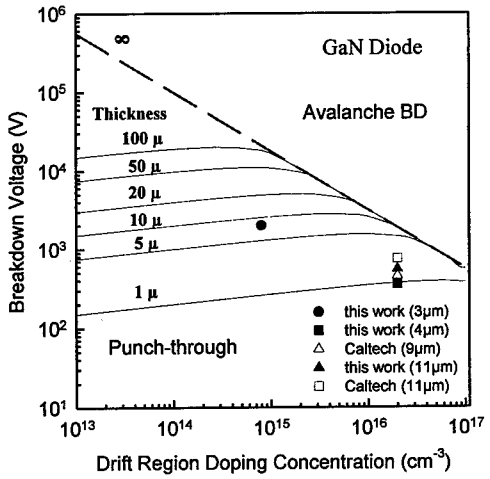

Figure 3. Calculated breakdown voltage as a function of doping and epi thickness in GaN Schottky diodes. Experimental points from Caltech work [3] and this work are also shown.

Figure 4 shows a compilation of reverse current density data for recently reported SiC and GaN diodes, as a function of reverse bias. [9] It is clear that some SiC devices are relatively close to optimal performance, at least for biases less than ~1000 V. At higher biases, both GaN and SiC diodes show relatively high reverse current densities. We have generally found in our diodes that at low reverse biases (<50 V) the reverse current was proportional to the size of the contact perimeter, indicating the domination of perimeter leakage currents. By sharp contrast, at higher biases the current was proportional to diameter squared. This indicates that bulk leakage is the primary contributor under these conditions. It is likely this latter current results from the problems discussed earlier, i.e. dislocations and impurities.

Summary and Conclusions

High breakdown voltage GaN diode rectifiers have been fabricated on MOCVD-grown epi layers. Mesa diodes on structures with an 11μm thick undoped layer showed V_{RB} of 550 V and extremely low specific on-resistance (6-10 mΩ·cm^2). Planar diodes on structures with a 3 μm thick high resistivity layer showed V_{RB} >2000 V, which is above the theoretical value for a vertically-depleting device. Lateral diodes or thyristors involving implant doping for contacts or junction formation may be a promising approach for ultra-high power GaN device. This

approach would avoid the necessity to remove the dry etch damage inherent in mesa diodes. All of the diodes display negative temperature coefficients for V_{RB}, emphasizing the need for improved surface passivation methods.

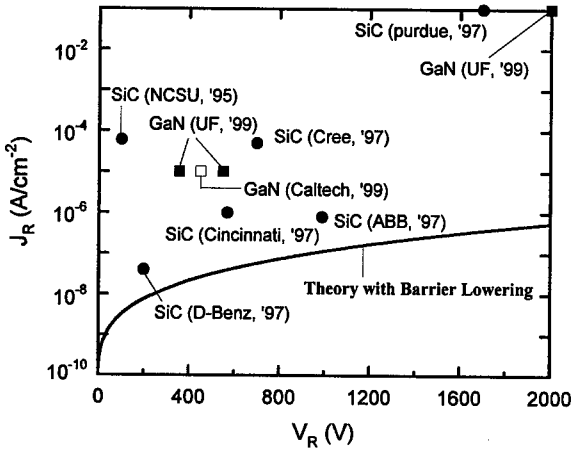

Figure 4. Reverse current density in GaN and SiC diodes as a function of reverse bias voltage. The solid line is the theoretical value for 4H-SiC (after ref. 9).

Acknowledgements

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Materials Science Forum Vols. 338-342 (2000) pp. 1635-1638

Monte Carlo Simulation of Gunn Effect and Microwave Power Generation at 240 GHz in n^+-n^--n-n^+ GaN Structures

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Keywords: Microwave Generation, Monte Carlo Simulation, Transferred Electron Devices

Abstract: Electron transport, Gunn oscillation condition and microwave power generation in n^+-n^--n-n^+ GaN structures have been studied by Monte Carlo Particle simulation which solves BTE and Poisson's equation along with the equations governing the associated circuit elements and a parasitic contact resistance. Temperature and frequency dependence of microwave power generation and conversion efficiency will be presented for zincblende GaN n^+-n^--n-n^+ transferred electron devices (TEDs) in a parallel resonant circuit.

Introduction: The negative differential resistivity (NDR) in GaN was predicted in 1975 [1]. Twenty years later the NDR in GaN was observed by Huang et al. [2]. Some publications appeared recently on Monte Carlo simulation of high field transport in GaN [3,4]. The ensemble Monte Carlo (MC) calculation including a full band zone structure gives the NDR threshold field values of 110 kV/cm for zincblende and 180 kV/cm for wurtzite GaN modifications [3]. The latter is close to the experimentally observed 191kV/cm [2]. The MC calculations using three valleys model with nonparabolicity [4] show that the approach is a good approximation in comparison with the full band simulation [3]. Investigation of the velocity overshoot and electron transit time at high electric fields shows that GaN, especially zincblende GaN, is better than that of GaAs for high frequency power generation [4]. To quantify this point, it is necessary to investigate the high field carrier transport in GaN microwave device structures. In this paper we present the Monte Carlo Particle (MCP) simulation of electron transport in n^+-n-n^+ GaN structures and microwave power generation in notched n^+-n^--n-n^+ GaN TEDs. Because of the difficulty in achieving negligibly low contact resistance for GaN and the importance of skin effect at very high frequency, an effective parasitic resistance is included in the MCP simulation to quantify the effects of parasitic resistance on microwave power generation.

Monte Carlo Particle Simulation: The simulations are performed for n^+-n^--n-n^+ GaN structures with the corresponding doping concentrations of $10^{18}cm^{-3}$ -1 to $50x10^{16}cm^{-3}$ - $10^{18}cm^{-3}$ and the corresponding layer thickness of 0.05μm - 1 to 10 μm - 0.2 μm. The zincblende and wurtzite GaN material parameters for the MCP program are taken from [4]. The scattering mechanisms included in the simulations are polar optical phonon, ionized impurity, deformation potential, as well as intervalley scattering. As the first step, the electron transport in the structures is investigated under constant bias voltage V_0 for different active region length l(1 to 10 μm) and doping level n(1 to $50x10^{15}cm^{-3}$). It is found that when $nl > 5\times 10^{12}cm^{-2}$ current oscillation arises for both zincblende and wurtzite GaN due to the formation, motion and dissipation in the anode contact of accumulation layers, as expected for the Gunn effect devices. It should be pointed out that the criterion for Gunn oscillations is about 5 times greater than that of GaAs and InP

devices. This is due to the larger effective mass in the Γ-valley of GaN and the much stronger scattering in this valley at low electric fields as compared with GaAs and InP. Fig. 1 shows the current - voltage relations for the 10μm long zincblende (dashed curve) and wurtzite (solid curve) GaN structures with the active region doping equal to $10^{16}cm^{-3}$ and an n*l* product equal to $10^{13}cm^{-2}$. Fig.1 is plotted up to the thresholds of current oscillations and the inset shows the high frequency oscillations beyond the threshold for zincblende structure. The threshold for zincblende GaN device is 120 kV/cm and for wurtzite GaN device is 180 kV/cm. These are in close agreements with the bulk zincblende and wurtzite GaN negative differential resistivity thresholds of 110 and 180kV/cm [3], respectively. The analysis of the time dependencies of concentration, velocity and electric field profiles under current oscillation conditions shows that the accumulation layer moves with a speed of about $2.2\times10^{7}cm/s$. The oscillation period is, therefore, 25 ps, as shown by the inset in Fig. 1. Fig. 2 (a-c) presents the profiles of concentration, velocity, and electric field in the 10μm long zincblende GaN structure during current oscillations at a bias of V_0 = 140 V. Curves a, b, c and d in Fig. 2 are plotted with a time interval of 5 ps. Fig. 2(a) clearly shows the formation, growth and drift of accumulation layer. The corresponding velocity and field distributions are shown in Fig.2(b) and (c), respectively. It is clear that GaN devices can generate microwave power at considerably higher frequencies than GaAs and InP devices of same geometry because the accumulation layer in GaN moves at a speed twice of that of InP and GaAs devices.

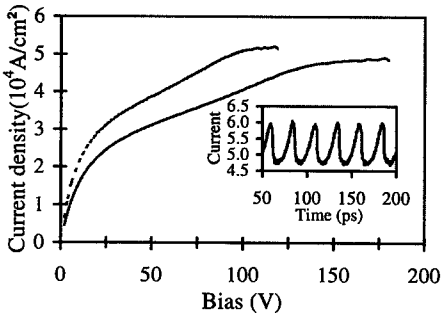

Fig.1: I-V relations for zincblende (dashed curve) and wurtzite (solid curve) GaN n^+-n-n^+ structures. Inset shows current oscillation for zincblende GaN structure.

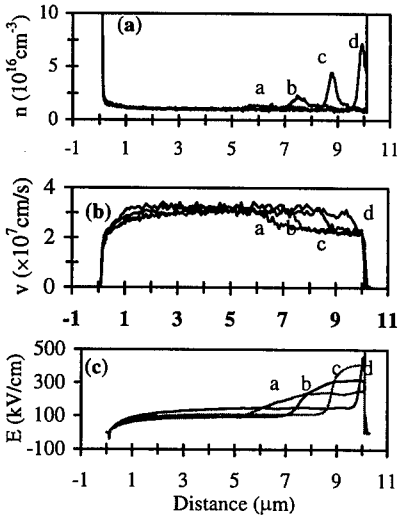

Fig.2: Profiles of carrier concentration (a), velocity (b), and electric field (c) in zincblende GaN structure

Monte Carlo Particle TED Simulation: Microwave power generation is investigated by MCP simulations by directly connecting the n^+-n^--n-n^+ structure in a parallel resonant circuit. A standard R = 50Ω load resistor and a capacitor C are connected in parallel with an inductor L and then in series with the device. The generation frequency is tuned by the capacitor C. The number of simulated particles, depending on the case, varies between 5000 and 20000. The time step in all cases is 1 fs. Such a short time step is needed for the correct account of the possible plasma effects in highly doped cathode and anode regions. It should be pointed out that the high NDR threshold field in zincblende GaN will inevitably lead to a high consumed power in GaN TEDs. To the best of our knowledge the maximum dissipated power over 4 MW/cm^2 have been demonstrated in Si IMPATT diodes in pulsed mode operations [5]. In GaN, higher power dissipation in the pulsed mode operation can be reasonably expected because GaN has a large bandgap and can be operated at much higher temperatures. Hence, in our device simulation, a

notched doping profile of the active region is designed to limit the power dissipation in the range of a few MW/cm^2. All the microwave power generation simulation results to be presented are given for an n^+-n^--n-n^+ zincblende GaN structure with corresponding dimensions of 0.05 - 0.2 - 0.8 - 0.2μm. The doping concentrations are $n^- = 10^{16}cm^{-3}$, $n=5\times10^{16}cm^{-3}$, and $n^+ = 10^{18}cm^{-3}$. To get the maximum microwave power conversion efficiency at a load resistance of R = 50Ω, the cross sectional area of the structure is simulated and found to be 600μm^2. The inductance of parallel resonant circuit is L = 2.5pH and the microwave generation frequency is tuned by capacitance C, which is varied in the range from 0 to 0.4 pf. The simulated frequency dependencies of the generated power and efficiency in zincblende GaN at different biases are illustrated in Fig. 3 (a) and (b). The generation starts at V_0 = 13V, when the average field is slightly over the NDR threshold. The generated power (Fig. 3 (a)) and efficiency (Fig. 3 (b)) are increasing with the applied bias. The microwave power generation is simulated up to V_0 = 25 V when the dissipated power reaches 7 MW/cm^2. It is seen that a very high microwave power in a wide frequency range can be generated by the GaN device. At 240 GHz the device can generate more than 0.5W power. This power is more than 3 times greater than the theoretically predicted peak power of 150 mW at 140 GHz for a 1μm long InP device [6]. This result is not very surprising because the NDR threshold in GaN is about ten times higher than that of InP. Another important advantage of GaN devices is the very high value of NDR. Our small-signal impedance calculations (see Fig. 3 (b)) show that the device negative specific resistance (DNSR) at 225 GHz is $10^{-4}\Omega cm^2$. This DNSR value is close to that in similar InP devices at a much lower frequency of 140 GHz [6].

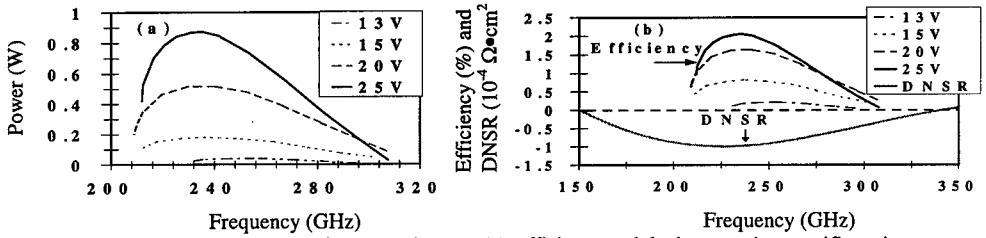

Fig.3 Frequency dependence of generated power (a), efficiency and device negative specific resistance (DNSR) (b) for zincblende GaN TED under different biases.

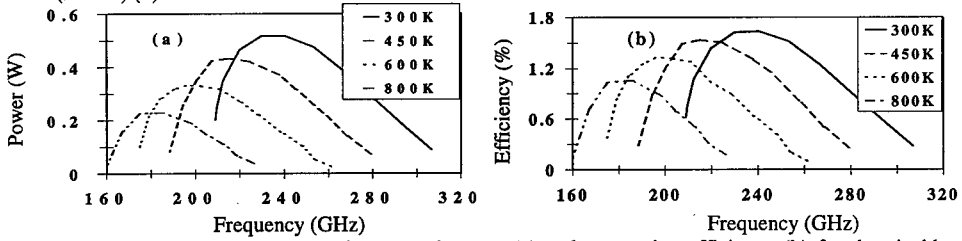

Fig.4: Frequency dependence of generated power (a) and conversion efficiency (b) for the zincblende GaN TED under different temperatures.

It is well known that the device active region temperature can be much higher than the ambient temperature. This usually leads to a strong degradation of the generated power and efficiency. Therefore, we have performed simulations for power generation in the notched GaN TED over the temperature range of 300 K to 800 K. Fig. 4 (a) and (b) present the power and efficiency spectra dependencies on temperature when the notched GaN TED is biased at V_0 = 20 V. It is seen that GaN devices can deliver high microwave power at temperatures up to 800 K. The frequency range of power generation shifts to lower frequencies because the drift velocity decreases when temperature is increased. It is interesting to note that the power generated at

212GHz by the structure actually increases from 300 mW at 300 K to 420 mW at 450 K. Over 450 K, the generated power starts to decrease. The dissipated power is always found to decrease with increasing temperature. For the case shown in Fig. 4 the dissipated power is 5.1, 4.8, 4.2, and 3.6 MW/cm^2 at 300 K, 450 K, 600 K, and 800 K, respectively. Therefore, the pulsed mode operation at elevated temperatures may be possible. Because of the difficulty in achieving negligibly low specific contact resistance and the increasing skin effects at the high frequency range considered in this work, detailed MCP simulations have been done with a parasitic resistor accounting for an effective specific contact resistance up to 10^{-5} ohm-cm^2 range. The results are shown in Fig.5 (a) and (b). It is seen that the contact resistance can drastically reduce the available output power and conversion efficiency. At 25V bias, output power available is decreased to a few tens of mW for an effective contact resistance up to about 3.7×10^{-5} ohm-cm^2.

Conclusion: We have investigated the Gunn effect in n^+-n^--n-n^+ GaN structures by Monte Carlo Particle simulation. It is found that current oscillation under a constant voltage bias is possible when the structure parameters fulfill the relation of $nl>5\times10^{12}$cm^{-2}. The threshold fields for Gunn effect in zincblende and wurtzite GaN devices are 120 and 180 kV/cm, respectively. The accumulation layer velocity in the GaN structures is about 2.2×10^7cm/s, which is twice the velocity of InP and GaAs structures. This means that GaN devices can be operated at considerably higher frequencies than InP or GaAs devices of similar dimensions. The high Gunn effect thresholds in the GaN structures can lead to high microwave power generation. Our simulation of the 1μm long notched n^+-n^--n-n^+ GaN TED in the parallel resonant circuit with a standard 50Ω load resistor at room temperature gives a microwave power of 0.5 W at 240 GHz, which is more than 3 times higher than the theoretically predicted peak power from similar InP device at 140 GHz. The simulation shows the excellent performance of GaN transferred electron devices at high temperatures. No significant decrease of generated power and efficiency is observed for temperatures up to 450 K. Moreover, the power generated by the GaN device at T = 800 K still exceeds the power available from similar InP device at room temperature. Parasitic resistance effects have been modeled and lower than 3.7×10^{-5}ohm-cm^2 effective specific contact resistance is needed in order to generate a few tens of mW power at 240 GHz.

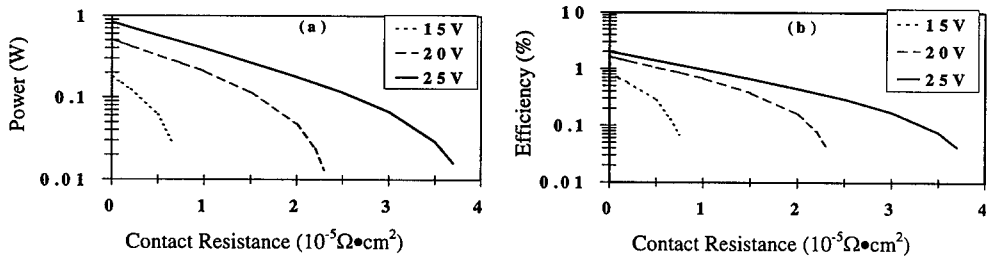

Fig.5: Specific contact resistance dependence of generated power (a) and conversion efficiency (b) for the zincblende GaN TED under different biases.

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Materials Science Forum Vols. 338-342 (2000) pp. 1639-1642

DC and Large-Signal RF Performance of Recessed Gate GaN MESFETs Fabricated by the Photoelectrochemical Etching Process

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Keywords: Maximum Frequency, MESFET, Photoelectrochemical Etching, RF

Abstract In this paper, we report on the DC and large-signal RF performance of recessed gate GaN MESFETs fabricated using the photoelectrochemical etching process. The fabricated GaN MESFET exhibits a current saturation at V_{DS} = 4 V and a pinch-off at V_{GS} = -3 V. The peak drain current of the device is about 230 mA/mm at 300 K and does not significantly change with temperature up to 500 K operation. The f_T and f_{max} from the device are 6.35 GHz and 10.25 GHz, respectively. The experimental device characteristics were compared with the results obtained by the large-signal RF model utilizing the harmonic balance techniques. The simulated power added efficiency (PAE) was about 40 % at an operating frequency of 4 GHz.

1. Introduction

Interest in field effect transistors (FETs) for high power and high temperature application has attracted attention to GaN-based semiconductors because of their properties such as wide band gap, high electron velocity, and high electric field at breakdown voltage[1]. The devices fabricated from these materials are predicted to offer superior DC and RF performance compared to more conventional Si and GaAs devices[2]. Many prototype devices have been successfully fabricated and have demonstrated their potential for the application to high power microwave systems[3, 4, 5]. Despite the excellent electronic properties of GaN, however, the fabrication of GaN metal – semiconductor FETs (MESFETs) with novel designs have been hindered by the chemical inertness of this material. A MESFET with an optimally recessed gate design allows higher output power and higher transconductance than from the characteristics of a conventional flat type structure. The advantages of the recessed structure over the flat structure mainly stem from the relaxation of the electric field at the drain region and the suppression of the source parastic resistance. The fabrication of the recessed gate structure requires highly controlled etching technique which results in low damage on the etched surface. Due to the chemical inertness of GaN, however, several dry etching methods have been proposed and are commonly used for the fabrication of GaN-based devices[6, 7, 8]. However, these techniques are known to result in ion-induced damage on the etched surface, which is highly undesirable for the high frequency and high power operation of MESFETs. Wet chemical etching is a desirable substitute for dry etching method by providing low damage on the surface of active region. In this paper, we report on the fabrication of the recessed gate GaN MESFETs, where a photoelectrochemical etching process is employed with a photoresist mask. The experimental device characteristics were compared with the results obtained by the large-signal RF model utilizing the harmonic balance techniques. The simulation was used to find out optimized device performance.

2. Experiments

The sample for this experiment consisted of 2 - 3 μm -thick undoped ($1.2 \times 10^{17}/cm^3$) n-GaN and Mg-doped ($1.3 \times 10^{16}/cm^3$) p-GaN layers grown on c-plane sapphire substrates by metalorganic chemical-vapor deposition (MOCVD) method. The source and the drain ohmic contacts, with a contact resistance of 3×10^{-6} Ω cm^2, were obtained by the deposition of Ti/Al bilayers followed by a rapid thermal annealing (RTA) at 700 ℃ for 20 seconds. The schottky contact was formed by using a Pt/Au alloy, and it showed a good blocking capability. The gate length and the gate width of the device were 0.7 μm and 100 μm, respectively. The spacing between the gate and the source or the drain was 5 μm. The recessed gate structure of MESFETs were obtained by using a photoresist mask in the photoelectrochemical etching of an n^+ cap layer with a thickness of 1000 Å. The etching rates for the 0.5 mol % and 1.0 mol % solutions of KOH were about 460 Å/min and 1600 Å/min, respectively. The operation of recessed gate GaN MESFETs was investigated using a large-signal RF frequency model simulator[9, 10]. The simulator accepts as input data semiconductor material parameters, device structure, bias conditions, and d.c. and RF circuit impedance information and delivers as output dc and RF performance data such as d.c. bias currents, RF output power, gain, power-added efficiency, input and output impedances, and spectrum. The maximum frequency was calculated from the power gains at different operating frequencies.

3. Results and Discussion

Figure 1 shows the morphology of the etched surface, which displays a well-defined etched edge. This figure demonstrates that the photoresist can be used as a suitable pattern mask in this wet etching process. The etching rates for the 0.5 mol % and 1.0 mol % solutions of KOH were about 460 Å/min and 1600 Å/min, respectively. Note that the etching rate observed in this experiments is comparable with (0.5 mol %), or higher than (1.0 mol %) the etching rate achieved by a typical reactive ion etching (RIE) method. The surface rms roughness of the as grown GaN wafer and the wet etched surface were characterized by AFM and the measured values are 3.26 and 37.7 Å, respectively. The sample in this figure was etched (DC bias of 2.5 V, UV Power of 35 mW) to a depth of about 2000 Å. Figure 2 (a) compares the experimental and simulated current - voltage characteristics. The gate voltage step is - 1 V and the saturation of the source-drain current occurs at $V_{ds} = 4$ V and the pinch-off voltage occurs at $V_{gs} = -3$ V. The maximum drain-source current of the device operating at 300 K is about 230 mA/mm and any significant change was not made at 500 K. Figure 2 (b) shows the temperature dependence of the drain-source peak current of the device in a temperature range between 300 K and 500 K. The insensitivity of the drain current level with temperature may be caused, presumably, by a high activation energy of dopants for ionization and the traps of carriers at the sub-grain boundaries in GaN films. GaN thin films are known to possess a high density of sub-grain boundaries, which are responsible for band-bending[9]. The driving force for electrons to overcome the transverse grain boundaries is better provided by a device operating at higher temperatures. Thus, the mobility of electrons at higher temperature could be higher than that at lower temperatures. Figure 3 (a) compares the experimental and simulated frequency characteristics of the device. The RF performance shows a cut-off frequency and a maximum frequency of 6.25 GHz and 10.25 GHz at $V_{gs} = 0$ V, $V_{ds} = 8$ V, respectively. The simulated maximum frequency matches well with the experimental results.

The large-signal RF model calculates the power added efficiency (PAE), output power, and power gain at different frequencies. The simulated maximum frequency was calculated from the power gains at different frequencies. The PAE and output power degraded with increasing frequency. Figure 3(b) is a typical large-signal RF (4 GHz) performance of the simulated device showing about

40 % of PAE and of output power (at V_{gs} = 0 V). Further investigation using the simulator suggested that the maximum frequency could be enhanced by the optimization of the impedence matching during the device characterization.

4. Conclusion

The DC and large-signal RF performance of recessed gate GaN MESFETs fabricated using the photoelectrochemical etching process was investigated. The fabricated GaN MESFET exhibits a current saturation at V_{DS} = 4 V and a pinch-off at V_{GS} =-3V. The peak drain current of the device is about 230mA/mm at 300 K and the value is remained almost same for 500K operation. The f_T and f_{max} from the device are 6.35 GHz and 10.25 GHz, respectively. The experimental device characteristics were compared with the results obtained by the large-signal RF model utilizing the harmonic balance techniques. It was suggested from the simulation that the frequency performance of the device could be enhanced by the optimization of tuning during the device characterization.

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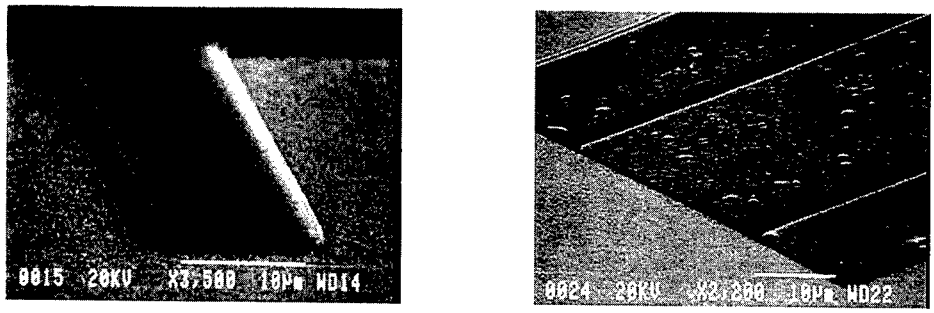
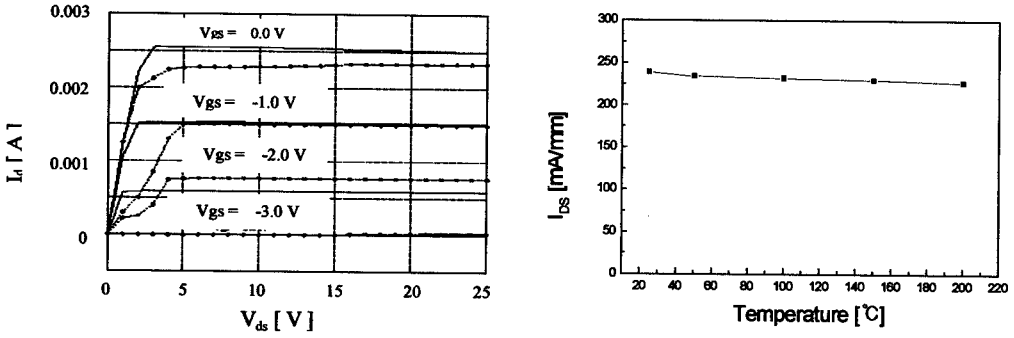


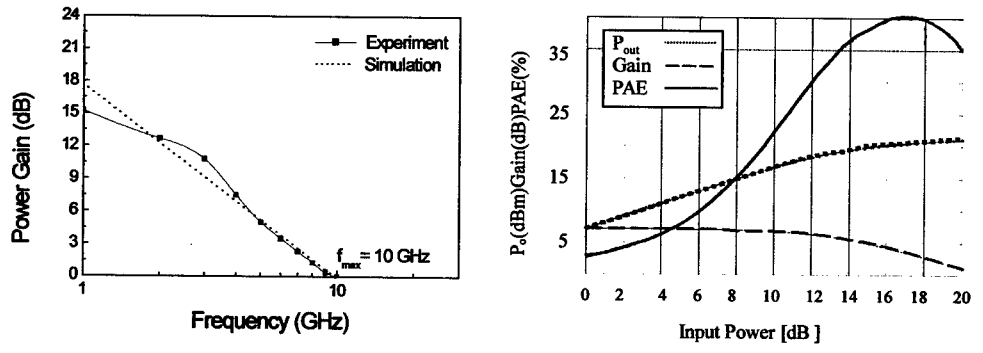
(a) (b)

Fig. 1 SEM micrograph for the surface morphology of etched edge (a) of GaN thin film and of etched mesa. (b) The etched edge is well definded by the photoelectrochemical etching using the photoresist mask.



(a) (b)

Fig. 2 (a) Comparison of the experimental and simulated current - voltage characteristics and (b) the temperature dependence of the drain peak current of a recessed gate GaN MESFET.



(a) (b)

Fig. 3 (a) Comparison of the experimental and simulated frequency performance and (b) the simulated large-signal performance of the device operating at 4GHz.

Materials Science Forum Vols. 338-342 (2000) pp. 1643-1646

Improved 10-GHz Operation of GaN/AlGaN HEMTs on Silicon Carbide

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Keywords: HEMT, High Efficiency, Microwave Power, Semi-Insulating SiC, X-Band

Abstract. GaN/AlGaN epilayers were grown on semi-insulating silicon carbide by MOCVD and fabricated into high electron mobility transistors (HEMTs) with 0.45-μm gate lengths. Standard 0.25-mm HEMTs with an Al molar fraction of 16% demonstrated an extremely high power-added efficiency of 60% and 3.7 W/mm when measured under deep Class AB conditions at 10 GHz. High power densities were maintained even on HEMTs with multi-mm gate peripheries, where a 2-mm-wide device has demonstrated a total output power of 8.3 W (4.15 W/mm) at 10 GHz with a PAE of 33% when measured under Class AB conditions. HEMTs with gate peripheries of 6-mm were demonstrated for the first time, which exhibited typical saturated drain currents of 5.2 A and extrinsic transconductances of 1 S.

1. Introduction

GaN/AlGaN HEMT technology is maturing quite rapidly, due in part to the aggressive development of III-Nitride growth and processing techniques related to the commercialization of blue and green emitters [1]. HEMTs fabricated in the GaN/AlGaN material system can generate large amounts of RF power because of a unique combination of material characteristics, including: (a) high breakdown fields due to the wide bandgaps; (b) large conduction band offset; (c) piezoelectric strain effects; and (d) high saturated-electron drift velocity. In addition, the high thermal conductivity of semi-insulating (SI) SiC substrates enables a higher power handling capability for large periphery devices as compared to those grown on sapphire substrates[2]. The recent demonstrations of extremely high power density and total RF power from GaN/AlGaN HEMTs on SI SiC substrates [2-4] give a strong incentive for further development. Because of the potential for improved performance over GaAs-based devices, the GaN/AlGaN-on-SiC HEMT is generally viewed as the RF power device on which to base next generation X-band power amplifiers, but it is contingent on improvements in power-added efficiency (PAE), increases in total device periphery, and device reliability. Here we present new results showing devices with improved efficiency for a 0.25-mm periphery and improved power density and total power for multi-millimeter peripheries at 10 GHz.

2. Device Fabrication

In our devices, GaN/AlGaN epilayers are grown on SI 4H-SiC wafers by MOCVD using an insulating AlN buffer layer to achieve high quality GaN. The general epilayer structure of the devices described here is comprised of a thin AlN nucleation layer, 2 μm of undoped GaN and

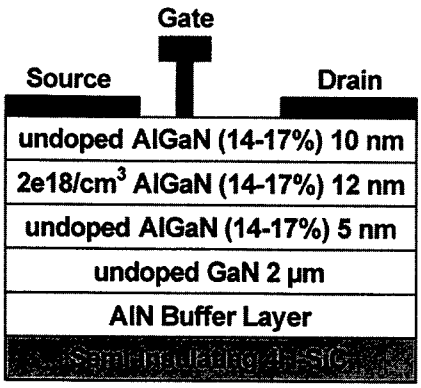

Fig. 1: Schematic cross-section of the GaN/AlGaN HEMT on SI SiC substrates.

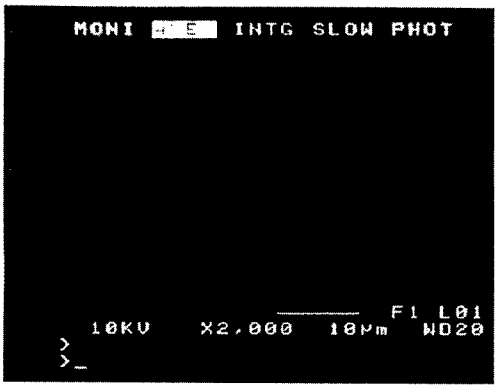

Fig. 2: SEM microphotograph of a finished HEMT structure, showing thick metal over the ohmic contacts, Au airbridges, and T-gates that are offset towards the source.

27 nm of $Al_xGa_{1-x}N$ with Al molar fractions in the range of 14-17%. As shown in Fig. 1, the AlGaN cap is nominally grown with a 5 nm undoped spacer layer, a 12 nm Si-doped donor layer (~2e18/cm^3), and a 10 nm undoped barrier layer. Device isolation is achieved with mesa etching to a depth of 200 nm, using an RIE process that yields smooth surfaces and sloped sidewalls. Ohmic contacts are formed by liftoff of Ti/Si/Ni contacts annealed at 900 °C. These contacts have a very smooth morphology, in contrast to other contact metallurgies that have been used for GaN [5], and the contact resistances were in the range of 0.75-1.25 Ω-mm, depending on the actual thickness of the AlGaN cap layer. Standard T-gates with 0.45-µm gate lengths, and 2.0 µm-thick gold overlayer metal is employed. Finally, an Au airbridge process is used to achieve source connections for multi-millimeter gate peripheries. An SEM photomicrograph in Fig. 2 shows the salient features of the airbridge and T-gate technologies used in this process.

3. On-wafer Device Performance

The 0.25-mm HEMTs with 16% Al content exhibited maximum saturated current values in the range of 680-720 mA/mm with typical g_m's of 200 mS/mm. S-parameter measurements from devices with 0.45 µm gate length at a bias of V_{DS} = 10 V typically show f_T values in the range of 25-33 GHz and f_{MAX} values as high as 77 GHz, depending on the gate bias.

On-wafer RF power data measurements were performed at Cree at 10 GHz using a Focus Microwaves load-pull system with mechanical slide tuners and 10-GHz harmonic power filters. A power sweep for a 0.25-mm HEMT in deep Class-AB operation and at quiescent drain bias of V_{DS} = 30 V is plotted in Fig. 3. At these conditions, a peak PAE of 62% was achieved. The device had a peak output power level of 29.7 dBm (3.7 W/mm) with a simultaneous PAE of 60% and an associated gain of 11.6 dB. Higher values of output power could be achieved upon driving the device further into compression at the expense of PAE. This is one of the highest values of PAE reported to date for GaN at 10 GHz, which is attributed in part to the low off-state currents observed with these devices (<2% of $I_{DSS,max}$ at 60 V).

In order to demonstrate on-wafer RF power measurements of large periphery devices, 2-mm HEMTs from a wafer with 14% Al were measured. A 10 GHz power sweep for a 2-mm HEMT at a drain bias of V_{DS} = 35.4 V is shown in Fig 4. Under Class AB operation, this device exhibits a maximum total power of 8.3 watts CW (4.15 W/mm) with a PAE of 33 % and an associated gain of about 6.2 dB. This is a 200% improvement in power density over the 2 W/mm that was previously reported for a 2-mm gate periphery [2]. It is also a significantly high total power for a

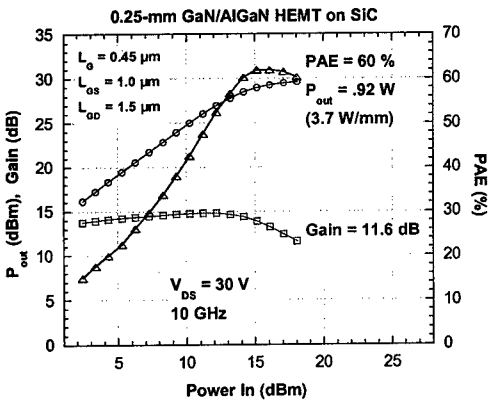

Fig. 3: On-wafer 10 GHz power sweep for a 0.25-mm GaN/AlGaN HEMT on SI4H-SiC in deep Class-AB operation, showing a record value for PAE at this frequency.

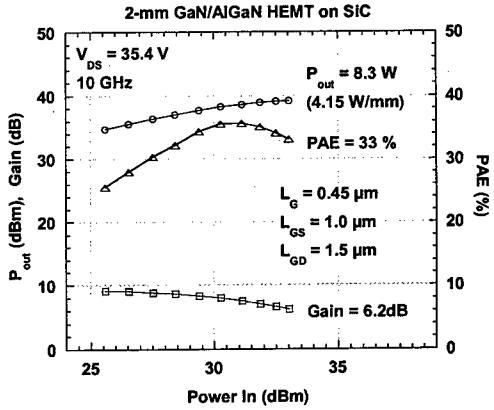

Fig. 4: On-wafer 10 GHz power sweep for a 2-mm GaN/AlGaN HEMT on SI4H-SiC, showing a record value for power density from a multi-mm RF device at this frequency. The device was biased in Class-AB operation.

single GaN/AlGaN device at 10 GHz. Although the reduced efficiency is due in part to the higher off-state current seen from the devices with 14% Al molar fraction, it is also due to the difficulty in efficient matching at the input of the larger devices, as reflected in the lower value of associated gain.

Typical dc output characteristics of a 3-mm-wide HEMT with 16% Al demonstrate that the dc characteristics scale well to multi-millimeter peripheries. As shown in Fig. 5, the peak current achieved at V_{GS} = +2 V is 2 A (667 mA/mm) with a V_{KNEE} near 5 V, and the maximum $g_{m,ext}$ is about 600 mS (200 mS/mm). Fig. 6 shows the characteristics of this same device on half the current scale and 10X the voltage scale to illustrate the off-state current at high drain bias. At 60 V, the leakage current is only 50 mA, or about 2.5% of I_{DSS}, showing that even the off-state characteristics scale to large devices. The low-voltage dc characteristics of 3-mm devices fabricated on another wafer with x=0.14 were very similar, but the off-state leakage at 60 V showed values between 100 and 200 mA over several devices.

Given the interest to move to higher total power, GaN/AlGaN-on-SiC HEMTs with total peripheries of 6-mm were fabricated on a wafer with ~17% Al molar fraction and characterized

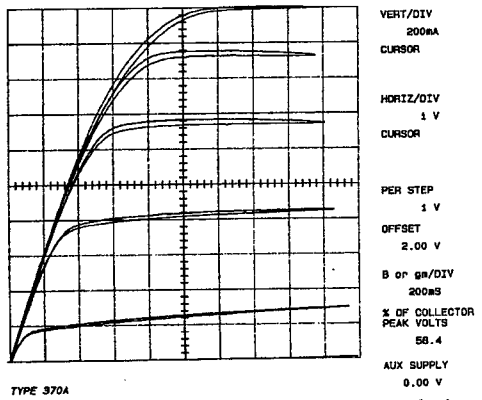

Fig. 5: Typical output characteristics of a 3-mm device (x=0.16) with L_G = 0.45 µm, L_{GS} = 1.0 µm, L_{GD} = 1.5 µm. The gate sweep begins at V_{GS} = +2 V with -1 V steps.

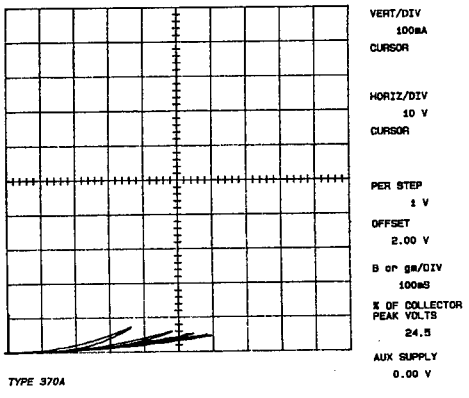

Fig. 6: Output characteristics of the device in Fig. 1 showing the off-state current at 60 V of about 50 mA, which is about 2.5% of I_{DSS}.

for the first time. As shown in Fig. 7, the on-wafer dc characteristics of a 6-mm (48x0.125-mm gate fingers) HEMT exhibits a peak current of about 5.2 A and a maximum g_m of about 1 S, or 166 mS/mm. The functional yield of 6-mm HEMTs on 1-3/8 inch SiC wafers was as high as 85%, which is an encouraging result in the first iteration of these large gate peripheries.

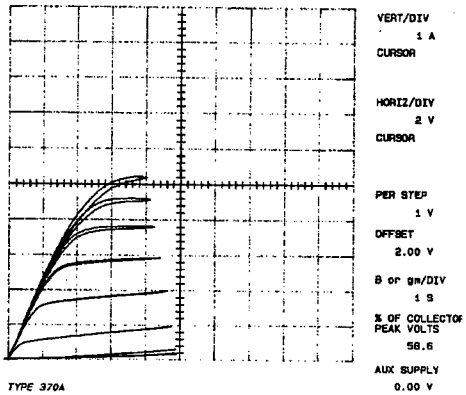

Fig. 7: Typical output characteristics of a 6-mm device (~17% Al) with L_G = 0.45 μm, L_{GS} = 1.0 μm, L_{GD} = 1.5 μm. The gate sweep begins at V_{GS} = +2 V with -1 V steps.

4. Conclusion

GaN/AlGaN HEMTs on silicon carbide substrates have demonstrated record power added efficiencies and high total power levels at 10 GHz. Considering the recent advances in III-Nitride growth and processing techniques for high-frequency power transistors, it is not surprising that GaN/AlGaN HEMTs on SiC substrates are beginning to the reach the extremely high power levels that have been predicted for this material system. Future efforts will be focused on RF characterization of large periphery devices, reliably increasing the total device peripheries up to 12-mm, and the fabrication of X-band devices with substrate source contact vias on 2-inch SI SiC wafers to eliminate parasitic wirebond inductance.

Acknowledgements

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Materials Science Forum Vols. 338-342 (2000) pp. 1647-1650

Characterization of AlGaN/GaN HEMT Devices Grown by MBE

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Keywords: Dislocation, Heterojunction, MBE, Microwave, TEM

Abstract

Ammonia-MBE growth techniques were developed to allow the production of AlGaN and GaN layers suitable for electronic applications on sapphire [0001] substrates. DC and RF characterization of AlGaN/GaN HEMT devices have been carried out over a temperature range from -40 °C to 200 °C. The devices characterized were two finger x 50 μm wide designs with measured gate lengths ranging from 1 μm to 3.5 μm. Hall and CV measurements indicate a 2DEG sheet charge density at the AlGaN/GaN heterojunction interface as high as 1.9×10^{13} /cm^2 and 1.5×10^{13} /cm^2 respectively. Low field mobilities in excess of 950 cm^2/V×s have been measured. Room temperature measurements for a device with a gate length of 1 μm and Vds set to 10 V exhibited a pinch off voltage of -5 volts. A maximum drain current of 946 mA/mm and a peak transconductance of 160 mS/mm were also measured. The off state drain to source breakdown voltage is 33 volts. Room temperature RF characterization with Vds=10 volts indicate intrinsic device f_T and f_{MAX} to be 15.6 GHz and 49.4 GHz respectively. At maximum power dissipation and chuck temperature, the channel temperature is estimated to be > 320 °C.

Introduction

Gallium Nitride and related alloys constitute a group of wide bandgap semiconductor material systems that have received increasing interest through out the research community in recent times[1,2]. This interest is primarily due to its extraordinary characteristics that lend itself to optoelectronic and electronic applications.For electronic device applications, GaN and its related alloys hold the promise of high voltage, high frequency and high temperature operation. In this work, the temperature dependence of the high frequency device performance will be studied as well as the impact on transport. It will be shown that not only is the perfection of the epitaxial growth of the nitrides a requirement for a successful device, but also the thermal issues associated with device design need to be well understood.

Device Fabrication

Starting substrates used for the MBE growth were 2 inch sapphire [0001]. Ammonia-MBE growth techniques were developed to allow the production of AlGaN and GaN layers suitable for electronic device applications[3]. The growth sequence starts with a 200Å AlN buffer layer deposited by magnetron sputter epitaxy (MSE) at 880 °C. Next a 2 μm C-doped GaN layer, followed by a 2000Å unintentionally doped GaN channel layer was grown by MBE at 910 °C[4]. Unintentionally doped GaN has been demonstrated to exhibit n-type background carrier conductivity. It is believed that the source of these carriers are due to native defects such as N vacancies[2]. The role of carbon doping in GaN is thought to act as a deep acceptor which

compensates or pins the Fermi level deep in the bandgap of the GaN film. This effect allows the fabrication of insulating GaN films with a resistivity $>1\times10^6$ Ω-cm, essential for the development of HEMT device structures. Finally a 130Å Al_xGaN_{1-x} barrier layer with x~0.3 were grown, completing the vertical structure for the HEMT growth. TEM analysis indicates a dislocation density of ~ 7×10^8 /cm^2.

Lateral isolation was achieved via mesa formation using a Chemically Assisted Ion Beam Etching (CAIBE) technique. The mesa was etched a total of 0.25 μm, placing the floor of the mesa well into the i-GaN and ensuring lateral isolation. Ohmic contacts were formed using a Ti/Al 300Å/800Å double period stack and patterned with a lift off technique. The patterned ohmics were annealed at 900 °C in N2 for 30 seconds. Schottky gate formation was accomplished using lift off with an initial 300Å sputtered Pt layer followed by an additional 1000Å/2000Å e-beam evaporated Pt/Au stack. A more complete description of the device fabrication is given elsewhere [5].

Results and Discussion

The design of the HFETs used in this work consisted of two gate fingers of varying length and 50 μm wide. These devices were set into microwave probable G-S-G pad structures and were complete with opens and shorts for extrinsic parasitic compensation. For CV characterization, careful attention has been given to remove the fringe component of the gate capacitance associated with short gate lengths. Open pad measurements indicated a capacitance of 2.2×10^{-18} F/μm^2 confirming the insulating nature of the underlying i-GaN layer. Ohmic contacts were characterized using

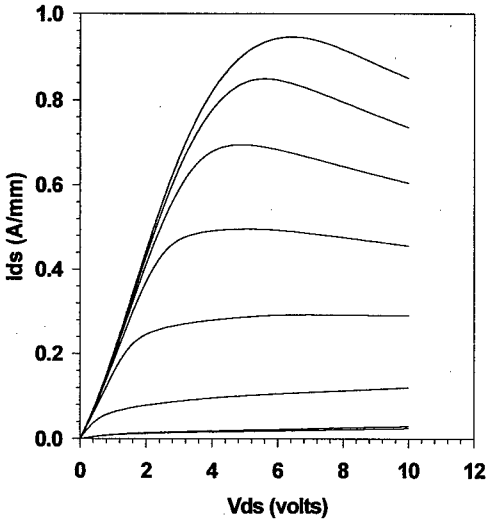

Fig.1: Measured Id Vd characteristics for a 2 gate 1 μm ×50 μm wide device. Vgs from +1V to -6 V step =-1V. From linear region, Rs=Rd~2 Ω-mm.

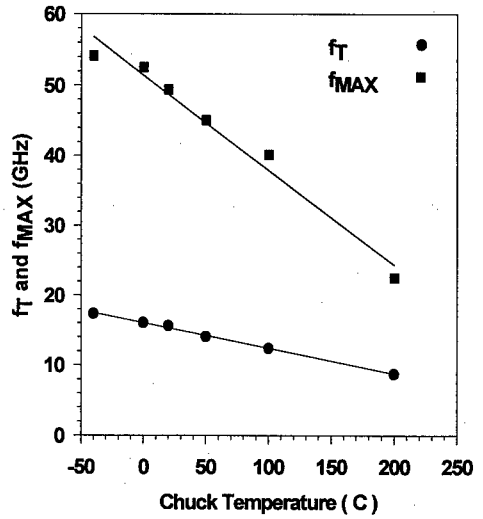

Fig. 2: Measured f_T and f_{MAX} over temperature for the device in fig.1. Vds is 10 volts.

a TLM structure. A channel sheet resistance of approximately 496 Ω/sq and contact resistances of 0.9 Ω-mm were measured using the TLM technique. From the sheet resistance measured, the 2DEG mobility density product is found to be 1.26×10^{16} $(V\times s)^{-1}$comparable to that seen elsewhere[1]. CV characterization of the channel using a 3.5 μm gate device at room temperature indicated a 2DEG charge density at Vgs=0 volts to be 1.15×10^{13} /cm^2. Figure 1 shows the current

voltage characteristics for a two gate finger 1 μm long ×50 μm wide device measured at room temperature. The source to drain and source to gate spacing are 2.5 μm and 0.5μm respectively. The off state breakdown voltage was 33 volts, the Vt was -5 volts with a maximum DC transconductance of 160 mS/mm and a maximum in the drain current of 946 mA/mm. The negative output conductance observed at high Vds is attributed to heating in the channel and subsequent reduction in 2DEG mobility/velocity. RF characterization was carried out from -40 °C to 200 °C and over a frequency range from 0.5 to 40 GHz with careful consideration to maintaining calibration at each temperature. The drain voltage was set to 10 volts and the gate swept from -4 volt to + 1 volt. At room temperature, an f_T of 15.6 GHz was measured and f_{MAX} was extrapolated to be 49.4 GHz from the unilateral gain. RF performance over temperature is shown in figure 2. From fig. 2, the

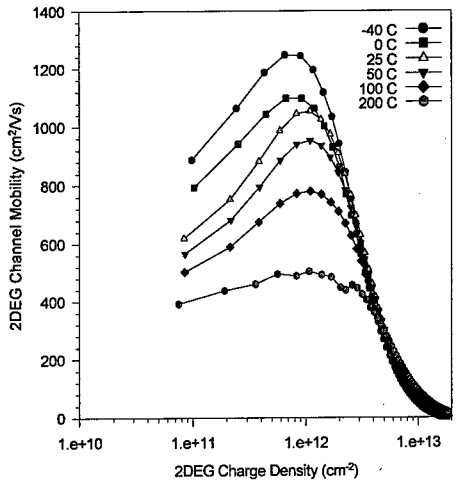

Fig.3:Channel field effect mobility vs. channel charge density measured over the temperature range of -40 °C to 200 °C.

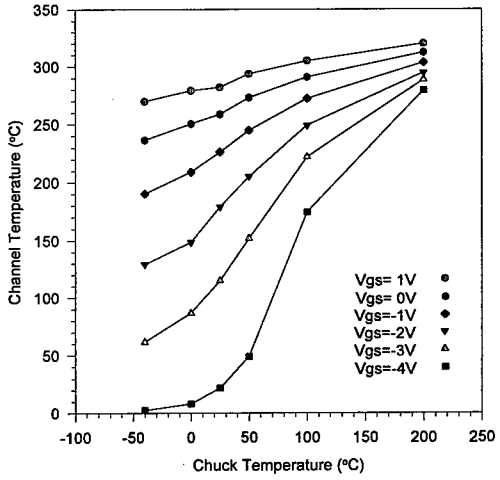

Fig.4: Estimated channel temperature vs. chuck temperature from the device shown in fig. 1.

slope associated with f_T and f_{MAX} are found to be -35.8 MHz/°C and -135.4 MHz/°C respectively. 2DEG channel mobility measurements over temperature using a 2 finger 3.5 μm ×50 μm wide device are depicted in figure 3. To minimize the change in charge density along the channel, a drain bias of 0.5 volts was used. Over the temperature range of -40 °C to 200 °C, the peak channel mobility is seen to decrease 1250 cm^2/Vs to 500 cm^2/Vs. The collapse of mobility with increasing 2DEG charge density is due to a number of factors including the effect of series source-drain resistance Rs and Rd as evidenced in fig.1 and surface scattering. As the 2DEG charge distribution is moved toward the AlGaN/GaN heterojunction interface by the large normal component of the electric field estimated to be ~2×10^6 V/cm, mobility reduction associated with surface interface roughness will also become important. To determine if the 2DEG channel carriers are velocity saturated, estimates of the channel velocity at the source side of the gate were made from Id data[6] measured over temperature with Vds=10 volts. The results indicate that at 25 °C, the carrier velocity, v in the channel is ~8×10^6 cm/s at peak f_T. From this result, the f_T for L=1μm is estimated to be 11.4 GHz using $f_T=v/2\pi L$ at 25 °C. This estimate of fT will set a lower limit since the carriers may increase in velocity as they transit the gate. Over temperature, the slope of the estimated f_T vs. T data is -39 MHz/ °C in good agreement with the measured slope of -35.8 MHz/°C.

This result along with the measured data indicates that the channel saturated velocity is probably somewhat higher at 1.1×10^7 cm/s. Using the mobility dependence in fig. 3, and Id at Vds=10 volts dependence on temperature, an estimate of the channel temperature can be made. The results are given in figure 4. For the 25 °C chuck temperature and a low current drive corresponding to Vgs=-4 V, the channel temperature is essentially the chuck temperature and from fig. 1, there is no evidence of self heating in the device characteristics. As Vgs increases to -3 V however there is a significant jump in channel temperature to 120 °C and a noticeable corresponding change in the device output conductance. At a gate voltage of +1 V, the maximum channel temperature is estimated to be 282 °C and a significant negative output conductance in fig.1 can be seen indicating self heating. At this channel temperature, the mobility of the carriers has been reduced to 240 cm^2/Vs from the room temperature value of 1053 cm^2/Vs.

Conclusions

Characterization of MBE grown HEMT devices has been carried out. Two gate finger devices with a 100 μm total width were used in the characterization. Channel 2DEG charge densities of 1.5×10^{13} $/cm^2$ were measured using CV techniques at microwave frequencies. Devices with gate lengths of 1 μm exhibited an f_T and f_{MAX} of 15.6 and 49.4 GHz respectively and a maximum drive current of 946 mA/mm. The breakdown voltage of this device was 33 volts when biased at pinch off. Mobility measurements carried out between -40 °C to 200 °C indicate a low field mobility reduction > 2.5. Negative differential output conductance seen in the Id-Vd characteristics appear to be due to self heating with estimated channel temperatures as high as 282 °C.

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A Comparative Study of n+p GaN/SiC Heterojunction and p-n 6H-SiC Homojunction Diodes

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Abstract: A comparative study between GaN/SiC heterojunction and 6H-SiC homojunction diodes has been performed to understand the physical properties of n-p GaN/SiC heterojunction interface. The 6H-SiC homojunction diodes presented typical I-V characteristics with satisfactory breakdown voltage (≅-800 V), however, the GaN/SiC heterojunction diodes showed an abnormal low forward turn-on voltage (≅1.8 V). The presence of a deep-level 1 eV below the p-SiC conduction band, is probably responsible for a tunneling- assisted current at low forward voltages, due to a high concentration of interface defects.

Introduction

The combination of electronic and physical properties of two wide band gap semiconductors such as GaN and SiC is very attractive for use in high power and high temperature semiconductor electronics. A first GaN/SiC high temperature heterojunction bipolar transistor (HBT) with high current gain was demonstrated a few years ago by Pankove *et al.* [1]. The understanding of the electrical characteristics of both GaN/SiC emitter-base heterojunction (HJ) diode and SiC base-collector homojunction diode are fundamental to the development of such device.

In this work we present a comparison between the physical properties of n-p GaN/SiC heterojunction and p-n 6H-SiC junction diodes, using current-voltage (I-V) and capacitance-voltage (C-V) measurements, as well as 300 K electroluminescence (EL) and photoluminescence (PL) experiments.

Experimental procedure

Epitaxial n-type GaN (0.5 μm, 3×10^{18} cm^{-3}) films were grown using metalorganic vapor deposition (MOCVD) on commercially available Si-face p-type 6H-SiC 3.5° off substrates (1×10^{18} cm^{-3}) [2]. Mesa-style 80 μm diameter HJ diodes were fabricated from these structures using reactive ion etching (RIE). Ti/Al and Al/Ti ohmic contacts were RF sputtered on the n-type GaN layer and p-type SiC substrate, respectively. The fabrication process was completed by rapid thermal annealing of the contacts. No passivation was used for the HJ diodes. A similar process was used to fabricate 100 μm diameter 6H-SiC p-n homojunctions diodes on n^--p^+ homoepitaxial layers (5 μm, 3.6×10^{15} cm^{-3}- 0.2 μm, 8.5×10^{18} cm^{-3}) grown on n^+ (2×10^{18} cm^{-3}) SiC substrates [2]. In these diodes a wet thermal oxidation was performed for mesa passivation. Unpatterned Nickel was E-beam evaporated onto the n^+ substrate, and for the contact on p-type side, a Al/Ti contact, similar to the one used for the HJ diodes, was used.

Results and discussion

Typical semi-logarithmic I-V characteristics obtained on the 6H-SiC p-n diode at 442 and 294 K are shown in Fig. 1. At forward bias, the ln(J) vs V plot exhibited two linear regions. At room

temperature, in the low voltage region from 1.75 to 2.25 V, the extracted ideality factor (n) equals 2.05 ±0.05, indicating that carrier recombination mechanism dominates the current transport. Above 2.3 V, and before the effect of the series resistance ($\cong 5\times10^{-3}$ $\Omega.cm^2$) becomes predominant, the ideality factor was estimated to be 1.5 ±0.10, far from the theoretical value of 1 expected for pure diffusion current. The extrapolated saturation current densities are 1×10^{-21} and 3×10^{-27} A/cm^2, for recombination and diffusion currents respectively, at 294 K. The temperature dependence of the saturation recombination current density revealed an activation energy (E_a) of about 1.40 eV as shown in the Arrhenius plot (Fig. 2). This result is close to half bandgap of 6H-SiC ($E_g \cong$ 3.0 eV), as predicted by the Shockley-Noyce-Sah's theory [3].

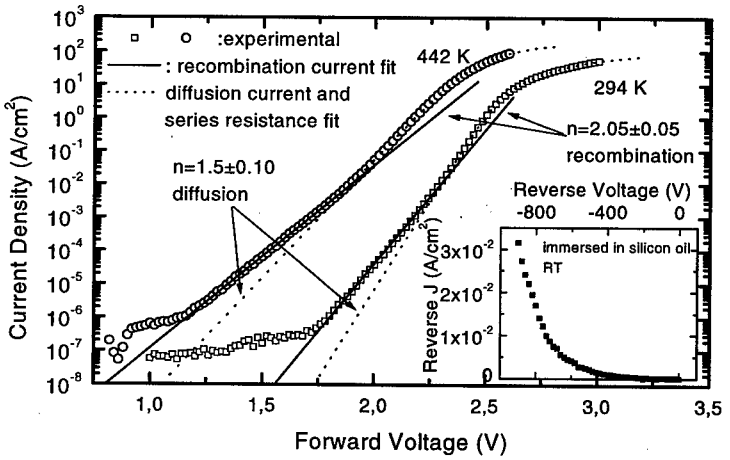

Fig. 1- Semi-logarithmic plot of forward J-V for a 100 µm diameter 6H-SiC p-n diode at 294 and 442K. The inset shows the linear reverse plot J-V at 294K.

The reverse characteristics vs. temperature were tested up to 100 V, and no significant variations in the reverse currents were detected (not shown). When immersed in silicon oil, the 6H-SiC p-n diodes exhibited good rectification characteristics for reverse voltages up to

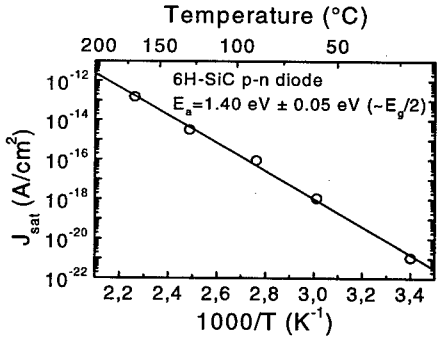

Fig. 2- Arrhenius plot of saturation recombination current density of a 6H-SiC p-n junction diode.

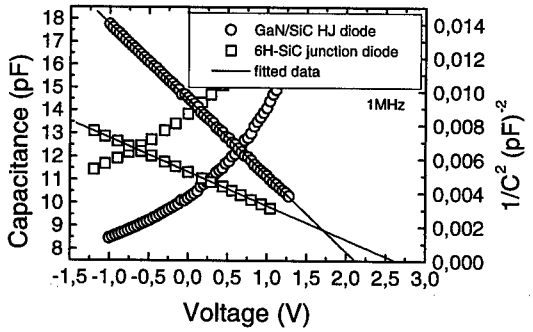

Fig. 3- C-V characteristics of a 6H-SiC p-n diode and GaN/6H-SiC n-p HJ diode.

800 V at room temperature as shown in the inset of Fig. 1.

The C-V characteristics of both types of diodes (HJ and homo) are shown in Fig. 3. The intercept $1/C^2$ with the voltage-axis gives the built-in potential (Φ_{bi}) around 2.1 (HJ) and 2.6 eV (homo), respectively. From the drift-diffusion theory [4], one would expect the value of Φ_{bi} for this HJ to be

about 2.8 eV, significantly higher than the one we have measured. Anomalous low Φ_{bi} values have been reported previously in GaN/SiC n-p HJ diodes [5].

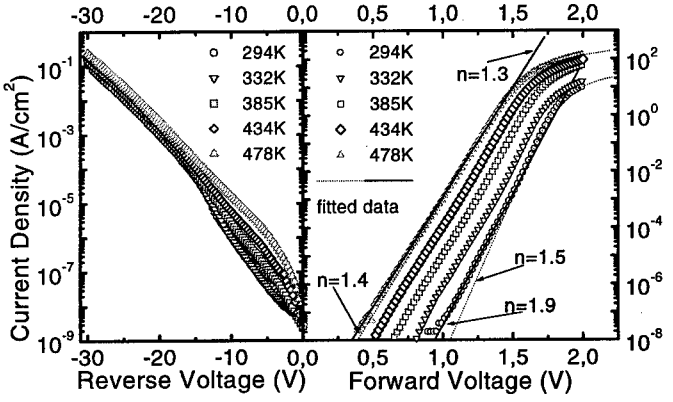

Fig. 4- Semi-logarithmic plot of forward and reverse J-V for an 80 μm diameter GaN/6H-SiC HJ diode at several temperatures.

Forward and reverse I-V characteristics at 478 K and room temperature are shown in Fig. 4 for the HJ diodes. The turn-on voltage at room temperature of about 1.8 V is in agreement with the measured Φ_{bi}. We have tried to draw activation energy plots of either reverse currents at fixed bias voltage or saturation current densities extrapolated from I-V forward characteristics. None of them yielded linear Arrhenius-like results as expected. The ideality factor changes with temperature and, also, a too high saturation current density of about 1×10^{-16} A/cm^2 is observed at room temperature. The change in ideality factor with temperature is not well understood at this time but suggests that mechanisms other than thermal recombination-generation are involved.

Carrier generation mechanisms induced by a high density of morphological defects (scratch, micropipe, misfit dislocations, stacking fault) and also carrier tunneling are expected to be the dominant leakage mechanisms for the HJ diodes samples presently available. These diodes presented high leakage currents of 1 mA/cm^2 at -20 V with catastrophic reverse failures between -40 and –50 V.

The 6H-SiC p-n junction diodes showed typical blue light emission, when forward biased, as shown in Fig. 5. The electroluminescence spectrum is dominated by the free exciton recombination peak at 425 nm (2.9 eV) as previously reported [6,7]. Donor-acceptor recombination (N and Al) as well as deep acceptor centers are probably involved in the yellow-green emission. The room temperature PL emission of the 6H-SiC p-n homojunction is dominated by the near band edge recombination peak at ~3.0 eV.

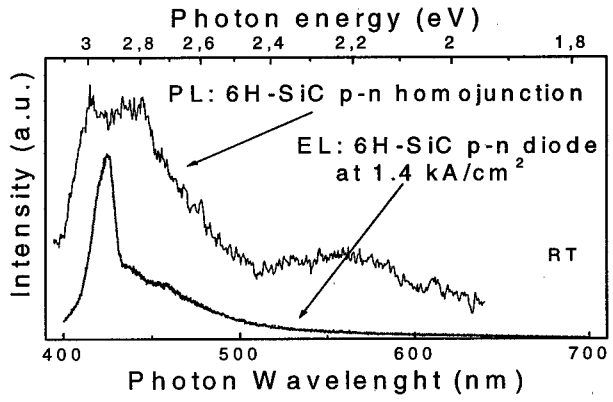

Fig. 5 – Comparison between the EL spectrum of the p-n 6H-SiC diode and the PL spectrum from the same p-n homojunction, excited with a HeCd laser at room temperature.

The HJ diodes presented an orange-red light emission with maximum at 1.88 eV in the forward biased region as shown in Fig. 6. In the same figure, the PL spectra from the HJ and p-type 6H-SiC substrate shows at room temperature a broad emission band at 1.98 eV when excited by 390 nm

light. This result shows that the p-SiC is responsible for the EL emission. At 10 K the PL of p-type 6H-SiC is dominated by near band edge emission (DAP N-Al). This is strongly quenched above 60 K while a band at 1.8 eV increases and progressively shifts to the room temperature value of 1.98 eV. Preliminary results of the PL temperature dependence suggest that a level about 1 eV below the conduction band acts as an effective electron trap, leading to the PL and EL emissions. Since Vanadium is a usual SiC contaminator it is possible that the related deep levels (630-780 meV) are involved in the radiative emission [8]. A tunneling assisted current to this deep level [9] in forward bias regime below the turn-on voltage is improbable, since the depletion layer for this range of voltages is large enough (590 to 190 Å) to prevent such tunneling, unless the presence of some interface defects can locally reduce the depletion layer or create field enhancement by sharp edge effects.

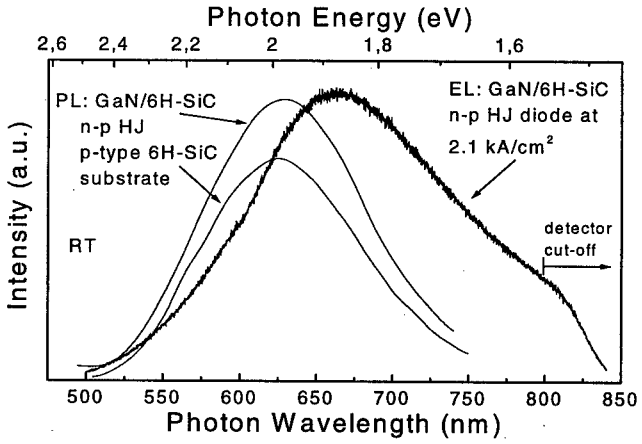

Fig. 6- Comparison between the EL spectrum of the GaN/6H-SiC HJ diode and the PL spectrum from the same HJ and p-type substrate, excited with a Xe lamp (390 nm) at room temperature.

Conclusion

We found that the low turn-on voltage in the GaN/SiC HJ diodes is probably related to the presence of a deep-level in the p-SiC substrate. Further work will be necessary to well understand the tunneling-assisted current mechanism at low forward voltages, and also to improve the GaN/SiC interface growth.

Acknowledgements

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Electrical Characteristics of 6H-SiC/GaN Isotype n-n Heterojunctions

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Keywords: Electrical Properties, Equilibrium Energy-Band Diagram, Hydride Vapor Phase Epitaxy, Interface States, Isotype n-n Heterojunction

Abstract Electrical characteristics of 6H-SiC/GaN isotype n-n heterojunctions were investigated. The forward current-voltage (IV) characteristics were measured in the temperature range 200–600 K. Conventional capacitance-voltage (CV) measurements were performed at different frequencies (1 MHz, 10 kHz and 1 kHz). According to Anderson's theory the discontinuities in conduction-band and valence-band edges were calculated to be 0.6 eV and 1.0 eV, respectively. The density of interface states was found to be $7x10^{12}$ cm^{-2}.

Introduction Vertical current flow geometry is preferred for high-power semiconductor devices. A heteroepitaxial growth of GaN directly on SiC without the employment of an intermediate AlN buffer is important for the development of vertical GaN-based devices. Moreover, the direct growth of GaN layers on SiC should give the perspective to develop a new area of SiC-based devices. The GaN/SiC heterojunction bipolar transistor has been demonstrated [1, 2, 3]. The investigation of electrical characteristics of GaN/6H-SiC np anisotype heterojunction has been published [4, 5]. In this paper, we report on the investigation of electrical characteristics of 6H-SiC/GaN isotype n-n heterojunction.

Experiment GaN epitaxial layers of n-type conductivity were grown using hydride vapor phase epitaxy (HVPE) growth machine equipped with resistively heated furnace [6]. In a horizontal open-flow reactor, HCl was reacted with liquid Ga metal to form GaCl gas, which was transported to the growth zone of the reactor and reacted with NH_3 resulting in GaN deposition on SiC substrates. Argon was used as an ambient gas. GaN films were grown on the Si face of 6H-SiC (0001) on-axis commercial wafers. The growth temperature was kept between 950 and 1050°C. The GaN growth rate was controlled in the range from 0.05 to 0.6 μm/min. The GaN layer was deposited directly on the SiC substrate without any buffer layer. The substrates were n-type 6H-SiC wafers with a doping level of $2x10^{18}$ cm^{-3}. The thickness of n-GaN layers ranged from 0.5 to 1.5 microns. Crystal quality of the n-GaN layer was studied by X-ray diffraction. The full width at half maximum of the double crystal X-ray rocking curves for the (0002) reflection ranged from 100 to 180 arc sec indicating high crystal quality of the grown material. Using CV measurements of Schottky barrier diodes, the uncompensated impurity concentration in the epitaxial layer was found to be $2x10^{18}$ cm^{-3}. To investigate the electrical characteristics of the n-n heterojunctions, mesa-structures of 150 microns in diameter were fabricated by reactive ion etching [7]. Ti/Ni ohmic contact was formed by vacuum thermal evaporation onto the n-GaN layer and In was used as ohmic contact to substrate. The position of the n-n heterojunction was found using electron beam induced current (EBIC) measurements. The EBIC measurements showed that n-n heterojunction is on the GaN/SiC interface. The forward IV characteristics of the mesa-structures were measured in the

temperature range 200 – 600 K. Conventional CV measurements were performed at different frequencies (1 MHz, 10 kHz and 1 kHz).

Results Before describing the experimental results, let us consider the equilibrium energy-band diagram of a 6H-SiC/GaN isotype n-n heterojunction. The equilibrium energy-band profile for 6H-SiC/GaN isotype n-n heterojunction constructed according to Anderson's theory [8] is shown in Fig.1. In this diagram subscripts '1' and '2' refer to 6H-SiC and GaN, respectively; χ is the electron affinity. The value of χ was found from CV measurements to be about 3.5 eV for 6H-SiC and 4.1 eV for GaN [9]; V_d is the built-in potential; x is the width of the depletion region; ΔE_C and ΔE_V are the discontinuities in conduction-band and valence-band edges, respectively. The basic characteristics of the equilibrium energy-band diagram were calculated according to Anderson's theory. The built-in potential was found to be 0.56 eV. The discontinuities in conduction-band and valence-band edges were found to be 0.6 eV and 1.0 eV, respectively.

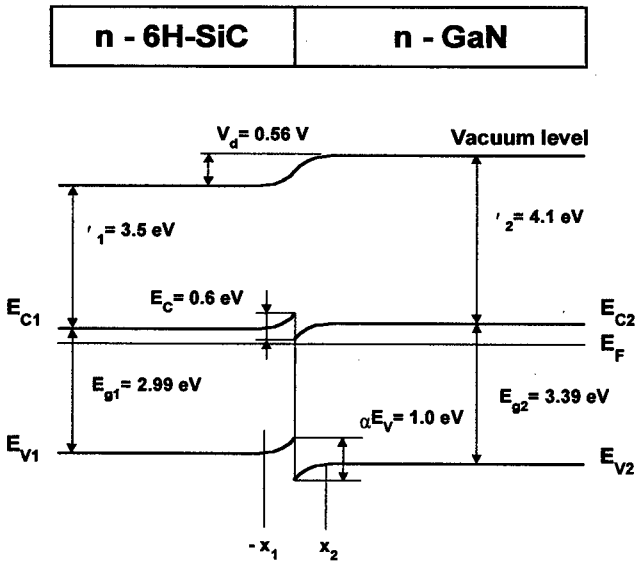

Fig.1. Equilibrium energy-band diagram of a 6H-SiC/GaN isotype n-n heterojunction.

The electronic properties of the mesa-structures exhibited typical diode behavior (Fig.2). A rectifying n-n heterojunction conducts in a forward bias condition when the SiC side is made negative with respect to the GaN. The turn-on voltage of the forward IV characteristic is about 0.4 V at current of 1 mA. The forward IV characteristics were measured in the temperature range 200 – 600 K (Fig.3). The forward current varies exponentially with applied voltage and can be expressed by equation: $I = I_0 \exp(qV_a/nkT)$, where I_0 is saturation current, n is non-ideality factor. The non-ideality factor was found to be close to 1.0 at temperature range of 400 - 600 K. In this temperature range we can use emission model to describe current transport. In this case, the value of barrier height can be determined from temperature dependence of saturation current. The saturation current was found to vary exponentially with temperature. The activation energy of saturation current was found to be 0.51 eV (Fig.4).

Conventional CV measurements were performed using three different test signal frequencies (1 MHz, 10 kHz and 1 kHz). The CV characteristics were linear when plotted in C^{-2} versus V

co-ordinates (Fig.5). The cut-off voltage of the CV characteristics was found to be 0.9 V that gives the value of barrier height of 0.94 eV. This value is higher than the built-in potential determined theoretically (0.56 eV) using Anderson's theory and experimentally (0.51 eV) from IV measurements. It seems likely that a high density of interface states that not surprise because of taking place considerable difference between the lattice constants of two semiconductors forming the heterojunction. This difference is about 3.4% for GaN and 6H-SiC [10]. Estimation of the density of interface states from CV characteristics according to the Anderson's theory gave the value of $7x10^{12}$ cm^{-2}.

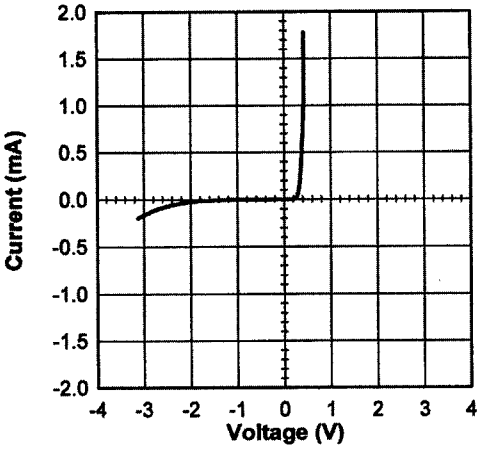

Fig.2. IV characteristic of a 6H-SiC/GaN n-n heterojunction at room temperature.

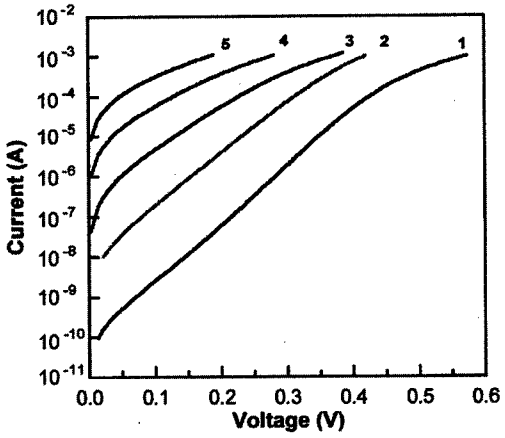

Fig.3. Forward IV characteristics of a 6H-SiC/GaN n-n heterojunction: (1) 200 K, n=1.73; (2) 300 K, n=1.29; (3) 400 K, n=1.17; (4) 500 K, n=1.14; (5) 600 K, n=1.14; where n is non-ideality factor.

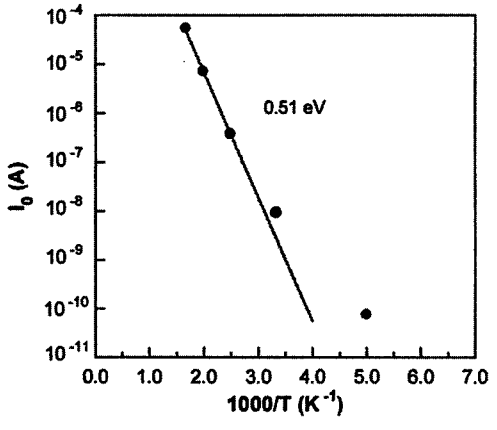

Fig.4. The temperature dependence of saturation current.

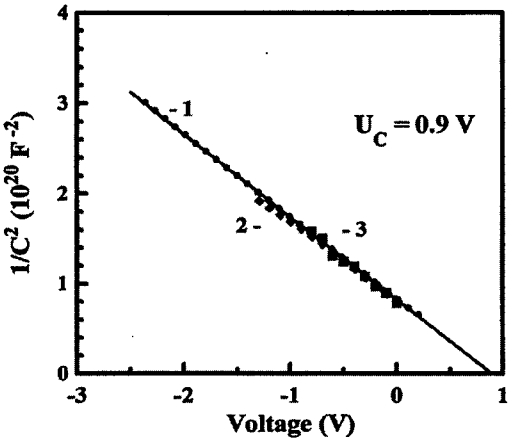

Fig.5. CV characteristics of a 6H-SiC/GaN isotype n-n heterojunction: (1) 1 MHz, (2) 10 kHz, (3) 1 kHz.

Conclusions High crystal quality n-type GaN have been grown on n-type 6H-SiC commercial wafers by HVPE. The forward IV characteristics of a 6H-SiC/GaN isotype n-n heterojunction have been investigated in the temperature range of 200-600 K. The turn-on voltage of a forward IV characteristic is about 0.4 V at room temperature. In the temperature range of 400-600 K, the current transport can be described by emission model. Using CV measurements, the density of interface states has been estimated to be $7x10^{12}$ cm^{-2}. According to Anderson's theory, the equilibrium energy-band diagram has been calculated. The built-in potential of a 6H-SiC/GaN isotype n-n heterojunction has been found to be 0.56 eV. The discontinuities in conduction-band and valence-band edges were found to be 0.6 eV and 1.0 eV, respectively.

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Author Index

M

N

Keyword Index