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14. ABSTRACT

This report summarizes a one year program to investigate issues related to fabrication and performance of III-V nitride static induction power transistors. To understand vertical conduction mechanisms in this device a nearly ideal, vertical Schottky barrier diode was fabricated and analyzed. By applying the diffusion theory of Schottky barriers, a vertical mobility of ~950 cm2/Vs was measured which, when compared to a lateral mobility in the same film of 160 cm2/Vs, indicates a minimal role of dislocations in scattering electrons in the vertical direction. In an effort to develop the required processing for a GaN static induction transistor, high density plasma etching was optimized for fabricating the recessed gate structure. The effect of such processing on ohmic contact quality was examined as a first step to understanding such surfaces. It was found that even etches with very low ion energies degraded the contacts and that the damage could be recovered with a short (<30sec) rapid thermal anneal at 700C.

15. SUBJECT TERMS
gallium nitride, static induction transistor, vertical mobility, vertical Schottky diode

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FINAL TECHNICAL REPORT

Gallium Nitride Static Induction Power Transistors

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1. Objectives of the program

This was a one year program to investigate issues related to the fabrication and performance of III-V nitride static induction transistors (SITs) whose structure is schematically illustrated in Figure 1. SITs are short channel FET structures which are suitable for high power, high frequency and high temperature operation. GaN has particularly favorable properties for SIT operation. Modeling efforts show that output power for such devices can be as high as 10.75 W/mm at 2GHz operating frequency, with a power added efficiency of 73.8%. These results also show a cut-off frequency of 24.8 GHz and an f_T of 75.2 GHz. For detailed modeling results see Appendix A.

The program objectives were the following:

- Since the static induction transistor is a vertical device, as opposed to conventional field effect transistors, the first objective of the program is to investigate the mechanism of vertical transport in gallium nitride and determine the role of dislocations in this type of transport.
- Investigate the fabrication and characterization of vertical Schottky barriers since the majority of the reported literature has concentrated on lateral Schottky barriers.
- Since this device requires recessed gates it is important to address issues related to plasma etching of gallium nitride. This program investigates the application of high density plasma etching to gallium nitride for these purposes.
- As a starting point for contacting plasma processed surfaces, investigate the properties of ohmic contacts to n-type gallium nitride surfaces subjected to high density plasma etching.

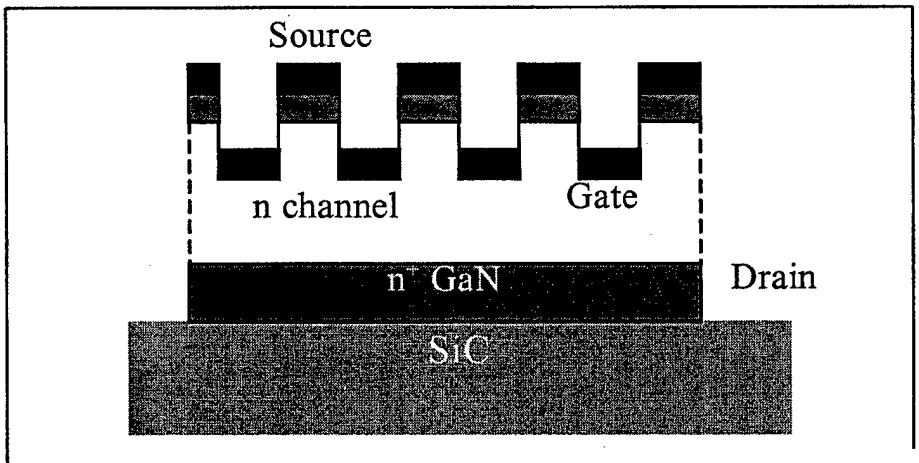

Figure 1. Schematic cross-section of gallium nitride static induction transistor.

2. Experimental results

The various objectives of the program were addressed and the results are discussed in the following sections.

2.1 Formation of vertical Schottky barriers & investigation of vertical transport

Schottky barriers in gallium nitride have primarily been investigated in the planar form whereby both the ohmic contacts as well as the Schottky barriers are deposited on the front surface of the wafer. In the current project we utilize reactive ion etching for the formation of mesas of 300μm diameter to investigate two types of vertical Schottky barrier devices which are shown schematically in Figure 2. Both devices contain the same n^- GaN layer, however, in the first one we have included an n^+ GaN layer ($5x10^{18}$ cm^{-3}) for the formation of a better ohmic contact. Circular mesas approximately 3μm deep were defined by reactive ion etching using Cl_2 gas. Ohmic contacts were defined on the bottom of the mesa by electron beam deposition of 200/1000/200/2500Å Ti/Al/Ni/Au metal multilayers. The ohmic contacts were rapid thermal annealed at 750°C for 60 sec, prior to deposition of the Schottky contacts. Schottky contacts were formed at the top of the mesa by patterning 200 μm dots by photolithography and depositing a 200/1000/3000Å Ni/Pt/Au metal multilayer stack by electron beam evaporation. Some of the diodes were mounted on transistor headers and Au wires were bonded to the contacts by thermosonic bonding. A top view photograph of a fully fabricated device is shown in Figure 3.

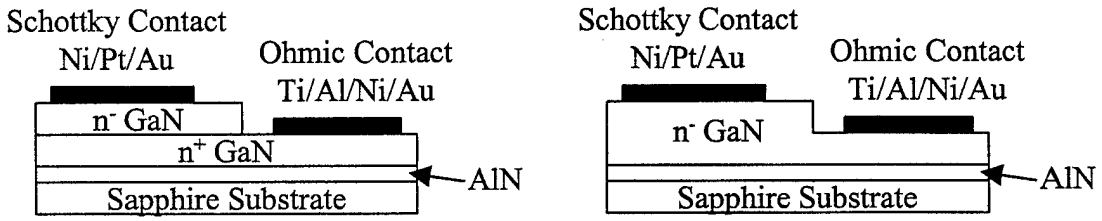

Figure 2. Schematic diagram of vertical Schottky barrier structures investigated.

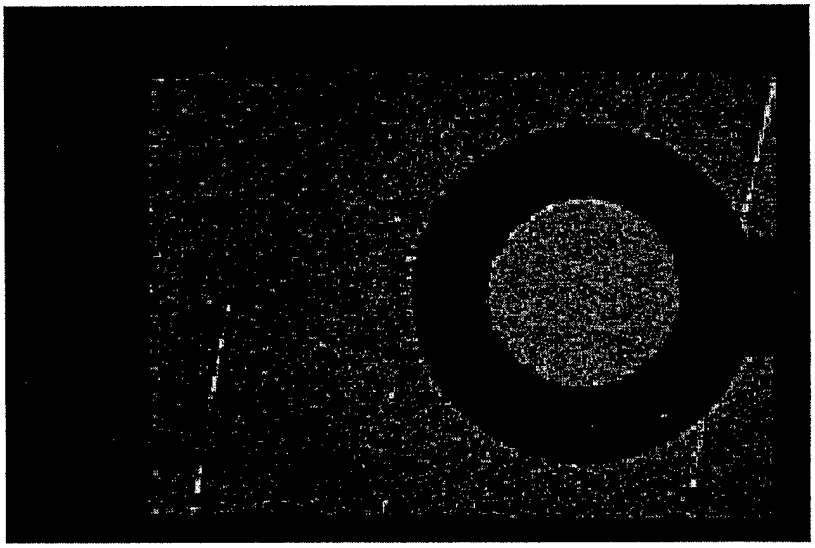

Figure 3. Optical micrograph showing top view of fabricated vertical Schottky barrier diode.

These Schottky barriers were evaluated by studying their I-V characteristics and C-V characteristics and the results are show in Figures 4 and 5.

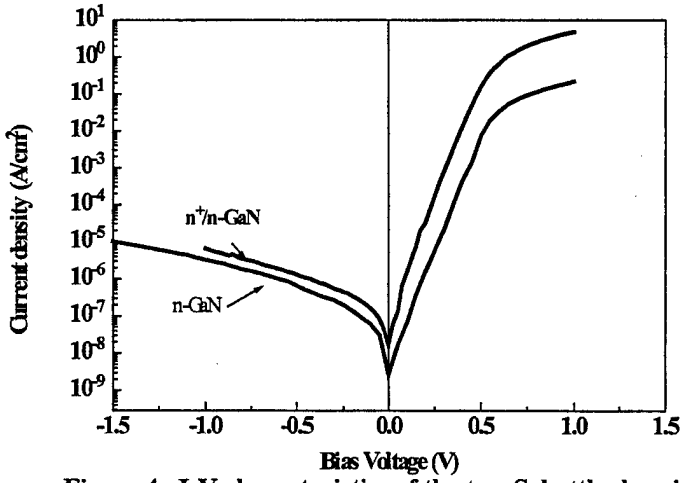

Figure 4. I-V characteristics of the two Schottky barrier devices described in Figure 2.

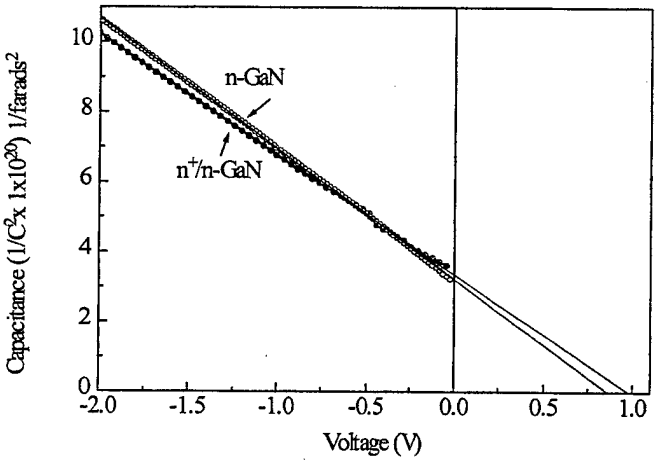

Figure 5. C-V characteristics of the two devices described in Figure 2.

From the measurements described in Figure 4, we found that the diodes are practically ideal (ideality factor = 1.1-1.2) and the reverse saturation current ranges from 10^{-9} to 10^{-8} A/cm^2. From the C-V measurements described in Figure 5, we obtained the doping concentration in the two devices, which ranges 8-9x10^{16} cm^{-3}, and the Schottky barrier height was measured to be between 0.95 eV and 1.0 eV. This part of the work has demonstrated our ability to form ideal vertical Schottky barriers, we do however realize that for high temperature and high power applications both the fabrication of the ohmic

contacts as well as the Schottky barriers must be based on refractory metals such as platinum for the Schottky barriers and tungsten for the ohmic contacts.

The traditional way of studying the transport mechanism in a semiconductor is through the study of conductivity and the Hall effect using four probe measurements. Indeed in the second structure described in Figure 2, which does not involve an n^+ layer in the bottom of the device, we were able to perform such measurements and found the electron concentration in the films to be 1.4×10^{17} cm^{-3} (approximately the same as the C-V measurements from the Schottky barriers) and the electron mobility to be 160 cm^2/Vs.

In order to investigate the electron mobility for vertical transport we considered the diffusion theory of Schottky barriers which expresses the relation between the reverse saturation current as a function of barrier height and the diffusion coefficient of electrons in the space charge region. In this model the reverse saturation current density is given by the following relation:

$$J_0 = \left\{ qN_c\mu_v \left[\frac{2qV_{bi}N_d}{\varepsilon_s} \right]^{1/2} \right\} \exp\left(\frac{-q\phi}{kT} \right)$$

where N_c is the effective density of states in the conduction band, μ_v is the electron mobility in the vertical direction, V_{bi} is the built-in voltage, N_d is the doping concentration, ε_s is the dielectric constant, and ϕ is the barrier height. Using this relationship we obtain a vertical mobility μ_v=932 cm^2/V s for the n^+/n^- GaN and μ_v=949 cm^2/V s for the n^- GaN film. In the calculation of vertical mobility, we have assumed that the active area is equal to the geometric area of the device. However a reduction of the active area (up to one-third for a dislocation density of 5×10^9 cm^{-2} and doping concentration of 1×10^{17} cm^{-3}) is expected due to depletion around each charged dislocation. Specifically, considering the active area to be two-thirds the geometric area, increases the doping concentration and reverse saturation current density to 1.9×10^{17} cm^{-3} and 1.62×10^{-9} A/cm^2, respectively for the n^+/n^- device. This leads to a vertical mobility of 1070 cm^2/V s for the same device (in good agreement with theoretical calculations). For details and references see Appendix B.

2.2 Development of high density plasma etching and contacts to processed surfaces.

Since this device requires recessed gates it is important to address issues related to plasma etching of gallium nitride. Further, developmental devices grown on sapphire will require drain contact access etches. To address these needs the device processing efforts focussed on establishing appropriate etch rates for the gate recess and, for same-side drain contacts, for drain access. We employed chlorine chemistry in an inductively coupled high density plasma etching reactor. We established a set of etching conditions that even at low rf bias powers (0-50W) provided etch rates in the 2000Å/min range. These conditions included relatively low ICP powers (300 W) to maintain the high

density discharge at operating pressures of ~3-4 mTorr. Gas flow rates of approximately 10 sccm were employed.

As the vertical mobility results indicate, there is a need for improved ohmic contacts to n-GaN, meeting or exceeding the current best contacts. Furthermore, there is a need for thermally stable barrier contacts in the SIT device. To address this issue a considerable fraction of the effort concentrated on characterization of the damage resulting from these somewhat "gentle" etches in the form of degradation of ohmic contacts (Ti/Al/Au) to n-GaN surfaces. What was observed was that even at these low biases, etches resulted in considerable damage to the surfaces as measured by ohmic contact resistivity compared to the control surface. This damage led to considerably worse degradation in more lightly doped n-GaN that will be expected in electronic devices such as the SIT. In Figure 6, we see the contact resistivity as a function of rf bias during high density plasma etching. Clearly the degradation effect is larger in the $3x10^{17}$ cm^{-3} n-GaN sample than the $3x10^{18}$ cm^{-3} sample with contact resistivity increasing by a factor of 50 compared to a factor of 2 in the higher conductivity sample. These results are for as-deposited contacts without annealing.

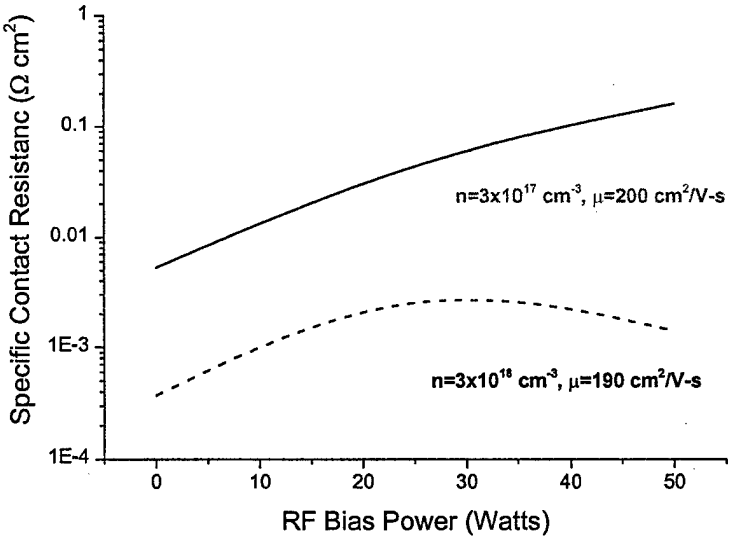

Figure 6. Specific contact resistance vs. rf bias power during ICP etching in a Cl_2 discharge.

It is well known, however, that annealing is required to achieve improved contact resistivities. Therefore, we subjected each of these surfaces, including the control surface, to consecutive rapid thermal anneals at 700°C to evaluate the response of the contact to annealing as a function of time. The results of this study are presented in Figure 7. As can be seen, the contact properties rapidly improve after just a 20 sec anneal and often reach their best values after 30 secs of annealing time. Continued anneals out to 20 minutes in cumulative duration showed no further improvement. In this portion of the project, the best contact resisitvity measured was approximately 10^{-4} Ω cm^2 range, two orders of magnitude higher than that required as per the vertical mobility results (ρ_c=10^{-6} to 10^{-8} Ωcm^2). We are currently looking at multilayer contacts to improve that

number as well as additional in-situ and ex-situ treatments of etched surfaces to address this deficiency.

These results are all for simple contact systems. Studies are currently underway on more sophisticated metal multilayer systems for ohmic contacts and barrier contacts, and contact schemes utilizing refractory metals for high temperature applications are planned.

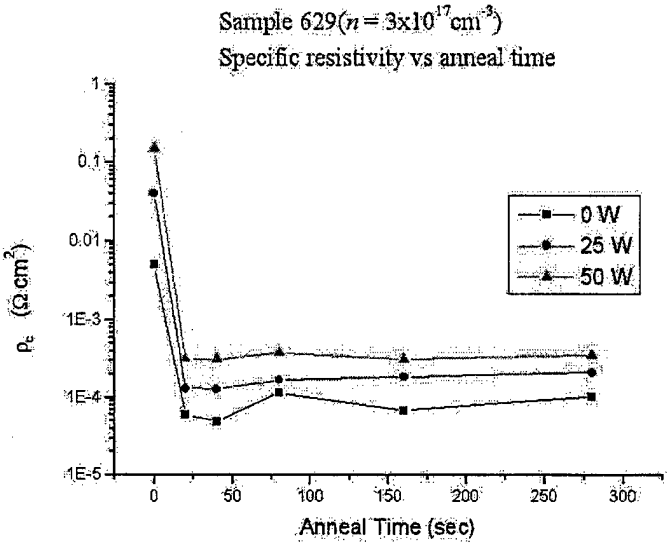

Figure 7. Specific contact resistivity vs. anneal time for damaged and control samples.

Appendix A. Investigation of vertical transport in n-GaN films grown by molecular beam epitaxy using Schottky barrier diodes.

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MODELING OF A GaN BASED STATIC INDUCTION TRANSISTOR

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ABSTRACT

Static induction transistors (SITs) are short channel FET structures which are suitable for high power, high frequency and high temperature applications. GaN has particularly favorable properties for SIT operation. However, such a device has not yet been fabricated. In this paper we report simulation studies on GaN static induction transistors over a range of device structures and operating conditions. The transistor was modeled with coupled drift-diffusion and heat-flow equations. We found that the performance of the device depends sensitively on the thermal boundary conditions, as self-heating effects limit the maximum voltage swing.

INTRODUCTION

GaN is a wide-bandgap semiconductor (Eg=3.4 eV), and therefore has a high breakdown field [1] and low thermal generation rate. These properties combined with good thermal conductivity and stability make GaN an attractive material for high power/ high temperature and radiation harsh environment electronic devices. Monte Carlo simulations predict a peak electron velocity of 3.2×10^7 cm/s and a saturation electron velocity of 2.5×10^7 cm/s [2]. This makes possible high frequency operation of GaN devices.

SIT's are short channel FET structures in which the current, flowing vertically between source and drain, is controlled by the height of an electrostatically induced potential barrier under the source [3]. A cross-sectional diagram of the SIT is shown in Figure 1.

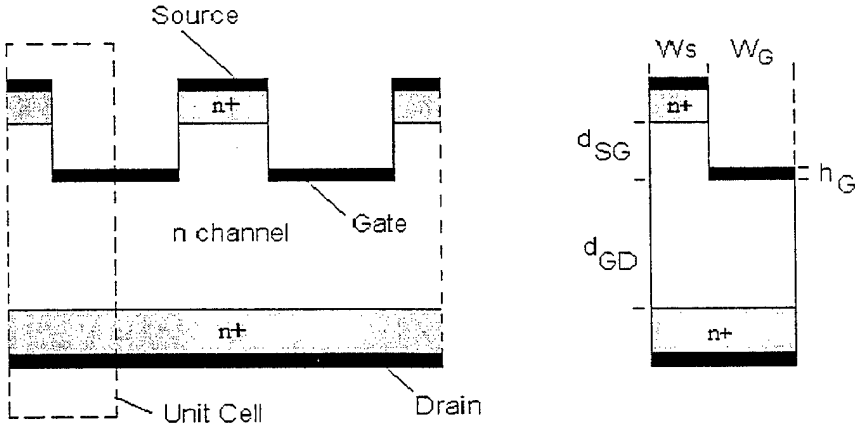


Figure 1. Cross-section of static induction transistor (SIT) structure considered in this work and the unit cell simulated with critical dimensions labeled.

Electrons are emitted from the source, which is at ground potential, and are accelerated to the drain, which is biased at positive potential, where they are collected [4]. A very thin heavily doped layer is deposited next to the drain and source contacts in order to form ohmic contacts. A grid structure is located in the space between the source and drain electrodes so the charged carriers can be externally modulated. The RF gain of the device is determined by the efficiency

with which the modulation is affected. The grid structure is generally fabricated using pn or Schottky junctions.

A range of field effect transistors including MESFET, MISFET, inverted channel AlGaN/GaN and MODFET have been developed with potential applications for high power/ high temperature electronics [2,5-8]. To our knowledge, the highest cut-off frequency reported for GaN-based FET's is 52 GHz [9], and the maximum frequency of oscillations is over 97 GHz [10]. Significant results regarding the power output of GaN-based FET's have been reported by several groups [9, 11]. Wu reported an output power of 3 W/mm at 18 GHz, with a power added efficiency (PAE) of 19% for a 0.25 μm gate AlGaN/GaN MODFET [9]. In comparison, our SIT simulation results show a cut-off frequency f_T of 24.8 GHz, a maximum frequency of oscillations f_{max} of 75.2 GHz. Operated under class B, the output power decreases from 10.75 W/mm to 1.95 W/mm as the operating frequency changes from 2 GHz to 40 GHz. Correspondingly, the PAE changes from 73.8% to 9.1 %.

THEORY

Basic simulation equations and physical models

We employed a commercially available 2D device simulator (ATLAS [12]) which was modified appropriately for GaN, based on experimental observations and theoretical calculations. The transistor was modeled with coupled drift-diffusion and heat-flow equations. The effect of lattice temperature on the performance of the device was taken into account by including the thermoelectric factor in current density equations (1,2) and by adding the heat-flow equation (3).

$$J_n(x,y) = n(x,y)q\mu_n E(x,y) + qD_n\nabla n(x,y) - q\mu_n n(x,y)P_n(x,y)\nabla T(x,y) \tag{1}$$

$$J_p(x,y) = p(x,y)q\mu_p E(x,y) - qD_p\nabla p(x,y) - q\mu_p p(x,y)P_p(x,y)\nabla T(x,t) \tag{2}$$

$$C\frac{\partial T(x,y)}{\partial t} = \nabla(\kappa\nabla T(x,y)) + H(x,y) \tag{3}$$

where T is the lattice temperature, and P_n and P_p are thermoelectric power coefficients for electrons and holes, respectively, C is the heat capacitance per volume (1.97 J/K cm^3 [13]), κ is the thermal conductivity (1.3 W/cm K [14]) and H is the heat generation based on Joule effect.

The models used in the simulation are based on those from Si and GaAs, but have been modified to fit the available data for GaN. The temperature dependence of bandgap energy:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} \tag{4}$$

with $E_g(0)$=3.5 eV, α=9.39x10^{-4} eV/K, and β=772 K, based on optical absorption measurements [15]. The electron (hole) low-field mobility as a function of the impurity concentration (N) and temperature T is given by [12]:

$$\mu(N,T) = \mu_1 + \frac{\mu_2(\frac{T}{300})^{\beta} - \mu_1}{1+(\frac{T}{300})^{\gamma}(\frac{N}{N_{crit}})^{\delta}} \tag{5}$$

where μ_1, μ_2, β, γ, δ and N_{crit} were determined by fitting the values available from the literature for both electrons and holes [2,16-19]. For electrons: μ_1=15 cm^2/Vs, μ_2=1800 cm^2/Vs, β= -3.04,

γ= -2.55, δ= 0.66, N_{crit}= 8x10^{16} cm^{-3}. For holes: μ_1=0.14 cm^2/Vs, μ_2=880 cm^2/Vs, β= -1.5, γ=0, δ= 0.67, N_{crit}= 5.5x10^{14} cm^{-3}. A comparison between experimental and predicted values (from Monte Carlo simulation) of low field electron mobility versus doping level and the model used in our simulations is presented in Figure 2a. Figure 2b presents a similar comparison for the electron low field mobility versus temperature [19]. In our simulations, we employ a channel doping of 5x10^{16} cm^{-3}. The low field electron mobility reported for such a doping level is 900 cm^2/Vs [5,20]. However this mobility was measured laterally. There is evidence that the lateral mobility is reduced due to the scattering by charged dislocations, while the vertical mobility is significantly higher because the electrons are repelled from the dislocation lines by band bending due to the negative charge on the dislocations [21]. In our device, which is a vertical one, we employ a room temperature electron mobility of 1050 cm^2/Vs, which we believe is a reasonable value.

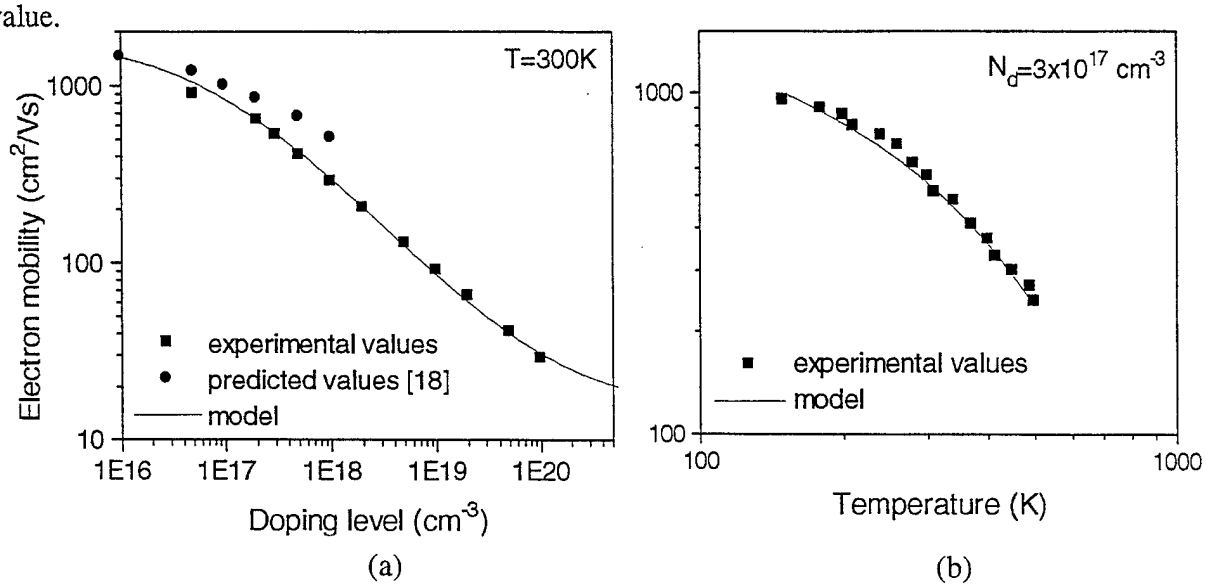


Figure 2. Electron mobility (a) versus doping level at T=300K [2, 16-19], and (b) versus temperature, for a doping level of 3x10^{17} cm^{-3} [19].

For high fields, we use a simple model for mobility versus electric field, which ignores the overshoot effect. This slightly underestimates the current, but the effect is minor for high power devices because they operate at high fields. In high electric fields, the saturation velocity is weakly dependent on temperature. The saturation velocity is modeled as a function of temperature by an empirical relation obtained by fitting the results from Monte Carlo simulation [18]:

$$v_{sat} = 2.87 \text{ x}10^7 - 9.8\text{x}10^3 \text{ x } T \text{ (cm/s)} \quad (6)$$

We assumed that optical recombination is given by:

$$R_{opt} = C_{opt}\,(np - n_i^2) \quad (7)$$

with C_{opt} =3x10^{-11}cm^3/s, from absorption experimental data and calculated electron energy band dispersion [15].

The generation rate of electron-hole pairs due to impact ionization is modeled according to Selberherr [22]:

$$G = \alpha_n \frac{|J_n|}{q} + \alpha_p \frac{|J_p|}{q} \quad (8)$$

To our knowledge, there are no experimental measurements of impact ionization rates on GaN. However, calculations of impact ionization rates using ensemble Monte Carlo simulation including the full details of all the relevant valence bands, based on pseudopotential approach, have been published recently [23]. We assume that the impact ionization rates (α_n and α_p) are dependent on the electric field and temperature for both electrons and holes according to the formula [12, 22]:

$$\alpha(E,T) = \alpha^{\infty} \exp[-(\frac{E^{crit}}{E})^{\beta}]\{1 + A[(\frac{T}{300})^{M} - 1]\} \quad (9)$$

The critical electric field also depends on T:

$$E^{crit}(T) = E_0^{crit}\{1 + B[(\frac{T}{300})^{M} - 1]\} \quad (10)$$

By fitting the results from [23], the parameters were found to be: for electrons (α^{∞} = 4.55 x 10^6 cm^{-1}, E_0^{crit}=1.19x10^7V/cm, β=1), for holes (α^{∞} = 1.48 x 10^6 cm^{-1}, E_0^{crit}=8.95x10^6 V/cm, β=1). Since there are no available results for T dependence of α, we use the values for silicon for both electrons and holes (A=0.588, B=0.248, M=1 [12]).

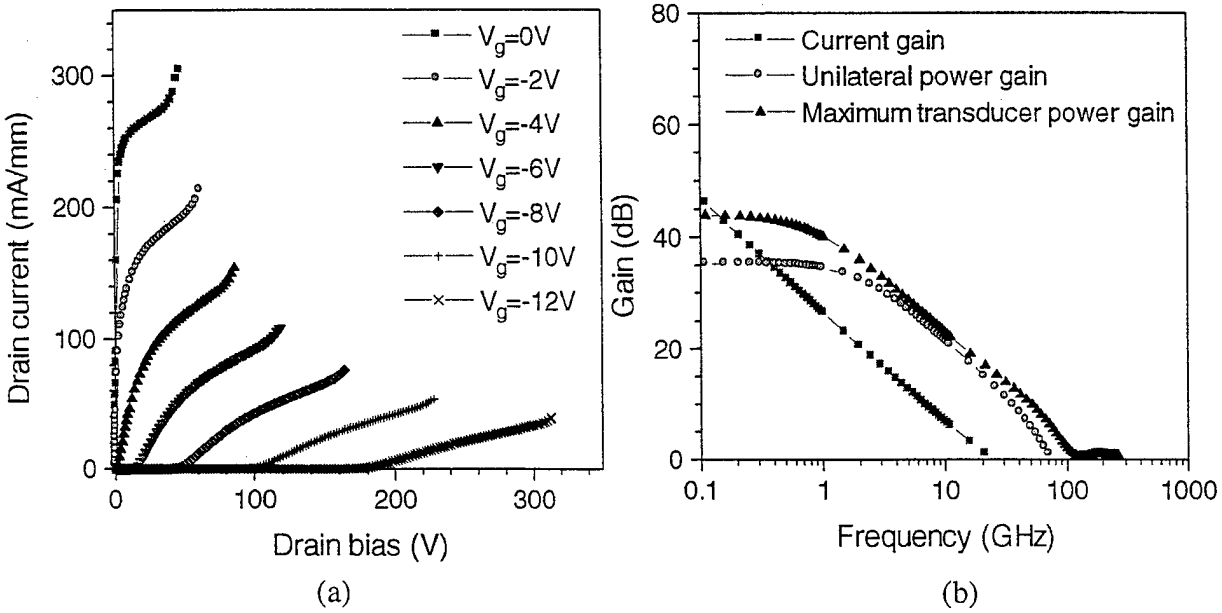
Device optimization

In order to optimize the SIT structure for operation at high power, high temperature and high frequency, DC, small signal and large signal analysis have been performed. Due to symmetry, we need to simulate only one unit cell of the transistor (Figure 1). In order to maximize the breakdown voltage as well as carrier mobility we want low doping in the channel, and 5x10^{16} cm^{-3} was chosen as a value that is achievable with current technology. As the distance between source and gate (d_{SG}) decreases, the voltage gain μ as well as transconductance, g_m increases. The value of d_{SG} is limited by the need to avoid the source to gate punch-through, when the depletion region from gate extends to that from the source. A large distance between gate and drain (d_{GD}) is desirable in order to have a large breakdown voltage. However as d_{GD} increases the series resistance also increases and this limits the frequency and current response of the device. The half-width of the source finger (W_S) determines the blocking voltage of the transistor, so it controls the voltage swing in power measurements. By balancing the above considerations we obtained the following values: the channel is 3 μm thick with a doping concentration of 5x10^{16} cm^{-3}; the n+ layers are 0.2 μm thick and have a doping concentration of 1x10^{19} cm^{-3}. The top of the device is modified in a comb configuration having the following dimensions: source half-width W_S=0.5 μm, gate half-width W_G=1.5 μm, gate height h_G=0.2 μm, d_{SG} =0.6 μm, d_{GD} =2.4 μm.

RESULTS

Our simulations indicate that the performance of the device is very sensitive to the thermal boundary conditions, as self-heating effects limit the voltage swing. In order to increase the power output we have assumed that the device is build on a SiC substrate. According to Binary [5] the SiC substrate allows about a 4x increase in power density due to the higher thermal conductivity of SiC compared to GaN or sapphire. For the same purpose, a layer of diamond paste is assumed to be present on the top of the device. We have calculated the equivalent thermal impedance of the SiC substrate and diamond layer, assuming that the length and height of the SIT is much smaller than the thickness and length of the SiC and diamond layers [12,24]. For one finger of the device, the calculations lead to a thermal impedance of 3300

W/cm^2 K for drain contact, 12000W/cm^2 K for source contact and 4050 W/cm^2 K for gate contact. Simulated drain I-V characteristics with the gate voltages varying from 0V to -12V are shown in Figure 3a. We notice that the breakdown voltage varies with the gate bias from about 50V at 0V gate bias to 320V at –12V gate bias. The simulations indicate that the breakdown is due to self-heating effects. Our results show that the performance of the device is not significantly affected by thermal generation as long as the maximum temperature in the device does not exceed 700K. The gains obtained by small signal ac simulations for a drain bias of V_d=100V and a gate bias of V_g=-6V are plotted as a function of frequency in Figure 3b. The cut off frequency is f_T=24.8 GHz and the maximum frequency of oscillations is f_{max}=75.2 GHz.



(a) (b)

Figure 3. Transistor characteristics: (a) drain I-V characteristics, and (b) gain versus frequency. The cut-off frequency is f_T=24.8 GHz and maximum frequency of oscillations f_{max}=76.5 GHz.

Large signal analysis was performed under class B, in order to obtain the output power and power added efficiency (PAE). In Figure 4 we present the output power and PAE as functions of frequency, with a DC drain bias of V_{DD}=180V, load resistance of 7.2x10^5 ohm and a gate bias voltage swing between 0 and –12 V. Under these conditions, the output power varies from 10.75 W/mm to 1.95 W/mm and PAE varies from 73.8 % to 9.1 % as we increase the operation frequency from 2 GHz to 40 GHz. The maximum theoretical PAE for operation under class B is 78.5 % [4]. Note that operation under class B requires two transistors and gate periphery of both transistors is included in output power calculations.

CONCLUSIONS

In conclusion, we modeled a static induction transistor based on GaN films. Our results show that with a SiC substrate and top side diamond paste as thermal sinks, the output power can be as high as 10.75 W/mm at 2 GHz operating frequency, with a PAE of 73.8 %. The cut-off frequency was found to be 24.8 GHz and the maximum frequency of oscillations was 75.2 GHz. These results demonstrate the excellent potential of GaN based static induction transistors for high power, high temperature and high frequency operation.

This work was supported in part by ONR through a subcontract by Raytheon.

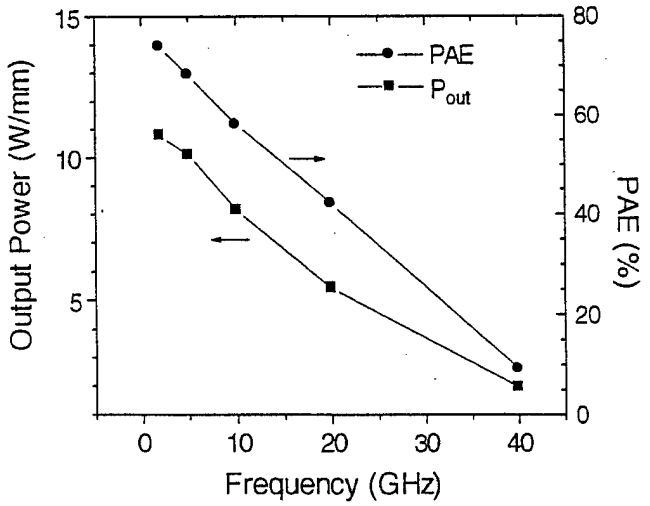


Figure 4. Output power and power added efficiency (PAE) versus frequency.

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Appendix B. Investigation of vertical transport in n-GaN films grown by molecular beam epitaxy using Schottky barrier diodes.

Investigation of vertical transport in *n*-GaN films grown by molecular beam epitaxy using Schottky barrier diodes

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In this letter, the lateral and vertical transport in lightly doped n^--GaN films, grown by plasma assisted molecular beam epitaxy, were investigated in order to explore the role of electron scattering by charged dislocations. Lateral transport constants were determined by Hall effect measurements on n^--GaN films. The doping concentration and mobility of the investigated films was $1-2\times10^{17}\,\mathrm{cm}^{-3}$ and 150–200 $\mathrm{cm}^2/\mathrm{V\,s}$, respectively. Vertical transport was studied by etching mesa structures and forming Schottky barrier diodes. The diodes exhibit near ideal forward current–voltage characteristics with reverse saturation current densities in the $1-10\times10^{-9}\,\mathrm{A\,cm}^{-2}$ range. The doping concentrations as well as the barrier height of the diodes were determined from capacitance–voltage measurements to be $8-9\times10^{16}\,\mathrm{cm}^{-3}$ and 0.95–1.0 V, respectively. The analysis of the reverse saturation current, using the diffusion theory, leads to vertical mobility values of 950 $\mathrm{cm}^2/\mathrm{V\,s}$. The significant increase in mobility for vertical transport is attributed to reduction in scattering by charged dislocations. © *2000 American Institute of Physics.*
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Several III–V nitride based devices, including lasers, light emitting diodes, photodiodes, and bipolar junction transistors have been demonstrated.[1–4] All of these devices have a vertical geometry structure. However, most measurements of transport properties in these materials are made by placing contacts on the surface of the film and measuring the lateral conductivity. Thus, lateral transport in n^--GaN films has been studied extensively and the evidence suggests that scattering by charged dislocations dominates the transport at low carrier concentrations ($n<5\times10^{17}\,\mathrm{cm}^{-3}$). At higher carrier concentrations, the charged dislocations are screened out and the lateral transport, at room temperature and below, is primarily dominated by ionized impurity scattering.[5–7] In such a model, the vertical transport is expected to be unaffected by the charged dislocations and thus electron mobility is expected to be significantly higher than that determined by using lateral transport measurements. In this letter, lateral versus vertical transport in n^--GaN films was investigated by using Hall effect measurements for the lateral transport and deducing the electron mobility for vertical transport from vertical geometry Schottky barrier diodes.

The GaN films were grown on *c*-plane sapphire, by plasma assisted molecular beam epitaxy, following procedures described earlier.[8] In this letter we present only a brief description. Prior to introduction into the growth chamber, the substrates were subjected to solvent degreasing. The Al_2O_3 surface was converted to AlN by exposing the surface to nitrogen plasma, using an electron cyclotron resonance (ECR) microwave plasma source to activate the molecular nitrogen. This nitridation step, performed at 800 °C, was followed by growth of an AlN layer (1000 Å thick) at 750 °C. The n^--GaN films were grown at 750 °C. Reflection high-energy electron diffraction (RHEED) studies of films grown under such conditions were found to have 2×2 surface reconstruction at the growth temperature, consistent with Ga polarity.[9] Two types of n^--GaN films were investigated. In the first type, the n^--GaN films were grown directly on an AlN buffer. The particular sample reported in this letter was 4.25 μm thick and it was doped *n* type with Si to doping levels in the high $10^{16}\,\mathrm{cm}^{-3}$ range. The second type of samples consisted of n^+ GaN (doping level of about $5\times10^{18}\,\mathrm{cm}^{-3}$) followed by n^--GaN doped at the same doping level as that of the first type of samples. For the particular sample reported in this letter, both the n^+ and the n^--GaN layers were 2.25 μm thick.

Circular mesas approximately 3 μm deep and 300 μm in diameter were defined on both samples by reactive ion etching, using Cl_2 gas. Ohmic contacts were defined on the bottom of the mesa by electron beam deposition of 200/1000/200/2500 Å Ti/Al/Ni/Au metal multilayers. The Ohmic contacts were rapid thermal annealed at 750 °C for 60 s, prior to deposition of the Schottky contacts. Schottky contacts were formed at the top of the mesa by patterning 200 μm dots by photolithography and depositing a 200/1000/3000 Å Ni/Pt/Au metal multilayer stack by electron beam evaporation. Some of the diodes were mounted on transistor headers and Au wires were bonded to the contacts by thermosonic bonding. Figure 1 shows a schematic illustration of the two types of devices reported in this letter.

Hall effect measurements were performed on the n^--GaN films by the Van der Pauw method, using indium contacts in the clover leaf configuration. Current–voltage characteristics were measured, at room temperature and in the range from 300 to 420 K, using the HP 4155A semiconductor parameter analyzer. The high temperature measurements were performed by heating the device on a hot chuck fitted with a temperature controller. Capacitance–voltage

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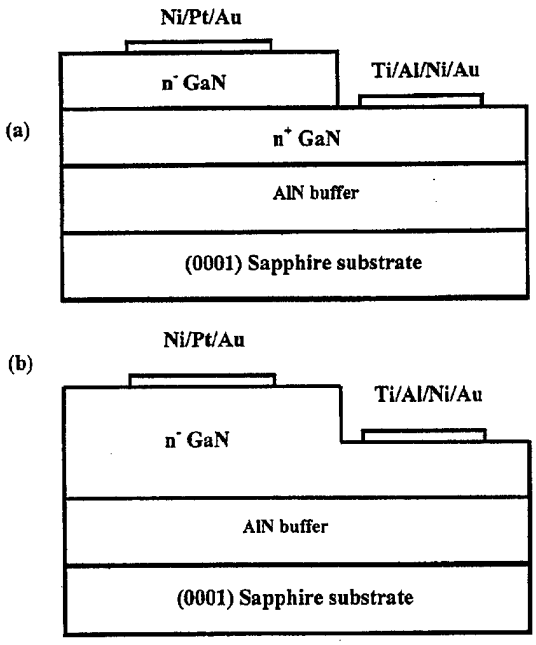

FIG. 1. Schematic illustration of the vertical geometry Schottky barrier diode on samples (a) with n^+/n^--GaN layers and (b) n^--GaN layer.

measurements were performed using the HP 4275A LCR measurement system.

The current–voltage characteristics of the two reported devices are shown in Fig. 2. In the forward direction the data can be fitted to the expression

$$J = J_0 \exp\left(\frac{qV}{nkT}\right), \tag{1}$$

where J_0 is the saturation current density and n is the ideality factor. Applying Eq. (1) to the data of Fig. 2, we find that the diodes are practically ideal ($n = 1.15$–1.2) and the value of the reverse saturation current densities for the n^+/n^- and n^--GaN samples are 1.08×10^{-9} and 1.08×10^{-8} A/cm^2, respectively. In addition, for the sample with the n^+/n^- configuration the current–voltage (I–V) characteristics were measured as a function of temperature, in the 300 to 420 K range, and the barrier height was determined to be $\phi = 1.0$ V.

The carrier concentration in the two types of samples was determined by measuring the Hall effect on the n^--GaN

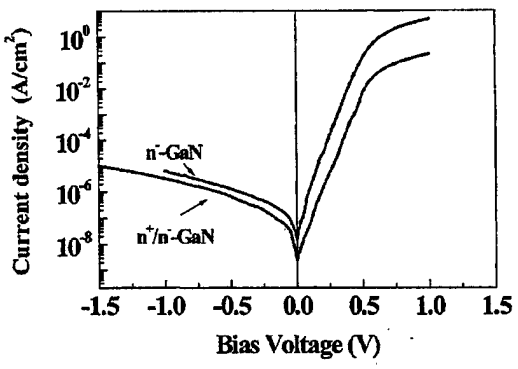

FIG. 2. Current–voltage characteristics of n^--GaN Schottky barrier diodes fabricated with vertical geometry.

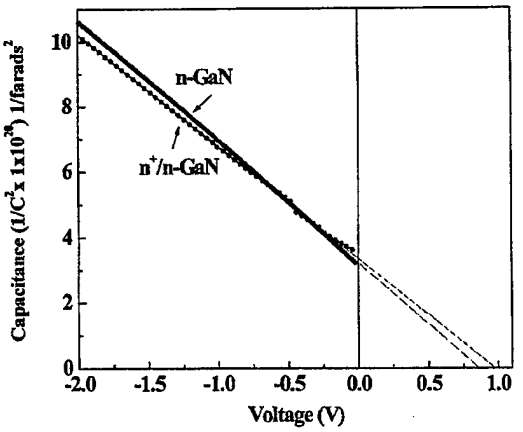

FIG. 3. Capacitance–voltage characteristics of n^--GaN Schottky barrier diodes fabricated with vertical geometry.

films as well as by measuring the capacitance voltage characteristics of both types of Schottky barrier diodes. From the Hall effect measurements we found that the carrier concentration of the n^--GaN film was 1.4×10^{17} cm^{-3} and the lateral mobility (μ_1) was 160 cm^2/V s. Although the dislocation densities in these particular samples have not been measured, from measurements on samples grown under similar conditions, the threading dislocation density are estimated to be in the range of $5-10\times10^9$ cm^{-2}.[5–7] As discussed previously, the lateral electron mobility in our samples attains its highest value at 300–400 cm^2/V s at a carrier concentrations of $3-5\times10^{17}$ cm^{-3} and then it reduces at lower carrier concentrations. This result was accounted for by scattering from negatively charged dislocations.

Results of the capacitance–voltage (C–V) measurements are shown in Fig. 3. The doping concentration and barrier height were determined from the C–V measurements, using the following equation:[10]

$$\frac{1}{C^2} = \frac{2}{A_e^2}\left(\frac{(V_{bi}-V)}{q\epsilon_s N_d}\right), \tag{2}$$

where C is the measured capacitance, V is the applied voltage, V_{bi} is the built-in voltage, ϵ_s is the dielectric constant, N_d is the doping concentration, and A_e is the geometric area of the device. The barrier height is given by

$$\phi = \left[V_{bi} + \left(\frac{kT}{q}\right)\ln\left(\frac{N_c}{N_d}\right)\right], \tag{3}$$

where N_c is the effective density of states in the conduction band.

The doping concentration and barrier height, obtained by fitting the data of Fig. 3 to Eqs. (2) and (3), were determined to be 9×10^{16} cm^{-3} and 1.0 eV for the n^+/n^--GaN diode and 8.4×10^{16} cm^{-3} and 0.95 eV for the n^--GaN diode. These results are in general agreement with those reported earlier.[11,12] A number of devices, fabricated on the same wafer were tested and were found to give similar values of barrier heights, doping concentration, and reverse saturation current densities. Table I summarizes the values of the various parameters of the investigated samples (devices) determined from the Hall effect, I–V and C–V measurements.

TABLE I. Transport and material parameters measured for n^--GaN films and Schottky diodes with vertical geometry.

Sample	Hall effect measurements		Schottky barrier diode measurements				
	μ_1 ($cm^2/V\,s$)	N_d ($cm\,s^{-3}$)	n	J_0 (A/cm^2)	ϕ (V)	N_d (cm^{-3})	μ_v ($cm^2/V\,s$)
n^--GaN	160	1.4×10^{17}	1.15	1.0×10^{-8}	0.95	8.4×10^{16}	949
n^+/n^--GaN			1.2	1.08×10^{-9}	1.0	9.0×10^{16}	932

In order to investigate the electron mobility for vertical transport, we consider the diffusion theory of Schottky barriers, which expresses the relation between the reverse saturation current as a function of barrier height and the diffusion coefficient of electrons in the space charge region. According to this model, the reverse saturation current density is given by the relation[13]

$$J_0=\left\{qN_c\mu_v\left[\frac{2qV_{bi}N_d}{\epsilon_s}\right]^{1/2}\right\}\exp\left(\frac{-q\phi}{kT}\right), \tag{4}$$

where μ_v is the electron mobility in the vertical direction. Using the values of J_0, N_d, ϕ, and V_{bi} in Eq. (4), we obtain a vertical mobility $\mu_v=932\,cm^2/V\,s$ for the n^+/n^--GaN and $\mu_v=949\,cm^2/V\,s$ for the n^--GaN film. In the calculation of the vertical mobility, we have assumed that the active area is equal to the geometric area of the device. However a reduction of the active area (up to one-third for dislocation density of $5\times10^9\,cm^{-2}$ and doping concentrations of $1\times10^{17}\,cm^{-3}$) is expected due to depletion around each charged dislocation. Specifically, considering the active area to be two-thirds the geometric area, increases the doping concentration and reverse saturation current density to $1.9\times10^{17}\,cm^{-3}$, $1.62\times10^{-9}\,A/cm^2$, respectively for the n^+/n^- device. This leads to a vertical mobility of $1070\,cm^2/V\,s$ for the same device. These results are in good agreement with Monte Carlo calculations for electron mobility in GaN thin films.[6]

In conclusion, we have studied lateral and vertical transport in n^--GaN films and found that for samples doped at the level of $1\times10^{17}\,cm^{-3}$, the vertical mobility is approximately six times higher than the lateral mobility. This result is attributed to the reduction of electron scattering by charged dislocations during vertical transport.

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