NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA

THESIS

ANALYSIS, SIMULATION, AND FABRICATION OF CURRENT MODE CONTROLLED DC-DC POWER CONVERTERS

by

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December 1999

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	December 1999	Master's Thesis

4. TITLE AND SUBTITLE
ANALYSIS, SIMULATION, AND FABRICATION OF CURRENT MODE CONTROLLED DC-DC POWER CONVERTERS

5. FUNDING NUMBERS

6. AUTHOR(S)
Thomas P. Hekman

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Naval Postgraduate School
Monterey, CA 93943-5000

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(maximum 200 words)*

A modular DC Zonal Electrical Distribution System (DC ZEDS) offers advantages in both cost and weight over traditional radial shipboard distribution. In order to equip the next class of surface combatant with DC ZEDS, preparative research includes the design of autonomous DC-DC power converter modules having robust load sharing capability. This thesis examines the utility of current-mode switch control applied to high-voltage DC-DC power converters. A state-space representation for a current-mode controlled buck converter is developed. The system is modeled dynamically using the Advanced Continuous Simulation Language (ACSL). System stability and frequency response is modeled using MATLAB. A hardware controller is fabricated to implement current-mode control using available laboratory equipment.

14. SUBJECT TERMS	15. NUMBER OF PAGES
DC-to-DC Buck Converter, Current-Mode, ACSL	104
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18, 298-10

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ANALYSIS, SIMULATION, AND FABRICATION OF CURRENT MODE CONTROLLED DC-DC POWER CONVERTERS

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Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
December 1999

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ABSTRACT

A modular DC Zonal Electrical Distribution System (DC ZEDS) offers advantages in both cost and weight over traditional radial shipboard distribution. In order to equip the next class of surface combatant with DC ZEDS, preparative research includes the design of autonomous DC-DC power converter modules having robust load sharing capability. This thesis examines the utility of current-mode switch control applied to high-voltage DC-DC power converters. A state-space representation for a current-mode controlled buck converter is developed. The system is modeled dynamically using the Advanced Continuous Simulation Language (ACSL). System stability and frequency response is modeled using MATLAB. A hardware controller is fabricated to implement current-mode control using available laboratory equipment.

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I. PROJECT BACKGROUND

A. MACHINERY REQUIREMENTS FOR THE 21ST CENUTRY NAVAL VESSEL

The affordability objectives of standardization and process simplification will guide naval ship design and construction well into the first half of the 21st century. The Engineering Directorate of the Naval Sea Systems Command has established that future construction programs will use common modules with standard components and interfaces to support generic build strategies thereby reducing the total cost of ownership. Tying affordability objectives together with operational effectiveness requirements results in a need to design a power distribution architecture which is scalable, flexible, and capable of being applied to any ship class with minimal design effort. Crew size reduction objectives for future vessels require that maintenance time and crew operating requirements be minimized. Survivability objectives require the architecture be designed with sufficient redundancy and capacity to sustain damage. Enhanced survivability further requires the equipment associated with this architecture occupy a minimal space volume. Traditional power distribution for seagoing vessels uses a radial distribution architecture. This architecture must be designed for each ship class and does not meet the requirements stated above for the 21st century combatant. A zonal electric distribution system with integrated full electric propulsion is envisioned to meet the requirements stated above. [1]

B. RADIAL AND ZONAL DISTRIBUTION

Naval vessels currently use a radial electric power distribution system. This system consists of multiple generators which provide power directly to a specific

switchboard. Power is distributed from each switchboard to load centers located throughout the ship. Numerous three-phase transformers step down the 450V three-phase AC to single-phase 115V AC for ships service power. The generators are usually located in a main machinery space, co-located with the switchboard and the main propulsion machinery. Survivability for critical loads is enhanced by providing redundant power sources which originate from separate generators and switchboards.

A zonal power distribution architecture typically employs two main busses, one port and one starboard. These busses are separated vertically as well with one being below the waterline and one above the waterline. Figure (1-1) illustrates the differences between the zonal and radial distribution. Each bus supplies a zone via a load center. Vital loads are connected to each load center and, therefore, each bus via an Automatic Bus Transfer (ABT). The major advantage of zonal distribution is that only the main busses will pass through watertight boundaries. This has an inherent benefit to production as all electrical cabling may be installed and tested in a zone or module prior to final hull assembly. A comparison of a proposed zonal and a current distributed architecture on a U. S. Navy DDG-51 class ship was completed in 1993 and is documented in Table (1-1) and Table (1-2). [2]

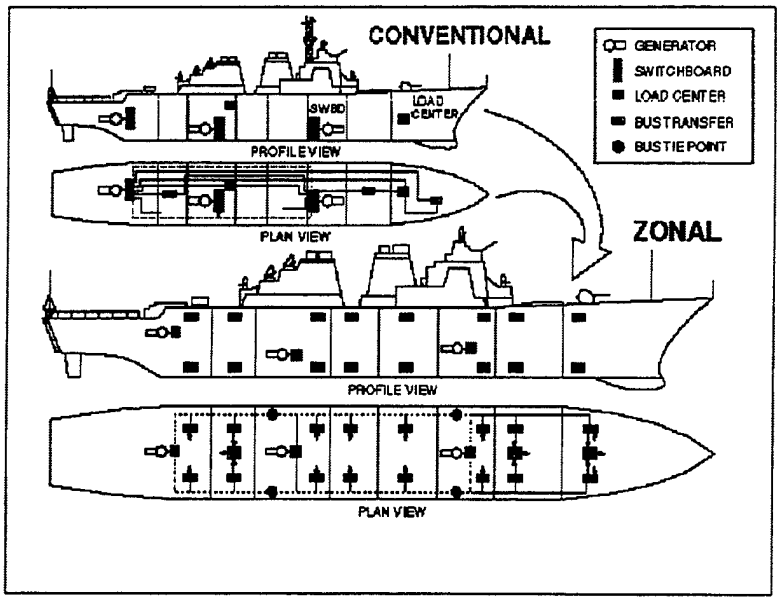

Figure 1-1: Conventional Radial vs. Zonal Distribution. (From Ref. [2])

Apparatus	Removal (LT)	Install (LT)	Net Change (LT)
Foundation	3.3	4.3	+1.0
Power Cables	116.7	79.8	-36.9
Switchgear	20.8	20.0	-0.8
Total	**140.8**	**104.1**	**-36.7**

Table 1-1: Zonal vs Radial Architecture Weight Comparisons. (From Ref. [3])

Apparatus	Radial (Material and Labor)	Zonal (Material and Labor)
Foundation	34k	44k
Power Cables	4,151k	2,839k
SWBD and Load Centers	1,807k	1,736k
Total	**5,992k**	**4,619k**

Table 1-2: Zonal vs Radial Architecture Cost Comparisons. (From Ref. [3])

C. DC VERSUS AC DISTRIBUTION

There are several advantages to utilizing DC distribution over AC distribution. The converter and inverter modules are capable of performing many functions that currently require separate components. These functions include power conversion, system monitoring, and current limiting. The solid-state semiconductor devices present in converters and inverters offer inherent system protection during fault conditions. Since the control inputs to both are DC Currents, fault current detection systems are simpler and can operate faster than their AC system counterparts. This reduces the lag time associated with Automatic Bus Transfers thereby enhancing system protection and survivability. Major faults are isolated to the systems fed by the affected converter or group of parallel converters and do not affect the main bus.

Another benefit to DC distribution over AC is that the bus frequency does not need to be tied to the operating frequency of any major equipment. Therefore, power consuming equipment may be operated at the most efficient speed rather than at a speed determined by bus frequency. This decoupling of generator frequency from distribution requirements allows for flexibility in the selection and operation of power generation equipment. As new technologies emerge, for example fuel cells, power generation equipment could be replaced with more cost effective or environmentally sound

technology and this replacement would have no impact on distribution in a DC architecture.

Finally, space and weight savings, as illustrated in Table 1-1, would permit the inclusion of additional weapon systems, fuel, cargo, and/or habitability improvements in future ship designs. [2]

D. DC ZONAL DISTRIBUTION

Shipboard DC power distribution will be designed utilizing a zonal architecture. This distribution architecture is referred to as the DC Zonal Electric Distribution System (DC ZEDS). DC ZEDS is comprised of the following major components: power generation and rectification, Ship Service Converter Modules (SSCM), Ship Service Inverter Modules (SSIM), and the required connection, protection, and control electronics.

In DC ZEDS power may be generated by any method provided sufficient wattage is produced. NAVSEA estimates that future surface combatant electrical loads will exceed 4MW. The current plan is to use AC generators driven by a prime mover. The output is then stepped down with a transformer, rectified using phase-controlled rectifiers, and distributed along the main bus. The type of generator and prime mover is not important to the distribution system. This fact creates the flexibility to include evolving and more cost effective technologies in construction and ship class improvement programs. Examples of new AC power conversion technology include superconducting homopolar machines, high-temperature superconducting synchronous machines, and permanent magnet rotor machines. [2]

Advances in DC power generation technology may allow the inclusion of DC generators thereby eliminating the need for rectification prior to supplying the DC bus. Fuel cells are an example of a DC generation method which can be adapted for shipboard use. The German Navy is currently operating prototype fuel cell power generation systems for the Type 212 Submarine. Current projections estimate multi-MW fuel cell

prototype field tests will be completed in the year 2000. Given current projections for cost reduction, improvement in efficiency, and increased power capacity, coupled with the environmental benefits inherent to the technology, fuel cells are a viable alternative for electrical power generation. [4]

One element of power conversion in DC ZEDS is accomplished by the SSCM. The SSCM is a buck converter and serves as a buffer between the main bus and the loads of the zone that the converter serves. This buffer provides the protection to the main bus inherent in a zonal architecture. Typical DC ZEDS zone loads are expected to range from approximately 400kW to 800kW. Several SSCM units may be paralleled for redundancy and to meet the expected current levels (364-728A).

AC power is supplied by the SSIM. The inverter module converts the SSCM output to three-phase AC. The SSIM output is used to drive both single-phase and three-phase loads. The single-phase loads are evenly balanced across the three-phases of the SSIM to maintain balanced operation. Expected AC power requirements within a zone range from 10kW to several hundred kW. As with the DC converter modules, the SSIMs would be operated in parallel within a given zone to provide the required redundancy and sufficient power. [2]

E. POWER ELECTRONIC BUILDING BLOCK

In order to accommodate the numerous converter switching schemes expected in an integrated zonal distribution system, the common platform controller is to be implemented using a Digital Signal Processing (DSP) approach rather than an analog approach. As no commercially available controllers meet all requirements, especially the intensive Input/Output signal handling requirements of the SSIM, personnel at NSWC Carderock Division, Annapolis, Maryland, (now Philadelphia, PA) designed the Power Electronic Building Block (PEBB) Universal Controller. The prototype PEBB Controller is based on the Texas Instruments TMS320C30 DSP chip. Communication between the controller bus and the converters and inverters is accomplished by optical fiber for

enhanced reliability and reduced ElectroMagnetic Interference (EMI). An illustration of the first-generation PEBB Controller is shown in Figure (1-2). [5]

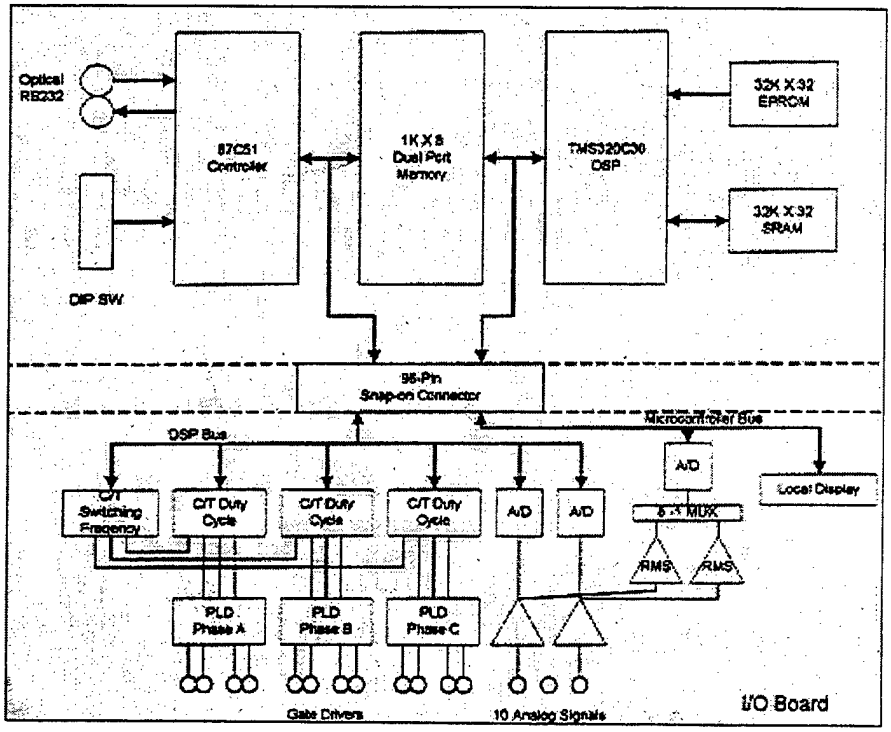

Figure 1-2: PEBB Controller. (From Ref. [2])

F. DC ZEDS AND PEBB RESEARCH AT NPS

A number of Naval Postgraduate School theses in recent years have investigated DC ZEDS and PEBB issues. A brief overview of those efforts in order of thesis completion follows.

- A detailed SIMULINK model of a portion of a shipboard electric distribution system was developed in order to investigate control of a three-phase synchronous generator [6].
- Constant power characteristics of a DC ZEDS were investigated with reduced-order DC-DC converter models. From these PSPICE models, observations were made concerning stability and controllability [7].

- A method for using the Advanced Continuous Simulation Language (ACSL) built-in algebraic solver which neither relied upon reformulated machine representations nor introduced fictitious circuit components was developed [8].
- Work was begun on detailed ACSL modeling of DC-DC buck switching converter and a three-phase inverter. Closed-loop algorithms for buck converters were investigated, and hardware-in-the-loop studies were conducted using a dSPACE card in order to validate computer models [9].
- A detailed ACSL simulation containing a steam turbine-driven synchronous machine, rectifier, filter, and buck converters was developed. This ACSL model was used to identify paralleling issues [10].
- The closed-loop buck converter algorithm was significantly advanced [11].
- A detailed ACSL representation of an Auxiliary Resonant Commutated Pole (ARCP) Inverter was developed [12].
- The one-cycle control algorithm for a buck converter was considered and implemented. Comparisons were made between the hardware and computer representation [13].
- Design and fabrication of several buck converter power sections were documented [14].
- A voltage-mode buck controller was designed, along with the required gating circuitry. The associated analog hardware was built and documented [15].
- A PEBB testbed interconnecting DC-DC and DC-AC converters was fabricated. This testbed was intended to simulate various configurations of SSCM and SSIM modules. Hardware studies investigating transient response of the testbed in a few different configurations were designed and performed [16].

- The operation of the Programmable Universal Controller (PUC)—an in-house programmable DSP controller—was documented and the closed-loop algorithm for the buck controller was programmed and validated. Additionally, an approach for implementing closed-loop control of ARCP inverters was suggested [17].
- Closed-loop ARCP algorithms were implemented using the PUC [18].
- Frequency-based load sharing in current-mode controlled buck converters was investigated and an ACSL model developed. In addition, an RMS frequency estimation circuit was designed and constructed in order to estimate the current from individual converters operating in parallel [19].
- Algorithms were developed for paralleling 3-phase DC-AC inverters to ensure proper sharing of real and reactive power. [20]
- A soft-switching DC-DC buck converter was simulated in PSPICE and fabricated. [21]

G. THESIS GOALS

This thesis explores the design and fabrication process for a current-mode controlled DC-DC converter. Two control methods are evaluated to determine the best control response for the available lab equipment. The converter and the respective control implementations are modeled using MATLAB and the Advanced Continuous Simulation Language (ACSL). Controller designs are modeled using PSPICE. In addition, the use of the Unitrode Corporation UC3846 chip as a controller for DC-DC converters is explored. The initial goal is to apply the UC3846 chip to a single converter and, if successful, apply the chip to two converters operating in parallel. Additional goals include the construction and implementation of current-mode control using two control methods suggested in the literature. These controllers will then be used in future research into parallel operation of converters.

H. CHAPTER OVERVIEW

Chapter II covers the design and construction of the converter power section. Voltage-mode and current-mode control are compared and contrasted. A stability problem present in current-mode control when operating above 50 percent duty-cycle is introduced and a method for ensuring stability is discussed. Two separate methods of current-mode control are proposed and controller designs are presented. The application of the Unitrode UC3846 PWM Controller as a control method is investigated and an analysis of the chip is presented. Chapter III covers the derivation of a mathematical model for current-mode control. A closed-loop solution for a buck converter using current-mode control is presented. The required integral and proportional gains are determined and closed-loop stability is investigated. The closed-loop model derived in Chapter III is used as the model for the dynamic simulations covered in Chapter IV. Chapter IV presents a dynamic analysis of current-mode control in response to various step-changes in load. A summary of the research work and recommendations for additional follow-on work is presented in Chapter V.

II. BUCK CONVERTER

A. POWER SECTION

The bulk of this thesis deals with development of a switch controller for a DC-DC converter using commercial-off-the-shelf components. The following section discusses determination of the components of the buck converter power section. Figure (2-1) illustrates the power section of a buck converter.

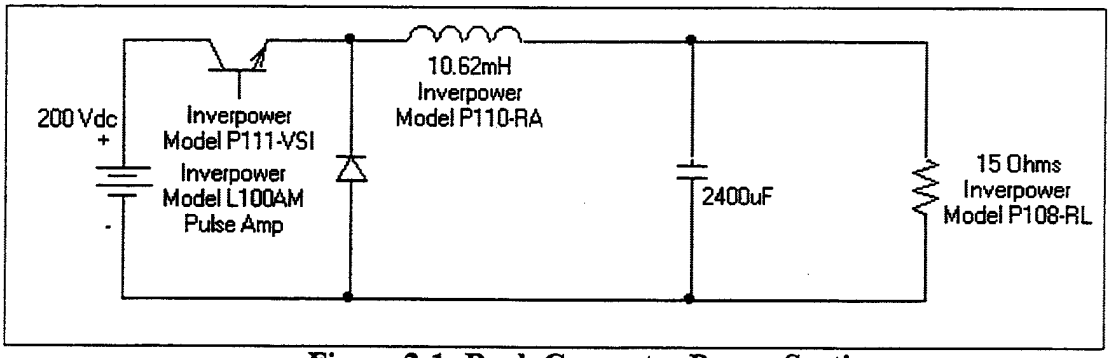

Figure 2-1: Buck Converter Power Section.

1. Specifications

The power converter constructed for this thesis is a 1.5 kW buck converter with a reference output voltage (V_{out}) of 150 V and nominal input voltage (V_{in}) of 200V. This combination of V_{out} and V_{in} yields a steady-state duty ratio (D_{ss}) of 0.75. The switching frequency (f_s) is selected to be 2 kHz, resulting in a switching period (T_s) of 0.5 ms. These values are not meant to be representative of values anticipated for DC ZEDS, rather they were selected to illustrate proof-of-concept and to be consistent with available laboratory equipment. The next section highlights critical inductance and capacitance derivations for the system used in the subsequent analysis and simulation.

2. Critical Inductance

Critical inductance, or the minimum inductance for continuous conduction mode [22], is given by

$$L_{crit} = \frac{R_{crit}}{2f_s}(1 - D_{ss}) \tag{2-1}$$

where R_{crit} is the critical load resistance. Since continuous conduction is desired for loads above 10 percent of rated load, R_{crit} is determined from

$$R_{crit} = 10R_{rated} \tag{2-2}$$

R_{rated} is calculated from the desired power (1.5kW) and V_{out} (150V) and was determined to be 15Ω. R_{crit} for this converter is 150Ω, thus L_{crit} is 9.37mH. A value of 10.62mH was selected to match the 25 percent tap on the inductors available in the lab.

These values can be used to determine the steady-state inductor current maximum and minimum values, I_{max} and I_{min}, using the following equations from Fisher [23]

$$I_{\min} = D_{ss}V_{in}\left[\frac{1}{R_{rated}} - \frac{(1 - D_{ss})T_s}{2L}\right] \tag{2-3}$$

$$I_{\max} = D_{ss}V_{in}\left[\frac{1}{R_{rated}} + \frac{(1 - D_{ss})T_s}{2L}\right] \tag{2-4}$$

yielding I_{max} = 10.88A and I_{min}= 9.12A.

3. Capacitance

Capacitor selection to meet the ripple criterion, as stated by Ashton and Ciezki [22], is given by the expression

$$C_{\min} = \frac{D_{ss}}{8\Delta V_c f_s^2 L}(V_{in} - V_{out}) \tag{2-5}$$

where ΔV_c is peak-to-peak capacitor voltage ripple. In this case a value of 1.0 volt was arbitrarily specified. This yields a C_{min} of 73.5μF as the absolute minimum. Past experience has shown that the required value of C can range from 10 to 100 times C_{min} based on achieving the desired transient response. A 2.4mF capacitor was used as it was available in the lab. Preliminary bench tests of the converter using the above components were satisfactory with performance well within all expected parameters.

B. CONTROL OF BUCK CONVERTERS

The power section as described may be fitted with any of a number of types of switch controllers. Voltage-mode and current-mode control are the most common methods. Both control methods use constant switching frequency, which is also assumed in the previous L_{crit} and C_{min} derivations.

1. Voltage-Mode Control

The classical switch control method is Pulse-Width-Modulation (PWM), also known as duty-ratio programming. PWM control of DC-DC converters using voltage

feedback is commonly referred to as *voltage-mode control.* The switch is controlled by a constant frequency pulse function of varying duty cycle. The switch control signal is generated by comparing an error-derived signal with a repetitive waveform, typically a sawtooth. The reference voltage, V_{ref}, is subtracted from the output voltage, V_{out}, to form an error signal which may be then processed through a compensator to produce the control modulating signal. An illustration of voltage-mode switch control is given in Figure (2-2). A drawback of voltage-mode control is that any perturbation in the input voltage will not be detected by the control circuit until it has passed through the output filter of the converter. This delay limits the response of the control circuit to sinusoidal variations in the input voltage, resulting in slow dynamic performance. Two separate control methods may be used to alleviate this problem: voltage feed-forward control and current-mode control. Current-mode control offers the fastest dynamic response. [24]

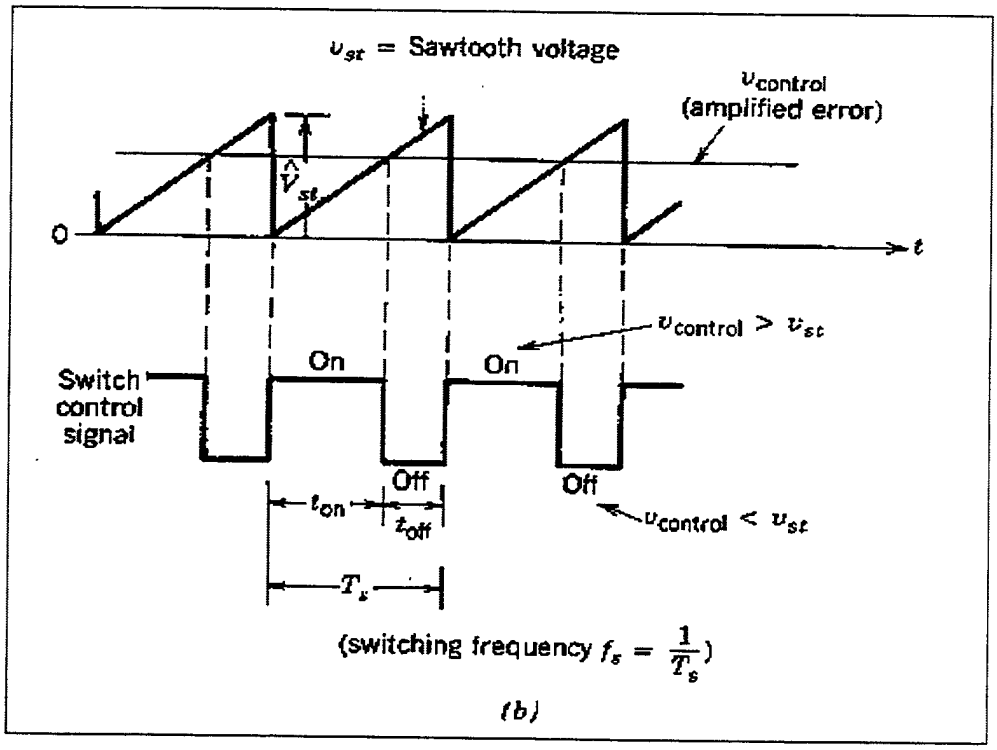

Figure 2-2: PWM Switch Control. (From Ref. [24])

2. Current-Mode Control

Current-mode control adds an inner loop where the control voltage directly controls the inductor current. The control voltage is generated from the difference between a reference voltage and the actual output voltage of the converter. This control voltage is referred to as I^* in the text and I_{star} in drawings. The inductor current provides a virtual measure of the input voltage. The inductor current (I_L) or the switch current (I_{sw}) is sensed prior to the output filter of the power section and therefore does not experience any of the delays associated with the output filter. Directly controlling the current feeding the output stage significantly improves dynamic performance. A comparison of voltage-mode and current mode topologies is shown in Figure (2-3).

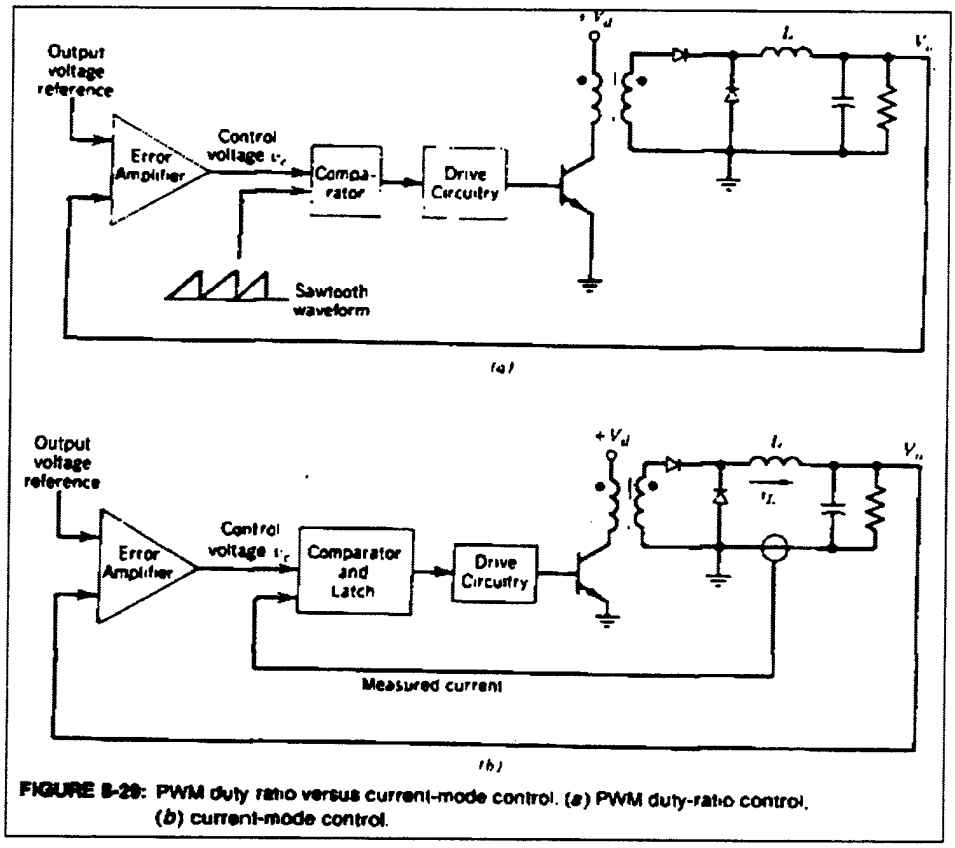

FIGURE 8-29: PWM duty ratio versus current-mode control. (*a*) PWM duty-ratio control. (*b*) current-mode control.

Figure 2-3: Voltage-mode (a) and Current-mode (b). (From Ref. [24])

The most common method of current-mode control is *constant-frequency control with a turn on at clock time*. The switch is closed at the beginning of each clock interval (T_s). The control voltage signal determines when the switch is turned off. A constant frequency switch period is assumed when determining the values of L and C in Chapter II. A slope compensation must be added to the sensed current waveform or subtracted from the control voltage to ensure stability when operating above a 50 percent duty cycle (D_{ss}). This requirement is discussed in the next section. The advantages of current-mode control include:

1. Peak switch current limiting is inherent to the design.
2. One pole is removed from the control-to-output transfer function. The second-order system therefore reduces to a first-order system, simplifying the control.
3. Allows for equal current sharing when multiple converters are operated in parallel using the same control voltage.
4. Inherently provides for input voltage feed-forward as any perturbation in the input voltage will be almost immediately reflected in the switch or inductor current. Since either the switch or the inductor current is a direct control input, this perturbation is very rapidly corrected. [24]

Possible current-mode control functional flow block diagrams for the voltage control loop and current control loop are illustrated in Figure (2-3) and Figure (2-4).

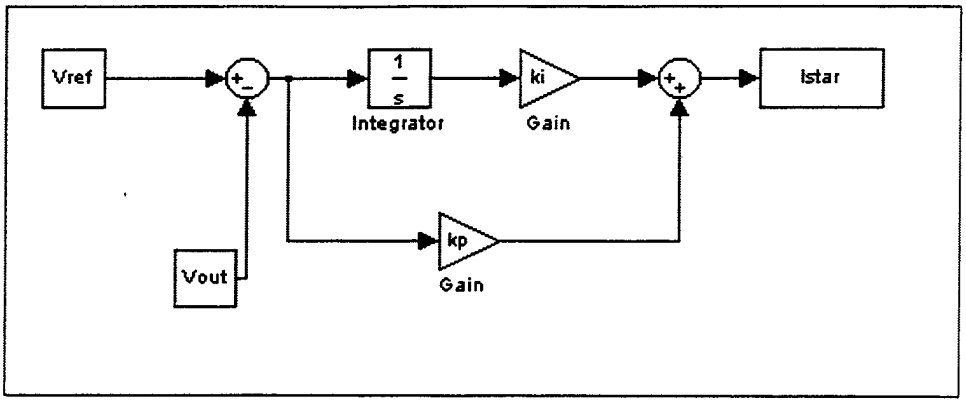

Figure 2-4: Voltage Control Loop.

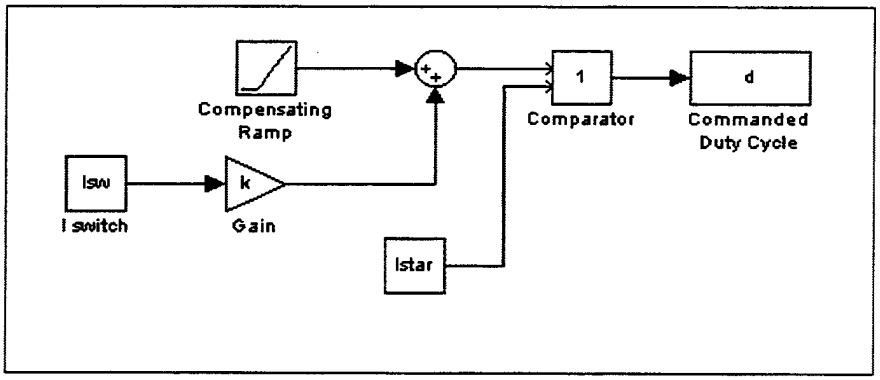

Figure 2-5: Current Control Loop.

3. Stability Issues in Current-Mode Control

Current-mode control exhibits an inherent instability that results from using the switch current to control the same switch. This constitutes an internal feedback which has the potential to introduce oscillation when the duty cycle exceeds fifty percent. This instability is illustrated in Figure (2-6).

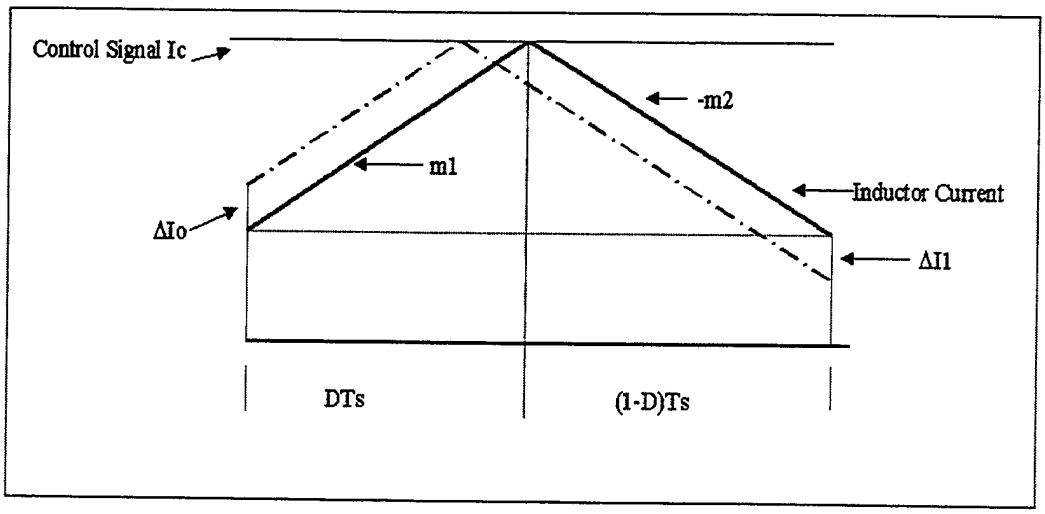

Figure 2-6: Propagation of a Perturbation in a Single Cycle. (From Ref. [25])

When the switch is closed the steady-state inductor current has a slope of m1 = $(v_{in}-v_{out})/L$; when the switch is open the steady-state inductor current has a slope of – m2 = $(-v_{out}/L)$. Using the basic rise over run formula for the slope of a line it is evident that m2/m1 = D/(1-D), where D is the ideal steady-state duty cycle, (V_{out}/V_{ref}). A perturbation to the inductor current at the beginning of a cycle is shown as ΔI_o. This perturbation is shown as ΔI_1 at the end of a single cycle (T_s). ΔI_1 is now the initial value of the perturbation for the next cycle. This pattern repeated indefinitely potentially results in the perturbation growing exponentially over a number of cycles. The final value of the perturbation after n cycles is given by:

$$\Delta I_1 = -\left(\frac{D}{(1-D)}\right)^n \Delta I_0 \qquad (2\text{-}6)$$

Equation (2-6) clearly illustrates that current-mode control is unstable above a fifty percent steady-state duty cycle as the perturbation grows whenever the quantity (D/(1-D)) is greater than one.

This instability can be eliminated by the addition to the measured current of a suitable ramp function or the subtraction of a ramp from the control signal I^*. This procedure is illustrated in Figure (2-6) and Figure (2-7).

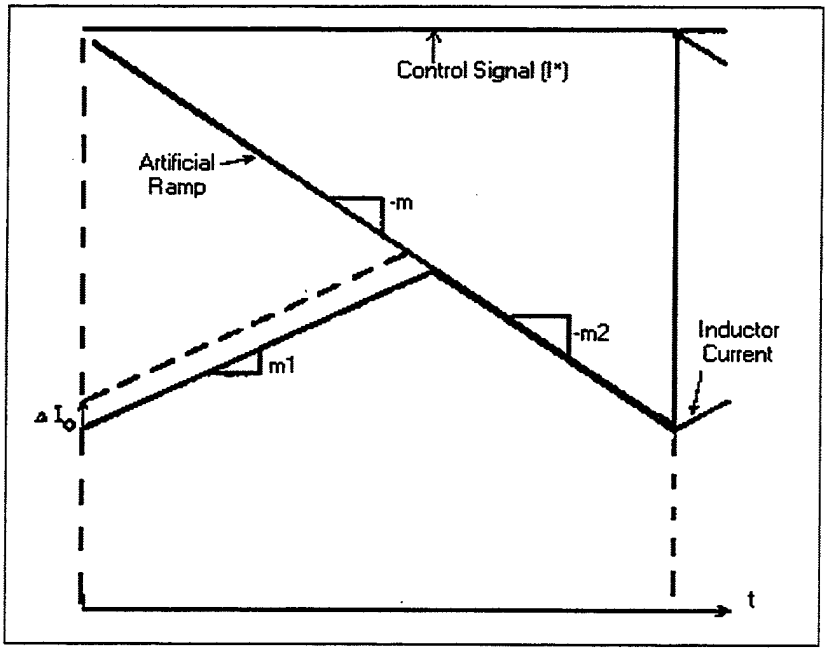

Figure 2-7: Elimination of Perturbation after a Single Cycle. (from[25])

The addition of a stabilizing slope (m) to Equation (2-6) results in:

$$\Delta I_n = \left(-\frac{m2 - m}{m1 + m} \right)^n \Delta I_0 \qquad (2\text{-}7)$$

From Equation (2-7) it is evident that a stabilizing slope of m = m2 will result in the elimination of a perturbation in a single cycle. The stabilizing slope will ensure inner loop stability and also serve to guarantee the fastest possible transient response.

Two additional issues concerning stability warrant discussion.

1. Current must be sensed using a non-magnetic device. A magnetic device, such as a Hall Effect transformer, will introduce an additional stability concern due to the magnetizing current of the transformer.
2. Ideally, the stabilizing slope should always match the slope m2 exactly, this would ensure stability at any operating point. To accomplish this within the time span of the same cycle would require a very fast method of evaluating the slope m2 and then creating a suitable ramp function. As this is not always feasible, common practice is to use a constant-slope stabilizing ramp which is determined from the steady-state operating point. [25]

C. CONTROLLER DESIGN

1. Classical Design Approach

The control algorithm used in the simulation for model one in Chapter IV is based on the discussion on current-mode control found in Krein (Ref.[26]). A detailed mathematical development for this control is described in Chapter III . Determination of the gains for the control are also described in Chapter III. The control is implemented using LM741 Operational Amplifiers and is illustrated in Appendix C.

2. Middlebrook Based Design

In this section a controller is designed using Middlebrook's approach (Ref. [27]). The converter specifications listed in Chapter II, Section A, apply to all calculations in this sub-section. This design is the basis for simulation model two described in Chapter IV. The control topology is shown in Figure (2-8).

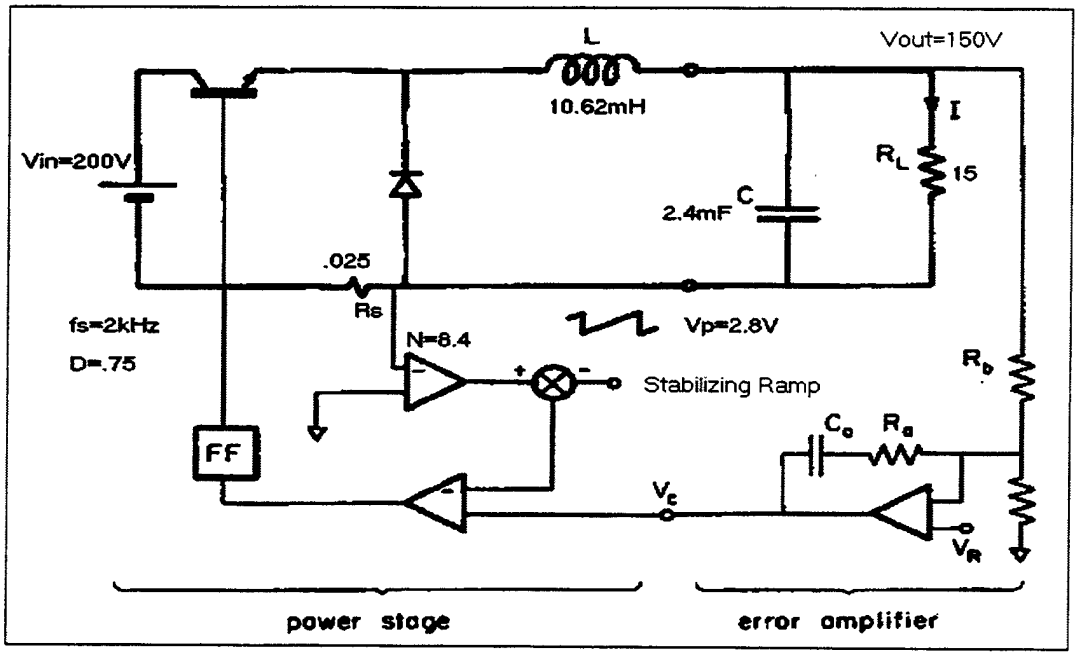

Figure 2-8: Middlebrook-Based Control Topology. (From Ref. [27])

a) Current Sensing and Slope Compensation

A 25mΩ resistor is used to sense the switch current. This resistor is made up of four Allied Electronics 100mΩ wire wound resistors connected in parallel. This produces a steady-state differential voltage of 0.250V at the gain amplifier input. The actual differential voltage should vary from 0.228V to 0.272V based on an I_{max} of 10.88A and an I_{min} of 9.12A. The gain (N) is selected so that the gain amplifier output will be equal to the product of the peak voltage of the stabilizing ramp (V_p) and the steady-state duty cycle (D_{ss}). A gain of 10.5 was selected to produce 2.6V out based on a 3.5V stabilizing ramp. The previously stated stability requirement for the stabilizing ramp slope to equal the current slope during the switch open period is not followed here and instead a numerical parameter n is defined to relate the equivalent current slope (M_c) to the inductor switch closed current slope (M_1). This parameter is defined:

$$n \equiv 1 + \frac{2M_c}{M_1} \tag{2-8}$$

and M_c is defined as:

$$M_c = \frac{V_p}{T_s N R_s}. \tag{2-9}$$

V_p is the stabilizing ramp peak voltage, N is the current sense amplifier gain, T_s is the switching period, and R_s is the value of the resistor used for current sensing (25mΩ). The above values result in a value of n = 12.32. The maximum duty cycle is given by D_{max} = n/(n+1) and this yields a maximum duty cycle of 0.924. The minimum line voltage required to sustain 150V is given by V_{out}/D_{max} or a voltage of 163V. The parameter n1 is defined as the minimum value of n required for stability and is given by $(1+D_{ss})/(1-D_{ss})$. For a duty cycle of .75, the minimum value of n1 is 7. The system as designed will be stable as n>n1. [27]

b) Voltage Control Loop (Open-Loop Solutions)

Open and closed-loop solutions will be derived for the converter using the approach in [ref. 27]. The open-loop model is the transfer function up to the control voltage output shown as v_c in Figure 2-7. The closed-loop system connects the v_c output to the comparator and closes the loop to the switch.

Three small-signal open-loop transfer functions are of interest. These are:

1. The control-to-output transfer function, v_{out}/v_c.
2. The line-to-output transfer function (audio susceptibility), v_{out}/v_{in}.
3. The output impedance including the load.

The crossover frequency, ω_c, appears in all poles and is defined as:

$$\omega_c = \frac{\omega_s}{\pi n D'} \tag{2-10}$$

where ω_s is the switching frequency in radians per second and D' is equal to 1-D.
The control-to-output transfer function, A_c, is determined by:

$$A_c = A_{cm} \frac{1}{(1+s/\omega_p)(1+s/\omega_c)} \tag{2-11}$$

where ω_p is determined by:

$$\omega_p = \frac{1}{\left(\frac{\omega_c L}{(1-D)/nD'} \| R_L\right) C} \tag{2-12}$$

and is equal to 50.652 rad/sec or 8 Hz. A_{cm} is determined by:

$$A_{cm} = \frac{\frac{\omega_c L}{1-D/nD'} \| R_L}{R_f} \tag{2-13}$$

where R_f is equal to $R_s N$. Using the values from Chapter II, Section A, A_{cm}=39.17 or 31.85 dB. Substituting Equations (2-10), (2-12), and (2-13) into Equation (2-11) yields:

$$A_c = 39.17 \frac{1}{(1+s/50.652)(1+s/1297.8)} \tag{2-14}$$

The line-to-output transfer function is designated A_g and is determined by:

$$A_g = A_{gm} \frac{1}{(1+s/\omega_p)(1+s/\omega_c)} \tag{2-15}$$

An equivalent expression is $A_g = A_{gm}(A_c/A_{cm})$. A_{gm} is determined from:

$$A_{gm} = \frac{D(1-1/nD')}{\omega_c L}\left(\frac{\omega_c L}{(1-1/nD')} \| R_L\right) \tag{2-16}$$

Substituting actual values into Equation (2-16) results in a value of 0.302, or equivalently, –10.4dB for A_{gm}. Substituting this value into Equation (2-15) yields the line-to-output transfer function, Equation (2-17).

$$A_g = (0.302)\frac{1}{(1+s/50.652)(1+s/1297.8)} \tag{2-17}$$

The output impedance is determined from:

$$Z_o = R_{om}\left(\frac{1}{1+s/\omega_p}\right) \tag{2-18}$$

where R_{om} can be found from:

$$R_{om} = \frac{\omega_c L}{1-(D/nD')} \| R_L \tag{2-19}$$

For this design R_{om} is 8.226Ω. Substituting this value into Equation (2-18) results in:

$$Z_o = 8.226\left(\frac{1}{1+s/\omega_p}\right) \tag{2-20}$$

Figure (2-9) provides a Bode plot of the open-loop transfer functions and the output impedance.

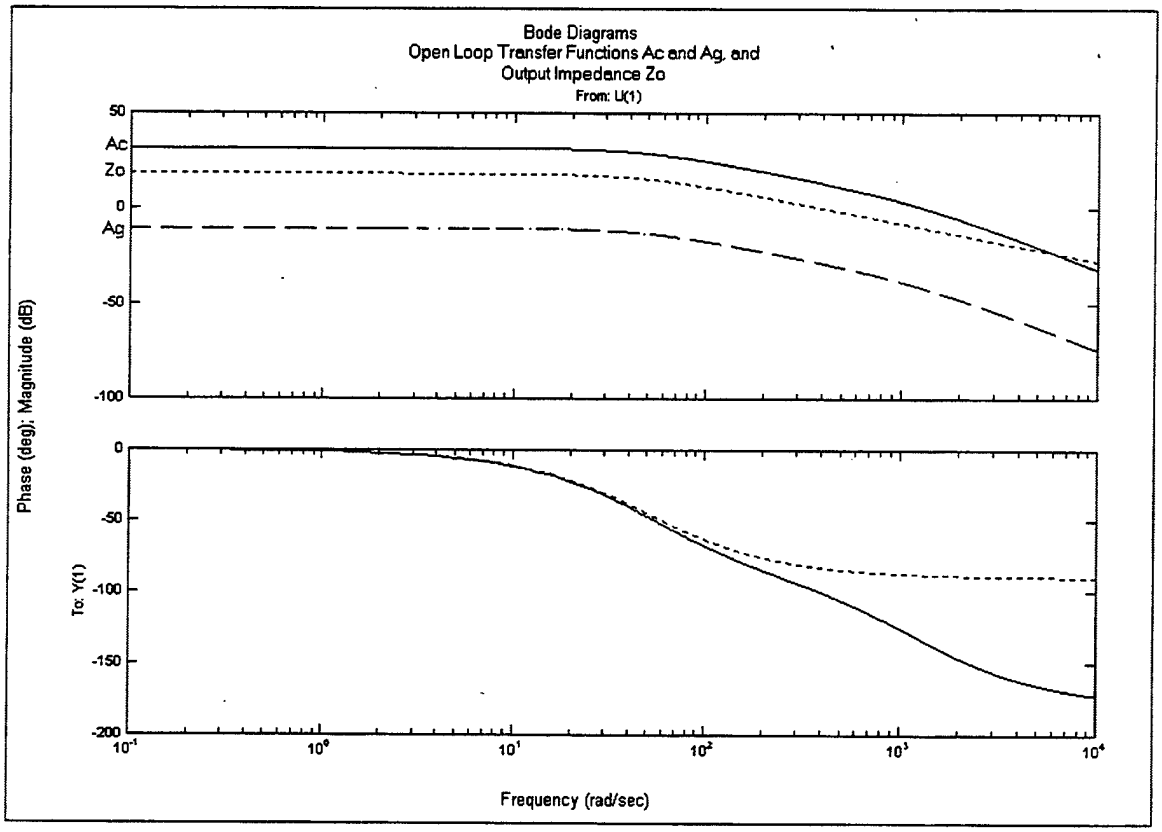

Figure 2-9: Open-Loop Response.

In Figure (2-9), the phase plot of Ag and Ac are identical and show only as a solid line since Equations (2-14) and (2-17) only differ by a scale factor. The open-loop response illustrates stability and a gain margin of greater than 25dB.

c) *Closed-Loop Solution*

Prior to determining the closed-loop transfer functions, the loop gain (T), phase margin (Φ), and feedback factor (1 + T) must be determined. The loop gain is designated T and is given by $T = A_1 A_c$, where A_c is specified from Equation (2-11) and A_1 is the error amplifier gain. The error amplifier gain is determined from Equation (2-21), where ω_1 can be any value but should add only a minimal phase lag at the crossover frequency.

$$A_1 = A_{1m}\left(1 + \frac{\omega_1}{s}\right) \tag{2-21}$$

A diagram of the error amplifier is illustrated in Figure (2-10).

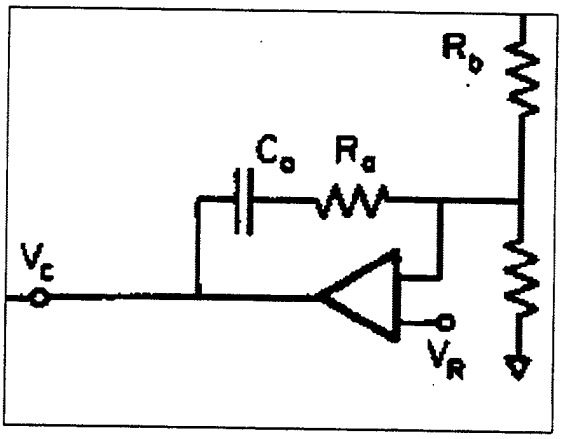

Figure 2-10: Error Amplifier. (from[27])

By suitable selection of ω_1, A_1 can be assumed constant at the switching frequency. T is then simply a vertical scaling of A_c. Therefore, if A_1 is set equal to a constant designated A_{1m}, then A_{1m} determines not only the midband loop gain but also the loop gain crossover frequency. The midband loop gain is given by $T_m = A_{1m}A_{cm}$, where A_{cm} is given by Equation(2-13) . The crossover frequency is given by $\omega_{vc} = T_m\omega_p$, where ω_p is given by

Equation (2-12). To maintain a proper phase margin, ω_{vc} must occur below the pole ω_p. Within that constraint, the pole ω_{vc} should be at as high a frequency as possible for maximum bandwidth. A value of 1005 rad/sec (160Hz) was selected for ω_{vc} to place it below ω_p and maintain an appropriate phase margin. The phase margin was determined from:

$$\Phi = 180 - \left(\tan^{-1}\left(\frac{\omega_{vc}}{\omega_p}\right) + \tan^{-1}\left(\frac{\omega_{vc}}{\omega_c}\right)\right) \qquad (2\text{-}22)$$

The phase margin for this design is 55°.

From the above equation for ω_{vc}, T_m is determined to be 19.86. Using this value, A_{1m} is determined to be 0.6212. As ω_1 is directly related to the RC components used for the error amplifier, ω_1 was chosen based on available components. From Figure (2-10), it is evident that the $A_{1m} = R_a/R_b$. Given $A_{1m} = 0.6212$ as previously determined and selecting $R_b = 100k\Omega$, R_a is determined to be $62k\Omega$. To keep phase lag to a minimum, ω_1 must be as low as feasible. Since ω_1 is related to the capacitor C_a by

$$\omega_1 = \frac{1}{R_a C_a} \qquad (2\text{-}23)$$

a value of 0.56μF was selected for C_a which yielded a value of 28.8 rad/sec (4.58Hz) for ω_1.

The Loop Gain (T) is then determined from:

$$T = T_m \frac{(1+\omega_1/s)}{(1+s/\omega_p)(1+s/\omega_c)} \tag{2-24}$$

where $T_m = A_{1m}A_{cm}$ with $A_{1m} = 0.6212$ as noted above and A_{cm} specified by Equation (2-13). The remaining functions to be determined are the closed-loop output impedance (Z_{of}) and the line-to-output transfer function (A_{gf}). Z_{of} is specified by:

$$Z_{of} = \frac{Z_0}{1+T} \tag{2-25}$$

A_{gf} is specified by:

$$A_{gf} = \frac{A_g}{1+T} \tag{2-26}$$

where A_g and Z_o are the open-loop solutions specified by Equations (2-15) and (2-18) respectively. A factored pole-zero expression for 1+T is found geometrically in Middlebrook (Ref.[27]). This expression is:

$$1+T = (1+T_m)\frac{\left(1+\frac{\omega_1}{s}\right)\left(1+\frac{T_m s}{(1+T_m)\omega_{vc}}\right)}{\left(1+\frac{s}{\omega_p}\right)} \tag{2-27}$$

Substituting Equations (2-18) and (2-27) into Equation (2-25) yields:

$$Z_{of} = R_{ofm}\frac{1}{\left(1+\frac{\omega_1}{s}\right)\left(1+\frac{T_m s}{(1+T_m)\omega_{vc}}\right)} \tag{2-28}$$

where R_{ofm} is specified by:

$$R_{ofm} = \frac{T_m}{1+T_m} \frac{1}{\omega_{vc} C} \tag{2-29}$$

Substituting Equations (2-15) and (2-27) into Equation (2-26) yields:

$$A_{gf} = A_{gfm} \frac{1}{\left(1+\frac{\omega_1}{s}\right)\left(1+\frac{T_m s}{(1+T_m)\omega_{vc}}\right)} \tag{2-30}$$

where A_{gfm} is specified by:

$$A_{gfm} = \frac{T_m}{1+T_m} \frac{A_{gm}}{T_m} \tag{2-31}$$

An alternate expression is:

$$A_{gfm} = \frac{T_m}{1+T_m} \frac{D(1-1/nD')}{\omega_c L} \frac{1}{\omega_{vc} C} \tag{2-32}$$

The candidate system closed-loop Bode plot for A_{gf} and Z_{of} are illustrated in Figure (2-11).

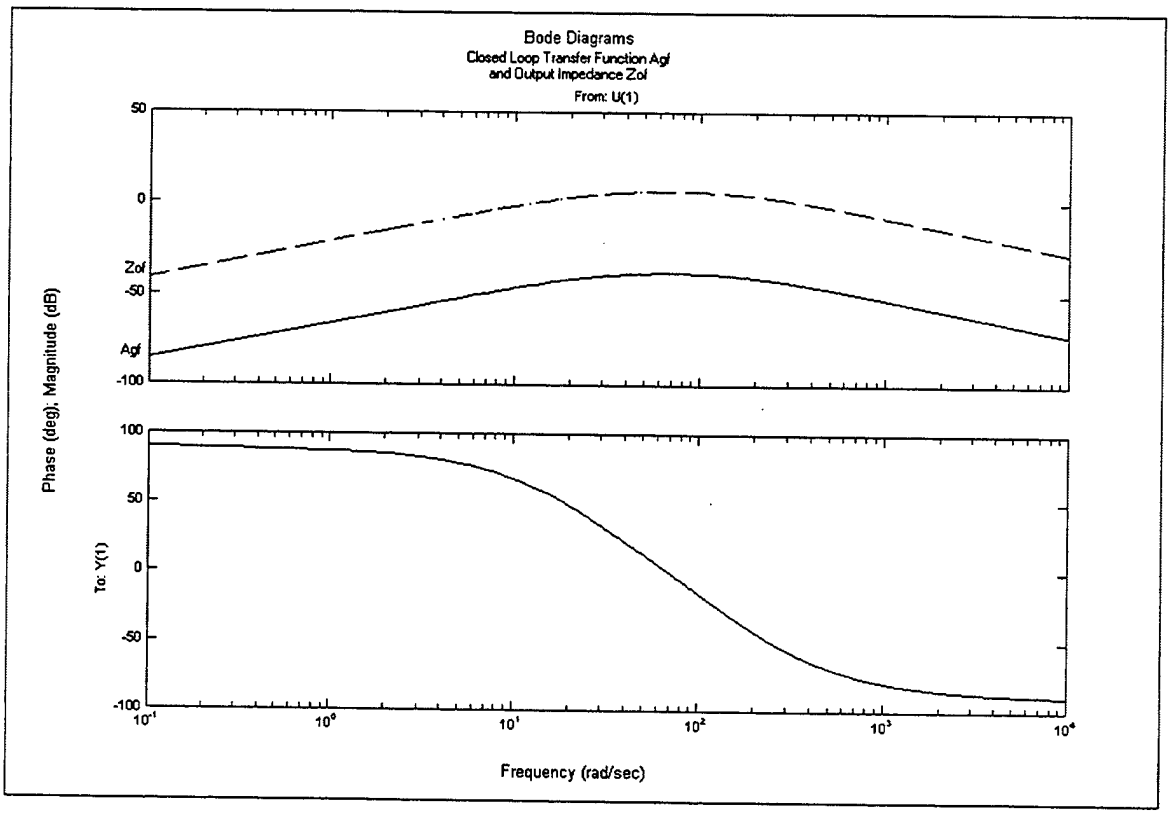

Figure 2-11: Frequency Response of A_{gf} and Z_{of}.

The closed-loop line-to-output transfer function illustrates stability throughout the expected range of operation and indicates the significant damping of any perturbation in the input voltage (-50dB at the frequency of operation). The phase of A_{gf} is coincident with the phase of Z_{of} in the phase plot as required by Equations (2-25) and (2-26). Figure (2-12) illustrates the step response of the closed-loop transfer function A_{gf}. The step response clearly illustrates the significant damping of a perturbation in the line input voltage and illustrates the settling time for this design is approximately 150 msec. [27]

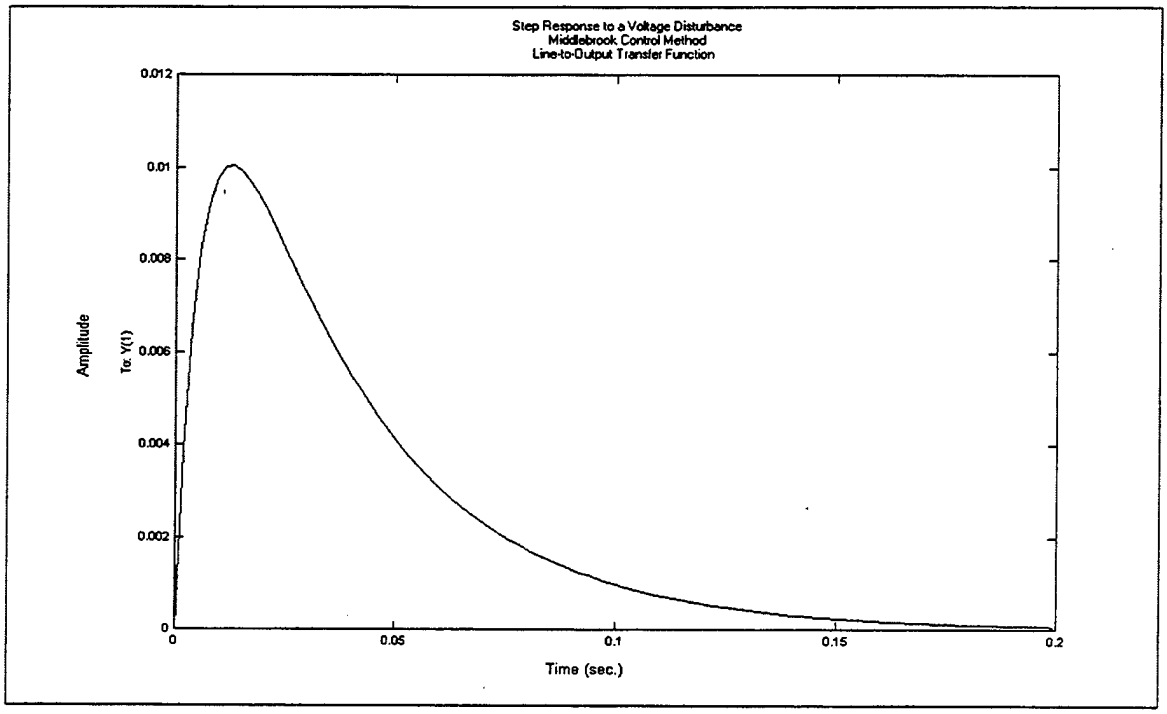

Figure 2-12: Middlebrook Closed-Loop Step Response.

D. UNITRODE UC3846 CURRENT-MODE PWM CONTROLLER

UNITRODE Corporation produces a current-mode control integrated circuit designated UC1846. The model 3846 is the MILSPEC variant of the 1846 chip. A block diagram of the UC3846 chip is included in Appendix E. The UC3846 chip was investigated as a candidate control implementation and was also used to provide synchronous clock and stabilizing ramp inputs for the other two control realizations.

The circuit provides for two feedback loops. The outer voltage control loop consists of an output voltage sensor and an error amplifier; the inner or current control loop consists of a current sensing resistor and a current sense amplifier. [28] The output of the error amplifier and the current sense amplifier are then compared to produce a commanded duty cycle signal output. The voltage error amplifier provides the control signal (I^*) previously discussed in Section B of this chapter. The current sense amplifier

provides the inductor current value (I_L) previously discussed in the same section. The comparator output serves as the S input to an RS latch.

The current sense amplifier is connected to pin 3 (negative) and pin 4 (positive). The maximum allowable differential voltage between the pins is 1.2 volts. [29] Current must be sensed by resistive sensing unless any perturbations in the sensed current waveform due to the magnetizing current of a transformer are accounted for. [27] A 25mΩ resistor was used to sense inductor current. A small RC filter is required across pins 3 and 4 to reduce switch transients which may be sufficient to trip the RS latch. A resistor placed in series with the pin 4 input and a 100nF capacitor across pins 3 and 4 should suffice.

Switching period control is provided by an oscillator. The oscillator frequency is determined by a resistor placed from pin 9 to ground and a capacitor placed from pin 8 to ground. A 24kΩ resistor and 47nF capacitor were used to produce a 2kHz oscillation. [29] The output on pin 8 is a 2kHz ramp which will provide the stabilizing slope compensation signal for operation above 50 percent duty-cycle. How this is accomplished is discussed later in this section. The ramp signal produced using the 24kΩ resistor and the 47nF capacitor is a 1.904kHz signal with a peak-to-peak voltage of 1.73V and centered at +2.2V. The oscillator also provides a clock pulse output at pin 10 which can be used to synchronize other UC3846 chips operating in parallel. In this design, the clock pulse is a 1.904kHz signal with a clock on-time pulse width of 11.6μs. The clock signal exhibits a +2.2V DC bias. To operate the UC3846 in parallel, one chip serves as the master while others act as slaves. The master provides an output pulse on pin 10 which then serves as the input to pin 10 on the slave. Pin 9 of the slave must be connected to pin 2 which is the 5.1V output of the internal voltage regulator. An illustration of this parallel configuration is included in Appendix E.

Slope compensation was implemented by connecting pin 8 to pin 4. This added the compensating slope to the measured inductor current. This is the opposite of what

was done with the other two methods of control but is equally effective. [28] The resistor values used to make this connection are given by:

$$\frac{R_1}{R_1 + R_2} = \frac{R_s (m_2 / 2)}{\Delta V / \Delta t} \tag{2-33}$$

In Equation (2-33), adapted from reference [28], m_2 is the magnitude of the slope of I_L during the switch off time and is equal to v_{out}/L. R_s is the current sensing resistor and is equal to 25mΩ. R_1 is connected in series between the high side of R_s and pin 4. This resistor also serves as part of the RC filter between pins 3 and 4 described above. R_2 is connected between pins 4 and 8. R_1 is 20kΩ and R_2 is 390kΩ. The denominator value $\Delta V/\Delta t$ is equal to $1.8/[(0.45)R_tC_t]$ where R_t and C_t are the resistor and capacitor connected to pins 9 and 8 respectively (24kΩ and 47nF in this case). Figure (2-13) illustrates this configuration.

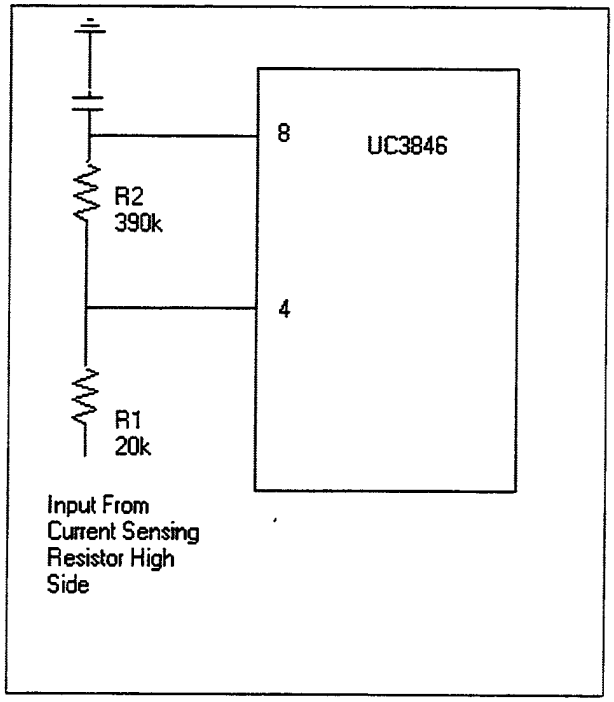

Figure 2-13: Slope Compensation for the UC3846. (From Ref. [28])

The input for the control signal reference voltage is pin 5, the non-inverting input to the error amplifier. The reference voltage is a constant 1.5 volts derived from the internal voltage regulator output, pin 2. Pin 2 is a 5.1 volt output which is reduced by a voltage divider to the correct value of 1.5V. Pin 2 is also connected to pin 1, the current limit input. This forces pin 1 high to the point that current limiting is not a factor. Current limiting schemes are discussed in ref. [29]. The measured converter output voltage is input to pin 6, the inverting input to the error amplifier, via a 100:1 isolation transformer. pin 7 is used to close the negative feedback loop of the error amplifier.

The remaining pins are for output and power. Pin 15 is the input voltage and can range from 8V to 40V. A nominal 15V was used in this project. Pin 12 is the ground pin. Pin 13 is the output transistor collector voltage and is supplied by the input voltage (15V) through a 180Ω resistor. Pin 16 is the shutdown circuit input and is grounded as shutdown capability is not employed. If a shutdown and re-start scheme is employed, the shutdown circuit will activate whenever 350mV is applied to pin 16. Pins 11 and 14 are the output pins and provide a pulse output of suitable frequency and duty-cycle. The control output pulse is a square pulse of 14.3V amplitude, in this case. The output amplitude is dependent on the input voltage which can be from +8V to +40V. Additional features such as peak current limiting and shutdown/re-start were not used in this project but are included in the data sheet in Appendix E and reference [29].

Using the UC3846 chip as a source for clock pulses and the stabilizing ramp for use in other analog control designs presented several problems. As noted above, both pin 10 and pin 8 outputs exhibit a DC bias. The ramp exhibited a bias of +1.2V from ground to the minimum value of the ramp signal and +2.2V to the center of the ramp. The clock output exhibited a bias of 2.2V from ground to the bottom of the clock pulse signal. This bias was eliminated using small capacitors in series. The pin 8 ramp output was then centered about zero volts. The ramp had to be scaled to the application and then biased such that it originated at zero and was always greater than zero. In this project, the slope compensation was subtracted from the control signal prior to the comparator. To

accomplish this in the Middlebrook and classical design approaches, the control voltage was inverted to produce a negative value and then summed with a positive-sloped ramp originating at zero volts. This output was then inverted to produce the desired control voltage signal. The oscillator output also exhibited a DC bias and the magnitude of the pulse was insufficient to drive TTL devices such as flip-flops or NAND gates which would be used to implement the final stage of control prior to the switch. A non-inverting gain was required to boost the pulse up to between 4 and 5 volts. Oscilloscope plots of ramp and clock signals are included in Appendix E as Figures (E-1) and (E-2).

In operation, the oscillator clock pulse resets the RS flip-flop at the beginning of each cycle forcing the flip-flop output to low. When the output of the current sense amplifier equals the output of the voltage of the error amplifier, the comparator output goes from low to high. This in turn forces the output of the RS flip-flop to high. The RS flip-flop output is alternately steered by a T flip-flop through two separate 3-input OR gates. The result is that one output transistor is high whenever the RS flip-flop output is low. Therefore, with reference to the schematic included in the data sheet in Appendix E, output A is high at the start of each clock pulse and switches low when the current sense amplifier output is greater than the control voltage signal which is the output of the voltage error amplifier. The T flip-flop causes the two output waveforms, pins 11 and 14, to be 180 degrees out of phase. [28]

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III. MATHEMATICAL MODEL DEVELOPMENT

A. DERIVATION OF THE CONTROL EQUATION

The control objective when utilizing current-mode control is to match the commanded current and the average inductor current. An example of this is illustrated in Figure (3-1).

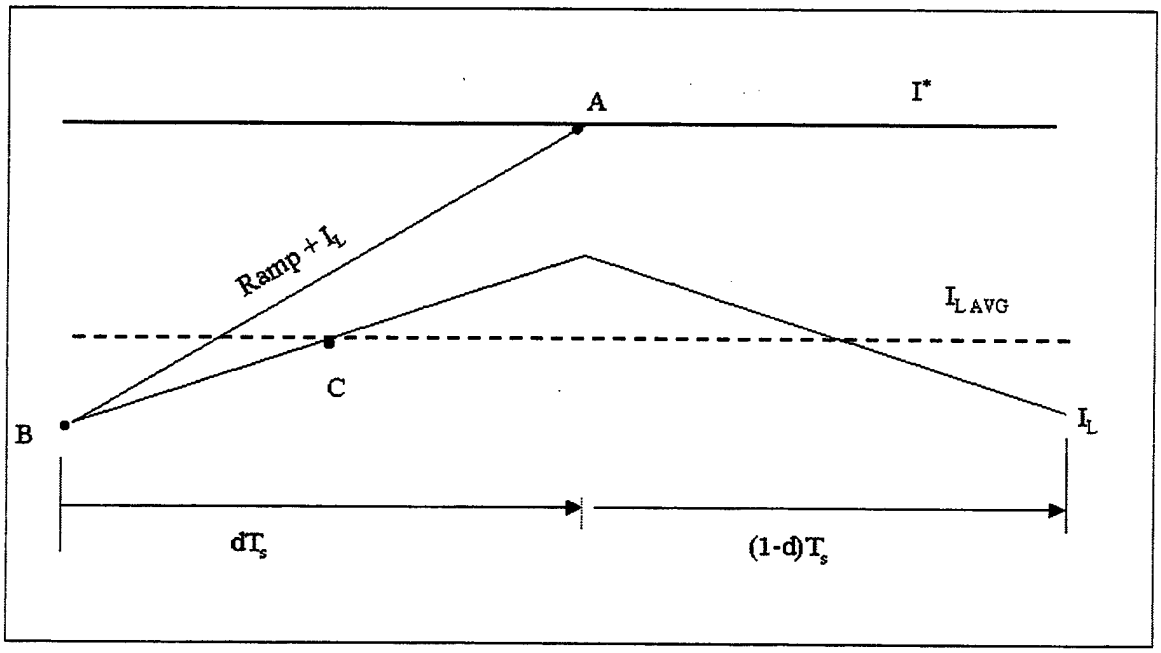

Figure 3-1: Current-Mode Control Derivation Diagram.

In Figure (3-1), dT_s represents the switch duty cycle or the on-time of the switch. The switch off time is represented by $(1-d)T_s$. $I_{L\,AVG}$ represents the average inductor current and I^* represents the desired inductor current. The (Ramp + I_L) line represents the I_L waveform plus the slope compensation ramp discussed previously. The slope of I_L during the switch closed period is given by $(V_{in} - V_{out})/L$. The slope of I_L during the switch open period is given by $-V_{out}/L$. Setting the ramp slope equal to the V_{out}/L and designating this value m, the value of I_L at point B of Figure 3-1 is given by:

$$i_B = I^* - \left[\frac{v_{in} - v_{out}}{L} + m\right] dT_s \tag{3-1}$$

The lower case designation indicates the combined large and small-signal current. Similarly, for point C, midway in the dTs interval, the equation is:

$$i_C = i_{LAVG} = i_B + \left[\frac{v_{in} - v_{out}}{L}\right] \frac{dT_s}{2} \tag{3-2}$$

Substituting for i_B and setting $m=V_{out}/L$ yields:

$$i_{LAVG} = I^* - \left[\frac{v_{in} + v_{out}}{2L}\right] dT_s \tag{3-3}$$

Setting V_{out} (steady-state) equal to V_{ref}, D_{ss} equal to V_{ref}/V_{in} equal to d_o, and linearizing yields:

$$\Delta i_{LAVG} = \Delta I^* - \left(\frac{v_{in} T_s}{2L}\right) \Delta d - \left(\frac{v_{ref} T_s}{2L}\right) \Delta d - \left(\frac{T_s d_o}{2L}\right) \Delta v_{out} \tag{3-4}$$

Solving for Δd yields:

$$\Delta d = \left(\frac{2L}{(v_{in} + v_{ref}) T_s}\right) \Delta I^* - \left(\frac{2L}{(v_{in} + v_{ref}) T_s}\right) \Delta i_{LAVG} - \left(\frac{v_{ref}}{(v_{in} + v_{ref}) v_{in}}\right) \Delta v_{out} \tag{3-5}$$

The open-loop representation of the system can be found by merging Equation (3-5) with the differential equations describing the buck converter specified in Fisher, Ref. [22], and provided in Equations (3-6) and (3-7).

$$\frac{d}{dt}v_{out\,AVG} = \frac{1}{C}i_{L\,AVG} - \frac{1}{RC}v_{out\,AVG} \tag{3-6}$$

$$\frac{d}{dt}i_{L\,AVG} = \frac{1}{L}d(v_{in}) - \frac{1}{L}v_{out\,AVG} \tag{3-7}$$

The d term on the right-hand side of Equation (3-7) refers to the combined small and large components of the duty cycle. The open-loop state-space representation is:

$$\frac{d}{dt}\begin{bmatrix}\Delta v_{outAVG}\\ \Delta i_{LAVG}\end{bmatrix} = \begin{bmatrix}-\frac{1}{RC} & \frac{1}{C}\\ -\frac{1}{L} - \frac{v_{ref}}{(v_{in}+v_{ref})L} & \frac{-2v_{in}}{(v_{in}+v_{ref})T_s}\end{bmatrix}\begin{bmatrix}\Delta v_{outAVG}\\ \Delta i_{LAVG}\end{bmatrix} + \begin{bmatrix}0\\ \frac{2v_{in}}{(v_{in}+v_{ref})T_s}\end{bmatrix}I^* \tag{3-8}$$

B. CLOSED-LOOP REPRESENTATION

The closed-loop solution is derived by merging the open-loop solution with the voltage control loop. The voltage control loop flow diagram is illustrated in Figure 3-2. The linearized control equation for the voltage control loop is:

$$\Delta I^* = ki\,\Delta x + kp(\Delta v_{ref} - \Delta v_{out}) \tag{3-9}$$

with $v_{ref} - v_{out}$ defined as:

$$\frac{d}{dt}x = v_{ref} - v_{out} \tag{3-10}$$

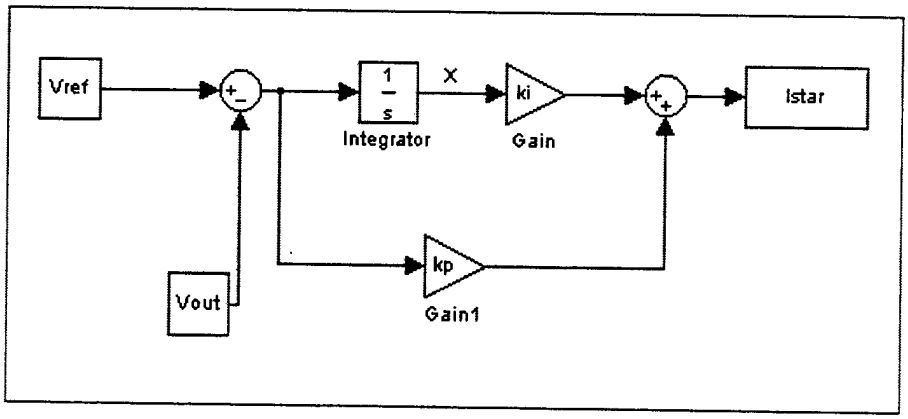

Figure 3-2: Voltage Control Loop.

Equations (3-8, 3-9, and 3-10) are combined to yield the following result.

$$\frac{d}{dt}\begin{bmatrix} \Delta v_{out_{AVG}} \\ \Delta i_{L_{AVG}} \\ \Delta x \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} & -\frac{1/RC}{(v_{in}+v_{ref})L} & -\frac{2v_{in}k_p}{(v_{in}+v_{ref})T_s} \\ & -1 & \end{bmatrix} \begin{bmatrix} \frac{1/C}{-2v_{in}} & \frac{0}{2v_{in}k_i} \\ \frac{}{(v_{in}+v_{ref})T_s} & \frac{}{(v_{in}+v_{ref})T_s} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta v_{out_{AVG}} \\ \Delta i_{L_{AVG}} \\ \Delta x \end{bmatrix} \tag{3-11}$$

$$+ \begin{bmatrix} 0 \\ \frac{2v_{in}k_p}{(v_{in}+v_{ref})T_s} \\ 1 \end{bmatrix} \begin{bmatrix} \Delta v_{ref} \end{bmatrix}$$

C. DETERMINATION OF GAINS AND POLE SELECTION

The square matrix of Equation (3-11) is the system matrix. The gains k_p and k_i are determined from the desired eigenvalues of the system matrix. The eigenvalues, denoted by λ, are the roots of the characteristic polynomial specified by the determinant $|\mathbf{A}-\lambda\mathbf{I}|$. Substituting the values for R, L, C, T_s, Vin, and V_{ref} specified in Chapter II into Equation (3-11) and using MATHCAD to solve the determinant, the characteristic polynomial was found to be:

$$-\lambda^3 - \lambda^2(2257.944) - \lambda(952381.595k_p + 119523.073) - 952381.595k_i \quad (3\text{-}12)$$

The Bessel prototype pole locations for n = 3 and ω_o = 1 rad/sec were used as a starting point for solving for the gains of Equation (3-12). The Bessel poles for n=3 are (-0.9420), and (-0.7445 ± j0.7112). The characteristic polynomial given by these roots is:

$$\lambda^3 + \lambda^2 2.4310 + \lambda 2.4627 + 0.9986 \quad (3\text{-}13)$$

Equation (3-13), being the characteristic polynomial for ω_o = 1 rad/sec (yielding a settling time of approximately 9 seconds), had to be scaled to match the system of Equation (3-12). Since the second-order term (λ^2 coefficient) of Equation (3-12) is not a function of k_p or k_i, the second-order term of Equation (3-13) was multiplied by a scaling factor of 928.8128 to match the second-order term of Equation (3-12). Once the equations are matched, k_i and k_p are easily determined by direct comparison of the remaining polynomial coefficients. The integral gain k_i was found to be 840.167 and the proportional gain k_p was found to be 2.105. These gains resulted in initial system poles of (-874.94) and (-691.5 ± j660.5).

Following computer simulation and evaluation of step response, the integral and proportional gains were adjusted to $k_i = 902.74$ and $k_p = 2.216$. These gain values yielded system poles at (-816.6), and (-720.6 ± 730.7) . This pole selection results in a theoretical settling time of 9.7msec.

IV. DYNAMIC SIMULATION

A. COMMENTS ON THE SIMULATION

The simulation of the two algorithms was straightforward. Model one is the classical control implementation derived in Chapter III; model two is the Middlebrook based implementation. The only significant point was the requirement to handle large starting transients that were observed in the initial studies. These transients were eliminated by exponentially ramping the control reference voltage v_{ref}. This was accomplished using the following equation:

$$v_{ref} = 150 - 150e^{(-t/tau)} \tag{4-1}$$

For model one, tau is 25.0. For model two, tau is 15.0. The time for the reference voltage to rise to within 1V of the specified value of 150V is 0.2 seconds for model one and 0.334 seconds for model 2.

B. RESULTS

Figure (4-1) illustrates the response of ACSL model 1 to start-up and a 50 percent step reduction in the output power brought about by an increase in load resistance. The inductor current indicates that the start up oscillations do not exceed 11 Amps and the peak overshoot is on the order of 13 Amps. Both of these phenomena are easily managed with existing power devices. The plots illustrate that output voltage and current both stabilize within the limits specified in Chapter II. Voltage oscillations are minimal during start-up.

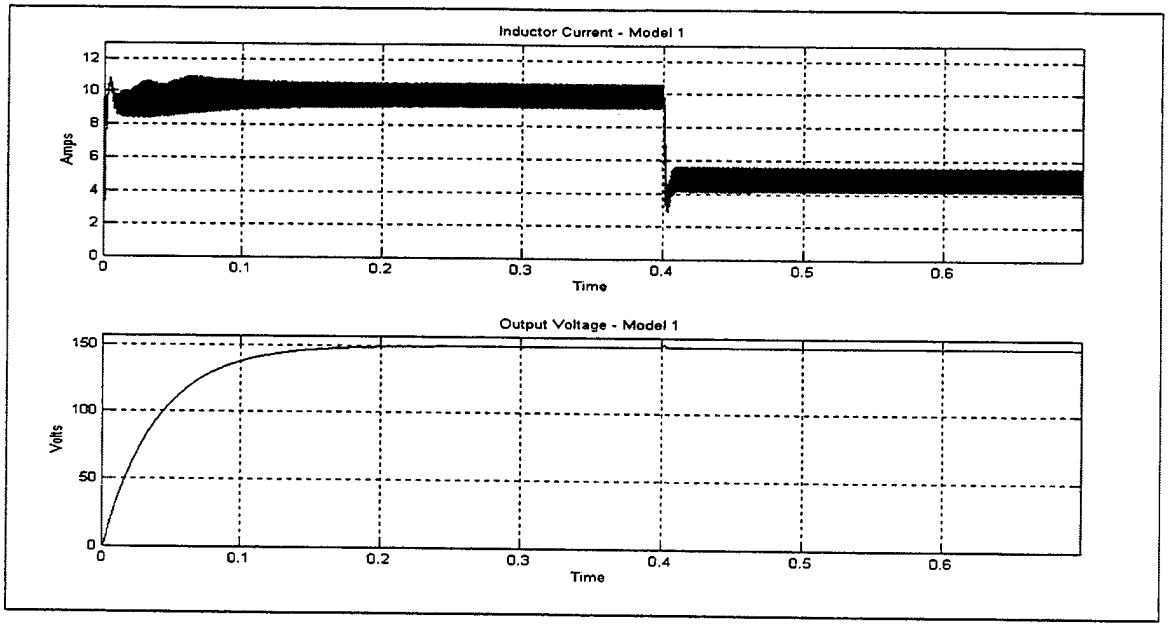

Figure 4-1: Start-up and Step Response for ACSL Model 1.

Figure (4-2) illustrates the initial start-up response of model one. Of note is the initial overshoot which is well within normally acceptable limits and the oscillations which occur out to 0.1 second. The output voltage stabilizes at 0.2 seconds, this is a function of the decaying exponential of the reference waveform as it approaches the steady-state value of 150 volts as discussed above.

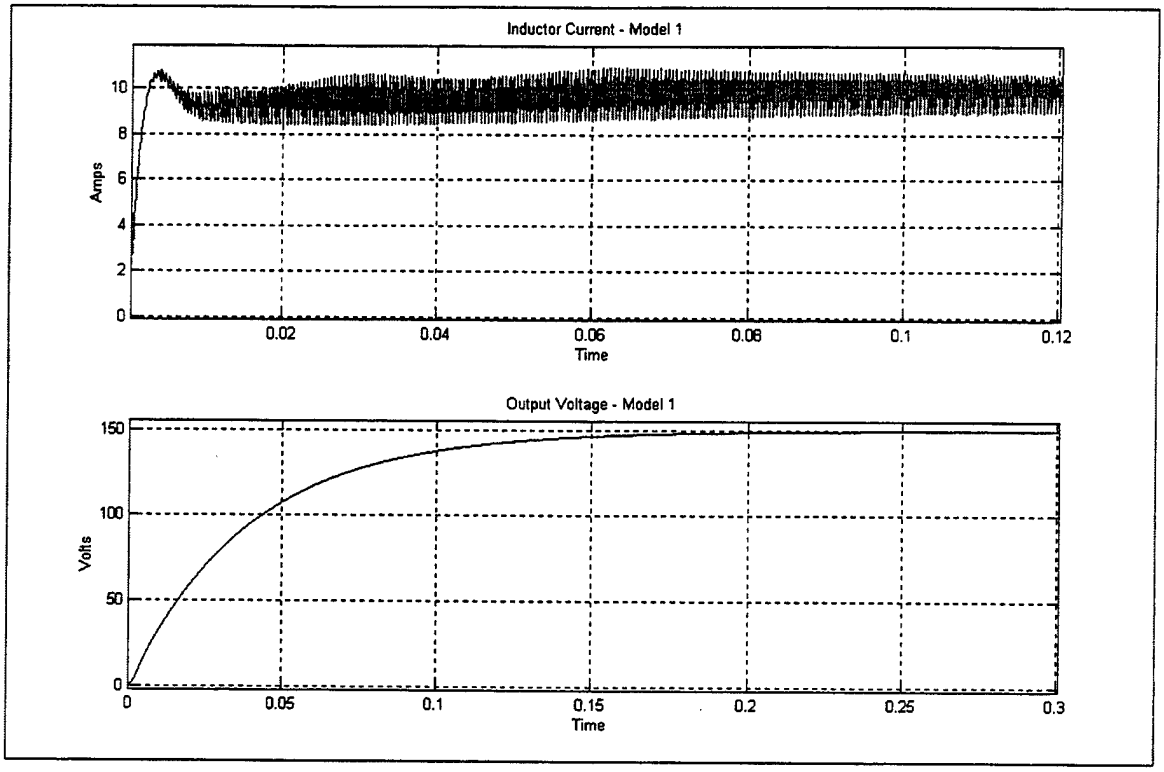

Figure 4-2: Start-Up Transient Response for ACSL Model 1.

Figure (4-3) illustrates a step response to a change from 100 percent power to 50 percent power. The figure shows no oscillations in voltage or current response. Current settles in under 8msec which is below the expected settling time of 9.7msec. Output voltage settles in under 7msec. The current overshoot is approximately 40 percent of the new steady-state value which, while high, is acceptable for this application. The voltage perturbation is less than two volts or 1.33 percent which is well within accepted limits.

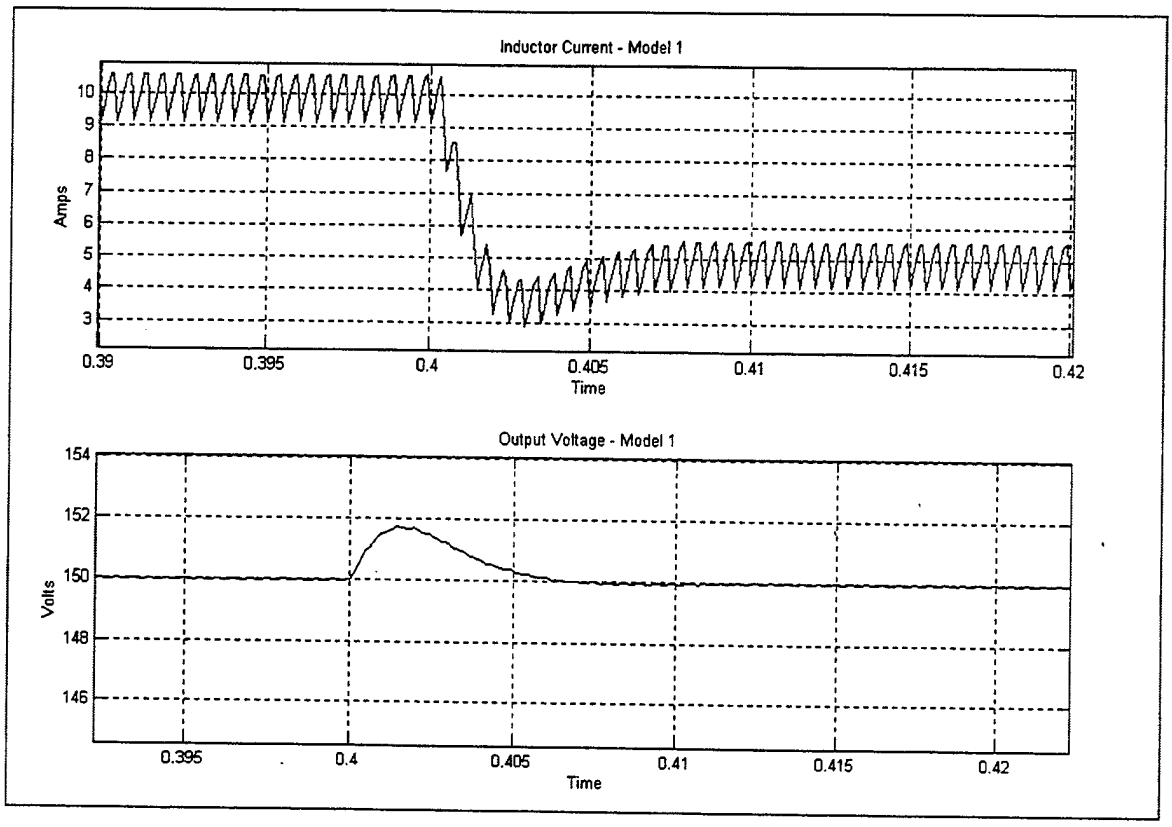

Figure 4-3: Step Response for Model 1.

Figure (4-4) illustrates the steady-state output voltage waveform for the converter of model 1. In addition to the 2kHz oscillation resulting from switching, there is a periodic variation in the output at a period of approximately 5msec. This 200 Hz variation is induced by the complex poles of the controller ($\pm j730.7$). The peak-to-peak amplitude of the sum of the variation is less than 50mV which is well within the specifications listed Chapter II.

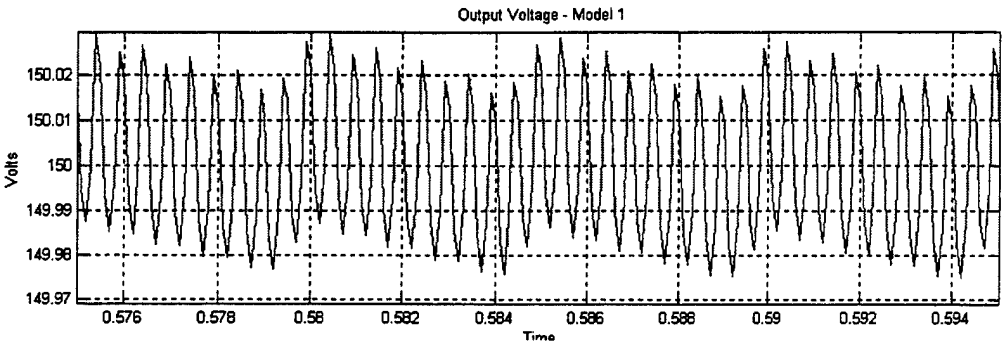

Figure 4-4: Steady-State Voltage Output for Model One.

Figures (4-5) and (4-6) illustrate the response of model one to two step changes in load. The study includes a 50 percent decrease in power as before and then a return to full power.

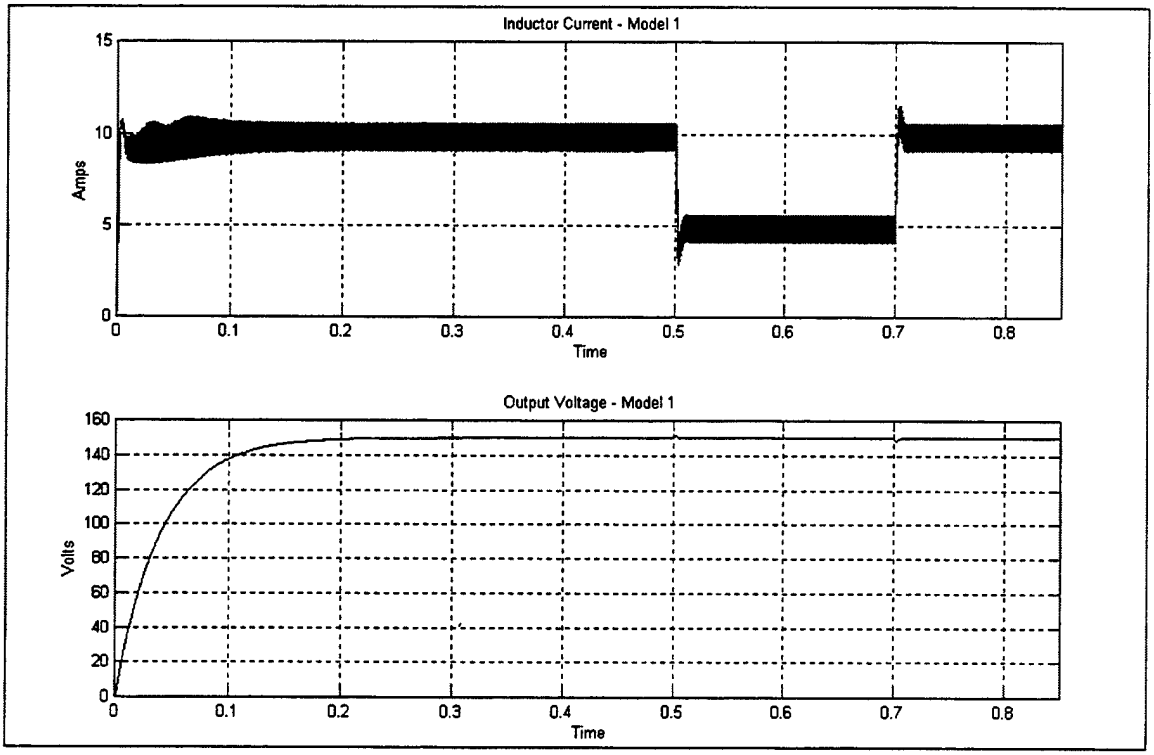

Figure 4-5: Model 1 Response for Two Step Changes in Load.

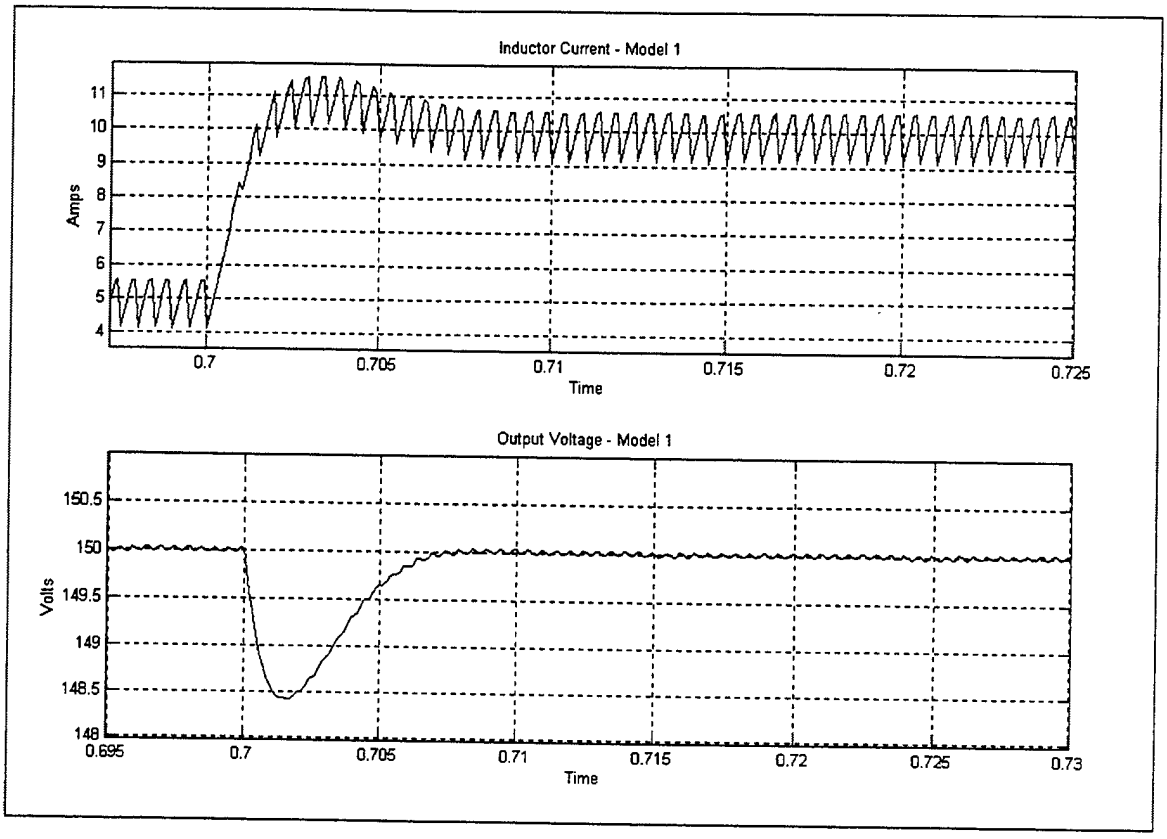

Figure 4-6: Model 1 Response to Step Increase in Load.

Figure (4-6) illustrates the response to a step increase in load power following the step decrease in power. Output voltage settling time is less than 7msec and the perturbation to the output voltage is less than 2 volts.

The response of the Middldlebrook control design, ACSL model two, is illustrated in Figures (4-7) through (4-11). As with model one the response to initial start-up, a step decrease and increase in load power, and two successive step changes are illustrated.

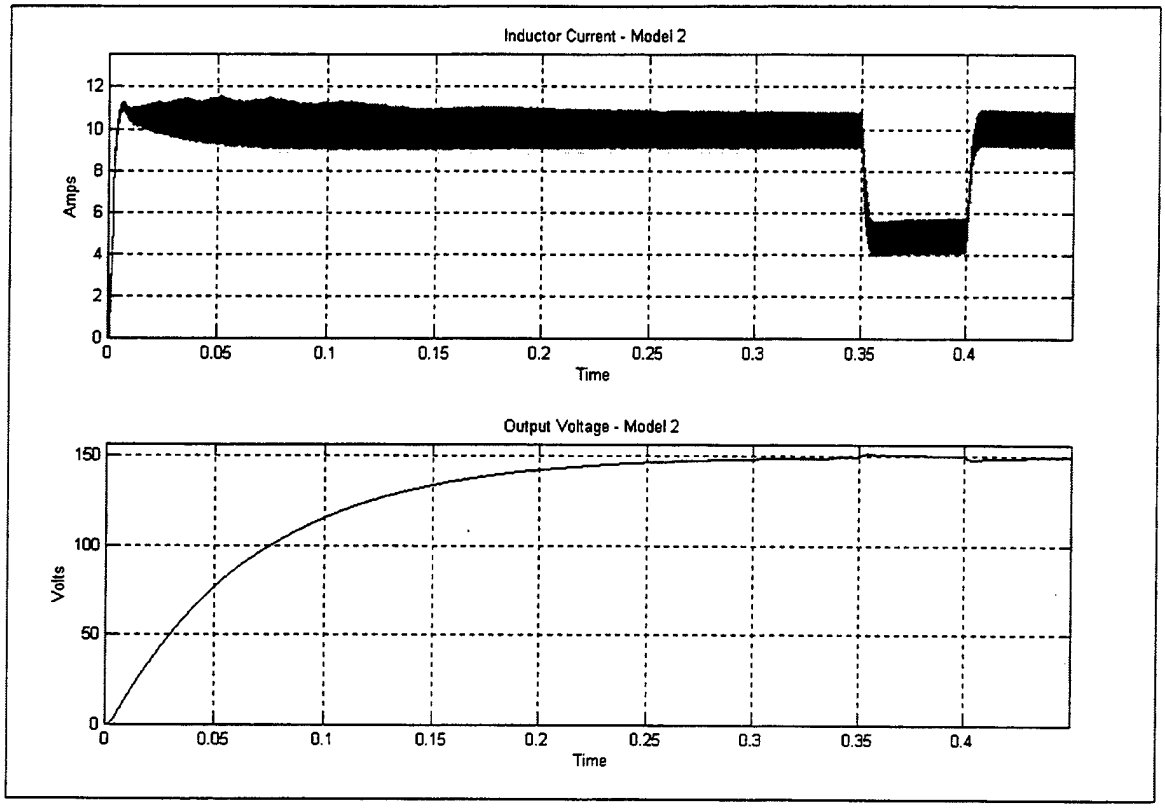

Figure 4-7: Model 2 Start-Up and Two Step Changes in Load Power.

The most noticeable difference between model one and model two is that the model two output voltage approaches 150V asymptotically and never settles at 150V during the observation period. The output voltage reaches the minimum value of 149 in 0.335 seconds and remains within the lower half of the ±1 volt criteria throughout. The initial transient current overshoot is less, 11.5A verses 13A for model one, and is illustrated in Figure (4-8).

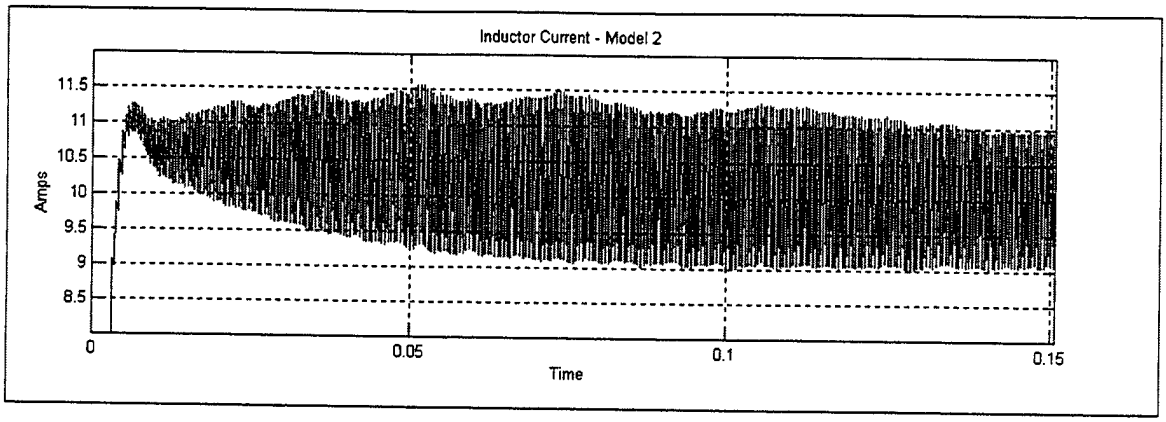

Figure 4-8: Model 2 I_L Initial Start-Up Response.

The simulated inductor current settling time following a step change for model 2 design is 7msec, identical to the settling time of the inductor current for model one. The output voltage settling time for model two is 0.25 second which is significantly greater than the model one output voltage settling time of 7 msec. This is illustrated in Figure (4-9) and Figure (4-10).

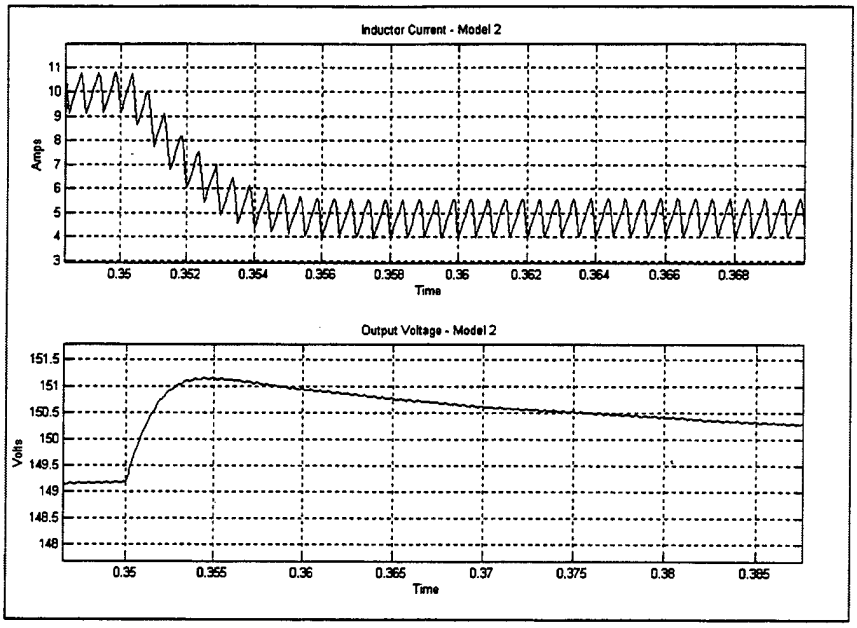

Figure 4-9: Model 2 Response to a Step Decrease in Load Power.

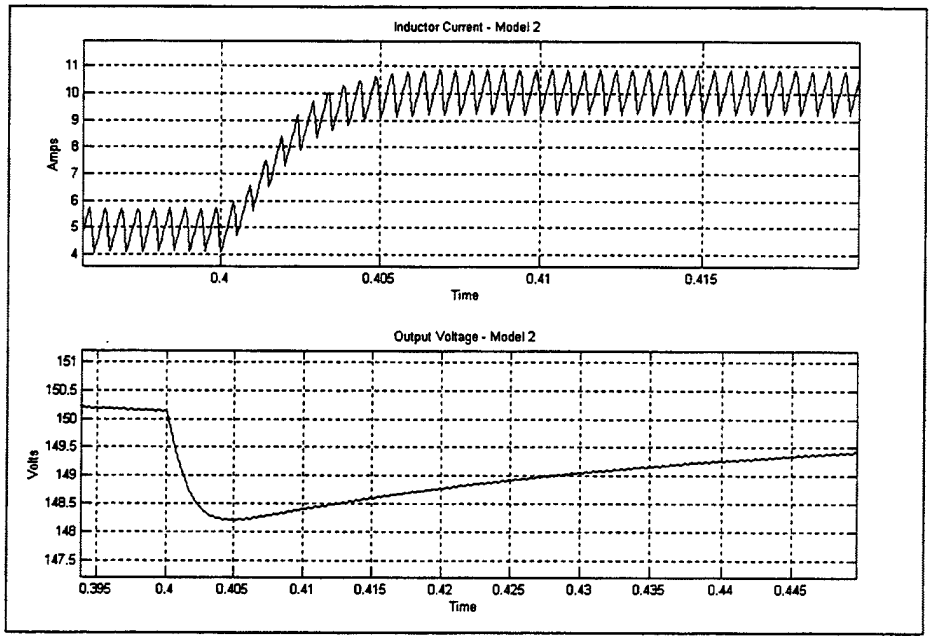

Figure 4-10: Model 2 Response to a Step Increase in Load Power.

The model two output voltage following the second step change is illustrated in Figure (4-11). The waveform clearly depicts the asymptotic approach to 150 volts and the 2kHz oscillation resulting from the switching frequency.

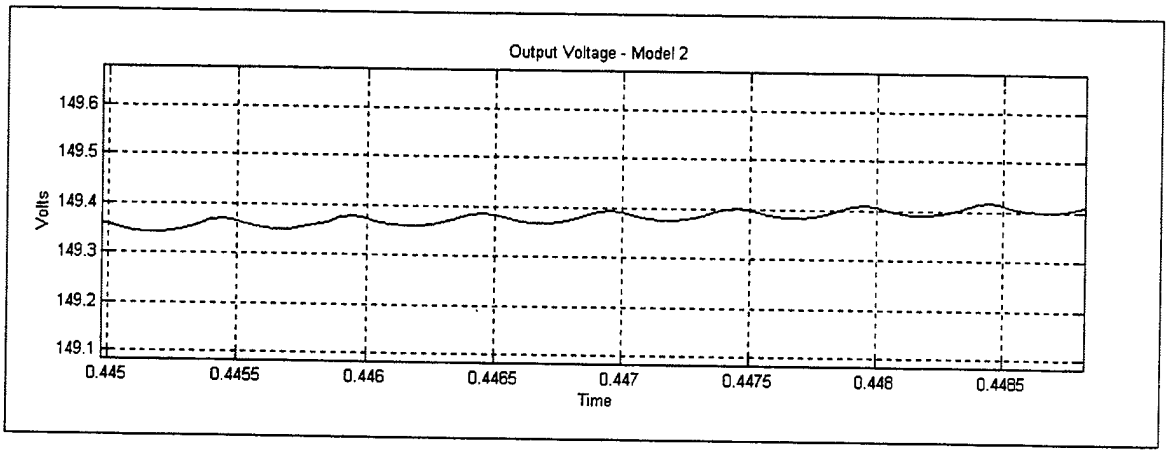

Figure 4-11: Model 2 Output Voltage.

V. CONCLUSIONS

A. SUMMARY OF FINDINGS

A background search for applicable literature was performed. In addition to the references cited in the text of this thesis, references [30] through [40] were reviewed for background material and educational benefit. Two ACSL simulation models were developed, a state-space representation was derived for model one, various transfer functions were derived and examined for model two, gains were analytically determined, and the simulations exercised for start-up, steady-state, and load transient conditions.

Current-mode control does result in an improvement in responsiveness over voltage-mode control. Further, current-mode control requires fewer components and is simpler to implement with hardware. The classical control method produced superior results in simulation. Both methods exhibited a 0.7ms settling time for inductor current, but the classical method exhibited an improvement in output voltage settling time of an order of magnitude. Therefore, the classical method is the recommended method for laboratory implementation of current-mode control.

The Middlebrook control and the UC3846 control were constructed and tested in the laboratory. Neither produced satisfactory operation of the buck converter. The Middlebrook control requires a means of ensuring that the switching will occur only once in a 2kHz cycle. This requires some method of combinational logic. Several methods were attempted, a D flip-flop, a RS flip-flop, and a JK flip-flop, all without success. Both control implementations require a method of isolating the high voltage present at either side of the current sensing resistor from the controller without introducing a perturbation to the current waveform.

The UC3846 PWM controller did not produce an operational controller either. The applicable documentation does not support a direct implementation of this chip as a controller for a buck converter. Most significant is the lack of any documentation

supporting the error amplifier function of the chip and determination of required gains or any required scaling. The UC3846 chip was one of the first integrated current-mode control chips and has primarily been used in low voltage applications and push-pull configurations. The UC3846 has since been surpassed by improved current-mode PWM control chips. This chip is not recommended for laboratory implementation of current-mode control; however, a more recent current-mode control chip may be worth evaluating.

B. FUTURE WORK

The United States Navy is currently pursuing an Integrated Power System which will employ zonal distribution. For reasons of ship survivability, DC zonal distribution will be the most likely power distribution architecture. The recent establishment of an IPS program office underlines the importance of IPS as a centerpiece of future combatant designs. High-voltage DC-DC converters are an integral part of any DC distribution system and thus far current-mode control has received little attention with regard to a shipboard IPS. This thesis provides a preliminary look at current-mode control modeling, simulation, and hardware design.

Possible topics for future work in the area of DCZEDS include:

1. Develop a working hardware prototype to implement current-mode control using the Middlebrook model and integrated circuit approach.
2. The digital implementation of a current-mode control algorithm for single and parallel high voltage buck converters using the dSPACE hardware-in-the-loop development package.
3. Implementation of current-mode control in soft-switching converters and performance comparison to voltage-mode control of soft-switching converters.
4. Modeling and simulation of permanent magnet motors and their associated control systems in ACSL.

APPENDIX A: MATLAB CODE

A. MODEL ONE CLOSED-LOOP RESPONSE

```
r=15;
l=10.62e-3;
c=2.4e-3;
Vdc=200;
Vref=150;
T=1/2000;
z=Vdc+Vref;
kp=2.216;ki=902.74;
A=[-1/(r*c) 1/c 0;((-1/l)-(Vref/(z*l))-(2*Vdc*kp/(z*T))) -
2*Vdc/(z*T) (2*Vdc*ki/(z*T));-1 0 1];
B=[0;(2*Vdc*kp)/(z*T);1];
C=[1 0 0];
D=0;
sys=ss(A,B,C,D);
figure(1)
bode(sys)
figure(2)
step(sys)
```

B. MODEL TWO OPEN AND CLOSED-LOOP RESPONSE (MIDDLEBROOK CALCULATIONS)

```
%Current Mode Control, Buck Converter
%200-150 Volts  1.5kW

%Open Loop Gains, Ac,Ag, and Line Impedance Zo
%Ac
wp=50.652;
wc=1297.8;
acm=39.17;
numac=[acm];
denac=conv([1/wp 1],[1/wc 1]);
sysac=tf(numac,denac);
```

```
%Ag
agm=.302;
numag=[agm];
denag=conv([1/wp 1],[1/wc 1]);
sysag=tf(numag,denag);

%Zo
rom=8.226;
numzo=[rom];
denzo=[1/wp 1];
syszo=tf(numzo,denzo);

w=linspace(.1,10000,10000);
figure(1)
bode(sysac,'-',sysag,'--',syszo,':',w)

wvc=160;
w1=28.8;
tm=19.86;
c=2.4*1e-3;

%Line to Output Impedance Closed Loop
Rofm=(tm/(1+tm))*1/(wvc*c);
numzf=[Rofm 0];
denzf=conv([1 w1],[tm/((tm+1)*wvc) 1]);
syszf=tf(numzf,denzf);

%Line to Output Voltage Closed Loop
Agf=(tm/(1+tm))*agm/tm;
numagf=[Agf 0];
denagf=denzf;
sysagf=tf(numagf,denagf);

figure(2)
bode(sysagf,'-',syszf,'--',w)
```

APPENDIX B: ACSL CODE

A. MODEL ONE

1. .CSL File

```
!  T. Hekman
!  Filename: cmc1.csl

!  Single converter -- CURRENT MODE
!  Features:
!     *  continuous or discontinuous conduction mode operation
!     *  purely resistive load
!     *  closed loop control algorithm
!  Control algorithm:
!        i1ref = hn*x + hv*(Vref - vC)
!        dx/dt = Vref - vC

PROGRAM

INITIAL

!  Simulation Parameters "
MAXTERVAL  maxt = 1e-5  !"max step for var step integration algorithm"
   MINTERVAL  mint = 1e-6 !"min step for var step integration algorithm"
   CINTERVAL  cint = .5e-4       !" data communication interval "
   ALGORITHM  ialg = 5          !" 4 -> RK 2nd, 5 -> RK 4th "
   NSTEPS     nstp = 1
   CONSTANT   tstop = 0.01      !" stop point for integration "

!  Power Section Parameters "
   CONSTANT  P = 1500.          !" Converter Power 1.5kW "
   CONSTANT  fs1 = 2000.       !" Switching Frequency 2 kHz "
   Ts1 = 0.0005                  !" Switching Period "
   CONSTANT  L1 = 10.62e-3
   CONSTANT  C1 = 2.4e-3
   CONSTANT  RLD = 15.
   CONSTANT  Vdi = 0.0          !" Diode Voltage Drop "
   CONSTANT  Vsw = 0.0          !" Switch Voltage Drop "
   CONSTANT tau = 25.0
   LOGICAL  SW1on
   SW1on = .true.
   iomax = P/Vref

   " Controller Parameters "

   CONSTANT  hv1 = 2.216
```

```
   CONSTANT  hn1 = 902.74

"State Variable Initial Conditions "
   CONSTANT  iL1ic = 0.
   CONSTANT  vC1ic = 0.
   CONSTANT  x1ic = 0.

   " Continuous Conduction Mode "
   LOGICAL ccm1
   ccm1 = .true.

END  !"initial"

DYNAMIC

   TERMT (t .GE. (tstop-0.5*cint))


   DERIVATIVE
vin1=200.
vref=150.-(150.*exp(-tau*t))


      " Outer Voltage Loop, PI Controller "
      x1 = INTEG((Vref - vC1),x1ic)
      i1ref = hn1*x1 + hv1*(Vref - vC1)

      " Reference Current Ramp with Slope Compensation -- Vsw ignored "
      iramp = (-vC1/L1)*mod(t,Ts1)
      i1comp = i1ref+iramp

      " Determine if Switch 1 is ON or OFF "
      PROCEDURAL(SW1on,isw1 = i1comp,i1ref,iL1)
         IF (i1comp .GT. iL1) THEN
            SW1on = .true.
            isw1 = iL1
         ELSE
            SW1on = .false.
            isw1 = 0
         ENDIF
      END  !"procedural"

      " Derivative of Inductor 1 Current:  v = L di/dt "
      PROCEDURAL(piL1=SW1on,ccm1,Vin1,vC1,Vdi,Vsw,L1)
         IF (SW1on) THEN
            ccm1 = .true.
            piL1 = (Vin1-Vsw-vC1)/L1
         ELSE
            IF (ccm1) THEN
               piL1 = (-Vdi-vC1)/L1
            ELSE
               piL1 = 0.0     !"discontinuous conduction mode"
            ENDIF
         ENDIF
      END  !"procedural"

      " Derivative of Capacitor Voltage:  i = C dv/dt "
```

```
      pvC1 = (iL1 - io1)/C1

      " State Variables"
      iL1ub = INTEG(piL1,iL1ic)
      iL1 = BOUND(0.0, 1.0e6, iL1ub)

      vC1 = INTEG(pvC1, vC1ic)


      " Discontinuous Conduction Mode when iL tries to go neg "
      SCHEDULE  dcm1 .XN. iL1

      " Power Section Dynamics "
      io1 = vC1/RLD

      " Converter Output Power "
      S1 = vC1 * io1

   END  ! "of derivative"

   DISCRETE dcm1  !" discontinuous conduction mode transition "
      ccm1 = .false.
      iLub1 = 0.0
   END

END  ! "of dynamic"

END  ! "of program"
```

2. .CMD File

```
s strplt = .t.     ! "one variable per x-axis"
s plt = 1
s calplt = .f.
s devplt = 1       ! "6 -> X-windows"
                     "5 -> ps"
                     "1 -> ???"
s ppoplt = .f.     ! "true rotates plot 90 deg"
s xinspl = 6       ! "x-axis plot units"
s weditg = .f.     ! "false suppresses data write each time SCHEDULE
occurs"
s nrwitg = .f.     ! "true enables accumulation of data after a CONTIN"
s alcplt = .f.

prepare t,iL1,vC1,il1ref,il1comp,io1,isw1,x1,S1,iramp,vramp

proced iv
  plot vc1,il1
end

proced r1
  s cint = 1.e-5
```

```
   s tstop = 0.25
   s RLD = 15.          !" 100% load for 1.5kW converter "
   start
   s nrwitg = .true.
   s tstop = 0.45
   s RLD = 30.          !" 50% load "
   contin
   s tstop = 0.65
   s RLD = 15.
   contin
   s nrwitg = .false.
   iv
end

proced r2
   s cint = 1.e-5
   s tstop = 0.4
   s RLD = 15.          !" 100% load for 1.5kW converter "
   start
   s nrwitg = .true.
   s tstop = .7

   s RLD = 30.          !" 50% load "
   contin
   s nrwitg = .false.
   iv
end

proced ev
   analyze /eigen
end
```

B. MODEL TWO

1. .CSL File

```
!  T. Hekman
!  Filename: cmc2.csl

!  Single converter -- CURRENT MODE
!  Features:
!     *  continuous or discontinuous conduction mode operation
!     *  purely resistive load
!     *  closed loop control algorithm
!  Control algorithm: Middlebrook
```

```
PROGRAM

INITIAL

!  Simulation Parameters "
   MAXTERVAL  maxt = 1e-5 !"max step for var step integration algorithm"
   MINTERVAL  mint = 1e-6 !"min step for var step integration algorithm"
   CINTERVAL  cint = .5e-4       !" data communication interval "
   ALGORITHM  ialg = 5          !" 4 -> RK 2nd, 5 -> RK 4th "
   NSTEPS     nstp = 1
   CONSTANT   tstop = 0.01      !" stop point for integration "

!  Power Section Parameters "
   CONSTANT  P = 1500.          !" Converter Power 1.5kW "
   CONSTANT  fs1 = 2000.       !" Switching Frequency 2 kHz "
   Ts1 = 0.0005                 !" Switching Period "
   CONSTANT  L1 = 10.62e-3
   CONSTANT  C1 = 4.8e-3
   CONSTANT  RLD = 15.
   CONSTANT  Vdi = 0.0          !" Diode Voltage Drop "
   CONSTANT  Vsw = 0.0          !" Switch Voltage Drop "
   CONSTANT  w1 = 28.8
   CONSTANT  a1m = .6212
   CONSTANT  tau=15.
   CONSTANT  vin1=200.

   shift = 4.625
   LOGICAL  SW1on
   SW1on = .true.
   iomax = P/Vref

   " Controller Parameters "
        !"Removed vref=150 from here replaced with if then below"
       !" Rated Converter Output Voltage "


"State Variable Initial Conditions "
   CONSTANT  iL1ic = 0.
   CONSTANT  vC1ic = 0.
   CONSTANT  x1ic = 0.

   " Continuous Conduction Mode "
   LOGICAL ccm1
   ccm1 = .true.

END  !"initial"

DYNAMIC

   TERMT (t .GE. (tstop-0.5*cint))


   DERIVATIVE


   vref=150.-(150.*exp(-tau*t))
   Is=.025*10.4*iL1
```

```
Is1=3.5*mod(t,Ts1)/Ts1
Is2=Is+Is1


   " Outer Voltage Loop, PI Controller "
   x1 = INTEG((Vref - vC1),x1ic)
   vcont = alm*w1*x1 + alm*(Vref - vC1)



   " Determine if Switch 1 is ON or OFF "
   PROCEDURAL(SW1on,isw1 = vcont,Is2,iL1)
      IF (vcont .GT. Is2) THEN
         SW1on = .true.
         isw1 = iL1
      ELSE
         SW1on = .false.
         isw1 = 0
      ENDIF
   END  !"procedural"

   " Derivative of Inductor 1 Current:  v = L di/dt "
   PROCEDURAL(piL1=SW1on,ccm1,Vin1,vC1,Vdi,Vsw,L1)
      IF (SW1on) THEN
         ccm1 = .true.
         piL1 = (Vin1-Vsw-vC1)/L1
      ELSE
         IF (ccm1) THEN
            piL1 = (-Vdi-vC1)/L1
         ELSE
            piL1 = 0.0     !"discontinuous conduction mode"
         ENDIF
      ENDIF
   END  !"procedural"

   " Derivative of Capacitor Voltage:  i = C dv/dt "
   pvC1 = (iL1 - io1)/C1

   " State Variables"
   iL1ub = INTEG(piL1,iL1ic)
   iL1 = BOUND(0.0, 1.0e6, iL1ub)

   vC1 = INTEG(pvC1, vC1ic)


   " Discontinuous Conduction Mode when iL tries to go neg "
   SCHEDULE  dcm1 .XN. iL1

   " Power Section Dynamics "
   io1 = vC1/RLD

   " Converter Output Power "
   S1 = vC1 * io1

END  ! "of derivative"
```

```
    DISCRETE dcm1  !" discontinuous conduction mode transition "
       ccm1 = .false.
       iLub1 = 0.0
    END

END  ! "of dynamic"

END  ! "of program"
```

2. .CMD File

```
s strplt = .t.     ! "one variable per x-axis"
s plt = 1
s calplt = .f.
s devplt = 1       ! "6 -> X-windows"
                     "5 -> ps"
                     "1 -> ???"
s ppoplt = .f.     ! "true rotates plot 90 deg"
s xinspl = 6       ! "x-axis plot units"
s weditg = .f.     ! "false suppresses data write each time SCHEDULE
occurs"
s nrwitg = .f.     ! "true enables accumulation of data after a CONTIN"
s alcplt = .f.

prepare t,iL1,vC1,vcont,Is2,io1,isw1,x1,S1,Is1

proced iv
  plot vc1,il1
end

proced r1
  s cint = 1.e-5
  s tstop = 0.5
  s RLD = 15.          !" 100% load for 1.5kW converter "
  start
  s nrwitg = .true.
  s tstop = 0.7
  s RLD = 30.          !" 50% load "
  contin
  s tstop = 0.9
  s RLD = 15.
  contin
  s nrwitg = .false.
  iv
end

proced r2
  s cint = 1.e-5
  s tstop = 0.5
```

```
  s RLD = 15.          !" 100% load for 1.5kW converter "
  start
  s nrwitg = .true.
  s tstop = 1.0

  s RLD = 30.          !" 50% load "
  contin
  s nrwitg = .false.
  iv
end

proced r3
  s cint = 1e-5
  s tstop = 0.2
  s RLD = 15.          !" 100% load for 1.5kW converter "
  start
  iv
end

proced ev
  analyze /eigen
end
```

APPENDIX C: CLASSICAL CONTROL SCHEMATIC

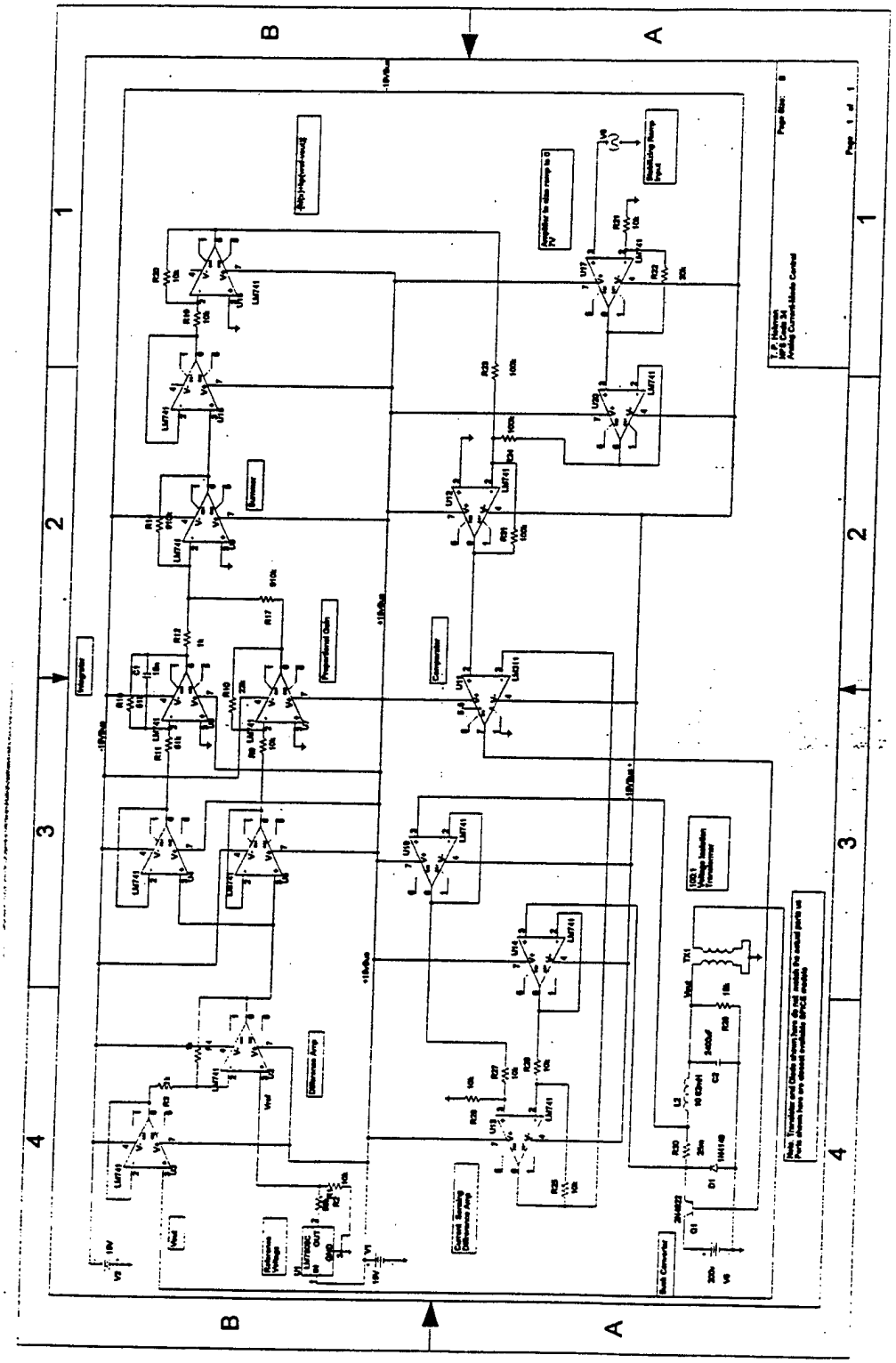

Figure C-1: Classical Control Method Schematic.

Figure (C-1) illustrates the implementation of current-mode control using classical control methods. The circuit is analog and uses LM741 Operational Amplifiers.

Starting with the bottom right of Figure (C-1), stabilizing slope compensation is provided by using the ramp signal from pin 8 of the UC3846 PWM chip. The UC3846 ramp exhibits a DC bias as discussed in Chapter II which must be removed and the signal biased to yield a 0V – 7.1V ramp. The 7.1V peak value is determined from the slope of the inductor current during the switch-off period ($-v_{out}/L$) and the period of the ramp signal (5ms). The circuits required to remove the bias and adjust the zero point of the ramp are not shown in Figure (C-1) due to space limitations. The slope compensation circuit for this control is identical to the one shown on the bottom row of Figure (D-1), up to the point that the ramp is summed with the control signal. The only exception is that no gain is applied in this case. The DC bias of the ramp is removed by a 47nF capacitor placed in series. The signal is then summed with an approximately 0.8V signal to bias the ramp so that the minimum value is zero volts. The 0.8V signal was provided by a LM7806 voltage regulator through a voltage divider. The summing process inverts the signal requiring a second inversion. The signal is buffered before being input to amplifier U17 of Figure (C-1). Amplifier U17 is a non-inverting amplifier sized to produce a 7.1V peak ramp voltage as discussed above in this section. The ramp is now a 0V – 7.1V positive-sloped ramp with a 5ms period. The signal is then buffered before being summed with the inverted value of the control voltage to produce I^*. Summing an inverted voltage control signal with a positive-sloped ramp and then inverting the result has the same effect as adding a negative slope to a positive control signal.

In retrospect, a better solution for properly sizing the ramp signal would have been to remove the initial bias, amplify the signal, and then adjust the signal to originate at zero volts. This would have eliminated the problem of amplifying a signal and ensuring the minimum value remained at zero. Amplifying the signal after biasing the signal to start at zero resulted in some offset as the signal was not exactly at zero. This

was accounted for by adjusting the voltage divider on the output of the LM7806 experimentally.

The bottom left portion of Figure (C-1) illustrates the current sensing section of the control. The inductor current was sensed using four 0.1Ω wire wound resistors in parallel for an effective resistance of 0.025Ω. This value was selected to reduce power loss in the current sensing resistor while still providing an acceptable signal out. The difference between the high and low sides of the current sensing resistor was determined using a difference amplifier. This output was then sent to the LM311 comparator where it was compared with the slope compensated control signal to produce a gating pulse which is sent to the pulse amplifier.

The top section of Figure (C-1) illustrates the voltage control loop. Converter output voltage is sensed using a 100:1 isolation transformer. The sensed voltage signal is then buffered and sent to a difference amplifier. The difference amplifier determines the value of $v_{ref} - v_{out}$. This signal is the input separately to an integrator and a proportional gain amplifier via two buffers. The inverting integrator has a DC gain of one and a pole at 200Hz. The pole placement was selected to place it one decade below the switching frequency. The gain amplifier is an inverting amplifier with a gain of 2.2 to reflect the gain determined in Chapter III. The signal is then summed using an inverting summer. The integrator output is summed with a gain of 910; the gain amplifier output is summed with a gain of one. The control voltage signal is the output of the inverting summer. This signal is buffered and inverted with unity gain prior to summing with the stabilizing ramp as described above in this section. This is then input to the comparator where it is compared with the slope compensated control signal to produce a gating pulse which is sent to the pulse amplifier.

Not illustrated here, and still required for proper operation, is a method of combinational logic which will guarantee a gate-on signal (comparator output high) only once per 2kHz cycle. The clock pulse output of the UC3846 can provide a synchronized clock signal for digital logic circuits providing that the clock signal DC bias is eliminated and the signal properly sized in amplitude as discussed in Chapter II.

APPENDIX D: MIDDLEBROOK BASED CONTROL SCHEMATIC

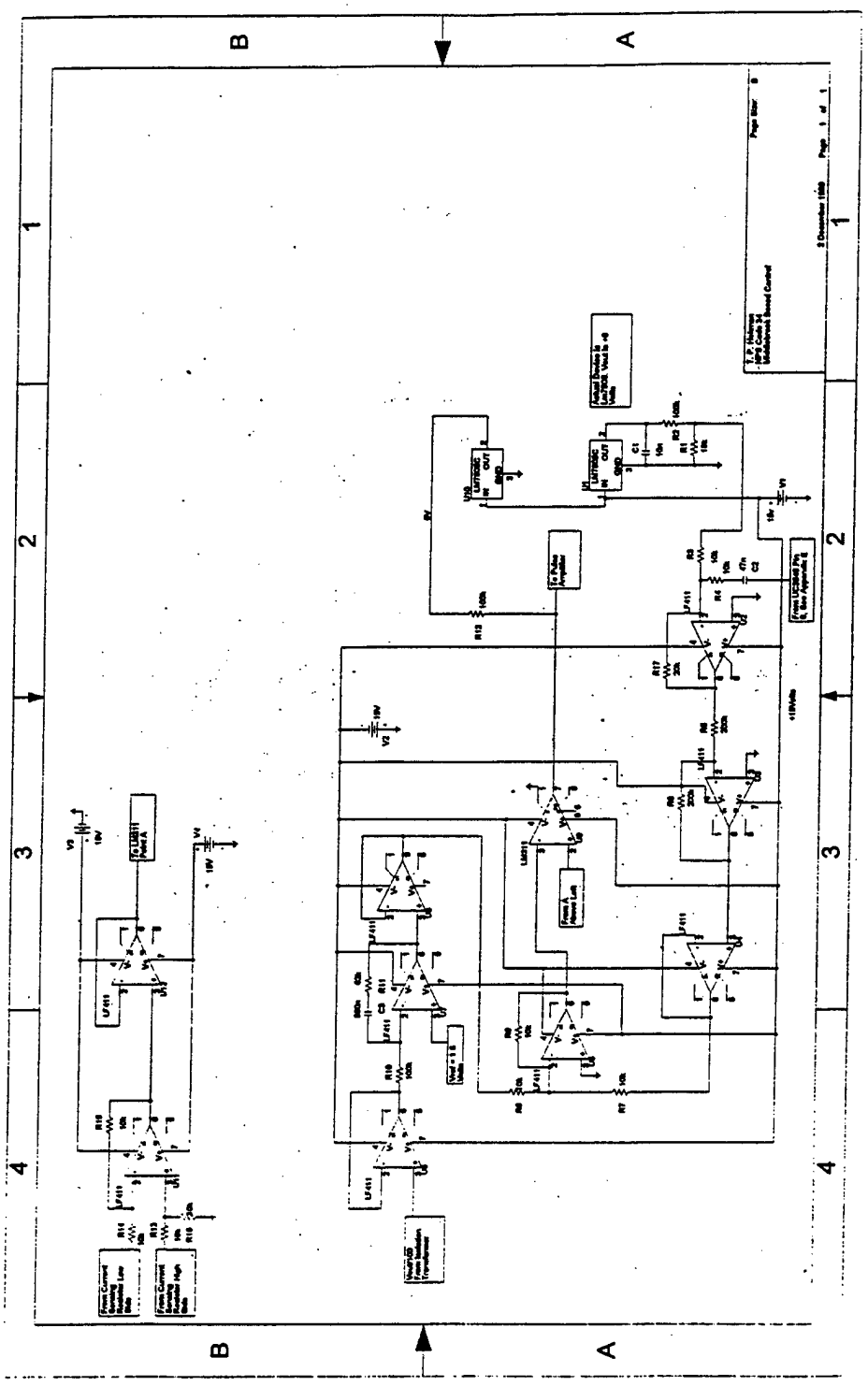

Figure D-1: Middlebrook Based Control Schematic.

The control illustrated in Figure (D-1) is an analog implementation of the control method described in reference [27].

Slope compensation is provided by the UC3846 PWM chip which is used to provide a clock pulse and ramp as described in Chapter II. The ramp signal was passed through a 47nF capacitor placed in series to eliminate any DC bias. The ramp signal was then summed with a DC signal to place the origin of the ramp at zero volts and it was amplified with a gain of 2 to achieve the desired 3.5V peak ramp amplitude. A LM7806 voltage regulator was used to provide a stable 6V DC signal for this purpose. The 6V signal was reduced using a voltage divider. The values of 100kΩ and 18kΩ were determined experimentally and yielded the desired result. The summing process inverted the signal requiring a second inversion to return the signal to a positive-sloped ramp. The stabilizing ramp was then buffered prior to summing the ramp with the inverted control signal using an inverting summer. An alternative method would have been to remove the DC bias of the ramp and then invert the ramp signal. A DC bias could then be applied to the inverted ramp causing the signal to originate at a maximum value at the start of each clock period and have a negative slope to zero volts over one switching period. This negative-sloped ramp would be summed with the control voltage to produce the proper slope-compensated control signal. This approach would require the addition of a stable negative voltage supply.

The control voltage was sensed using a 100:1 isolation transformer. This signal was then buffered before being sent to the integrator of Figure (2-10). The integrator inverts the control signal which is then buffered before being summed with the stabilizing ramp using the inverting summer mentioned above. Summing an inverted voltage control signal with a positive-sloped ramp and then inverting the result has the same effect as adding a negative slope to a positive control signal.

The inductor current was sensed using four 0.1Ω wire wound resistors in parallel for an effective resistance of 0.025Ω. This value was selected to reduce power loss in the current sensing resistor while still providing an acceptable signal out. The difference

between the high and low sides of the current sensing resistor was determined using a difference amplifier. This output was then buffered and sent to the LM311 comparator where it was compared with the slope compensated control signal to produce a gating pulse which is sent to the pulse amplifier.

Not illustrated here, and still required for proper operation, is a method of combinational logic which will guarantee a gate-on signal (comparator output high) only once per 2kHz cycle. The clock pulse output of the UC3846 can provide a synchronized clock signal for digital circuits providing that the DC bias is eliminated and the signal properly sized in amplitude as discussed in Chapter II.

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APPENDIX E: DATA SHEETS

LINEAR LSI PRODUCTS

GENERAL PURPOSE OPERATIONAL AMPLIFIER — μA741/μA741C/SA741C

DESCRIPTION

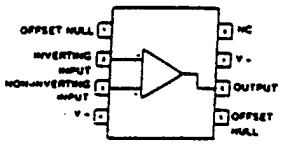
The μA741 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit protected and allows for nulling of offset voltage.

FEATURES

- Internal frequency compensation
- Short circuit protection
- Excellent temperature stability
- High input voltage range

PIN CONFIGURATION

D,FE,N PACKAGE



TOP VIEW

ORDER NUMBERS

μA741N μA741FE
μA741CN μA741CFE
SA741CN
μA741CD

ABSOLUTE MAXIMUM RATINGS

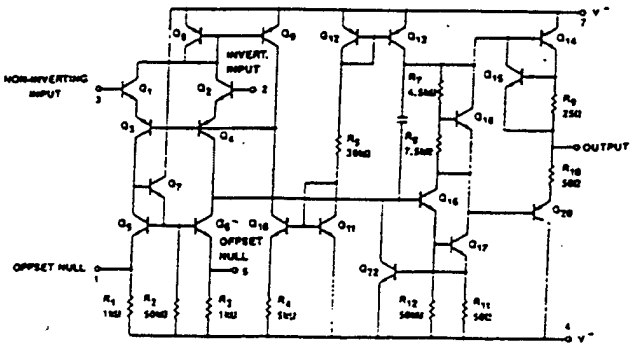
PARAMETER	RATING	UNIT
Supply voltage		
μA741C	±18	V
μA741	±22	V
Internal power dissipation		
N package	500	mW
FE package	1000	mW
Differential input voltage	±30	V
Input voltage	±15	V
Output short-circuit duration	Continuous	
Operating temperature range		
μA741C	0 to +70	°C
SA741C	−40 to +85	°C
μA741	−55 to +125	°C
Storage temperature range	−65 to +150	°C
Lead temperature (soldering 60sec)	300	°C

NOTE

1. For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.

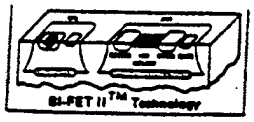
EQUIVALENT SCHEMATIC

μA741, μA741C, SA741C



B. LF411

National Semiconductor Corporation



LF411A/LF411 Low Offset, Low Drift JFET Input Operational Amplifier

General Description

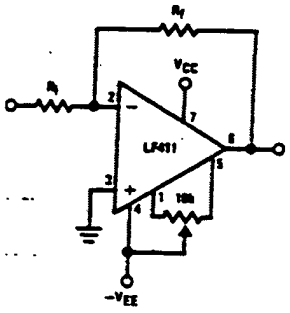
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

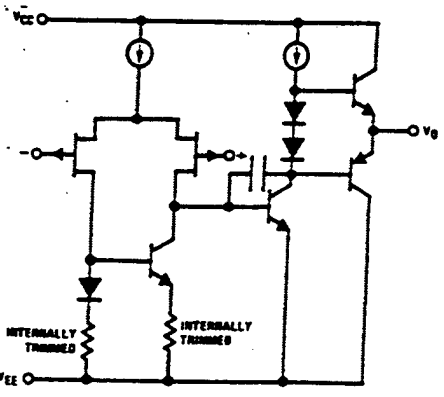
■ Internally trimmed offset voltage	0.5 mV(max)
■ Input offset voltage drift	10 μV/°C(max)
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	3 MHz(min)
■ High slew rate	10V/μs(min)
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



TL/H/5665–1

Simplified Schematic



TL/H/5665–6

Ordering Information

LF411XYZ

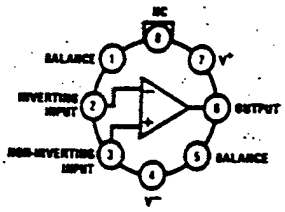
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package



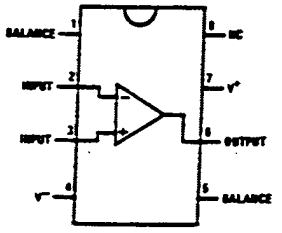
TL/H/5665–3

Top View

Note: Pin 4 connected to case.

Order Number LF411AMH, LF411MH, LF411ACH or LF411CH
See NS Package Number H08B

Dual-In-Line Package



TL/H/5665–7

Top View
Order Number
LF411ACN or LF411CN
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 8)

	LF411A	LF411
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	H Package	N Package
Power Dissipation (Notes 2 and 9)	670 mW	670 mW
$T_J$max	150°C	115°C
θ_{JA}	225°C/W (Still Air) 160°C/W (400 LF/min Air Flow)	120°C/W
θ_{JC}	25°C/W	
Operating Temp. Range	(Note 3)	(Note 3)
Storage Temp. Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
Lead Temp. (Soldering, 10 sec.)	260°C	260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		LF411A Min	LF411A Typ	LF411A Max	LF411 Min	LF411 Typ	LF411 Max	Units
V_{OS}	Input Offset Voltage	$R_S = 10\,k\Omega$, $T_A = 25°C$			0.3	0.5		0.6	2.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\,k\Omega$ (Note 5)			7	10		7	20 (Note 5)	µV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 4, 6)	$T_j = 25°C$		25	100		25	100	pA
			$T_j = 70°C$			2			2	nA
			$T_j = 125°C$			25			25	nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 4, 6)	$T_j = 25°C$		50	200		50	200	pA
			$T_j = 70°C$			4			4	nA
			$T_j = 125°C$			50			50	nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10k$		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	100		dB
I_S	Supply Current				1.8	2.8		1.8	3.4	mA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF411A Min	LF411A Typ	LF411A Max	LF411 Min	LF411 Typ	LF411 Max	Units
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	10	15		8	15		V/µs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, $f = 1$ kHz		25			25		nV/√Hz
i_n	Equivalent Input Noise Current	$T_A = 25°C$, $f = 1$ kHz		0.01			0.01		pA/√Hz

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA}.

Note 3: These devices are available in both the commercial temperature range $0°C \le T_A \le 70°C$ and the military temperature range $-55°C \le T_A \le 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 4: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF411A and for $V_S = \pm 15V$ for the LF411. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 5: The LF411A is 100% tested to this specification. The LF411 is sample tested to insure at least 90% of the units meet this specification.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

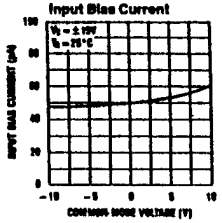
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from ±15V to ±5V for the LF411 and from ±20V to ±5V for the LF411A.

Note 8: Refer to RETS 411AX for LF411AMH military specifications and to RETS 411X for LF411MH military specifications.

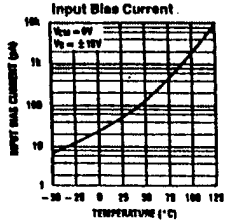
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

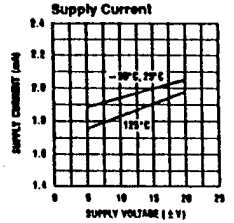
Input Bias Current



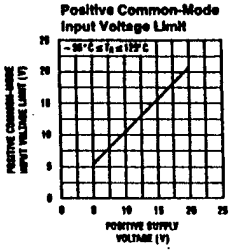
Input Bias Current



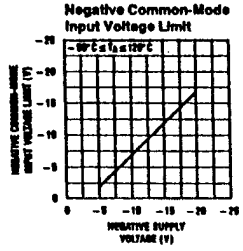
Supply Current



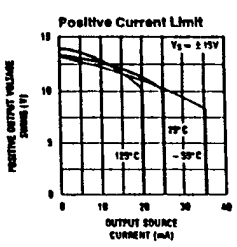
Positive Common-Mode Input Voltage Limit



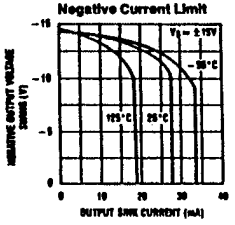
Negative Common-Mode Input Voltage Limit



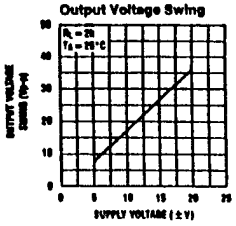
Positive Current Limit



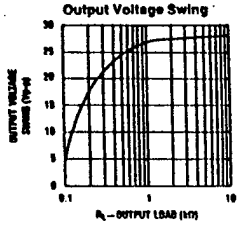
Negative Current Limit



Output Voltage Swing



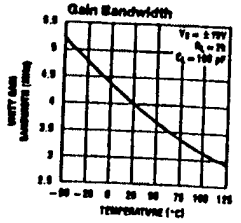
Output Voltage Swing



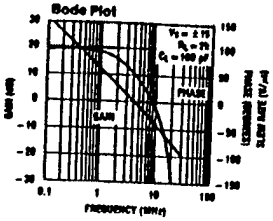
TL/H/5655-2

Typical Performance Characteristics (Continued)

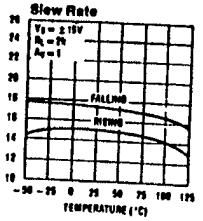
Gain Bandwidth



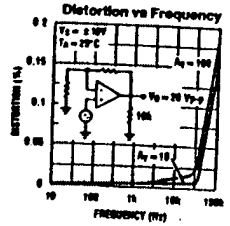
Bode Plot



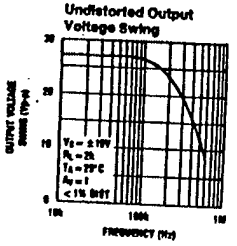
Slew Rate



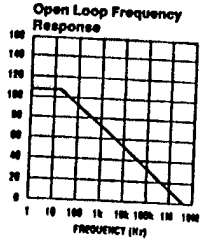
Distortion vs Frequency



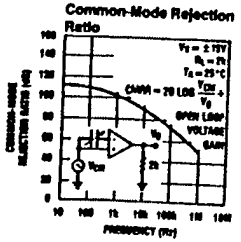
Undistorted Output Voltage Swing



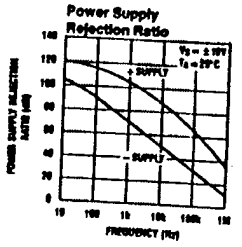
Open Loop Frequency Response



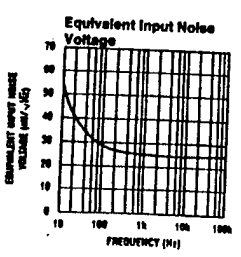
Common-Mode Rejection Ratio



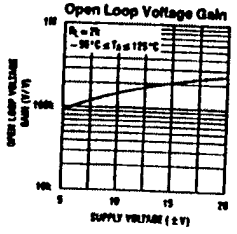
Power Supply Rejection Ratio



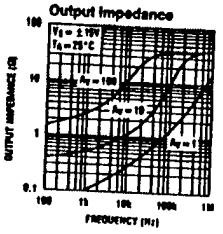
Equivalent Input Noise Voltage



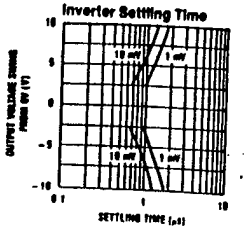
Open Loop Voltage Gain



Output Impedance



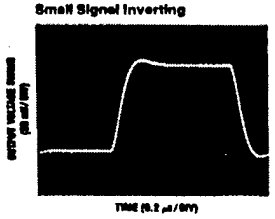
Inverter Settling Time



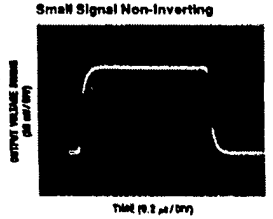
TL/H/5655-3

Pulse Response $R_L = 2\,k\Omega$, C_L 10 pF

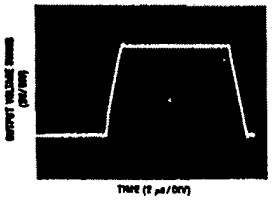
Small Signal Inverting



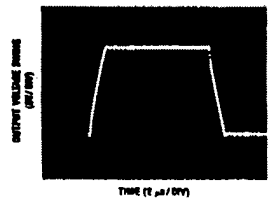
Small Signal Non-Inverting



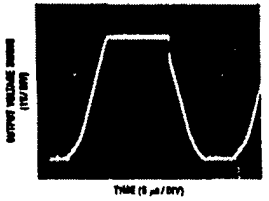
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



TL/H/5655-4

Application Hints

The LF411 series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

Application Hints (Continued)

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

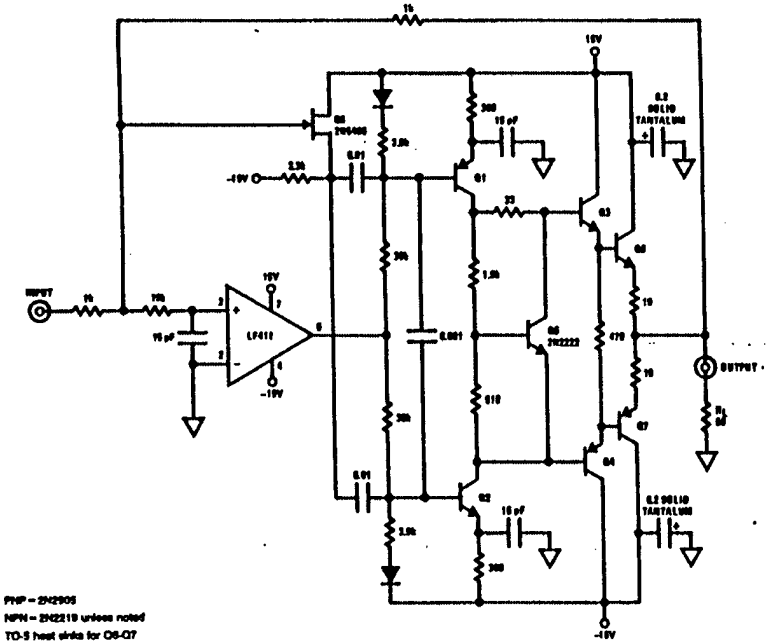
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

Ultra High Speed Current Booster

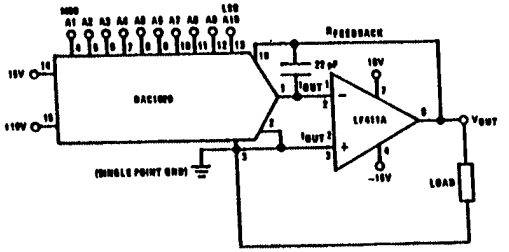


PNP = 2N2905
NPN = 2N2219 unless noted
TO-5 heat sinks for Q6-Q7

TL/H/5655-9

Typical Applications (Continued)

10-Bit Linear DAC with No V_{OS} Adjust



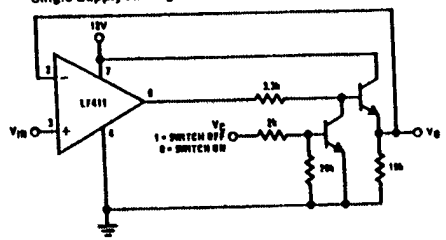
$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

$-10V \leq V_{REF} \leq 10V$

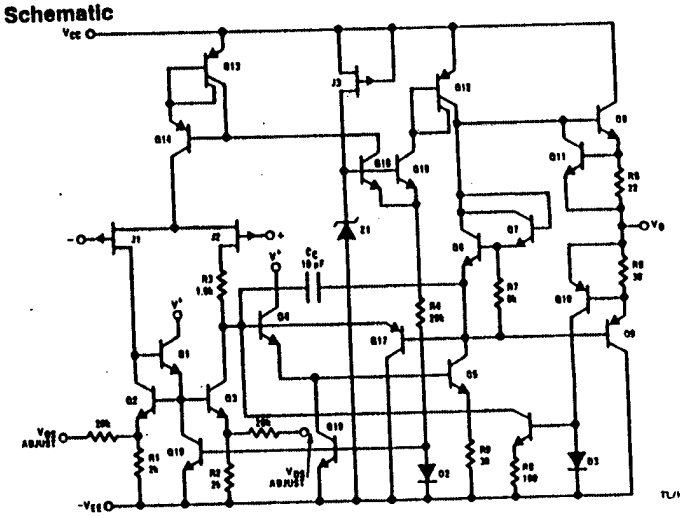
$0 \leq V_{OUT} \leq -\frac{1023}{1024} V_{REF}$

where $A_N = 1$ if the A_N digital input is high
$A_N = 0$ if the A_N digital input is low

Single Supply Analog Switch with Buffered Output



Detailed Schematic



TL/H/5655-10

C. LP311

National Semiconductor Corporation

LP311 Voltage Comparator

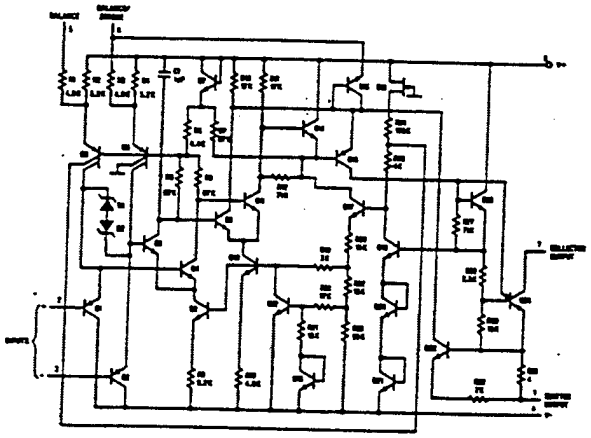
General Description

The LP311 is a low power version of the industry-standard LM311. It takes advantage of stable high-value ion-implanted resistors to perform the same function as an LM311, with a 30:1 reduction in power drain, but only a 6:1 slowdown of response time. Thus the LP311 is well suited for battery-powered applications, and all other applications where fast response is not needed. It operates over a wide range of supply voltages from 36V down to a single 3V supply, with less than 200 μA drain, but it is still capable of driving a 25 mA load. The LP311 is quite easy to apply without any oscillation, if ordinary precautions are taken to minimize stray coupling from the output to either input or to the trim pins. (See the LM311 section of the Linear Databook.)

Features

- Low power drain, 900 μW on 5V supply
- Operates from ±15V or a single supply as low as 3V
- Output can drive 25 mA
- Emitter output can swing below negative supply
- Response time: 1.2 μs
- Same pin-out as LM311
- Low input currents: 2 nA of offset, 15 nA of bias
- Large common-mode input range: −14.6V to 13.6V with ±15V supply

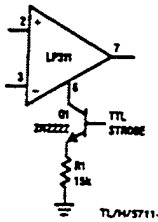
Schematic Diagram



TL/H/5711–7

Auxiliary Circuits

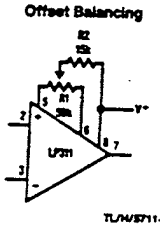
Strobing



TL/H/5711–1

Note: Do not ground strobe pin.

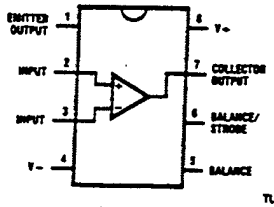
Offset Balancing



TL/H/5711–2

Connection Diagram

Dual-In-Line Package



TL/H/5711–4

Top View

Order Number LP311N
See NS Package Number N08E

4-75

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Total Supply Voltage (V_{8-4})	36V
Collector Output to Negative Supply Voltage (V_{7-4})	40V
Collector Output to Emitter Output	40V
Emitter Output to Negative Supply Voltage (V_{1-4})	±30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 100k$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		2.0	25	nA
Input Bias Current	$T_A = 25°C$		15	100	nA
Voltage Gain	$T_A = 25°C$, $R_L = 5k$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		1.2		µs
Saturation Voltage (Note 6)	$V_{IN} \leq -10$ mV, $I_{OUT} = 25$ mA, $T_A = 25°C$		0.4	1.5	V
Strobe Current (Note 7)	$T_A = 25°C$	100	200	300	µA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$, $T_A = 25°C$		0.2	100	nA
Input Offset Voltage (Note 4)	$R_S \leq 100k$			10	mV
Input Offset Current (Note 4)				35	nA
Input Bias Current				150	nA
Input Voltage Range		V− +0.5	+13.7, −14.7	V+ −1.5	V
Saturation Voltage (Note 6)	$V^+ \geq 4.5V$, $V^- = 0V$, $V_{IN} \leq -10$ mV, $I_{SINK} \leq 1.6$ mA		0.1	0.4	V
Positive Supply Current	$T_A = 25°C$, Output on		150	300	µA
Negative Supply Current	$T_A = 25°C$		90	150	µA
Minimum Operating Voltage	$T_A = 25°C$		3.0	3.5	V

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LP311 is 85°C. For operating at elevated temperatures, devices in the dual-in-line package must be derated based on a thermal resistance of 150°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq 70°C$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 4V supply up to ±15V supplies.

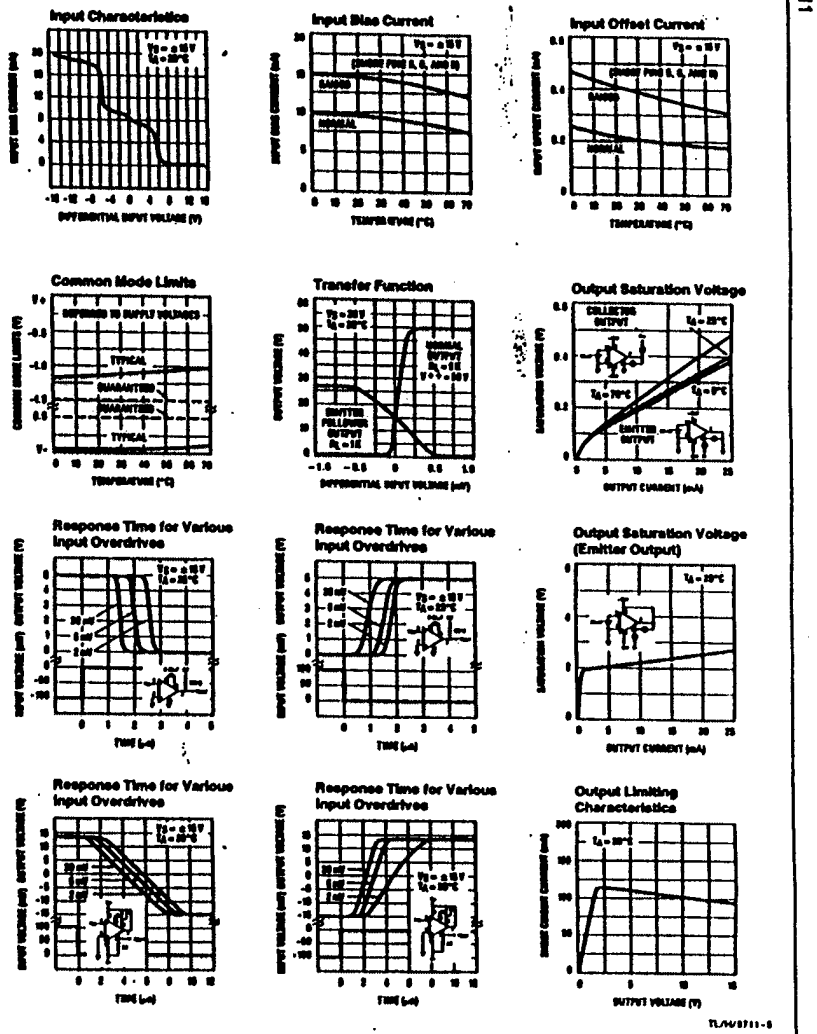
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

Note 6: Saturation voltage specification applied to collector-emitter voltage (V7-1) for $V_{COLLECTOR} \leq (V^+ - 3V)$.

Note 7: Do not short the strobe pin to ground. It should be current driven, 100 µA to 300 µA.

Typical Performance Characteristics



D. UC3846

1. UC3846 Data Sheet

UNITRODE

UC1846/7
UC2846/7
UC3846/7

Current Mode PWM Controller

FEATURES

- Automatic Feed Forward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- Automatic Symmetry Correction in Push-pull Configuration
- Enhanced Load Response Characteristics
- Parallel Operation Capability for Modular Power Systems
- Differential Current Sense Amplifier with Wide Common Mode Range
- Double Pulse Suppression
- 500mA (Peak) Totem-pole Outputs
- ±1% Bandgap Reference
- Under-voltage Lockout
- Soft Start Capability
- Shutdown Terminal
- 500kHZ Operation

DESCRIPTION

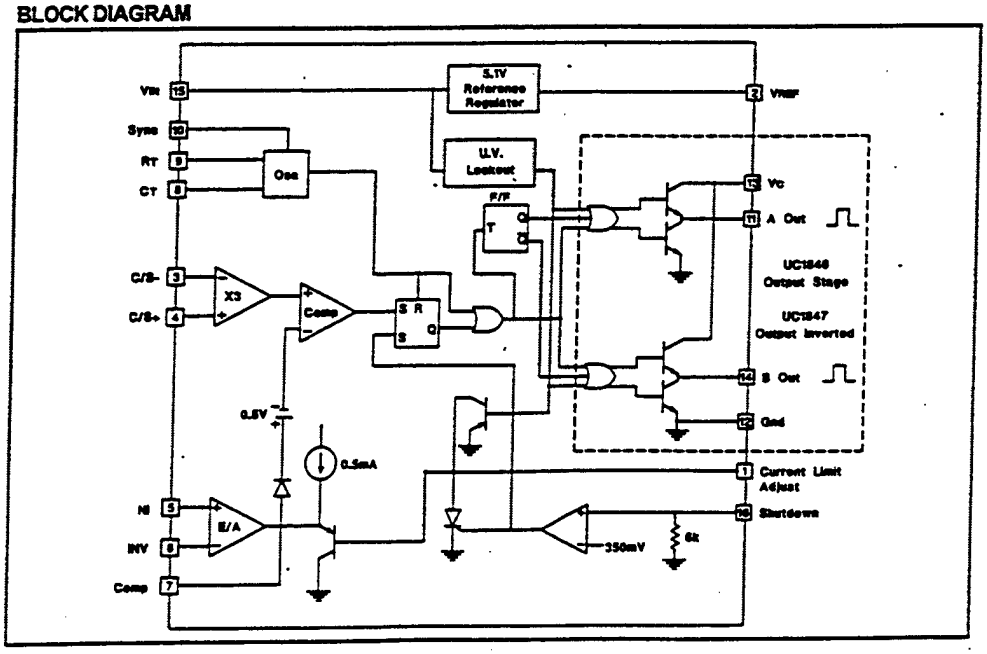
The UC1846/7 family of control ICs provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression, deadline adjust capability, and a ±1% trimmed bandgap reference.

The UC1846 features low outputs in the OFF state, while the UC1847 features high outputs in the OFF state.

BLOCK DIAGRAM



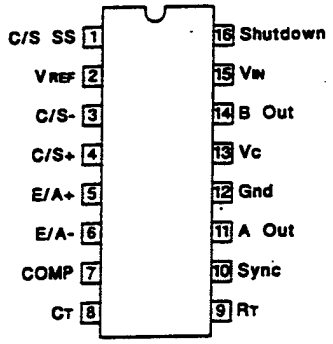
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pin 15) ..... +40V
Collector Supply Voltage (Pin 13) ..... +40V
Output Current, Source or Sink (Pins 11, 14) 500mA
Analog Inputs (Pins 3, 4, 5, 6, 16) ..... -0.3V to +V_{IN}
Reference Output Current (Pin 2) ..... -30mA
Sync Output Current (Pin 10) ..... -5mA
Error Amplifier Output Current (Pin 7) ..... -5mA
Soft Start Sink Current (Pin 1) 50mA
Oscillator Charging Current (Pin 9) 5mA
Power Dissipation at T_A=25°C 1000mW
Power Dissipation at T_C=25°C 2000mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

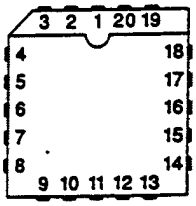
Note 1. All voltages are with respect to Ground, Pin 13. Currents are positive into, negative out of the speficied terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL and SOIC packages only.

CONNECTION DIAGRAMS

DIL-16, SOIC-16
(TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
C/L SS	2
V_{REF}	3
C/S-	4
C/S+	5
N/C	6
E/A+	7
E/A-	8
Comp	9
C_T	10
N/C	11
R_T	12
Sync	13
A Out	14
Gnd	15
N/C	16
Vc	17
B Out	18
V_{IN}	19
Shutdown	20

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_J=25°C, Io=1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN}=8V to 40V		5	20		5	20	mV
Load Regulation	I_L=1mA to 10mA		3	15		3	15	mV
Temperature Stability	Over Operating Range, (Note 2)		0.4			0.4		mV/°C
Total Output Variation	Line, Load, and Temperature (Note 2)	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz≤ f ≤10kHz, T_J=25°C (Note 2)		100			100		µV
Long Term Stability	T_J=125°C, 1000 Hrs. (Note 2)		5			5		mV
Short Circuit Output Current	V_{REF}=0V	-10	-45		-10	-45		mA

ELECTRICAL CHARACTERISTICS (cont.) (Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Oscillator Section								
Initial Accuracy	T_J=25°C	39	43	47	39	43	47	kHz
Voltage Stability	V_{IN}=8V to 40V		-1	2		-1	2	%
Temperature Stability	Over Operating Range (Note 2)		-1			-1		%
Sync Output High Level		3.9	4.35		3.9	4.35		V
Sync Output Low Level			2.3	2.5		2.3	2.5	V
Sync Input High Level	Pin 8=0V	3.9			3.9			V
Sync Input Low Level	Pin 8=0V			2.5			2.5	V
Sync Input Current	Sync Voltage=3.9V, Pin 8=0V		1.3	1.5		1.3	1.5	mA
Error Amp Section								
Input Offset Voltage			0.5	5		0.5	10	mV
Input Bias Current			-0.6	-1		-0.6	-2	µA
Input Offset Current			40	250		40	250	nA
Common Mode Range	V_{IN}=8V to 40V	0		V_{IN}-2V	0		V_{IN}-2V	V
Open Loop Voltage Gain	ΔVo=1.2 to 3V, V_{CM}=2V	80	105		80	105		dB
Unity Gain Bandwidth	T_J=25°C (Note 2)	0.7	1.0		0.7	1.0		MHz
CMRR	V_{CM}=0V to 38V, V_{IN}=40V	75	100		75	100		dB
PSRR	V_{IN}=8V to 40V	80	105		80	105		dB
Output Sink Current	V_{ID}=-15mV to -5V, $V_{PIN\ 7}$=1.2V	2	6		2	6		mA
Output Source Current	V_{ID}=15mV to 5V, $V_{PIN\ 7}$=2.5V	-0.4	-0.5		-0.4	-0.5		mA
High Level Output Voltage	R_L=(Pin 7) 15kΩ	4.3	4.6		4.3	4.6		V
Low Level Output Voltage			0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain	$V_{PIN\ 3}$=0V, Pin 1 Open (Notes 3 & 4)	2.5	2.75	3.0	2.5	2.75	3.0	V
Maximum Differential Input Signal ($V_{PIN\ 4}$-$V_{PIN\ 3}$)	Pin 1 Open (Note 3) R_L (Pin 7)=15kW	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		5	25		5	25	mV
CMRR	V_{CM}=1V to 12V	60	83		60	83		dB
PSRR	V_{IN}=8V to 40V	60	84		60	84		dB
Input Bias Current	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		-2.5	-10		-2.5	-10	µA
Input Offset Current	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		0.08	1		0.08	1	µA
Input Common Mode Range		0		V_{IN}-3	0		V_{IN}-3	V
Delay to Outputs	T_J=25°C, (Note 2)		200	500		200	500	ns
Current Limit Adjust Section								
Current Limit Offset	$V_{PIN\ 3}$=0V, $V_{PIN\ 4}$=0V, Pin 7 Open (Note 3)	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{PIN\ 5}$=V_{REF}, $V_{PIN\ 6}$=0V		-10	-30		-10	-30	µA
Shutdown Terminal Section								
Threshold Voltage		250	350	400	250	350	400	mV
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current ($I_{PIN\ 1}$)	(Note 6)	3.0	1.5		3.0	1.5		mA

ELECTRICAL CHARACTERISTICS (cont.)

(Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Shutdown Terminal Section (cont.)								
Maximum Non-Latching Current ($I_{PIN\ 1}$)	(Note 7)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	T_J=25°C (Note 2)		300	600		300	600	ns
Output Section								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_C=40V (Note 5)			200			200	µA
Output Low Level	I_{SINK}=20mA		0.1	0.4		0.1	0.4	V
	I_{SINK}=100mA		0.4	2.1		0.4	2.1	V
Output High Level	I_{SOURCE}=20mA	13	13.5		13	13.5		V
	I_{SOURCE}=100mA	12	13.5		12	13.5		V
Rise Time	C_L=1nF, T_J=25°C (Note 2)		50	300		50	300	ns
Fall Time	C_L=1nF, T_J=25°C (Note 2)		50	300		50	300	ns
Under-Voltage Lockout Section								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.75			0.75		V
Total Standby Current								
Supply Current			17	21		17	21	mA

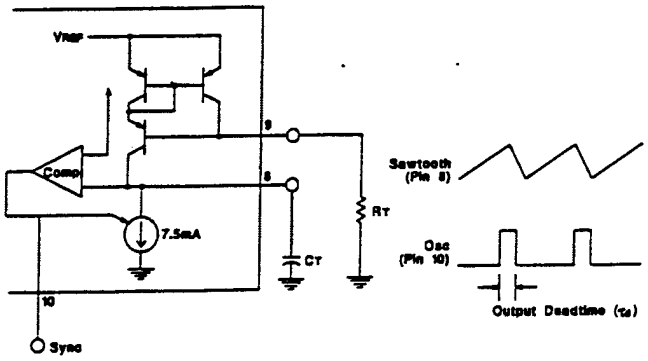
Note 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 3. Parameter measured at trip point of latch with $V_{PIN\ 5}$ = V_{REF}, $V_{PIN\ 8}$ = 0V.

Note 4. Amplifier gain defined as: $G = \frac{\Delta V_{PIN\ 7}}{\Delta V_{PIN\ 4}}$; $\Delta V_{PIN\ 4}$ = 0 to 1.0V.

Note 5. Applies to UC1846/UC2846/UC3846 only due to polarity of outputs.
Note 6. Current into Pin 1 guaranteed to latch circuit in shutdown state.
Note 7. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

APPLICATIONS DATA

Oscillator Circuit



Output deadtime is determined by the external capacitor, C_T, according to the formula: $\tau_d(\mu s) = 145 C_T(\mu f)\left(\frac{I_O}{I_O - \frac{3.6}{R_T(k\Omega)}}\right)$.

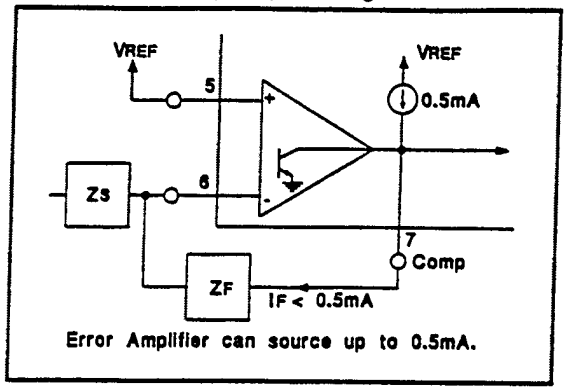
I_O = Oscillator discharge current at 25°C is typically 7.5.

For large values of R_T: $\tau_d(\mu s) \approx 145 C_T(\mu f)$.

Oscillator frequency is approximated by the formula: $f_T(kHz) \approx \frac{2.2}{R_T(k\Omega) \bullet C_T(\mu f)}$.

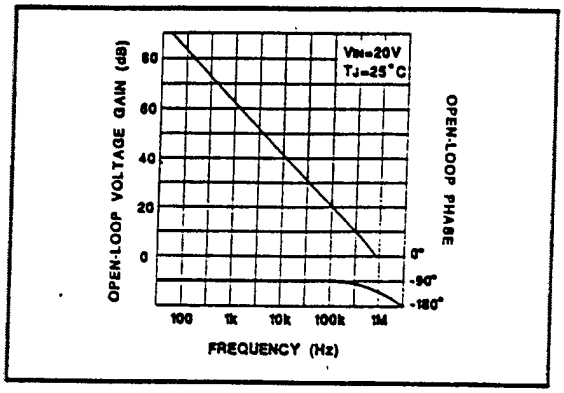
APPLICATIONS DATA (cont.)

Error Amp Output Configuration

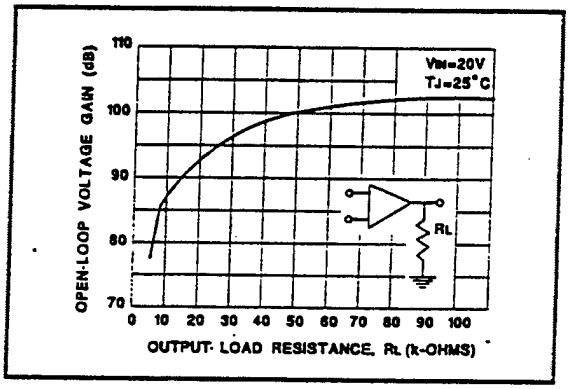


Error Amplifier can source up to 0.5mA.

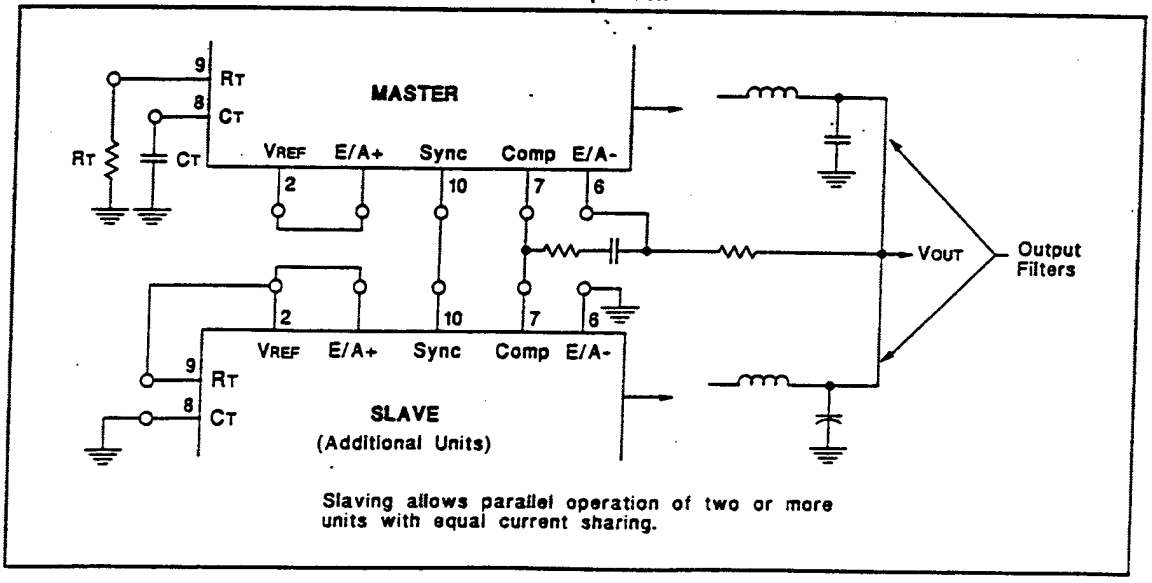
Error Amp Gain and Phase vs Frequency



Error Amp Open-Logic D.C. Gain vs Load Resistance



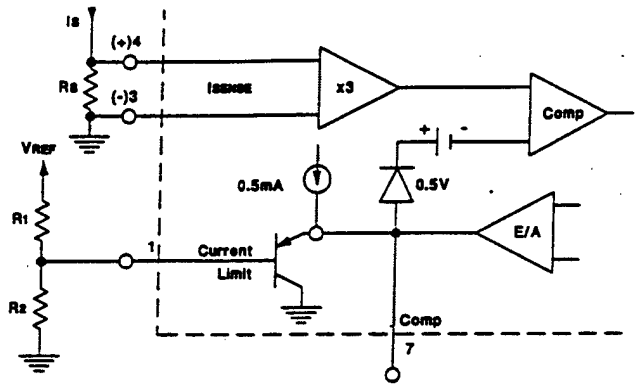
Parallel Operation



Slaving allows parallel operation of two or more units with equal current sharing.

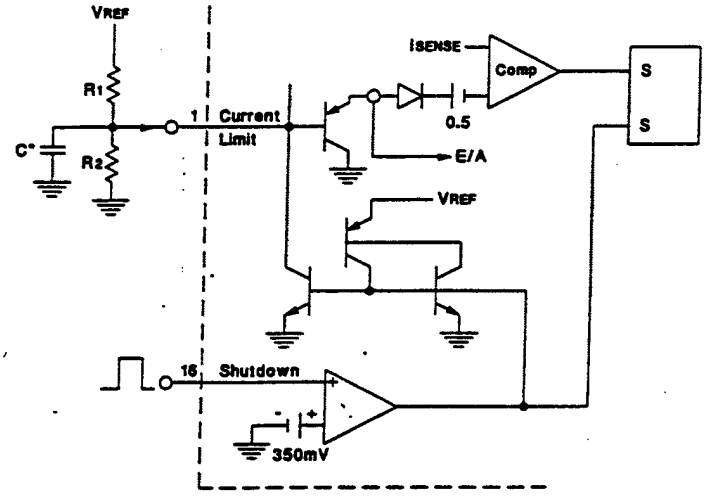
APPLICATIONS DATA (cont.)

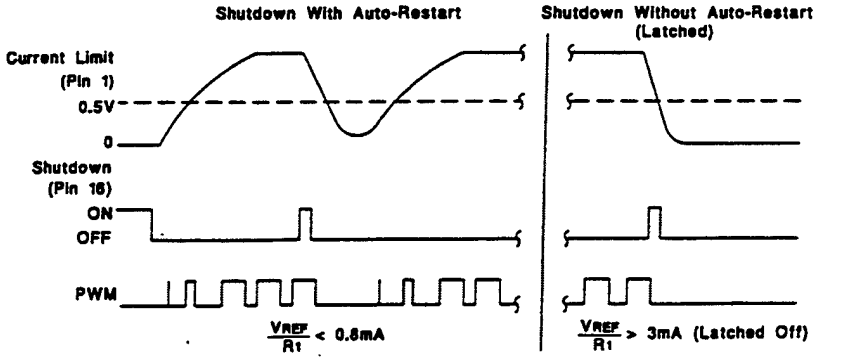
Pulse by Pulse Current Limiting



Peak Current (Is) is determined by the formula: $Is = \dfrac{\dfrac{R2\ VREF}{R1 + R2} - 0.5}{3Rs}$

Soft Start and Shutdown /Restart Functions



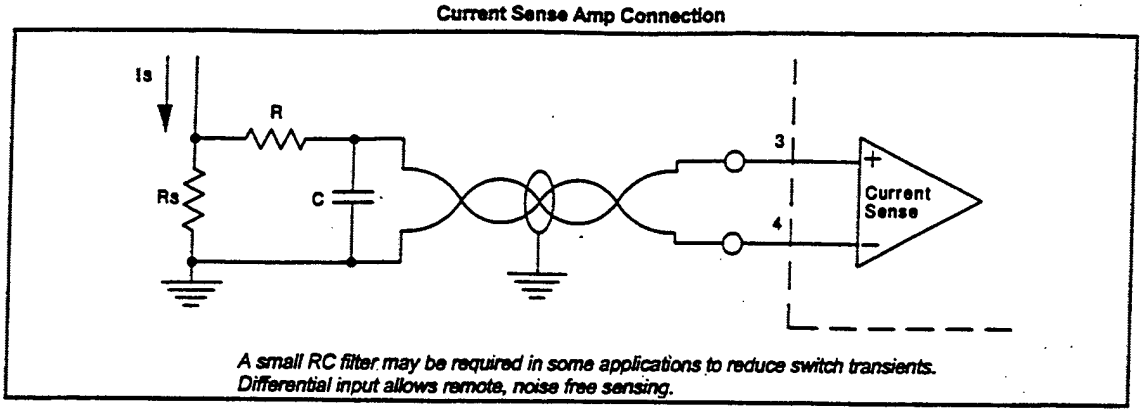


If $\frac{VREF}{R1}$ < 0.8mA, the shutdown latch will commutate when Iss = 0.8mA and a restart cycle will be initiated.

If $\frac{VREF}{R1}$ > 3mA, the device will latch off until power is recycled.

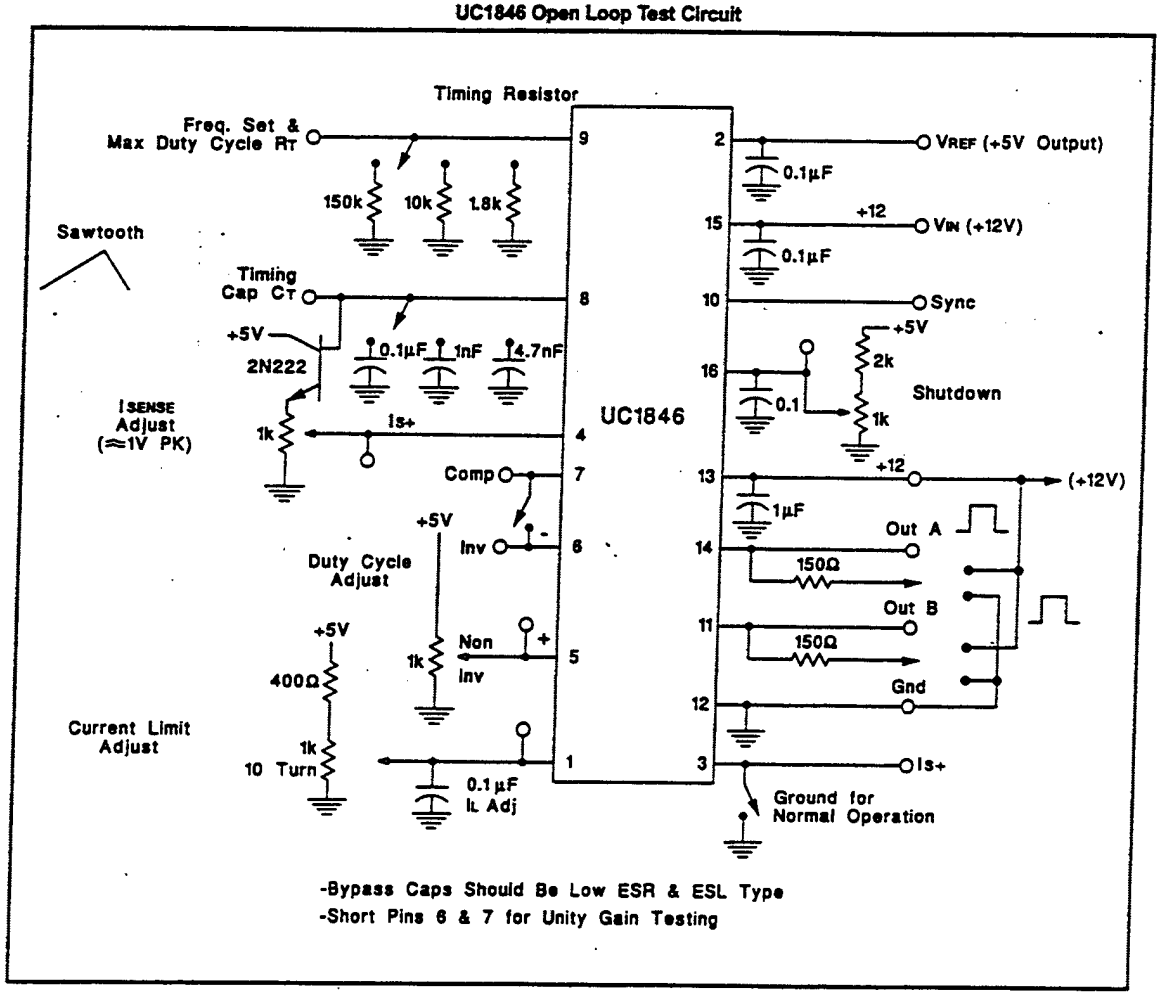
APPLICATIONS DATA (cont.)

Current Sense Amp Connection



A small RC filter may be required in some applications to reduce switch transients.
Differential input allows remote, noise free sensing.

UC1846 Open Loop Test Circuit



-Bypass Caps Should Be Low ESR & ESL Type
-Short Pins 6 & 7 for Unity Gain Testing

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2. UC3846 Plots

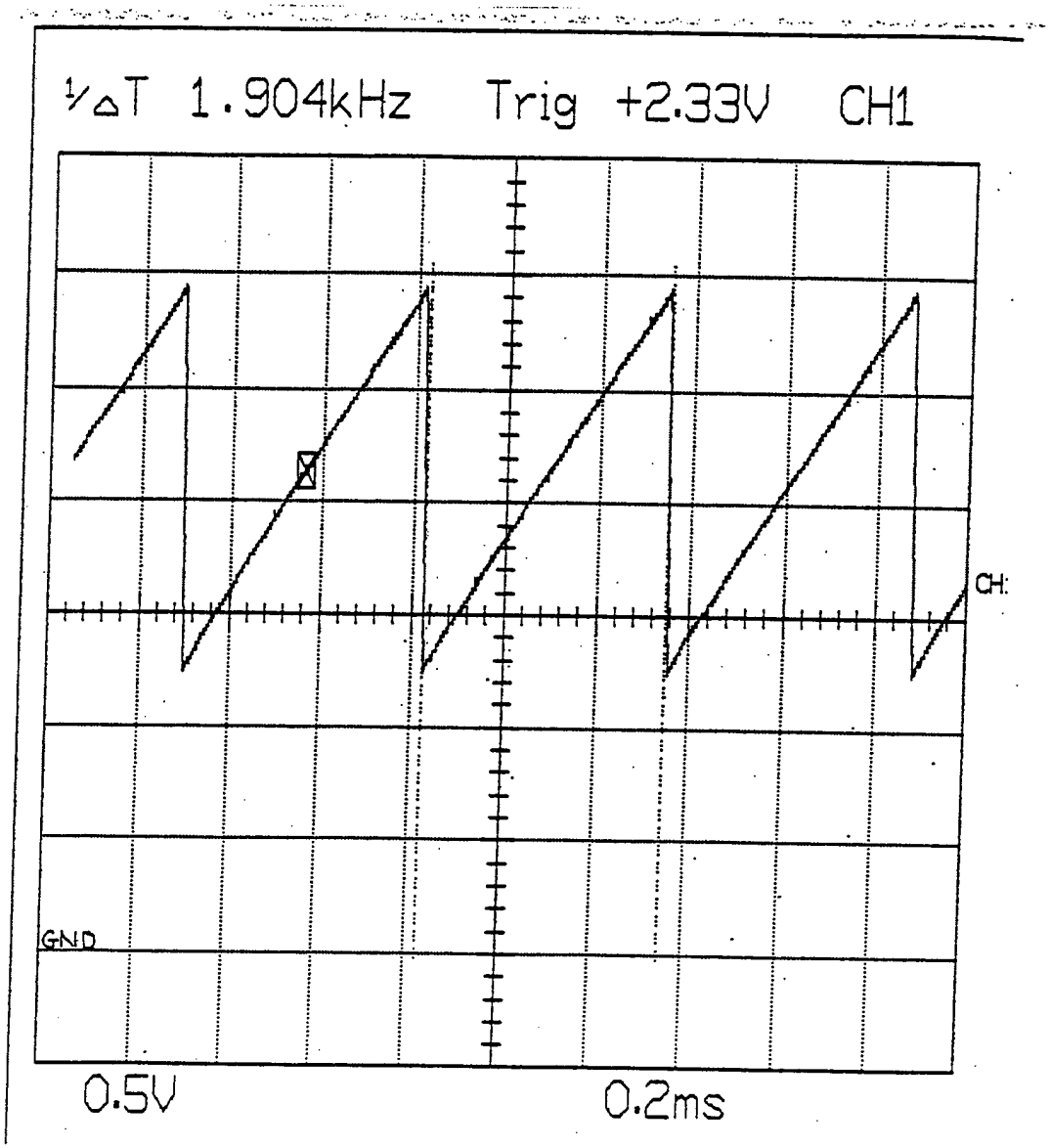

Figure E-1: UC3846 Ramp Waveform,

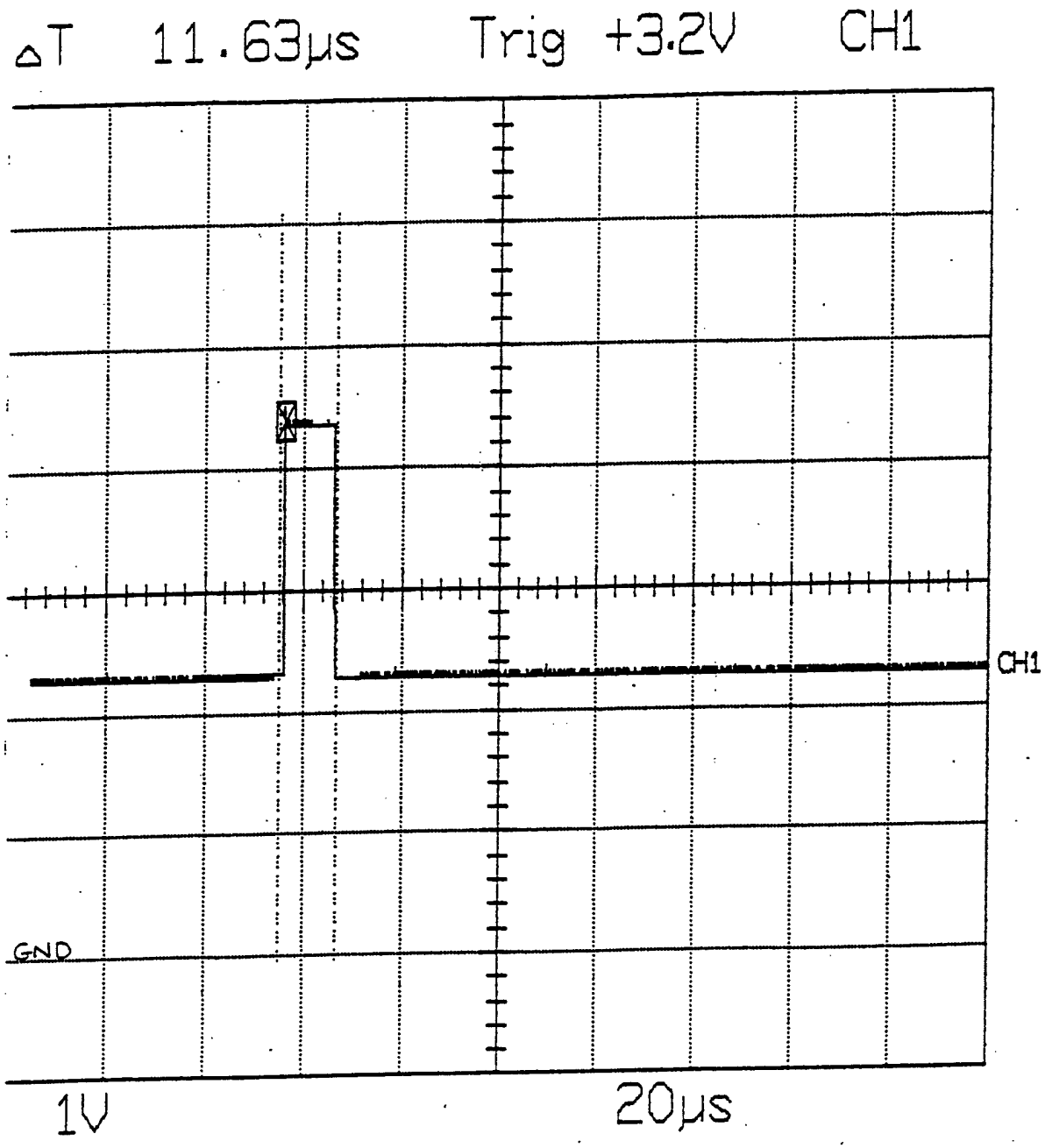

Figure E-2: UC3846 Clock Pulse Waveform

3. UC3846 Schematic

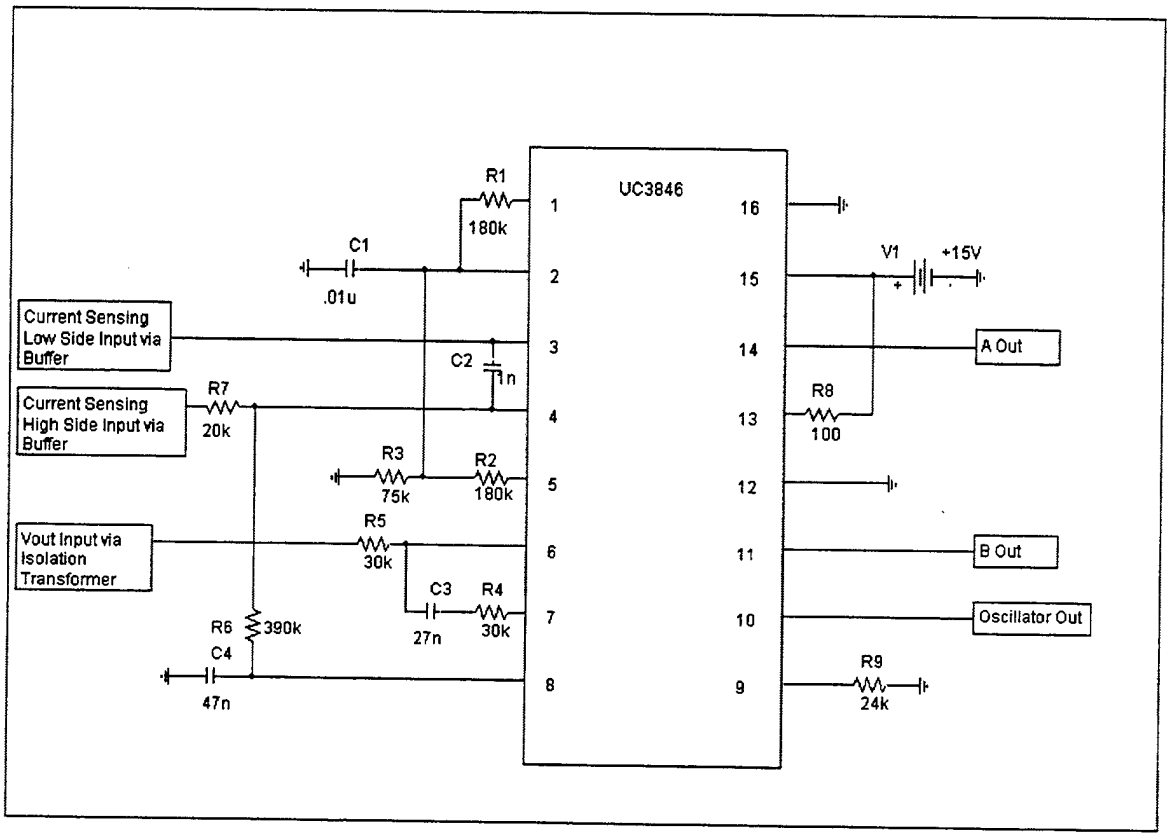

Figure E-3: UC3846 Connection Schematic.

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