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13. ABSTRACT *(Maximum 200 words)*

This program's goal was to develop a writeable RFID tag using an integrated, permeable core coil as the inductor/antenna for communication and power transfer and MRAM as the low write energy, nonvolatile memory. In the final reporting period, wafer processing, to integrate magnetoresistive memory cells with associated electronics, was completed. Success with this integration would demonstrate the memory technology which was proposed for the RFID tag. The IC wafers containing the electronics were completed through metal 1 at the foundry, and subsequent deposition and patterning of magnetoresistive material and metal 2 were completed at Nonvolatile Electronics. Two lots of wafers were processed, and in both cases problems with the inter-metal dielectric, over metal 1, prevented successful completion and testing of the memory devices. Thus, the program finished with successful demonstration of the magnetic memory cell and completion of the RFID tag circuit design, but development of the integrated inductor/antenna and demonstration of an integrated magnetoresistive memory device were not able to be completed within the time and budget constraints of the program.

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LOW COST WRITEABLE RFID TAG WITH MRAM MEMORY

FINAL PROGRESS REPORT

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STATEMENT OF THE PROBLEM STUDIED

The overall goal of this program was to develop a writeable RFID tag, using an integrated coil as the inductor/antenna for communication and power transfer and using magnetoresistive RAM (MRAM) as the low write energy, nonvolatile memory. Success with the integrated coil required the development of a process which integrated a high permeability core with multiple turns of conductor around the core. This would produce the high inductance and magnetic coupling required to power the tag with a remote source. For the writeable aspect of the RFID tag, a nonvolatile, low power memory, which could be written and read using the relatively low power available through the non-contact power source, was required. This program was to demonstrate a magnetoresistive memory which exhibited performance characteristics which are suitable for the RFID tag application.

SUMMARY OF RESULTS

During the course of the program, significant effort was expended on developing a suitable MRAM cell, developing a 3D integrated coil with permeable core, designing a complete writeable RFID tag integrated circuit, and demonstrating an integrated MRAM device (MRAM cell integrated with write and read electronics). At the program end, a suitable MRAM cell had been demonstrated and the RFID tag circuit design had been completed, but processing difficulties prevented the fabrication of permeable core 3D coils and demonstration of an integrated MRAM device.

Details of the MRAM cell were presented in the first interim report, #ARPA06-01, and in the technical report of 28 July 1998. For the integrated MRAM device work, the spin valve (SV) cell detailed in the technical report was chosen. This cell has low write field requirements and two stable states at zero applied field. Two such cells would be used to store one bit of information, with one cell set to each zero field state. On readout, the resistance of the two cells is compared and a "1" or a "0" is output, depending on which of the two cells was in the high reference state. A summary of this SV cell, taken from the technical report, is given in Appendix A.

The second interim report, #ARPA06-02, contained circuit schematics and a description of the RFID tag circuit. This circuit was designed to receive its power through inductive coupling to an integrated permeable core coil and to provide the currents necessary to write the MRAM memory cells. The communication scheme was designed to be compatible with existing RFID systems, but the operating frequency was increased to accommodate the requirements of the integrated inductor/antenna. A description of the RFID tag circuits, culled from the second interim report, is included here as Appendix B.

Both of the interim reports contain information about the development of the integrated, permeable core coil. While the first process experiments, without the permeable core, looked promising, subsequent work was not successful in producing a suitable coil with a permeable core. Despite a number of process and materials changes, the step coverage issue proved to be too much for the process constraints - i.e. no planarization steps. Any future attempts at fabricating integrated permeable core coils will make use of chemical mechanical polishing (CMP) to planarize the wafer surface subsequent to the deposition of the permeable core. A summary of the last reported details of the coil development work, taken from the second interim report, are given in Appendix C.

The final task mentioned above, demonstration of an MRAM cell integrated with drive electronics, was completed in this final reporting period of the program. At the time of the

second interim report, the integrated circuits were being fabricated at an outside foundry. Once completed, the IC wafers were put into NVE's backend process to add the MRAM cells to the electronics. This included deposition and patterning of the magnetoresistive film which is used in the MRAM cell, followed by deposition and patterning of two additional interconnect metal layers. Two lots of wafers were run through backend processing, lot 81202 and lot 82510.

The first lot processed was lot 81202. As received from the foundry, the IC wafers contained one layer of interconnect metal which was patterned, but not covered with an intermetal dielectric. The wafers were ordered this way because past experience showed that the magnetoresistive films did not have optimal properties when deposited on foundry dielectric films. Thus, NVE's first process step was to deposit an intermetal dielectric. While an NVE dielectric could be deposited on top of the foundry dielectric prior to deposition of the magnetoresistive material, this would increase the dielectric thickness, which could lead to worse roughness and topography problems and higher thermal resistance between the MRAM cell and the wafer substrate.

Because the required dielectric thickness was relatively large, a PECVD silicon nitride dielectric, rather than a higher stress sputtered silicon nitride, was deposited. Since NVE's PECVD dielectric process is a low temperature, and, therefore, low density, process, it was felt that it represented a possible stress risk due to densification during any subsequent anneals. Therefore, an anneal was used to increase film density prior to deposition of the magnetoresistive material. Figure 1 shows the surface of one of the wafers subsequent to the anneal.

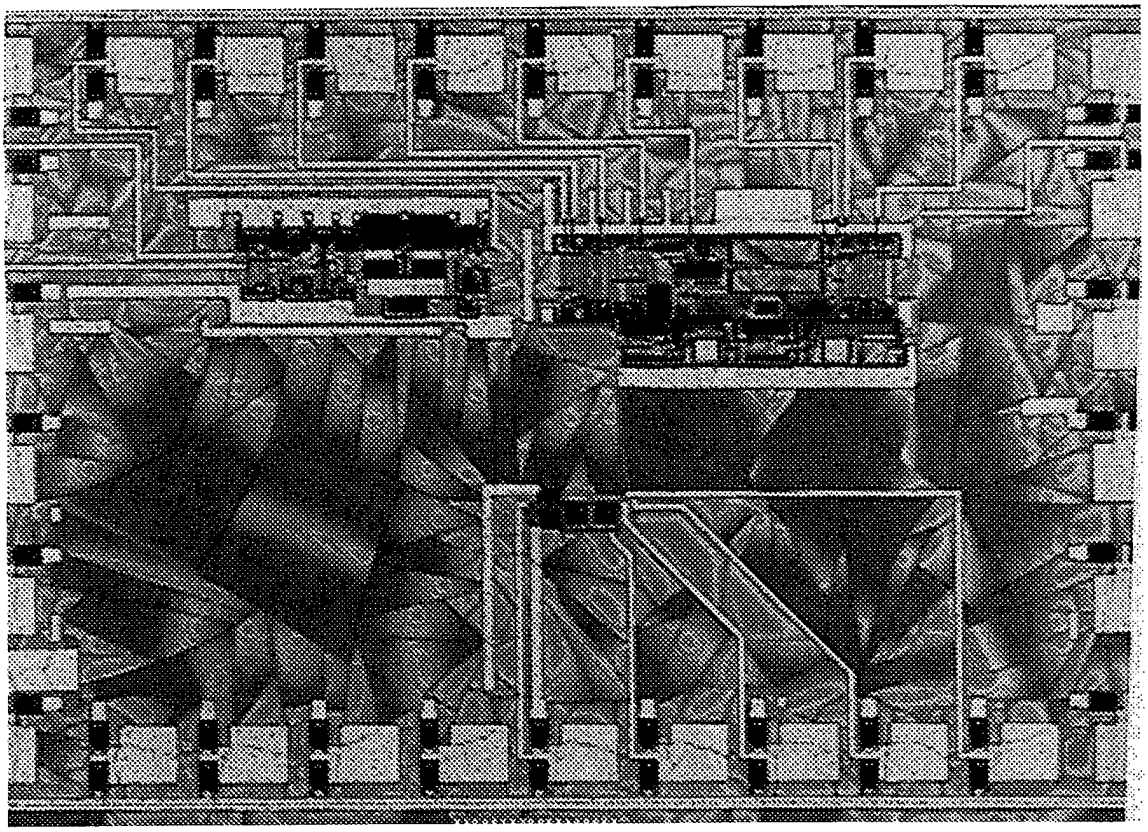

Figure 1. Photomicrograph of the surface of one wafer from lot 81202 following a 30 minute, 450 °C anneal of the 6000Å PECVD silicon nitride. Extreme cracking of the nitride is evident.

Clearly, the anneal produced significant cracking of the silicon nitride dielectric. These wafers were reworked, at this point, by etching the nitride in buffered HF and redepositing a nitride film - but the anneal was not done following the second nitride deposition.

Next, the magnetoresistive film was deposited, after using a pilot wafer to verify that the magnetoresistive material being deposited in the sputter system had the desired properties. A sample magnetoresistance plot for the pilot wafer is given in Fig. 2. As can be seen, the material has two stable zero field states, one high resistance and one low resistance.

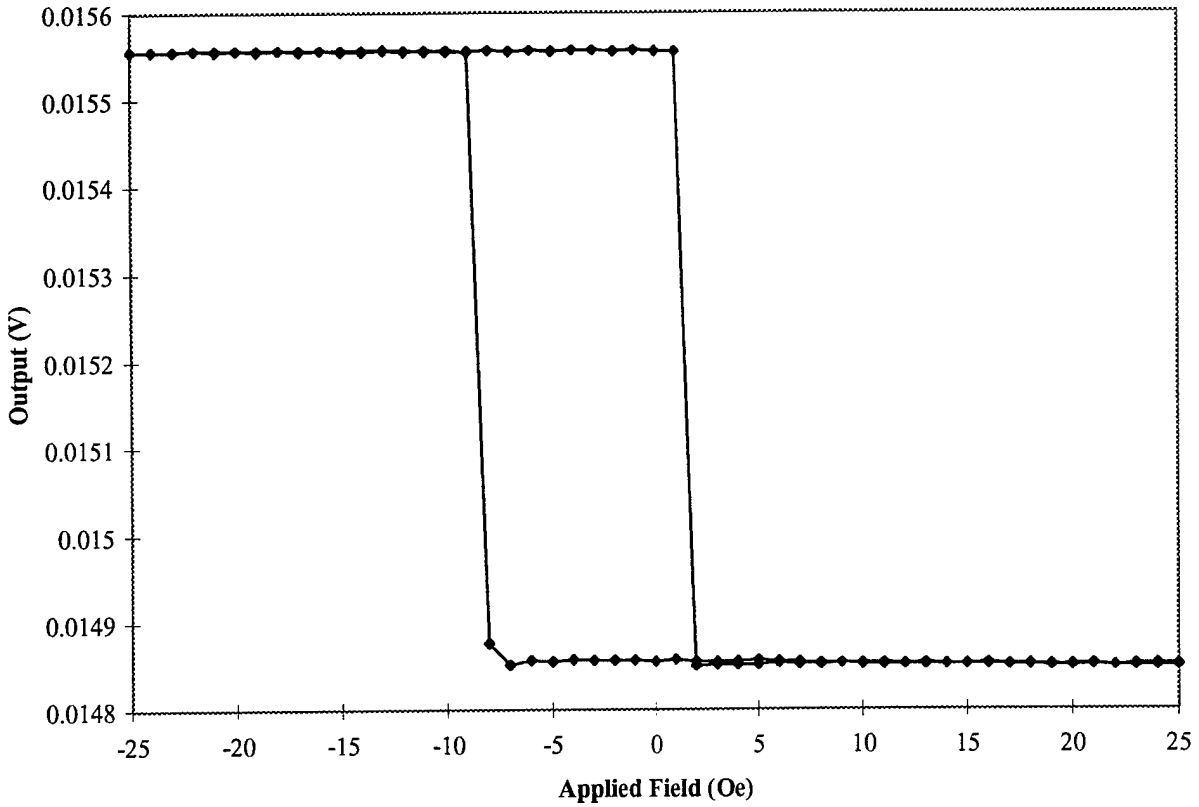

Figure 2. Magnetoresistance characteristic of the SV material used for the integrated MRAM device.

Further processing of lot 81202 brought it to the point that parametric testing could be done on the wafers. At this point, the lot was scrapped because of shorting between the metal layers, unacceptably high switching fields in the magnetoresistive test structures, and opens in other magnetoresistive test structures. These problems were attributed to the cracked PECVD nitride.

The second lot of wafers to be processed, lot 82510, followed essentially the same process as the first lot, except that the post deposition anneal of the PECVD nitride was left out. Again, this lot was processed up through patterning of metal 2 and initial parametric testing was begun. As devices were probed for testing, it became clear that there was a severe adhesion problem between the magnetoresistive film and the PECVD nitride (a problem not seen in the previous lot). An example of the problem is shown in Fig. 3.

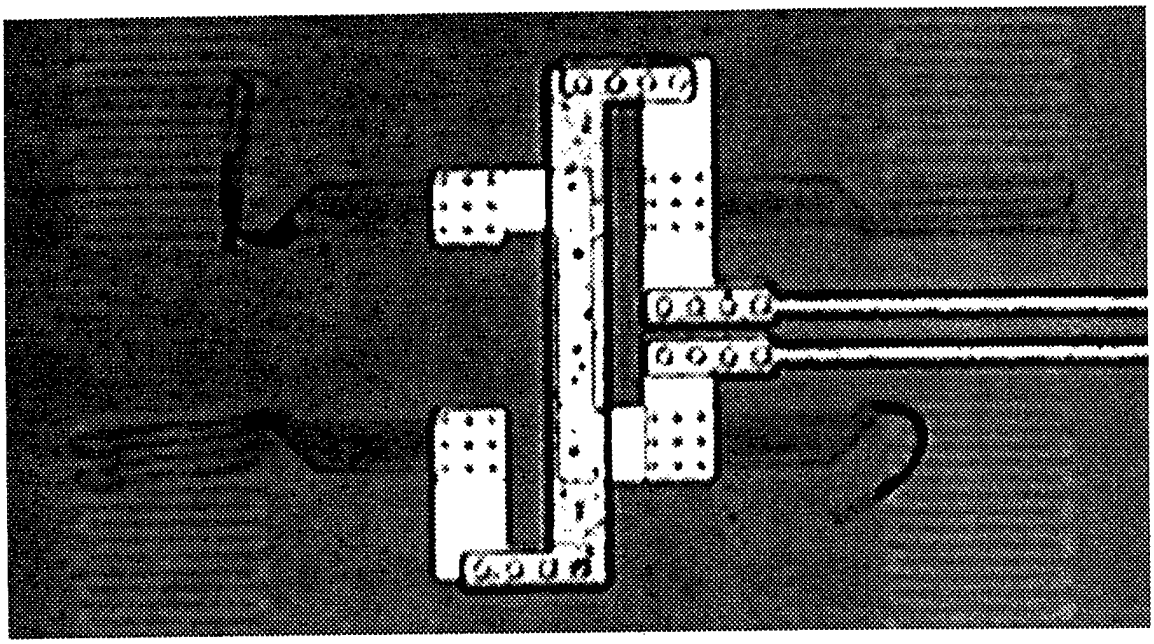

Figure 3. Photomicrograph showing the magnetoresistive film peeling off of the PECVD nitride surface upon which it was deposited. The serpentine shapes in the four corners of this figure are the "shadows" of magnetoresistive resistors in a test structure. Remnants of the magnetoresistive structures can be seen attached to the metal in the center of the figure.

Figure 3 shows that very little of the magnetoresistive material remains attached to the wafer following patterning of metal 2. Clearly, any further work with these devices will require a change in the process to eliminate the adhesion issue. One possibility would be to let the foundry process the wafers through the intermetal dielectric. This would require processing of another lot of wafers at the foundry. NVE would then deposit a relatively thin sputtered silicon nitride film as a base for the magnetoresistive film - a process which has worked in the past with magnetoresistive sensors. Alternately, a thin sputtered silicon nitride film deposited on top of NVE's PECVD nitride might also work.

LIST OF PUBLICATIONS AND TECHNICAL REPORTS

Interim Progress Report	24 March 1997	#ARPA06-01
Technical Report	28 July 1997	
Interim Progress Report	31 March 1998	#ARPA06-02

LIST OF PARTICIPATING SCIENTIFIC PERSONNEL

The scientific personnel listed below were supported, in part, by this project. None of these scientific personnel received an honor, award, or advanced degree while employed on this project.

Mr. John Anderson	Dr. Russell S. Beech	Dr. James M. Daughton
Dr. Brenda Everitt	Mr. David Lee	Mr. Steve Loper
Mr. Scott Mundon	Dr. Arthur Pohm	Mr. Jim Schuetz
Mr. Robert Sinclair	Mr. John Stokes	Dr. Dexin Wang
Mr. Erik Lange		

INVENTIONS

No invention disclosures or patent applications resulted from this program.

APPENDIX A: TWO BIT SPIN VALVE LATCH CELL

The original program plan was to use X-Mode memory cells. A representative diagram of an array of X-mode cells, from reticle 100037, is shown in Figure A1. These types of bits produce characteristic resistance vs. field traces of the type shown in Figure A2. The resistance curves for increasing and decreasing fields cross to form an "X" about the zero field position. The bit is written with either a positive or negative word field pulse, and read by applying, sequentially, both a negative and a positive half-select word field. The signal transitions for a bit read is illustrated in Figure A2. First, a negative word field is applied, and the sense amplifier is autozeroed. Then, a positive word field is applied and the bit resistance either increases or decreases, depending upon which state the bit is in, as indicated by arrows in the figure. The read may also be accomplished using only a single polarity of word read field, although the signal will be reduced. For this mode of operation, fairly high fields are necessary, up to about 60 Oe to write, as shown in Figure A2.

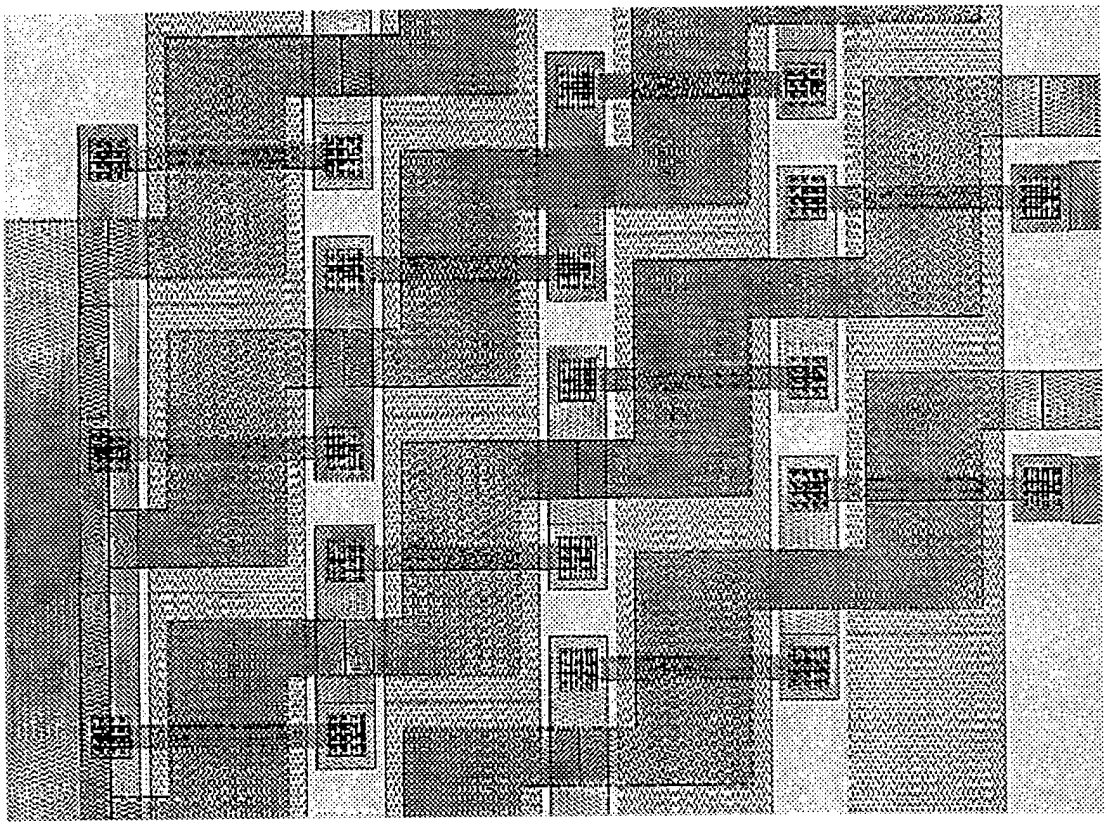

Figure A1. Typical array from reticle 100,037. Bits are connected in series along each sense line. Read and write fields are generated from two sets of word line conductors patterned over the top of the bits.

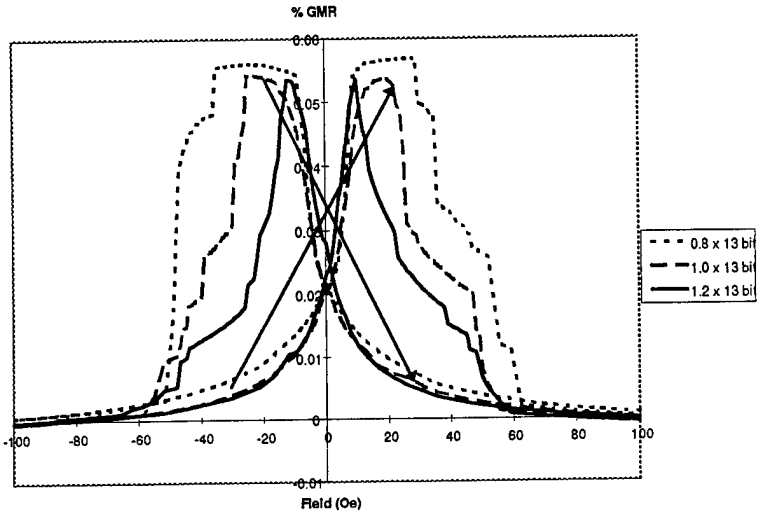

Figure A2. GMR vs. field characteristic for three sizes of "X-mode" style bits. A read operation is indicated by arrows: first, the sense amplifier is autozeroed at negative word field. Upon application of a positive word field, the bit resistance either increases or decreases, as shown. These bits are written by application of word fields in the 40-60 Oe range.

The new memory cell uses two spin valve (SV) bits, that exhibit two stable resistance states at zero field, which are part of a latch circuit. With the two bits set to opposite states, one high resistance and the other low resistance, a latch circuit, which is initially forced to a balanced state by a strobe pulse, will latch to one state or the other depending on which bit is high (a similar latch cell can be made with X-mode bits, but a word current would be required to drive the bits to high/low resistance state during the read cycle). Figure A3 illustrates the magnetoresistance characteristic of an FeMn pinned SV material which could be used for this application - in particular, note the two resistance states at zero field. In addition to the two states at zero field, the SV bit also writes at a relatively low field - about ±15 Oe in Fig. A3. This is only about 1/4 of the field required to write the X-mode bits.

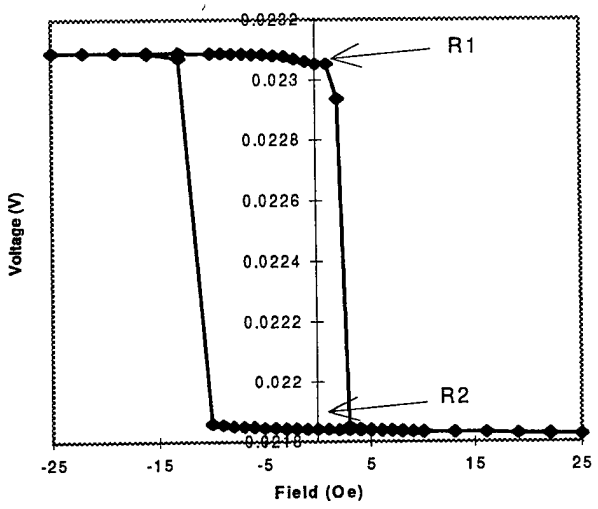

Figure A3. Minor loop for as-deposited spin valve material. At zero word field, two possible resistance states (R1 and R2) are present. The state is written by applying word field of ±15Oe. No word field in necessary to read the cell, making this the lowest power MRAM cell alternative for the RFID tag program.

A schematic diagram of the SV latch cell is shown in Figure A4. The two SV bits show up in series with the sources of the n-channel devices in the latch circuit. The two halves of the latch are shorted together, bringing them into balance, when the AZ line is activated. When the AZ line is turned off, the latch switches to one state or the other depending on which of the two SV bits is in the high resistance state. Power is consumed only during this latch operation, not in steady state, and no word line current, to drive the bits, is required - making this a very low power circuit.

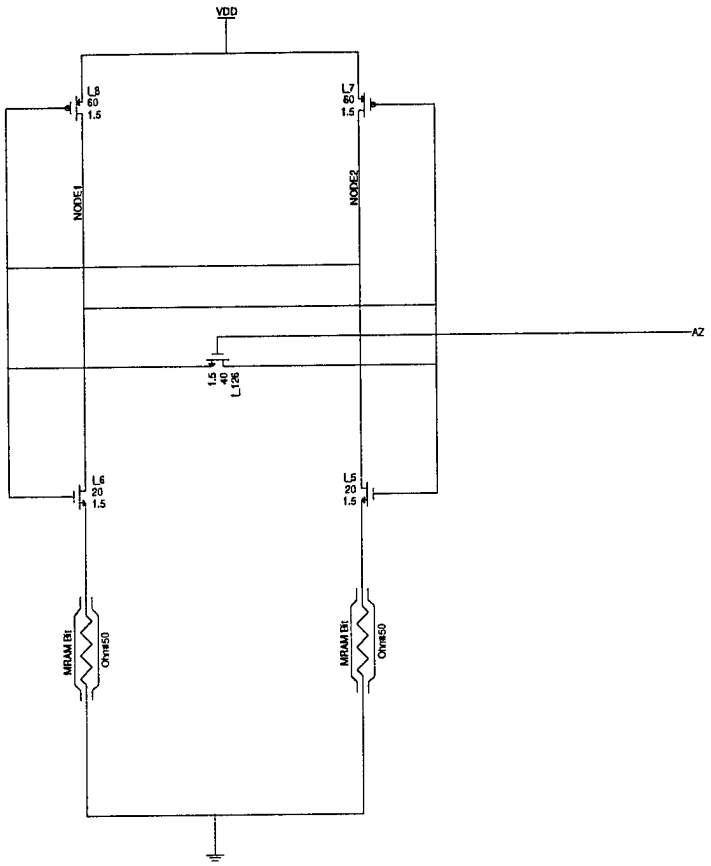

Figure A4. Schematic of a SV latch cell.

APPENDIX B: RFID TAG CIRCUITRY

The following sections detail various circuit blocks and functions of the overall RFID tag integrated circuit design.

Wireless Interface - Preliminary design work included the breadboard of a wireless interface using discrete components for the purpose of developing design requirements. The breadboard employed bipolar NPN and PNP devices connected in a simple inverter configuration to drive an energy pulse into a tuned LC circuit. A coil two (2) inches in diameter with 35 turns yielding an inductance of approximately 10uH was wound as the primary coil on the reader/writer side of the wireless interface. A capacitor tuned the LC circuit to the carrier frequency of 400KHz. Amplitude modulation of the carrier signal was demonstrated through pulse width modulation of the input pulse to the drive inverter.

The RFTAG side of the wireless interface was breadboarded using an LC circuit interfaced to a full wave rectifier. A coil 1.5" inches in diameter with 120 turns yielding an inductance of approximately 100uH was used as the receive coil. A capacitor was used to tune the LC circuit to the carrier frequency of 400KHz. The receive coil was excited via the magnetic field generated by the transmit coil, the output of the full wave rectifier was monitored. Distance versus DC voltage output of the rectifier was considered. Results indicate that a DC voltage exists at the output of the full wave rectifier sufficient to power the RFTAG at a distance of approximately 6 to 8 inches depending on the alignment of the coils. Within this distance an integrated voltage regulator will regulate the voltage to the desired +5VDC required by the RFTAG.

The final design of the wireless interface is dependent on the actual power dissipation and demodulator characteristics of the RFTAG. Once the necessary parameters have been characterized the size and drive requirements of the coils can be derived. It is anticipated that only minor iterations of the breadboard design will be required.

RFTAG System Overview - The RFTAG is designed to be totally integrated and powered by an on-chip power supply energized by the external coil and capacitor of the wireless interface. The external resonant circuit is tuned to the carrier frequency of 400KHz. Data transmission occurs through amplitude modulation (AM) of the carrier at a 50KHz rate. In the case of a write operation the data is demodulated and decoded prior to storage in a 256 bit memory array. An additional 16 bits are reserved for storage of a header or checksum bring the total on chip memory to 272 bits. In the case of a read operation the data is sequentially clocked out of the 272 bit array in packets of four (4) bits. A fifth bit is inserted into the packet by an even parity bit generator. The data including the parity bit is then PSK encoded and transferred to the modulator. The modulator shunts the resonant circuit reflecting energy back to the reader/writer unit where it is detected. A conceptual system block diagram of the RFTAG is presented in Figure B1. The following sections briefly discuss the functionality of each block.

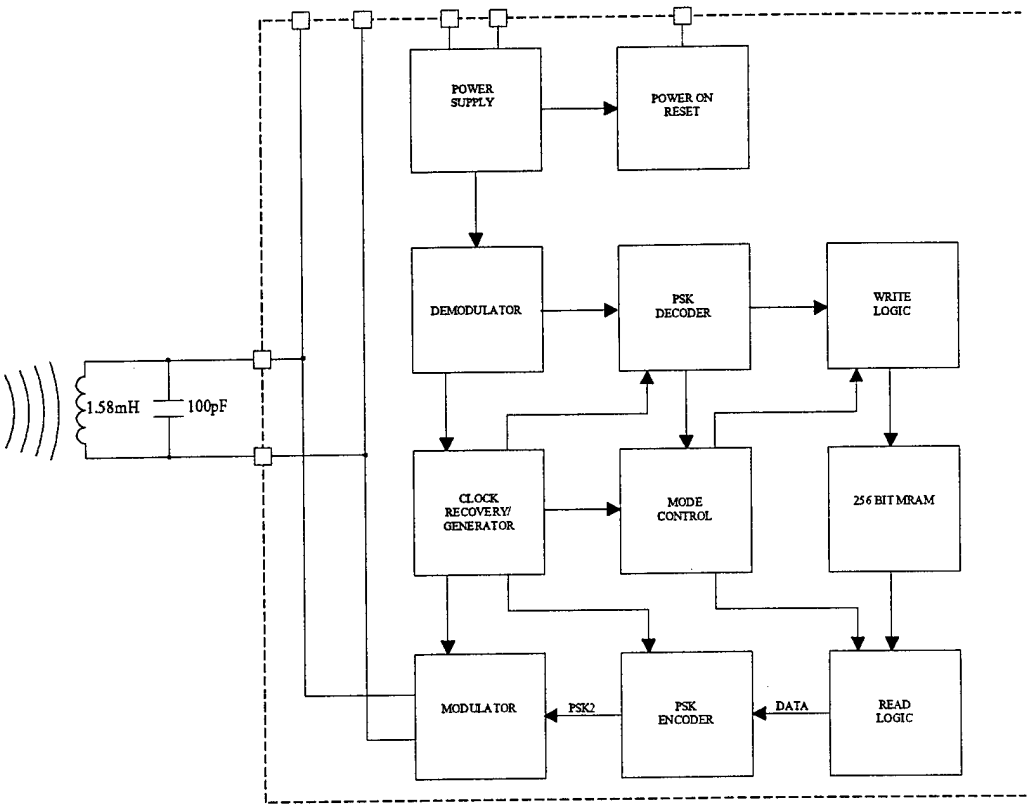

Figure B1. RFTAG system block diagram, showing external tuned LC resonant circuit for wireless interface.

Power Supply - The power supply is essentially a full wave rectifier followed by a voltage regulator designed to supply a regulated +5VDC to the RFTAG circuitry. The power supply interfaces directly to the LC circuit of the wireless interface. An on chip capacitor of 200pF is required to hold up the supply voltage to within a 0.5 V drop during each write to the memory array. This is based on a write pulse of 5ns supplying approximately 20mA through an integrated coil. The power supply is also bonded out such that the RFTAG can be powered from an external battery. Battery operation will be usefully during initial tests.

Power On Reset - The power on reset circuit holds the master reset line low while the supply voltage ramps up to its regulated voltage level. A logic "low" on the master reset initializes all registers to a known state.

Demodulator - The demodulator filters the 50KHz data from the amplitude modulated signal received by the tuned resonant circuit and converts it into a digital bit stream. This is accomplished by a two stage 4^{th} order switch capacitor Butterworth bandpass filter followed by a digital output comparator shown conceptually in Figure B2 as a continuous time domain circuit.

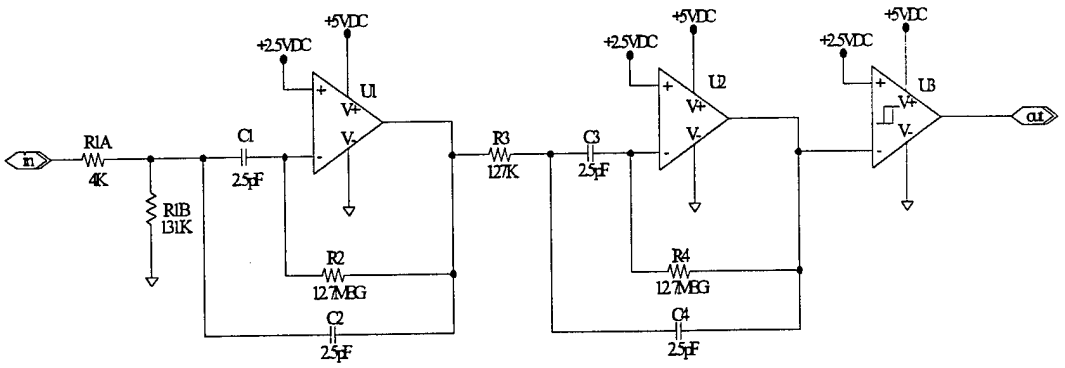

Figure B2. Demodulator shown conceptually as a continuous time domain circuit. A two stage 4th order Butterworth bandpass filter and an digital output comparator provide the demodulation.

The first stage attenuates the 400KHz carrier frequency by approximately 15dB allowing the 50KHz frequency to pass through unattenuated. Attenuation of the 400KHz in the first stage is important to prevent saturation of the amplifiers. The second stage further attenuates the 400kHz by approximately 5dB and amplifies the 50KHz data signal by 10dB. The filtered signal is input to a comparator which converts the 50KHz sinusoidal waveform to a digital output.

In the actual circuit implementation the resistors are replace by switched capacitors. The size of the capacitors are determined by the following relationship to the sample frequency,

$$C = \frac{1}{f_s R}.$$

Each filter stage is design to have a Q value of 5. The capacitors are selected to be of a size (2.5pF) that are easily fabricated in an integrated design. Then equivalent resistor values are determine from the following design equations,

$$R_2 = \frac{Q}{\pi f_c C} \quad \text{and} \quad R_1 = \frac{R_2}{4Q^2},$$

where R1 is the equivalent input resistance and R2 is the feedback resistance. Using a center frequency of 50KHz for the bandpass filter response and the above equations the equivalent resistor values are determined to be R1=127K ohms and R2=12.7MEG ohms.

To achieve the desired attenuation at 400KHz through the first stage a simple resistor divider is employed to adjust the gain amplitude of the frequency response to the desired level.

The amplifiers employed in the integrated design are fully CMOS Operational Transconductance Amplifiers (OTA) shown schematically in Figure B3. The amplifier is designed to drive a 5pF load while providing 47dB of open loop gain with a phase margin of greater than 75 degrees at unity gain. The open loop frequency response of the OTA is shown in Figure B4.

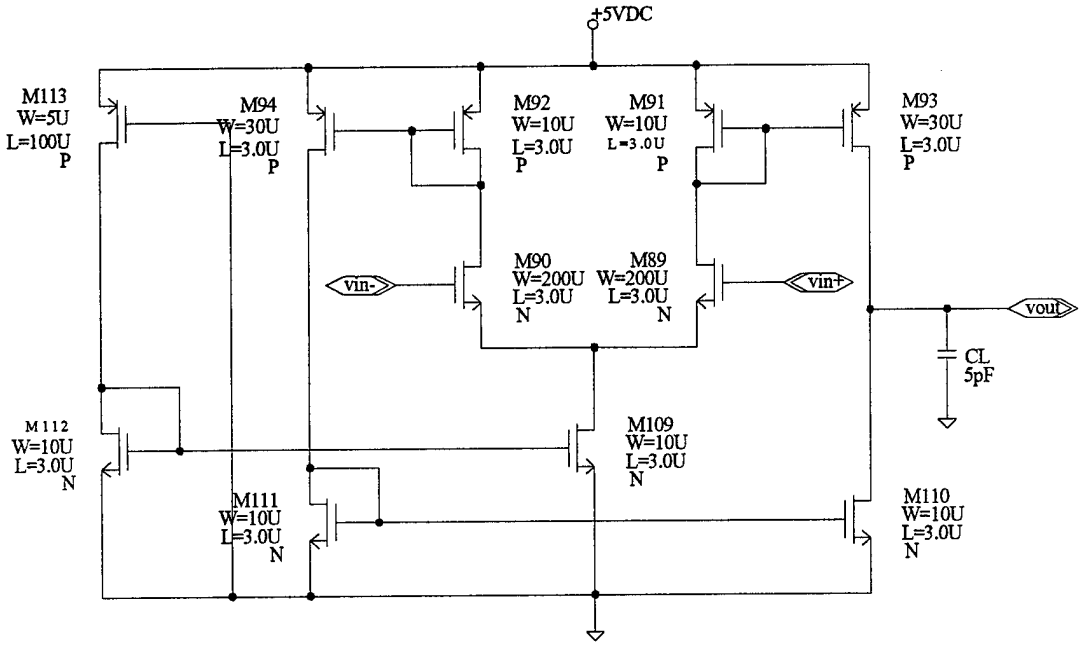

Figure B3. Operational Transconductance Amplifier (OTA) employed in the demodulator filter stages.

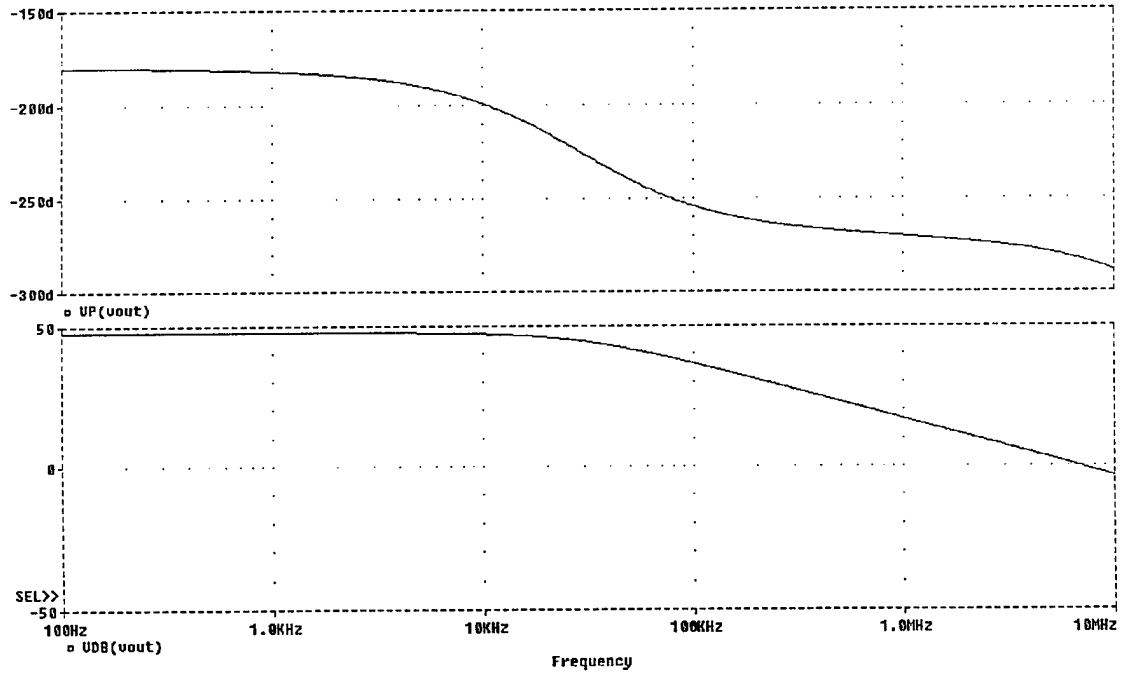

Figure B4. Open loop frequency response of OTA driving a 5pF load.

The digital output comparator employed as the final stage of the demodulator uses the same OTA design with additional cross coupled PMOS devices providing positive feedback for hysteresis.

Clock Recovery/Generator - The 400KHz carrier of the wireless interface is extracted and used as the master clock for timing control of the RFTAG integrated electronics. The signal, after the full wave rectifier but prior to the voltage regulator, is input to a CMOS comparator. The high gain of the comparator converts the 400KHz sine wave to a CMOS level output. The 50KHz modulation of the carrier signal is not sufficient to trigger the comparator output. Hence, the comparator outputs a 400KHz master clock.

The master clock is divided down by a five (5) bit counter generating lower frequency clocks. The lower frequency clocks are use throughout the RFTAG electronics to ensure synchronous timing of control pulses.

PSK Decoder - The PSK decoder is required to decode the PSK formatted data received from the reader/write unit after passing through the demodulator of the RFTAG. The PSK encoded data ensures reliable transmission across the wireless interface in the event of consecutive "zeros" or "ones". Figure B5 shows an example of PSK encoded data.

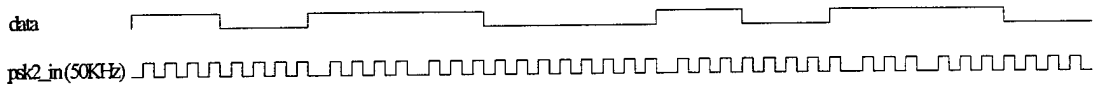

Figure B5. Example of PSK encoded data, where each phase shift corresponds to a logic "one" in the input data.

A 180 degree phase shift of the 50KHz modulated output corresponds to a logic "one" in the input data. The PSK decoder detects the phase shift of the encoded data by comparing it to a continuous 50KHz clock generated by dividing down the 400KHz clock. The change in phase of the encoded data generates a pulse width variation. A narrow pulse is generated when the two signals are in phase, representing a logic "zero". A wide pulse is generated when the signals are out of phase, representing a logic "one".

Write Logic - The write logic, when triggered, generates a 2ns pulse that drives the input to the H-bridge of the selected memory bit. The pulse is applied to the appropriated side of the H-bridge depending on rather a "zero" or a "one" is to be written.

Read Logic - The read logic, when triggered, generates a 5ns auto-zero pulse to the selected memory bit. The pulse auto-zeros the flip-flop and triggers a read operation of the bit.

Memory Array - The memory is organized into 16 identical columns of 16 bits each, forming a 256 bit memory array. An additional column is added for storing a 16 bit check sum bring the total number of memory bits to 272. The support electronics is organized such that each bit in a column shares a common H-bridge and auto-zeroed flip-flop for performing write and read operations, respectively. The read/write operations are performed by selecting a column and multiplexing between the 16 bits within the selected column. An address decoder is included in the design to sequentially select columns and rows of the memory array.

Mode Control - The mode control block is the main discrete timing block of the RFTAG. The mode control block determines from the decoded data if a start condition has been received. The start condition is the occurrence of nine (9) consecutive "ones". The data is transferred across the wireless interface in packets of five bits. The packet consists of four (4) data bits and one (1) parity bit. The even parity bit ensures the start condition will never occur during data transmission. Once the start condition has been received the next received bit indicates a read or a write condition.

If a write condition has been received the data to be written shall follow. As the 256 bits of data are received by the RFTAG it is sequentially written into the memory array along with a 16 checksum. During actual system operation the reader/writer unit would immediately follow a write with a read. A compare will be performed to determine if the data read from the RFTAG is what was intended to be written. In the field the reader/writer will not have the actual data stored to compare with what is in the RFTAG. During these operations several checks have been put in place to help detect with a high degree of confidence if the data has been successfully transferred.

First, the data is transmitted from the RFTAG in packets of 5 bits, the same format used to perform the initial write operation. The even parity bit is generated by the parity bit generator integrated in the RFTAG. Next, the reader will receive the data and verify through a parity check that the data has been successfully transmitted via the wireless interface. The reader will also calculate the checksum of the data and verify against the checksum received from the RFTAG. This process will detect most transmission errors or determine if the RFTAG memory has been corrupted. In either case the user shall be alerted that the integrity of the received data is suspect.

Parity Bit Generator - During a read operation the stored data is sequentially clocked from the memory array in packets of four (4) bits. The four bits are passed through the parity bit generator where an even parity bit is generated and inserted into the serial data stream.

PSK Encoder - Prior to transmitting the data via the wireless interface the serial data stream must be PSK encoded. This is to ensure reliable transmission in the event of several "zeros" or "ones" in a row. Refer to Figure B5 for an example of PSK encoded data. In the RFTAG the PSK encoding is accomplished by modulating the data at 50KHz, then creating a phase shift of 180 degrees upon each occurrence of a "one".

Modulator - The data is transmitted via the wireless interface by shunting the LC resonant circuit continuously being excited by the 400KHz carrier from the reader/writer unit. Shunting the resonant circuit causes a reflection of the energy stored in the circuit back to the reader/writer where it is detected. To achieve this a single MOS device is connected to the resonant circuit. When the device is off the circuit resonates as desired. During data transmission from the RFTAG the gate of the MOS device is driven with a low duty cycle pulse. During the pulse the MOS device is turned on and momentarily shunts the LC resonant circuit causing the dissipated energy to be reflected back to the reader/writer receiver coil.

APPENDIX C: PERMEABLE CORE INTEGRATED COIL

During calendar year 1997, processing was completed on two coil lots, 64509 and 64605, and three additional lots were processed: 70613, 71810, and 72512. None of these lots resulted in working, permeable core coils, as was the goal of this coil development. The final lot, 72512, was only partially completed, with two of the twelve wafers in the lot completing the entire process. At that point, this portion of the program had exceeded its planned budget and further coil processing/development was suspended so that funds and effort could be expended against development of the tag memory and circuitry.

Lots 64509 and 64605 both used a polyimide insulating layer to cover the permeable core prior to deposition of the top windings. For lot 64509, difficulty was encountered in clearing the vias down through the polyimide to the first metal windings. This resulted in unacceptably high resistances for the coils - up to 50 kΩ.

Lot 64605 utilized plating in the vias to minimize the step coverage issues with a single, deep via cut after the core was formed. This technique required that the vias be opened during the permeable core plating steps. As the core was being plated, small "pillars" were plated on all of the vias. Thus, the top winding did not have to drop into a via which was slightly deeper than the height of the core. Instead, the top winding connected to vias which were at essentially the same level as the top of the core. Resistance measurements from these devices were more in line with the expected results, and those from the initial coreless lot, 64508 (data on this lot was presented in the previous report). One of the devices was probed from winding to winding in order to check the uniformity of resistance from one turn to the next. A plot of this data shows that the resistance rises linearly as the probe point moves down the length of the coil and the resistance difference from one turn to the next averages about 2 Ω.

A few devices from the 64605 lot were packaged for further testing. Some devices were given to Omni ID, a program subcontractor, for magnetic coupling evaluation. When subjected to the interrogation signal of a typical RFID reader, however, the 64605 coils did not generate an appreciable signal as was expected, and required. While the resistance of the coils was somewhat higher than ideal, it was not so high as to cause the poor results. One possibility is that there was shorting between the top windings so that the devices did not really have conductive turns encircling the permeable core.

In order to better evaluate whether or not the devices being fabricated are really coils as desired, subsequent lots, 70613, 71810, and 72512, included a GMR film. The reticle set being used contains a GMR bridge sensor with biasing coils. By including the GMR film deposition and patterning when processing the coil lots, it is possible to use the biased bridge to check the coil fabrication. If the coil processes properly, then the GMR bridge resistance will vary in response to a current in the bias coil. If, instead, the coil is shorted between the top windings, then no GMR response is expected when current is passed through the coil terminals.

The first two lots with GMR, lots 70613 and 71810, suffered from contact problems between the top windings and the bottom windings. Neither of these lots yielded any working devices. Based on compositional analysis of the bottom of the vias, as well as how they looked visually, it appeared that seed layer residue was hindering the etch of the polyimide - a sputter deposited seed layer is used for plating both the core and the top windings, this seed appears to become embedded in the polyimide, which is not completely cured because of the temperature restrictions of the GMR material, and subsequently hinders the via etch. At this point, a method of using sputtered nitride rather than polyimide for the core dielectric was conceived.