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DEVELOPMENT OF ADVANCED TECHNOLOGY FOR 2000 LPI HEAD-MOUNTED DISPLAYS

by

Ollie C. Woodard

Kopin Corporation
Taunton, MA 02780

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Ollie C. Woodard

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Kopin Corporation
695 Myles Standish Blvd.
Taunton, MA 02780

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13. ABSTRACT *(Maximum 200 words)*

Operational 2560x2048 active matrix liquid crystal displays (AMLCD) and operational 1280x1024 active matrix electroluminescent displays (AMEL) were demonstrated. Manufacturing technologies were developed for high resolution active matrix displays made in both electroluminescent and liquid crystal formats, extending the state-of-the-art from 1280x1024 pixel (1000 lines/in) to 2560 x 2048 pixel (2000 lines/in) displays. The 2560x2048 displays have12 μm pixel pitch and a 1.5 in. screen diagonal. On-board circuits, which include video decode, row and column scanners and the pixel TFT's, contain over 5,000,000 transistors—the equivalent of a large scale integrated circuit. The program provided breakthrough display technologies, which are now used in both AMEL and AMLCD display manufacturing processes. 2000 LPI displays for Head-Mounted Display applications are in development.

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PREFACE

This project was funded by the Defense Advanced Research Projects Agency (DARPA) under BAA94-04 to continue AMEL/AMLCD DARPA Head-Mounted Display(HMD) development program. Manufacturing technologies were developed for high resolution active matrix displays made in both electroluminescent and liquid crystal formats, extending the state-of-the art from1280 x 1024 pixel arrays with 1000 lines/in (LPI) to 2560 x 2048 pixel arrays with 2000 LPI. The program provided breakthrough display technologies which are now used in both AMEL and AMLCD display manufacture. Operational 2560x2048 AMLCD displays and operational 1280x1024 AMEL displays were demonstrated.

This program involved a number of organizations that collaborated to attain the project goals. The technical work was carried out by Kopin [Prime Contractor, providing project integration, Silicon-On-Insulator (SOI) materials, AMLCD design and assembly], Sarnoff (active matrix circuit design, process design), Planar (EL processing), Allied Signal (IC foundry for AMEL circuits), MIT Lincoln Laboratory (IC processing of AMLCD circuits). Honeywell was responsible for development of the HMD display through its parallel Combat Vehicle Crew (CVC) HMD contract. Display characterization and consulting was provided by the U.S. Army at Ft. Monmouth and Natick RD&E Center.

The Program Managers were Dr. Mark B. Spitzer (now CEO of MicroOptical Corp) and Mr. Ollie C. Woodard, Sr. (Kopin Corporation). Mr. Patrick Green managed the Planar 2000DPI display subcontract. The Principal Technology Expert and VLSI Specialist was Dr. Alfred C. Ipri (Sarnoff). Dr. Ipri also served as the Project Manager of the Sarnoff subcontract and was responsible for display designs and process development. Dr. Bor-Yeu Tsaur was responsible for the final 2560x2448AMLCD design and fabrication. Mr. Danny Kagey headed the subcontract team at Allied signal which fabricated 12 um test pixel arrays and produced the 2000DPI AMEL displays. Mr. Henry Girolamo (U.S. Army Soldier and Biological Chemical Command) provided essential guidance and management through the course of the program. Other key participants included:

AlliedSignal:
Mr. G. Becker - process development
Dr. T. Keyser - process development

Honeywell:
Mr. M. Helgeson - HMD applications

Kopin:
Mr. M. Zavracky - Systems engineering
Dr. Frederick Herrmann -display design

Planar:
Mr. W. Sproull - Program Manager
Mr. L. Arbuthnot- display debug
Mr. K. Ping - Planar Staff

Sarnoff:
Mr. Roger Stewart - Project Management
Dr. H. Eric Kim - display design
Dr. F.-L. Hsueh - display design
Mr. F. Cuomo - display design

And many others

The Project Team has a special debt of gratitude to Mr. E. C. Urban of DARPA/ESTO for recognizing the importance of silicon-based, miniature displays, and for funding and managing this work.

SECTION 1

EXECUTIVE SUMMARY

1.0 Introduction:

This document is the Final Report for DARPA contract MDA972-94-C-0023. This work was carried out between May, 1994 and November, 1997. The work comprised the development of both advanced active matrix electroluminescent (AMEL) and active matrix liquid crystal displays (AMLCDs) for use in head-mounted display (HMD) systems. In this introduction, we will review the specific objectives of the program, as well as the overall results. Subsequent sections will review the research and development with a discussion of the findings of the program.

This project directly addressed the DOD need for advanced displays for HMDs in both the active matrix electroluminescent (AMEL) and active matrix liquid crystal display (AMLCD) technologies.

The principal objective of this program was the design, fabrication, and delivery of advanced high resolution, 2000 LPI (lines-per-inch) displays made using electroluminescent and liquid crystal technology. This work was highly successful, and will result in the delivery of advanced prototype displays to DARPA and to the Armed Services for potential use in military, commercial and consumer personal display systems. Having established the importance of using single crystal silicon (x-Si) for miniature displays in previous DARPA contracts, this work achieved the 2000 LPI resolution goal and extended pixel array sizes to 2560x2048, a total of 5,242,880 pixels. Drive circuitry is integrated with the active matrix circuits on the display glass resulting in single "chip" display circuits with the electronic complexity of large scale integrated circuits. These displays, which have a 1.5" diagonal dimension, have over 5,000,000 transistors on the glass, the electronics equivalent of a large microprocessor chip.

This project was preceded by the DARPA project carried out by the same team: Demonstration of Advanced Flat Panel EL and Liquid Crystal Head Mounted Displays Based on x-Si Thin-Film Transistors. This project produced 1280x1024 displays with 1000 LPI resolution and established the viability of using single x-Si circuits for displays, thereby exploiting their performance advantages over amorphous silicon and polycrystalline circuits used by other display manufacturers. The CMOS based circuit designs also take advantage of established IC foundry operations to manufacture the display circuits more economically.

DARPA project DAAK60-94-C-0016: Development of Support Technology For Color AMEL and AMLCD Head-Mounted Displays produced operational 2000 LPI, 1280x1024 AMLCD displays using a "shrink" version of the 1000 LPI design thereby proving the feasibility of 2000LPI displays. The second task addressed the assembly processes required to assemble AMLCD's with 12 μm pixels. Narrow (2 μm) gap assembly processes and new liquid crystal (LC) formulations were developed. A tri-color backlight was developed by ILC which provides narrow color spectra and reduced

background for better color gamut and reduced power requirements. Current, additional funding was provided to ILC for delivery of advanced lamps to Armstrong Laboratories. In the fourth task, a color filter process was also developed which allowed the integration of the color filter process steps into the AMEL and AMLCD display circuit processes. Filters are fabricated directly on to the active pixel areas to eliminating alignment problems and to extend viewing angles.

A parallel TRP project for AMEL product insertion is being conducted by Planar.

This project and the related projects outlined above have developed a rich repertoire of enabling technologies for the rapid insertion of high resolution miniature displays into military systems.

1.1. Technical Rationale for a 2560x2048 Array of 12 μm Pixels

The design, development and manufacture of advanced HMD systems continue to require displays with smaller and smaller pixels, owing to the ever increasing need for high resolution and small size. In analyzing the requirements for high resolution, two related factors must be considered: data resolution, and field of view. By data resolution, we mean the total pixel count that must be displayed to present completely at the image plane the level of detail in the data supplied to the display. The maximum miniature AMLCD array size available is Kopin's 1280x1024 developed under the previous DARPA contract. Now there are applications for larger arrays. Digitized still imagery displays are desirable at higher levels of resolution such as for highly detailed map, terrain photography or other imagery. Additionally, Forward Looking Infrared (FLIR) detectors and other active sensors are in development may exceed the 1280x1024 standard by a wide margin (for example, a Night Vision 2000 by 2000 I^2CCD). Thus, as high resolution sensor development matures, it will be necessary and desirable to have displays capable of providing the images in an HMD; however, there is a human factor issue that arises as pixels are added to the display. Since the displays must fit near the eyes with minimal mirrors and lenses, the displays must be less than or equal to about 1.5"x1.5" (the size selected for the 1280x1024 displays for this reason). Therefore, to add pixels, one must make the pixels smaller to fit more in a given area. To advance from 1280 columns to 2560 columns, we reduced the pixel size from 24 μm to 12 μm to maintain the desired 1.5" format.

The second factor that must be considered is the field of view (FOV) within the goggle system. Considering the Combat Vehicle Crew Head-Mounted Display (CVC HMD) goggle (the baseline demonstration platform defined for the 1280x1024 display developed), a 40 degree diagonal FOV, with 1280x1024 pixels (1639 diagonal pixels) resulted in a Snellen acuity of about 20:40. An acuity of nearly 20:20 can be attained by using the new 2560x2048 display with four times the pixel count, a highly desirable improvement for HMD's. Our objective is to attain this improvement by providing a display with 2560x2048 pixels (3200 pixels diagonal) for insertion in the demonstration platform.

A third factor affecting the need for small pixels involves the manufacture of color displays of lower resolution. Requirements for color 1280x1024 display could be satisfied with a display based on 12 μm pixels (grouped in a quad to form a 24 μm color pixel). The color filter fabrication technology developed is illustrated in Section 3, figure 3-9. Red, green

and blue filters are placed directly on to the active pixel areas by photolithographic processes as an integral part of the wafer fabrication process.

1.2. Specific 2000 LPI Advanced Display Technology Development Objectives

The specific objective of this program is the development of new high resolution (2560x2048) display technology and the delivery of prototype displays. Through collaboration with Honeywell, the team developed optical, electrical and mechanical interface specifications for demonstration of the display technology in a goggle platform. Technology transfer to manufacturing facilities is spawning new display products for both military and commercial applications.

The technology development required to develop 2000 LPI displays was the further development of high density single crystal silicon circuit based AMEL displays and AMLCD's. Using the 1280x1024 pixel display project results as a base, research was carried out on display design, pixel development, transistor development, integrated circuit processing, and process compatibility.

The common display specification goals for AMEL and AMLCD displays are summarized in Tables I-1. However; Table I-1 does not reflect AMEL project redirection by DARPA toward a 1280x1024 display delivery. See Section II for details. The monochrome versions of the displays were designed for insertion into the Honeywell CVC HMD. The color display approach comprised a 2560x1024 AMEL display formed with white phosphor and color filters, and a 2560x2048 AMLCD with color filters.

TABLE 1-1. SUMMARY OF THE AMEL/AMLCD DISPLAY SPECIFICATIONS

Characteristic	Item	Specification
Display Format	Monochrome	2560x2048
	Color	1280x1024
Pixel Resolution	Monochrome	2000 lines per inch
	Color	1000 lines per inch
Pixel Pitch	Horizontal and vertical	12 μm
Dimensions	Active Area	1.2 inch x 1.0 inch
	Packaged Part (Max)	1.5 inch x 1.5 inch
	Device Thickness (Max)	0.070" (1.8 mm)
Data Refresh	Frames/sec	60Hz
Gray Scale	Resolution	6 bits
Interface	Logic Voltage	5 V
	Video Data Lines	Digital(AMEL)
		Analog(AMLCD)
	Timing System	External clock

1.3. Development Approach

The development carried out in this program was a basic research investigation followed by application of the results in displays. Accordingly, the work plan involved two phases: First, work focused on the design and fabrication of small-scale test arrays, a continuation of the pixel development tasks of the preceding contract. These test arrays included an array of pixel parameter variations to allow selection of the best performing 12 μm pixel designs under test. The test arrays were also used as a vehicle to develop the fabrication process on a small scale before we attempted to make the full array displays. Many of the design, process development and process compatibility issues were resolved on the small-scale displays, as we will describe later in this report.

Display design and development proceeded with the goal of developing two displays (AMEL and AMLCD) with the same physical size, pixel pitch, and mechanical interface. The same electrical interface was considered but this added too much complexity to the designs.

1.4. Development Results

The program resulted in the creation of two new display technologies. To prove the success of this development, we demonstrated and will delivered AMEL and AMLCD displays to the U.S. Army Research Laboratories, Adelphi, MD. Figures I-1 and I-2 are photographs of the two displays. Both displays have 2000 LPI resolution (12 μm pixel pitch). The AMLCD has a 2560x2048 pixel array. The AMEL display has a 1280x1024 pixel array.

FIGURE 1-1. PHOTO OF AN OPERATIONAL 2000 LPI, 1280X1024 AMEL DISPLAY.

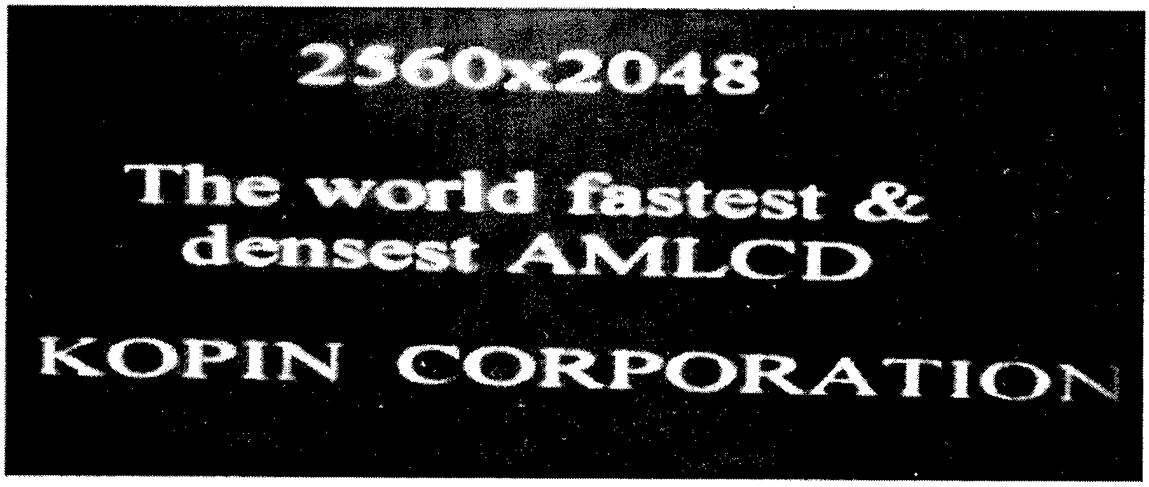


FIGURE 1-2. PHOTO OF AN OPERATIONAL 2000 LPI, 2560X2048 AMLCD DISPLAY.

1.5. 2000 LPI Display Products Insertion

This project has demonstrated working 2000LPI displays which attest to the realization of enabling technologies for the design and manufacture of advanced displays for military and commercial applications. However, additional development is required to produce these displays with sufficient manufacturing yields for product viability and insertion into military systems. Additional development tasks required are discussed in subsequent sections. 2000 LPI display products based on the technologies developed are under development at Kopin and at Planar for insertion into government systems. A 2000 LPI, 1280x1024 AMLCD is under development at Kopin for the AIHS/Comanche program. First manufacturing lot displays are operational with good performance. A prototype 2000LPI AMEL display for the Army Land Warrior program is operational at Planar. AMEL and AMLCD products are in production which use some of the new technologies developed.

SECTION 2
2000 LPI Active Matrix Electroluminescent (AMEL) Display Development
- Final Report -

1.0 Introduction

1.1 Overview

The objective of the Active Matrix Electroluminescent (AMEL) portion of this program has been the development of the first 12μm pixel technology for use in very high resolution AMEL displays. These devices are expected to fulfill a need for next generation applications of head mounted and other types of personnel-retained displays. This program has been able to leverage off the earlier successful design implementation of 24μm AMEL display technology which combined the expertise of Planar Systems, Sarnoff Corporation and AlliedSignal MTC. The AMEL 2000 LPI displays provide an unprecedented ability to display a very high information density in an extremely compact package while maintaining the excellent image quality and environmental performance previously demonstrated by AMEL 24μm displays.

1.2 AMEL 2000 LPI Program Responsibilities

The division of responsibilities are shown below:

- Integrated Circuit Design (Sarnoff)
- Integrated Circuit Processing (AlliedSignal)
- EL Processing and Packaging (Planar)
- AMEL Program Management (Planar)
- Overall Program Management (Kopin)

The listing of the detailed developmental tasks and the team members responsible for those tasks is shown in Table 2-1.

Table 2-1 Summary of AMEL Development Tasks

Development Area	Task
IC Design (Sarnoff)	Designs of 12μm pixel candidates Design of peripheral circuitry to drive the 12μm pixel Design process and yield control structures Development of a test system to evaluate 2000LPI test arrays
IC Processing (AlliedSignal)	1μm large area photolithographic processing Development of a new dielectric to improve comformality Development of higher voltage DMOS devices Silicide process development to improve select line conductivity Evaluation of wafer material Test system to evaluate IC performance
EL Processing and packaging (Planar)	Modify 24μm AMEL process for 12μm pixels Develop test system to evaluate EL and overall display performance Develop color process for full color display Establish approach for 2k LPI display packaging

To enhance program communication, team members participated in weekly teleconferences for information exchange and problem solving. In addition, quarterly reviews were held on a rotating basis at the three team member sites with the Government program manager (Henry Girolamo) as well as other potential Government users.

2.0 AMEL 2000 LPI Display Design and Processing

2.1 Introduction

This section describes the architecture, theory of operation and process development for the 2000 LPI Active Matrix Electroluminescent (AMEL) device development. The pixel dimension for this resolution is 12x12μm. As in previous AMEL devices, the design incorporates on-chip data drivers and vertical select scanners to access the pixel array. In addition, the EL stack is located over the pixel array region to maximize aperture ratio.

2.2 AMEL 12um Pixel Design and Selection

2.2.1 Pixel Selection Criteria

The selection of the 12μm pixel design was the key task in early part of the AMEL 2000 LPI development program. The challenge in defining the new pixel design was to maintain or improve upon the performance and manufacturability of the 24μm pixel and to miniaturize it to an area one-quarter that of the 24μm pixel. The primary issues are listed below:

- Minimizing the length of the drift region (see Figure 2-1) of the high voltage DMOS (Diffused Metal Oxide Semiconductor) transistor while maintaining an adequate blocking voltage (>80V) to allow for full phosphor voltage modulation
- Selection of a common source versus a grounded pixel approach (see Figure 2-2)
- Maximizing the hold node capacitance to increase pixel voltage margin while maintaining a manufacturable topology
- Selection of a pixel layout which shares DMOS source grounds for compactness
- In general, minimizing topological relief in the pixel layout

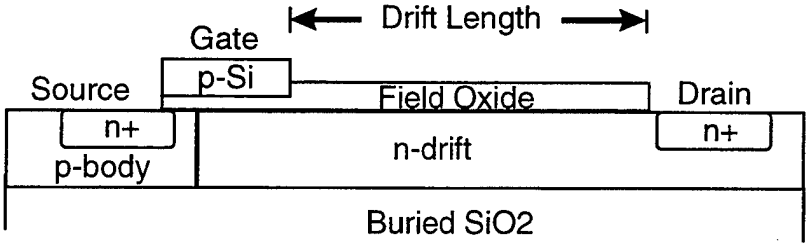


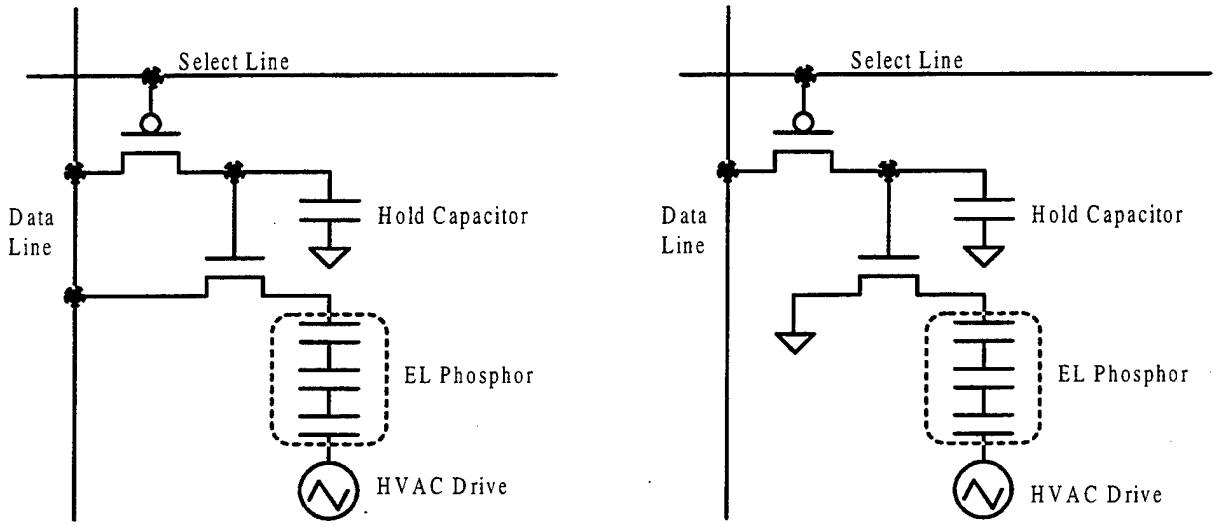
Figure 2-1 Location of the drift region (drift length) in the DMOS transistor

2.2.2 12μm Pixel Testing

A total of twelve 12μm pixels were defined and tested in eight wafer lots. The pixels were laid out in arrays of 256x256 pixels and were tested at Sarnoff and Planar. Test pixels of 6 and 9μm were also included to investigate the limits for future AMEL designs. Key parameters for pixel testing were voltage margin, defect density and gray scale response. All twelve of the 12μm pixels proved to be functional. The selected pixel design makes use of a shared source between two adjacent pixels instead of four because

of concerns that sharing among four would group the pixels at irregular intervals and perhaps cause visual artifacts.

A key consideration in the pixel selection process was whether to use a pixel structure with a common source or grounded source configuration. As shown in Figure 2-2, in the common source design the source of the high voltage DMOS transistor is connected to the data line. This means the data line must sink the current flowing through the EL stack. In the grounded source configuration, the source of the DMOS is connected directly to the ground plane.



Common Source Configuration **Grounded Source Configuration**

Figure 2-2 Two Possible Considerations for the AMEL 12µm pixel design

Both configurations were demonstrated to work adequately on test arrays, however, there are numerous advantages of the grounded source configuration. The primary advantage is its increased operating voltage margin. It also allows for addressing and illumination to occur simultaneously. The disadvantage of this approach is that it requires more space inside the pixel layout and an additional mask step is required. After reviewing the design data and results from test array analysis, it was agreed that the advantages of the grounded source configuration outweighed the potential processing drawbacks.

2.3 Architecture and Theory of Operation

2.3.1 Operation Fundamentals

Figure 2-3 shows the top level internal partitioning of the AMEL 1280x1024 12µm display functions. The display is made up of:

- The 1280 x 1024 pixel array
- Data input demultiplex timing generator
- Data latches
- Row select scanners
- Row scanner and column line test circuitry

The array is addressed one row at a time, from top to bottom. To address each row, the data scanner is first loaded with all data bits for the row and this data set is then latched onto each of the 1280 column data lines. The select scanner activates each PMOS pixel access transistor by pulling the select line low. After sufficient time has elapsed for the data to be written into the storage nodes of each transistor on the row, the select line is returned to the high (unselected) state, and the process repeats for the next row.
The data scanner is composed of a 160 stage shift register, which sequentially demultiplexes the 8 data inputs into the column line latches. Data is latched in on both edges of the data clock signal (PCLK). Data can be clocked in at up to 100MHz, which translates to a PCLK running at 50MHz.

The select scanners are composed of a 1024 stage shift register which propagates a select bit. The scanner is initiated by START and is clocked by SCLK. Each row select line is driven simultaneously by scanners on the right and left side of the display. This dual drive approach enables the rows to charge and discharge in a time sufficient to allow the 100MHz data rate operation.

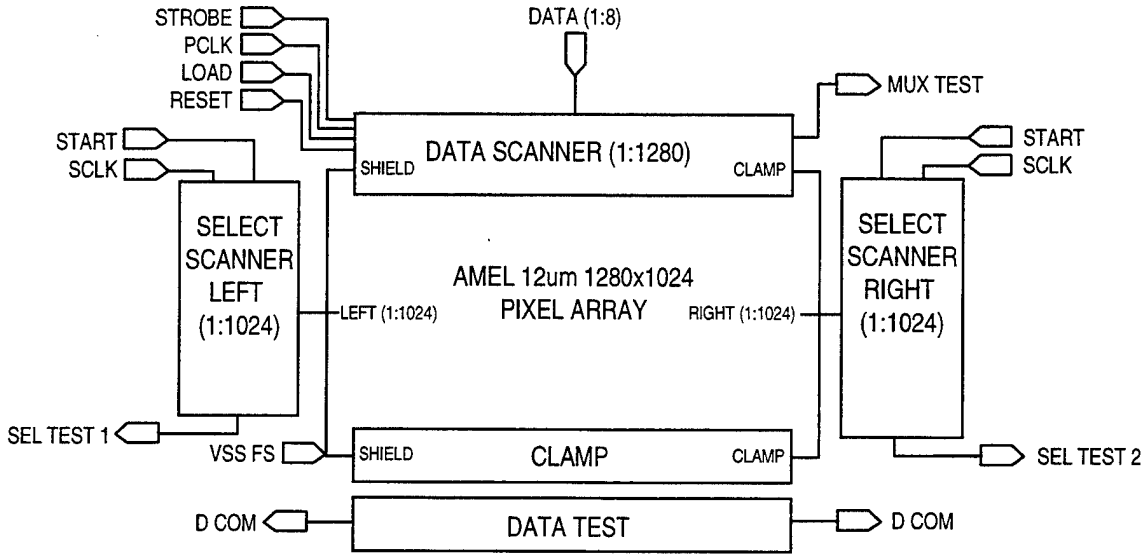


Figure 2-3 1280x1024 12-um pixel AMEL Internal Functional Block Diagram

Gray scale is achieved using a temporal dithering approach shown in Figure 2-4. After the array is addressed with a bit field, a burst of high voltage sinusoidal pulses is used to excite EL material for illumination of that bit field. The number of high voltage pulses applied depends on the bit weighting of the bit field. Bit zero and bit one both contain one pulse, however bit zero must be amplitude modulated to provide approximately half the luminance of bit one. The total EL illumination time required in one frame time of 16.7 msec is 7.1 msec which includes 63 cycles for an ideal six binary bits plus eight extra cycles to compensate for AMEL saturation. This achieves 64 levels of grayscale.

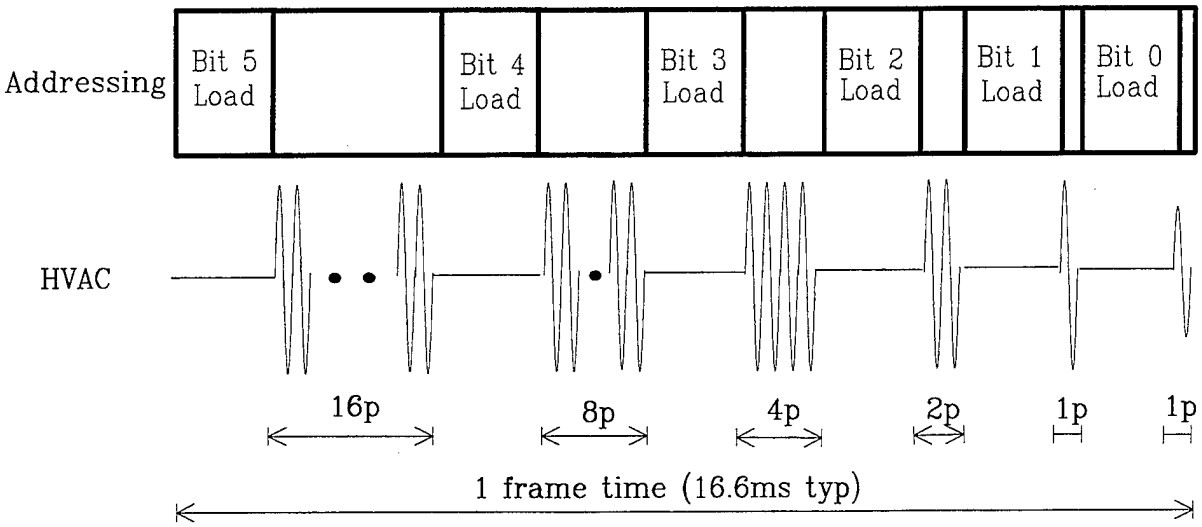
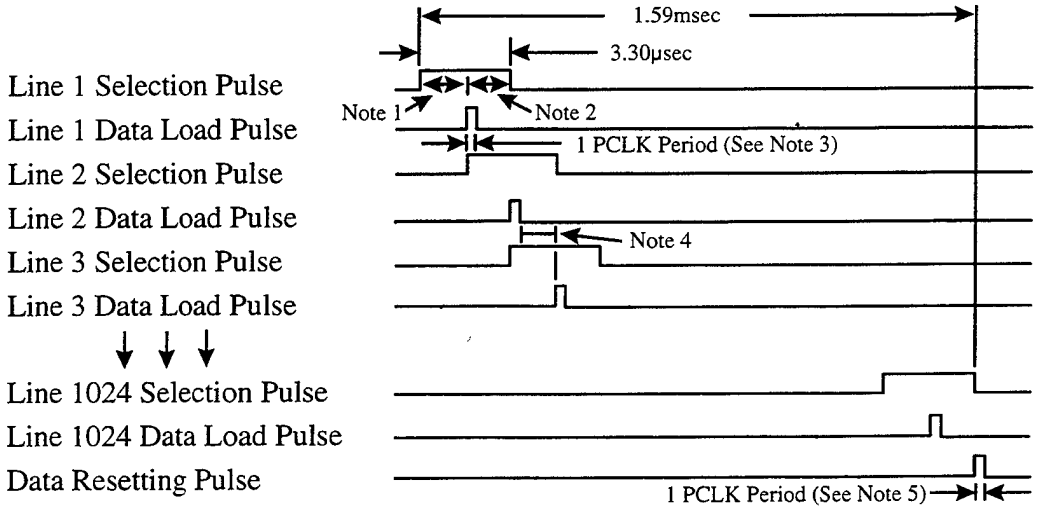


Figure 2-4 AMEL 12μm 1280x1024 Frame Timing for Loading Digital Data to Pixels and for EL Illumination when AC Frequency is Fixed at 6 kHz and Frame Rate is 60 Hz

Figure 2-5 shows the general timing relationships between the row and data scanner control logic. A pre-selection pulse is used to charge up the select line prior to data loading. At the 100MHz data rate, both the pre-selection and active selection take 1.56μ sec making the total selection time 3.11 μsec long. The pre-selection of a given row overlaps the active-selection of the previous row, just as the active-selection of a given row overlaps the pre-selection of the next row.



Note 1: Pre-selection line time which one half of 3.3μsec, i.e. 1.65μsec

Note 2: Real selection line time to load 1280 digital data in parallel to pixels in Line 1

Note 3: Time interval during which 1280 digital data from dynamic shift registers are latched simultaneously

Note 4: Time interval to shift 1280 digital data in dynamic shift registers (1.65μsec)

Note 5: Reset pulse to initialize 1280 data lines to 0V

Figure 2-5 1280x1024 12μm pixel AMEL Field Timing for loading Digital Data

Figure 2-6 shows the control timing relationships in more detail. Figure 2-6 shows that a START signal begins each field of data. The START pulse width (low enable) is two clock periods of SCLK. This results in a pre-select and active-select for each row. The falling edge of START is synchronized with the falling edge of SCLK with a setup delay. A total of 160 writes are performed during each consecutive SCLK period with the LOAD signal switching to a 'high' state to latch data onto the column data lines.

Figure 2-6 shows one data-write cycle is comprised of 82 PCLK cycles of which 80 are used to perform 160 data input operations to a row of the display pixel. The STROBE signal occurs at the same time as the first data load to initiate the data scanner shift register. After all 160 loads are completed for a row, LOAD goes high to transfer the data into the column data lines.

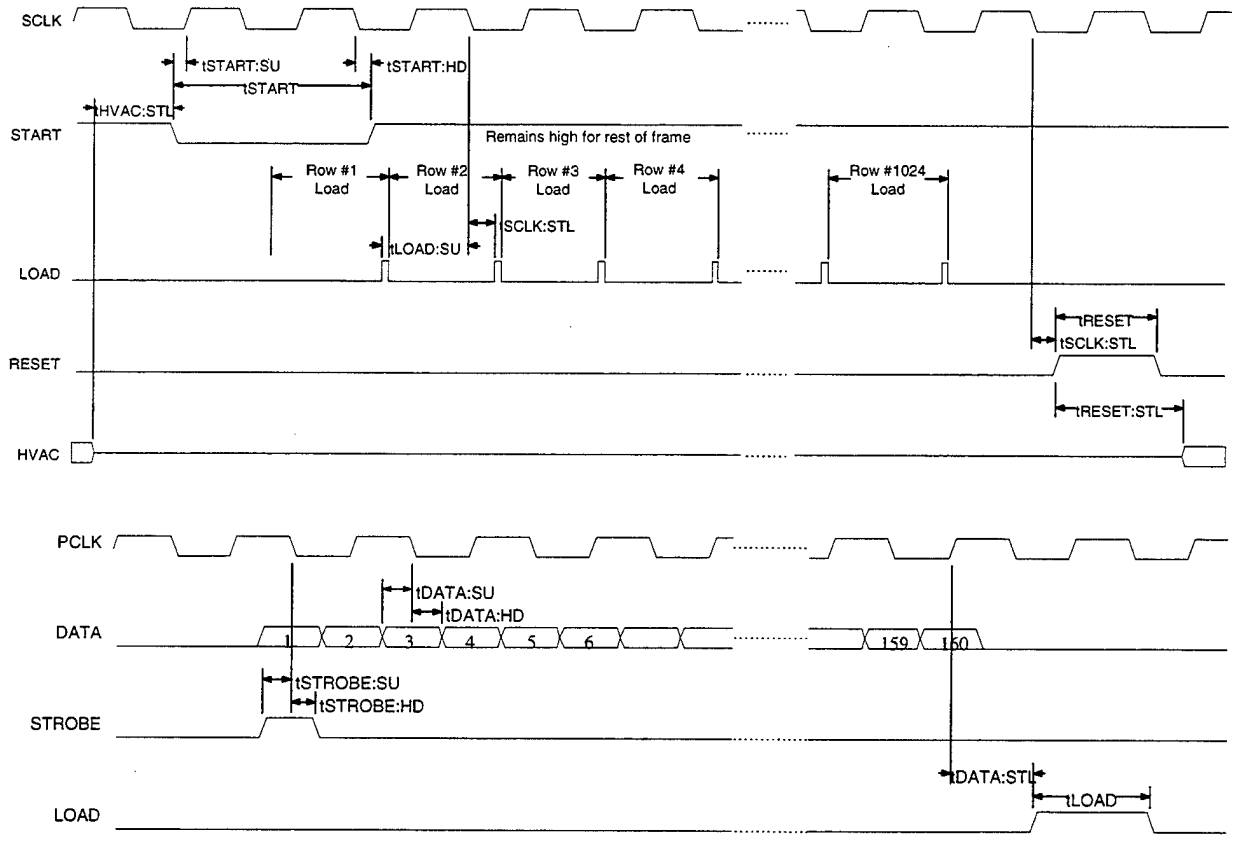


Figure 2-6 AMEL 1280x1024 12μm Control Signal Timing for Each Field

With this information, the PCLK (min) required for 60 fps operation can be calculated as follows:

# of PCLKs per frame time = [(82 PCLKs / row) (1024 rows / field) + (82 PCLKs / START) x 1 START / field)] (6 fields / frame)
= 504,300 PCLKs / frame time

This can be used to calculate the $PCLK_{min}$ resulting in a requirement for 52.7 MHz.

# of nsec per PCLK = (9.566 msec / frame) / (504,300 PCLKs / frame)

= 19 nsec / PCLK (which is ~ 52.7 MHz of PCLK frequency)

2.4 Display Interface and Layout

Once the 1280x1024 array was chosen as the AMEL 2k technology demonstrator, a goal for this development effort was to make the package design dimensionally identical with that of the 24μm pixel 640x480 AMEL VGA display. This will allow users of the AMEL VGA displays to readily upgrade to a higher resolution device.

Table 2-2 shows the pin description for the 12μm 1280x1024 display design. In the current configuration, the pixel needs additional power supply inputs (VDD2, GND2) to achieve optimum performance. The VDD2 pad is placed next to VDD and GND2 is placed next to VSS in the layout so they can easily be shorted when the pixel design and processes are optimized to a point where the additional inputs are no longer needed.

Table 2-2 AMEL 12μm 1280x 1024 Display Interface

Input Name	Description
DATA	Parallel digital data inputs (8)
LOAD	Data loading control signal to transfer data from latch circuits into pixel data lines
RESET	Pixel data line reset control to set data line at ground potential at the beginning of applying EL illumination AC burst
STROBE	Initial data transmission for each 2560-pixel row.
SCLK	Select line clock for select scanner shift registers
START	Initial selection line pulse with pulse width of two clock periods of SCLK to achieve a double-line-time selection
VSS	Common ground
VSS_FS	Field shield isolation ground
GND2	Data line negative voltage
VDD	5 volts power supply in the three middle panels
VDD2	3-5V power supply
VDD1	7-10 volts power supply for select line driver (off state)
VSSR	-3 volts power supply for select line driver (on state)
ITO	250V sine waveform for EL excitation
Sel_test	Select scanner output test signals
S_com	Pixel data line test PMOS common source
D_com	Pixel data line test PMOS common drain
MUX_TEST	Buffered data multiplexer output

A drawing of the display prototype is found in Figure 2-7. The overall package size, including flex connector, is 1.935 x 0.815 inches (49.1x20.7mm) with an active area of 0.605 x 0.484 inches (15.4x12.2 mm). The size of the ceramic package is 0.935x0.815 (23.7x20.7).

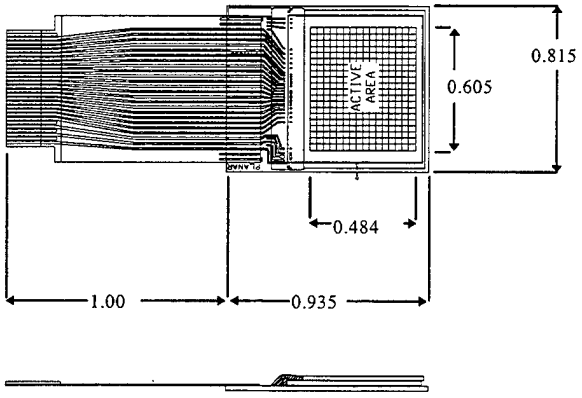


Figure 2-7 AMEL 12μm 1280x1024 Display Dimensions

2.5 AMEL Display Processing

A primary intent for the program has been to develop a prototype fabrication capability for the 2000 LPI displays under development. This required process development for both IC fabrication at AlliedSignal and for EL processing at Planar. During the course of the program, the 256x256, 2560x2048 and 1280x1024 arrays were used for both IC and EL process development. The following are the key tasks for IC process development which lead to the capability of fabricating high speed CMOS (low voltage Complementary Metal Oxide Semiconductor) transistors and high voltage DMOS transistors on SOI (silicon on insulator) wafers:

- Development of large area photolithographic processing to 1μm design rules with field stitching
- Planarization for triple level refractory metal interconnection
- Selection of optimum SOI material

The primary EL development consisted of refining the processes developed for 24μm pixel devices to the 12μm pixel display. In addition, white phosphor development for use in color displays was undertaken. Adaptation of photoprocesses for the higher resolution display were the most significant task in the process transfer from 24μm to 12μm devices. Controlling the phosphor etch undercut and the dimension of the aluminum traces has been the focus of critical attention.

The white phosphor work involved further development of the ZnS:Mn/SrS:Ce phosphor which would be used with a liquid crystal color shutter to achieve color. A key concern with the SrS:Ce/ZnS:Mn broadband white phosphor at the beginning of this program has been the aging characteristics. During this program the aging stability of the

SrS:Ce/ZnS:Mn phosphor was significantly improved by implementing a non-chloride Atomic Layer Epitaxy (ALE) deposition process for the ZnS:Mn phosphor and by eliminating the Al_2O_3 buffer layer between the SrS:Ce and ZnS:Mn films. Less than 10% "on" latent image was measured after 1000 hours using test devices. This performance would satisfy Planar specifications and other industry standards for differential aging.

3.0 AMEL 12um 1280x1024 Performance Data

3.1 AMEL 12um 1280x1024 Characterization Data

3.1.1 Luminance and Power

Figure 2-8 shows the luminance and power vs. voltage measured from a sample 12μm 1280x1024 display processed using a yellow emitting ZnS:Mn phosphor recipe. Both on-state and off-state luminance vs. voltage curves are shown. The difference in voltage between the on-state and off-state curves for a given luminance represents the blocking voltage capability of the high voltage pixel DMOS transistor. Due to the charge transport behavior of the EL stack, the effective blocking voltage is one-half the actual DMOS reverse breakdown. In Figure 2-8 the 42 volt blocking voltage translates to a 84 volt DMOS reverse breakdown. For maximum luminous efficiency and pixel contrast, the device is typically operated at 120V for this phosphor recipe. At this voltage, the display luminance is 250fL and dissipates 1W of power.

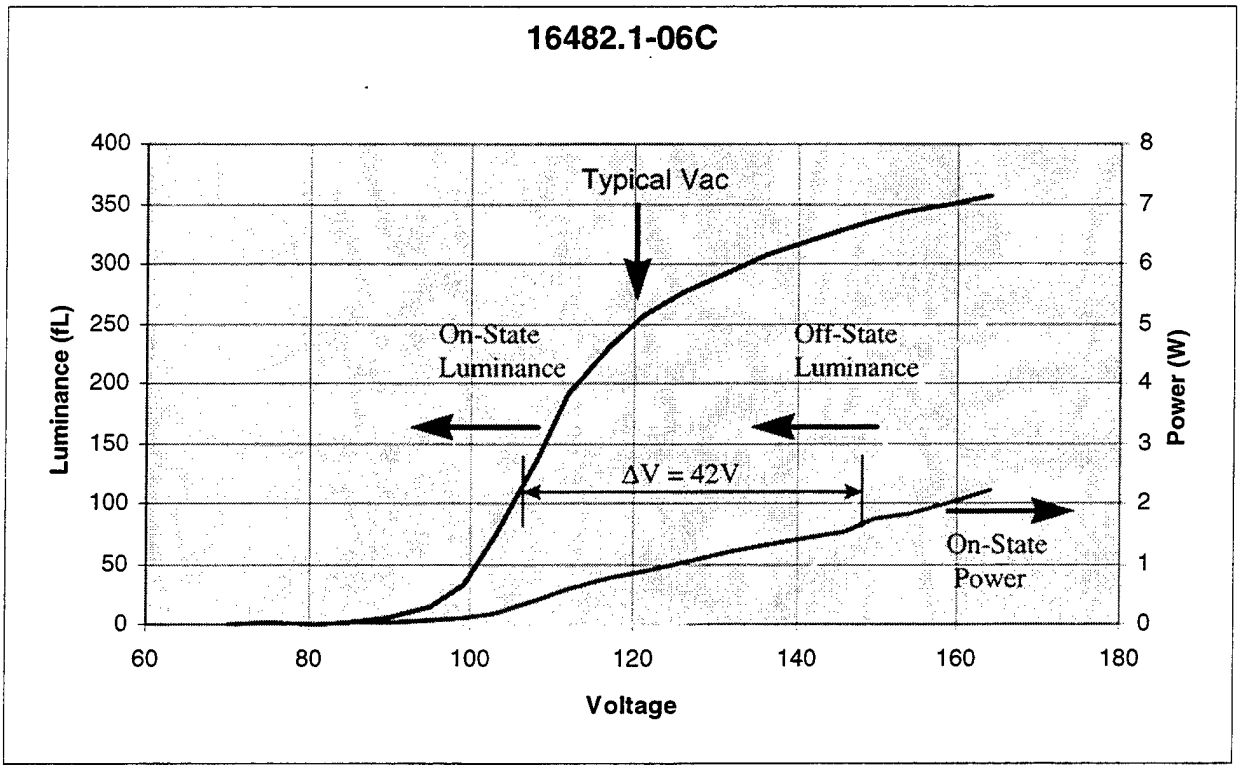


Figure 2-8 Luminance and Power vs. Voltage Data for an AMEL 12μm,1280x1024 Display

3.1.2 Voltage Margins and Input Current

Table 2-3 shows the allowable voltage margin for each of the power line inputs. These margins were found to be adequate for the initial prototype displays and are consistent with the values derived from circuit simulations.

Table 2-3 Allowable voltage margins for 12μm 1280x1024 Prototypes

Power Line	Unit	Min	Typ	Max
VDD	V	4.5	5	5.5
VDD2	V	4	4.5	5.5
VSSR	V	-4	-3	-2
VDDP	V	5	6	7
GND2	V	-0.5	-1	-1.5

Table 2-4 lists the typical input currents drawn from the power lines of the initial prototype units. All values were found to be within acceptable limits.

Table 2-4 Typical Current Draw for 12μm 1280x1024 Prototypes

Power Line	Input Current (typical)
VDD	<10mA
VDD2	10mA
VSSR	<10mA
VDDP	<10mA
GND2	10mA

3.1.3 Data Scanner Operation

The initial prototype displays were demonstrated to be completely operational at data load rates as high as 66MHz and as low as 1Mhz. At the design data input rate of 100MHz some minor data integrity problems were observed, the source of which are under investigation. Correct patterns were observed on the display and electrical tests on internal probe points verified proper operation up to 66MHz.

3.2 Preliminary AMEL 12μm 1280x1024 Display Specifications

A preliminary performance specification for the AMEL 12μm 1280x 1024 prototype display are found in the Table 2-5. The interface pinout is found in Table 6.

Table 2-5 Preliminary 12μm AMEL 1280x1024 Performance Specifications

Characteristic	Parameter	Value
Display Resolution	Matrix	1280 (H) by 1024(V)
		2000 lines per inch
Dimensions	Viewable Area	0.605 x 0.484 in (15.4 x 2.3mm)
	External Package	0.935 x 0.815 in (23.7 x 20.7mm)
	Thickness	0.068 in (1.7 mm)
	Weight	2.1 grams typical
Pixel Pitch	Monochrome	0.304 x 0.304 inch (0.012 x 0.012mm)
Pixel Fill Factor		69%
Data Refresh		15 to 70 Hz
Illumination Frequency		4.5 KHz sinusoidal
		140V peak
Luminance		≥75 fL
Contrast Ratio		>100:1
Gray Scale		64 levels (6 bits)
Luminance Non-uniformity		20% maximum
Operating Temperature	Min/Max	-40 / 75C
Storage Temperature	Min/Max	-55 / 85C

Table 2-6 Preliminary 12µm AMEL 1280x1024 Interconnect Pinout

Pin	Signal	Description
1	VB	Substrate Bias Voltage
2	NV	No Connect
3	HVAC	High Voltage AC for EL Illumination
4	NC	No Connect
5	NC	No Connect
6	NC	No Connect
7	D0	Pixel Data
8	D1	Pixel Data
9	D2	Pixel Data
10	D3	Pixel Data
11	SCLK	Row Select Scanner Shift Clock
12	START	Initiates row scanner at beginning of addressing period
13	STROBE	Initiates data load into data scanner for each row
14	VDD2	Positive data write voltage (+5v typ)
15	VDD	Positive supply for input circuit and data scanner (+5v typ)
16	VDDP	Positive supply for row scanner (+6.5V typ)
17	GND	Common Ground
18	VSSR	Negative supply for row scanner (-3V typ)
19	GND2	Negative Data Write Voltage (-1V typ)
20	PCLK	Pixel data Clock
21	LOAD	Data Loading Latch. Asserted after row data is loaded into data scanner.
22	RESET	Column Line Reset. Asserted at end of addressing period.
23	D4	Pixel Data
24	D5	Pixel Data
25	D6	Pixel Data
26	D7	Pixel Data
27	NC	No connect

Note: The flex cable mates to Molex 52437-2891

4.0 AMEL Summary

AMEL 2000 LPI technology has been successfully developed and demonstrated using 1280x1024 prototype displays. Table 2-7 is a summary of the AMEL display development milestones completed. A photograph of the 1280x1024 demonstrator is shown in figure 2-9. Validation of the 12μm pixel design has been achieved with 12μm pixel test arrays, 2560x2048 arrays and in the 1280x1024 technology demonstrator. A prototype fabrication capability has been created for the 1280 displays and this capability can readily be expanded to other AMEL 12μm designs. Initial electrical and optical characterization has been performed on the 1280x1024 display making use of the test capability that was developed on the program. This characterization capability will also be applicable to other AMEL 12μm displays.

Figure 2-9 12μm 1280x 1024 Display Prototype

Table 2-7: 2k AMEL Project Milestones

Task	Lead	Date	Status
Choice of test structures	All	12/30/95	Completed
Layout completed	Sarnoff	3/3/95	Completed
First lot completed	Allied	6/15/95	Completed
First operational sample	Planar	7/24/95	Completed
Completion of Lot 4	Allied	10/1/95	Completed
Selection of 12μm pixel design	All	10/15/95	Completed
Completion of 2560x2048 design	Sarnoff	12/15/95	Completed
First 2560 AMEL display	Planar	6/1/96	-
First 1280 color display	Planar	9/15/96	In TRP
Final AMEL deliverables	Planar	11/1/96	Revised
Revised Milestones			
First 2560 AMEL array demo	Planar	10/22/97	2/98
First 12μm 1280 display demo	Planar	10/22/97	2/98
Army Research Labs evaluation of 12μm 1280x1024 display	Planar/ARL		Completed

Acknowledgment: The participants in the development effort at Planar, AlliedSignal, Sarnoff, and Kopin wish to express their appreciation to Mr. Dick Urban of DARPA for funding this initiative and his commitment to the development of revolutionary technology. In particular, the team wishes to thank Mr. Henry Girolamo for his guidance, always-constructive input and continuing support for high resolution, miniature display development.

SECTION 3
2000 LPI Active Matrix Liquid Crystal Display (AMLCD) Development
- Final Report -

1.0. Objectives of the AMLCD Project

The principal objective of this work is the development of AMLCD pixel technology at the 2000 pixel per inch level (monochrome). To make this possible, we continued the development of AMLCD pixels suitable for active matrix displays with pixel pitch of 12 μm. In addition to standard twisted nematic liquid crystals, we investigated ferroelectric liquid crystals for improved AMLCD operation. The purpose of including ferroelectric LCDs in this work is to establish a baseline for ferroelectric LCD pixels using the test arrays that have been successful for twisted nematic liquid crystals and to assess their advantages in terms of contrast and speed at the 12 μm pitch.

The second objective of the program is the design, fabrication, and delivery of 2000 LPI, 2560x2048 monochrome displays. These displays are based on the 12 μm pixels developed in this program, and have nominal dimensions of 1.5 inch by 1.5 inch. The application of color filters developed previously will enable these displays to provide 1280x1024 in full color. As part of this work, however, we anticipated the display requirements of 1997, and modified the entire display design approach accordingly to demonstrate displays of the greatest military and commercial significance. This work led to the selection of an analog grey scale interface for the AMLCD and to the current 2000 LPI, 1280x1024 display development now underway for the Commanche program and other applications.

The lack of image sources for a 2560x2040 display and a suitable video interface standard is an application problem. Nevertheless, the 2560x2048 displays were completed to assess its manufacturing feasibility and performance issues for large pixel arrays. Surprisingly high display circuit yields and a relatively large number of functional 2560x2048 AMLCD displays provided valuable data for current HMD product development efforts. These results show conclusively that very large AMLCD arrays can be manufactured.

2.0. Summary of Deliverables

Kopin will deliver three prototype monochrome 2560x2048 AMLCD displays for demonstration. The nominal specifications and corresponding achievements for these displays are shown in Table 3-1. The project deliverables and their status are listed in Table 3-2. All official hardware deliveries are provided to U.S. Army Electronic Devices & Technology Laboratory for evaluation. The project team worked closely with Honeywell to define drive requirements for their design of the interface circuitry

necessary to connect the display to a graphics processor. In this way, DARPA could be provided with a complete demonstration of the technology.

TABLE 3-1. AMLCD DISPLAY SPECIFICATIONS AND RESULTS

Characteristic	Item	Specification	Achieved
Display Format	Monochrome Color	2560 x 2048 1280x1024	Yes Filter technology developed
Pixel Resolution	Monochrome Color Color	2000 LPI 1000 LPI 2000 LPI	Yes Available color filter process Available color sequential
Dimensions	Active Area Total Area Packaged Part Thickness	1.2 inch x 1.0 inch 1.5 inch x 1.5 inch 1.5 inch x 1.5 inch 0.05 inch (nominal)	Yes
Data Refresh Luminous Output Optical Aperture Grey Scale Contrast Ratio		60 Hz Back light dependent >30% analog >50:1	No (see 3.3) Yes 24 % (see 3.3) Yes Yes
Interface	Logic Voltage Video Lines	5 volt digital Parallel < 32 analog	5 V logic 16 analog video lines (Total of 80 I/O lines)

TABLE 3-2. AMLCD DELIVERABLES SUMMARY

#	Item	Description	Status
1	256 Test Arrays	Deliver 256x256 Test Array Data Report	Delivered
2	2560 Data Pack	Deliver Design Report 2560x2048 AMLCD	Delivered
2a	2560 Data Pack II	Deliver Design Report for the 2560x2048 AMLCD including Lincoln Laboratory design changes	11/30/96
3	First 2560 AMLCDS	Deliver 4 2560 AMLCDs	Delivered
4	Final 2560 AMLCDS	Deliver 3 Final 2560x2048 AMLCDs to DARPA	Delivered
5	Report	Deliver Final Report on 2560x2048 AMLCDs	11/30/97 (This report)

3.0. The Development of the 2560x2048 AMLCD

Display development required the development of the 12 μm pixel design, the selection of a suitable LC material, and the pixel array and scanner circuits design to provide the performance specified in Table 3-1. The following discussion includes alternatives considered and the design approach chosen

3.1. The Development of Small AMLCD Pixels

The basic pixel design forms the basis for the overall display design, providing the optical performance required of the overall display. The pixel of an active matrix display is composed of three elements, an electrode to apply voltage to the liquid crystal material, a transistor switch, and a storage capacitor. The transistor is off most of the time, connecting the electrode to the data line briefly each refresh cycle (frame). The storage capacitor maintains the pixel voltage during the long off state. Leakage currents must be very low to prevent the voltage from decaying between frames. The x-Si circuits hold the pixel voltages to > 90% of initial values.

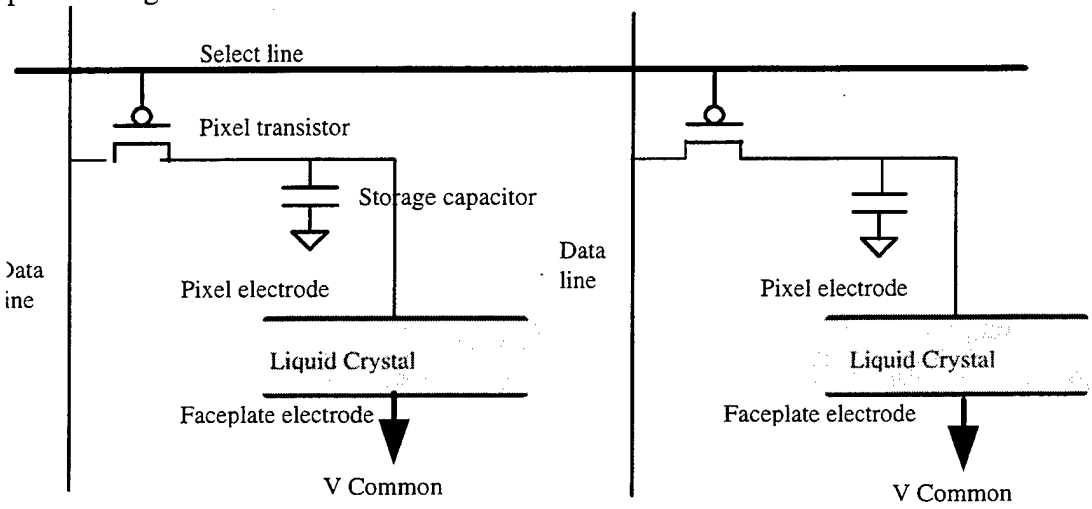


Figure 3-1: AMLCD Pixel Circuit

Display circuit operation is similar to the AMEL circuit described in Section II, except only one transistor per pixel is required because the voltages required are lower and no ac drive voltage is applied. Operation for the AMLCD is plus and minus 4.5 Volts around the faceplate voltage, Vcommon. Scanner circuits are somewhat similar to figure II-3. The basic Sarnoff display circuit design is a common technology, shared by both AMEL and AMLCD displays, which has been reported previously.

Twenty four alternative AMLCD pixel structures were defined by Sarnoff with design rule variations and process variations making a total of 39 different pixels. Refer to Sarnoff's AMLCD Test Pixel Array for 2048 x 2560 Display report (Deliverable 0002AC) for pixel array details. Of these, there were six basic pixel structure concepts which are summarized in Table 3-3 with their advantages and disadvantages.

Table 3-3 Major Pixel Electrode Construction Options

Electrode Construction	Advantages	Disadvantages
Active Area Silicon	Simplest process	Low light transmission, particularly in blue, causing the display to appear yellowish. Striped appearance created by minute variations in ISE material thickness.
Thin Polysilicon	Higher light transmission than Si	Requires triple poly process. Blue light transmission is better but still low.
Thin Polysilicon with anti-reflective layers	Higher light transmission than thin polysilicon	Added process steps are expensive. Blue transmission is increased somewhat. Green and red are increased significantly.
ITO (transistor side)	Excellent light transmission	Extra circuit side process steps. Materials incompatibility with IC foundry makes this process unacceptable.
ITO (liquid crystal side)	Best light transmission, best contrast.	Extra LC side process steps to fabricate the electrode and make contact through release oxide. Process after transfer in a separate facility from the IC foundry is acceptable.
Reflective pixel	High aperture ratio. Pixel areas devoted to transistor, data and select lines do not reduce effective aperture	Contact through release oxide required. Reflective optics are more complex, Planarized pixel area is required for best performance, possibly by CMP process.

Figure 3-2 illustrates the thin polysilicon pixel cross section. The release SiO2 layer surface which contacts the LC material is the surface which contacted the silicon wafer before transfer. The integrated circuit which was on top the wafer is now encapsulated by the adhesive. The silicon pixel cross section is similar except for the electrode material. The SiO2 dielectric layer forms a series capacitance between the pixel electrode and the LC gap which attenuates the drive voltage across the LC gap. The stored charge in the SiO2 can cause an offset in the LC gap voltage which causes image defects.

Figure 3-3 illustrates the LC side ITO pixel cross section. Note that the pixel electrode is in close proximity to the LC material and separated from the transistors and interconnect circuits. This arrangement eliminates the SiO2 stored charge effects and reduces the stray fields which cause LC disclinations (LC molecule orientation errors). The electrodes can be larger to cover the transistors and interconnect circuits, thereby shielding the LC from their fields. Placing the ITO electrodes close together also minimizes adverse field effects between adjacent pixels. LC materials require a periodic voltage polarity reversal to operate properly. This may be done by inverting the pixel drive voltages in each

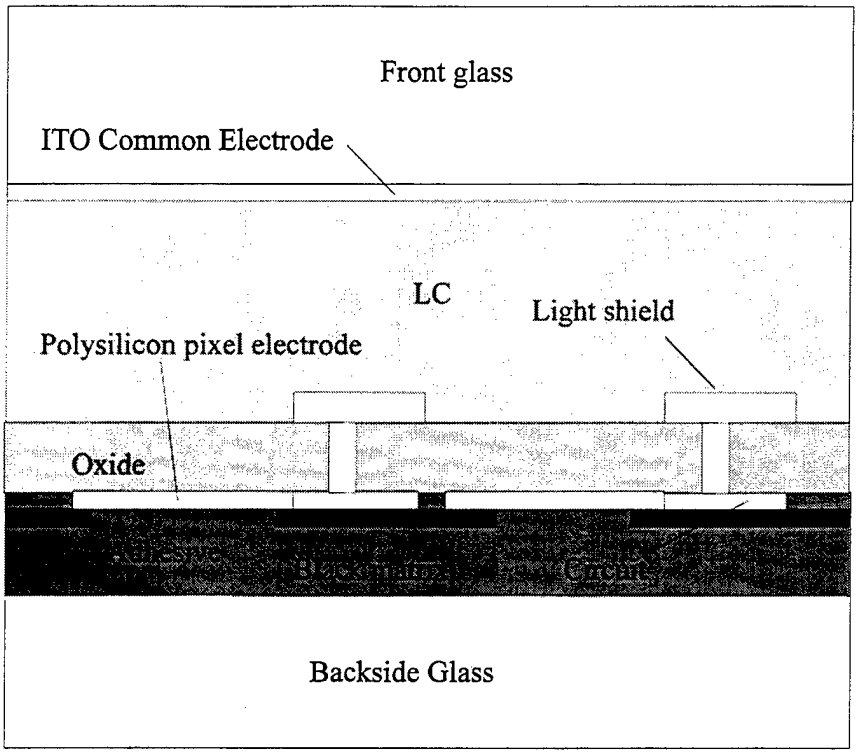


Figure 3-2: Thin Polysilicon Pixel Cross Section Concept

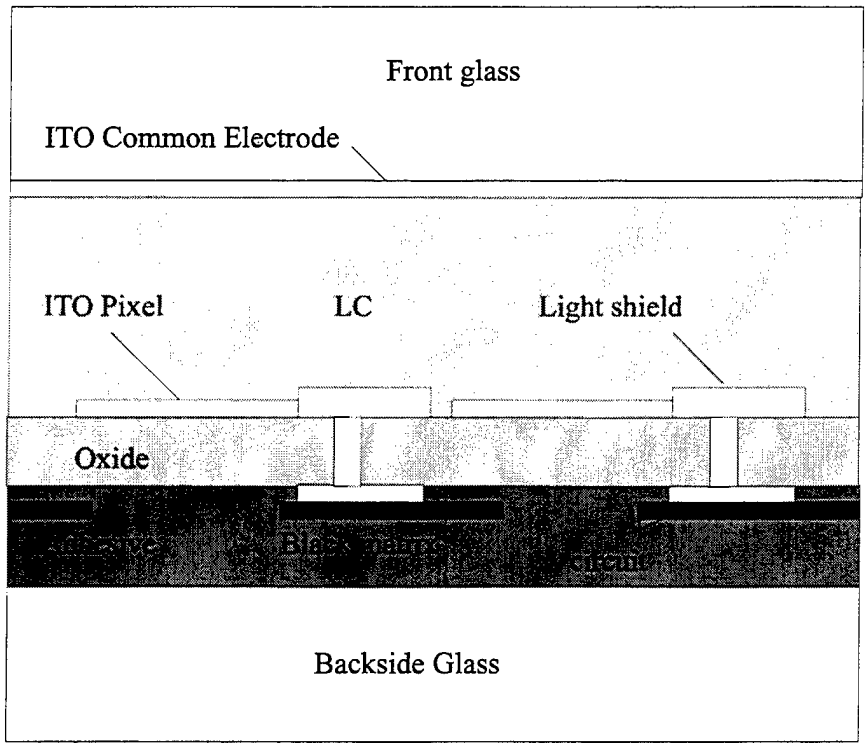


Figure 3-3: Liquid Crystal Side ITO Pixel Cross Section

successive frame. Frame inversion is prone to image flicker unless positive and negative drive voltages are precisely matched. For this reason, alternating pixel column inversion is preferred over frame inversion. In this mode neighboring columns of pixels have inverted voltage polarities which maximizes voltages between adjacent pixels.

An ITO pixel electrode fabricated on the LC side of the release oxide layer after display circuit transfer to glass has several potential benefits. First, the release oxide layer field loss is eliminated which reduces pixel drive voltage requirements. Additionally, image sticking and image flicker may be caused by the stored charge in the oxide layer. The stored charge in the oxide causes an unbalance in the alternating positive and negative voltage applied to the LC material. The LC side ITO electrode is located further out of the plane of the transistor and column lines (see Figure 3-3), thereby reducing the effects of fields from these structures. The ITO electrodes can be larger, overlapping the transistors and interconnect structures and forming a shielding structure to reduce LC disclinations. Capacitive coupling of voltages to the pixel electrodes from the row and column lines is further reduced by the attenuation of the oxide layer.

Modeling results show that the distance between electrode edges and the LC layer thickness should both be small to reduce adjacent pixel effects. The field in the LC between an electrode and the common ITO electrode will be distorted severely by the neighboring electrode voltage for a distance of about the thickness of the LC gap. In Figures 3-4 and 3-5, 3-D plots of voltage gradients in the LC gap shows distortions across the boundary between pixel electrodes with opposite voltages. These plots illustrate voltage gradients a vertical cross section of the LC gap crossing the boundary between pixels. Ideally, pixel voltage lines would all be parallel to the pixel electrode plane and describe a ramp function from Vcommon (4.5V) to 9 volts for one pixel and from Vcommon to 0 volts for the neighboring pixel. Figure 3-4 for the polysilicon case shows a flat area at the pixel boundary caused by the light shield tied to Vcommon. From there, the voltage lines are curved and are beginning to flatten at the edges of the plot which are one LC gap from the pixel boundaries. Note that the voltages do not reach 0 V and 9 V because there is a voltage drop in the oxide.

The plot of Figure 3-5 represents the case of closely spaced LC-side ITO pixels. The light shield is assumed to be covered by the ITO and electrically tied to one pixel. In this case the voltage lines become horizontal a shorter distance from the pixel boundary and no voltage is lost in the oxide.

The worst LC disclination areas around the edges of each pixel electrode must be hidden by the black matrix thereby limiting the aperture size and reducing display brightness. This implies a gap of 1 or 2 um to maximize the 12 um pixel aperture opening. Assuming an LC gap of 2 um for 12 um pixels, then the black matrix must cover 2 um of the pixel edges. This leaves a 6x6 um opening, an aperture efficiency of 36/144 or 25%. This is somewhat pessimistic, because the black matrix coverage between pixels in the same column can be smaller because vertically neighboring pixel voltages are of the same polarity. For 1 um design rules, the aperture efficiency could be 100/144 (69%) but might be limited by the interconnect circuit space required. This analysis illustrates the importance of a narrow LC

gap for small pixels to achieve high light transmission and brightness. Optimization of the LC layer thickness must also consider the LC material used and its alignment parameters.

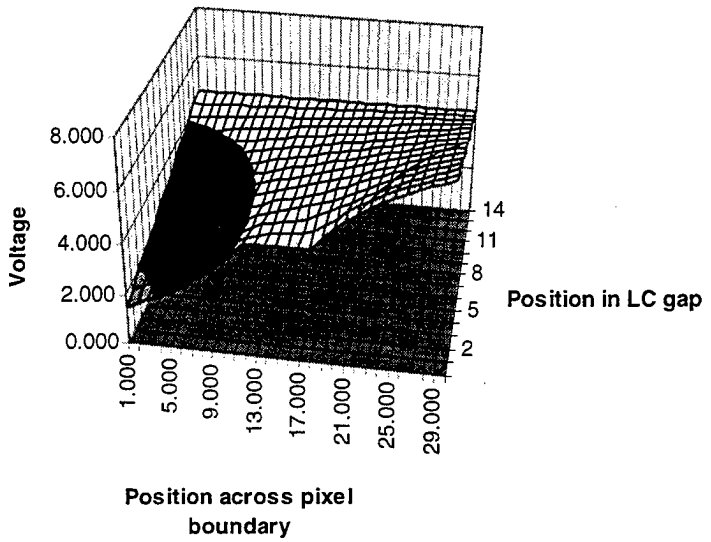


Figure 3-4: Voltage gradient surface plot of voltage in LC gap across pixel boundary for polysilicon electrode.

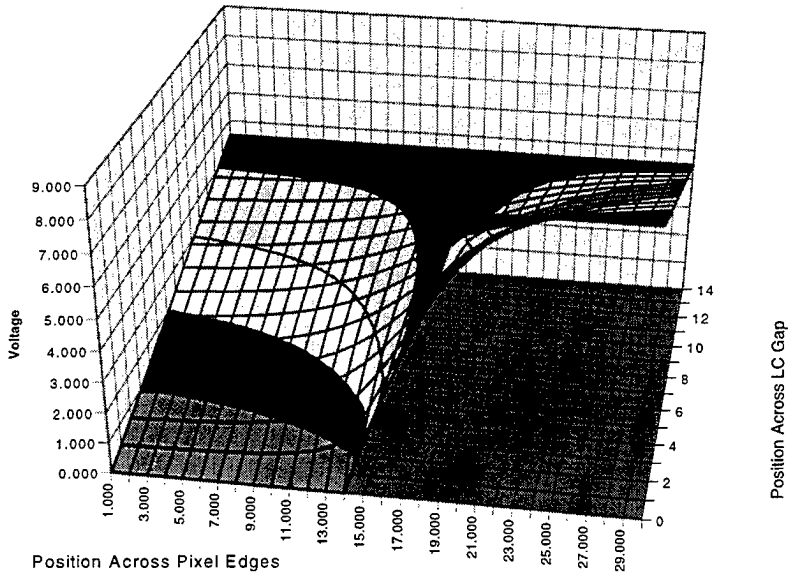


Figure 3-5: Voltage gradient surface plot of voltage in LC gap across pixel boundary for LC side ITO pixel electrode.

Cell gap reduction is the most effective method of intensifying the fields across the gap, thereby reducing LC disclinations, reducing voltage requirements, and speeding up LC

switching. Lower display voltages reduces the power required to operate them. Low power displays are desirable for portable, personnel electronics in the field for longer battery life and/or lighter equipment weight.

Major issues in implementing narrow LC gaps involve gap control in production. A reliable assembly process in a class 10 environment is required to produce narrow gap displays with high yield. A single particulate larger than the desired gap can act as an unwanted spacer to cause a gap error over an area which contains multiple displays. At this writing, Kopin has developed a process for narrow gaps for its CyberDisplay™ color display. There are 150 of these displays on each wafer. A narrow LC gap process is also under development for the AIHS and Comanche 2000 LPI displays.

3.1.1. Pixel Light Transmission Studies

Pixels contain multiple internal layers which cause a substantial loss in transmitted light owing to internal optical reflections and light absorption. The use of optically optimized layers of quarter wave thicknesses can be used to minimize internal reflections and maximize the light transmission of the pixel. Sarnoff used optical modeling codes to analyze the structure of the shielded pixel and determine optimum values for the thicknesses of the internal layers in the structure.

Parallel modeling and experimental studies at Kopin show that light transmission will exceed 80% through the pixel aperture areas by selecting highly transmissive materials such as ITO for pixel electrodes, by using optimal materials thicknesses and by index matching adjacent materials. Note that this excludes the polorizer and analyzer film losses. The major finding was that the silicon pixel used for the 1280 and polysilicon pixel used for the 2560 accounted for most of the light losses. The silicon oxide, glass, and LC material have fairly well matched refractive indexes around 1.5. TO used as the counter electrode on the faceplate and perhaps for the pixel electrode has an index around 1.9. The silicon and poly-silicon has an index which varies greatly over the visible spectrum, increasing in the blue to about 5. Differences in the indexes of adjacent materials causes reflections which account for much of the light loss. Absorption in the blue region by silicon is also a problem.

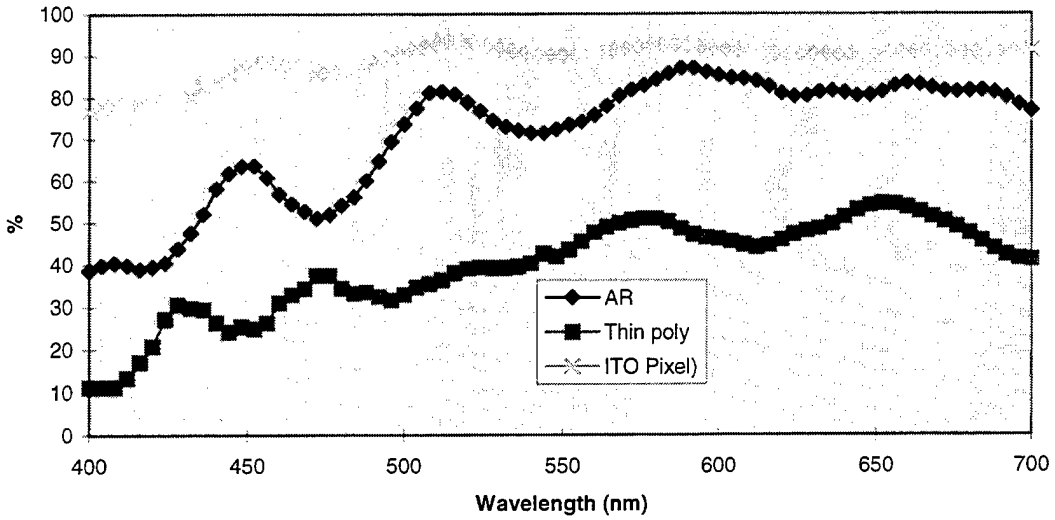


Figure 3-6. Transmissivity of thin polysilicon pixel structure, thin polysilicon with two layers of silicon nitride encapsulating it, and the LC-side ITO pixel. The nitride layers act as anti-reflective layers. Polorarizer and analyzer losses are not included.

The use of silicon nitride as an index matching material on both sides of the silicon pixel layer was shown to increase pixel transmissivity significantly. This approach combined with a very thin pixel structure produced even higher transmission; however, blue light transmission where the silicon index increases was not increased significantly. When color balancing is considered for color displays, the transmission benefits of this process may not be considered worth the added process complexity. A monochrome display with the nitride layers will be significantly brighter, with the overall transmission roughly doubled. However, the low blue light transmission makes a monochrome display appear slightly yellow.

The transmissivity of the ITO pixel structure is higher than the polysilicon particularly in the blue region of the spectrum as shown by measured data plotted in Figure 3-6.

3.1.2. Sarnoff Test Pixel Array Results

The 12 μm pixel array test data was limited by transistor leakage, which prevented testing under normal conditions, was identified as a process problem which would not be a problem for the actual displays. Extrapolations of data taken at very low light levels indicated that contrast ratios of between 40 and 60 could be achieved with contrast limiting problems resolved as discussed below.

A principal finding was electric field distortions in the LC caused by voltages on the row and column (data and select) lines. The Sarnoff test pixel design reduced this effect by adding a field shield plane of polysilicon positioned between the pixel electrode plane and

the data and select lines. The field shield is tied to the potential of the counter electrode (Vcommon) thus preventing fields from the data and select lines from influencing the liquid crystal. Consequently, few disclinations are formed and the resultant contrast ratio can potentially exceed 50:1.

Another issue was a contrast ratio limitation of less than 10:1 between neighboring pixels when the array is operated in column inversion mode. Note that no data was obtained from the ITO-LC side test pixels. In column inversion mode neighboring columns of pixels have inverted voltage polarities causing a large field between adjacent pixels and a disclination between pixel electrodes. These disclinations cause grey scale errors along the edges of the pixel opening. A dark pixel will have lighter bands along its edges. The extent of the field effects between pixels is greatly influenced by the pixel configuration. Positioning of the electrodes closer to the LC material and the reduction of the gap between the electrodes and the common faceplate electrode reduces the disclination band around the pixel, allowing a larger pixel aperture.

The Sarnoff pixel array development addressed the issues above by shielding techniques, by altering the inversion techniques and by improving the pixel design configuration. In addition to the poly-Si shield, the Sarnoff 2000 LPI, 2560x2048 AMLCD design incorporated a frame inversion technique, in which the required LC voltage drive inversions are applied on a frame-to-frame basis, thereby eliminating large voltages between neighboring pixels except along high contrast pattern edges. Frame inversion greatly reduced the disclinations, but resulted in image flicker caused by small differences in transmissivity for positive and negative drive voltages. This accentuated sensitivity to unbalanced positive and negative drive voltages was addressed by careful balancing to minimize the image flicker.

The pixel array data also confirmed the advantages of making the LC gap smaller and positioning the electrode in close proximity to the LC material. A gap in the range of 1 to 3 microns was indicated. Optimizing the gap must also includes considerations for light transmission, contrast ratio and the LC material chosen. An ITO pixel electrode on the LC side of the release oxide was advocated to reduce disclinations, to eliminate stored charge in the oxide and to eliminate the drive voltage losses across the oxide.

In addition to the pixel array development at Sarnoff, parallel developments at MIT Lincoln Lab and Kopin for commercial displays produced good results. Contrast ratios of >80:1 were shown in Kopin's SVGA (800x600) displays running in column inversion mode. Although, these pixels were 18 μm, scaling down to 12 μm showed promise for achieving the 50:1 2KAMLCD specification. At this writing, contrast rations >150:1 have been achieved by Kopin's CyberDisplay which has 15 μm pixels.

Using test array results, Sarnoff identified several factors to improve contrast ratio in the 2560 design. The Sarnoff pixel design, test results and process was made available to Lincoln Laboratory as planned. Lincoln Laboratory also fabricated the displays instead of AlliedSignal to take advantage of the SVGA display development and to use a 6" wafer process more suited for future display production.

Kopin and Lincoln Laboratory utilized what has been learned in designing and in producing Kopin's commercial SVGA display. This knowledge was combined with 12μm test array results to design a pixel structure for the 2560 AMLCD displays. The crosstalk and data noise characterized by the Sarnoff pixel array was useful in identifying the design differences with the SVGA pixel that made it more immune to these problems. This was a useful reference in scaling the pixel down from 18 μm to 12 μm without re-creating these problems; however, the resulting pixel is basically a scaled down SVGA pixel.

Once the pixel structure was identified, work was focus on development of processes to yield the desired structure in a reliable and manufacturable way. Differences in the Sarnoff and in the SVGA processes were studied and used to set process parameters for the 2560x2048. The SVGA production process was utilized as a base with improvements required to produce the 2560 AMLCD displays.

In summary, the key technical achievements required in the development of a high contrast ratio pixel are a narrow LC gap process, the selection of a suitable LC material and the positioning of the pixel electrode as close to the LC material as possible.

The Sarnoff pixel array developments and the Kopin/MIT Lincoln Lab display designs provided ample data on which to base the pixel design. However, process risks weighed heavily on the design chosen. Referring to Table 3-3, the thin polysilicon pixel was chosen instead of the ITO (liquid crystal side) pixel and the would provide higher light transmission and better performance but was not chosen because the achievement of operational 2000 LPI , 2560x2048 displays was considered more important. The future development tasks discussion of paragraph 4 includes further analysis of this approach.

3.2. Liquid Crystal Materials Selection and Evaluation

The pixel design for 2000 LPI and its implications: narrow LC gaps, crosstalk reduction, etc. required that the LC materials be studied also. Kopin has an ongoing effort to identify promising LC materials and to reformulate them for enhanced performance. Faster materials have been developed for the high frame rates required for color sequential color operation. These materials require narrow LC gaps which makes them suitable also for small pixels. Kopin has identified materials for narrow LC gaps, which are suitable for 2000 LPI displays.

In a parallel effort, Prof. Kristina Johnson at University of Colorado investigated other enhanced pixels possibilities using ferroelectric liquid crystals (FELC). In particular the smectic type A crystals offer fast switching as well as greyscale and may be more suitable for a small pixel display than twisted nematic. The University of Colorado work focussed on 2000 LPI reflective displays but the results are applicable to transmissive cells with considerations for the differences in the light paths.

Prof. Johnson also designed test pixels for use with chiral smectic liquid crystal (CSLC) materials, including the ferroelectric liquid crystal, electroclinic and distorted helix ferroelectric (DHF). The former has the advantage of high speed and optical memory (in certain alignments, the switch is bistable), but is a binary modulator, while the latter two chiral smectics are analog materials. The DHF in particular switches at moderate speeds

with low voltage applied (electro-optic response saturates at as low as one volt per micron, with 25 to 40 microsecond switching speeds. Tradeoffs in pixel design include pixel capacitance versus polarization of the CSLC materials, fill factor, planarization, and optical throughput. It is also necessary to optimize CSLC material mixtures and alignment schemes to achieve the highest contrast ratio and optical throughput possible.

The LC work encompassed a wide range of applications. Narrow gap, high contrast TN LC materials were included which exhibited promising performance for 12 μm pixels. Fast settling LC materials are now being used for Kopin color sequential displays which operate at 180 Hz frame rates. Sequential frames with the array loaded with red, green and blue color data are synchronized with corresponding color backlights. The 180 Hz period must contain the array loading time, the LC switching time and the light on time. These fast materials can also be used for displays used for target tracking and other applications where fast moving images might cause streaking. See the future tasks discussion of section 4.

For the 2000 LPI AMLCD application, a well characterized LC material already proven in other displays was conservatively chosen to help assure the production of operating displays. In addition, a wider LC gap assembly process was used which was developed for the LC material chosen. These choices, which greatly helped to assure that working 2560x2048 displays were produced, reduced the performance of the displays. The narrow gap LC process and materials are now providing better performance in the AIHS/Comanche 2000 LPI display and other Kopin display products.

3.3. Design of The 2560x2048 Pixel Display

The creation of a large high resolution display requires not only a small pixel, but also scanning circuitry capable of driving data and select lines. These scanner circuits must be formed on-pitch with the pixel rows and columns. Scanner miniaturization was initially studied in the BAA93-19 project that produced working 12 um pitch scanners. The use of 1 μm design rules made possible a reduction in scanner circuitry size, so that data and select scanners were formed adjacent to a 12m active matrix. This was achieved by compressing the circuitry as much as possible. This was made more difficult by the use of larger, edgeless MOS transistors in the scanner design to eliminate the formation of parasitic transistor devices. By using four rows of select scanners, the effective scanner pitch of 12 μm was attained using a 48 μm true circuit pitch.

The second factor in the design of a 2560x2048 display is the data rate that must be supplied to the display. The scanners must operate at double the rates needed for the 1280x1024 display. Data from single crystal silicon (x-Si) scanning circuits on the 1280x1024 design showed that the active circuits could run at the rate necessary for a 60 Hz frame rate. This capability results from the use of x-Si for the circuitry. However, the extremely long row and column lines for driving the 2560x2048 require a reduction in the line resistances to minimize RC effects.

The Lincoln Laboratory design addressed the line resistance issue by adding a second level of metal over the polysilicon to reduce its resistance. The standard design uses

metal as the column line conductors and polysilicon as the row line conductors where each column line crossing occurs. The second metal layer was designed to be formed directly over the polysilicon, thereby reducing the row resistance. This process was new and untested so the decision was made to omit the layer from the first lots; however, the first two lots did not produce fully operational displays so the decision was made to omit the metal from lot 3 also. Lot 3 produced functional 2560x2048 AMLCD's without the second metal which will not operate at full frame rates.

The Sarnoff design for the 2560x2048 AMEL addressed the line resistance issue by adding a silicide process to reduce the polysilicon resistivity.

The final technical issue affecting the feasibility of a 2560 display was the attainment of 1 μm design rules over the field size required for these displays (1.5" x 1.5"). We had reasonably good success in developing an approach at AlliedSignal based on the stepper field stitching concept. In this approach, a stepper capable of better than 1 μm design rule is used for multiple stepped exposures to accomplish the patterning of a large field of the necessary size. We initially established techniques that permit highly accurate stitching; nevertheless, there was still a requirement to eliminate discernible stitching features in the final display. The plan was to be accomplished by using a Perkin-Elmer projection aligner to pattern the electrode array in one exposure (no stitching), and the stepper for critical layers requiring 1 μm design rules.

This mix-and-match approach was used with AMEL to make possible the 12 μm pixels; however, process problems combined with unforeseen design rule issues caused problems which were difficult to diagnose. However, late results at AlliedSignal showed promise for this approach. When design rule effects and process problems were understood, the results held promise that the approach might be used on future designs. This could become important in future designs which require submicron design rules and the circuit size exceeds the stepper field size.

The approach used at Lincoln laboratory is to use the same aligner for all levels. A Perkin Elmer 700, with 1 μm feature resolution, was used for all levels. The move to 6" wafers was also a step toward Kopin's production process. This straightforward approach worked out very well. It is noteworthy to comment that future foundry selections for manufacturing are limited by the Perkin Elmer 700 approach. At this writing, AlliedSignal has produced promising results on the AMEL program using the stepper approach, making the stepper approach appear more viable. It should be considered for future display manufacturing of displays larger than a stepper field. Kopin's foundry partner for its smaller displays uses steppers with a field size limitation of less than 1 inch. Thus the 2560x2048 would require stitching.

The scanner circuit design was based on the 24um pixel, 1280x1024 AMLCD, however, some new aspects were considered. We considered putting the voltage ramp circuits on-board the display; however, correction and other linearity corrections are more difficult to accomplish, once the ramp circuit is on-board. A direct drive approach was considered and rejected in the new design by Kopin and Lincoln laboratory because wider bandwidth video

circuits are required and the channel balancing benefit provided by the ramp approach would have been lost.

The major deviation from the 1280x1024 design was to use analog video inputs rather than digital inputs. The predecessor 1280x1024 has 80 digital video inputs. The 2560 has 16 analog video inputs. This change was based mainly on the success of the analog video approach in several display designs since the 1280x1024 design. The balancing of video channels is an issue for either approach. If analog video levels are not closely matched, vertical band image artifacts (a venetian blind effect) appear. Digital video is inherently matched at the display interface; however, mismatch of digital-to-analog conversion circuits on the display will cause similar artifacts. When the design was finalized, the possibility of matching video channels by gain adjustment on each analog video line was attractive. Since the design, new concepts for on-chip digital-to-analog converters have been developed which provides channel matching. Digital video is attractive for future applications because new systems are using digital video for displays.

Another compromise in the design was the use of frame inversion rather than column inversion. The Sarnoff design approach was frame inversion based on the test pixel contrast results which were much better in frame inversion mode. The SVGA pixel had demonstrated >80:1 contrast in column inversion mode. Scaling the SVGA scanner and pixel down to 12 μm would have likely met the 50:1 contrast goal; however, replacing the Sarnoff design required major design changes. Considering the project schedule compression caused by the added redesign task, the Sarnoff scanner design configuration was retained with a few changes to enhance yields.

3.4. 2560 x2048 Display Fabrication

Fabrication of the displays began in November 1996 at Lincoln Laboratory. Originally, eight lots of 25 four inch wafers each were to be processed at AlliedSignal. Three lots of 25 six-inch wafers were fabricated at MIT Lincoln Lab. The 6" wafers allow more than three times the number of displays to be fabricated on each wafer than on 4" wafers. Therefore, more displays were produced in the three 6" wafer lots. In addition, the Lincoln Laboratory process development used much of the existing production process at Lincoln laboratory which has already be transferred to the foundry, thereby bringing the display closer to production.

3.5. 2560x2048 Display Electrical Testing Results

After fabrication of the displays at the foundry the wafers receive a battery of electrical tests. The tests include (1) device parameter testing, (2) array input shorts tests, (3) array functional testing, and (4) array performance testing. Device parameter data and performance test data were used to refine the process in subsequent lots to effect improvements. Functional testing identifies candidate display circuits for producing fully functional displays. An interesting note is that Kopin Cyber320 displays were included along with the 2KAMLCD's as test devices. Yield on these tiny display circuits was very high, illustrating Kopin's progress in developing a standard process for fabricating displays of all sizes.

Test results were very encouraging considering that the 2KAMLCD circuit complexity is equivalent to a large integrated circuit with over 5,000,000 transistors. Circuit tests include the horizontal data scanners which route video signals to the 2560 column lines, the vertical scanners which individually select the 2048 rows, and overall functionality of the display circuit. These tests do no detect all faults within the pixel array but do provide a good indication of candidate circuits for functional displays. The tests are conducted at low speed because the presence of the bulk silicon presents large parasitic capacitances which slows down the circuits. Three lots of 25 six-inch wafers were processed, a total of 450 display circuits. Lot 1 did not produce working circuits but parametric testing provided data for process adjustment for lot 2. Lots 2 and 3 were completed with functional circuit test results shown in Table 3-4. These results are quite remarkable considering the complexity of these displays.

Table 3-4: 2000 LPI, 2560x2048 AMLCD circuit test results

CIRCUIT TEST	LOT 2 YIELD	LOT 3 YIELD
Horizontal data scanners	44 %	49 %
Vertical row select scanners	67 %	50 %
Fully functional display circuits (all 4 scanner circuits working)	11 %	10 %

3.6. 2000 LPI, 2560x2048 AMLCD Display Testing Results

This task involved the construction of equipment to drive the arrays with simple patterns in order to make measurements such as brightness and efficiency will be made. After electrical testing and liquid crystal assembly the arrays were powered and driven by the test equipment to generate simple test patterns for visual assessment and for optical measurements. The initial test equipment had noise problems and produced some visual artifacts which were cleaned up to some extent for rudimentary demonstrations. The configuration of the test setup was also not compatible with optical display test equipment to measure display performance parameters. New test equipment was built to allow allow display measurements and delivered with the final 3 displays to David Morton at the Army Research Lab to satisfy the project deliverables.

Three hundred 2K-AMLCD display die were fabricated in Lots 2 and 3 of which there were 30 fully functional circuits tested before circuit transfer to glass and final display assembly. 18 functional displays were produced. The following are photographs of the display screens.

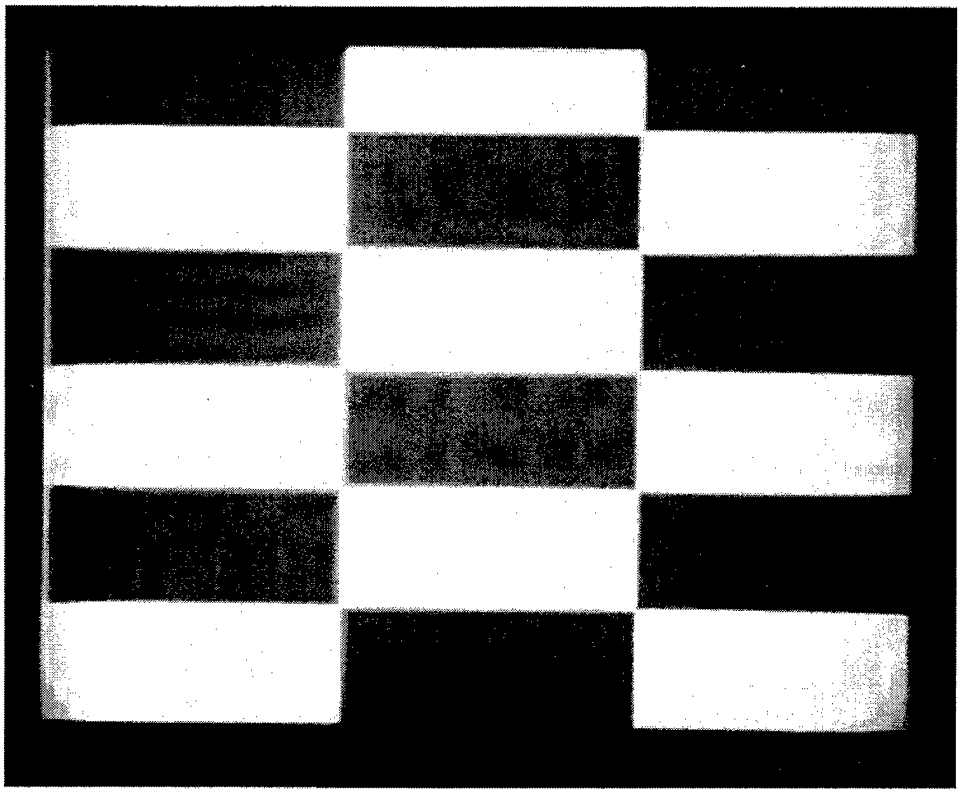


Figure 3-7. Screen Photo of 2000 LPI, 2560x2048 AMLCD Display

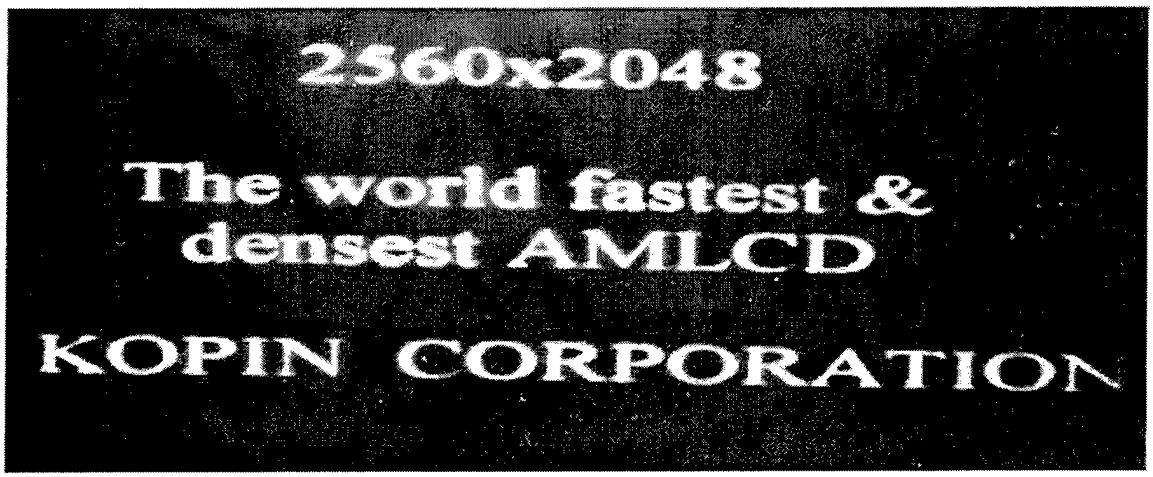


Figure 3-8. Screen Photos of 2000 LPI, 2560x2048 AMLCD Display

4.0.Future AMLCD Development Tasks

The 2000LPI, 2KAMLCD demonstrated the potential for high performance, large array displays in sizes optimized for HMD applications. The operational displays demonstrated lacked some of the promising technologies developed which had too much technical risk to include in the demonstration displays produced. The following discussion outlines these and other technology areas which are being addressed and areas which should be addressed.

An insertion project for the 2000 LPI, 2560x2048 AMLCD or other 2000 LPI display would not require the implementation of all these new technologies. The following changes are desirable:

1. The second metal layer or a silicide process must be added for a 60 Hz frame rate.
2. Circuit changes to run in column inversion mode are required to eliminate flicker.
3. A narrow gap assembly process (~ 2 um) for high contrast and high aperture efficiency.
4. A data scanner design which automatically matches multiple channel video levels.
5. An LC side ITO pixel for high light level applications such as projection and heads-up.

4.1. Further Pixel Improvements

Although the test array results produced by Sarnoff were not totally satisfactory, this body of work produced results that were valuable to the 2000 LPI, 2560x2048 AMLCD pixel design and will be a useful reference for future designs. Parallel studies at Kopin complemented the Sarnoff test array studies. The following discussion highlights some promising pixel improvements.

4.1.1. LC Gap Reduction

Cell gap reduction is the most effective method of intensifying the fields across the gap, thereby reducing voltage requirements, speeding up LC switching and reducing LC disclinations caused by adjacent pixel voltages and by row and column line voltages. The extent of the disclinations is approximately equal to the LC gap dimension. Narrow gap assembly is in the latter stages of development and will be available for future display products. The narrow LC gap assembly process also reduces the required display voltages and the power required to operate them.

4.1.2. Pixel Light Transmission improvement

Pixels contain multiple internal layers which cause a substantial loss in transmitted light owing to internal optical reflections and light absorption. The LC side ITO pixel electrode can increase light transmission by 300% over polysilicon and silicon electrodes. In addition to the increased transmissivity of the ITO structure, the reduction of field distortions allows larger pixel apertures. Decreased LC drive voltages also reduces display circuit power. Higher light transmission is desirable for projection applications, heads-up displays, and to reduce display and backlight power.

4.2. Color Display Implementation

4.2.1. Color Filters

A viable color filter technology was developed. Process steps were developed and added to the front-side display circuit fabrication process. Colored polyimides are spun directly on

to the display circuits and patterned using photo-masks. Following wafer transfer, the filters are effectively encapsulated by the transfer adhesive between the circuit and the display glass. Encapsulation was found to be beneficial because the filter material was stabilized with no fading or color changes during high temperature life testing. This process was tested on lower resolution displays with good success.

Colored polyimides are spun directly on to the display circuits and patterned using photo-masks. The color filters completely fill the active pixel areas so that all light must pass through the filters. The color filter process development was considered successful but was shelved in favor of the much more promising color sequential approach. The discussion below compares these two approaches.

4.2.2. Color Sequential Color Approach

Heretofore, color sequential implementations have been unsatisfactory, having cumbersome mechanical scanners, flicker, or other problems. Circuit speeds have not been fast enough, and implementation on AMLCD's has not been possible due to the slow response of the LC materials.

The two major elements required for color sequential operation of transmissive displays are a high frame rate to avoid flicker and a color sequential back light supplying red, green and blue light in synchronism with the display frames. Kopin x-Si display circuit technology enables high frame rates through high circuit speeds. Kopin has also developed liquid crystal materials with fast response times. LED (Light Emitting Diode) technology has developed to the point where high efficiency red, green, and blue diodes are available for the backlight.

AMLCD's have typically used filters to provide color operation; these are widespread in use in laptop computers. However, the advantages of color sequential over color filter technology for AMLCDs are many:

- Higher yields and lower cost because the number of pixels required for a given array size is reduced by a factor of 3 or 4 (depending on the color filter layout replaced, triad or quad.). A VGA Color display required a 640x480 array with color sequential operation compared with the 1280x1024 pixel array required with a quad pixel color filter layout.
- Brightness is increased by almost 6 times by the increased pixel aperture ratio.
- Brightness can be additionally increased 3 times by elimination of color filter losses.
- Color saturation and brightness increase while reducing display and backlight power.

The color sequential advantages are illustrated by the quad-pixel color filter arrangement compared with a larger single color sequential pixel shown in Figure 3-9.

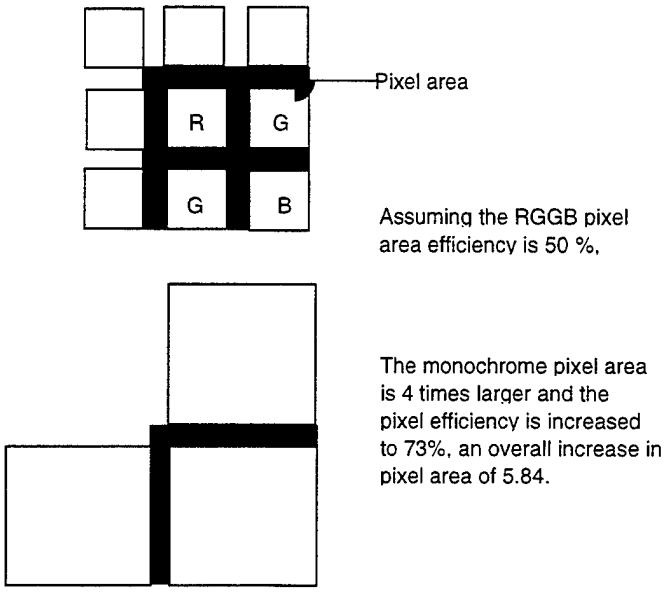


Figure 3-9. Pixel aperture efficiency increase by color sequential design

The 5.8 times increase in brightness illustrated above is not completely realized unless the backlight colors scan in synchronism with the color data loading with no dark bands. This is not possible because the LC must be allowed to switch and settle before illumination starts. If the LC settling time is assumed to be half the cycle time, the increase is reduced to a factor of 3; however, color filter removal provides an addition 3 times increase.

Alternating red-green-blue pulsed lighting without scanning simplifies the back light at the expense of more dark time between colors to load the active matrix and wait for the last pixels loaded to settle. This operational mode requires the use of pulsed high intensity, high efficiency devices so that illumination pulses can be short. Color balance and brightness are done by adjusting color pulse widths and drive power. This mode is used by Kopin's Cyberdisplay™ using red, green and blue LED's for the pulsed color sequential backlight.

Short LC response times and fast circuits fabricated in single crystal silicon (x-Si) have recently been achieved by Kopin allowed the successful development of a color sequential 320x240 pixel color sequential display which uses LEDs for sequential red, green and blue back lighting. The Cyberdisplay runs at a 180 Hz frame rate for an effective 60 Hz frame rate, displaying a flicker-free color image. The Cyberdisplay has 15 um pixels and a picture diagonal size of 0.24". Its backlight consumes only 30 mW of power. The CyberDisplay demonstrates the effectiveness of color sequential AMLCD display technology; however, the extension of the technology to a larger array displays requires improvements in the display, the backlight and the driver electronics.

The fast frame rate for large array displays causes a data bandwidth problem. 180 Hz frame rate operation for color sequential allows 5.5 msec to load the pixel array with the respective color video, to allow time for LC switching and to pulse the color LED. Allowing 3.5 msec for LC settling and pulsing the LED leaves 2 msec for loading the array. As an example, the effective data rate required to load an 800x600 SVGA array in

2 msec is 1.92 x 10^9 bits/sec. Using parallel channels to load more pixels in parallel can effectively lower the data rates. Six channels (assuming digital 8-bit gray scales) reduces the data rate to 30 Mbytes/sec on each channel. Thus Kopin's fast x-Si circuits and the use of parallel channels are to lower bandwidth requirements.

The scanner speed issue discussed in paragraph 3.3 must be addressed to achieve a 180 Hz frame rate. The second metal and silicide processes may not support 180 Hz. A true 2-level metal interconnect process may be required. This should not be very difficult because 2 or more metal levels are commonly use for IC's. It will add extra process steps and incremental costs.

The LC must be fully settled for an acceptable 800x600 resolution image. Illumination time cannot overlap settling time to avoid variations in color and brightness over the displayed image. If the LC in the last pixels loaded at the bottom of the screen has not completely switched, the color and hue there will be different than that at the top of the screen. Thus the LC switching time must be decreased from its present 10 msec + to the shortest time possible. Short switching times obtained by over driving the LC are not applicable for gray scale displays because switching times between shades of gray are longer. Recent LC switching time data for ECB materials is under 2 msec. This material requires narrow LC gaps with very tight tolerances. See paragraph 4.3.

A scanning backlight will allow more time. For even larger arrays, the video data loading time plus the LC switching time and the LED illumination time will likely exceed the 5.5 msec allowed by the180 Hz frame rate. Overlapping of data loading and illumination times can be accomplished with a scanning backlight which scans red, green and blue light bands down the display interspersed with black bands where data is being loaded for the following color band. A mechanical scanner approach has been developed for other projects. The mechanical scanner works well in projection applications but not for HMD applications. Kopin has proposed a scanning backlight using an electronically scanned LED array. The LED approach does not allow quite as much display and loading time overlap but is estimated to double the time allowed for data loading.

4.3. LC material improvements

Liquid crystal materials were studied by the University of Colorado using test pixel arrays to evaluate the potential of ferroelectric liquid crystals (FE LC's) for high contrast ratio, speed, and greyscale. FE LC's showed promising performance in the test array. High liquid crystal switching speeds and high contrast were demonstrated; however, the immaturity of the processes left too much risk for use on the 2560. FE LC's are under consideration for future display applications. These LC materials are particularly attractive for fast display applications such as for 180Hz frame rates for color sequential displays and for applications where fast moving images would cause smearing with a slower LC material.

The application of the CSLC materials requires a narrow LC cell gap which must be well controlled to avoid image performance variations between displays and even across the

same display. The gap dimension selected was 1.9 μm with a control objective of < ± 0.1 μm. Test cell gaps were set by fabricating photo-polymer (photo-BCB) cell walls as shown in figure 3-10. The photo-BCB material can processed as photoresist: spun-on, cured and patterned to form the spacer walls. After characterization, this process provided the required spacer height control. The LC filling process is affected by the cell walls and their design must allow flow for complete filling. The presence of the walls was found to cause LC alignment variations which produced image anomalies which appeared as "zig-zag" patterns. Similar effects were observed in other spacer experiments at Kopin. This problem remains to be completely fixed but it appears that for actual display applications, the effect can be hidden if the spacers are located around the perimeter underneath the black matrix. Larger displays require interior spacers to prevent gap variations. Spacer location underneath the black matrix pattern between pixel apertures may hide their effects but experiments remain to be done.

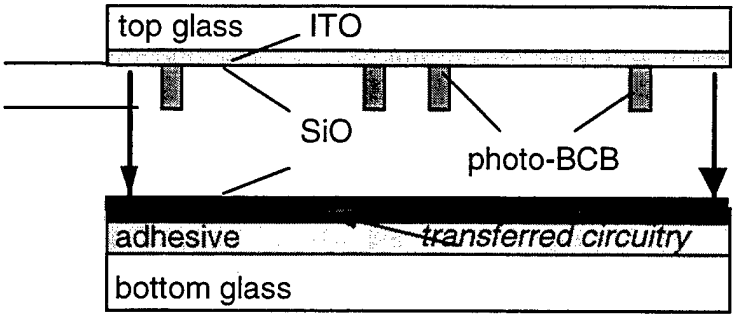


Figure 3-10. Photo-definable LCD cell walls and gap control using photo-polymer.

Table 3-5 is a summary of CSLC results with comparative nematic LC materials. High switching speeds at low voltages and high contrast ratios are demonstrated

Kopin LC development results which overlapped the U.C. research produced similar results. Kopin's LC assembly process will support the use of materials which switch in 2 msec. Further development is required to provide the stringent gap tolerances required by some materials.

Table 3-5. Test cell results for Kopin 2000 DPI AMLCDs

Material	ZLI3654	SCE13	764E	E7	E7	PTTP
LC phase	SmC*	SmC*	SmA	N	N	N
Tilt angle	±25°	±22.5°	±12°			
Δn	.13	.14	.16	.22	.22	.5
Assembly:						
Cell gap [μm]	1.9	1.9	1.9	1.9	.9	.6
Aperture [in]	1x1.2	1x1.2	1x1.2	1x1.2	.7x.7	.5
Alignment	N6 ,||	N6, ||	N6, a-||	N6, ||	SiO_x, ||	N6, a-||
Contrast ratio[a]	1000:1	1000:1	80:1	700:1	30:1	35:1
λ/2 [nm]	507	580	596	725	422	590
% Transmission[a]	90%	90%	87%	90%	84%	85%
τ_{rise} [ms][a]	.11	.10	.06	1.15	.80	.72
τ_{fall}[a]	.11	.10	.06	.62	.30	.15
Voltage [V][b]	±5	±5	±10	6	6	7.3,16.2

[a] measured at 633 nm. [b] for nematics, RMS values are given.

4.4. **Display power, weight and size reduction**

The reduction of display power consumption, weight and size are critical issues for mobile and wireless systems applications. Reducing power alone reduces mobile system size and weight because smaller, lighter batteries can be used. Kopin's displays already consume less power than other approaches because the x-Si circuits operate at lower voltages than a-Si or polysilicon circuits. The recent development of lower voltage LC materials allows further circuit voltage reductions, thereby saving power proportionally to the voltage squared. Cutting the voltage by half will reduce the power by a factor of four.

Narrow LC gap assembly and LC side ITO pixel electrodes reduce the display drive voltages required as discussed above.

The reduction of display circuit voltages involves redesign starting with the basic circuit components. The reduction of MOS transistor voltages causes a slow down in response time, a problem to resolve in achieving 180 Hz frame rates. Gate oxide thickness and device sizes are two of the parameter variables which can be used to counteract the bandwidth reducing effects of lower voltages.

The overlapping of operations described above also saves power because circuit power is proportional to clock rate. The integration of external drive functions into low power processors can also save space and power. New low voltage, lower power IC's are becoming available which can be used for external data conversion and drive functions.

4.5 **Wide temperature range operation**

Although low power display operation is highly desirable for portable electronics in the field, a major problem with LC displays is their inability to operate at low temperatures. The x-Si circuit transfer process allows the integration of a temperature control system onto the display circuit chip. The control system will extend the operating range to lower temperatures. Higher temperature operation is achieved by selection of the LC material used. A wide operational can realized by this system. The display's image consistency in color, hue and contrast will be significantly improved by keeping the LC at constant temperature.

The regulation of temperature of an AMLCD is important to operations outdoors or in applications where the temperature of the liquid crystal exceed the ideal operating range of 30C to 50 C. This innovation comprises (1) temperature sensor, (2) a method of heating the liquid crystal, and (3) a regulator circuit to maintain the liquid at a constant temperature. All these elements can be integrated into the CMOS display circuit.

Using resistive elements inside the display, heat is applied directly to the liquid crystal material. The liquid crystal is confined between two sheets of glass which are good insulators. Thus the application of heat required will be very small, in the milliwatt range. This innovation is vastly superior to LC heaters which use a heater on the outside of the display glass. The poor heat conductivity through the glass and other parts which receive heat results in a much higher heating power requirements and the LC temperature response is slow. We will be applying heat directly to the LC between the two display glass substrates. In this case the poor heat conductivity of the glass is beneficial, insulating the LC so that little heat escapes. The thicknesses of the insulating glass substrates are more than a hundred times as thick as the LC material, The volume of the LC material to be heated is very small, about 0.02 mm^3. With the low thermal mass of the LC, the uniform heating, and the glass insulation, the regulator will provide fast display turn-on measured in seconds and constant LC temperatures for long term image quality and consistency.

5.0. AMLCD Conclusion

AMLCD technology has been advanced significantly by the DARPA x-Si based miniature display development program which began about 5 years ago. Each project was extremely aggressive making it very difficult to achieve all of the performance objectives; however, every AMLCD display developed is operational and was demonstrated. What was learned on the VGA was applied to the XSVGA which provided data for the 2560x2048 display. Along the way a rich repertoire of display manufacturing technologies has be assimilated into Kopin's display production process. A critical mass was reached in the production of Kopin's first viable display product, the CiberDisplay320 which is a 320x240 pixel (Quarter VGA). The CyberDisplay received a 1997 "Product of the Year Award" from Electronics Magazine, one of eight chosen from about 20,000 products reviewed by the editors. This tiny ¼ inch diagonal display is available in monochrome and in color sequential. This display demonstrates the x-Si display advantages foreseen in the first proposal over five years ago. Over 200 circuits are produced on each 6" wafer with yields around 90%, allowing this display to compete in the consumer electronics market. Color sequential operation demonstrates the speed advantage of x-Si and marked LC speed increases. Kopin's product roadmap includes displays of increasing array size and increased resolution over the next few years.

Additional funding is required to accelerate Kopin's product evolution. The recent funding and proposed additional funding of a 2000 LPI, 1280x1024 AIHS/Comanche display is helping to leap frog commercial products. This display will include some of the improvements discussed in paragraph 4. The first lot of the new 1280x1024 display produced operational displays with impressive images which are now being evaluated. The insertion of this complex display and others can be accomplished with relatively low development costs using the standard circuit designs and production processes which are now in place, primarily as a result of DARPA's vision and funding.

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