Microlithographic Mask Development (MMD)

CDRL H007: Option 3 Contract Summary Report
CDRL H004: Contractor Progress, Status, Management Report

22 January 1999

Contract Number N00019-94-C-0035

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ENCLOSURE NO: 99-MMD-LMFS-00003

Prepared for:

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Contract Number N00019-94-C-0035
Lockheed Martin Federal Systems

Lockheed Martin Federal Systems, Manassas, Virginia

Certification of Technical Data Conformity

The Contractor, Lockheed Martin Federal Systems, hereby certifies that to the best of its knowledge and belief, the technical data delivered herewith under Contract Number N00019-94-C-0035 is complete, accurate, and complies with all requirements of the contract.

1/28/99

Date

T.F. Jamba, Program Manager

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1.0 Introduction

This document provides the data required under contract N00019-94-C-0035 in accordance with CDRL H007, Option 3 Contract Summary reporting on the period from 25 December 1997 through 31 December 1998, and CDRL H004, Contractor Progress, Status, Management Report, 4Q98, covering the period from 01 September 1998 through 31 December 1998.

A final report documenting the work at IBM Yorktown is provided as Appendix A. The final report for the SVGL activity will be delivered separately as an addendum to this document upon completion of the SVGL aligner activity which is currently extended through March, 1999.

Program Summary

During Option Year 3, the primary focus has been the complete implementation of the refractory process in the MMD, and optimization of the associated processes and tooling. The major tooling development was the qualification of in-house deposition systems for refractory metal, hard mask and etch stop. There were also two major upgrades at EL-4+ P0: a conversion to smaller fields and subfields, and the table laser upgrade. A new bake/develop tool was also installed and qualified. The major developments in the process area were the completion of both the UVIII etch design-of-experiments (DOE) and the UVN2 resist process DOE. The MMD now has a stable 130nm etch process.

The MMD schedule is shown in Table 1 on page 3, and the MMD contract deliverables are shown in Figure 1 on page 4.

In addition, a three-month capacity demonstration was initiated on 24 August 1998 to demonstrate MMD's manufacturing capability by shipping 50 product masks, to customer specifications, within a three month period. A successful two week preliminary demonstration was completed in June: a total of 70 masks were fabricated during the two week period with an average BEOL turnaround time of 1.5 days and 18 masks were shipped to customers.

The three-month demonstration was suspended after 11 weeks due to vibrations and electrical noise caused by nearby construction, as well as a process shift caused by maintenance of the SiON etch system. During the 11 weeks, 37 masks were shipped against customer specifications, 95% availability was achieved on EL-4+P0. Three hundred and thirteen masks were exposed.

Highlights

- The MMD now has the capability for Cr, SiON, and TaSi deposition. All mask processing is done in the MMD facility.
- An annealing furnace from Eaton Corporation was installed in the MMD and qualified.
- A Tencor FLX 5510 stress measurement tool was installed in the MMD and qualified.
- An SSI bake/develop tool was installed in the MMD and qualified.
- An EL-4+ P0 upgrade to smaller fields, subfields and exposure spot was completed, as well as a table laser upgrade.
- The array mode software was installed on the KLA SEMSpec and is operational.
- The UVIII positive resist etch process DOE was completed and process changes were implemented.
- The UVN2 negative resist process DOE was completed. The optimum process conditions were determined.
- A two-week preliminary capacity demonstration was completed. Seventy masks were fabricated in a two-week period, with a 1.5 day average BEOL turnaround time.
- A three-month capacity demonstration is underway.
- Seven product Power PC masks were shipped to the Advanced Lithography Facility (ALF); image size 3σ on Power PC average below 15nm. A total of nine defect-free masks were shipped.
- Fifteen Advanced DRAM masks (nine product, six EWR) were shipped to the customer (ALF).
- Four product quality MMIC (monolithic microwave integrated circuit) masks (130nm and 100nm) were shipped to Sanders.
- Resolution of 75nm was demonstrated on an ALF line monitor mask.
- A multiple pass exposure process was brought online for both UVIII positive resist and UVN2 negative resist.
- Image placement of 20nm was demonstrated on the Falcon line monitor. Image placement of 23nm was demonstrated on Power PC.
- Image size control of 7nm was demonstrated on the Nighteagle line monitor. Image size control of 5nm was demonstrated on an MMIC mask.
- An advanced materials team was established to investigate the viability of future substrate materials. The team is comprised of representatives from IBM Yorktown Research and the MMD.

- An evaluation of Crystallume diamond films was initiated. A 50×50mm^2 diamond membrane was fabricated, as well as a Falcon mask and a Nighteagle mask.
- Ta_4B film depositions were completed with the MMD SFI deposition system.
- Six Technical Interchange meetings were held this year, as discussed in Section 7.0.

Table 1. 1998 MMD Objectives

	1Q98	2Q98	3Q98	4Q98
Line Monitor	*0.13μm Ref Proto* *Defects: TBD* *5 starts/wk* *IP=35nm,CD=20nm*	*0.13μm Ref Proto* *Defects: TBD* *5 starts/wk* *IP=30nm,CD 20nm*	*0.13μm Ref Proto* *Defects: TBD* *5 starts/wk* *IP=25nm,CD=15nm*	*0.13μm Ref Proto* *Defects: TBD* *5 starts/wk* *IP=25nm,CD=15nm*
Product Applications	*64Mb SRAM test site* *1Gb SRAM test site (Viper)* *IBM Logic test mask* *IBM Memory test mask* *OEM Orders*	*64Mb SRAM test site* *1Gb SRAM test site (Viper)* *IBM Logic test mask* *IBM Memory test mask* *OEM Orders*	*256Mb SRAM test site* *1Gb SRAM test site (Viper)* *IBM Logic test mask* *IBM Memory test mask* *OEM Orders*	*256Mb SRAM test site* *1Gb SRAM test site (Viper)* *IBM Logic test mask* *IBM Memory test mask* *OEM Orders*
MMD Contract Deliveries	*0.18μm/0.13μm masks*	*0.18μm/0.13μm masks*	*0.18μm/0.13μm/ 0.10μm masks*	*0.18μm/0.13μm/ /.10μm masks*
		Technology Learning		
	EL-4+ P0 laser upgrade	*Order thickness measurement system*	**UVN2 resist qualification**	**Evaluate e-beam patterning h/w improvements**
	Absorber deposition system qualification	**TaSi deposition development**	**Install rapid thermal anneal system**	*Install SiC absorber stack clean system*
	KLA array mode software installation	**Fountain cup etch system acceptance test**	**Optimum TaSi stack**	*Install wafer flatness tool*
	Stress measurement system qualification	**Defect reduction demonstration at 50nm**	**Evaluate Ta_4B stack**	*Install backside lithography system.*
				EL-4+ P0 magnetics upgrade
		Build defect-free line monitor baseline	**Evaluate multi-pass patterning on CAR**	*Optimize sub-130nm etch*
		Order substrate defect inspection system		
		Order analytical SEM		
		Evaluate diamond films		

Note: Highlighted text indicates completed activity.

0.18um DEFECT REDUCTION

Qty=15, Defect Free, CD 3 sigma=30nm (goal=18), I/P=44nm (goal=20), CD mean=166-194
(I/S=25; I/P=26, Defect Spec Applies For May - Nov Shipments)

	J	F	M	A	M	J	J	A	S	O	N	D
Schedule	1	1	1	1	1	1	1	1	1	2	2	2
Actual	1	1										

0.18um PROTOTYPE

Qty=36, Not Defect Free, CD 3 sigma=30nm (goal=18), I/P=44nm (goal=20), CD mean=166-194

	J	F	M	A	M	J	J	A	S	O	N	D
Schedule	3	3	3	3	3	3	3	3	3	3	3	3
Actual	3	3	3	3	3	3	3	3	3	3	3	3

0.13um PROTOTYPE

Qty=8, Not Defect Free, CD 3 sigma=20nm (goal=12), I/P=30nm (goal=18), CD mean=120-140

	J	F	M	A	M	J	J	A	S	O	N	D
Schedule		1		1		1		1	1	1	1	1
Actual		1		1		1		1	1	1	1	1

0.10um PROTOTYPE

Qty=4, Not Defect Free, CD 3 sigma= 16 nm (goal=08), I/P= 20 nm (goal=10), CD mean= 90-110
No Catrastrophic Defects, Up to 3 Defective Areas

	J	F	M	A	M	J	J	A	S	O	N	D
Schedule							1		1		1	1
Actual							1		1		1	1

Figure 1. MMD Contract Deliverables (January - December, 1998)

2.0 Validation Study (Task 1)

Task Objective: Develop a pilot line validation study for the production of masks with test and/or circuit patterns that use 0.18μm and below design rules.

2.1 Validation Plan

The Validation Plan (CDRL G001) was updated in accordance with contract requirements during 1Q98 (reference 98-MMD-LMFS-00018). No additional updates to the Validation Plan were scheduled.

2.2 Nighteagle/Falcon Manufacturing Measurement Vehicle

2.2.1 Nighteagle/Falcon Writes Per Plan

The number of Nighteagle and Falcon writes per plan are shown in Figure 2 on page 8. The line monitor exposure target of three exposures per week was consistently met throughout the year with two exceptions. There were no exposures between 08 December 1997 and 26 January 1998 while EL-4+ P0 was down for a small field/subfield upgrade. In addition, there were no exposures between 26 April and 17 May 1998 during an EL-4+ P0 table laser upgrade. There were also two periods when exposures peaked. A preliminary capacity demonstration was completed between 28 May 1998 and 11 June 1998 in preparation for a three month capacity demonstration which began on 24 August 1998. The demonstration was suspended after 11 weeks, but the volumes through exposure have remained high due to engineering evaluations.

2.2.2 Nighteagle/Falcon Yields

Yields for Nighteagle and Falcon masks were measured for overall yield and for the individual yields of image size, image placement and defects. The targets are 80%, 80% and 25% for image size, image placement and defects, respectively. The overall yield target is 16%

2.2.3 Image Size

Image size results for line monitor masks are shown in Figure 3 on page 8. During the first quarter, enhancements made in the etch process, as well as better control seen at the EL-4+ P0 due to smaller fields, contributed to improved image size performance on line monitors. During the second quarter, line monitors averaged $<$20nm 3σ and yield to 15nm was $>$50% on Power PC masks. Nighteagle image size performance remained stable throughout the year with 7nm achieved and $>$70% yield at 20nm 3σ. There were problems, however, with Falcon performance. As reported in

the third quarter, image size degradation on the membrane edge (approximately 2mm from the edge) caused unacceptable 3σ results. A helium cooling backing plate in the silicon oxynitride etch tool had been installed improperly, causing non-uniform cooling. When the plate was returned to its proper position, etched image size 3σ improved. However, this introduced a process shift which resulted in smaller overall image size. The process has been re-optimized and is back on-line.

2.2.4 Image Placement

Image placement results for line monitors are shown in Figure 4 on page 9. Significant progress was achieved with image placement during 1998. Image placement on masks fabricated with films deposited at Motorola PCRL in 1997 was optimized at between 40-60nm. As masks were fabricated with film deposited in the MMD, more control of the deposition conditions and resulting stresses led to better image placement performance, as expected.

In mid-February, work began to determine the TaSi and the hard mask stresses that would minimize the BEOL image placement movement. By mid-April the stress conditions were determined, and in mid-May masks were fabricated with these films. Falcon yield at 44nm was >50% during the preliminary capacity demonstration between 27 May and 11 June. A Falcon mask with 27nm image placement was fabricated with single pass exposure.

It was determined that multiple pass exposures would be required to achieve reasonable yields at 30nm. Work began in June to bring a multiple pass process on-line in July (see 4.2.1). Initial exposures showed a 20% improvement in mask-to-mask repeatability and it was determined that a 5-7nm improvement in image placement would be realized. A stable product specific emulation (PSE) was installed on 29 July and masks results were excellent. Twelve Falcon masks were made with image placement 30nm or below, with two masks measuring 20nm. Yield on product SiC substrates was >50% at 30nm.

Results on Nighteagle masks were less impressive. As referenced in previous progress reports, repeatability with SNR resist was not as consistent as with UVIII resist, which resulted in less effective PSEs. While <40nm image placement was demonstrated, yield and consistency of results were unacceptable throughout the year. Recent results with UVN2, the new negative resist, show comparable repeatability to UVIII. Final image placement of 30nm was demonstrated with multiple pass exposure and UVN2 resist. Optimization for yields continues.

2.2.5 Defect Learning

The defect learning for line monitors is shown in Figure 5 on page 9. Defect performance has improved consistently throughout 1998. High defect levels were seen through the first three months of the year, mainly driven by substrate (SiC and TaSi deposition) and process (extra shapes caused by noise problems at EL-4+ P0)

defects. All of these areas showed improvement in the second quarter. Hoya made significant improvements in SiC quality. TaSi depositions made on the MMD SFI system showed >2× improvement in TaSi-related defects, and EL-4+ P0 resolved the noise issues that caused the extra shape defect. Total defect density averaged approximately 10/cm^2 for the remainder of the year, while the total number of non-repairable defects decreased from around 60 on some Falcon masks to typical performance of <10 by the end of the year. In addition, nine defect-free Power PC masks were shipped to the ALF. Implementation of the sacrificial layer in the FEOL significantly reduced the front-side membrane damage that was seen as non-repairable clear defects in the final mask. Work is ongoing to fabricate defect-free Falcon and Nighteagle masks.

2.3 Viper Prototype Test Vehicle

The 180nm Falcon (UVIII) and the Nighteagle (UVN2) are the current line monitors. (No 130nm full Viper line monitors were exposed in 1998.) Each line monitor has two 130nm test sites in the kerf which are used for process development at 130nm. There has been improvement in the etch process in recent months. During April, a DOE was completed for the UVIII positive etch process. Several mask orders were completed that include 150nm, 130nm and 100nm nominal images, while 75nm image resolution was realized on one mask order. Limited success has been achieved on 130nm and lower images.

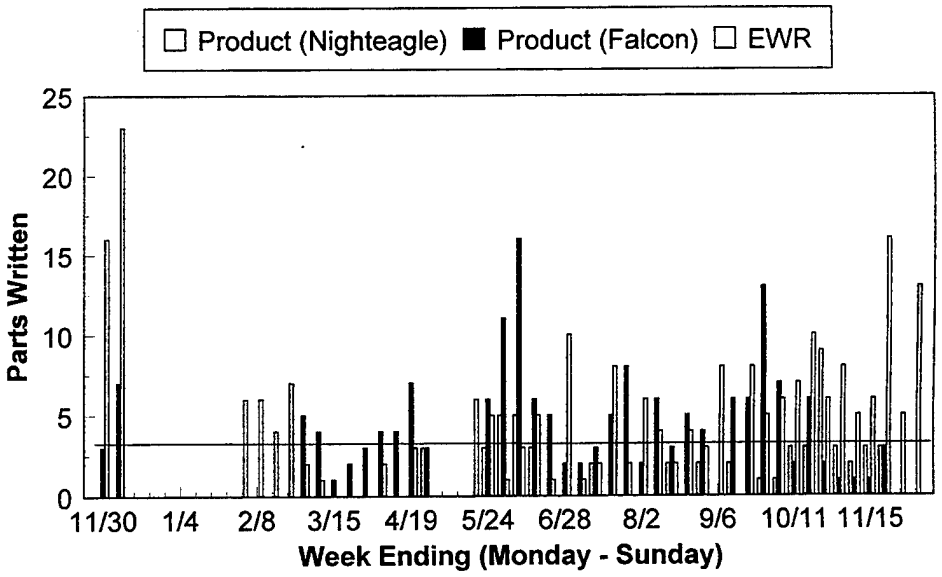


Figure 2. Line Monitor Writes per Week

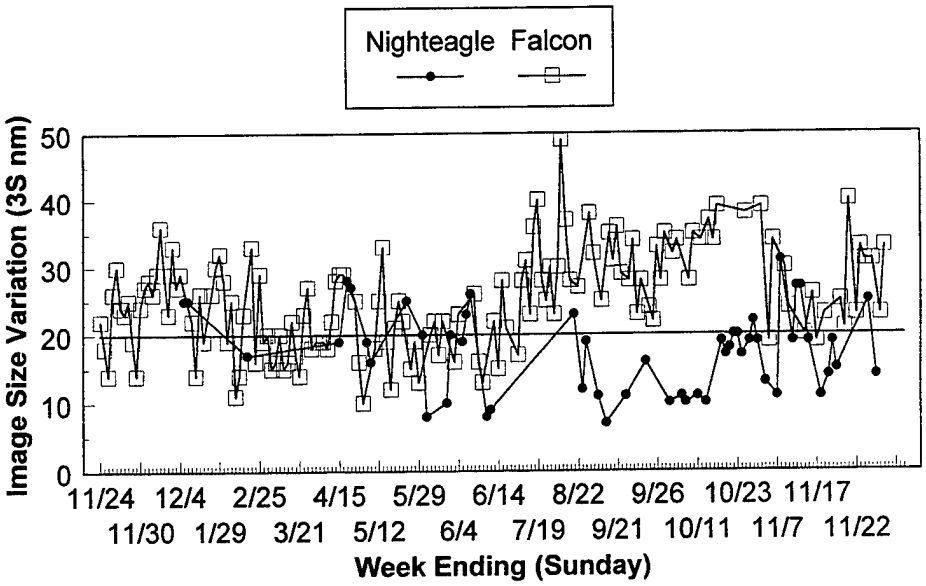


Figure 3. Image Size Variation (Line Monitor)

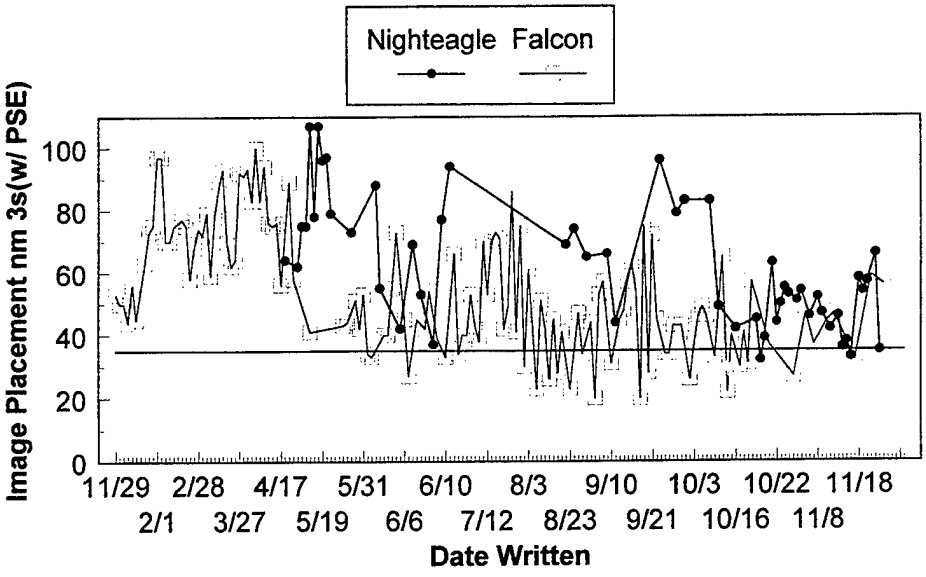


Figure 4. Image Placement (Line Monitor)

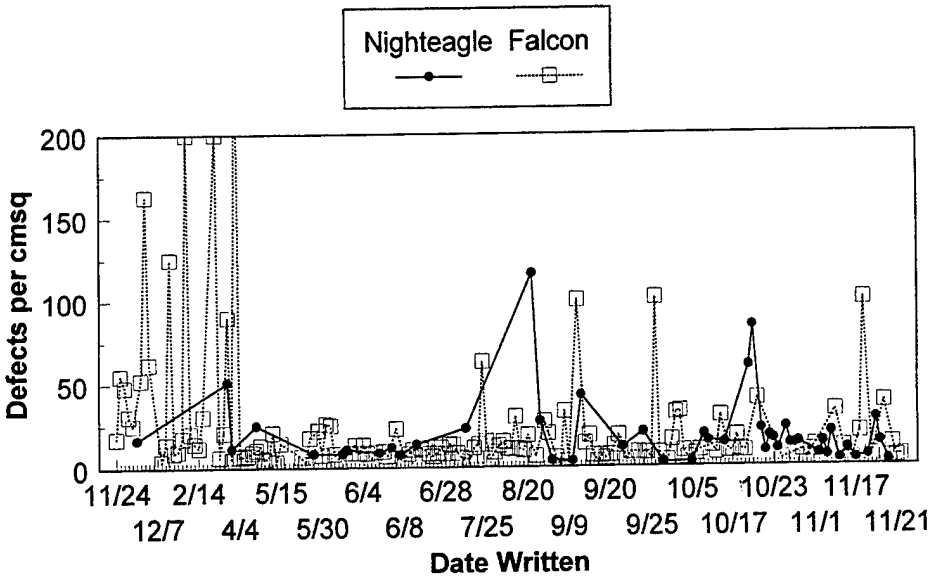


Figure 5. Defect Density (Line Monitor)

3.0 Roadmap Activities (Task 1)

Task Objective: Devise a comprehensive MMD technology roadmap.

3.1 Technology Roadmap

The Technology Roadmap (CDRL G002) was updated during 1Q98 in accordance with contract requirements (reference 98-MMD-LMFS-0019). No additional updated to the Technology Roadmap were scheduled.

3.2 Metrology, Inspection and Repair

3.2.1 Substrate Defect Inspection System

With a system sensitivity higher than 2μm on the TaSi/SiON film stack, the MMD's current Q.C. Optics defect inspection system, used to inspect x-ray mask substrates, must be replaced.

A specification of requirements was sent to Inspex, Q.C. Optics, KLA-Tencor, Eutecnics and Applied-Orbot. Only Inspex has expressed interest in building the system, using their new "Eagle" system as a base and modifying the handler. The Inspex "Eagle" system was evaluated in March and the results are given in Table 2.

Table 2. Results of Inspex "Eagle" Evaluation

Films	Sensitivity Demonstrated (μm)	Repeatability Demonstrated
TaSi/SiON	0.126, 0.157, 0.204, 0.238, 0.404, 0.486, and 3.063	1.9% C.O.V. for random defects 0.9% C.O.V. for 0.157μm defects
Si bare	0.157, 0.204, and 0.496	
Cr	0.15	
TaSi/Cr	0.2	
TaSi/SiON/Resist	0.15	

C.O.V. - Coefficient of variance

IBM plans to purchase an Inspex "Eagle" substrate defect inspection system, and will modify the tool to handle x-ray masks. IBM funding for this project is planned for 1999. The updated schedule is shown in Figure 6 on page 17.

3.2.2 Advanced KLA SEMSpec Inspection Project

A joint statement-of-work was developed between the MMD and Japan's Association of Super-Advanced Electronics Technologies (ASET) for an advanced x-ray mask inspection system to support the 150nm to 70nm inspection requirements. The joint specification is summarized in Table 3 on page 11.

Table 3. Advanced KLA SEMSpec Specification

Parameter	Specification		Mask Technology Generation
Target Ground Rule	150nm to 130nm	100nm to 70nm	
Minimum Image Size	120nm to 100nm	70nm to 50nm	
Sensitivity	26nm	14nm	97% Capture Rate
Throughput	30 minutes/cm^2		(Same as Current Tool)
Image Detectors	Secondary and Transmission		25kV (or higher) acceleration voltage for Transmission
False Defect Rate	4/cm^2		
Nuisance Defect Rate	4/cm^2		Detection of Image Placement and Image Size variation
Form Factor	NIST X-Ray Mask, 100 to 200mm wafers, EUV masks, Scalpel masks		
Mask Structure	SiC/Refractory, Surface Resistance Ohms/cm^2		
Mask Damage	< 0.001%		
Contamination Control (Process-induced defects (PDI))	10 at 26nm sensitivity 5 at 200nm sensitivity	10 at 14nm sensitivity 1 at 150nm sensitivity	Adders / m^2 / pass at inspection sensitivity Adders/m^2/pass at 150nm sensitivity (non-repairable)
Die Size	25mm×36mm (900mm^2)	25mm×44mm (1100mm^2)	Maximum size
Defect Review 1nm	0.60×0.60μm^2	0.35×0.35μm^2	Minimum scan field size System Resolution
Off Line Review Support	Amray AutoSEM		
Repair System Support	Micron Repair System		
Cost	1.3X current tool cost		
Reliability	MTTF: 1000 hr, MTTR 4 hr, Reliability: > 95%		MTTF, MTTR etc.
Safety and Ergonomics Specification	SEMI S2-93 and S8-95 and Sematech's Application Guide for SEMI S2-93 and S8-95"		
Documentation	Full operator and level one maintenance documentation		
Options			
Handling/Product Environment	Integrated SMIF input output. Class 1 environment		Immediate Availability
Die to Data Base Option	Design Languages Supported: GDSII, GL1		Future Option

3.2.3 Advanced Repair System Project

Discussions are underway with Micrion to build the next generation mask repair system to support 150nm to 70nm groundrule masks. An initial specification was sent to Micrion; capital funding from IBM is expected in 1999.

3.2.4 Substrate/Wafer Flatness Measurement System

The flatness measurement system currently used in the MMD, a Tropel Flatmaster, is not capable of measuring masks to the required specification. A project was started to develop a fully automated SMIF interface mini-environment system capable of inspecting x-ray mask substrates for out-of-plane flatness. The statement of work was sent to Veeco, ADE and Zygo. Zygo was selected because they met all system parameters and cost objectives. The project definition, costing, system concept, and evaluation have been completed with Zygo, and the project is awaiting IBM funding in 1999. The updated plans are shown in Figure 6 on page 17.

3.2.5 Analytical SEM

The MMD requires a higher resolution scanning electron microscope (SEM) to support the development of 100nm groundrule masks. The requested system specifications are shown in Table 4 on page 13, and the schedule is provided in Figure 6 on page 17. Funding for this project is planned for late 1999.

3.2.6 KLA SEMSpec Array Mode Inspection

Proximity X-Ray Lithography Association funding for the KLA SEMSpec array mode inspection software option was released in 1997, and the software was delivered and installed in March, 1998.

The array mode inspection software is specifically designed to inspect masks with repetitive patterns (e.g., DRAM and SRAM cells). The defect detection mechanism of array mode inspection is based on a cell-to-cell comparison (versus die-to-die mode with the current software). The defect detection algorithm looks for and flags as a defect any differences between two adjacent cells (within microns of each other); an arbitration algorithm will be used to determine the location of the defect. One advantage to running inspection in array mode is that by comparing images over such a short distance, the system will not be as sensitive to image placement errors and systematic image size errors. In addition, inspection of single die masks can now be performed in array areas, although not in non-repetitive support circuitry. Therefore, application is limited to memory devices with repetitive patterns.

Table 4. Scanning Electron Microscope Specification	
Parameter	**Specification**
Image Detectors	Secondary Everhart-Thornley Through the lens detector Robinson Backscatter Energy Dispersive X-Ray
Resolution	4nm at 1kV 1.5nm at 10kV 0.3nm at 25kV Vibration free micrographs at 0.6×0.6μm^2 (200kX) scan size.
Electron Optics	Gun: Field Emission Final Lens: 60° Conical to support micrographs at 45° angle.
Acceleration Voltage Ranges	Voltage: 0.600 to 25kV (Automatic Beam Alignment) Probe Current: 1pA to 10nA Probe Stability: 1% per hour (rms)
Stage	Five Axis's stage, eucentic stage calibration Automatic (laser) Z-height focus tracking better than 1μm X and Y travel: > 8 inches Mechanical Accuracy: < 5mm (3σ) z range: 25mm Tilt Range: 0 to 60°. Rotation 360° Continuous
Defect Review	100 defect per hour review speed Automatic (Laser) Z-track focus better than 1μm Support the following defect file format: KLA SEMSpec, Tencor 6420, IBM TFF format, KLA 300 Series Format.
Optical Microscope Support	Magnification of the Optical microscope should be 200x and 1000x. Imaging should be on the same monitor as the SEM images, and control integrated into the SEM and defect review functions
Short Term Precision	Less than or equal to 5nm (3σ).
Long Term Precision	Less than or equal to 5nm (3σ).
Form Factor	NIST X-Ray Mask, 100 to 200mm wafers, Optical Masks, 5″x5″ and 6″x6″
Mask Damage	< 0.001%
Safety and Ergonomics Specification	SEMI S2-93 and S8-95 and Sematech's Application Guide for SEMI S2-93 and S8-95″
Documentation	Full operator and level one maintenance documentation

3.2.7 Thin Film Stress Measurement System

Film stress is important for image placement control, and to control the stress level in the TaSi and SiON deposition system the MMD required a thin film stress measurement system. A Tencor Flexis 5510 thin film stress measurement system was installed, qualified, and released to production in March, 1998. The acceptance criteria was the system signal-to-noise; acceptance results are shown in Table 5.

Table 5. Flexis 5510 Acceptance Summary

	Resolution (1σ) for Average stress (MPa)		Resolution (1σ) for stress uniformity (MPa)		
Film Type	Specification	Actual	Specification	Actual	Phantom Film Thickness (nm)
Si	$\pm$2.5	0.75	8	0.77	500
TaSi	$\pm$2.5	0.49	8	0.73	500
N	$\pm$6.0	1.67	15	1.91	200
Cr	$\pm$40.0	10.92	120	17.35	20

3.2.8 KLA SEMSpec Adapter Change

A new adapter for the KLA SEMSpec was required to support inspection of the new SFI films. The SFI system leaves a 2mm ring around the mask with no metals (Cr/TaSi) deposited on it. The adapter for the KLA SEMSpec was redesigned to move the grounding points further in to achieve proper grounding. The adapter was implemented into production in June, 1998.

3.3 Process Equipment

3.3.1 SSI Develop Tool

Note: SSI has been purchased by FSI; the name of the company has been changed to FSI-Fremont, while the develop/bake tool remains the SSI develop/bake tool.

The SSI develop/bake cluster tool was qualified and released to production on 14 April 1998. The qualification results were reported in the 2Q98 Progress Report. The results indicated that the image size, image placement and defect results were similar to those of the controls.

During the third quarter, masks were occasionally rejected for improper alignment on the hot plate. New aligner and hotplate centering devices were installed by SSI field service in July. An adjustment was made to the optical aligner and the masks aligned correctly for several weeks. In late August, masks were occasionally misaligned, and the right side of the mask appeared to be under-baked. This was caused by expan-

sion of the rollers on the hotplate centering device which prevented the masks from sliding into the proper position on the hotplate. The three centering devices have been repaired by the supplier (FSI) and have been reinstalled on the system. All masks baked properly between 28 September, when the new devices were installed, and 18 October. Four masks were rejected for improper centering on the hot plate over a two week period in October.

The aligner angle (theta) was adjusted since the masks were catching on the notch locator of the bake centering device. The centering devices for all three ovens were readjusted at the new aligner theta position on 06 November. No further centering failures have occurred since these adjustments were made. However, the aligner failed to find the notch on two masks with faint stains on the Pyrex support rings.

The vendor is addressing the aligner failures with the following actions, scheduled to be completed by 29 January 1999. First, an aligner position for each of the three hotplates will be supplied by the software to improve the tolerances on each hotplate. Second, the vendor will provide a setup centering fixture to assure that the centering devices are properly installed. Third, the vendor will adjust the sensitivity of the aligner to avoid picking up blemishes on the ring instead of the notch. The supplier will also define a calibration procedure for the aligner sensitivity. These actions should minimize bake losses on the SSI tool.

3.3.2 Suss Automated Resist Coating System, Tool Status

A number of improvements to the Suss Automated Resist Coating System were implemented this year. The primary improvements included the installation of a new edge bead rinse nozzle, a new process recipe with a spin speed ramp up, and a new solvent that significantly reduced clear defects caused by edge bead solvent splatter. In addition, two software upgrades were installed on the system. The first upgrade was completed in late April to facilitate operation of the system; the second upgrade was installed on 14 October to facilitate the use of the robotic safety interlocks. The new software allows the system to reset the robot only, rather than requiring the entire system to reset, which improves turnaround time and prevents the pumps from losing their prime. The pumps have continued to lose their prime, however, when other tool errors occur. Suss is working with Millipore, the pump supplier, to determine the cause of this problem. Millipore suspects that the pump controllers are causing the pumps to lose their prime and they will visit the MMD to diagnose problem.

Removable GRYSET covers were installed on the Suss coater in late June. The original covers had jagged edges and required scraping to remove dried resist. The new covers, which are easily removed for cleaning, have a smooth edge which should reduce foreign material due to particle shedding.

3.3.3 Carbon Room Upgrade

The apply, bake and develop equipment located in the carbon-filtered room is critical for defect reduction. Measurements of particle counts on settling wafers indicated high particle counts for the HMDS oven, the stand-alone hotplates, and the UV blanket expose tool. Shrouds were installed over these tools to improve the air flow and particle counts. The settling wafers processed after the upgrade clearly indicate a 10× improvement in foreign material counts. KLA inspection data also shows a reduction of mesa (large, non-repairable opaques) which are caused by foreign material.

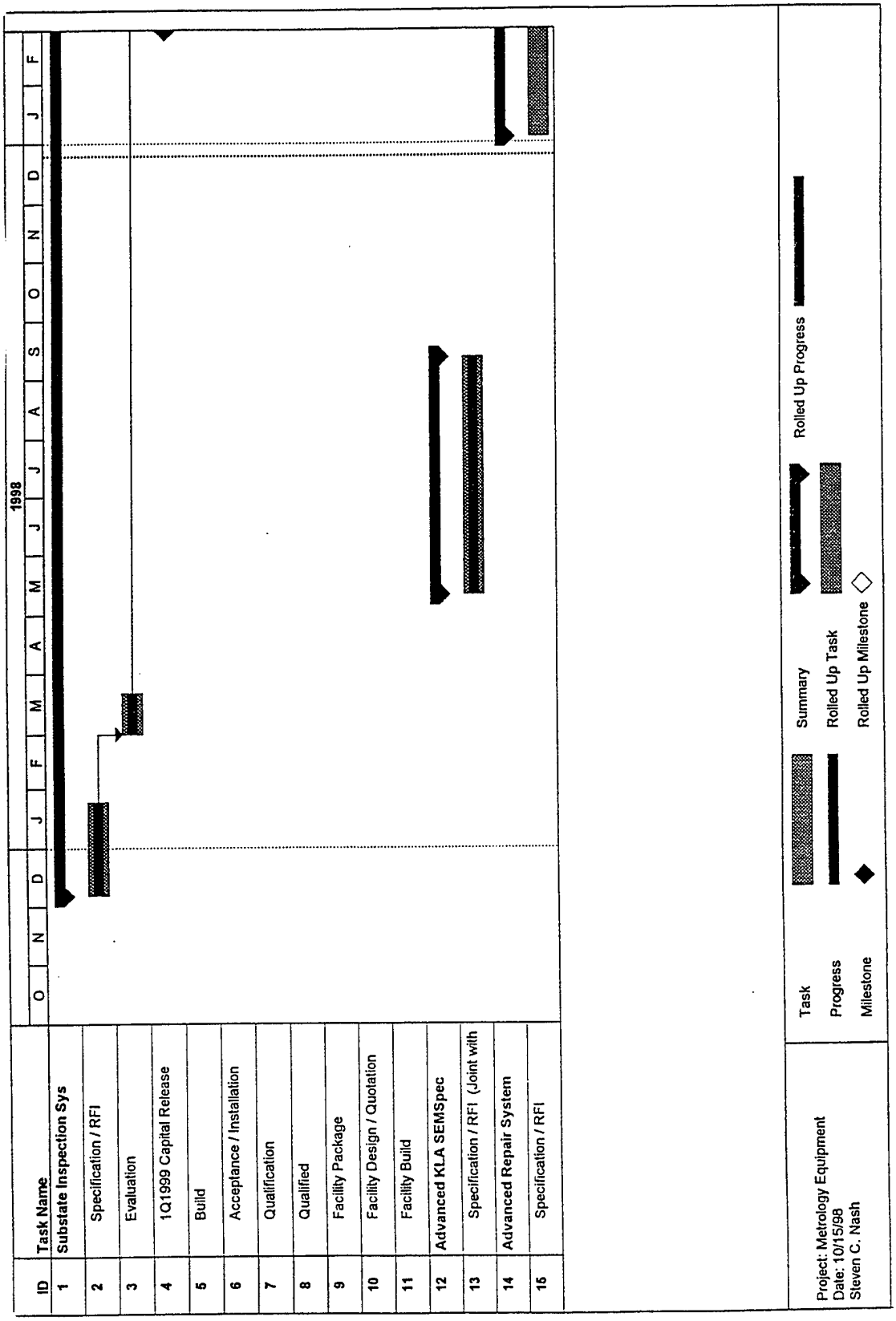


Figure 6 (Part 1 of 5). Metrology, Inspection and Repair Equipment Schedule

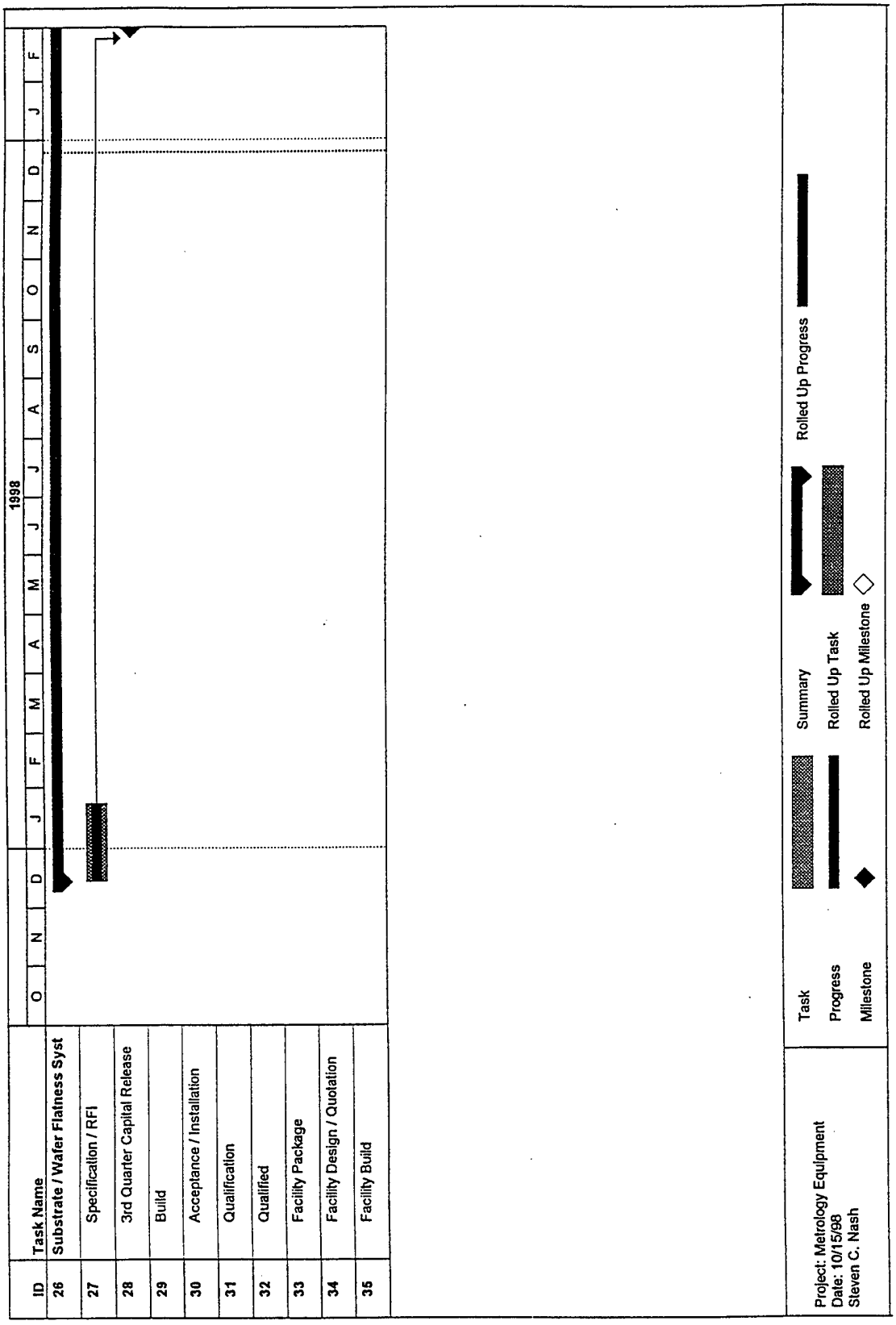


Figure 6 (Part 2 of 5). Metrology, Inspection and Repair Equipment Schedule

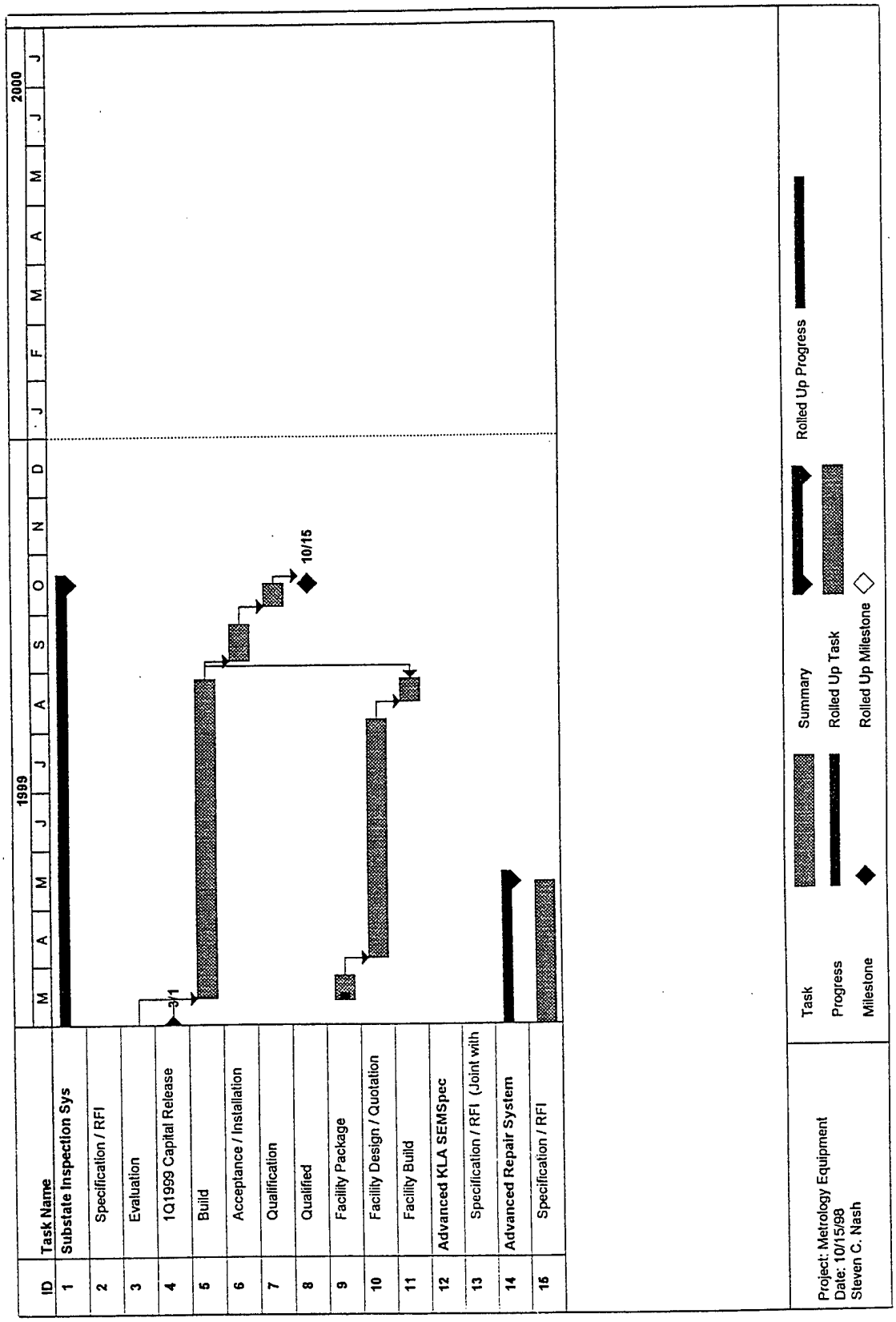


Figure 6 (Part 3 of 5). Metrology, Inspection and Repair Equipment Schedule

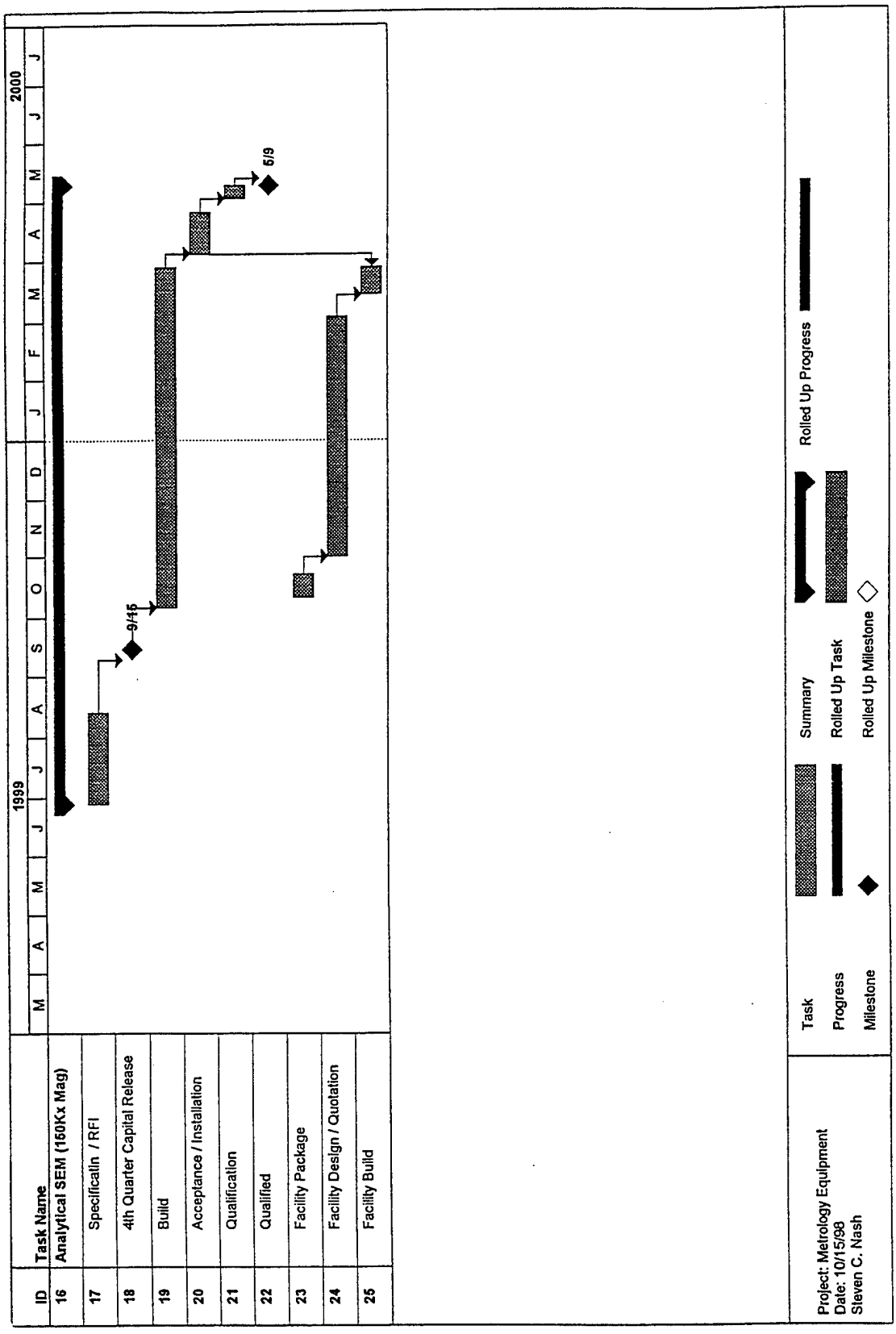


Figure 6 (Part 4 of 5). Metrology, Inspection and Repair Equipment Schedule

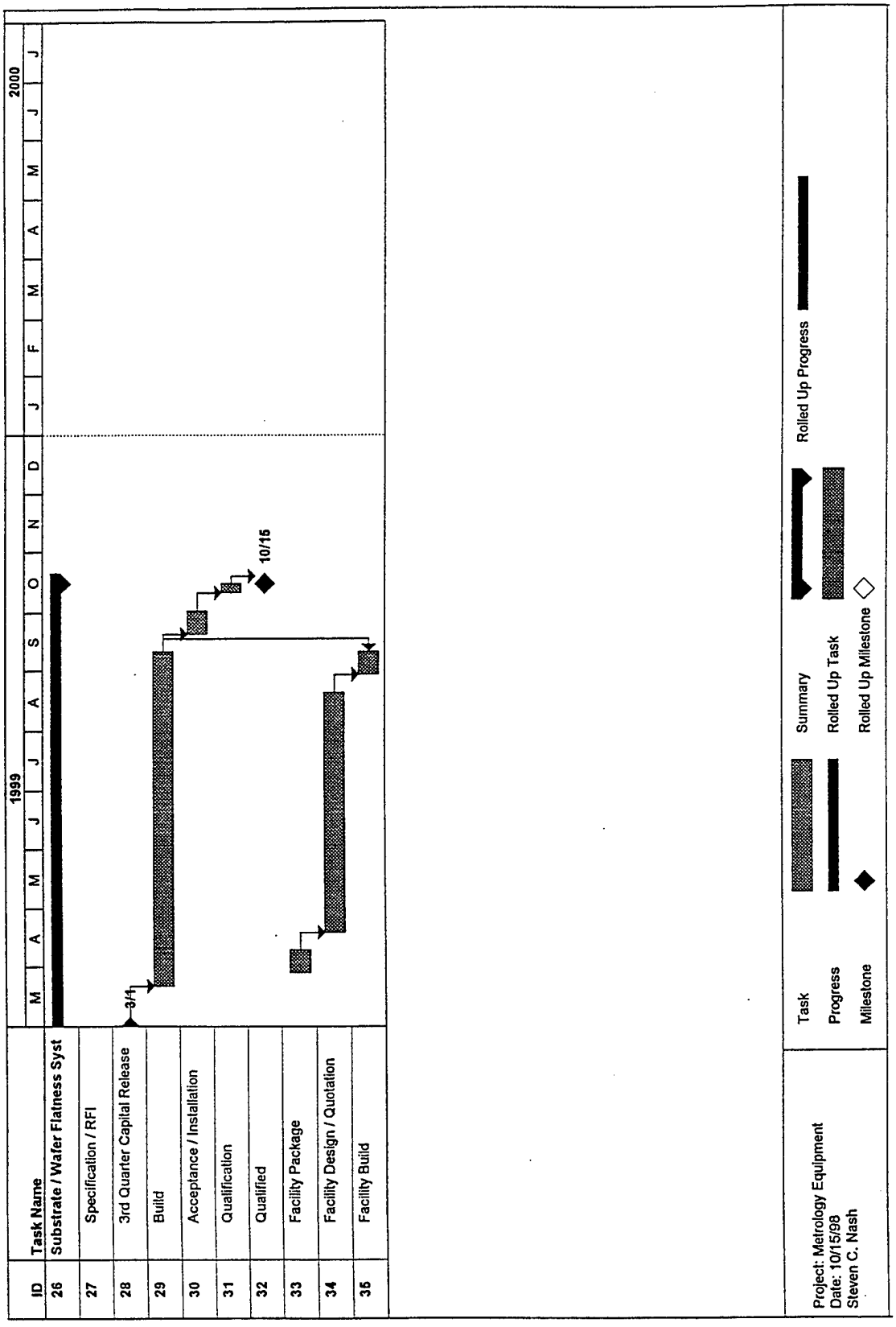


Figure 6 (Part 5 of 5). Metrology, Inspection and Repair Equipment Schedule

4.0 Develop Sub-0.18μm Mask Fabrication Capability (Task 3)

4.1 Sub-0.18μm Defect Reduction/Validated Mask Fabrication (Task 3.2)

Task Objective: Establish and maintain a pilot production facility capable of on-premises x-ray mask production, and demonstrate 0.18μm mask fabrication capability by fabricating masks of increasing complexity.

4.1.1 Line Status

The focus during the first quarter was the upgrade of EL-4+ P0 to smaller fields and subfields. No exposures were made between 08 December 1997 and 17 January 1998, and subsequently no product exposures were made until 26 January. The MMD film deposition system was also qualified during this period. In addition, no exposures were made between 25 April and 16 May during an upgrade to the EL-4+ P0 laser. (Also see Section 2.2.1.)

EL-4+ P0 has been available since 16 May averaging 30 mask starts per week, approximately half SiC and half B:Si. B:Si was used mainly for EWRs and PSE creation, while the majority of product mask starts used SiC. Two capacity exercises were attempted in 1998. A two-week preliminary capacity study was completed on 11 June which assessed the MMD's manufacturing capability. Seventy masks were started with an average BEOL turnaround time of 1.5 days; 18 were shipped to various customers, including IBM, Sanders and the University of Wisconsin. This preliminary study was done in preparation for a three-month demonstration to complete 50 mask shipments to customer specifications. This demonstration was started on 24 August. It was suspended after 11 weeks because of vibrations and electrical noise caused by nearby construction, and a process shift caused by a change to the SiON etch system. Three hundred and thirteen exposures were completed and 37 masks were delivered to customer specifications. Ninety-five percent availability of EL-4+P0 was achieved.

Several process enhancements were completed during 1998. An automated bake/develop tool from SSI was installed and qualified. DOEs were completed for the UVIII etch process and the UVN2 negative resist process. A multiple pass exposure process was introduced that demonstrated 20nm image placement with no significant degradation of image size or defect performance. In addition to the new deposition systems, a new annealing tool and a new stress measurement tool were installed and qualified in the FEOL.

In 1Q98, etch processes were defined for etching Falcon (UVIII) and Nighteagle (SNR200) line monitors. The descum, hard mask etch and resist strip are common to both patterns, but the TaSi absorber etch is at a higher *RF* bias power for etching the

higher line-to-space aspect ratio trenches on Falcon masks. The higher *RF* bias is needed to completely clear the trenches.

During 2Q98, gas lines and flow controllers were added to the AM42 etch tool (a Plasmatherm 770 SLR reactive ion etch system used primarily for resist strip) to allow it to function as a descum and/or hard mask etch tool. A more anisotropic descum process was defined on this tool to reduce etch bias, and is used as the process-of-record. A polymer cover over the ceramic wafer clamp was added to AM42 to allow it to function as a backup hard mask etch tool. The Falcon masks confirm that this tool can be used as a backup hard mask etch tool.

In 4Q98, work concentrated on understanding the impact of process parameters on Falcon image size uniformity (see Task 8 summary).

4.1.2 4Q98 Equipment Engineering Changes and Facilities Activities

Engineering changes completed during the first three quarters of 1998 are listed in the respective quarterly status reports.

Suss Resist Coat Tool:

New software and hardware were installed for robot interlock.

RTA Oven:

The new Eaton Summit RTA Oven has been installed. The Eaton 850 was re-installed near the new RTA oven for interim process support.

Ultrafab Fountain Etch Tool:

This new tool has arrived and is in process of being installed.

SMIF Activity:

The SMIF Clean tool was modified for improved pod cleaning. Additional pods have been reconditioned for improved FM control.

Plasmatherm Activity:

A fixture for a sensor, an aluminum disk for parts, and several ardel covers for the ceramic disk were designed, built, and installed.

Other Tool Activity:

EL-3+ #6 has been de-commissioned. A new membrane etch fixture was designed and built for improved etch process reliability and ability to etch 25% more product.

New stainless steel bellows were installed on bonding fixtures. A new nitrogen purge box was installed in the carbon-filter room. New stainless steel shelving was installed in the process line.

4.1.3 University of Wisconsin Modeling Verification

Monthly Sematech teleconferences are held with the University of Wisconsin to monitor their mask modeling work. Work in 2Q98 focused on modeling image placement distortions due to radiation damage. The modeling work predicts that irradiation of a small part of the Nighteagle pattern area gives rise to distortions up to approximately 11nm in the X and Y directions. These distortions can be reduced somewhat by magnification correction. If the entire pattern area is irradiated, the distortions are lower: 2.55nm in the X and 2.98nm in the Y direction.

Current work at the University of Wisconsin is focused on updating the mask substrate fabrication model by including the effects of different wafer topographic shapes or warpage, and a more accurate representation of the bonding process. Parametric studies are also being performed to understand the effect of different film stresses and thicknesses, different membrane materials, different wafer shapes, as well as order of process flow. The image placement distortion of both Nighteagle and Falcon patterns will be used in this study, and any pattern-dependent issues will also be identified.

A Mask Modeling Workshop Technical Interchange Meeting (TIM) was held on 13 July 1998 at the University of Wisconsin to review current x-ray mask modeling work being performed at the University of Wisconsin and to coordinate future x-ray mask modeling-related projects. The meeting was documented in CDRL H002, 98-MMD-LMFS-00048 (also see Section 7.0 of this report).

4.1.4 Defect Reduction

4.1.4.1 Defect Density Focus/Defect-Free Mask Status

The MMD has continued to make progress in reducing both the overall defect density and the number of non-repairable defects on a mask. Figure 7 on page 37 shows the defect density versus the 1998 learning plan. The overall average defect density has been reduced from greater than 100 defects/cm^2 to 5.0 defects/cm^2 in November, bringing the total number of repairs well within the defect repair window. The average number of non-repairable defects on a mask has dropped to 13.1 defects/cm^2, but the best mask demonstrated each month has dropped from 14 non-repairable defects in February to no non-repairable defects in November. In September a Falcon mask was repaired down to only one defect (in 5cm^2), and one was reduced to defect-free in November. The progress in reducing the number of non-repairable defects versus the 1998 learning plan is shown in Figure 8 on page 37. In June there were five primary types of non-repairable defects (clears, mesa, TaSi, e-beam data and SiC 'blobs') as shown in Figure 9 on page 38. The primary defect

sources have been identified and progress continues to be made in minimizing the defects. Figure 10 on page 39 shows the November distribution of non-repairable defects.

The source of the clear defects was determined to be the substrate quality. Figure 11 on page 40 shows one underlying cause of a clear defect, which was damage to the hard masks. The implementation of the sacrificial layer (discussed in Section 4.1.4.7) has reduced clear defects to an average of one per mask.

Another defect type, mesa, is shown in Figure 12 on page 42. By inspecting a mask through the process flow, the source of this defect has been identified as foreign material acting as a micromask during either the SiON hard mask etch or TaSi etch. It has also been demonstrated that foreign material on the resist during e-beam write blocks the resist exposure causing the resist to act as an etch mask. Based on clean room evaluations (see Table 6), the carbon filter room was found to contribute a high number of adders. During the bake process the mask is exposed to room conditions for 5-10 minutes. A mini-environment was built to protect the mask from contaminants while cooling.

Table 6. Clean Room Evaluation

AREA	Adder (1 hour exposure time)
Descum	4 adders (0 larger than 1μm)
TaSi Etch	4 adders (0 larger than 1μm)
SiON Etch	5 adders (0 larger than 1μm)
Carbon Room - Blanket Expose / Hot Plate	108 adders (51 larger than 1μm)
Carbon Room - Yes Oven / SMIF Pod Handler	23 adders (17 larger than 1μm)
Carbon Room - APT / Hot Plate	37 adders (12 larger than 1μm)
EL-4+ P0 Loading Area	-1 adder
EL-4+ P0 Chamber Loading Station	0 adders
Carbon Room - SSI Tool	1 adder
Carbon Room - Scope	0 adders
Carbon Room - Suss Coater	3 adders (2 larger than 1 micron)
Leica Room Tool	1 adder
Leica Room - SMIF Pod	7 adders (3 larger than 1 micron)

The e-beam data defect (Figure 13 on page 44) was caused by a data path error in the e-beam system. The defect was eliminated by replacing a faulty array disk drive that was causing a timing error.

At the start of the year every SiC mask had at least one SiC deposition defect (called 'blobs') as shown in Figure 9 on page 38. Hoya has changed their process and has minimized this defect.

The partitioning of TaSi defects is shown in Figure 14 on page 45 and discussed in Section 6.4.

4.1.4.2 Point-of-Use Defect-Free Mask Project

A project has been established in conjunction with the Advanced Lithography Facility (ALF) at IBM East Fishkill to demonstrate point-of-use defect-free mask prints (no repeating defects on a mask verification print). The plans are shown in Figure 15 on page 46. Five masks have been sent to ALF to expose verification prints to benchmark the current capability.

4.1.4.3 Final Mask Clean

During 1998 the MMD evaluated a new chemical clean system. A statement of work for a wafer cleaning system was sent to Verteq, Steag, CFM and SemiTool. The Verteq VcS system was selected. The Verteq system demonstrated cleaning efficiency for silicon nitride (Si_3N_4) contamination, for SiON, TaSi, Cr and Si. The results are shown in Table 7 on page 27. The system also demonstrated cleaning x-ray mask substrates without breaking the membrane. This was very encouraging; it will allow for a single system to clean both wafers (incoming wafer clean, SiC wafer clean, Post Cr, TaSi and SiON deposition wafer clean, and post back side lithography clean) and x-ray mask substrates (post membrane etch and post bonding clean). Funding for this project is planned for 1999 (see Figure 16 on page 50).

4.1.4.4 Mask Transfer Tool

As noted above, the Verteq tool will be adapted to perform final mask clean, eliminating the need to purchase an additional final mask clean system. A SMIF pod shuffle tool capable of removing masks from a single-mask SMIF pod and buffering them into a multiple-mask SMIF pod is planned to support this. Zygo was selected for this project (see Section 3.2.4) which is planned for 1999.

4.1.4.5 Backside Lithography System

A new backside lithography system was ordered in August from Karl Suss to replace the Perkin Elmer 600 currently in use. The Perkin Elmer 600 system leaves chuck marks on the front surface of the x-ray masks. The updated project plans are shown in Figure 15 on page 46.

4.1.4.6 Mini-Environments

Mini-environments are planned for some of the MMD's critical, manually loaded tools. The tools under consideration are listed in Table 8 on page 29. A statement-of-work was sent to Infab, Huntair and ASYST and cost proposals from these vendors are currently being reviewed. The project plans are shown in Figure 15 on page 46.

Table 7 (Page 1 of 2). Verteq VcS System Evaluation. Si_3N_4 Contamination Clean 4" Wafer Demo, 2/3/98.

Substrate Type	Surface Condition	Slot # IBM	Slot # ERTE	Scan Threshold	Pre-scan	LPD Count Using Pre-clean	Tencor 6400 Contamination	Post-Clean	Clean Eff (%)
Si - Out of Box	Hydrophilic	9	9	0.125μm	6393	62(Vc1234)	2877	117(Vc1234)	98.08
Si - Out of Box	Hydrophilic	10	10	0.125μm	4946	22(Vc1234)	2752	31(Vc1234)	99.67
Si - Out of Box	Hydrophilic	11	11	0.125μm	6568	18(Vc1234)	2801	86(Vc1234)	97.56
Si - Out of Box	Hydrophilic	12	12	0.125μm	7681	21(Vc1234)	2681	47(Vc1234)	99.02
Si - Out of Box	Hydrophilic	13	13	0.125μm	17600	25(Vc1234)	2522	100(Vc1234)	96.64
Si - Out of Box	Hydrophilic	14	14	0.125μm	5857	8(Vc1234)	2664	127(Vc1234)	96.52
Average STDEV					**8174.17 4703.87**	**26.00 18.58**	**2714 124.15**	**86.0 39.13**	**97.75 1.53**
Si - Out of Box	Hydrophilic	1	1	0.125μm	1013	13(Vc141)	2682	8(Vc1)	100.19
Si - Out of Box	Hydrophilic	2	2	0.125μm	4093	5(Vc141)	2373	7(Vc1)	99.92
Si - Out of Box	Hydrophilic	3	3	0.125μm	17962	1(Vc141)	2088	33(Vc1)	98.47
Si - Out of Box	Hydrophilic	4	4	0.125μm	7228	3(Vc141)	1855	24(Vc1)	98.47
Si - Out of Box	Hydrophilic	5	5	0.125μm	10153	4(Vc141)	1684	5(Vc1)	99.94
Si - Out of Box	Hydrophilic	6	6	0.125μm	9793	2(Vc141)	1800	8(Vc1)	99.67
Si - Out of Box	Hydrophilic	7	7	0.125μm	11470	1(Vc141)	1634	4(Vc1)	99.82
Si - Out of Box	Hydrophilic	8	8	0.125μm	9798	1(Vc141)	1603	8(Vc1)	99.56
Si - Out of Box	Hydrophilic	9	9	0.125μm	20890	7(Vc141)	1496	7(Vc1)	100.00
Si - Out of Box	Hydrophilic	10	10	0.125μm	8849	4(Vc141)	1633	4(Vc1)	100.00
Si - Out of Box	Hydrophilic	11	11	0.125μm	9679	5(Vc141)	1966	12(Vc1)	99.64
Si - Out of Box	Hydrophilic	12	12	0.125μm	8496	7(Vc141)	2332 :c62(Vc1)	100.04	
Average STDEV					**9952.00 5319.42**	**4.42 3.45**	**1928.83 369.74**	**10.50 8.89**	**99.68 0.51**
SiON	Hydrophilic	22	22	0.25μm	493	493(Vc1)	1092	494(Vc1)	99.83
SiON	Hydrophilic	23	23	0.25μm	2666	257(Vc1)	848	254(Vc1)	100.51
SiON	Hydrophilic	24	24	0.25μm	182	178(Vc1)	966	182(Vc1)	99.49

Table 7 (Page 2 of 2). Verteq VcS System Evaluation. Si_3N_4 Contamination Clean 4″ Wafer Demo, 2/3/98.

Substrate Type	Surface Condition	Slot # IBM	Slot # ERTE	Scan Threshold	Pre-scan	LPD Count Using Pre-clean	Tencor 6400 Contamination	Post-Clean	Clean Eff (%)
SiON	Hydrophilic	25	25	0.25μm	286	271(Vc1)	1158	280(Vc1)	98.99
Average					**306.75**	**299.75**	**1016.00**	**302.50**	**99.70**
STDEV					**132.09**	**135.18**	**137.43**	**134.23**	**0.64**
TaSi	Hydrophilic	1	10	0.25μm	758	383(Vc1)	1838	369(Vc1)	100.96
TaSi	Hydrophilic	2	2	0.25μm	579	315(Vc1)	2091	309(Vc1)	100.34
TaSi	Hydrophilic	3	3	0.25μm	720	402(Vc1)	1621	395(Vc1)	100.57
TaSi	Hydrophilic	4	4	0.25μm	471	271(Vc1)	1507	298(Vc1)	97.82
TaSi	Hydrophilic	5	5	0.25μm	426	172(Vc1)	1591	172(Vc1)	100.00
TaSi	Hydrophilic	6	6	0.25μm	652	329(Vc141)	1163	328(Vc1)	100.12
Average					**567.25**	**293.50**	**1470.50**	**298.35**	**99.63**
STDEV					**141.10**	**97.13**	**210.60**	**93.435**	**1.23**
Cr	Hydrophilic	11	15	0.25μm	828	320(Vc1)	5128	318(Vc1)	100.04
Cr	Hydrophilic	12	12	0.25μm	669	749(Vc1)	8725	488(Vc1)	103.27
Cr	Hydrophilic	13	13	0.25μm	535	401(Vc1)	9089	451(Vc1)	99.42
Cr	Hydrophilic	14	14	0.25μm	1026	769(Vc1)	18031	465(Vc1)	101.76
Cr	Hydrophilic	15	15	0.25μm	558	544(Vc141)	11468	446(Vc1)	100.90
Cr	Hydrophilic	16	16	0.25μm	2662	1175(Vc1)	10957	1179(Vc1)	99.96
Average					**1195.25**	**722.25**	**12386.25**	**635.25**	**10051**
STDEV					**1003.66**	**337.71**	**3899.62**	**362.59**	**1.03**

Table 8. Proposed Mini-Environment Tools split=yes		
Plasmatherm SLR Series SiON Deposition	Model- SRL-730 Mn Frame 56G4786AA AM99	Class 1 Mini-environment SMIF Pod opener (have) wafer vacuum wand
Plasmatherm SLR Series TaSi Etch System	Model- ECR Main Frame 56G427AA AM50	Class 1 Mini-environment SMIF Pod opener X-Ray mask vacuum wand
Plasmatherm SLR Series Resist Descum/Resist Strip	Model- 770 56G4083AA AM42	Class 1 Mini-environment SMIF Pod opener X-Ray mask vacuum wand
Plasmatherm System VII Shuttlelock SiON etch	Model- SSL-720 20F78170-AA AM36	Class 1 Mini-environment SMIF Pod opener X-Ray mask vacuum wand
Polyvar MET Microscope Resist Develop check		Class 1 Mini-environment SMIF Pod opener Wafer and X-ray mask vacuum wand
Cost Effective Equipment Resist Bake	92H7905aa and ab (Both hot plates and a chill plate can be placed in the same mini -environment	Class 1 Mini-environment SMIF Pod opener X-ray mask vacuum wand
Tencor P-1 Long Scan Profiler Film Thickness	Model- P-1 20FG994 AM02	Class 1 Mini-environment SMIF Pod opener X-ray mask vacuum wand
Leica LMS 2020 Image Placement Metrology	Model- LMSA 2020 79X6911-AF M966	Class 1 Mini-environment SMIF Pod opener (have) X-ray mask vacuum wand SMIF Pod storage for parts in tool (10x)
Polyvar MET Microscope Process Line		Class 1 Mini-environment SMIF Pod opener Wafer and X-ray mask vacuum wand
Tencor 6420 Defect inspection	Model- Surfscan 6420 (289108) 56G4724-AA AM52	Class 1 Mini-environment SMIF Pod opener (have) Cassette Gripper
Applied Material Precision 5000 SiC Trench etch - Back Side Litho	Model- Precision 5000 79X6731 AL AM17	Class 1 Mini-environment SMIF Pod opener (have) Cassette Gripper

4.1.4.7 Sacrificial Layer Process Change

An alternative process flow with an SiON sacrificial layer (Table 9 on page 30) was evaluated as a possible means of reducing damage to the front surface of the x-ray mask during backside lithography. SiC wafers with 0.5μm and 1.0μm of sacrificial SiON were processed with the alternative process flow and compared to wafers processed without the sacrificial layer (see Table 10 on page 30). The results showed that a 1.0μm thick SiON sacrificial layer reduced the backside lithography defect adders by 20×. These wafers were then processed into final masks to determine if the reduction in the backside lithography defect adders resulted in a reduced number of clear defects in the final masks. Final mask inspection data to date has shown that the number of clear defects has dropped from 42% of the final mask defect total to just

6% of the total. Based on these results, the alternative process flow with 1.0μm of sacrificial SiON was implemented on all MMD production lots released after 22 July 1998.

Table 9. Alternative Process Flow	
Current Process	**Alternative Process**
SiC Deposition	SiC Deposition
Metal Stack Deposition	Sacrificial Layer Deposition
Backside Lithography	Backside Lithography
Membrane Etch	Metal Stack Deposition
Bond	Membrane Etch
	Bond

Table 10. Process Comparison	
Sacrificial Layer Thickness	**Increase in Defects after Backside Lithography**
0μm (Control)	200%
0.5μm	90%
1.0μm	10%

4.1.5 Etch Chemistry/Tooling (Fountain Etch Station)

MMD personnel visited UltraFab in San Jose, CA on 22 and 23 July as a follow up on the open issues from the 13 May acceptance test of the fountain etch station. Open issues from the first visit were satisfactorily corrected and only minor issues remained. These issues were resolved to the satisfaction of MMD and the fountain etch tool was granted acceptance for delivery on 26 August. The tool was delivered to the MMD on 22 September and the tool installation is delayed due to supplier bankruptcy.

4.1.6 UV (Ultraviolet) Adhesive Bonding

An ultraviolet (UV) adhesive is being investigated as a replacement for the current anodic bonding process, which attaches the Si wafers to the Pyrex rings. The UV adhesive:

- Reduces mask contamination and damage by significantly decreasing front surface contact during the bonding process.
- Enables extensive process automation.
- Improves mask flatness by eliminating the affects of the thermal expansion mismatch between the Si wafer and the Pyrex ring.
- Reduces the cycle time of the bonding operation.

- Allows for the rework/recovery of the Pyrex rings.

UV adhesives from Norland, Loctite and Dymax were compared (Table 11) and, based on its excellent chemical resistance and low outgassing properties, the Norland adhesive was chosen for evaluation.

Table 11. UV Adhesive Vendor Comparison

	Norland Products	Loctite	Dymax
Chemical Resistance	Excellent	Good	Good
Substrate Compatibility	Excellent	Excellent	Good
Outgassing	< 0.01% CVCM*	< 0.1% CVCM*	< 0.1% CVCM*
Temperature Range	-50 to 175°C	-50 to 150°C	-40 to 150°C
Tensile Strength	1900 psi	4500 psi	3000 psi
Cure Time	2 minutes	30 seconds	30 seconds

* CVCM - Collected Volatile Condensable Material (CVCM)

The compatibility of Norland adhesive with the actual manufacturing BEOL processes was evaluated by repeated exposure to individual process steps (wet chemical cleaning, wet/dry etching and resist develop) and also by processing multiple substrates through the entire BEOL process (e-beam write, resist bake and inspection tooling, in addition to the wet chemical processes discussed above). From the experimental matrix that was run, it has been determined that the Norland adhesive is compatible with all MMD BEOL tooling and processes, and there was no visible or mechanical degradation of the Si-Pyrex bond integrity of the final mask when compared to a "just-bonded" mask, although image placement is still being evaluated.

Based on the data collected to date, it was determined that the use of the Norland UV adhesive as a replacement for the anodic bonding process is feasible. Further UV adhesive process development is required to achieve control of the post bond mask flatness and to reduce the required curing time.

4.1.7 Bond Before Membrane Etch

Prototypes of a new design of compact etch holders capable of holding a bonded wafer during the membrane etch process were built. The membranes are currently etched into the wafers and the wafers are then bonded to the Pyrex rings. An evaluation is underway to determine if the flatness of the wafer and the membrane area is improved by bonding the wafers before membrane etch.

4.2 Develop Sub-0.18μm Production Mask Fabrication Capability (Task 3.3)

4.2.1 Multiple Pass Write Evaluation

A process has been established for multiple pass write with UVIII resist. Exceptional image placement results have been achieved using this process: best to date on a membrane was 20nm and best to date on a bonded wafer was 19nm. Image size and defect density results are similar to those of single-pass write. Several products have been fabricated using multiple pass write including Falcon, Power PC and DRAM development masks.

A process for UVN2 with multiple pass write has also been defined. Image placement results for UVN2 resist with single pass write are typically in the 30nm range. The multiple pass repeatability is about 3nm better than that of masks written using single pass write. Synthetic PSE indicates a 2nm improvement in final image placement will be achieved with multiple pass write relative to single pass write. No degradation in image size and defect density was observed with multiple pass write. Therefore, multiple pass write has been implemented for UVN2. The actual improvement with multiple pass write on product is being assessed.

Further details on the process and results for UVIII and UVN2 resists is given in CDRL G004, Multi-pass Writing on Chemically Amplified Resists, 98-MMD-LMFS-00085.

4.2.2 SNR 200 Resist Status

SNR resist is being phased out and replaced with UVN2 resist for several reasons. The supplier, Shipley, plans to discontinue the manufacture of SNR resist. Also, the post-expose bake (PEB) temperature latitude, image placement repeatability, image quality and coat uniformity of UVN2 are superior to those of SNR.

4.2.3 Thin Resist

Thin UVIII resist (300nm versus 400nm) has been used to manufacture an ALF testsite mask and 75nm resolution has been achieved. Thin resist will be used as necessary for the fabrication of high resolution masks.

4.2.4 UVN2 Resist

The UVN2 resist process has been established and optimized using a statistical design of experiments (DOE) matrix. Several Nighteagle masks have been processed using UVN2 resist with the optimized process. Excellent post-exposure bake (PEB) latitude, material repeatability, resolution, image size and image placement results have been achieved, demonstrating that the resist is qualified for the fabrication of x-ray masks.

The write-to-PEB delay stability and thinning of UVN2 are acceptable but not as good as those of UVIII and SNR resists. The resist supplier, Shipley, believes the mechanism for the delay stability and thinning is humidity absorbed by the resist (crosslinker) which decreases the amount of crosslinking. A dry box (N_2 purge) has been implemented to improve the PEB delay stability. In addition, UVN30, a new formulation of UVN2, will be evaluated in the first quarter of 1999. UVN30 crosslink is less susceptible to humidity and is, therefore, more stable.

The UVN2 evaluation is documented in CDRL G004, Technology Assessment Report, 98-MMD-LMFS-00066. The UVN2 etch process was implemented on all product requiring negative resist, with no process variation.

4.2.5 Image Size Characterization

Falcon and Nighteagle image size data obtained this year on SiC substrates continue to have 3σs ranging from 8nm to 36nm. The image size 3σ results for Nighteagle (SNR) are typically in the teens, while the Falcon 3σs have ranged from the low teens to 36nm. The data for several Falcon masks has been plotted and the variation in image size is dominated by a severe edge character. The images at the edge of the membrane are significantly smaller than those at the center of the masks. The character is different than the typical bow character because the edges drop off sharply rather than gradually with the bow. The Nighteagle masks have the bow and some edge effect, but do not have the severe edge effect seen on Falcon masks.

Analysis of image size data taken over several months indicated higher 3σ on B-Si masks compared to the SiC masks. The edge effect was more severe for B-Si parts and was the major contributor to the high image size variation. The edge effect for SiC masks has been more severe, however, in the fourth quarter.

The lithography team designed several experiments to determine and eliminate the image size error components. Better 3σs have been observed for Falcon patterns written on bonded wafers and larger membranes than on Falcon membranes, indicating the edge effect is a membrane edge effect. The edge effect is not seen in the resist image size measurements but is seen after SiON etch.

Several etch experiments for pre-etch descum, SiON etch and TaSi etch have been completed in an effort to optimize the process for better image size uniformity, e.g., varying the backside helium pressure, varying the cathode temperature and using different etch tools. However, none of the processes investigated improved the edge effect and CD uniformity.

Recent results for single-pass write masks with e-beam blockout are better than multiple pass write masks with UV blockout. Additional masks are being written to confirm this result. Results from masks recently processed on the APT tool are better than the results from parts processed on the SSI tool. Now that the new SSI centering device is on-line, more masks will be written to determine if this caused the APT masks to have better results.

Falcon patterns written straddling the membrane edge demonstrated that the image size variation is due only to membrane edge effects and not to pattern edge effects. Pattern edge effects can be caused by e-beam proximity effects or edge microloading. Membrane edge effects are likely due to differences in stress caused by heating during resist processing or etch.

In November, a split lot experiment was completed to compare the two SiON etch tools, AM42 versus AM36. The results of this experiment suggested a problem with the AM36 hard mask etch tool since the results for 3σ were worse for this tool than for the AM42. Thermal modeling suggested an overall reduction in wafer cooling. The etch rate uniformity as measured on resist-coated bonded wafers was also significantly worse for AM36 than for AM42. An investigation was completed and revealed that the feature plate was misaligned and Falcon mask results confirmed that the 3σs have returned to the 2Q98 values. However, the mean shifted as a result of this change and the process is being optimized to bring the mean back within specification.

The new experiments listed below are underway to identify and correct the 3σ.

- Hardbake the resist after develop to improve the etch resistance of the UVIII resist. This experiment had no effect on the CD uniformity.
- Evaluations of hardbake were completed and showed no effect.
- Repeat the SSI versus APT experiment. This will be completed when the image size mean is within specification.
- Run a focus (e-beam) versus image size study.
- Process a Falcon mask using ZEP non-chemically amplified resist.
- Process Falcon with new bake pedestal with border that is in closer proximity to the membrane during bake to compensate for the edge effect.
- Run a Falcon membrane with dose wedges written all over the membrane to determine the variation across the membrane.
- Run a Falcon on a membrane without the SiON hard mask and with thin TaSi (300nm instead of 500nm). This process did not improve the image size 3σ.
- Run a pattern with a dose boost on the edges of the pattern to compensate for the edge effect.

- Try a lower temperature bake for a longer time for the PEB. A mask was processed at 130°C for 13 minutes (the process-of-record is 143°C for two minutes) but the image size was very small and several measurements were missed on the SEM. This experiment needs to be repeated when the mean is back within specification.

When the mean is back within specification the lithography team will revisit the following experiments: multiple pass versus single pass, APT versus SSI, and blockout versus no blockout. The team will also discuss additional experiments to be completed to further improve image size uniformity.

4.2.6 Status of EL-4+ P0

The EL-4+ P0 system underwent extensive modifications during the end of 1997 and into 1Q98. The system full spot size was changed from 2×2μm to 1×1μm. This change reduced the current at the target from 1.200ma to 0.300ma of current, which had a negative impact to tool throughput. To increase throughput, the beam current density was increased from 30 amps/cm^2 to 60 amps/cm^2, yielding 0.600ma of current at the target. The field and subfield sizes were also reduced. The subfields were shrunk from 37.5×37.5μm to 18.75×18.75μm, while the field size was reduced from 2.1×2.1μm to 1.05×1.05μm. This change reduced the size of the beam deflections, thereby reducing the system noise, allowing better placement. The range of the dynamic corrections was also reduced to decrease the systems sensitivity to noise. These improvements reduced the noise level at the system by 25%. In addition, an attempt was made to reduce noise contributions from the system's servo activity. The alignment 5 driver was replaced with a lower power card to reduce noise by reducing the least significant bit (LSB) weight-to-position ratio.

The λ/1024 laser and beam feedback system were upgraded during the second quarter. Further noise damping was also added to the Dynamic Corrections system. The electron gun and top hat assembly were also replaced at this time. The new assembly had a fully populated filament ball to allow operation into 1999. Several components of the column were changed to reduce charging that had been previously measured. Initial results after bringing the system back on line showed improvements in all charging tests.

During 3Q and 4Q98, the EL-4+ P0 system was at full functionality with only minor downtime. The system typically has been running 30 to 35 mask/wafer starts per week. The work done in the first half of the year yielded placement consistently below 30nm, with some parts yielding at below 20nm, as noted in 2.2.3. Image size stability (3σ) has also been consistent when measured in resist, typically below 20nm and often below 10nm.

Mask exposure starts at the EL-4+ P0 system have been maintained at four to five parts per day since 24 August, with the system typically running 24 hours per day, seven days per week. A monitor substrate for image placement has been resumed

using the Falcon pattern (180nm images) on ring bonded wafers. Placement at the system has been stable, running below 30nm (Figure 18 on page 55).

The best placement to date on a ring bonded wafer is (19nm,17nm) 3σ (X,Y), as shown in Figure 19 on page 55. Placement on product membranes has been following the trends of the tool monitors with repeatable placement within a product family. The best placement to date on a membrane has been on a Falcon product which measured (18nm,20nm) 3σ (X,Y). (See Figure 20 on page 56.)

The Raid array that was malfunctioning and causing a non-repairable defect, as reported in the 3Q98 Progress Report, has been fixed. All nine disks in the array were replaced and the system was fully tested. The e-beam patterning defect has not recurred.

The EL-4+ P0 system is undergoing extensive testing for its contributions, if any, to foreign material defects. Previous tests have shown that the tool is not a significant source of contamination. Procedures were changed to enhance the clean room practices, such as wearing extra gloves during manual handling of parts before and after exposure, as an added precaution.

Work on EL-4+ P0 computer upgrades continues. The third Programmable Work Station (PWS) has been completed and released to the manufacturing operators; this work station will be placed in the MMD cleanroom. This is the first PWS to run OS/2 Warp 4 as an operating system. The server system is being upgraded to a Pentium machine, also running OS/2 Warp 4; PWS1 and PWS2 will subsequently be upgraded.

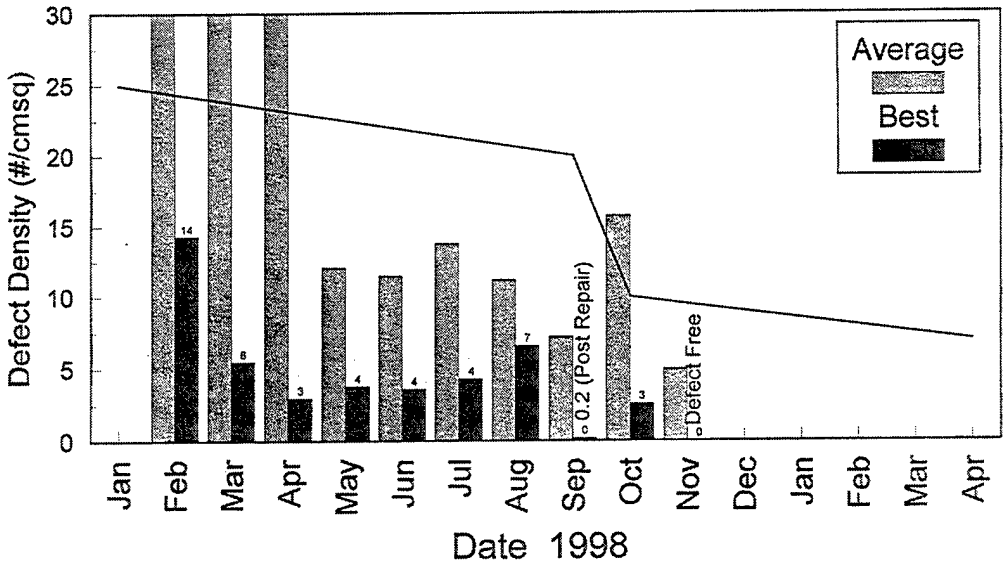


Figure 7. Defect Learning Targets (1998). 5.3cm² inspection area - 256k SRAM.

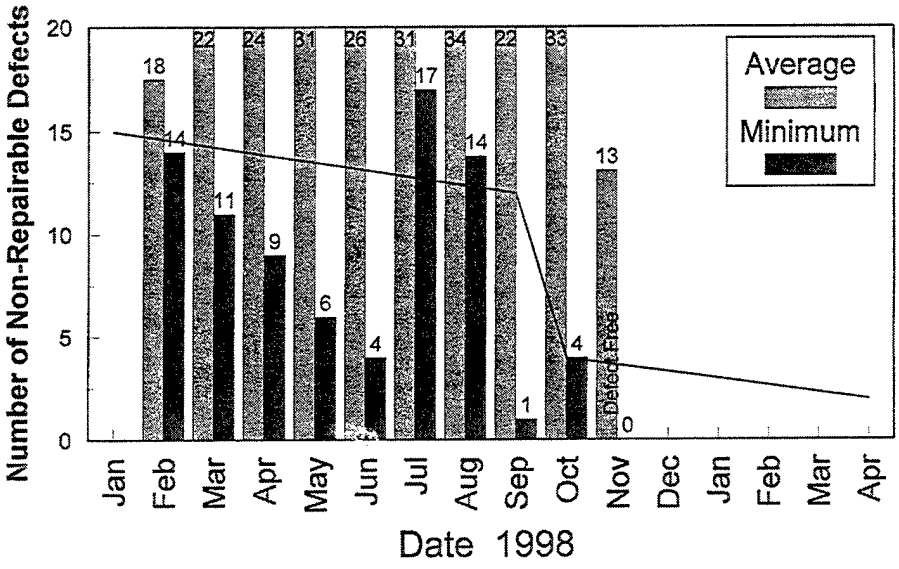


Figure 8. Non-Repairable Defect Learning Goals (1998)

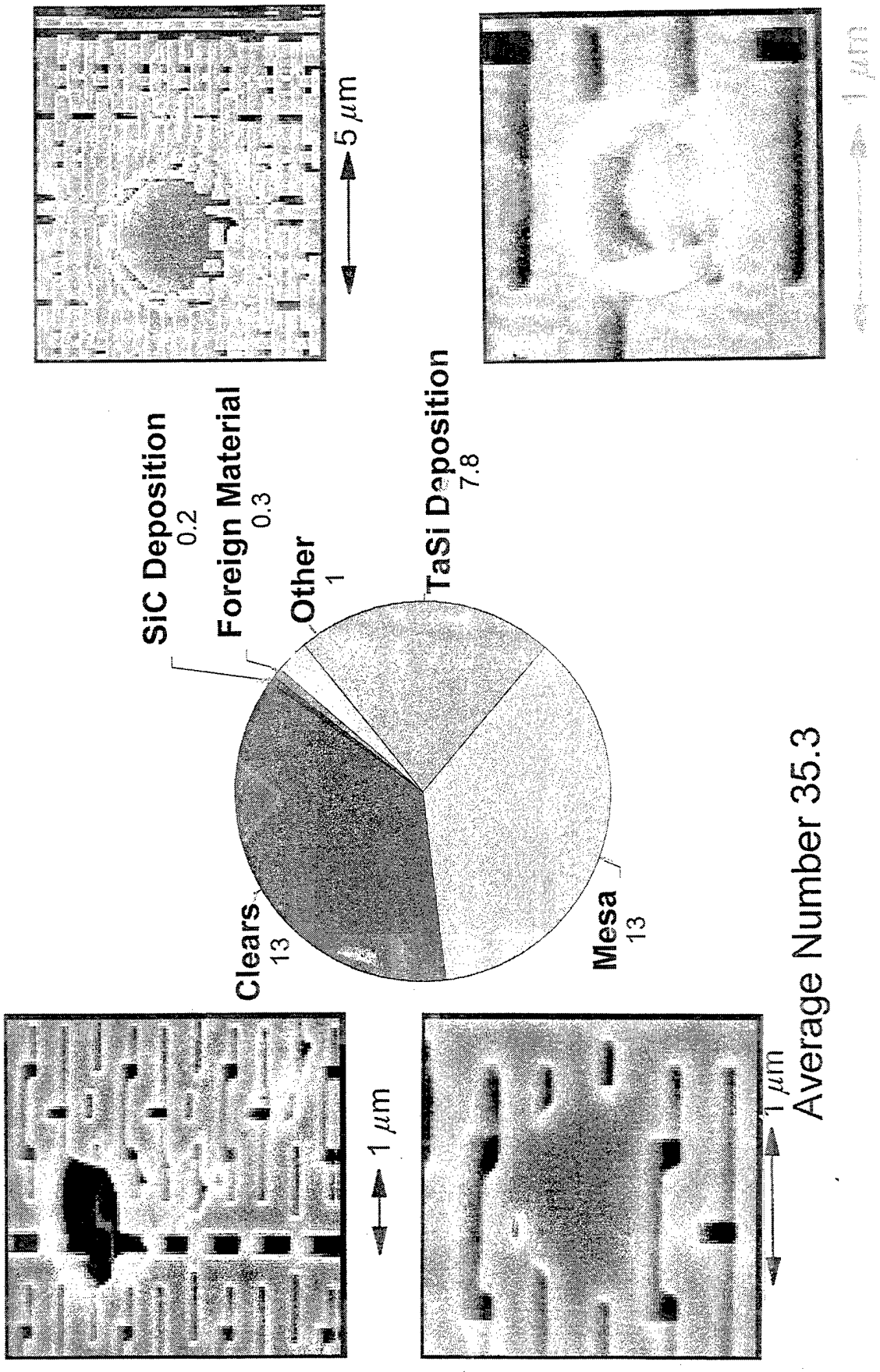


Figure 9. Non-Repairable Defect Types (March, 1998)

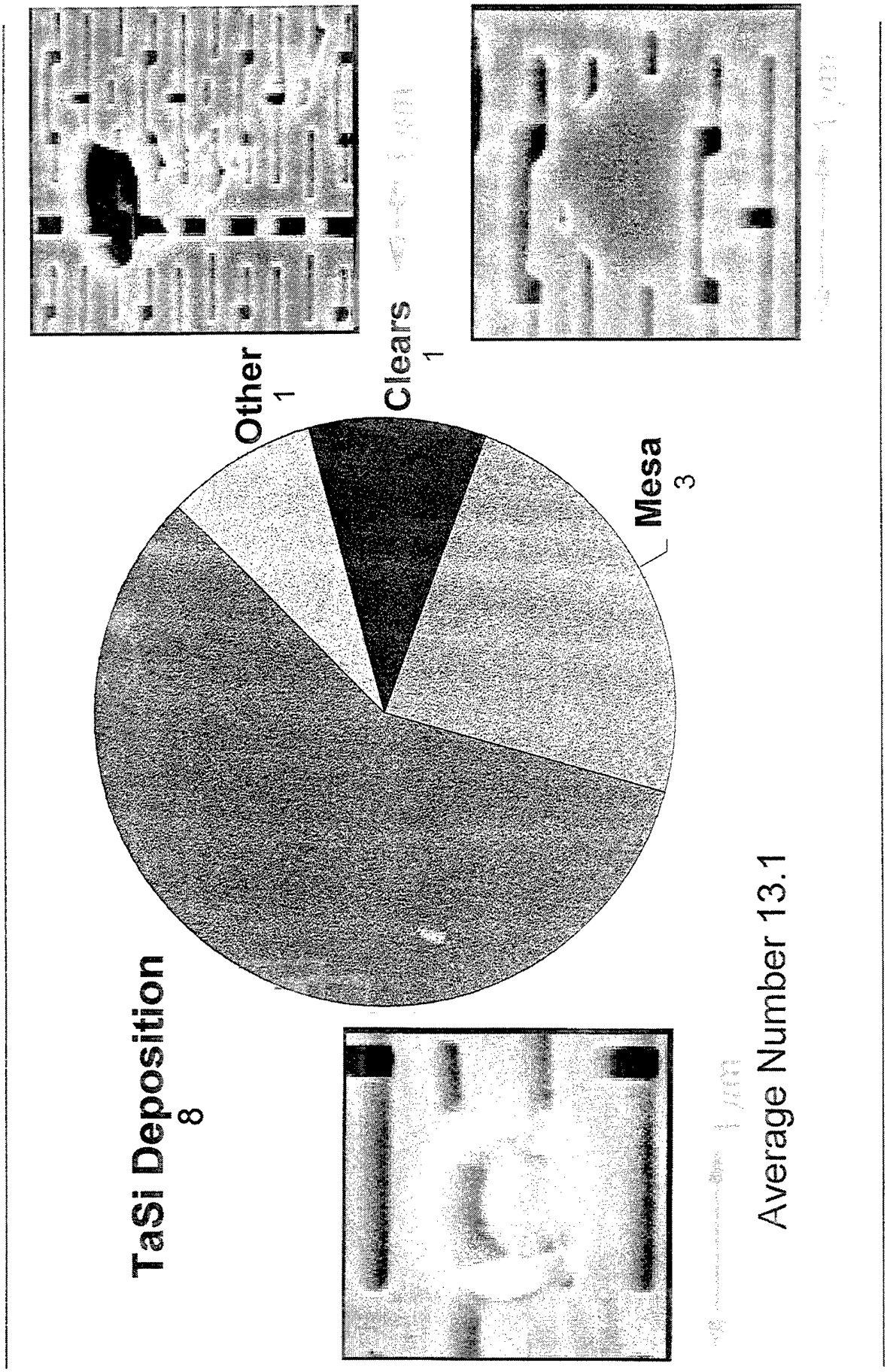


Figure 10. Non-Repairable Defect Types (November, 1998)

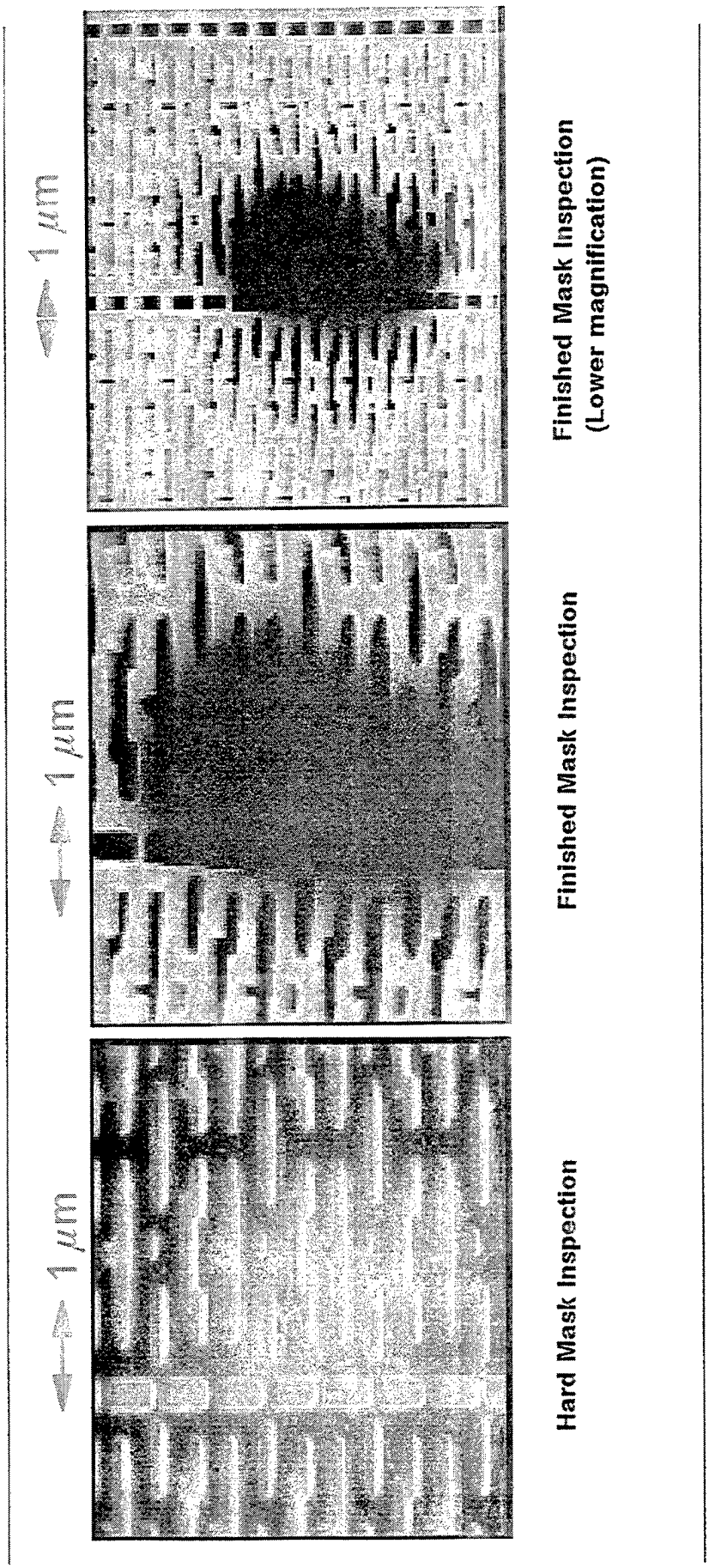


Figure 11 (Part 1 of 2). Clear Non-Repairable Defect

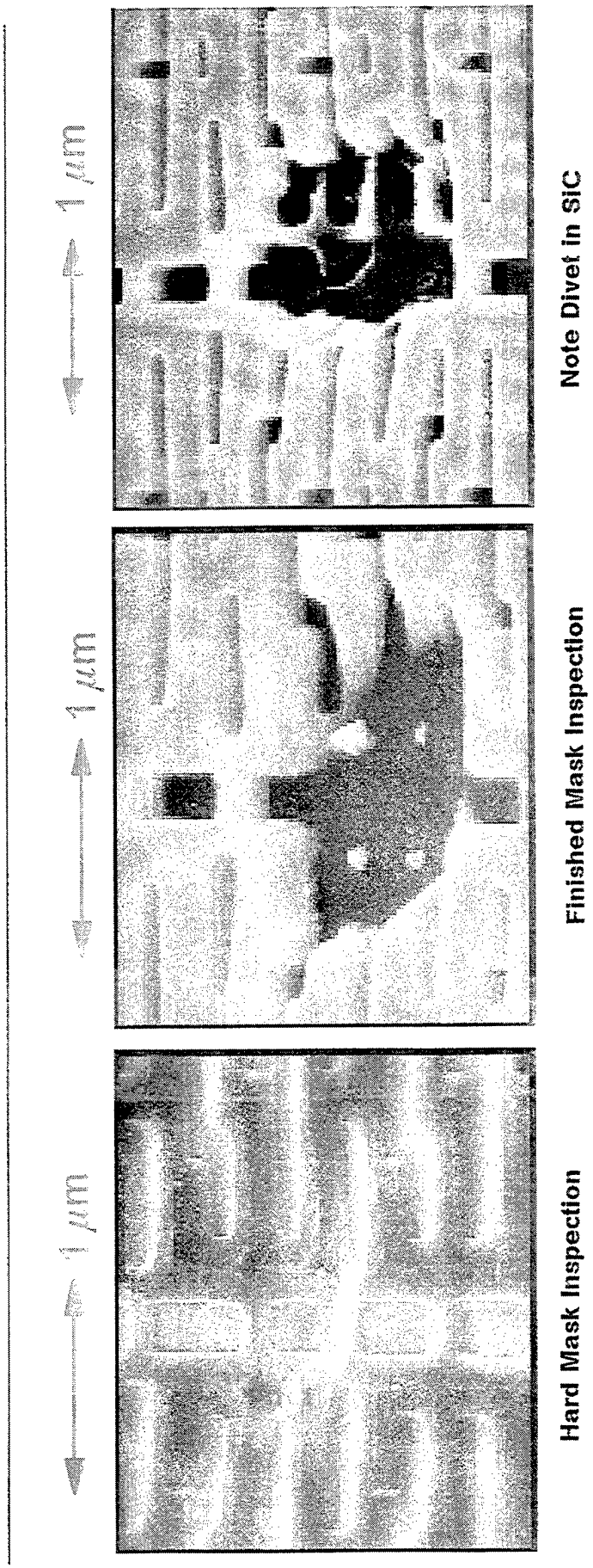


Figure 11 (Part 2 of 2). Clear Non-Repairable Defect

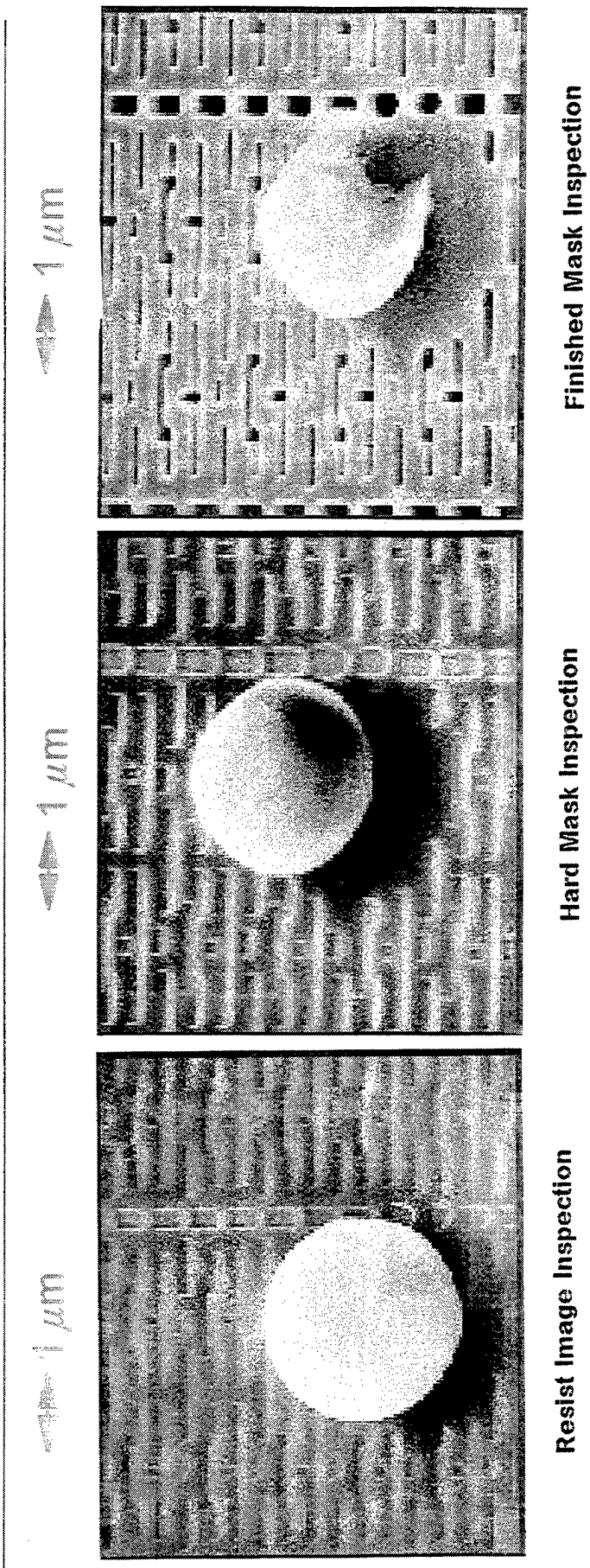


Figure 12 (Part 1 of 2). Mesa Non-Repairable Defect

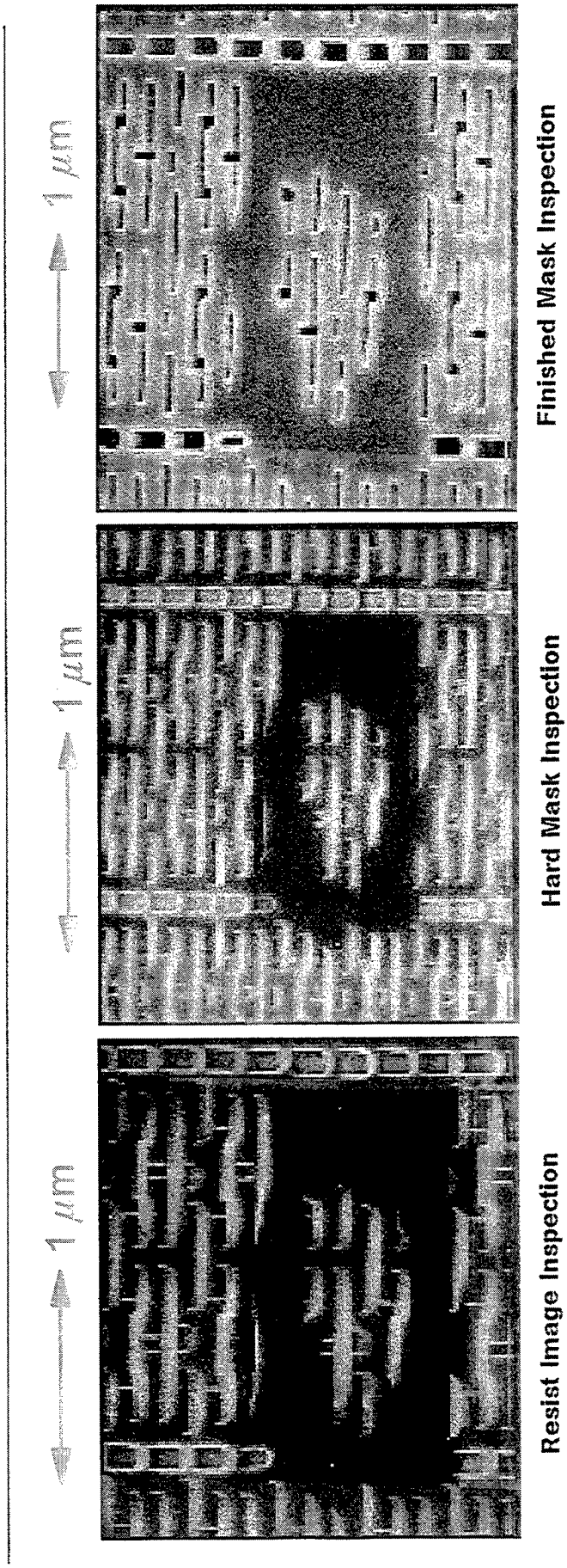


Figure 12 (Part 2 of 2). Mesa Non-Repairable Defect

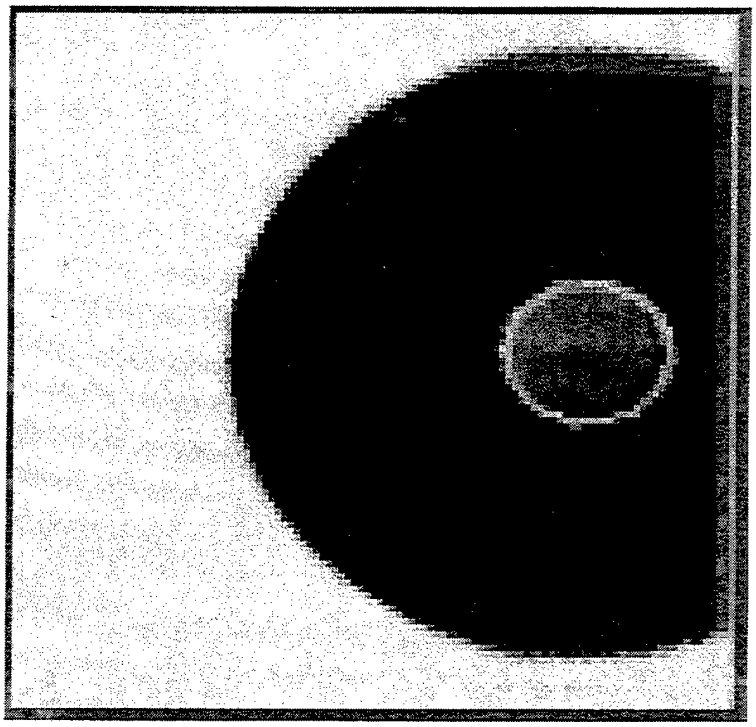


Figure 13. E-Beam Non-Repairable Defect

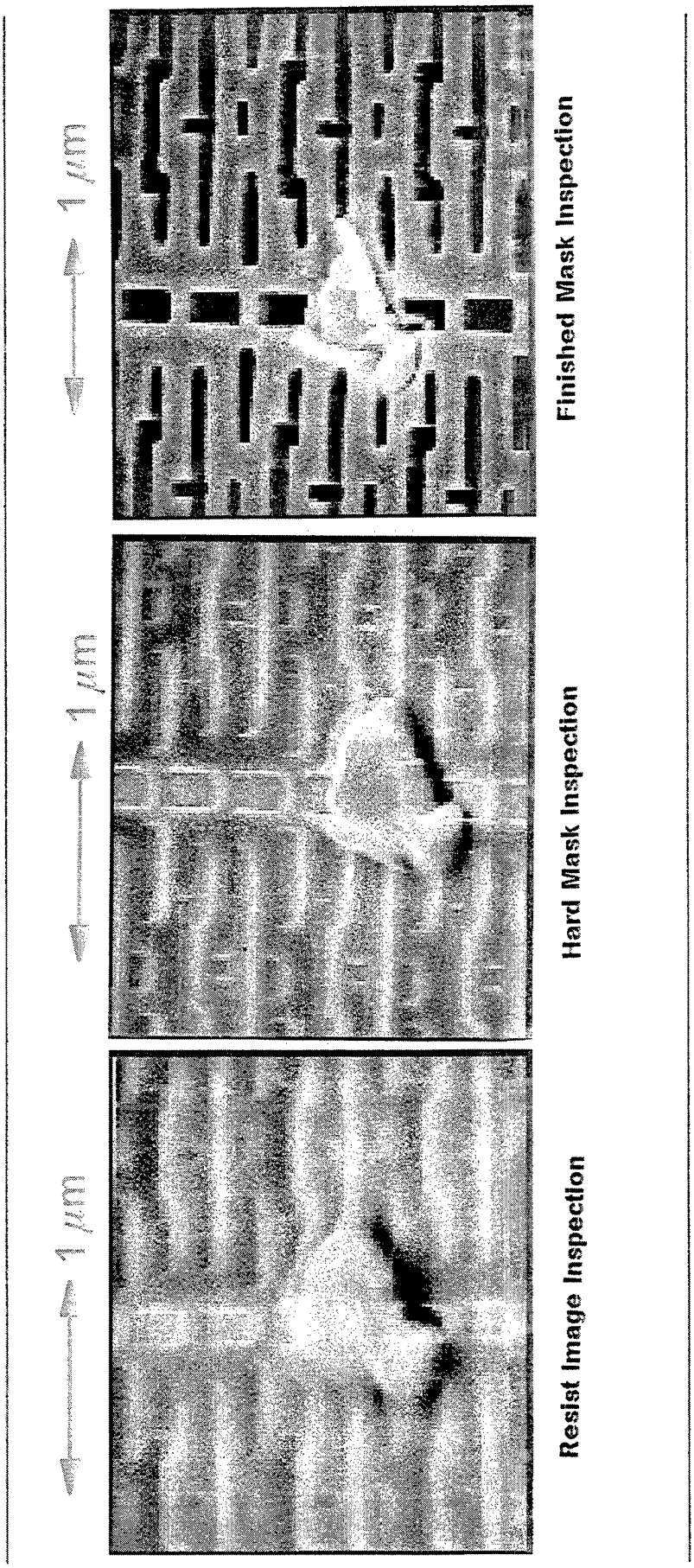


Figure 14. TaSi Non-Repairable Defects

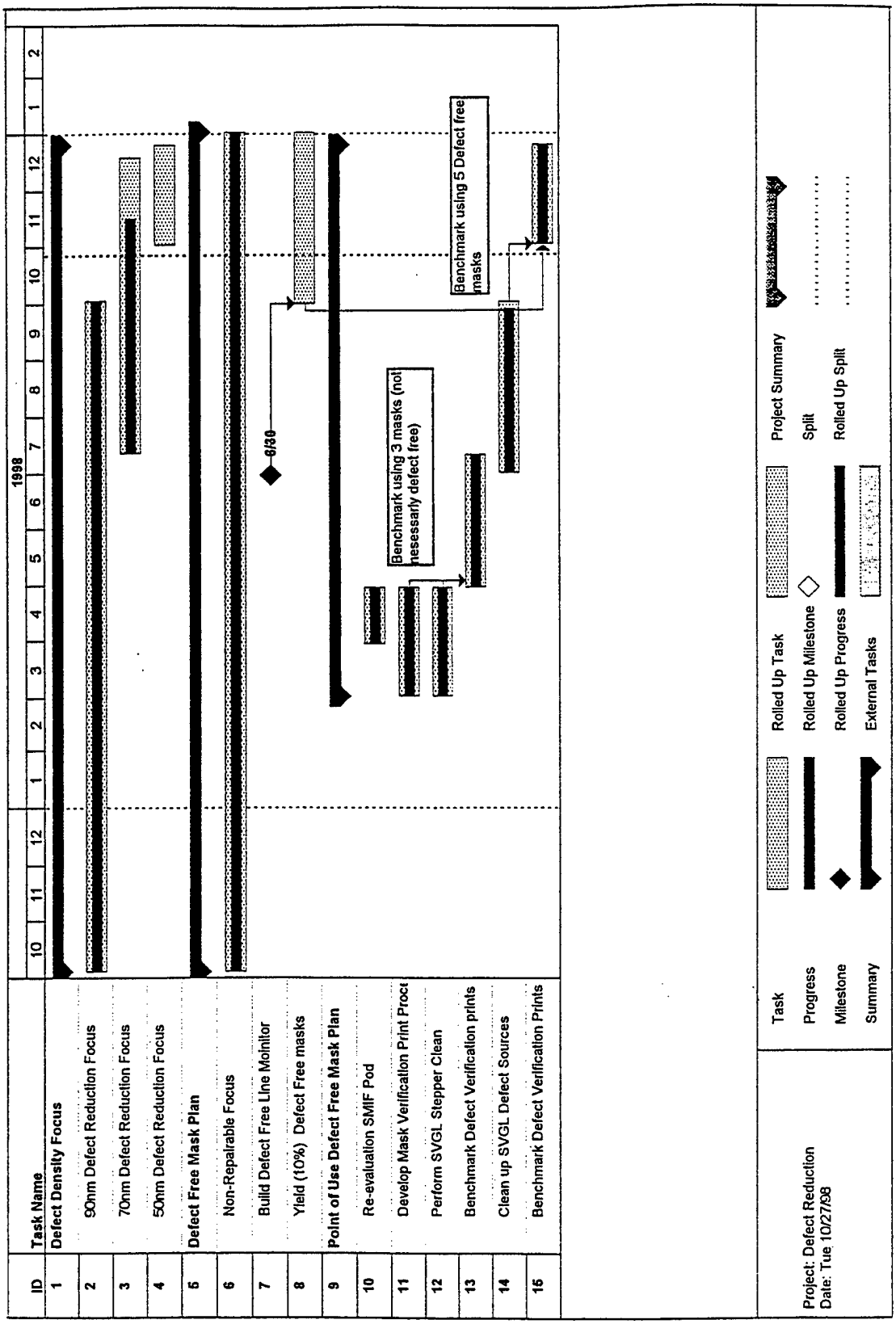


Figure 15 (Part 1 of 4). Defect Reduction Projects

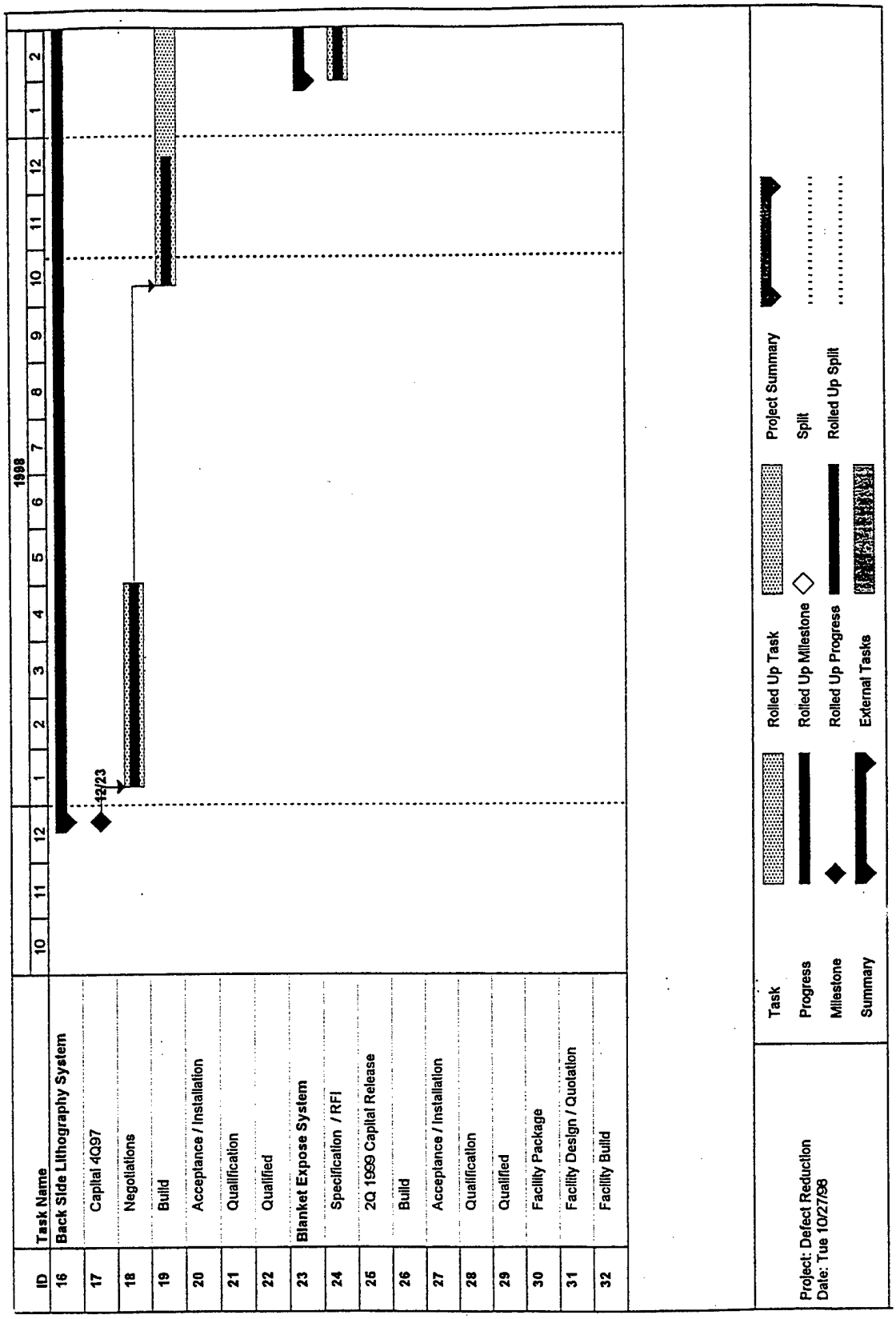


Figure 15 (Part 2 of 4). Defect Reduction Projects

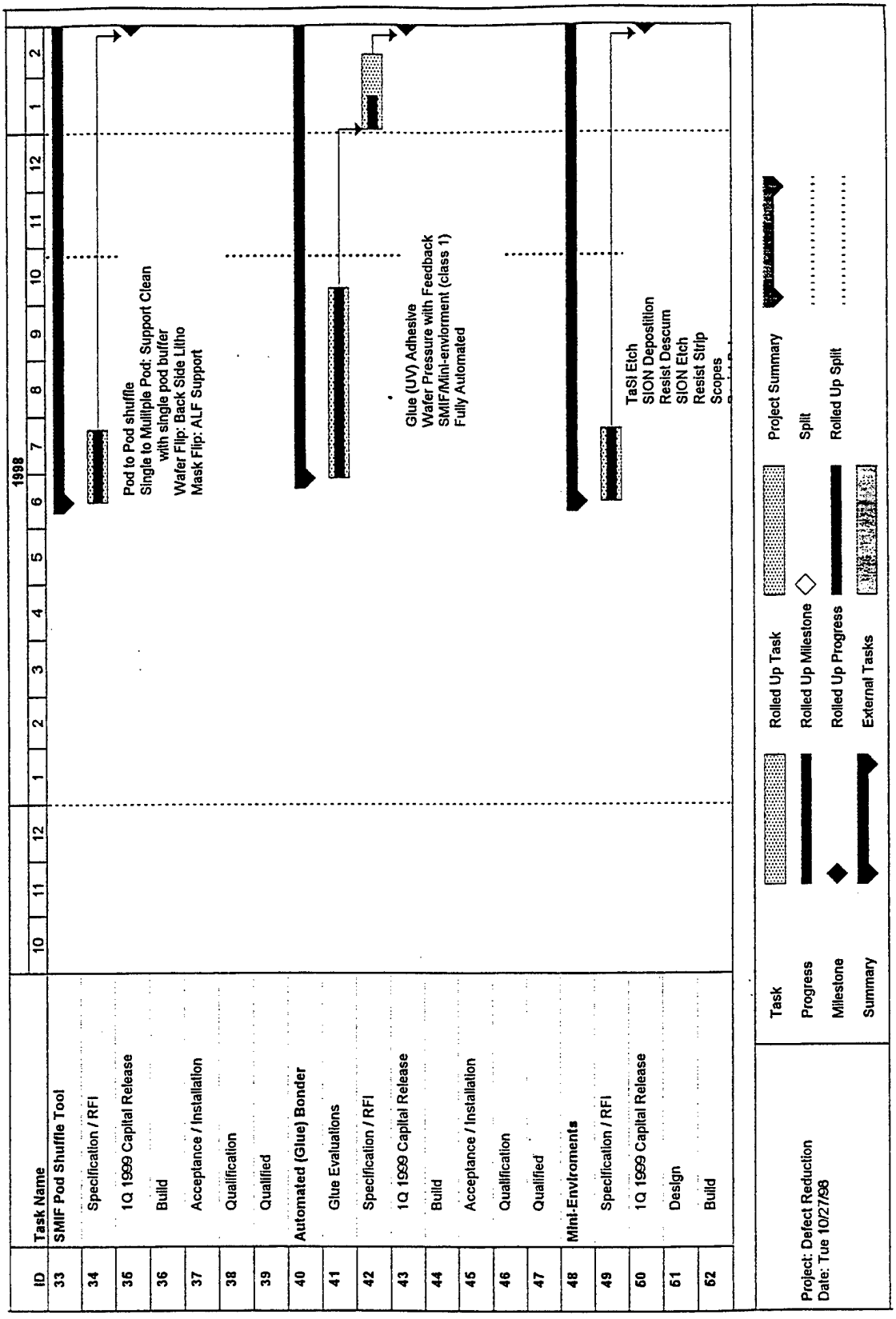


Figure 15 (Part 3 of 4). Defect Reduction Projects

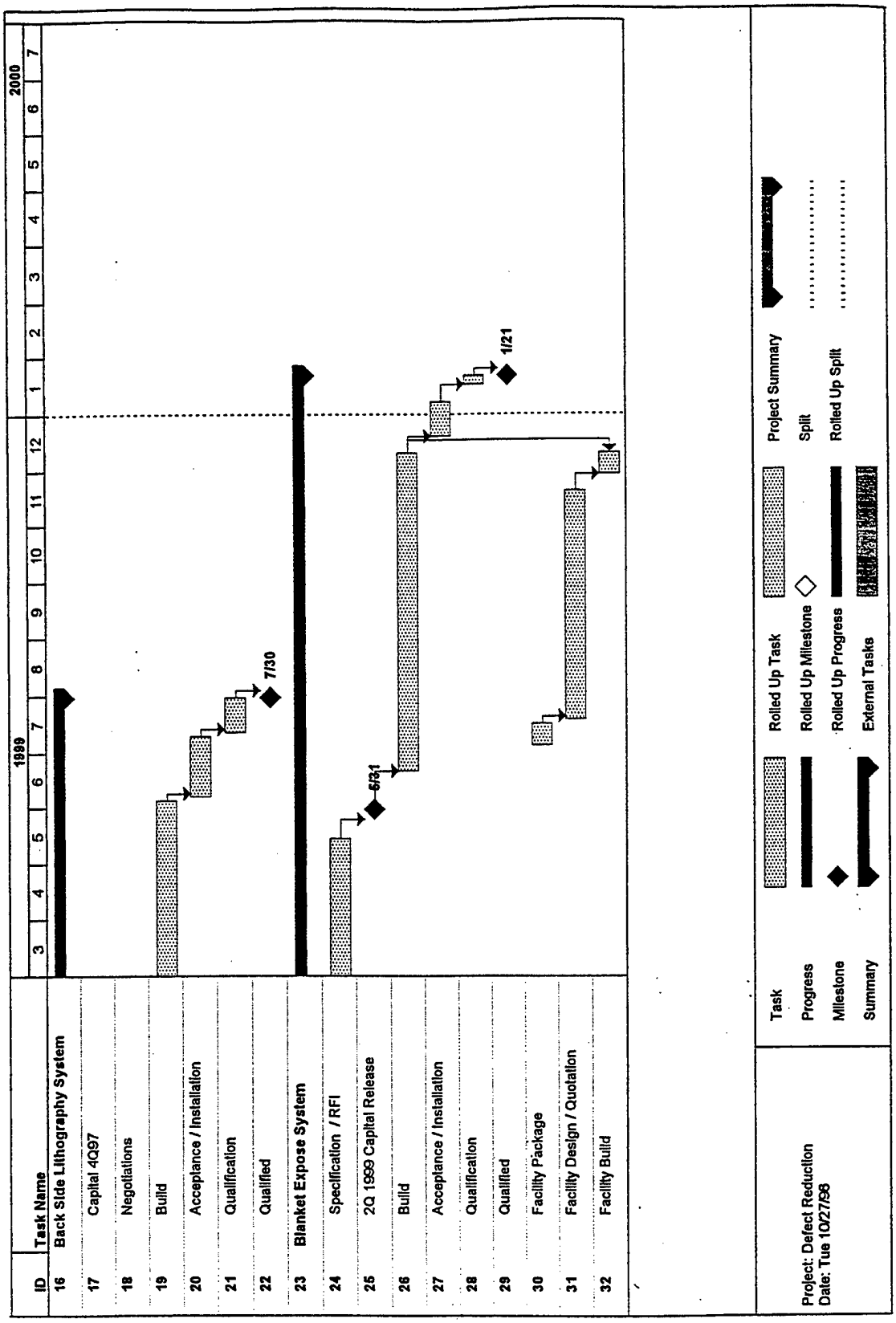


Figure 15 (Part 4 of 4). Defect Reduction Projects

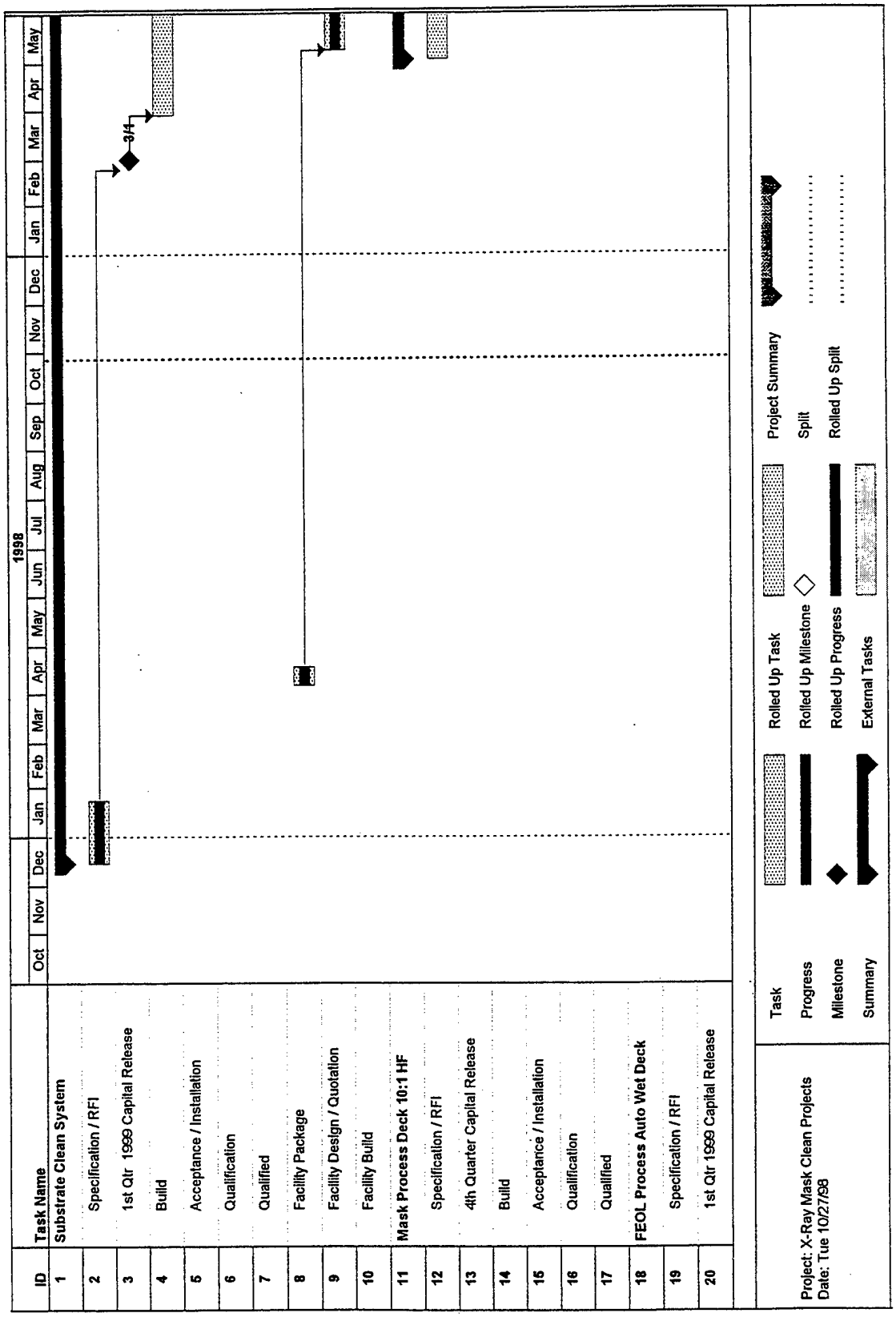


Figure 16 (Part 1 of 3). X-Ray Mask Cleans and Wet Process

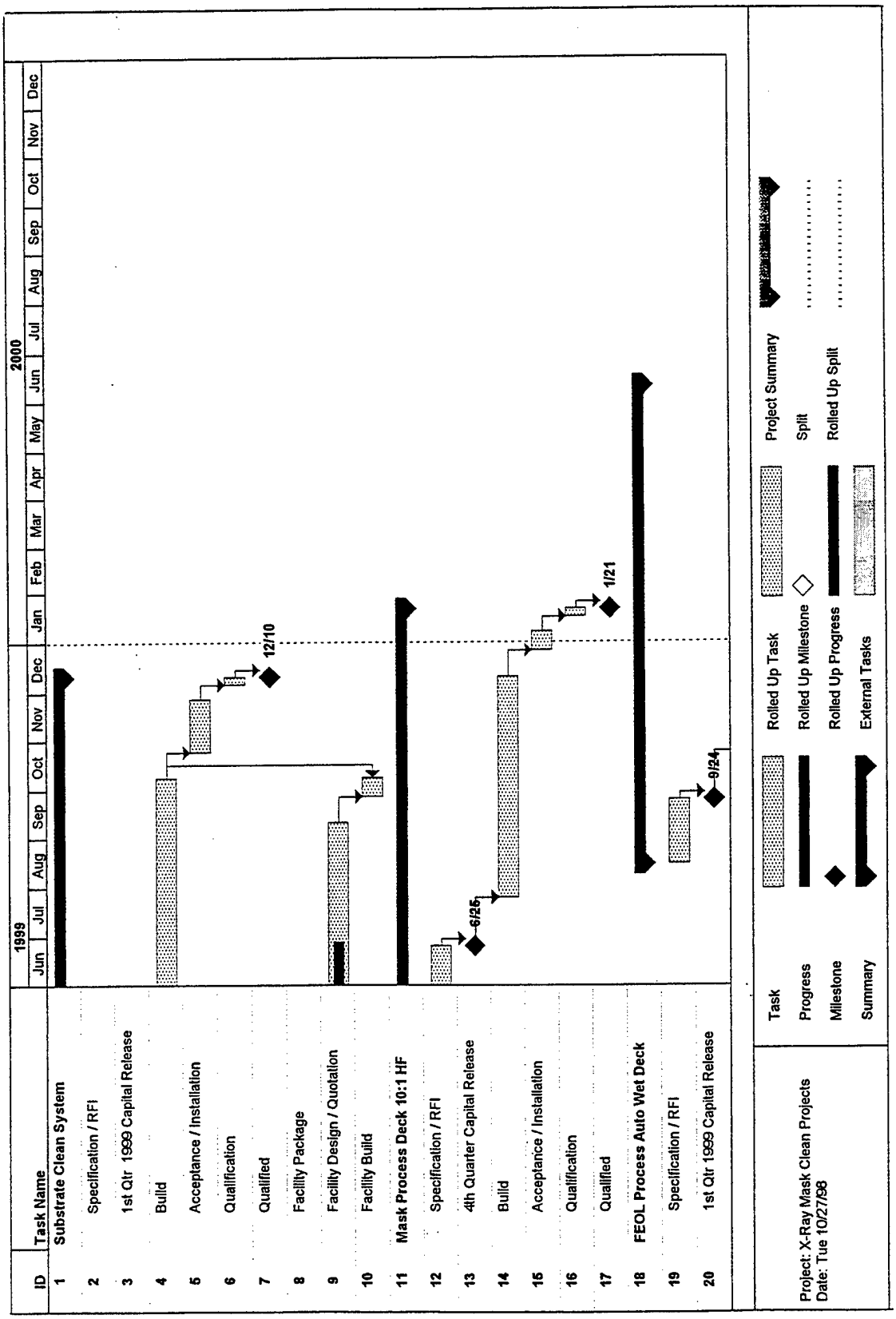


Figure 16 (Part 2 of 3). X-Ray Mask Cleans and Wet Process

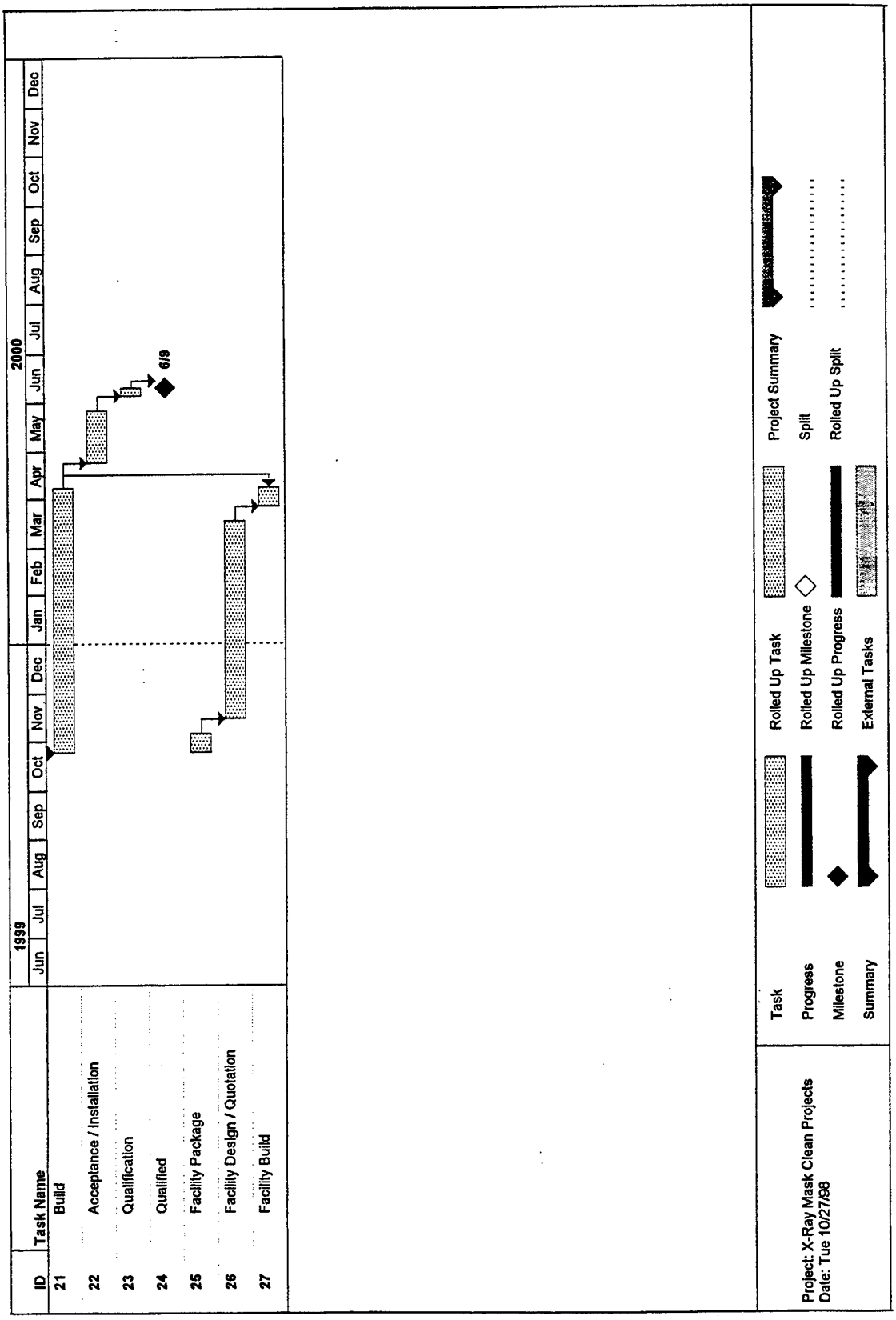


Figure 16 (Part 3 of 3). X-Ray Mask Cleans and Wet Process

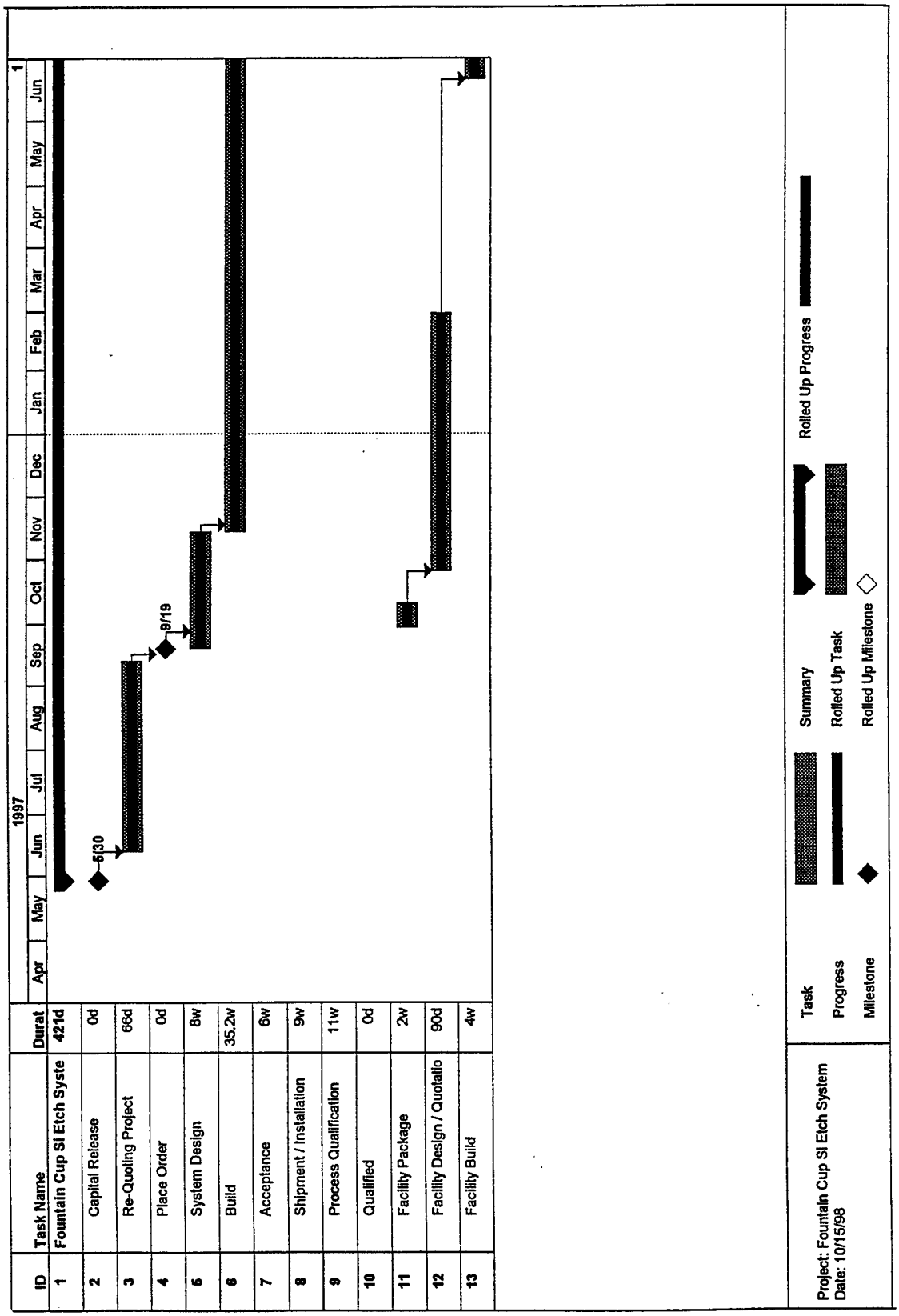


Figure 17 (Part 1 of 2). Fountain Etch System

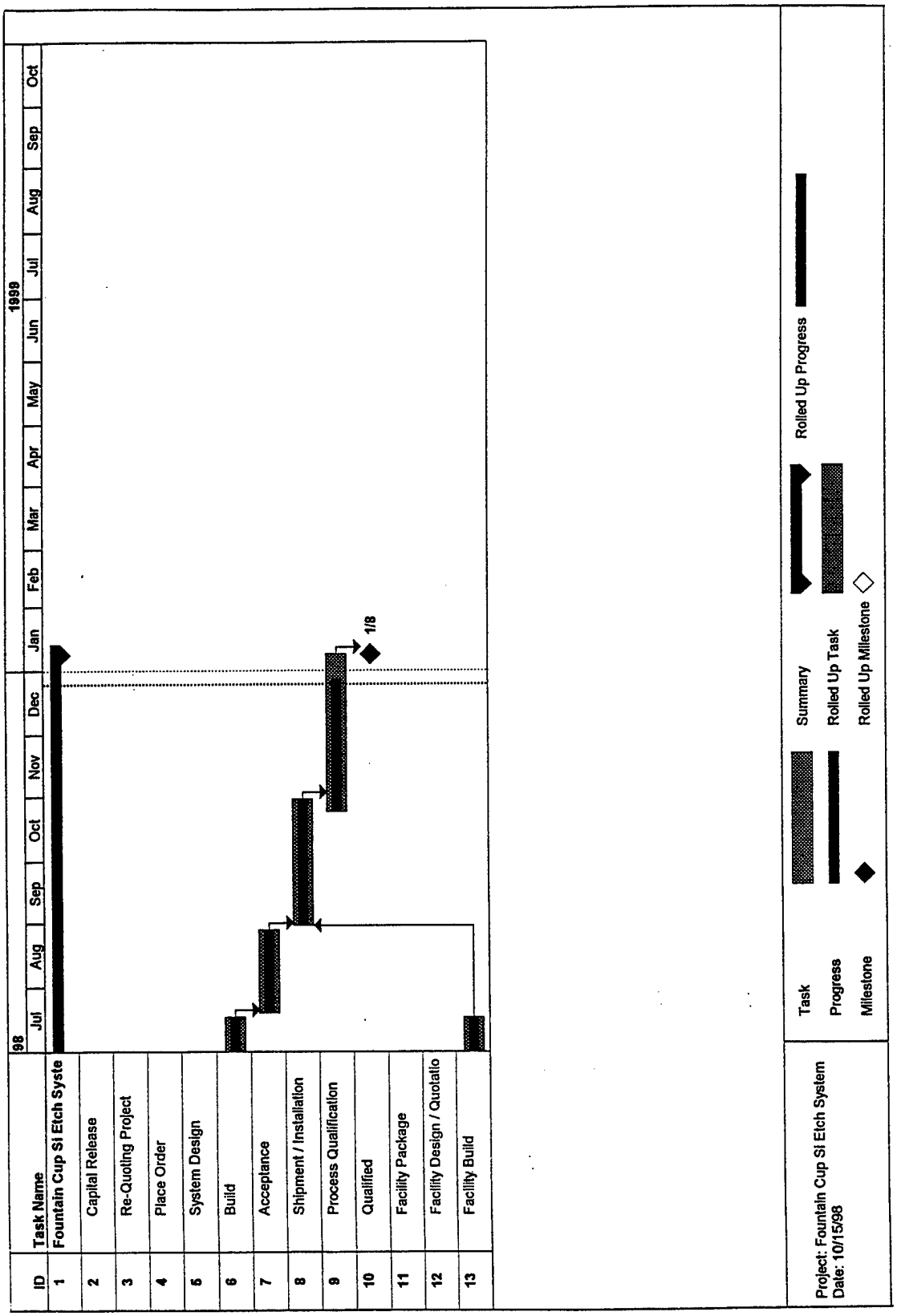


Figure 17 (Part 2 of 2). Fountain Etch System

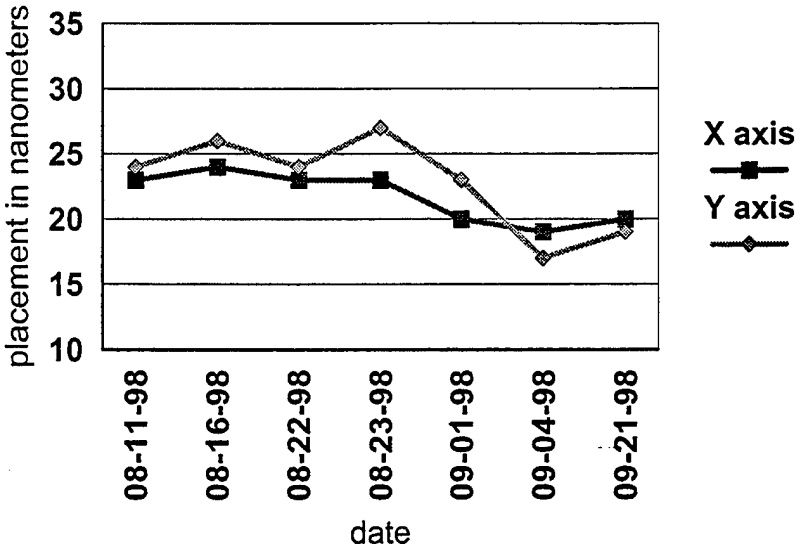


Figure 18. Ring Bonded Wafer Placement

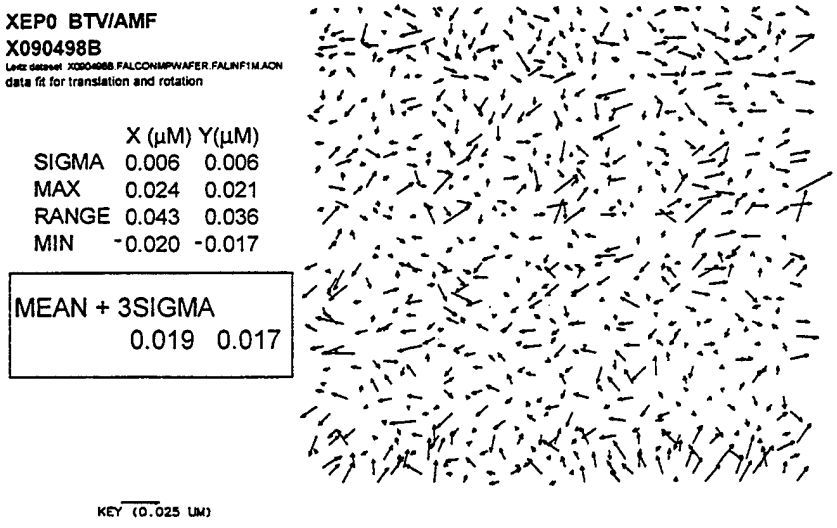


Figure 19. Falcon Multi-pass Placement on a Ring Bonded Wafer

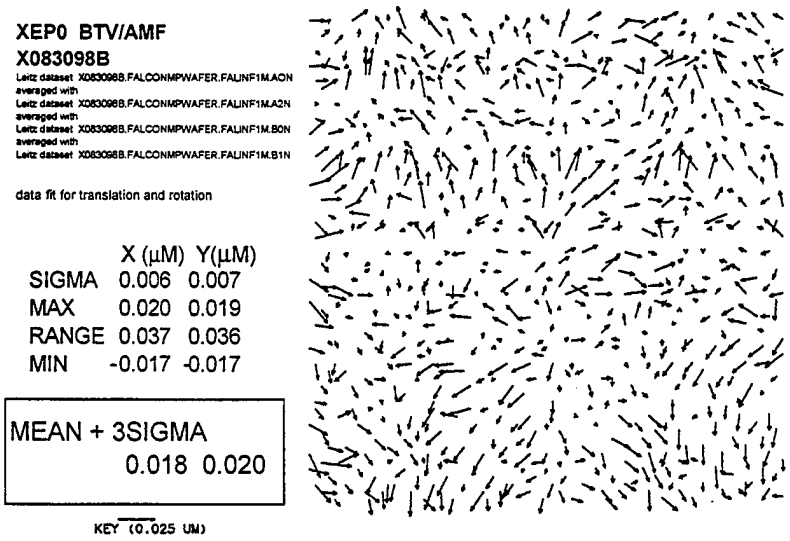


Figure 20. Falcon Multi-pass Placement on a Membrane

5.0 Advanced Lithography Mask Verification

5.1 Radiation Damage Beam Lines

ALF beamlines RD-1 and ALF-2 have been reconfigured for use as radiation damage beamlines. The existing components of RD-1 and ALF-2 beamlines were used to the maximum extent practicable to save cost and time. The systems contain a single, parabolic, collimating mirror placed 2.575 meters from the source, and a stationary beryllium window 20μm thick. The single mirror system provides increased flux levels at the exit window, decreasing exposure times as compared to multiple-mirror beamline systems. The specimen under test is scanned across the stationary beam by means of a computer-controlled motorized stage. Exposures take place in a 1 atmosphere helium environment similar to the SVGL stepper stage. The new human interface software package is designed for fully automatic exposure operation 24 hours per day, seven days per week, as long as the x-ray beam is available. The system is in use and performs as planned. The flux delivery parameter *K* for ALF-2 is 18.3 watts/cm and for RD-1 is 16.0 watts/cm. The difference between the beamlines is associated with the RMS surface roughness of the individual beam collimating mirrors.

With a source injection schedule of two refills per day on Monday through Friday and a single injection in the middle of the weekend, a target exposure of 80KJ/cm^2 should require about 11-1/2 days. Our results to date show that this accelerated schedule (versus the original plans) is working. Since two masks can be exposed simultaneously on the two beamlines, the average throughput of the beamlines for a full dose of 240KJ/cm^2 is 2.5 exposure weeks per mask. This result is being achieved with mask exchange at each 80KJ/cm^2 interval.

5.2 Overlay Tools

There was no activity on overlay tools in 1998.

5.3 SVGL Stepper

5.3.1 Small Gap Operation

One of the ALF goals for 1998 was to evaluate exposure performance down to 100nm or smaller images. Most previous exposures on the SVGL stepper have been made at mask-to-wafer gap settings of 25-40μm. In order to evaluate the performance in the 100nm area, operation at smaller gaps is required. Activities undertaken to achieve

and characterize operation at gaps of 15μm or less[1] included upgrades to the stepper, the installation of a particle detection system (PDS) and exposure studies at small gap.[2] A key component of the x-ray stepper is the X-ray Image Sensor (XrIS) which is used to define both in-plane (X,Y) and out-of-plane (Z) coordinate systems. Scanning the XrIS across the mask defines the mask location for fine alignment relative to the wafer stage. Detecting the XrIS surface with a capacitive sensor on the mask defines the wafer plane for gap sensing. Operation at gaps below 25μm required assuring that the XrIS is flat, clean and level, improving mask and wafer leveling and tightening mask protection features. Mask and wafer flatness are also compared to preset parameters in the process file to match the desired lithographic performance. If either the mask or the wafer exceed these criteria, it is rejected prior to gapping. Small gap operation was implemented by:

- Cleaning and leveling the XrIS.
- Adding sampling points outside of the membrane to increase mask protection.
- Adding a fifth measurement point on the membrane surface.
- Reducing the mask and wafer protection planes from 10μm to 5μm.

Prior to use with actual masks, small gap operation was tested and verified to 15μm. Flatness sensitivity was increased to $\pm$1μm and verified with a 3μm flat membrane. Tilt of the wafer plane setting was characterized by scanning an ultraflat wafer mounted on the wafer stage across the gap gauge sensor mounted on the mask stage. Figure 21 on page 73 shows the resultant horizontal scans with mapper calibration included. X-axis tilt is satisfactory for small gap operation well below 15μm. Y-axis tilt was further reduced by refinement of the calibration, as shown in Figure 22 on page 74, resulting in tilt of less than $\pm$0.25μm in both axes.

Because the XrIS lies in the same plane as the wafer and is scanned across the mask during fine alignment, it must be flat, parallel to stage travel, and contain no surface particles that protrude far enough to interfere with the desired gap. To prepare for 15μm gap operation, a backup XrIS was mounted, cleaned and inspected before being installed in place of the original XrIS. The new XrIS was characterized in-situ using the capacitive gauge on the mask stage. Adequate parallelism and surface quality for 15um operation was confirmed. The original XrIS was cleaned and remounted to serve as a spare.

The small gap lithography operations which confirmed the small gap stepper operations are described in section 5.5.1.

[1] A. Flamholz, and A. Krasnoperova, Small Gap Operations report to Sematech, 29 Jan 1998.

[2] This work was done with partial Sematech support.

After the 15μm gap operations were characterized and optimized, they were implemented under the stepper's RUN program and work proceeded to extend the operation to the 10μm gap setting required for imaging at and below 100nm. Operation at 10μm gap was found to be restricted by the height of surface imperfections on the XrIS installed on the aligner. Several activities were implemented to work around this limitation. First, the aligner was adjusted so that the portion of the wafer that does not travel under the XrIS could be exposed at 10μm gap. Then, in order to expose full wafers, the aligner was adjusted so that gapping could take place with the wafer positioned in front of the XrIS and completely clear of its surface. Since then an XrIS has been cleaned by laser ablation to meet the criteria for 5μm gap operation. Full wafers have now been exposed for extendibility studies at 10μm gap.

The aligner has now been optimized so that masks containing sub-100nm lines and spaces can be run automatically at 10μm gap. Acceptable 70nm lines have been produced and studies are continuing.

A discrepancy has been identified between modeling and actual exposures at 10μm gap setting which indicates that the gap is smaller than the setting. Several experiments are underway to independently measure the gap setting. These include a feeler gauge approach using wafers with calibrated standoffs, tilting of the x-ray beam to generate a gap dependent shift, and an optical interference technique.

Two beam interference techniques to determine mask-wafer gap in-situ have been designed, developed, tested and used on the aligner to calibrate the gap at point-of-use. The system consists of two diode lasers of slightly different frequencies which are combined and directed at a fixed point on the mask mounted within the aligner. The combined return signal is modulated in proportion to the mask-to-wafer gap distance. The modulation minima identify known unique points along the gap and can be used as calibration points relating the cap gauge signal to the known gaps at the sharp minima. This technique has been used with various masks including Si-B, SiC (POR process) and diamond of various thickness. The expected minima separation of 9.54μm is present in all scans. A specially designed fixture has been developed in which the gap can be scanned, the minima identified, and the gap locked and measured accurately at the minima positions using a laser confocal microscope. The gap is then calibrated by matching the locations of the minima in the in-situ scans with the calibrated minima positions determined from the calibration fixture and microscope. Preliminary results indicate that there is little difference between the measured gaps made by the aligner and the calibrated values, and the cause of the discrepancy between theory and measurements might be found elsewhere.

5.3.2 Particle Detection System

In-situ detection of particles on the wafer large enough to interfere with the mask at gap is necessary for safe, reliable operation of the aligner at small gaps. A wafer particle detection system (PDS) was designed and built by SVGL to detect particles as small as 5μ on the wafers. Hardware and software for this system were installed and

integrated as part of the extension of aligner performance to smaller gaps. The system has been characterized and is in full operation under "RUN" software.

Particles are detected by a mechanical probe which is extended above the wafer surface at the desired gap. When detection occurs, the probe, which makes light contact with the particle in order to not damage the wafer, creates a detection signal which initiates a wafer reject sequence in the control software. The probe was calibrated in-situ using a special test wafer containing a square mesa 30μm above the surface. It was used to calibrate both the probe position and sensitivity.

The positional accuracy of the probe in the gap direction was determined to be better than its specified performance of $\pm$0.5μm. It was also determined that a test particle could be located to within 1μm of its actual position. Calibration was completed and verified, and an actual wafer containing resist particles was loaded, leveled and scanned past the PDS probe. A sketch of the wafer and the actual detection signal from a 30μm particle is shown in Figure 23 on page 75.

Stepper contamination tests with the PDS system on and off showed no significant differences. PDS-on is now the standard operating procedure as shown in Figure 24 on page 75 and Figure 25 on page 76.

A spare/backup system for the PDS probe or bow has been completed. Leveling techniques for the wafer and PDS have been refined. Excellent correlation is being obtained with fixed foreign material (FM) to less than 1μm. As exposure gap is decreased, the PDS must reliably detect and reject smaller particles. To do this accurately, calibration of the wire-to-wafer gap must take place at 5μm. This has been accomplished by using a specially prepared 200mm wafer containing a single 5.5μm pedestal for use as a gap standard. The pedestal was fabricated at IBM Yorktown using electroplating, and cleaned and inspected at ALF using wet cleaning and laser ablation techniques developed for wafer inspection in general. The system is now calibrated routinely for wire-to-wafer gap accuracy for all exposures. Additional calibration wafers with 10 and 18μm pedestals have also been built and will be used to extend the range of calibration. As a result of the increased selectivity, accuracy and sensitivity, PDS has proven to reliably detect and reject particles down to 6μm.

Many wafers that pass the Inspex test are rejected by the PDS. A problem with the PDS was initially suspected, but it was subsequently found that many wafers have significant contamination at the edges where the Inspex cannot measure.

This is an excellent demonstration of the value of the PDS and it allows small gap operation at 15μm and 10μm without mask or wafer damage. A mechanical probe has been installed on the wafer stage to allow an in-situ check of the PDS wire quality and stability.

There was also a concern that PDS was interfering with overlay precision. The problem was identified as a seasonal temperature control problem in ALF. A perma-

nent fix has been implemented as described in section 5.3.4. The PDS wire has broken several times while processing wafers. Severe contact with a very large particle at a small gap causes a significant amount of mass to hit the wire, breaking it. The wire is easily replaced, with operation resuming quickly. To reduce this effect, a second scan has been added which takes place at a large gap and is performed first to protect the wire. Since the addition of this precautionary scan no breakage events have occurred.

The PDS digital detection software has been installed and tested for sensitivity. One hundred percent of all contacts are detected within 1μm of initial contact. This is a 2× sensitivity improvement over the previous analog circuitry.

5.3.3 Throughput

A throughput value of 21 wafers per hour for aligned exposures was measured in 1998. This is in good agreement with the previously reported value of 29 wafers per hour, non-aligned. Both were measured under the standard benchmark conditions.

5.3.4 DALP Aligner Overlay Performance

Overlay activities in 1998 include improving performance to 30nm (mean + 3σ), performance monitoring, and evaluating the results of new features on overlay performance.

Overlay performance baselines were taken as part of regular stepper monitoring in preparation for overlay improvement activities.

The possible effect on overlay of the new PDS system was studied. Initial results showed a baseline drift with time, possibly due to thermal or mechanical drifts introduced by the PDS system. However, it was determined that the drifts were caused by changes in the stepper make-up air temperature due to seasonal temperature changes in the ALF air handling units (AHU). The problem was solved by adding the AHU from the Suss 2 chamber in series with the house AHU and reprogramming its PID controller to supply temperature pre-conditioned air to the SVGL stepper AHU.

Overlay performance was improved by addressing stage noise, vibration and stage stability, geometric offset errors and alignment system detection robustness. The major source of stage noise was uncovered by removing the stage. It was found that the epoxy material that holds the magnets of the stepper's monolithic stage was delaminating. This was repaired and the stage's static noise was reduced by a factor of 5×. Further work also reduced the dynamic noise of the stage which affects aligner accuracy and repeatability. Wafer global alignment repeatability tests show a 10-20% reduction in overlay errors as shown in Figure 26 on page 76. The goal of tool-to-itself overlay of 30nm (mean + 3σ) has been reached (Figure 27 on page 77). Ongoing problems with the tool's stage isolation system are affecting general overlay performance. The stage isolation system was repaired to improve stability. The soft-

ware was updated and the adjustment of the control system was optimized. This adjustment required several fine adjustments to achieve stable operation. During this period of adjustment, a measurable reduction in system reliability occurred until proper tuning level was achieved.

5.3.5 Reliability and Contamination

Reliability is monitored regularly and assessed quantitatively during "marathon" runs. During a mask lifetime marathon in May of 1998, MTBA of 48 hours and an MTBF of 16 hours were measured. As a result of improvements in stage stability and control, vibration isolation control, PDS protection, and water pump design, MTBF improved to 51 hours during the November, 1998 lifetime-with-overlay marathon.

Regular contamination monitoring continues with PDS "on". Performance is consistent at 2-4 adders below 5μm per pass, with no difference observed before and after the stage repairs.

5.4 ESR Status

Source operations in 1998 have been affected by the status of the klystrons. The klystron that failed in 1997 was returned after rebuilding at the factory. This klystron has been installed into modulator 1 and is being used for the routine injections. There has been some concern that it is not delivering full output which may indicate a problem in the modulator. This is a continuing area of investigation. It has not been established if the problem is a true reduction in power output or an instrumentation problem.

The two other klystrons are now available as spares, but both are running with limited output. Serial Number 0011 requires extensive reconditioning before each use following an idle time of several months, and also has limited power. Serial Number 0014, the original spare, is only operating on one of the two filaments. This limits its output and will also severely limit its lifetime. A decision must be made as to which of the two will be returned next to the factory for reconditioning.

Even with these limitations, injection times have nearly returned to the normal mean of 15 minutes with somewhat more than normal operator intervention. Up-time has remained good. See Figure 28 on page 77.

A study of the ALF light source equipment necessary for maintenance and spare parts upgrades has been started by Oxford Instruments and their consultants. We have changed this from a quick, two month study to a more detailed, longer term study. Present plans do not allow for the installation of either the previously identified new control system or the upgraded cryo system this year. These are both required to ensure reliable operation for the next five to 10 years.

The ALF facility was shut down for one week in the spring for maintenance. Maintenance activities included replacing the noisy motor on the helium compressor, replacing cracking cooling water hoses and replacing a cracked plastic flange on the jacket cooling water system. The new "quick purge" was used on the cryo system since the compressor was down for less than 24 hours. It is considered successful even though a slight decrease in fridge excess capacity was observed.

The rebuilt helium compressor motor that was installed during the maintenance week was found to have a noisy bearing and it had to be replaced in a second shutdown. A cracked metal flange was also repaired in a liquid helium transfer line. This time a full fridge purge was performed. Cooling capacity is still slightly lower than expected which could be caused by wear on the turbines in the fridge.

Beam lifetime has improved significantly after the recent shutdown and warmup of the dipoles (see Figure 29 on page 78). The improved beam lifetimes should permit fewer refills for long term runs.

A new provision of the 1998 contract with Oxford Instruments was the formation of a rapid response team to respond quickly to any problem with the equipment in ALF. This concept was successfully tested recently after a weekend failure of the cryo system. The Oxford Instruments engineers were notified by the telephone call-out system at 4:00 am on a Saturday morning. They found the deWar heaters on full and helium gas being vented rapidly from the emergency over-pressure vents. They determined that it was not a simple problem and an expert was called in from Oxford Instruments. He arrived Monday and remained for the entire week until normal operation was restored. The investigation revealed that two cryogenic valves were in the wrong position which could have caused the problem and would have prevented the normal system controls from preventing the problem. The vacuum seals on the deWar valve box were sprung as a result of the excess pressure. Fortunately, the inner seal reseated after it was warmed up and an epoxy patch was successfully applied to the outer seal. Steps are being taken to prevent a recurrence.

5.5 Mask Verification and Wafer Process

5.5.1 Lithography Characterization at 15μm Gap

Prior to lithographic experiments at small gap, the stepper was tested with resist-coated wafers and a test site mask. The wafers were exposed at 17μm gap and both the mask and wafers were inspected visually for any signs of damage. None was found.

The system was then tested for gap control. The experiments were done in a manner that eliminated the effects of mask and wafer flatness. The exposures were done at several plane levelings with values of 3μm and 8μm gap variation. Any effect would be expected to be less pronounced at 25μm gap than at 15μm gap. An LTM-4 lithography test mask with 175nm linewidth was used for the tests. The results were in general good agreement with the predictions, with the gap variation having a larger effect at 15μm than at 25μm, as discussed in the 1Q98 progress report. At 8μm variation, the gap variation dominates the results. Similar effects were seen with both negative and positive resists.

The SVGL stepper has been shown to work well at 15μm gap, with printing demonstrated at 150 to 125nm dimensions. It has been shown that CD mask variation is the major contributor to CD error on the printed wafer. At smaller gap (15μm), CD was closer to nominal for these image sizes, and gap control is also critical for precise CD control.

5.5.2 DRAM Test Masks

DRAM test masks are utilized to analyze the leading edge cell designs for DRAM memory cells. The current linewidth target is 150nm and special test masks are being made at 130nm. DRAM test masks have been ordered to provide early learning with respect to lithographic processes and all processes involved in integrating a DRAM integrated circuit.

In 1998, ALF received the mask types shown in Table 12 on page 65. The first (type 1) was used to demonstrate x-ray lithography and develop reactive ion etch processes at 150nm and below. The second mask type (type 2) is a lithography test site used to demonstrate x-ray lithography at 150nm and below. These masks contain the latest cell designs for 1Gb DRAM cells. New non-orthogonal design shapes (tilted lines, multiple lines, multiple segment lines, curved shapes, et al.) have recently been introduced and have proven to be a challenge to both the mask fabrication process and the lithographic process. The type 3 mask listed in the table focused attention on the challenge of these new shapes. Type 4, 5 and 6 expands the range of sizes and shapes. Printing of the new design shapes by x-ray has exceeded the optical capability. X-ray lithography, driven by the MMD's ability to make masks, is now the front-up learning vehicle for DRAM integration.

5.5.3 Power PC Logic Test Site Masks

In the continuation of a project started in 1997, a series of x-ray masks for the gate level of an advanced Power PC™ microprocessor were exposed in ALF. The exposure field consists of six chips and an electrically testable kerf. The specifications were:

- Critical dimension = 250nm (3σ = 20nm).
- Image placement = 40nm (3σ).
- Defect-free: one chip plus kerf minimum.

Table 12. DRAM Test Masks

Mask ID	Level ID	Mean Linewidth	Placement 3σ	Defect Specification	Date Delivered
66C6	Type 1	0.150μm	48nm	0 > 100μm^2	3/23/98
65B-4	Type 2	0.139μm	NA	0 > 100μm^2	4/21/98
66B-6	Type 2	0.148μm	NA	0 > 100μm^2	4/21/98
68D-1	Type 1	0.154μm	88nm	0 > 100μm^2	6/23/98
B17B6	Type 2	0.138μm	NA	0 > 100μm^2	6/25/98
70A-3	Type 3	0.142μm	NA	0 > 100μm^2	7/30/98
74D-1	Type 5	0.165μm	NA	0 > 100μm^2	10/29/98
B36C-4	Type 5	0.152μm	NA	0 > 100μm^2	10/6/98
75C-1	Type 5	0.155μm	NA	0 > 100μm^2	10/16/98
76D-2	Type 5	0.129μm	22nm	0 > 90nm	11/12/98
B38C-5	Type 6	0.148μm	NA	0 > 100μm^2	10/29/98
71D-5	Type 6	0.163μm	NA	0 > 100μm^2	10/29/98
71D-3	Type 6	0.148μm	NA	0 > 100μm^2	10/29/98
71D-1	Type 2	0.131μm	NA	0 > 100μm^2	11/12/98

Two engineering quality masks were used for critical dimension print verification and wafer process development. The best process was chosen by optimizing critical dimension control variations.

Another engineering mask was used for verification of mask cleaning procedures in ALF. The mask was pre-inspected on the MMD KLA SEMSpec, cleaned in ALF, and re-inspected by the KLA. No additional repeaters were found.

The best of the product quality masks were chosen for wafer runs. All chips on mask #60A-2 were defect-free and the ACLV on the individual chips was 17-21nm (3σ). It was used for the first exposure lot. A second mask (55A-6) with five defect-free chips was used for a second lot. The results were:

- ACLV in one field of 17 to 26nm first mask. 7 to 19 for the second.
- AWLV 8nm 3σ.

- Image placement better than 70nm 3σ.
- No repeaters after x-ray prints.

Figure 30 on page 78 shows the distribution of ACLV on 24 chips on a wafer from the second lot (four exposure fields, 6 chips per field).

Another lithography process control test using a logic test site was run jointly with IBM Yorktown Research. In this study, linewidth control was measured on nominal 100nm images across the wafers using UV-4 resist. The first lot of wafers was exposed and processed successfully with ACLV values of about 10nm for X and Y. A second lot was then exposed. In the second case, a large variation in linewidth was found in a section near the top and edges of the wafers (Figure 31 on page 79). Variations as great as 40nm were measured for both X and Y. The variables of dose, gap and development have been eliminated as causes. It seems most likely that the cause is non-uniformity in the postbake hotplate at position #8 in the stepper track. UV-4 resist is very sensitive to postbake. These variations might not be observed with other resists.) The investigation is continuing.

5.5.4 Extendibility Studies

In cooperation with IBM Yorktown Research, gate level logic test site samples were exposed with CD of 70nm. The LTM-4 mask used was written on the VS-5 vector scan e-beam writer at Yorktown. The exposures were done on the SVGL DALP aligner at 15μm gap and produced 70nm isolated lines in resist (Figure 32 on page 79).

Another test mask was used for studies of the extendibility of x-ray lithography to 75nm groundrules. This mask had various features with CD = 75nm, including 75nm lines and spaces at 150nm pitch. The exposures were made at 10μgap using UV2HS resist.

5.5.5 Type 3 Mask Verifications

The effects on x-ray masks used with a large number of wafers in the SVGL stepper were studied in 1997 with Sematech support. In the first phase of the 1997 test a significant amount of foreign material (FM) was deposited on the mask and significant distortion was also observed in the mask. After taking a variety of steps to eliminate possible causes, a second phase was performed without similar depositions or distortions. This work has continued in 1998 with Sematech support.

In the first phase of the 1998 study, 1000 wafers were exposed in a single, seven-day "marathon" run using the same low absorber coverage Nighteagle pattern mask as used in 1997. All wafers were coated with UV2-HS photoresist and exposed at 20μm gap (compared to partial coating and 30μm gap in 1997). In addition, the SVGL Particle Detection System (PDS) was used to detect the presence of large FM on the wafers prior to exposure. Inspection of rejected wafers confirmed that the PDS was

operating properly. Both the synchrotron and stepper performed very well, with no significant time lost to any failures.

There was no observable difference in image size on the mask from pre- to post-exposure. There was, however, a shift in image placement. Y shifted about 23nm and X about 5nm. These changes are believed to be due to the use of silicon oxynitride as the hard mask for etch control.

Repeater defects were measured on 10 wafers during the test. The results are significantly improved over the 1997 results, with no adders between wafer #468 and wafer #904 (see Table 13).

Table 13. Wafer Repeater Check Results

Wafer Number	Repeaters	Adders Above Baseline	Δ Wafer-to-Wafer
1*	28	---	---
109	29	+1	+1
208	31	+3	+2
350	32	+4	+1
468	36	+8	+4
562	36	+8	+0
742	36	+8	+0
904	36	+8	+0
960	35	+7	-1
1028	32	+4	-3

* Baseline

Significant improvements have been demonstrated in this work compared to the 1997 results. Over 550 wafers were exposed with no increase in the number of printed defects, no change in image size and only small changes in image placement which can be explained by a change in the stress of the membrane.

A second phase was run with about 100 wafers exposed at 15μm gap following the general plan of the first phase. In this three day marathon run a total of 121 wafers were exposed with a similar Nighteagle pattern mask at 59 fields per wafer. There were some brief interruptions to this run caused by the stepper's vibration isolation system. The synchrotron again performed very well.

There was no detectable change in image size and only a 10nm change in image placement for this run. During the exposure run, a resist adhesion problem developed that caused some features to fall over. This was traced to wafer surface contamination. After two additional exposure runs, wafer #121 was deemed acceptable for repeater check inspection and was sent to the MMD.

Three of the 121 wafers exposed were inspected for repeater defects. The results are presented in Table 14 on page 68. Again, very few defects were added during the extended processing. (There were five additional mask load/unload cycles during this test.) Wafer cleanliness continues to be a key element in defect-free exposures. Some of the wafers used for this experiment were reworked from the previous phase, which caused the resist adhesion problems. Additional mask load/unload cycles were required to diagnose the resist problems, which contributed to the additional adders between wafers #97 and #121. An unexpected, large quantity of new foreign material was found on the mask used for the marathon run, attributable to the additional cycles.

Table 14. Wafer Repeater Check Results

Wafer Number	Repeaters	Adders Above Baseline	Δ Wafer-to-Wafer
1*	14	---	---
97	17	+3	+3
121	18	+4	+1

* Baseline

This work has demonstrated that continuous exposures at 15μm gap is currently possible, and has also provided additional information about defect printability.

As part of a continuing contract with International Sematech, IBM Yorktown Research is testing the radiation hardness of the process-of-record (POR) mask materials as well as that of new materials available in a semi-experimental basis, that are likely candidates for future masks. Twelve masks are being exposed in ALF beam lines ALF-1, ALF-2, RD1 and in the stepper.

In this year's effort the test of POR materials included determination of threshold for radiation damage detection, saturation dose value, effect of external applied forces during irradiation, and distortion during uniform irradiation of the mask. Additionally, use of overlay (O/L) measurements, as opposed to direct measurement of fiducials on the mask, is being investigated due to its potentially higher resolution and repeatability with consequent higher sensitivity. New materials tested included Ta_4SiC supplied by Hoya, SiC supplied by ATT-AT (alternative to Hoya's material), and diamond films supplied by Crystallume. The external applied forces were of the same magnitude as those needed for the magnification correction scheme under consideration. All the masks used were fabricated by the MMD and irradiated at ALF. Uniform irradiation of the full 26×33mm mask field was achieved using new exposure stations built onto existing ALF beamlines that provide for scanning of the sample in the vertical direction to mimic the type of irradiation provided in the SVGL stepper. Direct and O/L measurements in the Leica LMS 2020 and KLA 4015 were performed in MMD and ALF, respectively.

In addition to the above tests using specially fabricated test samples, off-the-shelf Nighteagle masks were irradiated in the SVGL stepper under conditions identical to normal wafer exposures.

For the TaSi/SiC POR stack, the threshold and saturation values were determined using an accelerated damage test, where a 5×15mm spot was irradiated in a 26×33mm TaSi/SiC mask membrane. Using available metrology tools (Leica 2020), the minimum dose needed to detect distortion was found to be approximately 20kJ/cm^2. Saturation occurs between 60 and 80kJ/cm^2. Further refinement of these figures is not considered worthwhile. Results obtained so far (160kJ/cm^2) using uniform irradiation confirm earlier results obtained using a tiling technique (quasi-uniform irradiation) that demonstrated a distortion within the resolution limits of the Leica 2020 (approximately 12, 12nm mean+3σ), with no discernible character. Applied external forces during irradiation do not appear to induce additional distortion, either during accelerated or uniform irradiation.

Damage to one sample of Ta_4B/SiC using uniform irradiation to 240kJ/cm^2 also showed distortion within the resolution limits of the Leica 2020, with no discernible character. The ATT-AT SiC and diamond films, one sample of each material, were tested using accelerated irradiation. The distortion of ATT-AT SiC was found to be 23, 28nm, mean+3σ, at 240kJ/cm^2, approximately 2× larger than that of the Hoya material. Uniform irradiation results are needed before a decision can be made regarding the viability of this material. The diamond sample showed unacceptable large distortion of 148, 165nm, mean+3σ, at 240kJ/cm^2. The cause of this large distortion (probably hydrogen content) is being investigated. The information will be provided to the manufacturer for modification of the deposition process.

The O/L technique appears to indicate a slightly higher sensitivity than direct measurement, in that it reveals the presence of character at the same dose. Experiments are presently underway to rule out artifacts that might cause this effect.

Off-the-shelf Nighteagle masks irradiated in the SVGL stepper to 8.5 and 17kJ/cm^2 have shown unusual distortion results: distortion that is larger than expected and character that is not reproducible from sample to sample and that can even reverse direction as the dose is increased. It is hypothesized that these effects result from the use of SiON as a hard mask during patterning of these masks (the SiON is removed at the end of the process). Tests are in progress to pinpoint the origin of the problem.

5.5.6 Printability of Repaired Mask Defects

Both opaque and clear defects are routinely repaired on x-ray masks in the MMD. Opaque defects are repaired by focused ion beam (FIB) milling and clear defects are repaired by ion beam deposition of gold. A joint ALF/MMD study was conducted that looked primarily at the edge placement accuracy of the repairs on the mask as reported in the 3Q98 progress report.

Based on the study, the following recommendations were made to produce repaired masks with better edge placement:

- For opaque defects, use a 20nm larger repair box.
- For clear defects use a 20nm smaller repair box.
- For opaque defects, overetch to ensure no remaining film.
- For either opaque or clear defects it may be necessary to remove film splattered from the repair process and deposited in other locations.

5.5.7 Mask Verification Summary

5.5.7.1 Type 1

Five masks have been exposed in ALF as part of a defect reduction joint test with the MMD (see section 4.1.4.2).

5.5.7.2 Type 2

A total of 14 advanced DRAM masks have been given type 2 verifications for image placement and quality in 1998.

5.5.7.3 Type 3

Two masks have been exposed in the SVGL stepper for extended lifetime tests.

Twelve masks are being exposed in the various beamlines for extended radiation damage tests.

5.5.8 Contamination and Lifetime

A series of mask contamination and lifetime studies are ongoing in the ALF with partial support from Sematech.[1] In the first part of the study, a target of 5000 wafer passes in the stepper was planned: 3000 with a low absorber coverage mask and 2000 with a high absorber coverage mask. The masks were pre- and post-exposure measured on the KLA SEMSpec tool in the MMD. Mask image placement and linewidth data (CD) were other key parameters compared before and after exposure. Repeating defects on wafer prints were also monitored.

The low absorber mask, a Nighteagle line monitor, was exposed in October and November of 1997. The high absorber mask, a Falcon (reverse tone Nighteagle), was exposed in December of 1997. For both series of exposures, selected wafers were gold coated and sent to the MMD for KLA inspection. The masks were also inspected before and after exposures as described above.

The results from the low absorber mask were complicated (as discussed in the 1Q98 status report) by "scratch" events that appeared on the mask. If these scratch events had not occurred, the defect repeater adders over the full 3000 wafers, within the KLA

measurement precision, would have oscillated near zero. These results are shown in Table 15 on page 71 and Figure 33 on page 80.

Table 15. Phase I Wafer KLA Repeater Data			
Cumulative Wafer #	KLA Repeater Count	Cumulative Wafer #	KLA Repeater Count
250	88	2012	455
500	149	2512	531
725	162	2761	516
1014	329	3036	529
1289	340	3286	610
1614	481	-	-

During the period between the Nighteagle mask run and the Falcon mask run, significant changes were made to the experimental setup. A tilt in the wafer stage in the SVGL aligner was corrected. Additional mask leveling sites were added and more care was used in mask and wafer handling. No evidence of mask scratches was seen on wafers printed with the Falcon mask. As reported in section 5.5.5, however, a spot was observed on the center of the mask. This spot appeared around wafer #723. This mask also showed significant image placement change as shown in Table 16. The cause of these anomalous results has not yet been determined, but residual hard mask seems to be a possibility.

Table 16. Image Placement Data - Mask 61B-2			
Pre-Expose		Post-Expose	
Mean + 3σ X	Mean + 3σ Y	Mean + 3σ X	Mean + 3σ Y
42nm	53nm	279nm	219nm

Three additional phases of these experiments are underway. A few key changes from the previous procedures were implemented to make them more representative of standard wafer process conditions: [3]

- Phase 1. The first phase will expose 1000 wafers. All will be resist coated and exposed at 20μm gap.
- Phase 2. The second phase will expose 500 wafers. All will be resist coated with full alignment under actual lot exposure conditions at 20μm gap.
- Phase 3. The third phase will be 100 wafers under the same conditions as phase 1 but at 15μm gap.

[3] J. Leavey, ALF X-ray Mask Usage Phase 1 Milestone 7 report to Sematech 8/24/98, and Phase 3 Milestone 9.

The mask selected for phase 1 was a low absorber coverage Nighteagle, the same pattern used in 1997. The mask image size was measured five times over four days and the results are presented in Table 17 on page 72. Image placement was measured five times over 10 days and is presented in Table 18 on page 72. This mask was also measured for membrane flatness three times over a four day period. KLA SEMSpec defect measurement of the mask was performed four times over five days. The total of classified counts was relatively stable and the mask was deemed fit to use for the tests.

Table 17. Mask Pre-expose Image Size - Mean (3σ)

Site	4/30/98	5/1/98	5/2/98	5/2/98	5/3/98	Average
SRAM 118 sites	187nm (19nm)	178nm (17nm)	176nm (17nm)	175nm (16nm)	177nm	

Table 18. Mask Pre-expose Image Placement - Mean (3σ)

Direction	4/25/98	4/25/98	4/30/98	5/1/98	5/4/98
X	47nm	47nm	45nm	45nm	43m
Y	75nm	75nm	75nm	76nm	77m

For this test the resist will be UV2HS with SVG puddle development. As before, selected wafers will be gold coated and shipped to the MMD for SEMSpec inspection.

The mask chosen for the second and third phases of this work is also a low absorber coverage Nighteagle. The mask parameters of interest for this phase were measured multiple times and the measurements were very consistent. The results are presented in Table 19 and Table 20. Resist UV2HS will also be used for this phase with similar processing and measurements as phase 1.

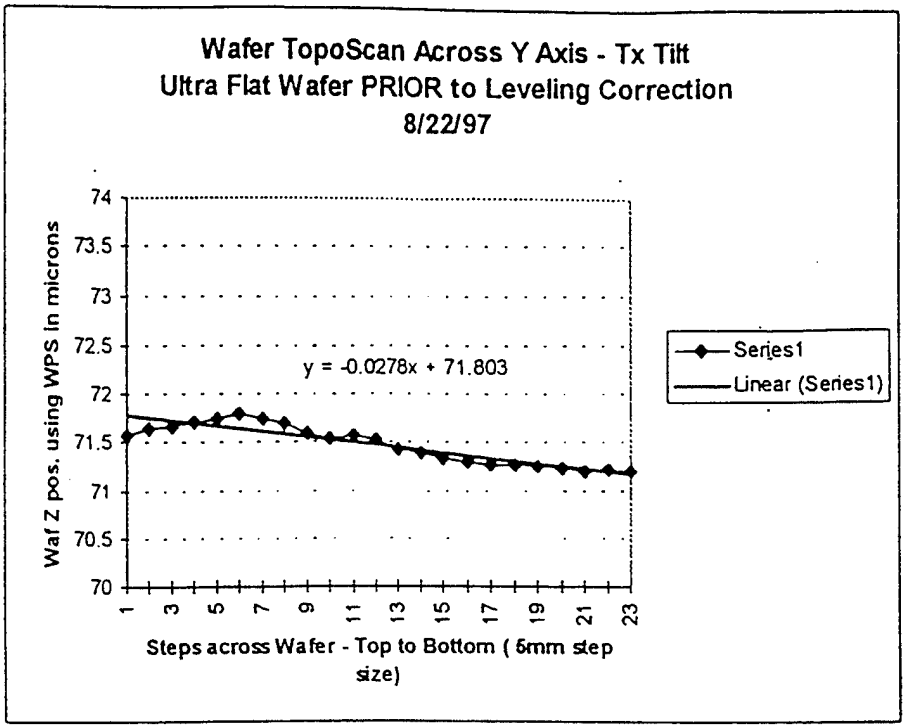
Table 19. Mask Pre-expose Image Size - Mean (3σ)

Site	5/30/98
SRAM 118 sites	172nm (8nm)

Table 20. Mask Pre-expose Image Placement - Mean (3σ)

Direction	6/10/98
X 73nm	Y 35nm

The conclusion, based on these results, is that x-ray masks are capable of withstanding manufacturing quantities of wafer passes, and that the light source and stepper can perform well for extended periods.



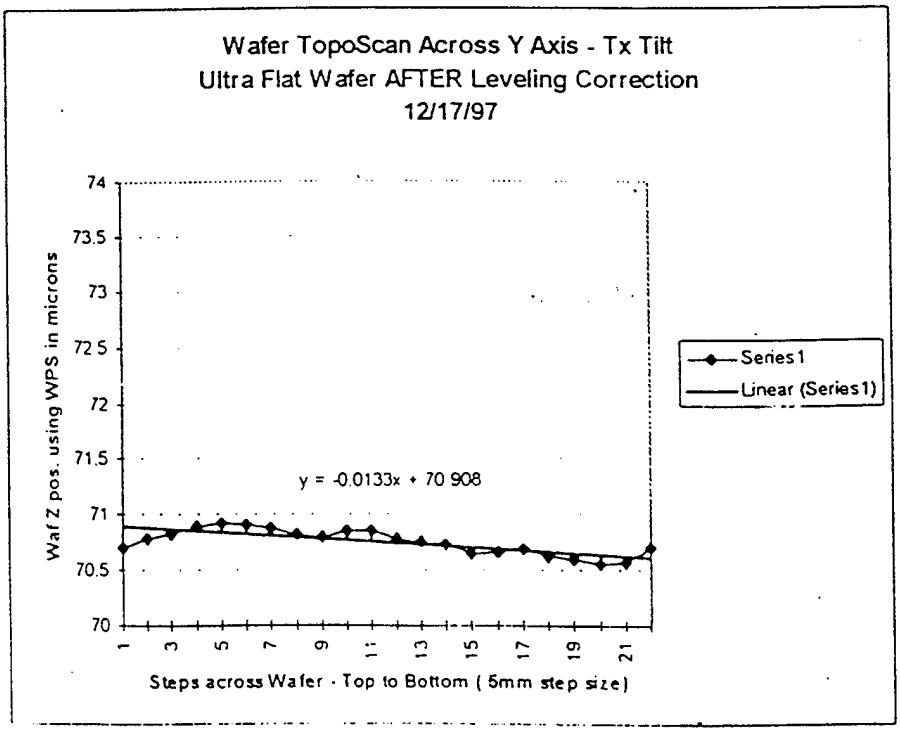
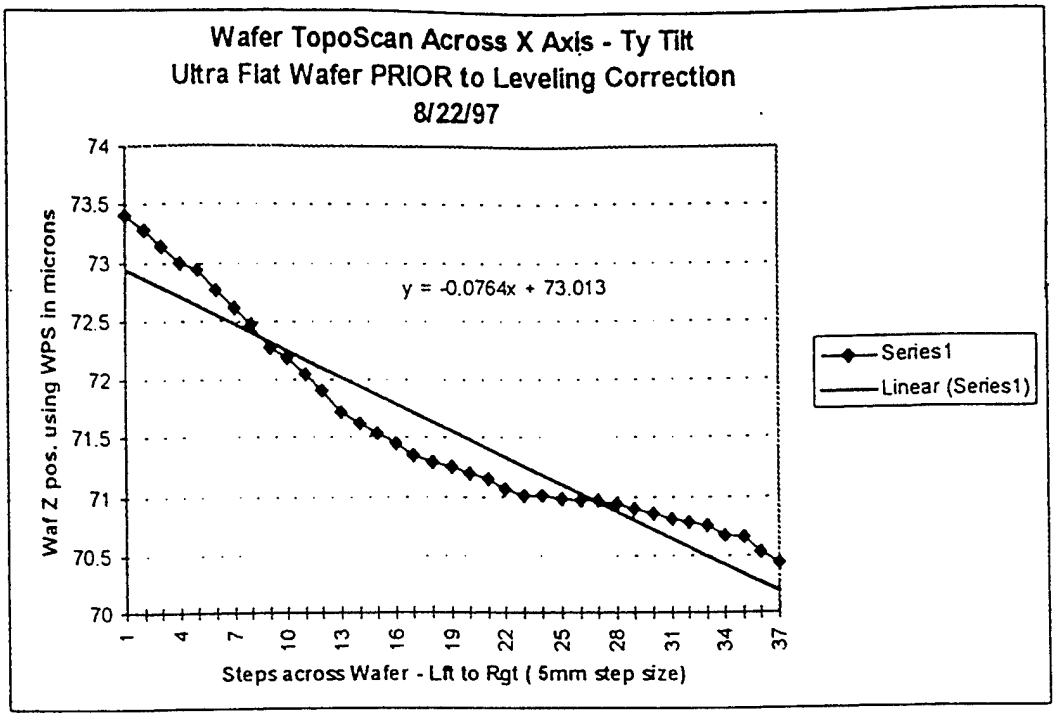


Figure 21. Wafer Tilt Before and After Correction (Y Axis)



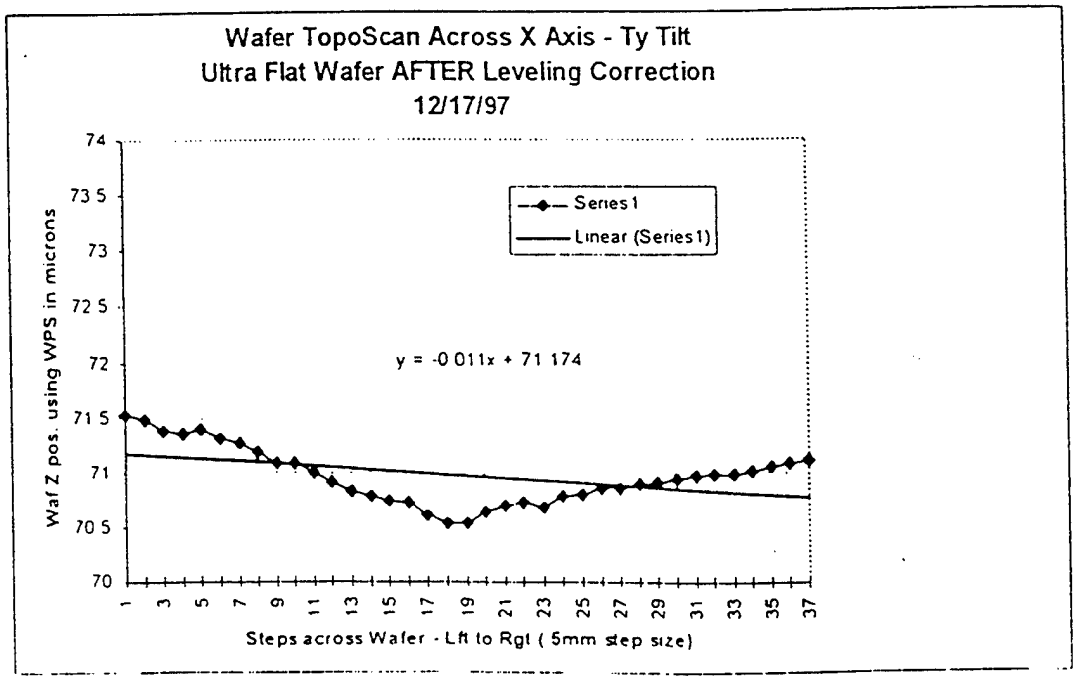


Figure 22. Wafer Tilt Before and After Correction (X Axis)

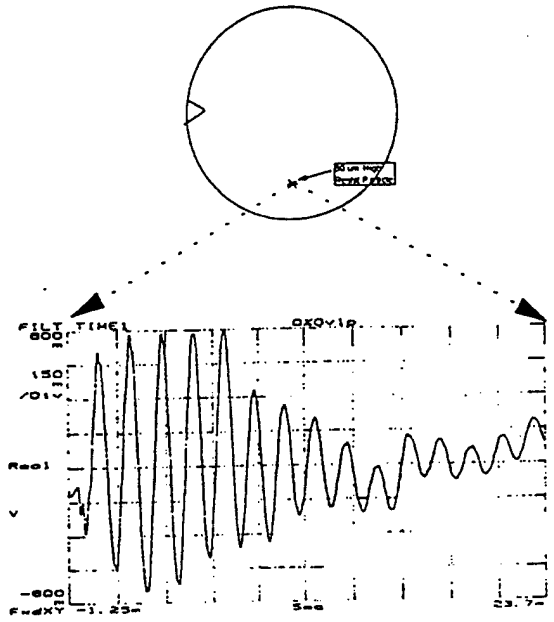


Figure 23. PDS - In Situ Particle Detection

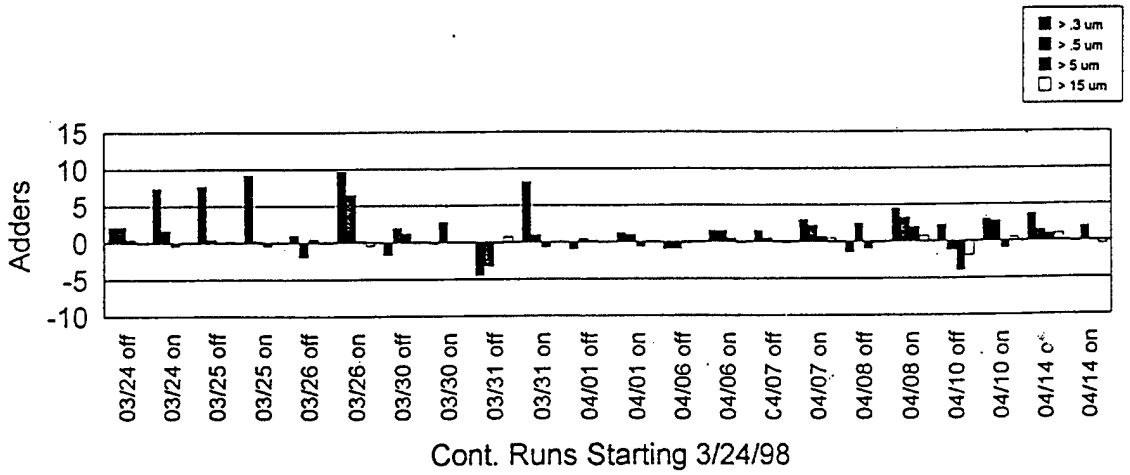


Figure 24. SVGL Contamination, PDS Off/On

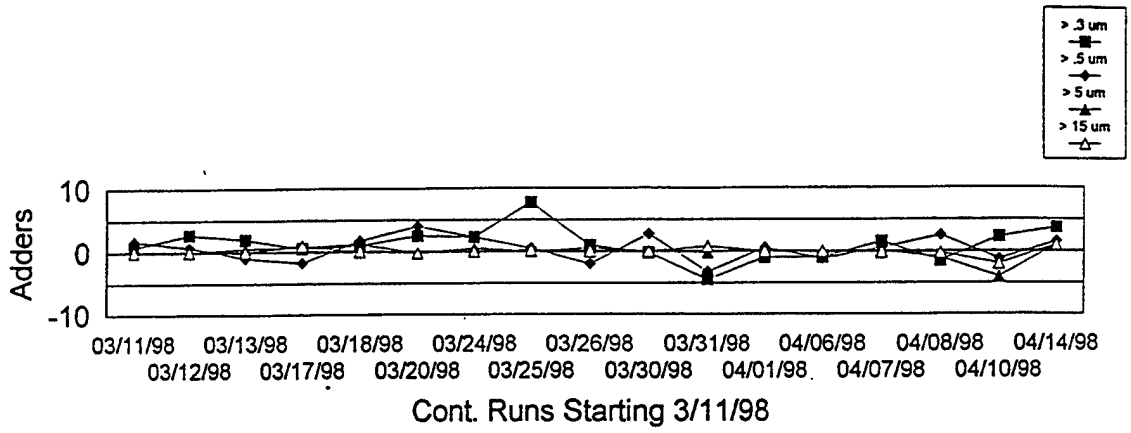


Figure 25. SVGL Contamination Net Adders, PDS Off Only

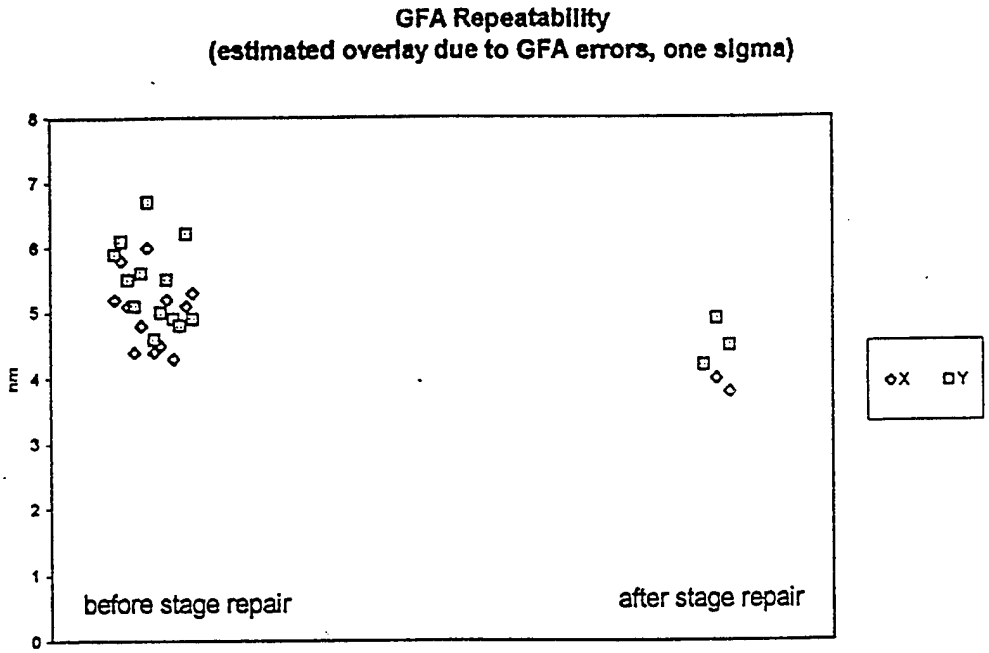


Figure 26. DALP Aligner Wafer Global Fine Alignment Repeatability Test Results

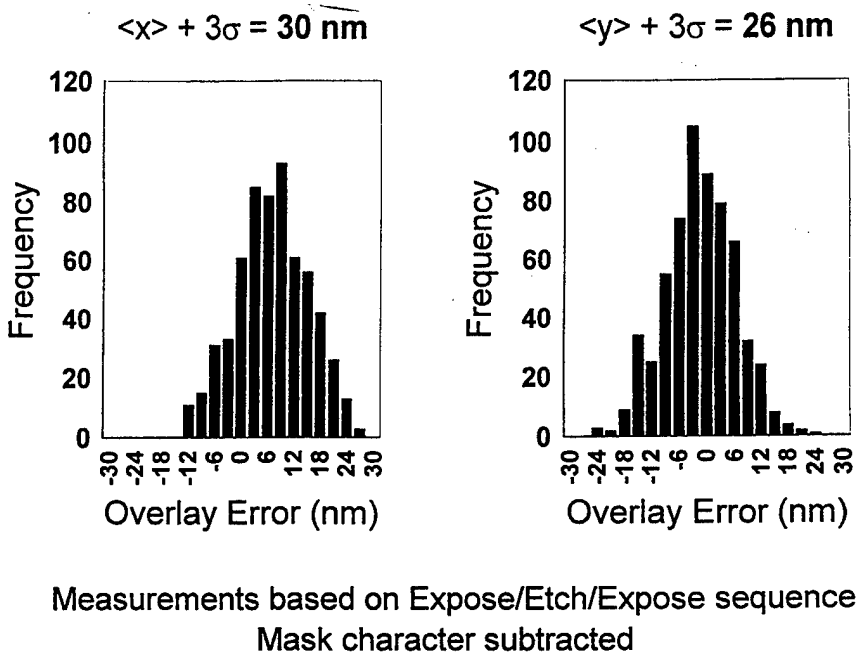


Figure 27. SVGL Aligner Overlay, Tool to itself

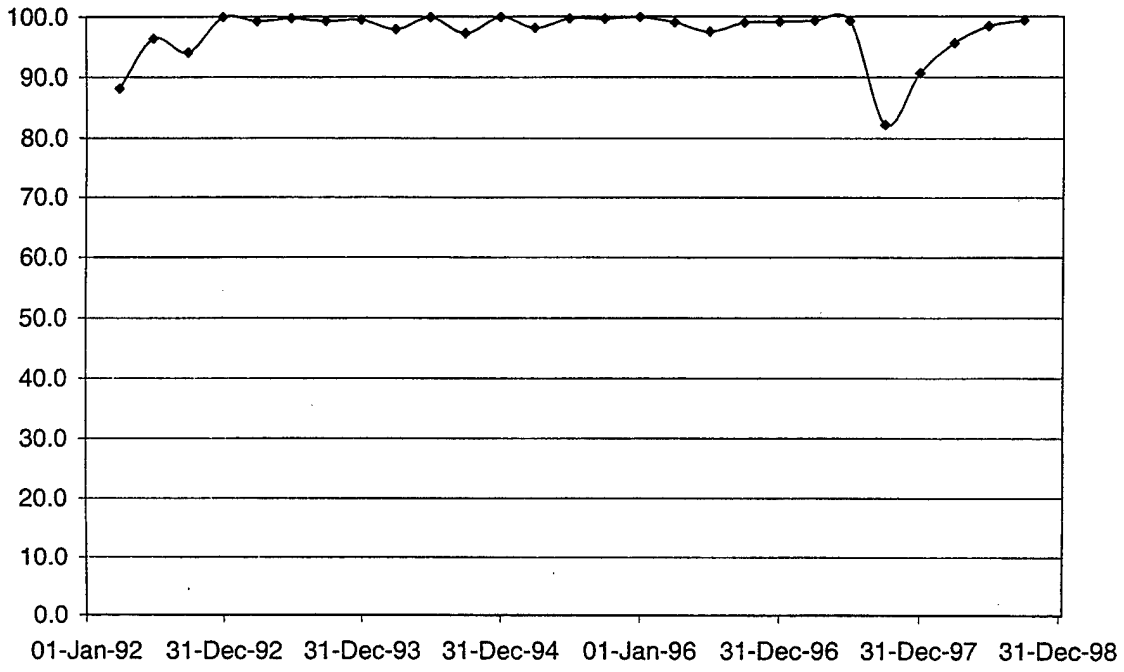


Figure 28. Helios Availability

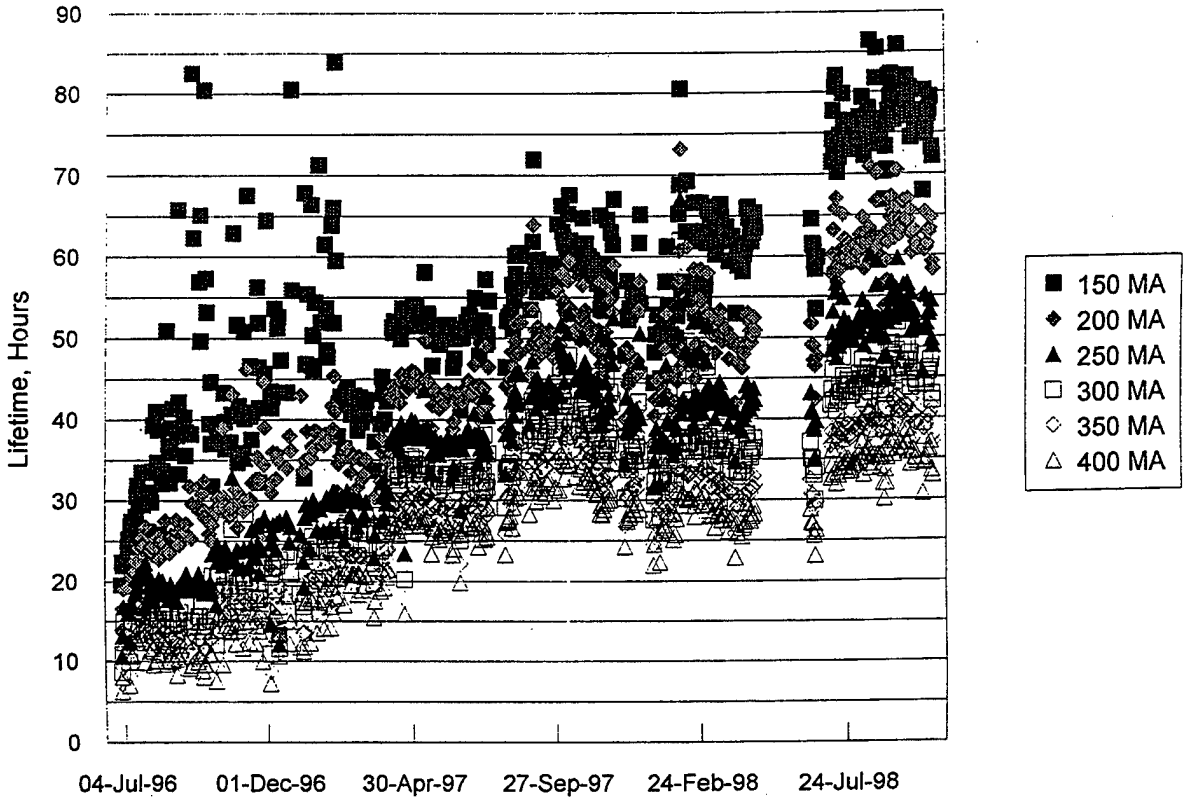


Figure 29. Lifetime at Various Beam Currents

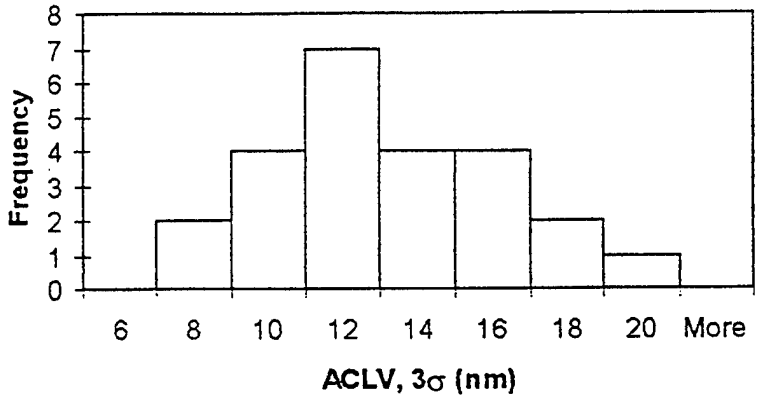


Figure 30. ACLV on Wafer (resist prints). 24 chips measured. N = 15 per chip (Mask #55A-6).

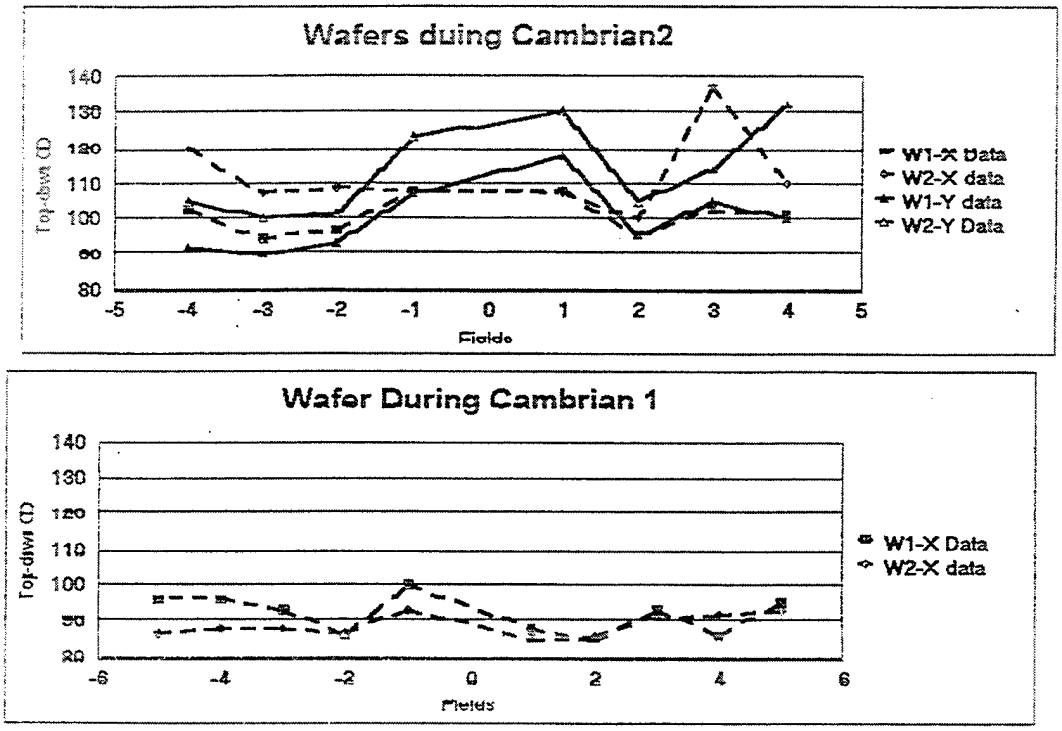


Figure 31. Wafers During Cambrian

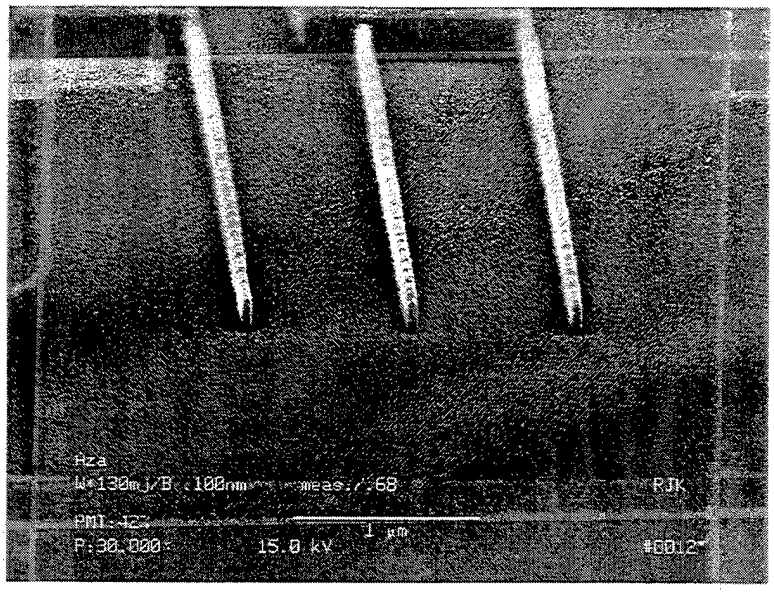


Figure 32. 70nm Isolated Gates

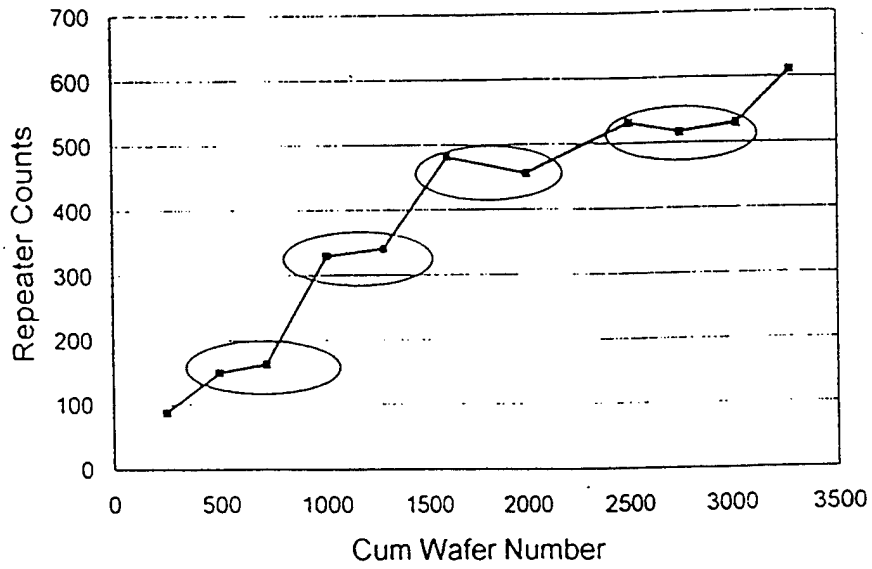


Figure 33. KLA Repeaters versus Wafer Number

6.0 Technology Acquisition (Task 8)

Task Objective: Evaluate the applicability and utility of new technology and tools to use in the MMD pilot production lines with the objective of improving production efficiency, quality, and profitability, and achieving progressively smaller mask feature sizes.

Work is ongoing with HOYA to improve the quantity and quality of SiC substrate deliveries. Film stress control of both TaSi and SiON depositions has allowed excellent image placement results. Installation of a new annealing tool and a new stress measurement tool were completed this quarter. Alternate materials being evaluated during this reporting period include diamond substrates supplied by Crystallume, silicon carbide films supplied by NTT-AT, Ta_4B (absorber), TaGe (absorber), CrN (hard mask), and Cr (hard mask) deposited in the MMD. The DOE (Design of Experiments) for the UVIII TaSi etch process was also completed during this reporting period.

6.1 Silicon Carbide Status

HOYA shipments in 1998 have averaged 51 parts per month. The average post-clean defect density is 2.35 defects per cm^2, and 2.42 defects per cm^2, including ten wafers from the new CVD deposition system. For all films, the thickness averaged 1.95μm with a uniformity of 0.899μm (3σ).

Several attempts were made to etch wafers into membranes using KOH. The continued presence of blisters, however, prevents the use of this membrane etch formation process. The ethanolamine process works well and has been providing blister-free membranes.

Very fine scratches have been detected in the films when inspected on the Tencor inspection system. The scratches appear to be at the threshold of detection when inspecting the silicon carbide films. These have not been a problem, but film quality of every lot continues to be monitored.

Since the previous reporting period, HOYA has shipped an additional 310 films, bringing the total to 580 for the year. The progression of wafers sent and other measurement data are shown in Figure 34 on page 104.

During the fourth quarter, HOYA supplied thirty films on Rokko (a Japanese supplier) wafers for engineering evaluations. The Rokko wafers were sorted by HOYA for defect levels and classified as first or second quality. They were inspected on the Tencor tool in the MMD and found to have an average of 0.078 and 0.181 defects per cm^2, respectively. MEMC (Electronic Materials Inc.) wafers supplied by the MMD, processed in the same lot of first and second quality, averaged 0.068 and 0.097 defects per cm^2, respectively. KLA data for SiC film on Rokko wafers was 0.28 defects

per cm^2 compared to MMD-supplied wafers from MEMC with 0.65 defects per cm^2. This apparent contradiction with the Tencor data is not unusual because the KLA inspects a small area and excludes the outer area. The larger sample size from Tencor shows higher FM levels on Rokko wafers. When measured on a Tropel for wafer flatness, Rokko wafers averaged 12μm of warpage versus MEMC/MMD-supplied wafers, with 8μm of warpage. Film thickness and uniformity were similar. MEMC wafers had a film thickness of 1.97μm with a 1σ of 0.026μm, and Rokko wafers were 1.96μm with a 1σ of 0.028μm. These are from nine sites measured across a 50×50mm^2 area. The MMD has requested that HOYA continue to use MEMC-supplied wafers.

On 01 October the MMD received ten wafers deposited by HOYA on their new CVD (chemical vapor deposition) system. The as-received foreign material level of 6.9 defects per cm^2 is about twice the defect level of the older deposition system. The post-clean defect density levels are about four times those of the current tool (see Figure 34 on page 104). All lot data is post clean. The ten-wafer film thickness averaged 1.92μm with a 1σ of 0.0028μm (Figure 35 on page 105). The wafer warpage measured 12.1μm. The hydrogen content of the film was about 0.2 atomic percent which is below the detection limit of the hydrogen forward scattering technique used for the measurement. KLA data provided a defect density of 0.43 defects/cm^2. "Blob" defects were found during KLA inspection. Surface roughness measured 0.159nm RMS.

New CVD films exhibit the backside blister phenomena when etched in KOH. The new CVD films etch well in ethanolamine galic acid, the current membrane etch process. An additional 50 films were received on 11 November; incoming visual inspection rejected 30 for edge damage. Hoya is aware of this problem and is working to resolve it. Subsequent shipments are from Hoya's older deposition system.

6.2 HOYA

MMD and Hoya personnel met at the MMD in April and October of 1998 and at Hoya during April of 1998 to continue discussions regarding production levels and defect reduction. It was agreed that MMD will continue to supply silicon wafers for silicon carbide deposition until HOYA demonstrates that their supplier can provide low warpage, clean silicon wafers with reduced defects. As reported in section 6.1, evaluations to date have shown that silicon carbide deposited on wafers provided by Hoya's silicon suppliers have equal or marginally better defect levels and the wafers are significantly more warped than MEMC-supplied wafers. Hoya continues to have the MEMC silicon wafers polished prior to silicon carbide deposition.

During May and June, Hoya experienced problems with their old CVD system and a complete reconditioning was required to bring the system back up. They also experienced difficulties with the implementation of their new CVD system which was supposed to solve defect problems and significantly increase capacity. As a result, 1998

shipments were significantly below the 120 wafers/month expected at the beginning of the year. Actual shipments totaled 580 wafers as of 01 December.

Hoya has committed to providing 120 wafers/month in 1999 with expectations for higher quality in stress, defect levels and thickness control.

6.3 Advanced/Alternate Materials

6.3.1 Alternate Membrane Materials

6.3.1.1 Crystallume Diamond Films

In 1994, SiC and diamond were pursued as alternate membrane materials (under the DALP X-ray contract, N00019-91-C-0207). It was determined that SiC, a mature technology, produced better results than the diamond films from Crystallume. (Crystallume, located in Santa Clara, California, is a division of Advanced Refractory Technologies, Inc. and specializes in CVD diamond products.) Purchase orders were placed with Crystallume in 1998 for 2μm thick CVD diamond films for further evaluation.

The initial purchase order for 50 diamond films was placed with Crystallume with the understanding that some development work would be required to achieve diamond films that met specification. The order was completed in August and samples were evaluated for various material properties. The results of the evaluation work for each of the relevant parameters is discussed below in detail.

The first set of diamond films was unpolished, but it was clear from the results that Crystallume had made considerable progress in establishing a process with controlled film thickness and stress. Evaluation of these diamond films revealed the need for a robust backside protection layer for membrane etch. Crystallume agreed to provide a diamond layer on the backside of the wafer for this purpose. A second purchase order was placed in September for 150 polished diamond films; 71 have been received as of 12 August. Crystallume plans to ship the remaining 79 diamond films by the end of 1998.

Film thickness measurements for the first set of unpolished diamond samples are shown in Figure 36 on page 105. For the most part, Crystallume has good control of film thickness with values generally averaging between 1.8 and 2.3μm. The plot also shows how the thickness varied with the first set of samples as the supplier was working to establish a process. The film thickness uniformity was also measured on several samples in a 50×50mm area. The diamond film thicknesses varied by up to 0.6μm within a wafer. However, the film thickness uniformity has improved to less than 10% on the latter samples. Film thickness measurements performed on polished wafers are shown in Figure 37 on page 106. Thicknesses average between 1.8 and 2.0μm, with some samples falling outside of that range. It is believed that as

Crystallume is working to establish a polishing process, some wafers are polished more aggressively than others resulting in film loss. The film thickness uniformity is acceptable, with some samples measuring less than 2%.

Optical transmission measurements were performed on a number of etched diamond membranes; the results are shown in Figure 38 on page 106. Initial diamond film transmission was low (<20%). Crystallume recognized this issue and altered the process to improve the transmission. Transmission of a film built by Crystallume with process improvement is shown in Figure 39 on page 107. The transmission of the polished diamond films should be higher than unpolished films because the rough surfaces of the unpolished films are known to cause significant light scattering. Figure 39 also shows the transmission for different locations on the membrane and indicates the level of non-uniformity in some samples. This should also improve with polishing. Polished diamond films are currently being processed in the MMD for membrane transmission measurements.

As mentioned above, the first diamond film order was for unpolished substrates. Crystallume has optimized their deposition process to achieve a relatively smooth (10-15nm Ra) as-deposited film. Roughness data measured on several samples is summarized in Figure 40 on page 107. A typical surface profile, as measured by AFM, is shown in Figure 41 on page 108. However, in order to make high quality x-ray masks, polished substrates are required. Ideally, the surface roughness should be below 1.0nm Ra, but since diamond is extremely difficult to polish, roughness numbers below 5.0nm Ra are considered acceptable initially. (It should be noted for comparison purposes that unpolished SiC has roughness on the order of 12.0nm Ra, which necessitates polishing as well.)

In August, Crystallume acquired a new diamond polishing tool in order to achieve the target roughness specifications. Preliminary tests using a prototype of this polishing tool showed that the surface quality of polished films looked promising, with roughness below 1.0nm Ra as measured in a localized area. A number of the polished samples received recently were measured for surface roughness by AFM. The Z range is a measure of the maximum low to high surface profile. RMS is the "root mean square" of the area measured and the Ra is the average value of the area measured. The AFM data from polished samples is shown in Table 21 on page 85.

The average of the Z range is 55.1nm, RMS averaged 6.4nm and Ra 4.7nm. The polished parts are roughly three times smoother than the unpolished parts; however, there are still large divets as represented by the Z range measurements. An example AFM of polished diamond is shown in Figure 42 on page 109.

Table 21. AFM Data of Polished Diamond Samples				
P/N	Location	Z range (nm)	RMS (nm)	Ra (nm)
E4C3	Edge	52	4	2.3
E4C3	Center	53.5	4.6	3.2
C1D2	Edge	47.2	5.2	3.6
C1D2	Center	78.1	12	9.8
C2A3	Edge	54.4	6.3	4.7
C2A3	Center	39.7	4	2.7
CRY-59	Edge	71.5	10.5	8.6
CRY-59	Center	44.6	4.4	3

Film stress measurements were performed on diamond films to evaluate the films, as well as to help Crystallume establish a deposition process that achieves the target of 100MPa tensile stress. A summary of the stress for diamond films is given in Figure 43 on page 110. As the process was being established, the film stress varied somewhat. However, once a process was established, the control of film stress was good, as seen by the last set of samples which are very close to the target 100MPa stress. The Tencor Flexis 5510, which measures induced wafer bow, was used for the film stress measurements. The stress of several diamond membranes was also checked using resonance frequency measurements and the numbers were found to be in good agreement with the Flexis measurements. Film stress uniformity is also acceptable and generally less then 20MPa 3σ within a 90mm diameter. It is difficult to measure film stress on the polished samples received to date because they have diamond on both sides. Film stress measured on one polished sample was 45.6MPa.

The defect density of the initial group of diamond films was difficult to measure since the films were not polished. Measurements show defect densities greater than 100 defects per cm^2 at sizes of $0.5\mu m$ and larger, but most of these defects could be attributed to roughness. The distribution of defects is consistent with the diamond film uniformity, with a much larger density towards the outside of the wafer. Some dark granular defects are visible under the microscope, and experiments are being performed to determine whether the defects will print under x-ray irradiation.

A more extensive defect analysis is being performed on the second group of higher quality polished diamond samples. Defects measured by Tencor 6420 with a $1.0\mu m$ threshold and a 10mm edge exclusion (to avoid unpolished areas), averaged 35.8 defects per cm^2 and 16.3 defects per cm^2 for two lots in process. KLA inspection of one Nighteagle mask mask averaged 220.6 defects per cm^2. Some of these defects can be seen in Figure 44 on page 111. They are large, embedded defects in the diamond film. Crystallume has started some processing in a clean room environment, but not to ultimate levels. The MMD will monitor defect levels continuously and provide the data to Crystallume.

Some preliminary radiation damage measurements have been performed on Crystallume diamond membrane samples. This involved measuring the membrane stress using a resonance frequency measurement before and after x-ray irradiation. Any differences in membrane stress would be an indication that some material damage was occurring. To obtain a quick result, accelerated radiation was performed on two diamond samples to a dose of 60kJ/cm^2, and no changes in the resonant frequencies were observed. The irradiated area was relatively large (approximately 20% of the total membrane area), possibly indicating no change in the membrane stress. (The resolution of the resonance frequency measurement is such that changes in membrane stress of less than 1MPa would be detectable.) This is initial evidence that the diamond films do not suffer from any gross radiation damage. More extensive testing is currently being performed on diamond x-ray masks built specifically for accelerated radiation damage testing.

A 50×50mm, 2μm thick membrane was tested for x-ray transmission in the ALF facility. The measured transmission of the diamond membrane was 73% taken at five membrane locations (compared to 63% typical for 2μm thick SiC). The data range was 71.8% to 73.9% for the five samples. A scanning densitometer trace (30μm scan spot diameter) was taken and indicates that the rms noise for transmitted dose is indistinguishable from that of the radiachromic film - about 1% peak-to-valley or about 0.7% rms. This was the highest mask material transmission ever measured at ALF, and the rms noise was as good as SiC and better than the B:Si samples previously tested. The membrane transmission was also rechecked after irradiating with a dose of 205kJ/cm^2, and no change was observed. This is further evidence that the diamond material does not suffer any gross radiation damage that would result in a transmission change.

A high degree of crystallinity is desirable for these types of films because of the strength and resistance to radiation damage. The crystal structure of the Crystallume diamond samples was determined by transmission electron microscopy (TEM) and selected area electron diffraction (SAD) analysis. A TEM image of the diamond material is shown in Figure 45 (a). The grain size throughout the film appears to be less than 10nm. The electron diffraction pattern is shown in Figure 45 (b), where each ring represents diffraction from a specific crystal plane. The measured interplanar spacings agree very well with the calculated interplanar spacings for a crystalline diamond sample. The only diffraction ring that is absent is from the {200} plane. However, based on kinematical scattering theory, the {200} diffraction is a forbidden reflection in the diamond cubic structure, but is present due to double diffraction in polycrystalline diamond samples with grain sizes larger than 10nm. Since the grain size appears to be below 10nm in this case, the {200} diffraction ring produced by double diffraction should indeed be absent. The SAD pattern also exhibited no reflections that could be attributed to graphite. This implies that if there is any graphitic component present in the sample, it is below the detection limit of the analysis.

The first set of unpolished diamond wafers from Crystallume was fabricated with no backside protective layer. It was necessary for MMD to deposit a layer on the back to protect the silicon during the membrane etch process. Unfortunately, the diamond deposition at Crystallume also resulted in some backside defect problems. By altering the deposition process, Crystallume was able to improve these defect problems slightly. Membranes were initially fabricated in the MMD by covering the backside with a protective sandwich consisting of a 1μm layer of PECVD (plasma enhanced chemical vapor deposition) silicon nitride, a layer of 25nm thick chromium, and another 1μm thick silicon nitride. KOH was used to build some membranes that were used for diamond characterization; however, etch yield was low, with several samples exhibiting backside blister problems.

Evaluation of this first set of diamond films revealed the need for a more robust backside protection layer and/or the elimination of any backside defects. Crystallume agreed to provide a diamond layer on the backside of the wafer for this purpose. The backside diamond films are unpolished and range between 0.7 to 1.0μm in thickness. A diamond etch process developed on the AME tool will be used to define the membrane area. This etch consists of a high power, 100% O_2 plasma process; the diamond etch rate is roughly 300nm/minute. High quality membranes have been fabricated with the diamond film protecting the backside. Unfortunately, the backside diamond film inhibits anodic bonding between the Pyrex ring and the wafer. A UV-activated adhesive is currently being used to bond diamond wafers to rings and to allow the fabrication of diamond x-ray masks (see section 4.1.6).

A process for fabricating x-ray masks with diamond film substrates is currently in place in the MMD. The new lots of polished diamond samples are currently being processed and deposited with the Cr/TaSi/SiON refractory stack. These samples will then be used to fabricate Falcon and Nighteagle masks and check image size, image placement and final mask defect performance.

6.3.1.2 NTT-AT SiC and Diamond Films

NTT-AT, a Japanese research company and subsidiary of NTT, announced early in 1998 that they had the capability to deposit SiC and diamond films for x-ray mask blanks. Since NTT-AT is not a manufacturing facility, they currently have only limited capacity for producing x-ray mask blanks. Nevertheless, additional x-ray mask substrates may be required by MMD to complement the supply of SiC from Hoya. For evaluation purposes, a purchase order for 20 SiC and 10 diamond samples from NTT-AT was placed in June of 1998. Sixty double-side polished wafers were provided by MMD for the x-ray mask blanks. The order was initially delayed because of some work required to allow handling of 4-inch substrates. The standard deposition and polishing processes used by NTT-AT are optimized for 3-inch substrates, consistent with a format for x-ray masks commonly used in Japan.

The diamond samples from NTT-AT have not yet been received. As mentioned above the deposition and polishing processes are optimized for 3-inch substrates. Since

diamond film fabrication is even more difficult than SiC, considerable effort is required to obtain good quality (uniform and polished) films on 4-inch substrates.

Twenty SiC samples were received from NTT-AT on 07 August and have been characterized and evaluated. The data is summarized in Table 22 on page 89 with the lot average in the last table row. Each wafer was measured for incoming foreign material and foreign material levels after a clean. The initial average was 54.4 defects per cm^2. The inspection also includes an area count which measures large defects. The initial average area count was 114. After a megasonics clean in sulfuric acid and hydrogen peroxide, followed by a hydrochloric acid, ammonium hydroxide and hydrogen peroxide (RCA-A and RCA-B) clean, the films were reinspected. The post-clean average defect numbers were 8.6 and 43.6 for the defects per cm^2 and the area counts, respectively. The cleans removed greater than 50% of the surface foreign material. The NTT-AT SiC Defect Data graph Figure 46 on page 113 shows the amount of change from cleaning.

Table 22. NTT-AT Silicon Carbide Evaluation Summary

Date	Samples received	Incoming FM	Transmission optical HI MEAN LO	flatness: overall, membrane	thickness and uniformity final	KLA	Comments
units	LOT(qty)	defx/cm²	%@=610nm	(μm)	(μm)	(defx/cm²)	
Target/ Spec		<1 of .5μ <5 of .2μ>	>50	<1.0	2.0±0.1 0.05	10 rprbl 0 non	
8/10/98	wafer 1 (16Y0002)	(62.5/128)		26.25	2.37 .041		backside chuck marks RMS=0.307nm Ra=0.218nm
8/10/98	wafer 2 (16Y0003)	(36.5/61) 6.57/34		29.11	2.34 .052		backside chuck marks
8/10/98	wafer 3 (16Y0004)	(69.1/48) 27.2/18	39	21.06	2.32 .034	359.9	backside chuck marks
8/10/98	wafer 4 (16Y0005)	(17.8/65) 3.78/13		14.93	2.29 .017		backside chuck marks
8/10/98	wafer 5 (16Y0007)	(16.8/137) 4.99/88		15.86	2.26 .024		backside chuck marks
8/10/98	wafer 6 (16Y0008)	(18.9/114) 4.12/76		25.24	2.31 .023		backside chuck marks
8/10/98	wafer 7 (16Y0010)	(38.0/54) 5.94/39		11.03	2.26 .024		backside chuck marks
8/10/98	wafer 8 (16Y0011)	(64.9/168) 11.7/29		12.90	2.36 .056		backside chuck marks
8/10/98	wafer 9 (16Y0014)	(96.7/403) 8.00/30		13.08	2.34 .092		backside chuck marks
8/10/98	wafer 10 (16Y0017)	(37.2/125) 7.62/71		16.85	2.21 .039		backside chuck marks

Table 23. NTT-AT Silicon Carbide Evaluation Summary

Date	Samples received	Incoming FM	Transmission optical HI MEAN LO	flatness: overall, membrane	thickness and uniformity final	KLA	Comments
8/10/98	wafer 11 (16Y0018)	(114/153) 17.2/69		35.21	2.23 .032		backside chuck marks
8/10/98	wafer 12 16Y0019)	(112/203) 8.93/94		8.48	2.29 .029		backside chuck marks
8/10/98	wafer 13 (16Y0020)	(63.7/131) 9.81/68		19.22	2.18 .023		backside chuck marks
8/10/98	wafer 14 (16Y0021)	(38.2/83) 4.27/44	38	7.29	2.17 .038		backside chuck marks
8/10/98	wafer 15 (16Y0022)	(78.9/110) 8.86/26		11.51	2.17 .032		backside chuck marks
8/10/98	wafer 16 (16Y0023)	(13.8/48) 2.78/20		30.62	2.19 .030		backside chuck marks
8/10/98	wafer 17 (16Y0024)	(23.5/33) 2.85/19		11.00	2.30 .036	23.8	backside chuck marks
8/10/98	wafer 18 (16Y0025)	(89.2/64) 8.49/25		8.76	2.36 .024		backside chuck marks
8/10/98	wafer 19 (16Y0027)	(41.8/82) 6.97/47		16.83	2.23 .031		backside chuck marks
8/10/98	wafer 20 (16Y0031)	(53.9/67) 13.4/19		15.74	2.33 .062		backside chuck marks
8/10/98	lot mean	(54.4/114) 8.6/43.6	38.5	17.55	2.28 .037		backside chuck marks

Note: (as shipped defx)

These films were also inspected on the KLA SEMSpec for defects. The two wafers inspected were found to have 23.8 and 359.9 defects per cm^2. The inspection found foreign material, some embedded defects, and also some holes in the film.

The wafers were measured for flatness and the average post deposition warpage was 17.6μm. The stress measured 271.39MPa on a Tencor Flexis. The front side SiC film was stripped to obtain the measurement from wafer bow difference. This is only an approximate method of measuring the SiC film stress, but it indicates that the film stress is in the 300MPa range.

A small spot spectrophotometer (SSS) tool is used to measure film thickness, reflectivity and membrane transmission. The average film thickness across a central 50×50mm^2 area is 2.28μm with 0.037μm standard deviation. Uniformity from nine sites is shown in Figure 47 on page 113. Measurement tool offset could explain the delta between the MMD tool and the NTT-AT tool. The film reflectivity from one sample is plotted, as well as the transmission of two membranes. The average membrane transmission at 610nm is approximately 40%. This data can also be seen in Figure 48 on page 114 comparing two NTT-AT samples with a HOYA sample.

One NTT-AT sample was delivered to the IBM analytical laboratory for Atomic Force Microscopy. The films are very smooth, but there are small scratches seen in the surface. The surface roughness of the areas measured averaged 0.307nm RMS and 0.218nm Ra. The wafers also have backside chuck marks.

The analytical laboratory also ran an NTT-AT SiC sample through a technique known as hydrogen forward scattering, which is similar to Rutherford back scattering but uses a proton instead of an electron source. The technique inspects for hydrogen content. The sample inspected was found to have hydrogen in amounts below the detection limits of the system or 0.2 atomic percent. This is a good preliminary indication that radiation damage in these films will be small.

6.3.2 Alternate Absorber Materials

6.3.2.1 Hoya Tantalum Boride (Ta4B) Absorber

Several masks were processed in late 1997 and early 1998 with a SiC/Hoya Ta_4B/Motorola SiON stack. The goal was to evaluate the use of Ta_4B as an absorber material. The etch characteristics of the Ta_4B were impressive, with a similar etch process as for TaSi, and down to 0.1μm features on benchmark patterns achieved. Six logic testsite masks were also made with Ta_4B as the absorber. The final image size on these masks averaged 150nm (160 nominal) with 3σ less than 20nm. Placement data was also measured on these parts. There was a magnification character observed on the parts that may be attributable to difficulty grounding the parts on EL-4+ P0 (there was no Cr etch stop). In any case, a PSE was built, and final image placement on Ta_4B parts with that PSE averaged 40-50nm 3σ. These numbers were comparable to TaSi logic testsite masks processed during the same time period. KLA

defect data from a limited number of parts indicates that most defects during that period were e-beam-related rather than stack-related.

A second set of SiC substrates with Ta_4B absorber were received from Hoya in late 1997. These samples also contained a CrN etch stop. Tencor defect analysis indicated similar levels of defects as the current MMD Cr/TaSi stack. The SiC/CrN/Ta_4B stack was also tested for radiation damage; none was found. Several of these parts, with a CrN etch stop, were made into Falcon masks (with an SiON hard mask) and processed through the line. The etch quality of these masks was equally impressive as the previous results (with no etch stop), and 100nm etched images were achieved as shown in Figure 49 on page 114. A magnification character was also observed in the image placement distortion of these masks, but no PSE was built to try to compensate. The measurement data from these masks is summarized in Table 23. The film stress on these samples could not be measured because the samples were as-deposited by Hoya. The unknown Ta_4B stress may have been contributing to the strange image placement results.

Table 23. Ta4B Final Mask Results

Part	Ta_4B Type	Mask Type	Image Size Average	ImageSize 3σ	Image Placement Final	Image Placement BEOL
Ta_4B1	Hoya	Falcon	202	29	N/A	N/A
Ta_4B4	Hoya	Falcon	182	28	187,123	142,70
Ta_4B6	Hoya	Falcon	205	25	110,105	N/A
B29A2	IBM	Falcon	199	23	250,228	283,225
B29D1	IBM	Falcon	199	23	250,228	283,225
B29D3	IBM	Nighteagle	199	23	250,228	283,225

6.3.2.2 IBM Tantalum Boride (Ta4B) Absorber

An initial study of Ta_4B deposition and annealing processes was completed at IBM Yorktown in 2Q98. Based on these experiments, it was concluded that: 1) compressive as-deposited film stress can be annealed through 0MPa; 2) the change in stress during annealing is a linear function of temperature for as-deposited stresses ranging from -500 to 1200MPa; and 3) the as-deposited stress varies monotonically with pressure (22 to 24mT pressure corresponds to -500 to -100MPa as-deposited stress). In addition, it was apparent that oxygen contamination plays a significant role in film annealing behavior, causing more compressive stress during high temperature annealing above approximately 350°C. This phenomena was much more apparent on films annealed in the Yorktown annealing tool, which has 20ppm oxygen contam-

ination, as compared to films annealed in the MMD tool which has oxygen levels below 5ppm.

In May, the Ta_4B target was installed in the SFI tool and approximately 100 wafers were deposited. As-deposited stress was studied as a function of power and Argon flow. The results of this work are shown in Figure 50 on page 115. In general the as-deposited stress increases (becomes less compressive) as Ar flow is increased. At the same flow conditions, lower power results in higher (less compressive) as-deposited stress. The effects of both anode and *RF* bias were also studied, and the results indicated that the effects were only evident at flows above 10sccm, where they cause more compressive as-deposited stress. Depositing Ta_4B on Cr/B:Si gives less compressive stress than depositing on Si. For example, 5kW, 10sccm gives -380MPa on Si but only -150 to -200MPa on Cr/B:Si.

The annealing character of the SFI Ta_4B films was also studied. Annealing experiments were done on a number of films with as-deposited stresses in the range of -520 to -150MPa. In all cases, stress became less compressive with temperature and the annealing slopes were in the range of 1-2 MPa/°C (depending on initial as-deposited stress). This data is shown in Figure 51 on page 115. After many successive anneals on the same sample, a phenomena is seen on some of the Ta_4B/Cr/B:Si samples, where the films stop annealing and in some cases get more compressive. This may be due to a small amount of oxygen contamination in the annealing furnace or due to material properties of the Ta_4B. However, in all cases it is possible to anneal past zero stress by annealing directly at higher temperatures.

A set of 10 wafers with the Ta_4B/Cr/B:Si stack was annealed to approximately zero stress. These parts were sent on for SiON hard mask deposition and further processing. Because of membrane etch problems, only three of the 10 samples were successfully made into masks. These three parts were processed through the BEOL and measured for image size and image placement. The data is summarized in Table 23 on page 92. Generally, image size performance is good, with etch quality comparable to the Hoya Ta_4B results. The image placement performance of these masks was poor, however. There was a large distortion due to BEOL processing. This movement was isolated to the Ta_4B etch step. Even though the Ta_4B stress was annealed to zero, it appears that there is still some residual stress or some other material property causing the images to move after etch. The image placement distortion is less but still significant on the Nighteagle mask, as compared to the Falcon masks. The source of this distortion will be studied in further detail when a second set of Ta_4B depositions on the SFI tool is performed. It is expected that, when the stress and material properties are optimized, the image placement performance on Ta_4B masks will be as good as current TaSi results.

6.3.2.3 Other Absorbers

NEC and Fujitsu are working on x-ray mask development and have reported good results with other refractory absorbers such as TaGe and TaReGe. In 1998, we have been working closely with researchers at IBM Yorktown in order to establish the capability to deposit other refractory absorber compounds. The first major effort focused on establishing some process learning on Ta_4B absorber, as discussed in Section 6.3.2.2. After the Ta_4B work was completed in the Yorktown deposition tool, a TaGe target was installed. Experiments are now being performed to gain deposition and annealing process learning on TaGe films. Initial results show that the TaGe low-stress deposition regime occurs at a lower pressure than the Ta_4B deposition. This is shown in Figure 52 on page 116.

In addition to the single target sputter tool, a multi-component sputter deposition tool is available in Yorktown. Progress has been made in the last three months in debugging the source of the oxygen contamination in the Yorktown tool. An inductively coupled plasma (ICP) source with a helical resonator has been installed in the Yorktown tool and used to extend the plasma inside the tool to the walls during a plasma clean process. This has been shown to reduce the oxygen contamination problem. This tool can be used for studying other potential multi-component absorber compounds such as TaReGe. Other options include making tile/mosaic targets for the single target sputter tool to allow the deposition of refractory alloys with varying composition.

6.3.2.4 Alternate Hard Mask Materials

Deposition experiments are proceeding in an effort to develop a low-stress, chromium-based, hard mask deposition process. Two films being considered for this are pure chromium and chromium nitride. The SFI deposition system is being used for this development work.

6.3.2.5 Chromium Hard Mask

A number of Cr deposition conditions were run, and it is evident that the film stress can be controlled somewhat with *RF* power. This data is shown in Figure 53 on page 116 for 50nm Cr films deposited directly on Si wafers. It was also discovered during these experiments that for Cr deposition on TaSi, the conditions that yield zero stress are slightly different than for Cr deposition on Si. Subsequent measurements of the Cr film stress showed that the film stress increases with time. Current work is being aimed at understanding the substrate dependence and apparent lack of stability of the Cr film stress. For better stress stability, it may be necessary to operate the process at a lower cathode power. A new power supply for the Cr module of the SFI tool is being considered for this purpose. Deposition studies using a more stable CrN film are also being developed and are described in 6.3.2.6.

Wafers with Cr hard mask films were used to study the etch selectivity of the material under the TaSi etch conditions. This data is shown in the first half of Table 24 on page 95. Under regular TaSi etch conditions for a Falcon pattern (high *RF*), the Cr etch stop and hard mask films both have etch rates around 26nm/minute which gives a selectivity of 11:1. Under low *RF* TaSi etch conditions, this etch rate drops below 16nm/minute, giving a selectivity greater than 19:1.

Table 24. Summary of Absorber Deposition Improvements, 1997 to 1998

	1997	1998	Improvement Factor
Overall Deposition Cycle Time	32 days	4 days	8×
Chromium Defects/cm²	0.7@1μ	<0.3@0.25μ	8×
TaSi Defects/cm²	5@1μ	<3@0.25μ	6×
SiON Defects/cm²	0.5@1μ	<0.9@0.25μ	2×
Wafer-to-Wafer Film Uniformity	Variable	Consistent	-
Image Movement Due to Films	80-100nm	30-40nm	2-3×
Best Achieved Image Placement	35nm	23nm	1.5×

A number of bonded wafers with B:Si/Cr/TaSi/Cr stack were run on the XEPO tool and compared to regular stack for any possible image placement improvement. This data is shown in Table 25 on page 96. The overall raw image placement for single-pass parts was significantly better on the Cr stack as compared to the regular stack bonded wafers. There was also better part-to-part repeatability on the Cr wafers (36nm versus 43nm). This could be due to a better grounding at the EL-4+ P0 tool and/or less backscattering. The difference from average on the Cr bonded wafers was 21nm which is an indication that with a PSE in place, approximately 20nm image placement in resist is achievable. The image placement on bonded wafers with multiple pass writing was also investigated. These parts were written using a PSE established for regular stack parts. The raw image placement for both stacks is comparable; however the difference from average for the Cr bonded wafers is lower at 12nm. An initial PSE specific to the multiple pass Cr bonded wafers was then built. Two Cr-bonded wafers written using this PSE exhibited image placement comparable to but not better than regular stack bonded wafers. Even better placement performance is expected from the Cr-bonded wafers after the PSE is updated.

Table 25. Bonded Wafer Image Placement Data			
	Raw Image Placement (Avg.)	Repeatability	Difference from Average
Reg.Stack BW	70nm	43nm	27nm
Cr Stack BW	52nm	36nm	21nm
Reg.Stack BW MP	22nm*		18.4nm
Cr Stack BW MP	24nm*		12nm
* Multiple pass parts were written using a PSF set up for regular stack parts			

6.3.2.6 Chromium Nitride (CrN) Hard Mask

X-ray mask development work at Hoya in Japan has shown that CrN films have better and more stable stress characteristics than pure Cr films. CrN development work began in the MMD in April of 1998. The as-deposited stress of these films is being studied as a function of cathode power, *RF* power, total flow and Ar:N_2 flow ratio. An experimental DOE of deposition conditions (*RF* power and cathode power) was run to understand the low-stress deposition regime of CrN films on the SFI tool. The results of this DOE are plotted in Figure 54 on page 117. For this study, the Ar and N_2 flows were kept constant at 20 and 10sccm, respectively. In general, the CrN as-deposited stress seems to be well-behaved with higher *RF* power resulting in lower (more compressive) film stress. Higher cathode powers for the same *RF* power result in higher (more tensile) film stress. The results indicate that both compressive and tensile films can be achieved by varying the parameters. CrN depositions on TaSi were also performed. At low *RF* powers, the CrN stress became more compressive than samples on Si at similar conditions. At high *RF* powers, there was less of an observable change.

There also seems to be an initial change in the CrN stress over time. The stress on five samples (CrN on TaSi) was measured 5 minutes after deposition and then again after 12 hours. The stress on all samples became more tensile by an average of 30 MPa. Subsequent measurements have shown that the CrN stress stabilizes within 48 hours after deposition. RBS data has been collected in Yorktown on a number of the CrN samples, indicating the presence of oxygen (O_2). The O_2 level can be estimated to be roughly on the order of 10%, with more O_2 evident in the CrN samples deposited with higher flows. The presence of O_2 in the CrN may be related to the initial change in CrN film stress. In the meantime, other factors will be investigated to see if the CrN can be deposited under slightly different conditions leading to more stable stress and/or no O_2.

An etch rate study of various CrN films under regular TaSi etch conditions was also performed. This data is shown in Table 26 on page 97. A 50nm film deposited at low stress with conditions established from the DOE (Ar:20sccm, N_2:10sccm) was completely removed before the end of a typical two minute etch. The low etch selectivity is most likely due to the combination of Cl_2 and O_2 present in the TaSi etch. In order

to establish a more suitable hard mask film, CrN depositions at different flows and flow ratios were also performed. The data shows that the CrN films that have the lowest etch rates are those deposited at low flows. The Ar:N_2 ratio does not seem to be a factor affecting etch selectivity. For example, a CrN film deposited at Ar:N_2 flows of 6:2 sccm has an etch selectivity to TaSi of 7.7:1. Unfortunately, the CrN film stress is also a function of total flow and becomes more tensile at low flow deposition conditions. Figure 55 on page 117 shows this effect for a constant Ar:N_2 flow ratio. Further work is required to adjust the Ar:N_2 ratio at low flows in order to develop an optimized CrN hard mask film that has good etch selectivity and stress properties. It is also expected that lower flows would yield even higher etch selectivities. The Ar flow controller was too large (100sccm), however, to adequately control flows below 10sccm. This flow controller is being replaced with a 20sccm controller for future, low-flow deposition studies.

Table 26. CrN and Cr film etch selectivity comparison

Cr/CrN Film	Etch Process	Etch Rate	Selectivity
Etch stop Cr	High rf, Cl_2, 0_2	26nm/min.	11.5:1
Hard mask Cr	High rf, Cl_2, 0_2	27nm/min.	11:1
Hard mask Cr	Low rf, Cl_2, 0_2	16nm/min.	>19:111.1
Hard mask Cr	High rf, Cl_2 only	26nm/min.	>111.5:1
CrN, Ar:N_2=20:10	High rf, Cl_2, 0_2	26nm/min.	>11.5:1
CrN, Ar:N_2=20:2	High rf, Cl_2, 0_2	50nm/min.	<6:1
CrN, Ar:N_2=10:2	High rf, Cl_2, 0_2	47nm/min.	6.4:1
CrN, Ar:N_2=6:2	High rf, Cl_2, 0_2	39nm/min.	7.7:1

6.4 Refractory Metal Stack

A Sputtered Films, Inc. Endeavor DC magnetron sputter deposition system was installed in the MMD in October, 1997. Film deposition studies with the new system began in November, 1997 and have continued throughout 1998. This cluster system, as configured for the MMD contains three deposition chambers and utilizes a unique target configuration comprised of two concentric ring cathode targets. Target voltages may be varied independently to adjust film uniformity. Stress in sputter deposited refractory films is usually controlled by varying sputter gas pressure. The Endeavor tool indirectly controls pressure by varying flow. Since pressure is not measured in the deposition mini-environment, flow is a critical parameter with this system. This tool deposits one wafer at a time in a continuous process up to 25 wafers per cassette load. Because the tool is completely different in design from the Motorola deposition system, it was necessary to develop each of the measurement, metal deposition and annealing capabilities at MMD in order to transfer the absorber manufacturing process from Motorola PCRL to the MMD.

Over 725 refractory metal stacks have been fabricated on both silicon carbide and boron-doped silicon substrates. Table 26 provides a summary of improvements for refractory metal deposition processes. Overall deposition time improved dramatically from 32 days to four days due to elimination of shipping time and queue time, and more efficient deposition equipment and processes. Wafer-to-wafer film uniformity has improved across the wafer and through the film.

The MMD process line is operating exclusively with refractory metal film stacks deposited in the MMD; several masks with good image placement have been made. The Endeavor 8600 AT deposition system continues to operate well, providing films exhibiting good film thickness and as-deposited stress uniformities. During the third quarter, 157 absorber stacks were deposited at MMD (42 SiC and 115 B-Si) for use in engineering studies and for shipment to customers.

Compared to data from 1997, chromium defects have been reduced from 0.7 particles/cm^2 at 1000nm sensitivity to 0.3 particles/cm^2 at 250nm, a factor of eight. Tantalum silicon defects decreased from 5 particles/cm^2 at 1000nm sensitivity to 3 particles/cm^2 at 250nm, a factor of 6. Figure 56 on page 118 shows the defect reduction progress of tantalum silicon films deposition from June, 1997 through September, 1998. Projected improvements for the fourth quarter of 1998 and early 1999 are also provided. Silicon oxynitride defects decreased from 0.5 particles/cm^2 at 1000nm sensitivity to 0.9 particles/cm^2 at 250nm, a factor of two.

Best-achieved image placement control on a final mask improved from 35nm to 20nm during 1998. Image movement after absorber etching improved from 80-100nm to 30-40nm. This is an indication that film uniformity has improved significantly. Taken together, these are remarkable improvements which enable the formation of excellent x-ray mask substrates for the fabrication of defect-free masks with good image quality and placement.

6.4.1 Etch Stop Deposition

Flow versus as-deposited stress curves at various powers are provided in Figure 57 on page 118 for chromium. These curves show that chromium film stress can be varied from a very high tensile value to lower tensile stress by increasing argon gas flow or reducing deposition power. Stress did not become compressive under the conditions studied. From this data, 1500 watts and 30sccm argon flow were selected as process conditions for chromium etch stop deposition. At these conditions, a 22 second deposition time produces chromium approximately 25nm thick with stresses ranging from 300 to 500MPa. It is very difficult to measure and control wafer-to-wafer stress uniformity for chromium at these thin film thicknesses. Fortunately, since the chromium film acts only as an etch stop and conductivity layer, the stress levels obtained are adequate. Additional experiments are underway to develop lower stress chromium and chromium nitride deposition processes for use as a hard mask layer.

6.4.2 Refractory Metal Deposition

Flow versus as-deposited stress curves at various powers are shown in Figure 58 on page 119 for tantalum silicon film deposition. They demonstrate that tantalum silicon film stress behaves differently from chromium, becoming less compressive as argon flow increases or deposition power decreases, passing through zero and becoming tensile. This data is consistent with the relationship between pressure and stress for this material as cited in literature on deposition. Process conditions of 5000 watts deposition power and 6sccm argon flow were selected for tantalum silicon absorber deposition. At these conditions, 500nm thick tantalum silicon films are deposited in 112 seconds with compressive stresses ranging from -230 to -145MPa. Generally, 20 to 25 wafers constitute a deposition lot and exhibit stress variation of less than ± 5 MPa from the mean value. Typical stress values for films on several substrates are given in Table 27. They show that as-deposited stress is dependent not only on deposition conditions but on underlying substrate composition. It is believed that this dependence is largely the effect of surface roughness, but other factors may also play a role. Figure 59 on page 120 is a sheet resistivity plot of a single wafer demonstrating uniformity of 5%. This is also an indication of good film thickness uniformity.

Table 27. Tantalum Silicon Stress. As-Deposited Tantalum Silicon Stress on Several Substrates With the Same Deposition Conditions at MMD.

TaSi on Boron-doped Si (MPa 1σ)	TaSi on Cr/Si (MPa 1σ)	TaSi on Cr/Boron-doped Si (MPa 1σ)	TaSi on Cr/SiC (MPa 1σ)
-213 (11)	-194 (5)	-152 (14)	-169 (11)
-209 (14)	-196 (10)	-153 (15)	-174 (11)
-211 (10)	-194 (9)	-151 (12)	-176 (11)
-209 (10)	-194 (8)	-151 (9)	-175 (16)
-210 (11)	-194 (11)	-151 (18)	-169 (11)
-211 (8)	-194 (6)	-151 (12)	-169 (18)
-200 (11)	-	-151 (11)	-171 (10)
-213 (9)	-	-150 (17)	-
-207 (12)	-	-149 (17)	-
-200 (11)	-	-149 (15)	-
-209 (12)	-	-145 (15)	-
-207 (14)	-	-	-
ave. = -208	ave. = -194	ave. = -150	ave. = -172

Thickness measurement has been accomplished by a combination of profilometry and x-ray fluorescence. Profilometry is slow and requires monitors in which a step edge has been etched or created by masking during deposition. Accuracy is estimated to be good for smooth films a few hundred nanometers thick, but precision is highly dependent on the condition of the step edge at the point of measurement. X-ray fluorescence has a high precision but is dependent on good calibration standards for accuracy. The tool available for use by the MMD at the IBM Burlington facility is set

up for use primarily for eight inch wafers, and is located outside of the MMD facility. Capital justification is proceeding for purchase of a dedicated x-ray fluorescence tool with funding expected in 1999. Figure 60 on page 121 demonstrates the within-wafer and wafer-to-wafer thickness uniformity for a typical tantalum silicon deposition run. Although these numbers indicate a 530nm thickness, the real value is 500nm since there is an offset between the x-ray fluorescence measurements and the profilometry measurement of approximately 30nm. This is due to calibration error and will be corrected when a dedicated tool is available.

The annealing process used at Motorola was duplicated at MMD by refurbishing a used AG 610 rapid thermal annealing furnace. A silicon carbide coated graphite susceptor was employed to hold the wafer and improve temperature uniformity. At the low annealing temperatures required, pyrometry was unsuitable for furnace temperature control. An AG Associates "cantilever thermocouple" was installed in contact with the susceptor bottom to provide temperature information for furnace control. A silicon wafer with a thermocouple (TC) potted into the silicon was used as an independent measure of the temperature inside the susceptor. Furnace recipes were developed by varying purge gas flow, furnace temperature and annealing time while monitoring TC wafer temperature. In this manner, conditions were found to obtain good correlation between the furnace control "cantilever thermocouple" and the silicon wafer thermocouple temperature (<5 degree delta). Ten minute annealing recipes were developed for temperatures between 350 and 450°C at 10 degree increments. Films were shown to anneal reliably between 360 and 450°C (Figure 61 on page 121). Annealed films typically exhibited within-wafer stress variation of 10MPa (1σ). In practice, these curves are used to estimate annealing temperature for send-ahead wafers which are annealed to determine the correct temperature for each lot. The remainder of the lot is then annealed at the conditions that provide acceptable stress.

Stress measurement has been accomplished using a dedicated Tencor Flexus 5510 with SMIF interface. This tool provides a stress uniformity map as well as an average stress value for the wafer surface. Figure 62 on page 122, Figure 63 on page 123 and Figure 64 on page 124 are representative stress maps from chromium, tantalum silicon and silicon oxynitride films, respectively. Figure 65 on page 125 provides stress data for three typical production lots of tantalum silicon. This data shows that MMD metal films have good stress repeatability within lots both for as-deposited and annealed films. The one to two wafer variation seen in the graph is due to send-ahead wafers that are annealed to find the correct conditions for each lot.

A new Summit 200 Rapid Thermal Processing Furnace ordered in late December, 1997 from Eaton Thermal Processing Corporation was delivered and installed in early October, 1998. The Summit 200 has a Standard Mechanical Interface (SMIF) which reduces handling defects during annealing. This system has demonstrated ± 1 degree temperature uniformity across a four-inch wafer and <0.0005 particles/cm^2 during acceptance testing.

Tantalum silicon films deposited with the Endeavor system in the MMD have been characterized using Rutherford Backscattering Spectroscopy (RBS), Auger Electron Spectroscopy (AES), X-Ray Diffraction (XRD), Secondary Mass Spectrometry (SIMS) and Atomic Force Microscopy (AFM). Figure 66 on page 126 is an RBS plot of a tantalum silicon film. Figure 67 on page 127 and Figure 68 on page 128 are XRD plots of the frontside and backside of silicon wafers with annealed and un-annealed tantalum silicon films. These graphs show that the tantalum silicon films are amorphous and composed of 70-75 atomic percent tantalum and 25-30 atomic percent silicon, with 1-2 atomic percent oxygen possibly present as a deposition impurity. Figure 69 on page 129 shows AES profiles of Motorola and MMD tantalum silicon films. Comparison of these shows that the MMD films are more consistently uniform throughout the depth of the film. Chromium films have not been analyzed since the etch stop composition has minimal effect on the performance of the x-ray absorber. In addition, the chromium films are deposited from a single component target and should be relatively pure.

6.5 Silicon Oxynitride Hard Mask Deposition

The Plasmatherm SLR PECVD system was qualified for hard mask and sacrificial layer deposition. Hard mask deposition conditions and film stress were optimized to give the smallest amount of image placement movement during BEOL processing. Hard mask thickness is measured on one wafer from each deposition run, stress and particle counts are measured on each wafer. The yield is 100% for both thickness and stress. A shield to block the deposition of the hard mask in the EL-4+ P0 ground-contact area was evaluated and is now being used for all product hard mask depositions. The shield eliminated the need for a wet contact etch step prior to resist coat without changing the thickness uniformity or stress and without increasing defect levels. A 1μm sacrificial protective layer for the front side of the wafers was developed and evaluated. The sacrificial layer is deposited before the membrane definition and is removed using 10:1 BHF before the chrome, TaSi and hard mask are deposited. Since the implementation of the sacrificial layer process there has been a significant reduction in the number of defects cause by frontside handling during the membrane definition.

6.6 Refractory Etch

In late 1997 and early 1998, an etch process was defined for Falcon and Nighteagle line monitors, and the results were compared for MMD- and Motorola-deposited film stacks. It was found that the MMD-deposited stacks etch at similar rates and with similar etch profiles to the Motorola film stacks. The TaSi films deposited with the SFI Endeavor sputter deposition system at MMD were found to be more uniform in composition versus thickness as observed in the emission endpoint signals during the absorber etch.

Etching of <180nm structures has proceeded this year. One-hundred-fifty nanometer deep trench structures, and 130 and 100nm microwave device gates have been fabricated. In a thinner TaSi absorber with thinner hard mask and UVIII resist, 75nm lines and 75nm spaces were fabricated (Figure 70 on page 130).

An experiment was conducted to quantify the etch bias at each process step. Several Falcon and Nighteagle masks were measured in resist, and after descum, hard mask etch, resist strip, TaSi etch, and hard mask strip. Significant etch biases were observed in the descum (leading to the qualification of the new descum discussed above) and the TaSi absorber etch. Figure 71 on page 131 shows the total etch bias (for all the steps). A small nested-to-isolated offset and RIE lag was observed in the hard mask etch, but no process changes have occurred on the hard mask etch.

A more anisotropic descum was qualified on the AM42. By operating at a lower pressure, the process is more anisotropic with less etch bias than the old process-of-record. The typical resist removal during the descum is about 30nm with about a 15nm etch bias. The etch bias versus descum time was also quantified so that the descum can be used as a CD trim etch when necessary. For Nighteagle masks, the etch bias decreases approximately 1.3nm per second of descum time.

Considerable effort has been expended to understand the CD variations within Falcon line monitors and how process parameters affect CD variations. Several Falcon masks have been measured with a CD SEM partition measurement program that characterizes the cross-mask image variations from cross-mask bow, with electron beam write field, field-to-field, and microloading components to the CD 3σ. The largest contributor to the CD 3σ was the cross-mask bow (a reduction in CD near the edge of the membrane). The within-field component is approximately 6 to 9nm, field-to-field is approximately 4nm, and the microloading (edge of pattern effect not near the membrane edge) is near zero. However, the effect from the edge of the membrane is highly variable and can contribute 5 to 35nm.

The TaSi absorber etch is known to be the major driver of CD variations in back-end-of-line processing (as confirmed by CD measurements by process step), and a three-factor response surface model designed experiment was conducted to observe the impact of oxygen flow, *RF* bias power, and cathode temperature on CD results (etch bias, uniformity, RIE lag, and nested-to-isolated offset). A strong interaction between oxygen flow and bias power was observed on hard mask selectivity, and hard mask selectivity was seen to be strongly related to etch bias control. At high oxygen flows, more bias power can be tolerated without compromising the hard mask. Cathode temperature had only a small effect on CD parameters. Figure 72 on page 132 shows the response chart for the designed experiment results.

Several experiments were conducted to understand how backside cooling in the critical etch processes affect Falcon CD 3σ. Various temperature and backside helium pressure settings were tried in the SiON hard mask etch. Cathode temperature showed negligible effect on CD and uniformity, but backside helium pressure caused

a measurable shift in CD (about 7.3nm/Torr). As the wafer temperature increases (lower backside pressure), the resist etch rate rises and the CD increases. However, the CD uniformity did not change with backside cooling parameters. Etch rates of SiON and resists on membranes were also checked and found to agree fairly closely with those on wafers.

In the tantalum etch process cathode temperature was one of the parameters in the designed experiment, and it was found to have little impact on CD and CD uniformity. As in the hard mask etch process, backside helium pressure had a much larger effect. Changing to 2 Torr backside pressure resulted in the hard mask failing in the center of the mask, leading to large, rough images. Eight Torr backside pressure resulted in slightly smaller images with slightly worse sidewalls. There was little change in CD uniformity with cooling parameters, however.

Etching of alternative materials has been explored. Early results on Ta_4B etching have been favorable. Falcon line monitors fabricated in Ta_4B have had excellent sidewall angle using a lower *RF* power than has been used for TaSi masks. Lower power is better for hard mask selectivity. Fabrication of Nighteagle line monitors in Ta_4B took place during 3Q98. Blanket etch rates of chromium and chromium nitride hard masks indicate that the 50 Watt TaSi etch provides good selectivity of TaSi to Cr/CrN. The etch rate of Cr at 50W TaSi etch is $<$16nm/minute.

6.7 Proximity Correction Algorithm Evaluation and Optimization

A statistically-designed experiment was completed in 2Q98 using the DOSE6 two-Gaussian algorithm. This experiment found that the optimized settings were very close to the original settings, and no improvement in dose range was expected over the original settings. It was decided, therefore, to remain with the original settings with this algorithm. Analysis of the three-Gaussian algorithm is planned, but has been on hold due to line priorities.

In addition, we have been working with Auburn University in Alabama to evaluate a shape-modification method of proximity correction. The shape-modification patterns were written without dose modulation proximity correction, and SEM micrographs of the Falcon pattern were taken. The shape-modification patterns did not result in acceptable images: there were gaps between the shapes. Display subfield program (DSP) plots showed thin regions of 50nm images which did not resolve, causing the gaps.

Auburn University has developed a new calibration and has submitted new data for evaluation. The new data has been post-processed and will be written on a Falcon mask in the test site areas.

6.8 Conductive Polyaniline

No work was done on the conductive topcoat during 1998. Current results with multiple pass writing have not shown an immediate need for a conductive topcoat. This project will remain on hold until a need is determined.

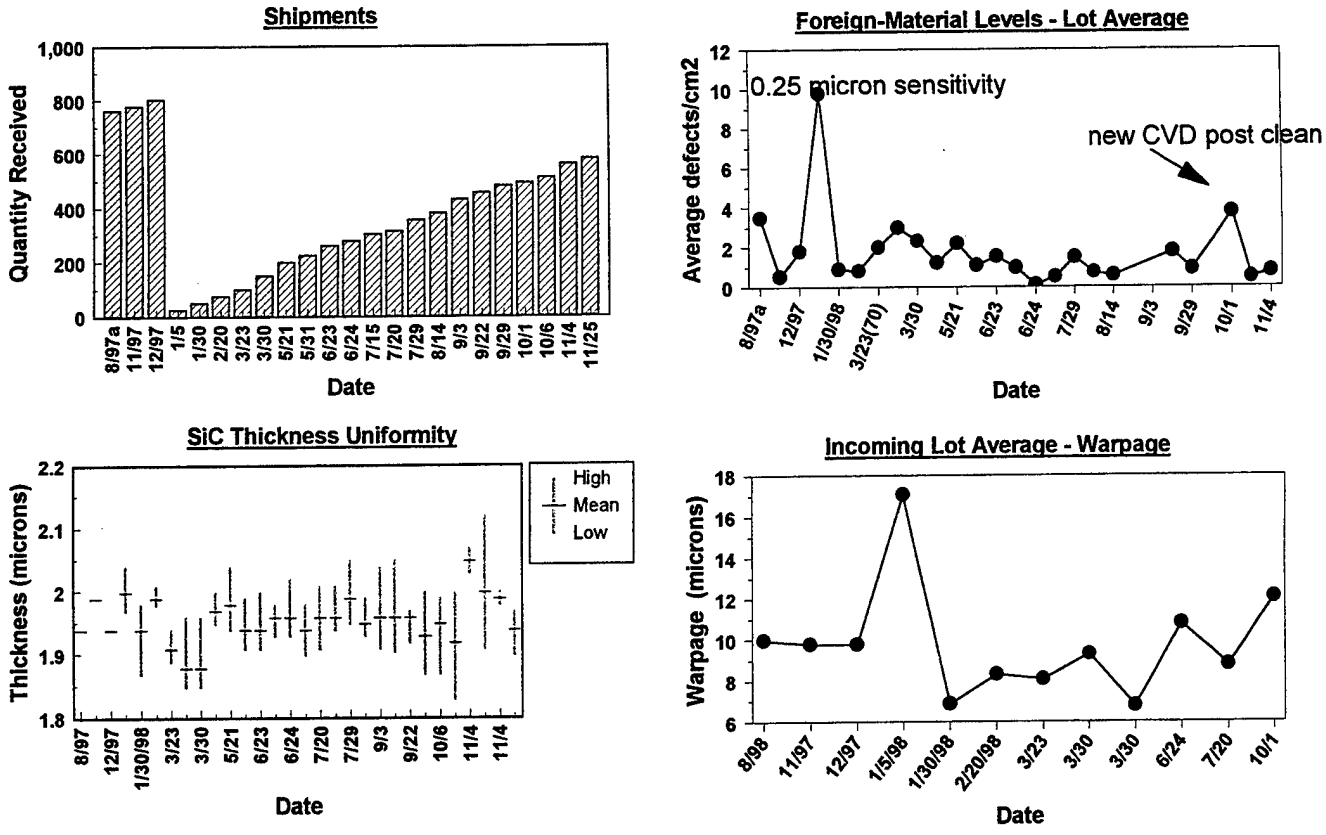


Figure 34. Silicon Carbide

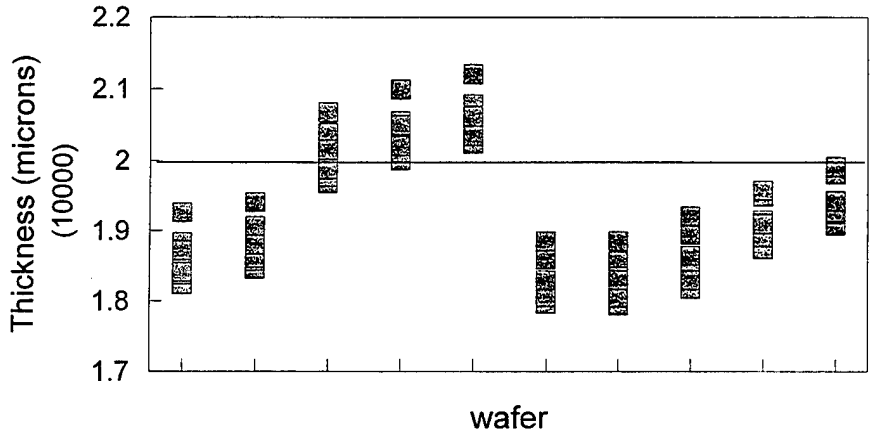


Figure 35. Silicon Carbide Uniformity

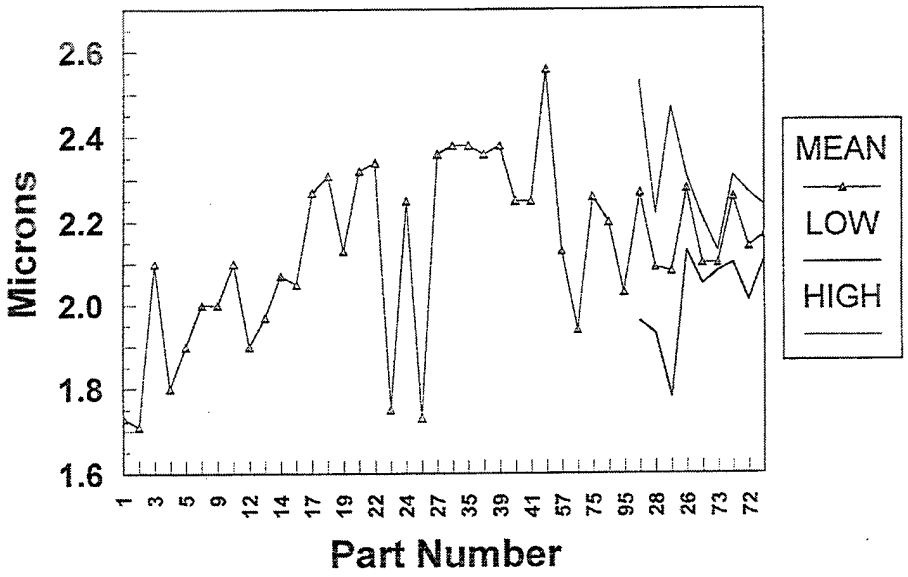


Figure 36. Diamond Thickness

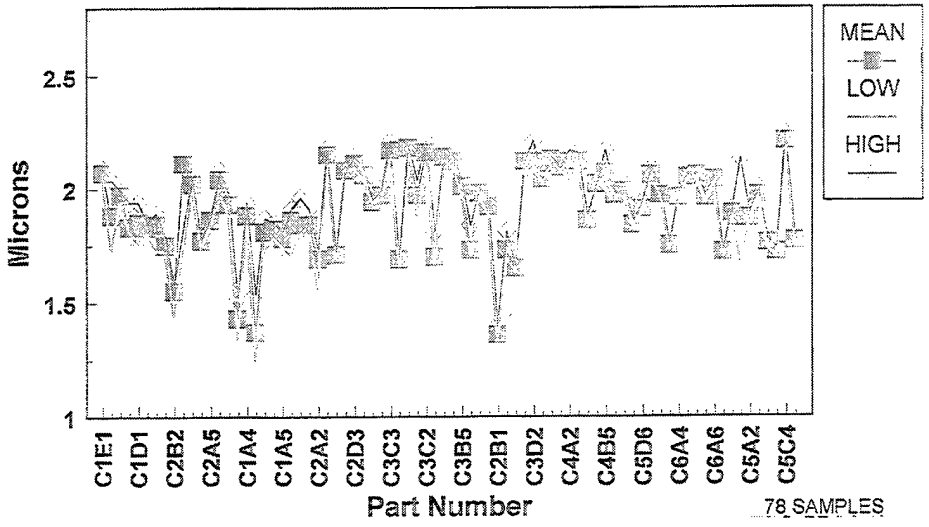


Figure 37. Crystallume Diamond Films (Diamond Thickness)

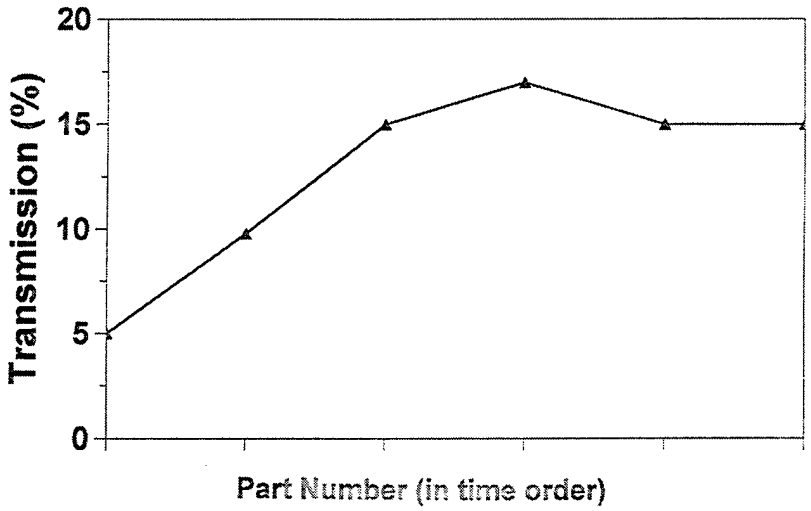


Figure 38. Crystallume Diamond Optical Transmission

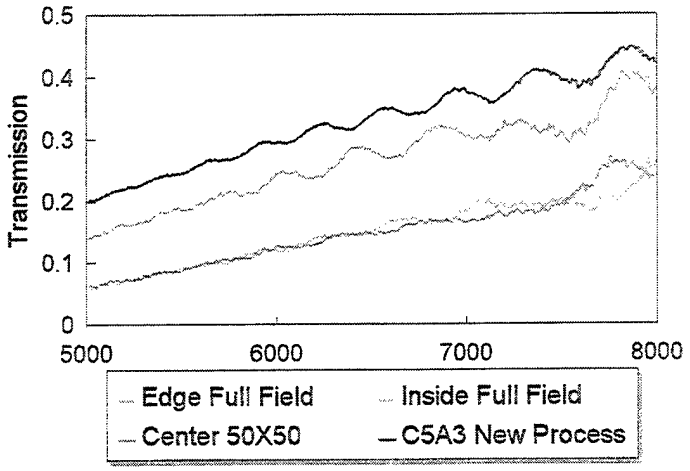


Figure 39. Crystallume Diamond Transmission Uniformity

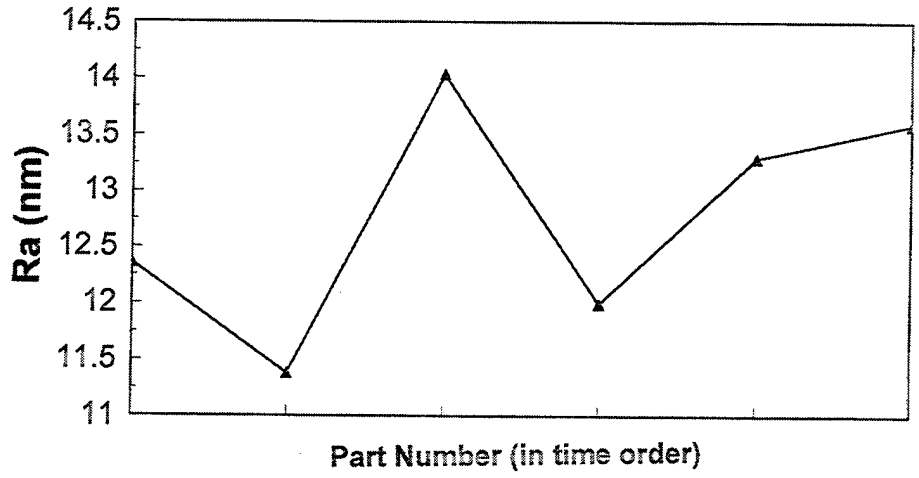


Figure 40. Crystallume Diamond Surface Roughness

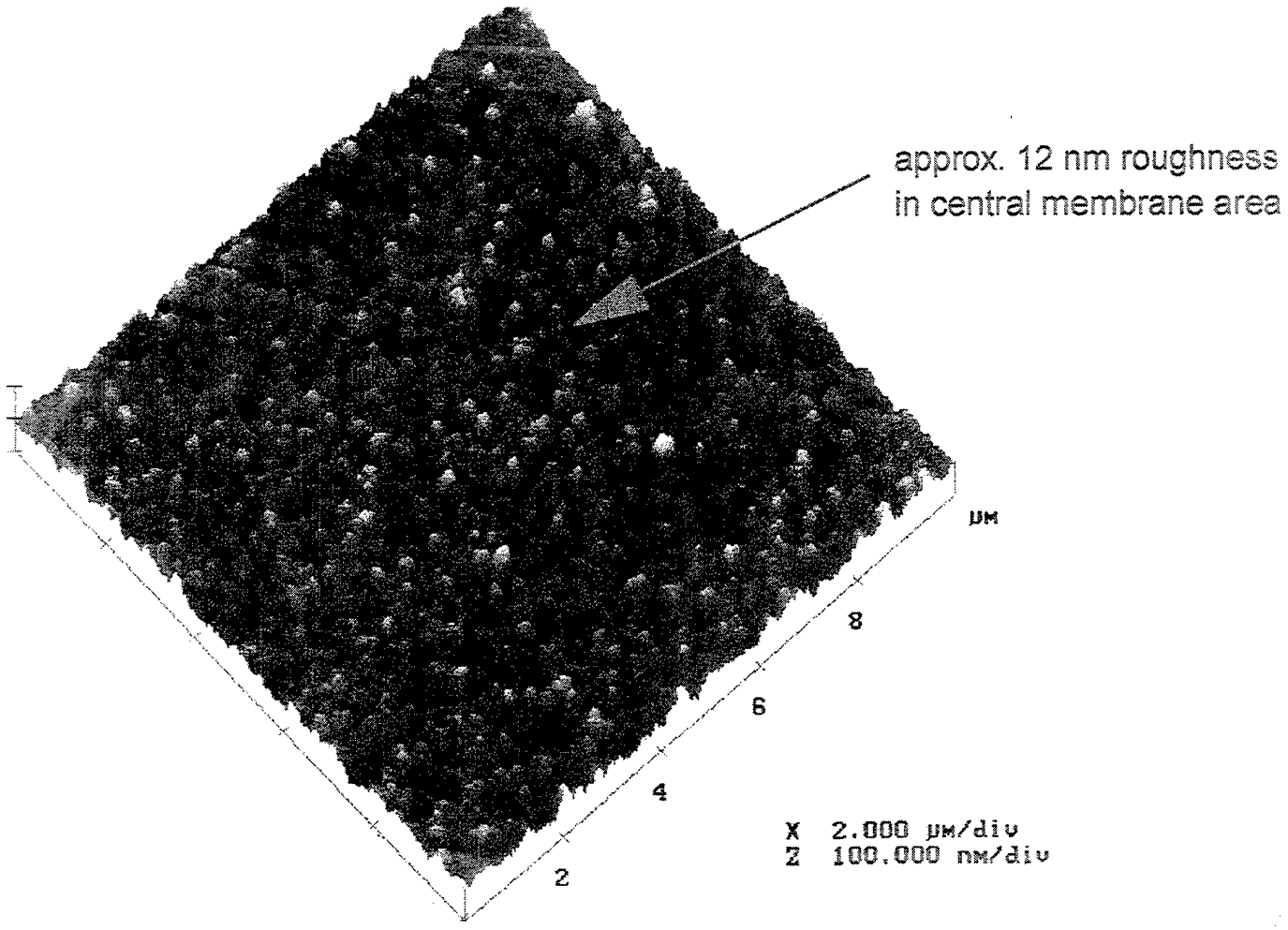


Figure 41. Crystallume Diamond Unpolished Film Surface Quality

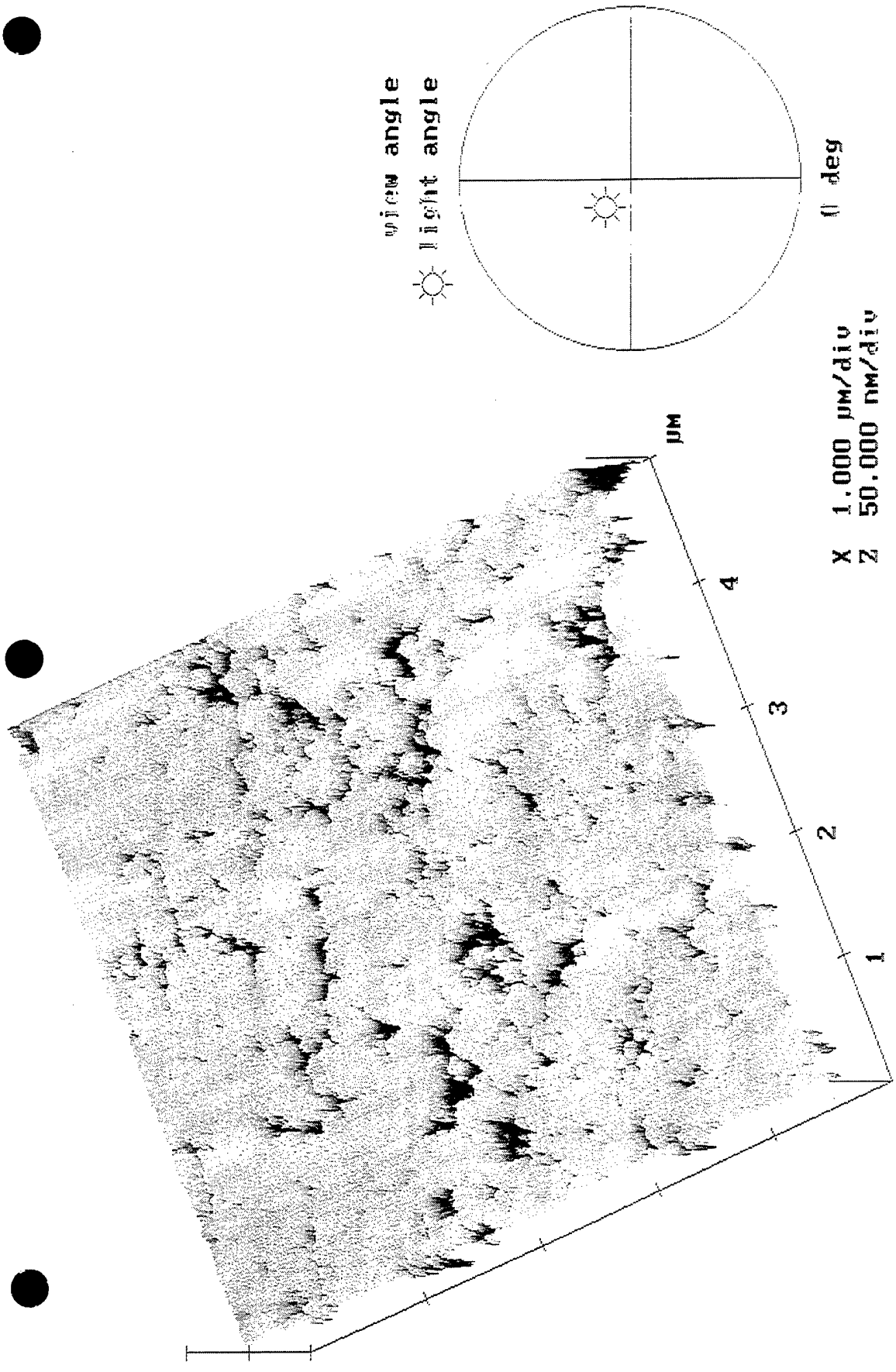


Figure 42. Surface Roughness of Polished Diamond Film

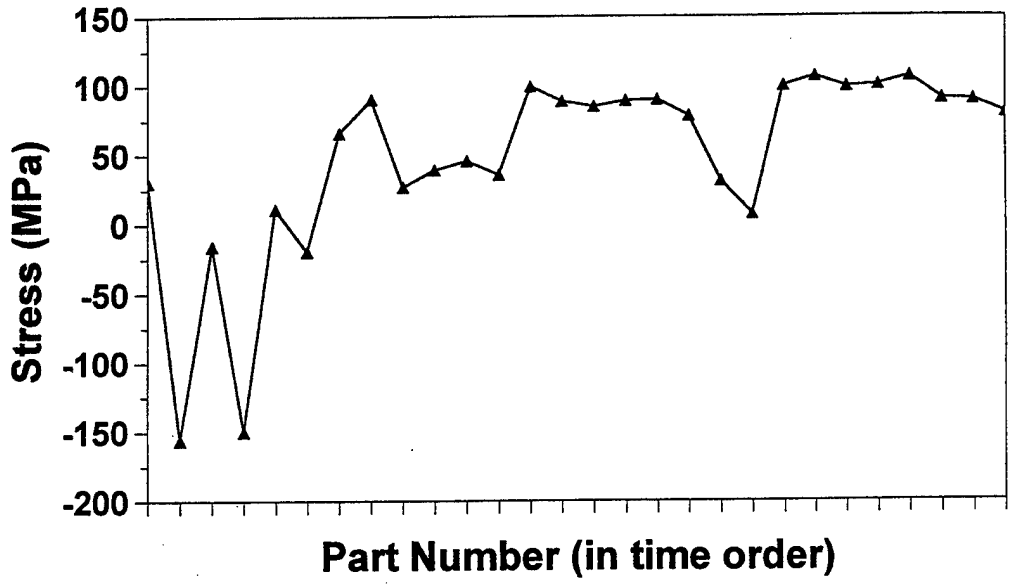


Figure 43. Crystallume Diamond Film Stress

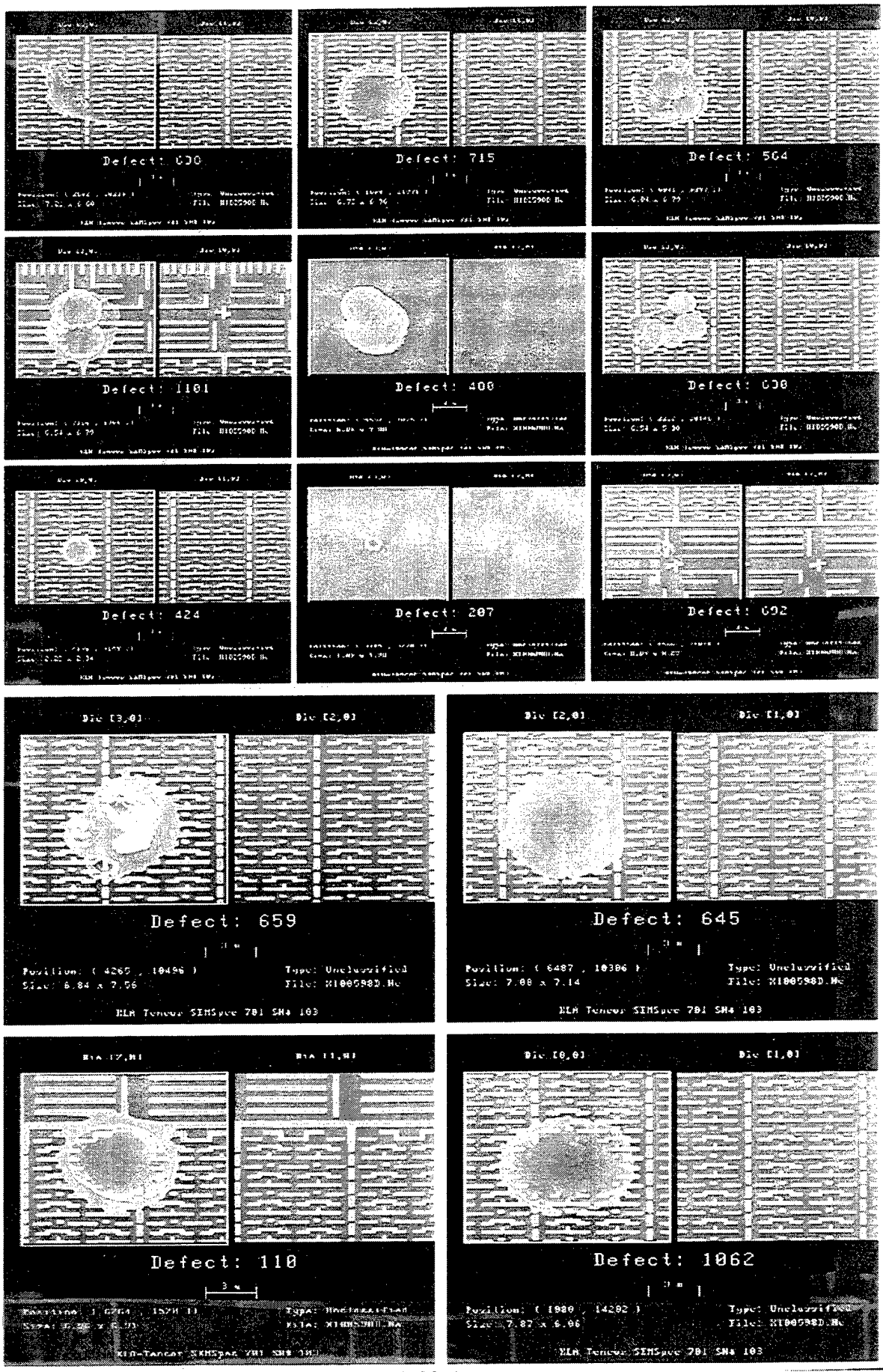


Figure 44. Crystallume Diamond Defects in Nighteagle Masks

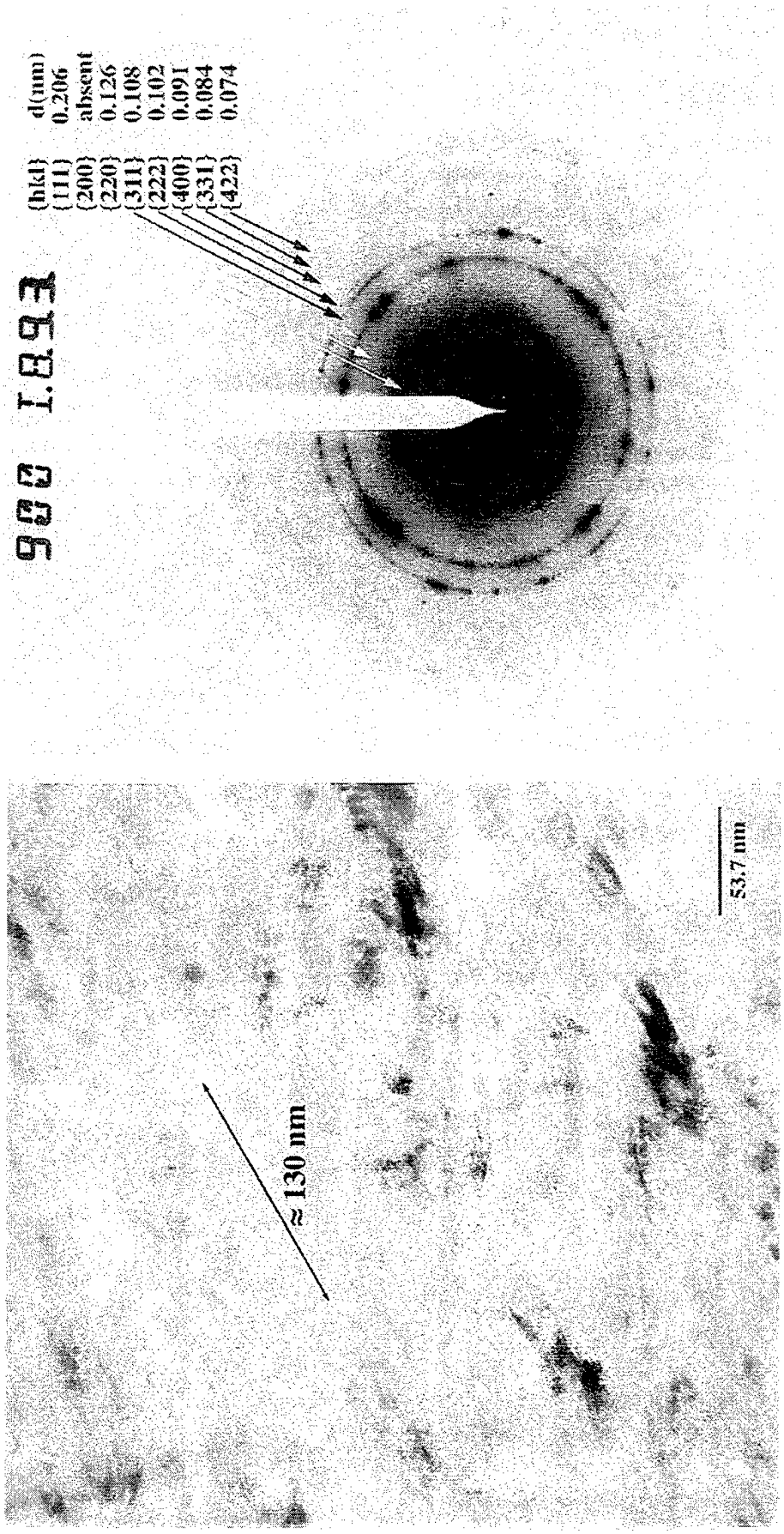


Figure 45. Crystallume Diamond Crystal Structure Measurements. Left - TEM micrograph shows < 10nm grain size. Right - Location of diffraction rings indicates crystalline diamond structure.

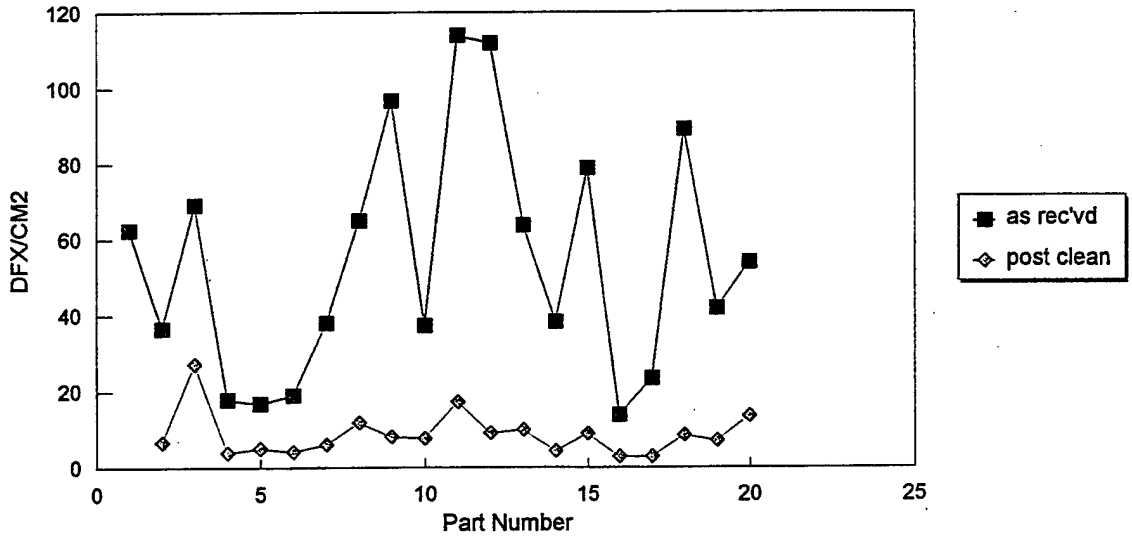


Figure 46. NTT-AT SiC Defect Data

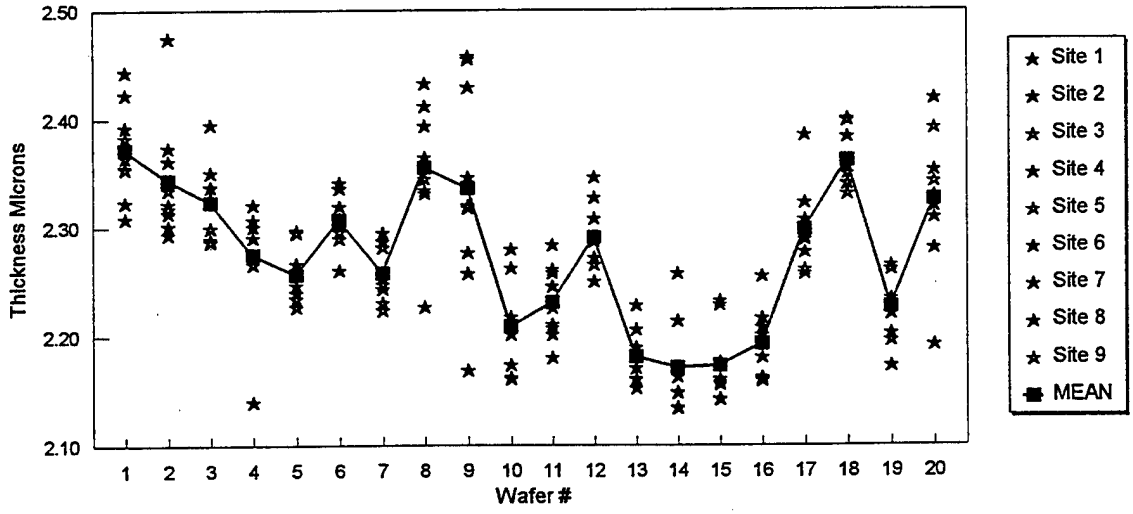


Figure 47. NTT-AT SiC Thickness Uniformity

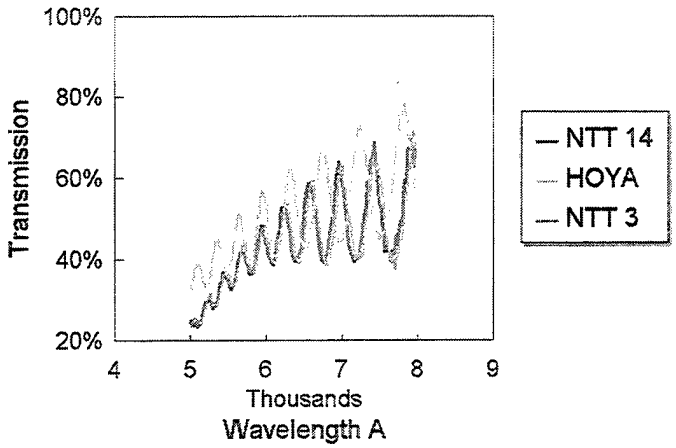


Figure 48. SiC Membrane Transmission

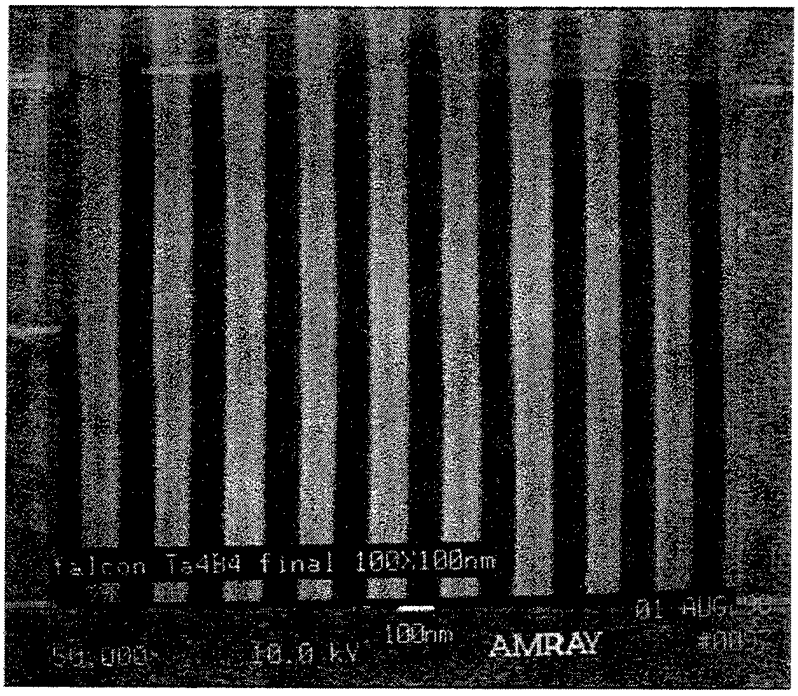


Figure 49. Hoya Ta4B Mask Results (100nm line/space)

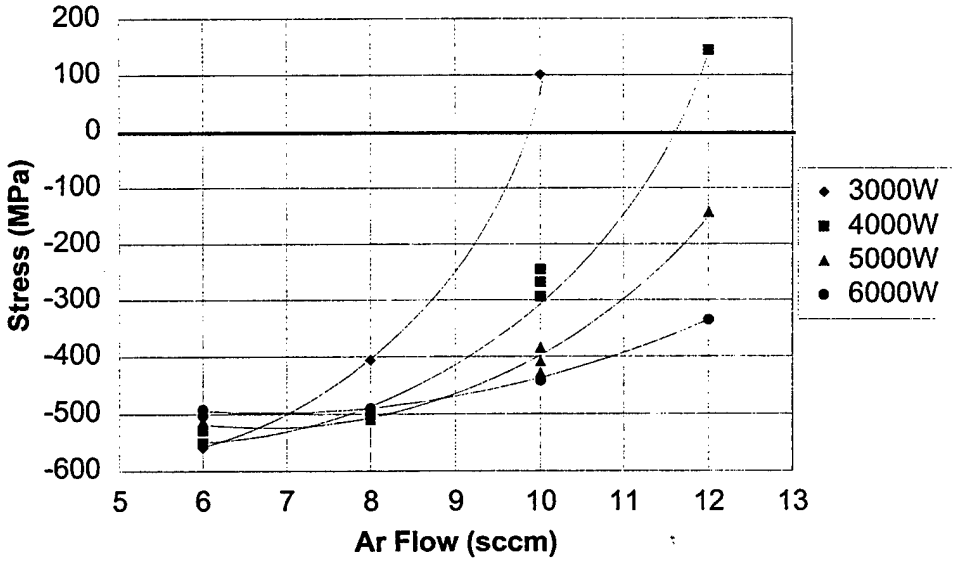


Figure 50. Ta4B Film Stress Characteristics. Ta4B stress versus argon flow and cathode power.

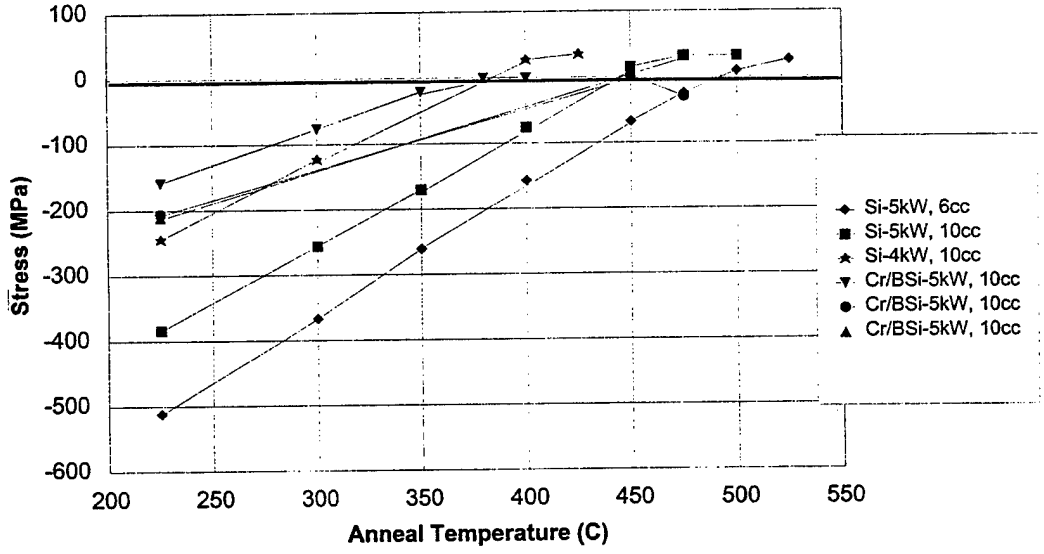


Figure 51. Ta4B Annealing Behavior. Ta4B stress versus anneal temperature.

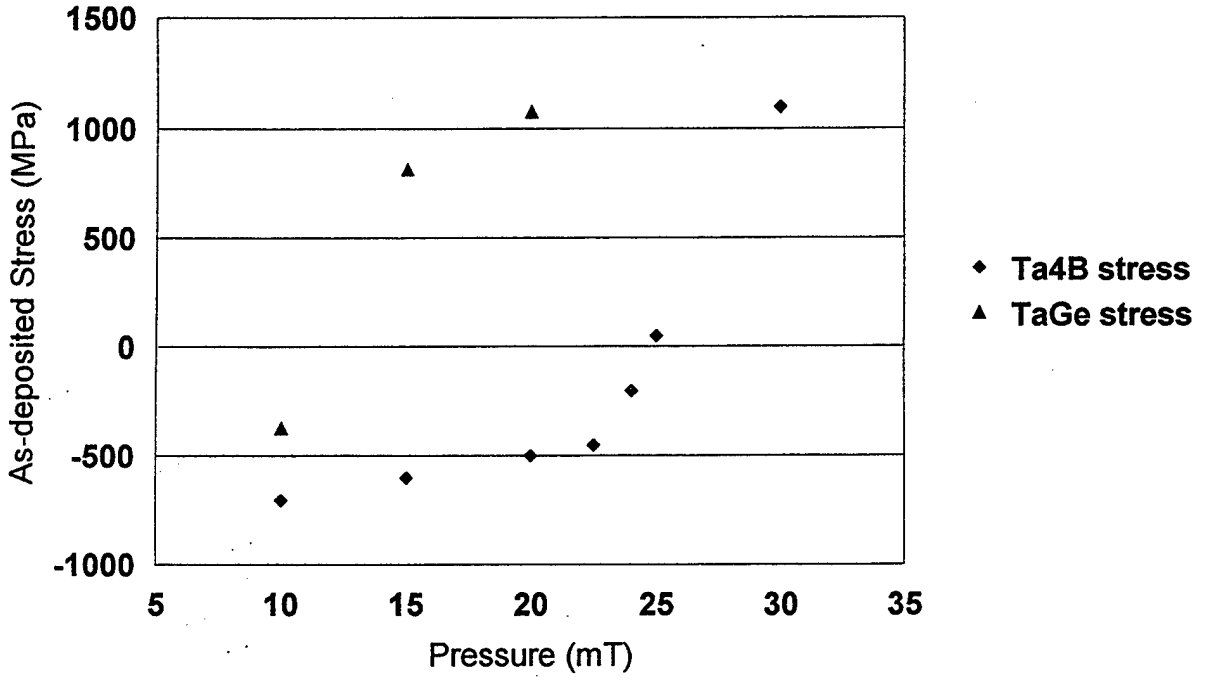


Figure 52. Ta4B and TaGe Deposition Conditions

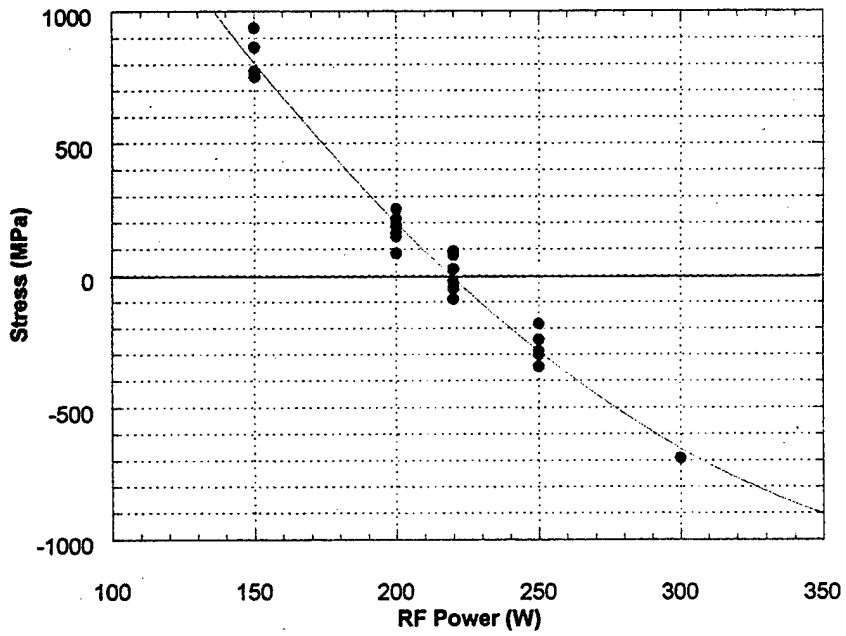


Figure 53. Cr Stress with RF (on Si)

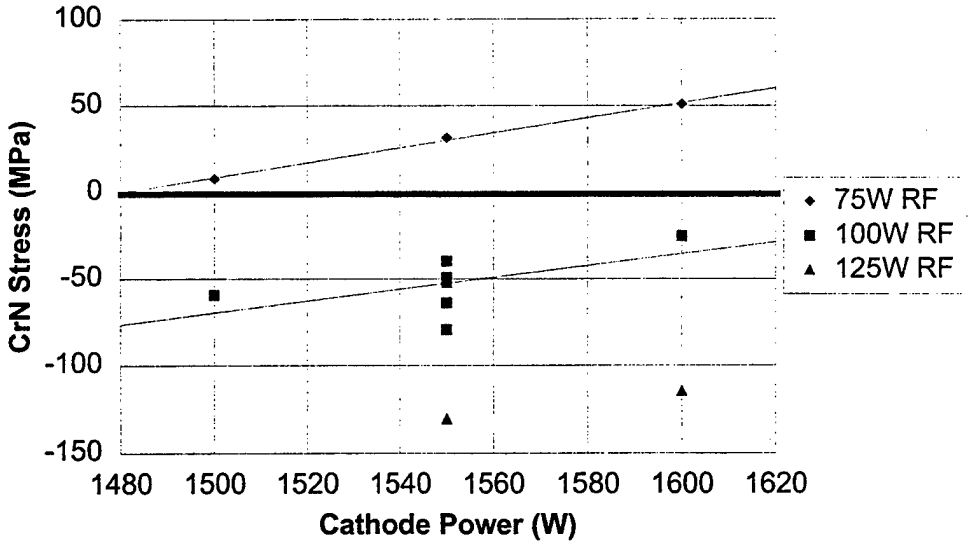


Figure 54. CrN Film Stress Characteristics. CrN stress versus cathode power and RF bias.

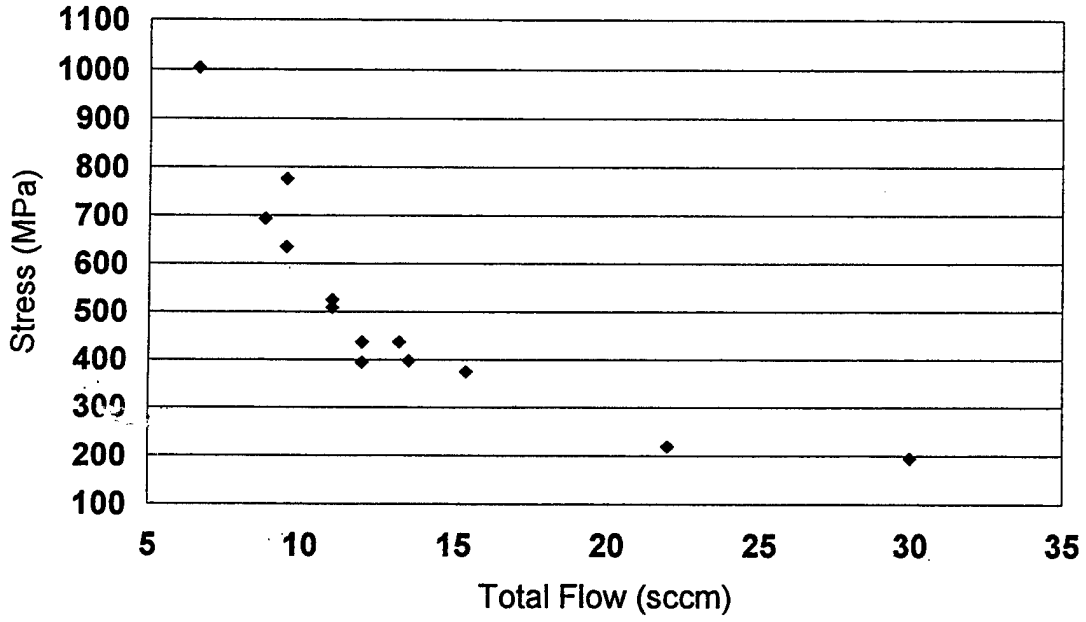


Figure 55. CrN Stress versus Total Flow. Constant AR:N_2 ratio.

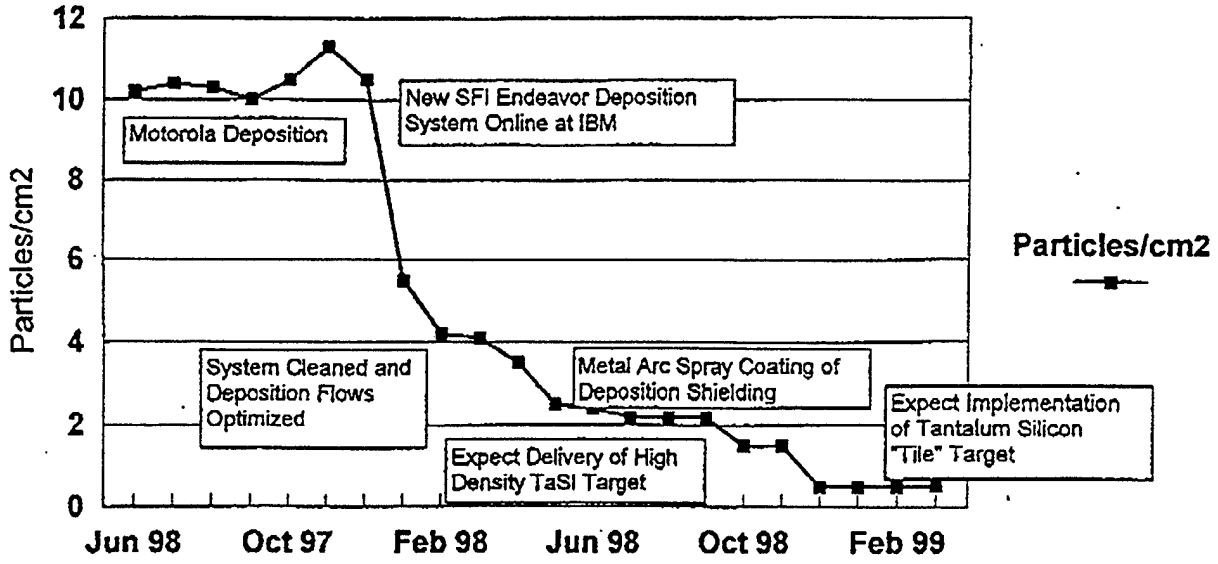


Figure 56. Foreign Material Reduction for TaSi Deposition

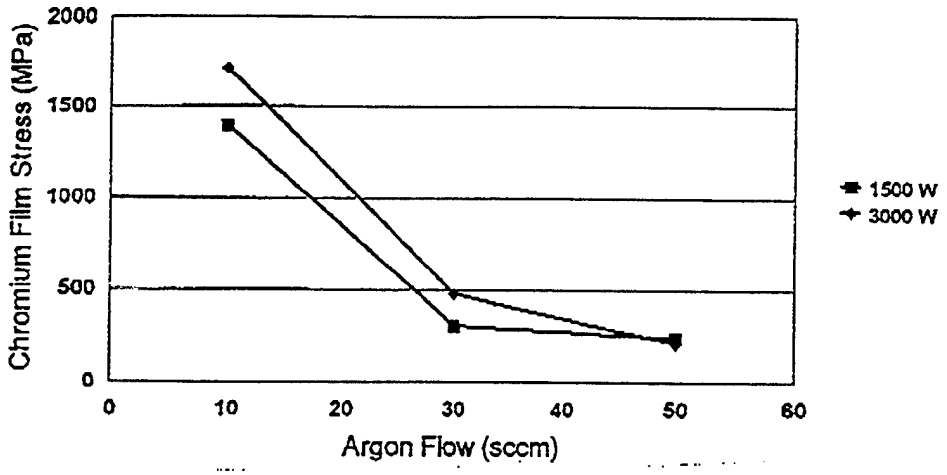


Figure 57. Variation of Chromium Stress with Power and Argon Gas Flow

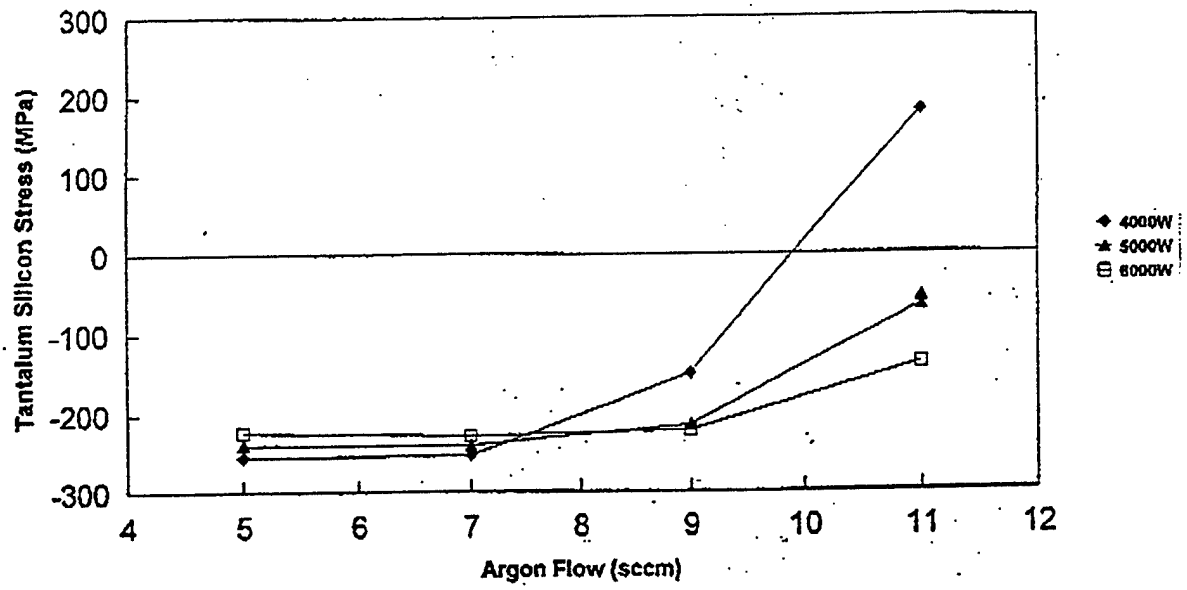


Figure 58. Variation of TaSi Stress with Power and Argon Gas Flow

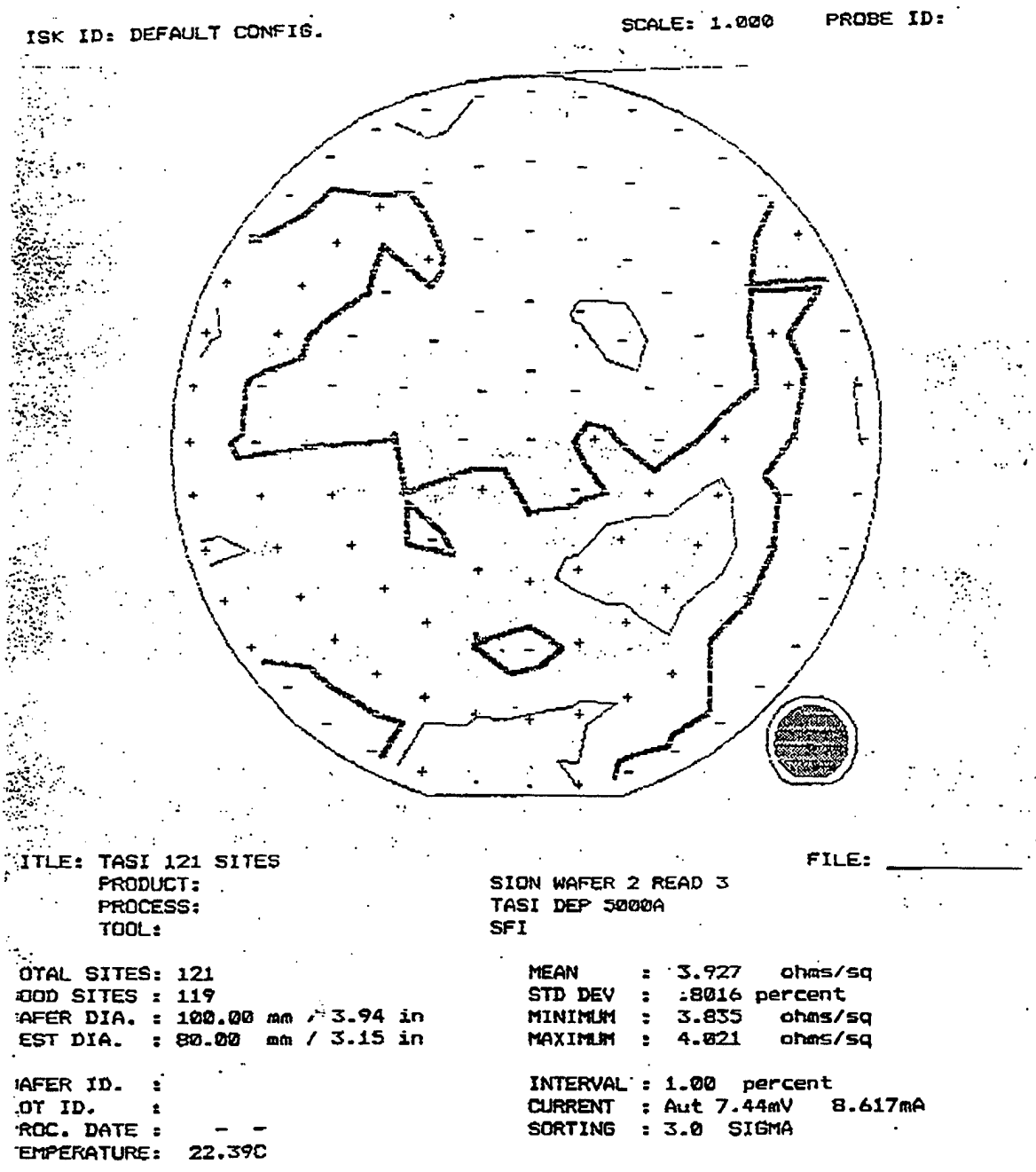


Figure 59. Sheet Resistivity of TaSi Film

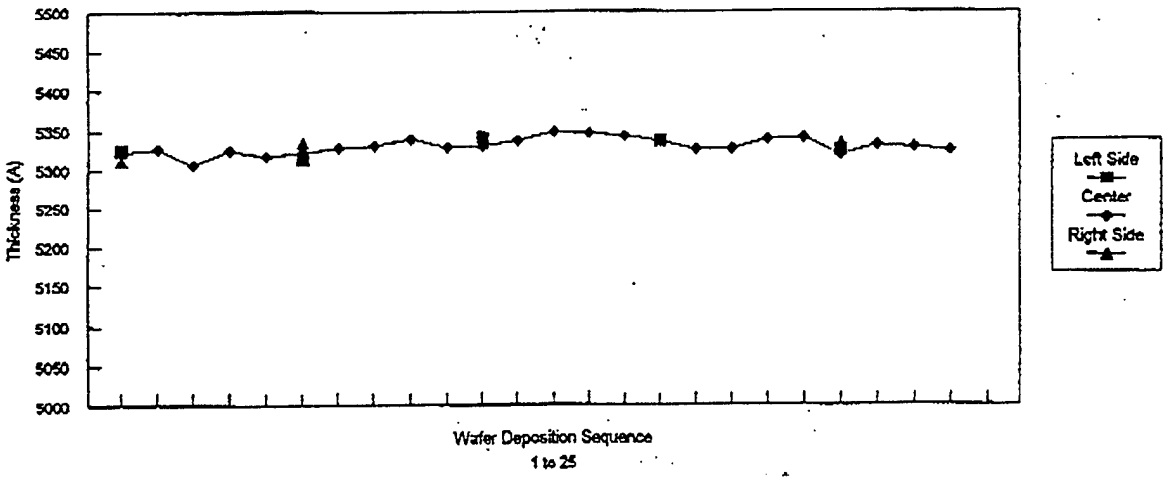


Figure 60. TaSi Thickness Uniformity

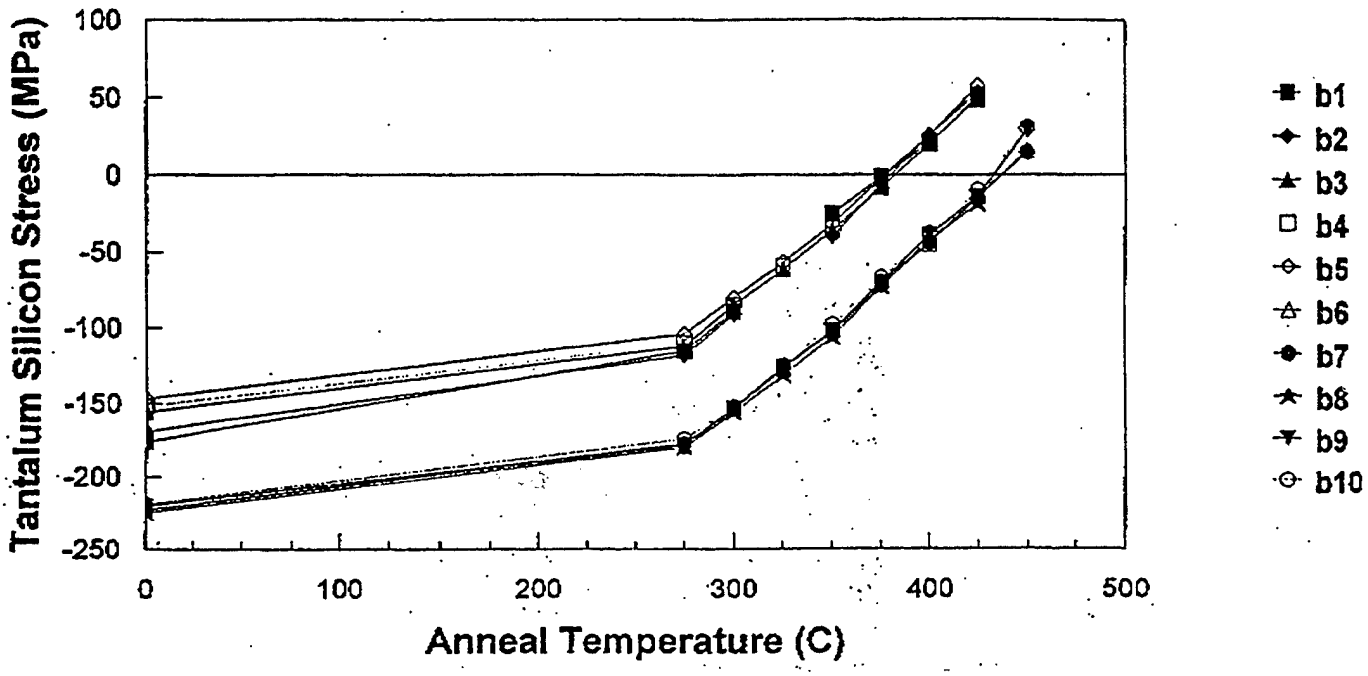


Figure 61. TaSi Stress versus Annealing Temperature for Two Process Conditions

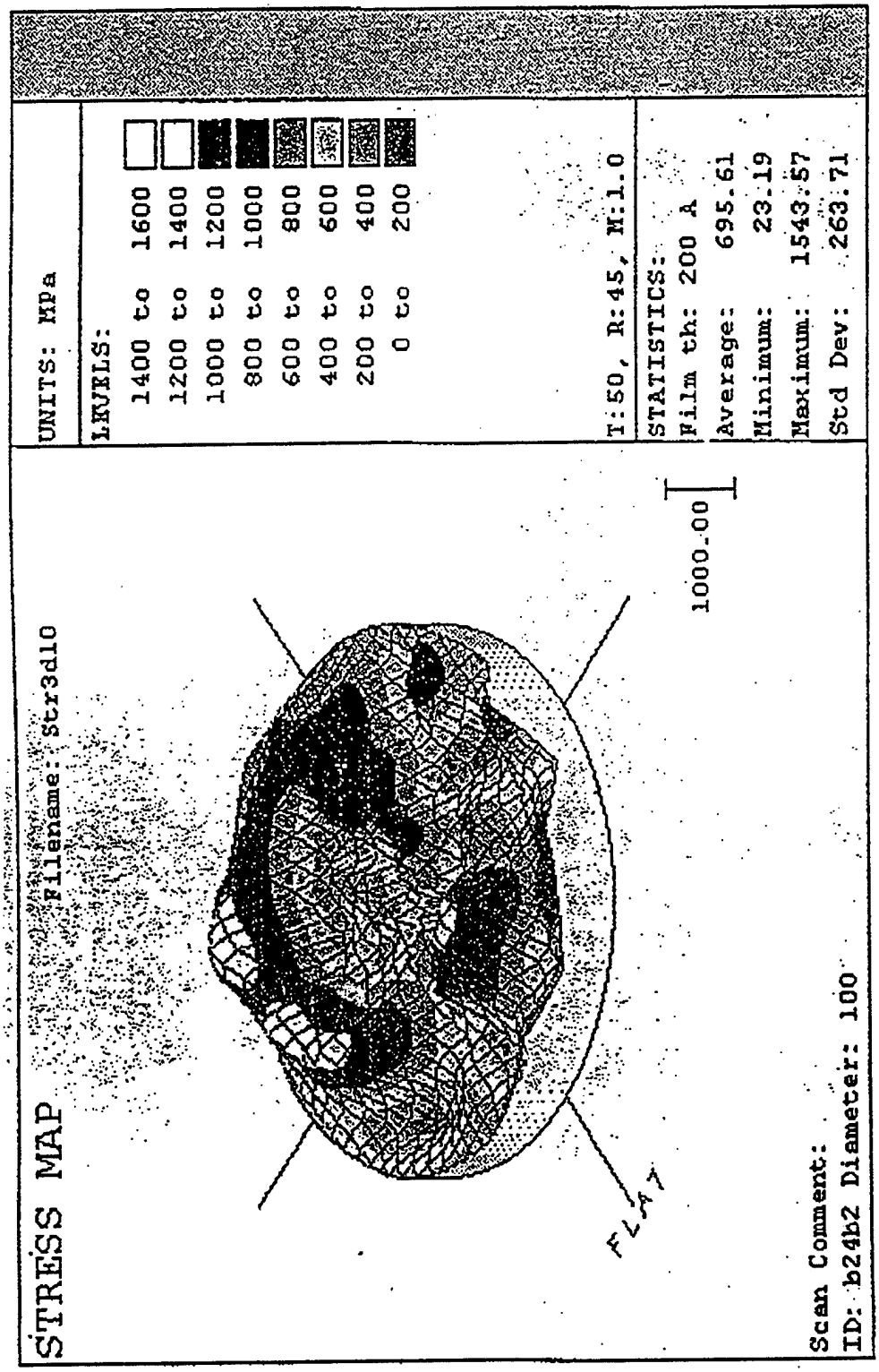


Figure 62. Stress Map for Chromium Film

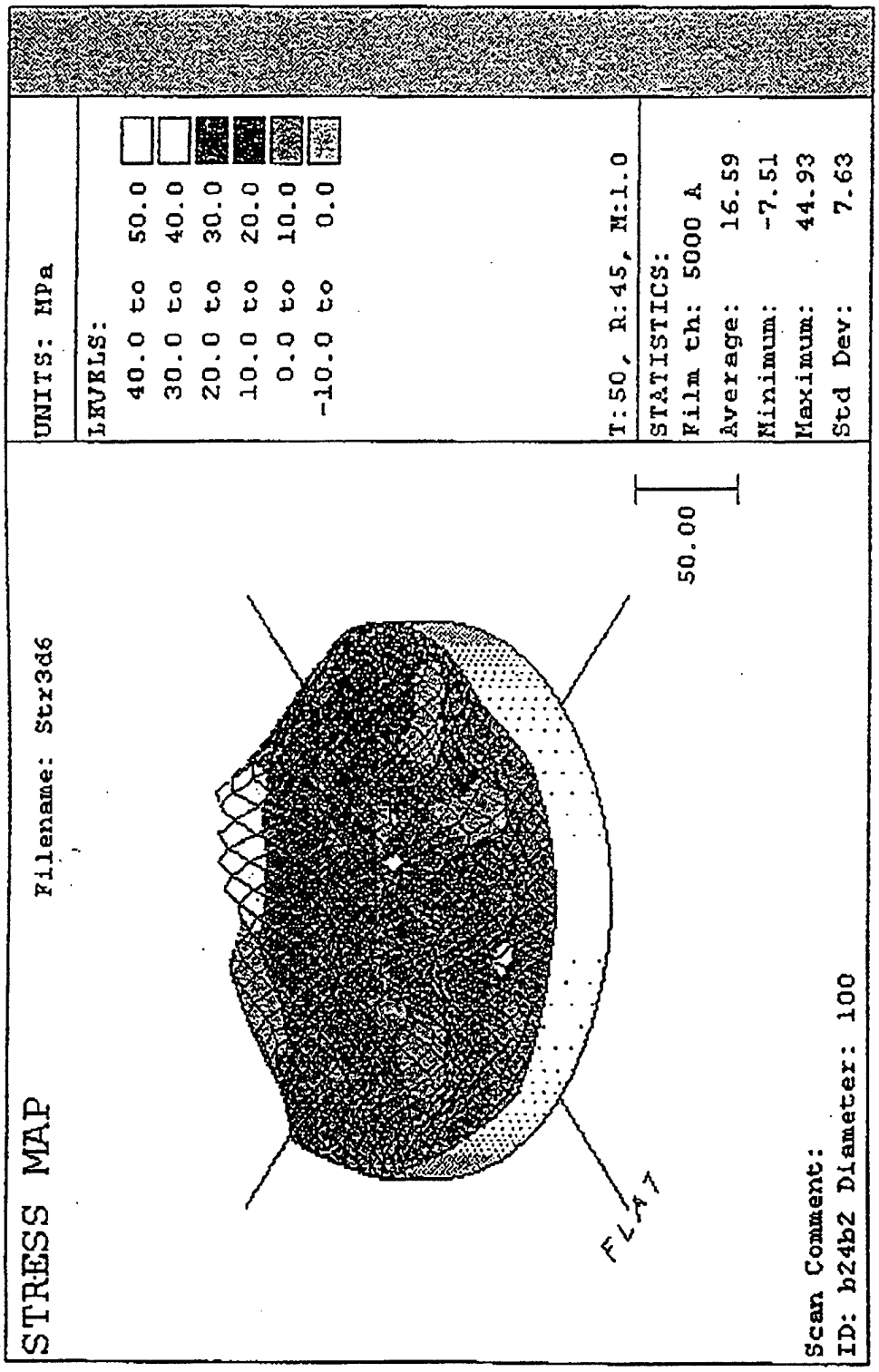


Figure 63. Stress Map for TaSi Film

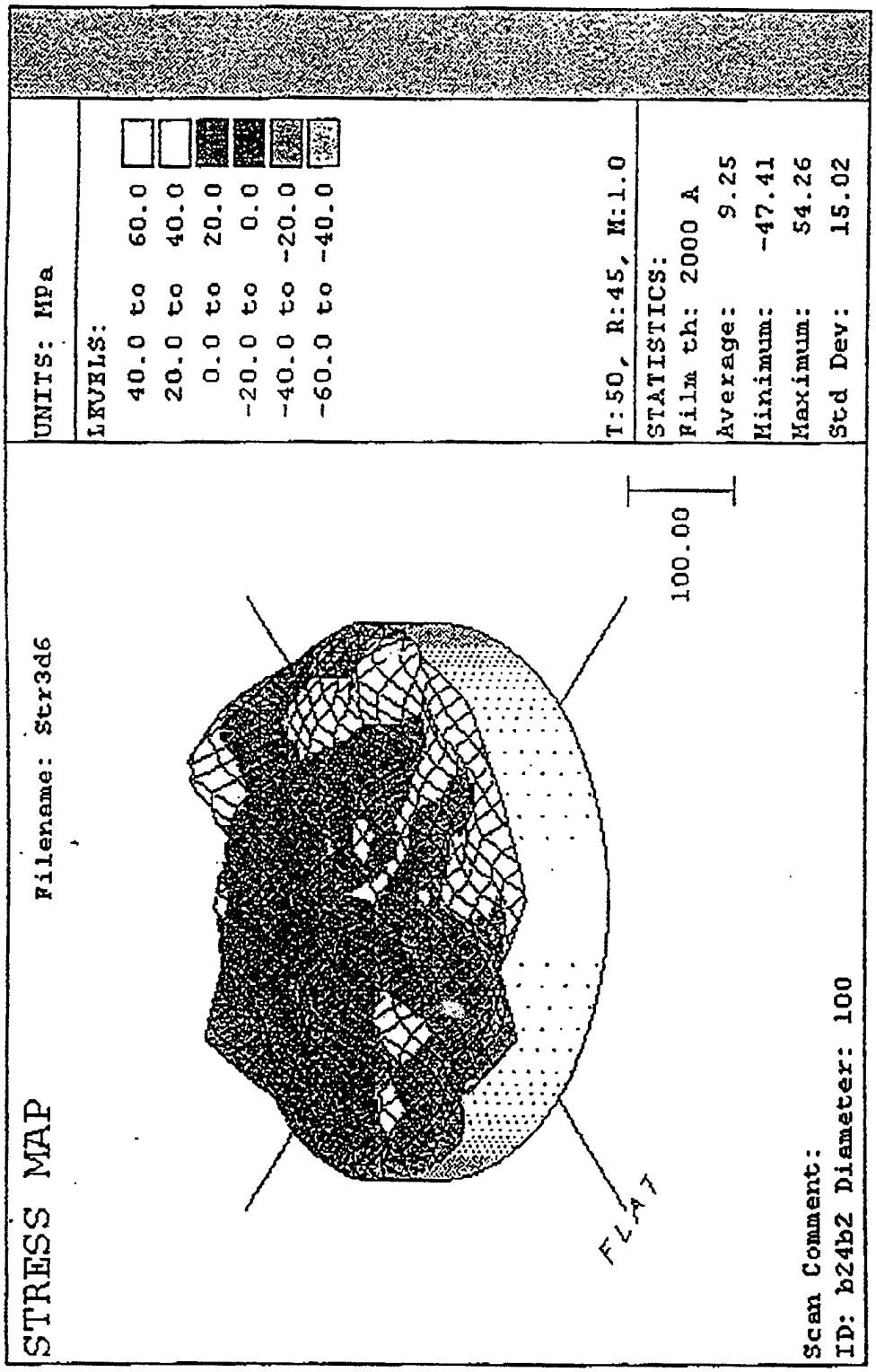


Figure 64. Stress Map for SiON Film

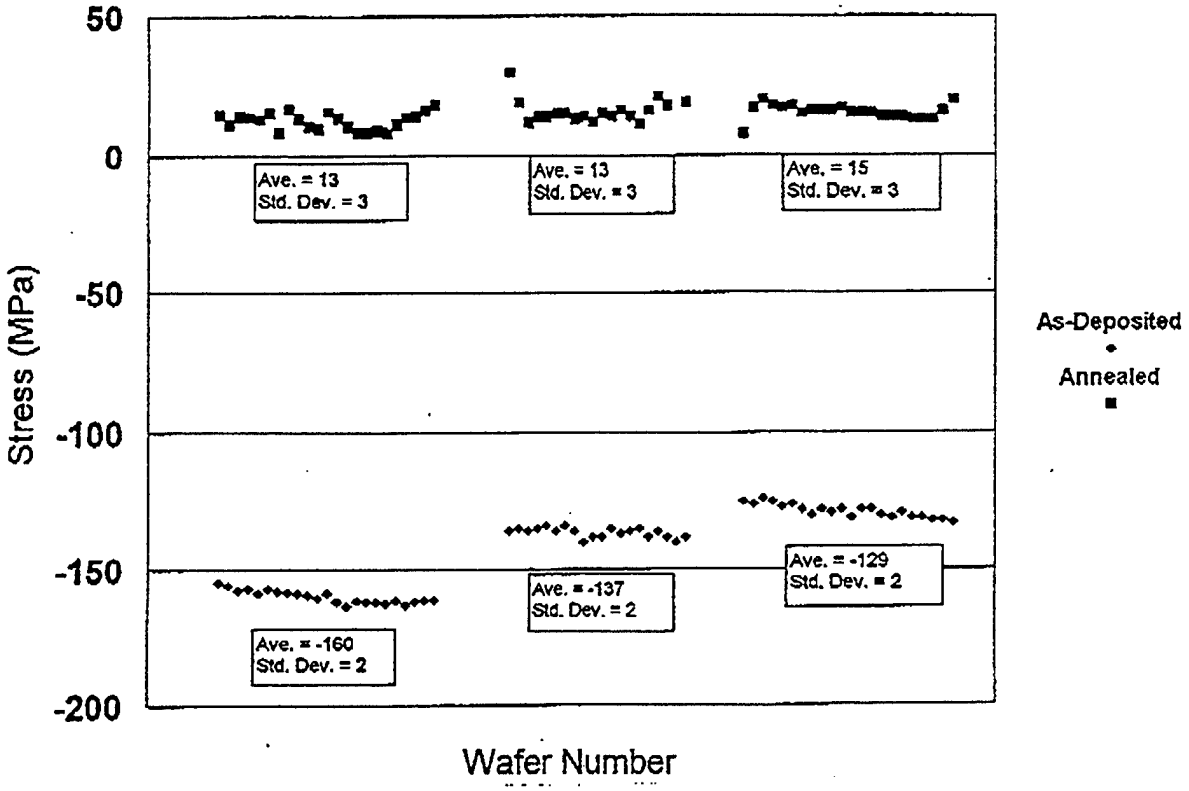


Figure 65. As-Deposited and Annealed Stress for Typical Wafer Lots

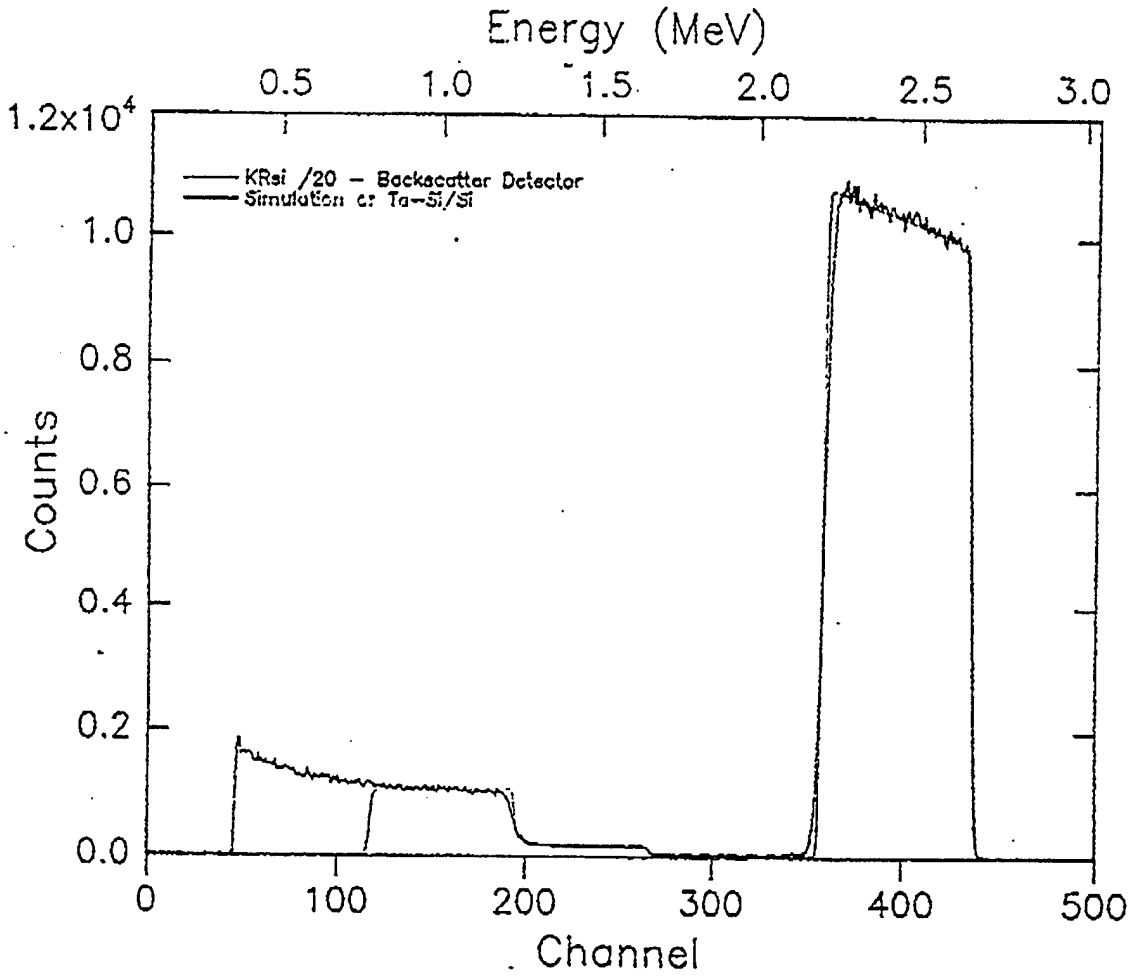


Figure 66. RBS Plot of TaSi Film Analysis

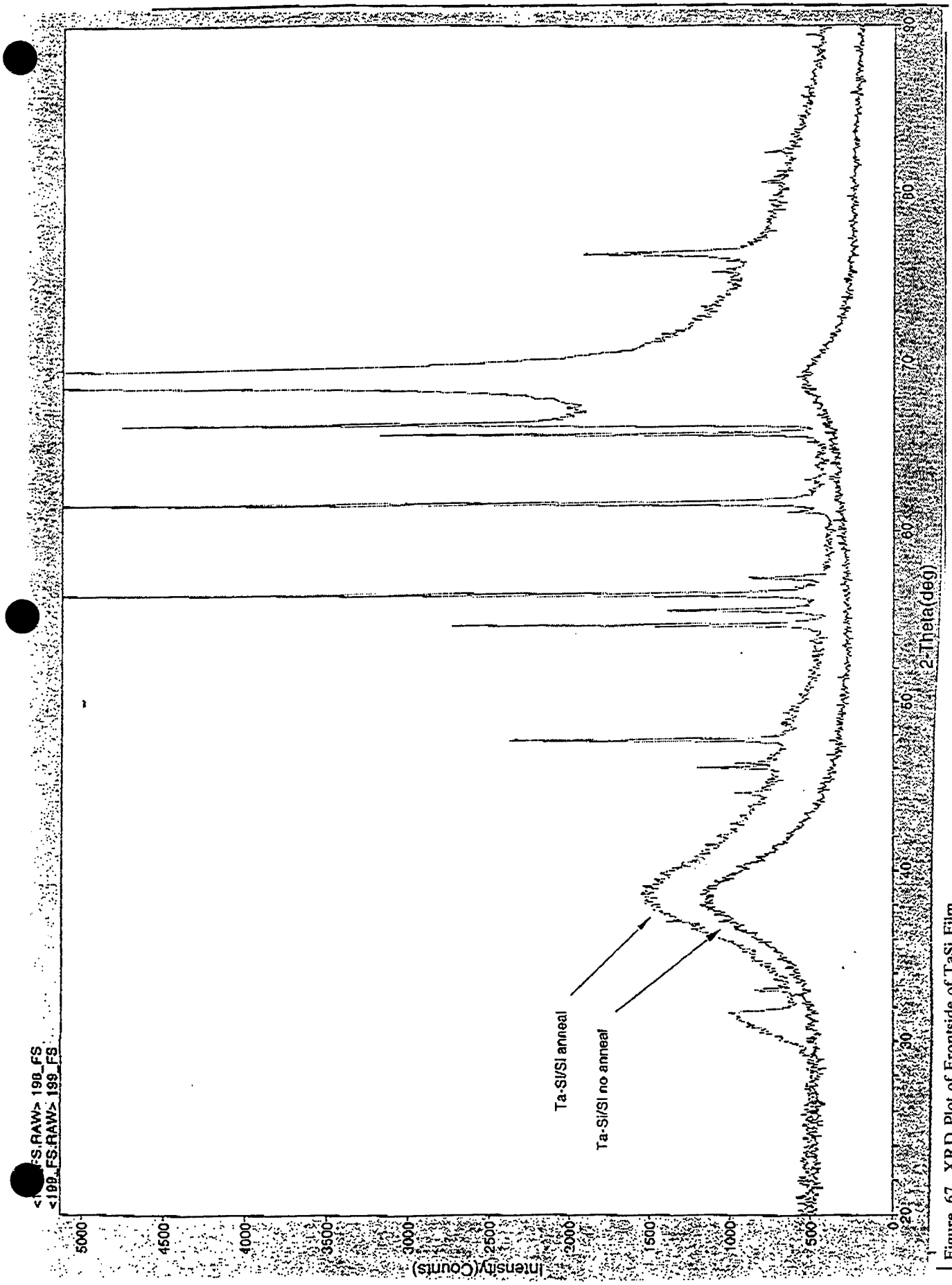


Figure 67. XRD Plot of Frontside of TaSi Film

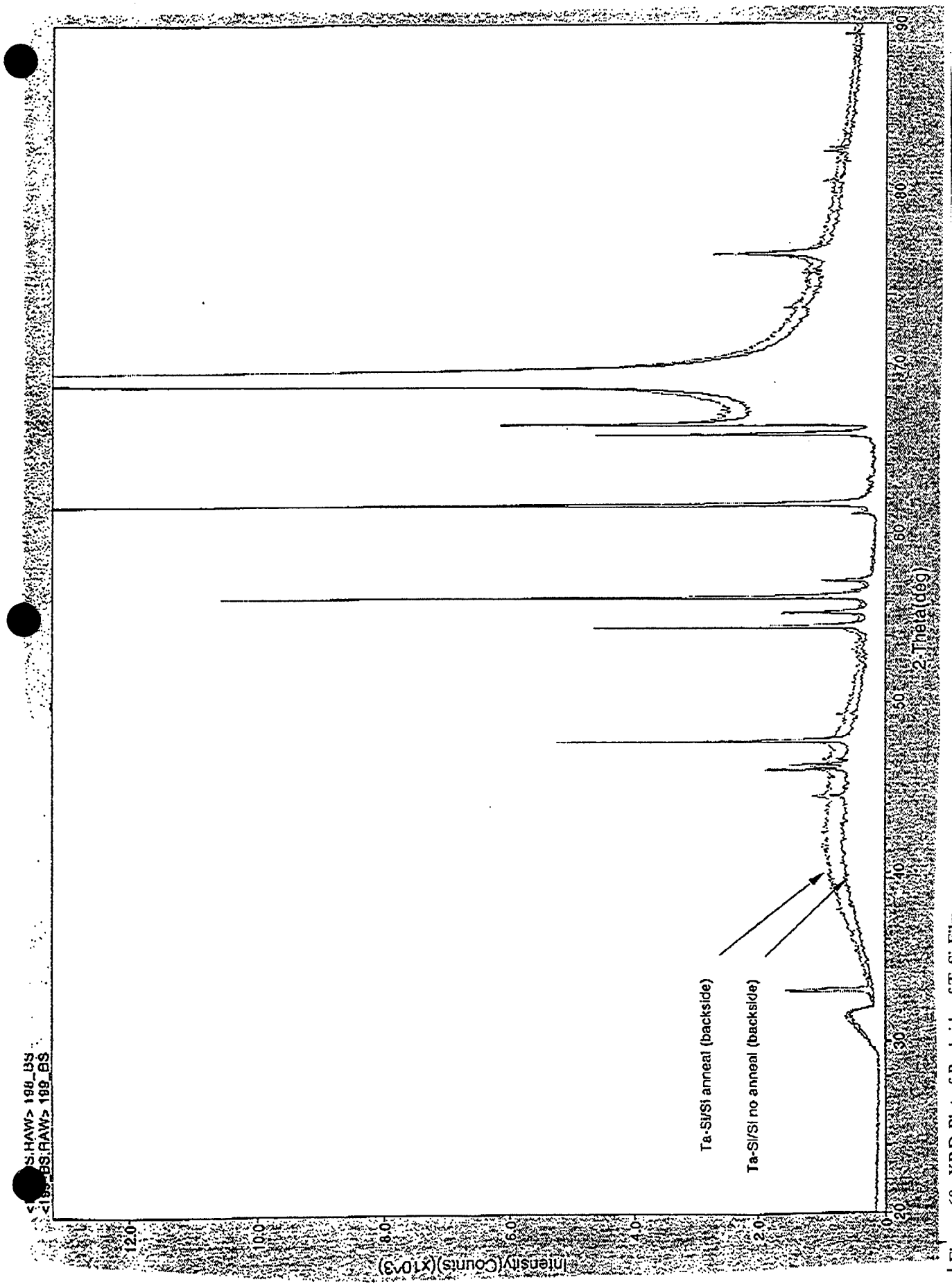
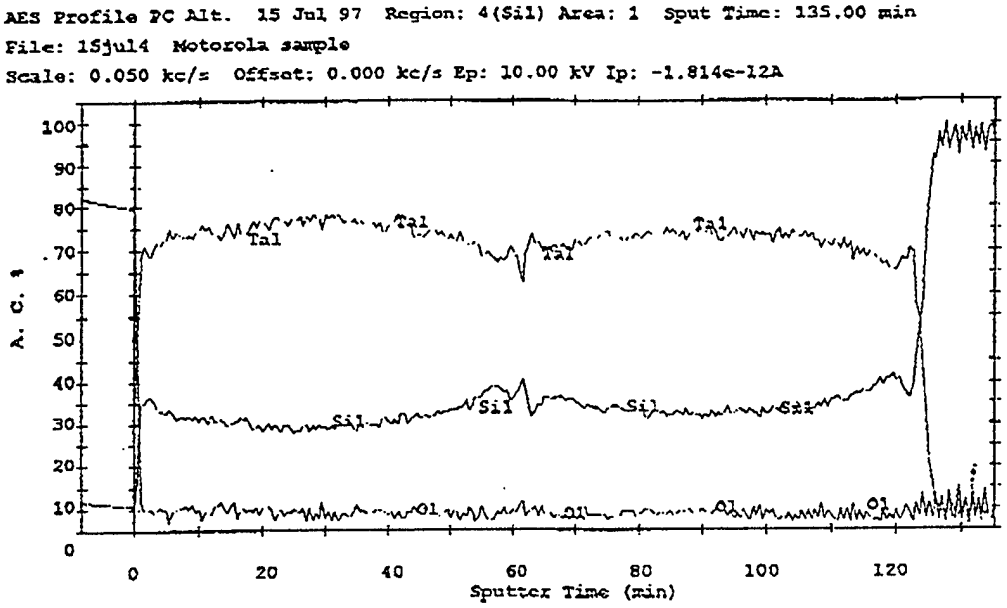


Figure 68. XRD Plot of Backside of TaSi Film

Motorola Sample



MMD Sample

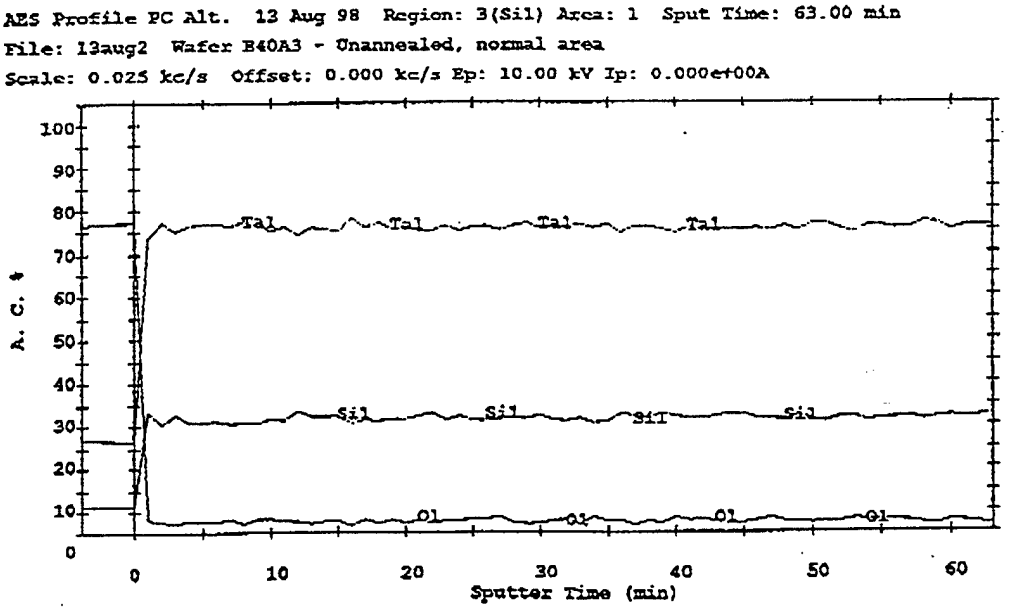
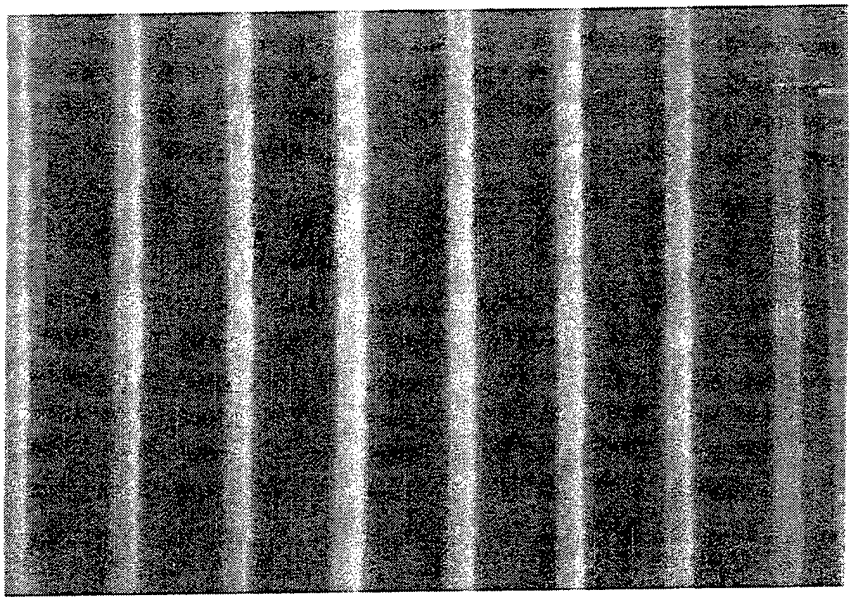
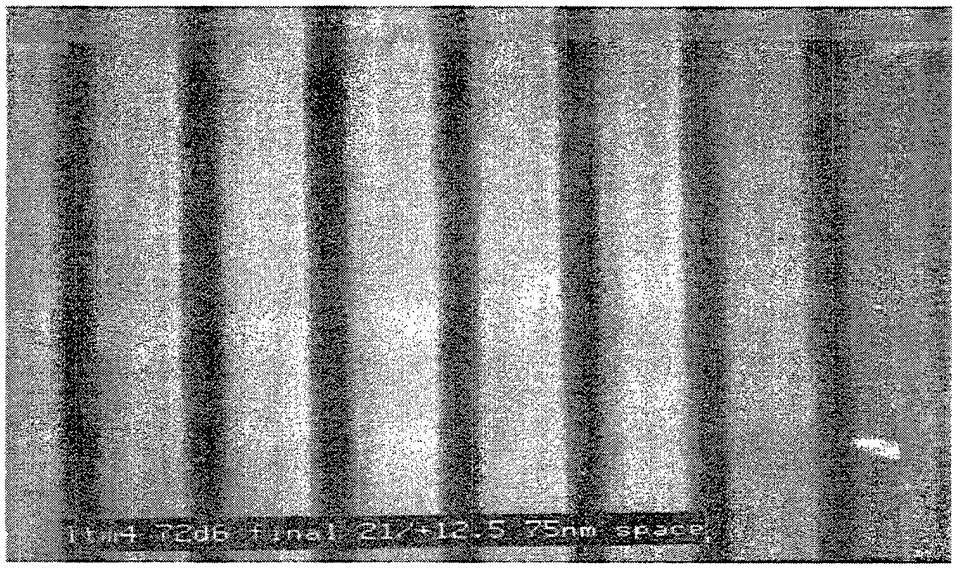


Figure 69. Auger Electron Spectroscopy Profiles. Motorola and MMD Deposited TaSi Film.

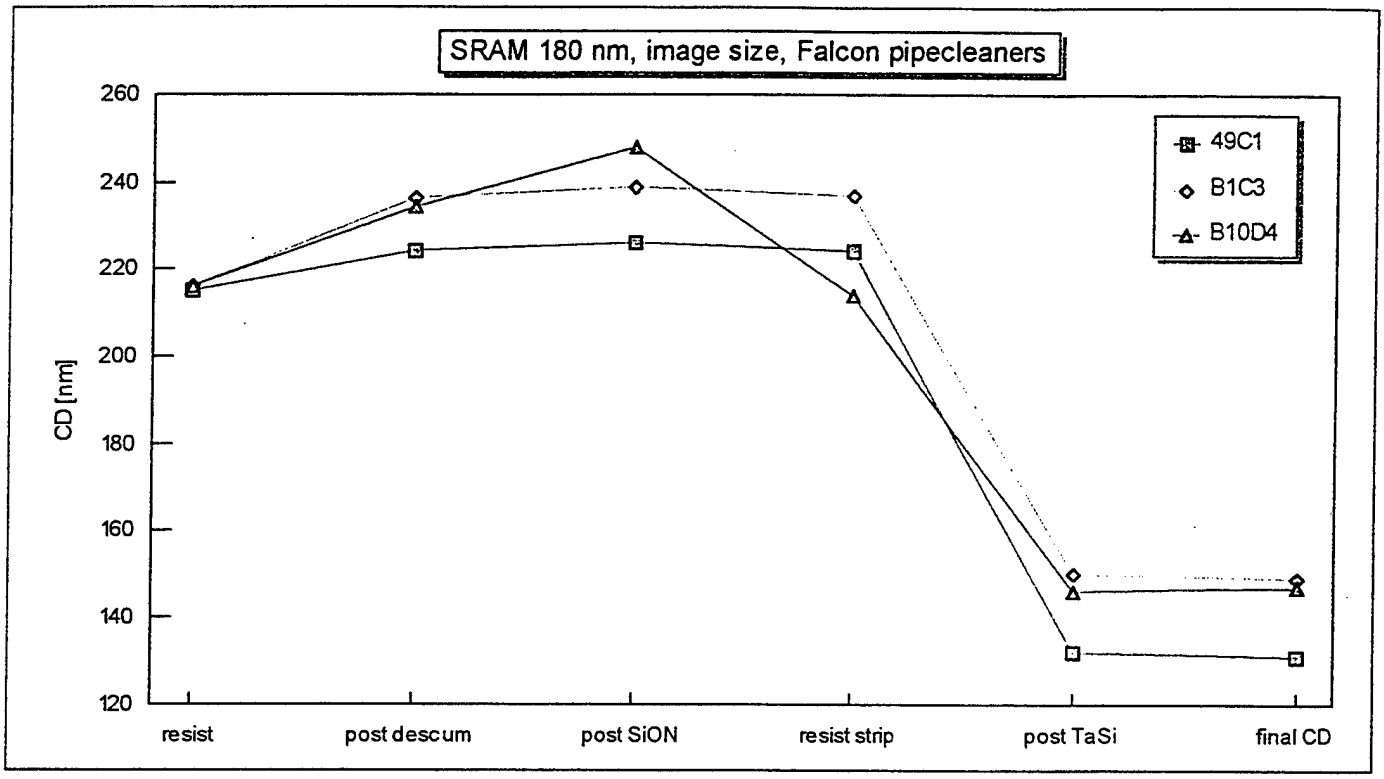


100 nm



100 nm

Figure 70. 75nm Lines and Spaces. Line and space pattern in TaSi formed with UVIII resist.



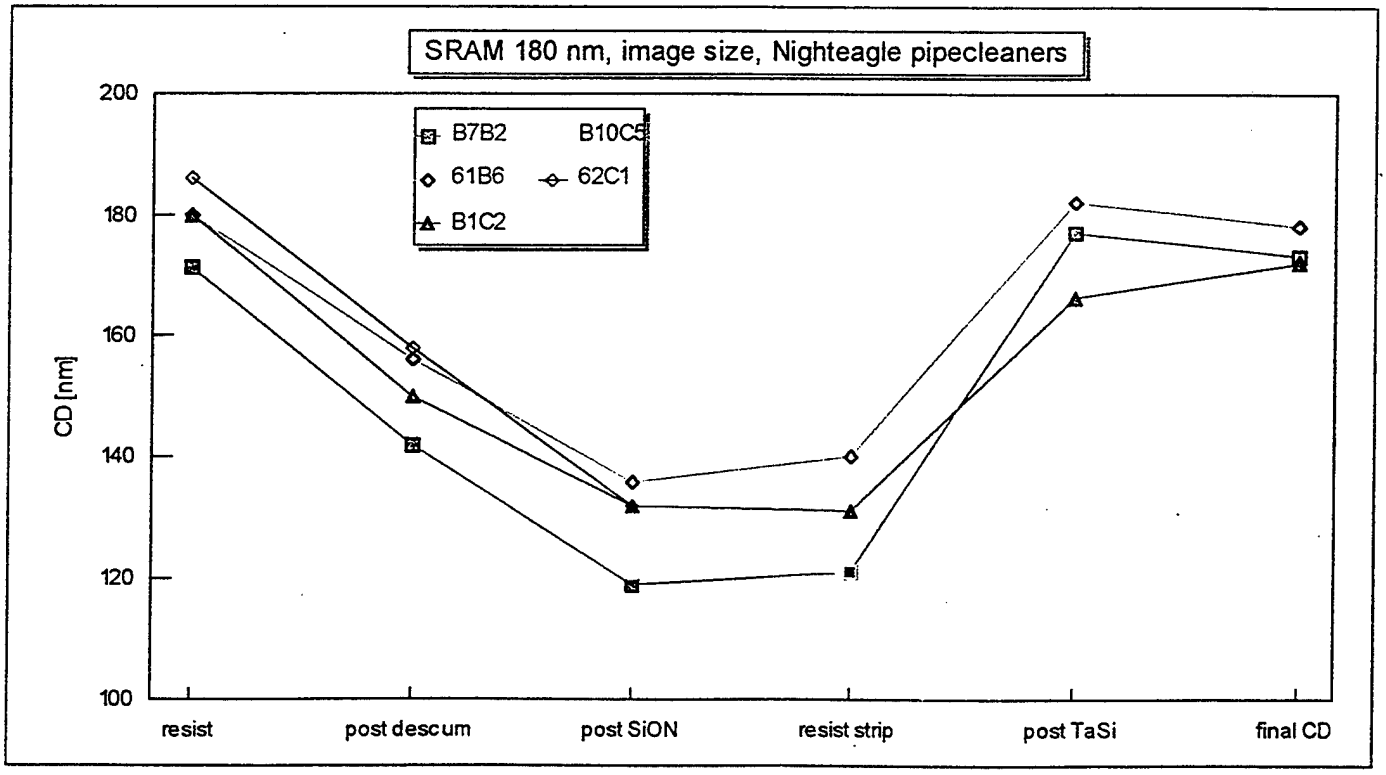


Figure 71. 180nm SRAM Features Sizes by Step

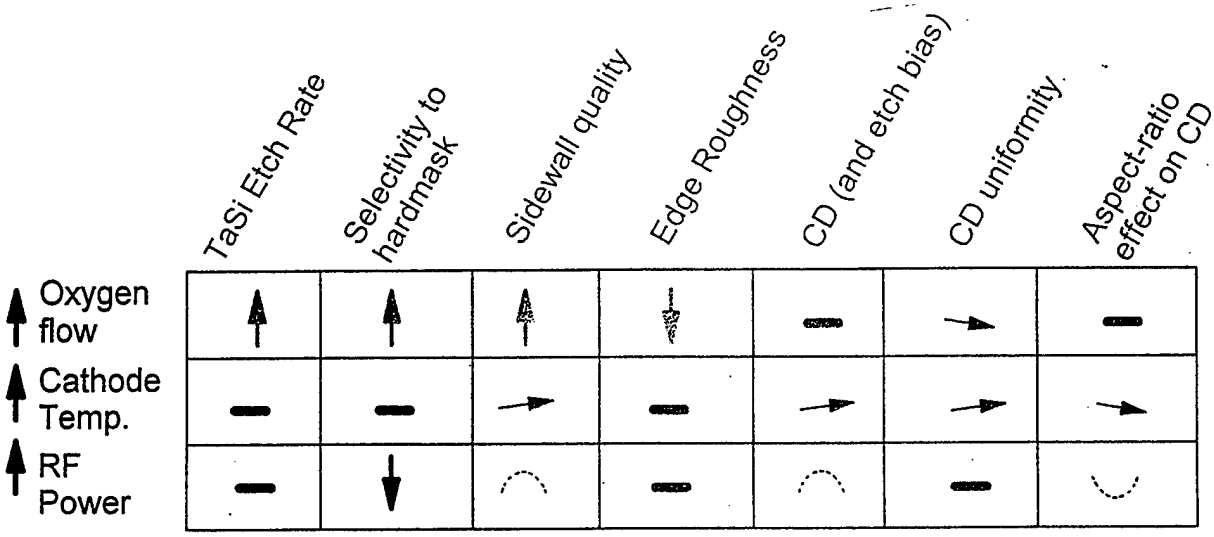


Figure 72. Process Trend Chart from TaSi Etch Experiment. The arrows indicate the change induced by increases in the process variables. For example, increasing oxygen flow increases TaSi etch rate.

7.0 Technical Interchange Meetings (Task 10)

Task Objective: Conduct Technical Interchange Meetings (TIM) for industry and government on a bimonthly basis.

A Technical Interchange Meeting was held during the SPIE Conference in Santa Clara, CA on Friday, February 27, 1998. Presentations were given covering various aspects of x-ray lithography for semiconductor manufacturing. Attendees included representatives from the government, industry and academia. The minutes of the meeting were submitted in accordance with CDRL H002, 98-MMD-LMFS-00022.

A mask modeling workshop Technical Interchange Meeting (TIM) was held on 13 July 1998 at the University of Wisconsin. The meeting coincided with the annual DARPA/SRC Program Review held at the University. The objective of the meeting was to review current x-ray mask modeling work being performed at the University of Wisconsin and to coordinate future x-ray mask modeling-related projects. Attendees included professors and students from the University of Wisconsin, IBM, Lockheed Martin and Sematech representatives, as well as government representatives. The minutes of the meeting, including copies of presentations, were submitted in accordance with CDRL H002, reference 98-MMD-LMFS-00048.

A Business Summit for X-Ray Lithography TIM was held on 28 September in Burlington, VT. The meeting was hosted by SAL, Inc., with attendees from industry and the government. The meeting is documented in CDRL H002, 98-MMD-LMFS-00065.

A TIM was HELD on 07 October at the Naval Research Laboratory in Washington, D.C. to examine the plans in place to continue to provide masks to the government upon termination of the MMD X-ray contract. The meeting was attended by representatives from the government, Lockheed Martin, IBM and Photronics. The meeting is documented in CDRL H002, 98-MMD-LMFS-00069.

A Technical Interchange Meeting on Resists for X-ray Lithography was hosted by Sanders (a Lockheed Martin company) in Nashua, NH on 20 October 1998. The focus of the meeting was an information exchange regarding resist process issues specific to x-ray lithography, and on formulating a consensus on requirements for development and manufacturing of x-ray resist. Attendees included representatives of Sanders, Shipley, OCG, Lincoln Laboratory (MIT), University of Wisconsin - Madison, Lockheed Martin, and ETEC. This meeting was reported in CDRL H002, 98-MMD-LMFS-00082, dated 23 November 1998.

A Mask Distortion Modeling Workshop TIM was held on 29-30 October 1998 at the University of Wisconsin in Madison, WI. The meeting was organized and sponsored by International Sematech. Invitees included representatives from key Sematech member companies, University of Wisconsin students and professors, mask suppliers,

and other associated vendor companies. The purpose of the meeting was to provide member companies, technology champions and suppliers with results of the efforts of the University of Wisconsin Computational Mechanics Center (UW-CMC) and to obtain feedback to improve the models and make them more useful for suppliers. The meeting is documented in CDRL H002, 98-MMD-LMFS-00081

Appendix A - IBM Yorktown Research

Progress Report (12/98), Contract #161783

Introduction

This document provides the data under Contract #161783 in accordance with the requirements of the Statement of Work. It summarizes the work performed through 1998, and covers the reporting period from October 24, 1997 through December 18, 1998.

During this reporting period, activities by IBM Research Division personnel covered a wide range of activities, as described below. They reflect the changes to the Statement of Work for the extension of the contract which was signed on October 22, 1997.

X-Ray Absorber Deposition

Overview

Research Division personnel have provided support to the AMF concerning the deposition of materials used in the mask absorber stack, including hard mask and etch stop layers as well as the absorber material itself. This work has been carried out both in Yorktown Heights, where deposition systems have been used to provide preliminary characterizations of a variety of materials and processes, and at the AMF in Burlington in collaboration with AMF personnel. Work at Yorktown Heights has included development and characterization of stress measurement tooling as well as actual depositions of materials, including TaSi, Ta_4B, and TaGe absorbers and Cr and CrN layers for potential use as hard masks or etch stops. TaSi has been the material used in the Process of Record (POR) in the AMF, while Ta_4B and TaGe are among the materials that have shown promise in development work reported from Japan. In particular, Ta_4B is under development by Hoya, the supplier of SiC mask blanks to the AMF.

Stress Measurements

In applications such as x-ray mask fabrication, it is critical to limit and control the stress in the absorber stack in order to improve image placement and reproducibility. The post-deposition anneal is the favored process to achieve close to zero stress in the absorber layer (<10 MPa). The stress change during these anneals is known to be roughly linear with anneal temperature for compressive films (a few MPa per degree towards the tensile direction for films under compressive stress of a few hundred MPa).

Since the stress of initially tensile films will not decrease linearly and cross the zero point during anneals, it is important to determine the uniformity of the stress through the layer. As an example, if a film showing an average stress as compressive after deposition can be divided into two distinct regions of opposite stress (i.e., a tensile region followed by a more compressive one), the stress change during anneal will be different for each region and globally non-linear through the whole thickness of the film. In order to obtain predictable behavior during post-deposition anneals, it is necessary that the stress be uniform throughout the thickness of the film.

It is therefore very valuable to be able to measure stress *in situ* during the deposition process, so that the stress uniformity through the layer can be assessed. To measure low stress levels during deposition, a new *in situ* monitor for stress (KMOS) was tested on metal sputtering tools. The system is available through K-Space Associates (Ann Arbor, MI) and was on loan to us from the company. Tests were performed both in Yorktown and Burlington and involved the participation of personnel from Yorktown, the AMF in Burlington, K-Space, and SFI (the vendor of the deposition system in the AMF). Although the KMOS system has been already tested during relaxation of epitaxial strained layers in which the coherency strain in the crystalline

overlayers is very large, it is questionable whether system can measure the low stress/thickness combination levels (< 10 MPa-μm) that can be obtained when sputtering polycrystalline metal films under the right conditions of gas pressure and plasma power. The dual goal of this study was to determine if the KMOS system had the sufficient resolution to measure the evolution of stress *in situ* during deposition and if this tool would be of use in the research and development environment in Yorktown and ultimately in the production environment in Burlington.

The physical principle of the KMOS system is the same as the principle used in the Tencor stress tool in that the curvature of the wafer is also measured using the deflection of a laser beam. Two different geometries were used. In the first one, the laser beam passes through a highly reflective etalon that splits the beam into a linear array of parallel beams. The beam spacing is usually around 2 mm and depends on the angle of the etalon. The spacing between the reflected beams is measured using a CCD detector. When the curvature of the wafer changes, the spacing between the beams changes as well. (With two etalons, this array can be transformed into a rectangular one. This geometry has stress mapping capability but has not been tested here.) Since the sensitivity increases with beam spacing, we also used a combination of beam splitter and mirrors to generate two parallel beams with about 30 mm spacing.

(It is important to realize that the technique does not give a stress map of a full wafer but rather, the curvature around the center of the wafer. Even if the measured stress is correlated well with the results from the Tencor tool, the KMOS system is not a substitute for the Tencor tool with its full stress mapping capabilities.)

The two geometries were tested both on the multisource UHV sputtering system in Yorktown and on the SFI sputtering system in Burlington. The evolution of the stress was followed during deposition of chromium (Cr), tantalum boride (Ta_4B) and tantalum silicon (Ta_5Si_3) on Si(100) and chromium-coated boron-doped Si(100) substrates under a variety of deposition conditions, and the noise level of each geometry under different conditions was measured to determine the sensitivity of the system. In the best conditions on the production tool in the AMF, the sensitivity was shown to be sufficient to measure stress levels as low as 2 MPa-μm on a 620 μm thick silicon substrate. This means that the detection limit can be smaller than 4 MPa for a 0.5 μm thick film and about 80 MPa for a 200A thick film. This is definitely sufficient for following stress evolution during the deposition of the Ta_5Si_3 or Ta_4B and studying the influence of various deposition parameters. It was also shown to be useful to compare chromium depositions. With thinner wafers (200 μm thick), this could even be used for tuning the chromium deposition process (resolution of about 8 MPa for 200A).

As a practical matter, the KMOS system is most useful when developing a process. The system would be of particular interest when process conditions for new target material need to be determined. For example, a film that does not show a well-behaved linear change in the beam spacing can be expected to lead to non-reproducible results in the anneal after deposition. The use of such a tool could save considerable amount of time in determining the process window.

For the KMOS system to be of use in exploring alternative materials on the UHV system in Yorktown, it has to be used during substrate rotation. Although the resolution was not as good

as on the SFI system in the AMF, it was sufficient to determine the sign of the stress and the pressure "region" at which films can be deposited with low stress. This would be a definite advantage in the stress characterization of new alloys. With this information, significant experiments can be designed more efficiently.

The KMOS system would allow studies determining the effects of surface preparation (roughness, oxidation levels, cleanliness) on the stress evolution in thin films. Beside the advantage of learning about stress variation during deposition, this system could also be used to deposit a given layer imbedded in a structure with relatively low stress without necessity of breaking vacuum for stress measurement, and therefore without oxygen exposure.

Absorber and Etch Stop Deposition Capability at the AMF, Burlington

The AMF in Burlington, needed to set up a deposition system for the etch stop and absorber layers by year-end 1997. With Ken Racette of the AMF, a specification for a magnetron sputtering, cluster tool deposition was written. Sputtered Films Incorporated (SFI) was selected to manufacture the system. Despite early problems in demonstrating the required absorber stress control, we demonstrated this control with TaSi absorber films during the qualification of the tool at the SFI site in Santa Barbara, California. This was done in a week of experiments at SFI with measurements being done there, at the University of California, Santa Barbara, and at the IBM Almaden and Burlington sites. The deposition system was then delivered to the AMF and was running within two weeks.

All the systematic variation of the TaSi absorber stress with deposition pressure, measured by flow in the SFI system, that was learned in the deposition system at Yorktown Heights was reproduced in this new system. This included the variation in the stress and the stress-anneal dependence with substrate. These properties vary as the substrate is changed from Si, to Cr-coated Si, to Cr-coated B-doped Si.

Sputter Deposition System, Stress Measurement, and Annealing at Yorktown Heights

The cryopumped system with a load-lock and a planetary substrate holder set up in Yorktown Heights has been used to deposit Ta_4B films. This is an alternative absorber material that will subsequently be tested using the AMF deposition system. Initial work has been done in the Yorktown system to learn the variation of the stress and stress-annealing behavior of Ta_4B absorber films as a function of deposition conditions.

The stress in the deposited films was originally measured with a Tencor Flexus instrument. In addition to measuring the stress at room temperature, this instrument can also measure the stress as a function of temperature. Samples can be annealed using two methods: individually in the Flexus stress measuring tool using a He gas ambient, or in batch mode using a tube furnace with an Ar ambient.

It should be noted that we have had an oxygen contamination problem in each of the Yorktown Heights tools used for annealing. In the Flexus, the measured oxygen concentration is 20 ppm; the tube furnace had slightly less oxygen. The result of this oxygen contamination level is that with anneals above at 350°C, the stress becomes more compressive with anneal rather then becoming less compressive. The oxygen concentration levels have very little effect on the measurements below about 350°C. Figure 1 shows the room temperature stress as a function of anneal temperature for two Ta_4B samples with an initial stress of about -330 MPa. The result on the left was annealed and measured by the AMF. The result on the right was annealed in our tube furnace with ~ 5 ppm oxygen contamination. The line is a fit to the data points between 200°C and 350°C. These results demonstrate that the effect of oxygen contamination causes the stress to decrease at anneal temperatures above 350°C. The size of this effect at a given anneal temperature is determined by the amount of oxygen contamination. The AMF result on the left further demonstrates that the stress can be annealed to low levels. The variation in the stress with anneal temperature is linear.

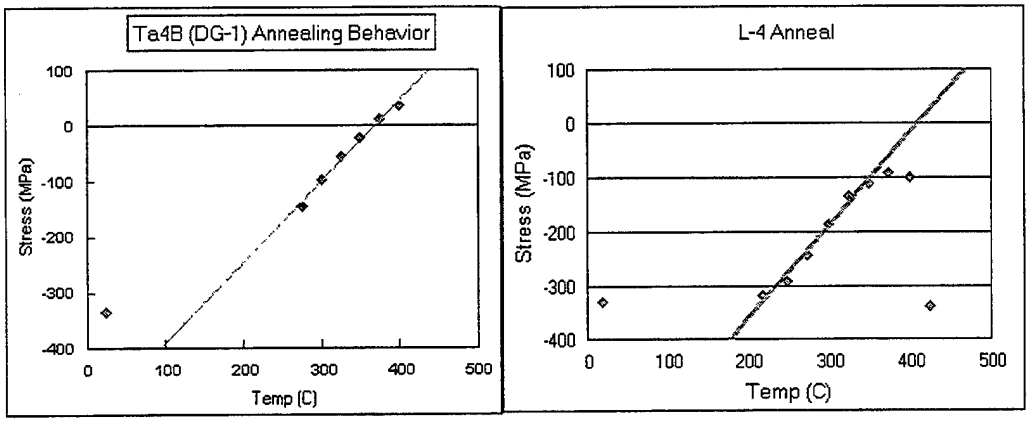


Figure 1. Ta_4B annealing behavior without (left) and with (right) oxygen contamination

To date, with Ta based films, Ta-Si and Ta-B, the compressive stress always decreases with annealing in inert gas ambients. If the stress becomes tensile, the magnitude of the tensile stress increases with further annealing. If there is oxygen in the annealing ambient the stress becomes more compressive with annealing. This effect, with both the Ta-Si and Ta-B material systems, has been observed here. The effect has also been observed by Motorola with the Ta-B system.

To reduce this oxygen contamination, a gas purifier with an oxygen monitor has been installed on the tube furnace. With the purifier on, the oxygen contamination in the exhaust gas is much less then .01 ppb, significantly lower then the 5 ppm without the purifier. Two Ta_4B samples with initial stresses of -150 MPa and + 330 MPa were annealed at both 310°C and 390°C in the oxygen-free ambient. Table I below summarizes these annealing results.

Table I. Stress Versus Anneal Temperature with <.01 ppm Oxygen

	Sample L16 (MPa)	Sample L15 (MPa)
Initial Stress	-149	303
Stress after 310°C anneal	- 29	344
Stress after 390°C anneal	37	359

These results show that as the anneal temperature increases the stress continues be become less compressive and more tensile. If the anneals were done in 5 ppm oxygen, the measured stress after anneal would be move compressive.

In the following discussion, we will ignore the decrease in stress with anneal at the higher temperatures in the presence of oxygen, as this is just a result of our oxygen contamination and is not characteristic of the material.

Ta_4B Absorber Deposition

Figure 2 shows the stress versus anneal temperature for Ta_4B films, with the stress being measured at temperature. The as-deposited stress is -500 MPa. The sample is first heated at a constant rate to 250°C and then held at 250°C for 10 minutes. The initial linear increase in the stress magnitude is due to the differential thermal expansion coefficients between the Si substrate and the Ta_4B film. Between 200°C and 250°C the decrease in the stress is due to the onset of annealing. While held at 250°C for 10 minutes, the stress anneals from -600 MPa to -550 MPa. The sample is then cooled to 40°C with the decrease in stress for this temperature range being due to the differential thermal expansion coefficients. The sample is then heated to 275°C and held at that temperature for 10 minutes. At 275°C the stress anneals to -525 MPa. The sample is then cooled to 40°C again with the near room temperature stress now at -350 MPa. The sample is then heated a third time to 300°C where the stress at 300°C anneals from -525 MPa to --510 MPa. The sample is then cooled to 40°C with the near room temperature stress now being at about -310 MPa. Annealing this sample to 300°C decreased the room temperature stress from the as-deposited -500 MPa to -310 MPa. Furthermore, the stress for the cooling and subsequent heating in the temperature range of 250°C to 40°C is the same, the changes being due to the differential thermal expansion coefficient. This demonstrates the stress is stable, i.e. repeatable, following anneal for temperatures below the anneal temperature. A similar statement can be made for the second cooling and subsequent heating cycle in the temperature range of 275°C to 40°C.

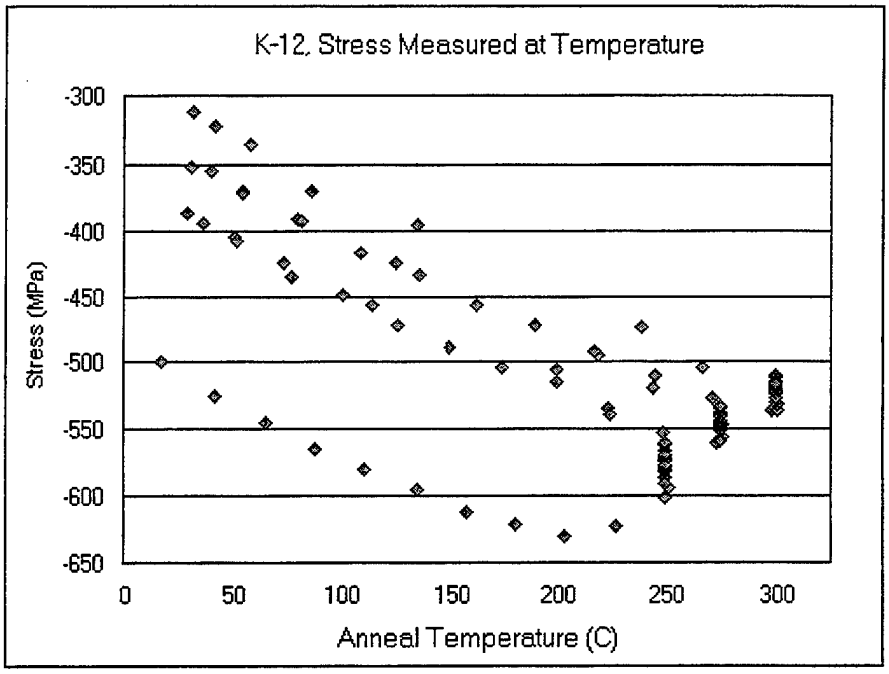


Figure 2. Ta_4B stress, measured at the anneal temperature, over full temperature range.

Table II below lists the as-deposited stress for several different Ta_4B samples.

Wafer ID	Stress (MPa)		Wafer ID	Stress (MPa)
K-7	1,199		L-1	-209
K-16	250		K-18	-296
K-17	112		L-4	-330
K-10	57		L-5	-351
L-3	-9		L-2	-438

For the samples in the above Table, Figure 3 shows the stress as a function of anneal temperature for a limited range of temperatures and for expanded stress scales. Not shown are the higher temperature anneal results where the stress variation is mainly due to oxidation. The plots are ordered from the most tensile to the most compressive as-deposited films. The top four plots use a stress range of 300 MPa while the bottom six plots use a stress range of 500 MPa. The straight line in these figures is the result of a linear fit to the data from 220°C to 350°C. The equations for these fits are also shown on each plot. From these results, one sees the stress is a linear function of anneal temperature over a wide range of as-deposited stresses.

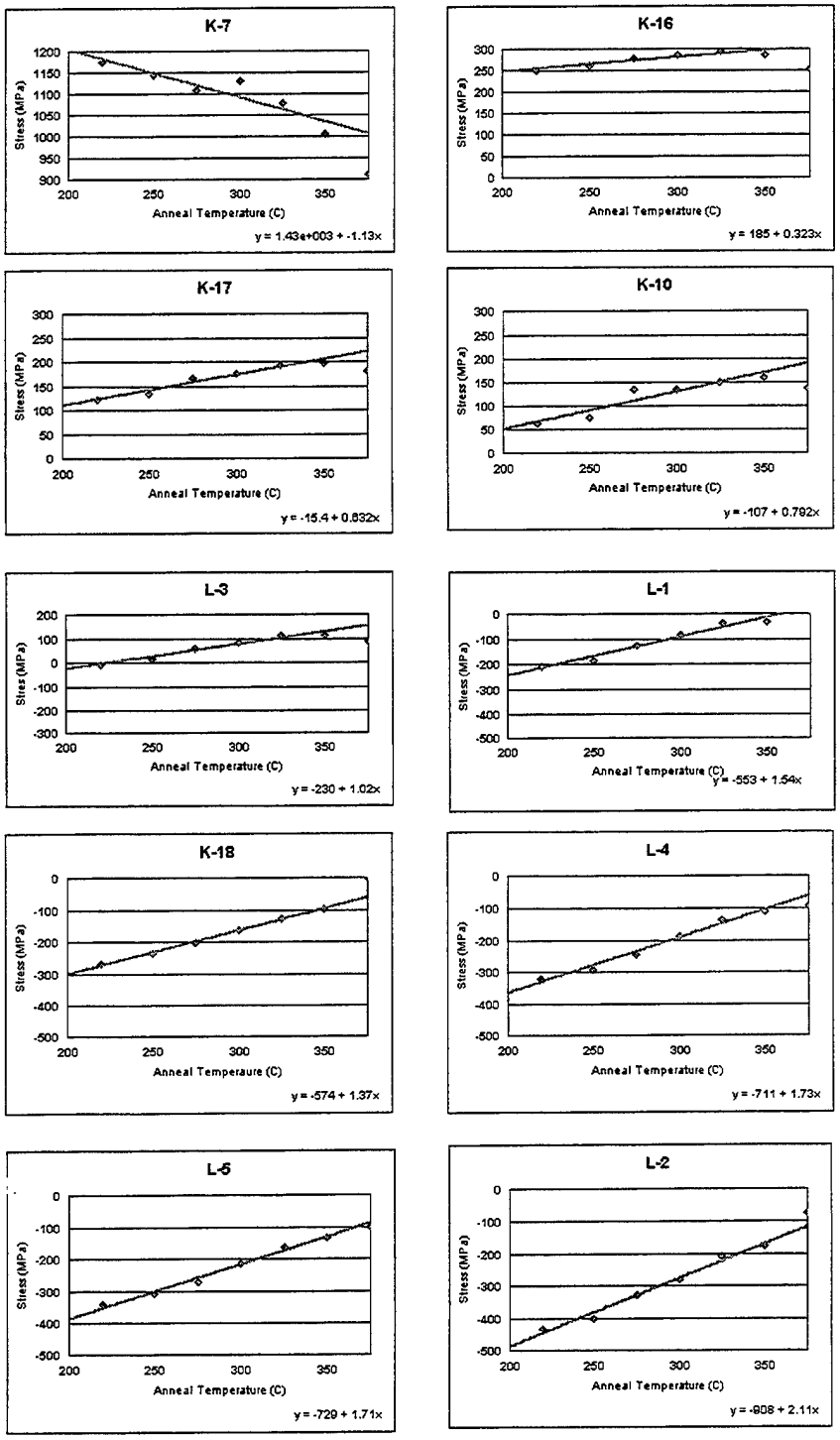


Figure 3. Room temperature stress versus anneal temperature for Ta_4B films with different as-deposited stress.

In Figure 4, the slopes of these linear fits are plotted versus the as-deposited stress over the full range of stress. The change in stress with anneal in larger for greater compressive stress and decreases as the stress is reduced. When the stress becomes tensile, the stress change increases in magnitude with increasing tensile stress. The K-7 film with the +1199 MPa stress is consistent with this result.

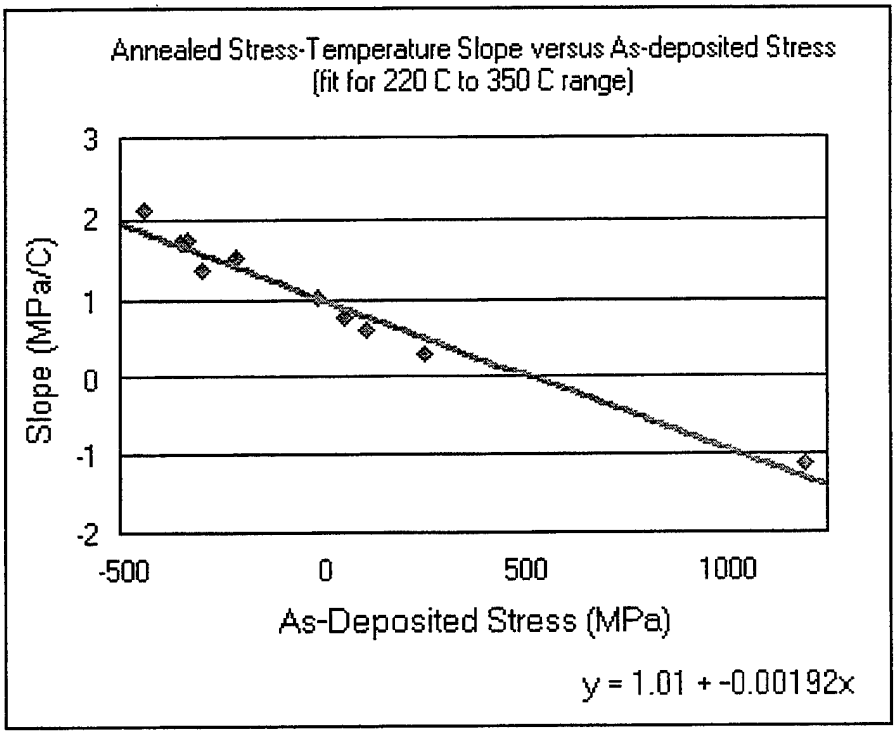


Figure 4. Slope of the stress-anneal temperature versus the as-deposited stress for Ta_4B samples with different as-deposited stresses.

As-deposited Ta_4B Film Stress

The stress of the as-deposited Ta_4B films can be controlled with the deposition conditions. For a fixed sputtering power and Ar gas flow rate, the stress varies systematically with the sputtering pressure, becoming less compressive with increasing pressure. Figure 5 shows the room temperature stress as a function of deposition pressure for 500 nm thick films deposited on undoped Si wafers. For all depositions 1.5 kW was used as the DC sputtering power; power control was used. The open circles and diamonds in Figure 5 should be disregarded, as they correspond to films deposited after exposing the sputtering cathode to atmospheric pressure. Although for these films the cathode was conditioned by sputtering using conditions that worked for the Ta-Si material system, for Ta_4B a longer pre-sputtering time is required. With an additional hour of pre-sputtering, the stress in the films was reduced by

400-500 MPa, resulting in stress that is more consistent with the other results shown. As the pressure is increased from 10 mTorr the stress becomes slightly less compressive. Around 20 mTorr the stress change becomes a more sensitive function of pressure. Our intent was to deposit films that, when annealed, have a final room temperature stress of 1-2 MPa. The anneal temperature would then be used to control the value of the final stress value. This material system is more sensitive then the Ta-Si system.

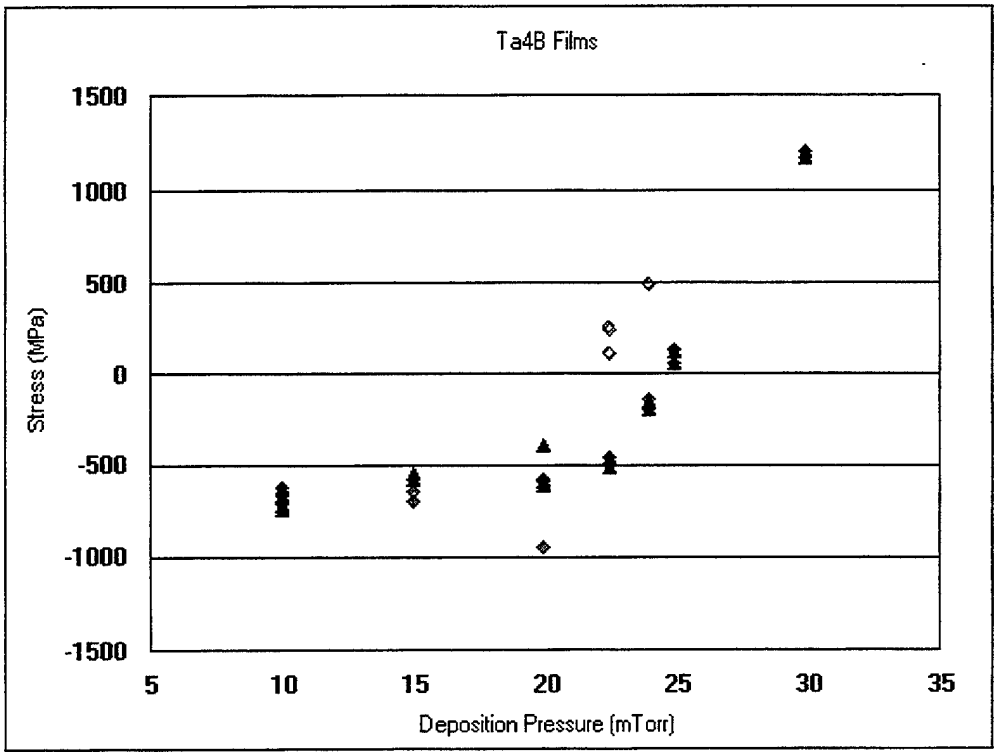


Figure 5. As-deposited stress as a function of deposition pressure for Ta_4B films. The open circles and diamonds should be disregarded (see text).

In the AMF system, only the gas flow (and not the deposition pressure) is measured. The as-deposited stress as a function of argon gas flow for five different sputtering powers is shown in Figure 6. The general trend is that the as-deposited stress at lower flows (which correspond to lower pressures) is -500 MPa compressive for all gas flows. As the flow (pressure) is increased, the magnitude of the stress decreases, actually becoming tensile at the lower sputtering powers and higher gas flows.

Based on the work at Yorktown (and repeated at Burlington), for an anneal temperature of 300°C, the as-deposited stress should be about -300 MPa. This desired 300°C anneal temperature is about 25°C greater then the anodic bonding temperature. If the as-deposited stress is -500 MPa, a higher anneal temperature, >400°C, is required.

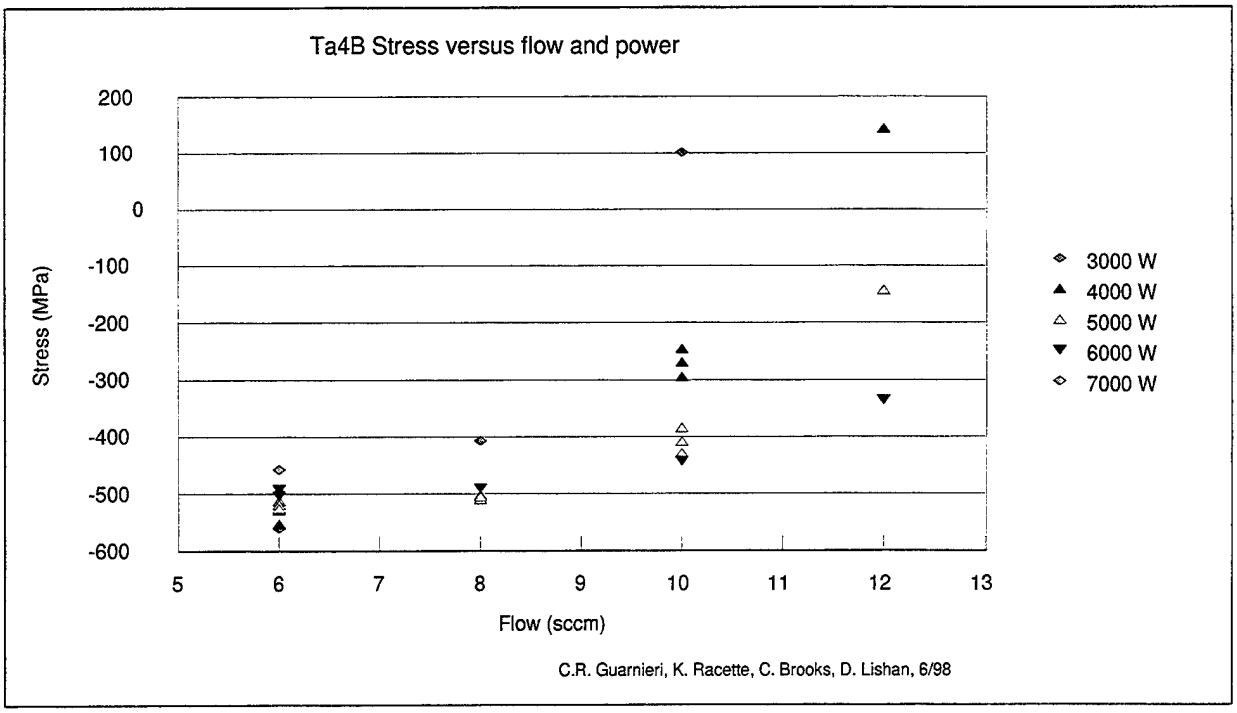


Figure 6. Stress versus Ar gas flow as a function of power of Ta_4B films.

The effects of anode bias and substrate RF bias, both of which have similar effects, were systematically determined. These are controls of the deposition process which are not available on theYorktown system. Figure 7 shows the effects of +60 V anode bias on the dependence of stress on gas flow for two different sputtering powers. Increasing the anode bias increases the magnitude of the as-deposited compressive stress. The RF substrate bias has a similar effect. Increasing substrate temperature also makes the as-deposited stress slightly more compressive.

The general features of the annealing dependence were similar to those determined in Yorktown. The dependence of stress on anneal temperature is slightly sublinear compared to the linear dependence observed in Yorktown; it is suspected that this may be due to oxygen contamination in the annealing furnace in Burlington.

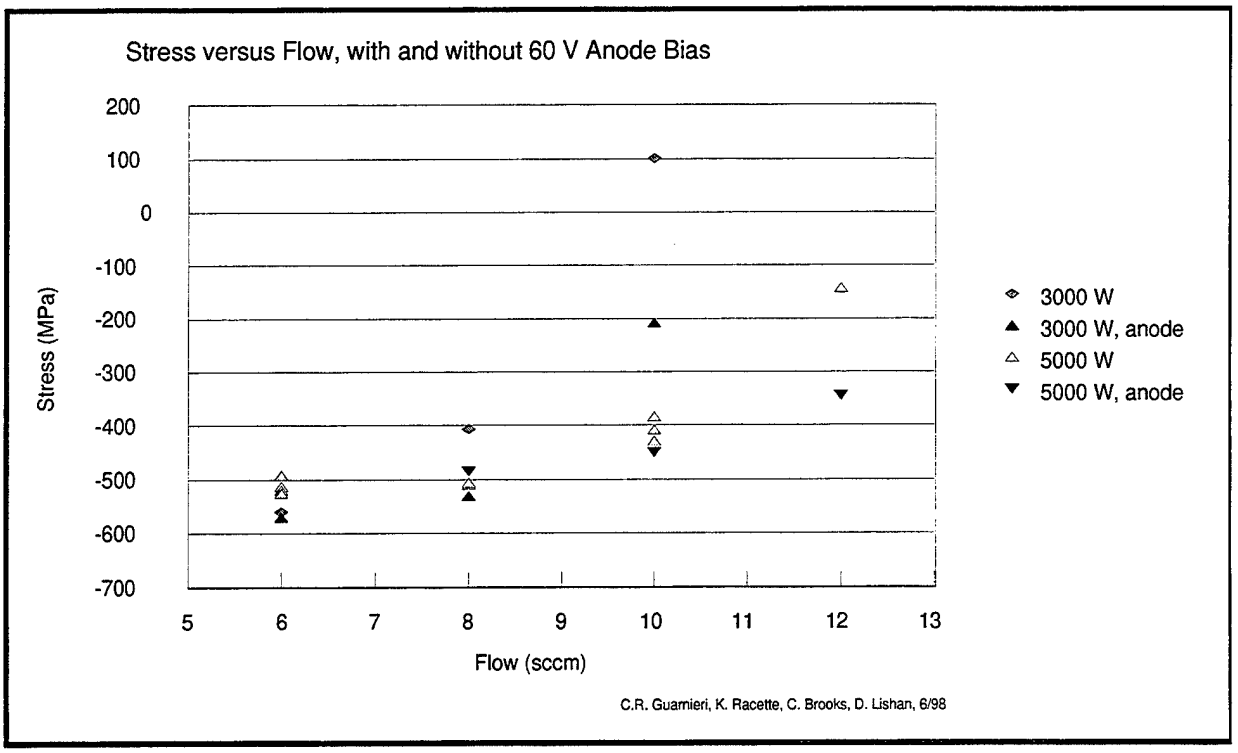


Figure 7. Stress versus flow as a function of anode voltage at 3000 W and 5000W deposition powers for Ta_4B films.

Ta-Ge Absorber Deposition

TaGe is an alternative absorber material for x-ray masks that has shown promising results in work by NEC in Japan. Consequently, it has been deemed worthwhile to investigate its use as a possible substitute for TaSi in the AMF, and development of such films has been undertaken at Yorktown Heights, where films deposited from a $Ta_{0.9}Ge_{0.1}$ cathode are being deposited.

As with the Ta-Si and Ta_4B material systems, the as-deposited stress becomes less compressive with increasing deposition. However, for the TaGe films, the required deposition pressure to obtain as-deposited stress of about -300 MPa, which anneals to -1 to -10 MPa at approximately 300°C is shifted to lower pressure. Figure 8 shows, for a limited number of samples, the variation of the film stress as a function of pressure for films deposited onto silicon substrates using a sputtering power of 1400 and 1500 Watts. A linear trend line is also shown for each of these film sets. The slope of these results is 215 MPa/mTorr. For these $Ta_{0.9}Ge_{0.1}$ films, this slope is more sensitive then that of the Ta-Si and Ta_4B material systems. Thus, in this material system the as-deposited stress is more will be more difficult to control. Figure 9 shows the above dependence for many more depositions. Also included are the results for films deposited at 1,600 Watts. Trend lines are also shown. From these results, we see that, at a fixed pressure, as the deposition power increases the change in the as-deposited stress gets greater.

With the power in the range of 1,400-1,500 Watts there is very little change in stress with a change in power. The slope of the stress-pressure plots is independent of power. The differences in slope in the 1,400 and 1,500 W curves is probable due to the experimental error. The scatter in the data is believed due to the sensitivity is the stress as a function of pressure.

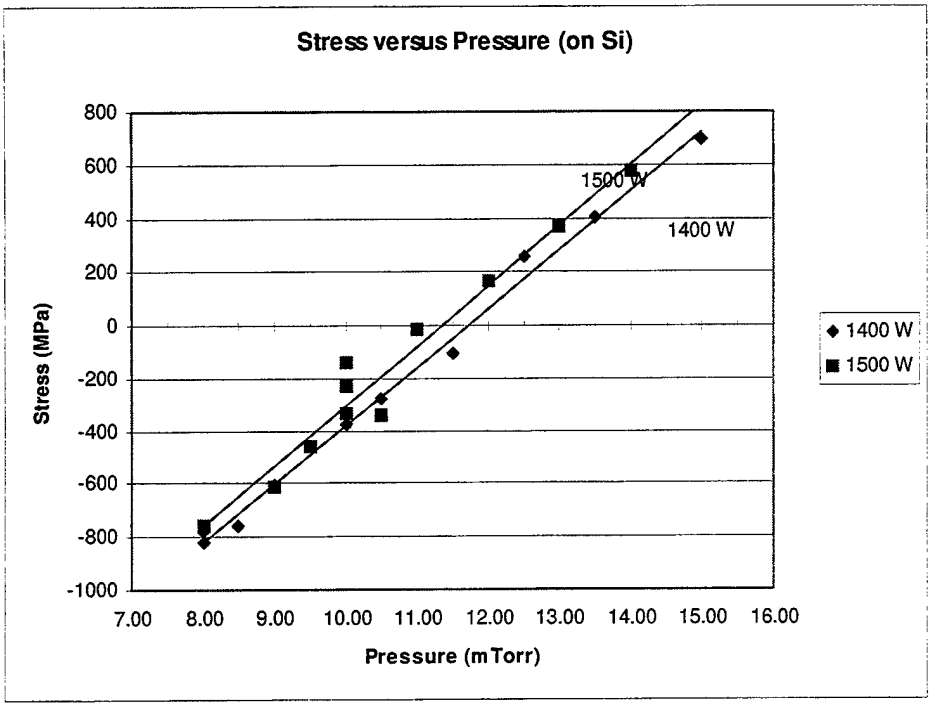


Figure 8. Stress versus sputter deposition pressure for Ta-Ge films for films deposited with powers of 1,400 and 1,500 Watts.

As can be seen in Figure 8, the required deposition pressure is ~ 10 mTorr. By comparison, with the TaSi and Ta_4B material systems, a deposition pressure of approximately 25 mTorr was required to obtain -300 MPa as-deposited stress.

The variation of film stress with film thickness was determined for films deposited using a 10.50 mTorr pressure and 1,500 Watts sputtering power. Figure 10 shows these results. For a film thickness greater then 300 nm this variation is small. Most of the subsequent work was done with a film thickness of 480 nm, the approximate thickness required for an x-ray lithography absorber.

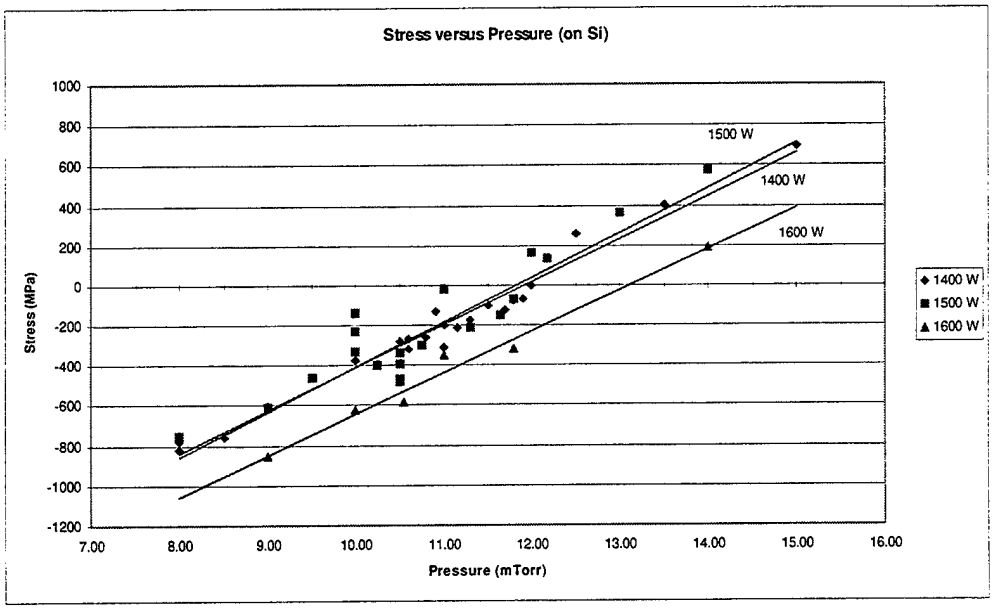


Figure 9. Stress versus sputter deposition pressure for Ta-Ge films.

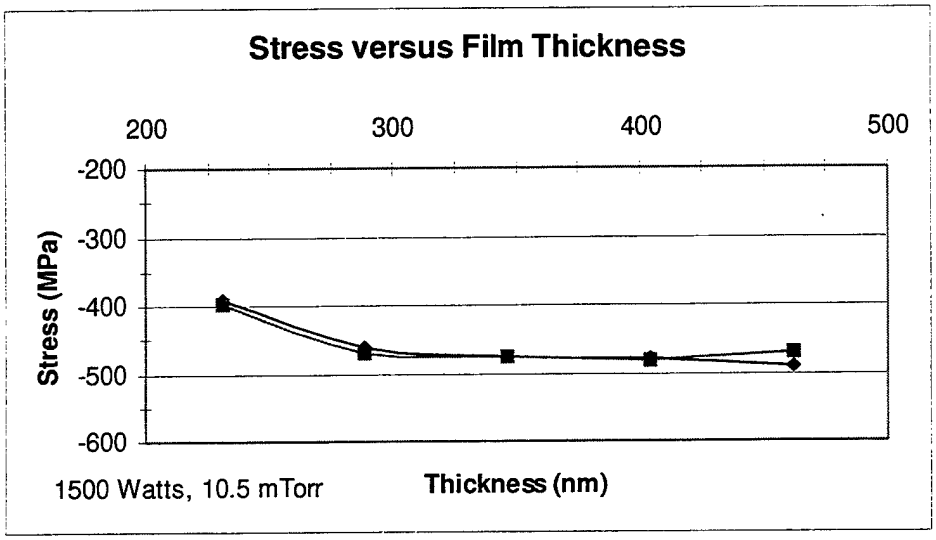


Figure 10. Stress versus film thickness for Ta-Ge films deposited at 1500 Watts cathode power and 10.5 mTorr sputtering pressure.

In the x-ray lithography reticle, a Cr etch stop layer is used on the substrate, under the absorber layer. Previous results with the Ta-Si and Ta-B material systems, showed that the as-deposited stress shifted to slightly less compressive values when the absorber material was deposited onto a Cr film on the Si substrate when compared to depositions on uncoated si substrates. Similar results are measured in the Ta-Ge system. Fig. 11 shows some of these results along with the linear trend lines. For both the films deposited at 1,400 and 1,600 Watts, when deposited onto a Cr film, the stress shifts by about 100 MPa to less compressive values. This shift is relatively independent of the sputtering pressure.

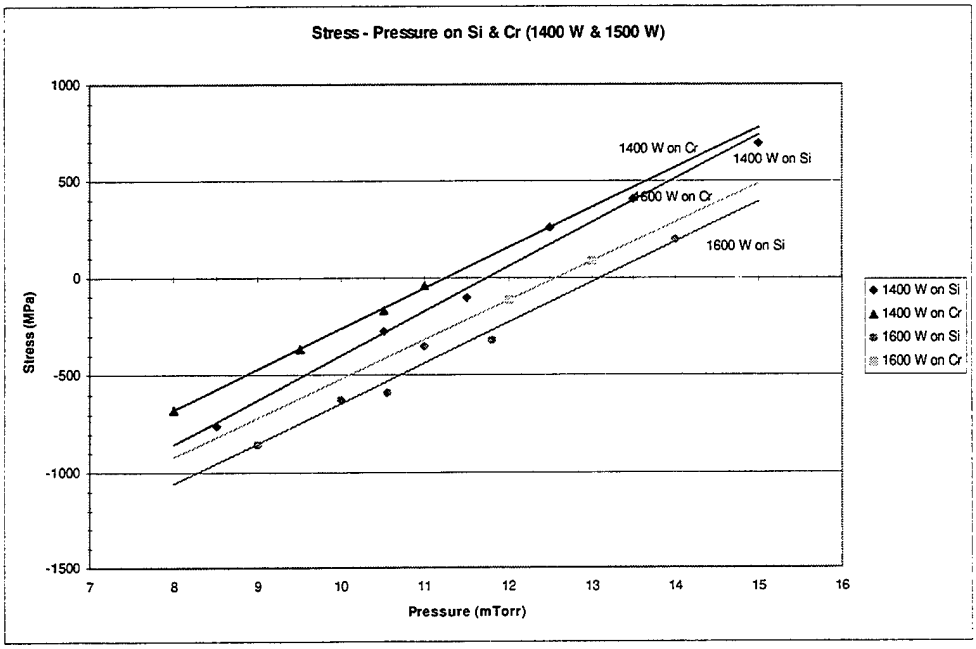


Figure 11. Stress versus pressure for films deposited onto Si and Cr coated Si. Deposition powers are 1,400 and 1,600 Watts.

CrN Reactively Sputtered Films

SiON films are used in Burlington as a hard mask on top of the absorber. These films have a high stress of a few hundred MPa. A lower stress film is desired for this hard mask. The SFI deposition has a Cr sputtering cathode in one of its deposition chambers, so CrN films are being developed as an alternative hard mask material. This material should have a reduced grain size which should make the stress easier to control. It is also expected to be etch resistant in the

TaSi or Ta_4B plasma etching environment. Work has been initiated at the AMF in collaboration with AMF and SFI personnel to develop the conditions for depositing this material. We have been successful in reducing the stress for the +300 MPa to +400 MPa tensile values of Cr to lower values. The stress can even be made compressive.

Dry Etching of Refractory Absorber Stack

The Research Division contribution to etch development has concentrated on providing guidance and consultation to the AMF regarding resist descum and SiON/TaSi etch manufacturability. In particular, focus was on etch biases introduced by each step after resist development (descum → SiON etch → resist strip → TaSi etch → SiON strip) for both Falcon (UVIII resist) and Nighteagle (SNR resist). All of the actual etch work was done in BTV by the AMF team.

The descum step for the SNR was found to decrease linewidth by > 20 nm, and the descum process was shortened to reduce this effect. Significant biases appear to be introduced by the TaSi etch step; however, after careful examination of the data, a significant amount of the bias could be attributed to differences in SEM image sensitivity to the line material (resist vs. SiON vs. TaSi). It is thus quite difficult to ascertain true/accurate biases from each step. This effect may also play a role in the observed nested-isolated feature biases measured for both SNR and UVIII. Nonetheless, the bias is most apparent in SNR, where the isolated lines are relatively more undercut than the nested lines.

Methodologies for manufacturing control are also being pursued in the AMF. These include Statistical Process Control Charts for process variables such as etch time, etc. In addition, some masks will have linewidth measurements taken at several points in the pattern transfer process into TaSi to track possible process drift and potentially trigger tool maintenance procedures.

Further details of the work conducted by the Research/AMF team will be reported by the AMF. It should also be noted that the AMF is switching from the use of SNR to UVN-2 resist.

Electron Beam Resists

Work has been carried out on ZEP 7000A, a commercial non-chemically amplified resist. ZEP exhibits excellent resolution down to 100 nm or below (see section of this report on VS5 X-Ray Mask Fabrication below) but generally has low contrast (<2) and quite a bit of thinning when developed with the developer recommended by the manufacturer. Solvent mapping studies were done to understand the solvent characteristics of ZEP. Using these studies, a number of improved developers were found which exhibit better performance. One developer in particular gives excellent performance with similar resolution to the vendor-recommended developer (100 nm) but exhibits 40% less thinning than with the recommended developer.

Furthermore, the post-apply bake (PAB) sensitivity of the material has been studied. It was found that above 200°C, the polymer degraded resulting in a decrease in molecular weight. The optimum bake temperature was found to be 180°C.

The etch resistance of ZEP has been found to be dramatically improved by the incorporation of several types of organometallics. Standard ZEP etches at a rate of 1403 Angstroms/min, whereas the modified ZEP materials etch at significantly lower rates of 1038-655 Angstroms/min (with the actual rate dependent on the specific organometallic and the amount of organometallic). The modified ZEP materials actually etched at a slower rate than novolak based resist (1125 Angstroms/min).

However, it was also found that the organometallic must be chosen carefully to maintain the lithographic performance of the resist. Many of the organometallics were found to come out of the film during the resist bake (at 180°C). TGA/Mass Spectroscopy and Rutherford Backscattering measurements were performed to deduce the distribution of the organometallic in the film at a variety of temperatures. From this study, a number of additives were selected which blended well with ZEP and remained in the film after Post Apply Bake (PAB) and Post Expose Bake (PEB).

The original material chosen was found to result in a significant post apply bake (PAB) sensitivity. We therefore carried out studies to understand the reason for this impact on PAB. By running gel permeation chromatography (GPC), it was found that this additive resulted in chain scissioning of the resist yielding lower molecular weight. We also found a second organometallic additive which gave excellent etch resistance but did not result in a PAB sensitivity. GPC confirmed that this additive did not catalyze the degradation of the molecular weight of the resist. Lithographic studies were carried out on this formulation and it was found that 130 nm line/space patterns were resolved on a 50 kV tool. The image quality was excellent, resulting in very square profiles which were better than those observed with ZEP alone. We believe this latter result is due to the additive also acting as a dissolution inhibitor.

Studies were also carried out to determine if the additive was removed from the resist during the develop process. Two films (one exposed to developer and one that was not) were examined using Rutherford Backscattering. It was found that the organometallic was not leached

out of the film by the developer. Thus, this organometallic/ZEP formulation gives excellent combination of lithography and etch resistance.

VS5 X-Ray Mask Fabrication of 75 nm Line/Space Patterns

VS5 Probe Size at 100 kV

The beam size was measured in VS5 by scanning the beam at a calibrated scan speed across a cleaved GaAs edge while recording the transmitted electron signal, as shown in Figure 12. For a Gaussian beam current distribution the 12% and 88% points on the signal's rising or falling edge mark the full width at half maximum (FWHM) of the current distribution, which is the value commonly used for the beam diameter. For beam currents in the range of 0.5 - 2 nA at 100 kV beam voltage the minimum beam diameter in VS5 is in the range of 30 - 35 nm.

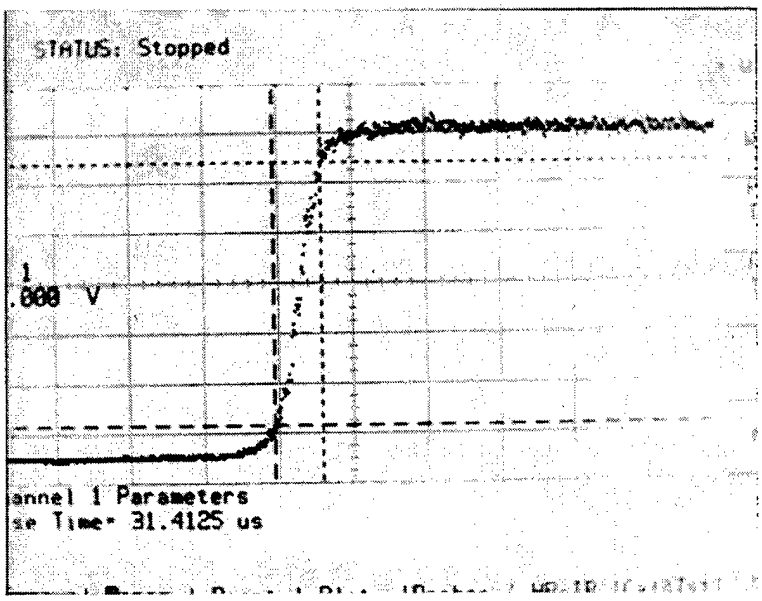


Figure 12. Oscilloscope recording of the transmitted electron signal while scanning the beam at 1 mm/s across a GaAs edge. The signal rise time measurement indicates a beam diameter of 31.4 nm FWHM.

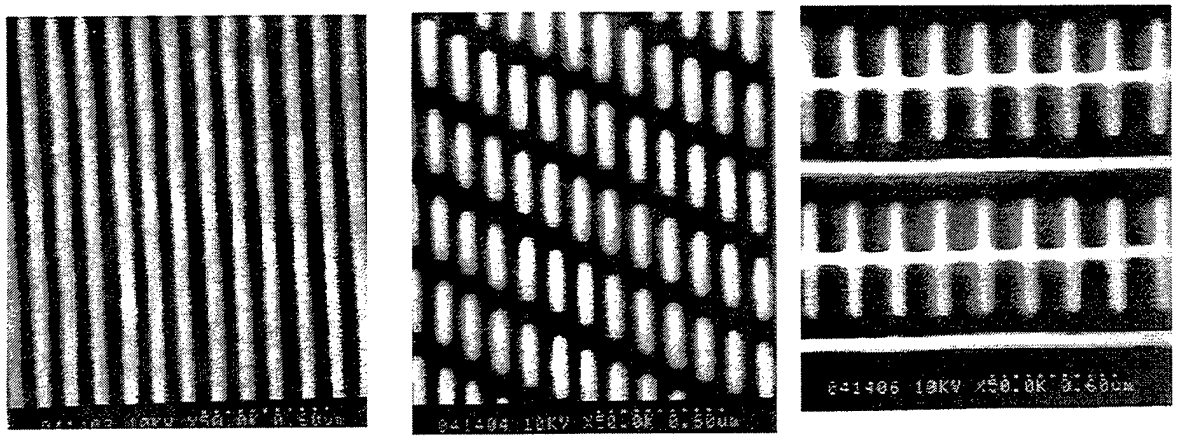
X-ray Mask Deliverables

During the reporting period three device masks (PlutusII), for fabricating CMOS devices at channel lengths below 50 nm, and three test masks (LTM-4), for studying the extendibility of x-ray lithography printing to 70 nm line width, were delivered to ALF. The PlutusII mask design consists of the P1 level test site for the devices, the chip kerf, and the necessary SVGL alignment marks to allow for mix-and-match lithography between the optical stepper and the P1 level exposure in the x-ray stepper. The original testsite design contained a large number of shape overlaps which had to removed before e-beam exposure. The pattern is proximity effect

corrected, and an edge bias is applied to optimize the electron beam exposure for all shapes with minimum dimensions of less than 125 nm.

The LTM-4 mask design contains a large variety of high resolution patterns with minimum dimensions in the range of 75 - 175 nm in 25 nm increments. The design also contains grating and brick patterns with 75 nm minimum linewidth which extend across the full 2 mm chip size and can therefore be easily be used for cross-section SEM imaging.

The mask patterns were exposed at 100 kV in 400 nm thick PMMA on boron-doped silicon membranes. After optimizing the exposure dose, the edge bias, the resist development, and the descum etch parameters, 300 nm of gold were plated into the resist patterns with line width very close to nominal. Figure 13 shows SEM images of the gold absorber patterns on one of the LTM-4 masks. The line width was measured in a Hitachi CD SEM in ALF and the results are summarized in Table III.



A B C

Figure 13. Images of the gold absorber patterns on LMT-4 mask #B11A-2: (A) 75 nm line/space pattern; (B) brick pattern with 150 nm pitch; (C) gate pattern with 75 nm lines and 150 nm spaces.

Table III: Line width measurements from LMT-4 mask pattern using a Hitachi CD SEM.

	Nominal Linewidth	Measured Linewidth
Line/space pattern	75 nm	76 nm
Brick pattern	75 nm	80 nm
Gate pattern	75 nm	73 nm

Results from printing these masks in ALF were compared with modeling of the x-ray lithography resist exposure at linewidths below 75 nm, including diffraction effects. The results of the comparison indicate that a thinner gold absorber should yield higher resolution printed resist lines. For x-ray mask making, the use of a thinner gold absorber also allows the use of a thinner resist, thereby decreasing the effects of beam broadening from forward electron scattering during the electron beam resist exposure. As a result, it is expected that using 300 nm thick resist in the VS-5 e-beam mask writer to fabricate an x-ray mask with a 200 nm thick absorber will result in less than 60 nm minimum linewidth in the plated absorber pattern. Such a mask would be very valuable for extendibility studies.

A new LTM-4 pattern mask with a 200 nm thick gold absorber has therefore been fabricated using VS-5. Figure 14 shows SEMs taken at a 45 degree angle of a 75 nm line/space pattern in 200 nm of gold.

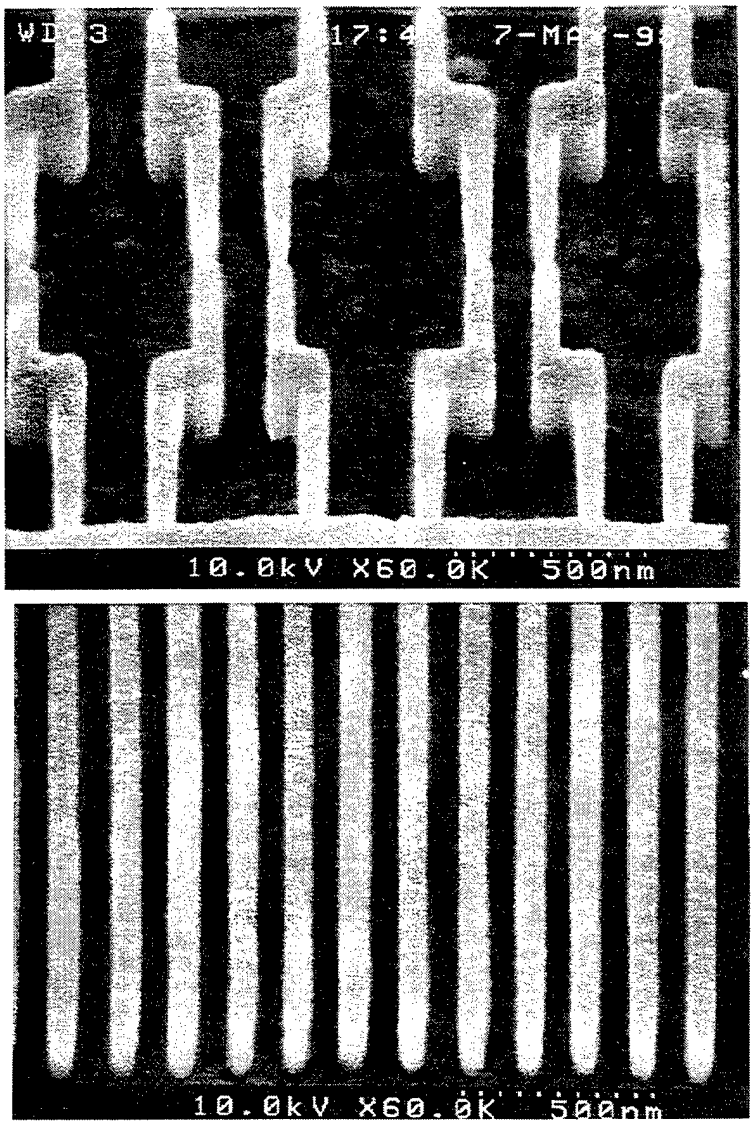


Figure 14. SEM images of 200 nm thick gold absorber pattern taken at 45 degree angle tilt.

Resist Process Development

For subtractive pattern transfer, such as reactive ion etching (RIE), PMMA resist suffers from a relatively high etch rate and, therefore, poor selectivity to the substrate etch rate. A resist material with a reportedly better etch selectivity (see section on Electron Beam Resists above), is ZEP 7000 from Nippon Zeon Co., Ltd, which has an etch rate closer to that of novolak based photoresists. ZEP 7000 resist was spin coated on silicon wafers at 1000 rpm which results in a film thickness of 334 nm after a short post apply bake at 200 C for 2 minutes on a hot plate. The wafers were exposed in VS5 at 100 kV and developed for 15 s in hexyl acetate. The measured contrast curve is shown in Fig. 15. With a large area clearance dose of 350 $\mu C/cm^2$, the resist is almost a factor of 2 more sensitive than PMMA and shows a similar gamma value of 4.9. Fig. 16 shows a grating pattern with 150 nm period. The exposed lines have a linewidth close to 50 nm.

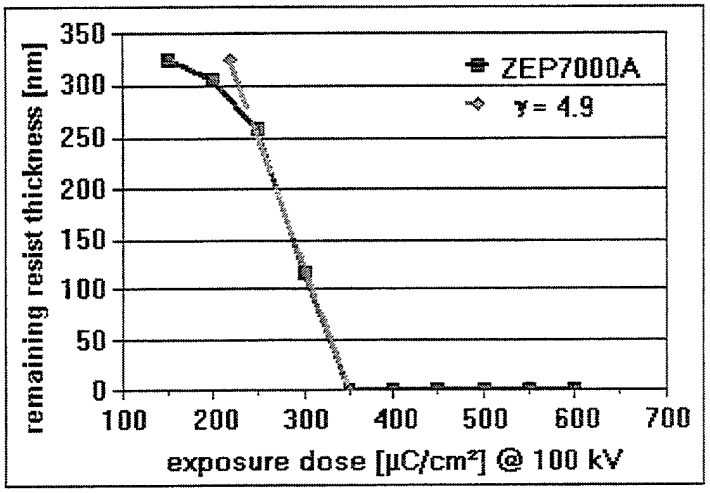


Figure 15. Contrast curve for ZEP 7000 resist exposed in VS5.

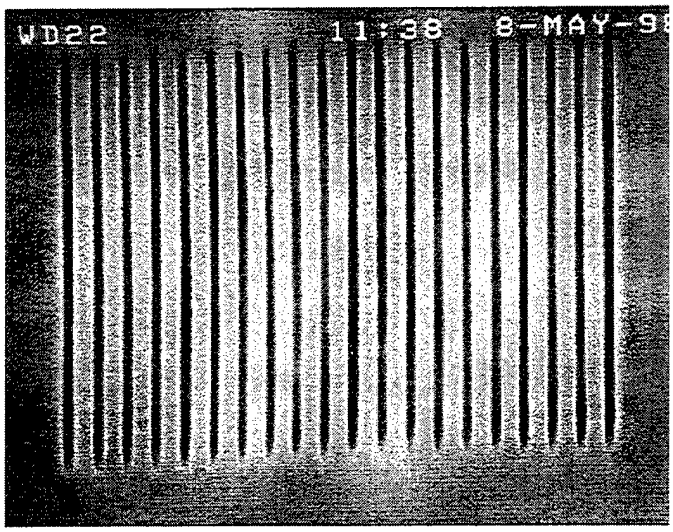


Figure 16. SEM image of 150 nm pitch grating pattern exposed in 334 nm ZEP 7000 resist at 100 kV.

X-Ray Mask Protective Covers ("Pellicles")

Testing of radiation hardness of potential materials for mask protective covers ("pellicles") has been carried out. Inorganic films (SiN) as well as organic films (a variety of polyimides) were tested in an accelerated fashion by localized irradiation in ALF-1, the radiation testing beamline. The polyimides offer the advantage of being low cost and more flexible, which would permit mounting over the edge of the mask. The SiN films are, however, were expected to be superior with regards to radiation damage.

The particular polyimide (PI) materials were chosen based on consideration of their chemical structure and/or use of solvent. As expected, it was found that SiN films have the highest radiation stability (no evidence for radiation damage up to a dose of 130kJ/cm^2 was observed at which point the experiment was stopped). The radiation damage of polyimides was found to depend on the particular polyimide. Dupont 2611 was less stable (<10kJ/cm^2) than was Dupont 5879 which survived up to 30 kJ/cm^2 without breaking, but with considerable darkening in color. The 2611 is a more rigid polyimide as compared to the 5879 which contains flexible units in the form of oxydianiline. From the present results, it appears that the more rigid structure is more susceptible to radiation damage potentially due to stress build up in the film upon irradiation.

Irradiation of vapor deposited Parylene films has also been conducted. Free-standing films were spot irradiated to 20 kJ/cm^2. A noticeable color change was observable at 5 kJ/cm^2. At 20 kJ/cm^2 the film broke, apparently as a result of its having become brittle. Further studies are underway to see if the radiation stability of Parylene can be enhanced by appropriate substitution of the polymer backbone.

A separate concern with the use of the polyimide is whether any outgassing occurs, such as amine evolution during radiation exposure which could contaminate the resist and have an adverse impact on its imaging. To investigate this issue, a very sensitive chemically amplified resist (APEX) has been used to highlight any contamination. Apex samples were exposed using standard conditions in the SVGL stepper. Before post-exposure bake (PEB) the samples were promptly exposed to various doses of X-rays in close proximity to the 5879 PI film, with a metal grid shadowing the exposure. In this way any contaminating volatiles released from the PI would be expected to diffuse into the adjacent (unexposed) resist areas. The samples were subsequently processed through standard PEB and developed. Controls consisted of paired wafer samples, as well as of fields exposed on the same wafer that were not exposed in contact with the PI. The initial results showed that the protected areas of Apex adjacent to the areas exposed to PI were grossly overdeveloped. At very high X-ray doses, this effect extended even to the control chips. Our conclusion is that an unexpected, apparently acidic compound evolves during PI exposure. The effect of this contaminant is to speed up the resist, making control of the exposure dose extremely difficult.

These results suggest that further emphasis needs to be placed on inorganic films for use as protective covers.

Program Management Support

Program management support has been provided during this period, including:

- Management of contract activities in Yorktown Heights, including generation of progress reports
- Program management helping coordinate activities in Burlington, East Fishkill, and Yorktown Heights
- Representation of X-Ray Lithography as Technical Champion in presentations to the SIA Lithography TWG and at Sematech workshops, including organization of and presentations at the Sematech Next Generation Lithography Workshops held in Colorado Springs on November 6-7, 1997 and December 7-10, 1998, and the International Sematech X-Ray Lithography Critical Review held in San Francisco on 6 May, 1998. The preparations for the NGL Workshops also included the writing of a White Paper on X-Ray Lithography.
- Meetings and discussions with Sematech management concerning x-ray lithography and possible Sematech support for x-ray activities, which has led to Sematech funding for certain activities in ALF
- Exploration of possible joint activities in x-ray lithography with other organizations in Japan
- Attendance and presentations at the DARPA Advanced Lithography Review in San Antonio, TX, 26-29 January 1998
- Attendance and participation at the U. of Wisconsin DARPA program review on July 7, 1998
- Attendance at conferences in the U.S. and Japan (including XEL'97 and and XEL'98) to represent our x-ray lithography program
- Participation in a SEMI x-ray mask standard meeting in San Francisco on July 14, 1998