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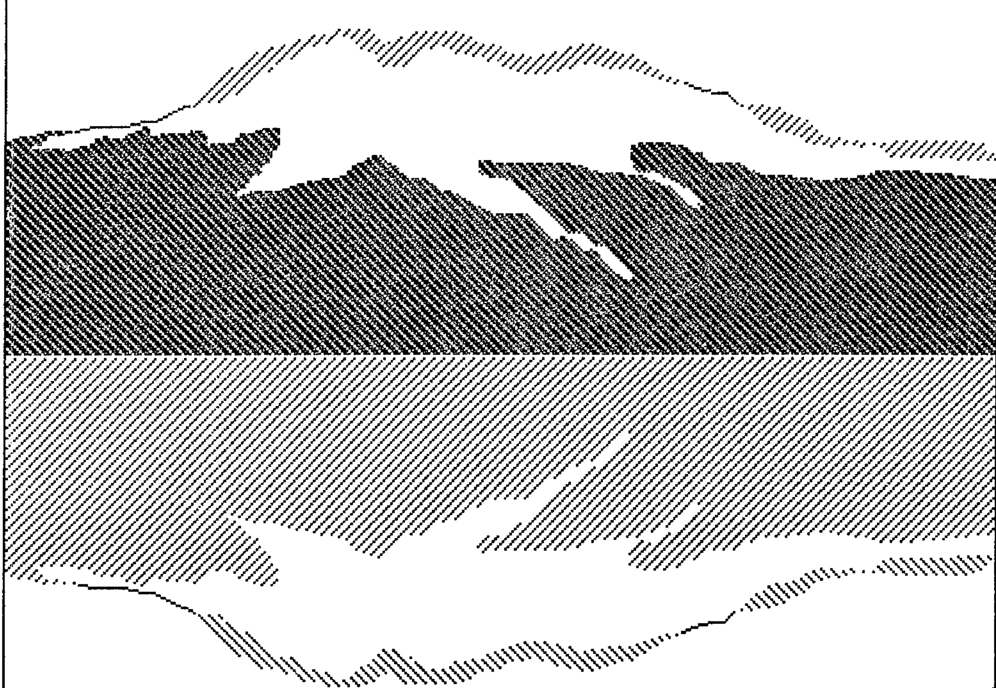

16th NORDIC SEMICONDUCTOR MEETING

LAUGARVATN, ICELAND, JUNE 12-15, 1994

SCIENCE INSTITUTE, UNIVERSITY OF ICELAND

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LAUGARVATN, ICELAND, JUNE 12-15, 1994

ABSTRACTS

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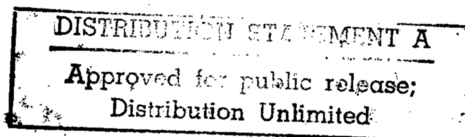

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P R O G R A M

Monday, 13.06.1994				
Time		Speaker		Speaker
8.30 h	Gordon Davies			
9.15 h	Lars Samuelson			
10.00 h	**Coffee**			
10.30 h	proc1	P. Tidemand-Petersson	edev1	C. Fröjdh
10:45 h	proc2	B. Junno	edev2	O. Tornblad
11.00 h	proc3	J. Cardenas	edev3	L. Ramberg
11.15 h	proc4	S. Leppävuori	edev4	M. Rosling
11.30 h			edev5	B. Edholm
11.45 h	proc5	E. Sirén	edev6	O. Engström
12.00 h	**Lunch**			
13.30 h	Markus Büttiker			
14.15 h	meso1	J. Pettersson	edev7	H.H. Radamson
14.30 h			edev8	S. Tiensuu
14.45 h	meso2	A. Brataas	edev9	P. Rangsten
15.00 h	meso3	T. Garm	edev10	T. Clausen
15.15 h	meso4	A.M. Zagoskin	edev11	V. Gruzhinskis
15.30 h	**Coffee**			
16.00 h	meso5	K.-A. Chao	def1	B. Monemar
16.15 h				
16.30 h	meso6	R.I. Shekhter	def2	J. Mäkinen
16.45 h	meso7	M. Gisselfält	def3	E.Ö. Sveinbjörnsson
17.00 h	meso8	M. Jonson	def4	M. Fanciulli
17.15 h	meso9	Y.M. Galperin	def5	I.S. Hauksson
17.30 h			def6	A.N. Larsen
17.45 h	meso10	J.P. Hessling	def7	G.S. Pomrenke
18.00 h	meso11	H. Xu	def8	T. Egilsson
20.00 h	**POSTER SESSION**			

Tuesday, 14.06.1994

Time		Speaker		Speaker
8.30 h	Detlef Heitmann			
9.15 h	low1	H. Sigg	design1	L.M. Molarius
9.30 h	low2	S. Løvold	design2	T.E. Karlin
9.45 h	low3	H. Pettersson	design3	K. Leinonen
10.00 h	**Coffee**			
10.30 h	low4	S. Wang	design4	S. Franssila
10.45 h	low5	S. Løvold		
11.00 h	low6	A. Matulis	design5	M. Bakowski
11.15 h	low7	V. Gudmundsson	design6	G. Schuppener
11.30 h	low8	E.B. Hansen	design7	R. Punkkinen
12.00 h	**Lunch**			
13.30 h	Chris Palmstrøm			
14.15 h	ssm1	H. Stubb	odev1	P. Eriksson
14.30 h	ssm2	J. Gordon	odev2	P. Heimala
14.45 h	ssm3	N. Lundberg	odev3	K. Ljungberg
15.00 h	ssm4	C. Hallin	odev4	C. Fröjdh
15.15 h	ssm5	P. Morgen	odev5	K. Smekalin
15.30 h	**Coffee**			
16.00 h 16.15 h	ssm6	E. Janzén	odev6	O. Inganäs
16.30 h	ssm7	C.-M. Zetterling	odev7	A. Hovinen
16.45 h	ssm8	O. Nur		
17.00 h	ssm9	M. Bergh		
17.30 h	**CONFERENCE EXCURSION AND BANQUET**			

Wednesday, 15.06.1994

Time		Speaker		Speaker
8.30 h	Klaus v. Klitzing			
9.15 h	mdev1	T.A. Fjeldly	proc6	A.N. Larsen
9.30 h	mdev2	L. Lundqvist	proc7	J. Saarilahti
9.45 h	mdev3	P. Kuivalainen	proc8	J. Salmi
10.00 h	**Coffee**			
10.30 h	mdev4	K. Nordgren	proc9	J. Grepstad
10.45 h	mdev5	J. Olsson		
11.00 h	mdev6	T. Ytterdal	proc10	S. Hatzikonstantinidou
11.15 h	mdev7	H.-E. Nilsson	proc11	J. Salonen
11.30 h	mdev8	V. Gruzhinskis	proc12	L.-Å. Ragnarsson
11.45 h			proc13	S.-L. Zhang
12.00 h	**Lunch**			
13.30 h	phot1	J.M. Hvam	proc14	A. Paulsen
13.45 h			proc15	K. Pedersen
14.15 h	phot2	O. Hunderi	theory1	K. Grahn
14.30 h	phot3	B. Ullrich	theory2	U. Sannemo
14.45 h	new1	H.H. Radamson	theory3	T.S. Rantala
15.00 h				
15.15 h	**CLOSING OF THE CONFERENCE COFFEE**			

def Defects
design Design and fabrication
edev Electrical devices
low Low dimensional systems
mdev Modelling of devices
meso Mesoscopic systems
new New experimental techniques
odev Optical devices
phot Photonics
proc Process technology
ssm Solid state materials
theory Recent advances in theory

Monday morning

Configurational instabilities at isoelectronic centres in silicon

Gordon Davies

Physics Department, King's College London,
Strand, London WC2R 2LS, UK

Abstract

When an exciton is bound on an isoelectronic centre, one particle (electron or hole) may be severely localised on the centre. In this paper attention is drawn to the importance of the lattice relaxations stimulated by this localised charge density, both in contributing to the binding energy of the exciton and in determining its properties.

Two examples from crystalline silicon are discussed in detail. The concept of vibronic self-trapping is introduced using an electron-attractive centre. The exciton is shown to be bound to the centre primarily by the electron-phonon interaction of the localised electron. The effects of externally applied perturbations can be understood in detail using the properties of the valence and conduction band of perfect silicon, but paradoxically no symmetry information about the isoelectronic centre may be obtained from the tightly bound particle. The second example is a hole-attractive centre. The hole is trapped in an axial field at the centre, which is shown to derive entirely from the coupling of the hole to phonons. The results of well-established Jahn-Teller theory can therefore be exploited. For example, tunneling is observed between the different Jahn-Teller configurations of the centre, and the properties of the localised exciton can be understood with remarkable accuracy using properties of the perfect crystal modified by the Jahn-Teller effects.

STM-BASED LUMINESCENCE SPECTROSCOPY OF LOW-DIMENSIONAL STRUCTURES

Lars Samuelson

Department of Solid State Physics/"nanometer structure" Consortium

Lund University, Box 118, S-221 00 LUND, Sweden

Abstract

With the strong world-wide efforts to fabricate low-dimensional semiconductor structures for physics and devices it has become urgent that new techniques be developed which are suitable for characterization and investigation of such nano-objects. This talk will concentrate on our recent development of a luminescence probe technique which uses the tip of a scanning tunneling microscope (STM) for local excitation of the luminescence (STL) from quantum-wells, -wires and -dots. In the talk will be described possibilities to perform luminescence excitation spectroscopy where the potential between the tip and the sample defines the excitation energy. I will also give examples of the strongly local character of the excitation that can be obtained and which allows excitation of a single quantum wire with the recording of spectrally resolved emission. The technique and its potential for spectroscopic studies of low-dimensional structures will primarily be compared with conventional cathodoluminescence (CL).

Process Technology 1-5

SELECTIVE-AREA MOVPE FOR InP-BASED OPTOELECTRONIC COMPONENTS

P. Tidemand-Petersson, O. Albrektsen and J. Salzman*

Tele Danmark Research,
Lyngsø Allé 2, DK-2970 Hørsholm, Denmark

Selective-area metalorganic vapour phase epitaxy (SA-MOVPE) is gaining interest as a fabrication tool for optoelectronic components. One way to achieve SA-MOVPE is to deposit a thin dielectric layer on the semiconductor substrate, to pattern the dielectric in order to expose the desired areas for selective growth, and finally to perform the conventional epitaxial growth. For applications of this technique it is important to know the enhancement factor of the growth rate as a function of the relative dimensions of the surrounding dielectric material, and furthermore to adjust the growth parameters, e.g. pressure, temperature and reactant flow, in order to achieve an optimal morphology of the selectively grown epi-layers, e.g. mono-crystallinity, planarity and surface smoothness.

Examples of undesired growth properties in SA-MOVPE will be presented, and the means to circumvent them by proper choice of growth parameters will be addressed. In Fig. 1 is shown an example of nearly optimized growth morphology in the InP/InGaAs material system: planar, flat InGaAs layers embedded in InP, with smooth sidewalls along the <111> termination planes.

After establishing the growth conditions for near-optimal morphology, the growth-rate enhancement due to the partial cover of the substrate with SiO_2 was studied with a specially designed pattern. Having in mind various photonic devices, we opted for a selectively grown 3 μm wide "waveguide" surrounded by a masked region of varying width. A partial view of the calibration mask is shown in Fig. 2. Details of the growth-enhancement dependence on the mask geometry and growth parameters will be discussed, and applications of the technique will be mentioned.

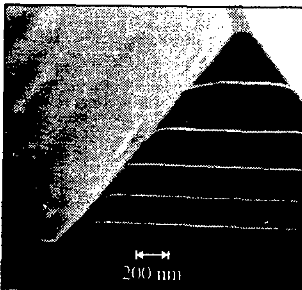

Fig. 1. SEM micrograph showing nearly optimized selectively grown epitaxial layers of InGaAs and InP.

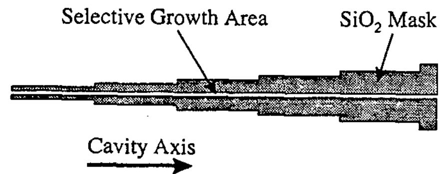

Fig. 2. Partial view of the selective growth calibration mask. The total width of the mask varies from 9 μm to 1000 μm.

* Permanent address: Dept. of Elec. Eng. and Solid State Inst., Technion, Israel Inst. of Technology, Haifa 3200, Israel

RHEED and RD transient studies of surface desorption from InGaAs/GaAs surfaces in chemical beam epitaxy.

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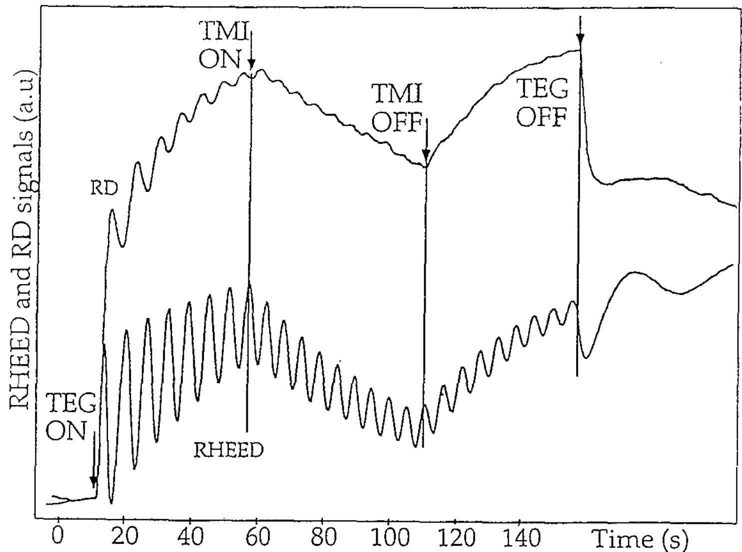
InGaAs quantum wells (QW) were grown in a Chemical Beam Epitaxy (CBE) machine with trimethylindium (TMI), triethylgallium (TEG) and tertiarybutylarsine (TBA) as precursors. Growth was monitored in-situ by Reflectance Difference (RD) and Reflection High Energy Electron Diffraction (RHEED), on both flat and vicinal (001)GaAs substrates. The RD was monitored at 632.8 nm. At this wavelength the RD signal is primarily related to the absorption by Ga-dimers.

In this study we have monitored the growth transients when growing GaAs and InGaAs and measured the time constants of these transients, which exhibited an exponential behaviour: Intensity = $I_0 \exp(-t/t_0)$. The extraced reaction rates were plotted versus temperature in an Ahrrenius plot to extract the reaction energies. The measured energies had a negative value in the growth temperature regime we studied (400-620 °C), and coincided with reaction energies extracted from a growth rate versus temperature plot. Based on this we propose that the measured energies are the energies determining desorption of different group III precursors on the crystal surface.

Fig: RD and RHEED signal transients during the growth of an InGaAs quantum well.



Kinetics and phase formation of Co/Ti bilayer on Si-(100)

Juan Cardenas, Sofia Hatzikonstantinidou, Shili Zhang, Bengt G Svensson and C Sture Petersson

Royal Institute of Technology, Solid State Electronics, P.O. Box E229, S-16440 Kista-Stockholm, Sweden

From Si integrated circuits(IC) technology point of view it has been a growing interest during the last decade to establish reliable and easily implementable processes for metallization when scaling down the linewidth to sub-micrometer range. Solid state reactions in Co/Ti/Si systems offer a way to form low resistive (12 μΩcm) epitaxially grown $CoSi_2$ with excellent thermal stability up to 1100°C. These structures are promising for future devices.

The aim of this study is to learn about the role of Ti in the bilayer diffusion process and to determine the phase formation sequence of the Co-silicides. The epitaxial growth of the cobalt disilicide on the Si substrate is expected to be related to the Co/Ti thickness ratio. This can be so partly due to the dependence on the main moving species (Co or Ti) and the thickness of the gettering Ti-layer forming a diffusion barrier for the Co-atoms.

The epitaxial relation at the interface betweeen the silicide and the Si substrate has been confirmed both by X-Ray Diffraction (XRD) and Rutherford Backscattering spectrometry (RBS) measurements. The distinct layers, before and after annealing, have been verified by Secondary Ion Mass Spectrometry (SIMS) analysis indicating a complete inversion between the Co and Ti layers. The phase formation sequence, nearest to the Si surface, has been studied in detail over a broad temperature range. Data on sheet resistance, RBS, XRD and SIMS will be presented. Moreover, the experimental conditions, such as annealing temperature and time, influencing the growth will be discussed.

LASER ABLATION DEPOSITION AS A PREPARATION METHOD FOR ELECTRONIC MATERIALS

Seppo Leppävuori
Microelectronics and Material Physics Laboratories, University of Oulu, FIN-90570 Oulu, Finland

In the development of new electronic materials and devices, laser ablation deposition (LAD) offers a relatively easy technique to realise complicated material compositions and multilayer structures. In this presentation LAD of different types of thin films, includung High T_C superconductors, for sensor and actuator materials will be presented.

$YBa_2Cu_3O_{7-\delta}$ films and $YBa_2Cu_3O_{7-\delta}/PrBa_2O_{7-\delta}$ superlattices have been deposited on $SrTiO_3$ single crystal substrates using in situ process. Films can also be deposited on silicon by using buffer layers. $CuInSe_2$ (CIS) and $Cu(In,Ga)Se_2$ (CIGS) are well-established as exceptionally efficient semiconductors with potential applications in the fields of solar cells, infrared radiation monitors and fibre optic infrared detectors. CIS and CIGS thin films were deposited by in situ process on fused silica and single crystal silicon substrates. The composition of the target material was largely maintained in the thin films. Lead zirconium titanate (PZT) materials are widely used in sensor and actuator applications. Laser ablation has been used to produce piezoelectric thin films for use in a low voltage cantilever bimorph actuator structure. Nd-doped PZT films were deposited on to Ag-coated oxidised silicon substrates. PZT films were deposited also in situ process on Y-Ba-Cu-O films. Diamond-like carbon thin films also have potential in sensor applications. By varying the peak power density of the laser beam and the deposition temperature, it was found to be possible to tailor the electrical and optical properties of the deposited films between the extremes of diamond-like and graphite-like carbon.

Fabrication of Nanostructures using MBE and MOVPE

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Optoelectronics Laboratory, Faculty of Electrical Engineering, Helsinki University of Technology, Otakaari 1, SF-02150 Espoo, Finland

Nanometer scale semiconductor structures, such as quantum wells, quantum wires and quantum dots are currently being investigated because of their optical and electronic properties, which make new types of semiconductor devices possible. Various fabrication methods include both maskless material deposition and mask-defined material etching. Masking for the nanofabrication based on reactive ion etching is done either by electron beam lithography, aerosol techniques[1] or by formation of etch-resistant islands on the surface. The density of the randomly located columns in the latter masking method can be far more greater than obtained by e-beam lithography. In this paper we present technologies for the fabrication of quantum wire and dot structures using maskless growth and reactive ion etching through masks formed by both e-beam and random nucleation techniques. A different technique to realize small features is to utilize lattice mismatch induced random nucleation in MOVPE. The minimum feature size depends on the process parameters and can be easily made much less than 100 nm.

The fabricated structures are characterized by electron microscopy, atomic force microscopy and photoluminescence.

[1] I. Maximow, A. Gustafsson, H.-C. Hansson, W. Seifert and A. Wiedensohler, J. Vac. Sci. Technol. **A 11 (1993) 748**

Electrical Devices 1-6

Processing and Characterisation of an Etched Groove Permeable Base Transistor on 6H-SiC.

Christer Fröjdh, Göran Thungström, Sofia Hatzikonstantinidou, Hans-Erik Nilsson and C. Sture Petersson

Royal Institute of Technology, Dept of Solid State Electronics, Electrum 229 S-164 40 KISTA, SWEDEN

ABSTRACT

Silicon Carbide is an interesting material for high temperature, high frequency and high power devices. Many devices have been manufactured in SiC during the past years including diodes, MOSFET:s and MESFET:s

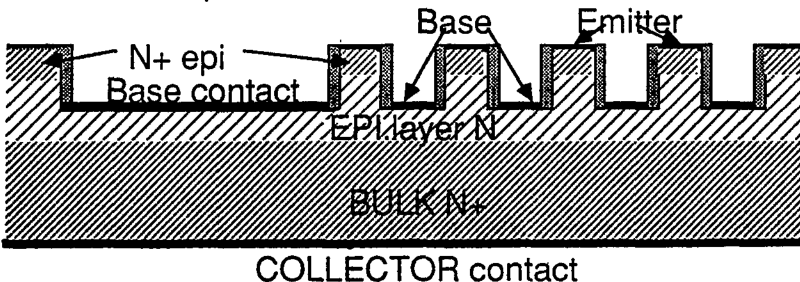
The PBT is well known as a promising device for high frequency applications. Many research groups have been working on PBT:s on silicon or gallium arsenide. So far no work on PBT:s on silicon carbide has been reported

SiC offers a number of advantages for manufacturing of PBT:s compared to silicon. The high saturation velocity for electrons in SiC predicts higher operating frequency than in silicon. Schottky contacts formed on SiC generally have much higher barriers than Schottky contacts to silicon. This will reduce the gate leakage current and in combination with the high breakdown field in SiC allow fabrication of PBT:s with high channel doping. This is important since the maximum operating frequency of a PBT increases with its transconductance and thus the dopant concentration in the channel.

In this paper we report on the fabrication of an etched groove PBT structure on 6H-SiC. The wafer used in our process was a n-type 6H-SiC bulk wafer with two n-type epitaxial layers on top of it. The first layer was used for the channel of the PBT and the second, thin layer formed the emitter contact. By using expitaxial layers doping by ion implantation could be avoided.

Finger shaped grooves were formed by dry etching. The width of the grooves was in the range 1 - 2 μm and transistor areas were in the range 625 - 10000 μm^2. Base and emitter contacts were formed by self aligned metallisation. Ti was evaporated on to the wafer. The sidewalls of the grooves were then cleaned by a short wet etch.

DC characterisation of the devices has been done The characterisation include IV and CV measurements on the Schottky diodes as well as measurement of the IV characteristics of the transistors. IV characteristics for transistors with different areas and different linewidths are compared in order to verify the scaling properties. The results are also compared to results for similar transistors made on silicon.



The influence of emitter properties on the heat generation in SiC and Si PIN diodes under forward conduction

Olof Tornblad[1], Bo Breitholtz[1,2] and Mikael Östling[1,3]

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The PIN diode represents the fundamental structure for several types of power devices under forward conduction, e.g. the thyristor. Recombination at high current densities will predominate in the highly doped n^+ and p^+ emitters and will influence the injection level of the electron-hole plasma in the n-base, which affects the forward voltage drop [1-4]. The heat generation in the diode will thus strongly depend on the properties of the emitters.

In this work both 6H-SiC and Si 5 kV n^+np^+ diodes were simulated under forward conduction for different emitter designs. The distribution of recombination in the n^+ and p^+ emitters and the n-base as a function of injection level was quantified. The influence of the SRH lifetime on the forward voltage drop was also studied. It was found that the forward voltage drop of the 5 kV Si diode depends much stronger on the SRH lifetime than the 5 kV SiC diode. This is due to the larger voltage drops over the emitters and a smaller contribution from the middle region in 5 kV SiC diodes compared to Si.

The emitter doping profiles were Gaussian and abrupt and were varied with respect to doping concentration, depth and surface recombination velocity for minority carriers at the emitter contacts.

The distribution of recombination was investigated with respect to temperature for both Si and SiC. Simulations were carried out for isothermal conditions at 25, 100 and 200 °C. Two-dimensional simulations of a deep emitter design were performed utilizing a simulation code including anisotropic physical models, e.g. mobility and dielectric constant in 6H-SiC [5]. The anisotropy was found to result in a decreased current density around the emitter corner. This result is interesting since it shows the importance of anisotropic effects and may affect future design and modeling of bipolar power devices in SiC.

The physical models for 6H-SiC were based on general considerations [5] and modified Si models with parameters found in the literature [5]. All simulations were based on software developed by Technology Modeling Associates Inc.

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[3] J. Burtscher, F. Dannhäuser and J. Krausse, "Die Rekombination in Thyristoren und Gleichrichtern aus Silizium: Ihr Einfluss auf die Durchlasskennlinie und das Freiwerdezeitverhalten", Solid St. Electron., **18**, No. 1, pp. 35-63 (1975).
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[5] U. Lindefelt, private communication.

High-voltage silicon carbide devices - results of experiments and simulation

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Silicon carbide has been identified as an excellent material for power devices[1], and it is expected to replace silicon in most high-voltage applications. The key useful properties are the extraordinarily high dielectric strength (ten time that of silicon), the high thermal conductivity (similar to copper) and a wide bandgap that permits high-temperature operation.

We have successfully fabricated the fundamental building block of all bipolar devices, the pin diode, and used numerical simulation to further investigate the merits of very high voltage SiC switching devices.

Vertical $p^+n^-n^+$ diodes were fabricated using commercial CVD-grown epitaxial SiC of the 6H polytype. A typical epitaxial structure consists of a n^+ buffer layer grown on the n^+ substrate, followed by 9 μm 9 x 10^{15} cm^{-3} n^- base and a 1 μm 2 x 10^{18} cm^{-3} p^+ emitter and contact layer. Al is used for p-type doping and N for n-type. A reactive ion etching process based on $CH_4/Ar/H_2$ was used to define 1,2 μm tall p^+-emitter mesas with diameters up to 200 μm.

The highest measured reverse breakdown voltage is V_{br}=1100 V, at which point breakdown of the surrounding media occurs in a destructive way. The yield was high, as >60% of the devices sustained >1000 V. The devices show excellent forward I-V-characteristics, with a low series resistance and small excess current at low voltages. The forward voltage drop at a current density J_F=1000 A/cm^2 typically measured a low V_f=3,5 volts, decreasing with increased temperature.

The structure that were realized experimentally have also been simulated numerically using a unique computer program that correctly solves the drift-diffusion equations for anisotropic semiconductors such as 6H SiC. The resulting I-V-characteristics tally well with the experimental observations, while an examination of the carrier and current distribution inside the device reveal that the plasma density and the emitter injection efficiency are realtively low. While sufficient for giving the present 1 kV diodes a low voltage drop, it raises the qustion of what constraints the limited material quality of SiC impose on the performance of future high-voltage devices.

In order to quantify these constraints, numerical simulation was used to investigated what minority carrier lifetimes, diffusion lengths and other material properties high voltage devices such as 10 kV pin-diodes will require. We have also used the program to predict the characteristics of high voltage switching devices.

[1] P A Ivanov and V E Chelnokov, "Recent developments in SiC single-crystal electronics", Semicond. Sci. Technol. 7 (1992) 863-880

Investigations of the Temperature Dependence of the Turn-On Process in Gate Turn-Off Thyristors

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Abstract - In the operation of gate turn-off (GTO) thyristors, a higher gate current is required in order to turn on the device at low temperatures compared to normal working temperatures, *i. e.* elevated temperatures. Hence, the gate-driving circuit has to be over-dimensioned as regards normal conditions in order to be able to turn the GTO on in the starting condition of low temperature. Certainly, this is a problem which costs money for the system designer as well as for the end user: a bulky gate driver is necessary because such rare special conditions are part of the natural operation mode.

The physical explanation of this temperature dependence is yet not well known, and, hence, the temperature dependence of a new design may not be predictable. Thus, it is of major concern for device manufacturers to gain a better knowledge of the behindlying physics of the turn-on process. A phenomenological study of experimental turn-on properties is already performed [1].

In the present paper, the free-carrier absorption (FCA) technique of 2-D space and time resolved measurements of internal carrier distribution is used combined with purely electrical (I-V) measurements and 2-D simulations, in order to investigate the origin of this phenomenon. For instance, it is experimentally verified that the anode-doping level has an impact on the temperature dependence of the turn-on process. Further experimental investigations are going on to establish what models are appropriate to use in computer simulations in order to predict the temperature dependence for an efficient device design. The results of this work will be presented in this paper.

[1] M. Rosling, H. Bleichner, K. Nordgren, F. Vojdani, E. Nordlander; A Study of Anode-Shorted Thin-Cathode GTO Thyristors During the Turn-On and Turn-Off Cycles, submitted to IEEE Trans. Power Electronics, 1993.

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Steady State and Transient Thermal Characterization of Silicon on Diamond Materials

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Abstract: Replacing silicon dioxide as the buried insulator in Silicon On Insulator materials has attracted considerable attention recently. This is because self heating effects in SOI devices are serious performance limitations and possible cause of early failure. One possible replacement has turned out to be diamond, due to its excellent thermal conductivity and high electrical resistivity. However, existing methods for diamond deposition yields a polycrystalline film with properties different from those of bulk diamond. There is also a possible thermal resistance problem in the silicon-diamond interface.
In order to investigate this, we have developed a method for measuring the steady state and transient temperature distribution in real silicon on diamond devices. The measurement results can then be compared with thermal and electrical simulations in order to fit values of thermal capacity and conductivity with measurement data.

Experimental: An array of avalanche diodes where manufactured in a 10 μm silicon film on top of approx. 5 μm diamond membrane. The diodes have a common anode and where distributed over the membrane with a spacing of 61 μm. The avalanche voltage was found to be approx. 40 V. Diodes where also manufactured widthout diamond in a silicon membrane and in regular SOI-material as reference samples.

Measurement setup: One of the diodes was used as a heat source by pulsing the diode in reverse direction with a 100 μs voltage puls. In the meantime the avalanche voltage of the neighboring diodes where monitored with an oscilloscope. Since the avalanche voltage is temperature dependent, the diode temperature can be extracted. By mapping the neighboring diodes, a time dependent temperature distribution can be determined.

Finally a fit of the experimental results with simulated or calculated data will be made in order to extract values of the thermal properties of the silicon on diamond.

Silicon devices based on artificial microcavities

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Three different semiconductor devices based on optical interference in artificial cavities inside silicon crystals are presented. The first case is a fiberoptical sensor for the measurement of pressure at high temperatures. The second is a fiberoptical device for the measurement of voltages on high potentials and the third is a light modulator for the control of light intensity by light.

Silicon related materials with smooth surfaces which are brought into contact with each other and heat treated build up strong bonding forces in the contact areas. The bonding strengths between different combinations of silicon and silicon dioxide surfaces have been measured with values comparable to those of correponding bulk materials. By using this technique, microcavities can be formed inside the volume of two silicon wafers bonded together. One possibility is to bond a silicon wafer with a patterned oxide together with the bare silicon surface of a second wafer. Then, areas where no oxide is present define the cavities with depths which can be accurately predicted by controlling the thickness of the oxide. Light penetrating the cavity will be subject to interference if the cavity depth is comparable to the light wavelength. Due to the possibilities of accurate dimension control and high reproducibility in preparation, structures of this kind can be used in a number of device applications.

One, obvious application of the microcavities is to measure the strength of optical interference when the cavity depth is changed by an external pressure. By combining the device with an optical fiber, a sensor is obtained for the measurement of pressure. Apart from other advantages given by fiberoptical sensors, this particular device utilizes the well controlled mechanical properties of the silicon crystal, which makes it especially suited for use at high temperatures. The sensor has been tested for measuring the pressure inside the cylinders of combustion engines with excellent results.

By etching one of the cavity walls to a thin membrane with a thickness of about 1 µm and furnishing each of the two silicon bodies with electrical contacts, the cavity depth can be changed by applying a voltage between the contacts. In combination with an optical fiber, this device can be used to measure voltages on high electric potentials.

The voltage sensitive device has been developed into a structure with the possibility of modulating the intensity from one light source with the light from a second source. This structure has the potential of becoming a spatial light modulator when cavities are distributed across the area of a silicon wafer. Results from the investigation of discrete modulator elements will be demonstrated.

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Monday afternoon

CAPACITANCE AND ADMITTANCE OF MESOSCOPIC CONDUCTORS

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Abstract

We present a discussion of capacitances and admittances of small phase-coherent conductors. Modern conductors often consist of a number of metallic layers separated by insulators. The metallic layers interact via long range Coulomb forces. The electric fields in such a structure are discussed with the help of characteristic potential functions which determine the variation of the microscopic potential inside the sample in response to an increase of the chemical potential at a contact. We first discuss the capacitance matrix for the case that each metallic portion of the structure is connected to one contact only. Due to the fact that electric potentials can penetrate into the conductor the capacitance matrix of such a structure is of electro-chemical and not electro-static nature. In this case the capacitance matrix is an even function of the magnetic field. If at least one of the conductors has two or more contacts the leading order low-frequency behavior is determined not only by capacitance coefficients but also by emittances which allow for direct transmission from one contact to the other. In this case the capacitance coefficients are not necessarily even functions of magnetic field. We discuss recent related experiments by Wei and Smith which demonstrate capacitances which are completely asymmetric in magnetic field.

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1. M. Büttiker, H. Thomas and A. Prêtre *Phys. Lett.* **A180** 364, (1993).

2. M. Büttiker, J. Phys. Condensed Matter **5**, 9361, (1993).

Mesoscopic Systems

Coulomb Blockade, Aharonov-Bohm Effect, and Landau Quantization in GaAs Quantum Dots

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ABSTRACT

Experiments on GaAs quantum dots at mK temperatures and in high magnetic field are described. The conductance through a quantum dot is measured via two split-gate contacts, and the quantum dot and the leads to the quantum point contact are defined by submicron gate depletion in a high mobility 2-dimensional electron gas. At low magnetic fields, Aharonov-Bohm-like oscillations indicate a non-uniform charge distribution in the dot. Coulomb blockade oscillations occasionally show a periodic envelope. The conductance variation in certain geometries of a quantum dot is suggested to originate from a gathering of states into shells, in analogy to what is found in nuclei. In high magnetic field, where the Landau quantization is assumed to be dominating, the Aharonov-Bohm quantization is found to be related to magnetic edge states. We have in this regime studied the validity of the fluxoid quantization, $Nh = \oint p_F\, dS - \int eB\, dA$, where N is an integer, p_F is the Fermi momentum, B the magnetic field and dS and dA differentials of the perimeter and the area respectively. A model for the variation of p_F, S and A as function of B and a center gate voltage, V_g, allows a separation of the two terms in the fluxoid. Extensive measurements of the Aharonov-Bohm oscillations as function of B and V_g have been performed in order to uncover the fluxoid. At intermediate magnetic fields, where the size quantization and magnetic quantization compete, the variation of conductance with B and V_g is extremely complicated and a matter of continued investigations.

Quantised Raman Spectra in 2D Disk Shaped Quantum Dots

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Abstract

Electronic Raman scattering from doped 2D disk shaped quantum dots is considered with emphasis on the plasmon peak. The Raman cross section is calculated within the random phase approximation (RPA). If the energy of one-electronic states is quantised and a mean distance between levels is not too small, it is expected that the spectrum of electronic excitations, including many-particle ones (plasmon) must consist of single peaks at low temperature. We show that the quantisation in the Raman spectra manifest themselves in oscillations within the one-particle spectrum extending from zero Stokes shifts up to frequencies of the order of v_F/a, where v_F is the Fermi velocity and a is the size of the system. In the depolarized spin-flip spectra the oscillations are given by excitation energies of a noninteracting electron gas. These energies are however shifted by long-range Coulomb electron-electron interactions in the polarized Raman spectra. The quantised electronic motion manifest themselves in a fine structure of the plasmon peak.

Local field calculation for a spherical semiconductor quantum dot with parabolic confinement

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Abstract

A self-consistent calculation of the local electro-magnetic field inside a spherical quantum dot is presented. The confinement potential is taken to be parabolic and isotropic, and the interaction between the field and the quantum dot electrons is described by a nonlocal paramagnetic response function. A particular feature of the treatment is that the calculation is carried out without making use of the electric dipole approximation. As a consequence the magnitude of the electro-magnetic field has a finite value at all positions in space. The direct and self-field parts of the field are discussed separately, as well as the near- and far-field cases. A resonance condition is set up for the local field, and an expression for the resonance frequency is obtained.It is found that the resonance frequency is blue-shifted with respect to the electronic transition frequency by an amount inversely proportional to the extend of the electronic wavefunctions. The theory is applied to a $GaAs$ quantum dot embedded in a $Ga_{1-x}Al_xAs$ medium. For this system the "local field correction" is calculated, and the frequency shift is evaluated.

Indirect Backscattering Statistics in Quantum Point Contacts

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We discuss the breakdown of conductance quantization in a quantum point contact in the presence of random long-range impurity potential. It is shown that in linear response regime the significant role is played by indirect backscattering mechanism via quasilocalized states at the Fermi level, which can provide much higher backscattering rate than any direct backscattering process. The distribution function of conductance fluctuations is evaluated and compared to direct numerical calculations. It is shown to be a generalized Poisson distribution. Estimates are made for QPC performance at different choice of parameters.

RESONANT TUNNELING: FROM MODEL HAMILTONIAN TO MODERN ELECTRONIC DEVICES

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ABSTRACT

Resonant tunneling (RT), especially in double-barrier (DB) structures, has been thoroughly studied within the framework of single-particle model, including the effects of electron-phonon interaction, the uniform external magnetic field, and the ultra-high frequency AC bias. However, almost all well-understood results are measurements on unipolar DBRT samples. Even in unipolar systems, the effect of electron-electron interaction, which is the origin of bistability, is only qulitatively understood. The potential of technological applications of the currently much studied DBRT systems, which are mostly based on III-V compounds, seems in the optoelectronic devices. If so, the many-body effect is of crucial importance, especially for bipolar DBRT structures. This talk will provide a general review on the theory of DBRT, its devices applications, and its possible future development.

Quantum Interference Effects in Inelastic Electron-Photon Scattering in a 2-D Ballistic Microstructure

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We demonstrate a new effect where electron-photon interaction in a ballistic microconstriction plays the same role as impurity scattering does in a "dirty" system. In the presence of an external electromagnetic field all relevant photons are coherent and spatial interference effects in electron-photon scattering become possible in spite of the inelastic nature of the collisions. These interference effects can be controlled by the gate voltage or the frequency of the electromagnetic field. As an illustration we calculate the photoconductance of a double point-contact geometry.

Parity Effects in Josephson Tunneling through a Coulomb Dot

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We study the Josephson current through a superconducting or normal grain coupled by two tunnel junctions to macroscopic superconducting leads and capacitively to a gate. For a superconducting grain the critical Josephson current has a threshold behavior — due to the Coulomb blockade — when the superconducting gap Δ is suppressed below the charging energy E_C by a magnetic field. This effect is a direct consequence of a discrimination by the superconducting ground state between odd and even number of electrons on the grain. The critical current is periodically modulated by the gate voltage; it is 2e-periodic in the gate-induced grain charge if $\Delta > E_C$, but tends to become e-periodic as $\Delta \to 0$. In the intermediate region the gate-modulated critical current develops a double-peak structure; the gap between peaks increases as Δ decreases. If the gap energy on the grain Δ_g is smaller than in the leads, the Josephson current is reduced, but reaches a finite, temperature dependent asymptotic value corresponding to a normal grain if $\Delta_g \to 0$.

Persistent Current of a One-Dimensional Wigner Crystal-Ring

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We calculate the magnetic moment ('persistent current') in a strongly correlated electron system — a Wigner crystal — in a one-dimensional ballistic ring. The flux- and temperature dependence of the persistent current is shown to be essentially the same as for a system of non-interacting electrons. In contrast, by incorporating into the ring geometry a tunnel barrier, that pins the Wigner crystal, the current is suppressed and its temperature dependence is drastically changed. The competition between two temperature effects — a reduced barrier height for macroscopic tunneling and a loss of quantum coherence — results in a sharp peak in the temperature dependence, which for a rigid Wigner crystal appears at $T \sim 0.5\ \hbar s/L$, (s is the sound velocity of the Wigner crystal, L is the length of the ring).

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Noise in Correlated Tunneling Current

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The aim of the talk is to discuss physics of electrical noise in nanoscale structures with correlated tunneling, namely in quantum dots coupled to two junctions and in double-barrier resonant tunneling structures (DBRTS).

At very low voltages only equilibrium Nyquist-Johnson noise is present which is due to electron interaction with a thermal bath. At higher voltages two non-equilibrium contributions to noise spectra become important.

1. The first one – so-called shot noise – is due to discrete electronic charge and to stochastic character of electronic transport through the device. If transport events are uncorrelated the low-frequency correlation function $S(\omega) = \langle(\delta J(t)\,\delta J(0))^2\rangle_\omega$ is determined by universal relation $S(\omega) = 2e\langle J\rangle$.

Any kind of correlation in transport events effects upon the shot noise. In real nanoscale structures two kinds of correlation are important

- Statistical correlation due to Pauli principle,
- Coulomb correlation due to dependence of escape probability on the number of electron inside the structure.

The first mechanism has been extensively discussed. We work out a theory of the Coulomb correlation influence on the shot noise. Calculations are based on the solution of Master equation for relevant stochastic process in a system exhibiting Coulomb blockade. We present results for Coulomb-blockade diode and transistor devices. It is shown that both intensity and shape of shot noise spectra are strongly voltage and temperature dependent. Investigation of these dependencies allows one to determine important characteristics of the device and of the electromagnetic environment.

2. The second contribution – so-called flicker noise – is important at very low frequencies. This mechanism is due to low-frequency fluctuations in the surrounding of a nanostructure, the electronic system being a sort of 'detector' of such fluctuations. At very low voltages and temperatures only few defects with internal degree of freedom are important, and the current exhibits 'random telegraph noise', the intensity being proportional to J^2. At higher voltages and temperatures number of effective dynamical modes increases and the spectrum becomes close to $1/\omega$.

A model of 'noisy environment' will be presented which allows one to estimate both the intensity and statistical properties of flicker noise.

Consequently, we demonstrate that *noise spectroscopy* is a powerful method to investigate dynamical properties of nanoscale electronic devices and to determine important parameters.

Noise in a Quantum Point Contact due to Impurity Rearrangement

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Low-frequency noise in a quantum point contact (QPC), electrostatically defined in a 2D electron gas on a GaAs-AlGaAs interface is considered. In such contacts electron scattering by soft impurity or boundary potentials leads to a coherent wave function splitting between different transverse modes. The phase differences between the modes are sensitive to the gate and source-drain voltages, external magnetic field, etc. As a result, an oscillating contribution to the QPC $I-V$ curve must appear. Such a mechanism has been recently proposed to explain conductivity nonlinearities observed in QPC. In the present study we employ this mechanism to analyze a low-frequency (telegraph-like) noise which has also been observed along with the conductivity nonlinearities. For a simplified case of a channel with two extended (current carrying) modes, a simple analytical formula for noise intensity is derived. This expressions allows one to relate the noise to the measurable oscillatory part of the current-voltage characteristics. We believe that noise measurements can provide an additional piece of information of dynamical properties of QPC in comparison with the more traditional ones based upon d.c. transport.

Theory of Conductance Fluctuations in Finite Antidot Lattices

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We present an exact quantum-mechanical calculation of the conductance for large but finite antidot lattices based on a scattering-matrix formalism. Rich structure is predicted for the mesoscopic systems and can be charaterized by two kinds of conductance fluctuations: slow fluctuations as shown by the presence of many broad dips in the thermally averaged conductance and rapid fluctuations which appear at low temperature on the top of the slow ones. The slow fluctuations, which are insensitive to temperature up to a few Kelvin, are due to wave interferences in a form of Bragg reflections by the periodic potential of the systems. The rapid fluctuations, which may only be observed at very low temperature and in the condition that electrons remain phase coherent over the entire lattices, can be attributed to resonant tunneling through rather randomly distributed localized electron states in the systems. We predict that, instead of the "conventional" miniband structure as observed in one-dimensional quantum-dot lattices, rapid fluctuations should be seen at low temperature in the measured conductance of a finite antidot lattice.

Electrical Devices 7-11

Enhancement of Si electron mobility using delta-doped structure

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Abstract

A large enhancement in the electron mobility for a pair of closely spaced Sb δ-doped layers are placed in Si. The room temperature mobility is enhanced by a factor of two compared to corresponding uniformly doped layers or singly δ-doped structures (see Fig.1). Even higher mobilities were obtained by using a Schottky gate on top and applying a voltage to adjust the potential well. With an effective gate voltage of ~ -0.3 V the mobility was 1200 $cm^2 V^{-1} s^{-1}$ at room temperature, which is an enhancement by a factor of ten relative to the layer with equivalent bulk doping concentration (see Fig.2). The high mobility is attributed to wave-functions with nodes at the δ-doped layers.

Fig.1

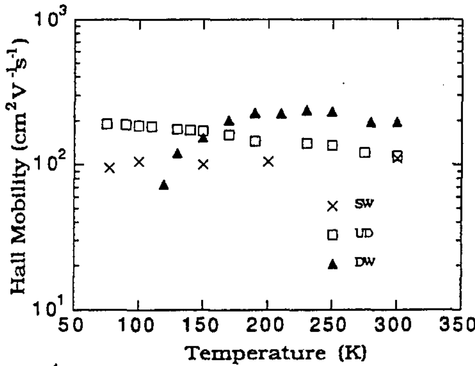
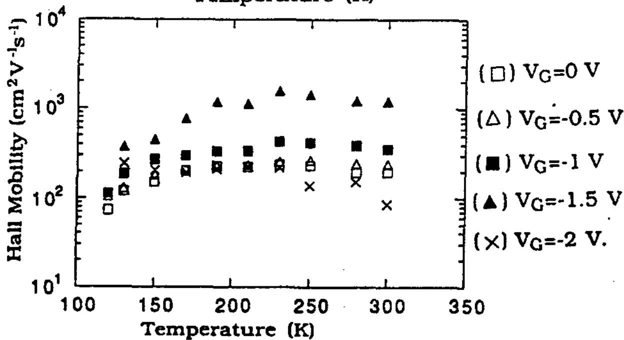


Fig.2



MUCH Transistor – A Novel MOS-Switch Structure for Smart Power Applications

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A novel concept using a sandwiched MOS structure for high voltage switching is presented. A p-channel device is put directly on an n-channel device so that the channel of each device act as the gate electrode of the other. Compared to lateral DMOS, the mutual channel structure (MUCH) has a lower on resistance, shorter switching time and higher breakdown voltage in the off condition for a given chip area.

The concept description is as followed: Two enhancement type complementary field effect devices are sandwiched on each other, separated only by a thin gate oxide, as shown in figure 1a and 1b. Mutual crosstalk between the channels is used to control the current through both devices. In the on state, shown in figure 1a, the p-channel is positively biased compared to the n-channel. In this condition, the high voltage side of the p-channel can be open, thus current through the n-channel is controlled only from the low voltage side. In off-state, shown in figure 1b, both the low and the high voltage side should be shorted or reverse biased. The field is then distributed uniformly over the two channels. Failure due to gate oxide breakdown is eliminated and the voltage breakdown is only limited by the channel length and rigorous designed field plates.

The MUCH has been realised using wafer bonding between an n-type SIMOX wafer and an oxidised p-type bulk silicon wafer. The SIMOX wafer was then thinned by grinding and wet etching using the implanted oxide as etch stop. The MUCH device was then manufactured using standard IC process technology.

Both simulation and experimental results show the advantages of the MUCH concept. Figure 2 shows the IV-characteristic when the p-channel high voltage side is open. In table I, measured and simulated data are summarised.

Fig 1a: MUCH in on state

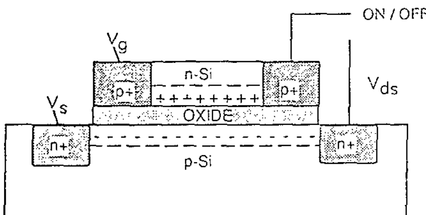

Fig 1b: MUCH in off state

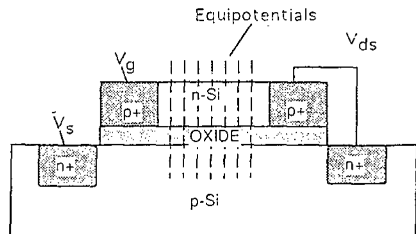

Fig 2: IV-char whith the high voltage side of the p-channel open

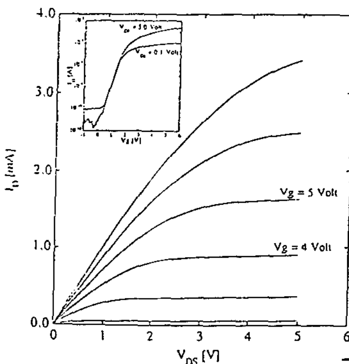

Table I

Quantity	Data
d_{ox}	600 Å
r_{on} (V_g=7 V)	2 kΩ/□
g_m (V_d=5 V)	1 mS 50mS/mm
V_{br} (L_{pch}=20µm)	> 100 V
S (V_d=0.1V)	250 mV/dec.
t_r (simulated)	4ns
t_f (simulated)	4ns

Electroplated Copper Coils for Wireless Monitoring of Sensors

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Abstract

The background to this work is our interest in performing wireless sensor measurements in situations where electrical or optical connections are impractical. A major application area is sensors for medical care, others are monitoring in transportation and process industry. We have in this work focused on wireless measurement of a passive pressure sensor , i.e. an electrical resonant circuit consisting of a capacitor and inductor whose resonant frequency is pressure dependent. The fabrication of the sensor element, a micromachined silicon capacitor, has been presented earlier [1] and we're now focusing on the integration of the inductor on the silicon capacitor chip.

Electroplated copper coils have been manufactured on silicon wafers with a maximum height of 36.5 µm. These were made using an electroplating mould of thick resist (Shipley's STR 1075) deposited in four layers. In order to electrically isolate the coils from the substrate, a thermal oxide layer of 1.12 µm was grown on the silicon wafers. A thin chromium/gold layer was sputtered onto the oxide to serve as a seed layer, i.e. a thin metal layer for the plated copper to grow on. Copper was chosen as the plating metal for its low resistivity and it's ease to use. The resulting copper coils had remarkable differences in height, from 17.5 µm to 36.5 µm on the same wafer, depending on their position on the wafer (compared to the position of the electrode). Nevertheless, the measured resistance and inductance values were essentially in accordance with the theoretical values. The coils where characterized remotely using a grid-dip meter, inductively coupled to our electroplated coils.

Reference

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Transition metal-based metallizations to InP

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abstract. Ni and Cr metallizations to low doped n- and p-type InP have been investigated in order to clarify how they affect the electrical performance of advanced multilayer metallization schemes for ohmic contact and Schottky diode applications. It was found that the Ni and Cr contacts to n-type InP exhibit unstable ohmic behaviour at all annealing temperatures (300-500°C), and that Ni and Cr metallizations to p-type InP exhibit diode behaviour. The behaviour of the contacts were compared to phase formation paths of the Ni-In-P and Cr-In-P ternary systems. From this it was found that amorphous ternary phases are forming first by interdiffusion of Cr and Ni into the InP crystal. Subsequently, crystallization and eventually phase seperation into a Cr-P binary phase and pure In for the Cr-In-P system and Ni-In and Ni-P binary phases for the Ni-In-P system are formed. These phases the determine the contact behaviour. At 500°C annealing the Cr diodes to p-type InP were almost ideal, as deduced from barrier height measurements using a combination of J-V and C-V methods. This indicates that the metallization forms a two-layer structure with Cr-P phases lying above pure In. The Ni diodes to p-type InP annealed at 500°C, on the other hand, were not ideal, indicating that Ni-In and Ni-(In)-P phases in parallel are determining the electrical properties of the diode.

Based on these results and previosly obtained results on Au-Cr and Au-Ni ohmic contacts to highly doped n-type InP it is concluded that Ni and Cr are active in determining the electrical properties of any multilayer metallization scheme to InP containing Ni or Cr. In particular for ohmic contacts to n-type InP it is of great importance to incorporate a Ni or Cr layer close to the metal-semiconductor interface for Schottky barrier lowering purposes. But also for ohmic contacts to p-type InP it is of importance to physically separate the Ni- or Cr-containing layers from the MS interface in order to reduce the specific contact resistance.

IMPEDANCE FIELD AND MICROWAVE POWER GENERATION IN InP DIODES

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The near-micron n^+nn^+ InP diodes are widely used in modern semiconductor generators of short millimeter waves. To improve the high-frequency performance of these generators various doping profiles and a reduction of the n-region length are suggested. For a proper choice of the diode design it is firstly necessary to investigate how a variation of these parameters influences on the device operation. For such a consideration the diode characteristics which allow for the spatial analysis of various physical quantities are most preferable. The main aim of this work is to demonstrate that the impedance field can be successfully used for this sake. By definition, the impedance field $\nabla Z(f,x)$ is given by the ratio of the Fourier components of the local electric field E and the total current j at the frequency f in the point x. Since the total current is constant throughout the diode the impedance field reflects spatial behavior of possible perturbations of the local electric field caused by a harmonic perturbation of j. Thus, the impedance field describes the additive contributions which every point of the diode gives to the small-signal impedance. Therefore $\nabla Z(f,x)$ can be used for a detailed analysis of the physical processes responsible for the diode performance and can help in a proper choice of the doping profile and the diode geometry. To simulate the carrier transport in n^+nn^+-InP diodes the closed hydrodynamic approach based on the carrier number, drift velocity and mean energy conservation equations coupled with the Poisson equation for the self-consistent electric field has been used. Results of calculations can be summarized as follows.

The generation spectrum in short n^+nn^+ diodes is formed mainly by the near-anode area of the n-region where the transit-time dynamics of accumulation layers takes place. Under the constant current operation a reduction of the n-region length leads to no variation of the dead zone and results primarily in a reduction of the active area only. The diode can be considered as a sequence of series connected areas which give separate contributions into the net spectrum of the microwave power generation. These contributions can be described by a spatial profiles of the impedance field calculated at various frequencies. Such a map clearly individuates the diode regions which are responsible for the generation at low, intermediate and high frequencies and, hence, can be used for a proper choice of the doping profile and the diode length.

Defects

DIRECT DETERMINATION OF THE EEH AUGER THRESHOLD ENERGY IN SILICON

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The Auger mechanism has recently been recognised to be an important electron-hole recombination process in silicon, both for the intrinsic case at high carrier densities [1] and in the extrinsic case where the recombination is governed by deep levels [2]. Also, the Auger recombination process has been shown to be an important part in the mechanism of transformation of a defect from a stable to a metastable configuration [3]. At low temperatures the excitonic Auger process has been argued to be dominant [2,3].

The probability of various possible Auger processes is determined by the band structure, and it has been shown that the electron-electron-hole (eeh) process, where the excess energy in the recombination process is given away to an electron which is excited high up in the conduction band, is dominant [4]. A threshold energy $E_g + E_{th}$ for the Auger process, exceeding the bandgap E_g, is in general expected from the requirement of energy and momentum conservation in the eeh process. However, E_{th} could not be predicted with a better accuracy than $0<E_{th}< 50$ meV from the knowledge of the band structure [4]. Later theoretical calculations claim that experimental Auger data can be well understood if E_{th} is zero [1]. No direct experimental determination of this Auger threshold has appeared up to now, to the best of our knowledge.

We have examined possible ways of observing this Auger threshold. It appears that an excitation spectrum for the Auger induced transfer from a stable to a metastable configuration of a complex Cu-S related defect in silicon provides the spectroscopic tool for such a study. Two independent measurements using different equipment in two different laboratories confirm a blueshift by (5±1) meV at 2 K of the excitonic Auger response function for the transformation to the metastable configuration, compared with the fundamental silicon excitonic absorption spectrum. Thus the value of E_{th} is (5±1) meV at 2 K, i e a quite small quantity. This observation also serves as a further confirmation of the excitonic Auger effect as the mechanism responsible for the configurational change of the defect, in addition to the arguments presented in Ref. 3. This determination of E_{th} also allows a more accurate evaluation of the band structure parameters in silicon.

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POSITRON ANNIHILATION AND MICROSCOPIC STRUCTURE OF THE DX CENTER IN AlGaAs

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In GaAs substitutional group-IV impurities (Si, Ge, Sn) at the Ga-site site and group-VI impurities (S, Se, Te) at the As-site are shallow donors. However, irrespective of the nature of the donor species they also give rise to deep electron levels known as *DX*. In GaAs the DX level is not localized in the energy gap, but in $Al_xGa_{1-x}As$ it becomes the lowest-energy state of the donor when the AlAs mole fraction is $x > 0.22$. At this range of alloy compositions it controls the conductivity of n-type material. At low temperatures the DX center also gives rise to persistent photoconductivity. Because of these two circumstances - defect metastability associated to an isolated substitutional impurity atom and the difficulty in n-type doping - a lot of effort has been taken to understand the fundamental properties of donors in III-V semiconductor alloys.

A strong boost to understanding the metastability of donor impurities comes from theoretical studies. They have given an indication that an isolated donor impurity may undergo a shallow to deep transition. From total-energy calculations, a metastable state is found for the negatively charged donor. The formation of the DX center involves a large bond-breaking displacement of the group-IV atom along its bond axis into an interstitial site. The calculations predict that the nature of sp-hybridization in covalent crystals is responsible for the metastability of the donor impurities.

Apparently, there is no direct information on the atomic structure of the DX center, or the interpretation of the experiments is ambiguous. We address the microscopic structure of the DX center in $Al_xGa_{1-x}As$ using *positron annihilation spectroscopy*. The discovery that a positron can become localized at vacancies has led to a highly versatile method for the study of atomic-scale defects in solid. The potential benefit of this technique is that it differentiates vacancies from other types of defects such as interstitials or antisites.

In this work we report the observation of *a vacancy* as a part of the structure of the DX center in Si- and Sn-doped $Al_xGa_{1-x}As$. It indicates a large lattice relaxation associated with the transitions between the stable and metastable states. We also present evidence of the *negative* charge of the DX ground state. The positron results are in a good agreement with the vacancy-interstitial model predicting the displacement of the donor atom from the substitutional lattice site to the interstitial position. Finally, we point out the close similarity between the present findings and those made earlier on the EL2 center in GaAs.

Lithium Passivation of Gold in N-type Crystalline Silicon

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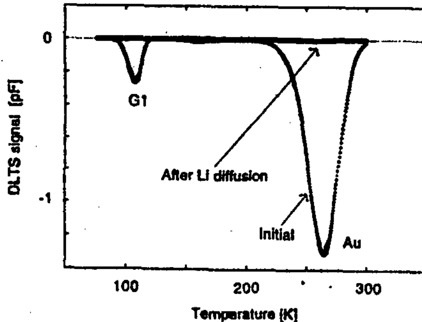
We demonstrate that lithium in-diffusion into gold doped n-type silicon at temperatures between 200 and 300°C results in strong passivation of gold acceptors. This was investigated using deep level transient spectroscopy (DLTS) combined with secondary ion mass spectroscopy (SIMS) and capacitance voltage (CV) profiling. Li doping of ≈ $1{\cdot}10^{17}$ cm^{-3} results in a decrease of the active gold acceptor concentration by about three orders of magnitude (10^{14} cm^{-3} => 10^{11} cm^{-3}) and less than 10% of the gold is electrically active in a crystal containing comparable concentrations of gold and lithium (10^{14} cm^{-3} range).

The thermal stability of the passivation appears to be similar to that observed for gold passivation by hydrogen. About one third of the Li passivated gold acceptors are reactivated after 15 minutes annealing at 400°C. Furthermore, we find that the passivation process is reversible as long as free lithium is available in the crystal. This is in contrast to hydrogen passivation where the atomic hydrogen released during dissociation of Au-H complexes is rapidly lost as molecular hydrogen (H_2).

The starting material, n-type floating zone silicon, was first doped with gold at 900°C resulting in gold acceptor concentration of ≈ $2{\cdot}10^{14}$ cm^{-3} in the middle region. After etching and cleaning the specimens were covered with Li (99.9%) imbedded in mineral oil. Lithium was then pre-deposited at 300-350°C for 10-30 minutes in a diffusion furnace. Excess Li was removed off the surfaces of the samples and the Li was driven in at temperatures between 250 and 350°C followed by rapid quenching in liquid nitrogen. Two types of reference samples received the same heat treatments as the Au-Li co-doped specimens: 1) samples doped with gold but no Li and 2) samples only doped with lithium. The gold acceptor concentration in the gold doped reference samples did not change during the processing. No deep levels were found in the lithium doped reference specimens.

CV profiling was used to estimate the shallow lithium donor concentration in the samples. It turned out that the concentration of electrically active lithium was comparable to the total Li content estimated with SIMS. The samples used in this study had Li densities ranging between $5{\cdot}10^{13}$ cm^{-3} and $1{\cdot}10^{17}$ cm^{-3} and the Li concentration did not change appreciably during storage at room temperature.

In addition to gold acceptor passivation we observed a new-lithium-gold-related DLTS peak (labeled L1), with an activation energy of 0.40 eV, after lithium diffusion at 200-300°C. This trap was maximized after heat treatments between 250 and 300°C but anneals out reversibly within few minutes at 100°C. Finally, using DLTS depth profiling we observed that injection of hydrogen into the sample surface region by wet chemical etching resulted in dissociation or passivation of the L1 trap.



The figure shows DLTS spectra before and after lithium diffusion at 300°C resulting in lithium concentration of ≈ $4{\cdot}10^{16}$ cm^{-3}. The electrically active gold acceptor concentration decreases from $2{\cdot}10^{14}$ cm^{-3} to $2{\cdot}10^{12}$ cm^{-3}. The G1 peak is not observed after Li diffusion. The signal is hydrogen-gold-related and is introduced by the etching treatment.

CONVERSION ELECTRON MOSSBAUER SPECTROSCOPY STUDY OF IRON SILICIDE FILMS GROWN BY MBE

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The growth and the structural and electronic characterization of epitaxial iron-silicide phases on Si has attracted increasing interest during the last years from both the fundamental and technological points of view. In particular the semiconducting β-$FeSi_2$ phase, with a direct gap of 0.85 eV due to a Jahn-Teller-like instability, has potential optoelectronic applications, when integrated with the well developed Si technology. Moreover, the great versatility of Fe to form a number of epitaxial silicides offers a wide spectrum of potential applications.

Iron silicide films have been grown on Si(111) at room temperature by molecular beam epitaxy (MBE). Structural and electronic properties were investigated by RHEED, XPS, STM, TEM, RBS and XRD. Bulk stable (ϵ-FeSi, β-$FeSi_2$ and Fe_3Si) and epitaxially stabilized (γ-$FeSi_2$, FeSi which has the CsCl structure and exists also in a $Fe_{1-x}v_x$ Si defective phase containing Fe vacancies v) phases have been grown allowing the unambiguous identification of the Mossbauer spectra of the different metallic, semimetallic, semiconducting and magnetic silicides. The Mossbauer parameters (isomer shift, quadrupole and magnetic splitting) for the different phases are discussed with respect to the local surrounding of the Fe atoms. The proposed kinetic phase diagram of the Fe-Si system has been explored by annealing at different temperatures films with various thickness and the structural phase transformations have been monitored through the Mossbauer spectrum. For example the FeSi (CsCl) structure with a lattice constant $a_0 = 2.77 Å$ shows a single line spectrum and transforms upon annealing at a thickness dependent temperature into the ϵ-FeSi phase which, due to the lower point symmetry, shows a quadrupole doublet. At higher temperatures the metallic ϵ-FeSi phase transforms into the semiconducting β-$FeSi_2$ phase which shows two doublets due to two different Fe sites. The direct study of interface phases of MBE deposited Fe on Si, allowed by the high sensitivity of Mossbauer spectroscopy, will be also presented.

Problems of p-type doping of zinc selenide

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Abstract

There has been a long history of attempts to dope ZnSe p-type. Park et al. [1] and Ohkawa et al. [2] were the first to successfully dope ZnSe grown by molecular beam epitaxy (MBE) using nitrogen as a dopant. Doping levels up to 10^{18} cm^{-3} have been reported but doping levels higher than that are difficult to achieve since additional nitrogen is not active. Nitrogen creates an acceptor with a binding energy of 110 meV and by examining the photoluminescence spectra from ZnSe:N we have observed different donor acceptor pairs (DAP) for different nitrogen concentrations (N_D-N_A). In this paper, we will report on optical studies of ZnSe:N epilayers grown by MBE. Photoluminescence spectra of the donor-acceptor pair region at different temperatures and different carrier concentration shows that two donors are present in the samples, residual shallow donors with activation energy 26 meV and deep donors with activation energy of 46 meV previously reported as a V_{Se}-Zn-N_{Se} complex [3]. In the exciton region we observe new emission at 2.7653 eV and the intensity increases when the epilayer is compensated by the deep donor. We therefore propose that this transition is related to a deep donor bound exciton. A selective excitation photoluminescence measurements shows a creation of a impurity band in highly doped ZnSe:N.

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Electron-irradiation induced defects in $Si_{1-x}Ge_x$

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Electron-irradiation induced defects in silicon have been studied intensively for many years, and many defects have been identified. Much less attention has been devoted to such defects in germanium, and the identification of the observed defects is controversial. Silicon and germanium are completely miscible over the entire composition range, thus any composition of $Si_{1-x}Ge_x$ can be grown offering the possibility of studying the development of irradiation induced defects as the composition changes gradually from pure Si to pure Ge.

We have initiated such an investigation based on molecular beam epitaxially (MBE) grown, relaxed $Si_{1-x}Ge_x$, grown by the compositional grading technique on Si-wafers using deep level transient spectroscopy (DLTS) to trace the defects. The present paper reports the first results of this investigation comprising results on n-type $Si_{.75}Ge_{.25}$.

Low dislocation density ($\sim 5x10^5$ dislocations/cm^2), p^+n-layers of relaxed $Si_{.75}Ge_{.25}$ were grown by MBE on o.o1 ohm-cm, n-type, <100>-oriented Si-substrates. The thickness of the n-type epi-layer was 2 μm, doped with Sb to $1.5x10^{16}$ cm^{-3}; the p^+-layer was 0.2 μm thick doped with B to $\sim 1x10^{20}$ cm^{-3}. Mesa-diodes of different areas (0.002 - 0.01 cm^2) were made by photolitography and etching. Diodes with low leakage currents ($\sim 1x10^{-6}$ Amp/cm^2) and ideal capacitance-voltage characteristics were made. DLTS on these diodes revealed a broad distribution corresponding to a maximum defect concentration of about $5x10^{12}$ cm^{-3}, probably originating from dislocations.

The electron irradiations were done with 2-MeV electrons to different doses between $1x10^{16}$ and $6x10^{16}$ cm^{-2}; during irradiation the diode-temperature changed from 50 K to 110 K. After irradiation the diodes were allowed to warm up to room temperature before the DLTS-analysis. Three well-defined lines are found in the DLTS-spectra, two of them showing Poole-Frenkel effect corresponding to a single donor state and one shows no Poole-Frenkel effect demonstrating that it is an acceptor state. The acceptor level is tentatively assigned to the Sb-vacancy pair defect, whereas the two donor defects resemble defects observed in pure Ge. Detailed annealing experiments are presently being undertaken and will be included in the discussion of the assignments of the lines presented in the paper.

RARE EARTH INTEGRATION WITH SEMICONDUCTORS AND RELATED MATERIALS.

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Future potentials for rare earths (RE) in electronic and optoelectronic materials include RE doped semiconductors, RE mono-pnictides, and RE silicides. The last decade saw the investigation of such dopants as Er, Yb, Tm, Nd, Pr, Ho, and Sm in the III-V semiconductors GaAs, InP, AlGaAs, and GaP. The interest was spurred on by the possibilities of fabricating pn junction diodes and diode lasers with frequency stable emissions. Novel applications may also include photoconductive switches, MIS structures, metallization, radiation hardening, quantum dot structures, and magnetoresistors using narrow bandgap III-Vs. Due to an increased possibility of Group IV optoelectronics, erbium has been explored in Si and SiGe with emphasis on the 1.54 μm emission important for silicon based fiber optics. Room-temperature electroluminescence from Er-doped silicon has been demonstrated and exciting new results point toward potentials for Er doped porous silicon. Research interest in Group II-VI:RE has had a resurgence due to electroluminescence devices for flat panel displays. A new material system has emerged which combines semi-metallic RE mono-arsenides with compound semiconductors like GaAs and AlAs. These RE mono-pnictides enable buried structures for resonant tunneling and hot electron transistors. Other RE mono-pnictides include LaN with possible infrared detector applications. A competing system is the erbium silicide ($ErSi_2$)/silicon system also with infrared operation. Research is being pursued for establishing fundamental understanding of these RE-based systems: structure, optical and electrical properties, excitation dynamics, and source materials.

Passivation of shallow and deep levels by lithium in GaAs

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Similar to hydrogen the group-I element lithium passivates various shallow and deep levels in GaAs. In p-type GaAs lithium passivates the shallow acceptors Zn_{Ga} and Cd_{Ga} [1] and the deep acceptor Cu_{Ga} [2]. In n-type GaAs it passivates native deep donors such as EL2 and EL6 [3]. However, in contrast to hydrogen there is no evidence of the passivation of shallow donors by lithium in GaAs.

The passivation of Zn_{Ga} and Cd_{Ga} acceptors in p-type GaAs is inferred from a simultaneous increase of the Hall hole mobility and decrease in free carrier concentration throughout the bulk of Li-diffused samples. The acceptors can be reactivated by thermal annealing. We attribute the passivation to the formation of neutral Li-Zn and Li-Cd complexes. The passivation of Cu_{Ga} is concluded from the disappearance and reappearance of deep level transient spectroscopy (DLTS) and photoluminescence (PL) signals. DLTS signals due to acceptor levels at E_v+0.15 and E_v+0.40 eV which are commonly attributed to the two ionization levels of Cu_{Ga} disappear when the material is diffused with Li. A similar disappearance is observed for the well known PL band at 1.36 eV also attributed to the Cu_{Ga} defect. The DLTS and PL signals can be reactivated by thermal annealing. Passivation of native deep donors in n-type GaAs is concluded from the reduction of the relevant peak heights in DLTS spectra after Li-diffusion. The defects can be reactivated by thermal annealing.

In n-type GaAs the electron mobiltity decreases as the carrier concentration is reduced by Li-diffusion. We believe that this is a manifestation of increased impurity scattering in the material. From this it is evident that the dominant mechanism responsible for the decrease in carrier concentration is compensation as opposed to passivation in p-type GaAs. We therefore conclude that Li does not passivate shallow donors in GaAs, but rather compensates the material by forming acceptors.

We compare our results for Li-diffused GaAs to those for hydrogenated GaAs which has attracted much attention in recent years. We explain qualitatively the main similarities and differences with simple arguments based on the different atomic structure of Li and H.

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Poster Session

Design Optimization of Negative Charge Pumps for IGBT driver ICs

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Abstract

Negative gate biases are used in driving IGBTs for improving the noise margin and preventing dv/dt induced turn-on, and for speeding up the switch-off. The negative gate bias can be supplied from the power supply. However, in many cases it is more economically to generate the negative bias on the driver chip by using a circuit called charge pump.

Charge pumps can also be used for generating voltages over the supply voltage (positive charge pump) [1] [2]. Very few papers have been published of the optimized design of negative charge pumps. Basically a negative charge pump consists of two capacitors, pump capacitor C_p and hold capacitor C_h, and four switches for transferring the charge from the power supply via the pump and hold capacitors to the load. The steady state voltage upper limit with resistive load is

$$V_{out}(\infty) = \left(-V_{DD}C_P e^{\frac{-t_1(C_P+C_H)+t_2C_P}{R_L C_H (C_P+C_H)}}\right) \Big/ \left(C_P + C_H\left(1 - e^{\frac{-t_1(C_P+C_H)+t_2C_P}{R_L C_H (C_P+C_H)}}\right)\right) \tag{1}$$

where V_{DD} is supply voltage, R_L load resistance, t_1, t_2 hold and pump capacitor discharge time. Equations for the voltage ripple and average output current can also be derived. Equation (1) shows that the output voltage has a steady state level between the negative of the supply voltage and ground. From the desired output current and the minimum allowable bias level one can calculate the requirements for the parameters, e.g. pumping frequency and capacitance values.

The practical realization of the charge pump can be done with CMOS transistors. It requires either a n-substrate process or the possibility of floating NMOS transistors. The on-resistance of the real switches sets another limit for the design, to the pump frequency. If the pump charging time approaches the time constant $\tau_p = C_P R_{on}$, V_{DD} in Eq. (1) will be under the actual supply voltage. The substrates of the switching CMOS transistors must always be in the most negative potential to prevent latch-up. This determines the timing of t_1 and t_2 within a cycle.

The application of the negative charge pump described is limited to processes with n-substrate or suitable floating NMOS transistors. The design limitations come from the large area needed. For example a -5V 10mA source with 4.9V upper limit with 50nF/10nF capacitors needs min. 3.3 MHz pumping frequency. This set the maximum resistance of the main switches to 1.3 Ω. Typical gate width would then be 15 - 40 mm and area 0.6 - 1.4 mm^2. The fact that the outputs to the external capacitors cannot have protection components may cause reliability problems.

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Maskless Selective Growth of Wire Structures on Planar Substrates

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The fabrication of nanoscale semiconductor structures, quantum dots and quantum wires, has attracted attention due to the predicted improvement in device performance. The fabrication of these structures typically consists of complicated lithographical, etching and regrowth steps. Here we report a novel simple method for fabrication well-defined structures on planar surface in one growth step.

The fabrication process is schematically shown in Fig. 1. GaAs(100) 2°-off wafers were bombarded by focused ion beam (FIB), Fig. 1(a). InP was then deposited on patterned substrates by hydride vapor phase epitaxy (VPE), Fig. 1(b).

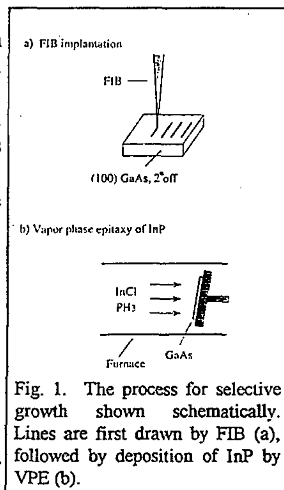

Fig. 1. The process for selective growth shown schematically. Lines are first drawn by FIB (a), followed by deposition of InP by VPE (b).

Continuous wires were obtained on lines implanted in [011] direction. In [01$\bar{1}$] direction, rows of detached islands on the implanted lines were formed. At the optimum dose, 3×10^{10} cm^{-1} for 260 keV Si^{++}-ions, complete selectivity in the growth was achieved and 1000 μm long continuous wires with a submicron cross-section were obtained. In Fig. 2 is shown a topview SEM micrograph of InP wires formed on lines implanted along the [011] direction with a 1 μm pitch. The smallest wires obtained were 220 nm wide and 160 nm high.

A cross-sectional TEM micrograph of a wire is shown in Fig.3. The cross-section is a triangle formed by (100) plane of the substrate and (111)B side planes. The defect density in the wire is relatively low despite of the lattice mismatch of 3.9 %.

This work is part of Quantum Wave Project of ERATO Program of Research Development Corporation of Japan (JRDC).

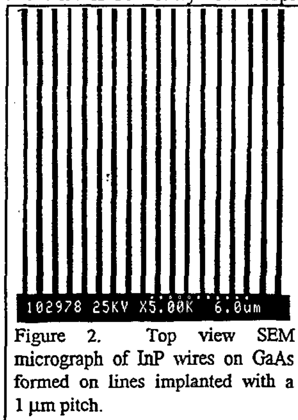

Figure 2. Top view SEM micrograph of InP wires on GaAs formed on lines implanted with a 1 μm pitch.

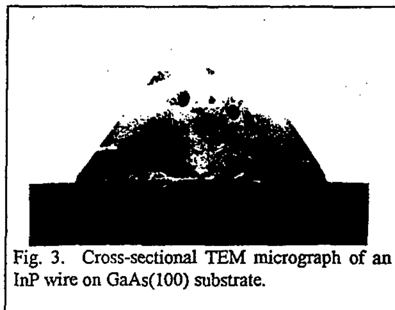

Fig. 3. Cross-sectional TEM micrograph of an InP wire on GaAs(100) substrate.

MOLECULAR BEAM EPITAXY OF SILICON CARBIDE ON (100) SILICON SUBSTRATES USING A PLASMA SOURCE

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Cubic silicon carbide (SiC) is a wide band gap semiconductor with potential applications for high frequency, high power and high temperature devices. Moreover, SiC could provide a suitable substrate for the growth of epitaxial diamond on silicon. Molecular beam epitaxy (MBE) has been used for the growth of epitaxial SiC on silicon [1] and has considerable promise for the successful growth of epitaxial diamond. For this purpose we have developed a plasma activated gas source MBE process in which the molecular beam is formed by activating a methane-hydrogen mixture in a plasma source.

The background pressure in the MBE chamber is about 10^{-11} mbar when the system is idling. During the growth the pressure rises to 10^{-4} mbar due to the hydrogen background. Methane gas is mixed with hydrogen in a gas manifold. Typical flow rates are 3.5 sccm for H_2 and 0.35 sccm for CH_4. Clean 75 mm diameter (100)-oriented silicon wafers are used as substrates. The native oxide is removed in situ by heating the substrate above 1000°C. The growth of epitaxial SiC occurs when the substrate temperature exceeds 900°C. The size of the SiC crystallites ranges between 100-200 nm and they are oriented along the <110> directions of the Si substrate. The layers are characterized by reflection high energy electron diffraction, Rutherford backscattering, X-ray photoelectron spectroscopy and atomic force microscopy.

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AN EMPIRICAL RULE FOR THE ENERGY LEVELS OF T^{2+} IONS OF TRANSITION METALS IN COMPOUNDS A_3B_5 AND A_2B_6

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When the counting off level of the ionization energy of transition metal impurities is changed, we observe a certain tendency in their ground states. This tendency shows that the energy position of impurity levels caused by T^{2+} ions of transition metals practically does not change in compounds of the same semiconductor group, if measured with respect to the vacuum. Using the relation between the gap energy and the electronegativities of the compound atoms, we can demonstrate this rule more precisely and extend it to uninvestigated impurities and semiconductor compounds.

THE SCANNING KELVIN MICROSCOPE FOR CONTACT'S INVESTIGATIONS

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We have constructed the equipment for the investigation of surface potential. Its characteristics are as follows: spatial resolution is 20 lines per mm, sensitivity is 5mV, rage of voltage is -+ 100V. We used this equipment to investigate the thermal dependence of the work function of pure Cu, Au, Pt, Al, dynamics of the surface charge in semiconductor materials, the effect of ionic implantation on the surface potential, of metal-semiconductor electrical contacts, menylayers compounds, etc.

The physical investigations are carried out within the temperature interval from -150 to 100°C at the 10^{-3} Pa vacuum or at room temperature, using the light of various wavelengths.

An Investigation of the Stability of Copper Germanide Thin Films in the Presence of Si and SiO2

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Copper germanide (Cu_3Ge) has received interest in recent years as a potential metallization for VLSI applications due to its exceptionally low room temperature resistivity (~6 μΩ-cm).

We have investigated the thermal stability of Cu_3Ge thin films on both silicon and thermally oxidized silicon wafers. Films were deposited by electron beam evaporation of sequential layers of Ge and Cu and exposed to an annealing schedule ranging from 100 to 450 °C. Secondary ion mass spectrometry (SIMS) analysis has revealed an interaction of the film with both substrate types. At temperatures as low as 200 °C, diffusion of silicon into the copper germanide film was observed with the concentration and depth of penetration scaling with increased annealing temperature. Results on controlling this interaction will also be presented and correlation made with resistivity measurements.

Iron silicide contact properties to n- and p-type silicon

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The semiconducting phase of the iron disilicides, β-$FeSi_2$, with a band structure indicating a direct transition of about 0.87-0.89 eV, is considered to be a suitable material for a future light emitting silicon device [1-2]. However, to date only a few publications [3-5] have been reported on the electrical transport properties across iron silicide-silicon junctions. These investigations all show the presence of non-ideal currents across the silicide-silicon junction and the question to ask is whether the presence of iron at elevated temperature induces these defects or if they may be related to the fabrication method used. Recent studies [6] however, have shown nearly ideal current voltage characteristics which will be further presented in this paper.

Iron is reported to act as a deep level impurity in silicon and also has a high diffusivity which makes it necessary to further investigate the possible occurrence of iron defects and iron silicide formation induced defects in silicon. Early investigations of iron deposited on clean vacuum cleaved silicon showed ideality factors of 1.2-1.7 and barrier heights to n-Si in the range of 0.63-0.7 eV [7-8]. In this presentation thin polycrystalline films of the metal like phase FeSi and the semiconducting β-$FeSi_2$ phase were formed via solid state reaction with either boron or phosphorus doped silicon. The electrical junction properties were studied by current-voltage and capacitance-voltage temperature activated analysis.

The Schottky barrier heights of FeSi were estimated by current-voltage to 0.66±0.03 eV and 0.41±0.03 eV at 295 K for n- and p-type silicon respectively. The corresponding current transport mechanism ,with ideality factors of about 1.03-1.06, was dominated by thermionic emission across the interfaces and indications of a recombination mechanism through deep defect levels were only seen at temperatures below 175 K on n-type samples.

The current transport mechanisms across the β-$FeSi_2$/n-Si and β-$FeSi_2$/p-Si junction interfaces displayed ideality factors with values of about 1.02-1.04 and 1.03-1.05 on n- and p-type silicon respectively . Temperature activated current voltage analysis yielded an activation energy of about 0.65±0.03 eV on n-Si and 0.42±0.03 eV on p-Si. Indications of a recombination current mechanism through deep levels inside the silicon depletion layer were only seen on n-Si samples annealed at 800°C and measured below 225 K.

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Effect of Partial Ionization on the Characteristics of Lateral Diamond MESFET's

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ABSTRACT

Experimental results [1] for diamond thin films indicate, that only a very small fraction (~1/1000) of impurities is ionized. It is not certain that this drawback can be eliminated in the future as the diamond technology develops. We have performed two-dimensional simulations on lateral diamond p-MESFET structures by taking this effect into account.

In the case of power transistors the partial ionization means that in order to get a low on-state resistance with a carrier concentration of 10^{16} cm $^{-3}$, the doping concentration should be as high as 10^{19} cm^{-3}. On the other hand, the heavy doping decreases the breakdown voltage and results in a very low mobility, which in turn increases the on-state resistance. Therefore it is not obvious in advance, that diamond would remain a superior material for power transistors, when the partial ionization is taken into account.

The MESFET structure was chosen since a Schottky junction is a more realistic gate structure in diamond than a pn-junction in a JFET. A p-type device was chosen due to difficulties in growing doped n-type diamond epitaxial layers. The minimum value for the drain to gate distance L_{dg} (equal to the source to gate distance L_{sg}) is determined by a chosen breakdown voltage V_{br}. On the other hand, large values of L_{dg} increase the on-state resistance R_{on}, and therefore an optimized value for L_{dg} must be found. When the simulated V_{br} is just above 1000 V, the minimum value for L_{dg} is 3 µm for a doping density of $N_A = 1.0 \cdot 10^{16}$ cm^{-3} of the active layer. In this case R_{on} is as small as 7 mΩcm^2. This value is almost two orders of magnitude smaller than the theoretical minimum value 266 mΩcm^2 for vertical 1000 V silicon power MOSFET's. The transconductance value in this p-type diamond MESFET is 8.6 mS/mm at V_{DS} = -10 V and V_{GS} = 1 V. If we assume that only 1/1000 of the acceptors in the active layer is ionized, the calculated R_{on} is 24 mΩcm^2 and the calculated V_{br} is 110 V for a doping density of $N_A = 10^{19}$ cm^{-3}. For a corresponding power Si MOSFET (100V) with a gate length of L_g = 0.3 µm the on-resistance is 4 mΩcm^2.

The partial ionization problem must be solved before a general breakthrough of diamond semiconductor technology can be seen.

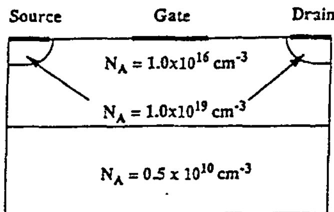

Fig.1. Cross-section of a lateral diamond MESFET used in the simulations. The gate length is 2µm and both the drain-gate and source-gate distances are 3 µm. The thickness of the active diamond layer having the doping density $N_A = 10^{16}$ cm^{-3}, is 1.5 µm.

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Epitaxial Growth of Silicon Carbide by Chemical Vapour Deposition

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Silicon Carbide (SiC) is a very suitable material for high power devices, however, there still exists some problems that need to be solved before successful device manufacturing in SiC can be started. One of these problems is to produce thick, low-doped material with long lifetimes, in order to make devices capable of blocking high voltages.

We report on the successful growth of SiC by Chemical Vapour Deposition (CVD). The system is a commercial, GaAs MOCVD reactor suitably converted into a hot-wall CVD reactor for SiC epitaxy previously reported by O.Kordina et al (International Conference on Silicon Carbide and Related Materials, Washington DC, November 1-3, 1993 (to be published)). The precursors used for growth of SiC are silane as Si source and propane or methane as C source. P-type doping is accomplished by trimethylaluminium (TMA). The growth systems we have studied are:

1) 6H SiC on off-axis cut 6H SiC substrates
2) 3C and 6H SiC on on-axis cut 6H SiC substrates
3) 3C SiC on (100) Si substrates and
4) 3C SiC regrown on 3C SiC layers with the initial Si substrate etched off.

The regrown samples were made on 3C layers approximately 15 μm thick where the Si substrate had been etched off using a solution of HF and HNO_3. Using this method some high quality 3C layers could be obtained. Photoluminescence (PL) of these samples compare well with the best 3C layers produced on on-axis 6H substrates. Growth of 6H on off-axis substrates gives impurity concentrations in the low 10^{14} cm^{-3}. PL measurements show strong free exciton (FE) related lines indicating material of supreme quality. The ratio between the 77 meV phonon replica of the FE and the nitrogen bound exciton s-line is as high as 8.7 which is the highest reported value.

Thermal conduction in thin films of CVD-diamond and silicon dioxide on silicon

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Diamond has the unique property of being an electric isolator and a good thermal conductor. This makes diamond the ideal isolator in a SOI-material. To be able to compare different methods for producing these types of silicon on diamond materials (SOD) it is necessary to have a simple method for measuring the thermal conductance.

We have measured the thermal conduction in thin CVD diamond layers grown on silicon wafers and compared with simulations. A measurement method originally used for thin silicon dioxide layers was chosen. Test devices were fabricated on silicon wafers with CVD-diamond films and as comparison silicon dioxide films. The test structures consist of a long and narrow metal wire with four terminals. Two terminals are used to drive a current through the wire and the other two terminals are used to measure the voltage over the central part of the wire (Kelvin bridge). The measurement procedure is as follows:

- Measure the resistance of the wire using a relatively small current (10mA). This should be done at different temperatures to determine the temperature coefficient of the metal resistivity.
- Use a larger current (50mA-500mA) and measure the resistance and the dissipated power.
- Calculate the mean temperature of the wire from the measured increase in resistance and the temperature coefficient. The thermal resistance is calculated from the temperature difference between the wire and chuck divided by the dissipated power.

The wires are 2mm long and the width varies from 5µm to 20µm. The voltage tap lines measure over 1mm in the middle of the wires. These test structures can with good accuracy be compared to 2D-simulations. Note that heat is generated along the 2mm long wire but the mean temperature is only measured in the central part of the wire. Possible error sources are heat conduction through the metal wires especially the voltage tap lines. The metallization (Al) is placed either directly on the silicon, on a 1-3µm thick diamond film grown on silicon, or on 0.5-1.0µm thick wet oxide on silicon.

The following observations can be made from a comparison between simulations and measurements on silicon dioxide.

- For silicon without oxide(d_{OX}=0) the measured thermal resistance was higher than the simulated.
- For silicon with oxide, the measured thermal resistance was lower than the simulated.
- For different widths of the wires, the measured thermal resistance did not vary as much as the simulated.

The first observation is probably explained by the thermal resistance between the wafer and the chuck. The simplest explanation of the other two are that silicon dioxide have a higher heat conduction than expected. However, this is completely different from measurements published in recent papers. Test structures with different types of oxide (dry, wet, CVD) are under fabrication.

Measurements show that the CVD-diamond materials have higher thermal resistances than silicon without oxide, especially the thinnest diamond material. Published measurements on CVD-diamond films indicates that the thermal conductivity in the films are in the range 1000-2000 W/Km. To explain our measurements, the thermal resistances in the interfaces between silicon-diamond or diamond-metal must be rather high. The explanation to this is probably the difficulty to get a high density of nucleation points on the silicon surface. Thus, the diamond is in contact with the silicon at very small and relatively few points which reduces the thermal conductance through the interface.

To be able to determine the thermal resistance through the two interfaces it is necessary to measure the temperature at several places on the surface of the chip and compare with simulations. Measurements of this type gives very small temperature differences and it is impossible to get a reasonable agreement with simulations. Larger test structures are under fabrication which should give more accurate measurements.

Physical Models and Parameters Describing the Behaviour of Power Devices Operating under Real Conditions

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Abstract – At Scanner Lab, optical methods are used for the characterization of semiconductors. Our equipment makes it possible to look inside a component during its transient cycle and trace the inner carrier distributions. Since the method used is best suited for low-doped silicon devices of larger dimensions, *i. e.* power devices, the research is closely cooperated with ABB.

This paper states the methodology of finding a reliable set of physical models/parameters for computer simulations of power semiconductor devices. Since such devices are supposed to work under high injection level at elevated temperatures, models and parameters have to be adjusted for these requirements. Measured data serve as the necessary feedback to the simulations.

The free-carrier absorption (FCA) technique is used in different modes to support the feedback data. In this technique absorption data is converted to calibrated carrier-density data.

Simulated carrier distributions in P-I-N diodes, at different current levels, are compared to FCA-measured for different temperatures. The simulation is made using the program MEDICI with improved physical models/parameters.

An example of our parameter fitting is the ambipolar Auger coefficient. If this is changed from the default value to the value we propose, the data fit is good at all current levels covering a broad temperature range.

Other transport parameters which are highly dependent of injection level and temperature are the ambipolar diffusion coefficient and the effective ambipolar lifetime. The validity of these parameters modelling to *e. g.* high carrier-density effects is also visualized.

In addition, dynamic measurements and simulations on gate turn-off thyristors (GTO) are performed. The GTO, being a more complicated device, gives good possibilities for the validity of the modelling work under real conditions. A typical sequential measurement of a GTO transient turn-off cycle is compared to the corresponding 2-D simulation result. However, for the sake of clearness in the modelling work, 1-D presentations taken from the 2-D simulations are better suited to be compared with measurements. The turn-off cycle is produced in different ways, and in this paper stress is put on Q-circuit turn-off.

In GTO modelling, it is shown that there are much more research to come before a complete set of reliable, carrier and temperature dependent models/parameters will be available. On the other hand, this paper shows that experimentally verified physical models and parameters are needed for reliable computer simulations. This goal can only be achieved by coupling measurements to simulations.

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FABRICATION OF NARROW ALUMINIUM PATTERNS BY I-LINE OPTICAL LITHOGRAPHY

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ABSTRACT

In summer 1993 VTT/Semiconductor laboratory bought a Canon 2000i1 i-line stepper with high NA (0.52). It has a resolution limit of about half microns. With a new i-line stepper VTT Semiconductor laboratory is developing submicron process technology for telecommunication electronics. One possible application is surface acoustic wave devices.

Before buying the i-line stepper we used ASM 2000 h-line stepper (NA = 0.30). Usually we used image reversal lithography and dark field masks for patterning of metal layers. Because there is no image reversal photoresists or negative photoresists suitable for i-line submicron lithography available we moved to positive photoresist.

Since then we have tried several photoresists from different manufacturers. We have come to conclusion that it is advantageous in this application to use dyed and relatively thin photoresist layer. The resist must also have excellent dry etch resistance. The resist thickness is limited by the plasma etch resistance and the linewidth requirements. In this case, because these test are made with flat aluminium surface, the limited depth-of-focus is not a restriction.

For these tests the aluminium sputtering process is specially modified for deposition of thin layers. We have used electrical measurements and surface inspection system to locate the best wafer positions inside the process chamber. Currently, we can deposit very low resistivity aluminium films with ±2% uniformity of sheet resistance on wafer.

For resist development we have used both immersion development and single phase spray/puddle development on resist track. The achieved minimum line-width of photoresist pattern is about 0.4 µm on highly reflective aluminium surface and 0.3 µm on bare silicon surface.

The aluminium is etched by reactive ion etching (RIE) using standard chlorine based chemistry. The developed etching process yields very uniform line widths. The aluminium etching process is anisotropic. Only slight lateral etching of aluminium occurs and the aluminium line-width is linear down to about 0.5 µm. The measured line-widths on a wafers are well within a 100 nm wide range. For line-width measurements we have used both electrical measurements and SEM.

The narrowest achieved aluminium line and space patterns have 1.0 µm pitch.

SPIN RESONANCE DETERMINATION OF THE EFFECTIVE ELECTRON G-FACTOR IN LOW DIMENSIONAL (GaIn)As/InP STRUCTURES

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The effective spin-splitting factor of electrons in the conduction band, g*, is a fundamental property directly related to the electronic state of a semiconductor. In direct band-gap type-I quantum well (QW) systems, the most powerful and precise technique for measuring the g*-values, the technique of spin resonance in combination with optical polarization spectroscopy, is prevented by the unfavorable relation between the time constants for optical recombination and spin relaxation. This is the reason that, so far, the g*-values in low dimensional systems have been determined only in (a few) type-II QW systems, and only for holes.

In order to perform spin resonance measurements of g* of the electrons in type-I (InGa)As/InP QW's, we have designed several series of samples with different composition and well width. The key feature was an one-side, p-type modulation doping of the QW. This modulation doping induces an electric field which separates the holes from the optically induced electrons, thus reducing the recombination rates substantially. This allows optically detected spin resonance measurements in polarization mode to be performed. The experimental results were, first, that clear g* resonances from electrons in the QW can be obtained for active layer thicknesses between 6 nm and 100 nm, and for composition $0.4<x_{Ga}<0.6$. The related g*-values showed a clear dependence on QW composition and well width. Second, the observed g* values were very anisotropic when changing the angle between magnetic field and QW axis, giving a g-tensor with two components $g^*_{\parallel}$ and $g^*_{\perp}$. This anisotropy depends significantly on the confinement potential, but the ratio $g^*_{\parallel} / g^*_{\perp}$ remained constant for varying composition. The $g^*_{\parallel}$-values were modeled by a **kp**-calculation, where a self consistent potential was considered. However, no quantitative theory on which to base the calculation of the anisotropy is available. The strong dependence of the g*-values ($g^*_{\parallel}$, as well as anisotropy) on the confining potential is very encouraging for the characterization of structures with further reduced dimensionality. Investigation on quantum well wires are currently under way.

Quantum Corrections to the Threshold Voltage of Short Channel MOSFETs

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Abstract

The modelling of the semiconductor devices, both for 2 D-numerical simulations and at circuit simulation level, is based on classical current continuity and Poisson equations. However, in a MOSFET at the onset of strong inversion electron motion is quantized in the direction perpendicular to the Si-SiO_2 interface. This quantization can usually be neglected at room temperature, but in modern MOSFETs having their channel lengths in the deep submicron region, channel doping must be increased to suppress punch-through phenomena. The high doping, in turn, results in a more prominent quantum effect. We have developed an analytical model to account the quantum effects on the threshold voltage V_T in the deep submicron n-channel MOSFETs. The model is based on a variational solution of the Schrödinger equation for electrons in an inversion layer of a MOSFET [1], and it takes into account the effects of the quantized electron energies, the electron charge distribution, and bandgap shrinkage due to high doping on V_T. The present model can be applied both in 2D-numerical simulations and in accurate circuit simulation level modelling. The model explains well the measured shift of V_T, as shown in Fig.1. The experimental data has been taken from ref. [2], where the measured V_T was compared to the results from a classical device simulator, resulting in the quantum corrections shown in Fig.1. The shift of V_T is large in deep submicron devices and it cannot be neglected in the accurate device modelling.

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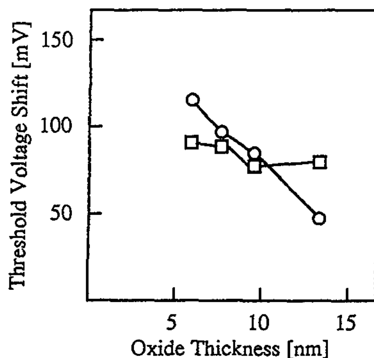

Fig.1. Shift of the threshold voltage due to quantum corrections. The experimental data (o o o) has been taken from Ref. [2]. The squares (□ □ □) have been calculated by using the present model.

Physical Modelling of Vertical DMOS Power Transistors for Circuit Simulation

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Abstract

The use of power DMOS transistors, both as discrete components and as output stages of power integrated circuits (PICs) is growing rapidly today. This growth is based on the steady increase in the power ratings of DMOSTs. Modern MOS devices cover drain voltages from 50 V to 1000 V. Therefore PIC and power electronics designers require power transistor models for circuit simulations in this voltage range. Computer-aided design of analog circuits including DMOSTs is critically dependent on reliable device models implemented in circuit simulators, e.g. SPICE. However, SPICE was developed at a time when all MOS transistors were lateral, low power devices. Therefore, SPICE MOSFET models as such are not able to simulate the unique features of new power DMOST devices such as quasisaturation, space charge limited current, channel doping-density gradient, and changes of internal capacitances with changing bias conditions. We have developed an analytical model for vertical power DMOSTs based strictly on device physics. A common feature in all MOS-gated power devices is a short MOS channel region. Therefore we have especially concentrated on the modelling of this region by taking into account various short channel effects such as mobility degradation and velocity saturation due to high electric field in the DMOS channel, and a decrease in the threshold voltage. Also the effect of channel doping density gradient on the threshold voltage is modelled. The space charge limited current due to excess electrons in the accumulation region close to silicon surface is treated by deriving iterative numerical solutions to the coupled Poisson's and current equations. In the modelling of the drift region the velocity saturation and the device geometry are taken into account. The model has been implemented in the APLAC circuit simulator. Fig.1 shows the good agreement between the results from the simulations and the measurements [1] of the dc electrical characteristics of a vertical power DMOST.

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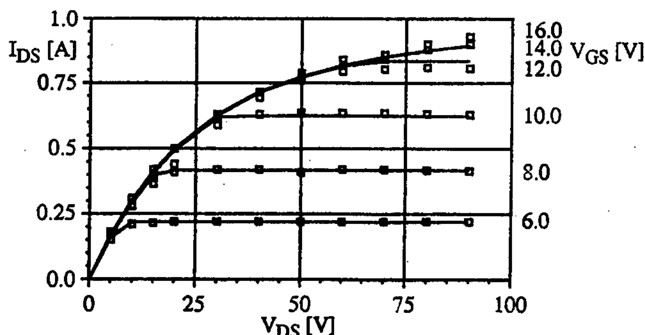

Fig. 1. Measured [1] (□ □ □) and simulated (——) I-V characteristics of a vertical power DMOST.

Special case of exciton binding: a satellite problem

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We study a bound two-particle system, consisting of a negative and a positive charge, in which merely one of the particles is attracted by a local potential $V(\vec{r})$. An exciton, in the effective-mass description depicted as a bound hole-electron system, in which the electron, say, is attracted by the local potential, is such a system. The question we investigate is the following: Under the assumption that the potential $V(\vec{r})$ is unable to trap a single electron, can it nevertheless bind the electron plus its satellite, the hole? One might wonder whether the answer is trivally affirmative, by simply replacing the electron mass by the exciton mass. However, the problem is more subtle.

One physical motivation for studying this question comes from trapping of excitons by isoelectronic impurities, an impurity with the same valence electron configuration as that of the host atom it replaces. The mechanism for binding has been described as follows: A primary particle (electron or hole) is trapped in the short-range potential of the isoelectronic impurity, and then the secondary particle (hole or electron) is bound by the Coulomb attraction from the primary particle. However there have been suggestions that this picture is too simple, and that systems may occur which display bound exciton even if the primary particle does not bind by itself. We study a simple and transparent model based on the Hamiltonian

$$H = -\frac{\hbar^2}{2m_e}\nabla_e^2 - \frac{\hbar^2}{2m_h}\nabla_h^2 + V(\vec{r_e}) - \frac{e^2}{4\pi\epsilon|\vec{r}_e - \vec{r}_h|}$$

which demonstrates precisely this effect. Here $V(\vec{r})$ is a square-well potential.

LASER ABLATION DEPOSITION OF $CuInSe_2$ AND $CuIn_{1-x}Ga_xSe_2$ THIN FILMS

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$CuInSe_2$ (CIS) and $CuIn_{1-x}Ga_xSe_2$ (CIGS) are well established as exceptionally efficient semiconductors with potential applications in the fields of solar cells, infa-red radiation monitors and fibre optic infra-red detectors. They have a large absorption coefficient and superior radiation resistance. With the usual deposition processes, such as sputtering, coevaporation and selenisation, there have been problems in the control of homogeneity, composition and carrier concentration in the films. In this study, CIS and CIGS films were prepared by laser ablation deposition, which has proved to be a suitable method for the deposition of multicomponent films, especially in the reproduction of the target composition.

CIS and CIGS thin films were deposited by an *in situ* process on different insulating, semiconducting and metallic substrates by pulsed laser ablation using an XeCl excimer laser and polycrystalline and single crystal targets. The effect of deposition temperature and substrate material on the structure and orientation of the films was investigated. The structure and properties of the films were studied by X-ray diffraction, micro-Raman spectroscopy, scanning electron microscopy, scanning tunneling microscopy, electrical and electro-optical measurements. The composition of the target material was largely maintained in the films deposited below 450 °C. On most of the substrate materials, the films were highly oriented with the (112) planes of the chalcopyrite structure along the substrate surface. The films deposited on to Si (100) developed, under some conditions, {100} orientation and epitaxy.

A SEMI-ANALYTIC I-V MODEL OF THE PERMEABLE BASE TRANSISTOR

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ABSTRACT

A semi-analytic model of the Permeable Base Transistor (PBT) extracted from two-dimensional simulations is presented. The PBT is a unipolar device that can work in two different modes of operation, in barrier limited mode or as a short channel MESFET. In the barrier limited mode the current is controlled by a potential barrier formed in the depleted channel. An analytical solution of Poisson's equation in two dimensions demand knowledge about the form of the depletion boundary. The depletion boundary is also a key parameter for the drain to source current. From this point of view the only solution available seems to be semi-analytical. Our approach is built on two major empirical approximations: the maximum depletion into the channel is the most important parameter for the current and transition between the linear region and the saturation region is mainly controlled by the field dependent mobility. Using this approximation the current can be expressed as a product of a mobility dependent modulation factor and a saturation current controlled by the maximum depletion width towards the channel. Thus it is not needed to know the exact form of the depletion region. Two dimensional simulation reveals that the maximum depletion can be modelled using the depletion region expression for a conducting cylinder multiplied by a weight factor. This weight factor is only dependent on the grid thickness and can be computed numerically. The mobility dependent factor extracted from a reference transistor contains all the information needed to evaluate the current in an arbitrary PBT as long as it has the same grid thickness. In the saturation region the demand for current continuity will increase the carrier concentration in the channel as the drain to source voltage increases. This effect is similar to the channel length modulation in a MOSFET and can be modelled in a similar way.
In the sub threshold region the PBT is working in a barrier limited mode. Conformal mapping of a charged metal strip to find a solution of Poisson's equation for a one dimensional approximation of the depletion region has been reported in the literature. This solution is valid only deep down in the barrier limited mode and can not be used when V_{gs} is near the threshold voltage. We have based our sub threshold model on two empirical approximations: the potential barrier should be a second order function of drain to source voltage, the form of this second order function is completely described by the V_{ds} value at which the barrier vanishes and the potential barrier at $V_{ds}=0$. All empirical approximations has been checked carefully with two dimensional simulations. The final model consists of a set of equations and a set of parameters that can be extracted from two reference transistors.

EFFECT OF THE INTERATOMIC SI-SI POTENTIAL ON DEFECT PRODUCTION DURING ION IMPLANTATION OF SI

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Processes that produce damage in crystalline silicon during ion implantation have been studied extensively. Low-energy ion irradiation used for various applications has further emphasized the need to understand the dynamics of low-energy collision cascades.

In this work the effect of the interatomic Si-Si potential on vacancy production in silicon has been examined using molecular dynamics simulations [1]. The dependence of defect production on the repulsive potential was examined by simulating full collision cascades in silicon produced by 1 keV silicon recoils. The simulations were carried out using three different repulsive interatomic potentials. It was found that although the repulsive potential has a significant effect on the number of recoiling atoms having energies greater than 15 eV, the number of vacancies produced is not significantly affected by the choice of the potential.

Molecular dynamics simulations using classical interatomic potentials tend to overestimate the number of defects produced in silicon compared to what is experimentally observed [2]. To examine the effect of the attractive interatomic potential on vacancy production, collision cascades produced by 300 eV Si recoils were simulated. The interatomic potential was modified to obtain different widths and depths of the potential well. The results indicate that the width of the potential strongly affects vacancy production. This suggests that interatomic potentials with narrower wells than those in commonly used potentials should be used to realistically simulate vacancy production.

The time evolution of different vacancy types was examined for a time period of several ps.

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Oscillations in photoluminescence excitation spectra as a measure of passivation of Zn acceptors in GaAs by Li.

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Abstract

Diffusion of GaAs:Zn samples with Li at 400-600°C enhances their photoluminescence (PL) intensity and causes two new bands to appear in their PL spectrum. Monitoring these bands we sometimes observe oscillations with the period of 42 meV in photoluminescence excitation spectra (PLE), when excited in the 750-800 nm wavelength range. We correlate the presence of these oscillations with the passivation of Zn acceptors by Li [Ref. 1].

Conditions for such oscillations are well known[2,3]. After very fast initial loss of excess energy by LO phonon emission[4], electrons leave the conduction band before thermalization is completed. At 14 K full thermalization requires several collisions with ions. We explain the appearance of oscillations with Li diffusion by assuming that passivation by Li reduces the concentration of charged ions (Zn^-) with which hot electrons can collide.

Of the two new PL peaks, the one with higher photon energy (1.447-1.48 eV) has the hallmarks of DA transitions. If the acceptor is Zn the donor must be about 40 meV below E_c. PLE oscillations are caused by energy dependent capture of electrons into these donors. Decay times of the PL are in the ns range except for excitation close to the bandgap, when ms time constants are observed.

The other peak or shoulder at 1.42-1.46 eV is absent at low excitation but grows very fast with higher intensities to become the major feature in some cases. This peak is quenched at lower temperatures than the other PL peaks.
When the Li concentration is high enough, so that compensation dominates over passivation, the oscillations disappear. Both PL bands are still present, but their shift with excitation intensity is larger, indicating fluctuations of the band edges[5].

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Planar Inductors for RF Integrated Circuits

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Abstract

Inductors are widely used in RF systems for realizing passive filters, in oscillators as energy tanks, matching of I/Os and widening the bandwidth of amplifiers [1], [2]. For large volume, portable RF systems for 1 - 2 GHz frequency range the number of discrete components will be minimized for increasing the productivity and reducing the size. We have developed a modeling and characterization technique up to 18 GHz for planar inductors, which can be manufactured with low cost, silicon technologies.

There are several common technological aspects defining the Q value of an integrated inductor like dielectric layers (SiO_2, Si_3N_4, polyimide), the thickness (usually 0.6 - 1.2 μm) and resistivity of metal layers (Al, Al-Si, Al-Cu) available from the process. Extra conductive layers like polysilicon or a well under the inductor - for isolating the inductor from the substrate - increases the Q value. By clamping all available metal layers together for decreasing the serial resistance of the inductor, optimizing the width of the inductor wires and space between wires it is possible to achieve Q values of 2 - 5 at 1 GHz with a low cost two metal layer silicon technology. Because of the low Q value there is only limited use of integrated planar inductors in real applications: as energy tanks in oscillators and amplifies, as baluns in mixers and matching. However accurate, distributed modeling over a wide frequency range is needed, Fig. 1 before introducing planar inductors as elements in integrated RF systems.

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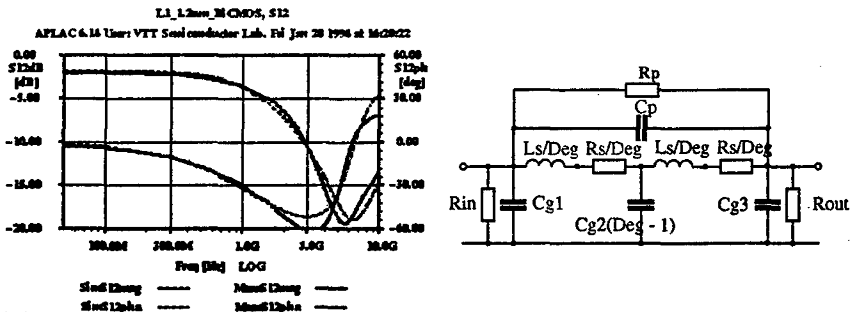

Fig. 1. a) Measured and simulated S12 of a planar inductor up to 10 GHz based b) on a distributed model. Deg is the number of the degree (here 3) of the distributed model.

Reflection and Tunneling in One-Dimensional Disordered Potentials

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One-dimensional tunneling through a region with a disordered potential is considered. The potential is modelled by Gaussian white noise. Two coupled stochastic differential equations of the Ito type for the phase and the absolute value of the complex reflection amplitude, and the corresponding Fokker-Plank equation for their distribution function are obtained. The equations are investigated analytically in the most interesting case of a weak transmission and solved numerically in the general case. In the limit of weak disorder the phase distribution function is almost uniform while in the limit of strong disorder the distribution function manifest a narrow peak. For both limiting cases a single differential equation for the probability distribution of the logarithm of the absolute value of the transmission amplitude is obtained. The developed approach can be used for investigation of other models of disorder, such as colored Gaussian noise or random telegraph signal.

Electrical Design of the Resonant Tunneling Diode

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Simple expressions for the key electrical properties of a RTD are derived. These are intented to be used for the optimization of the device performance. The expressions relate the processing parameters, ie barrier height and width, quantum well length, doping profile, etc to the peak and valley currents and voltages. Formulas for the elements of the ac-equivalent circuit are given and high frequency performance of the device is described.

A STUDY OF DUAL CONDUCTANCE RESPONSE TO CARBON MONOXIDE OF CdS AND α-$SnWO_4$ THIN FILMS

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The chalcogenides CdS and α-$SnWO_4$ are n-type semiconductors with band gaps typical for insulators. The semiconducting behaviour arises in both structures from native point defects; donors being related to oxygen vacancies in α-$SnWO_4$ and to cadmium interstitials or to sulphur vacancies in CdS. In the case of conductance response to changes in oxygen partial pressure, oxide materials like α-$SnWO_4$ may reflect changes in the amount of oxygen vacancies (donors) in addition to changes in the amount of adsorbed oxygen, while the first changes are not possible in the case of CdS. In the case of conductance response to carbon monoxide, for instance, some semiconductor materials show an unusual dual response so that conductance can either increase or decrease depending on temperature, CO partial pressure and treatments of the material.

This study considers the dual conductance response to CO of CdS and α-$SnWO_4$ thin films. An electro-hydro-dynamical spray technique was used for the deposition of CdS thin films from $CdCl_2$ and $(NH_2)_2CS$ solutions on a glass substrate. A variation of the stoichiometric composition of the films was achieved by mixing the initial solutions in different proportions of Cd/S ions. XPS was used for the determination of the atomic Cd/S ratios at the film surfaces. The films of stannous tungstate were grown by reactive co-sputtering in an 11% O_2/Ar atmosphere where a tungsten target was in RF mode and a tin target in DC mode. The films sputtered with 150 W power for both modes were found to have crystalline α-$SnWO_4$ structure after annealing at 400°C. X-ray diffraction and energy dispersive X-ray analysis (EDAX) together with Rutherford back-scattering spectroscopy (RBS) and conversion electron Mössbauer spectroscopy (CEMS) were used for the characterization of the films.

At temperatures below a border temperature T*, CO behaves as an oxidizing gas decreasing the conductance. T* for this dual conductance response to CO was found to be around 50°C for CdS films. The enrichment of the surface with cadmium species had a decreasing effect on T* which was also increasing with increasing partial pressure of CO. For α-$SnWO_4$ films, T* was around 250°C depending on the partial pressure of CO. In the case of CdS films, IR spectroscopy was also used, in combination with conductance measurements, for the study of the adsorption of CO. The results are discussed in terms of a model considering the correlation between local energy levels of the sorption subsystem and collective electronic characteristics of the crystal.

The Ionization Process of α Particles in Mesoscopic Structures: Simulation by Monte Carlo Method[1]

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The ionization caused by α particles plays an important role in semiconductor meso-structures (e.g. in CMOS memories). The incident α particle generates thousands of electron-hole pairs on a path of 1 μm.

First the properties of the α particle and the interaction with the silicon crystal lattice are summarized, thereafter the principles of the simulation are explained. Finally, as an example, results are presented for the 3D particle dynamics Monte Carlo simulation[4] of the ionization process and the current transients caused by an α particle passing through the depleted region of a reverse biased pn–junction.

The carrier distribution in the structure vs. time will be demonstrated. Initially, an extraordinarily dense electron - hole plasma is formed along the path of the a particle in its very close neighbourhood. The local carrier concentrations are close to the "concentration" of the Si ions in the crystal. It can be observed, that in the first phase the very strong Auger recombination consumes a sufficient part of the generated carriers. However, the remaining part of the generated electron–hole pairs is sufficient enough to initialize an avalanche process by impact ionization.

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- Digital Equipment Co. (External European Research Projects HG-001 and SW-003,
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- Swedish Institute,
- Hungarian Research Foundation (OTKA)

2 Permanent address: Technical University Budapest, Department of Electron Devices, H-1521 Budapest, Hungary

3 Permanent address: Uppsala University, Institute of Technology, Department of Solid State Physics, P.O.Box 534, S-751 21 Uppsala, Sweden

4 The principle of the simulation is described in the following references:

[1] K. Tarnay, F. Masszi, A. Poppe, P. Verhás, T. Kocsis, Zs. Kohári: A 3D Monte Carlo Semiconductor Device Simulator for Submicron Silicon MOS Transistors. Software Applications in Electrical Engineering (ed. P. P.Sylvester), Computational Mechanics Publ. Southampton-Boston, 1993 pp. 345-358

[2] K. Tarnay, F. Masszi, A. Poppe, P. Verhás, T. Kocsis, Zs. Kohári: The MicroMOS 3D Monte Carlo Simulation Program - a Tool for Verifying the MINIMOS Mobility Models. Simulation of Semiconductor Devices and Processes (ed. S. Selberherr et al.), Springer, Vol. 5. pp. 477-480 (1993)

[3] K. Tarnay, F. Masszi, A. Poppe, P. Verhás, T. Kocsis, Zs. Kohári: MicroMOS - a First Principle Based 3D Monte Carlo Simulation Program for Sub-half Micron Si MOSFETs. UPTEC 93 039R, June 1993

OHMIC CONTACTS BETWEEN MONOCRYSTALLINE N- AND P-TYPE SILICON LAYERS BY WAFER BONDING USING COBALT AS INTERFACIAL LAYER

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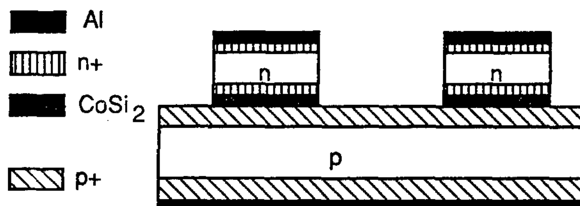
ABSTRACT

In this paper we will demonstrate a technique to bond a p-type wafer to an n-type wafer using an intermediate Co-layer. This technique will allow the formation of a direct contact between p- and n-doped layers with good ohmic behaviour due to the intermediate metal bonding layer. A test structure to determine the electrical properties of the n^+-p^+ contacts with an intermediate cobalt disilicide layer is demonstrated.

A p^+-layer is formed on a p-type (111) Si substrate by diffusion of boron from a boron-nitride source. A 300 Å thick Co-layer is deposited, using e-gun evaporation. Prior to evaporation, the wafer is dipped in diluted HF-solution to strip the oxide from the wafer surface. An n^+-layer is formed on an n-type (100) wafer, by diffusion of phosphorus from a $POCl_3$ source. Immediately after a cleaning step, the two front surfaces of the wafers are contacted. The wafers are bonded together at 800°C, in N_2 ambient, during the formation of cobalt disilicide.

One of the bonded silicon wafers (the n-type (100)) is then thinned by wet etching in KOH-solution down to a distance of 40μm from the silicide layer. The back side of the p-wafer is covered with SiO_2 and a second n^+ layer is formed to obtain good ohmic contacts to the n-side. The test pattern is then defined in the remaining n-type silicon by a KOH-etch and the silicide-layer is etched using an HF-solution.

The system is then characterised with IV-measurements to determine the quality of the contacts.



ELECTRICAL PROPERTIES OF Pt-$Si_{1-x}Ge_x$ AND PtSi-$Si_{1-x}Ge_x$ JUNCTIONS

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Schottky barrier height of PtSi-$Si_{1-x}Ge_x$ junctions have been determined for different Ge concentration by using I-V and activation energy techniques. The strain and the Ge content in the MBE grown $Si_{1-x}Ge_x$ have been analysed by high resolution x-ray diffractometer. The relation between measured Schottky barriers and the parameters of $Si_{1-x}Ge_x$ layer has been discussed. It is shown that the barrier height decreases with increasing Ge content in the strained $Si_{1-x}Ge_x$ layer and that PtSi-$Si_{1-x}Ge_x$ junctions are good candidates for infrared applications

A theoretically accurate mobility model for drift-diffusion power device simulation

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The well-known drift-diffusion transport equations, if the momentum exchange effect (carrier drag) of the electron-hole scattering is taken into account, can be extended with cross terms[3]:

$$J_n = -qn\mu_{n1}\nabla\psi + k_BT\mu_{n2}\nabla n + k_BT\mu_{n3}\nabla p \quad (1)$$

$$J_p = -qp\mu_{p1}\nabla\psi - k_BT\mu_{p2}\nabla p - k_BT\mu_{p3}\nabla n \quad (2)$$

Note that here the mobilities $\mu_{n1...3}$ and $\mu_{p1..3}$ are completely different from those in the commonly used drift-diffusion equations with no cross terms, and only two of them are actually independent from each other,

$$\mu_{n1} = \mu_{n2} - \mu_{p3} = \mu_{n2} - \frac{p}{n}\mu_{n3}, \quad \mu_{p1} = \mu_{p2} - \mu_{n3} = \mu_{p2} - \frac{n}{p}\mu_{p3} \quad (3)$$

These mobilities can be theoretically determined from the *Boltzmann* kinetic equation (BKE). Up till now, only zero-order solutions of the BKE (and consequently zero-order mobilities) have been used in device simulation. In this paper we report a general, theoretically infinite order solution method of the BKE using *Kohler's* variational principle, thus avoiding the relaxation time approximation, but including all possible scattering effects, where scattering matrices can be calculated in the first *Born* approximation (acoustic and optical phonon scatterings, ionized impurity scatterings both for electrons and holes, electron-electron, hole-hole, electron-hole and hole-electron scatterings, neutral atom scatterings and dislocation scatterings). An accurate mobility model has been defined, based on this solution:

$$\mu_{n2} = \frac{q}{m_n}\frac{1}{|G|}\sum_{r=0}^{N}\frac{(r+3/2)!}{(3/2)!}\,|D_n|_{2r+2,1}, \quad \mu_{n3} = -\frac{q}{m_p}\frac{1}{|G|}\sum_{r=0}^{N}\frac{(r+3/2)!}{(3/2)!}\,|D_n|_{2r+3,1} \quad (4)$$

with similar formulas for $\mu_{p2,3}$. Here $N \to \infty$, and the determinants $|G|$ and $|D|$ include the scattering parameters. This model has been installed into the device simulation code DYNAMIT[3]. The new mobility model (1st order, N=1) will be shown, compared to the old one (which corresponds to a zero-order solution, but with an experimentally fitted J^{eh} function[3]), on a 1200 μ long power PIN diode, at J=1000 [A/cm^2]. In more figures, the IV characteristics and the excess carrier and electric field distributions of the same diode and in the same operating point will be also shown, calculated by DYNAMIT with the old and the new mobility models, and with the program MEDICI (i.e. without any cross terms in the transport equations) using the CCSMOB (*Dorkel-Leturcq*-type) carrier-carrier scattering mobility model.

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3 see Velmre,Koel and Masszi: SISDEP '93 Proceedings (edited by S.Selberherr et al) pp.433-436

FABRICATION AND CHARACTERIZATION OF ION IMPLANTED PN JUNCTION DIODE/UV DETECTORS IN 6H-SiC

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Silicon Carbide is a well known material for high temperature and power electronics due to its wide bandgap (2.8 eV) and high breakdown electric field (5 x 10^6 V/cm). We are reporting an ion implanted pn junction diode, which was also tested as a UV light detector.

The diode was fabricated using Al ions implanted onto an n-type 6H-SiC substrate from Cree Research. A mesa structure was drawn using reactive ion etching to isolate the diodes from one another. The diodes were fabricated in different sizes, from 50 x 50 μm^2 to 500 x 500 μm^2 in steps of 50 μm.

The current voltage characteristics showed a good rectification and extremely small reverse leakage current in the order of pA range as expected in wide bandgap semiconductors. Fig.1 shows the I-V characteristics of one of the diode Area = 500 x 500 μm^2. The same diode was then placed under the UV lamp and an area of 100 x 100, 150 x 150 and 200 x 200 μm^2 was exposed to the UV light using a Micropattern generator equip with a UV lamp. By placing under the UV lamp an increase in the reverse leakage current in the range of nA was obtained. Fig.2 shows the reverse leakage current in four different cases (a) with no UV light, {off condition} (b) UV light on with an aperture area of light 100 x 100 μm^2, (c) UV light on with an aperture area of light 150 x 150 μm^2 and (d) UV light on with an aperture area of 200 x 200 μm^2. In the forward direction at about 35 mA of current the diode starts emitting blue light.

These results demonstrate that a good quality pn-junction diode has been fabricated on 6H-SiC material and a UV detector is realized.

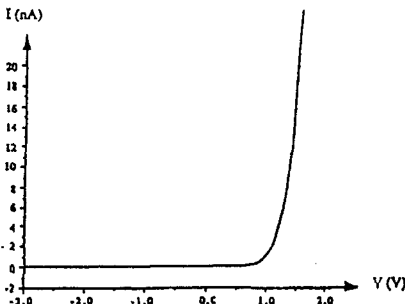

Fig.1

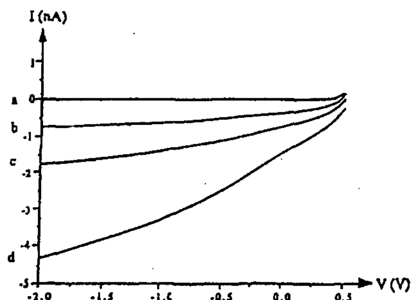

Fig.2

Tuesday morning

FIR Spectroscopy of Quantum-Dot Atoms and Antidots

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and
Max-Planck-Institut für Festkörperforschung, Stuttgart, Germany

Starting from two-dimensional electron systems in layered semiconductors structures with quantized energy levels in the z-direction, very small lateral structures with additional quantum confinement in the x- and (or) y-direction can be prepared. The ultimate limit of quantum confinement is a quantum dot, an artificial "atom" which contains only a very small number of electrons and exhibits discrete energy levels. Typical quantisation energies are some meV. In my talk I will address particularly far-infrared (FIR) spectroscopy on modulation-doped quantum-dots arrays in AlGaAs-GaAs heterostructure systems where the quantum confinement was induced by the field effect of a laterally modulated gate electrode. In these structures we observed discrete steps in the gate voltage dependence of the FIR-absorption strength indicating directly the incremental charging of each dot of the array with N = 1,2,3, and 4 electrons. It is found that a high single electron Coulomb charging energy of 15 meV stabilizes this well defined number of electrons per dots. Due to the nearly parabolic shape of the confining potential the excitation spectrum only reflects the center-of-mass motion of the many electron system. With taylored deviations from the parapolic potential we can excite internal relative motion within the atom.

I will also address a complementary structure with respect to dots, so call antidots, an originally 2DES with small geometrical "holes" "drilled" into the plane. The far-infrared excitations show a characteristic dispersion with a low frequency branch that can be characterized by a collective skipping orbit motion of electrons around the outer diameter of the geometrical hole. This behavior can be elucidated by circularly polarized spectroscopy.

Low Dimensional Systems

MAGNETO LUMINESCENCE OF NATURALLY GROWN InAs/InP QUANTUM WELL ISLANDS

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InAs/InP quantum well structures are investigated by magneto luminescence. From the magneto exciton energy shift, the amount of lateral localisation is deduced. The results indicate that the island formation in epitaxial growth may present an opportunity for producing naturally grown lateral quantum structures.

Increasing the strength of the exciton recombination is one of the key motivations for using lower dimensional electron systems in opto-electronic devices. Its strength depends on the overlap between the electron and hole wave function. Quantum well (QW) systems, with confinement in one dimension, are therefore successfully used in efficient light emitting and modulator devices. In principle, with confinement also in the lateral dimension, an additional reduction of the exciton radius can be achieved. The fabrication of such systems are however very difficult. Of substantial interest therefore, is to find semiconductor systems and growth procedures which produce lateral confinement in a natural way.

Here we present investigations of the magneto-luminescence of ultra-thin InAs/ InP QWs grown by chemical beam epitaxy (CBE). The structures consist of a single, 2 monolayer thick InAs QW layer, which after an approximately 10 sec growth interruption at the InAs-InP interface, deform spontaneously into a manifold of islands of different thicknesses . Covered by the large bandgap material InP, these InAs islands are found to form effective recombination centres.[1]

We will present our investigation of the exciton radius as a function of the well width, which has been determined from the diamagnetic shift measured with the magnetic field applied perpendicular to the QW layers and in the principal lateral directions.

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Intersubband infrared absorption in p-type GaAs/AlGaAs multiple quantum wells

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Intersubband absorption in quantum wells and superlattices has been offered a great deal of attention due to the potential applications in infrared detectors and modulators. Most of the experimental work has been performed using n-type structures, where the quantum mechanical selection rules for optical excitations require that the radiation field has a component perpendicular to the wells. In p-type quantum wells the strong mixing between the heavy (hh) and light hole bands (lh) for $k \neq 0$ gives rise to finite matrix elements for transitions with the polarisation in the quantum well plane. Hence the normal incident illumination geometry can be used, which is highly desirable for detector applications.

In this work the intersubband absorption in p-type GaAs/AlGaAs multiple quantum wells has been studied using Fourier transform infrared spectroscopy. Depending on the polarisation of the light, either intersubband-like transitions ($hh_0 \rightarrow hh_1$) or interband-like transitions ($hh_0 \rightarrow lh_1$) have been observed. The experiments are performed using a procedure to polarise the light by adjusting the boundary conditions for the radiation field at the sample surface.

Persistent Decrease of Dark Conductivity due to Illumination in AlGaAs/GaAs Modulation-Doped Heterostructures

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ABSTRACT

Modulation-doped heterostructures are of fundamental importance in modern high-speed electronics. They are superior to conventional MESFETs for low noise high frequency operation which, make them particularly suitable for supercomputers and sattelites. This is due to the fact that the two-dimensional electron gas (2 DEG) formed at the interface between the highly doped AlGaAs layer and the GaAs epilayer is used as a high conductivity path (high mobility and sheet carrier concentration) in high electron mobility transistors (HEMTs). Such structures allow short transit times and, hence, short switching times.

We report on a persistent decrease of the dark conductivity (NPPC) in AlGaAs/GaAs heterostructures due to illumination. The decrease was observed for photon

energies between 0.7 eV and 1.15 eV and larger than 1.4 eV in the temperature range $170<T<300K$. Using proper bias conditions the dark conductivity after illumination can be nearly a factor of two smaller than the dark conductivity in thermal equilibrium. The origin of this effect is best understood in terms of an interaction between the 2DEG formed at the AlGaAs/GaAs interface and the EL2 level in the GaAs epilayer. We have also established that the NPPC effect can be avoided by either changing the growth method from MOVPE to MBE or by applying a small positive bias to the substrate.

Initial Strain Relaxation and Optical Quality in Lattice Mismatched InGaAs/GaAs Single Quantum Wells

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Abstract

Lattice mismatched $In_xGa_{1-x}As/GaAs$ heterostructures are important in device applications such as lasers and transistors. The ternary layer can be grown within a critical layer thickness (CLT) which is measurable experimentally before destructive structural relaxation occurs. Among different types of structures, we have investigated initial strain relaxation and optical quality in $In_xGa_{1-x}As/GaAs$ single quantum wells (SQWs) as a function of In content, x, growth temperature, well and cap layer thicknesses using several structural and optical characterisation techniques. Samples were grown by molecular beam epitaxy with solid sources. The initial relaxation was caused by formation of misfit dislocations for $x<0.3$ and formation of three-dimensional islands for $x\geq0.3$. The CLT decreased with increased x and growth temperature. Optical degradation was hardly observed at the initial stage of relaxation caused by dislocations in terms of luminescence efficiency and linewidth broadening. In the case of formation of three-dimensional islands, the optical signal was still strong but broadened or even split into several peaks. For partially relaxed SQWs having a few dislocations, GaAs cap layer recovers part of the strain and thus improve optical quality with increasing thickness. Therefore not only the ternary well but also the cap layer thicknesses strongly influence the CLT. The compositional and temperature dependent CLT and the strain recovery with cap layer thickness could be explained by the mechanical equilibrium model proposed by Matthews and Blakeslee with inclusion of a friction force and a slight tensile strain of the GaAs cap layer. Finally the resolution of each experimental method was found to play an important role in detecting onset of relaxation.

Interband magneto-absorption in narrow-gap HgTe/CdTe superlattice structures

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We demonstrate that interband magneto-absorption is a powerful technique to determine the electronic band structure of narrow gap HgTe/CdTe superlattices. We use HgTe/CdTe superlattice structures grown on CdZnTe substrates by molecular beam epitaxy (MBE). The set-up for the absorption experiments consists of a Fourier transform spectrometer which is coupled to a superconducting magnet. The transmission is measured as a function of the photon energy for various magnetic fields up to 11 Tesla in Faraday geometry. The rich optical spectra permit extraction of superlattice miniband energies by extrapolating corresponding transition energies to zero magnetic field. The spectra also permit a close comparison with theoretically evaluated band structures and provide a valuable feedback to the MBE growth.
We will present measured spectra and extract the energy separation between hole and electron minibands in the superlattice structures. The experimental results are compared with numerical calculations.

Electron correlation effects in quantum dots

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Recently the quantum dots containing one, two and more electrons, say quantum dot "helium" and higher "elements" respectively, were created and investigated [1]. The exchange and correlation effects were shown to be of great importance [2]. The theoretical investigation of the correlation effects is based on the straightforward numerical Hamiltonian diagonalization in the many particle function space. It is rather laborious procedure.

We propose to treat the correlation effects in more simple way making use of the expansion in a power series in electron-electron (ee) interaction. The correlation effects are known to manifest themselves in the second order of that expansion already. The expansion is actually in dimensionless ee-interaction constant $\lambda = a_0/a_B (a_0 = \sqrt{\hbar/m^* \omega_0}$ is the characteristic quantum dot width and $a_B = \varepsilon\hbar^2/m^* e^2$ is Bohr radius) powers. Thus , the effective strength of ee-interaction can be easily varied by changing electron confining potential. Usually the values $\lambda \geq 2$ are of interest.

We calculated the first and second λ-expansion orders for the ground and some excited levels energy in the case of two electron in the quantum dot with the parabolic confining potential, and compared the obtained results with the known results of the exact numerical calculation. This comparison showed that two above orders are quite adequate in the $\lambda \leq 1$ region. However, this λ-expansion could hardly be used for larger λ values. It seems that in fact the λ-expansion is divergent.

We succeeded in calculating the electron energy for all λ values by means of renormalized λ-expansion such as was used in the case of nonparabolic oscillator problem [3]. The renormalized λ-expansion was constructed making use of the above two orders of λ-expansion, the asymptotic expansion for large λ values which was obtained in quasiclassical aproximation, and the symmetric properties of the Schrödinger equation. The above renormalized λ-expansion coincides with the exact result within 1% for all λ values.

The proposed renormalized technique is not restricted to the case of two electrons only. It can be also used in the case of quantum dot with the magnetic field applied as the magnetic field can be taken into account by the proper scaling of quantum dot dimensions and the corresponding interaction constants.

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Enhancement of the g-factor and spin-density wave state in a confined 2DEG in the quantum Hall regime.

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(May 19, 1994)

Abstract

We investigate the spin splitting of the Landau bands (LB's) in a confined two-dimensional electron gas (2DEG) using the Hartree-Fock approximation (HFA) for the mutual Coulomb interaction of the electrons. The exchange term of the interaction causes a large splitting of the spin levels of a LB whenever the chemical potential lies between them. These oscillations of the splitting with the filling factor of the LB's are conveniently interpreted as an oscillating enhancement of the effective g-factor, g^*. The reduction of g^* when a LB is becoming completely filled is accompanied by a spontaneous formation of a static spin-density wave state whose details depend on the system size and temperature.

71.70.Gm, 73.20.Dx, 75.30.Fv

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Dissipation in the quantum Hall effect by transverse circulation of electrons.

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Abstract. We consider a mid-plateau situation, where the Fermi level lies between the ν-th and the ν+1-th Landau level. The existence of a finite longitudinal field E_x results in an up hill (in the direction of the Hall field E_y) flow of the electron liquid with the current density $J_{liq}=\sigma_{yx}E_x=\nu\frac{e^2}{h}E_x$. Inelastic processes, which heat the lattice by phonon emissions, cause the excitations, (electrons in the ν+1-th Landau level and holes in the ν-th level) to move down hill. The excitation current density $J_{exc} = \sigma_{yy} E_y$ satisfies the condition $J_{liq} + J_{exc} = 0$, so that the total transverse current becomes zero. The up hill flow stores potential energy at the rate $J_{liq}|E_y|=\nu\frac{e^2}{h}E_x|E_y|$ per unit area. The rate of work done by external sources is $V_L \cdot I=L_xE_xL_y\nu\frac{e^2}{h}|E_y|$,showing that the rate of work per unit area is equal to the rate of storage, which again is equal to the rate of dissipation $J_{exc} \cdot E_y$. By the reversible up hill motion of the electron liquid, edge states of the ν-th Landau level and the levels below, which were empty for I = 0, will now be filled up to such an extend that electrons tunnel (or are inelastically scattered) into states of the ν+1-th Landau level at a rate that leads to a steady state. In this way electrons, which came up the hill by the reversible motion of the electrons in the ν-th and lower Landau levels, are circulated back (down hill) across the sample via the dissipative electron-phonon processes taking place within the ν+1-th Landau level. It is shown that dissipation by transverse circulation of electrons imply the temperature independence of the ratio $\frac{\Delta\rho_{xy}}{\rho_{xx}^{min}}$, where ρ_{xx}^{min} is the minimal value of the longitudinal resistivity at the given temperature T, and $\Delta\rho_{xy}\equiv\rho_{xy}(T)-\rho_{xy}(0)$.

Design and Fabrication

Characterisation of Semiconductor Wafer Surfaces by Light Scattering Topography

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Light Scattering Topography (LST) is especially developed to characterise semiconductor surfaces[1]. The LST system optically scans the surface and the resulting scattered light image displays the topographic form of the wafer. Different contributions to elastic light scattering are a) features on top of the surface (e.g. dust, remnants of treatments), b) features at the surface, resulting from surface treatments or polishing (e.g. roughness, scratches) and c) features below the surface (e.g. stacking faults). Elastic light scattering appears to the eye as haze. Term haze is used to describe mass effects related to surface roughness on a semiconductor wafer surface. It was also noticed to be harmful to semiconductor processing, if the haze level on wafers is too high.

Most often LST systems are used as defect or particle counters. These Light Scattering Anomalies (LSA was formerly called light point defect, LPD) are counted with advanced nanodefect scanners like ANS-100. It can detect particles from 0.1 µm up, spatial resolution is good and it can store the size and position information of each LSA detected.

This large amount of collected data needs to be fully utilised. Therefore we have developed a software package VTTWafer[2] for handling Censor ANS-100 data files. VTTWafer is a Windows™ program and it is also compatible with Windows NT. Software includes several modules for performing mathematical operations, including comparisons of different data on files and statistical computations. The software was designed to be fast, flexible and graphics-intensive. Features include 2-D and 3-D LSA maps, as well as haze maps, from individual wafers or averaged over multiple wafers.

The above mentioned tools were applied to silicon and GaAs wafer characterisation. We will present several examples of applications were we used LST successfully. In wafer cleaning experiments both particle removal efficiency and particles added by wafer pass were analysed. Determination of true particle removal efficiency in real processes was achieved with the VTTWafer software.

Defects in the surface region of the semiconductor wafers were also characterised using LST. Stacking faults on epi-wafers can be readily identified. In revealing Crystal Originated Particles a method for comparing wafers before and after processing particle-by-particle was utilised. These results will be discussed in detail in the forthcoming paper.

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Metallisation in sub-micron technology

a prestudy

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Abstract

Metallisation issues are of crucial importance when devices are scaled down to sub-micron dimensions where the polysilicon runners linewidth becomes comparable to the grainsize of the material. A thin silicide film is preferably used to decrease the resistance of polysilicon runners. While the linewidth is shrinked, the morphology of these thin and narrow runners has to be carefully controlled. Studies of grainsize, nucleation and stability are of great importance.

In this prestudy we have determined the titanium silicide phase and measured the silicide grainsize, thickness, surface roughness and sheet resistance on unpatterned wafers. The results will be used for reference in the main study of sub-micron silicide lines.

The titanium silicide was formed on 4000Å amorphous or polycrystalline silicon layers deposited on top of a 1000Å oxide. The silicon layer was arsenic, boron or undoped and activated by rapid thermal annealing (RTA) before being coated with either 600Å titanium or 400Å titanium with a 400Å titanium nitride cap on top. After silicide formation by RTA for 60s at 650°C, the unreacted titanium and the optional titanium nitride cap were removed from all wafers with a standard etch. X-ray diffractometry (XRD) was used to determine the silicide phase and grainsize. Rutherford backscattering spectrometry (RBS) gave the silicide thickness. Surface roughness was measured both by measuring the amount of scattered light from an incident laser beam with a total integrated scattering system (TIS) and with a conventional mechanical surface profilometer (Alpha-Step) with a diamond stylus. A four-point probe was used for sheet resistance measurements. The samples were subjected to a second RTA anneal at higher temperatures to transform the titanium disilicide from the metastable C49 phase to the low resistive and stable C54 phase. Measurement results before and after the second anneal were compared.

From this prestudy and previous work it can be concluded that the transformation from C49 to C54 phase does not significantly affect the morphology. The thickness of the silicide affects the transformation temperature. The doping of the deposited silicon layer affects the silicide growth during formation.

TiN cap during silicide formation	⇒	Smoother silicide surface
Boron doped silicon layer	⇒	Silicide surface smoother on α–Si than on poly-Si
		Silicide grainsize fairly insensitive to the crystallinity of the deposited silicon layer
Arsenic doped silicon layer	⇒	Silicide surface smoother on poly-Si than on α–Si, due to more pronounced arsenic enhanced grain growth of α–Si.
		Silicide grainsize larger on α–Si than on poly-Si

USING A 5:1 WAFER STEPPER IN PATTERNING LARGE AREA DEVICES

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Radiation detectors often require a very large area per one device. In case of strip detectors the size of one device could be for instance 20 by 80 mm^2 having two chips on a 100 mm wafer or 60 by 60 mm^2 having only one device per wafer. Conventionally these devices are patterned with 1:1 contact, proximity or mirror projection aligners using one exposure shot that covers all the wafer area. Using a 5:1 i-line wafer stepper it is possible to achieve 0.5 micron or even finer patterns and get rid of problems associated with other aligners, like contamination and mask wear. The image size of older 5:1 steppers is often limited to 10 by 10 or 15 by 15 mm^2, being in the modern and expensive equipment 20 by 20 to 23 by 23 mm^2. This implies that in patterning larger devices special tricks must be made.

We have developed a method to pattern any size of devices using a small field size 5:1 wafer stepper. In this example we pattern an ac-coupled strip detector with integrated bias resistors. The inner structure of most layers consists of narrow parallel lines that end to a bonding and contact areas. The bias resistors are located at both ends of the device. A common bias line and a guard ring encircle the whole device. An important notice is that this kind of device can be constructed from only nine different parts: one for each corner, one for each edge and one for the interior. The size of each part is determined according to device requirements. The reticle is like a small detector with only these nine basic parts. The stepper program picks the right part on the reticle, blanking the others, and exposes it on the wafer on the correct site. For every part this is repeated as many times as needed to make a detector of desired size.

Reticle blanking systems are never absolutely accurate. There is a shadow area ranging from 10 to 700 microns. Overlapping these shadow areas of two adjacent exposure shots never gives accurate results. We have used an opaque area on the reticle between adjacent parts i.e. images. This must be wide enough to blank the shadow area, also taking into account the mechanical inaccuracy of reticle blanking plates. Having this opaque area there is no need nor is it allowed to make any overlaps. The adjacent shots are simply exposed exactly next to each other on the wafer. Using an accurate wafer stepper no discontinuity at the borders of adjacent shots in exposed and developed pattern is found.

In practice there are evident limitations. The stepper should be very flexible. It must have an automatic reticle blanking system with a large or unlimited number of different images. Often the space on one reticle is not enough. An automatic reticle changing system is thus a necessity. Until now we have used maximum 25 images on 4 reticles. The required minimum number of images is usually nine. In theory any device can be patterned, but of course the stepper and reticle requirements are mitigated a lot if the structure of the device repeats itself with a constant period.

BiCMOS PROCESS FOR MOBILE RF-APPLICATIONS

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INTRODUCTION

Process sequence for simple BiCMOS with add-on self aligned NPN for CMOS process is presented. Emphasis is those steps that are needed for NPN transistor formation. Then main differences and additions to CMOS design rules and layer definitions are discussed. Finally some measurement results are presented. Main differences between this and standard non-selfaligned process are following: Epitaxial layer is not used which makes the process simple compared with buried layer/epitaxial processes. Only one polysilicon layer is needed for both CMOS and NPN fabrication, a saving of two mask layers compared with the standard process. Performance at high current levels has been sacrificied due to these process simplifications.

LAYER AND MASK DEFINITIONS

N-well and collector-well layers are generated in the design phase. Four physical masks are formed from these two layers: n-well, p-well, pmos-threshold and bipolar-base. N-well and P-well masks are used for well formation. Pmos-threshold mask is used for PMOS transistor threshold implant and bipolar mask is used for base formation. Same design rules can be used for n-well and collector-well layers. Deep collector contact diffusion is usually drawn around the whole transistor.Distance from active area is the most critical design factor. If too large distance is used transistor collector resistance will be too large for high frequency operations. If distance is too small transistor breakdown voltage will be too low and emitter and collector can be shorted.

PROCESS SEQUENCE

Collector contact diffusion is implanted with arsenic before local oxidation stack. Local oxidation nitride/oxide stack is grown using wet oxidation at low temperature and LPCVD nitride. P-well and n-well are implanted using complementary masks. Only one n-well implant is used. PMOS bulk and NPN collector concentrations will be equal. This concentration is too high for correct PMOS VTO, but VTO tailoring implant will be masked and higher than usual doses will be used. This should also remedy PMOS short channel problems.Well drive in and field oxidation are performed in one step. If field threshold implants are used, they are done between drive-in and field oxidation. Because both well concentrations are high, only n-field implant is needed, if distance from n-well edge to included active area is less than 4 µm. Both wells will be much deeper than is standard process with comparable lateral dimensions. Extra polysilicon layer which is used for capacitor plate and resistors is deposited, implanted and patterned before gate/emitter process. 17 nm gate oxide is grown in dry oxygen atmosphere. PMOS treshold implant is masked with pmos-mask. Simultaneous implant to both wells without mask is possible, but then new p-well dose should lowered. This change would be useful, as p-well and n-well concentrations would nearly equal and final placement of well boundary would nearer to drawn boundary. Base diffusion is masked with bipolar mask. Gate oxide is wet etched before implantation with boron. Base implant is self aligned to field oxide edge. Oxide etch before implantation should not be too long in order to maintain designed emitter area. If shallower junction is desired, BF2 with higher dose should be used. Rest of the process is similar to standard two metal CMOS.

MEASUREMENT RESULTS

MOS transistors have threshold voltages of 0.50 and -0.65 Volts. Unit delay for 19/0.8 µm inverter is 0.2 ns. Cut off frequency for 0.8x12 µm NPN transistors is 9 GHz.

A FINE PATTERN GTO THYRISTOR PROCESSED USING A SELF-ALIGNED PROCESS

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ABSTRACT

There is a clear trend towards smaller emitter dimensions in GTO thyristor design. This decrease in dimensions opens new possibilities to improve dynamic properties of the devices. The GTO thyristors are normally designed with a recessed gate which allows the device to be placed in a pressure contact. The processing of such devices with significantly reduced dimensions would lead to serious problems in the photolithographic patterning.

We have developed a self-aligned process utilizing standard steps from VLSI technology. The self-aligned processing replaces the photolithography in the most critical patterning steps. Those are gate contact definition, emitter junction passivation and gate metallisation and isolation.

The self-aligned gate contact definition uses the fact that thermal oxide is thicker on the n-doped mesas compared to the recessed and lower doped gate area. A subsequent etch-back uncovers the gate area. The oxide spacers on the sides of the mesas and the oxide on top of them are used as a mask during the implantation of the p-base contact doping and as the passivation of the cathode junction. The self-aligned patterning of the gate metal uses the fact of photoresist thickness variation between the mesa and the recessed areas. A partial etch-back of the polymer uncovers the emitters. This technique is later repeated with the polyimide instead of the photoresist to form the isolation on top of the gate metal.

We have processed and evaluated $2cm^2$ test devices using this technology. We have shown that it is possible to increase the yield while decreasing the cathode emitter size to 40*40µm. Each device consists of 176 $1mm^2$ large segments containing 100 individual emitters. The criterion of acceptance was that the leakage current of one segment should be smaller than 1mA at reverse voltage of 12V. The best results were 97% of the total number of segments and 23% of the devices accepted without repair in a batch containing 49 $2cm^2$ devices. Two lateral designs were evaluated. One with the 56µm spacing between emitters and the second one with the 30µm spacing.

The dynamic evaluation of the devices was performed under both snubbered and snubberless conditions. Under snubbered conditions, the maximum controllable current was measured with an inductive load against a voltage of 1600V. Under snubberless conditions the critical anode voltage has been determined in a range of dI_{RG}/dt values from -10 to -500A/µs.

Device simulations have been used to clarify experimental results. In particular the role played by the quality of the surface for the gate trigger current and forward voltage drop is demonstrated.

Application Of KTH-Laboratory III-V-Semiconductor Based Heterojunction Bipolar Transistors Towards Multi-Gbit/s 4:1 Multiplexer

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Technical Track: High Speed Devices and IC Design

Abstract

An HBT-based prototyping technology is being developed at The Royal Institute of Technology's Semiconductor Laboratory, aiming for transistors cut-off frequencies in the region of 70 GHz. Both AlGaAs/GaAs- and InP/InGaAs-HBTs have been fabricated showing cut-off- and maximum oscillation frequencies well above 60 GHz.

The overall circuit technology is based on two level metallization separated by silicon-nitride, NiCr-based resistors and MIM capacitors.

A 4:1 time division multiplexer was targeted to explore the feasibility of the in-house technology for MSI circuit implementations.

MULTICHAMBER-PROCESSOR FOR SMALL SEMICONDUCTOR LABORATORIES - THE FIRST RESULTS

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Silicon technology has advanced very fast during the last years: the diameter of the wafer has grown to 20 cm and the minimum line width is below 1 µm. All this has emphasized the single wafer processing. So in reactors the wafers are processed separately.
At the University of Turku in the Laboratory of Electronics and Information Technology we have been designing and constructing a research multichamber-processor for wafer diameter 150 mm since 1991. The goal is to build a modern compact silicon semiconductor processing reactor which should need only little clean room space and form a complete system for various process steps e.g. towards novel structures of silicon IC's. The system consists of three typical reaction chambers with a combined vacuum system. The first reactors are aimed for chemical vapor deposition, etching and sputtering. The dimensions of the prosessor including gas cabinets are about 3 m x 1.5 m x 1 m. The vacuum equipment consists of a mechanical pump and a turbo pump and UHV valves. The chambers are connected via flexible tubing and vacuum valves to the common element which is used to collect the residual gases for spectral analysis. The gas system contains nine high purity process gases with proper mass flow controllers, filters and valves. The whole system is regulated and controlled by using a special PC controlled process controller.
One of the key points of this system is to keep the wafer in controlled clean condition. The pretreated wafer is inserted into the special cassette out of which it is tranferred through the load lock to the reactor chamber, which is then pumped to a (ultra)high vacuum.
The first reactor was a low-pressure CVD-reactor which was aimed to study the production of silicon oxide films and especially silicon epitaxy at low temperatures and low pressures. Preliminary results after using the epitaxial CVD-reactor during the period of one year gave promising results. The growth rate of epitaxial Si has been studied intensively. Sofar we have succeeded in epitaxial growth in the temperature range of 650 - 750 °C. The process pressure was varied from 0.5 to 200 Pa. In these conditions the growth rate varied 1 - 5 nm/min. Initially, the quality of the formed films seem to be good, but the final characterization is to be completed.
The plasma etching chamber is ready for the operation and the third one for metallization is under construction. This novel type of a modular research reactor seems to be working satisfactorily.

Tuesday afternoon

Dissimilar Material Epitaxy: Growth and Properties of Metal/Compound Semiconductor Heterostructures

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Epitaxy of materials with different crystal structure, bonding and physical properties allows the fabrication of novel structures with exciting physics and device possibilities. Epitaxial metallic films grown on semiconductor substrates become particularly attractive when they consist of materials which are thermodynamically stable with respect to the underlying semiconductor. The overgrowth of epitaxial semiconductor layers is also possible under proper growth conditions. Two classes of metallic compounds, the transition metal aluminides and gallides and the rare earth monopnictides, have been used to grow III-V semiconductor/metal/III-V semiconductor heterostructures. The emphasis of this talk will be on the growth and properties of GaAs/$Sc_{1-x}Er_xAs$ heterostructures. Growth of other metallic compounds on III-V compound semiconductors will also be discussed.

Solid State Materials

Polyaniline - a versatile conducting polymer

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The recent discoveries of processability of polyaniline (PANI) has made it one of the most central conducting polymers today. The fusibility facilitates, for instance, blend concepts for bulk applications whereas the solubility gives rise to various thin film structures. To support such applicative efforts intensive research is being pursued. Polyaniline has been the subject in several Finnish research programs. Some results from these are presented in the paper.

The use of bulky surfactant counter-ions, such as dodecyl benzene sulfonic acid (DBSA), as dopants for PANI is the key to the processability. High p-type conductivity levels of the order of some 100 S/cm are achieved for the processable product. The maximum conductivity in polymer blends of PANI is reduced by 2-3 orders of magnitude. Surprisingly low percolation thresholds, below 1 wt%, are typically observed. Some commercial materials are already available. Various electromagnetic and antistatic shieldings are the main applications foreseen. Our studies, which have been focused on the electrical conductivity will be presented. The metallic transition can be seen for instance in the thermoelectric (TEP) behaviour. The EMI applications are related to high frequencies. Our impedance spectroscopy studies show the power law behaviour $\sigma(\omega) = \alpha\omega^s$, where $s \leq 1$ and ω the frequency, typical of a disordered material.

Thin film structures can be fabricated from solution e.g. by spin-coating. Technical applications such as transparent conducting electrodes have been demonstrated. Thin films also lend themselves to electronic device structures which can be used for the characterization of transport properties. By the latter method we have studied the conductivity and mobility in PANI prepared from solution by spin-coating or by the Langmuir-Blodgett (LB) technique. We have also used other technology oriented fabrication methods including evaporation from oligomers and a self-assembly process based on alternating dipping in two solutions. The latter method results in films which are conducting in the as-grown state. Common to all of these films is a low mobility, typically below 10^{-3} cm^2/Vs, which is of n-type, however. Accompanying optical measurements will also be reported.

Adsorption of Lithium, Caesium and Oxygen on a-Si:H

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Compared to the wealth of information now available on bulk properties of a-Si:H there is only a small amount of information relative to their surface properties. Lack of such type of information hinders the advance in technological applications of this important semiconductor material. Adsorption of lithium and caesium and the coadsorption of both alkali-metals and oxygen on a-Si:H surfaces were investigated by AES, XPS, UPS and secondary emission related to work function changes. Studies of metallic adsorbates on a-Si:H have been generally limited to transition metals which often complicate the experimental and theoretical analysis due to d-electron interactions. We have rather selected a simple alkali-metal/a-Si:H system as a means to investigate the fundamental aspects of the formation of metal-semiconductor interfaces. The Li-Cs/a-Si:H interface provides a model system for investigations into the initial stages of metallization of a semiconductor surface. Clean surfaces were prepared by low energy (400-600eV) argon ion sputtering and annealing. Sub-monolayer and monolayer ultra-thin films of the alkalis were deposited in UHV conditions and oxidized subsequently. In this report, the mechanism and kinetics for alkali-metal adsorption on a-Si:H surfaces will be presented and analyzed.

Cobalt Silicide Schottky Contacts to 6H-SiC

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Silicon carbide (SiC) has received considerable attention during the last years because of its suitable electronic properties for robust electronic applications [1, 2]. SiC devices have the ability to work at high temperatures for both high power and high frequency applications [3], and most of the common device structures from silicon technology have also been realised in SiC. However, future development of SiC device technology depends largely on the ability to form well controlled Schottky contacts and low resistive contacts [4].

In high frequency power circuits, Schottky diodes are superior rectifiers because of their low turn-on voltage and fast reverse recovery characteristics. Well controlled and thermally stable Schottky contacts are also essential for the fabrication of MESFET's and PBT's. Refractory metals and their metal silicides have been suggested as appropriate contact materials because of their thermal stability, low resistivity and reliability.

This study presents rectifying contacts in the Co / Si / 6H-SiC material system. Previous studies have shown that this system is rather well behaving since no cobalt carbides are formed [5]. Stochiometric $CoSi_2$ was formed by subsequently e-gun evaporated cobalt and silicon films that were annealed in a vacuum furnace.

The thermal stability of the contacts were investigated for temperatures ranging from 500°C to 900°C. Solid state reactions occurring during the heat treatments were monitored by RBS and XRD. SEM micrographs revealed changes in the surface morphology after heat treatment. Electrical investigation of the contacts were performed by C-V and I-V measurement at temperature ranging from 280 K to 475 K. The Schottky barrier height ϕ_B, the ideality factor η and the reverse leakage current I_{rev} were extracted from the measurements.

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Cross-sectional TEM and ohmic property study of (Au/Ni)/SiC contacts

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Abstract- The SiC technology is much less developed than e.g. the Si and GaAs-technology. Ohmic contacts are still a problem, especially for high-power and high-frequensy devices. We have investigated the properties of a Au/Ni ohmic contact, which is aimed for n-type 6H-SiC. 300 Å Ni and 900 Å Au were evaporated on 6H-SiC wafers ($n=1*10^{18}/cm^3$) at room temperature and alloyed at 600°C in N_2-gas for 5 min. The Au/Ni contact gave a specific contact resistance $\rho_c= 5*10^{-4}\,\Omega cm^2$, using a four-point method. Cross-sectional images taken with TEM show a sharp interface between the metals and the semi-conductor. The corresponding electron diffraction pattern chose that Au/Ni form a solid solution.

The Pt / Si(111) interface and the properties of thin Pt layers on Si

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The Pt / Si(111) interface is known to be reactive, and the contact reaction creates silicide like features in surface sensitive electron spectra taken during evaporation of Pt on Si, at room temperature (1). In the present study the near surface composition of the deposited Pt film is followed by Auger- and photoelectron spectroscopy, emphasizing the near surface- *and* deeper regions of the system. It is found, as seen earlier, that the upper surface develops a very thin layer with chemically reacted Pt and Si, but the Pt layer below is relatively free from Si. At higher temperatures, a (40 Å) thick Pt layer is penetrated by Si, but without forming a homogeneous compound. Instead a surface enriched in Si atoms is found. For reference purposes, similar experiments are made with an oxidized Si(111) surface. Here the oxide forms a barrier to a contact reaction between Pt and Si, which may occur only near the desorption temperature of the oxide layer, about 800°C. Neither in this case is a silicide formed by annealing. Signs of a more homogeneous metallic like compound are observed, however, during processing of a system of 15 Å of Pt *with a strong surface contamination of C and O.* In this case doubling of the Si plasmons occur, indicating the presence of a metallic system, with a high number of active electrons, at the surface.
The reactivity to oxygen was tested at room temperature and at higher temperatures. It was found that Pt at the Si(111) surface, in various concentrations and after different heat treatments, has a significant influence on the reactivity. A relatively thick layer of oxide may now be grown, with some features more towards SiO_2 than SiO_x.
By comparing the present results with those for Au / Si(111) (2), we believe that a sharp interface may continue to exist after deposition of more than a monolayer of Pt, but with a partial reordering of the 7x7 reconstruction. The Si adatoms are removed and segregate to the top surface where they are coordinated - or reacted - differently from the rest of the Si (surface) atoms.

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SiC - a semiconductor for high-power, high-temperature and high-frequency devices.

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SiC has in comparison with Si superior basic properties for applications in high-power, high-frequency and high-temperature electronics. The material has extremely high thermal conductivity (5 W/cm K), can withstand high electric fields (4 MV/cm) before breakdown and also high current densities. The high bandgap results in low leakage current even at high temperatures (> 700 °C). The potential applications of SiC were known decades ago, but the poor quality of the material produced at that time has delayed the device development. However, during the last years the crystal growth process of SiC has been improved considerably. Today 30 mm bulk wafers of reasonable quality are commercially available. The availability of such wafers has made it possible to develop the SiC CVD process faster. This is the background for the dramatically increased, recent interest for SiC. In this paper we will present some important properties of SiC, describe the two most common growth processes and discuss fundamental material problems that remain to be solved. A further aspect, which we will discuss, is that the polytypism of SiC may allow us to obtain generic knowledge of, for instance, defects in semiconductors. The emphasis will be on the work performed at Linköping University.

Thermal Oxidation of n- and p-type 6H-Silicon Carbide

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Silicon carbide, SiC, has been suggested as a suitable material for high temperature and high power electronic devices [1, 2], due to its wide bandgap and high thermal conductivity. SiC exists in several polytypes, but only three are commercially available: 6H, 3C (grown on (100) silicon) and recently 4H. When polishing the wafers, either the silicon face or the carbon face may be selected. Many characteristics of the material differ depending on which face is used, for instance oxidation rate [3] and contact resistance. Oxidation studies have received much attention, since high quality oxides will be needed for MOS-gates, insulation and passivation. However, most oxidation studies so far have concentrated on n-type material, neglecting possible difficulties with p-type material.

In this study both nitrogen doped (n-type) and aluminum doped (p-type) wafers with both silicon face and carbon face were used for the oxidation experiments. The oxides were grown at 1250°C in a dry oxygen ambient with and without chlorine addition. Polysilicon was subsequently deposited and phosphorus-doped using $POCl_3$. Aluminum was deposited and used as both the gate metallization and as a mask for dry etching of the MOS capacitors. Backside contacts of aluminum or nickel were used for the p-type and n-type silicon carbide MOS structures respectively.

Two types of electrical characterisations were used: CV-methods to compare flatband voltage shifts, and to determine oxide and interface charges; breakdown voltage measurements were used to compare the quality of the oxides [4]. The electrical measurements were made both at room temperature and at elevated temperatures. Secondary ion mass spectrometry was used to determine the amount of aluminum incorporated in the oxides on the p-type substrates [5].

This presentation will also give a review of the present theories of SiC oxidation. The following questions will be adressed: Do we understand the mechanism of silicon dioxide formation on silicon carbide? How does the oxidation on n- and p-type SiC differ? How does the oxidation on the silicon face and the carbon face differ? Can these oxides be used for MOS devices?

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Strain relaxation in epitaxial $Si_{1-x}Ge_x$ layers induced by the formation of $CoSi_2$

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ABSTRACT

Strain relaxation in $CoSi_2$/n-$Si_{0.9}Ge_{0.1}$ heterostructures is presented. Silicon molecular beam epitaxy (Si MBE) is combined with Co sputtering and Co implantation to obtain these structures. The strain in the $Si_{1-x}Ge_x$ is investigated after the formation of the $CoSi_2$ by using high resolution x-ray diffraction mapping in reciprocal space (HRXRD) and cross sectional transmission electron microscopy (XTEM). The results show that in order to keep the strain in $Si_{1-x}Ge_x$ unaffected, a sacrificial Si layer is needed. The direct formation of 80 nm $CoSi_2$ on $Si_{1-x}Ge_x$ can lead to defect formation and 60% strain relaxation .

High thermal conductivity silicon-on-insulator materials formed by wafer bonding.

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Wafer bonding is one of the most promising techniques for manufacture of Silicon-On-Insulator (SOI) materials [1]. The aim of this project is to use wafer bonding to combine different materials in order to form tailored and effective SOI material for specific applications where conventional SOI structures do not fulfil the requirements. An interesting case is when dielectric isolation *combined* with high thermal conductivity in the buried (electrical) insulator is required. We are currently investigating poly-crystalline diamond films as an example of a promising insulator material. The current state of our activities will be presented at the conference and in the proceedings.

Silicon-On-Diamond (SOD) materials formed by wafer bonding have the advantages of combining high thermal conductivity (diamond: ~15 W/Kcm), high radiation hardness and high electrical resistivity (10^{13} Ωcm at 10 V). The used poly-crystalline diamond films are deposited at Diamonex Inc., USA, by use of a hot filament CVD reactor in an atmosphere of methane in hydrogen.

Direct wafer bonding requires clean and smooth surfaces with rms surface roughnesses of typically ≤ 5 Å to be successful. As-deposited diamond films are considerably rougher and problems therefore arise. Further, since diamond is one of the hardest materials known, the possibilities to polish diamond are limited. Hence, other solutions to the problem are preferred.

To reach the goal of forming an SOD structure, several different techniques are under investigation. The first one is based on deposition of polycrystalline or amorphous silicon on top of the diamond followed by silicon polishing and a subsequent direct bonding to a silicon wafer. Preliminary results show that the polished surface can be successfully bonded to a thin silicon film (~10 μm) but not yet to a ordinary wafer, probably because of a non-optimized polishing procedure.

Another promising method is based on the use of the anodic bonding technique [2]. Successful experiments has been made to join two diamond-coated silicon wafers using this technique. This may seem surprising because of the rough diamond surface, but it is most likely explained by the fact that different bonding mechanisms are involved in anodic bonding and in conventional direct bonding. Still, the anodic bonding technique has to be improved for diamond, because the adhesive forces keeping the wafers together at room temperature disappear when the bonded structure is annealed at an elevated temperature.

In spite of the difficulties in polishing diamond we are planning to investigate two different methods to obtain a smoother diamond surface. The first deals with direct polishing of the diamond surface with an excimer laser and the second one is based on a hydrogen plasma treatment at an elevated temperature. Promising results using the latter technique have recently been reported in the literature [3].

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Optical Devices

Interferometric, low Thermal Mass IR-Absorber for Thermal IR Detectors Fabricated by Surface Micro Machining.

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Abstract-An absorber for a thermal IR detector has been designed. It features high absorption and low thermal mass. It can be optimised for a wide range of wavelengths and it is fabricated by using surface micro machining techniques. The latter are well suited for the fabrication of large detector arrays based on the bolometer, the pyroelectric or the thermoelectric principles

To absorb IR radiation, thin metal films, "black metal" or interferometric structures have been used but they normally suffer from either low absorption or high thermal mass. This absorber is an interferometric structure which will be compared to these conventional absorbers. It makes use of an air gap instead of a dielectric medium as a $\lambda/4$ layer. This replacement significantly reduces the thermal mass without reducing the absorption. Its spectral dependence is well adapted for the 8-12 μm window normally used by IR detectors for thermal imaging.

The structure consists of the following 5 layers (from the top), detector material, isolating dielectric medium, impedance matched metal, air-gap and a reflecting metal. The detector material is chosen according to what kind of thermal detector being used. The isolating dielectric medium should have low thermal conductivity and low thermal mass. The thickness of the first metal is set to optimise its wave impedance, the air gap is chosen as $\lambda/4$ to obtain destructive interference and the metal at the bottom should have highest possible reflection.

FABRICATION OF ERBIUM-DOPED SILICA WAVEGUIDES ON SILICON

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Erbium-doped glass waveguides can potentially be applied to active integrated optics operating in the 1.5 m wavelength band [1]. Planar waveguide technology on silicon substrate offers a view to the integration of optical components such as couplers, beam splitters, waveguide lasers and amplifiers into planar lightwave circuits. As a result of the intensive research work during the past few years the first demonstrations on the planar waveguide amplifier modules have been published [1,2].

We have used the flame hydrolysis deposition method to grow thick phosphorus-doped silica layers on thermally oxidized silicon substrates. The solution doping method has been used to introduce erbium ions into the grown oxide layer. Multimodal rib-waveguide structures have been formed with a three-level resist process and reactive ion etching.

The erbium-doping concentration was measured both with the Rutherford backscattering method and the energy dispersive x-ray spectrometry. The erbium-doping varied from 0.2 to 0.5 wt-% in different samples. The measured transmission spectrum showed a broad minimum around 1470 nm and a sharper absorption around 1535 nm which correspond well to the absorption spectrum of erbium in phosphosilicate glass [3]. The measured fluorescence peaks at 1536 nm as expected.

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Permanent Fixing of Optical Fibres on Silicon Substrates Using Bonding Techniques

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Abstract

In this work we present ways to attach optical fibres on micromachined silicon substrates, using bonding techniques. Nowadays the most used techniques are gluing and soldering which result in a thick and uncontrolled intermediate layer, giving a poor reproducibility. In addition, glues are known to suffer from creep and aging effects. The aim is to attach optical fibres in e.g. anisotropically etched V-grooves on silicon, with a high degree of precision and alignment. Two promising bonding techniques have been investigated, i.e. anodic bonding and Au-Si eutectic bonding of glass fibres in V-grooves. Anodic bonding is performed at an elevated temperature, typically 400 °C, and with an applied voltage of about 400 V. The Au-Si system has its eutectic temperature at 368°C, which can be used to create a bond between the silicon substrate and the gold-coated fibre. A possible third technique is bonding with the aid of silicidation of an intermediate metal layer. Here the fibre will be coated with a metal that easily forms a silicide, e.g. platinum. These techniques have in common that they are relatively low temperature techniques, which is of fundamental importance due to the different thermal expansions of silicon and glass. At the conference, a comparison of the techniques will be given with respect to bonding strength and feasibility.

The rapid developments of integrated electronic components and systems are well known. The building practice has become the limiting factor for the overall system capacity. This calls for new techniques for packaging and building practice which enable more compact structures. The trend is going towards optical integrated circuits, i.e. hybrid technologies where integrated, monolithic building blocks are put together to form more complex systems. Important areas of applications that call for a more compact building practice are: telecommunication links as well as medical, electrical and chemical sensor systems. Important ingredients in such a new building practice, we believe, are anisotropic and selective etching for three-dimensional structuring of semiconductors and solid-state bonding of surfaces to combine them.

UV-sensitive Photodetectors based on metal-semiconductor contacts on 6H-SiC.

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ABSTRACT

Schottky diodes on Silicon Carbide are interesting for use in different applications because of the relatively simple fabrication process. Many metals form dic les with high schottky barriers when deposited on silicon carbide. A number of reports on diodes made from Pt, Co, Ti, Au and other metals exist in the literature. In this work we demonstrate that Schottky diodes on 6H-SiC can be used as photodiodes.

The diodes were made by evaporation of Ti on an n-type 6H-SiC wafer with an epitaxial layer on top of it.The doping of the epitaxial layer was $N_D=2*10^{16}$ cm^{-2}. Finger shaped openings in the metal were formed by a standard lift-off method. Finger widhts are in the range 1 - 2 µm. A back contact is made by evaporation of Al on the back side of the wafer.

The diodes were electrically characterised by IV and CV measurements. The ideality factor was close to unity and the reverse leakage current was below 1 nA at low reverse voltages.

Optical measurements were made using a monocromator in the spectral range 200 - 400 nm. Light enters the diode through the finger shaped openings in the metal. The measurements indicate good sensitivity to UV-radiation with a peak response below 300 nm. The photoresponse of diodes with different areas and different finger widths are compared.

The results form the measurements are compared with results from simulations made with MEDICI and optimization of the structure for increased sensitivity in different spectral ranges is discussed.

Large area GaInAsP and GaInP solar cells for space application

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Phosphorus containing III-V compound semiconductors, such as GaInAsP and GaInP have shown excellent stability of their material parameters when irradiated by high-energy particles and therefore they are considered as good candidates for space solar cell materials [1,2]. In comparison to InP, these materials have the advantage that they can be grown lattice-matched on lighter and mechanically stronger GaAs or Ge substrates. Moreover, by appropriate choice of energy band gaps solar cells of these materials can be also made current-matched to Ge (GaInAsP) and GaAs (GaInP) when utilized as top cells in monolithic tandem cell structures under AM0 illumination.

We report the fabrication and characterization of large area (1×1 cm^2) $Ga_{0.84}In_{0.16}As_{0.68}P_{0.32}$ (E_g=1.50 eV) and $Ga_{0.51}In_{0.49}P$ (E_g=1.88 eV) solar cells. The cell structures were grown by gas-source MBE on 2" (100) GaAs substrates. Both n-on-p and p-on-n structures were processed and studied. For the InGaAsP material, the n-on-p cells showed significantly better active area conversion efficiencies (17.5% at AM0, 1-sun illumination) than p-on-n structures (13.0%, same conditions) due to lower sheet resistance of the n-type GaInAsP emitter layers and longer minority carrier diffusion length in p-type base layers. For GaInP cells the best conversion efficiency of 14.0% was also achieved for n-on-p structure. Since only single layer of SiN_x was utilized as an antireflection coating, we expect that the application of an optimized two-layer antireflection coatings could increase the efficiencies up to 19% and 15% for GaInAsP and GaInP solar cells, correspondingly. The excellent uniformity in all the cell parameters across the 2" wafers indicates that larger area solar cells (up to 10 cm^2) can be fabricated.

The results reported make it possible to proceed to the next step - the development of monolitic tandem solar cell structures fabricated of GaInAsP/Ge and GaInP/GaAs. A preliminary estimation shows that such structures can exhibit efficiencies over 25% at AM0, 1 sun illumination, along with excellent radiation resistance [2] and therefore they are very promising candidates for space applications.

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Conjugated polythiophene polymers in light emitting diodes: From the blue into the infrared

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Polythiophenes with alkyl and alkylphenyl substituents, with bandgaps from 1.8 to 3 eV, have been synthesised and used in polymer light emitting diodes. The bandgap is systematically tuned by the pattern and character of substituents on the polythiophene main chain. By using these soluble polymers as the active layer in light emitting diodes we have obtained the colours blue, green, red and infrared, with quantum efficiencies reaching the 0.1-1 % range. Using multilayers we have obtained multicolour emission in these diodes. Special geometries allows the use of these polymer LEDs as ≤100 nm diameter light sources.

We discuss the electrical and optical aspects of electroluminninescence in conjugated polymers, based on these results. Contributions from exciton transfer in multilayers is presented. The technical implications of flexible, multicolour polymer LED's are discussed.

FITTING OF THE SOLAR CELL IV-CURVE TO THE TWO DIODE MODEL

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The current versus voltage characteristics of a solar cell under illumination is commonly translated to an equivalent circuit containing a photocurrent source and a diode with a shunt resistor, and a series resistor in the load branch. To get a more accurate fit to a measurement data, a second parallel diode is sometimes added to the circuit. The two diode model allows one to separate the diffusion current term, in which the diode ideality factor n equals 1, and the recombination current term, in which the diode ideality factor n equals 2. The other model parameters are the photocurrent density, Iph, the diode saturation currents Is1 and Is2, the shunt resistance Rsh, and the cell series resistance Rs.

The task for extraction of the five model parameters from the cell current equation is not analytically solvable, and iterational methods must be used to fit the measured current versus voltage curve to the equation. The fit can be based on a set of five equations derived from the current equation in different ways. To proceed for the solution, a Newton-like 5x5 matrix iteration can be done. Another way is to solve as many parameters as possible with respect to a smaller set of parameters and iterate from this limited set of equations. With a proper choice of starting equations, four of the parameters can be presented as a function of the series resistance only, as presented in this paper. The series resistance Rs remains to be iterated. As the parameters Iph, Is1, Is2 and Rsh are represented as functions of Rs only, and should be positive in sign in the correct solution, one has a very effective mean to narrow out the Rs ranges inside which the solutions are to be found.

In this paper, the five base equations are derived from the cell current equation in the short circuit, open voltage, and maximum power points. The input parameters defining the specific cell under study are the short circuit current, the open circuit voltage, the voltage and current in the maximum power point, the current versus voltage curve slope at short circuit, and temperature. The derivation of the formulas for the four parameters as a function of Rs is straight forward, as will be shown. The parameter extraction is initiated by checking the range of Rs inside where positive values of Iph, Is1,Is2 and Rsh can be found simultaneously. The correct value for Rs is then iterated in this range.

Wednesday morning

Transport Spectroscopy on Quantum Dots

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A quantum dot is characterized by a discrete energy spectrum and therefore far infrared spectroscopy in an important tool to characterize the system (see talk by D. Heitmann). In addition transport measurements on dots, where the small island is electrically connected to reservoirs by tunnel barriers, give additional information about the electronic properties of such a system. Not only the discrete energy spectrum of such a dot but also the Coulomb charging energy influences the measurements.

The talk gives a review about electrical measurements on GaAs/AlGaAs quantum dots where the island is formed either by a lateral confinement of a two-dimensional electron gas or by AlAs barriers like in a resonant tunnel diode. The conductance is analyzed as a function of the electrostatic energy of the dot, the source-drain voltage, the magnetic field etc. and the measurements demonstrate that not only optical measurements can be used to do spectroscopy on quantum dots.

Modelling of Devices

Unified Capacitance Modeling of MOSFETs

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Abstract

Accurate modeling of MOSFET capacitance-voltage (C–V) characteristics is needed for precise simulation of the transient and small-signal behavior of MOSFET/CMOS circuits. Previously, we introduced a modification of the simple C–V model by Meyer[1] in order to account for subthreshold conditions, using the concept of a unified channel capacitance[2]. However, a serious drawback of the Meyer model is the use of reciprocal capacitances between the terminals which forces charge conservation to be violated in this model[3].

Combining the Unified Charge Control Model (UCCM)[4] of FETs with a charge based model description, utilizing a precise description of the bulk charge in terms of body plot parameters, we were able to derive a more accurate, charge conserving C–V model which also accounts for non-uniform doping profiles and for short channel effects[2,5]. This model is, however, somewhat cumbersome to implement in SPICE.

Here, we describe yet another unified C–V model for MOSFETs suitable for implementation in SPICE. This model utilizes an approximate, analytical solution of UCCM in combination with the charge conserving, Meyer-like approach proposed by Turchetti et al.[6] – all within the Quasi-Static Approximation. The present model was implemented in our circuit simulator AIM-Spice[2] and was tested by simulating various demanding benchmark circuits such as charge pumps, switched capacitor filters and dynamic RAM cells[7]. These tests clearly reveal the shortcomings of the original Meyer model, while the results obtained using the present model compare favorably with analytical estimates of the behavior of the test circuits.

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GaAs/AlGaAs quantum well infrared photodetector arrays for thermal imaging applications

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ABSTRACT

The performance of GaAs/AlGaAs multiple quantum well infrared detectors is studied theoretically and experimentally, with special emphasis on 8-12 μm thermal imaging applications. The dependence of detector performance on various factors like light coupling configurations (one and two dimensional reflection gratings with or without waveguides), detector temperature, response wavelength and quantum well doping density is dealt with. It is found that an optimised 32 μm x 32 μm detector pixel (a detector pixel size suitable for large staring arrays, i.e 256x256 or larger) with 9.0 μm cut-off wavelength, f#=2 optics and 70% optical transmission reaches back ground limited operation at 74 K detector temperature.

The potential of making highly uniform staring arrays utilising the mature GaAs material and processing technology is demonstrated by uniformity measurements of detector dark current and absorption wavelength. The experiments show that a metalorganic vapour phase epitaxy (MOVPE) grown structure can have a dark current standard deviation over a 10 mm long linear detector array of less than 2%.

The staring array performance in terms of noise equivalent temperature difference (temporal NETD) is calculated to NETD <20 mK at 77 K detector temperature and NETD <10 mK at 70 K detector temperature.

A Compact Model for the Cut-Off Frequency in High Speed Bipolar Transistors

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Abstract

Analog IC design based on modern bipolar transistors requires accurate device models for circuit simulation. We have developed a compact but physical model suited both for pure silicon bipolar junction transistors (BJT) and $Si_{1-x}Ge_x$/Si heterojunction bipolar transistors (HBT). The application of strained silicon-germanium alloys to HBT technology provides many advantages over the conventional silicon BJTs. The SiGe-base hats allow extreme vertical scaling without excessive base resistance for high speed performance. In addition to having already established record cut-off frequency performance (75 GHz), SiGe-base HBTs can also offer analog designers a very high current gain through dramatically improved Early voltages. Our model for the cut-off frequency is based on the de Graaf-Kloosterman formalism [1] for the modelling of the bipolar transistors, but adds important heterostructure device physics as well as physical properties of SiGe material. The model, implemented in APLAC circuit simulator, shows how currents and charges depend on minority carrier concentrations, which in turn are functions of the junction voltages. In this way the influence of the built-in electric fields due to doping density and Ge concentration gradients, the bias-dependent transit times, and the Early effect can be incorporated naturally. Comparisons between the model prediction and the experimental data for the DC current/voltage characteristics and cut-off frequencies both in Si BJTs and in $Si_{1-x}Ge_x$/Si HBTs have been made to demonstrate the model utility and accuracy. Figs. 1 and 2 show that the agreement between the measured [2] and simulation results is very good both for dc and high frequency characteristics.

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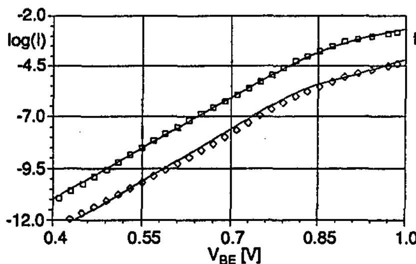

Fig. 1. Simulated (——) and measured base (◊) and collector (□) currents vs. base-emitter voltage in a SiGe HBT (x=0.08).

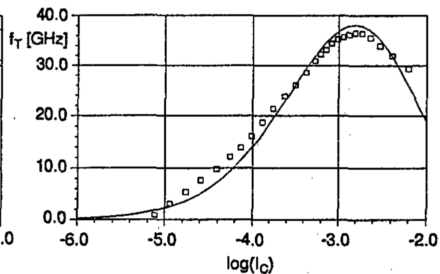

Fig. 2. Simulated (——) and measured (□) cutoff frequency vs. collector current in a SiGe HBT (x=0.08).

A Study of Turn-Off Failure Mechanisms in GTO Thyristors of Different Anode Designs Supported by 3-D Simulations

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Abstract – The destructive failure mechanisms in dynamically operating thyristors are still subject to great confusion. Nonetheless, the dynamic destruction due to local melting of devices operating near the safe-operating area (SOA) limit is a major problem for device designers and system manufacturers. A clear and unambiguous understanding of the physical processes occurring in the turn-off phase of operation, is a necessity for further development of *e. g.* high-power gate turn-off (GTO) thyristors.

In previous papers, we have shown that at least two dynamical mechanisms may serve as origins for destructive turn-off failure in GTOs [1, 2]. The principal phenomenon responsible for these mechanisms is the development of an unevenly distributed electric field of the device blocking junction, which is denoted as the quasi space-charge region (QSC). Thus, depending on how this QSC develops, either a dynamic punch-trough failure or a dynamic avalanche-injection failure may occur.

In this paper, three types of anode designs, which all are considered by device designers, are investigated regarding the above outlined failure mechanisms. The "Ring" and "Finger" type of anode designs represent different anode shorting patterns whereas the "n^+-stop" type anode design has a covering anode structure in combination with a buffer layer.

The investigations are based on electrical measurements in conjunction with optically based time-resolved 2-D measurements of the excess-carrier redistribution in the turn-off phase of operation [3]. The measurements show the development of the QSC for turn-off operation near the SOA limit of the "n^+-stop" type of device. The QSC will extend to the vicinity of the anode region. However, a genuine punch-through process is obstructed by the presence of the highly doped buffer layer, but, nevertheless, a locally increased anode injection implies a localized drift current region that may be of a destructive nature.

In the shorted-anode type of devices, the buffer layer is omitted, and, hence, the QSC may reach the anode region thus invoking a more genuine punch-through turn-off failure. In this case, the field region is represented by an increased carrier density in the measured turn-off carrier-map sequence. This reflects that a diffusion current is flowing in this region. Further on, the two types of anode shorting patterns will act differently as regards the turn-off failure tolerance. This is due to the different situations of field distribution in the blocking junction.

This paper will clearly show the impact of design differences of power GTOs in terms of physical mechanisms of the turn-off failure. The measurements are vigorously supported by 3-D computer simulations.

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Simulation of the electrical and thermal behaviour of SOI/SOD devices

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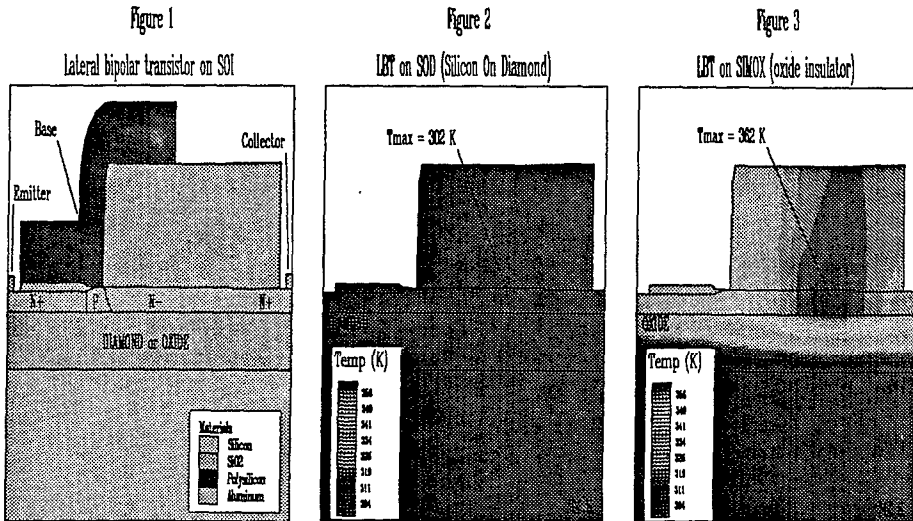
Silicon-On-Insulator (SOI) device technology has many well known advantages compared to silicon bulk technology. However, self heating effects in SOI devices are believed to be a serious problem. Negative resistance in MOS devices which limits the current drive, and thermal runaway in bipolar devices, are examples of self heating effects. The heating of the devices is caused by the poor thermal conductivity of the buried silicon dioxide. A promising replacement to the oxide is diamond, which has very high thermal conductivity and high electrical resistivity. It is therefore believed that many of the thermal problems can be avoided with the use of silicon on diamond material (SOD) instead of silicon on oxide.

The purposes of this work are to simulate how the electrical behaviour of different SOI devices are affected by the thermal properties of the buried insulator material, and to determine the thermal and electrical requirements of future SOI/SOD materials. A lateral bipolar transistor (LBT) on SOI material , figure 1, was used in the simulations. Figures 2 and 3 shows the temperature distribution in the device at a steady state solution for the cases of diamond and oxide as the buried insulator. No significant increase of the temperature is seen in the SOD material, figure 2, while for the other material the buried oxide acts as a thermal isolator which causes heating of the LBT, figure 3. The simulations also show that SOD devices had higher cut-off frequencies, and thermal runaway effects were suppressed.



Extrinsic versus Intrinsic Models for FETs

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Abstract

As integrated circuit technology advances and the channel length of FETs are steadily reduced, the importance of the source and drain parasitic resistances, R_s and R_d, become increasingly important in the overall operation of the devices. This is due to the fact that in scaled down devices, the value of the channel resistance becomes comparable to the parasitic resistances.

In the equivalent circuits used for modeling such devices, it has been common to either neglect R_s and R_d altogether (intrinsic model) or to combine the intrinsic model with additional nodes to account for the parasitics. However, with the introduction of new analytical techniques, it has become possible to include R_s and R_d directly into the expression for the drain current, resulting in so-called extrinsic models[1,2].

In this paper, we compare extrinsic and intrinsic models in terms of computing speed and accuracy. We also point out problems with extrinsic models encountered in cases where gate leakage current is present and in simulating transients.

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THE EFFECT OF USING DIFFERENT TRANSPORT MODELS IN COMPUTER SIMULATIONS OF THE PERMEABLE BASE TRANSISTOR

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ABSTRACT

Numerical simulations of the Permeable Base Transistor (PBT) has been performed using MEDICI Ver. 1.0. The PBT is a short channel device and hot electron effects are expected to be important and the transport model used in the simulation is critical.
The present work compares the effect of different transport models on the operation of a sub micron PBT. The transport models used are the ordinary drift-diffusion model and the hydrodynamic model as they are implemented in MEDICI. In sub micron devices the transport parameters become both device and bias dependent. The transport parameters are directly related to the distribution function and should be extracted from the solution of Boltzmann's Transport Equation (BTE). However, if the distribution function is known we have all information about the device and no further simulation is needed. The most popular and effective way of solving the BTE is Monte Carlo simulation. Monte Carlo models carrier transport in an accurate way, but suffers from large simulation run times. Present work includes a comparison between simulations using bulk material transport parameters and device dependent transport parameters extracted from Monte Carlo simulations.
The Monte Carlo simulation is based on a full band bulk Monte Carlo program from University of Illinois [1]. The program has been upgraded to include many particle simulation, constant time technique for free flight generation and a fourth and fifth order Runge-Kutta algorithm for solving the equation of motion. The parameter extraction is made from a Monte Carlo simulation using one dimensional boundary conditions for particles and a fixed electric field extracted from two-dimensional simulation in MEDICI. The Monte Carlo simulation, parameter extraction and MEDICI simulation has been repeated until the change in electric field between iterations could be neglected.
Both I-V and f_T results has been analysed. It is clear that the hydrodynamic model gives higher current levels and higher f_T than the drift-diffusion model.

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MONTE CARLO SIMULATION OF HOT CARRIER NOISE IN SHORT n^+nn^+ DIODES

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The correlation functions of the current and voltage fluctuations and their spectral densities are known to play a rather essential role in theoretical consideration of hot-carrier transport in semiconductor devices. On the one hand, the time and frequency behavior of the fluctuations reflect both dynamic and relaxation processes inherent for the hot carrier system and can be used for detailed investigation of the physical phenomena responsible for the device performance. On the other hand, noise consideration is of great practical importance since the frequency dependence of the current and voltage fluctuations determines the lower limit of a device sensitivity and can also indicate appearance of generation processes. The Monte Carlo Particle method is the most appropriate for hot-carrier noise investigations since it allows the correlation functions to be calculated by a natural way using a time-averaging over a multi-particle history simulated during a sufficiently long time interval.

In the present work the Monte Carlo methods are applied to calculate the current- and voltage-noise in short n^+nn^+ InP and GaAs structures. The noise calculations have been carried out in parallel with the hydrodynamic modelling of the small-signal admittance and impedance of the same diodes. This allows the noise features to be interconnected with spectral behavior of the negative differential resistance of the diodes. Quite different behavior of the noise features are observed under the voltage and current driven operations. Under the constant voltage operation the time dependence of the current fluctuation correlation function exhibits damped oscillations at the transit-time and plasma frequencies. This results in appearance of two spikes in the current noise spectrum at corresponding frequencies. Similar peaks are observed in the frequency dependence of the small-signal admittance. The transit-time oscillations and the corresponding noise are shown to be connected with formation of the differential negative resistance caused by the Gunn-effect. In contrast, the voltage noise spectrum has a regular Lorentzian shape under the constant current operation. It reflects a presence of a big external resistance which damps all oscillations.

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Growth and characterization of compositionally graded $Si_{1-x}Ge_x$

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It has recently been shown that relaxed, epitaxial $Si_{1-x}Ge_x$ layers of any composition and thickness can be grown with a low density of threading dislocations on Si substrates by molecular beam epitaxy (MBE) or chemical vapour deposition (CVD). This has been achieved by growing the top layer of the required composition on top of a buffer layer in which the Ge content has been increased gradually. Threading dislocation densities between $1x10^5$ and $1x10^6$ cm^{-2} in the top layer have been reported.

We have performed detailed measurements of the properties of compositionally graded $Si_{1-x}Ge_x$ grown by MBE on <100>-oriented Si substrates. Growth parameters such as composition, temperature, doping, and grading have been varied. The epitaxial layers have been characterized by combining information from a number of experimental techniques such as Rutherford backscattering spectrometry/channeling, transmission electron microscopy, atomic force microscopy, photoluminescence, Hall effect versus temperature, and deep level transient spectroscopy.

We have found that for growth temperatures higher than ~700°C and a linear grading of 10%Ge/μm fully relaxed $Si_{.75}Ge_{.25}$ epitaxial layers of high structural and electrical quality can be grown. The layers are characterized by a channeling χ_{min} of 4%, a threading dislocation density of ~$1x10^5$ cm^{-2}, and strong near-band gap luminescence. Electrical measurements have revealed Hall mobilities similar to published bulk values and concentrations of electrically active deep levels less than $5x10^{12}$ cm^{-3}. The surface morphology of these epi-layers is, however, strongly influenced by the grading procedure which produces a high degree of crosshatcing.

RBS Channeling Spectroscopy of Ge implanted epitaxial $Si_{1-x}Ge_x$ layers

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RBS channeling spectroscopy was used for optimizing high-dose Ge implantation into (100) Si substrates. $Si_{1-x}Ge_x$ layers were formed through the implantation process. For tailoring the distances between the original amorphous/crystalline (*a/c*) interfaces and the Ge profile maxima, and ensuring the strained epitaxial regrowth of the implanted SiGe layers, two alternative implantation techniques along with that of the single-energy Ge implantation were separately adopted: the double-energy Si^+ and Ge^+ implantation recipe, and the double-energy Ge^+ and Ge^{++} recipe. All the implanted samples were epitaxially regrown at 600°C. The RBS channeling measurements confirm that the double-energy Ge^{++} and Ge^+ recipe is optimum since it can result in fewer residual defects, significantly reduce implant processing time, and provide the possibility to wilfully tailor the spatial separation between the original *a/c* interface and the Ge profile maximum.

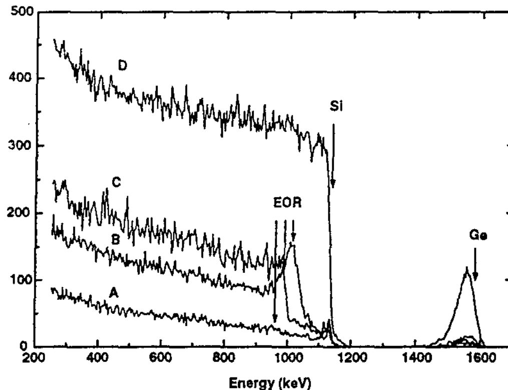

Figure: *RBS Channeling spectra.* **A:** double-energy Ge^+ and Ge^{++} implantation; **B:** double-energy Si^+ and Ge^+ implantation; **C:** single-energy Ge^+ implantation; **D:** random spectrum of A. All the samples were annealed at 600°C.

Etching of the BLM Layers in a Fluxless Flip Chip Process

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Etching of the ball limiting metallurgy (BLM) was examined to develop a fluxless flip chip process. Silicon wafers with test chips containing 1224 electroplated 90 %-10 % Pb - Sn solder bumps were used for the process evaluation. The bumps were used to mask the BLM etching and the reflow was carried out in a N_2 or Ar/H_2 ambient.

Wet etching and reactive ion etching (RIE) using SF_6 were tested for patterning the BLM adhesion and wettable metal layers like Ti, Ti-W, Cr, Mo, Ni and Cu. Most of the etchants studied were found to react with the solder bump metals. This yields not only to losing part of the bump metals but the etching residues on the bump surface render the bump reflow. Effect of the different etchants on the bump reflow is presented. A selective etching procedure was found for the Mo/Cu BLM structure. An alkaline etchant is used for the Cu layer and a phosphoric acid etchant for the Mo layer.

As CAPPING OF MBE-GROWN COMPOUND SEMICONDUCTORS; NOVEL OPPORTUNITIES IN INTERFACE SCIENCE AND DEVICE FABRICATION

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Condensation of an amorphous arsenic cap in the molecular beam epitaxy (MBE) growth chamber has been found to offer effective protection of reactive compound semiconductor surfaces against ambient contamination.[1] The technique has had a profound impact on III-V surface and interface research, in providing easy experimental access to high-quality epilayer surfaces.[2] Moreover, this As passivation has been shown to efficiently suppress carrier depletion at air-exposed and MBE growth-interrupted interfaces.[3]

Most work reported so far relates to As-capped $Al_xGa_{1-x}As$. Detailed investigation with surface sensitive structural (RHEED, LEED) and chemical (XPS) probes, confirms that the As cap is conveniently desorbed by annealing in UHV environments at a temperature in excess of some 350°C. Clean, ordered epilayer surfaces with different atomic reconstructions and corresponding (Al)Ga:As compositions may now be routinely prepared in this manner.[4] Reconstruction-dependent reactivity and electronic barrier formation at metal/GaAs(001) interfaces are reported.

Exploiting the protection offered by an arsenic cap in microelectronic and photonic device fabrication, e.g., for making contacts to buried epilayers or in selective MBE regrowth of 3D (quantum) structures, demands a suitable technique for pattern definition in the condensed As layer. The cap is found to be chemically stable upon exposure to standard lithographic processing chemicals, such as photoresist, developer, and acetone (the photoresist solvent). However, the temperature required for thermal desorption of As leads to excessive polymerization of photoresist, which renders subsequent dissolution of the photomask virtually impossible. A novel technique for (reactive) decapping at room temperature in a beam of hydrogen radicals (H^*) is demonstrated. This innovation makes recovery of As-capped $Al_xGa_{1-x}As(001)$ epilayer surfaces compatible with standard photolithography. Pattern definition with $\sim 5\ \mu m$ linewidth is demonstrated. XPS and SEM data for the H^*-etched specimens show clear evidence of superficial Ga-oxide and of As residues along the photomask edges. This technique thus needs further refinement, in order to be practicable in fabrication of III-V device structures.

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Process optimisation and characterisation of PBT structures

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ABSTRACT

The fabrication of silicon etched-groove Permeable Base Transistor (PBT) test devices have been studied.

We developed an optimised process for the fabrication of a PBT, using self aligned cobalt disilicide. The process is compatible with CMOS technology and is based on self aligned silicide technology.

We used the etched geometry to form the Base/Emitter grid. The self aligned oxide spacers achieve the sidewall passivation. After the cobalt deposition, a RTA step forms the cobalt disilicide on top (Emitter) and on bottom (Base) of the grid.

The highly doped, backside area of the wafer was used as Collector contact .

The $CoSi_2$ has been chosen because it has low resistivity and thus, reduces the Base resistance. Its barrier height to n-type Si ensures good rectifying behaviour of the Schottky Base diode. Another important property of the cobalt disilicide is its excellent chemical stability.

Several test PBT devices with different process parameters have been fabricated and characterised. Such parameters are the doping levels of the Base and Emitter, the grid depth, line width/spacing and the grid length, as well. Different metal (Co) deposition methods and different metal thicknesses have been used.

The characterisation of the PBT test devices includes analytical techniques, e.g. X-Ray Diffraction (XRD), Rutherford Backscattering Spectrometry (RBS), Secondary Ion Mass Spectrometry (SIMS), and electrical measurements. We measured and compared the transistors I-V characteristics, the results from the Schottky Base diodes I-V and C-V measurements (barrier height, ideality factor). The resistivity of the different silicide layers has also been measured.

The presented optimised process can be used for the fabrication of a PBT for high frequency performance and also can be included in an already developed, VLSI/ULSI fabrication process.

A Flip Chip Process Based on Electroplated Solder Bumps

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Compared to wire bonding and TAB, flip chip technology using solder joints offers the highest pin count and packaging density and superior electrical performance. The chips are mounted upside down on the substrate, which can be made of silicon, ceramic, glass or - in some cases - even PCB. The extra processing steps required for chips are the deposition of a suitable thin film metal layer(s) on the standard Al pad and the formation of bumps. Also, the development of new fine line substrate technologies is required to utilize the full potential of the technology. In our bumping process, bump deposition is done using electroplating, which was chosen for its simplicity and economy.

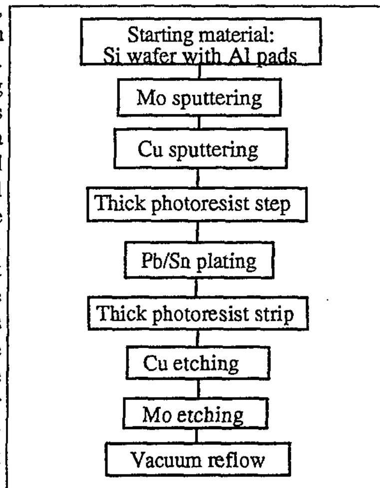

Fig. 1. Flip chip process flow.

A layer of a solderable metal is required under the bumps. A blank layer of metal is also needed for the cathode electrode in the electroplating step. 500 *nm* of sputter-deposited Cu is used for these purposes. 150 *nm* of sputter deposited Mo is used as a buffer layer between the Al bonding pads on the chip and the solder joints. A reason for this choice is that the metals can be selectively etched after bumping using the bumps as a mask, thus circumventing the need for a separate mask for etching the thin film metals. The bumps are electroplated from a binary 90%-10% Pb-Sn bath using a 20 μm thick liquid photoresist. A piece of platinized titanium mesh is used as a passive anode. The bump diameter/ pitch is 100 μm/250 μm for our standard process. The bumps as grown have a mushroom shape; after thick photoresist strip and under bump metal etching they become spherical in a vacuum reflow step in an Ar-H_2 ambient. The pitch is defined by the resist thickness and bump volume.

A somewhat similar process without the bumping step is used for the substrates. The Al pads on the substrate are covered with electroless Ni/Au to prevent the oxidization of the pads in the bonding step. Alignment is done on an extensively modified Laurier Model TL-271 flip chip bonder. Heat assisted tack bonding is used to attach the chips to the substrate, and final reflow joining is done without flux in a vacuum furnace.

Low temperature insulators deposited by Remote Plasma Enhanced CVD

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Remote Plasma Enhanced CVD (RPECVD) is a low-temperature CVD process where some of the gases are excited remotely from the substrate and mixed with un-excited gases to form precursors which deposit a film on a heated substrate. The remote nature of the plasma minimizes the etching effect on the substrate surface and gives enhanced control of reactions taking place in the plasma region.

A system for RPECVD has been manufactured by DCA Instruments Oy, Turku, Finland and is presently being tuned at the department to make high-quality SiO_2 on Si at low temperatures. The system consists of a UHV-deposition chamber with a separately pumped load-lock for convenient loading of 3"-Si-wafers as well as small pieces. After loading, the deposition chamber is pumped to UHV-conditions resulting in a clean environment. The base pressure in the deposition chamber is below 10^{-10} mbar after pumping and bakeout at 200 °C for 24 hours. Deposition is carried out at a pressure between 0.1 - 0.5 mbar. The plasma is inductively excited at 13.56 MHz and 10 - 600 W. Process gases used are high purity SiH_4 (2% in He), O_2, H_2, N_2, He, NH_3 and N_2O. Silane is injected through a gas ring positioned downstream between the sample holder and the plasma and the other gases can either be fed through a similar second gas ring or the plasma tube. Installed equipment for in-situ analyses are a Reflection High Energy Elctron Diffraction (RHEED) unit which enables us to analyze the structure of the substrate surface and a Residual Gas Analyzer (RGA) to analyze chemical reactions and residual gases in UHV before and after deposition as well as after baking.

The system can be used to deposit several types of thin films e.g. mixtures of SiO_2 and Si_3N_4 - oxy-nitrides with potentially superior breakdown characteristics, stacked dielectrics (e.g. O-N-O) with precise interfaces, ultra-thin high-quality tunnelling dielectrics for use in non-volatile memories (e.g. EEPROM), plasma assisted nitridation of thermal oxides etc.

We will present the current state of our activities at the conference and in the proceedings.

LOW TEMPERATURE SILICON EPITAXY BY RTCVD WITH MICROWAVE HEATING

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A new concept of rapid thermal processing (RTP) is presented. Single Si wafers are heated volumetrically by microwaves, which is different from the prevailing RTP systems where wafer heating is realized by surface absorption of heat radiated from tungsten-halogen lamps. Designed as a resonant cavity working at a frequency of 2.45 GHz, the process chamber is capable of processing 100 mm wafers with uniform temperature profile. Mathematical modelling shows that the T^4-dependence of thermal radiation is a key factor contributing to the improvement of the temperature uniformity. The temperature-dependent nature of skin depth (a parameter that determines how deep the microwaves can penetrate into the substrate) of the Si material constitutes a self-regulating factor that prevents the warmer to be further heated up and allows the colder to absorb more microwave energies. Thermal conduction within the wafer also benefits uniform temperature profile across a wafer. Convective heat transfer from the wafer to the environment of lower temperature deteriorates the uniformity.

The new type system can be used for basic RTP applications, including annealing, dopant drive-in and activation, metal silicide formation, oxidation and nitridation. It can also be used for chemical vapour deposition (RTCVD) at reduced pressures. Equipped with a molecular-turbo pump backed by a booster/rotary pump package, the base pressure of the process chamber is better than 10^{-7} torr. Gaseous precursors for RTCVD are introduced into the process chamber via respective mass-flow controllers. RTCVD of Si films from SiH_4 has been performed. During Si deposition, the pressure is typically around 0.01 - 0.2 torr. Silicon epitaxial layers are deposited at 700 °C, both on blank and patterned Si wafers. *In-situ* surface cleaning is carried out by purging the wafer in H_2 atmosphere at low pressure and intermediate temperature. The quality of the epi-layers is studied by means of Rutherford backscattering spectrometry (RBS) at channelling mode, X-ray diffraction (XRD), and cross-sectional scanning electron microscopy (SEM).

MOLECULAR BEAM EPITAXIAL GROWTH OF HIGH QUALITY III-V MATERIAL FOR ELECTRONIC AND OPTICAL APPLICATIONS

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High quality material is grown by molecular beam epitaxy by a proper choice of growth parameters. Important parameters are V/III flux ratio, substrate temperature, growth speed, and duration of growth interrupt. With our Riber 32 system machine a number of different structures have been grown. Pseudomorphic $In_{0.15}Ga_{0.85}As$/GaAs high electron mobility transistors with submicron gate lengths show excellent DC and RF characteristics. The unity current gain frequency f_T is 110 GHz and the transconductance 610 mS/mm, for a 120 nm gate length device. The electron mobility in the 2-dimensional electron gas at room temperature is 6600 cm^2/Vs with a sheet carrier concentration of 1.4×10^{12} cm^{-2}. Furthermore, quantum well structures have been grown to study optical intersubband transitions in the conduction band. A pair of strongly coupled, *i.e.*, closely spaced, quantum wells is compared to a quantum well with a width equal to the whole double-well structure. The former structure shows a significantly larger peak absorption. In contrast to what one would expect when two additional heterointerfaces are introduced, a narrower linewidth is also observed. The heterointerfaces need to be smooth to obtain the narrower linewidth. The results for the transistor and the quantum well structures show that the material grown is of high quality.

The Au/Si(111) system studied by optical second-harmonic generation.

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Optical second-harmonic generation (SHG) is a relatively new technique for surface investigations. The surface sensitivity is a result of an electric dipole response existing at the surface but not in the centrosymmetric bulk. In the present context, the interesting aspects of SHG are, that the growth process can be followed continuously during the evaporation and, that the technique will be sensitive to the properties of the Au/Si interface as long as it is accessible to light. For proper choice of the pump wavelength and light polarization directions, SHG is very sensitive to the order of the system.

The room temperature growth of Au on Si(111) 7x7 has been followed continuously with SHG, and at selected coverages with LEED and AES, during the evaporation of the first 10 monolayers. The clean surface shows a large SH signal due to a resonant transition between localized surface states. During the evaporation of the first monolayer the SH signal decays to zero as the 7x7 reconstruction is destroyed. In the range from 1 to 5 monolayers the SH signal goes through a local maximum and a local minimum which is ascribed to variations in the island formation on the surface. At a coverage of 6 monolayers the Au has formed a closed layer and the SH signal has increased to a saturation level of 20% of the initial 7x7 surface signal.This signal shows a perfect 3-fold symmetry though there is no observable LEED pattern. It is therefore a sign of an ordered structure on the Au/Si interface. The Si $L_{2,3}VV$ Auger peak decrease during the evaporation and starts to show a splitting at a coverage of 3 monolayers. At 6 monolayers it has evolved into two clearly separated peaks indicating that reacted Si is present on top of the Au layer.

Annealing of the sample leads to increased order and thus increased SHG. The ordering into a $\sqrt{3}x\sqrt{3}$ structure starts at low temperatures but the main increase in SHG takes place from 450 to 550 °C. After annealing to 1000 °C the SH signal has increased to a level considerably higher than that of the 7x7 surface.

Wednesday afternoon

Photonics

Ultrafast Nonlinear Optics in GaAs/AlGaAs Quantum Wells

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In low-dimensional semiconductor nanostructures as produced by modern crystal growth techniques, e.g. molecular beam epitaxy (MBE), the excitonic features of the linear and the nonlinear optical properties are strongly enhanced, even at room temperature. The study of exciton dynamics is of importance for applications in future ultrafast optical and opto-electronic devices, such as lasers, optical modulators and switches. Similarly, linear and nonlinear optical spectroscopy with ultrafast time resolution of excitonic transitions provide an important tool for the study of the fundamental properties and the quality of these low-dimensional quantum structures. Such studies have been made possible by the development of ultrafast laser systems, and they have recently been undertaken by a number of research groups around the world.

We have performed coherent degenerate four-wave mixing (DFWM) experiments in a two-beam geometry on GaAs/AlGaAs multiple quantum wells, investigating the initial coherence and dephasing of quasi two-dimensional excitons after resonant excitation by ultrafast laser pulses. The dependence of the dephasing rate on exciton density, lattice temperature (phonon scattering), well width and interface roughness will be discussed. Well width fluctuations lead to inhomogeneous broadening and/or splitting of the exciton lines depending on the interface island configuration. The formation of biexcitons in GaAs MQW's is being observed, and in the coherent DFWM experiments a number of quantum beats and polarization interferences between different exciton transitions appear. By spectrally resolving the DFWM signal, we can estimate the degree of inhomogeneous broadening and determine the nature of the observed interferences and beats.

We have also performed DFWM, or transient grating, experiments in a three-beam geometry, revealing recombination lifetimes and diffusion coefficients of the excitons. From the diffusion coefficients, the momentum relaxation rates of the excitons are being determined and compared with dephasing, or polarization relaxation rates.

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Ellipsometric Characterization of Semiconductor Heterostructures

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Abstract

The potential of spectroscopic ellipsometry for characterization of III-V semiconductor quantum heterostructures is demonstrated by several ellipsometric techniques, chosen to match polarization selection rules and spectral region of interest.

Brewster-angle geometry and transmission arrangement has been used for non-destructive studies of electronic intersubband transitions in the MIR. The inversion problem is solved to determine the extraordinary dielectric response in the wells. Enhacement of sensitivity in the case of reflection ellipsometry is achieved by the use of a metal overlayer on the quantum-well or supperlattice region.

Photo-modulated spectroscopic ellipsometry utilizing a tunable laser source has been used for studies of near band-gap transitions in the NIR/VIS. This provides information that is not supplied by conventional techniques like PLE.

All-Optical Bistability in Luminescence of Thin CdS Films

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All-optical (all-OB) bistabilities represent the future philosophy of optical cavity-free and wireless device concepts for optical data treatments. Laser induced optical devices (LIODs) exhibit in a convenient practicable way photo-thermal all-OBs which underlie the principle of increasing absorption by photo-irradiation. The LIOD investigated was realized with a thin (≤10μm) CdS film driven with the 514.5nm Ar^+-laser line. Recently, an interesting observation which was not theoretically predicted was performed: Surpassing the well known all-OBs in transmission and reflection a LIOD exhibits all-OB in luminescence.[1,2] For the first time, we present a comparison of the switching times (≤200μs) of bistabilities in transmission and luminescence. We have pointed out that the bistable switch in luminescence takes place about three times faster than in transmission. Hence, bistabilities in luminescence are not only driven by photo-thermal effects but also by electronic ones. In particular, bistabilities in luminescence represent a new class of nonlinearities of semiconductors, a *photo-thermally induced electronic bistability*. In fact, we present a theory for bistabilities in luminescence taking into account both thermal and electronic processes of highly excited semiconductors. Finally, on the basis of the presented data new all-optical measuring methods as the determination of the free carrier type of semiconductors, all-optical current measurements and all-optical temperature measurements are discussed.

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New Experimental Techniques

Strain characterization of $Ge_{1-x}Si_x$ / Ge layered structures by using two-dimensional reciprocal lattice mapping

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Abstract

Two-dimensional reciprocal lattice mapping by high-resolution X-ray diffraction (HRXRD) has been used to characterize the strain in $Ge_{1-x}Si_x$(001)/Ge structures grown by molecular beam epitaxy (MBE). Two-dimensional (2D)-diffraction maps were obtained by using a high-resolution, multi-reflection X-ray diffractometer equipped with a 4-crystal monochrometer and a 2-crystal analyzer using Cu $K_{\alpha 1}$ X-ray radiation . With this configuration the diffraction intensity can be measured with a high resolution as a function of both the incident angle, ω and scattering angle, 2θ. Scanning the angle ω with fixed 2θ (ω scan) probes different orientations of planes with a given plane separation, while a simultaneous scan of ω and 2θ with a ratio of 1:2 (ω/2θ scan) probes different planar spacings in a given direction. A two-dimensional reciprocal space map can be obtained by performing several ω/2θ scans for a range of incident angles. In this way, the relative difference in lattice parameter for a layer and a substrate (Δa /a) can be obtained both in the parallel ($\Delta a_{//}$) and perpendicular ($\Delta a_{\perp}$) directions from measurements of an off-normal reflection.

Tetragonal lattice distortion along (see Fig.1) and perpendicular to the growth direction have been determined over a range of Si-fractions up to 45%. The thickness of the samples has been shown in Fig.2. In this way metastable critical thickness for different Si concentrations can be measured.

Fig.1

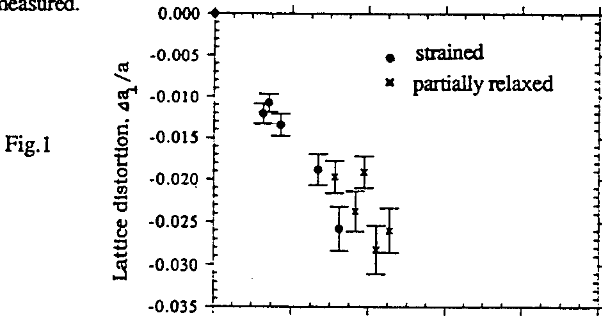
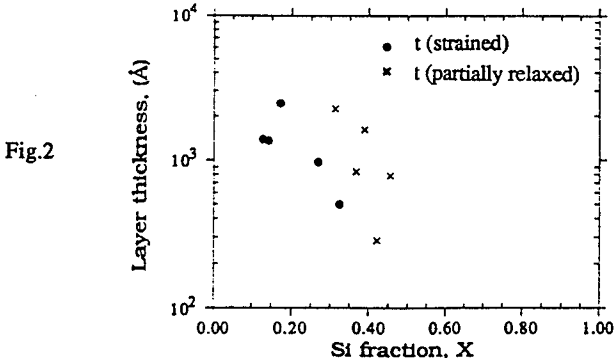


Fig.2



Recent Advances in Theory

A Novel Two-Dimensional Hydrodynamic Transport Model

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ABSTRACT

A novel two-dimensional hydrodynamic model for heterostructure semiconductors has been derived under the assumption of nonparabolic energy bands. The governing equations have been obtained from the first three moments of the Boltzmann transport equation. No specified carrier energy distribution function is needed and the model accounts for degeneracy. The relaxation time model has been applied to the Boltzmann collision integral and the isothermal approximation is assumed for the lattice. Transport equations of lower level of sophistication are easily obtained from this hydrodynamic model. The transport equations coupled to Poisson's equation have been discretized by using a generalization of the finite difference scheme, the box integration method. To achieve good accuracy and stability, the current density and the energy flux density are discretized by a scheme resembling the Scharfetter-Gummel approach.

With the assumption of nonparabolic energy bands, the energy dispersion is often expressed by the first-order approximation, $\hbar^2k^2/2m = \varepsilon(1+\alpha\varepsilon)$, where $m = m(r)$ is the conduction (valence) band effective mass and $\alpha = \alpha(r)$ is the conduction (valence) band nonparabolicity factors, respectively. Unfortunately, this expression will not give easily solvable equations. Therefore, we use a further approximation, $\hbar^2k^2/2m = x\varepsilon^y$, where $x = x(r)$ and $y = y(r)$ are position-dependent fitting parameters to be determined for each band edge.

Three equations for conservation of charge, momentum and energy for electrons are obtained:

$$\frac{\partial n}{\partial t} - \frac{1}{q}(\nabla \cdot J_n) = -R_n$$

$$J_n = \mu_n n \nabla E_c - \mu_n \frac{1}{y_n} n w_n \nabla (ln(m_n)) + \frac{2}{3y_n}\mu_n w_n \nabla n + \frac{2}{3y_n}\mu_n n \nabla w_n$$

$$\frac{\partial (n w_n)}{\partial t} + \nabla \cdot S_n - \frac{J_n}{q} \cdot \nabla E_c = -\frac{n}{\tau_w}(w - w_0)$$

The expression for the energy flux density S_n is taken from Ref.1. Similar equations can be written for holes.

This device simulation model has been implemented in the two-dimensional numerical simulation program SCORPIO [2].

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DIFFERENT METHODS OF TREATING THE DEPLETION REGION IN MONTE CARLO SIMULATIONS OF A SCHOTTKY DIODE

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ABSTRACT

Monte Carlo (MC) simulations is a well established tool for studying semiconductor devices, and hot electron phenomena. It has also been shown [1] that the model becomes more powerful when a full band structure is used. Even though the method is very appealing, since a lot of physics can be included without the drastic approximations used in other models, there are also problems. MC is very time consuming, especially when Poisson's equation is coupled self-consistently with Boltzmann's equation and a full band structure. This puts a limit to the number of particles that can be simulated. One introduces the concept of "superparticles", each one consisting of many electrons so that typically about 10^4 superparticles are simulated. In each scattering event the particles are treated as electrons but in the solution of Poisson's equation the superparticles are used. Since MC is basically a statistical method the results depend heavily on the reliability of the statistical data.
Accurate results are more difficult to obtain in "rare" regions like a depletion region where the number of particles is relatively low. The accuracy of the solution of Poisson's equation is also affected by the occurrence of "rare" regions.
We have implemented the full band Monte Carlo program published in [1] with several modifications in order to be able to solve Poisson's equation as well. A one-dimensional Si Schottky diode has been simulated with the purpose of studying how different charge assignment schemes affect the field distribution. Both schemes used frequently [2] and other schemes, obtained from theory of digital signal processing, have been used.
We have also studied the effect of "splitting" the superparticles in different ways in order to get better statistics. The results shows that the best way of assigning charge to mesh points depends on the particular application and the extension of the depletion region, it might be worthwhile to use a more complicated assignment function in the depletion region than those generally used. Possibly some kind of adaptive method with different functions in different regions is the optimal choice. Splitting of the particles in the statistically sensitive region improves the results but the improvement depends quite strongly on how the splitting is implemented.

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A CLUSTER APPROACH FOR MODELLING OF SURFACE CHARACTERISTICS OF STANNIC OXIDE

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Stannic oxide, SnO_2, in its pure form is an n-type, wide band gap semiconductor. Its electrical conduction results from point defects which are native (oxygen vacancies) or foreign atoms that act as donors or acceptors. Some unique electrical and optical properties of SnO_2 make it useful for many applications, like for gas reduction and detection. Local energy levels, originating from defects like oxygen vacancies at or near SnO_2 surface, may have an important role in both the electrical transport and gas response properties of SnO_2.

Calculations with a cluster of up to fifty or more atoms may simulate the characteristics of a large crystal surface, also reflecting the energy levels of the surface with band formation. The cluster can also include foreign atoms at the solid surface or surface defects like oxygen vacancies in oxidic semiconductors. The model gives a detailed picture of the energy and shape of the individual orbitals of the surface atoms and their modification by the presence of many other atoms including foreign adsorbates.

Some results are given from a cluster approach for the electronic structure of the SnO_2 (110) - 1 x 1 surface together with some oxygen vacancies, foreign impurities and adsorbates. Computations are based on the local density approximation and atomic orbitals as a basis set. Solutions were calculated self-consistently, but also using a composition of atomic potentials for some smaller clusters. The atomic-orbital nature (origin) of the cluster levels was traced by projection onto the atomic basis set. The results here refer to two clusters with 39 and 97 atoms, respectively. For instance, the larger cluster with 97 atoms had 35 atoms (19 Sn and 16 O) for modelling the (110) face and 62 atoms for the next few bulk layers. The computations consider the energy levels related to oxygen vacancies, foreign impurities and some adsorbates. On particular, the focus was on the levels related to oxygen vacancies and originating from Sn5s orbitals, which are well-known donor levels in the deep bulk, making SnO_2 an n-type semiconductor. The results support some other theoretical and experimental predictions that oxygen vacancies behave as neutral defects at or near SnO_2 surfaces. Chromium is considered here as an example of foreign impurity atoms. Many energy levels originating from 3d orbitals of Cr 'bulk' impurities appear around the middle point of the SnO_2 'band gap'. The levels originating from 3d orbitals of a Cr surface impurity are near the bottom of the 'band gap'. The results may explain the strong effects originating from chromium impurities both on electrical conductivity and on some catalytic properties of SnO_2.

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