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COMPUTER-AIDED PROTOTYPING OF ADVANCED MICROSYSTEMS TECHNOLOGY

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FINAL TECHNICAL REPORT

Principal Investigator: Dimitri A. Antoniadis Massachusetts Institute of Technology

PROGRAM TITLE: Computer-Aided Prototyping of Advanced Microsystems Technology -

CONTENT:
A. Advanced Modeling and Computational Prototyping
A.1 Numerical Methods for Interconnect Electrical Performance Analysis
A.2 Modeling of Interconnect Reliability A.3 Modeling of Advanced Device Structures
B. Methodologies for Design with Flexible Design Rules
B.1 Circuit-Level Reliability
B.2 Technology Variation Assessment
B.3 Design Integration using Flexible Design Rules
C. National Infrastructure for Networked Design and Prototyping
D. Exploration of Emerging Technologies

TASK TITLE: A. Advanced Modeling and Computational Prototyping

A.1 Numerical Methods for Interconnect Electrical Performance Analysis

PROJECT LEADER(S): J. White

Developed Coordinate-Transformed Arnoldi Algorithm for automatically generating arbitrarily accurate, guaranteed stable circuit models from 3-D interconnect simulation.

Developed a new 3-D transient interconnect (RC) simulation approach that remains well-conditioned even for long lines.

Developed a perturbation approach that allows arbitrary permitivity ratios and and arbitrary dielectric geometries.

Developed a generalized precorrected-FFT Method with new grid projection scheme up to ten times faster than our earlier simulator FASTCAP.

Released FastFFT - A precorrected-FFT based 3-D Capacitance extraction program which uses modified Green's functions for ground planes and is up to an order of magnitude faster and more memory efficient than FASTCAP.

Publications

L. Miguel Silveira, Mattan Kamon, Ibrahim Elfadel, and J. White "A Coordinate-Transformed Arnoldi Algorithm for Generating Guaranteed Stable Reduced-Order Models of RLC Circuits," To Appear, Proceedings of the International Conference on Computer Aided Design, San Jose, CA, November 1996.

L. M. Silveira, I. Elfadel, M. Kamon, and J. White, "Coupled Circuit-Interconnect Analysis Using Stable Arnoldi-Based Model-Order Reduction," Proceedings of Progress in Electromagnetics Research Symposium, Cambridge, MA, July, 1997

J. Tausch and J. White, "Multipole Accelerated Capacitance Calculation for Structures with Multiple Dielectrics with High Permitivity Ratios." Proceedings of the 33nd Design Automation Conference, Las Vegas, June, 1996.

M. Chou and J.K. White, "Efficient Formulation and Model-Order Reduction for the Transient Simulation of Three-dimensional VLSI Interconnect", IEEE Trans. on Computer-Aided Design, December 1997, Vol. 16, no. 12, pp. 1454-1476.

J. R. Phillips and J. K. White, "A Precorrected-FFT method for Electrostatic Analysis of Complicated 3-D Structures," IEEE Trans. on Computer-Aided Design, October 1997, Vol. 16, No. 10, pp. 1059-1072.

A.2 Modeling of Interconnect Reliability

PROJECT LEADER(S): C. V. Thompson, D. E. Troxel

Our goal in this program was to develop process and layout-specific models and simulations for interconnect reliability and to use theses tools in developing a tool for making process-sensitive and layout-specific circuit-level interconnect reliability simulations. This tool will provide a means of making much more accurate reliability assessments, will allow process and layout design for optimized interconnect reliability, will allow rapid evaluation of the impact of changes in materials and processes on interconnect reliability, and will provide the bases for quantitatively assessing the trade-off between performance and reliability during design and fabrication of high performance integrated circuits.
Our major accomplishments have been:

* Development of MIT/EmSim: a tool for simulation of electromigration and electromigration-induced failure of interconnects,

* Adaptation of GGSim for modeling grain structure evolution in interconnects,

* Development of hierarchical interconnect reliability assessment methodologies based on analyses of the reliability of individual interconnect trees, and

* Design of ERNI, a tool for process-sensitive and layout-specific circuit-level reliability assessments.

These developments will be briefly discussed.

MIT/EmSim

We have developed a method for simulation of stress evolution along the length of an interconnect line as caused by electromigration and stress migration, as a function of time, temperature and current density. The method is based on the model of Korhonen et al [1] as discussed by Clement and Thompson [2] and as adapted for analytic solution by Knowlton et al [3-6]. The method tracks the atomic flu into and out of incremental volumes along the length of a line, and accounts for the effects of stress gradients, gradients in chemical potentials (in alloys), and the electron wind force [7-9]. The effects of grain structure are accounted for by appropriately varying the diffusivity along the length of the lines and the effects of filled studs versus contact pads are treated through variations in boundary conditions. Failure times can be defined as the time required to reach the critical tensile stress for void nucleation, the time required to reach a critical void size (to a corresponding maximally acceptable line resistance increase), or the time required to reach the critical compressive stress leading to mechanical failure of the dielectric. EmSim/MIT is discussed in more detail in recent publications and at http;//nirvana.edu.mit/emsim. A Web-base version of MIT/EmSim can be found and used (with a password) at the same Web site. MIT/EmSim has been used, and the web site visited, by a large number of people from companies, universities, and government sites.

Interconnect are made from polycrystalline films and their reliability depends strongly on the grain size of the films relative to the interconnect dimensions, especially the line width, as well as on how the grain structure evolves during post-patterning processing. When line widths and the sizes of the grains are comparable, as they usually are, lines are broken into polycrystalline segments characterized by high diffusivity and segments in which grains span the width of the lines so that diffusivities along the line length are much lower. Statistical variations in the lengths and spacings of these segments lead to statistical variations in the time to electromigration-induced failure, and therefore control the reliability of interconnects. As will be discussed shortly, we have adapted our grain growth simulator to simulate the development and evolution of grain structures in interconnects. The grain growth simulator (GGSim) can be linked directly to MIT/EmSim for electromigration simulations. Alternatively, analytic models for grain structure statistics as a function of line geometry and thermal history can be embedded in MIT/EmSim. The web-based version of MIT/EmSim, has embedded functions for predicting grain structure variations, and can therefore be used to predict variations in electromigration-limited lifetimes allowing the use of MIT/EmSim for *reliability* predictions [5].]

In summary, MIT/EmSim allows prediction of the reliability of interconnects as a function of

* Their widths, thickness and length,
* The dimensions and resistivities of the high conductivity metal (Al-based or Cu-based) and any overlayers, underlayers or liners,
* The boundary conditions (e.g., stud-to-stud vs. stud-to-pad vs. pad-to-pad),
* The amount and species of alloy additions,
* Processing-induced variations in grain structures, and
* The current density and temperature.

The latter allows testing of conventional methods for scaling results from accelerated test conditions to service conditions. We have found that conventional scaling methodologies can lead to highly inaccurate reliability projections which are neither necessarily pessimistic nor optimistic [6,8,10].

MIT/EmSim has also been modified to allow simulation of electromigration in interconnect trees with junctions and wide-to narrow transitions, and is being used to generate reliability models for trees for use in ERNI, as will discussed later.

GGSim

Through the CAPAM program we modified an existing grain growth simulation for modeling of grain structure evolution during processing of interconnects. This simulation is based on a 2-dimensional front-tracking model for capillarity-driven grain boundary and triple junction motion [11]. It has been modified to account for 3-dimensional effects known to be important in thin films, including the effects of grain boundary surface grooves [12], the effects of anisotropic free surface and film-substrate interface energies [13], the effects of strain energy anisotropies [14], solute drag [15], precipitate pinning [16], and variable grain boundary energies and mobilities [17]. Results from simulation of grain growth in continuous thin films have been extensively tested by comparison with experiments [18].

For the CAPAM program we created an extensively modified version of this tool, called GGSim, which can be used to simulate post-patterning grain structure evolution in interconnects of arbitrary rectilinear shapes [19]. Post-patterning grain structure evolution occurs during dielectric deposition and other high temperature steps, and results in evolution toward 'bamboo' grain structures which lead to greatly improved reliability, but also complex reliability scaling behavior [3,6]. Using GGSim we have analyzed grain structure statistics as a function of the initial grain size and the line geometry [19-20], as well as evolution of the statistical characteristics of grain structures during post-patterning annealing [19,21]. Analytic models have been extracted from these analyses and have been embedded in MIT/EmSim to provide compact models for generating the variable grain structures which lead to lifetime variations, allowing predictions of interconnect reliability.

Simulations of post-patterning grain-structure evolution have been compared with experiments involving in situ annealing of Al-based and Cu interconnects in a transmission electron microscope, and the accuracy of the simulation has been improved by accounting for the effects of grain boundary drag at line edges and the effects of evolving thickness non-uniformities [22]. We have also developed an experimental technique involving observations of froth evolution in 3D shapes, in order to characterize 3D effects that occur in lines with near-unit aspect ratios. We are collaborating with Los Alamos National Laboratories in use of their new fully 3-D front-tracking grain growth simulation in making comparisons between observations of froths and simulations. The methodology developed for analysis of 2D simulations will be employed in analyzing 3D experiments and simulations to develop improved compact analytic models for inclusion in MIT/EmSim.

Hierarchical Reliability Analyses Based on Analysis of Interconnect Trees

Experimental characterization as well as modeling and simulations of interconnect reliability generally treat straight interconnects without junctions. Actual layouts contain interconnect units with more complex shapes; with bends, junctions and wide-to-narrow transitions. In developing layout-specific circuit-level reliability assessment tools we have recognized that the fundamental unit of an interconnect system, from the reliability point of view, is not a straight segment connected only to other segments at its end, but is instead an interconnect 'tree' [23]. An interconnect tree is defined as any continuously connected collection of interconnect segments, none of which are connected through a diffusion barrier such as a W-filled via. Trees typically lie within one layer of metallization and have multiple terminations (2 or more) at diffusion barriers at vias or contacts.

We have developed algorithms and simulations which can be used to analyze the reliability of trees, based on information obtained from testes on straight stud-to-stud lines without junctions or reservoirs (to be referred to as I's). We have shown that for the purpose of determining if a tree is immune to electromigration-induced voiding, the experimentally determined the current-density line-length product, jL, that defines the 'Blech' length below which I's are immune to voiding can be used to predict the conditions for immortality of a tree. This is done by comparing the experimentally determined jL product for I's with an effective jL product for a tree [23-25]. The effective jL product is the maximum of the sums of the jL products of the segments over all possible paths through a tree. Once trees are identified, a worst-case effective jL product can be easily and compactly calculated by assuming all segments are at the maximum allowable current density. Even under these worst case conditions, many trees will be tagged as immune to failure at service conditions and can be removed from subsequent analyses. In the past year, an algorithm has also been developed for testing with respect to void-growth or resistance saturation [24-25]. This algorithm, when conservatively and simply applied, will lead to the removal of a still larger number of trees from further considerations.

By testing for immortality assuming that all segments in a tree are at the current density limit, many trees will be filtered from more complex calculations. Remaining trees can be treated with increasingly complex models for circuit operation, to more accurately estimate effective jL products. Conservative and compact reliability models can then be applied to the remaining trees, and trees with poor reliability can be tagged for layout changes, or for more detailed simulations based on the direct use of GGSim and MIT/EmSim. This hierarchical approach to circuit-level reliability analyses is the basis for development of ERNI, which is discussed in the next section.

In order to analyze the reliability of trees that are not immortal, we have modified MIT/EmSim to allow simulation of electromigration and electromigration-induced failure of trees with junctions, bends and wide-to-narrow transitions. This will allow the use of MIT/EmSim to develop compact reliability models for mortal trees, for use in ERNI. The basic assumptions implicit in this modified tool are being tested in SRC-funded electromigration experiments on lines with junctions, reservoirs and wide-to-narrow transitions.

ERNI

We have completed the design of ERNI (Electromigration Reliability for Network Interconnect), a microstructure-based VLSI metal interconnect electromigration reliability assessment tool. In this design the input design is represented by MAGIC files. These are parsed to extract interconnect trees. This list of trees is then filtered to remove those trees which can be proved to never fail. The design rules to identify these trees are based on calculations of steady-state mechanical stresses with worst case current densities. Circuit simulations are then used to calculate the actual currents in the remaining trees. At this point the trees are matched to models and the models are used to calculate their reliability. EMSIM and CGSIM can be used to produce better models as required. The overall reliability and the worst offenders are then displayed for the designer who can take corrective action either by accepting the calculated reliability or modifying the design to be more reliable.

Significant portions of this tool have been implemented. MAJIC, which is a rewrite of MAGIC in JAVA, has been accomplished. Using the new MAJIC applications programmer interface (API) interconnection trees have been derived from standard magic files representing designs by a number of others. This list of trees is then pruned by removing the trees that never fail. At present, our model database is sparse. Interfaces to modeling software, CGSIM and EMSIM have been defined and tested.

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TASK TITLE: A.3 Modeling of Advanced Device Structures
PROJECT LEADER(S): M. B. McIlrath, D. A. Antoniadis

* Used transistor electrical (e.g., I/V) data obtained under a variety of carefully designed experimental test conditions to characterize dopant distributions in advanced devices.

* Developed a new inverse modeling-based technique for the extraction of 2D doping profiles in submicron MOS transistors using I-V characteristics in the subthreshold region. The main advantages of this technique include: (1) ability to extract 2D doping profiles of devices having very short channel lengths due to its immunity to parasitic capacitances and noise; (2) low sensitivity to gate area variations; (3) low dependence on mobility model; (4) non-destructive nature; and (5) simplicity of data collection and preparation, as well as general ease of use.

* Tested the inverse modeling technique with MOS devices with channel lengths down to 120 nm and 4.5 nm gate oxides. Extracted doping profiles show complex 2D shapes, including retrograde and halo doping sructures. Verified that the technique is reliable in providing unique solutions.

* Studied effects of oxide thickness, mobility, and mobility model on profiles extracted by inverse modeling technique.

* Using extracted 2D doping profiles, mobility models were calibrated using device I-V data in the linear and saturation regions. It was found that very accurate device characteristics can be simulated once appropriate mobility models have been calibrated.

* Implemented a semiconductor device parameter space exploration tool in java. This tool allows the user to specify electrical constraints and receive feasible sets of parameters as outputs. An optimization module allows for optimization of the feasible parameter set based on a prespecified penalty function. Four compact analytical models have been implemented for use with this tool: two bulk CMOS models (one region-based, one charge-sheet based), a silicon-on-insulator with active substrate(SOIAS) model, and a silicon-germanium model.

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TASK TITLE: B. Methodologies for Design with Flexible Design Rules

B.1 Circuit-Level Device Reliability

PROJECT LEADER(S): J. Chung

Throughout the duration of the program we collaborated with leading reliability CAD-tool vendor (BTA Technology) on developing and implementing new improved hot-

carrier lifetime-prediction models and parameter extraction techniques. This work was primarily contained in W. Jiang's and A. Kim's thesis work and publications listed below.

We also developed and transferred to industry (HP & LSI Logic) new lifetime-prediction models, hot-carrier reliability test structures, and measurement and data-analysis methodologies for establishing circuit-performance-based hot-carrier reliability criteria. This work was primarily contained in V. Chan's, W. Jiang's, and H. Le's thesis work and publications also listed below.

S.M./M.Eng. Student Thesis:

Abraham Kim, (January 1995) "Modeling for Hot-Electron Reliability Simulation"

Beniyam Menberu, (January 1996) "Analysis of Hot-Carrier AC Lifetime Model for MOSFET"

Huy Le, (March 1996) "Characterization of Hot-Carrier Reliability in Analog Sub-circuit Design"

Ph.D. Student Thesis:

Vei-Han Chan, (January 1995) "Hot-Carrier Reliability Evaluation for CMOS Devices and Circuits"

Wenjie Jiang, (May 1998) "Hot-Carrier Reliability Assessment in CMOS Digital Integrated Circuits"

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B.2 Technology Variation Assessment
PROJECT LEADER(S): D. Boning, J. Chung

A key goal of this work has been to develop methodologies to understand and characterize manufacturing variation (Task B.2) and to connect that understanding to flexible design rules and approaches (Task B.3). Substantial progress has been made in defining a new "statistical metrology" approach where the sources of systematic variation

in key fabrication processes can be characterized. Key variation assessment accomplishments have been (1) statistical decomposition methods to separate wafer-level and die-level variation elements; (2) focus on dielectric thickness variation in interconnect processes arising from CMP; and (3) examination of systematic within-die poly and metal critical dimension (CD) variation. The work on CMP in particular has had a dramatic impact in the field: this research has contributed standard CMP characterization mask sets that are widely used in the industry (and have been licensed for commercialization) to understand pattern dependencies in CMP. In the second part of this work, we have developed and applied new approaches to understand how within-die variation affects circuit performance. For example, for a 1Ghz IBM microprocessor case study, we found that clock skew can be seriously overestimated if worst-case approaches are used that do not account for the true underlying systematic variation. This work has also contributed to "dummy fill" approaches that minimize pattern density variation within each die with consideration of the tradeoffs between manufacturability and performance.

PUBLICATIONS (TASKS B.2 AND B.3)

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B.3 Design Integration Using Flexible Design Rules

PROJECT LEADER(S): D. Boning, C. V. Thompson

SIGNIFICANT RESULTS/FINDINGS:

* A new variation analysis and screening methodology has been explored, in collaboration with IBM Austin Research Labs. The approach uses a single RC extraction to which adjustments are made based on thin film or other geometric variation models, and then use of this information in timing analysis. The approach allows thousands of global nets to be analyzed for skew and delay issues, and was applied to a 1GHz microprocessor design. A paper for the 1998 IEDM conference has been accepted.

* We have developed a filtering procedure which allows identification of interconnect trees which will not fail due to resistance increases associated with electromigration. This analysis builds on our earlier filtering procedure for trees which are immune to void formation. Use of these filters will allow the elimination of a large fraction of the total interconnect in a circuit from further, more computationally intensive reliability analyses. This new filter is being implemented in ERNI. [J.J. Clement, S.P. Riege, R. Cvijetic, and C.V. Thompson, "Methodology for Electromigration Critical Design Rule Evaluation", submitted to IEEE Trans. on CAD of Integrated Circuits and Systems, April 1998.]

PUBLICATIONS (See list under Task B.2)

TASK TITLE: C. National Infrastructure for Networked Design and Prototyping

PROJECT LEADER(S): D. E. Troxel, D. Boning, M. B. McIlrath

We have developed a flexible, distributed system architecture capable of supporting collaborative design and fabrication of semiconductor devices and integrated circuits. Such capabilities are of particular importance in the development of new technologies, where both equipment and expertise are limited. Distributed fabrication enables direct, remote, physical experimentation in the development of leading edge technology, where the necessary manufacturing resources are new, expensive, and scarce. Computational resources, software, processing equipment, and people may all be widely distributed; their effective integration is essential in order to achieve the realization of new technologies for specific product requirements. Our architecture leverages current vendor and consortia developments to define software interfaces and infrastructure based on existing and emerging networking, CIM, and CAD standards. Process engineers and product designers access processing and simulation results through a common interface and collaborate across the distributed manufacturing environment.

We have developed an integrated, open system architecture enabling distributed experimentation and process control for plasma etching. The system employs in-situ CCD interferometry based analysis in the sensor-feedback control of an Applied Materials Precision 5000 Plasma Etcher (AME5000). Our system supports accelerated, advanced research involving feedback control algorithms, and includes a distributed interface that utilizes the internet to make these fabrication capabilities available to remote users.

The system architecture is both distributed and modular: specific implementation of any one task does not restrict the implementation of another. The low level architectural components include a host controller that communicates with the AME5000 equipment via SECS-II, and a host controller for the acquisition and analysis of the CCD sensor images. A Cell Controller (CC) manages communications between these equipment and sensor controllers. The CC is also responsible for process control decisions; algorithmic controllers may be integrated locally or via remote communications. Finally, a System Server manages connections from internet/intranet (web) based clients and uses a direct link with the CC to access the system. Each component communicates via a predefined set of TCP/IP socket based messages. This flexible architecture makes integration easier and more robust, and enables separate software components to run on the same or different computers independent of hardware or software platform.

We have developed a remote microscope. It is a telemicroscopy system that allows users to remotely control and view a microscope over the internet with a graphical interface that runs on an ordinary workstation computer. The microscope server consists of an automated Zeiss microscope that is controlled by a personal computer, while the client interface is implemented with an applet which is downloaded by a browser running on virtually any type of computer. The system was designed primarily to provide remote

inspection capabilities for semiconductor researchers during the remote fabrication of integrated circuits, but can also be used as a general purpose instrument for remote inspections. The remote microscope also allows any number of clients to simultaneously view the microscope in a conference inspection mode, enabling collaboration opportunities among distant viewers. Because clients require no special hardware, the internet remote microscope is extremely accessible and easy to use, yet provides powerful remote inspection capabilities, collaboration opportunities, and easy access to hard to reach locations such as clean room environments for semiconductor processing. This remote microscope has been installed in the Microsystems Technology Laboratory here at MIT and has been operated remotely by people at CNRI in Virginia.

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Michael B. McIlrath, Duane S. Boning, and Donald E. Troxel, "Architecture for distributed design and fabrication" SPIE Proc. 2913, Plug and Play Software for Agile Manufacturing, Intl. Symp. on Intelligent Systems and Advanced Manufacturing, Boston, MA, Nov 1996.

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James Kao, S.M., "Remote Microscope for Inspection of Integrated Circuits," September 1995.

Nadir E. Rahman, M. Eng., "Extraction of MOSFET Doping Profiles from Device Electrical Measurements," July 22, 1996.

Somsak Kittipiyakul, B.S., M. Eng., "Automated Remote Microscope for Inspection of Integrated Circuits," September 6, 1996

Manuel Perez, M. Eng. "Java Remote Microscope for Collaborative Inspection of Integrated Circuits," June 1997

Matthew D. Verminski, S.M., “A distributed Software Architecture for Semiconductor Process Design,” February 1998.

Brian Lee, S.M., “Exploring Semiconductor Device Parameter Space using Rapid Analytical Modeling,” January 30, 1998.

Jared D. Cottrell, M. Eng., “Server Architecture for MEMS Characterization,” September 1998.

TASK TITLE: D. Exploration of Emerging Technologies

PROJECT LEADER(S): A. Chandrakasan, D. Antoniadis

The key contribution of this task was developing design methodologies and tools for ultra low-voltage/low-power operation. The technology, circuit and architecture issues of scaling supply voltages to 1V and below have been investigated. Multiple-threshold CMOS is a key emerging technology, for which transistor sizing is a very challenging task. We have developed a tool for sizing transistors, replacing ad-hoc techniques used currently in industry. System energy models that consider module activities, usage patterns and leakage have been developed for system-level power estimation and exploration. Finally, to exploit remote resources, we have developed a web-based design framework that allows uses to remotely access and manipulate designs. The tool can be accessed at apsara.mit.edu.

Other significant results include:

* Developing a framework for characterizing the effect of substrate bias in controlling threshold voltage in scaled MOSFETs for use in extreme low-voltage power supply applications.

* Preliminary work has been done for controlling the substrate bias to compensate for process variations. The approach uses performance feedback to adjust the delay instead of previously reported approachs that control a fixed threshold. We have started the design of the control circuits in an advanced CMOS process.

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A. Chandrakasan, I. Yang, C. Vieri, and D. Antoniadis, "Design Considerations and Tools for Low-voltage Digital System Design", IEEE/ACM Design Automation Conference, pp. 113-118, June 1996.

A.P. Chandrakasan, A. P., V. Gutnik, T. Xanthopoulos, "Data Driven Signal Processing: An Approach for Energy Efficient Computing", ACM/IEEE International Symposium on Low Power Electronics and Design , pp. 347-352, August 1996. (Invited Paper)