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SEMI TECHNOLOGY SYMPOSIUM 90
PROGRAM SCHEDULE

Program Chairman: Norikazu Hashimoto
Chief Engineer, Mobara Works, Hitachi, Ltd.

Monday, October 22, 1990

i-Line Lithography

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1. Introduction

In the manufacture of ICs, most exposure equipment has switched from g-line to i-line steppers because of their increased focus depth at the same resolution. The development of higher NA i-line steppers and high-resolution i-line photoresist have also accelerated the use of i-line lithography. Accordingly, several device manufacturers will use i-line lithography on their 4M-DRAM production lines. This makes a review of the state of the art and projection in i-line process as timely.

2. Current i-Line Process

i-line lenses(resolution 0.65μm) and first-generation i-line photoresists were first anounced last year, and already higher NA i-line lenses(resolution 0.6 μm) and second-generation photoresists have come out. With these tools, we can resolve a minimum 0.35μm L&S at a critical best focus (Figure 1).

Figure 2 shows the focus-depth of i-line steppers NSR1755i7A (NA=0.5) and NSR1505-i6A(NA=0.45). An older i-line lens, i6A (NA=0.45), has a 0.3μm (range) depth of focus for 0.4 μm L&S. The i7A lens increases focus-depth to about 0.8 μm (range) for the same L&S.

The focus margin for 16M-DRAM (0.5μm-rule) lithography is estimated as follows.: The 0.5 μm L&S has a 1.3μm focus-depth (Figure 2) at the center of the lens field. The effective focus-depth is decreased by aberrations such as field curvature and astigmatic difference, focal-plane tilt and wafer surface roughness. Real values for these are shown in Table 1.

ΔZ is the value over a lens field (=24.7 mmϕ=480 mm^2). The 2-chip area size of 16M-DRAM is about 270 mm^2, so ΔZ is relaxed to 0.7 μm ($\equiv \Delta Z' = 270/480 \cdot \Delta Z$). Thus, the available focus-depth is estimated as 0.6 μm ($= \Delta Z - \Delta Z'$) for 0.50-μm

L&S. This value was 0.3μm only last year [1].

Regarding alignment accuracy, large scaling errors previously occurring on Al layers have been decreased by the introduction alignment FIA, [2] which uses a bright field iamge and broad-band light to decrease this scaling errors (LSA: $\pm$7 ppm, FIA: $\pm$ 2 ppm. Figure 3)

3. Problems

The 0.7 μm focus-depth of 0.5 μm L&S will be critical to 16M-DRAM production lines. To increase the focus-depth, we must decrease field curvature, astigmatism, focal-plane tilt and wafer LTV. Improving alignment accuracy could enlarge the minimum feature size, and, in turn, the focus margin. If a substrate could be made low-reflective for the exposure wavelength, higher resolution photoresists having a larger transmittance could be developed.

4. Trends

Many manufacturers will produce 16M-DRAM using the i-line process.

Some device manufacturers also think that the i-line process can be applied to 64M-DRAM production.

The typical parameters of a recently developed i-line lens and those of a widely used KrF lens are listed in Table 2.

Focus-depth data on these lenses is shown in Figure 4 [3], [4]. Both lenses have 0.9 to 1.0μm focus-depth for 0.35 μm L&S (64M-DRAM rule), the NA of the i-line lens is near the limit, and the field-size is too small (64M-DRAMs need more than a 20 mm $\square$ field). Large field i-line lenses may have an NA less than 0.55 to 0.60. It will be difficult to further improve i-line photoresist.

For the foregoing reasons, I believe the i-line process will not get a higher focus-depth than that in Figure 3 without using enhancement such as phase-shift [5] or FLEX. [6]

In contrast, the KrF stepper will be able to have a higher NA under the narrow band -width of a laser source and have a 20 mm $\square$ field. Quality excimer photoresists await only the attention of resist manufacturers willng to produce them regularly. Theoretically, KrF lithography has a 50% higher focus-depth than the i-line process,

an attractive advantage to IC plants.

Resolution and focus-depth can be improved in both i-line and KrF lithography using phase-shift. However, in general, aberrations appear more clearly on resist-profiles at defocusing, reducing the effect of enhanced focusing. These require further study.

5. Summary

In conclusion, 16M-DRAM will be manufactured using i-line process, and KrF lithography would be the most promising candidate for 64M-DRAM if resist manufacturers would concentrate on developing the needed excimer resists.

Acknowledgments

I thank Mr. M. Tominaga for his support.

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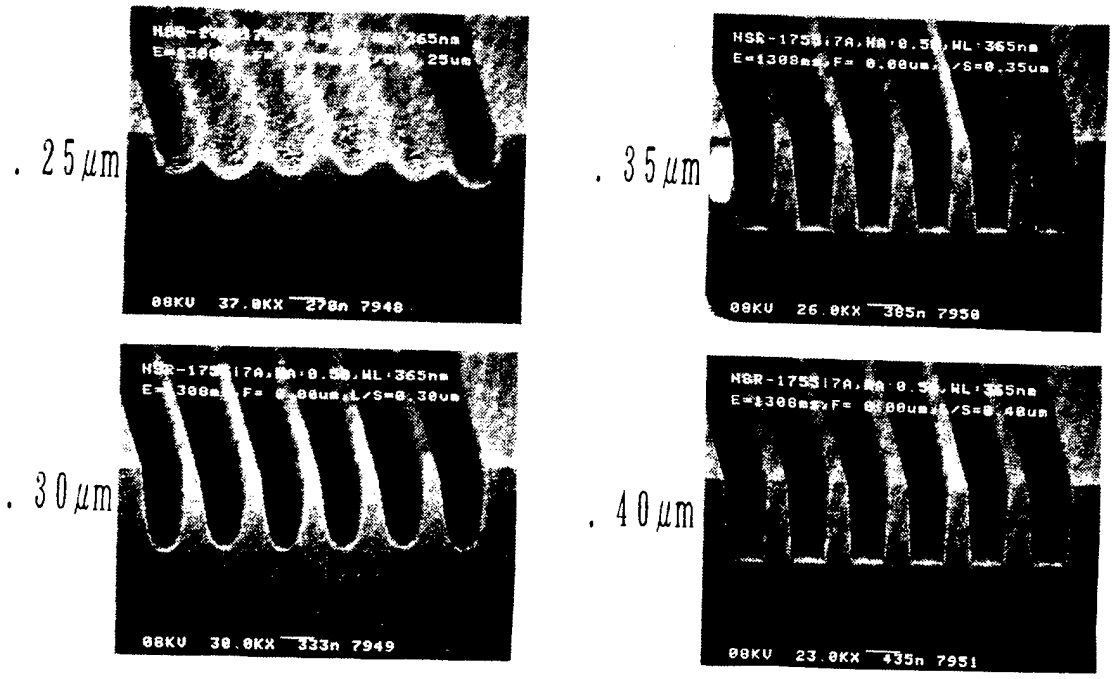

Figure 1 . SEM micrographs of the i-line photoresist patterns NSR1755i7A, 1.18μm thick. , 0.25~0.40μm L&S

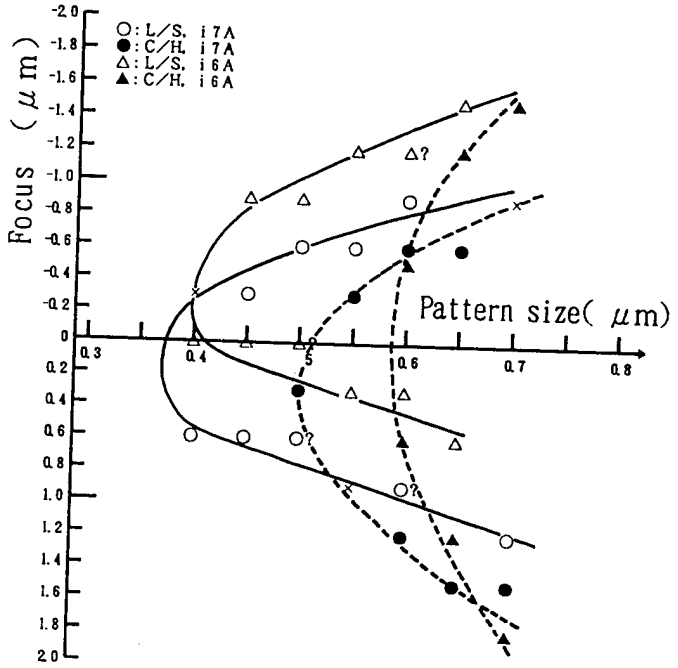

Figure 2. Focus-depth : NSR1755i7A, NSR1505i6A

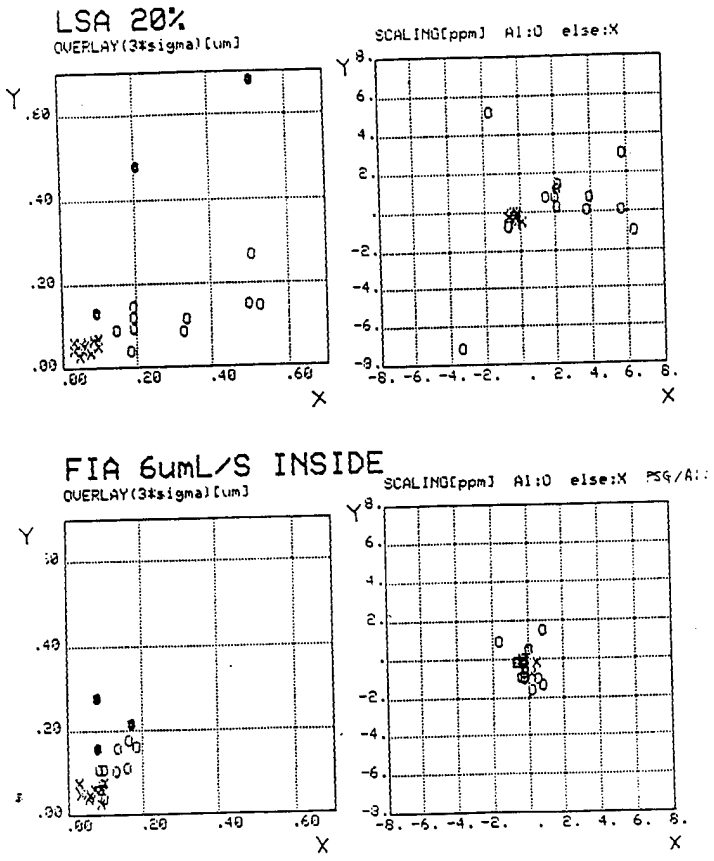

Figure 3. Alignment accuracy : Al layer (using LSA , FiA)

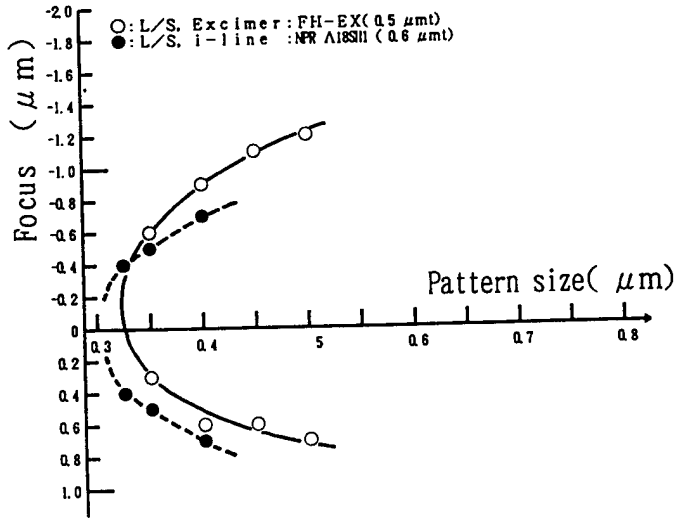

Figure 4. The depth of focus for various L&S with i-line 0.65NA lens & KrF 0.42 lens.
Resist : NPR Λ18SH1(0.6 μmt) for i-line, FH-EX(0.5 μmt) for KrF

Component	:	Typical value
Field curvature(range)	:	ΔC=0.2 μm
Astigmatic difference(max.)	:	ΔA=0.3 μm
Focal-plane tilt(/field diam.)	:	ΔT=0.2 μm
Autofocus repeatability	:	ΔF=0.1 μm
DXD leveling repeatability	:	ΔL=0.1 μm
Wafer LTV value	:	ΔW=0.5 μm

LTV: Local Thickness Variation

→ Total value $\Delta Z = \Delta C+\Delta A+\Delta T+[(\Delta F)^2+(\Delta L)^2+(\Delta W)^2]^{1/2} = 1.2\ \mu m$

Table 1 Components that decrease focus-depth.

Wavelength	Lens	Photoresist	Resolution(0.8 λ/NA)
i-line (365nm)	NA=0.65, 5 mm□	High-level	0.45 μm
KrF (248nm)	NA=0.42, 15 mm□	Low-level	0.47 μm

Table 2 Comparison of i-line and KrF lithography.

High Resolution Resists for i-line Process

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1. Introduction

Recently the technical level of fine patterning processes in the fabrication of semiconductor devices has remarkably advanced. The line-width processes have been oriented from submicron to halfmicron, and quarter-micron or the like that fine patterning is endlessly advancing. With its fine line patterning, reliable source operation also in lithographic process is now being studied from g-line to i-line, reducing the excimer laser source wavelength.
We are now actively devloping resist materials with high system performance moving with such demands. Here, the prosperous i-line light source as half-micron process technologies are focused and the development circumstances on positive-tone and negative-tone resists are presented.

2. i-line resist materials

2 -1 i-line light source

As well known, the wavelength 365nm of the emission spectrum of a high pressure mercury lamp is i-line and high resolution can be expected from the relationship of resolution $R=K\lambda/NA$ (λ: wavelngth, NA: numerical aperture, k=constant) compared to high NA g-line(436nm). To obtain the same resolution from the relationship of depth of focus(DOF)$=K\lambda/NA^2$ (K: Constant), the use of i-line light source is more advantageous than increasing the NA value by the g-line light source. (Fig. 1) Although i-line resist materials can use g-line materials, optical characteristics must be optimized for i-line. Actual evaluated effects of DOF characteristics are shown in Fig. 2.

2-2 i-line positive-tone resists

The positive-tone resist used for the i-line light source can use general-purpose resists e.g. OFPR-800, but resist profiles with a high aspect ratio are not obtainable due to a strongly absorbing resist after exposure and low optical transmittance in resist films. Therefore, high transmittance in i-line resists is required for preparing the rectangle resist profile. Fig. 3 shows OFPR-800 being used often as general-purpose resists and Fig. 4 shows the pre-and postexposure transmittance spectrum of the i-line resist TSMR-365 iR. TSMR-365 iR is found to be a substantial increase of postexposure transmittance compared to OFPR-800.

For further high resolution, some considerations to enhance better transmittance may be given. To enhance the i-line transmittance, it is allowed by operating developers. However, when increasing the resist transmittance more than that, the i-line high reflectivity on the Si substrate compared to g-line will be greatly affected with multiple interference in resist films and the dimensional disperson by changes of film thickness becomes bigger. It is likely to be affected by halation from the step coverage patterning on the underlying substrate. It is expected that the dimensional stability will be badly affected.

Fig. 5 and 6 show the effect which has been checked on its affection by standing wave for different resists with A B parameters(by models of F.H.DiII, etc.) This was measured for the movement of sensitivity when changed the resist film thickness on the Si substrate. These figures show that resists with the big B parameters have small amplitude of sensitivity against changes of film thickness and few affection on standing wave because of high optical absorbance by non-sensitivity constituent in films. There are few affection on standing wave for large B parameters, but sensitivity changes in a wide range of film thickness, that is,the bulk effect will become great. A parameters are affecting complicatedly to standing wave effects, bulk effects, halation effects. To provide high

performance of i-line resists, dissolution inhibiting effects at the exposure field and dissolution properties at the exposure field must be controlled including optimization of optical parameters such as ABC parameters, thereby the balanced resists are expected to show its excellent performance in resolution, exposure margin, DOF properties.
One example of resists obtained as a result of having studied the above performance is shown in Fig.7 ~ Fig. 10
It is found that the resolution properties and a wide focus margin are not only obtainable but excellent in important thermal resistance as resist properties.

2-3 i-line negative-tone resists

As for high resolution resist materials for i-line explosure, the conventional process can be applied as it is. Although the familiar positive-tone resist materials with processing are mainly used, the desired patterns may not be occasionally prepared by mask patterning in processes to apply the phase shifting method towards fine patterning. In such cases, negative-tone resist materials are very prosperous.
The negative-tone resist materials have several requirements. - 1. high sensitivity to the i-line light source 2. excellence in resolution 3. developable with organic alkali developer being used for positive-tone resists 4. exposure in the stepper is allowed (The reaction system is not easily affected by atmospheric constituent).
For resist materials to satisfy these requirements, the system using the optical crosslinker as the conventional bisazide is considered to be difficult for these requirements and we have employed the chemical amplifying system resists.
The chemical amplifying resists originated in the system[4) 5)] using the acid-catalyzed deprotection approach which Ito and Willson of IBM proposed and a lot of reaction systems have been announced since then.[6) 7)]

For chemical amplifying negative resist materials, the Novolak system base resin can be used, so that excellent resists in dry etchning resistance is expected, and the high sensitivity is possible. Here, the i-line negative resists studied by us is presented.

As for the process requirements, it is not so different from positive resist materials, that is, processes in the order of coating(film thickness:1.00um) ⟶ bake(90 °C/90 sec) ⟶ exposure(by the stepper system) ⟶ PBB(110 °C/90 sec) ⟶ developer(NMD-32.38% 65 sec).

Fig.11 shows the transmittance spectrum of pre-and postexposure resist films. The transmittance in the vicinity of i-line resists has a tendency which post-exposure transparency decreases resists as opposed to positive resists. Fig.12 shows the sectional view of patterns when this resist was exposed in the use of 0.43 i-line stepper for a NA value. For resolution, an i-line path to 0.40um was achieved and vertically high resist profiles were obtained. The linearity is advancing to about 0.50 um in feature size(Fig.13).

3. Conclusion

For the i-line resist, there have been many achievements especially on positive-tone resist materials. Issues to be improved are, for example, optical properties in resist films, the possible optimization of high resolution resists by improvement from a point of view of the dissolution-speed difference to pre-and postexposure devloper. Although it may be fundamentally the same effect on negative-tone resists, there are many unknown issues still now and specific and require research and development in future will be required more than postive resist materials.

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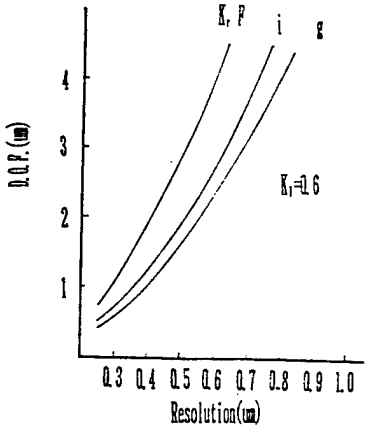
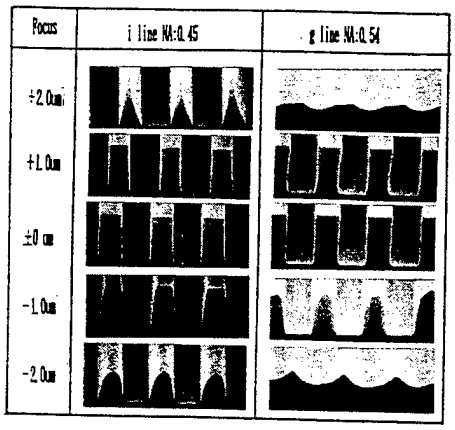
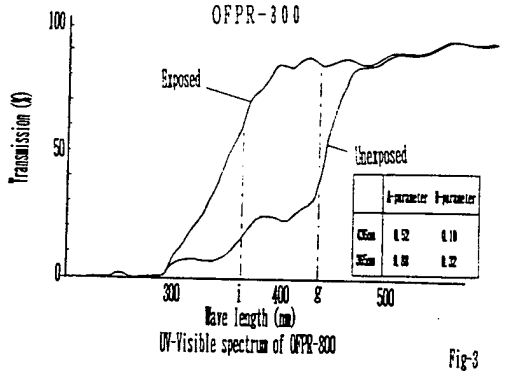


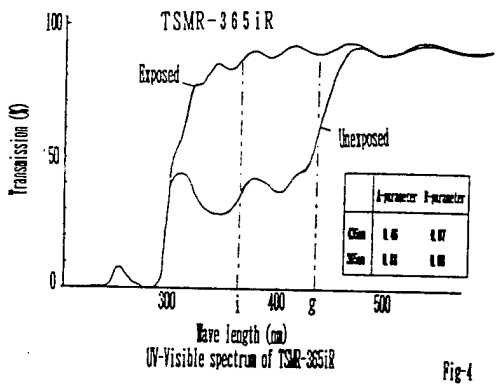
Resolution vs. D.O.F. Fig-1



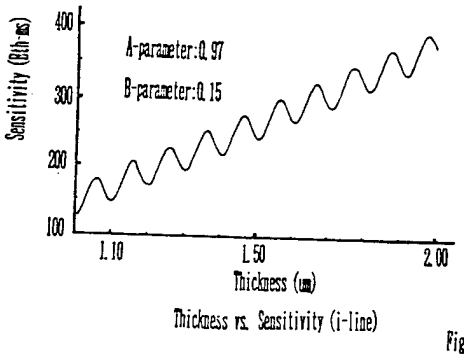
Positive resist profile of 0.7um L&S Fig-2



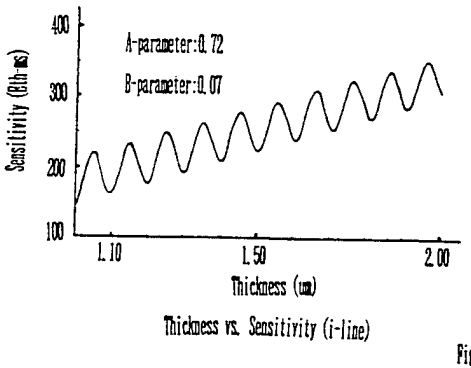
UV-Visible spectrum of OFPR-800 Fig-3



UV-Visible spectrum of TSMR-365iR Fig-4

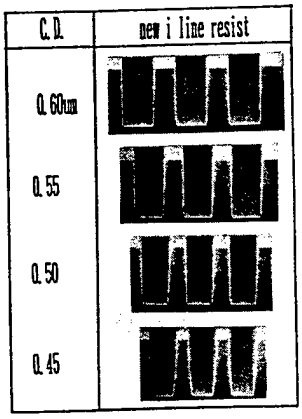


Thickness vs. Sensitivity (i-line) Fig-5



Thickness vs. Sensitivity (i-line) Fig-6

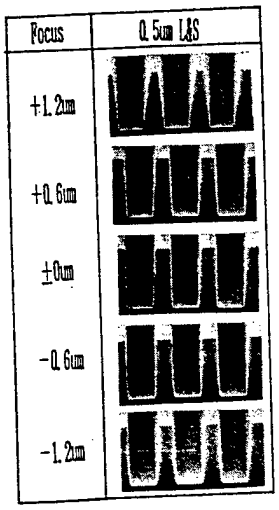
NA : 0.43



Cross sectional profile of the new i line resist

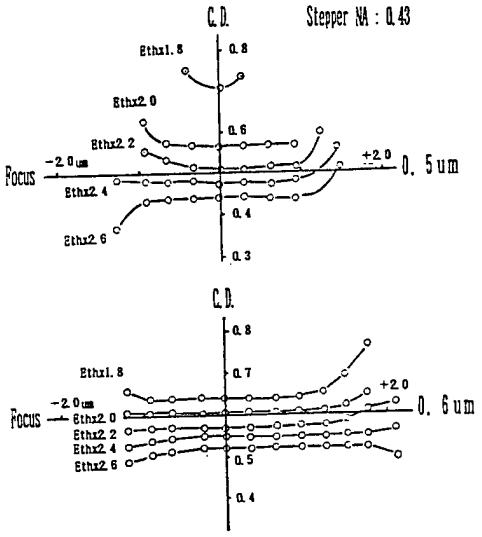
Fig-7

NA : 0.43



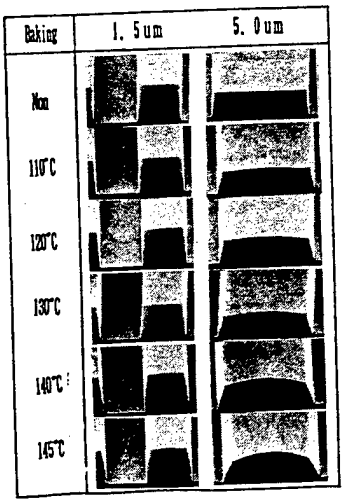
Focus latitude of the new i line resist

Fig-8



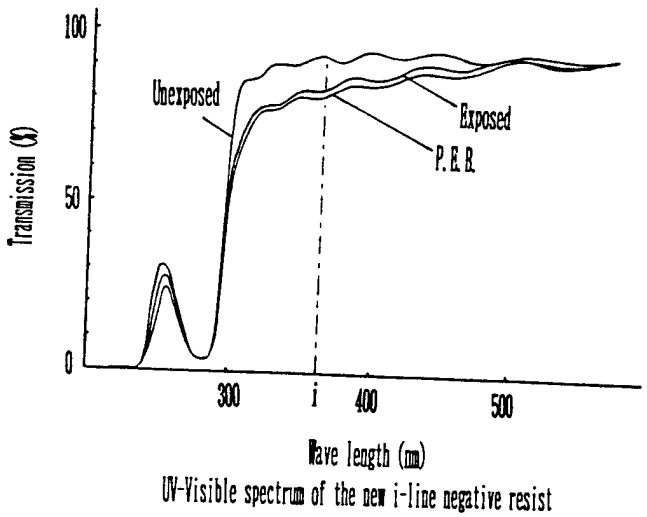
Focus latitude of the new i-line resist

rig-9



. Thermal resistance of the the new i line resist

Fig-10



UV-Visible spectrum of the new i-line negative resist

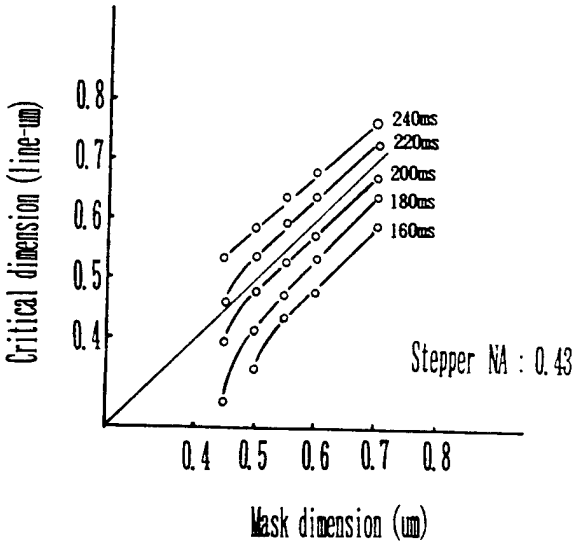
Fig-11

NA : 0.43

C.D.	Exp : 220ms	Exp : 240ms
0.60um		
0.55um		
0.50um		
0.45um		
0.40um		

Cross sectional profile of the i line negative resist

Fig-12



C.D. linearity of the new i-line negative resist

Fig-13

HIGH RESOLUTION I-LINE POSITIVE PHOTORESISTS

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1.Introduction

According as the design rules of VLSI technology are being rapidly and steadly reduced through sub-micron to half-micron features, the resolution required for both resist materials and optical steppers is becoming higher year by year. Therefore, strong efforts can be observed in the improvements of resist materials,[1] and processes like surface silylating systems,[2] phase-shifting mask method.[3] Within the last years, the numerical apearture (NA) of g-line steppers has incrased up to 0.6,[4] to realize the requirements for higher resolution. However, the increase of NA reduces the depth of focus (DOF) of imaging system, and the lack of DOF is very serious problem in practical device fabrication. On the other hand, instead of conventional g-line exposure systems, the i-line lithography is becoming more popular, nevertheless, future optical lithographers set their hope in KrF excimer laser lithography.[5]

Among these technologies, at prsent, i-line lithography has shown itself to a viable technology in mass-production level, capable of providing improved resolution and DOF, when compared with well-established high NA g-line exposure systems.

These trends lead us to develop i-line resits with higher resolution capability. In this paper, the developments of resists suitable for i-line exposure system are introduced from the point of view of material design, that is, novolak resins and photo-active compounds (PAC) based on naphtoquinonediazides(NQD). And evaluation results of these newly developed resists are also described. We will emphasize that the choice of ballast molecules of PACs play significant roles in the performance of i-line resist materials compared with those in g-line resists. Safety solvent (non-ECA) grades, which are rapidly required since

this year, are also included.

2.Material Design

Positive photoresist generally comprises an alkaline-soluble novolak resin, and PAC, usually a NQD sulfonic ester of hydroxybenzophenone, a solvent and various additives that improve film quality. We will consider the material design concept for high performance i-line resist separating into two parts, resin and PAC.

1)Resin

The largest difference between i-line and g-line resists design is probably the transparency of the resist films at exposure wavelength. The pattern profiles of some g-line resists composed of conventional resin and PAC are not enough well in i-line exposure. This poor pattern profiles are thought to be caused by lower transmittance of the resist films. For novolak resin design, however, we have employed the same concept as that of g-line resists, because novolak resins don't affect the transparency around i-line region.

Concerning the improvement of the performance of g-line resists, we have investigated the influence of substituents of phenol rings on the performance of the formulated resists.[6] It has been demonstrated the importance of methylene bond position, and intramolecular and intermolecular hydrogen bond between novolak resins and PACs. We have tried to control the methylene bond position and the degree of hydrogen bond by introducing methyl substituents on phenolic compounds. And then, we have succeed in the balance of the trade-off relationships between sensitivity, heat resistance, resolution capability and so on by applying some novel novolak resins polymerized from m-cresol and substituted phenols.

2)PAC

The role of the PAC has received considerable attention on the transparency of the formulated resist films. The PAC based on conventional hydroxybenzophenone has significant absorption

around 365nm both before and after exposure. This absorption may be due to π-π^* (and or n-π^*) transmition of benzophenone chromophore.

Thus, we have examined several PAC strucures, and as a results, it has been found that a special non-benzophenone strucure is suitable for the PAC ballast molecule in i-line exposure. Figure 1 shows absorption spectra of this new ballast compound, also included the conventional hydroxybenzophenone for comparison. This new ballast compound has higher transparency around i-line compared with the conventional hydroxybenzophenone, expecting better photobleaching properties (see Fig. 2).

In next we will mention newly developed i-line resists using the novel resins and new PAC described above. Table 1 indicates comparison of the components of two i-line resists, that is, our conventional i-line resist, PFR IX150 and a newly developed i-line resist, called as "Resist A". PFR IX150 is composed of the resin synthesized from m-cresol (M) and substituted phenol (α), and the conventional PAC based on hydroxybenzophenone. On the other hand, a new i-line resist is composed of the resin Mα' and the new PAC derived of a non-benzophenone ballast molecule. Phtosensitive groups are common NQD in both i-line resists.

Figure 2 displays transmittance curves of the two resists before and after exposure. Resist A has a superior transparency both before and after exposure,and smaller A and B parameters[7] compared with those of PFR IX150 (Table 2). It should be, however, mentioned that there is an optimum A value becasuse of the standing wave effect and the bulk effect, while the smaller B value is necessary for obtaining excellent resist profiles.

3.Evaluation results of new i-line resists

Table 3 summarizes evaluation results of the new i-line resist, Resist A. Resist A has a resolution of 0.38μm in exposure of i-line lens with a NA=0.45 stepper. Figure 3 shows SEM photographs of line and space (L/S) profiles of the resists. The pattern geometries are 0.5μm down to around 0.40μm. The rectangular pattern profiles even in 0.40μm are obtained in Resist A, and the pattern of 0.38μm L/S is separated without a

scum. On the other hand, PFR IX150 has a round top pattern profiles below smaller features of 0.50μm L/S.

The defocus properties of the resists at 0.50μm L/S geometry are photographed in Fig. 4, and DOF for various L/S patterns are shown in Fig. 5. In Fig. 5, we have defined DOF as without loss of remaining resist thickness and within $\pm$5% pattern width loss. Resist A has a wider focus latitude.

The comparison of the pattern profiles of 0.60μm contact hole versus defocus are shown in Fig. 6, indicating the better profiles of Resist A.

Lastly, let's see their heat resistance properties (Fig. 7). The heat resistance of Resist A maintains up to 130℃ at lager pattern (100μm).

These improvements of resist profiles, resolution capability, defocus properties and other lithographic performance of Resist A may be due to better photo-bleaching characteristics of the new PAC based on a non-benzophenone structure.

Furthermore, we have developed a new resist, Resist B, with more improved resin, which resist is formulated by using non-ECA (ethyl lactate) as a coating solvant. Resist B has superior resolution capability of 0.36μm with excellent wall profile printed on a 0.45 NA i-line stepper (Fig. 8). This pattern feature is almost equal to the exposure wavelength. Other lithographic properties of this new Resist B will be published elswhere in the near future.

4.Summary

In summary, the new PAC on a non-benzophenone ballast molecule cause the improvement of transparency of the resists at i-line region. Resist A and B with the new PAC have been developed and these resists have superior lithographic performance. At present, the resolution capability of 0.36μm have been obtained by exposed a 0.45 NA i-line stepper. These new resists will be applicable to less than half-micron design rules.

5.Acknowledgement

I will wish to express my great thanks to Messrs. H. Hara, M. Ebisawa, T. Kajita, M. Kurokawa, and Dr. T. Ohta for their helpfull experiments and discussions. I also would like to my gratitude to T. Miura and Y. Yoshida for their encouragements through this work.

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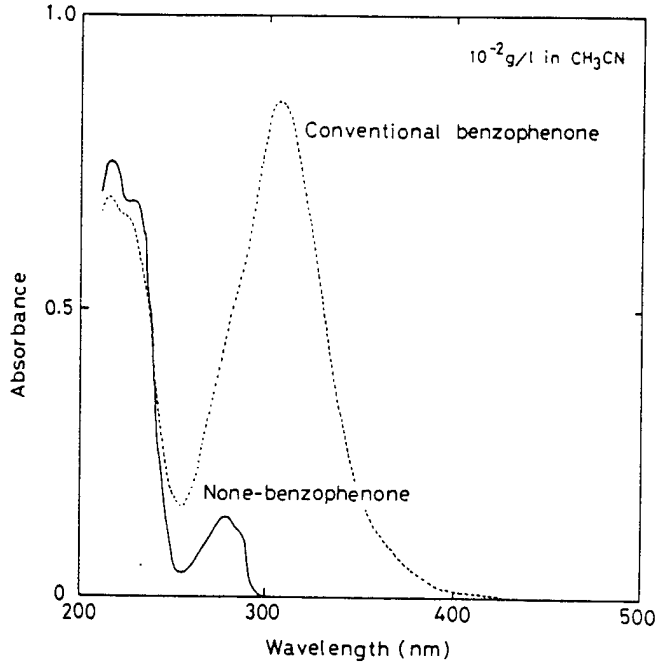

Fig. 1. UV–VIS spectra of the new none–benzophenone ballast compound and conventional benzophenone.

Table 1 Components of PFR IX150 and Resist A

Resist	Resin Monomer	PAC Photosensitivity Moiety	PAC Ballast Molecule
PFR IX150	Mα	NQD	Conventional Benzophenone
Resist A	Mα'	NQD	None-benzophenone

M: m-Cresol, α, α': Substituted Phenol, NQD: 1,2-Naphtoquinonediazide.

Table 2 Comparison of A, B parameters

Resist	$T_{(0)}$ %	$T_{(\infty)}$ %	A μm^{-1}	B μm^{-1}
Resist A	44.2	93.3	0.75	0.069
PFR IX150	21.8	91.8	1.20	0.071

Resist thickness: 1.2μm.

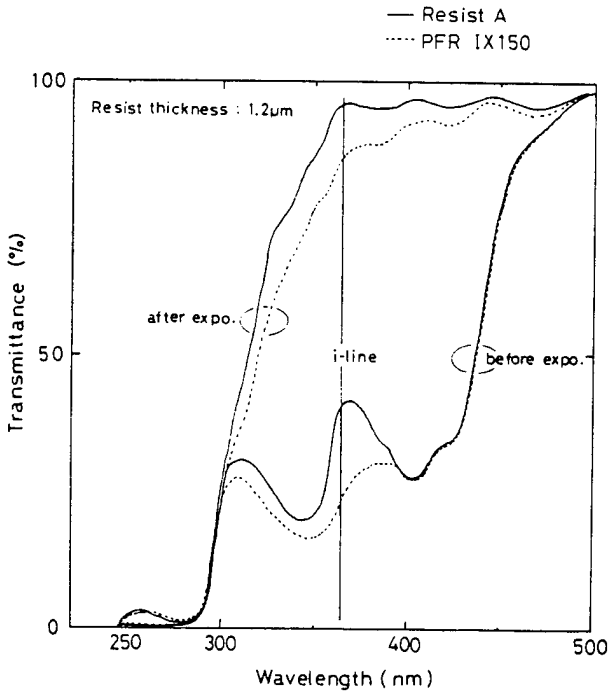

Fig. 2. Unexposed and bleached transmittance spectra of Resist A and PFR IX150.

Table 3 Evaluation results

Resist	Sensitivity Eth (msec)	Sensitivity Eop (msec)	Eth/Eop	Resolution (μm)
Resist A	200	400	0.50	0.38
PFR IX150	235	490	0.48	0.42

Eth: Threshold. Eop: Optimum (0.60μm L&S).
Coating thickness : 1.21μm. Exposure: NIKON NSR 1505 i6A (NA=0.45).
PEB : 110 ℃ 60sec.

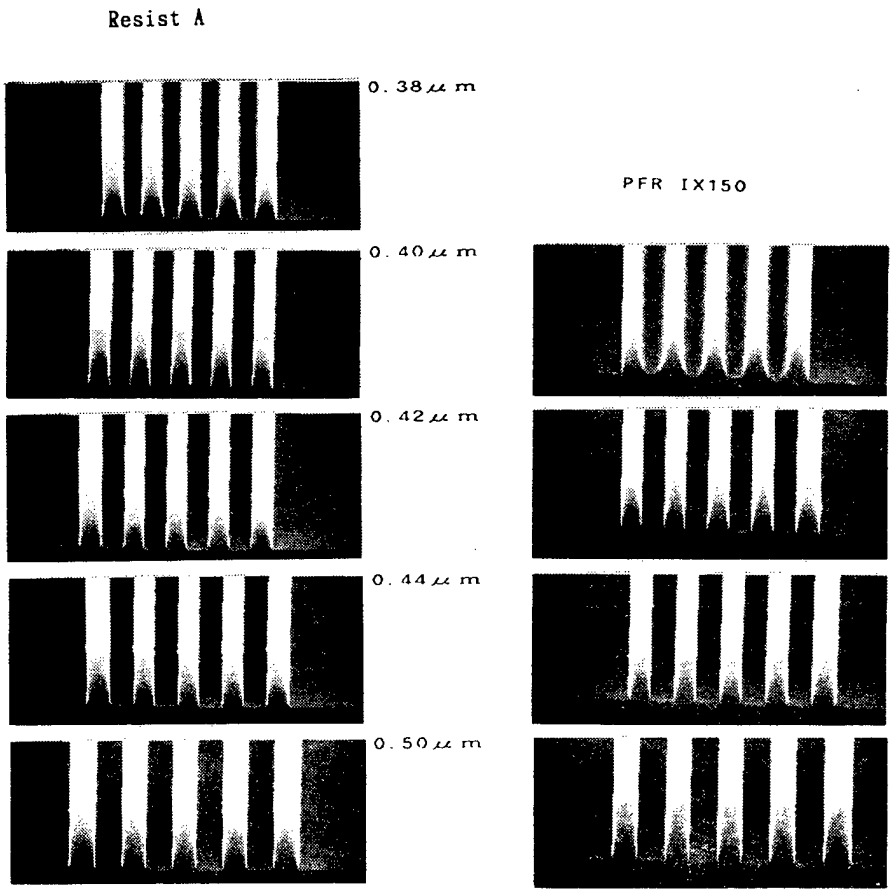

Fig. 3. Resist pattern profiles of various L/S features in Resist A and PFR IX150.

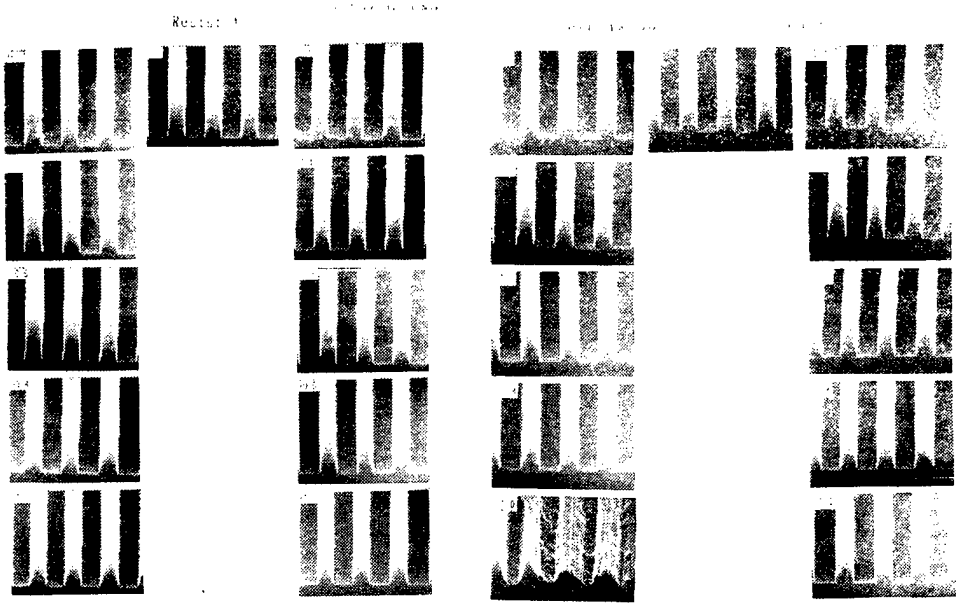

Fig. 4. Defocus properties of 0.50 μm patterns in Resist A and PFR IX150.

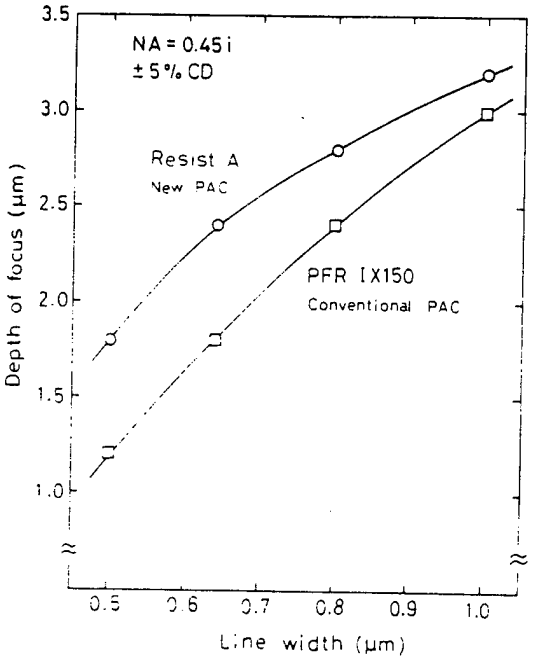

Fig. 5. The depth of focus for various L/S patterns.

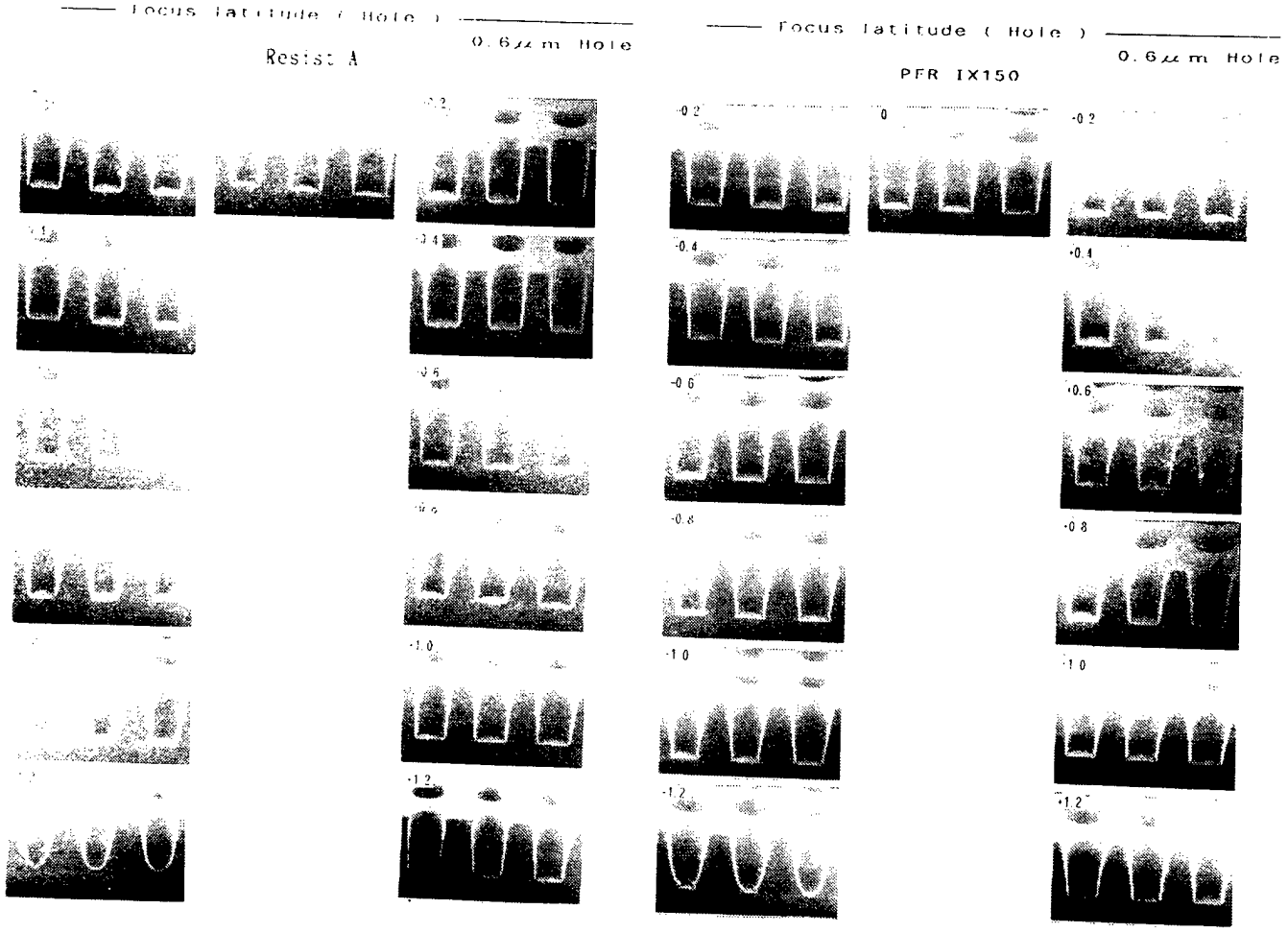

Fig. 6. Defocus properties of 0.60 μm hole in Resist A and PFR IX150.

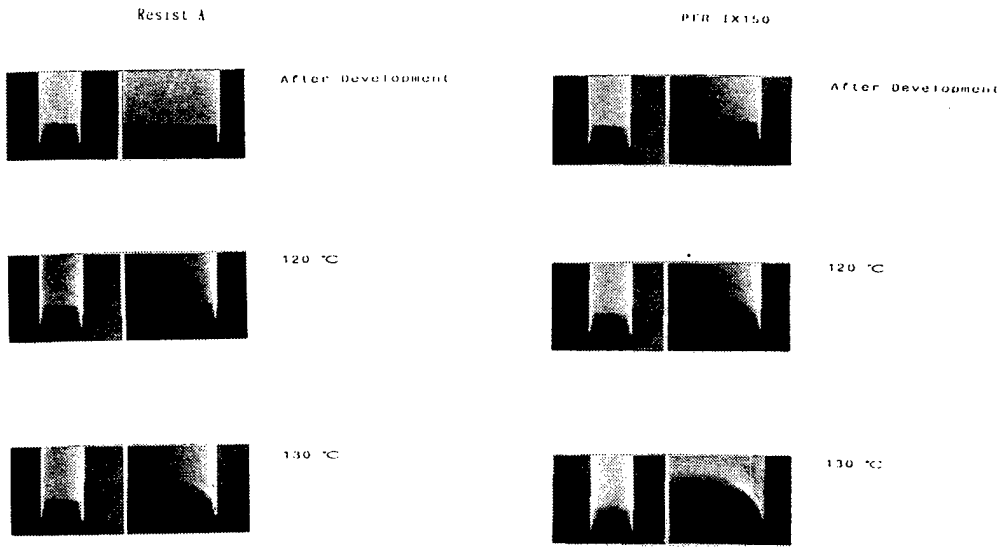

Fig. 7. Heat resistance properties of Resist A and PFR IX150.

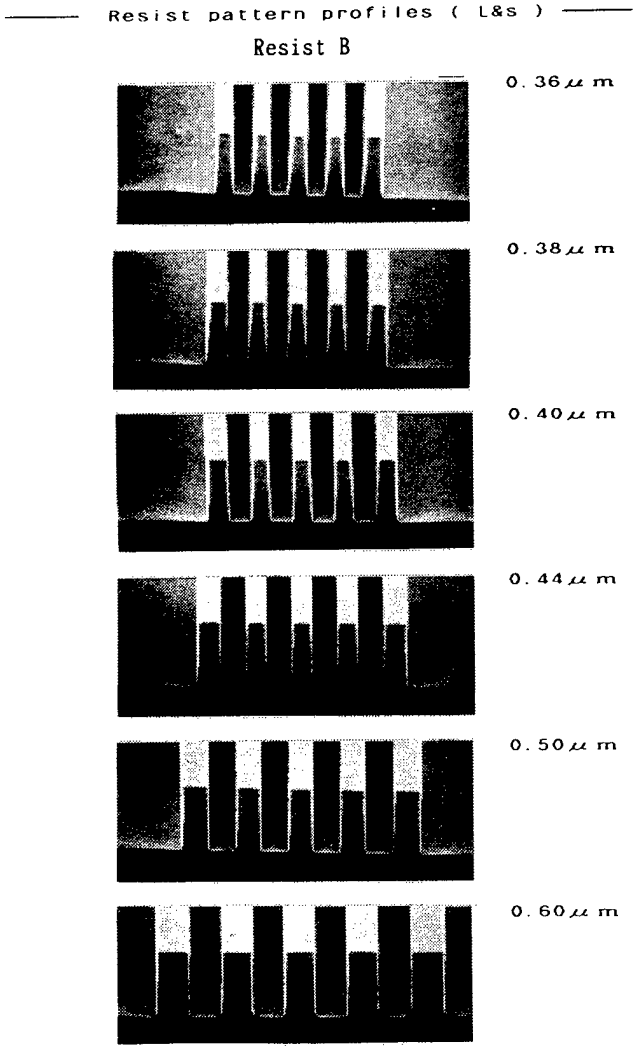

Fig. 8. Resist pattern profiles of various L/S features in Resist B.

High Performance Positive I-line Resist

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1. Introduction

Positive i-line resists for the fabrication of half-micron designed devices are required to have high resolution, excellent profile, wide focus and exposure latitude, and chemical stability.

The design concept and performances of our "®Sumiresist PFI-series" are presented.

2. Design Concept

High performance positive i-line resists "®Sumiresist PFI-series" are composed of novolak resins and 1,2-diazoquinone-5-sulfonyl(1,2,5-DQ) ester of a novel non-benzophenon-type ballast group. This new sensitizer is the important feature of our i-line resists.

Conventional g-line resits, using 1,2,5-DQ ester of a tetrahydroxybenzophenon(THBP)group(Fig.1). Comparing i-line exposure of these g-line resists with g-line exposure, smaller γ value, more slanted profile, decreased resolution are observed (Fig.2).

This is because of their large optical parameters A and B for i-line exposure. Dill[1] defined optical parameters as follows, where d is a thickness of resist film, T(0) and T(∞) are transmittances of unexposed and fully exposed resit film, respectively. Therefore, parameter A represents the absorbance of photo active compound(PAC), Parameter B corresponds to the absorbances of photo inactive components, resins and ballast group.

$$A = (1/d) \cdot \ln [T(\infty)/T(0)] \qquad (1)$$

$$B = (1/d) \cdot \ln [T(\infty)] \qquad (2)$$

Based on above observations, we decided that optical parameters of high performance i-line resist should be favorable to the same magnitude with that of g-line resists for g-line wavelength.

In the case of i-line wavelength, parameter B largely depends on the absorbance of sensitizer's ballast group. Absorption of novolak resin is negligible. Benzophenon compounds are unfavorable because of their strong absorption at i-line. Therefore we decided to chose non-benzophenon-type ballast group, which has smaller absorption, for our high perforamance i-line resists.

To reduce parameter A of i-line resit, it is necessary to reduce the quantity of PAC than that of g-line resist, because of larger absorption coefficient of 1,2,5-DQ for i-line than that for g-line.

However, in the case of conventional sensitizer of g-line resist, reduction of PAC contents reduces resolution. The reason of this observation seems to be explained as follows.

When the developement of resist film, sensitizer may inhibit the dissolution and photo decomposed compound of sensitizer acts as a dissolution accelator. Therefore reduction of sensitizer may decrease the difference of dissolution rates between exposed and unexposed resist area.

In the case of the conventional sensitizer, 1,2,-diazoquinone-5-sulfonyl ester of THBP, above mentioned problem may be resolved by increasing its esterification ratio.

However, the high-esterified sensitizer often gives scums and particles, because of its low solubility to the resist's solvent.

We considered that novel ballast group which gives high γ value is necessary to our high resolution i-line resists which have smaller quantity of PAC than g-line resists.

The conditions required for our new sensitizer are listed as follows.

① Sensitizer having non-benzophenon-type ballast group, which has small absorption for i-line
② Sensitizer having novel ballast group which gives high γ value for i-line resist
③ Sensitizer having high solubility to the resist's solvent
④ Sensitizer which is far from scum

After several screening, we invented novel sensitizer which satisfy all of above conditions. Then We developed high performance positive i-line resists "®Sumiresist PFI-series" by optimizing their composition.

3. Performances of ®Sumiresist PFI-15, PFI-16

In this section, we show performances of PFI-15 and PFI-16 which contain high-γ sensitizer having non-benzophenon-type ballast group. PFI-16 is the improved version of PFI-15.

Fig.3 shows absorption spectra of unexposed and fully bleaced film of PFI-15 on glass plate. Optical parameters of PFI-15 and PFI-16 for i-line are almost same with that of our conventional g-line resist PF-7400 for g-line(Table 1).

Resolution of PFI-15 and PFI-16 at each E_0 are listed on Table 2 for three i-line lenses. Here, E_0 is defined as the exposure energy required to make L/S 0.5μm same with mask size. It is clearly shown that the high-γ sensitizer can give excellent resolution even though its small content. In the case of higher NA lenses, PFI-16 shows higher resolution than that of PFI-15.

Fig.4 shows focus latitude of PFI-15 and PFI-16 at each E_0 for L/S 0.5μm (NA 0.40). We can get almost vertical patterns maintained through wide depth of focus by using the high-γ sen-sitizer.

Hole pattern's linearity of PFI-15 and PFI-16 are given in Fig.5 (NA 0.40). PFI-16 has higher hole resolution than that of PFI-15.

As far as particles in resist, quality control on production and storage stability of 0.2μm size level are important for the fabrication of half-micron designed devices.

For PFI-15, Table 3 shows the storage stability of particles at 23℃. PFI-15 shows high stability for every particle size. It may be attributed to high solubility of the novel sensitizer, which can dissolve in the resist's solvent about 10 times more than conventional sensitizers.

	Particles for several size(μm) (particles/ml)				
	0.2~0.3	0.3~0.5	0.5~1.0	1.0~2.0	>2.0
after bottoling	190	64	7	0	0
23℃ at 1month	210	68	8	0	0
23℃ at 2month	180	57	5	0	0
23℃ at 3month	230	81	11	0	0

Table 3 Monthly observation of number of paricles of PFI-15 stored at 23℃ measured by RION kl-20

Acknowledgement

Performances shown here were measured under following conditions

Substrate : 4-inch Si wafer (exposed to HMDS vapor at room temperature)
Prebaking : 90℃ 60s (Direct hot plate)
Initial film thickness : 1.265μm (measured by optical thickness meter
" Lambda Ace ; Dainippon Screen Co.Ltd." using n=1.68)
Exposure : i-line stepper " LD5010-i " ; Hitachi Co.Ltd. (NA 0.40)
Postexposurebaking(PEB) : 110℃ 60s (Direct hot plate)
Developement : 2.38% TEMAH 60s, paddle method at 23℃

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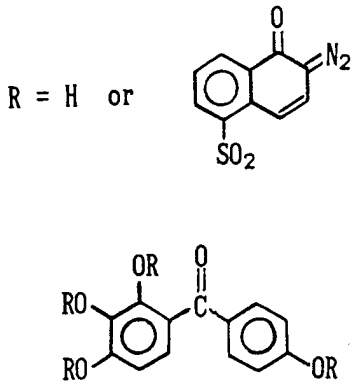
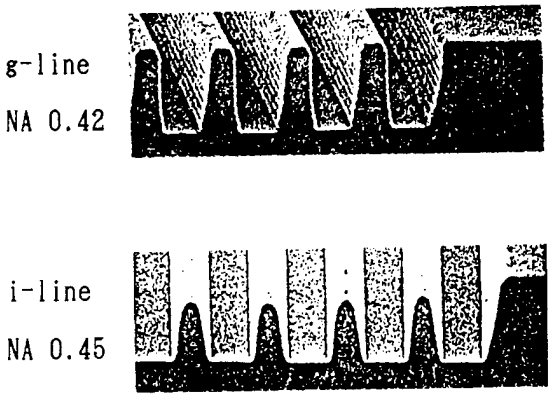


Fig.1 Conventional Sensitizer
1,2,5-DQ ester of THBP

Resist	optical parameters(μm^{-1})			
	i-line		g-line	
	A	B	A	B
PF-7400	1.36	0.16	0.77	0.05
PFI-15	0.78	0.05	0.45	0.05
PFI-16	0.78	0.05	0.45	0.05

Table 1. List of Optical parameters
PF-7400 is our conventional g-line resist



L/S = 0.55μm

Fig.2 SEM images of g-line resist
exposed g- and i-line

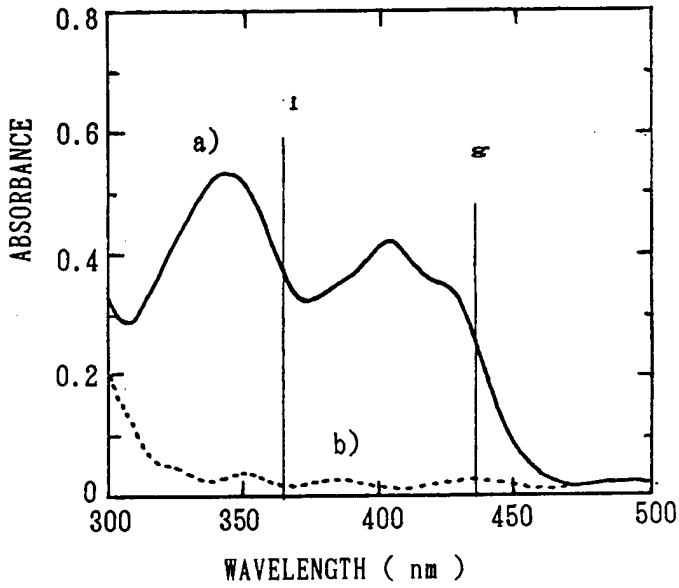


Fig.3 Absorption spectra of PFI-15
0.95μm thickness film on glass
a) unexposed
b) after bleaching

NA	L/S Resolution (μm) at E_0	
	PFI-15	PFI-16
0.40	0.45	0.45
0.5	0.40	0.36
0.65	0.35	0.30

Table 2
List of L/S Resolution (μm)
at E_0 of PFI-15 and PFI-16
for three i-line lenses

i-line NA 0.40 L/S 0.50μm

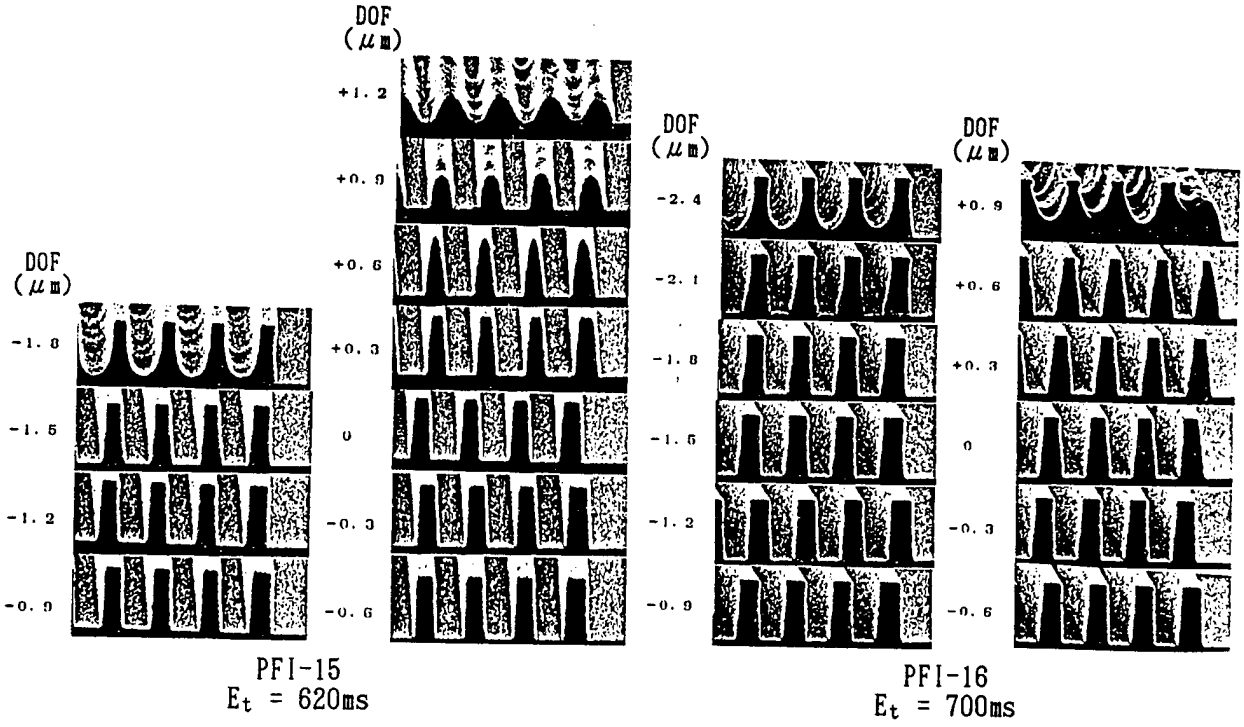


Fig.4 SEM images of focus latitude of PFI-15 and PFI-16
Film thickness 1.265μm, L/S 0.50μm, NA 0.40 i-line stepper

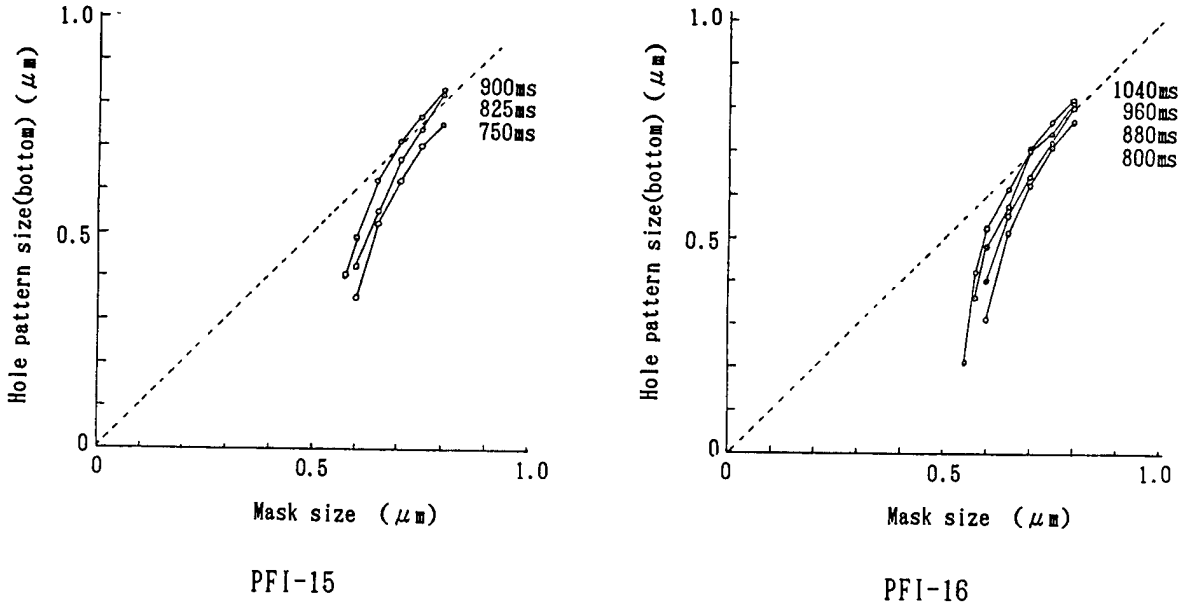


Fig.5 Hole-liniarity of PFI-15 and PFI-16
Film thickness 1.265μm, NA 0.40 i-line stepper

i-LINE STEPPER

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Nikon Corporation, Tokyo, Japan

1. Introduction

As sub-halfmicron processing technologies are being established toward mass production of 16M DRAM and for the development of 64M DRAM, the reduction projection exposure system (hereinafter referred to as the "stepper") using the i-line has proved to be the primary candidate in practical lithography technology. This article introduces the performance of the latest i-line stepper and discusses the propriety of applying the stepper to the mass production of 16M DRAM. Some views are presented later with regard to the potentialities of the i-line stepper as the next-generation lithography technology for 64M DRAM, together with the problems which need to be solved.

2. Mass Production of 16M DRAM with an i-line Stepper

Lithography requirements for mass production of 16M DRAM seem to be at a practical resolution of 0.5 μm and a total overlay accuracy of 0.15 μm or better. Under the assumption that a discussion of "why the i-line for 16M DRAM" is finished, this article discusses what levels of performance requirements for 16M DRAM mass production have been achieved with the current i-line steppers.

2.1 Resolution

It is generally believed that mass production of 16M DRAM requires a resolution of approximately 0.5 μm. On the other hand, the depth of focus (DOF) needed by the projection optics seems to be approximately 1.5 μm from such considerations as process topography, wafer flatness, and focus error of the exposure system.

Simulations of DOF against NA of i-line lenses are shown in Figure 1. Photoresist #1 is the first-generation i-line resist, while photoresist #2 is a high-resolution resist in current use. A lens of higher NA has been sought, to allow for any small increase of resolution margin in processes. At levels around the 0.5 μm L/S required in 16M DRAM, however, the DOF projected by the simulation is close to the 1.5 μm DOF requirement mentioned above and is not satisfied with NA = 0.54. Therefore, a level of approximately NA = 0.5 is considered to suit the 16M DRAM production using this data of resolution and DOF.

The DOF for 0.5 μm L/S of the i-line lens of NA = 0.5 currently announced from Nikon is shown in Figure 2. The lens provides DOF of 1.5 μm or better, substantially meeting the requirements. We intend to make further improvements toward even greater allowance of DOF.

2.2 Overlay

When we consider the mix-and-match of exposure systems, overlay error should be discussed in terms of total overlay accuracy (matching), which is given as a synthesis of lens distortion and alignment accuracy. Recent steppers offer effective capabilities of approximately 0.15 μm in matching performance. When we merely look at the value, the steppers appear to meet the mass production requirements for 16M DRAM. However, when we consider the practical capabilities of machines for mass-production, the accuracy mentioned above must also be:

(1) stable over the long term, and

(2) achievable in production processes.

First we will look at the stability of lens distortion mentioned in (1). The heat of the exposure light absorbed by the i-line lens has decreased with the improvements of glass materials. However, the absorption cannot be reduced to zero, and the resultant change in magnification is inherently unavoidable. Thus this is a variation contributor that cannot be ignored with the finer patterns of the future.

At Nikon, minute variation in magnification is minimized by controlling the air pressure in the lens. This technique was first made available at the stage of g-line lens. Figure 3 presents experimental data showing the time-based magnification variations of the i-line described above when the light energy is varied. The data demonstrates that magnification variation is acceptably small.

For alignment accuracy, both of considerations (1) and (2) are important. Factors of overlay error include measurement capability of the sensor, positioning accuracy of the wafer stage, reticle rotation and so on. Of these, the measurement capability of the sensor in production processes is considered to have the largest influence. Today, the common method in use detects the diffraction and scattering of laser and is highly evaluated for its performance with ordinary layers[1]. But a problem has been pointed out when the method is applied to metal layers. Depending on the condition of the metal surface, the high coherency of alignment light tends to produce distorted signals due to interference, which deteriorates alignment accuracy.

A new alignment sensor has been developed, in which the coherency is decreased by using a wider band of alignment light and image processing technique is used to detect the edge of the alignment mark[2]. This approach, called Nikon Field Image Alignment (FIA), is compared with the present sensor, Nikon Laser Step Alignment (LSA), in Figure 4, in terms of accuracy in various aluminum processes. (The data on LSA was taken without alignment optimization.) As shown, accuracies with FIA are mostly around 0.1 μm.

Because the light band is sufficiently broad, the new sensor consists of off-axis optics. Yet the measurement stability (baseline drift) of the sensor is as high as that of the TTL system in current use, as demonstrated in Figure 5.

These data convince us that the level of 0.1 μm alignment accuracy can be realized while satisfying the requirements of stability and achievability in production processes.

3. Prospect for Lithography of 64M DRAM

Lithography for 64M DRAM requires resolution of approximately 0.3 μm. Some people propose exposing micropatterns of the 0.3 μm level with the i-line while others suggest the use of a KrF excimer laser. At Nikon, development is under way to deal with both of these alternatives. Here, we will discuss the potentialities of the i-line stepper.

As described earlier, the problems with resolution cannot be solved by merely increasing NA. A process factor K of 0.5 or lower will be needed. A proposal worth attention as a solution is phase shift technology. Since this technology is effective regardless of exposure wavelength, it is taken as one of the most important technologies to be tackled at Nikon. Major issues with the new technology are:

(1) Developing an optimum imaging system, including reconsideration of NA/σ.

(2) Establishing technologies, such as the inspection (defects, particles, etc.) and measurement (film thickness, etc.) of the phase shift mask.

Now we will look at alignment issues. Process compatibility will call for an alignment sensor suitable for the planarization process which is said to be already in partial use in 16M DRAM production. Nikon has developed a new sensor, called Nikon Laser Interferometric Alignment (LIA), which applies optical heterodyne detection in a two-beam interference method[2]. The structure of the new sensor is shown in Figure 6. Resolving power is 1 nm, with measurement repeatability of approximately 4 nm. Since this sensor illuminates and detects the whole mark area at a time, it provides high averaging capability and deals well even with rough surfaces. Figure 7 provides accuracy comparisons with the present sensor (LSA) for an aluminum layer and indicates significant improvement. This averaging capability also boosts alignment mark detection sensitivity and is thus effective for the alignment patterns with low step height. Evaluation is under way to ascertain the limit of step height for various processes.

To realize the 0.1 μm or better alignment accuracy required in 64M DRAM, the improvement of fundamental performance of the stepper is an essential condition as well as the practical availability of a high-accuracy sensor described above. A breakthrough, including a review of system fundamentals, will be required.

4. Conclusion

Exposure system has little allowance left in its performance when it goes beyond a 16M level. It is important to work on comprehensive development, including the development of new imaging technologies, by exchanging more information between LSI makers and exposure system suppliers.

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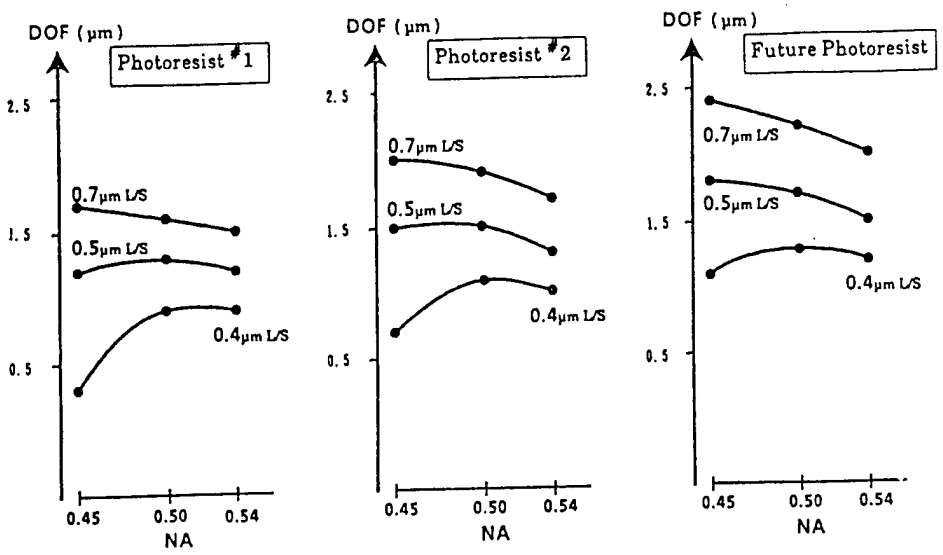


Fig. 1 Depth of Focus (DOF) VS NA (i-line, $\sigma = 0.6$)

(Computer Simuration for ideal optics)

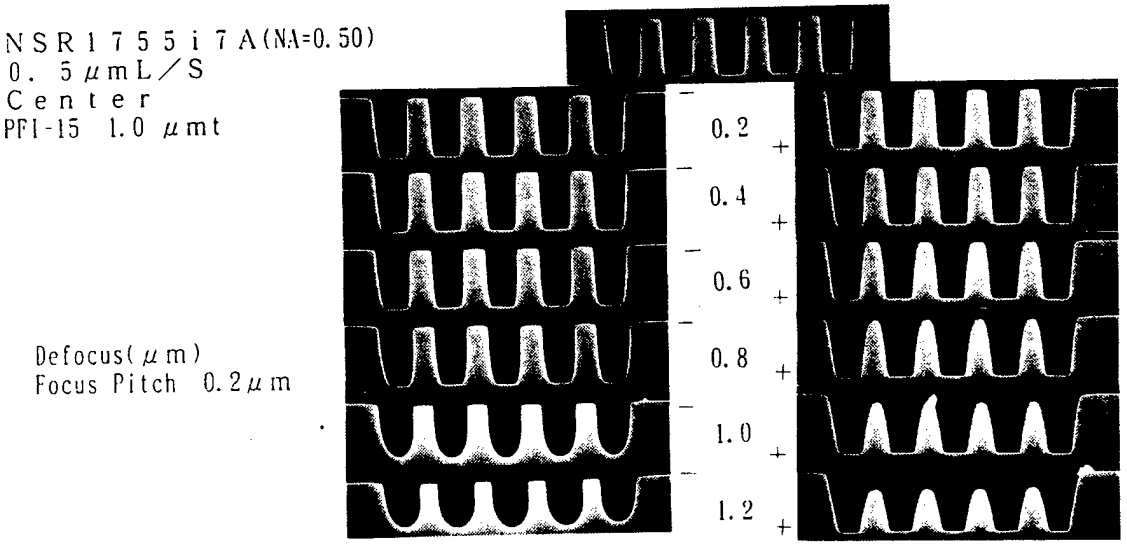
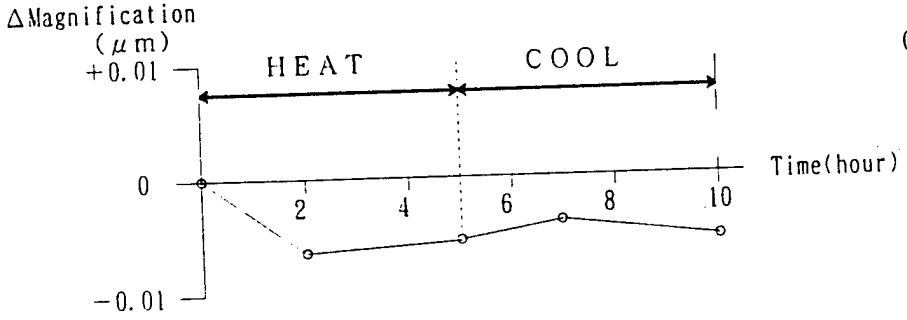


Fig. 2 0.5μmL/S Resist Profiles of Various Defocus



Condition

Body : NSR1755i7A

Lamp Power : 447mW/cm²

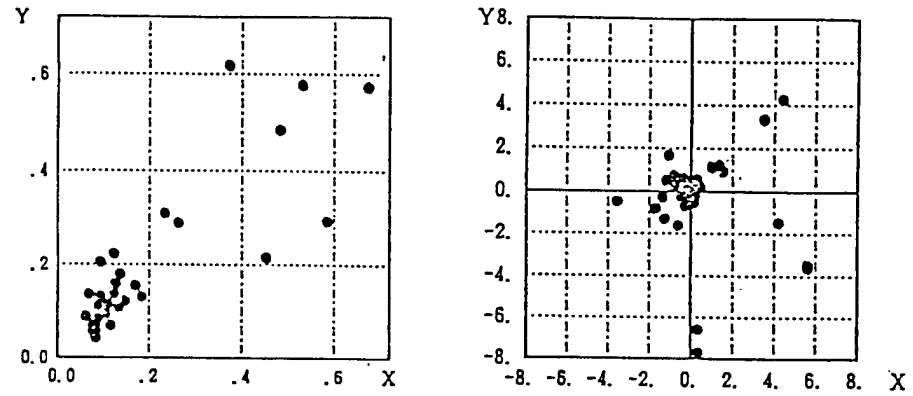
Reticle : Nikon Test Reticle

Shutter OPEN/CLOSE Time

: 2000/100(msec/msec)

Fig. 3 Magnification Stability

LSA Alignment Result



FIA Alignment Result

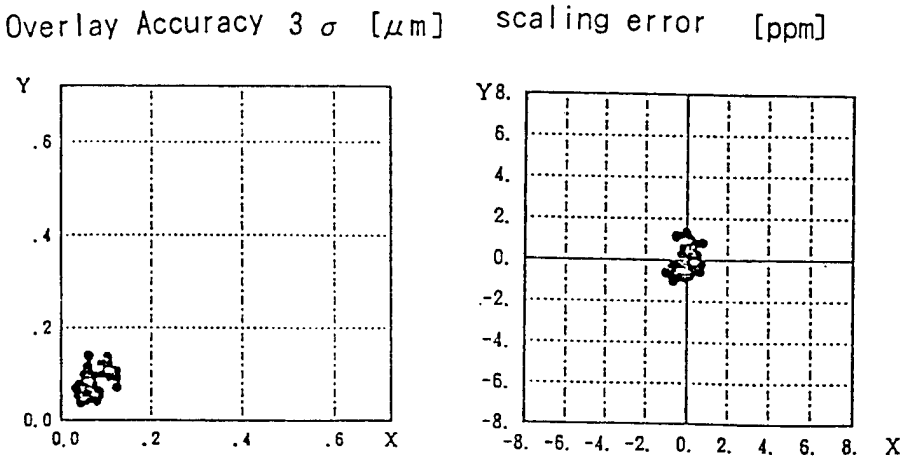


Fig. 4 Overlay Comparison of LSA & FIA on Al Layers

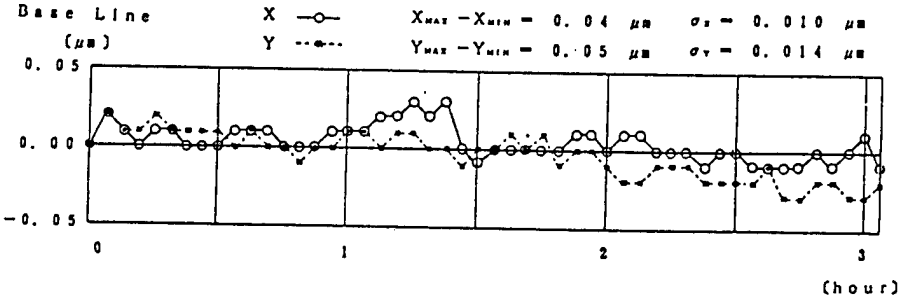


Fig. 5 Baseline Stability of FIA

LIA Optics

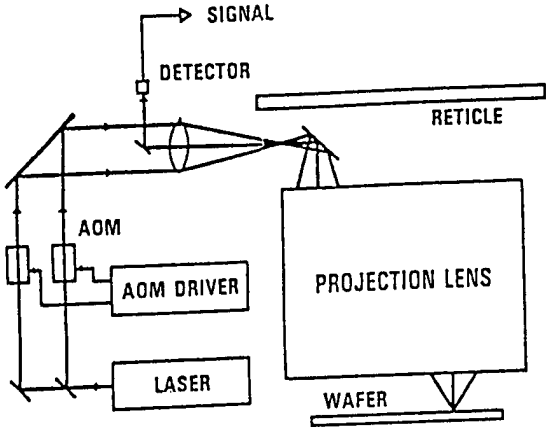
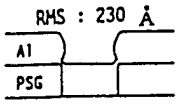
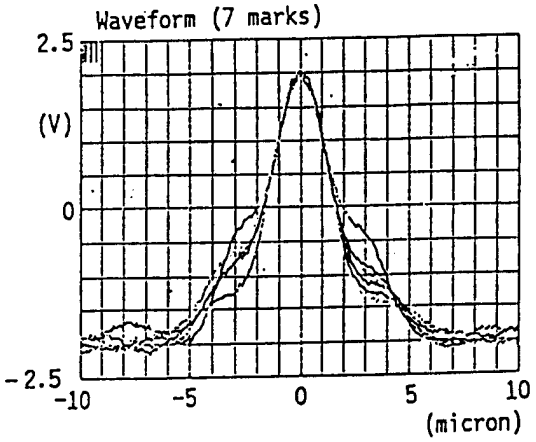


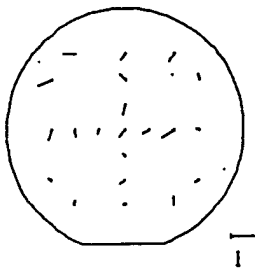
Fig. 6 LIA Optics

LSA Alignment Result





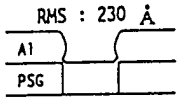
Overlay accuracy (D/D)



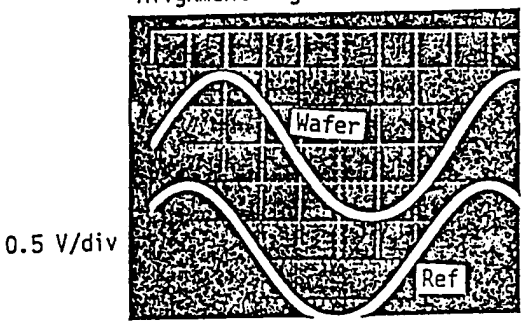
3σ
X : 0.242 (μm)
Y : 0.301 (μm)

1 μm

LIA Alignment Result

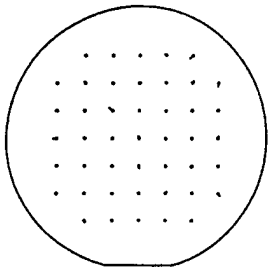


Alignment signal



Overlay accuracy (D/D)

3σ
X : 0.090 (μm)
Y : 0.101 (μm)



1 μm

Fig. 7 Overlay Comparison of LSA & LIA on Al Layer

EXCIMER LASER LITHOGRAPHY

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1 INTRODUCTION

Photolithography maintains an indisputable position as a fine patterning technology of LSIs. The optical system has been changed from contact printing, through reflective optical system, to refractive optical system. The integration of memory devices proceeds stedily as if there may be no termination. The design rule of halfmicron or sub-halfmicron will be necessary in near future for advanced devices. The most effective means for improving resolution is the use of short wavelength light, so the excimer laser has been studied as the light source for the next generation lithography.

However, a strong absorbance of resist materials at DUV region prevents to obtain thick and vertical pattern profiles with the present material systems. Much efforts have been made to overcome this barrier. Chemical amplification system, which utilizes the different mechanism from the conventional resist, support the recent rapid progress in DUV resist. Some promissing materials are reported and encourages us the realization of excimer laser lithography.

In this paper, the trend of resist technology is reviewed, and the present level of fine patterning is elucidated, along with the perspective of realization of excimer laser lithography.

2 EXPOSURE TOOL

The exposure tool of the refractive optical system is called "Stepper" which uses g-line(436nm) of high pressure mercury lamp as the exposure light source. The resolution is expressed as the function of lens NA and exposure light wavelength. One of the effective way to increase the resolution is to use high NA lens, which has progressed stedily and the lens with NA larger than 0.5 can be available at present. On the contrary, the increase in NA results in the decrease in the depth of focus(DOF). Accordingly, the other way of shortening of exposure light wavelength should be intended simultaneously. From this viewpoint, i-line stepper (365nm) has been developed and introduced into the LSI fabrication line. The increase in resolution will be estimated abou 20% in case of i-line stepper. Excimer laser has been also remarked as a new light source of photolithography, and was used to contact printing[1.2], or reflective optical system[3,4], but the present concern is in the refractive optical system. KrF(248nm) is exclusively studied because of its high efficiency, long life-time, and relative easiness of material design. In this case, the increase in resolution will be estimated about 70%. There are two lens systems in refractive optical system, achromatic lens with a raw KrF excimer laser[5] and all quartz chromatic lens with a spectrally line-narrowed KrF excimer laser[6,7]. Now, the latter is the main object of practical excimer laser stepper because of the difficulty in manufacturing a large field size achromatic lens. Recently, KrF excimer laser stepper has become commercially available, which will accelarate the development and realization of KrF excimer laser lithography. The block diagram and specifications of KrF excimer laser stepper are shown in Fig.1 and Table 1, respectively.

3 RESIST

The novolac type resist based on the novolac resin and diazonaphtoquinone photoactive compound is widely used in LSI fabrication. The optimization of novolac structure[8], esterification ratio[9],etc., has satisfied the resist properties required for fine patterning. However, the optical property of this material system is unfaborable for DUV exposure due to the strong absorbance, as shown in Fig.2. The difference of incident light between the top and the bottom of the resist film is very large, which makes it impossible to obtain a high aspect ratio vertical profile. SEM micrographs of 0.5 micron L/S are compared in Fig.3, where (a) is obtained with i-line stepper, and (b) is obtained with KrF excimer laser stepper. In the latter case, large loss of film thickness(from 1.0 to 0.7 micron) and the resultant triangular profile means that the novolac type resist is not practical to KrF excimer laser lithography. Thus, the resist material is the key point of realization of KrF excimer laser lithography. Some approach of resist technology is described in the following sections.

3-1 Development of new resists

New sensitizers replacing DNQ are reported. Four examples, meldrum's diazo[10], o-nitrobenzyl ester[11], diazodimedon[12], and 3-diazo-2,4-dione compounds[13], are illustrated in Fig.4. Investigation of the base polymer of higher transparency at 248 nm is also carried out. The copolymers of styrene-maleic acid, maleimide-styrene[14], vinylphenol-MMA, vinylphenol-AN,etc., are studied. The point is how to reduce the absorbance at 248 nm with keeping the inhibition effect of sensitizers and without losing the RIE resistance.

Some negative resists are also reported and three examples of sensitizers, bisazide, 1,3-dioxin-4-one derivative, and halogenated triazine, are illustrated in Fig.5. Polyvinylphenol is used as the base polymer in the above three examples.

Silicon-containing resist has been developed in order to simplify the tri-level resist system[18]. For KrF excimer laser, p-hydroxybenzylsilsesquioxane[19], polyvinylphenysilsesquioxane[20], polysiloxane with phenol moiety[21], acetylated poly(phenylsilsesquioxane)[22],etc. are developed.

3-2 Application of novolac type resist

The overall properties of the resists above described do not reach the device fabrication level in comparison with i-line lithography. The properties will be improved day by day, but it is difficult for a new material to get reliability of production line in a short term. Therefore, the application of the reliable novolac type resist is a short cut for realizing KrF excimer laser lithography, though it involves some limitations. The decrease in film thickness is one way to relieve the absorbance problem. In addition, surface modification process such as alkali treatment[23] or REL[24] is effective to improve the resist profile.

Recently, we developed a new process which uses alkali treatment and step development[25], and obtained better profile up to 0.7 micron thickness. The process is named LASER[26]. The process sequence and an example of cross sectional view are shown in Fig.6 and Fig.7, respectively. The application of LASER for a device fabrication is shown in Fig.8. The thickness of the resist depends on the conditions of substrate topography or RIE. The adoption of tri-level resist system will be necessary in some circumstances. Fig.9 shows the pattern obtained by tri-level resist system. The improvement of resist itself is also progressed, and an excellent sample is announced[27]. The users would like to cope with the KrF excimer laser lithography by the novolac type single resist if possible.

3-3 Chemically amplified resist

It becomes clear to satisfy resolution, sensitivity, and RIE resistance with conventional resist is very difficult. One approach to overcome this problem involves the chemical amplification concept, which consists of two steps, i.e., acid generation by exposure and acceralation of catalytic reaction by postexposure bake. The basic idea was presented in 1982[28,29,30]. The further investigation of this resist system is activated recently, and the chemical amplification concept is thought to be the last resort of DUV or EB/X-ray resist. Commercially available SAL-601ER7 of Shipley impresses the actuality of a chemically amplified resist. Acid catalyzed reaction involves deprotection, depolymerization, or crosslinking. Two components system and three components system are proposed. The examples of reaction scheme are illustrated in Fig.10. Postexposure bake is the point of these resists mechanisms. The onium salts[31] or organohalides[32,33] are generally used as the photoacid generators. High sensitivity such as 50 mJ/cm^2 can be easily achieved in most samples. This is very attractive when the throughput of lithography is considered. The pattern profile obtained by a chemically amplified resist (1.2 micron thick) is shown in Fig.11, where 0.3 micron L/S is sharply resolved at the dose of 37 mJ/cm^2. However, the chemical amplification system includes more process factors to be controlled than the conventional resist, so that the contrivance and experience should be necessary to demonstrate the constant resist performance. In addition, unknown factors such as material stability and constituent control still remain. The effort to solve these problems will be owned by resist makers, but it is clear that the chemical amplification system is the most promissing resist for KrF excimer laser lithography at present.

4 Comparison with i-line

The higher the memory devices are integrated, the larger the chip sizes become, which results in the requirement of the large field area of the steppers. It will be difficult to manufacture large and uniform lenses with high NA for i-line steppers. On the other hand, the manufacturing of KrF excimer laser lens is rather advantageous because spectral narrowing technology can be applicable. The i-line steppers have just now being introduced into the production line of 16M dRAM, and also used for the trial of 64M dRAM. In the manufacturing of 64M dRAM, i-line lithography will compete with KrF excimer laser lithography. The feature of 0.4 or 0.35 micron will be needed at that time. Therefore, i-line lithography may be considered to borrow some assisting technology to satisfy the practical resolution. The accelerated recent study of phase shifting mask[34] reveals the situation of the i-line lithography. Accordingly, a turning point of i-line and KrF excimer laser will depend on the degree of completion of phase shifting mask and DUV resist, respectively. The timing is considered to be approximately in 1993.

5 Summary

Either i-line or KrF excimer laser lithography was thought to be the successor of g-line lithography, and they have competed with each other. The contest results in the success of i-line lithography. This is the normal selection from the practical viewpoint because it serves the minor change of lithographic technology. However, we can not expect the long life to i-line lithography so well as g-line lithography. KrF excimer laser lithography should also be provided as soon as possible. A chemically amplified resist will respond to the realization of KrF excimer laser lithography. If the development of DUV resist was faster, KrF excimer laser lithography would be already applied in some place of LSI production. It makes us consider how difficult to develop materials used at short wavelength. In this sense, the combination of i-line or KrF excimer laser stepper and the other technology such as multi-level resist system or phase shifting mask will be high-lighted as the prolongation of each lithography life rather than the realization of ArF excimer laser lithography(193nm).

It goes without saying that the development of ArF excimer laser resist is strongly expected. Henceforth, the photolithography will be asked the responsibility as the practical lithography despite of being cornered to the limitation of its ability.

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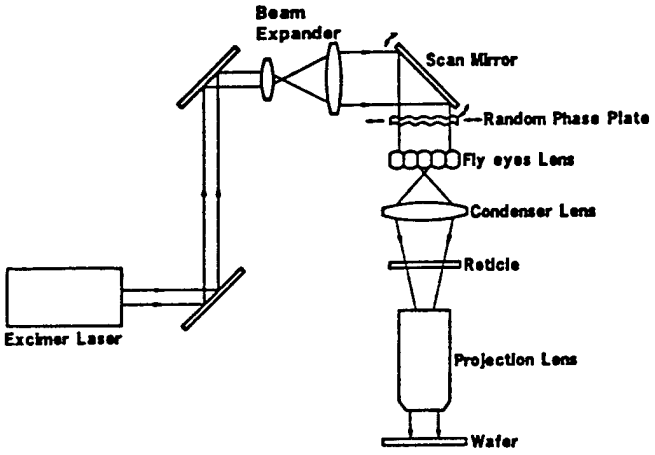


Fig.1 Block diagram of excimer laser stepper

Table 1 Specifications of excimer laser stepper

NA	0.42
Reduction Ratio	5X
Field Size (mm)	21.2φ
	(15.08×18.86)
Distortion (μm)	±0.12
Wavelength (nm)	248.4
Bandwidth (pm)	5(3)
Resolution (μm) (K=0.8)	0.47
Illumination Power at Wafer (mW/cm²)	40
Alignment Precision (3σ, μm)	±0.18 (including X)
Alignment Method	off-axis

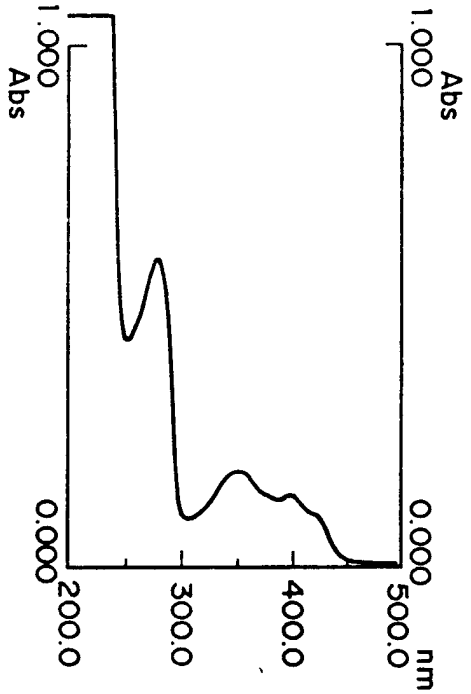
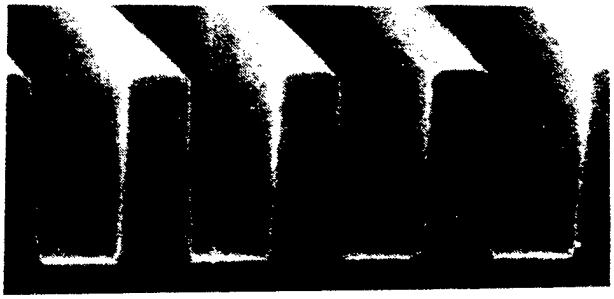


Fig.2 UV spectrum of novolac resist

(a) i-line



(b) KrF excimer laser

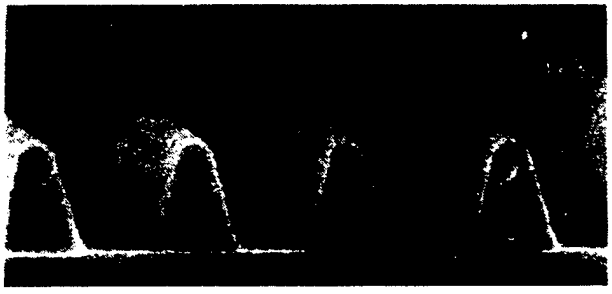
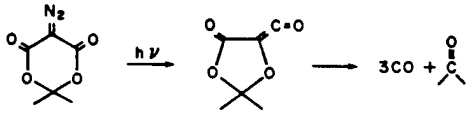
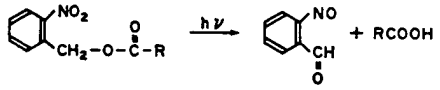


Fig.3 0.5 micron L/S of novolac resists

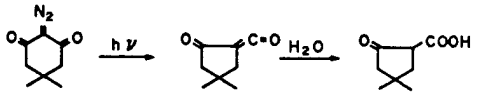
meldrum's diazo



O-nitrobenzyl ester



diazodimedone



3-diazo-2,4-dione

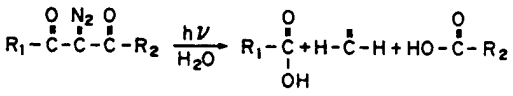
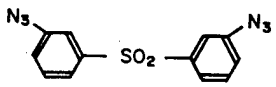
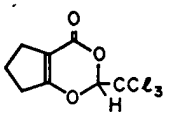


Fig.4 Photochemical reaction of sensitizers

bisazide



1,3-dioxin-4-one



halogen compound

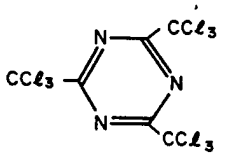


Fig.5 Sensitizers for DUV negative resists

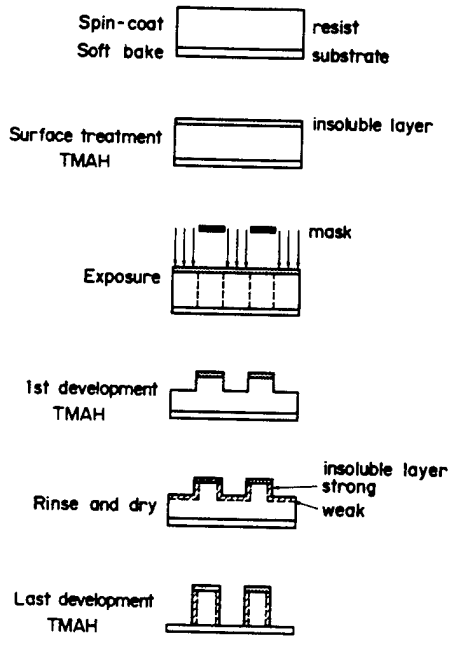


Fig.6 Process sequence of LASER

Fig.7 0.35 micron L/S obtained by LASER

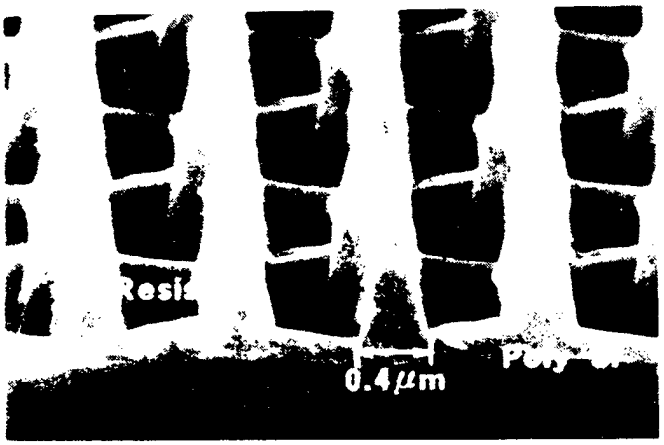


Fig.8 Application of LASER for device fabrication

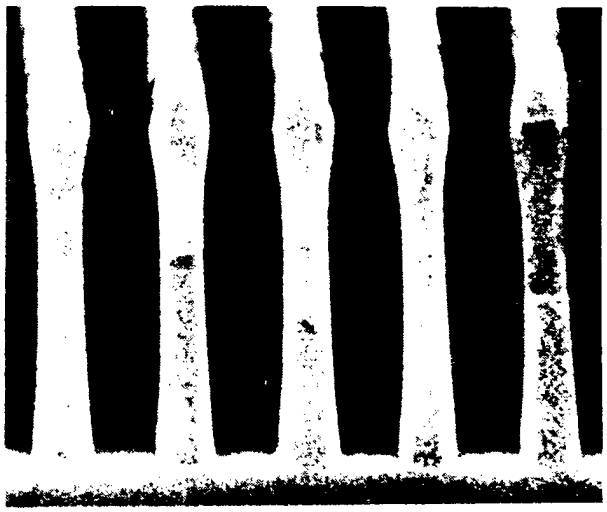
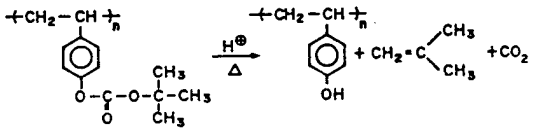
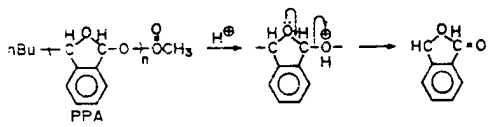


Fig.9 0.3 micron L/S obtained by tri-level resist system

deprotection



depolymerization



crosslinking

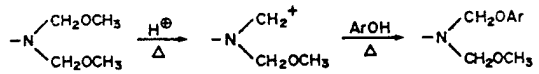


Fig.10 Types of chemical amplification system

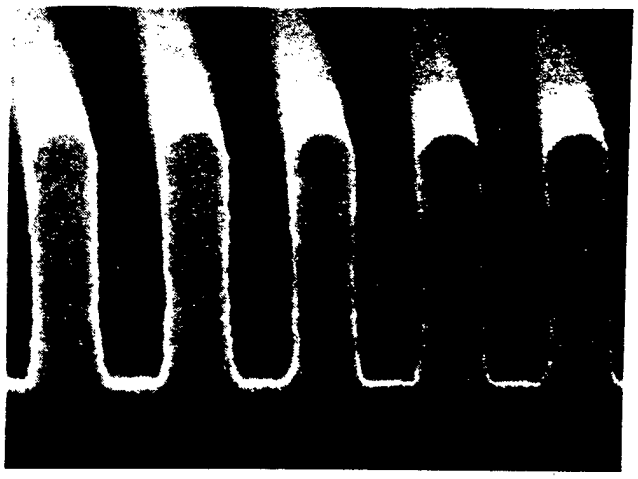


Fig.11 0.3 micron L/S obtained by chemically amplified resist

EXICIMER LASER STEPPER

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1. INTRODUCTION

Fine patterning technology in semiconductor manufacturing has made enormous progress. The two reasons for this progress are the increased numerical aperture (NA) of the reduction lens for g-line lithography and the increased contrast of resists. To achieve further fine patterning , however, the wavelength of the exporsure light needs to be reduced. Indeed, it seems almost certain that through the devlopment of i-line stepper with a wide image field and high-NA, high-contrast i-line resists, i-line lithography will replace the g-line lithography as the main lithography process for the mass production of 16M DRAMs scheduled to start in 1992. To further reduce the wavelength, excimer lithography is regarded as the best candidate as it is going to attain, in a sense, the ultimate optical lithography methods.

But when will excimer lithography replace i-line lithography ? It goes without saying that this will occur when excimer lithograpy can be clearly distinguished from i-line lithography in term of, first, resolution/DOF, and, secound, profitability in terms of cost/chip. Since it is clear that the resolution/DOF of excimer lithography is far better than that of i-line lithography under same conditions, excimer lithography will replace i-line lithography when the cost of the former becomes lower than that of the latter. Of course, when this happens, i-line lithography will try to prevent itself from becoming obsolete by using multi-layer resists, phase shifting mask, and the like. The three major technical items for excimer lithography, namely, the development of resists, the laser, and the stepper exprosure system, have been developed vigorously. Nevertheless, the running costs due to the short life of the laser and the sensitivity of the resists still remain high enough to reduce the profitability of installing excimer lithography in mass production lines.

This paper describes the technical problems of the the stepper exposure system, with main emphasis on raising the profitability of excimer lithography, with reference to resists and laser. The paper also attempts to provide solutions.

2. CONDITIONS FOR THE EXCIMER LITHOGRAPHY TO BE INSTALLED IN MASS PRODUCTION LINES

The minimum conditions for excimer lithography to be installed in the mass production lines for 64M DRAMs are the following four main performance specifications :

①	Resolution	:	0.35 μm
②	Field size	:	20 x 20 mm
③	Throughput	:	50 wafers/hour (for 6-inch wafer,45shots)
④	Life of laser	:	One year (Narrow-band element,Electrodes,etc.)

Table 1 lists the target specifications for the three major technical items required to achieve this performance. For comparison, the specifications of the prototype stepper developed by CANON four years ago are also listed.[1] These target specifications are related. All the main target performance specifications must be satisfied based on the level of accomplishment at the time of installation, taking advantage of the mutual compensation.[2]

For example, it is necessary to increase the NA to improve resolution. To increase the NA, it is necessary to correct the chromatic aberration of the excimer projection lens more exactly. But this requires narrowing the band of the laser, for it is difficult to correct the chromatic aberration of a conventional excimer projection lens made of single glass material. If the band of the laser is narrowed, improvement in the laser output is restricted. To compensate for this, improving the optical efficiency of the stepper becomes a more technical problem.

There are two ways to improve throughput: Improving the laser output and improving the resist sensitivity. Improving the laser output increses the power density entering the optical element of the stepper. This gives the technical problem of coating durability. Improving the resist sensitivity reduces the number of exposure per shot. This makes countermeasures against uneven illumination difficult because they use the smoothing effect by multiplication. At the same time, improving the resist sensitivity adds a technical problem concerning dose control. This is because, although count control has been used here, now the exposure dose per one pulse must be variable.

Table 2 lists the relationships between these performance specifications and the technical problems. As seen from this table, the important technical problems for installing excimer lithography into the mass production lines are optical efficiency, coating durability, illumination uniformity, and dose control. These problems belong to the illumination optical system, and are peculiar to excimer lithography (pulse like, coherent, and DUV light).

3. TECHNICAL PROBLEM OF THE EXCIMER ILLUMINATION OPTICAL SYSTEM

3-1 Optical Efficiency and Illumination Uniformity

Fig.1 shows the factors influencing the optical efficiency and illumination uniformity. Note that the illumination uniformity is dependent on the characteristics of the excimer laser. The illumination uniformity is disturbed by random unevenness in the asymmetric beam profile, or by the speckles and fringes caused by the comparatively higher spatial coherence of the excimer laser than that of the light source of the g-line or i-line. A speckle is a random interferance pattern caused by particles in the light path or by the diffuser plate. A fringe is a periodic interferance pattern caused when the integrator divides the wavefront of the laser beam and overlaps them. This unevenness in illumination are technical problems peculiar to the excimer illumination optical system which are receiving the full attention of all stepper manufactures.

Table 3 lists the three types of smoothing methods to eliminate uniformity unevenness. Shifting is a parallel move of the laser beam pulse by pulse, and is effective in reducing all the uneven illumination uniformity mentioned above. But it necessarily increases the number of exposure pulse per shot. Although the effect becomes much greater when the moving amount s is enlarged, it also decreases the optical efficiency. Rocking is a method to deflect the laser beam pulse by pulse. For higher effect, the number of exposure pulses must be increased. However, it has no effect on uneven illumination caused by beam profile. Integrating uses an integrator such as fly's eye lens or optical rod, and becomes more effective when the number of divisions n is increased. And it takes no more than one pulse to smooth the unevenness. But increasing the number of divisions involves increasing the fringes. Table 4 shows the relationships between them. The figures in the upper half represent the uneven uniformity due to beam profile ranging over all the illumination area. The lower half shows the uneven uniformity due to fringes, whose period is several ten of μ ms.

Each method has its merits and demerits. It is necessary to use the three smoothing methods at one time to optimize each parameter in designing the illumination optical system with fewer exposure pulses, high optical efficiency, and more even illumination.

3-2 Coating Durability

When the excimer stepper has been used for long time, the illumination of the image plane may decrease. This is mostly because the change of the characteristics of the optical coating reduces the transmission and the reflection. From experience with the prototype stepper, we may identify the following two causes of this change in characteristics:

① Some product of a photochemical reaction from molecules floating in the air is deposited on surface of the optical coating.

② The optical coating is damaged and the refractive indexes of the materials change.

A countermeasure for ① is to place the optical components in an atmosphere of some inert gas such as N_2 gas. For this purpose, materials and surface treatment for the cover and the lens barrel of the optical components should be selected to prevent gas generation.

A countermeasure for ② is to take special care in the design stage to minimize the power density of the light entering the optical coating. Other measure includes optimizing the coating composition and improving the control of the coating process, including treatment of the substrate.

3-3 Dose Control

If the number of exposure pulses per shot is reduced, the exposure energy must be varied quickly in the last several pulses. To accomplish this, there are several methods: One is to change the laser output itself, while another is to use the AO element. Others are to mount several types of ND filter to rotating disc, and to use the angle characteristics of the transmission of optical coating, etc. One or more of them should be used according to the dynamic range, response, and durability.

4. EXCIMER ILLUMINATION OPTICAL SYSTEM FOR MASS PRODUCTION.

Fig.2 is a sketch of CANON's new excimer illumination optical system for mass production, developed considering the items mentioned above. Its main features are as follows:

① It is desirable that the distribution of the optical intensity in a fly's eye integrator is rotationally symmetric to reduce uneven illumination and effective source distortion. This new illumination optical system can form the rotationally symmetric distribution of the light intensity without loss of energy even if its form is not symmetric. This is done by dividing the amplitude of the laser beam into four and rotating the beam before it enters the the fly's eye integrator.

② The number of the fly's eye lenses into which single laser beam can enter is restricted according to the spatial coherence of them. But the number of beam can be multiplied because it is divided into four. This takes better effect on smoothing. And the four beams can cancel the fringes produced by each laser beam at one pulse because they enter the

fly's eye integrator from different angles.

③ This illumination optical system is separeted into two blocks, which are mounted on the stepper side and on the laser side. The driving unit for smoothing and controlling the exposure dose is mounted on the laser side to reduce the negative influence of vibration from the driving unit on image performance and alignment accuracy.

④ Corresponding to the phase shifting mask and such like, this system can be easily varies the value σ , from 0.3 to 0.7 , with low deterioration of illumination.

5. SUMMARY

The age of the KrF excimer stepper is near at hand. The resist, laser, and the stepper have been developed to attain the level suited to mass-production while compensating for each other's shortcoming. Though alignment technology is not treated in this paper, it has been steadily making progress on the basis of valuable experience in the g-line or i-line lithography. Although no more major obstacles are visible, a more highly sophisticated excimer stepper is necessary to move smoothly from i-line to excimer lithography. For that purpose, the most important thing is a correlation of the component technologies as well as an improvement in each technology.

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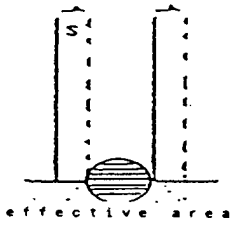
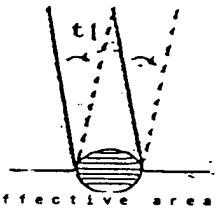
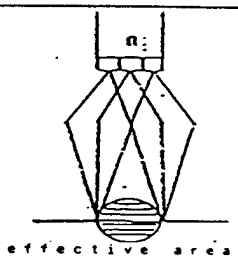
Table 1. Specification (Target)

Items	Specification		unit
	Target	FPA4500	
[Stepper]			
NA	0.45	0.37	
Image field	20 x 20	15 x 15	mm
Uniformity of Illumination	± 1.5	± 5.0	%
Dose control	± 1.5	± 3.5	%
Optical efficiency	25.0	2.8	%
Number of exposure pulses	50	100	pulses
[Laser]			
Wavelength	248.3	248.3	nm
FWHM	2.0	3.0	pm
Wavelength drift	± 0.5	± 1.0	pm
Power	5.0	3.0	W
Pulse energy	12.5	15.0	mj
Repetition rate	400	200	Hz
Parts life time	10^9	6×10^8	pulses
Gas life time	2×10^8	5×10^8	pulses
[Resist]			
Sensitivity	25		mj/cm^2

Table 2. Improvement of stepper

Main performance				Improvement of stepper
[Resolution]	Stepper (NA)	Laser (FWHM)	Laser (Power)	⇨ Optical efficiency
[Throughput]	Laser (Power)			⇨ Durability of coating
	Resist (sensitivity)	Stepper (Number of exposure pulses)		⇨ Uniformity Dose control
				⇨ Optical efficiency
[Durability of laser]	Laser (Power)			⇨ Optical efficiency
	Resist (sensitivity)	Stepper (Number of exposure pulses)		⇨ Uniformity Dose control

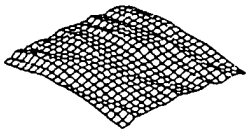
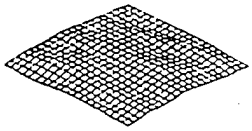
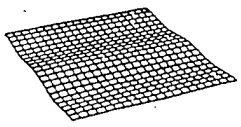
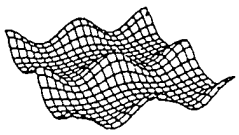
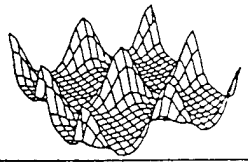
Table 3. Methods of smoothing

Methods of smoothing		Shifting	Rocking	Integrating
				
Parameters		s . pulse	t . pulse	n
Uniformity	Beam profile	○	–	○
	Speckle	○	○	○
	Fringe	○	○	×
Optical eff.		×	–	–

× ⇨ ○ worse ⇨ better

○ , × : depend on parameter.
– : not depend on parameter.

Table 4. Uniformity by integrator

Num. of divisions	4 (2 x 2)	9 (3 x 3)	16 (4 x 4)
Beam profile			
(Uniformity)	19.0 %	5.5 %	3.1 %
Fringe			
(Uniformity)	2.5 %	14.9 %	26.8 %

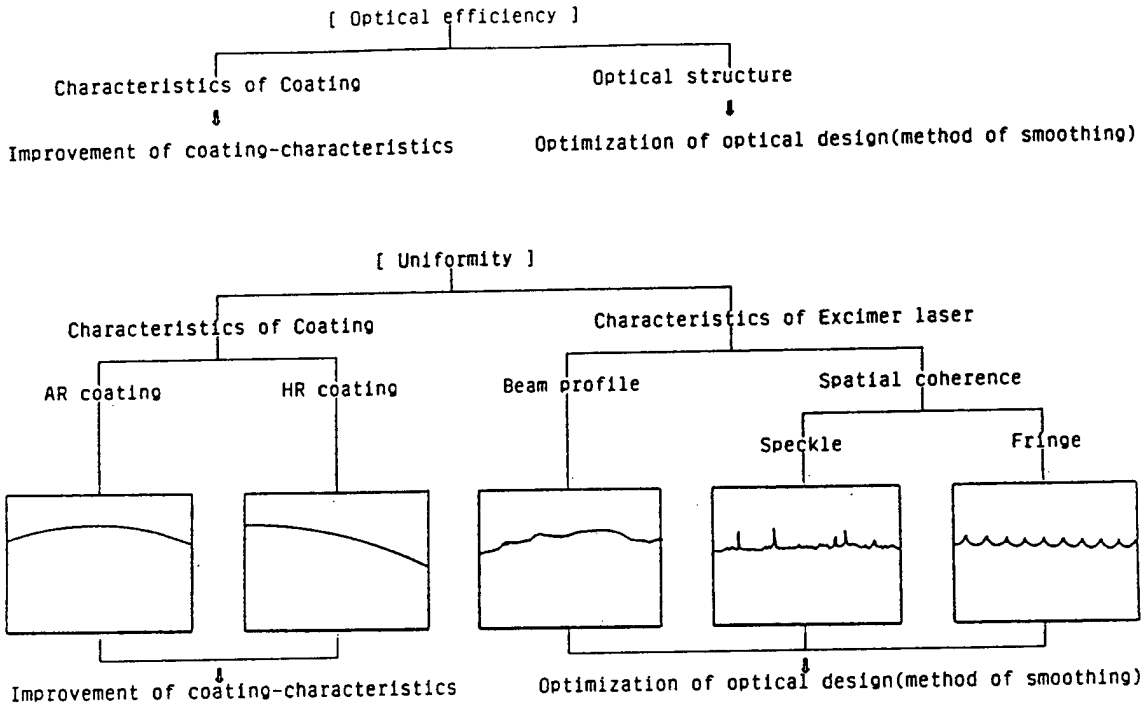


Fig.1 Optical efficiency and Uniformity.

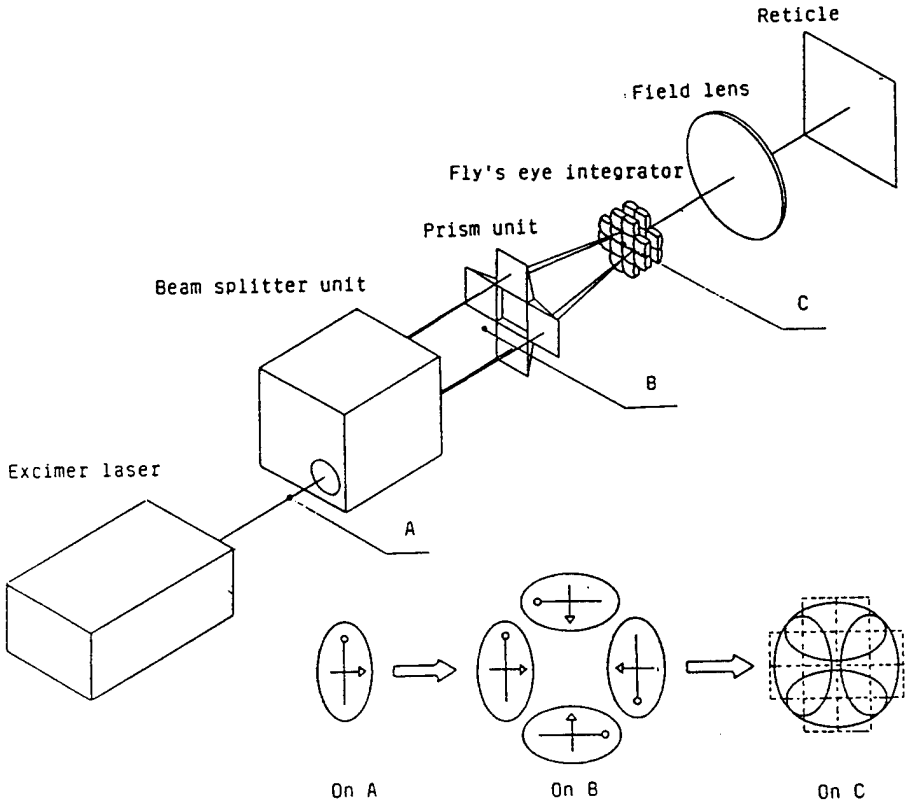


Fig.2 Schematic diagram of illumination system

PHASE-SHIFTING MASK AND FLEX METHOD FOR ADVANCED PHOTO-LITHOGRAPHY

- Approaches to 0.2 μm photo-lithography -

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1. Introduction

The basic approach to improving the resolution limit of optical lithography is to use a higher numerical aperture (NA) optics and a shorter exposure wavelength.[1,2] However, this rapidly decreases the depth of focus (DOF). For LSI processes, a certain DOF (usually ± 0.75 μm $\sim \pm 1$ μm) is required to delineate fine patterns on LSI substrates because of large topography and astigmatisms of projection lenses. Consequently, this basic approach to improving resolution can no longer be a good guideline.[3]

This paper discusses the phase-shifting method[4,5] and the FLEX method[6] as new approaches for overcoming the limitation in photo-lithography.[7]

2. Limitation of conventional photo-lithography

In photo-lithography, the resolution limit and the corresponding DOF are usually described by Rayleigh's equations. When Rayleigh's DOF becomes smaller than the focus tolerance required in actual LSI production lines, a new expression for the practical resolution limit becomes necessary.

Figure 1 shows the schematic relation between the pattern feature size and DOF. The DOF decreases with shrinking pattern size for even the same optics. Thus, the practical resolution limit is given by the minimum feature size satisfying the required DOF. This is shown by point A in Fig.1.

The NA dependences of the practical resolution defined above are shown in Fig.2 for various exposure wavelengths and required DOF. Here, calculations are made for line and space (L/S) patterns, and it is assumed that the image contrast must be larger than 70% for pattern delineation. On the best focus plane, the resolution limit is given by Rayleigh's equation. However, as the required DOF increases, the practical resolution deviates from Rayleigh's equation.

Deviation from Rayleigh's equation begins at a smaller NA for a shorter λ. That is, a high NA lens becomes less effective as λ becomes shorter. Reduction in the required DOF greatly improves the practical resolution in the high NA region. However, it is generally difficult to reduce it to less than ± 0.5 μm. Consequently, a high NA - short λ optical system is not effective and may even be harmful in the conventional method.

To overcome this problem, new innovative approaches are necessary. The phase-shifting method and the FLEX method will be discussed as new approaches in the next section.

3. Phase-shifting method

The principle of the phase-shifting method is shown in Fig.3. If this method is applied to L/S patterns by alternately introducing phase differences as shown in Fig.3, the spatial frequency response can almost be doubled. As shown in this figure, 0.17 μm patterns were actually delineated. In this experiment, a KrF excimer laser stepper with 0.42 NA and 0.3 σ (Nikon) and chemically amplified resist SAL601 (Shipley) were used.

The NA dependences of the practical resolution (L/S patterns) with and without the phase-shifting method are shown in Fig.4(a) for various exposure wavelengths. The dashed lines represent the conventional method, and the solid lines represent the phase-shifting method. It is assumed that the image contrast must be larger than 70% over a +0.75 μm focal range, and that the coherence factor σ is 0.5 for the conventional method and 0.2 for the phase-shifting method.

Because of the improved spatial frequency response, the practical resolution is improved by the phase-shifting method over the whole range of practical NA, as shown in Fig.4. Moreover, by using the phase-shifting method, we can suppress the deviation from Rayleigh's equation. This means that the phase-shifting method makes the DOF large. Consequently, high NA - short λ optics can be effectively used with the phase-shifting method.

The coherence factor greatly affects the optical images in the phase-shifting method. Figure 4(b) shows the NA dependences of the practical resolution of L/S patterns for various coherence factors σ in the phase-shifting method. The effectiveness of the phase-shifting method increases greatly with decreasing coherence factor.

The phase-shifting method, however, is not always effective. It is not effective on isolated patterns, such as contact hole patterns. In such cases, the FLEX method is more effective.

4. FLEX method

Figure 5 shows the principle of the FLEX method. Plural image planes are created at different focal levels along the light axis. By using of this exposure concept, the DOF increases drastically. The FLEX method is most effective for isolated transparent patterns like contact holes. This is because the effect of a defocused image which is superposed to a sharply focused image, is negligible for this kind pattern. In this method, the distance between plural image planes must be optimized according to optical system parameters and/or patterns.

The NA dependences of a practical resolution (hole patterns) with and without the FLEX method are shown in Fig.6 for various λ. The dashed lines represent the conventional method, and the solid lines represent the FLEX method.

In the conventional method, the practical resolution of hole patterns deviates from Rayleigh's equation, and the deviation from Rayleigh's equation begins at a smaller NA for a shorter λ. This is the same as for L/S patterns. On the other hand, with the FLEX method, the practical resolution corresponds to Rayleigh's equation itself. As a result, high NA - short λ optics can be effectively used by the FLEX method.

5. Approaches to below 0.2 μm

Finally, approaches to below 0.2 μm by projection photo-lithography are discussed. Figure 7 shows again the NA dependences of the practical resolution for i-line, KrF excimer laser, and SOR X-ray light (λ=15 nm). Results using the phase-shifting method and the FLEX method are also shown for i-line and KrF cases. Required DOF of ±0.5μm was assumed. This figure shows the following two approaches to realizing below 0.2 μm.

One approach is to shorten wavelength with decreasing NA to maintain the required DOF. This would require a very short wavelength of SOR X-ray light.[8] The other approach is to use the phase-shifting and FLEX methods. Here, various technologies we have already developed could be used, such as, resist materials and processes, mask technologies, and exposure equipment (steppers).

6. Conclusion

In conventional photo-lithography, the practical resolution is not improved, and may even be degraded by increasing NA and shortening wavelength. This means that the high resolution

capability of future advanced optical systems cannot be effectively used in actual ULSI production lines. With the phase-shifting method and the FLEX method, it is possible to overcome this limitation in conventional photo-lithography. Using these advanced techniques, we can delineate patterns in the range of 0.15 $\sim$ 0.3 μm using KrF or i-line steppers with sufficient focus latitudes.

Acknowledgments

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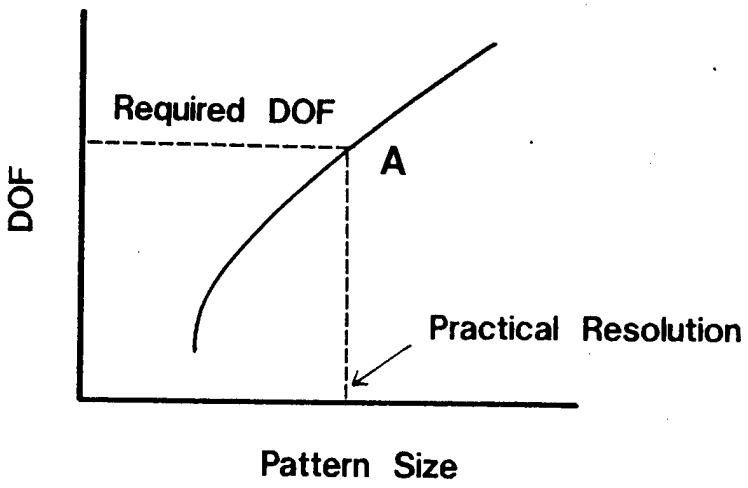

Fig.1 Schematic relation between pattern size and depth of focus

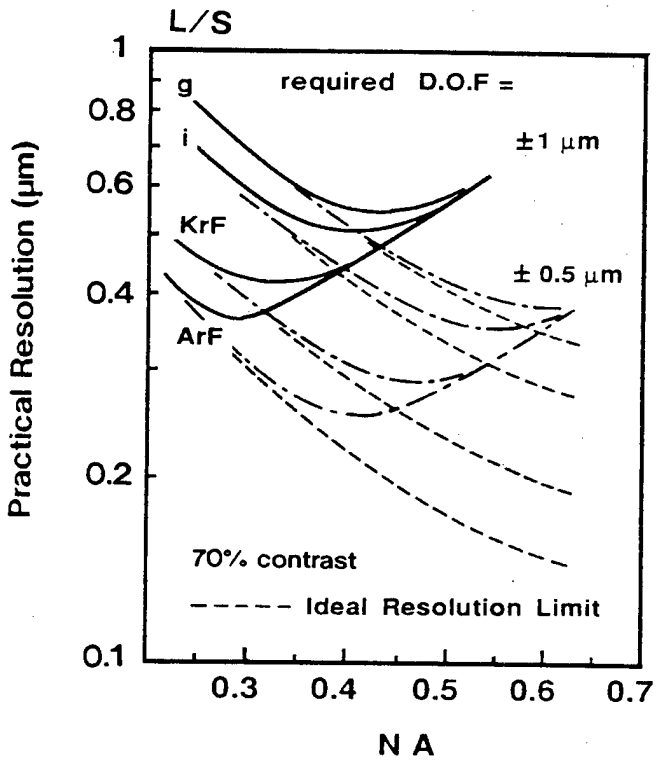

Fig.2 NA dependence of practical resolution for various wavelength and required DOF

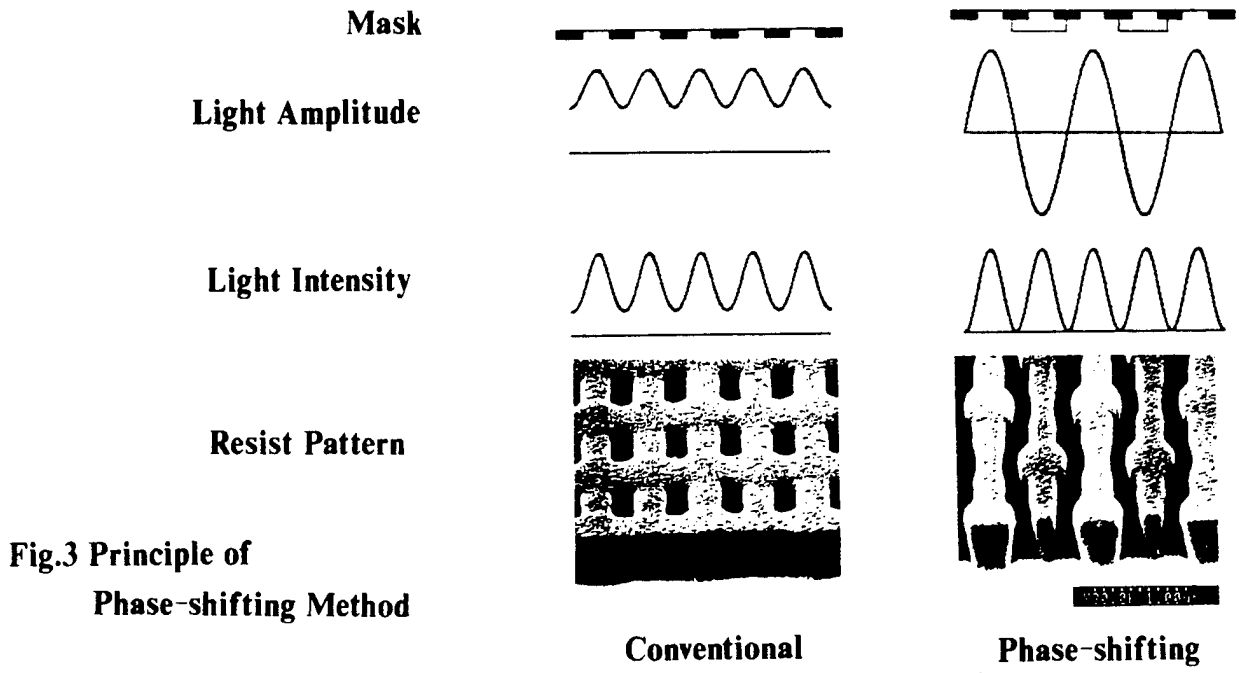

Fig.3 Principle of
Phase-shifting Method

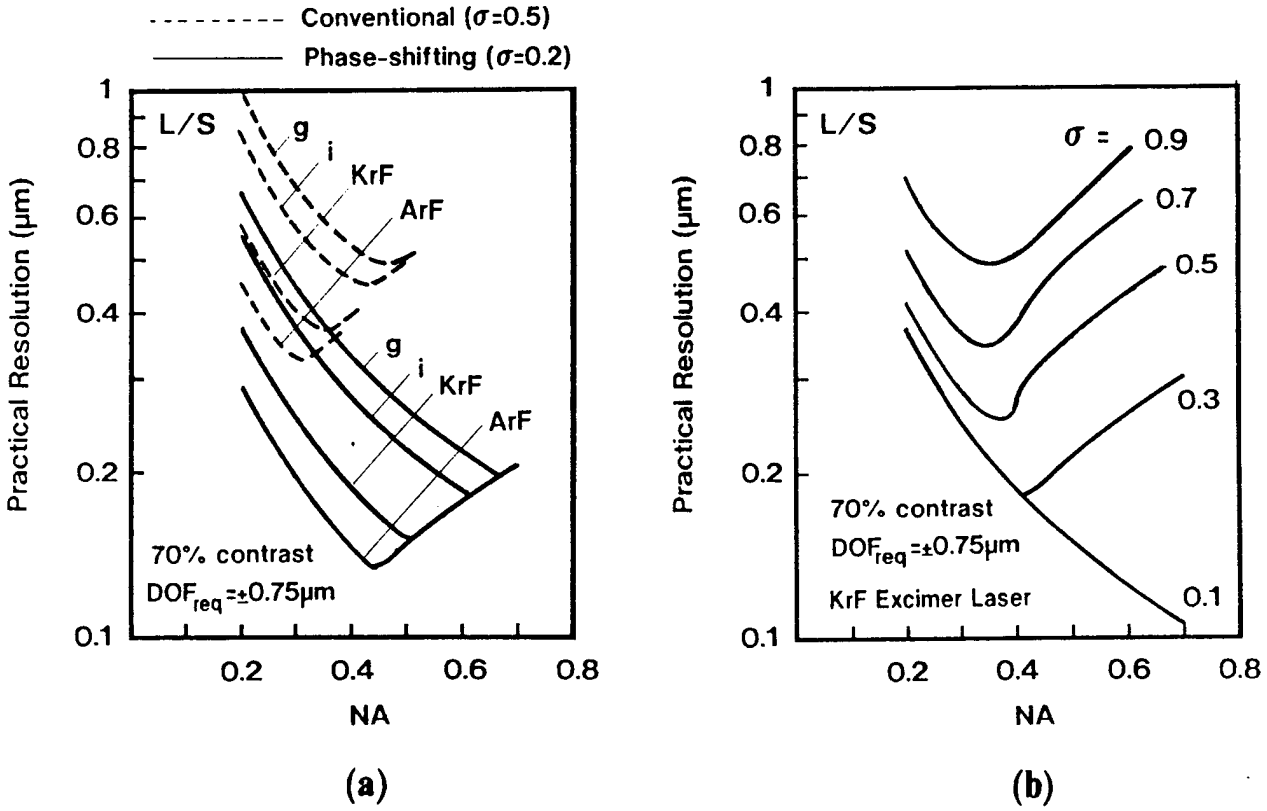

Fig.4 NA dependence of practical resolution in phase-shifting method
(a) for various wavelengths and (b) for various coherence factors

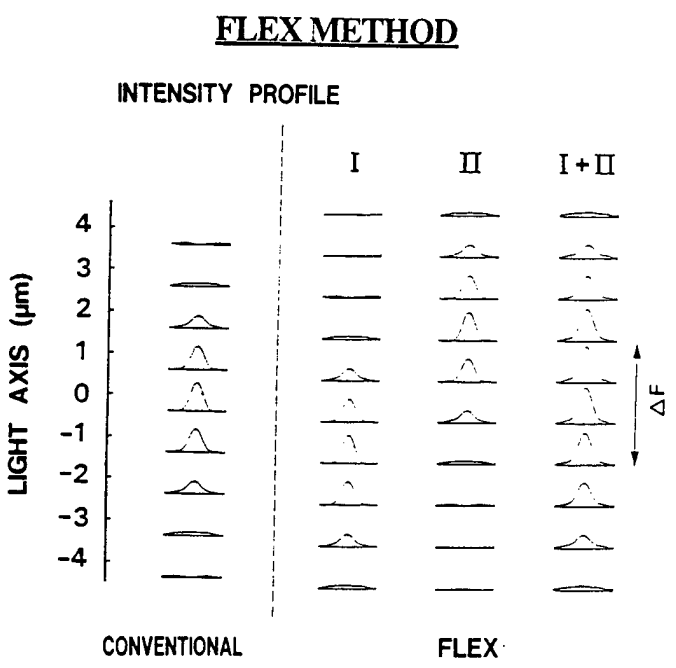

Fig.5 Principle of FLEX

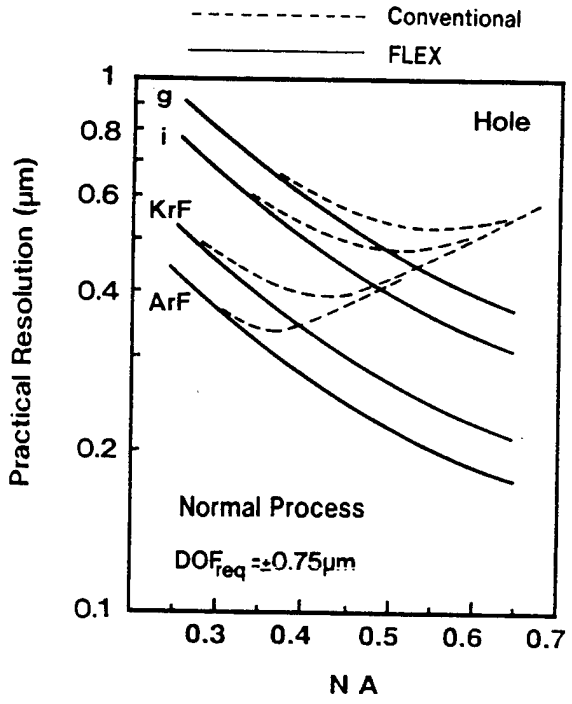

Fig.6 NA dependence of practical resolution in FLEX

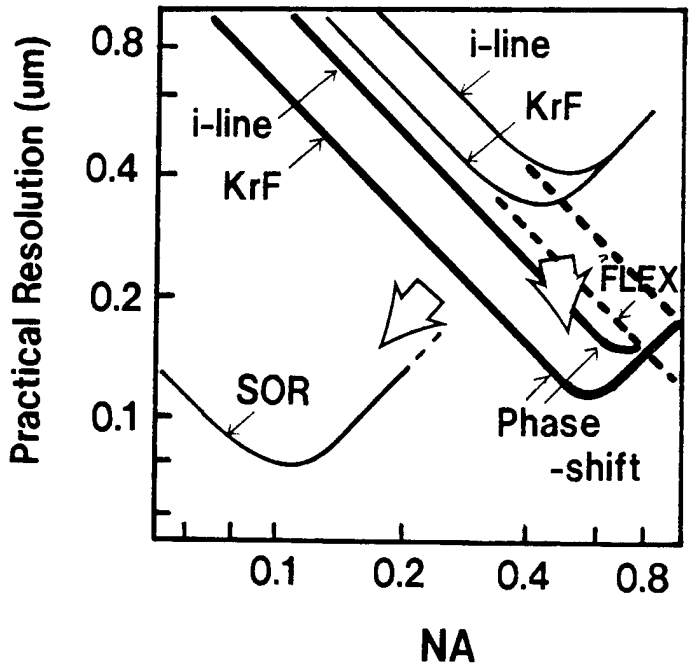

Fig.7 Approaches to below 0.2um by optical lithography
Required DOF = ± 0.5μm

X-ray lithography

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1. Introduction

X-ray lithography is expected to be the process technology for manufacturing future VLSIs. However, there are many problems which must be resolved to put x-ray lithography to practical use in VLSI device fabrication. In this paper, x-ray lithography technology for DRAM devices will be discussed. First, x-ray mask with W-Ti absorber[1] and fabrication of 1-Mbit DRAM using x-ray lithography[2] will be described as a previous works for DRAM fabrication. Next, the approach for 256-Mbit DRAM will be shown.

2. Low distortion x-ray mask with W-Ti absorber

An x-ray mask consists of a membrane (1~5μm thickness) with a low absorption coefficient and an absorber (0.3~1μm thickness) with a high absorption coefficient. The accuracy of the x-ray mask mainly depends on the stress of the absorber material. Therefore, in order to obtain a low distortion x-ray mask, the absorber material with small stress must be found. The properties of W-Ti alloy has been evaluated as an x-ray mask absorber[1]. In this section, the results will be described.

The W-Ti films were deposited by sputtering W-Ti target of 1 wt% Ti content with Ar or Ar+N_2 gas. The W film was also deposited for comparison. Figure 1 shows the dependence of internal stress of W and W-Ti films on the sputtering gas pressure and the constitution of sputtering gas. As shown in Fig.1, the internal stress of W and W-Ti changes with increase in the sputtering gas pressure. The stress of W-Ti film deposited using Ar+N_2 of 30% N_2 content decreased with increase in the gas pressure from a very large compressive stress, and reached low stress (0.5~ 2.0 $\times$ $10^7 N/m^2$) at the pressure region of above 2Pa. It is seen that stress control is very easy by applying Ar+N_2 (30%) gas to the sputtering process in W-Ti film formation. The density of the low stress W-Ti film is about 14 to 16g/cm^2 . The dry etching properties of W-Ti film for CF_4 +O_2 gas plasma were investigated. The etching rate of W-Ti film becomes the maximum (150nm/min.) at 15-20% O_2 content. This etching rate indicated that the patterning of W-Ti film by reactive ion etching is very easy. As a result, it can be said that W-Ti film is effective as a superior x-ray mask absorber.

In order to demonstrate the superior properties of W-Ti film, W-Ti x-ray masks were fabricated using a 3"-diameter mask blank with SiN/Polyimide membrane. This mask comprises two chips of 1-Mbit DRAM. Figure 2 and 3 show the photograph of the fabricated x-ray mask and the SEM photograph of W-Ti absorber patterns, respectively. Figure 4 shows the W-Ti mask distortion which was measured with Nikon LAMPAS 2I. As shown in Fig.4, the maximum pattern placement error of the W-Ti x-ray mask is less than 0.1 μm, which is satisfactory for fabrication of 1-Mbit DRAM.

3. Fabrication of 1-Mbit DRAMs by using x-ray lithography

In order to demonstrate that x-ray lithography technology has the potential for use in VLSI fabrication, 1-Mbit DRAMs were fabricated by using x-ray lithography[2]. In this section, the results will be described.

3-1. X-ray lithography for 1-Mbit DRAM

In the fabrication of 1-Mbit DRAM, the x-ray stepper SX-5, x-ray resist XPB and the W-Ti x-ray mask mentioned in the previous section were used.

The x-ray stepper SX-5 was developed for laboratory use, and to achieve high resolution for the next-generation VLSI with half-micron linewidth. Therefore, the mask-to-wafer proximity gap is held very narrow (15μm) during the exposure in order to reduce the penumbra. The specifications of SX-5 are summarized in Table 1. Figure 5 shows a photograph of the x-ray stepper SX-5 placed in a super-clean room.

X-ray resist XPB is novolak-based positive resist which consists of poly (2-methyl-1-penten sulfone) and cresol novolak resin. The dry etch resistance of XPB is as high as that of positive photoresists currently used such as OFPR-800. Figure 6 shows the sensitivity curves of XPB, EBR-9HS and CPMS[3] for Pd L_α radiation. The sensitivity of CPMS and EBR-9HS was also evaluated for comparison. As shown in Fig.6, although the sensitivity of XPB is lower than that of CPMS, it is similar to that of EBR-9HS which is one of the most sensitive positive resists. The contrast of XPB is higher than EBR-9HS. As a result, it can be said that XPB has high performance as an x-ray resist.

3-2. Fabrication results of 1-Mbit DRAM

X-ray lithography was applied to the contact hole process which is one of the most critical processes for 1-Mbit DRAMs. Figure 7 shows a photograph of a chip fabricated by x-ray lithography. The chip layout is composed of two 1-Mbit DRAMs and TEG (Test Element Group) chips. Figure 8 shows an SEM photograph of the contact holes (SiO_2) which were formed by using XPB as an etching mask. It can be seen that excellent contact-hole patterns were obtained by using X-ray lithography. Figure 9 shows the histogram of overlay error in the contact hole process. As shown in Fig.9, it seems that the alignment accuracy of x-ray lithography is a 3σ of less than 0.15μm for both the X and Y directions. This accuracy is satisfactory for 1-Mbit DRAM fabrication. It can be said that the excellent alignment accuracy is due to the combination of the highly accurate alignment system and the low-distortion x-ray mask with W-Ti absorber.

Figure 10 shows the bit yield for 1M bits. Although full-functional 1-Mbit DRAMs were not found, a maximum bit yield of 99.5% was obtained. Table 2 shows the results of the characteristic test. The 1-Mbit DRAMs fabricated by using photolithography for all the processes were also evaluated for comparison. As shown in Table 2, 1-Mbit DRAMs fabricated by x-ray lithography and those fabricated by photolithography had the same characteristics. It is demonstrated that x-ray lithography technology has the capability for fabrication of 1-Mbit DRAM.

4. X-ray lithography for 256-Mbit DRAM

Lithography for 256-Mbit DRAM must have the specifications of 0.15~0.25μm resolution and 0.05~0.08μm alignment accuracy. As the candidates, excimer lithography

(KrF,ArF), electron beam direct writing and x-ray lithography are developed at present. However, since the resolution of an excimer lithography with a phase-shifting mask is almost equal to the requirement resolution for 256-Mbit DRAM, it is predicted that excimer lithography can not be applied to the process of 256-Mbit DRAM. The electron beam direct writing has the required resolution, but its throughput is not enough for mass production. Although there are many problems, x-ray lithography which uses synchrotron radiation as a x-ray source can satisfy both the resolution and the throughput requirement. Furthermore, x-ray lithography is in an advantageous position from the view point of cost, because the resist, which is a main part of the lithography cost, can be simplified by using x-ray lithography. Other lithography needs the complicated resist process such as multilayer resist. Therefore, it can be said that x-ray lithography has the best prospect as a lithography for 256-Mbit DRAM.

The two types of x-ray lithography, the proximity system, and the reduction system[4,5] are developed at present. Since the x-ray reduction system facilitates the x-ray mask process and has the resolution of less than 0.1μm, it is expected as a most promising technology for future micro devices. However, it is considered that the reduction lithography will not be in time for 256-Mbit DRAM production, because it has problems whose solutions can not be expected soon. Therefore, it is considered that the proximity printing system will be selected as an x-ray lithography for 256-Mbit DRAM.

Table 3 summarizes the requirements of x-ray lithography for 256-Mbit DRAM compared with the specifications of x-ray lithography used in 1-Mbit DRAM fabrication. As shown in Table 3, all the items for 1-Mbit DRAM are not satisfactory for 256-Mbit DRAM. This suggests that the development of x-ray lithography must be done for all the items. In recent years, the prospect of the resist and the x-ray source is obtained by the appearance of the chemical amplified resist[6] and the SR compact ring[7,8]. For mask-to-wafer alignment accuracy, the alignment system using an optical-heterodyne interferometry is expected[9]. The most difficult problem in x-ray lithography is x-ray mask, because the mask process technology such as the electron beam writing and the defect inspection are not completed, and the mask material and the mask structure are not fixed. Therefore, in order to put x-ray lithography to practical use for 256-Mbit DRAM, it is important that the mask technology be focused on the development of x-ray lithography. Furthermore, x-ray lithography must be improved up by applying it for the practical devices.

5.Summary

In this paper, x-ray lithography for DRAM devices were described. We feel that the improvement of the resolution of photolithography is very difficult on the development of sub-half devices such as 256-Mbit DRAM. It can be said that x-ray lithography will become a key technology for manufacturing future DRAM device.

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Table 1 Specification of x-ray stepper SX-5.

Mask Size	Diameter of Frame 76mmΦ
	Thickness of Frame 0.38～3mm
Wafer Size	Diameter 76～150mmΦ
Minimum Field Size	11×11mm
Maximum Field Size	29×29mm
Alignment Accuracy	±0.15μm($\bar{X}$+3σ)
Mask to Wafer Gap	15μm
Source to Mask Distance	200mm
Penumbra Width	0.23μm
X-ray Source Type	Electron-beam excited X-ray Source which has the Rotating Target
Source Power	10kW(25kV)
Wavelength	4.37 Å (Pd Lα)
Effective Source Diameter	3.0mmΦ

Table 2 Characteristics of 1-Mbit DRAMs.

	X-ray lithography for contact process	Photo-lithography
$\overline{RAS}$ access time (n sec)	109.5	113.1
$\overline{CAS}$ access time (n sec)	33.5	35.1
Pause-refresh time test T=2sec	good	good
Margin test for supply voltage V=7V	good	good

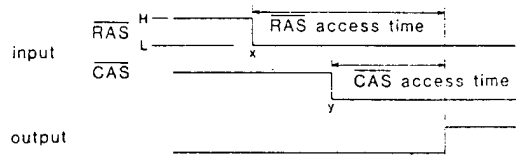

Table 3 Requirements of x-ray lithography for 256-Mbit DRAM.

Item	Requirements for 256-Mbit DRAM	Specificafions of 1-Mbit DRAM Fabrication
Mask Minimum Pattern Size	≦0.2μm	0.5μm
Mask Pattern Distortion	0.03μm	0.1μm
Resist Semjitivity	≦100mJ/cm²	250mJ/cm²
Resist Resolution	≦0.2μm	0.5μm
Overlay Accuracy	≦0.08μm	0.15μm
Throughput	>20wafer/hr.	<1wafer/hr.
X-ray Source Intensity	100mW/cm² (SR source)	0.5mW/cm² (Electron beam excited x-ray source)

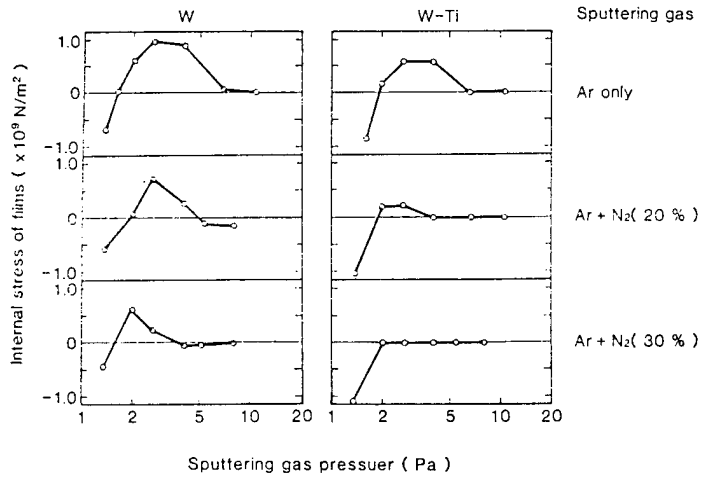

Fig. 1 Dependence of internal stress of W and W-Ti films on sputtering gas pressure and construction of sputtering gas.

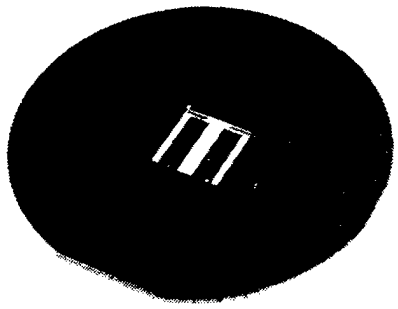

Fig. 2 Photograph of x-ray mask with W-Ti absorber.

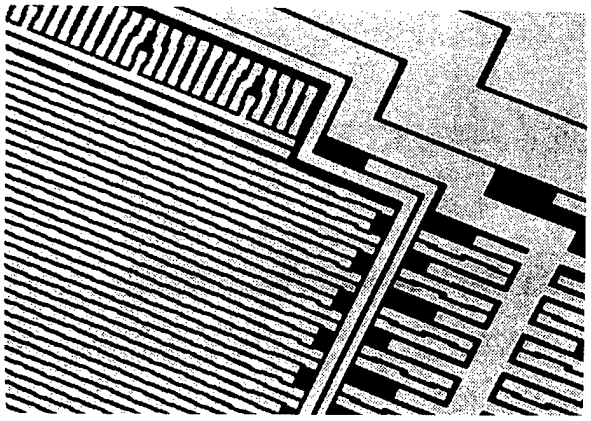

Fig. 3 SEM photograph of W-Ti absorber pattern.

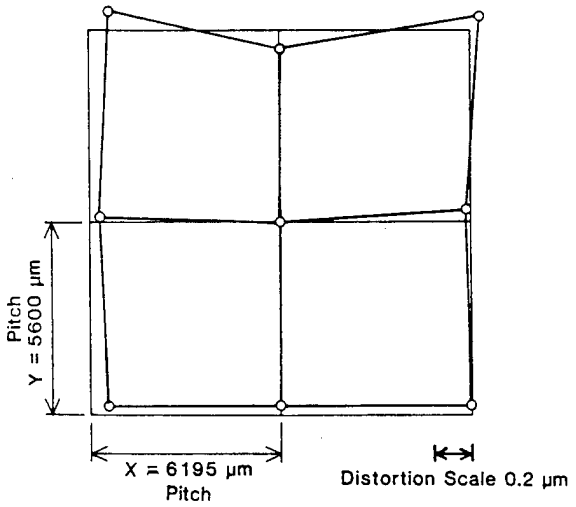

Fig. 4 Distortion of W-Ti x-ray mask.

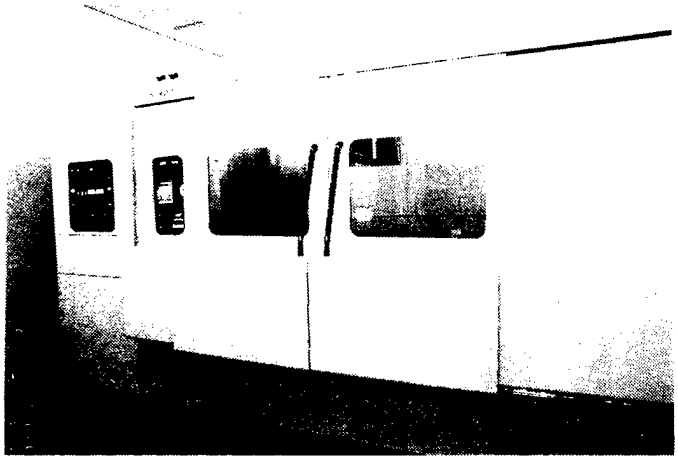

Fig. 5 Photograph of x-ray stepper SX-5.

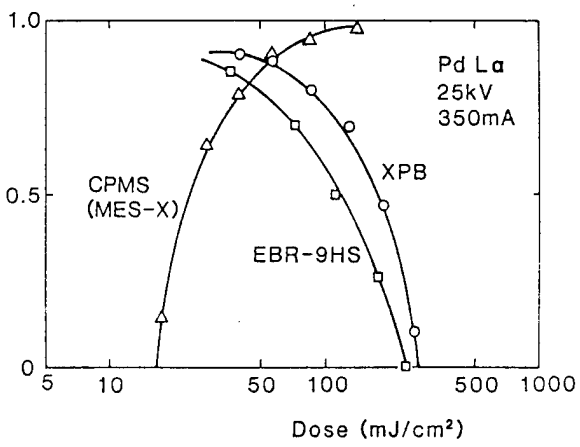

Fig. 6 Sensitivity curves of XPB, EBR-9HS and CPMS for Pd L_α radiation.

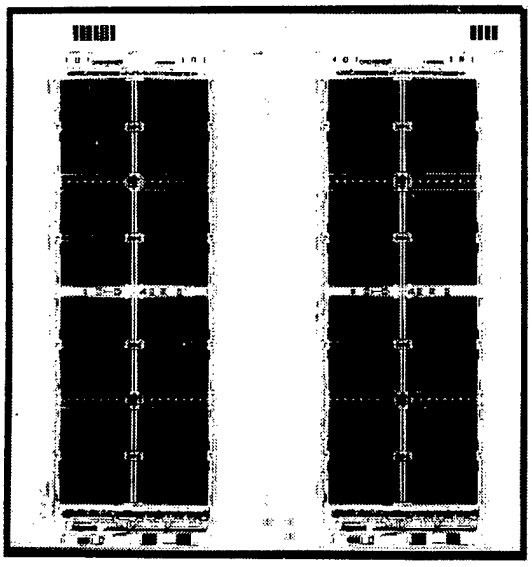

Fig. 7 Photograph of 1-Mbit DRAM in one x-ray exposure field.

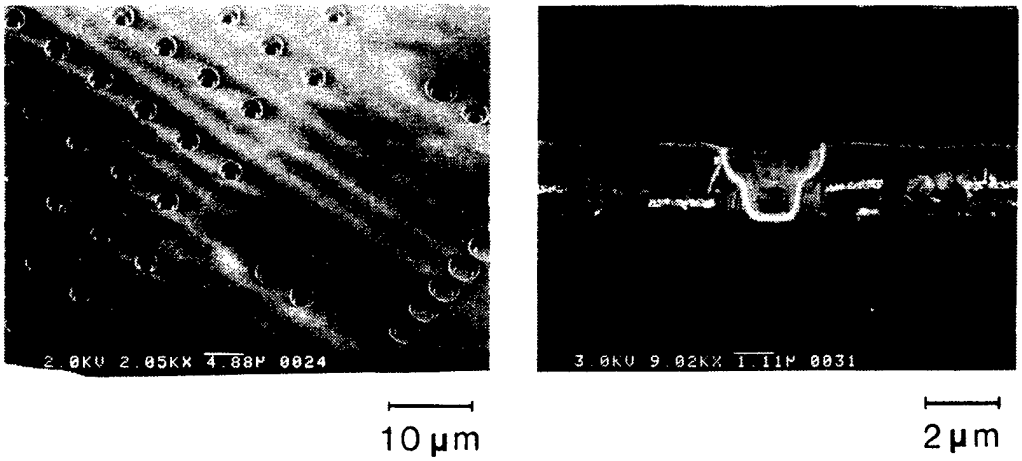

Fig. 8 SEM photographs of contact holes (SiO_2) which were formed by using XPB as an etching mask.

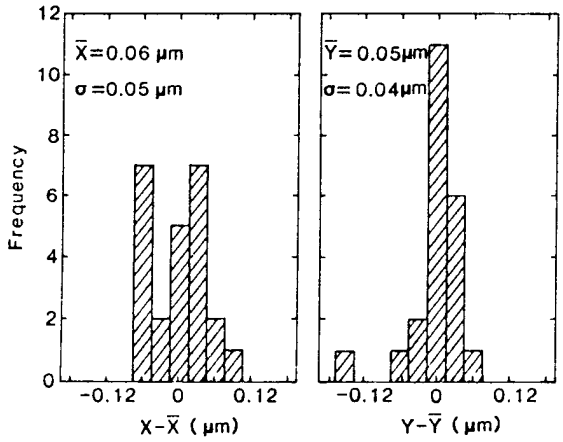

Fig. 9 Histogram of overlay error (contact process).

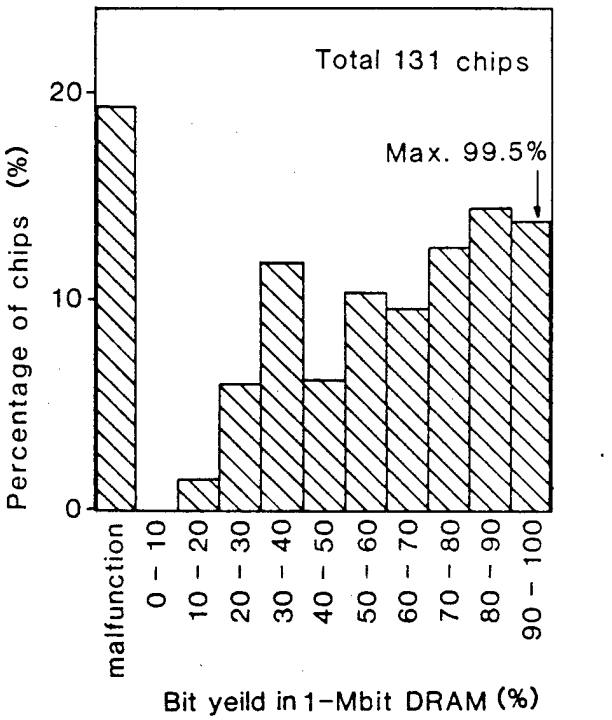

Fig. 10 Bit yield of 1-Mbit DRAMs fabricated by using x-ray lithography.

Key Technologies for 0.5 μm Si ULSI Devices

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1. INTRODUCTION

Greater integration of dynamic RAM which was initiated at 1Kbit in 1970 has still been continuing at an interval of one generation/three years simultaneously driving that of other memories and logics. According to the trend commercial 4-Mbit DRAM products have appeared in 1988. Thus, it seems that 16Mbit is now being extensively developed among DRAM manufacturers at present. Furthermore, a 64Mbit at R&D level has recently been presented at an academic conference.

While, it is getting more and more difficult to maintain the development rate because the number of fabrication steps increases and a chip area also increases associated with further integration level of DRAM. In particular, various fabrication technologies have become complicated and equipment cost has also risen up exponentially in response to requirements for finer patterning. A present stepper for 1 μm costs as 100 times as much compared to conventional contact aligner for 10 μm. Thus the arrangement of fabrication technologies becomes much more risky, therefore, inappropriate arrangement may loose big business chance.

Since fabrication equipments and processes have continuously been improved during LSI development, it is not necessarily easy to predict right equipments, technologies, and device/process at production. In this presentation, 16Mbit will be referred as a representative of LSI's with 0.5 μm feature size. Fundamental technology trends are shown in Table 1 and key subjects for 0.5 μm MOS devices are illustrated in Fig. 1.

2. DEVICE

Since fundamental performance becomes higher according to down-scaling, the down-scaling of MOS transistor is quite convenient to greater integration. While, various breakdown voltages such as those of source-to-drain and hot-carrier immunity:BV_{DS} and BV_{HC}, respectively, are reduced. In general, power supply voltage is expected to be the same as before from the compatibility point of view, then scaled devices will not be able to stand the voltage. To coped with this problem device structures have been improved in response to the requirement.

Voltage breakdown occurs at the highest electric field, then it is quite effective to reduce the field concentration in order to realize higher BV_{DS}. As shown in Fig. 2, DDD(Double Diffused Drain) having graded phosphorus profile and

LDD(Lightly Doped Drain)[1] have been introduced to attain higher BV_{DS} instead of SD(single Drain) having steep arsenic profile. Although 0.5μm devices will be realized with an optimization of this LDD, its transconductance:g_m is adversely reduced due to series resistance associated with lightly doped region. Furthermore, BV_{HC} is also reduced due to hot-carrier injection into side-wall oxide having no gate electrode on it.

An improved structure GOLD(Gate Overlapped LDD)[2] which has a electrode on side-wall oxide may be one of the solutions. Its structure and field distribution are shown in Fig. 3 (a) and (b), respectively. A reduction effect of field strength is at most 20-30% however, the improvement of BV_{DS} is remarkable as shown in Fig. 4. This is because avalanche multiplification directly related to breakdown has extremely strong dependence on the field strength. Oblique ion implantation which realizes the similar structure as GOLD gives rise to the same improvement effect.

3. MEMORY CELL

A few manufacturers have produced DRAM's with trench capacitor cells in 1M-bit instead of the conventional planar capacitor. Then, stacked capacitor cells (STC) have been added to 4-Mbit products. Various cells commercially available are slighly modified ones from fundamental these two cell types.

Two types of cells such as HPSC(Half-Vcc Sheath Plate Capacitor)[3] and DASH (Diagonal Active Stacked capacitor cell with Highly packed strorage node)[4] have been proposed by the author's group. HSPC which requires buried-insulator technique without crystallographic defect can achieve a large Cs providing low soft-error rate. More planalized surface compared to that of STC can make patterning easier. On the other hand, DASH has potential merits that high S/N ratio is obtained due to shielded bit-line and good compatibility to conventional STC. A guiding rule, "which cell has to be chosen," is strongly dependent on the past experiences and faborite technologies which each manufacturer possesses.

4. PROCESS

As previously shown in Table 1, 0.5μm technologies are on the projected trend of 0.8μm and the former ones. Though, a stepper has to be improved to some extent. A g-line(λ = 436nm) stepper with high NA lens and an i-line(365nm) are now being competitively developed. Since good i-line photoresists have recently been proposed, the i-line stepper becomes advantagerous. Several methods which enhance spacial resolution are illustrated in Fig. 7.

High NA lens adversely gives rise to narrow DOF(Depth Of Focus). Step height of surface of a film to be etched is required to be lower as aspect ratio goes high due to finer patterning. But actual surface becomes higher against the requirement due to more complicated device structures and increased metal layers.

In response to this problem, FLEX(Focus Latitude Enhancement eXposure)[5], which effectively increases DOF by multiple exposures at multiple focal planes. For example, a three-time exposure provides a DOF of $\pm 4\mu m$ compared to single one, that of $\pm 1\mu m$, as shown in Fig. 8.

In addition, a phase-shifting mask, which varies a phase of incident light by 180° between ajacent two patterns, has been proposed for i-line and excimer steppers[6] offering improved resolution. Using this, the same stepper can provide finer patterns at the next generation ahead, as shown in Fig. 9. It is very convenient also to investment to production tools. Its subjects at present are some restrictions when applied to plane patterns and the maskfabrication technology under development. It is supposed that this will be effective to simple line -and-space multiple patterns and memory cell arrays. It may be possible in the near future that a combination of this method and an excimer stepper will be able to delineate patterns of smaller than $0.2\mu m$.

As described previously, films have to be patterned with very high aspect ratio. Etching techniques having high derectionality and high material selectivity, these may conflict each other, are needed. As one of the candidates, a low temperature dry etching technique has been developed[7]. The mechanism is as follows; radical atoms, capable of highly selective etching but inactive at the temperature, are sticking on the entire surface, then highly directional incident ions assist to perform actual etching combined with radicals. As the results, high directionality and high selectivity are obtained simultaneously. For instance, as shown in Fig. 10, at a temperature of -90℃, an etch rate of silicon increases, side etching almost vanishes, furthermore, etch rates of SiO_2 and resists decrease deriving higher selectivity. The temperature varies strongly depending on material and etching gas.

As the width of aluminum wiring becomes narrower, its reliability is getting worse. Copper doping into Al-Si centainly enhances current-stress strength however, more reliable wiring is required. In response to the requirement, sandwich structure utilizing W- and Mo-silicides, TiN, or TiW are proposed. However, these layered structures often reduce the reliability as shown in Fig. 11.[8] The reason is validly speculated that electromigration(EM) strength strongly depends on size of Al grains, and these layered Al films give rise to rather small grains closely related to underlying film.

In addition, via and contact holes become small, conventional Al sputtering becames incapable of filling holes. Thus, selective W filling methods, utilizing selective W deposition on Al surface at the bottom of the hole and a combination of W sputter deposition and its etch back, have been under development. In any case, metallization below $0.5\mu m$ will require a proper technique.

Besides these technologies cited above, there are many other key issues such as reliability of thin gate oxide and high permittivity insulators, and p-n junction integrity. For instance, long-term reliabilities of various films are shown

in Fig. 12.[9] Concerning total processings of manufacturing, total cleaness of ambient air, water, gas, etc. and contamination- and defect-free processing will be enevitable for successful production. Though these subjects are not referred to in detail in this digest.

5. SUMMARY

In long-term experience of manufacturing, it is widely known that production with simple and high throughput processes will provide high yield and high reliability. However, actual production can not stop accepting more complicated and low throughput processes. It is quite difficult to find a solution to this dilemma. In addition to dust elimination, totally clean ambient will be strongly needed simultaneously with simple processings for the coming 16-Mbit DRAM and the related LSI's.

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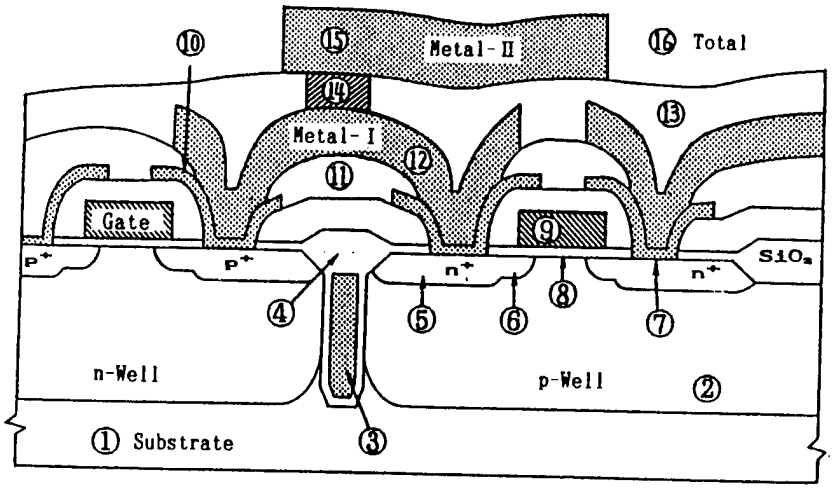
Table 1 Process-Device Technology Trends in MOS IC's

Production Start		1970 △	1975 △	1980 △	1985 △	1990 △	1995 △	2000 △
Feature Size(μm)		12	8	5	3	2	1.3	0.8	0.5	0.3	0.2	0.13
DRAM (Bit)		1K	4K	16K	64K	256K	1M	4M	16M	64M	256M	1G
Memory Cell	Structure	3T	1T·Planar					Stack/Trench				3D
	Insulator Thick.(nm)	120	100	50	35	20	10	8	5	4	3	
Device	Power Supply (V)	~20	12			5			(Int.3.3)		3.3~1.5	
	Transistor	pMOS	nMOS					CMOS				(BiCMOS)
	Drain Structure	SD				DD		LDD		(Improved)		Vertical
	Oxide Tick.(nm)	120	100	75	50	35	25	20	15	12	10	8
	Channel Length(μm)	~8	5	3	2	1.3	0.8	0.8	0.5	0.3	0.2	0.15
	Junction Depth(μm)	~1.5	0.8	0.5	0.35	0.3	0.25	0.2	0.15	0.12	0.1	0.08
Process	Lithography	Contact			1/1PJ	1/10PJ	1/5PJ (g)		(i)		(Excimer)	EB/X
	Ecthing	Solution			Plasma, RIE			ECR			LT-ECR	
	Isolation	Planar	LOCOS				(Improved)		Recessed			Trench
	Gate Material	Al	p-Si	Double p-Si		Polycide			(Al-Shunt)			Refractory
	Metallization	Al		Al-Si			Al-Si-Cu(Barrier)				Multi-L. Metal	
	Wafer Size	2	2.5	3	4	5	6	6~8	8	8~10 "ϕ		



1.Substrate	Epitaxial, SOI	9.Gate Material	Low R., Polycide
2.Well Formation	Retro-grade, Low R.	10.Selfaligned Cont.	Poly-Si, Silicide
3.Trench Isolation	Etching, Doping	11.Interm. Insul.-I	Low-Temp. Reflow
4.LOCOS Isolation	Short bird's beak	12.Metal Layer-I	High T., Low R.
5.Diffusion Layer	Low R., Silicide	13.Interm. Insul.-II	Planarization
6.Impurity Profile	High BV_{DS}, High gm	14.Via/Contact	Plug, Selfalign
7.Contact to n^+&p^+	Low R., Barrier	15.Metal Layer-II	Reliability, Low R.
8.Gate Insulator	Thinning, Integrity	16.Finer Patterning	Lithography, Etching

Fig.1 Subjects for Submicron MOS Device

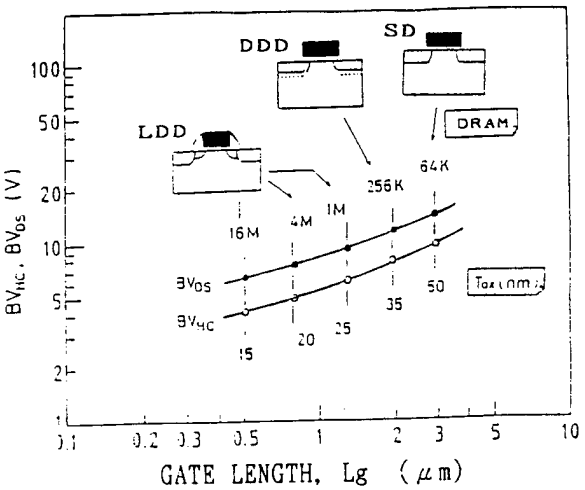


Fig. 2 Trend in Breakdown Strength of MOS Transistors

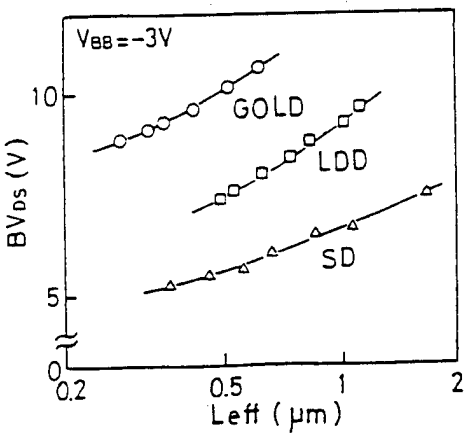


Fig. 4 Breakdown Strength of Various MOS Transistors

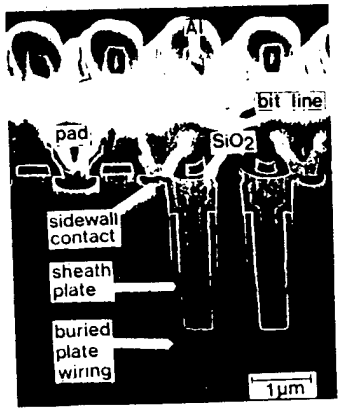


Fig. 5 Sheath-Plate Cap. Cell[3] (4.2 μm²)

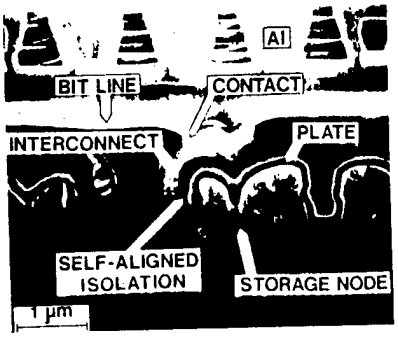
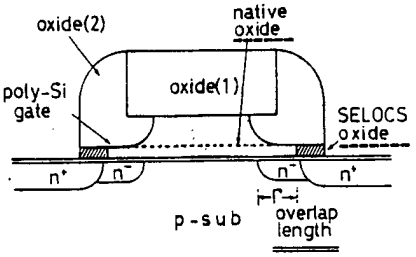
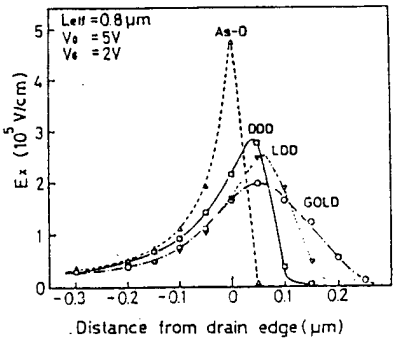


Fig. 6 Stacked-Capacitor Cell[4] (4.2 μm²)



(a)



(b)

Fig. 3 Structure of GOLD(Gate Overlapped LDD)(a) and Its Electric-Field Distribution(b).[2]

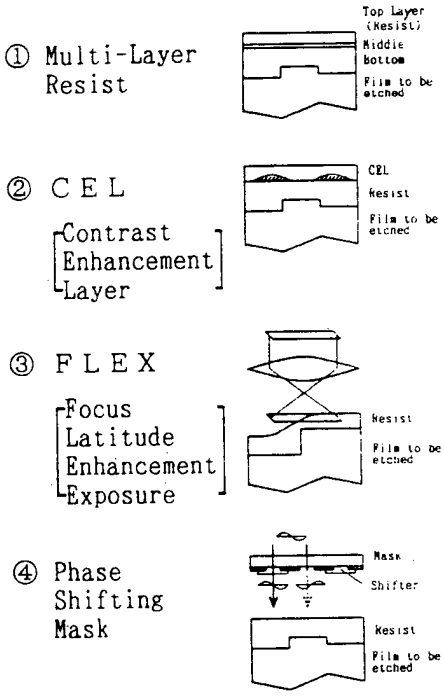


Fig. 7 Resolution Enhancement Methods for Optical Lithography

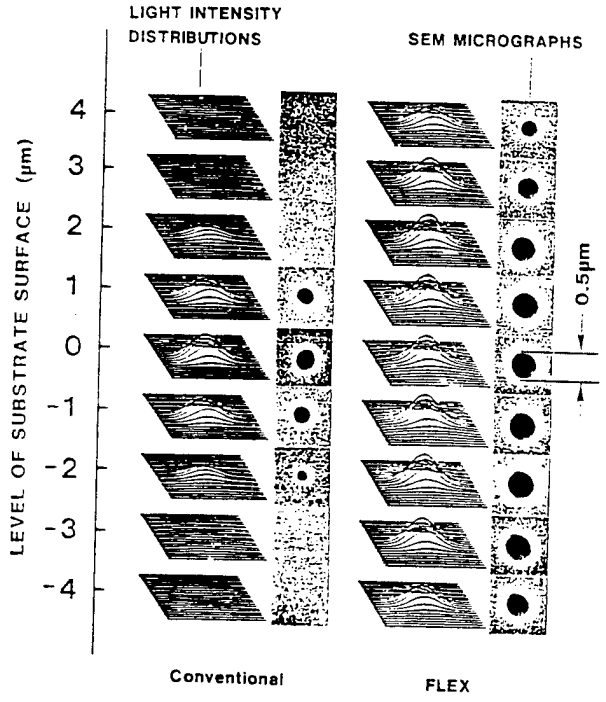


Fig.8 DOF Enhancement with FLEX[5]

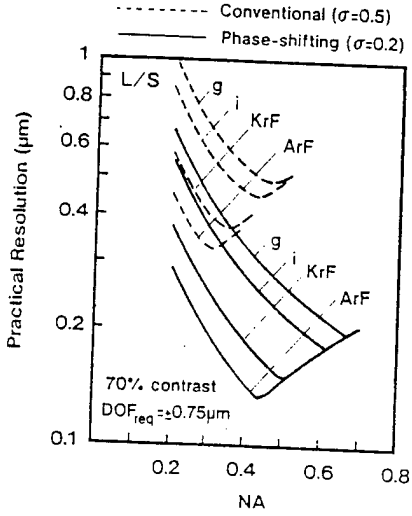


Fig.9 Effects of Phase-Shifting[6]

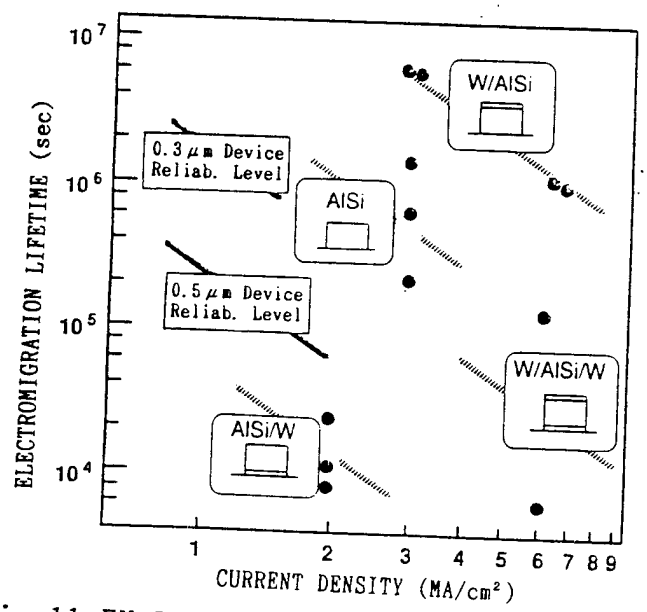


Fig.11 EM Lfetime of Layered Conductor[8]

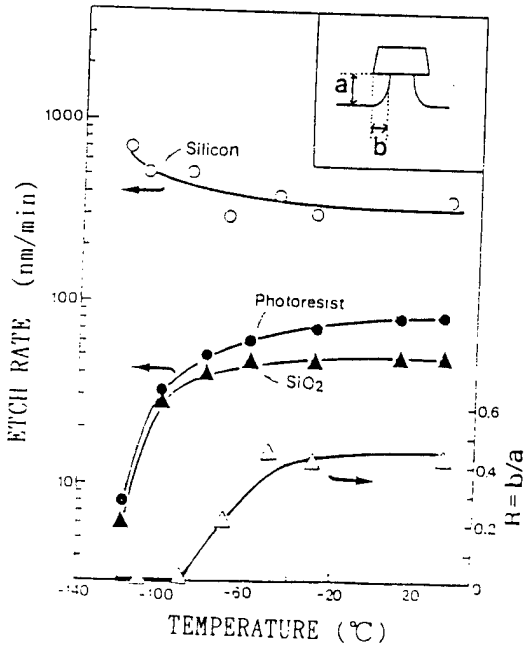


Fig.10 Characteristics of Low Temperature Dry Etching[7]

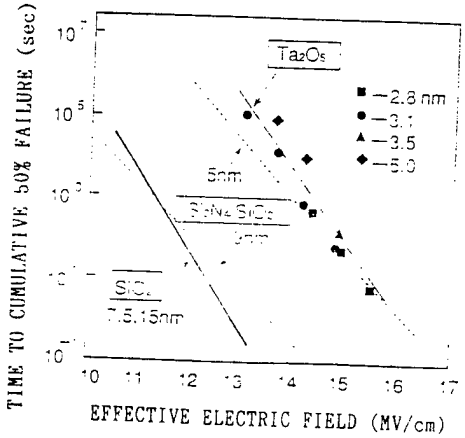


Fig.12 Long-Term Reliability of Insulators[9]

Stacked Capacitor DRAM Cell Technology

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1. Introduction

Memory cell technology is the key to producing high-density DRAM. Of the many types of cell structures proposed and applied to experimental and commercial devices, the stacked capacitor cell [1)2)] appears to have become the major candidate for current use.

We first adopted the stacked capacitor cell for 1M DRAM, as reported at the 1985 ISSCC [3)]. The stacked capacitor cell can achieve a larger plane capacitor area than the planar cell but, as we have pointed out, three-dimensional (3D) effects in the storage electrode, which signifficantly increase effective capacitor area, are the most important feature of this cell structure, hence the name " 3D stacked capacitor cell." Future DRAM would do well to take advantage of these 3D effects. For example, 16M DRAM needs about 4-μm^2 in cell and capacitor area. Large 3D effects mean a severe topography which makes fabrication difficult, however. This makes it very important to balance 3D effects with fabrication requirements. This paper discusses second-generation 3D stacked capacitor cells developed for use in fabricating 16M and 64M DRAM with an optimum balance between process and performance.

2. Fin Structure

As shown in Figure 1, the area of the stacked capacitor is determined by both the plane area and 3D effects. One is the curvature effect caused by underlying word lines, and the other is the sidewall effect. These both increase the effective capacitor area, but requirer a difficult topography. The curvature effect increases the effective capacitor area proportional to the two sides of the storage electrode, and the sidewall effect proportional to the four sides. To get the maximum performance with the minimum sacrifice requires that we take advantage of the sidewall effect. Figure 2 shows a 16M DRAM cell with thick storage electrodes. The aspect ratio of the bit line contact hole is very severe, and it is difficult to design a reasonable fabrication process. We worked to find a way to reduce the thickness of storage electrodes while maintaining the total surface area.

One way is to make vertical trenches [4)5)6)7)] in the electrode, and another is to make horizontal trenches [8)9)10)11)], but, again, these involve complicated fabrication. As is discussed later, horizontal trenches are more effective than vertical. We call the horizontal arrangement a "fin structure." Figure 3 [7)] shows a proposed fabrication for vertical trenches (i.e. "vertical structure"), which involves only conventional process technology. Figure 4 shows fin structure fabrication[9)] using only conventional process technology. Figure 4 shows the case for two fins, but this number can be varied by changing the number of polySi-SiO_2 deposition cycles without an additional mask process.

Photograph 1 shows a SEM cross section of a 4M DRAM cell using the vertical structure. Photograph 2 shows the one-fin structure. Photograph 3 shows a two-fin structure.

Figure 5 shows the measured and calculated storage capacitances for conventional, vertical, and fin structures. Storage capacitance was increased by 70% for the single fin, and tripled for the double fin. We confirmed that the fin structure is more effective than a simple vertical structure, and we have focused on this fin structure. Figure 6 shows the measured leakage current of the capacitor insulator film. Note that the fin structure caused no degradation. Figure 7 shows the distribution of capacitor film breakdown voltage. The fin structure did not increase defects in the capacitor film.

As explained above, we developed a way to fabricate the fin structure using only conventional process technology. Electrical characteristics such as large storage capacitance and reliability were satisfactory.

3. Proposed Cell Architecture (Shielded Bit Line Structure)[6)9)11)12)13)]

Figure 8 shows a 0.2-μm design rule cell. We used 50-nm-thick fins and 50-nm fin-to-fin spacing. Even with the fin structure, the aspect ratio of the bit line contact hole will be too large to keep down fabrication complexity. The difficult fabrication steps include the patterning of cell plate and bit line contact holes and bit lines. These problems occur if we form the bit lines after storage capacitors.

We therefore changed the cell structure to form the bit lines before storage capacitors, in what we call our "proposed cell architecture." As explained later, bit-line-to-bit-line coupling noise can be suppressed in this architecture, which is also called a "shielded bit line structure." Figure 9 compares the conventional and proposed cell architectures. The proposed architecture has three important advantages over the conventional: First, fabrication scalability is good, because no strict patterning is needed in the cell area after storage electrodes are formed. Second, large storage plane areas are possible because no other patterning, such as for bit line contact holes, is needed among storage electrodes, enabling storage electrode thickness to be reduced. Third, bit-line-to-bit-line coupling capacitance can be reduced because the cell plate acts as a shield.

Photographs 4 and 5 show SEM cross sections of 16M DRAM cells combining the fin structure and our proposed cell architecture. Photograph 4 shows a view parallel to bit lines, and Photograph 5 that parallel to word lines. The cell is 4.4 μm^2 and uses a 0.5-μm design rule. This gives us about 6 μm^2 in effective capacitor area. As shown in Photograph 5, the cell plate covers bit lines and can be expected to act as a shield. Figure 10 shows the measured bit line capacitance of the 16M DRAM cell. Although the cell plate capacitance increases to up to half the total capacitance, the total value remains an acceptable 1.8 fF/cell. As we expected, the bit-line-to-bit-line coupling capacitance was very small, less than 1% of the total capacitance.

To verify the fabrication scalability, we made 0.3-μm and 0.2-μm design rule cells using electron beam lithography. We thinned both word and bit lines down to 100-nm. Photograph 6 shows a SEM cross section of the 0.3-μm design rule cell, and Photograph 7 that of 0.2-μm design rule cell. Both were able to be fabricated. With the 0.2-μm design rule cell, the topography for both word and bit line patterns strained fabrication

conditions to the limit. Even if both word and bit lines are thinned to 100-nm, the total aspect ratio is 1 in the 0.2-μm design rule cell. This makes it very important to consider the topography in view of the aspect ratio.

4. Future Considerations

In 3D stacked capacitor cells, a serious conflict is expected to arise between storage capacitance and fabrication. A large storage capacitance is achieved using large 3D effects, but this means a severe topography and fabrication. To reduce the height of the storage electrode, we adopted a fin structure in addition to a new cell architecture. Both will be needed to make 64M DRAM reasonable.

In the case of 256M DRAM and its successors, it is very important to reduce the height of storage electrodes, even with the proposed cell architecture. Thick storage electrodes raise the top of the memory cell area above peripheral logic circuit areas, making it difficult to form wiring metal layers such as Al word line shunt layers, which cross over the cell area, due to the limited focusing depth of photolithography.

As reviewed earlier, the storage electrode height can be reduced by increasing the electrode surface area using vertical or fin structures or by increasing the capacitance per unit area by using thin capacitor film and/or introducing film with a high dielectric constant[4].

In vertical structures, the surface area of the inner wall is inevitably smaller tha nthat of the outer wall (Figure 3). Storage electrode thickness cannot be reduced to half even if a vertical structure is introduced. Repeatedly forming many walls[6] could concievably reduce the thickness, but again we must face the problem of complicated fabrication.

With films having a high dielectric constant, such as tantalum oxide (Ta_2O_5), the thickness equivalent to SiO_2 can be thinned to 3 nm[4]. SiN-SiO_2 composite film equivalent to SiO_2 can be thinned to 4.5 nm. Using Ta_2O_5 would enable us to increase the capacitance per unit area 1.5 times, meaning capacitor area could be decreased two-thirds and reducing storage electrode thickness by half. Ta_2O_5 needs tungsten (W) for the cell plate, but the deposition of W film by CVD has problems of poor adhesion. Sputtering is not suited to vertical or fin structures because of poor coverage. Therefore fabrication would be too unpredictable tobe practical.

Storage electrode thickness can be reduced by thinning both fins and fin-to-fin spacing. For convenience, we considered a 256M DRAM cell having an area of 0.6 μm^2, and estimated the storage electrode thickness. A vertical structure would require 0.8-μm electrodes and Ta_2O_5 film 1.1-μm electrodes. These values are very large in view of focusing depth limitations. For a fin structure, electrode thickness could be reduced to less than 0.25 μm.

In conclusion, we believe that thinning the fin structure offers the most practical solution for DRAM larger than 256M.

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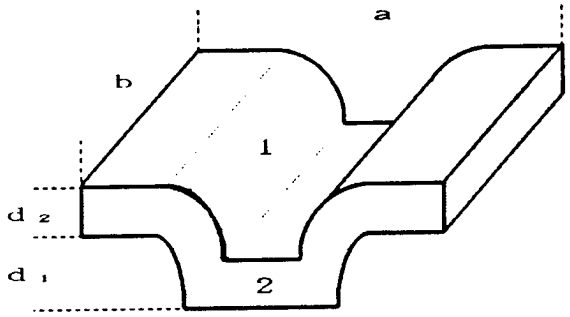


1 Curvature effect ~ 2*b*d1

2 Side wall effect ~ 2*(a-b)*d2

Figure 1 3D Effects of stacked capacitor

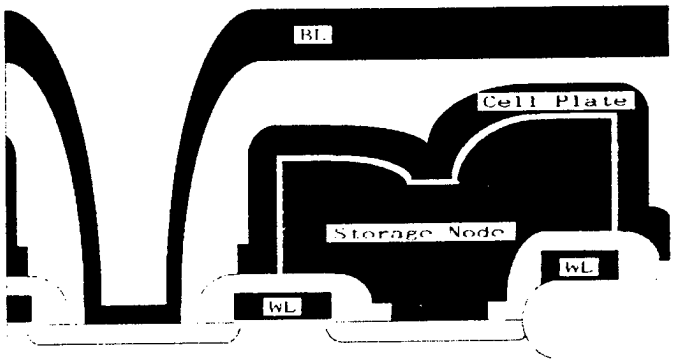


Figure 2 16M DRAM cell with thick poly-Si

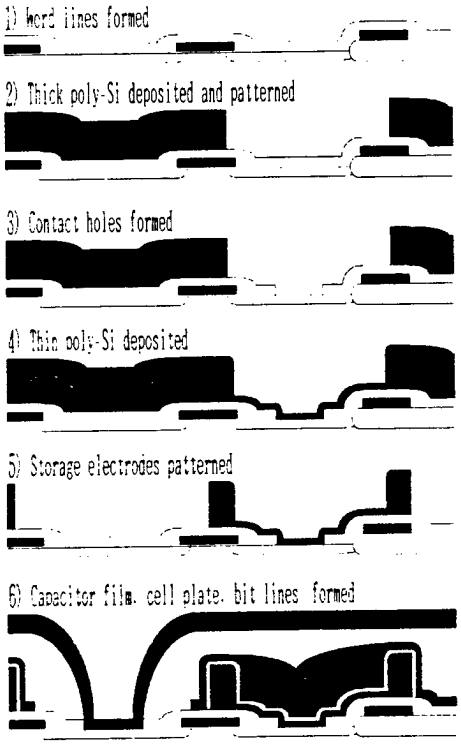


Figure 3 Vertical structure

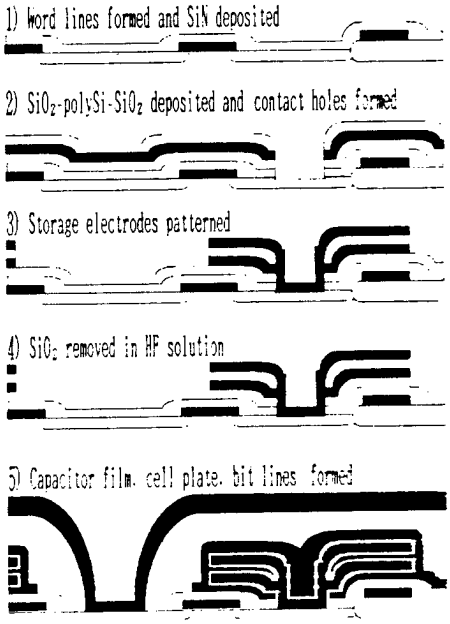
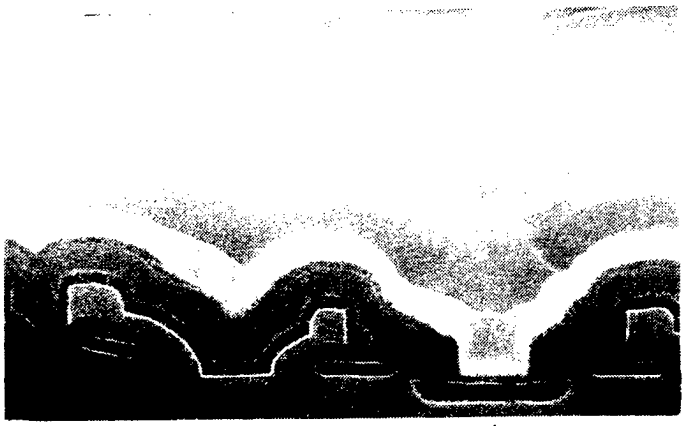
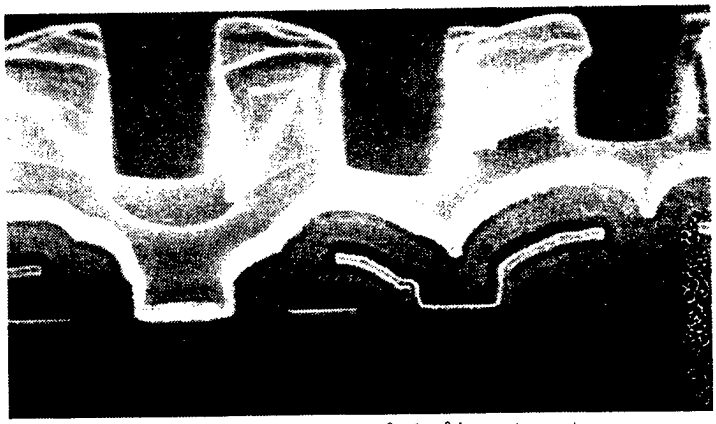


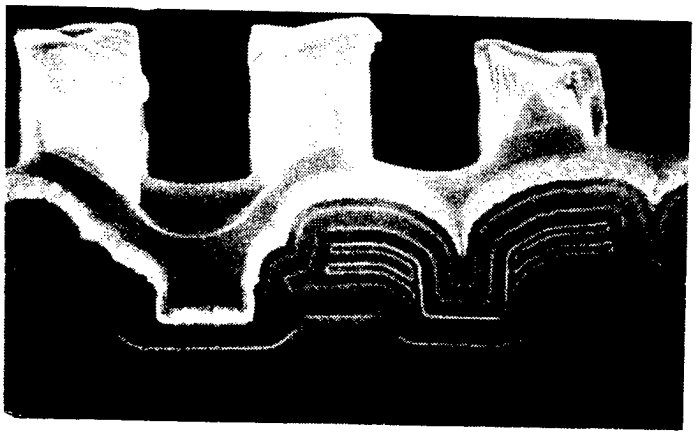
Figure 4 Fin structure



Photograph 1 SEM view of vertical structure



Photograph 2 SEM view of 1-fin structure



Photograph 3 SEM view of 2-fin structure

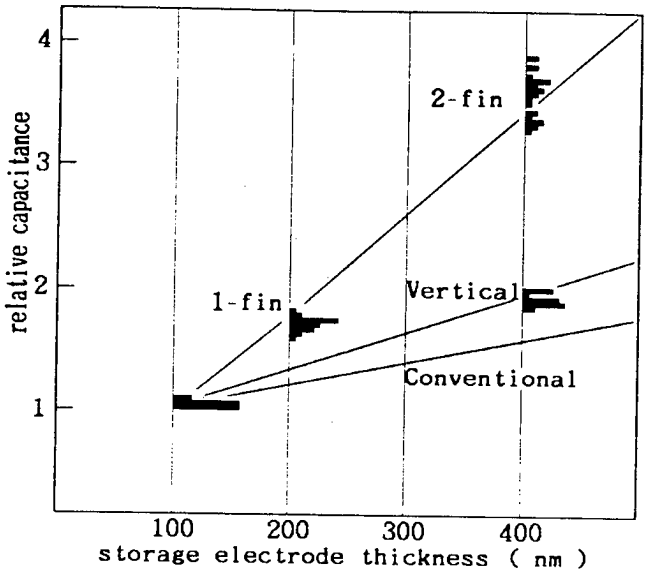


Figure 5 Storage capacitance of differnt structures

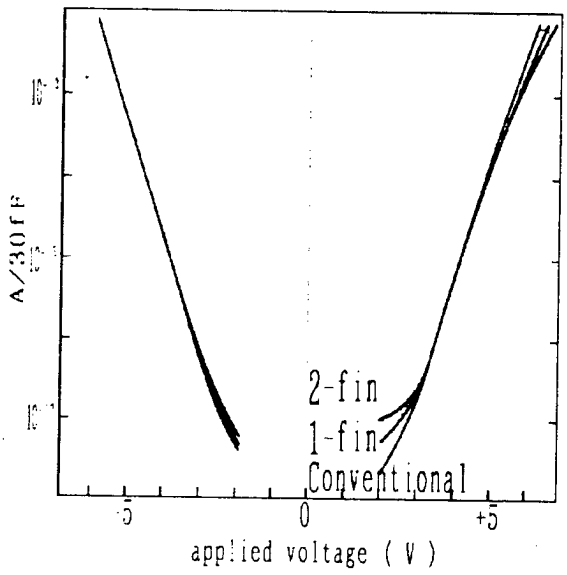


Figure 6 Capacitor film leakage current

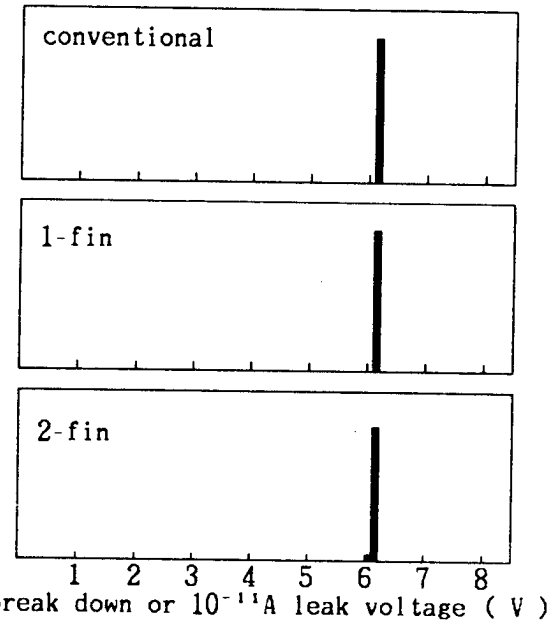


Figure 7 Breakdown voltage distribution

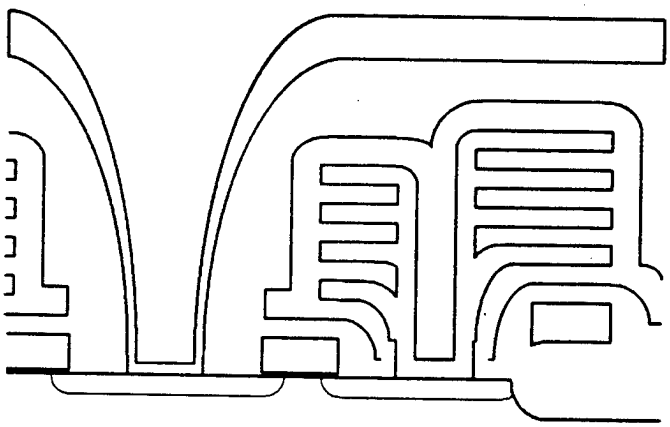


Figure 8 0.2-μm-rule cell with fin

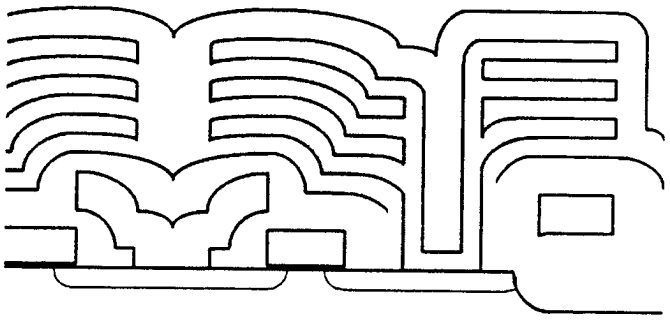
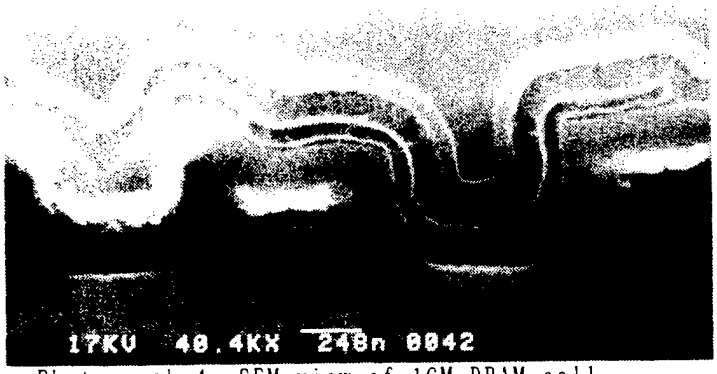
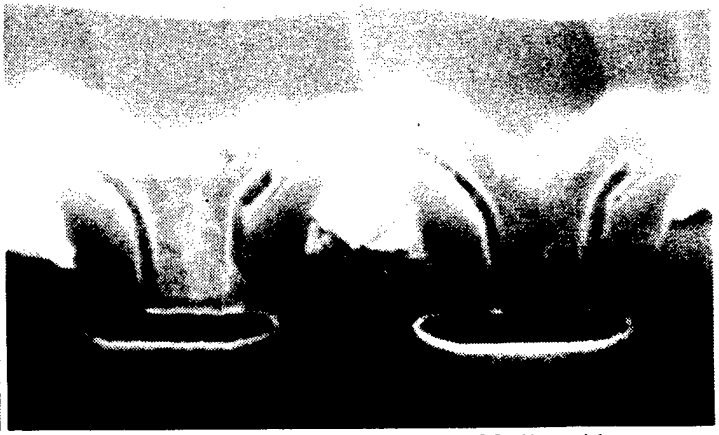


Figure 9 0.2-μm-rule cell with fin and proposed cell architecture



Photograph 4 SEM view of 16M DRAM cell parallel to bit line



Photograph 5 SEM view of 16M DRAM cell parallel to word line

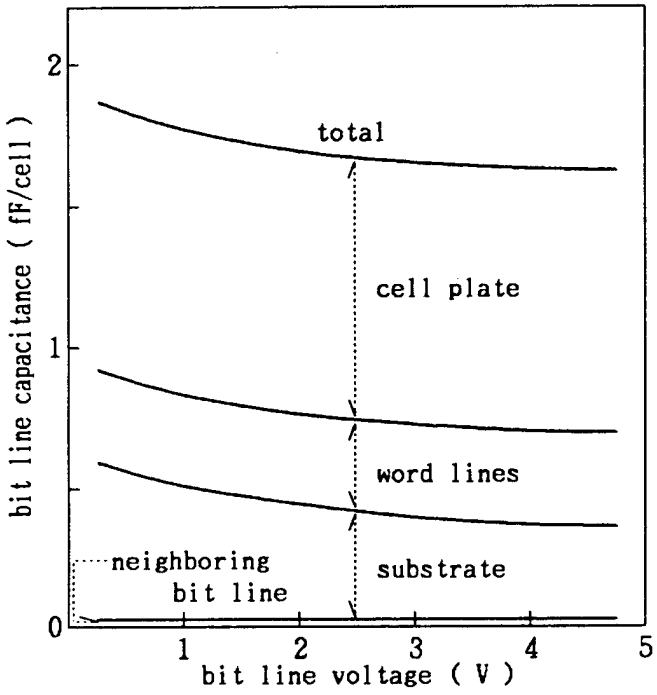
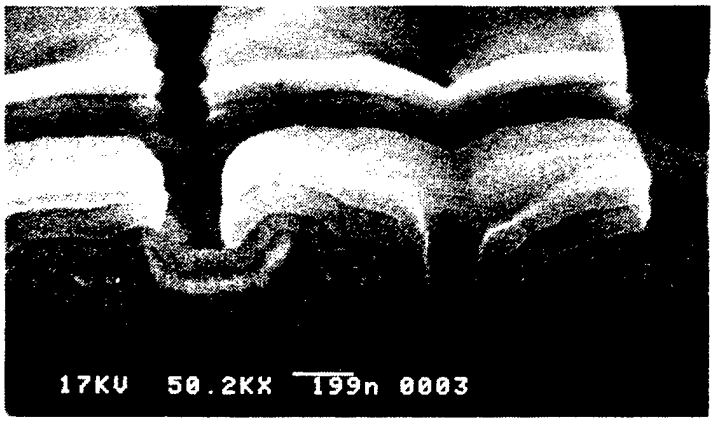
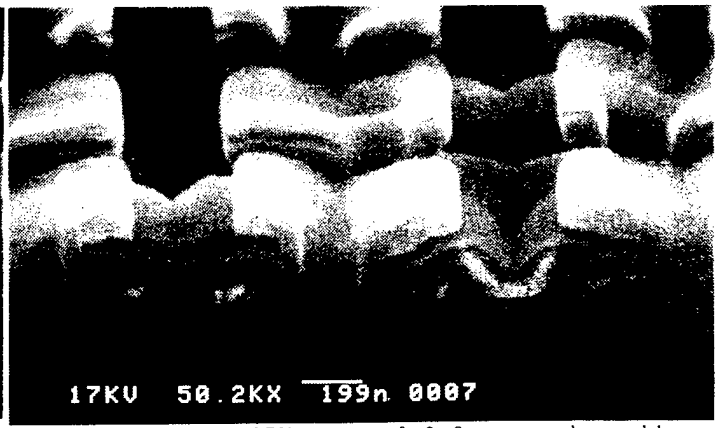


Figure 10 16M DRAM bit line capacitance



Photograph 6 SEM view of 0.3-μm-rule cell



Photograph 7 SEM view of 0.2-μm-rule cell

Process Technology in Stacked Capacitor 16Mb DRAM

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1.Introduction

Beyond 4Mb DRAMs, 3-dimensional memory cells must be used for sufficient cell charge. Toward a 16Mb DRAM, several kinds of 3-dimensional cells such as, BSCC[1], STT[2], SCC[3] and TSAC[4] have been proposed. Among them, we have concluded that the stacked capacitor cell (STC) is one of the most promising candidates for its high productivity. Since the capacitors are stacked on the gates and field oxides in the STC, increasing storage capacitance and planarization technology should be key factors for successful fabrication comparing with the trench cells. Figure 1 shows the trend of the effective field strength across the capacitor dielectric films in 64Kb through 16Mb DRAMs. In spite of the applied voltage lowering by half Vcc and the internal voltage converter, the electric field strength increases by thinning of dielectric films beyond 1Mb. In the case of STCs, the characteristics of dielectric films are very important because STCs need very thin dielectric to secure sufficient charge.

This paper describes the very thin (5.5nm SiO_2 eq.) ONO films to make simple structure STCs, the interlayer insulator for the planarization and the high aspect ratio contacts.

2. Cell parameters of 16Mb DRAM

Recently, small-size and low profile ICs have rapidly been developed by the new types of packages. Assuming the JEDEC standard 400x725mil^2 SOJ as a package of the first generation 16Mb DRAM, the maximum chip size will be around 130mm^2. The cell size is designed to be 4.06um^2 considering the cell array organization and the peripheral layout. Because cell size shrinkage reduces the soft error, critical cell capacitance is limited rather by the sensitivity of the sense amplifiers, signal to noise ratio and data retention during the refresh intervals. The storage capacitance (Cs) was set to 25fF taking the factors mentioned above and the process margin into account.

The cell structure is designed to be simpler as long as the cell capacitor satisfies its critical value. Self-align contact technologies reduce the necessary alignment margin, but they generally degrade flatness of underlying layers. It becomes essential to consider the trade-off between the reduction of the alignment margin and the lithographic simplicity of the above layers. In the developed memory cell, an effective storage node area of 4um^2 is obtained and the cell capacitance will be 25fF if capacitor dielectric films with a thickness of 5.5nm are

used. Since half of the internal Vcc of about 4V, which is lowered by on-chip voltage converter, is applied on the cell plate, the maximum electric field across the capacitor dielectric films will be ±3.6MV/cm under normal operation. The leak current of the dielectric films must be sufficiently smaller than the limited value in this electric field. Furthermore, the 4K refresh cycle design, which is proposed for the 16Mb DRAM besides 2K cycle, must guarantee the retention time of more than 64ms which is 4 times longer than that of the 4Mb DRAM. Hence acceptable leakage current gets even smaller.

The gate length of the transfer gate transistor is designed to be 0.6um. The leakage current caused by punch-through is prevented and soft error immunity is improved by fabricating the memory cell in the relatively high concentration P-well.

3. Technology of fabricating very thin ONO film

The ONO structure based on Si_3N_4 deposited by LPCVD[5] is used as a capacitor dielectric film because of its excellent adaptation to the MOS process and electric characteristics. The structure consists of the Si_3N_4 film, oxide film formed by oxidation of the Si_3N_4 (top oxide film) and oxide film at interface between polysilicon and the Si_3N_4 film (bottom oxide film). Capacitor dielectric films with low defect density, small leakage current and high reliability are formed by controlling the structure and the formation conditions.

The most serious problem in thinning ONO films is an increase in the leakage current. Figure 2 shows the I-t characteristics of capacitors with various film structure. It can be seen that thickening of the top oxide is effective for decreasing the leakage current while thickening of the bottom oxide is not effective unless the oxide becomes fairly thick. The I-t characteristics are also affected by the deposition condition of Si_3N_4, the doping condition into polysilicon and so on. Figure 3 shows the distribution of breakdown voltage for ONO dielectric films fabricated under controlled conditions. The breakdown voltage is defined by the voltage when the leakage current becomes $1uA/cm^2$. The calculated defect density is less than $0.1/cm^2$. Figure 4 shows the dependence of TDDB lifetime on the applied voltage across dielectric films with a thickness of 5.4nm and 8.5nm. The slope of lines becomes steeper as film thickness becomes thinner. Therefore in thin films, the TDDB lifetime will be longer than that of thick films under normal device operation with low applied voltage[6].

4. Planarization technology

The surface steps on STCs are severer than that of the trench type because the capacitors are stacked on the surface. The surface steps seem to increase the effective storage node area because the step side component increases. However, the effective storage node area does not increase as expected because of patterning difficulty and large transfer bias. CVD oxide film using O_3

and TEOS (tetraethyl orthosilicate)[7] which provides excellent step coverage is deposited fairly thick as an interlayer insulator. Figure 5 shows the SEM view of the memory cell after storage node patterning. The picture shows a good shape of the storage node. Conventional CVD oxide film employing O_2-SiH_4 system results in an overhanging shape and patterning of the storage node is very difficult.

BPSG films of optimum concentration of boron and phosphorous are used as interlayer insulators between the capacitor and bit line and between the bit line and metal wiring layer. Furthermore, polysilicon and polycide layers are formed as thin as possible to improve flatness.

5. Refilled contact technology

The aspect ratio of contact holes (between the aluminum wiring and diffusion layers) in STC 16Mb DRAMs becomes higher than two because of down-scaling in the contact diameter and thickening of insulating films for planarization. Thus electrical discontinuity due to insufficient step coverage by sputter deposited aluminum film has become a serious problem and contact hole refilling has become necessary for high aspect ratio contacts. Though polysilicon has been used as refilling material[8], it needs rather complicated processes with separated P-type and N-type ion implantations, and has high resistivity especially in P^+ contacts. Hence tungsten was selected because of its simple process and low resistivity compared with polysilicon.

Tungsten plugs are fabricated by the blanket CVD[9] employing WF_6 and H_2 as gas sources and etchback process. Figure 6 shows the SEM view of the tungsten plugs after the etchback. Blanket CVD can fill up contact holes of various depths at the same time. TiN film is used to make up for poor adherence of CVD tungsten film to insulating film. This film also works as a barrier layer to prevent encroachment, which is often observed in the selective deposition[10], at the bottom of contact holes.

Figure 7 shows contact resistance distribution for N^+ and P^+ contacts with 0.7um diameter and 1.7um depth. Average contact resistance for N+ and P+ is 35 and 70 ohms, respectively. Low contact resistance below several ohms is obtained for contacts on the polycide layer.

6. Summary

In this paper, important process technologies for a 16Mb DRAM with stacked capacitor cell are described. These device processes are based on 0.5um fine line patterning employing i-line steppers and RIE/ECR etchers. Aluminum alloy material of high reliability[11] and double level aluminum wiring technology are also indispensable. Figure 8 shows the cross-sectional TEM photograph of the 16Mb DRAM cell. The 16Mb DRAM device structure is summarized in Table. After this, improvement in stability of each process and a massproduction system would be required as the next step.

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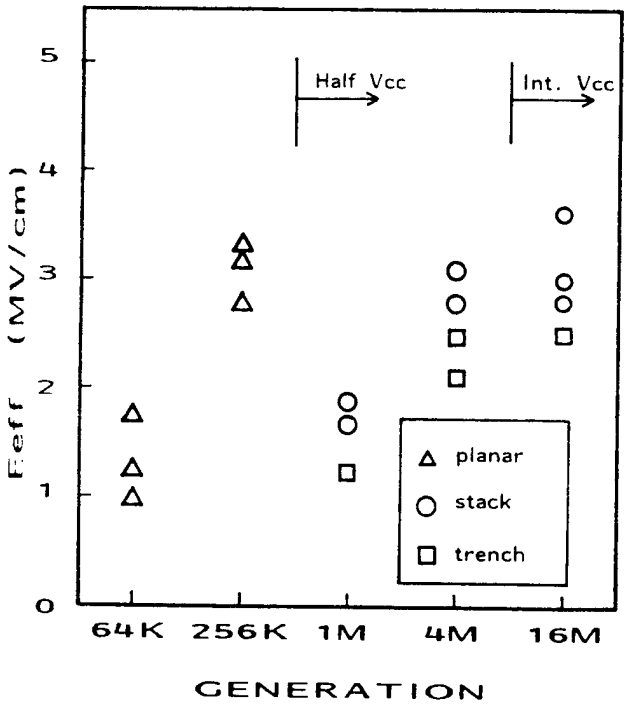

Fig.1 Trend of effective field strength across capacitor dielectric

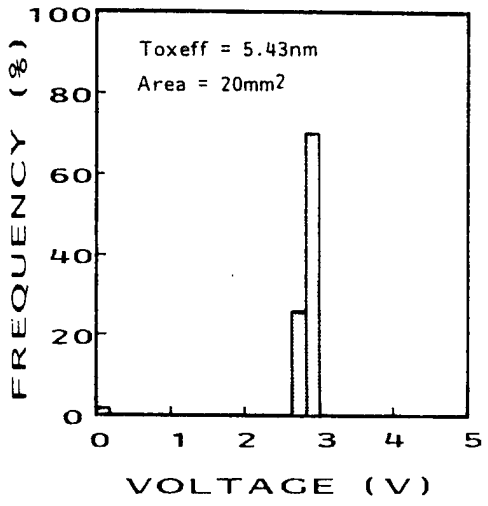

Fig.3 Distribution of breakdown voltage for ONO dielectric films (@I=1uA/cm2, storage node positive)

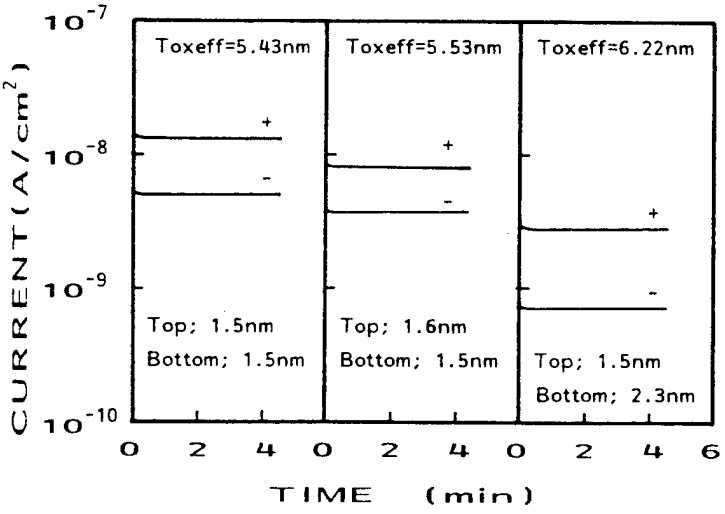

Fig.2 I-t characteristics for ONO films with various top and bottom oxide thickness (@Eeff=3.6MV/cm2)

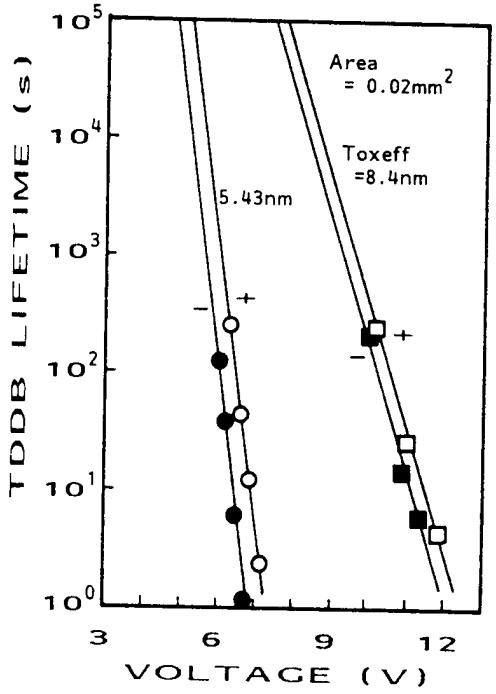

Fig.4 Dependence of TDDB lifetime on applied voltage for dielectric films with thickness of 5.4 and 8.4nm

Fig.5 SEM view of memory cell after storage node patterning

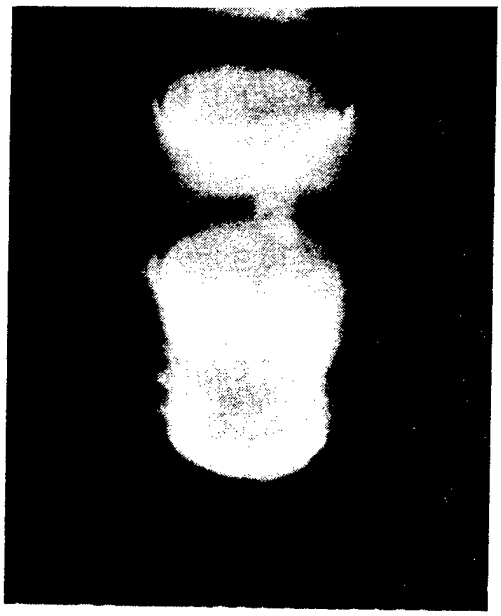

Fig.6 SEM view of tungsten plugs after etchback

Table. Summary of 16Mb DRAM device structure

Basic Process	0.5um Twin Well CMOS Process
Chip Size	7.67x16.36mm² (125.5mm²)
Memory Cell	Stacked Capacitor Cell
Cell Size	4.06um²
Capacitor	Poly Si - ONO - Poly Si Toxeff= 5.5nm
Word Line	W-Polycide + 1st Level Aluminum
Bit Line	W-Polycide
MOS Transistor	Tox = 16nm
NMOS	LDD Minimun L = 0.6um
PMOS	LDD Minimun L = 0.8um
Contact	Blanket Tungsten CVD / Etchback
Metalization	Double Level Aluminum

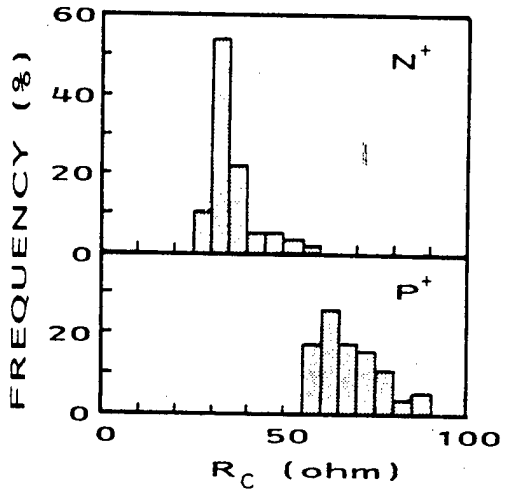

Fig.7 Contact resistance distribution for N+ and P+ contacts with 0.7um diameter and 1.7um depth

Fig.8 Cross-sectional TEM photograph of 16M DRAM cell

Trench Type Capacitor Cell

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Stacked type capacitor cells have become increasingly popular over trench type counterparts. This happens because many obstacles in the stack type cell fabrication are being overcome. For example, thanks to new generation steppers and SiO_2 etchers which have become available, it is no longer difficult to patter on corrugated surfaces reliably. In addition, adequate cell capacitance can be achieved by the optimized ONO thin film process. On the other hand, only simple trench structures, among many trench types, are of practical use at moment.

New processes developed for trench type cells, however, have large influence on the silicon process technology. For example, a method of doping into trench sidewalls (sidewall doping) by ion implantation was established in the course of development of a SCC (Surrounding Hi-Capacitor Cell)[1]. This sidewall doping technique has already been used in fabricating simple trench type cells. This implant technology also influenced new device technologies, e.g., a gate overlap structure and an improvement of asymmetrical characteristics of MOS.[2,3] Other new techniques used for the SCC fabrication will be explained to help development of DRAM of over 64 Mbits.

Advantages and disadvantages of trench capacitor cells are summarized:

○Advantages

1.Less difficulty in metallization due to small surface corrugation.

2. Compatible to the CMOS process after forming trench capacitors.

3. Large capacitor area.

○Disadvantages

1. Low through-put in the trench etching process.

2. Low through-put in poly silicon etch-back.

3. Large soft-error rate due to α particles. (except stacked trench type)

4. Many leak current paths. (gate controlled diode)

5. Punch-through between trench sidewalls.

6. More process steps. (though the number of masks is about the same as that of stacked types)

There are various kinds of trench cells:

1. Simple trench type.[4](Fig. 1)

2. Stacked trench type.[5-7](Fig. 2)

3. Double structures in a trench. (Fig. 3)(both node and plate are formed in the same trench[8])

4. Isolation is formed at the bottom of the trench.[9,10] (Fig. 4)

5. Combination of any types mentioned above. [1,11,12]

So far, only a simple trench type has been practical for mass-producing 1 M and 4 Mbit DRAMs. There also are two types of cells with a vertical transfer gate.[13,14](Fig. 5)
Listed below are processes/techniques required for the trench capacitor fabrication :

1. Trench etching technique.
2. Etch-back of SiO_2 and polysilicon.
3. Impurity doping into sidewalls of the trench.
4. Technique to reduce the punch-through between trenches.
5. Deposition of n-doped polysilicon.[15]

Shown in Table 1 are various methods for the sidewall doping. Selective doping through photomasks is realized only by ion implantation and plasma-doping methods.[16] From this table, it is understood that ion implantation is the most feasible means. However, there are several disadvantages in using ion implantation for the sidewall doping as follows:

1. Reflection of implants due to the glancing incidence (Fig. 6).
2. Higher dopant concentration in the bottom of a trench than in the sidewalls (Fig. 7).
3. The dopant concentration is too sensitive to the fluctuation of the ion incident angle (Fig. 8).[17]

Figure 9 shows a cross sectional SEM image of 0.4 μm wide trenches implanted with arsenic at a tilt angle of 4°. Figure 10 shows a cross sectional SEM image of trenches. In this case, both sidewalls are implanted with arsenic ions and etched by 0.3 μm and then boron ions are implanted into the trench bottom for isolation.

○ Leakage current

Sophisticated trench type cells, (except simple trench cells) tend to form a gate-controlled diode structure as shown in Fig. 11 (a).[18] This structure inherently increases the leakage current from the capacitor node to the substrate. And band-to-band tunneling current is also a serious problem in terms of the leakage current.[19] (Fig. 11(b)) Very thin ONO or another high dielectric films that are used in stacked type cell can not be used in order to maintain the leakage current at a low level because thin films induce high electric field in the silicon substrate.

SCC type cell

Figure 12 shows a SCC cell that is designed to overcome above problems to some extent. Its unique features are shown as follows. All surrounding sidewalls are utilized as capacitor nodes. Therefore, the whole area of the capacitor is 30 % larger than that of a simple trench cell if the

same trench depth is assumed. Cells are isolated at the bottom of the trench. Contacts with polysilicon plates are formed at the edge region of the cell array. A Hi-C structure surrounding the trench sidewall is formed by sidewall boron implantation. Isolation for the transfer gate MOS is formed by buried SiO_2. Thus the pattern shift between masks is very small, and large g_m and large contact area can easily be kept. The buried SiO_2 trench isolation will be a very attractive method for future ULSI technology. Boron implantation into sidewalls of isolation trenches are performed to control the threshold voltage of the parasitic sidewall MOS.[20] The surface corrugation after the etch-back is very flat in contrast to the LOCOS isolation. Although only an open bit line type has been considered at the beginning,[21] a folded bit line type is currently fabricated for a better noise margin by the self align contact technology and rearrangement of cells. The plane pattern of trenches in the SCC is not a dot array but a mesh form. So plasma for etching can reach easily into the trench bottom. The lowering of the etch rate with decreasing the trench width becomes very dull for the mesh type trench. Also, it is easy to clean inside of the trench in contrast to the dot type trench.

Figure 13 shows a process flow of the SCC. Both shallow and deep trenches are crucial in this cell. The LPCVD SiO_2 sidewall formation is used skillfully to make this deep trench. The connections between transfer gates and capacitor nodes are formed by selective sidewall implantation through photo resist mask. Additional etching is performed after arsenic ion implantation into deep trench sidewall to form isolation between neighboring cells. After this sidewall etching Hi-C boron is implanted into all sidewalls. Neither arsenic nor boron are implanted into shallow trench sidewalls as they are prevented by a SiO_2 film over shallow trench sidewalls.

Isolation of peripheral circuit is formed by LOCOS for practical purpose. The serious problem in application of the SCC type to DRAM over 64 Mbit is punch-through between nodes in a very narrow cell island. A high boron concentration well and a Hi-C structure would solve this problem[22] although it is very difficult to optimize the impurity profile to reduce the leakage current.

Recently Sunouch proposed a cell for 256 Mbit DRAM resemble to the SCC.[14] (Fig. 5) This capacitor structure is just the same as the SCC while the transfer gate is vertically formed.

The future of trench capacitor

The trench type with inner nodes is promising in terms of reduction of (1) punch-through between nodes and (2) the α particle soft error. But it becomes very complicated to fabricate connections to electrodes in the trenches as shown in Fig. 14.[5~7] These structures are, unfortunately, suited for mass production.

On the other hand, with a cell area under 1.5 μm^2 demanded for 64 Mbit DRAMs, the storage capacitance of stacked type cells can be increased by use of a Ta_2O_5 film[23] as a new dielectric or a fin type capacitor.[24] Thus the current trend is increasingly toward stacked type cells for realizing 64 Mbit-DRAMs.

Finally, the author would like to point out that trench type cells should be considered again in the following cases:

1. In the case where sub-micron metal pattern can not be formed over large surface corrugation.
2. In the case when capacitor cannot be formed with enough capacitance and reliability with the stacked geometries.

For example, a trench stacked hybrid type may be used for over 64 M bit as it is capable of reducing punch-through between nodes.
As long as it is possible, however, the LOCOS isolation and the stacked capacitor will continue to be key vehicles for high M bit DRAM production owing to the less difficult fabrication processes compared with those of trench type calls.

The author would like to thank Dr. S. Horiuchi, Dr. T. Takemoto, Mr. M. Inoue, and Dr. H. Iwasaki from Matsushita Electric for their encouragement and suggestions throughout this work.

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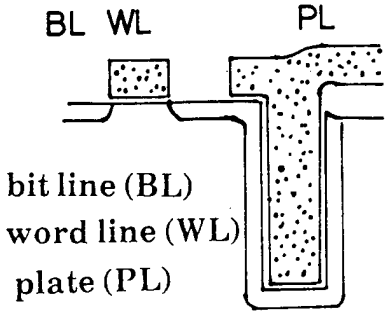


Fig. 1 A simple trench type.

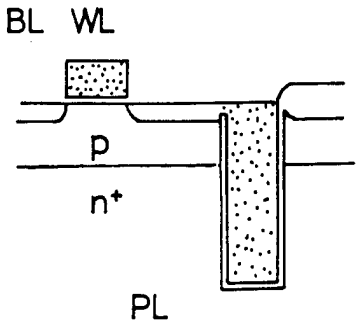


Fig. 2 A stacked trench type.

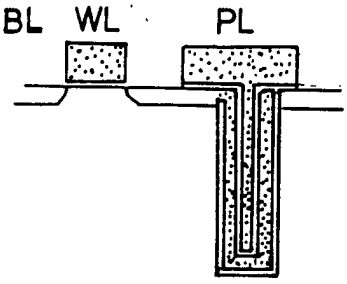


Fig. 3 A double structure in a trench.

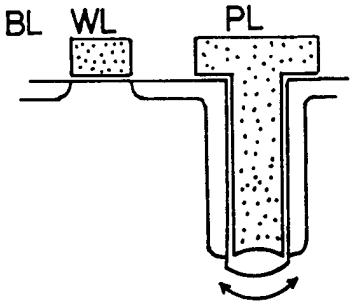
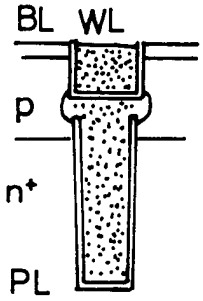
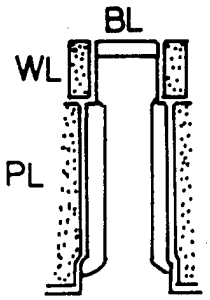


Fig. 4 A bottom isolation trench.



(a)



(b)

Fig. 5 Two types with a vertical transfer gate.

Item / Method	control of low dose	repeata-bility	photo resist mask	adding thermal anneal	influence of native oxide	removal of deposited film
gas source	×	×	×	×	×	×
solid source	△	△	×	×	×	×
spin on grass	△	△	×	×	×	×
doped CVD SiO_2	△	△	×	×	×	×
epitaxial method	○	○	×	×	×	○
plasma doping	△	△	○	○	○	△
ion implantation	◎	◎	○	○	○	○

Table 1 The comparison of sidewall doping methods.

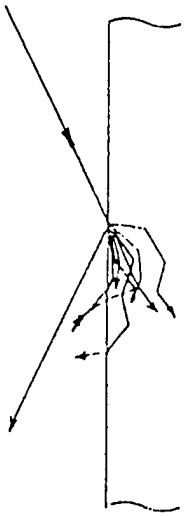
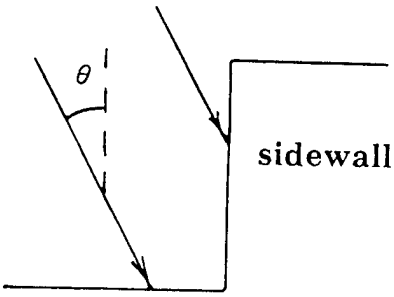


Fig. 6 Reflection and forward scattering at large tilt angle implantation.

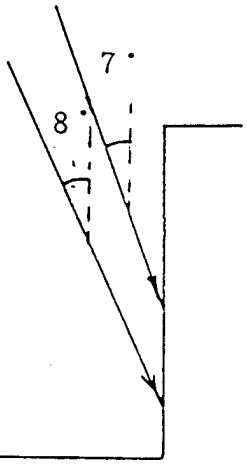


sidewall dose = dose × sinθ

bottom dose = dose × cos θ

Example $\sin\theta = 0.12$ $\cos\theta = 0.99$ at $\theta = 7°$

Fig. 7 Dose difference between a trench bottom and a sidewall.



$$\frac{\sin 8^\circ - \sin 7^\circ}{\sin 8^\circ} \times 100\% = 12.4\%$$

Fig. 8 Influence of small implant angle error.

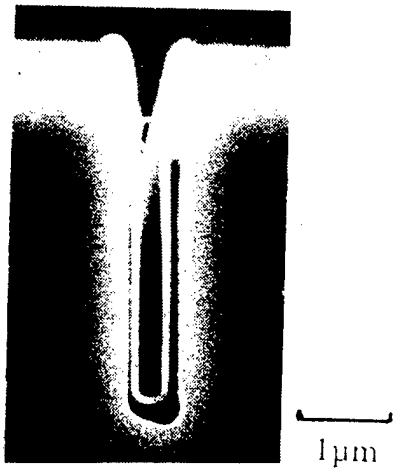


Fig. 9 A cross sectional SEM of a implanted 0.4 μm width trench at angle of 4°.

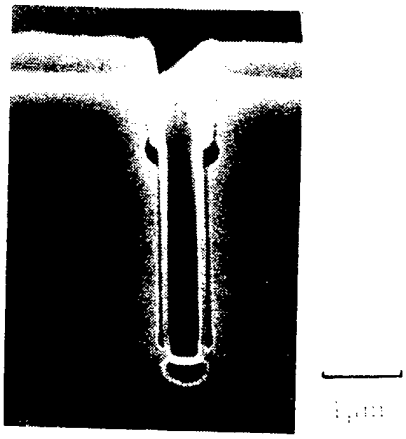
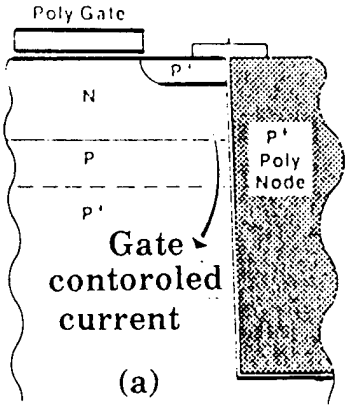


Fig. 10 A cross sectional SEM of a implanted both sidewalls with isolation.



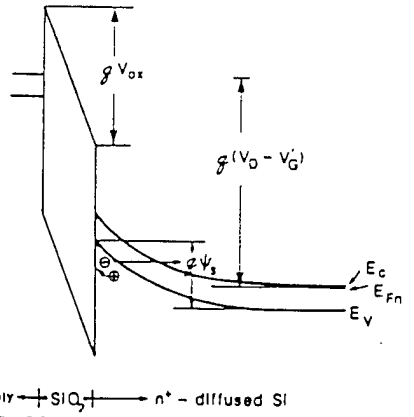


Fig. 11 Leakage current by (a) gate controled diode structure and (b) band to band tunneling mechanism.

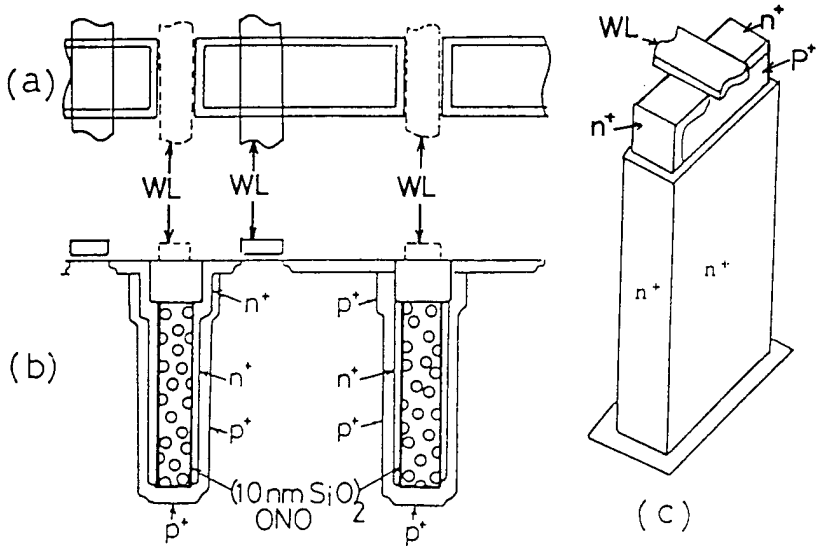


Fig. 12 A SCC structure.

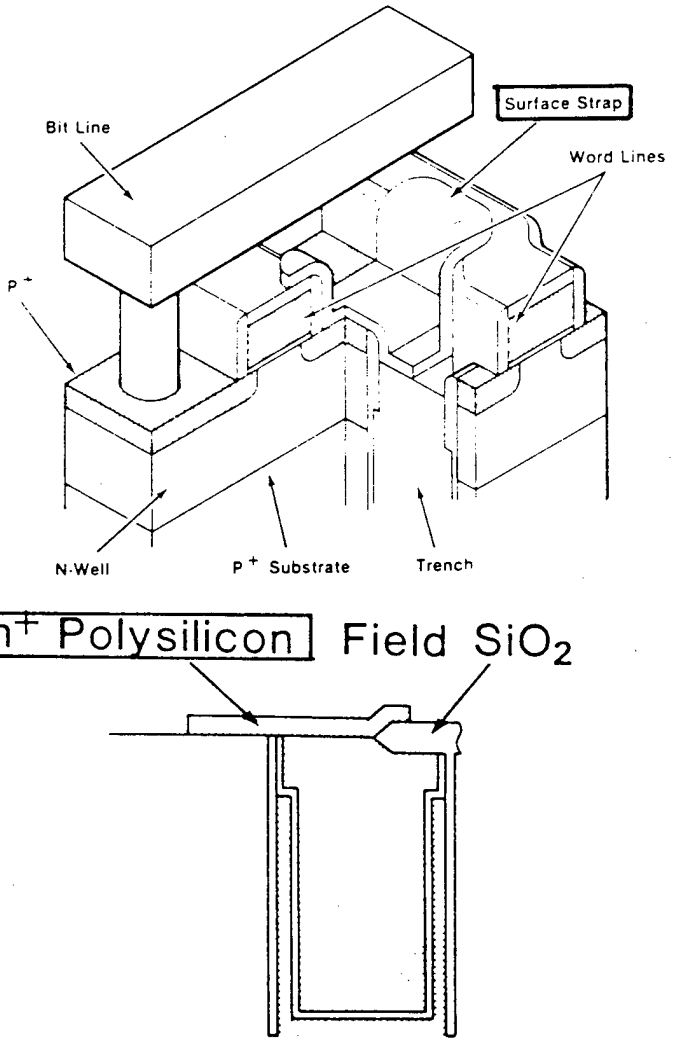


Fig. 14 Methods of the connection from a transfer gate to a electrode in trench.

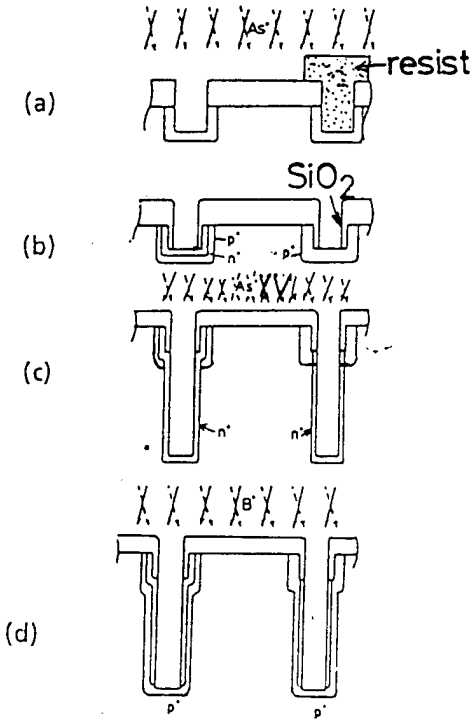


Fig. 13 Process flow of SCC.

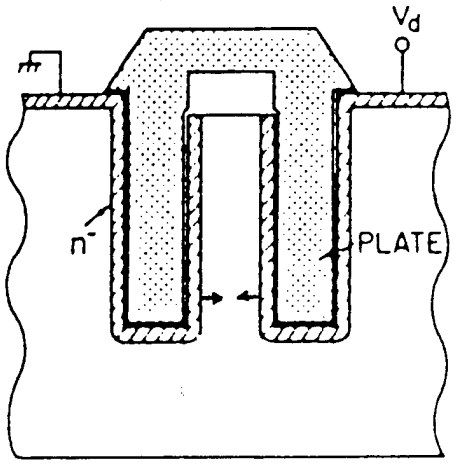


Fig. 15 Punch-through between trench sidewall electrode.

4Mbit SRAM Cell

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1. Introduction

The market for SRAM is growing steadily and ranges from portable consumer products to main memorys of super computers. Because SRAM has the merits of low power consumption and high access speed.

4MSRAMs were presented by five companies at ISSCC from 1989 to 1990. 1MSRAMs were developed by the improvements of conventional techniques. However, we are at a technological turning point in the development of 4MSRAMs. For example, the choice of power supply voltage must be carefully considered. The emergence of active TFT load cell provides a choice over conventional high resistive load cell. The design rule of 4MSRAMs is 0.5~0.6μm, and the reliability of MOS transistors and microfabrication techniques, including the reproducibility at 0.5μm level, must be established before mass production can begin in 1992.

The trends in device and process technology for 4MSRAM cell will be presented in this report.

2. Trends in SRAMs technology

Memory capacity of SRAMs has increased at the same pace as DRAMs, four-fold in the three years, after 64KSRAM of 2μm design rule was developed in 1982 (Fig.1).

Trends in cell and chip size are shown in Fig.2. The cell size of 4MSRAM is around $20\mu m^2$, about half of that of 1MSRAM. The chip size of 4MSRAM is around $130mm^2$, 1.6 times larger than that of 1MSRAM. It is estimated that the cell and chip size of 16MSRAM will be $8\sim10\mu m^2$ and $200mm^2$, respectively.

3. Features of 4MSRAM

The main features of 4MSRAMs that have been reported by various semiconductor makers are shown in Table 1. Design rules are 0.5~0.6μm. Cell sizes range from 17 to $20\mu m^2$. Occupation ratio of memory cell area in SRAM chips is about 60%. Consequently, reduction of cell size leads to a more compact SRAM chip, and the most important task in the design of SRAM is to reduce the cell size while maintaining the cell performance.

The main factors that determine cell size are the following:

(1) Ratio of access transistor and driver transistor (cell ratio)
(2) Isolation width
(3) Contact hole size
(4) Pattern delineation accuracy, including alignment

All of the above factors except (1) depend heavily on process technology, especially photolithography.

Chip sizes in Table 1 are rather large (121.7~150.3mm^2). However, these chips are developed for presentation at major conferences, and they will be under 130mm^2, by the time mass production starts.

Chip size is mainly determined by cell size and package size.

The types of power supply voltage, all 5V, 5V external supply with reduced internal supply, and all 3.3V, have been proposed recently. Power supply voltage will be set differently in various system utlization. However, on the vendor side, retrofittable chips for both 5 and 3.3V, or if possible all 3.3V chips, are favored for process simplification.

4. Structure of memory cells

Recently, two types of memory cell are mainly used for large scale SRAMs, a high resistive load cell composed of four nMOS transistors and two high resistive load, and a full CMOS cell composed of six transistors.

The full CMOS cell has better data retention and lower power consumption, but 1.6 times larger cell area than that of the high resistive load cell. Hence, the high resistive load cell is more suitable for large scale integration than the full CMOS cell. Actually, large scale SRAMs as 1MSRAMs exclusively use the high resistive load cell. However, for 4MSRAMs, TFT load cells have been proposed. A comparison of high resistive load cells and TFT load cells will be described in this section.

4-(1). High resistive load cell

The circuit of a high resistive load cell is shown in Fig.3. High resistances can be placed above the nMOS transistors formed on silicon substrate, and a small cell is easily realized. Low standby current, which is one of the most important feature of SRAMs, can be achieved by the increase of the resistances. The required standby current per memory cell to keep the standby current of the whole SRAM chip under 1μA, versus integration scale, are shown in Fig.4. The standby current per cell approaches the leakage current of the cell node as the integration scale increases. For this type of cell, bit data retention will be

impossible if the standby current is nearly equal to the leakage current level. As shown in Fig.3, if the leakage current passing through the node N1 is the same level as the current flowing in the high resistance R1, the bit data held on the node will be destroyed.

If the distributions of poly-Si resistance and leakage current value and the temperature dependence of leakage current are considered, the standby current should be several orders of magnitude larger than the leakage current. Because the leakage current is thought to arise from crystal defects that are located at the edges of LOCOS and LDD regions, it is important to eliminate these crystal defects. The crystal defects at an edge of LOCOS is shown in Fig.5. In Fig.6, temperature dependences of the standby current through high resistances and the leakage current with and without crystal defects are shown.

Soft-error is also a problem for this type of cell. The reduction of node capacitance and node voltage, which is accompanied by the reduction of cell area and power supply voltage,and the lower supplied current through the high resistances, result in lower immunity to soft-error.

This problem is avoided by shallower p-well, suppression of narrow channel effect of access transistor Q3 and substrate bias effect, regulation of sub-threshold current of driver transistor Q1, and use of lower α-particle material.

4.-(2). TFT load cell

The circuit for the TFT load cell is shown in Fig.7. Because pMOS TFT instead of high resistance, can be placed above the nMOS transistors, the cell area is the almost same as that of high resistive load cell. The standby current of this cell is determined by the off-current of pMOS TFT and is expected to be very low. Bit data for high level is held on node N1 by the on-current of pMOS TFT and, consequently, the data retention characteristics is extremly stable. An experimental data of poly-Si pMOS TFT characteristics is shown in Fig.8. On-current and off-current per cell are 10nA and 0.1pA, respectively, and on/off ratio of five orders of magnitude is obtained. A standby current of 0.5μA is expected for 4MSRAMs. Increase of on-current will lead to not only better data retention but also higher immunity to soft-error. As device structures for TFT load cell, several types have been proposed: a cell with triple poly-Si layers, of which the second poly Si is the gate electrode and the third poly-Si is the pMOS TFT channel [7], a cell that uses the high level node of the diffusion layer as pMOS gate [8], and a cell that uses a pMOS TFT with a double gate structure to increase the drivability [9], etc. (Fig.9). These device structures are thought to be promising for 4MSRAM and 16MSRAM, in spite of problems of controllability, reliability, and performance of the pMOS TFT.

5. Process technology for memory cells

Here I describe the process technology for high resistive load type memory cell developed in Sony. First, process optimization of 0.5μm MOS transistor is important. Supression of short channel effect and band-to-band tunneling current, immunity to hot carrier, and reliability of thin gate oxide film must be assured by the process optimization and the choice of power supply voltage.

Planarization, contact refilling, and wiring process are especially important for fabrication of 0.5μm design rule memory cells with high accuracy and reliability. Table 2 shows design rule of 4MSRAMs. The cell size is $3.4 \times 5.4 \mu m^2$. A structure with two aluminium layers, of which the first layer used for bit lines and the second layer for main word lines and ground lines, is used. Line and space of the first layer are 0.8 and 0.65μm, respectively, and those of the second layer are 1.5 and 1.5μm. Materials in the first layer are TiON/AlSi/TiON/Ti. The materials under the aluminium are barrier metals to prevent penetration of the aluminium, and the top material, TiON, is used as an anti-reflection film to facilitate the fabrication of fine aluminium lines. The second layer for wiring is composed of AlSi/Ti. Immunity to stress migration is increased by the bottom material, Ti. The aspect ratio of contact holes of 4MSRAM is nearly 1.0. By conventional techniques, step coverage in these contact holes is poor, and this results in a high probability of wire failure and low immunity to stress migration and electro-migration. To solve these problems, contact refilling is necessary, and following methods have been proposed:

(1) Selective W CVD
(2) Blanket W CVD
(3) Poly-Si refill (CVD)
(4) High temperature deposition of Al with bias sputtering

We applied the poly-Si refill as a highly practical technique. In Fig.10, a comparison of coverages in contact holes by poly Si refill and conventional technique is shown. Very good coverage is obtained by the poly-Si refill. Also low contact resistances were obtained by the combination with ion implantation and RTA, 40Ω for n+, and 80Ω for p+ contact of 0.6μm□ size. The relationship between contact hole size and contact resistance is shown in Fig.11.

Via holes are refilled by the use of high temperature bias sputter deposition of the second layer Al.

Planarization technique is also very important. A CVD etch back method was used for planarization between the top poly-Si layer and the first Al layer, and the combination of plasma CVD and SOG was used between the first and

second Al layer. A cross sectional view of the 4MSRAM memory cell in which aforementioned techniques are applied, is shown in Fig.12.

6. Conclusions

I have described the device and process technology for 4MSRAM in the above sections. 1MSRAMs were realized by the extention of conventional technology. However, for 4MSRAMs, the choice for the following must be made:

(1) Power supply voltage
(2) Memory cell structure (High resistive load type or TFT load type)
(3) Contact hole refilling method

There are remaining problems in microfabrication techniques, of which practical 0.5μm lithography is the most important. Other unsolved problems include the productivity, yield, and reliability of the device. However, the development of 4MSRAM is steadily proceeding to mass production which is predicted to begin in1992.

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Fig. 1 Trends of SRAMS and Design Rule (from ISSCC)

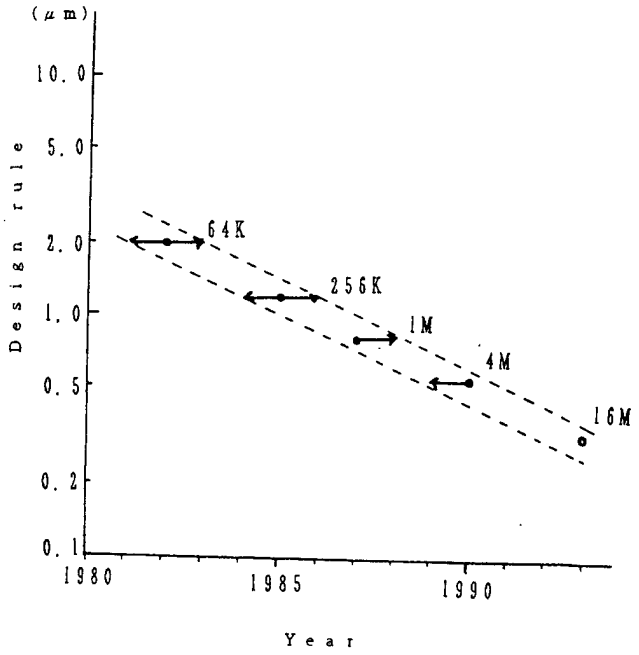


Fig. 2 Trends of cell size and chip size of SRAMS (from ISSCC)

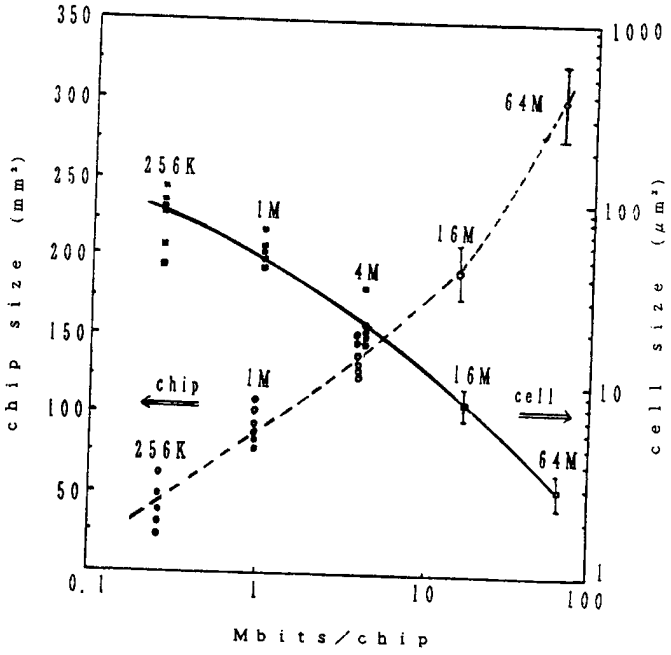


Table1 Features of 4Mbit SRAM presented at ISSCC

	design rule	cell size	chip size	cell type	Vcc (V)
Hitachi	0.6	17 μm²	121.7 mm²	TFT	5
Toshiba	0.5	20.3	135.9	TFT	5/3.3
Mitsubishi	0.6	18.55	150.3	H/R	3.3
NEC	0.55	19.04	143.22	H/R	5/4
Sony	0.5	21.15	129.9	H/R	3.3

Fig. 3 Equivalent circuit of H/R cell

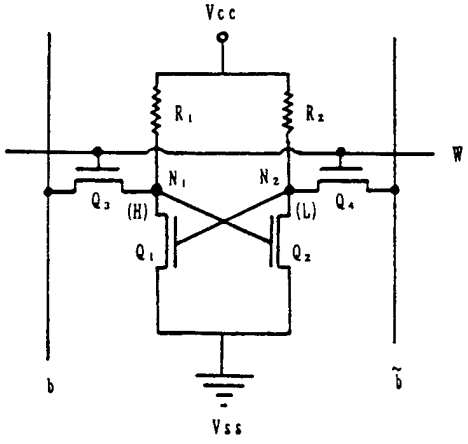


Fig4 Required through current per memory cell to achieve 1uA standby current.

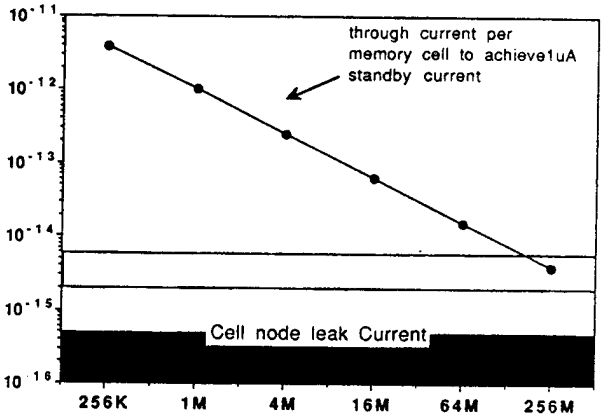


Fig. 5 Cross sectional view of the defect at LDD edge Which induces leakage current.

Fig. 6 Normal and abnormal leakage current versus H/R through current as a function of temperature

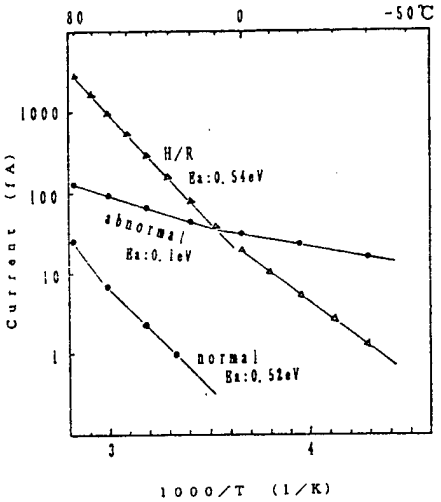


Fig. 7 Equivalent circuit of TFT cell

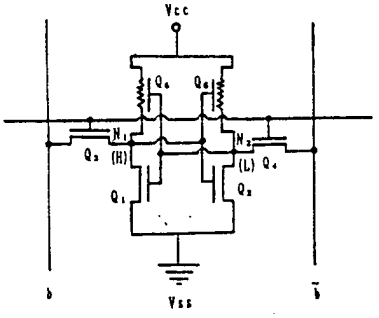


Fig. 8 Characteristic of TFT

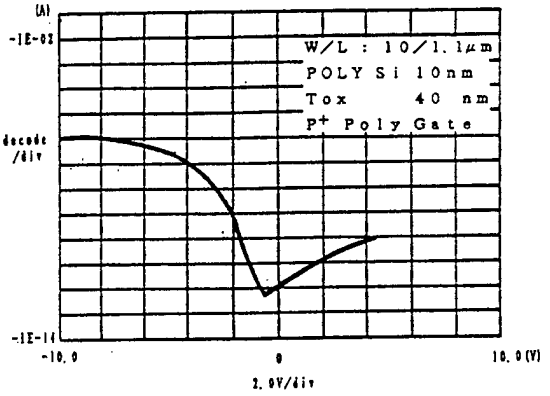


Fig. 9 Cross schematic views of a TFT cell

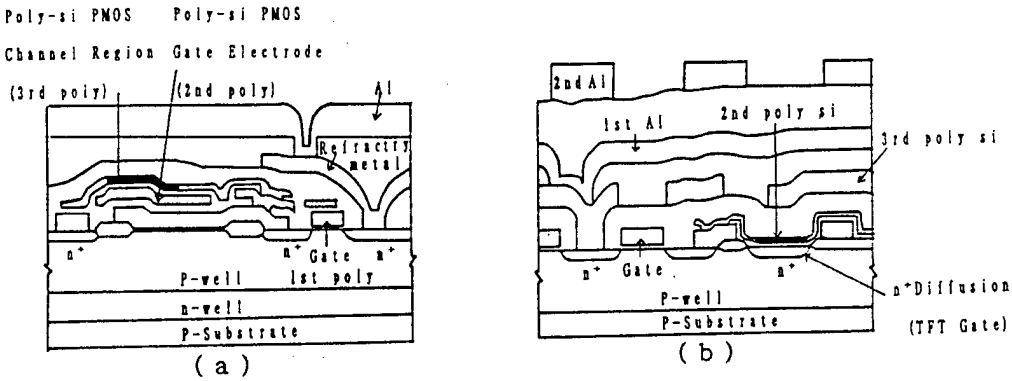


Table2 Design rule of 4Mbit SRAM

Process	0.5μm CMOS 3poly-2Al
Gate Length	NMOS 0.5μm PMOS 0.6μm
memory cell	3.4μm×5.4μm
1 Poly L/S	0.5μm/0.6μm
2 Poly L/S	1.0μm/0.6μm
3 Poly L/S	0.5μm/0.6μm
contact hole	0.6μm×0.6μm
1st Al L/S	0.8μm/0.65μm
Via Hole	0.7μm×0.7μm
2nd Al L/S	1.5μm/1.5μm

Fig. 11 Contact resistance of poly si refilled contact

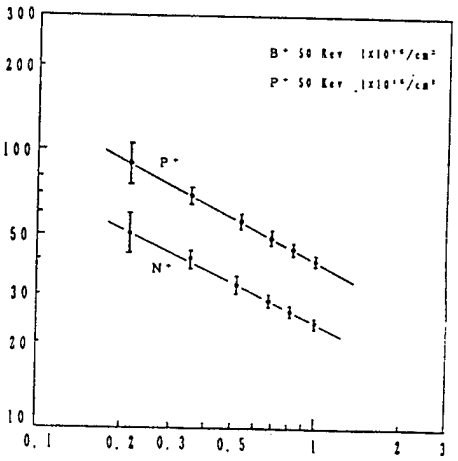
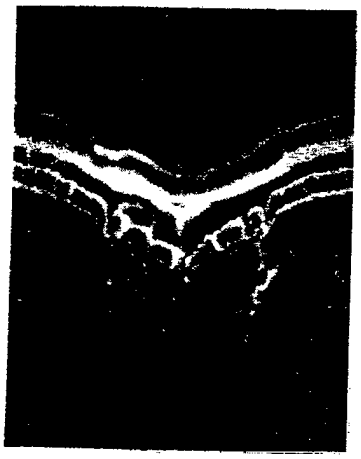


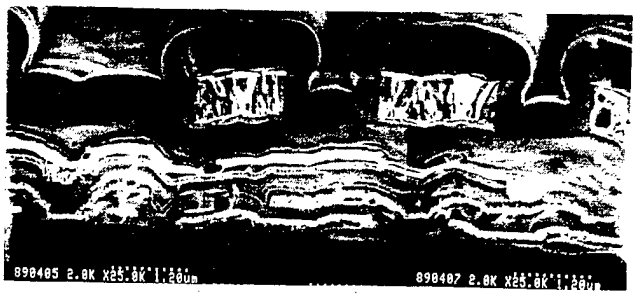
Fig. 10 Cross sectional view of a Conventional and a Refilled Contact

(a) Conventional (not Refill)



(b) Refilled Contact

Fig. 12 Cross sectional view of the 4Mbits SRAM



Interlayer Film Planarization Technology

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Introduction

Progress in integration/performance for VLSI devices is quite remarkable. In a few years, 16 megabit DRAMs will replace 4 megabit DRAMs, which are the main products fabricated today. Logic devices also will progress from 10 thousand gates to 100 thousand gates.

To achieve the VLSI progress, described above, the intentional development of 0.5 μm process technologies is required, especially for multilevel interconnection. In 0.5 μm rule designed devices, the wiring aspect ratio is larger than 1.0. Therefore, interlayer film planarization is more and more difficult. Further, reliability problems appear, because of the increase in intermetallic via-hole connection and reduction in the via-hole size.

This paper describes interlayer film planarization technologies for 0.5 μm rule designed VLSI devices. The following presents O3-TEOS APCVD BPSG for the interlayer film below Al wirings, and O3-TEOS APCVD SiO2, siloxane polyimide, complete planarization etchback for the interlayer film above Al wirings, along with the authors' data.

Interlayer Film below Al Wiring

BPSG reflow is indispensable for interlayer film planarization below Al wirings, now and in the future. The conventional technology utilizes SiH4-O2 APCVD for reflow BPSG formation. However, this technology is unsufficient for achieving 0.5 μm rule designed VLSIs, because step coverage characteristics for SiH4-O2 APCVD is not good, which leads to poor reflow planarization.

Improvement in BPSG film step coverage is achieved by using TEOS CVDs, because TEOS surface migration is large. For TEOS CVDs, low pressure CVD (LPCVD), plasma CVD (PECVD), and O3 atmospheric pressure CVD (O3-APCVD) have been studied. Especially, O3-TEOS APCVD is superior to others in regard to step coverage characteristics, productivity, and so on.

A schemetic diagram for the O3-TEOS APCVD system is shown in Fig.1. The reaction chamber consists of a dispersion head and susceptor with heator block. A 6 inch diameter silicon wafer is set face down. TEOS gas is produced by N2 bubbling of TEOS liquid. TMP/TMB, which are P/B doping sources, are also produced by N2 bubbling of TMP/TMB liquid. Ozone is produced by

using a silent discharge ozone producer. Ozone and TEOS (or TMP, TMB) are separately fed to the reaction chamber and are mixed on the dispersion head. The susceptor chucking the wafer reciprocates. This system forms silicon oxide films with good uniformity and without particle generation.

Deposition conditions for O3-TEOS APCVD BPSG are listed in Table I. Under these conditions, a high deposition rate, above 200 nm/min, is obtained. This high deposition rate leads to good productivity.

O3-TEOS APCVD BPSG films were formed on polysilicon lines with submicron spacing, and were annealed at 900°C in an N2 ambient, for reflowing. SEM observation was carried out after the reflow. The obtained SEM micrograph is shown in Fig.2. As shown in Fig.2, the O3-TEOS APCVD BPSG films form excellent reflow planarization. Further, atomic composition analysis (SIMS, etc) and investigation on physical, chemical, and electrical properties have clarified that O3-TEOS APCVD BPSG has no problem in regard to reliability.[1,2,3]

Interlayer Film above Al Wiring

Conventional technology for the interlayer film formation above Al wirings was a combination of SOG and SiH4 PECVD SiO2. Now, a combination [4] of SOG and TEOS PECVD SiO2, which is superior to SiH4 PECVD SiO2 in regard to step coverage characteristics, is being applied to multilevel interconnection for 0.8 μm rule designed devices. However, further improved technologies are required for 0.5 μm rule designed devices. In this section, the authors present more improved technologies, such as (1)O3-TEOS APCVD SiO2 [1,2,3,5], (2)siloxane polymer [6], and (3)complete planarization etchback. These technologies have the following advantageous features. (1)O3-TEOS APCVD SiO2 achieves multilevel interconnection process consititution, without SOG, which involves instability in the fabrication process. (2)Siloxane polymer is low stress film, which is indispensable for ultra multilevel interconnection with Al wirings above 5-layer. (3)The complete planarization etchback eliminates a problem in regard to focus point fluctuation in a device chip. In the following, these new technologies are described in detail.

(1)O3-TEOS APCVD SiO2

Non doped silicon oxide formed using O3-TEOS APCVD, as mentioned in the previous section, achieves interlayer planarization by itself. Figure 3 shows deposition sequence for O3-TEOS APCVD on Al wiring with submicron spacing. As shown in Figs.3 (a) and (b), ratio S/T (S: side film thickness on Al wiring, T: top film thickness on Al wiring), which expresses step coverage characteristics, is larger than 95 %. Further, interlayer film planarization with no void, is achieved along the deposition, as shown in Figs.3 (c)-(e). This is explained by a mechanism whereby a quasi liquid layer is formed on the film surface in the deposition. More-detailed discussion for the mechanism is described in References [2,3].

(2)Siloxane Polyimide

The film stress related problem is considered to be significant, when ultra-multilevel interconnection with Al wirings, above 4-5 layer, is fabricated using only inorganic interlayer film. Therefore, polyimide film, which is low stress organic film, is indispensable for the ultra-multilevel interconnection in 0.5 μm rule designed devices. For this purpose, the siloxane polyimide has been newly developed.

The siloxane polyimide structure is shown in Fig.4. Here, the siloxane polyimide has 3-dimensional Si-O bond network in the molecular structure. This leads to the following merits for the siloxane polyimide, compared with conventional polyimide. They are :(1)Excellent adhesion to SiO2 film or SiN film and (2)Increase in stiffness, to achieve a good combination of this film and inorganic films. (3)Improvement in insulating characteristics, especially at high temperature (200°C) device operation. Figure 5 shows a cross sectional view of CMOS device using the siloxane polyimide film for a 2 layer Al wiring system. As shown in Fig.5, the passivation cover SiN film can be formed on the siloxane polyimide. Therefore, Al wiring multilevel interconnection system with the siloxane polyimide garantees high reliability.

(3)Complete Planarization Etchback

SOG planarization and even the two new technologies described above cannot achieve complete planarization, in which interlayer film height on Al wiring unit in a device chip equals that on others. Therefore, these technolgies cannot eliminate the photo-lithography related problem, wherein exposure light is not focused for the entire chip. This problem must be solved for 0.5 μm rule designed multilevel interconnection. In this section, the complete planarization etchback, developed for this purpose, is described.

A key to achieving complete planarization etchback is the adoption of a new etchback film. The new etchback film is the polymer, which is formed from stylene-chloromethylstylene copolymer, shown in Fig.6, whose molecular weight is as low as 1000 with narrow dispersion. Advantageous features of this polymer are as follow: (1)Spin on planarization is excellent. Further, this polymer reflows at a relatively low temperature, 200°C. (2)This polymer accompanies bridge-reaction under ultra violet light exposure, after spin on, leading to high reproducibility for the etchback process. The complete planarization etchback sequence, using the new etchback polymer, is shown in Fig.7. The obtained result for the complete planarization etchback is shown in Fig.8. As shown in Fig.8, complete planarization is achieved for all of the device chip.

CONCLUSION

Interlayer film planarization technologies for 0.5 μm rule designed VLSIs are described. For the interlayer planarization below Al wirings, O3-TEOS APCVD BPSG reflow is being adopted in mass production. For the interlayer planarization above Al wirings, more intentional developments for new technologies, such as O3-TEOS APCVD SiO2, siloxane polyimide, complete planarization etchback, and so on, are required.

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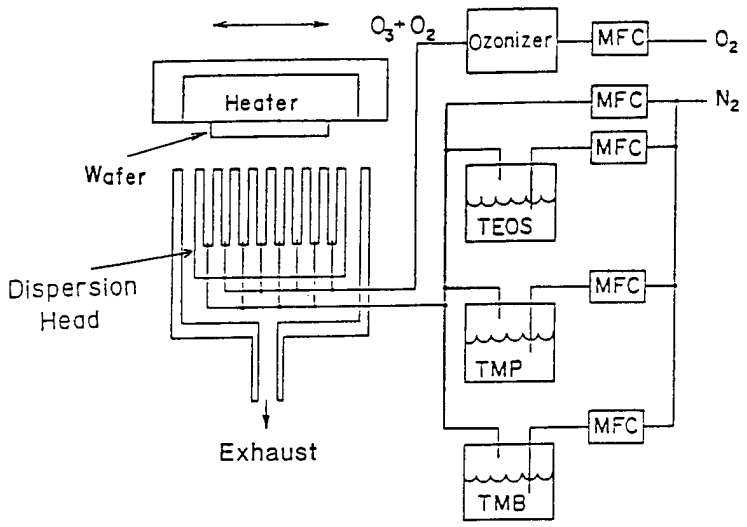


Fig.1 Schematic Diagram for O3-TEOS APCVD System.

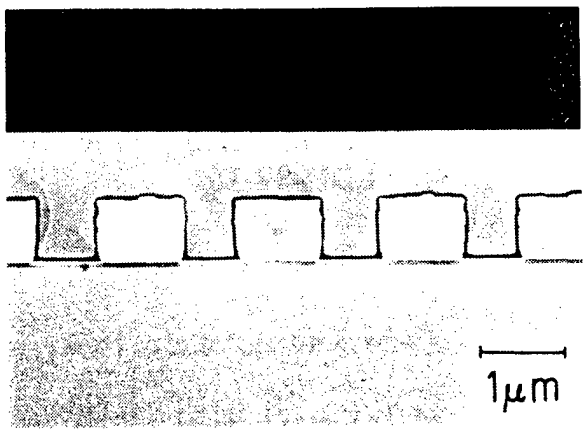


Fig.2 Planarization for O3-TEOS APCVD BPSG reflow.

Item	Values (unit)
Depo. Temp.	250-480 (C)
TEOS(a) Flow Rate	80-160(sccm)
O2 Flow Rate	7.5 (SLM)
O3 Concentration	0.3 - 4.8 (%)
TMP(b) Flow Rate	4 - 40 (sccm)
TMB(c) Flow Rate	3 - 24 (sccm)

(a)Tetra Ethyl Ortho-Silicate : Si(OC2H5)4
(b)Tri-Methyl Phosphate : PO(OCH3)3
(c)Tri-Methyl Borate : B(OCH3)3

Table.I Deposition process parameters.

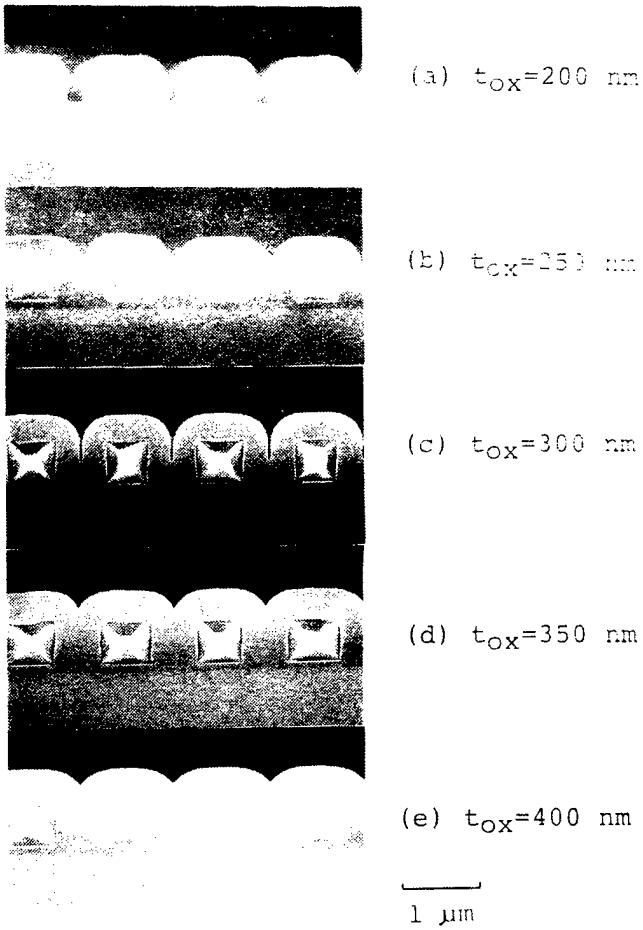


Fig.3 O3-TEOS APCVD SiO2 deposition sequence.

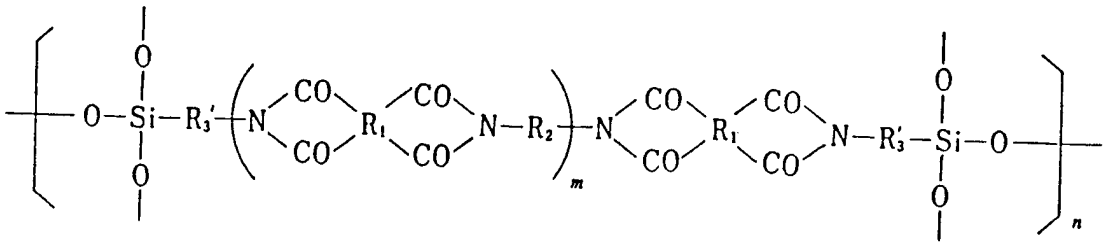


Fig.4 Siloxane polyimide structure.

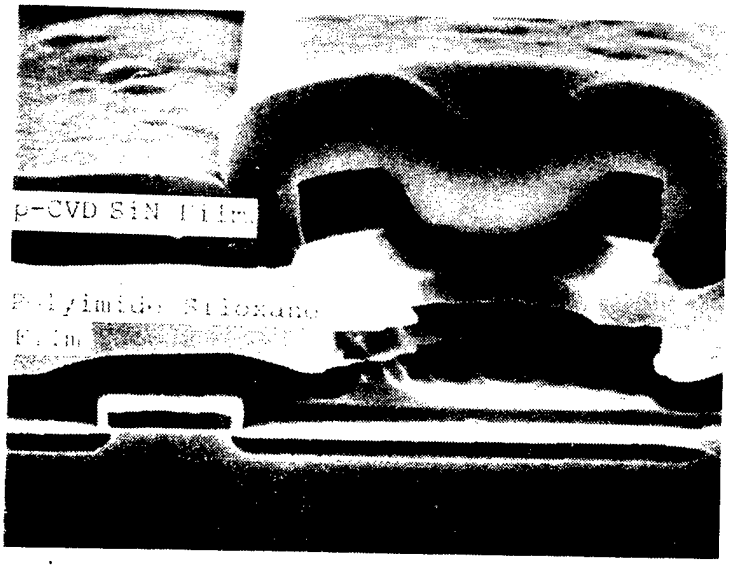


Fig.5 Cross sectional view of a CMOS using the siloxane polyimide.

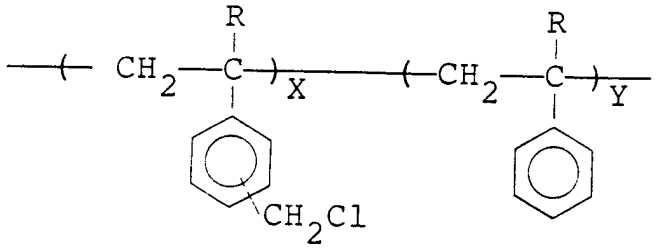


Fig.6 Stylene-chloromethylstylene structure.

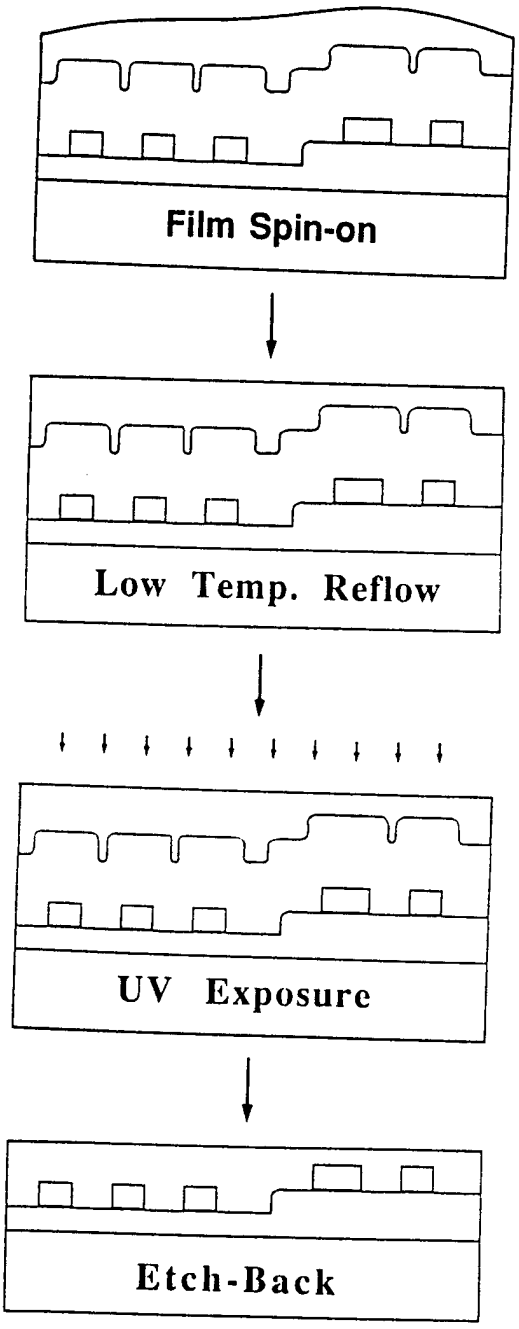


Fig.7 Complete planarization etchback process sequence.

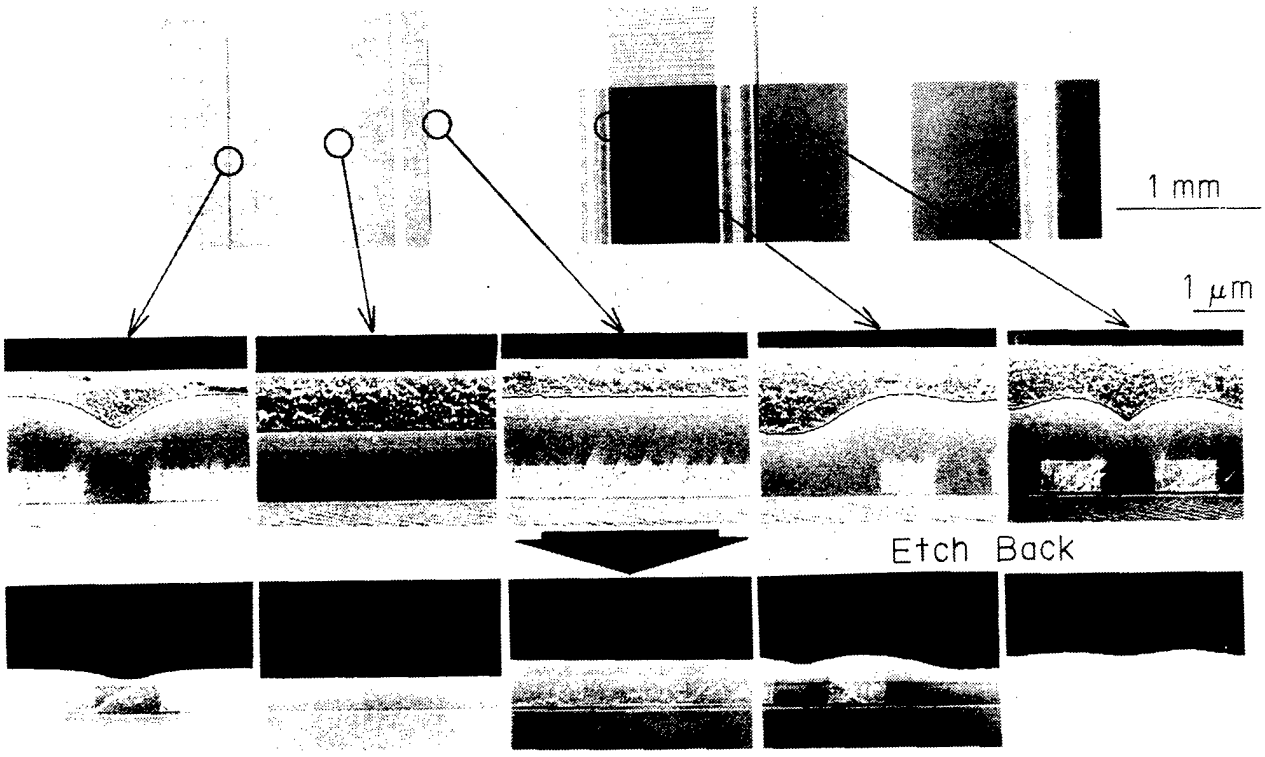


Fig.8 Result for complete planarization etchback.

Planarization using Spin-on glass(SOG)

1. Introduction

With the rapid progress of high integration and faster speed devices by VLSI interconnect technology, the devices shrink in lateral dimensions for fine line patterning, while the shrinkage in vertical dimensions is hardly allowed. Therefore, device surface structure such as high-rise building architecture with a further high aspect ratio highlights the need for surface smoothing. And the current major issue is how to select"planarization technology" and "materials" on step coverage together with an intermetal dielectric as the multilevel interconnection advances.

2. Planarization methods

The planarization approaches which have been developed and practised so far are as follows:

1. Reflow steps (CVD, PSG or BPSG)
2. Vias ECR CVD ① :(1) Semicon News, June 1989, p.54
3. Vias sputter quartz ② : (2) Draft of the lecture at the autumnal Applied physics related federation, 1989, p.976, 30p-D-2
4. Atmospheric temperature TEOS-based oxide + a O_3 CVD system
5. Etchback method(Photoresist, SOG, and polyimide are used for a mask)
6. Planarization method by coating(Inorganic SOG, organic SOG, and polyimide)

3. Planarizing points

Device structural points to be planarized are as follows: (quoted from Semicon News, June, 1989, pp.49-55 by Mr. Kazuo Maeda)

1. Field oxide film
2. Trench element separation
3. Intermetal dielectric on gate electrode
4. Position with a high aspect ratio of Al-Al
5. Intermetal dielectric via hole fill over the contact hole and Al lines

In addition, Al optical reflection brings about the abnormal exposure and standing wave effect in the step coverage. When considering poor focus and "photolithographic factors" such as poor dry etching resulting in dispersion of resist film thickness, various points to be planarized may increase further.

4. Advantage and disadvantage of the SOG processes

This time, "planarization methods using SOG are demonstrated below as a SOG materials maker.

When the conventional CVD method(AP, LP, PE) and the PVD method(sputter, evaporation) print the underlying topography and advance the processing to satisfy occasionally stringent quality requirements, the feature in step coverage becomes severe. With the flow of each generation such as IC $\longrightarrow$ LSI $\longrightarrow$ VLSI $\longrightarrow$ ULSI, several approaches for step coverage and planarization are required.

For this purpose, Spin-on glass(SOG) as full planarization methods suited for advanced devices has been used increasingly for improving satisfactorily step coverage. However, there are disadvantages also in planarization methods, for which how to avoid such disadvantages for practicality is a major point at its introduction.

4-1. Disadvantages by the SOG processes are as follows:

1. Too much thick films will likely be cracked.
2. Film quality is poor at low temperature bake compared with the CVD system films
   ..... (Degas and moisture absorption issues)
3. Non-conformal deposition profiles in the underlying topography
   ..... due to thin deposition on the convex and thick one on the concave in a single intermetal dielectric process, electrical characteristics are likely dispersive.

Therefore, in the intermetal dielectric process, the SOG process is not singly employed, but in conjunction with various CVD films with conformal deposition profiles for its practicality.

4-2. One of advantages by the SOG processes is presented below:

For the advantage of planarization methods or how to improve the step coverage by SOG processes, coated profiles of the topography become similar step coverage and planarization if the underlying step coverage has the same ratio as the lines and spacings.(Refer to Fig. 1)

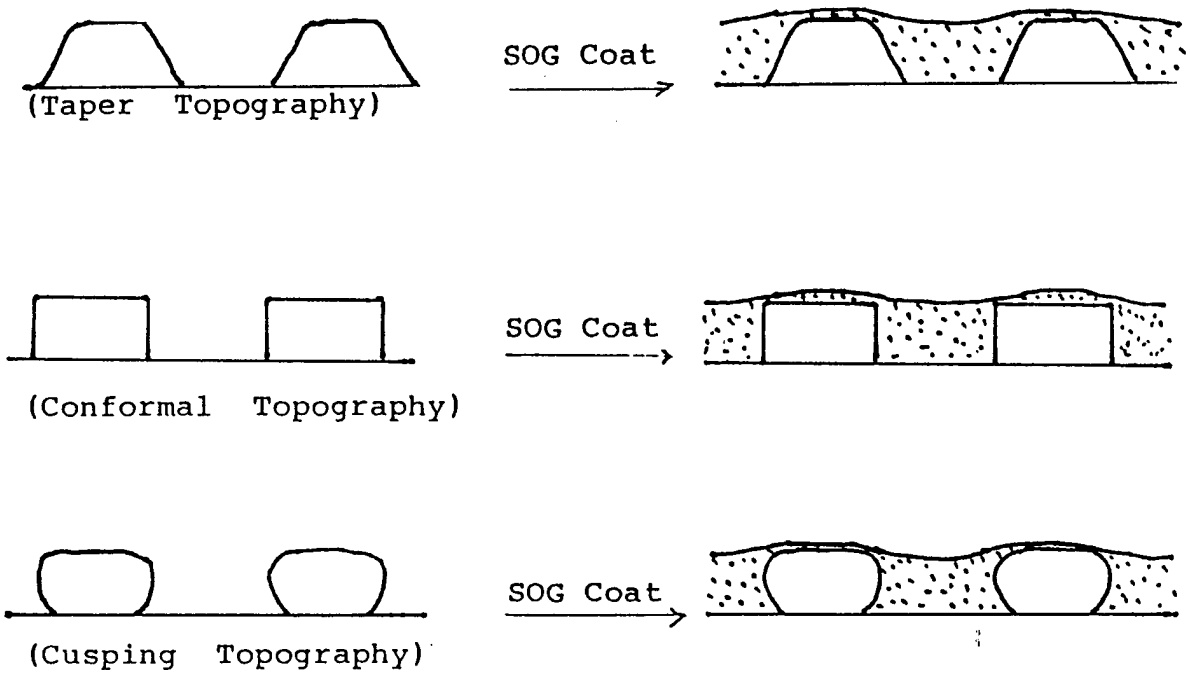
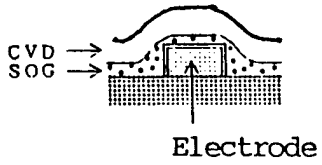


Fig. 1

Even the same step coverage, lines, and spacings as described above, different step coverage and planarization appear when deposited CVD films such as APCVD, LPCVD, P-TEOS, and O_3 -TEOS films, etc. on the different formed substrate(taper, conformality, cusping). Void formation will occur across the substrate with patterns of cusping, but this can be prevented by multi-layer coat and a lot of bakings of different type coat liquids with solid concentration.

5. Planarization techniques using SOG is presented below: (Refer to Fig. 2 - 5)

5-1. Undercoat



* This method is not so popularized.

Fig. 2a

◎ When electrodes are polisillicon or metal at high melting point, polyside(processes under the Al)

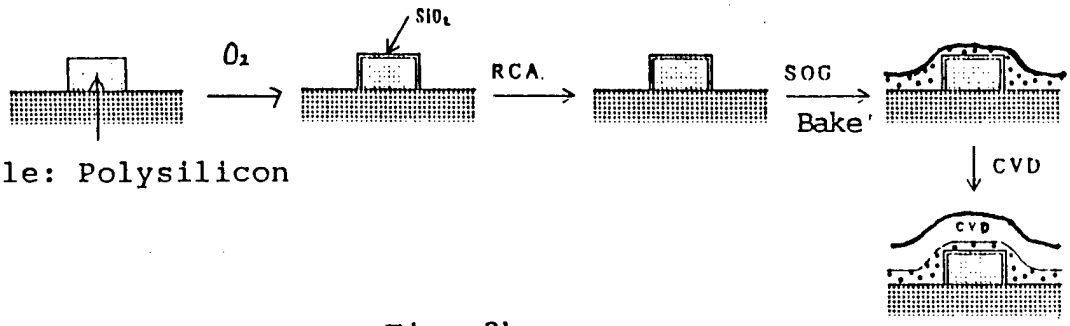


Fig. 2b

° When electrodes are Al or Al alloys(processes under the Al) * Semiconductor World, October, 1984, pp.129-133 by Jun Kanamori(Oki Electric Co.)

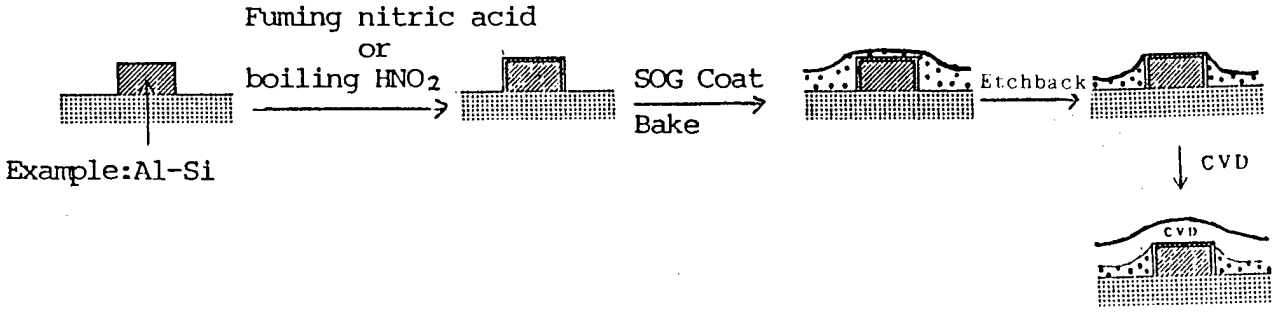


Fig. 2c

5-2. Overcoat

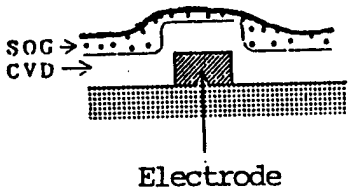
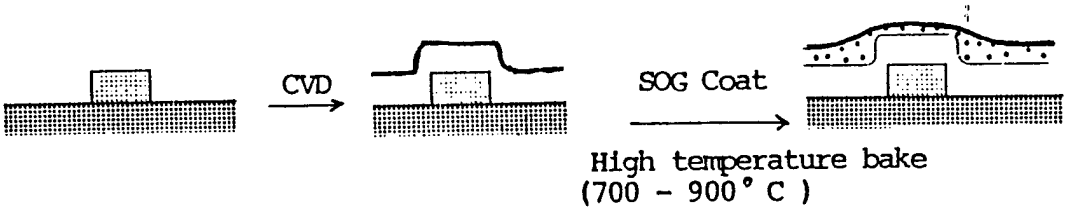


Fig. 3a

* In processes available for high temperature bake under the Al, that is, at 700 to 900°C, the overcoating method is employed for the same purpose as phosphosilicate glass (PSG) and Borophosphosilicate glass (BPSG) to be generally "reflowed".

° Process under the Al



Example: Polysilicon, polyside, metal at high melting point

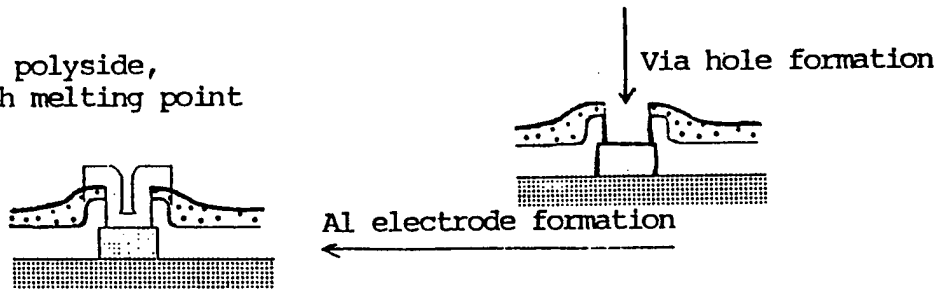
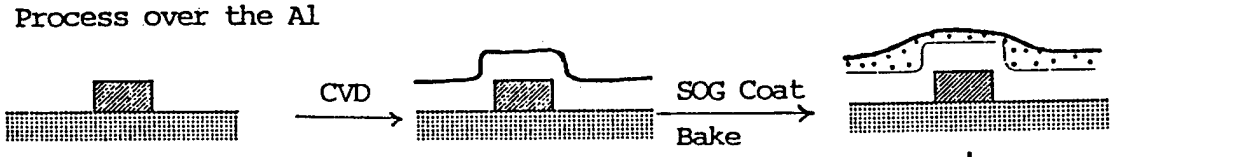


Fig. 3b

° Process over the Al



Example: Al-Si

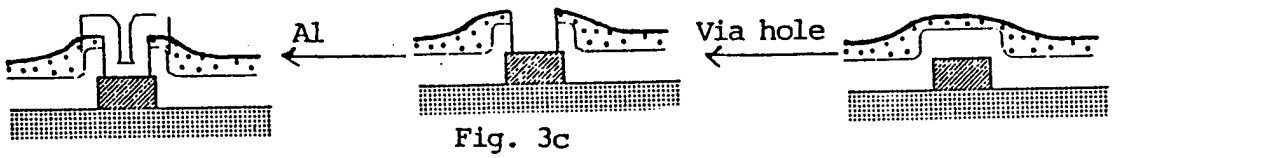


Fig. 3c

5-3. Sandwich process

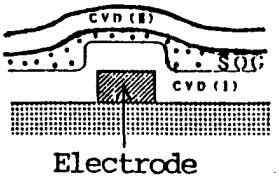


Fig. 4a

* This technique is often used in processes over the Al.

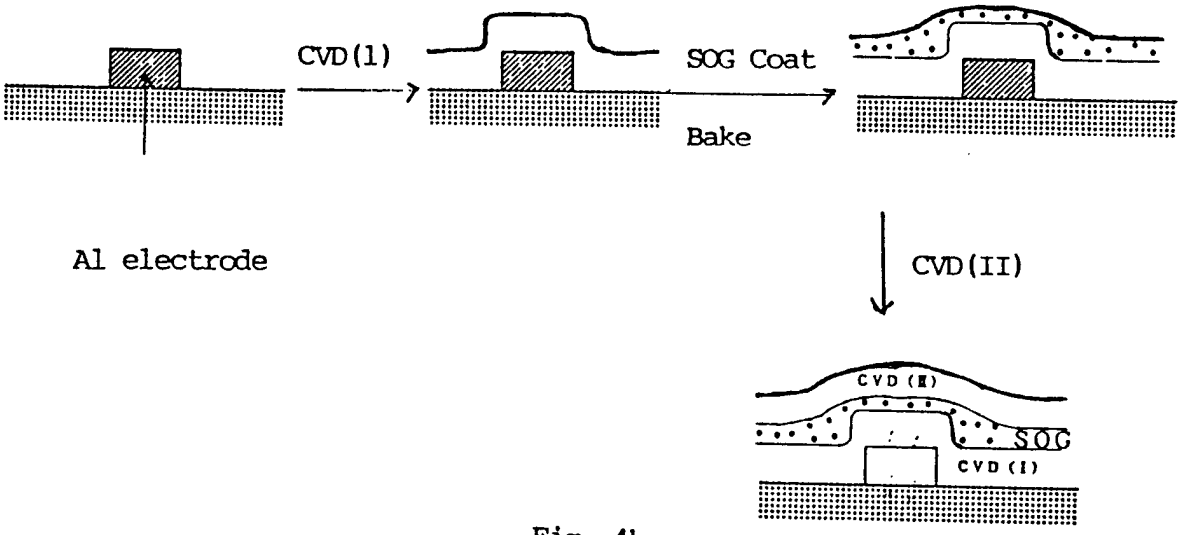


Fig. 4b

5-4. Etchback processes(E.B.)

* Etchback processes were used initially around the time when via holes became submicron technology sizes and this is used aiming at entirely no affection of moisture absorption, degas in device processes on the Al which the high temperature bake is not allowed.

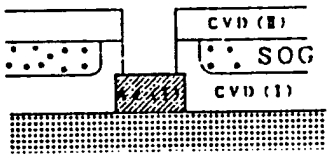


Fig. 5a

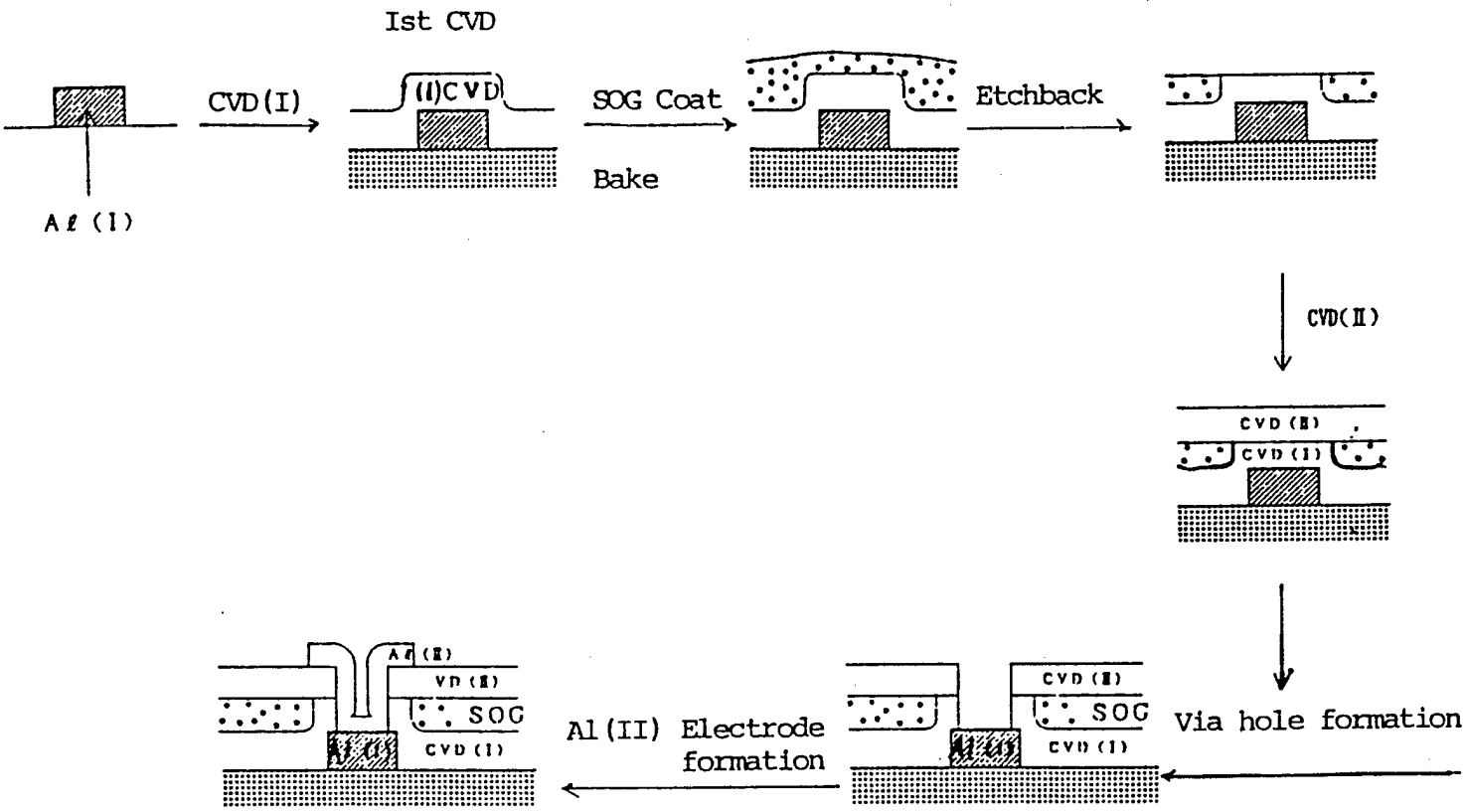


Fig. 5b

6. Several points to introduce planarization by SOG techniques

   A. Judgement of planarization and cracking resistance
   B. Surface processes prior to SOG coat
   C. Baking of SOG films and processes for enhancing film quality
   D. Judgement of stress by a combination of electrode materials, CVD films, and SOG films.
   E. Processes at the formation of via holes and contact holes.
   F. Prevention of particle production and usage of spin coater
   G. Selection control of SOG materials

7. Table 1 shows the generation flow on devices by the intermetal dielectric technologies for planarization combining CVD processes with SOG process.

Table 1

Design rule (Example:DRAM)	SOG(OCD)						Combined types of CVD	Etchback employing rate (estimatic
	Inorganic SOG(OCD T-2)			Organic SOG(OCD) T-7)				
	SiO concentration(wt%)	Film thickness	Coating	Solid cencentration(wt%)	Film thickness	Coating		
2.0μm (64K)	5 - 6 wt% (1000 - 1200Å)		1 = 2 times	———			AP-CVD LP-CVD P-SIN	0 - 1%
1.2μm (256K)	3 - 5 wt% (400 - 1000Å)		1 - 2 times	———			AP-CVD LP-CVD P-SIN PE-CVD	2 - 4%
1.0μm (1M)	2 - 5 wt% (200 - 1000Å)		1 - 3 times	6 - 20 wt% (1000 - 7000Å)		1 time	AP-CVD LP-CVD PE-CVD	5 - 10%
0.8μm (4M)	1 - 5 wt% (100 - 1000Å)		1 - 3 times	6 - -7 wt% (1000 - 5000Å)		1 - 2 times	AP-CVD LP-CVD PE-CVD P-TEOS O_3- TEOS	20 - 30%
0.5μm (16M)	1 - 4 wt% (100 - 800Å)		1 - 3 times	6 - 17 wt% (1000 - 5000Å)		1 - 2 times	AP-CVD LP-CVD PE-CVD P-TEOS O3 -TEOS	50 - 60%

AP - CVD : Atmospheric pressure SiH_4 CVD(NSG, PSG)

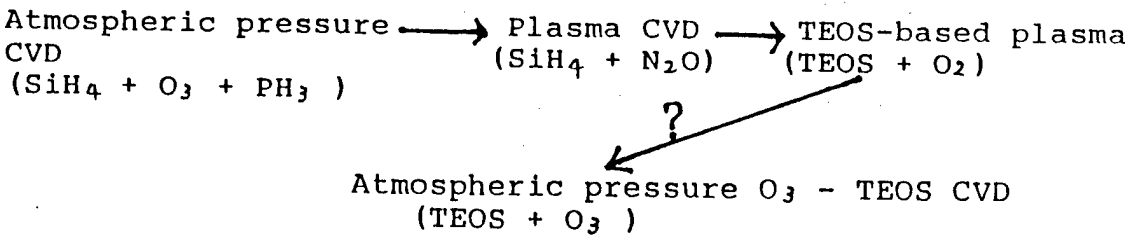
LP - CVD : Reduced pressure SiH_4 CVD(NSG, PSG)

PE - CVD : Plasma SiH_4 CVD(NSG, PSG)

P-TEOS : Plasma-enhanced TEOS CVD(NSG)

O_3 - TEOS : Atmospheric pressure TEOS CVD(NSG, PSG, BPSG)

With the generation flow of fine line patterning and the intermetal dielectric in multilevel metal technologies as described above, CVD processes combined with SOG processes have been diversified. The next industry challenge for 4MDRAMS seems to give priority to p-TEOS CVD and amospheric pressure O - TEOS CVD for 16MDRAMS is also expected to play a major role in the fabrication of semiconductor devices.



8. Characteristic comparison between inorganic SOG (OCD T-2) and organic SOG(OCD T-7): Rerfer to Table 2

Table 2

Itmes \ SOG Type	Inorganic SOG (OCD T-2)	Organic SOG (OCD T-7)	
Reliability	○~◎	△~○	
High temperature resistance(500 - 900°C)	◎	X~○	(mainly on the Al)
Cracking resistance (1 coating/limit)	△~○ (~ 2,000Å)	◎ (~ 2,000Å)	
Moisture absorption	X~○	○	
Etching characteristics wet	Fast ~ slightly slow	Slow	
Etching characteristics dry	Slow	Fast	
Dielectric constant	6 or more(high)	3.5 or more(low)	
Applied processes	Mainly non-etchback	Mainly etchback	

9. Processes proposed by TOK

9-1. Proposal of the overcoat by processes combining inorganic SOG(OCD T-2) with processes for enhancing its film thickness.

O TEOS CVD dielectric films are originally processed by the CVD technologies for planarization, which are therefore, expected as the satisfactory technique in every respect by a simple use: Due to planarization methods for the surface chemical reaction fabrication in principle, the planarization in the fine line patterning is excellent as shown in Fig. 6, but it is said that planarization in the wide line patterning will have some problems.

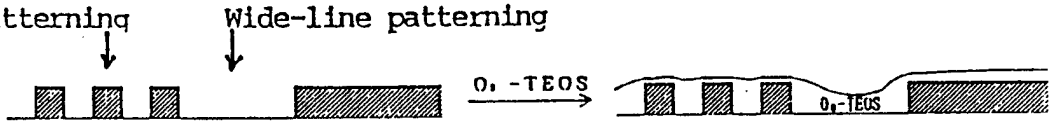


Fig. 6

Here, overcoat processes by O_3 - TEOS + SOG as shown in Fig. 7 are proposed.

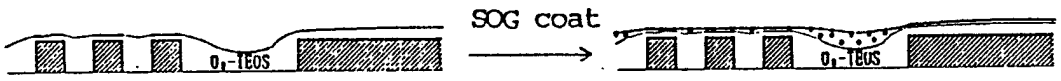


Fig. 7

However, when establishing directly Al(II) interconnections on that low temperature bake SOG layer (700°C or less), organic constituent and water stayed behind in the SOG layer between the SOG layer and Al(II) at sputtering are catched up with the Al(II), thereby troubles of dry etching and contact patterning, and etching between Al(I) and Al(II) will likely occur.

Therefore, for conventional CID(I)/SOG/CVD(II) sandwich processes, inorganic SOG(OCD T-2 developed product) as high grade films is proposed, including the overcoating method of P-TEOS + O_3 - TEOS + SOG processes combining plasma processes or O_3 processes to enhance the film quality further "after fabrication". (Refer to Fig. 8)

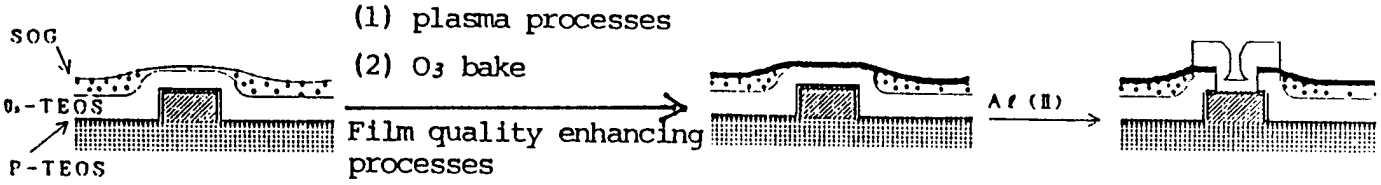


Fig. 8

Of course, it is considered that this technique is applied not only for O_3 - TEOS CVD but a combination of AP, LP, PECVD films with SOG overcoat processes, and expected as a simplified method than sandwich processes.

* Film quality enhancement of inorganic SOG film by plasma-enhanced deposition.
  Refer to:
  Patent disclosure "89-181533(Toshiba)
  Patent disclosure "89-25543(Hitachi)
* Film quality enhancement of inorganic SOG film with O_3 . (Refer to Table 3)

9 - 2. Proposal of planarization method by using organic SOG(OCD T-7)

(1) If the device systems are allowed, non-etchback processes by the high temperature vacuum bake method are preferable.

(2) As shown in Fig. 5b, " etchback, sandwich processes" such as P-TEOS, O_3 -TEOS, APCVD, LPCVD, etc. are proposed.

Table 3

OCD coat Bake ~ 140°C, 30min.

Film quality enhancing processes(O_2 , UV, O_3 /UV)

Bake (400°C, 30min., in N_2)

Measurement of etching rate (0.25% HF, 25°C)

OCD (Type-2)	Reference	O_2	UV	O_3 /UV
Si - 59000 - SG	870	250	390	240
P-59320 - SG	430	230	290	230
P-59350 - SG	1650	410	1370	490

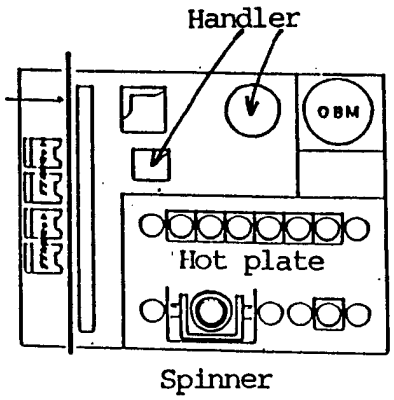
* Coating liquid for P.S.G.

10. An integrated SOG process system

With the advancement of device fine line patterning multilevel metal planarization methods, contact failure issues such as contact holes, via holes, the use of Si-nodule, stress migration, hillock, and various barrier metals for reflection preventive measures have advanced a multi-process system. Process equipment is getting to be a multi-process system. For SOG processes, the introduction of a single process equipment(spinner, postbake, prebake) is decreasing.

Under the above circumstances, simple schematic diagrams and functional examples of SOG integrated equipment being already marketed by TOK and several types which seem to be introduced for future development are shown below. (Refer to Example 1 - 4)

Example 1



OBM function

(1) Bake (200 - 600 C)

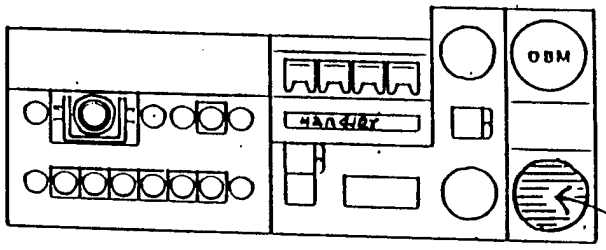
(2) Ramping bake

(3) Vacuum bake

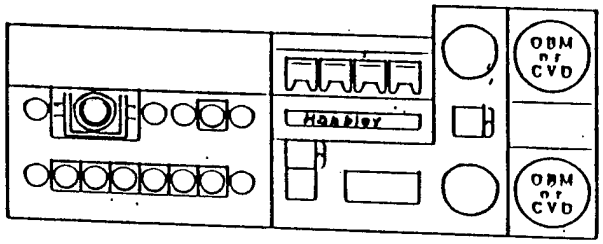
(4) Introduction of various kinds of gas

(5) Thermal uniformity is kept decreasing the airflow by the vertical type

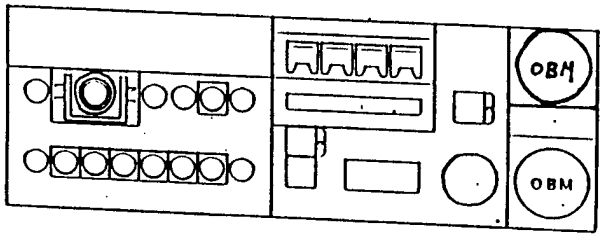
Example 2



Example 3



Example 4



11. NIKKEI Michrodevice, May 1990,p.42

An intermetal dielectric in two level metal technology for 0.5μm generation

Table 4

Maker	NEC	TOSHIBA	HITACHI	FUJITSU	MITSUBISHI	MATSUSHITA	OKI	SONY	SHARP	SANYO
Al-Al intermetal dielectric	P-TEOS SiO SOG P-TEOS SiO	①P-TEOS SiO [E.B] ②P-TEOS SiO [E.B] Planarization Film	P-TEOS SiO Inorganic SOG [E.B] P-TEOS SiO	P-SiO Organic SOG P-SiO	P-TEOS SiO AP O_3-TEOS SiO SOG[E.B] P-TEOS SiO	①P-TEOS *15 ②AP O_3-TEOS SiO *15	AP O_3-TEOS SiO	P-TEOS SiO O_3-TEOS SIO [E.B]	P-TEOS SiO SOG[E.B] *16 P-TEOS SiO	P-TEOS SiO [E.B]

E.B. represents that etchback processes are present.

(1) - (2) : Priority order

* 15: A combination of SOG or etchback

* 16: Double coating

As seen in Table 4, about half of those makers are expected to employ SOG processes as an intermetal dielectric planarization for 0.5um generation. However, 80% or more of makers is expected actually to introduce the SOG processes.

References:

(1) Quoted from Semicon News, June, 1989, pp.49-55 by Kazuo Maeda.

(2) Semicon News, June, 1989, p.54

(3) Draft of the lecture at th e autumnal Applied Physics related federation, 1989,p.976, 30p-D-2

Al ALLOY METALLIZATION for ULSI's

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1.Introduction

As device dimension miniatuarizes, requirements for individual technologies that constitute the LSI fabrication process become formidable. In order to meet the requirements in Al metallization, some efforts to improve the Al alloy metal line have been taken, such as stacked structures with refractory metal compounds[1], impurities incorporation to Al, and so on. The stacked structure has been employed in 1Mbit DRAM by some device manufacturers. Cu incorporation into Al alloy became prevailing in submicron level LSI's. In addition to Cu, recently, Pd[2,3], Ti[4-6], F[7] etc. have been reported to improve Al properties.

In this paper, requirements for Al alloy metal line will be discussed. Then, impurities incorporation to Al will be chosen from the technologies that meet those requirements, and the results will be shown in detail.

2.Requirements for the metallization technology

Al line width became less than 1 μm in 4Mbit DRAM level devices, and in this line width, various problems that were trivial in wider width metal lines became serious. These problems along with requirements for Al metallization are shown in Table I. Among these problems, the stress-induced migration is the most serious recently. There are several methods to solve these problems in addition to the stacked structure described above. That is, Al alloy line wrapped with refractory metals[8], Al alloy lines with intermetalic compounds in interlayer[9], and so on. The fabrication processes, however, become complicated in these methods, and it is desirable to use the single layer strengthened Al alloy line. In this paper, Al alloy interconnects containing Hf and B were chosen and investigated[10].

3.Hf and B addition to Al-Si-Cu alloy

3-1.Why Hf and B?

When impurities are doped in Al alloys, care must be taken not to spoil the Al properties. Cu is a popular effective dopant for this purpose. But, too much Cu doping will have a serious influence on the fine-line patternability. In this experiment, we try to improve Al-Si-Cu alloy films in respect of hillock suppression and void formation. Cu content of Al alloy films is 0.5wt% to keep electro-migration resistance and patternability.

Why were Hf and B chosen for doping impurities? In bulk materials, it is well known that the mechanisms shown in Table II are effective to pin dislocation motion and to suppress the self diffusion of the matrix element[11]. By impurity doping, solid solution strengthening, dispersion hardening, and precipitation hardening are mainly effective for strengthening metals. Among these, we paid attention to precipitation hardening to improve the Al alloy film quality because it will not increase the film resistivity. In this respect, the precipitation of stable compounds of transition metals such as borides, nitrides and carbides with only a small amount were thought to be effective for this purpose. Table III shows the standard free energy of formation of borides, nitrides, and carbides of 4a, 5a, and 6a group transition metals. Hafnium-boride is the most stable among the compounds listed here. Moreover, the melting point of Hafnium chlorides is lower

than that of Copper chlorides. This means that etching of the Al alloy containing Hf and B will not be difficult. From these respects, we chose Hf and B as doping elements.

3-2.Effects of impurities doping

Al alloy films of 0.7 to 1.0μm were deposited on BPSG film on Si substrates by a DC magnetron sputtering system. A small amount of Hf(200ppm) and B(400ppm) were added to Al-Si-Cu alloy simultaneously or seperately.

First, the effects on the hillock formation will be discussed. The temperature-stress curves of the different Al alloy films on the SiO_2/Si substrates were measured by the in-situ wafer curvature measurement. Figure 1 shows the results of three Al alloy films(Al-1%Si, Al-1%Si-0.5%Cu, Hf and B added Al-1%Si-0.5%Cu) in one temperature cycle. As increasing the sample temperature, the stress changes at first from tensile to compressive because of the difference in expansion coefficients of the metal alloys and substrate. And then, the elastic range has been exceeded. The arrows in the figure indicate the transition temperatures from elastic to plastic flow of the metal alloys. At these temperatures, hillocks begins to form. The temperatures are different on each samples. That is, around 100^{o}C for Al-Si, about 200^{o}C for Al-Si-Cu, and about 300^{o}C for Hf and B added alloy. The transition temperature becomes higher because of the Hf and B addition.

Figure 2 shows the vertical hillock height distribution measured by Taly-step after annealing at the range from 200^{o}C to 350^{o}C for 5min. As the annealing temperature increases, the number of hillocks increases. The hillock formation occurs at less than 200^{o}C for Al-Si, and at about 200^{o}C for Al-Si-Cu, and 300^{o}C for Hf and B added sample. These temperatures coincides well to the transition temperatures shown in figure 1.

Figure 3 shows the lateral hillock length distribution of 200μm width metal lines estimated by the optical microscope. The effect of Hf and B addition on lateral hillock formation is clearly seen.

Those observation indicates that the Hf and B addition into Al-Si-Cu raises the temperature of the plastic flow of the material and suppresses the hillock formation.

The migration resistance of the metal lines has been measured. Figure 4 shows the number of voids formed in the 1μm width metal lines during aging test at 125^{o}C. The voids were discerned when they were larger than one-third of metal line width. The number of voids in metal lines increases with the aging time. The trend, however, varies in the kinds of metal alloys. The Hf and B addition suppresses the formation of voids in metal lines. Although, not shown in the figure, the sample only Hf added has almost the same number of voids as the Al-Si-Cu sample.

Four kinds of metal materials have been tested for the electro-migration(EM) resistance. The results of EM measurements are shown in Figure 5. The sample only Hf added has about 100 times longer life time than Al-Si and it is longer than Al-Si-Cu. The Hf and B simultaneously added sample has a few initial failures, but after that, the samples do not have any failures until the testing time of 2500 hours when the test was suspended.

3-3. Existance state of Hf and B

Next, the relation between existence state of Hf, B and the addition effects will be discussed.

Because the amount of impurities are too small, we can not identify the location of impurities and the compound of added impurities in the films. Therefore, for a reference, bulk Al alloys were evaluated by EPMA. Figure 6 shows the SEM image and X-ray images of the Al-Si-Cu with Hf at the same area of the sample. From the SEM and Si Kα images, Si precipitates at grain boundaries. Cu Kα image shows the Cu dissolves in Al matrix and the concentration is higher at near Si precipitates. And, Hf also dissolves in Al matrix and some are segregated at the Si precipitates.

Figure 7 shows the case of Al-Si-Cu with Hf and B. Also in this case, Si precipitates at the grain boundaries. And Cu dissolves in Al matrix, and also precipitates at grain boundaries, though it is not shown in the photograph. From the Hf Lα and B Kα images, Hf and B existed at the same location, and the location differes from that of precipitated Cu.

From these results in addition to the low free energy of formation, we can speculate the

possibility of Hafnium boride formation seperated from Cu.

As the final subject in this section, the influence of precipitated Hafnium boride on Al alloy properties will be discussed.

Table IV shows the grain sizes of the as-dposited and sintered Al alloys, and also shows the resistivities of as-deposited films. Hf and B addition greatly reduces the grain size of the as-deposited Al alloy film. The grain size after 400^{o}C annealing also shows the fine grain structure, and Hf and B addition of a few hundreds ppm order is effective not only to reduce the grain size of the as-deposited film but also to suppress the grain growth during sintering. The resistivity of the sample has no increase compared with that of Al-Si-Cu film.

A brief summary of existance state of impurities and their effects will be given as follows. In the case of only Hf added Al alloy, Hf dissolves in Al matrix. But, in the case of the simultaneous addtion of Hf and B, Hf and B precipitates as Hafnium boride. However,the effect is different between two materiols. In both cases, impurities addition causes the fine grain structure. With the Hafnium boride precipitation, Hafnium boride precipitation and the fine grain size improve the Al alloy quality. And for the electro-migration, Hafnium-boride precipitation effect is greater than the degradation caused by the grain size effect.

4.Conclusion

Al alloy interconnects containing Hf and B as doping impurities has been investigated. A few hundreds ppm order of Hf and B addition into Al-Si-Cu alloy greatly improves the hillock formation during heat treatments and the stress-induced void formation during aging test without degrading the Al alloy properties such as the patternability, low ohmic contact resistance, and so on. Hf and B are thought to be precipitated as Hafnium-boride in Al alloy film. This precipitation effect contributes to the imprvement of Al alloy interconnects.

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- ○ Low Resistivity
- ○ Low Rc
- ○ Good Adherence
- ○ Fine Line Patternability
- ○ Resistance to EM / SM
- ○ Resistance to Hillock Formation

Table I Requirements for Al interconnects.

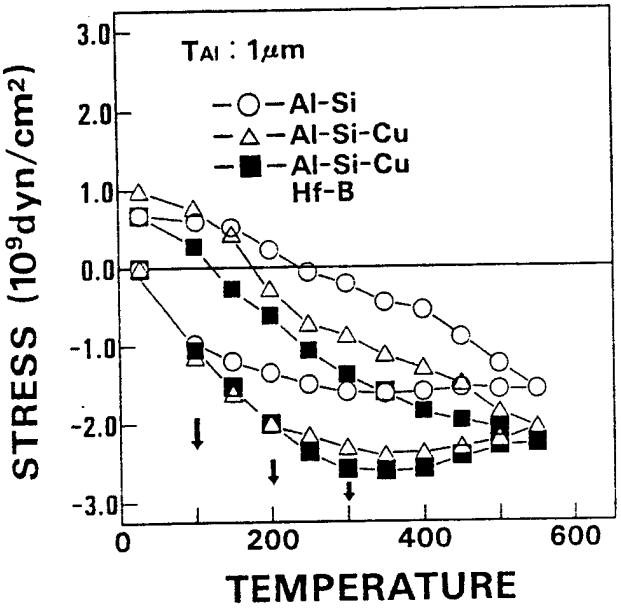

Fig.1 Temperature-stress curve of Al alloy films.

- ○ Strain Hardening
- ○ Grain Boundary Strengthening
- ○ Solid Solution Strengthening
- ○ Dispersion Hardening
- ○ Precipitation Hardening

Table II Metal strengthening mechanisms.

	Standard Free Energy of Formation(Kcal/mol)		
	BORIDE	NITRIDE	CARBIDE
Ti	−69.1	−73.6	−54.4
Zr	−76.2	−80.5	−47.1
Hf	−85.0	−81.4	—
V	−61.3	−53.7	−24.5
Nb	−61.6	−54.8	—
Ta	−46.2	−58.7	—
Cr	−30.0	−21.6	−63.1
Mo	−50.7	−22.3	−16.8
W	−37.5	−13.0	−13.5

Table III Free energy of formation.

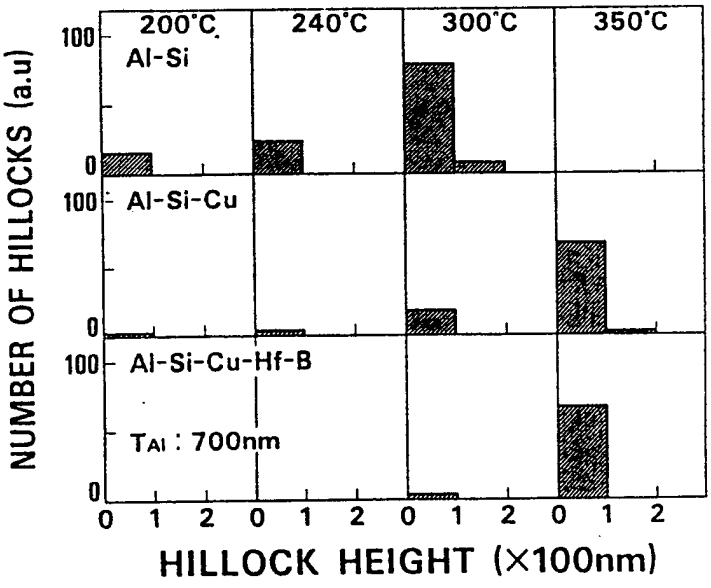

Fig.2 Vertical-hillock height distribution.

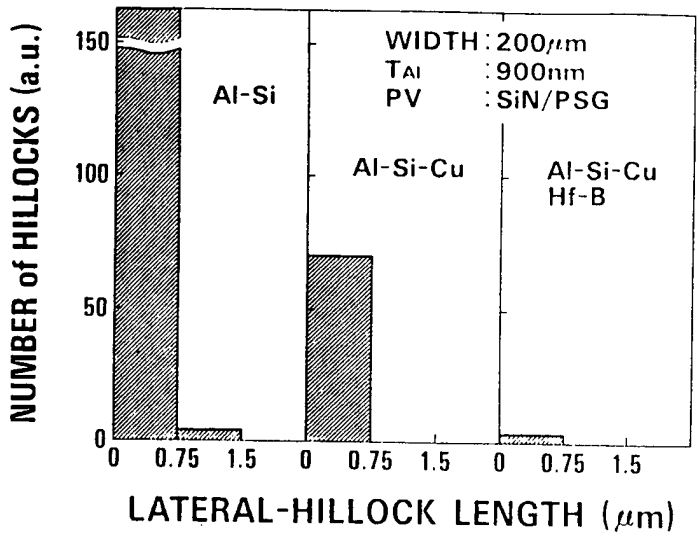

Fig.3 Lateral-hillock length ditribution.

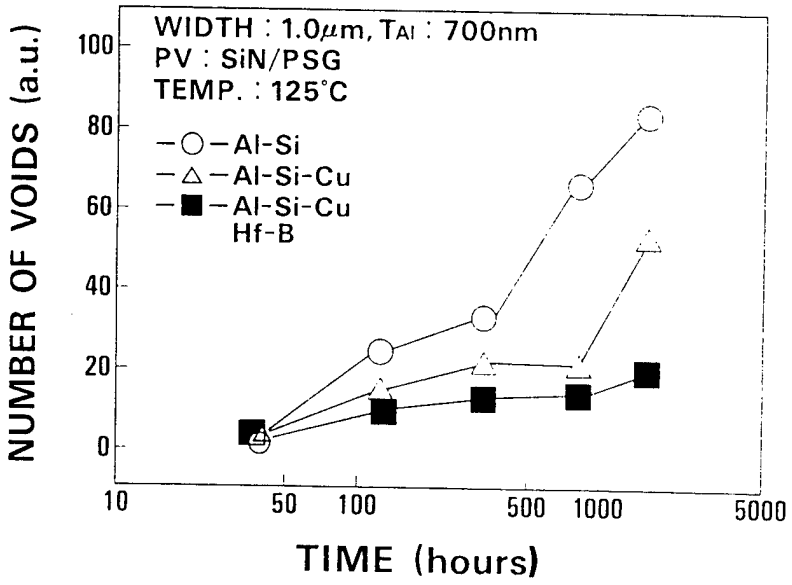

Fig.4 The number of voids formed in 1 μm width metal lines during aging test at 125^{0}C.

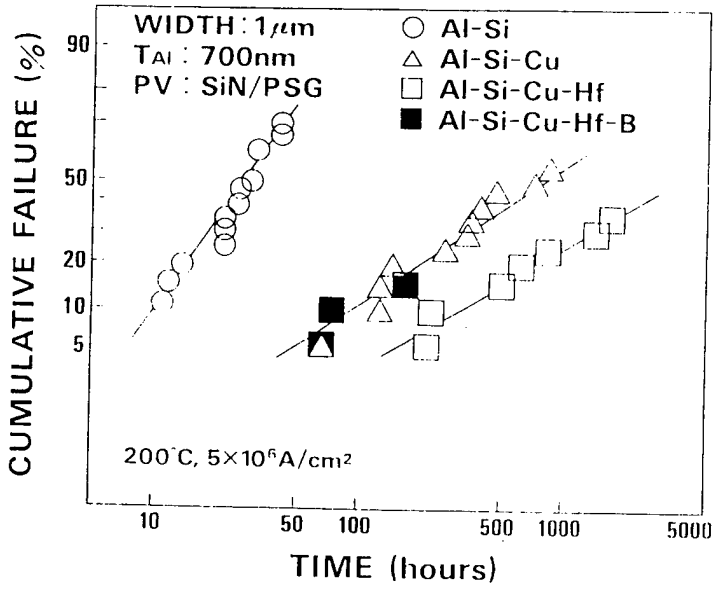

Fig.5 Weibul plots of cumulative failure rate in EM tests for 1 μm width Al alloy films.

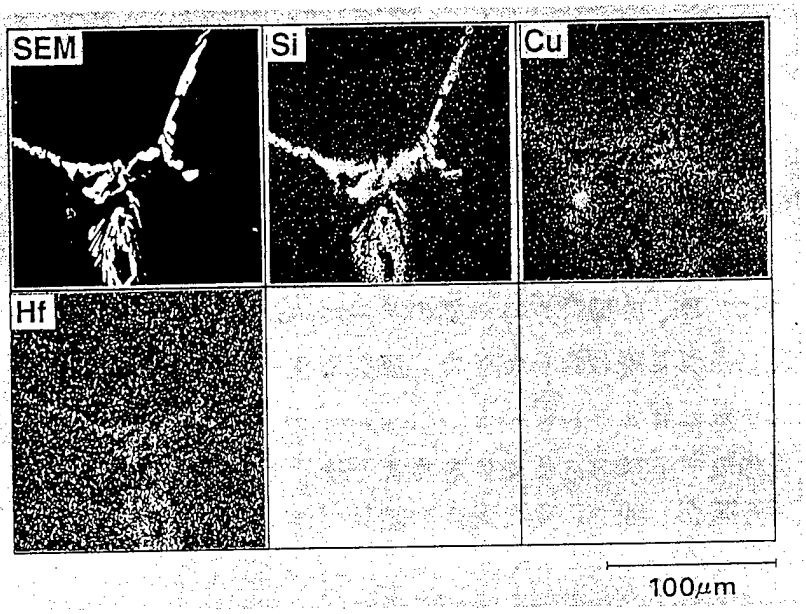

Fig.6 SEM and X-ray images of Al-Si-Cu-Hf alloy.

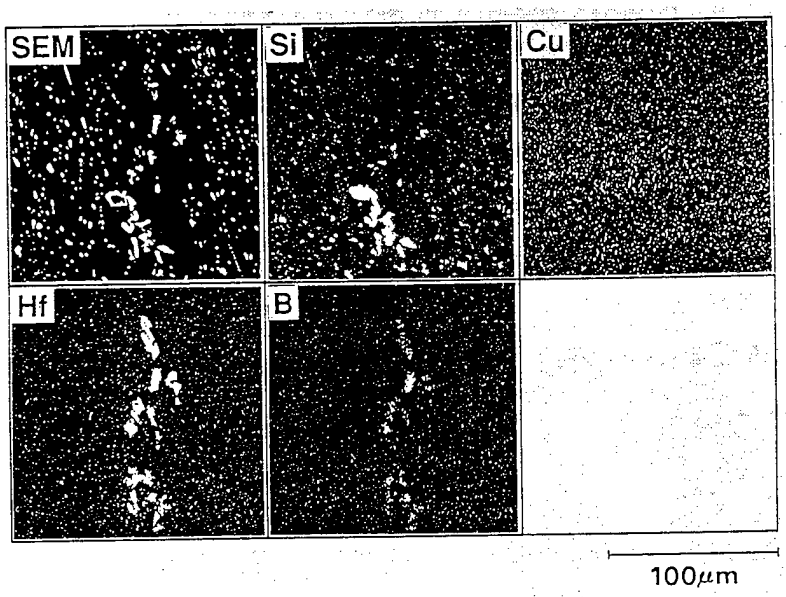

Fig.7 SEM and X-ray images of Al-Si-Cu-Hf-B alloy.

	RESISTIVITY as depo.(μΩ·cm)	GRAIN SIZE(μm)	
		as depo.	400°C 30min
Al-Si	2.95	1.03	2.47
Al-Si-Cu	3.21	0.87	1.80
Al-Si-Cu -Hf	3.10	0.68	1.60
Al-Si-Cu -Hf-B	3.18	0.44	1.26

Table IV Resistivity and grain size.

Selective Tungsten Growth Technology

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1. Introduction

In the past ten years, dry etching technologies employing low pressure plasma have been rapidly introduced into the ULSI production line, and they promoted the shrinkage of minimum device feature size. However, the manufacturing in the next decade necessitates thin film growth technology, not deposition, for various new materials. This is because, in the near future, present devices may become deadlocked without innovation related to materials, and also, from the aspect of process technology, the self-aligned silicon process technique based on selective thin film growth would be the key to future ULSI devices.

In order to realize highly selective thin film growth technology, it is very important to prepare a well controlled surface in situ, and to control interface reaction precisely. Considering these circumstances, many surface treatment techniques, such as native oxide removal, surface passivation, and so on. However, a mechanistic study on the origin of selectivity itself is not sufficient for clarifying the elementary process, and up to date, there seems to be no useful guiding principle to design a new selective thin film process. From the viewpoint of practical use, the purpose of the anthor's group is to make an original process and equipment by creating new source gases through a better understanding of the origin of selectivity, and also by preparing surface conditions fit for respective purposes.

This paper focuses on the limited issue of from where the selectivity is derived, and to propose one of the useful guiding principles for a new selective thin film process.

2. Electronic interaction between adsorbate and solid surface

2.1 Selective tungsten film growth

Figure 1 shows the cross-sectional view of a W film buried in n type and p type contact holes without a barrier metal. W film growth was carried out employing a WF_6 + SiH_4 mixture gas. The W film growth was accomplished accompanying the consumption of the Si substrate, and much of the n type Si substrate was consumed, as compared with the p type Si surface, as shown by an arrow in Fig. 1-a. Thns, the initial stage in the selective W film growth on n type and p type Si substrates has been investigated in order to understand why such a difference between the two kinds of Si substrate is derived.

Figure 2 shows the weight change in W, which was grown on the p type Si substrate, as a function of growing time. The W on the Si substrate was all dissolved in a HCl and H_2O_2 solution, and then, the weight gain was measured employing inductively coupled plasma mass spectroscopy. After a short induction time of about 10 seconds, the slope was nearly 1, which means that the W film growth occurred linearly in proportion to the surface area of a uniformly formed seed layer, as shown by an insertion in Fig. 2. On the other hand, the slope was 1.7 at the initial stage of the selective W film growth. This result means that the seed layer was formed accompanying an increase in the number of nucleation centers simultaneously with the nucleation growth itself.

Figure 3 shows the same data as Fig. 2, but expressed by a linear scale. When a WF_6 and SiH_4 mixture gas was used, the weight gain increased gradually with increasing growing time, and suddenly rose after a short induction time. On the other hand, when Ar was added to WF_6, instead of SiH_4, the weight gain only continued to increase at the same rate as the initial growth rate for the case of a WF_6 and SiH_4 mixture gas. This result demonstrates that WF_6 was reduced by the reaction with the Si substrate at the initial stage in the selective W film growth, even if SiH_4 was mixed with WF_6.

When W film growth was performed on an n type Si substrate, there existed no measurable induction time. However, the n type Si substrate was greatly consumed instead. The induction time means the length in which a uniform seed layer for further W film growth is formed. Considering the meaning of such induction time, it is concluded that the reduction in WF_6 for the n type Si substrate takes place faster than for the p type surface.

These results suggest that the electron transfer from the Si substrate to adsorbed WF_6 initiates the WF_6 dissociation process. Next, in order to obtain a more deep insight into the initiation of the WF_6 dissociation process, the W film growth was carried out on several polar material surfaces.

Figure 4 shows an optical photograph of respective material surfaces observed in the dark field as a function of electronegativity, which was defined as the arithmetic mean value of Mulliken's electronegativity for respective atoms constituting the individual insulators. As the bond property of the substrate material becomes ionic, W growth is not easy. However, selectivity is inclined to be lost when the growing time is prolonged. Taking these facts into account, the growing time was fixed at a relatively long 5 minutes. Many W islands, projected as bright spots in the photograph, existed on the SiO_2 surface. On the other hand, there is not a speck of W on the LiF substrate. In the case of Al_2O_3 and Si_3N_4 surfaces, the W islands combined with each other to grow into a relatively thick W film, but there remained a few W islands on the Si_3N_4 surface.

Considering the concept of electronegativity, Fig. 4 can be summarized as indicating that WF_6 molecule dissociates readily on the electron donating material surface. This conclusion was reconfirmed by comparing the induction time on respective material surfaces.

2.2 Possible mechanism for the WF_6 dissociation process

Figure 5 shows the possible mechanism for the WF_6 dissociation process based on the average electronegativity concept. Since fluorine atoms surrounding the centered W in the octrahedral structure of WF_6 have a larger electronegativity, fluorine atoms pull the valence electrons from the Si substrate. As a result, relatively strong bondings between F and Si (96 kcal/mol) are formed, accompanying the bond breaking between F and W (69 kcal/mol), which results in a fluorine containing seed layer on the Si surface, and simultaneously releases unsaturated molecules, such as $WF_{x(x=5)}$. The resultant WF_x molecules dissociated sequentially on the clean Si surface, due to the electron transfer controlled reaction.

At present, the donation or the backdonation level on the Si surface is not clear. However, according to this model, WF_6 dissociates readily on an n^+ Si surface rather than on a p^+ Si, because an n^+ Si substrate involves many free electrons near the surface. Actually, much of the n^+ Si substrate was consumed by the Si reduction of WF_6, compared with the p^+ Si substrate, as shown in Fig. 1.

Thus, by considering the origin of selectivity in selective W film growth, it has been found that WF_6 dissociation is preferentially initiated by electron transfer from the substrate surface to the adsorbate. This preferential dissociation, in turn, results in the selective seed layer formation for further W film growth. However, at present, the reason why the WF_6 molecule is decomposed by electron attachment remains unclear. However, its detailed mechanism will be clarified in the near future, by, for example, energy calculation for the adsorbed molecule on the respective materials, and then the dissociation process will be interpreted more universally.

3. Conclusion

One of the useful clues for the selective growth procedure has been proposed considering the reaction mechanism for W film selective growth. More precise understanding of the interface reaction will lead to the construction of a universal rule for selective thin film growth. In the future, a deep insight into the selectivity origin should put precursor design, surface modification, and so on to

practical use.

Acknowledgment

The author is grateful to H. Itoh, N. Kaji, T. Watanabe, N. Hayasaka, K. Horioka, T. Arikado, R. Nakata, H. Nishino, T. Yoda for their useful discussions, and M. Kashiwagi and K. Okumura for their continuing encouragements. He is also indebted to F. Umibe for giving valuable comments to the original English manuscript.

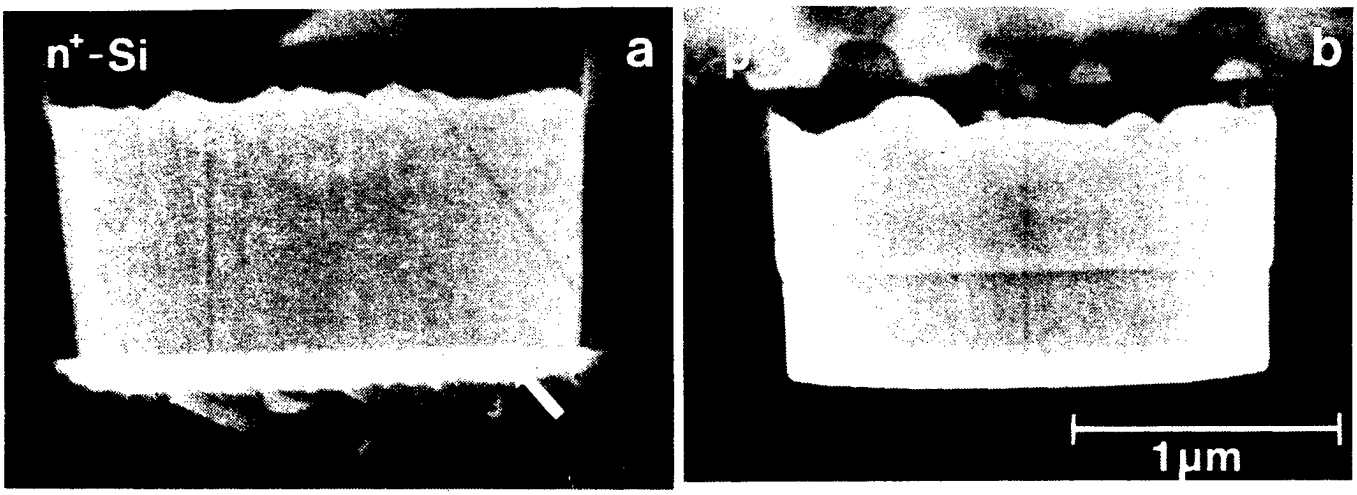

Fig.1 Cross - sectional view of W.

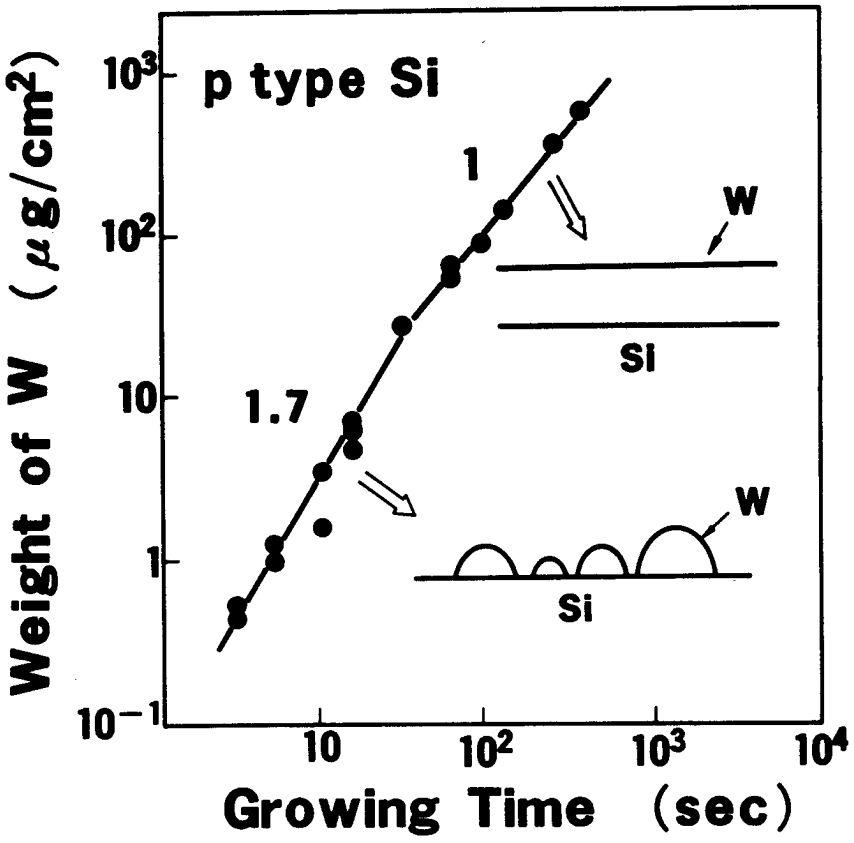

Fig.2 Weight change of W vs. growing time.

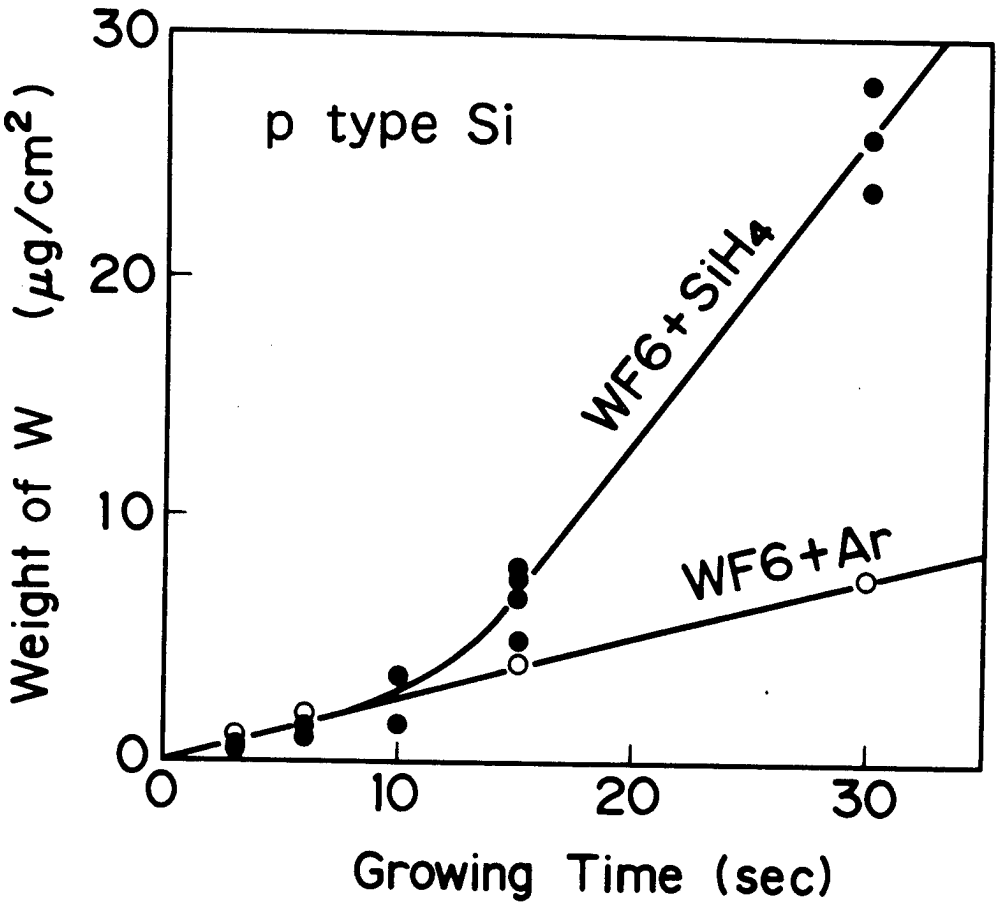

Fig.3 Weight change of W vs. growing time.

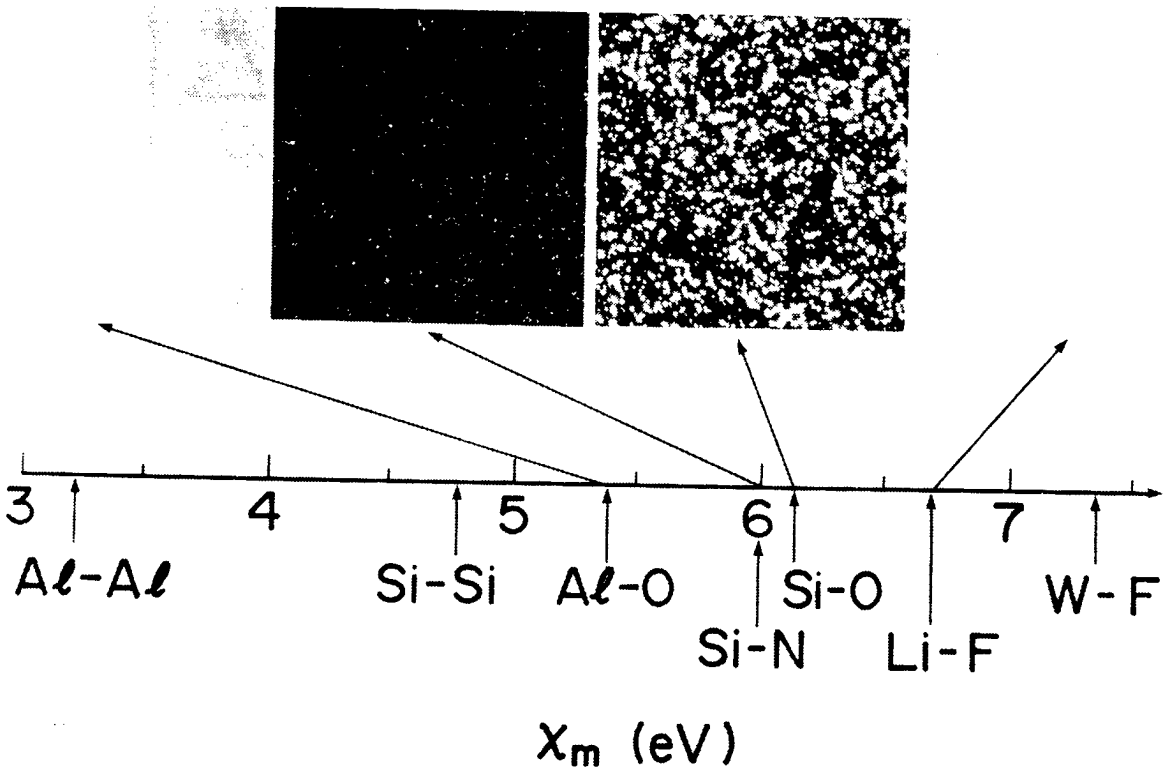

Fig.4 Optical Photograph of various polar material surfaces.

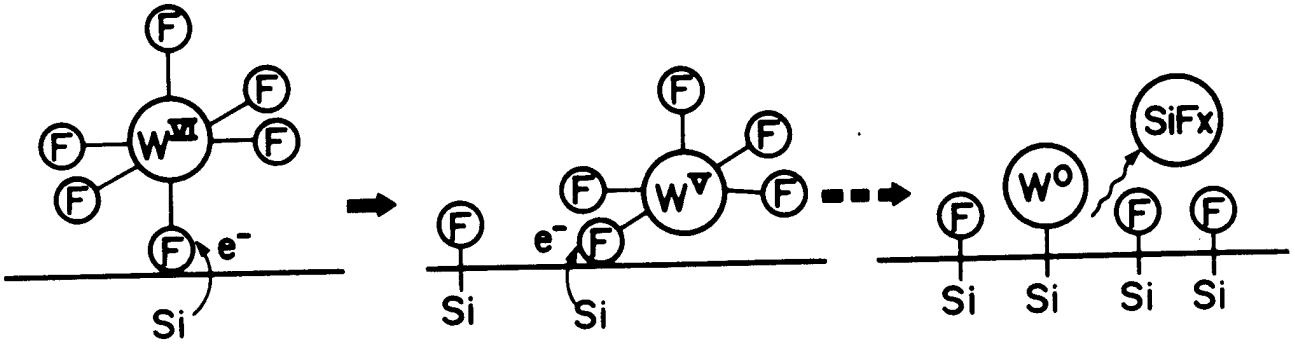

Fig.5 Possible mechanism of WF_6 dissociation process.

BIAS SPUTTERING FOR PLANARIZATION

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INTRODUCTION

New metallization materials and processes are required for ULSI interconnection. The requirement for these new metallization technology reflect device needs for improved performance with far greater reliability than has been achieved in VLSI.

However, to meet the requirement for mass production of ULSI, there are enormous hurdles impeding successful implementation of these new metallization materials and processes. Therefore, aluminum and its alloys will be still the key metallization system in ULSI.

Many efforts have been made to improve the step coverage of Al films to contact-hole and through-hole.(1)-(6) By the use of current technology, we have investigated the possibility of extending bias sputtering technology to the submicron metallization process.

A few of the key factors which are desirable for bias sputtering equipment include

1) Sputtering source providing uniform deposition condition all over the wafer,

2) Repeatable wafer temperature control system,

3) Ultra High Vacuum system,

4) Reliable RF bias control.

In this paper, one of sequential bias sputtering will be introduced for TiN / Ti / Al-Si(without bias) / Al-Si(with bias) system.

MULTIPLE-STEP BIAS SPUTTER PROCESS

Figure 1 shows multiple-step sputter sequence. The system consists of RF sputter etch having an independent pumping system and three deposition stations. Each stations has heater table with gas-assisted heating. Station of RF bias sputtering is accomplished by applying an rf power(13.56MHz) to heater table. Configuration of the rf-bias sputtering system is shown in Fig.2. At the first deposition wafers were sputter-etched and then 20 - 50nm of Ti was sputter-deposited. Wafers were transferred to the second deposition station heated below 150 degree C and deposited about 200 nm Al without bias.

The surface profile after this deposition is shown in Fig.3(a) SEM. The Al film is covered over steps. But at high temperature, no metals are appeared on side walls, as shown in Fig.3(b). This low temperature deposition is important for the next step being the deposition with RF bias at high temperature.

WAFER HEATER SYSTEM

The wafer was held to the face of a heater table by clips and the heating was accomplished by gas conduction, that is, the heat is transferred by Ar gas from the heater table to the wafer. It makes conduction of heat coupling better and raises the wafer temperature uniformly and reproducibility at sufficient gas introduction. We can see from Fig. 4 that the argon pressure should be above 1 mTorr. At condition of the required lower pressure deposition being under 1 mTorr,it is needed to improve more tight heat coupling.

RF BIAS SPUTTER SYSTEM

Figure 5 shows the dependence of the cathode power on the RF power, under the condition of constant of cathode self-bias. Figure 5(a) shows the case of constant source coil field strength. We have found that the relationship between cathode power and RF power is linear, and it is found experimentally that this relation is stable. As shown in Fig.5(b), in the case of variable source field strength, the dependence becomes very complicated, and also there are unstable.

Therefore the combined effects between RF power and source coil field strength should be minimized for the simple system for mass-production.

EFFECT OF A TI UNDERCOATING

Figure 6 shows typical SEM picture of multiple step bias-Al films. In this experiment, the sample had left in the air after TiN deposition by reactive sputter. Then, multiple-step bias deposition has been made under the 5 mTorr of Ar pressure. The base pressure of the vacuum chamber prior to deposition was 8 x 10 -8 Torr. The total Al film thickness was 0.8 micron and sequential time corresponds to the throughput of 40 wafers/hours. In case of providing Ti on underlayer, the following two step Al films (no-bias Al/bias Al) was uniformalized the grain boundary on steps compared with non-Ti case and abnormal material in the grain boundary varnish and become smooth surfaces.

CONCLUSION

Improvement of a continuation of the present sputter equipment is important because a new metallization materials and processes in ULSI has not been established yet.

Recently new equipment of multi-chamber system and cluster system has come to mass-production. In such an equipment, the optimization of sputter process such as the low-pressure deposition will be achieved with good condition before high temperature Al deposition without bias or with bias.

In device development, it will contribute one of the metallization technique by sputtering thechnology.

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MULTIPLE-STEP BIAS SEQUENCE

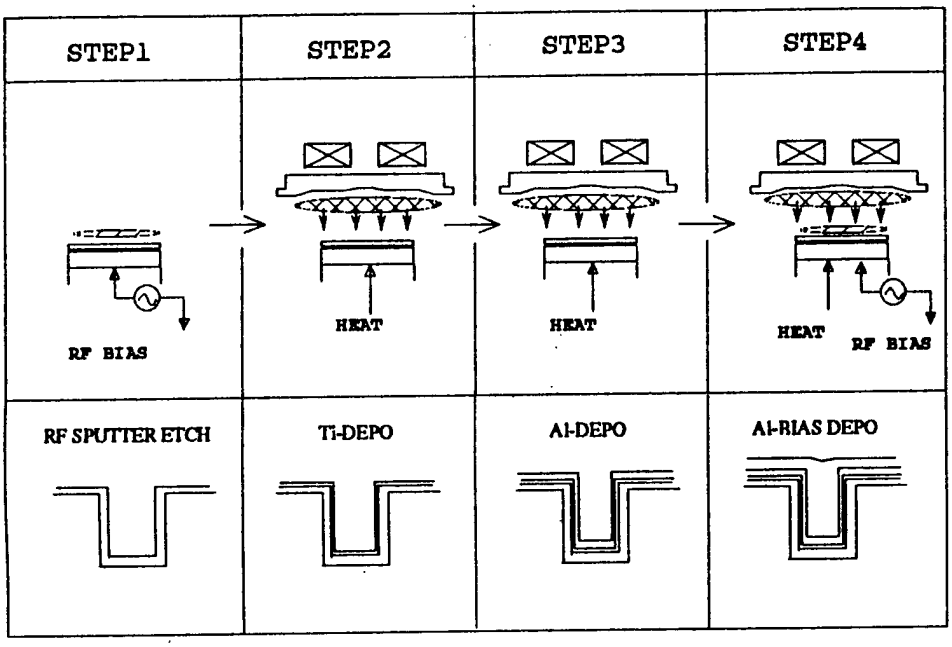
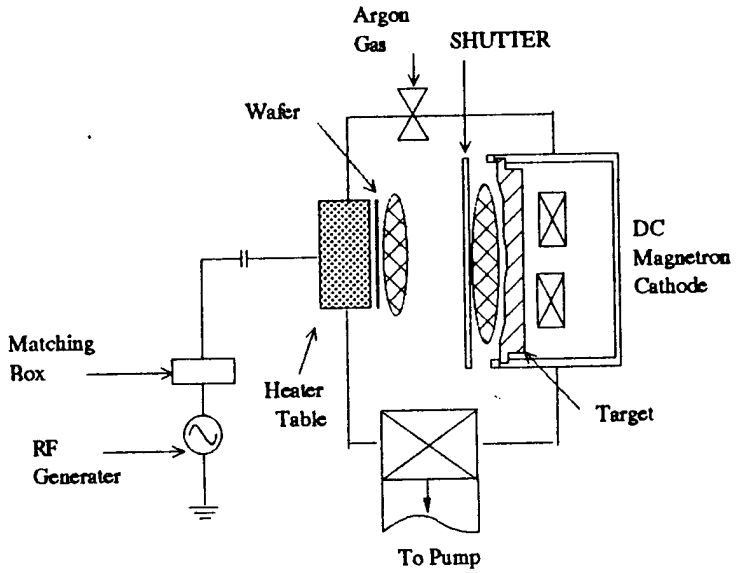
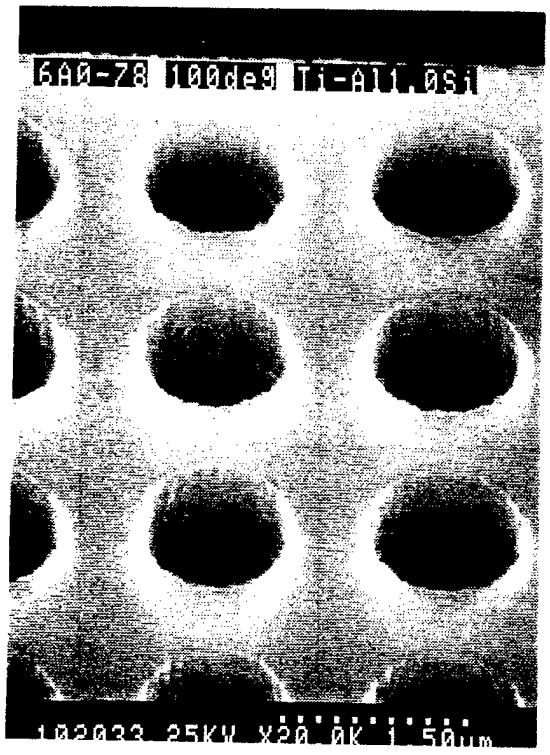


Fig. 1 Multiple bias sequence Diagram

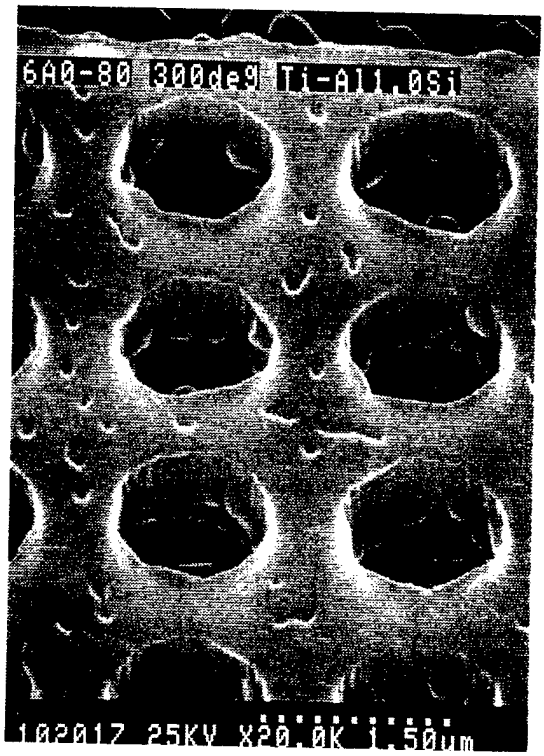


RF-BIAS SPUTTERING SYSTEM

Fig. 2 Configuration of RF bias sputtering System



(a) 2000Å-Al at 100°C



(b) 2000Å-Al at 300°C

Fig. 3 Thin-Al over Ti at 100°C and 300°C

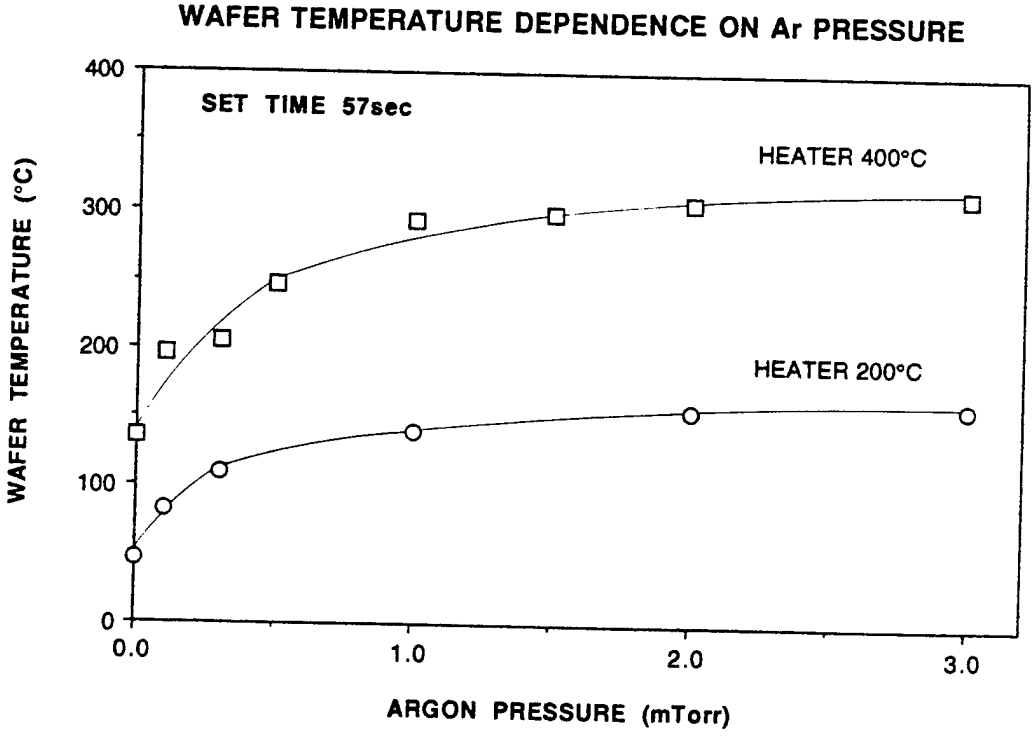
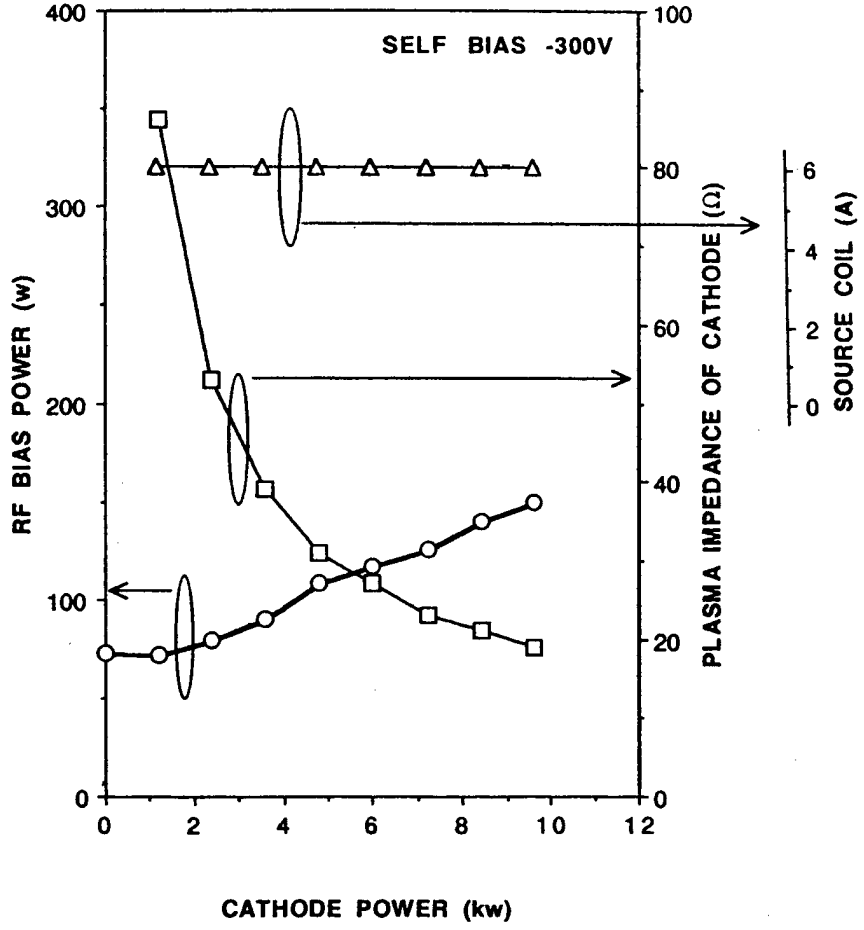
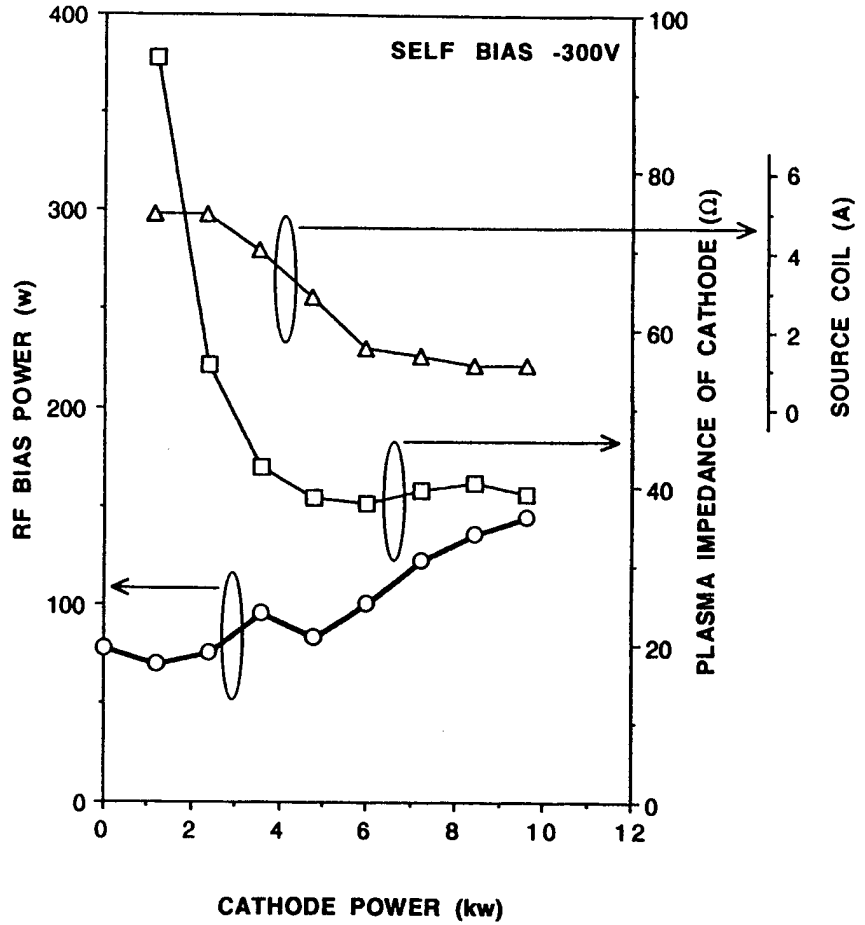


Fig. 4 Wafer Temperature dependence on Ar



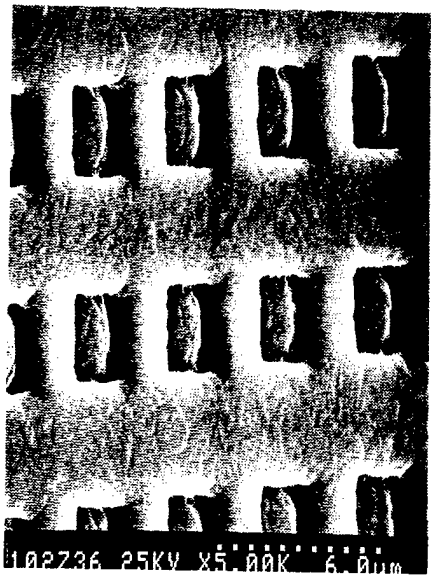
(a) Under Constant Source Coil Current



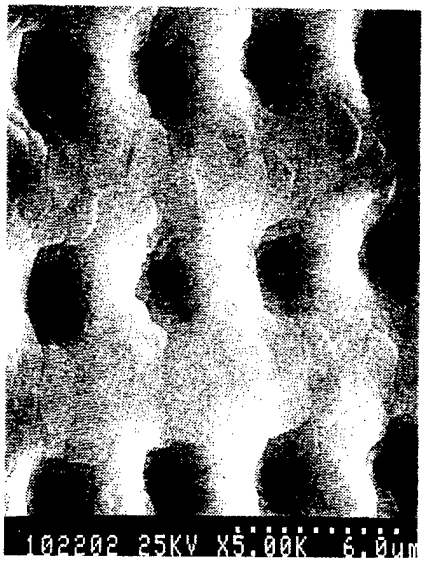
(b) Under Variable Source Coil Current

Fig. 5 RF power dependence on Cathode Power under - 300 v self bias

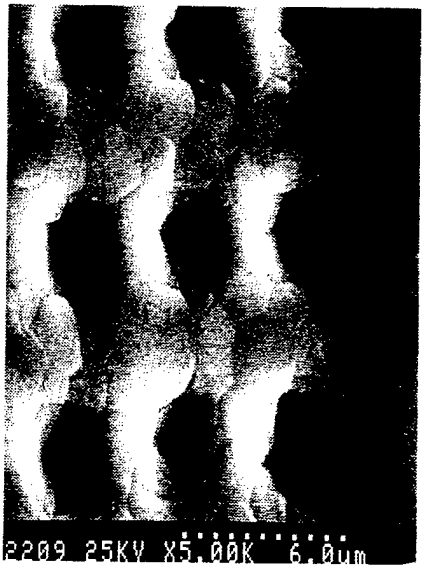
Top View of 3 μm Hole



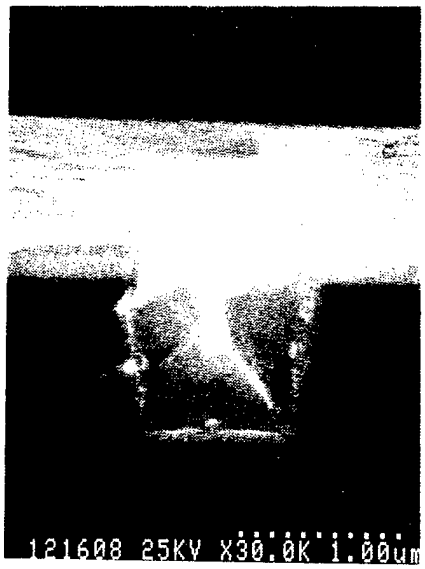
(a) no bias-Al



(b) bias-Al with Ti



(c) bias-Al w/o Ti



Side View of 1 μm Hole

Fig. 6 SEM of Sequential bias sputter,
(a) no bias sputter Al at 200 deg.C
(b) bias sputter Al with Tiundercoating
(c) bias sputter Al without Ti undercoating

DRY ETCHING TECHNOLGY FOR HALF-MICRON PATTERNING

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1. Introduction

The half-micron patterning places many demands on etching process. In order to realized half-micron patterns for VLSI devices, it is necessary to form patterns having anisotropic profiles, without damage and contamination. To achieve this, dry etching technologies using magnetron discharge and ECR plasma are proposed.[1-4] These technologies are expected to be useful not only for delineating fine patterns but also for reducing plasma induced damage or contamination problems to the devices.

In this paper, the author will report the results of the etching characteristics of AlSiCu with magnetron discharge and poly-Si with ECR plasma. The relationships between the etching characteristics and plasma parameters are investigated.

2. Magnetic enhanced RIE

The anisotroipic and highly selective etching to photoresist could be realized by using BBr_3/Cl_2 magnetron discharge.

Here, the author will report the etching characteristics of AlSiCu film with the BBr_3/Cl_2 magnetron discharge in comparison with conventional Cl containing gas process. Particularly, we made clear the mechanism of the highly selective etching with gas plasma containing Br.

2.1. Highly selective etching

Figure 2 shows the dependence of selectivity of AlSiCu to photoresist on the magnetic field. The concentration of Cl_2 was 70 % in each mixture.

In the case of BBr_3/Cl_2[5] and $SiCl_4/Cl_2$ gas process, the etch rate

of AlSiCu and photo-resist increase with increasing magnetic field. The density of plasma is higher, because the magnetic field and the reactive efficiency is enhanced. As the result, selectivity increases with increasing magnetic field, as shown in Fig.2. The reason is cosidered that the etch rate of AlSiCu is enhanced and the physical sputtering effect to photoresist by ions in plasma is weaker with increasing magnetic field.

2.2. Dependence of etching characteristics on gas composition

Figure 3 shows SEM photographs of AlSiCu patterns etched by both BBr_3 and $SiCl_4$ gas at the same concentration (30%). AlSiCu film is etched anisotropically in the both case. However, in spite of being etched over 100%, the remaining thickness by BBr_3/Cl_2 gas process is much greater than that by $SiCl_4/Cl_2$ gas process. The etched profile of photo-resist by BBr_3/Cl_2 is also much better than that by $SiCl_4/Cl_2$.

2.3. XPS analysis of the etched photoresist surface

In order to clarify why the etching of AlSiCu with BBr_3/Cl_2 gas process provides so high selectivity to photoresist, we analyzed the surface of an etched photo-resist on AlSiCu film by XPS.

We prepared several samples for XPS analysis, which were made by varying BBr_3 gas concentration for a constant flow rate of Cl_2 gas.

Figure 5 shows variations of photoelectron intensity of the C-Br and Al_2O_3 obtained from photo-resist surface by BBr_3/Cl_2 plasma. There should be a signal peak of Al(2p) near about 73 eV as binding energy.

We observed about photoelectron signals of Br-Br, B-Br and C-Br bond, and their signal peaks can be separated, whereas their binding energy were very close. So, it is clear that the produced component on photo-resist surface is C-Br. It is sure that C-Br compound is produced during the etching on photo-resist. This C-Br compound prevents the etching of photo-resist film. The selectivity of AlSiCu to photo-resist is obtained about 6 at 10% BBr_3 concentration, and 100 Gauss. Accordingly, the highly selective etching to photo-resist can be realized.

3. Cold and low-energy ion etching (COLLIE)

Dry etching for fabrication of VLSI devices will be required to realize stronger anisotropy, lower radiation damage and higher selectivity.

In order to achieve these characteristics, an etching technique using Electron Cyclotron Resonance (ECR) has been studied.

However, it is difficult to satisfy both anisotropy and low ion energy which is needed for lower damage and higher selectivity, because the angular distribution of ions is greater than that of RIE.[7,8] Therefore, to get an anisotropic etched profile, we had to raise the ion energy by applying external electric bias. We found the angular distribution of ion was caused by the ratio of ion sheath potential to ion temperature.[8] Accordingly, good etching characteristics can be expected by reducing the ion temperature even under low ion energy, as shown in Fig.5.

On the basis of the above study, we developed a new cold and low-energy ion etching system (COLLIE) with a hybrid magnetic field. In this system, plasma parameters such as ion temperature and ion sheath potential were controlled by a hybrid magnetic field, and uniformity of etched profile was maintained by magnetic mirror field , as shown in Fig.6. This concept will be necessary for large diameter plasma systems, too. In this paper, we report the performance of our COLLIE system and the etching characteristic results under low ion temperature.

3.1. Multicusp field

Figure 7 shows the dependence of the anisotropic factor on the number of magnetic poles when surface magnetic flux of each magnet was 0.12T. Vs/Ti has its maximum value in a 6 or 8 pole multicusp field. Vs has a constant value irrespective of the number of magnetic poles. However, the rotational motion of plasma is reduced by the multicusp field, so the ion temperature is suppressed and has its minimum value in a 6 or 8 pole multicusp field. It is not effective to have more than 6 magnetic poles, because the magnetic flux generated by multipole magnets localizes near the chamber wall and does not enter the plasma significantly.

Figure 8 shows the ion energy distribution. By using a minimum-B field with an 8pole multicusp field for solenoid coil which has an MHD stable region of 8cm, Ti is lowered from 2.3eV without multicusp to 1.8eV with multicusp field. In Fig. 8, the conventional condition which gives high ion temperature (Ti=5.3eV) is also shown.

3.2. Micro-loading effect

We studied the micro-loading effect in poly-Si etching under these typical conditions. Figure 9 presents the dependence of the micro-loading effect on pattern size when the thickness of photoresist is 1.6μm. In

this figure, the normalized etch rate is defined as the ratio of the etch rate for the specific pattern size to the etch rate for the 20μm pattern. The micro-loading effect is smaller when the ion temperature is low as shown in Fig. 9. In this experiment, the temperature of the susceptor was maintained at -30°C to avoid lateral etching caused by radicals and which was confirmed by SEM photographs. Therefore, the micro-loading effect must be caused by ions only. It is known that the micro-loading effect is affected by incident angular distribution of reactive species to a wafer. It is also known that there is a strong relationship between angular distribution and anisotropic factor Vs/Ti.[8] Namely, small angular distribution and a large anisotropic factor are achieved by reducing ion temperature.

3.3 Etched profile and selectivity

Figure 10 shows the change of the etched profiles with ion temperature. There are the necks and the tails on the pattern sidewall when ion temperature is high. By reducing ion temperature, these distortions disappeare and an anisotropic profile is realized. As mean ion energy is low enough, the selectivity of poly-Si to SiO_2 is greater than 70. That is also effective to reduce the radiation damage.

3.4. Dependence of ion temperature on ion mass

We tried some inert gas addition to make clear the relationship between ion energy profiles and ion mass. We chose krypton and xenon as additional gases, because their mass are nearly equal to clorine molecules or larger than chlorine molecules. Figure 11 shows the dependence of ΔE on inert gas concentration. In Fig. 11, ΔE shows an almost constant value with Kr addition, He addition reduced ΔE and Xe addition introduced a rise of ΔE.

We presented formerly that the width of energy distribution greatly influenced the reentrant angle of the etched profile.[9] Figure 12 shows a dependence of the reentrant angle on inert gas concentration. The reentrant angle is smaller than in the case of pure Cl_2 when the mean ion mass is lighter than chlorine ions.

We considered that hydrogen halide gas is suitable for controlling an instabilities, because mean ion mass is low enough by the existance of protons produced through an electron impact dissociation. Figure 13 shows halogen ion energy profile in the hydrogen halide plasmas. The energy profile of Br^+(m/e=79)ions in HBr plasma shows the narrowest

profile.

We studied the micro-loading effect for the n^+poly-Si etching process using Cl_2, HCl, HBr and HI gas. Figure 14 shows the dependence of the normalized etch rate on the pattern size. The micro-loading effect is greatly improved by using hydrogen halide gas. Especially, using HBr and HI gas produces no micro-loading effect.

Figure 15 shows the change of etched profiles with hydrogen halide gases. The anisotropy is enhanced by increasing the mass of halogen ion. From the results shown in Fig. 13–15, we should consider the relaxation process for the instabirities. Because ions move according to the electric field generated by the instability, but the electric field is quickly neutralized by very light ion such as protons. As the energy of instability is distributed to ions according to their mobility, we must consider the mass ratio between the species of positive ions.

4. Summary

We obtained anisotropic and highly selective etching for AlSiCu film by using BBr_3/Cl_2 magnetron discharge. BBr_3 gas dose not work as main reactive etchants but rather to restrain the etch rate of photoresist. The cause of highly selective etching is that C-Br compound produced during etching protects photo-resist strongly. So, BBr_3/Cl_2 magnetron discharge for etching of AlSiCu is very effective for the fabrication of devices which have big topography.

The COLLIE system with a hybrid magnetic field shows not only a good performance for the micro-loading effect but also a strong anisotropic etching, high selectivity and low damage even with low ion energy.

We also found that it is effective for reducing the plasma instability to lighten the mean ion mass. Then, we were able to successfully lower the ion energy dispersion by lightening the mean ion mass.

Anisotropic factor Emin/ΔE was enhanced by using hydrogen halide gases. So we were able to produce a no micro-loading etching process. Therefore, the concept showed in this paper is effective for fabricating fine patterns less than 0.5μm used in 16MDRAMs or higher integration devices.

Acknowledgement

The author would like to thank Dr. H.Komiya and Dr. H.Abe for their encouragement and guidance throughout this study. The author also wished thank Messrs. M.Yoneda, N.Fujiwara, T.Ogawa and H.Sawai for helpful discussions.

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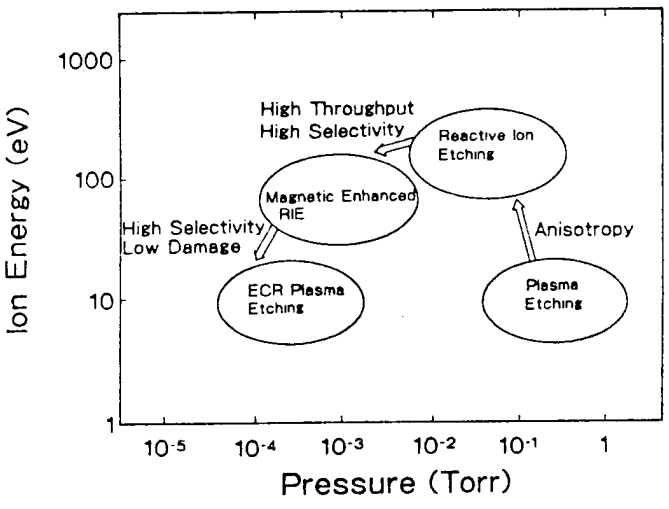


Fig.1 Trend of dry etching technology.

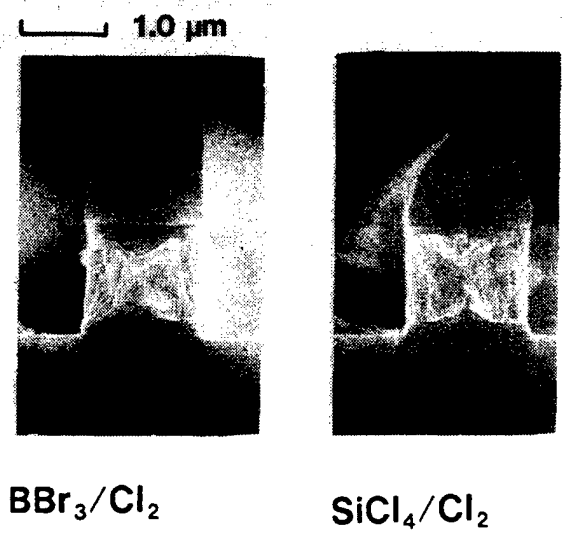


Fig.3 Comparision between etched profile by BBr_3/Cl_2 and by $SiCl_4/Cl_2$

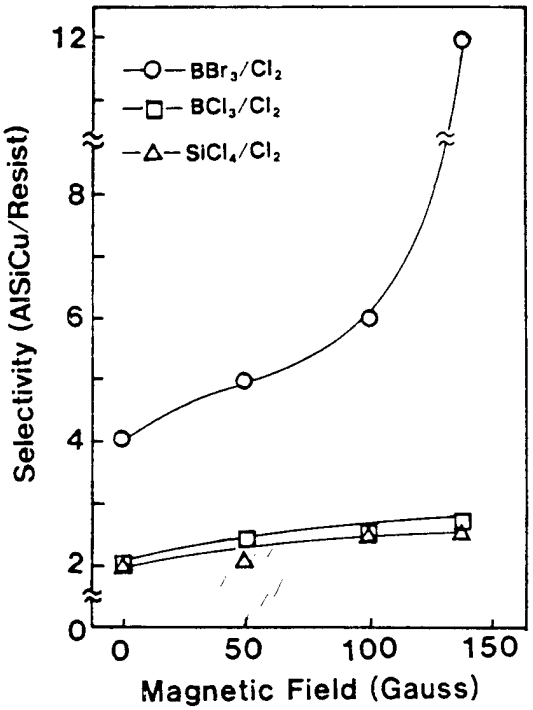


Fig.2 Variations of selectivity with BBr_3/Cl_2 and with $SiCl_4/Cl_2$ and with BCl_3/Cl_2 as a function of magnetic field

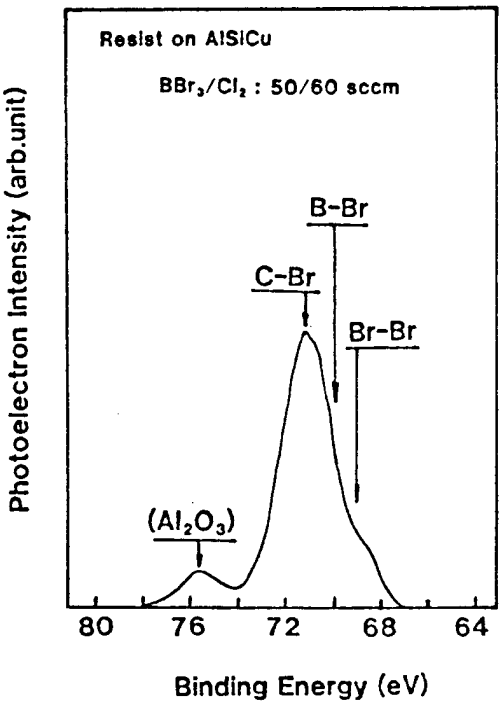


Fig.4 Al_2O_3 and Br(3d) signal in XPS spectra obtained from photo-resist surface etched on AlSiCu

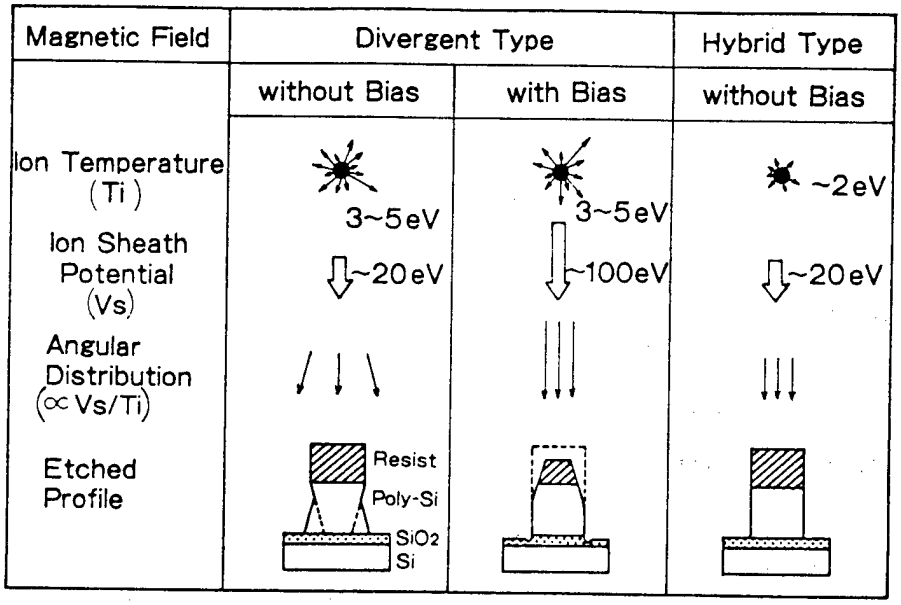
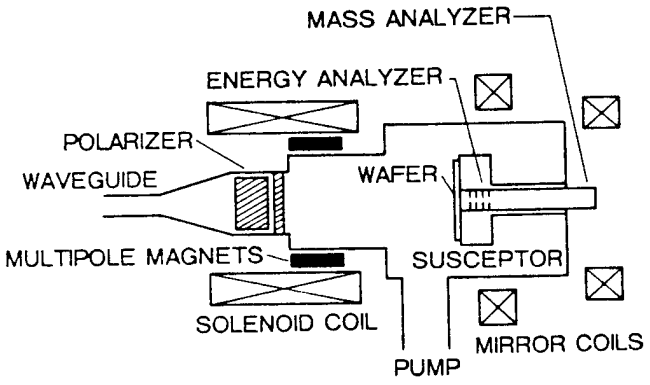


Fig.5 Relationship between ion temperature and etched profiles.



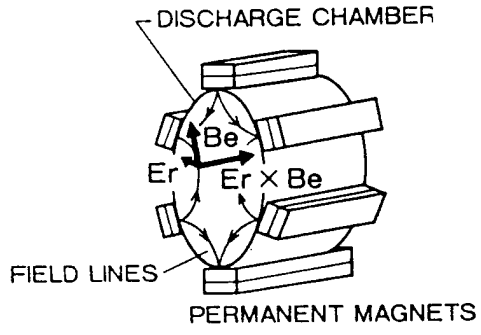


Fig.6 Schematics of the experimental apparatus. (a)Diagram of experimental apparatus. (b)Cross sectional view of discharge chamber.

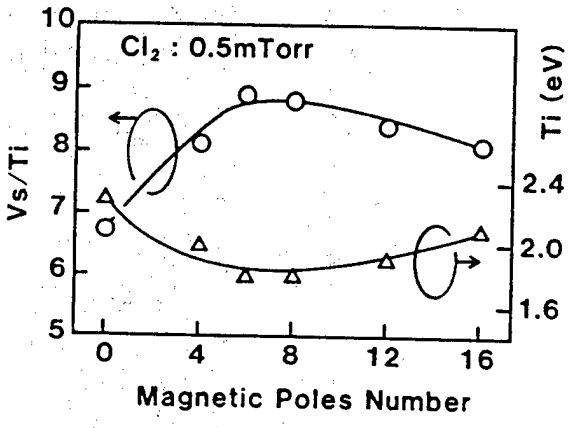


Fig.7 Effect of the number of magnetic poles on Ti and Vs/Ti.

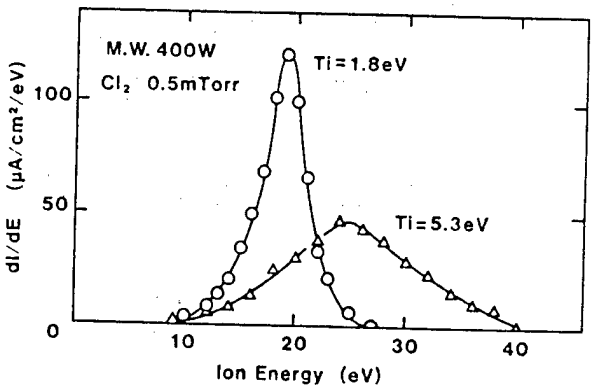


Fig.8 Ion energy distribution at different ion temperature.

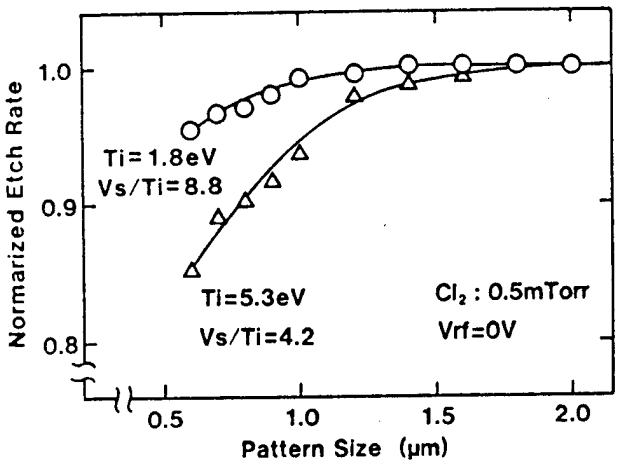


Fig.9 Microloading effect of two typical plasma conditions.

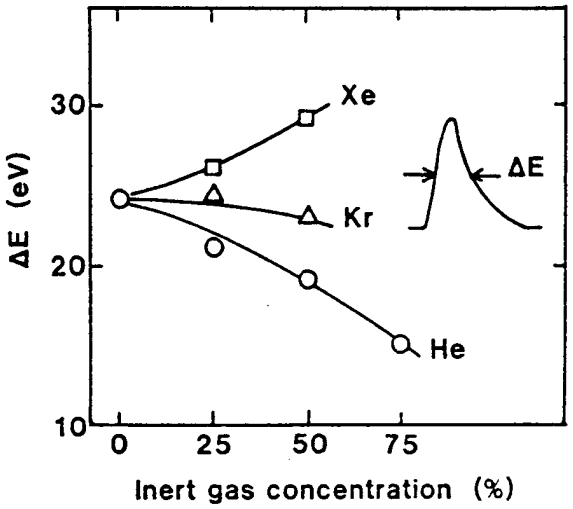


Fig.11 Dependence of ion energy dispersion on inert gas concentration.

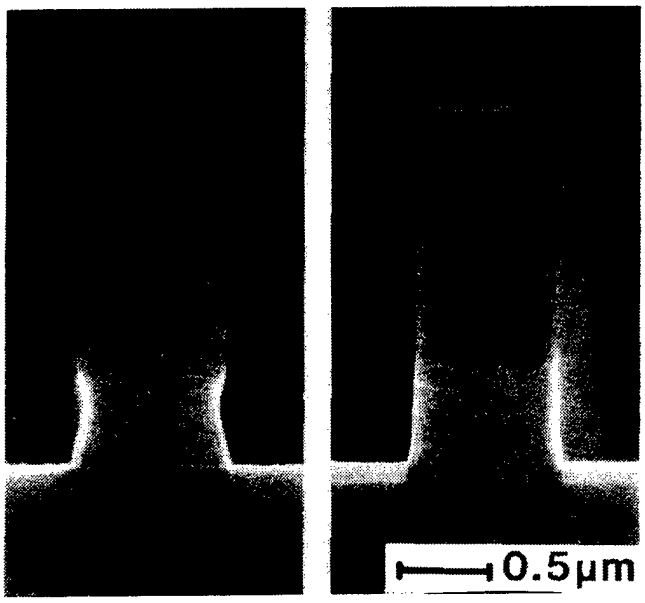


Fig.10 Comparison of etched profiles between two typical plasma conditions with Vrf = 0 V and Cl_2 : 0.5 mTorr.

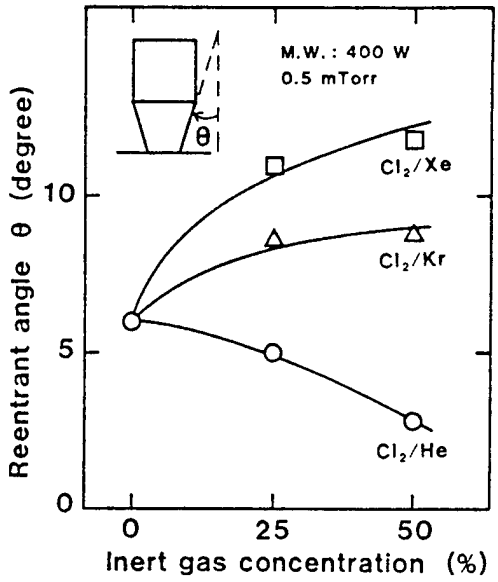


Fig.12 Dependence of the reentrant angle on inert gas concentration.

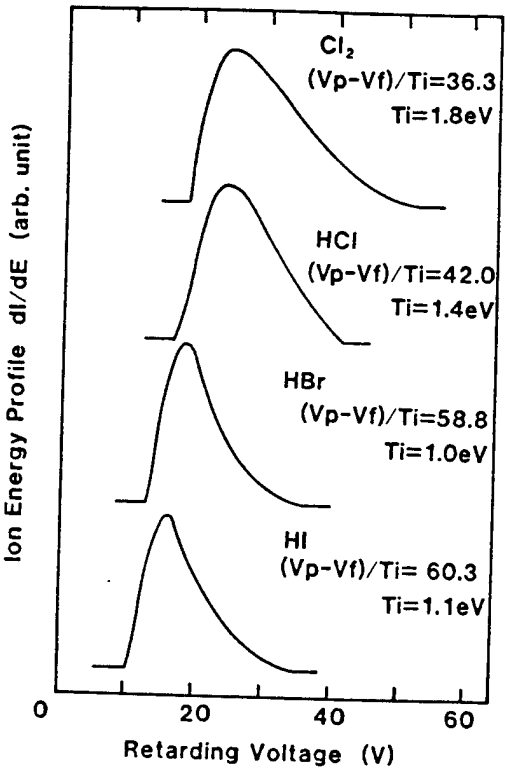


Fig.13 Ion energy profiles of halogen contained gas. Ion energy profiles show Cl^+ions for Cl_2, HCl and Br^+ions for HBr and I^+ions for HI.

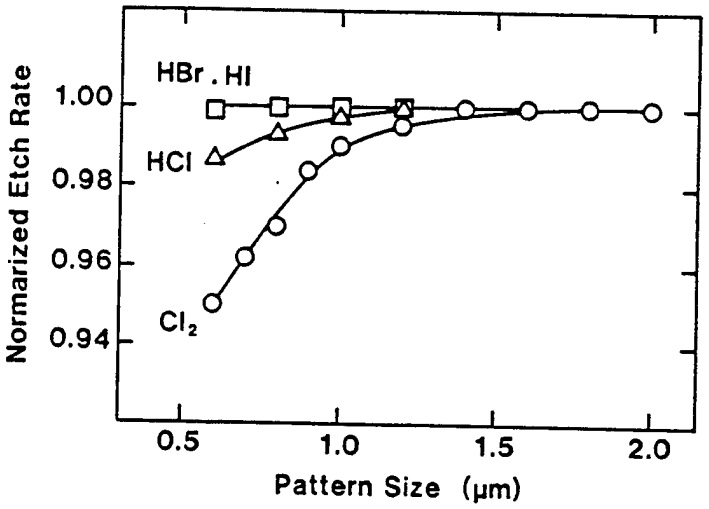


Fig.14 Micro-loading effect by using halogen contained gas.

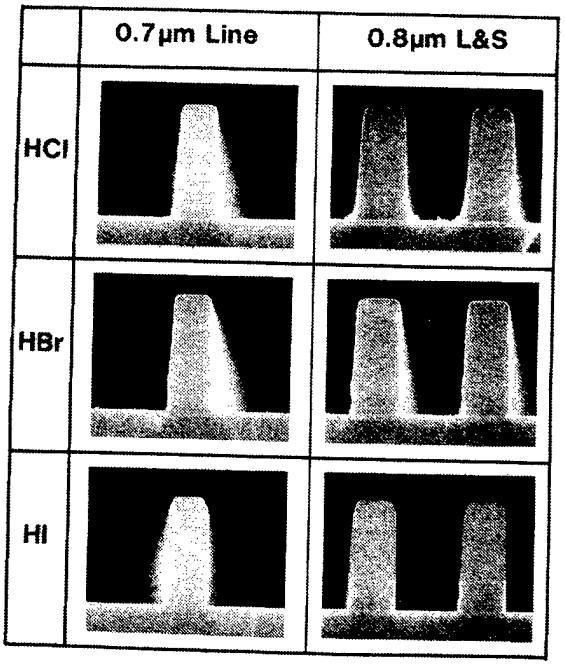


Fig.15 Comparison of etched profiles with hydrogen halide gas.

LOW PRESSURE ETCHING BY ECR PLASMA

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1. Introduction

As to the advance of semiconductor device integrations, the minimum feature size becomes smaller and smaller. In 16Mbit DRAM process, the minimum feature size is 0.5μm and the high performance etcher is strongly demanded such that it should control etching profile in sub-half-micron scheme.

As the plasma in lower pressure is easier to satisfy this demand, we have developed ECR plasma etching process. ECR etching characteristic at the pressure less than 10^{-4}Torr is discussed below.

2. Vertical profile at the periphery of large diameter wafer

ECR plasma is stably generated even in the pressure less than $1x10^{-3}$Torr (Fig.1). As anisotropic ion can reach wafer without scattering in this pressure region, low pressure ECR plasma will be effective for sub-half-micron pattern etching.

But ECR plasma under divergent magnetic field had a inherent problem. The problem was that slanting profile was observed at the periphery of wafer. It was thought that the slanting profile is caused by the slantwise magnetic line of force[1]. Fig.3 shows the magnetic field around wafer stage. Though the magnetic line of force is perpendicular to wafer in the center of the wafer, it slants at the periphery of wafer. It is thought that slanting profile is observed as ion reaches the wafer along the

magnetic of field. In order to verify that ion is restrained along the magnetic line of force, ion incident angle and direction of the magnetic line of force were measured. In these measurement, the magnetic field over wafer is controlled by subsidiary magnetic coil below wafer stage[2]. Fig.4 shows the subsidiary magnetic coil current dependence of incident angle and direction of magnetic line of force. It is obvious that ion incident angle agree well with the direction of the magnetic line of force. Therefore when the magnetic line of force is perpendicular to wafer over the whole wafer stage, vertical profile will be observed even at the periphery of wafer. Vertical profile is obviously obtained from Fig.5.

In ECR plasma etching process, slanting profile was sometimes observed in the periphery of wafer. This leaning profile remedied by controlling magnetic field around wafer stage with submagnetic coil.

3. Low pressure etching for controlling profile

In order to study ECR etching properties dependence on gas pressure, ECR plasma was applied to multi-layer resist etching. Etching gas was pure O_2 and RF bias was not applied. Fig.6 shows the sample structure. Middle layer is Al(400A) and bottom layer thickness is 1.4μm. Fig.7 shows the etching profile dependence on the gas pressure. Isotropic etching profile is observed at the gas pressure of 5mTorr. As decreasing gas pressure, anisotropic etching predominates over isotropic etching and undercutting decreases. This predominance of anisotropic etching is caused by suppression of ion scattering in lower gas pressure.[3] Decrease in undercutting will be caused by change of a relative ratio of radical to ion, because the undercutting is related to the chemical reaction with radicals. To investigate the relative ratio dependence on the gas pressure, the relative intensities of radical and ion are estimated by optical emission spectroscopy, supposing that intensity of atom correspond to the number of radicals. Fig.8 shows the gas pressure dependence of emission intensity of O_2 atom(615nm) and of O_2 ion(558nm). As the gas pressure dependence of emission intensity of O_2

ion(558nm) is similar to the gas pressure dependence of ion current density(Fig.1), the relative number of ion and radical can be estimated by the optical emission intensity of O_2 ion and O_2 atom respectively. Emission intensity of O_2 ion(558nm) and O_2 atom takes a maximum value in the pressure range from 0.5mTorr to 0.8mTorr. But as the gas pressure decreases below 0.5mTorr, emission intensity of O_2 atom(615nm) decreases more drastically than that of O_2 ion(558nm). Fig.9 and 10 show the gas pressure dependence of undercutting length and the relative ratio of radical to ion respectively. Both undercutting length and relative ratio of radical to ion decrease rapidly, when the gas pressure decreases below 1mTorr. From these result, the relative ratio of radicals to ion decreases as the gas pressure decreases.

Especially at the gas pressure lower than 0.2mTorr, ion dominant plasma is generated and such a low pressure plasma will be suitable for half-micron pattern etching process.

4. Half-micron pattern etching in low pressure

Etching in lower pressure is effective to control profile as mentioned above. In this section, performance of ECR plasma for sub-half-micron pattern etching is discussed in the issue of micro-loading effect[4].

Fig.11 shows the sample structure. In order to evaluate etch profile and micro-loading effect in the sub-half-micron range, line and space (L/S)resist patterns with the minimum width of 0.1μm are delineated in silylied photo resist top layer by means of E-beam direct writing and bottom photo resist layer is etched with O_2 ECR plasma. In this experiment RF bias was not applied. Fig.12 shows etching profile dependence on gas pressure. The etch rate of 0.2μm width pattern is different from that of isolated pattern and the undercutting occurs definitely in the pressure of $4x10^{-4}$Torr. The etch rate difference is not observed but small undercutting is still observed in the gas pressure of $8x10^{-5}$Torr. In the lowest pressure of $6x10^{-5}$Torr, undercutting is not observed. Fig.13 shows the relationship between the normalized etch rate and pattern size. In the curve of $4x10^{-4}$Torr pressure, etch rate drop starts from 0.4μm width pattern, and the etch

rate of 0.1μm pattern is reduced to be 60% of the original one. On the other hand, in the lowest pressure curve, there is no etch rate drop even at the 0.2μm width pattern. Moreover the etch rate of 0.1μm width pattern increases up to 90% of the original one.

Therefore, it is easily expected that etching rate depends on the aspect ratio as well as the pattern size. Fig.14 shows the relationship between the etch rate and the aspect ratio. It is clearly shown that the etch rate is kept up without any drop until at aspect ratio 3 in 6×10^{-5} Torr O_2 pressure.

Resist profile with 0.2μm L/S pattern without undercutting was obtained as shown in Fig.15. By applying ECR plasma to multi-layer resist etching, vertical profile is obtained especially in very narrow patterns by generating plasma in lower pressure without RF bias. But the pressure must be reduced in the range of 10^{-5}Torr.

It is assumed that such a good etching profile will be obtained higher pressure if ion energy is controlled by applied RF bias. This assumption will be revealed through further feasible studies and intensive investigations.

5. Conclusion

Low pressure etching with ECR plasma was investigated by etching multi-layer resist. By reducing gas pressure and thereby decreasing the relative quantity of radicals, the excellent etch profile is obtained down to 0.2μm pattern with less micro-loading effect. This suggests that ECR plasma has capability to meet 16Mbit DRAM process.

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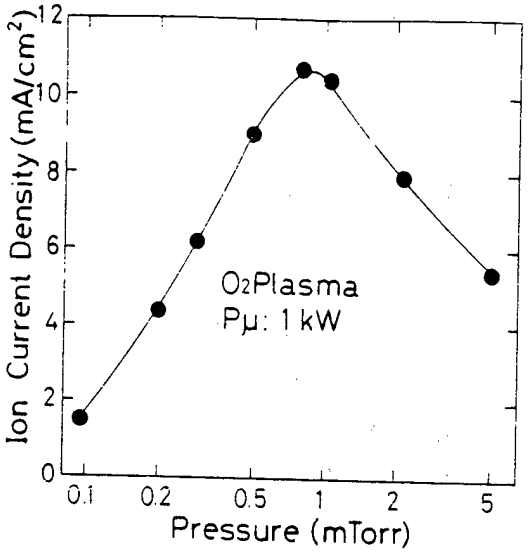


Fig. 1 Relationship between pressure and ion current density at O_2 plasma

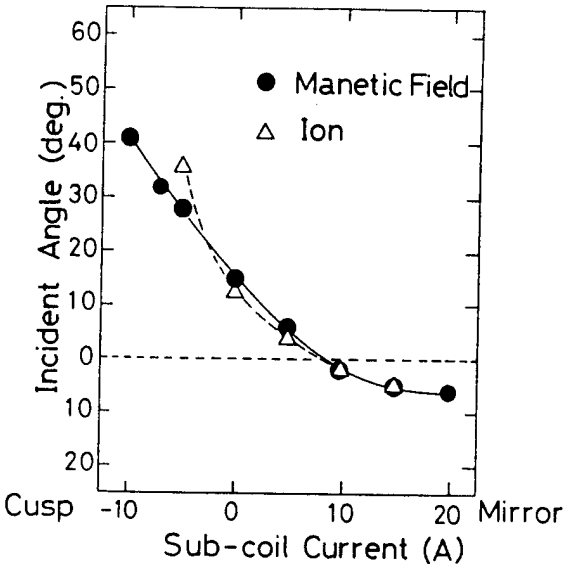


Fig. 4 Relationship between magnetic field and ion incident angle at various sub-coil current

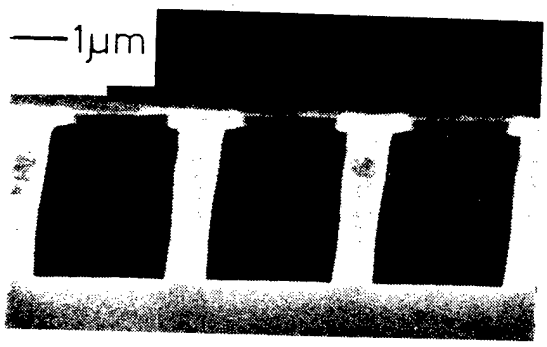


Fig. 2 Poly-Si pattern etched at wafer periphery

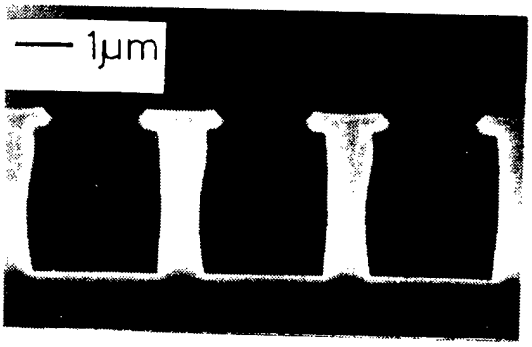


Fig. 5 Poly-Si pattern etched under perpendicular magnetic field

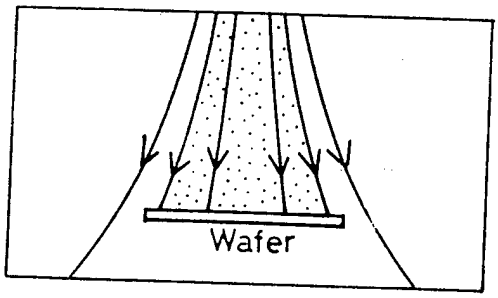


Fig. 3 Magnetic field around wafer stage

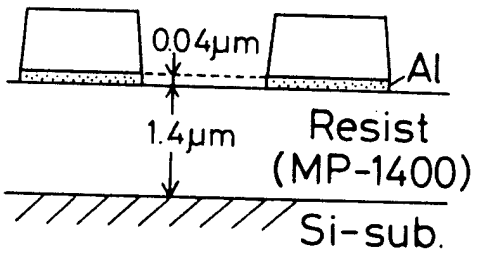


Fig. 6 Sample structure

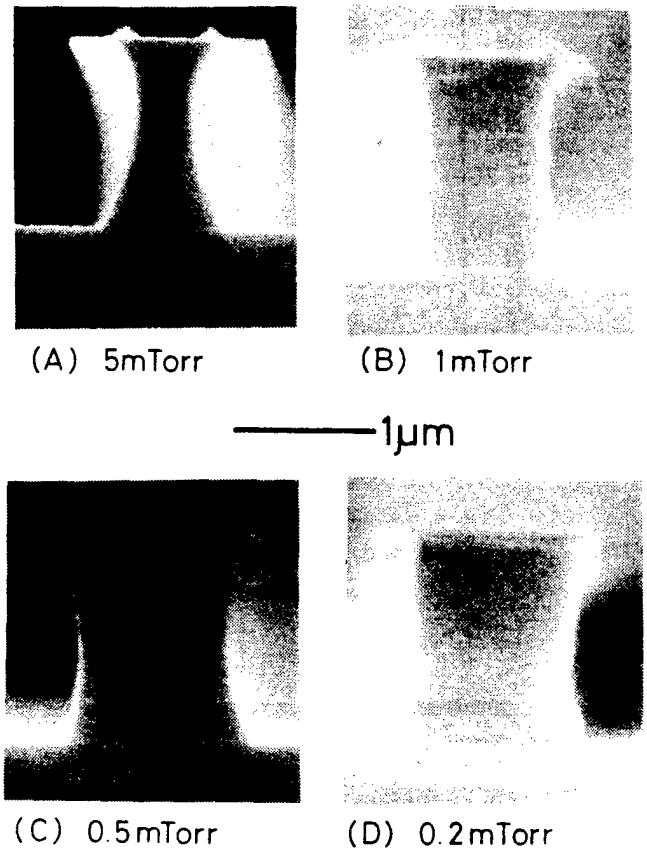


Fig. 7 Resist pattern etched at various O_2 gas pressure

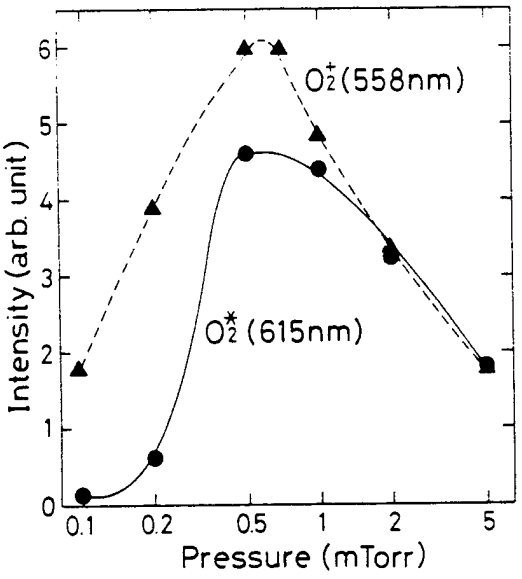


Fig. 8 Characteristics of intensity of O_2^*(558nm) and O_2^+(615nm) at various gas pressure

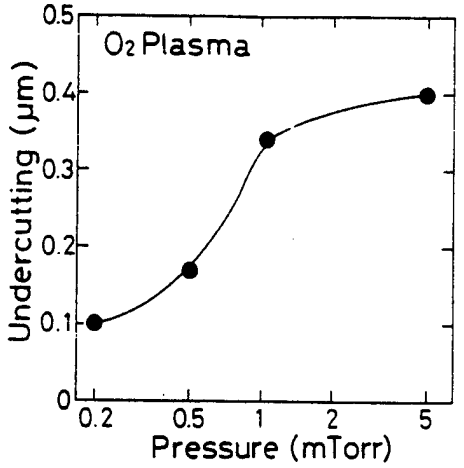


Fig. 9 Relationship between undercutting and gas pressure

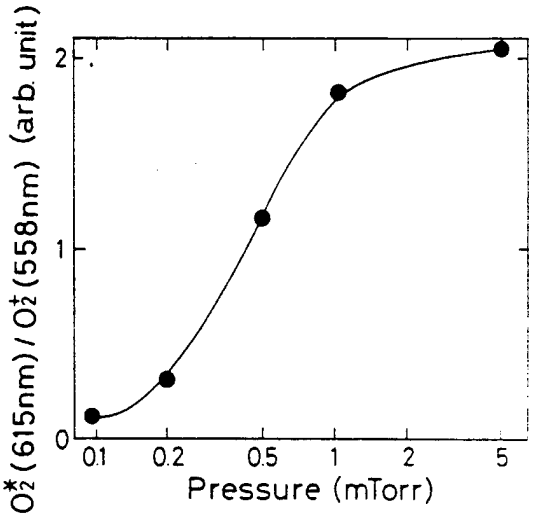


Fig. 10 Ratio of O_2^*(558nm) to O_2^+(615nm) at various gas pressure

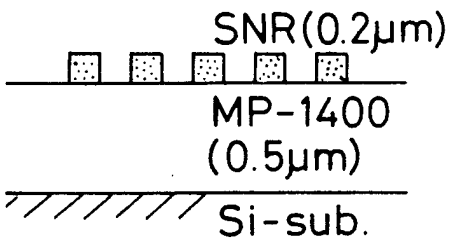


Fig. 11 Sample structure

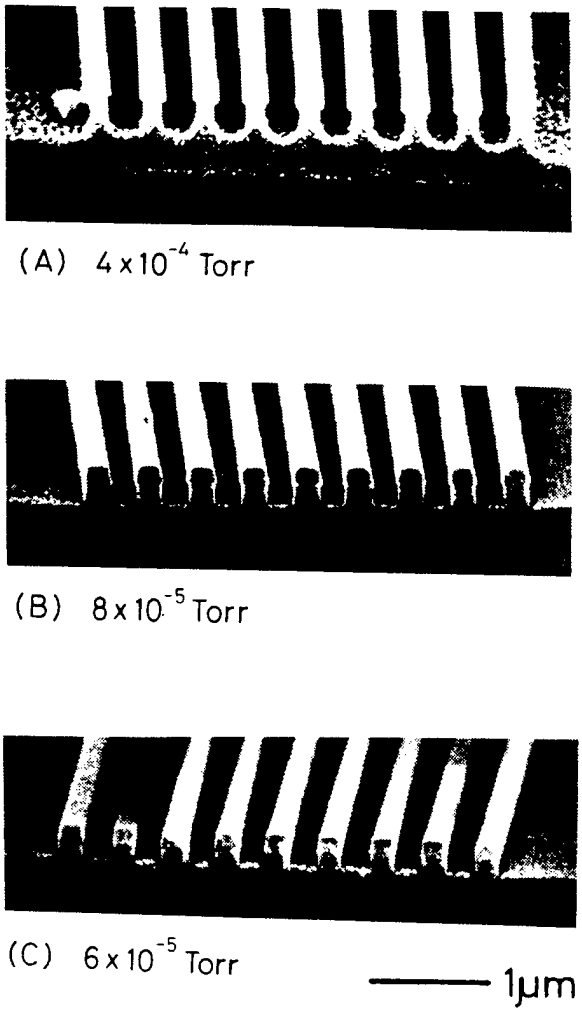


Fig. 12 Resist pattern etched at various O_2 gas pressure

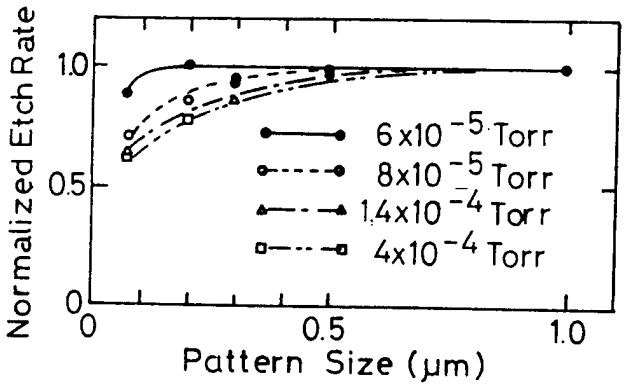


Fig. 13 Relationship between pattern size and etch rate at various gas pressure

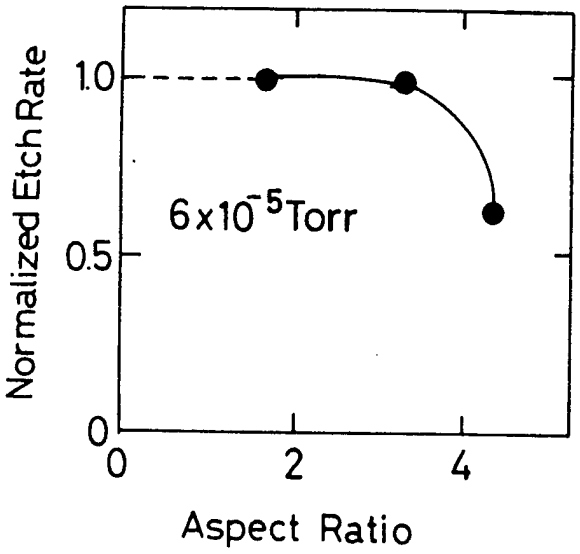


Fig. 14 Relationship between aspect ratio and etch rate at gas pressure $6x10^{-5}$ Torr

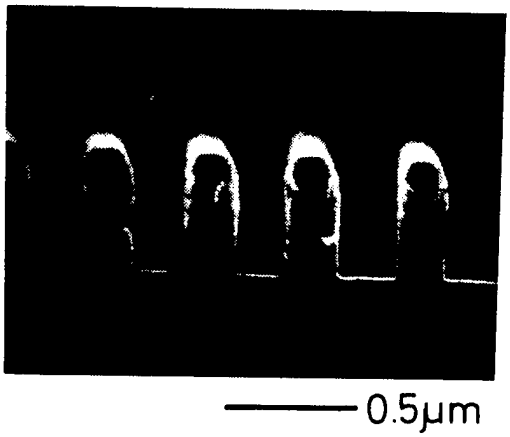


Fig. 15 0.2μm L/S resist pattern etched at O_2 gas pressure $6x10^{-5}$ Torr

"IC PACKAGE FOR MINIATURIZATION OF ELECTRONIC MACHINES"

Kazuo AKIBA
FA & Precision Products Group
SONY Corporation

1. INTRODUCTION

Small and light products like Camcorder, CD player, Personal Computer & telephone have been of great success, for they met the requirements of the present era of diversified 'Personal-use'. One of the common and important technology to realise theseproducts, I should mention, must be High Density Mount Technology(SMT).

As shown on Fig.1, High Density Mount Technology has become one of the key-technology of electronics not only to realise smaller & lighter SET, but also to make possible high-quality, high-reliability and high productivity. Consequently, it is necessary to devise the parts like IC or PCW used on high density mounting which can satisfy various needs rather than merely become smaller & lighter.
So, it will be expressed the trends and problems awaiting to be solved of IC package, especially important parts.

2. The Trends towards Smaller Size of SET

Now, it will explain about the miniaturization trends in SET and the progress in mount density.

Fig.2 shows the trends of size & weight in Portable VTR including Camcorder. It has achieved to realise 1/10 smaller & lighter products with achieving better function & performance at the same time. While the reduction on parts number by the use of IC and the development of high density mounting technology have greatly contributed to PCB mounting.

Fig.3 shows the trends in mount density of

mother PCW of Camcorder. It has achieved twice as much density in about three years, and it has put to practical use of the high density mounting of ~10components/㎠ in the present analogue circuit.

Fig.4 shows the relation between the PCB area of high density mounting and the projected area of mounted parts. It is easily seen that the ratio occupied by semiconductors such as IC, Tr and Di is large even in analogue circuit. It can be expected that the development towards digital circuit will be rapid, so the occupied area by semiconductors will become more important subject than it is now .

3. Mount Technology in Camcorder TR55

Here is presenting the mount technology used on CCD-TR55, merchandised in June '89 by SONY for the concrete example of recent applied-SET of high density mounting.

Fig.5 shows technical points of mounting and parts structure. It has achieved the mount density of ~10 components/㎠ on mother PWB and ~20 components/㎠ on HIC in this set.

Fig.6 shows the form and check points of mounting of 0.5mm-pitch QFP, which was used in this SET and greatly contributed to miniaturization. The precise form-measurement for IC Package including Lead is the important point to realise high quality mounting.

Fig.7 shows the structure and technology points of 150μ-rule & thin(0.6t) 4-layers PWB. Adopting new preflux is the important factor for high quality by restudying all the materials for miniaturization.

Fig.8 shows the technology point of cream solder-material to realize high quality micro-connection. Those factors, stability of properties of solder-material, conditions of printing and reflow process, are important.

Fig.9 shows an example of mount machines for chip-parts used in parts mounting. Basically, it is necessary to equip the functions of parts-check and getting precise mount dimensions & position by adopting image processing technology.

Fig.10 explains the points of process control in order to perform high density mount production with high quality and high productivity. It is required to achieve coordinate-integration of total technology, consists of "Designing", "Process" & "Production System", observing fundamental principles.

4. Trends in High Density Mount Technology

Fig.11 shows trends in mount density and development in fundamental technology as well. It can be anticipated that 15~20components/㎠ density mother PWB will be demanded, and further improvement for PWB with 100μ-pattern, 1005-size CR, 0.3~0.4㎜ P, QFP-IC &etc. will be indispensable.
Fig.12 shows the relation between mount system and mount density. It can be said that high density both-sides chip mount system will become general, and bare chip mounting of semiclnductor will be used in many ways.

Fig.13 shows the various kinds of reflow soldering system. It is natural every soldering system shall be made best use of according to its use and purpose, though, on the whole, it is under the development towards micro-connection point; and there are possibilities of improvement to apply other connecting technologies like welding process, bonding process, anisotropy electric conduction film process &etc.

5. Trends in IC Package

Fig.14 shows the application ratio of semiconductor IC on PWB mounting and HIC mounting. It can be estimated that the ratio of small SMT package and bare mounting will increase, so it must be important to retain capacities and

qualities.

Fig.15 shows the forms and characteristics in mounting of IC packages, those factors such as miniaturization of package, increasing ratio of plastic package, development of multi-pins' are the present situations and future directions.

Fig.16 shows the comparison of each IC package of form and mounted area. It is required to have the mount system as close to flip chip as possible. It must also be the important problem the miniaturization of bump unit for flip-chip type.

Fig.17 shows the structural comparison of each bare-chip mount system which have been in practical use. Many ideas are efficiently used to overcome the problem of the coefficient difference in thermal expansion.

6. The Problem of IC Package in Future

1) Miniaturization of fine-pattern and connection
Fig.18 shows the relation between IC mount form and mount density, and Fig.19 shows the relation between mount form and PWB pattern. It will be required the connection with 50~100μ pattern in small package system of SMT, and with 5~10μ pattern in wafer-scale integration system.

2) Development towards Multi-pins IC and High-radiation
The qualities and density of IC chips have been highly developed, so, consequently, it has been towards multi-pins ICs. While it is also required high-rediation mount system to meet the need of package miniaturization.
Fig.20 shows an example of high-radiation mount system used in the mounting of main frame of flexible computer. It is likely that the similar system at lower-price than this is expected.

3) The property of high-frequency
It is indispensable to develop the mount sys-

tem and PWB wiring technology capable of making as much as 100%-effeciency performance of high speed/flequency capacities of IC chip by the time 1~10GHz high-speed/flequency signal operation will be used generally for both analogue and digital elctronics equipments. Fig.21 shows an example of mount system on high-speed digital circuit. The points must be forming signal line on polyimid with low-dielectric constant.

4) Utilisation of TAB Technology
Fig.22 shows TAB technology, which can be expected to expand the application area, for it has much advantages for thinner and multi-pins technology. It can be said how to realise the automatic production for various kinds/amounts is one of the important problems.

5) Mount IC Inspection
As shown on Fig.23, it will become difficult to make visual inspection. Consequently, it will be necessary to develop new inspection-system like function-inspection giving some stress or some other system.

6) Reconsider the Standards & System of Reliability Evaluation
It is not likely that it is easy to unite the stadards and system of reliability evaluation into single absolute one when taking diversifications of mount system and its use.

7. Conclusion

I have expressed about technology-trends and problems for future of high density mount technology and IC package as above, and I believe that the key for the future successful growth must lie in the efforts striving for "total optimization of products functions" not in proceeding individual theme of "optimization of single IC" and "optimization of SET". However, I suspect, it may be more difficult theme to solve than the development of edge-technology.

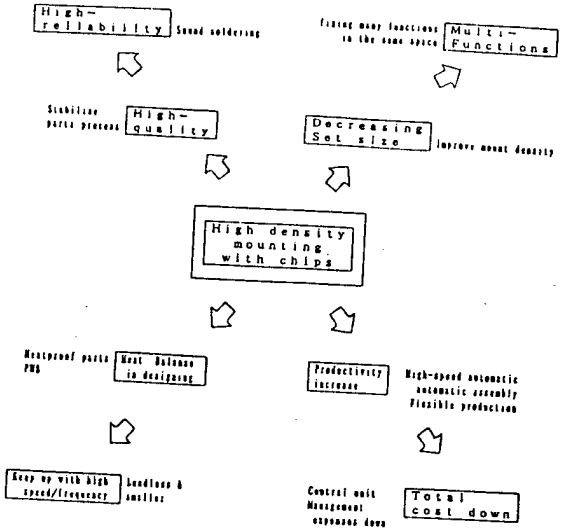


Fig 1

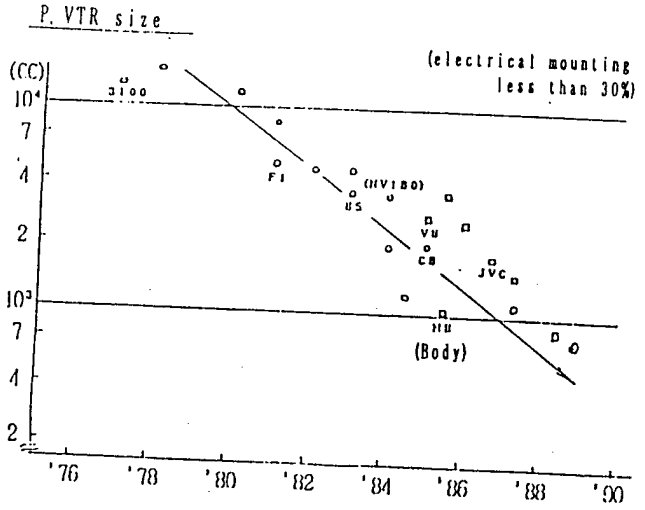


Fig 2

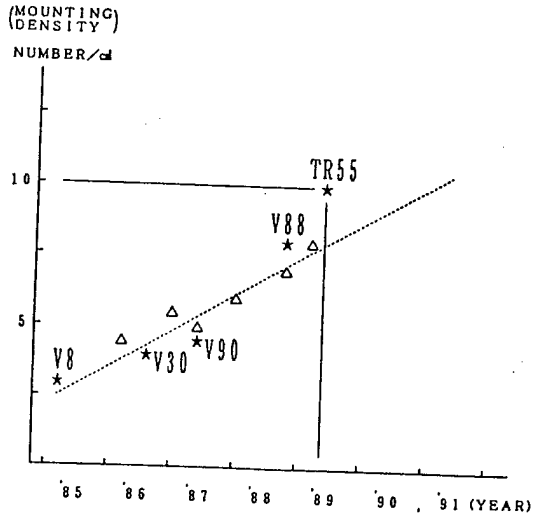


Fig 3

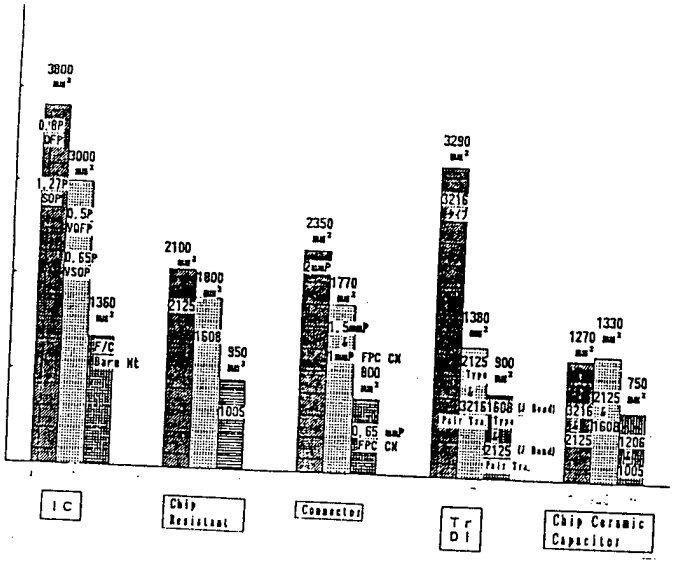


Fig 4

①Achieving accurate & stable supply form of IC Lead

②Achieving accurate & high grade PWB

③Stable & proper-quantity Solder Paste

④Carrying precise IC

⑤Achieving stable & uniform Reflow Temperature Profile

⑥Thorough control of Mount Process

1608 Chip C	490comp
1608 Chip R	130comp
Mixed Chip R	10comp
3125, 3216 Chip CR	130comp
MMTr (Inc. pair-TR)	103comp
SMMTr	92comp
VQKP IC	11comp
VSOP IC	1comp
other ICs	39comp
others	
TOTAL	abt1200comp

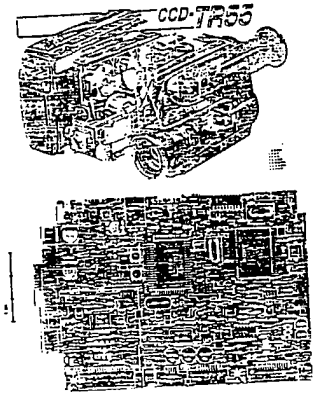


Fig 5

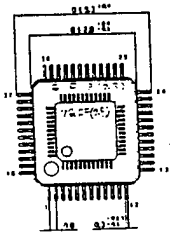
☆IC Lead Surface Process ... Coating Solder

☆Size of IC Lead ... Width0.18mm, Thick0.127mm, Foot Length0.5mm

☆Stable Supply ... Adopting Embossed Tape & Hard Tray

↓

(Achieving Accurate-carrying & High Quality Soldering)



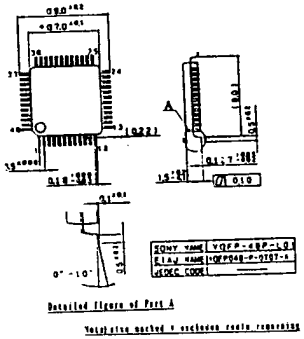


Fig 6

☆Adopting Fine board(t=0.6mm) 4-layers flow-pattern PWB

・150μm Pattern Rule, Through Hole(Land caliber Φ0.5mm, Hole cal. Φ0.35mm)

☆Connection with newly-developed Heat-resistant Preflux (OFF-connected PWB with a Snapitch)

・Etching Accuracy / Pattern Dimensions&Position Accuracy
/Oxidation Preventive Process of Cu Foil
— Accurate Appriciation of Heat-resistant Preflux

↓

①High Thermal Stability

②Improvement in Replacing with Postflux & Good Soldering Properties

③High Anti-Oxidation Effect

↓

(Achieving Good Soldering Properties even in the 3rd Reflow at 253℃)

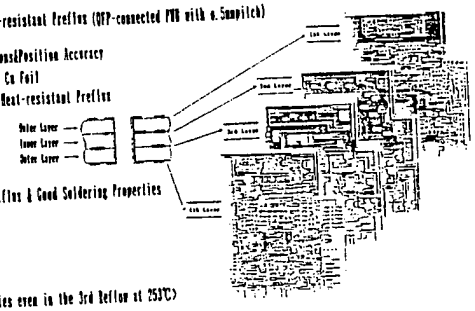


Fig 7

☆Cream solder... Globular(Spherical) Soldering Paste, Characteristics Assurance & Quality Retention of Solder Paste

☆Metal Mask ... Achieving Highly Precise Finish on Opening, Quality Assurance of Screen

☆Screen Printer ... Auto-Fixing of Screen Frame(min. printing shear) Perpendicular Print Structure(min. losing shape)

Auto-Solder Supply(min. print dispersion)

↓

(Successful Finish-Quality of High Density Mount PWB Demands Best Printer&Reflow-Furnace)

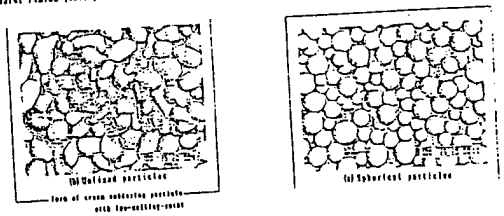


Fig 8

High Precision IC Mount

-Viblation-resistant Structure & Mount Machine with High Precision Image Processing-

☆Adopting Viblation-resistant Structure

・High-stiffness XY-direct-crossing Robot, Obtaining High Precision of Y-axis

☆Adopting High Precision Image Processing

・Adopting Parts Recognition Camera System (With 2-Magnifying Optical System & Capable to Select Total/4-division recognition)

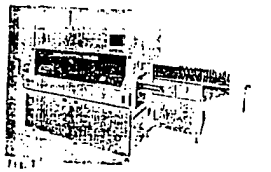
☆Establishing System Technology of High Precision Parts Mount

・Mount Dimention & Position Accuracy, Parts Cassette Accuracy....)

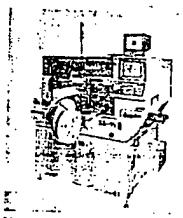
↓

《High Speed Electrical Parts Mount M/C with Visual Recognition SS-Ⅱ》

《Flexible Electrical Parts Mount M/C with Visual Recognition SS-Y$_2$》



High-Speed Electrical Parts Mount M/C (SS-Ⅱ)



Flexible Electrical Parts Mount M/C (SS-Y$_2$)

Fig 9

☆Thorough Control on Mount Process

・Prior Improvement ・Control Standard Keep

☆Adopting High Quality Fine Board 4-layers PWB

・Heat Resistant Preflox ・Precise Measurement

☆Establishing High Quality Soldering Technology

・Fine-Pattern Solder Print Tech. ・Highly Reliable Reflow Tech.

☆Establishing High Precision Parts Mount System Technology

・Mount Dimensions&Position Accuracy ・Parts Cassette Accuracy

・Mount Machine with Image Processing

↓

《Achieving High Quality Mount with 0.5mm pitch QFP》

《Realising Rapid Start-up & High Quality Mount Line》

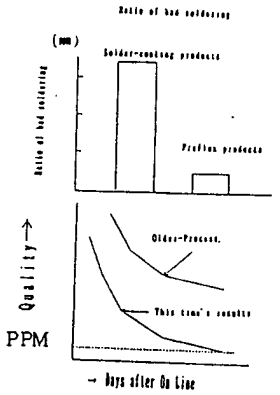


Fig 10

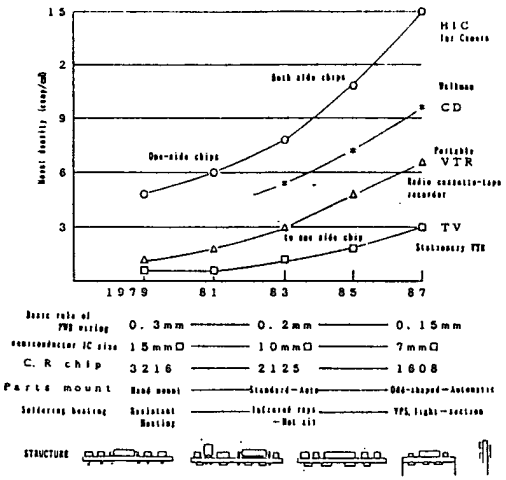


Fig 11

	Structure	PWB	Parts	Connection	Mount density (comp./)	wiring density	Use
Lead insertion		One-side	Lead Chip	Dip	1～4	High	Audio TV
One-side Mixed mount		One-side	Lead Chip	LV/Dip	3～7	Mid.	AC TV
Both-side Mixed-mount		Both-side	Lead Chip	LV/Dip/Reflow	5～9	Mid.	EVS VTR FDD CD-Deck
One-side Chip		One-side	Chip	Reflow	3～5	High	Compact-CD EIC Component
Both-side Chip		Both-side	Chip	Reflow	7～12	Low	Compact-CD Walkman VTR-Camera
Bare Chip		Both-side	Chip Bare IC	Reflow Bare Bonding	8～14	Low	HIC
Both-side Mixed mount		Both-side	Lead Chip	Reflow	5～10	Mid.	United Camera

Fig 12

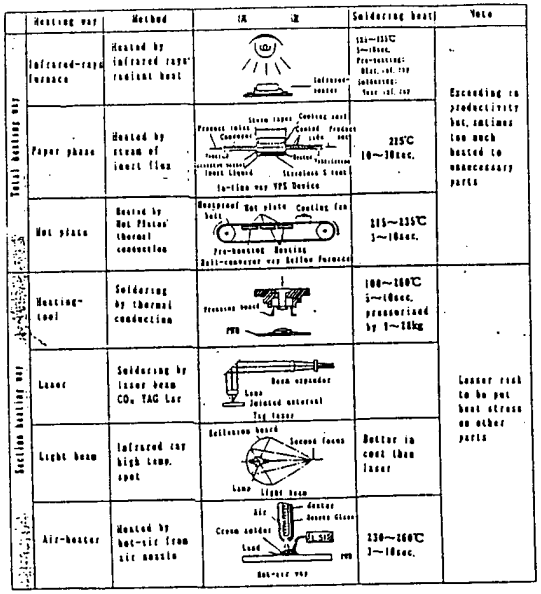


Fig 13

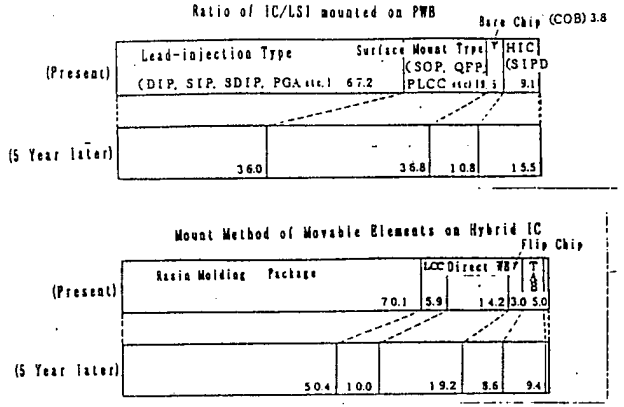


Fig 14

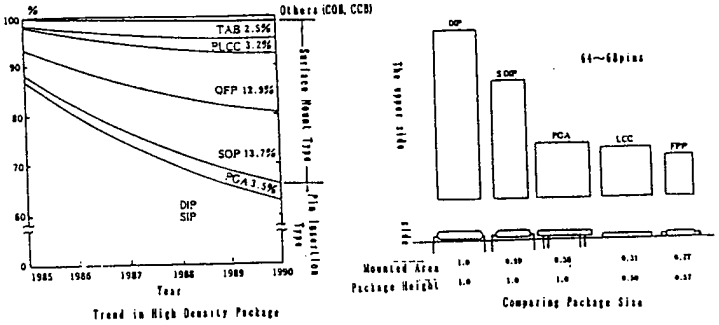


Fig 15

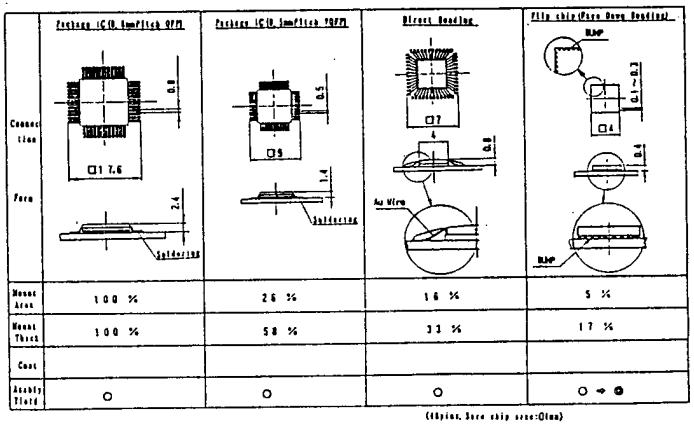


Fig 16

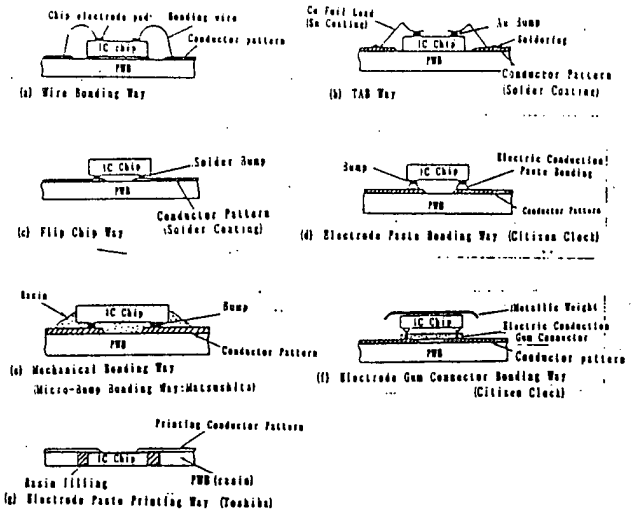


Fig 17

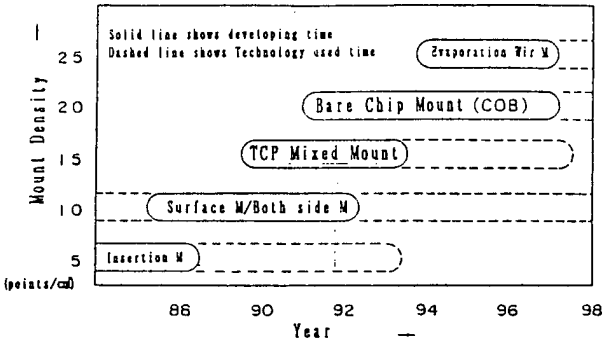


Fig 18

(1) Fine-Pattern Forming (50～100μm)

☆ Forming low-conduction-resistant metal material to PWB by coating/fine-foil method, make fine-pattern form by photo-process(etching).

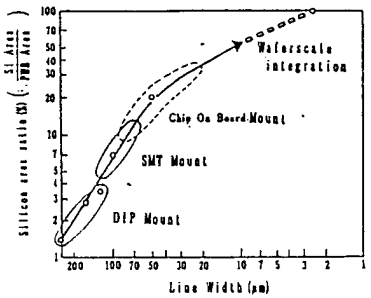


Fig 19

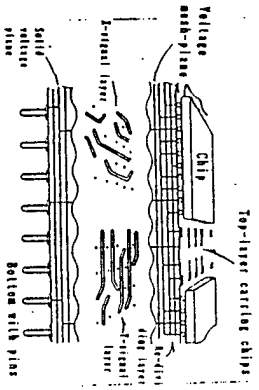
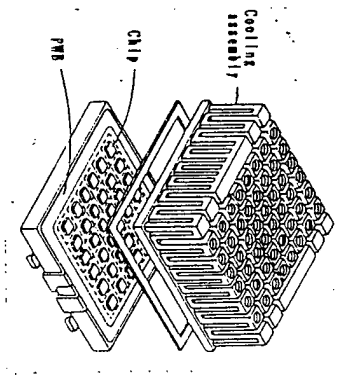


Fig 20



IC Multi-Chip Radiant Structure

(mount structure of High frequency circuit module)

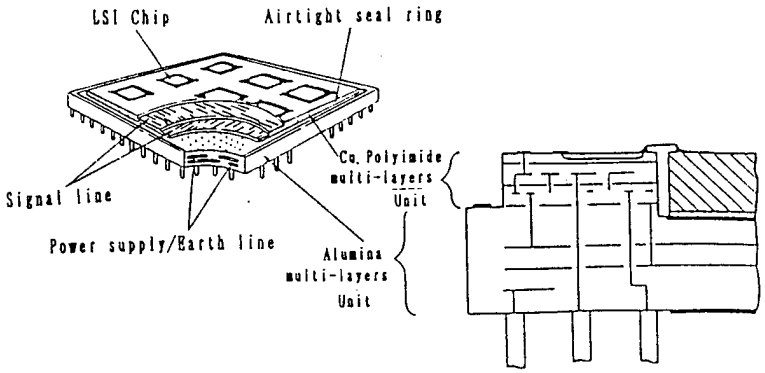


Fig 21

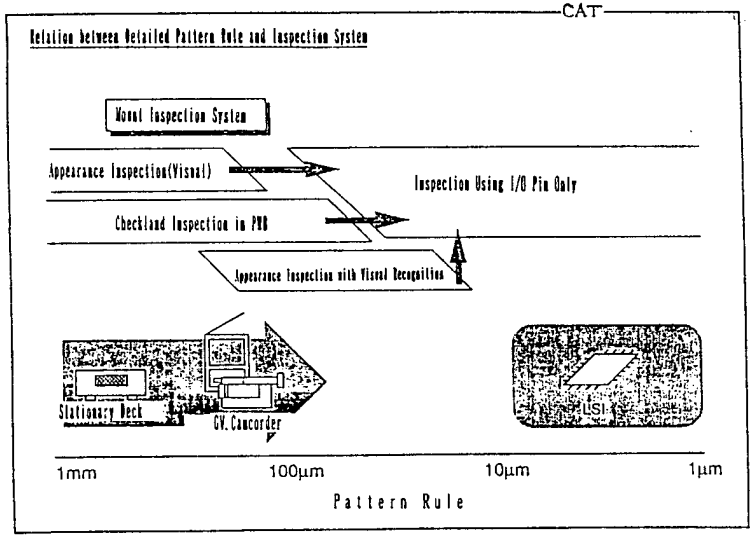
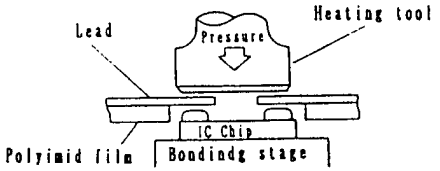
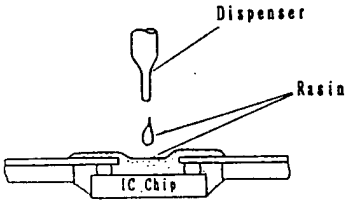


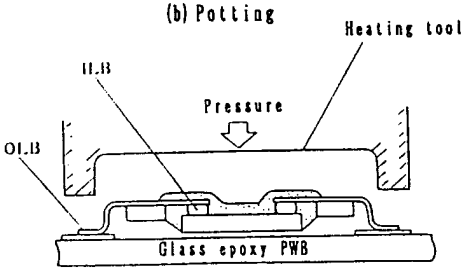
Fig 23



(a) Inner-Lead Bonding



(b) Potting



(c) Outer-Lead Bonding

Fig 22

MULTI-CHIP PACKAGING TECHNOLOGIES FOR COMPUTERS

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1. Introduction

The performance of a computer is largely influenced not just by the design of its logical structure but by the speed of its logical circuit. Realization of a high-speed logical circuit leads directly to speeding up of the machine cycle and is therefore the most important factor in upgrading the system performance. The logical circuit is divided into the active circuit using mainly LSIs and the interconnection wirings.
In the case of recently developed high-performance systems, about 1/2 of the machine cycle is shared by the active circuit and the delay in the connecting system, so that the overall speed increase of logical circuit calls for the use of high-speed LSIs and for the shortening and speeding up of connecting wires.
The delay in the interconnection system depends on the packaging technologies in a broad sense of the term which include the LSI terminal connections, packaging method, wiring board, cabling, connectors, and cooling method. Accordingly, the high-density, high-speed packaging technologies bear closely upon the improvement of system performance. In the following, the fundamental approach to the high-density multi-chip packaging technologies and their practical applications are introduced, with specific reference to supercomputers.

2. Fundamental Approach to High-performance Packaging

(1) Improvement of Packaging Performance
Quantitative evaluation of the packaging performance is quite difficult and requires some measure to grasp the degree of its improvement. In our sense, the improvement in packaging performance is measured on the basis of Kanai's power·time product theory[1] which is expressed by the following formula.

$$PF = \frac{\theta_B\{1-b\lambda_o \exp(\alpha\theta_B)}{\dfrac{U_B \cdot R\theta_B}{\text{Instruction}}}$$

where, P_B : Performance factor
θ_B : Temperature rise of functional block
U_B : Equivalent energy of functional block B
$U_B = T_B \cdot P_B$ (Delay time x Power consumption of functional block B)
$R\theta_B$: Equivalent thermal resistance
$R\theta_B = \theta_B/P_B$
$\lambda_o \exp(\alpha\theta_B)$: Failure rate of functional block B

The above formula indicates that the following improvements are required for packaging technologies in order to raise the system performance, PF.

1) Minimize $U_B.R\theta_B$/Instruction, i.e., minimize both the energy U_B and the package thermal resistance $R\theta_B$.

2) In order to minimize the energy U_B, raise the packaging density to minimize the interconnection delays and minimize the basic delay due to wiring.

(2) Indicator of Packaging Performance
The following formula is used as an indicator of the interconnection delay. [2]

$$T_M = \tau \cdot \sqrt{S/G}$$

$$\tau = \sqrt{\varepsilon\gamma}/C \text{ (Delay per unit length of wire)}$$

In the above formula, S indicated the substrate area, G the number of gates on the substrate, $\varepsilon\gamma$ the dielectric constant of insulative layers, and C the velocity of light. T_M is the indicator of the media delay in interconnection which should be made as small as possible. To reduce T_M, it is necessary to use a wiring material having a low dielectric constant and raise the packaging density G/S. Thus, the improvement of packaging performance requires the shortening of interconnection wire by high-density packaging, realization of low-energy circuit by the use of low dielectric constant materials, and reduction of thermal resistance of packaging. An example of supercomputer packaging based on this approach is introduced below.

3. Multi-chip Packaging for SX-3 Supercomputer

3.1 Packaging Hierarchy

Supercomputers are intended primarily to realize highly upgraded system performance, so that it is inevitable to use the high-performance LSI technologies as well as the multi-chip packaging for high-speed interconnection and high-density packaging. Figure 1 shows the packaging hierarchy for the NEC SX-3 Supercomputer[3] . The features of the packaging shown in Figure 1 include the TAB chips, the micro-chip carrier mounting the TAB chips called FTC(Flipped TAB Carrier), and the polyimide-ceramic substrate 22.5 cm square on which 100 FTCs are mounted.
The use of the FTC has made it possible to realize high-efficiency cooling of an LSI whose power consumption has reached 33 w owing to its high-integration, and also has opened up the possibility of high-density, high pin-count packaging of LSIs.
The polyimide-ceramic substrate accomodates up to 100 FTCs and high-density I/O interconnection of about 12,000 pins with reduced delay, thus contributing greatly to the reduction in overall packaging areas. A detailed discussion of this advanced packaging method is given below.

3.2 LSI Packaging (FTC)

The number of signal terminals required for gate array LSIs increases gradually with the rise in the degree of integration according to Rent's law[4]. Accordingly, the key point of LSI packaging exists in how to realize higher number of I/Os at high-density. While there are many ways for higher number of terminals on LSI, the face-down TAB packaging method has been selected because of the ease of LSI cooling discussed later.
Figure 2 is a sectional drawing of the FTC, and Figure 3 shows its external appearance.

As seen Figure 2 and 3, the FTC method is used for face-down mounting of TAB chips on the substrate, with the terminals arranged on the bottom surface of the substrate and the heat path coming up from the substrate surface. Since the terminals are arranged in a staggered grid pattern on the bottom surface of the substrate, it is possible to connect many I/O terminals with very small spacing.
Packaging densities can be compared on the basis of a silicon(chip) vs. substrate area ratio. Figure 4 is a comparison of the silicon vs. substrate area ratio between different LSI packages[3]. As is clear from Figure 4, the FTC method allows the packaging density to be increased continuously even in case of higher pin counts of LSI mounting, and fully exhibits this advantage when it is combined with the polyimide-ceramic substrate. As for the case of cooling, the silicon chip itself is die bonded directory to the FTC cap as shown in Figure 2, so that it is possible to obtain a very low thermal resistance by using copper-tungsten alloy or aluminum nitride as the cap material, because these materials have high heat conductivity and their thermal expansion coefficient is close to that of silicon.
As is clear from the above description, the FTC technology, developed and applied for the first time for the SX-2 Supercomputer[5], is the most advanced method of high-density, higher pin counts of LSI packaging promising reduced thermal resistance.

3.3 Substrate (Polyimide-Ceramic Substrate)

When the logical gate number on the substrate increase, it results in an increase in the number of interconnections between LSIs and external I/O terminals according to the aforementioned Rent's law. The substrate is thus required to have the capacity to accommodate a large number of wires and at the same time connect the wires with the least signal propagation delay T_M.
The polyimide-ceramic substrate developed for the SX-2 Supercomputer is most suitable for these two purposes.
As can be seen from its sectional drawing shown in Figure 5, alumina ceramic is used as its base substrate with power supply and ground wiring formed inside to lower the impedance of power distribution circuits. Input/output pins brazed to its bottom surface in a staggered grid pattern make it possible to connect many I/O terminals. The through hole wire connecting the top and bottom sides of the substrate provides the shortest wirings between the surface wiring layers and the I/O pins for external connections. Thin films of multilayer connections are formed on the substrate surface, with polyimide inserted as insulating layers. Since the polyimide wiring layers has a low dielectric constant of $\varepsilon\gamma = 3.5$, it can reduce the signal delay by about 40% as compared with the alumina ceramic substrates which have an $\varepsilon\gamma$ of 9.
Furthermore, polyimide insulating layer has a very smooth surface suitable for the formation of fine, multilayer wiring layers. Compared with the conventional printed circuit-board, the polyimide-ceramic substrate has a much lower thermal expansion coefficient, which makes it suitable for both alumina and silicon mounting and allows a very large number of pins to be connected.
Thus, the polyimide-ceramic substrate is best suited to high-density, high-speed logical circuit packaging.
The packaging performance T_M, discussed in section 2 , is compared between different substrate in Figure 6, which clearly indicates that the polyimide-ceramic substrate is most suitable for reducing the delay in connection.

3.4 Multi-chip Package

Figure 7 shows an external view of the multi-chip package for the SX-3 Supercomputer. Since 100 FTCs are mounted on the substrate 22.5 cm square and each LSI has a maximum gate number of 20,000, the package as a whole has a maximum of 2 million gates. This means that the packaging density is high enough to mount one complete unit of processor on the multi-chip package.
On the periphery of the substrate is fitted a frame called "flange," which is used in connecting as many as about 12,000 I/O pins to the board back side simultaneously with zero insertion force (ZIF).
A mechanism for very precise position alignment with the ZIF connector is provided on the flange and board, which realizes high reliability of pin connecting operation. Figure 8 shows an external view of the ZIF connector.

3.5 Cooling Module

The rise in packaging density results in increased power consumption on the multi-chip package, which amounts to a maximum of 3.8 kw or 7.9 w/cm^2 in the case of the SX-3 Supercomputer.
This means that the thermal resistance per LSI needs to be lowered to 0.7℃/W or less in order to maintain the LSI junction temperature at an average of less than 55℃. Since it is impossible to realize such low thermal resistance by air cooling, the only choice is liquid cooling. Liquid cooling is divided into the immersion cooling method in which the unit to be cooled down is immersed in an inert liquid and the water cooling method in which water is circulated to cool down the unit by heat conduction. When the heat density is high, the water cooling method is suitable because it has a larger thermal capacity , is lower in cost and easier for maintenance. The basic structure of water cooling is to circulate cooling water through a cooling jacket and bring the jacket in contact with the LSI without giving it any undue stress. Figure 9 is a sectional drawing of the water cooling system for the SX-3 Supercomputer.
The LSIs do not come in direct contact with the cooling mechanism because they are housed in the FTC. The FTC cap is made of a material with high heat conductivity and naturally has a larger area than the LSIs, so that it serves as an excellent heat spreader and provides a large area of thermal contact with the cooling mechanism. The heat conduction block, which is the water cooling jacket, has an internal jet impingement of water to the jacket inside facing the LSIs in order to raise the heat exchanging efficiency. A very small gap of about 80 microns is provided between the heat conduction block and the FTC, and a thermal compound is fitted in the gap to lower the thermal resistance. This structural arrangement has made it possible to lower the thermal resistance from the LSI junction to cooling water to less than 0.6℃/W. Figure 10 shows an external view of the cooling module.

5. Conclusions

In the foregoing, the multi-chip packaging technologies have been discussed, with specific emphasis on their application for supercomputer performance improvement. Considering the anticipated progress in science and technology in the future, it is highly probable that the demand for upgrading the performance of sophisticated systems like supercomputers will become more pressing and exacting. The packaging technologies focused on multi-chip packaging will carry a heavy weight just as LSI technologies as one of the most effective and practical means of meeting this ever growing demand for higher product performance.

It is our expectation that the packaging technologies focused on multi-chip packaging will be further improved and applied to a greater variety of products, as has been the case with the TAB technologies which have recently been applied extensively to mass sales products with the growing market inclination for smaller, lighter and easier-to-use products.

6. References

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[4] B.S.Landman and L.Rosso, "On a Pin Versus Block Relationship for Partitions of Logic Graphs", IEEE Trans. on Computers, vol. C-20, No.12, pp.1469-1479, Dec. 1971

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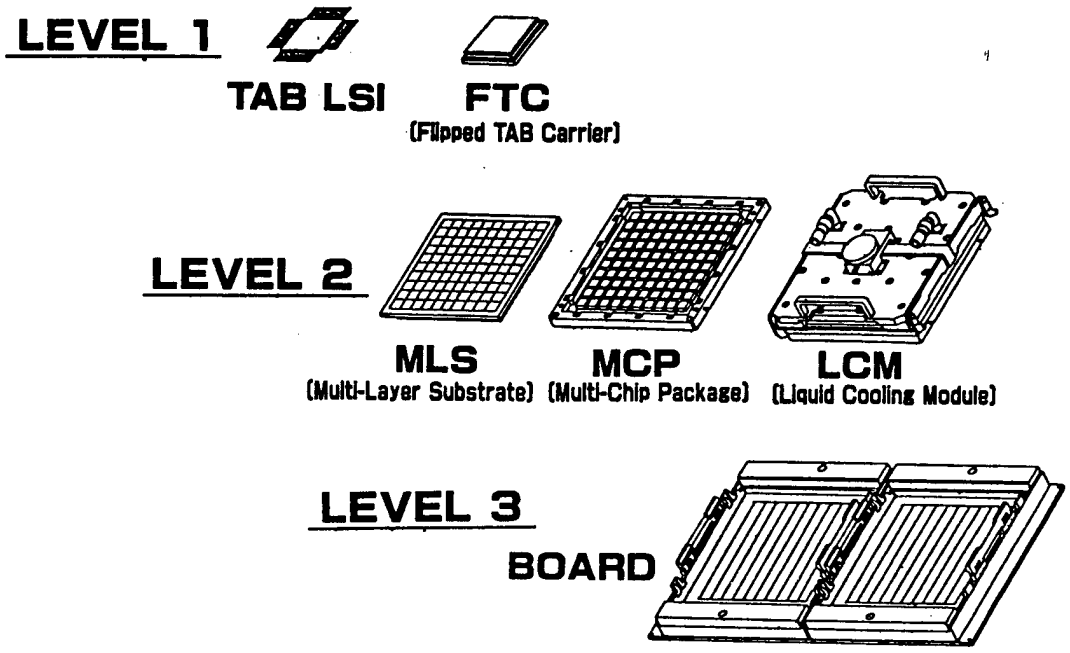

Fig.1 Packaging Hierarchy of Supercomputer SX-3

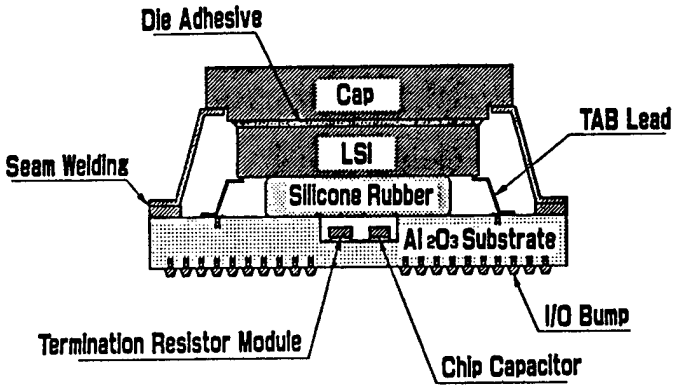

Fig.2 Cross Section of FTC

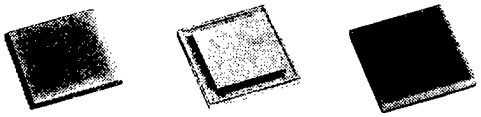

Fig.3 Outward Appearance of FTC

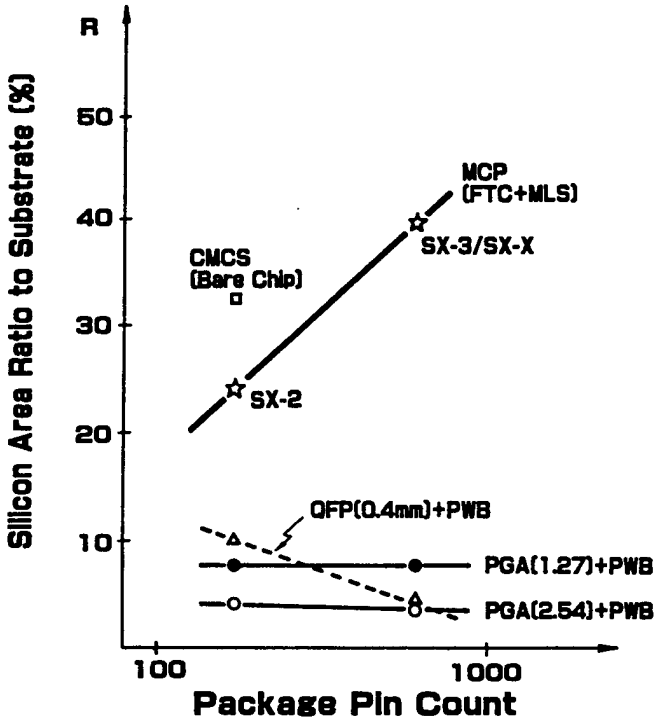

Fig.4 Comparisons of Silicon Area Ratio on Various Packages

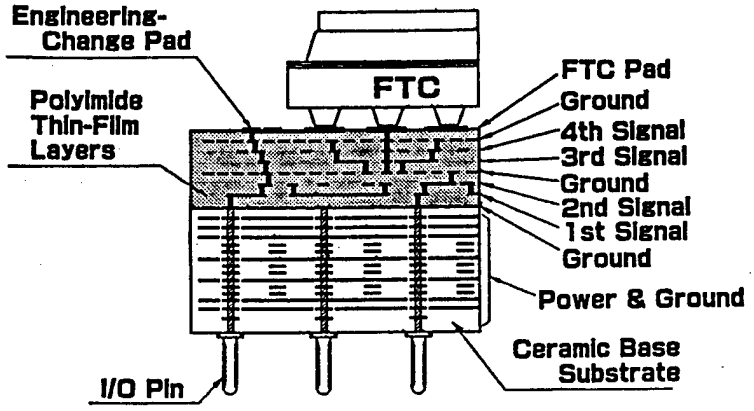

Fig.5 Cross Section of SX-3 Polyimide-Ceramic Substrate

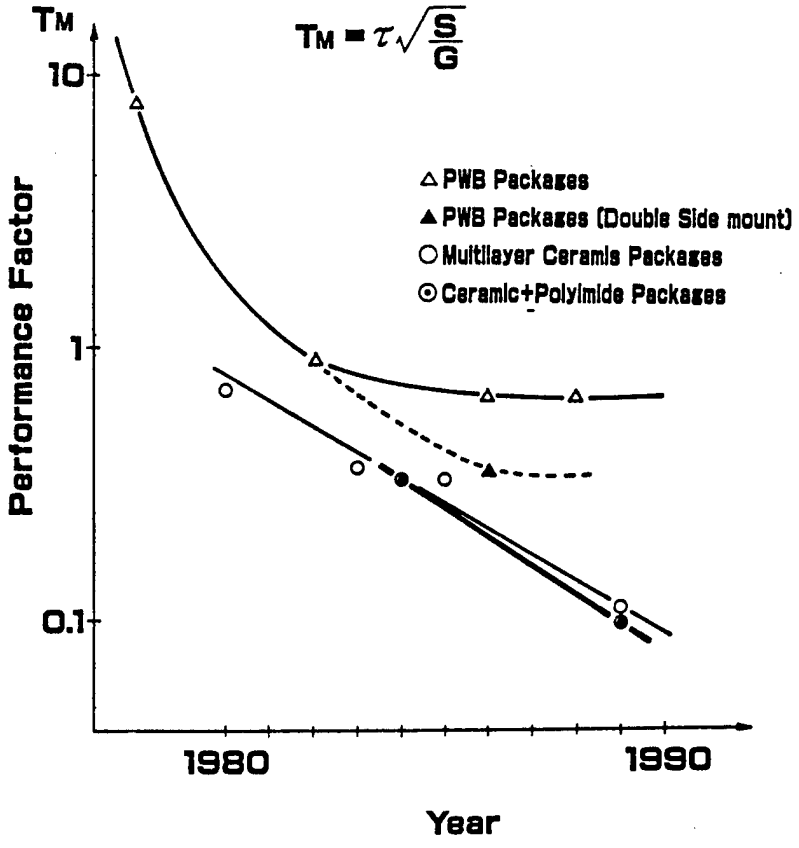

Fig.6 TM Coparisons on Various Substrate

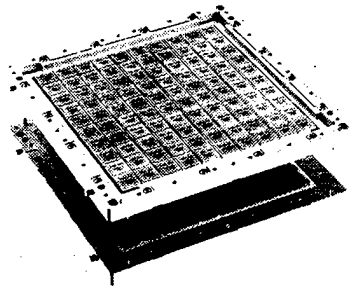

Fig.7 SX-3 Multi-Chip Package

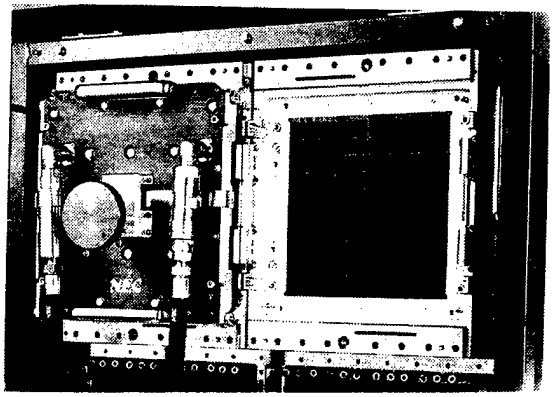

Fig.8 SX-3 ZIF Connector on Board

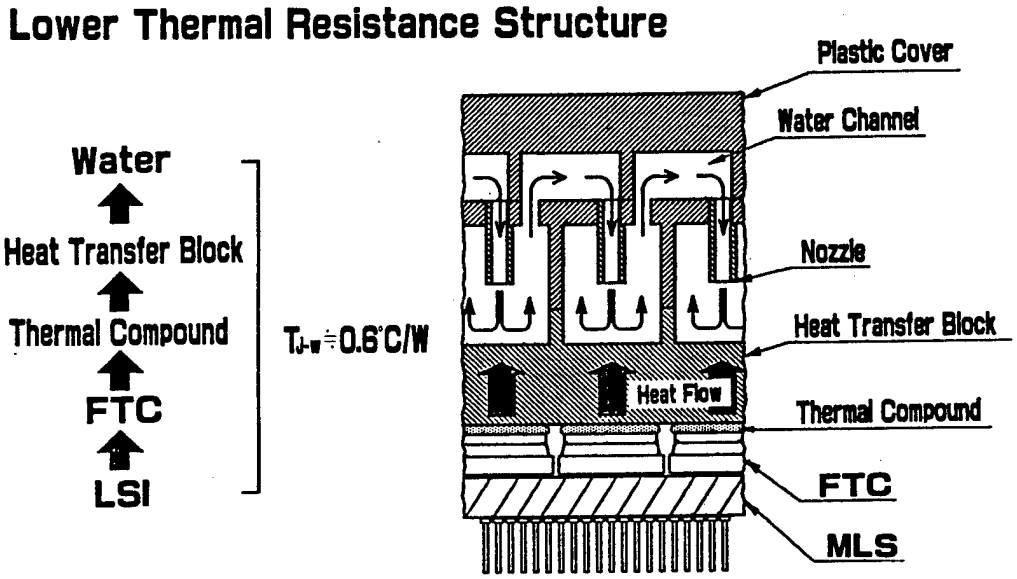

Fig.9 Cross Section of SX-3 Liquid Cooling Module

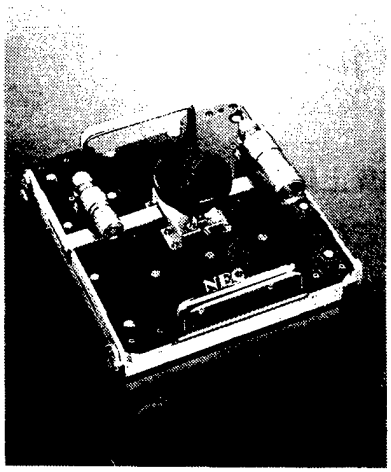

Fig.10 SX-3 Liquid Cooling Module

THE TECHNICAL TREND OF EPOXY MOLDING COMPOUNDS FOR THINNER PACKAGE OF SEMI-CONDUCTOR DEVICES

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1. Introduction

IC and LSI packages have rapidly become diversified to comply with the trend in electrical and electronic parts becoming very compact. Packages are changing to a thinner type and to a higher pin count type despite the fact that the size of the chip is getting larger and larger. The method of mounting is moving toward the surface type. Recently the TSOP package has begun to be put into practical use. It fills the gap between SOJ/QFP and TAB methods and it will become the main style of packaging in the field of memories from now on (Figures 1 and 2) [1], [2].

With such circumstances as background, the design of a molding compound has come to require a highly advanced level of technology. Figure 3 summarizes the trends in surface mounted devices and those technical problems which a molding compound has to solve. The following two points, among others, are the most critical problems:

1) Reduce those thermal stresses which are generated due to a difference in coefficient of thermal expansion between the silicone chip/lead frame and the molding compound.
2) Prevent package cracks and the delamination of the lead frame or the chip from the molding compound, which occur when a package is entirely exposed directly to a soldering temperature of 215°C to 260°C.

This paper deals with some techniques for developing an epoxy molding compound to cope with thinner type packages, and trends in the development for the future.

2. Reducing Stress

As a result of employing larger chips and thinner packages, a semiconductor package molded with a molding compound is liable to create problems, such as package cracks, chip cracks, and chip passivation layer cracks, which are attributed to the thermal stress generated by a difference in the coefficient of thermal expansion between the molding compound and the silicone chip/lead frame. This results in a more rapid deterioration in moisture resistance.

An internal stress can be generally expressed by using the following equation.

$$\text{Stress } \rho = K\int E \cdot \alpha \delta T$$

where, E: modulus of elasticity of molding compound
α: coefficient of thermal expansion of molding compound
T: temperature
K: constant

As gathered from the equation given above, it is necessary to decrease both the modulus of elasticity and the coefficient of thermal expansion of the molding compound to reduce stress.

2-1 Reducing the Modulus of Elasticity

A silicone polymer forms a two-phase structure (sea-island structure) in the epoxy matrix. Applying silicone, therefore, permits achievement of a lower modulus of elasticity without lowering the glass transition temperature (Figure 4). To disperse a silicone polymer in the epoxy matrix, two roughly classified methods are available. One is the physical dispersion method in which silicone rubber or silicone gel powder is added. The other is the chemical dispersion method in which a pre-reactive product between silicone and phenol novolac resin or epoxy resin is added (Figures 5 and 6). In the chemical dispersion method, it is possible to reduce the domain size of silicone polymer in the matrix to the submicron level, because the compatibility of silicone polymer to the matrix can be controlled. Stress characteristics are significantly dependent upon the domain size. As shown in Figures 7 and 8, it is possible to obtain a remarkably lower stress characteristic by using an optimum domain size.

The effect of reducing stress by using silicone polymer can also been shown in the impact characteristic (Figures 9, 10 and 11). Accordingly as the silicone polymer increases in loading, the impact energy gets larger. This correlates with the crack resistance in heat cycles.

2-2 Reducing Thermal Expansion

A decrease in coefficient of thermal expansion could be achieved by increasing to load of silica (Figure 12). A higher loading of silica, however, would bring out the disadvantage of a decrease in flowability and of an increase in modulus of the cured product. The load of silica, therefore, can not be increased without giving elaborate consideration to this problem. To prevent the melt viscosity from increasing, it is necessary to develop a loading material capable of very close packing. To achieve the closest packing, the material must have particles shaped nearly to a true sphere and these must have optimum particle size distribution (Figure 13).

Applying a new filler composition capable of being most closely packed would allow achievement of a high level of flowability and a lower coefficient of thermal expansion (Figure 14).

Using the new type filler is also effective in preventing packages cracks when soldering them as referred to later. From the determination of a stress intensity factor (K1c), it may be concluded that toughness is improved according to an increase in silica loading (Figure 15).

Spherical silica is a material which is very useful in reducing the melt viscosity of a molding compound. As compared with pulverized silica, however, spherical silica reduces the strength of a molding compound and deteriorates the soldering crack resistance after absorbing moisture (Figure 15). It is possible, however, to improve the strength by controlling the surface condition of spherical silica. Figure 16 shows that spherical silica with a very porous surface is useful to increase strength.

It is necessary to research shapes and distributions of silica, including its surface characteristics, because the shape of a package will become more complex, and the pin count will increase.

3. Preventing a Package Crack while Soldering

When a device is soldered, the moisture contained in the package will rapidly expand, resulting in a package crack. To overcome this cracking mechanism, a comprehensive series of countermeasures have been taken, including altering the design of the lead frame, coating the lead frame with polyimides, packing a package so that it does not absorb moisture, and so on. Countermeasures associated with the molding compound, however, may be summarized as follows (Figure 3):

1) Lower moisture absorption.
2) Lower the modulus of elasticity at high temperature.
3) Heighten toughness.
4) Improve the adhesive strength between the molding compound and the silicon chips/the lead frame.

3-1 Lowering Moisture Absorption

Generally, a resin with a low moisture absorption tends to have a low glass transition temperature. At a lower glass transition temperature, there are possibilities that a device may have its reliability reduced when exposed to a high temperature over a long time. It is necessary to keep the glass transition temperature at least 150°C. Figure 17 shows the relation between glass transition temperature and moisture absorption in molding compounds, with a variety of epoxy resins applied. Changing the chemical structure of a resin permits us to obtain material which has low moisture absorption while at the same time showing a high glass transition temperature. The molding compound with such resin applied shows a low water diffusion constant, as well (Figure 18).

Figure 19 shows the relation between water absorption and soldering package crack characteristics. A package molded with a conventional molding compound was found cracked when the package was immersed in solder at 240°C for 10 seconds after left for 12 hours in an atmosphere having a relative humidity of 85% at 85°C. Another package molded with a lower moisture-absorbing resin, however, was found greatly improved. In the case of a package we employed this time, it is considered possible to prevent cracking as long as water absorption is kept at 0.3% or less if the package is of 2.3 mm thickness, or 0.23% or less if 1.9 mm thickness.

However, the thinner the thickness of package is, and the larger the size of chip is, the more severe the moisture absorption limitation will be. It is all the more necessary to study further decreases in moisture absorption.

3-2 Reducing the Modulus of Elasticity at a High Temperature

Figure 20 shows the relation between the modulus of elasticity at a high temperature and package cracks. A package with a lower modulus of elasticity has a more favorable crack resistance. In relation to the modulus of elasticity at a high temperature, a package with a lower modulus of elasticity shows a lower glass transition temperature in general similarity with its moisture absorption. Changing the chemical structure of a resin, however, allows achievement of a higher glass transition temperature and a lower modulus of elasticity as well (Figure 21).

3-3 Increasing the Toughness

As has already been described, the molding compound with higher filler loading will make the molding compound tougher and will improve the package crack resistance in soldering. Figure 22 shows the relation between the stress intensity factor of a molding compound and package cracking, with epoxy resin changed in type. From the figure, it may be surmised that the crack resistance is effectively improved by making the molding compound tougher. Even in this case, a tougher resin has the disadvantage of a low glass transition temperature.

3-4 Increasing Adherence

As shown in Figure 23, an increase in adhesive strength tends to improve crack resistance. A higher adhesive strength to silicon chips is one of the items critical for the prevention of corrosion in aluminum wiring. It is difficult, however, to prevent a package from cracking while soldering using an adherence improvement technique only. A combination of techniques using the methods referred to above will eventually be required.

4. Performance of Materials Developed

Given in Table 1 is a list of characteristics available in a molding compound having low stress. The new molding compound which has been developed by a well-balanced combination of the above methods for a thinner type package has a low coefficient of thermal expansion and a low moisture absorption. It shows excellent performance as a molding compound for surface mounted devices (Figures 24 and 25).

5. Summary

This paper has referred to the techniques used in developing a molding compound for thinner type packages.

1) Reducing stress: It is important to use the most suitable silicone polymer and silica.
2) Preventing a package crack while soldering: It is necessary to lower moisture absorption, decrease the modulus of elasticity, and to make the

package tougher. All of them, however, tend to lower the glass transition temperature. Our newly developed epoxy resin enabled us to improve upon the above-mentioned characteristics while keeping a high glass transition temperature.

Apparently, packages will be more and more progressively diversified from now on. As a result, a molding compound will be required to meet the severer characteristic requirements. It is necessary to continue technologically innovating epoxy molding compounds, including silicone polymer, silica, and epoxy resin technologies.

References

[1] Nikkei Microdevices pp. 32-35, 8, 1988
[2] Nikkei Microdevices pp. 32-40, 6, 1990

Fig. 1 Trend of IC Package

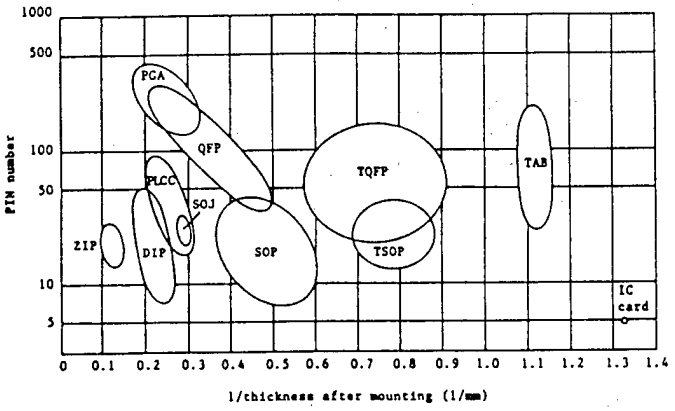


Fig. 2 TSOP as Percent of Total Memory Package

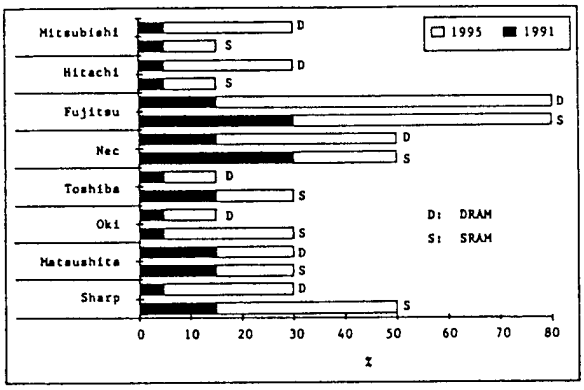


Fig. 3 Development of EMC for SMD Package

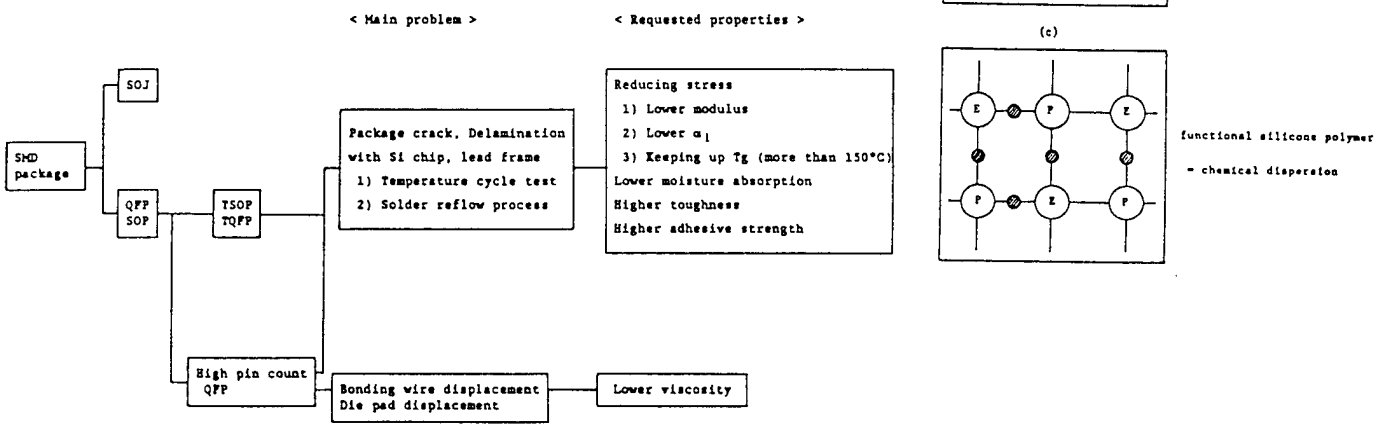


Fig. 4 Effect of Silicone Polymer for Reducing Stress

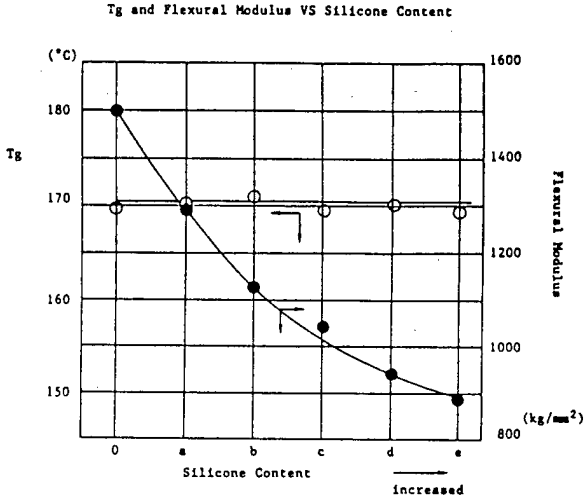


Fig. 5 Morphology Control

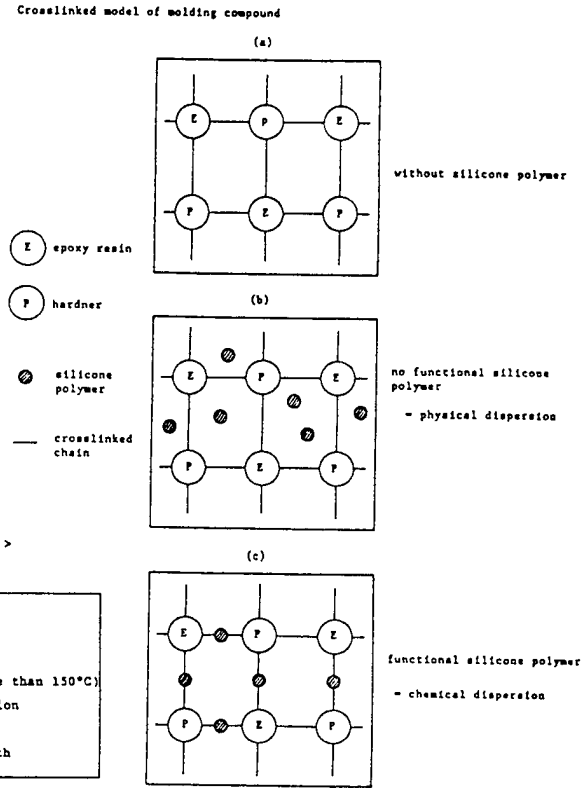
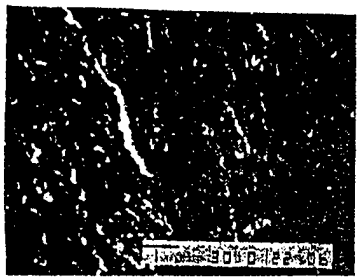


Fig. 6 SEM View of Silicone Domain

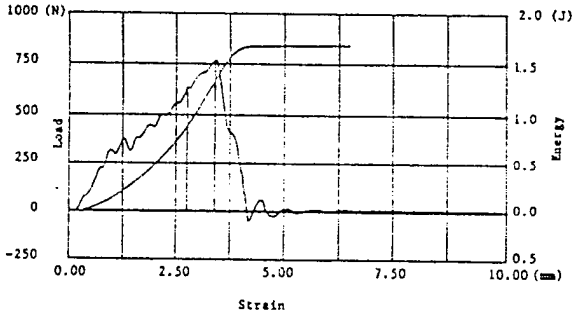
Example of physical dispersion



Example of chemical dispersion

Fig. 9 Impact Resistance

by Graphic Impact Tester TOYO SEIKI



Influence of Domain Size

Fig. 7

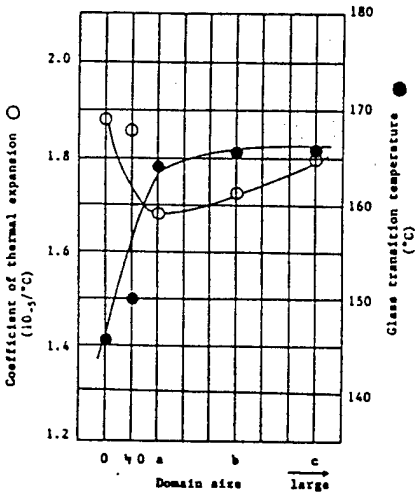
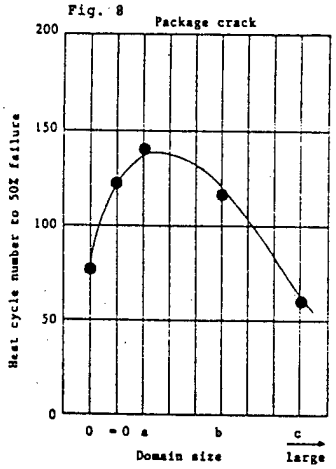


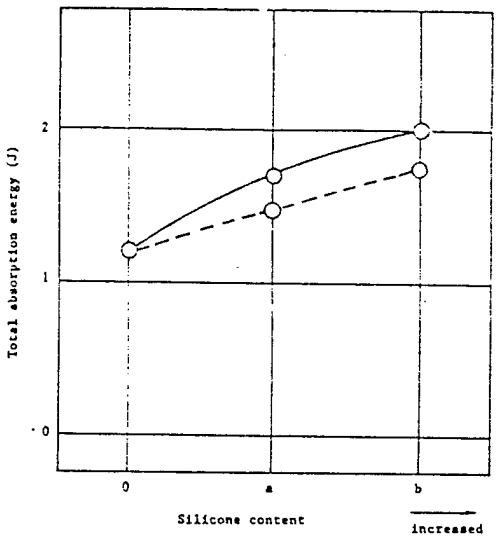
Fig. 8



Test condition
Package : 14 pin DIP
Chip size : 4.0 x 9.0 x 0.6 mm
Heat cycle: 260°C to -196°C
(30 sec) (60 sec)

Fig. 10 Impact Resistance

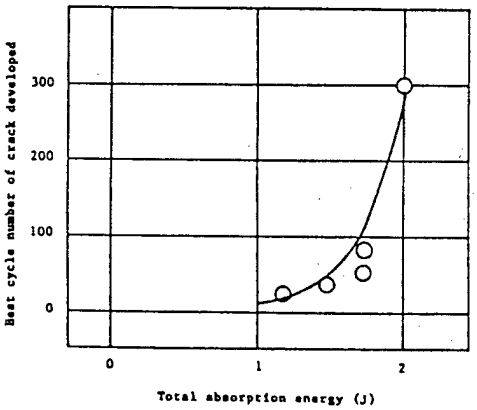
vs Silicone Content



Silicone modifier A (Optimum domain size)
Silicone modifier B

Fig. 11 Crack Resistance

vs Impact Resistance



Test condition
Package : 14 pin DIP
Chip size : 4.0 x 9.0 x 0.6 mm
Heat cycle: 260°C to -196°C
(30 sec) (60 sec)

Fig. 12 Physical Properties vs Silica Content

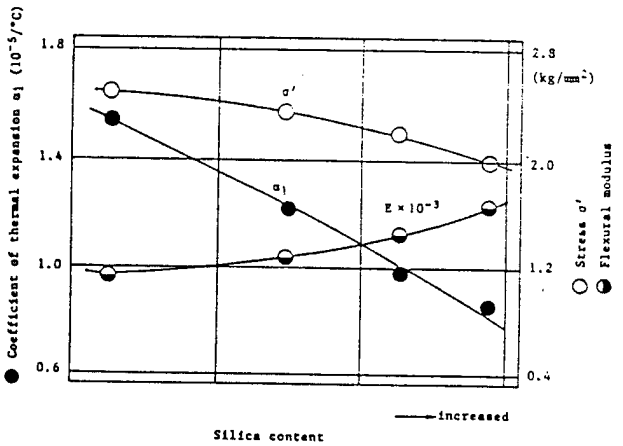


Fig. 13 Lowering Melt Viscosity

1) Mooney's equation

$$\ln\eta = K_e\phi/(1 - \phi/\phi_m)$$

η ; Specific viscosity

K_e; Einstein's constant

ϕ ; Volume ratio of filler

ϕ_m; Closest packing rate

2) Fuller's ideal curve for closest packing

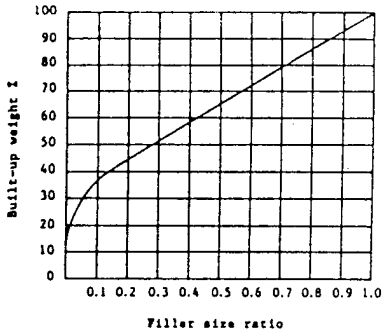


Fig. 14 Spiral Flow vs Silica Content

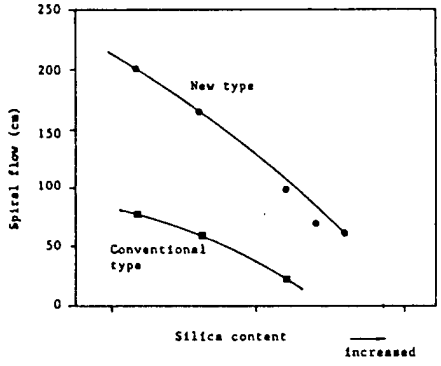


Fig. 16 Porous Volume of Spherical Silica

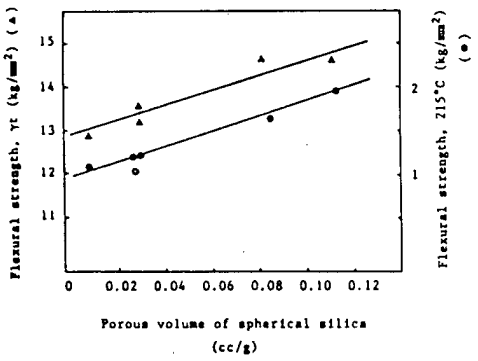
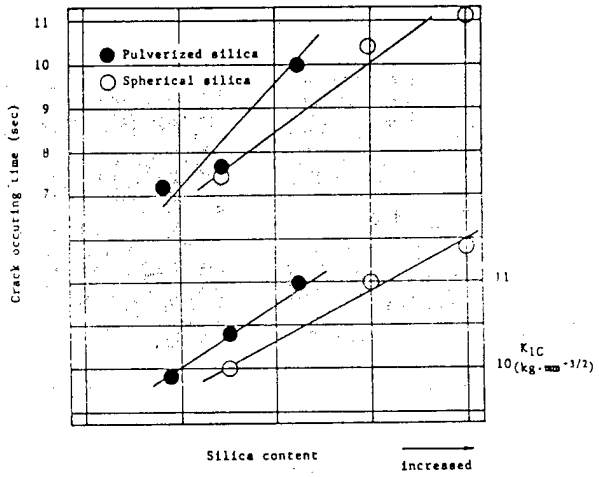
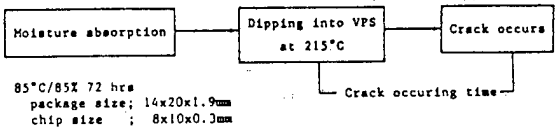


Fig. 15 Fracture Toughness, Crack Resistance



- K_{1c} ; Stress intensity factor
- <Method of measuring the crack occurring time>



85°C/85% 72 hrs
package size; 14x20x1.9mm
chip size ; 8x10x0.3mm

Fig. 17 Lowering Moisture Absorption

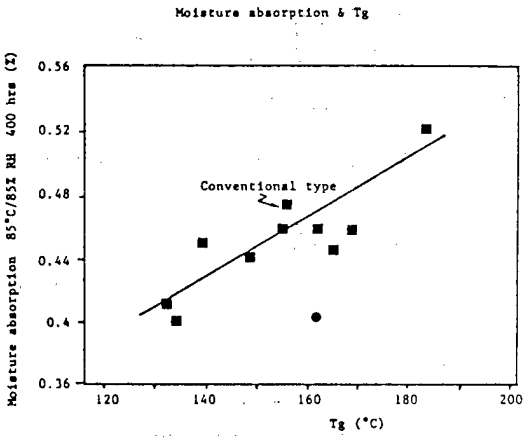


Fig. 18 Diffusion Constant & Tg

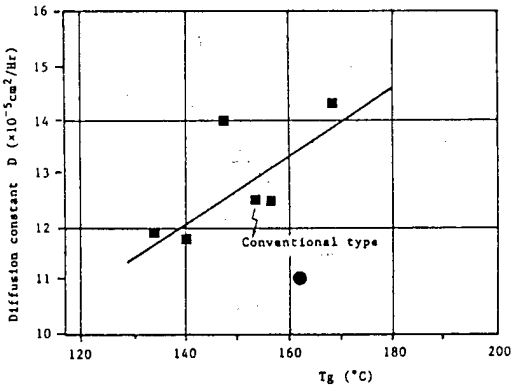
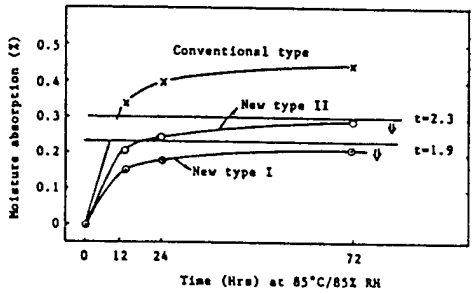


Fig. 19 Crack Resistance at Solder Process



Frame material ; 42 alloy
Package size ; 14 x 20 x t mm
Chip size ; 8 x 10 x 0.3 mm
Soldering condition; 240°C/10 sec

	t=1.9	t=2.3
◉	No crack	No crack
○	Crack	No crack
X	Crack	Crack

Fig. 20 Flexural Modulus vs Crack Resistance

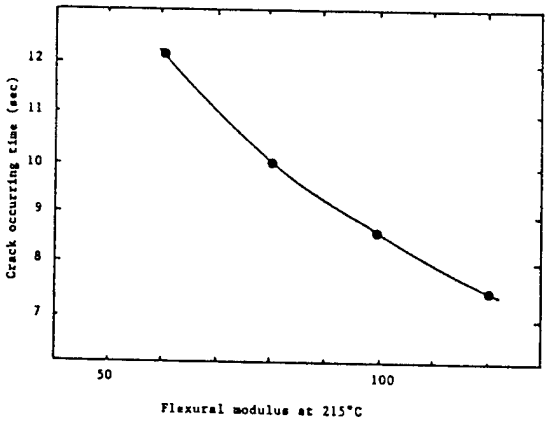


Fig. 21 Lowering Modulus at 215°C

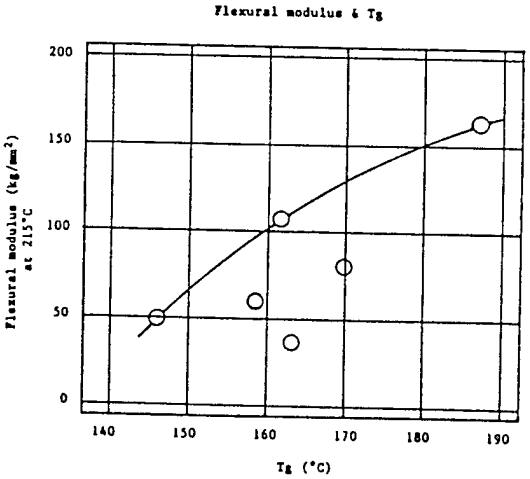


Fig. 22 Stress Intensity Factor (Klc) vs Crack Occurring Time and Tg

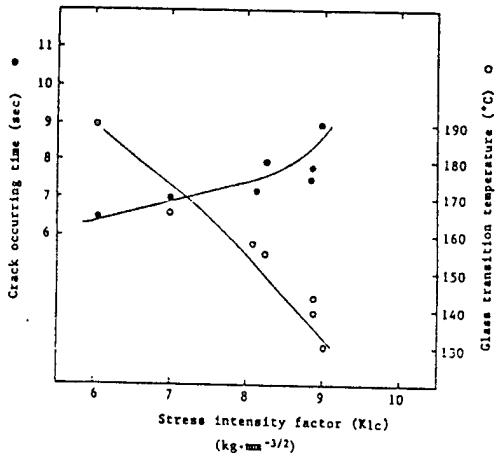
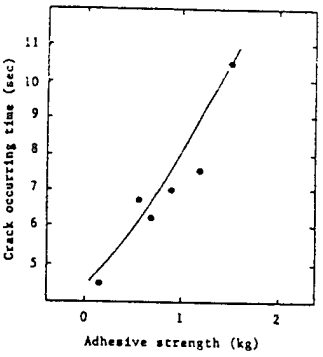


Fig. 23 Adhesive Strength to 42 Alloy



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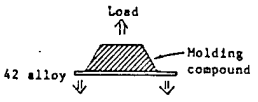


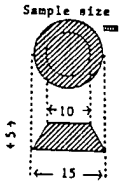


Table 1 Low Stress Molding Compound

	KMC163VA	KMC180VA	KMC188	KMC184VA	Newly developed type
Low stress	o	o	o	o	o
Low thermal expansion		o	o	o	o
Low moisture absorption					o
Low modulus at high temperature	o				o
High adhesive strength				o	o
Spiral flow, 175°C (cm)	28	24	30	32	30
Gelation time, 175°C (sec)	18	18	17	20	22
Melt viscosity, 175°C (poise)	350	450	280	250	250
Coefficient of thermal expansion,					
50-100°C (10^{-5}/°C)	1.6	1.3	1.3	1.3	0.9
190-240°C	7.0	5.8	5.8	5.8	3.7
Flexural modulus, 215°C (kg/mm²)	100	130	160	140	110
Flexural strength, 215°C (kg/mm²)	1.2	1.5	2.2	2.0	2.0
Water absorption (%)					
85°C/85% RH 24H	0.30	0.22	0.32	0.33	0.15
100H	0.43	0.33	0.43	0.42	0.26

Fig. 24 Package Crack after Soldering

< TSOP >

Package ; 18 pin TSOP (Thickness 1mm)
Pretreatment condition; 30°C/85%RH
Soldering ; 260°C, 10 sec, solder bath

Crack failure (%) after solder dipping

	Pretreatment time (Hrs)			
EMC	16	24	48	192
New type	0	0	0	0
General type	0	40	100	100

< SOJ >

Package ; 4MDRAM 20 pin SOJ (350mil)
Pretreatment condition; 85°C/85%RH
Soldering ; VPS (215°C), 90 sec

Crack failure (%) after VPS

	Pretreatment time (Hrs)		
EMC	48	72	168
New type	0%	0	0
General type	40	60	80

< QFP >

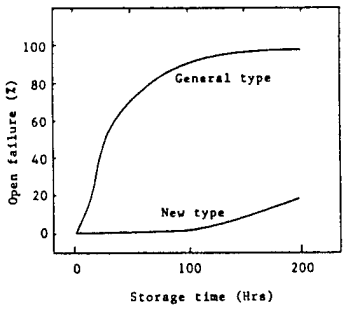
Package ; 14 x 20 x 2.3mm 64 pin
Pretreatment condition; 85°C/85%RH
Soldering ; 240°C, 10 sec, solder bath

Crack failure (%) after solder dipping

	Pretreatment time (Hrs)	
EMC	24	50
New type	0	0
General type	100	100

Fig. 25 Aluminum Corrosion Test

Package; 20PIN SOP 5.2 x 12.5 x 1.8 mm
Chip ; without passivation layer, 2 x 4 x 0.3 mm
Pretreatment condition; 121°C PCT 24 Hrs + 260°C/10 sec solder dipping
Test condition; 121°C PCT



MULTILATER LEAD FRAME ON PRINTED CIRCUIT BOARD TECHNOLOGY

Atsushi Hiroi, Katsumi Sagisaka, Tsukasa Yamamoto
Mitsuhiro Kondo, Kouji Ukai

INTRODUCTION

Plastic QFP is widely used in the high pin count package field. (see Fig.1) Lead frame play the role of both wiring and structure material.The progress of LSI brings the requests for the many properties such as fine inner lead corresponding to small IC chip size (see Fig.2),reduction of lead inductance for high frequency sigal and high heat dissipation structure.

There exists one of the good answer for the above request,which is the conbination of the conventional lead frame and multilayer printed circuit board technology. This paper describes newly developed lead frame concerning about 1. Basic structure,2.General Properties,3.Features,4.Design rule,5.Reliabilty in detal.

1. BASIC STRUCTURE

Basic structure is shown in Fig.3. This lead frame consist of the insulatin layer on inside of the transfer mold area with conductor that is electrolicaly conected with internal lead frame .Glass/triazin is adopted for the insulation layer that is used in the plastic PGA.The copper foil is applied for the conductive layer.Through hole is performed cupper plating. Embodied lead frame has the same connection between outer conductor and internal lead frame like inner layer connection of multilayer printed circuit board by plated through hole.

Thickness of insulation layer made by glass/triazin is 0.3mm.Glass/triazin laminated 3 ply 0.1mm glass cloth.Triazin resin have the good properties such as a approximately 200℃ glass transition temperature,low dielectric constant and dissipation factor.Thickness of copper foil is 18 μm with 15 μm plated copper. Wire bondig area is coverd with nickle and gold plating.

In other words,this structure is considered for the multilayer PCB with outer lead or metal core printed circuit board with exposed inner layer metal as a outer lead.

2. GENERAL PROPERTIES

General properties are devided into electrolical properties and phisical properties.Table 1 shows the electrical propeties that indicate the almost same propeties of printed circuit board. Table 2 shows the physical properties that indicates the medium properties between lead frame and PCB material.

Surface resistance and volume resistance reaches more than 10^{13} Ω.Concerning about dielectric

constant and dissipation factor, this table illustrates little bit higher but almost the same value as insulation material. Lead resistance have no problem even if is connected via plate through hole. Compared with the normal PCB with same thickness, capacitance value is bigger under the innerlayer metal effect. Characteristic impedance is controlable with in 15% like multilayr PCB.

Specific gravity is from 3.6 to 4.2 depending on the structure. In case of Yang Mogulous value, it superior to the conventional PCB with same thickness. Water absorption and impurities is almost same value as the conventional transfer mold resin. Bow and twist indicates less than 0.5% owing to the good combination of the copper alloy and printed circuit material. Bondability of the gold plated surface indicates enough properties that are in practical use for the plastic PGA as a chip on board.

3. FEATURES

Compared with the conventional lead frame, main characteristics are as follows.

1) It is possible that perform the less than 0.15㎜ fine inner lead pitch.

2) Easy to built the multilayer structure.

3) Easy to attach the heat sink with the execellent heat dispersion.

4) Easy to reduce the lead inductance under the design flexibility with multilayer structure and through holes.

5) Mountable on the both side of the lead frame as for bonding side and the back side. (chip components like chip capacitor)

6) Multi chip package in the standard plastic package body size is available.

To sum up, inner area of the plastic package body is allowed to design like multilayer printed circuit boards.

4. DESIGN RULE

Design rule is classfied into the surface area , inner layer PCB construction and lead frame. (see Fig.5 and Fig.6) It takes same fine pitch pattern reached to 0.15㎜. The normal diameter of the land is 0.5㎜ and the diameter of the drill tool is 0.3㎜. The minimam space from through hole egde to the board edge is 0.4㎜. What we call solder mask is applied on the inner lead pattern to save the gold plating area for cutting in in price. The multilayer structure is permited to built up till the limit of the thickness on the transfer mold technology under the condition of the 0.2㎜ thickness symmetrical insulation layer from the center of the lead frame. (see Fig.7) If necessary, milling process can be applied on the die pad area to control chip mounted height. To improve the heat dissipation property, lead frame can be exposed by sever controled milling

operation.

Further more the heat dissipation property is needed, copper and copper-tangsten material heat sink which is exposed after transfer mold process is easy to attached on the rigid and insulation PCB material. (see Fig.8) Standard structure is consist of the three layer that the surface conductor is inner lead bonding pattern, involved lead frame is grand plane and back side of conductor layer is utilized for power plane. If require d, heat sink can be connected to the grand plane.

Fig.6 shows the design rule that makes it possible to form the 0.3mm fine pitch outer lead by using the 0.3mm diameter drill with cross stech form. The standard thickness of the lead frame material is 0.15mm but there exists the no limitation in case of under 0.25 mm thickness. Standard lead frame material is copper alloy family.

5. RELIABILITY

High reliablity is recognized in result under the evaluations based on the sevral main specifications refer to printed circuit board and semiconductor devices. (see table 3) Depending upon IPC, MIL and JIS standerd, the reliability of the connection by the plated through hole from outer lead frame to inner leads bonding pads result in almost the same high reliablity of the multi layer PCB's.

Fig.9 shows that pull strength is independent of the hole diameter and the shape of the connec tion area High reliability is confirmed to reach the working limitation of the lead frame. In conclusion, there is no need for transfer mold injection to get high pull lead strength. In other words, This forms the printed circuit board with high pin count outer leads that is impossible to fix after final assembly process.

CONCULUSION

The semiconductor outline committee of Electronic Industry Association of Japan standerdize the dimesion of plastic package. On the contrary to the progress of standerdization with the progress of the semiconductor, inner lead operation of connection is groping for reasonable methods. Even if the hard study of the technology of the PCB and lead frame combination, there exists the no answer in solution for the latest problem. Utilizing the conventional through hole technology, newly developed multilayer lead frame - PACKTHOL answers the this problem that have not been solved by present.

As for based on the basic conbination of the conventional lead frame technology and the conventional multilayer technology, the application covers the wide range in the high pin count package field.

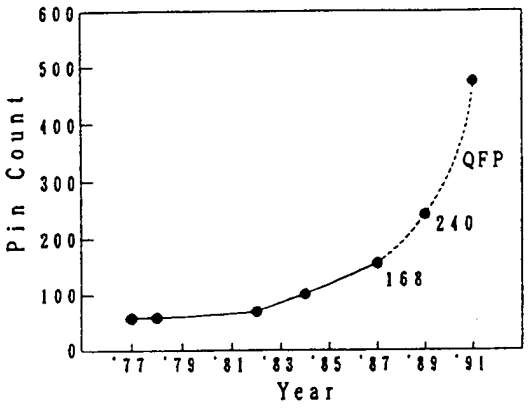


Fig. 1 Pin Count of Gate Array Device

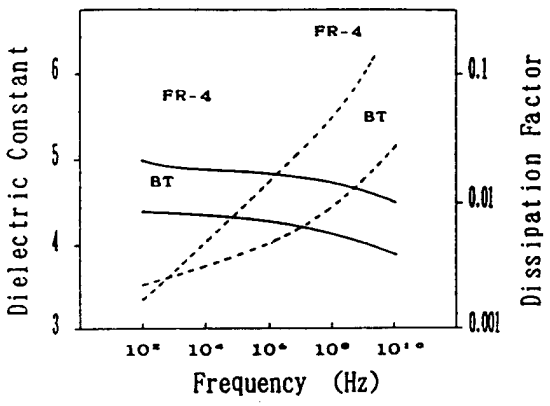


Fig. 4 Frequency Characteristics of Dielectric Constant and Dissipation Factor

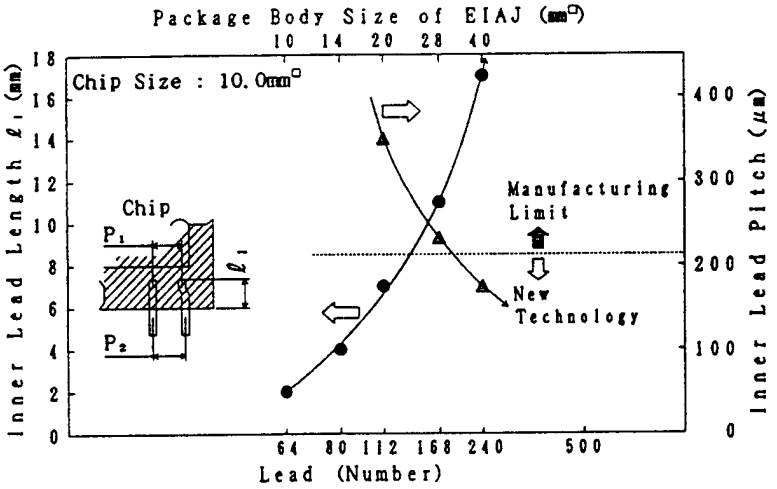


Fig. 2 QFP Lead Frame Design Limits

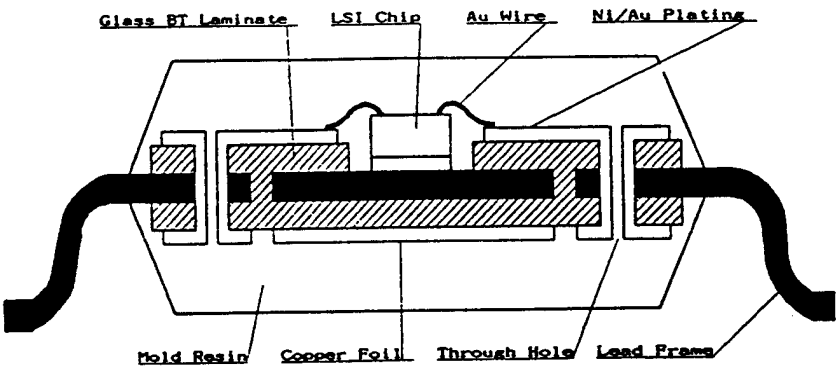


Fig. 3 Basic Structure

Table 1.Electrical Property

TEST ITEM		UNIT	CONDITION	VALUE
Surface Resistance		Ω	C-96/20/65	10^{13}~10^{14}
Volume Resistivity		Ω · cm	C-96/20/65	10^{14}~10^{15}
Dielectric Constant		——	C-96/20/65 (1MHz)	5.3
Dissipation Factor		——	C-96/20/65 (1MHz)	0.007
Conductor Resistance	L/F	Ω	C-96/20/65	0.01~0.02
	T/H			0.7 ~ 0.8
Electrical Capacity	PCB	pF	C-96/20/65 (1MHz)	30.0~31.0
	PCB L/F			47.0~48.0
Impedance	75Ω	Ω	C-96/20/65	±10~15
	50Ω			±10~15

CONDITION

A. Without perconditioning
C. Isothermal humidity
D. Isothermal water
E. Isothermal enviroment
S 4. solder float at 260 ℃×20sec

Table 2.Physical Property

TEST ITEM		UNIT	CONDITION	VALUE
Specific Gravity		——	A	3.6 ~ 4.2
Yang Mogulous		Kg/mm²	A	2000~2100
Peel Strength	35μ	Kg/cm	A	1.4 ~ 1.6
			S4	1.4 ~ 1.5
Water Absorption		wt%	E-24/50 + D-24/23	0.1 ~ 0.15
Impurities		ppm	D-20/121	under 1.5
Bow and Twist		%	A	within 0.5
Surface Solidity		——	A	60.0~70.0
Bondavility		ε	A	more than 7.0 (B.C mode)

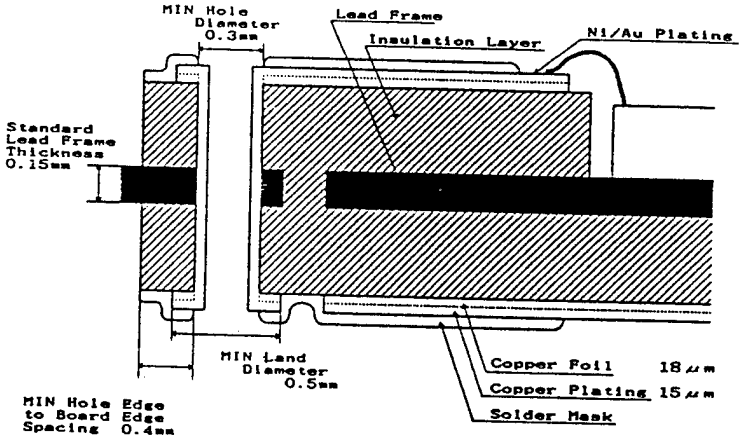


Fig. 5 Standard Design Rule-1

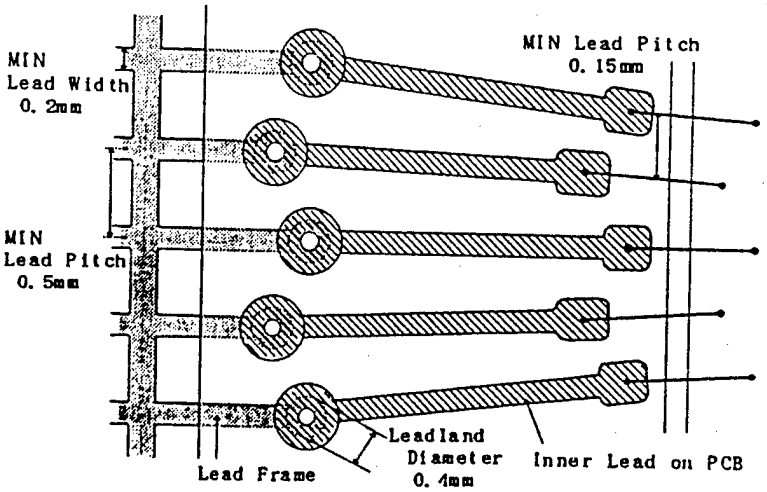


Fig. 6 Standard Design Rule-2

	Stadard Structure	
2 layer	Outer layer	0.1t (18μm)
	Prepreg	0.1t×2
	L/P	0.15
	Prepreg	0.1t×2
	Outer layer	0.1t (18μm)
3 layer	Outer layer	0.1t (18μm)
	Prepreg	0.1t×2
	L/P	0.15
	Prepreg	0.1t×2
	Outer layer	0.1t(35/18μm)
4 layer	Outer layer	0.1t(18/35μm)
	Prepreg	0.1t×2
	L/P	0.15
	Prepreg	0.1t×2
	Outer layer	0.1t(35/18μm)
4 layer Blind VIA	Outer layer	0.2t(18/18μm)
	Prepreg	0.1t×2
	L/P	0.15
	Prepreg	0.1t×2
	Outer layer	0.2t(18/18μm)
6 layer	Copper foil	18μm
	Prepreg	0.1t×1
	Inner layer 1	0.1t(35/35μm)
	Prepreg	0.1t×2
	L/P	0.15
	Prepreg	0.1t×2
	Inner layer 2	0.1t(35/35μm)
	Prepreg	0.1t×1
	Copper foil	18μm

Fig. 7 Multilayer Structure of PACKTHOL

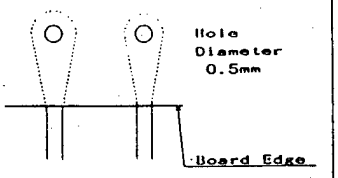
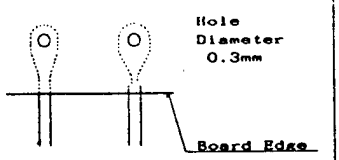
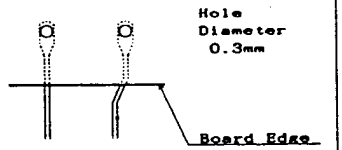
Leadland Configuration	Strength
	50Kg/mm²<
	50Kg/mm²<
	50Kg/mm²<

Fig. 9 Lead Tensional Strength

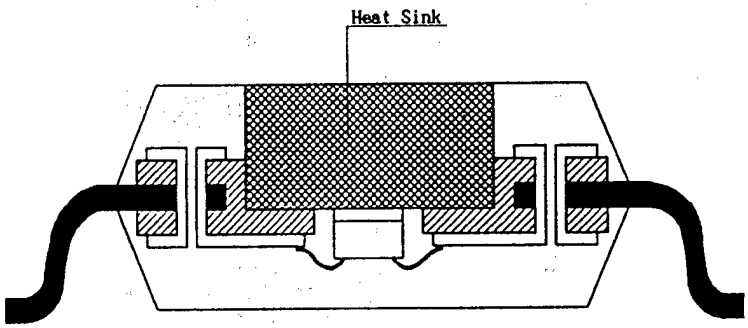


Fig. 8 Package Structure (Heat Sink Type)

Table 3.Reliability

VALUATION ITEM	CONDITION		EVALUATION	RESULT
Heat Resistance	E-1000/150		No blister, No delamination. No through hole crack	0/20
Solder Temperature Resistance	260 ℃ 20sec	DIP	No blister, No delamination. No through hole crack	0/20
		FROAT		
Heat Shock	-65 ℃ ⟷ 150 ℃ 1000 Cycles		electric resistance conductor 10% >	0/10
Oil Dip	26 ℃ ⟷ 260 ℃ 100 Cycles		electric resistance conductor 10% >	0/10
Isothermal Humidity	C-1000/85/85 30V		insulation resistance value $10^4\Omega$ >	0/10
Pressure Cooker Test	C-500/121/100		No blister, No delamination	0/10
Chemical Resistance	A	boiling $CHCl_3$ 5min	No blister, No delamination	0/10
		CH_2ClCH_2Cl (35 ℃±2) 5min		0/10
		33%NaOH (40 ℃±2) 2min		0/10
Lead to Lead Dielectric Strength	A (Lead Pitch 0.5mm~2.0mm)		1.0KV >	0/25
Lead Bending	A (Lead Width 0.1mm~1.0mm)		2.0 Cycle >	0/25

Wednesday, October 24, 1990
17:00-17:35

Surface Mount Technology for LSI-Package

Kenshu Oyama, Kyushu Matsushita Electric Co., Ltd.
Fukuoka, Japan

LSI パッケージ実装技術

小山　賢秀
九州松下電器㈱
生産技術事業部商品企画課長

1 Introduction

The advance of electoronics is so rapid these years that such products as a camcorder, a cellular phone, a personal computer and a palm-top memo are becoming more and more attractive with respect to their size , weight and capability. A camcorder is the most advancing and leading product in SMT(surface mount technology) due to its highly competitive business environment. This far-advanced SMT has been tranferred to a personal computer, making it smaller and handier from lap-top type to note-book type,and further way down to palm-top type. That is also the case with a cellular phone. In the near future, the probability is that a telephone is combined with a personal computer in order to add communication capability . From the viewpoint of surface mounted components, miniature chip components and a high lead-density QFP are the major keys to compact design for a PCB. Chip components as small as 1608(1.6mm long and 0.8mm wide) and QFP with leads on 0.5mm centers have so far contributed to the improved product design . However, there is no end to the needs of better and newer products. To meet the further needs of a camcorder and a cellular phone, chip components 1005 and a QFP with leads on 0.3mm centers are expected to be developed for commercial use. This paper will address process-oriented approaches to SMT for high density LSI packages.

2 High density SMT

2-1 Miniaturization of LSI packaging : higher pin-count and finer lead-pitch

A high pin-count LSI is required not to exceed certain out-line dimensions in spite of its natural needs because of the followng reasons:

(1) An LSI as well as chip components is expected to be so small that it occupies only so much area in a PCB.

(2) Solder defects can be encountered on a large LSI due to the PCB deflection during reflow process.

This will inevitably result in higher lead-density packaging for a high pin-count LSI. In this context, the maximum allowable LSI package outline is normally assumed to be 40mm square. 30mm square, however, is the recommended dimensions to meet the current manufacturing capabilities. The relationship between pin-count and lead-spacing according to Fig1 indicates that those packages with 300 pins on 0.5mm centers, with 400 pins on 0.4mm centers, or with 500 pins on 0.3mm centers are practical. These packages are expected to be available within a few years, which will eventually force SMT to be upgraded. Fig2 shows the trend of QFP packages. Aside from a large LSI package with hundreds of leads, one with less than a hundred leads can be designed to be small enough to contribute to the

product needs of being smaller and lighter. However, that can not be expected of a conventional lead-frame package, for the gull-wing formation requires a certain length of inner leads to be molded in the plastic package. It is thin copper-lead for TAB that enables an LSI package to be designed to be smaller. Fig 3 shows an example of a thin copper-lead package. Because surface mounting process and reflow process are sequentially divided, it enables mass components to be mounted with high speed and attached to the PCB at the same time. But when it comes to the placement of a high pin-count LSI, it is confronted with such defects as solder bridging, solder balls and a lack of lead co-planarity. Therefore, some manufacturers prefer a spot reflow soldering technique just for LSI packages. Although it assures reliable soldering, it offers the disadvantages in time and cost over mass reflow soldering. Precise placement of an LSI with high pin-count and fine lead-pitch is another requirement. A PCB is usually populated with chip components as well as those LSI packages. If conventional chip mounters and a mass reflow soldering process are available, it is economical and efficient to add a new dedicated LSI mounter alone to the existing facilities.

2-2 Micro connecting approach

As mentioned above, LSI package design must change as the lead-pitch gets finer than 0.5mm. Conventional processes from solder printing, chip mounting through reflow soldering are adaptable to 0.4mm lead-pitch QFP with some improvement in solder paste, printing process and mounting accuracy. However, when it comes to 0.3mm lead-pitch, solder bridging becomes a major defect, which requires the current mass reflow process to be improved. Fig4 indicates the comparison of area occupied by various types of devices. An LSI with a lead spacing less than 0.3mm can be realized by means of thin copper-lead , whereas 42 alloy lead frame is the most popular for an IC with a normal lead spacing. TAB makes use of thin copper-lead. Beyond TAB go wire-bonding, flip-chip and micro-bump, as the level of integration in an LSI steps up.

2-3 Wire-bonding or TAB?

It is still a question whether wire-bonding or TAB is advantageous for inner-lead bonding in an LSI package with high pin -count and fine lead-pitch. TAB is capable of gang-bonding, which is more efficient but less reliable than wire-bonding. If bonding reliability is a critical issue, then single-point-bonding by means of conventional wire bonding is preferable to TAB. Wire bonding, however, has a constraint regarding wire loop length, which offers a break-point between TAB and wire bonding. According to Fig5 and Fig6, the break-point is located somewhere between 200-pin and 250-pin. Generally speaking, TAB is applicable to a high pin-

count LSI package with 300 pins or more, and wire bonding is restricted to lower pin-count.

3 Soldering reliability and process

This chapter will discuss techniques of mounting and soldering chip components and analyze their technical issues. It is evident that a soldering technique has been and will still be the most popular and conventional, though not perfect enough, because of the following reasons.

(1)Low melting temprature (below 200°C)
(2)Self-alignment effect
(3) Visco-elastic at room temperature providing stress relaxation against vibration and deflection.
(4)Mature technique ever since B.C. era
(5)Simple and easy handling technique

3-1 Requirements for a soldering process

Listed below are the requirements for a reflow soldering process.

(1) No bridging and open
(2) Adequate solder paste supply to form a well defined fillet
(3) Wettable
(4) Few solder bolls
(5) Easy to be cleaned
(6) Able to firmly hold components

Some of the major solder defects are shown in Fig7. Lack of solder joint due to a lead bent upward is almost inevitable, even though solder volume and PCB warp are appropriate, if co-planarity of the leads is beyond a certain limit. An alternative to the conventional procedures of package supply is the requirement to prevent the leads from being bent upward. In the following sections, 3-2 and 3-3, how solder bridging and solder balls take place will be summarized.

3-2 Solder bridging

As illustrated in Fig8, solder bridging is solder shorting of spacing between two or more components. It occurs when a portion of solder paste is spread out of the pad by some reasons. One of the reasons can be that a portion of solder paste crawl down to the underside of a screen if there is any lack in parallel between a PCB and the screen. If solder volume and solder wettability are adequate, the solder spread-out is absorbed back to where it should be.

3-3 Solder balls

Solder balls as well as solder bridging result from the solder spread-out. Besides,they can be promoted even without the solder spread-out if the solder paste is oxidized. Fig9 illustrates that oxidized solder particles get drifted on the flux as solder balls while they are heated up to their melting temperatrue. Conventional solder paste consists of non-uniform particles, which expose more surface area to the air than uniform particles resulting in more oxidization. Solder balls can get on the increase depending upon the flux, for the prime duty of the flux are to remove oxides and to protect the surfaces from re-oxidation. Fig10 indicates the cause-and-effect of solder bridging and solder balls.

4 SMT for LSI with leads on 0.3mm centers

This chapter will concern itself with SMT for fine lead-pitch LSI, especially a mass reflow soldering technique regarding LSI with leads on 0.3mm centers, bacause the technique has many advantages over any other alternative.

4-1 Solder fillets and solder volume

Fig11 shows the calculation results of a simplified model of solder fillets and volume required. According to Fig11, the amount of melt solder with the equivalent thickness of 44 μm is enough to make up a proper fillet. This amount is equivalent to 88μm-thick solder paste. More precisely speaking,the solder volume required for screen printing can be less than that thanks to the solder pre-coats on the leads and the pads. Actually, however ,extra solder paste is added during the screen printing operation to make up for leads co-planarity. This conception is not adaptable to the case with LSI lead-pitch shrunk down to 0.3mm, for solder bridging becomes more common. Fig12 shows solder paste printed for pads on 0.3mm centers at varying dimensions of the leads. If the minimum requirement of solder volume can be supplied by the solder pre-coats on the leads and the pads with little solder paste printed, the conventional mass reflow soldering technique is applicable to a finer lead-pich LSI. A copper-lead instead of a 42 alloy lead, necessitates only 10μm-thick solder, which is fulfilled by the pre-coat on the pad. It , however , runs short of physical strength. This can be complemented by fixing the plastic package of an LSI to a PCB. The model of solder pre-coat is exhibited in Fig13.

4-2 Measures for co-planarity

Leads of QFP are so sensitive that they get bent easily during burn-in, packing, transportation and baking. It is hard to expect them not to be bent beyond a certain limit of co-planarity prior to placement. An alternative to the current operations is to cut and bend the leads just prior to placement on or off the mounter. This will render a mounter maker, instead of an IC maker, accountable for normal co-

planarity of the leads. *Tape-Pak* proposed by *National Semiconductor* makes this alternative realized, as shown in Fig14. A flat-lead QFP or a molded TAB is another package for this alternative, enabling burn-in as they are and cut-and-bend right before placement. Copper leads on a molded TAB are subject to bend, though solder suppy is not enough, requiring an improvement in firm attachment between the leads and the PCB. This improvement was discussed above and is shown in Fig16.

4-3 The thickness control of solder pre-coats

Solder pre-coating is generally carried out by plating or levelling. The former has the disadvantage in cost to the latter. The latter tends to expose a copper-tin compound on the surface. Because this exposure aggravates wettability, the material and supply are essential in order to keep the pre-coats uniform. Fig17 shows pre-coating reported lately. This pre-coating technique is easy and able to control the solder thickness in micron-meter without the exposure of a copper-tin compound. It is an effective and indispensable technique for attachment of a fine lead-pitch LSI.

4-4 Highly precise placement

Placement accuracy is an important factor for reliable attachment of an LSI with leads on 0.3mm centers. The versatile chip mounter , CM 92P manufactured by KME(*Kyushu Matsushita Electric Co., Ltd.)*, has been able to place a QFP in 2.5 seconds by means of an optical vision system with a CCD camera pattern-recognizing all the leads of a QFP by one shot. This optical system can not help but constrain the applicable outline dimensions of a QFP within 30 mm square. Besides, it needs additional detector to pick up leads bent upward. A new technique has been developed by means of laser, solving all those problems and enabling to handle an LSI with larger outline dimensions up to 50mm square and with leads on 0.3mm centers. Fig18 shows how laser detects all the leads and Fig19 exhibits laser output signals.

4-5 How to detect leads bent upward and sideward

As the lead-pitch of a QFP gets finer, leads bent even slightly become a major cause for solder defects. To detect leads bent is now a necessity for a chip mounter. The laser detector enables a QFP with leads bent to be removed in advance of placement, resulting in the improvement in soldering reliability.

4-6 Reflow soldering of fine lead-pitch LSI package

The basic design concept of an LSI package has been proposed above. According to it ,an original LSI package with 212 leads on 0.3mm centers has been made by KME.

Fig21 shows this LSI package attached with solder and Fig22 shows the configurations of the solder fillets. No solder paste but the pre-coats on the leads and the pads was provided, fixing the LSI in advance of a reflow process with the help of the flux. Fig23 indicates that soldering was successful with the pre-coats alone, showing no solder bridging and solder balls. However, unless co-planarity of the leads is within an allowable degree, it falls short of solder adhesion resulting in an open, as shown in Fig24. It is recommended that co-planarity is controlled to be below 20 μm considering the thickness of pre-coats and the flatness of a PCB. The concept and technique descussed above offer reliable forming of the leads as a key issue.

5 Future trend of SMT

5-1 Molded dice or bare dice

Further pursuit of more compact packaging in density and volume leads to direct placement of bare dice onto a substrate. But some problems still remain to be overcome. One of them is the reliability of bare dice. Bare dice normally pass through few tests and inspections, whereas molded dice are subject to various tests and inspections. Any defect or mal-function in bare dice encountered after attached onto a substrate is hard to be traced back. Bare dice must be handled more carefully than molded dice, requiring preventive measures for surface corrosion, clean environments and a lot of efforts in process control. Difficulties in repair work and quality control with regard to bare dice are also impediments to be removed. Although bare dice confront those problems and impediments, it is apparent that they are ultimate and indispensable devices for high density SMT. It is generally admitted that digital ICs will be supplied as bare dice owing to their ease of testing, and analogue ICs will go with molded packaging to facilitate testing and screening.

5-2 Flip-chip

A flip chip can be gang-bonded with its face down onto a substrate, suitable for thinner packaging. Fig25 shows a flip chip with solder bumps. It is already prevalent among main frame computers and automobile electronics. It has a minor disadvantage in cost, for 3-layer barrier metals are utilized to protect aluminum pads on the chip from solder. A stud-bump technique is now proposed to remove this disadvantage, which is shown in Fig26. Here, gold is used for bumps and silver paste as adhesive. Solder can work as adhesive instead of silver paste, as shown in Fig27. Solder is pre-coated and controlled to be 30~40μm thick, melting through a reflow process. Low-cost barrier metals, however, are still required to protect aluminum pads on the chip from solder. The major advantage is that it is allowed to go through a mass reflow soldering process, as shown in Fig28.

5-3 Future development

The concept and activities for SMT concerning an LSI with leads on 0.3mm centers have been introduced with some suggestion and orientation of future SMT. Now that it is not a mature process technique yet, it must be improved and upgraded in accordance with the demand of the market. This will be enhanced if those related suppliers, such as a device maker, a chemical maker and an equipment maker, get along in some joint program for the process development. In addition to that, application of this process technique to electronic products is indispensable. As an equipment maker, KME will pursue and develop a better process technique.

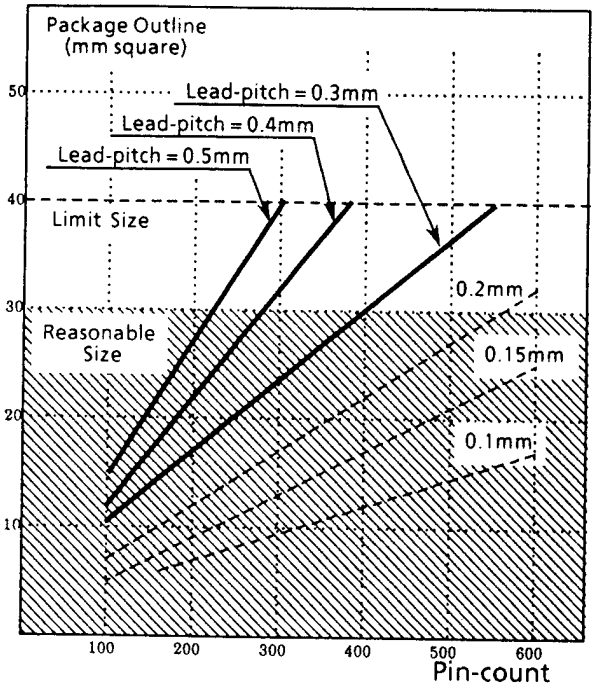


Fig.1 Lead-pitch & Pin-count of QFP Package

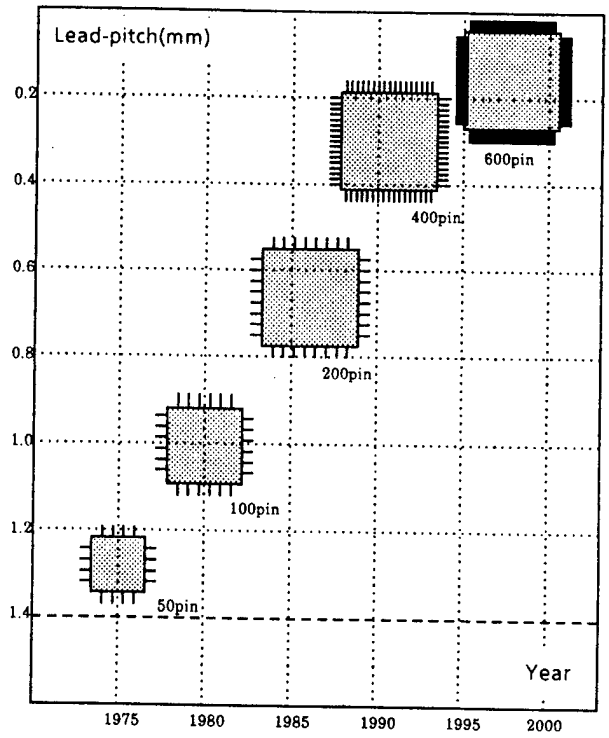


Fig.2 Trend of QFP Package

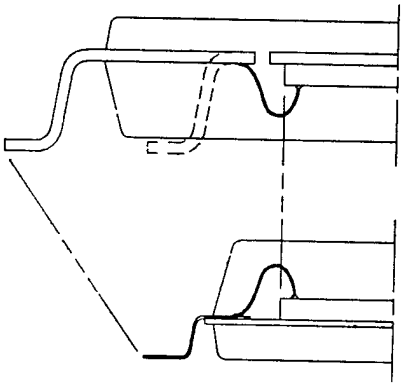


Fig.3 Small Package with Thin Lead

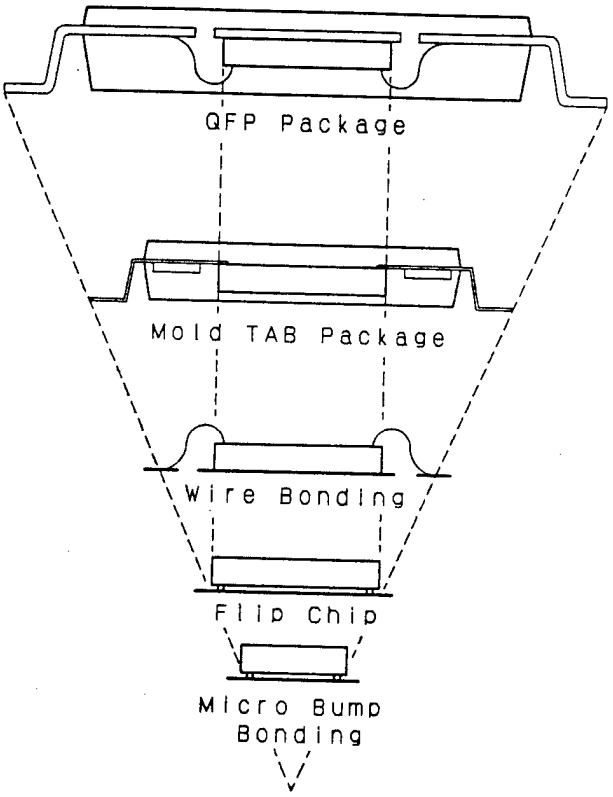


Fig.4 Various Types of Devices

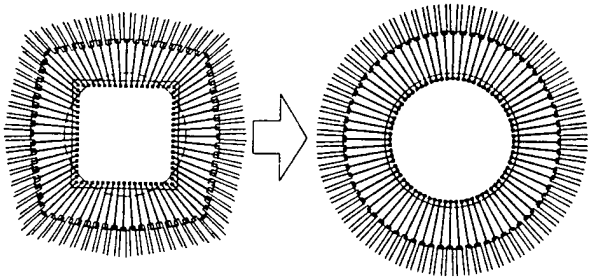


Fig.5 Model of Inner Lead Wiring

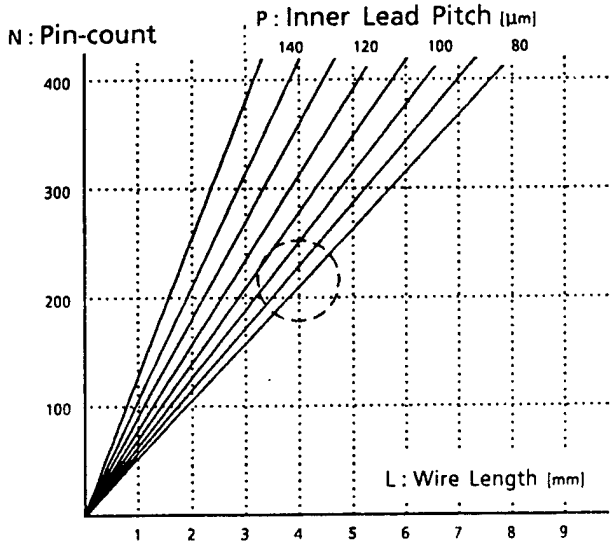


Fig.6 Pin-count vs. Wire Length
with a Parameter of Inner Lead Pitch

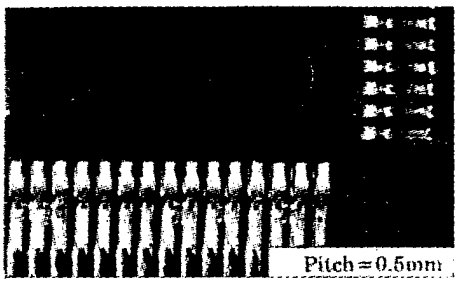


Fig.7-1 Solder Bridging

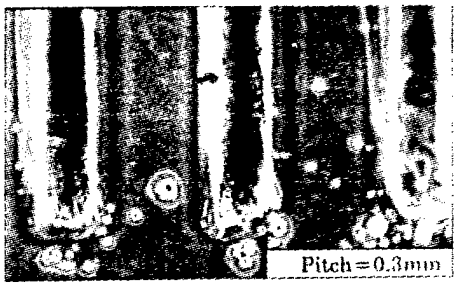


Fig.7-2 Solder Balls

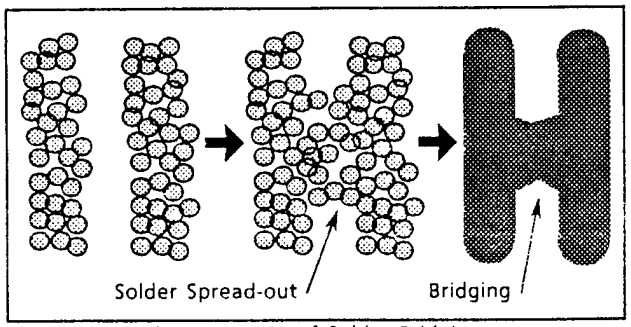


Fig.8 Process of Solder Bridging

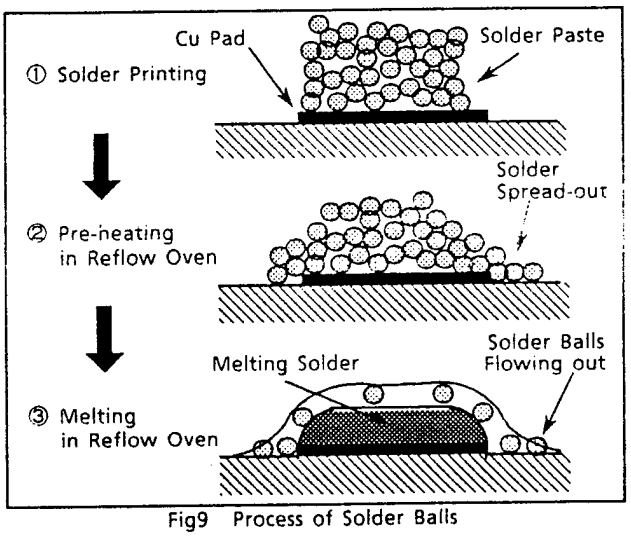


Fig9 Process of Solder Balls

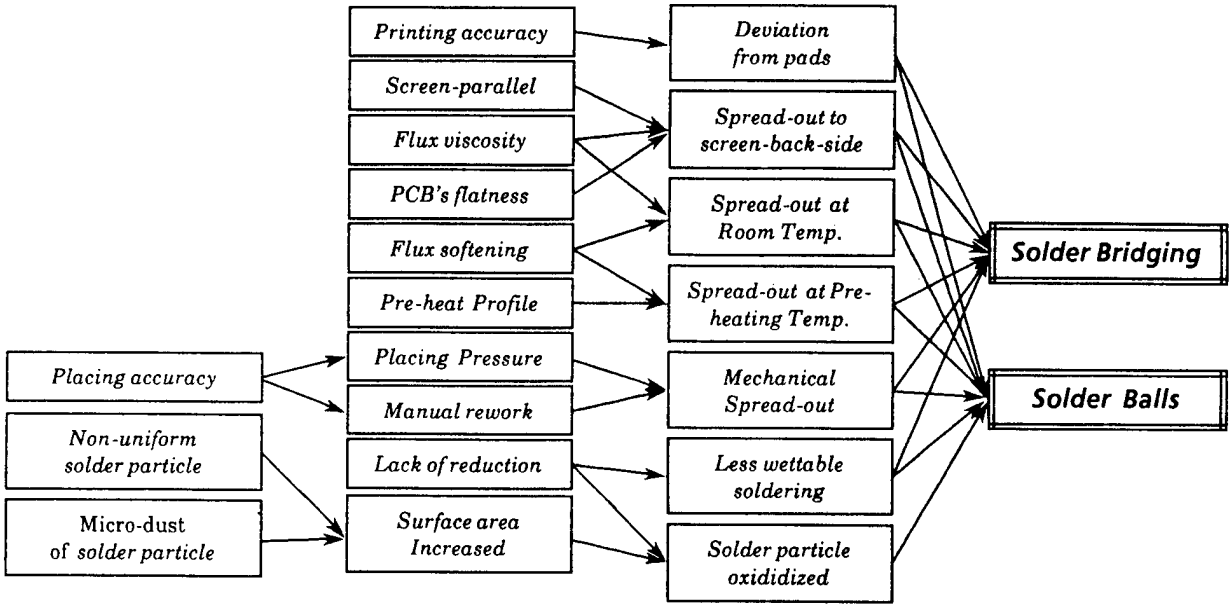


Fig.10 Cause-and-effect of Solder Bridging and Solder Balls

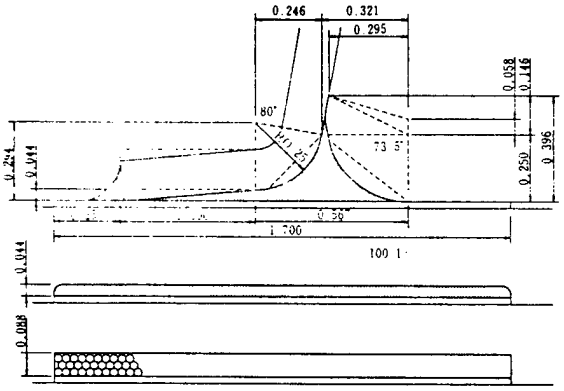


Fig.11 Solder Fillets vs. Solder Paste Volume

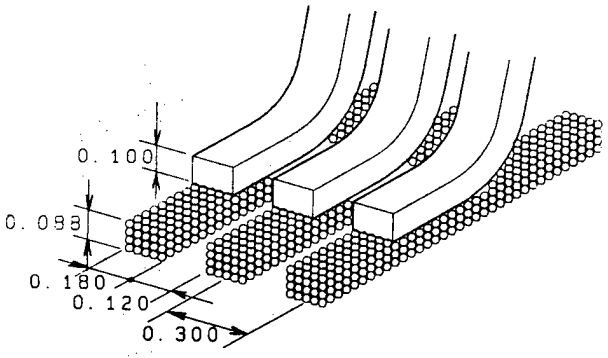


Fig.12 Solder Paste and Fine-pitch-leads

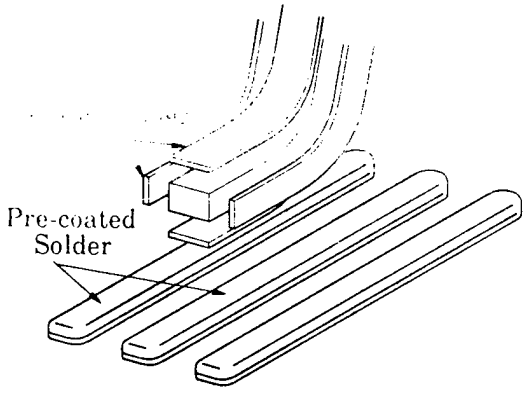


Fig.13 Pre-coats and Fine-pitch-leads

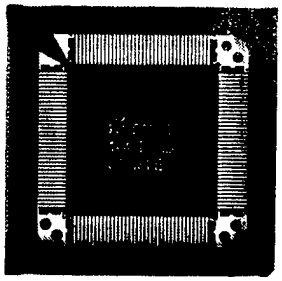


Fig.14 *TapePak* Package

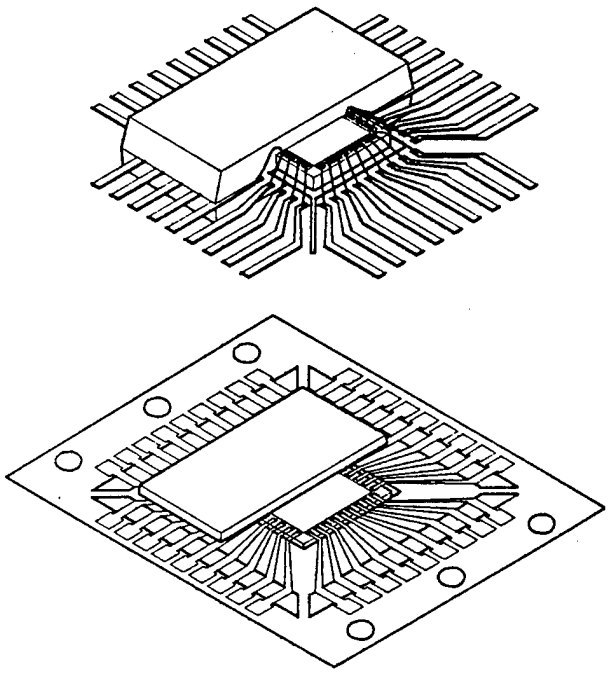


Fig.15 Flat-lead QFP and Molded TAB

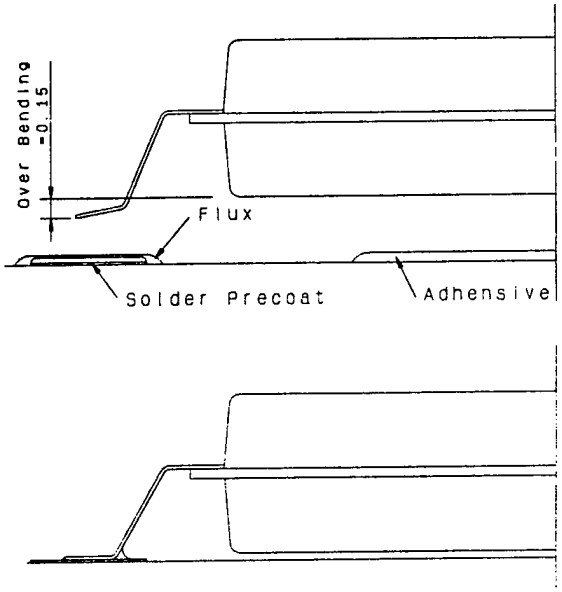


Fig.16 Counter Technology for Thin Lead Co-planarity

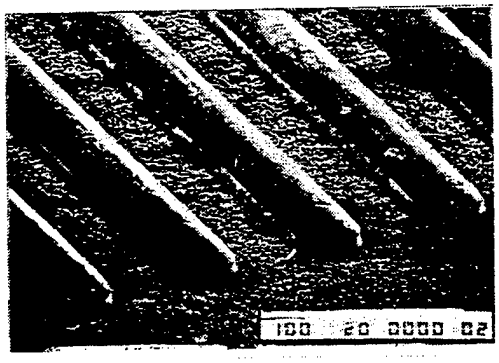


Fig.17 New Solder Pre-coats

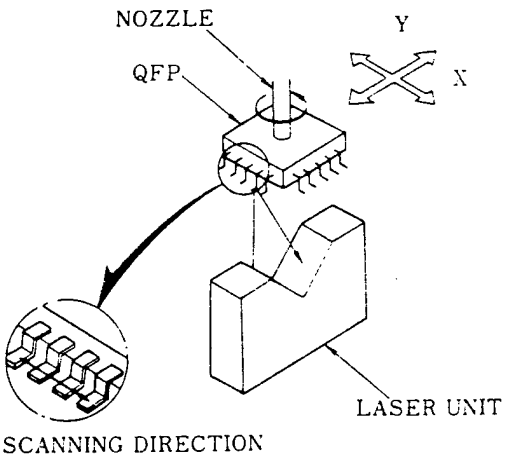


Fig.18 Laser Detection of All Leads

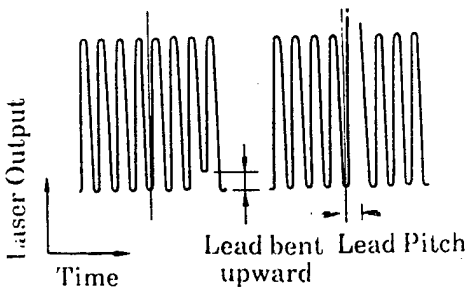


Fig.19 Laser Signal Output

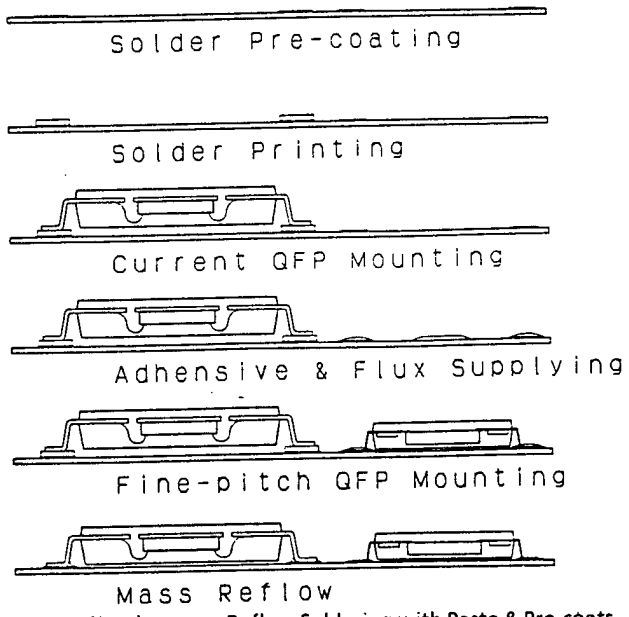


Fig.20 Simultaneous Reflow Soldering with Paste & Pre-coats

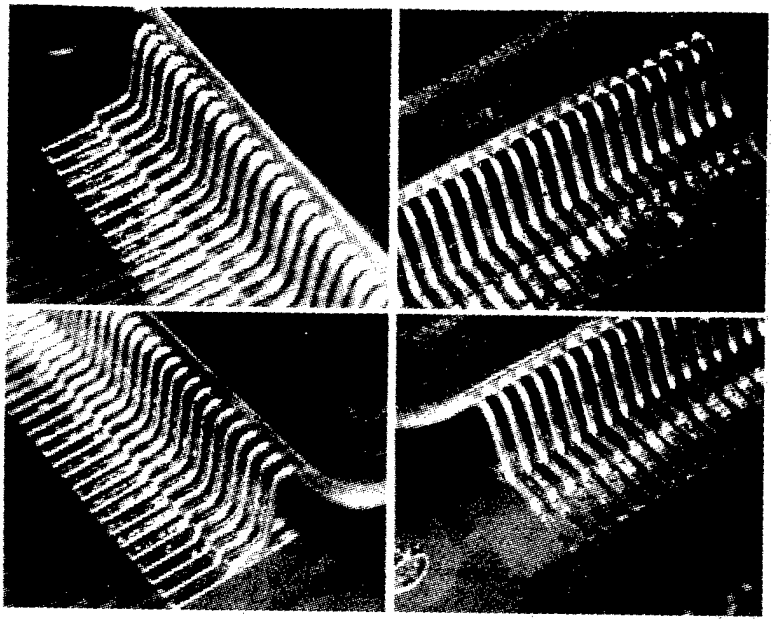


Fig.21 Fine-pitch QFP after Reflow Soldering (P = 0.3mm)

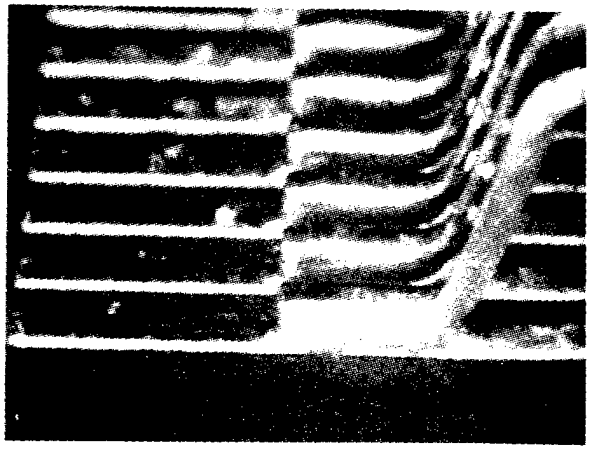


Fig.22 Side-view of Solder Fillets (P = 0.3mm)

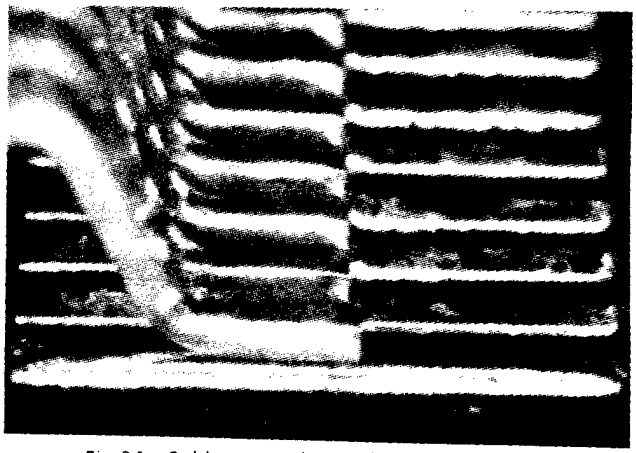


Fig.24 Solder-open due to the Lead bent upward

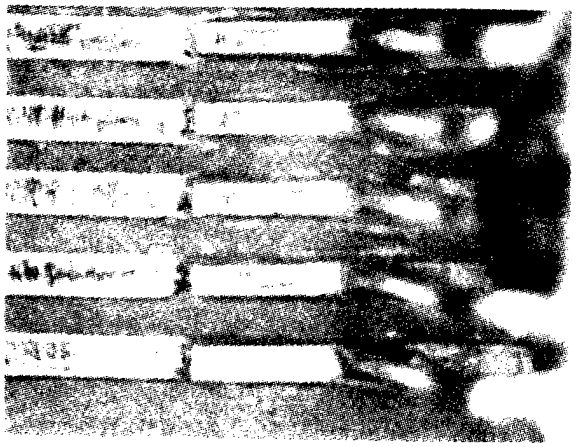
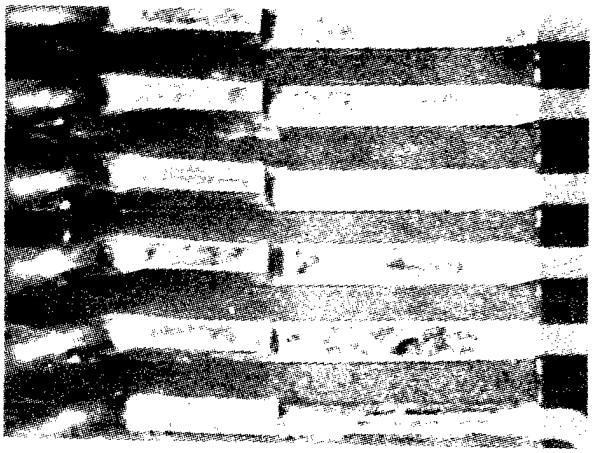


Fig 23 Top-view of Solder Fillets (P = 0.3mm)



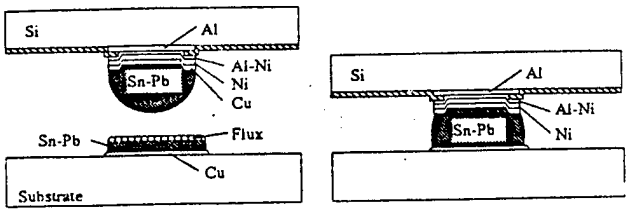


Fig.25 Flip-chip Solder Connection (Solder Bump)

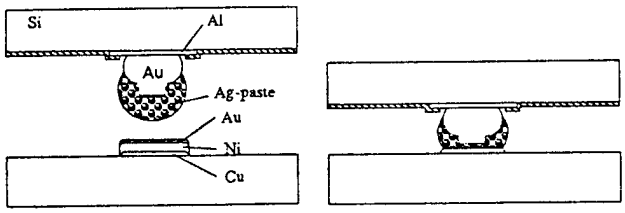


Fig.26 Flip-chip Adhensive Connection (Gold Bump)

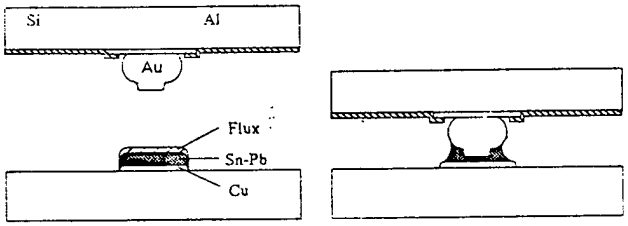


Fig.27 Flip-chip Solder Connection (Gold Bump)

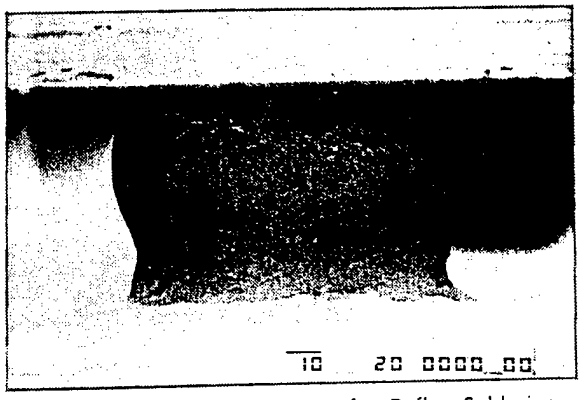


Fig.28 Gold-bump Connection after Reflow Soldering

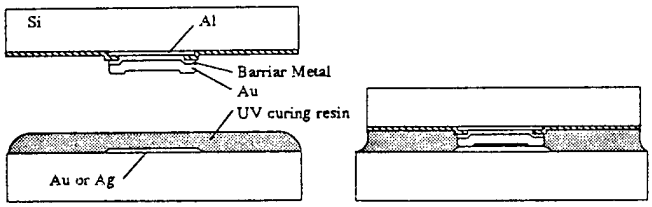


Fig.29 Micro Bump Connection

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1) *Nikkei Electronics (no.495)* , p.130 , March 19 , 1990

2) A . Wakigawa *HYBRIDS Vol.6 No.3* (SHM) ,p.20~25 ,March , 1990

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