

Quarterly Technical Report

Solid State Research

1998:1

Lincoln Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LEXINGTON, MASSACHUSETTS



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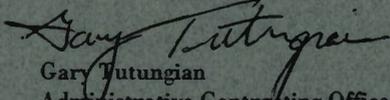
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LINCOLN LABORATORY

SOLID STATE RESEARCH

QUARTERLY TECHNICAL REPORT

1 NOVEMBER 1997 – 31 JANUARY 1998

ISSUED 19 JUNE 1998

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ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 November 1997 through 31 January 1998. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, High Speed Electronics, Microelectronics, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, BMDO, DARPA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

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INTRODUCTION

1. QUANTUM ELECTRONICS

A real-time, point bioaerosol sensor for early warning of threat bioaerosols has been developed, which is based on laser-induced fluorescence detection of aerosol particles and incorporates two spectral channels for discrimination of threat from background aerosols. Field test results indicate that the detector is sensitive to bioaerosols, and under the field test conditions could discriminate bacterial and natural aerosols.

2. ELECTRO-OPTICAL MATERIALS AND DEVICES

GaInAsSb epitaxial layers have been grown on (100) GaSb substrates with a 6° toward (111)B mis-orientation. The layers exhibit a smoother surface morphology and narrower photoluminescence full width at half-maximum compared to layers grown on (100) 2° toward (110) substrates.

3. SUBMICROMETER TECHNOLOGY

Fused silica and calcium fluoride materials have been evaluated in terms of absorption and optical damage for application to 193- and 157-nm optical lithography systems. Accelerated life-cycle testing techniques have been used to assess the longevity of these materials in a production environment.

Wavelength scaling and resolution enhancement techniques have been evaluated for application to advanced photolithography systems. Patterning of 110-nm lines using a 193-nm exposure wavelength and 80-nm lines using a 157-nm exposure wavelength has been demonstrated.

4. HIGH SPEED ELECTRONICS

A novel technique has been developed for the fabrication of a pseudomorphic high-electron-mobility transistor (pHEMT) with protons implanted through the InGaAs channel, converting conductive layers underneath to a high-resistivity buffer. This new method can be used to integrate quantum devices with a transistor, and maintains a highly planar surface.

5. MICROELECTRONICS

The charge-coupled device (CCD) flight array has been assembled for the Advanced X-ray Astronomical Facility (AXAF), which is planned for launch in late 1998 and will be used to observe x rays between 0.25 and 10 keV. The CCDs on this unit have very low noise and background current and have been optimized for this energy range, thereby contributing to the capabilities of AXAF to provide unparalleled energy and angular resolution for an x-ray observatory.

6. ANALOG DEVICE TECHNOLOGY

A charge-domain matched filter with 128 ternary-weighted (+1, -1, and 0) programmable taps has been fabricated in an external foundry using a 1.2- μm CMOS/CCD process. The device has been configured using a preponderance of charge-domain elements to produce a compact low-static-power design for applications requiring circuitry with minimal size, power, and weight.

7. ADVANCED SILICON TECHNOLOGY

The integrated circuit fabrication equipment in the Microelectronics Laboratory has been applied to build multichip module (MCM) substrates, and the first lot of substrates has been completed and is being evaluated. The MCMs, which are far more precise than those available commercially, are needed for DoD applications at frequencies of several gigahertz.

REPORTS ON SOLID STATE RESEARCH

1 NOVEMBER 1997 THROUGH 31 JANUARY 1998

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R. R. Kunz
S. T. Palmacci
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| Photolithography at 0.10 and 0.13 μm
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S. P. Doran
M. Rothschild | <i>J. Vac. Sci. Technol. B</i>
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M. B. Stern
P. W. Wyatt | <i>Opt. Lett.</i> 23 , 141 (1998) |

Theory and Experimental Results of a New Diamond Surface-Emission Cathode	M. W. Geis N. N. Efremow, Jr. K. E. Krohn J. C. Twichell T. M. Lyszczarz R. Kalish J. A. Greer M. D. Tabat	<i>Linc. Lab. J.</i> 10 , 3 (1997)
Zeeman Spectroscopy of Shallow Donors in GaN	W. J. Moore* J. A. Freitas, Jr.* R. J. Molnar	<i>Phys. Rev. B</i> 56 , 12,073 (1997)
Photolithography at 193 nm	M. Rothschild M. W. Horn C. L. Keast R. R. Kunz V. Liberman S. C. Palmateer S. P. Doran A. R. Forte R. B. Goodman J. H. C. Sedlacek R. S. Uttaro D. Corliss A. Grenville	<i>Linc. Lab. J.</i> 10 , 19 (1997)
Nanochannel Fabrication for Chemical Sensors	M. B. Stern M. W. Geis J. E. Curtin	<i>J. Vac. Sci. Technol. B</i> 15 , 2887 (1997)

ACCEPTED FOR PUBLICATION

Thermal Coefficients of the Optical Path Length and Refractive Index in YAG	T. Y. Fan J. L. Daneu	<i>Appl. Opt.</i>
-----------------------------------------------------------------------------	--------------------------	-------------------

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Bromine Ion-Beam-Assisted Etching
of InP and GaAs

W. D. Goodhue
D. E. Mull
J. M. Rossler
Y. Royter
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J. Vac. Sci. Technol. B

High-Power, High Efficiency Quasi-CW
Sb-Based Mid-IR Lasers Using 1.9- μm
Laser Diode Pumping

H. Q. Le
G. W. Turner
J. R. Ochoa

Photon. Technol. Lett.

OMPVE Growth of GaInAsSb in the
2- to 2.4- μm Range

C. A. Wang

J. Cryst. Growth

PRESENTATIONS[†]

Silicon-Containing Methacrylate
Based Bilayer Resist for 193-nm
Lithography

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R. R. Kunz

Olin Microelectronic Materials
Interface 1997,
San Diego, California,
9-11 November 1997

Semiconductor Diode Optical
Amplifiers and Lasers with
Tapered Gain Regions

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Lincoln Laboratory
Technical Seminar Series,
University of Pittsburgh,
Pittsburgh, Pennsylvania,
10 November 1997

* Author not at Lincoln Laboratory.

[†] Titles of presentations are listed for information only. No copies are available for distribution.

High Power Mid-Infrared Semiconductor Lasers	H. K. Choi G. W. Turner H. Q. Le	} IEEE Lasers and Electro-Optics Society Annual Meeting, San Francisco, California, 10-13 November 1997
Ultralow Threshold (50 A/cm^2) Strained Single-Quantum-Well GaInAsSb/GaAsSb Lasers Emitting at $2.05 \mu\text{m}$	G. W. Turner H. K. Choi M. J. Manfra	
Dual-Layer, Optimal Antireflection Coatings for Diode Lasers	C. C. Cook	SPIE Annual Paper Contest, Boston, Massachusetts, 20 November 1997
Optical Lithography at Feature Sizes of $0.25 \mu\text{m}$ and Below	M. W. Horn	Lincoln Laboratory Technical Seminar Series, Pennsylvania State University, University Park, Pennsylvania, 1 December 1997
Internal Cylindrical Magnetron Sputtering of YBCO Thin Films for Microwave Device Applications	A. C. Anderson R. L. Slattery	} Fall Meeting of the Materials Research Society, Boston, Massachusetts, 1-5 December 1997
Substrate Misorientation Effects on Epitaxial GaInAsSb	C. A. Wang	
Frequency-Agile Microwave Applications of Oxide Materials	D. E. Oates	International Workshop on Oxide Electronics, College Park, Maryland, 8-9 December 1997
Magnetization and Hysteresis Modeled from the Approach to Saturation	G. F. Dionne	Intermag '98, San Francisco, California, 6-9 January 1998

Multifunction Integrated Optical
Chip

G. E. Betts
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Microwave Links Using Externally
Modulated Semiconductor Laser
Sources

G. E. Betts
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K. G. Ray
L. M. Johnson

8th Annual DARPA
Symposium on Photonics
Systems for Antenna
Applications,
Monterey, California,
12-15 January 1998

Diamond Emitters Fabrication and
Theory

M. W. Geis

Lincoln Laboratory
Technical Seminar Series,
Worcester Polytechnic Institute,
Worcester, Massachusetts,
19 January 1998

Low Threshold, High-Power,
High-Brightness GaInAsSb/
AlGaAsSb Quantum-Well Lasers
Emitting at 2.05 μm

H. K. Choi
G. W. Turner
J. N. Walpole
M. J. Manfra
M. K. Connors
L. J. Missaggia

Photonics West '98
San Jose, California,
24-30 January 1998

High Power 1.5- μm Tapered-Gain-
Region Lasers

J. P. Donnelly
J. N. Walpole
S. H. Groves
R. J. Bailey
L. J. Missaggia
A. Napoleone

Optoelectronics '98,
San Jose, California,
24-30 January 1998

Photolithography at Wavelengths
Below 200 nm

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SPIE Conference on Laser
Applications in Micro-
electronic and Optoelectronic
Manufacturing III,
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24-30 January 1998

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1. QUANTUM ELECTRONICS

1.1 BIOAEROSOL FLUORESCENCE SENSOR

The early detection of pathogenic bioaerosols is of paramount importance for mitigating the adverse health effects of such aerosols. The development of early detection sensors is a high priority for the defense of military personnel against potential future biological attack. Previous research has shown that one of the most promising techniques for obtaining real-time warning of the presence of bioaerosols is the detection of laser-induced fluorescence from the aerosol particles [1]–[5].

A prototype point bioaerosol fluorescence sensor has been developed for measurement of atmospheric bioparticle concentrations. Figure 1-1 illustrates the bioparticle sensor concept. Air is drawn through a sample flow channel by an exhaust fan. Intersecting the air flow at right angles is an ultraviolet laser beam which is reflected from mirrors on either side of the channel so that the laser beam passes through the sampled air multiple times. Adjacent to the path of the laser beam are two photomultiplier tubes. When a particle in the air stream is illuminated by the laser beam, some of the induced fluorescence is incident on the photodetectors. Different spectral filters in front of each photocathode pass different spectral portions of the fluorescence radiation to the photocathodes. The signals from the photodetectors are measured by temporally gated charge integrators and are recorded and analyzed in real time by a

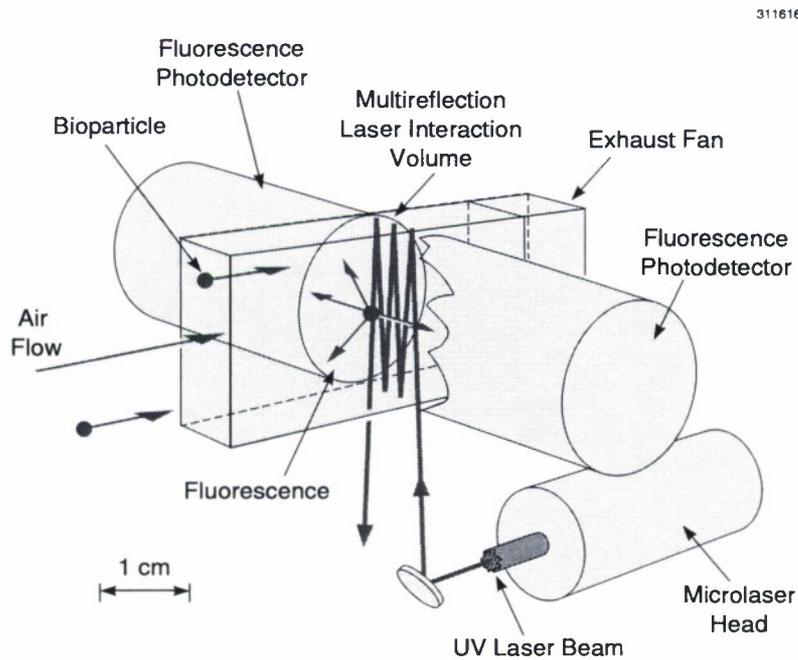


Figure 1-1. Schematic of bioaerosol fluorescence sensor.

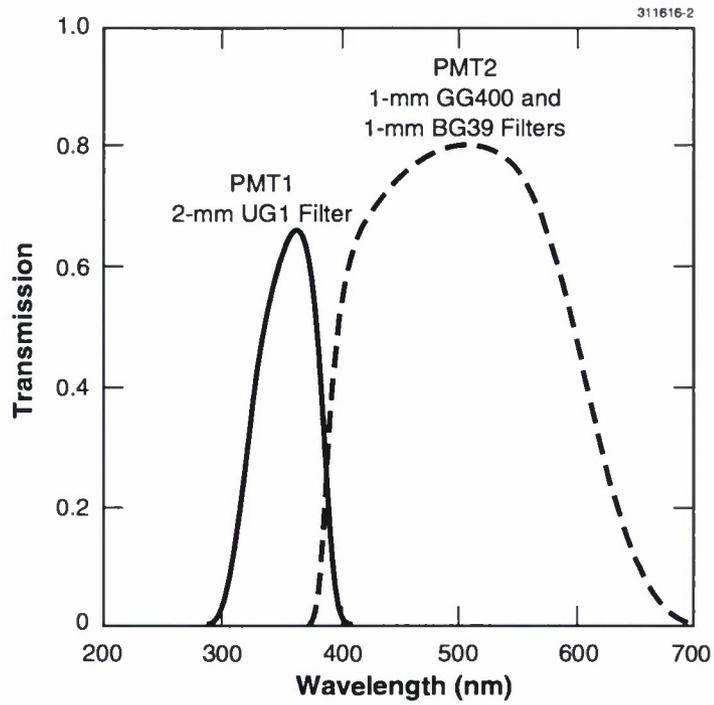


Figure 1-2. Spectral transmission of filters in front of photomultiplier tubes PMT1 and PMT2.

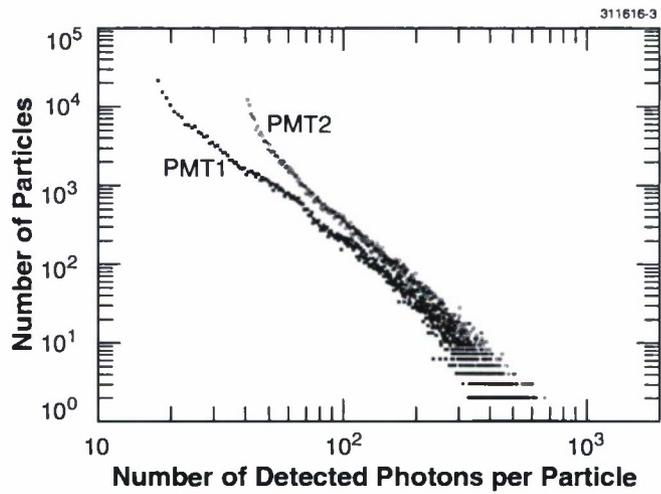


Figure 1-3. Pulse height distributions in photomultipliers PMT1 and PMT2 for aerosol of *Bacillus subtilus* spores.

portable computer system. The ratio of the two photomultiplier signals is used to discriminate background aerosols from potential threat bioaerosols.

The ultraviolet laser beam is produced by a diode-pumped, passively Q -switched Nd:YAG microlaser which is frequency quadrupled to 266 nm by KTP and BBO crystals [6]. The 266-nm microlaser pulses have an energy of 0.3 μJ , a duration of 400 ps, and a repetition rate of about 8 kHz. The laser beam has a diameter of about 0.5 mm in the sample chamber. The photomultipliers (Hamamatsu R1924) each have a 21-mm-diam bialkali photocathode ($\sim 20\%$ quantum efficiency), which are separated from one another by 20 mm. This geometry results in a fluorescence collection efficiency for both photocathodes, averaged over a 20-mm length of the laser beam, of 26% (1.6 steradians per photocathode). One photomultiplier (PMT1) has a 2-mm-thick UG1 Schott glass filter (300–400 nm) in front of the photocathode while the other photomultiplier (PMT2) has both 1-mm-thick BG39 and 1-mm-thick CG410 Schott glass filters (400–600 nm) in front of the photocathode. The spectral transmission of these filters is shown in Figure 1-2.

The photomultiplier signal is measured with charge-to-digital converters which are temporally gated on for a 50-ns window centered on the laser pulse. Figure 1-3 shows typical PMT1 and PMT2 pulse height distributions for a *Bacillus subtilis* aerosol sampled by the sensor. The pulse height distributions are a convolution of the variation of the fluorescence cross section from particle to particle and the variation of the position (and hence excitation intensity) of the particles in the laser beam. The ratio of coincident signals in PMT1 and PMT2 for various bioaerosols is shown in Figure 1-4. Threat aerosols are discriminated from background aerosols by coincident photodetection in both photomultipliers where the ratio of the signal in one photomultiplier to the signal in the other photomultiplier is within a predetermined range.

The prototype sensor has an optical head, with a volume of 28 L. A blower draws air through the sensor at a rate of 2.4 L/s, of which a few percent is sampled by the laser beam. The signals are acquired by electronics in a CAMAC crate and are processed and displayed in real time by a portable personal computer. For the field tests the optical head was mounted on an outside tripod and the acquisition electronics were housed in a small utility van with electrical cables connecting the sensor and electronics.

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A. Sanchez-Rubio	C. A. Primmerman

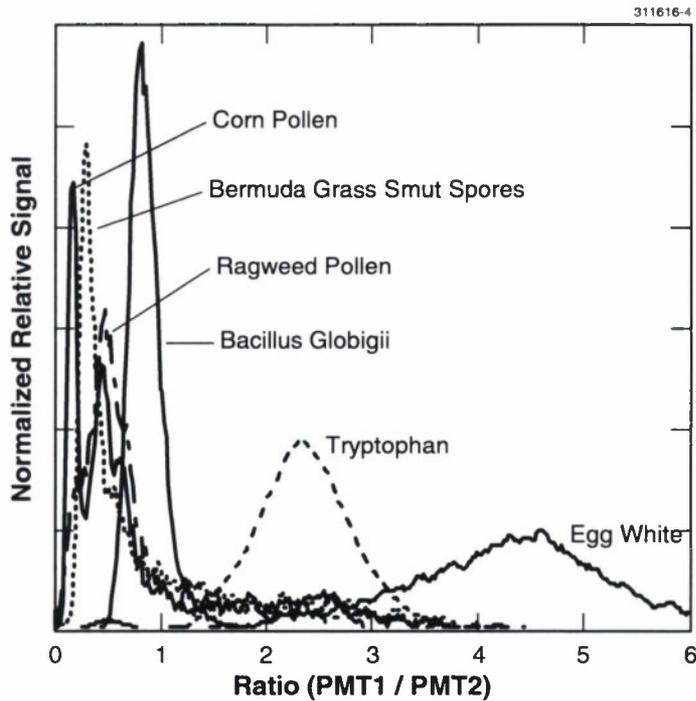


Figure 1-4. Distribution of sensor signal as a function of the ratio of coincident signals in photomultipliers PMT1 and PMT2 for various bioaerosols.

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2. ELECTRO-OPTICAL MATERIALS AND DEVICES

2.1 EFFECT OF SUBSTRATE MISORIENTATION ON EPITAXIAL GaInAsSb

GaInAsSb alloys lattice matched to GaSb substrates are of particular interest for thermophotovoltaics [1]. Recently, we reported external quantum efficiency as high as 55% at 2 μm for GaInAsSb devices grown by organometallic vapor phase epitaxy (OMVPE). The use of vicinal substrates for the growth of III-V semiconductors can play an important role in the resulting material quality. For example, the surface morphology of GaAs layers was reported to be smoother for OMVPE growth on (100) substrates with a 2° misorientation toward (110) [2], and higher optical quality was observed for GaAs/AlGaAs quantum wells grown on vicinal substrates by molecular beam epitaxy (MBE) [3]. Furthermore, the device performance of GaAs/AlGaAs quantum-well lasers was significantly improved on tilted substrates [4]. Here, we report the growth and optical properties of GaInAsSb alloys lattice matched to GaSb substrates with misorientations of 2 and 6° off (100) toward (110), (111)A, and (111)B. The best surface morphology and highest optical quality are obtained for substrates with a 6° toward (111)B misorientation.

$\text{Ga}_{1-x}\text{In}_x\text{As}_y\text{Sb}_{1-y}$ epilayers were grown in a vertical rotating-disk reactor with H_2 carrier gas at a flow rate of 10 slpm and reactor pressure of 150 Torr as described previously [5]. GaInAsSb was grown on (100) Te-doped GaSb substrates with misorientation angles of either 2 or 6° toward (110), (111)A, or (111)B. Solution trimethylindium, triethylgallium, tertiarybutylarsine, and trimethylantimony were used as organometallic sources. The growth rate was typically 2.5 $\mu\text{m}/\text{h}$. The V/III ratio ranged from 1.1 to 1.3 and the growth temperature ranged from 525 to 575°C. The surface morphology was examined using Nomarski contrast microscopy. Double-crystal x-ray diffraction was used to measure the degree of lattice mismatch $\Delta a/a$ to GaSb substrates. Photoluminescence (PL) was measured at 4 and 300 K using a PbS detector. The In and As content of epilayers was determined from the lattice mismatch, the peak emission in 300-K PL spectra, and the energy gap dependence on composition based on the binary bandgaps [1].

The surface morphology of $\text{Ga}_{1-x}\text{In}_x\text{As}_y\text{Sb}_{1-y}$ layers grown at 550°C on vicinal GaSb substrates is shown in Figure 2-1. These are Nomarski interference micrographs of $\text{Ga}_{0.82}\text{In}_{0.18}\text{As}_{0.15}\text{Sb}_{0.85}$ layers grown at 550°C and V/III = 1.25 on (100) GaSb substrates with a 2 or 6° misorientation toward (110), (111)A, and (111)B, respectively. The layers grown on substrates with a 2° misorientation exhibit considerable texture. A smoother surface morphology is observed for layers grown on substrates with a 6° misorientation, and the smoothest surface is observed for 6° toward (111)B misorientation. Since the most common substrate misorientation for OMVPE growth is (100) 2° toward (110), further comparisons are made for GaInAsSb layers grown on this misorientation and (100) 6° toward (111)B.

Figure 2-2 shows PL spectra measured at 4 K of GaInAsSb layers grown at 550°C on (100) GaSb substrates with either a 2° toward (110) or 6° toward (111)B misorientation. The $\Delta a/a$ for these layers was less than 1.7×10^{-3} . The full width at half-maximum (FWHM) is 15.4 meV for layer A with a 2° toward (110) misorientation compared to a FWHM of 7.5 meV for layer B with the 6° toward (111)B misorientation. In addition, the peak emission is slightly longer at 2045 nm for layer A compared to 1995 nm for

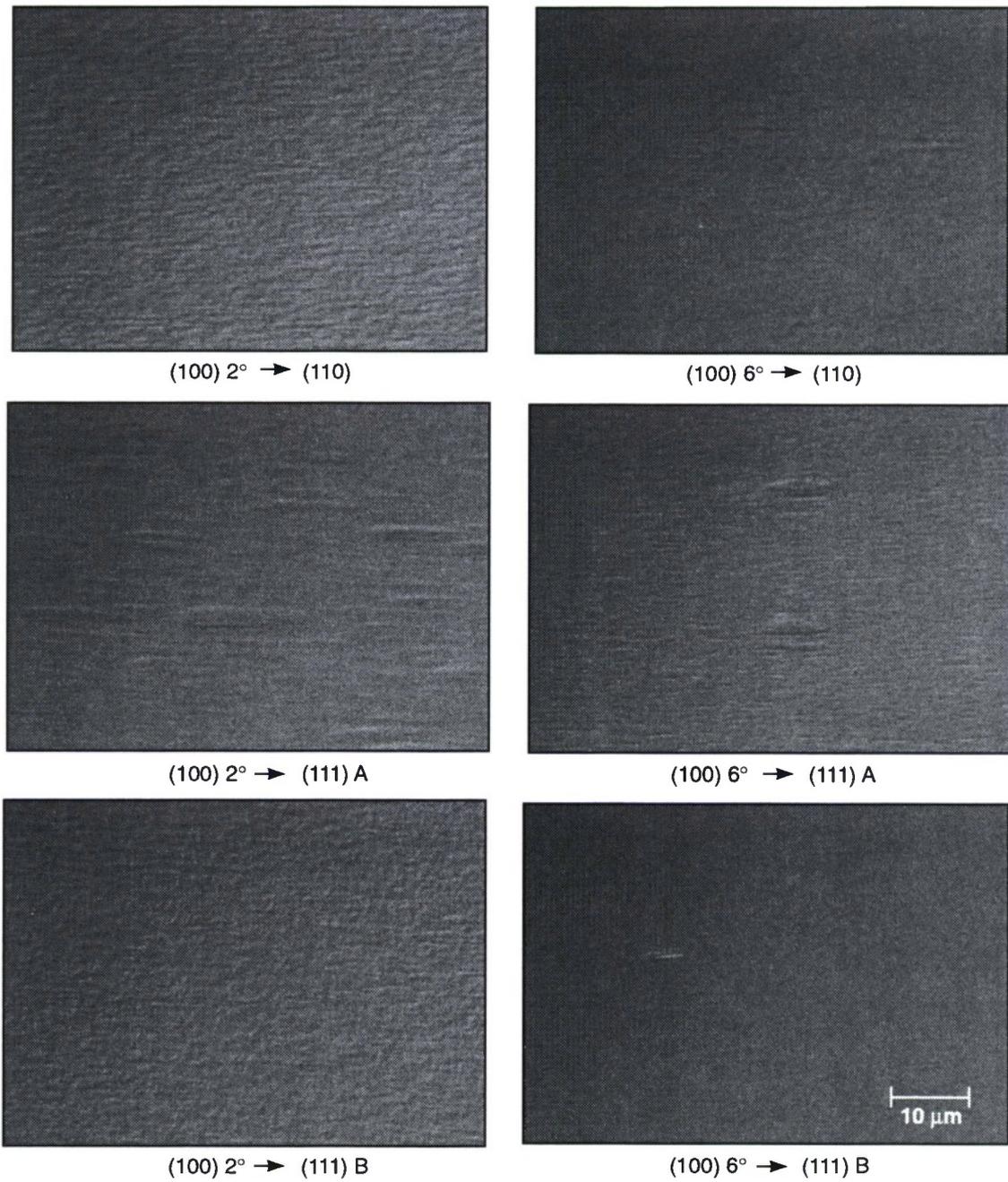


Figure 2-1. Surface morphology of $\text{Ga}_{0.82}\text{In}_{0.18}\text{As}_{0.15}\text{Sb}_{0.85}$ epilayers grown on GaSb substrates at 550°C and various substrate misorientations.

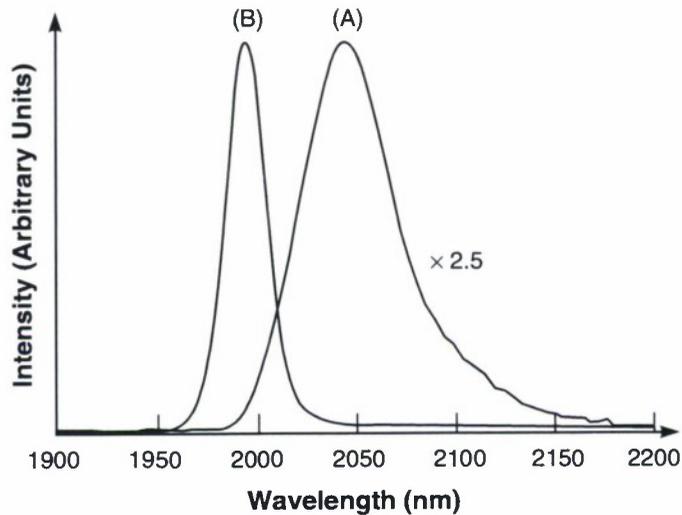


Figure 2-2. Photoluminescence spectra measured at 4 K of GaInAsSb grown on (100) GaSb with (A) 2° toward (110) and (B) 6° toward (111)B misorientations.

layer B. The PL spectra measured at room temperature also shows a longer peak emission for layer A at 2236 nm compared to 2217 nm for layer B. This difference corresponds to a small decrease in In content from about 0.142 to 0.139.

Table 2-1 lists PL data for lattice-matched ($\Delta a/a < 2 \times 10^{-3}$) GaInAsSb layers of various alloy composition grown at 525 and 550°C, and indicates similar trends as discussed above. The FWHM values are lower and the PL peak position is at shorter wavelength for the 6° toward (111)B misorientation compared to the 2° toward (110) misorientation. A dependence of In incorporation on substrate misorientation has also been reported for InGaAs [6]. However, in the present study, the misorientation angles and directions are different, so a possible mechanism for the observed In dependence cannot be suggested. In addition, the data in Table 2-1 suggest that FWHM values are dependent on growth temperature. Narrower FWHM values are obtained for GaInAsSb grown on (100) 2° toward (110) substrates when grown at 525°C compared to 550°C. For most of the layers, the difference in PL peak energy at 4 and 300 K is in the range between 0.05 and 0.07 meV, which is in line with the energy difference of the near-bandedge transitions for GaSb [7] and InAs [8]. The PL peak position is at a longer wavelength at 4 K compared to 300 K for sample 392a. Since the FWHM value is large, it is more likely that the peak is related to an impurity transition.

Figure 2-3 summarizes our best FWHM data for GaInAsSb epilayers. These samples were grown at 550°C on (100) 6° toward (111)B substrates or at 525°C on either (100) 2° toward (110) or 6° toward (111)B substrates. Also shown for comparison are data for layers grown by OMVPE on (100) substrates

TABLE 2-1
Photoluminescence of GaInAsSb

Sample	4-K PL Peak (nm)	300-K PL Peak (nm)	4-K FWHM (meV)	Growth Temperature (°C)	Substrate Misorientation
404a	2082	2296	11.2	525	2°(110)
404b	2042	2276	9.5	525	6°(111)B
413	2030	2263	8.1	525	2°(110)
416b	2047	2267	7.1	525	6°(111)B
392a	2432	2396	45	550	2°(110)
391b	2138	2355	16.4	550	6°(111)B
415a	2045	2236	15.4	550	2°(110)
415b	1995	2217	7.5	550	6°(111)B
396a	1875	2100	15.4	550	2°(110)
396b	1865	2080	9.6	550	6°(111)B

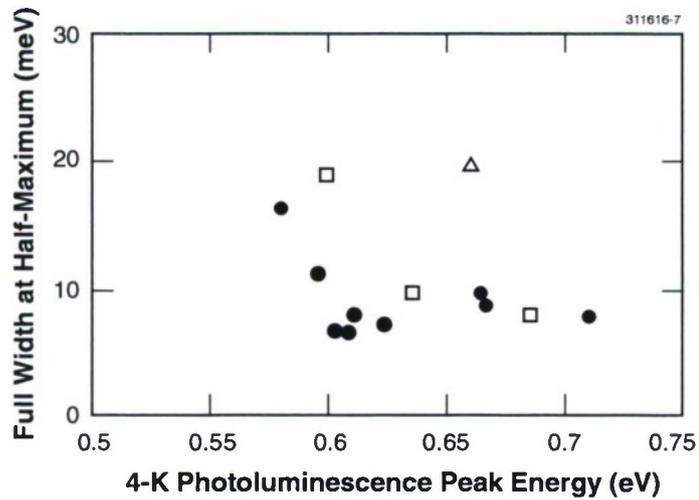


Figure 2-3. Photoluminescence full width at half-maximum measured at 4 K of GaInAsSb layers grown on GaSb substrates. Solid circles this work; open squares from [9]; open triangle from [10].

[9],[10]. The FWHM values decrease with increasing PL peak energy. Our FWHM values are significantly smaller than those reported previously, especially for samples at lower PL peak energy. The smallest FWHM value measured is 7.1 meV at 0.606 eV. Our FWHM values are comparable to those reported for layers grown by MBE [1] and liquid-phase epitaxy [11].

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3. SUBMICROMETER TECHNOLOGY

3.1 OPTICAL MATERIALS FOR 193- AND 157-nm LITHOGRAPHY

The availability of suitable optical materials is one of the key challenges facing 193- and 157-nm lithography. Such materials must not only be transparent, but must also display good index homogeneity, low stress birefringence, and the ability to withstand prolonged irradiation (the expected lifetime of a lithographic tool is ~10 years) without undergoing changes. In fact, high-purity synthetic fused silica and crystalline calcium fluoride are probably the only two practical materials for 193-nm lithography. Fused silica is too absorptive at 157 nm, and calcium fluoride seems to be the only practical choice of transparent optical material. Other materials, although transparent, are birefringent (magnesium fluoride), hygroscopic (lithium fluoride), or have other deficiencies.

Extensive transmission measurements at Lincoln Laboratory have shown that there is a broad range of absorption coefficients across materials, across grades within each material, and even from batch to batch. Lens heating during exposure, caused by absorbed 193- or 157-nm radiation, results in a change in index of refraction which may seriously impact lens performance. At 193-nm wavelength, fused silica has absorption coefficients of 0.001 to 0.004 cm^{-1} , whereas calcium fluoride varies from 0.002 to less than 0.0005 cm^{-1} . The thermal coefficient of the index of refraction of fused silica at 193 nm is $\sim 22 \times 10^{-6} \text{ K}^{-1}$. We have also measured the absorption coefficient of calcium fluoride at 157 nm to be $\sim 0.004 \text{ cm}^{-1}$, as shown in Figure 3-1. This value, while four times higher than that of the best fused silica at 193 nm, is

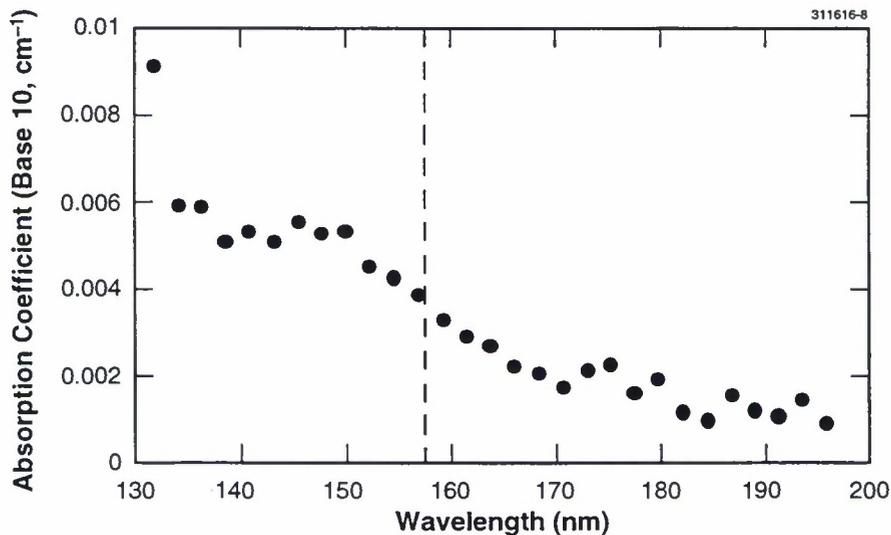


Figure 3-1. Absorption coefficient of calcium fluoride in the range 130–200 nm, as calculated from transmission measurements performed with vacuum uv spectrophotometer on three prism-shaped samples along their 10- and 40-mm axes. At 157 nm the absorption coefficient is $\sim 0.004 \text{ cm}^{-1}$.

mitigated by the effect of two other properties of calcium fluoride: the thermal coefficient of its refractive index at 157 nm is ~ 7 times lower than that of fused silica at 193 nm, and its thermal conductivity (which is inversely proportional to the laser induced temperature rise) is ~ 7 times higher than that of fused silica. Thus, the overall optical effect of 157-nm absorption in calcium fluoride is smaller than that of 193-nm absorption in fused silica.

Upon exposure to 193-nm radiation both fused silica and calcium fluoride tend to develop color centers, and their absorption at 193 nm may grow over time [1]. The magnitude of this effect is again quite variable from grade to grade and occasionally from sample to sample. Long-term durability data are still sparse: the pulse repetition rate of lasers is at present limited to ~ 1 kHz, and accelerated damage testing at high fluences may not be indicative of material performance at the low fluences encountered in lithographic systems. Some of the recent data obtained in an extended study at Lincoln Laboratory are summarized in Figure 3-2. Here, the absorption coefficient of several grades of fused silica is plotted for samples exposed at ~ 1 mJ/cm²/pulse for up to 2 billion pulses. As can be seen, some samples show no change in absorption, while others double their initial absorption coefficient. Since the safety margin on absorption of fused silica is quite low to start with, the added laser-induced absorption must be kept low. Indeed, it appears from these data that, notwithstanding the variations shown in Figure 3-2, certain grades of fused silica can be used in 193-nm lithographic systems. Similar results, although at present based on fewer samples, have been obtained also in calcium fluoride.

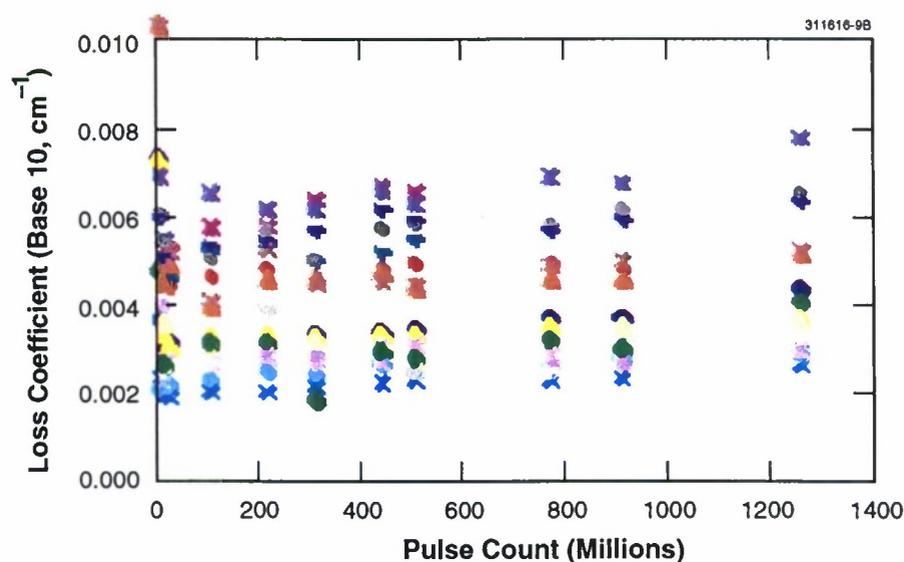


Figure 3-2. The loss coefficient of five grades (18 samples) of fused silica exposed to 193-nm radiation at ~ 1 mJ/cm²/pulse. The absorption coefficient is obtained from these data by subtracting ~ 0.0008 cm⁻¹, which is the estimated coefficient of Rayleigh scattering at this wavelength. This figure illustrates the wide range of absorption coefficients of fused silica, and also the apparent lower limit of its value.

Irradiation of fused silica also causes compaction, i.e., a volumetric reduction accompanied by an increase in index in the exposed area and by stress birefringence in adjacent areas. The scaling laws governing compaction are better understood than those of added absorption [2]. The compaction appears to be proportional to $(N\Phi^2/t)^x$, where N is the pulse count, Φ is the laser fluence, t is the laser pulse duration, and x is an experimentally determined factor ($x \sim 0.5\text{--}0.7$ for all grades of fused silica). A compilation of compaction data obtained at several laboratories under varying experimental conditions indicates that the coefficient of proportionality varies by a factor of 4, as seen in Figure 3-3. This variation may in part be attributed to different measurement methods and in part to real variations among materials. As with absorption, the safety margin is quite small: in order to keep the compaction at sub- 1×10^{-6} levels at practical fluences and pulse counts, the lifetime of the optics will vary from a respectable 12 years to an unacceptable 3 years. It should be noted that no compaction has been detected in crystalline calcium fluoride, probably because compaction is associated with glassy material such as fused silica.

Transmissive mask technology based on calcium fluoride substrates must also be developed at 157 nm. Specifically, various processing steps which are used routinely in the mask industry with fused silica substrates must be requalified. For instance, we have observed that wet etchants used in the patterning of the chromium absorber chemically attack the surface of calcium fluoride. On the other hand, plasma

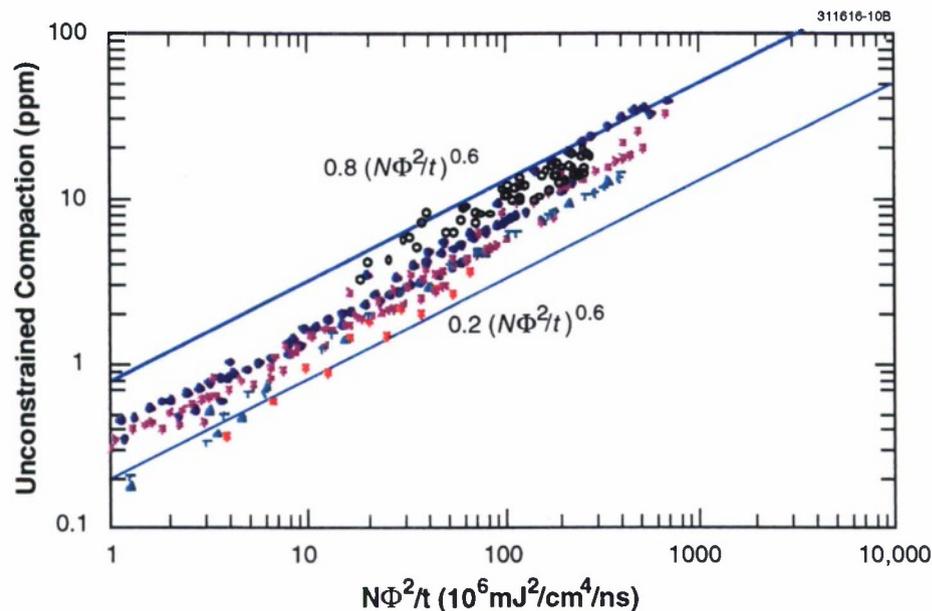


Figure 3-3. Growth of unconstrained compaction in fused silica as a function of the quantity $N\Phi^2/t$, which is proportional to the number of two-photon events at 193 nm. The data are a compilation of measurements of compaction in two grades of fused silica, obtained at several laboratories, including the University of California at Berkeley and MIT Lincoln Laboratory, with different irradiation geometries, fluences, pulse counts, and pulse durations. The compaction was determined in some laboratories by interferometry and in others by measurement of stress-induced birefringence. Most of the data appear to fall between the two solid lines, which differ by a factor of 4.

etching of chromium, with an oxygen-chlorine mix, leaves calcium fluoride unaffected. At Lincoln Laboratory, we have fabricated small masks with calcium fluoride substrates and have used them in the initial imaging experiments.

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3.2 PHOTOLITHOGRAPHY AT WAVELENGTHS BELOW 200 nm

Projection photolithography is widely expected to remain the main high-throughput patterning technology of microelectronic circuits in the next few years. As the critical dimensions of these devices shrink to $0.18 \mu\text{m}$ and below, the lithographic wavelength will decrease from 248 to 193 nm, and possibly to 157 nm.

The smallest feature, LW, that can be printed is determined by the wavelength used, λ , and the numerical aperture of the imaging optics, NA:

$$\text{LW} = k_1 \lambda / \text{NA} \quad , \quad (3.1)$$

where k_1 is a parameter larger than 0.25 (for dense lines). Its exact value is determined by the processing conditions of the wafer, and at present it is larger than ~ 0.5 . The most critical process margin in photolithography is the depth of focus (DOF), which must be larger than any variations in the flatness of the photoresist surface. It is also determined by λ and NA, via the expression

$$\text{DOF} = k_2 \lambda / (\text{NA})^2 \quad , \quad (3.2)$$

where the parameter k_2 may depend on k_1 . At present the DOF in production is at least $0.8 \mu\text{m}$, but it is expected to shrink to $\sim 0.5 \mu\text{m}$ in the future. Expressions (3.1) and (3.2) above indicate that a reduction in wavelength as a means to improved resolution carries with it less of a penalty in DOF reduction than would the alternative, i.e., an increase in numerical aperture. The combination of these short wavelengths and a reduction in k_1 (for instance, using phase-shifting masks) holds the promise that projection photolithography will remain the technology of choice for at least one more decade.

Photoresists developed for 248-nm lithography have demonstrated excellent performance, but they cannot be used effectively at 193 nm because the base polymers are typically too absorptive to be exposed to more than ~ 100 -nm thickness at this wavelength. For 193-nm lithography a new class of photoresists has been developed using polyacrylates [3],[4]. Other photoresist systems have been developed which have alicyclic groups (cyclic configurations with single C-C bonds) and are thus more plasma etch resistant and also semitransparent at 193 nm [4].

An alternative resist approach is the so-called top-surface imaging (TSI) [5] system in which an absorptive polymer is used (polyvinylphenol), which is crosslinked by 193-nm radiation. Following exposure, the wafer is placed in a vapor of organosilicon compound (dimethylsilyldimethylamine), which diffuses into the unexposed areas, and then the wafer is processed in an oxygen-based plasma etch. The latter step etches the crosslinked, unsilylated regions down to the underlying substrate. Careful optimization of the exposure, silylation, and plasma-etching steps is required in TSI, but the outcome has been a high-resolution process with wide latitudes [6].

Photoresist processes still must be developed for 157 nm. Single-layer resists may be more difficult to engineer at 157 nm, because fewer polymers are semitransparent at this wavelength than at 193 nm. On the other hand, our results indicate that the TSI process optimized for 193 is effective at 157 nm as well; the required dose is somewhat higher, but the intrinsic resolution appears to be excellent.

Several optical and computational methods have been under development for several years, to extend the usefulness of photolithography at longer wavelengths (365, 248 nm). Effectively, they can reduce k_1 in Equation (3.1), while increasing the corresponding k_2 in Equation (3.2). These resolution-enhancing techniques (RETs) include off-axis illumination, phase-shifting masks, and optical proximity correction. Lincoln Laboratory has begun investigating their applicability to 193 nm [7]. One example, using TSI and a 0.5-NA 193-nm stepper, is shown in Figure 3-4. The RET used here involves a chromeless phase-shifting mask, which replaces the traditional chrome-on-quartz reticle. The chromeless edge shifter enhances the sharpness of the image of edges on the photomask by relying on destructive interference, and is capable of resolution approaching the fundamental limit of $k_1 = 0.25$. Figure 3-4 demonstrates the power of this method, where we printed 0.11- μm features with a DOF approaching 1 μm .

A simple 157-nm projection system has been built at Lincoln Laboratory [8]. It is based on a 200-Hz, 40-mJ/pulse commercial F_2 laser. The projection optics is a Schwarzschild microscope objective with a numerical aperture of 0.5, and the field size is the ~ 0.1 mm typical for this kind of optics. The resolution achieved to date, by combining TSI and a chromeless phase-shifting calcium fluoride mask, is shown in Figure 3-5; 80-nm lines are obtained, a value close to the theoretical limit of $\lambda/(4NA)$. These results demonstrate the potential of 157-nm lithography. The various infrastructure technologies—lasers, optical materials, resists, projection optics, and photomasks (including the phase-shifting type)—are all extensions of efforts under development at longer wavelengths. A shift to 157 nm could provide an extra latitude in resolution and DOF, thereby enabling an extension of optical projection lithography to the printing of sub-100-nm dimensions.

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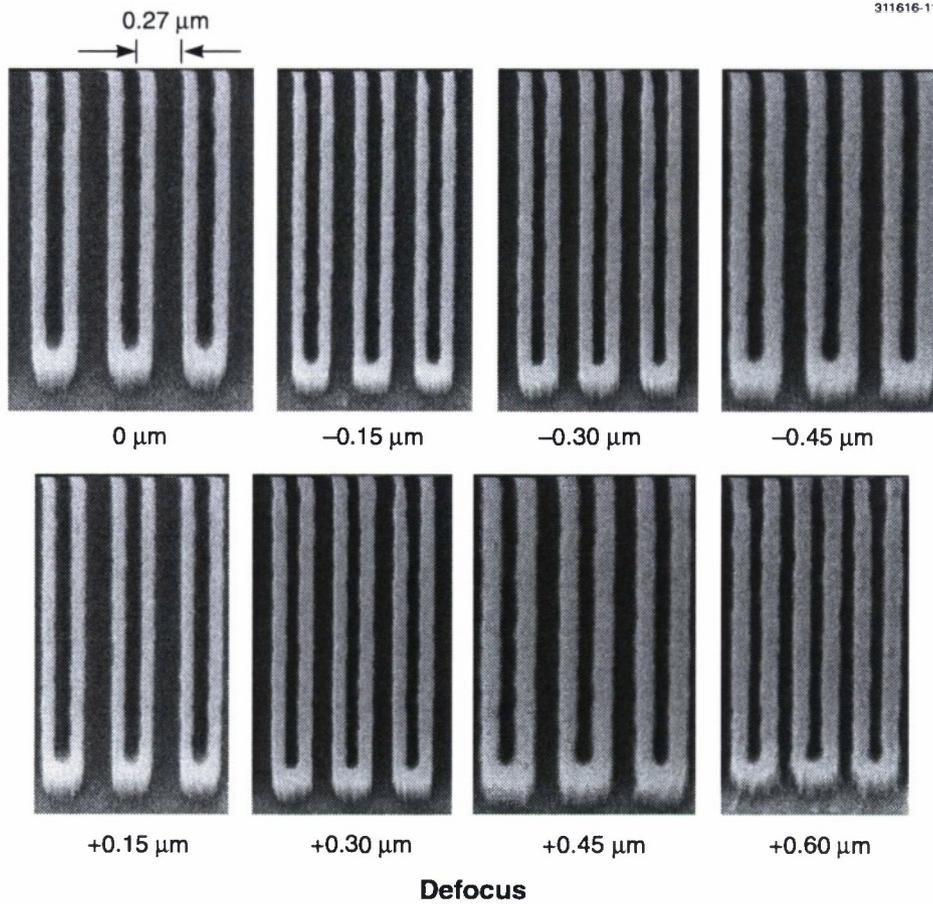


Figure 3-4. Scanning electron micrographs of 110-nm lines on 270-nm pitch produced using chromeless phase-edge photomask in conjunction with 193-nm, 0.5-numerical-aperture (NA), 0.6- σ lens. The images show the change in feature size as the focus is varied.

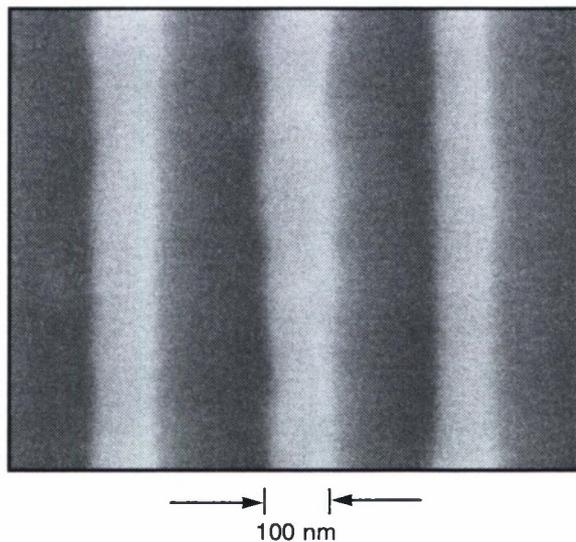


Figure 3-5. Scanning electron micrograph of 80-nm lines on 250-nm pitch printed in projection at 157 nm with 0.5-NA objective. The resist process was top-surface imaging in polyvinylphenol, followed by vapor-phase silylation and oxygen reactive ion etching. The mask was a 36 \times chromeless edge shifter, fabricated in calcium fluoride.

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4. HIGH SPEED ELECTRONICS

4.1 FABRICATION OF PSEUDOMORPHIC HIGH-ELECTRON-MOBILITY TRANSISTORS ON PROTON-ISOLATED GaAs CONDUCTING BUFFER

The performance and functionality of circuits based on devices such as resonant-tunneling diodes (RTDs), diode lasers, and photodetectors can be greatly enhanced by integrating with field-effect transistors (FETs). To solve the difficulties of integrating these devices with vastly different layer structures while maintaining a planar surface for complex circuits, a novel technique utilizing proton implantation is developed. In our new approach, the FET structures are grown on top, and the layers for other types of devices underneath the FET are converted to the high-resistivity buffer by proton implantation.

The layer structure used in this study was grown by molecular beam epitaxy and is shown in Figure 4-1. A pseudomorphic high-electron-mobility transistor (pHEMT) consists of a 130-Å-thick $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ undoped channel, a 30-Å-thick $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$ spacer, a 50-Å-thick $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$ charge-supply layer doped with Si to $8 \times 10^{18} \text{ cm}^{-3}$, a 200-Å-thick n -type $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$ gate barrier doped to $2 \times 10^{17} \text{ cm}^{-3}$, and a 100-Å-thick $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ cap doped to $6 \times 10^{18} \text{ cm}^{-3}$. A 2500-Å-thick GaAs buffer is doped to $1 \times 10^{17} \text{ cm}^{-3}$ to simulate conductive layers of devices to be integrated. The AlGaAs gate layer is also doped to provide a vertical low-resistance path from the top cap to the device under the pHEMT in a real circuit.

Two samples were first implanted with protons at 30 keV with doses of $3 \times 10^{12} \text{ cm}^{-2}$ (sample A) and $6 \times 10^{12} \text{ cm}^{-2}$ (sample B). Then Ni/Ge/Au ohmic metal was patterned on the implanted samples as well as an as-grown control sample by liftoff and alloyed at 420°C for 20 s. The devices were isolated by mesa etch while the leakage current between isolated devices was monitored during the etch. For proton-implanted samples, the isolation became acceptable after only 600 Å of etch while greater than 3000 Å of etch was required for the control sample. Finally, the n^+ InGaAs cap layer was etched off in the gate opening, which was defined by optical lithography, followed by a Ti/Au gate-metal liftoff. The gate length and the source-drain spacing are 1.5 and 7 μm, respectively.

The objective of the experiment is to provide a highly resistive buffer to the pHEMT by converting the conducting GaAs layer under the channel with implantation, as shown in Figure 4-1. This is possible by taking advantage of the fact that, although ion-implanted protons transform conducting GaAs to high-resistivity material, it has little effect on InGaAs [1]. The peak concentration of the proton is located near the interface of the conducting and the doped GaAs buffer layer.

The I_{ds} - V_{ds} plots for the pHEMTs are shown in Figure 4-2. At gate bias $V_{gs} = +1 \text{ V}$, the I_{ds} and the transconductance g_m for the control sample are 500 mA/mm and 200 mS/mm, respectively. These values decrease to 300 mA/mm and 185 mS/mm for sample A, and to 225 mA/mm and 150 mS/mm for sample B. The pinch-off voltage is greater than -4 V for the control sample, and -2 and -1.5 V for samples A and B, respectively. It is clearly shown that the drain current was reduced by proton implantation, and the amount of reduction increases with the dose of the proton. The g_m for sample A is comparable to that of a pHEMT fabricated on an undoped buffer layer. For the control sample, higher I_{ds} and g_m are attributed to the added

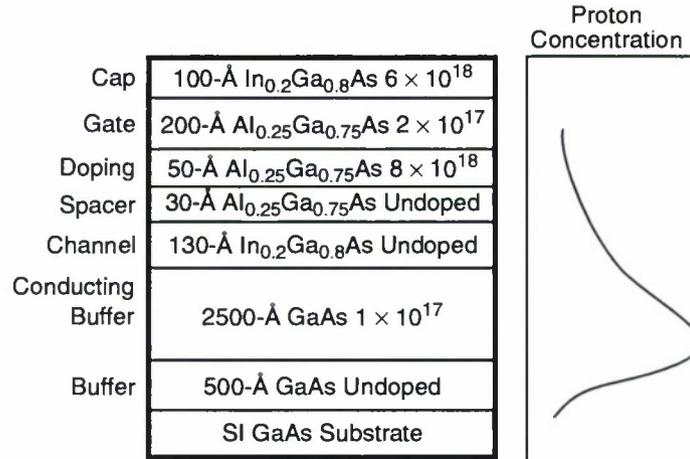


Figure 4-1. Layer structure of pseudomorphic high-electron-mobility transistor (pHEMT) and estimated profile of proton concentration for 30-keV implant. The profile of proton-induced damages is similar, but the density of the damage is generally higher, especially near the peak of the proton concentration.

parallel conduction in the buffer layer. The conductive buffer also results in a higher output conductance near pinch-off and the inability to remain pinched off at higher V_{ds} . The heat treatment during the ohmic alloying increased the I_{ds} of implanted samples only slightly, and the thermal effect diminished with increasing proton dose.

The 600-Å-deep mesa etch removed only the InGaAs channel and the doped layer above it. The breakdown voltage of Schottky contacts to the proton-implanted buffer, exposed after removing the top 600-Å-thick layers, is greater than 60 V. This breakdown voltage is approximately 10 times higher than that of the Schottky contacts on top of the buffer of the control sample, indicating a highly resistive layer is formed by the proton implant. The drain-source leakage current below pinch-off was 1.2 mA measured at $V_{ds} = 5.0$ V for the control sample, and it is less than 1 μ A for samples A and B. Since the off-state leakage current is mainly through the buffer layer, the result also proves the conversion of the doped buffer by the proton implant. The effective carrier concentration in the buffer after the proton implant, approximated from the conventional C-V technique, decreases with the depth and is more than an order of magnitude lower than the original 10^{17} cm⁻³. However, there is no apparent difference in carrier concentration in AlGaAs layers above the InGaAs channel for all samples, indicating that the proton caused negligible damage in these layers.

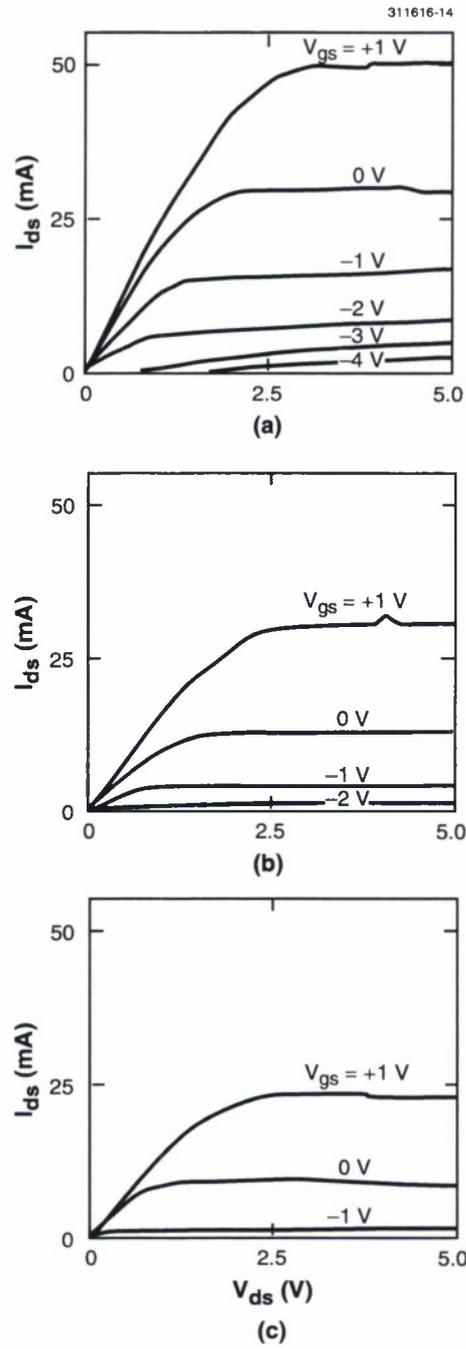


Figure 4-2. I_{ds} - V_{ds} plots of 100- μm -wide pHEMTs: (a) control sample, (b) sample A, and (c) sample B.

The unity-current-gain cutoff frequency f_T , obtained from on-wafer S-parameter test data, increased from 7.2 GHz for the control to 16.2 GHz after $3 \times 10^{12} \text{ cm}^{-2}$ proton implantation (sample A) and dropped slightly to 13.8 GHz with heavier proton dose (sample B). The f_T values of implanted samples are higher than the 12 GHz of a conventional pHEMT having similar device dimensions, strongly suggesting that the quality of the InGaAs layer was preserved. The maximum frequency of oscillation f_{max} also increased from 14.3 GHz for the control to 25.2 and 23.0 GHz for samples A and B, respectively.

Values of the equivalent-circuit elements were derived by fitting the calculated results to measured S-parameters of 100- μm -wide pHEMTs. The most significant difference for all circuit elements is the gate-source capacitance C_{gs} , which is 0.26 pF for sample A and 0.3 pF for sample B. In the control sample the gate voltage has to modulate charges not only in the InGaAs channel but also those in the conducting buffer, resulting in a more than doubled C_{gs} of 0.72 pF. The gate-drain capacitance also increases from 0.013 pF for the implanted samples to 0.033 pF for the control sample. Although g_m is approximately 15% higher, a much larger gate capacitance of the control sample results in a lower f_T than the implanted samples. Higher resistivity of the buffer layer increases the drain-source output resistance by two folds in proton-implanted samples. On the other hand, the increase of the source resistance R_s for the implanted samples is less than 10% because R_s is determined mainly by the contact resistance and the resistivity of doped InAlAs layers and the InGaAs cap, and none of them was affected by the proton implant.

Based on the selective effectiveness with different materials, it is demonstrated for the first time that protons can be implanted through pHEMT structures to convert conductive GaAs buffer layers underneath while preserving the pHEMT performance. The heavily damaged area, which is near the peak of the proton concentration, should be kept away from the AlGaAs charge-supply layers to minimize possible carrier compensation. The fabrication is compatible with planar GaAs manufacturing processes, and all the critical features are lithographically defined on the top surface, allowing a planar integration of high-density integrated circuits consisting of pHEMTs and previously incompatible devices like RTDs and photodiodes.

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5. MICROELECTRONICS

5.1 AXAF CCD IMAGING SPECTROMETER

The Advanced X-ray Astronomical Facility (AXAF) is the third of NASA's Great Observatories (the other two being the Hubble Space Telescope and the Compton Gamma Ray Observatory), and it is planned for launch in late 1998. It is intended to observe x rays at energies between 0.25 and 10 keV in both spectroscopic and imaging modes, using two arrays of extremely high performance charge-coupled devices (CCDs) developed in the Microelectronics Group. The first array of CCDs is abutted in a 1×6 pattern, as shown in Figure 5-1. This is the spectrometer array, and an x ray impinging on a given column of a CCD has a specific energy, due to the diffraction grating of the high-resolution mirror assembly aboard AXAF. The 2×2 group of CCDs constitutes the imager array, allowing an image of x-ray sources to be obtained. In this latter array, spectrometry may also be performed since the relationship between x-ray energy and photoelectron packet size has been calibrated. Knowledge of the x-ray energy allows astronomers to establish the chemical species present in the x-ray source.

In order to obtain the highest resolution, the CCD chips in the spectrometer array are arranged to approximate a cylindrical surface, and those in the imaging array are arranged to approximate a spherical surface. Conforming to these geometries requires a precision of about $12 \mu\text{m}$ in the placement of the chips.

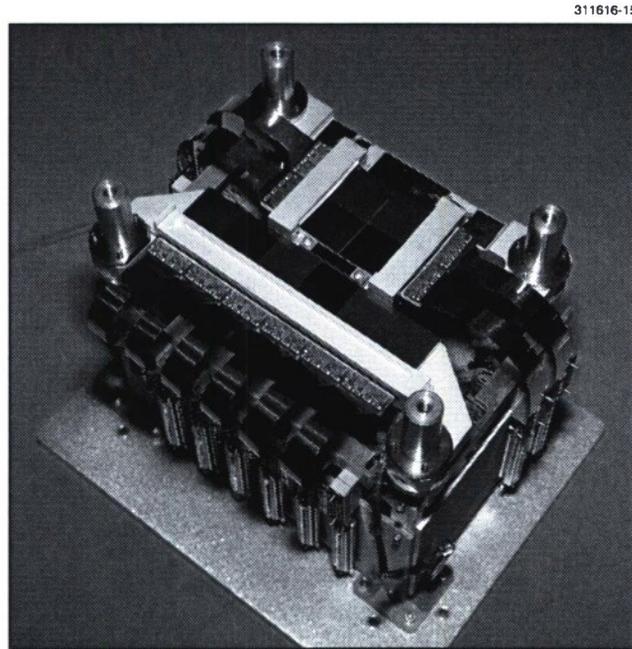


Figure 5-1. Advanced X-ray Astronomical Facility (AXAF) charge-coupled device (CCD) imaging spectrometer.

Maintaining this placement between room temperature and the temperature of operation (-120°C) and during launch places severe constraints on the alignment system and the beryllium paddle that holds the chips, as well as on the flexible connectors which allow for input and output to the devices.

As mentioned above, the CCDs are extremely high performance chips with noise levels on the order of 3 to 5 electrons per frame. The charge-transfer efficiency (CTE) is 0.99999 or better at the beginning of the mission, with narrow troughs incorporated in the columns of the CCDs to mitigate the effects of proton-induced damage while in orbit [1]. To improve the response of the CCD to low-energy x rays, two of the devices in the spectrometer array have been back-surface illuminated [2] so the x rays are not absorbed in the polysilicon gates that are present on the front side of the device. In this process the devices were thinned from the back so that only $45\ \mu\text{m}$ of Si remains, and the exposed surface is treated to lower the background current and to drive photoelectrons through the Si to the buried channel of the CCD. This is critical, since the absorption distance for x rays at these energies is only around 100 nm. The difference in performance is illustrated in Figure 5-2, where it is apparent the quantum efficiency of the back-illuminated device is clearly superior for energies of 1500 eV or lower, especially below the $0\text{-}K_{\alpha}$ absorption edge at 527 eV. The back-illuminated devices are the second and fourth from the left in the spectrometer array, as shown in Figure 5-1.

At the other end of the spectrum, around 10 keV, the absorption depth of the x rays is tens of μm , so it is necessary to have depletion depths in the Si of this order, which requires the use of single-crystal material with dopant concentrations around $10^{12}/\text{cm}^3$. This very high purity, in turn, requires the use of Si prepared by a method that makes it more susceptible to the generation of dislocations during the fabrication process. These dislocations can lead to the presence of bright columns, high background current,

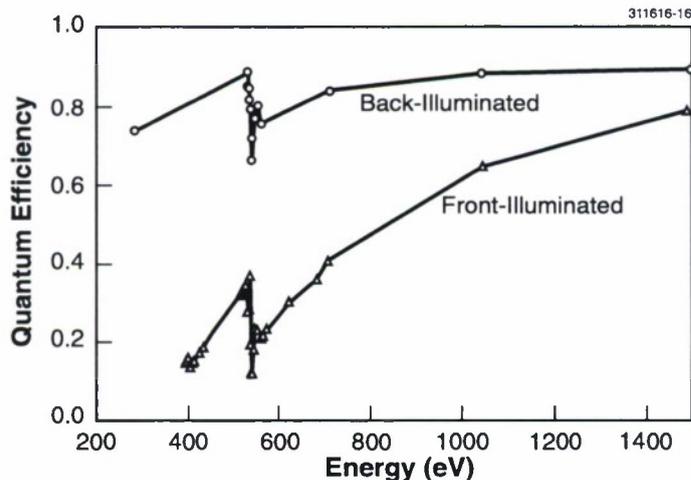
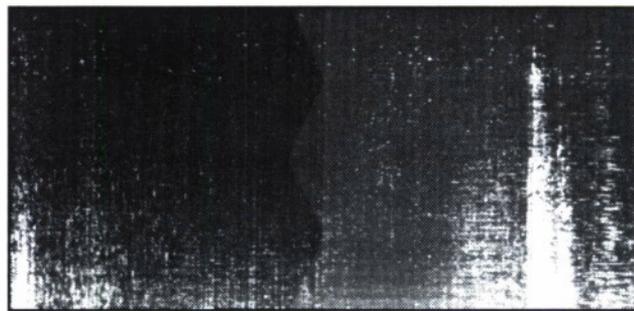


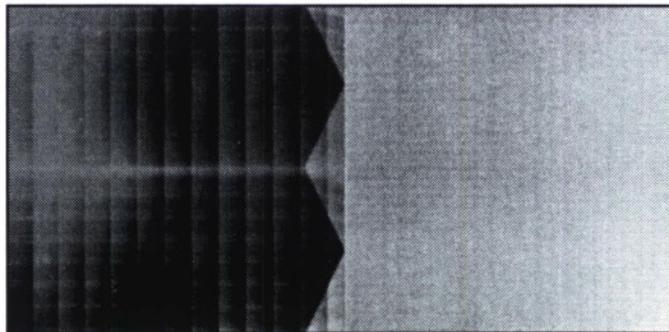
Figure 5-2. Quantum efficiency of front- and back-illuminated CCDs.

and poor CTE, so it is essential for AXAF that the number of dislocations is minimized. Processes were developed to control the generation of slip [3]. These included the use of polysilicon furnace boats, wider spacing of wafers in the boats, and control of thicknesses of overlayers, such as the polysilicon, that contain residual stresses. The results are shown in Figure 5-3, which indicates the presence of dislocations as bright regions (areas of high background current). In Figure 5-3(a) the results are shown for the standard process; this chip contains regions of very high dislocation density (approximately $10^6/\text{cm}^2$), particularly near the lower right corner of the chip. The results of incorporating the process improvements are shown in Figure 5-3(b), where there are no dislocations present at all.

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(a)



(b)

Figure 5-3. Background current maps for CCD chip, showing results for (a) standard process with dislocations, and (b) improved process with no dislocations.

With these devices verified as being flight quality, population of the flight paddle was performed in 1997 and the paddle was installed into the instrument by the MIT Center for Space Research, which with Pennsylvania State University is responsible for the AXAF CCD imaging spectrometer design and integration. The flight array has been tested at NASA Marshall Space Flight Center, and both energy resolution and angular resolution are limited by the x-ray optics and not the CCDs. Nevertheless, the energy resolution, DE/E is approximately 0.001, and the angular resolution is 1.0 arc sec; both of these quantities are a factor of 10 superior to those achieved on any x-ray observatory in orbit, and suggest that AXAF will make great advances in our understanding of high-energy processes in the universe.

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6. ANALOG DEVICE TECHNOLOGY

6.1 LOW-POWER MATCHED FILTER CONFIGURED FROM CHARGE-DOMAIN ELEMENTS

A charge-domain matched filter has been developed and demonstrated in a standard 1.2- μm CMOS device-prototyping process incorporating charge-coupled device (CCD) elements. The device was developed to provide binary matched filtering in applications requiring minimal size, power, and weight and is well suited to mobile and handheld binary communication equipment for fast data acquisition and demodulation.

A photomicrograph of the charge-domain matched filter is shown in Figure 6-1, where major elements in the design have been indicated. The circuit was designed to operate with a 5-V positive supply, -1 to -4 -V substrate bias, 0.5-V analog inputs, and 0–5-V clocks. The matched filter operates effectively to an input-sampling rate of 20 MHz, and expectations are that a refined version of this device would be capable of operation to beyond a 40-MHz sampling rate.

The matched filter consists fundamentally of a CCD analog delay line tapped at periodic intervals along its length. The delay line stores and delays a representation of an analog input signal. As the stored signal propagates along the line, taps nondestructively sense the signal at their location and pass signal

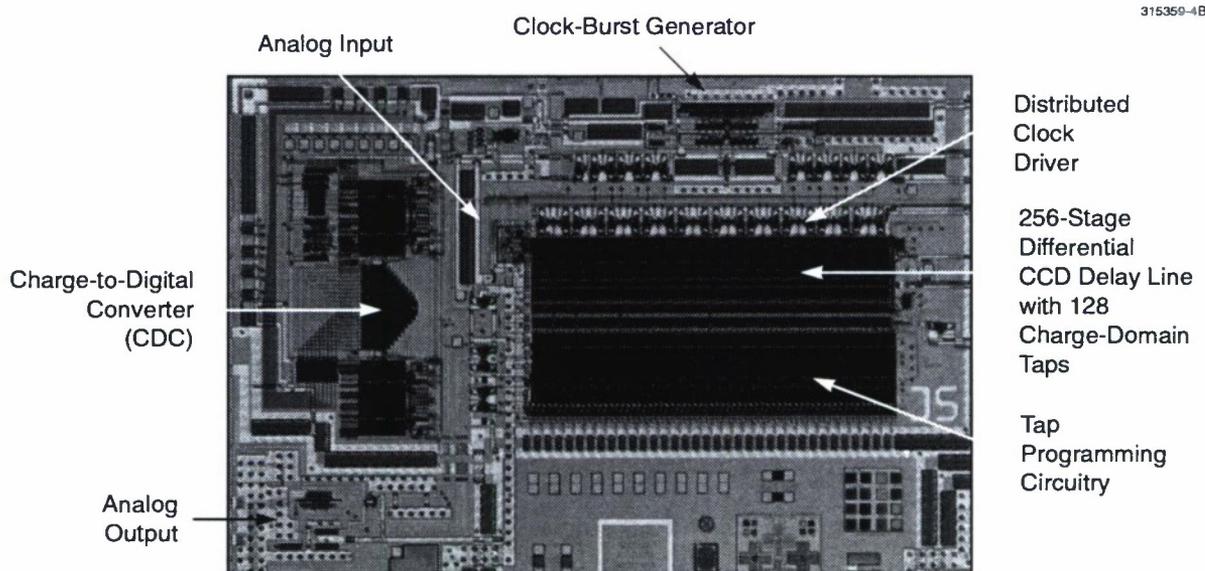


Figure 6-1. Photomicrograph of charge-domain matched filter.

replicas to a plus or minus sum bus through switches, which are controlled by binary signals from tap-programming circuitry. Each sum bus integrates the signals from all the taps tied to it, and a differential circuit takes the difference of the integrated signals from the two busses to produce the final matched-filter output. The plus bus is tied to the plus input of the differential circuit, and the minus bus is tied to the minus input so that a tap tied to the plus bus has a positive weight while a tap tied to the minus bus has a negative weight. Taps tied to neither bus have a zero weight and can be used to control the overall length of the matched filter. A device of this type with ternary-weighted taps is ideal for the matched filtering of binary waveforms.

In charge-domain circuitry a fixed amount of charge is operated upon in response to a clock, and there are no continuously moving charges or currents. There is, therefore, only dynamic power consumption in circuits of this type, which is dependent upon the amount of charge transferred each clock cycle and is directly proportional to clock frequency. A matched filter implementation that takes maximum advantage of charge-domain techniques will be superior in terms of minimal size, power, and weight relative to ones that do not. Furthermore, when charge-domain circuitry is used for voltage-to-charge generation, it provides a considerable improvement in linearity compared to more conventional approaches.

Figure 6-2 is a functional block diagram of the device. In practice, the charge-domain matched filter requires a fully differential approach to avoid a code-dependent offset at its output, and this is realized by effectively using two filters in parallel. The analog-input section generates charge packets based upon the difference between samples of analog inputs $IN+$ and $IN-$. Delay-line taps are charge replicators that non-destructively sense delay-line charge and pass charge replicas to charge-integrating sum busses. Each delay-line tap in one filter has a corresponding tap in the other. Taps are programmed so that when a tap in one filter is tied to one of the two sum busses its corresponding tap is automatically tied to the other. The effect of this arrangement is that the output from the overall matched filter is the difference in the outputs from the two filters. Since the input signal fed to one filter is fed inverted in amplitude to the other and the delay-line constant-charge levels are the same, the signal responses from the two filters reinforce while the output offsets cancel. Total charge integrated by the sum busses produces a voltage across the total bus capacitance that includes any capacitive load to the bus. The quantity of charge collected by a sum bus, however, is typically much too large to pass on for further processing so that the sum-bus voltage is converted to a smaller charge packet using a voltage-to-charge converter. The smaller charge packets from the plus-and-minus sum busses are subsequently fed to the differential input of an analog-to-digital charge-domain converter (CDC) [1] to produce an 8-bit digital representation of the matched-filter output. Sum-bus voltages are also fed to a differential amplifier that is separately powered when an analog output is desired.

As with past Lincoln-designed CCD-based matched filters [2],[3], there are twice as many CCD delay-line stages as there are taps. This is necessary to allow for the accommodation of taps within the delay-line pitch. Minimal tap size is limited by process design rules while delay-line pitch is chosen on the basis of maximum speed. The differential CCD delay line has 256 stages with 128 differential taps distributed uniformly along its length at every other stage. Since only every other stage is tapped, an input signal must be double sampled into the device. A benefit of this approach is that it ensures that at least one sample

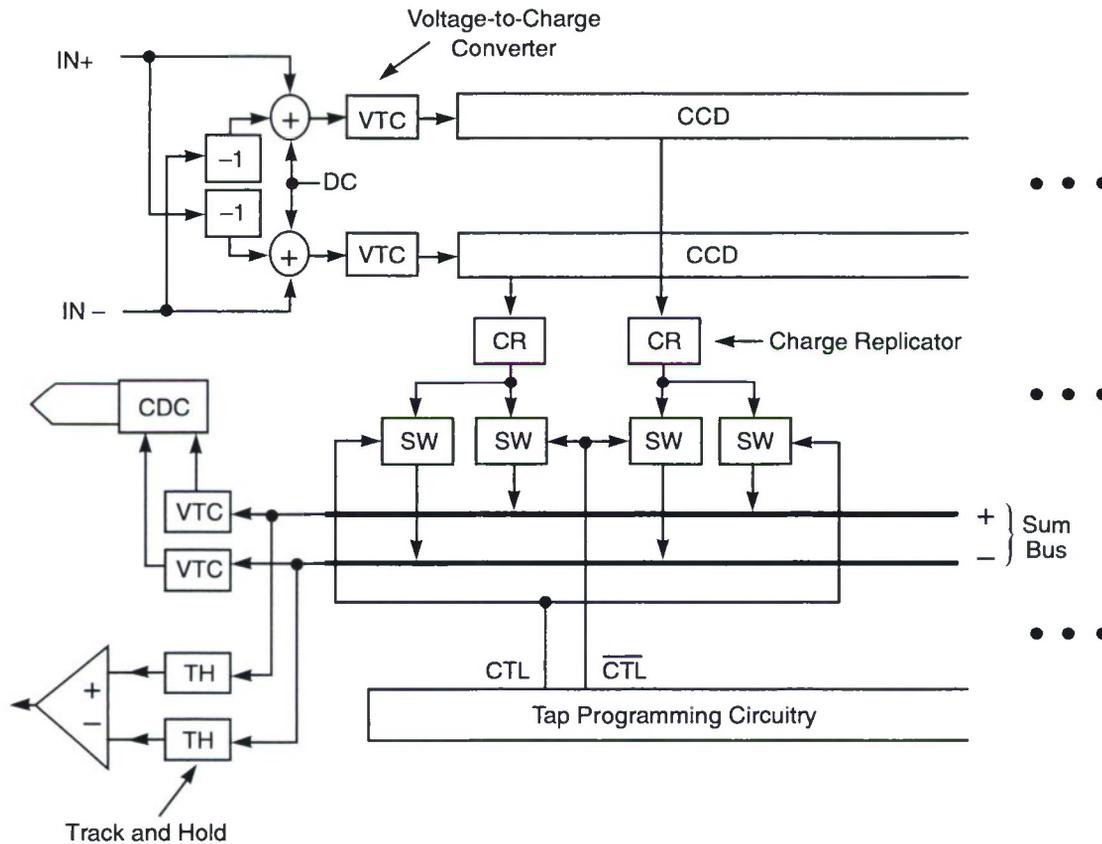


Figure 6-2. Functional block diagram of charge-domain matched filter.

does not fall at a bit transition and can, therefore, be used to fine tune the input-sampling process. Also, specific signal-processing algorithms have been devised that advantageously exploit this half-tapped architecture. Alternatively, two different signals can be alternately sampled at the input. These two signals will subsequently produce interleaved charge patterns within the CCD delay line that will correlate independently against the same pattern of programmed taps. Their independent results will be interleaved at the matched-filter output and can be separated by demultiplexing in either the analog or digital domain.

Clock burst-generator and driver circuits have been indicated on the photomicrograph of Figure 6-1. These have been purposely left out of the block diagram of Figure 6-2 for the sake of simplicity, but they are otherwise critical elements in the design. Clocking is required throughout the matched filter for input-voltage sampling, voltage-to-charge generation, charge transfer, charge replication, and sum-bus and various circuit resets. The numerous clocked functions that must be performed between sample times, however, cannot be performed simultaneously. The sample period must be divided into a minimum of nine

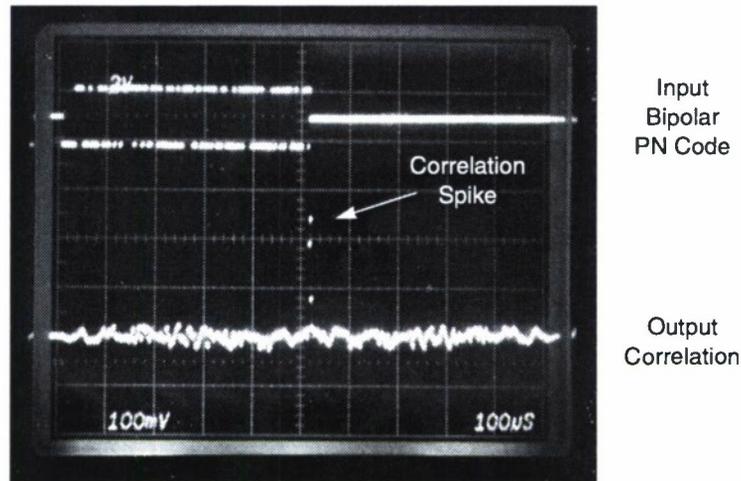
distinct timing states to operate effectively. In our design, a burst of clocks is generated at every input rising clock edge. To accomplish this, the clock burst-generator circuitry incorporates a nine-tap digital delay line to define nine timing states. An input rising edge acts as a burst trigger. This edge propagates down the delay line, which consists of a string of inverters, and produces a narrow pulse, used to set or reset flip-flops, as it passes by each tap. Such a design is modular. The number of taps equals the number of timing states and the number of flip-flops equals the number of clocks. Furthermore, since clocks are defined by connections to delay-line taps, they are easily modified by a change in only a single mask layer—the vias between two layers of metal.

Charge is transferred in the differential CCD delay line using a four-phase clock. For each phase, ten drivers are tied in parallel and distributed evenly along the length of the delay line. The drivers for the four phases are interleaved in an alternating pattern. This distributed-driver architecture was adopted to ensure uniform clocking of charge along the CCD delay line with minimal timing skew and minimal time for charge settling on the sum busses. The distributed clock driver is indicated on the photomicrograph of Figure 6-1.

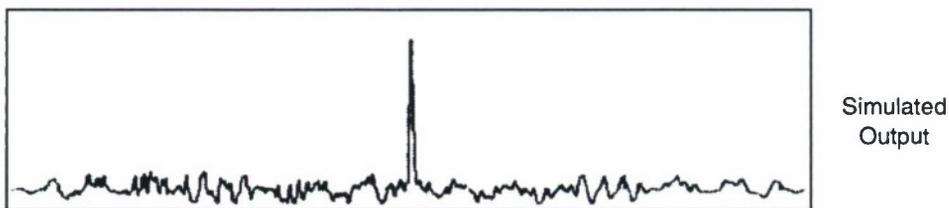
The maximum voltage on a sum bus in the charge-domain matched filter is proportional to the maximum amount of charge dumped onto the bus and inversely proportional to the total bus capacitance. The CDC was designed to quantize the expected full range of bus-voltage variation into 256 levels (8 bits). As more taps are turned off, however, the maximum charge dump and bus voltage decrease. Although a CDC reference input can be changed to force 8-bit digitization over a smaller input voltage range, this approach reduces accuracy and the inherent value of the least significant bits. To circumvent this problem, externally controlled switching field-effect transistors have been incorporated into the charge-domain matched filter to switch out portions of the sum bus in factor-of-2 increments, thereby reducing bus capacitance and renormalizing maximum bus voltage. The bus can be reduced to a minimum length encompassing eight taps. Ideally this approach maintains a full 8 bits of accuracy over the full range of bus-voltage variation whenever a power-of-2 number of taps is used. As bus length is progressively shortened, however, the effectiveness of full-scale renormalization degrades as the extraneous capacitive load represents a greater and greater portion of the overall bus capacitance.

The CDC is a Lincoln design that has been described elsewhere [1]. It is a charge-domain pipelined analog-to-digital converter architecture whereby digital bits evolve successively in time with highest-order bits generated first. Reformatting circuitry is required to ensure that all 8 bits for each output-sample exit simultaneously from the device. The original form of the design was limited to a clocking rate of just over 20 MHz. To boost operation into the 40–50-MHz range, a circuit structure incorporating two multiplexed CDCs was adopted.

Observations based solely upon the analog output indicate that the bulk of the charge-domain matched filter works well for a first-cut design. The static-power requirement is less than 5 mW while the dynamic power is about 10 mW/MHz. A significant reduction in circuit size with an equivalent reduction in dynamic power is considered highly likely since the differential CCD delay line and clock drivers were both sized somewhat conservatively in this design.



(a)



(b)

Figure 6-3. Matched-filter correlation performance: (a) input pseudonoise (pn) code (upper trace) with respective output correlation (lower trace), and (b) simulated correlation output using equivalent charge-transfer efficiency.

A lower-than-expected CCD delay-line charge-transfer efficiency (CTE) currently limits the performance of the device. Since a buried-channel implant was used in the CCD delay line to force the charge-propagation channel into the substrate, surface states are not considered the source of the low CTE, and an investigation will be required to determine the precise mechanism involved. The CTE improves for greater current starving and longer clock bursts, which appears to indicate a potential clock-skew-related problem. The burst generator, however, stops functioning when current starving broadens the burst to only about 2 to 3 times its minimum width, and this thereby sets a limit to the improvement in CTE using this approach. Beyond about 20 MHz the clock burst must be decreased from its maximum attainable width, which degrades the CTE. Furthermore, an apparent skew-related problem kicks in beyond 20 MHz causing

a progressive reduction in tap signal strength down the length of the delay line. Design refinement will require investigation into all these phenomena.

Figure 6-3 shows the performance of the charge-domain matched filter for a 127-chip pseudonoise (pn) code. An actual oscilloscope trace of a pn-code input is shown at the top of Figure 6-3(a), and the matched-filter output for this code is shown in the bottom trace. This latter result can be seen to compare well to the simulated output in Figure 6-3(b), obtained using an equivalent level for CTE.

One of the motivating factors for producing an analog form of matched filter is that analog samples of a signal can be operated upon using circuitry encompassing a significantly smaller integrated circuit die area than an equivalent digital circuit working upon digitized versions of the analog samples. The trade-off between an all-digital vs an analog approach is usually a trade-off between size/power and accuracy. A digital implementation can operate at higher accuracy at the expense of greater size and power owing to the need to carry and operate upon many bits per sample. Analog processing is typically limited to accuracies representing about 6 to 8 digital bits and accuracy exceeding 8 bits is typically very hard to obtain. Applications that do not require accuracies greater than this, such as matched-filter detection and demodulation in a handheld communication receiver, can benefit greatly from the use of analog processing techniques.

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7. ADVANCED SILICON TECHNOLOGY

7.1 PRECISION MULTICHIP MODULES

The precision multichip modules (MCMs) program consists of collaboration between the Mayo Foundation's Special Purpose Processor Development Group (SPPDG) and MIT Lincoln Laboratory to design and fabricate high-performance MCMs for RF and mixed-signal applications. Results of a Mayo SPPDG study indicated that commercial companies are focused on the high-volume, low-cost segment of the market. It was concluded that these commercial substrates are not precise enough for many high-performance DoD needs. In particular, transmission line impedance is not adequate. The intent of this program is to meet the DoD need for low-volume, tight-tolerance, and high-performance MCM substrates not available elsewhere. This will be accomplished through the application of advanced integrated circuit processing techniques that include tight control of process specifications. A set of design rules will be developed, and research substrates will be provided to the DARPA MCM user community. If demand warrants, the technology will be transferred to a commercial manufacturer for DoD applications.

Development is focused on a fully planar approach modeled on Lincoln Laboratory's fully planar CMOS back-end metallization [1]. This approach includes chemical mechanical polishing of intermetal dielectrics, damascene aluminum via and stacked via plugs, and dry etching of all levels. A proposed MCM cross section is shown in Figure 7-1. The initial test coupon contains one power/ground-plane pair and two signal levels separated by low-stress silicon dioxide. All metallization consists of pure aluminum except for the via plugs which consist of aluminum (1% silicon) and a plug liner containing titanium nitride and titanium. The dielectric between the power and ground planes will initially be silicon dioxide, but will later be replaced with anodic aluminum oxide for decoupling purposes. The anodization process is being transferred to Lincoln Laboratory from the University of Arkansas. Detailed layer thicknesses and linewidths are presented in Table 7-1.

Process development started with Lincoln's fully planar CMOS back-end process module [1]. Levels of interconnect are built up through the repeated application of this module, which contains the following steps: low-stress silicon dioxide dielectric deposition, chemical mechanical planarization (CMP) of the dielectric, vertical via etch, aluminum (1% Si) plug fill, CMP to remove field metal, signal layer deposition, and patterning.

Low-stress silicon dioxide is deposited by plasma-enhanced chemical vapor deposition from TEOS and oxygen precursors. The deposition tool has built-in stress control that operates by controlling the ion bombardment of the growing film. Stress in the film is adjusted to be $\sim 8 \times 10^8$ dynes/cm², compressive. Film stress is measured on a mechanical profilometer by analyzing wafer curvature before and after film deposition.

Following dielectric deposition the film is planarized through the use of CMP. This technique makes use of urethane polishing pads and silica slurry to remove topography. A planar surface means that less overetch is required at the signal level. This reduced overetch translates into better linewidth control, which

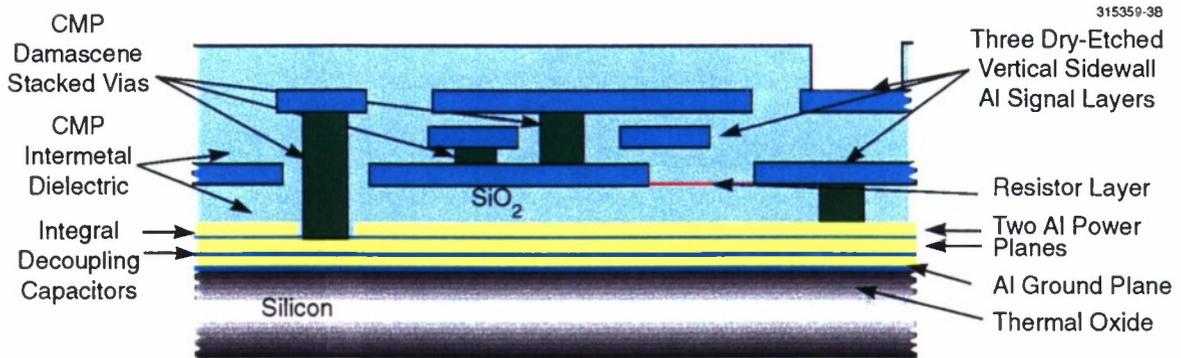


Figure 7-1. Proposed multichip module (MCM) cross section.

TABLE 7-1
Process Design for Multichip Modules

Layer	Thickness (μm)	Dimension (μm)
Power/ground planes	1	N/A
Power/ground-plane dielectric	0.15	N/A
Signal-2/ground-plane dielectric	7	N/A
Via 3/via 2/via 1	0.15/7/2	7
Signal 2	2	10.5
Signal-2/signal-1 dielectric	2	N/A
Signal 1	2	19
Passivation	4	N/A

directly impacts transmission line impedance. In addition, the metal crosses no steps, which cause an abrupt change in thickness. Planarization does, however, have some difficulties. Film uniformity is both pattern and process sensitive. Intradie and across-wafer dielectric thickness variations exist, which are caused by pattern effects and by slurry depletion across the wafer during CMP. Work is in progress to minimize the nonuniformity.

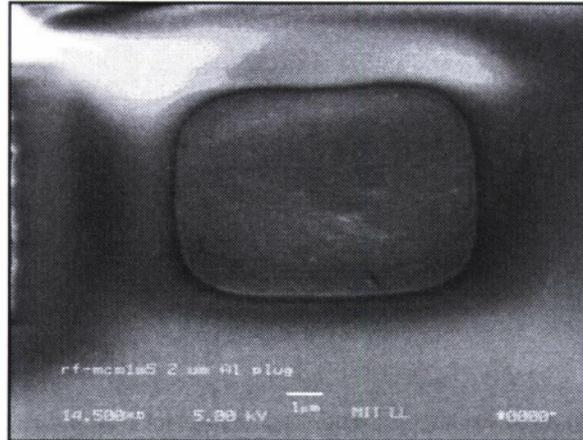
Vertical via etching is accomplished by reactive ion etching. The all-dry process guarantees that the etched via maintains its mask dimension. This minimizes the surround requirements for metal above and below the via. These MCM dielectrics are much thicker than in conventional integrated circuit processing. Because of this it was determined that our traditional photoresist etching masks were too thin for the via etches. A new photoresist, Shipley 3625, is being used which can be spun to a thickness of 4 μm with 1% nonuniformity, 1σ , across wafer. For the via etch used, a silicon dioxide-to-photoresist selectivity of 2.3 to 1 was established.

Following via etching, the aluminum plug process is performed. This is a two-step process consisting of hot metal sputter deposition and CMP removal of field metal. The hot metal sputter deposition consists of a degas/soft sputter etch step, a 100-nm/30-nm TiN/Ti plug liner, and finally 500°C aluminum (1% silicon) deposition to flow metal into the via openings. CMP removal of the metal outside the vias is accomplished with alumina slurry. The dielectric serves as a polish stop (selectivity ~ 30 to 1). The use of metal plugs allows vias to be stacked. Some partial voiding of the 7- μm -deep plugs was observed during processing. This voiding in turn caused local recessing of dielectric during plug polish. Work is under way to resolve this problem, perhaps by reducing the aspect ratio and performing the plug in two steps. No voiding was observed on the 2- μm -deep plugs. Figure 7-2 shows scanning electron micrographs (SEMs) of via plugs.

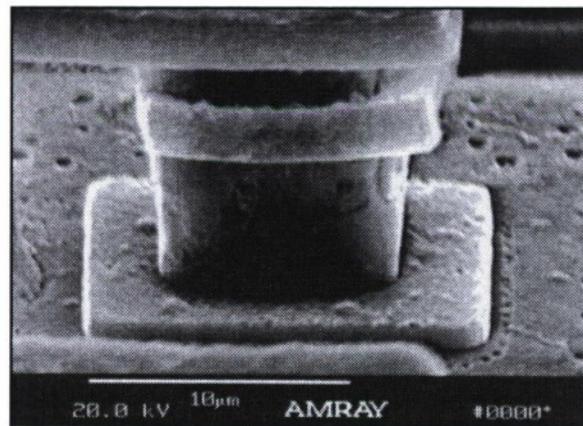
Signal layers are fabricated of pure aluminum and are sputter deposited at room temperature. The signal layers are currently being dry etched in an older tool. Etches performed in this tool exhibit pattern-dependent effects and the edge-to-center line uniformity is not ideal. As part of this program, a state-of-the-art metal etch system was evaluated and purchased. It should exhibit less pattern-dependent effects, have better photoresist selectivity, and better etch uniformity. It is currently being installed in the Microelectronics Laboratory. Figure 7-3 shows an SEM photograph and drawing of a finished MCM test coupon.

The RF test structures in the MCM test coupon were designed by Mayo SPPDG, with transmission lines designed for 50- Ω impedance. There are four complete coupons per 150-mm wafer. Process monitors, both SEM and electrical, were added by Lincoln Laboratory. They consist of signal vias and via chains, including stacked structures, snakes and combs for interlevel and intralevel shorts and opens, line-width loss measurement structures, and SEM structures consisting of staggered and stacked vias and lines of various dimensions. Figure 7-4 shows some examples of process test devices.

The first lot of test coupons has been fabricated, and the process monitoring structures have been measured. Via chain yield was 100% for all chain combinations. The mean resistance of single vias was $<0.2\ \Omega$ with $1\ \sigma$ being $<0.02\ \Omega$. The yield on snakes and combs was also 100%. The resistance of signal 1



(a)



(b)

Figure 7-2. Aluminum via plugs: (a) top down view after metal chemical mechanical planarization, and (b) four-level metal with stacked via plugs (oxide removed to show detail).

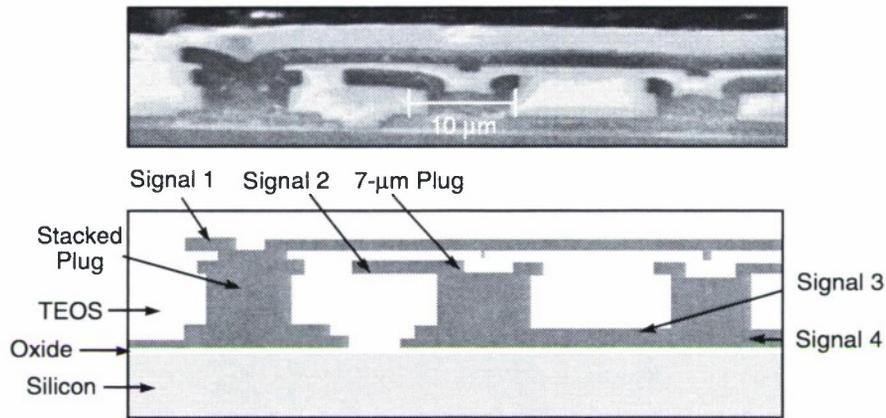


Figure 7-3. Fabricated MCM cross section.

was $\sim 35 \Omega$ for a 37.8-mm line with $19\text{-}\mu\text{m}$ linewidth. Signal 2 was $\sim 100 \Omega$ for a 37.8-mm line with $10.5\text{-}\mu\text{m}$ linewidth. Leakage was $< 3 \times 10^{-11}$ A. Initial RF test results from Mayo look promising. Figure 7-5 shows S-parameters measured by Mayo of transmission lines of different lengths.

Thus, during 1997 an MCM test coupon has been designed, and masks have been fabricated. During the design phase, initial process development and process flow for the MCM coupons was established. The first lot of coupons has been successfully fabricated. A state-of-the-art metal etcher was evaluated and purchased and is being installed. Finally, a subcontract has been issued to the University of Arkansas to transfer the aluminum anodization process for the decoupling capacitor.

J. M. Knecht

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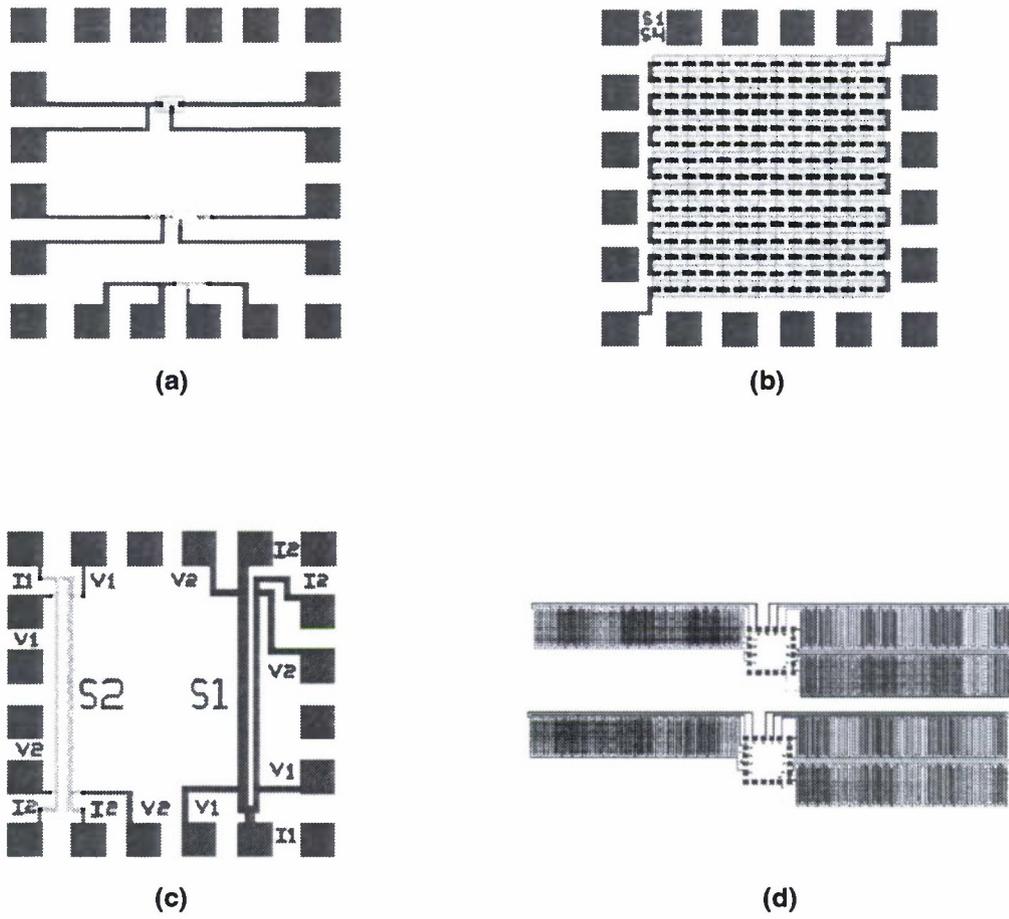


Figure 7-4. Process test structures: (a) single via, (b) via chain, (c) linewidth measurement, and (d) snake and comb.

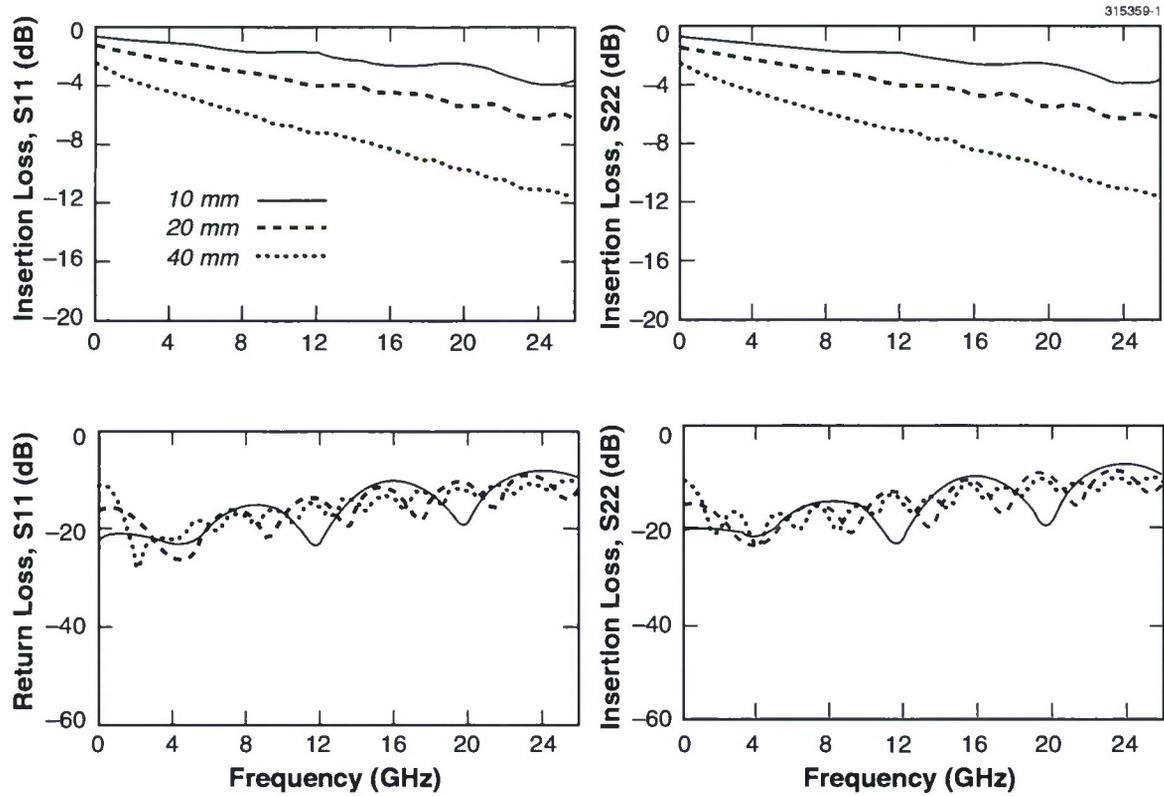


Figure 7-5. Frequency domain measurements from upper microstrip transmission lines of three different lengths.

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