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DEVELPOMENT AND PACKAGING OF MICROSYSTEMS USING FOUNDRY SERVICES

Dissertation

Jeffrey T. Butler, Captain, USAF

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DEVELOPMENT AND PACKAGING OF MICROSYSTEMS USING FOUNDRY SERVICES

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- Jeffrey T. Butler

Table of Contents

List of Figures

List of Tables

Abstract

Micro-electro-mechanical systems (MEMS) is a relatively new and rapidly growing field of research. Several advances to the MEMS and microsystem state of the art were achieved through the design and characterization of novel MEMS devices and packaging which are compatible with CMOS microelectronics. Empirical and theoretical models of polysilicon thermal actuators were developed to understand and simulate the behavior of thermal actuators. These models can be implemented in microelectronic circuit simulators such as SPICE and allow the simultaneous simulation of thermally actuated MEMS and microelectronics.

The most extensive investigation of the Multi-User MEMS Processes (MUMPs) polysilicon resistivity was also performed. The first published value for the thermal coefficient of resistivity (TCR) of the MUMPs *Poly 1* layer was determined as 1.25×10^{-3} K^{-1}. In addition, the sheet resistance of all the MUMPs polysilicon layers was found to be dependent on the linewidth due to the presence or absence of lateral phosphorus diffusion.

The development of robust devices and models permitted the functional and physical integration of MEMS with CMOS controllers. The functional integration of MEMS with CMOS was demonstrated through the design of automated positioning and assembly systems. A new power averaging scheme was devised to take advantage of the physical characteristics of polysilicon thermal actuators. The development of this scheme creates a whole new arena of control methodologies for MEMS.

The packaging of MEMS using foundry multichip modules (MCMs) was also demonstrated and shown to be a feasible approach to the physical integration of MEMS with other microelectronic technologies. MEMS test die were packaged using the Micro Module Systems MCM-D and the General Electric High Density Interconnect and Chip-on-Flex MCM foundries. Procedures were developed and implemented for successfully releasing the MEMS die after packaging. Xenon difluoride (XeF_2) was found to be an

excellent post-packaging etchant for MCM packaged bulk micromachined MEMS die. For surface micromachining, hydrofluoric acid (HF) can be used for release of MEMS after MCM packaging.

Finally, all of the MCM packages, MEMS die, and CMOS microelectronics die used in this research were foundry fabricated. In addition, a concerted effort was made to use and develop simple post-processing procedures for release and handling of the MEMS/MCM packages. The increasing availability of affordable, high performance foundry processes combined with the methodologies developed in this dissertation will allow a wide range of designers to implement robust and cost-effective microsystems.

Chapter 1. Introduction

The objective of this research is to investigate the development and packaging of Micro-electro-mechanical Systems (MEMS) and microelectronics. This chapter presents a summary of the problems to be solved, specific objectives, and accomplishments of this research effort as well as the organization of the document.

1.1 Problem Statement and Research Objectives

The over-arching mandate for this research effort is to develop procedures or a family of procedures for effectively and reliably packaging MEMS with integrated circuits in multichip modules (MCMs) using foundry sources. Micromachining is a rapidly emerging field which is making the transition from a research novelty to commercial industry. Micro-electro-mechanical Systems (MEMS) have already found commercial applications as accelerometers, pressure sensors, ink jet nozzles, and projection displays. More complex micromachined devices are now reaching maturity with the promise of greatly reducing the size while improving system and sensor performance in a wide range of applications.

The U. S. Air Force is particularly interested in MEMS as a way of reducing the size and cost of satellites and unmanned aerial vehicles (UAVs). The life cycle cost of a satellite or air vehicle is largely dependent on the weight of the system. For example, it has been estimated that every pound of weight eliminated from the Brilliant Eyes spacecraft would result in a life cycle cost savings of 2 million dollars [1]. MEMS clearly has the potential for reducing the weight of the system. In a recent example, an

inertial navigation unit used for aircraft was replaced by a MEMS-based system weighing less than $1/20^{th}$ of the original system at less than 10 percent of the cost [1]. Clearly, the Air Force and industry have strong reasons to be interested in the development and insertion of MEMS technology into many new applications.

One of the key problems addressed by this research is integration and packaging of MEMS and control circuitry in a manner that minimizes the size of microsystems while still providing superior functionality. The many advantages of micromachined systems are largely negated if they cannot be efficiently integrated and packaged with electronics [1]. Integration of MEMS and electronics is complicated by incompatibilities in the fabrication and processing of MEMS and integrated circuits. In addition, complex MEMS devices are now reaching the level of sophistication where volume production and reliability are being considered. Consequently, research dedicated to the packaging and development of microsystems is both timely and of great importance to the Air Force and the MEMS community. The Air Force Research Laboratory, the sponsor of this research, is particularly interested in integration and packaging of MEMS with other technologies using multichip modules. The use of multichip modules would provide a cost-effective means of efficiently integrating MEMS systems without the expense involved with developing unique fabrication processes.

Another critical problem addressed by this research is the ability to develop integrated MEMS systems using computer automated design (CAD) and foundry services. Several classes of MEMS such as thermally actuated devices do not have performance models suitable for use in commonly used CAD tools. Theoretical models

and accurate material characterizations are absolutely needed for the development of CAD tools for MEMS. These models are particularly important for MEMS designers planning to employ foundry processes as they provide a means of simulating the performance of systems prior to fabrication. The use of simulation enables the designer to perform numerous design iterations before expending money on foundry fabrication which typically takes two months to complete.

The problems of MEMS packaging and the development of integrated microsystems are significant issues addressed by this research. The specific objectives and questions targeted by this research are outlined in more detail in Sections 1.1.1-1.1.3.

1.1.1 Are multichip module foundries suitable for MEMS?

One approach to the integration and packaging of MEMS and electronics is to use multichip modules (MCMs). MCM technology has improved dramatically over the last decade in response to requirements for better packaging and performance in microelectronics [2]. MCMs offer an attractive approach to integrating and packaging MEMS with electronics because of the ability to support a variety of die types in a common substrate without requiring changes or compromises to either the MEMS or electronics fabrication processes.

Foundry services for MEMS, MCMs, and microelectronics are available, but little research has been done to marry the various technologies to produce viable microsystems. The use of foundry services may not provide the technologically optimum solution for meeting a specific requirement as compared to a custom solution. However,

foundry services provide access to state of the art alternatives for institutions such as AFIT which can not afford the high cost of in-house fabrication facilities.

Three of the more advanced MCM foundries were investigated for MEMS packaging. The General Electric high density interconnect (HDI) and chip-on-flex (COF), and Micro Module Systems (MMS) MCM-D represent three substantially different state of the art foundry multichip module processes. HDI and COF MCMs are unique in that the die are embedded in the substrate, while the MCM-D process is a more traditional approach to packaging where the die are located on top of a patterned substrate.

Although these processes were originally developed for microelectronics, the results of this research show that they can be adapted for MEMS packaging. Key considerations for MCM packaging of MEMS include whether to release the micromachined devices before or after packaging and the compatibility of the package materials with the MEMS release procedures.

1.1.2 Modeling and Simulation of MEMS Devices and Processes

Computer-aided modeling and simulation has become a key element in the success of microelectronics. Likewise, the models for MEMS devices and fabrication processes developed in support of this dissertation are important for the integration of MEMS and microelectronics. These models allow for the interaction of the MEMS devices with microelectronics and packaging to be simulated without the need for costly and time-consuming experimental trial and error. The models not only provide a means of simulating the performance of MEMS but also provide a theoretical insight into the

operation of the devices. The theoretical insights provided by the models are quite often non-intuitive and allow a greater understanding of the MEMS devices than can be achieved through empirical testing alone.

1.1.3 Development of Microsystems Using MCMs

The integration of MEMS and microelectronics to produce functional microsystems was also a specific area of research. This research effort provides methods of exploiting the thermal and mechanical nature of certain MEMS devices to make them more amenable to control by CMOS electronics. In addition, key considerations for successfully designing and producing a microsystem in a multichip module are defined.

1.2 Research Accomplishments

Several significant results were achieved or demonstrated during the course of this research effort. Some of the more exciting accomplishments are briefly highlighted below:

Multichip packaging of MEMS:

- Demonstrated feasibility of using HDI and COF for MEMS packaging.
- Proposed and demonstrated methods of reducing MEMS device damage and residue accumulation due to laser ablation during HDI/COF packaging.
- Developed procedures for using xenon difluoride (XeF_2) as a tool for post packaging release of bulk micromachined MEMS.

Modeling and simulation of MEMS:

- Developed electrothermal SPICE model for polysilicon thermal actuators.

- Conducted experiments to produce first estimates of the thermal conductivity and thermal coefficient of resistivity of the intermediate polysilicon layer in the multiple-user MEMS processes (MUMPs).

- Generated a TSUPREM model of the MUMPs fabrication process which was used to characterize process parameters and explain resistivity variations.

Development of microsystems:

- Created and validated new average power control strategy for thermally actuated devices based on pulse modulation of control signals.

- Designed and demonstrated automated assembly of MEMS using CMOS controllers for flip-up structures.

1.3 Organization of Dissertation

This dissertation is organized into nine chapters and a set of appendices. Chapter 1 is an overview of the research objectives and accomplishments. Chapter 2 is a primer on micro-electro-mechanical systems and discusses the main classes of MEMS fabrication. Chapter 3 contains a more focused discussion on MEMS devices developed or used during the course of this research effort. Chapter 4 describes the theory and implementation of electrothermal SPICE models for thermal actuators. Chapter 5 includes MEMS fabrication modeling work conducted to support the SPICE model and gain a better understanding of polysilicon resistance properties. The TSUPREM model of the MUMPs process is presented in this chapter and was particularly useful.

After chapter 5, the perspective broadens to functional and physical integration of MEMS with CMOS. Chapter 6 discusses the research efforts on microsystem development including the creation of the average power control scheme for thermally actuated MEMS and the CMOS chips which were designed to demonstrate this new

control methodology. Automated assembly systems using thermal actuators and the CMOS control chips are also demonstrated.

Chapter 7 discusses the fundamentals of MCM packaging as well as inherent difficulties with MEMS/MCM packaging. Chapter 8 details the MEMS/MCM-D packaging work conducted in support of this dissertation which incorporates the joint effort with Dr. Patrick Chu from the University of California at Los Angeles (UCLA) on XeF_2 etching of MCM packaged MEMS. Chapter 9 contains the results of HDI and COF packaging of MEMS including the various processing steps developed for mitigating MEMS device damage due to laser induced heating and residue.

The conclusions and recommendations for future research are located in Chapter 10. Finally, the appendices contain listings of items such as software code and process procedures which were deemed too long to appear in the chapter text.

Chapter 2. Fundamentals of MEMS Fabrication

2.1 Background

Dr. Richard Feynman is credited with originating the concept of micro-electro-mechanical systems (MEMS) in a speech given in 1959 [3]. Dr. Feynman discussed the potential of several technologies which could be used for the development of microsystems and micromachines. The accuracy and prescience of Dr. Feynman's predictions on microfabrication and MEMS are remarkable.

Nonetheless, the field of MEMS was largely dormant until the late 1980's when researchers embraced the concept of leveraging the burgeoning integrated circuit fabrication industry for the construction of micromachines. As a result, current MEMS fabrication processes borrow heavily from the technology developed for the integrated circuit industry. However, the success of early micromachines, such as the single chip accelerometer shown in Figure 2-1, has led to an era of extensive research into MEMS-specific fabrication processes and materials.

There are numerous methods used to fabricate MEMS devices, and three prevalent classes of MEMS processing have matured to the stage where foundry services are available: bulk micromachining, surface micromachining, and electroplating. These processes are capable of producing unique and useful MEMS devices. Each process has unique characteristics which must be understood to make the best decision on how MEMS can be designed and employed. The following sections provide a review on these fundamental MEMS fabrication processes.

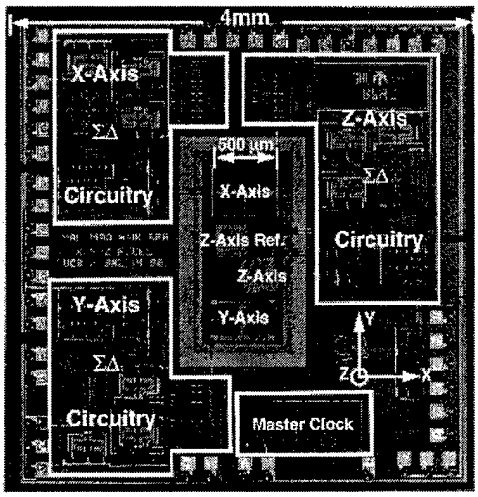


Figure 2-1. Surface micromachined, three-axis accelerometer [4]. Similar single axis devices are commonly used in airbag sensors due to their effectiveness and low cost [5].

2.2 Bulk Micromachining

In bulk micromachining, the micro devices are constructed by etching a single-crystal substrate to remove portions of bulk. The structural and mechanical features of the devices are determined by thin film masks patterned on the substrate and the differing etch rates in the various crystal planes. Bulk micromachining can be used to fabricate larger devices than are achievable with surface micromachining, but the bulk process is not as flexible for creating intricate and small features. Gallium arsenide and quartz have been used as substrates; but silicon is the most common substrate material used in bulk micromachining for solid state micro sensors and actuators. Silicon is preferred because high-purity material and mature fabrication techniques are readily available at low cost as a result of the microelectronics industry. Consequently, the following descriptions will focus on silicon bulk micromachining.

Miller indices are used to define crystal planes and provide a means to describe how anisotropic etchants can be used for bulk micromachining. The Miller indices for crystal planes are shown in Figure 2-2. Amorphous and polycrystalline materials used in microelectronic processing usually etch at the same rate in all directions. This type of etching is known as isotropic etching. Conversely, the various crystal planes in a single crystal silicon substrate can be etched at different rates by using specific chemical etchants, varying doping concentrations, temperature, or other environmental factors.

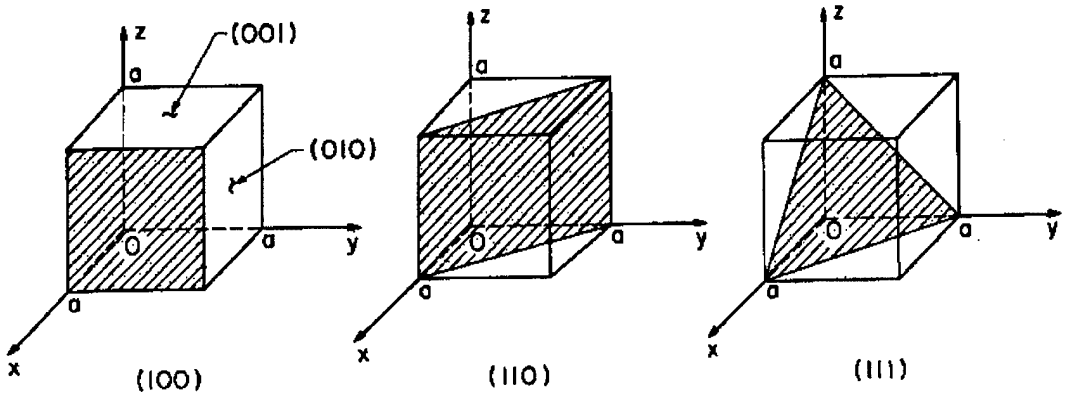


Figure 2-2. Miller indices for primary crystal planes [6].

The specific phenomena which causes the etch rate to be orientation dependent is not completely understood [7]. One theory is that the density of atoms in the various crystal planes affects the rate of the etchant chemical reaction. In crystal silicon, the <111> direction has the highest density of atoms while the <100> direction has the lowest density [6]. Most anisotropic etchants etch much faster in the <100> and <110> direction [6]. For example, one of the more common anisotropic etchants is Ethylene-Diamine Pyrochatecol (EDP) which etches the <100> plane 35 times faster than in the <111>

direction [7]. A figure of merit for anisotropic etchants is selectivity which is defined as the ratio of the etch rate in the desired direction to the etch rate in other directions. Some anisotropic etchants such as potassium hydroxide (KOH) have selectivities as high as 400 with respect to the <100> and <111> directions [7].

The ability to mask or control the progress of an etchant is a key to successful micromachining. One reason anisotropic etchants such as EDP and KOH are popular choices for bulk micromachining is that they have very low etch rates for silicon oxides and nitrides [6]. Consequently, these materials can be used as masks for defining the features of devices. In addition, high doping concentrations can also be used to control the progress of the etch. For example, a high P-type doping concentration will reduce the etch rate of EDP in silicon [7]. Reductions in the etch rate of over three orders of magnitude can be achieved by using a heavy P-type boron doping greater than 2.5 x 10^{19} cm^{-3} [8].

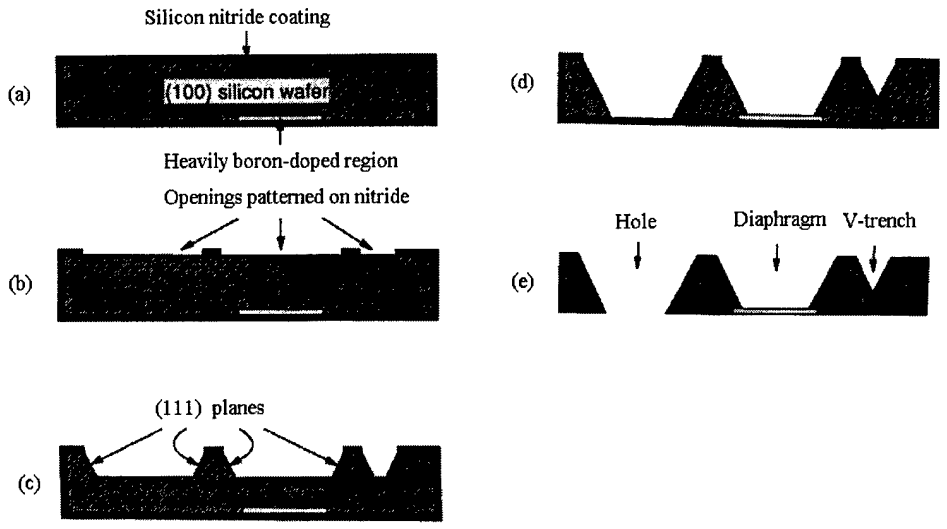


Figure 2-3. Bulk micromachining example [7].

The selectivity of anisotropic etchants and the ability to effectively mask areas exposed to the etch are tools which can be used for creating devices and structures in silicon. Figure 2-3 displays a representative progression of bulk etch processing steps used for creating device structures. In this example, silicon nitride is patterned and used as an etch mask. In Figure 2-3 (c), the substrate is anisotropically etched with the etch proceeding much faster in the <100> direction as compared to the <111>. As a result, sidewalls begin to develop along the <111> direction. In Figure 2-3 (d), the etch is stopped by penetrating all the way through the silicon substrate and hitting the nitride barrier, contacting the highly doped boron etch stop, or reaching the convergence of two <111> planes. Removing the nitride completes the construction of a hole, a thin silicon diaphragm, and a V-shaped trench. Hence, the use of anisotropic etchants in combination with masking and etch controlling techniques can be used to build three dimensional structures in bulk silicon.

Isotropic silicon etchants are also used for bulk micromachining. Isotropic etchants such as the ones shown in Table 2-1 are commonly employed. Xenon difluoride (XeF_2) and other gas phase silicon etchants are gaining popularity due to their high etch rates and selectivity. While isotropic etchants are useful in creating a wide array of microdevices, a potential disadvantage is the lack of an etch stop or method of controlling the etch progress. Fortunately, significant improvement has been made in controlling the etch progress by pulsing gas phase etchants and using reactive ion etching (RIE) to augment the etching process [9,10].

Table 2-1. Comparison of Various Etchants Used in Silicon Bulk Micromachining

Etchant	Type	Target Crystal Plane	Etch Rate (A/min)	
EDP	Wet anisotropic	<100>	10000	[7]
KOH	Wet anisotropic	<100>	7500	[7]
TMAH	Wet anisotropic	<100>	6000	[11]
$HNO_3 + H_2O + HF$	Wet isotropic	All	3000	[12]
XeF_2	Gas isotropic	All	4600	[12]
BrF_3	Gas isotropic	All	4000	[13]

One of the benefits of bulk micromachined devices is that they can be constructed in silicon microelectronic processes with little modification. The CMOS MEMS process is one of the first foundry services for producing MEMS devices [14]. This process is an extension of a basic CMOS process and uses bulk micromachining to create the MEMS structures [14].

EDP and KOH are the anisotropic silicon etchants most commonly used to release the devices in the CMOS MEMS process since silicon dioxide can act as a mask material. In standard CMOS processes, the entire die is encased in silicon dioxide both as an inter-layer dielectric and as a final layer to protect the top wiring level. The MEMS designer specifies which areas of the die are to be exposed to the etch by cutting through the protective oxide and dielectric layers, down to the silicon substrate. Additionally, areas for boron doping can be specified which will act as an etch stop [14]. These tools allow the designer to create a useful but limited set of MEMS devices as shown by the examples in Figure 2-4.

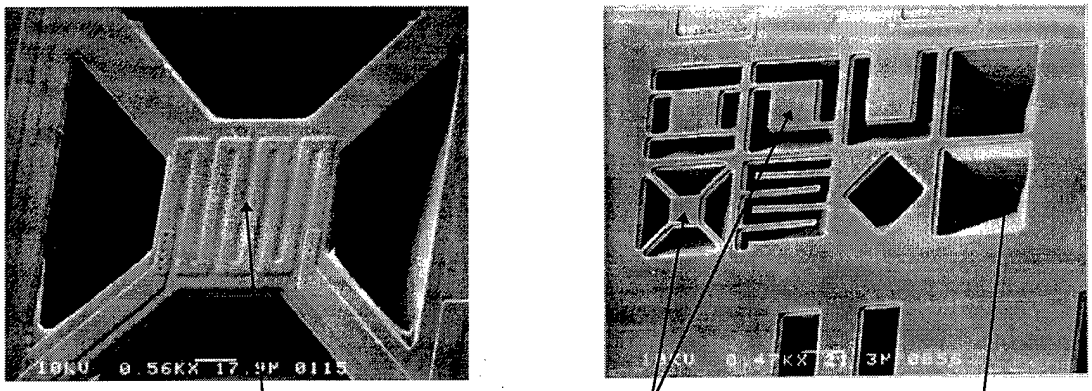


Figure 2-4. Examples of devices from CMOS MEMS process [15].

The CMOS MEMS process does allow for monolithic integration of MEMS and electronics, but the MEMS capability is compromised in order to make the process feasible. The MEMS devices constructed through the CMOS MEMS process are primarily static structures that benefit from electrical or thermal isolation from the substrate such as suspended heaters, thermal actuators, and cantilevers [15]. More mechanically complex MEMS devices are not realizable because they would require modification of the underlying CMOS process. Thus, the CMOS MEMS process highlights the tradeoffs which are often necessary in order to fabricate MEMS and electronics in one process.

2.3 Surface Micromachining Processes

Surface micromachining employs many of the processes used to form microelectronic circuits. In silicon surface micromachining, thin films of materials such as polysilicon, silicon nitride, and silicon oxide are deposited on a substrate and then

patterned using standard microelectronic thin film deposition, photolithography, and etching techniques. One of the unique features of surface micromachining is the concept and use of sacrificial layers. Structural layers are separated by 'sacrificial' layers which can be removed by a 'release etch' after all of the layers are deposited. After the release etch, the patterned structural layers are left suspended in space or free to move since they are no longer encased in the sacrificial layers.

The use of integrated circuit processing techniques affects the general appearance of surface micromachined devices. Surface micromachined devices tend to be flat with a depth of only a few microns but can have much greater widths giving them a two-dimensional aspect analogous to the layout of a VLSI circuit. Also, surface micromachined devices can be designed to the same scale as integrated circuits due to the use of the same photolithography and etching techniques. This makes surface micromachining an attractive MEMS fabrication process for integration with electronics.

A simple visualization of the silicon surface micromachining process is shown in Figure 2-5. In Figure 2-5, an electrical isolation layer such as silicon nitride is deposited on a silicon substrate, and a sacrificial layer of material is then deposited and patterned. Next, a structural material such as polysilicon is deposited and patterned. A final release etch is then performed to remove the exposed sacrificial layer. Removing the sacrificial layer leaves a polysilicon cantilever structure which can be used for a variety of mechanical applications. The use of multiple structural and sacrificial layers allows for the construction of increasingly more complex devices.

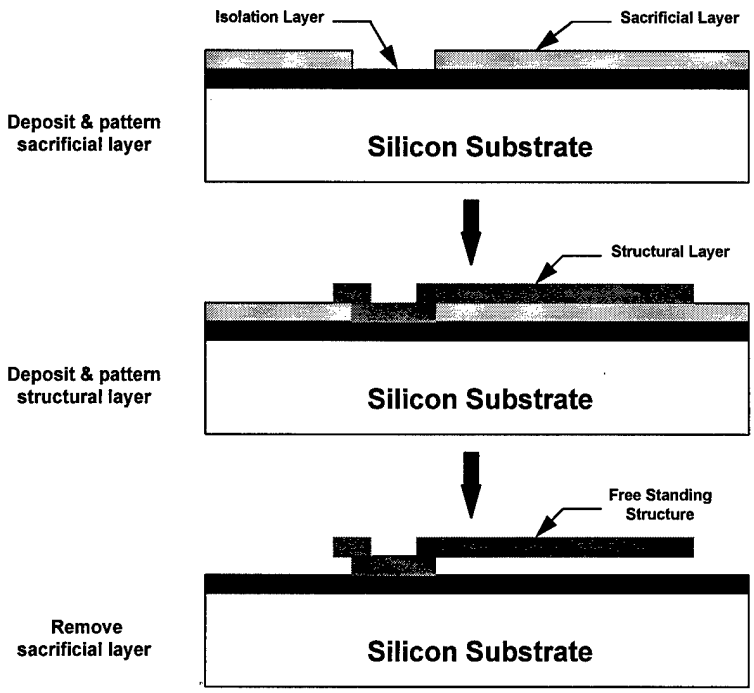


Figure 2-5. Surface micromachining process.

There are many combinations of substrate, structural, and sacrificial layers which can be successfully employed for surface micromachining. Some of the key considerations for which materials to use are the existence and availability of compatible masking and etching materials, the interaction between the processing for each layer, structural and electrical properties of the materials, and the target application. There are several foundry and private surface micromachining processes which vary in terms of the types of materials used, the number of structural and sacrificial layers, and the availability of low-impedance wiring.

Some of the more common choices for layers include polysilicon, silicon nitride, and silicon oxide. Quite often, the choice of material for the structural or sacrificial layers dictates the materials used for other layers. For example, silicon oxide is often

chosen as a sacrificial layer because of the existence of highly selective and efficient etchants, the ability to deposit oxide on a variety of other silicon based materials, and the industrial support base from the microelectronics industry [7]. Consequently, polysilicon is often chosen as the structural material because it has many desirable features as a structural material and is an excellent complement to silicon oxide. Table 2-2 lists some of the more commonly used structural and sacrificial layer pairings for surface micromachining.

Table 2-2. Commonly Used Structural and Sacrificial Material Pairings [16].

Structural Layer	Typical Thickness (μm)	Sacrificial Layer	Thickness (μm)
Polysilicon	1 - 4	PSG, SiO_2	1 - 7
Si_3N_4	0.2 - 2	PSG, SiO_2	2
SiO_2	1 - 3	Polysilicon	1 - 3
Polyimide	10	Aluminum	1.5 - 3

One problem with using polysilicon as a structural layer is an unwanted buildup of residual stress within the polysilicon layers. The most common method of depositing polysilicon is through Low-Pressure Chemical Vapor Deposition (LPCVD). The LPCVD process deposits layers of polysilicon with high residual stress. This results in curling and deformation of MEMS devices after release as shown in Figure 2-6.

The most prevalent technique used to mitigate stress in polysilicon is thermal annealing. For thermal annealing, the die is raised to a high temperature (~ 1000 °C) which allows the polysilicon grains to realign in a manner which reduces internal stress. The stress reduction is even greater when the polysilicon is heavily doped. Consequently, the polysilicon is often doped directly and indirectly through diffusion by intentionally

doping the surrounding silicon oxide sacrificial layers with phosphorous [7]. Phosphorous has a greater affinity for silicon than silicon oxide and readily diffuses into the polysilicon during the annealing process [6].

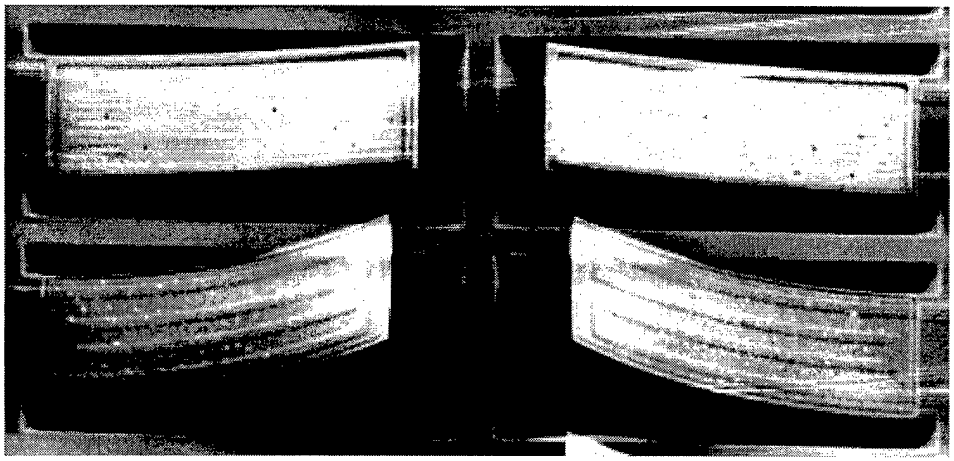


Figure 2-6. Curling of bulk micromachined cantilevers due to residual stress [15].

The first widely available surface micromachining foundry is the Multi-User MEMS Processes (MUMPs). The MUMPs process is a Defense Advanced Research Projects Agency (DARPA) supported program that provides a low cost surface micromachining foundry service to encourage prototype and proof-of-concept work. It is designed to be a general purpose, high yield service and is not optimized for any specific application [17]. Most of the design work performed at AFIT has been accomplished through the MUMPs foundry service.

The MUMPs process has three structural layers of polysilicon which are separated by sacrificial layers of silicon oxide. The substrate is electronically isolated from the polysilicon layers by a silicon nitride barrier. The top layer of the process is a metal layer

which is provided to facilitate low-impedance wiring of the MEMS devices [17]. Table 2-3 lists nominal thicknesses of the various layers, and Figure 2-7 shows a cross-sectional view of a notional MUMPs design.

Table 2-3. MUMPs Layer Names and Thickness [17].

Layer	Thickness (μm)
Gold	0.5
Poly 2	1.5
2nd Oxide	0.75
Poly 1	2.0
1st Oxide	2.0
Poly 0	0.5
Nitride	0.6

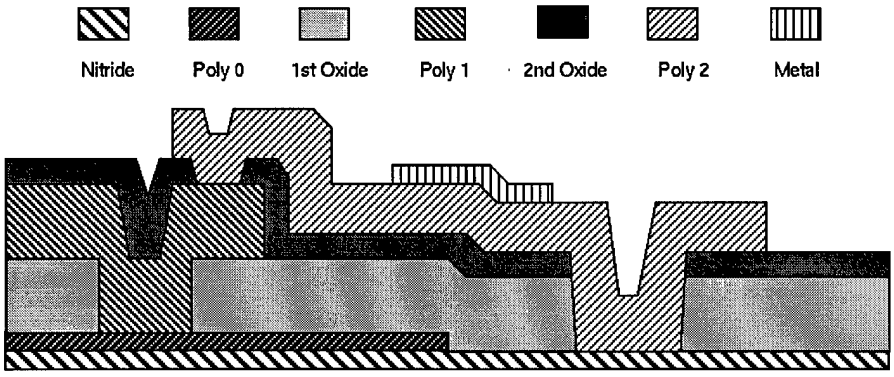
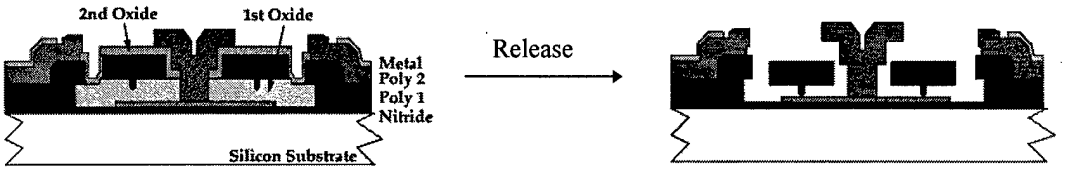


Figure 2-7. Cross-sectional view of notional MUMPs device [17].

The MUMPs process starts with a (100) silicon wafer on which a thin nitride layer is deposited to provide electrical isolation from the polysilicon layers. Next, the first polysilicon layer, '*Poly 0*', is deposited and patterned using photolithography and Reactive Ion Etching (RIE). RIE is a dry etching technique where the material to be removed is bombarded by a stream of high energy ions in a reactive plasma or gas. The

force of the ions impacting the material dislodges atoms which then combine with the reactive ions and are carried away from the surface. RIE is able to etch the target material with little undercutting of the photomask [6]. This allows for the creation of MEMS which have flat and predictable sidewalls. After the *Poly 0* is patterned, the first sacrificial oxide is deposited. This process is repeated for the second polysilicon layer, '*Poly 1*', and the second oxide. The final two layers, *Poly 2* and metal (*Gold*), are then processed. Figure 2-8 (a) shows a cross sectional view of a rotor structure before the final release etch.



(a) (b)

Figure 2-8. Side view of (a) unreleased and (b) released rotor [17].

After each of the polysilicon layers has been deposited, the entire structure is annealed at 1050 °C for one hour to remove residual stress in the polysilicon layers. This anneal also allows phosphorous to diffuse from the highly doped silicon oxide into the polysilicon. The wafers are then diced and sent to the customers where the final release etch is performed. The final release is normally accomplished by immersing the die in a 49% HF solution for two minutes at room temperature [17]. Figure 2-8 (b) shows the rotor structure after the sacrificial oxide layers have been removed by the HF release etch.

The Sandia Ultra-planar Multi-level MEMS Technology (SUMMiT) is a "second generation" surface micromachining foundry offered by Sandia National Laboratories.

This process has recently been extended to include five layers (four releasable) of structural polysilicon [18]. The 5 level polysilicon/oxide stack is shown in Figure 2-9 (a). It consists of 4 mechanical levels of polysilicon plus an electrical interconnect layer underneath. The polysilicon layers are separated by sacrificial layers of oxide that are etched away in HF/HCl after the entire stack is fabricated. The *Poly 1* and *Poly 2* layers can be stacked together to create three equal thickness layers as shown in Figure 2-9 (b).

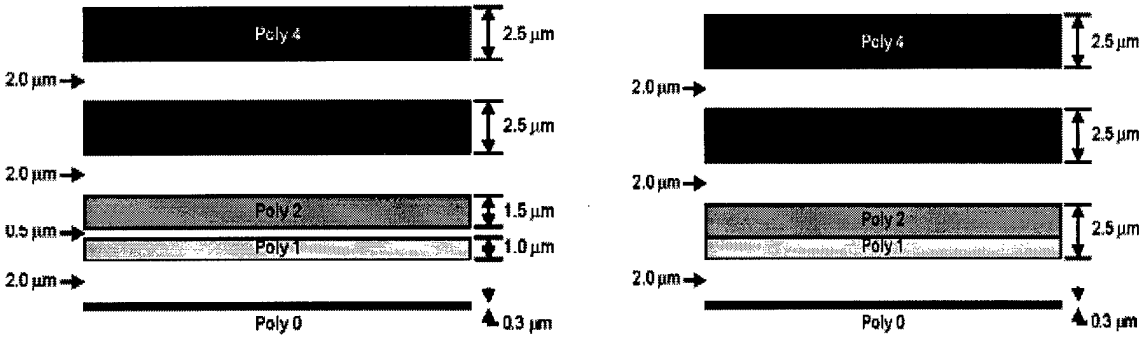
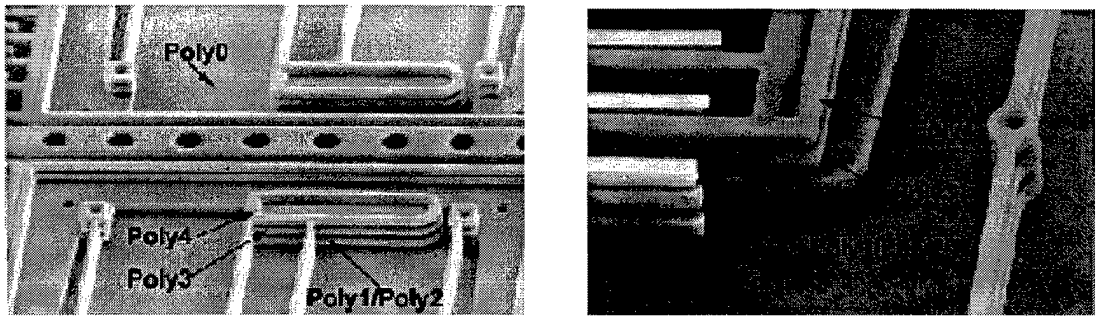


Figure 2-9. Polysilicon layer arrangement in Sandia SUMMiT Process [18].

One of the hallmarks of the SUMMiT process is that the *Poly 3* and *Poly 4* layers are planarized using a chemical mechanical process [19]. Planarization allows for greater control of the topology of the microsystem which is particularly important in optical applications and for devices which have moving parts. Figure 2-10 depicts two perspectives of an electrostatic comb drive fabricated in the SUMMiT process. The composite *Poly 1* and *Poly 2* layers are combined in this design and used for the lower mechanical level.



(a) (b)

Figure 2-10. Scanning electron micrograph (SEM) of (a) electrostatic comb drive fabricated in the Sandia SUMMiT process and (b) close up of gear teeth showing the various polysilicon levels [18].

One of the most intense areas of research in surface micromachining is in the development of processes which allow integration of MEMS and integrated circuits. The removal of all oxide layers in the MUMPs process makes monolithic integration with CMOS VLSI circuits a difficult if not impractical undertaking [20]. Additionally, the high temperature anneal can be harmful to the carefully controlled diffusion budgets of microelectronic circuits [20]. However, some processes, such as Sandia's Modular, Monolithic Micro-Electro-Mechanical Systems (M^3EMS) process, do allow monolithic integration of surface micromachined MEMS and electronics by fabricating the MEMS completely before the microelectronics [21].

In the Sandia M^3EMS process, shallow cavities (~ 6 - 12 μm) are etched into a silicon substrate as shown in Figure 2-11. Unreleased MEMS devices are then fabricated in the cavities and sealed with a silicon nitride cap. The surface of the wafer with embedded MEMS is planarized using a chemical-mechanical polishing technique. A

high-temperature anneal is performed to relieve the residual stress in the structural polysilicon layers.

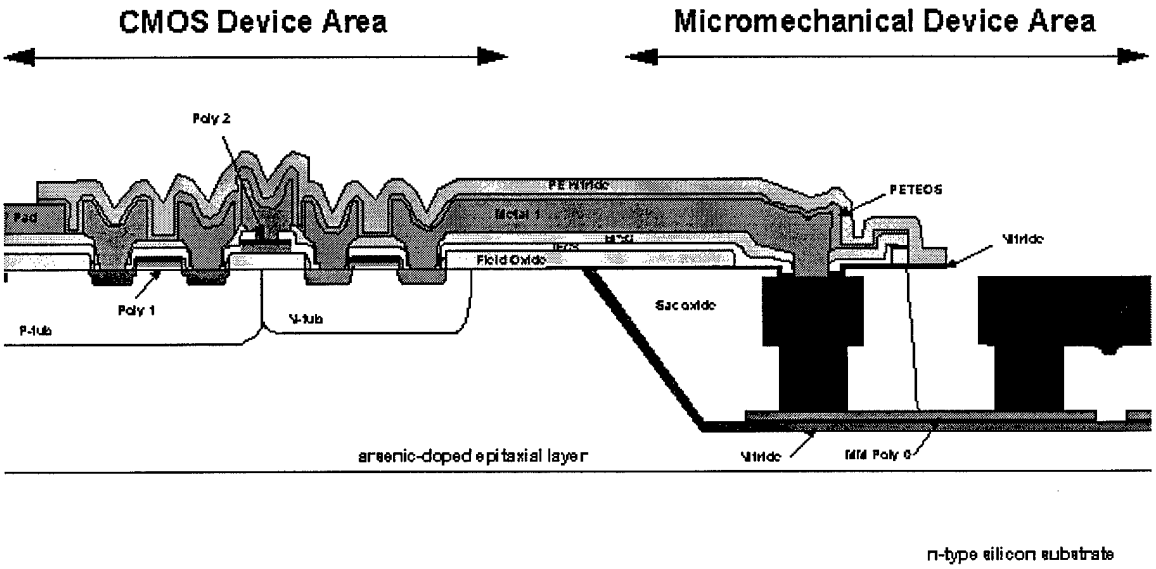


Figure 2-11. Cross-section of embedded MEMS approach to CMOS/MEMS integration [21].

After the anneal, these wafers are ready for use in a standard CMOS process without any modification to the wafer or the CMOS process, although a nitride layer over the CMOS circuitry is needed to protect the microelectronics from the final release. After CMOS processing, the final step is to open the nitride above the MEMS devices and perform the final release. During the final release process, the CMOS devices are protected by a nitride barrier, and the bond pads are protected with photoresist [21]. The three-axis accelerometer shown in Figure 2-1 was fabricated in the M^3EMS process.

2.4 Electroplating (LIGA)

Electroplating is micromachining process which uses three basic fabrication steps: lithography, electroplating, and molding to build micro devices. The most widely known electroplating process is the LIGA service which is a German acronym for the three fabrication processes: LIthographie, Galvanoformung, and Abformung (LIGA). One of the main advantages of electroplate micromachining is the ability to create structures as thick as bulk micromachined devices while retaining the design flexibility and small lithography feature sizes associated with surface micromachining. Depending on the process used, devices as thick as 500 μm are realizable [7].

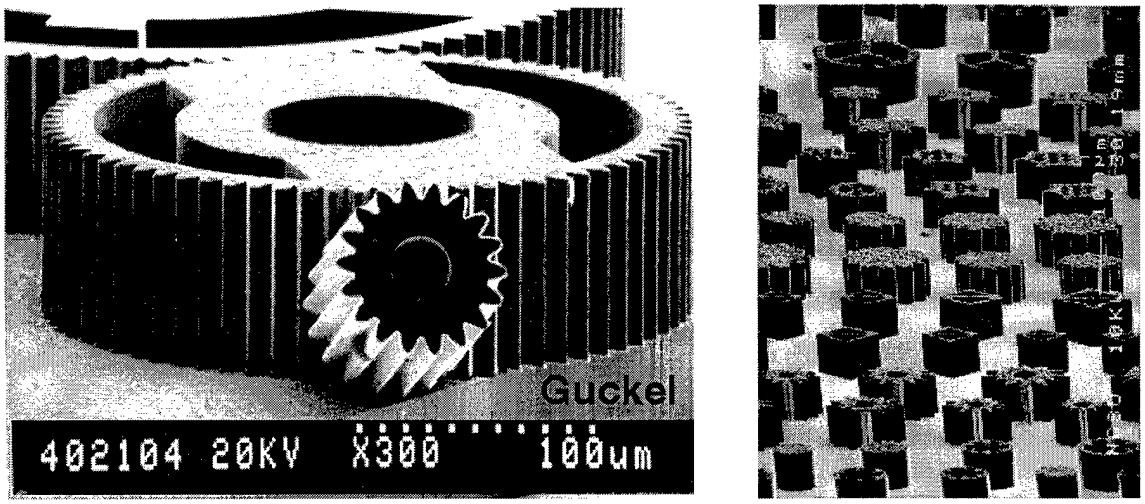


Figure 2-12. Gears fabricated in LIGA process at University of Wisconsin [22].

The LIGA process starts by patterning a thick photoresist (up to 500 μm) on a plating base. Since the photoresist is so thick, lithography is accomplished by using X-ray radiation from a synchrotron through an X-ray mask. Metal is then electroplated onto the exposed plating base. As the electroplating procedure continues, metal conforms to

the shape of the patterned photoresist. The photoresist is then removed which leaves a patterned metal structure which can be used as a micro device or as a mold for making more copies without going through the entire process again [7]. Figure 2-12 shows gears fabricated in the LIGA process at the University of Wisconsin.

One of the key disadvantages of the original LIGA process is the high cost and limited availability of the X-ray lithography process. Hence, LIGA-like processes have been developed which use ultraviolet (UV) light sources to pattern photosensitive polyimides. UV electroplating processes are able to create devices as thick as 40 μm which is much less than the X-ray LIGA process. Additionally, the smallest feature size is not as good as in the LIGA process. However, the cost of UV electroplating is significantly less than that of the LIGA process, and the equipment needed to perform the UV electroplating process is widely available [7].

Monolithic integration of LIGA and CMOS is complicated by the significant differences in the processing techniques. Moreover, LIGA or electroplated devices tend to be electrostatically operated and consequently require very high voltage levels which are incompatible with conventional digital CMOS electronics. However, LIGA devices may have other applications such as micro-relays which could be integrated with electronics [15].

One of the author's favorite LIGA micrographs is shown in Figure 2-13. The LIGA fabricated gear has an approximate diameter of 100 μm. The striking contrast between the size of the gear and the ant gives a pictorial description of the incredibly

small dimensions of the structures used in micromachining. This concept is quite often difficult to express in words.

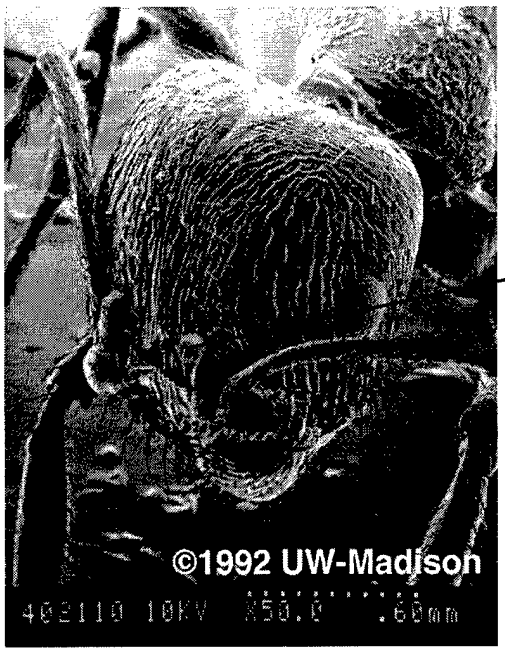


Figure 2-13. Micrograph of 100 μm diameter LIGA gear on the head of an ant [22].

2.5 Summary

Bulk, surface and LIGA micromachining processes have reached enough maturity that complex MEMS devices can be reliably and inexpensively fabricated. MEMS foundries have been established and are capable of at least prototyping and proof of concept research. At AFIT, the majority of MEMS device work is performed using the MUMPs surface micromachining process. This research will be discussed in the next chapter.

Chapter 3. MEMS Components and Systems

This chapter presents a concise overview of devices used or developed during the course of this research effort. Initially, the development and design of MEMS components was not expected to be in the purview this dissertation. However, the need to understand the properties and behavior of MEMS devices for modeling, packaging, and integration led to a significant amount of original MEMS-specific design work building upon existing structures.

The descriptions in this chapter will allow a better understanding of the material presented in subsequent chapters. Basic components such as hinges, latches, and wiring constructs are thoroughly described in [15,23] and will not be presented here. All of the devices in this chapter are surface micromachined devices fabricated through the MUMPs process. Both thermal and electrostatic devices are described. More complex systems which are composed of multiple components were also employed and are described in the sections 3.3 and 3.4.

3.1 Thermally Actuated Devices

One of the most recognized and popular devices created at AFIT is the polysilicon thermal actuator. Thermal actuators are capable of delivering relatively high force actuation without the need for the high voltages associated with other forms of microactuators [15].

3.1.1 Lateral Thermal Actuator and Arrays

Lateral thermal actuators use ohmic heating to generate thermal expansion and movement. Actuators fabricated in the MUMPs process are capable of providing deflections of greater than 10 microns while typically requiring drive voltages less than 5 volts. Figure 3-1 shows the basic lateral actuator design and lists the terminology used to describe the key components. Similar to a metal bimorph, the key to generating actuator deflection is to have one arm expand more than the other. Consequently, these actuators can take on a wide variety of geometries and can be fabricated in any MEMS process that has at least one releasable, current carrying layer. One of the benefits of constructing thermal actuators in the MUMPs process is that the polysilicon layers are highly doped. As a result, the actuators can be designed to operate at voltages and currents compatible with CMOS electronics. For example, a 230 μm long, 2 μm thick actuator with a 2.5 μm wide hot arm produced a force of greater than 7 μN and a deflection of greater than 16 μm when driven by a CMOS driver at 5 volts.

The actuators can be operated in two modes. In the basic mode, current is passed through the actuator from anchor to anchor, and the higher current density in the narrower 'hot' arm causes it to heat and expand more than the wider 'cold' arm. The arms are joined at the free end, which forces the actuator tip to move laterally in an arcing motion as shown in Figure 3-1.

Another mode of operation is to create a permanent deformation in the hot arm of the actuator. This can be accomplished by applying enough current to cause plastic deformation of the polysilicon. In general, the amount of current necessary to create a

permanent deformation is slightly higher than the current needed to generate the maximum tip deflection. When the current is removed, the actuator is left permanently back bent from its original position due to bowing or buckling of the hot arm. The amount of deformation or 'back bending' depends on the amount of over-current that is applied. After back bending, the actuator can be operated in the basic mode. Back bending is particularly useful for one time positioning of actuators and as a tool in self-assembly of complex devices [23-25].

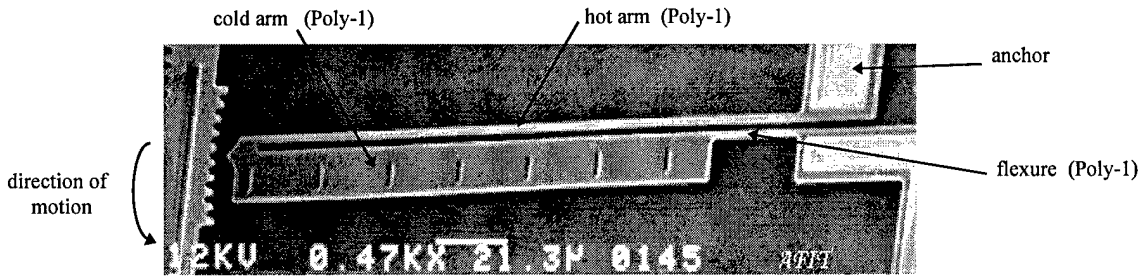


Figure 3-1. Basic design of the lateral thermal actuator. Typical dimensions of the hot arm, cold arm, and flexure (length/width/thickness) are 230/2.5/2, 180/16/2, and 50/2.5/2 μm.

3.1.1.1 Improved Lateral Thermal Actuators

An improved actuator design has been implemented based on the results of force and deflection testing. Reid and Comtois conducted extensive testing and analysis of the empirical relationships between actuator design and performance to establish a set of design guidelines [26]. One of the key conclusions identified in the optimization study was the need to make design tradeoffs between deflection and force. For example, increasing the length of the cold arm tends to increase the tip deflection but decreases the amount of delivered force. Conversely, decreasing the length of the cold arm tends to

increase delivered force but reduces the tip deflection. The thermal actuators and actuator arrays used previously were designed to maximize deflection. Consequently, the force generated by these thermal actuators was not optimal [26].

For the MUMPs process, the actuator design that optimizes power consumption, tip deflection, and delivered force has the dimensions listed in Figure 3-1. Testing accomplished by the author and Reid confirmed that the new actuator design was indeed superior to the original actuator. Table 3-1 compares the performance of the original thermal actuator and the improved actuator.

Table 3-1. Comparison of Original and Improved Thermal Actuator Performance.

Actuator	Hot arm l/w/t (μm)	Cold arm l/w/t (μm)	Flexure l/w/t (μm)	Volts (V)	Current (mA)	Power (mW)	Deflection (μm)	Force (μN)
Original	200/2/2	170/14/2	30/2/2	4.3	3.8	16.3	8	4.0
Improved	230/2.5/2	180/16/2	50/2.5/2	4.3	3.7	15.9	8	7.5

3.1.1.2 Improved Actuator Arrays

Arrays of thermal actuators are used in applications which require more force than a single actuator can provide or when linear motion is required. The yoke is a critical component in the design of an actuator array and combines the motion and force of the actuators into a linear deflection. Force testing of actuator arrays revealed that the yoke used in previous array designs was inefficient [26].

A new yoke design has been developed which significantly improves the performance of the actuator array. Figures 3-2 and 3-3 show versions of actuator arrays using the original yoke design and a new, more efficient yoke. When coupled with the improved actuators, the improved arrays are capable of delivering twice as much force as

the previous design. In addition, the improved thermal actuators and the improved yoke design were used to develop more efficient actuator arrays which were able to replace larger arrays of the original design. This more efficient array can thus reduce power and space requirements in some instances.

Further optimization of thermal actuators and arrays can be achieved by using a more advanced fabrication process. Comtois [27] designed and fabricated thermal actuator arrays using the Sandia Ultra-planar Multi-level MEMS Technology (SUMMiT) which are twice as efficient as the improved MUMPs actuator array shown in Figure 3-3. Comtois' new design employs mechanical features such as rotary-joints which can not be fabricated in MUMPs but are available in the SUMMiT process [27].

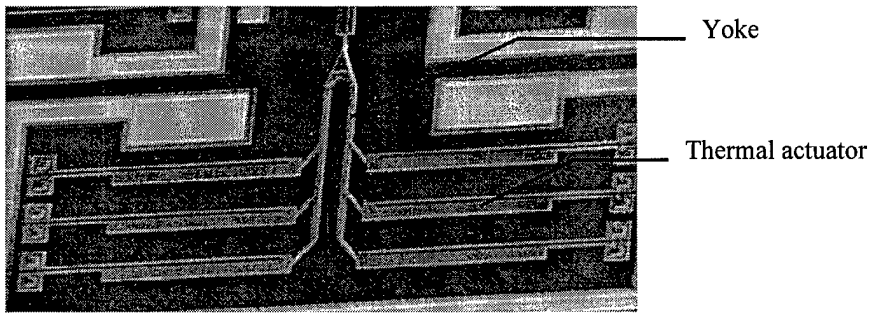


Figure 3-2. Original actuator array design.

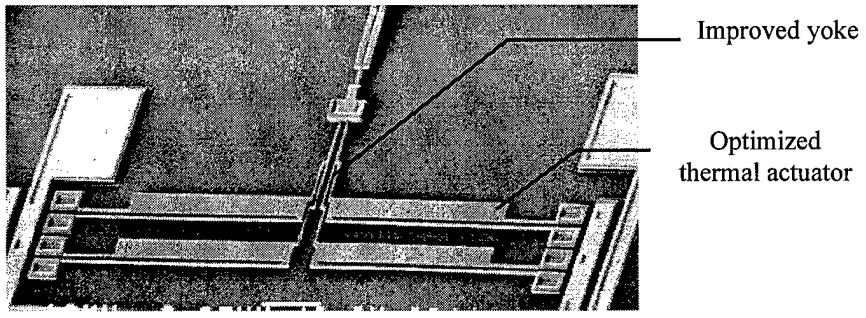


Figure 3-3. Improved actuator array using new yoke design and improved thermal actuators.

3.1.2 Vertical Thermal Actuators

Thermal actuators can also be designed to provide vertical deflection. Figure 3-4 shows a vertical thermal actuator. Similar to the lateral thermal actuator, the deflection of a vertical thermal actuator is generated by inducing thermal expansion as a result of ohmic (or resistive) heating. Vertical actuators can also assume a variety of designs.

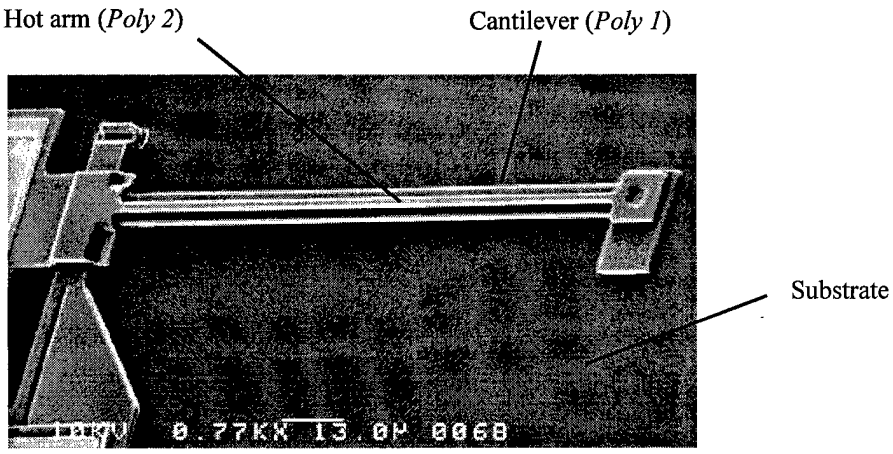


Figure 3-4. Vertical thermal actuator. The length/width/thickness of the *Poly 2* hot arm is 170/3/1.5 μm. The length/width/thickness of the *Poly 1* cantilever is 170/8/2 μm.

For the actuator shown in Figure 3-4, current is passed through *Poly 1* cantilever bar and the *Poly 2* hot arm. The *Poly 2* hot arm expands much more quickly than the *Poly 1* cantilever due to the smaller cross section of the hot arm and the higher resistivity of *Poly 2*. *Poly 2* structures of the same length and width are normally at least twice as resistive as similar sized *Poly 1* structures as a result of the fabrication process and smaller thickness. The rapid expansion of the hot arm forces the free end of the actuator to move down toward the substrate which allows ~ 1.25 μm of tip deflection.

The range of actuator motion can be significantly increased by back bending the vertical actuator prior to operational use. Back bending a vertical thermal actuator is accomplished by applying enough current to cause the actuator tip to drive into the substrate. Increasing the current causes the hot arm to bow upward. If enough current is applied to cause a plastic deformation, the hot arm will retain its bowed shape when the drive current is removed. The bowed hot arms cause the actuator tip to be permanently elevated above its as-fabricated position. Upward tip deflections in excess of 12 μm have been observed for 150 μm long actuators after back bending [24]. After back bending, the actuator can be operated with a greater range of downward deflection. Figure 3-5 shows a double hot arm vertical thermal actuator after back bending.

The back bending phenomenon of vertical thermal actuators has been observed to be a predictable and repeatable process [24,28]. In a controlled ambient environment using an automated back bending process, it is anticipated that positioning within +/- 50 nm can be achieved for a nominal deflection of 10 μm [28]. The consistency of back bending allows vertical thermal actuators to be used as set-up tools in the automated assembly of complex MEMS devices as demonstrated in Chapter 9.

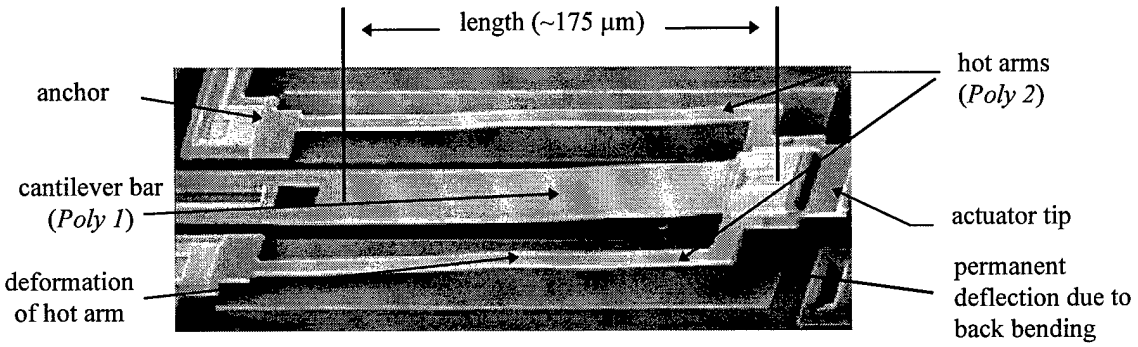


Figure 3-5. A double hot arm vertical thermal actuator. The actuator has been back bent by applying 13.5 volts with a current of 4.5 mA [28].

3.1.3 Thermal Piston Micromirror

Micromirrors are one of the key applications of MEMS. The ability to reconfigure the surface of a mirror is of great interest to the adaptive optics community, and micromachined mirrors appear to be well-suited for this application. Thermal actuators can also be used to control the deflection of a micromirror like the ones shown in Figure 3-6. The mirror plate is positioned by controlling the thermal expansion of the flexures when current is passed through the device. In this design, two of the flexures are connected in parallel to the power source. Current is then passed through the mirror plate and through two more flexures connected in parallel to ground. Use of four flexures and balanced thermal heating insures a pure piston deflection of the mirror surface. Mirror piston deflection of greater than 2 μm has been observed.

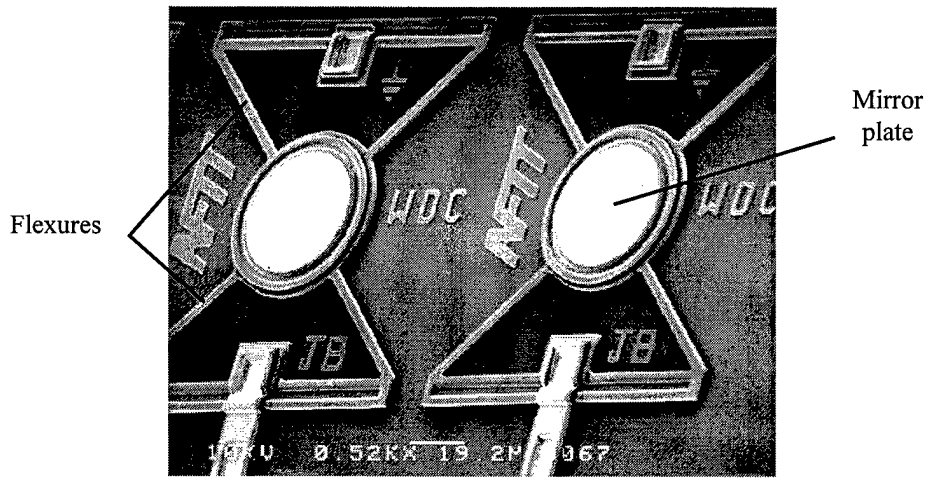


Figure 3-6. Thermal piston micromirrors. The length/width/thickness of the flexures are 64/4/2 μm. The mirror plate has a diameter of 70 μm.

One of the attractive features of the thermal piston micromirror is that it can generate large (~ 2 μm) deflections with low voltages. Moreover, the flexures can be

easily sized to allow the mirror to be directly compatible with digital drive circuits. The author and Cowan [29] have developed mirror designs which are designed for operation with the digital CMOS voltage of 3-5 volts. Figure 3-7 shows the deflection versus voltage for the micromirror shown in Figure 3-6.

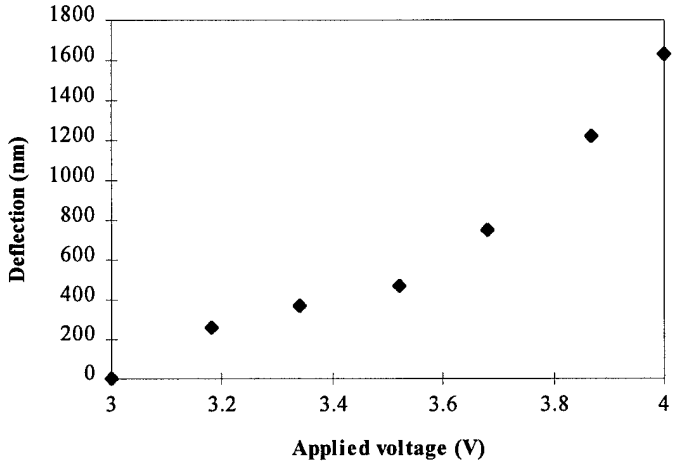


Figure 3-7. Deflection versus voltage for thermal piston micromirror shown in Figure 3-6. Buckling due to thermal expansion does not occur until 3 volts are applied, hence, there is no significant deflection below 3 volts.

3.2 Electrostatic Micromirrors

Electrostatic piston mirrors are another type of movable mirror investigated. These mirrors are designed to move up and down in response to an electrostatic potential placed between the mirror plate and another electrode below the plate. Electrostatically driven mirrors operate at higher frequency and use less power than other types of movable mirrors such as thermally actuated mirror described in the previous section. A hexagonal micromirror used in joint research between AFIT and the University of Dayton Research Institute is shown in Figure 3-8.

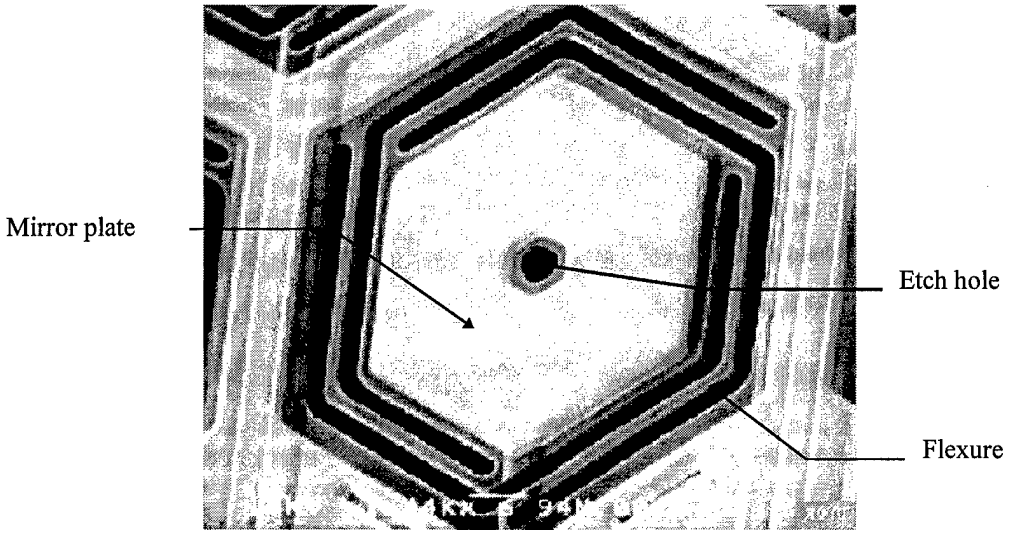


Figure 3-8. Scanning electron micrograph (SEM) of hexagonal micromirror [15]. The corner-to-corner diagonal across the mirror plate is 50 μm. Each of the three flexures has a length/width/thickness of 62/2/1.5 μm.

While electrostatic actuators use less power than thermal actuators, early designs of electrostatic mirrors, such as the one shown in Figure 3-8, required in excess of 25 volts in order to move the mirror through the complete range of motion [15]. However, lessons learned from previous mirrors and a maturing design methodology has led to the development of electrostatic piston mirror designs which will be more compatible with CMOS voltage levels. Several versions of low voltage (<10 V) electrostatic micromirrors were designed which are directly compatible with digital CMOS.

An analytical model used to calculate the applied voltage versus mirror displacement was developed at AFIT and can be used for designing micromirrors [30]. The model can be simplified by ignoring thermal and fringing effects from neighboring

mirrors and ignoring mirror deformation or sag due to gravity [30]. The simplified model is shown as [30]:

$$V = \left(z_0 - d_f\right)\sqrt{\frac{2kd_f}{\varepsilon_0 A}} \tag{3-1}$$

where V is the applied voltage, z_0 is the initial separation between the mirror plate and the address electrode, d_f is the desired downward displacement, ε_0 is the free space dielectric constant, and A is the micromirror plate area. The k term is a total spring constant which accounts for the number, geometry, and material of the mirror flexures [30]:

$$k = N\left(k_{cs} + k_s\right) = N\left[\frac{Ewt^3}{L^3} + \frac{\sigma(1-\nu)wt}{2L}\right] \tag{3-2}$$

where N is the number of flexures, and k_{cs} is a cross-sectional spring constant. L, w, t, and E are the length, width, thickness, and modulus of elasticity of the flexures. Finally, k_s is a stress term which accounts for the residual material stress, σ, and Poisson ratio, ν, of the flexure material. If the downward displacement of the mirror plate exceeds 1/3 of z_0, the mirror will typically snap all the way down to the surface. In some applications, the mirror can be operated in a binary mode by applying enough voltage to force the mirror all the way down to the substrate.

3.2.1 Low-voltage piston mirrors

Equations (1) and (2) provide insight into designing micro mirrors which operate at low voltage. Using a large mirror plate and minimizing the distance between the mirror plate and the address electrode are effective techniques for minimizing the needed

voltage. Additionally, minimizing the total spring constant, k, also serves to reduce the necessary applied voltage. The total spring constant can be reduced by using as few flexures as possible, increasing the length of the flexures, and minimizing the cross section of the flexures.

Figure 3-9 shows an example of an electrostatic piston micromirror designed to operate at low voltages. The mirror has only two, long flexures. Each flexure is 3 μm wide and 220 μm long and runs along two sides of the mirror. In addition, each side of the mirror plate is 100 μm which makes for a relatively large surface area of 1×10^4 μm^2.

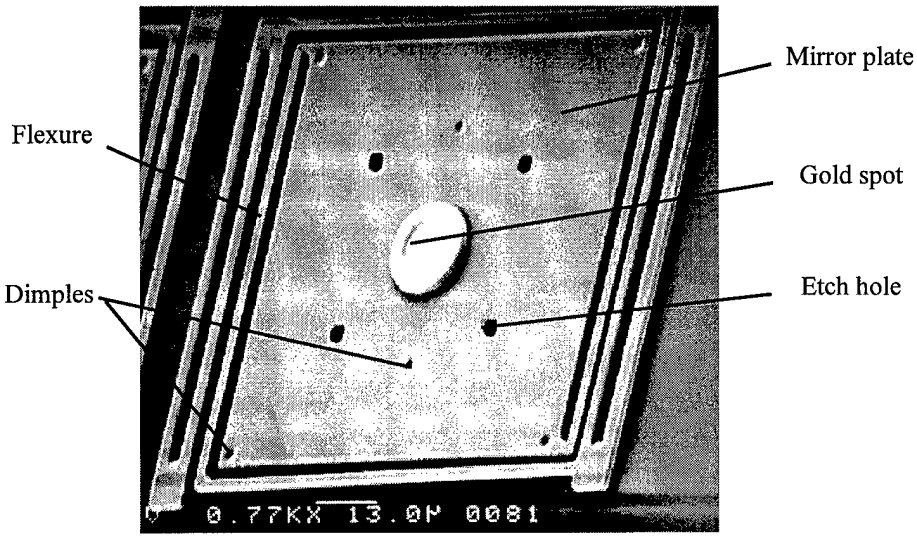


Figure 3-9. Low-voltage micromirror. The length/width/thickness of the flexures is 220/3/2 μm. Each side of the mirror plate is 100 μm. The dimples help to prevent stiction.

The main tradeoff to using these operating voltage lowering techniques is the device yield. For example, the low-voltage mirror shown in Figure 3-9 is capable of being driven through "snap-down" with a voltage of less than 5 volts. However, the yield after release is less than twenty percent because the flexures are not able to support the

weight of the large mirror. The mirror plate still sags even when the flexure width is increased to 5 μm.

A much more viable low voltage electrostatic mirror design is shown in Figure 3-10. These mirrors are smaller and more stable and provide a much better yield while still providing a low operating voltage. Like the previous design, these mirrors have only two flexures, but the length is reduced to 88 μm and the flexure only runs along one side of the mirror. The flexure width is reduced to 2 μm to partially counteract the impact of the reduced flexure length.

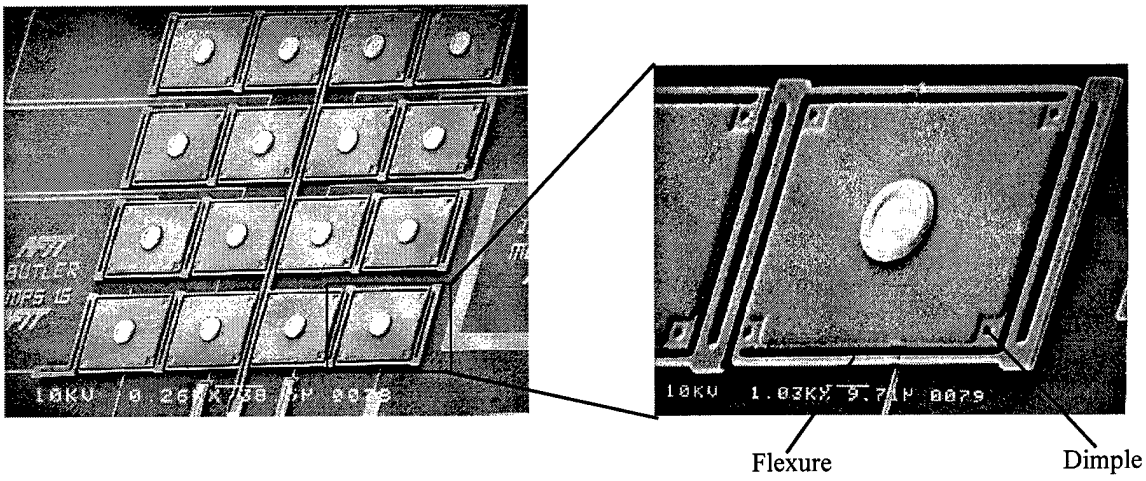


Figure 3-10. Improved binary, low voltage mirror design. The flexure length/width/thickness is 88/2/2 μm. The mirror plate is an 82 x 64 μm rectangle. The gold spot has a diameter of 20 μm. (MUMPs 16)

Furthermore, the surface area of the plate is only 5.2 x 10^3 μm^2 which is slightly more than half the area of the previous design. The smaller surface area increases the operating voltage but greatly increases the yield since the flexures are more able to support the smaller mass. These mirrors have a maximum operating voltage of 7 volts

and do not sag even with a flexure width of only 2 μm. Moreover, all 16 of the mirrors in the array shown in Figure 3-10 fabricated properly. The yield for these devices was greater than 80 percent (158 good out of 192) for a random sampling of released devices. If the flexure width is increased to 3 μm, the voltage rises to 8-9 volts but the yield improved to over 90 percent (111 good out of 120).

3.3 Complex Systems

Complex MEMS designs can be produced by combining different types of individual components or subsystems. The synergy achieved by properly using thermal actuator and arrays in combination with other devices such as flip up mirrors and rotating bases allows for the creation of simple and effective systems. Among such systems investigated are the scanning micromirror, the stepper motor, and the flip-up, rotating mirror.

3.3.1 Scanning Micromirror

The scanning micromirror used in this research is a derivative of a previous design by Reid [31] with the incorporation of the improved actuator array. The scanning micromirror has three main elements: an actuator array, a locking tether, and a flip-up mirror. A scanning micromirror using an improved 4 element array is shown in Figure 3-11. The position of the mirror plate is scanned up to 20 degrees by actuating the thermal array. The improved efficiency of the optimized array allows for a reduction in the number of actuators needed for operation. Previous designs used a minimum of 6 actuators [23]. Versions of the new mirror design have been built and operated which

only require a 2 element actuator array, although at least 4 elements are needed to provide performance equivalent to the original 6 element design.

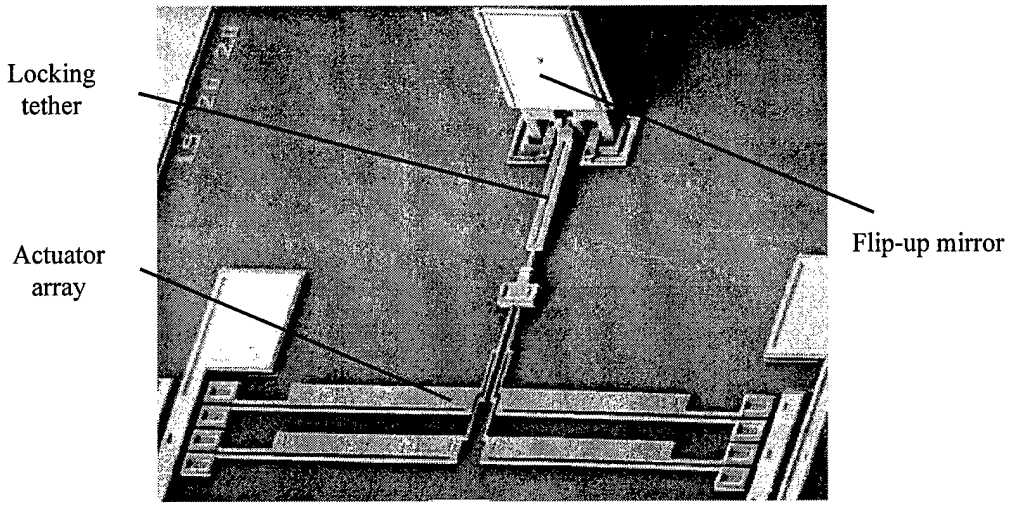


Figure 3-11. Scanning micromirror system. (MUMPs 15)

The locking tether is 15 μm wide and 100 μm long. The tether is connected to the actuator yoke by a 3 μm wide, 15 μm long flexure. At the other end of the tether, a self-engaging locking mechanism is used to secure the mirror. When the mirror plate is lifted off the substrate, the grooves in the tether fall into the small hole in the base of the mirror plate. The mirror is fabricated using a combination of both releasable layers of polysilicon. Gold is added to the surface of the mirror plate to provide optical reflection. The use of both polysilicon layers provides a stiffer mirror surface and thus reduces the curvature of the mirror surface due to residual internal stresses in the deposited polysilicon and gold. The gold coated mirror surface is a square with 75 μm sides. A 3 μm square etch hole is cut in the center of the mirror to ensure that the mirror is

completely released during the etching process. The mirror is connected to the substrate using two substrate hinges.

The performance of a scanning mirror driven by the improved 4 element array is shown in Figure 3-12. There is little deflection below 1 volt because the current flow is not sufficient to cause expansion in the thermal actuators. Above 4 volts, the mirror deflection is limited by mechanical interference in the design of the micromirror. The actuator array was effective in relative positioning of the scanning mirror in the sense that the mirror plate deflection would increase or decrease as commanded. While the positioning of the actuator array was consistent, the tolerances in the design of the micromirror hinges allowed too much play in the movement of the mirror plate. Consequently, the positioning of the plate was not as precise as desired as demonstrated by the RMS error bars in Figure 3-12.

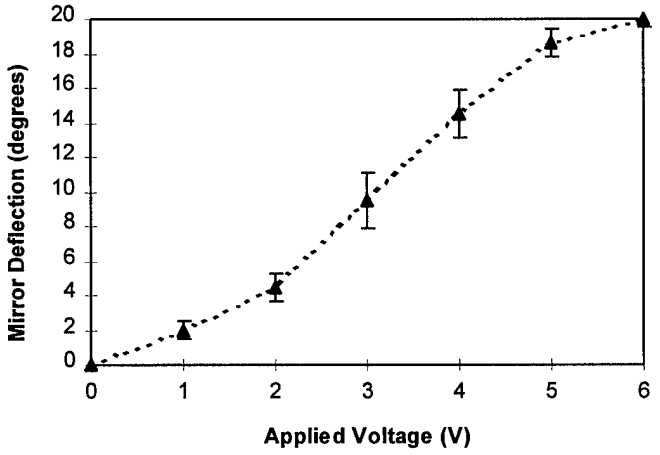


Figure 3-12. Mirror deflection versus applied voltage for scanning micromirror using 4 element drive array. Error bars represent RMS of measured data. Maximum power dissipation at 6 volts was 90 mW.

Several applications exist for the scanning micromirror. A device of very similar design was recently demonstrated as an optical scanner [32,33]. This device can also be used in an optical corner cube reflector or optical coupler [34]. This device could also be used as a component in a micro-optical bench [35].

3.3.2 Stepper Motors

Lateral actuator arrays can also be used in pairs to create micromotors [15,23]. A representative stepper motor is shown in Figure 3-13. In this example the stepper motor is used to drive a rotating wheel, and the wheel is, in turn, used to drive the linear bar. The two actuator arrays work together to rotate the wheel. The drive array is used to turn the wheel while the push array is used to ensure that the drive pawl stays engaged with the teeth etched into the side of the wheel. The sequencing of the drive and push arrays controls the direction of motion.

One of the unique and desirable features of this motor design is that no back bending is required prior to operation. Previous designs of stepper motors typically required back bending of either or both of the drive and push arrays. In this example, all of the actuator arrays are designed to operate as fabricated. The main advantage of this feature is the elimination of the back bending step which can be troublesome in this application.

Furthermore, the use of improved actuator arrays and small gear teeth allow for the operating voltage of the motors to be reduced compared to previous designs. The improved power of the improved actuator arrays allows for the wheel to be rotated at 5.5

volts. The use of small gear teeth allows for the drive array and the push array to be operated at the same voltage. The use of small gear teeth minimizes the distance the drive array must rotate the wheel on each step. This then reduces the amount of deflection and drive voltage needed for the drive array. Both arrays are able to accomplish their function at 5.5 volts although the drive array does require more current (~35 mA) than the push array (~16 mA).

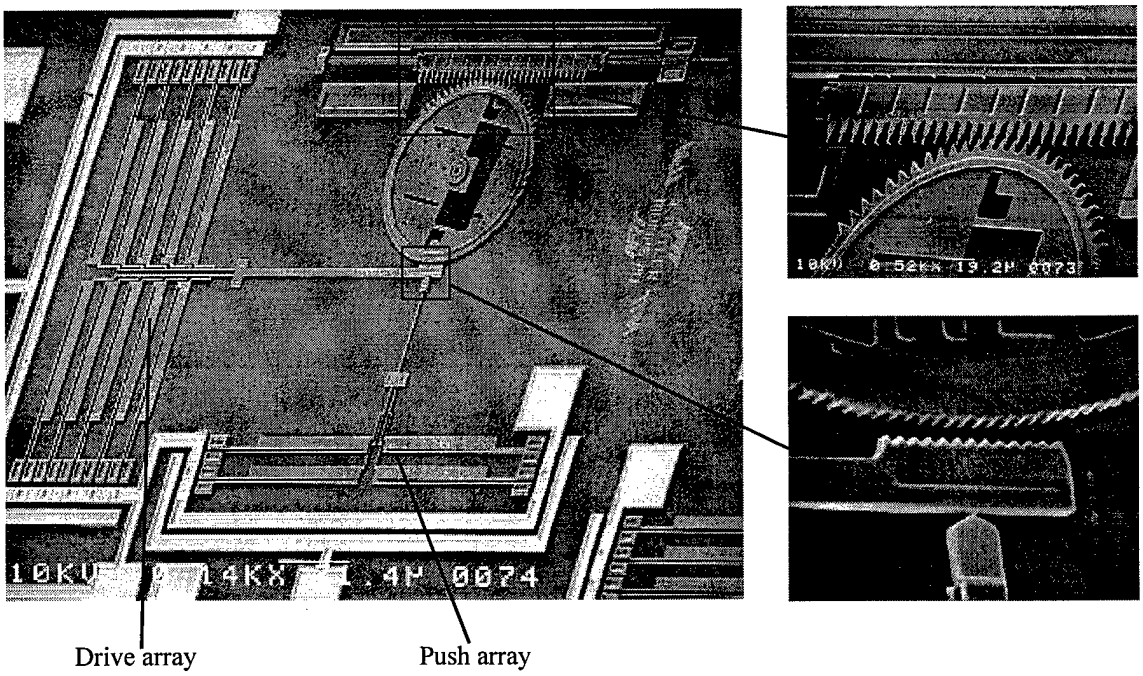


Figure 3-13. Stepper motor geared to linear bar. (MUMPs 20)

3.3.3 Flip-Up Rotating Micromirror

The flip-up, rotating mirror is also a derivative of a previous design [36]. The new rotating mirror system uses improved actuator arrays, a smaller mirror plate, and a smaller rotating base. Figure 3-14 shows the entire mirror system. Previous designs of

the rotating mirror did not operate consistently due to the use of unoptimized drive arrays which were not able to move the large rotating base [23]. The new actuator arrays are able to effectively rotate the smaller mirror and base. Moreover, the elimination of the need for back bending greatly simplifies the setup of the motor system. The smaller mirror plate is 100 μm square and the rotating base has a diameter of 220 μm. The mirror plate is constructed of two, stacked polysilicon layers (3.5 μm total thickness) and coated with 0.5 μm of gold for improved reflectivity.

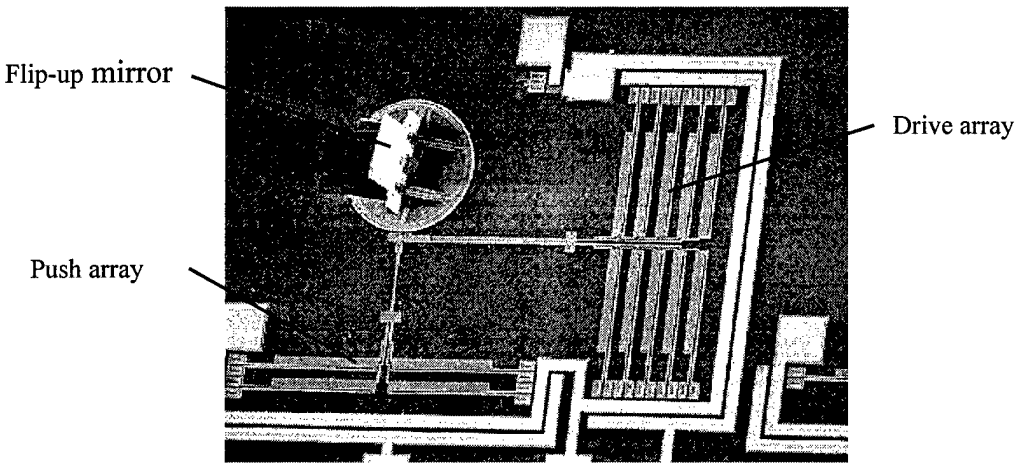


Figure 3-14. Flip-up, rotating micromirror system. (MUMPs 16)

The mirror plate is lifted off the substrate using microprobes and locks into a vertical position as shown in Figure 3-15. Once the mirror is locked into the upright position, a micromotor consisting of two actuator arrays is used to rotate and position the mirror. Teeth are etched into the edge of the rotating base and interface with the drive pawl from the micromotor.

The mirror is able to rotate through a range of approximately 210 degrees. The micromotor can move the mirror through the entire 210 degree range in 200 steps. This results in a positioning resolution of slightly greater than 1 degree. The error increases if the actuator arrays are overdriven and back bend out of position or if the input power fluctuates enough to alter the deflection of the arrays so that the step size varies.

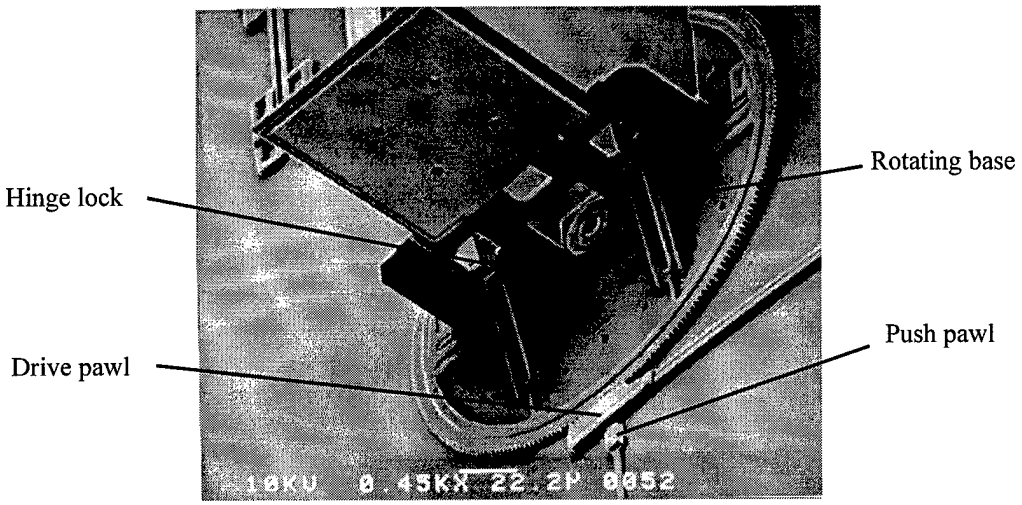


Figure 3-15. Close-up view of rotating base and flip-up mirror. (MUMPs 16)

3.4 Automated Assembly of MEMS

One of the obstacles to widespread use of flip-up structures is the need for assembly prior to operation. The assembly of flip-up structures has traditionally been performed manually which is a tedious and time-consuming process. Hence, there is great interest in automating the assembly of MEMS. The automated assembly of MEMS eliminates the need for manual assembly or adjustment, thus making batch fabrication feasible. Moreover, the automated assembly of MEMS will be particularly important for

applications which require reliable deployment and remote assembly of delicate structures in the operating environment or readjustment of components to align a system for optimum performance.

The first automated assembly system for flip-up micromirrors was developed by Comtois [37] with subsequent augmentation by Reid [38]. The development of this system has been continued by applying it to new devices and using novel assembly techniques. Figure 3-16 shows Reid's automated assembly system connected to a scanning micromirror. The system consists of three separate parts: a linear assembly motor (Figure 3-16a-c), a vertical actuator (Figure 3-16d), and a microlatch (Figure 3-16e). A lift arm is connected to the drive rod of the linear assembly motor with a hinge. The other end of the lift arm is connected to the flip-up plate.

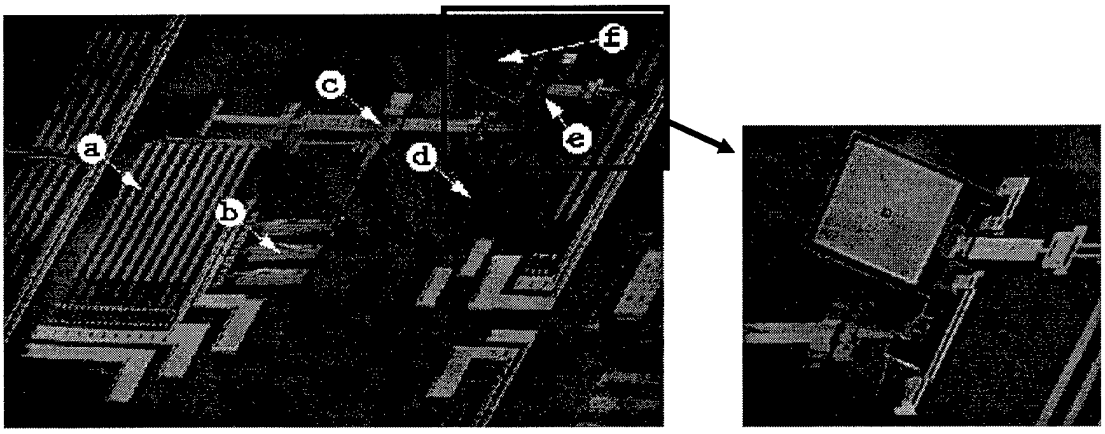


Figure 3-16. An automated assembly system connected to a scanning micromirror [38]. The system consists of three distinct parts: a linear assembly motor consisting of a drive actuator array (a), coupling actuator array (b), and drive arm (c); a vertical actuator (d); and a microlatch (e). The system is connected to a scanning micromirror (f).

First, the vertical actuator is used to lift the free end of the flip-up plate off the substrate, forming a triangle with the substrate, the lift arm, and the flip-up plate. The linear assembly motor then drives the lift arm towards the base of the flip-up plate, thus rotating the flip-up plate around its substrate hinges. Finally, the microlatch engages to hold the flip-up plate in position (Figure 3-15 inset). If necessary, the linear assembly motor can be reversed to pull the lift arm away from the assembled structure.

The coupling array of the linear motor used in the automated assembly system requires back bending prior to operation. The coupling array must be back bent to force the drive array to engage with the drive arm. Back bending of the coupling array is accomplished by applying a voltage of 7.8 V and a current of 3 mA until the required plastic deformation is achieved. After back bending, the linear motor is driven by properly sequencing the drive and coupling actuator arrays.

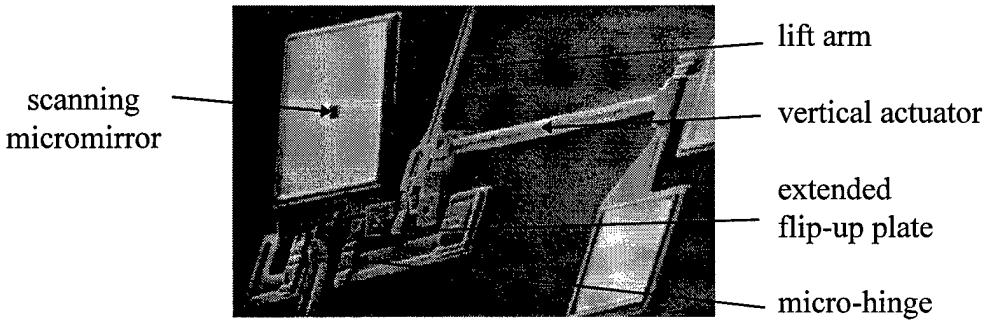


Figure 3-17. A small polysilicon plate is extended from the base of the scanning micromirror. This plate provides a place to connect the automated assembly system. The plate does not affect the scanning performance of the mirror [28].

Figure 3-17 shows a more detailed view of how the automated assembly system is connected to the scanning micromirror. The micromirror plate is formed by a 75 μm

square gold layer on top of a 3.5 μm thick, 79 μm square stacked polysilicon layer. A *Poly 1* layer extends below the mirror and is connected to the substrate with substrate hinges. To accommodate the automated assembly system, a *Poly 1* plate is extended from the base of the mirror as shown in Figure 3-17. The extended plate provides a lever for connection to the automated assembly system.

The automated assembly system is extremely versatile and has been adapted for use with different flip-up structures including an alignment mirror and a rotating mirror.

3.4.1 Automated Assembly of Alignment Mirror

The automated assembly system was applied to an alignment mirror as shown in Figure 3-18. The alignment mirror is one of the simplest types of flip up mirrors. It consists of a mirror plate and a support plate. The mirror plate is formed with a 104 μm high by 108 μm wide polysilicon plate. An area of 88 μm high by 92 μm wide is coated with gold to form the mirror surface. The mirror plate is attached to the substrate with fixed position substrate hinges allowing it to rotate about the base of the plate. The top of the mirror plate is connected to the support plate with scissors hinges. The base of the support plate is then mounted to the substrate with sliding substrate hinges that allow the plate to freely rotate while the base slides along a single axis.

For assembly of the alignment mirror, two vertical actuators were mounted on opposing sides of the mirror. The single hot arm actuators used in the original assembly system did not provide enough force to lift the alignment mirror plate. Consequently, vertical actuators with two hot arms were used to provide additional leverage. The

double hot arm vertical actuators were able to lift the plate off the substrate as shown in Figure 3-19. These actuators were 180 μm long with 4 μm wide hot arms and 15 μm wide cold arms. Back bending of the double hot arm vertical actuators required 4.2 mA of current with a drive voltage of 13.5-14.5 V.

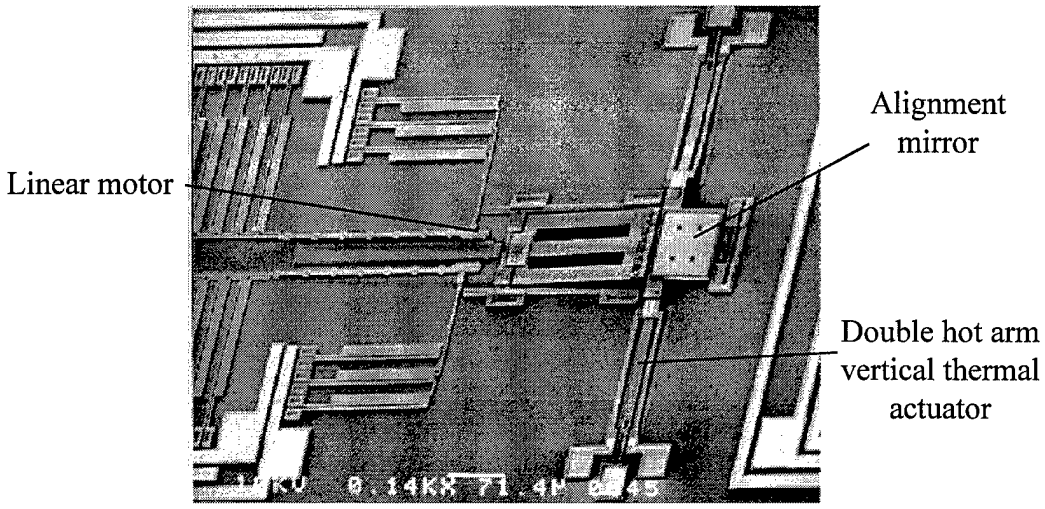


Figure 3-18. Automated assembly system attached to an alignment mirror.

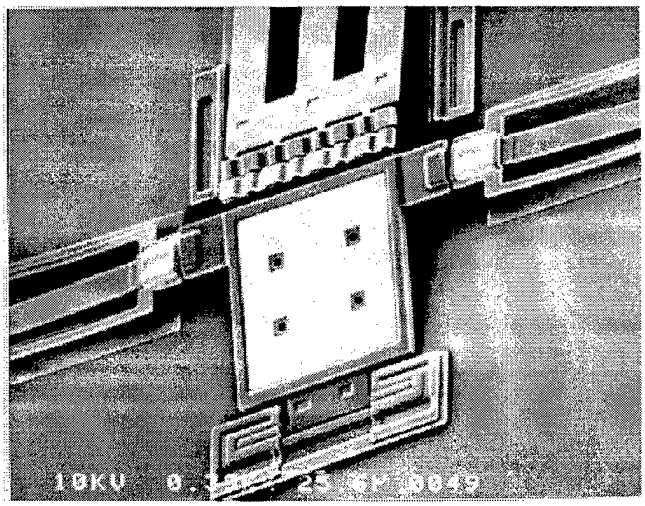


Figure 3-19. Alignment mirror lifted off the substrate by double hot arm vertical actuators.

An assembled alignment mirror is shown in Figure 3-20. Testing of the system showed that only one of the vertical actuators was required to lift the mirror plate off of the substrate. The linear motor was successfully operated and allowed the mirror's angle with the substrate to be controlled. The drive motor required a 132 mW (5.5 V and 24 mA) to drive the coupling array and 210 mW (6.0 V and 35 mA) for the drive array.

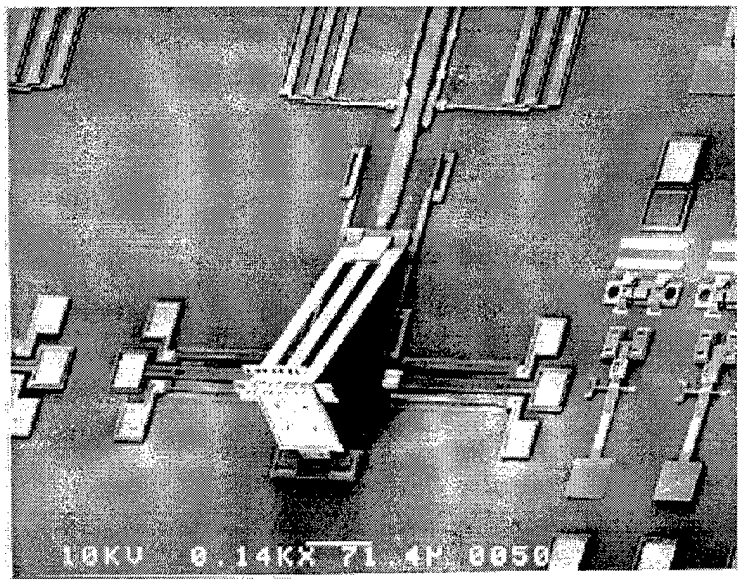


Figure 3-20. Alignment mirror after assembly. (MUMPs 16)

3.4.2 Automated Assembly of Rotating Micromirror

The automated assembly system was also integrated with the rotating micromirror as shown in Figure 3-21. Double hot arm vertical actuators were used for the arrangement shown in Figure 3-21. However, single arm actuators can be used if the attachment point is moved to the side of the mirror plate.

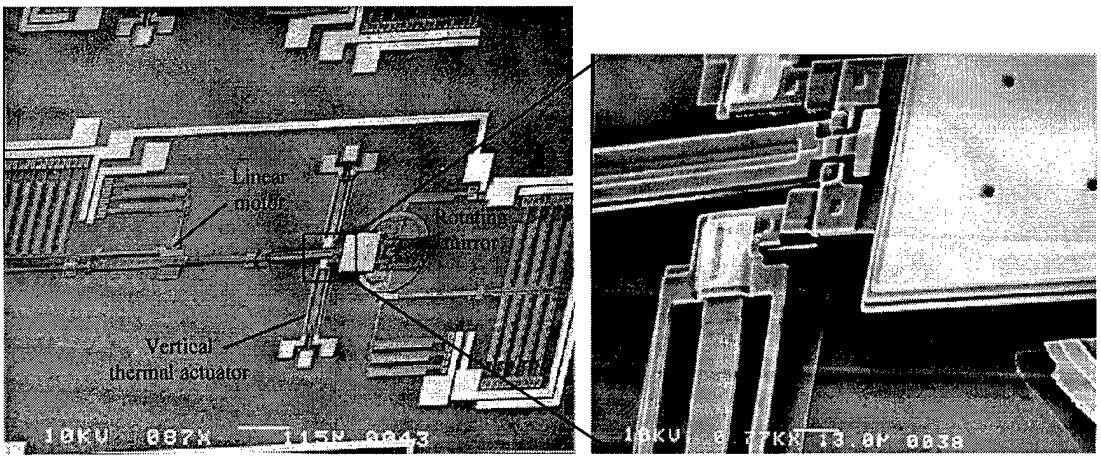


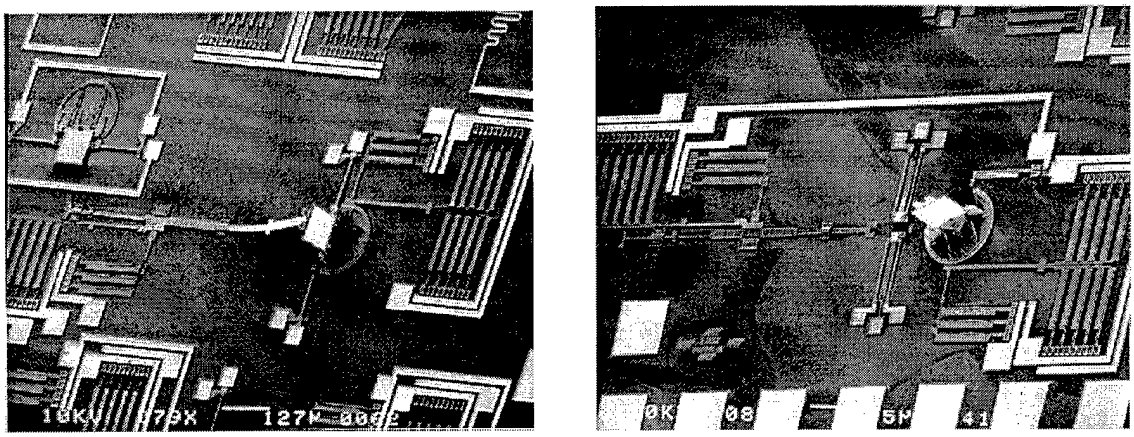
Figure 3-21. Automated assembly system attached to rotating micromirror (MUMPs 16).

After the vertical actuators give the mirror the initial lift off the substrate (Figure 3-21 inset), the linear motor is designed to raise the mirror into the upright position as shown in Figure 3-22 (a). Unfortunately, the 10 element linear motor was only able to partially raise the mirror. A microprobe was used to push the linear motor drive arm and finish the assembly process. New designs are in fabrication which have more powerful actuator arrays and should be able to complete the assembly process. After assembly, the rotating mirror is fully functional and operates as designed. Figure 3-22 (b) shows a rotating mirror which was operated after being raised with an assembly system.

3.4.3 Use of Stressed Cantilevers for Automated Assembly

One of the characteristics of suspended surface micromachined structures is curling due to residual stresses in the materials. This curling is usually undesirable since most microfabricated structures are designed to be flat. However, the stress induced

curling can be used to good effect by replacing the function of the vertical thermal actuators in the automated assembly system.



(a) (b)

Figure 3-22. Rotating micromirror (a) during and (b) after assembly. (MUMPs 16)

The curling due to residual stress of a MUMPs fabricated cantilever is demonstrated in Figure 3-23. Prior to release, the cantilever is held flat due to the surrounding oxide. After release, the residual material stresses in the *Gold* (tensile) and *Poly 2* (compressive) layers cause the free end of the cantilever to curl upward. The amount of curl or deflection is dependent on the amount of stress and the physical dimensions of the material layers. Table 3-2 shows the observed tip deflection for a stressed cantilever.

Table 3-2. Observed Deflection for Unloaded Stressed Cantilever.

Material	Length (μm)	Width (μm)	Thickness (μm)	Stress [39] (MPa)	Deflection (μm)
Gold	238	63	0.5	57 (T)	~ 25
Poly 2	240	65	1.5	8 (C)	

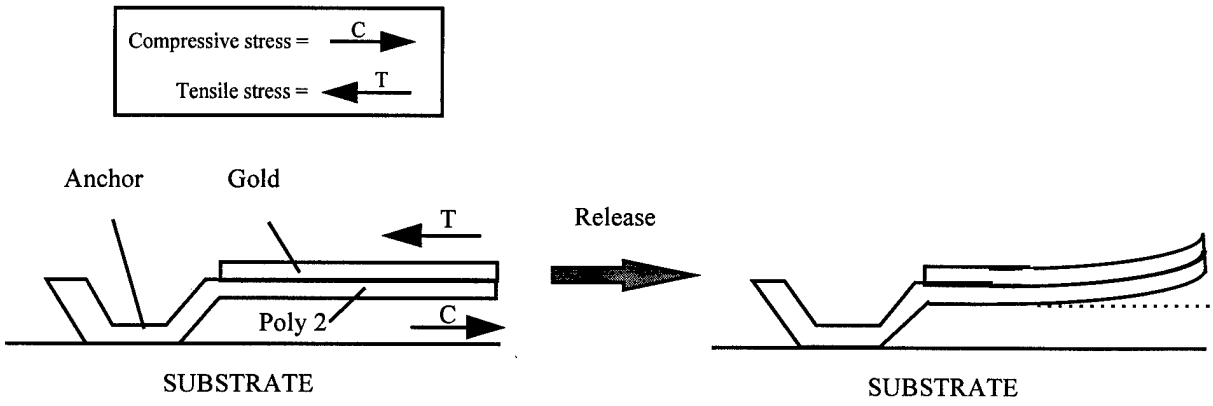


Figure 3-23. Example of cantilever curling due to residual material stress.

The upward force of the free end of the cantilever is strong enough to lift the mirror plate of the scanning micromirror. Figure 3-24 shows a stressed cantilever used to lift a scanning micromirror. The cantilever is composed of *Poly-2* and *Gold*. The *Poly 1* downstops are used to ensure that the cantilever bar does not stick to the substrate during the release process.

The ability of the cantilever to lift the scanning micromirror plate was very consistent. The cantilever successfully lifted the mirror plate on 48 out of 48 mirrors across three different die. The cantilever was able to lift the mirror plate a minimum of 10 μm at the point of contact with the mirror plate which is more than sufficient for the automated assembly system. In some instances, the cantilever was able to propel the mirror plate all the way into the locked position as shown in Figure 3-25.

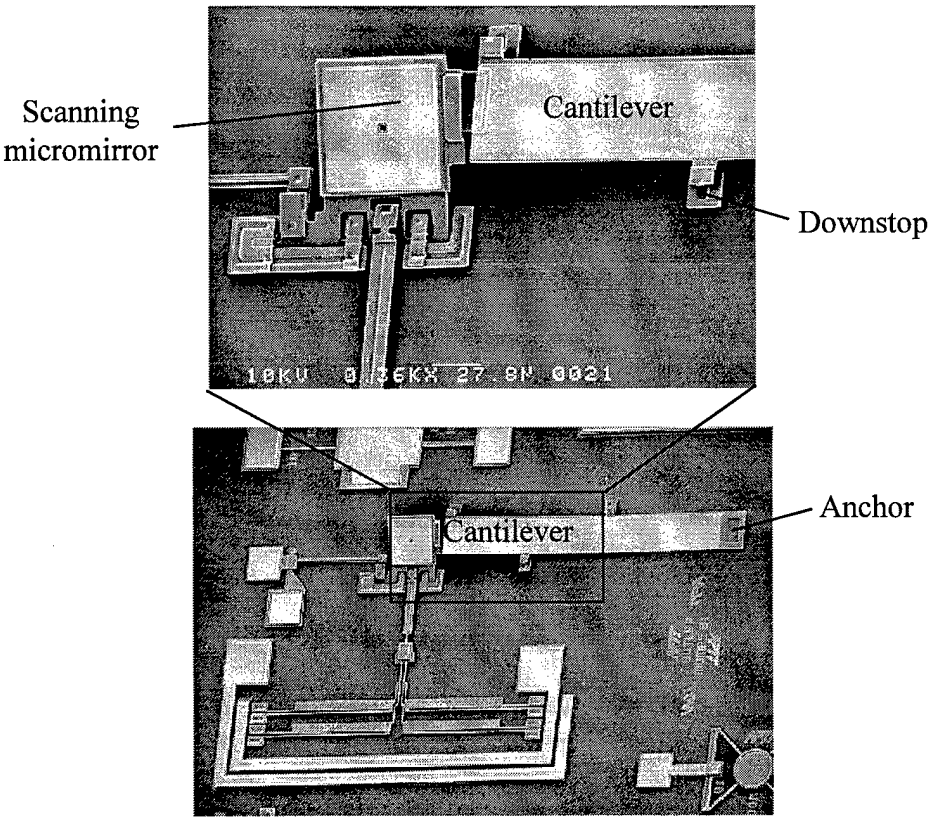


Figure 3-24. Stressed cantilever used to lift scanning micromirror. The cantilever has the dimensions shown in Table 3-2. (MUMPs 21)

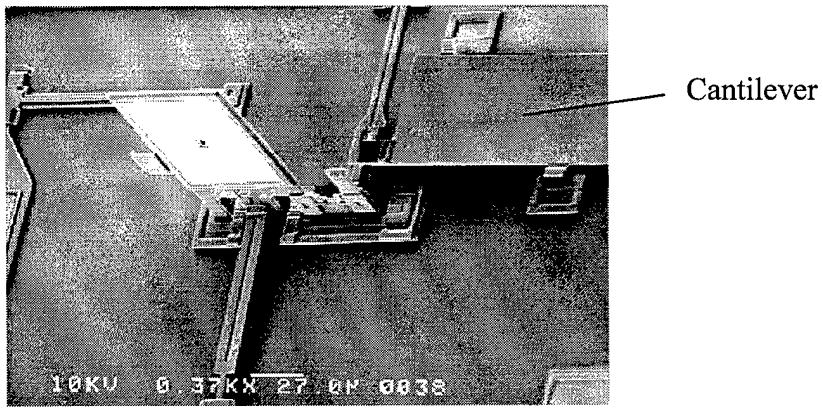


Figure 3-25. Scanning micromirror lifted into locked position by stressed cantilever. (MUMPs 21)

The effectiveness of the cantilever in lifting the scanning micromirror plate make it an attractive alternative to the vertical thermal actuator for use in automated assembly. Figure 3-26 shows a new version of the automated assembly system which uses the stressed cantilever in place of the vertical thermal actuator.

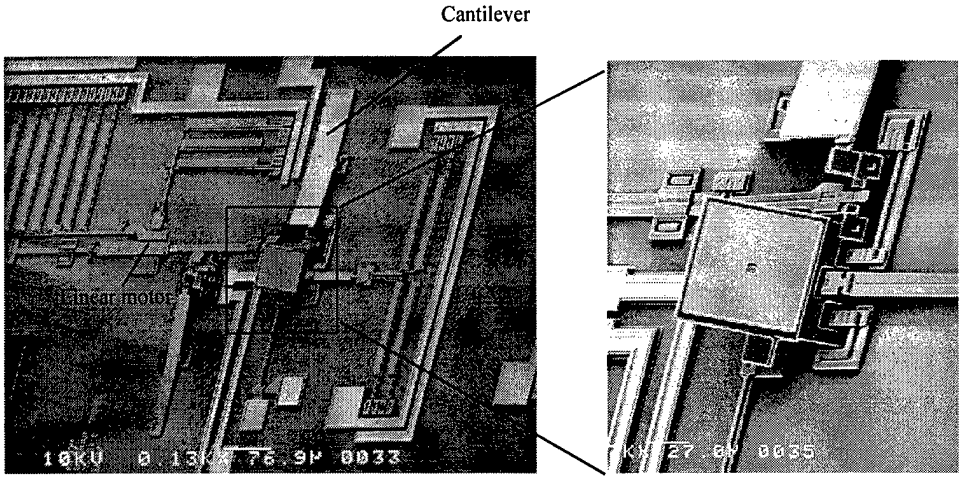


Figure 3-26. Stressed cantilever used as part of the scanning mirror automated assembly system. (MUMPs 22)

One of the key advantages of the cantilever is that it does not require any type of control signal for operation. While back bending of vertical thermal actuators can be automated, it is still a relatively unique set up operation which requires significant design and testing in order to be used properly. Conversely, the stressed cantilever requires no input during the assembly process. In essence, the use of stressed cantilevers for lifting the mirror plate is a first step toward *self* assembly as opposed to *automated* assembly. The availability of releasable, non-conductive layers such as silicon nitride with known high stress could be of great value in the development self assembled MEMS and should be considered for future MEMS fabrication processes.

3.5 Summary

The viability of several MEMS devices has been demonstrated using the MUMPs foundry fabrication process. The devices incorporate previously developed components such as microhinges, cantilevers, and thermal actuators to improve or create new complex devices such as the scanning and rotating micromirror. The automated assembly of flip-up structures was also investigated as the assembly systems for various types of micromirrors were developed. Moreover the concept of using stressed cantilevers for the automated assembly of flip-up structures was pioneered in this research effort.

A focus of the device research was to design MEMS devices capable of being easily integrated with CMOS digital electronics. Low voltage electrostatic and thermal micromirrors were designed, tested, and improved which can be reliably operated at less than 10 volts. In addition, improved thermal actuator arrays were implemented which allow systems such as the scanning and rotating micromirrors to be controlled by digital CMOS electronics as demonstrated in Chapter 6.

While the devices developed in this chapter are amenable to CMOS control, the creation of simulation models for these devices would greatly enhance the design process for MEMS and CMOS integration. The electrostatic micromirrors have been previously studied and modeled [15,30]. Conversely, the thermal actuators have not been modeled in a manner which allows them to be simulated in the same environment with microelectronics. Hence, the modeling of polysilicon thermal actuators is the topic of the next chapter.

Chapter 4. SPICE Modeling of Polysilicon Thermal Actuators

4.1 Electrothermal SPICE Models

One of the hurdles to efficiently employing thermal actuators is understanding and modeling the complex electrothermal system inherent in these devices. The availability of models which are compatible with commonly used circuit simulators such as SPICE are extremely useful for design of integrated microsystems which include thermal actuators. Hence, two types of electrothermal SPICE models were developed to simulate the behavior of polysilicon thermal actuators. The first model uses empirically measured relationships between input voltage, average power, and actuator deflection.

The second model uses process parameters and physical geometry to calculate device performance. Prior research on analyzing the electrothermal response of polysilicon microbridges and line structures [40-42] provides the tools needed to construct the parametric SPICE model. The SPICE model simulates the performance of polysilicon thermal actuators when driven by a DC or pulsed signal. Furthermore, the electrothermal model provides a useful temperature profile of the actuator which can be used to estimate some aspects of the thermo-mechanical behavior of the device. This model provides insight into the operation of thermally actuated devices and allows for predicting the performance of new designs before fabrication.

4.2 Empirical Electrothermal SPICE Model

The empirical SPICE model provides a simple model for describing the performance of thermally actuated devices. The empirical SPICE model was used to simulate the performance of thermal piston micromirrors and lateral thermal actuators and arrays. This model is particularly useful in simulating the electrical load effects of thermal devices when integrated with microelectronic drive circuitry. Figure 4-1 shows a schematic of the model for a thermal actuator.

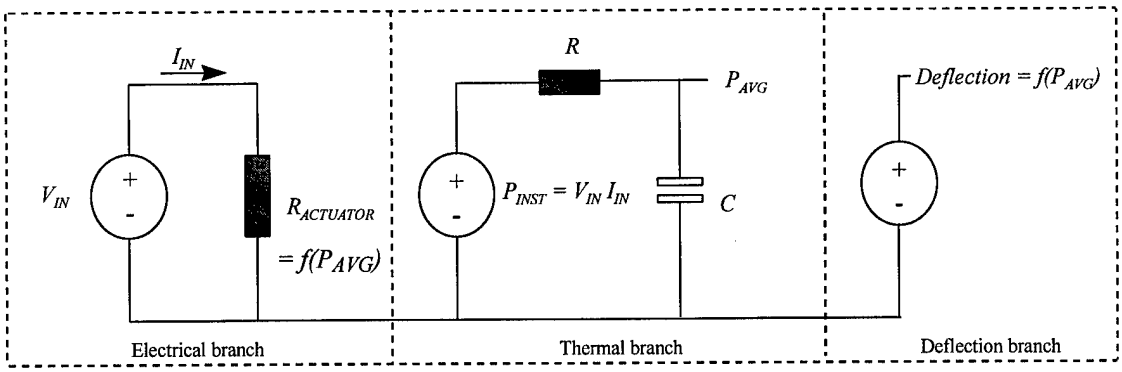


Figure 4-1. Schematic of empirical electrothermal model for thermal actuator.

This model is based on the observation that the electrical resistance of the actuator varies as a function of temperature, and the temperature is in turn a function of the average input power. Thus, the main element in the electrical branch of the model is a voltage controlled resistor, $R_{ACTUATOR}$, which represents the variable actuator resistance. The controlling voltage, P_{AVG}, represents the average power applied to the device. Since SPICE only allows voltage and current dependent variables, the average and instantaneous power are represented as voltages in our model. The average input power

is computed in the thermal branch of the model by integrating the instantaneous power, $P_{INST} = V_{IN}\ I_{IN}$, over time. A capacitor, C, is used to perform the integration as shown in Figure 4-1. The value of R and C are chosen to best match the thermal time constant of the device. The deflection of the actuator is also a function of the average input power and can be represented in the model as a dependent voltage source with P_{AVG} used as the controlling node.

The relationships between input power and actuator resistance and deflection were determined by measuring the response of actual devices to DC inputs. The results were plotted and empirical equations were generated from best fit curves. These equations were then incorporated into the model to establish the required dependencies.

The transient thermal response of the piston micromirror was measured using a laser interferometer system previously used to test electrostatic piston devices [30,43]. This system is currently equipped with a four probe pressure vessel allowing testing to be performed at pressures of 20 mT to 1000T in ambient nitrogen or air. The interferometer system requires dynamic motion of the mirror under test to produce accurate deflection measurements. Thus deflection measurements were performed by driving the mirror with a pulsed input and recording the transient response of the interferometer's detector diode. The detector signal must then be unwrapped to produce a mirror deflection vs. time curve. Deflections of at least $\lambda_{HeNe}/4$ are required to facilitate unwrapping of the detector signal. Figure 4-2 shows the raw drive signal and PIN detector diode response for one transient measurement. Also shown is the resulting deflection vs. time curve as the mirror moves to the powered position. The thermal time response (analogous to an RC

time constant) of the device can be read directly from the deflection vs. time curve as annotated in the figure. Mirror peak deflections and drive pulse amplitudes for a set of measurements are plotted to produce a static deflection curve. Matlab® scripts automate processing of laser interferometer data [44].

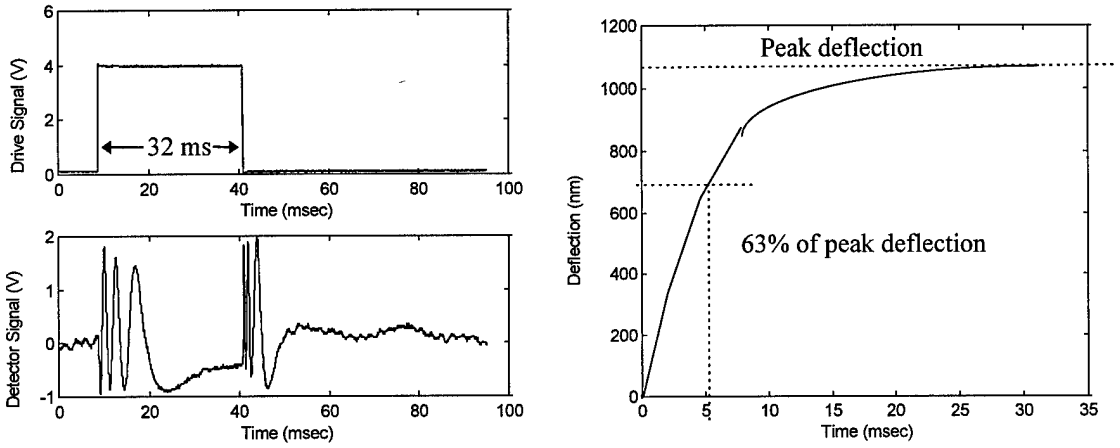


Figure 4-2. Raw drive signal and detector signal from laser interferometer (left), and micromirror deflection vs. time (right) produced by data analysis. Also shown is measurement of thermal time constant. The length/width/thickness of the micromirror flexures were 40/3/2 μm. The mirror plate had a diameter of 80 μm.

The transient response of the lateral actuators was measured by using the laser source, PIN diode detector, and digital oscilloscope from the laser interferometer system. After positioning the laser spot (~4 μm diameter) at a fixed distance from the actuator tip, a pulsed drive signal was applied. Due to focus effects and the differing optical reflectivity of the substrate and actuator, passage of the actuator tip through the laser spot was easily detected by the PIN diode. The pulse width and period of the drive signal were chosen to allow the lateral actuator to fully deflect and then return to the initial

position before the next pulse. The time from the start of the drive pulse to the passage of the actuator tip through the laser spot was recorded for several deflection values.

The measured transient response data was then plotted and an exponential curve fit was used to produce an estimate for the time constant:

$$\text{Exponential fit} = Max\_deflection * (1 - e^{(\frac{-t}{\tau})}) \qquad (4\text{-}1)$$

where *Max_deflection* is the maximum deflection the actuator will achieve, t, is elapsed time, and τ is the time constant. The time constant of the exponential function was used to select the resistor, R, and capacitor, C, values used in the model where $\tau = RC$. Figure 4-3 shows the measured thermal response for a lateral thermal actuator.

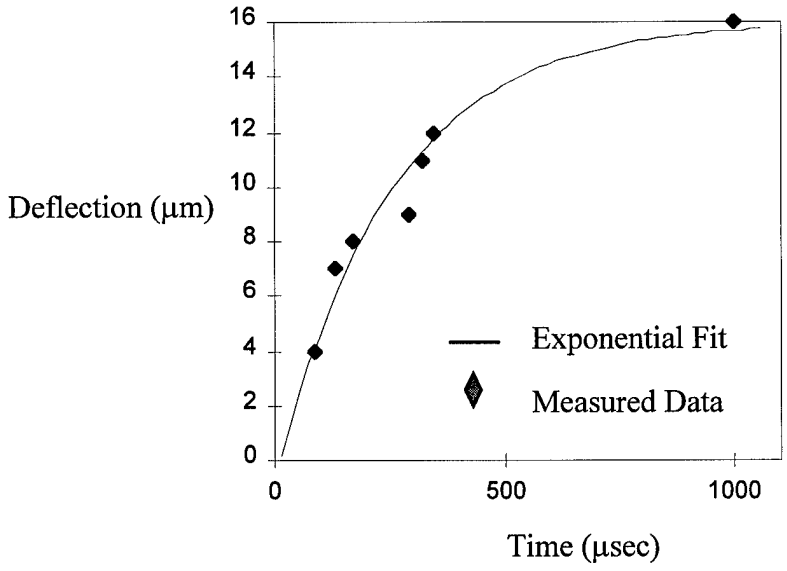
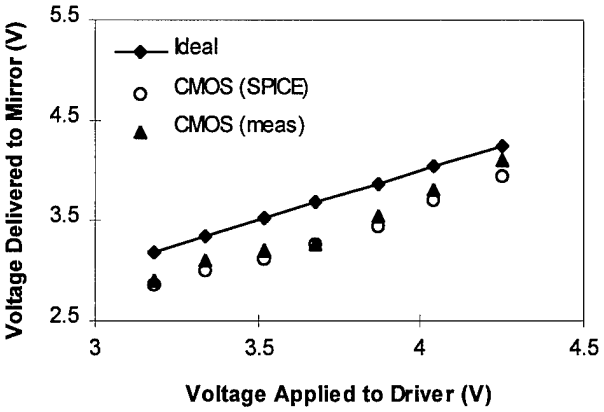


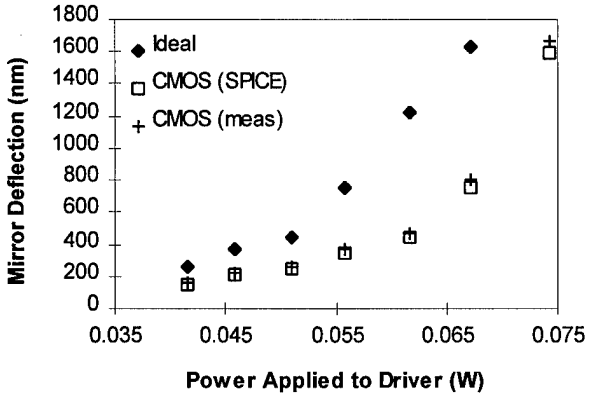
Figure 4-3. Exponential curve fit of measured transient response of lateral thermal actuator in 20 mT vacuum. The length/width of the actuator hot arm, cold arm, and flexure were 200/2.0 μm, 170/14 μm, and 30/2.0 μm. The thickness of the polysilicon was 2 μm. The time constant, τ, for the exponential curve was 250 μs.

One application of the empirical model is to assess the loading impact of thermally actuated devices on drive circuitry. Figure 4-4 compares the SPICE model versus measured data for the deflection of a piston micromirror when driven by a pulsed or DC input from an ideal (regulated) voltage source and a CMOS driver. The SPICE model of the micromirror was generated using the procedure discussed above prior to testing with pulsed and DC inputs. In this example, the CMOS drivers were undersized and were not able to supply enough current to maintain the desired voltage across the piston mirror. Hence, the amount of power actually applied to the micromirror was less than expected. The SPICE model was able to accurately predict the impact of resistive loading on the CMOS drivers and the reduction in mirror deflection.

An attractive feature of the empirical model is the ability to easily generate representative models of complex systems. Since the model only seeks to simulate the performance of an existing system or component, only empirical measurements are needed to adjust the flexible model parameters to match the performance of the device. Several commercial software programs such as Matlab and Excel have the built-in functions which generate n^{th} order, best fit equations to a paired data set. Consequently, the author was able to quickly generate electrothermal models of complex systems such as stepper motors and mirror arrays by measuring the system I-V response and incorporating the results into the variable equations in the empirical SPICE model.



(a)



(b)

Figure 4-4. (a) Driver output loading and (b) deflection characteristics for piston micromirror when positioned by ideal power source and CMOS driver (SPICE model and measured). The lower mirror deflection when using the CMOS driver is due to resistive loading effects.

4.3 Parametric Model

A limitation of the empirical SPICE model is that it is not useful for predicting the response of a device before fabrication nor does it provide any real insight into the internal functioning of the device. The parametric SPICE model provides another method of simulating thermal actuators by using process parameters and device geometry. While computationally more intense, this model does provide insight into the

operation of thermally actuated devices and allows for predicting the performance of new designs before fabrication.

4.3.1 Theory

The current flowing in a polysilicon microbridge or thermal actuator causes resistive heating to occur. Due to the small physical dimensions of MEMS devices, it is easy to quickly raise the temperature of the device to the polysilicon melting point of 1685K. As shown in Figure 4-5, four heat loss processes exist for dissipating the heat build up in the microbridge or actuator: (1) heat conduction through the bridge, H_{bridge}; (2) heat conduction through the surrounding gas into the substrate, $H_{conduction}$; (3) heat loss through convection into the surrounding gas, $H_{convection}$; and (4) heat loss through thermal radiation, $H_{radiation}$.

Aside from convection, these heat loss mechanisms can be conveniently modeled. Convection requires a knowledge or model of the gas movement in the environment. However, if we make the reasonable assumption that the microbridge will be operated in a protected or benign environment in which it will not be subjected to gas currents, convection can be ignored [41]. Consequently, we are left with three heat loss processes which can be thermally modeled using material and physical properties alone. The heat balance equation is thus reduced to:

$$I^2R = H_{bridge} + H_{conduction} + H_{radiation} \tag{4-2}$$

where I^2R represents the power generated by current flow in the microbridge or actuator.

Thermal entities such as heat flow and temperature have electrical analogues which obey the same mathematical relationships. This allows for thermal networks to be described in terms of electrical circuits. Table 4-1 lists thermal parameters and their electrical equivalent. The ability to use electrical circuit theory for thermal analysis is of great benefit because of the wide availability of electrical circuit simulators such as SPICE which can therefore be used for thermal analysis. For our application, SPICE will be used to simulate a coupled electro-thermal model of polysilicon microbridges and thermal actuators.

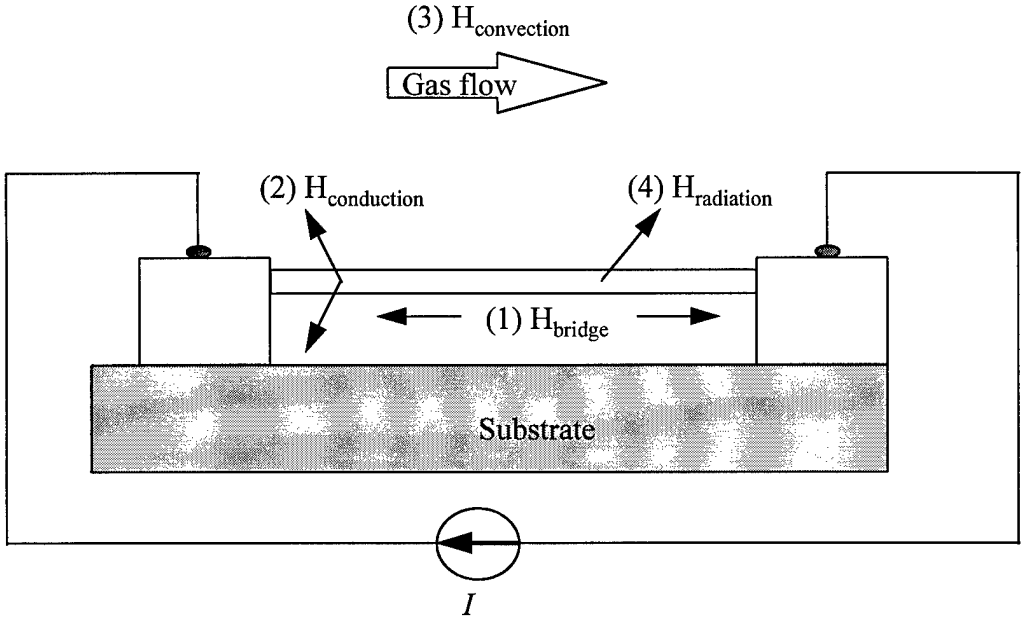


Figure 4-5. Heat loss mechanisms in polysilicon microbridge.

Table 4-1. Thermal Parameters and Their Electrical Equivalents [7].

Thermal Parameter	Thermal Units	Electrical Equiv.	Electrical Units
Temperature (T)	Degrees (K)	Voltage (V)	Volts
Heat Flow (Power) (P)	Watts (W)	Current (I)	Amps (A)
Heat (Q)	Energy (J=W-s)	Charge (Q)	Coulombs (C=A-s)
Capacity (C)	J/K	Capacitance (C)	A-s/V
Resistance (R)	K/W	Resistance (R)	Ω=V/A
Conductance (G)	W/K	Conductance (G)	Ω^{-1}
Resistivity (ρ_{th})	K-m/W	Resistivity (ρ_{el})	Ω-m
Conductivity (κ)	W/K-m	Conductivity (σ)	Ω^{-1}/m

4.3.2 Finite Element Model of Microbridge

The heart of the parametric model is an electro-thermal representation of a microbridge or actuator element. The model uses finite differences to provide a straightforward numerical solution for device performance which can be implemented in SPICE. When using finite differences, the device is divided into elements small enough that a linear temperature distribution can be assumed throughout each element. This assumption allows for an individual element to be represented as a coupled electrothermal network as proposed by Mastrangelo [41]. Figure 4-6 (a) defines the nomenclature used to describe the physical dimensions of an individual finite element, while Figure 4-6 (b) represents the electrical circuit model.

In the electrical branch of Figure 4-6, ΔR represents the temperature dependent electrical resistance, while V is the applied voltage. In the thermal branch, G_T is the thermal conductance for heat flow through the element, G_G is the thermal conductance for heat flow through the surrounding gas to the substrate, and G_R represents heat loss due to thermal radiation. C_T is the thermal capacity of the element, and P_G represents the heat

generated in the element through ohmic (or joule) heating. $T+$ and $T-$ are the temperatures at the ends of the element, T_{AVG} is the average temperature in the element, and T_S is the substrate temperature.

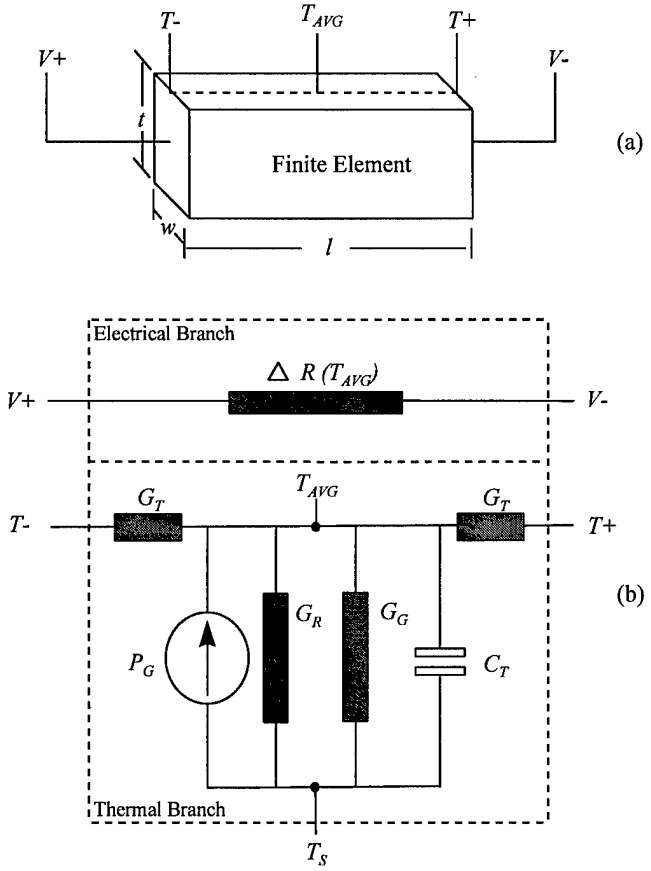


Figure 4-6. (a) Physical and (b) electrothermal representation of finite element derived from Mastrangelo's polysilicon microbridge model [41] with the addition of a thermal radiation conductance, G_R.

The values of the components in the model are calculated using the physical dimensions of the element and material properties of polysilicon and the surrounding gas. In the thermal branch C_T, G_T, and G_G can be calculated as [41]:

$$C_T = C_p wtl \tag{4-3}$$

$$G_T = \frac{2\kappa_p wt}{l} \tag{4-4}$$

$$G_G = \frac{F_s \kappa_G wl}{s} \tag{4-5}$$

where C_P is the heat capacity of polysilicon, and κ_p and κ_G are the thermal conductivity of the polysilicon and surrounding gas, respectively. F_S is the shape factor which accounts for the impact of the shape of the element on heat-transfer to the gas [40,41], and s is the elevation of the element above the substrate. The length, width, and thickness are represented by l, w, and t.

The thermal conductivity of the gas is pressure dependent, hence the heat loss through gas conduction to the substrate is also pressure dependent. A common method of approximating the pressure dependency of κ_G is:

$$\kappa_G(P) = \kappa_G(\infty)\left[\frac{\frac{P}{P_o}}{1+\frac{P}{P_o}}\right] \tag{4-6}$$

where $\kappa_G(\infty)$ is the thermal conductivity of the gas at one atmosphere or greater, P is the pressure in Pascal, and P_0 is an empirically derived constant which defines the dependency of the gas conductivity with pressure [41].

The thermal radiation, G_R, is calculated as:

$$G_R = \frac{P_{RADIATION}}{T_{AVG} - T_S} \; . \tag{4-7}$$

The power radiated from a polysilicon microbridge due to resistive heating can be computed as [42]:

$$P_{RADIATION} = 2\varepsilon\sigma(t+w)\int_0^l [T^4(x) - T_S^4]dx \tag{4-8}$$

where ε is the emissivity of polysilicon, σ is the Stefan-Boltzmann constant, and *T(x)* is the temperature distribution along the bridge. For our applications, we assume a linear temperature distribution throughout the element, and *T(x)* then becomes:

$$T(x) = T_- + \frac{(T_+ - T_-)}{l}x, \quad 0 < x < l. \tag{4-9}$$

The radiated power is then found using Equations (4-8) and (4-9) as:

$$P_{RADIATION} = 2\varepsilon\sigma l(t+w)[\frac{T_+^5 - T_-^5}{5(T_+ - T_-)} - T_S^4]. \tag{4-10}$$

For short microbridge elements (l < 20 μm) the temperature distribution can be assumed to be uniform throughout the element, and then the temperature distribution simplifies to $T(x) = T_{AVG}$. Thus, the radiated power can be more easily calculated as:

$$P_{RADIATION} = 2\varepsilon\sigma l(t+w)[T_{AVG}^4 - T_S^4]. \tag{4-11}$$

This simplification provides an estimate of the thermally radiated power that is within eight percent of the result of generated by Equation (4-10) for a bridge element of length 20 μm and width and thickness of 2 μm.

The thermal radiation conductance increases the accuracy of the model for devices such as the lateral thermal actuator which can be operated at elevated device temperatures (>1000 °C). At these elevated temperatures, thermal radiation becomes significant, especially in vacuum or low pressure ambients. The addition of the thermal radiation conductance reduces the error of the model for the lateral thermal actuator at high drive

voltages from +/- 15 percent to well within 10 percent. One caveat to modeling thermal actuators at high drive voltages is that the actuator resistance must be closely monitored since irreversible changes in the polysilicon structure can occur [40,41,44].

The thermal radiation conductance can be omitted for devices which are not designed to operate at temperatures high enough to generate substantial thermal radiation. For example, the gold surface on the thermal piston micromirror will fail when the mirror plate temperature exceeds the silicon-gold eutectic temperature of 363 °C. Consequently, the temperature in the thermal piston micromirror must be kept below this point, and thermal radiation becomes negligible. Removing the thermal radiation conductance in the model shows no degradation in accuracy for the thermal piston micromirror.

Both ΔR and P_G are functions of the average element temperature, T_{AVG}, and are represented as [41]:

$$\Delta R = R_O [\, 1 + \alpha(T_{AVG} - T_S) \,] \tag{4-12}$$

$$P_G = \frac{V^2}{\Delta R} \tag{4-13}$$

where R_O is the small signal electrical resistance of the element and α is the temperature coefficient of resistivity (TCR) of polysilicon. The TCR of MUMPs *Poly 1* was determined empirically in a series of experiments as described in Chapter 5.

Tables 4-2 through 4-4 summarize the constants and equations used for each element in Figure 4-6.

Table 4-2. Equations for Components shown in Figure 4-6.

Model Equations
$C_T = C_p wtl$
$G_G = \frac{F_s \kappa_G wl}{s}$
$G_R = \frac{P_{RADIATION}}{T_{AVG} - T_S}$ $P_{RADIATION} = 2\varepsilon\sigma l(t+w)[\frac{T_+^5 - T_-^5}{5(T_+ - T_-)} - T_S^4]$
$G_T = \frac{2\kappa_p wt}{l}$
$P_G = \frac{V^2}{\Delta R}$
$\Delta R(T_{AVG}) = R_O [\, 1 + \alpha(T_{AVG} - T_S) \,]$

Table 4-3. Elements Used In Coupled Electro-Thermal Model Shown In Figure 4-6.

Nomenclature	Description
l	Element length
w	Element width
t	Element thickness
C_T	Thermal capacity of element
G_G	Conductance of heat into gas
G_R	Conductance of thermal radiation
G_T	Conductance of heat flow through element
P_G	Heat generated due to joule heating
$\Delta R(T_{AVG})$	Temp. dependent electrical resistance
T-, T+	Temperature at ends of element
T_{AVG}	Average temperature
T_S	Substrate temperature
V	Applied voltage

Table 4-4. Material and Physical Parameters Used in Equations in Table 4-2.

Parameter	**Value**	**Description**
s	design dependent	Element elevation above substrate
C_P	7.54×10^{2} $JKg^{-1}K^{-1}$	Heat capacity of polysilicon [46]
F_S	design dependent	Element shape factor [40,41]
R_O	design dependent	Small signal electrical resistance (see Chap 5)
α	1.25×10^{-3} K^{-1}	Thermal coefficient of resistivity (TCR) of polysilicon (see Chapter 5)
ε	0.7	Emissivity of polysilicon [47]
κ_G	2.6×10^{-2} $Wm^{-1}K^{-1}$	Thermal conductivity of gas (nitrogen) [41]
κ_P	30 $Wm^{-1}K^{-1}$	Thermal conductivity of polysilicon [41,48]
σ	56.7×10^{-9} $Wm^{-2}K^{-4}$	Stefan-Boltzmann constant [7]

4.3.3 Generating SPICE Subcircuits From Electrothermal Model

The electro-thermal microbridge model is easily implemented in SPICE; however, both the lateral thermal actuator and the piston micromirror have geometries which are more complex than a single microbridge. Consequently, our approach to generating an electro-thermal model is to decompose the device into a network of microbridges which are further divided into finite elements.

Since the microbridges are in close proximity, there is the potential for the introduction of another heat loss mechanism through gas conduction from a hot microbridge to a cooler bridge. However, this is not significant in our case because the thickness of the actuators is usually only 2 μm which limits the area for conduction between microbridges as compared to conduction to the substrate. In addition, the temperature difference between the microbridges is typically much less than the temperature difference between a microbridge and the substrate since all of the bridges have an elevated temperature due to current or heat flow while the substrate temperature remains fixed. Consequently, the conduction of heat to the substrate is normally much greater than heat conduction to neighboring microbridges which allows us to ignore inter-bridge conduction.

Figure 4-7 shows how a lateral thermal actuator is decomposed into a series of three microbridges. Each microbridge is then divided into a series of finite elements. The electrothermal SPICE model is formed from the interconnected finite elements defining the microbridges.

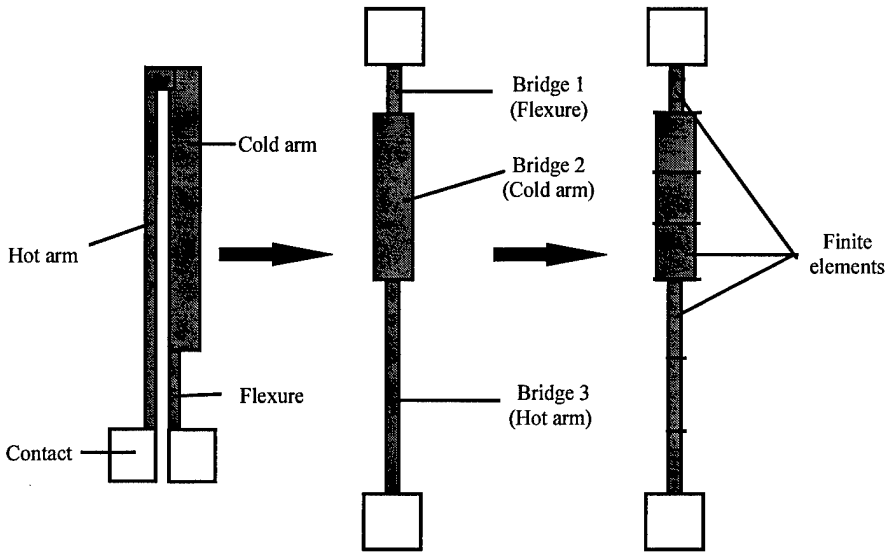


Figure 4-7. Lateral thermal actuator as a series of three microbridges.

The finite difference model for the piston micromirror was also developed using this approach as shown in Figure 4-8. One additional step for generating the model for the thermal micromirror was to "Manhattanize" the mirror section in order to simplify the calculations for the model. Converting the mirror shape from circular to square does not impact any of the expected outputs from the model.

Programs and batch files have been written which automatically generate the SPICE model for both the lateral thermal actuator and the piston micromirror. Each microbridge is typically divided into 10 finite elements. The accuracy of the model increases with more elements, but the simulation time also increases. Ten elements provides good accuracy while maintaining fast simulation speed [41]. Moreover, the development of software to automatically generate the SPICE model is greatly simplified by using microbridges. Each of the finite elements in a microbridge has the same

physical dimensions; and consequently, each element has identical values for the components in the electrothermal SPICE network.

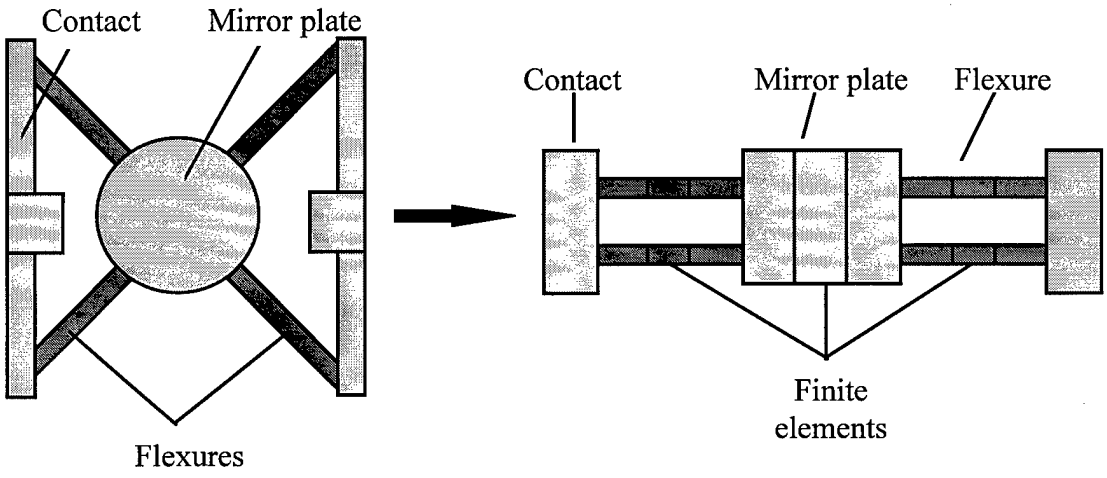


Figure 4-8. Decomposition of thermal piston micromirror for model representation.

Moreover, a software routine which greatly simplifies the calculation of the shape factor, F_S, has been added. As mentioned previously, the shape factor accounts for fringing heat flux effects which are a function of the shape of the element and its elevation above the substrate [40,41]. For arbitrary shapes, F_S is found by using computationally intense numerical methods or conformal mapping [41]. However, if a Manhattan (rectangular) geometry is assumed, the calculation for the shape factor can be accurately and simply reduced to the empirical equation [40]:

$$F_s = \frac{t}{w}\left(\frac{2s}{t}+1\right)+1 \tag{4-14}$$

where s is the elevation above the substrate and t and w are the thickness and width of the element. For Manhattan structures, this equation is accurate to within five percent of the

answer obtained from the numerical method previously used by Mastrangelo [41]. In addition, the equation can be incorporated into the program that generates the SPICE listing which obviates the need for an external program to calculate shape factor.

The equation can be further simplified for the MUMPs process by recognizing that the elevation above the substrate and thickness are usually both 2 μm for *Poly 1* thermal actuators [17]. Therefore, F_S for Manhattanized *Poly 1* structures can be reduced to a function of width alone:

$$F_s = \frac{6}{w} + 1 \tag{4-15}$$

Figures 4-9 and 4-10 demonstrate the accuracy of the finite element SPICE model in predicting the I-V characteristics of a lateral thermal actuator and thermal piston micromirror. For the SPICE model results shown in Figures 4-9 and 4-10, bridge elements were each divided into 10 finite elements. The theoretical I-V curve in Figure 4-9 was generated using Tai's model described in [42]. This model is discussed in more detail in Chapter 5.

4.3.4 Uses For Temperature Profile

One of the benefits of the finite element SPICE model is that it provides a temperature profile of the device. This temperature profile can be used to generate inputs for estimating the deflection and other thermal related properties of the thermal actuator.

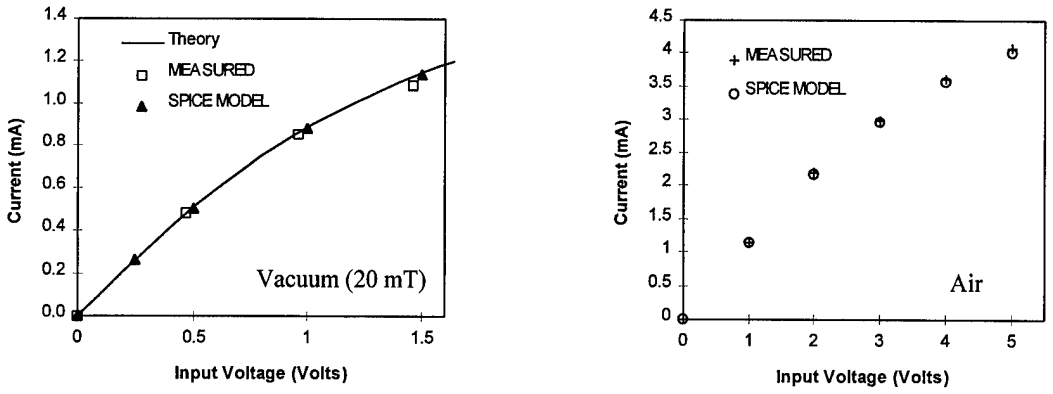


Figure 4-9. Theoretical, SPICE model, and measured current versus voltage for lateral thermal actuator in 20 mT vacuum and air. The length/width of the actuator hot arm, cold arm, and flexure were 230/2.5 μm, 180/16 μm, and 50/2.5 μm. The thickness of the polysilicon was 2 μm. The theoretical curve was generated from a model developed by Tai, et al. [42].

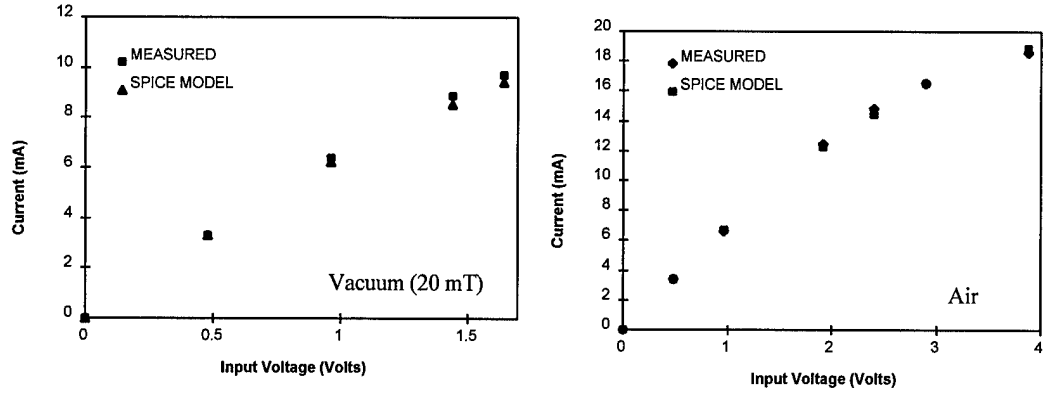


Figure 4-10. Measured and SPICE model current versus voltage for thermal piston micromirror in 20 mT vacuum and air. The length/width/thickness of the mirror flexures was 64/4/2 μm. The mirror plate had a diameter of 70 μm.

The deflection of the lateral thermal actuators is approximated by a simplified macroscale formula since SPICE is not an optimum environment for mechanical modeling. For the lateral thermal actuator, the tip deflection, $\delta_{LATERAL}$, is estimated using a formula for cantilevered thermal bimorphs constructed from materials with the same or similar Young's modulus [49]:

$$\delta_{LATERAL} \approx \frac{3L^2(T_{HOT} - T_{COLD})[\lambda(T_{HOT}) - \lambda(T_{COLD})]}{4W_{H+F}} \tag{4-16}$$

where T_{HOT} is the average temperature of the 'hot arm' of the thermal actuator, and T_{COLD} is the average temperature of the 'cold arm' and flexure. L is the length of the hot arm, and W_{H+F} is the sum of the widths of the hot arm and flexure. λ is the coefficient of thermal expansion of polysilicon as a function of temperature [50]:

$$\lambda(T) = (3.725\{1 - e^{[-5.88\times10^{-3}(T-124)]}\} + 5.548\times10^{-4}\,T)\times10^{-6}\ (\mathrm{K}^{-1}) \tag{4-17}$$

T_{HOT} and T_{COLD} are calculated from the temperature profile of the device generated in the thermal branch of the SPICE model. Figure 4-11 compares the deflection prediction of the finite difference SPICE model with measured data. The measured data was collected from a pulsed input signal with a 5 volt amplitude and a variable duty cycle. The period of the input signal was 10 μs which is much faster than the response of the thermal actuator.

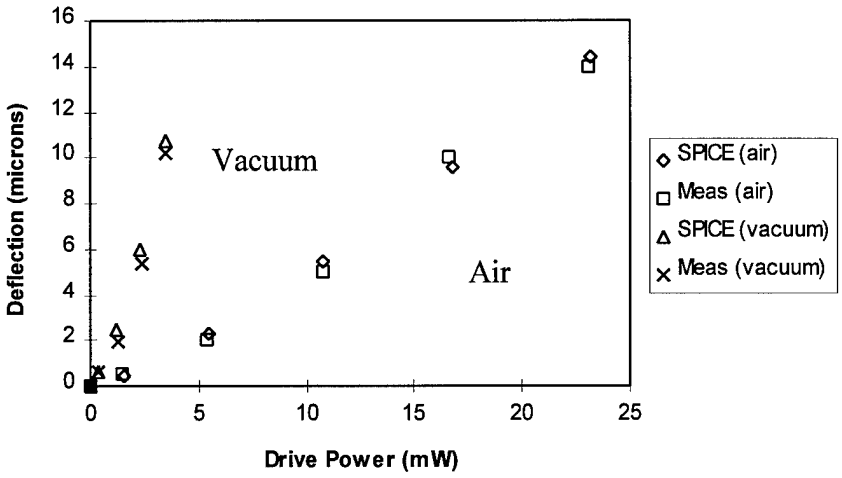


Figure 4-11. SPICE model and measured deflection versus average power for lateral thermal actuator. The length/width of the actuator hot arm, cold arm, and flexure were 200/2 μm, 170/14 μm, and 30/2 μm. The thickness of the polysilicon was 2 μm. The vacuum pressure was 20 mT.

The SPICE model provided insight into the difference in deflection of lateral thermal actuators in air versus a vacuum. The temperature profiles generated from SPICE models showed that lateral thermal actuators are able to achieve greater overall deflections in air because of the increased temperature difference between the hot arm and cold arm. Table 4-5 illustrates the difference in average temperatures for a lateral actuator in vacuum and air. In air, the relatively large surface area of the cold arm allows for significantly more heat conduction into the surrounding gas to the substrate as compared to the hot arm. This extra gas cooling keeps the cold arm temperature much lower than that of the hot arm. In a vacuum, there is negligible loss of heat into the gas, and this source of additional cooling is not available; consequently, the temperature difference between the hot arm and cold arm is not as great.

Table 4-5. SPICE Model Maximum Average Temperature of Lateral Actuator Components in Air and 20 mT Vacuum.

Component	Length/Width/Thickness (μm)	Avg Temp (Vac) (K)	Avg Temp (Air) (K)
Hot arm	200/2/2	950	1160
Cold arm	160/14/2	790	435
Flexure	40/2/2	490	380

Another illustration of the usefulness of the temperature profile is in predicting failure characteristics for a lateral thermal actuator. In particular, the temperature profile is useful in determining the general location of failure by predicting the physical location that will reach the melting point first. In a vacuum, thermal conduction through the actuator to the substrate is the primary heat loss mechanism. Consequently, the hottest spot should be the point for which the thermal and, in this case, electrical resistance to the substrate is the greatest.

The SPICE model was able to accurately predict this phenomena for a wide variety of actuator designs. Figure 4-12 shows a two element actuator array driven to failure in a 20 mT vacuum. For these actuators, the failure point should theoretically be at 127 μm along the hot arm which represents the point of maximum electrical and thermal resistance to the substrate. Since the hot arm is 200 μm long, the failure should occur at roughly two-thirds the length of the hot arm. This compares favorably with the observed failure points shown in Figure 4-12 and the SPICE prediction of 125 μm.

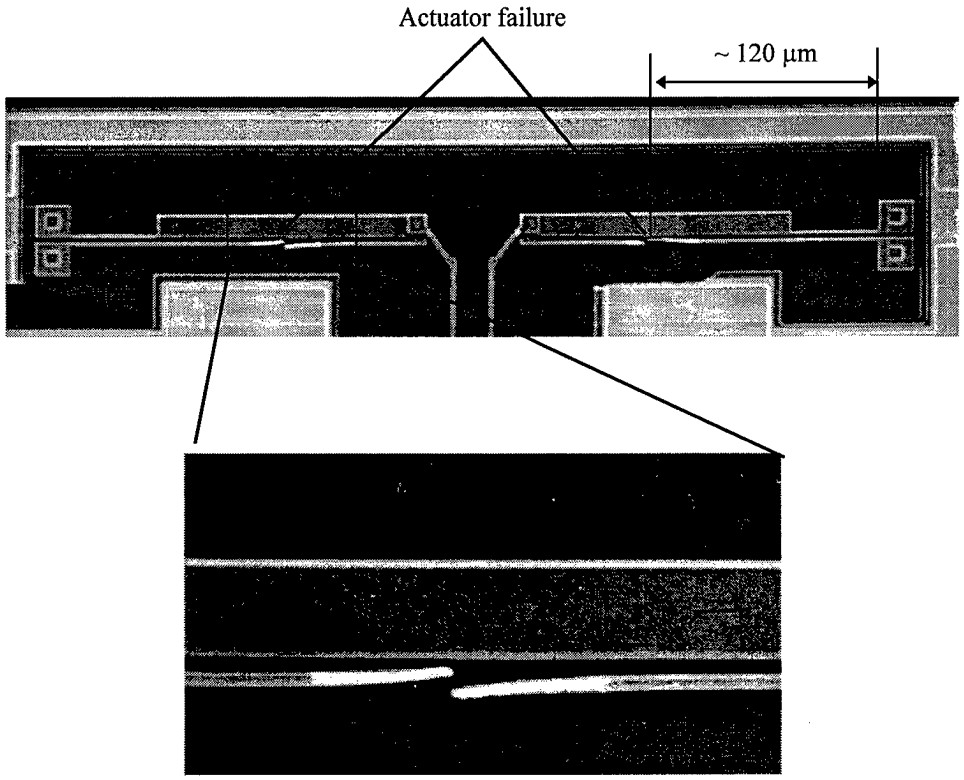


Figure 4-12. Two element actuator array driven to failure in a 20 mT vacuum. The length/width of each actuator hot arm, cold arm, and flexure were 200/2 μm, 170/14 μm, and 30/2 μm. The thickness of the polysilicon was 2 μm.

The presence of gas cooling changes the characteristics of actuator failure. As mentioned previously, gas cooling greatly reduces the temperature of the cold arm. This in turn alters the temperature profile of the hot arm and moves the expected failure location toward the center of the hot arm. This allows a greater region of the hot arm to reach high enough temperatures to cause melting and possibly failure. Figure 4-13 shows an actuator driven to failure in air. The failure point predicted by SPICE was 120 μm which is roughly 60 percent of the length of the hot arm. This agrees well with the observed failure point as seen in Figure 4-13.

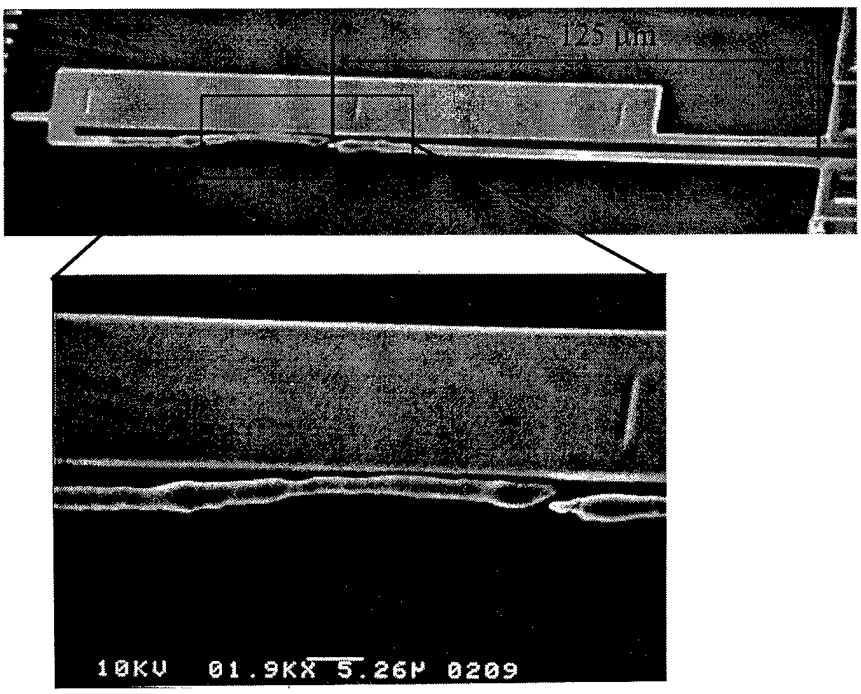


Figure 4-13. Lateral thermal actuator driven to failure in air. The length/width of the actuator hot arm, cold arm, and flexure were 200/2 µm, 170/14 µm, and 30/2 µm. The thickness of the polysilicon was 2 µm.

The SPICE model also provides insight on back bending which is another characteristic of lateral actuators operated near failure. Back bending of thermal actuators is difficult in a vacuum. Typically, the actuator fails before a large and controlled plastic deformation can be achieved. However, back bending in air produces a much larger plastic deformation and is much easier to control [24].

The SPICE generated temperature profile demonstrates that the rate of temperature increase in the hot arm is much faster in a vacuum than in air. This is due to the absence of gas cooling. In a vacuum, when the hot arm of the thermal actuator is hot enough to undergo plastic deformation, a small increase in the applied current is enough

to elevate the temperature to failure because the main cooling mechanism is conduction to the substrate through the actuator. Conversely, in air, the presence of gas cooling allows for a slower and more controlled increase in the temperature which allows for greater plastic deformation without destroying the hot arm. Moreover, the presence of gas cooling greatly increases the segment of the hot arm which is able to reach a high enough temperature to induce a plastic deformation.

Figures 4-12 and 4-13 illustrate these points. Notice how 'clean' the break is along hot arm of the actuator operated in a vacuum as compared to the elongated and rough surface of the actuator failed in air. This is due to the temperature in the failure region rapidly progressing through the range of temperatures that cause plastic deformation. Conversely, in a gas, the temperature increase is slower and not as sensitive to the applied current. Consequently, a larger plastic deformation can be achieved without destroying the hot arm.

In addition, the length of the hot arm which is affected is much greater in air than in vacuum. Air cooling allows for more of the hot arm structure to achieve a plastic deformation before failure. In a vacuum, much less of the hot arm reaches back bending temperatures, and the affected region is much smaller. Figures 4-12 and 4-13 show that the length of the hot arm affected by plastic deformation is greater than 100 μm in air versus less than 50 μm in vacuum.

The SPICE generated temperature profile also sheds light on the performance of a variant of the lateral thermal actuator. The operation of the double hot arm lateral thermal actuator is similar to the single actuator except a second 'hot arm' is added as

shown in Figure 4-14. Additionally, no current flows through the 'cold arm' because one terminal is not electrically connected. The double hot arm lateral thermal actuator provides greater deflection and force than a similarly sized single arm actuator [51].

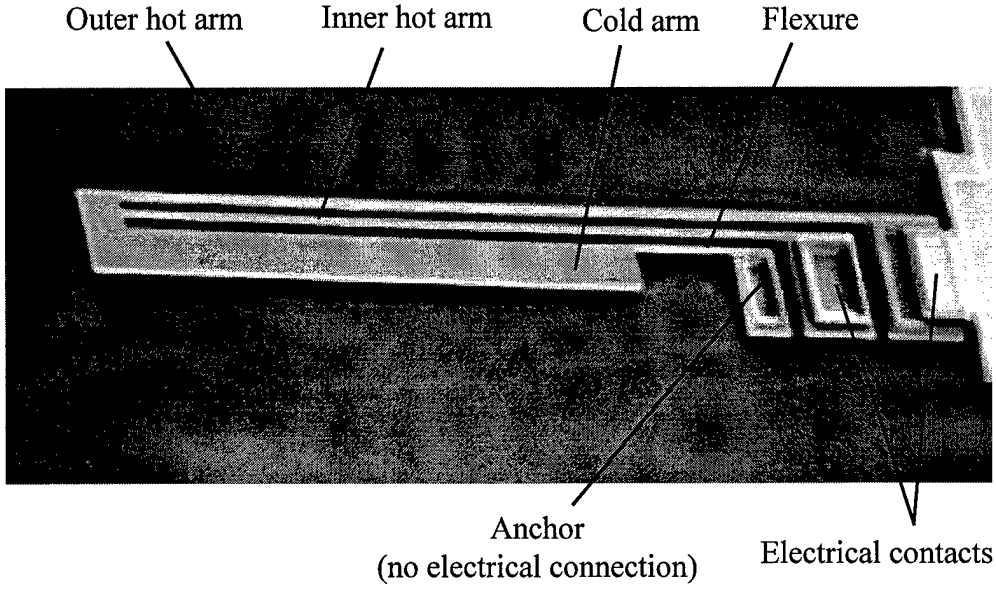
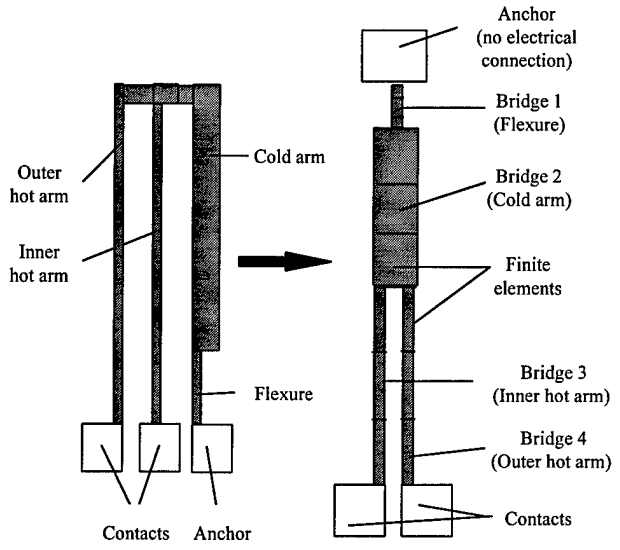
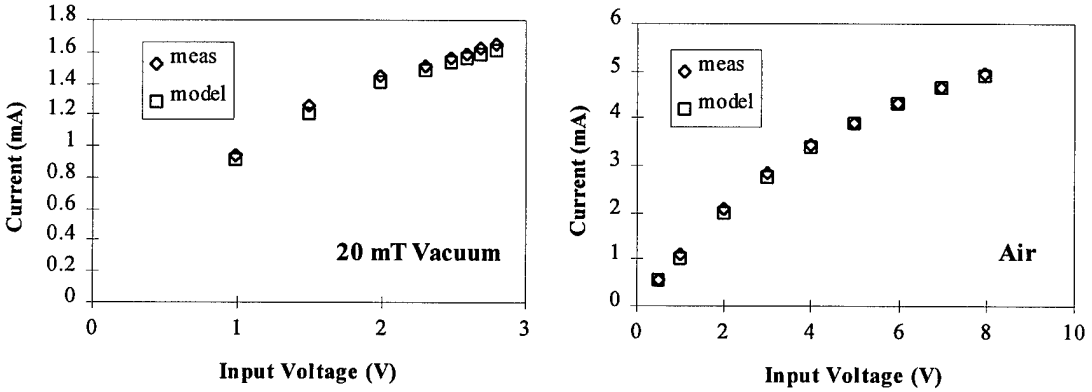


Figure 4-14. Double hot arm thermal actuator [51]. Note that the anchor for the cold arm/ flexure is not an electrical connection. Consequently, no electrical current flows through the cold arm/flexure.

A SPICE model of the double hot arm actuator was constructed to validate the ability of the model to analyze the more complex structure and to gain insight into the temperature profile. The model was constructed from the finite element decomposition shown in Figure 4-15 (a). The model very accurately predicted the I-V response of the double hot arm actuators as shown in Figure 4-15 (b).



(a)



(b)

Figure 4-15. (a) Finite element decomposition and (b) SPICE model versus measured I-V response for double hot arm lateral thermal actuator. The length/width/thickness of the hot arms were: 256/2.5/2 μm and 225/2.5/2 μm. The length/width/thickness of the cold arm and flexure were 176.5/14/2 μm and 27.5/2/2 μm, respectively.

Moreover, the temperature profile of the actuator demonstrated that the increased deflection of the double hot arm actuator is largely due to the increased cooling ability of the cold arm in this design. Unlike the single hot arm actuator, no electrical current flows through the cold arm in this design. Consequently, no heat generation due to ohmic

heating occurs, and the average temperature in the cold arm stays much lower. This, in turn, allows the double hot arm design to achieve a similar temperature difference between the hot arms and the cold arm as the single hot arm actuator. Table 4-6 shows the SPICE model maximum average temperatures for a double hot arm actuator.

In addition, the cold arm is better able to sink the heat flow from the two hot arms such that the average temperature in the hot arms does not reach failure any more rapidly than for the single arm actuator design in air or vacuum. In a vacuum, the measured current density in the hot arm (l,w,t = 200, 2, 2 μm) of a single hot arm actuator was 0.38 mA/μm^2 just prior to failure. The measured current density for a double hot arm actuator with similar sized hot arms (l,w,t = 225, 2.5, 2 μm and 256, 2.5, 2 μm) was 0.34 mA/μm^2 at the failure point. This indicates that the cold arm on the double hot arm actuator was nearly able to sink the heat from two hot arms as well as the cold arm in the single hot arm design which only had to cool one hot arm. Thus, the double hot arm design has a similar range of operating temperatures with the benefit of the greater force and deflection inherent with two hot arms as shown in Figure 4-16.

Table 4-6. SPICE Model Maximum Average Temperature of Double Hot Arm Lateral Actuator Components in Air and 20 mT Vacuum.

Component	Length/Width/Thick (μm)	Avg Temp (K) (Vacuum)	Avg Temp (K) (Air)
Outer hot arm	256/2.5/2	960	1200
Inner hot arm	225/2.5/2	870	1130
Cold arm	176/14/2	810	440
Flexure	28/2/2	470	310

A SPICE implementation to estimate the deflection of the piston micromirror has not yet been found due to its more complex geometry and thermo-mechanical interactions. However, an empirical relationship between average power and deflection for the piston micromirror can be incorporated into the model as a dependent voltage source. Preliminary investigation into using the electrothermal SPICE model to predict the power required for the onset of buckling has been encouraging. The temperature increase needed to cause thermal buckling, ΔT, can be estimated as [49]:

$$\Delta T = \frac{4\pi^2 I}{A\lambda L^2} \tag{4-18}$$

where I is the moment of inertia for the flexure, A is the cross-sectional area of the flexure, λ is the coefficient of thermal expansion of polysilicon, and L is the length of the suspended structure which is the sum of the lengths of two flexures and the diameter of the mirror plate. The temperature profile from the SPICE model was used to calculate the drive power required to raise the average temperature in the flexures to the buckling point. The SPICE model predicted the power required for buckling as 40 mW for the thermal piston micromirror described in Figure 4-10. This value compares well with the measured value of 37 mW.

Another useful insight provided by the SPICE model temperature profile is the ability to accurately predict the failure of the gold-silicon eutectic formed between the gold mirror plate and the polysilicon support plate. The melting point of the gold-silicon eutectic is approximately 363 °C. The temperature profile from the model was used to predict when the applied DC voltage and current would elevate the temperature on the

mirror plate to 363 °C. The model predicted that the interface between the four flexures and the mirror plate would be the first point to reach the eutectic failure point.

In order to validate the model, DC current was applied to several thermal mirrors to empirically determine the failure point. As predicted by the model, the gold failure was observed to consistently begin at the interface between the flexures and the mirror. Table 4-7 compares the measured failure voltage and current to the model predictions. The measured data shown in Table 4-7 is the average of five measurements.

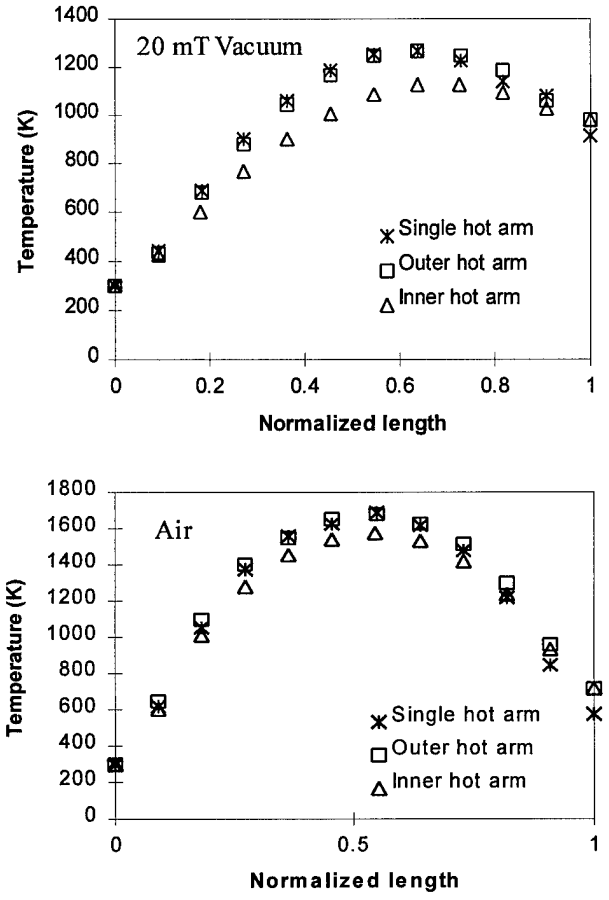


Figure 4-16. Comparison of SPICE model hot arm temperature profiles for single and double hot arm lateral actuators in (a) 20 mT vacuum and (b) air. The dimensions of the actuators are shown in Tables 4-5 and 4-6.

Table 4-7. Comparison of SPICE Model and Measured Voltage and Current Required to Cause Thermal Piston Mirror Failure.

Source	Environment	Applied Voltage	Current
Measured	20 mT	1.7	9.3
SPICE Model	20 mT	1.5	8.7
Measured	Air	3.9	18.6
SPICE Model	Air	3.7	18.1

*The length/width/thickness of the mirror flexures was 64/4/2 μm. The mirror plate had a diameter of 70 μm.

4.3.5. Limitations of the Parametric Model

The parametric model has been far more versatile and useful than originally envisioned; but it still has some key limitations. First, the model is only as good as the material and physical parameter inputs (i.e. in computer parlance GIGO -- garbage in . . . garbage out.) MEMS metrology is not as advanced a field as metrology for macroscale materials. Consequently many of the parameters used in the model have not been thoroughly researched for applicability at the micron level. In particular, high temperature effects on material parameters needs more work. Several of the key inputs such as thermal conductivity of polysilicon have not been researched for behavior at high temperatures. Some quantities such as TCR and resistivity of MEMS-specific processes have not been addressed at all as will be discussed in Chapter 5.

In addition, there is a great need for an electro-thermal-*mechanical* modeling system. The model works well in SPICE for electro-thermal modeling, but the ability to

mathematically model the thermo-mechanical behavior in the same simulation tool would be of great benefit. On a positive note, two of the leading firms in developing computer aided tool suites for MEMS designers have inquired about incorporating aspects of the parametric model and methodologies into an integrated electro-thermal-mechanical simulator [52,53].

4.4 Summary

Electrothermal SPICE models were developed for modeling and analyzing the response of polysilicon thermal actuators. Both empirical and parametric approaches to modeling were implemented to simulate the electrical load and deflection characteristics of a polysilicon lateral thermal actuator and a thermal piston micromirror. The parametric model was able to accurately predict the electrothermal response of thermally actuated devices and has excellent agreement with measured data and theory. The deflection predictions from the parametric model are only estimates due to the limited ability to perform complex thermo-mechanical analysis in SPICE. These models are particularly useful for investigating the performance of thermally actuated devices when driven by DC and pulsed inputs due to the complex and non-linear relationships between resistance, power consumption, and deflection.

The creation of the electrothermal SPICE models is a significant contribution to the development of integrated microsystems. The ability to simulate both the MEMS device and the control electronics in the same analysis package greatly improves the design process. Moreover, the parametric model allows the designer to gain some insight

into the expected performance of the microsystem prior to fabrication. The parametric model is now being evaluated by a leading MEMS software simulation company for possible incorporation into their product.

One area of further research identified during the course of developing the electrothermal SPICE models was the need to better understand the MUMPs fabrication process. The resistivity of the various MUMPs layers was of particular concern. Thus, the MUMPs resistivity and fabrication process were investigated as described in Chapter 5.

Chapter 5. MUMPs Resistivity and Fabrication Modeling

Metrology and fabrication modeling have become active areas of MEMS research due to the need to better understand and characterize the behavior of the materials used in micro devices. Many of the MEMS-specific fabrication processes such as MUMPs have not been thoroughly characterized in terms of the electrical, thermal, and mechanical properties of the various polysilicon layers.

The development of the electro-thermal SPICE model described in Chapter 4 necessitated an analysis of MUMPs resistivity in order to provide inputs for some of the key material parameters. In addition, AFIT researchers have observed anomalies in the behavior of some MUMPs fabricated structures which prompted an investigation into possible links between the fabrication process and variances in device resistance. The outcome of these research efforts are discussed in this chapter.

5.1 Determination of Temperature Coefficient of Resistivity for MUMPs *Poly 1*

One of the key parameters for electrothermal modeling of polysilicon actuators is the temperature coefficient of resistivity (TCR). The TCR of polysilicon has been shown to vary depending on the fabrication process [54]. The thermal actuators modeled in Chapter 4 were constructed from the intermediate polysilicon layer in the MUMPs process, *Poly 1*. Prior to this research effort, no estimate for the TCR of *Poly 1* had been published [39]. Consequently, the TCR of this polysilicon layer was determined empirically in a series of experiments based on previous work by Tai, et al. [42].

In a vacuum, R_b, the resistance of a polysilicon microbridge as a function of applied current, can be calculated as [42]:

$$R_b = \frac{2R_o}{Bl}\tan(\frac{Bl}{2}) \tag{5-1}$$

where B is defined as:

$$B = \sqrt{\frac{IR_o^{\,2}\alpha}{\kappa_p wtl}}\ . \tag{5-2}$$

For Equations (5-1) and (5-2), I is the current through the microbridge, R_O is the small signal electrical resistance, α is the TCR of polysilicon, and κ_p is the thermal conductivity of polysilicon. The length, width, and thickness of the microbridge are represented by l, w, and t, respectively.

A necessary condition for Equations (5-1) and (5-2) to hold true is that convection or free-molecule air conduction must be negligible [42]. Tai's work was carried out in a 2 μT vacuum which is significantly lower than the 20 mT vacuum used for MEMS research at AFIT. Consequently, the validity of these equations for a 20 mT vacuum must be established.

The total free-molecule conduction power, P_{fmc}, can be calculated as [42]:

$$P_{fmc} = \frac{1}{4}a\Lambda_0 Pwl\left(\frac{273.2}{T_s}\right)^{\frac{1}{2}}(T_c - T_s) \tag{5-3}$$

where a is the accommodation coefficient (a = 1 for this case), Λ_0 is the free molecule heat conductivity at 273.2 K, P is the pressure in mT, w and l are the width and length of the microbridge, T_C is the surface temperature, and T_S is the substrate and ambient temperature.

Consider a microbridge with a length of 200 μm and width of 10 μm, which is a representative size for an element in a thermal actuator. If nitrogen is the residual gas in the vacuum chamber, Λ_0 = 1.663 x 10^{-5} W cm^{-2} K^{-1} mT^{-1} [41]. The P_{fmc} for this microbridge in a 20 mT vacuum with T_S = 300 K and T_C = 1685 K is approximately 2.2 x 10^{-6} W which is negligible since it is three orders of magnitude lower than power dissipated due to ohmic heating which is modeled by Equations (5-1) and (5-2). T_C = 1685 K represents a worst-case scenario since it is the melting point of silicon, and the bridge would have failed before reaching this temperature. Lower temperatures result in less P_{fmc}; therefore, P_{fmc} is considered negligible for polysilicon thermal actuators in a 20 mT vacuum, and Equations (5-1) and (5-2) are applicable.

Once the appropriateness of the Tai model was established, the change in resistance of polysilicon microbridges of varying lengths and widths was measured as a function of applied current in a vacuum. Figure 5-1 shows an array of microbridges used to collect I-V data.

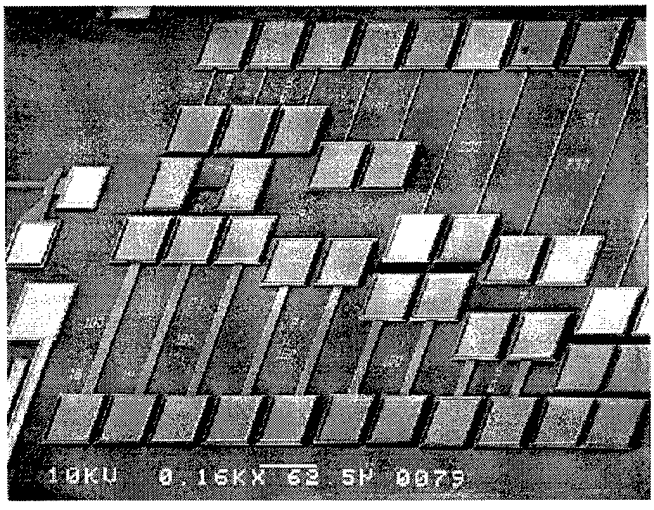


Figure 5-1. Microbridge array used for determination of *Poly 1* TCR. (MUMPs 19)

The measured I-V data was plotted and Equations (5-1) and (5-2) were then used to fit the plots. The only two parameters in Equations (5-1) and (5-2) which were not known or could not be directly measured were κ_p and α. The value of κ_p for phosphorus doped LPCVD polysilicon has been widely reported as approximately 30 $Wm^{-1}K^{-1}$ [41,42,48]; and this value was used for κ_p. Therefore, α was the only unspecified fitting parameter. The data was collected from MUMPs runs 9 and 16-21. The measured data was plotted and (5-1) was adjusted to fit the plot by varying α. Using this technique, α was estimated to be 1.25 x 10^{-3} K^{-1} for *Poly 1* in the MUMPs process which compares favorably to results for similar polysilicon processes [42,48].

Table 5-1 lists the parameter values for several microbridges, and Figure 5-2 compares the measured and calculated I-V characteristics for the microbridges where $V = IR_b$.

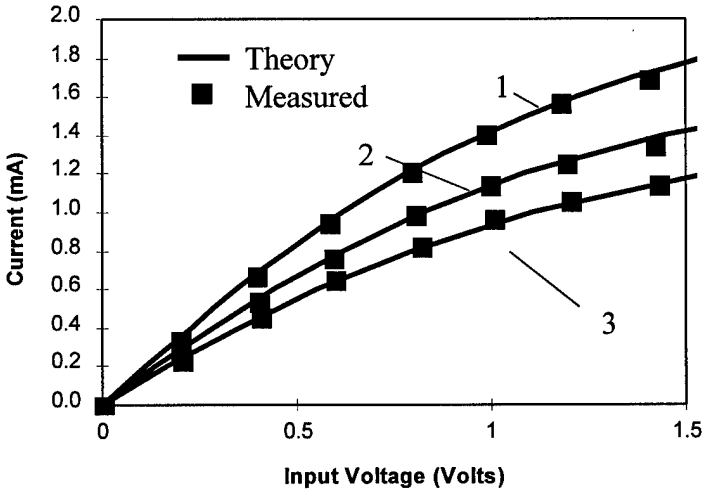


Figure 5-2. Measured versus calculated I-V characteristics for polysilicon microbridges in 20 mT vacuum.

Table 5-1. Parameter Values Used For Calculating I-V Plots in Figure 5-2.

Microbridge	R_O (ohms)	l (μm)	w (μm)	t (μm)	κ_p [42,48] ($W\ m^{-1}\ K^{-1}$)	α (K^{-1})
1	550	214	2	2	30	1.25×10^{-3}
2	690	271	2	2	30	1.25×10^{-3}
3	840	329	2	2	30	1.25×10^{-3}

5.2 MUMPs Resistivity Modeling

The electrical resistivity, ρ, is also a key parameter for the effective modeling and characterization of polysilicon micromachines. The resistivity is used in the electro-thermal SPICE model and is required to calculate the resistance of devices as a function of geometry. Consequently, the resistivity of the MUMPs polysilicon was investigated through a TSUPREM fabrication model and analysis of measured data.

5.2.1 Discrepancies Between Published and Measured Resistivity Values.

Unlike the TCR, values for the resistivity of the various MUMPs layers are published with each run. However, significant differences (> 25%) between the published values and measured results have been observed, particularly for small linewidths. Table 5-2 compares the published sheet resistance, R_S, values against measured sheet resistances for a 2 μm wide, 100 μm long polysilicon (*Poly 1*) microbridge over several MUMPs fabrication runs.

Table 5-2. Measured *Poly 1* R_S for Released, 2 μm Wide Microbridges vs. Published Values.

MUMPs Run	Published Sheet Resistance [39,55] (ohms/sq)	Measured Sheet Resistance (ohms/sq)
9	10.88	5.1
10	12.6	7.5
18	9.77	7.5
19	6.90	6.5
20	10.80	7.6

Variations were also noted between the resistivity behavior as a function of the MUMPs layer as well as the linewidth. For example, the resistivity of unreleased *Poly 0* and *Poly 1* microbridges tends to decrease as the linewidth decreases. While unreleased *Poly 2* microbridges tend to have fairly constant resistivity until the line width decreases below ~ 6μm, at which point the resistivity increases.

Discussions with MUMPs fabrication engineers revealed that the published resistivity values are taken from measurements made from 40 μm wide test structures on a test wafer which is processed with the production wafers [39]. No attempt is normally made to measure the resistivity variation as a function of linewidth. MCNC did perform subsequent in-house testing, and their results also demonstrated a link between linewidth variation and resistivity [39].

5.2.2 Resistivity As a Function of Linewidth for MUMPs

After brainstorming sessions between AFIT researchers and MCNC, lateral diffusion of phosphorus was identified as a likely cause of the decreased resistivity of small linewidth, unreleased *Poly 0* and *Poly 1* structures. In the MUMPs process, the

doping of the polysilicon layers is accomplished through thermal diffusion of the dopant from the oxide layers to the surrounding polysilicon layers [17]. For structures with a large width to thickness ratio, *w/t*, most of the doping is achieved from diffusion of phosphorus from the oxide layers directly above and below the polysilicon (vertical diffusion). However, for polysilicon structures for which the width is comparable to the thickness, the diffusion of phosphorus through the sidewall (lateral diffusion) becomes significant and can impact the overall resistivity as shown in Figure 5-3.

Poly 2 does not generally experience lateral resistivity effects because there are no anneal cycles after the *Poly 2* layer is patterned. Consequently, a *Poly 2* structure does not have the opportunity for diffusion through the sidewalls. In fact, the increased resistivity of small linewidth *Poly 2* structures is due to the absence of lateral diffusion. As the linewidth decreases, the high resistivity of the undoped sidewalls becomes more significant because of the reduced cross-sectional area.

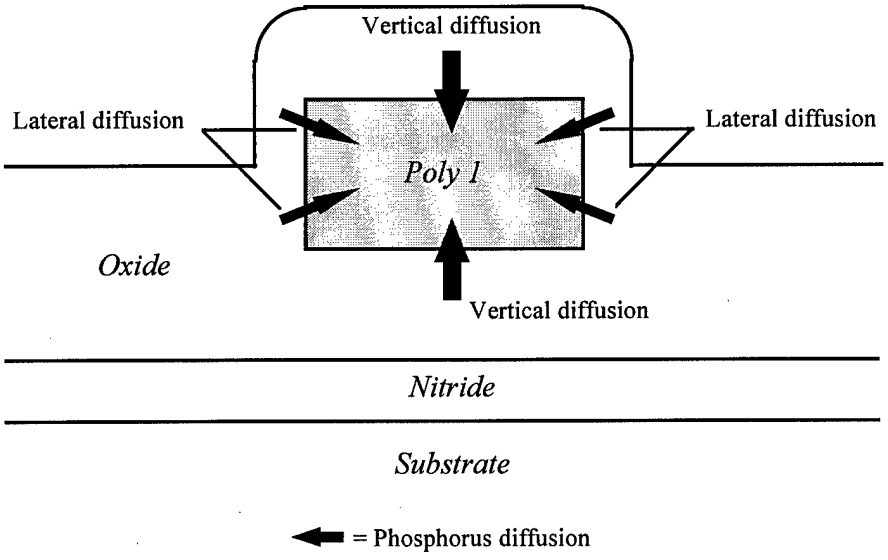


Figure 5-3. Lateral diffusion in MUMPs *Poly 1*.

5.2.3 TSUPREM Model of MUMPs Fabrication Process

In order to validate the lateral diffusion theory, a TSUPREM model of the MUMPs fabrication process was created. TSUPREM is a microelectronics fabrication simulation tool developed by Stanford University [56]. In addition, a set of microbridge test arrays of varying lengths and widths were designed to gather quantitative, empirical data to compare with the qualitative insights provided from TSUPREM.

The TSUPREM model of the MUMPs fabrication process was based on details provided by MCNC [17,39]. A listing of an example TSUPREM input file is in the Appendices. Not all of the MUMPS fabrication steps were modeled because the scope of this research effort was only to investigate the phosphorus diffusion profile as a function of linewidth. Hence, only the processing steps which are critical to phosphorus diffusion are included explicitly in the model. Table 5-3 lists the various steps in the MUMPs process as modeled in TSUPREM.

The TSUPREM simulation demonstrated that lateral diffusion is a key contributor to the decreased resistivity of small linewidth structures in unreleased *Poly 0* and *Poly 1*. Figure 5-4 shows a comparison of the dopant concentration distribution for *Poly 1* microbridges as a function of linewidth. For a 2 μm wide bridge, the lateral diffusion causes the entire structure to be doped uniformly. As the linewidth increases, the impact of lateral diffusion becomes less significant as shown in Figure 5-4.

Table 5-3. MUMPs Fabrication Process As Modeled in TSUPREM.

Process Step	Thickness (μm)	P Doping Conc. (cm^{-3})	Temp (°C)
1. Start P-doped silicon substrate	-	1×10^{21}	-
2. Deposit *Nitride*	0.6	-	-
3. Deposit *Poly 0*	0.5	-	-
4. Pattern *Poly 0* with RIE	-	-	-
5. Deposit *Oxide 1*	2.0	4.2×10^{20}	-
6. First Anneal (1 hour)	-	-	1050
7. Deposit *Poly 1*	2.0	-	-
8. Deposit oxide cap	0.2	4.2×10^{20}	-
9. Second Anneal (1 hour)	-	-	1050
10. Pattern *Poly 1* with RIE	-	-	-
11. Deposit *Oxide 2*	0.75	4.2×10^{20}	-
12. Third Anneal (1 hour)	-	-	1050
13. Deposit *Poly 2*	1.5	-	-
14. Deposit oxide cap	0.2	4.2×10^{20}	-
15. Fourth Anneal (1 hour)	-	-	1050
16. Pattern *Poly 2* with RIE	-	-	-

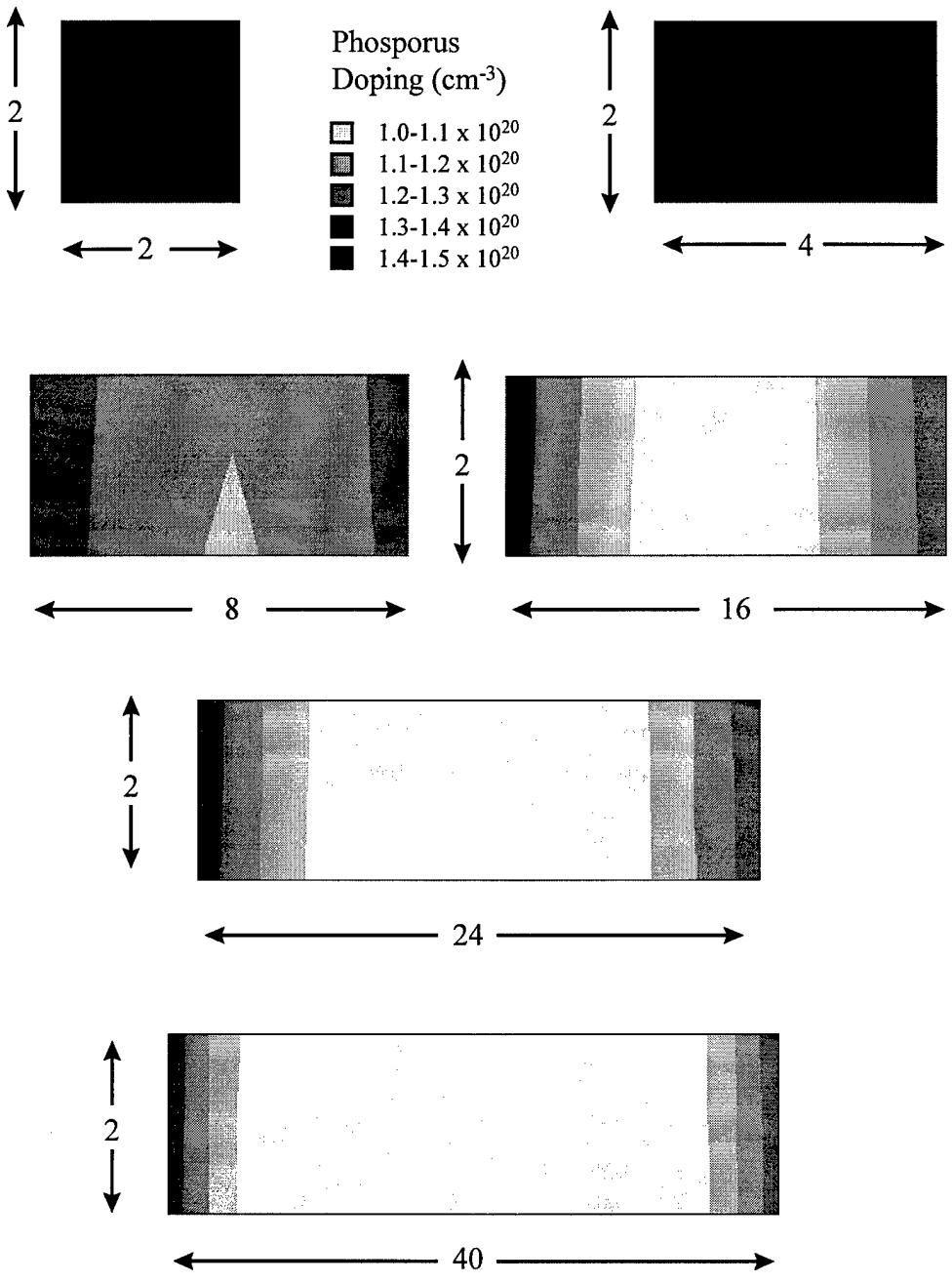


Figure 5-4. TSUPREM cross-section view of phosphorus doping profile of *Poly 1* microbridges of various widths. All physical dimensions are in μm. Note that the drawings are not to scale.

The results of the TSUPREM simulation of *Poly 0* are similar to the *Poly 1* example in Figure 5-4 except the impact of lateral diffusion is mitigated by the fact that *Poly 0* is only one-fourth the thickness of *Poly 1* (0.5 vs. 2.0 μm). The small thickness in combination with the fact that *Poly 0* undergoes all four anneal cycles allows for a high concentration of phosphorus to vertically diffuse throughout the *Poly 0* layer. Consequently, the extra doping provided by lateral diffusion does not influence the resistivity of *Poly 0* as significantly as *Poly 1*.

The TSUPREM simulation of *Poly 2* line structures is shown in Figure 5-5 and shows no lateral diffusion. Moreover, the TSUPREM model correctly predicted that *Poly 2* resistivity would be higher than *Poly 1*. This is due to *Poly 2* having only one anneal cycle as compared to three cycles for *Poly 1*. The extra anneal cycles allow more phosphorus to diffuse into the *Poly 1* layer which reduces the resistivity. Lateral diffusion also reduces the *Poly 1* resistivity since two of the anneal cycles occur after the layer is patterned.

Arrays of microbridges were designed to collect empirical data to confirm the TSUPREM model predictions. Figure 5-6 shows an example test array. All three MUMPs polysilicon layers were investigated, and the results matched the predictions generated by the TSUPREM model including the high resistivity of small linewidth *Poly 2* structures. Figure 5-7 shows the measured sheet resistance as a function of linewidth for the various MUMPs polysilicon layers over several fabrication runs.

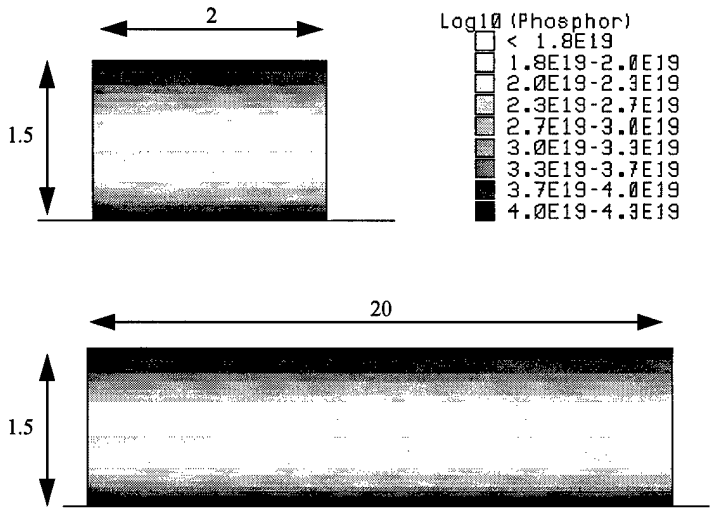


Figure 5-5. TSUPREM cross-section view of phosphorus doping profile of *Poly 2* microbridges. All physical dimensions are in μm. Note that the drawings are not to scale.

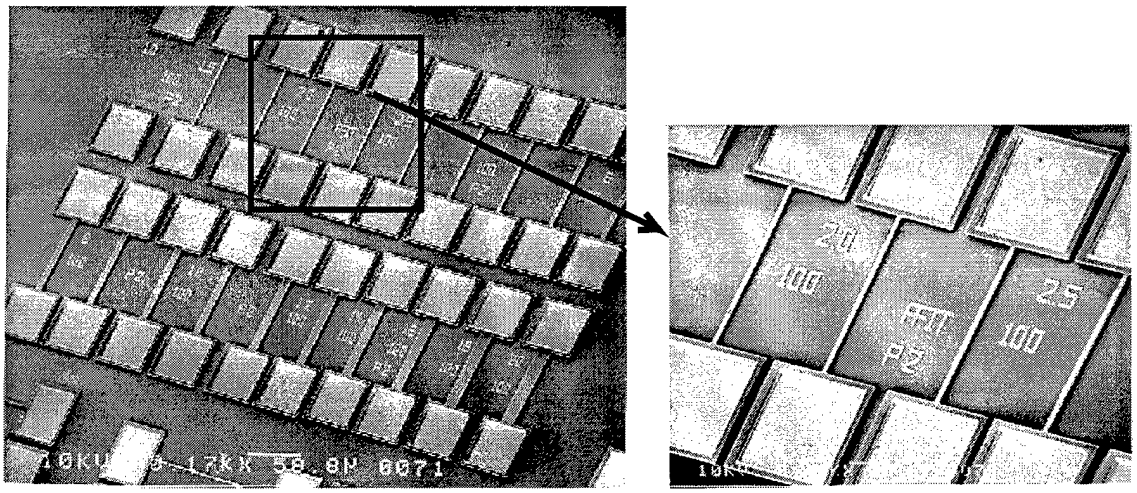


Figure 5-6. *Poly 2* test bridge array used for validating TSUPREM model of lateral diffusion affects on MUMPs 19 polysilicon microbridges. *Poly 0* and *Poly 1* test arrays are similar.

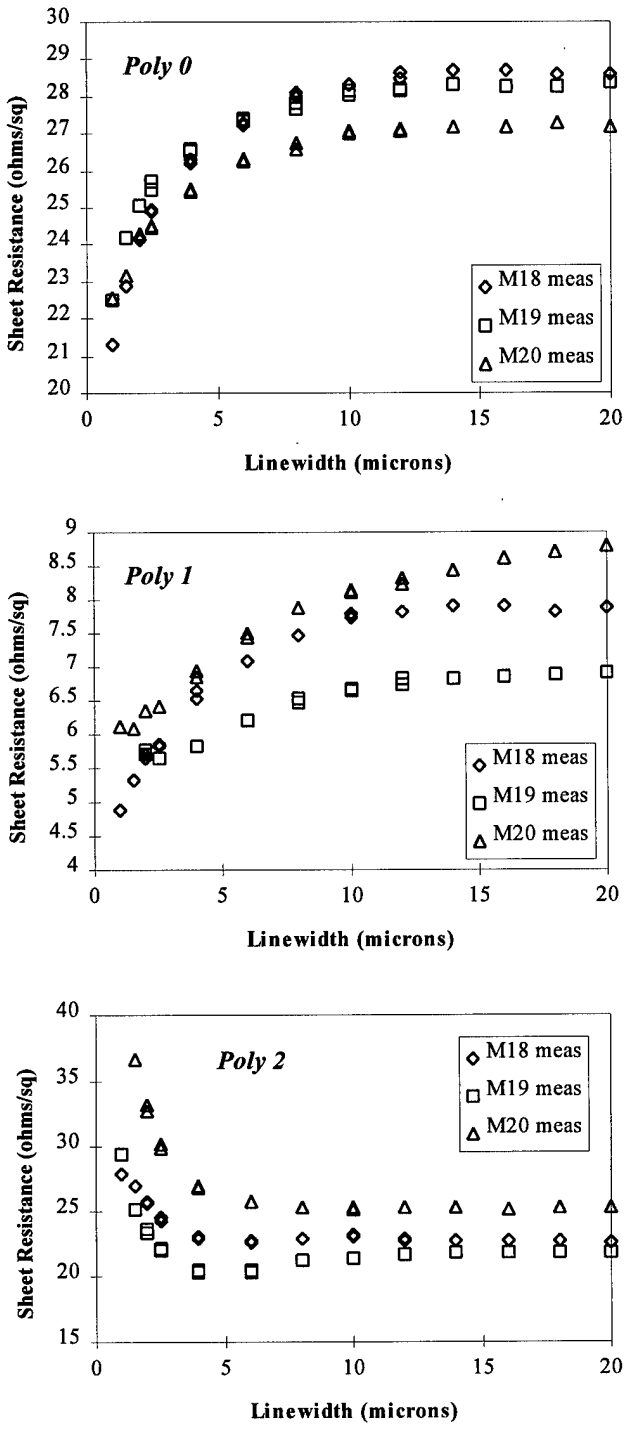


Figure 5-7. Measured variation in MUMPs polysilicon sheet resistance, R_S, as a function of linewidth. The resistance measurements were taken from unreleased microbridges.

The relative impact of lateral doping on *Poly 0*, *Poly 1*, and *Poly 2* was estimated by comparing the TSUPREM calculation of the phosphorus doping concentration between a 2 μm bridge and a 20 μm bridge of the same length. The doping concentration was used to estimate the resistivity, ρ, of the bridge material using empirical charts [57]; and the resistivity was then used to calculate the sheet resistance, R_S, as:

$$R_S = \rho / layer\_thickness \quad \text{(ohms/sq)}. \tag{5-4}$$

The results are shown in Table 5-4 along with a comparison of the measured results.

Table 5-4. Comparison of TSUPREM and Measured Data of Unreleased Microbridges.

	MUMPs Run	MCNC Rs (ohms/sq)	Measured Rs w = 20 μm (ohms/sq)	Measured Rs, w = 2 μm (ohms/sq)	Change in Rs (%)	TSUPREM Predicted Change (%)
Poly 0	18	26.3	28.6	24.1	16	15
	19	27.6	28.4	25.0	12	
	20	25.8	27.2	24.3	11	
Poly 1	18	9.77	7.9	5.7	27	28
	19	6.9	6.9	5.73	17	
	20	10.8	8.8	6.35	27	
Poly 2	18	15.0	22.6	25.8	14	15
	19	17.8	21.8	23.5	8	
	20	20.0	25.3	30.0	18	

The model and measured data also illuminated several non-intuitive truths about the fabrication process. Originally, the increased resistivity of small linewidth *Poly 2* structures was thought to be a result of neighboring *Poly 1* structures depleting *Oxide 2* of phosphorus which would then result in less dopant available for *Poly 2*. However, the TSUPREM model showed that the presence of *Poly 1* marginally *increases* the amount of phosphorus available for *Poly 2* doping.

After the TSUPREM results contradicted the initial hypothesis on *Poly 2* doping, a more thorough investigation was conducted, and it was discovered that the TSUPREM model was correct. The presence of *Poly 1* increases the doping of *Poly 2* by holding dopants in *Oxide 2* during the 3rd anneal cycle. In the MUMPs process, a thin oxide cap is placed over the die prior to the anneals, but no overpressure is used to prevent phosphorus atoms from escaping through the surface of the die [39]. Consequently, the phosphorus content at the top of *Oxide 2* is depleted through phosphorus outgassing and sublimation during the anneal. This outgassing reduces the amount of phosphorus available for subsequent doping of *Poly 2*. When *Poly 1* is present, the gradient of phosphorus diffusion from *Oxide 2* into *Poly 1* entices more of the phosphorus to remain near the top of *Oxide 2* and increases the amount of phosphorus available for *Poly 2* doping.

A special test array of microbridges was fabricated in order to gather empirical data. The test array contained pairs of *Poly 2* microbridges of varying widths. Each microbridge pair contained a *Poly 2* bridge and another *Poly 2* bridge with a *Poly 1* rectangle beneath it as shown in Figure 5-8. The *Poly 1* rectangle was not attached to the *Poly 2* bridge and was anchored to the substrate so it would not float away after release. Table 5-5 compares the resistance of the bridge pairs which shows a slight decrease in resistance for the *Poly 2* bridges with underlying *Poly 1* which is what was predicted by the TSUPREM model.

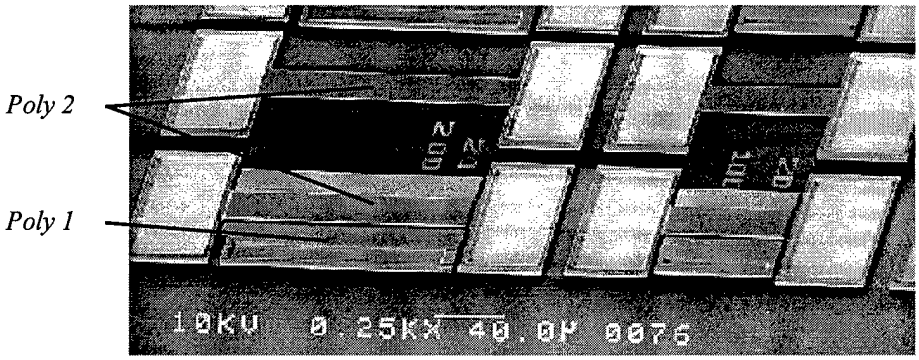


Figure 5-8. MUMPs 19 *Poly 2* bridge and *Poly 2* bridge with underlying *Poly 1*.

Table 5-5. Comparison of *Poly 2* Bridge R_S vs. *Poly 2* Bridge over *Poly 1* R_S.

Linewidth (μm) (MUMPs 19 data)	*Poly 2* R_S (ohms/sq)	*Poly 2* over *Poly 1* R_S (ohms/sq)
6	20.66	19.95
10	20.79	20.35
20	21.06	20.31

Measured data also shed light on the potential impact of RIE etching on the resistivity of small linewidth *Poly 2* structures. RIE induced lattice damage has been shown to increase the sheet resistance of polysilicon layers if the damage is not repaired through annealing [6,7]. Unlike the other polysilicon layers, there is no post-RIE anneal for *Poly 2*. Hence, any RIE induced damage is not repaired. Unfortunately, TSUPREM does not account for crystal structure damage due to RIE [56], and the model could not be used. As a result, a MUMPs test die to empirically investigate the magnitude of the link between RIE damage and *Poly 2* resistivity was developed.

Several of the test die were annealed to measure if the resistivity of the *Poly 2* would decrease. The MUMPs test die contain *Poly 2* test bridges and have no gold on the

die which allows them to be safely annealed. Prior to annealing, the sheet resistance of the test bridges was measured. The die were then baked in a furnace for one hour at 1050 °C to match the anneal conditions used by MCNC. In addition, a steam atmosphere was used to grow an oxide cap in order to minimize the sublimation of phosphorus into the air.

The results of the extra anneal indicate that RIE damage is not a significant contributor to the resistivity of *Poly 2*. Figure 5-9 compares the measured sheet resistance before and after the one hour anneal. The difference between the two curves is due to sublimation (outgassing) of phosphorus during the anneal. The sheet resistance did not change significantly for die which were annealed for another hour (2 hours total).

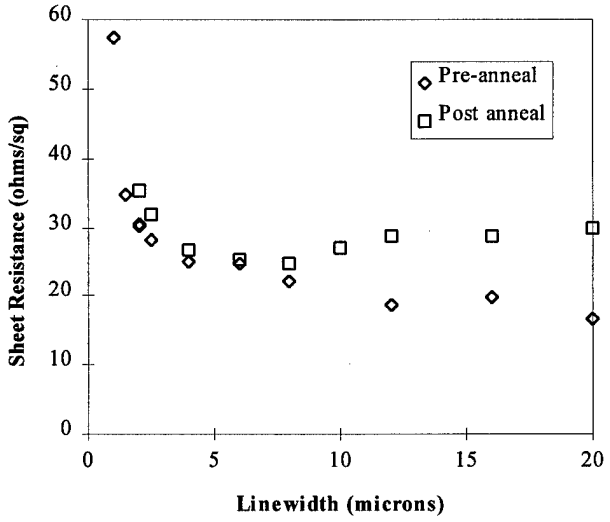


Figure 5-9. Comparison of pre and post anneal sheet resistance for unreleased, MUMPs 21 *Poly 2* test bridges. The test bridges were annealed for one hour in a steam atmosphere at 1050 °C.

A second anneal experiment was performed to validate the link between the absence of lateral diffusion and *Poly 2* resistivity. A second set of test die were annealed, but this time phosphorus sources were placed into the furnace to allow for dopant diffusion. The pre and post anneal sheet resistances for these *Poly 2* test bridges are shown in Figure 5-10. The sheet resistance of the *Poly 2* decreased after the diffusion. Moreover, the lateral diffusion effects are demonstrated by the fact that the sheet resistances of the small linewidth test bridges are now lower than that of the wider bridges as in the case for *Poly 0* and *Poly 1*. A TSUPREM simulation also demonstrates the effect of lateral diffusion as shown in Figure 5-11. The impact of lateral diffusion is seen by comparing the doping profiles shown in Figure 5-5 and 5-11. The post-diffusion profiles show significant dopant concentration near the sidewalls.

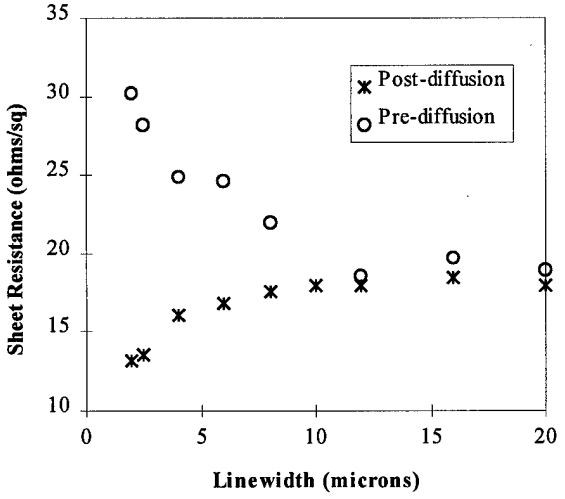


Figure 5-10. Comparison of pre and post diffusion sheet resistance for unreleased, MUMPs 21 *Poly 2* test bridges. The test bridges were annealed with a phosphorus diffusion source for one hour at 950 °C.

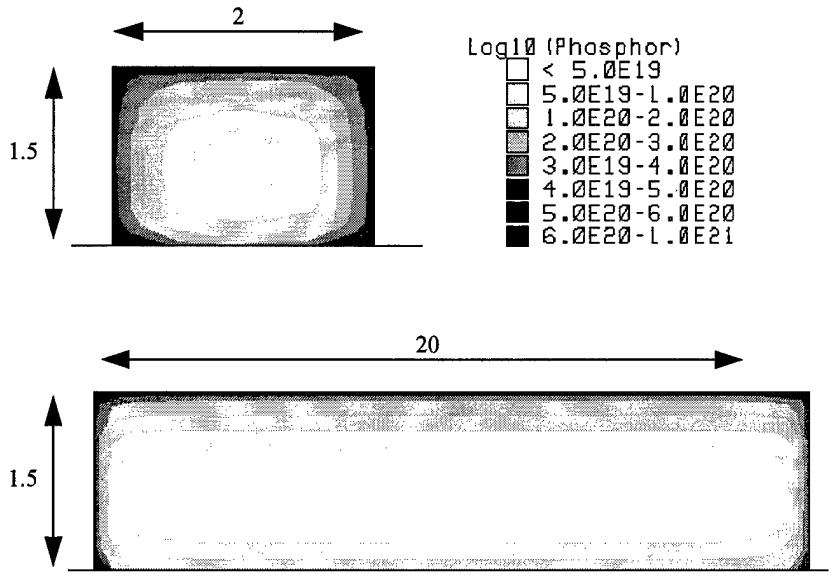


Figure 5-11. TSUPREM cross-section of *Poly 2* test bridge after a one hour phosphorus diffusion at 950 °C.

Finally, the TSUPREM model also provided other revelations about the MUMPs process. First, virtually all of the doping of a polysilicon layer is accomplished in the anneals prior to deposition of subsequent layers. Hence, the presence of *Poly 2* has little impact on *Poly 0* or *Poly 1* doping; and likewise, the presence of *Poly 1* has little impact on *Poly 0* doping. Also, the oxide layers are thick enough that the phosphorus atoms do not diffuse across the entire width of the oxide layer, but the distribution of phosphorus atoms is altered. Consequently, the presence of a lower lying polysilicon layer does have an impact on the resistivity of higher layers; but it is not a large influence. Topology is another method whereby a lower lying polysilicon layer can impact the resistivity of a higher layer. The topology induced by the device structure can alter the amount of or, in the case of *Poly 2*, create lateral diffusion.

5.2.4 Post Release Resistivity Effects

The sheet resistance of the MUMPs polysilicon microbridges increases after release due to etching of the polysilicon. HF is used as the release etchant for MUMPs die because it rapidly etches oxide; but it also will etch polysilicon, albeit much more slowly. A ten minute etch in HF is capable of destroying a 1 μm polysilicon linestructure. In some respects, the release etch acts to reduce the impact of the lateral diffusion phenomena described in the previous section since the increase in resistance of smaller linewidth structures is proportionally greater than that of larger linewidths. For a fixed reduction in width and thickness, the percentage reduction in the cross-sectional area of a small linewidth structure will be greater than for a larger structure. Consequently, the resistance of the small linewidth structure will increase more rapidly than that of a larger linewidth structure. Figure 5-12 compares the pre release and post release sheet resistances of *Poly 1* and *Poly 2* for a specific MUMPs run.

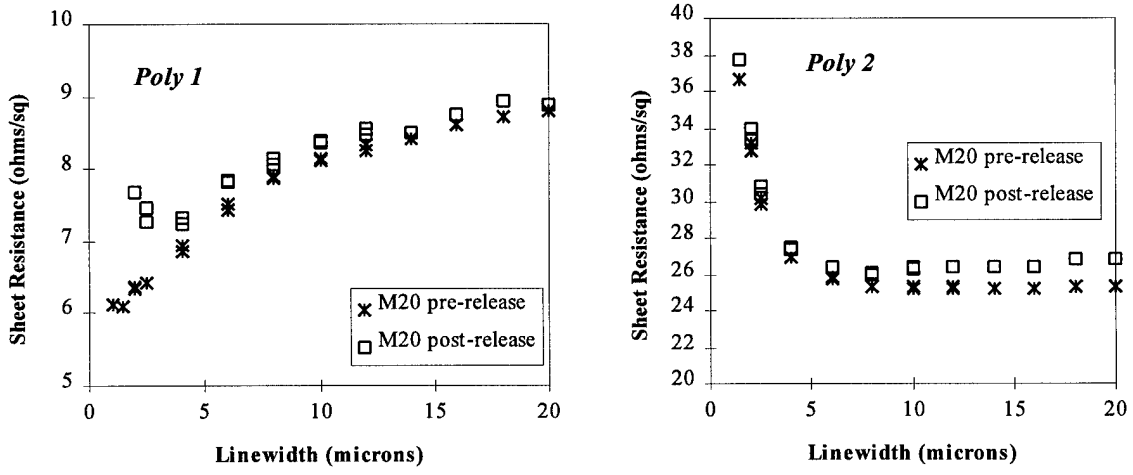


Figure 5-12. Comparison of pre and post release sheet resistance for *Poly 1* and *Poly 2*. The release etch was 2 minutes 30 seconds in 49% HF.

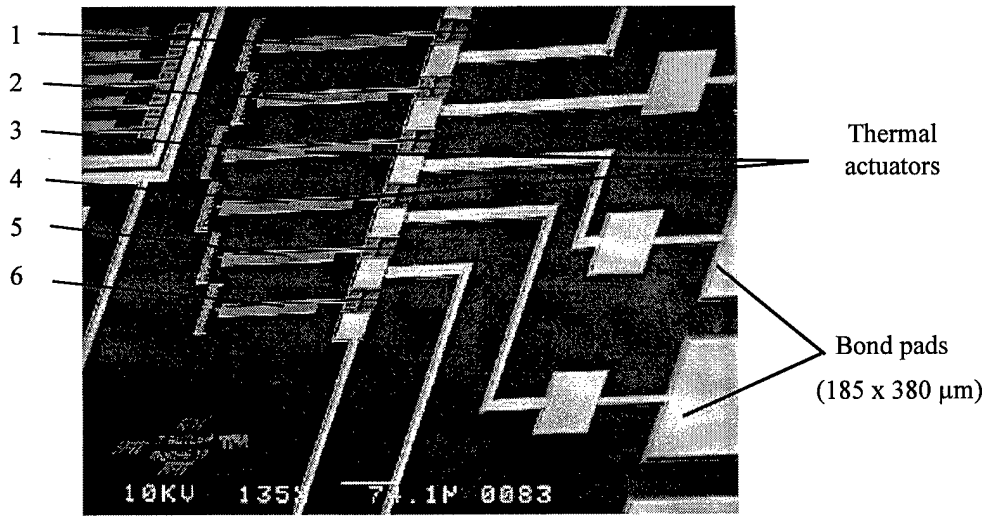
The sheet resistance will also significantly increase if the polysilicon bridge is electrically connected to gold. The amount of resistance increase is proportional to the quantity of gold that is connected to the polysilicon structure. *Poly 0* is most impacted by this electrochemical etch phenomena. After release, the color of *Poly 0* line structures connected to large bond or probe pads changes from yellow to brown. In addition, these *Poly 0* linestructures have greatly increased resistance as shown in Table 5-6. In fact, narrow *Poly 0* structures become virtually unusable as current carrying devices because of the elevated resistance.

Table 5-6. Impact of Electrochemical Etch on *Poly 0*.

	MUMPs 19		MUMPs 20	
Linewidth (μm)	Before Release (ohms/sq)	After Release (ohms/sq)	Before Release (ohms/sq)	After Release (ohms/sq)
2	25	120	24.3	125
4	26.5	65	25.5	64
8	27.7	40	26.7	44
12	28.2	42	27.1	42
20	28.3	36	27.2	38

Poly 1 and *Poly 2* line structures are also subject to the electrochemical etch phenomena. Figure 5-13 shows an array of *Poly 1* lateral thermal actuators connected to wire bond pads. A second array of actuators was located in the center of the same die with no connection to bond pads. Table 5-7 compares the resistance of the actuators connected to bond pads before and after release. The array of actuators not connected to

wirebond pads exhibited less than 2 percent increase in resistance. Similar results were obtained for *Poly 2* lateral actuators.



Actuator No.	Hot Arm l/w/t (μm)	Cold Arm l/w/t (μm)	Flexure l/w/t (μm)
1,3	321/2.5/2	272/16/2	50/2.5/2
2,4	294/2.5/2	244/16/2	50/2.5/2
5	257/2.5/2	207/16/2	50/2.5/2
6	230/2.5/2	180/16/2	50/2.5/2

Figure 5-13. Array of MUMPs 18 *Poly 1* lateral thermal actuators used for measuring electrochemical etch impact on device resistance.

Table 5-7. Electrochemical Etch Impact on *Poly 1* Lateral Thermal Actuators Attached to Large, Gold Wirebond Pads.

Actuator Number (see Figure 5-13)	Pre-release Resistance (ohms)	Post-release Resistance (ohms)	Resistance Increase (%)
1	968	1315	37
2	901	1285	42
3	972	1416	45
4	903	1271	41
5	799	1081	35
6	725	987	36

MEMS wiring is also subject to the effects of electrochemical etching. The physical construction of the MEMS wiring plays a factor in the extent of electrochemical etching. Table 5-8 shows the pre and post resistance measurement of resistance for 4 different types of commonly used MEMS wires. Each wire is 8500 μm long and is connected to a 185 x 380 μm wirebond pad at each end. Both the *Poly 1* and *Poly-2/Gold* wires are stapled to the substrate every 100 μm. The increase in resistance due to electrochemical etching is significant, particularly for thin *Poly 0* lines.

Table 5-8. Electrochemical Etch Effects on MUMPs 16 Wiring.

MUMPs Wire Type	Length (μm)	Width (μm)	Thickness (μm)	Pre-Release Resistance (K ohms)	Post-Release Resistance (K ohms)
Poly 0	8500	2	0.5	98.3	125
Poly 0	8500	16	0.5	13.8	15
Poly 1	8500	16	2.0	3.8	3.9
Poly 2/Gold	8500	16/10	2.0/0.5	0.05	0.05

After release, the *Poly 0* and *Poly 1* lines displayed the discoloration characteristic of electrochemical etching. The discoloration was most pronounced near the bond pads and gradually tapered off with increasing distance from the pads. The discoloration was not visible through at 40x magnification at distances of greater than 600 μm from the gold bond pads.

Wirebonding also affects the magnitude of the electrochemical etch. The addition of a wirebond greatly increases the mass of gold physically connected to the thermal actuator. Consequently, the electrochemical etch is greatly magnified if the thermal

actuators are wirebonded *prior* to release. The result can be dramatic as entire arrays of piston micromirrors (electrostatic and thermally actuated) have been observed to fail because they were wirebonded before release and the electrochemical etch weakened the flexures. Lateral thermal actuators can also be destroyed if released after wirebonding. This is an important result because these devices are fragile, and wirebonding after release requires extreme care.

5.3 Polysilicon Thermal Actuator Trimming and Response

After discussing resistance characteristics during fabrication and release, the final resistance characteristic investigated was the impact of operation. The most pervasive impact of operation is the permanent change in resistance for polysilicon thermal actuators subjected to high current density. The electrical nature of driving polysilicon thermal actuators closely parallels polysilicon resistor trimming which is a technique for intentionally altering the resistivity of polysilicon resistors.

5.3.1 Theoretical Model of Polysilicon Resistor Trimming

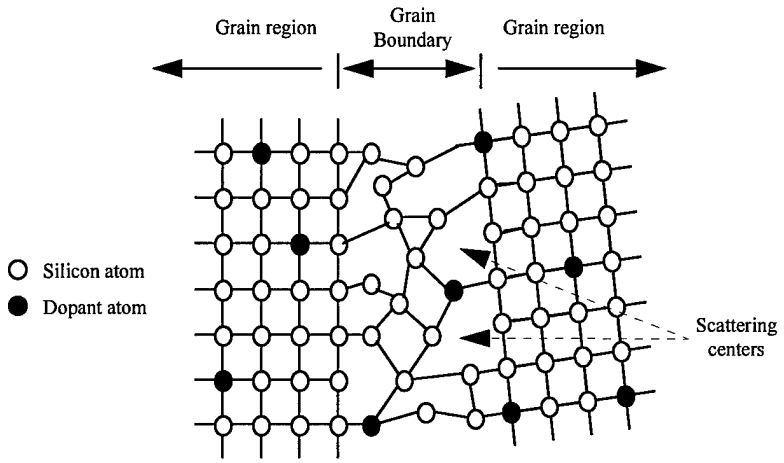
A theoretical model has been proposed to explain the trimming response of polysilicon resistors [45], and this theory can also be used to explain the observed behavior of polysilicon thermal actuators. Resistor trimming is used in the microelectronics industry to precisely adjust the resistance of highly doped polysilicon resistors. By heating the resistor through electrical current pulses or a laser source, the resistance can be trimmed by as much as 50 % [45].

The initial reduction in resistance is caused by changes in the makeup of the polysilicon grain boundary. The most important mechanism for resistance reduction is elimination of scattering centers which occur at the grain boundary [45]. There are large numbers of dangling bonds at the grain boundary due to the number or defects in the crystal. These dangling bonds and defects produce scattering centers which reduce the carrier mobility. When a high current is applied, the grain boundary heats up more rapidly than the grain region due to the increased number of carrier collisions induced by the scattering centers. Hence, the area around the grain boundary reaches the melting point before the rest of the crystal grain structure.

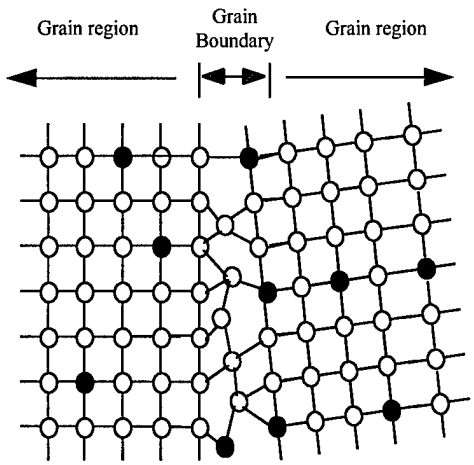
Moreover, after the current or laser pulse is removed, the boundary region remains molten longer than the bulk grain region. Upon solidification, the bulk grain on either side acts as a seed for re-crystallization which allows the boundary region to become more crystalline and shrinks the disordered region. The permanent reduction in the region of disorder allows for greater carrier movement through the boundary which results in significantly less electrical resistance [45]. Figure 5-14 shows a pictorial representation of the current pulse trimming effect on the grain boundary.

A second resistance phenomena is resistance recovery. After trimming, a small component (less than 5 %) of the resistance loss can be recovered by applying a current pulse of smaller magnitude than the trim pulse. If the recovery pulse creates enough local heating, some of the loosely bound dopants near the boundary escape and diffuse into the grains. This diffusion (or segregation) of dopants results in the formation of new scattering centers at the boundary which in turn increases resistance. The resistance

increase or recovery is however, much less than the initial decrease achieved from the trimming operation. The total amount of recoverable resistance is limited by the number of loosely bound dopants in or near grain boundaries. Once these dopants have been released, further recovery pulses will not produce an increase in resistance [45].



(a) Grain boundary before current trimming



(b) Reduced grain boundary after current trimming

Figure 5-14. Pictorial representation of polysilicon grain boundary (a) before and (b) after current pulse trimming (after Feldbaumer, et al. [45]). Note the reduction in the grain boundary and dangling bonds and scattering centers after current trimming.

5.3.2 Conformance of Polysilicon Thermal Actuators to Resistor Trimming Theory

Polysilicon thermal actuators are essentially resistors which are partially unconstrained and free to thermally expand. Thus, the theoretical model presented in the previous section should apply to thermal actuators as well as resistors. This supposition appears to be true as evidenced by measured data collected from lateral thermal actuators.

Several lateral thermal actuators were tested to determine if the resistance would decrease after applying current pulses of increasing amplitude. Figure 5-15 shows the change in resistance of lateral thermal actuators as a result of applying current pulses of at least 10 seconds long. Similar behavior was observed for lateral actuators of varying construction as well as for the microbridges used in the TCR and lateral diffusion studies. The typical resistance reduction for lateral actuators operating in vacuum was approximately 10 percent before device failure. In air, the actuator resistance could be trimmed by up to 15 percent. This additional range of trim values is due to gas cooling which allows for more of the actuator to reach a high enough temperature to experience resistance trimming effects.

Measured data also demonstrated the reversible nature of the resistance. Figure 5-16 shows a plot of the resistance recovery phenomena for a lateral thermal actuator. The 'Trim cycle' data in Figure 5-16 represents the resistance after each current pulse was applied. The final trimming pulse had an amplitude of 4.6 mA and the actuator resistance decreased from a starting value of 647 ohms to a trimmed value of 580 ohms.

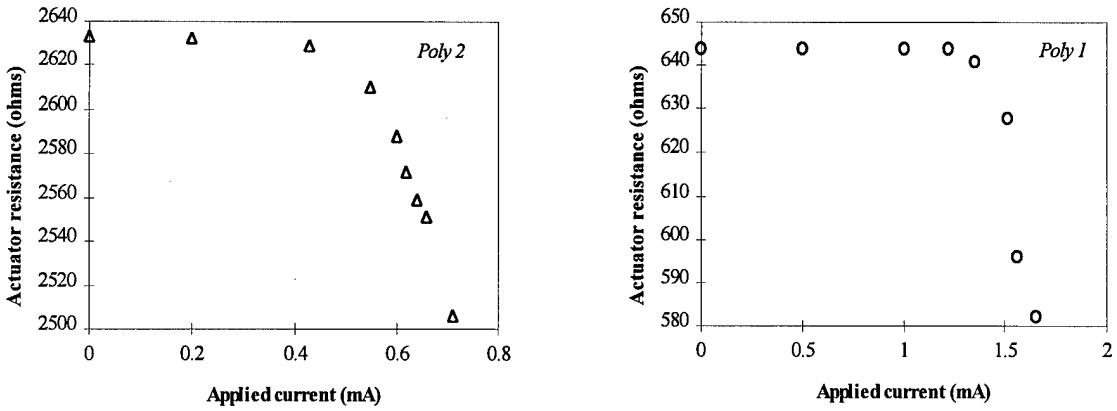


Figure 5-15. MUMPs 9 *Poly 1* and *Poly 2* lateral thermal actuator resistance trimming as a function of applying current pulses in 20 mT vacuum. Both actuators have hot arm, cold arm, and flexure dimensions (length, width, thickness) of 200/2/2, 170/14/2, and 30/2/2 μm.

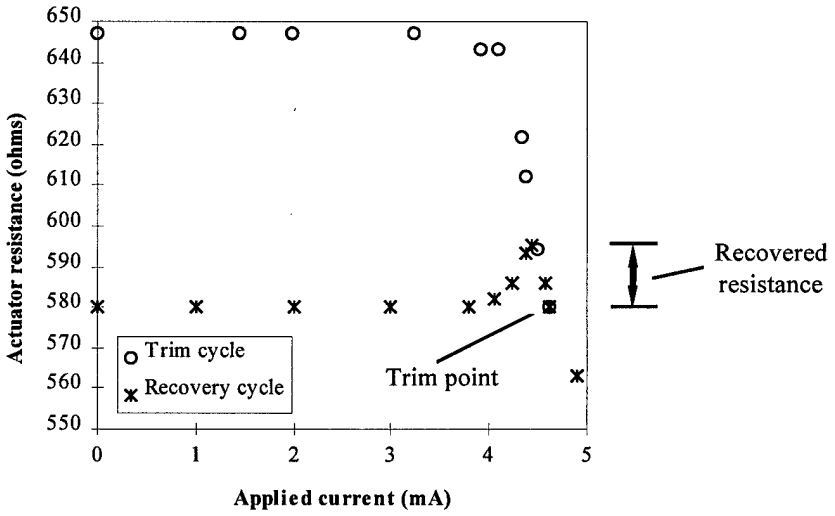


Figure 5-16. Recovery characteristics of MUMPs 9 polysilicon thermal actuator operated in air. The thermal actuator was constructed from *Poly 1* and has hot arm, cold arm, and flexure dimensions (length, width, thickness) of 200/2/2, 170/14/2, and 30/2/2 μm. The variation in resistance is significantly reduced after trimming as shown by the recovery cycle data. Also note that the resistance of the actuator continues to decrease when the recovery cycle pulse exceeds the initial trim point which in effect creates a new trim point.

Following the trim cycle, current pulses were again applied to see how much of the actuator resistance could be recovered as shown by the 'Recovery cycle' data in Figure 5-16. In this example, approximately 2.5 percent of the resistance could be recovered. For a wide range of lateral actuators tested, the magnitude of the recovery was typically a maximum of 3 percent of the original actuator value before trimming. This applied for both vacuum and air environments. The recovered resistance disappeared if the initial trim current amplitude was applied again. If the initial trim current was exceeded, the resistance of the actuator decreased below the initial trim value (as shown in Figure 5-16), and a new trim resistance was established.

5.4. **Design Impacts of Polysilicon Resistance Characteristics**

The impact of variations in resistivity can be significant to the MEMS designer using MUMPs. Small linewidths have significantly different resistivity than large linewidths. In addition, the use of diffusion as a mechanism for phosphorus doping is subject to a wide range of process parameter variations. Hence, the sheet resistance can and does change from fabrication run to fabrication run. Moreover, the type of etchant and length of etch time can impact the resistance of a particular device as well as whether or not it is attached to a large gold surface. Wirebonding requirements also need to be factored into the design equation. The bottom line is that using small linewidths (< 5 μm) is not advisable if precise resistance is essential. Designing for a specific resistance in the MUMPs process is difficult; however designs, such as thermal actuators, that use relative

resistances will be successful as long as there is tolerance for resistance variations due to fabrication and post-processing.

The resistance trimming nature of polysilicon thermal actuators during operation also has impacts for the MEMS designer. First, the designer must be aware that high current densities will cause an irreversible change in the actuator resistance. This can be mitigated by either ensuring that the applied current does not exceed an acceptable threshold or by trimming the actuators before operational use to minimize the resistance variation. A rule of thumb is to never apply a current greater than two-thirds of the amount which would cause failure in a non-trimmed thermal actuator. This rule was adopted since none of the thermal actuators tested suffered an appreciable loss of resistance in air or vacuum when operated at less than two-thirds of the maximum tolerable current. For high current operations, trimming the actuators before use allows for consistent operation since the resistance variation over the entire range of operation is less than 3 percent as opposed to 10-15 percent for non-trimmed actuators.

Back bending is another area for which resistance trimming must be taken into account. The phenomena which cause the trimming effect occurs before back bending can be visually discerned. Hence, the amount of current required to visually back bend or cause a plastic deformation in the actuator will always cause a permanent and significant change in the device resistance. Furthermore, empirical results show that repeatedly operating the actuator at currents less than but within ~ 20 % of the current required for back bending will eventually induce small plastic deformations. Using the resistance trimming model discussed earlier, the increase in TCR at the grain boundaries due to

dopant segregation results in increasing localized heating at the grain boundaries. This heating effect increases as dopants leave the boundary in response to repeated applications of high current. Hence, the increased local heating due to the gradual segregation of dopants may eventually elevate the local thermal expansion to the point that plastic deformation occurs.

5.5 Summary

An in-depth analysis of MUMPs resistivity characteristics was conducted in order to gain a better understanding of MUMPs fabricated MEMS devices. The MUMPs process is one of the most popular MEMS fabrication processes in the United States and is the primary MEMS foundry used by researchers at AFIT. The MUMPs process uses LPCVD polysilicon, and the resistivity of LPCVD polysilicon is known to vary depending on fabrication and post-processing.

The first published estimate of the temperature coefficient of resistivity (TCR) for the MUMPs *Poly 1* layer was established as 1.25×10^{-3} K^{-1}. This value is critical to thermal modeling of polysilicon thermal actuators fabricated in MUMPs and is now in use by other MEMS researchers.

Furthermore, the sheet resistance and resistivity of all the MUMPs layers was shown to be a function of linewidth due to lateral diffusion. Small linewidth *Poly 0* and *Poly 1* structures have reduced resistance due to increased doping while small linewidth *Poly 2* structures have higher resistance due to the absence of lateral diffusion. A

TSUPREM simulation of the MUMPs process was developed to model resistivity effects. The model was validated with measured results from test structures.

Finally, a theory for the trimming of thermal actuator resistance during operation was proposed. This theory is based on a polysilicon resistor trimming model and has very good agreement with measured data.

The knowledge of polysilicon behavior gained through this investigation can be used to enhance the electrothermal models presented in Chapter 4 and to develop better MEMS devices. A principal benefit of improved MEMS models and devices is the ability to better design integrated MEMS and CMOS systems as will be discussed in Chapter 6.

Chapter 6. Functional Integration of MEMS and CMOS

6.1 Merits of MEMS/CMOS Integration

The discussion in Chapters 1-5 is focused on MEMS specific fabrication, design, and modeling; however, MEMS devices are not likely to reach their full potential unless they are integrated with microelectronic control and processing circuits [7]. Integration of MEMS with electronic control circuits at the integrated circuit level will maximize the size and performance advantages associated with microsystems. In addition, the development of microelectronic control schemes which tolerate or take advantage of the physical and mechanical nature of MEMS is also desirable.

The work presented in this and subsequent chapters explores methods of functionally and physically integrating MEMS with other microfabrication technologies such as CMOS. The first area of investigation was the development of CMOS-based control circuits for automating the movement of MEMS. Consequently, electronic control systems were developed to position and operate several of the MEMS devices discussed in Chapter 3 such as the scanning and rotating micromirrors. The high force, low power dissipation, and CMOS compatible voltage and current requirements of the improved thermal actuator arrays makes these designs particularly suited to integration with digital CMOS technology.

In addition, the use of pulse modulation and average power for positioning the thermal actuators was investigated and implemented. The use of pulsed inputs allows the

development of flexible control systems which can take advantage of the physical characteristics of MEMS.

6.2 Voltage Amplitude Control and Implementations

The first type of CMOS control systems developed were based on voltage amplitude control. The two target MEMS devices were the scanning micromirror and the rotating micromirror employing thermal actuators. The key to the voltage amplitude control schemes is to vary the magnitude of the voltage applied to the actuator arrays driving these optical components. Varying the applied voltage can be used to control the position of the actuators and hence the optical device [31,36]. Different voltage amplitude schemes were used for the scanning mirror and the rotating mirror due to the different types of control systems needed for each device.

6.2.1 Voltage Amplitude Control of Scanning Micromirror

For the scanning micromirror, a software program running on a computer takes user inputs and converts them to positioning commands. A standard computer I/O card is used to control a digital-to-analog (D/A) converter which translates the digital positioning command into an analog voltage to drive the scanning mirror. Figures 6-1 and 6-2 show the scanning micromirror and the basic interfaces in the control system.

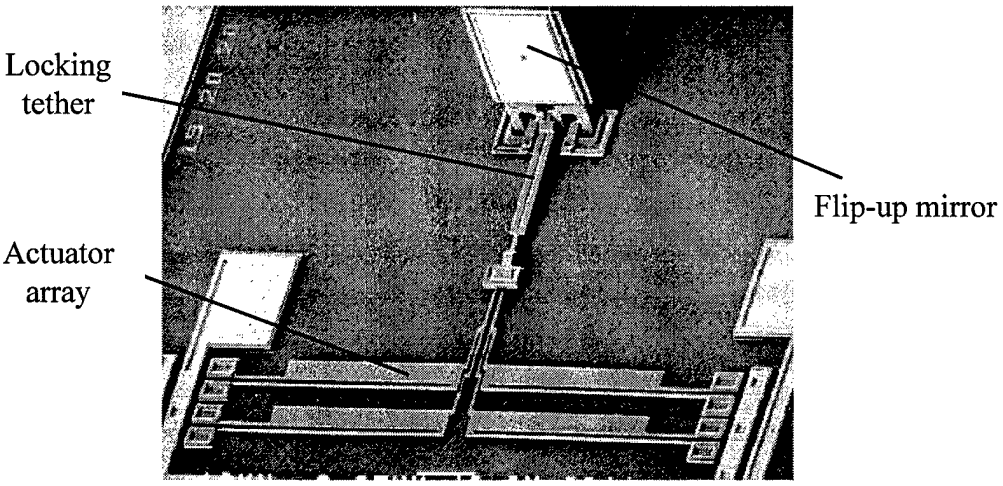


Figure 6-1. Scanning micromirror system.

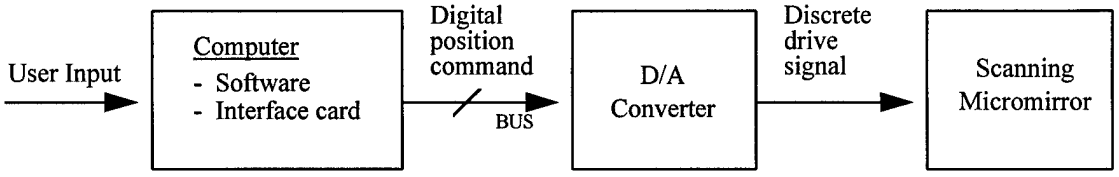


Figure 6-2. Scanning micromirror and block diagram of position control system.

The positioning commands are based on an empirically derived relationship between applied voltage and mirror plate movement. This empirical relationship was determined by measuring the deflection of the actuator array and mirror plate in response to a fixed input voltage. The data was plotted, and a best fit curve was used to generate the equation used in the software program. The performance of a scanning mirror driven by a 4 element drive array is shown in Figure 6-3. There is little deflection below 1 volt

because the current flow is not sufficient to heat the thermal actuators. Above 4 volts, the mirror deflection is limited by mechanical interference in the design of the micromirror.

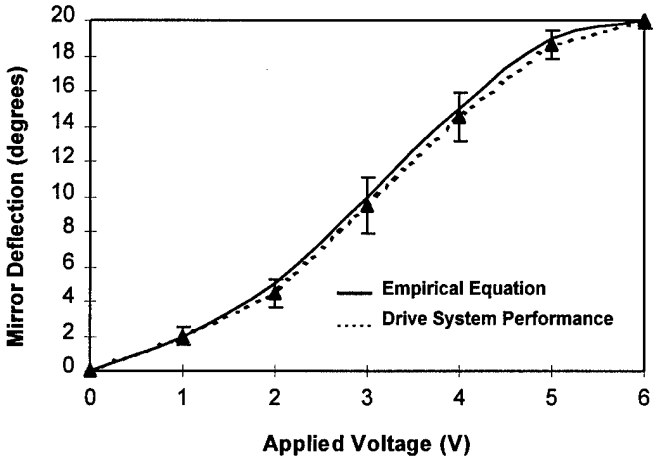


Figure 6-3. Mirror deflection versus applied voltage for scanning micromirror using 4 element drive array. Maximum power dissipation at 6 volts was 90 mW.

The drive system was effective in relative positioning of the scanning mirror in the sense that the mirror plate deflection would increase or decrease as commanded. The positioning of the actuator array was consistent, but the tolerances in the design of the micromirror hinges allowed too much play in the movement of the mirror plate. Consequently, the positioning of the plate was not as precise as desired as demonstrated by the RMS error bars in Figure 6-3. Another limitation of this control scheme was the inability of the D/A converter to drive large arrays due to the increased current demands of large actuator arrays. The largest array successfully employed had 4 elements.

The control system shown in Figure 6-2 is also able to drive electrostatic micromirrors which can be operated with less than 10 volts. The low voltage mirrors discussed in Chapter 3 were effectively driven with this system. This system is

particularly well-suited for this application because the D/A converter is able to provide a wide range of voltages for precisely positioning the mirror plate, and the electrostatic mirrors do not require significant current drive.

6.2.2 Voltage Amplitude Control of Rotating Micromirror

The rotating micromirror has different control requirements than the scanning mirror. Unlike the scanning mirror, the actuator arrays used in the rotating mirror are not required to hold the mirror position. Instead, they are used as a motor to position the rotating base. Therefore, the rotating mirror does not need to have the range of precision voltages required for the scanning mirror design. In addition, the arrays in the rotating micromirror are larger and require more power. The inability of the D/A scheme to drive large loads necessitated a different approach to controlling the rotating micromirror.

For the rotating mirror, a CMOS ASIC was designed which has large output drivers and a digital interface as shown in Figure 6-4. One of the advantages of integrated circuit design over MEMS design is the availability of tools for rapidly prototyping circuits. Using the VHSIC Hardware Description Language (VHDL), the ASIC controller layout was developed and tested with minimal manual effort. The ASIC was fabricated using the ORBIT 2 μm CMOS fabrication process.

The controller has three input select lines which will allow up to eight outputs to be addressed. The ACTIVATE signal is used to set the logic level for the selected output, and LOAD is a positive-edge triggered signal which latches the data on the select and

ACTIVATE lines into the controller. The synchronous RESET signal forces all of the outputs to '0'.

The output drivers are sized to provide varying levels of current drive. SPICE was used to determine the transistor sizing in the CMOS output drivers needed to position thermal actuator arrays of up to 10 elements. The actuator arrays were modeled using the empirical electrothermal SPICE model described in Chapter 4.

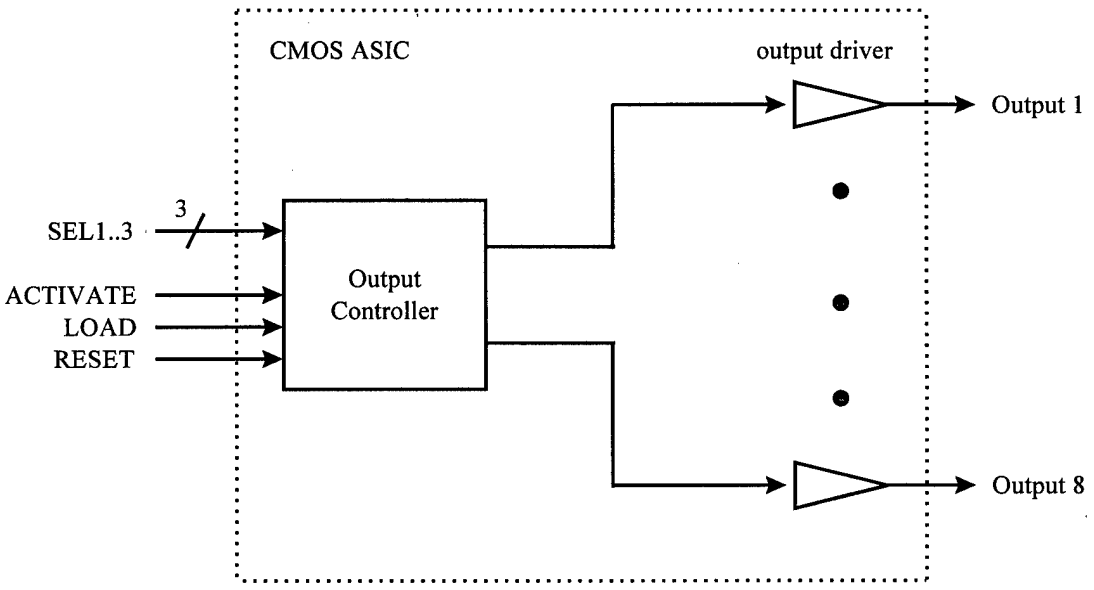


Figure 6-4. Block diagram of CMOS ASIC.

Figures 6-5 and 6-6 show the rotating micromirror and a block diagram of the voltage amplitude control system. In this design, the computer accepts user inputs for positioning the mirror and sends control signals to the CMOS controller via a computer interface card. The controller then selects the proper output channel and drives the actuator array. The mirror is able to rotate through a range of approximately 210 degrees. The micromotor can move the mirror through the entire 210 degree range in 200 steps.

This results in a positioning resolution of slightly greater than 1 degree. This scheme worked well for the rotating micromirror as the controller was normally able to move the mirror to the commanded positions with less than 3 degrees of error. The error increases if the actuator arrays are overdriven and backbend out of position or if the input power fluctuates enough to alter the deflection of the arrays so that the step size varies.

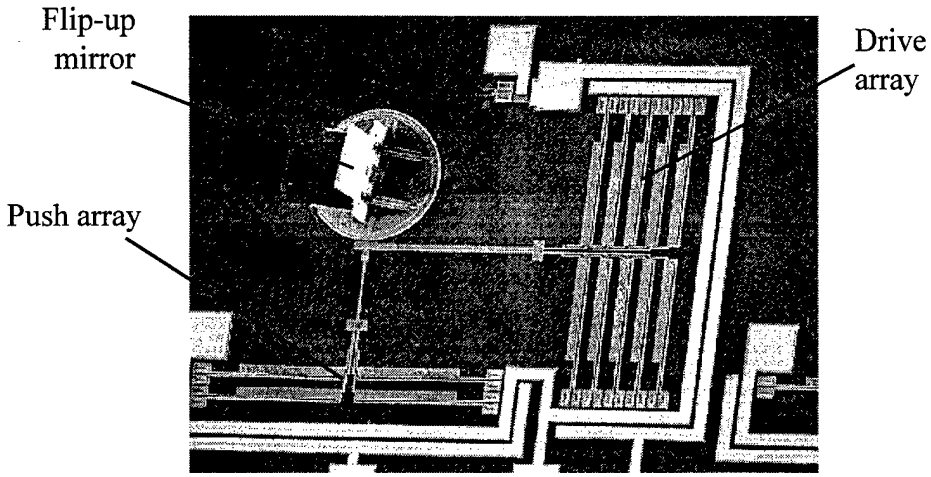


Figure 6-5. Rotating micromirror system.

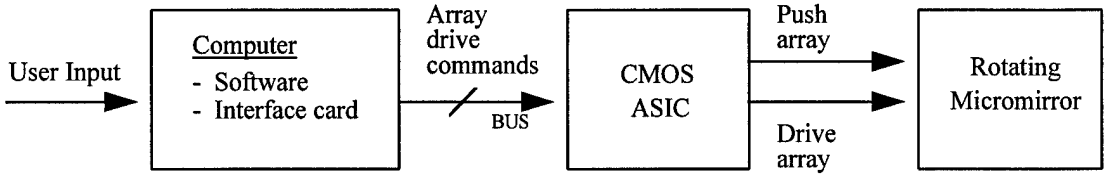


Figure 6-6. Rotating micromirror and block diagram of the position control system.

A disadvantage of this control scheme is the need for multiple supply voltages in order to minimize power dissipation. The drive array in the rotating mirror is normally

much larger and requires more voltage and power than the push array. The DC voltage used for the drive array is usually high enough to damage or even destroy the push array. As a result, separate DC drive voltages are often used for the two arrays which adds complexity and overhead to the design. A single drive voltage can be used by increasing the size of the push array so that it will operate at a higher voltage without overheating. However, this solution results in unnecessary power dissipation.

6.3 Pulse Modulation Control for Thermal Actuators

The desire to create a control methodology that would meet the requirements of both the scanning and rotating micromirrors led to the investigation of a pulse modulation scheme. A control system capable of meeting the requirements of both mirror designs should provide the fine positioning resolution needed by the scanning mirror along with the current drive required by the rotating mirror. Other desirable attributes are minimum power dissipation and the use of a single supply voltage. Pulse modulation was found to meet all of these requirements and was implemented to control both types of mirrors.

The key to pulse modulation control of thermal actuators is to exploit the thermal time constant of the device. When the period of the pulsed drive signal is much less than the thermal time constant of the device, the actuator does not have time to dissipate the heat generated by current flow. Consequently, the actuator retains its deflected position as if driven by a DC voltage. The drive pulse can be varied in width and/or amplitude to achieve a desired deflection. This situation is analogous to the refresh cycle of a dynamic memory cell in which the electrical capacitance is periodically refreshed to maintain the

memory state. The average input power is the key parameter for determining the deflection of a thermal actuator driven with a pulsed signal.

6.3.1 Average Power Response of Thermal Actuators

A series of experiments were conducted to gain insight into the behavior of thermal actuators when driven by a pulsed input. The deflection characteristics of lateral thermal actuators and piston thermal micromirrors were measured. Analysis of the data demonstrated that the actuator deflection was a function of the device temperature; and the temperature was in turn a function of the average input power when driven by either a DC or pulsed input.

6.3.1.1 Lateral Thermal Actuators

A test array of lateral thermal actuators was used to measure the I-V and transient response of the devices. Initially, the deflection and power dissipation characteristics of the actuator were measured by applying a DC voltage and recording the actuator tip deflection and current draw. The transient response of the lateral actuators was then measured using a laser source, PIN diode detector, and digital oscilloscope as demonstrated in Chapter 4. Using this technique, the lateral actuators were observed to have a maximum operating frequency of less than 2 KHz. When driven by signals above 10 KHz, the actuator deflected to a fixed position and movement could not be visually detected. Consequently, 100 KHz was chosen as the pulse frequency for driving the lateral actuators to ensure the pulse frequency was much greater than the thermal response of the device.

Next, the response of the lateral actuators to a pulsed input was investigated. In the first experiment, the pulse width of the drive signal was fixed and the pulse amplitude was increased until the actuator achieved a fixed deflection of 8 μm. The period of the input signal was 10 μs. This procedure was repeated for several pulse widths, and the average power for each scenario was calculated as:

$$P_{AVG} = \frac{V^2}{R}\left(\frac{PULSE\_WIDTH}{PULSE\_PERIOD}\right) \tag{6-1}$$

where V was the pulse amplitude and R, the actuator resistance, was determined from the DC measurements. The resistance of the thermal actuator is a function of the average applied power regardless of whether a DC or pulsed signal is used. Hence, the resistance of the actuator for a specific deflection is the same for DC and pulsed inputs.

The lateral actuator tip deflection was also found to be a function of the average applied power. Figure 6-7 shows the results for a lateral actuator in a 20 mT vacuum. In this example, pulse width modulation was used. A wide variety of lateral actuators of different lengths and construction were tested and produced results similar to those shown in Figure 6-7.

Figure 6-8 shows a comparison of the deflection versus average power for a different lateral thermal actuator in air. In this case, the pulse width was fixed and the pulse amplitude of the drive signal was varied to drive the thermal actuator through the full range of deflection. The correlation between the average input power and the deflection for both the DC and pulsed signals is evident.

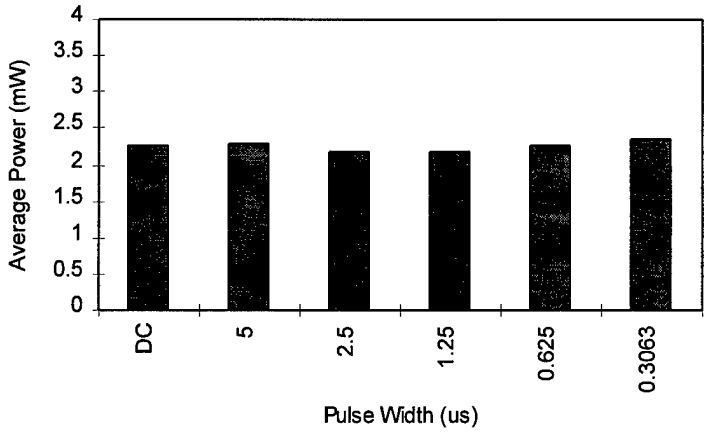


Figure 6-7. Average power required for 8 μm deflection of MUMPs 9 lateral thermal actuator in 20 mT vacuum. The resistance of the actuator when deflected to 8 μm was measured as 960 ohms. The pulse period was 10 μs. The length/width of the actuator hot arm, cold arm, and flexure were 200/2 μm, 170/14 μm, and 30/2 μm. The vacuum pressure was 20 mT. The thickness of the polysilicon was 2μm.

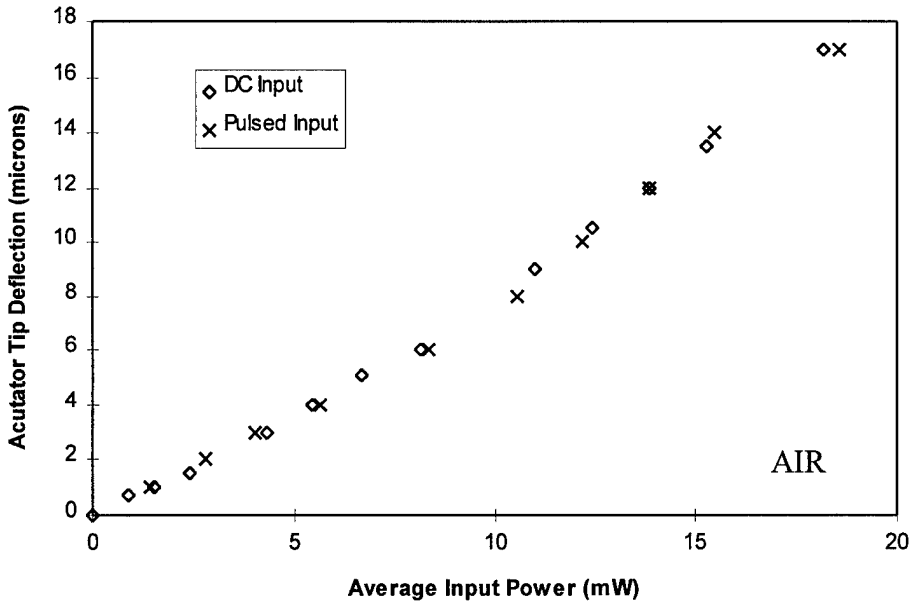


Figure 6-8. Deflection versus average power for a MUMPs 16 thermal actuator driven by DC and pulsed input. DC input amplitude varies from 0 to 4.2 volts. Pulsed input has a fixed pulse width of 5 μs, period of 10 μs, and a variable amplitude. The length/width of the actuator hot arm, cold arm, and flexure were 230/2.5 μm, 180/16 μm, and 50/2.5 μm. The thickness of the polysilicon was 2μm.

6.3.1.2 Thermal Piston Micromirror

The response of thermal micromirrors to pulsed inputs was also investigated in order to validate the use of pulse inputs on a different type of thermally actuated device. The deflection of the piston micromirror was measured using the laser interferometer system previously discussed in Chapter 4. Both pulse amplitude and pulse width modulation were used to position the mirror over a ~2 μm range. Pulse width modulated signals were generated by varying the duty cycle of a 100 KHz pulse train which was applied in a burst for the transient deflection measurement. Bursts of a 50% duty cycle, 100 KHz square wave were used to verify amplitude modulated pulse drive.

The average power of the pulse train was computed using the measured device resistance and Equation (6-1). Shown in Figure 6-9 are DC and pulse drive deflection measurements for a thermal piston micromirror device operating in vacuum.

6.3.2 Electrothermal SPICE Model and Pulse Modulation

One of the hurdles to efficiently employing pulse modulated drive signals for thermal actuators is understanding and modeling the complex electrothermal system inherent in these devices. The availability of the SPICE model developed in Chapter 4 proved to be invaluable in simulating the behavior of polysilicon thermal actuators when driven by a pulsed input. Pulsed inputs are easily simulated in SPICE, and the electrothermal model was designed to emulate the frequency behavior of the device.

The SPICE model provided insight into the operation of thermally actuated devices and allowed for predicting the performance of new designs before fabrication.

Table 6-1 shows the accuracy of the model in predicting the power dissipation of a lateral thermal actuator when driven by DC and pulsed drive signals. Figure 6-10 demonstrates the deflection prediction of the electrothermal SPICE model for the same actuator when driven by a pulse width modulated signal.

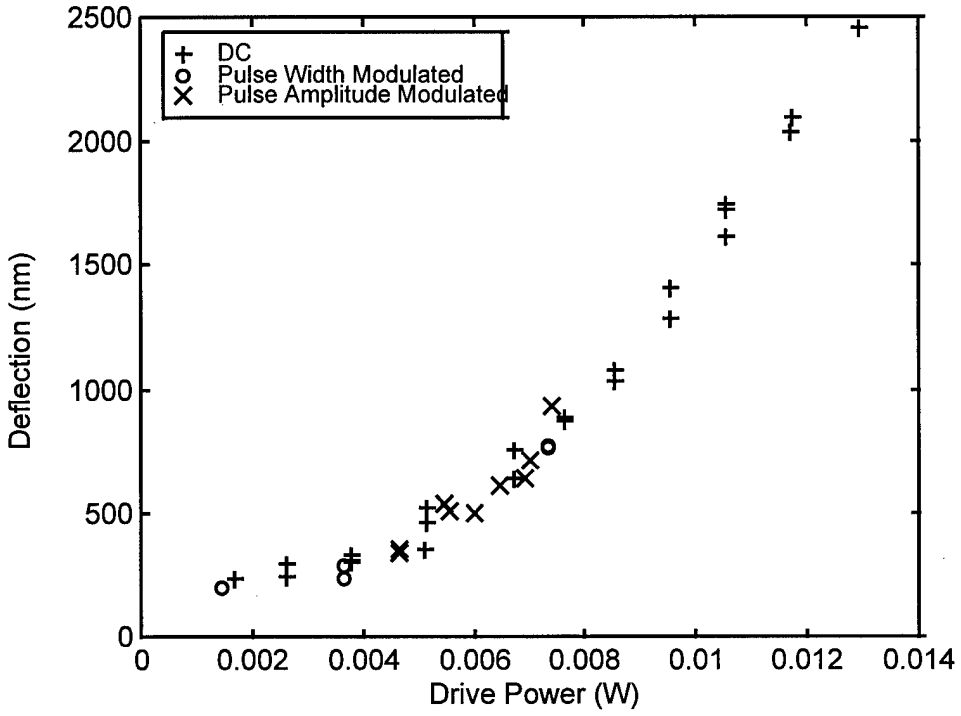


Figure 6-9. Deflection vs. power for a MUMPs 17 thermal piston micromirror operating in vacuum [29]. The length/width/thickness of the mirror flexures was 64/4/2 μm. The mirror plate had a diameter of 70 μm.

Table 6-1. Comparison of SPICE Model versus Measured Average Power Dissipation for Lateral Thermal Actuator.

Pulse Width (μs)	Amplitude (Volts)	Average Power (mW) Measured	Average Power (mW) SPICE
DC signal	1.47	2.25	2.22
5	2.10	2.29	2.24
2.5	2.90	2.19	2.17
1.25	4.10	2.19	2.17
0.625	5.90	2.26	2.25
0.3063	8.60	2.35	2.29

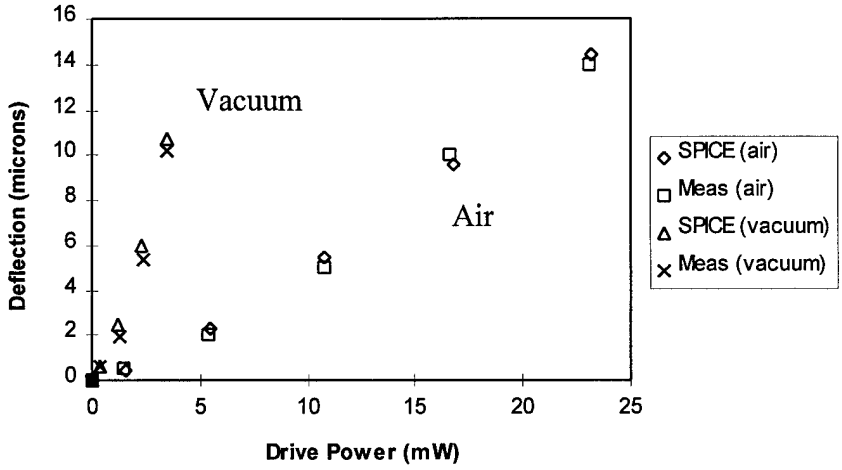


Figure 6-10. SPICE model and measured deflection versus average power for MUMPs 9 lateral thermal actuator. The drive signal had an amplitude of 5.5 volts and period of 10 μs with variable duty cycle. The length/width of the actuator hot arm, cold arm, and flexure were 200/2 μm, 170/14 μm, and 30/2 μm. The vacuum pressure was 20 mT. The thickness of the polysilicon was 2 μm.

6.4 Pulse Modulation Control Implementations

The use of pulsed inputs allows for flexible positioning and control of thermal actuator arrays. A CMOS application specific integrated circuit (ASIC) was designed which uses pulse width modulation to automate the positioning of thermally actuated devices. This system has been used to drive thermal micromirrors, stepper motors, and automated assembly systems. The SPICE model was useful in predicting the electrical load effects of the thermal actuators and allowed for proper sizing of the CMOS drivers prior to ASIC fabrication.

The control implementation using pulse modulation allows for analog positioning of the actuator deflection without the need for D/A converters or other analog circuits. This allows for a single voltage, all digital control system to be used for many thermal actuator applications.

6.4.1 Pulse Modulation Control of Scanning and Rotating Micromirrors

The invention of pulse modulation control for thermal actuators allowed for the development of a single control system which was able to drive both the scanning and rotating micromirrors. Pulse width modulation was chosen in order to produce a simple, single voltage control system. The heart of this pulse width modulation scheme is an ASIC chip with programmable pulse width modulation. Figure 6-11 shows a block diagram describing the functionality of the pulse width modulation ASIC. The ASIC has a digital interface and eight output drivers. Four of the outputs can be pulse width modulated.

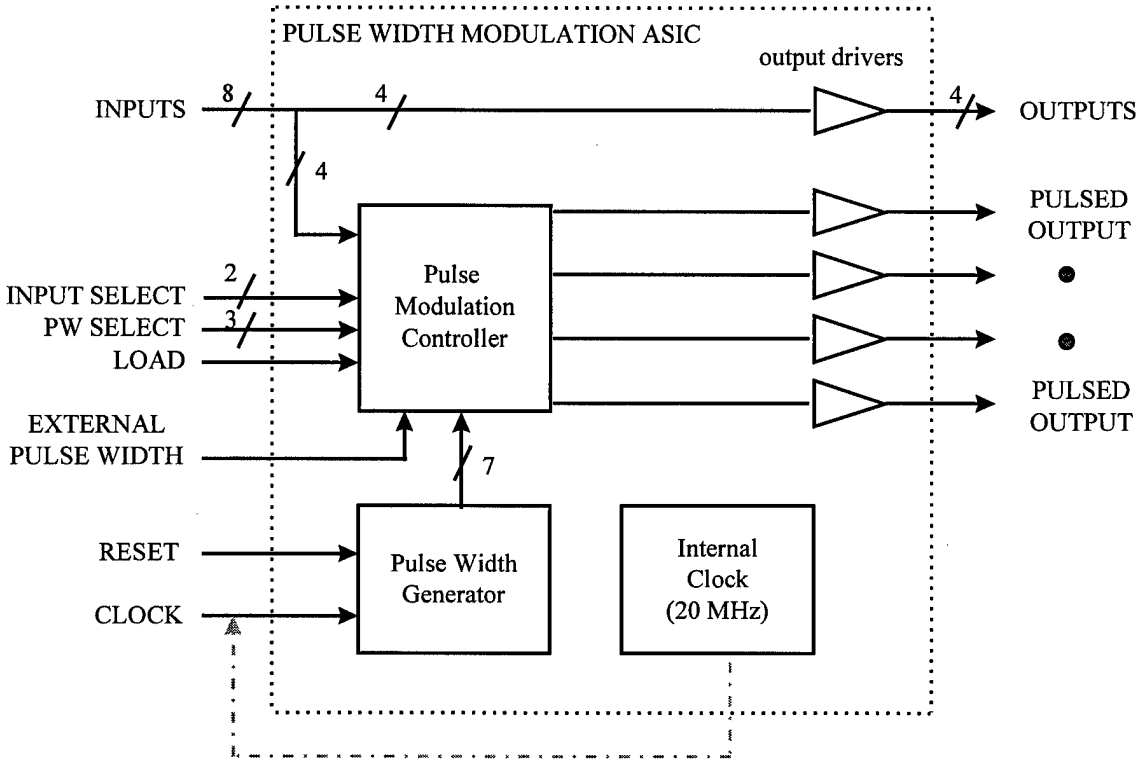


Figure 6-11. Block diagram of CMOS ASIC.

The ASIC has an internal pulse generator which produces seven pulse trains with different pulse widths. The pulse widths are based on the period of the clock signal. The shortest pulse width is equal to the period of the clock, and each of the subsequent pulse widths is a multiple of the clock period. For example, if the clock signal has a total period of 1 ms, then the pulse generator will produce eight pulse trains with pulse widths of 1-7 ms. The total period, P_{total}, for all of the generated pulse trains is:

$$P_{total} = 8 * P_{clk} \tag{6-2}$$

where P_{clk} is the clock period. An external pulse modulation signal can also be provided. This is allows the use of unique pulse modulation signals which can not be generated on-chip.

The internal pulse modulation controller uses the PW SELECT and INPUT SELECT signals to identify which one of the 8 pulse trains should be used for the specified output channel. The pulse trains from the pulse width generator and external source are buffered and can be used to modulate more than one channel at a time. In addition, after selection of the pulse train, the output channel continues to be modulated by the specified pulse train until that particular channel is selected and updated again. This allows for programming the pulse width on a single output without affecting the operation of the other channels.

An on-board clock was also implemented to provide a convenient way to run the pulse width generator. SPICE analysis demonstrated that the pulse width generator had a maximum operating frequency of 25 MHz. Consequently, a ring-oscillator was incorporated into the design to provide an on-chip 20 MHz clock. At 20 MHz, the period of the internal clock is 50 ns. Therefore, the period of the generated pulse trains can be estimated as 400 ns by using Equation (6-2) which corresponds to a frequency of 2.5 MHz. Subsequent testing of the fabricated chips demonstrated a measured period of 410 ns (2.4 MHz) for the pulse modulated outputs when using the internal clock.

After the pulse width modulation ASIC was fabricated and tested, a control system was developed as shown in Figure 6-12. For the scanning micromirror, a software subroutine determines the required pulse width and sends the drive signal and the modulation commands to the CMOS chip in order to drive the actuator array. This system worked as well as the first scanning micromirror control system of Figure 6-2 and was able to drive arrays with up to 10 elements. Similar to the previous control system,

this implementation was also unable to overcome the loose tolerances in the mechanical design and fabrication of the micromirror.

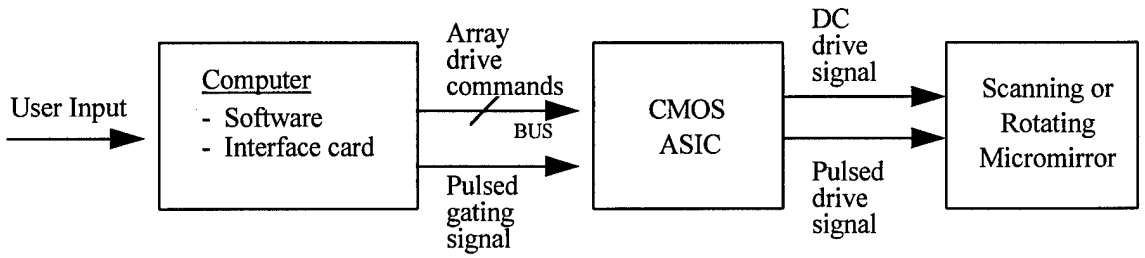


Figure 6-12. Micromirror position control system using pulse width modulation.

The pulse width modulation implementation was also used for the rotating mirror. The supply voltage was set at 6 volts to allow the drive array to operate using a DC value. The pulsed drive signal was used on the push array. Pulse widths of 7-9 μs with a period of 10 μs (70-90% duty cycle) were used. The pulse width modulation scheme was able to position the rotating micromirror as well as the previous design of Figure 6-6. Moreover, the pulse width modulation scheme only required a single supply voltage which was used to drive the CMOS microelectronics as well as both actuator arrays.

6.4.2 Pulse Modulation Control for Automated Assembly

Another application for the pulse width modulation control system is the supervision of automated assembly of MEMS devices. Figure 6-13 depicts the layout of an automated assembly system for a scanning micromirror as described in Chapter 3. This system consists of a vertical thermal actuator, an assembly motor, and a locking mechanism. The vertical actuator is used to give the mirror plate an initial lift off the

substrate. The assembly motor is then used to raise the mirror into an upright position where the locking mechanism from the scanning micromirror is engaged and secures the mirror plate [58].

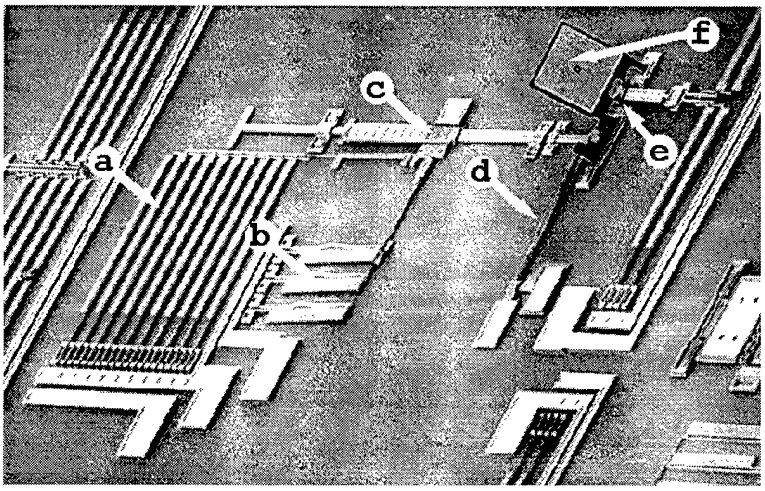


Figure 6-13. Automated assembly system for scanning micromirror [58]. The various components are: (a) assembly motor drive array, (b) assembly motor push array, (c) linear drive arm, (d) vertical thermal actuator, (e) self-engaging locking mechanism, and (f) scanning micromirror.

The pulse modulation control system was used to automate the assembly of the scanning micromirror. The backbending of the vertical thermal actuator was accomplished with the digital control system by programming a long pulse output. The voltage amplitude and duration of the pulse was determined empirically and then programmed into the computer. As discussed in Chapter 3, the single arm thermal actuators can be back bent by voltages around 7.5 volts.

After backbending the vertical thermal actuator, the digital control system was used to drive the linear motor. The linear motor used in the automated assembly system has similar voltage and current requirements as the micromotor used in the rotating mirror. Only the sequencing of the drive arrays needed to be changed in order to use the

digital control system. Once assembled, the position of the micromirror plate was controlled by pulse modulating the drive signal. The use of one automated control system for assembling and operating the scanning micromirrors (Figure 6-14) greatly simplifies the development and implementation of a practical microsystem.

The lack of a feedback mechanism in this design prevents the entire assembly process from proceeding without manual intervention. A status signal indicating the completion of raising the mirror plate is needed so that the control system will know when to stop driving the assembly motor. Several types of switches were investigated which could be incorporated into the automatic assembly system to provide a feedback signal. All of the switches are designed to engage after the assembly motor has lifted the mirror into the locked position.

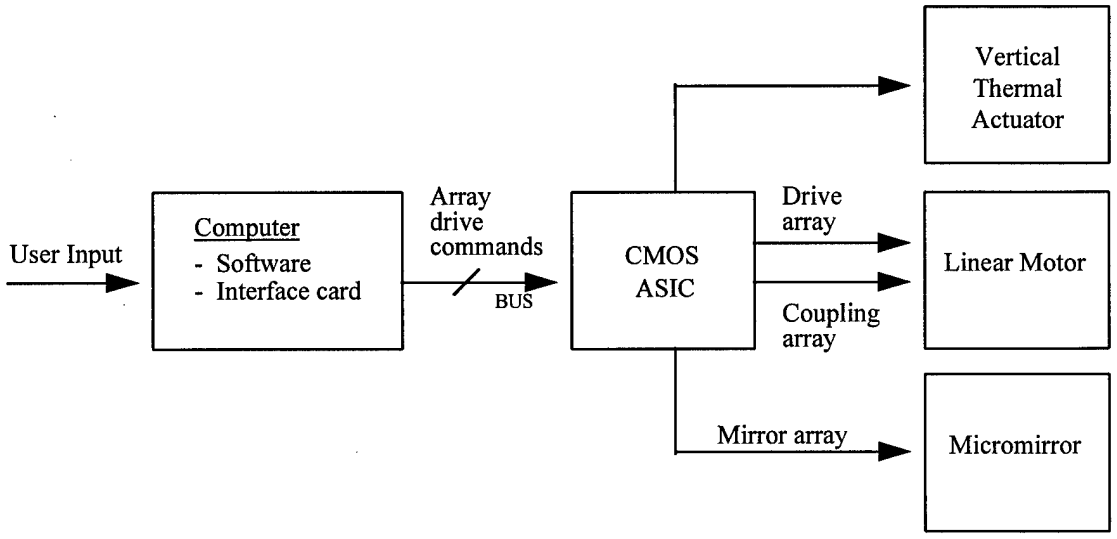


Figure 6-14. Computer based control system for automated assembly and operation of scanning micromirror.

The switches which used polysilicon-to-polysilicon contact such as the one shown in Figure 6-15 were able to be engaged during the assembly process, but were ineffective because of the high resistance. This switch operates by attaching a tab to the end of the linear drive arm used to raise the mirror plate. When the arm has moved far enough to ensure the plate is locked into position, the polysilicon switch is pushed into the latch which provides a complete circuit between the two contact pads. Unfortunately, the contact resistance of this switch is very high (> 10^6 ohms) due to the small surface area in the latch region and the polysilicon-to-polysilicon contact. Moreover, the contact resistance can not be detected after native oxide has formed on the polysilicon. Consequently, the switch is only operative for a short time after release of the die.

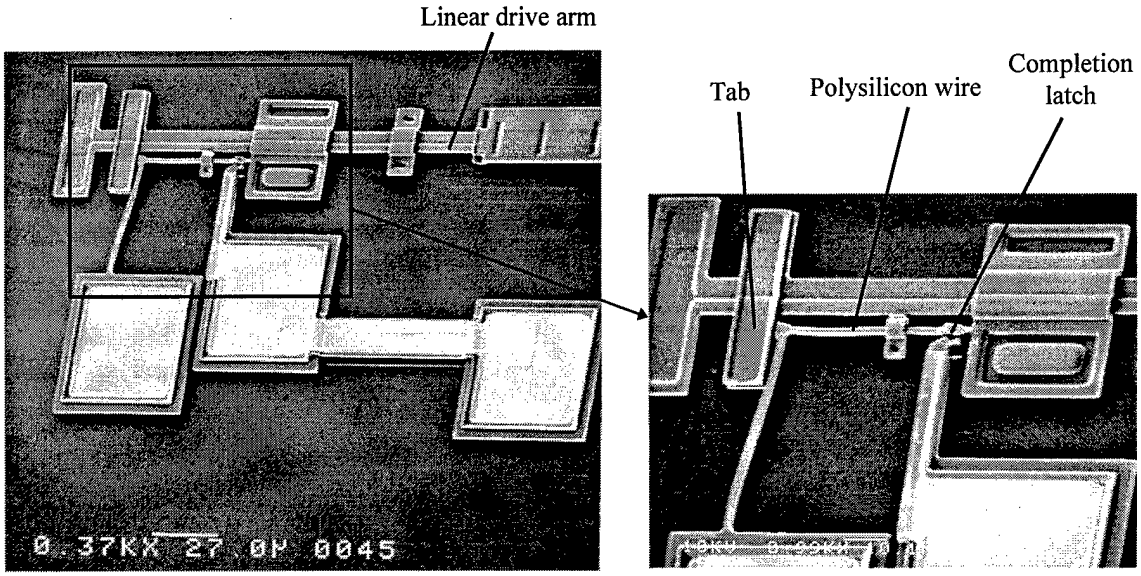


Figure 6-15. Polysilicon switch for detecting completion of automated assembly.

A gold-to-gold flip-over switch was able to be successfully employed as shown in Figure 6-16. This switch is similar to the one in Figure 6-15 except the linear drive arm

is used to flip-over a metallized contact bar. The use of a metallized contact bar allows metal-to-metal contact when the switch is closed [15]. This switch provided a low resistance contact which was easily detectable and useable as a completion signal. Furthermore, the gold surfaces do not oxidize and continue to provide good electrical contact long after the device has been released.

6.4.3 Other Applications of Pulse Modulation

The digital control system using pulse width modulation has also drawn interest for space-based MEMS applications because of its simple, single supply voltage implementation and ability to operate different types of MEMS devices while minimizing power requirements. Pulse modulation is particularly suited for MEMS applications because it leverages the physical characteristics of the device to increase the efficiency of the overall system.

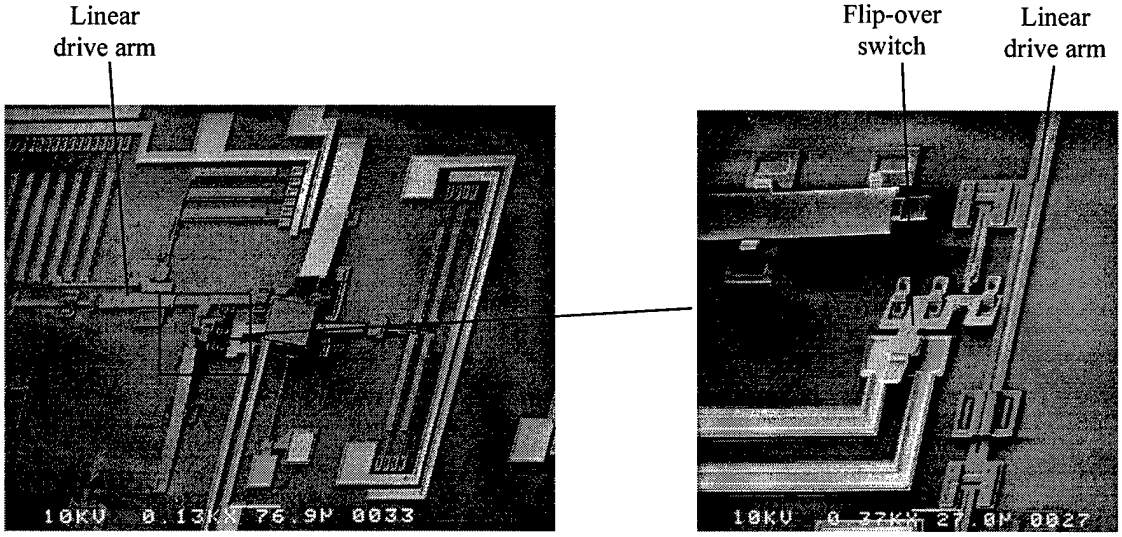


Figure 6-16. Gold flip-over switch incorporated into scanning micromirror automated assembly system.

Other applications for pulsed inputs include time-multiplex drive schemes which can be used to reduce the number of wires needed for driving large arrays of MEMS devices [29,44]. In this application, pulse amplitude modulation has great potential because a short, fixed pulse width can be used in conjunction with row, column addressing to control the average power delivered to an array of thermal devices analogous to the refresh cycle used for dynamic memory cells. Figure 6-17 shows a 3 x 3 array of elements using row, column addressing. Each element in the array is addressed by driving the appropriate row line and grounding the proper column line. For example, the center element can be accessed by driving ROW 2 and grounding COLUMN 2 while keeping the other rows and columns in a high impedance state.

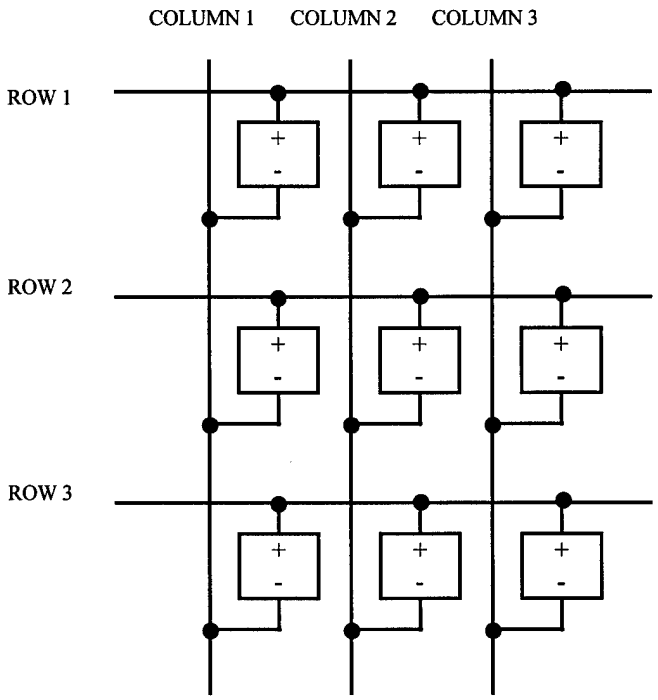


Figure 6-17. 3 x 3 array of devices using row, column addressing.

For an array of thermally actuated devices, the average power of each node defined by a row, column address can be controlled by using a pulse modulated signal. As long as the refresh rate is sufficiently faster than the thermal time constant, the deflection of each thermal actuator in the array can be controlled by adjusting the average power applied to the appropriate row, column node.

The primary advantage of row, column addressing is that the number of connections needed for wiring an n x n array of devices is only $2n$ as compared to n^2 for individually addressed arrays. For the 9 element array shown in Figure 6-17, only 6 wires are needed as opposed to 9 wires for individually addressing each device. The savings in the number of wires becomes much more dramatic for larger arrays. A 32 x 32 array of thermal micromirrors (1024 devices) using row, column addressing only requires 64 wires which is much more manageable than the 1024 wires needed for individually addressing each device.

Finally, pulse modulation control of electrostatic devices is also feasible. The success with pulse modulated drive of thermally actuated devices led to a preliminary investigation of pulsed signal drive for electrostatic devices. The key to pulse modulation control of electrostatic devices is to manage the electrical charge at the controlling node. The capacitance of an isolated, electrostatic MEMS device is typically very small which would suggest that its electrical response would be very fast. However, MEMS wiring tends to be very resistive and capacitive which slows the overall system response to the hundreds of kilohertz which makes the design of a CMOS pulse modulation control

system feasible. Figure 6-18 shows the resistance and capacitance impact of a long, thin polysilicon (*Poly 0*) wire fabricated in the MUMPs process. The 'Before' trace shows the pulse train just before connection to the polysilicon wire, and the 'After' trace shows the pulse train after passing through the MEMS wire. In this example, the maximum frequency of a system using this wire would most likely be limited by the wiring and not the device.

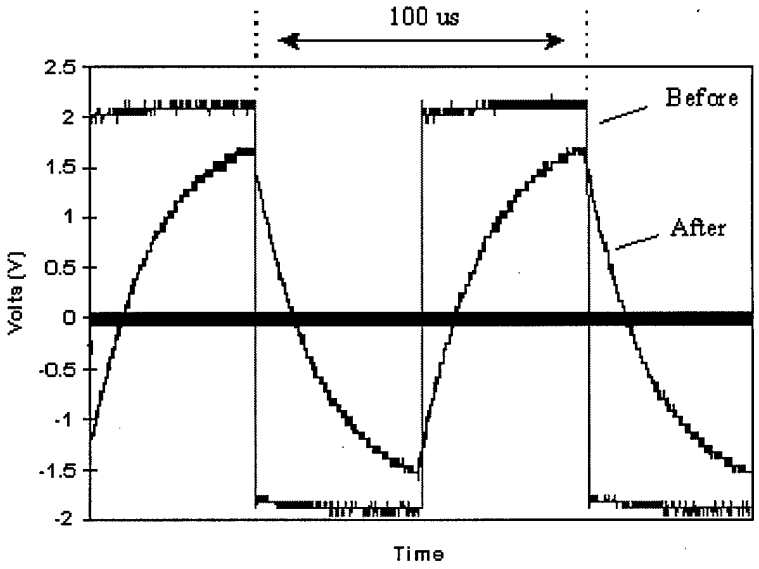


Figure 6-18. Resistive and capacitive impact of a long MUMPs 16 *Poly 0* wire. The wire was 2 μm wide and 8500 μm long.

As a proof of concept, electrostatic piston mirrors were successfully positioned in air using pulse modulated signals. However, significant work remains in characterizing the frequency behavior of the electrostatic mirrors and MEMS wiring under pulse modulation particularly in vacuum conditions where squeeze film damping is not present. Investigation of the impact of squeeze film damping also needs further investigation. In addition, it should be possible to add a large external capacitance at each device node

which would be much larger than the capacitance of the MEMS device or wiring. This external capacitance could then be used to facilitate pulse modulation control of any electrostatic MEMS device without having to work with its small capacitance. Work in this area will be continued by Captain Paul Rounsavall as part of his AFIT master's thesis.

6.5 Summary

Computer-based control systems using CMOS drivers and pulse width modulation were developed to control a variety of devices such as micromirrors and automated assembly systems. The digital control system automated the positioning of both the scanning and rotating micromirrors. CMOS technology is an attractive choice for integration with thermal actuators because of the wide availability of CMOS interface circuits and CAD design tools. Moreover, the thermal actuators used in the micromirror systems were designed to be compatible with CMOS voltage and current levels. Much of the logic for the control system was implemented in software running on a desktop computer in order to maintain prototyping flexibility. However, all of the logic functions can be implemented in ASICs or programmable gate arrays.

A key to the success of the digital control system was the use of pulsed control signals to drive the thermal actuators. Thermal actuators employ ohmic heating and thus function on the average applied power. Thermal actuators can be controlled and positioned using a pulsed input with a period much less than the actuator thermal time constant. The use of pulsed versus DC inputs allows for flexible positioning of the

actuator arrays and the ability to drive large arrays. In addition, the use of pulsed inputs allows for a single or reduced set of supply voltages to be used to drive the microelectronics as well as a variety of thermal actuator arrays.

Pulse width modulation was chosen for the implementations described in this dissertation; but pulse amplitude modulation schemes can also be used. Pulse width modulation was determined to be easier to implement in an all digital system with a single supply voltage; however, pulse amplitude schemes have more potential for high-speed, multiplexed operation since a short, fixed pulse width can be used.

The functional integration of MEMS and microelectronics is a significant step in the creation of a useful microsystem. Another requirement is the physical integration of MEMS with microelectronics. Many researchers are exploring monolithic fabrication of MEMS and control electronics to accomplish physical integration. An alternative approach to physical integration of MEMS and microelectronics is to use a multichip module which is the topic of the Chapters 7-9.

Chapter 7. Fundamentals of MEMS/MCM Packaging

The miniaturization advantages of micromachined components and systems are not realized if they cannot be efficiently integrated and packaged with microelectronics. Moreover, commercially viable MEMS devices are just now reaching the level of sophistication where volume production and reliability issues are being seriously considered and researched [1]. Consequently, MEMS packaging and hybrid integration research is emerging as a high-visibility area in the field of microsystems.

The most desirable approach to integration of MEMS and microelectronics is to create a single or monolithic fabrication process capable of supporting both microelectronics and MEMS. Research into monolithic fabrication of MEMS and microelectronics is progressing as demonstrated by the Sandia M^3EMS process described in Chapter 2. However, monolithic integration of MEMS and electronics is complicated by incompatibilities in the fabrication and processing of MEMS and integrated circuits.

An alternative to monolithic integration is to use multichip modules (MCMs). MCM technology has improved dramatically over the last decade in response to requirements for better packaging and performance in microelectronics [2]. MCMs offer an attractive approach to integrating and packaging MEMS with electronics because of the ability to support a variety of die types in a common substrate without requiring changes or compromises to either the MEMS or electronics fabrication processes. Furthermore, MCMs will offer design flexibility by providing packaging alternatives for applications for which it is cost or time prohibitive to develop a monolithic solution.

7.1 MEMS and CMOS/VLSI Integration

The integration of MEMS with CMOS/VLSI integrated circuits is of great interest because of the enhanced performance gained when micro sensors and actuators are placed in close proximity. This section reviews some of the basic integrated circuit fabrication technologies and highlights some of the obstacles that must be overcome when integrating MEMS and microelectronics either monolithically or in multichip modules.

7.1.1 Integrated Circuit Technologies

There are two dominant integrated circuit (IC) technologies: Bipolar Junction Transistor (BJT) and Metal-Oxide Semiconductor (MOS) which include Complementary MOS (CMOS). Both of these technologies have qualities which affect their application and desirability for use as an interface to MEMS devices.

Bipolar circuits are the oldest class of integrated circuit technology. Bipolar ICs have very high switching speeds and are able to drive large loads. They are often used in microwave and analog applications where gigahertz frequency operation is required or as line drivers because of their high current capability. Bipolar devices are also the best technology for producing general purpose utility devices such as voltage references, voltage regulators, and current sources [7].

Bipolar ICs are not usually the best choice of technology for MEMS integration. Bipolar ICs tend to require larger areas (low packing density) than MOS and CMOS devices and draw considerably more power. The fabrication process for bipolar devices is also more complicated than MOS or CMOS. Furthermore, most MEMS sensor

interfaces require high input impedance which is not as easy to achieve with bipolar circuits as with MOS circuits. Consequently, bipolar technology is traditionally only used in circumstances where its unique high speed and high drive capability is needed [7].

MOS and CMOS integrated circuits have simple, high yield fabrication process as well as high packing densities and low power dissipation. Most importantly for MEMS integration, MOS devices have inherently high input impedances and are easily configured to provide interface functions such as analog switches, multiplexers, and amplifiers.

Of the various MOS technologies, CMOS is generally accepted as the best circuit technology for integration with sensors even though the fabrication process for CMOS is more complicated than for NMOS or PMOS. As compared to NMOS, CMOS devices have higher gain per stage due to the presence of the p-channel transistors and lower power dissipation due to the minimal static power discharge. CMOS also is the preeminent technology for digital IC design, and therefore has the advantage of leveraging off the wealth of circuit design performed for the digital IC market [59].

Perhaps the best technology for MEMS and electronics integration is Bipolar-CMOS (BiCMOS). BiCMOS circuits combine the benefits of both bipolar and CMOS technologies. In digital IC design, CMOS circuits are used to perform logic operations and bipolar circuits are used as line drivers because of their ability to drive high current loads at high speed. The BiCMOS industry is not as well established as bipolar or

CMOS, but foundry services such as the Analog Devices *iMEMS* process which use BiCMOS exist and are now becoming important players in the industry.

7.1.2 MEMS and CMOS Integration Pitfalls

A great deal of work is currently underway to produce fabrication processes which will allow the development of MEMS and CMOS electronics on the same die. There has been some success such as the Sandia process mentioned earlier and the CMOS MEMS process. There are, however, several hurdles which must be overcome when integrating MEMS and CMOS. Even though many of the fabrication processes used in the development of MEMS are taken from the CMOS fabrication industry, the requirement to remove sacrificial layers in micromachining presents unique problems. First, the choice of sacrificial material for the MEMS device may be incompatible with the CMOS devices or microelectronic packaging. In CMOS, silicon dioxide is a critical material which is used as the gate insulator and for passivation; but many MEMS processes use silicon dioxide as the sacrificial layer. Consequently, the selection of structural and sacrificial materials in the MEMS devices impacts the integration of CMOS electronics.

In addition, several of the etchants for surface or bulk micromachining MEMS are not compatible with microelectronic materials or wiring. For example, KOH is often used in bulk micromachining, but it dissolves aluminum which is commonly used in IC metallizations. EDP, another of the often used etchants in bulk micromachining, is not as aggressive in attacking aluminum but still requires masking the aluminum in order to

have a reasonable chance of preserving the integrated circuits or the package. As a result, the integration of MEMS with electronics usually requires additional processing steps and materials to protect the CMOS circuits and the package during the final release.

Another problem with integrating of MEMS and CMOS devices is the high temperature anneal needed to remove residual stress in surface micromachined devices. As discussed previously, the high temperature anneal is needed to prevent curling and distortion of the MEMS devices. The temperature of the anneal is typically around 1000 °C which leads to undesirable diffusion of the dopants in the CMOS devices and can melt low temperature conductors such as aluminum which is often used in CMOS processing. Consequently, the fabrication process has to be changed to account for the high temperature anneal.

Electrical and environmental considerations also hamper monolithic integration of CMOS and MEMS. Many MEMS are designed to operate electrostatically and use high voltages (> 30 V) which are difficult to implement with submicron digital CMOS technologies. Other MEMS are designed to operate inside living organisms or are exposed to chemicals which would be destructive to the CMOS integrated circuits.

All of these factors combine to provide challenges for integration of MEMS and CMOS technology. For space applications in particular, monolithic integration may be even more difficult to achieve because of additional requirements such as radiation hardening which are needed for reliable spaceborne systems [60]. Building space qualified MEMS and integrated circuits in the same process may not always be cost effective or realizable. However, it may be possible to use Multichip Module (MCM)

technology to gain the benefits of MEMS and CMOS integration without the extra cost or additional technical challenges of monolithic integration.

7.2 MCM Technologies

The Multichip Module (MCM) is one of the key technologies for microelectronic packaging in the 1990's and for the foreseeable future. A formal definition for the MCM is [2]:

> "A MCM is a structure consisting of two or more integrated circuit chips electrically connected to a common circuit base and interconnected by conductors in that base."

In general, the term MCM is used to describe a variety of electronic packaging alternatives which seek to combine multiple die into a single package. The purpose of this section is to analyze the benefits of MCMs and review some of the more prevalent MCM technologies currently available and in development.

The term "Multichip Module" has been used for over 30 years, and the concept for repackaging integrated circuit (IC) and other components into a single package is not new [61]. However, the ability and need to commercially produce multichip modules did not gain momentum until the late 80's and early 90's [2]. Early MCMs were labor intensive and limited in interconnect ability since the initial concept was to attach various electronic die on a substrate and then use a single layer of metallization or wire bonding for the interconnects. Additionally, the early MCMs were difficult to repair and did not provide a significant improvement in performance [62]. Consequently, MCMs were not a major factor in the general electronic packaging industry until recently.

Within the last decade, there has been a resurgence in the interest and viability of MCM technology. One reason for the increased optimism for MCM technology is that long-standing research programs of several U. S. and foreign electronics companies have produced new packaging processes which have overcome many of the earlier limitations and made MCMs feasible and attractive alternatives for satisfying both general purpose electronic packaging requirements as well as unique requirements [61].

7.2.1 Benefits of MCMs

MCMs possess several characteristics which make them attractive for satisfying today's electronic packaging requirements. One of the prime benefits of MCM packaging for MEMS and IC integration is the ability to combine die from incompatible processes in a common substrate. Other benefits of MCM technology are the electrical, size, and weight performance improvement over conventional packaging techniques as shown in Table 7-1.

Table 7-1. Performance Benefits of MCM Packaging.

MCM Characteristic	Performance Benefit
Hybrid IC Integration	Increased Flexibility & Applications
Higher Packaging Efficiency	More I/O to 'outside world'
Reduction in Physical Size of System	Greater Range of Applications
Reduction in Total Interconnect Length	Higher Speed/Lower Power
Reduction in Interconnect Capacitance	Higher Speed/Lower Power
Reduction in Electrical Noise Generated	Higher Speed/Lower Power
Reduction in Connection Levels	Higher Reliability

MCM packaging is a key enabling technology for high performance, low voltage, and low power systems. MCMs indirectly allow the use of low supply voltages because

the environment inside a MCM can be designed to have low-capacitance interconnects, low-inductance leads, and very low loss power and ground planes when compared to traditional printed circuit boards [2]. The low noise MCM environment helps to maintain signal integrity because noise immunity is reduced when the supply voltage is reduced as is often the case in low power systems. Additionally, the elimination and reduction of parasitic capacitances and inductances result in a substantial reduction in propagation delay.

The U. S. Air Force Research Laboratory (AFRL) is sponsoring research on Ultra Low Power CMOS technology which is targeting high performance MCMs in order to be able to reduce the supply voltage and minimize propagation delay. The combination of the extremely low supply voltage (< 500 mV) in combination with MCM packaging is predicted to reduce power dissipation by two orders of magnitude with no loss in system throughput [63].

Equation (7-1) shows how reducing the capacitive load of the interconnects lowers power dissipation:

$$P_{dynamic} = C_L * V_{dd}^2 * frequency \qquad (7\text{-}1)$$

where C_L is the load capacitance and V_{dd} is the supply voltage. This is an attractive feature of MCMs because lowering the node capacitance does not negatively affect any other desirable circuit performance parameters [2]. Capacitive loading is reduced in MCM packaging as compared to printed circuit boards because intermediate layers of interconnects and packaging are eliminated or simplified. Since each die does not have

its own package, line lengths are reduced and fewer drive transistors are needed to propagate signals through highly capacitive and inductive packaging interconnects. Shorter interconnect length equates to less line capacitance. Consequently, less energy has to be expended to charge the smaller load capacitances characteristic of the MCM environment.

7.2.2 MCM Packaging Alternatives

Any decision to use MCM technology must include an analysis of the various MCM packaging alternatives as well as the performance benefits. There are several methods for categorizing the various types of MCM packages. The two most common characteristics used for classification include the type of substrate used and the means of interconnecting signals between the die [2]. The three dominant MCM substrate technologies available today are MCM-L (Laminate), MCM-C (Ceramic), and MCM-D (Deposited); but other substrate alternatives are beginning to emerge. The following sections describe the most prevalent technologies for substrate type and interconnect choice.

7.2.2.1 MCM-Laminate Technology

MCM-L technology is essentially a direct miniaturization of a printed circuit board and is often referred to as "chip on a board" technology. In MCM-L packaging, bare die are mounted on a 'PCB-like' laminated substrate, wire bonded, and then encapsulated with epoxy to protect the IC and wire bonds from the environment. MCM-L is used in digital watches, calculators, and many inexpensive consumer electronics.

The chief attribute of MCM-L technology is low cost. MCM-L technology is able to leverage off the existing infrastructure supporting the PCB industry which allows for low cost production. Furthermore, MCM-L is very effective when only a few chips need to be packaged together or the interconnections between the die are low. MCM-L technology is able to borrow many of the 'tricks' used in the PCB industry to make interconnects and keep costs low [2]. The disadvantages of MCM-L include limited wiring density, relatively thick line widths, and a high coefficient of thermal expansion as compared to silicon.

7.2.2.2 MCM-Ceramic Technology

MCM-C represents the class of packages using multilayer ceramic structures as a substrate. The two main types of MCM-C in use today are High Temperature Cofired Ceramic (HTCC) and Low Temperature Cofired Ceramic (LTCC). HTCC technology has been available since the 1970's and is presently the most commonly used [62]. HTCC uses metals such as tungsten (W), molybdenum (Mo), and manganese (Mn) with high temperature melting points for the interconnects. However, the need for more conductive interconnects has led to the development of LTCC technology so that gold, aluminum, and copper can be used [2].

For both LTCC and HTCC, a liquid slurry is made from ceramic particles and organic binders and formed into a solid sheet. This sheet is often referred to as "green tape" because of its appearance before firing. Next, holes are drilled in the sheet for vias, and then a conductive ink (metallization) is applied in a screen printing process. When

all of the sheets have been printed, they are stacked in the appropriate order and fed into a furnace for firing (1400 °C for HTCC, 800 °C for LTCC) [2].

MCM-C packaging provides the best cost/performance combination of the three predominant substrate choices -- it is more costly than MCM-L, but offers a significant increase in wiring density and electrical performance [64]. MCM-C has an established infrastructure, and ceramic materials are well understood which allow packaging engineers flexibility in adapting the ceramic materials to new or unusual requirements [2]. LTCC also has a limited 3-dimensional capability in that a range of passive components (e.g., inductors, resistors, and capacitors) can be embedded into the substrate [64].

The primary drawback of MCM-C packaging is the relatively high dielectric constant of the currently used ceramic insulators. Most of the dielectric materials used in MCM-C processing have dielectric constants which are two to three times higher than the materials used in other MCM technologies [2]. The dielectric constant of the insulator impacts the signal speed, power consumption, and wiring density of the packaged system. On-going research is producing new ceramic materials suitable for MCMs which have dielectric constants on par with the other MCM technologies [65].

7.2.2.3 MCM-Deposited Technology

The third common MCM substrate choice is MCM-D or thin film multilayer packaging. Just as MCM-L is strongly related to the PCB industry, MCM-D technology shares many of the same characteristics of the semiconductor fabrication industry. In

fact, the 'D' suffix and thin film moniker are associated with the use of IC thin film deposition processes to achieve high density patterns for interconnects. The use of IC processes enables MCM-D systems to achieve the highest performance of any MCM process in general.

MCM-D systems typically use high conductivity interconnect metals such as Cu, Al, or Au. The conductor layers are separated by deposited dielectric layers with low dielectric constants. The metal interconnects can be patterned using the same lithography techniques available to the semiconductor industry; therefore, MCM-D systems are able to achieve very high wiring density and high frequency performance. Special purpose MCM-D prototypes have been designed for clock speeds in excess of 3 GHz [2].

While MCM-D represents the high end of the MCM performance spectrum, it also represents the high end of the cost spectrum. The high cost and limited availability of MCM-D systems has slowed the widespread use of MCM-D technology below projections made 5-10 years ago [2]. The imposing cost of the infrastructure to support MCM-D technology parallels the semiconductor industry where only the largest companies can afford to support the equipment costs. Recent advances in MCM-C technology such as LTCC provide alternatives to MCM-D at much less cost. Despite these drawbacks, MCM-D is considered the core technology for future research in MCMs, and many pundits believe that as performance requirements continue to rise, more applications will utilize derivatives of MCM-D technology [2].

7.2.2.4 MCM-D/C Technology

A hybrid of deposited and cofired ceramic substrate technology designated MCM-D/C has garnered a great deal of attention. By using the MCM-D dielectric deposition process on a ceramic base, many of the advantages of MCM-C and MCM-D can be cost effectively combined. The use of an MCM-C base provides lower cost and a greater degree of engineering flexibility due to the use of ceramics. Furthermore, the deposited interconnect layers provide the high frequency and interconnect density associated with MCM-D technology.

Another benefit of the MCM-D/C combination is the ability to make use of the different dielectric constants of the insulating layers. In MCM-C, the high dielectric constant is considered a disadvantage because of the negative impact on signal lines; however, in MCM-D/C, signal lines are embedded in the low loss deposited layer. Consequently, some designers are *increasing* the dielectric constant of the ceramic base and embedding the power and ground planes in the ceramic to create a large decoupling capacitance between power and ground [63]. This technique allows much if not all of the external bypass capacitors to be eliminated from the design and avoids a secondary assembly step [2].

7.2.2.5 MCM-Silicon Technology

Another derivative of MCM-D is MCM-Silicon (MCM-Si) or "silicon on silicon" technology. MCM-Si is similar to MCM-D in that IC fabrication processes are used to deposit the interconnect layer; however MCM-Si differs in that a silicon wafer is used as

the substrate base. Aluminum and copper are used as the conductors and silicon dioxide is used as the dielectric. MCM-Si has the highest signal interconnect density of any substrate choice and its coefficient of thermal expansion is typically an excellent match for any silicon die [2]. The primary disadvantage of MCM-Si is that silicon is not a good base for the MCM package assembly because it is relatively fragile, and consequently the MCM-Si substrate must be repackaged causing additional cost [2]. Also, MCM-Si utilizes the same high cost infrastructure as MCM-D; and consequently, MCM-Si systems can be relatively expensive.

Another advantage of MCM-Si technology is that bulk micromachining techniques can be used to pattern the silicon substrate. The substrate can be patterned using silicon bulk etchants and wafer bonding to form useful features such as embedded passive components and microchannels [66,67]. Microchannels may be used to carry fluids to and from pressure or chemical sensors and to micropump actuators mounted in the module. In addition these microchannels can provide an efficient way to cool the MCM [67].

7.2.2.6 MCM-Optical Technology

MCM-Optical (MCM-O) may represent the next generation in high performance MCM technology. The use of optical interconnections between ICs could eliminate many of the limiting factors affecting electrical interconnects such as electromagnetic interference and limited bandwidth. Optical systems have a terahertz bandwidth which is at least an order of magnitude greater than the bandwidth of electronic systems [2]. Also,

thin film optical waveguides have been shown to exhibit negligible crosstalk even when physically connected and simultaneously transmitting optical signals [68]. This may allow a reduction in the number of interconnect levels since the need for cross-overs and vias will be eliminated for the optical interconnects.

7.2.2.7 Wirebond Interconnects

Wire bonding is the oldest and most widely used MCM interconnect methodology, and thermosonic wire-bonding is the most prevalent technique in use today [57]. Figure 7-1 demonstrates the process.

The primary advantages of wire bonding are low cost and wide accessibility. The disadvantages include high inductance which increases propagation delay and power dissipation. Also, the wires tend to be longer than other interconnect options which contributes to low performance. Testability is a concern when using wire bonding because 'at speed' testing of the die before packaging is not feasible for high performance circuits due to the inductance in the probe wires used to make connections on the die [2]. Consequently, a full speed test of a wire-bonded MCM is not usually performed until the entire unit is assembled which may be undesirable if there is a high failure rate for any of the individual die.

7.2.2.8 Tape Automated Bonding (TAB)

Tape Automated Bonding (TAB) consists of bonding a lead-wire framework to the die and then attaching the die and frame assembly to the substrate as shown in Figure 7-2. The chief advantage of TAB is ease of testability which allows die to be tested and

burned-in prior to installation into an MCM. Disadvantages include inductance in long lead traces and significant cost increase as compared to wire bonding. TAB connections are typically used in applications were the need for testability and reparability justify the additional cost.

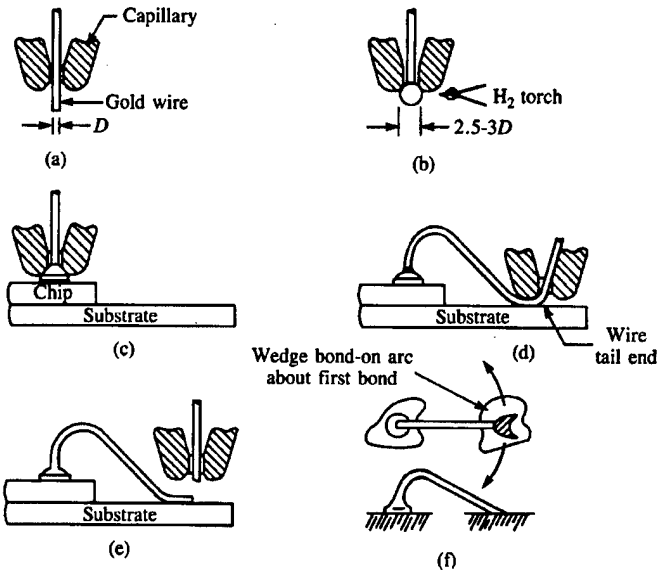


Figure 7-1. Processing steps for thermosonic bonding of a gold wire [57].

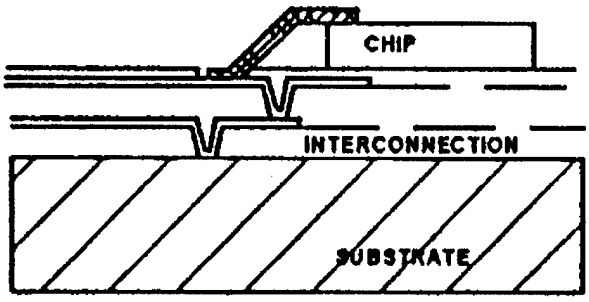


Figure 7-2. An example of TAB interconnect on an MCM-D substrate [69].

7.2.2.9 Flip Chip Interconnects

Flip chip, which was originally known as Controlled Collapse Chip Connection (C^4), offers outstanding electrical and density performance because it eliminates leads altogether. As the name implies, the die or chip is 'flipped' over and connected to the substrate via solder bumps as shown in Figure 7-3. The ability to attach and remove the die is simply a matter of locally heating the substrate to reflow the solder. Reliability concerns with flip chip technology have been largely eliminated through manufacturing improvements [64]. Other than direct metallization, flip chip and other forms of leadless interconnects provide the best technical solution for MCM packaging.

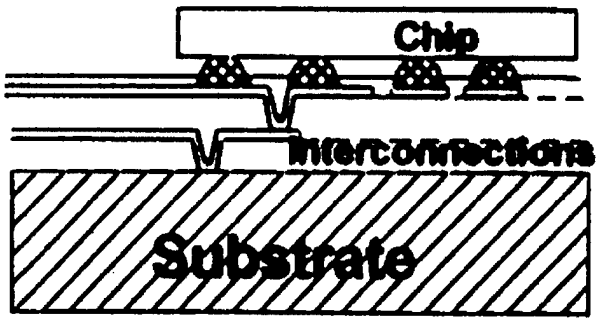


Figure 7-3. An example of flip chip interconnect on an MCM-D substrate [69].

One of the first foundry attempts at multichip packaging of MEMS and electronics using flip chip technology is the SMARTMUMPs process available from MCNC. The SMARTMUMPs process consists of flip chip attaching a standardized electronics die onto a MUMPs die as shown in Figure 7-4 [17]. The MUMPs die is released prior to attachment of the electronics die.

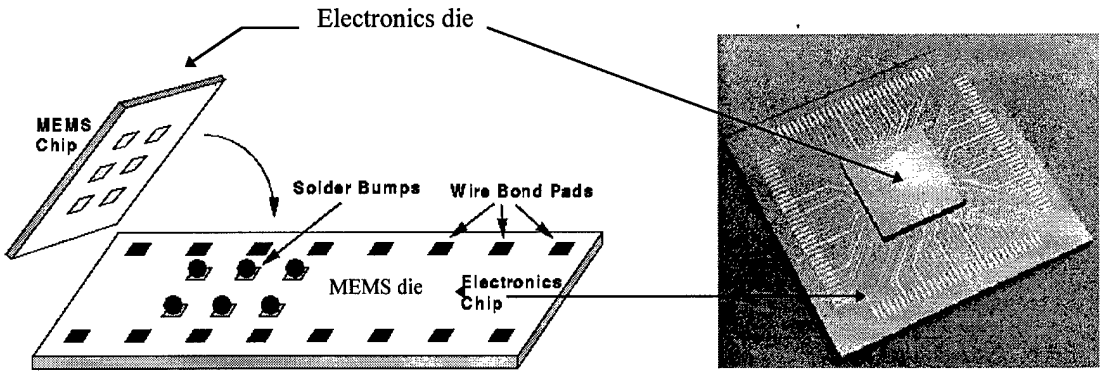


Figure 7-4. SMARTMUMPs flip chip attachment from MCNC [17].

The electronics die contains a representative set of devices useful for interfacing with and testing MEMS devices. Among the circuits contained on the electronics die are signal amplifiers and integrators, current repeaters, a clock generator, and a pulse generator. The mix of circuits was based on survey information from MUMPs users [17].

Some of the drawbacks to this integration technique for general purpose use is that the electronics die will block physical and optical access to any MEMS devices located underneath it, and there is no access to the electronics die except through wiring or test points located on the MEMS die [17]. In addition, the current electronics die is limited in area and capability and is not optimized for any particular application. Moreover, MCNC has experienced significant difficulty in developing a pad frame in the MUMPs process which is compatible with the flip-chip bonding procedure and the analog CMOS circuits [39]. These difficulties highlight the obstacles to integrating MEMS and CMOS.

7.2.2.10 Direct Metal Deposition Interconnects

One of the newest methods for making interconnects between die on an MCM is known as direct metal deposition. Direct metal deposition uses the same types of VLSI fabrication processes as in fabricating the die themselves to pattern a layer of metal directly onto the bond pads. Two broad categories of direct metal deposition techniques are patterned overlay and patterned substrate as shown in Figure 7-5. Patterned overlay occurs when the die are embedded in the substrate and the metal is deposited above the die. Patterned substrate describes the scenario when the metal is deposited first then the die are attached on the surface.

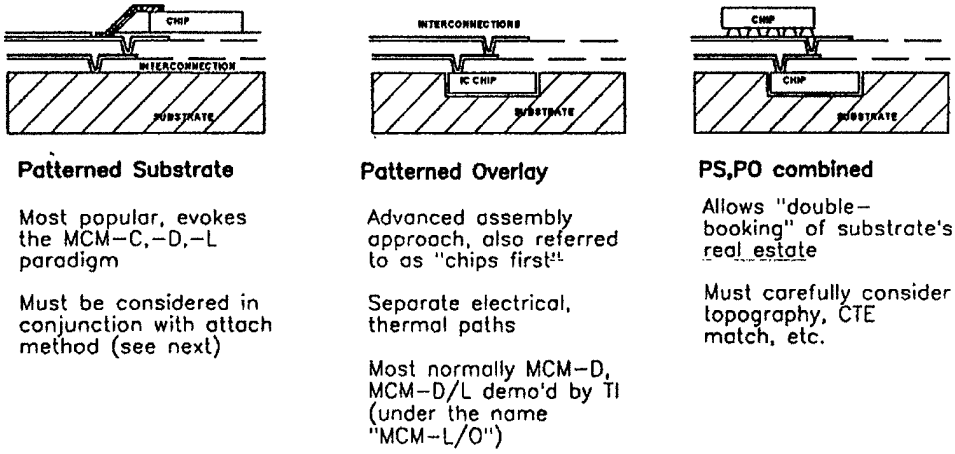


Figure 7-5. Examples of direct metal deposition interconnects [69].

7.2.3 High Density Interconnect MCM Technology

The General Electric High Density Interconnect (HDI) is a novel process which uses the 'die first' or patterned overlay concept. In the HDI process, holes are milled in the substrate to house the various die. After the die are placed and bonded in the substrate, Kapton sheets are glued over the top and via holes are created through a laser

drilling process. Metal is then deposited and patterned to form interconnects. The Kapton lamination and metallization process is repeated until all of the interconnect layers are created [70]. Figure 7-6 demonstrates the HDI fabrication flow.

The HDI process has several attractive features for MEMS and electronics packaging. First, the use of direct metallization interconnects allows for high speed and low power performance. The HDI process can produce systems capable of operating at over 1 GHz which is a significant improvement over existing available MCM-D technologies. For example, HDI packaging is being used in the Ultra Low Power CMOS project because of its ability to provide the low noise and low parasitic environment needed for such systems [63]. HDI packages can also be designed for repair. The Kapton overlay can be removed without destroying the embedded die. The faulty die can be replaced and a new Kapton overlay deposited over top. This repair procedure has been successfully conducted over ten times on an HDI package [70].

HDI technology can easily be extended to form a three dimensional package by flip chip attaching die on top of the Kapton overlay as shown in Figure 7-7 or by stacking entire HDI packages. 3-D stacking has the potential to further increase the size, weight, and electrical benefits associated with 2-D MCMs. Considerable progress has been made in extending the HDI process to three dimensions with actual prototype MCMs fabricated and tested [62].

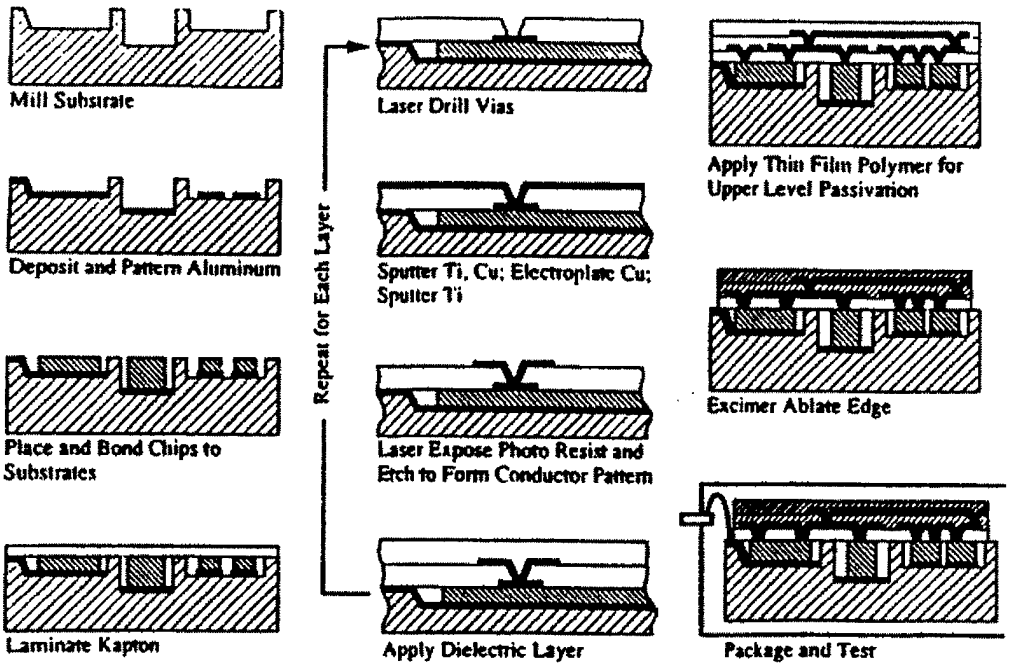


Figure 7-6. HDI MCM fabrication flow [70].

HDI is also an attractive option for integrating MEMS and electronics in the same package. First, the HDI process can accommodate die from a variety of processes because the die wells can be milled and configured to accommodate each individual die. In addition, the HDI process allows for bond pads to be located virtually anywhere on the chip. This is particularly advantageous for MEMS packaging because many MEMS processes have very limited wiring capability. In essence, the Kapton overlay can be used to create multilevel wiring on the MEMS die without the need to modify or compromise the MEMS fabrication process. Another desirable feature of HDI packaging is that the use of direct metallization for the die interconnects can result in electrical performance equivalent to monolithic integration [62,70]. Finally, the HDI overlay can also be used wholly or in part as a mask to protect other die in the package from the

release procedures of the MEMS die or the environment to which the MEMS die must be exposed.

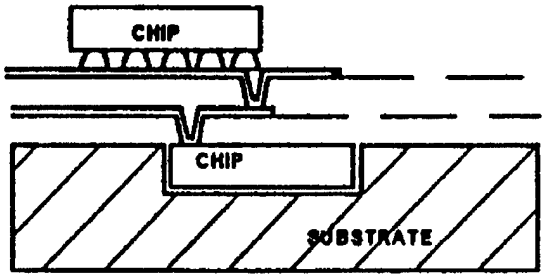


Figure 7-7. 3-D HDI packaging by flip-chip attaching components [69].

7.3. MCM Future Outlook

The growing need to match different types of technologies and processes into a single package will continue to make MCMs an attractive alternative. DARPA is investing $50 million for development of next generation packaging with the emphasis on combining wireless technology with digital systems in MCMs [71]. MCMs hold the promise of allowing MEMS and ICs to be combined together in a single substrate to provide the similar benefits as monolithic integration.

The optimism over MCMs is tempered somewhat by the realization that MCMs are often used to fill a void until monolithic fabrication or integration capability is available or affordable. MCMs are rarely viewed as the optimum integration solution when compared to a monolithic solution with similar costs and availability. For example, MCMs have been frequently used in desktop computers in order to improve the performance of the CPU chipset by bringing the main controller in closer proximity to the

cache memory, I/O controller, etc. However, as microelectronic fabrication capabilities have increased, the cache memory and other peripherals are routinely monolithically integrated into the main CPU chip which obviates the need for an MCM.

One area where MCMs have made a potentially long term impact is in chip scale packaging. A chip scale package (CSP) is generally defined as a packaged part that is approximately the same size or slightly larger than the bare chip alone [72]. MCM interconnect technology has been infused into CSPs which allow them to provide superior interconnect performance with low cost [73]. Unlike the MCM market, CSP demand is growing faster than industry projections. Hence, while MCMs in general may be an alternative packaging choice, MCM technology will continue to have a fundamental impact on CSPs and other parts of the mainstream packaging landscape.

7.4 MCM Testing

Testing is a key aspect of validating the success of MEMS/CMOS integration and packaging. One of the major interests in MEMS packaging is defining a set of failure modes which can be used as a basis for qualification testing. MEMS technology and advanced packaging technology such as the HDI process are so new that a database of knowledge is not available for building this data [74]. This lack of test data may slow the commercial use of MEMS especially for high reliability applications such as satellites. In an effort to start acquiring this type of knowledge, the U. S. Air Force Research Laboratory and the National Aeronautics and Space Administration Jet Propulsion Laboratory (NASA/JPL) are sponsoring the first space launch of MEMS accelerometers

with the express purpose of trying to ascertain the performance of MEMS components in the space environment [60].

7.4.1 Parametric MCM Testing

One approach to testing MEMS packaging is to extrapolate from testing standards based on microelectronic systems since MEMS devices have much in common with microelectronics in terms of materials and processing. MIL-STD-833C, Test Methods and Procedures for Microelectronics Users, is a military standard which provides guidance on environmental and mechanical testing of packaged electronics. Table 7-2 lists a subset of tests from MIL-STD-833C which were used for HDI testing and may be applicable to MEMS and MEMS/CMOS packaging.

Table 7-2. MIL-STD-833C Tests [75].

Test	Conditions
Stabilization bake	205 °C for 2000 hr.
Temperature cycling	-55 °C to 150 °C
Thermal shock	Liquid Nitrogen to 150 °C
Self heating (Power)	150 °C
Die shear strength	12 lb.
Mechanical shock	drop 5 times to 1,500 G
Vibration	20 G @ 20 - 2000 Hz

Some of the key electrical performance parameters that are often cited in specifying multichip modules are listed in Table 7-3. Many of these tests are applicable to MEMS packaging. Moreover, the mechanical nature of many MEMS devices will require additional packaging tests if a purely parametric approach to testing is used. Quantitative measurements of characteristics such as fluid flow, mechanical spring

constants, and range of motion may be needed which will require different types of testing equipment and expertise. Unfortunately, the equipment and procedures for measuring these types of mechanical quantities on the micro or nano scale are not well developed [1].

Table 7-3. Commonly Used Parameters for Evaluating Electronic Packaging.

Parameters for Evaluating Electronic Packaging
Dielectric Constant of Insulator
Sheet Resistivity of Metallization
Power Plane Capacitance
Operating Frequency
Signal Line Characteristics Impedance Resistance Capacitance Inductance Propagation Delay

7.4.2 Process Compliance

Another approach to validating the quality of MEMS and advanced packaging technology is to focus not on parametric testing standards for the end product but on maximizing the quality of the processes involved in producing the product [60]. This quality based approach to testing electronics has been successfully used on major defense programs such as the F-22 Advanced Tactical Fighter (ATF) [76]. For the ATF, many of the MCM packaging technologies are so new or revolutionary that no one is sure what the measurable standards should be. Consequently, engineers and managers focus on ensuring that the procedures and equipment used to package the electronic and avionic

systems are as good as possible. This requires more of a subjective, process-based assessment of the capability of the packaged electronic systems. The interim results have been very positive. The ATF electronics passed their Critical Design Review using this approach to electronic packaging [76], and the results are being validated in flight test.

Likewise, assessing the performance and reliability of MEMS and advanced packaging concepts may require a more flexible, process-based approach than simply applying existing microelectronic standards [60]. While MEMS devices borrow heavily from microelectronic fabrication, MEMS is not a subset of microelectronics. MEMS devices have failure modes and characteristics which do not have microelectronic analogs. For example, the optical reflectivity of a deposited metal layer is rarely a concern for a microelectronics designer, but the same quantity could be the overriding measure of quality for a MEMS designer using the same fabrication process.

One way to generate a process based assessment for MEMS/MCM packaging is through the development of assembly test chips (ATC). ATC's are special test die which contain sensors and test devices which monitor the health of the die through the packaging process [77,78]. Sandia National Laboratory has pioneered this concept for microelectronics. The same concept can be extended for MEMS packaging by developing MEMS test chips designed to identify and monitor the electrical, thermal, and mechanical properties of critical importance to the MEMS designer [1,15]. Thus, the use of MEMS packaging test chips was adopted for use in the MEMS/MCM packaging assessments described in the following chapters.

7.5 Summary

Integrating MEMS with microelectronics allows for the development of microsystems which make maximum advantage of the miniaturization and performance benefits expected from micromachines. CMOS and BiCMOS are prime candidates for integration with MEMS; however, differences in the fabrication and processing of MEMS and microelectronics creates obstacles to the physical integration of the two technologies. A solution to this physical integration problem is to use multichip modules (MCMs).

Multichip technology has matured over the past decade and provides an effective method of integrating die fabricated in different technologies. Furthermore, advanced MCM foundries are now available which provide affordable and high-performance packaging solutions for a wide range of applications. Two of the most advanced MCM alternatives available through foundries are MCM-D and patterned overlay modules. These foundry MCMs can be cost-effectively adapted for MEMS packaging as demonstrated in Chapters 8 and 9.

Chapter 8. MCM-D/MEMS Packaging

8.1 Introduction

The primary goal of the MCM-D/MEMS packaging research was to explore methods of leveraging the advances in microelectronic foundry MCM technology for the packaging of MEMS. Custom MCM technologies designed for MEMS applications have been proposed [66,79] but have not yet become available as foundry services. Successfully adapting existing MCM foundry technologies will provide a means for near term and low-cost development of microsystems as these products make the transition from research to commercial manufacturing.

The MCM-D process was selected for investigation because it is state of the art and is available through MCM foundries. The first foundry MCM process used for MEMS packaging was the Micro Module Systems (MMS) MCM-D. The MMS MCM-D represents a traditional packaging approach where the interconnect layers are deposited on the substrate and the die are mounted above the interconnect layers. The interconnect between the die and the substrate is made through wirebonding as shown in Figure 8-1.

The MMS process was chosen because its substrate and wiring materials are most compatible with the release procedure for the surface micromachined test die as explained later. Table 8-1 lists the characteristics of the MMS MCM-D package.

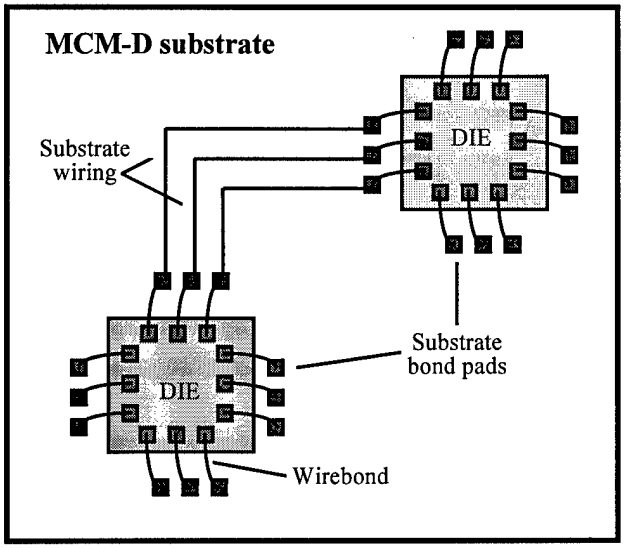


Figure 8-1. Notional view of MMS/MCM-D substrate.

Table 8-1. Characteristics of MCM-D Package [80].

Property	MMS MCM-D
Substrate material	Aluminum
Signal/power wiring layers	3/2
Dielectric material	Polyimide
Conductor metallization	Copper
Die attach adhesive	Ablebond 789-3
Die interconnect method	Wirebond
Die edge-to-edge spacing	> 500 μm
Max operating frequency	100 - 400 MHz

Key considerations for MCM-D packaging of MEMS include whether to release the micromachined devices before or after packaging and the compatibility of the package materials with the MEMS release procedures. Most MEMS devices require a 'release' etch prior to operational use. The release process involves removing selected materials to create three dimensional structures and, in some cases, to allow physical movement. Released MEMS devices are typically very fragile and require special

handling. Consequently, it would be desirable to release the devices after packaging especially when using foundries. However, many of the release etchants commonly used for MEMS are harmful to microelectronics and microelectronic packaging. The results of this research demonstrate methodologies for protecting released MEMS devices during the packaging process and for releasing MEMS devices after foundry MCM packaging.

8.2 MEMS Packaging Test Die

As discussed in the previous chapter, MEMS devices and technology are relatively new and parametric standards for ensuring the quality of packaging and assembly have not been developed. An assessment of the performance and reliability of MEMS and advanced packaging concepts can still be accomplished by using a process-based approach. Moreover, MEMS devices have failure modes and characteristics which do not have microelectronic counterparts. Hence, MEMS-specific packaging test die were designed to provide a disciplined method of evaluating the compatibility of MEMS with MCMs.

Sandia National Laboratory developed the concept of using specially designed chips for evaluating the impact of assembly and packaging on microelectronics [77]. Their Assembly Test Chip (ATC) series of test die are designed to monitor the health and performance of integrated circuits during manufacturing, packaging, and operation. The MEMS packaging test die used in this research incorporated a variety of devices and test structures designed to assess the impact of foundry MCM packaging on MEMS. The initial test die used in this research were a legacy from previous research conducted at

AFIT by Comtois [15]. Additional surface and bulk micromachining test die have been developed and employed during the course of this research.

Most of the surface micromachined MEMS packaging test die were fabricated using the Multi-User MEMS Processes (MUMPs) [17]. Silicon dioxide is the sacrificial material in this MEMS process and is removed with a wet etch in hydrofluoric acid. This test die contains a variety of devices and test structures designed to monitor the ability of surface micromachined MEMS to survive a foundry packaging process. Among the test structures are breakage detectors to monitor excess force and polysilicon resistors to monitor excess heating. Other devices on the die are representative of MEMS structures which might be used in an actual application. Table 8-2 lists general categories of devices on the surface micromachined test die.

The bulk micromachining test die was fabricated through the Metal Oxide Semiconductor Implementation Service (MOSIS) using the Orbit CMOS MEMS process. The CMOS MEMS process is based on a standard 2 μm CMOS technology and has two metal and two polysilicon layers. Provisions are made to specify cuts in the overglass to expose the silicon substrate for bulk micromachining. In addition, regions of boron doping can be specified to form etch stops for anisotropic silicon etchants such as ethylene diamine pyrocatechol (EDP) and potassium hydroxide (KOH). These tools allow for bulk micromachining to be accomplished in the standard CMOS process [14]. Table 8-2 lists some of the device categories represented on the bulk micromachining test die. A sampling of integrated circuits such as ring oscillators for testing package interconnects are also included on the test die.

Table 8-2. MEMS Device Categories on Test Die.

Device Category	Surface Micromachining Test Die	Bulk Micromachining Test Die
Electrostatic Piston Mirrors	√	
Electrostatic Comb Drives	√	
Flip-up/Rotating Devices	√	
Thermal Actuators	√	
Variable Capacitors	√	
Breakage Detectors	√	√
Cantilevers	√	√
Polysilicon Resistors	√	√
Suspended Structures		√
Thermal Bimorphs		√

8.3 MCM-D/MEMS Packaging Experiments

MEMS packaging test chips were sent to the DARPA-sponsored MCM Designers' Access Service (MIDAS) for MCM-D packaging. MIDAS provides access to low cost, prototype quantities of MCMs by acting as a brokerage for MCM foundries [80]. The MMS MCM-D is one of three foundry processes supported by MIDAS. The MCM-D/MEMS packaging experiment was a pure foundry transaction in that the fabrication was treated as a routine work order with no special handling requirements. MIDAS handled the entire transaction, and there was no interface between AFIT and Micro Module Systems. Figure 8-2 shows a photograph of one of the MCM-D/MEMS modules.

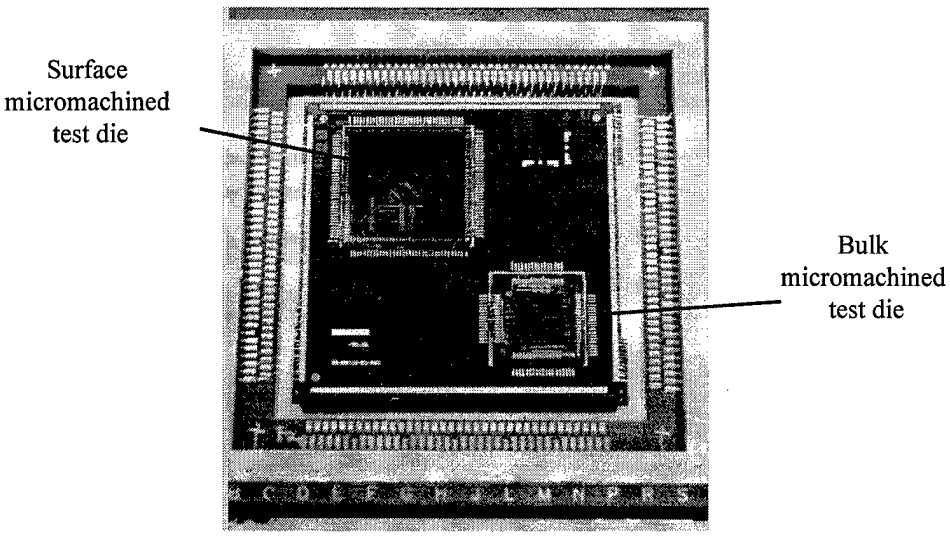


Figure 8-2. MCM-D/MEMS package.

8.4 Post Processing of MCM-D/MEMS Package

After packaging, the MCM-D modules were returned to AFIT for post-processing and release. The devices on the bulk micromachined devices were found to be more rugged than the surface micromachined devices due to their larger size and the nature of bulk micromachining. Bulk micromachined devices are sculpted out of the substrate which provides for good mechanical support. Moreover, unlike their surface micromachined counterparts which are located above the substrate, bulk micromachined devices are typically coplanar with the substrate and are not the highest feature on the die surface as shown in Figure 8-3. Consequently, the MEMS structures on the bulk micromachined test die are somewhat protected by the surrounding overglass and interconnect levels from incidental contact; but the surface micromachined devices are much more susceptible and vulnerable. In addition, bulk micromachined devices are much less likely to stick to the substrate as a result of rough handling or processing.

Hence, the decision was made to release the bulk micromachined test die first and attempt to protect it during the release of the surface micromachined test die.

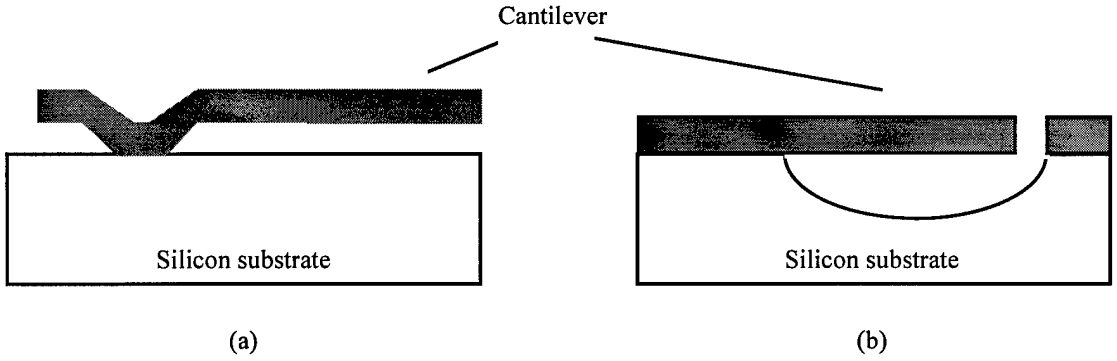


Figure 8-3. Comparison of (a) surface and (b) bulk micromachined cantilevers.

8.4.1 Post Processing of Bulk Micromachined Test Die

A wet etch procedure for releasing unpackaged bulk micromachined test die (Table 8-3) was initially planned. However, this wet etch procedure was not compatible with the packaging materials used in the MCM-D process [15]. The MCM-D module was not able to withstand the extended EDP or KOH etch. The polyimide dielectric used in the MCM substrate tended to crack and delaminate. Tetramethyl ammonium hydroxide (TMAH) was also tried as a substitute etchant for EDP, but the cracks and delamination still occurred. The cracks were large enough to allow etchant to penetrate the surface and delaminate the polyimide. In addition, no suitable mask was found to protect the other die in the module.

Table 8-3. Wet Etch Release Procedure for Bulk Micromachined Test Die.

1. Dip in 10 % hydrofluoric acid for 10 seconds
2. Soak in deionized water for 5 minutes
3. Etch in EDP at 95 °C for 45 - 60 minutes
4. Soak in deionized water for 5 minutes
5. Soak in 2-propanol for 5 minutes
6. Dry on hot plate at 50 °C

The inability to use a wet etch procedure led to the investigation of the feasibility of using xenon difluoride (XeF_2), which is an isotropic dry (gas phase) etchant for silicon. XeF_2 is a member of the fluorine-based silicon etchants which include ClF_3 and BrF_3 [9]. XeF_2 was first used to study the mechanisms of fluorine etch chemistry of silicon and was found to have high etch rates and reaction probabilities at room temperature [81]. The chemical reaction equation for the Si/XeF_2 etching process is [9]:

$$2\,XeF_2 + Si \rightarrow 2\,Xe + SiF_4 + Heat. \tag{8-1}$$

XeF_2 requires no external energy sources or ion bombardment to etch silicon, and it exhibits high selectivity to many metals, dielectrics, and polymers commonly used in microelectronic processing and packaging.

Efforts to gain permission to establish a XeF_2 etch chamber at AFIT were unsuccessful due to the special handling requirements needed for XeF_2 which is a combustible gas at room temperature and low pressure (< 4 Torr). In addition, the gas will form HF vapor in the presence of water which is also a safety hazard. As a result,

outside assistance was sought from Dr. Patrick Chu, a colleague at the University of California at Los Angeles (UCLA).

The MEMS research group at UCLA is a leader in exploring XeF_2 as a bulk silicon etchant. At UCLA, etching is conducted in a computer controlled multi-chambered system which provides precisely metered pulses of XeF_2 gas as shown in Figure 8-4. Dr. Chu and other researchers have discovered that the etch profile is more consistent and controllable when "pulses" of the gas are used as opposed to a prolonged exposure [9].

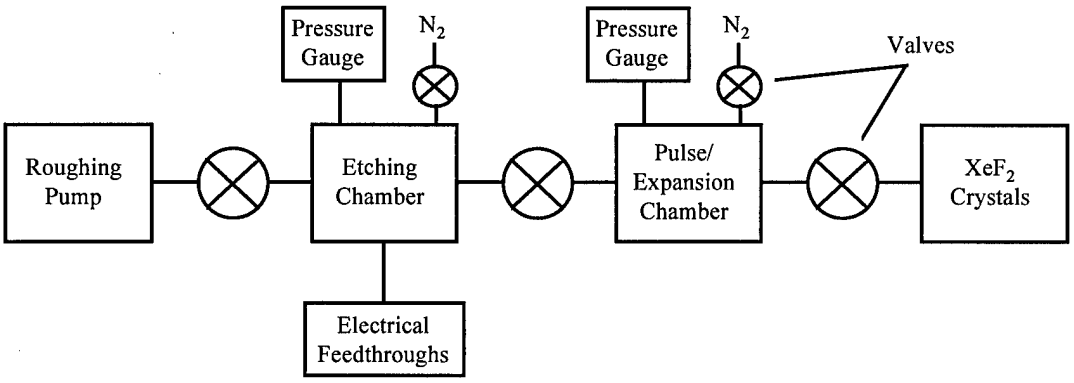


Figure 8-4. Block diagram of UCLA XeF_2 etching system (after Chu, et al. [9]).

A typical XeF_2 pulse etching cycle proceeds as follows. The target is placed in the etching chamber, and the roughing pump is used to evacuate both the etching and pulse/expansion chambers to a nominal pressure of ~ 20 mT. After evacuating the chambers, the valve between the etching and expansion chambers is closed in order to provide isolation. Next, the pulse/expansion chamber is filled with XeF_2 until the desired pressure is reached (typically ~ 3 Torr). The amount of XeF_2 contained in the expansion chamber at 3 Torr represents one "pulse".

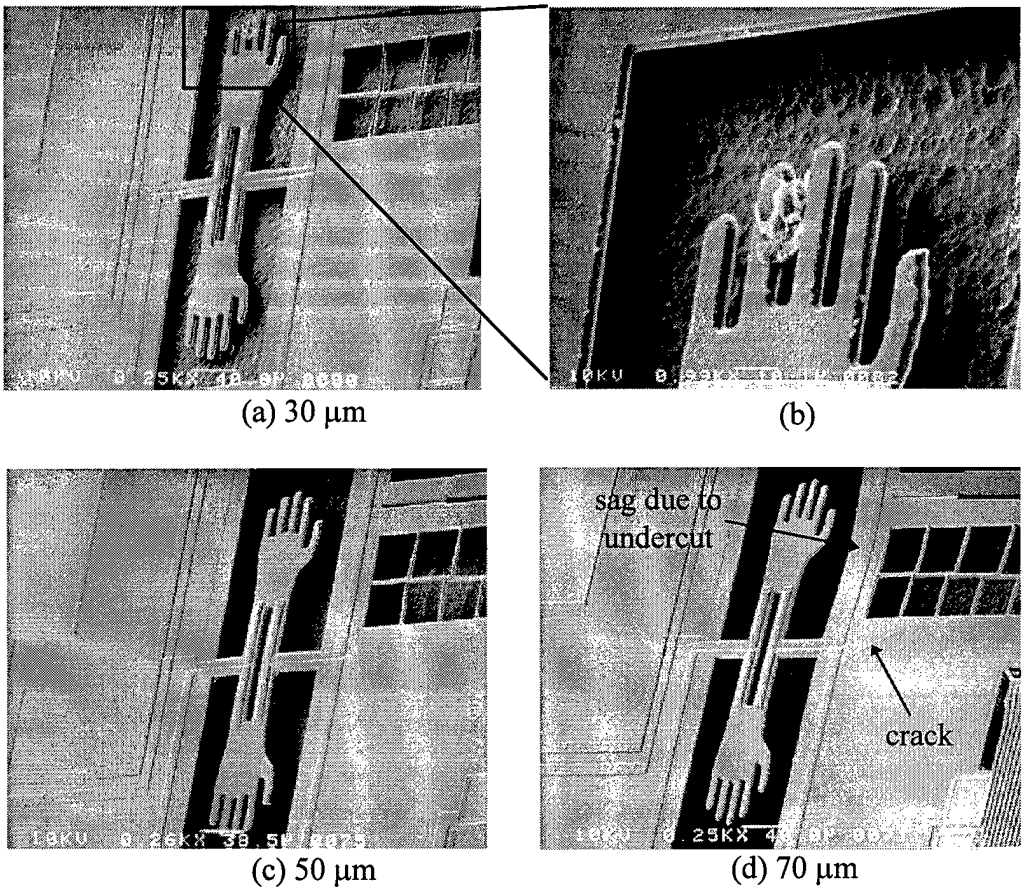
Once the pulse of XeF_2 is prepared, the valve between the etching and expansion chambers is then opened so that the XeF_2 vapor can flow into the etching chamber. The pressures in both chambers quickly equilibrate, and the target in the etching chamber is etched for a fixed amount of time. Both chambers are then evacuated and purged with three short bursts of nitrogen to complete the pulse cycle.

The etch rate per pulse depends on etch window dimensions and how much etching has previously occurred. The etch rates range from 3 to 5 μm per pulse vertically and 1.75 to 4.25 μm per pulse laterally [9]. A decrease in etch rate is apparent for smaller openings indicating a diffusion limited aperture effect. In addition, the rate of etching is much greater during the initial 15 seconds of a pulse. After 4 minutes, the etch rate drops off dramatically [9].

While several of the more common microelectronic materials had been tested for compatibility with XeF_2, UCLA researchers had not considered the use of XeF_2 for post-release of MCM packaged MEMS and had not performed any research in this area. As a result, packaging samples and test die were sent to UCLA to test their compatibility with XeF_2. The bulk micromachined test die were originally designed for release by an anisotropic etch; however, it was determined that the MEMS structures could be safely and reliable released with XeF_2 by monitoring the progress of the etch.

Three different etch depths (30, 50, and 70 μm) were used for releasing the bulk micromachined die. Since it was not possible to make an in-situ measurement of the etch depth, the die was periodically taken out of the etch chamber and inspected under a microscope. The process was continued until the desired amount of etching was

observed. Figure 8-5 shows a comparison of a test structure etched to a depth of 30, 50, and 70 μm.



(a) 30 μm (b)

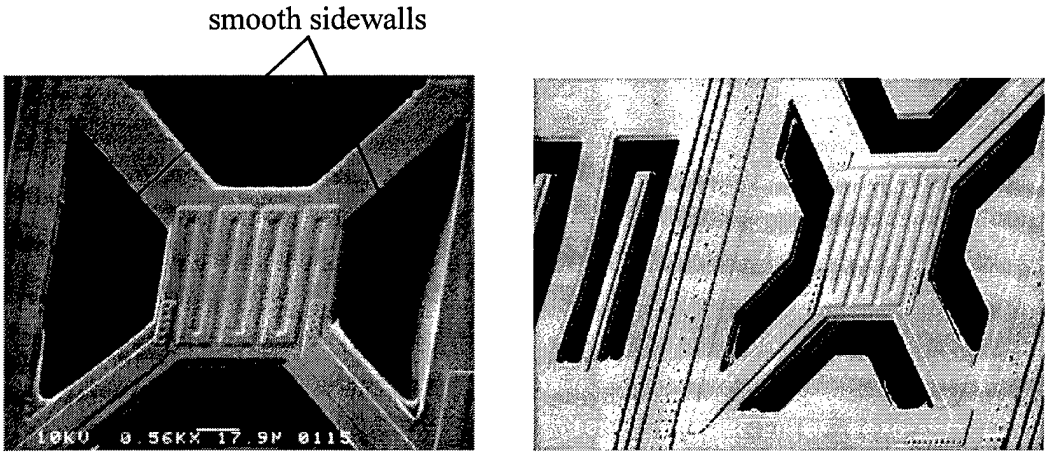
(c) 50 μm (d) 70 μm

Figure 8-5. Bulk micromachined test structure etched by XeF_2 to a depth of (a) 30 μm, (c) 50 μm, and (d) 70 μm. A close-up of the 30 μm example (b) reveals the silicon surface roughness characteristic of XeF_2 etching.

Figures 8-5 and 8-6 visually illustrate some of the differences between MEMS devices formed through anisotropic and isotropic etching. The smooth, angled sidewalls of the suspended plate shown in Figure 8-6 (a) are characteristic of anistropically etched devices. The convergence of the sidewalls at the bottom of the pit provides for a built-in etch stop. Conversely, the isotropically etched plate in Figure 8-6 (b) does not have

visible sidewalls because the silicon is being etched at nearly the same rate in all directions.

Moreover, isotropically etched silicon tends to have a rough surface as compared to anisotropically etched surfaces (compare Figure 8-5 (b) and Figure 8-6 (a). The smooth surface of the anisotropically etched silicon is a result of the silicon being etched along a crystal plane. The isotropic etch process does not have this natural boundary and proceeds non-uniformly across the surface.



(a) anisotropically etched (EDP) (b) isotropically etched (XeF_2)

Figure 8-6. Comparison of (a) anisotropically and (b) isotropically etched suspended structures.

Figure 8-5 also demonstrates one of the disadvantages of isotropic etching which is the requirement to accurately time or monitor the etch. Unlike anisotropic etchants which have natural mechanisms to stop progress of the etch, the isotropic nature of XeF_2 can create undesirable undercutting of surrounding support structures if the etching is not stopped. Figure 8-5 (d) shows that the 70 μm etch removed all of the bulk silicon underneath the support structures and created an undesirable sag in the frame. In

addition, cracking of the oxide occurred on the 70 μm sample due to the same phenomena. The 30 and 50 μm etches produced much less damage due to undercutting.

The package samples subjected to the XeF_2 release procedure did not show any signs of being impacted by exposure to the gas. The package samples consisted of unpopulated MCM-D substrates and ceramic chip carriers similar to the ones used for holding the MMS MCM-D substrates. Package samples were placed in the etch chamber with the test die during the longest release experiment (70 μm). Inspection of the package samples after etching by both Dr. Chu and the author revealed no impact to either the substrate or chip carrier after the prolonged exposure to XeF_2.

After the compatibility of the test die and the package samples was established, a populated MCM-D/MEMS package was etched in the XeF_2 chamber. The module was etched to an approximate depth of 50 μm. Figure 8-7 shows some of the released microstructures on the MCM-D/MEMS packaged test die. The surface micromachined die was masked to protect it from the XeF_2 etch. One of the benefits of XeF_2 is that it is easily masked. Common materials such as photoresist and silicon oxide can be easily and effectively used for masking [82]. The author must confess that *masking tape* was literally and successfully used as the mask during the first experiment.

8.4.2 Post Processing of Surface Micromachined Test Die

The surface micromachined die in the MCM-D/MEMS package was released after XeF_2 etching of the bulk micromachined die. The MCM-D package was known to able to withstand the wet etch procedure for the surface micromachined test die (Table 8-4)

[15,83]. Consequently, the main issue was protection of the released bulk micromachined die.

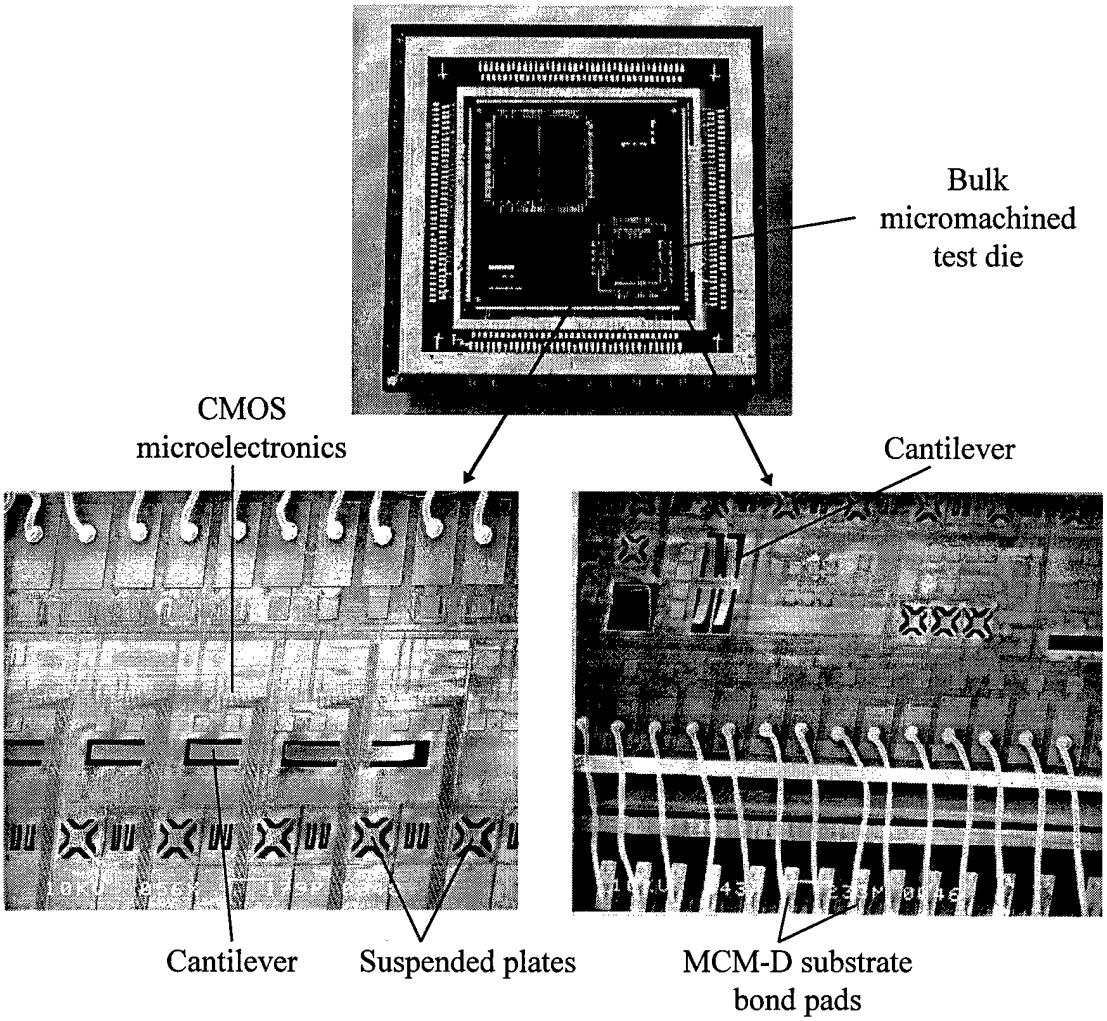


Figure 8-7. Released bulk micromachined test die on the MCM-D/MEMS module.

Table 8-4. Wet Etch Release Procedure for Surface Micromachined Test Die.

1. Soak in 2-propanol for 5 minutes
2. Dry on hot plate at 50 °C
1. Etch in 49% hydrofluoric acid for 2 min. 30 sec.
2. Dip in deionized water for 5 seconds
3. Soak in 2-propanol for 10 minutes
4. Dry on hot plate at 50 °C

8.4.3.1 Processing for Released Devices

Several encapsulants and masks were investigated for resistance to the HF etch used for releasing the MUMPs surface micromachined test die. It was discovered that epoxy encapsulants, spin-on polyimide, and negative photoresists were able to withstand the HF etch but were impossible or at least difficult to remove cleanly and also tended to damage the structures on the released bulk micromachined test die. So while these materials could be used as a non-removable mask, they were not suitable for the case at hand.

A solution to the problem was found by changing the problem. The only encapsulant tested which was easy to apply and remove without damaging the released bulk micromachined test die was positive photoresist. Even when fully baked, the Shipley 1350 photoresist was easily and cleanly removed in an acetone rinse. Unfortunately, the positive photoresists were unable to withstand immersion in the HF long enough to release the MEMS devices. However, it was found that positive photoresist was an effective mask against the HF vapor if the masked region was not immersed in the acid bath. Even when not immersed in the acid, the HF vapor is still capable of etching silicon dioxide which necessitates the use of a protective mask.

8.4.3.2 Release of Surface Micromachined Test die

Following the decision to use positive photoresist, the released bulk micromachined die in the MCM-D package was carefully coated with Shipley 1350 positive photoresist and soft baked for 20 minutes at 60 °C. The procedure in Table 8-4 was then used to successfully release the devices on the MCM-D packaged surface

micromachined test die. The bulk micromachined die was not submerged in the HF bath during the release process. Figure 8-8 shows devices on the surface micromachined die. Following release, the entire module was soaked in acetone for 10 minutes to remove the protective photoresist from the bulk micromachined test die and then cleaned in methanol.

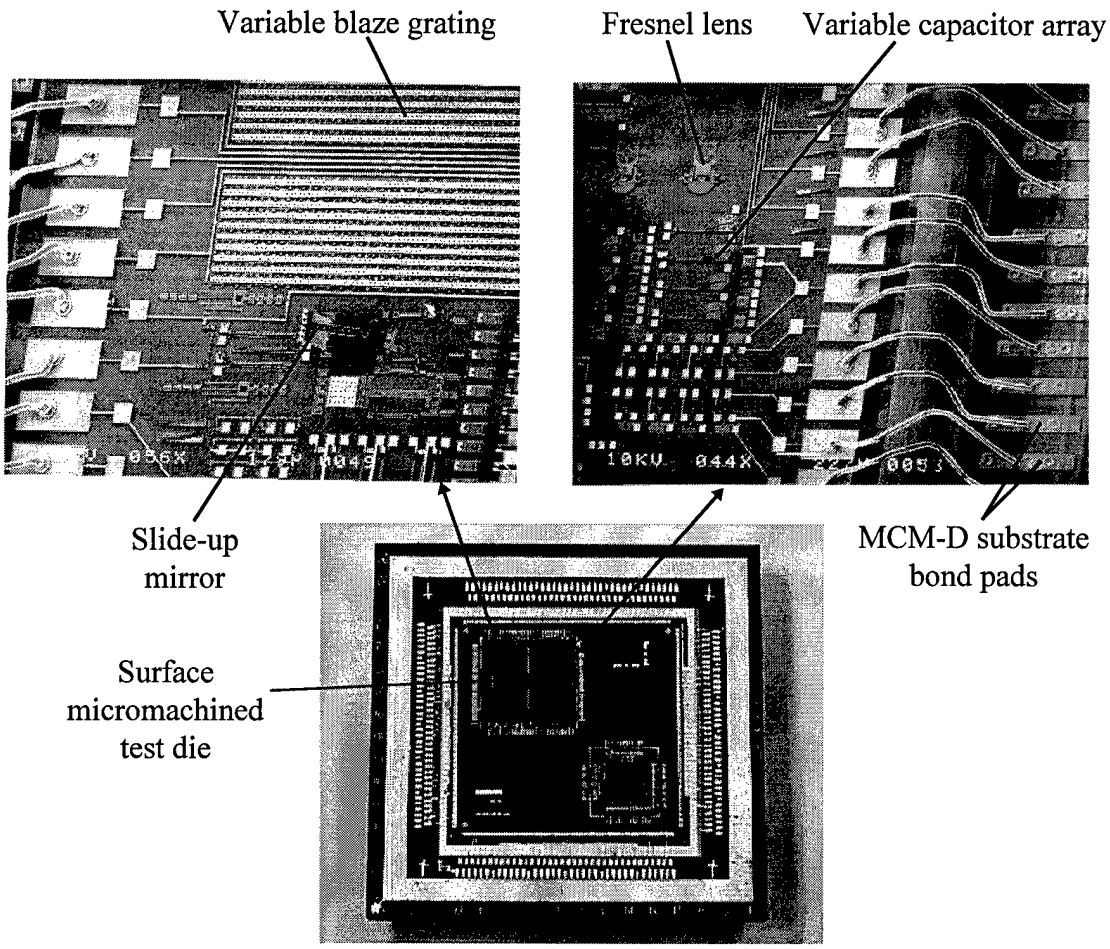


Figure 8-8. Released surface micromachined test die on MCM-D/MEMS module. The slide up mirror was manually assembled after release.

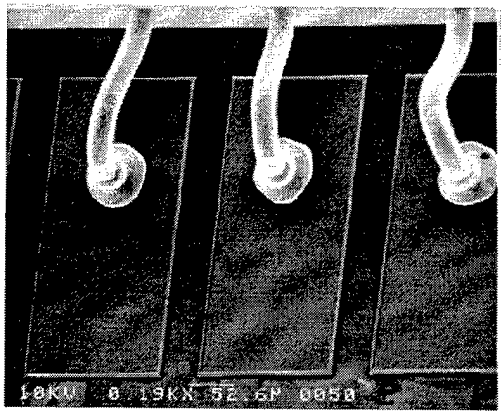
Subsequent analysis of the module showed no impact to the bulk micromachining test chip or MCM wiring. In addition, good conductivity was observed from the MCM

package pins to the pads on both MEMS die, and the CMOS electronics on the bulk micromachining test die performed as expected. Figure 8-9 shows wirebonds connecting the bulk micromachined test die to the MCM-D substrate after undergoing the entire battery of processing to include release of the both test die and removal of the protective photoresist.

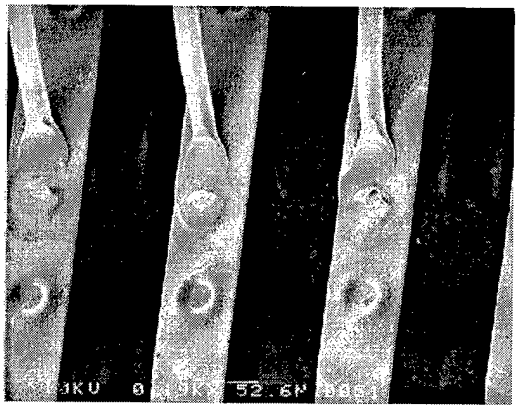
The wirebonds appear unaffected by any of the processing with the exception of the bond wires being slightly bent due to application and removal of the photoresist masks used during the various stages of processing. The electrical performance of a ring oscillator on the bulk micromachined test die was the same before and after release. This is a good indication that the wirebonds were not affected by the release process since the oscillator requires four of the wirebonds to complete the circuit.

The results of the various experiments demonstrate that bulk and surface micromachined MEMS can be packaged and released using foundry MCM processes using the proposed techniques. Furthermore, xenon difluoride (XeF_2) was found to be an excellent post-packaging etchant for MCM-D packaged bulk micromachined MEMS die. For surface micromachining, hydrofluoric acid can be used for post-packaging release of MEMS and can be masked for short (< 5 min.) etches.

The case study solved in this experiment was somewhat complex in that two types of MEMS die were packaged in the same MCM. A more likely scenario would include a particular MEMS device and some type of microelectronic control chip. In this case, the problem becomes much easier since the microelectronics die can be permanently masked which enables a much wider selection of masks to be used.



(a) Bond pads on MCM-D packaged bulk micromachined test die



(b) Bond pads on MCM-D substrate

Figure 8-9. Wirebond attachments on the (a) bulk micromachined test die and (b) MCM-D substrate after release of both test die and removal of photoresist.

8.5 MCM-D Packaging of Pre-released MEMS

The majority of the discussion in this chapter has focused on post-packaging release, but pre-released die can also be MCM-D packaged if carefully handled. AFIT researchers have successfully packaged and bonded hundreds of surface and bulk

micromachined die into ceramic chip carriers. These packages have similar material composition to many MCM-D packages. Also, success has been achieved by employing MEMS devices wire bonded into "MCM-D like" packages by personnel at the Air Force Research Laboratory who were not familiar with MEMS. Figure 8-10 shows a multichip module designed by the author and packaged by the Air Force Research Lab as part of a work order. There was no face-to-face contact with the technician until after the project was complete.

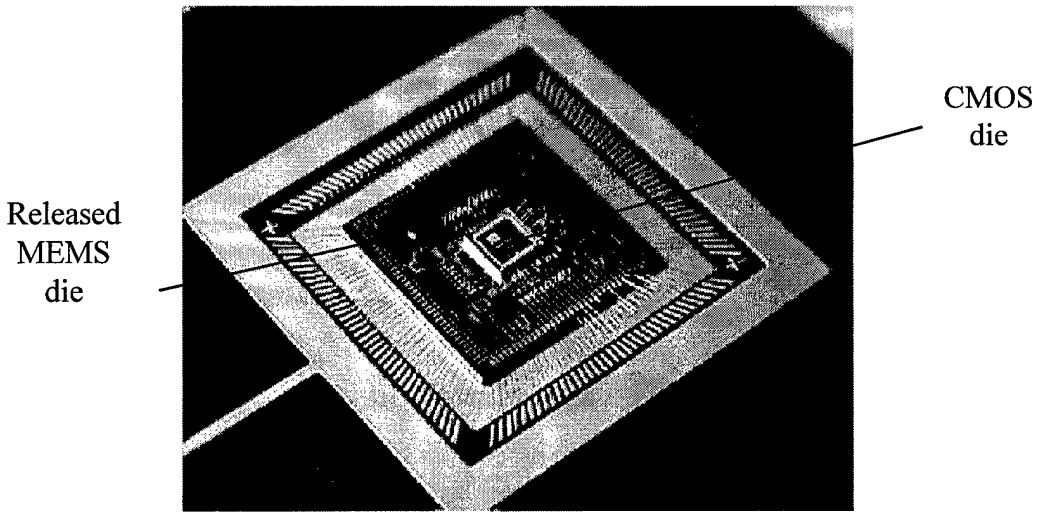
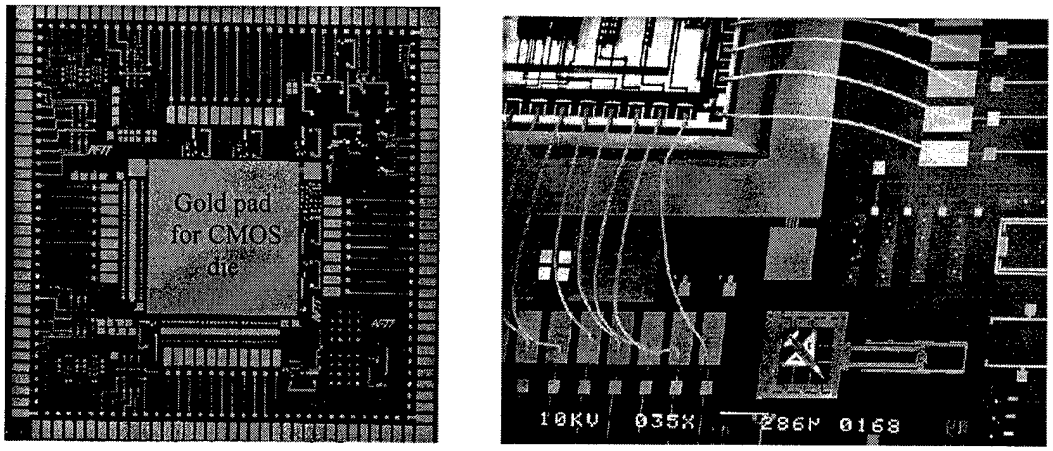


Figure 8-10. CMOS and pre-released MEMS die packaged in a MCM-D package. The die were wirebonded by technicians at the Air Force Research Lab in a foundry-like transaction.

The MCM-D package of Figure 8-10 was implemented in order to demonstrate functional and physical integration of MEMS and CMOS. The MMS MCM-D foundry would have been preferred, but cost and schedule concerns led to the development of an

inexpensive MCM-D module which could be fabricated locally while still meeting the desired research objectives.

Unlike the MMS MCM-D where each of the two die has its own attachment to the substrate, the CMOS die in the pseudo-MCM-D module is stacked on top of the MEMS die. The layout of the MEMS die was designed to support the physical and electrical attachment of a small CMOS ASIC. This was accomplished by providing a large gold pad in the center of the MEMS die and an internal pad frame for connecting the CMOS die as shown in Figure 8-11. The CMOS die is bonded to the gold pad and then wire bonded to the internal pad frame. The internal pad frame is connected to the outside pad frame through gold wiring on the MEMS die.



(a) (b)

Figure 8-11. (a) MEMS die designed for attachment of CMOS controller. The die was fabricated through MUMPs, and the large gold pad is square with 3500 μm sides. The attached CMOS die is shown in (b).

The MEMS die can be released before or after assembly and packaging. The CMOS ASIC can be protected by a coat of negative photoresist prior to the HF bath to

allow the MEMS devices to be released after bonding. However, the electrochemical etch phenomena discussed in Chapter 5 can damage many of the devices. Thus, pre-release processing was found to be preferable for this situation. For pre-release packaging, the MEMS die was glued to a pin grid array (PGA) package and then released using the procedure in Table 8-4. The CMOS die was then glued to the gold pad on the MEMS die and wire bonded to the internal pad frame. The external pad frame was subsequently wire bonded to the PGA bond pads to complete the module. A completed module is shown in Figure 8-12.

Testing of the stacked die MCM-D module demonstrated that the die were functionally as well as physically integrated. Both of the CMOS ASIC chips described in Chapter 6 were packaged with and used to control MEMS devices in the module. A computer was used to provide digital inputs to the CMOS ASIC which in turn controlled the actuation of thermal micromirrors, electrostatic micromirrors, and lateral thermal actuator arrays.

Appropriate and prudent handling of the die was a key ingredient to the successful implementation of the stacked die MCM-D. Technicians at the Air Force Research Lab "foundry" processed the die and modules manually since only eight packages were being fabricated. Similarly, all of the processing done by the author was also performed by hand. Unfortunately, microelectronic packaging foundries use automated methods for handling die, and the pick and place machinery used currently is clearly unsuitable for released MEMS devices.

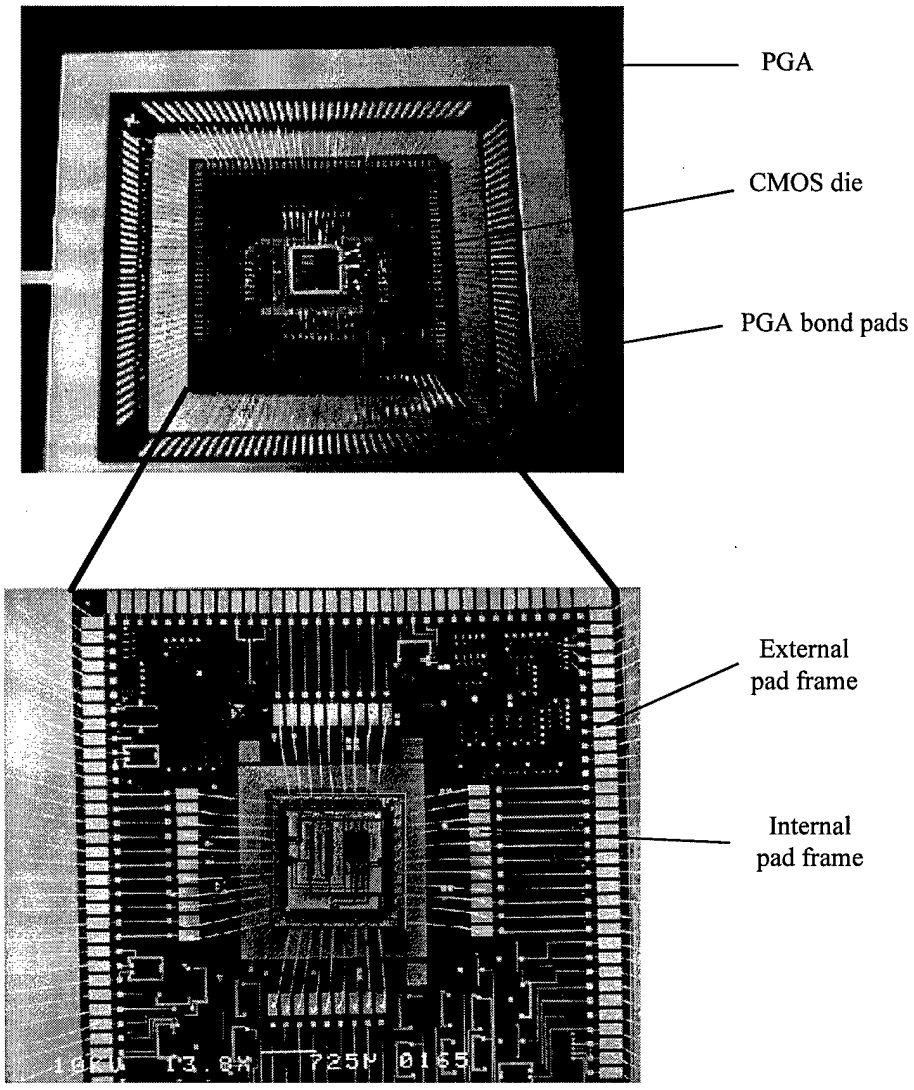


Figure 8-12. Completed "stacked die" MCM-D in PGA-144 package.

These experiments show that released MEMS can by effectively handled and packaged; and once the manufacturing of MEMS reaches volume production, it should be possible to devise different types of handling machinery to adeptly process and package released MEMS in an automated foundry environment. This would provide a logical

complement to the post-packaging release methodologies developed during the course of this research.

8.6 Summary

The feasibility of co-packaging of bulk and surface micromachined MEMS using a foundry MCM-D process has been established. A surface and bulk micromachined test die were packaged in the Micro Module Systems MCM-D foundry. The bulk micromachined die was released using xenon difluoride (XeF_2) marking the first use of this etchant for post-processing of MCM packaged MEMS. XeF_2 is a gas phase silicon etchant which exhibits high selectivity of silicon over other materials commonly found in MCM packages. Hydrofluoric acid was used for post-packaging release of the surface micromachined test die. Simple and effective masking techniques were developed to allow both die to be packaged and released in the same module.

Functional and physical integration of MEMS and CMOS was demonstrated through the use of a "stacked chip" MCM-D in which the CMOS die was attached to the surface of the MEMS die. This MCM-D module incorporates many of the key concepts developed in earlier chapters such as CMOS controllers for MEMS, MEMS device development, and microsystem modeling and simulation.

Chapter 9. High Density Interconnect/MEMS Packaging

9.1 Introduction

High density interconnect (HDI) MCMs have great potential for MEMS packaging due to the combination of high performance electrical interconnects with the ability to physically protect microelectronics or other die under the overlay. HDI MCMs are unique in that the die are embedded in the substrate as opposed to the MCM-D package where the die are located on top of the substrate. Hence, the potential for MEMS packaging using the General Electric HDI foundry was investigated.

Unlike the MMS/MCM-D, the HDI process required additional processing for MEMS. Therefore, General Electric, the developer of the HDI process, was contacted to assist in developing a low impact method of adapting the HDI foundry process for MEMS packaging. In addition, Chip-on-Flex (COF), a variant of the standard HDI process, was also investigated for MEMS packaging. The MEMS packaging test die described in Chapter 8 were used to evaluate the success of the experimental packaging procedures.

9.2 Description of High Density Interconnect and Chip on Flex Processes

A basic description of the HDI and COF processes is necessary for understanding the packaging experiments described in later sections. The HDI process is described in Chapter 7 and will be briefly covered in this chapter for completeness. An overview of the COF process is also presented in this section.

9.2.1 High Density Interconnect

The standard high density interconnect (HDI) procedure consists of embedding bare die into cavities milled into a base substrate and then fabricating a thin-film interconnect structure on top of the components. The first step in the process is to mechanically mill cavities in the ceramic substrate as shown in Figure 9-1. Each cavity is precisely milled to match a specific die so that the surface of each embedded die will be coplanar with the substrate surface after the module is populated. If necessary, a metal layer can also be deposited on the substrate to provide an electrical contact to the bottom of the die. After milling the substrate, the die are bonded into the cavities using conductive or non conductive adhesives [70].

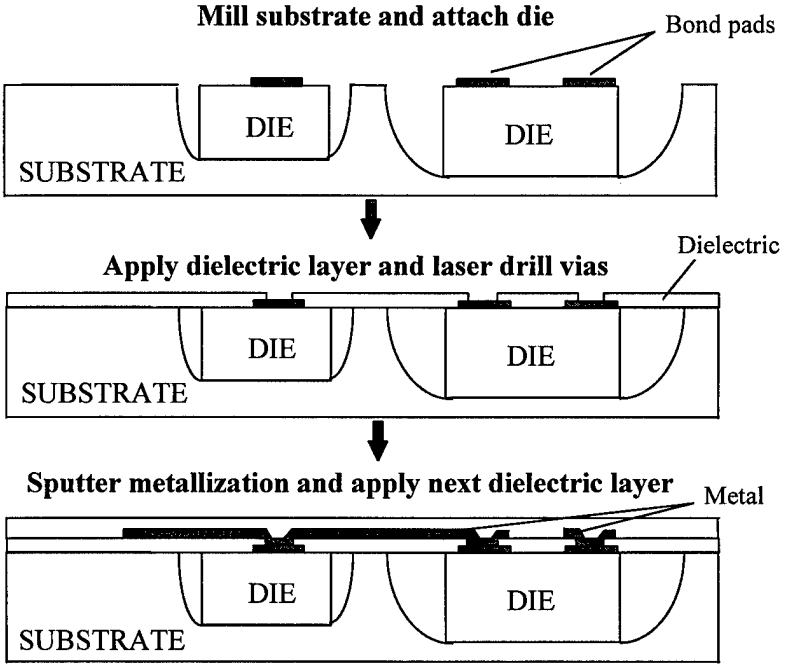


Figure 9-1. Standard HDI process (after W. Daum, et al. [70]).

The HDI interconnect overlay is fabricated after the die have been secured into the substrate. The first layer in the HDI interconnect overlay is constructed by bonding a sheet of dielectric film on the substrate. A 25 μm thick film of Kapton is typically used, and a thermoplastic such as Ultem is used for the adhesive [70]. After the dielectric layer is laminated, via holes are drilled directly through the dielectric film to the component bond pads using laser ablation (Figure 9-1). The Ti/Cu/Ti metallization used for the die interconnects is then created through sputtering and photolithography. Additional layers can be added to create a multilevel interconnect structure.

9.2.2 Chip-on-Flex

The Chip-on-Flex (COF) technology is an extension of the HDI technology and was developed only in the last few years [84]. COF was created to provide a low cost, multichip packaging solution which would approach the performance of high-end MCMs such as the General Electric (GE) high density interconnect (HDI) [84]. Table 9-1 compares the characteristics of HDI and COF modules. Furthermore, COF provides the capability for chip scale packaging (CSP) which can also be of great benefit to MEMS die that need to be individually packaged.

COF processing retains the interconnect overlay used in HDI, but molded plastic is used in place of the ceramic substrate. Figure 9-2 shows the COF process flow. Unlike HDI, the interconnect overlay is prefabricated before chip attachment. The bottom layer of the overlay is usually Kapton. The top layer of the overlay can also be

Kapton; however a spin-on or spray-on polyimide such as Ultradel can be substituted for the top dielectric. Copper is used for metallizing the prefabricated overlay.

The chip(s) are attached face down on the COF overlay using a polyimide or thermoplastic adhesive. After the chip(s) have been bonded to the overlay, a substrate is formed around the components using a plastic mold forming process such as transfer, compression, or injection molding. The module temperature does not exceed 210 °C during the substrate molding [85].

The next step in the process is to electrically connect the die to the overlay. This is accomplished by laser drilling vias through the overlay to the component bond pads. Next a Ti/Cu metallization is sputtered and patterned to form the electrical interconnects. Different types of top layer metallizations can be used depending on the target application [84].

Table 9-1. Characteristics of HDI and COF Packages.

Property	HDI	COF
Substrate material	Alumina	Molded plastic
Signal/power wiring layers	9 (1 layer used in this research)	3 (1 layer used in this research)
Overlay dielectric material	Kapton	Kapton/Ultradel
Conductor metallization	Ti/Cu/Ti	Ti/Cu/Ti/TiW/Au/TiW
Die attach adhesive	Ultem	Ultem
Die interconnect method	Direct metallization	Direct metallization
Die edge-to-edge spacing	> 375 μm	> 800 μm
Max operating frequency [70]	> 1 GHz	> 1 GHz

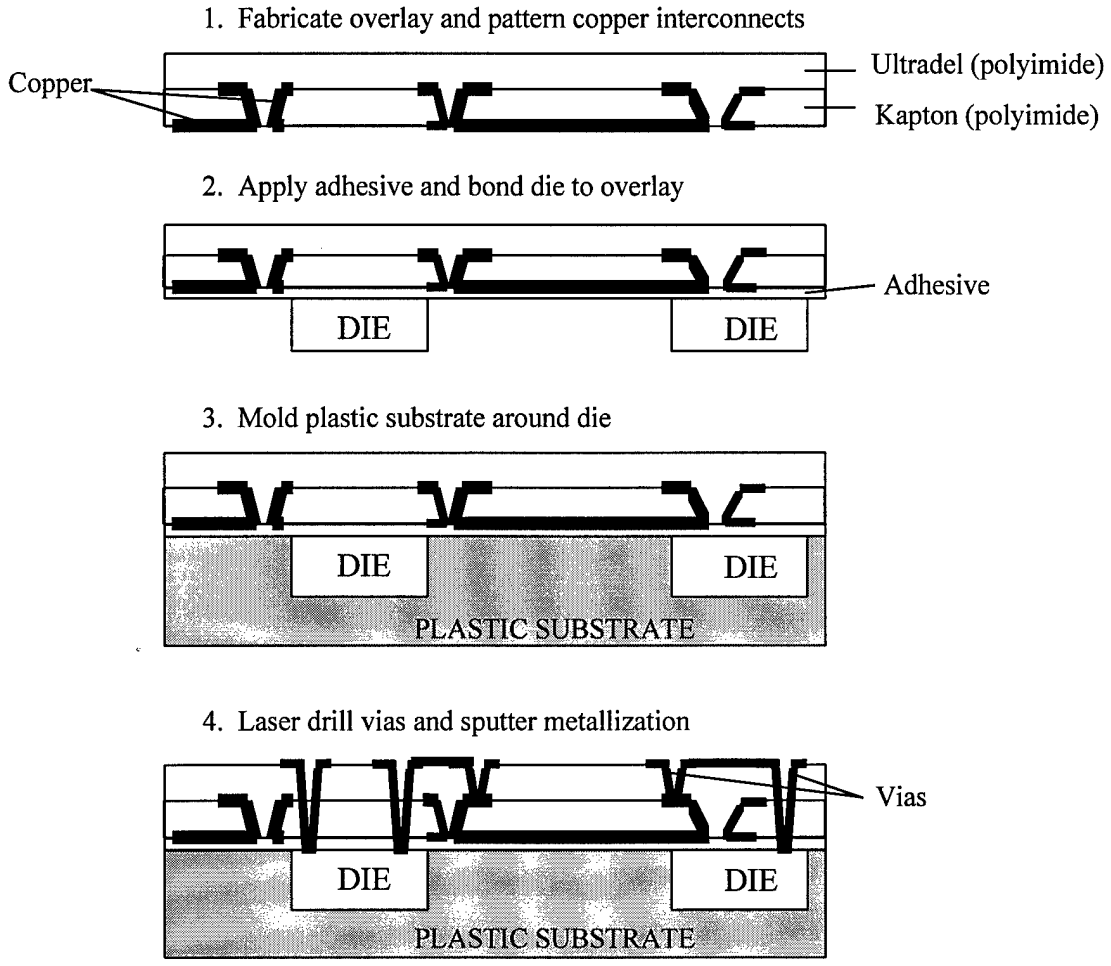


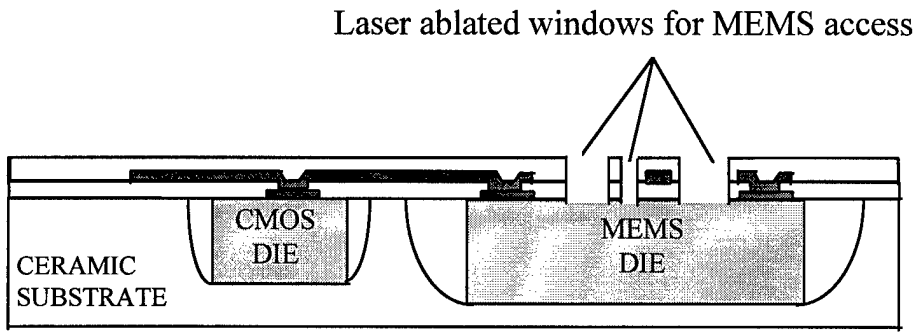
Figure 9-2. Chip-on-Flex process flow (after R. Fillion, et al. [84]).

9.3 Packaging and Post Processing of HDI and COF/MEMS Packages

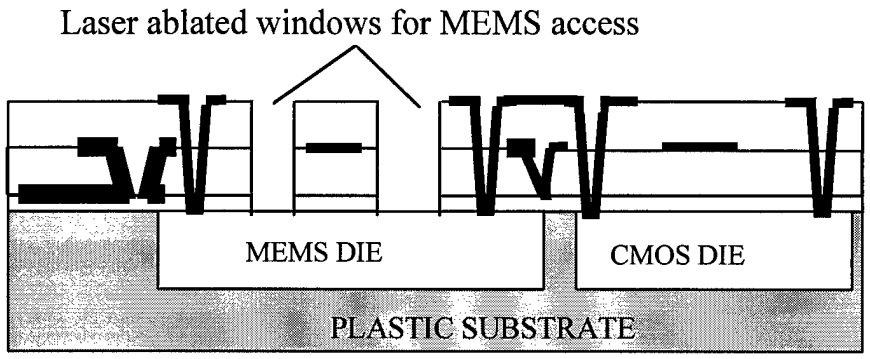
9.3.1 Modifications to HDI/COF Process for MEMS Packaging

Since the die are embedded in the overlay, both HDI and COF need additional processing in order to provide access to the MEMS devices. The selected approach for

packaging MEMS die in the HDI (or COF) process is to add an additional laser ablation step to allow physical access to the MEMS devices as shown in Figure 9-3. Additional plasma etching is also performed to minimize the ablated dielectric residue which can accumulate in the exposed windows.



(a) HDI/MEMS Package



(b) COF/MEMS Package

Figure 9-3. Large area ablation for MEMS access in (a) HDI and (b) COF package.

The metallization in the HDI/COF process is also modified for MEMS packaging. Typically, a Ti/Cu/Ti metallization is used. However, the hydrofluoric acid used in the

release of the surface micromachined test die will etch away the top Ti layer and will expose the copper layer. This is undesirable because exposed copper will oxidize.

Consequently, a more complex metallization was implemented for MEMS packaging using a Ti/Cu/Ti/TiW/Au/TiW structure. The tungsten in the intermediate TiW layer is used as barrier between titanium and gold to allow good adhesion of the metals. The top TiW layer is used to promote adhesion to the polymer adhesives used in fabricating the overlay. After ablation and MEMS release, the top TiW layer is removed by the hydrofluoric acid and exposes the gold layer.

9.3.2 HDI/COF Packaging Procedure

Both the surface and bulk micromachined test die were packaged at the General Electric Corporate Research and Development Center using the standard HDI and COF procedure. The test die were packaged in modules containing a generic CMOS electronics die and ablation test cells. Figure 9-4 shows a layout of one of the COF/MEMS modules.

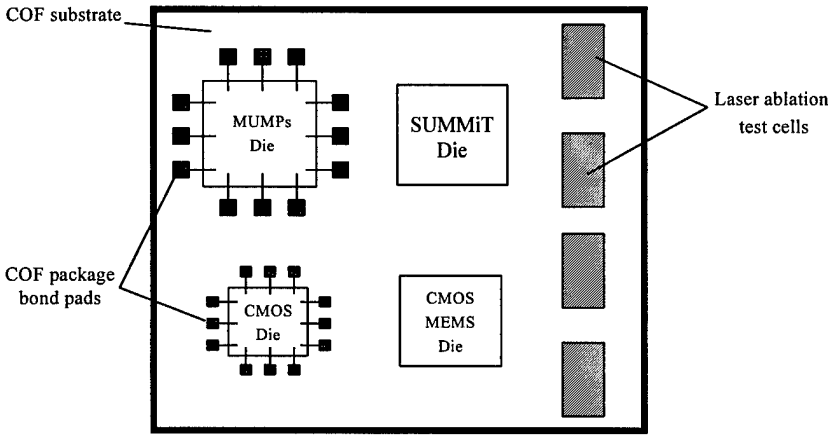


Figure 9-4. COF/MEMS MCM fabrication layout.

After passivation, windows in the dielectric overlay above the MEMS die were selectively opened using laser ablation. The ablation was accomplished with a continuous argon ion laser (350 nm wavelength). The laser spot was circular with a nominal diameter of 9 μm. The initial laser power was approximately 1.6 W and the scan rate was 360 μm/sec for the first fabrication lot. For subsequent lots, the ablation power was varied to reduce the risk of damage to the MEMS die. The bulk of the overlay was ablated at a high power and then the laser power was reduced to minimize the likelihood of device damage. The laser ablation process is covered in more detail later in this chapter, and the complete COF/MEMS process sequence flow is listed in Appendix C.

Some of the attractive features of the COF/HDI MCM are illustrated in Figure 9-5 which shows a populated COF and HDI/MEMS package. First, each package has a thin profile of approximately 1.5 mm which compares favorably to a dime. In addition, co-packaged die can be placed in close proximity to each other. The CMOS and surface micromachined die of Figure 9-6 are nearly 5 mm apart in the HDI package, but they can be placed as close as *0.375* mm apart in HDI. The minimum die spacing in the COF process is larger (0.8 mm), but this is still an impressive capability compared to most other packaging technologies.

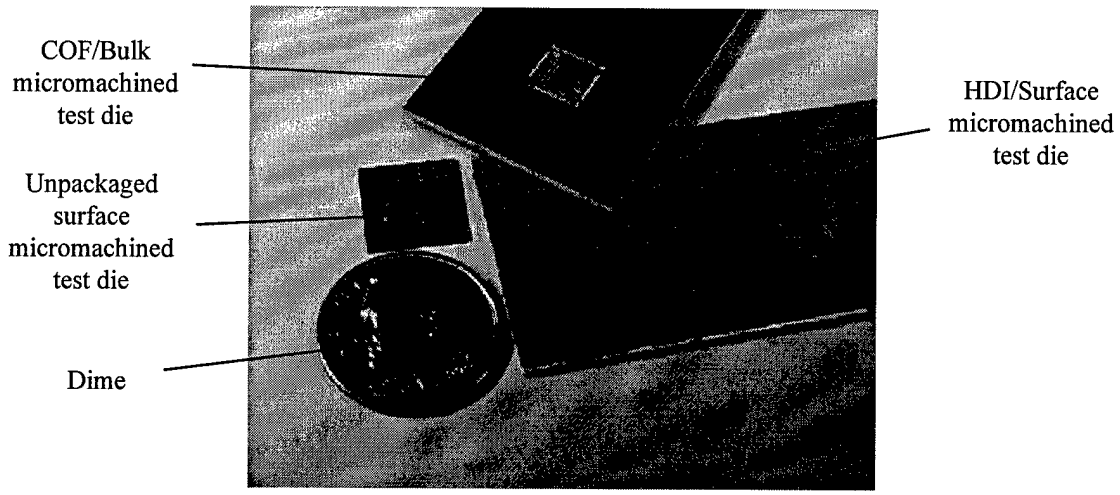


Figure 9-5. HDI and COF/MEMS packages.

The wiring density is also impressive. The HDI package in Figure 9-6 has a center-to-center wire spacing of 350 μm. However, both HDI and COF are capable of supporting a center-to-center wire spacing of 150 μm. Moreover, the HDI and COF process can support arrays of ball grid array (BGA) pads which can be located virtually anywhere on the die [84]. The use of BGA pads greatly increases the number of I/O pads which can be used in a given area.

9.4 HDI/COF Packaging of Surface Micromachined Test Die

9.4.1 HDI/COF Packaging of MUMPs Die

Three different MUMPs fabricated test die were used for the HDI/COF packaging experiments. The first MUMPs packaging test die was a legacy from Comtois' dissertation research [15]. The other two die were designed. Figure 9-7 shows a layout of one of the test die and some of the various test structures.

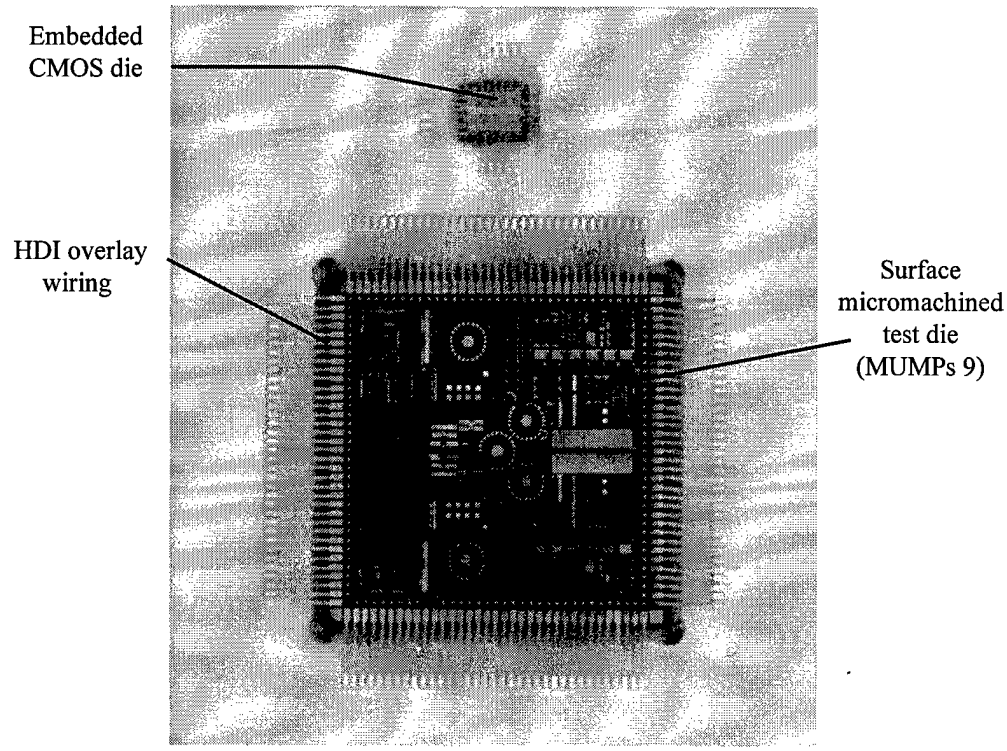


Figure 9-6. Close-up of HDI/MEMS MCM package.

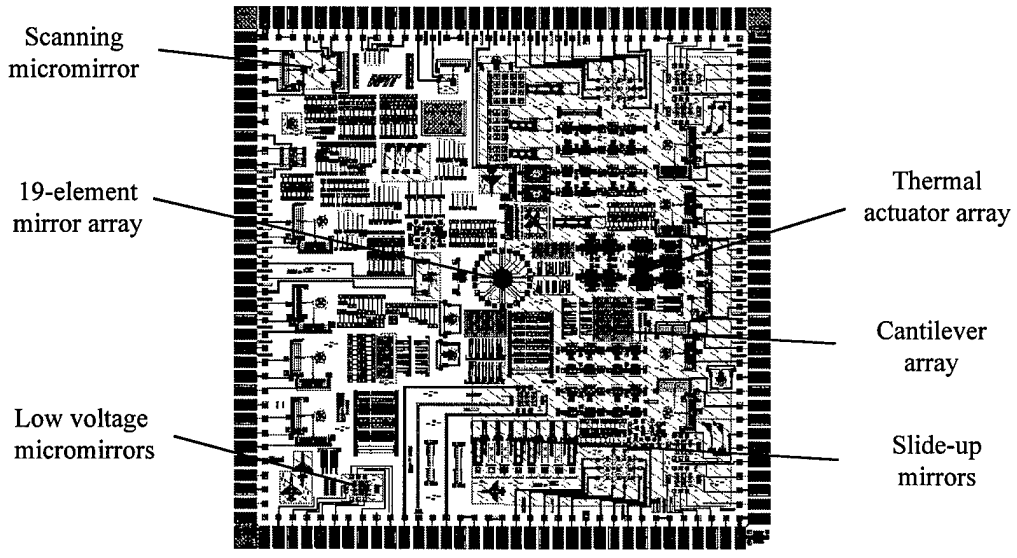


Figure 9-7. MUMPs 19 test die for HDI/COF Packaging.

The process for packaging and releasing the surface micromachined test die was as follows. The test die were packaged at GE using the standard HDI or COF process. Next, a pattern was ablated in the overlay to expose the MEMS devices and bond pads. Only one laser ablation pattern was used for all of the MUMPs test die in order to minimize cost and schedule. The computer-generated artwork to define the laser ablation pattern is done by GE from high resolution imagery of the die. This process is time-consuming and can be costly. Figure 9-8 shows the ablation pattern used for the HDI/COF packaging experiments. The pattern contains a large window and a set of smaller openings. The large window is approximately 8000 μm long and 4600 μm wide, while the smallest window is 370 μm long and 170 μm wide.

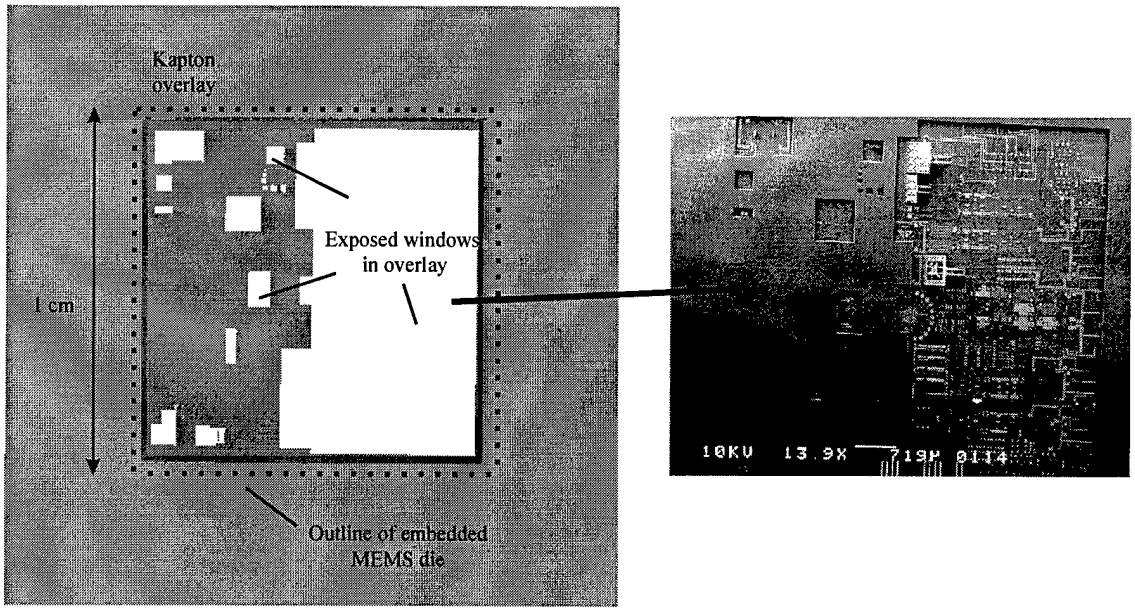


Figure 9-8. Ablation pattern used for MUMPs test die.

The modules were sent to AFIT for release after HDI or COF packaging. None of the surface micromachined test die were released before packaging due to concerns that

the fragile MEMS devices would not survive the packaging process. The HDI/COF packaged surface micromachined test die were released using the procedure shown in Table 9-2. Material compatibility tests conducted prior to packaging indicated that the Kapton dielectric, adhesives, and substrates used in the HDI and COF packages would survive the release procedure [15]. The release of the packaged MEMS test die was successful with no evidence of device 'stiction' to the substrate or deterioration of the HDI or COF package.

Table 9-2. HDI/COF Release Procedure for Surface Micromachined Test Die.

1. Etch in 49% hydrofluoric acid for 2 min. 15 sec.
2. Rinse in deionized water for 5 seconds
3. Rinse in 2-propanol for 10 minutes
4. Dry on hot plate at 50 °C

In general, the MEMS devices on the packaged test die performed electrically and mechanically the same as devices on unpackaged control die. Rotating, hinged and flip-up devices moved freely and operated as designed. In addition, devices were operated through the package bond pads which demonstrated good continuity through the overlay and onto the MEMS die. Figure 9-9 shows exposed package bond pads on a COF module. Finally, the HDI/COF overlay protected the CMOS die from the release etch as predicted by the material chemical compatibility tests. Figure 9-10 shows several of the ablation windows in the HDI overlay as well as a close-up of a micromirror array.

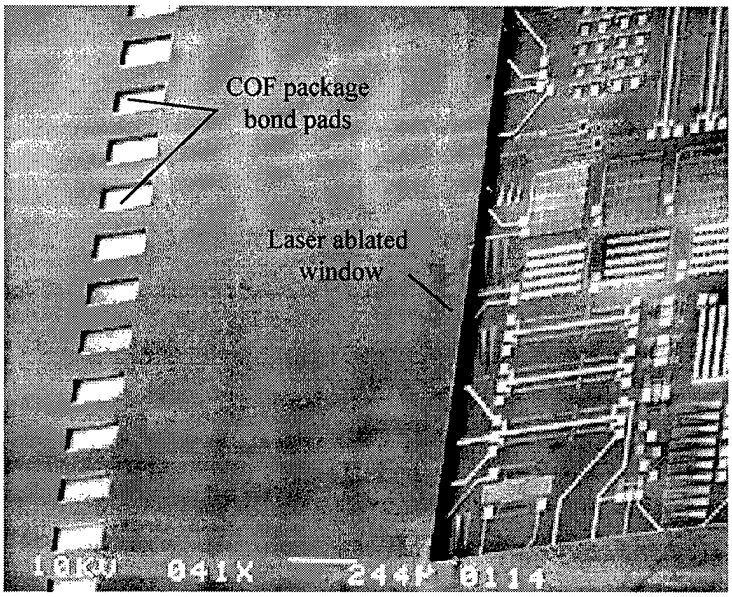


Figure 9-9. COF package bond pads exposed through laser ablation (MUMPs 15).

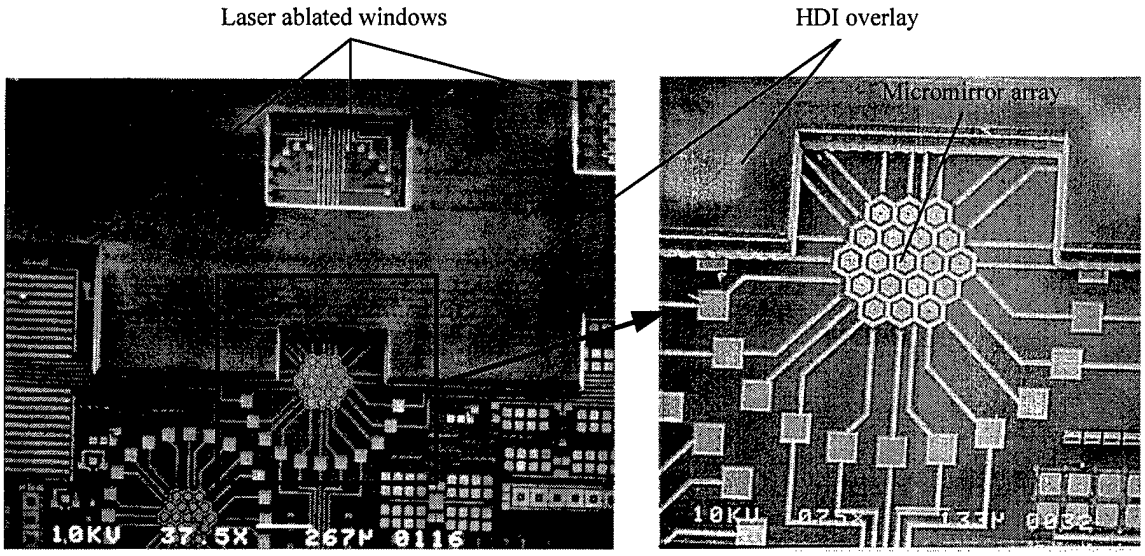
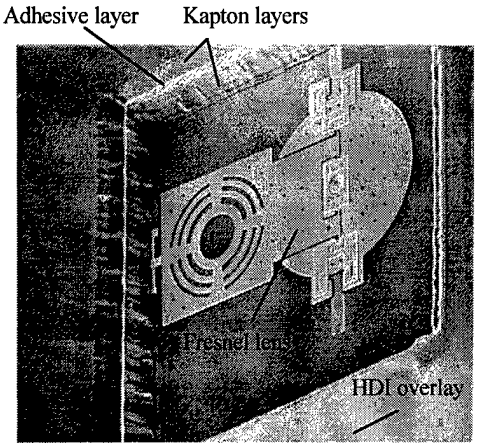


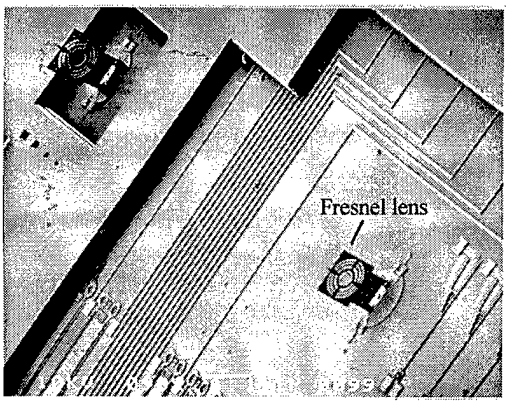
Figure 9-10. Ablation windows in HDI overlay to expose MEMS devices (MUMPs 15).

Figure 9-11 shows a close-up view of an HDI packaged Fresnel lens before and after assembly. The ablated window shown in Figure 9-11 (a) is approximately 400 μm long on each side. Each layer of Kapton dielectric is nominally 25 μm thick, and the

thickness of the adhesive layer between the Kapton sheets is 12 μm before pressure lamination. After lamination, the adhesive layer is compressed and planarizes the surface. Therefore, the depth of the laser ablated windows is approximately 55-60 μm. The Kapton and adhesive layers can be discerned in Figure 9-11 (a). The assembled Fresnel lenses shown in Figure 9-11 (b) are 250 μm tall and were manually assembled after packaging and release.



(a) Released Fresnel lens before assembly



(b) Assembled Fresnel lenses on COF/MEMS package

Figure 9-11. HDI/COF packaged surface micromachined Fresnel lens (a) before (MUMPs 9) and (b) after assembly (MUMPs 15). The devices were assembled manually with a microprobe.

9.4.2 HDI/COF Packaging of SUMMiT Die

Surface micromachined die fabricated in the Sandia Ultra-planar Multi-level MEMS Technology (SUMMiT) process were also packaged using the COF/MEMS process. The SUMMiT process is a "second generation" surface micromachining foundry offered by Sandia National Laboratories. This process has five layers (four releasable) of structural polysilicon [86]. The polysilicon layers are separated by sacrificial layers of oxide that are etched away in HF or HF/HCL. SUMMiT die require a much longer HF release etch than MUMPs due to the presence of more oxide layers and the slower etch rate of the oxide in the SUMMiT process.

The two SUMMiT die layouts used in this research were not designed specifically for packaging but do contain useful test structures and were used to provide a look at COF packaging of another surface micromachining process. One of the die contains arrays of thermal actuators and fabrication test cells designed by Comtois [27]. The other die has arrays of fabrication test cells and devices designed by engineers at Sandia.

The SUMMiT die were packaged at GE using the COF/MEMS process, and a large window was ablated over the whole die. The modules were then released using the procedure shown in Table 9-2 with the exception that the 2 minute HF etch was replaced with a 20 minute HF or 30 minute HF/HCL etch. The HF/HCL etch is preferred by Sandia engineers because it provides a higher selectivity for oxide over silicon and nitride. The devices were successfully released and functioned as expected. Figure 9-12 shows released devices on a SUMMiT die in a COF/MEMS package.

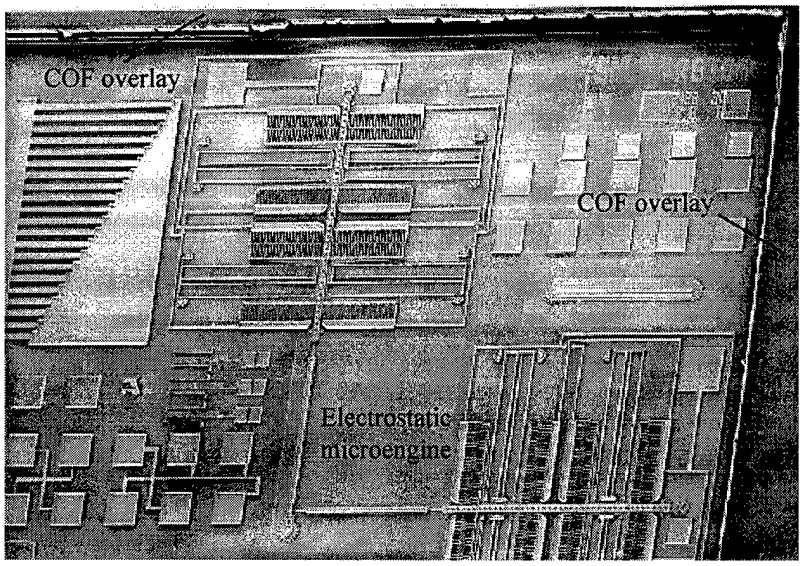


Figure 9-12. SUMMiT surface micromachined die in COF/MEMS package. The microengine and other devices on the die were designed and fabricated at Sandia National Laboratory [86].

The molded plastic COF substrate was largely unaffected after the long HF and HF/HCL etches but did show a slight loss of grains from the matrix on exposed surfaces. Figure 9-13 shows a module were the window ablated in the overlay was too large and inadvertently exposed part of the Plaskon substrate surrounding the die. The loss of grains was determined to be limited to the surface, and the COF/MEMS modules were still serviceable with no discernible impact to the overlay or any other embedded die in the module.

Most of the COF/SUMMiT modules etched for greater than 30 minutes showed a slight delamination of the overlay at the periphery of the package, but no delamination was observed in the windows ablated for MEMS access. Delamination at the perimeter

of the package can be easily prevented by using a fixture to shield the edges of module from the release etch.

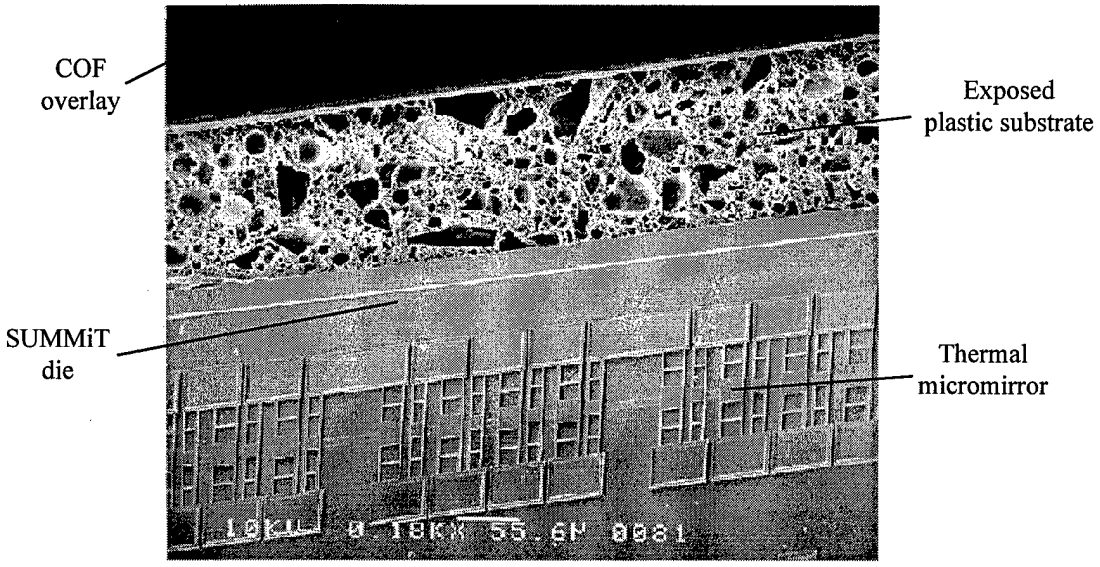


Figure 9-13. Exposed substrate COF/MEMS package after 20 min. HF release.

Following the COF/SUMMiT die packaging evaluation, ceramic HDI package samples were tested for compatibility with the long HF or HF/HCL release etch. The ceramic substrate and overlay was unaffected by either etch. Slight delamination of the overlay at the edges of the package were observed for samples etched for 30 minutes or longer. Thus, HDI packaging of SUMMiT die should be even more successful than COF packaging due to the increased HF resistance of the ceramic substrate.

9.4.3 Unablated Material in Corners of Large Openings

An intermittent problem seen on some of the HDI and COF/MEMS modules was the incomplete ablation of material in corners of large openings in the overlay. Figure 9-

14 shows an example of incompletely ablated material. This phenomena was not observed in any of the small windows ablated in the overlay. Consultation with GE revealed that different computer subroutines are used for ablating large and small openings in the overlay.

The first ablation program uses multiple lateral scan patterns across the surface of the module and is typically used to ablate windows in the overlay with a length or width greater than approximately 4000 μm [85]. This program must be used for windows which have a length or width of greater than 6300 μm (~ 0.25 inches). Smaller openings are handled by a program that uses one lateral scan distance but is more accurate in controlling the uniformity of ablation. No residual material was observed in any of the windows ablated with the single lateral scan program. Thus, it appears that the program used for ablating larger windows does not consistently produce a complete ablation in the corners of openings. GE is currently investigating the issue.

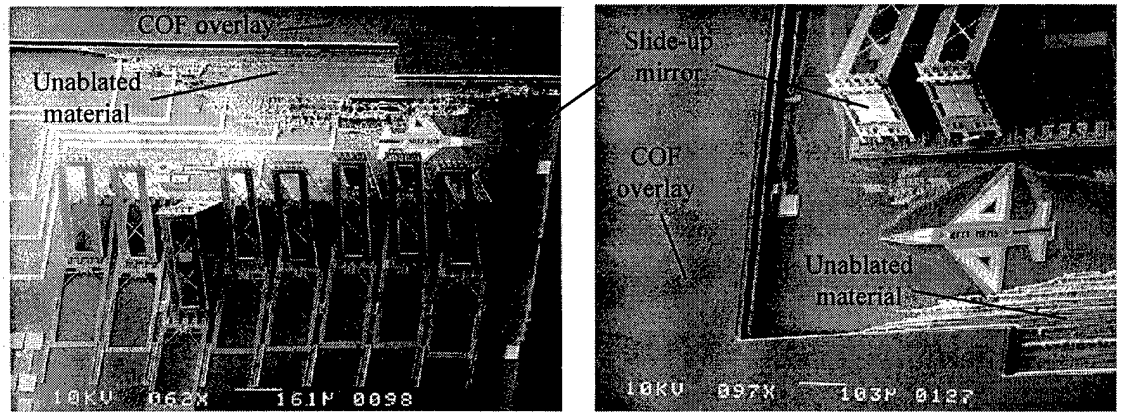


Figure 9-14. Incomplete ablation of the Kapton overlay on COF/MEMS modules. (MUMPs 19)

The main impact of the unablated material is that MEMS devices should not be placed within 500 μm of the edge of an opening in the overlay ablated with the multiple scan width ablation program. This design guideline is particularly applicable to devices in the corners of large openings since these areas are most susceptible to incomplete ablation. Overlay windows containing devices which must be close (< 500 μm) to the edge of the opening should only be ablated with the single lateral scan program.

9.5 Reducing Heat Induced Damage From Laser Ablation

The most serious problem discovered during post-packaging analysis of the surface micromachined test die was MEMS device warping or failure due to excessive heating from laser ablation. Devices most susceptible to overheating were long, thin structures with poor heat loss paths to the substrate such as the thermal actuators shown in Figure 9-15. Polysilicon resistors in areas which received high laser ablation power also showed resistance drops of 10-15% which is consistent with the change in resistance typically encountered during polysilicon resistor trimming [45].

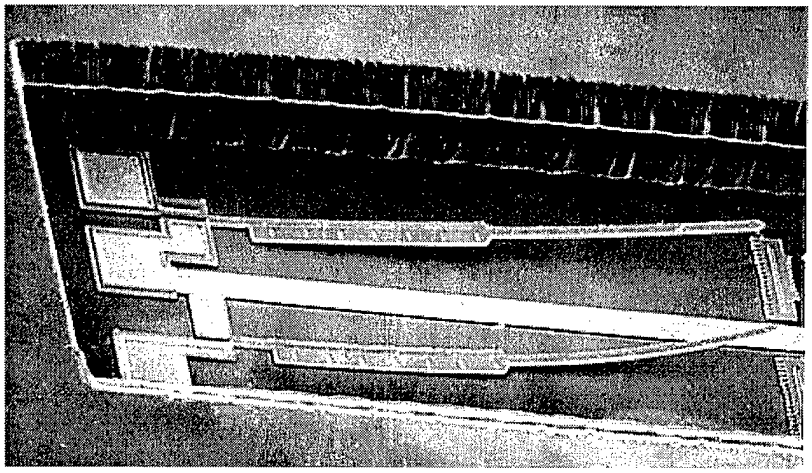


Figure 9-15. MUMPs 9 polysilicon lateral thermal actuators warped due to excessive laser ablation power.

The properties of the materials used in the MEMS fabrication are pertinent to efforts to minimize the potential for damage during laser ablation of the dielectric overlay. The ablation for HDI/COF is accomplished with a continuous argon ion laser at 350 nm. This wavelength is particularly conducive to damaging polysilicon devices in the MUMPs process because polysilicon absorbs virtually all of the incident laser energy at 350 nm [87]. Moreover, the top polysilicon layer (*Poly 2*) in MUMPs is particularly vulnerable to heat damage because it is uncovered and directly exposed to the laser beam during ablation. The underlying polysilicon layers can also receive a high fraction of the incident laser power when they are only covered by sacrificial layers of silicon dioxide since the optical transmittance of silicon dioxide is approximately 90 percent at 350 nm [88].

9.5.1 Analysis of Overlay Ablation

One method used to reduce the potential for heat damage was to find the minimum power and time required for ablating through the overlay. This was accomplished by conducting a detailed study and analysis of the HDI/COF laser ablation process. During the study, the ablation of the Kapton overlay was measured while varying the power, scan rate, and overlap between passes of the laser.

9.5.1.1 Description of Ablation Process

As mentioned previously, the laser ablation in the HDI/COF process is performed with a continuous argon laser operating at 350 nm. The half power beam width (HPBW) of the laser is nominally 9 μm. Figure 9-16 shows the raster scan pattern used during

ablation. For each pass, the laser is scanned across the surface of the module in a 6-12 mm swath. A shutter is used to control when the laser beam is allowed to impact the surface of the module.

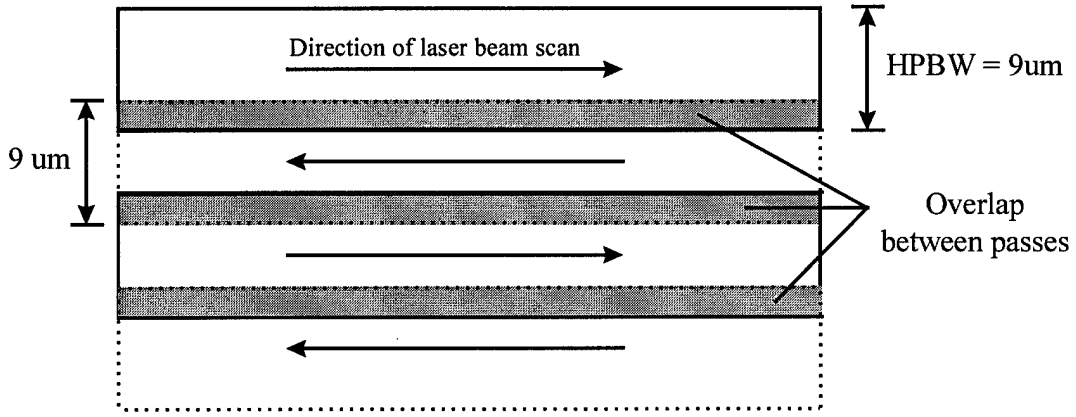


Figure 9-16. Ablation scan pattern on HDI or COF module.

At the end of a pass across, the laser is stepped orthogonally and reverses course to make another pass across the module. The amount of the orthogonal step determines the amount of overlap between passes. An overlap is used to improve the uniformity of the ablation. Less Kapton is ablated at the edges of the beam since the power is only half that at the center of the beam. After a single pass, the depth of Kapton ablation is not uniform. Using an overlap allows a second opportunity to ablate areas which did not get enough power on the previous pass. It is critical to select an overlap that is not too large or too small. Large overlaps can result in too much ablation while an insufficient overlap will result in unablated material remaining on the module. Figure 9-17 shows rows of overlay material left on a bulk micromachined test die for which the overlap between passes was too small to allow good uniformity of the ablation.

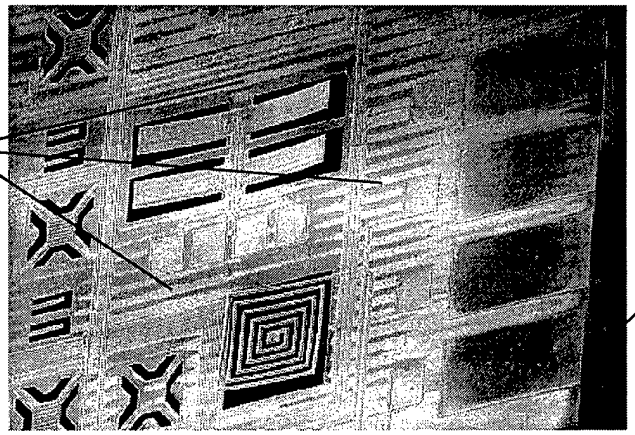


Figure 9-17. Rows of unablated material left behind on module with a small overlap between passes.

The scan rate is another critical factor in determining the characteristics of the ablation process. A slow scan rate allows more 'time on target' and will ablate more material. Faster scan rates are used to clean up residual Kapton or to minimize the danger of over-heating the target area.

9.5.1.2 Overlay Ablation Characterization

Several COF package samples were tested to measure the progress of the laser ablation. Only had a limited number of scan rates were available due to the setup of the laser in the GE laboratory. Hence, 150 Hz (1350 μm/sec) was chosen as the scan rate for ablating the bulk of the material, and 600 Hz (5400 μm/sec) was chosen for the polish ablation used to clean-up residual material after bulk ablation. As a result, the only two variable parameters were the overlap between passes and the power level.

The overlap between passes was the first quantity to be investigated. Test samples were ablated with varying overlaps to determine which overlap would provide

the greatest amount of uniformity. Analysis of the test samples revealed that a 3 μm spacing between the center of adjacent passes provided the most uniform ablation coverage, and this spacing was used in subsequent tests to determine the sensitivity of the ablation depth to variations in laser power.

The next step was to measure the depth of ablation as a function of the power level. COF package samples with a 60 μm thick overlay were used for this experiment. Windows were ablated in the test sample overlay while varying the laser power from 1-4 watts for bulk ablation and 1-5 watts for the ablation polish. Following each pass at a particular power level, the depth of the overlay ablation was measured with a Dektak profilometer. Figure 9-18 shows the results of these experiments.

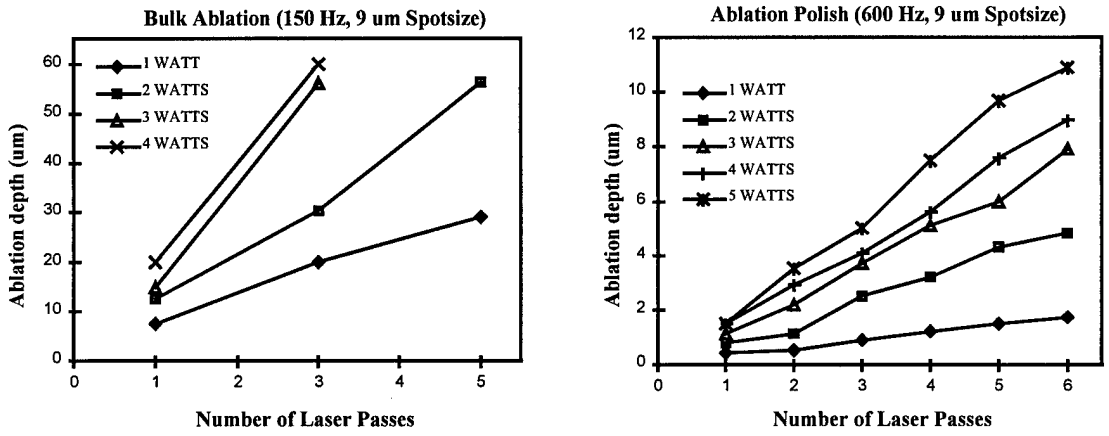


Figure 9-18. Ablation depth versus power level for COF overlay.

9.5.2 Development of Improved Overlay Ablation Procedure

After the laser ablation process had been characterized, an optimal ablation protocol was developed. The first HDI/MEMS module which showed MEMS device damage was ablated with a power of 1.6 W. However, the power was not reduced until the laser was within a few microns of the embedded die. Consequently, a new ablation

procedures which used lower laser power and alternative methods of removing the overlay was researched and developed.

9.5.2.1 Initial Attempts at Low Power Ablation

The first attempt at a lower power ablation was not successful. The laser power was set a 1 watt in hope that simply lowering the power would reduce the potential for MEMS device damage. Unfortunately, ablating at 1 watt (150 Hz) is slow and had the undesirable side effect of producing excessive residue after several passes. Moreover, the residue began to harden and became difficult to ablate and could not be removed with O_2 or CF_4/O_2 plasma etches.

The next procedure used was to combine a high power ablation to remove a large part of the overlay and then lower the power as the ablation proceeded closer to the die. A COF/MEMS module was ablated with a power of 2 watts until less than 10 μm of material were left. A 3 watt ablation polish (600 Hz) was then used to remove the remainder of the material. This procedure worked better than the previous attempt in that the majority of the overlay was removed, and the residue did not harden. However, the ablation polish was unable to completely remove the nearly 10 μm of material left after bulk ablation. A 4 hour plasma ash was used to remove the residual overlay; but while the rest of the overlay material was removed, the ash cycle was too long and caused delamination of the overlay and also began to etch exposed polysilicon on the MEMS die.

9.5.2.2 Development of Improved Ablation Protocol

The ablation protocol that produced a substantial reduction in ablation-induced damage combined elements from the first two attempts. The first attempt failed because

1 watt was unable to ablate enough material before the dielectric residue hardened. The second procedure failed because too much material was left behind for the ablation polish and plasma ash to remove. The success of the third procedure was due to the use of a three step ablation followed by a short plasma ash. A high pressure water scrub is also performed after each ablation step and the plasma ash. The water scrub helps to minimize the residue left after each step and thus minimizes the likelihood of the hardening. The steps of this procedure are shown in Table 9-3.

Table 9-3. Improved Ablation Protocol for COF/MEMS Overlay

Process Step	Power (W)	Scan Rate (Hz)	Passes Over Entire Module	Duration (Min.)
1. High Power Bulk Ablation	2	150	3	N/A
2. Low Power Bulk Ablation	1	150	5-7	N/A
3. Ablation Polish	3	600	6	N/A
4. Plasma Ash	300	N/A	N/A	60-90

Note: A high pressure (500 psi) water scrub is performed after each step

Laser characteristics: Continuous argon laser (350 nm)
9 μm HPBW
3 μm center-to-center spacing between adjacent laser scans

The goal of the first ablation step is to remove enough of the overlay to allow a low power setting to be used. This first step is accomplished with 3 passes at 2 watts. This step removes the first layer of Kapton and the inter-layer adhesives (~ 30 μm). The second ablation step consists of 5-7 passes at 1 watt. This step ablates the bottom Kapton layer (~25 μm) and leaves only the lower adhesive layer to be removed by the ablation polish. The ablation polish (6 passes, 3 watts, 600 Hz) cleans up most of the residual dielectric and adhesives.

After ablation, a plasma ash and high pressure water scrub are used. One of the positive lessons learned from the second attempt at low power ablation was that a short (< 90 minute) plasma ash (CF_4/O_2) was very effective in removing residue left behind after the ablation polish. The use of low pressure (~ 1 Torr) minimizes any etching of oxides or nitrides on the packaged die [85]. Consequently, a 90 minute plasma ash is performed after the ablation. The final step is a high pressure water scrub to remove any silica residue which may remain on the surface of the MEMS die. A high pressure scrub is also used after each ablation step. The high pressure scrub is obviously not a good idea for released microdevices as will be discussed later.

9.5.3 Results of Using Improved Overlay Ablation Protocol

The use of the improved ablation protocol was very successful. Figure 9-19 shows the progress of the ablation of a window containing a pair of scanning micromirrors in a COF/MEMS module. The result of the improved process is a very clean ablation with little residue in the ablated cavity.

The use of the improved ablation protocol in conjunction with plasma cleaning significantly reduced the occurrences of laser-induced damage on the test die. Figure 9-20 shows an array of lateral thermal actuators of the same design as the actuators in Figure 9-15 which were successfully packaged and released with no evidence of warping. These devices have the same resistance and deflection characteristics as similar devices on an unpackaged control die which indicates no permanent change in performance occurred as a result of packaging, ablation, and release.

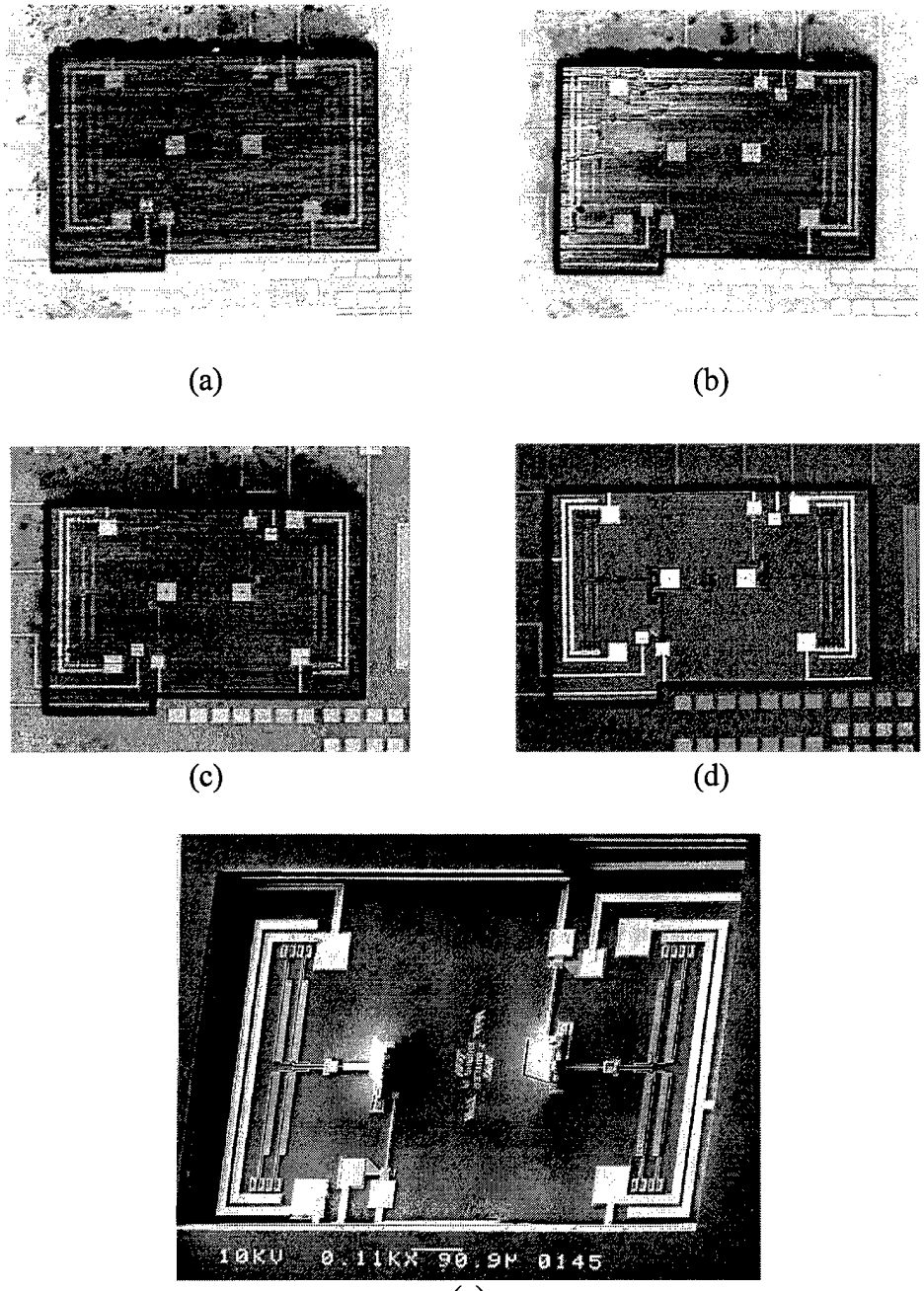


Figure 9-19. In progress view of improved ablation protocol (a) after 2 W ablation, (b) after 1 W ablation, (c) after 3 W ablation polish, and (d) after plasma ash. The released and assembled scanning micromirrors (MUMPs 19) are shown in (e). The width of the ablated window is 1200 μm.

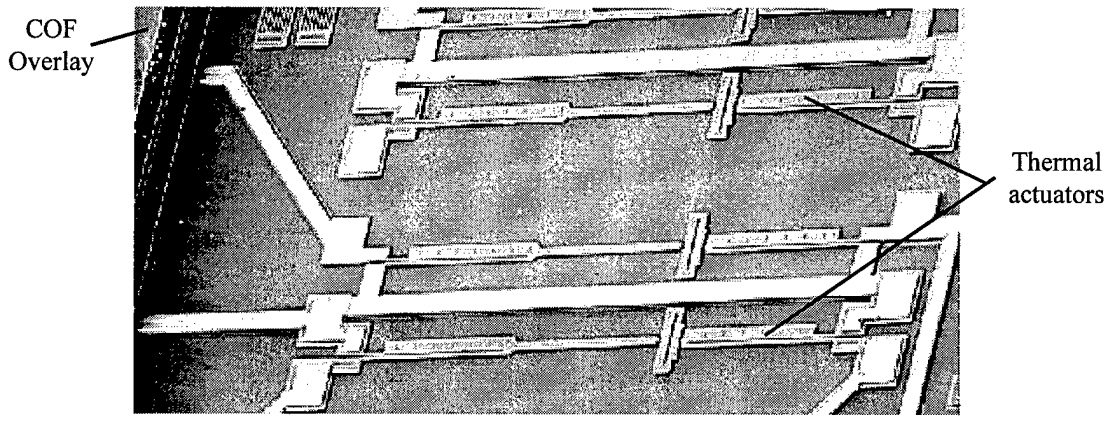


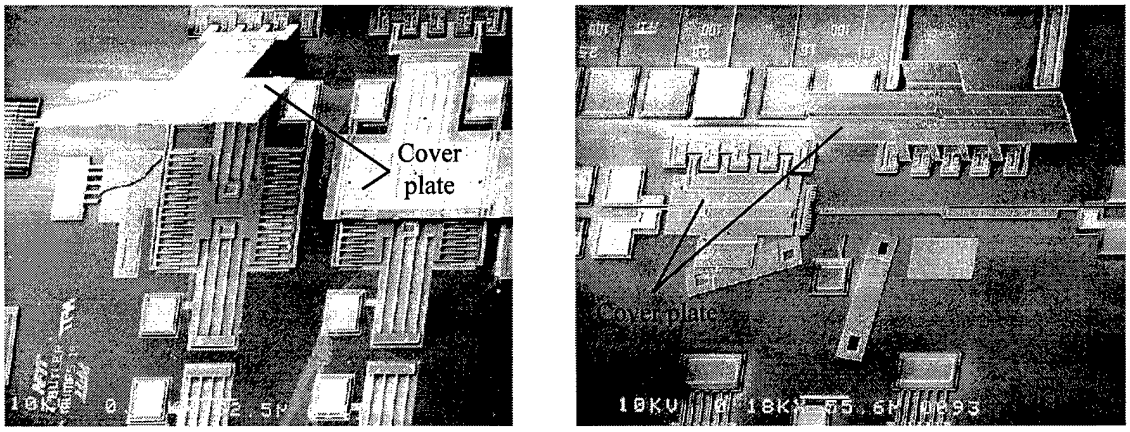
Figure 9-20. Array of MUMPs 15 polysilicon thermal actuators on COF package with no laser heating damage.

9.5.4 Use of Cover Plates

MEMS devices can also be designed to make them less susceptible to damage from laser radiation. For example, the vulnerability of MEMS devices to laser ablation heat can be reduced by using one or more of the fabrications layers as a screen or mask. For example, the MUMPs *Gold* and *Poly 2* layers can be used to protect *Poly 0* and *Poly 1* devices from the UV laser used in the HDI and COF/MEMS ablation process. *Gold* is a good protective layer because it is highly reflective at 350 nm, and *Poly 2* is also good protective layer because it absorbs all of the incident laser energy at 350 nm.

Several devices were fabricated and packaged to validate this idea. Figure 9-21 shows an electrostatic comb resonator and lateral thermal actuators which were packaged in a COF/MEMS module. These devices were designed to incorporate a hinged cover to protect them from laser ablation. The covers were constructed from *Poly 2* or a combination of *Poly 2* and *Gold*, and proved very effective at protecting the devices from the laser ablation process. No ablation-related damage was observed for any device with

a protective cover plate regardless of whether a *Poly 2* or *Poly 2/Gold* cover plate was used. This was true even for modules for which the overlay was ablated at 2 watts.



(a) (b)

Figure 9-21. (a) MUMPs 19 Electrostatic comb resonators and (b) lateral thermal actuators with cover plates successfully packaged and released in a COF/MEMS module.

A tradeoff associated with the use of cover plates is that the designer must either sacrifice one or more of the fabrication layers or add additional layers to construct the ablation shields. The addition of new layers is probably the more attractive option because there are several, well-established methods of applying and patterning thin films on devices. Moreover, adding protective layers to MEMS die to be packaged in the HDI/COF process has other benefits as will be discussed in the next section.

9.6 Minimizing Residue In Exposed Windows With Protective Oxide Layers

In addition to thermally-induced damage, another undesirable side effect of laser ablation is the accumulation of residue on the surface of the package. The residue from HDI or COF/MEMS process is a byproduct of the ablation process as well as the

adhesives used to bond the chip to the overlay. The residue is particularly troublesome for the MUMPs die because it adheres to the exposed gold and top layer of polysilicon (*Poly 2*). Plasma cleaning is effective at removing enough residue to satisfy microelectronic packaging requirements and most MEMS needs. However, even after plasma cleaning, some residue may be left on the MEMS devices that could potentially impair their mechanical or optical function.

In order to protect the MEMS devices from residue, a thin layer of silicon dioxide was applied over the test die before packaging. Silicon dioxide was chosen since it can be quickly removed with a dip in hydrofluoric acid and can be sputtered or spun-on at low temperatures which is necessary to protect the metallization on the MEMS die.

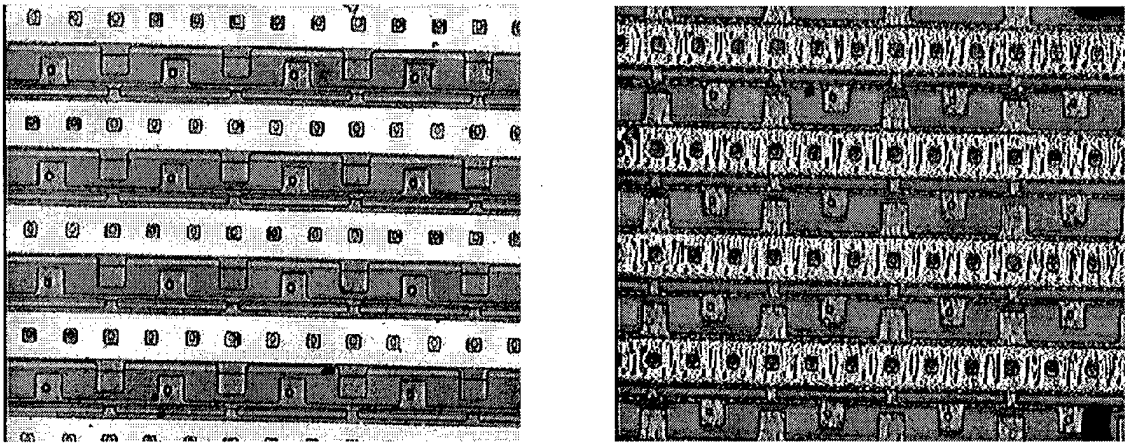
9.6.1 Sputtered Silicon Dioxide as a Protective Layer

Approximately 100-300 nm of silicon dioxide was sputtered on some of the MUMPs test die before COF packaging. After packaging, the die were released using the procedure in Table 9-2. The HF bath was extended by 10 seconds to account for the additional oxide. The reduction in residue on gold surfaces due to the protective oxide coating is apparent in the released variable blaze gratings shown in Figure 9-22. Both gratings were on the same die, but the grating in Figure 9-22 (b) was masked when the silicon dioxide layer was sputtered.

9.6.2 Spin On Glass as a Protective Layer

Spin on glass (SOG) can be used as an alternative to sputtering for low temperature (< 300 °C) applications. SOG has the desirable traits of being inexpensive,

easy to apply, and providing surface planarization. It was developed in the late 1980's and is commonly used as an interlevel dielectric for microelectronic processes [89]. SOG liquids consist of Si-O network polymers dissolved in organic solvents [90,91] and are applied by spin coating the liquid material onto a wafer or die. After coating, the sample is cured to drive off the solvents and allow the Si-O network to crosslink and form a solid film. The cure is normally a series of short bake cycles followed by a long cure cycle in a furnace. After curing, a silica-like glass film is formed.



(a) (b)

Figure 9-22. Comparison of residue deposited on released variable blaze grating (a) with and (b) without silicon dioxide protective layer in HDI package.

Most SOG compositions are designed to be cured at or around 400-425 °C. This allows them to be used safely with the aluminum metallizations commonly used in microelectronics. However, 400 °C is still too high for application in the packaging of MUMPs die in the HDI or COF process because of the gold-silicon eutectic formed in the

MUMPs process. An analysis of the temperature sensitivity of MUMPs die by Burns showed that the gold-silicon eutectic bond could fail at temperatures as low as 250 °C [92]. As a result, a 200 °C cure procedure for Allied Signals T-311 Accuglass SOG which allows the SOG to be used as a protective layer for MEMS die was developed and tested.

Allied Signals T-311 Accuglass is a commercially available SOG designed to be cured at 425 °C [93]. Table 9-4 shows the recommended cure procedure. In consultation with an Allied Signal engineer, it was discovered that high temperature part of the cure process improves the dielectric quality of the oxide by driving off solvents and maximizing the polymerization of the film [94]. However, these qualities are not critical to use as a protective layer, and most of solvent evaporation and polymerization can be accomplished at lower temperatures. It was then surmised that an extended bake at lower temperatures would probably provide a good enough oxide for use as protective layer.

Allied Signal provided a complimentary supply of SOG to test low temperature curing. Silicon wafers were coated with the SOG, and the samples were baked according to the specified procedure with the exceptions that the third bake was performed at 200 °C and the cure cycle was varied in temperature and duration. After spin-on and curing, all of the samples were examined with a Leica film thickness monitor to measure the thickness and quality of the oxide. Table 9-5 compares the thickness and index of refraction for the various samples.

The index of refraction and etch rate in hydrofluoric acid are considered figures of merit for evaluating the quality of silicon oxides. Good quality oxides have an index of

refraction close to the crystalline SiO_2 value of 1.46 [6]. Oxides with an index of refraction below 1.46 (1.39-1.46) are considered porous, but acceptable as a dielectric. In addition, higher quality oxides usually etch more slowly when exposed to hydrofluoric acid [6].

Table 9-4. Recommended Cure Procedure for Accuglass T-311 [93].

Process Step	Comments
1. Spin Coat Target	10 sec. @ 3000 RPM
2. Bake	60 sec. @ 80 °C
3. Bake	60 sec. @ 150 °C
4. Bake	60 sec. @ 250 °C
5. Cure	1 hour @ 425 °C

Table 9-5. Comparison of Film Thickness and Index of Refraction of SOG Samples.

Oxide Type	Cure Temp (°C)	Cure Time (Hrs.)	Film Thick (nm)	Index of Refraction	Relative HF etch rate
SOG	425	1.0	600	1.43	Fast
SOG	350	1.5	600	1.41	Fast
SOG	220	24.0	600	1.42	Fast
SOG	220	4.0	600	1.42	Fast
Sputtered	N/A	N/A	100	1.42	Fast
Thermal (wet)	1000	1.0	400	1.46	Slow

All of the SOG samples appear to be porous but still have a reasonable index of refraction. The SOG samples were also etched much more quickly than the thermally grown oxide; but the etch rate was virtually the same as that of the sputtered oxide.

These results indicate that the low temperature cure produces a SOG film which is useable as a sacrificial or protective layer but is not a premium quality oxide.

The success in using the low temperature cure to produce oxide films prompted the use SOG as a protective layer in COF/MEMS packaging experiments. SOG was spun on silicon wafers and MUMPs packaging test die and baked at 220 °C for 24 hours. Following the bake, polyimide was applied to the wafers and hard baked. The polyimide was then ashed in an oxygen plasma to manufacture a residue similar to that produced in the COF laser ablation process. Figure 9-23 shows the residue on a wafer after the plasma ash. Next, the wafers and die were etched in hydrofluoric acid to remove the oxide and residue. The residue removed cleanly and the wafer and test die surfaces showed no trace of polyimide. Furthermore, the gold on the MEMS test die was unaffected by any of the processing.

The SOG procedure was developed too late in the research effort for incorporation in a full COF/MEMS package. However, the results of the residue testing and index of refraction analysis indicate that the SOG film is of similar quality to the sputtered oxide which was successfully employed in several COF/MEMS modules. Hence, SOG should be a suitable alternative as a protective layer in HDI or COF packaging.

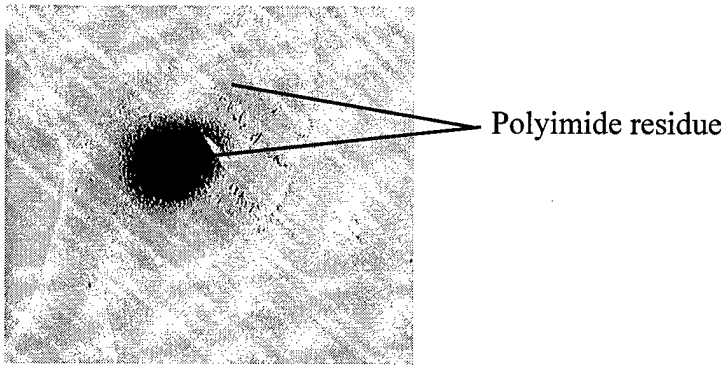


Figure 9-23. Plasma ashed polyimide residue deposited on silicon wafer.

9.6.3 Thermal Protection of Silicon Dioxide Layers

One of the unexpected benefits of the protective oxide coating was that it reduced the vulnerability of the MEMS devices to laser ablation. MEMS devices in areas with the oxide coating showed noticeably less evidence of laser heating damage even when the ablation was done at 1.6 W. The reduction in damage is most likely due to the thermal isolation provided by the oxide layer.

The physical phenomena which leads to the ablation of polyimide can be either photothermal, photochemical, or a combination of both [95]. For photochemical ablation, the material removal is a result of direct bond breaking from electron excitation. There should not be any noticeable temperature change for ablating the material, and the ablated features should be clean with no damage beyond the target area [95]. Photochemical ablation is usually associated with using high power and short pulse widths (< 1 ns) [96].

Conversely, in a photothermal ablation process, the absorbed photon energy leads to a significant increase in temperature prior to material removal. The temperature increase is due to the transfer of energy from the excited electron states into mechanical

vibration of the lattice [95]. The rapid rise in temperature is the mechanism for ablation. The thermal breakdown of the material leads to fragmentation and ejection of the surface layer in a process similar to a chemical explosion or detonation [97]. Photothermal ablation is usually associated with continuous or long pulse width (> 1 μs) ablation [96].

The ablation in the COF/MEMS process is primarily a photothermal phenomena. The "pulse width" of the laser used in the COF/MEMS process can be defined as the amount of time that the HPBW of the beam is covering a point on the surface [98]. By this definition, the pulse width of the bulk ablation and ablation polish steps are 6.67 and 1.67 ms respectively, and the ultraviolet laser ablation of polyimides using pulse widths greater than a millisecond has been shown to be primarily a photothermal reaction [95-98].

The temperature threshold for the photothermal ablation of Kapton at 350 nm has been reported as a minimum of 850 °C [95,97]. The optimum photothermal ablation of Kapton has also been theorized to occur at temperatures from 1100-1500 °C [96]. As a result, any material in close proximity to the Kapton ablation, such as an embedded MEMS die, may be subjected to a heat source of least 850 °C and potentially as high as 1500 °C. Temperatures of this magnitude can easily cause failure in polysilicon structures.

The protective oxide layer was initially used for residue protection, but it also provides good thermal isolation. The thermal conductivity of silicon dioxide is 1.0-1.4 W $K^{-1}m^{-1}$ [99] which is much lower than that of silicon (160 $WK^{-1}m^{-1}$) or polysilicon (30 $WK^{-1}m^{-1}$). The presence of the sputtered or SOG oxide protective layer is particularly

important for MUMPs *Poly 2* structures because these devices are exposed on the surface and would otherwise have no isolation from the thermal effects of ablation. Figure 9-24 shows a large slide-up F-16 packaged in a COF/MEMS module. The die was covered with 300 nm of sputtered oxide prior to packaging. Previous attempts at assembling this device failed because the *Poly 2* used in the frame and support structures was either warped by laser ablation or weakened by the plasma etch.

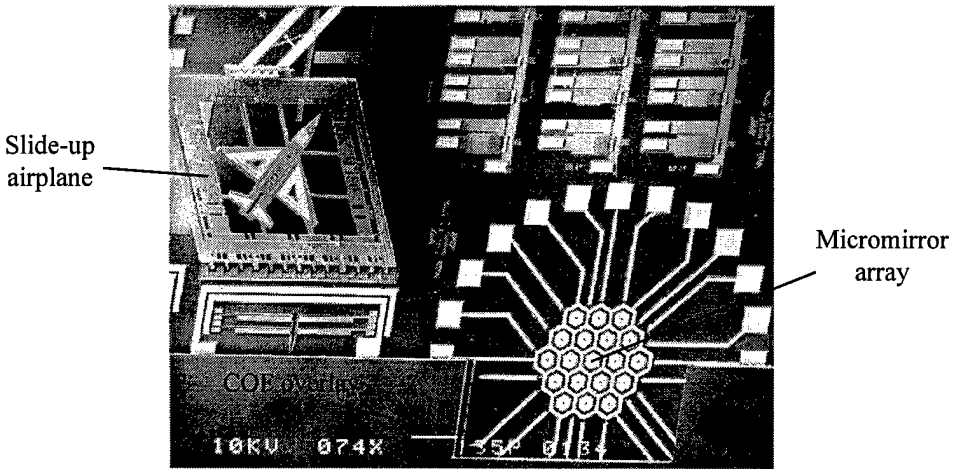


Figure 9-24. Assembled MUMPs 19 slide-up structure on COF/MEMS package. The slide-up frame is 650 μm long and the airplane has a length of 500 μm.

9.7 COF Packaging of Bulk Micromachined Test Die

The bulk micromachined test die was also used in COF packaging experiments. Both pre and post release packaging of the bulk micromachined test die was investigated. The devices and test structures on the bulk micromachined test chip are structurally more robust than their surface micromachined counterparts. Consequently, devices on some of

the CMOS MEMS die were released before COF packaging to test if released bulk micromachined devices could withstand the packaging process.

9.7.1 Packaging of Pre Released Bulk Micromachined Test Die

The pre released test die were etched using the procedure for bulk micromachined die shown in Table 9-6. The die were then sent to GE for packaging. After going through the standard COF packaging process, a large opening was ablated over the die to allow access to the micromachined devices.

Table 9-6. Wet Etch Release Procedure for Bulk Micromachined Test Die.

1. Dip in 10 % hydrofluoric acid for 10 seconds
2. Soak in deionized water for 5 minutes
3. Etch in EDP at 95 °C for 45 - 60 minutes
4. Soak in deionized water for 5 minutes
5. Soak in 2-propanol for 5 minutes
6. Dry on hot plate at 50 °C

Many of the released structures on the test die survived the packaging process. The most common failures were physical destruction of devices with a width of less than 25 μm and accumulation of adhesives in the etched cavities. Figure 9-25 shows pre-released cantilevers which survived the packaging process. Nearly all of the MEMS structures on one pre-released die actually survived the COF packaging process; but most of the devices were later destroyed when the module was inadvertently subjected to a high pressure water scrub.

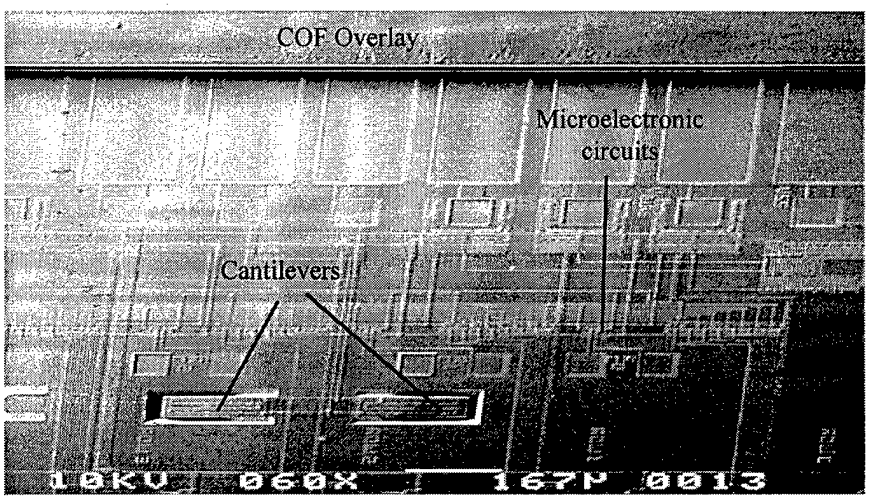


Figure 9-25. Pre-released cantilevers on COF packaged bulk micromachined test die.

9.7.2 Post Packaging Release of Bulk Micromachined Test Die

The majority of the bulk micromachined test die were packaged before release in order to maximize the likelihood of the MEMS structures surviving the HDI/COF process. However, the wet etch procedure of Table 9-6 could not be used for releasing the bulk micromachined test die after COF packaging. Similar to the MCM-D package in Chapter 8, the COF (and HDI [15]) package materials were not able to withstand the wet etch procedure for the bulk micromachining test die. As a result, xenon difluoride (XeF_2) was investigated as an alternative etchant.

COF and HDI package samples were sent to UCLA for compatibility testing in their XeF_2 etch chamber [9] (see Chapter 8). Each sample package sample is 12 mm x 12 mm, and a 5 mm stripe was laser ablated on each sample to expose the sidewalls of the layers. Figure 9-26 shows a cross-section of the package samples and their physical composition. The samples were etched in XeF_2 along with two of the bulk

micromachined test die. The etching continued until an etch depth of approximately 70 μm had been achieved on the test die.

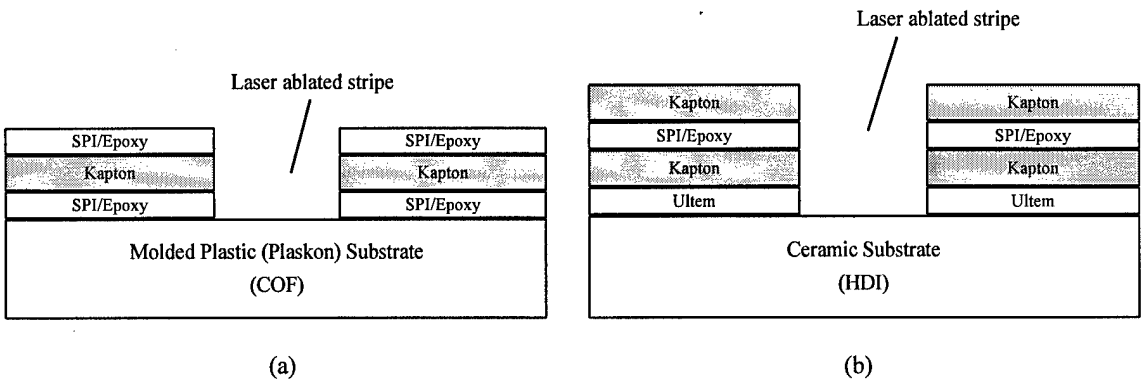


Figure 9-26. Cross-section of (a) COF and (b) HDI package samples.

The package samples subjected to the XeF_2 release procedure appeared unaffected by exposure to the gas. Inspection of the package samples after etching revealed no impact to either the COF or HDI substrates or overlay after the prolonged exposure to XeF_2.

A populated COF/MEMS package was etched in the XeF_2 chamber after the compatibility of the test die and the package samples was established. The module was etched to an approximate depth of 50 μm. Figure 9-27 shows some of the released microstructures on the COF/MEMS packaged test die. Initially, the XeF_2 etching of the module shown in Figure 9-27 proceeded more slowly than expected because rows of residual overlay were left on the die from ablation. Some of these rows can be discerned in the close-up of the spiral in Figure 9-27. Fortunately, the XeF_2 gas was able to penetrate through the gaps in the residue and etch the bulk silicon. The etch rate increased to expected levels after the residue was removed with the top layer of silicon.

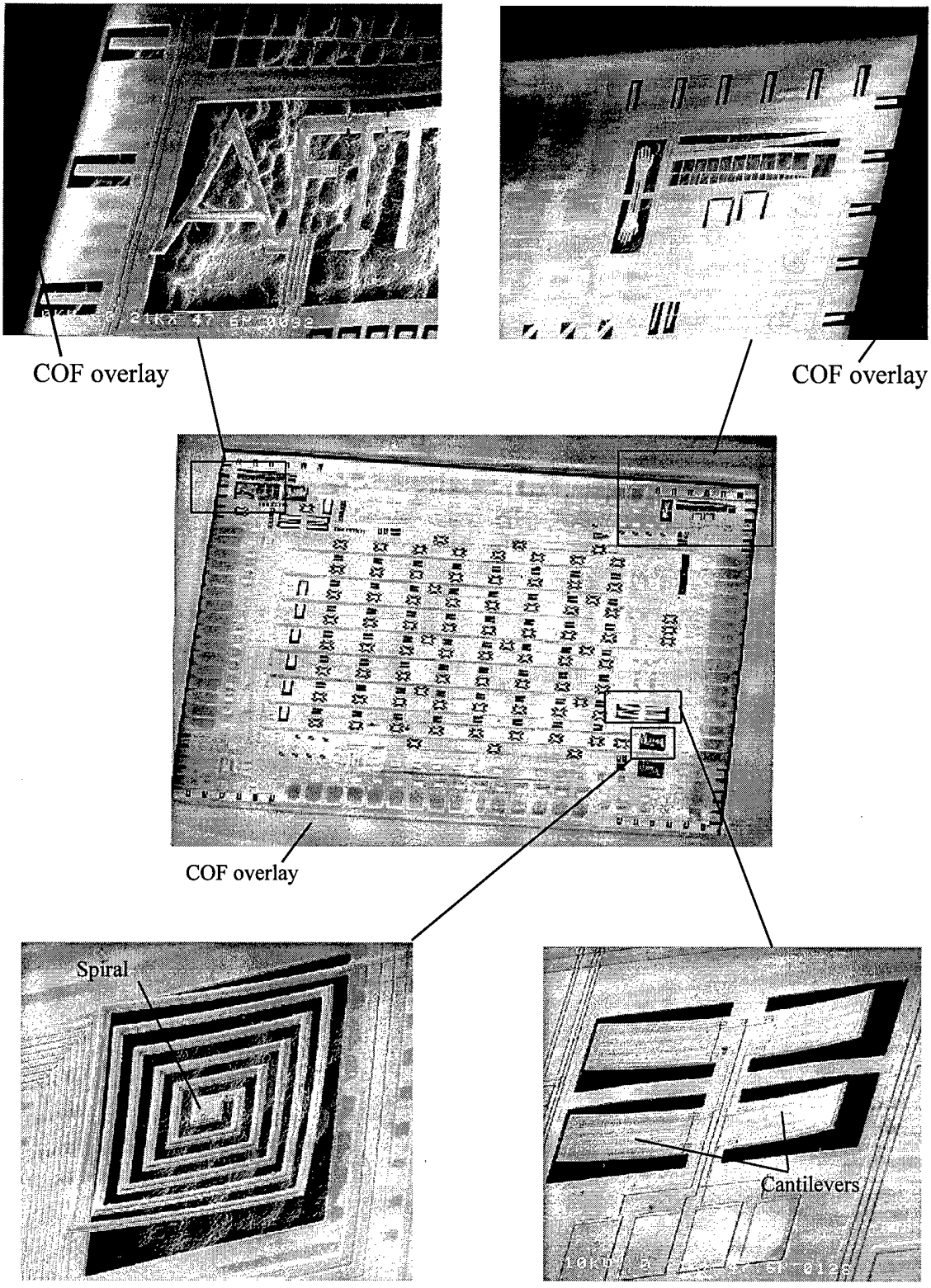


Figure 9-27. Released bulk micromachined test die in COF/MEMS module.

The devices shown in Figure 9-27 demonstrate that a wide variety of bulk micromachined devices can be COF packaged and released using XeF_2. The suspended "AFIT" logo is constructed from silicon dioxide. Each letter is 200 μm tall and 25 μm wide. The cantilevers are composed of metal and polysilicon encased in oxide. Each cantilever is 250 μm long and 70 μm wide. Fragile structures such as the spiral shown in Figure 9-27 were also successfully packaged. The width of the spiral arm is only 12 μm wide and is formed from polysilicon and metal encased in oxide. Perhaps the best endorsement of the packaging success was that the bulk micromachined devices were released without impacting the functionality of the CMOS electronics on the test die.

9.8 Summary

The General Electric (GE) high density interconnect (HDI) and Chip-on-Flex (COF) multichip packaging technologies have been adapted for packaging MEMS. Silicon surface and bulk micromachining test die were successfully packaged with a CMOS electronics die in the COF process. Methodologies to reduce the potential for MEMS device damage due to laser ablation and accumulation of residue were also implemented. The potential for damage in HDI processing from laser ablation is a concern but can be mitigated through lower ablation power, protective coatings, and prudent use of plasma etching. In addition, protective layers and plasma cleaning also remedy the formation of residue on the device package.

Pre and post-packaging release of MEMS die was investigated. The decision to release MEMS devices before, after, or incrementally during the packaging process is

strongly dependent on the physical and material properties of the MEMS devices, other co-packaged components, and the package itself. Moreover, the MEMS release procedures and the specifics of the packaging process such as cleaning procedures must be addressed and understood by the MEMS designer and the system integrator to ensure the highest possibility of success.

Furthermore, the importance of test structures dedicated to the effects of packaging and assembly was affirmed. Failure modes of MEMS devices can differ significantly from macroscale devices and microelectronics.

The outcome of the this research has several implications for MEMS and microsystems. First, integrating MEMS and microelectronics in advanced MCMs can be a flexible alternative to monolithic fabrication. This is particularly important for spaceborne applications which have unique qualification requirements that may be difficult to achieve with a monolithic process. In addition, advanced MCM packaging such as HDI can improve the performance and capabilities of MEMS when the packaging environment is factored into the design of the overall microsystem. For example, the COF/MEMS technology can enhance the capabilities of a MEMS fabrication process by providing integration with electronics, multilevel interconnects, or chip scale packaging.

Chapter 10. Conclusions

"*. . . Of making many books there is no end, and much study wearies the body. Now all has been heard; Let us hear the conclusion of the whole matter:* . . ." - Ecclesiastes 12:12-13.

10.1 Summary

This research investigated the design, modeling, integration, and packaging of microelectromechanical systems (MEMS). Several advances to the MEMS and microelectronic state of the art were achieved during the course of the dissertation research. These advances were accomplished through the design and characterization of novel MEMS devices and packaging which were compatible with CMOS microelectronics. Moreover, empirical and theoretical models of polysilicon thermal actuators were developed to understand and model the behavior of thermal actuators. The most extensive investigation of the MUMPs polysilicon resistivity was also performed as part of this research effort.

The development of robust devices and models permitted the functional and physical integration of MEMS with CMOS controllers. The functional integration of MEMS with CMOS was demonstrated through the design of automated positioning and assembly systems. A new power averaging scheme was devised to take advantage of the power averaging characteristics of polysilicon thermal actuators. The development of this scheme creates a whole new arena of control methodologies for MEMS. The packaging of MEMS using foundry multichip modules was also demonstrated and shown to be feasible approach to the physical integration of MEMS with other microelectronic

technologies. Table 10-1 summarizes the most significant contributions and developments from this dissertation.

Table 10-1. Significant Contributions and Developments.

Contribution	Chapter	Application
Automated assembly systems	3	Simplifies setup and assembly of hinged and flip-up MEMS devices
Low voltage micromirrors	3	Beam steering, aberration correction
CMOS compatible thermal actuator arrays	3	Enables simple integration of thermally actuated devices with digital CMOS
Electrothermal SPICE models for polysilicon thermal actuators	4	Co-simulation of thermally actuated devices and microelectronics
Polysilicon thermal actuator theory of operation	4,5	Provides behavioral insights on thermal actuators; improves future designs, models
TSUPREM model of MUMPs fabrication	5	Provides insight into resistivity of MUMPs polysilicon layers
Estimate of MUMPs *Poly 1* TCR	5	Critical parameter for thermal modeling of MEMS devices constructed from *Poly 1*
Pulse modulation positioning of thermal actuators	6	Enables design and development of simplified control systems for MEMS
XeF_2 etching of MCM packaged MEMS	8,9	Method for post packaging release of silicon bulk micromachined MEMS
Improved ablation procedure for HDI/COF	9	Reduces potential for MEMS device damage in HDI or COF/MEMS packaging
Protective Coatings for MEMS	9	Reduces potential for MEMS device damage and residue accumulation during packaging and handling
Low temperature cure for spin-on glass	9	Simple and inexpensive method of applying a protective layer for MEMS packaging

The significance of this research effort is highlighted by the amount of interest from other researchers and organizations. The benefits of this research are already being harvested by fellow researchers in government, industry, and academia. The work on the automated assembly of MEMS is being pursued by UCLA and the U. S. Army. Two of the leading MEMS CAD tool developers have often consulted with the author and used aspects of the electrothermal SPICE model for developing their commercial tools. In fact, the empirically derived value for the thermal coefficient of resistivity (1.25×10^{-3} K^{-1}) for the MUMPs *Poly 1* layer is currently being used in one of the leading MEMS CAD tools.

10.2 Resolution of Research Objectives

The primary objectives of this dissertation were to (a) determine the suitability of MCM foundries for MEMS packaging, (b) develop models for MEMS devices and fabrication processes, and (c) explore the functional integration of MEMS and CMOS microelectronics.

10.2.1 Suitability of MCM Foundries for MEMS Packaging

The results of the MEMS/MCM packaging experiments described in Chapters 8 and 9 demonstrate that MCM foundries can be effectively adapted for packaging a wide variety of MEMS. A key to the success of MCM packaging of MEMS is an inter-disciplinary evaluation of the microsystem including (but not limited to) the MEMS, microelectronic, and packaging components.

One aspect of this MEMS packaging analysis must be a determination of whether the MEMS die should be released before, during, or after packaging. For pre-release, an understanding of the handling and packaging procedures are vital in order to protect the fragile devices. For post packaging release, the chemical compatibility of the module components with the MEMS release procedure(s) must be established because there are combinations of MEMS and MCMs that are not ideal. For example, a MCM using exposed silicon dioxide in the substrate may not by a good choice for post packaging release of a MUMPs die which requires an oxide removing etch in hydrofluoric acid.

In some cases, it may even be advantageous to alter the release of the MEMS devices to suit the packaging process. For example, release and re-encapsulation was used with the bulk micromachined test die in the MCM-D module (see chapter 8) to facilitate the release of multiple MEMS die. Likewise, a thorough examination of the package and components may reveal non-intuitive procedures which can be used for a specific combination of MEMS and package.

The high density interconnect (HDI) and chip-on-flex (COF) packages were shown to be particularly well-suited for MEMS packaging. The Kapton overlay can protect embedded die from many of the MEMS release procedures, and the high performance interconnects provide electrical performance on par with monolithic fabrication. An improved ablation protocol was developed to minimize the potential for device damage due to laser ablation. In addition, protective oxide coatings were found to reduce the impact of heat damage from ablation as well as mitigate the accumulation of residue on MEMS devices such as micromirrors.

10.2.2 Modeling of MEMS Devices and Fabrication

The modeling of MEMS devices and fabrication was also successfully completed. Electrothermal SPICE models were developed for modeling and analyzing the response of polysilicon thermal actuators. Empirical and parametric models were implemented to simulate the electrical load and deflection characteristics of a polysilicon lateral thermal actuator and a thermal piston micromirror. The parametric model was able to accurately predict the electrothermal response of thermally actuated devices and has excellent agreement with measured data and theory.

The creation of the electrothermal SPICE models is a significant contribution to the development of integrated microsystems. The ability to simulate both the MEMS device and the control electronics in the same analysis package greatly improves the design process. Furthermore, the parametric model allows the designer to gain some insight into the expected performance of the microsystem prior to fabrication.

An in depth analysis of MUMPs resistivity characteristics was also conducted. The MUMPs process is one of the most widely used MEMS foundry fabrication processes and is the primary source of MEMS fabrication for research at AFIT. The first published estimate of the temperature coefficient of resistivity (TCR) for the MUMPs *Poly 1* layer was generated as 1.25×10^{-3} K^{-1}. This value is critical to thermal modeling of polysilicon thermal actuators fabricated in MUMPs. Furthermore, the sheet resistance and resistivity of all the MUMPs polysilicon layers was shown to be a function of linewidth due to the presence or absence of lateral diffusion. Finally, a theory for the

resistance trimming effects of polysilicon thermal actuators was also proposed and validated.

10.2.3 Development of Microsystems Using MCMs

The final objective for this research was to functionally and physically integrate MEMS with CMOS in a multichip module. This was demonstrated by first developing CMOS controllers for MEMS and then physically integrating the MEMS and CMOS die in an MCM. Computer-based control systems using CMOS drivers and pulse width modulation were developed to control a variety of devices such as micromirrors and automated assembly systems. A key to the success of the CMOS controllers was the use of pulsed control signals to drive thermal actuators. The use of pulsed versus DC inputs was shown to allow flexible positioning of thermal actuators arrays.

The physical and functional integration of MEMS and CMOS in a MCM was achieved by designing a special 'stacked' module in which the CMOS die was bonded to the surface of the MEMS die. The 'stacked' die MCM was employed to automate the operation of a variety of electrostatic and thermally operated MEMS devices.

Finally, all of the MCM packages, MEMS die, and CMOS microelectronics die used in this research were foundry fabricated. In addition, a concerted effort was made to use and/or develop simple post-processing procedures for release and handling of the microsystems. The increasing availability of affordable, high performance foundry processes combined with the research presented in this dissertation should allow a wide range of developers to implement robust and cost-effective microsystems.

10.3 Areas for Further Research

MEMS is a rapidly growing field, and many of the contributions described in this dissertation will be stepping stones for other researchers to build upon or assimilate into new technologies. This section proposes recommendations for how the answers generated by this research effort should be incorporated into future work.

10.3.1 MEMS Device Design and Modeling

The design of new devices is an area of great potential for new research as MEMS provides the ability to fabricate structures that operate on principals not realizable at the macro level. However, there other areas in MEMS device research which need an increased level of attention in order for MEMS to make the transition from a promising technology to a commercially viable industry. First, automated or self assembly of MEMS needs to be aggressively pursued. High yield and volume production of MEMS will require the ability to rapidly and automatically assemble MEMS structures. The automated assembly systems developed in this dissertation are only a start, and more robust and reliable means of assembling MEMS are needed.

Furthermore, MEMS metrology research must also be addressed. Surprisingly little work has been done validating the physical and mechanical properties of commonly used MEMS materials at the microfabrication level. The research in Chapters 4 and 5 clearly show that material properties on the micron level can vary from macroscale; and undoubtedly, the behavior of nanoscale device will be different from even devices at the micron level. The material properties of the MUMPs *Poly 1* layer were examined, but

more characterization work still remains to be accomplished for the majority of MEMS fabrication processes currently in use.

Another area for new research is the development of coupled electro-thermal-mechanical models and simulation tools for MEMS. The SPICE models address the electro-thermal aspect of this problem. However work remains in the addition of mechanical simulation. One solution is to link SPICE to a mechanical finite element analysis tool such as ANSYS. This approach is currently being pursued by industry, but there will be many problems to overcome before MEMS modeling and simulation tools mature to the level of the products currently available for the design of microelectronics.

10.3.2 Microsystem Development

The integration of MEMS and microelectronics is another area for future research. The CMOS controllers used in this research were fabricated as application specific integrated circuits (ASICs). However, the design of many MEMS controllers can be more cost-effectively implemented using field programmable gate arrays (FPGAs). FPGA technology is well-established and is an integral part of the microelectronics industry. FPGA controllers would allow the development of general purpose microsystem modules in which the FPGA could be electronically reprogrammed to accommodate a variety of MEMS devices. FPGAs are particularly suited for implementation of pulse width modulation systems because only the FPGA and the target MEMS die may be needed. Finally, charge modulation control of electrostatic devices is also an area for continued investigation. The development of control schemes which

control the charge applied to electrostatic MEMS would allow the creation of simplified control systems for another class of MEMS devices.

10.3.3 MCM Packaging of MEMS

The MEMS/MCM packaging experiments were very successful, but there are still areas which need to be explored. First, packaging of LIGA devices was not accomplished during the course of this dissertation. MCM-D packaging of LIGA should not be too difficult especially since LIGA devices are robust and could be re-encapsulated for packaging. HDI and COF packaging of LIGA MEMS may also be possible. HDI and COF package samples will survive the LIGA release etch if acetone is not used. The packaging of LIGA die was not successful because the tall structures on the available test die did not possess enough surface area to bond to the overlay. However, this can be overcome by designing a test die suitable for HDI/COF packaging.

Improved solutions to the laser ablation and residue problems in the HDI and COF/MEMS process are also fertile grounds for new research. One area with great potential is the use of a high power, short pulse width laser for ablating the overlay. The heat damage problems described in this research were the result of using a slowly scanned CW laser. New, high power pulsed lasers have been developed which are capable of ablating materials so rapidly that there is no temperature increase in the sample. This type of laser would also greatly reduce residue formation.

Finally, the use of protective layers for MEMS/MCM packaging is proposed; but the surface has only been scratched on this topic (pun intended). It should be possible to

develop protective coatings which provide better thermal isolation than silicon dioxide while also protecting the packaged MEMS die from residue or even incident laser energy. In addition, protective layers may also be useful for increasing the survivability of MEMS die during the automated handling used for high-volume packaging processes.

Appendix A. HSPICE Electrothermal Subcircuit Generator for Microbridges

This appendix contains the source listing of the electrothermal HSPICE subcircuit generator for microbridges. The program is written in C. An example input and output file are also listed. The model generator program accepts the input file and makes the necessary computations and formatting to produce an electrothermal SPICE subcircuit compatible with HSPICE.

The author's electrothermal subcircuit generator was adapted from a model presented in Dr. Carlos Mastrangelo's doctoral dissertation, *Thermal Applications of Microbridges*, U. C. Berkeley, 1991. Dr. Mastrangelo's model was written to generate a complete SPICE deck file of a microbridge compatible with SPICE3. This model has been modified to generate a subcircuit file for use in HSPICE. In addition, provisions are made to allow the bridge element to be connected to other elements to form a network of microbridges. Other changes include the addition of a thermal radiation component and the automatic calculation of the excess flux coefficient, η, from the device parameters as described in Chapter 4.

The example input and output files describe a 180 x 16 μm MUMPs *Poly 1* microbridge which represents the dimensions typically used for the cold arm in a lateral thermal actuator. The input file listing shows the physical parameters and information required by the subcircuit generator. For this example, the microbridge will be divided into 10 finite elements (*NUM_ELEM*) and has been designated as the second actuator element (*ACTUATOR_ELEMENT*). The designation as the second actuator element

controls the node numbering used for creating the HSPICE subcircuit. The generated output file is immediately ready for use as a subcircuit in an HSPICE network.

A.1 Example Input File Listing

```
$
$                   Electrothermal HSPICE Microbridge Input File
$                   Capt Jeff Butler  AFIT/ENG
$                   Adapted from Mastrangelo, Thermal Applications of Microbridges,
$                         PhD Dissertation, UC Berkeley, 1991.
$
$         Microbridge Dimensions
$
BRD_LEN          180.0e-6 m     /* bridge length      */
BRD_WIDTH        16.0e-6 m           /* bridge width      */
BRD_THICK        2.0e-6 m            /* poly thickness    */
TRNC_DEPTH       2.0e-6 m            /* height above substrate      */
$
$         Material Parameters
$
KAPPA_GAS        2.6e-2 W/m/K        /* gas thermal cond.  */
KINK_PRESS       1.34e4 Pa           /* kink pressure      */
SUBS_TEMP        300  K              /* substrate temp.    */
ETA              1.375   -           /* excess flux coeff. */
KAPPA_POLY       30.0  W/m/K         /* poly therm. cond.  */
KAPPA_NIT        3.0  W/m/K          /* nitride therm. cond. */
HEAT_CAP_POLY    7.0e2 J/kg/K        /* poly heat cap      */
HEAT_CAP_NIT     8.0e2 J/kg/K        /* nitride heat cap   */
DENSITY_POLY     2.33e3 kg/m/m/m     /* poly density       */
DENSITY_NIT      3.0e3 kg/m/m/m      /* nitride density    */
RESISTIVITY      1.525e-5 ohm-m      /* poly resistivity   */
POLY_TCR         1.25e-3 1/K         /* temp. coeff. res.  */
AREA_POLY        3.2e-11  m^2        /* area of poly       */
AREA_NIT         1e-19  m^2          /* area of nitride    */
$
$         Conversion Parameters
$
NUM_ELEM                 10          /* number of elements  */
INIT_NODE                1000        /*   initial node      */
ACTUATOR_ELEMENT         2           /* 1-Hot 2-cold 3-flex */
```

A.2 Example Output File Listing

```
*$
*$                  Electrothermal HSPICE Microbridge Output File
*$                  Capt Jeff Butler  AFIT/ENG
*$                  Adapted from Mastrangelo, Thermal Applications of Microbridges,
*$                        PhD Dissertation, UC Berkeley, 1991.
*$
*$
*$         Microbridge Dimensions
*$
*BRD_LEN         180.0e-6 m          /* bridge length      */
*BRD_WIDTH       16.0e-6 m           /* bridge width       */
*BRD_THICK       2.0e-6 m            /* poly thickness     */
*TRNC_DEPTH      2.0e-6 m            /* height above substrate      */
*$
*$         Material Parameters
*$
```

```
*KAPPA_GAS          2.6e-2 W/m/K        /* gas thermal cond.   */
*KINK_PRESS         1.34e4 Pa           /* kink pressure       */
*SUBS_TEMP          300  K              /* substrate temp.     */
*ETA                1.375               /* excess flux coeff.  */
*KAPPA_POLY         30.0  W/m/K         /* poly therm. cond.   */
*KAPPA_NIT          3.0  W/m/K          /* nitride therm. cond. */
*HEAT_CAP_POLY      7.0e2 J/kg/K        /* poly heat cap       */
*HEAT_CAP_NIT       8.0e2 J/kg/K        /* nitride heat cap    */
*DENSITY_POLY       2.33e3 kg/m/m/m     /* poly density        */
*DENSITY_NIT        3.0e3 kg/m/m/m      /* nitride density     */
*RESISTIVITY        1.525e-5 ohm-m      /* poly resistivity    */
*POLY_TCR           1.25e-3 1/K         /* temp. coeff. res.   */
*AREA_POLY          3.2e-11  m^2        /* area of poly        */
*AREA_NIT           1e-19  m^2          /* area of nitride     */
*$
*$          Conversion Parameters
*$
*NUM_ELEM                   10          /* number of elements  */
*INIT_NODE                  1000        /*   initial node      */
*ACTUATOR_ELEMENT           2           /* 1-Hot 2-cold 3-flex */
*$
* calculated value of eta is: 1.375
*.subckt subckt_name inputs outputs power ground
*.subckt bridge elec1 elec2 therm1 therm2 temp_sub pressure
.subckt bridge2 1013 1023 1001 1012 1000 1024
*
*
*-------------------------------------------------------
*                                  -
*             Node Information     -
*                                  -
*-------------------------------------------------------
*       electrical branch      - thermal branch  -
*                    -              -
* xa(um)  xb(um)  node_a  node_b - xc(um)  node   -
*-------------------------------------------------------
*         therm1                 0    1000   -
*    0     18    1012    1013     9    1001   -
*   18     36    1013    1014    27    1002   -
*   36     54    1014    1015    45    1003   -
*   54     72    1015    1016    63    1004   -
*   72     90    1016    1017    81    1005   -
*   90    108    1017    1018    99    1006   -
*  108    126    1018    1019   117    1007   -
*  126    144    1019    1020   135    1008   -
*  144    162    1020    1021   153    1009   -
*  162    180    1021    1022   171    1010   -
*         therm2                180    1011   -
*-------------------------------------------------------
* gas pressure node:            1024          -
* substrate temperature node:    1000         -
*-------------------------------------------------------
*
* gas pressure voltage source
*
*vPress 1024 0 dc
*
*-------------------------------------------------------
*
*             Thermal branch
*
*-------------------------------------------------------
*
* heat conduction loss resistors
*
```

```
Rc_th1   1001 1002  9.375k
Rc_th2   1002 1003  18.75k
Rc_th3   1003 1004  18.75k
Rc_th4   1004 1005  18.75k
Rc_th5   1005 1006  18.75k
Rc_th6   1006 1007  18.75k
Rc_th7   1007 1008  18.75k
Rc_th8   1008 1009  18.75k
Rc_th9   1009 1010  18.75k
Rc_th10  1010 1011  18.75k
Rc_th11  1011 1012  9.375k
*
* heat storage capacitors
*
Cth1   1002  0  0.939456nf
Cth2   1003  0  0.939456nf
Cth3   1004  0  0.939456nf
Cth4   1005  0  0.939456nf
Cth5   1006  0  0.939456nf
Cth6   1007  0  0.939456nf
Cth7   1008  0  0.939456nf
Cth8   1009  0  0.939456nf
Cth9   1010  0  0.939456nf
Cth10  1011  0  0.939456nf
*
*   pressure dependent heat losses
*
Glgc1   1002 1000 CUR='(v(1002)-v(1000))/194250*v(1024)/(1 + v(1024))'
Glgc2   1003 1000 CUR='(v(1003)-v(1000))/194250*v(1024)/(1 + v(1024))'
Glgc3   1004 1000 CUR='(v(1004)-v(1000))/194250*v(1024)/(1 + v(1024))'
Glgc4   1005 1000 CUR='(v(1005)-v(1000))/194250*v(1024)/(1 + v(1024))'
Glgc5   1006 1000 CUR='(v(1006)-v(1000))/194250*v(1024)/(1 + v(1024))'
Glgc6   1007 1000 CUR='(v(1007)-v(1000))/194250*v(1024)/(1 + v(1024))'
Glgc7   1008 1000 CUR='(v(1008)-v(1000))/194250*v(1024)/(1 + v(1024))'
Glgc8   1009 1000 CUR='(v(1009)-v(1000))/194250*v(1024)/(1 + v(1024))'
Glgc9   1010 1000 CUR='(v(1010)-v(1000))/194250*v(1024)/(1 + v(1024))'
Glgc10  1011 1000 CUR='(v(1011)-v(1000))/194250*v(1024)/(1 + v(1024))'
*
*   Thermal radiation losses
*
Gltr1   1002 1000 VCCS poly(2) 1002 0 1000 0  0 0 0 0 0 0 0 0 0 0 2.57191e-17 0 0 0 -2.57191e-17
Gltr2   1003 1000 VCCS poly(2) 1003 0 1000 0  0 0 0 0 0 0 0 0 0 0 2.57191e-17 0 0 0 -2.57191e-17
Gltr3   1004 1000 VCCS poly(2) 1004 0 1000 0  0 0 0 0 0 0 0 0 0 0 2.57191e-17 0 0 0 -2.57191e-17
Gltr4   1005 1000 VCCS poly(2) 1005 0 1000 0  0 0 0 0 0 0 0 0 0 0 2.57191e-17 0 0 0 -2.57191e-17
Gltr5   1006 1000 VCCS poly(2) 1006 0 1000 0  0 0 0 0 0 0 0 0 0 0 2.57191e-17 0 0 0 -2.57191e-17
Gltr6   1007 1000 VCCS poly(2) 1007 0 1000 0  0 0 0 0 0 0 0 0 0 0 2.57191e-17 0 0 0 -2.57191e-17
Gltr7   1008 1000 VCCS poly(2) 1008 0 1000 0  0 0 0 0 0 0 0 0 0 0 2.57191e-17 0 0 0 -2.57191e-17
Gltr8   1009 1000 VCCS poly(2) 1009 0 1000 0  0 0 0 0 0 0 0 0 0 0 2.57191e-17 0 0 0 -2.57191e-17
Gltr9   1010 1000 VCCS poly(2) 1010 0 1000 0  0 0 0 0 0 0 0 0 0 0 2.57191e-17 0 0 0 -2.57191e-17
Gltr10  1011 1000 VCCS poly(2) 1011 0 1000 0  0 0 0 0 0 0 0 0 0 0 2.57191e-17 0 0 0 -2.57191e-17
*
*   power generation
*
Glpg1   1000 1002 CUR='((v(1013)-v(1014))*(v(1013)-v(1014)))/(5.36133 + 0.0107227*v(1002))'
Glpg2   1000 1003 CUR='((v(1014)-v(1015))*(v(1014)-v(1015)))/(5.36133 + 0.0107227*v(1003))'
Glpg3   1000 1004 CUR='((v(1015)-v(1016))*(v(1015)-v(1016)))/(5.36133 + 0.0107227*v(1004))'
Glpg4   1000 1005 CUR='((v(1016)-v(1017))*(v(1016)-v(1017)))/(5.36133 + 0.0107227*v(1005))'
Glpg5   1000 1006 CUR='((v(1017)-v(1018))*(v(1017)-v(1018)))/(5.36133 + 0.0107227*v(1006))'
Glpg6   1000 1007 CUR='((v(1018)-v(1019))*(v(1018)-v(1019)))/(5.36133 + 0.0107227*v(1007))'
Glpg7   1000 1008 CUR='((v(1019)-v(1020))*(v(1019)-v(1020)))/(5.36133 + 0.0107227*v(1008))'
Glpg8   1000 1009 CUR='((v(1020)-v(1021))*(v(1020)-v(1021)))/(5.36133 + 0.0107227*v(1009))'
Glpg9   1000 1010 CUR='((v(1021)-v(1022))*(v(1021)-v(1022)))/(5.36133 + 0.0107227*v(1010))'
Glpg10  1000 1011 CUR='((v(1022)-v(1023))*(v(1022)-v(1023)))/(5.36133 + 0.0107227*v(1011))'
*
* substrate temperature
```

```
*
*vTs 1000 0 300v
*
*--------------------------------------------------------------
*
*               Electrical branch
*
*--------------------------------------------------------------
*
*Vb 1013 0 pulse(0 2 1ms 10ns 10ns 10ms 20ms)
*
Gbr1   1013 1014 VCR poly(1) 1002 0 5.36133 0.0107227
Gbr2   1014 1015 VCR poly(1) 1003 0 5.36133 0.0107227
Gbr3   1015 1016 VCR poly(1) 1004 0 5.36133 0.0107227
Gbr4   1016 1017 VCR poly(1) 1005 0 5.36133 0.0107227
Gbr5   1017 1018 VCR poly(1) 1006 0 5.36133 0.0107227
Gbr6   1018 1019 VCR poly(1) 1007 0 5.36133 0.0107227
Gbr7   1019 1020 VCR poly(1) 1008 0 5.36133 0.0107227
Gbr8   1020 1021 VCR poly(1) 1009 0 5.36133 0.0107227
Gbr9   1021 1022 VCR poly(1) 1010 0 5.36133 0.0107227
Gbr10  1022 1023 VCR poly(1) 1011 0 5.36133 0.0107227
*
*R1 1023 0 1
*
*.tran 200us 17ms
*.option brief post
*--------------------------------------------------------------
*
.ends
```

A.3 HSPICE Electrothermal Subcircuit Generator Program Listing

```
/*
-------------------------------------------------------------------------
HSPICE Electrothermal Subcircuit Generator Program
Capt Jeff Butler   AFIT/ENG
Adapted from Mastrangelo, Thermal Applications of Microbridges,
            PhD Dissertation, UC Berkeley, 1991.
-------------------------------------------------------------------------
*/

#include      <time.h>
#include      <stdio.h>
#include      <math.h>
#include      <strings.h>
#include      <sys/types.h>
#include      <sys/timeb.h>
#define       TRUE   1
#define       FALSE  0
#define       MAXLINELEN     80
#define       NULL_CHAR      "\0"

main(argc, argv)
int argc;
char *argv[];

{
    /*
    ---------------------------------------------------------------

        Usage: cbridge_spc  < in_file > out_file.spice

        create a finite-difference HSPICE model of a
        microbridge.
```

microbridge input parameters:

length
width
thickness
depth
kappa_gas
kink pressure
substrate temperature
excess flux coefficient
kappa_poly
kappa_nitride
C_poly
C_nitride
dens_poly
dens_nitride
poly resistivity
poly TCR
cross sectional area of polysilicon
cross sectional area of silicon nitride
number of elements
initial node number

The output of the program is a HSPICE file.

---
*/

```
int   i,j;
int   num_therm_nodes;
int   num_elec_nodes;
int   num_tot_nodes;
int   num_elem;
int   init_node;
int   Ts_node;
int   press_node;
int   node;
int   tnode;
int   last_node;
int   temp_sub_node;
int   enode;
int   res_num;
int   actuator_element;


char  line[MAXLINELEN];
char  label[MAXLINELEN];

double bridge_length;
double bridge_width;
double bridge_thick;
double trench_depth;
double kappa_gas;
double kink_pressure;
double kappa_poly;
double kappa_nit;
double heat_cap_poly;
double heat_cap_nit;
double area_poly;
double area_nit;
double density_poly;
double density_nit;
double kappa_eq;
```

```
double  density_eq;
double  heat_cap_eq1;
double  resistivity;
double  TCR;
double  delta;
double  eta;
double  Ts;

double  Rc_th;
double  Rp_th;
double  Ro_el;
double  Cp;
double  x,dx;
double  emissivity;
double  stef_con;
double rad_con, rad_con_neg;

/*
-----------------------------------------------------------------
     Reading the input parameters
-----------------------------------------------------------------
*/

     gets(line);
     printf("* %s\n",line);
     gets(line);
     printf("* %s\n",line);
     gets(line);
     printf("* %s\n",line);
     gets(line);
     printf("* %s\n",line);
     gets(line);
     printf("* %s\n",line);
     gets(line);
     printf("* %s\n",line);
     gets(line);
     printf("* %s\n",line);
     sscanf(line,"%s %lg\n",label,&bridge_length);
     gets(line);
     printf("* %s\n",line);
     sscanf(line,"%s %lg\n",label,&bridge_width);
     gets(line);
     printf("* %s\n",line);
     sscanf(line,"%s %lg\n",label,&bridge_thick);
     gets(line);
     printf("* %s\n",line);
     sscanf(line,"%s %lg\n",label,&trench_depth);
     gets(line);
     printf("* %s\n",line);
     gets(line);
     printf("* %s\n",line);
     gets(line);
     printf("* %s\n",line);
     gets(line);
     printf("* %s\n",line);
     sscanf(line,"%s %lg\n",label,&kappa_gas);
     gets(line);
     printf("* %s\n",line);
     sscanf(line,"%s %lg\n",label,&kink_pressure);
     gets(line);
     printf("* %s\n",line);
     sscanf(line,"%s %lg\n",label,&Ts);
     gets(line);
     printf("* %s\n",line);
     sscanf(line,"%s %lg\n",label,&eta);
```

```
        gets(line);
        printf("* %s\n",line);
        sscanf(line,"%s %lg\n",label,&kappa_poly);
        gets(line);
        printf("* %s\n",line);
        sscanf(line,"%s %lg\n",label,&kappa_nit);
        gets(line);
        printf("* %s\n",line);
        sscanf(line,"%s %lg\n",label,&heat_cap_poly);
        gets(line);
        printf("* %s\n",line);
        sscanf(line,"%s %lg\n",label,&heat_cap_nit);
        gets(line);
        printf("* %s\n",line);
        sscanf(line,"%s %lg\n",label,&density_poly);
        gets(line);
        printf("* %s\n",line);
        sscanf(line,"%s %lg\n",label,&density_nit);
        gets(line);
        printf("* %s\n",line);
        sscanf(line,"%s %lg\n",label,&resistivity);
        gets(line);
        printf("* %s\n",line);
        sscanf(line,"%s %lg\n",label,&TCR);
        gets(line);
        printf("* %s\n",line);
        sscanf(line,"%s %lg\n",label,&area_poly);
        gets(line);
        printf("* %s\n",line);
        sscanf(line,"%s %lg\n",label,&area_nit);
        gets(line);
        printf("* %s\n",line);
        gets(line);
        printf("* %s\n",line);
        gets(line);
        printf("* %s\n",line);
        gets(line);
        printf("* %s\n",line);
        sscanf(line,"%s %d\n",label,&num_elem);
        gets(line);
        printf("* %s\n",line);
        sscanf(line,"%s %d\n",label,&init_node);
        gets(line);
        printf("* %s\n",line);
        sscanf(line,"%s %d\n",label,&actuator_element);
        gets(line);
        printf("* %s\n",line);

/*
-----------------------------------------------------------------
            Find the node elements
-----------------------------------------------------------------
*/

        /* Eta (shape factor) calculation */

eta = (bridge_thick/bridge_width)*((2*trench_depth/bridge_thick) + 1) + 1;
printf("* calculated value of eta is: %lg \n", eta);

        delta = bridge_length/num_elem;

        kappa_eq = kappa_poly;

        heat_cap_eq1 = ( density_poly*heat_cap_poly);
```

```
    density_eq =  (density_poly);

    area_poly = bridge_width*bridge_thick;
    printf("* calculated cross-sectional area is: %lg \n", area_poly);


    Rc_th = delta/2.0/kappa_eq/bridge_width/bridge_thick*1e-3;

    Rp_th = trench_depth/eta/kappa_gas/bridge_width/delta;

    Ro_el = resistivity*delta/bridge_width/bridge_thick;

    Cp = (heat_cap_eq1*delta)*
       (area_poly + area_nit)*1e+9;

    /*  assemble the bridge      */

dx = bridge_length/num_elem;
temp_sub_node = init_node;
Ts_node = init_node;
press_node = init_node + 2*num_elem + 4;
node = init_node;
enode = init_node + num_elem + 1;

      /*  Thermal radiation constants     */

emissivity = .7;
stef_con = 56.7e-9;
rad_con = 2*emissivity*stef_con*(bridge_thick + bridge_width)*dx;
rad_con_neg = -rad_con;

      /* HSPICE Subcircuit data */

printf("*.subckt subckt_name inputs outputs power ground   \n");
printf("*.subckt bridge elec1 elec2 therm1 therm2 temp_sub pressure   \n");
printf(".subckt bridge%d %d %d %d %d %d %d \n",actuator_element, init_node + num_elem + 3,
     init_node + (2*num_elem) + 3, init_node + 1, init_node + num_elem + 2,
     init_node, press_node);

printf("* \n");
printf("* \n");
printf("*-------------------------------------------------------\n");
printf("*                                                -\n");
printf("*              Node Information                  -\n");
printf("*                                                -\n");
printf("*-------------------------------------------------------\n");
printf("*       electrical branch      - thermal branch   -\n");
printf("*                              -                 -\n");
printf("*  xa(um)  xb(um)  node_a  node_b - xc(um)   node    -\n");
printf("*-------------------------------------------------------\n");
printf("*          therm1              %6lg   %6d    -\n",0.0,node);

x  = 0.0;
node++;
for (j=1;j <= num_elem;j++) {
     printf("* %6lg  %6lg  %6d  %6d  %6lg   %6d    -\n",
     x*1e6,(x+dx)*1e6,enode+1,enode+2,(x+dx/2)*1e6,node);
     node++;
     enode++;
     x = x + dx;
}

printf("*          therm2              %6lg   %6d    -\n",x*1e6,node);
printf("*-------------------------------------------------------\n");
```

```
printf("* gas pressure node:            %6d          -\n",press_node);
printf("* substrate temperature node:   %6d          -\n",init_node);
printf("*-------------------------------------------------------\n");

num_therm_nodes = num_elem + 1 ;
num_elec_nodes = num_elem + 1 ;

node = init_node;

printf("*\n");
printf("* gas pressure voltage source \n");
printf("*\n");
printf("*vPress %d 0 dc \n",press_node);
printf("*\n");

printf("*-------------------------------------------------------\n");
printf("*\n");
printf("*              Thermal branch              \n");
printf("*\n");
printf("*-------------------------------------------------------\n");

res_num = 1;

printf("*\n");
printf("*  heat conduction loss resistors    \n");
printf("*\n");


printf("Rc_th%-3d %d %d  %lgk\n",res_num,node+1,node+2,Rc_th);
node++;
res_num++;

for (j=2;j <= num_elem; j++ ) {

     printf("Rc_th%-3d %d %d  %lgk\n",res_num,node+1,node+2,2.0*Rc_th);
     node++;
     res_num++;
}

printf("Rc_th%-3d %d %d  %lgk\n",res_num,node+1,node+2,Rc_th);
node++;

printf("*\n");
printf("*  heat storage capacitors    \n");
printf("*\n");

node = init_node+1;
res_num=1;
for (j=1;j <= num_elem; j++ ) {

     printf("Cth%-3d %d  0  %lgnf\n",res_num,node+1,Cp);
     node++;
     res_num++;
}

printf("*\n");
printf("*    pressure dependent heat losses    \n");
printf("*\n");

res_num = 1;
tnode = init_node+2;
for (j=1;j <= num_elem; j++) {

     printf("GIgc%-3d %d %d ",res_num,tnode,init_node);
     printf("CUR='(v(%d)-v(%d))",tnode,init_node);
```

```
        printf("/%lg*v(%d)/(1 + v(%d))'\n",Rp_th,
        press_node,press_node);
        tnode++;
        res_num++;
    }

    printf("*\n");
    printf("*   Thermal radiation losses    \n");
    printf("*\n");

    res_num = 1;
    tnode = init_node+2;
    for (j=1;j <= num_elem; j++) {

        printf("GItr%-3d %d %d ",res_num,tnode,init_node);
        printf("VCCS poly(2) %d 0 %d 0 ",tnode, Ts_node);
        printf(" 0 0 0 0 0 0 0 0 0 0 ");
        printf("%lg 0 0 0 %lg \n",rad_con, rad_con_neg);
        tnode++;
        res_num++;
    }

    printf("*\n");
    printf("*    power generation   \n");
    printf("*\n");

    res_num = 1;
    tnode = init_node+2;
    for (j=1;j <= num_elem; j++) {

        printf("GIpg%-3d %d %d ",res_num,init_node,tnode);
        printf("CUR='((v(%d)-v(%d))*",node+2,node+3);
        printf("(v(%d)-v(%d)))",node+2,node+3);
        printf("/(%lg + %lg*v(%d))'\n",Ro_el*(1.0-Ts*TCR),
        Ro_el*TCR,tnode);
        tnode++;
        node++;
        res_num++;
    }

    printf("*\n");
    printf("*  substrate temperature       \n");
    printf("*\n");
    printf("*vTs %d 0 %lgv\n",init_node,Ts);
    printf("*\n");
    printf("*--------------------------------------------------------------------\n");
    printf("*\n");
    printf("*                Electrical branch                    \n");
    printf("*\n");
    printf("*--------------------------------------------------------------------\n");
    printf("*\n");

    node = tnode + 1;
    res_num = 1;
    tnode = init_node+2;
    printf("*Vb %d 0 pulse(0 2 1ms 10ns 10ns 10ms 20ms) \n", node);
    printf("*\n");

    for (j=1;j <= num_elem; j++) {

        printf("Gbr%-3d %d %d ",res_num,node,node+1);
        printf("VCR poly(1) %d 0",tnode);
        printf(" %lg %lg \n",Ro_el*(1.0-Ts*TCR), Ro_el*TCR);
        last_node = node+1;
        tnode++;
```

```
            node++;
            res_num++;
        }

        printf("*\n");

printf("*R1 %d 0 1\n",last_node);
printf("*\n");


printf("*.tran 200us 17ms\n");

printf("*.option brief post \n");


printf("*--------------------------------------------------------------\n");
        printf("*\n");
        printf(".ends\n");


}


int strindex( s, t )
char s[],t[];
{
        int i,j , k;

        for ( i=0; s[i] != '\0'; i++ ) {
            for ( j=i,k=0;t[k] !='\0' && s[j] == t[k]; j++,k++)
                ;
            if ( t[k] == '\0' )
                return (i);
        }
        return (-1);
}
```

Appendix B. TSUPREM Simulation of MUMPs Fabrication

Appendix B contains an example input file for simulating the MUMPs fabrication process in TSUPREM-4 version 6.0.x. This particular file was used for evaluating the resistivity of MUMPs *Poly 1* as discussed in Chapter 5. The file describes the fabrication of a 12 μm wide *Poly 1* linestructure with no surrounding *Poly 0* or *Poly 2* structures. The commands for creating and patterning *Poly 0* and *Poly 2* are in the example but have been commented out so that they are not executed.

TSUPREM has good graphics capability, and Figures B-1 through B-3 show 1-3 dimensional perspectives of the final phosphorus doping profiles from the example input file.

B.1 TSUPREM Input File for MUMPs *Poly 1* Fabrication

```
$ Capt Jeff Butler
$ MUMPs Process
$ Resistivity Simulation for 12 um Wide Poly 1 Linestructure

$ Set up the grid
LINE X   LOC=0.0  SPAC=0.5
LINE X   LOC=9    SPAC=0.5

LINE Y   LOC=0    SPAC=0.5
LINE Y   LOC=3.0  SPAC=0.5

$ (100) Si substrate with Phosphor doping concentration of 1E15
INITIALIZE <100> phosphor=1e15

$deposit nitride, poly 0, and 1st oxide
deposition nitride thick=0.6
$deposit poly thick = 0.5
deposition oxide thick=2.0 phosphor=4.2e20

SELECT    Z=LOG10(phosphor) TITLE="Phosphor Doping before anneals"
PLOT.1D   X.V=3.1  y.min=15

$first anneal
diffusion time=60 temp=1050 inert

SELECT    Z=LOG10(phosphor) TITLE="Phosphor Doping after 1st Anneal"
PLOT.1D   X.V=3.1  y.min=15
```

```
$deposit poly 1
deposition poly thick=2.0
deposition oxide thick=.2 phosphor=4.2e20

$second anneal
diffusion time=60 temp=1050 inert

$ pattern poly
etch oxide old.dry thick=.2

$etch poly all
ETCH poly left P1.X=3

STRUCTURE REFLECT RIGHT

SELECT    Z=LOG10(phosphor) TITLE="Phosphor Doping after 2nd (Center)"
PLOT.1D   X.V=9  y.min=15

SELECT    Z=LOG10(phosphor) TITLE="Phosphor Doping after 2nd (Edge)"
PLOT.1D   X.V=3.1  y.min=15

$deposit 2nd oxide
deposition oxide thick=.75 phosphor=4.2e20
$ phosphor initially 4.2e20

SELECT    Z=LOG10(phosphor) TITLE="Phosphor Doping after 2nd ox (Center)"
PLOT.1D   X.V=9  y.min=15

SELECT    Z=LOG10(phosphor) TITLE="Phosphor Doping after 2nd ox (Edge)"
PLOT.1D   X.V=3.1  y.min=15

$Third anneal
diffusion time=60 temp=1050 inert

SELECT    Z=LOG10(phosphor) TITLE="Phosphor Doping after 3rd (Center)"
PLOT.1D   X.V=9  y.min=15

SELECT    Z=LOG10(phosphor) TITLE="Phosphor Doping after 3rd (Edge)"
PLOT.1D   X.V=3.1  y.min=15

$deposit poly 2
$deposition poly thick=1.5
deposition oxide thick=.2 phosphor=4.2e20

SELECT    Z=LOG10(phosphor) TITLE="Phosphor Doping after 2nd cap (Center)"
PLOT.1D   X.V=9  y.min=15

SELECT    Z=LOG10(phosphor) TITLE="Phosphor Doping after 2nd cap (Edge)"
PLOT.1D   X.V=3.1  y.min=15

$fourth anneal
diffusion time=60 temp=1050 inert

SELECT    Z=LOG10(phosphor) TITLE="Final Phosphor Doping (Center)"
PLOT.1D   X.V=9  y.min=15

SELECT    Z=LOG10(phosphor) TITLE="Final Phosphor Doping (Edge)"
PLOT.1D   X.V=3.1  y.min=15

$ 2D contour plot of phosphor contours
SELECT    Z=LOG10(phosphor)  TITLE="2-D Phosphor Doping"
PLOT.2D   y.max=2.0 y.min=-8.2

          COLOR   MIN.V=(LOG10(1e1))  MAX.V=(LOG10(1e17))     COLOR=12
          COLOR   MIN.V=(LOG10(1e17)) MAX.V=(LOG10(1e18))     COLOR=13
```

```
          COLOR   MIN.V=(LOG10(1e18)) MAX.V=(LOG10(1e19))     COLOR=14
          COLOR   MIN.V=(LOG10(1e19)) MAX.V=(LOG10(5e19))     COLOR=15
          COLOR   MIN.V=(LOG10(5e19)) MAX.V=(LOG10(1e20))     COLOR=16
          COLOR   MIN.V=(LOG10(1e20)) MAX.V=(LOG10(5e20))     COLOR=17
          COLOR   MIN.V=(LOG10(5e20)) MAX.V=(LOG10(1e21))     COLOR=18
          COLOR   MIN.V=(LOG10(1e21)) MAX.V=(LOG10(1e22))     COLOR=19
PLOT.2D   ^AXES ^CLEAR
LABEL     X=.55 Y=-8.0 LABEL="Log10(Phosphor)" SIZE=0.3
LABEL     X=1.15 Y=-7.8 LABEL="< 1E17" SIZE=0.3 C.RECT=12 W.R=0.4 H.R=0.4
LABEL     X=1.15 Y=-7.6 LABEL="1E17-1E18" SIZE=0.3 C.RECT=13 W.R=0.4 H.R=0.4
LABEL     X=1.15 Y=-7.4 LABEL="1E18-1E19" SIZE=0.3 C.RECT=14 W.R=0.4 H.R=0.4
LABEL     X=1.15 Y=-7.2 LABEL="1E19-5E19" SIZE=0.3 C.RECT=15 W.R=0.4 H.R=0.4
LABEL     X=1.15 Y=-7.0 LABEL="5E19-1E20" SIZE=0.3 C.RECT=16 W.R=0.4 H.R=0.4
LABEL     X=1.15 Y=-6.8 LABEL="1E20-5E20" SIZE=0.3 C.RECT=17 W.R=0.4 H.R=0.4
LABEL     X=1.15 Y=-6.6 LABEL="5E20-1E21" SIZE=0.3 C.RECT=18 W.R=0.4 H.R=0.4
LABEL     X=1.15 Y=-6.4 LABEL="1E21-1E22" SIZE=0.3 C.RECT=19 W.R=0.4 H.R=0.4

$ 2D contour plot of phosphor contours
SELECT    Z=LOG10(phosphor) TITLE="2-D Phosphor Doping 1e20-2e20"
PLOT.2D   y.max=3.0 y.min=-8
          COLOR   MIN.V=(LOG10(1e1))  MAX.V=(LOG10(5e19))     COLOR=08
          COLOR   MIN.V=(LOG10(5e19)) MAX.V=(LOG10(1e20))     COLOR=9
          COLOR   MIN.V=(LOG10(1e20)) MAX.V=(LOG10(1.1e20))   COLOR=10
          COLOR   MIN.V=(LOG10(1.1e20)) MAX.V=(LOG10(1.2e20)) COLOR=11
          COLOR   MIN.V=(LOG10(1.2e20)) MAX.V=(LOG10(1.3e20)) COLOR=12
          COLOR   MIN.V=(LOG10(1.3e20)) MAX.V=(LOG10(1.4e20)) COLOR=13
          COLOR   MIN.V=(LOG10(1.4e20)) MAX.V=(LOG10(1.5e20)) COLOR=14
          COLOR   MIN.V=(LOG10(1.5e20)) MAX.V=(LOG10(1.6e20)) COLOR=15
          COLOR   MIN.V=(LOG10(1.6e20)) MAX.V=(LOG10(1.7e20)) COLOR=16
          COLOR   MIN.V=(LOG10(1.7e20)) MAX.V=(LOG10(1.8e20)) COLOR=17
          COLOR   MIN.V=(LOG10(1.8e20)) MAX.V=(LOG10(1.9e20)) COLOR=18
          COLOR   MIN.V=(LOG10(1.9e20)) MAX.V=(LOG10(1e21))   COLOR=19

PLOT.2D   ^AXES ^CLEAR
LABEL     X=0.55 Y=0.0 LABEL="Log10(Phosphor)" SIZE=0.3
$LABEL     X=1.15 Y=0.2 LABEL="< 5E19" SIZE=0.3 C.RECT=8 W.R=0.4 H.R=0.4
$LABEL     X=1.15 Y=0.4 LABEL="5E19-6E19" SIZE=0.3 C.RECT=9 W.R=0.4 H.R=0.4
$LABEL     X=1.15 Y=0.6 LABEL="6E19-7E19" SIZE=0.3 C.RECT=10 W.R=0.4 H.R=0.4
$LABEL     X=1.15 Y=0.8 LABEL="7E19-8E19" SIZE=0.3 C.RECT=11 W.R=0.4 H.R=0.4
$LABEL     X=1.15 Y=1.0 LABEL="8E19-9E19" SIZE=0.3 C.RECT=12 W.R=0.4 H.R=0.4
LABEL     X=1.15 Y=1.2 LABEL="9E19-1E20" SIZE=0.3 C.RECT=13 W.R=0.6 H.R=0.4
LABEL     X=1.15 Y=1.4 LABEL="1E20-1.1E20" SIZE=0.3 C.RECT=14 W.R=0.6 H.R=0.4
LABEL     X=1.15 Y=1.6 LABEL="1.1E20-1.2E20" SIZE=0.3 C.RECT=15 W.R=0.6 H.R=0.4
LABEL     X=1.15 Y=1.8 LABEL="1.2E20-1.3E20" SIZE=0.3 C.RECT=16 W.R=0.6 H.R=0.4
LABEL     X=1.15 Y=2.0 LABEL="1.3E20-1.4E20" SIZE=0.3 C.RECT=17 W.R=0.6 H.R=0.4
LABEL     X=1.15 Y=2.2 LABEL="1.4E20-1.5E20" SIZE=0.3 C.RECT=18 W.R=0.6 H.R=0.4
LABEL     X=1.15 Y=2.4 LABEL="1.5E20-1E21" SIZE=0.3 C.RECT=19 W.R=0.6 H.R=0.4

$pattern poly 2

etch oxide old.dry thick=.2

$etch poly left p1.x=3
$etch poly right p1.x=5
$etch poly all

$ 3D contour plot of phosphor contours
SELECT    Z=LOG10(phosphor) TITLE="Final 3-D Phosphor Doping"
PLOT.3D   theta=45 phi=45  y.max=1.0 num.cntr=30

$ End of simulation
```

B.2 Final Phosphorus Doping Profiles From TSUPREM Simulation

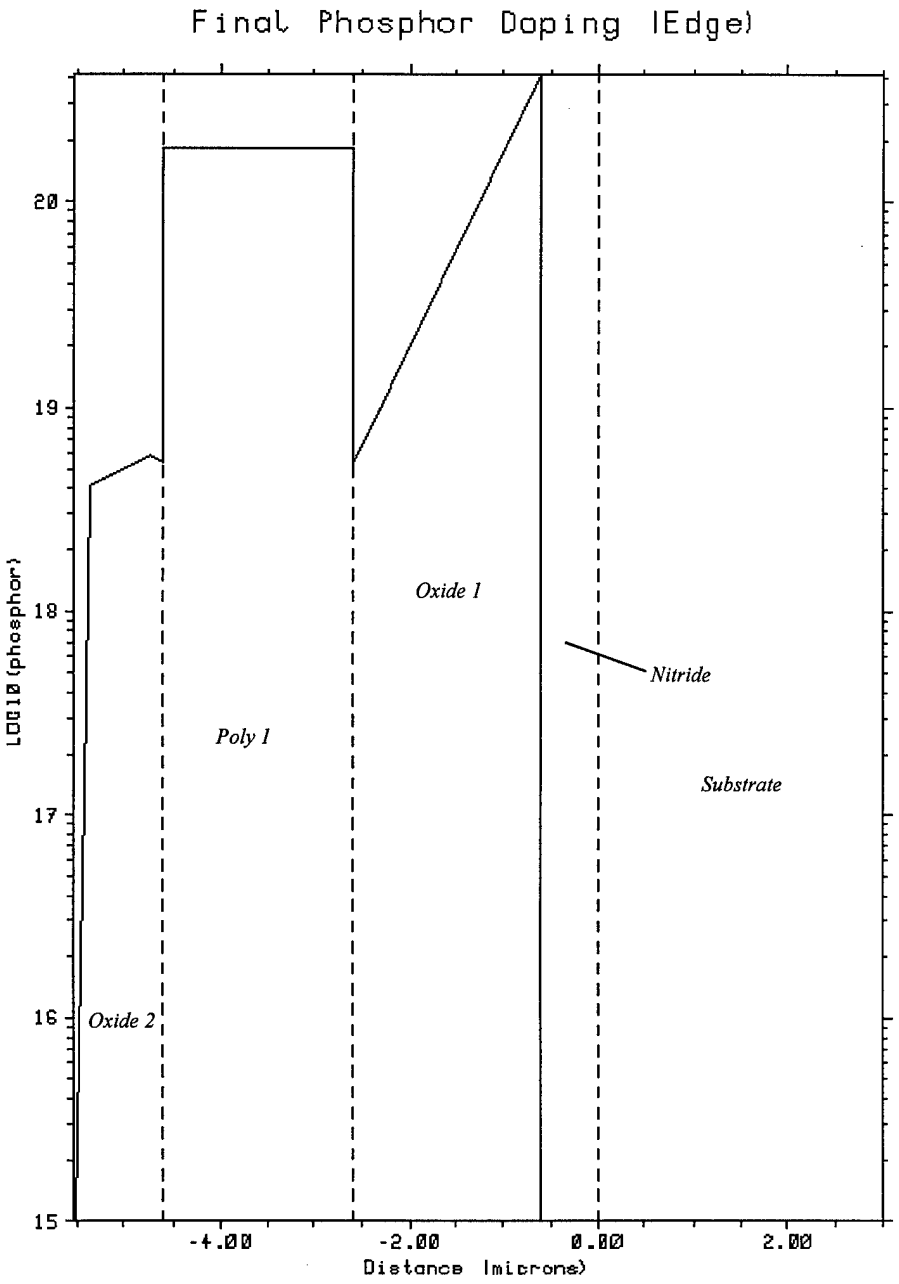


Figure B-1. TSUPREM 1-D phosphorus doping profile at the edge of a 12 μm wide *Poly 1* linestructure.

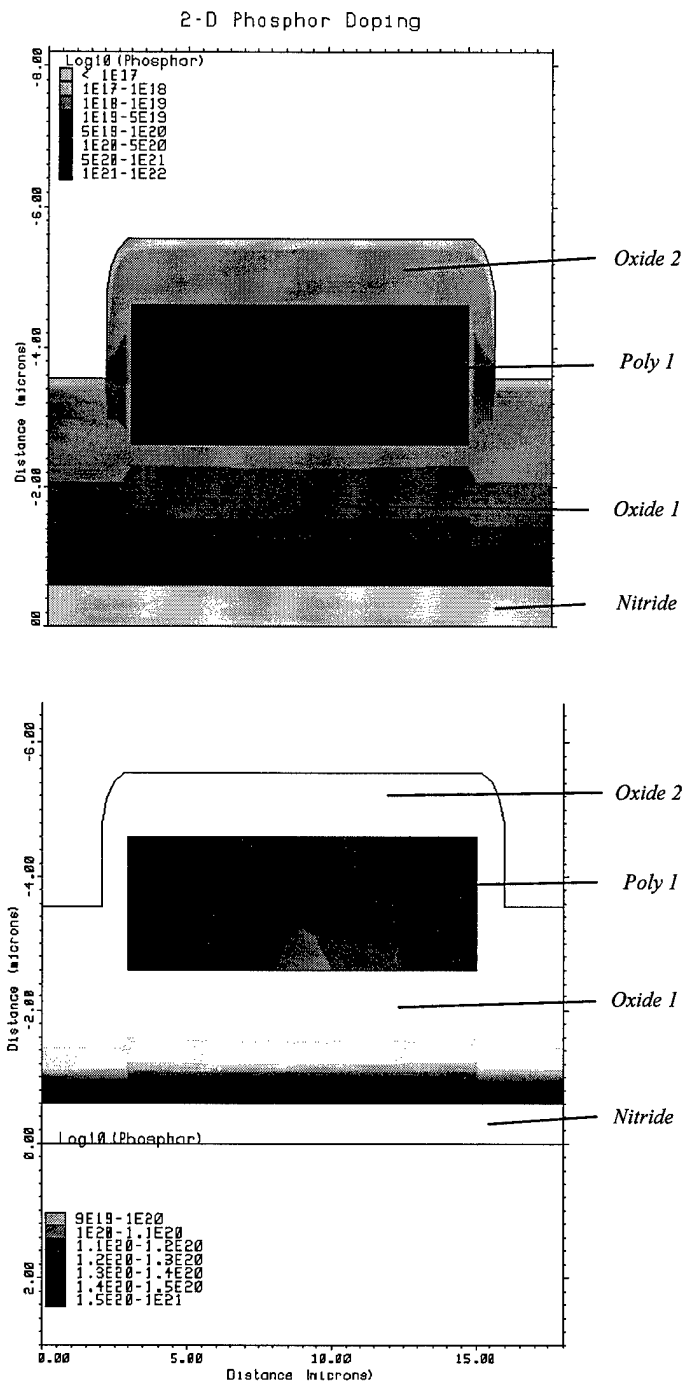


Figure B-2. TSUPREM 2-D phosphorus doping profiles for 12 μm wide Poly 1 linestructures. Note that the two plots represent the same data but are scaled differently to highlight different levels of doping.

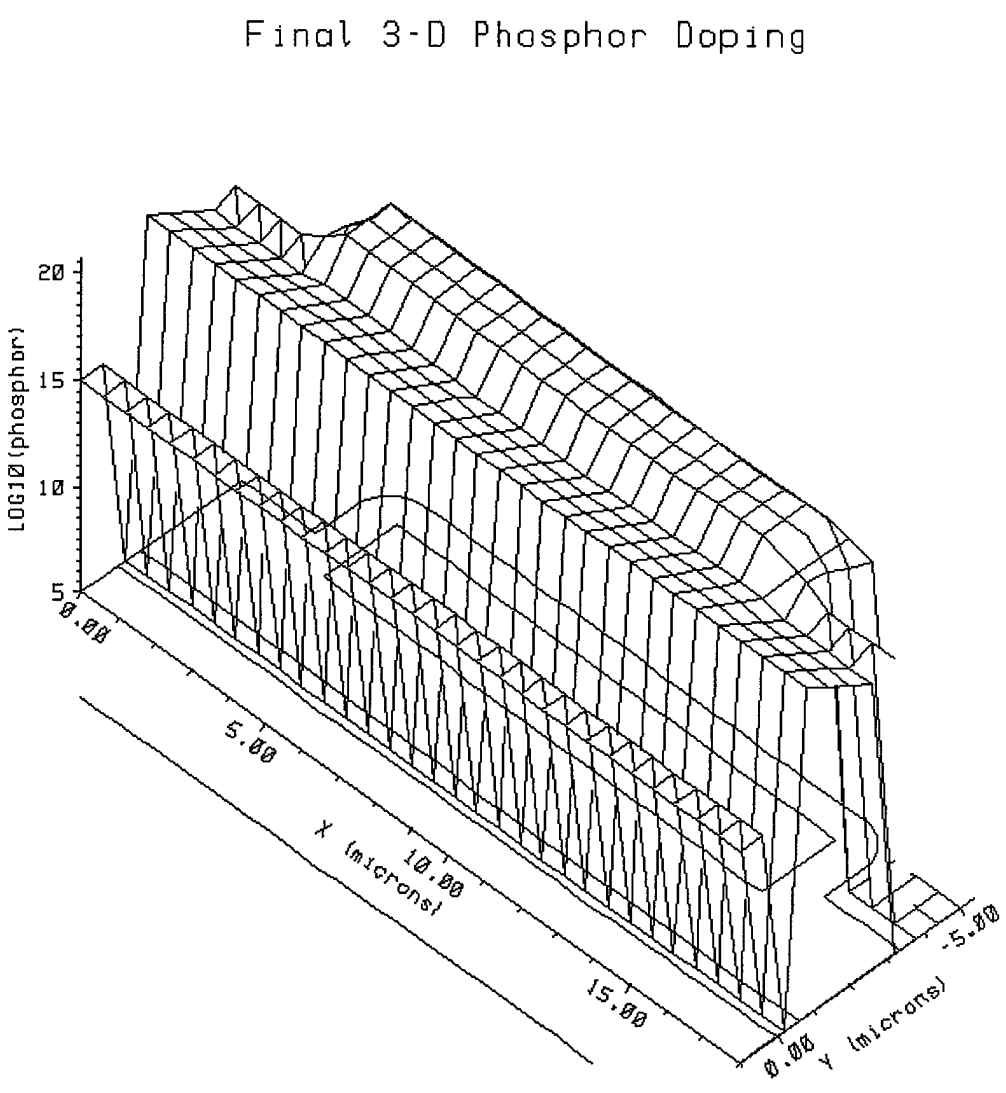


Figure B-3. TSUPREM 3-D phosphorus doping profile for a 12 μm wide Poly 1 linestructure.

Appendix C. VHDL Code and Descriptions for CMOS ASIC Controllers

This appendix provides the behavioral VHDL code for the two CMOS application specific integrated circuit (ASIC) controllers discussed in Chapters 6 and 8. The controllers on both chips were synthesized from behavioral VHDL using Synopsys, and they were fabricated through MOSIS using the Orbit 2.0 μm 'Tiny Chip' process. The VHDL code for both ASICs is very simple and methodical in order to assist the synthesis process. Attempts at synthesizing more 'elegant' code with nested loops and iteration were unsuccessful because the tool set could not properly convert the more abstract VHDL to a realizable layout.

C.1 Basic Controller

C.1.1 Description

The basic controller was the first ASIC design and was used for voltage amplitude control of the rotating micromirror. Figure C-1 shows a functional block diagram of the entire chip. The controller has three input select lines which will allow up to eight outputs to be addressed. The ACTIVATE signal is used to set the logic level for the selected output, and LOAD is a positive-edge triggered signal which latches the data on the select and ACTIVATE lines into the controller. The synchronous RESET signal forces all of the outputs to '0'.

The 8 output drivers are composed of varying numbers of California Institute of Technology (CIT) standard 2.0 μm pad drivers connected in parallel to provide varying

levels of current drive. The CIT pads are available from MOSIS and are widely used for the Orbit 2.0 μm process. Each of the CIT drivers is capable of sourcing a minimum of 15 mA. The two largest output drivers on the ASIC have 4 CIT drivers in parallel which provides greater than 60 mA of current at 5 volts which is sufficient to drive virtually all of the thermally actuated devices described in this dissertation.

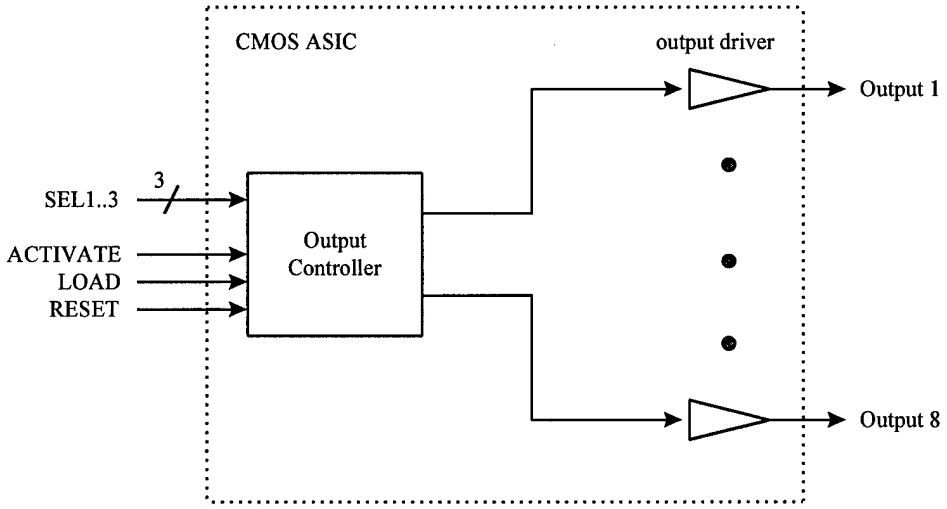


Figure C-1. Block diagram of first CMOS ASIC.

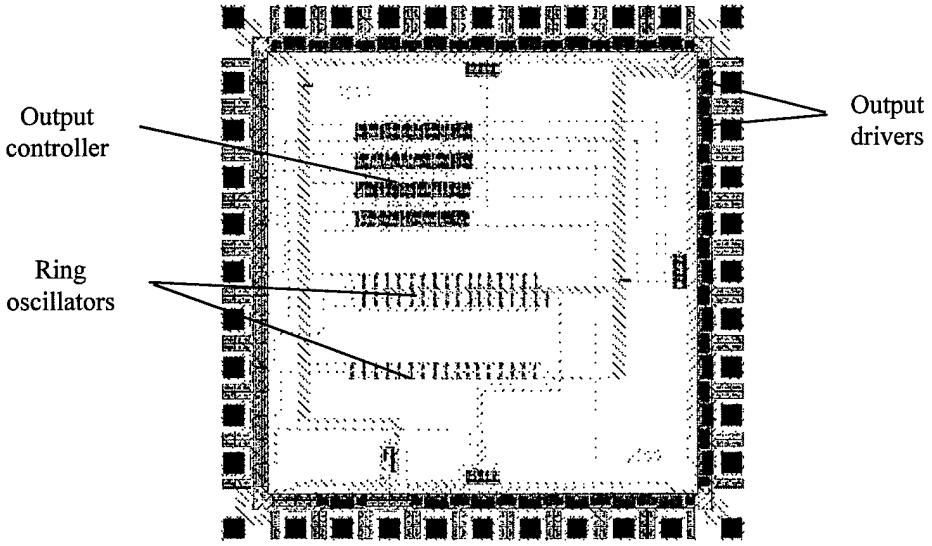


Figure C-2. Layout of first CMOS ASIC.

C.1.2 VHDL Code Listing

The output controller shown in Figure C-1 is the heart of this ASIC and was synthesized without modification from the following behavioral VHDL code.

```
------------------------------------------------------------
-- This is the behavioral entity/arch for CMOS packaging ctlr
--
-- Capt Jeff Butler
------------------------------------------------------------

library IEEE;
use IEEE.std_logic_1164.all;

ENTITY pack_ctlr IS
    Port (          RESET : IN STD_LOGIC := '0';
                    LOAD : IN STD_LOGIC := '0';
                    ACTIVATE : IN STD_LOGIC;
                    SEL1, SEL2, SEL3 : IN STD_LOGIC;
                    OUT0, OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7 : OUT
                    STD_LOGIC );
END pack_ctlr;


architecture behave of pack_ctlr IS

Begin
operation : PROCESS

begin -- process begin


wait until (LOAD'event and LOAD='1');

IF RESET = '1' THEN
  OUT0 <= '0';
  OUT1 <= '0';
  OUT2 <= '0';
  OUT3 <= '0';
  OUT4 <= '0';
  OUT5 <= '0';
  OUT6 <= '0';
  OUT7 <= '0';

ELSIF (SEL3='0') AND (SEL2='0') AND (SEL1='0') THEN
  OUT0 <= ACTIVATE;

ELSIF  (SEL3='0') AND (SEL2='0') AND (SEL1='1') THEN
  OUT1 <= ACTIVATE;

ELSIF  (SEL3='0') AND (SEL2='1') AND (SEL1='0') THEN
  OUT2 <= ACTIVATE;

ELSIF  (SEL3='0') AND (SEL2='1') AND (SEL1='1') THEN
  OUT3 <= ACTIVATE;

ELSIF  (SEL3='1') AND (SEL2='0') AND (SEL1='0') THEN
  OUT4 <= ACTIVATE;

ELSIF  (SEL3='1') AND (SEL2='0') AND (SEL1='1') THEN
```

```
    OUT5 <= ACTIVATE;

ELSIF  (SEL3='1') AND (SEL2='1') AND (SEL1='0') THEN
    OUT6 <= ACTIVATE;

ELSIF  (SEL3='1') AND (SEL2='1') AND (SEL1='1') THEN
    OUT7 <= ACTIVATE;

END IF;
-- wait until (CLK'event and CLK='1');

 END process operation;
END behave;
```

C.2 Pulse Modulation Controller

C.2.1 Description

The invention of pulse modulation control for thermal actuators required the design and fabrication of an ASIC chip with programmable pulse width modulation. Figure C-2 shows a functional block diagram of the pulse width modulation ASIC. The ASIC has a digital interface and eight output drivers. Four of the outputs can be pulse width modulated.

The ASIC has an internal pulse generator which produces seven pulse trains with different pulse widths. An on-board 20 MHz clock is included to provide a convenient way to run the pulse width generator. The internal pulse modulation controller uses the PW SELECT and INPUT SELECT signals to identify which one of the 8 pulse trains should be used for the specified output channel. The pulse trains from the pulse width generator and external source are buffered and can be used to modulate more than one channel at a time. In addition, after selection of the pulse train, the output channel continues to be modulated by the specified pulse train until that particular channel is selected and updated again. This allows for programming the pulse width on a single output without affecting the operation of the other channels.

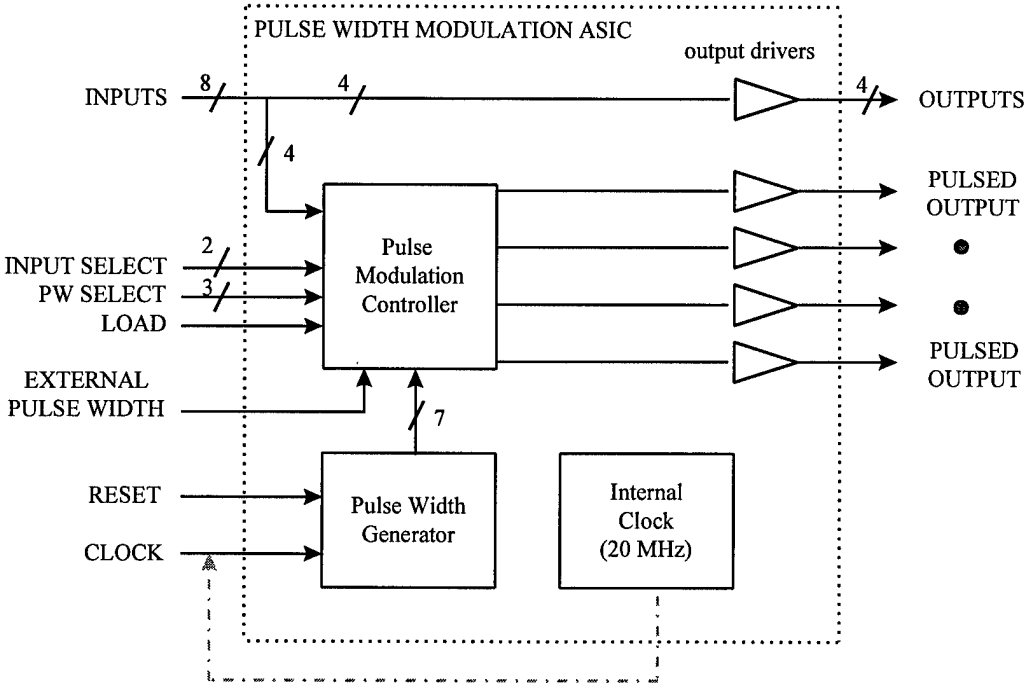


Figure C-3. Block diagram of Pulse Width Modulation ASIC.

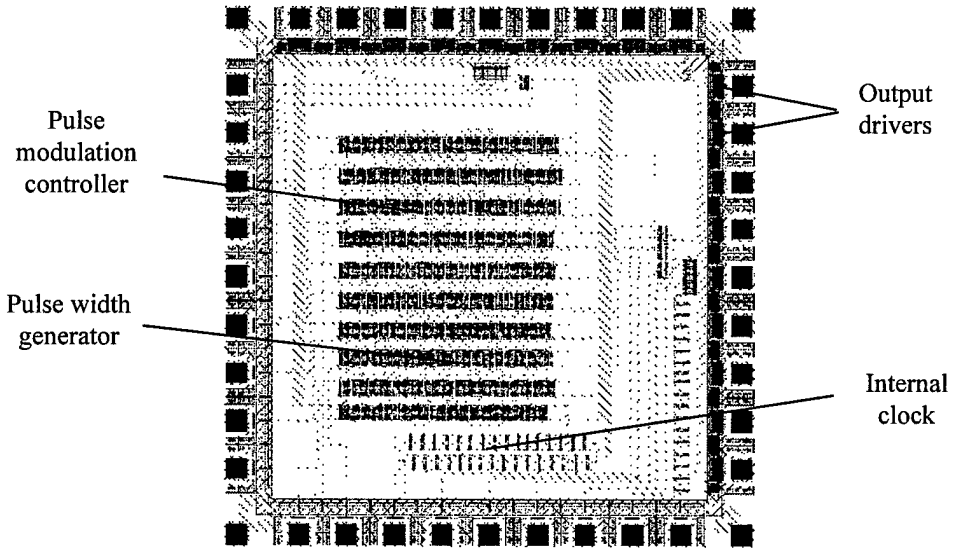


Figure C-4. Layout of pulse width modulation ASIC.

C.2.2 Synthesized Block Diagrams and VHDL Code Listing

The pulse width generator and the pulse modulation controller were synthesized from behavioral VHDL code. The following diagrams and schematics show the design as synthesized. The VHDL behavioral code is listed at the end of this section.

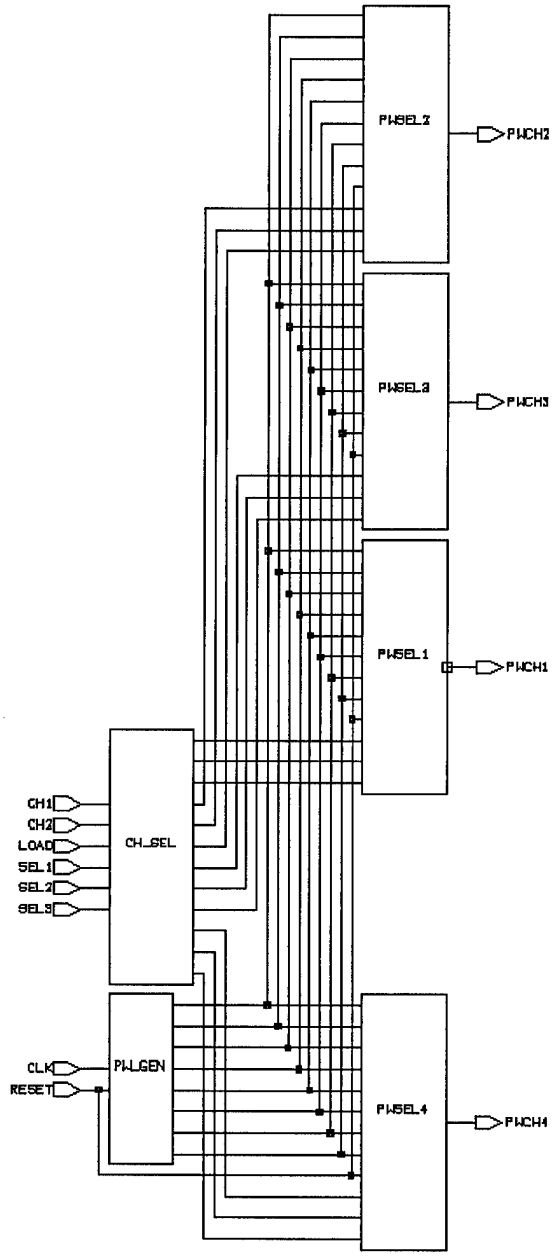


Figure C-5. Top level architecture for pulse width controller and generator.

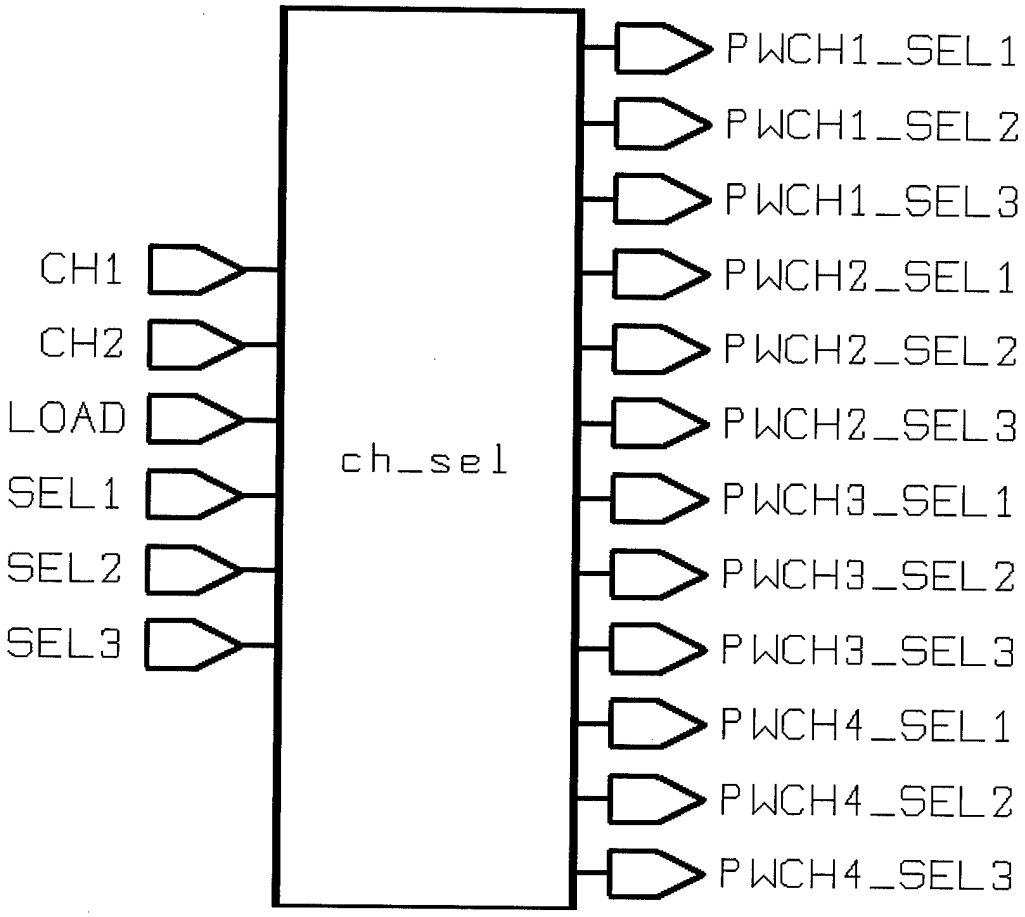


Figure C-6. I/O ports for the channel select (CH_SEL) element of the pulse width controller. This element determines which output channel should be updated.

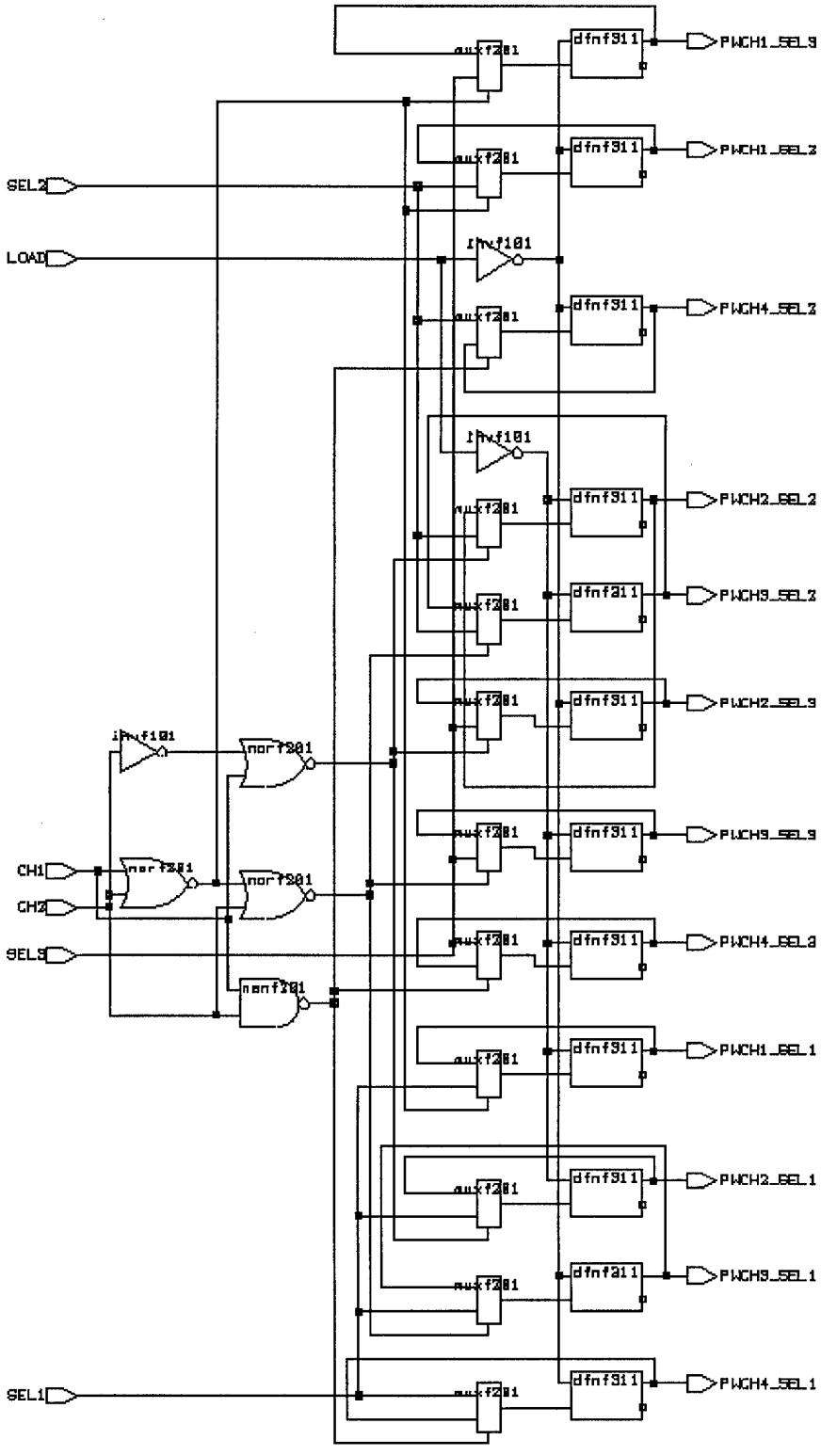


Figure C-7. Schematic of synthesized channel select (CH_SEL) element.

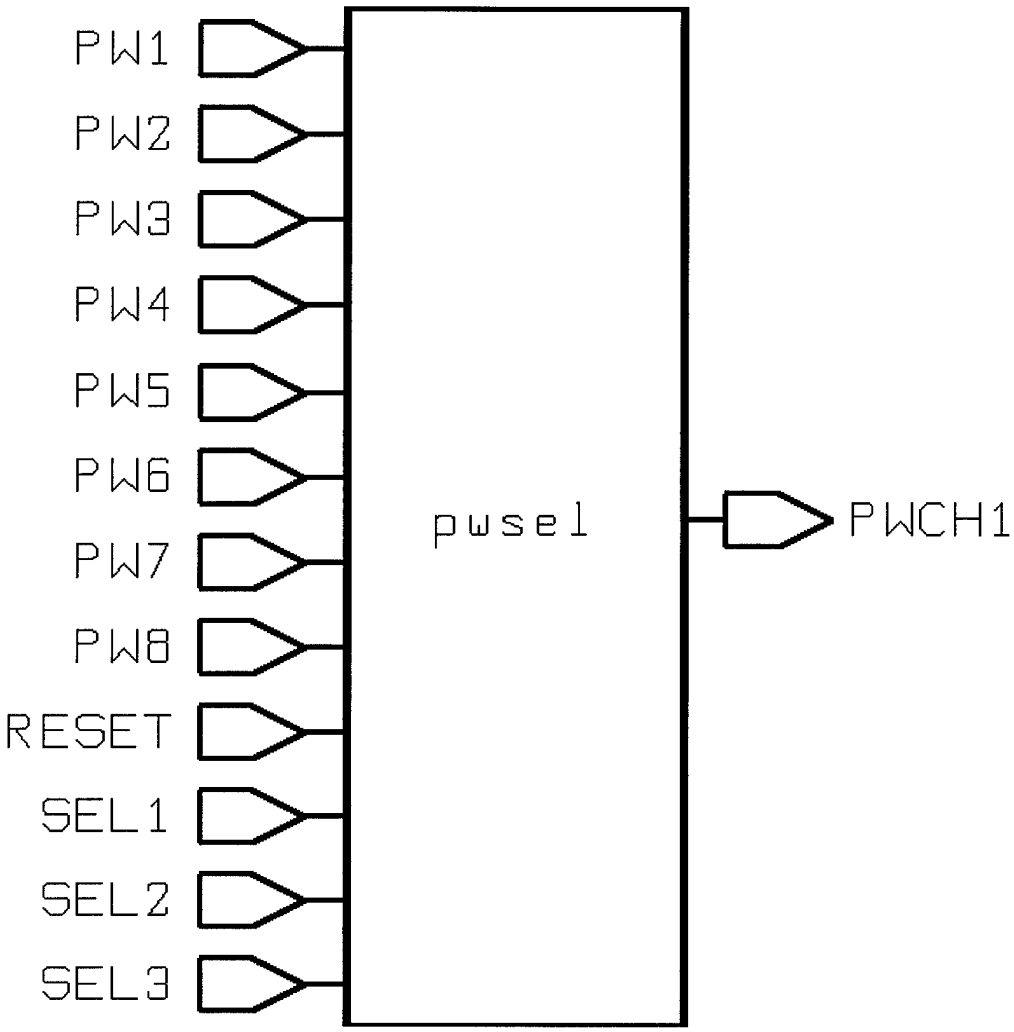


Figure C-8. I/O ports for the pulse width select (PW_SEL) element of the pulse width controller. This element accepts control inputs from the channel select element and selects the proper pulse width from the pulse width generator.

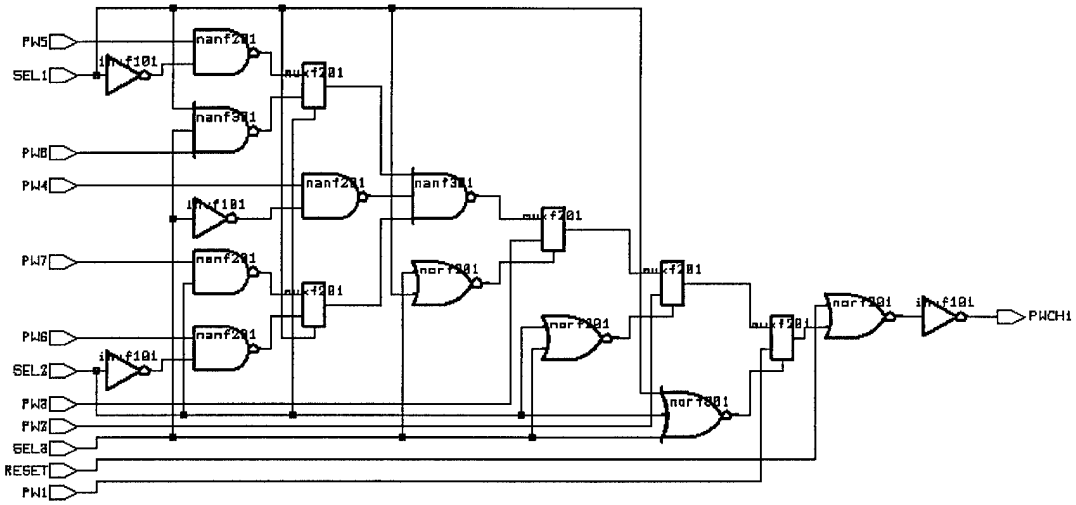


Figure C-9. Schematic of synthesized pulse width select (PW_SEL) element.

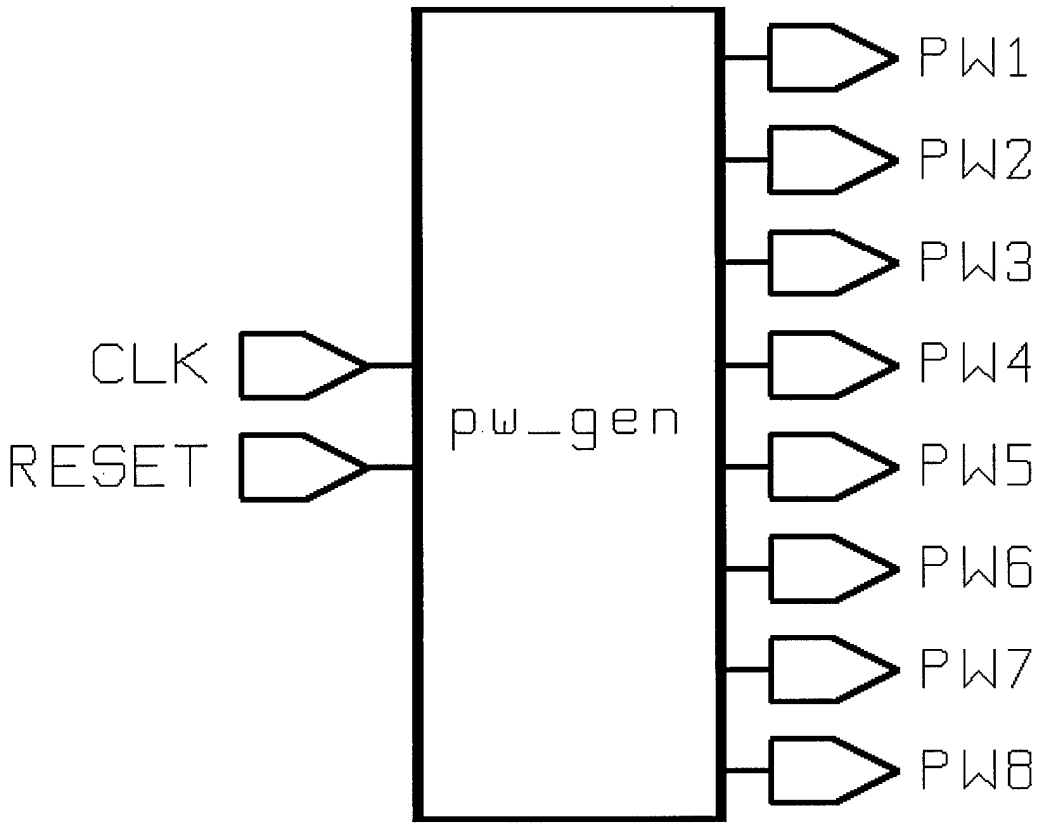


Figure C-10. I/O ports for pulse generator (PW_GEN). This element generates the seven pulse widths.

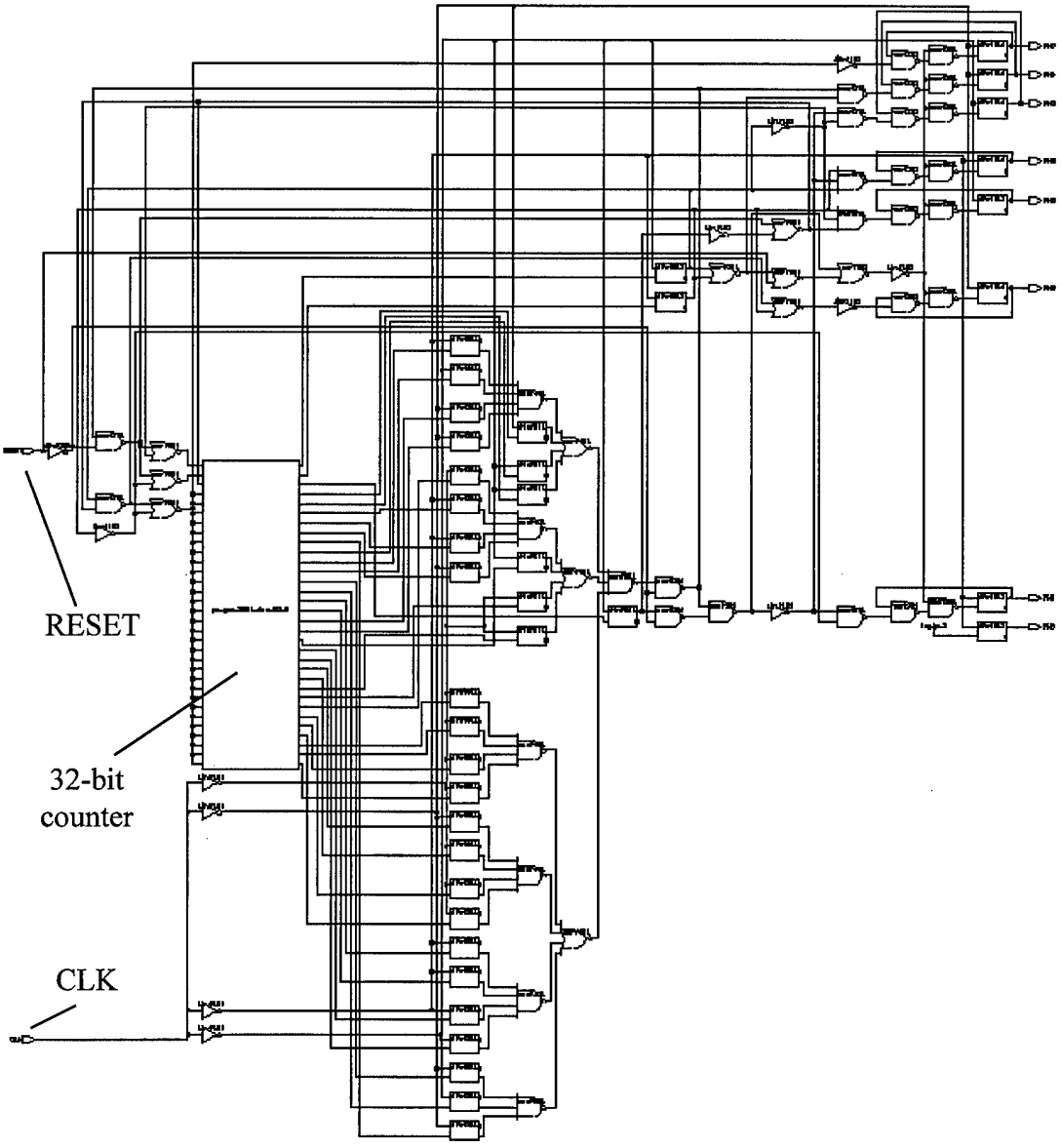


Figure C-11. Schematic of synthesized pulse generator (PW_GEN) element.

Behavioral VHDL code listing used to synthesize pulse width controller and generator:

```
-------------------------------------------------------------------
-- Date:  1 May 97
-- Version:
-- Author:  Capt. Jeff Butler
-- Unix filename:  pwctlr_behave.vhd
--
--  This file is a behavioral description of a pulse width modulation controller
--  for thermally actuated MEMS devices
-------------------------------------------------------------------

library IEEE;
 use IEEE.std_logic_1164.all;

entity PW is

    Port (
          CLK, RESET, LOAD : IN STD_LOGIC := '0';
          CH1, CH2 : IN STD_LOGIC;
          SEL1, SEL2, SEL3 : IN STD_LOGIC;
          PWCH1, PWCH2, PWCH3, PWCH4 : OUT STD_LOGIC );

end PW;

architecture behave of PW is

signal PWCH1_SEL1, PWCH1_SEL2, PWCH1_SEL3: STD_LOGIC;
signal PWCH2_SEL1, PWCH2_SEL2, PWCH2_SEL3:  STD_LOGIC;
signal PWCH3_SEL1, PWCH3_SEL2, PWCH3_SEL3: STD_LOGIC;
signal PWCH4_SEL1, PWCH4_SEL2, PWCH4_SEL3: STD_LOGIC;
signal PW1, PW2, PW3, PW4, PW5, PW6, PW7, PW8: STD_LOGIC;

begin


chan_select : PROCESS

begin -- process begin

wait until (LOAD'event and LOAD='1');
-- IF (LOAD'event and LOAD='1')  then

   if (CH1='0') and (CH2='0') then

   PWCH1_SEL1 <= SEL1;
   PWCH1_SEL2 <= SEL2;
   PWCH1_SEL3 <= SEL3;

   ELSIF  (CH1='0') and (CH2='1') then

   PWCH2_SEL1 <= SEL1;
   PWCH2_SEL2 <= SEL2;
   PWCH2_SEL3 <= SEL3;


   ELSIF  (CH1='1') and (CH2='0') then

   PWCH3_SEL1 <= SEL1;
   PWCH3_SEL2 <= SEL2;
   PWCH3_SEL3 <= SEL3;
```

```
    ELSIF  (CH1='1') and (CH2='1') then

    PWCH4_SEL1 <= SEL1;
    PWCH4_SEL2 <= SEL2;
    PWCH4_SEL3 <= SEL3;

    END if;

-- end if;

end process chan_select;

pwgen : PROCESS

variable COUNTER : integer;

begin -- process begin

PW8 <= '1';

IF RESET = '1' then COUNTER := 0;
end if;

case COUNTER is

   when 0 =>
     PW1 <= '1';
     PW2 <= '1';
     PW3 <= '1';
     PW4 <= '1';
     PW5 <= '1';
     PW6 <= '1';
     PW7 <= '1';


   when 1 =>
     PW1 <= '0';

   when 2 =>
     PW2 <= '0';

   when 3 =>
     PW3 <= '0';

   when 4 =>
     PW4 <= '0';

   when 5 =>
     PW5 <= '0';

   when 6 =>
     PW6 <= '0';

   when 7 =>
     PW7 <= '0';

   when others =>
     COUNTER := 0;

end case;

if counter = 7 then
  COUNTER := 0;
else
 COUNTER := COUNTER + 1;
```

```
end if;

wait until (CLK'event and CLK='1');

END process pwgen;

chan1 : PROCESS (RESET, PWCH1_SEL1, PWCH1_SEL2, PWCH1_SEL3, PW1, PW2, PW3, PW4, PW5, PW6, PW7,
PW8)

begin -- process begin

   -- wait until (LOAD'event and LOAD='1');

IF RESET = '1' THEN
  PWCH1 <= '1';
--  PWCH2 <= '1';
--  PWCH3 <= '1';
--  PWCH4 <= '1';


 ELSIF ( PWCH1_SEL3='0') AND (PWCH1_SEL2='0') AND (PWCH1_SEL1='0') THEN
  PWCH1 <= PW1;

  ELSIF  (PWCH1_SEL3='0') AND (PWCH1_SEL2='0') AND (PWCH1_SEL1='1') THEN
  PWCH1 <= PW2;

  ELSIF  (PWCH1_SEL3='0') AND (PWCH1_SEL2='1') AND (PWCH1_SEL1='0') THEN
  PWCH1 <= PW3;

  ELSIF  (PWCH1_SEL3='0') AND (PWCH1_SEL2='1') AND (PWCH1_SEL1='1') THEN
   PWCH1 <= PW4;

  ELSIF  (PWCH1_SEL3='1') AND (PWCH1_SEL2='0') AND (PWCH1_SEL1='0') THEN
   PWCH1 <= PW5;

  ELSIF  (PWCH1_SEL3='1') AND (PWCH1_SEL2='0') AND (PWCH1_SEL1='1') THEN
  PWCH1 <= PW6;

  ELSIF  (PWCH1_SEL3='1') AND (PWCH1_SEL2='1') AND (PWCH1_SEL1='0') THEN
  PWCH1 <= PW7;

  ELSIF  (PWCH1_SEL3='1') AND (PWCH1_SEL2='1') AND (PWCH1_SEL1='1') THEN
   PWCH1 <= PW8;

END IF;

-- wait until (CLK'event and CLK='1');

 END process chan1;


chan2 : PROCESS (RESET, PWCH2_SEL1, PWCH2_SEL2, PWCH2_SEL3, PW1, PW2, PW3, PW4, PW5, PW6, PW7,
PW8)


begin -- process begin


-- wait until (LOAD'event and LOAD='1');

IF RESET = '1' THEN
  -- PWCH1 <= '1';
    PWCH2 <= '1';
--  PWCH3 <= '1';
--  PWCH4 <= '1';
```

```
  ELSIF ( PWCH2_SEL3='0') AND ( PWCH2_SEL2='0') AND ( PWCH2_SEL1='0') THEN
   PWCH2 <= PW1;

   ELSIF  ( PWCH2_SEL3='0') AND ( PWCH2_SEL2='0') AND ( PWCH2_SEL1='1') THEN
   PWCH2 <= PW2;

   ELSIF  ( PWCH2_SEL3='0') AND ( PWCH2_SEL2='1') AND ( PWCH2_SEL1='0') THEN
   PWCH2 <= PW3;

   ELSIF  ( PWCH2_SEL3='0') AND ( PWCH2_SEL2='1') AND ( PWCH2_SEL1='1') THEN
    PWCH2 <= PW4;

   ELSIF  ( PWCH2_SEL3='1') AND ( PWCH2_SEL2='0') AND ( PWCH2_SEL1='0') THEN
    PWCH2 <= PW5;

   ELSIF  ( PWCH2_SEL3='1') AND ( PWCH2_SEL2='0') AND ( PWCH2_SEL1='1') THEN
   PWCH2 <= PW6;

   ELSIF  ( PWCH2_SEL3='1') AND ( PWCH2_SEL2='1') AND ( PWCH2_SEL1='0') THEN
   PWCH2 <= PW7;

   ELSIF  ( PWCH2_SEL3='1') AND ( PWCH2_SEL2='1') AND ( PWCH2_SEL1='1') THEN
    PWCH2 <= PW8;

END IF;

-- wait until (CLK'event and CLK='1');

 END process chan2;

chan3 : PROCESS (RESET, PWCH3_SEL1, PWCH3_SEL2, PWCH3_SEL3, PW1, PW2, PW3, PW4, PW5, PW6, PW7,
PW8)

begin -- process begin

    -- wait until (LOAD'event and LOAD='1');

IF RESET = '1' THEN
--    PWCH1 <= '1';
--    PWCH2 <= '1';
  PWCH3 <= '1';
--    PWCH4 <= '1';


  ELSIF ( PWCH3_SEL3='0') AND (PWCH3_SEL2='0') AND (PWCH3_SEL1='0') THEN
   PWCH3 <= PW1;

   ELSIF  (PWCH3_SEL3='0') AND (PWCH3_SEL2='0') AND (PWCH3_SEL1='1') THEN
   PWCH3 <= PW2;

   ELSIF  (PWCH3_SEL3='0') AND (PWCH3_SEL2='1') AND (PWCH3_SEL1='0') THEN
   PWCH3 <= PW3;

   ELSIF  (PWCH3_SEL3='0') AND (PWCH3_SEL2='1') AND (PWCH3_SEL1='1') THEN
    PWCH3 <= PW4;

   ELSIF  (PWCH3_SEL3='1') AND (PWCH3_SEL2='0') AND (PWCH3_SEL1='0') THEN
    PWCH3 <= PW5;

   ELSIF  (PWCH3_SEL3='1') AND (PWCH3_SEL2='0') AND (PWCH3_SEL1='1') THEN
   PWCH3 <= PW6;

   ELSIF  (PWCH3_SEL3='1') AND (PWCH3_SEL2='1') AND (PWCH3_SEL1='0') THEN
```

```
   PWCH3 <= PW7;

   ELSIF  (PWCH3_SEL3='1') AND (PWCH3_SEL2='1') AND (PWCH3_SEL1='1') THEN
    PWCH3 <= PW8;

END IF;

-- wait until (CLK'event and CLK='1');

 END process chan3;

chan4 : PROCESS (RESET, PWCH4_SEL1, PWCH4_SEL2, PWCH4_SEL3, PW1, PW2, PW3, PW4, PW5, PW6, PW7,
PW8)

begin -- process begin

-- wait until (LOAD'event and LOAD='1');

IF RESET = '1' THEN
--   PWCH1 <= '1';
--   PWCH2 <= '1';
--   PWCH3 <= '1';
     PWCH4 <= '1';


  ELSIF ( PWCH4_SEL3='0') AND (PWCH4_SEL2='0') AND (PWCH4_SEL1='0') THEN
   PWCH4 <= PW1;

   ELSIF  (PWCH4_SEL3='0') AND (PWCH4_SEL2='0') AND (PWCH4_SEL1='1') THEN
   PWCH4 <= PW2;

   ELSIF  (PWCH4_SEL3='0') AND (PWCH4_SEL2='1') AND (PWCH4_SEL1='0') THEN
   PWCH4 <= PW3;

   ELSIF  (PWCH4_SEL3='0') AND (PWCH4_SEL2='1') AND (PWCH4_SEL1='1') THEN
    PWCH4 <= PW4;

   ELSIF  (PWCH4_SEL3='1') AND (PWCH4_SEL2='0') AND (PWCH4_SEL1='0') THEN
    PWCH4 <= PW5;

   ELSIF  (PWCH4_SEL3='1') AND (PWCH4_SEL2='0') AND (PWCH4_SEL1='1') THEN
   PWCH4 <= PW6;

   ELSIF  (PWCH4_SEL3='1') AND (PWCH4_SEL2='1') AND (PWCH4_SEL1='0') THEN
   PWCH4 <= PW7;

   ELSIF  (PWCH4_SEL3='1') AND (PWCH4_SEL2='1') AND (PWCH4_SEL1='1') THEN
    PWCH4 <= PW8;

END IF;

-- wait until (CLK'event and CLK='1');

 END process chan4;

END behave;
```

Appendix D. Chip-on-Flex (COF)/MEMS Fabrication Process

This appendix contains the process flow sequence for the chip-on-flex (COF)/MEMS process used in Chapter 9. The information on the basic COF process is shown in Table D-1 and was provided by General Electric (GE). The procedure in Table D-1 is used to produce a COF module with two Kapton layers and a single metal interconnect layer. The author was not given permission to publish the specific process parameters (e.g., temperature, time, materials, etc.) on the basic COF procedure as this information is proprietary to General Electric. Specific detail is included in Table D-2 for the author's modifications to the COF process to allow MEMS packaging.

The same laser was used for all of the ablation steps in Tables D-1 and D-2. The laser had the following characteristics: (a) continuous argon laser (350 nm), (b) 9 μm half-power beam width (HPBW), and (c) a 3 μm center-to-center spacing between adjacent laser scans.

Table D-1. Basic COF Process Sequence Flow.

Step	Description	Comments
1	Kapton (1 mil) frame mounting	Prepare bottom layer of overlay
2	Adhesion promote	
3	Apply chip attach adhesive	Ultem used for COF/MEMS
4	Attach chips to overlay	
5	Cure die attach adhesive	
6	Anneal bake adhesive	
7	Adhesion promote	
8	Plaskon molding to create plastic substrate	
9	High pressure water scrub (500 psi)/Propanol rinse	
10	Post Plaskon molding bake anneal	Max temperature 190 ^{o}C
11	High pressure water scrub (500 psi)/Propanol rinse	
12	Laser drill vias	
13	High pressure water scrub (500 psi)/Propanol rinse	
14	RIE via desoot (O_2 or CF_4/O_2)	Plasma etch to clean vias
15	High pressure water scrub (500 psi)/Propanol rinse	
16	Metal deposition (Ti - 200 nm / Cu - 600 nm)	
17	Electroplate Cu - 4 μm	
18	Metal deposition (Ti - 100 nm)	
19	Metal deposition (TiW - 150 nm / Au - 300 nm / TiW 50 nm)	
20	High pressure water scrub (500 psi)/Propanol rinse	
21	Resist spray coating	
22	Laser pattern resist	
23	Develop resist	
24	Etch metal	
25	Strip resist	
26	Propanol rinse	
27	Adhesion promote	
28	Propanol rinse	
29	Apply Silicon-Polyimide (SPI)/Epoxy	
30	Laminate top Kapton layer	
31	High pressure water scrub (500 psi)/Propanol rinse	
32	Laser ablation to expose probe and I/O pads	
33	High pressure water scrub (500 psi)/Propanol rinse	
34	Plasma etch 500 TiW/Desoot pad openings	End of basic COF process

Table D-2. Additional COF Processing for MEMS Packaging.

Process Step	Power (W)	Scan Rate (Hz)	Passes Over Entire Module	Duration (Min.)
1. High Power Bulk Ablation	2	150	3	N/A
2. High pressure water scrub (500 psi)/Propanol rinse				
3. Low Power Bulk Ablation	1	150	5-7	N/A
4. High pressure water scrub (500 psi)/Propanol rinse				
5. Ablation Polish	3	600	6	N/A
6. High pressure water scrub (500 psi)/Propanol rinse				
7. Plasma Etch (CF_4/O_2 @ 1 Torr)	300	N/A	N/A	60-90
8. High pressure water scrub (500 psi)/Propanol rinse				

Appendix E. Publications Related to This Research

Refereed Journal Articles:

1. J. Butler, V. Bright, and J. Comtois, "Multichip module packaging of MEMS," accepted for publication in *Sensors and Actuators*.

2. J. Butler and V. Bright, "Investigation of MEMS packaging Using multichip module foundries," Invited paper to be published in *Sensors and Materials*.

3. J. Butler, V. Bright, R. Saia, and P. Chu, "Adapting multichip module foundries for MEMS packaging," Invited paper to be published in *International Journal of Microelectronics and Electronic Packaging*.

4. V. Bright, J. Butler, W. Cowan, D. Burns, and J. Reid, "Automated assembly of micro-electro-mechanical systems," accepted for publication in *International Journal of Advanced Manufacturing Systems*.

5. J. Reid, V. Bright, and J. Butler, "Automated assembly of flip-up micromirrors," *Sensors and Actuators*, vol. A66, pp. 292-298, April 1998.

6. J. Butler, V. Bright, W. Cowan, "Average power control and positioning of polysilicon thermal actuators," submitted for publication in *Sensors and Actuators*.

Conference Papers:

1. J. Butler, V. Bright, and J. Comtois, "Advanced multichip module packaging of microelectromechanical systems," *Tech. Digest of the 9th International Conference on Solid-State Sensors and Actuators (Transducers '97)*, vol. 1, pp. 261-264, June 1997.

2. J. Butler, V. Bright, and J. Reid, "Scanning and rotating micromirrors using thermal actuators," *Proc. of SPIE*, vol. 3131, *Optical Scanning Systems*, pp. 134-144, July 1997.

3. J. Butler, V. Bright, R. Saia, and J. Comtois, "Extension of high density interconnect multichip module technology for MEMS packaging," *Proc. of SPIE*, vol. 3224, *Micromachined Devices and Components III*, pp. 169-177, September 1997.

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Vita

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13. ABSTRACT *(Maximum 200 words)*

Micro-electro-mechanical systems (MEMS) are a new and rapidly growing field of research. Several advances to the MEMS state of the art were achieved through design and characterization of novel devices. Empirical and theoretical models of polysilicon thermal actuators were developed to understand their behavior. The most extensive investigation of the Multi-User MEMS Processes (MUMPs) polysilicon resistivity was also performed. The first published value for the thermal coefficient of resistivity (TCR) of the MUMPs Poly 1 layer was determined as 1.25 x 10-3 K-1. The sheet resistance of the MUMPs polysilicon layers was found to be dependent on linewidth due to presence or absence of lateral phosphorus diffusion. The functional integration of MEMS with CMOS was demonstrated through the design of automated positioning and assembly systems, and a new power averaging scheme was devised. Packaging of MEMS using foundry multichip modules (MCMs) was shown to be a feasible approach to physical integration of MEMS with microelectronics. MEMS test die were packaged using Micro Module Systems MCM-D and General Electric High Density Interconnect and Chip-on-Flex MCM foundries. Xenon difluoride (XeF2) was found to be an excellent post-packaging etchant for bulk micromachined MEMS. For surface micromachining, hydrofluoric acid (HF) can be used.

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