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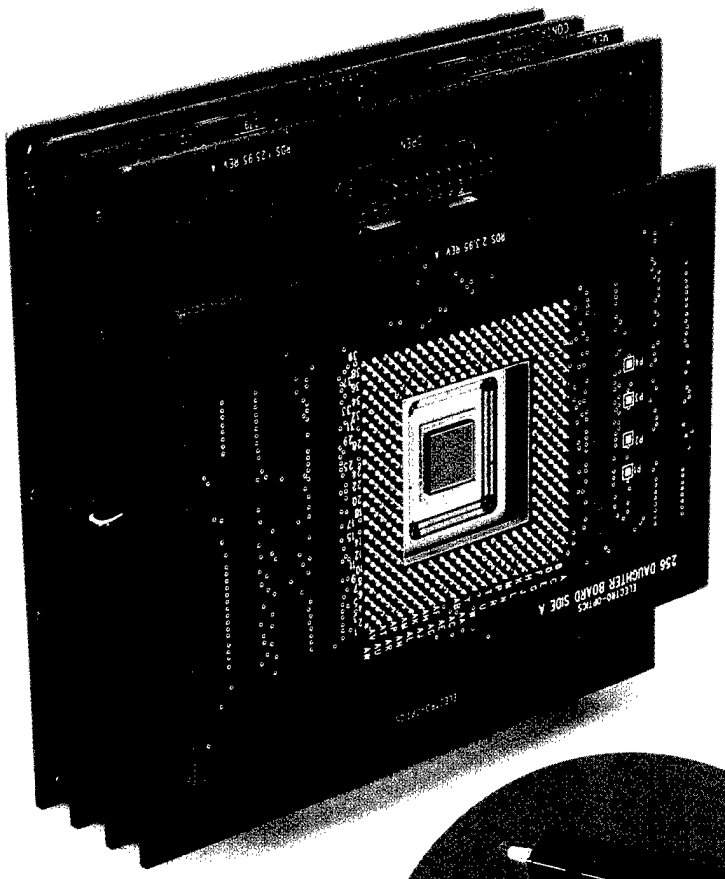
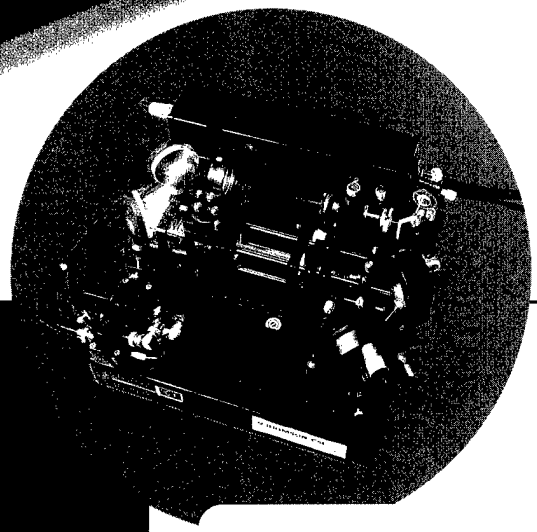


Spatial Light Modulators



Edited by Geoffrey Burdge and Sadik C. Esener

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The OSA topical meetings that received support under this grant provided a forum for reseracners in various specialty areas to meet and share ideas and technology in their fields.

Follcwing are the meetings that were supported by this grant:

--Optics in Computing-- topics for discussion included optical interconnections within electronic computers, system demonstrations of digital optical computing optical neural networks, optical signal processing and novel optical processing architectures, etc.
--Spatial Light Modulators -- this meeting concentrated on material and device research and development, novel system applications and their requirements on SLMs, and on future directions.
--Ultrafast Electronics and Optoelectronics -- this meeting explored the advances in high speed phenomean in the areas of optics, optoelectronics, and electronics.
--Other meetings were in the areas of glass fibers and biomedical optics.

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Volume 14

SPATIAL LIGHT MODULATORS

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Volume 14

SPATIAL LIGHT MODULATORS

Edited by
Geoffrey Burdge and
Sadik C. Esener

From the Topical Meeting
March 17-19, 1997
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Cover art courtesy of J. A. Trezza, Sandia National Labs: Photo of the 256 x 256 SLM chip connected to its interface electronics module. The module allows PC interfacing, data transfer to the SLM at 10 gigabits/second, display of 156,000 frames per second (160ns frame switching) and storage for 1000 frames. (See article on pp. 11-17)
Inset image courtesy of Henri Rajbenbach, Thomson-CSF: An optical correlator. (See article and viewgraphs on pp. 170-196)

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Spatial Light Modulators

Contents

SLM Materials and Sructures

SLM Applications

Preface

Once perceived as expensive gadgets developed for target recognition, spatial light modulators (SLMs) are quickly becoming commodity products for projection and mounted displays. The advent of multimedia and virtual reality, coupled with significant advances made in photonics technology have combined to create a healthy display market. Advances made in the ability to control the alignment process of liquid crystals on CMOS circuits, wide availability of CMOS foundries, and rapid development of micromechanical devices on silicon have enabled this important transition from gadget to product.

As this transition is occurring, computation-oriented photonic markets, including optical correlators, communication switching fabrics, parallel optical storage access, and Free-Space Optical Interconnect Accelerators (FOSIA), are emerging that place additional requirements on SLMs. The insatiable thirst of these applications for speed makes Multiple Quantum Well (MQW) modulators attractive. Consequently, we are witnessing the emergence of ultrafast optical correlators and CMOS/SEED Smart Pixels, the electronically enhanced, functionally more sophisticated cousin of conventional SLMs based on MQW technology. CMOS/SEED smart pixels, using flip-chip bonding of MQW arrays on CMOS, now enable optoelectronic systems to outperform their electronic counterparts. And when coupled with low threshold Vertical Cavity Surface Emitting Laser (VCSEL) arrays, the CMOS/VCSEL smart pixels offer increased speed of parallel optical systems by considerably reducing the cost associated with system assembly. Both CMOS/SEED and CMOS/VCSEL smart pixels are presently integrated using flip-chip bonding of optoelectronic chips with CMOS chips. But newer, potentially more cost-effective and flexible, optoelectronic integration methods, including epitaxial lift-off wafer fusion bonding and fluidic self-assembly techniques, offer to enhance the capabilities of these devices.

This TOPS volume on Spatial Light Modulators brings into focus various SLM fabrication technologies and highlights the present capabilities through papers demonstrating numerous applications from correlators and pattern recognizers to free-space atmospheric turbulence compensators and interconnects. This volume emerged from the OSA-sponsored Spatial Light Modulator Topical Meeting held in Incline Village, Nevada March 17-19, 1997.

The authors of the accepted papers at the topical meeting were invited to submit their papers to this TOPS volume. The submissions were reviewed by referees selected from the technical organizing committee. In addition, paper summaries from the invited speakers have been included, and when available, edited vu-graphs from the invited speakers' presentations were also included. Following a reprint of a recent Optics and Photonics News article introducing SLMs, four major sections VLSI-based SLMs, Integration and Packaging Techniques, SLM Materials and Structures, and SLM Applications comprise a volume that allows the reader instant reference to those papers ranging from SLM design and fabrication to application.

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Reprint

Spatial Light Modulators: Processing Light in Real Time

By Pierre R. Barbier and Garret Moddel

Improvements in spatial light modulators (SLMs) are expanding their applications. Barbier and Moddel describe how SLMs work and provide insight into the latest SLM applications.

Spatial light modulator (SLM) is the inscrutable name for a device that is making its quiet, yet steady entrance into our daily lives. Also called light valves, SLMs are essentially time-varying masks. An example of their function can be seen in an optical crossbar switch. It can be visualized as a bar consisting of a linear array of light emitters, and another bar consisting of a linear array of light detectors crossed with respect to the first one and at some small distance from it. Each emitter illuminates all of the detectors. As described, the crossbar switch does not appear interesting. If we now insert a mask between the emitter array and the detector array, only those parts of the mask that are transmissive will provide a connection between specific emitters and selected detectors. The mask is an SLM. The selected interconnects that have been formed may be reconfigured by changing the pattern on the SLM.

SLMs include a large range of devices whose primary function is to spatially modulate a readout beam. The image can be input either electrically or optically. Electrically addressed spatial light modulators (EASLMs) can be distinguished from optically addressed spatial light modulators (OASLMs). Liquid crystal displays (LCDs) are a type of EASLM, and photographic film and low-light image intensifiers are types of OASLMs (see Fig. 1).

The dividing line between display technology and SLM technology is vague. Generally SLM devices provide higher frame rates or resolution than display devices. In many applications, SLMs must exhibit other properties, such as phase flatness and small size (to be compatible with available optics), which are not required of displays. In this article, we include high performance LCDs as SLMs. Because so many different types of SLMs have been developed over the years, we must limit our discussion to some new SLM technologies that have the potential to provide superior performance over video displays, and to recently developed and new potential SLM applications. Although linear arrays may use the same SLM technology, we will limit this discussion to two-dimensional arrays.[1]

Two prominent display applications of SLMs that are starting to affect our everyday lives are in the entertainment industry. They consist of large screen video projectors[2] and virtual reality, head-mounted displays. Even though these applications were originally developed around the traditional cathodic ray tube (CRT), recent breakthroughs in SLM technology have increased their performance dramatically.

CRT-based video projectors were limited by the brightness of the image formed onto their phosphors and projected onto the screen, restricting the use of these devices to dimly lit rooms. In contrast, in an SLM-based video projector, the image is formed by the SLMs and read out by a high-power lamp or by laser beams before being projected onto a screen. Consequently, much

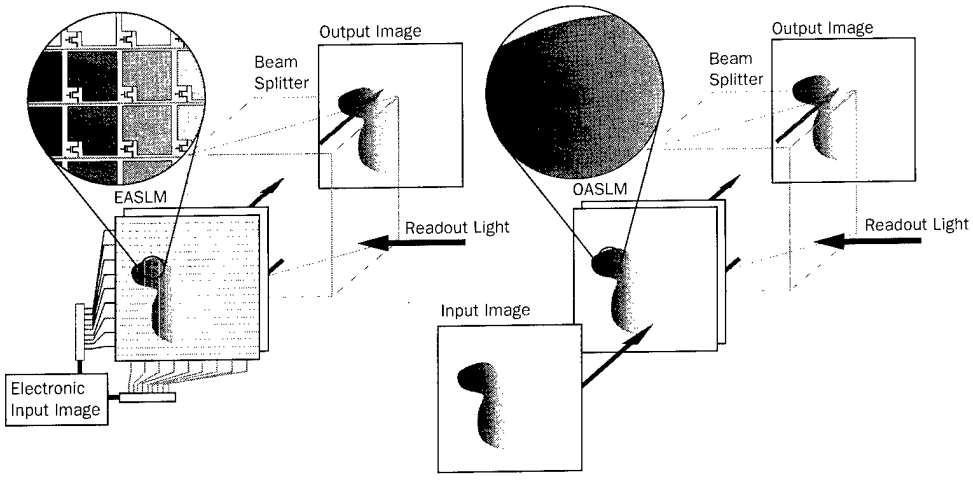

Figure 1. Electrically addressed spatial light modulators (left): individual pixels are addressed electrically. Optically addressed spatial light modulator (right): an input image is sent onto the device, which forms a replica in the modulating medium. Both devices are read out with an external light beam, which is modulated and reflected by (as shown here) or transmitted through the device. Note that OASLMs may also be pixelated.

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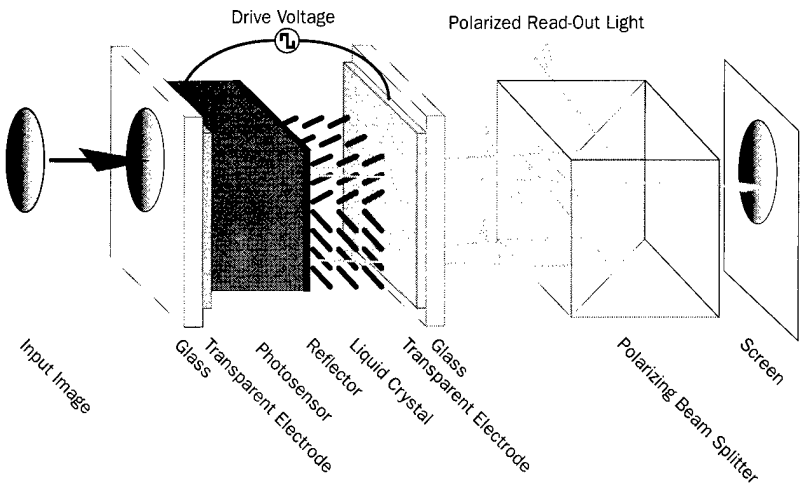


Figure 2. Diagram of the operation of a liquid crystal optically addressed spatial light modulator: the input image is absorbed in the photosensor. The photogenerated charges cause the liquid crystal molecules to rotate, which in turn affects the polarization—in this example—of the polarized readout light. This polarization replica of the input image is transformed into an intensity replica by filtering through a polarizing beam splitter.[3]

brighter and larger images can be projected, and are limited mainly by the intensity of the light source. With current video projectors, images that have a diagonal dimension of a few meters are perfectly visible in a normally illuminated room. Applications of these systems in entertainment include network or traffic-control monitoring rooms. These systems are manufactured by several companies including Ampro Greyhawk Division, Hughes-JVC, In Focus, Sharp, and Texas Instruments.

Head-mounted displays used to be bulky because of the electronics and the high voltages required to control the small CRTs. New liquid crystal SLMs, which are much smaller and require only a few volts, have reduced these constraints considerably, yielding light-weight head-mounted displays that produce a striking stereoscopic effect. Along with applications in 3-D video games, these devices can be used in virtual reality applications. Such devices are manufactured by Kaiser Electro-Optics, Virtual Research Systems, Liquid Image, and so on.

Addressing

The light-modulating medium modifies the readout light using an electro-optic effect. The most practical and common approach to make an EASLM is to apply matrix-addressing electrodes to a substrate. The pixels are formed at the intersection of the electrodes, which modulate the voltage dropped across the sandwiched light-modulating medium. To make it possible to address a large number of rows sequentially, a transistor at each pixel transfers and stores the electrical information for that pixel. Therefore, the addressing of the device can be carried out rapidly while the reading can be done more slowly in the remaining frame period. For example, EASLMs used in head-mounted displays incorporate an integrated circuit (IC) silicon substrate addressing matrix, and a liquid crystal light-modulating medium. The pixel size in these active backplane SLMs is limited to that which can be formed by very large-scale integration (VLSI) IC fabrication. For some coherent optical processing applications, the current state of the art is not sufficiently small. Technical challenges include increasing the maximum number of pixels, frame rate, fill factor (fraction of an area that is optically usable), number of distinct gray levels, and contrast ratio.

In optically addressed active backplane devices, a photodiode, which replaces the control electrode matrix, can be incorporated into each pixel. The optical write-image is directly sensed by the photodiodes and the image is transferred to the modulating layer. Some "smarts" can be built into this OASLM in the electronic circuit between the photodiodes and the pixels, implementing some specific optical image processing functions such as edge detection or human retina simulation. This forms one type of smart pixel SLM.

Often such optical image processing is not necessary, and the substrate can be coated with a uniform film of photosensing material that absorbs the write-image photons and converts them to electron-hole pairs. These carriers locally alter the electric field across the electro-optic material modulating the readout light. The light modulating medium may be adjacent to the photosensor film forming a hybrid OASLM. This is the case in liquid crystal-amorphous silicon OASLMs, represented in Figure 2.[3] Alternatively, a single material can act as both photosensor and light-modulating medium, forming monolithic OASLMs. This is the case in multiple-quantum-well (MQW) self-electro-optic devices (SEEDs) where the effect is two-dimensional,[4] and photorefractive crystals OASLMs that form volume holograms. The resolution of OASLMs can be quite high, above 100 linepairs/mm, limited only by the physical properties of the photosensing and modulating layers. In addition to spatial resolution, performance limitations of these devices include

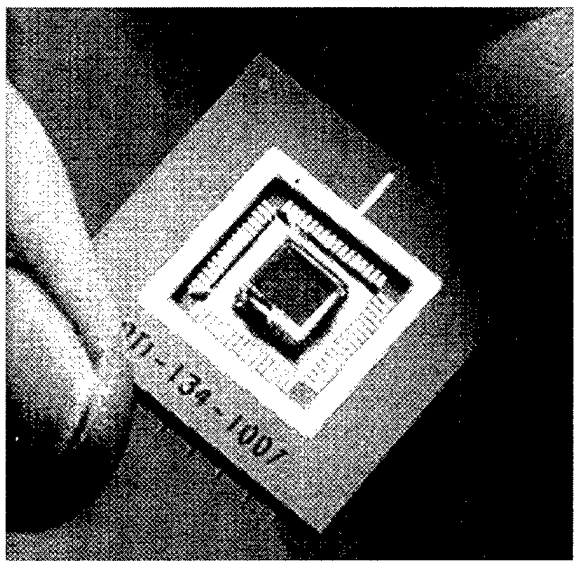


Figure 3. Integrated circuit backplane spatial light modulator incorporating a ferroelectric liquid crystal. The 256 × 256 array of pixels can be driven at frame rates of up to 3 kHz.

response time, contrast ratio, write-light sensitivity, and linearity. (SLM resolution is usually quoted in linepairs per millimeter (lp/mm) and display resolution in lines per millimeter. Therefore, the resolution in linepairs per millimeter of a display used as an SLM is twice that of its resolution expressed in lines per millimeter.)

Glossary

EASLM A spatial light modulator in which a silicon integrated circuit addresses each pixel individually (predominantly implemented with liquid crystal technology).

Extinction ratio The on-to-off ratio of the output light intensity (ideally infinity).

MTF The curve corresponding to the contrast ratio versus the spatial frequency of a periodic one-dimensional pattern expressed in linepairs per millimeter (lp/mm).

Pixel The minimum addressable area as defined by patterning.

OASLM A spatial light modulator in which a silicon VLSI circuit performs an image processing operation and addresses each pixel.

Resolution The spatial frequency expressed in linepairs/millimeter (lp/mm) at which the MTF reaches 50% or 10%, depending on the definition. The inverse of the spatial resolution is equivalent to pixel dimension for an unpatterned OASLM. The spatial resolution is simply the inverse of the pixel dimension divided by two for a patterned SLM.

TFT Transistor fabricated in thin semiconductor films, such as hydrogenated amorphous silicon, to drive the pixels of an active matrix liquid crystal display.

Devices

As shown in Figure 1, the output pattern of an SLM is imposed onto the readout light, which may be a coherent laser beam or an incoherent filtered or unfiltered white light. SLMs may reflect or transmit the readout light, and modulate its intensity, phase, polarization, or angle depending on the light modulating medium. We discuss four types of SLM light modulation approaches: liquid crystal, SEED, digital micromirror device (DMD), and photorefractive crystal. Note that other devices not discussed in this article have been developed, such as the charge-transfer-plate membrane-mirror OASLM, the magneto-optic OASLM, and the Si/PLZT OASLM.

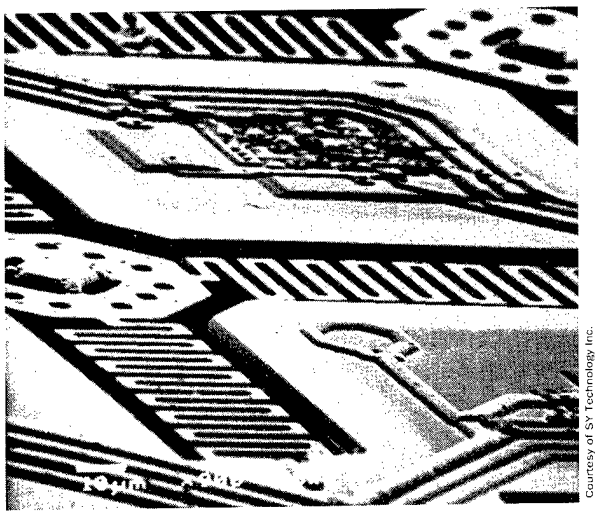
How they work

The application of an electric field across a liquid crystal (LC) film causes the molecules to rotate. The refractive index along the optic axis parallel to the long axis of the liquid crystal is significantly different from the index along a perpendicular short axis. This difference, the birefringence, is quite substantial for liquid crystal molecules, typically about 0.2. By an appropriate choice of the twist of the liquid crystal axis or the thickness of the material, and of the polarization of the readout light, the polarization of the light may be rotated or its phase modulated. Polarization rotation can be converted to intensity modulation by filtering through a polarizer, as is done in most laptop computer screens or in LC SLM-based video projectors (see Fig. 2). Phase modulation can be used for adaptive optics applications or to create thin-film holograms for optical image processing applications. Two main types of liquid crystal materials have been used in SLMs:

- Nematic liquid crystals (NLCs) provide analog response, but are limited by the natural relaxation of the material, to a response time of approximately 10 msec.
- Surface-stabilized ferroelectric liquid crystals (SSFLCs) switch much faster (10 μsec), but are inherently binary in their response.

Both types of material have been incorporated into EASLMs, using IC backplanes to provide the drive circuitry (see Fig. 3), and OASLMs, using thin film photosensors such as hydrogenated amorphous silicon,[3] polycrystalline silicon thin film transistors (TFTs), or crystalline silicon photodiode arrays.[4] LC SLMs were pioneered by Hughes and are now manufactured by several companies, including Hughes-JVC, CRL, Displaytech (see Fig. 3), and Hammamatsu.

Amplitude modulation may be achieved in a SEED through the modulation of the excitonic absorption edge by an electric field (quantum-confined Stark effect) applied across a multiple quantum well (MQW) structure.[5] OASLMs have been formed by depositing



Courtesy of SY Technology Inc.

Figure 4. SEM photograph of a phase-modulating micromirror and its electronic driver. Drive electronics controls the vertical position of the micromirror with an electrostatic field. The silicon micromirror array is micromachined on cantilevers. Using a separate microlenslet array, light is focused onto each micromirror to modulate the phase.

photodiode films on top of the MQWs and by making them semi-insulating. A modified version of this technology is the bonding of a GaAs/AlGaAs MQW chip with photodetectors and modulators onto a VLSI silicon chip to improve switching performance.[6] Because they switch rapidly (on the order of 1 GHz), MQW SLMs are used predominantly in photonic switching such as in the crossbar switch described earlier.

DMDs are fabricated by micromachining a silicon wafer.[7] Tiny (16 μm × 16 μm) suspended mirrors are micromachined on cantilevers. The mirrors are rotated by an electrostatic field to one of two stable positions. The reflection angle modulation is converted into an intensity modulation after spatial filtering through an aperture. DMDs, with 400 × 600 pixels, can be fabricat-

ed with their addressing circuitry into a single chip. Their response time is short (0.3 msec), but they are inherently digital, and require multiplexing to achieve grey levels. Texas Instruments has fabricated and incorporated DMDs into commercial TV projection systems. SY Technology is developing a new generation of micromirrors that can modulate the phase only and could be used in adaptive optics applications (see Fig. 4).

Photorefractive crystals use an effect that results from a local modulation of the index of refraction of the crystal after illumination with a write light.[8] The photorefractive effect can be used for phase conjugation, which is described in the following section. This effect is usually relatively slow (10-100 msec) and requires a single wavelength. To this category belongs the Pockels Readout Optical Modulator (PROM), which uses the longitudinal electro-optic effect and is commonly made from a $Bi_{12}SiO_{20}$ (BSO) crystal, and the Russian PRIZ (a Russian acronym for "image transformer"), which uses the transverse electro-optic effect.

Applications and trends

Video projection

The most apparent applications of SLMs have been in displays. Liquid crystal EASLMs and OASLMs, as well as DMDs, are at the heart of new video projectors. They are used to modulate a bright white light for projection of video or computer images onto a screen. The picture is sent electronically to the EASLMs, or to CRTs that are imaged onto the photosensor of the OASLMs, which then modulate the readout light. Red, green, and blue images must be generated and combined to reconstitute color images. Video projectors are presently limited by the brightness of the readout source and the insertion loss of the light modulating scheme. Refinements may improve this projection efficiency and larger pixel numbers should be soon possible to accommodate high definition television.

Image processing

Correlators aid machine vision and pattern recognition. Specific optical image processing operations necessary in machine-vision applications include image correlation using LC or fast MQW OASLMs at the Fourier plane as an intensity sensor. Image correlation consists of image recognition using Fourier transform processing. This can be achieved in real time by using an OASLM-based image correlator, which may be much faster than processing the images numerically on a desktop computer. Image correlators can be used for pattern recognition such as for finger print identification. With the development of smart pixel OASLMs other specific machine vision applications may be expected.

Image conversion

Optical computing applications also take advantage of SLMs when an incoherent scene needs to be converted in real time to a coherent monochromatic image. This is done using LC OASLMs, or MQW OASLMs. Other applications include wavelength conversion where a visible scene is converted into an infrared image for simulation purposes, and conversely, for image amplification.

Interconnects

EASLMs may be applied to optical interconnects where it is necessary to rapidly interconnect a matrix of different processors to one another. This can be done by using a crossbar switch described in the introduction incorporating a fast MQW SLM. The SLM acts as a switch matrix that rapidly controls the interconnection between the outputs and inputs of all the processors.[6]

Phase conjugation

Phase conjugation can be accomplished using OASLMs, such as photorefractive crystals and liquid crystal/amorphous silicon devices. In phase conjugation, the exact complex conjugate of a laser beam is redirected precisely along the incoming path. A plane wavefront that passes through a distorting medium will return as an unaberrated plane wave after reflection from the phase conjugate mirror and propagation through the same medium. Applications for this include imaging or laser beam propagation through a turbulent medium such as the atmosphere.[10]

Optical compensation

Photorefractives have found applications as optical compensators where there is a need to clean up a laser beam that is distorted by a mechanism whose characteristic time is slower than the photorefractive effect. The Hughes Compensated Laser Ultrasonic Evaluation (CLUE) system employs a $BaTiO_3$ (barium titanate) crystal double-phase conjugate mirror to clean up the spatial information of a laser beam reflected and distorted from the rough surface of a metal part.[11] The metal part is excited by ultrasound vibrations and modulates the phase of the reflected laser beam. The double-phase conjugate mirror transfers the energy of the distorted reflected beam to a clean reference beam. The ultrasonic response of the part is recovered by heterodyne detection of the cleaned beam and recorded. After raster-scanning a welded metal part, an image of the quality of the weld joint can be obtained in the industrial environment.

Adaptive optics

Phase-modulation EASLMs can be used in adaptive optics to compensate for phase distortions of an arriving light wavefront after propagation through a distorting medium.[9, 10] This can be used for imaging through the atmosphere in astronomical or terrestrial applications or to precompensate a laser beam before sending it through the atmosphere and achieve diffraction-limited performance, *i.e.*, the smallest possible spot size.

Turbulence simulation

Finally, an unusual application of SLMs that was developed at the Army Research Lab is in an atmospheric turbulence simulator.[12] This system uses EASLMs and OASLMs in a close-loop configuration. By adjusting the characteristics of the input phase screen generated by

the EASLM, the system can be set to a chaotic behavior with characteristics similar to atmospheric turbulence.

Future developments

In addition to previously mentioned applications, the next few years will see other emerging applications made feasible by the appearance of new material systems. In particular, for some photorefractive applications, photopolymers will be more practical than photorefractive crystals, and biological material, in particular bacteriorhodopsin, may also be used to form practical OASLMs.

The commercially driven applications that are more likely to make an immediate entrance are machine vision applications, optical correlators for pattern recognition in machine vision and security applications, and the use of SLMs as page formatters in holographic storage. With improvements in OASLMs, there may be wider application of SLMs in adaptive optics and in optical crossbar switches. Finally, like other technologies, SLM technology might exceed our current expectations with regard to potential applications.

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VLSI-based SLMs

Optoelectronic/VLSI

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A great goal of optics in computing is the eventual failure of electrical interconnects. This leads to two guiding principles for smart pixel technologies, which integrate optoelectronic devices to electronics for optical read-in/out. One, that the electronics be state-of-the-art, or, in other words, not compromised by the integration with optoelectronics, since the above stated goal will be reached sooner with leading edge electronics. Two, since a probable failure mode of electrical interconnects is a limitation of electrical chip pin-out, the number of optical channels per chip must be in the thousands, since it is apparently not until this number is reached that there will be a problem. Therefore, any integration process must be capable of producing such numbers of optoelectronic devices, preferably in a single step. Also, since currently only MQW modulators are available in arrays this large, that is what we use for the transmitting device. It is convenient that the MQW modulator also functions as a detector, but as described below we also have the capability of multiple levels of integration for dissimilar input and output devices.

The only integration technique that suffices both of the preceding criteria is flip-chip bonding, since it is a low temperature process and attaches many devices at once. We have shown that thousands of solder pads can be produced on chips by photolithography and evaporation. Using our commercial bonding machine, manufactured by Research Devices in Piscataway, New Jersey, aligning an optoelectronic chip laterally to a Si CMOS chip can be routinely performed to 2 micron accuracy. Thus attaching thousands of high speed devices in a single step is routine. The temperatures involved are below 200 ^{o}C. and so do not affect the Si electronics.

We have innovated on the process of flip-chip bonding, particularly for optoelectronics devices. The need for this is because the best MQW modulators operate at a wavelength of 850 nm [K.W. Goossen, M.B. Santos, J.E. Cunningham and W.Y. Jan, IEEE Photon. Tech. Lett. **5**, 1392 (1993)]. However, the GaAs substrate of such modulators is opaque at that wavelength. Therefore, we remove it after the bonding [K.W. Goossen, J.E. Cunningham and W.Y. Jan, IEEE Photon. Tech. Lett. **5**, 776 (1993)]. This optoelectronic/VLSI process arranges so that both the n and p contacts of the diodes are brought to the surface and are coplanar, and defines each device so that it is electrically isolated from its neighbors. Solder is deposited on one or both of the Si and GaAs chips, and the chips are bonded together. We find that gold-coated tin works well as a solder and good bonding occurs by tacking the chips together at an elevated temperature and pressure without the need for reflow. Then epoxy is wicked between the chips by capillary action. The epoxy both provides mechanical stability, and protects the front surfaces of the chips during the next step, which is the removal of the GaAs substrate. This is done by chemical etching. The etch is stopped by a stop-etch layer which has been placed between the GaAs substrate and the device layers. The epoxy may subsequently be removed if necessary, e.g., to expose wire-bond pads. We demonstrated arrays of bonded modulators and simple circuits in [K.W. Goossen, J.A. Walker, L.A. D'Asaro, S.P. Hui, B. Tseng, R. Leibenguth, D. Kossives, D.D. Bacon, D. Dahringer, L.M.F. Chirovsky, A.L. Lentine and D.A.B. Miller, IEEE Photon. Tech. Lett. **7**, 360 (1995)]. Our largest chips to date are 7x7 mm Si chips with 140000-450000 CMOS gates with a 64x68 array of modulators arranged in a 5.5x5.5 mm field. We have produced such chips with 100 % modulator yield, but typically have about 5 nonworking diodes, with the yield reduction mostly due to defects in the modulators. Thus for these larger chips our device yield is about 99.9 %.

That our circuits are not compromised by the optoelectronic integration is demonstrated since they have been designed with standard modeling tools and work accordingly. We have shown switching circuits in 0.8 μm CMOS operating with clocks of 700 Mbit/sec [A.L. Lentine, K.W. Goossen, J.A. Walker, L.M.F. Chirovsky, L.A. D'Asaro, S.P. Hui, B.T. Tseng, R. Leibenguth, D. Kossives, D. Dahringer, D. Bacon, T. Woodward, and D.A.B. Miller, IEEE Photon. Tech. Lett. **8**, 221 (1996)].

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An important advance of the hybrid CMOS-SEED process was demonstrated in [A. Krishnamoorthy, A.L. Lentine, K.W. Goossen, J.A. Walker, T.K. Woodward, J.E. Ford, G.F. Aplin, L.A. D'Asaro, S.P. Hui, B. Tseng, R. Leibenguth, D. Kossives, D. Dahringer, L.M.F. Chirovsky, and D.A.B. Miller, IEEE Photon. Tech. Lett. 7, 1288 (1995)]. Here it was shown that the modulators may be bonded to metal interconnect layers on the Si chip directly above transistor layers, creating a three-dimensional optoelectronic/VLSI circuit. Typically CMOS has three levels of metal, so the modulators may be bonded to the top level. Thus our modulators form an optoelectronic overlay to the electronics, and in a sense, our mission is complete of being able to provide optical I/O to Si CMOS without compromising in any way its ability to form circuits. Using this technique we can make chips with dense modulator arrays. Our densest chips have 32x64 modulators arranged in a 2.3x2.3 mm field. We routinely have only one or zero bad diodes in these dense chips, for a yield > 99.95 %.

The limits of yield will ultimately be determined by defects in the optoelectronic semiconductor. Yield limits such as missing solder bumps or photolithographic errors on the optoelectronic array can be screened fairly easily since they are regular arrays. Screening at this point is highly desirable since no work has been performed except the preparation of the chips which can be done on a wafer basis. In our rudimentary processing environment chips that are perfect in this sense appear possible with 100000 diodes, in a yield of at least one chip per two inch wafer. In a well-controlled processing environment higher yields in this sense would certainly be achieved. In terms of the flip-chip bonding itself, it appears that if uniform bonding occurs over the area of the chip, and all metalizations are present, no errors occur in the bonds. The substrate removal is a step that only produces errors when a gross mistake is made such as the epoxy not filling the space between the chips uniformly. Errors due to substrate removal for *single* chip bonding (see discussion below regarding our foundry runs) can be characterized on a per area basis of approximately 2 bad diodes per square centimeter.

This leaves defects in the optoelectronic semiconductor itself, which are of two types. The first is literally "dirt", large (~1-10 micron) particles which are incorporated into the epitaxial layers during growth. These appear to occur on the order of $10/cm^2$, but tend to be localized so their effective yield reduction is on the order of $1/cm^2$. These particles are almost always fatal to a device. They are easily visible after the substrate has been removed. Finally, there are microscopic defects. The number of these is usually quoted at 100-1000 cm^2, but based on our densest array, described above, which has very little space between the diodes, the sensitivity of modulators to these defects is only on the order of $<1/(2.3x2.3$ mm), or $<19/cm^2$. So our current yield limit is approximately 10-20 defects/cm^2, mostly due to microscopic defects. It is probably reasonable to assume that we could cut this number in half with sufficient research, and make projections based on a defect density of $7.5/cm^2$. This means that a dense array of 3.7x3.7 mm can be made perfect with reasonable yield.

Now we project how many diodes we can fit into a 3.7x3.7 mm area to determine ultimate array size. Our current alignment accuracy is <2 microns, so it is reasonable to assume that solder bumps of 5 microns on a side can be used in the future. Simply scaling our current device design from our dense chip results then in chips with 47,700 diodes. Scaling device area smaller than this may be beyond the capability of optics to handle.

Removal of the substrate has other positive qualities. We have performed process runs where multiple chip designs are aggregated onto a single Si chip, then a modulator array encompassing this entire large chip is processed, and after substrate removal, can be sawed into the individual chips. This is the basis for our continuing workshop runs when in a manner like a foundry, we aggregate smaller designs into larger chips to reduce our workload. Our Lucent/George Mason U. workshop consisted of 16 2x2 mm CMOS circuit designs aggregated onto a single 8x8 mm Si chip. Each of the 16 subchips has a 10x20 array of MQW modulators bonded onto it. The diode attachment area of these chips was 7.8x7.8 mm.

Although the problems of bonding and removing the substrate of such large chips were solved, another unexpected problem specific to the foundry chip remains. That is, that due to the geometry involved, voids are left in the epoxy. Since the foundry chips contained lanes of wire-bonding area

separated by modulator fields, the epoxy may wick in faster or slower along certain paths, creating the opportunity for air to be trapped. We are working on this issue. The ability to do batch processing is not only useful for our foundry runs but also illustrates how this technology may be manufactured in a cost-effective manner.

Another useful aspect of substrate removal is that after the substrate is removed, further chips may be bonded. In particular, since the modulators may be pixilated leaving spaces between them on the chip, we may bond another chip in the same area as the first chip and produce interleaved devices. Thus dissimilar devices, either separately optimized detectors and modulators, or detectors and lasers, may be collocated on the Si chip. We have demonstrated this procedure [K.W. Goossen, et al, to be published].

In conclusion, we have produced a technology for placing thousands of surface-normal input and output optoelectronic devices onto VLSI circuitry. We have demonstrated circuit clock speeds near 1 Gbit/sec and chips with thousands of optoelectronic devices. Thus we have the capability of having aggregate data flows of greater than 1 terabit/chip.

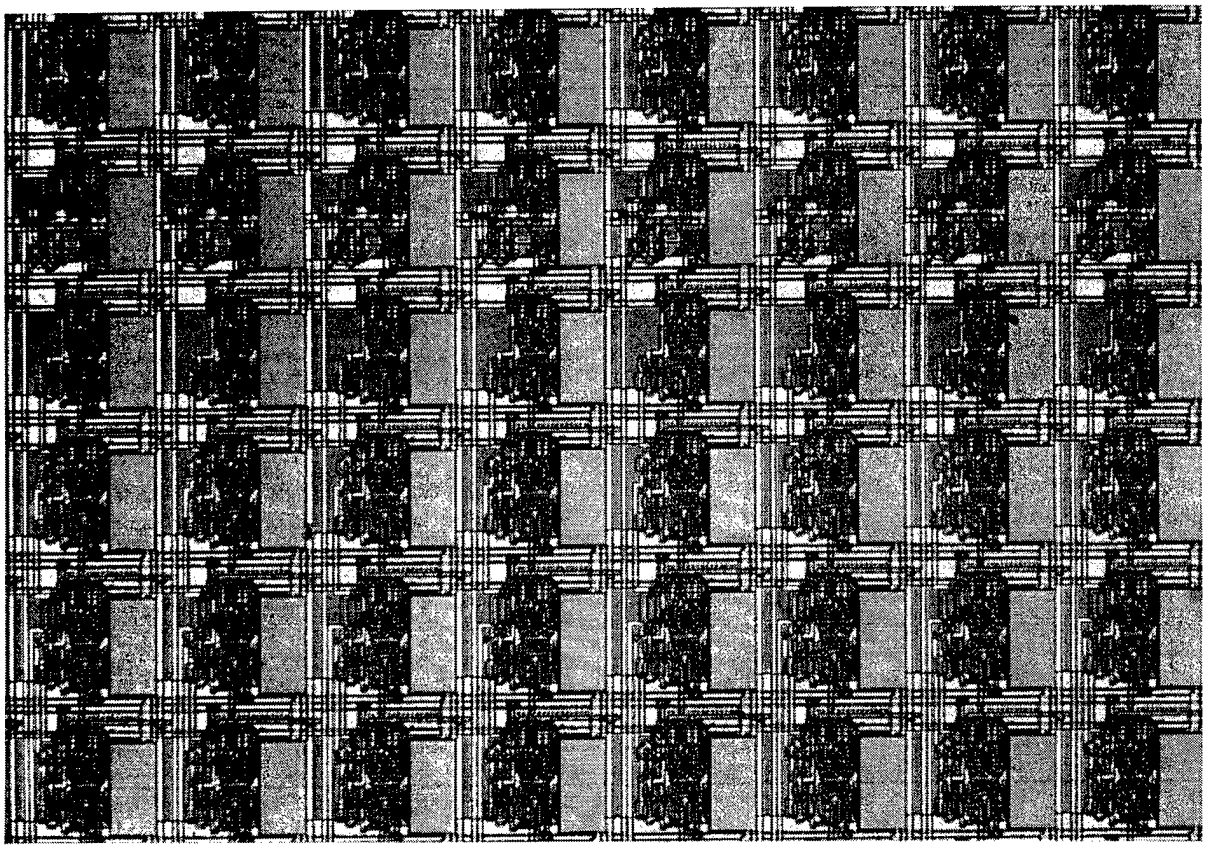

Fig. 1: Typical section of our optoelectronic/VLSI chips, showing ~ 17x50 μm rectangular isolated modulators above CMOS. Each modulator consists of 15x15 μm n and p contacts spaced by 15 μm. The n contact is the active area and functions as the mirror for reflective modulation.

Large Format GaAs Based Spatial Light Modulators and Their use in Optical Correlation Applications

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Abstract

Spatial light modulators using GaAs asymmetric Fabry-Perot vertical cavity modulators have been demonstrated in large format devices. The experimental devices have been extensively characterized. Simulations have been performed which examine both single pixel and array responses. Arrays with improved dynamic range and reduced operating voltages have been designed. The experimental devices have been used to perform optical correlation as well as other system applications. Additional uses for the pixels include detection, phase modulation, directional modulation, and light-emitting capability. Our latest designs allow high-speed gray-scale array implementation.

Key Words
Spatial Light Modulators
Quantum Well Devices
Electro-optical Devices
Optoelectronics

Introduction

Spatial light modulators (SLMs) are the key component for real-time electro-optical signal processing, computing, optical memory storage, free-space optical interconnect, information processing, laser printing, and data conversion systems. We have used a proprietary process to develop the world's largest format, highest performance, close pixel (>90% fill factor) GaAs quantum-well vertical cavity SLM arrays bump-bonded to silicon CMOS. The SLMs consist of a pixelated GaAs optical chip which is flip-chip indium bump-bonded to a Si driver chip, forming an integrated hybrid module. Each optical pixel receives independent data directly from the supporting pixelated driver chip, enabling display properties to change at any moment. Our flip-chip bonding technology has been used to connect pixelated GaAs devices to silicon drivers on chips over 2 square centimeters in size; which contain as many as 300,000 pixels with pixel yields of 99.98%.

We have used our SLM technology to develop several optical processing and data routing demonstration units, including beam steering units and optical correlators. Using interconnected SLM modules, correlations can be performed at a maximum rate of 1,200,000 128 x 128 binary two dimensional (2-D) correlations per second.

Vertical Cavity Modulators

The optical portion of the SLM consists an array of vertical cavity modulator structures. These structures incorporate quantum wells in the cavity region of what forms an optical Fabry-Perot cavity. Electrically, the device is constructed as a p-i-n diode; 100Å GaAs/ 50Å AlGaAs quantum wells reside in the intrinsic region of this diode. The cavity employs top mirrors composed of quarter wave dielectric stacks and bottom mirrors which are either purely metallic or a combination of metallic and dielectric mirrors. If the diode is forward biased, current is injected into the quantum wells and the device emits light--i.e. it acts as an LED. Figure 1 displays a 128 x 128 SLM operating in an LED mode at 860nm. Conversely, by reverse biasing the diode, the quantum well exciton absorptive and dispersive properties are altered at the Fabry-Perot resonance wavelength. This allows modulation and/or detection.

In devices which use single, independent quantum wells, changes in absorption and dispersion with reverse bias are mediated by the *quantum confined Stark effect.*[1] In more complicated quantum well structures, o*scillator strength modulation* [2] can be used. The latter is particularly useful for modulation below 3 volts.

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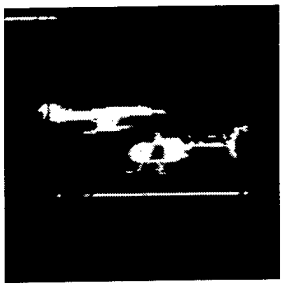

Figure 1. 128 x 128 SLM operating in LED mode (no incident laser light is present).

As the quantum well changes its absorption/dispersion with bias, the modulators alter their reflected intensity, their reflected transmission, and/or their reflected phase. Devices which switch only reflected phases [3] are extremely useful for beamsteering applications[4,5]. Pixels which switch from primarily reflective to primarily transmissive absorb very little light in either state. Such pixels (which are a subset of so called X-modulators) provide the lowest power, highest speed optoelectronic switching elements available[6]. The simplest and most widely used types of pixels, however, are ones that alter between highly reflective and highly absorptive states. Such pixels can simultaneously act as intensity modulators and as detectors--making them ideal pixels for optical transcievers as only one type of optical element need be used. Since the major economic bottleneck for optoelectronic systems which use hybridized GaAs and silicon wafers is the labor cost of bump bonding individual chips together and packaging the final chips with high yield. Such a combination device is extremely attractive as only one hybridization step is necessary. This advantage is potentially enhanced when the optical pixels can also be used as light emitting (LED) pixels.

This combination pixel--one that with one structure can act as either modulator, detector, or LED-- is the one we have chosen to integrate with silicon CMOS to create large pixelated SLM arrays. The properties of each pixel at any given time are determined by the data sent to a CMOS driver chip.

The GaAs modulators are currently operated at wavelengths of either 855 or 860 nm (or both) with single pixel reflectivity changes from $0.43e^{0.7i}$ to $0.03e^{2.2i}$ at 860 nm and $0.4e^{0.2i}$ to $0.04e^{0.3i}$ at 855 nm (thus our contrast ratio is 10:1). The optical chips operate optimally with a 9-V applied bias. Defect-free 256 x 256 arrays draw a total of about 3 mA. In arrays with two or three 'bad' pixels these pixels typically draw the majority of device current; this creates arrays with total current draw of 30 mA. (which still corresponds to far less than 1 microamp per pixel). In our typical devices, modulation occurs *before the matching condition*, meaning that with zero applied bias, each pixel exhibits maximum reflectivity. [7]

GaAs SLM Technology

The GaAs optical and silicon driver chips are combined by placing indium bumps on the chips and then using these bumps as points of contact to both electrically and mechanically connect these chips. The hybrid chip is then sealed for further mechanical stability, wirebonded into a standard IC package, and epoxy potted to form a robust product.

Pixelated, GaAs based spatial light modulators have been made by Lockheed-Martin for several years in both 1-D and 2-D formats[8]. Recently, 2-D SLMs with as large as 256 x 256 close packed pixels (>90% fill factor) have been created and demonstrated at Sanders. These devices have maximum allowable input data rates of 10 gigabits/sec and maximum frame rates (all pixels updated) of 312,500 frames/sec using the current 40 MHz capable silicon drivers. Turn on and turn off times for the array are approximately 200ns. The CMOS driver circuitry for these 2-D devices allows one of two voltages to be placed on each pixel at any particular time. Thus these devices fundamentally operate in a binary (black and white) mode. With speeds of over 312,500 frames/second, however, gray-scale operation can be obtained by time-slicing a frame into various time segments. For example, by switching at our maximum frame rate, 8 bit gray scale (256 level) frames can be produced at rates of 1,220 frames/second (1,220 = 312,500 / 256). We note that the optical pixels themselves are capable of speeds on the order of 10's of Gigahertz (limited by RC charging times) while the underlying physical mechanism of the optical modulation occurs on time scales of picoseconds[9]. Thus current SLM speeds are CMOS speed limited; as CMOS technology improves, the GaAs chips will be able to easily accommodate these speed improvements.

Figure 2. SLM operating in time-sliced Gray scale mode

Nevertheless, time slicing is not the only method we employ to achieve gray scale operation. One-dimensional (1-D) SLMs, with a maximum of 2048 pixels have been created. These SLMs have been made with digital-to-analog (D/A) converters located on the input of each pixel. To date, all of the 1-D SLMs created and demonstrated are

capable of 6 bits of gray scale on each pixel. By integrating D/A converters to produce gray scale, instead of using time slicing, frame rates can be substantially higher. This is clear since the volume of data required for each pixel per frame is $\log_2 N$ instead of N, where 'N' is the number of gray scale levels available. Because the devices are CMOS limited, by requiring less data to be loaded, frame rates can be higher.

Device pixel pitch is currently 40 microns for the 2-D devices (38 microns pixel width) and 8 microns (6 micron width) for our 1x2048 1-D devices. Fig. 3 shows an integrated 2-D SLM package, close up of the optical chip, and a photo of the module displaying data.

Within the SLM, the electronic driver chip consists of a custom, "mixed signal" silicon ASIC. In the 2-D devices, all of the relevant drive circuitry for an individual pixel is located in the CMOS chip below that pixel. In the 1-D arrays, the driver and relevant D/A circuitry are located both below and beyond the edges of the optical part of the chip.

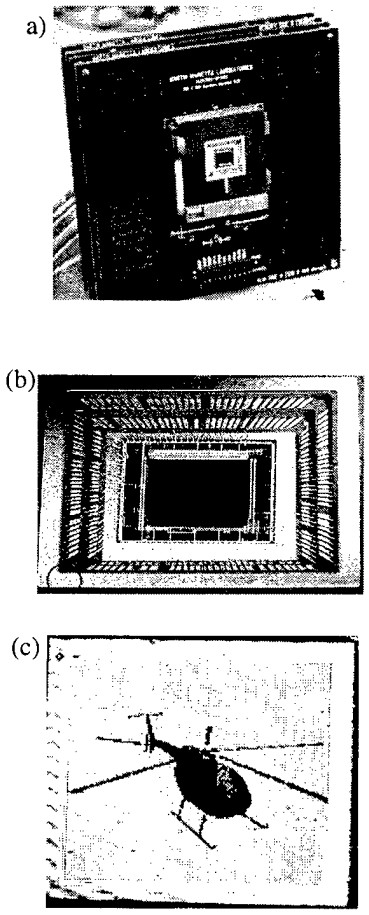

Figure 3. 2-D SLM (a) hybridized/packaged module on circuit board with integrated PC interface and on-board memory. (b) Close up of bump-bonded chip, and (c) infrared image (860 nm) of SLM operation.

SLM Design

Extensive simulations have been used to improve SLM designs. As shown in Fig. 4, the baseline experimental chips have a maximum change in reflectivity of around 40%. However, with improved quantum well and Fabry-Perot cavity design in our next generation arrays, we can easily achieve large arrays with near 70% reflectivity change. At the same time, we can reduce voltages from 9 to 3.3 V. Single pixels have been experimentally demonstrated with reflectivity changes over 90%, contrast ratios over 100 (where contrast ratio is defined as R_{on}/R_{off}), and applied bias of 3 volts.

The simulation software takes into account the complex refractive index (absorption and dispersion) of all epitaxial layers. In addition, it uses semi-empirical models to incorporate the complex refractive index of quantum-well excitons in the simulation. This program has been routinely used to design and accurately predict performance to within 1%. In addition to reflectivity changes, we have been using the simulation tools to predict phase behavior of our devices. Such phase distortions during operation can have significant, adverse effects on coherent light optical signal processors such as correlators.

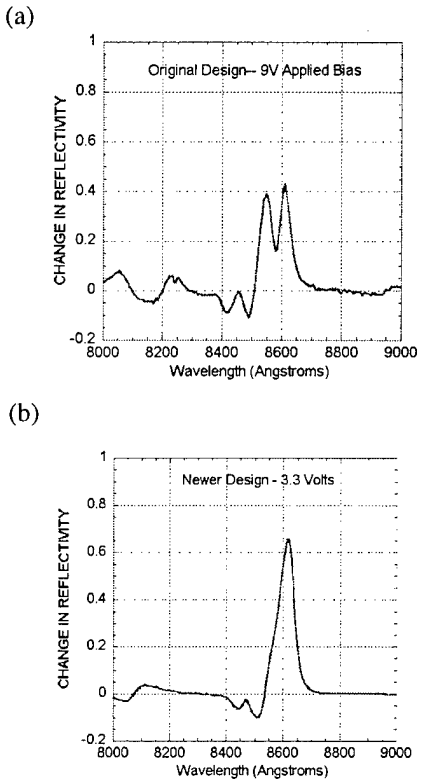

Figure 4. Change in reflectivity vs. wavelength for (a) current experimental and (b) simulated improved array.

In general, GaAs based SLM design must account for operating voltage, optical bandwidth, maximum on-state reflectivity, optical contrast ratio, and optical bandwidth (wavelength range over which modulation is achieved). By using our simulations, parameter space plots can be made for designs that use our various processing techniques. In this way, tradeoffs in device operation can be made when choosing a modulator design for a particular application. Fig. 5a shows a parameter space plot for a variety of modulator designs; all of which have a contrast ratio (on state reflectivity/off state reflectivity) of 10 or better. The plot then shows the different designs that could be accomplished--giving the tradeoffs in maximum on-state reflectivity and optical bandwidths for various required operating voltages. For example, this plot shows that using the 'standard' processing technique and 100 angstrom quantum wells at 860nm, a modulator could be made which require 5 volts to operate and which would provide a contrast ratio of 10, a maximum reflectivity of 50% and an optical bandwidth of 5.6nm. Note that performance beyond that shown in these plots is possible with further design refinement. Recall that single pixel devices with reflectivity changes greater than 90% have been achieved[10].

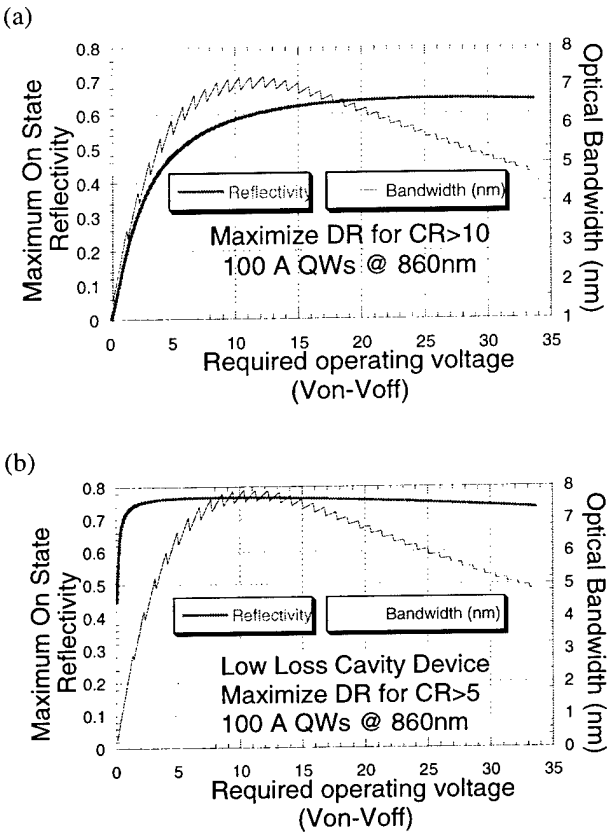

Figure 5. Paramter space plot for devices with (a) contrast ratios > 10 and (b) slightly modified cavity and contrast ratios > 5

Correlation, Modeling, and Relevant Setups

To create a multi-SLM-based optical processor, we have developed modular external printed circuit board (PCB) control hardware that interfaces the SLMs to host computers for data input and control. This integrated module allows multiple SLMs to operate in system-level configurations. In such a setup, the master module provides the clock and control signals to the slave modules. This synchronizes the data loading of multiple SLMs and allows maximum integration time. The external control modules have sufficient on-board static random access memory (SRAM) for storing up to 1000 filter images. Once data are loaded locally into the module, through a PC for example, computer connections can be removed and the module can run and display SLM data independently. A picture of the experimental and a schematic of the correlator setup is shown in Fig. 6.

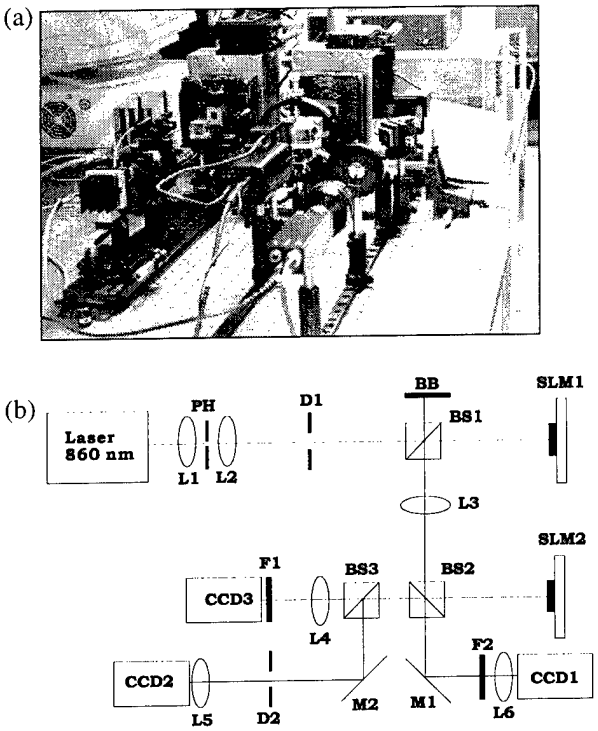

Figure 6 (a) Photo and (b) schematic of Sanders dual SLM based 4F optical correlator.

In the 4F correlator setup, two modules are used. By placing input images on one SLM (SLM1) and Fourier filters (of reference images) on a second SLM (SLM2), we can perform filtering and correlations at our high frame rates. The input images from SLM1 are Fourier transformed by a positive lens (L3), and the reference images from SLM2 are placed at the focal plane of the lens L3. The inverse Fourier transforms of the products of

these two images (Fourier transformed image and reference image) are performed by a positive lens (L4) and captured by a camera (CCD3). The cameras, CCD1 and CCD2, display the images of SLM1 and SLM2, respectively.

High-speed correlation has been performed using either two 128 x 128 SLMs (which permits 300,000 128 x 128 correlations per second). By using one 256 x 256 image plane SLM (with four 128 x 128 images on it) and one 128 x 128 filter plane SLM, a maximum speed of 1,200,000 128 x 128 correlations per second is achievable. We note that the inherent switching speed of each pixel is in the gigahertz range. Thus, with further evolution in control electronics, we can accommodate several orders of magnitude increases in data rates.

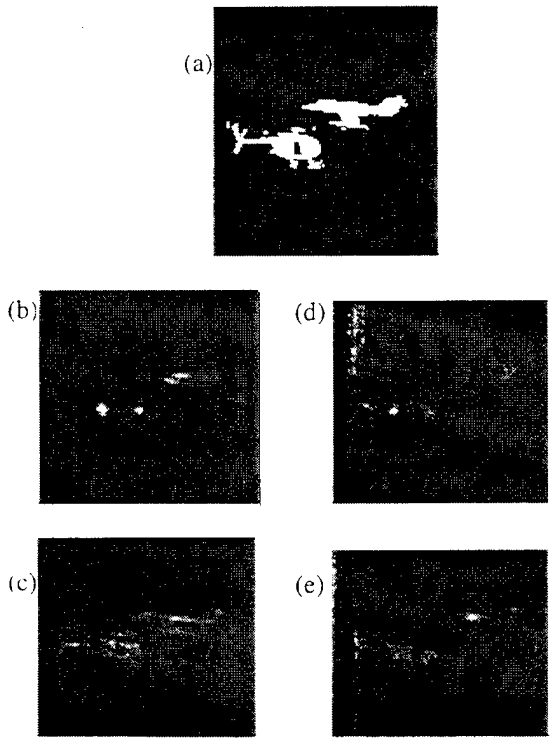

Figure 7. (a) Input to SLM1 and correlation output for simulated (b)helicopter and (c) airplane identification and. experimental (d) helicopter and (e) airplane identification. Excellent agreement is obtained.

We have been working with a variety of images to analyze the performance of the correlator system. A simulation program we have developed is an extension of a program that we use to create files that can be put directly onto the SLMs. The correlator simulation program takes the input images for what corresponds to SLM1 and SLM2 of Fig. 6. The program can perform Fourier transforms on any of the frames and can multiply the two frames together. Thus pure products and correlations can be calculated. The program allows the user to input specific pixel characteristics, such as the maximum and minimum reflectivity and the maximum and minimum reflected phase change as a function of voltage. The program then can determine the change in correlation output that results from the non-ideality of the individual pixel response.

Our agreement between simulated and experimental correlation is quite good. Fig. 7 depicts an identification scheme where a helicopter and an airplane are identified via the simulation program and the experimental correlator setup. In the correlator system, encoding the phase information of the target's Fourier transform onto the binary amplitude modulating SLM creates the Fourier filter planes. Such amplitude encoded binary phase only filters have been shown to have high optical efficiency, good target discrimination, and virtually no sidelobes[11]. As is shown in Fig. 7, changes in the target filter permit identification of either the helicopter or the airplane in this experiment. Furthermore, as the input image changes, the correlator can track the movement of the desired object. Using our current set of Fourier filters, peak to secondary efficiencies of 2.9:1 have been achieved in simulation while efficiencies of 2.:1 were obtained experimentally. This is sufficient for the military uses we are targeting. Fig. 8 shows some of these results.

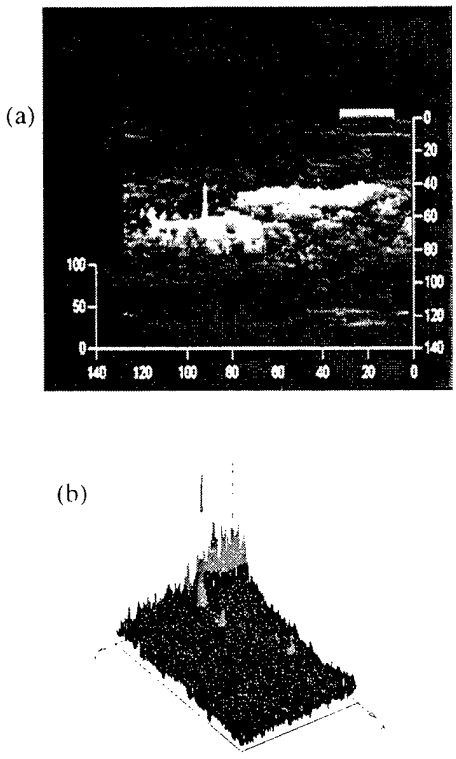

Figure 8. Intensity mapping of helicopter identification for (a) simulated and (b) experimental demonstrations. The major correlation peaks is clearly distinguishable from the background.

2-D 8-bit Gray-Scale Capable SLMs

Spatial light modulators (SLMs) realized with gray scale capability are key to the improvement of signal processing resolution over binary (on-off) devices--particularly because most image sensors generate pictures with gray scale levels. We currently have 2-D binary SLM devices that provide up to a 256 x 256 pixel format and input display data in a parallel row format (total number of data inputs is the square root of the total number of pixels for a given array). Gray scale capability can be simulated by time slicing, but only at the expense of significant decreases in frame rates.

In order to develop high-speed 2-D gray-scale capability for our optical devices, there are several technical and mechanical factors pertaining to I/O and signal conversion. These factors need to be resolved by the drive electronics. First, for binary devices, each pixel is represented by one data bit (on or off); for gray-scale devices, data representation/pixel increases by a factor of 8 for 256 gray-scale levels. To maintain the same frame rate, the total number of data input pads would need to increase from 256 to 2048 for a 256 x 256 array. This would make SLMs more difficult, and hence more expensive, to manufacture. Second, the optical pixel spacing currently sets the maximum area allowable for the drive electronics for an individual pixel. For our future pixel sizes, designing and developing a Si driver chip that can house an individual digital to analog converter (DAC) within that available area is physically not possible.

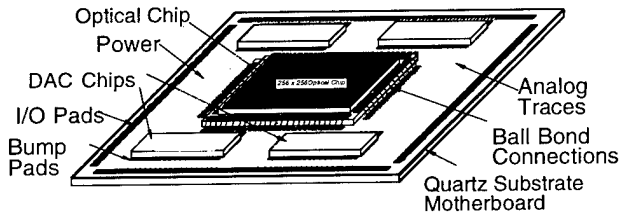

Figure 9. 2-D 8-bit gray-scale multi-flip-chip-module (MFCM) baseline design concept; quartz mother board supports a maximum of four Si digital-to-analog converter (DAC) chips, hybrid .

Fig.9 depicts our approach for creating a cost-effective packaging technique to support large 2-D gray-scale arrays. This approach will leverage existing drive chip designs to reduce cost, maintain high frame rates for 2-D gray-scale devices (>100,000 frames/sec.), and utilize bump-bond hybrid technology for ease in data routing.

The logic frame motherboard will support one of four, 64-channel DAC circuits depending upon system configuration (hard coded by bond configuration), and a hybrid optical/signal interconnect chip that will be used in all configurations. The completed multi-flip-chip-module (MFCM) will reside on a printed circuit board (PCB) assembly that includes logic functions such as a host PC interface, local frame memory, and a master/slave control scheme for operating multiple SLM assemblies in synchronization.

Conclusion

In conclusion, we are developing high-speed systems based upon our GaAs-based spatial light modulator arrays. Our intent is to maximize data and image throughput in systems, while taking advantage of the large reflectivity and low power switching afforded by GaAs Fabry-Perot modulators. Such modulators have a multitude of possible operating modes. The devices favored can operate as either modulator, LED, or detector. Detailed simulations allow both pixel designs to be improved and system level performance to be modeled. Our modules use local SRAM for high-speed data access and frame loading, while synchronizing frame updating through the use of a master-slave control network among several data independent SLM modules. Our modular approach allows very complex systems such as correlators to be developed, and we have demonstrated a very-high-speed correlator system. Advanced, multi-chip packaging techniques will allow us to enhance per-pixel functionality on larger format arrays.

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High Throughput Opto-electronic VLSI Switching Chips

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Integrated Optoelectronic Circuits, Optoelectronics, Optical Interconnects, Quantum Well Devices

Abstract

We describe chips containing 8 x 8 and 4 x 8 arrays of 16 input, 16 output switching networks operating from 600 Mb/s - 900 Mb/s per channel using MQW modulators and detectors flip-chip bonded to silicon CMOS.

As the demand for telecommunications services continues to increase, the need to switch large bandwidths of data becomes important. While purely electronic solutions are possible, photonic solutions, using the integration of electronics with optical I/O (smart pixels), provides the potential for smaller physical volume, lower latency, lower power dissipation, and lower cost. We describe initial results from two opto-electronic switching chips, one with 1024 differential optical inputs and 1024 differential optical outputs with individual channels tested above 600 Mb/s and a second with 512 differential optical inputs and outputs with individual channels tested up to 900 Mb/s. The technology for the chip consists of flip-chip bonding of 850 nm GaAs/AlGaAs multiple quantum well (MQW) detectors and modulators onto silicon CMOS with substrate removal to allow access to the optical devices [1] (see Fig. 1a).

	Chip 1 [4]	Chip 2 [7]	Chip 3
Technology	1.0 μm (λ=0.5)	0.8 μm (λ=0.4)	0.35 μm (λ=0.24)
Pixel function	16 x 1 node (mux)	16 x 16 switch	16 x 16 switch
Number of processing units	256	64	32
max data rate @ < 10^{-10} BER	450 Mb/s	600 Mb/s	790 Mb/s *
best case sensitivity at design rate	-18 dBm @200Mb/s	-15dBm@600 Mb/s	-15dBm@625 Mb/s
required optical energy/beam	(~80fJ)	(~50 fJ)	(~50 fJ)
Optical I/O	4096 in	1024 x 2 in	512 x 2 in
	256 out	1024 x 2 out	512 x 2 out
Potential Throughput	115 Gb/s	600 Gb/s	404Gb/s
Potential I/O Bandwidth	230 Gb/s	1.2 Tb/s	800 Gb/s
Tested Throughput	2.92 Gb/s [5]	600 Mb/s	790 Mb/s
Chip size	7 x 7 mm	7 x 7 mm	4 x 4 mm
Optical field size	5.44 x 5.44 mm	5.12 x 5.44 mm	2.24 x 2.24 mm
Optical window spacing	80 μm	80 μm	35μm, 70μm
Window density	15.6K/cm^2	15.6K/cm^2	40K/cm^2
Electrical static dissipation	1W @ 5.5 V	5W @ 5V	<1W @3V
#FETs	160K	450K	225K
Electrical I/O	23 @ 120 Mb/s	23	23

Table 1 Characteristics of previous chip and the two new chips. (*limited by test equipment)

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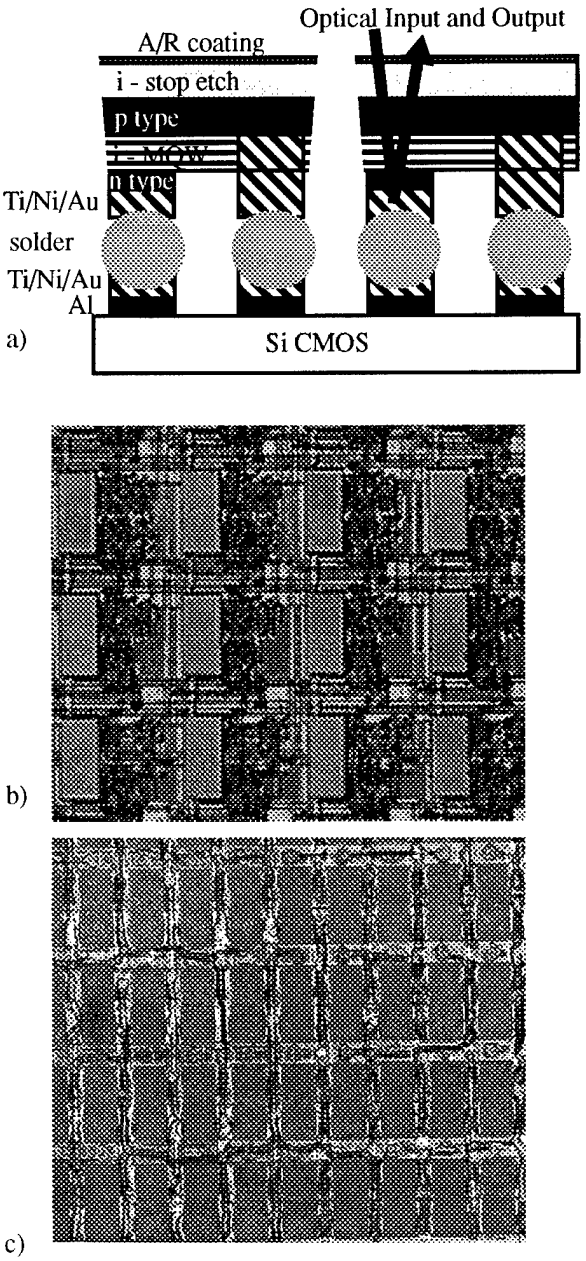

Fig. 1.a) Side view pictorial of Optoelectronic VLSI b) Photograph of 1.0 μm CMOS chip [4], (0.8 μm CMOS chip has same layout), and c) 0.35 μm chip. Rectangles (~ 20 μm x 50 μm) are optical modulators and detectors on 80 μm centers in b) and 35/70 μm centers in c.

The switching chip implements part of a simplified distribution fabric for a growable packet ATM switch [2,3]. Previously, an opto-electronic chip [4] and system [5] have been demonstrated implementing this architecture. That chip, designed using 1 μm CMOS, contained two hundred fifty-six 16 x 1 nodes (or sixteen 16 x 16 switches with optical fan-out) operating at a maximum speed of 450 Mb/s. The system operated at 208 Mb/s as a time multiplexed switch, capable of routing ATM cells at OC-3c rates (155 Mb/s) with an appropriate out-of-band controller.

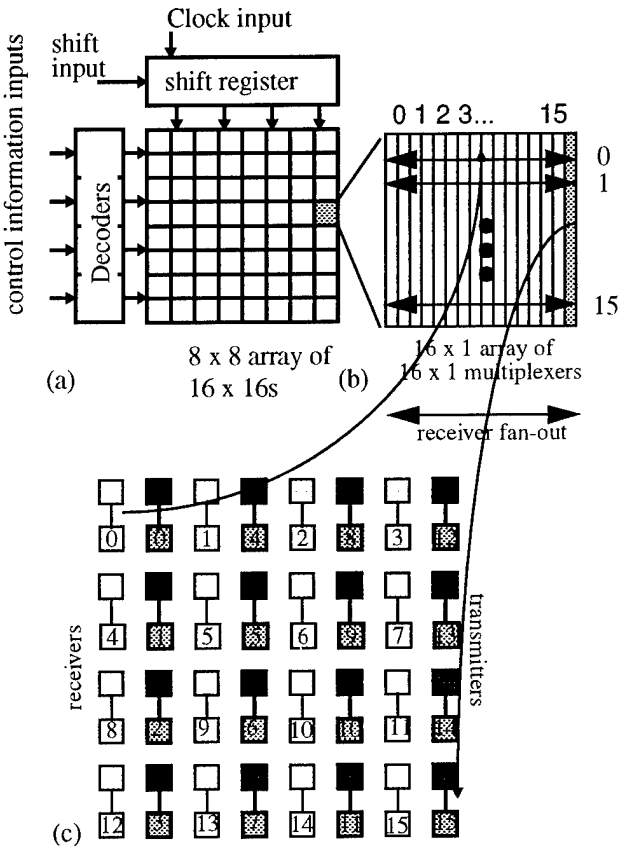

Fig. 2. (a) Block diagram of chip. Each square in represents a 16 x 16 switch. (b) Each switch is implemented using sixteen 16 x 1 multiplexers with electrical fan-out of receiver outputs (arrows). (c) optical differential receivers (light color) and transmitters (dark color) that are overlaid on top of the switches. Receivers are mapped by number to horizontal fan-out lines (arrows) and transmitters are mapped from multiplexers (column numbers)

The current chips, designed in 0.8 μm and 0.35 μm CMOS, contain sixty-four and thirty two 16 x 16 switches respectively (Fig. 2.). The 16 x 16 switches are implemented by fanning out the *electrical* outputs from 16 differential receivers to sixteen 16 x 1 multiplexers, each with a differential optical output. The optical inputs an outputs are arranged in a rectangular array on top of the multiplexers. Control of the chips is electronic. The combination of

increased density, the use of a third level metal with circuitry underneath the flip-chip bonding pads [6], and electrical fan-out allows four (0.8 μm) to ten (0.35 μm) times the functional circuitry in the same area. Table I gives a summary of the characteristics of the previous chip [4] and the two new chips.

The receiver for chip 2 (Fig. 3a.) uses a modified design of that described in [8]. The sensitivity versus bit-rate (Fig. 3b.) was measured for a single receiver. The performance is not quite as good as that in [8], one reason for this, is that an imbalance was intentionally introduced in the stage following the receiver before a large electrical fan-out driver to reduce the static dissipation. A second reason is that the receiver outputs from neighboring 16 x 16 switches were inadvertently pair-wise connected and testing was done by driving both receivers in tandem using a 1 x 2 binary phase grating. Unequal powers on the receivers may cause signal distortion in the common line. Our previous chip with single ended receivers showed good uniformity (< +/-400 ps gate delay variations) across the chip [4]. We expect the variations in these circuits to be comparable or less.

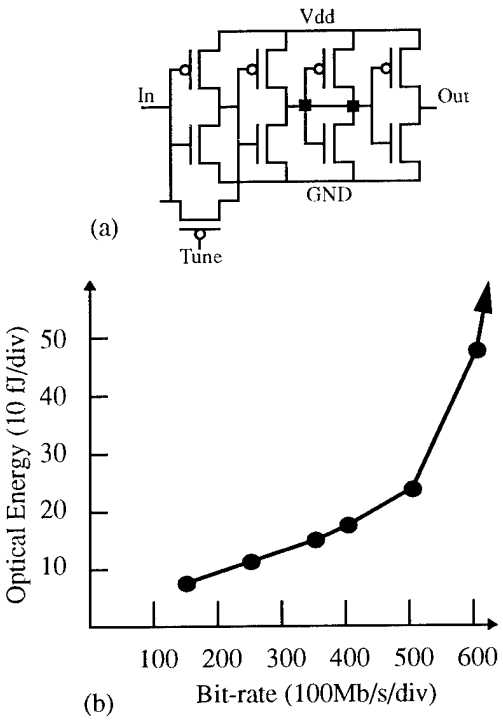

Fig. 3. (a) receiver schematic and (b) sensitivity versus bit-rate for the switching nodes in chip 2.

The large number of active receivers leads to a static power dissipation of almost 5W. The exciton shift due to thermal heating of the circuit was found to be almost 10 nm both at the center and at the edges of the array (Fig. 4). Using a shift of 0.28 nm/ °C, the thermal resistance of the package was found to be < 7 °C/W. The uniformity of the position of the exciton peak in reflectivity while dissipating 5W indicates the temperature uniformity across the array is within a few degrees. The chip mount was specifically designed for temperature uniformity [9].

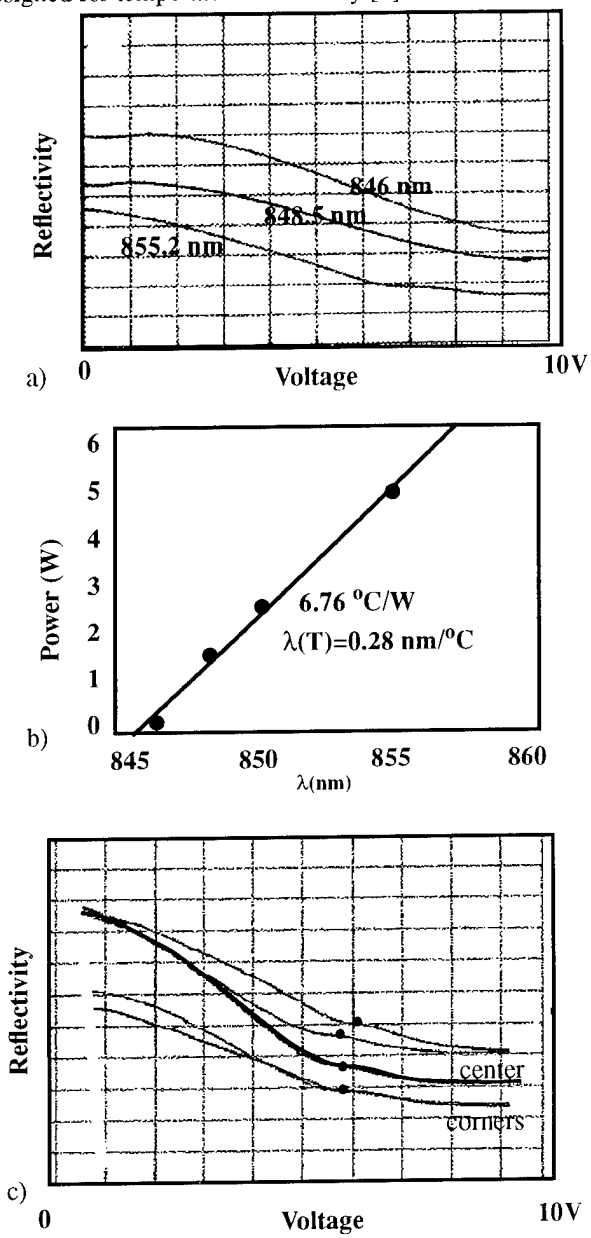

Fig. 4. a) Reflectivity vs. voltage at 3 different power dissipations, from top: 0W, 1.4W and 5W, achieved by adjusting receiver bias voltage. b) Dissipated Power vs. Optimum wavelength. c) Reflectivity at the four corners and in the center of the array showing little temperature dependence evidenced by locations of the indicated points of inflection.

There are 16,384 (64 x 16 x 16) paths through the switching chip. Sixteen paths were measured at a data rate of 625 Mb/s (Fig. 5), sampling the upper left 16 x 16

switch, exercising each receiver and each modulator driver from that switch. Due to the architecture of the chip, we would not expect large delay variations between inputs, this was indeed the case on our earlier chip that was more thoroughly characterized [4]. Care was not taken to ensure uniformity of photocurrent throughout this set of measurements, so there might be some power dependent variations in delay. Individual channels had bit error rates below 10^{-11} at 600 Mb/s and below 10^{-9} at 625 Mb/s. While all paths weren't measured, all but 7 MQW diodes luminesced under forward bias. Thus, if there are no additional problems in the silicon circuit, nearly all paths should be operational.

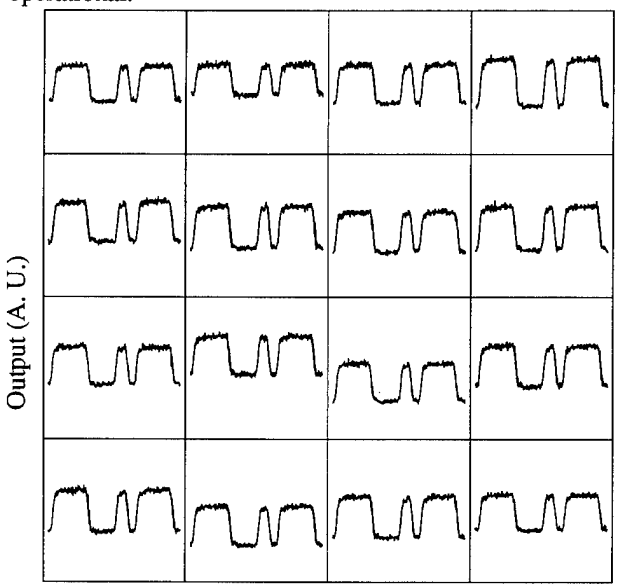

Fig. 5. Sixteen outputs from the upper left 16 x 16 switch with output i selecting input i at 625 Mb/s with a bit pattern of 01000111 for chip 2. The zero line is accurate, i. e. the contrast ratio is approximately 2:1.

Crosstalk was measured by operating one path of the switch at one frequency and a second path at a slightly different frequency. When looking at the eye diagram, no noticeable eye closure was seen. However, on a spectrum analyzer, one can see the undesired signal as shown in Fig. 6. Its magnitude greatly depended on the value of the feedback resistor, getting substantially worse than that shown, for receivers biased for maximum sensitivity.

The chip was redesigned in 0.35 μm CMOS. Because of the decreased feature sizes, another factor of 2.5 in density was achieved (see Fig. 1b,c). The receiver design eliminated the second stage gain broadening transistors and included clamps in the feedback path. Elimination of the gain broadening transistors reduces the static power dissipation at the expense of increased sensitivity. If the feedback FET is gated off, the clamps further reduce power dissipation and allow dynamic operation, which has not yet been tested on this chip.

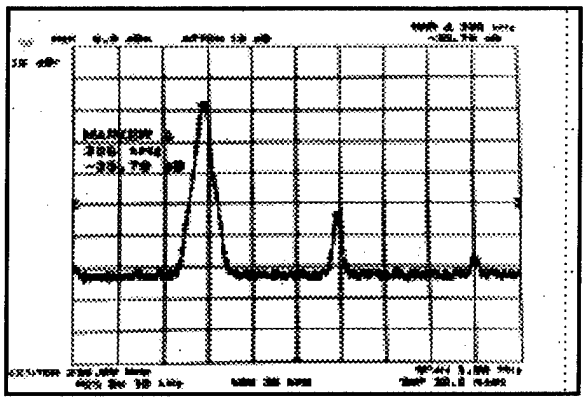

Fig 6. Desired and undesired signals through one path of the 0.8 μm switching chip.

This chip had a few minor design errors, which are currently being corrected. We were still able to pass signals through many paths of the chip and control many of the nodes. Fig. 7 shows operation of a single channel at 800, 900, and 1000 Mb/s with pseudorandom (10^{-23})bit patterns. Bit error rates were measured up to 790 Mb/s which was the maximum rate that the BER receiver would respond to a direct laser input. (The specification for the BER receiver was 700 Mb/s). We might expect operation above 900 Mb/s judging by the eye diagrams and this will be investigated further.

We have described initial characteristics of opto-electronic switching chips with potentially greater than 1 Terabit per second I/O bandwidth. While crosstalk, thermal spatial variations under dynamic operation, and delay variations need to be rigorously characterized before this I/O bandwidth can be utilized in a system, these chips further illustrate the potential of hybrid opto-electronic VLSI smart pixel technologies.

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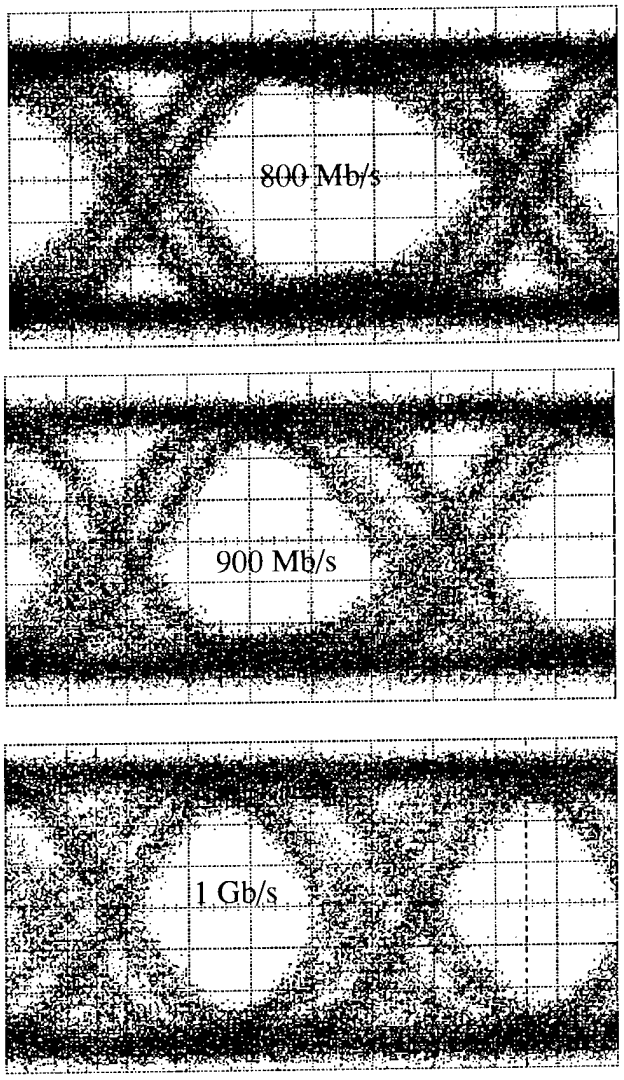

Fig 7. Operation of the 0.35 μm switching chip at 800, 900, and 1000 Mb/s. Optical power was roughly 250 μW per beam.

Demonstration of a CMOS Static RAM Chip with High-Speed Optical Read and Write

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Abstract: We demonstrate a dense VLSI RAM technology with high-speed optical read and optical write capability. The CMOS-based Static-RAM technology is capable of parallel optical access with read/write speeds limited by the native RAM access times. We have fabricated a 2mm x 2mm optoelectronic-VLSI test chip incorporating 800b storage and 200 optical I/O based on the hybrid integration of GaAs/AlGaAs MQW modulators onto CMOS. Results from the test chip confirm 6.2ns read and 8ns write capability.

Keywords: optical interconnects, smart pixels, memories

In the last three decades, random access memory (RAM) densities have progressed at an incredible rate, from the early 1 Kilobit chips to the 1 Gigabit DRAMs that have recently been produced [1]. Similar progress has been made in the development of micro-processors, with 64-bit RISC processors now operating at 450MHz, and GHz processors on the horizon [2]. Data transfer rates from high-density memories to processors have not, however, followed this growth curve, producing an increasing gap between memory and processor bandwidths. This has created an opportunity for new techniques for high-speed data transfer from main memory.

In this paper, we investigate the potential for parallel optical data transfer to and from silicon VLSI memories. Such optoelectronic memory devices are likely to be useful for a variety of applications. Special purpose hardware for direct processor-to-memory optical interconnection are under investigation by several research groups [3]. Recent efforts at developing high-capacity optical memories and free-space optical memory-access systems have also created a need for high-speed, optoelectronic buffer-memory interface circuits. Such free-space digital optoelectronic systems promise the ability for direct processing and data-reduction on the contents of high-capacity optical memories. The availability of parallel optical access to high-speed RAM will also permit the development of an efficient, *memory-based* optoelectronic-switch: a goal that cannot be achieved with conventional space-division photonic switching technologies.

Optoelectronic technologies that can provide fast optical access to Silicon VLSI chips now exist. One such technology is based on the hybrid integration of GaAs Multiple Quantum Well (MQW) photodetectors and light-modulators onto a pre-fabricated silicon integrated circuit using flip-chip bonding technique followed by substrate removal of the GaAs chip to allow surface-normal operation of the optical modulators at 850nm [4]. Previous work based on this hybrid technology has demonstrated that optoelectronic page-buffer circuits based on FIFO buffers [5] or shift-register pixels [6] can be achieved. Here, we present, for the first time, a dense CMOS VLSI RAM with high-speed optical read and optical write capability. Specifically, we demonstrate an optically-accessed SRAM technology with 6.2ns read and 8ns write capability.

The Photonic SRAM test chip (Fig. 1) is an optically and electrically accessible SRAM with 96 parallel optical inputs and 96 optical outputs. Data is stored in 8 separate addresses (words) with 96 bits per word, providing a capacity of approximately 800 bits. The eight least significant bits of each word of the RAM are electrically accessible from an on-chip shift register. Eight bits of data can be loaded into the shift register from off-chip and then stored in the RAM. Similarly, the first eight bits of the RAM can be transferred in parallel into the shift register and then shifted out serially. All 96 bits of each address can be written to, or read out, optically. Multiplexers select whether data is read/written electrically or optically. All

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data address lines (3 in this case) to the chip were electrical. These features permit electrical, optical, and electrical/optical mixed-signal testing of the RAM chip. The dimensions, of the Photonic RAM test chip were approximately 2mm x 2mm. The chip contained approximately 11,000 transistors.

Figure 1: Microphotograph of the 0.8μm, CMOS/MQW-modulator, Static-RAM integrated-circuit, showing a portion of the 10 x 20 array of diodes after bonding and substrate removal [11]. MQW modulators are 20μm x 50μm with 62.5μm / 125μm separations.

A SEM photograph of the chip surface before bonding is shown in Figure 2. The MQW diodes were integrated directly over the circuits in this design [5]. The top-level metal (Metal-3) was reserved for bond-pads and wiring to the diodes. Static-RAM cells were laid out beneath the bond-pads and wired with two levels of metal interconnect. Measured bit-cell sizes for the Photonic SRAM fabricated in a 0.8um technology was approximately 127μm^2. The cell efficiency was 55% due to the conservative layout applied to the metal bit-lines and supply lines. Scaling the design to a 0.5μm technology would provide a cell size of approximately 46μm^2 and an aerial density of 1.2 Megabit/cm^2. Figure 3 contrasts the aerial density of various electronic memory technologies, including embedded (synthesized) SRAM, optimized SRAM, Flash memory, and DRAM produced in standard logic (ASIC) as well as optimized technologies [7,8]. The use of DRAM circuits instead of SRAMs, even in logic (non-optimized) technologies can provide substantial increase in aerial density. Flash memory can provide further increases in aerial density, at the expense of slower writing times.

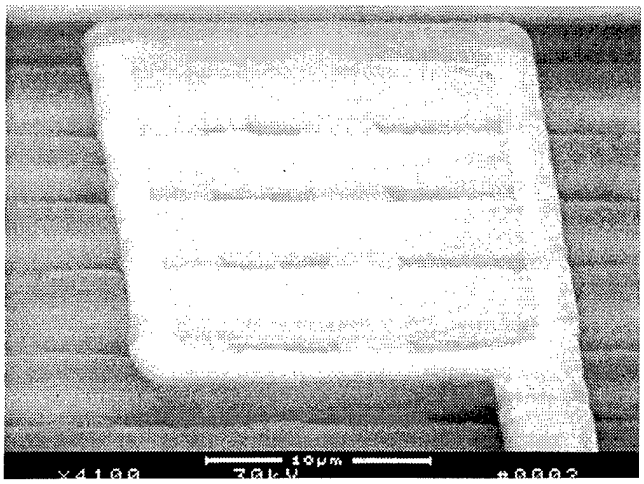

Figure 2: SEM of silicon CMOS integrated circuit prior to bonding, showing 20μm x 20μm flip-chip-bond pads (Metal-3) with underlying SRAM cells. Each memory cell occupies 10μm x 13μm in a 0.8μm technology.

Memory Technology	Process	Cell Size (μm²)	Cell Efficiency	KBits/cm²
PSRAM (0.8μm)	3-metal ASIC	127	0.55	431
PSRAM	3-metal ASIC	46	0.55	1,196
Embedded SRAM	3-metal ASIC	67	0.70	1,045
SRAM	2-metal & Local Int.	43	0.65	1,512
ASIC-DRAM	3-metal ASIC	23	0.60	2,609
DRAM	2-metal & Stack	3.2	0.50	15,625
Flash	3-metal & 3-poly	2.8	0.67	24,071

Figure 3: Cell-sizes and densities of optimized SRAM, DRAM, ASIC-DRAM and Flash memory technologies for typical 0.5μm implementations [7,8]. Projected photonic SRAM density based on the fabricated cell for the 0.8μm and a potential 0.5μm implementation are shown for comparison.

The memory array in the Photonic SRAM test chip is a two-dimensional grid of memory cells, each storing 1 bit. Each memory cell is a 6 transistor circuit that consists of two cross-coupled inverters and two pass transistors (Fig. 4). Although electronic SRAM ICs typically use only a small number of external I/O channels, internally, the SRAM can be a highly parallel device capable of supporting large word sizes.

Read/write circuitry is repeated once per bit column. The write circuit consists of write select multiplexers for data input lines. The read select circuitry consists of bit line pull-ups to precharge the bit lines to V_{DD}, write select multiplexers for data output lines, and a sense amplifier. The data-input and data-output circuitry is repeated once per bit column. This circuitry consists of a bit line drive for write operations and an output sense amp that supplies a second stage of amplifications. Receiver circuits and transmitter circuits accounted for the remaining area of the chip. These transceiver circuits have previously been implemented [9].

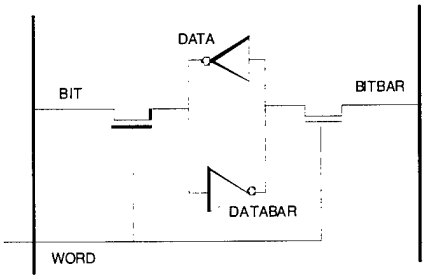

Figure 4. CMOS Memory cell circuit for static RAM uses 6 transistors and occupies 25λ x 20λ.

Writing to the RAM is performed in three steps. First the address bus is set to the memory address that is being written to. At the same time, the input-data bus is loaded with the data to be written. Second, the write signal (WR), which normally stays high, is pulled low and held there for a specified time period (t_{WC}). When the WR signal goes high, the data on the DIN bus is written to memory. As is typical for edge-triggered storage circuits, the input-data bus must remain unchanged for a specified amount of time before (setup time) and after (hold time) the rising edge of the WR signal.

Reading from the RAM is accomplished in two steps. First, the address bus is set to the memory address that is being read from. Second, after a certain amount of time (t_{RC}), the contents of that memory location appear on the data-output bus.

The photonic SRAM chip was tested for data storage and retrieval. Substantial electrical and optical read/write testing was performed for the photonic SRAM to verify correct operation. Once data was written to the photonic SRAM, the read cycle involved changing the three electrical address lines, and waiting for the appropriate data to appear on the output modulators. The minimum time required for data to be valid after the address lines had settled can be defined as t_{RC} (Fig. 5a). This was determined by continuing to increase the frequency with which the electrical address lines were cycled until invalid data was read out on the optical modulators. As shown in Figure 5b, t_{RC} was determined to be 6.2ns. This corresponds to a total read-bandwidth of 15 Gigabits/s from the test chip.

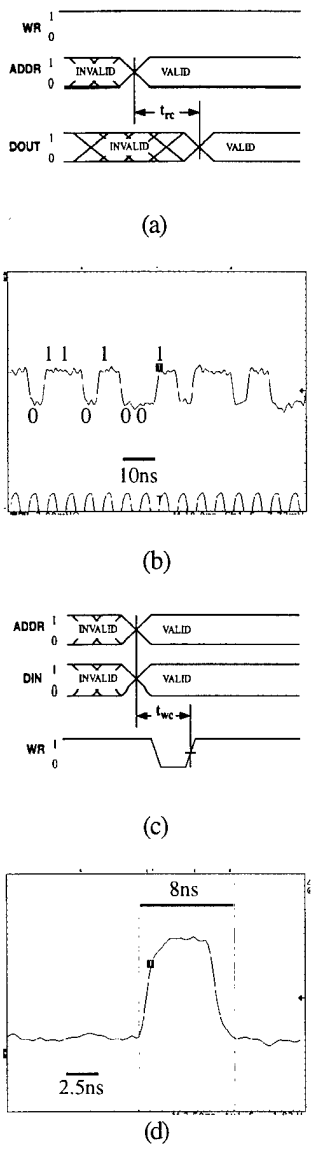

Figure 5. Read/write speed measurements of the photonic SRAM integrated circuit: (a) schematic waveform showing definition of minimum read cycle time t_{RC}; (b) measured output optical waveform from photonic SRAM at 160Mbit/s with t_{RC} = 6.2nsec; (c) schematic waveform showing definition of minimum write cycle time t_{WC}; (c) measured pulse width of t_{WC}=8ns applied to electrical WR line results in correct write operations to memory.

High speed writing to the photonic SRAM was, similarly performed both electrically and optically to a particular address. The minimum write cycle was determined by shifting a desired 8-bit data pattern into the shift register and then electrically pulsing the WR line

with a short pulse. The stored data was then loaded back into the shift register, shifted out of the chip, and compared to the original data. If the data was valid, the minimum pulse width was then reduced. For optical tests, the data was placed on the appropriate detectors before the WR line was pulsed. Data was then read out on the appropriate modulators and verified. Figure 5c shows a schematic waveform defining the minimum write cycle time t_{WC}. Figure 5d presents the measured minimum pulse width (t_{WC}) of 8ns applied to electrical WR line that result in correct write operations to memory. This corresponds to a total write-bandwidth of 12 Gigabit/s.

Static and dynamic power dissipation was measured during operation. The chip was mounted in a standard 84 pin grid array package. The tiny chip consumed approximately 650mW of static power dissipation due to the transimpedance receivers and the sense-amplifier read circuits. Dynamic power dissipation was measured at 110mW at 25MHz operation up to 300mW at the maximum readout operation speed of 160MHz. The maximum total chip dissipation was measured at 950mW at an operating voltage of 5V.

In summary, we demonstrate, for the first time, a CMOS Static-RAM technology capable of high-speed parallel optical access. The tiny 2mm x 2mm test chip incorporated 96 optical inputs and outputs, 800b storage, and several electrical and optical control and test features. Storage cell size was approximately 10μm x 20μm in a 0.8μm process. This is smaller than typical SRAM cells, but significantly larger than custom SRAM, DRAM, or Flash technologies. Minimum read-cycle and write-cycle times were measured at 6.2ns and 8ns respectively. This corresponds to aggregate optical read and write bandwidths of 15 Gigabit/s and 12 Gigabit/s, respectively.

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Design and Partitioning of a Free-space Optical Interconnection FFT Processor

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Abstract

We describe the design of a high-performance chipset for computing 1-D complex fast-fourier transforms (FFT). Our chip technology is based on flip-chip integration of submicron CMOS ICs with GaAs chips containing 2-D arrays of multiple-quantum wells (MQW) diode optical receivers and transmitters. Our system technology is based on free-space optical interconnection. Compared to an electronic implementation, the proposed design offers increased performance and a reduced chip count. Since our design uses direct, one-to-one interconnections between chips, it is compatible with a number of emerging three-dimensional free-space optoelectronic packaging technologies.

Keywords: FFT, optical interconnects, optical SRAM, smart-pixels, array processing, parallel processing

1. Introduction

Free-space optical interconnection (FSOI) of integrated circuits shows great potential for efficient implementation of high-performance parallel computing and signal processing systems [1,2]. On the implementation front, several FSOI technologies are now under development and prototype FSOI systems have been demonstrated [3,4,5,6,7,8]. On the theoretical front, a number of papers have been published that describe architectures and system designs for application specific FSOI systems. However, with the exception of switching and backplane interconnect applications [9,10,11,12], there has been relatively little published work that includes detailed integrated circuit (IC) design and accounts for the impact of IC layout constraints on FSOI system architecture, design and performance. Such a detailed design study is the objective of this paper. We focus on a specific problem of designing a high-speed FSOI FFT processor. Our FSOI technology is based on the hybrid CMOS-SEED platform that integrates GaAs MQW photodetectors and modulators with high-volume commodity CMOS VLSI processes[13]. For CMOS technology we use the 0.5 micron HP/MOSIS CMOS14 process [14]. This is a high-speed, high-density 3.3V/5V CMOS process with tight-pitch (1.4 micron), planarized interconnect system that allows three levels of metallized interconnect. Our optical interconnect technology is based on free-space holographic interconnect technology that has previously been used in several FSOI demonstrators [15].

The result of this work is the design of a chipset for building FSOI FFT processors consisting of the Photonic FFT (PFFT) chip and the Photonic RAM (PRAM) chip -- essentially an optical SRAM. The PRAM chip integrates over 2.5 million transistors in an estimated 1cm x 1cm die area. The PFFT chip integrates over 1.4 million transistors in an estimated 1.2cm x 1.2cm die area. Each chip has 768 optical inputs and 768 optical outputs, providing a chip-to-chip bandwidth of 29 Gbytes/sec at 150 Mhz clock speed. A complete 8,192 point (or smaller) FFT processor can be built using just three chips, while larger and faster systems can be built using additional chips. It is shown that the proposed design offers significant advantages over purely electronic implementations in terms of increased performance and reduced chip count. In section 2, we discuss electronic and FSOI technologies. Section 3 discusses the FFT algorithm and its partitioning for an FSOI implementation. In section 4, we present detailed IC design for the PFFT and the PRAM chips and a discussion of the optical system. Performance evaluation and comparison with existing electronic implementations is provided in section 5. Section 6 winds up with some conclusions about our design.

2. Background

The fast-fourier transform (FFT) is an important operation in many applications such as signal processing, telecommunications, speech processing, high-speed control, and instrumentation [16]. As a result of this, a number of hardware implementations for fast-fourier transform processors have been developed. These processors are built using multiple processor and memory chips packaged using multichip modules (MCMs), printed-circuit boards (PCBs) and backplanes.

The FSOI approach is based on the integration of low-power surface-normal optical interconnect technology with high-volume commodity VLSI processes. This approach provides fast and low-latency inter-chip interconnects effectively eliminating several levels of the electronic packaging hierarchy. In this paper, we will quantify the potential advantages of the FSOI approach for building FFT proces-

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sors. To achieve this, we perform a detailed architecture, system, chipset and optical system design for an FFT processor using the hybrid SEED FSOI technology platform. The hybrid CMOS-SEED technology was chosen based on its performance, availability and maturity [17].

The hybrid CMOS-SEED technology integrates optical inputs and outputs with standard silicon CMOS circuitry. Quantum well diodes can operate either as optical reflection modulators (outputs) or as photodetectors (inputs). These diodes are bonded and electrically connected in a regular grid directly over the silicon circuits. This technology offers optical inputs and outputs that can run at the speed of the underlying silicon technology, with small areas, low powers, and large densities of inputs and outputs. Since the quantum well diodes can operate either as modulators or detectors, the user can choose to use them either as inputs or outputs.

3. FFT Algorithm Mapping

3.1 Fourier Theory

The Discrete Fourier Transform (DFT) of an N-point sequence is given as:

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j\left(\frac{2\pi}{N}\right)nk} \quad k = 0, \ldots, N\text{-}1 \qquad (3.1)$$

Since this formula leads to a large amount of computations (N^2 complex multiplications and N(N-1) complex additions), some means of decreasing these time-consuming calculations is desired. The FFT algorithm is such a method of reduction and was developed from the DFT by Cooley and Tukey [18]. The efficiency of the FFT algorithm lies in its elimination of the repetitive computations of the exponential term in the DFT. As a result, there are only $(N/2)\log_2 N$ multiplications and $N\log_2 N$ additions. By comparison, a 1,024-point FFT requires only 1% of the calculations that a 1,024-point DFT does.

3.2 The FFT Algorithm

The FFT algorithm is a series of multiplications and additions which is performed in stages. It can be implemented using the butterfly processor (BP) as shown in Figure 3-1. The butterfly diagram can show graphically the

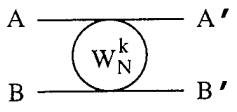

FIGURE 3-1. The butterfly processor

flow of data as the calculations are performed. For an N-point FFT, the FFT is calculated with N/radix# butterflies per stage and $\log_{radix\#}N$ stages. The radix-number tells how many inputs and outputs the BP will have. Using radix-2 butterflies, there will be N/2 BPs per stage and $\log_2 N$ stages where each BP has two inputs and two outputs. For example, Figure 3-2 shows a 16-point FFT having four stages with eight BPs per stage. The inputs of the FFT are data

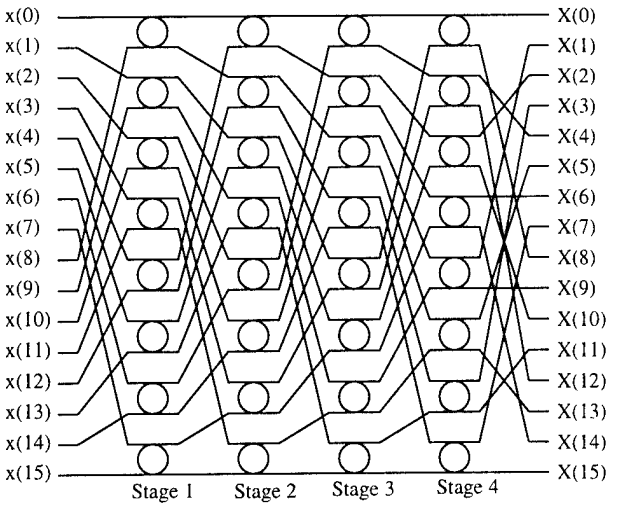

FIGURE 3-2. A 16-point FFT

points sampled in the time domain. The outputs are discrete frequency-domain data points.

The equations that result for a radix-2 BP are as follows:

$$A' = A + W_N^k B \qquad (3.2)$$

$$B' = A - W_N^k B \qquad (3.3)$$

where A and B are complex numbers. W_N^k is called the "twiddle factor" and is expressed as:

$$W_N^k = e^{-j\frac{2\pi k}{N}} \qquad (3.4)$$

For actual hardware implementation, these equations should be broken down into real and imaginary components:

$$A'_R = A_R + B_R W_R - B_I W_I \qquad (3.5)$$

$$A'_I = A_I + B_R W_I + B_I W_R \qquad (3.6)$$

$$B'_R = A_R - (B_R W_R - B_I W_I) \qquad (3.7)$$

$$B'_I = A_I - (B_R W_I + B_I W_R) \qquad (3.8)$$

The above equations can be implemented in a straightforward fashion using four multipliers and six adders as shown in Figure 3-3 (where subtraction can be performed by 2's-complement conversion utilizing inverters and the carry-in bit on the adder).

To improve the computational efficiency of the hardware, higher-radix butterfly processors could be imple-

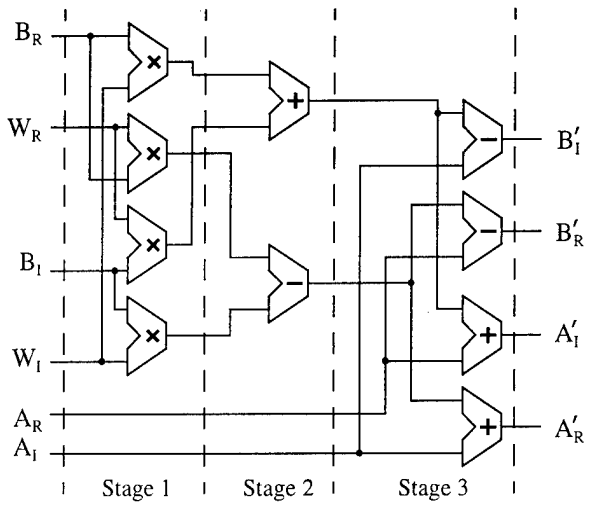

FIGURE 3-3. Radix-2 BP

mented. The concept here is that the higher radix BPs are more computationally efficient in that they have fewer multipliers per number of points processed. For example, a radix-4 processor uses twelve multipliers while an equivalent radix-2 implementation requires sixteen multipliers to process four data points. However, this efficiency comes at the price of design complexity. In the radix-2 BP, a simple bit-reversal scheme is used to determine the one twiddle factor for each BP. In higher radix BPs, a more complex algorithm is required to supply multiple twiddle factors for each BP. When multiple BPs are integrated on a single chip, as done in our approach, the generation and distribution of twiddle factors becomes an even more difficult problem. In addition, using higher radix BPs, leads to increased interconnection complexity for both the memory and the processor ICs. In this paper, we focus on the design of a radix-2 FFT processor.

The design presented in this paper makes use of the radix-2 butterfly processor as described above. Ideally, the quickest approach to computing the FFT would be a fully-parallel system with $(N/2)\log_2 N$ BPs. For an 8192-point FFT, that would be 53,248 BPs. Assuming that each BP is 1.8mm x 2.5mm in a 0.5μm CMOS technology, then only sixteen could feasibly fit on one die. In this case, there would be 3,328 die. With this many die, a single Multi-Chip Module (MCM) implementation would be impossible. A multiple MCM implementation would be possible. However, the butterfly architecture must be maintained, which means that each BP would be connected to four other BPs (212,992 connections). The partitioning of this massive design would be difficult and the physical realization on printed circuit boards would mean timing losses and therefore, a slower system. Alternatively, a free-space optical butterfly configuration is also possible. Assuming that there are still sixteen BPs on a die, then there would have to be 13,312 optical connections between the die. For a high-speed design, every optical connection would have to be parallel, meaning at least 32 bits per connection. Fully realized, this yields 425,984 beams of light being transmitted simultaneously and in a configuration that preserves the butterfly structure. Again, the logistics of an undertaking of this size renders it impractical. On the other hand, the most compact solution would be a serial implementation. This would include only one BP and the memory sufficient to keep track of the data. While this is an inexpensive setup, for an 8192-point FFT, there would have to be 53,248 passes, where a pass is a complete radix-2 calculation, of the BP, which would be too slow for real-time applications. Our scheme is a compromise between these two approaches. It is a semi-parallel implementation that places eight radix-2 BPs on one chip, called the Photonic FFT (PFFT). The PFFT as a system-level block, with the *A* and *B* inputs to the eight BPs, is shown in Figure 3-4. It takes

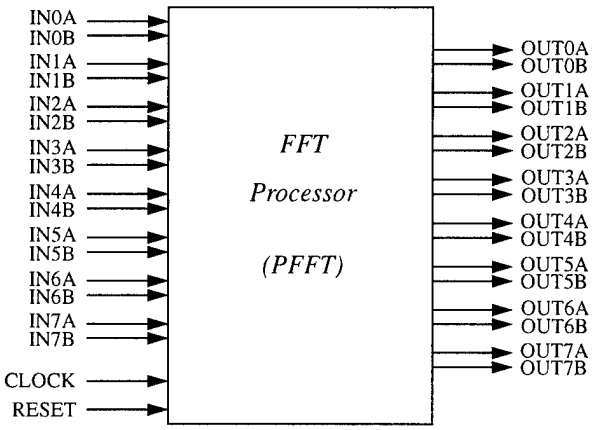

FIGURE 3-4. PFFT block diagram

advantage of both electronic implementations as well as optical. Eight butterfly calculations are performed electronically per clock cycle and data storage communication is accomplished through optical interconnects.

3.3 Butterfly Processor Operation

The inputs and outputs of the BPs are connected to optical receivers and transmitters that will be described later in the paper. The twiddle factor generator will be discussed later also. The processors operate in parallel and are loaded with data from a separate memory chip. The eight BPs will always work on data from one stage. The FFT procedure is as follows:

1. All of the data for one stage is entered into the eight BPs sixteen points at a time, where each retrieval of sixteen points is executed during one clock cycle. A perfect shuffle is required for the FFT and is achieved by reading in 2 points to each BP that are spaced N/2

apart as seen in Figure 3-5.

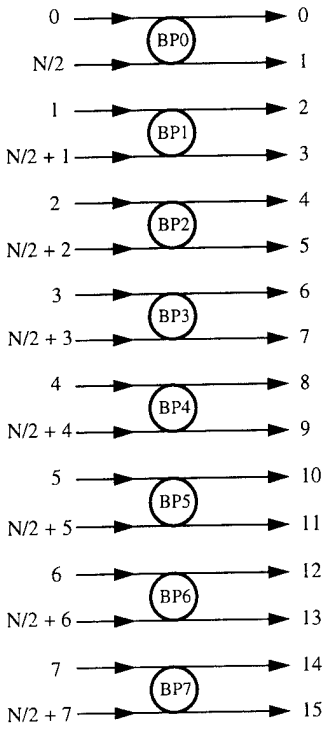

FIGURE 3-5. Data flow for the PFFT

2. The data that comes out of the BPs is stored in memory until it is needed for calculation in the next stage. As with the data input, each sixteen points of output is stored in one clock cycle. And, unlike the input, the output is cached as consecutive data points.
3. The procedure continues with data being read from one memory unit and stored in another until all the data from one stage has been processed. The next stage of data is then calculated in the same fashion using those numbers that were just stored from the previous stage.

The fact that eight BPs are operating in parallel along with the need for a perfect shuffle of the data requires a special data storage scheme. This memory configuration, called the Photonic RAM (PRAM), is shown at the system level in Figure 3-6. In order to get proper shuffle operation, the PRAM is divided into four banks of RAM, as shown in Figure 3-7. Each bank of RAM is further subdivided into four units representing the physical blocks of storage as indicated by the dashed lines in Figure 3-7. When reading data from the PRAM into the BPs, banks 0 and 2 will be read from at the same address, first. Then, banks 1 and 3 will be accessed from the same address also. This insures that all the BPs are supplied with data simultaneously and that each BP gets data that is N/2 points apart. For example, in reading from address 0 on banks 0 and 2, points 0

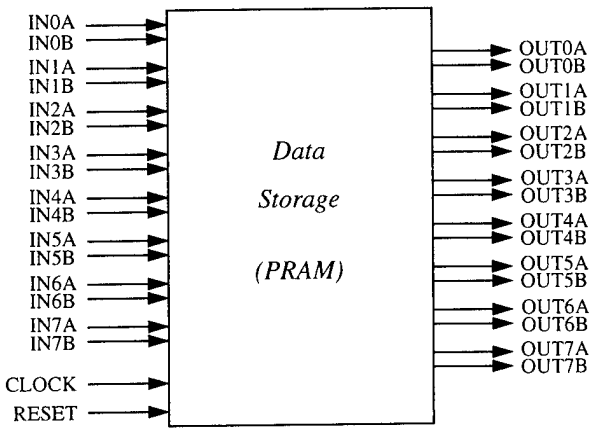

FIGURE 3-6. PRAM block diagram

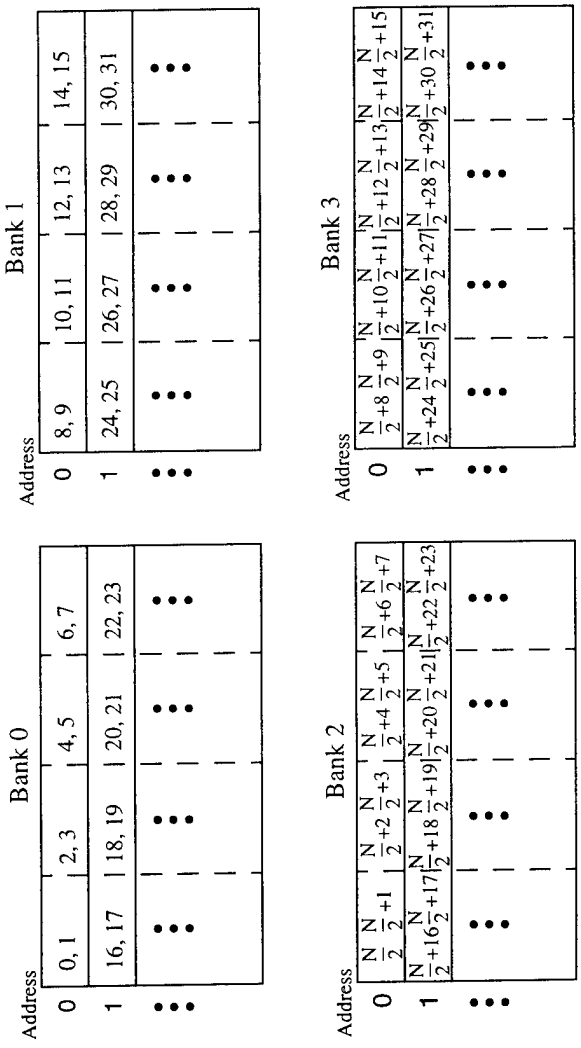

FIGURE 3-7. PRAM configuration

through 7 and N/2 through N/2+7 are supplied to the BPs just as shown in Figure 3-5. The operation continues, reading data from banks 0 and 2 followed by banks 1 and 3 at consecutive addresses until all the data for one stage has been read.

When storing data, on each pass, sixteen consecutive points of data have to be written simultaneously, seen in Figure 3-5. Therefore, the outputs are stored in the same address in banks 0 and 1 as shown in Figure 3-7. For example, on pass number 1, data points 0 through 15 will result from the BP computations and are stored in address 0 of banks 0 and 1. On the next pass, the outputs are stored in the next address of banks 0 and 1. This repeats until banks 0 and 1 are full. Then, the routine proceeds to write to the same successive addresses of banks 2 and 3. When banks 2 and 3 are full, another stage has been completed.

This memory retrieval and storage method has the added benefit that the data from the previous stage can be read directly into the current stage with no transformations. In other words, the data shuffle between stages is achieved without any physical reorganization of the data.

3.4 The Twiddle Factor Generator

The twiddle factor generator is a unit that was specially designed to work with the PFFT configuration of eight BPs on one chip shown in Figure 3-8. Twiddle factor generation is an important part of the FFT which is derived from a bit-reversal scheme based on the stage of the FFT calculation. For a single BP system, this is not a difficult task. Challenges arise, though, when trying to supply eight twiddle factors at a time. The data patterns that are discussed in the proceeding section are demanding to produce eight at a time. From the twiddle factor expression, W_N^k, the value of k is what is determined by the bit-reversal scheme. k ranges from 0 to N/2-1. This relates to the fact that there are N/2 BPs per stage. The bit-reversal algorithm for determining k goes as follows:

1. For stage 1, k is always 0.
2. The numbers between 0 and N/2-1 are written out in binary. Then, each number is rewritten with the bits reversed.
3. For the second stage, the bit-reversed numbers that were just written are taken as the values of k for each BP in the stage, except that the magnitude of the number will be determined from the most significant bit (MSB). For example, Table #1 shows the first six values for k that would be generated in a 64-point FFT for the second stage. So only the first bit is kept and the rest of the bits in the number are set to zero. In general, the values for k from the second stage will toggle between 0 and N/4.
4. For the subsequent stages, the value of k is determined in a similar fashion. The number of bits that is kept is equal to the stage number minus 1. As an example, for the fourth stage, the 3 most significant bits would decide the magnitude of k.

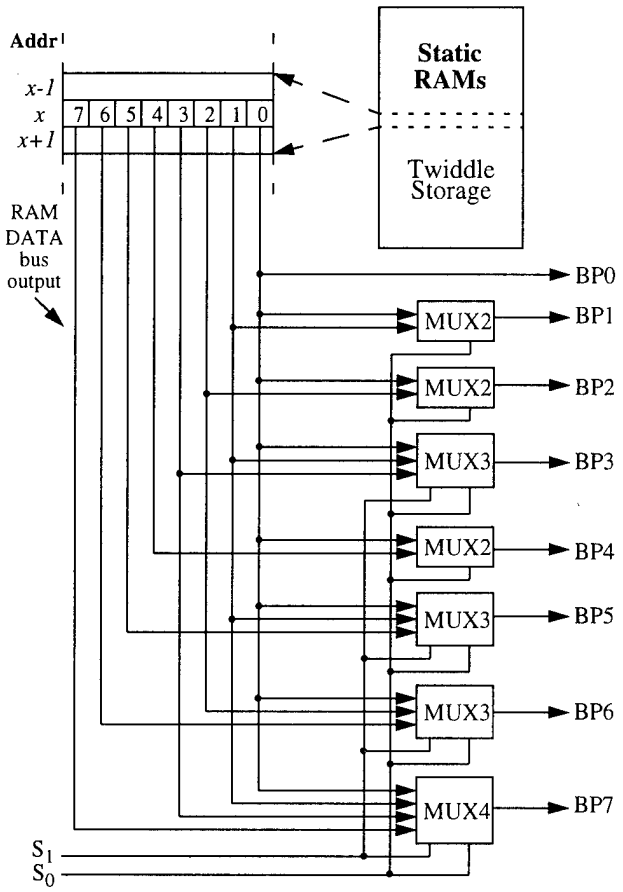

FIGURE 3-8. Twiddle factor generator

Normal representation	Bit-reversed representation	MSB magnitude
00000 (0)	00000 (0)	00000 (0)
00001 (1)	10000 (16)	10000 (16)
00010 (2)	01000 (8)	00000 (0)
00011 (3)	11000 (24)	10000 (16)
00100 (4)	00100 (4)	00000 (0)
00101 (5)	10100 (20)	10000 (16)

Table 1: Values of *k*

Once all the values for k have been established, then the twiddle factors can be calculated and stored in the static RAM, shown in Figure 3-8. N/2 twiddle factors are stored in the SRAM. They are stored in bit-reversed order in con-

secutive positions (0 through 7 in Figure 3-8) and in consecutive addresses, such that there are enough twiddle factors in one address to fill all eight BPs, if necessary. By only storing N/2 twiddle factors and not $(N/2)\log_2 N$, a large quantity of storage space is saved. Although if $(N/2)\log_2 N$ twiddle factors were stored, then the patterns necessary for each stage could be read out of the RAM directly, thus avoiding the need for extra circuitry to manipulate the twiddle factor data. However, the manipulation circuitry created for this design is extremely minimal compared to the excessive amount of area needed for the extra RAMs. It turns out that there is a nice regular pattern to the fashion in which twiddle factors are needed for the BPs. Eight different twiddle factors are not always needed for the eight different BPs. Fortunately, either only one twiddle factor is needed, or two, or four, or all four have to be different. Therefore, eight different ones are stored in one address of the RAM. And the multiplexers, shown in Figure 3-8, are selected such that the required number of different twiddle factors are sent to the BPs. So the combination of selecting the right address and setting the multiplexer select lines properly will provide the correct twiddle factors to the BPs.

3.5 The FFT System

The two basic elements of the FFT design are the PFFT and the PRAM. These two form a cascadable chip set. The system designer can choose however many are necessary for his system. The numbers can range from the fastest and largest design, which would be a pipelined system with $\log_2 N$ PFFTs and PRAMs, to the smallest and slowest configuration, which would be a single PFFT and two PRAMs. Any number of PFFTs and PRAMs in between those two extremes is also possible.

The smallest system would operate as follows, shown in Figure 3-9.

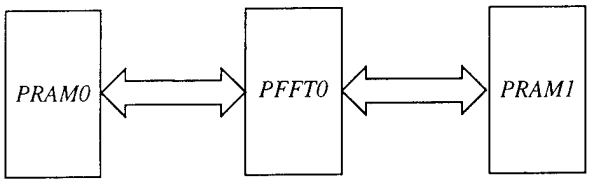

FIGURE 3-9. The low-cost system

1. PRAM 0 is filled with the initial data set.
2. The first stage of the FFT is calculated, sixteen points at a time through the PFFT, and the data is stored in PRAM 1.
3. The second stage of the FFT is performed, this time with data being read from PRAM 1 and the output stored in PRAM 0.
4. Steps 2 and 3 are repeated in a ping-pong fashion until enough passes have been completed to finish the FFT.

The multiple PFFT system is a variable sized pipelined structure as shown in Figure 3-10. It requires m PFFTs and

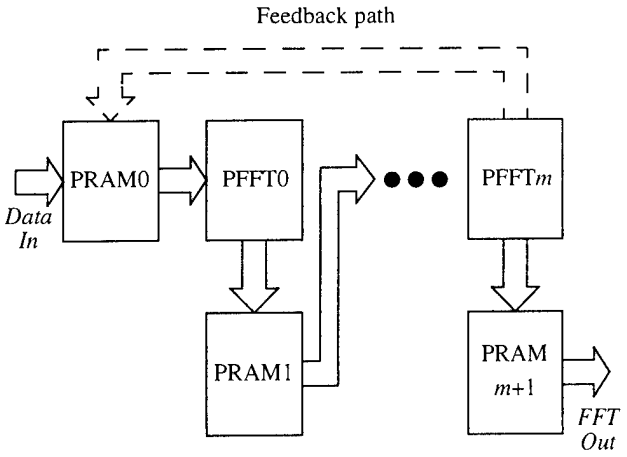

FIGURE 3-10. The high-performance system

$m+1$ PRAMs for maximum performance, where $m = \log_2 N$. The initial data set is stored in PRAM 0, and the final data is stored in PRAM $m+1$ or can be read directly from PFFT m. If, however, fewer than m PFFTs are chosen for the system, the data from the last PFFT will have to be "wrapped around" and stored in PRAM 0, as indicated by the dashed feedback line in Figure 3-10. The FFT process will continue in the original fashion, cycling through the available PFFTs as many times as are required for the successful completion of the calculation.

Normally, in the pipelined mode, the next stage will have to wait for the current stage to completely finish storing its data before the next stage can access that data. This will cause a bit of a lag in the flow of data. Be that as it may, maximum throughput and pipeline effectiveness can still be achieved in this setup by modifying the PRAM arrangement. In addition to the four subdivisions of RAM in each bank that was mentioned previously, an extra partition is needed. The odd-numbered addresses have to be separated from the even addresses. Since two different addresses in the same RAM cannot be accessed at the same time, a split is needed in order for the next stage to read data from the same RAM bank to which the current stage is writing data. In this fashion, the current stage can write data to the odd address while the next stage is reading data from the even address. And vice-versa. As a result, the next stage of the FFT doesn't have to wait for the current stage to complete its calculations before the next stage can start its own processing.

4. Chipset Design

Having established the theoretical operation of the but-

terfly processor and the FFT system, we now focus on the physical realization of the electronic circuitry and the optics. The following subsections describe the analog and digital integrated circuits and the optical setup.

4.1 Optical Transmitter and Receiver Circuits

A number of hybrid SEED receiver circuits have been designed and tested recently [19,20]. Experimental measurements on single-ended and two-beam transimpedance receivers have confirmed switching energies less than 60fJ and operation at data-rates in excess of 800Mb/s. The area of a simple transimpedance receiver circuit that uses one gain-stage and two parallel MOS transistors as the feedback element, is approximately $300\mu m^2$ in a 0.8μm 5V CMOS technology [19].

Current hybrid CMOS-SEED transimpedance receiver circuit designs typically consume 3-4mW of power operating at 5V with speeds in excess of 300Mb/s [19]. When large numbers of receivers are integrated on a single chip, this power dissipation must be accounted for in the power budget. For example, the 768 two-beam receivers used in the FFT chipset would dissipate 2.7W on-chip. If necessary, this value can be reduced by several means. First, the power consumption can be reduced by operating the receiver circuits at lower voltages (e.g. 3.3V). Because the FFT chip-set calls for 150Mb/s receivers, the receiver bandwidth can be traded-in for reduced power consumption. Finally, novel receiver designs may significantly reduce the consumption with only a small penalty in sensitivity [21].

The optical transmitter circuit is a CMOS inverter operating at 5V. The output of this inverter sees a pair of reverse-biased quantum well diode modulators as the capacitive load. With present the hybrid SEED process this capacitance is approximately 100fF [22], which is an order of magnitude smaller than the capacitance of flip-chip or perimeter pads used for electronic packaging. Lower capacitance translates directly into low on-chip power consumption. The dynamic power consumption per transmitter for the proposed chipset can be estimated using the following:

$$P_{diss} = \frac{1}{2}CV^2f = \frac{1}{2}(100fF)(5V)^2(150MHz) \qquad (4.1)$$

$$P_{diss} = 200\mu W$$

In addition, there will be an extra 200-300μW of power dissipation per transmitter due to the photocurrent flowing through the output driver when the modulator is in the absorbing stage. This leads to about 350mW of power consumption for the 768 transmitters used in our chipsets.

In summary, the chipset calls for 768 dual-beam optical receivers and 768 dual-beam optical transmitters per chip. These are arranged in a 48x64 array of quantum well diodes corresponding to a 48x32 array of transmitters and receivers. The floorplan for the proposed chipsets puts the quantum well diode array in the middle of the chip. The diode array uses a 96x64 array of pads which requires 3.8mm x 2.5mm of silicon area assuming 40μm pad pitch. Receiver amplifier and transmitter driver circuits are placed directly under the quantum well diode array. The power consumption of the entire receiver/transmitter section is approximately 3W per chip using existing transimpedance receivers. This can be reduced to 1-2W with receivers optimized for low power.

4.2 Optics Configuration

For typical smart pixel applications such as photonic switching, the cascaded optical connections between chips are strictly feedforward. Feedforward multi-chip optical systems have previously been demonstrated by combining polarization with space-division multiplexing [3] and polarization with pupil-division multiplexing [3]. Both of these optical systems are applicable to the multi-chip pipelined PFFT processor (system 2) and readers are referred to these papers for a detailed description. Because the PFFT processor uses only simple one-to-one connection, the use of a holographic optical interconnect is not required; this simplifies the system and reduces loss.

Most feedforward optical systems lack the flexibility to accomplish feedback or bi-directional communication. The three-chip smart-pixel PFFT processor (system 1) requires connections to (write cycle) and from (read cycle) the smart-pixel PRAM memory chip. Here we present one possible arrangement that uses polarization and space-division multiplexing, and can provide the required feedback as well as feedforward optical connectivity between photonic chips. Note that the connections are simple point-to-point optical connections between the FFT processors and corresponding RAM cells. No complex interconnect structure is necessary. Figure 4-1 shows an example of a telecentric optical system that can achieve this connectivity. Chips are

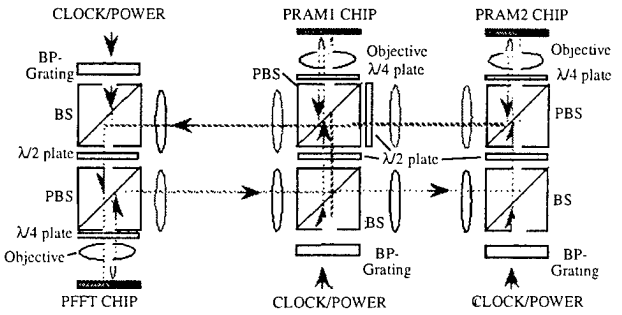

FIGURE 4-1. Optics system

connected using one path to place the arrayed optical readout beams from a PFFT chip onto the detectors of two of its associated PRAM chips, and a separate shared path to

image the outputs of the PRAM chips onto the PFFT chip. Simultaneously, the outputs of the chips are also split to their respective data I/O ports; these outputs can be used to feed another pair of PFFT-PRAM chips.

4.3 CMOS Building Blocks

All of the CMOS digital IC components used in our designs and discussed in this paper are from existing technology libraries. The PFFT chip design makes extensive use of 24-bit adder circuits. Each radix-2 butterfly processor in the PFFT chip uses six adders. With eight radix-2 BPs per chip, a total of 48 adders are used on the PFFT chip. Our adder design uses a carry-select architecture with a Manchester carry chain and can add two 24-bit fixed point numbers in 3ns [23,24]. It also determines an overflow condition automatically. Operating at 150MHZ, the adder consumes 6,980μW and requires126,000μm^2 of chip area, with 1053 transistors.

The edge-triggered flip-flop (or register) is another important building block of the PFFT chip. Each radix-2 BP in the PFFT chip uses 368 registers to pipeline the computation. With eight BPs per chip, a total of 2,944 registers are used on the PFFT chip. Operating at 150MHZ, the register consumes 150μW and requires 740μm^2 of chip area, with 34 transistors.

The most important circuit on the PFFT chip is the 24-bit multiplier circuit. Each radix-2 butterfly processor in the PFFT chip uses four multipliers. With eight radix-2 butterfly processors per chip, a total of 32 multipliers are used on the PFFT chip. Our multiplier design is a 2's complement pipelined multiplier that can multiply a 24-bit and a 16-bit fixed point number in under 5ns [23,24]. A modified Booth algorithm is used to produce a series of partial products, which are summed by a Wallace tree adder circuit. A Manchester carry chain is then used to generate the final product. A register is placed near the middle of the multiplication, allowing the multiplier module to produce results at a higher clock rate. The product is then produced one clock cycle later. Operating at 150MHZ, the multiplier consumes 46,900μW and takes up 600,000μm^2 of chip area, with 12,786 transistors.

High-speed static RAM (SRAM) circuits are used in both the PFFT and the PRAM chips. The PRAM chip uses sixteen banks of static RAM modules organized as 256 words, each word being 96 bits (256x96), to store the data points during the FFT computation. The PFFT chips uses two SRAM banks to store the twiddle coefficients, each bank being sized as 512x128. Our SRAM design uses static address decoding for fast access times, reduced power consumption and high density [25]. Bit storage is performed using conventional six-transistor circuit and current-mode amplifiers are used to amplify bit line signals. Tristate output drivers are used on the data output lines and they are controlled with an output enable signal. The cycle time is 5.5ns for the 512x128 (twiddle storage) SRAM and 5.1ns for the 256x96 (data storage) SRAM. Operating at 150MHZ, the 512x128 SRAM consumes 560mW and has the dimensions of 2.5mm x 3.3mm, with 406,628 transistors. The 256x96 SRAM consumes 328mW and has dimensions 1.8mm x 1.8mm, with 155,738 transistors.

4.4 Photonic RAM chip

The photonic RAM (PRAM) chip functions as an optical SRAM. It integrates sixteen 256x96 SRAMs on a single chip whose floorplan is shown in Figure 4-2. This yields a

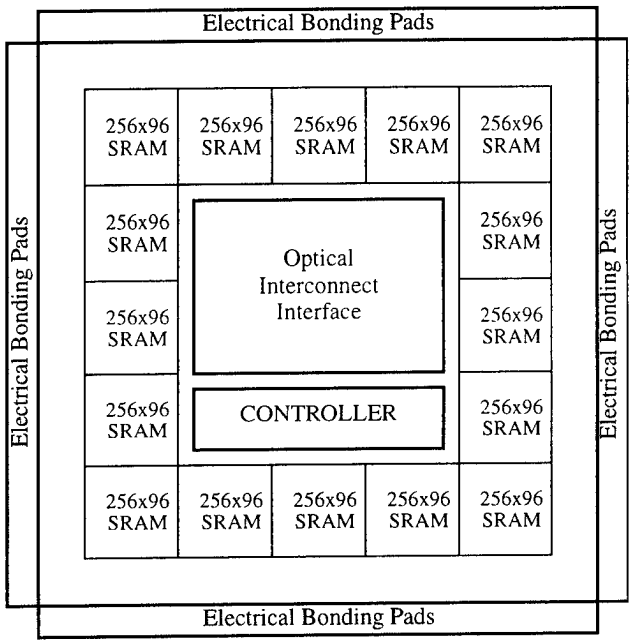

FIGURE 4-2. PRAM floorplan

sum of over 2.5 million transistors in an estimated 1cm x 1cm die area. The 768 optical inputs and 768 optical outputs are arranged as a 48x32 transmitter-receiver array in the center of the PRAM chip. The receiver amplifier and transmitter driver circuits are placed directly under the quantum well diode array. This floorplan allows for efficient wire routing between the SRAMs and the transmitter-receiver array.

The PRAM chip supports simultaneous READ and WRITE access to enable single-FFT and multi-FFT processor systems. In the single-FFT mode, the power consumption is reduced since only eight SRAMs out of sixteen are active at any single time. We estimate the on-chip power consumption at:

$$P_{diss} = P\left(optic\frac{I}{O}\right) + 8 \cdot P(256x96SRAM) = 5.72W \quad (4.2)$$

In the multi-FFT mode, twelve of the sixteen SRAMs are being accessed at the time. The on-chip power consumption

would then be:

$$P_{diss} = P\left(optic\frac{I}{O}\right) + 12 \cdot P(256x96SRAM) = 7.04W \quad (4.3)$$

4.5 Photonic FFT chip

The architecture of the radix-2 butterfly processor was described in section 3. The implementation uses a fixed-point 2's complement numeric format. It requires 70,136 transistors in a 1.9mm x 2.8mm area. A snapshot of the 0.5μm layout is shown in Figure 4-3. Power consumption is

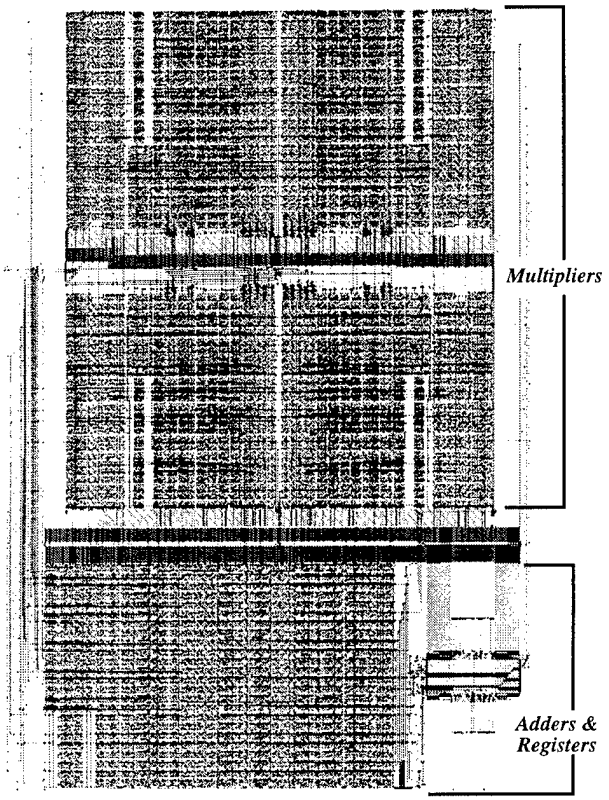

FIGURE 4-3. BP layout

estimated at 474mW operating at 150MHZ with 50% switching factor. The design is fully pipelined and can compute a new radix-2 butterfly in every clock cycle. The pipeline latency is 3 clock cycles. The processor has 96 inputs for two 48-bit complex numbers with 24-bit real and 24-bit imaginary parts. Similarly, 96 outputs are used for two 48-bit complex numbers. There are 32 input ports to bring in one 32-bit fixed-point complex twiddle coefficients with 16-bit real and 16-bit imaginary parts.

The photonic FFT (PFFT) chip integrates eight radix-2 butterfly processors and two 512x128 twiddle-storage SRAMs on a single chip. The floorplan of this chip is shown in Figure 4-4. The PFFT chip integrates over 1.4 million transistors in an estimated 1.2cm x 1.2cm die area.

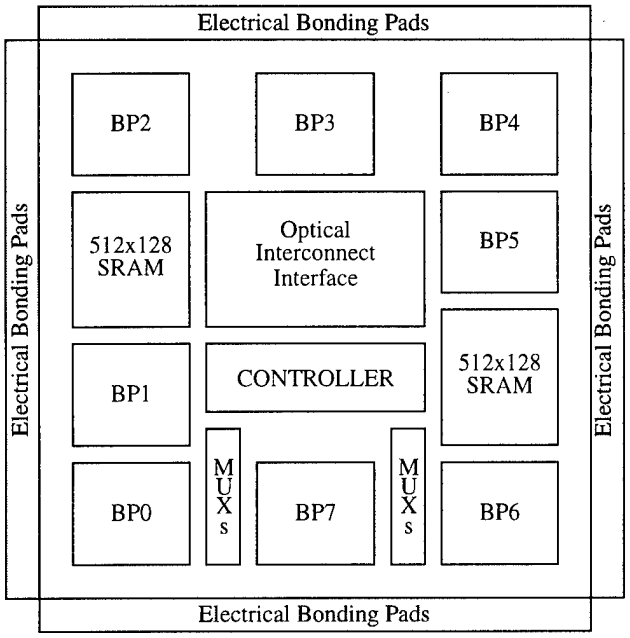

FIGURE 4-4. PFFT floorplan

The 768 optical inputs and 768 optical outputs are arranged as a 48x32 transmitter-receiver array in the center of the PFFT chip. The receiver amplifier and transmitter driver circuits are placed directly under the quantum well diode array. This floorplan allows for efficient wire routing between the eight processor modules and the diode array.

The PFFT chip operates in pipelined mode computing eight radix-2 butterflies every clock cycle. Thus on every clock cycle, 768 optical inputs are received and 768 optical outputs are transmitted. The twiddle coefficients required to compute the FFT are stored directly on the PFFT chip in two banks of 512x128 SRAMs. This memory capacity allows FFT sizes of up to 8,192 points to be computed. Twiddle coefficients are loaded electrically prior to computing the FFT. The power consumption for the PFFT chip is estimated at:

$$P_{diss} = P(optic\frac{I}{O}) + 8(P(BP) + 2P(512x128SRAM)) \quad (4.4)$$

$$P_{diss} = 8W$$

5. Performance Evaluation

Compared with electronic implementations, the photonic design described in this paper, provides higher chip pin-count and off-chip I/O bandwidth. Specifically, the PFFT and the PRAM chips have the following:

PINOUT = 8 (PEs) x [48*2 (inputs) + 48*2 (outputs)]
PINOUT = 1,536
BANDWIDTH = 1,536 x 150MHZ = 230,400Mbit/s
BANDWIDTH = 29Gbytes/s

which is an order of magnitude increase in off-chip bandwidth over conventional silicon ICs [26]. On-chip power density is less than 10 Watts/cm^2 and it is dominated by the switching of the internal electronic circuits.

The single PFFT system described in section 3.5 will now be referred to as system 1. Let us discuss the 8,192-point complex FFT, which is the maximum our design can handle. It requires 53,248 ((N/2)log$_2$N) radix-2 butterflies. Using our eight-processor FFT chip, we need a total of 53,248/8 passes, each taking up 6.7 ns (1/150MHz). This adds up to a total computation time of 44µs. For a 1,024-point FFT, 4.3µs is required. Table 2 compares the performance of our design with electronic FFT processors [27,28,29,30,31,32,33]. At the chip-level, the PFFT chip clearly outperforms electronic designs. At the board level, the performance advantage is not as clear. Since electronic systems have difficulty achieving 29Gbyte/sec interchip communication, they partition FFT computation to achieve maximum performance while keeping off-chip I/O within bounds of electronic packaging [27]. Typically, a radix-2 or higher butterfly is implemented on a single chip and data is fed to it from an SRAM. Then, to achieve higher performance, processors are arranged in pipelined fashion to execute the log$_2$N stages of the FFT computation [29].

Company	Part #	Type	1,024 FFT Benchmark	Cost
NEC	PD 77016	Chip	0.95ms	$32
Motorola	DSP56002	Chip	0.91ms	$44
Sproc	Sproc1210	Chip	0.9ms	$42
Zoran	Z89321	Chip	0.88ms	$42
Analog Devices	AD21060	Chip	0.46ms	$300
TI	TMS320C80	Chip	160µs	$400
TI	TMS320C6201	Chip	70µs	$100
Plessey	PDSP16510	Chipset	96µs	$2,000
Sharp	LH9124	Chipset	80µs	$1,000
Butterfly DSP	BDSP9124	Chipset	64.6µs	Not Available
Valley	UltraDSP	Board	80µs	$33,000
CRI	CRP1M40	Board	81µs	$10,000
CRI	CRCFV1M40	Board	31µs	>$50,000
Photonics	Low-cost	Chipset	4.3µs	
Photonics	High-perf.	Chipset	0.44µs	

TABLE 2. Performance comparison of FFT processors

The performance of an electronic board-level FFT processor can equal and even exceed our system 1 design. However, the electronic solution requires many more chips to achieve this. For example, an 8,192-point electronic FFT processor takes thirteen radix-2 processor chips (log$_2$8192=13) and 26 SRAM chips (using 48-bit wide SRAMs). This means that we are reducing system chip count from 39+ chips down to three chips by utilizing smart pixels. This reduction in chip count leads to systems with smaller size and lower power consumption.

To build a higher-performance smart pixel FFT processor, we can operate multiple photonic FFT and RAM chips in a pipelined fashion, as described in section 3.5. In this approach, the latency remains the same, while the throughput increases dramatically. This system, called system 2, can achieve an order-of-magnitude performance increase with a corresponding increase in hardware cost. For the 8,192-point complex FFT, there would be thirteen PFFTs and fourteen PRAMs for a total of 27 chips. Unlike system 1, where it is necessary to wait for the data to "ping-pong" back and forth before a new FFT can be calculated, system 2 is a straight-through pipeline, in which a new FFT is calculated every time a complete pass is made on the last stage. The resulting throughput is given by [(# of butterflies per stage)/8] * 6.7ns = (4096/8) * 6.7ns = 3.4µs. Which means that a new FFT is computed every 3.4µs. For a 1,024-point complex FFT, 0.44µs is required. The performance of this system exceeds all electronic FFT processor designs. One important consideration for pipelined systems is that their external bandwidth requirements are increased as well. Thus, these types of systems are useful in focal plane arrays where sensor data can be captured and passed to the processor array without creating a bottleneck.

6. Discussion and Conclusions

The design presented in this paper offers a greatly flexible, high-performance, low chip-count solution to the numerous applications that require a high-speed FFT calculation. Our design uses fixed-point complex number arithmetic. To increase precision, a simple modification, called block-floating point, can be added to our chipset [27]. On the other hand, a true floating-point implementation would significantly increase the complexity and transistor count of the PFFT chip.

The performance benchmarks show our design (system 1) to be the fastest in the lower cost and chip count categories. Specifically, we can compute a 1,024-point complex FFT in 4.3µs using a system with one PFFT chip and two PRAM chips. An electronic implementation that combines a single Sharp LH9124 processor chip with SRAM and glue-logic chips requires 87µs for the same computation [27].

The performance of our design (system 2) improves as compared with electronic implementations with a corresponding increase in chip count. Specifically, we can com-

pute a new 1,024-point complex FFT in every 0.44μs using a fully pipelined system with ten PFFT chips and eleven PRAM chips. A high-performance electronic system that uses four Sharp LH9124 FFT processor chips, twelve Sharp LH9320 address generator chips, twelve SRAM chips, and various glue-logic chips requires 31μs for the same computation [30]. More importantly, when multiple chips are connected to compute large FFTs, our chipset offers much higher performance than electronic solutions due to higher inter-chip bandwidth that is made possible with optical interconnects.

In addition, the designer can tailor the PFFT/PRAM chipset to fit his needs for speed and size. As it stands now, systems 1 and 2 can compute from a minimum of a 16-point FFT all the way to an 8,192-point FFT, with any power of 2 value between these extremes. Larger-point FFTs can be achieved without modifying the PFFT chip. Only enhancements to the PRAM are necessary with the appropriate scaling. For example, a 16,384-point FFT is possible by doubling the memory capacity. One way to achieve order-of-magnitude higher capacity PRAM chips is by using electronic 3-D memory stacking technology [34]. Higher performance FFTs can be achieved by increasing the number of radix-2 BPs on the PFFT chip. For example, doubling the number of radix-2 BPs on the PFFT chip, doubles the performance while doubling the number of off-chip optical IOs.

We have presented an implementation of our design using hybrid CMOS-SEED technology. Since our design uses direct, one-to-one interconnections between the PRAM and the PFFT chips, it is compatible with a number of emerging three-dimensional free-space optoelectronic packaging and device technologies [5,6,8]. Other partitioning choices to perform the FFT are possible and were not considered here [35,36].

Acknowledgments

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Hybrid Integration of Smart Pixel with Vertical-cavity Surface-emitting Laser Using Polyimide Bonding

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Abstract

We have developed a new three-dimensional integration technology which involves hybrid integration of photonic and electronic circuits by means of polyimide bonding. To demonstrate this technology, a vertical-cavity surface-emitting laser (VCSEL) and metal-semiconductor-metal photodetector arrays were fabricated on a Si substrate. The photoresponsivity of the photodetector was 0.3 A/W. The threshold current of the VCSEL was 3.1 mA and the maximum output power was 2.45 mW for a 15-μm-diameter mesa at 20 °C. The VCSEL was not lasing above 90 °C. The calculation shows the thermal resistance for the proposed hybrid structure strongly depends on the polyimide thickness. The difference in active layer temperature between the hybrid and monolithic structures is within 10 K when the thickness of the polyimide is less than 0.1 μm and the electrical power consumption is 30 mW. We also calculated the power consumption and the maximum number of pixels per chip. A lower threshold current of the VCSELs and a lower bias voltage to the Si-CMOS circuit are desired to obtain a higher I/O throughput device.

Key Words

Vertical cavity surface emitting lasers, Integrated optoelectronic circuits, Optical interconnects, Smart pixels

INTRODUCTION

The need to fabricate smart pixels that integrate a photonic circuit with an electronic circuit has recently been increasing, because the integration of an electronic circuit allows the implementation of many smart functions and a high bit-rate response. Flip-chip solder-bonding is one way to fabricate this kind of device. For example, the integration of GaAs-AlGaAs MQW modulators and detectors with a Si-CMOS circuit has been demonstrated in hybrid-SEED technologies [1,2]. These devices have shown great potential for use in optical interconnections and photonic switching networks. The integration of vertical-cavity surface-emitting lasers (VCSELs) with electronic circuits is also an important technology for fabricating smart pixels because they do not need a bias light. Furthermore, a VCSEL provides a good match with electronic circuits because it operates at a low voltage and a low current [3]. Thus, many smart pixels integrated with VCSEL have been demonstrated [4-7]. The integration of VCSELs and photodetectors with GaAs electronic circuit presents few difficulties to fabricate in monolithic structure [4], and can also be done by means of hybrid integration using such techniques as flip-chip bonding, epitaxial lift-off with a transfer diaphragm [5], or a thinned and drilled CMOS wafer [6]. However, it would be more difficult to integrate both VCSELs and photodetectors on Si electronic circuits, because the two elements have non-planar structures. Furthermore, these technologies require the alignment of VCSELs with Si-CMOS circuits. This also increases costs and lowers the yield.

To overcome these problems, the technology for hybrid integration of Si electronic circuits and photonic circuits needs to satisfy the following conditions:

i) low-temperature process, <400 °C,
ii) integration with the uneven surface of Si electronic circuits,
iii) precision alignment between Si electronic circuits and photonic circuits,
iv) high-density integration of multiple devices,
v) wafer-scale integration process.

We propose a new integration technology for fabricating the smart pixels, consisting of VCSELs and photodetectors on a Si-CMOS circuit [7]. Photonic elements are bonded on the Si-CMOS circuit with a polyimide and electrically connected by the electroplated gold. The advantages of our new fabrication technology are as follows. The integration does not require any alignment before wafer bonding. This integration technology is a wafer-scale fabrication process that produces multiple devices simultaneously. So, these features are good as regards high yield and low cost. The fabrication process for the photonic circuits is the same as that used for our monolithically integrated smart pixel [4]. The photolithography for fabricating the photonic circuit employs marks on the Si substrate. The accuracy of the positioning of the Si-CMOS circuit with the photonic

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circuit is, therefore, determined by the accuracy of the photolithography.

Using this technology, we have fabricated an array of metal-semiconductor-metal (MSM) photodetectors on a Si substrate. We obtained a photoresponsivity of 0.3 A/W. We have also fabricated the VCSEL array on a Si substrate. The threshold current of the VCSEL was 3.1 mA and the maximum output power was 2.45 mW for a 15-μm diameter mesa. We calculated the thermal resistance of our proposed hybrid structure. The temperature difference in the active layer of the VCSELs between the hybrid and monolithic structures was within 10 K when the polyimide thickness was less than 0.1 μm and the applied electrical power consumption was 30 mW. We also calculated the power consumption of the smart pixel. A low threshold current of the VCSEL and a low applied voltage of the CMOS circuit is important to obtain a high-density device with a high bit rate.

Device structure and fabrication process

The structure of the proposed hybrid smart pixel is shown in Fig. 1. The VCSEL and the photodetector are bonded onto a Si-CMOS chip by using the polyimide. The InGaP etch-stop layer is used to obtain the clean and flat surface of the MSM photodetector. The vertical electrical interconnection between the electronic circuit and the photonic circuit is electroplated gold. The gold electrode under the VCSEL is for reducing the thermal resistance.

The device fabrication process is shown in Fig. 2. A GaAs epitaxial wafer is spin-coated with polyimide and the bonding pads for three-dimensional contacts on the Si substrate are deposited. The GaAs and Si-CMOS wafers are pushed together and heat treated at 200 °C for 1 hour under pressure (Fig. 2(a)).

Next, the GaAs substrate is removed by using a PA solution (H_2O_2:NH_3OH), and etching is stopped at the $Al_{0.6}Ga_{0.4}As$ etch-stop layer. The $Al_{0.6}Ga_{0.4}As$ etch-stop layer is removed by using H_2SO_4:H_2O_2:H_2O solution, and the etching is stopped at the InGaP etch-stop layer. To obtain the clean and flat surface of the n^+-GaAs contact layer, the InGaP etch-stop layer is removed by using HCl:H_2O solution. As shown in Fig. 2(b), only the GaAs epitaxial layers remain on the Si-CMOS wafer. Then, we divide the GaAs epitaxial layer into chip-size sections, typically 2 x 2 mm^2. The photolithography for sectioning the wafer is done with an IR lamp and a camera so that we can see the marks on the Si-CMOS wafer through the GaAs epitaxial layers. The photolithography for fabricating the VCSELs and MSM photodetectors employs the marks on the Si-CMOS wafer. This is why the accuracy of the positioning between the photonic and electronic circuits is determined by the accuracy of the photolithography. Then, the wafer is heat treated at 350 °C for 5 hours.

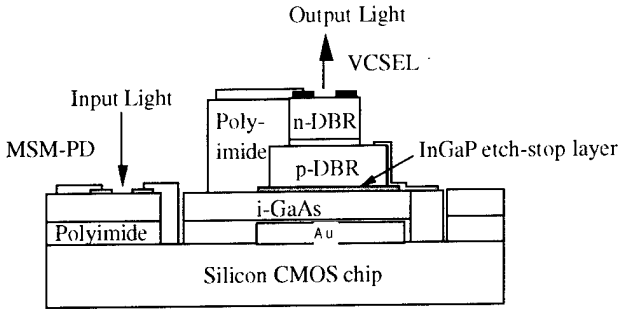


Figure 1. Structure of proposed hybrid smart pixel.

The next step is to fabricate the photonic devices, as shown in Fig. 2(c). The mesas are formed by ECR-reactive ion beam etching with Cl_2. Ni/Zn/Au p-contact and AuGe/Ni n-contact metals are evaporated, in turn. To get the ohmic contacts the wafer is annealed at 420 °C for 30 sec. Then the MSM photodetector is formed on the i-GaAs layer. The clean and flat surface of the i-GaAs layer is obtained by selective chemical wet etching using the InGaP layer.

Then, reactive ion beam etching with O_2 is used to remove the polyimide from the Si substrate except for the polyimide underneath the VCSEL mesas. Silicon nitride is deposited at 300 °C, and windows for the output light and three-dimensional contacts are opened by reactive ion beam etching with CF_4. We form three-dimensional contacts between the p-type contact of the VCSELs and the bonding pads on the Si-CMOS wafer with electroplated gold. Finally, we form the common contact both of the n- type contacts of VCSELs and the Schottky contact of the MSM photodetectors by using the polyimide and electroplated gold, as shown in Fig. 2(d).

This method is, therefore, a wafer-scale fabrication

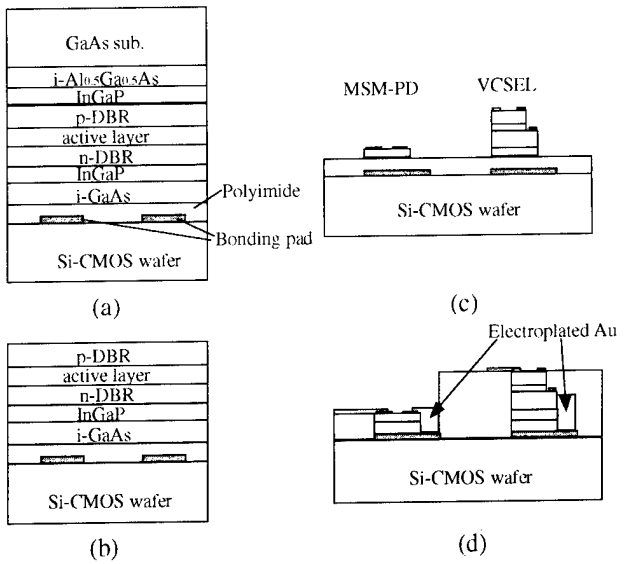


Figure 2. Schematic diagram of the device fabrication processes: (a) Bonding of GaAs wafer and Si substrate with polyimide, (b) removal of GaAs substrate with PA solution, (c) fabrication of photonic devices, and (d) fabrication of three-dimensional contacts.

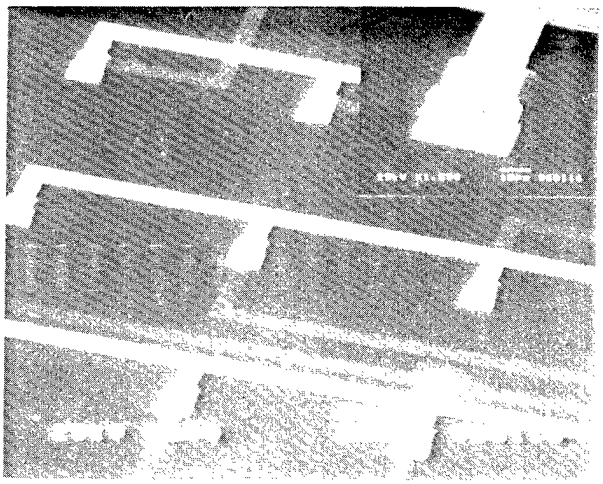


Figure 3. SEM image of a hybrid MSM photodetector array.

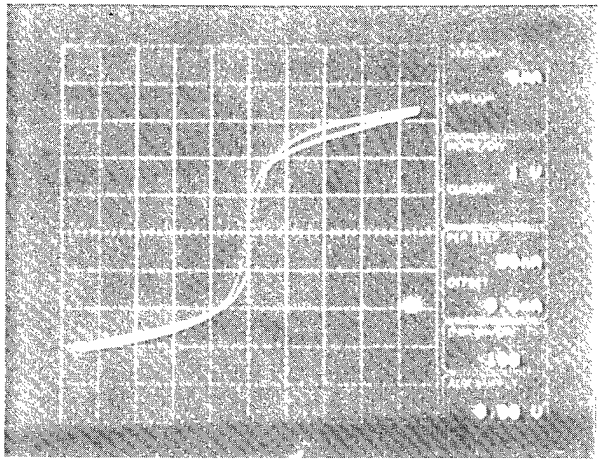


Figure 4. I-V characteristics of an MSM photodetector.

process and produces multiple devices at the same time. Furthermore, this method provides good yield and has a low cost. To demonstrate this technology, we fabricated the MSM photodetector and VCSEL arrays on a Si substrate.

Experimental Results

MSM photodetector array

The MSM photodetector and etch-stop layers were deposited by molecular beam epitaxy. The etch-stop layer contained a 0.5-μm-thick $Al_{0.6}Ga_{0.4}As$ layer and the absorption layer contained a 2-μm-thick i-GaAs layer.

Figure 3 is an SEM image of a hybrid MSM photodetector array. Each device is separated by 250 μm. The GaAs mesa is 25 x 25 μm^2 and the optical window is 20 x 20 μm^2. The fingers are 1-μm wide and the spacing is 2 μm. The gold electrodes were deposited on the polyimide and the silicon substrate. Schottky contacts

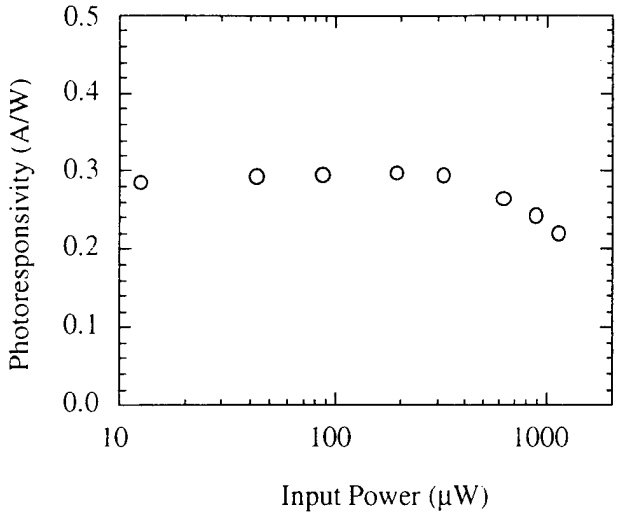


Figure 5. Dependence of MSM photodetector photoresponsivity on input power.

were formed by Ti/Pt/Au. The three-dimensional contacts between the Schottky contacts of the photodetectors and the bonding pads on the Si substrate were electroplated gold.

Figure 4 shows the I-V characteristics of an MSM photodetector. The input power was 40 μW. The wavelength of the input light was 850 nm. The dark current was 0.35 pA at a bias voltage of 3 V.

Figure 5 shows the dependence of the MSM photodetector photoresponsivity on input power. The photoresponsivity remained level at 0.3 A/W up to an input power of 300 μW, and then fell off. The deviation of the photoresponsivity was ±13.8 % in a 4 x 4 array.

VCSEL array on Si substrate

The VCSEL and etch-stop layers were deposited by metal organic chemical vapor deposition. The etch-stop layers contained a 0.5-μm-thick $Al_{0.6}Ga_{0.4}As$ layer and a 0.1-μm-thick InGaP layer. The VCSEL layers contained a Si-doped distributed Bragg reflector (DBR) consisting of 19.5 pairs of $Al_{0.15}Ga_{0.85}As$/AlAs layers and a C-doped DBR consisting of 35 pairs of $Al_{0.15}Ga_{0.85}As$/AlAs layers with a 10-nm-thick intermediate $Al_{0.6}Ga_{0.4}As$ layer. The active layer consisted of six GaAs quantum wells confined by a space layer of $Al_{0.3}Ga_{0.7}As$. The total thickness of the VCSEL layers was about 8 μm.

An SEM image of a hybrid VCSEL array is shown in Fig. 6. Each VCSEL is separated by 250 μm. The upper-mesa diameter is 15 μm and the lower mesa is 50 x 50 μm^2. The electroplated gold on the polyimide layer was the common electrode for n-type contacts. The gold electrodes on the Si substrate were used to control the bias voltage to the VCSELs. The three-dimensional contacts between the p-contacts of the VCSELs and the bonding

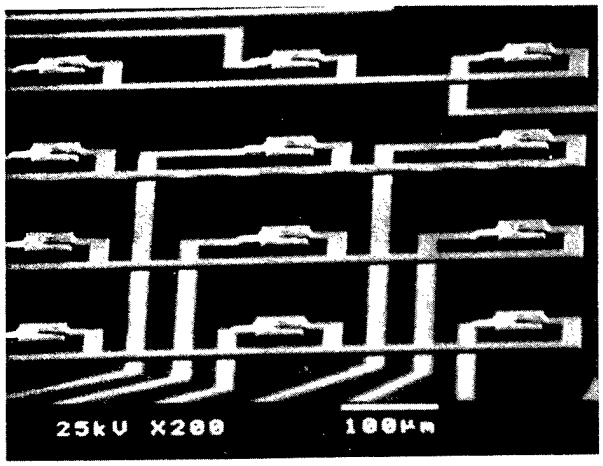


Figure 6. SEM image of a hybrid VCSEL array.

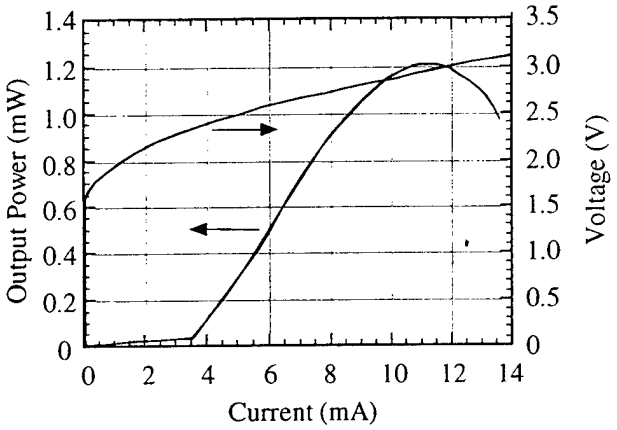


Figure 7. I-L and I-V characteristics of a VCSEL which has a 15-micron diameter.

pads on the Si substrate are electroplated gold.

Figure 7 shows the I-L and I-V characteristics of a VCSEL which has a 15-μm diameter. The threshold current was 3.3 mA and the maximum output power was 2.38 mW. The wavelength was about 865 nm. The threshold voltage and resistance at the threshold were 2.2 V and 150 Ω. This higher resistance was due to the contact resistance of the p-type contact on the p-DBR layer. To decrease a resistance, the p^+-GaAs contact layer is required under the p-DBR layer.

The I-L characteristics are shown in Fig. 8, as a function of device diameter. The threshold current increased from 2.7 mA to 7.9 as the diameter increased from 10 μm to 25. The maximum output power also increased from 1.05 mW to 5.4 with an increasing device diameter.

Figure 9 shows the threshold current density dependence on the device diameter. The threshold current density was about 1.6 kA/cm^2 when the device diameter was more than 20 μm. However, when the diameter was less than 15 μm, the threshold current density abruptly increased with a decreasing device diameter. This abrupt increase in the threshold current

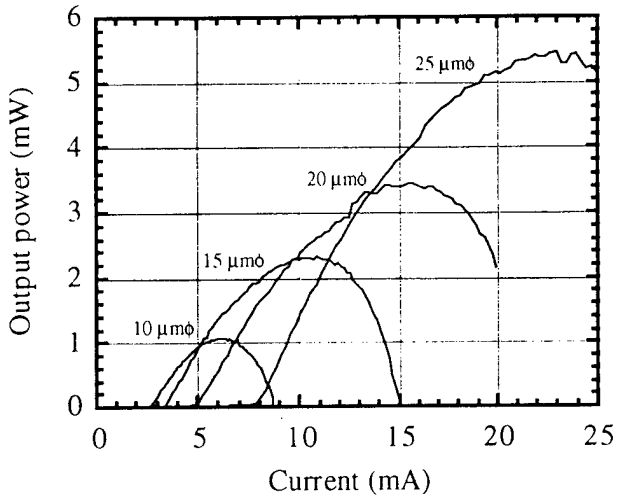


Figure 8. I-L characteristics of VCSEL as a function of device diameter.

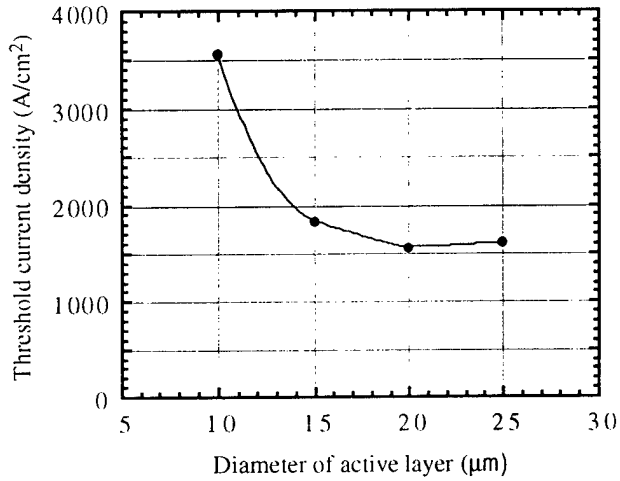
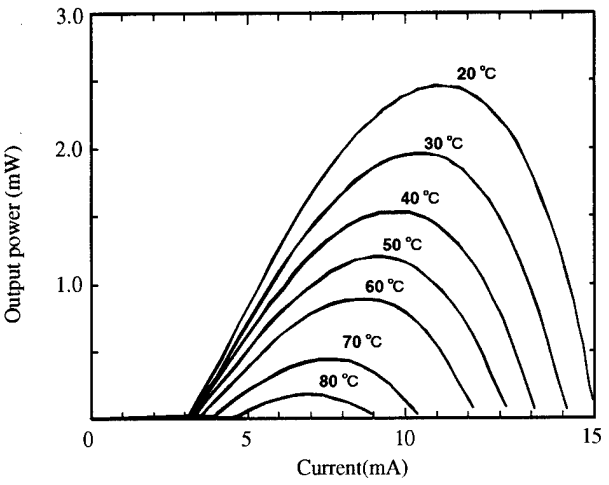


Figure 9. Threshold current density dependence on the device diameter.

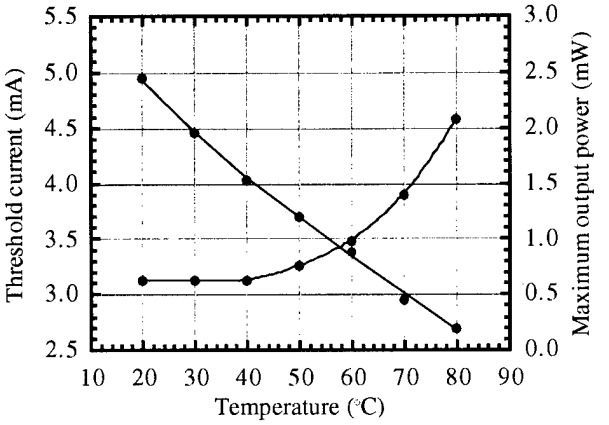
density is due to the increase of the electrical resistance and thermal resistance.

The temperature dependence of I-L characteristics is shown in Fig. 10 (a). The device diameter was 15 μm and the lasing wavelength was about 865 nm. The threshold current was 3.1 mA and the maximum output power was 2.45 mW at 20 °C. The output power decreased and the threshold current increased with the increasing temperature. The device was not lasing above 90 °C.

Figure 10 (b) shows the temperature dependence of the threshold current and the maximum output power. The threshold current was maintained at 3.1 mA when the temperature was increased from 20 °C to 40. Then, threshold current increased to 4.6 mA as the temperature increased to 80 °C. The maximum output power, however, was strongly dependent on the temperature: it decreased from 2.45 mW to 0.18 when the temperature was increased from 20 °C to 80. The thermal resistance was about 1800 K/W and was estimated from the change



(a)



(b)

Figure 10. (a) Temperature dependence of I-L characteristics, (b) temperature dependence of the threshold current and the maximum output power.

in the lasing wavelength when the electrical power consumption applied to the VCSEL was changed. We used the value of 0.0068 nm/°C when we estimated the thermal resistance [8]. This value was 1.8 times higher than that of the VCSEL fabricated on the GaAs substrate.

The dependence of the thermal resistance on the polyimide thickness is shown in Fig. 11. The thickness of the polyimide layer changed from 0.25 μm to 1.4 in the same chip. The lasing wavelengths of the measured VCSELs had almost the same value of 863 nm. The thermal resistance increased from 1600 K/W to 2900 with an increasing polyimide thickness. In the next section, we will calculate the thermal resistance.

Discussion

Calculation of Thermal Resistance

We calculated the thermal resistance using simple models, as shown in Fig. 12 [9]. Figure 12 (a) is for the hybrid structure. It consists of an active layer, a DBR and GaAs

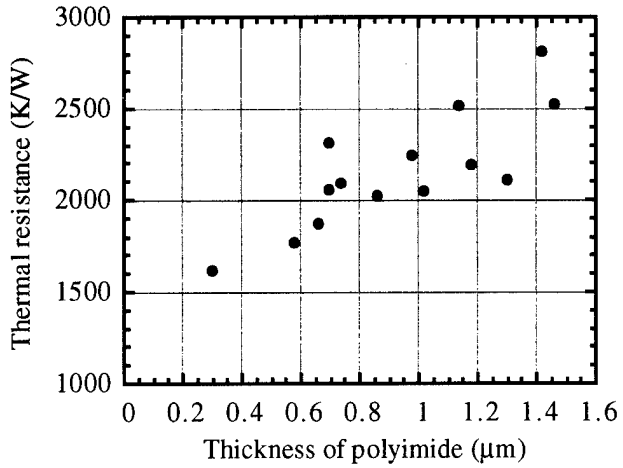


Figure 11. Thermal resistance depending on the polyimide thickness.

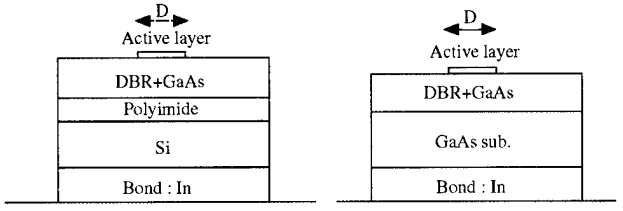


Figure 12. Calculation model of thermal resistance; (a) for the hybrid structure, (b) for the monolithic structure.

layers, a polyimide layer, a silicon wafer, an indium layer, and a heat sink. Figure 12(b) is for the monolithic structure. It consists of an active layer, a DBR layer, a GaAs substrate, an indium layer, and a heat sink. For simplicity, we assume that heat was generated only in the active layer.

We also assume that the thermal conductivity is 0.44 W/cm/K for the DBR and GaAs layers, 0.0018 for polyimide, 0.98 for the silicon substrate, 0.44 for the GaAs substrate, and 0.87 for indium.

Figure 13 shows the dependence of the calculation results of the thermal resistance on the diameter of the active layer. The dashed lines are for the hybrid structure. It assumes that the DBR and the GaAs layers have a combined thickness of 5 μm, the silicon wafer, 500, and the indium layer, 10. The solid line is for a monolithic structure on a 200-μm-thick GaAs substrate. As can be seen, the thermal resistance drops as the active layer gets wider. It's also greater for the hybrid structure.

Figure 14 shows how the ΔT changes as the polyimide thickness increases. We defined ΔT as the difference in the active layer temperature between the hybrid and monolithic structures when the same electrical power was applied. For the calculations, we assumed that the diameter of a VCSEL was 15 μm, that the combined

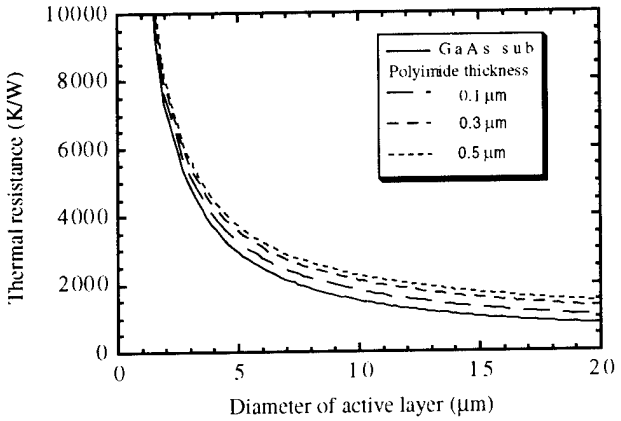


Figure 13. Calculation results of the thermal resistance depending on the diameter of the active layer. The dashed lines are for the hybrid structure. The solid line is for a monolithic structure on a 200-μm-thick GaAs substrate.

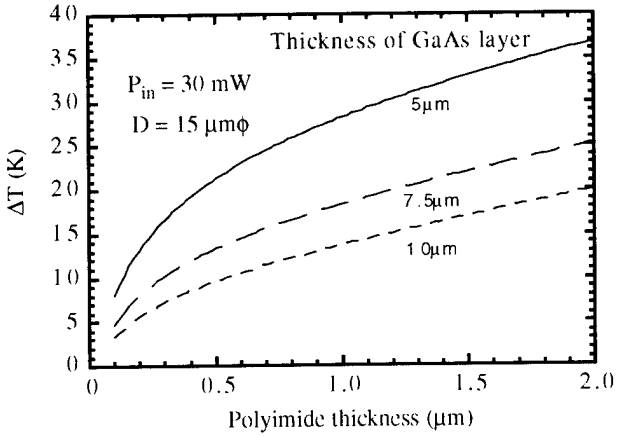


Figure 14. Polyimide thickness dependence of ΔT. We defined ΔT as the difference in the active layer temperature between the hybrid and monolithic structures when the same electrical power was applied.

thickness of the DBR and GaAs layers was changed from 5 μm to 10, that the electrical power consumption was 30 mW, and that the other parameters were the same as before. The ΔT and the dependence of the polyimide layer thickness in ΔT decreased with the increasing combined thickness of the DBR and GaAs layers. The decrease in the dependence of the polyimide thickness for ΔT is important to obtain the good uniformity of the VCSEL characteristics. When the thickness of the polyimide layer is smaller than 0.1 μm, the temperature rise in the active layer is within 10 K of that for the monolithic structure. This shouldn't be a serious problem for VCSELs because they consume very little electrical power.

Power Consumption and Packing Density

Finally, we will discuss the dependence of the power consumption on the operating frequency of a smart pixel that uses a VCSEL. This is important because it limits the number of pixels per chip.

The power consumption of the smart pixel PC_{total} is given by

$$PC_{total} = PC_{IC} + PC_{LD} + PC_{PD}\ , \qquad (1)$$

where PC_{IC} is the power consumption of the Si-CMOS circuit, PC_{LD} is the power consumption of the VCSEL and MOS transistor which are connected in series with the VCSEL, and PC_{PD} is the power consumption of the photodetector.

The power consumption of the Si-CMOS circuits is given by

$$PC_{IC} = \alpha f C V_{DD}^2\ , \qquad (2)$$

where α is the probability that a power-consuming transition occurs, f is the operation frequency, C is the loading capacitance which depends on the gate number of the CMOS circuit in one pixel, and V_{DD} is the voltage to the Si-CMOS circuits. When we assumed the 0.5-μm design rule for Si-CMOS circuits, the power consumption was proportional to 3 μW/MHz/gate at a supply voltage of 3 volts.

For a lower VCSEL power consumption, a lower bias current to the VCSEL is better. Thus, we assume that the bias current changes with the operation frequency. When the operation frequency is more than 100 MHz, the operation frequency is limited by the lasing delay time. The bias current to the VCSEL must be, therefore, increased with the increasing operation frequency. We assume that the lasing delay time t_d is less than $0.1/f$ to obtain error-free operation [10].

The lasing delay time t_d is given by

$$t_d = \tau_n \ln \frac{I_p - I_b}{I_p - I_{th}} \quad (I_b < I_{th}), \qquad (3)$$

where τ_n is the electron lifetime, I_p is the peak current to the VCSEL, I_b is the bias current, and I_{th} is the threshold current of the VCSEL.

From (3), the bias current to the VCSEL depending on the operation frequency is thus given by

$$I_b = I_p - \left(I_p - I_{th}\right) e^{\frac{0.1}{\tau_n f}}\ . \qquad (4)$$

The power consumption of a VCSEL and a MOS transistors, which connects to a VCSEL in series, is given by

$$PC_{LD} = \left\{I_b + \beta\left(I_p - I_b\right)\right\} V_D - \beta \eta_S \left(I_p - I_b\right) V_{LD,ON}\ , \qquad (5)$$

where V_D is the bias voltage, β is the probability that a VCSEL is in the bright state, η_S is the slope coefficient, and $V_{LD,ON}$ is the voltage across the VCSEL in the bright state. In this equation, the power converted to the light is subtracted because this power does not affect the thermal condition.

The power consumption of the MSM photodetector is given by

$$PC_{PD} = \gamma \eta_{PD} \eta_F \eta_S \left(I_p - I_b\right) V_{MSM}\ , \qquad (6)$$

Table I. Parameters used in calculations

CMOS circuit	VCSEL	MSM-PD
Number of gates: 25 V_{DD} = 1 or 3 V α = 0.3	Number of VCSELs : 2 η_S = 0.32 W/A [8] V_D = 3 V $V_{LD,ON}$ = 2.5 V τ_n = 2ns I_{th} = 1 or 2 mA I_p = 4 or 5mA β = 0.25	Number of PDs : 2 η_{PD} = 0.3 A/W η_F = 0.275 [11] V_{MSM} = 3 V γ = 0.25

where γ is the probability that the signal light is incident on an MSM photodetector, η_{PD} is the photoresponsivity of the detector, η_F is the coupling coefficient in the optical circuit between the VCSEL and the MSM photodetector, and V_{MSM} is the voltage to the photodetector.

Calculation conditions are listed in Table I. We assumed that one pixel contains 25 gates in the CMOS circuit, two VCSELs, and two photodetectors. The total current is 5 and 4 mA for threshold currents of 2 and 1 mA, respectively.

Figure 15 shows power consumption versus clock frequency. For a threshold current of 2 mA, the power consumption of a VCSEL is constant when the operating frequency is under 90 MHz. For a threshold current of 1 mA, the operating frequency also constant under 170 MHz. So, a VCSEL consumes more power at higher operating frequencies because the bias current is larger.

The power consumption of the CMOS circuit is proportional to the increase in the operating frequency and strongly depends on the bias voltage. As can be seen, at lower frequencies, the main contribution to the total power consumption comes from the VCSELs. At higher frequencies, it comes from the CMOS circuit.

Using these results, we can estimate the maximum number of pixels per chip for a 1-cm^2 area. Figure 16 shows the dependence of the maximum number of pixels in one chip on the operating frequency for two cases: i) a threshold current of 2 mA, a peak current of 5 mA, and a CMOS supply voltage of 3 volts, ii) the respective values are 1 mA, 4 mA, and 1 volt. We assumed that the cooling rate was 10 W/cm^2. When the operating frequency is under 100 MHz, the maximum number doesn't change because the power consumption is determined by the peak current to the VCSELs. Above that frequency, the number gradually drops. When we operate at the frequency of 1 GHz, the maximum number of pixels is 270 for case i) and 900 for case ii). So, in order to obtain a high-density array, we need a low threshold current while maintaining the wall-plug efficiency of the VCSELs, and also a low CMOS supply voltage.

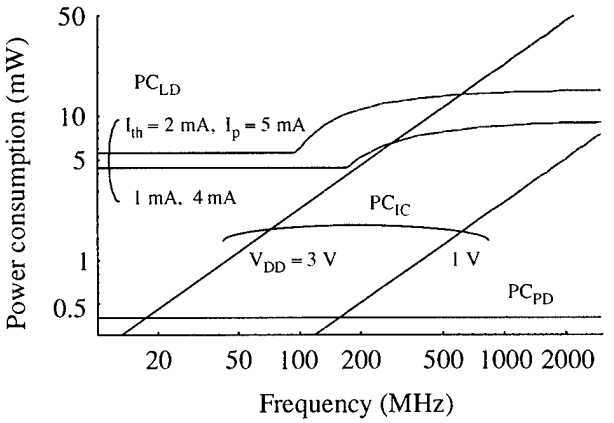


Figure 15. The dependence of the power consumption of one pixel on the clock frequency. We assumed that one pixel contains 25 gates in the CMO S circuit, two VCSELs, and two photodetectors. The total current is 5 and 4 mA for threshold currents of 2 and 1 mA, respectively.

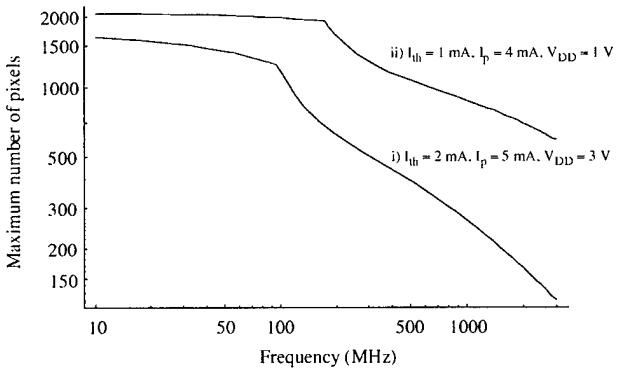


Figure 16. Maximum number of pixels varies with the operating frequency for two cases; i) a threshold current of 2 mA, a peak current of 5 mA, and a CMOS supply voltage of 3 volts, ii) the values are 1 mA, 4 mA, and 1 volt. We assumed that the cooling rate was 10 W/cm^2.

Summary

In summary, we proposed a smart pixel consisting of a hybrid structure of photonic circuits and Si-CMOS circuits, constructed by using polyimide bonding. To demonstrate this technology, we fabricated the MSM photodetector and VCSEL arrays on the Si substrate. The MSM photodetector shows the photoresponsivity of 0.3 A/W. In the VCSEL array, the threshold current was 3.1 mA and the maximum output power was 2.45 mW for a 15-μm-diameter mesa. These results show that hybrid integration technology using polyimide bonding is suitable for fabricating the VCSEL-based smart pixel.

We calculated the thermal resistance compared with the hybrid structure and the monolithic structure. The thermal resistance strongly depends on the polyimide thickness. We also calculated the power consumption and the maximum number of pixels per chip. We found that a lower threshold current of the VCSELs and a lower bias voltage for the Si-CMOS circuit are desired to obtain a higher I/O throughput device.

Acknowledgments

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Demultiplexing 2.48 Gb/s Optical Signals with a Lower-Speed Clocked-Sense-Amplifier-Based Hybrid CMOS/MQW Receiver Array

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Abstract

Eight 311 Mb/s data streams are extracted from a 2.48 Gb/s optical signal with a lower-speed 0.35 μm CMOS receiver array. The array consists of 16 clocked-optical receivers based on clamped-bit-line sense amplifiers realized through a hybrid $p-i(MQW)-n$/CMOS process.

keywords: (detectors-arrays, optical receiver, smart pixel, demultiplexing, optical communications, optical interconnects, integrated optoelectronics,)

The optoelectronic multiplexing and demultiplexing of data is a common operation on optical communication links, and one that is becoming more important as these links become increasingly prevalent. These operations permit multiple electronic data streams to be combined onto and removed from a single optical link, taking advantage of the high link-bandwidth available. Demultiplexing places particularly stringent demands on optoelectronic components. In this paper, we describe a method for demultiplexing optical data that utilizes clocked-optical receivers. This method permits the extraction of signals without the need for optoelectronic circuits operating at the full multiplexed-data rate, provided synchronization and timing information are available.

A conventional optoelectronic demultiplexer uses a high-speed-analog-optical receiver in combination with post-amplifier electronics used to convert the optical input data into an electrical signal at the same rate as the input data (*i.e.* the transport rate). These signals are then supplied to digital latches clocked at the slower rate of the constituent bit streams (*i.e.* the signal rate). By properly phase delaying the clock signals to the latches, the individual data streams are extracted. It is worth noting that once the data leaves the latches, the circuitry needed for further processing need only operate at the signal rate and *not* at the transport rate. However, transport-rate electronic signals are generated and amplified to logic level in the preceding stages. This poses a cost and performance challenge for optoelectronic systems. Either *all* the processing circuitry is made entirely in potentially high-cost transport-rate electronics, or the task is separated into transport-rate and signal-rate chips, thereby adding to packaging, board-design, and power dissipation problems.

This dilemma is unavoidable if synchronization and timing information are unavailable, for they must then be recovered from the transport signal. However, if such information is available, a different approach is possible, using the concept of a clocked optical receiver. Such synchronization information is available in *localized* digital systems such as switches, multi-processor networks, or supercomputers. In our approach to optoelectronic demultiplexing, multiple copies of the optical signal are generated, by use of a grating, a beamsplitter, or fiber couplers. These signals are imposed upon an array of clocked-optical receivers, as shown schematically in Fig.1.

These receivers are each clocked at the signal rate, and need not operate at the full transport rate. One requires a receiver that is only sensitive to input data that coincides with a clock transition. In other words, the receiver only 'sees' those bits that come at the time of the clock transition, and *ignores* the other bits. Since the receiver will hold its output state as long as the clock is held low, the output signals take on the periodicity of the clock signal, and not the shorter period

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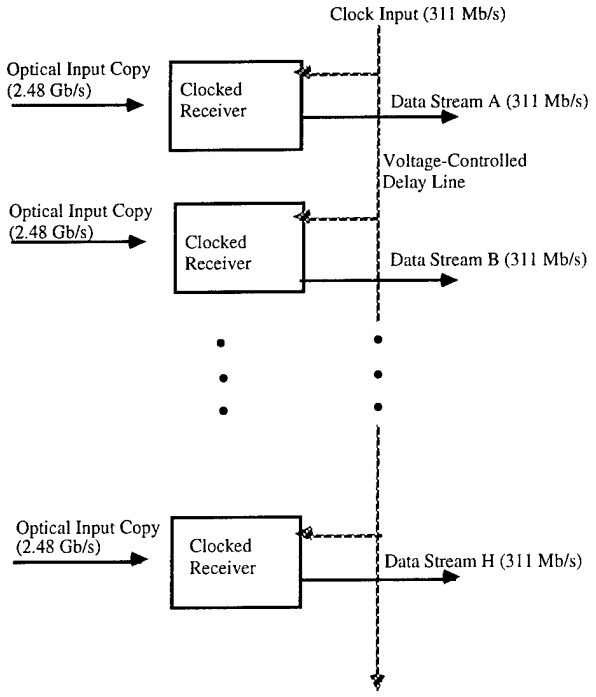

Figure 1: Schematic illustration of demultiplexing with clocked-optical receivers.

of the input data. Phase delay between the clock signals applied to the array elements permits extraction of all the constituent signals. The phase-delayed versions of the clock signal may be derived in a variety of ways. We have used a single input clock signal in combination with a voltage-controlled-delay-line (VCDL). At different points on the line, the signal is tapped and applied to a receiver, thereby providing a tunable phase delay between the clock signals for each array element.

We have previously introduced the concept of clocked-optical receivers based on clamped-bit-line sense amplifiers (CBLSA).[1, 2] There we described the advantages of optical receivers based on the CBLSA for compact, low-power dissipation amplification of optical signals to CMOS logic levels. A schematic of a CBLSA-based photoreceiver is shown in Fig.2. The receiver operates by unbalancing an unstable equilibrium established when the two sides of the sense amplifier are shorted together by Q7 and Q8. Photocurrent in one of the two detectors generates a current that biases one side of the receiver with respect to the other. When the clock signal drops to 0, positive feedback drives one side of the sense amplifier to V_{dd} while the other is forced to V_{clamp}, depending on the state of the input light.

We have designed and fabricated a 16-element lin-

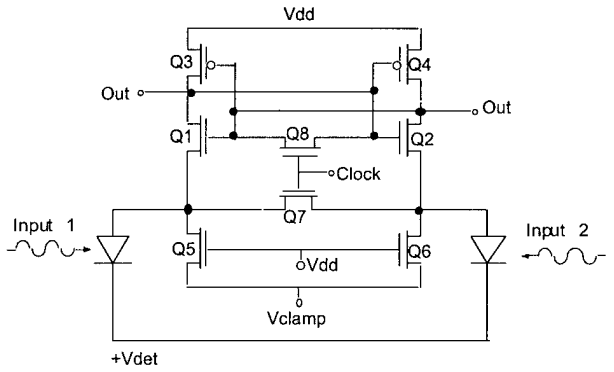

Figure 2: CBLSA-based optical receiver schematic.

ear array of CBLSA-based photoreceivers whose output was coupled to modulator driver circuits used to address normal-incidence MQW modulators that were attached to the circuit using a hybrid solder-bonding process previously described.[3] This permitted us to monitor the demultiplexed outputs optically. The optical detectors were provided in the same manner. The circuits were fabricated in Lucent Technologies' 0.35 μm linewidth CMOS process. For simplicity, a single set of optical test signals (input and output beams) was used, and these were translated from receiver to receiver to extract the individual data streams and demonstrate the demultiplexing function. One can also extract all eight streams from a single receiver by varying the phase delay of the clock signal electronically. All the receivers are switching on each clock cycle, regardless of whether an input is present, since all receivers are clocked, thereby providing a potential source of interference.

Experimental data from the operation of the demultiplexer array is shown in Fig.3, which depicts an optical input signal from the directly modulated semiconductor laser being used as the signal source in addition to eight plots depicting the eight separate output modulator signals being extracted from 8 independent receivers of the 16 present in the array. The input data is being supplied at 2.48 Gb/s, and the demultiplexed output is at 311 Mb/s in an RZ format. A 32 bit word is repetitively supplied to the circuit, and so a 4 bit 311 Mb/s word is repetitively output. The bias conditions were as follows: $V_{dd} = 3.3, V_{clamp} = 1, V_{det} = 5, V_{mod} = 9$ V, and the current from the V_{dd} supply was about 5 mA, for a total receiver array dissipation of just 11 mW. Demultiplexing was possible with single-ended inputs at a detected current of about 75 μA, corresponding to an input optical energy of about 120 fJ, or a power of -8.2 dBm assuming a responsivity of 0.5 A/W. Since

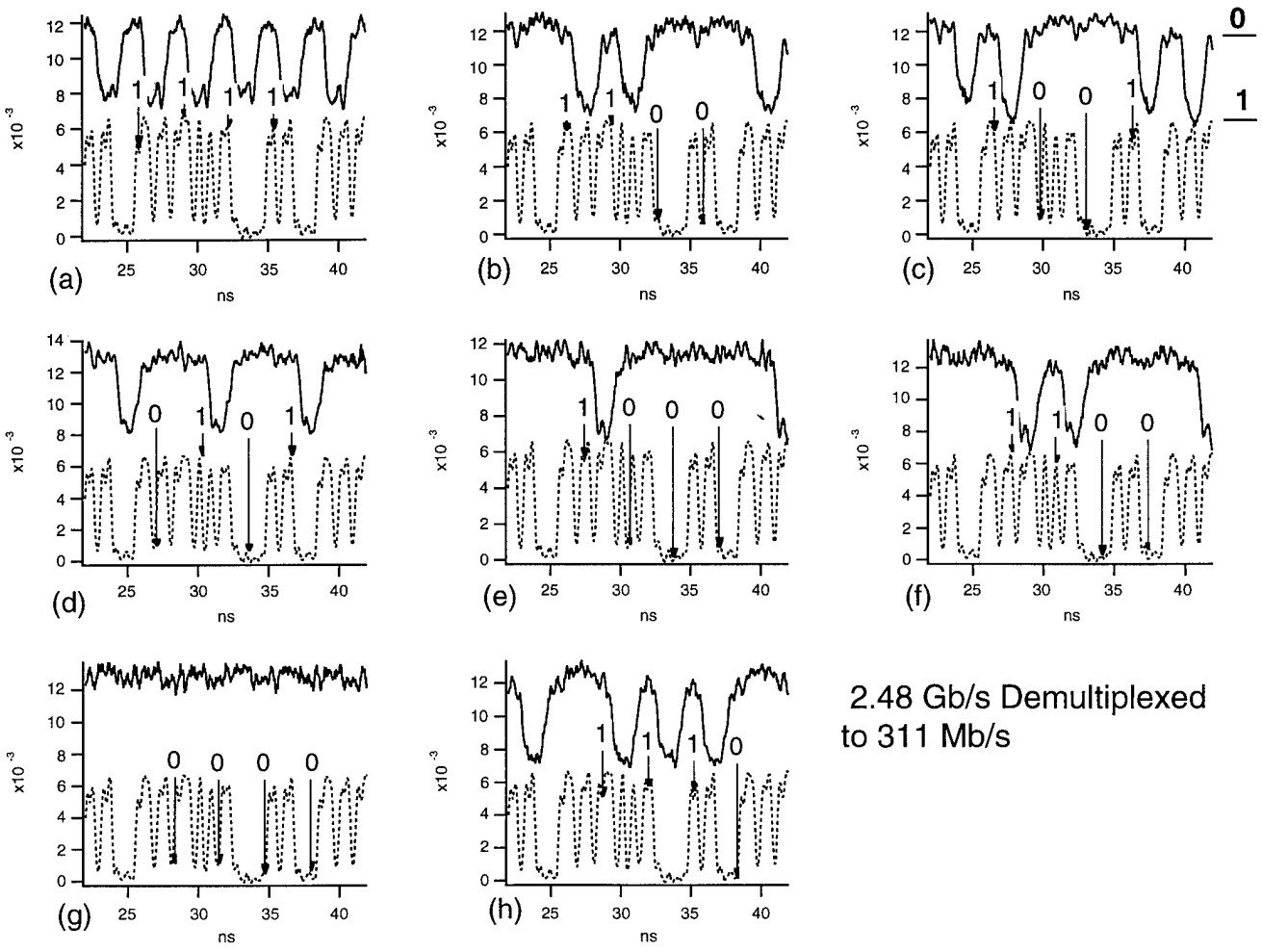

Figure 3: Demultiplexing of 2. 48 Gb/s optical input (bottom trace) into eight 311 Mb/s return-to-zero output signals. It is easiest to interpret the data if downward transitions of the output are taken as bit '1'. Since the receivers are clocked, outputs are phase delayed by at least one clock cycle with respect to the input.

this sensitivity did not improve much at lower bit rates, we believe that these receivers have an unintended imbalance that favors one state over another, resulting in both single-beam operation and unnecessary sensitivity degradation.[1]

Interestingly, when driven as repeaters (clock rate = transport rate), individual circuits could operate with RZ format output up to roughly 350 Mb/s, indicating a repeater bandwidth of roughly 350 MHz. Nevertheless, satisfactory demultiplexing of 2.48 Gb/s data is possible. This is because only certain parts of the circuit need to be able to follow the transport-rate signal. A simple-minded analysis of Fig.2 indicates that the relevant time constant is that associated with the input capacitance in the shorted state. Test data from the CMOS process indicates the on-resistance of Q5-Q7 is roughly 300 Ω. Assuming an input capacitance of 150 fF (input diodes and FETs) this yields an RC time constant of about 140 ps, more than sufficient to track the 403 ps bit period of the 2.48 Gb/s signals.

This work demonstrates one of the novel applications enabled by the use of clocked optical receivers. This opens the possibility to demultiplex fast optical signals with lower-speed electronics, broadening the potential of OE/VLSI to include high-data-rate telecommunications applications.

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Hybrid Electronic/Photonic 2D Neural Array Using InGaAs/AlGaAs Multiple Quantum Well Modulators Flip-Chip Bonded to a CMOS Si Analog Control Chip

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Abstract

A hybrid, flip-chip bonded, III-V/Si 2D *smart* spatial light modulator (SLM) has been designed and fabricated for use in photonic neural networks. The SLM consists of a 16 x 16 array of *neuron units* spaced with a 100 μm pitch. Each *neuron unit* contains Si CMOS control electronics, two Si photodiode detectors and two III-V multiple quantum well modulators, for dual input/dual output. The 2D arrays of InGaAs/AlGaAs multiple quantum well modulators operate at 980 ± 1 nm (with a 2D uniformity of ± 0.3 nm) and show an average contrast ratio of 13:1 at –9 V applied bias. The analog Si detection/modulator control chip provides a –2 to –9 V nonlinear sigmoidal response to the difference in light intensity at the two detectors. The III-V/Si hybrid device is flip-chip bonded using a nondeleterious *cold weld* indium bump process. The device is an important component for high performance photonic artificial neural networks.

Key Words

Spatial light modulators, Smart Pixels, Semiconductor MQW, Flip-chip bonding, Optical neural networks.

Introduction

Artificial neural networks (ANNs) have been used to solve problems not easily addressed via traditional algorithmic programming. Example problems include pattern recognition in noisy environments and system optimization under difficult-to-predict conditions. Artificial neural networks based on a hybrid electronic/photonic technology can potentially benefit from the weighted interconnection of large numbers of *neuron* units.

Photonic neural network architectures have been designed that incorporate vertical cavity surface emitting laser arrays for parallel input, hybrid electronic/photonic SLMs for implementation of neuron unit arrays with optical I/O, and photorefractive volume holographic optical elements for adaptive weighted interconnections [1]. Within such architectures, the hybrid SLM must be capable of the parallel detection of the weighted and summed input signals followed by a nonlinear *neural-like* transformation.

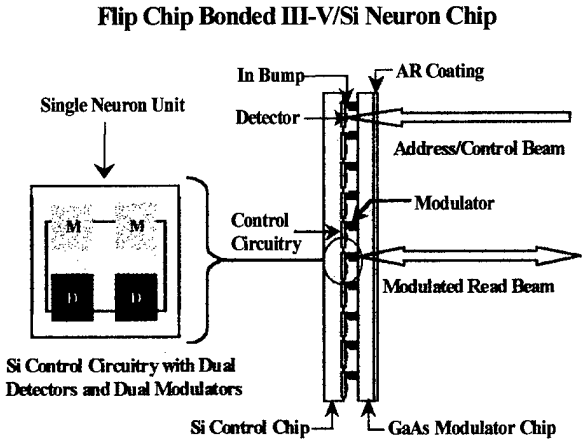

Figure 1. Hybrid InGaAs/AlGaAs MQW SLM with silicon drive electronic chip. A single dual input/dual output *neuron unit* pixel is also shown.

The hybrid neuron unit array described herein consists of a 16 x 16 array of *neuron-like* pixels. Each pixel has two III-V semiconductor multiple quantum well modulators, two Si photodiode detectors, and associated Si CMOS VLSI signal processing and modulator drive circuitry [1]. The modulators are fabricated via molecular beam epitaxy (MBE) on a GaAs substrate. The Si chip was fabricated through the MOSIS foundry service [2]

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using the 1.2 μm HP scalable CMOS *n*-well process. The GaAs modulator chip is flip-chip bonded to the Si detection/control chip using a *cold weld* indium bump process.

In the current front-side-illuminated implementation, the detectors are addressed and the modulators readout through the GaAs substrate of the hybridized structure (Fig. 1). The device is designed to operate at 980 nm to allow transparency of the GaAs substrate, sufficient detection by the Si photodiodes, and compatibility with available semiconductor laser sources. For the neuron unit array to function properly, the operating wavelength of 980 nm must be uniform over all of the individual modulators within the 2D array. The choice of 980 nm also allows for a back-side-illuminated implementation, with detector addressing through the Si substrate.

Modulator Design and Fabrication

The GaAs chip contains the 2D array of light modulators. The design of the modulators has been optimized for use in the flip-chip bonded hybrid Si/GaAs neuron unit array. However, the device is also potentially useful in other photonic systems employing SLMs such as joint transform correlators and optical crossbar switches.

Single Modulator Device Structure

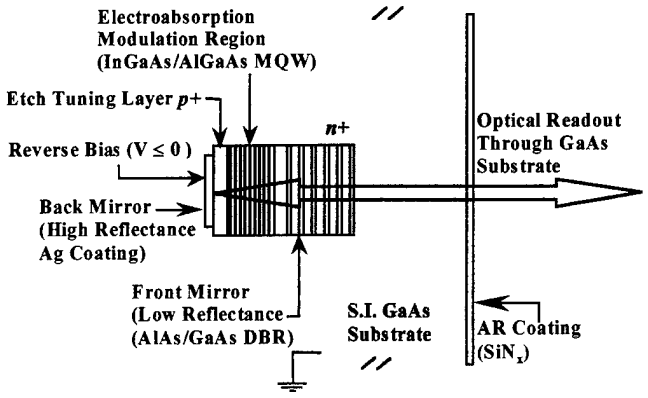

Figure. 2 The structure of a single electrically-driven InGaAs/AlGaAs MQW light modulator.

The light modulators employ III-V semiconductor materials grown using molecular beam epitaxy (MBE) on GaAs substrates. The structure includes an InGaAs/AlGaAs *p-i-n* multiple quantum well (MQW) region (980 nm operation) within an inverted asymmetric Fabry-Perot cavity (I-AFPC) (Fig. 2). The I-AFPC consists of an MBE-grown low-reflectance front mirror and a post-growth-fabricated high-reflectance back mirror. Such I-AFPC modulators are known to offer high contrast modulation, but fabrication of large 2D arrays has been a challenge [3]. Large 2D arrays of high contrast I-AFPC modulators have been demonstrated in the lattice-matched GaAs/AlGaAs system typically operating at 860 nm [4]. At this wavelength, the GaAs substrate is not transparent, and additional post growth processing steps such as substrate removal and/or device lift off are required. We have recently demonstrated high contrast uniform 2D arrays operating at 980 nm using strained InGaAs/AlGaAs MQWs [5].

The I-AFPC is designed to create incomplete destructive interference at the Fabry-Perot operating wavelength of 980 nm by means of unequal mirror reflectances. Voltage-controlled absorption modulation in the InGaAs/AlGaAs MQW region occurs at the operating wavelength via the well-understood quantum confined Stark effect [6]. By increasing the absorption in the cavity, the back mirror reflectance is effectively "matched" to the front mirror reflectance, switching the net device reflectance from a high to a low value.

To optimize the design of the modulator, isolated versions of the $In_xGa_{1-x}As/Al_yGa_{1-y}As$ *p-i*(MQW)-*n* region (typically 30 or 35 pairs) using 8.8 nm $In_{0.20}Ga_{0.80}As$ wells and 8.1 nm $Al_{0.26}Ga_{0.74}As$ barriers were grown. Absorption spectra of the *p-i*(MQW)-*n* structure under various reverse biases were studied. These layer thickness values and compositions were found to show high quality electro-absorption modulation behavior near 980 nm [7]. The isolated MQW shows optimal absorption modulation behavior at a wavelength 17.5 nm longer than the unbiased exciton wavelength. At this *operating* wavelength, the absorption strength per well (the product of the absorption coefficient and the well thickness) is observed to be 0.0045 at an applied bias of 0.26 V per well.

To keep the operating voltage below 10 V, 35 quantum wells are used. Keeping the number of wells to a minimum also reduces the total strain in the lattice-mismatched InGaAs/AlGaAs system. This results in a reduction in threading misfit dislocations that degrade device performance. The limited number of quantum wells, however, implies that the difference in reflectance values between the front and back mirrors in the I-AFPC cannot be made too large or the device will not completely turn off. For a back mirror reflectance of 97%, the front mirror reflectance must be at least 70% to achieve high contrast modulation. A 6.5 pair AlAs/GaAs distributed Bragg reflector (DBR) was selected for the front mirror that was theoretically and experimentally determined to give a reflectance of over 70% across a 70 nm wavelength range. A thin film silver layer is used for the back

mirror/electrical contact, giving a theoretical maximum reflectance of 97%. Metal coatings allow combining the function of mirror/electrical contact within a single structure. Combining these functions within a single structure eliminates processing steps, eases hybridization, and increases the device fill-factor compared to the alternative of a separate mirror and electrical contact.

Control of the operating wavelength associated with the Fabry-Perot cavity to within 1 nm cannot be reproducibly achieved using MBE growth without in-situ monitoring. To overcome this difficulty, we have developed methods of post-growth tuning of the Fabry-Perot cavity. One method uses a slow wet etch to *tune* the cavity to the desired operating wavelength. Etch tuning is done before deposition of the back mirror; thus, phase effects associated with the back mirror must be carefully considered during the tuning process [7]. An alternative method we have explored is unique to the use of dielectric DBRs as the back high-reflectance mirror. By adjusting the thickness of the DBR layers, the overall phase of the I-AFPC can be adjusted [8].

Modulator Array Results

Uniform 2D light modulator arrays have been fabricated showing 13:1 ± 4:1 contrast ratios, at –9.0 V applied bias (Fig. 3). The typical contrast ratio FWHM is about 3 nm and the FW at 90% of maximum is about 2 nm (Fig. 4).

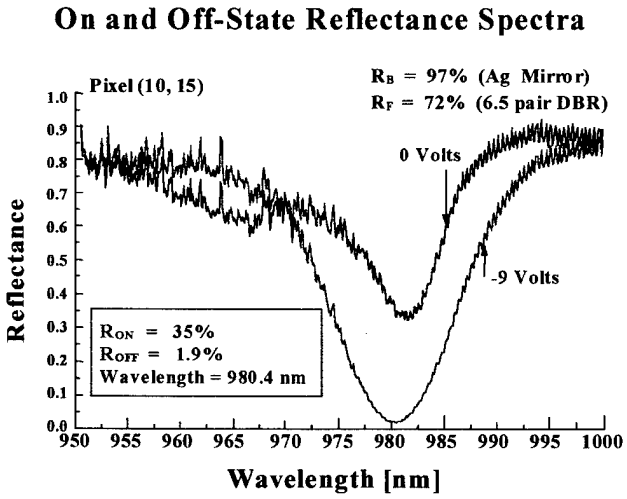

Figure 3. On-state and off-state spectra of a typical light modulating pixel.

The operating wavelength is 980.7 nm with an overall one-sigma uniformity of 0.3 nm over an area of 2.5 x 2.5 mm^2 (Fig. 4). Thus, all of the devices show high contrast modulation at a single common wavelength. Despite the strained MQW, no reliability problems such as a large number of shorted devices have been observed. We attribute this to using the fairly low number of 35 quantum wells.

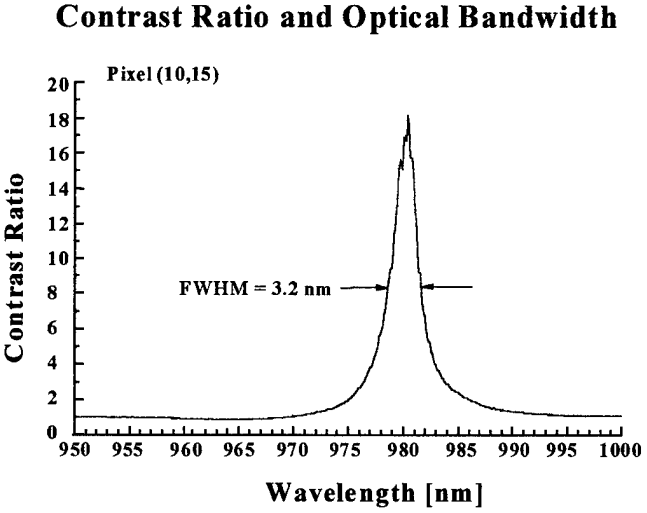

Figure 4. Typical contrast ratio and optical bandwidth of a pixel within the 2D array. Some devices show a CR over 30:1.

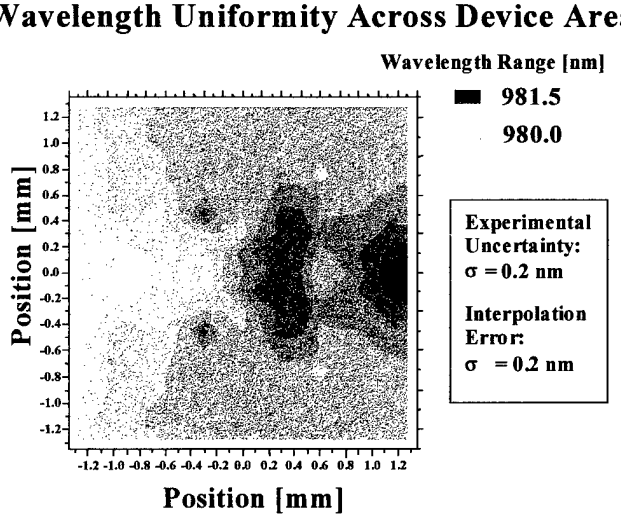

Figure 5. The wavelength at the minimum reflectance under a fixed –9 V applied bias is plotted across the 2D device area. An evenly distributed subset (about 25%) of the pixels were characterized.

The on-state reflectance is 35 ± 5% over the 2D array. Experimental and theoretical evidence indicates that the optical insertion loss within the device is due to three causes: absorption in the GaAs substrate, transmission through the GaAs/silver mirror interface, and residual

absorption within the MQW region. In this case, the separation between the zero-biased exciton wavelength and the 980 nm operating wavelength was smaller than the desired 17.5 nm. The slight fluctuation (± 3 nm) in the exciton wavelength is limited by our ability to control the InGaAs alloy composition (± 0.5%).

Theoretical and experimental investigations are underway to explore the tradeoffs associated with metal and dielectric DBR back mirrors to improve device performance. Metal mirrors offer the advantage of playing the dual role of mirror/electrical contact, thus simplifying device processing and maximizing the modulator fill factor. Dielectric mirrors offer the advantage of post-growth cavity tuning as mentioned above. Dielectric DBRs could also raise the back mirror reflectance to higher values, reducing the optical insertion loss. If the mirror reflectance is too high, however, it becomes difficult to turn the device off by biasing only 35 wells. Additional quantum wells and slightly higher drive voltages might be required.

Si Analog Control Chip

The analog Si IC performs a nonlinear sigmoidal input/output transformation similar to the transfer characteristics of biological neurons. Each pixel in the 16 x 16 array contains a pair of photodetectors to detect the dual-rail input signal. The control circuit produces a pair of sigmoidal modulator drive voltages in responses to the difference in intensity received by the two photodetectors. When the intensity at detector one is high compared to detector two (large intensity difference), modulator two receives a large drive voltage. The sigmoidal voltage response saturates at –9 V, turning off the normally-on modulator. Similarly, when the intensity at detector two is sufficiently high compared to detector one, modulator one is switched off. The dual-rail input intensity undergoes a sigmoidal transformation that is read out at the two modulators as a dual-rail output optical amplitude. The operational theory of the Si IC follows.

The Si control chip converts low-level optical signals incident on the two integrated photodiode detectors into large amplitude differential output voltages that drive the modulators [1]. The circuit performs the differencing as a current; cascoded current mirrors are used for high accuracy. The disadvantage of this design is that the power consumption can be large for high input signals, as multiple copies of the input current are created throughout the circuit. The advantage, however, is that the circuit has the potential for high-speed operation, because the voltage levels at most internal nodes do not vary significantly. The few nodes with wide voltage swings also have large currents to quickly charge/discharge the capacitance.

Silicon Circuit Operations Diagram

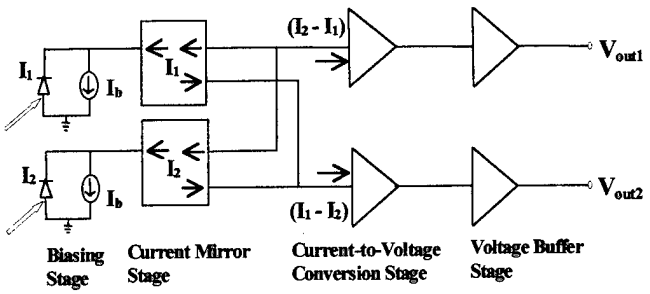

Figure 6. Schematic of the operational stages of a single processing element. Each element contains two cross-connected differential input/single-ended output comparator circuits.

The optoelectronic processing elements contain two cross-connected differential input/single-ended output comparator circuits. A schematic diagram of the operational stages of a single pixel is shown in Fig. 6. The circuit consists of five stages: a photodiode stage, a "keep-alive" current source, a current mirroring stage, a current-to-voltage conversion stage, and an output buffering stage.

The photodiode stage provides detection of the two optical input signals. The stage contains a pair of reverse-biased photodiodes consisting of an *n*-diffusion region in the *p*-substrate material. This photodiode design is different from the more commonly used *p*-diffused *n*-well design. The *n*-diffused *p*-well design allows for increased photocurrent collection efficiency within the *p*-type bulk substrate. Increased collection efficiency is necessary, as the responsivity of silicon is not optimally efficient at the 980 nm operating wavelength. Since the detectors are not electrically isolated from each other, the amount of crosstalk between adjacent detectors is a concern. A *p*+ guard ring surrounding the *n*-diffusion layer of each photodiode region is used to reduce the amount of crosstalk between detectors.

The "keep-alive" current source stage is used to keep the current mirror stage "alive" when no input signal is present on the photodiodes. This is achieved by keeping a small amount of current present in the current mirrors, thus preventing the current mirrors from shutting off. Shutting off the current mirrors would result in a significant speed penalty. The current mirror stage consists of groups of current mirrors that generate two opposite sign copies of the input current. One copy goes to the channel 1 input and the other to the channel 2 input of the summing node of the current-to-voltage stage.

At the current-to-voltage stage, copies of input currents generated from the photodetector stage are differenced and compared to a threshold value. The voltage at this node swings high or low, with a nearly ideal sigmoidal response characteristic, depending on whether the input difference is above or below threshold. The final stage is an output buffer stage. The wide voltage swing node of the previous stage has a high impedance and is unsuitable for driving a load. This stage buffers the output voltage to provide a low driving impedance.

The analog artificial neuron integrated circuit was fabricated through the MOSIS foundry service [2] using the 1.2 μm HP scalable CMOS *n*-well process. The chip has demonstrated a 2 to 9 V sigmoidal large-signal response at frequencies up to 100 kHz, and a small-signal response in excess of 1 MHz test equipment limited. Spice simulations indicate a small-signal response in excess of 4 MHz. The estimated chip power dissipation is 2 mW per pixel or about 0.5 W per chip.

Hybrid Device Integration

A cold weld indium bump flip-chip bonding process has been developed and used for the hybrid integration of the GaAs modulator and the Si control chip with indium bumps fabricated on both chips. First, the chips are coated with a thick (≥ 14 μm) photoresist. The thick photoresist is patterned using a contact mask aligner with standard photolithographic processing techniques. The die are placed in a vacuum chamber, where thermally evaporated indium is deposited on the surface. When the photoresist is lifted off, an array of indium bumps approximately 8 μm high is left on the surface of the silicon die. The indium bumps form the contacts between the Si die and the corresponding indium bumps on the GaAs modulator array. A visible flip-chip bonder-aligner (Research Devices, Model M8A, Piscataway, NJ) is employed to mate the indium-bumped silicon CMOS die and the GaAs modulators. Figure 7 shows the 16 x 16 neuron unit array analog Si IC with indium bumps.

The flip chip bonding is performed using a near-room-temperature *cold weld* bonding procedure that avoids heating the modulator and Si substrates. No deleterious effects associated with the flip-chip bonding procedure on the Si chip or modulator performance have been observed.

Conclusion

We have fabricated a hybrid III-V/Si flip-chip bonded 2D smart spatial light modulator array for use in photonic artificial neural networks. Each pixel in the 16 x 16 array contains two Si photodiode detectors and two InGaAs/AlGaAs MQW light modulators for dual input/output. In addition, each pixel contains two cross-connected differential input/single-ended output comparator circuits. The circuit provides a nonlinear sigmoidal response to the difference in intensity at the two detectors. The 2D array of InGaAs/AlGaAs multiple quantum well modulators operates at 980 ± 1 nm (with a 2D uniformity of ± 0.3 nm) and shows an average contrast ratio of 13:1 at –9 V applied bias. The III-V/Si hybridized device is flip-chip bonded using a cold weld indium bump process. Work is underway to assess the performance of the hybrid device.

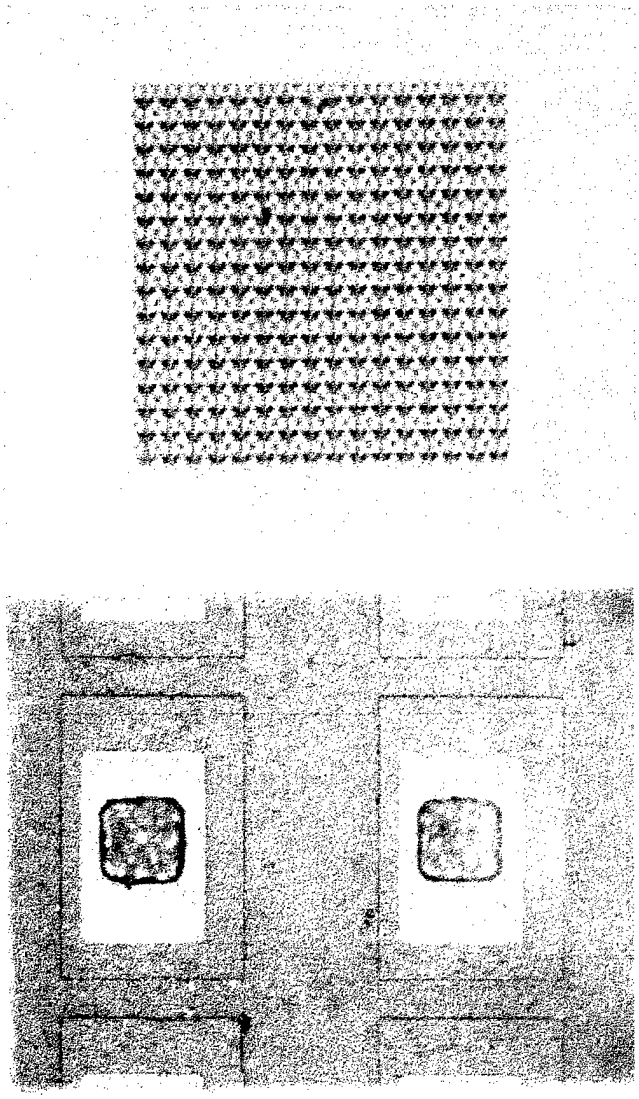

Figure 7. The 16 x 16 neuron array analog Si IC with indium bumps. The lower micrograph shows indium bumps on the light modulator array prior to flip chip bonding.

Acknowledgments

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Integration and Packaging Techniques

Wafer Bonding of InP to Si for Optoelectronic Integration

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Abstract

InGaAsP/InP optical devices have been successfully fabricated on Si wafers by using wafer bonding technology. Room temperature CW operation of edge-emitting lasers and photo-pumped operation of surface-emitting lasers have been achieved. A novel bonding process which allows integration of optical devices on structured wafers has also been proposed.

Key Words

Integrated optics- optoelectronics, Diode lasers, Optical interconnects, Integrated optical devices.

Introduction

Optical interconnections between Si LSI chips have been attracting increasing interest as a key technology to overcome communication bottlenecks in future LSI systems and/or to realize new functional LSI systems [1-3]. Figure 1 schematically illustrates the structure of the optically interconnected LSIs. InP lasers, preferably surface emitting lasers, are integrated on LSI chips and the optical signals are emitted through the transparent Si substrate to another LSI chip. InP lasers are suitable for this purpose because Si is transparent at the emission wavelength. Optionally, diffractive optical elements (DOEs) such as diffractive lens and beam diffractors can be integrated on backside of the Si wafer. In two-dimensional integration, the LSIs with lasers are mounted on a waveguide substrate such as glass or Si and are optically interconnected using DOEs fabricated on the Si back surface and the waveguide substrates.

In order to implement the interconnections, a technique has to be developed to integrate high-quality InP lasers on Si. Several approaches have been investigated for this purpose, including solder bonding [4], lattice-mismatched epitaxial growth [5-6], and wafer bonding[7-9]. Solder bonding with metals such as AuSn is the most straightforward method [4], but it is not suitable for vertical interconnections as shown in Fig. 1 (a) because the metals interrupt the surface-normal light propagation. Lattice-mismatched epitaxial growth has been widely investigated and room-temperature CW operation of the InP lasers has been successfully demonstrated [5-6]. However, there are some problems in this growth technique, such as high dislocation density (> $5x10^6$ cm^{-2}) and high growth temperature (typically > 900 °C for thermal pre-cleaning of Si and > 550 °C for epitaxial growth). The latter seems to be

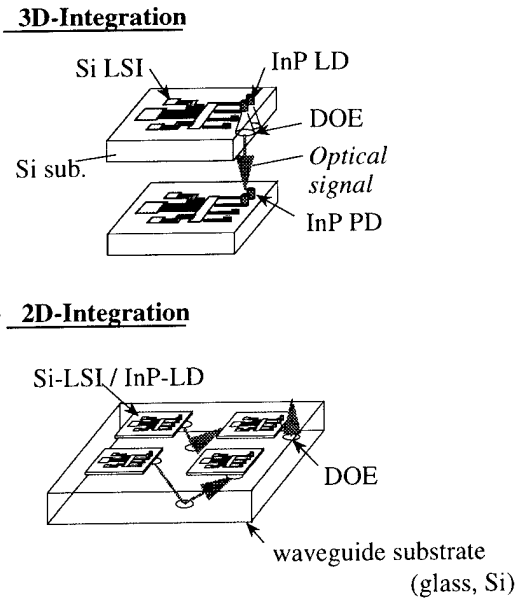

Fig. 1: Optically interconnected LSIs.

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more problematic for the device integration because the fully processed LSIs, especially aluminum interconnection metals, will be degraded when they are exposed to the temperature higher than 500 °C [10-11].

Wafer bonding is another promising candidate. It is a technique to bond different wafers by contacting the flat surfaces face-to-face after appropriate surface cleaning without using any adhesives. It is possible to bond wafers at low temperatures (even at room temperature) through Van der Waals force [7] and/or hydrogen bonding between surface OH-groups [12]. Therefore, we can integrate InGaAsP/InP materials on fully processed LSI wafers without degradation of the LSIs. Additionally, optical devices can be fabricated using photolithography after wafer bonding because the bonds can be strong enough to endure following device fabrication process. This will facilitate alignment of large number of small optical devices with Si circuits, resulting in a potentially inexpensive integrated system.

In this paper, we report on wafer bonding of InP to Si and fabrication of InGaAsP/InP lasers on Si substrates. Room temperature CW operation of edge-emitting lasers and photo-pumped operation of surface emitting lasers are discussed. In addition, a novel bonding process, which allows integration of optical devices on structured wafers, is also reported.

Wafer bonding process

Bonding process starts with chemical cleaning of wafer surfaces with H_2SO_4:H_2O_2:H_2O solution, followed by rinse in de-ionized (DI) water. After this cleaning, the surfaces show hydrophilic, which has been reported to be preferable for achieving strong bonds at relatively low temperatures [13-14]. The wafers are then spin dried and their surfaces are placed in contact at room temperature under some pressure applied on the wafers to ensure the surface contact. The wafers adhered to each other at this stage, though the adhesion is not very strong. Finally, the wafers are annealed at 400 °C for 30 min in an H_2 atmosphere to increase the bonding strength.

Bonding mechanism has been extensively discussed for Si-to-Si wafer bonding [12][15], and the similar mechanism is thought to be responsible also in the case of InP-to-Si. The proposed mechanism is schematically summarized in Fig. 2. First of all, OH-groups are absorbed on the wafer surface during the cleaning process with H_2SO_4:H_2O_2:H_2O (Fig. 2 (a)), which is thought to be an origin of the hydrophilicity. When the cleaned surfaces are brought into contact at room temperature, the wafers adhere by hydrogen bonding between the OH-groups (Fig. 2 (b)). In the following heat treatment at moderate temperatures (200 °C < T < 400 °C), water molecules start to escape from the interface and the hydrogen bonds are replaced by bonds like InP-O-Si (Fig. 2 (c)). This bond is usually stronger than hydrogen bond, which causes increased strength at higher temperatures. When the wafers are annealed at even higher temperatures (T > 500 °C), evaporation of phosphorus from InP and migration of indium atoms become pronounced and this can cause atomic rearrangement at the interface and result in stronger bonds (Fig. 2 (d)).

A unique feature in the case of InP-to-Si bonding is that thermal expansion coefficients are different between the materials and it causes thermal stress which may produce cracks or even separate the wafers during annealing under some conditions [9][16]. Therefore, the actual bonding mechanism should be more complicated than that described above. In addition, the bonding properties should also depend on other characteristics such as surface morphology, wafer size and thickness, which makes the full understanding of the mechanism more difficult. Further investigation is required to describe the mechanism more clearly.

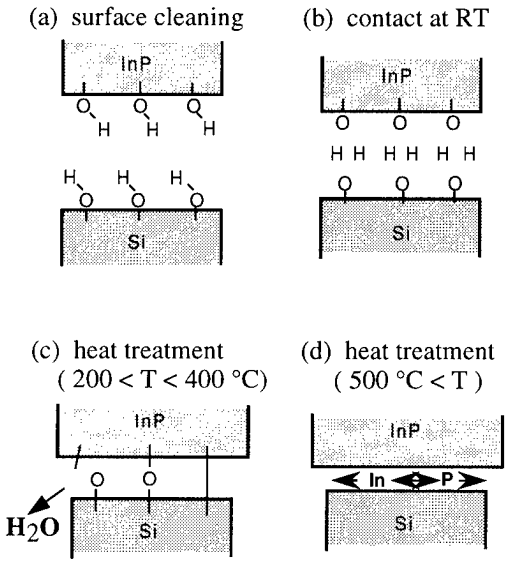

Fig. 2: Proposed bonding mechanism

As is suggested from the model described above, the bonding temperature strongly affects bonding properties, so is very important parameter. The temperature has been optimized in terms of (i) quality of the bonded InP crystals, (ii) bonding strength, and (iii) compatibility with device processes.

The higher temperature limit is imposed by the degradation of InP crystal quality and Si LSI circuits. The quality of the bonded materials has been evaluated by measuring photoluminescence (PL) intensity and found to

be degraded when the bonding temperature was higher than 600 °C [17], which can be attributed to the thermal stress induced by different thermal expansion between InP and Si. Therefore, the temperature has to be lower than 550 °C. Moreover, bonding below 500 °C is desirable to avoid the degradation of previously completed Si LSIs.

On the other hand, the lower temperature limit is imposed by laser fabrication process following the wafer bonding. The formation of ohmic contacts on InGaAs(P)/InP device requires to anneal the wafers at about 400 °C in the laser fabrication, as will be described in the next section. Additionally, higher bonding temperature is preferable in terms of bonding strength because bonds usually strengthen at higher temperatures [9] and the stronger bonds will facilitate the following device fabrication.

On consideration of these factors, the bonding temperature has been determined to be 400 °C in this work.

InP edge-emitting lasers on Si

In order to demonstrate the possibility of wafer bonding, we have first fabricated InGaAsP/InP edge-emitting lasers on Si. Figure 3 shows the laser fabrication process.

First of all, a double-heterostructure (DH) was grown by metalorganic vapor phase epitaxy (MOVPE) on a 350-μm-thick p-type (100) InP substrate. It was composed of a 0.2-μm InGaAs etch-stop layer, a 1.5-μm p-InP cladding layer, a 0.15-μm InGaAsP bulk active layer (λgap = 1.3 μm), a 1.5-μm n-InP cladding layer, and a 0.1-μm n-InGaAs cap layer. The epitaxial wafer, with a typical size of 10 x 10 mm^2, was then stuck on a glass plate with black wax for mechanical support (Fig. 3 (a)). Next, the p-InP substrate and InGaAs etch-stop layer were selectively etched to leave a thin DH film on a glass plate. The exposed surface of the p-InP cladding layer was then cleaned with H_2SO_4: H_2O_2: H_2O. The surface of a Si substrate was also cleaned with H_2SO_4: H_2O_2: H_2O. After a DI water rinse, the wafers were spin dried and their surfaces were placed in contact under a pressure of 4 kg/cm^2 at room temperature (Fig. 3 (b)). The wafers adhered to each other at this stage, though the bonding was not very strong.

Then, the bonded wafers were immersed in warm organic solvent to dissolve the wax completely and detach the glass plate from the wafers. The wafers remained still bonded after this wax dissolving. The sample was then annealed at 400 °C for 30 min in an H_2 atmosphere (Fig. 3 (c)) to increase the bonding strength. A weight of 30 g/cm^2 was applied on the wafers during the heat treatment. After this wafer bonding, 8-μm-wide mesa stripes were formed using standard photolithography and wet etching. The active layer was slightly undercut to reduce the active width to 6 μm. Finally, AuGeNi and AuZn were evaporated and alloyed at 400 °C to form n- and p-type ohmic contacts to complete the laser fabrication (Fig. 3 (d)).

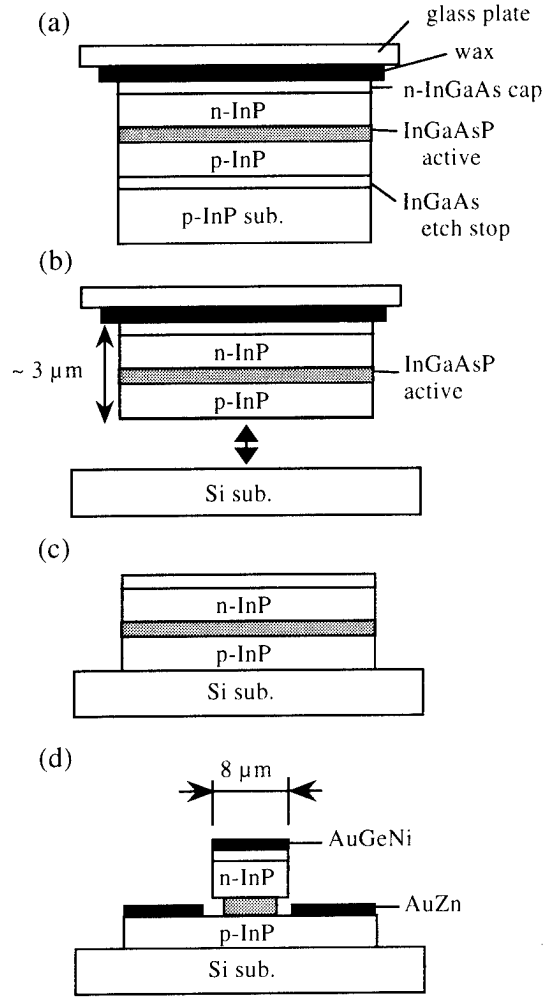

Fig. 3: Fabrication process of InGaAsP/InP edge-emitting lasers on Si using wafer bonding.

After thinning the Si substrate down to about 100 μm, the lasers were cleaved into 300-μm-long cavities and mounted on Si heat sinks with junction-up configuration. For comparison, the same laser structure was fabricated on a p-InP substrate. The light-current (L-I) characteristics of the devices were measured at room temperature (RT) without any facet coatings. A typical pulsed threshold current and corresponding current density were 36 mA and 2 kA/cm^2, which were identical to those of lasers on InP substrates. The slope efficiency was 0.25 W/A.

RT CW operation has been achieved with these devices as shown in Fig. 4. In this figure, the L-I curves of 3 lasers on Si are shown, together with those of conventional lasers on InP for comparison. The kinks in the L-I curves are due to multiple transverse-mode operation of the lasers with 6

μm-wide active regions. The threshold currents are about the same (I_{th} = 39 mA) for both structures, and higher output powers were obtained with lasers on Si. This can be attributed to lower thermal conductivity of Si substrates, which is one of the advantages of fabricating the lasers on Si. These results indicate that the wafer bonding is promising technique to integrate high-quality InP lasers on Si wafers.

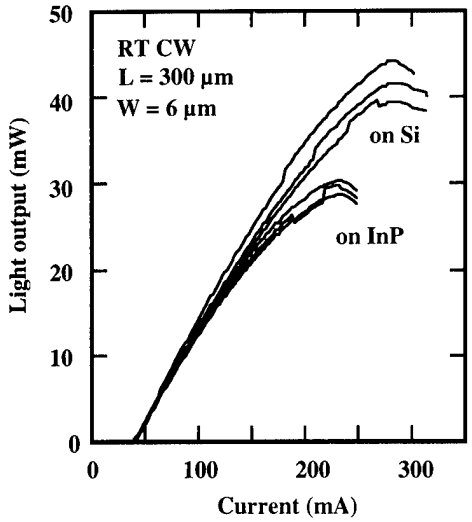

Fig. 4: L-I characteristics of the lasers fabricated on Si under room-temperature CW operation.

InP surface-emitting lasers on Si

In order to implement the optical interconnections between LSI chips illustrated in Fig. 1, InP surface-emitting lasers (SELs) are required to be integrated on Si wafers. We have tried to fabricate the InP SELs on Si by wafer bonding and achieved room temperature photo-pumped operation. In this section, the fabrication and characteristics of the InP SELs are discussed.

Figure 5 shows the structure of the SEL. The cavity was formed by wafer bonding of an InGaAs(P)/InP epitaxial wafer to 3.5-pair Al_2O_3/Si stacked mirror previously sputtered on a Si substrate. The InGaAs(P) / InP epitaxial wafer was grown by MOVPE on a p-type (100) InP substrate and was composed of a 0.1-μm p-InGaAsP (λg = 1.3 μm) etch stop layer, a 1.1-μm p-InP cladding layer, an undoped multiple quantum well (MQW) active layer, a 0.25-μm n-InP cladding layer, and a 40.5-pair n-InGaAsP (λg = 1.42 μm) / InP quarter-wavelength stacked mirror. The MQW active layer consisted of 12 unstrained InGaAs wells (7 nm-thick) and 11 InGaAsP barriers (6 nm-thick, λgap = 1.2 μm), embedded in 38 nm-thick InGaAsP (λgap = 1.2 μm) separate confinement layers on both sides.

The fabrication process is similar to that for the edge-emitting lasers and summarized as follows. The InGaAs(P)/ InP epitaxial wafer was first stuck on a glass plate with black wax and the InP substrate and InGaAsP etch stop layer were selectively etched. The surfaces of the exposed p-InP and Al_2O_3 top layer in the 3.5-pair Al_2O_3 / Si mirror were then cleaned with H_2SO_4: H_2O_2: H_2O. After rinse and spin-dry, the surfaces were placed in contact under a pressure of 4 kg/cm^2 at room temperature to result in adhesion of the wafers through hydrogen bonding between surface OH-groups. Finally, the bonded wafers were immersed in warm solvent to dissolve the wax completely and detach the glass plate from the wafers.

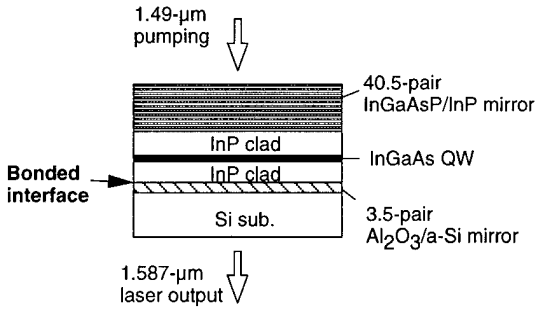

Fig. 5: Schematic structure of InP surface-emitting lasers fabricated on Si.

The fabricated structure was optically pumped by a 1.49-μm semiconductor laser through the 40.5-pair InGaAsP/InP mirror, as indicated in Fig. 5. The pumping laser was operated under a pulsed condition with 1-μs duration at 1-kHz repetition. The pumping light was focused on the sample surface using a hemispherical fiber with a measured spot size of 15 μm in diameter. Since 1.49-μm is out of the stop-band of the semiconductor mirror, the active layers can be optically pumped by the 1.49-μm laser diode. The reflectivities of both the InGaAsP / InP and Al_2O_3 / Si mirrors were measured to be higher than 99% at 1.55-μm wavelength. The resonant light of the cavity, whose wavelength was about 1.587 μm, was collected through the Si substrate and detected using a Ge photodetector with a lock-in amplifier.

Figure 6 shows light output versus input power characteristic at room temperature. A distinct lasing threshold (P_{th}) is clearly observed at the input power of 14.4 mW. Polarization-resolved characteristics are also shown in the figure. Above the lasing threshold, about 90% of the emitted light is confirmed to be linearly polarized along the (110) orientation. Full width at half maximum (FWHM) of the emission spectrum was confirmed to be reduced from

4.8 nm at the pumping level of 0.85 P_{th} to 1.6 nm above P_{th}. The relatively broad spectrum above the lasing threshold (1.6 nm) can be attributed mainly to thermally induced chirping caused by instantaneous temperature rise during the pulse excitation. The multi-transverse mode emission may be an additional reason for the broad spectrum.

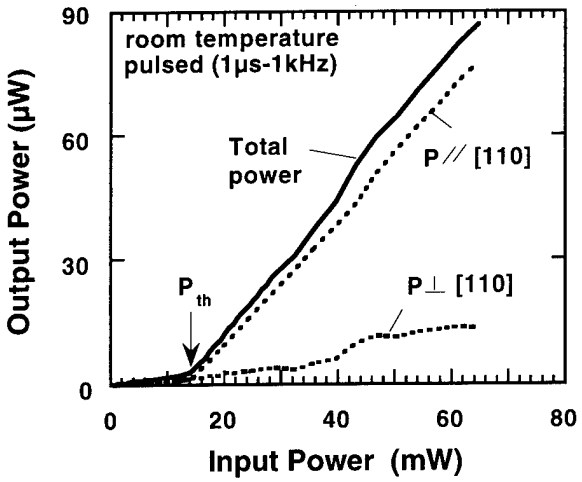

Fig. 6: Output power vs. input power characteristics of the SEL under room-temperature photo-pumped operation.

From this threshold pumping power, we can roughly estimate the corresponding threshold current density. Since 60% of the pumping light was measured to be reflected by the total cavity, 40% of the pumping light is thought to be absorbed in the laser structure. Half of that is estimated to be absorbed in the InGaAsP/InP mirror, and half in the active region. The pumping efficiency is, therefore, approximately 20%. Assuming this pumping efficiency and beam diameter of 15 μm, the threshold power density can be estimated to be 1.6 kW/cm^2. From this value, the corresponding current density can be calculated to be around 2 kA/cm^2. This result indicates that the cavity of high quality can be realized by the wafer bonding. Fabrication of electrically pumped SELs is now in progress.

Selective-area wafer bonding

In the previous sections, we have shown that high-quality InP lasers can be fabricated on Si substrates. However, Si LSI wafers, on which the lasers are required to be integrated, have many structures and steps on their surfaces. In this section, we propose a bonding process which allows the integration on such structured surfaces.

Figure 7 illustrates the proposed integration process. First, Si LSI wafers with some vacant spaces allocated for optical devices are designed and fabricated (Fig. 7 (a)). InP DH thin films are also prepared as described previously (Fig. 7 (b)), and the islands are formed in the thin films by photolithography and etching with the same pattern as the vacant spaces on the LSI wafers (Fig. 7 (c)). The surfaces of both wafers are then cleaned, and the islands are aligned to the vacant spaces and directly bonded at room temperature as described above (Fig. 7 (d)).

After removing the glass plate and annealing at 400 °C (Fig. 7 (e)), optical devices are fabricated on the DH islands by the lithography and the interconnection metals are deposited and patterned (Fig. 7 (f)). Since small optical devices can be fabricated at this step, the DH islands and the vacant spaces may be much bigger, which greatly facilitates the alignment at bonding in the step of Fig. 7 (d).

As a preliminary trial, we have fabricated InP LED arrays on bare Si substrates using this selective-area bonding. Figure 8 shows an example of the fabricated LEDs. InP DH islands, 200 μm x 3 mm, are bonded on Si and arrays of active regions 20 μm in diameter are fabricated in the islands. The ohmic contacts and interconnection metals are deposited and patterned after wafer bonding. As can be seen from this example, a large number of small devices can be fabricated after bonding of relatively large size of DH islands. The alignment tolerance at bonding are determined by the relative size of the DH islands and vacant spaces on LSI wafers as shown in Fig. 7 (d), and can be made large by appropriate design.

As illustrated in Fig. 7, we still can bond the DH islands even if there are Si LSI patterns on the wafers and make the optical devices aligned to the Si circuits by photolithography. In the example of Fig. 8, LEDs are located like electrical contact pads in LSIs, but, needless to say, optical devices can be fabricated anywhere in the LSI patterns by appropriate design.

A typical L-I characteristic of the fabricated LED is shown in Fig. 9, together with a schematic cross-section of the device. The emission wavelength was 1.3 μm and the light emitted through the Si substrates were detected. Output power more than 100 μW has been obtained. Higher output power will be obtained by using SELs in the future.

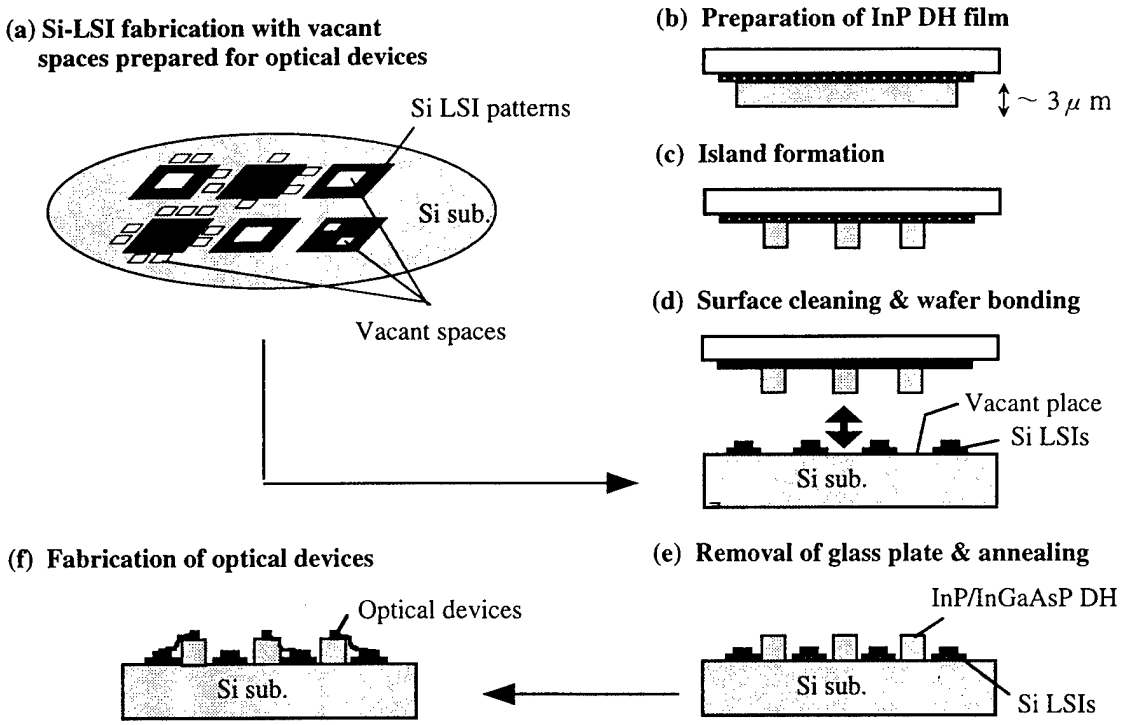

Fig. 7: Schematic illustration of the process which allows to integrate optical devices on Si LSI wafers.

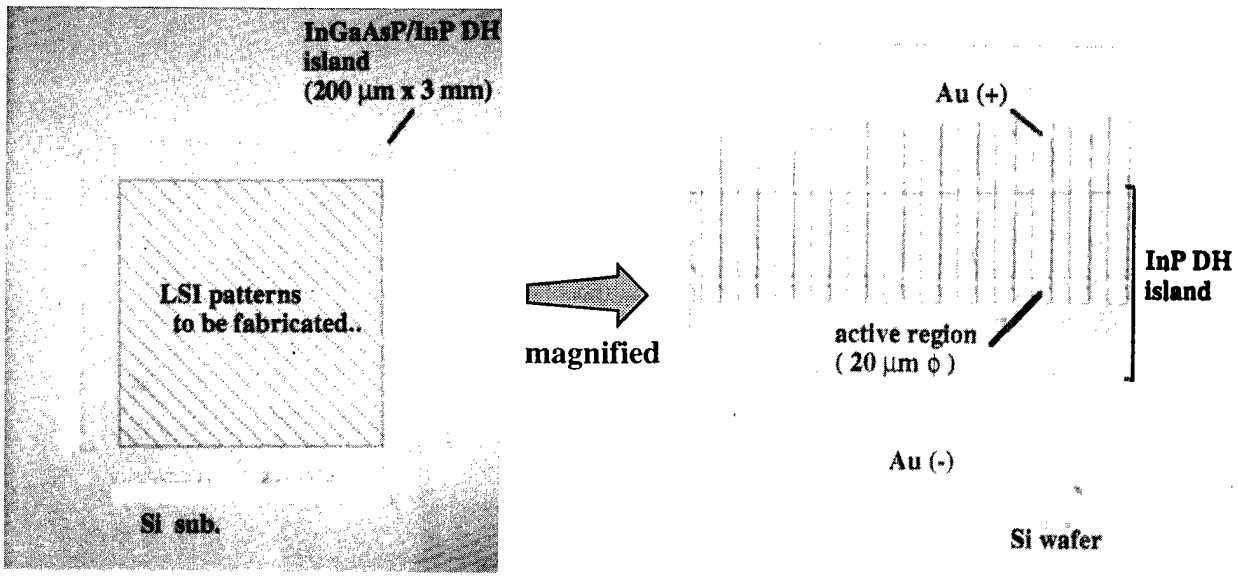

Fig. 8: An example of the fabricated LED arrays on Si wafer.

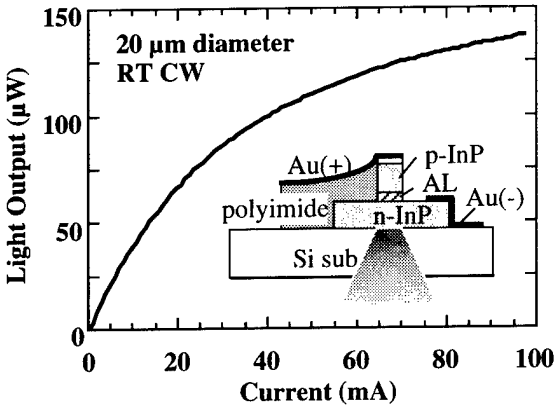

Fig. 9: A typical L-I characteristics of the LED fabricated on Si.

Conclusion

Wafer bonding of InP to Si has been investigated as an integration technique to implement optical interconnection between Si LSI chips and InGaAsP/InP optical devices have been successfully fabricated on Si wafers. Room temperature CW operation of edge-emitting lasers and photo-pumped operation of surface-emitting lasers have been achieved. A novel bonding process which allows integration of optical devices on structured wafers has also been proposed.

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DNA-Assisted Assembly of Photonic Devices and Crystals

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Abstract
DNA self-recognition properties are investigated for the heterogenous integration of optoelectronic devices. Prelimi-nary experimental results and their application to Smart Pixels and photonic crystals are reported

Key Words
DNA-assisted self-assembly, Integrated optical devices, Photonic crystals, Optoelectronics.

The progress made in III-V photonic devices and the practical necessity for their use with silicon chips make Heterogenous Integration (HI) techniques attractive for fast information handling hardware systems. This necessity has led to the adoption of the flip-chip bonding technique to build hybrid heterogenous chips such as CMOS-SEED Smart Pixels. However, in addition, to flip-chip bonding and various monolithic integration techniques based on heteroepitaxy, new hybrid integration methods that are potentially more cost effective, performant and flexible such as epitaxial lift-off, and wafer fusion bonding are emerging. These hybrid techniques are based on the transfer of thin film devices originally fabricated on mother substrates onto a silicon host substrate. With these hybrid techniques unless sophisticated pick and place systems capable of handling micron size devices can be developed e.g., by robotics precision assembly[1], the layout of the host substrate remains severely restricted by the layout and dimensions of the mother substrate. To remove this important limitation, self-assembly techniques such as the fluidic self-assembly [2] based on geometrical similarity or DNA based self-assembly techniques [3,4] based on the self-recognition properties of DNA, become attractive.

In this paper, we report a novel DNA assisted assembly process and discuss its application to the construction of Smart Pixels and photonic crystals. This technique promises to further enhance the capabilities of photonic devices, enlarging their application span and paving the way for a potential VLSI-Photonics revolution for information systems.

Synthetic DNA polymers show good promise for assisting the assembly of photonic devices onto an electronic mother board. This is due to the fact that the two strands of a DNA molecule have complementary base pairs providing an inherent self-organization mechanism. An (A)danine base on one strand will hybridize only with a (T)hymine base on the other, while a (G)uanine base has a (C)ytosine complement. For example, strands of DNA having the base sequence ATTTGC can be attached to a substrate in places where we want optical devices to be attached. We shall call this DNA the "capture" DNA. The complementary sequence of TAAACG can be attached to the optical devices. When brought together, the capture and complementary DNA strands will naturally tend to hybridize, resulting in the self-assembly of the optical devices on the substrate at the locations where the capture strands were placed. Using this technique, it is possible to position optical components at very precise locations on a substrate.

Experimentally, we have used artificially synthesized "capture" and "complementary" DNA strands with a desired sequence of bases. The sequence of bases was designed to minimize the possibility of intra-strand (self-) hybridization, while maximizing the strength of inter-strand hybridization. The DNA strands averaged 20 base-pairs (60 A) in length. Strands of this average length were long enough to be robust, while remaining short enough to be reproduced easily.

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To demonstrate the selective attachment of DNA to a substrate, the "capture" DNA strands were densely deposited on an SiO_2 coated silicon wafer that had been functionalized with amine groups. The wafer was then patterned with either UV light having a wavelength of 255 nm or an electron-beam. In either case, exposed capture DNA molecules lost the ability to hybridize with their complementary DNA strands. The complementary DNA strands were conjugated to fluorescent molecules in a sodium phosphate buffer and pipetted onto the substrate. Hybridization occurred between the fluorescently-tagged complementary DNA and the unexposed capture DNA on the substrate. Figure 1 shows the resulting patterned fluorescence. The minimum resolvable spot size in this picture is approximately 10 μm.

One of the practical considerations that must be addressed is the size of the object (or photonic device) that can be positioned using the DNA self-assembly processes. Preliminary experiments to determine size constraints were performed using polystyrene beads. First, the capture DNA strands were attached to amine-coated non-fluorescent polystyrene beads, having diameters of 0.871 μm and 3.1 μm. Both complementary and non-complementary DNA strands were conjugated to fluorofores in a sodium phosphate buffer. The fluorescently-labeled complementary DNA was mixed in one vial with the beads. The fluorescently-labeled *non*-complementary DNA was mixed with beads in a second vial, and served as a control. Both vials of bead-fluorofore solutions were centrifuged, and excess solution was pipetted off, leaving the beads in the vials. Fresh sodium phosphate buffer was added to the vials, and the beads were redistributed in the new solution. The centrifuging and diluting steps were repeated at least one more time. We then looked at the bead-fluorofore solutions under a UV (λ=350 nm) light. The bead solution that had been mixed with the complementary-DNA-conjugated fluorofores was brighter than the control solution (containing the non-complementary DNA) for both the 0.871 μm beads and the 3.1 μm beads. This indicates that capture DNA had successfully been conjugated to the beads, and was hybridizing with the fluorescently-tagged complementary DNA. The 0.871 μm beads exhibited a more pronounced difference between the control and complementary solutions than did the 3.1 μm beads. This suggests that the capture DNA conjugation was more effective with smaller beads--perhaps because the larger beads had a smaller number of surface amine groups.

To illustrate the movement of beads on a substrate, fluorescent polystyrene beads that had been coated with negatively-charged surface functional groups, and having diameters of up to 10.4 μm, were placed in an aqueous solution on a 5x5 array of contact pads. Using a probe-card, one contact pad was biased positively, while the

Fig. 1. DNA with conjugated fluorofores hybridized to a patterned Silicon substrate Minimum spot size is 10 μm

remaining 24 were given a negative bias. Under the influence of this potential difference, the charged beads selectively conglomerated around the positively-charged pad. When the positive bias was applied to a different pad, the beads migrated to this new position on the wafer. A similar experiment was conducted using fluorescent beads up to 10.4 μm in diameter and just two active pads–one biased positively, the other negatively. Again, we observed the beads moving under the influence of the electric field. These experiments demonstrate the possibility of moving relatively large optical devices in an aqueous solution under the influence of an applied electric field.

These results suggest that small devices (micron size) can be positioned onto desired areas on a host substrate by the utilization of the self recognition property of DNA polymers. When fully developed, this approach will provide the distribution of various thin film devices (electronic, optical, fluidic and possibly micromechanical) onto processed silicon chips in an arbitrary fashion in one single step without any geometrical or layout restrictions imposed by the mother nor the host substrates. Thus for example a dense array of photonic devices fabricated on a modest dimension mother substrate can be distributed sparsely on a large host substrate. In addition because individual devices can be controlled selectively, the technique allows for the utilization of only "known-good-devices" with a potential to significantly improving system yields. This assumes that the testing of photonic devices can be accomplished at low cost prior to the removal from host substrates and the DNA assembly process. Furthermore, this approach can have an important impact in the low cost manufacturing of wavelength encoded Smart Pixels in that VCSELs and/or detectors of different wavelengths fabricated on different substrates can be brought together on a single substrate thereby allowing accurate control of the spatial as well as spectral behavior

of the arrays. Other potential applications include various type of displays and heterogenous RF ICs.

In the remainder of this paper, we would like to illustrate the revolutionary capabilities of this approach by describing its potential impact on the synthesis of photonic crystals. Photonic crystals are artificial lattices comprised of various materials with different dielectric constants. When the dielectric variation is on the order of the optical wavelength, an optical wave entering the medium is diffracted either constructively or destructively depending the phase condition. The diffraction of the electromagnetic wave can lead to a decrease in the electromagnetic density of states and result in a photon-forbidden bandgap in the optical spectrum. Our first target in constructing the photonic crystal using the DNA self-assembly technique is to form a two-dimensional structure. A honeycomb configuration shown in Figure 2 is one of few two-dimensional structures known to exhibit a full photonic bandgap for both TE and TM polarized light [5].

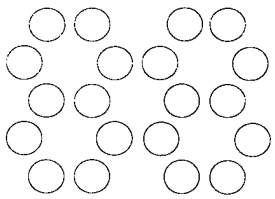

Fig.2: A cross-sectional view of a honeycomb structure with infinite rods

We have calculated the optical field dispersion in a honeycomb periodic structure consisting of infinitely long dielectric rods in air. The dispersion for TE and TM waves was calculated along the irreducible wedge defined by the K, Γ, and M symmetry points of the hexagonally shaped Brillouin zone of the honeycomb lattice. Maxwell's

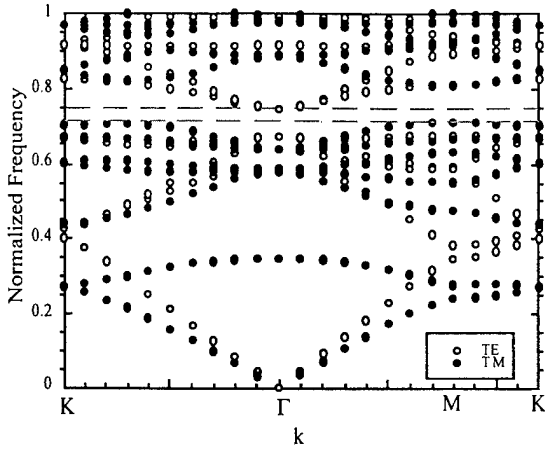

Fig.3: Dispersion relation of a two-dimensional honeycomb with a rod diameter to spacing ratio of 0.5

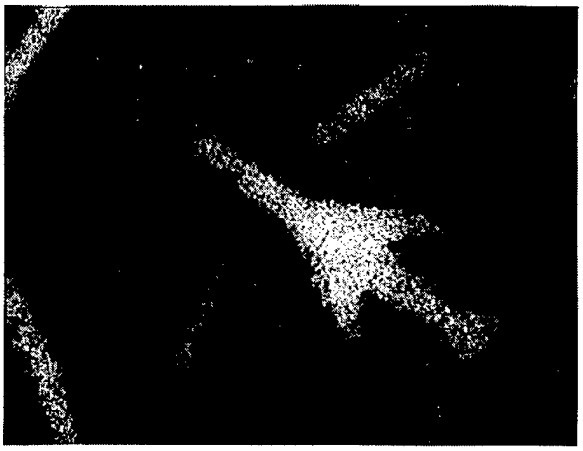

Fig.4: 160 nm fluorescent beads hybridized to patterned wafer

equation for the magnetic field was solved using plane wave expansion of the fields and the dielectric constant[6].

Figure 3 shows a bandgap for the two transverse electromagnetic fields centered at a frequency approximately equal to $0.6c/a$ where c is the speed of light in vacuum, and a is the spacing between rods. The hexagon structure has a lattice period larger than the rod spacing by a factor of $\sqrt{3}$. In the calculation, the ratio of the rod diameter to the structure spacing between neighboring rods is 0.5, which corresponds to approximately the optimum ratio for the largest photonic bandgap

We have conducted experiments that demonstrate the feasibility of constructing two dimensional photonic crystals using the DNA self-assembly technique. Capture DNA was conjugated to a SiO_2-covered silicon wafer that had been functionalized with amine groups. The wafer was then patterned using UV light. The complementary DNA strands were conjugated to amine-functionalized fluorescent beads of up to 1 μm in diameter. The beads were released in an aqueous solution on the substrate, and hybridized to the unexposed capture DNA. Figure 4 shows fluorescent beads 160 nm in diameter hybridized to the patterned substrate. A two dimensional photonic crystal might be realized in a similar fashion, by placing beads, on a honeycomb-patterned substrate.

In summary, DNA assisted assembly relies on the self recognition property of artificial DNA polymers as a "highly selective glue" to bring together devices with incompatible layout and structures. In this paper, we have presented results on attachment of DNA onto metallic and semiconducting materials. In addition, deposited DNA strands have been lithographycally patterned using UV exposure. DNA strands being charged negatively have been used to control the movements of devices from 10nm to 10μm in size under the influence of an electric field. Finally, patterned DNA strands deposited to a host substrate hybridize with complementary DNA strands

attached to individual devices, bonding them in a self aligned fashion to the desired location on the host substrate. We have argued that this technology can impact more than one area in photonics, including the synthesis of photonic crystals. Yet much research remains to be performed before this technique can be used in an industrial environment. To name a few areas that we are presently investigating we should cite further characterization of bonding strengths, and process yields, demonstration of selective bonding of multiple set of photonic devices (e.g., LED's with different wavelengths), and formation of ohmic contacts to the grafted devices.

Acknowledgments

The authors would like to thank Susan Wey for helpful discussions about photonic crystals.

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Self Aligned Epitaxial Liftoff for Smart Pixels

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Introduction

The need for increased processing speed in advanced computing systems is straining the limits of purely electronic systems. Opto-electronic systems may represent the future form of implementation of high throughput data processing systems. The components that are selected for Opto-Electronic data processing systems have to meet the requirements of both high speed and low power dissipation. GaAs/AlGaAs Multiple Quantum Well (MQW) Spatial Light Modulators (SLM) exhibit low switching power and very high speed. Moreover, they operate at voltages which are compatible with Si VLSI technology[1]. These make them attractive in high density optical information processing systems such as optical correlators. Thin film integration between Si integrated circuits and MQW modulators can be done by Epitaxial Lift-Off (ELO) technique. A major advantage of ELO is that Si circuitry and GaAs MQW modulators can be optimized individually and then integrated together resulting in improved yield and performance.

In this paper we report a novel self-aligned ELO integration scheme for a 16x16 reflective GaAs/AlGaAs MQW array on Si VLSI technology. The self-alignment of the MQW array on the Si driver circuitry was accomplished by controlling the respective aqueous surface tensions on lifted-off GaAs thin films and on the underlying bonding substrate surface.

Experiments

Reflective (normally-off) GaAs MQW modulators which contain 60 periods of (90Å)GaAs/(40Å)$Al_{0.15}$GaAs MQW's were fabricated. The drive voltage and operating wavelength were at 10Volts and 840nm, respectively. Foundry fabricated Si circuits, (MOSIS), designed with 2μm CMOS design rules served as drivers to the MQW array. The active area of the array had an effective fill factor of 97.3% and was composed of a 16x16 array containing 188μm×188μm pixels spaced on a 193μm pitch.

Most of the ELO processing procedures have been described in detail in other references[2]. The form of integration in this experiment consists of the detachment of a fabricated array of GaAs MQW modulators from their substrate by under-cutting a thin sacrificial AlAs layer from between substrate and modulators. This thin film is then transferred onto the Si driver chip. The typical surface roughness on CMOS chips (MOSIS-2μm-technology) is about 1.8μm. It is essential to planarize this circuit topography before marrying the MQW modulators to the CMOS substrate. A variety of planarization schemes have been discussed elsewhere[3]. In this research work, a polymeric planarization coating which can reflow at 200°C and smooth out the surface was spun onto the Si chip prior to thin film bonding. The degree of surface roughness was reduced by a factor of 10 after this coating. A 1500Å Au film reflector was then patterned onto the driver circuit array.

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By controlling the respective aqueous surface tensions, of the planarization coating (hydrophobic, with wetting angle > 90°) and the Au mirror (hydrophilic, with wetting angle < 10°), the lifted-off film can be locked[4] onto the surface pattern formed by the Au mirror. The modulators array is then "Self-aligned" onto the Si driver circuit when its surface pattern is exactly matched to the Au reflector. The processing sequence is shown in Figure 1. The major advantage of this self-aligned ELO is that Si circuits and GaAs MQW modulators can be fabricated and tested separately before being brought together. The alignment of all the modulator array to the underlying driver circuitry can be done at the full array scale, or even at the wafer scale within photolithographic accuracy, as shown in Figure 2.. After bonding the aligned lifted-off film onto the Au mirror, anti-reflection coatings and interconnection metallization were deposited.

The availability of a self-aligned epitaxial lift-off and bonding process, for modulator arrays, on planarized Si driver circuitry, may be extremely valuable in future dense, high speed, opto-electronic data processing systems. A manufacturable ELO technique has recently been developed. Black wax is absent from the process which makes the bonding alignment procedure much easier. Epoxy is used as the bonding medium, which can not only self-planarize the surface during thin film bonding, but achieve accurate alignment. These advances will also be reported in the conference.

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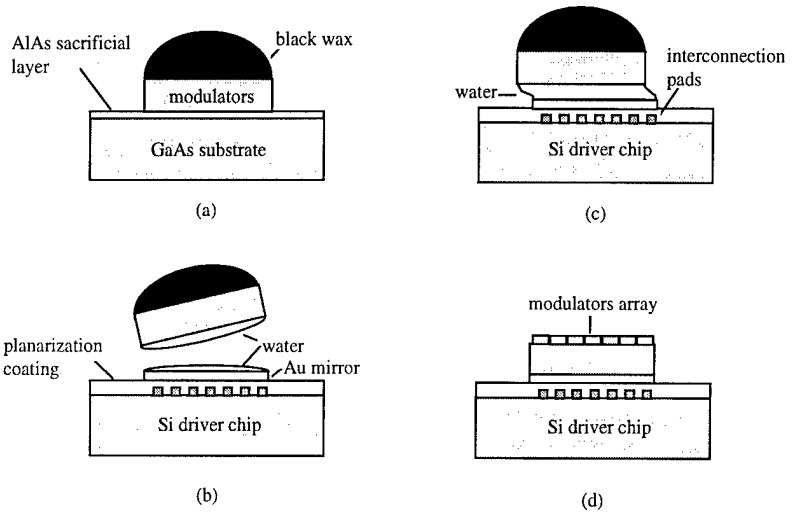

Figure 1: Self-aligned epitaxial lift-off thin-film integration. (a) Defining modulator array by mesa etching to AlAs sacrificial layer and selectively wax covering; (b) Lifted-off modulator array is brought together with the Si driver chip. Notice that water only adheres to hydrophilic surfaces. (c) Surface tension of water locks the thin film with respect to the underlying Au reflector. (d) The modulator array is self-aligned and bonded on to the Si chip.

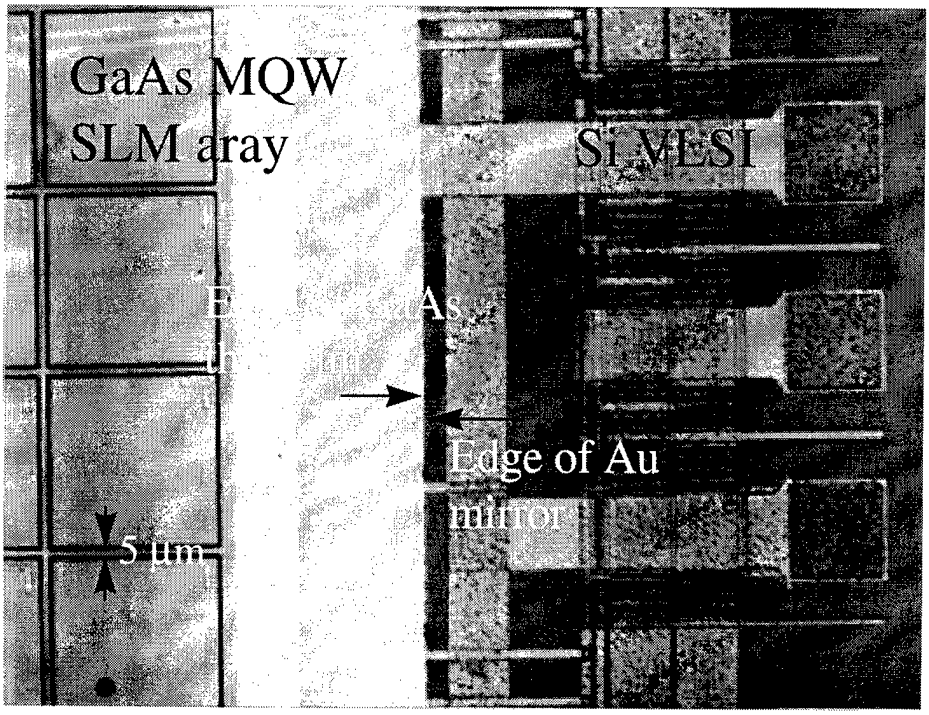

Figure 2: A photograph shows the bonding accuracy of thin film GaAs MQW array on Si circuitry through ELO self-aligned bonding process.

Packaging Optics for Smart Pixels

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Introduction

As optoelectronic devices move from the research laboratory towards the factory, optical packaging issues become increasingly important in developing a viable technology. Practical optoelectronic systems will have to be simple, inexpensive and reliable.

Holographic optical elements (HOE), and especially computer generated HOE (CGH), offer unprecedented control over the phase profile of an incident beam, allowing the creation arbitrary aspheres and multiple beamsplitting. CGH have proven their use in optoelectronic systems for spot array generation and interconnection. But this technology has already made it out of the lab: hybrid refractive and diffractive optics are starting to be manufactured for products such as lightweight binoculars, laser collimators, and others. Here we will discuss the next generation of holographic optics, which add selectivity in polarization or wavelength and allows great flexibility in optical system design.

CGH Design and Fabrication

A conventional kinoform CGH is a 2-D phase profile which transforms the input light (e.g., a plane wave) into the desired output (e.g. an array of points). The desired continuous phase profile is first computed, then reduced to a minimum of data by pixellation, truncation to modulo 2π, and quantization into discrete values. This data array is then used to fabricate the hologram.

A polarization- or color-selective CGH is similar in function to a conventional phase-only kinoform CGH, except that the element must create a different phase profile for each of the two orthogonal linear polarizations or colors that illuminate the hologram. This is made possible by use of material birefringence, for polarization selective CGH, or chromatic dispersion, for color-selective CGH.

Polarization-selective CGH were first fabricated in birefringent lithium niobate using a two-substrate design. described in reference 1. Both substrates are patterned and etched, then joined face-to-face, aligned, and joined with UV-curing epoxy to yield an element like that shown in Figure 1. The independent etch profile of the two substrates allows control of the relative phase between orthogonal polarizations transmitted through each pixel, and the absolute phase of the pixel with respect to its neighbors.

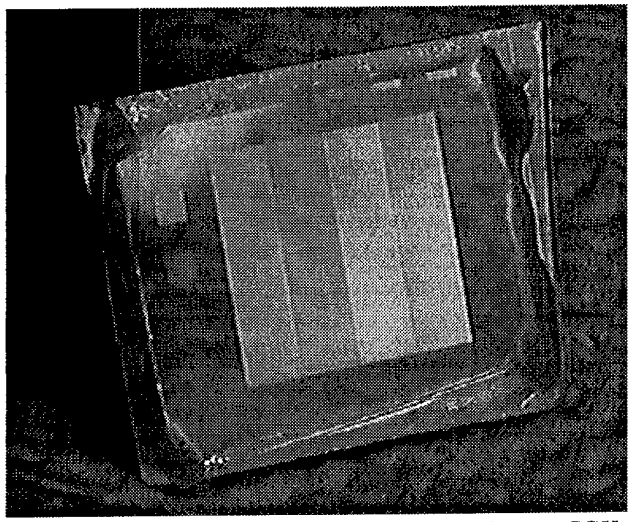

Fig. 1: Assembled 2-substrate polarization selective CGH

Binary holograms fabricated with this technique yielded a diffraction efficiency of 25% and polarization contrast ratio of 10:1. A four-level phase holograms produced a diffraction efficiency of 45% and contrast ratio of 120:1. The theoretical diffraction efficiencies of, for example, 80% for a four-level phase hologram have not been demonstrated due to fabrication errors, especially in the alignment between the two substrates.

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An alternative fabrication technique uses a single birefringent substrate with a multiple order delay (MOD) kinoform CGH. The concept is simple. Suppose a phase delay of π is required for horizontal (H) polarization, and 0 for the vertical (V) polarization. In a birefringent substrate, an etch depth sufficient to achieve a delay of exactly π for H polarization would produce a delay of $\pi-\delta$ for V polarization. Tripling the etch depth yields 3π for H and $3(\pi-\delta)$ for V, but the modulus of this delay is π for H and $\pi-3\delta$ for V. If the material is such that $(m+1)\delta$ is approximately π, where m is an even integer, then a binary phase hologram visible only for H-polarized light can be fabricated. Such a hologram, fabricated in YVO_4, produced a close-to-theoretically-limited diffraction efficiency of 39% and a polarization contrast ratio of 33:1 [2].

An entirely different approach to a single-substrate polarization-selective CGH is to use artificial form birefringence, where a surface relief profile with features much smaller than the optical wavelength creates a polarization-dependent index. [3]

The concepts of polarization-selective CGH can all be directly translated to obtain color-selective CGH by substituting material dispersion for birefringence. For example, a MOD binary-phase CGH designed to separate 1.3 and 1.55 μm light was fabricated with a 8 μm deep binary grating etched into BK7 glass [4]. The grating diffracted 1.55 μm light with 39% in the +1 and -1 orders and transmitted less than 1% in the zeroth order. The same element, illuminated at 1.3 μm, transmitted 83% in the zeroth order and diffracted less than 1.2% in any one of the diffraction orders.

Optoelectronic Packaging

To illustrate the potential application of polarization- and color-selective CGH in optoelectronic systems, we will describe three specific examples.

OE-VLSI Modulator Optics

To see how such elements can dramatically reduce the size, complexity and cost of packaged optoelectronic systems, consider a modulator-based OE-VLSI device [5] with quantum well modulators integrated onto silicon electronics.

Typical optics for efficient operation of such devices is shown in Figure 2. A CGH spot array generator is illuminated by a collimated, linearly polarized power beam. The diffracted beams are focused by a lens onto modulators on the chip surface through a polarizing beam splitter and a quarter wave plate. Light reflecting from the modulators is deflected on the second pass through the beam splitter and sent to the output.

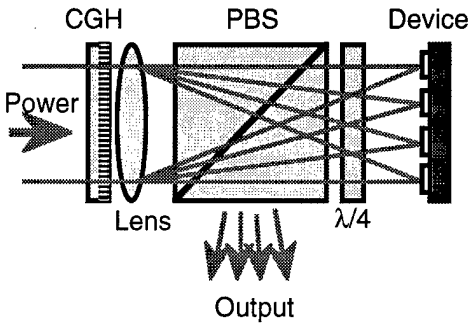

Fig. 2: Smart pixel with CGH spot array generator

Figure 3 shows how the same functionality is obtained with a polarization-selective CGH which acts as an off-axis lenslet array for one polarization yet is transparent to the orthogonal polarization. On the forward pass, the CGH creates an array of spots focused straight into each modulator. The reflected output, however, with polarization rotated by two passes through a quarter wave plate, is unperturbed by the CGH and heads straight out from the device. This package can be integrated directly onto the OE-VLSI chip to produce a robust and convenient component.

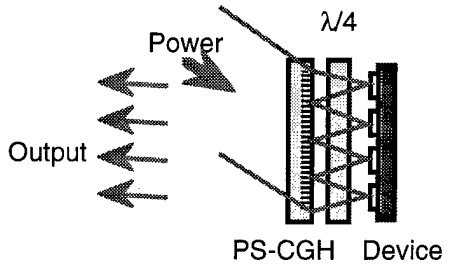

Fig. 3: Smart pixel with pol-selective CGH lenslets

Multistage Interconnection Network

In a passive optical network, data is carried from end to end without conversion to electronics by setting up an optical circuit-switched path. The data rate is not limited by the network switch response time, since it flows through the open path. Figure 4 shows the topology of an optical multistage interconnection network (MIN) which uses layers of binary switching elements interconnected by a predetermined network architecture.

The potential of role for polarization selective CGH in building optoelectronic MINs is discussed in detail in reference 6. The basic concept is that each layer of the network is implemented with a smart pixel array, where each pixel includes a modulator which can rotate the polarization of an incident data beam. Such modulators have been fabricated using liquid crystals as well as ferroelectric PLZT as the electro-optic medium.

Figure 5 shows how polarization selective CGH are used to make a self-routing 2x2 MIN switch. A transmissive modulator array has CGH on each side. Two optical inputs enter with orthogonal polarizations. The first CGH combines the inputs and focuses them into the modulator. The modulator either exchanges polarizations, or not, depending on the switch setting. The output is then routed to the appropriate destination in the next stage by a second CGH.

A small-scale system demonstration of a 4x4 switch using three cascaded stages of arrayed polarization-selective CGH is described in reference 6.

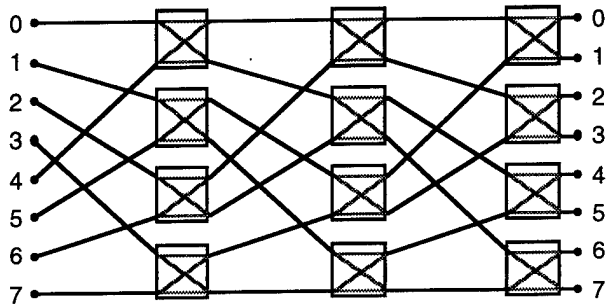

Fig. 4: Multistage interconnection network topology

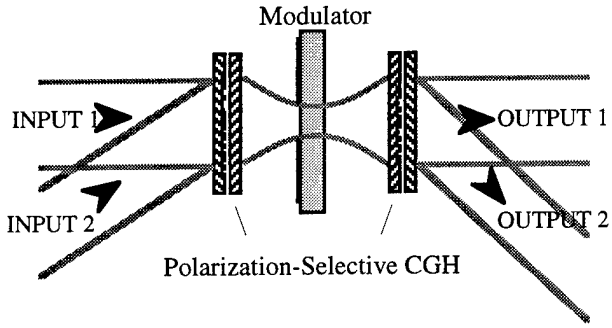

Fig. 5: Polarization-based 2x2 switch

Coarse Wavelength Division Multiplexing

Coarse demultiplexing of data transmitted at both the telecommunications wavelengths 1.3 and 1.55 μm is often accomplished using a dielectric notch filter placed between collimating and focus lenses. The resulting package, however, directs the demultiplexed output into two separate locations. For some applications, the demultiplexed beams can be routed into a single optoelectronic chip.

Figure 6 shows an experimental result from [4] which demonstrates how a simple optical system with a color-selective CGH can direct the demultiplexed output onto the same output plane. With micro-optics, such a system can be made extremely compact, simple and inexpensive, because only a single chip alignment is necessary

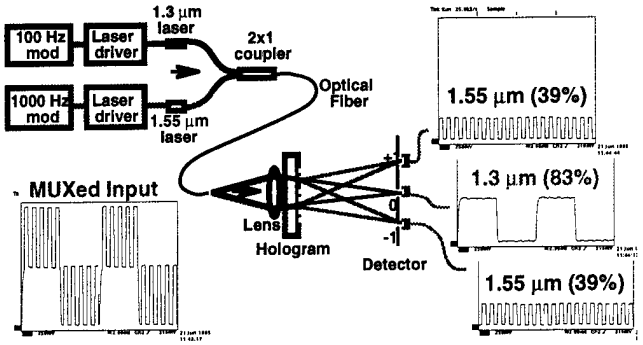

Fig. 6: Coarse λ-demultiplexing with color-selective CGH

Conclusions

We described the basic concepts of polarization- and color-selective CGH components, and described examples to illustrate their potential role in optoelectronic smart pixel' packaging. Such components represent a valuable new tool for developing compact and reliable optoelectronic systems.

Acknowlegdments

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SLM Materials and Structures

Ferroelectric liquid crystal over silicon spatial light modulators - principles, practice and prospects

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Abstract

The hybrid technology which combines a thin layer of ferroelectric liquid crystal directly on top of a CMOS backplane has provided a hybrid technology for spatial light modulators which has already reached a mature stage of development. Devices of around 10^6 pixels are under construction. The use of devices in a number of systems has already been demonstrated.

Key words

spatial light modulators head-up displays
optical data processing liquid crystal devices

1 Introduction

A spatial light modulator (SLM) is a device capable of impressing information onto an optical wavefront. SLMs exist in many forms [**1**]. Light modulation may be carried out by electro-optic, acousto-optic and mechanical effects, among others. A SLM may be addressed optically, acoustically, electrically, electronically or by electron beam. The applications of such devices are manifold and include information display, coherent optical data processing, data routing and holography. The overall field of SLMs has been reviewed in the past [**1**]. In this article, the discussion is restricted to a primarily descriptive treatment of SLMs in which the optical characteristics of a thin overlying layer of ferroelectric liquid crystal (FLC) are controlled in a binary fashion on a pixel by pixel basis by means of an underlying CMOS silicon backplane [**2,3**]. Here, we shall refer to the hybrid technology as FLC/CMOS. FLC/CMOS devices typically exhibit the following characteristics

- reflective mode operation
- binary modulation of light
- amplitude or phase modulation possible
- ease of electronic addressing (CMOS/TTL compatible)
- high line count (64 to 1280 lines)
- small pixel pitch (5 to 40 micron)
- fast frame rate (1 to 20 kHz)
- high optical quality
- acceptable light throughput

2 Principle of Construction and Operation

The principle of construction and operation of a pixel of a FLC/CMOS SLM is illustrated in Figure 1.

Principle of Construction

The substrate is a CMOS silicon chip containing an array of 1-bit digital memory cells [**4**]. The data bit stored at each pixel is present as a voltage (0V / $+V_{DD}$) on a discrete conducting metal pad on top of the silicon. A cover glass is used to define a thin layer (typically ~1 to 3μm) of FLC; an exact thickness is obtained by means of a spacer layer (not shown) which is often placed outside of the pixel array. The bottom face of the glass is covered by a continuous layer of a transparent conductor such as Indium Tin Oxide (ITO). Thin alignment layers on both inner surfaces are used to determine the alignment configuration of the FLC within the cell. Typically, the

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light for all pixels passes in through a single polarizer and out through a single analyzer.

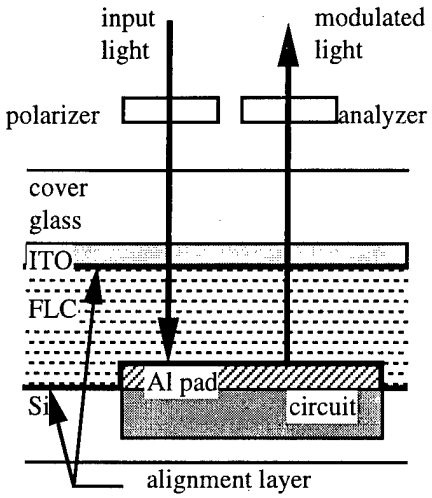

Figure 1 Schematic representation of the construction and operation of a single pixel

Principle of Operation

The FLC layer acts as a pixellated birefringent wave plate whose crystallographic orientation is programmed on a pixel basis by a suitable (polarity and amplitude) of voltage. The voltage is applied across the FLC layer as follows

$$V_{FLC} = V_{ITO} - V_{pad}$$

Although V_{ITO} is common to all pixels, V_{pad} (0V / $+V_{DD}$) can be programmed individually for each pixel. If V_{ITO} is fixed at $V_{ITO} = V_{DD}/2$, the possible values of V_{FLC} are $\pm V_{DD}/2$. Alternatively, occasional toggling of V_{ITO} between 0V and $+V_{DD}$ allows the FLC to be driven by the full voltage of $\pm V_{DD}$, giving faster FLC switching at the expense of a more complicated addressing scheme [**3,4**]. In either case a binary pattern is set up in the FLC as suggested in Figure 2 (amplitude as illustrated or phase).

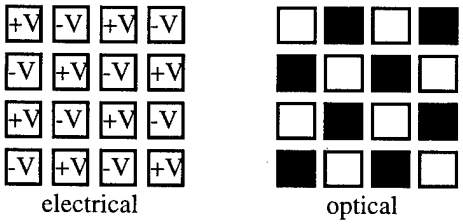

Figure 2. Schematic of portion of SLM pixel array

3 Liquid Crystal Materials and Configurations

Introduction

An often stated advantage of liquid crystals is that they allow a range of optical modulations depending on the precise material and configuration. From the perspective of the SLM designer this is generally true; from the perspective of the applications engineer it is true and relevant only if the precise modulation most suited to the application is available. Here we shall describe how binary amplitude and binary phase modulation are achieved using FLC.

Smectic LC

Most LC materials are characterized at the molecular level by anisotropic molecular shape leading at the bulk level to anisotropy in macroscopic properties such as refractive index; the average orientation of the long molecular axis (called the director) corresponds to the extraordinary axis of the liquid crystal [**5**]. The smectic LC mesophase is characterized by positional ordering of the molecules over a short range and orientational ordering over a longer range. In particular, the molecules reside in thin layers with the director at a fixed, usually small, angle to the layer normal as shown in Figure 3.

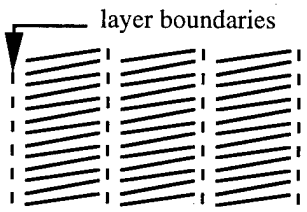

Figure 3 Schematic representation of smectic mesophase

In smectic C materials, the molecules typically contain a dipole. Alignment of the molecules gives alignment of the dipoles which leads, in the bulk, to ferroelectric properties.

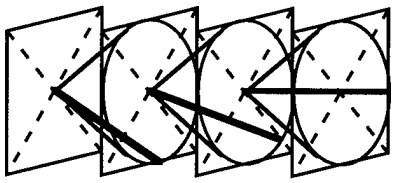

Figure 4. In Sm C* FLCs the director orientation exhibits an offset between adjacent layers

In chiral smectic C (or Sm C*), the director orientation varies in a controlled fashion from layer to layer. Constrained to lie on the surface of a cone, on progression through the layers the director (bold line) precesses around the cone as shown in figure 4.

Surface stabilized FLC

For binary operation, the most common configuration of FLC is based upon surface stabilization of the FLC (or SSFLC) [6]. This effect is explained in detail elsewhere and briefly here. Constrained in a thin layer (no more than a few microns) between two flat substrates, the director within each smectic layer is constrained to lie parallel to the substrates; this gives two options for the director orientation, demonstrated as E and W in layers n-1 and n+1 respectively in Figure 5.

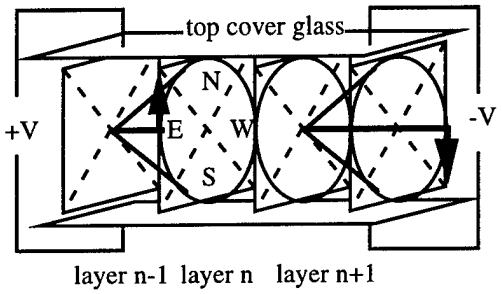

Figure 5 Two possible states of the director in SSFLC; arrows represents the dipole orientation in each state

Amplitude Modulation

Consider a transmission mode FLC cell placed between crossed polarizers. With the FLC director parallel to the input polarizer then the light transmitted through the cell remains linearly polarized and is blocked by the output polarizer - see Figure 6. If the state of the FLC is then switched by means of an applied voltage, the FLC director rotates through an angle 2ϕ, where ϕ is the angle between the director and the normal to the layer planes of figure 5. The polarization vector of light transmitted through the cell is rotated by twice the angle through which the director has shifted, i.e., 4ϕ. In this configuration the output, I, is given by

$$I = I_0 \sin^2(4\phi) \sin^2(\Delta n d\pi / \lambda)$$

where

I_0 is the maximum possible output
Δn is the birefringence
d is the cell thickness
λ is the wavelength

In transmission, it can readily be shown that, for maximum optical efficiency

$$\phi = 22.5 \text{ degrees and}$$
$$d = (2m+1)\lambda / 2\Delta n$$
where $m = 0,1,2,...$

Devices of other cone angle or thickness can produce useful modulation but will exhibit lower light throughput in the ON state. In practice, FLC materials are readily available with cone angles of around 22.5 degrees; a typical value of Δn is 0.15, giving a cell thickness of around 1.5μm in the visible wavelength region.

In reflection mode,

$$d = (2m+1)\lambda / 4\Delta n.$$
where $m = 0,1,2,...$

This suggests a minimum (i.e., $m = 0$) FLC thickness of around 0.75μm. In practice SLMs of this nominal FLC thickness can be difficult to produce with acceptable small thickness variations both within and between devices. The alternative is to aim for a FLC thickness of

$$d = 3\lambda / 4\Delta n.$$

or just over 2μm, trading off likely better uniformity for slower FLC switching.

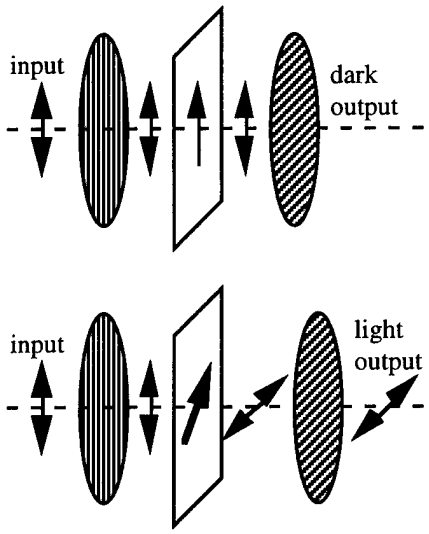

Figure 6. Binary amplitude modulation by FLC. Top - dark state. Bottom - Light state

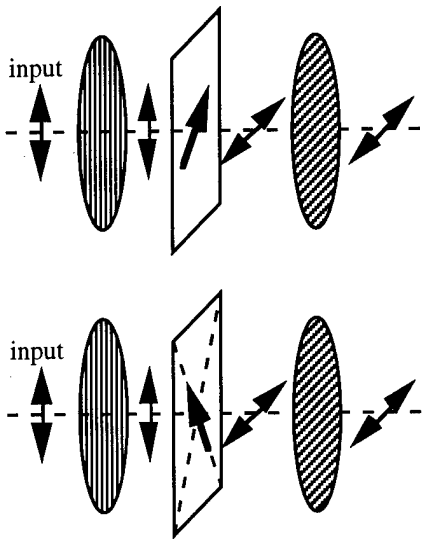

Figure 7. Binary phase modulation by FLC. Bottom - polarization rotated clockwise by FLC. Top - polarization rotated anti-clockwise by FLC.

Phase Modulation

A number of schemes have been proposed, and indeed demonstrated, for binary phase modulation. For maximum optical efficiency and π phase difference the thickness constraint is as before, however in this case

$$\phi = 45 \text{ degrees}$$

and the input polarization should be set to bisect the angle between the two possible director orientations as shown in Figure 7.

Once again, devices of other cone angle or thickness can produce useful modulation but will exhibit greater light loss. FLC materials with $\phi \sim 45$ degrees are not widely available.

Practical Issues

There are some practical issues concerning the use of FLC layers in CMOS backplane SLMs which are worthy of mention.

Contrast Ratio. In transmission mode cells, contrast ratios (CR) of $> 10^3$:1 have been achieved. The contrast ratio of FLC/CMOS SLMs is limited primarily by light leaking through pixels in the OFF state to values in the range 10:1 to 100:1. This is a function of the relatively poor alignment of FLC on the backplane (usually sputtered or evaporated aluminium or aluminium alloy with a relatively rough surface) which leads to the presence of multiple FLC domains within a pixel.

Bistability. While the SSFLC configuration is often described as bistable, in practice good bistability is often difficult to achieve in a silicon backplane SLM. A consequence of this fact is that the optical output of a pixel is voltage dependent. In other words, a stable drive voltage is required to produce a stable optical output.

DC Balance Requirement. It is widely recognized that, in order to avoid chemical, and consequently optical performance, degradation of a LC layer, the net drive voltage across the layer must be zero over a given time period. Generically

$$\int V\,dt = 0$$

over a time period of, say, around a second. Where a bipolar voltage is driving a FLC layer this is often made more specific - *"for every positive voltage pulse driving the LC, a negative pulse of equal duration must also drive the LC"*. This has significant consequences for FLC/CMOS SLMs [**3,4**].

Switching Speed. FLC switching speeds up with increasing drive voltage, increasing temperature and shrinking cell thickness. For cell thickness of 1 to 2 μm and typical CMOS drive voltages of 3 to 10 V, switching times typically range from around 10 to 200 μs.

Cone Angle. FLC cone angle is temperature dependent, rising from zero degrees as the temperature falls from the critical temperature.

Wavelength Dispersion. The birefringence of FLC materials is wavelength dependent. This means, for example, that in polychromatic applications (e.g., displays) FLC layer performance can be optimised for only one wavelength.

Summary. Some of the above properties are poorly characterized even for commercially available materials. Optimal device performance may require the detailed characterization of material parameters and dependencies as well as careful tolerancing of the critical device dimensions and operating conditions. In particular the custom design of materials and mixtures for use in silicon backplane driven devices is under way [**7**].

Other LC materials and configurations

While this article deals with binary FLC/CMOS SLMs, other LC materials and configurations exist which are capable of fast switching and analog modulation of the amplitude or phase of light. These include the distorted

helix effect (DHF) [8], the soft mode electroclinic [9] and antiferroelectric LC [10]. SLMs using some of these materials have been constructed [11,12].

4 Pixel Design

Most of the FLC/CMOS SLMs designed to date are based upon one of two fundamental pixel designs. The two root pixel designs [3] are in turn based upon (I) dynamic memory - the single transistor dynamic random access memory (DRAM) cell [13], and (ii) static memory - the six transistor (6T) static random access memory (SRAM) cell [13].

Dynamic Memory Pixel

In terms of the electronic circuit, the single transistor dynamic memory pixel is analogous to two other widely used cells - the pixel circuit for an active matrix LCD [14] and the DRAM cell for conventional electronic memory. (In the former case the active switching element is usually a thin film amorphous silicon or polysilicon transistor rather than, as in the latter, a MOSFET.) We shall henceforth refer to this pixel design as "DRAM".

The pixel circuit is sketched in Figure 8. The elements of the circuit are

- column bus line containing the voltage to be driven into the pixel
- row bus line controlling the state (ON/OFF) of the MOSFET
- MOSFET switch determines when the pixel is isolated from / connected to the column bus
- capacitance, C_{sub}, stores the pixel voltage and presents it to the FLC via the mirror / pad
- ITO counter electrode (common to all pixels)

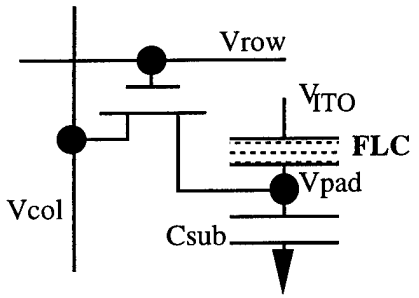

Figure 8. Single transistor pixel circuit

Advantages of DRAM pixel. The DRAM pixel design has a number of key advantages. These are

- Small area. As with electronic memory the 1T DRAM design has the smallest possible area and, for a given fabrication process, allows the maximum pixel packing density
- Low complexity. This is a very simple circuit. Of course, in order to maximise the performance of the circuit, the complexity of the fabrication process may have to be increased.
- Unipolar circuit. The cell contains no complimentary structures (i.e., nMOS and pMOS devices in close proximity).

Disadvantages of DRAM pixel. The disadvantages inherent in the DRAM pixel design are now listed.

- Loss of drive voltage. Assuming a supply rail voltage of V_{DD} on the silicon backplane, and assuming that in order to drive the pixel mirror high V_{DD} is applied to both row and column bus lines, the maximum voltage reaching the pixel mirror is

$$V_{pix,max} = V_{DD} - V'_T$$

where V'_T is the threshold voltage of the pixel MOSFET *enhanced by the body effect.* (The body effect boosts the threshold voltage from the zero bias case, V_{T0}, to a higher value when a positive potential is present between source and bulk [15].) For typical values of V_{DD} = 5V, V_{T0} =1V, then V'_T ~ 1.5 to 2V and $V_{pix,max}$ ~ 3 to 3.5V, i.e., $V_{pix,max}$ ~ 0.7 V_{DD} A loss of drive voltage represents a reduction in switching speed, a loss of stored charge on C_{sub}, a potential asymmetry in the efforts to dc balance the FLC and a variation in $V_{pix,max}$ because V_{T0} exhibits a natural process variation. The full magnitude of the column voltage, V_{DD}, can be achieved at the mirror only by applying a suitably larger voltage ($>>V_{DD}$) to the MOSFET gate via the row line.
- Drive limitations. The charge required to fully switch the state of the SSFLC is

$$Q = 2P_S A$$

where
P_S is the spontaneous polarization of the FLC and
A is the pixel area
The charge stored on the pixel mirror is

$$Q = C_{sub} V_{pix,max}$$

For efficient fast switching of the FLC, clearly we require

$$C_{sub} >> 2P_S A / V_{pix,max}$$

Insufficient charge storage (either too small a value of C_{sub} or too high a value of P_S) leads to slow or even incomplete switching of the FLC.

- Charge leakage. C_{sub} consists of several components, one being the capacitance of the reverse biased source to bulk pn junction [**15**]. This junction exhibits charge leakage causing any voltage stored on the pixel mirror to decay towards the substrate potential (0V for nMOS pixel FET, V_{DD} for pMOS). The rate of voltage discharge is increased when photons impinge on the silicon substrate and has been shown to allow a relaxation in the state of the FLC (i.e., a ripple in the orientation of the director) which, in turn, causes a loss of throughput and loss of contrast in SLMs performing amplitude modulation or a phase ripple in SLMs performing phase modulation. Voltage discharge implies a requirement to continually refresh the data in the pixel array before it becomes corrupted. Finally, it represents a real source of asymmetry in the efforts to dc balance the FLC.

Design Aims. The aims in designing the pixel circuit are

- maximise storage capacitance
- maximise flat fill factor
- minimise electrical crosstalk between storage and adjacent nodes
- minimise charge leakage

DRAM Pixel Summary. The overriding benefit of the DRAM style pixel is that it maximises pixel packing density. Even in an ASIC process, pixel pitch of down to around ten times the process geometry (i.e., 10μm pixel in a 1μm CMOS process) is generally easily possible. To that end much effort has been devoted, over the years, to the design and fabrication of DRAM SLM pixels which minimise the disadvantages listed [**16,17**]. The potential exists to increase pixel packing density further by the use of a DRAM specific process for SLM backplane fabrication.

Note. The DRAM style pixel is inherently an analog storage circuit (albeit neither robust nor linear) and is thus eminently suitable for use with analog LC materials. Much of the complexity of such analog SLMs lies in the drive circuits peripheral to the pixel array [**11**] and in the addressing schemes required in order to overcome the disadvantages described above.

Static Memory Pixel

In applications where one of the following takes precedence over pixel packing density

- switching speed
- output stability (phase or amplitude)
- high optical input power

static memory represents a preferred alternative to DRAM. A standard 6 transistor static RAM (6T SRAM) cell [**13**] is shown in Figure 9. A SLM based upon this pixel circuit would require one of the complimentary nodes of the SRAM to connect to the pixel mirror.

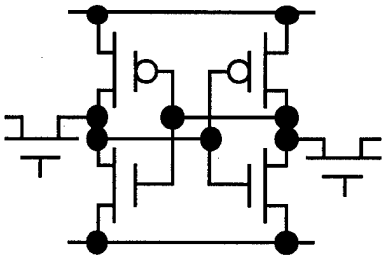

Figure 9. Six transistor static RAM circuit

In general, performance and stability is improved by inserting a buffer between the SRAM and the mirror as shown in Figure 10. Typical buffers include the 2 transistor MOS inverter [**18**] and the 4 transistor MOS XNOR or XOR gate [**19,20**] (the latter pair being functionally equivalent in this context).

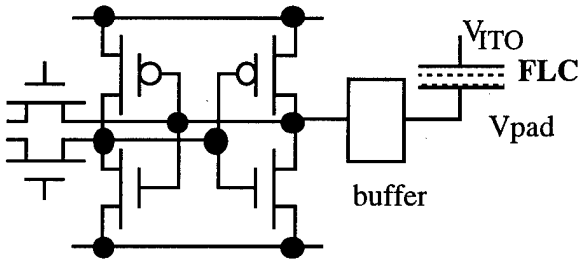

Figure 10. Static RAM based pixel circuit

The advantages and disadvantages of the SRAM style pixel circuit are complimentary to those of the 1T DRAM pixel circuit.

Advantages of SRAM style pixel

- V_{DD} drive voltage. The full power rail voltage of the backplane is available to drive the FLC
- Unlimited charge capacity. In this case the mirror is always shorted to one or other of the power rails via a MOSFET in the ON state thus allowing as much charge as required to flow on or off the mirror.
- Stable drive signal. The pixel mirror voltage is not subject to reduction as the FLC switches. Thus high P_S, high speed FLC materials can be used. Nor is the voltage subject to decay or leakage.

Disadvantages of SRAM style pixel

- Large area. The SRAM style pixel takes up a larger area (with a pitch of typically twenty to thirty times the process geometry).
- Latchup danger. The complimentary nature of the circuit leaves the pixel vulnerable to latchup (a permanent and destructive failure mechanism) which can be induced by the presence of light in the substrate [21].
- Switching transients. In large arrays the transient current produced by switching the state of a large number of SRAM cells simultaneously can cause temporary or permanent damage to the backplane.

Design Aims. The aims in designing the pixel circuit are

- maximise flat fill factor
- minimise switching current
- ensure sufficient latchup protection

SRAM Pixel Summary. The overriding benefit of the SRAM pixel circuit is its ability to apply a greater voltage and charge to the FLC. This is achieved at the expense of silicon real estate.

4 CMOS Silicon

Floor plan

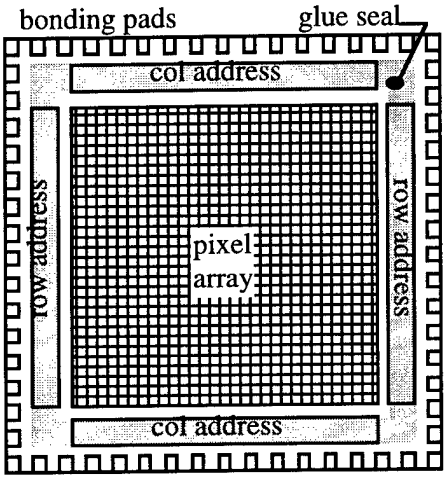

Figure 11. Schematic of typical SLM floorplan

Figure 11 shows a typical floorplan for a device. Electronic data flows into the bonding pads to be routed by the row and column address circuitry into the pixel array. Die sizes range up to around 20mm. The pixel array is typically 4 to 5mm less wide than the die. The area between the pixel array and the bonding pads is used for a glue seal to which the cover glass is attached.

Addressing the array

Data is normally written into the pixel array row-at-a time. The address circuit determines whether the array is addressed row sequentially or in any chosen order. Data for a row is assembled at the column drivers and transmitted to the column address lines. A pulse is then sent to the gate lines of a row of pixels which switches on the MOSFETs for that row, thus allowing the data to flow onto the mirrors as shown for the middle row of DRAM pixels in Figure 12.

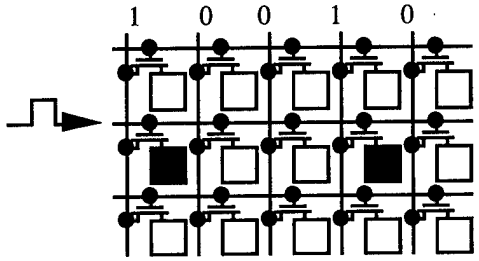

Figure 12. Data is written to a row of pixels by a pulse on the gate line. In the row being addressed here, black represents a logic zero and white represents a logic 1.

Consequences of DC balance

The requirement to DC balance the FLC at the pixel level is generally achieved at the SLM level as follows. Once a frame of data is written onto the array and optically interrogated to produce a bit plane image, it is immediately followed by a complimentary frame, i.e., one which produces the inverse of the image. The main consequence of this form of addressing is that the useful frame rate of the SLM is reduced, normally halved. A second consequence is that, in order to "see" only the actual image, the complimentary image is usually not interrogated. In other words, the read beam must be pulsed an synchronised with the SLM. A further consequence is that even for a still image, the SLM data must be constantly updated. Suitable combinations of addressing scheme and pixel circuit design can, at least partially, alleviate all of the above [22,23].

Frame rates

The electronic frame address time [24,25] for a FLC/CMOS SLM addressed line sequentially is given by

$$t_{frame} = 2\,(t_{address} + t_{FLC} + t_{interrogate})$$

where

$t_{address}$ is the time to electronically address the full frame

t_{FLC} is the FLC switching or settling time

$t_{interrogate}$ is the time during which the the SLM is illuminated

The factor 2 above arises due to the DC balancing requirement.

$t_{interrogate}$ is application specific, depending on the light output requirements.

t_{FLC} is device specific; it depends upon FLC material, drive voltage, temperature etc.

$t_{address}$ is given by

$$t_{address} = NM / fw$$

where

N is the number of rows
M is the number of columns
f is the bus clock frequency
w is the bus width

i.e., NM is the number of pixels and fw is the bandwidth of the address bus. For example, a device containing 1024x768 pixels driven at 60Mhz via a 64 bit wide bus has $t_{address}$ = 200μs and a burst data rate of almost 4 Gbit/s.

Power dissipation

The issues of backplane design for FLC/CMOS SLMs are primarily two fold - small scale pixel level circuit and layout design as discussed above and large scale chip / system level high speed digital design concerned with clock distribution and skew, current pulse handling and power routing and dissipation. Power dissipation from electrical switching and, in high intensity applications, from absorbed light can, in large fast devices, be significant. In the EU 512x512 pixel device (mentioned in table 1) operated at 50Mhz, electrical power dissipation on chip is around 100mW. McKnight and co-workers discuss the dependency of electrical power on the nature of the data being displayed [**26**].

5 FLC/CMOS devices

Post Processing

The surface finish of standard silicon wafers is not sufficient for SLMs in several ways

- poor flatness - underlying topology affects the surface profile of the mirror
- poor smoothness - too granular, affecting reflectivity and FLC alignment quality
- low flat fill factor - that fraction of the pixel area covered by a flat mirror electrode

One solution to these shortcomings has been the development of SLM specific wafer post-processing techniques for "planarization" of the silicon backplanes. Two main lines have been followed with significant success

- chemical-mechanical polishing (CMP) [**27**,**28**,**29**]
- spin-on coating (SOC) [**30**]

In both cases the process flow is outlined as follows

1. apply planarized dielectric layer - either spin-on polymer or low temperature PECVD oxide followed by CMP
2. etch via holes
3. deposit and pattern additional metal layer to give larger
4. (i.e., higher fill factor) flatter mirrors

Figure 13 shows electron micrographs of a backplane before and after an early planarization. Recent [**31**] developments have reduced the gap between mirrors and the via size, leading to a further increase in flat fill factor.

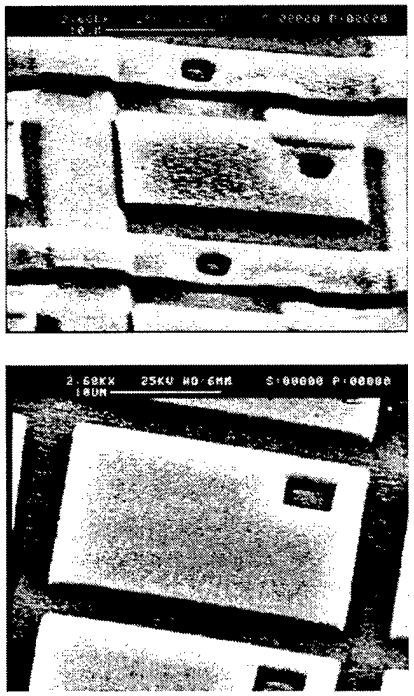

Figure 13. Silicon backplane before (top) and after (bottom) planarization by CMP

A recent development concerns use of damascene processing [**32**] to allow the mirrors to be recessed into the underlying oxide thus effectively fillng the trenches [**31**] usually left (see figure 13b) between the mirrors.

Cell Fabrication and Filling

Some of the current bottlenecks in device performance arise from lack of uniformity in

- FLC alignment
- FLC layer thickness
- global (i.e., chip scale) backplane flatness

Clearly, the final two are linked. The last is more of a problem for non-imaging (e.g., crossbar) systems than for imaging systems.

The contrast ratio and uniformity levels achieved in silicon backplane devices generally fall well short of those achieved in glass on glass test cells. Clearly the silicon backplane is not as "alignment friendly" as a glass substrate so particular attention has to be paid to the alignment layer. A number of techniques have been discussed and implemented for achieving LC alignment in general [**33**]. These include rubbed and treated polymers, evaporated ITO, Langmuir-Blodgett films and UV cured polymers. Some recent work suggests that the cell filling process plays a part in determining the alignment in a silicon backplane device [**34**]. This is an area in which there is much physics still poorly understood and where there is significant potential for performance improvement.

FLC cell thickness is typically set by the use of calibrated spacer balls or rods spread across the chip surface by blowing, or spun-on in a (subsequently evaporated) liquid. Some devices simply use high points in the topography available on the backplane to provide a cell gap [**18**] but this is haphazard as well as being incompatible with planarization. Recent work has demonstrated the feasibility of adding pillars of oxide to the backplane as an addendum to the planarization process in order to form inert spacers of precise and uniform height [**31**].

When diced from the wafer and examined interferometrically, backplanes typically exhibit several fringes indicating a significant bow or lack of flatness. Bowing at the global or chip scale on a device used in reflection mode gives rise to aberrations in the optical system. The bowing varies from chip to chip and so could only be compensated on an individual basis. Meanwhile, achieving absolute (i.e., optical) flatness of the backplane in a finished device is problematic. Several potential solutions currently being investigated include the fixing the backplane to an optically flat substrate, fixing the backplane to a thick optically flat cover glass and depositing stress relieving layers on to the back of the wafer prior to dicing.

6 The State of the Art

Some idea of the state of the art in backplane technology can be gained from Table 1. In summary, pixel counts of 256^2 to around 1000^2 are now (or, in some cases, soon will be) available. Pixel pitches of less-than-ten to a-few-tens-of microns are common. Planarized fill factors (not tabulated here) are commonly in the range 80% to 90%. I have not included many of the more detailed performance criteria such as frame rate and optical efficiency as these figures are measured or quoted in ways which are not always directly comparable.

In FLC technology typical switching speeds of a-few-tens to around a hundred microseconds can be obtained with CMOS compatible drive voltages. Materials with cone angles of close to 22.5 degrees are available. Contrast ratios of around 10:1 to 100:1 are being achieved in SLMs. This is much poorer than is available in test cells a fact which is generally attributed to difficulties is FLC alignment over silicon backplanes. Generally speaking, materials with higher P_S and / or smaller cone angle exhibit faster switching and cells with stronger bistability exhibit slower switching.

No of Pixels	Year	Pixel Pitch (μm)	Pixel Type	Design House	Status[1]	Ref	Notes
64^2	1992	80	DRAM	EU	no longer available	-	high voltage drive
64^2	1992	50	Buffered DRAM	CU	no longer available	-	
64^2	1990	60	SRAM	DT	no longer available	**18**	
64^2	1995		DRAM	CU	no longer available	**35**	high voltage drive
128^2	1992	22	DRAM	CU / BNS	available to buy	**3**	
128^2	1995	40	DRAM	CU / BNS	no longer available	**11**	analog
176^2	1990	30	DRAM	HPSLM	available to buy	**4**	planarized
256^2	1995	40	SRAM	EU	available to buy	**20**	planarized
256^2	1995	15* & 30	SRAM	DT	available to buy	**36**	*planarized
256^2	1996	40	DRAM	BNS	available to buy	-	analog
256^2	1994	21.6	DRAM	CU/ BNS	available to buy	**26**	
320x 240	1997	34	DRAM	CUED / DRA	demonstrated	**37**	high fill factor unplanarized
512^2	1995	20	DRAM	EU	demonstrated	**17**	light protected
512^2	1997	7.68	DRAM	BNS	in design	-	analog
640x 480	1996	13	N / K	DT	available to buy	-	
640x 512	1996	21.4	DRAM	CU	under test	**30**	analog / digital
1024x 768	1997	12	DRAM	SLIMDIS	demonstrated	**38**	light tight
1280x 1024	1997	7.6	DRAM	DT	in design	**39**	

Table 1. Sample of recent FLC/CMOS SLM Backplanes[2]

Key

Design house : BNS - Boulder Nonlinear Systems; CU - University of Colorado; CUED - University of Cambridge, UK; DRA - Defence Research Agency, UK; DT - Displaytech; EU - University of Edinburgh, UK; HPSLM- EU, GEC Marconi and STC Technology. SLIMDIS - SLIMDIS Consortium, UK[3].

Other N / K - not known by the author

7 Applications

Historically, the main applications for FLC/CMOS SLMs have been

- crossbar switching [**40**]
- telecomms switching [**41**]
- optical correlator (input and/or Fourier plane) [**42,43**]
- dynamic holography [**44,45**]

More recently, the increase in capability of the technology has led to its use as a component in miniature display systems [**36,39,46,47,48**] for use in head mounting, projection and other applications. A simple schematic of the heart of such a system is shown in Figure 14. The illumination subsystem typically consists of a white light source and fast-switching colour filter or red, green and blue LEDs. A full color single frame is made up of a number of sequentially displayed bitplanes, each

[1] For up to date availability, contact the design house except EU 256^2 - contact CRL Smectic Technology, Hayes, UK.

[2] Completed to he best of the author's knowledge, 1 June 1997.

[3] SLIMDIS - GEC Marconi Research Centre, Admit Design Systems, Davin Optical Holdings, Swindon Silicon Systems, The University of Edinburgh.

illuminated by the appropriate color light. For example, by binary weighting successive bit-planes illuminated by one color, n bit-planes can display 2^n colors.

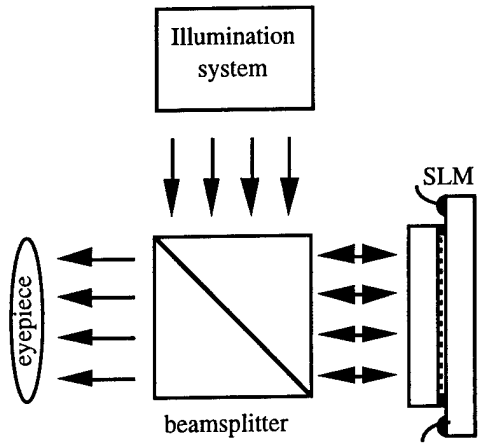

Figure 14. Basic schematic of miniature display system

The primary advantages of silicon backplane displays over other display technologies are

- small physical size (of course, image size can be made much larger using magnifying optics)
- ease of including additional on chip circuitry

Figure 15. A bit-plane color picture on a 176x176 SLM reproduced in greyscale. Some of the addressing circuitry at the edge of the pixel array is apparent

The primary advantage of this bit-plane display technology over other, e.g., analog nematic LC over silicon and active matrix LCD technologies is that with, this technology, each pixel exhibits the full range of color. (Other technologies require a triad consisting of a one red-, one green- and one blue-filtered pixel to produce a full range of color). The bit-plane approach produces a significant improvement (not apparent in Figure 15) in image appearance at high magnification.

8 Future Prospects

The prospects remain good for the continued development of FLC/MOS SLMs. The emergence of display applications has injected a previously lacking level of urgency and funding into the area thus increasing the level and pace of competition.

Specific directions in which the technology is likely to move in the near future include the development and use of

- small geometry silicon processes and specialised technologies such as BICMOS to speed up frame rates
- custom silicon processing and/or post-processing to optimise the optical and electrical performance of the pixel
- LC materials and mixtures designed and / or optimised for use in silicon backplane devices
- customised mechanical, optical, illumination and electronic interface components
- application specific SLM designs for, e.g., displays, correlators etc.
- accepted standards for bit-plane displays
- mass production processes and facilities to facilitate large volume low cost manufacture

It is likely that the miniature displays market will bring down the cost and drive up the availability of SLMs to the point that other systems, previously classed as not economically viable, will become feasible.

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A new high resolution FLC/VLSI Spatial Light Modulator

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Abstract

Recent advances in custom silicon design, post-processing technology and the use of new commercially available ferroelectric liquid crystal (FLC) mixtures has led us to develop a faster and higher resolution backplane. The backplane does not only have uses in incoherent illumination systems such as displays[1] but in coherent systems such as optical computing where a high optical through-put is desired.

Keywords

SLM, VLSI, FLC, DRAM pixel, display.

Introduction

The 512SLM was designed by Burns[2] and fabricated in 1996 by AMS using a 1.2μm 5.5V n-well CAE (epitaxial wafer, n-well, double polysilicon and double metal) CMOS process. This device incorporates an enhanced DRAM pixel, which drastically reduces the effects of pixel charge leakage and a better addressing architecture to simplify real-time digital video preprocessing. The device uses essentially the same peripheral addressing circuitry as the SBS256 SRAM-XOR SLM[3] making its implementation quick and reliable. With the device having the same physical dimensions as the SBS256 SRAM-XOR SLM, permitted the utilisation of many of the optical / packaging components already available.

The 512SLM consists of a 512 x 512 array of enhanced DRAM style pixels. Each pixel is enlarged using the in-house CMP post processing technique which increases the pixel mirror dimensions to 18.4μm x 18.4μm on a 20μm pitch (see figure 1). This corresponds to an array area of 1.0486cm^2 (10.24mm x 10.24mm) with a pixel fill factor of 85%.

The backplane addressing circuitry (figure 2) is based on a modified multiple serial shift register architecture, consisting of 64 x 8 bit shift registers and a decoder to write an assembled column of data (512 pixels) onto the array. The device has 64 data lines and 15 control lines controlling its operation. Instead of the rolling '0' (active low) column shift register, as used by the 176SLM, a column address decoder exists. This means that the device can be addressed on a column-by-column basis for a digital video sequential scan or in an interlaced format suiting analogue PAL and NTSC video. Data can be loaded onto the array at clock speeds of up to 48MHz (1.92GBits/s), giving rise to an electrical frame address rate of 8kHz. The backplane also includes support circuitry for image inversion which is necessary when addressing FLC in a DC charge balancing mode.

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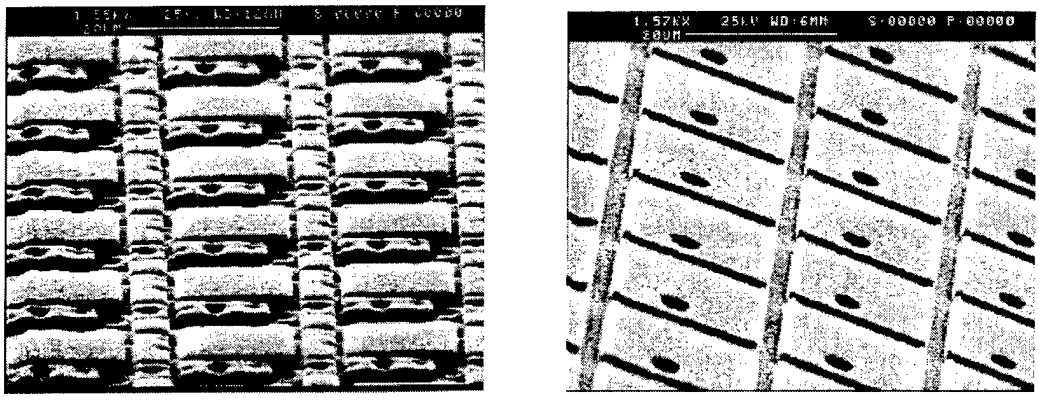


Figure 1: SEM micrographs showing the 512SLM before / after in-house CMP planarisation.

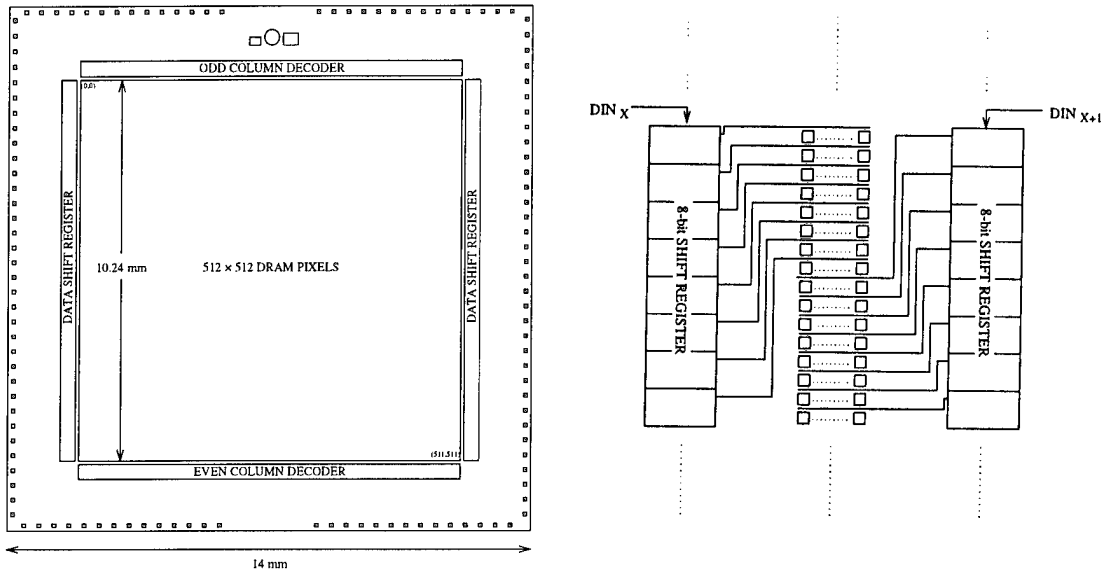


Figure 2: 512SLM architecture overview.

Enhanced DRAM pixel

Each pixel incorporates a pMOS pass transistor and a pMOS storage transistor capacitor along with the appropriate data, address and power lines. Figure 3 demonstrates the MOS model of the pixel and its silicon implementation. Figure 4 shows a diagrammatic cross sectional view of the enhanced DRAM pixel.

The motivation for this particular pixel design was driven by the desire to have a quick array addressing time whilst storing enough charge and furthermore, to compensate for leakage effects to fully switch the liquid crystal at a single pixel.

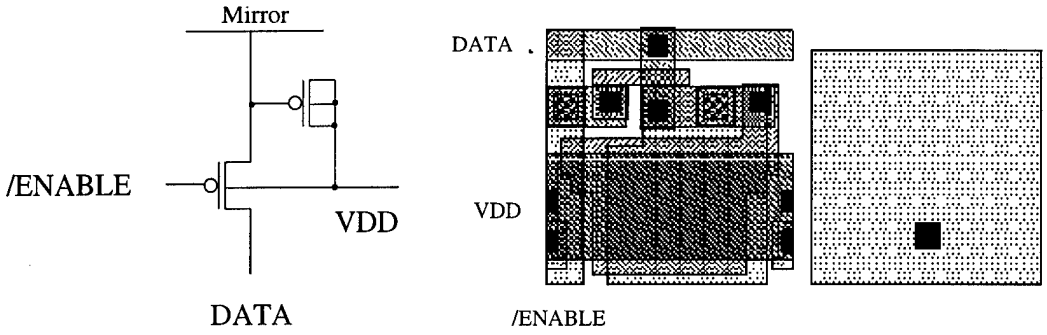


Figure 3: Enhanced DRAM pixel MOS model and its silicon implementation.

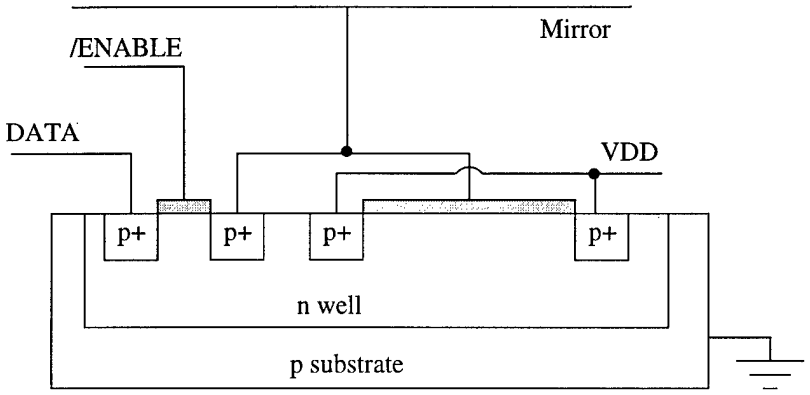


Figure 4: Cross sectional view of the enhanced DRAM pixel.

The concept of using what is essentially a dual transistor pixel is not new since a MOS storage transistor capacitance is the largest attainable. Previous implementations of this design suffered severely from the photoelectric effect since generated electron-hole pairs make the transistor active regions more 'leaky'. The enhanced DRAM pixel overcomes these problems by embedding the whole pixel array in an n-well on top of a grounded p-substrate. The following points detail and summarise the advantage of the enhanced DRAM pixel design.

- Pixel capacitance is large due to the large gate oxide of the pMOS storage capacitor.
- Grounded p-substrate acts as a charge collector absorbing the photoelectric carriers deep within the substrate.
- n-well eliminates all leakage currents associated with the substrate wafer.
- Planarised pixel mirrors shield the MOS capacitor and the address and data lines.
- Parasitic capacitances do not degrade the effectiveness of the storage capacitance since storage capacitance is much larger.

The amount of charge required within a pixel gate time period (typically 30ns) to fully switch the liquid crystal can be obtained experimentally by measuring the amount of current required to reverse the polarisation state of the liquid crystal material.

$$Q_{switch} = 2AP_s \qquad [1]$$

Equation 1 describes this operation and thus it was calculated that 240fC was required to switch the liquid crystal over a single 20μm x 20μm pixel; A = area (20μm x 20μm) and P_s = liquid crystal spontaneous polarisation (~30nC/cm^2 or 0.3fC/ μm^2). The overall storage capacitance of the enhanced pixel is approximately 200fF of which the pMOS capacitor contributes 175fF, the VDD / GATE / MIRROR capacitance's contribute 15fF and the FLC pixel capacitance contributes 10fF (assuming a 2.4μm cell gap). If 5 Volts can be applied across the pMOS storage capacitor, the amount of charge stored is approximately 1000fC, fours times that required for the particular FLC material used. This is good considering that for any image degradation to occur, the pixel will have had to have lost three quarters of its full charge capacity.

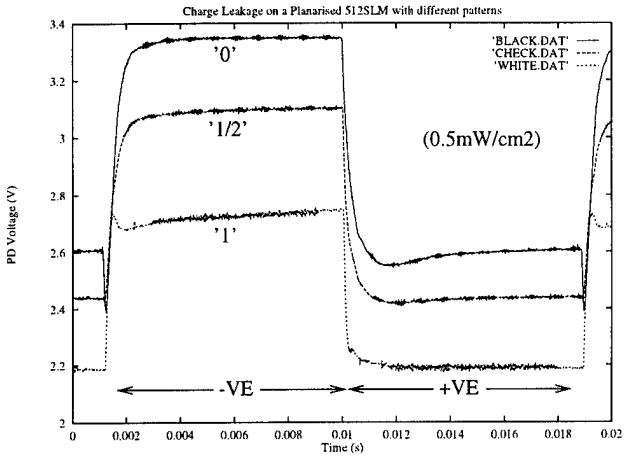


Figure 5: Image degradation effects (charge leakage) during the -ve and +ve addressing cycles of a planarised 512SLM (array fully ON '1', array half ON/OFF '1/2'and array fully OFF '0').

512SLM - An optical characterisation

Figure 5 depicts the charging and discharging characteristics of a planarised 512SLM under a continuous 0.5mW/cm^2 He-Ne illumination. The measurements where taken using a simple optical arrangement and a fast 10MHz calibrated photodiode/amplifier. The optical system consists of a collimated 5mW He-Ne laser, a polarising beamsplitter, 1/2 wave plate, SLM and lense with the photodiode at its focal point.

Figure 6 shows the effect of array charge leakage (FWHM) under different illumination levels. When compared to the 176SLM, the 512SLM is approximately 250 (±10%) times slower at half image discharge, under a continuous 0.5mW/cm^2 He-Ne illumination. In contrast, a SPICE 'dark' simulation showed that the enhanced pixels natural electrical discharge time was extremely long. The device also performs well with respect to its charge storage capability during the positive and negative addressing cycles.

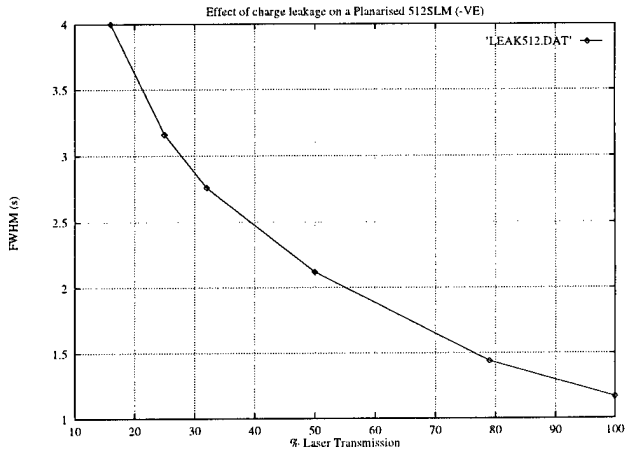
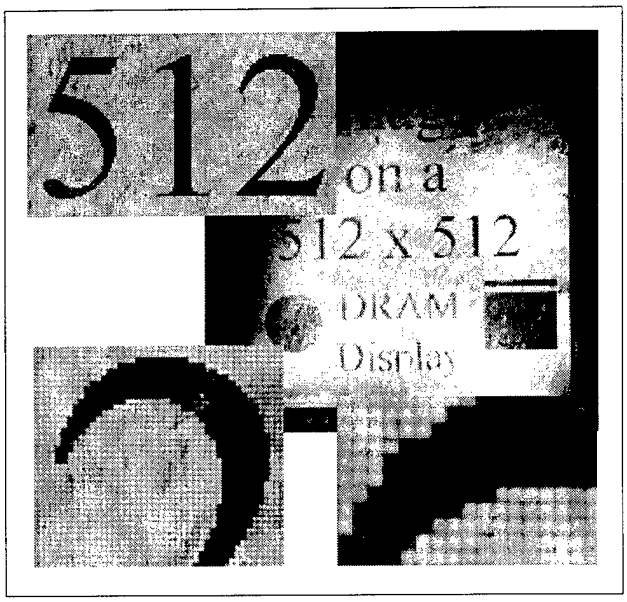


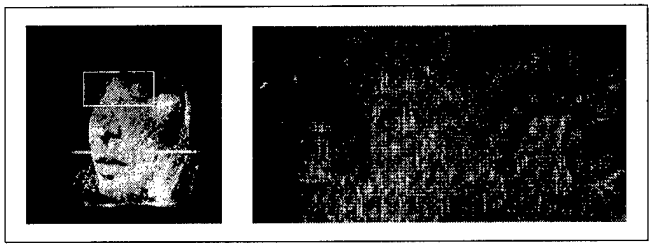
Figure 6: Effect of Photo-induced charge leakage on a planarised 512SLM.(100% laser transmission corresponds to 0.5mW/cm^2)

512SLM performance

Figure 7 demonstrates the functionality of the SLM. The device demonstrated has a array CR of approximately 12:1 under a He-Ne illumination.



(a)



(b)

Figure 7: Single bitplane images on a planarised 512SLM. (a: A single bitplane image; b: A single dithered bitplane image)

Conclusion

From the DRAM devices analysed, the 512SLM performed best under high intensity illumination. It is expected that a two metal planarisation process would make the device as robust as SRAM based devices. Figure 8 compares the planarised 176SLM and 512SLM half image degradation times versus illumination intensity on a log scale. As you would expect with the photoelectric effect, the image degradation is inversely proportional to the illumination intensity (1/I). Extrapolation of this graph enables the determination of the 512SLMs performance under higher illumination intensities outwith the region tested.

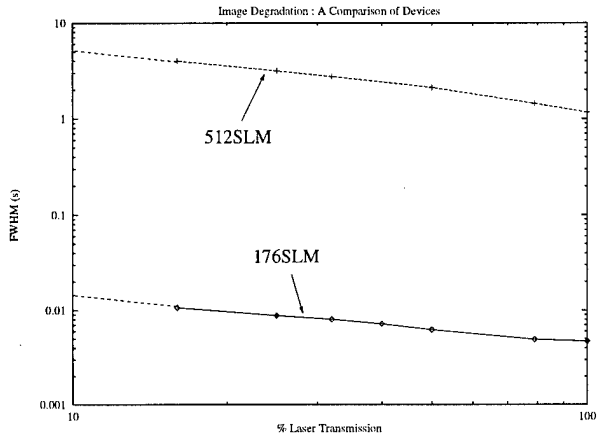


Figure 8: Image degradation comparison of a 176 and 512 SLM. (100% Laser Transmission corresponds to 0.5mW/cm^2)

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Low Voltage Polymer Dispersed Ferroelectric Liquid Crystals

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Abstract

Polymer dispersed ferroelectric liquid crystal (PDFLC) films were prepared and investigated. The saturation voltage of 15 V, the electrooptical response time of 15 μs, and the contrast ratio of 100:1 were reached at room temperature.

Key words

Polymers, Ferroelectrics, Liquid crystals, Electrooptics.

Introduction

Polymer dispersed ferroelectric liquid crystal (PDFLC) films were first developed in 1991 [1,2]. This material provides a fast electrooptical response in addition to the well-known advantages of PDLC. Therefore, one can principally design fast switching electrooptical films for SLM's and displays without glasses, polarizers and special hermetization using PDFLC. These films allow one to increase the light transparency and to simplify the technology in comparison to the monomeric FLC cells.

An electrooptical response is exhibited due to the FLC birefringence and polarizers in a transparent mode[3], or due to the light scattering effect[4].

Now there are available the publications on PDFLC [5-7], which allow to evaluate their outlook, taking into account especially a significant progress obtained during the last years in both the driving voltage diminishing and the bistability.

This work describes different aspects of the PDFLC preparation technology, the modulator design and its investigation (mainly for diminishing the control voltage).

PDFLC films preparation

Two stages of the film preparation can be selected: the PDFLC formation in a polymer matrix, and the one-direction orientation of the droplets. Both processes can be produced simultaneously in some cases. Different methods such as mechanical deformation or tension methods, orientation in the flow under extruding through the thin draw plate [1], dispersion under the magnetic field oriented in the film plane [8], photopolymerization under linearly polarized light and the others can be used for one-direction FLC droplet orientation as for nematics [5,9].

We used thermally induced separation (TIPS) method and chosed the simplest technique of the shift deformation extended usually in labs to reach the one-direction droplet orientation. Widely known thermoplastic - polyvinilbutyral - was used as a polymer matrix in the present work. The weight ratio of FLC materials (##178, 309C, 313, 340 and its modification) and polyvinylbuthiral was 1:2 . The main properties of FLC's which were used are the following:

1. ZhKS-178 with phase transitions temperatures:

$Cr \rightarrow (-10°C) \rightarrow S_C^* \rightarrow (55°C) \rightarrow S_A \rightarrow (69\,°C) \rightarrow I$

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The molecules tilt angle is 27° at 22°C, P_S=90·10^{-9} C/cm^2, $\tau_{0.1\text{-}0.9}$=30 mks at E=10V/mkm, Δn=0.15 (λ=633 nm). The helix is compensated over the whole volume.

2. ZhKS-309C with phase transitions temperatures:

Cr → (-1 °C) → S_C* → (42 °C) → S_A → (91 °C) → I

The molecules tilt angle is 26° at 20°C, P_S=51·10^{-9} C/cm^2, $\tau_{0.1\text{-}0.9}$=11 mks at E=10V/mkm, helix pitch p_o=0.5 mkm, Δn=0.15 (λ=633 nm).

3. ZhKS-340 with phase transitions temperatures:

Cr → (7 °C) → S_C* → (53 °C) → S_A → (86 °C) → I

The molecules tilt angle is 27° at 20°C, P_S=86·10^{-9} C/cm^2, $\tau_{0.1\text{-}0.9}$=23 mks at E=10V/mkm, Δn=0.165 (λ=633 nm). The helix is practically crushed over the whole volume.

4. ZhKS-313B with phase transition temperatures:

Cr → (6 °C) → S_C* → (45 °C) → S_A → (67 °C) → I.

The molecules tilt angle is 21° at 20°C, P_S=55·10^{-9} C/cm^2, $\tau_{0.1\text{-}0.9}$=9mks at E=10V/mkm, helix pitch p_o=3 mkm, Δn=0.145 (λ=633 nm).

FLC droplets in polyvinilbutyral have an ellipsoid form of 3÷9 mkm average size (depending on the conditions). They are placed at one layer not overlapping each other (fig. 1).

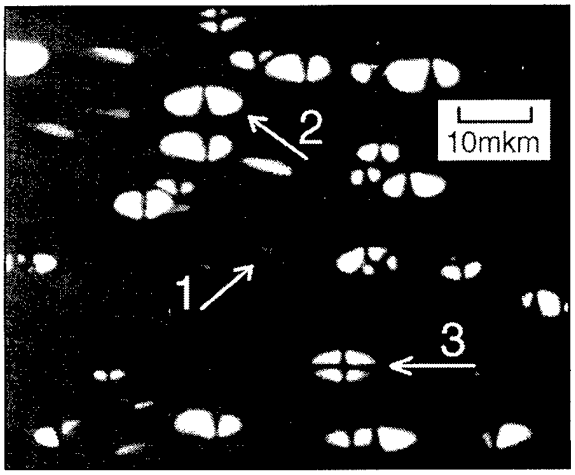


Figure 1. Microphoto of the FLC ZhKS-309C droplets group in a polyvinilbutyral film. The droplets are oriented by the shift deformation. The polarizers are crossed, and the shift direction is parallel to one of them.1 - droplet with a faint wave deformation of smectic layers; 2, 3 - droplets with a confocal domain texture.

One can single out two basic structures of the smectic layers inside the droplets(fig.2).

The first smectic layers structure corresponds to the texture which looks like a planar-oriented FLC layer with a primary director orientation along the shift deformation direction (see fig.1, position 1). The faint wave deformation of the smectic layers (fig. 2a) takes place in this case. The second structure (fig. 2b) corresponds to confocal domains (see fig.1, positions 2, 3). Both smectic layers structures were determined through the interpretation of FLC droplets image given(as for fig.1) by the polarizing microscope.

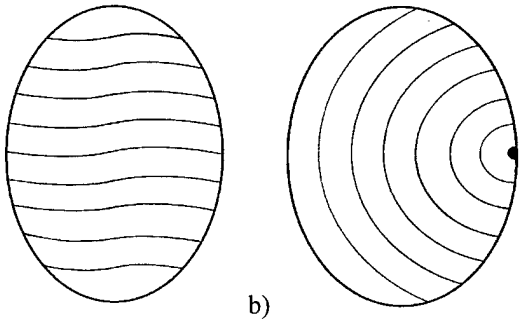


Figure 2. Two main structures of the smectic layers inside the droplets: a) faint wave deformation of the smectic layers which are almost perpendicular to the long droplet axis; b) deformation of smectic layers corresponding to the confocal domain texture.

The structure corresponding to fig. 2a and providing both the high modulation depth and the contrast ratio can be selected due to the technology of PDFLC creation.

PDFLC modulator design

The modulators with one or two polarizers were proposed in [1,2]. The PDFLC film can operate as an electrically controlled birefringent plate when the droplet size and the film thickness are of the same order of magnitude, and then at least one polarizer is used (fig. 3).

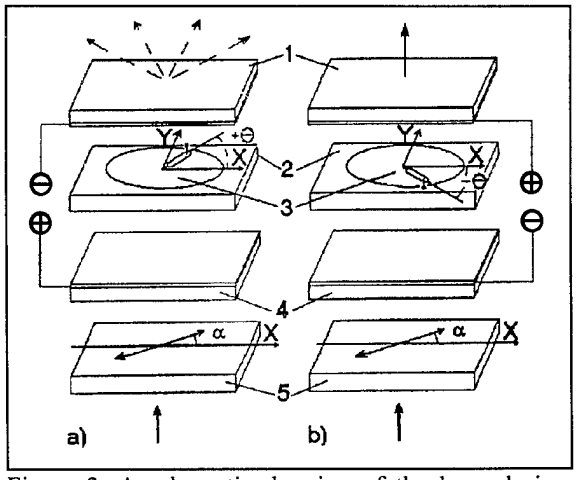


Figure 3. A schematic drawing of the base design of a PDFLC light modulator having at least one polarizer:1, 4 - substrates with transparent electrodes, 2 - polymer film, 3 - FLC-droplets, 5 - polarizers, α - the angle between the long droplet axis and the incident light polarization, θ - the tilt angle of molecules in smectic layers.

Quite good optical contrast 100:1 is achieved in such a film of 3-5 mkm thickness for this transparent mode.

Only the polarized light can be modulated by PDFLC film, and it is sensitive to the light polarization. Both disadvantages are avoided for the structure based on double PDFLC films [4]. Fig.4 shows a schematic drawing of the light valve consisting of two PDFLC cells arranged in series.

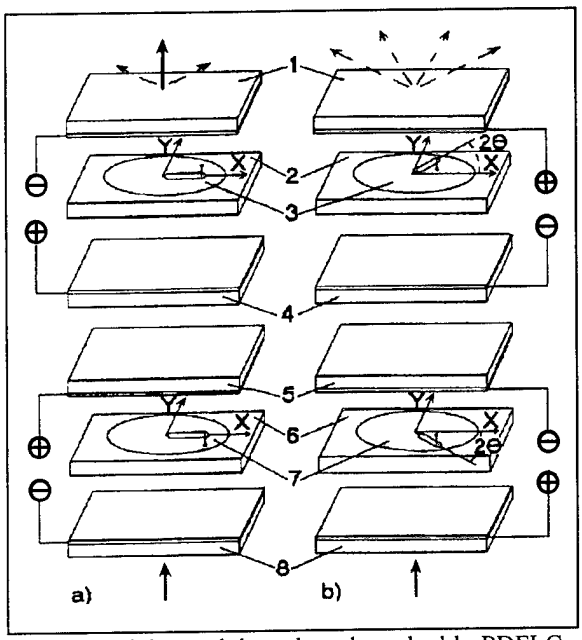


Figure 4. Light modulator based on double PDFLC-cells: 1, 4, 5, 8 - conducting substrates, 2, 6 - polymer films, 3, 7 - FLC-droplets.

PDFLC films in the upper and lower cells are identical, but for opposite directions of the electric field supplied. Fig. 4a shows that PDFLC molecules, under the applied field, are oriented so that their long axes in both films are parallel to each other and lie in the XY-plane. In this case the light with the polarization plane along the Y axis is not scattered when it is passing through the device because of the actual absence of the refractive index gradient on the polymer LC-droplet interfaces. So, the described arrangement is essentially a system of parallel oriented scattering polarizers [4].

Fig. 4b shows that the molecules turn at an angle of $2\theta=45°$ under the electric field polarity change, but still remain in the XY-plane. The molecules in the upper and lower films turn in the opposite directions to the X axis, so the angle between them becomes $4\theta=90°$. In this position the PDFLC device scatters the light of any polarization, like a nematic PDLC.

Double PDFLC films based on the light scattering effect possess not high light transparency (up to 30 percent until now).

Dynamic characteristics

It was shown [2] that the normalized to the electric field electrooptical responce time value, under the applied AC voltage, for PDFLC is the same as for monomeric FLC (namely DOBAMBC). The relaxation time of the droplets after the electric voltage switching off was several orders less than for monomeric FLC.

One can see that two types of bistability [5,7] are observed in the PDFLC with different FLC compositions and thickness.

It is possible to choose the PDFLC composition and preparation technology to provide the required electrooptical response time: from 10^{-5} to 10^{-3} seconds of the switch on time, and from 10^{-5} seconds to hours (days) for the relaxation time.

The switch off time τ_{off} under unipolar driving voltage is practically independent on the electric field tension, like the polymer dispersed nematics, but the value τ_{off} is about 100 mks. This is confirmed experimentally for the PDFLCs with the film thickness of 9 mkm, and the droplet size of 3 mkm (Fig.5).

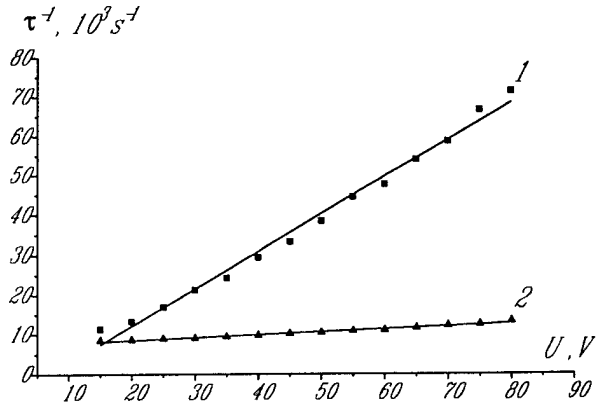


Figure 5. $\tau^{-1}_{0.1\text{-}0.9}(U)$ dependence for the AC driving voltage (curve 1), $1/\tau_{off}(U)$ for the unipolar driving voltage (curve 2). PDFLC layer thickness is 9 mkm, the droplet size is 3 mkm, the temperature is 22°C. PDFLC based on the FLC ZhKS-309C was used.

It is necessary to point out especially that the electrooptical response time $\tau_{0.1\text{-}0.9}$ for the AC driving voltage slightly depends on the disposition of FLC inside the polymer droplet or inside a monomeric FLC cell. This time was 15 mks at 8.4 V/mkm in optimized PDFLC film with 3 mkm droplet size at room temperature (Fig.6).

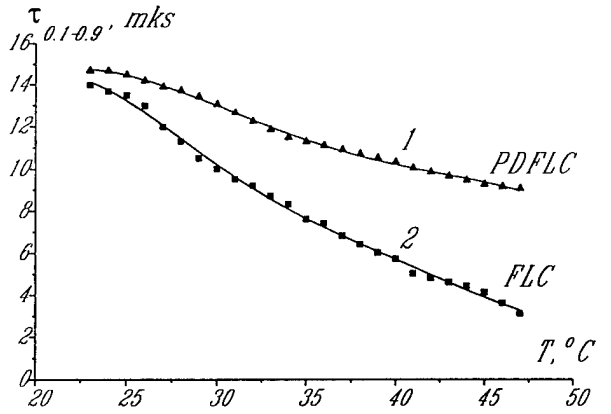


Figure 6. Temperature dependencies of electro-optical response time $\tau_{0.1\div0.9}$ for monomeric FLC cell on the base of ZhKS-309C (curve 2) and PDFLC on the base of ZhKS-309C with droplet size d_o=3 mkm (curve 1) for AC driving voltage and the electric field tension E=8.4 V/mkm.

Driving voltage

The driving voltage value is a critical parameter for PDFLC modulators, especially for the light scattering mode devices. This value must be not less than the saturation voltage V_{sat} . The saturation voltage strongly depends on the polymer type and the parameters of FLC, and was 250÷350 V when the PDFLC investigation was started [1]. Then it was diminished to 40 V [5] and 25 V [6].

Typical electric field/light transmittance dependencies of PDFLC cells in comparison with the monomeric ones are shown in fig.7.

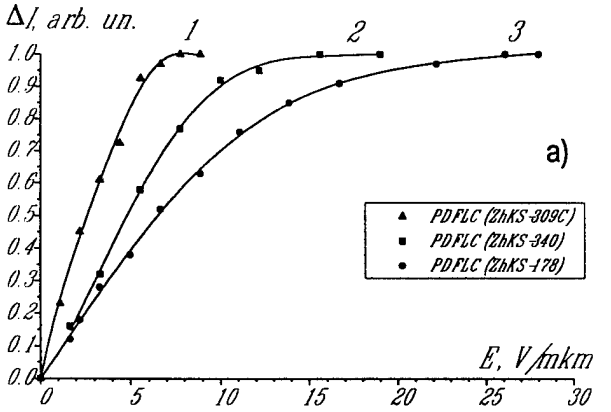
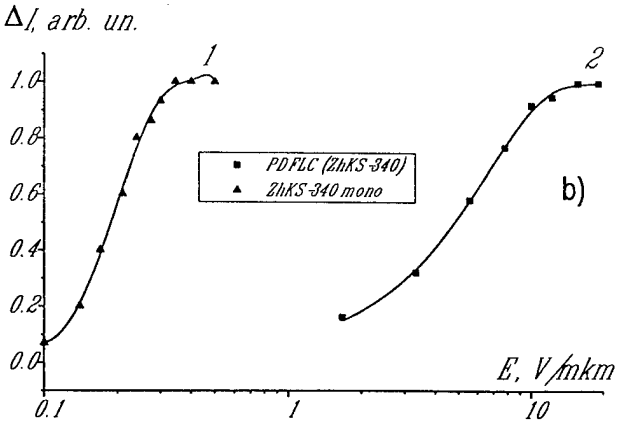


Figure 7. Electric field - light transmittance characteristics at 20°C:

a) PDFLC films of the 9.5 mkm thickness and the droplet size of d_o=3 mkm based on different FLC's: ZhKS-309C (curve 1), ZhKS-340 (curve 2), ZhKS-178 (curve 3).



b) monomeric FLC ZhKS-340 layer of 5.8 mkm thickness(curve 1), PDFLC film on the base of ZhKS-340 (curve 2) of 9.5 mkm thickness and the droplet size d_o=3 mkm.

One can see that U_{sat}= 97 V for PDFLC and U_{sat}=3 V for the corresponding monomeric FLC cell at the same film thickness (Fig. 7b). So, PDFLC saturation voltage is 30 - 35 times higher than for the corresponding monomeric FLC cell. This typical difference always exists for any type of polymers and FLC's, but PDFLC saturation voltage strongly depends on FLC type and its parameters (Fig.7a). The reorientation process is threshold free, the curve is linear up to the saturation region. Such a dependence is convenient for a gray scale in actively addressed displays.

The minimal V_{sat}=15V was reached due to the optimization of FLC compositions only (fig. 8).

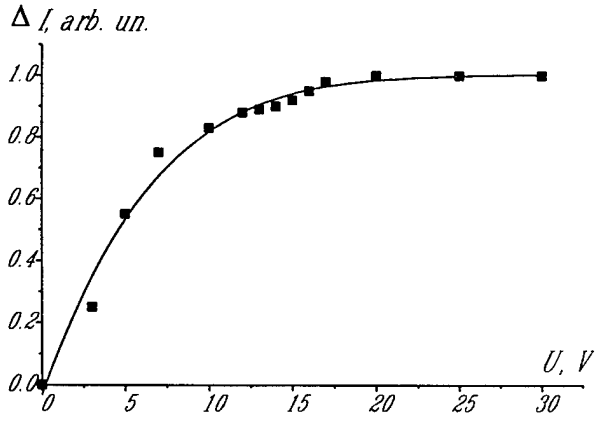


Figure 8. PDFLC volt - light transmittance characteristic for ZhKS-309C based PDFLC film of 5 mkm thickness, 4.5 mkm droplet size at the temperature of 22°C.

The charge mobility role

An approach is proposed to diminish the saturation voltage. It takes into account the mobility of polarization charges transferred in PDFLC droplets with the polarization reversal current caused by the FLC molecules reorientation under the external electric field.

When the interaction energy $P_S \cdot E$ of the electrical field and the spontaneous polarization is much more than the FLC elastic deformation energy in the droplets and much greater than the anchoring energy, the following relation is valid:

$$P_S \cdot E \cdot \sin \varphi = -\gamma_\varphi \cdot d\varphi/dt , \qquad (1)$$

where γ_φ is the rotational viscosity. The P_S projection onto the polar axis X (see fig. 9) is written:

$$P_{pol.} = P_S \cdot \cos \varphi , \qquad (2)$$

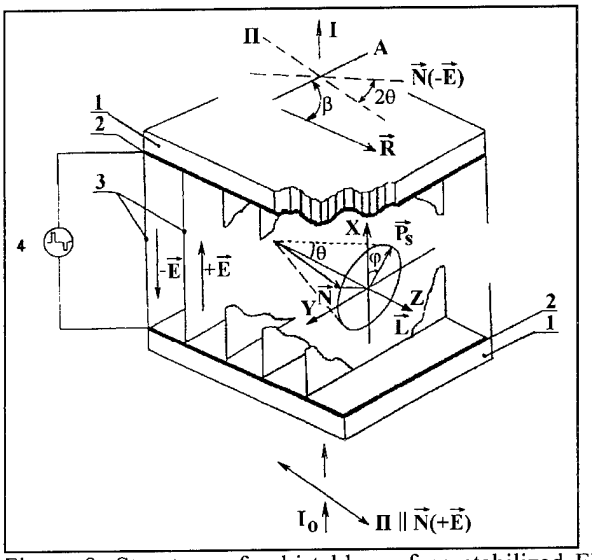


Figure 9. Structure of a bistable surface stabilized FLC cell with a "bookshelf" geometry of smectic layers.
1 - quartz or glass plates; 2 - transparent conductive electrodes with an orienting polymer layer; $\vec{R}$ - direction of polymer rubbing; 3 - smectic layers; 4 - voltage generator; θ - tilt angle, φ - azimuthal angle; Ï, A - polarizer and analyzer; β - angle between $\vec{R}$ and A; $\vec{N}$ - FLC director; $\vec{E}$ - electric field.

The polarization reversal current can be derived from relations (1) and (2):

$$j_R = dP_{pol}/dt = d(P \cdot \cos\varphi)/dt =$$
$$= P_S \cdot \sin\varphi \cdot d\varphi/dt = (P_S^2 \cdot \sin^2\varphi/\gamma_\varphi) \cdot E = \sigma_R \cdot E . \qquad (3)$$

where σ_R is the electroconductivity of the PDFLC film caused by the polarization reversal current expressed as:

$$\sigma_R = (P_S^2 \cdot \sin^2\varphi)/\gamma_\varphi . \qquad (4)$$

The amplitude value σ_R^a of the conductivity is:

$$\sigma_R^a = P_S^2/\gamma_\varphi . \qquad (5)$$

The electroconductivity and the charge mobility of the conductors and semiconductors are related as:

$$\sigma = e \cdot n \cdot \mu , \qquad (6)$$

where e·n product is the volume density of the transferred charges. However, the mobility of charges transferred due to the bias current distinguishes from the carriers' charge. The electroconductivity in PDFLC can be introduced as P_S/d_o, where d_o is a droplet diameter. That's why the value σ_R^a for PDFLC can be written like (6) as :

$$\sigma_R^a = P_S \cdot \mu_R / d_o , \qquad (7)$$

where μ_R is a charge mobility in droplets. From equations (5) and (7) it is obvious :

$$\mu_R = P_S \cdot d_o / \gamma_\varphi . \qquad (8)$$

Thus, the value μ_R is determined in the limits of our simplest consideration as the product of the droplet diameter d_o (this is a technological parameter of the PDFLC film), and the value P_S/γ_φ, which is a FLC material characteristic.

The ratio (8) can be also used to determine the charge mobility in monomeric FLC cell if the layer thickness d is substituted in to (8) instead of d_o. It is necessary to measure the droplet size (or the FLC layer thickness for monomeric cell) and P_S/γ_φ parameter of the liquid crystal in order to evaluate experimentally the charge mobility from (8). The geometry of a monomeric cell is the same as considered in Fig. 9.

The relation between the saturation field of the monomeric FLC cells and the mobility μ_R of the charges transferred with the bias current I_R from one electrode to another is considered at first. Fig. 10 shows that the charge mobility increases, and the saturation field decreases with the temperature increase.

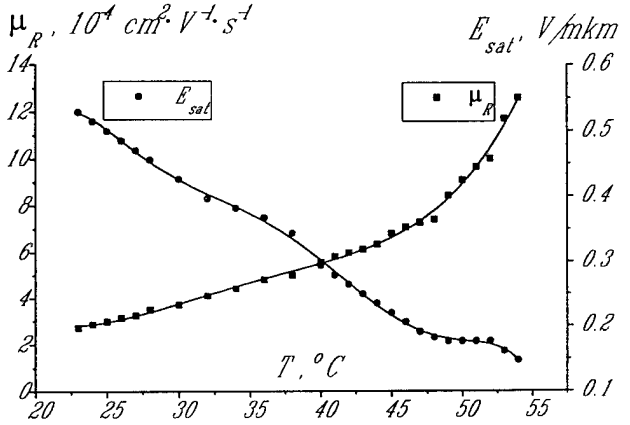


Figure 10. Temperature dependencies of the charge mobility μ_R and the saturation field E_{sat} of a monomeric FLC cell with FLC ZhKS-178 (layer thickness is 3.4 mkm).

The shape of the observed mobility versus temperature dependence is analogous to the semiconductor one. This similarity seem to be caused by the necessity of the motion over the potential barrier for the charge transfer both in the FLC cell and in the semiconductor. The charge mobility absolute values in FLC cells are approximately seven orders less than for the semiconductors (Fig. 10).

Fig. 11 shows the dependence $E_{sat}(\mu_R^{-1})$ which was plotted using the data of dependencies $\mu_R(T)$ and $E_{sat}(T)$ in fig.10.

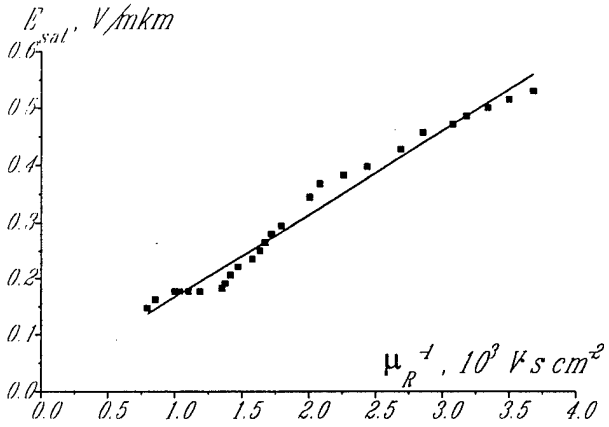


Figure 11. Dependence of the saturation field E_{sat} versus inverse charge mobility μ_R^{-1} which was obtained due to the temperature variation. Monomeric FLC is ZhKS-178, the layer thickness is 3.4 mkm.

It appears that the saturation field is inversely proportional to the charge mobility. Thus, it is possible to state an empirical relation between the saturation field and the charge mobility in FLC cell accounting the relation (8) and experimental dependencies in Fig. 11:

$$E_{sat}=k\cdot\mu_R^{-1}=k\cdot\gamma_\varphi/(P_S\cdot d_o)\,, \qquad (9)$$

where k is an experimentally determined proportion coefficient.

It is possible to conclude from (9) that the decreasing of γ_φ/P_S parameter and the increasing of the liquid crystal layer thickness d are necessary for the field saturation decrease in a monomeric FLC cell.

Let us consider dependence $E_{sat}(T)$ for monomeric FLC cell with a helix pitch p_o=0.5 mkm shown in fig. 12. One can see that the mobility increases and the saturation field decreases when the temperature increases for FLC of this type as for the helix free cells (see Fig. 11). But fig. 12 shows that the dependence $E_{sat}(\mu_R^{-1})$ is not a linear one.

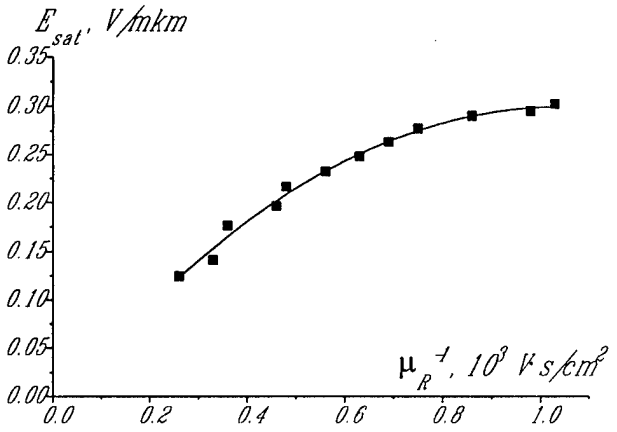


Figure 12. Dependence of the saturation field E_{sat} versus inverse charge mobility μ_R^{-1} for the monomeric FLC cell. The dependence was obtained due to the temperature variation. FLC ZhKS-309C, helix pitch p_o=0.5 mkm, the layer thickness is 6.4 mkm.

Thus, the relation (9) is not valid when k is constant. However, it was shown experimentally that the saturation field also increases with the mobility decrease and for the case considered. This dependence can be explained with the k dependence on some inhomogeneities of FLC director distribution because of its variations in a general case. For example, this inhomogeneity is a helix twist for the considered case. Within the framework of this hypothesis the equation (9) can be rewritten as:

$$E_{sat}=f(\mu_R)\cdot\mu_R^{-1}=f(\mu_R)\cdot\gamma_\varphi/(P_S\cdot d_o)\,, \qquad (10)$$

where $f(\mu_R)$ is a function dependent on the charge mobility, which, in its turn, depends on the FLC director distribution inhomogeneity. For PDFLC under this consideration it should be noted that the inhomogeneities of the director distribution in the droplets are always independent of their observation in the monomeric FLC.

The comparison of $E_{sat}(\mu_R^{-1})$ dependencies for PDFLC in fig. 13 and for the monomeric FLC in fig. 12 shows that they are similar. However, it is necessary to note that the saturation field for PDFLC based on FLC ZhKS-309C is approximately 20 times stronger than the same parameter for monomeric FLC cells. Another difference is a weak temperature dependence of E_{sat} for PDFLC. Fig. 13 shows that the saturation field reaches its maximal value, and becomes independent of the mobility when the charge mobility in the PDFLC is less than a certain critical value.

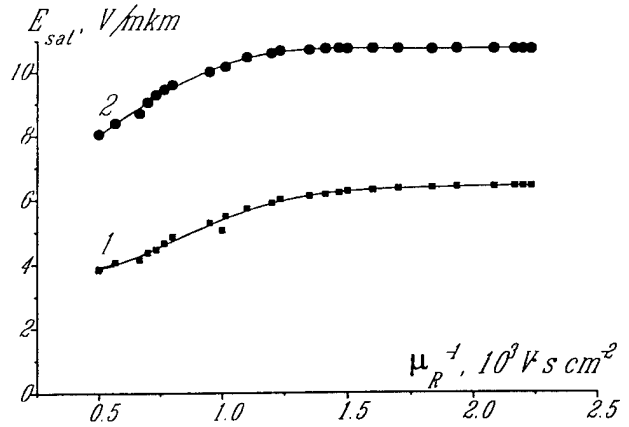


Figure 13. Dependencies of the saturation field E_{sat} versus inverse charge mobility μ_R^{-1} for PDFLCs based on FLC ZhKS-309C (curve 1) and FLC: ZhKS-340 (curve 2). PDFLC layer thickness is 9 mkm, the droplet size is 3 mkm. The dependence was obtained due to the temperature variation.

The μ_R^{-1} value depends on the liquid crystal type in the droplets for the same polymer (polyvinilbutyral) (fig. 13, curve 1 and 2). The μ_R^{-1} values region, where E_{sat} can be changed, is limited for PDFLC in contrast to the monomeric FLC. Nevertheless the charge mobility increase causes the saturation field decrease as for the monomeric FLC cells.

Fig. 14 shows $E_{sat}(\mu_R^{-1})$ dependencies for PDFLCs based on the polyvinilbutyral and the FLCs with different γ_φ/P_S values. The droplet sizes d_o are also different. It is

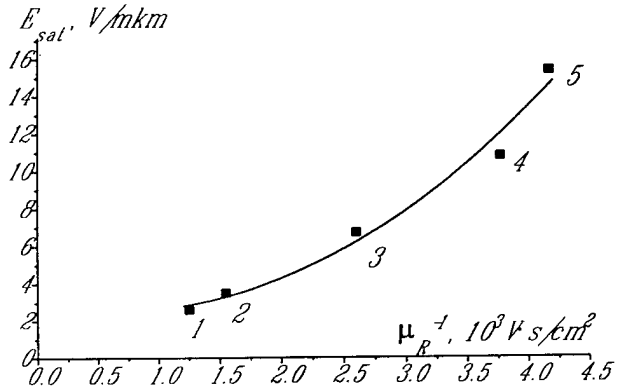


Figure 14. Dependence of the saturation field E_{sat} versus inverse charge mobility μ_R^{-1} for PDFLCs which was obtained due to variation of both the γ_ϕ/P_S and the droplet size d_o. Experimental points correspond to: 1 - FLC ZhKS-313B, the droplet size d_o=3 mkm, 2 - FLC ZhKS-309C, d_o=5 mkm, 3 - FLC ZhKS-309C, d_o=3 mkm, 4 - FLC ZhKS-340, d_o=3 mkm, 5 - FLC ZhKS-178, d_o=2.5 mkm.

evident (see the relation (10)) that the charge mobility is the function of γ_φ/P_S and d_o. This leads to the saturation field changing in the considered PDFLCs from 3 V/mkm to 15 V/mkm.

It should be noted that almost the same value is achieved for the polymer dispersed nematic liquid crystals also [10]. The best results among the published ones for the saturation field in PDFLC are 8 V/mkm [5] and 6 V/mkm [6]. Thus, we succeeded these values more than twice, increasing the charge mobility in PDFLC due to μ_R^{-1} parameter diminution (see Fig.14).

Droplet structure role

The further diminution of the saturation field can be achieved, probably, due to the polymer selection. However, the smectic layers structure and the boundary conditions in PDFLC droplet have to be taken into account.

Keeping in mind (10) one can write:

$$U_{sat} \sim \gamma_\varphi \cdot L/(P_S \cdot d_o), \qquad (11)$$

where L is a thickness of the PDFLC film. Then, to diminish the PDFLC saturation voltage it is necessary to diminish the ratio γ_φ/P_S for the liquid crystal, and the ratio of the film thickness L to the droplet size d_o. It is evident that the minimal L/d_o value is:

$$(L/d_o)_{min}=1, \qquad (12)$$

because in this case the film thickness is equal to the droplet size. The PDFLC film becomes birefringent when (12) is valid, because the multiple light reflection on droplet-polymer boundaries becomes impossible. That's why PDFLC film with the lowest saturation voltage, when the relation (12) is valid, can be exploited only in two polarizers design. PDFLC important properties such as high light transmission and the ability to work without polarizers are lost for this design as compared to a conventional birefringent display.

Actually it is necessary to satisfy the relation:

$$L/d_o \geq 3, \qquad (13)$$

for the one polarizer or polarizers free design.

The best light transmission is for the last two designs, but the higher driving voltage is necessary in principle in comparison with the two polarizers design.

The samples based on ZhKS-309C with droplet size d_o=4.5 mkm and the film thickness L=5 mkm were developed as the lowest voltage PDFLC. This is a double refractive film which is placed between two crossed polarizers. The PDFLC film saturation voltage is 15 V (see fig. 8) at the driving voltage frequency of 2000 Hz.

The lowest saturation voltage for PDFLC light shutters without polarizers is 57 V (Fig. 15).

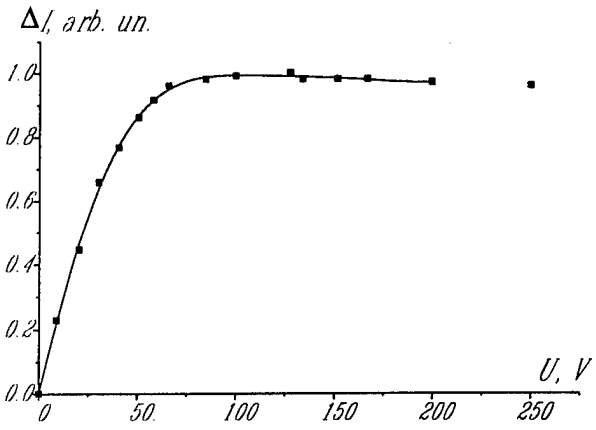


Figure 15. PDFLC volt - light transmittance characteristic for the ZhKS-309C based film of 9 mkm thickness with droplet size of 3 mkm at the temperature of 22°C.

The thickness of the film in use is 9 mkm and the droplet size is 3 mkm. Thus, the relation (13) is valid, and makes possible to get the contrast ratio more than 10 : 1 due to the multiple light refraction on the droplet boundaries for the polarizers free design.

Thus, the contrast ratio depends mainly on the film preparation technology for both modes (transparency and scattering) of modulators. The modulator light transmittance does not depend on the temperature practically within the whole C* phase interval, except of a narrow region near the transition into the high temperature phase [11].

Both types of PDFLC light modulators described above can operate under the alternating pulses of 2 kHz frequency when the driving voltage is equal to the saturation one.

Conclusion

PDFLC composition, textures and modulators design are considered.

The influence of the molecular structure and FLC features on to PDFLC saturation field is investigated.

The main role of the mobility of charges transferred in PDFLC droplets with the polarization reversal current caused by FLC molecules reorientation under the external electric field is pointed out. PDFLC films modulators with the driving voltage of 15 V were developed.

The method of further saturation voltage decreasing due to FLC γ_φ/P_S parameter is proposed.

One can expect further improvement of the PDFLC parameters during optimization of FLC and polymer composition as well as their weight ratio.

Acknowledgments

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THE FAST BIT PLANE SLM: A NEW FERRO-ELECTRIC LIQUID CRYSTAL ON SILICON SPATIAL LIGHT MODULATOR DESIGNED FOR HIGH YIELD AND LOW COST MANUFACTURABILITY

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ABSTRACT

We announce a new VLSI silicon backplane Spatial Light Modulator known as the DRA Fast Bit Plane SLM. The size of the pixel array is 320x240 with a fill factor of 65%; the pixel type is single transistor DRAM. With DRA2 liquid crystal [2] the maximum possible frame rate is 22.7kHz. Initial devices have been set up for binary phase modulation using a crystal with a cone angle wider than is optimal for intensity modulation. Even so a contrast ratio of 12:1, averaged over a small array of pixels, has been measured and results from imaging applications are presented. An image has been projected from the un-planarised device and displayed images are plainly visible under ambient illumination; full colour images are possible in a helmet-mounted configuration. In its planarised form the device is considered to be a low cost alternative to the TI DMD for many applications.

Key Words: Optical Devices - Theory and Technology - Spatial light modulators, liquid crystal devices, silicon backplane devices.

GENERAL DESCRIPTION

The Fast Bit Plane SLM is a VLSI silicon backplane EASLM of a generic type first reported by Collings et al [3]. The pixels are of the single transistor DRAM type laid out in a 320x240 array. The data bus is 64 bits wide with 5:1 de-multiplexing whilst the rows are controlled by a token and shift register scheme rather than by line address decoding. The pixel pitch is 34 microns and the overall die size is 14x14mm. The device has been manufactured by a commercial VLSI process from Austria Mikro Systeme International (AMS). This device is similar in some aspects to the devices reported by Handschy et al [4].

DESIGN CRITERIA

The principle design criteria were threefold:

- High yield and ease of manufacture.
- High fill factor and mirror flatness.
- Maximum possible addressing speed.

The second criterion arose from the requirement that the device should be usable even if un-planarised. This lead almost directly to the use of a DRAM rather than SRAM type pixel but also meant that there could be no circuitry underneath the pixel mirror.

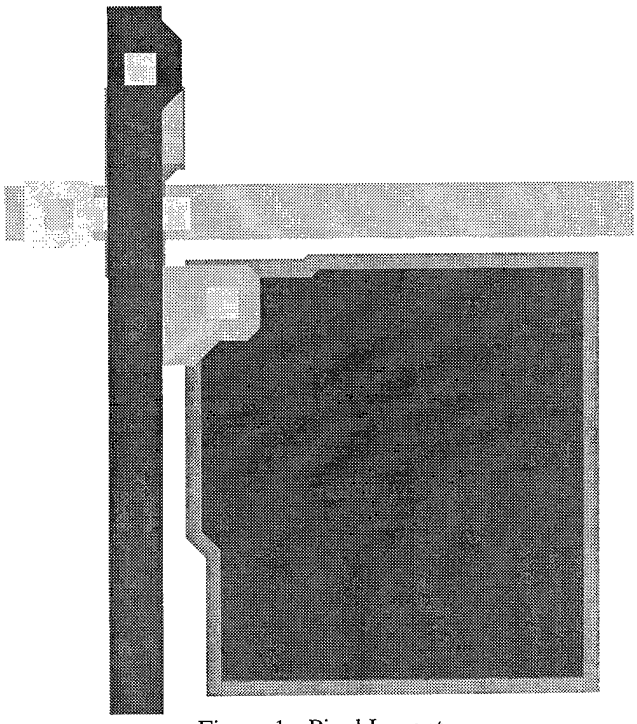

Figure 1 - Pixel Layout

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At an early point in the design sequence it was also decided that a high voltage 2 micron VLSI process would be used in order to switch the Liquid Crystal as quickly as possible. As a consequence of these two factors the best fill factor that could be achieved was 65% - note the Handschy devices achieve a much higher fill factor but this is done by placing the mirror over underlying circuitry. The pixel layout is shown in Fig 1.

Given that a 2 micron process was used, this would perhaps limit the speed of the device somewhat. Even so the device is rated at 50MHz, with a 100ns line address time. Coupled with the DRA2 liquid crystal mixture the maximum possible frame rate is 22.7kHz, although this is dependent on the liquid crystal drive scheme.

Assembly and Yield. Previous problems encountered in the high yield fabrication of these devices, particularly that of 'front to back' shorts, have been tackled and new, yield enhancing methods for device assembly and glue lane deposition have been employed.

Liquid Crystal Drive Schemes. In addition to the criteria mentioned above, the device has also been designed with a novel Liquid Crystal drive scheme in mind. In the past SLMs of this type (ie DRAM) have been driven by holding the potential of the front electrode at a point half way between ground and the maximum potential that the pixel can reach, in this way opposite polarity fields can be applied to the appropriate pixels. In order to maintain DC balance the data is either periodically reversed [4] or an inverse frame is written to the SLM for every image frame and the illumination is modulated appropriately [5]. The scheme the device was designed for is inherently DC balanced and in practice this has meant that extra functionality has been included in the electrical addressing scheme of the SLM. The significance of this scheme is that the SLM is now continuously viewable, unlike the previous 2 schemes. Previously only SRAM type SLMs have had this feature and they have relied on a much more complex pixel circuit and addressing scheme, often accompanied with a reduction in light throughput [6].

TEST FEATURES

In order to accurately assess devices and to monitor them in actual operation a number of test features have been included in the design.

At the end of each row and column line there are 2 MOSFETs (an n channel and a p channel). These are connected together such that, in combination with an external pull-up or pull-down resistor, they form both a wired NOR and a wired NAND gate monitoring the row and column lines. Using this feature, the switching of both row and column lines can be verified.

The most useful test feature is the pixel followers that have been connected to one pixel from each of the 2 bottom rows of the array. Using the outputs from these, the switching of the 2 pixels can be directly observed; this enables such experiments as observing the dipole switching current of the FELC and the effects of high intensity

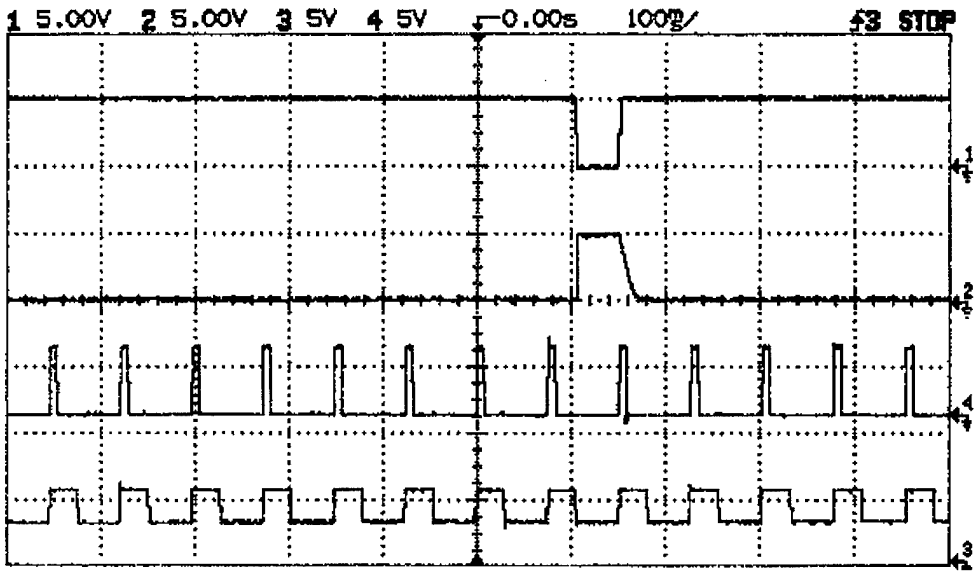

Figure 2 - Test outputs.

illumination on pixels (before, during and after they switch) to be carried out.

Other features include the token buffers at the bottom of each shift register which verify that the complete shift register is operating and a temperature sensor that, in addition to a peltier heater, could be used to accurately control the temperature of the device. A sample of the outputs from these test feature is shown in Figure 2; in this figure the top trace is the output from a token buffer, the next the pixel follower (incidentally this indicates a pixel droop under lab light illumination of around 10ms), trace 4 is one of the clocks and trace 3 is the output from the wired NOR gate connected to one set of row lines, indicating the switching of the rows.

ASSEMBLY AND YIELD RESULTS

Unsurprisingly there are many steps in the total assembly procedure but the 2 principal ones are the coming together of the silicon and glass and wire bonding and packaging. The former process has been carried out in the Class 100 clean room facility at Cambridge University Engineering Department (Photonics and Sensors Group) using a semi-automated system that enables 4 devices to be assembled at once. The packaging and wire bonding has been carried out at DRA Malvern.

Table 1 shows the overall yield and its constituent values. Note that, normally, dice would be probed once, whilst they were on the wafer, and for a second time after the front glass was glued in place. For simplicity and to increase overall yield (as the second probing will itself lead to some devices failing) the first probing is omitted. Consequently the figure for manufacture and assembly includes both the yield on the wafer and the yield of the assembly process. A separate wafer was probe tested initially, the yield on this was 88.5% although this is a little misleading as, of a necessity, this test is unable to reveal all faults that may exist on a device.

Table 1 - Manufacturing Yield

Process	Yield
Manufacture and Assembly	44%
Front to Back Shorts	100%
Bonding and Packaging	71%
Overall	31%

LIQUID CRYSTALS

The devices assembled so far have been filled with a high tilt angle material known as MPP3 [2]. In this case it has been aligned by a conventional rubbed nylon layer; both the cover glass and the silicon have been rubbed - unlike the Handschy devices [2] - although the silicon was rubbed more gently! Previously it was thought that rubbing the silicon in this way would damage the circuitry, mainly the pixel transistor gates. However this does not seem to be the case and the devices prepared in this way align extremely well.

In theory the liquid crystal can align into 1 of 2 domains, the difference being the inclination of the smectic layers to the rubbing direction. In practice only single domain structures have been observed both in these devices and simple glass test cells.

APPLICATIONS RESULTS

With MPP3 the maximum observed contrast ratio, averaged over 100 or so pixels, is 12:1; the switching speed is of the order of 100us. However one must remember that MPP3 has a high tilt angle (60 degrees) which is greater than that required for maximum contrast in a display application; the high tilt angle also explains to a certain extent the relatively slow switching speed of this material.

A full interface/framestore is nearing completion but was not available to drive the chip for the system described below, consequently the images shown are very simple. The full interface has the capability to drive the chip at its rated speed of 50MHz - a burst data rate of 3.2 Gbit/s - and can store sufficient image data for at least a 4 second full motion video clip [7].

Figure 3 shows an image written to the SLM and viewed under *ambient* illumination through a single polariser. Figure 4 shows the same image written to the SLM but projected onto a normal slide projector screen. The projected image is plainly visible in this way (albeit in a dimly lit room) although the actual image size is limited to about 40x30 cm (representing an image magnification of about 35 times). A very simple off axis reflection scheme - see Figure 5 - was used to project this image. The optical power incident onto the SLM for this experiment was around 10mW/cm^2. This is comparable to the figure quoted by Handschy for their Generation I devices. The Generation II devices would appear to be highly resistant to incident radiation, however one would expect this given their design (specifically that mirrors are placed over circuitry which acts to protect the circuitry from incident radiation as well as to increase fill factor). A detailed model of how the Fast Bit Plane SLM responds to the incident optical power will be the subject of a later paper.

Given that the device is currently unplanarised the performance of the projection display is very good.

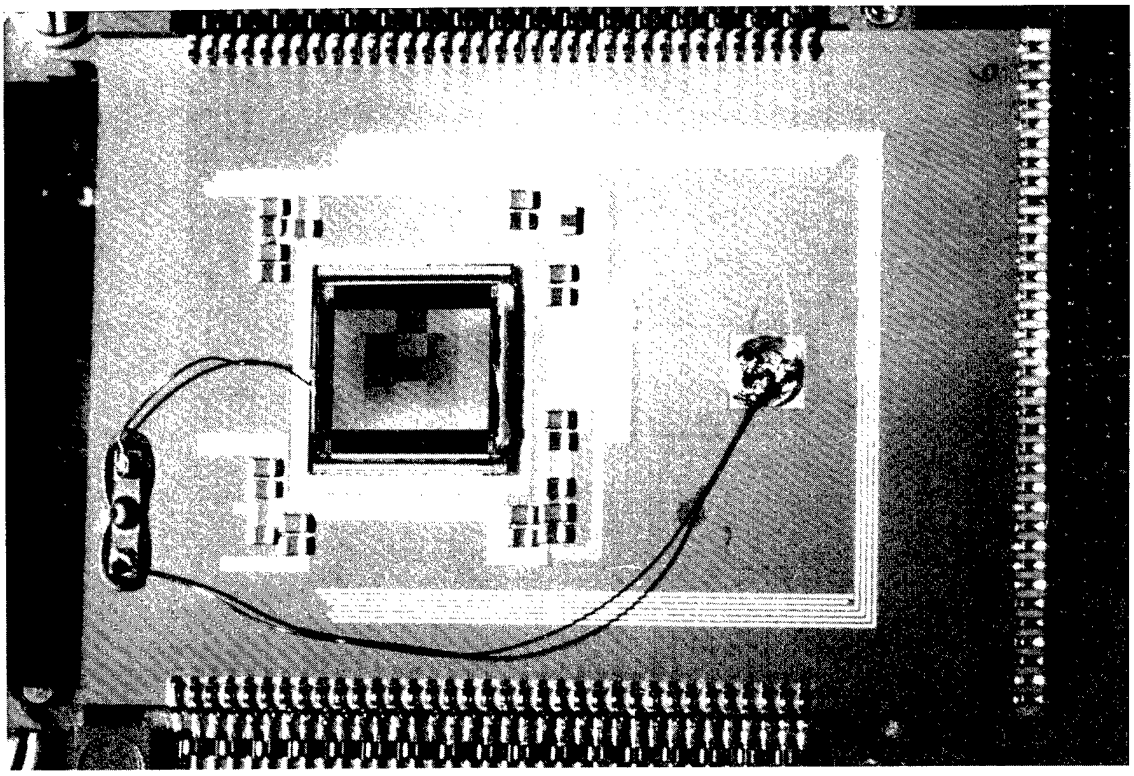

Figure 3 - Image viewed under ambient illumination through a single polariser.

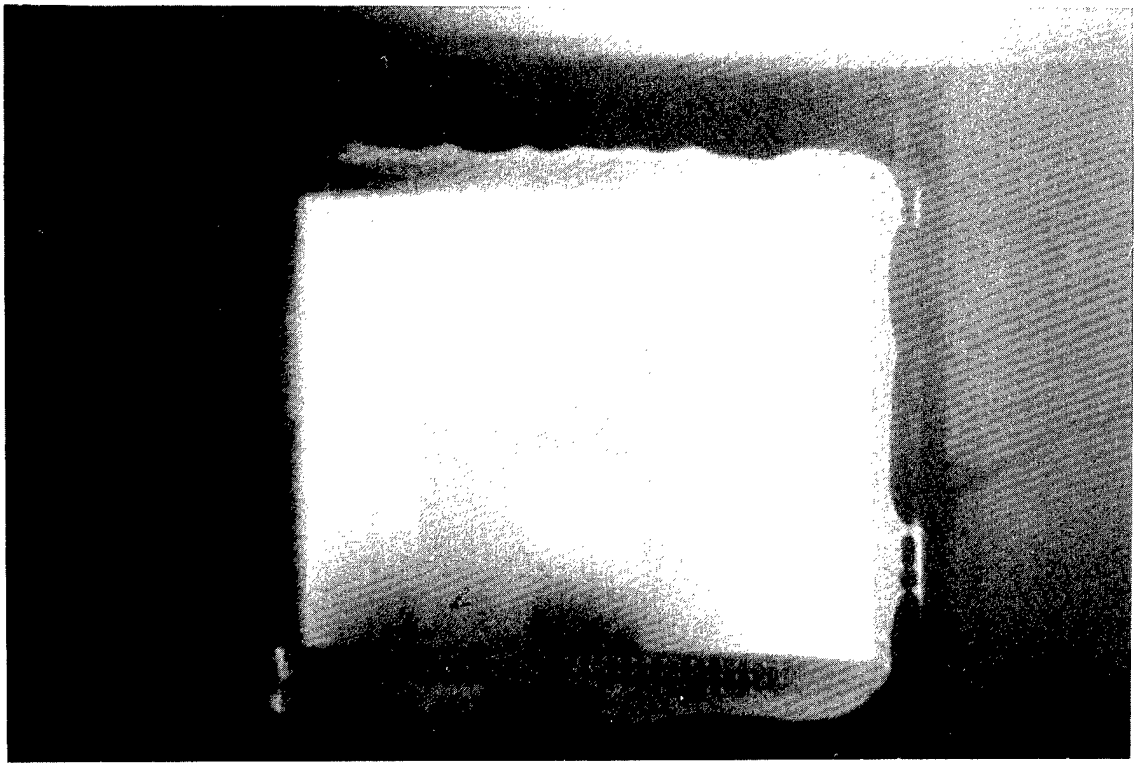

Figure 4 - Projected image.

Furthermore the planarised device is expected to be as resistant to high intensity illumination as the Generation II Handschy devices. With this in mind this device must be considered as a viable alternative to the Texas Instruments DMD, but at a fraction of what is assumed to be the cost of these devices.

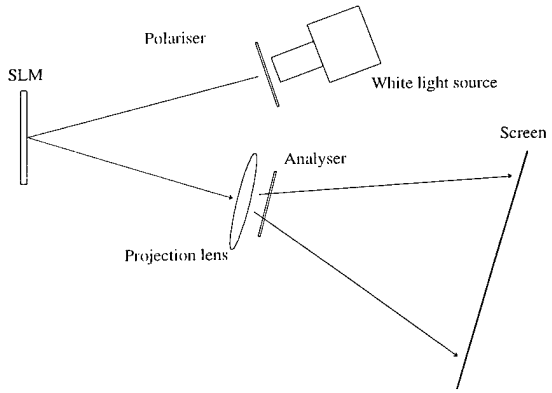

Figure 5 - Off axis projection system

A simple variant of the projection display is the helmet-mounted type, replacing the high intensity white light with simple LEDs and viewing the image through a beam splitter. This configuration also lends itself to a full colour imaging system [8].

The images shown here are simple black and white ones, however grey scale is easily achievable, even under fairly intense illumination, by using a temporal averaging or bit plane scheme. This has been demonstrated with simple images in the laboratory, both in projection and viewed directly.

CONCLUSION

The DRA Fast Bit Plane SLM is a silicon VLSI backplane electrically addressed SLM. It has been designed for speed, flexibility, high yield and ease of manufacture. Initial work has shown that devices can be made in quantity, although the overall yield is moderate at the moment. The first devices have been set up for binary phase modulation but even so good intensity contrast has been achieved. With a simple interface and optics a projection display has been constructed, whilst images, both grey scale and black and white, are directly viewable under ambient illumination. The resistance of the device to high intensity illumination in its unplanarised state is very good and consequently it is considered that the *planarised* device will be a viable, but much lower cost, alternative to the Texas Instruments DMD device.

Further work will include trials of the device as a phase hologram source, and the extension of the imaging application to full colour full motion video.

ACKNOWLEDGEMENTS

This SLM was developed for DERA Malvern under contract MAL 1b/2256. Our thanks are due to Drs Meirion Lewis and Brian Lowans of DERA Malvern, Mick Stone of the Engineering Department, Dr Martin Birch of CRL and Dr Ian Underwood of Edinburgh University. TM Coker is an EPSRC student and also has a CASE award from DERA Malvern.

NOTES AND REFERENCES

1. TCBY Yu designed and laid out the device whilst at Cambridge under a Croucher Foundation Research Fellowship.

2. The DRA2 mixture was supplied by DRA Malvern and the MPP3 material by the University of Hull under the LINK DTI programme 'Fast Optical and Electro-Optical Effects in Chiral Liquid Crystals'.

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Field-Dependent Birefringence of an Electroclinic Organosiloxane Liquid Crystal

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Abstract

The field-dependent birefringence is measured for an electroclinic organosiloxane liquid crystal, designated as DSiKN65. The measured field-induced change in the birefringence is large and can produce a modulation of the transmission comparable to that produced by the electroclinic effect. The induced change is attributed to a field induced optical biaxiality and is shown to be strongly correlated to the tilt angle. Optical biaxiality is shown to augment the electroclinic effect and enhance the achievable contrast ratio.

Key Words: Liquid crystals, Liquid crystal devices, Spatial light modulators.

Introduction

The growing desire for spatial light modulators with grey-scale capability and a fast response has stimulated interest in the development of new electroclinic liquid crystals with large tilt angles. The achievable contrast ratio in these devices is limited by the magnitude of the tilt angle as well as by a field-induced deformation of the smectic layers which degrades the extinction. Recently, it was shown that field-induced changes in the birefringence can also contribute significantly to the electro-optic response [1]. In this paper, optical phase retardation measurements are performed to investigate the field dependence of the birefringence and the contrast ratio for a new electroclinic liquid crystal, designated a DSiKN65, which has recently been synthesized and which exhibits both a large electroclinic tilt angle (>22.5^0) and a fast response (<100μs) [2]. The first observation of a large field-dependent optical biaxiality in this material is reported. The implications on these results on device performance will be discussed.

Experimental

Sample Preparation and Characterization

The molecular structure of DSiKN65 is shown in Fig. 1; its synthesis is reported elsewhere [2]. The phase transition sequence of DSiKN65 is: SmC*--40.5C--SmA*--55C--I. This material was loaded in temperature-controlled commercial glass cells whose interior surfaces were coated with ITO electrodes and with a rubbed polyimide alignment layer. The cell thickness was measured interferometrically prior to filling. The sample was aligned using a bipolar electric field (5V/μm) applied as the sample was slowly cooled from the

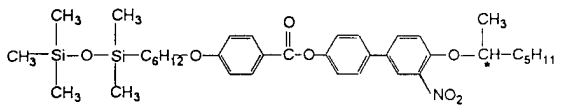

Figure 1. Molecular structure of DSiKN65.

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isotropic to the Sm A* phase. Spectra of DSiKN65 show that it is transparent in the visible and near-IR spectral regions.

Dispersion of the Birefringence

The birefringence and its dispersion were determined by measuring the transmission of the sample as a function of wavelength using a Perkin Elmer spectrometer which was modified to position the sample between polarizers. This technique allows one to determine uniquely the birefringence of the liquid crystal and its dispersion. The results are presented in Fig. 2. The curve through the data is a best fit calculated using the following expression for the transmitted intensity [3]

$$I = I_0[\cos^2(\chi)-\sin(2\phi)\sin(2\phi-2\chi)\sin^2(\delta/2)] \quad (1)$$

where I_0 is the incident intensity, χ is the angle between the polarizer and analyzer, ϕ is the angle of the long molecular axis relative to the orientation of the polarizer, δ is the phase angle introduced by

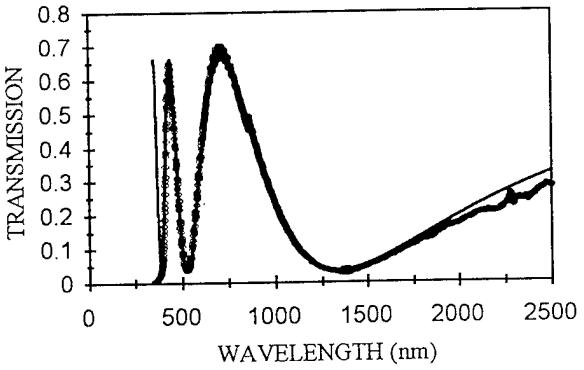

Figure 2. Transmission of 10.4 μm thick DSiKN65 sample interposed between parallel polarizers as a function of wavelength. The sample temperature is maintained at 42°C in the SmA phase.

the sample birefringence, Δn. ($\delta=2\pi\Delta n\, d/\lambda$, where d is the sample thickness and λ is the wavelength of light.) Δn is assumed to be of the form [4]

$$\Delta n = G(T)\frac{\lambda^2\lambda_0^2}{\lambda^2-\lambda_0^2} \quad (2)$$

where λ_0 is the mean resonance wavelength of the liquid crystal and G is a temperature-dependent parameter which depends on the anisotropy in the oscillator strength, the order parameter of the liquid crystal, and the density of active electrons. The dispersion of the birefringence is determined from computer simulations using G and λ_0 as fitting parameters. The results, presented in Fig. 3, reveal that the birefringence depends significantly on the wavelength in the visible spectral region. The best fit was obtained for $G(T) = 1.327\ \mu m^{-2}$ and $\lambda_0 = 0.2175\ \mu m$.

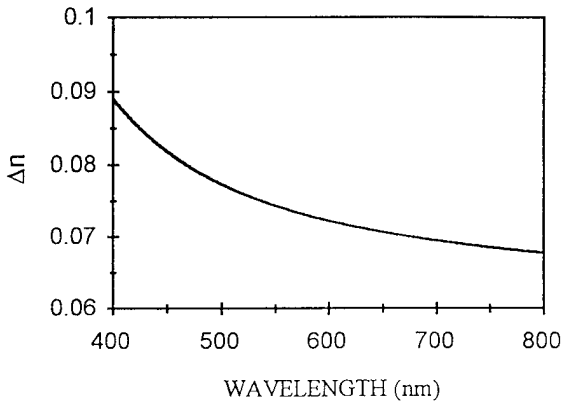

Figure 3. Dispersion of the birefringence of DSiKN65 at 42°C determined by fitting the data in Fig. 2.

Electro-optic Properties of DSiKN65

The electro-optic properties were determined by measuring the sample transmission placed between polarizers using a fixed wavelength. Measurements were performed using a chopped CW HeNe laser operating at 594 nm. This wavelength was chosen to provide a large change in transmission with field (see Fig. 2) subject to laser availability constraints. The laser output was mechanically chopped at 12.5 Hz with a 5% duty cycle and field dependent measurements were made by synchronizing bipolar square electrical pulses with the optical pulses. The optical pulses sampled the same polarity throughout these studies. In these studies, the polarization of the laser was rotated while the sample remained stationary. This was accomplished by mounting a Babinet-Soleil compensator, adjusted for half-wave retardation at the laser wavelength, in a computer controlled

rotation stage. The analyzer was also mounted in an automated rotation stage which could be rotated in tandem while maintaining either a parallel or crossed polarization configuration. With the sample removed, the extinction ratio was approximately 10^{-4} through a 360^0 rotation.

Results and Discussion

The measured crossed-polarized transmission as a function of polarization angle for several values of the applied field is presented in Fig. 4 for a 10.4 μm thick DSiKN65 sample maintained at 45°C. The field dependence of the electroclinic tilt angle, the birefringence and its field-induced change, and the contrast ratio are determined from the data in Fig. 4.

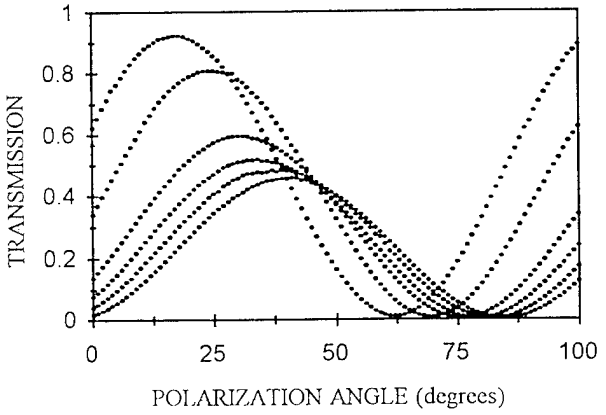

Figure 4. Crossed-polarized transmission as a function of polarization angle for a 10.4 μm thick DSiKN65 sample subjected to electric fields of 0V/μm (lowest data set), 1.0V/μm, 1.9V/μm, 2.9V/μm, 4.8V/μm, and 7.3V/μm (highest data set). The sample temperature was 45°C and the laser wavelength was 594 nm.

Electroclinic Tilt Angle

In Fig. 4, the angular shift in the position of the maxima and minima with applied field is due to the electroclinic tilt angle. The electroclinic tilt angle determined from Fig. 4 is plotted in Fig. 5. It increases monotonically with field (approximately linearly up to 7.3V/μm) in agreement with the published results of Naciri, et al [2]. At 9.7V/μm, the tilt angle exceeds 22.5 degrees, the angle necessary for maximum contrast ratio.

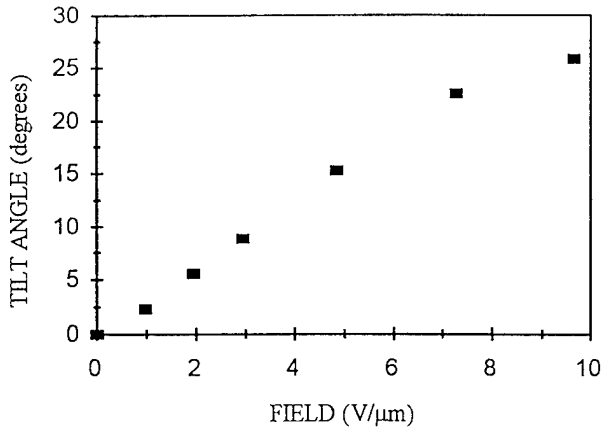

Figure 5. Field dependence of the electroclinic tilt angle.

Field-induced Change in the Birefringence

The field dependence of the birefringence is determined from simultaneously fitting the crossed-polarized data (Fig. 4) and the corresponding parallel-polarized data (not shown) using Eqn. (1). The change in the amplitude of the transmission maxima with field in Fig. 4 is a manifestation of a field-dependent birefringence. The measured birefringence at 594 nm with no applied field is 0.071 and its change with field, $\delta\Delta n$, is plotted in Fig. 6. Experimentally, $\delta\Delta n$ was found to vary quadratically with the applied field, in agreement with theoretical predictions for field-induced biaxiality. The curve through the data illustrates this quadratic field dependence. The field-induced increase in Δn is quite large for DSiKN65 (~30%)

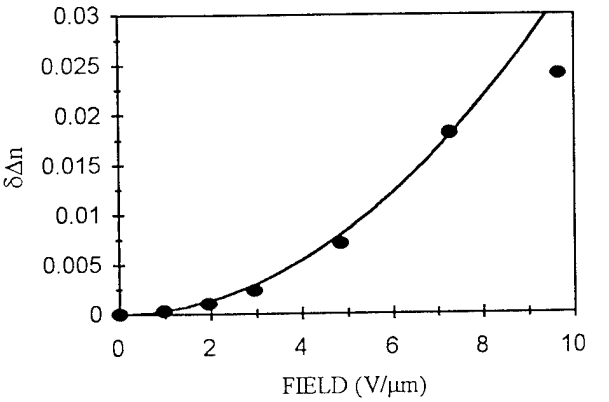

Figure 6. The field dependence of the change in the birefringence, $\delta\Delta n$, determined by fitting the curves in Fig. 4 using Eqn. (1). The line through the data is a quadratic fit.

when compared to KN125 (<5%) [1] and produces a phase retardation greater than quarter wave.

The change in the birefringence is attributed to a field-induced optical biaxiality. Although the molecules are biaxial, the random orientation produced by the free rotation about the long axis of the molecule makes these materials macroscopically uniaxial. When a field is applied, the free rotation is hindered due to the preferential alignment of the transverse dipole moment with the field, producing an increase in the birefringence and making the sample optically biaxial. Fig. 7 illustrates that the induced biaxiality is strongly correlated and varies quadratically with the electroclinic tilt angle. A similar coupling of the optical biaxiality and electroclinic effect has been previously observed in KN125 [1]. This coupling has significant implications for device applications.

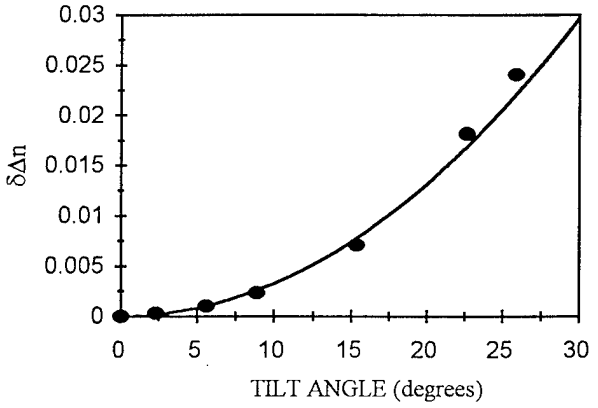

Figure 7. Dependence of optical biaxiality on the electroclinic tilt angle.

Contrast Ratio

The contrast ratio, defined as the ratio of the transmission with an applied field to that with no applied field, can be calculated using the data in Fig. 4. Although not fully optimized, a contrast ratio greater than 100 was observed for DSiKN65. Fig. 4. illustrates that the modulation of the transmission due to the induced optical biaxiality may be comparable to that produced by the electroclinic effect. Thus, both induced biaxiality and electroclinic tilt can be exploited to optimize the contrast in devices fabricated from this material. This may be particularly important in device design since low voltage operation is usually preferred.

Conclusion

In conclusion, the electroclinic tilt angle, birefringence, and contrast ratio of a new electroclinic liquid crystal, DSiKN65, have been measured. This material possesses a large electroclinic tilt angle (>25^0 at 10 V/μm) and exhibits a large induced optical biaxiality associated with the hindrance of the free rotation about the long molecular axis. The induced biaxiality is strongly correlated with the tilt angle indicating that a common mechanism is responsible for both. It augments the electroclinic effect and can be exploited to optimize the contrast in devices fabricated from this material. Contrast ratios greater than 100 have been measured.

Acknowledgments

The authors wish to thank the Office of Naval Research for support of this research and J. Naciri for synthesizing the liquid crystals studied here.

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Investigation of novel structures on silicon backplane SLMs to improve the device performance

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Abstract

Post-processing of commercially fabricated silicon backplanes for use in liquid crystal over silicon backplane spatial light modulators has improved their optical performance. This procedure entails the microfabrication of an additional metal layer which is optically optimised. Changes and additions to the post-processing procedure to enhance the pixel structure have been investigated to improve the silicon backplane for use as a spatial light modulator.

Spatial light modulators, Silicon processing, Chemical mechanical polishing, Damascene processing.

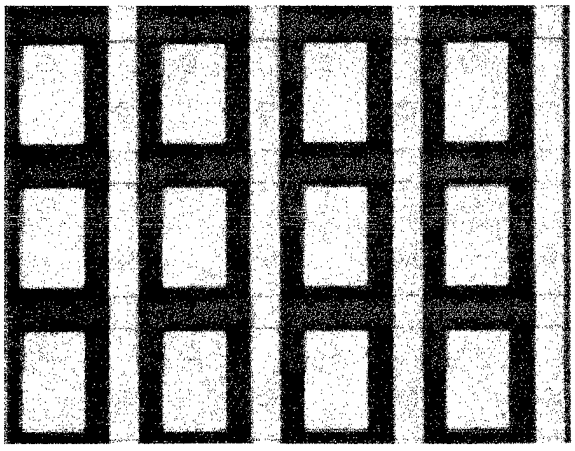
Introduction

Post-processing of commercial silicon backplanes have resulted in improved optical performance of liquid crystal (LC) over silicon spatial light modulators (SLMs). The use of chemical mechanical polishing (CMP) to planarise the wafers eliminates the topographical effect of the underlying circuitry and allows the production of high optical quality pixel mirrors with large fill factors [1]. Having control of the top layer metal process permits the optical optimization of the SLM backplane and allows the investigation of other interconnect structures to enhance the device. We are currently examining adaptions and additions to our post-processing procedure which will change the structure of the pixel and the die to further enhance the performance of the silicon backplane. The addition of an extra metal layer to protect DRAM devices from photo-induced charge leakage is demonstrated. The extension of the process to include an additional patterned dielectric layer to act as a spacer layer is investigated. Also, a new processing technique, Damascene processing is introduced to fabricate the metal electrode/mirrors which results in a new pixel structure with the potential to improve the LC alignment and the pixel mirror fill factor.

DRAM protection from light induced charge leakage

With single transistor DRAM SLMs light incident onto the silicon substrate causes charge leakage from the pixel capacitor to the substrate, this in turn reduces the voltage on the modulating electrode which results in the LC switching from its intended state [2]. This problem is compounded by the desire to use these devices with large light intensities which increases the rate of charge leakage.

Post-processing of SLM backplanes has increased the pixel mirror fill factor which reduces the amount of light reaching the substrate [3], reducing the effect of the photo-induced charge leakage. We have now developed this process further reducing the gap between the mirrors and therefore reducing still further the light reaching the substrate.



(a)

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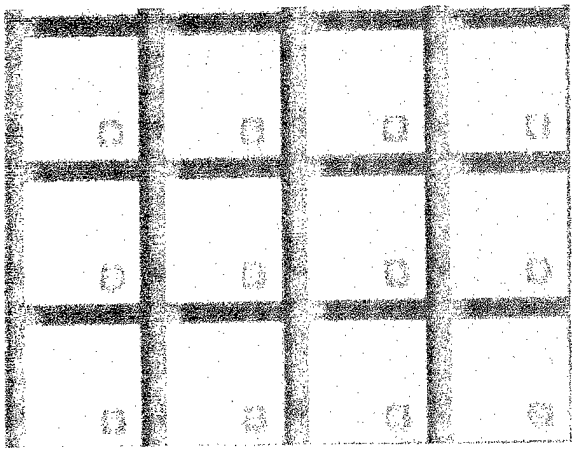

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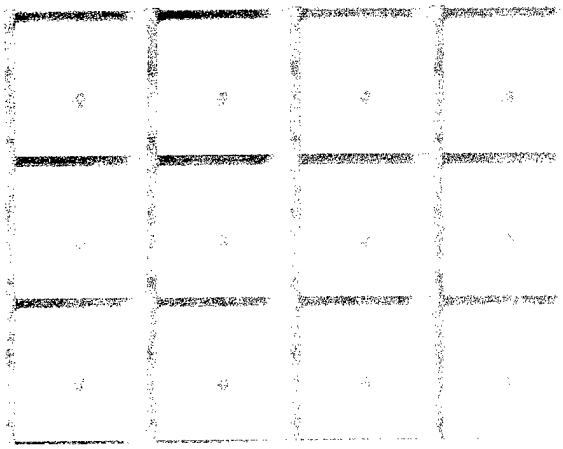


(c)

Figure 1. Improvement in the post-processing procedure leading to higher fill factor pixel mirrors.

Light can still reach the substrate through the gaps between the mirror/electrodes. Current silicon backplanes now employ silicon processing using multi-level metallization. Two and three levels of metal are now quite common. These numerous metal layers can be utilised to block light reaching the underlying silicon substrate. This technique was used in the design of our 512 DRAM SLM device [4]. The data and enable lines are arranged in a grid with the mirror positioned with the gaps between the mirrors coinciding with the underlying interconnect. figure 2. There is still the possibility of light which goes between the pixel mirrors scattering from the underlying interconnect and reaching the silicon substrate.

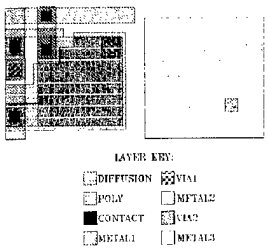


Figure 2. Schematic of the 512 DRAM SLM pixel layout.

Therefore, we have also developed the post-processing procedure to apply two metal layers with the intermediate layer acting as a blocking layer. These metal layers are designed to produce a large overlap to reduce the light transmission to a minimum, figure 3. This technique was applied to our 176 DRAM SLM, figure 4.

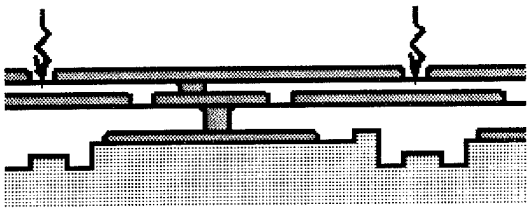
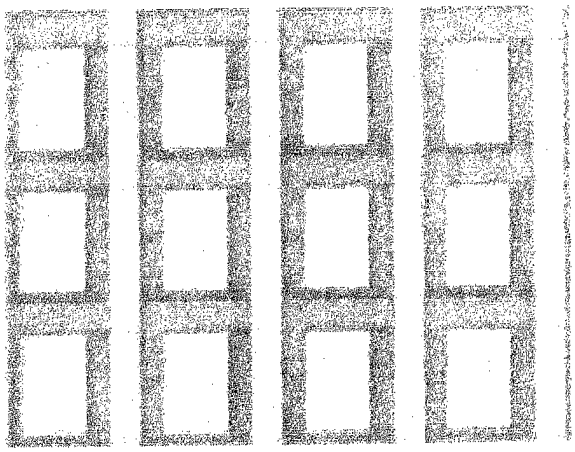
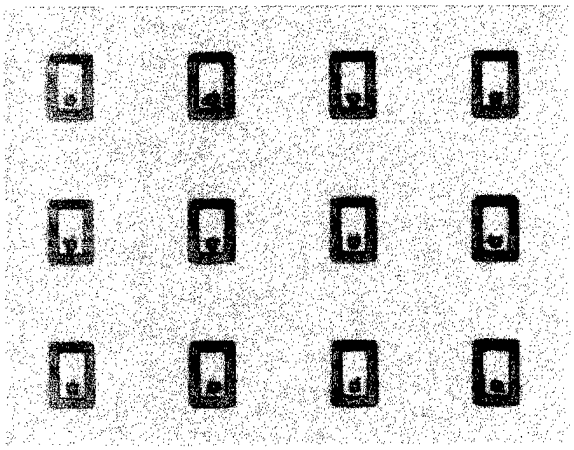


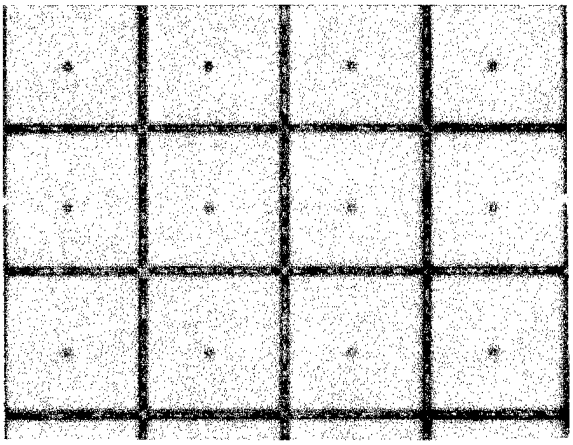
Figure 3. Schematic diagram of the pixel structure with the inclusion of an intermediate blocking layer.



(a)



(b)



(c)

Figure 4. Stages of the metallization process to microfabricate a light protected DRAM SLM. (a) Starting wafer, (b) the light blocking intermediate layer, (c) the top level metal.

The effectiveness of these changes to the DRAM pixel structure were investigated using the 176 DRAM SLM. Wafers were fabricated creating different pixel structures. The commercially fabricated wafer has one layer of metal and a low pixel mirror fill factor. One wafer was fabricated using the first generation of post-processing which resulted in mirrors with 3um gaps between them. The second generation post-processing pushed this down to 1.5um gaps between the mirrors. Finally a wafer was fabricated with the additional metal blocking layer.

SLMs were fabricated using these different silicon backplanes which were then investigated for photo-induced charge leakage. The system to measure the photo-induced charge is described in more detail in the paper on the 512DRAM SLM in this issue [4]. The times quoted for the full width half maximum (FWHM), the time for the image to discharge by half, in table 1, are for devices illuminated with 0.5mW/cm2 He-Ne light. The 100% fill factor referred to when using the light blocking layer is to indicate the percentage of metal in the pixel area blocking light directly reaching the underlying silicon substrate. It can be seen that the post-processing of the silicon backplane improves the performance with respect to the photo-induced charge leakage problem. This can be accounted for by the reduction in the amount of light reaching the underlying silicon substrate. The second generation improvement to the post-processing again enhances the device. Finally the blocking layer further reduces the light reaching the silicon substrate again improving the device's performance with respect to the photo-induced charge leakage effect.

The 512 DRAM SLM has a photo-induced charge leakage of 1.16s [4], ~100 times better than the equivalent planarised 176 DRAM SLM. This almost entirely due to the different pixel design which uses a pmos pass transistor in a n-well which has a very small leakage current.

Pixel structure	Metal layers	Pixel fill factor	Charge leakage to FWHM
Standard processing	1	45%	340us
1st generation post-processing	2	81%	4.7ms
2nd generation post-processing	2	90%	8.2ms
Intermediate blocking layer	3	100%	12.0ms

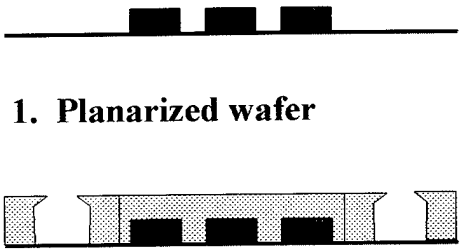
Table 1 Photo induced charge leakage for the different 176DRAM pixel structures.

Spacer Layers

Standard SLM construction relies on the use of spacer balls to determine the LC cell thickness. The cell thickness is therefore limited to the size of the spacer balls available. Also the use of spacer balls to construct the SLM cell results in the spacer balls on the active array seeding defects in the LC layer. We have developed a procedure to use microfabrication techniques to construct a spacer layer as part of our post-processing procedure. The spacer layer thickness can then be tailored to suit the application of the device. The LC cell thickness can be optimised depending on the wavelength or range of wavelengths being used.

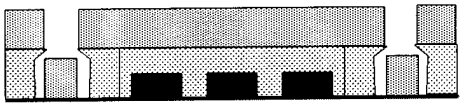
Since this layer follows the metallization of the mirrors a low temperature deposition technique must be used so that the metal layer will not deteriorate. A lift-off technique is also required to maintain metal quality which would be attacked during an etch process to pattern the spacer material. This places even stricter temperature requirements on the spacer material deposition as the photoresist used in the lift-off technique will only withstand temperatures up to approximately 140C. Also, since the ITO coating will be in direct contact with this spacer layer it must be constructed from a dielectric material to ensure no electrical shorts to the silicon substrate. Therefore, SiO2 deposited using electro-cyclotron resonance plasma enhanced chemical vapour deposition (ECR-PECVD) is used as the spacer layer material. Using this technique the SiO2 can be deposited at approximately room temperature.

The lift-off technique is described in figure 5. The starting point is a planarized silicon backplane wafer. Photolithography is performed to define the spacer layer. Prior to developing the wafer is soaked in chlorobenzene which hardens the top surface of the photoresist so that when the wafer is developed an overhang is created at the edges of the patterns. This helps to ensure that the ECR oxide film, which is deposited next, is not continuous over the photoresist. Finally the photoresist is removed taking with it the unwanted oxide leaving the patterned spacer layer. The thickness of the spacer layer is determined by the ECR oxide deposition which is accurately controlled.



1. Planarized wafer

2. Photolithography



3. ECR Oxide deposition

4. Remove photoresist

Figure 5. Schematic diagram of the lift-off technique used to microfabricate the spacer layer.

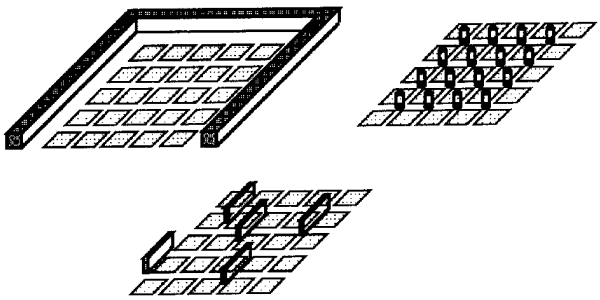


Figure 6. Structures of the various spacer layers under investigation.

Various spacer layer configurations have been designed and test structures fabricated, figure 6. The different structures are being used to investigate the effect on LC alignment of the new spacer structures. Initial results have shown that LC cells can be fabricated with LC cell thicknesses set by the oxide deposition process. As this technique is applied to devices with larger active areas supporting pillars or walls may be required in the middle of the array. Although these structures will seed LC defects, as they were microfabricated, there is some control of their position which will at least have the defects in designated regions.

It is anticipated that the spacer layers can also be used to help flatten the chip by forcing the chip to conform to the front cover glass. The chips warped by the silicon processing, multi-layer film deposition combined with numerous temperature cycling, can be supported by the much harder glass cover.

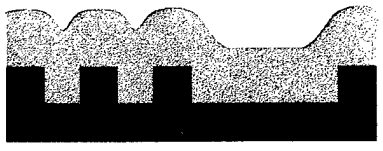
Once demonstrated with test structures this technique will be incorporated into the established post-processing procedure. The compatibility with the current procedure was considered when developing the spacer layer fabrication process and should therefore integrate with the current process without difficulty.

Damascene processing

The alignment of ferroelectric liquid crystal (FLC) is heavily influenced by the FLC flow rate during SLM cell filling [5]. This flow rate is affected by a number of factors which are determined by the quality of cell assembly and the control of the filling process. One aspect which could not be eliminated was the structure of the silicon backplane. Even when the device has been planarised the structure of the pixelated top layer metal still influences the FLC flow rate and therefore the FLC alignment. We have produced a flat silicon backplane substrate using damascene processing to manufacture the mirror/electrodes.

Damascene processing is a metal polishing technique developed in silicon processing to produce multi-level interconnect in advanced microelectronic devices [6]. In this process the oxide layer which has already been polished is etched to create trenches in the desired pattern of the metal layer, a blanket deposition of metal is then performed, which fills the trenches and covers the wafer surface, finally CMP is performed, which removes the excess material on the wafer surface leaving the metal in the trenches and the top surface flat, see figure 7.

1. Etch planarised dielectric layer



2. Blanket deposition of metal

3. Chemical mechanical polishing to remove excess metal.

Figure 7. Schematic diagram of damascene process.

The application of this technique changes the metal structure of the pixel. With the standard process the structure of the metal layer is still evident. It is normally in the region of 1um thick and the top surface has a variation of 1um. Also the effect of the pixel via is apparent which contributes to light loss through scattering. However, the pixel fabricated using the damascene process results in a flat substrate and the pixel via has no effect on the top layer, figure 8.

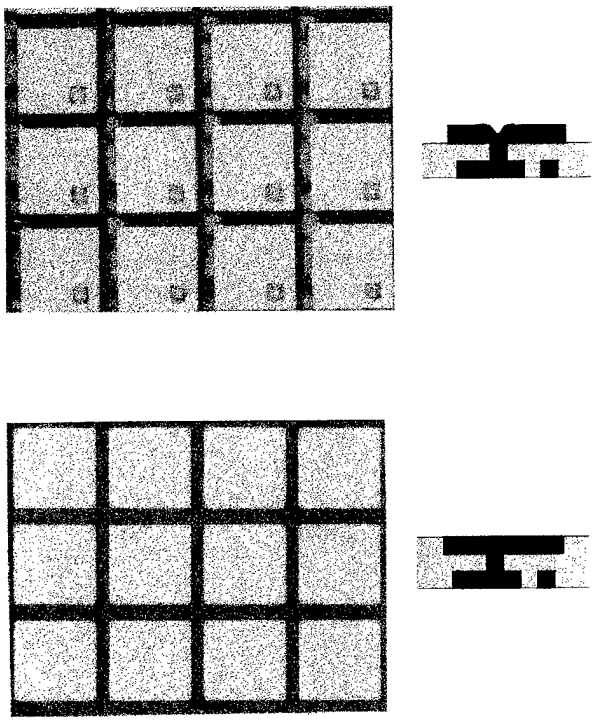


Figure 8. The different pixel structures produced using standard processing and damascene processing.

The pattern of the mirror/electrodes is defined in the standard process by the photolithography followed by the metal etch. With the damascene process the mirror/electrodes are defined by the photolithography followed by the oxide etch. The oxide etch to produce a square grid of very thin walls is easier than a metal etch to produce very thin gaps between the mirror/electrodes, figure 9.

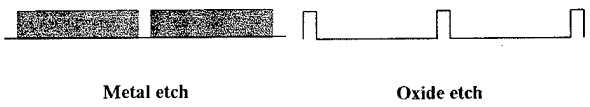


Figure 9. Schematic diagram illustrating the difference between the metal etch and the oxide etch.

A test structure based on the 176 DRAM SLM design was fabricated where the gap between the metal was made as small as possible. To do this the planarization mask used in the standard process was photographically copied onto another mask but with the opposite sense. This mask is then used to define the oxide etch. The gaps between the mirror/electrodes on the mask was set for 3um on the silicon, this is the first generation post-processing mask. To reduce the gap size ,ie. microfabricate very small wall structures in the oxide the mask was shifted and the wafer exposed multiple times. In this manner very fine features were created in the photoresist. The wafer then proceeded through the damascene procedure. Figure 10. shows the potential of the damascene process to produce very high fill factor mirrors.

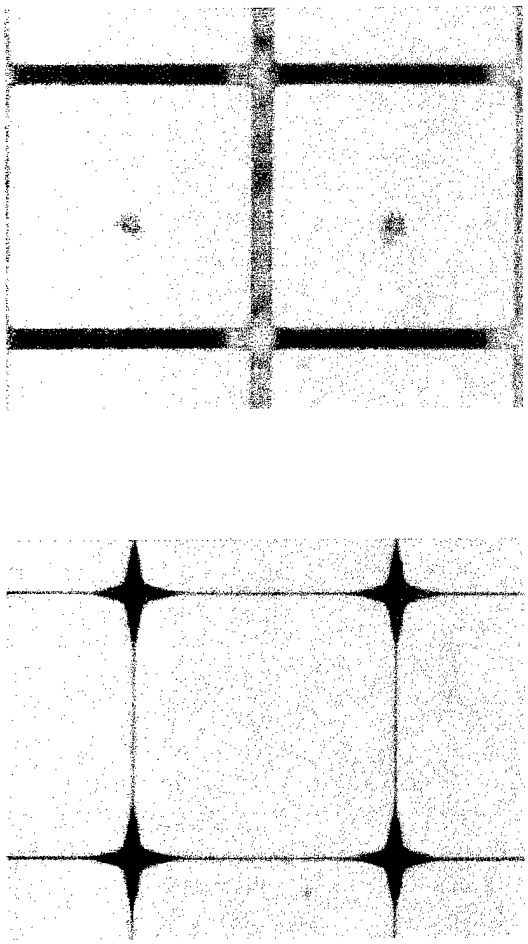


Figure 10. The 176 pixel mirror/electrodes microfabricated using the standard process and the damascene process with mask shifting and multiple exposure.

The reduction in definition of the mirror/electrodes at the corners is due to the multiple exposure of the wafer during photolithography, the edges of the mirrors being exposed twice to only once at the corners. Although a complex photolithography process was employed to define the oxide etch, the damascene process has reproduced in the metal layer the pattern defined by the photolithography.

The CMP system set up to polish the metal is different for the oxide polishing. A proprietry slurry based on ammonium persulphate was used with a Rodel politex polishing pad. The resultant metal surface showed no sign of scratching and was of an high optical standard.

Initial test samples have been studied and demonstrate the potential of this technique to improve the FLC alignment. Due to the flat surface of the completed metal structure the FLC flow across the device is more even which results in improved FLC alignment.

We have used this technique to pattern aluminium mirror/electrodes. This technique can also be uesd to produce copper mirror/electrodes which have better optical performance in the near infra-red. Dry etching of copper is very difficult and this is primarily the reason that copper is not used in standard silicon processing. However, with damascene processing which is based on a wet process and mechanical effects the copper can be processed. The damascene technique is being extensively investigated in the silicon microfabrication industry as a way to produce copper interconnect and at Edinburgh we are looking at the technique to produce copper mirror/electrodes.

Conclusions

The post-processing of commercially fabricated silicon backplanes for SLMs improves their optical performance. The use of chemical-mechanical polishing to planarise the inter level dielectric produces high optical quality surfaces onto which the mirror/electrodes are deposited.

Changes and additions to the post-processing procedure have been investigated with a view to enhancing further the optical performance of the silicon backplane. The large fill factor mirrors and the inclusion of an additional blocking layer reduced the amount of incident light onto the silicon backplane from reaching the substrate so improving the DRAM performance in the area of photo-induced charge leakage. An additional dielectric layer is being investigated to act as a spacer layer. This layer can be shaped and the thickness

determined to improve the FLC layer and tune it to the application wavelength of the device. Finally a change in the procedure to use damascene processing has been described. The application of this technique to produce high fill factor mirrors and a backplane with a flat surface conducive to good FLC alignment was demonstrated.

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THE CONCEPT OF ELECTROHOLOGRAPHY AND ITS IMPLEMENTATION IN KLTN CRYSTALS

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Abstract:

We present an experimental demonstration of **Electroholography** which is a new generic architecture for spatial light modulation. It is shown that Electroholography, which is based on the voltage controlled photorefractive effect at the paraelectric phase, enables to govern the reconstruction process, and perform electrical multiplexing of volume holograms by an external electric field.

Keywords

Photorefractive nonlinear optics, Volume holographic gratings, Electroholography, Spatial light modulators.

Electroholography (EH) is a generic concept in optoelectronics, which enables to govern the reconstruction process of volume holograms by an external electric field. EH is based on the use of the voltage controlled photorefractive (PR) effect in crystals at the paraelectric phase(1) . The PR effect enables the recording of volume holograms in a crystal, by spatially modulating its index of refraction in response to light energy it absorbs. In crystals at the paraelectric phase the PR effect is voltage controlled, namely, one can control the efficiency of the effect by applying an external electric field to the crystal during the reading (reconstructing) stage.

In general, the diffraction efficiency of a phase hologram is proportional to the local photoinduced changes in the index of refraction ($\delta(\Delta n)$). At the paraelectric phase the electrooptically induced modulation of the index of refraction depends quadratically on the induced (low frequency) polarization (1). When, during the PR process, a space charge field $E_{sc}(x)$ is formed in the crystal, the modulation which it induces in the index of refraction, and contributes constructively to the diffraction is given by:

$$\delta[\Delta n(x)] = n_o^3 \, g \, \varepsilon \, E_o \, E_{sc}(x) \qquad [1]$$

where $\delta[\Delta n(x)]$ is the amplitude of the induced birefringence grating, n_o is the refractive index, g is the effective quadratic electrooptic coefficient, ε is the dielectric constant (assuming the polarization is in the linear region (i.e. $P = \varepsilon E$), with $\varepsilon_r >> 1$), and E_o is the externally applied field.

Thus it can be seen that a hologram stored as a spatial distribution of a space charge is transparent to the reference beam, unless an external electric field is applied. The application of the field causes the space charge to induce a spatially correlated modulation in

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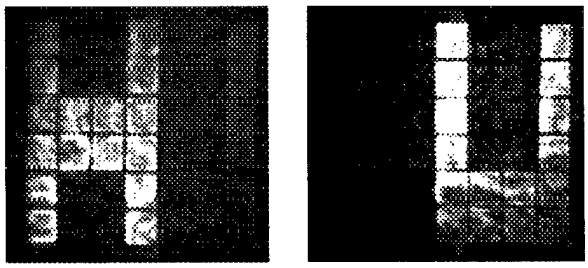
the index of refraction which diffracts the reference beam and reconstructs the hologram.

It should also be noted that since it is required that the reference beam will be Bragg-matched to the recorded hologram, a Bragg-detuning occurs by changing the field during the reconstruction (2). It can be shown that in a transmission geometry with equal angles of incidence there is no detuning. However, in a reflection geometry the detuning is zero only when the external field during the reading stage (E_R) is equal to the external field used in the writing stage (E_W). Thus, the transmission geometry is desirable for devices in which analog control of the diffraction is required, whereas the reflection geometry is advantageous for the implementation of electric field multiplexing of the holograms.

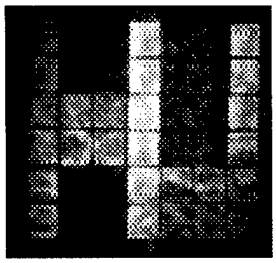
EH was originally conceived for the implementation of artificial neural networks(3). In the EH ANN the integration between the electronic processor and the holographic synapses is done at the component level (3). Each neuron is an electronic circuit integrated with a minute volume hologram acting as its synaptic terminals. Thus, a neuron complete with its synapses is implemented in an area element. As a result the dimension of the network scales as the area of the device (rather than its square root as in purely electronic realizations).

The EH concept was experimentally demonstrated on a system containing two EH pixels(4). A KLTN crystal doped with copper and vanadium was used. The temperature of the crystal was set to 12°C above its phase transition temperature, therefore the experiments were performed well within the paraelectric phase. Two samples (2x2x1 mm^3 each) were cut and polished along the crystallographic [100] direction, for realizing the two transmission EH pixels. Gold electrodes were sputtered over the edges perpendicular to the optical axis of the system. The same SLM was used to produce the source images of the holograms stored in the EH elements.

During writing, a different picture created by the SLM is stored in each one of the EH pixels separately. During reading (reconstruction), the reference beam is incident on both pixels and the stored holograms are reconstructed according to the voltages applied to the two EH elements (V_a and V_b respectively). Consider Figure 1 showing a typical experiment. The Letters 'H' and 'U' are produced by the SLM, and are stored as holograms in the EH pixels a and b respectively. Reconstruction of these letters is shown in Figure 1a and 1b. In figure 1a V_a=200V (producing a field of 1kV/cm on the crystal), and V_b=0. In Figure 1b V_a=0 and V_b=200V. In Figure 1c V_a=V_b=200V and consequently both hologram are reconstructed and superimposed in the detectors array plane.



(a) (b)



(c)

Figure 1: Selective reconstruction from two Electroholographic elements (a) V_A='on' & V_B='off', (b) V_A='off' & V_B='on', and (c) V_A='on' & V_B='on'

Electric field multiplexing of three planar gratings in a reflection EH element is presented in Figure 2. We recorded reflection holograms on a sample of KLTN crystal. The sample dimensions were 4x4x3 mm^3, it was cut and polished along the crystallographic [001] directions. Transparent ITO electrodes where deposited on the optical faces in order to align the external electric field with the direction of the grating wave vector. The three gratings were recorded under fields of 1.7, 2.7, and 3.7 kV/cm respectively. Finally, we multiplexed images of a resolution target rotated at three different angles under fields of 1.7 , 2.7, and 3.7 kV/cm respectively. No cross talk was observed during reconstruction of the three images at the respective writing fields.

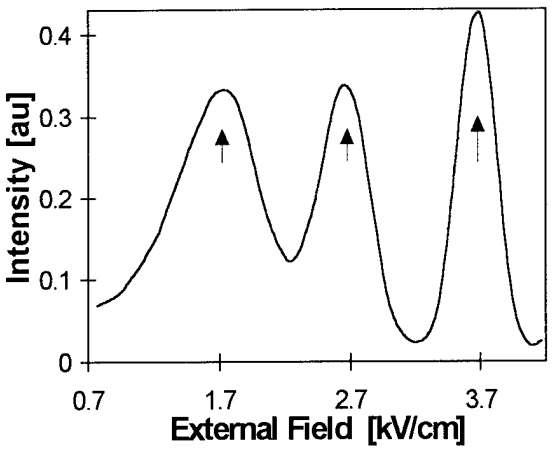


Figure 2: Electric field multiplexing Results of the Diffraction Efficiency as Function of the electric field applied during the reconstruction.

Finally it should be noted that EH was implemented in special KLTN crystals. The composition of these crystals was optimized for this purpose(5). Furthermore, special efficient fixing processes which do not require large temperature changes are being developed in these crystals(6).

The two sets of experiments described above demonstrate the potential of EH as new type of spatial light modulation. In the EH SLM each element can generate a complete image rather than one pixel. The image is not hard-wired but can be preprogrammed by the user. In addition if electric multiplexing is used, each element can generate one image out of a set of prestored user defined images.

Acknowledgments

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Modeling Electric Field Induced Effects in PLZT EO Devices

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Abstract

PLZT 8.8-9.5/65/35 electrooptic (EO) devices subject to electric fields on the order of 1 $\frac{V}{\mu m}$ can become highly scattering and depolarizing as well as exhibit high-order EO effects. We describe a method of modeling EO modulators that encounters for these effects. Utilizing these characteristics in simulating surface electrode devices we compare our model to measurements of a fabricated device and find excellent correlation.

Key Words
PLZT modeling, Scattering and Depolarization, Optical Characterization, Mueller Matrices.

Introduction

Applying the advances in electronic and optical computer aided design (CAD) to optoelectronic systems requires precision simulation of electrooptic (EO) devices. In this paper we present a simple but accurate method of modeling EO devices using, as an example, lanthanum-modified lead titanate zirconate (PLZT) with compositions 9.X/65/35. These ferroelectric ceramics have strong EO effects and are cost effective and are therefore excellent candidates for use in optoelectronic systems. In the absence of field the ceramic is optically isotropic whereas an applied field induces anisotropy and optical birefringence. This electrooptic response has been modeled as a classic Kerr quadratic effect [1] as well as a combination of linear and quadratic effects [2]. However, these techniques fall short of accurately modeling fabricated devices, which will be required for optoelectronic CAD tools.

We have developed a simple method of characterizing a sample of EO material (e.g. PLZT) using a set of equations that relate scattering, depolarization and electrooptic effect to applied electric field. By integrating these responses with the calculation of the field, for given device geometries and driving voltages, we have achieved excellent correlation to experimental data. In this paper we describe our EO characterization and device modeling, with an emphasis on comparisons of computer simulation to fabricated devices.

Transmittance Model and Characterization

Previous work [3] and experimental evidence shows that light passing through PLZT-based devices experiences depolarization due to multiple scattering effects. Therefore, we use the coherency matrix formalism, which describes partially polarized light by taking into account polarized and unpolarized

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components, to generate an equation describing the intensity of a monochromatic plane wave transmitted through our apparatus. For example, for linearly polarized light passing through crossed polarizers set at 45° the equation relating transmitted intensity to change in relative phase is given by

$$I = \tfrac{1}{4}\left\{A + B + 2C \pm 2\sqrt{AB}\cos(\phi)\right. \qquad (1)$$

where A and B represent the polarized light intensity measured along the two orthogonal basis and C is the unpolarized component, ϕ is the change in relative phase between the two orthogonal components. Choosing four pairs of angles, for the incident polarizer and analyzer, gives four equations which are used to solve for the relative change in phase ϕ.

By sandwiching our PLZT sample between two large, parallel, gold-plated copper plates we generate a constant field inside and outside the ceramic. The distance between plates and the thickness of the PLZT give us the electric field strength and interaction length, respectively. We experimentally measure the normalized optical intensity for various orientations of the polarizer/analyzer pairs (see Figure 1). For incident light polarized at 45° with a parallel analyzer we see a sinusoidal variation of the intensity as the relative phase is changed with applied voltage, as predicted in Eq. 1. In the measurement of the vertical (0°) and horizontal (90°) components we see the effects of scattering and depolarization as the field is increased.

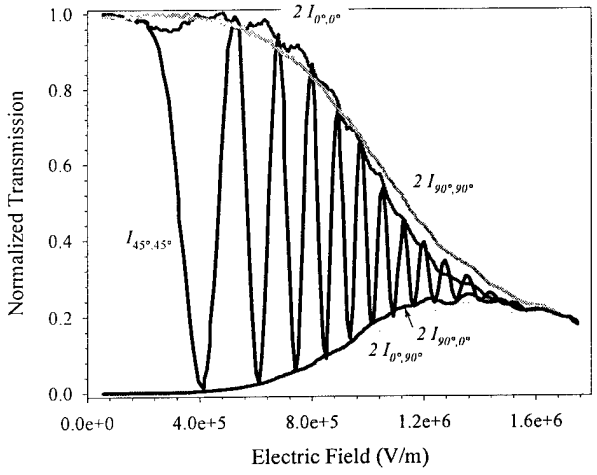

Figure 1. The sinusoidal curve is the transmission through parallel polarizers oriented at 45° to the direction of the electric field. The mismatch between this curve and the 'envelope' is due to a wedge shaped PLZT sample that results in slightly varying path length within the sampled region.

Using the transmission data from Figure 1, we solve for the change in relative phase ϕ as a function of electric field (see Figure 2). To accurately curve fit the EO data we need to use at least a fifth order polynomial, indicating that the EO behavior of these PLZT ceramics cannot be fully described by the quadratic EO effect.

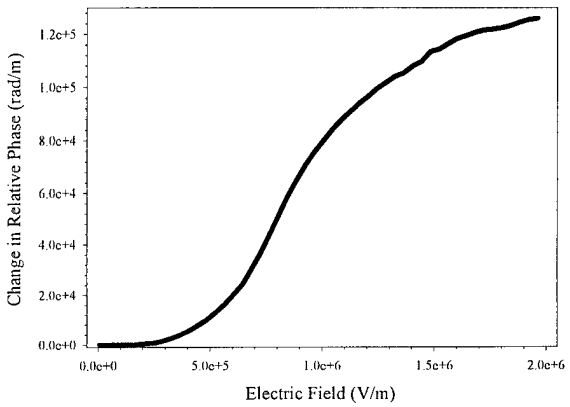

Figure 2. The change in relative phase is shown for the PLZT 8.9/65/35 composition.

Device Modeling

For a plane wave propagating through a PLZT based device we can use a standard index ellipsoid approximation [4] to find the index change for any two orthogonal polarization components of the light. We use a commercial finite element analysis (FEA) tool to calculate the electric field distribution for arbitrary device geometries. By integrating the change in index of refraction, scattering and depolarization data with the calculated electric field components we can determine the change in index as a function of position for any given device geometry.

For incident beam linearly polarized at 45° with respect to the electrodes and using an analyzer placed at -45° we compare our simulation with a fabricated surface electrode device. For this comparison, we used 1 mm CrAu electrodes spaced 500 μm apart and averaged the transmitted intensity from the center 100 μm of the gap. As can be seen in Figure 3, we

get an excellent match of device behavior, including the 'flat' response at low voltage, the reduction of maximum intensity due to scattering and the decrease in contrast due to an unpolarized bias component.

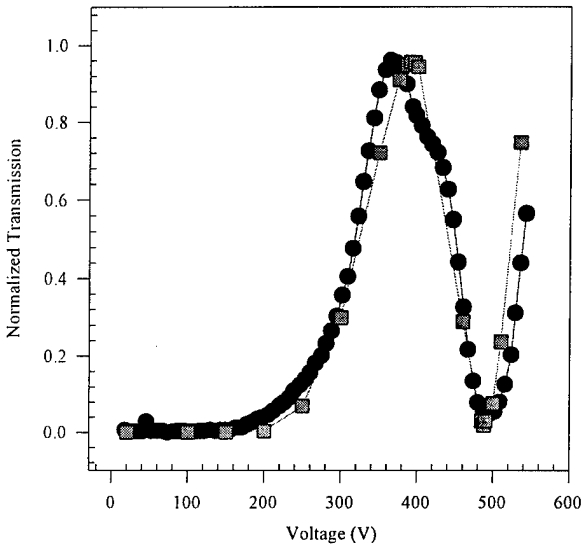

Figure 3. Comparison of measured performance of fabricated surface electrode PLZT device (dots) and computer simulation using new modeling method (line). Device has 2mm wide CrAu electrodes separated by a 500 μm gap and evaporated onto a 380 μm thick wafer.

Conclusion

By using four polarizer/analyzer orientations and taking measurements of optical response versus applied voltage we generate sufficient information to calculate the relative change in index of refraction for PLZT. From these measurements we extract information on the scattering, depolarization and change in relative phase. By incorporating that same information into simulating device behavior we then accurately model arbitrary geometries for polarization rotation devices. We are currently using this technique to optimize device design for a variety of performance characteristics including maximum contrast, efficiency and minimized cross talk. This empirically-based modeling of electrooptic devices is essential for developing accurate and reliable CAD tools necessary for design of future optoelectronic systems

Acknowledgments

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PHOTOREFRACTIVE MATERIALS FOR LIGHTWAVE MANIPULATION

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INTRODUCTION

Photorefractive materials are the key materials in future lightwave manipulation systems based on real-time holography. Typical photorefractive materials are ferroelectric crystals, such as $BaTiO_3$ and $KNbO_3$. These crystalline materials have a unique set of principal axes, and must be used in bulk form. Therefore they require very careful growth and processing before they can be used. For this reason there has been excitement by the recent development of new organic materials which can be easily made into thin films, and after poling exhibit photorefractive properties.

In order to exhibit photorefractive effects, materials must meet several requirements such as second-order optical nonlinearity to provide electro-optic response, and photoconductivity to create a space charge. Photorefractive effects were firstly observed in organic charge-transfer complex crystals: noncentrosymmetric organic crystals slightly doped with an electron acceptor.[1] After this demonstration, several research groups reported photorefractive effects in poled polymers.[2] Photorefractive polymers generally consist of three components: the first is a nonlinear optically active chromophore to provide an electro-optic response, the second is a hole transporting molecule and the third is a photosensitizer. The last two components provide photoconductive properties. Although these multicomponent systems have film-forming properties, they have multi-step carrier hopping processes which reduce the carrier mobility due to various traps. In order to create effective space charge modulation, efficient photocarrier generation and large drift mobilities are two of key factors which should be addressed. Moreover, there is a limitation of the maximum concentration of chromophores due to the phase separation in the multicomponent systems.

MONOLITHIC PHOTOREFRACTIVE MATERIALS

We have applied multifunctional chromophores to a new class of organic photorefractive materials.[3] They fulfill all the requirements for photorefraction and enable the development of "monolithic" photorefractive materials as shown in Scheme 1. As a building block, we selected acceptor-substituted carbazoles which are served as photoconductivity and electro-optic moieties. Highly branched structure with long alkyl chain offers film-forming property and glassy state with glass-rubber transition.

It should be noted that an alternative to our approach is through fully functionalized polymers. Although functionalized polymers have been developed as a macroscopic material, they have distributions of molecular weight, number and size of free volume, and molecular structures. On the other hand these molecular systems including the carbazole oligomers, can be considered as a perfectly defined structure.

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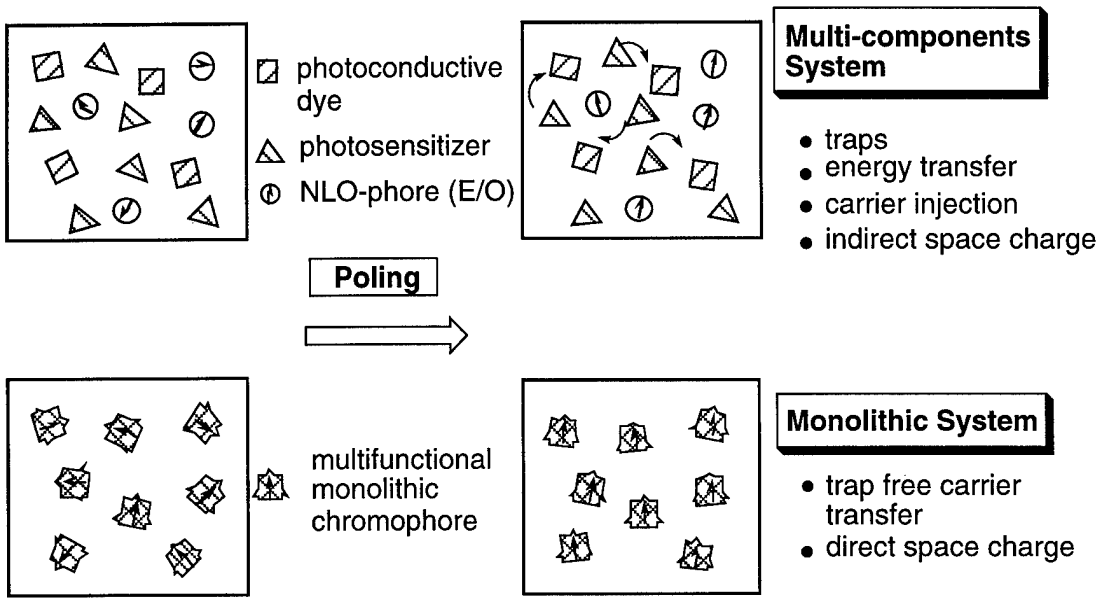

SCHEME 1 Multicomponent and monolithic photorefractive materials.

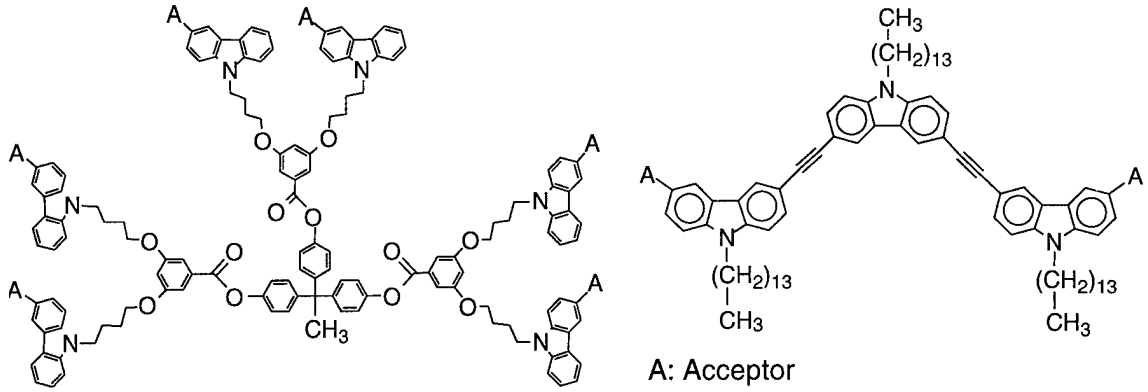

FIGURE 1 Multifunctional chromophores for monolithic photorefractive materials.

Carbazole starburst dendrimers and conjugated trimers have film-forming properties and as well as a glass-transition. The glass-transition temperature (Tg) changed depending on the length of a spacer, acceptor groups, and the number of carbazole rings. Amorphous molecular solid films were made without a support matrix by spin-coating from a solution. These thin films could be poled at above Tg to achieve the noncentrosymmetric alignment required for an electro-optic response.

PHASE CONJUGATION

Photorefractive effects in poled monolithic materials were confirmed by the two beam coupling and four-wave mixing measurements.[4] An asymmetric optical energy exchange in the two beams has been observed. Optical image reconstruction of distorted images using phase

conjugation was demonstrated. Figure 2 shows the phase conjugation demonstration via four-wave mixing. We have developed "monolithic photorefractive materials" using multifunctional chromophores and demonstrated their capability to manipulate the lightwave propagation using low power laser sources.

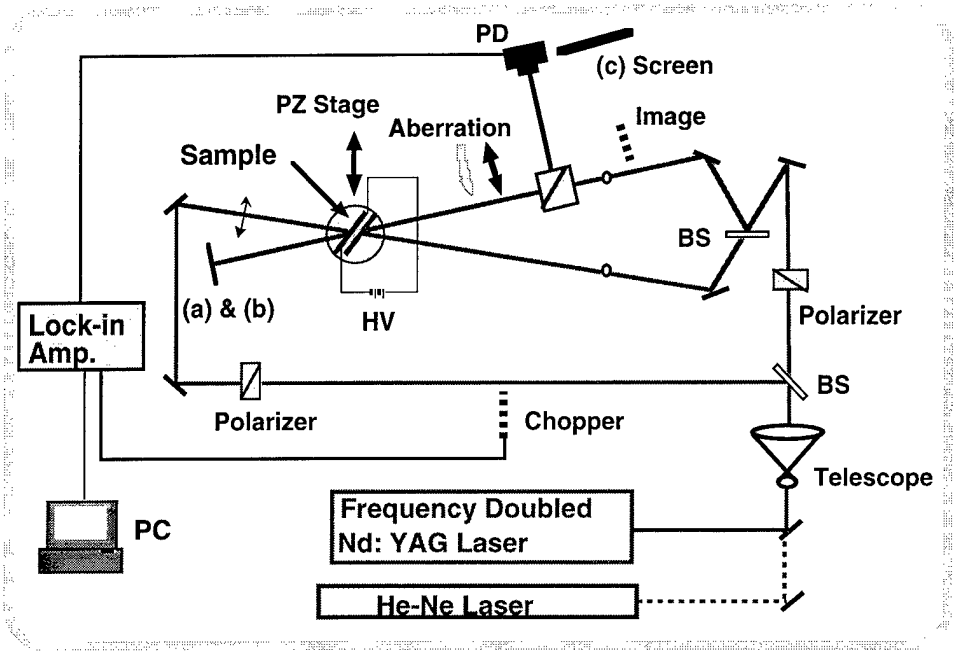

FIGURE 2 Phase conjugation via four-wave mixing for the correction of distorted images: (a) input image, (b) distorted image and (c) conjugated image.

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Spatial Light Modulators with Polymeric Thin Film Fabry-Pérot Etalons

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Abstract

An electrically addressable spatial light modulator with a spin-coated azo-dye/polymer thin film sandwiched with Fabry-Perot etalon is designed for optical information processing and display. Transmissivity of the device was electrically modulated. The contrast ratio of 70:1 was obtained at 1kHz with 15V ac applied voltage.

Key Words

Spatial light modulator, Fabry-Perot etalon, Polymeric material, Electrooptic effect.

Introduction

Spatial light modulators (SLMs) play very important roles for optical computing, including optical neural network and optical image processing. Advances in SLM technologies therefore have a direct impact on these critical application. [1)]

Liquid crystal SLMs generally used in optical computing have a very slow modulation speed and a low contrast ratio. Development of sophisticated SLMs with both very fast modulation speed and high contrast ratio is essential. One of the candidates for SLM material is nonlinear organic materials which have large optical nonlinearity. Some organic materials offer a lot of advantages such as large variety of molecular structures with large nonlinearities and quick electro-optical responses. [2)] Polymeric materials is one of the most promising organic materials for nonlinear applications. [3,4)] Their fabrication is easy compared with growing single crystals of organic and inorganic materials; moreover, the dielectric constants of polymeric materials are generally 1/10 that of $LiNbO_3$. This makes it possible to operate polymer devices at very high frequency. Operation at 40 GHz was demonstrated with poled polymer optical modulator. [5)] In recent years, considerable progress has been made in the development of nonlinear organic materials having large nonlinearities and thermal stability. [6-8)] Some poled polymers have large electrooptic coefficient r comparable to that of $LiNbO_3$. Very advanced materials using DR19 of r_{33}=40-60pm/V was reported. It is enough electrooptic coefficient for a waveguide light modulator to control the light, but not enough for a spatial light modulator because the effective optical pass length is much shorter than that of a waveguide light modulator. It can be solved by using the Fabry-Perot etalon structure because it increases the effective optacal pass length acting across the spacer region and minimizes the drive voltages.

We will discuss here the advantages of these

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materials and the development of SLMs using them. We have simulated and demonstrated the electrically induced changes in light intensity using polymeric thin film in a Fabry-Perot structure.

Polymeric Spatial Light Modulators with a Fabry-Perot Structure

A limited number of research has been done on SLMs with polymeric film. An electronically addressable SLM is designed here for optical information processing and display (Fig. 1).

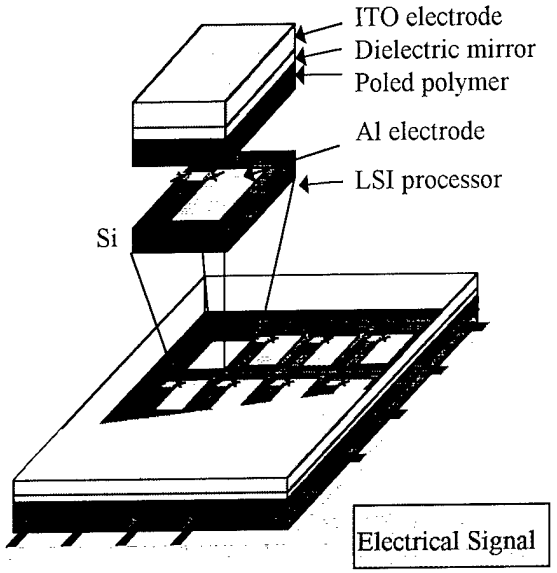

Figure 1. Electrically addressable SLM with polymeric materials.

It is composed of a dielectric mirror, a polymeric thin film, transparent electrodes, a planarization layer and a VLSI processor. The polymeric films which have a large electrooptic coefficient make it possible to achieve a high modulation speed and high contrast ratio. The use of a Fabry-Perot etalon is proposed to minimize the driving voltages(Fig. 2) Each mirror is composed of SiO_2(n=1.46) and TiO_2(n=2.35) of 17 layers. The reflectivity of the dielectric mirror is 99.4% at the wavelength of 633nm. The device shows a sharp spectrum in specific wavelength determined by the polymer film thickness and refractive index. We can control the intensity of monochromatic light by applying an electric field.

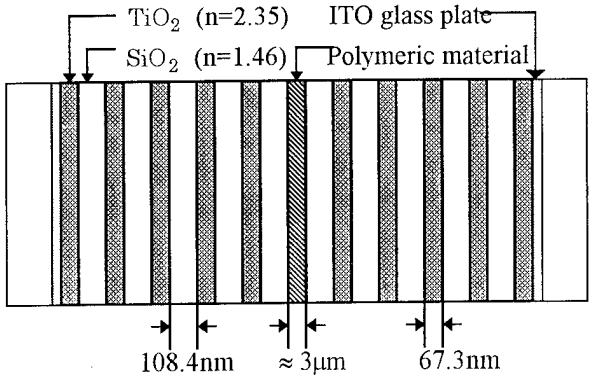

Figure 2. Resonator structure for polymeric materials.

Simulations

We simulated the light modulation of the polymeric thin film Fabry-Perot device. We have previously shown that Fabry-Perot devices are useful as electrooptic devices.[9] A film poled in the direction of the surface normal has the electrooptic tensor can be expressed as[10]:

$$\begin{vmatrix} 0 & 0 & r_{13} \\ 0 & 0 & r_{13} \\ 0 & 0 & r_{33} \\ 0 & r_{13} & 0 \\ r_{13} & 0 & 0 \\ 0 & 0 & 0 \end{vmatrix}$$

where $r_{33}=3r_{13}$.[11]

For an electric field in the direction of the surface normal(z-direction), the equation for the refractive index ellipsoid is

$$\left(\frac{1}{n_0^2}+r_{13}E_z\right)\left(X^2+Y^2\right)+\left(\frac{1}{n_e^2}+r_{33}E_z\right)Z^2=0 \quad (1)$$

where X, Y, and Z refer to the laboratory axes parallel to the principal dielectric axes parallel

to the principal dielectric axes of the film, and n_0 and n_e are the ordinary and extraordinary refractive indices respectively. On application of an electric field in the direction of surface normal, the change in refractive index experienced by ordinary ray is thus,

$$\Delta n_0 = -\frac{1}{2} n_0^3 r_{13} E_z \tag{2}$$

and for the extraordinary rays,

$$\Delta n_e = -\frac{1}{2} n_e^3 r_{33} E_z \tag{3}$$

Changes in the indices of refraction experienced by the ordinary ray can be related to the modulation voltage V by the expressions, using (3) as

$$\Delta n_0 = -\frac{1}{2} n_0^3 r_{13} \frac{V}{l} \tag{4}$$

where l is the separation of the two ITO electrodes. This induced Δn_o changes the device transfer characteristics by a phase change in the polymeric layer. Figure 3 shows the simulation of the change in transmissivity by applying dc voltage when film thickness was 3 μm, film refractive index was 1.6, dielectric mirrors had 17 layers, and electrooptic coefficient was 2pm/V. In this simulation, there is no optical loss of the sample, and there is no change of the reflectivity of the dielectric mirrors when applied voltage. We can control the intensity of monochromatic light by applying electric field. Figure 4 shows the calculation of the monochromatic light modulation. The contrast ratio in this case is estimated about 20:1 when the applied voltage is 10V/μm.

Experiment

We used a system consisting of disperse red 1 (DR1) doped poly-methyl-methacrylate(PMMA).

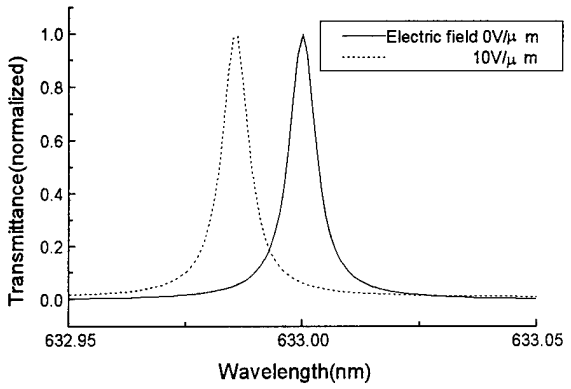

Figure 3. Simulation of changes in transmissivity by applying electric field when film thickness=3 μm, electrooptic coefficient=2pm/V, and dielectric mirror=17layers.

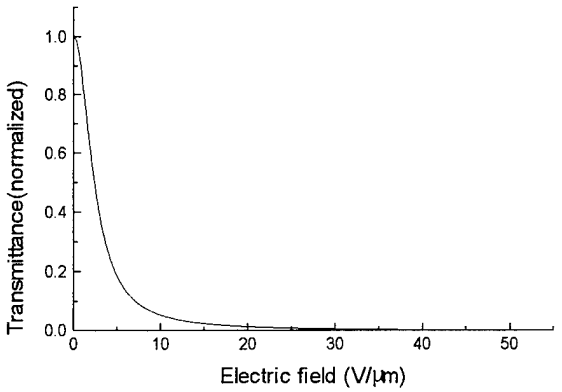

Figure 4. Simulation of changes in transmissivity at 633nm when film thickness=3 μm, electrooptic coefficient=2pm/V, and dielectric mirror=17 layers.

The azo dye disperse red 1(4-[*N*-ethyl-*N*-(2-hydroxyethyl)]amino-4-nitroazobenzene) is the nonlinear optic dopant molecule. PMMA is the polymer matrix material. The measured electro-optic coefficient r_{33} of DR1(3wt%)/PMMA was 2.9pm/V at the wavelength of 632.8nm. A 3 μm thickness film of DR1(10wt%) doped PMMA is prepared by spin coating on a ITO glass plate with dielectric mirrors. After baking at 90℃ for 30 min to remove the solvent, corona depositing poling[12] was performed to align the chromophore orientation. Then the sample was sandwiched between dielectric mirrors (Fig. 2).

Using experimental setup shown in figure 5, changes in transmissivity were observed by applying an ac voltage across the device and monitoring the transmitted light using a photo detector. Figure 6 shows the results of measurements of the changes in transmissivity of an unpoled DR1/PMMA film. Unpoled DR1/PMMA film has the center of inversion and has no electrooptic effect, these modulation are not by the electro-optic effect but by the mechanically induced changes in thickness due to compressive stress generated by attraction of the charged cavity mirrors. To separate any mechanical effects from the electro-optic effect, we measured the higher harmonics of the modulation frequency. Any mechanical effects will be observed at the second harmonic frequency, since the attractive force between the plates of a charged capacitor is proportional to the square of the modulation voltage. Figure 7 shows the results of modulation of poled DR1/PMMA at 1kHz. In this experiment, no mechanical effect was observed. Figure 8 shows the frequency response of the developed sample. The roll off occurred at 30kHz because of the electrical characteristics of the Fabry-Perot etalon. The contrast at 1kHz was 70:1 when the applied voltage was 15V.

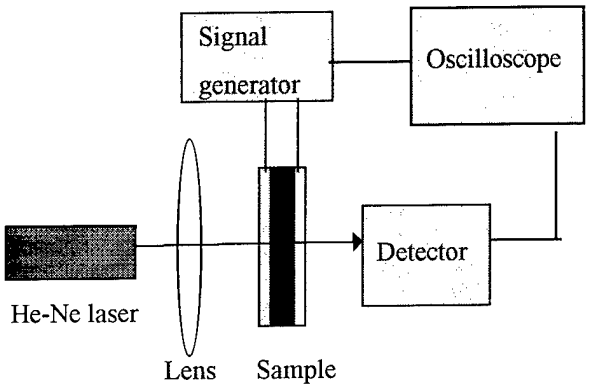

Figure 5. Experimental setup.

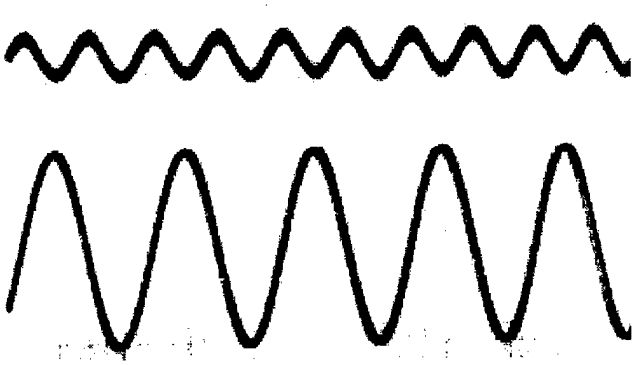

Figure 6. Light modulation of unpoled DR1/PMMA at 10kHz, 15V. (Upper: output signal)

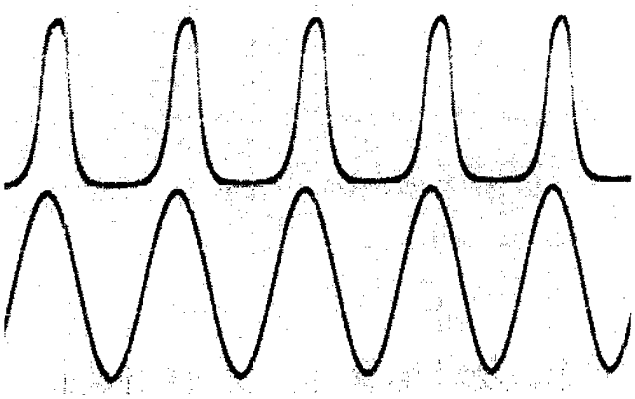

Figure 7. Light modulation of poled DR1/PMMA at 1kHz, 15V. (Upper: output signal)

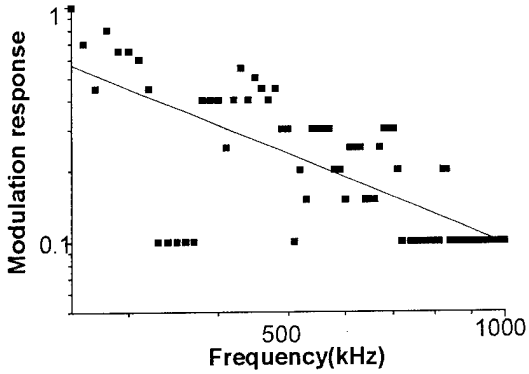

Figure 8. Frequency response of the developed sample

Conclusions

In conclusion, an electrically addressable high speed SLM is designed using polymeric thin film with Fabry-Perot etalons for optical information processing and display. The contrast ratio of

70:1 was obtained by applying ac voltage of ±15V. This contrast ratio is, to our knowledge, the largest modulation of the light intensity by electrooptic effect (may include some converse piezoelectric effect [13]). Fabry-Perot etalons have response limitations as a function of cavity finesse and cavity length.[14] Very high modulation speed cannot be expected using a resonator structure with large cavity finesse, but the modulation of devices with polymeric materials in our experiment was much faster than that of liquid crystal SLMs. These SLMs with nonlinear organic materials could be used for many applications in optical computing field.

Acknowledgements

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Microfabrication of Electro - Optical Structures in Polymer Films: Novel Polymer Waveguide Structure for Spatial Light Modulation

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Abstract

Microfabrication processing of polymer is suggested for creating new Spatial Light Arrayed Modulator (SLAM). This SLAM architecture is based on electro-optic modulation of light in 2-D array of polymer waveguide modulating pixels, providing also availability reconfiguration of optical interconnections between pixels of SLAM and optical processing scheme elements.

Key words

Spatial light modulator, waveguide, electro-optical polymer

Polymers for electro-optics

Electro-optical polymers feature large electro-optical coefficient, possibility to make waveguides, photoconductivity and photorefractivity, as well as attractive simple technology.

The possibility of the optical microfabrication (stable changes in optical parameters and film thickness) has been shown in azo dyes-containing polymers films [1].

Here we are reporting the light assisted microfabrication of resonance structures intended for spatial light modulation. The spatial light modulation structures based on Fabry-Perot resonator and similar resonant structures can be designed with such a processing.

Resonance structures for electro-optical modulation.

The sensitivity of E-O modulation can be enhanced significantly with application of the resonance structures as Fabry-Perot interferometers [2,3] or structures using internal total reflection, plasmon resonance and their combinations [4]. Another solution is concluded in waveguide light modulation, where there exists the possibility to extend the length of electrooptic interaction, increasing electro-optical response. Such modulating waveguides could be combined with Fabry-Perot and other resonance structures.

We have to take into account both the achievable contrast and possibility to integrate the separate modulating elements into SLM array.

Contrast considerations. The optical transmission for the birefringence mode of electro-optic modulator is described by expression:

$$T = T_0 \sin^2(\Delta\Gamma/2), \qquad (1)$$

with the phase shift $\Delta\Gamma = 2\pi \cdot \Delta n \cdot d / \lambda \Delta\Gamma$, where Δn is induced change of optical index, d is the thickness of film and λ is wavelength.

From (1) for $T \le 0.3\ T_0$ one can get with enough precision:

$$\Delta\Gamma \approx (T/T_0)^{1/2} \qquad (2)$$

It gives the requirements for phase shift. For example, the 30% depth of the modulation ($T/T_0 \approx 0.3$) requires near 1 rad of phase shift $\Delta\Gamma$.

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Similar consideration [2] for Fabry - Perot modulator gives:

$$\Delta\Gamma \approx (1\text{-}R)\cdot(T/T_0)^{1/2} \qquad (3)$$

One can see that in the case of Fabry-Perot resonator (F-P) the value of phase shift is diminished. approximately by the factor of F-P fineness: $F \approx 1/1\text{-}R$, where R is reflection of the F-P mirrors. Then for the same 30% modulation - $\Delta\Gamma \approx (1\text{-}R)$ rad. Compare (2) and (3) one can see how the depth of modulation is increased in F-P. For example with R=0.99 one needs only $\Delta\Gamma$ = 0.01 rad phase shift in E-O media to get the contrast of the amplitude modulation comparable with the contrast in the birefringence mode modulation (reachable there with the phase shift close to 1 rad).

With linear electro-optic effect the induced phase shift is $\Delta n \approx n^3 rE/2$, where r - is electro-optical coefficient and E - electrical field. For typical value for polymers: $r \cong 10^{-12}\text{-}10^{-10}$ m/V and the thickness of polymer film d=10 μm the phase shift at the wavelength of 0.63 μm is less than 10^{-2} rad for the electric field lower than 10^6 V/cm. This estimation of needed electric field is important for understanding of possibilities to integrate separate pixels into the array.

The integration of elements in the array. The SLM as a multi channel structure can be designed with electro-optic elements (formed in the polymer) placed on the top of microelectronic chip with electrical drivers. For a while microchips with large integration capacity (more than 10^4 cell/chip) allow the internal voltage only 30-40 V. Then to construct the SLM one or another technique have to be used to diminish required voltage to available 30 V.

Until now the known polymer-based F-P modulators [3] are working in the longitudinal mode, where the modulated light is propagating in the same direction as electric field and interaction length is restricted by the E-O layer thickness.

We suggest to use waveguide technology to enhance F-P modulation abilities as well as to provide new features to SLM. The schematic construction is depicted in Fig.1.

Here the polymer film over substrate creates an optical waveguide. The silicon (or GaAs) substrate carries electronic circuitry to address array of light modulating elements.

Each pixel consists of waveguide itself, beam coupling elements (prism-like elements are shown in Fig.1) and a couple of the Bragg mirrors, made as a rib on the surface of the waveguide or via optical index modulation of the bulk of polymer material. These Bragg mirrors form F-P resonator, acting in transmission.

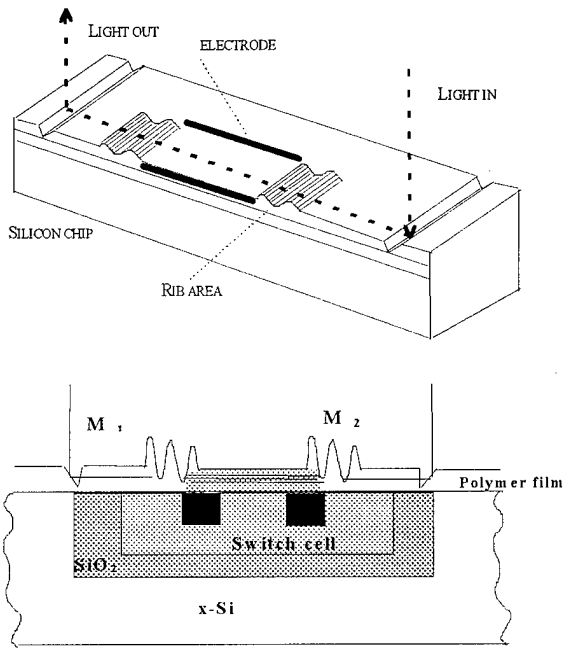

Fig.1. The waveguide Fabry-Perot interferometer as a pixel of Spatial Light Arrayed Modulator: optical layout of single pixel (upper part), the section of silicon wafer (chip with oxide dielectric isolation is shown as example) with polymer waveguide on its top (bottom part), M_1 and M_2 - holographic Bragg - type mirrors.

Electrodes laying aside of waveguide create transverse electric field. The advantage of transverse field in this case - one can make optical response larger than in longitudinal geometry due to longer E-O interaction length.

The light is entering the waveguide through the coupling element as it is pointed in Fig.1. Then traveling along the waveguide it fills F-P area. The optical length (and transmission) of this F-P is tuned by electrical field supplied by microchip via electrodes (as shown in Fig.1). Accordingly the intensity of light at the output of F-P is modulated. Finally through the second coupling element (left on the Fig.1) the modulated light breaks away waveguide to the free space again.

This construction does not need dielectric mirrors. The length of F-P cavity is determined by the distance between the Bragg-mirrors, those can be positioned by the accurate photolithography process. For fine tuning of the F-P resonator there is possibility to place additional pair of electrodes along with main pair. The same pair might serve for logical operations as additional input in F-P modulating element - in this case it turns out in two - inputs optical multiplier. The signals are delivered by silicon chip and can be initially electrical or optical (using photosensitivity of silicon) ones.

Planar geometry of suggested structure allows the distance between mirrors L = 100 μm (it means the density of elements at least 10^4 pixels/ cm^2 on the chip surface) and the width of F-P cavity area near d = 5 μm. With 30 V over all length phase shift under applied voltage could be as large as 6 10^{-1} rad - larger than in longitudinal F-P with the same polymer due to the ratio of L /d>>1.

With phase shift more than 10^{-1} rad the lower limit for the finesse of F-P drops to near 3-10, and correspondingly the demand to the Bragg-mirrors reflectivity to 70-90%. Reflectivity determines effective number of intracavity light pass, which to some extent equivalent to the corresponding elongation of length of electro-optical interaction. Then it is physically possible to perform electro-optical modulation in waveguide F-P in polymer with 30 V or even 5 V available with high speed microelectronics.

Bragg-mirrors can be made with the modulation of thickness or optical index of the waveguiding film. For guided wave rib-like area could achieve the high reflectivity. From coupled wave calculation reflectivity of rib-like waveguide area is approximately given by [5]

$$R=tanh^2 kL_0, \qquad (4)$$

where L_0 - is length of interaction (length of rib area along light propagation direction), $k = \omega\, \delta n/2c$, c- light velocity, δn - effective optical index modulation for material of Bragg- mirror.

Taking δn =0.1 we can estimate k = 0.1 μm^{-1}. With L= 10 μm Eq.4 gives R=60%, for L=20 μm R=97%, which leads to the finesse of F-P resonator near 30 - i.e. more than minimal requirements for the resonator finesse estimated above. In the case of surface relief (periodic change of film thickness - not its index) effective optical index modulation δn can be estimated by $\delta n= (n-1)\, \delta d/d$, where d is film thickness and δd is depth modulation.

There are a few methods to create the surface relief on the polymers: one can selectively etch the surface of silicon, direct etching of polymer can be applied, or direct optical writing can be used.

We have confirmed physical possibility with a few demonstration experiments making most of the suggested construction elements step by step. We have chosen for these experiments polymers with azo - dyes as side - groups. We have taken azo-dyes containing polymers (poly-Disperse Red-19 Toluendiisocyanate and poly-Orange Tom-1 Isophoronediisocyanate from Chromophore, Inc.). The structural formulae of both compounds are presented in Fig. 2.

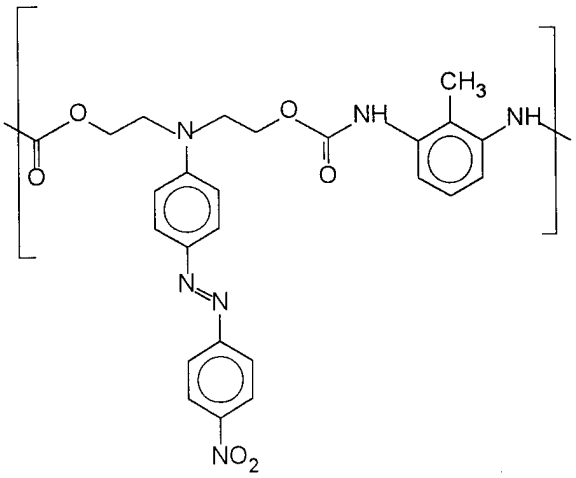

Fig.2 a. Poly-Disperse Red-19 Toluendiisocyanate

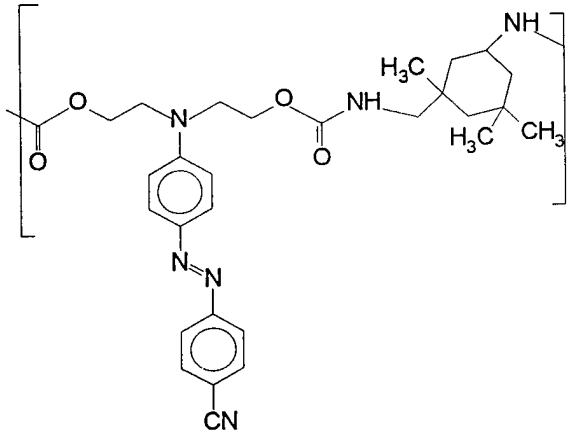

Fig.2 b. Poly-Orange Tom-1 Isophoronediisocyanate

These azo-dye groups impart a large electro-optical coefficient to polymers - up to 6 10^{-10} m/V for polymers with DR19 [1]

We prepared waveguides based on spin- coated films with thickness near 0.3-1 μm. The losses have been made less than 1 dB/cm in the best cases at wavelength 633 nm in these waveguides. This value is important as these are the losses contributing in the F-P resonator. The value 1 dB/cm corresponds to only a few percents of light losses for proposed length F-P cavity.

We have modeled the microstructures manufactured with the process of the photomodification of azo - dyes side polymers. This modification includes the change of refractive index of polymer as well as the surface relief creation and the change of absorption spectrum (as shown in Fig. 4).

For instance, we measured 50 nm change in the thickness of the polymer film under long UV exposure - 0.1-1 mW/cm^2 at 400 nm for 5 hours). So there is possibility to pattern the polymers like in photolithography - but with direct writing - without photoresist, solvents, etc.

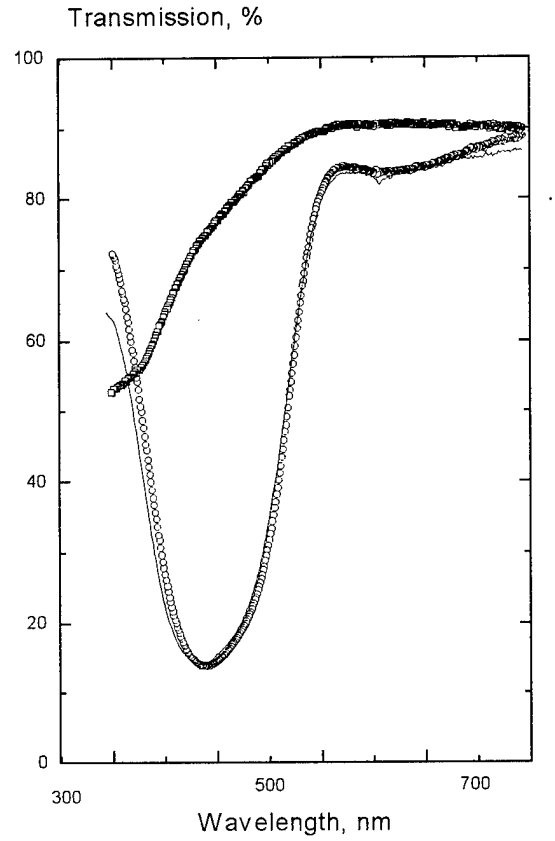

Fig.3 Optical transmission spectrum of poly-Orange Tom-1 Isophoronediisocyanate. Line marked with circles corresponds to the initial form of polymer, line with squares - to the bleached (with UV light) form, solid line - transmission of the film area with written holographic grating (diffraction efficiency near 8%).

We have made periodical resonance structures as a holographic gratings (suitable both for mirrors in F-P and for coupling purposes). To make these periodical structures we have recorded holographic phase gratings with 488 and 442 nm lasers at spatial frequencies up to 1000 lp/mm. Diffraction efficiency achieved 30% for transmitted light . Fig 4 shows the plot of the diffraction efficiency dependence of laser exposure.

This value of efficiency means that optical thickness of polymer films can be changed with at least 100 nm, what has been confirmed by direct measurement of surface relief with atomic force microscopy and contact scanning profiler.

Fig. 5 shows the result of investigation of obtained surface relief with AFM (Atomic Force Microscopy).

The combined optical, chemical and AFT techniques allowed to put forward the probable physical and chemical mechanisms of the observed photomodification of azo-polymers [6].

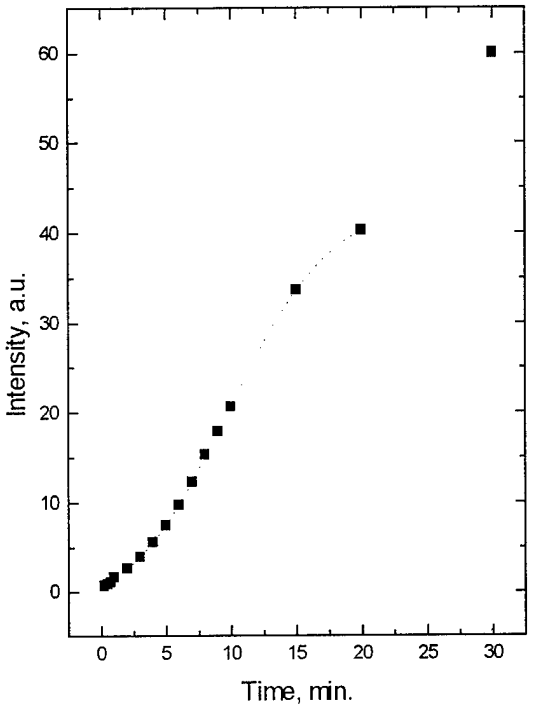

Fig.4. Diffraction efficiency of written hologram (in poly-Orange Tom-1 Isophoronediisocyanate film) as plotted during the exposure under Ar^+ laser illumination (488 nm with intensity near 20 mW/cm^2). Maximum efficiency is near 30%.

One can see that the spectrum of scan does not contain much of higher harmonics and the shape of grating is quite harmonical. This means that the process of the hologram writing is well linear on the light exposure. It means also that the shape of elements under the fabrication can be easily calculated and then constructed with the exposure of the light.

The grating coupling has been demonstrated. The efficiency of coupling in the waveguide was near 6-10%, while the efficiency of the coupling out the waveguide was close to 50% in one of diffraction order (as determined in respect to the light intensity coupled in waveguide). The difference is connected with length of interaction - in first case this length is of order of film thickness (1 μm), in the

second - of order of the aperture of the holographic pattern, (1-2 mm).

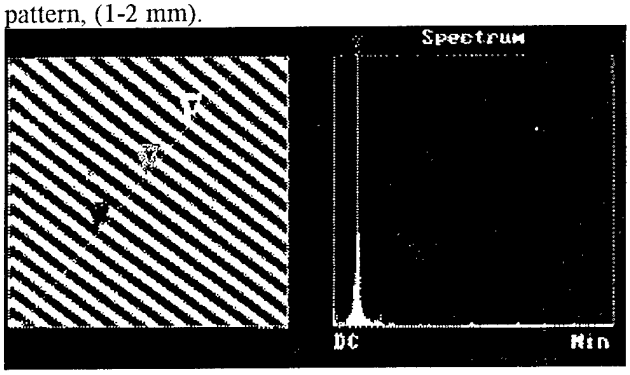

Fig. 5. The surface relief (near 30-36 nm) produced under holographic exposure with argon laser during a few minutes at intensity near 20 mW/cm^2 (measured with AFM). Period of grating is near 600 nm. Measured diffraction efficiency (in transmission) has near 10 % @ 633 nm. On the left side is AFT scan. On the right - the spectrum of this scan.

Diffraction coupling elements being manufactured from the same electro-optic material are giving new possibility. The angle of diffraction on these gratings is determined:

$$2\,D\sin\theta/2=n\lambda, \qquad (5)$$

where θ is the angle of diffraction and D is the period of pattern.

Deviation of diffraction angle is proportional to the index modulation :

$$\delta\theta \approx \delta n \cdot tg(\theta/2)/n. \qquad (6)$$

These consideration, presented here for wave propagating along the waveguide, means that this wave can be deflected from the initial by changing of optical index in the grating area.

Electro-optic effect in the polymers can be used for this change to deflect output light (additional electrodes should be placed in rib area). The deviation of angle is proportional to the optical index change. With $\delta n \approx 4\ 10^{-3}$ (under the same conditions as we describe for F-P resonator with $r = 6\ 10^{-10}$V/m) and at $\theta = 85°$ according to Eq.6 we can get $\delta\theta \approx 2.5\ 10^{-2}$ rad $=1.5^{o}$. In the same time the elements with $\delta\theta \approx 0.3^{o}$ are considered as practically useful [7].

This consideration is valid for thin holograms, while volume holograms obtain angle selectivity. Then electro-optic modulation of optical index leads to the modulation of diffraction efficiency[8]. The angular selectivity of volume holograms in electro-optic crystals is of order 0.1°. Then the change of optical index of polymer of order of 10^{-3} diminishes diffraction efficiency 10^2 times. Surely the thickness of this hologram has to fit the thick-hologram criteria, i.e. be in the region of 100 μm (or more) for optical index change of order of 10^{-3}. Apparently such a thickness of hologram can be combined with waveguiding thin polymer films via some hybrid technology.

Recently similar features for volume holograms have been suggested to use in neural network as it gives a tool for changing and learning of neural links[9].

Advanced SLAM architecture

The advanced SLAM architecture based on the polymers and enabling suggested features is shown in Fig.3.

Here we assume also that proposed enhanced SLAM could obtain possibility of optical and electrical control. Silicon chip carries the photodetectors with amplifiers, as well as electronic drivers controlling the electro-optical elements built in waveguide polymer film. We assume that these mentioned electronic drivers control as modulating elements, as well as coupling gratings, due the electro-optical interaction in waveguide and in grating areas.

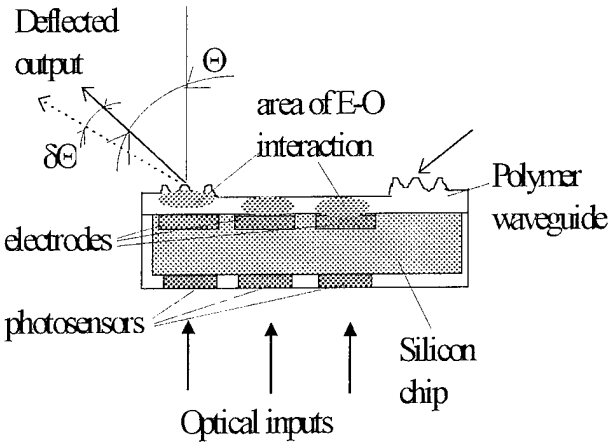

Fig.3. The simplified optical layout of the pixel part of the Advanced SLAM

It is important that one can write the holograms in polymer film placed over silicon chip, creating thus the links in optical processor (e.g., as the mentioned above coupling elements). The voltage applied to each pixel changes the intensity of each specific link or re-align this link to another site - changing the angle. All technology remains fully polymer-based - electro-optic modulation, wave-guidance, hologram writing, etc. are possible in the

same polymer material, featuring fast electro-optic response [1].

Conclusions

The light assisted microfabrication processing of polymers is suggested to create the resonance structures for integrated optics - such as Bragg -mirrors for Fabry-Perot interferometers.

On the base such structures in electro-optical polymers we propose the architecture of the new spatial light arrayed modulator (SLAM).

This SLAM provides electro-optic modulation of light in 2-D array of polymer waveguide pixels, reconfiguration of optical interconnection - the change of intensity of these connections or the change of the addresses of the pixels to be connected via deflection of the light. In this sense this polymer based SLAM can serve as a binding element between waveguide modulation scheme, delivering of light pulses, and an external free-space data array processing scheme.

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InGaAs Photodiodes for Infrared-Sensitive Optically Addressed Spatial Light Modulators

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Abstract

Infrared-sensitive InGaAs/InP photodiodes for liquid crystal spatial light modulators were grown by MBE. They exhibit record low dark current and capacitance.

Key Words: Detectors-infrared, Optical devices-spatial light modulators, Materials-detector materials

I. Introduction

Currently available optically addressed spatial light modulators (OASLMs) are sensitive only to the visible and near infrared (< 1.1 μm) light [1]. For many applications OASLMs which are sensitive to infrared (IR) light at 1.55 μm are required or preferred. A common OASLM light-modulating material is liquid crystal (LC) which can be addressed by a thin film photosensor [2]. This scheme requires that the photosensor exhibits very low dark current to prevent the LC from switching on in the absence of write light, and high photosensitivity to switch the LC on in the presence of write light [3]. An InGaAs/InP photosensor fulfilling these requirements will allow the successful fabrication of an IR-sensitive OASLM. An OASLM incorporating such a photosensor has been previously reported but exhibited a poor contrast ratio due to the large InGaAs/InP dark current [4].

In this paper, we investigate the optoelectronic properties of InGaAs/InP mesa-type p-i-n photodiodes grown by solid-source molecular beam epitaxy (MBE) for OASLMs. We summarize the requirements that these photodiodes must fulfill to address successfully ferroelectric liquid crystal (FLC) in an OASLM, as well as their fabrication and characterization. We present experimental data which include very low dark current densities ($1x10^{-5}$ A/cm^2), comparable to those of InGaAs photodiodes grown by other techniques [5-7], and the lowest reported for photodiodes grown by solid-source MBE. We found that the dark current at low applied voltage was limited by thermal generation-recombination in the depletion region. We measured a photoresponsivity at 1.55 μm of 0.8 A/W without anti-reflection coating. Capacitance was below 8 nF/cm^2 at 5 V reverse bias. Where defects were visible under an optical microscope, higher dark currents were measured which may explain the poor contrast ratio of OASLMs made with these films.

II. Design of IR-Photodiodes for LC OASLMs

For its fast response [8], we have chosen to incorporate FLC in our OASLM. The dark current of the IR-sensitive photosensor must be sufficiently small that it does not switch the FLC on during the *write* (negative voltage) drive period in the absence of write light. But the photosensor must provide sufficient photocurrent to switch the FLC on in the presence of IR write light during the *write* drive period of the OASLM [3]. Among various types of IR photosensors, InGaAs/InP p-i-n photodiodes provide both the lowest dark current and high photosensitivity to fulfill these requirements [4].

To achieve a high spatial resolution OASLM by incorporating the InGaAs/InP p-i-n photodiode to the FLC, the top p^+ layer must be made thin enough to reduce lateral charge spreading [9] in that layer. In addition to increase the depletion width in the InGaAs layer and hence reduce the undesirable asymmetry in the driving wave form which may cause ion accumulation in the FLC, the background carrier concentration of InGaAs must be as small as possible [4]. We have consistently obtained InGaAs background doping concentrations of $1\text{-}5x10^{15}$ cm^{-3}. Our calculations show that for this background carrier concentration and for typical FLC OASLM driving voltages, the depletion width should be about 1 to 3 μm. Our photodiodes have been grown accordingly and fabricated using this design.

III. Photodiode Fabrication and Characterization

Two InGaAs films were grown by solid-source MBE on InP substrates: film I is a p^+-InGaAs/υ-InGaAs/n^+-InGaAs homojunction structure with a 3 μm thick undoped InGaAs layer and film II is a p^+-InP/υ-InGaAs/n^+-InP heterojunction structure with a 2.6 μm thick undoped InGaAs layer. Both films have a very thin (< 1000 Å) and heavily doped p-InGaAs ohmic contact layer on top.

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Geoffrey Burdge and Sadik C. Esener (eds.)

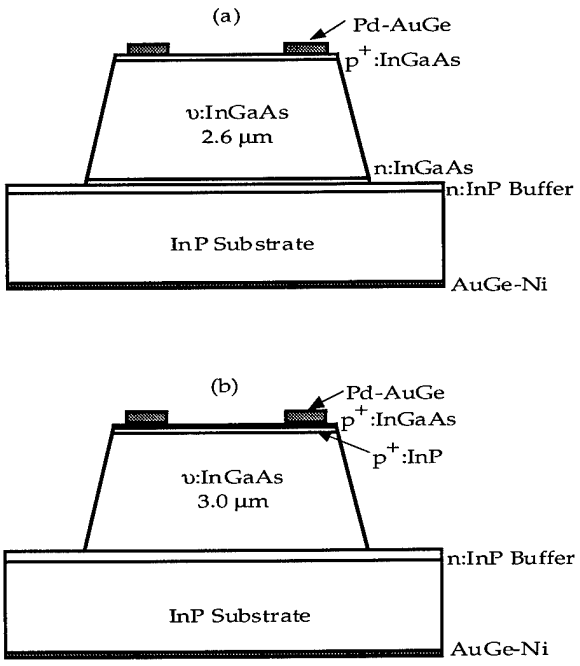

Figure 1. Schematic cross sections of (a) film I ($In_{0.53}Ga_{0.47}As$ homojunction) and (b) film II ($InP/In_{0.53}Ga_{0.47}As/InP$ double heterojunction) photodiodes.

Since the photosensor cannot be electrically probed after assembly with FLC into an OASLM, we fabricated mesa-type photodiodes of various areas (0.01, 0.05, 0.1 and 0.5 mm^2) by standard photo-chemical processing. The structures of the photodiodes obtained form both films are shown in Figs. 1(a) and (b). Capacitance-voltage (C-V) and current-voltage (I-V) characteristics were measured by probing the top metal contact and the substrate contact. The normalized C-V characteristics of photodiodes of film I are shown in Fig. 2. At 5 V reverse bias, the capacitance was below 8 nF/cm^2 for both films. However, while the

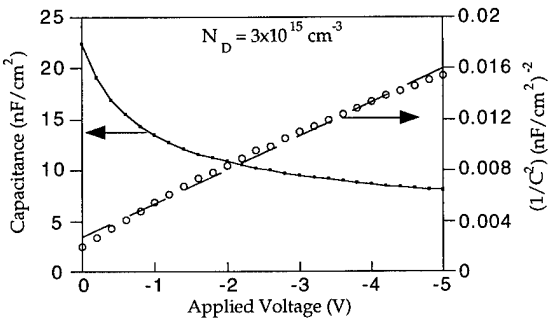

Figure 2. Capacitance-voltage characteristics of film I photodiode.

slope of the inverse capacitance squared versus reverse voltage curve ($1/C^2$-V characteristic) is linear for film I (and yields a net background concentration of $3x10^{15}$ cm^{-3}), it is nonlinear for film II because of the heterojunction. Still, we believe the background concentrations are the same in both films as they were grown by the same technique.

In Fig. 3 current densities versus applied voltage at room temperature are plotted for both films. Dark current densities were measured to be approximately $1\text{-}2x10^{-5}$ A/cm^2 at -5 V. At low reverse voltages the I-V characteristics fit well with a model of generation-recombination current in the depletion region assuming an intrinsic carrier concentration of $5x10^{11}$ cm^{-3} and an effective carrier lifetime of 0.8-1.0 μs (Fig. 3) [6].

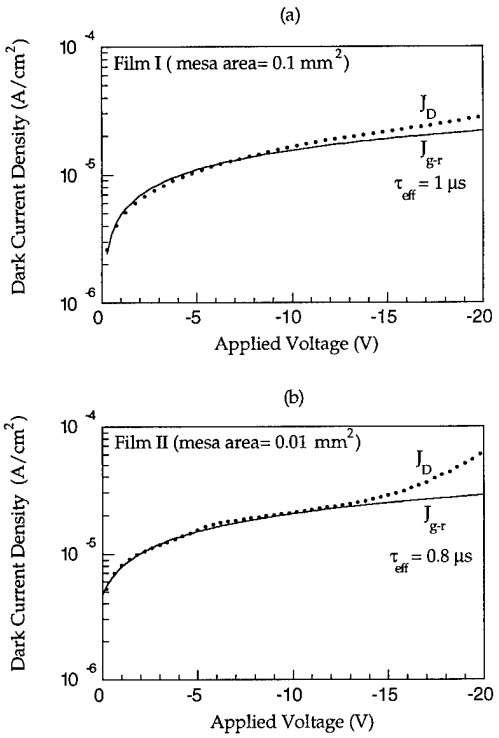

Figure 3. Measured dark current density, J_D , and generation-recombination current, density, $J_{g\text{-}r}$, versus applied voltage of (a) film I and (b) film II photodiodes.

IV. Anomalous dark currents

Although diodes of smaller areas exhibit low dark currents, some diodes of larger area (0.5 mm^2) have dark current densities 2 to 3 orders of magnitude higher (Fig. 4). These anomalous high dark currents have been found to correlate with visually observable defects (approximately 25 μm^2 in area). The average defect density was approximately

2000 cm^{-2} for both films after MBE growth. This large dark current which may be caused by these defects may explain the poor contrast ratio of OASLM assembled with these films. We are currently investigating the nature and cause of these defects.

Surface oxide on the mesa walls can also lead to additional leakage currents [10, 11] that we were able to eliminate by a simple passivation technique using a negative photoresist. This technique may also be used for pixellation of the InGaAs to improve OASLM spatial resolution.

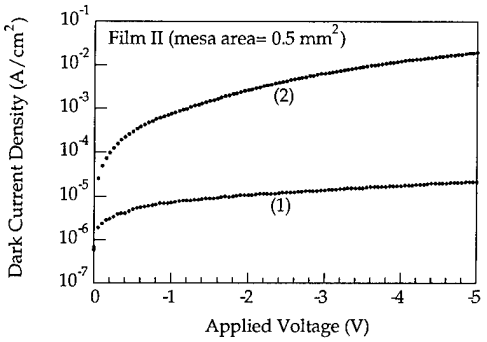

Figure 4. Dark current density versus applied voltage characteristics of film II diodes (1) without visible defects and (2) with a visible defect, approximately 25 μm^2 in area.

V. Summary and conclusions

We have fabricated low-dark-current, low-capacitance InGaAs/InP p-i-n photodiodes which meet the requirements of IR-sensitive liquid crystal OASLMs. However, the presence of defects in the InGaAs films seems to increase photodiode dark current and impede the proper operation of FLC OASLMs fabricated with these films.

VI. Acknowledgments

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Electro-optic polarization modulation in [110]-oriented GaAs-InGaAs multiple quantum wells

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Abstract

Ellipsometric techniques are used to measure the anisotropy in the complex indices of refraction of strained [110]-oriented quantum well p-i-n structures as a function of bias voltage and to characterize their performance as polarization modulators.

Key Words

Aniostropic optical materials, Semiconductors including MQW, Electro-optical devies, Ellipsometry and polarimetry.

Introduction

In order to modulate the polarization state of incident light, an in-plane anisotropy in the refractive index or the absorption coefficient or both are required. Unfortunately, conventionally-grown [001] heterostructures possess no intrinsic anisotropy in the plane of the quantum wells. Such material can be made anisotropic by application of an in-plane uniaxial strain. Indeed, Shen et al. [1] have recently fabricated a polarization rotation modulator with impressive performance by introducing uniaxial strain into a [001]-oriented multiple quantum well (MQW) structure. To obtain the uniaxial strain, they bonded a MQW structure to a substrate with an anisotropic thermal coefficient of expansion. In one direction, the substrate matched the expansion coefficient of the MQW material, while in the orthogonal direction the differential contraction between the substrate and the semiconductor imparted the required uniaxial strain. A maximum contrast ratio of 5000:1 was recorded; however, a significant amount of post-growth processing was necessary, and the thermally derived nature of the anisotropy make it sensitive to environmental temperature fluctuations.

Our approach here is to take advantage of the intrinsic anisotropy that can be obtained by growing in directions other than the [001] direction. The maximum anisotropy is predicted for growth on $(\sqrt{3}10)$ and $(1\sqrt{3}0)$ surfaces [2], however such material has not yet been fabricated. More readily available material can be found based on substrates orientated in the $[11\ell]$ family of planes, for which the [110] direction has the largest predicted anisotropy [3]. Application of an in-plane biaxial strain enhances the optical anisotropy [3,4].

We demonstrate that the optical anisotropy inherent in biaxially strained [110]-oriented GaAs-$In_xGa_{1-x}As$ MQWs can be used to construct a prototype electro-optic modulator that is sensitive to the polarization state of the transmitted light. In this device, application of a voltage across a p-i-n region containing the MQWs is used to produce a change in the in-plane birefringence and dichroism. This, in turn, causes a change in the ellipticity and a rotation of a linearly polarized input beam. Subsequently, a phase retarder and a linear analyzer are used to convert this polarization modulation into an intensity modulation. Ellipsometric measurements, which directly determine the degree of dichroism and birefringence as a function of wavelength and voltage, are used to optimize the operating wavelength, the alignment of the modulator and to predict the maximum contrast ratio. These results allow the design of future structures with an enhanced contrast ratio (1000:1), good bandwidth (4 nm), tunability (10 nm) and operating temperature range (35 °C), but with a relatively low throughput (1%). Even larger contrast ratios and throughputs are predicted for MQW structures with narrower excitons, but with a degraded bandwidth, tunability, and hence, increased sensitivity to temperature. This approach to the construction of polarization modulators requires only elementary post-growth processing. It is

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applicable to systems that require high contrast modulation and that can tolerate the larger insertion losses.

Experimental

The sample used in these studies is the same one used in our nonlinear optical studies and is described elsewhere [5,6]. It is a p-i(MQW)-n diode that was grown on a [110]-oriented semi-insulating GaAs substrate, which is tilted 6° towards the [111]B direction to ensure good layer quality [7]. The n region was grown immediately on top of the GaAs substrate and consists of a 1 μm n^+ GaAs buffer layer and a 100 nm layer of n-type GaAs. The intrinsic MQW region consists of 50 periods of 6-nm-wide $In_{0.13}Ga_{0.87}As$ quantum wells separated by 8-nm-thick GaAs barriers. The 13% indium concentration provides the necessary biaxial strain to enhance the optical anisotropy. The capping layer is 100 nm of p-type GaAs.

Following growth, the sample was processed into a series of mesas, each with an electrical contact which allows the capping layer to be biased with respect to a common electrical connection to the substrate. The electrical characteristics of the sample show it to be a good diode with a breakdown voltage of 20 V.

The laser used for these experiments was a mode-locked styrl-13 dye laser producing pulses with a full-width-at-half-maximum of 2 ps. The repetition rate was set at less than 3.8 MHz, to ensure complete recovery of the sample between pulses. Laser fluences of less than 0.2 μJcm^{-2} were used in order to ensure that the sample remained in a regime in which the absorption was linearly related to incident power.

Intrinsic Anisotropy

The room-temperature in-plane anisotropy in the absorption of the MQW region of this device is illustrated in Fig. 1. The solid curve represents the absorption spectrum measured for light polarized along the $[\bar{1}10]$ direction and the dotted curve for light polarized along [001]. The dashed curve gives the dichroism, $\Delta\alpha_{MQW}$ (i.e., the difference in the two spectra). The peak dichroism is seen to be $6.6x10^3$ cm^{-1}, which is close to the value predicted theoretically [3]. Also, notice that the heavy-hole excitonic resonance is much broader in this particular sample than in high-quality MQWs grown in the [001]-direction. As we discuss below, this feature can be advantageously used to increase the tunability and operating temperature range of the polarization modulator. For the data displayed in Fig. 1 the effects of the substrate have been eliminated by performing the measurements through the device plus substrate and through the substrate alone, then subtracting the two.

The birefringence Δn_{MQW} associated with the dichroism $\Delta\alpha_{MQW}$ can be indirectly obtained by performing a

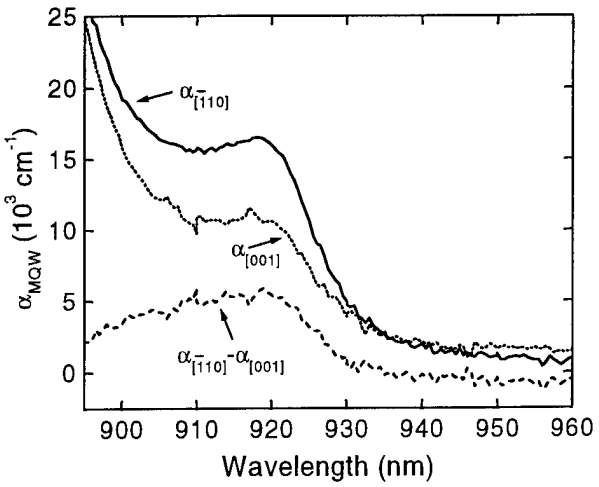

Figure 1. The absorption coefficients of the MQW region for light polarized along the two in-plane crystallographic axes (top two curves) and the dichroism (bottom line).

Kramers-Kronig transformation on the $\Delta\alpha_{MQW}$ data shown in Fig. 1. The results are shown as the open triangles in Fig. 2. For later comparison with our ellipsometric measurements, we also replot the dichroism shown in Fig. 1 as the open squares in Fig. 2.

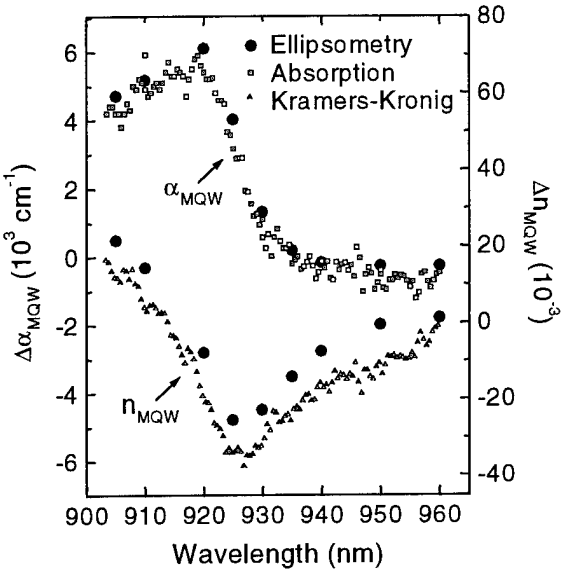

Figure 2. A comparison of the dichroism measurements obtained from absorption spectra (open squares) and the birefringence measurements derived from a Kramers-Kronig transformation of this data (open triangles) with the direct ellipsometric measurements of dichroism (top, solid dots) and birefringence (bottom, solid dots).

This birefringence and dichroism can be more directly and simultaneously determined by placing the sample between two crossed polarizers with its principal axes

oriented at 45° with respect to the polarizer axes and by subsequently measuring the transmission as a function of analyzer angle ψ. (Note that this geometry is identical to that described below for our modulator, which is shown in Figs. 5 and 6, except that the quarter wave plate is removed).

The transmission of the analyzer-polarizer pair with the sample in place is given (for small angles) by:

$$T(\psi) = (1-R)^2 \exp\left\{-(\alpha_{MQW} d + \alpha_S l)\right\} \left[\left(\psi - \frac{\Delta\alpha_{MQW} d + \Delta\alpha_S l}{4}\right)^2 + \left(\frac{\pi(\Delta n_{MQW} d + \Delta n_S l)}{\lambda}\right)^2 + X\right] \quad (1)$$

Where ψ represents the angular deviation of the analyzer from its crossed position, R is the sample reflection coefficient, λ is the wavelength, $\alpha = (\alpha_{[\bar{1}10]} + \alpha_{[001]})/2$ is the average absorption coefficient and X is the extinction coefficient of the crossed analyzer-polarizer pair. The subscripts $_{MQW}$ and $_S$ denote the MQW region and the substrate, respectively, and d and l represent their respective thicknesses. $\Delta\alpha = \alpha_{[\bar{1}10]} - \alpha_{[001]}$ denotes the dichroism and $\Delta n = n_{[\bar{1}10]} - n_{[001]}$ represents the birefringence, where n is the refractive index. Note that this equation assumes that the anisotropy (i.e. the applied voltage) and, therefore, the modulation of the polarization are constant during the transmission of the optical signal pulse, so that averaging over the pulse envelope is unnecessary [8].

Typical measurements of the transmission of the nominally-crossed analyzer-polarizer pair as the analyzer is rotated through a small angle ψ with and without the sample in place are shown in Fig. 3 for a wavelength of 925 nm and a bias voltage of 0 V. The key features to notice from inspection of Eq. (1) and Fig. 3 are that (i) the analyzer transmission is a parabolic function of the analyzer angle, (ii) the horizontal displacement of the minima determines the in-plane anisotropy in the absorption coefficient, and (iii) the vertical displacement determines the anisotropy in the refractive index.

Such measurements were systematically performed as a function of wavelength for each bias voltage of interest. Representative values for the MQW dichroism, $\Delta\alpha_{MQW}$, and birefringence, Δn_{MQW}, that are distilled from these measurements are shown in Fig. 4 for 0 and 6 V. For this figure, the effects of the substrate again have been carefully removed by performing the measurements through both the substrate and the MQW region and through the substrate alone.

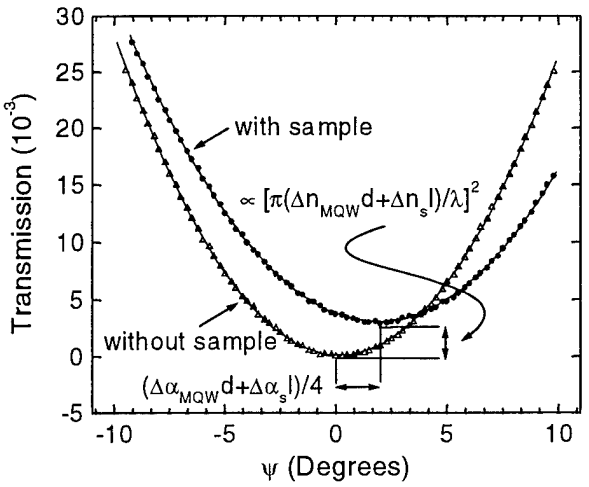

Figure 3. Transmission through two linear polarizers as a function of the final linear polarizer angle, ψ (open triangles). The same measurement with the sample placed between the linear analyzers (closed circles).

Finally, as a check on consistency and as assurance that we have successfully separated the effects of the MQWs from those of the substrate, we compared the direct ellipsometric measurements of the dichroism and birefringence with those extracted indirectly from the absorption measurements. One such comparison is shown in Fig. 2 where we have replotted $\Delta\alpha_{MQW}$ and Δn_{MQW} for 0 V from Fig. 4 as the solid circles. The overall agreement is very good, except for a slight systematic shift between the

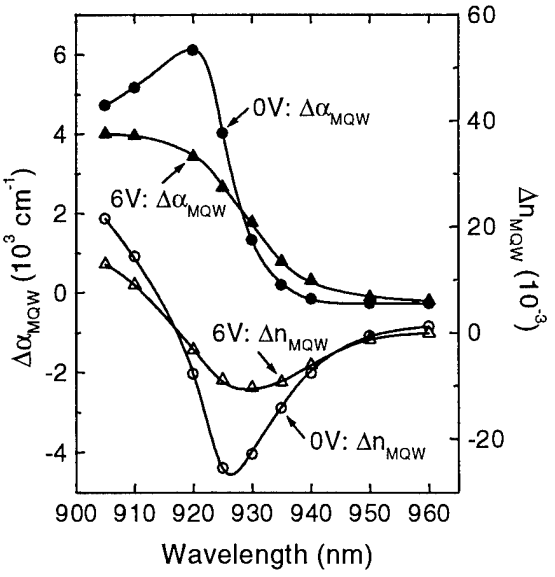

Figure 4. The two components of the complex index of refraction which relate to the optical anisotropy of the MQW region. The top two curves represent the dichroism at 0 V (solid circles) and 6 V (solid triangles) while the bottom two curves represent the birefringence at 0 V (open circles) and 6 V (open triangles).

birefringence data obtained by the two methods. We attribute this to the finite spectral window available for the numerical Kramers-Kronig transformation.

Polarization Modulator

The intrinsic anisotropy measured in the previous section can be used to fabricate a simple prototype polarization-sensitive electro-optic modulator by placing the MQW diode followed by a quarter wave plate (λ/4-plate) between two polarizers with the principal axes of the sample oriented at 45° with respect to the incident polarization, as shown in Figs. 5 and 6. In the absence of a bias voltage, the λ/4-plate and analyzer are initially oriented to reject the signal light. When a bias voltage is applied to the diode, it produces a change in the in-plane birefringence and dichroism (as discussed in the previous section), which in turn, modulates the ellipticity and the direction of polarization of the transmitted signal pulse, thus, increasing the device transmission.

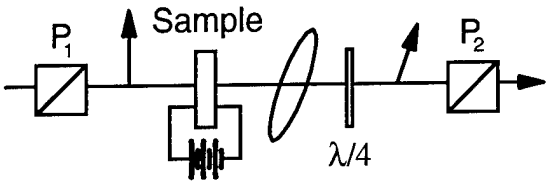

Figure 5. The geometry of a polarization modulator. P_1 and P_2 are linear polarizers, and "λ/4" represents a quarter-wave plate. The arrows and ellipse schematically represent the polarization state of light at that point in the device.

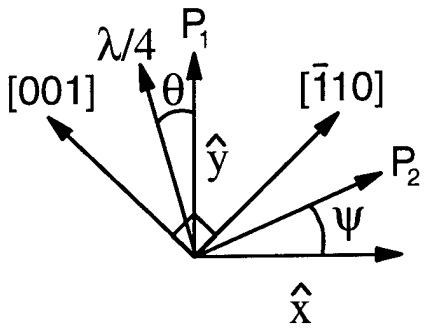

Figure 6. The nomenclature and relative alignment of the components of the polarization modulator shown in Fig. 5.

For small angular deviations of ψ and θ from their initial "off" positions, the modulator transmission can be written as:

$$T(\psi,\theta) = (1-R)^2 \exp\left\{-(\alpha_{MQW} d + \alpha_s l)\right\} \left[\left((\psi-\theta) - \frac{\pi(\Delta n_{MQW} d + \Delta n_s l)}{\lambda}\right)^2 + \left(\theta - \frac{\Delta\alpha_{MQW} d + \Delta\alpha_s l}{4}\right)^2 + X\right] \quad (2)$$

We emphasize that α_{MQW}, $\Delta\alpha_{MQW}$ and Δn_{MQW} are functions of both wavelength and voltage and that α_s, $\Delta\alpha_s$ and Δn_s are functions of wavelength, but not voltage, as discussed in the previous section. Notice that the device transmission is a parabolic function of the angle ψ (θ) for a fixed θ (ψ), bias voltage and wavelength λ. This behavior is illustrated in Fig. 7 for a wavelength of 923 nm, fixed θ and for bias voltages of 0 and 6 V.

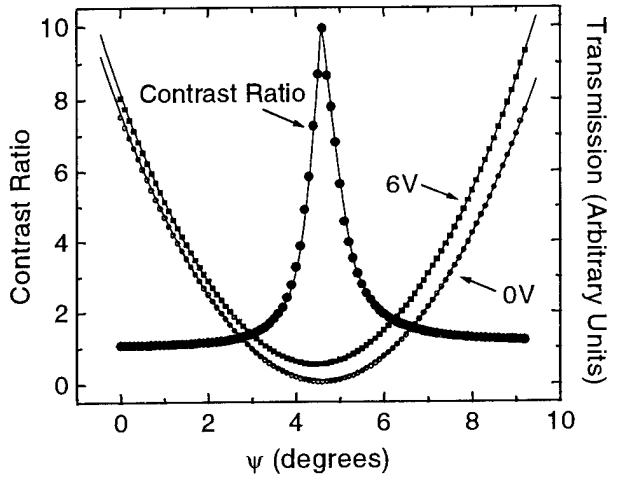

Figure 7. The measured transmission of the modulator at 923 nm in both the on (6 V) and off (0 V) states. The contrast ratio derived from these measurements is also shown.

The contrast ratio (CR), which is given by the transmission in the on-state (in this case, 6 V) divided by that in the off-state (0 V), is also shown in Fig. 7 for 923 nm and a fixed θ. Notice that the peak CR occurs very near (but not exactly at) the minimum in the transmission in the off state. This observation suggests a convenient means of (analytically and experimentally) optimizing the orientation of the λ/4-wave plate and analyzer, namely, that they should be oriented such that they minimize the transmission in the off state.

Using this condition, together with Eq. (2), we can write the contrast ratio as:

$$CR(\lambda) = \frac{\exp\left[\left(\alpha_{MQW}(0V,\lambda) - \alpha_{MQW}(6V,\lambda)\right)d\right]}{X}$$
$$\left[\left(\frac{\Delta\alpha_{MQW}(6V,\lambda)d - \Delta\alpha_{MQW}(0V,\lambda)d}{4}\right)^2 + \left(\frac{\pi(\Delta n_{MQW}(6V,\lambda)d - \Delta n_{MQW}(0V,\lambda)d}{\lambda}\right)^2 + X\right] \quad (3)$$

The first term in Eq. (3) gives the contribution of the dichroism, the second the contribution of the birefringence, and the third represents the contribution of the amplitude modulation of the average absorption coefficient as a function of voltage. The latter produces no change in the polarization state.

The measured values for $\Delta\alpha_{MQW}$ and Δn_{MQW} as a function of wavelength and voltage from the ellipsometric measurements described in the previous section can now be used in Eq. (3) to predictably optimize the operating wavelength. This procedure is illustrated in Fig. 8, where the contrast ratio has been calculated as a function of wavelength using the dichroism and birefringence shown in Fig. 4. The individual contributions of the dichroism, birefringence and amplitude modulation are also plotted. The contrast ratio is strongly peaked with a maximum value of ~10:1 predicted near 923 nm and a width of ~10 nm (FWHM). It is also clear from this figure that the contributions of amplitude modulation (i.e., the third term in Eq. (3)) to the contrast ratio are small and that the polarization modulation terms (i.e., the changes in the dichroism and birefringence) dominate. In fact, at the peak wavelength, dichroic effects (polarization rotation) dominate those of birefringence.

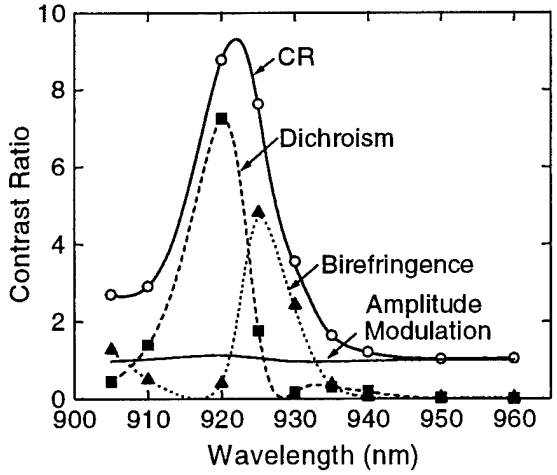

Figure 8. The contrast ratio calculated from the ellipsometric measurements shown in Fig. 4. The individual contributions from dichroism, birefringence and amplitude modulation to the contrast ratio are also shown.

This modulator can be tuned by simply rotating the analyzer slightly, as illustrated in Fig. 9. This figure shows the contrast ratio as a function of wavelength for several measured fixed analyzer orientations. Notice that an unoptimized device, which contains only 50 6-nm-wide wells and is operated at 6 V is capable of maintaining a contrast of >4:1 over a range of >10 nm. Since the excitonic resonance shifts at a rate of ~1 nm/3.5°C, this corresponds to a useful operating temperature range of ~35°C. In effect, this figure illustrates one of the potentially useful characteristics of polarization modulators. Namely, that the broad exciton in the present sample has effectively allowed us to trade contrast ratio for tunability or, equivalently, for insensitivity to changes in ambient temperature.

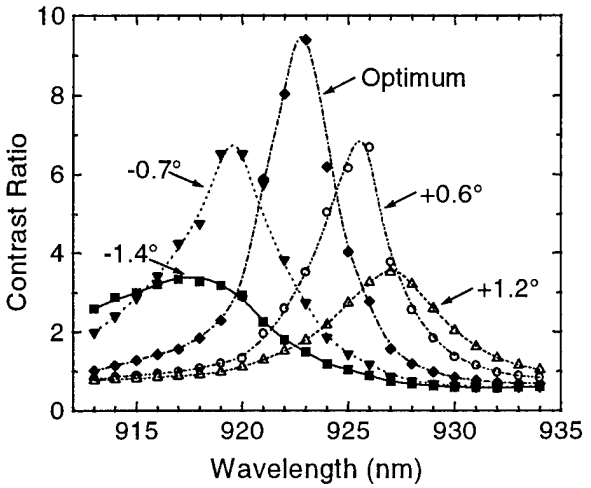

Figure 9. The measured contrast ratio as a function of wavelength for different values of ψ , the angle of the final linear analyzer. At $\psi = 0$, P_2 is optimized to give the largest contrast ratio possible. The orientation of the quarter-wave plate was fixed throughout at the value found to give the maximum contrast ratio at 923 nm.

Discussion

In summary, we have measured the birefringence and dichroism of a strained [110]-oriented InGaAs/GaAs p-i(MQW)-n diode as a function of wavelength and voltage. This information was then used to predictably evaluate the performance of this device when used as a polarization-sensitive modulator. The tunability (10 nm), optical bandwidth (4 nm), switching voltage (6 V) and temperature range (35 C) of the current device are impressive; however, the contrast ratio (10:1) is disappointing and the insertion loss (~33 dB) is daunting. This relatively low contrast ratio and the high insertion loss are not typical, however, but are primarily the result of the thin quantum well region and broad broad excitonic linewidth

of the unoptimized sample that happened to be available for this demonstration. By simply increasing the number of quantum wells, while continuing to use the current material, we estimate that the contrast ratio can be increased to >1000:1 and the transmission increased to ~1% while maintaining the current optical bandwidth, tunability, and operating temperature range, but at the expense of an increased switching voltage.

The use of MQW material with narrower excitonic features should further improve both the contrast ratio and throughput, but at the expense of optical bandwidth, tunability and operating temperature range.

Generically, polarization-sensitive quantum-confined Stark-effect (QCSE) modulators should be capable of higher contrast ratios than the equivalent amplitude modulators, but they will have a higher insertion loss. A disadvantage of the polarization modulators described here is that they require growth in an unconventional direction. Nevertheless, they have an advantage over uniaxially-strained polarization-rotation modulators, which require bonding to a substrate and subsequent epitaxial lift off, in that they require less post-growth processing. Consequently, as a class, QCSE polarization modulators will be most useful for applications that require high dynamic range and can tolerate large insertion loss.

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Fast response PROM using GaAs single crystal

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Abstract

A new Pockels Readout Optical Modulator (PROM) device using a GaAs single crystal (GaAs-PROM) has been developed for high speed operation. Its fundamental properties were experimentally investigated and the operational technique was given by them. The GaAs-PROM was driven by a sinusoidal alternating high voltage and its high sensitivity and high frame rate (>500 Hz) were experimentally confirmed . This is a extremely high compared with a conventional PROM

Key Words: Spatial light modulator, Pockels readout optical modulator, GaAs, high speed operation

1.Introduction

The spatial light modulator (SLM) is one of the essential components in optical computing and optical image processing systems. The optical addressing SLM has the advantages of optical parallelism in both input and output plane and so is used for wavelength converter and/or incoherent image to coherent image converter. The main performance requests on SLM are higher sensitivity, higher contrast ratio, higher spatial resolution, and faster response time. Especially, the sensitivity is the most important factor for high speed operation. A low sensitivity device needs high power write-in and erasing light sources. In this paper, we propose a new Pockels readout optical modulator (PROM) device using a GaAs crystal plate (GaAs-PROM) for high speed operation, and its characteristics and an operating system are investigated.

The PROM device is well known as the SLM for optical processing system [1-3]. This device consists of a photoconductive and electrooptic (Pockels effect) crystal plate covered with insulating films and transparent electrodes. Usually, $Bi_{12}SiO_{20}$ (BSO) crystal is used as the photoconductive and electrooptic crystal, and the device is called as BSO-PROM. Comparing to consumer-product spatial light modulator such as liquid crystal light valves, the PROM device has simple structure, faster response time of electrooptical effect, and higher contrast ratio (larger than 1000:1). However, the BSO-PROM has not so high sensitivity (several tens μ J/cm^2) and it is sensitive only to blue to green radiations. These facts are main reasons to prevent realization of high speed optical systems using the BSO-PROM.

The GaAs crystal is the attractive material because of its high carriers (electrons and holes) mobilities, wideband sensitivity (from visible to near infrared radiation), and large absorption coefficient. Consequently it has been used as a photoreceptor of the liquid crystal light valve [4-5]. When we make a plan to realize a PROM device with fast response, we need a photoconductive material with high carrier mobility and large absorption coefficient for a write-in light. The GaAs single crystal has both electrooptical and photoconductive effect and is considered useful material for the PROM device. Additionally, the GaAs has no optical activity and circular birefringence, although BSO crystal has those troublesome characteristics. Also, it is easy to make uniform plates with large sizes.

Using the Pockels effect of a crystal such as PROM devices, an applied voltage of several kilo volts is necessary for useful operations. Therefore, in the conventional use of the PROM device, high speed operations of the devices need high speed ON/OFF of the

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high voltage. It is not so easy to perform ON/OFF of the high voltage with a high speed. To remove the difficulty, in this paper, GaAs-PROM was driven by externally applying a sinusoidal alternating high voltage. Needless to say, the application of the ac voltage is easier than the ON/OFF operation in a high voltage at a high frequency.

In the following, we first describe the device structure of GaAs-PROM and its characteristics of sensitivity. Next, the SLM operation system is investigated and its high sensitivity and frame rate is experimentally confirmed.

2. Device fabrication and basic properties

The structure of GaAs-PROM is shown in Fig. 1. A thin plate with (001) surface was cut out from an undoped GaAs single crystal ingot grown by Liquid Encapsulated Czochralski (LEC) method. The dark resistivity of the plate was 4×10^{7} $\Omega \cdot$ cm. Thin glass plates were used as insulators. Each layer was bonded with lens bond. In this work, we prepared two kinds of devices (Device-1 and Device-2): the thicknesses of GaAs and glass plates were 400 μ m and 10 μ m in Device-1, and 600 μ m and 100 μ m in Device-2, respectively.

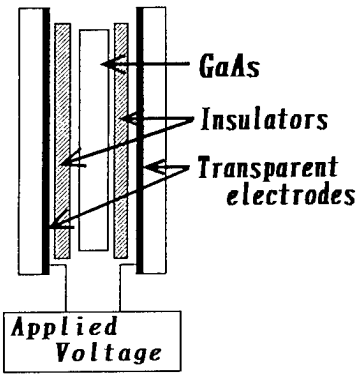


Figure 1. Structure of GaAs-PROM.

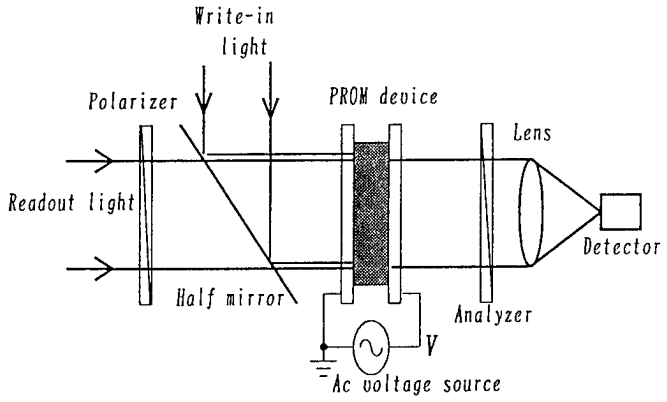
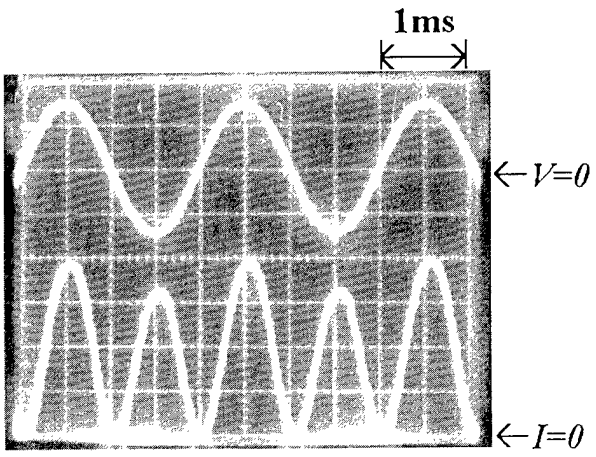


Figure 2. Experimental setup to investigate basic properties of GaAs-PROM.

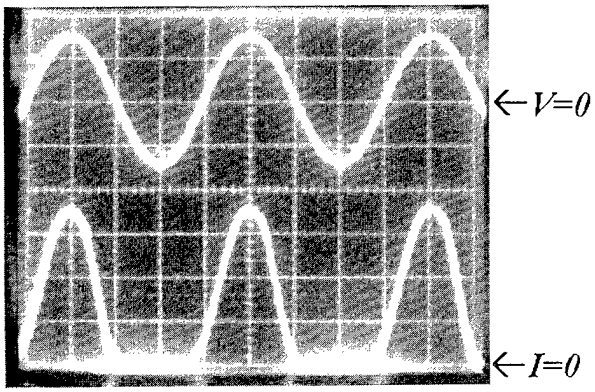
In this section, only the experimental results in Device-1 were mainly described, because the similar properties were also recognized in Device-2.

The basic properties of GaAs-PROM were investigated by an experimental setup shown in Fig. 2. A uniform write-in light in visible region was incident on the device by a half mirror. The recorded image (a uniform image) was read out by a near infrared light. The write-in and the readout lights were incident on the device from the same side. GaAs crystal has the symmetry of the point group 43m and the maximum retardation due to the Pockels effect is given in the readout light with linearly polarized light along the axis <100> or <010>. Then, the polarization of the readout light was set along the axis <100> or <010> and the analyzer was set perpendicular to the polarizer. The transparent electrode of the device in this incident side was earthed and an ac high voltages driving the device was supplied from a function generator through a high voltage power amplifier. The intensity of the readout light transmitting the device was measured by a photodetector through an analyser and a lens. The readout light was provided by a laser diode (LD) with the lasing wavelength of 980 nm. In this experiment, a filter isolating only the readout light was not necessary because the visible write-in light (its wavelength was over the band gap energy: 1.43 eV) was mostly absorbed within the surface layer of several μ m thick in GaAs plate. This absorption property is associated with high sensitivity over a wider region of the wavelength comparing to that of the BSO-PROM.

First, the basic properties were investigated under no write-in light and continuous illumination of the readout light. Under the conditions, the readout light was modulated by the Pockels effect of GaAS crystal plate due to only the externally applied electric field. Then the output light intensity from the device was modulated with the twice frequency of applied ac voltage. An example of time variations in the output light intensities are shown in Fig. 3(a) together with the waveform of applied ac voltage V. The result in the figure was obtained using the readout light with intensity of 940 μ W/cm ^{2} and the ac voltage with the amplitude of 3 kV and frequency of 500 Hz. It is seen that the output light intensity was modulated with the twice frequency of the ac voltage. However, the peak height of output light intensity when V>0 is slightly different from that when V<0. Theoretically, the two peaks should be similarly independent of the direction of



(a)



(b)

Figure 3. Observed signals of the Pockels effect in GaAs-PROM. These signals were observed under the following conditions. Externally applied ac voltage; amplitude of 3 kV at 500 Hz, uniform readout light; wavelength of 980 nm and intensity of 940 μ W/cm ^{2}, and uniform write-in light; wavelength of 780 nm and intensity of 2.2 mW/cm ^{2}, respectively. Upper and lower signals in each figure show the waveforms of applied ac voltage and the output signal, respectively. The signals in (a) and (b) were observed under no and continuous illuminations of the write-in light, respectively.

the electric field in GaAs crystal because the crystal is ideally optically isotropic. The actual GaAs crystal or wafer cut out from an ingot grown by the LEC method has two dimensional distributions of a small amount of birefringence [6]. Unfortunately, it seems that the GsAs plate in Device-1 had a small amount of birefringence.

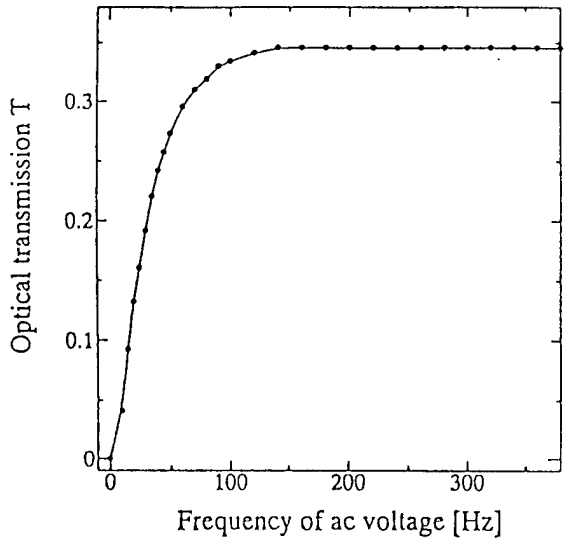


Figure 4. →Dependence of the Pockels effect in Device-1 on frequency of externally applied ac voltage. The amplitude of ac voltages were kept to 3 kV, and the magnitudes of the Pockels effect were represented by the optical transmission T of the device.

Consequently, the extinction ratio of this device became approximately 1000 ~ 500:1, on the contrary that of BSO-PROM is over 10^4:1, and the difference of two peaks might be caused by the birefringence. To realize a high contrast GaAs-PROM, we have to choose a GaAs crystal plate with very small birefringence. From the results of the Pockels effect in V<0, the half-wave voltage of Device-1 was determined as 7.5 kV. The half-wave voltage of Device-2 was also determined as 12.4 kV from the similar experiment.

The dependence of the Pockels effect on the frequency of the applied ac voltage was measured in Device-1. The results are shown in Fig. 4 as the variation of optical transmission T of the device versus the frequency of ac voltage, where the amplitude of external voltage was constantly kept to 3 kV. The transmission T was defined as the ratio of the peak value of output intensity to the output intensity when V=0 and the analyzer was set parallel to the polarizer. The transmission T increased as the frequency of ac voltage increased and saturated at the frequencies larger than 100 Hz. It is seen from the results that the conductivity of the GaAs plate can be ignored in the frequencies larger than around 100 Hz at V=3 kV and the GaAs-PROM can be considered as the series circuit of the capasiters which are made from GaAs plate and insulators, respectively. The time variation of the output light intensity coincides with the applied ac voltage in that situation. The electro-static relaxation time of Device-1 was estimated as 6.5 ms at V=3 kV from the results shown in Fig. 4.

Next, the sensitivity characteristics of GaAs-PROM for the write-in light, (1) asymmetric characteristics due to the mutual relations between the incident direction of write-in light and the direction of applied electric field and (2) the dependence of sensitivity on the wavelength of write-in light, were experimentally investigated.

2.1 Asymmetric characteristics of sensitivity

The write-in light generates photo carriers (electrons and holes), the carriers migrate in the GaAs crystal along the electric field and consequently negate the electric field in the crystal. The Pockels effect in the crystal plate decreases as the write-in light intensity increases. Then, the GaAs-PROM converts an input image to its negative image. Here, the characteristics relating to the intensity and the incident direction of write-in light are investigated.

The Device-1 was continuously illuminated by the uniform readout light (intensity: 940 μ W/cm ^{2} and wavelength: 980 nm) and a uniform write-in light (wavelength: 780 nm and various intensity levels) at the same time and driven by applying ac voltage with the amplitude of 3 kV and the frequency of 500 Hz. The readout signals were observed on various intensity levels of the write-in light.

An example of the readout signals is shown in Fig. 3(b). The readout signal decayed strongly and hardly when V<0 and V>0, respectively, comparing the readout signals obtained by no write-in light (Fig. 3(a)). The write-in light and the electric field due to the applied ac field were codirectional when V<0, and they were contradirectional when V>0. In the following, we refer the former and the latter to the codirectional and the contradirectional write-ins, respectively. The variations of peak values of the readout signals versus the write-in light intensity were summarized in Fig. 5, for the codirectional and the contradirectional write-ins. The codirectional write-in is high sensitive but the contradirectional write-in has almost no sensitivity. That is, the sensitivity of GaAs-PROM is asymmetric.

The write-in light is almost absorbed in the thin surface layer with thickness of about 4 μ m. The photo carriers are generated in the thin layer on the side where the write-in light comes incident and move along the electric field in the crystal. The holes and electrons become the effective carriers for the codirectional and the contradirectional write-ins, respectively. It is known that in low electric field, the mobilities of the electron and the hole in the GaAs are around 6000 cm ^{2} /(V · s) and 400 cm ^{2} /(V · s), respectively. From this fact, it is expected that the contradirectional write-in becomes more sensitive than the codirectional write-in. However, the experimental results were contrary to the expectation. The influence of

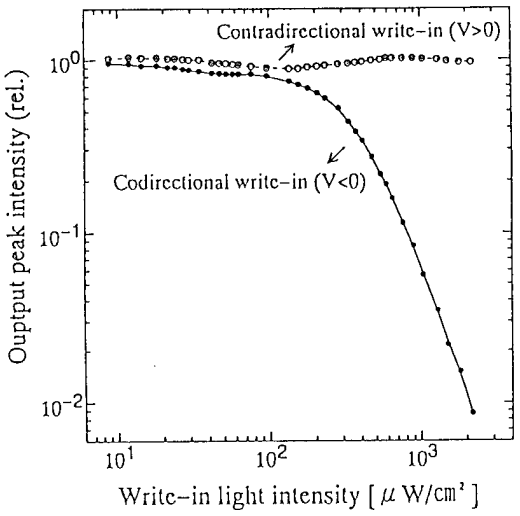


Figure 5. Asymmetric characteristics of sensitivity in Device-1 driven by a high ac voltage (3 kV). The sensitivity curves for the codirectional write-in and the contradirectional write-in versus there intensities are plotted by marks ● (solid curve) and ○ (dashed curve), respectively. The sensitivities were represented by the peak values of the output signals and the peak values are normalized by that for no write-in light intensity.

the electrons seems to cause this contrary results. In the semiconductors, the electron's mobility has a negative differential in the electric field larger than the threshold field. Those electrons are called as hot electrons and the threshold value of electric field is around 3 kV/cm in GaAs crystal [7-8]. The maximum electric field strength in GaAs crystal was estimated as 55 kV/cm when the applied ac voltage became 3 kV in the experiments. In such strong electric field, it seems that the drift velocity of holes is larger than that of electrons. To confirm these facts, the experiment in which variation of the readout signal versus the applied ac voltage was observed at the write-in light intensity of 400 μ W/cm ^{2} . The peak values of the signals in both cases of the codirectional and the contradirectional write-ins became almost same at the maximum electric field strength of around 25 kV/cm, that was made by V $\fallingdotseq$ 1.5 kV, and at V<1.5 kV the peak value in the latter case became smaller than the former, that is, the contradirectional write-in became more sensitive than the codirectional write-in. These experimental results indicate that the holes become effective carriers when V>1.5 kV and the codirectional write-in is useful to realize the high sensitive and high contrast when the GaAs-PROM is derived by a higher ac voltage.

2.2 Dependence of sensitivity on write-in light wavelength

The characteristics of Device-1 for the wavelength of

write-in light were investigated by the similar experimental setup as shown in Fig. 2. In the experiments, the output signals were read out using a uniform radiation (wavelength: 1300 nm and intensity: 55 μ W/cm ^{2}) from an incandescent lamp through an interference filter. The write-in lights were provided by using lasers (wavelengths: 780 nm, 980 nm, and 1064 nm) and LEDs (wavelength: 660 nm, 850 nm, and 950nm), and their intensities were kept a constant (940 μ W/cm ^{2}). The applied ac voltage was 3kV, and the device was always illuminated by both the readout and the write-in lights.

The variations of peak values of the output signals versus the wavelength of write-in light are shown in Fig. 6, where the peak values are normalized by that for no write-in light. When the write-in light wavelength is longer than 900 nm, the sensitivities for both the codirectional and the contradirectional write-ins have almost same values and became lower with the increase of the wavelength. But when the wavelength is shorter than the band gap of GaAs (around 850 nm), the sensitivities for the codirectional write-in and the contradirectional write-in became extremely different because of just described above. The sensitivity for the contradirectional write-in became highest around 900 nm. This might be because of that the absorption layer of the write-in light became moderately thick and the separation efficiency of holes and electrons became higher consequently. Conversely, the sensitivity for the codirectional write-in became higher as the wavelength decreased. It is seen that the highest sensitivity is attained by using the write-in light with wavelength of around 820 nm.

From the results in the above, it is known that the GaAs-PROM is (1) high sensitive to the codirectional write-in light but (2) hardly sensitive to the contradirectional write-in light, and (3) useful to transform a visible light image to its negative image in the near infrared region.

3. SLM operation system

From the above results, in order to organize a higher quality SLM using a GaAs-PROM, the following items were used for the SLM operation system, (1) the codirectional write-in should be introduced, (2) the recorded image should be read out by a short pulse illumination of infrared light at the peak of the applied ac voltage in V<0 because the effect of the write-in light on the contrast of the readout signals becomes maximum at the peak in V<0 as seen from the results in the previous section, and (3) it is desired that the erasing light prepares a uniform electric field in the GaAs crystal plate just before the write-in process. The third item is satisfied by introducing the erasing light as follows. From the characteristics shown in Fig. 5, GaAs-PROM is almost insensitive to a visible incident light in the sense of the contradirectional write-in, that is, in the write-in process the visible light is only useful in the sense of the codirectional write-in and is almost innocent in the sense of the contradirectional write-in. Then, a visible light illuminating the device contradirectional to the write-in light usefully acts as erasing light.

An optical setup for SLM is schematically shown in Fig. 7. The write-in light is imaged on GaAS-PROM by a lens L $_1$, the readout light from the PROM is also imaged on a CCD camera by a lens L $_2$, an erasing light is newly introduced behind the PROM, and the others are the same as Fig. 2. As a result of the following

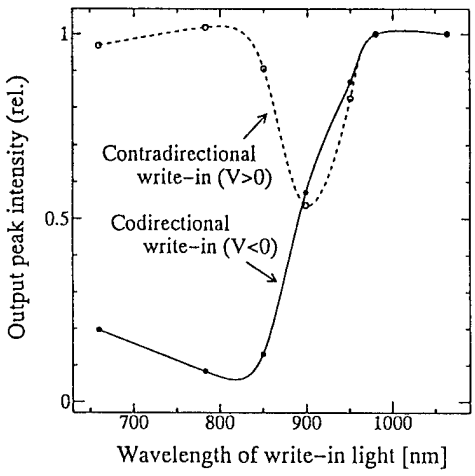


Figure 6. Variations of output signals versus wavelength of write-in light in Device-1.

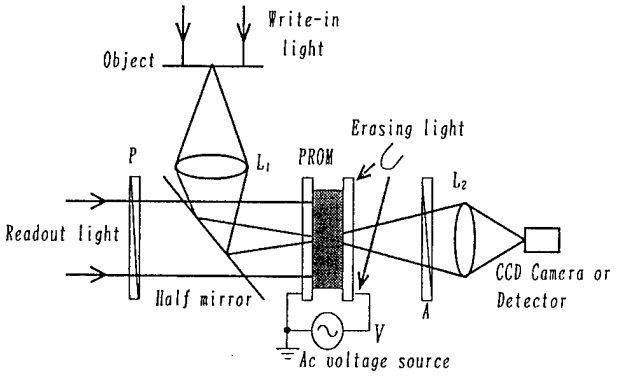


Figure 7. Optical setup for SLM operation. A, analyzer; P, polarizer; L $_1$ and L $_2$, lenses.

experiments, in an operation cycle of GaAS-PROM, the erasing of the image recorded in its previous cycle is performed in the first half period of the applied ac voltage (when V>0), a new image is recorded in the third quarter period (when V<0), and the recorded image is readout just after the third quarter period (at the negative peak of ac voltage) by a pulse of readout light, respectively.

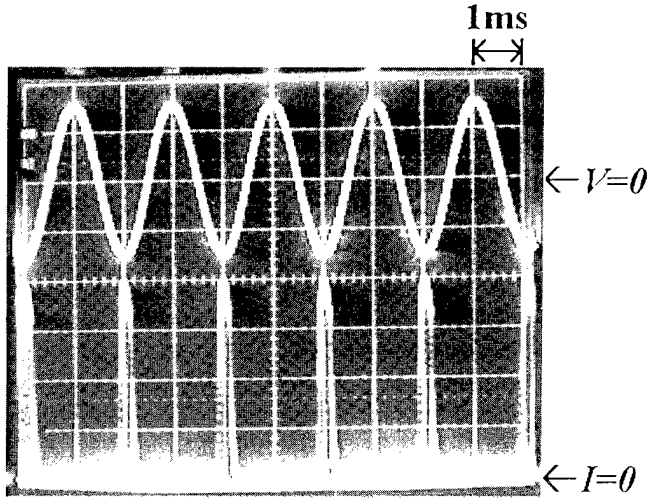
In the following experiments, a pulse light from a LD (wavelength: 980 nm) was used as the readout light and synchronized to the negative peak of ac voltage. The pulse width was 0.2 ms and its peak intensity was 9.4 mW/cm^2, which was needed to obtain enough bright readout images using the CCD TV camera. The pulse light had weaken the Pockels effect in GaAs because the light has weakly absorbed by GaAs and the pulse had large peak intensity. But this fact did not affect the investigations of erasing, recording, and readout characteristics in the SLM system.

3.1 Effects of erasing light and frame rate

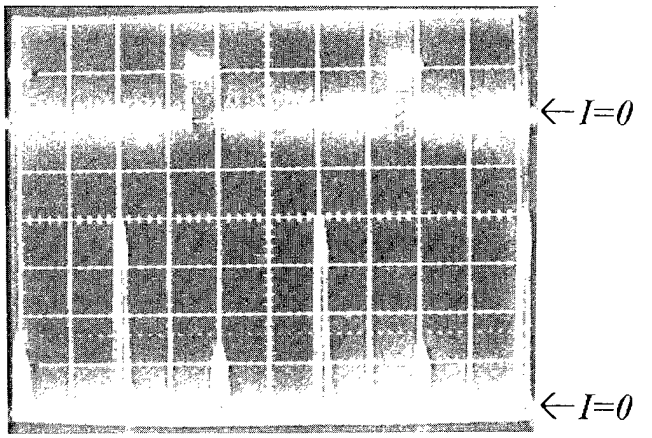
An incoherent uniform erasing light (wavelength: 660 nm from LED) continuously illuminated on the GaAs-PROM from its rear side. It provided faster erasing of the recorded image. The waveforms of readout signals shown in the Fig. 8(a) were obtained from Device-1 with no write-in light and the continuous illumination of the erasing light (intensity: 1.3 mW/cm^2), where the amplitude of ac voltage was 3kV (at frequency of 500 Hz).

The erasing light was mostly absorbed within several μ m thick and generated electrons and holes near the rear side surface of GaAs plate. The effects of the continuous erasing light are described as follows. When V>0 the light erases the electric field distribution in GaAs plate because the holes become the effective carrier corresponding the codirectional write-in. When V<0 the erasing light corresponds to the contradirectional write-in and the photocarriers do not erase the electric field so much because the electrons near the rear surface must move to near the front surface in order to effectively erase the electric field.

The erasing light must uniformize the electric field in GaAs plate and erase the recorded image within the half period in V>0. To confirm whether the requirement is satisfied or not, a uniform write-in light (wavelength: 850 nm from LED) was illuminated only at the third quarter period in every alternate periods of the ac voltage, the uniform erasing light was also continuously illuminated, and the uniform images recorded in Device-1 were read out every periods of ac voltage. The readout signals are shown in Fig. 8(b). The top signal in the figure shows the time variation of the write-in light intensity: the pulse signals with the third quarter period appeared only in



(a)



(b)

Figure 8. Readout signals from Device-1 with (a) no write-in light and (b) synchronously intermittent write-in light. Upper signals in (a) and (b) show waveforms of externally applied ac voltage (3 Kv) and write-in light, respectively. Lower signals in (a) and (b) show readout signals.

every alternate periods of ac voltage. The bottom signal shows the readout signal intensity from Device-1. The readout signal intensities in the periods with no write-in light recovered to the same as those shown the bottom in Fig. 8(a). On the other hand, due to the effect of the write-in light, the readout signal intensities just after the write-in light pulse became lower than those in the periods with no write-in light. Thus, it has been confirmed that the recorded images can be completely erased in the half period in V>0. Furthermore, the above experimental results suggest that the GaAs-PROM can be operated with a larger cycle than 500 Hz.

3.2 Dependence of sensitivity on write-in light intensity

First, it is shown by the following experiments that the continuous illumination of the write-in light is accepted. The write-in light pulses (wavelength: 850 nm and peak intensity: 940 μ W/cm ^{2}) with two kinds of width were separately illuminated on Device-1 delaying their starting times t_w from the starting time t_n of the negative ac voltage, under continuous illumination of the erasing light. The widths of the write-in pulses were the quarter and the half periods of the applied ac voltage, respectively. The variations of the readout signal intensities versus the delay time of t_w from t_n were measured and are shown in Fig. 9, where the delay times are expressed using the phase differences. From the results in the figure, it is seen that (1) the readout signal intensity monotonically decreased as the increase of the write-in light energy exposed on the device between the time t_n and the starting time t_r of the readout light pulse, (2) the write-in lights before t_n and after t_r hardly affected the readout signal intensity, and (3) the recorded signal fairly decayed from the end time of the write-in pulse until the time t_r . Then the continuous illumination of the write-in light realizes the efficient write-in and simplifies the control of SLM system.

The sensitivity curves of GaAs-PROMs were measured under the continuous illuminations of the erasing light and the write-in lights (wavelength: 780 nm and various intensities) from a LD by applying ac voltages with amplitude of 3 kV and 6 kV to Device-1 and Device-2, respectively. The variations of the readout signal intensities versus the write-in light intensity are shown in Fig. 10, where the vertical axis is normalized by the maximum output signal intensity obtained with zero intensity of the write-in light. The experimental results when Device-1 was driven by ac voltages with 500 Hz and 250 Hz are shown by the marks ● and ○ , respectively, and the results when Device-2 driven with ac voltage with 500 Hz are shown by the mark ■ . When the frequency of ac voltage was 500 Hz, the write-in light of intensities 400 and 130 μ W/cm ^{2} were required to reduce the output signal intensity to 1/e for Device-1 and Device-2, respectively. Device-2 with thicker GaAs crystal plate became more sensitive. The effective exposures corresponding these write-in light are 200 nJ/cm ^{2} and 65 nJ/cm ^{2} , respectively, and these devices are very high sensitive. When Device-1 was driven by the ac voltage of 250 Hz, the write-in light intensity of 230 μ W/cm ^{2} was required to reduce the output signal intensity to 1/e. This required write-in light intensity became around a half of that at the frequency of 500 Hz, because the effective exposure time of the write-in light became the two times.

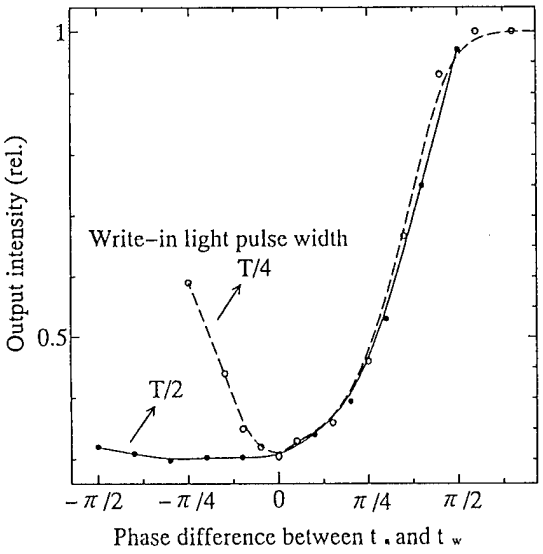


Figure 9. The sensitivity dependence of the phase difference between starting time t_n of negative ac voltage and starting time t_w of write-in pulse. The zero phase difference corresponded that the write-in light pulse started at the time t_n . The experimental results for the write-in light pulses with widths of T/2 and T/4 are shown by (● and solid curve) and (○ and dashed curve), respectively. Vertical axis was normalized by the peak intensity with no write-in light.

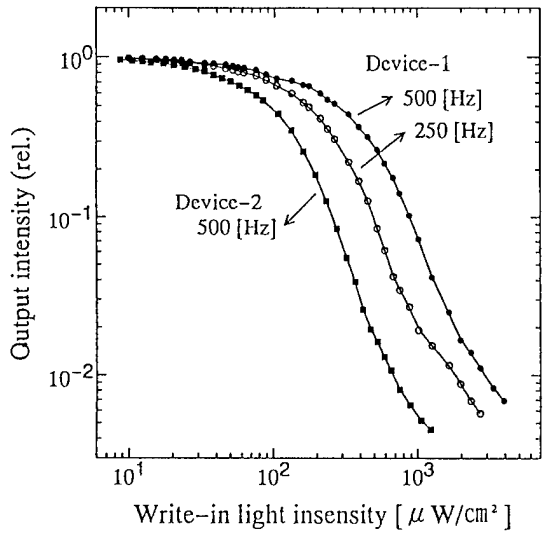


Figure 10. Sensitivity curve of GaAs-PROM versus write-in light intensity under continuous illumination of the erasing and the write-in lights. The experimental results of Device-1 driven by ac voltages of 3 kV with frequency of 500 Hz and 250 Hz are shown by marks ● and ○ , respectively, and the results of Device-2 driven by ac voltage of 6 kV with frequency of 500 Hz are shown by mark ■ . Vertical axis was normalized by the peak intensity with no write-in light.

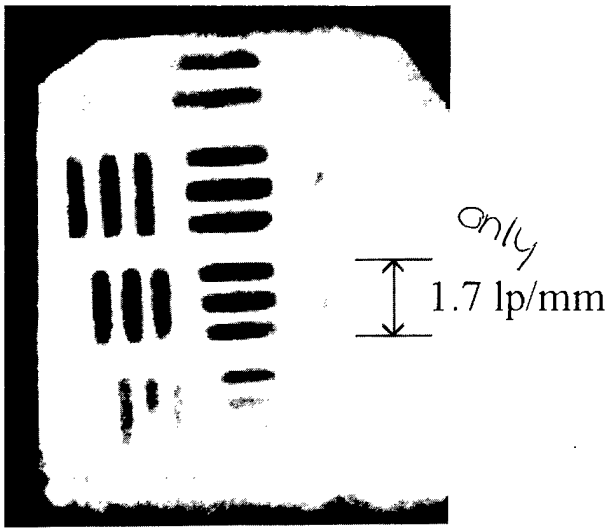


Figure 11. Example of readout images from Device-1.

In the experiments, we obtained the maximum contrast ratio of lager than 200:1 in the devices. The maximum contrast ratio would be improved by removing the birefringence in GaAs plate.

3.3 Resolution of readout image

An image of the US air force resolution test chart was recorded in Device-1 and Device-2, and read out by the pulse light described above. The applied ac voltage was 3 kV at 500 Hz and the write-in light (wavelength: 780 nm) was continuously illuminated. An example of the readout images from Device-1 is shown in Fig. 11. The image was taken by a CCD TV camera without an infrared filter and was a result of summarizing up about eight images sequentially read out. The limiting resolutions of readout images were about 10 lp/mm in both Device-1 and Deice-2. The value of resolution is smaller than that in BSO-PROM. This weak point will be recovered by the possibility of a GaAs-PROM with a large useful image area. The modulation transfer characteristics will be searched in near future.

4. Conclusion

A PROM device using GaAs for high speed operation was proposed, and following properties were experimentally confirmed: a higher frame rate operation (over than 500 Hz), higher sensitivity (required exposure smaller than 200 nJ/cm^2), and a limiting spatial resolution (about 10 lp/mm). In addition, the GaAs-PROM becomes equivalent to a simple capacitively coupled structure and is enable to construct inexpensive and compact size optical systems because we can use LDs and/or LEDs as all light sources in the systems. If a LD lasing at 1300 nm for a readout light source and GaAs plate with no birefringence were used, a higher performance system with higher contrast ratio of the readout image would be realized.

The detailed mechanism which limits the frame rate in the GaAs-PROM could not be investigated because of complexity of the influence of carrier mobility in GaAs in a strong electric field. But, this problem is the intrinsic problem in the GaAs-PROM requiring a strong electric field. GaAs has a negative differential mobility and this is not always the best semiconductor material for making a PROM device. So, we will further investigate other semiconductor materials, such as InP, which have the larger threshold than that of GaAs in the negative differential mobility.

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Optical Response of Polymer Dispersed Liquid Crystals to the Frequency of the Applied Voltage

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Abstract

We study the light transmittance of PDLCs a function of applied field shape and frequency. We present some experimental result and a mathematical model able to explain the device behaviour as a consequence of liquid crystal dielectric permittivity dependence on the applied voltage frequency.

Key Words

Optoelectronics, Liquid crystal devices

Introduction

A Polymer Dispersed Liquid Crystal (PDLC) is a material made by the dispersion of liquid crystal microdroplets in a polymeric binder [1-2]. Droplet size is close to visible light wavelength. Since they behave as randomly oriented anisotropic spheres they produce strong light scattering so that the sample is opaque translucent [3-5]. Light scattering can be controlled by changing the droplet effective refractive index mismatch to the surrounding polymer. The simplest and more used way to accomplish this result is the application of an external, low frequency, electric field [6]. PDLC may be used for several purposes, from large scale flexible displays to windows with controlled transparency or thermal sensors. We have recently presented detailed experimental and theoretical studies of the behavior of a PDLC sample when a light beam impinges on it [7-10]. In this paper we devote some attention to the study of the influence of the dependence of the liquid crystal dielectric permittivity response to the frequency of the applied voltage on the electro-optical behavior of the PDLC, and in particular on its transmittance.. To this aim we use a mathematical model assuming the liquid crystal dielectric permittivities $\varepsilon_{\parallel}$ and $\varepsilon_{\perp}$ to be the most important parameters for the applied field frequency dependence of light transmittance. Theoretical results show a sudden decrease of the transmitted intensity increasing the frequency of the applied voltage. We present also preliminary experimental results confirming this behavior.

The Model

In the framework of the Pallfy-Muhoray theory [11] we describe the PDLC sample by means of three order parameters: the *local order parameter*

$$S = \left\langle P_2\left(\hat{n}\cdot\hat{l}\right)\right\rangle,$$

the *droplet order parameter*

$$S_d = \left\langle P_2\left(\hat{N}_d\cdot\hat{n}\right)\right\rangle_{droplet},$$

and the *sample order* parameter

$$S_s = \left\langle P_2\left(\hat{E}\cdot\hat{N}_d\right)\right\rangle_{sample},$$

where P_2 is the second order Legendre polynomial $\hat{l}$ is the molecular axis $\hat{n}$ is the nematic director $\hat{N}_d$ is the droplet director (i.e. the mean value of $\hat{n}$ inside each droplet) $\hat{E}$ is the direction of the

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applied electric field and the <> parentheses denotes the spatial average.

The *local order parameter*, i.e. the usual scalar order parameter S is assumed to be unaffected by droplet configuration and by the external electric field. For the temperature dependence, from the Maier and Saupe theory [12] we have:

$$S = (1 - 0.98\theta)^{0.22}$$

where Θ is an universal function of the reduced temperature:

$$\theta = TV^2 / T_{NI}V_{NI}^2,$$

T is the temperature, V is the volume and T_{NI} and V_{NI} are their values at the Nematic-Isotropic transition.

The *droplet order parameter* S_d takes into account the liquid crystal orientation with respect to the droplet's symmetry axis, being $S_d = 1$ when all the molecules are parallel to $\hat{N}_d$ and $S_d = 0$ for a random distribution (isotropic droplet). It describes the droplet configuration and allows to compute the droplet ordinary and extraordinary refractive indices:

$$n_{do} = \frac{2}{\pi} n_o \, \mathrm{F}\left(\frac{\pi}{2}, \frac{1}{n_e}\sqrt{\frac{2}{3}\left(n_e^2 - n_o^2\right)\left(1 - S_d\right)}\right)$$

$$n_{de} = \frac{n_o n_e}{\sqrt{\frac{2}{3}\left(n_o^2 - n_e^2\right)S_d + \frac{1}{3}\left(n_o^2 + 2n_e^2\right)}}.$$

Where F(,) is the complete elliptic integral of the first kind and n_e and n_o are the extraordinary and ordinary liquid crystal refractive indices respectively. For the sake of simplicity, in this paper we assume a constant value for the droplet order parameter (S_d=0.7); a more detailed study can be found in [8].

The *sample order parameter* S_s describes the droplet reorientation due to the external field, and is computed by the implicit relations:

$$S_s = \frac{1}{4} + \frac{3\left(e_a^2 + 1\right)}{16e_a^2} + \frac{3\left(3e_a^2 + 1\right)\left(e_a^2 + 1\right)}{32e_a^3} \ln\left|\frac{e_a + 1}{e_a - 1}\right|$$

$$e_a\left(S_s\right) = E\sqrt{\frac{3v_{lc}\varepsilon_p}{\varepsilon_{lc} + 2\varepsilon_p - v_{lc}\left(\varepsilon_{lc} - \varepsilon_p\right)}\frac{\varepsilon_{\parallel} - \varepsilon_{\perp}}{K_d}}$$

$$\varepsilon_{lc}\left(S_s\right) = \varepsilon_{\perp} + \frac{1}{3}\left(1 + 2SS_dS_s\right)\left(\varepsilon_{\parallel} - \varepsilon_{\perp}\right)$$

where v_{lc} is the liquid crystal volume fraction in the sample, ε_p is the polymer dielectric permittivity, $\varepsilon_{\parallel}$ and $\varepsilon_{\perp}$ are the liquid crystal dielectric permittivities, K_d is an elastic constant per unit surface (units: Newton per square meter) taking into account the torque which, after the field is switched-off, produces relaxation of the droplets to their original orientation. The sample order parameter is a function of both the polymer and the liquid crystal dielectric permittivities.

For droplet radius approximately equal to the light wavelength, condition required to achieve high transmittance contrast, , the *transmitted intensity* of a PDLC sample is

$$I_t = \tau I_0 \exp\left(-\rho_N d_s \sigma_s\right)$$

where I_0 is the incident light intensity, τ is the Fresnel reflection coefficient for the air-glass and glass-polimer interfaces, ρ_N the droplet number per unit volume, d_S is the sample thickness, σ_S the sample scattering cross section given by:

$$\sigma_s = \left\langle \sigma_d \right\rangle_{sample} = \frac{1}{2}\sigma_G\left(2kR_d\right)^2\left(\frac{n_{de} - n_{do}}{n_p}\right)^2\left[\left(\frac{n_p - n_{do}}{n_{de} - n_{do}}\right)^2 - \frac{2}{3}\frac{n_p - n_{do}}{n_{de} - n_{do}}\left(1 - S_s\right) + \frac{4}{105}\left(7 - 10S_s + 3\widetilde{S}_s\right)\right]$$

and

$$\tilde{S}_s = \left\langle P_4\left(\hat{E}\cdot\hat{N}_d\right)\right\rangle_{sample} = \frac{7}{12} + \frac{5}{12}S_s - \frac{35}{32e_a^2}\left[\frac{2}{3} + \frac{\left(e_a^2-1\right)^2}{4e_a^2} + \frac{\left(e_a^2+1\right)\left(e_a^2-1\right)}{8e_a^3}\arctan\left(\frac{2e_a}{e_a^2-1}\right)\right],$$

$$\sigma_G = \pi R_d{}^2,$$

R_d is the spherical droplet radius, k is the wave number of the incident light and n_p is the polymer refractive index.

Frequency Dependence

We have used this model to study the response of the transmitted intensity to the variation of the parameters that are affected by the frequency of the applied voltage. The PDLC appears to be almost insensible to most of them. As an example in Fig.1 we show its dependence on the polymer dielectric permittivity εp . We see that transmitted intensity is constant in a range from one to twelve times the vacuum dielectric permittivity. The values we have assumed for the other parameters, here and everywhere in this paper when not differently stated, are: liquid crystal volume fraction in the sample v_{lc}=0.45, liquid crystal dielectric permittivities $\varepsilon_{\|}$ =18ε_0. and $\varepsilon_{\perp}$.=6ε_0., elastic constant per unit surface K_d=30 (units: Newton per square meter), droplet radius R_d=0.5μm , light wavelength λ=0.633μm, condition required to achieve high transmittance contrast, sample thickness d_s=20μm , polymer and glass refractive index n_p=n_v=1.54 , Temperature T=25.5 °C (room temperature), applied voltage V = 50 V, applied voltage frequency ν = 1Khz. The only frequency dependent parameters that appear to have a strong influence on the sample transmittance is the dielectric anisotropy of the liquid crystal. In Fig.1 we show the dependence of I/I_0 on $\varepsilon_{\|}$ - $\varepsilon_{\perp}$.. Now the polymer dielectric permittivity ε_p. is set equal to three times the vacuum one. Therefore we assume the liquid crystal dielectric permittivities $\varepsilon_{\|}$ and $\varepsilon_{\perp}$. to be the most important parameters for the applied field frequency dependence of light transmittance. On the other side for our experiment we use the liquid crystal E7 by BDH and we do not know the behavior of its permittivity versus the frequency.

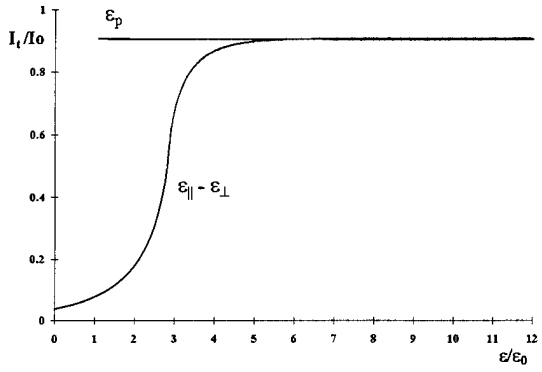

Fig. 1

To apply our model we have used at room temperature and at ν=1Khz the values $\varepsilon_{\|}$ =18ε_0. and $\varepsilon_{\perp}$.=6ε_0. that we have found in literature[13], but for the dependence on the frequency we used an expression able to simulate the behavior reported in [14] for liquid crystal K-24:

$$\varepsilon_{\|}(\nu) = \left(\varepsilon_{\|} - 1\right) erfc\left[2.4\left(Log\nu - Log\nu_0\right)\right] - 1$$

$$\varepsilon_{\perp}(\nu) = \left(\varepsilon_{\perp} - 1\right) erfc\left[2.4\left(Log\nu - Log\nu_0\right)\right] - 1$$

In Fig. 2 we show the behavior represented by these expressions. It can be seen to be very similar to the one reported in [14].

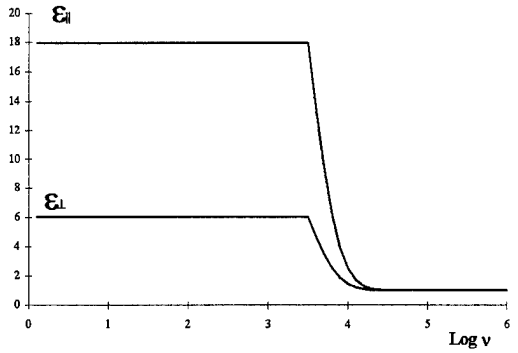

Fig. 2

Experiment

The PDLC solution is included between two glass slides coated with conducting transparent layers (ITO). Introduction of Mylar spacers 20μm thick before pressing the sandwich determines sample thickness. The sample is cured for 16 hours in a 60°C oven. The average molecular weight of the polymeric molecules increases while the reaction proceeds and liquid crystals droplets separate. Droplets diameter is determined by curing rate that, in our case, is low enough to have diameters comparable with visible light wavelength. The sample is translucent.

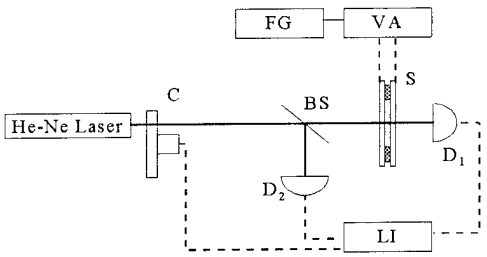

Fig.3

Experimental setup is depicted in Fig.(3). The beam from a 5 mW He-Ne laser (Fig.3) impinges normally on the sample (S). Voltage is applied by a function generator (FG) and a voltage amplifier (VA). A photodiode (D_1) is used to measure the transmitted intensity. A chopper (C) lock-in (LI) configuration is used to avoid noise and background signal. A reference beam is sent by a beam splitter (BS) to a second photodiode (D2) to check impinging beam stability.

In Fig.4 we report the experimental transmitted intensity Vs the applied voltage for different shapes of the field that is centered on zero value and has a frequency of 1000Hz (circular, square and triangular symbols correspond to sinusoidal, square and triangular signals respectively). As we can see the transmitted intensity is not influenced by field shape but only by its square average value.

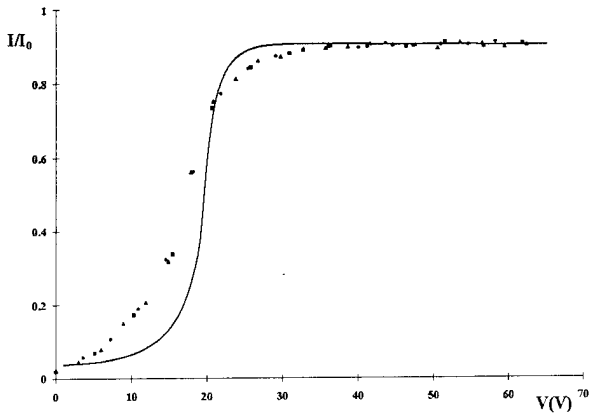

Fig.4

Full line represent the results of the application of the described model. We see that the switching is not simulated in a very accurate way. This fact had to be expected since here, for the sake of simplicity, droplet order parameters has been assumed to be constant. This problem has been discussed elsewhere[8]. Here we show this comparison only to demonstrate that the set of parameters value we have chosen to describe our sample is reasonable.

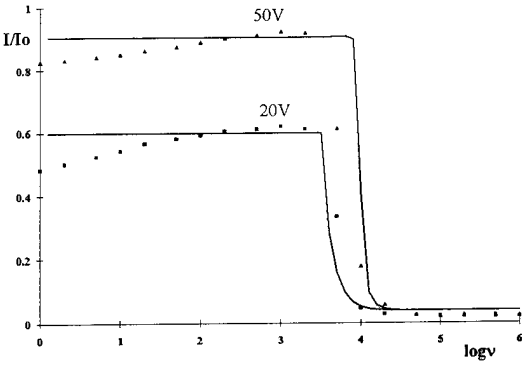

Fig.5

Finally in Fig.5 we report experimental data of the transmitted intensity versus the field frequency for two values of the applied voltage (circles for 50V and crosses for 20V). Full lines

are theoretical results of our model having as input the same set of parameters used for Fig.4 but with the dielectric permittivities dependence of Fig.2. These results seem to confirm the hypotheses that the sample transmittance depends almost exclusively on liquid crystal response. We hope to have more detailed and reliable information when experimental results about the liquid crystal dielectric permittivities dependence on the applied voltage frequency will be available.

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Novel Static RAM Pixel Circuits for Liquid Crystal over Silicon Spatial Light Modulators

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Abstract

In this paper, we present two novel Static RAM pixel designs for use in Liquid-Crystal-over-Silicon Spatial Light Modulators. Compared with existing designs, these new pixels have advantages in terms of circuit simplicity, circuit size, circuit connectivity, and power consumption. We discuss what considerations are required in the design of these pixels, why such considerations are important, and outline two schemes to drive the devices.

liquid crystal devices, spatial light modulators.

Introduction

Spatial Light Modulators (SLMs), consist of an array of pixels which, in binary devices, can be on or off (see Fig. 1).

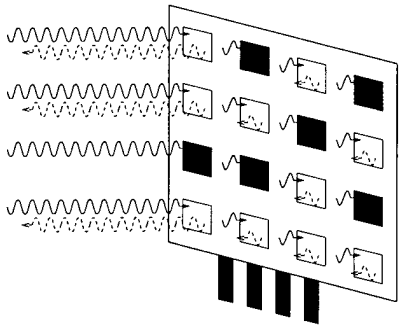

Figure 1. Spatial Light Modulator Pixel Array.

These devices have applications in displays, holography and optical computing systems [1].

Liquid Crystal (LC) devices use an LC material to modulate the amplitude and/or the phase of an incident light ray. There are several types of LC materials such as nematics and ferroelectrics [2]. For the purposes of this publication, ferroelectric liquid crystal will be discussed.

The devices are constructed by gluing the edges of a cover glass over a silicon die, on which an array of pixels is present. The inside of the cover glass is coated with a transparent electrode, and a gap is left between the electrode/glass and the surface of the die. This gap is filled with LC material.

One method of effecting amplitude modulation is as follows: Polarised light is presented to the pixel array. A voltage applied across the liquid crystal rotates the polarization of the light as it passes through the material. The "altered" light can be viewed through Polarizer B, the unaltered light cannot, and so the pixel appears dark (see Fig. 2).

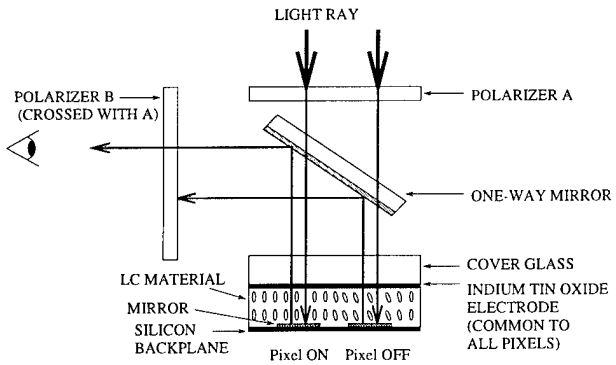

Figure 2. Amplitude Modulation using a LC SLM.

A requirement of liquid crystal materials is that they must be charge-balanced. This means that a voltage of

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$+V$ volts, applied for t seconds, must be followed by a voltage of $-V$ volts, for t seconds. That is, the net d.c. (i.e. time averaged), voltage across the material must be zero [3], otherwise the liquid crystal breaks down by electrochemical decomposition.

Each pixel in the array can be on or off, and thus has to store a logic '1' or '0' (for binary devices). This storage can be implemented using SRAM or DRAM cells.

DRAM and SRAM Pixels

DRAM cells are small and simple. However, they must be refreshed, suffer from photo-induced charge leakage, and may supply only a limited amount of charge to the mirror. To charge balance these devices may require a complex addressing scheme. This involves loading an image and then its inverse, possibly interspersed with blanking frames to turn the whole array on or off [4]. This lowers the frame rate of the device and means that the array has to be viewed under a pulsed light source.

SRAM cells are larger than DRAM. They require no refresh, are more robust, and provide better driving voltages for the pixel with an unlimited supply of charge (i.e. *Vdd* and *Vss*), via the SRAM cell — unlike the DRAM pixel which has a limited amount of charge stored in the DRAM capacitor. Also, SRAM cells can be viewed under a continuous light source. This is because specialised charge balancing circuitry can be incorporated directly onto the SRAM cell, and a complex addressing and driving scheme is not required (i.e. no inverse frame(s) require to be loaded). This in turn means that the device can have a higher frame rate.

Current SRAM Technology

Current charge-balancing SRAM pixels normally consist of a 10 transistor cell: Two pass transistors to allow data loading; two cross-coupled inverters to implement storage; and an XOR (or XNOR), gate to implement the charge balancing circuitry [5, p.64] [6] (see Fig. 3).

However, the internal XOR connectivity can be complex and the XOR circuitry may be large. This is because the transistors are lengthened in order to reduce current spikes when switching. The mirror is either driven by the **CLOCK** line through the transmission gate, or by a buffered (inverted) **CLOCK**. This means that the drive scheme is unequal as **CLOCK** is a global busline.

Charge balancing is effected by XORing the **CLOCK** signal — which is common to all pixels — with the stored data value (**LATCH**). This **CLOCK** signal is also present on the global Indium Tin Oxide (ITO), electrode. If the pixel is storing a '1', the mirror experiences a $+V_{DD}$, $-V_{DD}$, transition over one clock period. This will turn the pixel ON, and then implement the charge balance (the mirror having a 50% duty cycle). If the pixel is storing a '0', the XOR output is in phase with **CLOCK**, so the mirror will have a zero voltage drop and remain off. In each case, the net d.c. voltage across the mirror is zero (see Fig. 4) [5, pp.66-69]. Since the **CLOCK** line is common to all pixels, the charge balance occurs simultaneously across the whole array.

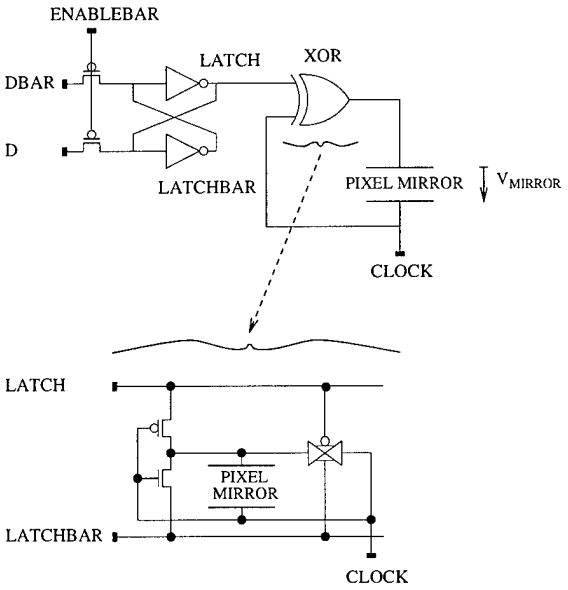

Figure 3. Conventional XOR SRAM Pixel.

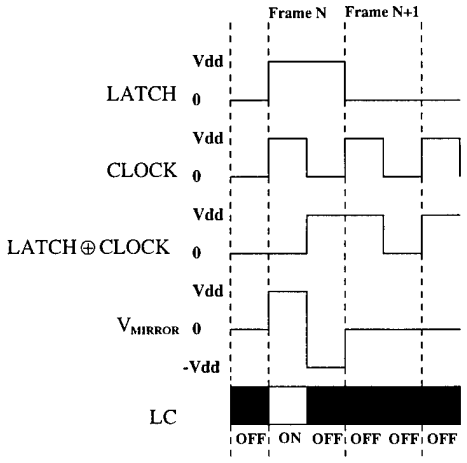

Figure 4. Charge Balancing Waveforms.

The XOR gate is merely required to implement a LO-HI transition if the pixel is to be ON, and a HI-LO transition, if the pixel is to be OFF (or vice versa). Our new pixels use simpler techniques to do this.

New Devices

The new devices make use of transmission gates or pass transistors to switch the output of the SRAM cell LO-HI or HI-LO (or vice versa), as required. Two devices

are discussed.

10 Transistor SRAM Pixel

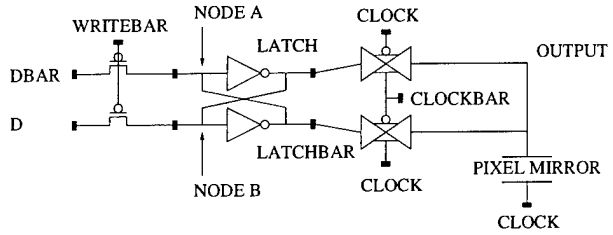

Figure 5. 10 Transistor SRAM Pixel.

This pixel contains 10 transistors. It consists of:

- A 6 transistor SRAM cell.
- 2 transmission gates switched by **CLOCK** and **CLOCKBAR** to toggle the SRAM outputs.
- When **CLOCK** is HI, **OUTPUT** is **LATCHBAR**.
- When **CLOCK** is LO, **OUTPUT** is **LATCH**.

Advantages The transmission gate transistors can be minimum sized and the connectivity of the pixel is simpler — this leads to a saving in pixel area. Also, the mirror is driven directly by the SRAM outputs (via the transmission gates), so the drive scheme is balanced.

8 Transistor Pixel

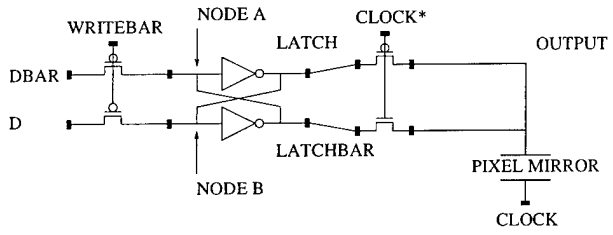

Figure 6. 8 Transistor SRAM Pixel.

This pixel contains 8 transistors. It consists of:

- A 6 transistor SRAM cell.
- 2 pass transistors switched by **CLOCK***.
- When **CLOCK*** is HI, **OUTPUT** is **LATCHBAR**.
- When **CLOCK*** is LO, OUTPUT is **LATCH**.
- The **CLOCK*** signal is switched between $(V_{SS} - V_{th})$ and $(V_{DD} + V_{th})$ to ensure good logic levels at **OUTPUT** (this will be discussed later). **CLOCK** switches between V_{SS} and V_{DD} as normal.

Advantages This pixel exhibits similar advantages to the 10 transistor design. In addition, it uses only 8 transistors, has an even simpler connectivity, and one less busline.

Comparisons

A comparison of pixel attributes, taken from the AMS 1.2μm, CMOS process, run at $5V$, can be seen in Table 1.

Table 1. Pixel Attributes.

Pixel	Area (μm^2)	RMS Power (μW)	I_{MAX} (μA)
256-XOR[1]	1600	86.068	86.68
256-XOR (revised)[2]	1020	190.78	155
10 Transistor	921	184.21	115.84
8 Transistor[3]	829	388.79	102.81

1. This pixel was used in a 256x256 SRAM LC-SLM designed at the University of Edinburgh.
2. This pixel is a redesign of the above.
3. Using an overdriven CLOCK* .

With savings in pixel area and the continuing reduction in process geometries (IMEC [Belgium] offer 0.5μm CMOS and will soon offer 0.3μm [7]; IBM offer 0.18μm CMOS [8]), it is now feasible to produce Ultra-scale SRAM SLM devices, i.e. having resolutions of 1000x1000 to 2000x2000 pixels and above.

The new pixel designs can be further modified to reduce the number of transistors and buslines and/or change the transistor type(s) and configurations [9].

Design Considerations

Care must be taken in the design of the new pixel circuits shown in Figs. 5 and 6. Several important features must be considered.

Charge Sharing and Current Spikes

If, as in this case, one-phase, complementary clock signals are being used, there will be a point when the clock signal switches where both **LATCH** and **LATCHBAR** are short-circuited. It is important to ensure that current spikes are acceptable under these conditions.

Pixel Mirror Capacitance

If the mirror capacitance is very large, and the capacitance at nodes **A** and **B** is small, then when the SRAM cell tries to drive the mirror to a different state, charge could leak *back* from the mirror into the SRAM cell. This would cause the SRAM cell to change state. That is, the mirror would drive the SRAM cell, rather than the SRAM cell driving the mirror. Care must be taken to ensure that the capacitance values associated with these nodes are ratioed properly, and that the inverters have sufficient drive capability.

Simulations show that with a 30x30μm mirror, the capacitance of the mirror node would have to be over an

order of magnitude above typical calculated values in order to effect this. That is, the mirror capacitance would have to be at least 1970fF, when the typical value is actually 134.1fF (with a node **A** capacitance of 13.29fF).

Driving Schemes

The 8 transistor cell drives the mirror through a pmos or nmos transistor. In isolation, these devices are not ideal switches. A pmos transistor is able to switch a HI logic signal, but will attenuate a LO logic signal; when the gate voltage is LO. A nmos transistor will switch a LO signal, and attenuate a HI; when the gate voltage is HI [10, p.56]. The attenuation, for an nmos transistor, is as follows (see Fig. 7).

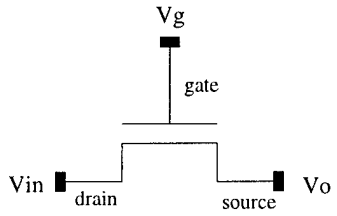

Figure 7. nmos transistor.

$$V_o = V_{in} \quad if \quad V_{in} < V_g - V_{th} \tag{1}$$

The threshold voltage V_{th}, is not constant. It varies with the body effect [10, p.41]:

$$V_{th} = V_{t(0)} + \gamma[\sqrt{V_{sb} + 2\phi_F} - \sqrt{2\phi_F}] \tag{2}$$

Where, V_{sb} is the substrate voltage, ϕ_F is a constant, $V_{t(0)}$ is the threshold voltage when $V_{sb} = 0$, and γ is a constant that describes the substrate bias effect.

Therefore in order to allow good switching of logic levels in the 8 transistor pixel, the pass transistors must be driven by a **CLOCK*** signal that switches between at least $(V_{SS} - V_{th})$, and $(V_{DD} + V_{th})$.

Implementation

Circuitry based on the above designs has been included on a test chip. The test chip (Xavier1), contains:

- an 8x7 array of 10 transistor SRAM cells.
- a 2x2 array of 8 transistor SRAM cells with drive scheme 1 (detailed below).
- a 2x2 array of 8 transistor SRAM cells with drive scheme 2 (detailed below).

The chip is being fabricated through MOSIS on the Orbit 2μm, $5V$, analogue, CMOS, n-well process.

Simulations show, that to drive the 8 transistor devices properly requires voltages of $-3V$ and $+7V$. The latter can be generated using on-chip circuitry by shielding a n-well and strapping it to +7 volts. As it is not possible in an n-well process to create individual p-wells, a similar technique cannot be used to generate the required -3 volts.

Drive Scheme 1

The first approach is to drive the transistors directly with $-3V$ and $+7V$. The **CLOCK** signal does not pass through any transistor circuitry on the chip. However, this means that the standard pads with Electrostatic Discharge (ESD), Protection circuitry cannot be used. Therefore there is a danger of damaging the circuitry when handling the chip. The actual voltage that could be generated at the transistor gate is given in Eq.3 [10, p.227]:

$$V = \frac{I\Delta t}{C_g} \tag{3}$$

The voltage produced can be extremely high relative to the small current that may flow onto the chip from external sources if handled incorrectly.

For example, if I=10μA, and C_g=0.03pF, and Δt=1μs; then V=330 volts.

In order to reduce this voltage, the capacitance of the node is increased, and the line resistance is also increased to reduce the potential current (see Fig. 8).

This approach limits the operational speed of the pixels, but will allow some testing and characterisation to be carried out.

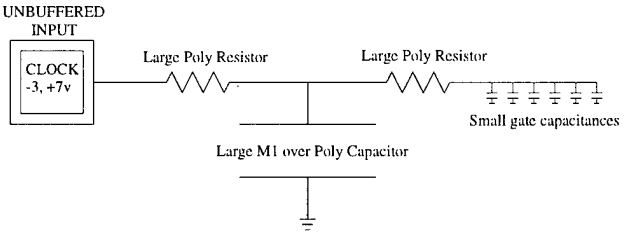

Figure 8. Simple ESD Protection Circuitry.

Drive Scheme 2

The second approach is to build a buffer on the chip itself. The buffer takes a $0V$, $5V$ input, and has a $+7V$, $-3V$ output. This means that the **CLOCK** signal can be buffered via a standard input pad that contains ESD protection circuitry. However, the buffer requires a $+7V$ n-well and a $-3V$ p-well in order to operate (see Fig. 9).

It is not possible to fabricate a p-well directly with the available process. However, one can be synthesized by creating an n-well ring around a small area of the p-substrate. This small area is tied to the required -3 volts and heavily shielded (see Fig. 10).

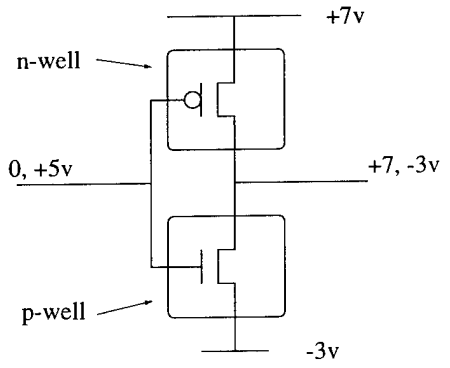

Figure 9. Buffer Schematic.

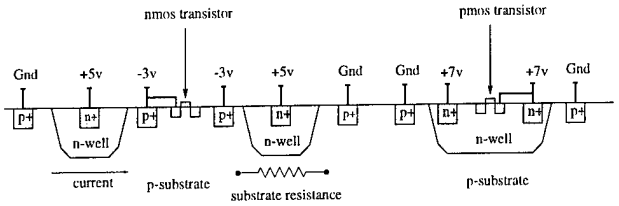

Figure 10. Synthesized p-well Inverter.

The guard ring shielding and the n-well ring (around the -3 volt area), with another Ground guard ring, should help to limit the substrate current.

Note that these drive schemes would not be required in a twin-well process. They are only required for single-well wafers.

Conclusions

It is desirable to use SRAM pixels in binary Liquid-Crystal-over-Silicon Spatial Light Modulators. On-pixel charge balancing circuitry allows devices to have a high frame rate.

We have presented two novel SRAM pixel circuits for use in LC SLMs. These devices exhibit several advantages over current designs.

Any saving in pixel area and current/power requirements can have a significant effect on the device resolution/size/performance/yield trade-off, especially in the design of very high resolution SLMs.

Acknowledgements

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Phase modulated liquid crystal spatial light modulator with VGA resolution

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Abstract

A phase type VGA resolution LC-SLM was developed. The SLM is capable of easy operation with ordinary PCs and phase modulation more than 2π.

Introduction

Phase type SLMs with real time operation are required for various kinds of applications. We have been developing liquid crystal SLMs and their applications for a decade. For examples are kinoform reconstruction [1], complex amplitude modulators, which are called spatial wavefront modulators (SWMs) [2] and light valves for projection displays [3]. Following projector market expansion, poly-Silicon thin film transistor liquid crystal displays (poly-Si TFT-LCDs) have rapidly progressed with their resolution, VGA, SVGA and more, and pixel density. Every fundamental SLM investigation, however, has been carried out with specialized SLMs and driving interface circuits. This is a barrier to the prevalence of the phase type SLMs to widely applicable fields. In this paper, we report a newly designed phase type SLM with VGA resolution, which accepts ordinary PC video outputs.

Device structure

Figure 1 depicts the SLM appearance. It incorporates liquid crystal modulating pixels with poly-Si TFTs active matrix as switching elements, and integrated poly-Si TFT drivers on the same glass substrate. The poly-Si TFT technology has been developed for liquid crystal projectors, and then they are very reliable devices under strong illumination.

A cross-section view of a pixel area is shown in Figure 2. Viewed from the bottom up, there is a quartz substrate and a TFT for a switching element, whose drain and source are fabricated on the substrate and gate is on the gate oxide,

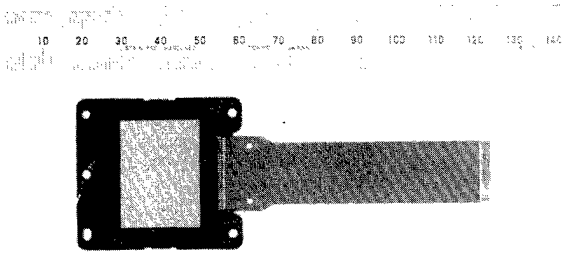

Fig. 1 Phase TFT-SLM with VGA resolution

whose structure is called a co-planar structure. After that there is a non-doped Silicate glass (NSG) formation, and Aluminum source electrodes, X electrodes, are photo-patterned. Then a Phospho-Silicate glass (PSG) layer is deposited, and finally Indium Tin Oxide (ITO) of pixel is photo-patterned.

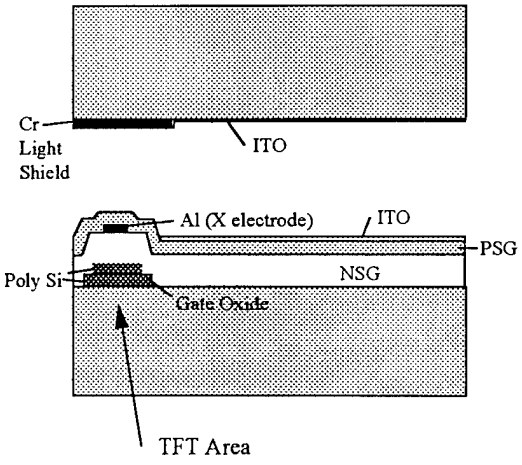

Fig. 2 Typical cross-section view

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Figure 3 shows a typical plane view of a light shielding pattern. TFT, even when fabricated with poly-Silicon, will leak photo-current under UV light irradiation. To avoid leakage, the light shielding is usually employed on the counter substrate. In the case of strong light illumination, the light should enter from the side of the counter substrate.

The shielding pattern decides aperture ratio and the diffraction characteristics, particularly efficiency. Usually, it is made of metal or pigment, in this case, we employed Chromium.

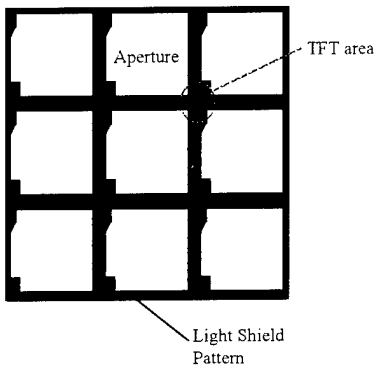

Fig. 3 Typical light shielding pattern

Although Smectic LC is usually used for high speed switching, we incorporated Nematic LC due to its stability and reliability. This is because LCs for active matrix require high resistivity. They show, however, low birefringence. Considering the ability for low driving voltage, we selected a relatively high birefringence LC mixture, whose value is $\Delta n=0.166$. In a simple theoretical calculation, 2π modulation requires more than 3.8μm LC thickness, and therefore we fabricated the panel with 4.5 μm thickness.

For the alignment of liquid crystal, homogeneous alignment has been used for electrically controlled birefringence, ECB, mode. Both substrates of the SLM in Figure 1 are rubbed in parallel along Y direction. The homogeneous LC alignment in Y direction is obtained accordingly.

Driving circuit

Figure 4 is a newly designed driving circuit. The interface allows easy connection with PCs. To obtain accurate horizontal pixel alignments between data and actual positions, a phased lock loop (PLL) circuit is used. In Fig. 4, the polarity alternation circuit generates a alternating driving waveform to avoid electro-chemical degradation of LC. "6ϕ Video" means the video signals expanded into 6 phases to reduce clock frequency of the TFT drivers. In the level shift circuit, video signals are corrected according to gray level linearity. This treatment is called γ-correction.

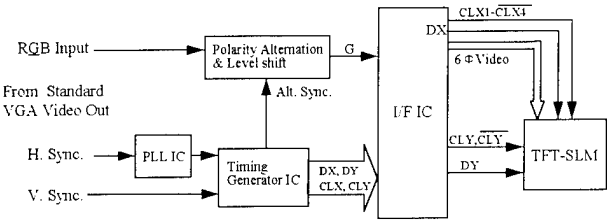

Fig. 4 Driving circuit

Phase modulation characteristics

Figure 5 (a), (b), (c) shows phase modulation characteristics including the dependency on LC materials and wavelength. Video voltage indicates actual voltage applied to an individual LC pixel through a TFT element. Due to the high resistivity of LC material, the voltage may represent the effective voltage applied to LC layer. The modulation characteristics show birefringence as an uniaxial crystal under less than 1.5v. Application of over 5v, still does not saturate modulation. Since 5v is the limitation of the driving circuit, we can not utilize all the birefringence of LC. Modulation of more than 2π is attained in the cases of $\Delta n=0.166$ and wavelength less than 550nm, and wavelength less than 450nm for $\Delta n=0.139$ and 0.129. In addition, using the TFT driving method with analog video signals, continuos phase modulation, in other words "blazed grating", is easily obtained, and it can provide high diffraction efficiency.

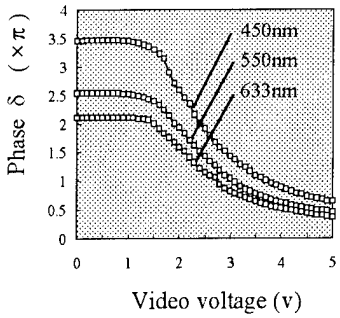

Fig. 5 (a) Phase modulation characteristics
$\Delta n=0.166$ at 589nm

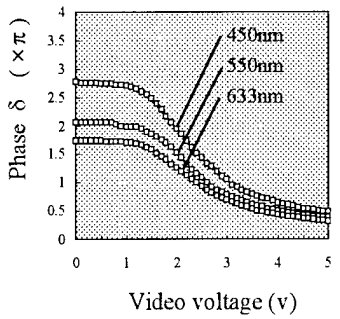

Fig. 5 (b) Phase modulation characteristics
Δn=0.139 at 589nm

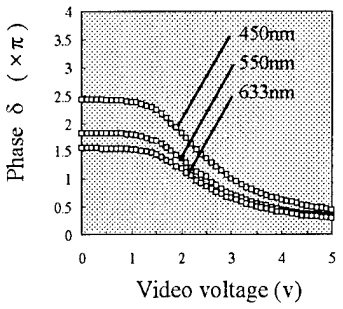

Fig. 5 (c) Phase modulation characteristics
Δn=0.126 at 589nm

Calculations of phase modulation are carried out by transmissivity measurements with cross Nicole configuration, whose setup is shown in Fig. 6.

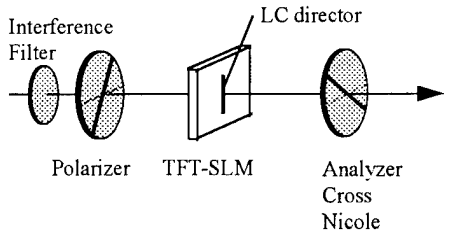

Fig. 6 Transmissivity measurement setup

Transmissivity is given by

$$T=T_0\sin^2(\delta/2) \quad \text{where } \delta=2\pi\,\Delta nd/\lambda..$$

The calculation steps are explained in Fig. 7.

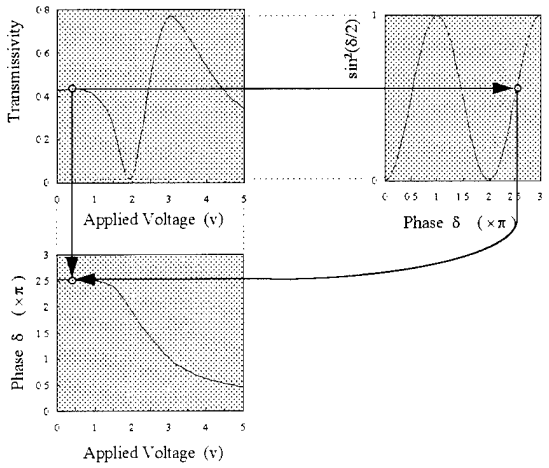

Fig. 7 Phase calculation

Kinoform reconstruction

In order to confirm the phase modulation characteristics, we tried to make kinoform reconstruction. We combined the same basic 12 kinoform patterns reported before[1] as shown in Figure 8. The basic pattern is computed using the iterative method. Thereby, 348×512 dots were used in this experiment, where VGA resolution was not utilized entirely.

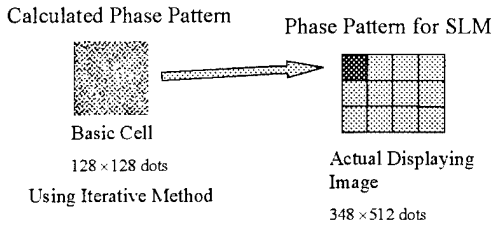

Fig. 8 Kinoform pattern

By using a He-Ne laser and a 800mm convex imaging lens, the images shown in Figure 9 are reconstructed. Speckle noise is well-suppressed and minus-order image is hardly observed. In this experiments, because we did not adopt the conjugation of lens function on the kinoform pattern, a residual zero-order spot remains, whose spot can be diminished with lens function.

Fig. 9 Reconstructed images

Diffraction efficiency is assumed to be a value close to the square of the SLM's aperture ratio, because phase distribution can be displayed with high fidelity. Hence, diffraction efficiency of about 40% for the aperture ratio of 64% is prospected.

In this paper, we measured the phase modulation characteristics through transmissivity measurements to obtain accurate values corresponding to phase modulation. Direct fringe measurements with the interferometer presented previously[1] show a good agreement with the transmissivity method.

We observed the improved kinoform image quality, whose clear lines and high contrast compared favorably to the previous results. This is because interference between pixels, e.g. speckle noise, is well suppressed due to an increase of modulating points and reduction of sampling errors on X scanning.

Current specifications and future prospects

Specifications of the SLM are summarized in Table 1. The right row in Table 1 shows specifications for next generation 0.9" VGA. Pixel density of 42μm pitch for 1.3" and 23μm pitch for 0.9" has been realized. Deducing the specifications according to TFT-LCDs developments speed, we may forecast a 10μm-order pixel pitch in the near future.

Table 1 Specifications of TFT-SLMs

	1.3" VGA	0.9"VGA (next genaration)
Size	26.9×20.2 mm	18.5×13.9 mm
Pixel Pitch	42μm×42μm	23μm×23μm
No. of Pixel	640×480	640×480
Aperture Ratio (Conventional)	64% (35%)	50%
δ (phase modulation) (Cell Gap)	2.5π (4.5μm)	2π (3.5μm)

Conclusion

LC-SLMs are essentially not capable of high speed switching compared to semiconductor base SLMs and optical crystals. The LC-SLMs, however, are easy to operate, reliable and capable of large pixel capacity based on LC technologies, e.g. active matrix, LC materials and fabricating technologies.

On the basis of these technologies, we developed newly designed SLM with VGA resolution that is easy to operate through standard PC video outputs. The interface for the SLM is newly designed for accurate pixel alignments between data and actual positions. As for LC, by selecting an LC material and suitable panel configuration, phase modulation of more than 2π is obtained, and thereby kinoform images with high fidelity are reconstructed for the confirmation of accurate phase modulation.

Acknowledgments

The authors acknowledge H. Sakata and H. Horiguchi for their cooperation and the TFT division of Seiko Epson Corporation.

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SLM Applications

Applications of SLMs to phased array antennas and optical correlators

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Introduction

We review two applications of liquid crystal SLMs: Optically controlled phased array antenna and optical correlators for biometric identification.

Phased array antenna

Wide instantaneous bandwidths will be required in the future active phased array antennas. As multifunction antennas they will be used in a variety of operating modes such as radar, communications and countermeasures. The far field pattern of a phased array antenna is controlled by the relative phase and the amplitude distribution of microwave signals emitted by regularly spaced radiating elements. Microwave phase shifters provide highly directive but frequency dependent microwave beam steering.[1] For radars with a wide instantaneous bandwidth and countermeasure systems, time delay networks have to be introduced. In this case the antenna far-field pattern is not altered when the frequency is scanned or when a wide spectrum is radiated. Delays equivalent to the size of the antenna are necessary to perform a ± 45° scan angle over a wide frequency bandwidth. Optoelectronic architectures, with their parallel processing and low loss transmission capabilities are attractive for time delay beam forming.[2]

The operating principle of our 2D optical architecture[3] is detailed in Fig. 1. A dual frequency laser beam is the optical carrier of the microwave signal. This beam is expanded an travels through a set of SLMs with the same number of pixels (pxp) as the number of radiating elements of the antenna. M_o is a parallely aligned nematic liquid crystal SLM. It controls the phase of the microwave signal by changing the relative optical phase of the cross polarized components of the dual frequency beam. At the output of M_o, the linearly polarized dual frequency beam intercepts a set of spatial light modulators SLM_i, polarizing beam splitters PBS_i and prisms P_i. They provide the parallel control of the time delays assigned to the antenna. The beam polarization can be rotated by 0° or 90° on each pixel. According to the polarization, PBS_i is transparent (and the light beam intercepts the next SLM_{i+1}) or reflective (and the microwave signal is delayed). The collimated beam travels through all the (PBS_i) and is focused by an array of microlenses (L) onto an array of pxp fiber pigtailed photodiodes (PDA). For a given photodiode, the phase of the microwave beating signal is determined by the applied voltage on the corresponding pixel of M_o and by the choice of the PBS_i on which the reflections occur. Since the positions of prisms P_i provide delay values according to a geometric progression (τ, 2τ, 4τ..), the beating signal can be delayed from 0 to $(2^{N-1})\tau$ with step τ.

The switching time of this architecture is mainly determined by the response time of the liquid crystal SLMs and can take advantage of their high resolution. To provide high speed switching, one can use ferroelectric liquid crystal SLMs. The response time of the analog control of the phase delays by M_0 can be reduced to 200 µs with chiral smectic liquid crystals.[4] Moreover, in a realistic radar application, even such long switching times can be handled. Resolution of liquid crystal SLMs (up to $10^3 \times 10^3$) greatly exceed the number of radiating elements of the antenna. It is then possible to replicate the image of the antenna M times on each SLM_i (p x p x M pixels) and to use a high speed (10 ns) integrated optic 1xM coupler placed just before BE (fig.1) to switch between the images.

We have recently completed the experimental demonstration of an optically controlled phased array antenna, operating between 2.5 and 3.5 GHz.[3] The 2D architecture is implemented with 6 SLMs of 4 x 4 pixels. It provides 32 delay values (5 bits), an analog control of the phase [0,2π] and permits the control of a 16 element phased array antenna. Fig.2 displays an example of the microwave beam deflection using time delays. Furthermore, when far field patterns at different frequencies are superposed for a given scan direction (Fig.3), one can notice the absence of any beam squint.

Based on this demonstrator (Fig.4) it is realistic to extend these concepts to a much larger number of radiating elements (up to 10^3 - 10^4) with 2^6 to 2^{11} delay values in order to provide low sidelobe arrays. A global compact architecture for the optoelectronic processing of both radar transmit and receive modes is furthermore under study. It could greatly benefit from recent advances of optical interconnects[5] and computer generated hologram technologies,[6] taking advantage of a holographic backplane scheme,[3] in order to solve the problems of compactness, reliability and scaling up to the millimeter wave frequencies.

Optical correlation for identification

Biometric recognition is of great interest in a wide range of validation, identification, and population control applications.[7] Fingerprint identification is most promising although the two major issues are the speed of recognition and the image distortions that occur in the fingerprint acquisition step, when a

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finger is placed in contact with a prism or paper. Image correlation provide a global and fast approach, but can handle only a limited level of distortions. We present a non-contact fingerprint acquisition technique (Fig.5) that significantly improves the recognition performance of our correlator.[8-9] In a first approach, the finger is covered with a metallic powder, then presented, "nail-against-the-guide" to a camera. The finger is illuminated by a ring white light source through a polarizer. An analyser is placed in front of the objective of the camera. A depolarization in the crests of the fingerprint occurs. Conversely, the ridge lines, covered with metal, preserve the polarization of the light and are thus clearly visible. The fingerprint image is very good: pores on the ridges can be seen (Fig. 5, B).

For some applications covering a finger with a metallic powder is not acceptable. In this case, the second alternative involves a digital processing after CCD detection. Parallel polarizer/analyser orientation exploits the depolarization effects in the fingerprint crests. A digital filter provides contrast enhancement and good image quality (Fig. 5, B).

The main advantage of these techniques is that from acquisition to acquisition, there is no fingerprint image modification.

Optical correlators provide the opportunity for processing fingerprint images at high speed.[9-11] The optical layout of our correlation demonstrator[9] is shown Fig. 6. It operates as follows: Reference R_i originate from a fast access hard disk memory, while the unknown fingerprint is captured with the non-contact sensor. The two video signals are mixed to generate a single video image which represents the intensity distribution $R_i + S$. This intensity distribution is relayed to a coherent optical beam with the use of a SLM (428 x 244 pixels with pitch 31 x 46 µm). A mini-YAG visible green laser is spatially expanded and is modulated by the image on the SLM. A specially designed Fourier transform lens system generates the complex Fourier transform field, which is recorded in the photorefractive BSO material. The photoinduced phase hologram is read out under Bragg direction by a plane wave from a 3mW red laser diode. The diffracted field amplitude undergoes Fourier transform through the same optical lens and provides the correlation peak at the CCD sensor. The whole optical system is 300 x 300 x 150 mm^3 (Fig 7).

Qualitative experimental results are shown in Fig.8. The distortions between two independant acquisitions with a classical prism sensor are clearly seen on the top pictures. The resulting correlation peak is low. Independent acquisitions using our new non-contact fingerprint sensor are shown in the middle pictures. Almost no distorsion can be seen, and the associated correlation peak is large. Finally, the bottom pictures depicts the results of correlation using our non-contact technique, with no metal powder on the finger, but with a digital filter to enhance the image contrast. The correlation peak is still high.

Preliminary quantitative experiments have so far involved the non-contact acquisition of 10 individuals. The recognition of a single person on this limited data base is always successful, with no false rejection. A statistical analysis using a larger data base will provide the False Acceptance Rate (FAR) and the False Rejection Rate. Our current measurements show a FAR smaller than 1%.

The authors thank the D.R.E.T. (Direction des Recherches, Etudes et Techniques) for partial support, the radar divisions of Thomson-CSF, S. Samouilhan and J. Colin for their contributions.

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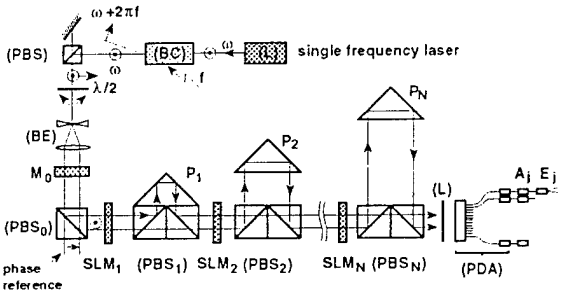

Fig.1 : Time and phase delays for phased array antenna : (BC) frequency shifter Bragg cell - (Aj) : microwave amplifiers - (Ej) : radiating elements.

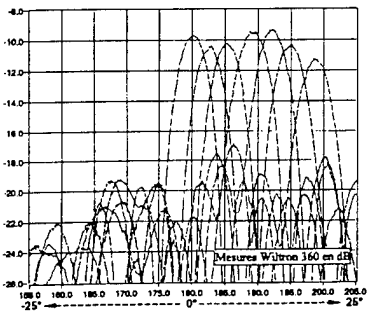

Fig.2 : Far field pattern of the optically controlled phased array antenna : time delay scanning, between 0° and 20° at frequency 3.1 GHz (amplitude in dB)

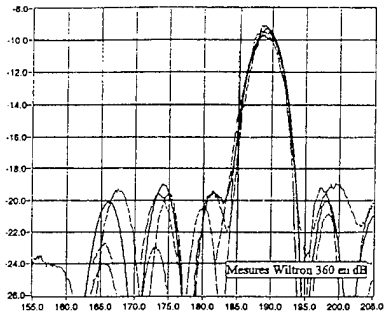

Fig.3 : Superposition of the far field patterns, obtained by time delay scanning, for frequencies ranging from 2.7 to 3.1 GHz and for a 8° scan angle - no beam squint (amplitude in dB).

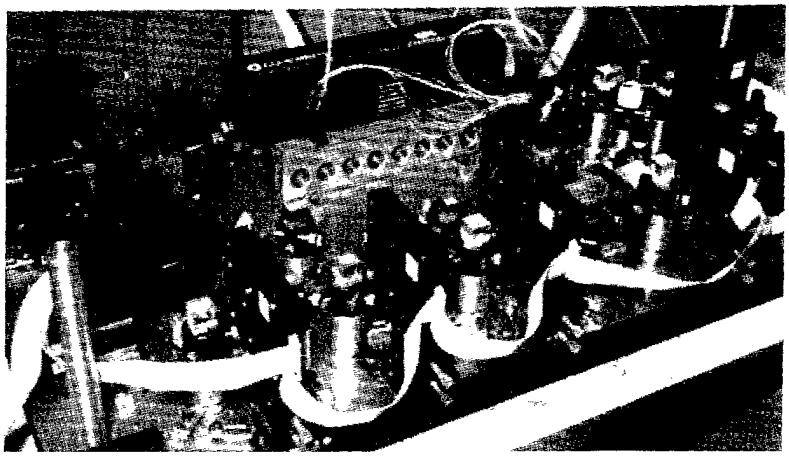

Fig.4 : Experimental set-up :4 x 4 channels, 32 time delays (5 bits : 17.5 , 35 , 70 , 140 , 280 mm), 7 bit phase control between 0 and 2π.

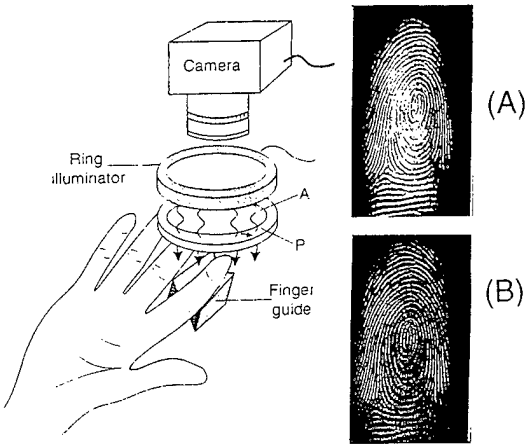

Fig. 5: Non-contact fingerprint acquisition technique: The finger is presented "nail-against-the-guide" to the camera; P, Polarizer; A, Analyser. (A): with metal powder; (B): with digital contrast enhancement.

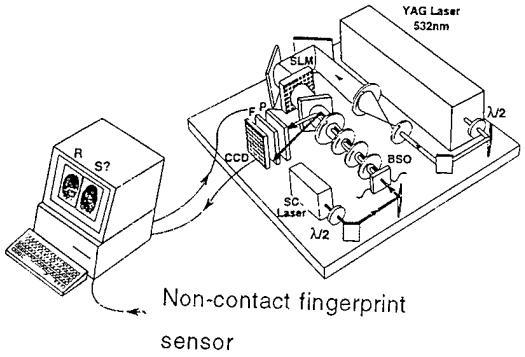

Fig. 6: Optical layout of the photorefractive joint transform correlator

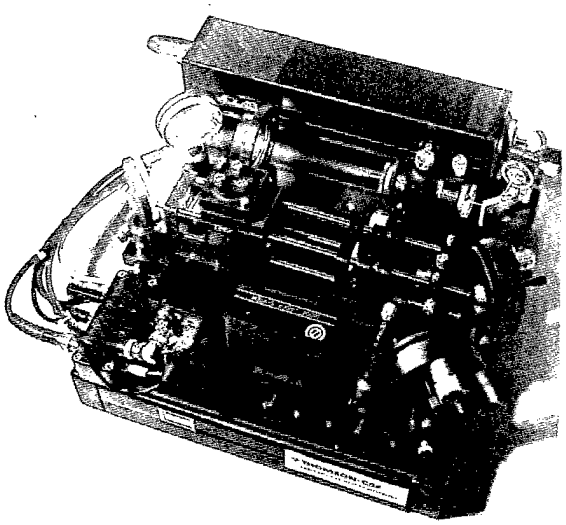

Fig. 7: Photograh of the correlator

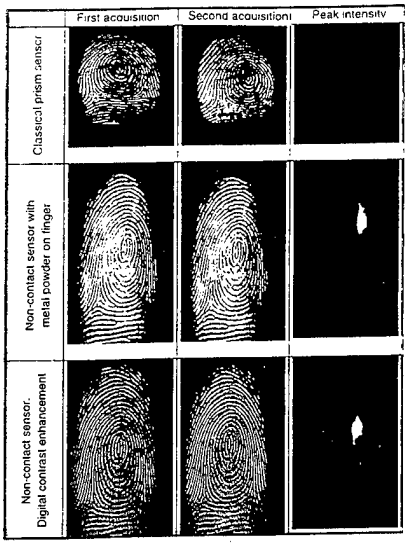

Fig. 8: Experimental results showing the correlation between two independent acquisitions. Top pictures: classical prism sensor; Middle pictures: Non-contact sensor with metal powder on finger; Bottom pictures: Non-contact sensor with a digital pre-processing.

Applications of SLMs to PHASED ARRAY ANTENNAS, OPTICAL CORRELATORS and LASER BEAM SHAPING

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Viewgraph

Outline

① Optically controlled phased array antennas

② Non linear joint transform correlator

- biometry
- target tracking

③ Beam shaping of high energy lasers

1

Optically controlled phased array antennas

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Viewgraph

PHASED ARRAY ANTENNAS

- Active antenna for multifunction systems:
  radar, communication, electronic warfare

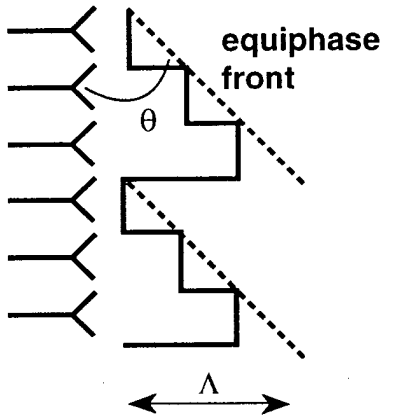
→ Large instantaneous bandwidth (stealth target)

→ Smart skin (for low observability platform)

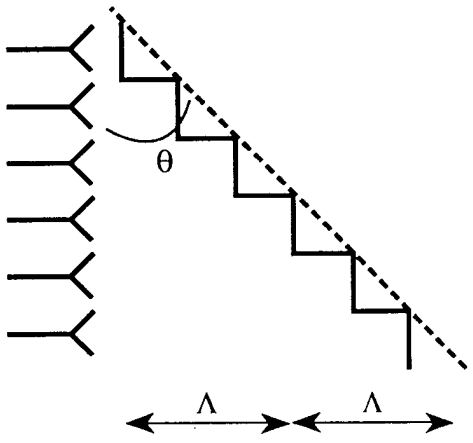
→ SLMs for control of phased array antennas

OPERATING PRINCIPLE OF A PHASED ARRAY ANTENNA

Phase scanning



Time delay scanning



Incremental phase shift

Constant with frequency

Proportional to the frequency

Scan angle

Frequency dependent

Frequency independent

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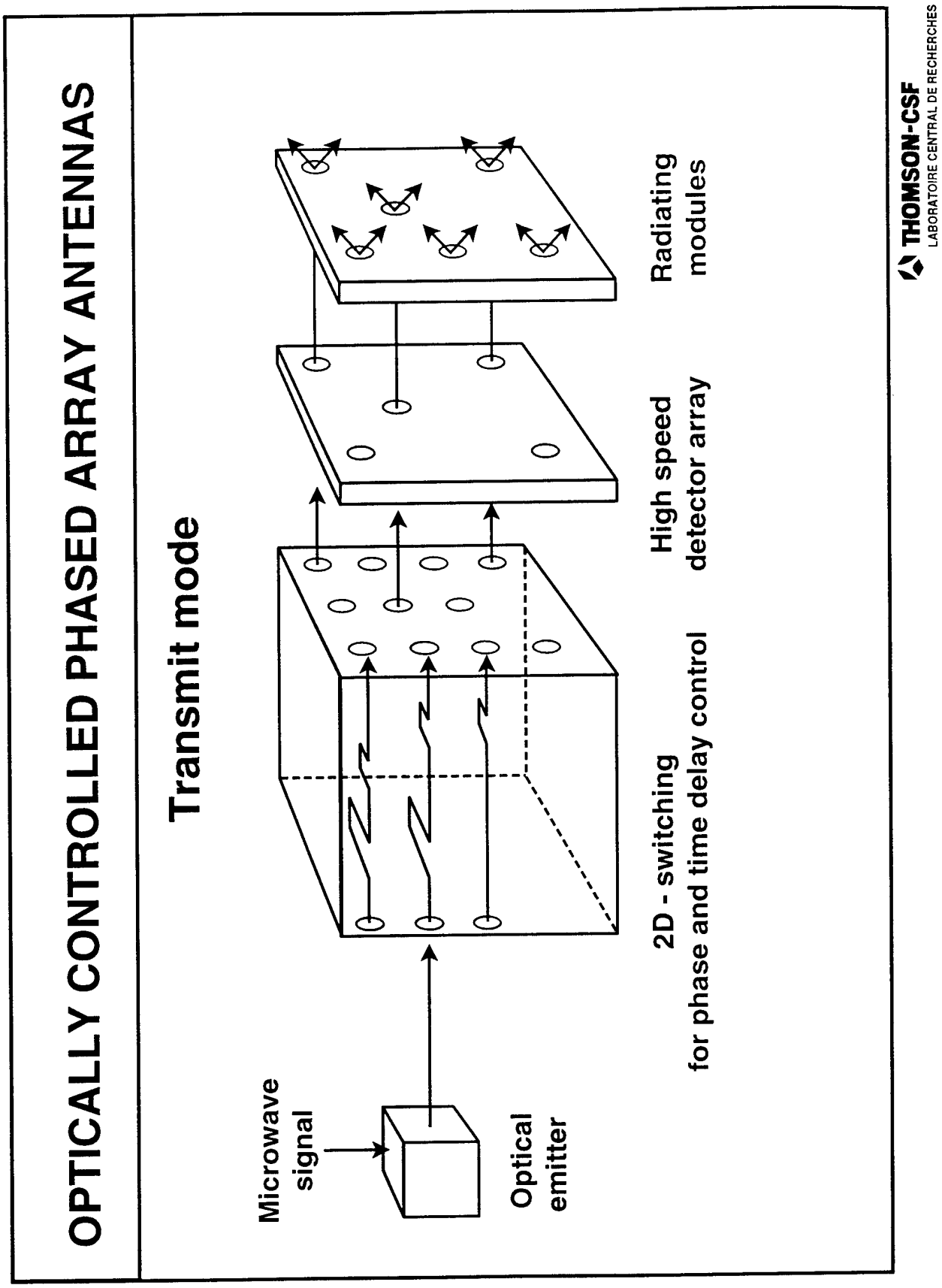
Viewgraph


OPTICALLY CONTROLLED PHASED ARRAY ANTENNAS
Transmit mode
Microwave signal
Optical emitter
2D - switching for phase and time delay control
High speed detector array
Radiating modules
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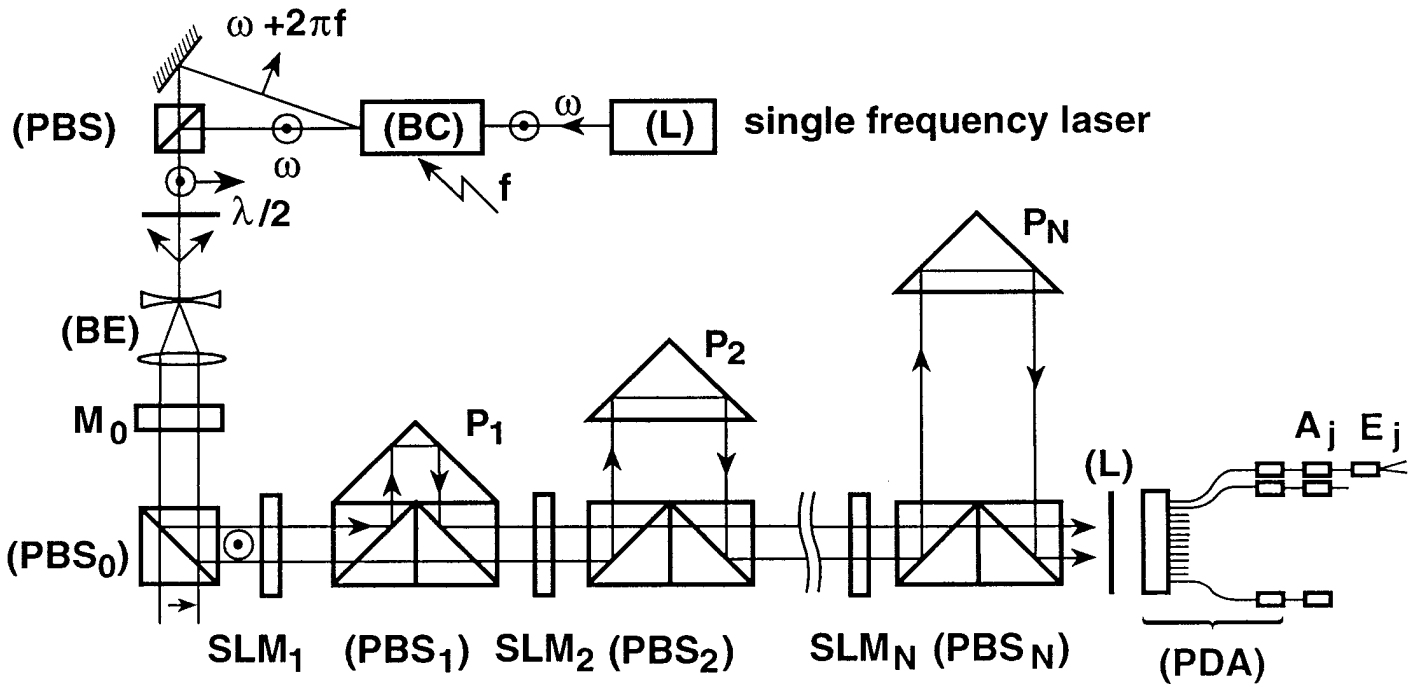
OPTICAL IMPLEMENTATION



- M_0 : SLM used in the electrically controlled birefringent mode
- SLM_i : rotate by 0° or 90° the light polarization on pxp pixels

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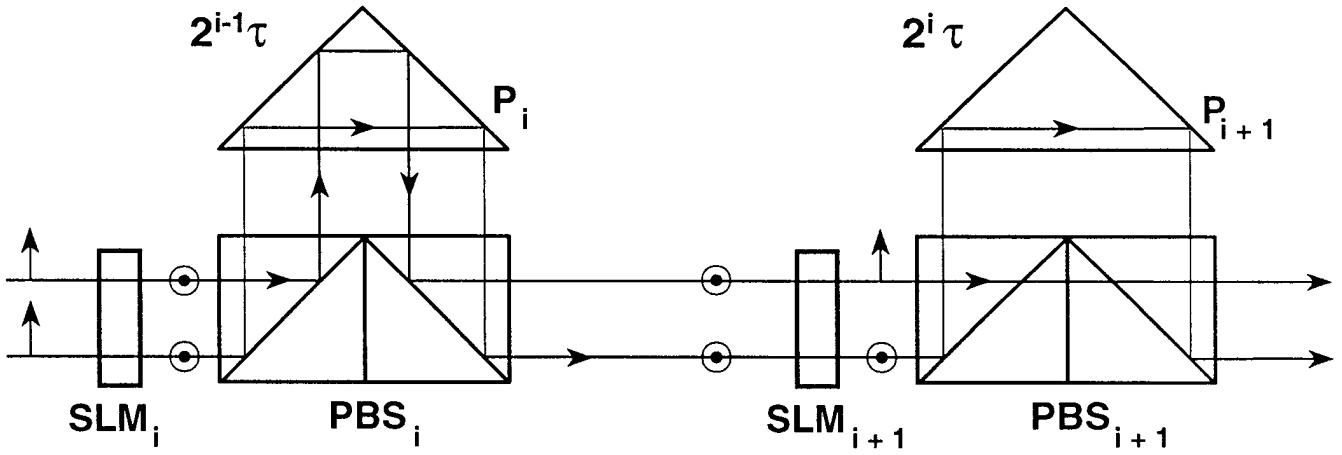
IMPLEMENTATION OF THE DELAYS



- N spatial light modulators ➡ 2^N delays
- Each SLM : P x P pixels
- Channel k : $i_k(t) = i_0 \cos\left(2\pi ft + 2\pi f \sum_{j=1}^{N} \varepsilon_{kj} 2^{j-1}\tau\right)$

  if reflection on PBSj : $\varepsilon_{kj} = 1$

  if not : $\varepsilon_{kj} = 0$

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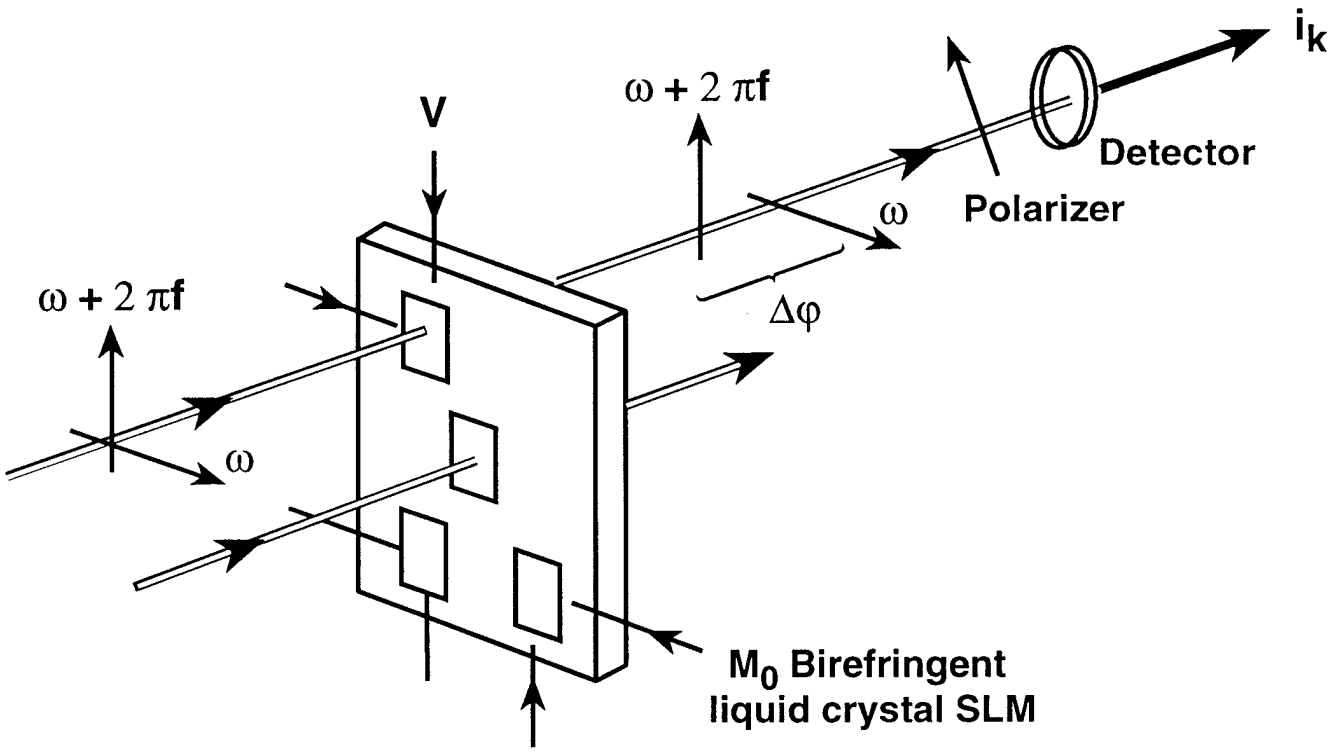
IMPLEMENTATION OF THE PHASE CONTROL



$$i_{ph} = i_o \cos\left[2\pi ft + \frac{2\pi}{\lambda} e\,\Delta n\,(V)\right] = i_0 \cos[2\pi ft + \Delta\varphi]$$

Transfer of the optical phase shift on to the RF signal

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Viewgraph

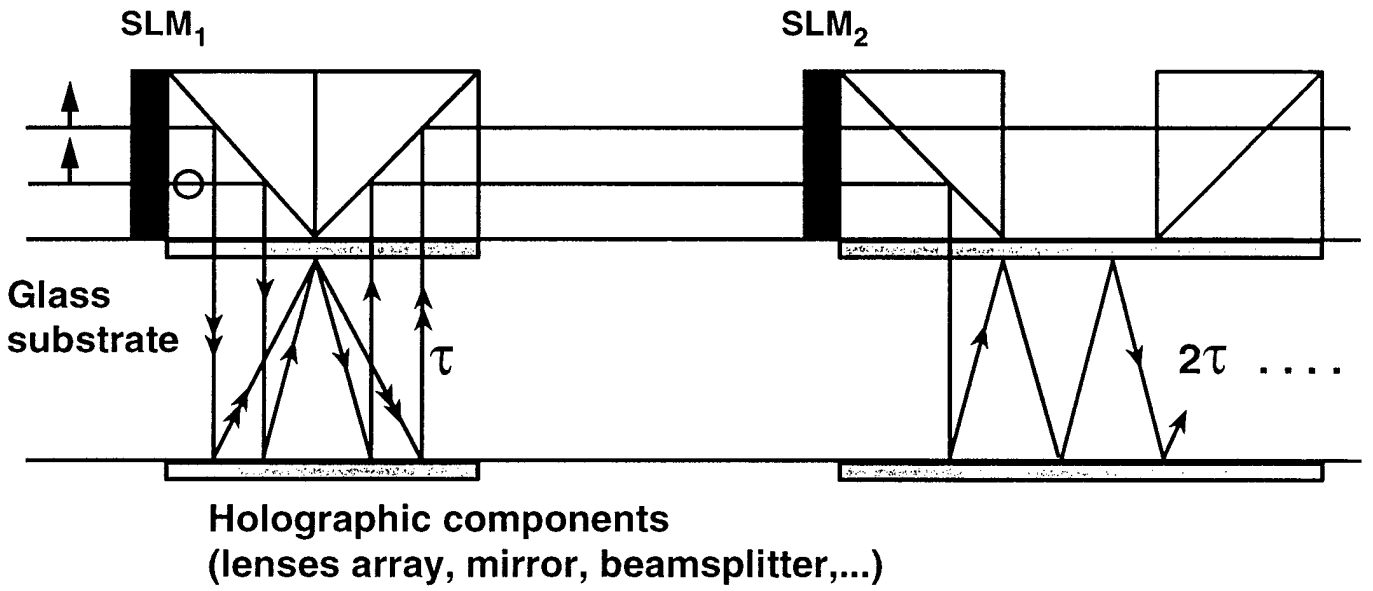
EXPERIMENTAL SET - UP

- Nematic liquid crystal SLMs (Thomson - LCD)
- Optical transmision: 95%
- 4 x 4 pixels (3.5 x 3.5 mm^2)
- Phase control precision : $\leqslant 5^\circ$
- Delay control:

  optical extinction ratio: $\approx$ 0.2% for each SLM (optimized thickness)

  : $\approx$ 1% for the complete architecture
- Computer controlled SLMs

COMPACT ARCHITECTURE



- Analogy with optical interconnects : holographic backplane technology

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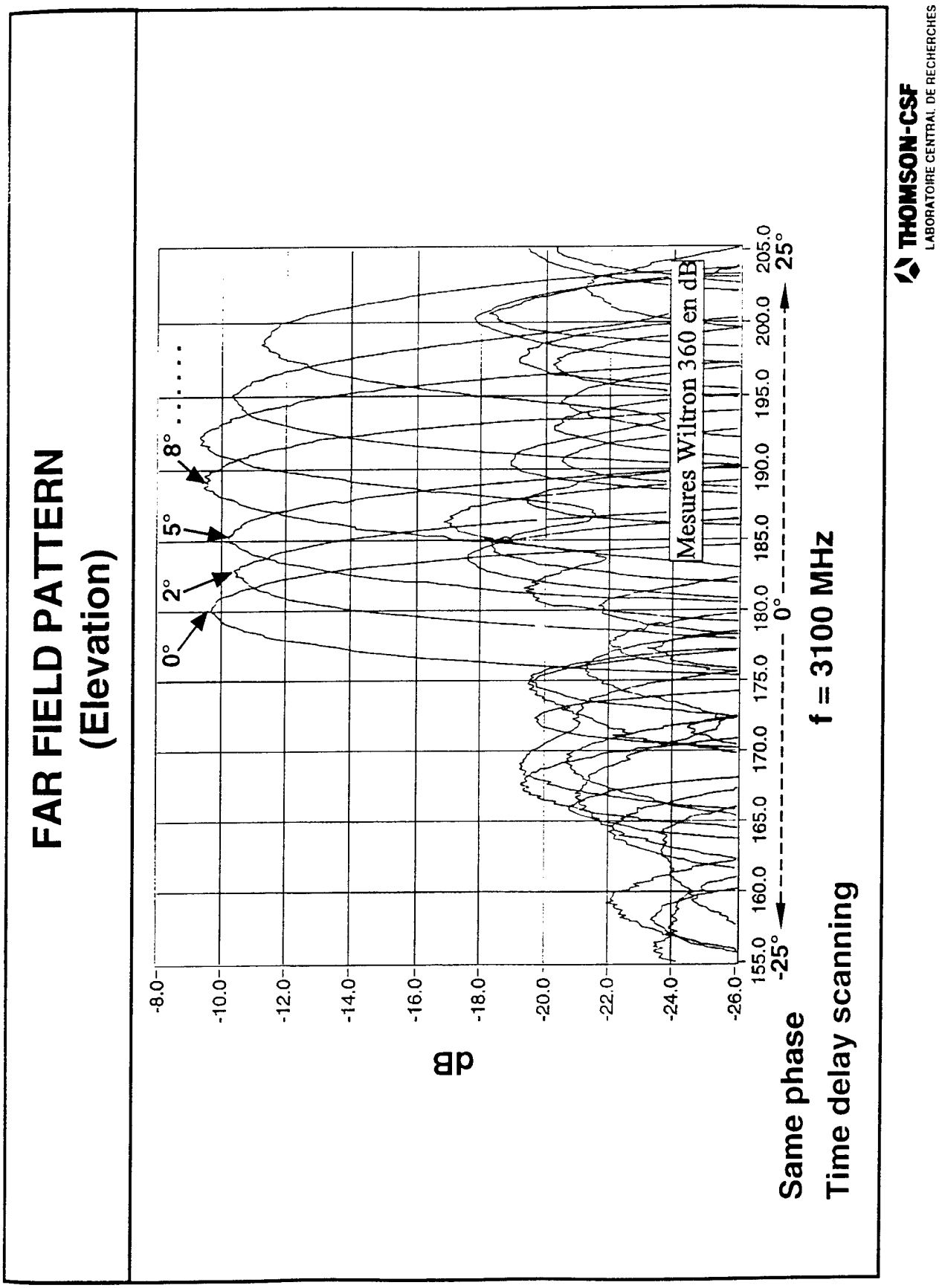
Viewgraph


FAR FIELD PATTERN
(Elevation)
0°
2°
5°
8°
Mesures Wiltron 360 en dB
dB
-8.0
-10.0
-12.0
-14.0
-16.0
-18.0
-20.0
-22.0
-24.0
-26.0
155.0
160.0
165.0
170.0
175.0
180.0
185.0
190.0
195.0
200.0
205.0
-25°
0°
25°
Same phase
Time delay scanning
f = 3100 MHz
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2

Non linear joint transform correlator

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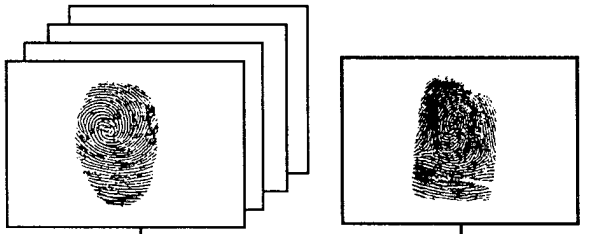
JOINT CORRELATION



Reference
R_i

Input
S

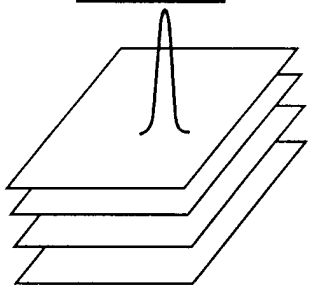
Fourier Transform Lens

$|\tilde{R} + \tilde{S}|^2$

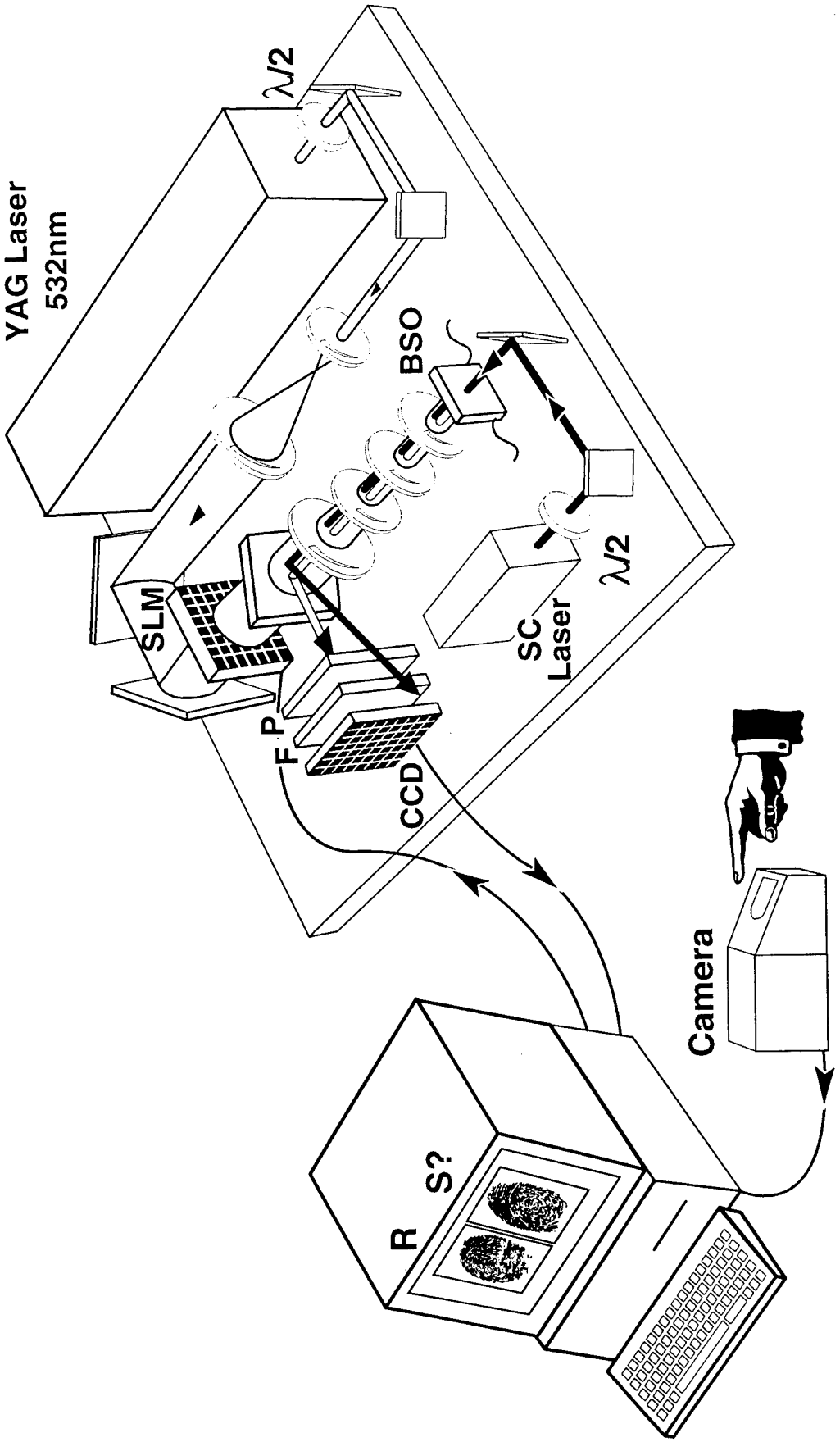
Photorefractive crystal: $\tilde{R}^2 + \tilde{S}^2 + \tilde{R}.\tilde{S}^* + \tilde{S}.\tilde{R}^*$

Inverse Fourier Transform Lens

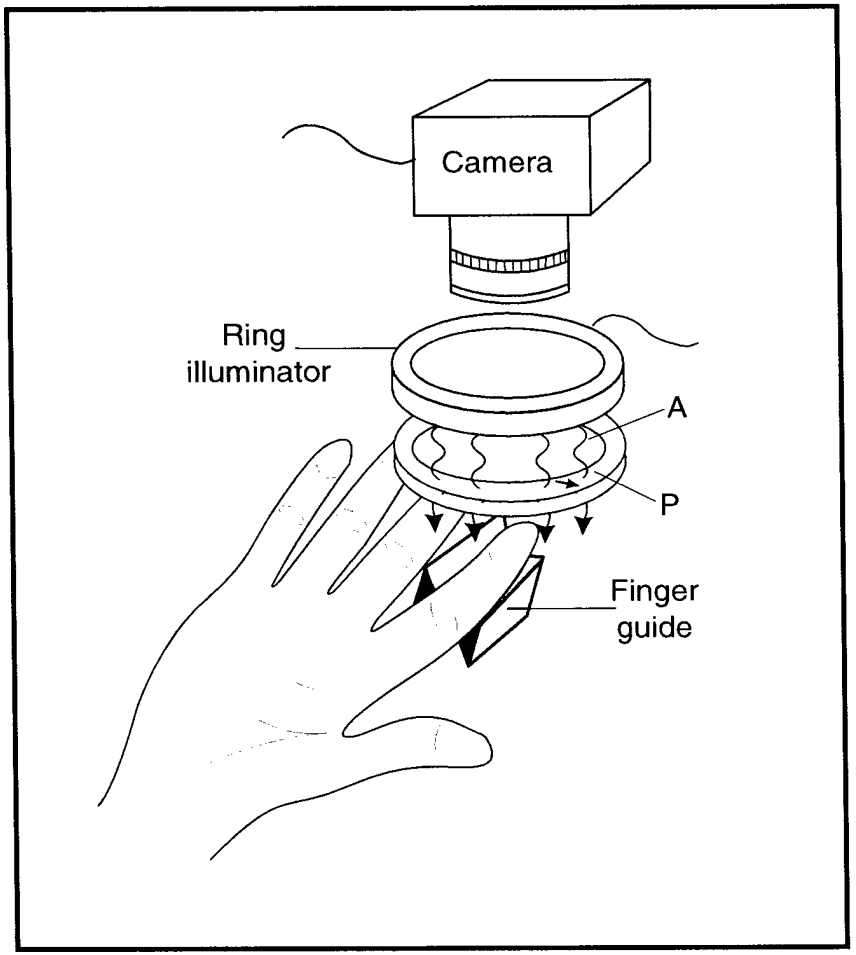
Detection plane : $R \otimes S$



Correlation


YAG Laser
532nm
λ/2
BSO
SLM
SC
Laser
λ/2
F
P
CCD
Camera
R
S?

Non-contact fingerprint sensor



- Nail-against-the-guide
- Polarized illumination
- Polarized detection
- Band-pass filtering : blue

Experimental results

- Data base : 10 individuals
- 2 independent acquisitions

→ Recognition rate : 100 %

→ False acceptance rate < 1 %

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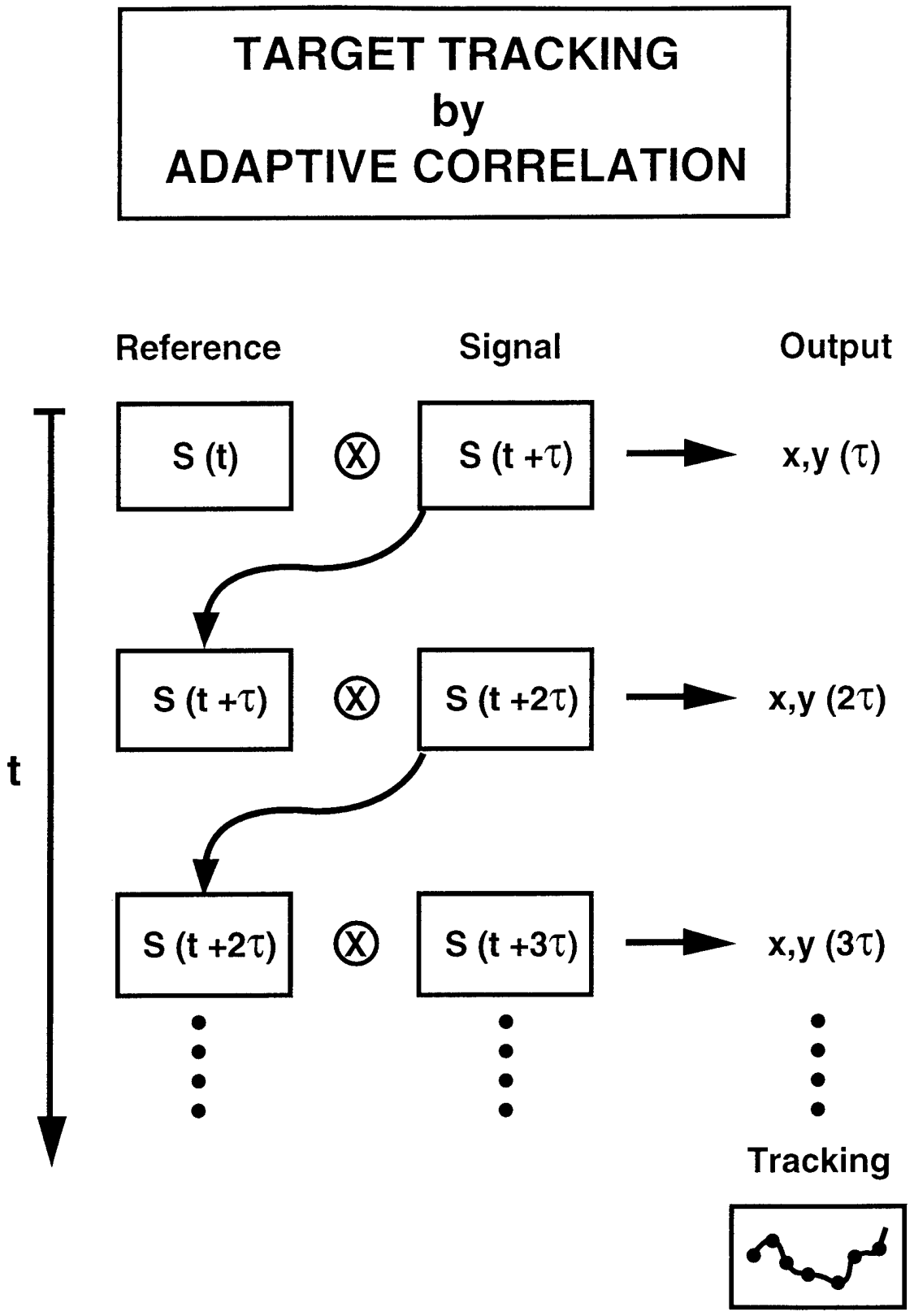
Viewgraph


TARGET TRACKING
by
ADAPTIVE CORRELATION
Reference
Signal
Output
S (t)
S (t +τ)
x,y (τ)
S (t +τ)
S (t +2τ)
x,y (2τ)
t
S (t +2τ)
S (t +3τ)
x,y (3τ)
Tracking
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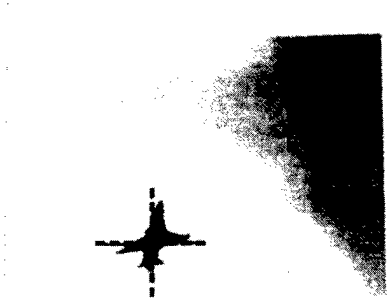
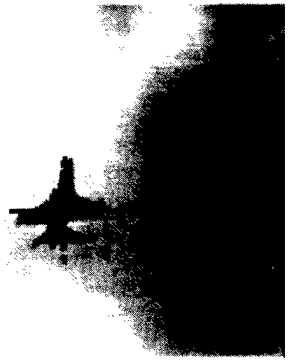
EXPERIMENTAL RESULTS

τ

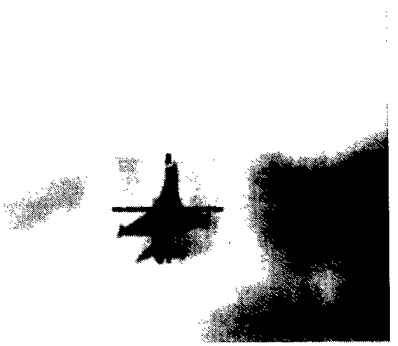


2τ

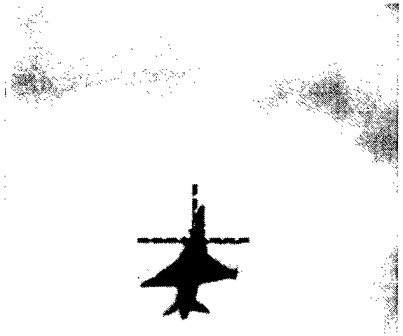


3τ

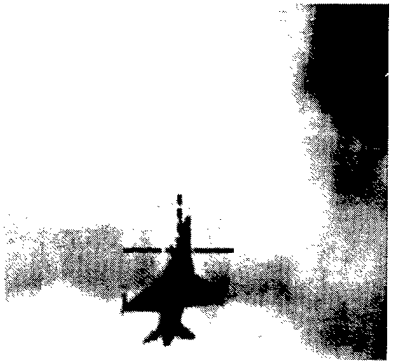
4τ



5τ



6τ



7τ

■■■■■■

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Viewgraph

3

Beam shaping of high-energy lasers

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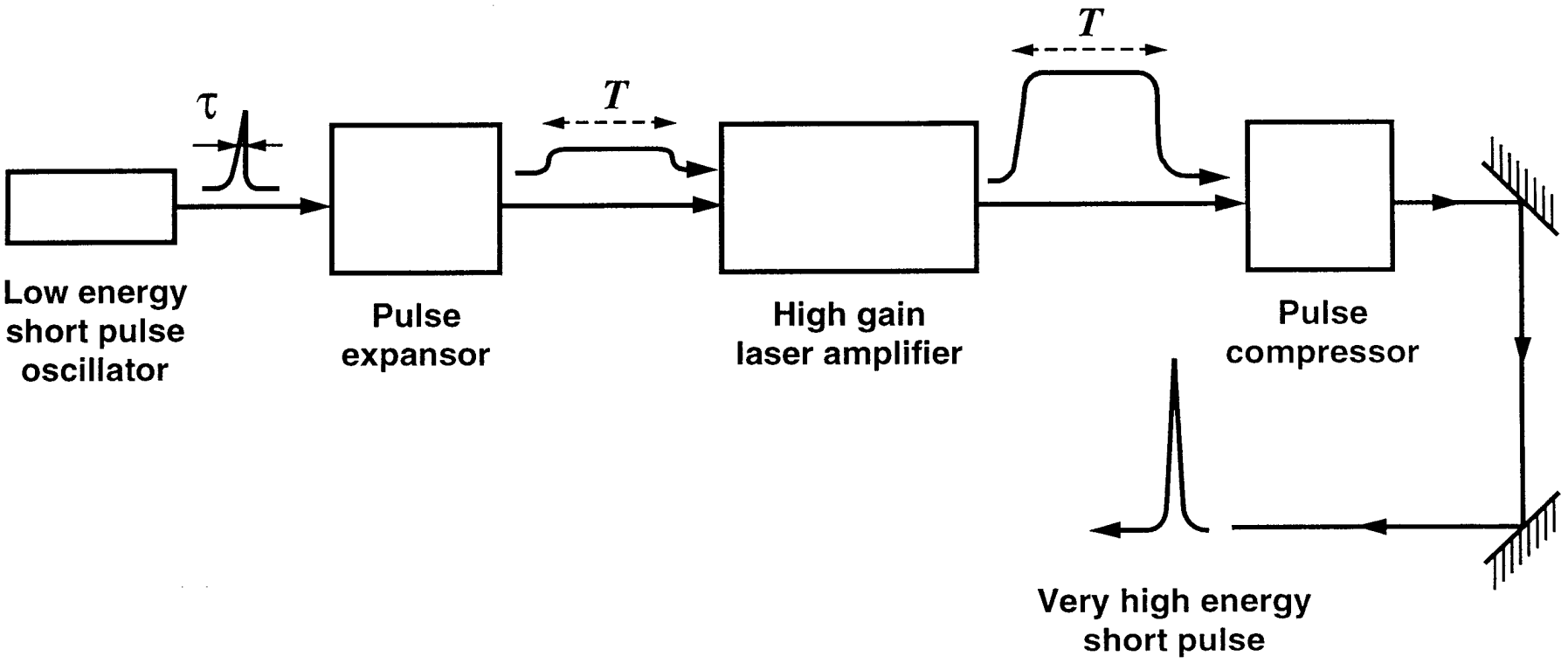
CHIRPED PULSE AMPLIFICATION - BASIC PRINCIPLE

D. Strickland - G. Mourou - Opt. Comm. 1985



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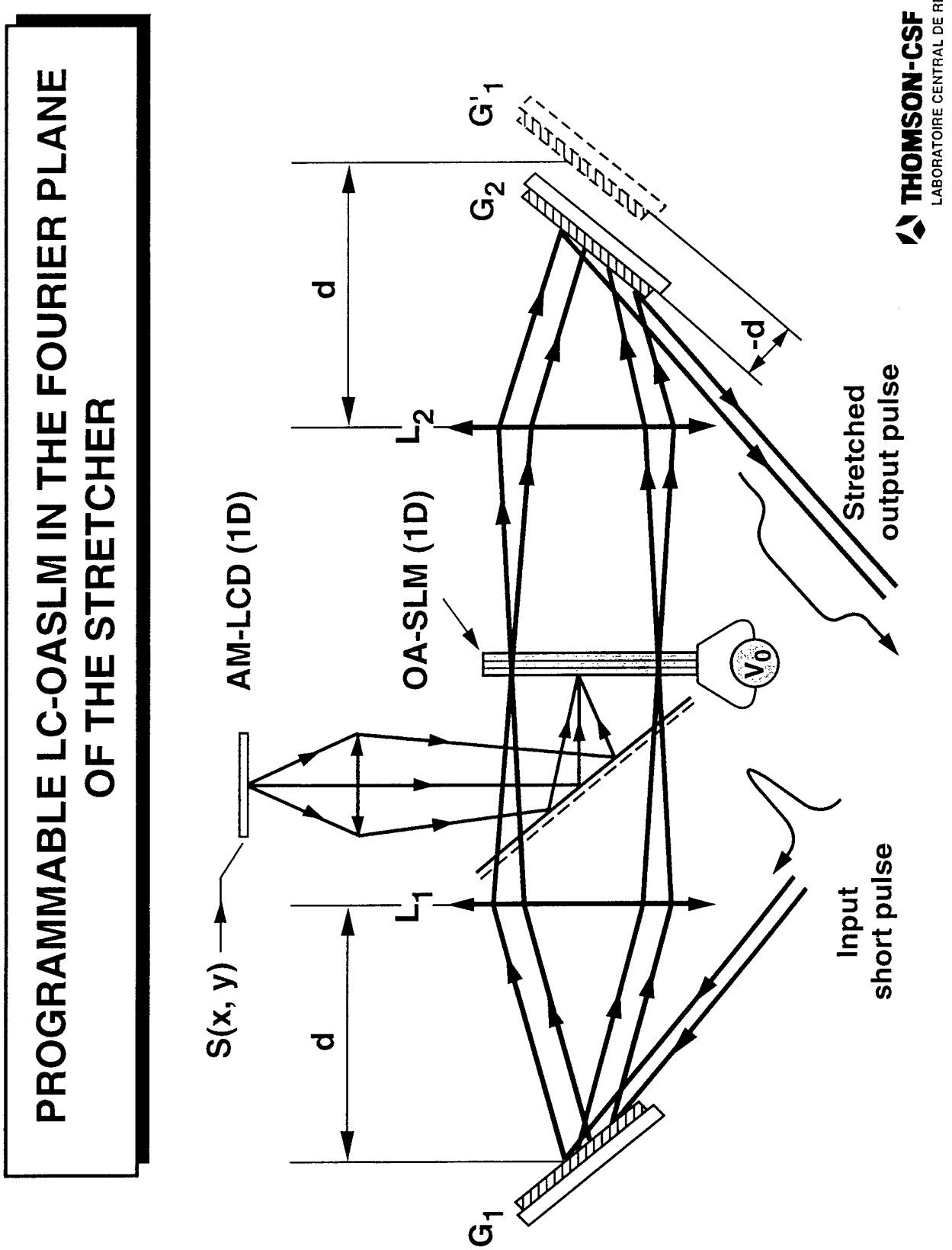
Viewgraph


PROGRAMMABLE LC-OASLM IN THE FOURIER PLANE OF THE STRETCHER
THOMSON-CSF
LABORATOIRE CENTRAL DE RECHERCHES
G'1
G2
d
-d
L2
AM-LCD (1D)
OA-SLM (1D)
V0
Stretched output pulse
S(x, y)
L1
d
Input short pulse
G1

Summary

- **SLMs for optically controlled antennas**
  - 2 D architecture based on polarization switch: phase and time delays
  - Prototype with 5 SLMs
    - → scanning : 0 - 20° , 2.7 - 3.1 GHz , no beam squint

- **SLMs for optical correlation**
  - Joint transform correlator with non linear photorefractive crystal
  - Compact 300 x 300 mm correlator
    - → fingerprint recognition with a non-contact sensor
      FAR < 1 % , RR = 100 % (10 individual database)
    - → target tracking with adaptive correlation

- **SLMs for beam shaping of high energy lasers**
  - Optically addressed SLMs
    - → compensation of the group velocity dispersion
    - → no damage at 300 mJ/cm2 - 10 nsec - 30 Hz (CLEO '97)

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Viewgraph

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EC (European Commision, ESPRIT)

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Multiple quantum well based optical correlator with tunable nonlinear response

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Abstract

The performance of a nonlinear joint transform correlator based upon an optically addressed multiple quantum well spatial light modulator is described. We show that the nonlinear response of the spatial light modulator can easily be tuned and demonstrate the utility of the system for face recognition.

Keywords

Nonlinear optical signal processing, optical correlators, quantum well devices, biometrics

Introduction

Optical correlators have, for over three decades, been considered as attractive alternatives to digital image processing for a variety of pattern recognition tasks.[1] Until recently however, there has been a lack of appropriate materials with which to implement these devices. A practical correlator requires an efficient, compact source of coherent light, a fast "optical memory" for displaying templates and, for joint-transform correlators, a sensitive, high resolution optically addressed spatial light modulator (OASLM). Recently, nonlinear joint transform correlators have been proposed as a way of enhancing the traditional architecture[2,3]. These devices require an OASLM that has a nonlinear response to light. In this paper we discuss a nonlinear joint transform optical correlator that uses a laser diode as the light source along with a GaAs/AlGaAs multiple quantum well optically addressed spatial light modulator (MQW-OASLM.)[4,5] We show that the nonlinearity of the MQW OASLM is easily tunable and that this tunability has important consequences for pattern recognition with these devices.

In a joint-transform correlator the Fourier transforms of the object and reference images are interfered on an OASLM while a third, read, beam is diffracted off the resulting hologram. This type of correlator has the advantage of being relatively robust and easy to align as compared to the Van der Lught geometry. It can also have an additional advantage

OSA TOPS Vol. 14 Spatial Light Modulators, 1997
Geoffrey Burdge and Sadik C. Esener (eds.)

when the response function of the OASLM is not simply linear. Nonlinear joint transform correlators (NLJTC) can offer better performance than linear correlators, providing automatic DC blocking among other features. When the response function of the OASLM is tunable these devices can act as an additional, programmable, processing step. This processing occurs at the response time of the OASLM which can be significantly faster than doing the processing via serial to parallel conversion of the image in the correlation plane followed by digital signal processing.

MQW OASLM Device

Nonlinear joint transform correlators have been demonstrated using bulk photorefractive materials such as $BaTiO_3$. These materials, though, have the disadvantages of being relatively insensitive to light and extremely insensitive to near infrared light. This means that near infrared diode lasers cannot be used as sources. Instead, much higher power visible sources such as argon-ion lasers are used. Even with these powerful sources the response times of bulk photorefractives are slow: typically milliseconds at best. In addition, because of the small index change in these materials, a volume hologram must be written to achieve reasonable diffraction efficiencies. Volume holograms, however, are less convenient than Raman-Nath holograms in optical correlator systems.

Optically addressed liquid crystal SLM's offer another option for correlator systems. These materials are more sensitive to light and do not require volume holograms, but fast switching materials, such as ferroelectric liquid crystals, offer no grey scale response.

Multiple quantum well based optically addressed SLM's are an attractive alternative to these other technologies. They are extremely sensitive to light. Depending on the mode of operation, a fluence of 100-500 nJ/cm^2 is sufficient to saturate the response[6]. This is approximately 10,000 times the sensitivity of bulk photorefractives and about 100 times the sensitivity of optically addressed liquid crystal SLM's. GaAs based MQW OASLM's are sensitive to write light at any wavelength shorter than about 850 nm. The read beam must be resonant with the GaAs exciton at about 850 nm, convenient for laser diode sources. The maximum operating rate of these devices is determined by the light intensity and the RC time. One cm^2 devices can operate a speeds of 1 MHz with sufficient illumination (about 1 W/cm^2). The resolution of the materials is high , with a modulation transfer function that drops to 50% at a grating spacing of about 5 μm. Device sizes of several square centimeters with good optical quality and uniformity are possible. Diffraction is in Raman-Nath mode as typical device thicknesses are on the order of a few microns.

MQW OASLM's can be fabricated in a number of ways. The device we used operated in a reflective mode.

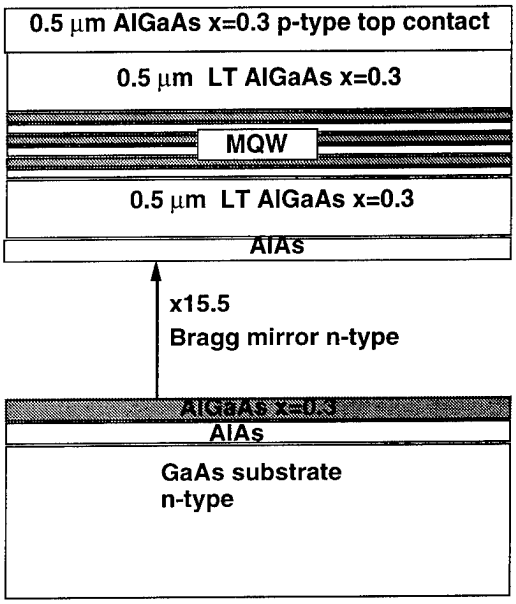

Fig 1

The structure of the MQW-OASLM is shown in Fig. 1. It was grown by molecular beam epitaxy on an n-type GaAs substrate. The structure consists of the following layers: a 15 period AlAs/AlGaAs Bragg mirror doped n-type, followed by a 0.5 μm low temperature grown AlGaAs trapping layer, followed by a 100 period GaAs/AlGaAs multiple quantum well, followed by another AlGaAs trapping layer and capped by a p-doped AlGaAs layer. The reflective geometry offers significant advantages over previous transmissive devices that have used etching or epitaxial lift-off in that, after growth, no further processing is needed. This greatly improves the optical quality of the material resulting in very low scatter. Electrical contacts are made to the top and bottom surfaces and a ±10 volt AC signal is applied. Details of the device performance and structure can be found elsewhere.[7]

MQW OASLM's work via light induced screening

of the applied electric field. The MQW layer acts as both a photodetector and the electro-optic medium. When a field is applied to the device, the position and magnitude of the heavy hole exciton absorption feature changes, resulting in both an absorption and index of refraction change near the band-gap of the material. When the device is exposed to write beams, photocarriers are created in the MQW layers which rapidly move across the device to screen the applied field. The presence, on either side of the MQW layers, of layers of trap laden low temperature grown (LTG) AlGaAs give the device its spatial resolution. Carriers that move into these layers, after having traversed the quantum wells, are trapped in about a picosecond. This prevents lateral drift, which would wash out the spatial pattern of screening created by the write beams. As the photocarriers screen the applied field in the illuminated regions, the heavy hole excitonic feature returns to its zero field state. Thus the absorption and index of refraction of the device becomes modulated in a pattern that mimics that of the write beams.

It is important to note that the time scale of this process is not set by the transit time of the carriers across the device (about 300 picoseconds), but rather the time it takes to store enough charge in the LTG layers to screen the applied field. Thus the rise time of the device is determined by the intensity of the write beams. When illuminated by a hologram, the diffracted order's intensity rises until the applied field is screened in the illuminated regions. It then falls as the darker regions also screen. Thus diffraction from these devices is always transient. The device is reset by driving it with a square wave voltage. A new diffraction pulse is produced for every voltage cycle.

The grey scale response of diffraction from these devices is determined by the light intensity, the drive frequency of the applied square wave and the nature of the detector which is used to observe the diffraction[8]. When using a detector that integrates over at least a drive voltage cycle, the grey scale is approximately linear for low writing intensities. That is the diffraction efficiency is approximately proportional to the writing intensity. For higher intensities, the diffraction efficiency saturates and then begins to drop exponentially. The saturation intensity at which this change in behavior occurs is determined by the drive frequency. The faster the applied voltage is cycled the higher the saturation intensity. The slope of the grey scale in the linear regime is also affected by the drive

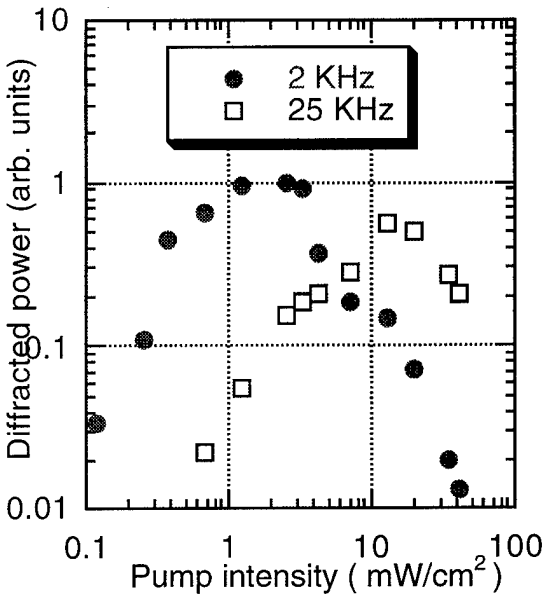

Figure 2

frequency. The grey scale for the MQW OASLM used in our experiments is shown for two different drive frequencies in Fig. 2.

Nonlinear joint transform correlator

We used the MQW OASLM to implement and test a tunable nonlinear joint transform correlator. A diagram of the experimental setup is shown in Fig. 3. A single mode laser diode operating at 849 nm is used for both the read and write beams. Because of the high sensitivity of the device only 200 μW of write beam power was necessary to drive the device at a frame rate of several kHz.

Both the reference and template images were high resolution transparencies. A 30 cm lens was used to create the Fourier transform hologram in the correlation plane on the MQW OASLM. A weak read beam was diffracted off the hologram. The read beam was inverse–Fourier transformed by a second lens onto the detection plane at which there was a high resolution CCD camera.

To study the tunability of the NLJTC we examined the problem of face recognition. This is a current

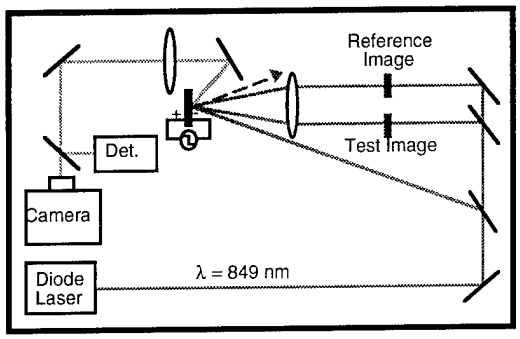

Figure 3

problem in biometrics with a variety of security applications.

In prior theoretical work we predicted that the discrimnation of a MQW NLJTC for different faces could be changed by adjusting the SLM drive

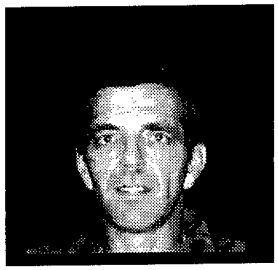

Figure 4 a

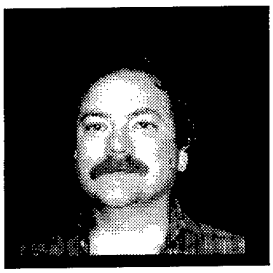

Figure 4 b

frequency.[9] This occurs because faces are complex objects with a wide range of spatial frequencies and intensities in the correlation plane. The brightest intensities tend to be near the center of the correlation plane, at low spatial frequencies. While the higher spatial frequencies tend to be weaker in intensity. By adjusting the grey scale of the MQW OASLM to be sensitive to certain intensity ranges we can emphasize or de-emphasize the importance of the lower or higher spatial frequencies.

Figure 4 a and b shows the two input faces, A and B, that were used for correlation. Fig 5a shows the auto-correlation spot of face A correlated to itself. The correlation spot was attenuated by a factor of 7. Fig 5b shows the unattenuated cross-correlation of face A to face B. Both correlations were done at a drive frequency of 4 kHz. At this drive frequency, where higher spatial frequencies are emphasized, the correlator can clearly distinguish the differences between the two faces.

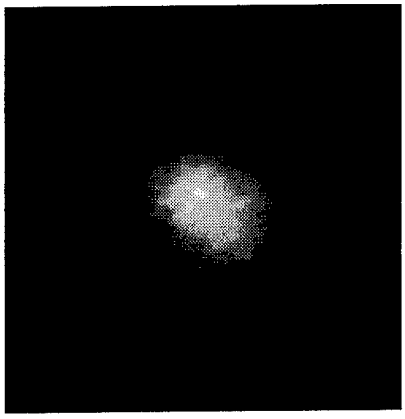

Figure 5a

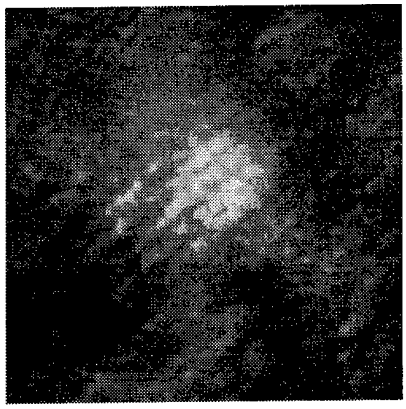

Figure 5b

The effect of varying the drive frequency is shown in Fig 6. Here the value of the correlation is determined by integrating the power in the correlation spot. Both the auto and cross correlations are displayed. The auto-correlation is strongly peaked at a drive frequency of 4 kHz. At this frequency the device is sensitive to the large area of the Fourier plane containing the higher spatial frequencies of the face. The cross-correlation is relatively flat with frequency. This is because faces A and B share fewer of the same high spatial frequency features but more of the same low frequency features (the overall shape of the face, for example). These lower spatial frequencies become more emphasized at higher drive frequencies and, so, the correlation drops

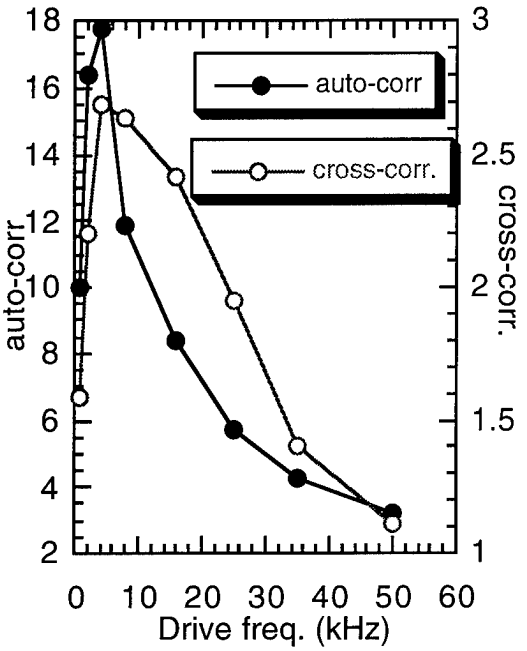

Figure 6

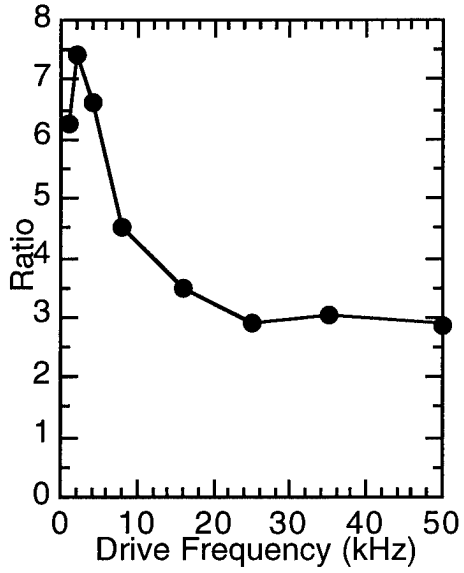

Figure 7

off less rapidly.

Because of this difference in behavior, the discrimination of the correlator between faces can be tuned simply by changing the drive frequency of the device. This is shown in Fig. 6 which displays the ratio of the two graphs in Fig. 7 as a function of frequency. This ability to quickly tune the discrimination could be important in several applications. For example correlation at high driving frequencies could be used to pull out face-shaped objects from a scene. This can be followed rapidly by correlation at lower driving frequencies to identify a particular face. We observed similar results when comparing correlations of profiles and other facial views.

Discussion

Optical correlation has held a great deal of promise for many years, but this promise has not been realized due to the unavailability of appropriate materials. Over the past decade, however, and particularly over the last five years developments in several areas have provided the necessary elements for all-optical processing. For optical sources, laser diodes have provided compact, highly efficient sources of coherent light. For generation of template images, ultra-fast electrically addressed MQW SLM's can provide 256x256 6 bit images at frame rates of hundreds of kilohertz.[10] Optically addressed MQW OASLM's, such as the device described here, offer both incoherent to coherent conversion and nonlinear mixing in the correlation plane at rates up to 1 MHz. Finally, smart pixel arrays can be used for fast thresholding detection in the detection plane. In combination all these elements can provide pattern recognition at rates orders of magnitude faster than digital computer techniques.

Conclusion and future directions

We have examined the performance of nonlinear joint transform correlator based upon an optically addressed multiple quantum well spatial light modulator. The tunability of the nonlinearity in this device allows us to easily and rapidly change the discrimination of the correlator.

Having demonstrated the utility of this system for static templates, we have begun work with a time varying input template and detection of the correlation signal using a fast detector. Preliminary data indicates that correlation at high speeds is possible with modest write light powers. Thus a future system using a fast electrically addressed SLM or other optical memory as input should allow correlations at a rate of several thousand to tens of thousands per second.

Acknowledgements

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Detection and Classification of Structural Defects on Textured Surfaces

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Abstract

In many industrial fabrication processes high-speed automated vision systems are needed in order to control certain product properties. A typical case is the real-time inspection of textured materials. Here, the amount of generated data and the computational complexity of applicable algorithms are usually such that current digital image processing systems are not able to fulfill the speed requirements. Optical processors offer a promising alternative to overcome current speed limits.

The scope of this paper is a concept based on wavelet theory for the design of diffractive filter elements and their application in an optical $4f$-processor in order to detect or classify certain structural deviations in textures. Critical points in this respect are the indeterministic natures of the "correct" textures themselves as well as of the occurring "defect structures", the fact that defect shapes and sizes are not among the a-priori knowledge, and the low energies, compared to the surrounding texture, that are contained in signals representing defects. These questions will be addressed using theoretical methods and computer simulations. Optical filtering experiments involving spatial light modulators will be presented.

Key Words

Optical correlators, pattern recognition and feature extraction, wavelets, visual inspection of technical objects

Introduction

Industrial products are defined and characterized by certain properties such as size, shape, surface structure, etc. A major goal of an industrial fabrication process is to ensure the fast replication of these product properties with sufficient accuracy. Visual inspection of the fabricated items is a powerful means to control the accuracy and so gather information that can be used to determine necessary adjustments within the fabrication process.

A widespread problem is the examination of structured surfaces of "endless" materials that are transported at high speeds, such as breadths of cloth, carpet, paper, plastic foil, or the like. These materials possess surface textures that are characterized by a certain global regularity but also by slight local variations of indeterministic nature. Fabrication errors can be identified as structures that violate the global regularity. Examples for common cloth textures carrying typical fabrication errors are depicted in figure 1.

The examination procedure can be divided into the detection and the classification of defects. Whereas the primary objective of the detection is to localize all irregularities, the latter part refers to the distinction of different defect types.

Correlation filters [3] implemented by diffractive elements in a $4f$-processor represent a powerful concept in image analysis. They have been proven useful for the recognition of objects in "low-noise" image scenes. Yet, their use for defect recognition in textured surroundings leads to poor results [8]. Because defects are not known beforehand, they can only be extracted from sample image data. Unfortunately, neither the error images nor the underlying textures are deterministic, which leads to a low recognition performance. In addition, signals representing defects are usually very weak compared to the background (i.e. the texture image).

Wavelet filtering [2] is typically used to analyse images in space and frequency domain to obtain features for a subsequent classification process. Wavelet correlation filters (WCFs) [6,8] combine the abilities of both filter types. So far, they have been used to enhance the

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discrimination abilities of correlation filters [6]. The application of wavelet filters and WCFs for detection purposes in textured images is novel and will be discussed in the following paragraphs.

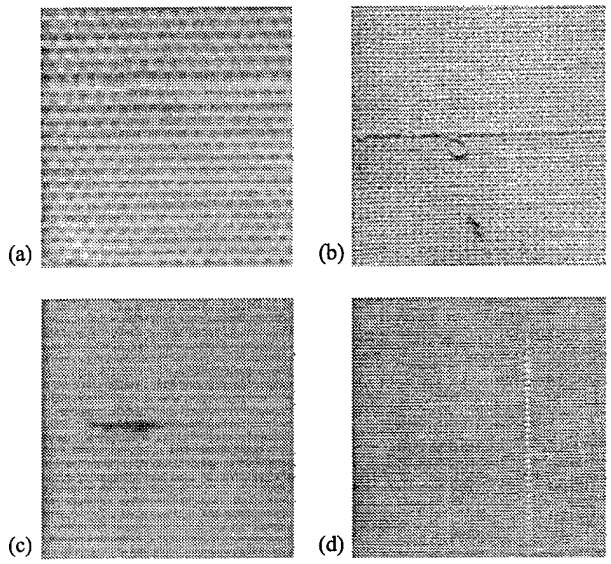


Figure 1. Several cloth textures carrying fabrication errors. Images: courtesy of Fraunhofer Institut für Industrieanlagen und Produktionstechnik, Berlin, Germany

Signal Analysis

In principle, textures could be subject to arbitrary statistical variations. Real-world materials and production conditions, though, justify the assumption that the relevant textures are characterized by a limited range of spatial frequencies and, in some cases, by a certain orientation. The same is valid for signals that typically indicate features that have to be classified as "defects". Due to this fact it is possible to extract textures from images by space-frequency analysis methods. We want to show that the wavelet transform is a suitable method in this case.

The wavelet transform $\mathcal{W}_\psi s$ of a two-dimensional signal s is defined by

$$(\mathcal{W}_\psi s)(\vec{b}, a, \phi) = \frac{1}{a} \int_{\mathbf{R}^2} s(\vec{x}) \overline{\psi_{\vec{b},a,\phi}(\vec{x})}\, d\vec{x}. \qquad (1)$$

Verbally, this means that the signal $s(\vec{x})$ is compared to shifted, scaled, and rotated versions

$$\psi_{\vec{b},a,\phi}(\vec{x}) = \frac{1}{a}\psi\left(\frac{\mathbf{R}_\phi(\vec{x}-\vec{b})}{a}\right) \qquad (2)$$

of the so-called mother wavelet $\psi(\vec{x})$, and the results are displayed as a function of the respective affine operations: translation by $\vec{b}$, scalation by a, and rotation by ϕ. The definition of a wavelet requires that $\psi(\vec{x})$ fulfils the admissibility condition

$$\int_{\mathbf{R}^2} \frac{|(\mathcal{F}\psi)(u)|^2}{|u|} < \infty, \qquad (3)$$

where $\mathcal{F}$ indicates the Fourier transform. Thus, $\psi(\vec{x})$ possesses a bandpass property.

The crucial step towards an optical implementation is that, for fixed a and ϕ, equation (1) can be written in the form of

$$\begin{aligned}(\mathcal{W}_{\psi_{a,\phi}} s)(\vec{b}) &= \frac{1}{a}\int_{\mathbf{R}^2} s(\vec{x})\overline{\psi_{a,\phi}(\vec{x}-\vec{b})}\, dx \\ &\propto (s * w)(-\vec{b}), \end{aligned} \qquad (4)$$

where $w(\vec{x}) = \overline{\psi_{a,\phi}(-\vec{x})}$. Hence, the wavelet feature $s_w = \mathcal{W}_{\psi_{a,\phi}} s$ can be obtained by a convolution operation as is performed by a $4f$-setup with impulse response w under coherent-optical conditions. The basic setup is depicted in figure 2.

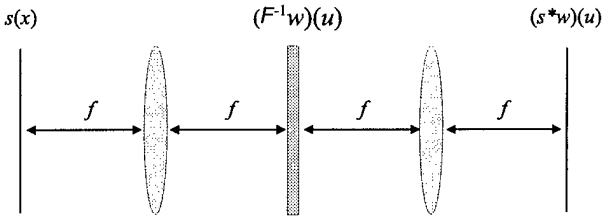


Figure 2. $4f$-system with impulse response $w(\vec{x})$.

In order to provide a recognition functionality for certain features, the autocorrelation $s_w \otimes s_w$ can be produced if the original signal s is present in the input plane of the $4f$-setup. In this case, the impulse response has to be chosen as

$$w(\vec{x}) * \overline{s(-\vec{x})} * \overline{w(-\vec{x})}. \qquad (5)$$

The corresponding filter with the transmission function

$$W(\vec{u})\overline{S(\vec{u})W(\vec{u})}, \qquad (6)$$

where the uppercase letters indicate the respective Fourier-transformed functions, is called wavelet matched filter (WMF) [6].

Let $S(\vec{u}) = A(\vec{u})\exp(i\Phi(\vec{u}))$, with phase and amplitude distribution $\Phi(\vec{u})$ and $A(\vec{u})$. In analogy to conventional fractional power filters [3] the filter transmission function stated in (6) can be replaced by

$$W(\vec{u})\overline{A^p(\vec{u})\exp(i\Phi(\vec{u}))W(\vec{u})} \qquad (7)$$

to define the wavelet fractional power filters (WFPFs). If the fractional power p takes on the values 0 or -1,

the wavelet phase-only filter (WPOF) and the wavelet inverse filter (WIF) are generated, respectively.

Defect Detection

According to the remarks of the preceding section, our first step in the design of a filter for a specific application is to select the mother wavelet. For all following considerations, the base function will be the so-called Mexican-Hat-wavelet. The rotational-symmetric version is defined by

$$\psi(r) = (1 - r^2)e^{-\frac{r^2}{2}}, \quad r = |\vec{x}|. \tag{8}$$

It "computes" the second derivative of the processed signal, which is a useful property, as will be demonstrated, and its bandpass characteristic is very smooth. Figure 3 shows the respective space and frequency domain representations of $\psi(r)$.

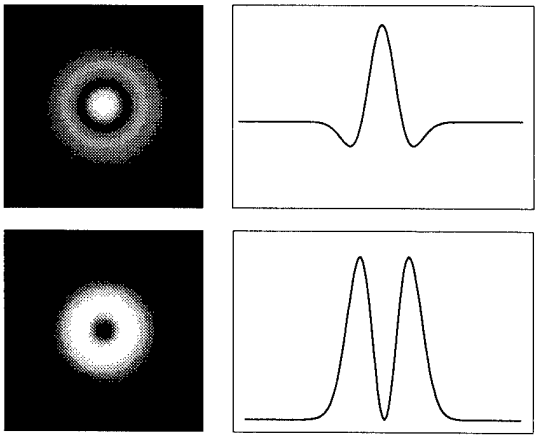


Figure 3. Mexican-Hat-wavelet. Upper row: space domain respresentation. Lower row: frequency domain representation

Since, in a first approach, isotropic (i.e. rotational-symmetric in the two-dimenstional case) wavelets are chosen, only an appropriate scale parameter a has to be determined. A systematic approach to do this is a multiresolution analysis (MRA). A finite set of impulse responses ψ_{a_i} is generated by varying a according to a dyadic series. The filter with the best suppression of the texture and best response to defects is selected for implementation.

Figure 4 shows the results of a MRA for the sample texture image from figure 1(b). The filter in row (c) can be used to detect the defects. Of course, it detects all defects of the same scale range, it does not distinguish between them. But for many applications, this is just the desired function.

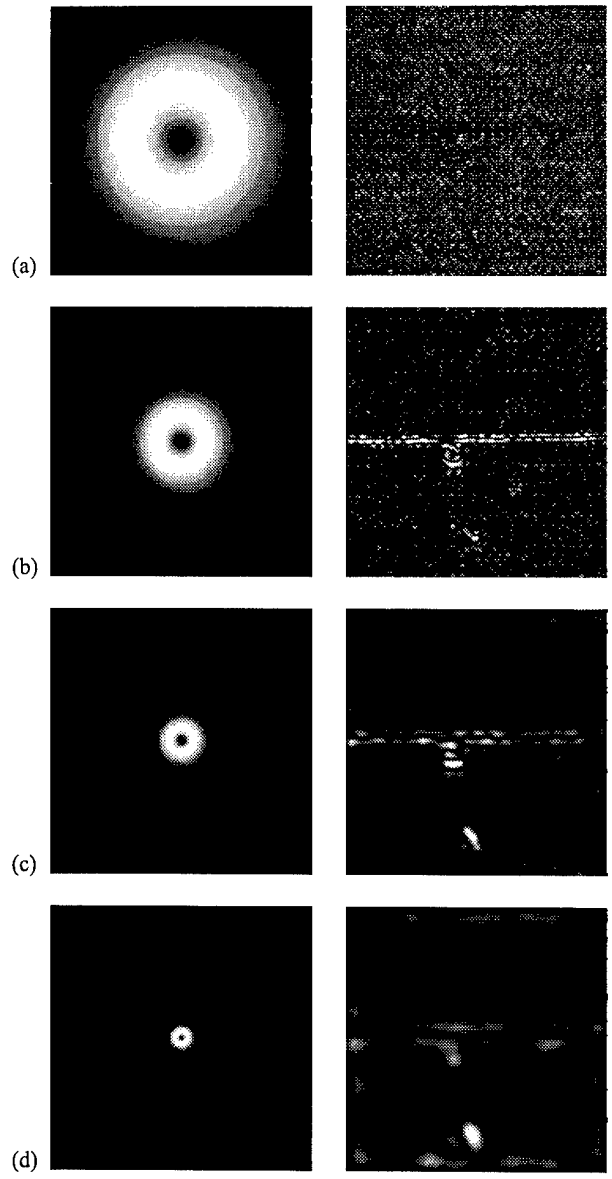


Figure 4. Multiresolution analysis of the texture image of figure 1(b) on a dyadic scale series. Left: filter transmissions. Right: respective system outputs.

Defect Classification by Directional Information

The only a-priori knowledge we have used so far is the frequency content of the underlying texture. If a distinction between different defect types is the goal, a more sophisticated approach is necessary: knowledge about the defects themselves must be considered. For the applications we are focused on, the examination of textile webs, this knowledge can have the form of directional information. Long horizontal structures, for example, usually indicate threads that were not properly

inserted. They are critical for the fabrication process. Other irregularities might be harmless.

The MRA based on isotropic wavelets as described in the previous section partitions the Fourier spectrum without making use of this information. However, since frequency domain directions correspond with space domain directions, it is possible to separate defect classes by partitioning the spectrum with separable wavelets. Consider the mother wavelet

$$\psi(\vec{x}) = (1 - x^2)\, e^{-\frac{x^2}{2}}\, e^{-\frac{y^2}{\sigma^2}}, \quad \vec{x} = \begin{pmatrix} x \\ y \end{pmatrix}, \qquad (9)$$

a "one-dimensional, horizontal" Mexican-Hat-wavelet. The "vertical extent" σ can be used to adjust its sensitivity to directional deviations in the examined features. The "wavelet direction" can be changed by rotating the (x, y)-coordinate-system. Figure 5 shows filter transmissions that partition the Fourier spectrum into the standard set [2] of a low-pass section and bandpass sections that correspond with horizontal (c), vertical (b), and diagonal (d) directions. Here, the scalation parameter has been chosen as previously determined by the isotropic MRA in order to match the defect scales. The respective system outputs for the sample texture image are depicted in figure 6. Clearly, several possibilities to distinguish between different defect types are demonstrated.

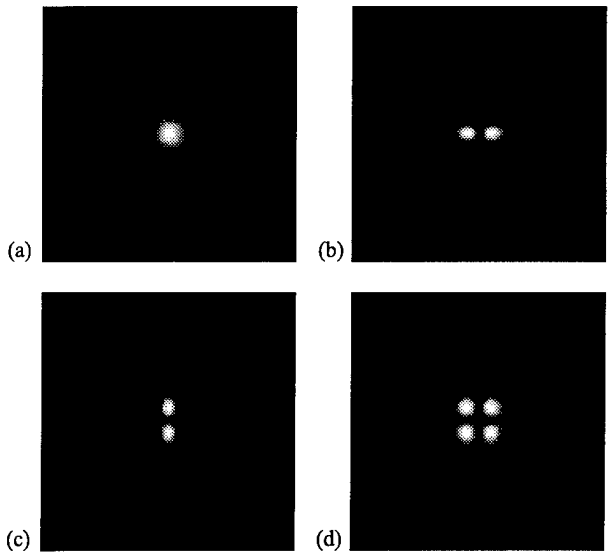


Figure 5. Filter transmissions that partition the Fourier spectrum into a low-pass section and bandpass sections that correspond with (a) vertical, (b) horizontal, and (c) diagonal directions.

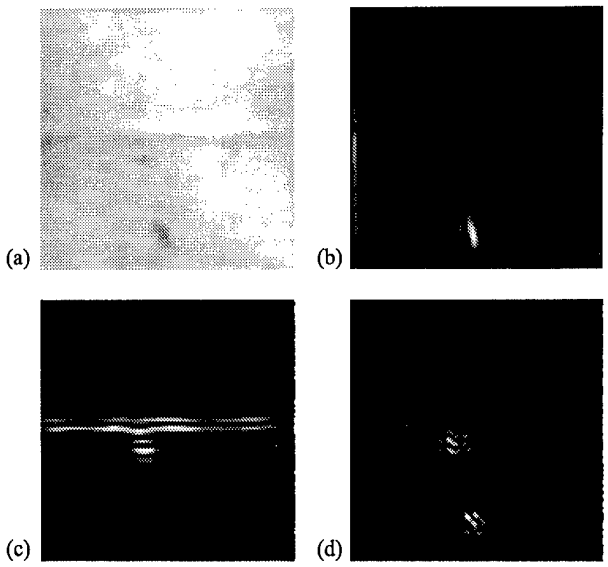


Figure 6. Defect classification: System outputs for the sample texture image from figure 1(b) and the filters displayed in figure 5.

Defect Classification by Shape Information

Of course, the most important and most expressive kind of information that can be exploited in a recognition process is the shape of a potential defect. Suppose the task is to find a sling structure like the one in figure 7.

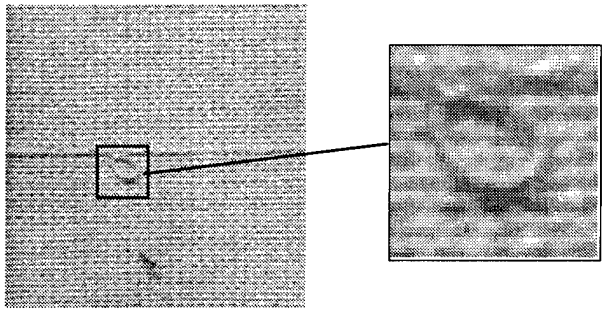


Figure 7. Defect example for a shape-based recognition.

For a number of reasons, it is not sensible to extract the displayed sling from the image and use it as a template for the design of a recognition filter. First of all, this sling is only one specimen for all sling-like features that are to be detected. Others may show minor deviations from this special shape that might influence the recognition process in a negative manner. Furthermore, the relevant image section contains information that is not important for the recognition, i.e. the un-

derlying texture. Finally, the energy contained in the defect signal is very low compared to the energy of the surrounding texture. Consequently, a conventional design will result in a recognition filter that responds not only to the defect itself but also to the texture [8].

If the shape information cannot be generated from image samples, the only way is to make a model for the typical defect. Consider the constellation in figure 8. It contains the sample defect and a primitive model for a shape generalization on the left. The corresponding wavelet features produced by the isotropic wavelet filter from figure 4 are displayed on the right. The similarity between the filter responses is a promising hint that a correlation of the wavelet features will lead to a good result. The use of a WCF for this classification problem is the logical consequence.

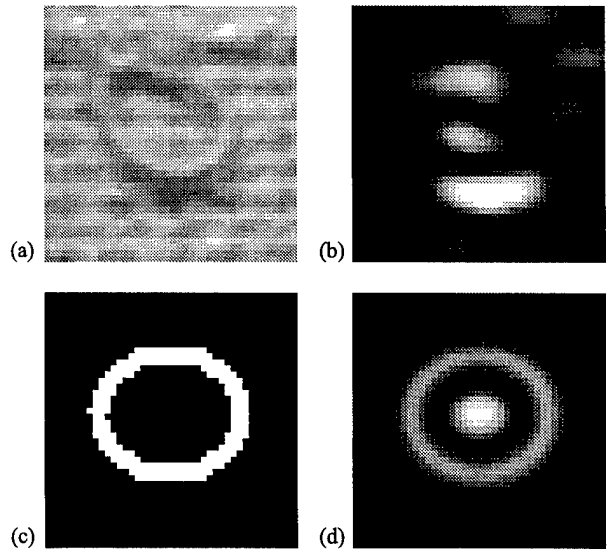


Figure 8. Left: defect example and model. Right: respective responses of the isotropic wavelet filter from figure 4(c).

On the basis of the isotropic Mexican-Hat-wavelet in figure 4(c) a WPOF has been computed according to (7) using the sling model as a template. The continuous filter amplitude and phase transmission is depicted in figure 9. Figure 10 shows the filtered sample texture image with a correlation peak at the correct position.

Filter Design

It is well known that neither static nor dynamic diffractive elements with a continuous complex transmission function as it would be necessary for the mentioned WPOF can be fabricated. In order to physically implement the filter a quantized amplitude or phase transmission that realizes the same optical function is required.

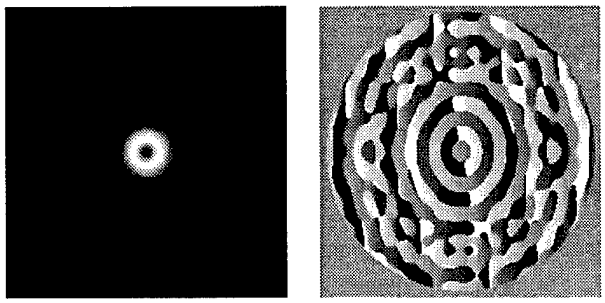


Figure 9. Wavelet phase-only filter for the sling-shaped defect. Left: amplitude transmission. Right: phase transmission.

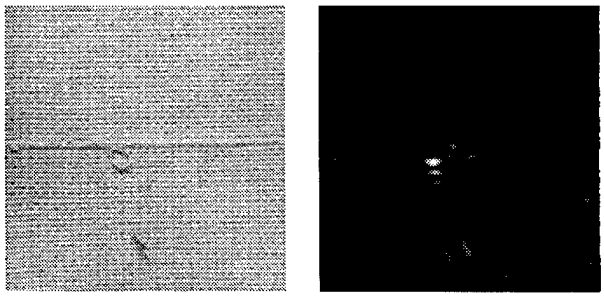


Figure 10. Sample texture image and corresponding response of the wavelet phase-only filter.

Iterative encoding methods [4] could be used to find such a function with good performance. However, these methods partly sacrifice the space-bandwidth-product in order to realize the optical function correctly. Considering a filter implementation on SLMs with a finite number of pixels, we suggest a different solution.

We have binarized the filter amplitude transmission using the Floyd-Steinberg algorithm [1]. The WPOF phase distribution has been hardclipped to four levels. A "sandwich" consisting of a binary amplitude-modulating element and a phase-modulating SLM can be used to implement the quantized transmission function. The Figures 11 and 12 display the new filter transmission and the result of the filter operation.

Optical Experiments

The proper optical function of the described diffractive elements can only be achieved in a coherent-optical regime. Spatial light modulators are required to perform the conversion of an incoherently illuminated real-world scene into a coherent image. We have examined two possibilities.

The incoherent scene can be imaged directly onto the write side of an optically addressable SLM like the

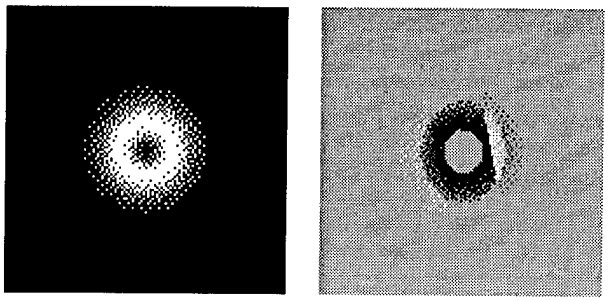


Figure 11. Quantized wavelet phase-only filter for the sling-shaped defect (magnified images). Left: amplitude transmission. Right: phase transmission.

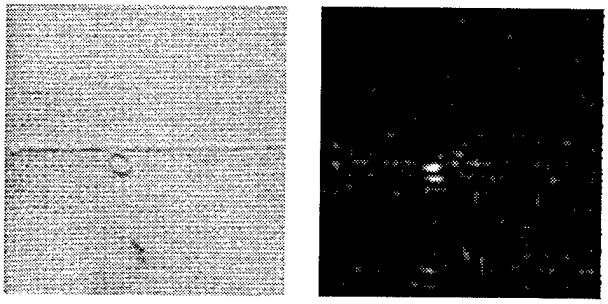


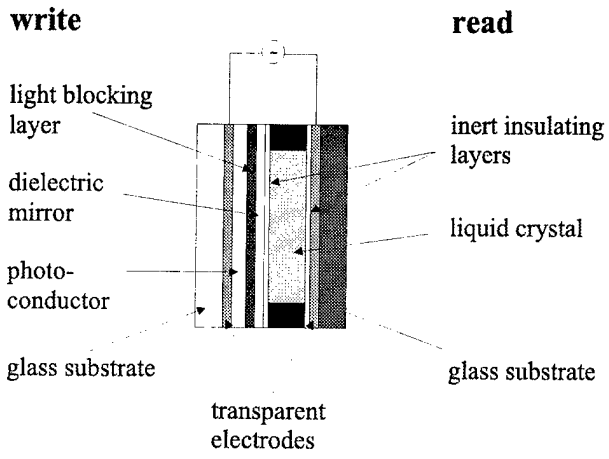
Figure 12. Sample texture image and corresponding response of the wavelet phase-only filter.

one depicted in figure 13. A coherent plane wave that impinges on the read side is then modulated according to the write side distribution. Figure 14 shows several texture samples with fabrication errors, the images obtained by the incoherent-to-coherent conversion using the OASLM, and the results of a filter experiment with an isotropic Mexican-Hat-wavelet that has been implemented on photographic film.

The second possibility is to use a CCD camera in order to record the image scene and display it on an electrically addressable SLM which can be illuminated by coherent light. Our experiments have been carried out on a Sanyio EASLM. Figure 15 demonstrates the excellent quality of the filtered images.

Conclusion

Focused on the automated visual inspection of textured materials, we have presented a signal analysis concept based on wavelet theory that can be implemented on an optical correlation processor. It has been demonstrated that space-frequency analysis methods are useful for detection as well as for classification purposes in textured images. Different forms of spectrum partitioning and the concept of wavelet correlation filters yield good results under practical conditions. Some results have been obtained by computer simulations only. However, we have implemented the wavelet filtering for defect recognition on an optical $4f$-setup. The results show excellent coincidence with computer simulations.



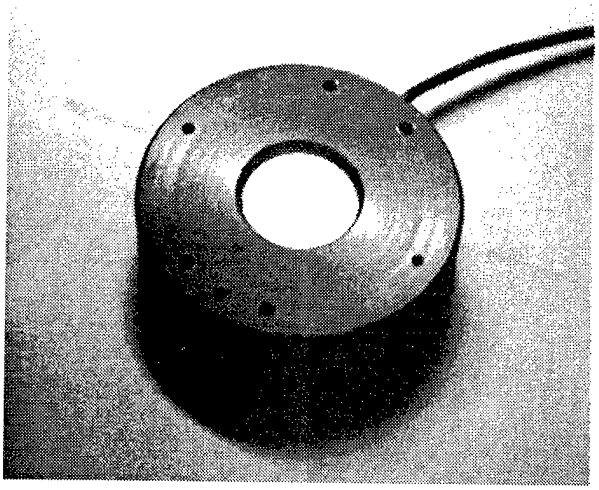


Figure 13. Technical sketch and photograph of the optically addressable SLM that has been used for the incoherent-to-coherent-conversion. Manufacturer: Jenoptik Technologie GmbH, Germany.

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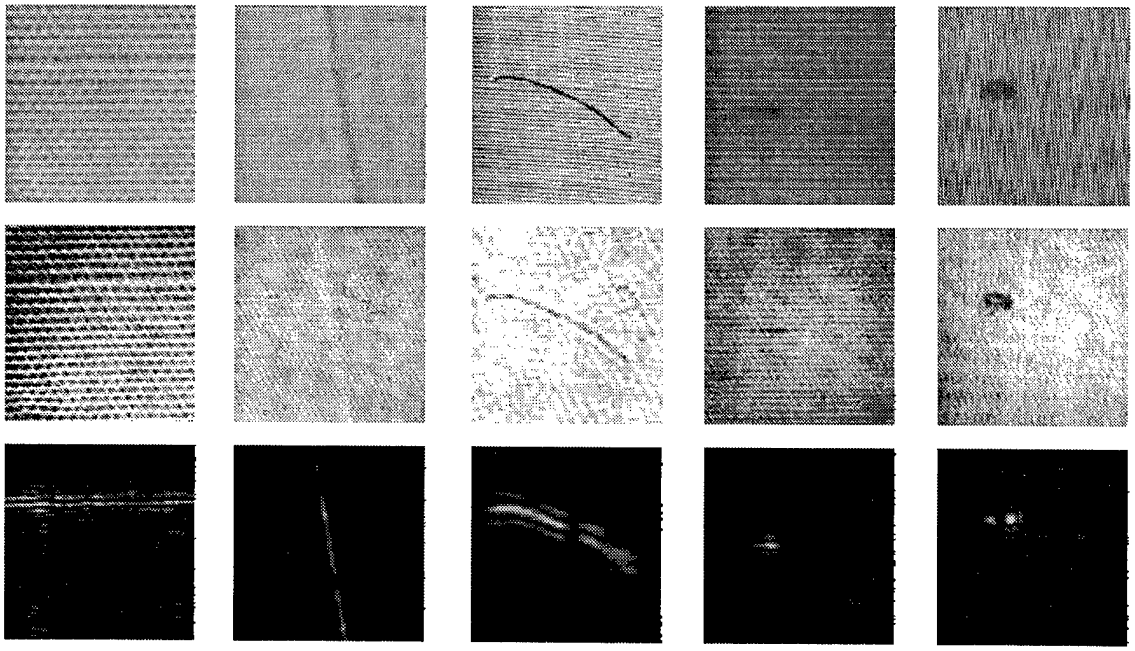

Figure 14. Defect detection with OASLM. Upper row: cloth samples carrying defects. Center row: coherent images on the OASLM read side. Lower row: optically obtained wavelet filtered images.

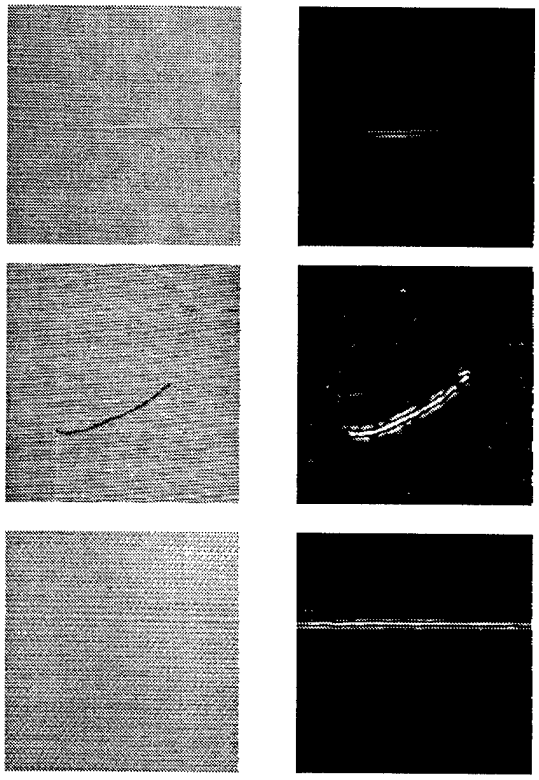

Figure 15. Defect detection with EASLM. Left column: cloth samples carrying defects. Right column: optically obtained wavelet filtered images.

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Silicon Spatial Light Modulators for Atmospheric Aberration Compensation

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Abstract

Northrop Grumman reports on a program utilizing a Silicon Light Modulator combined with Linear Phase Conjugation to compensate for atmospheric induced aberrations that severely limit laser performance. In a program to improve both the beam quality and laser energy delivered to the target, Northrop Grumman has developed a novel aberration compensation technique. This technique, hereafter referred to as Active Tracking System, utilizes a silicon Spatial Light Modulator as a dynamic wavefront reversing element to undo aberrations induced by the atmosphere, platform motion, or both. Northrop Grumman's aberration compensation technique results in a high fidelity, near-diffraction limited laser beam delivered to the target.

Introduction

Atmospheric induced aberrations can seriously degrade laser performance, greatly affecting the beam that finally reaches the target. This is especially true for propagation over long distances in the atmosphere. Lasers propagated over any distance in the atmosphere suffer from a significant decrease in fluence at the target due to atmospheric aberrations. This is primarily due to fluctuations in the atmosphere over the propagation path, and from the motion of the platform relative to the intended aimpoint. Also, delivery of high fluence to the target typically requires a low divergence beam, thus, atmospheric turbulence or platform motion results in a lack of fine aimpoint control to effectively keep the beam directed at the target. Northrop Grumman's Active Tracking System (ATS) continually tracks the target as well as compensates for atmospheric and platform motion induced aberrations. This results in a high fidelity, near-diffraction limited beam delivered to the target.

Energy deposited on target depends upon several factors including atmospheric turbulence strength, signal-to-noise ratio, and system latency time. With ATS, gains of one to several orders of magnitude increase in laser fluence at the target have been demonstrated. Additionally, a multitude of operational wavelengths may be addressed due to the linear system architecture, and powers well in excess of 1 kW can be routinely handled with the use of silicon-based SLMs. With ATS, and as a result of the aberration compensation and target tracking capability, lasers with very low divergence may be utilized. In this manner, a greater amount of laser energy is able to be delivered to the target. Some areas that can benefit from ATS include IRCM, EOCM, LIDAR, and laser radar.

Aberration Compensation Concept

The ATS concept is illustrated in Figure 1; its operation consists of two discrete steps. In the acquisition step, a low power illumination laser transmits a highly diverging beam to the target. Ideally, the divergence of this acquisition beam is matched to the uncertainty of the target direction. An OA return is received. This return is collected and interfered with a reference beam from the local oscillator (LO) on an integrating focal plane array (FPA) detector to form an electronic hologram. The hologram is read from the FPA, processed, and the conjugate written to the spatial light modulator (SLM).

In the engagement step, a beam from a second laser is reflected off the SLM. The SLM acts as a phase modulator and the reflected energy is contained in a beam that is the phase-conjugate of the target return. Now, this beam, which is the conjugate of the original beam, retraces the path to the target. During this time, any wavefront distortions are undone, thus resulting in near-diffraction limited energy delivered to the target. By continually repeating the acquisition and engagement steps, moving targets can be tracked (whether the target is moving relative to the platform or the platform is moving relative to the target) and compensation performed for time varying aberrations in the atmosphere.

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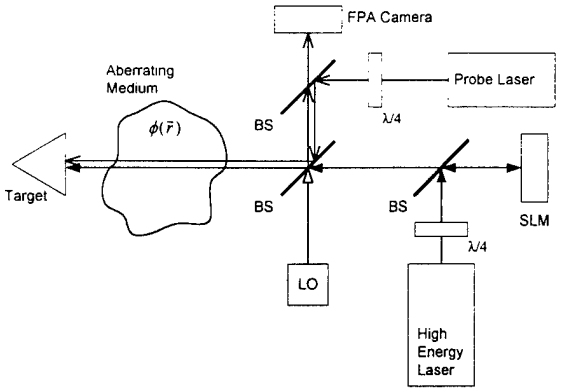

Figure 1. ATS Operation

The maximum energy-on-target enhancement factor for the high energy laser is equal to the number of SLM pixels multiplied by the hologram efficiency. Thus, for 64 x 64 pixel devices, and with a 0.4 hologram efficiency (the maximum efficiency for a plane, binary phase hologram) the enhancement factor is about 1640. Hence, the greater the number of SLM pixels, the greater the performance improvement that will be realized. Energy deposited at the target depends upon several factors including, atmospheric turbulence strength, signal-to-noise ratio, and system latency time, but gains of one to several orders of magnitude can be expected.

ATS provides automatic target acquisition within its field-of-view, as well as atmospheric aberration compensation. When compared to conventional adaptive optical schemes, no wavefront reconstruction algorithms are required. Additionally, when compared to all-optical phase conjugation schemes that require very high optical amplification factors, up to 10^{15}, amplification of the target return is not required. The energy of the propagated beam is limited only by the laser's maximum energy and the SLM damage limit.

The homodyne process utilized in ATS exhibits the high gain of a coherent detection process without the field-of-view limitation characteristic of the heterodyne process. If desired, even greater sensitivity may be attained using a multiple-step "bootstrapping" process, whereby targets with a signal-to-noise ratio of much less than unity can be detected. It allows target acquisition with low initial photon counts. Bootstrapping is an iterative process that utilizes a sequence of pulses, each pulse corrected by the return from the preceding pulse. Here, the illumination laser is reflected off the SLM; even very noisy holograms will slightly increase the illumination energy on the target, resulting in a higher signal-to-noise ratio in the subsequent hologram. This iterative process typically converges to a maximum energy-on-target in three to four pulses. This bootstrapping process is depicted in Figure 2.

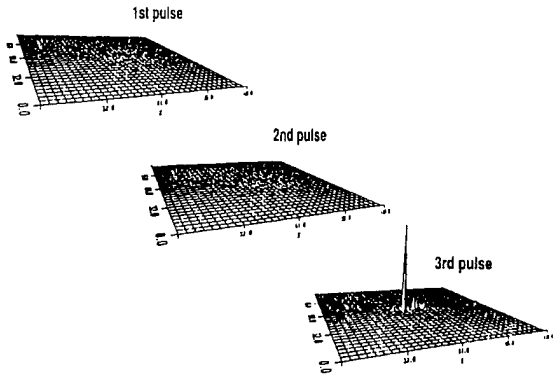

Figure 2. Bootstrapping Process

An advantage of ATS, when compared to all-optical phase conjugation techniques, is that the hologram that contains information about the target and the intervening medium is available in electronic form. This information can be stored in computer memory and processed to extract information about the target. With the very high processor speeds available, this may be performed very quickly. As an example, by computing the Fourier transform of the hologram, target direction relative to the optical axis is obtained. In cases where multiple targets are present, targets can be removed in the Fourier domain, thus allowing sequential target engagement.

Spatial Light Modulator and Electronics Subsystem

Northrop Grumman has developed a novel silicon SLM capable of displaying the phase information required for atmospheric correction. This SLM behaves as a dynamic wavefront reversing element to undo aberrations induced by the atmosphere, platform motion, or both. A hologram formed on an FPA camera is transferred, pixel-by-pixel, to the SLM. This hologram, the conjugate of that formed on the FPA, contains both intensity and phase information about the intervening medium between the SLM and the target. Due to their close interaction, the FPA, hologram processor, and SLM form a single subsystem. Their interrelationship is shown in Figure 3.

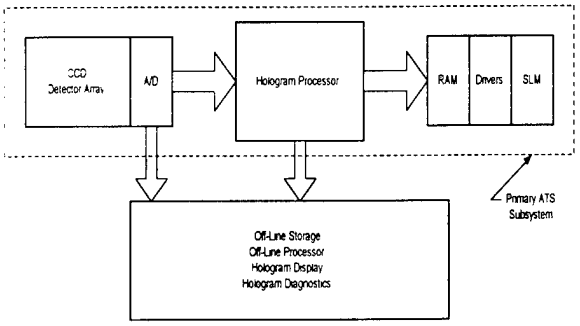

Figure 3. Camera, Hologram Processor, SLM Subsystem

The SLM is fabricated using silicon micromachining techniques. Figure 4 shows a diagram of the SLM constructed of a movable (deformable) diaphragm and a backplate to which an interconnect board and driver electronics are connected. The diaphragm is subdivided into N by N pixels; each supported from the backplate by an oxide grid. Individual pixels are etched with a flexure region, thus deflecting in a piston-like motion. In practice, the SLM behaves in much the same manner as a phased array antenna. The backplate, constructed from a flat, thick piece of silicon, serves as a support for the pixelated diaphragm and a structural surface to maintain device rigidity. Electrostatic attraction between the conductive silicon diaphragm (ground potential) and a deflection electrode requires a modest voltage (≈ 20 volts) to achieve deflection. The electrical connection from a deflection electrode to the X-Y addressable electronics through the interconnect passes through a via under each element. Additionally, this via serves as a vent for critical (fluid) damping of the diaphragm.

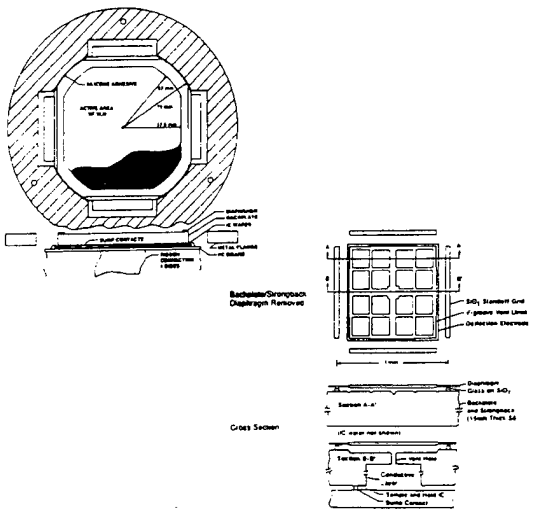

Figure 4. Design for N by N Pixel Silicon SLM

The N rows of the FPA are read-out in parallel, converted from analog to digital signals, and written to the SLM. The detected hologram (digital FPA output) and the processed hologram (written to the SLM) are stored electronically for post-processing, if desired. Mathematically, an expression for the intensity forming the hologram pattern is givenby:

$$H(i,j) \sim |R(i,j)|^2 + o(i,j)R(i,j)^* + o(i,j)^* R(i,j) + |o(i,j)|^2 \quad (1)$$

where $R(i,j)$ and $o(i,j)$ are the complex electric fields of the reference beam and the object beam at pixel (i,j). The reference beam profile, the first term on the right, must be nearly uniform across the FPA array while the object intensity, the fourth term on the right, must be small compared to the reference intensity. The second and third terms contain information about the target and the intervening medium.

The homodyne detection SNR is given by the expression:

$$SNR = \frac{2n_R n_{o,rms}(T_o / T_R)}{n_R + n_{o,rms} + n_B + n_D + n_j^2} \quad (2)$$

where n_R, $n_{o,rms}$, n_B, n_D, and n_j are the number of photoelectrons due to the reference beam, the object beam, the background, the detector dark-current, and the Johnson/readout noise, respectively. T_R and T_o are the pulse width of the reference beam pulse and the object beam pulse, respectively. Ideally, these two pulse widths would be equal, but, in practice, $T_R > T_o$ in order to reduce the required accuracy of the target-return arrival time.

The primary function of the hologram processor is to subtract the reference intensity term as shown in Equation 1. This term represents the bias and can be subtracted since it does not contain any useful information. However, since its value is considerably larger than that of the information containing terms, this subtraction must be performed with a high degree of accuracy.

The dynamic range of the FPA array and, hence, the number of bits in the analog-to-digital (A/D) converter is dictated primarily by the requirement to keep the object beam, which acts as a noise term, small when compared to the other terms in the hologram expression. The magnitude of this term varies both spatially and temporally because of atmospheric scintillation. Analysis indicates that the minimum number of bits is about eight, with higher numbers desirable to improve performance and reduce the accuracy to which the target range must be

known. The minimum FPA bucket size is primarily determined by the requirement that the Shot noise count due to the reference beam be greater than the noise count due to the other noise sources.

Performance

ATS presents several distinct advantages as compared to a conventional approach: 1) since most targets are found using OA, bootstrapping can permit a system utilizing this concept to lock onto targets incorporating significant cross section reducing counter countermeasures (CCM); 2) ATS acquisition beam may be several times wider than with a system not utilizing this technique, thus reducing pointing accuracy requirements with regard to the search beam; 3) there is a significant increase in the energy-on-target, thus minimizing engagement laser energy requirements (delivering a high fidelity, near-diffraction limited beam over the laser propagation path is essential to laser damage applications); 4) the automatic, vibration-insensitive, pointing capability eliminates the necessity for complex and expensive gimbals used in conventional pointing systems, and; 5) provision for sequential engagement of multiple targets within its field-of-view. Therefore, the output energy of the engagement laser may be significantly reduced, or, for a given engagement laser energy, the energy-on-target can be increased and the engagement range extended.

Figure 5 and Figure 6 show the fraction of energy-on-target without ATS and with ATS, respectively, for various degrees of atmospheric turbulence, C_n^2. Here, the transmit aperture is 10 cm and the target has a 5 cm receive aperture; the wavelength selected is 0.85 μm. Notice in Figure 5, the non-compensated case, that the energy-on-target decreases rapidly as the C_n^2 increases. Thus, for a C_n^2 of 10^{-14} at a 3 km range, the energy-on-target would be about 0.015 of that from the engagement laser. Now, for the compensated case, Figure 6, and identical conditions for a C_n^2 of 10^{-14} at a 3 KM range, the energy-on-target would be nearly 0.4 of that from the engagement laser. Therefore, if 10 mJ of energy is required on target, the non-ATS case would require a 670 mJ laser, while the compensated case would require only a 25 mJ laser; twenty-seven times more laser energy would be required for non-compensated laser case. Indeed, this would have a significant impact on system performance, size, weight, and cost, especially if greater energy or range performance is required.

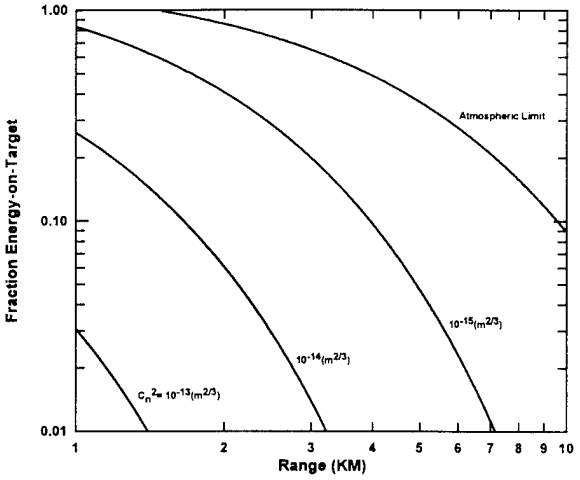

Figure 5. Typical Performance Without Compensation

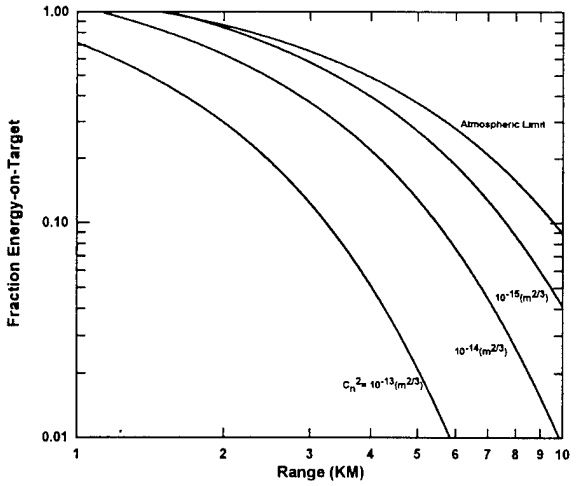

Figure 6. Typical Performance With Compensation

Test Results

Analytical, simulated, and experimental results of Strehl ratio (peak intensity to diffraction limited peak intensity) as a function of SNR is shown in Figure 7. Here, excellent agreement was obtained between theory and experiment, even at SNRs as low as 0.1. The difference between the analytical results and the computer simulations is due to the statistical nature of the noise. Figures 8 and 9 show computer simulations and experimental data, respectively, for bootstrapped operation. The top row in each figure shows the hologram written to the SLM and the bottom row shows the resulting intensity distribution at the target plane. Experimental results are shown as an intensity profile through the peak intensity.

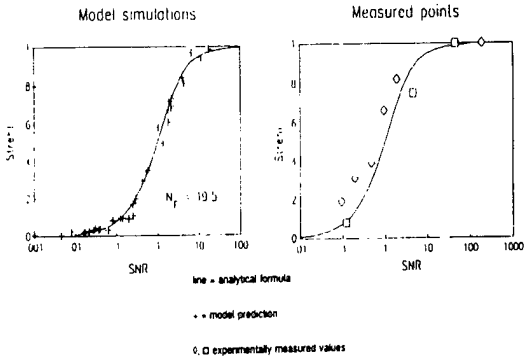

Figure 7. Simulated and Measured Target Intensity versus SNR

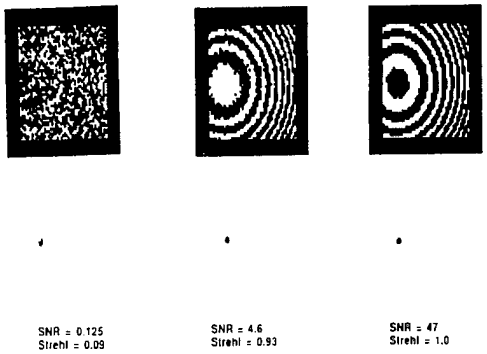

Figure 8. Bootstrapped Operation Model Predictions

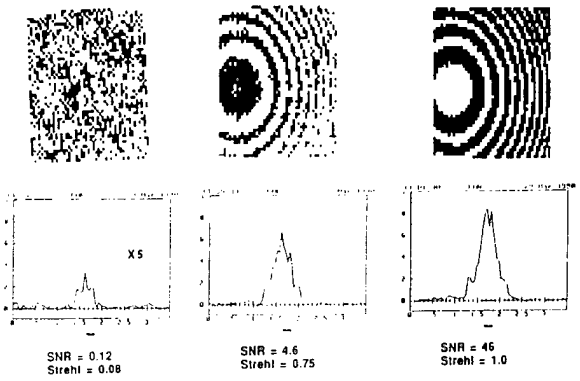

Figure 9. Bootstrapped Operation Experimental Results

Performance tests were carried out both during the daytime and at night to a range of 3 km; target acquisition tests were performed to a range of 5 km. Test objectives were to compare the performance of ATS with the performance of a non-ATS system, without aberration compensation. The goal was to demonstrate a five-fold increase in energy-on-target as compared to the non-ATS system. In actuality, more than a seventy-five-fold increase in energy-on-target was demonstrated. Figure 10a shows the variance in energy-on-target without ATS. It is important to notice how distorted the beam appears over the 3 km path. Figure 10b shows the improvement realized with ATS. Here, the near diffraction limited beam is clearly observed.

10a. Aberrated Farfield Image

10b. Improvement with ATS

Figure 10. Performance Improvement Realized with ATS

Summary

It is quite apparent that ATS can provide tremendous gains in increasing the laser energy delivered to a target. When coupled with a laser radar, IRCM, or EOCM system, a high fidelity, near diffraction limited beam is delivered to the target. In most cases, this translates into either an increase in energy on target for a given laser energy, or a reduction in laser energy required to deliver a specific amount of energy to the target. With ATS, laser size, weight, and cost may be reduced therefore making certain IRCM, EOCM, and LIDAR, and laser radar applications feasible.

SILICON SPATIAL LIGHT MODULATOR FABRICATION

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Abstract

Spatial light modulators (SLM) are utilized in systems which compensate for distortion of a laser beam caused by transmission through a distorting medium. The Northrop Grumman linear beam cleanup system [1] uses an SLM to modify the phase front of the input beam to cancel the phase changes produced along the transmission path. At longer wavelengths these phase changes may not be achievable with current liquid crystal or lead lanthanum zirconate titanate (PLZT) modulators. High laser power levels may also produce adverse effects in these materials if operated in transmission mode. The silicon SLM (Si-SLM) produces a phase change by reflection of the laser from the surface of moveable pixels. The all silicon construction of the Si-SLM reduces the effects of temperature changes on the flatness of the reflecting surface.

Key Words: Spatial light modulators, MicroElectrical-Mechanical Systems (MEMS), Atmospheric turbulence.

Description

The 32x32 Si-SLM [2] is composed of two silicon wafers - a thin diaphragm wafer bonded to a thick backplate wafer (Fig. 1). The highly polished front surface of the 250 mil thick backplate wafer provides support and serves as a flat reference plane for the reflective diaphragm. An array of ultrasonically ground and laser drilled through-holes provides electrical access from the backside to frontside and also serves to vent air from underneath the diaphragm. An insulating standoff grid on the backplate provides a support to which the diaphragm is bonded. Low Pressure Chemical Vapor Deposited (LPCVD) polysilicon on the backplate forms interconnected pixel actuation electrodes, through-hole conductors, and backside contacts.

A silicon wafer pre-thinned to ~ 4 μm is bonded to the standoff grid on the backplate using a sputtered layer of bonding glass as an adhesive. The diaphragm is coated with metal to increase reflectivity. When a voltage is applied between the polysilicon electrodes and the diaphragm, the diaphragm is pulled down via an electrostatic attractive force. The portion of the laser beam reflected from a pixel deflected downward a distance, d, will experience a phase change equal to 2π ($2d/\lambda$). Flexures etched into the diaphragm allow a piston-like up and down motion of the pixels. Each pixel is addressed individually via an ASIC driver assembly attached to the backside of the Si-SLM.

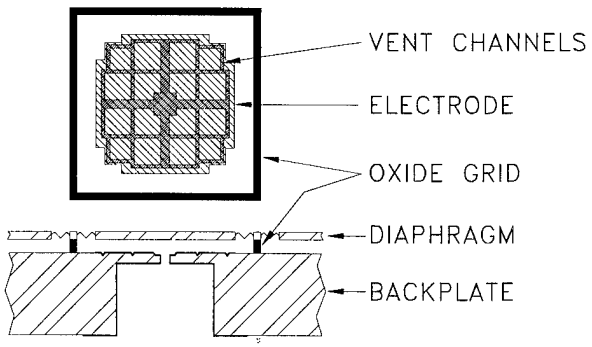

Figure 1. *Top (a) and cross section (b) views of individual pixel cell.*

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Design

The flatness of the individual pixels is expected to be λ/10. A full membrane diaphragm would exhibit a parabolic shape in the deflected mode. Taking the useful area of the pixel to be the area within the range of the desired deflection +/- λ/20, the fill factor for the pixel is reduced by ~ $(.48)^2$. To increase the fill factor, the Si-SLM pixel consists of a flat plate suspended by compliant flexures at each corner. A comparison between the shapes for a full membrane and the Si-SLM in the deflected mode is shown in Fig. 2. The plate with flexures allows a range of deflections in the on mode.

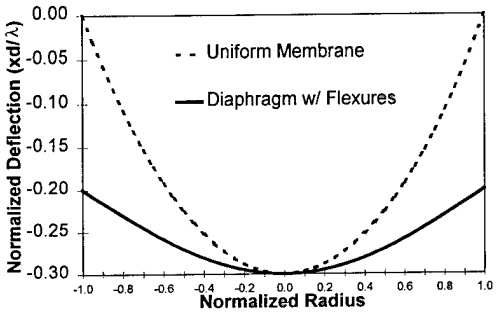

Figure 2. *Deflected shape of uniform membrane vs diaphragm with flexures.*

The resonant frequency of the Si-SLM structure is determined by the thickness (i.e. mass) of the plate and the strength of the flexures. For higher operating frequencies the stronger flexures require higher voltages to deflect the membrane. To maintain the flatness of the pixel in the deflected mode with stronger flexures means that the center plate must be made stiffer (i.e. thicker). Given that the resonant frequency is proportional to the square root of the stiffness of the flexures divided by the mass of the plate, a maximum operating frequency can be derived for a given maximum drive voltage.

As shown in Fig. 3, the electrostatic force, F_e, the electrode exerts on the pixel's diaphragm is given by:

$$F_e = \{\varepsilon_0 A V^2\}/\{2 (d_0 - x_d)^2\} \qquad (1)$$

where ε_0 is the permittivity of the air gap, A is the electrode area, V is the applied voltage, d_0 is the initial electrode to diaphragm gap, and x_d is the displacement.

The displacement, which is equal to the force F_e divided by the flexure spring constant, k, is then:

$$x_d = \{\varepsilon_0 A V^2\}/\{2 k (d_0 - x_d)^2\} \qquad (2)$$

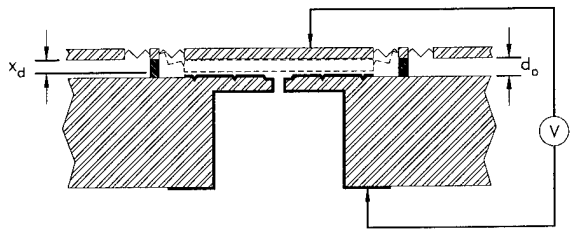

Figure 3. *Cross section of single pixel showing initial gap, d_O, and displacement, x_d.*

As the pixel diaphragm approaches electrode, the electrostatic force will eventually overcome the flexures' restoring force and the diaphragm will collapse onto the electrode. This occurs when x_d satisfies the following condition:

$$x_d > d_0 / 3 \qquad (3)$$

Thus for stable operation, the maximum displacement must be less than given in Eq. (3). For the Si-SLM, x_d maximum was set at $d_0 / 5$.

Given the conditions above for minimum gap, pixel flatness, and a maximum deflection of λ/4 the operating voltage can be calculated as a function of resonance frequency, Fig. 4.

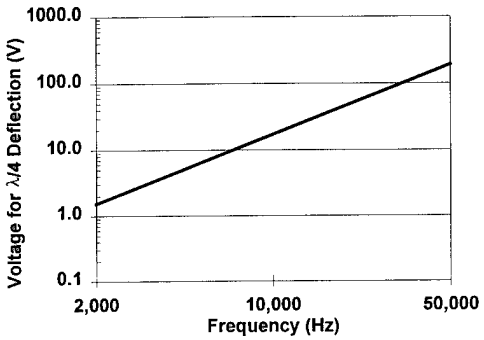

Figure 4. *Plot of voltage for λ/4 deflection vs resonance frequency for λ = 5μm.*

Backplate Fabrication

The backplate fabrication begins with the polishing of a 3 inch diameter, 250 mil thick single-crystal silicon wafer. The side which will face the silicon diaphragm (frontside) is polished to λ/10 (HeNe) and the opposite side (backside) is given a standard commercial wafer polish. Vent channels etched into the frontside of the backplate

funnel air trapped between the diaphragm and backplate to a through-hole at the center of the pixel as the diaphragm deflects downward. The channels are patterned using IC standard photolithography techniques and the silicon is etched from the channels using an RIE etch with nitrogen triflouride (NF_3) and argon as process gases. The size of the mesas formed by this channel etch determine the amount of squeeze film damping on the diaphragm. A mesa size was chosen to give critical damping for a pixel resonance frequency of 16 kHz.

At the same time the channels are formed, an array of wells are etched into the backside to serve as alignment guides for the ultrasonic through-hole machining. Registration of front and backside patterns to each other is accomplished using a hinged fixture which clamps the backplate wafer between two pre-aligned photomasks. A 32x32 array of blind holes, 20mil x 20mil, are then ultrasonically ground from the backside to within ~10 mil of the front surface. A Nd-YAG laser completes the through-holes by drilling 4 mil diameter holes from the frontside to intersect with the center of the blind holes.

A ~7 μm thick, thermally grown silicon-dioxide layer is photolithographically patterned to form the stand-off grid on the frontside. Further thermal oxidation produces a 3 μm thick field oxide on all backplate wafer surfaces which electrically isolates a subsequently deposited polysilicon layer from the backplate substrate. A thick layer of field oxide was used to reduce the polysilicon electrode parasitic capacitances which act as an added load on the ASIC driver circuits.

An LPCVD deposited layer of polysilicon (~ 5000 angstroms) uniformly coats both front and back surfaces and inside the through-holes on the backplate wafer. A Reactive Ion Etch (RIE) patterning of the polysilicon produces individual backside contact pads, through-wafer conductors, and frontside excitation electrodes at each pixel site, Fig. 5. The RIE etch was performed using nitrogen triflouride (NF_3) and argon as process gases. The backside polysilicon contacts are coated with TiW/gold metallization to aid in bump contacting to the ASIC driver assembly.

In preparation for attachment of the diaphragm wafer, a thin (~1200 angstrom) layer of Corning 7556 low-temperature, bonding glass is selectively sputter deposited on top of the oxide grid on the frontside of the backplate.

Diaphragm Fabrication

A heavily boron-doped epitaxial silicon layer (~4 μm) grown on a 3 inch diameter, 12 mil thick, (100) silicon substrate forms the diaphragm of the Si-SLM. The substrate material in the diaphragm area of the wafer

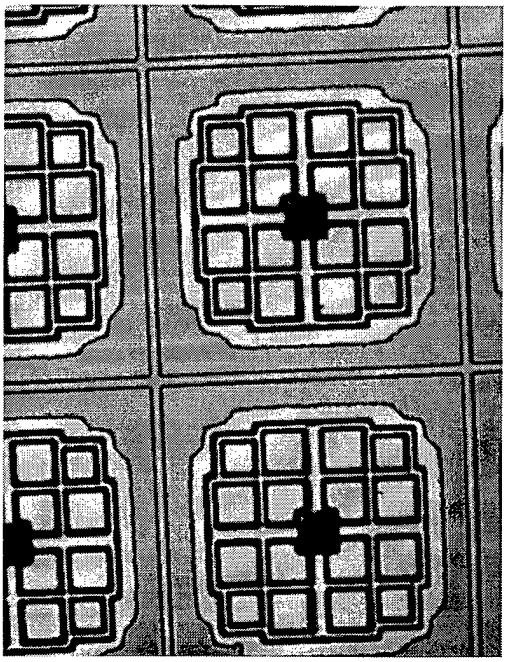

Figure 5. *Photo of frontside of backplate following patterning of vent channels, oxide grid, and polysilicon electrodes..*

is removed using a KOH etch. The boron doping in the epitaxial layer serves as an etch-stop for the KOH. Extremely uniform and close tolerance thickness across the diaphragm is achieved using this technique. The side of the diaphragm wafer to be bonded to the backplate is protected during the etch with an LPCVD deposited layer of silicon nitride. After wafer thinning, the silicon nitride is removed prior to bonding.

Bonding

Before assembly, the backplate and diaphragm wafers are cleaned and given a final isopropyl alcohol vapor bath to remove particles and any contaminants which might interfere with the wetting of the bonding glass to the silicon diaphragm. The bonding is done at a temperature of 570° C for 60 minutes in a N_2 ambient. A slight vacuum (~3.5 inches of H_2O) applied through the holes in the backplate serves to hold the diaphragm in contact with the glass during the bonding cycle.

Flexure Etching

After bonding, the diaphragm is metallized with ~300A of sputter deposited aluminum. The aluminum is photographically patterned and etched to form openings for etching flexures into the silicon diaphragm (Fig. 6). The diaphragm is etched with an NF_3-argon RIE etch

using the photoresist and aluminum as masks. The photoresist increases the anisotropy of the RIE etch producing flexures with straight sidewalls and minimal undercutting. The spring constant of the flexures, and hence the pixels resonance frequency and voltage sensitivity, is determined by the flexure lateral dimensions and the diaphragm thickness. A spring constant for the Si-SLM was chosen to give a resonance frequency of 16 kHz and a deflection of 1.25 μm at ~ 40 volts.

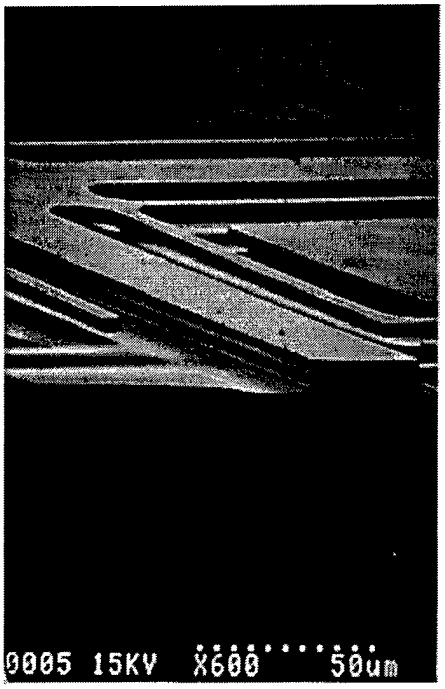

Figure 6. *SEM of one corner of pixel showing etched flexures.*

Measurements

The resonant frequency of the Si-SLM was measured in a vacuum using a fiber optic probe, Fig. 7. The measured value of 13.5 kHz agreed very well with the 13.1 kHz value calculated from flexure width and diaphragm thickness measurements. The displacement vs. electrode voltage was measured using a HeNe interferometer. A voltage of 25 V was needed to achieve a 1.25 μm displacement, Fig. 8.

Packaging

The Si-SLM is connected to the ASIC driver circuitry via a ceramic, multilayer metal, interconnect substrate sandwiched between the backside of the SLM and the ASIC chip. The interconnect substrate is necessary to

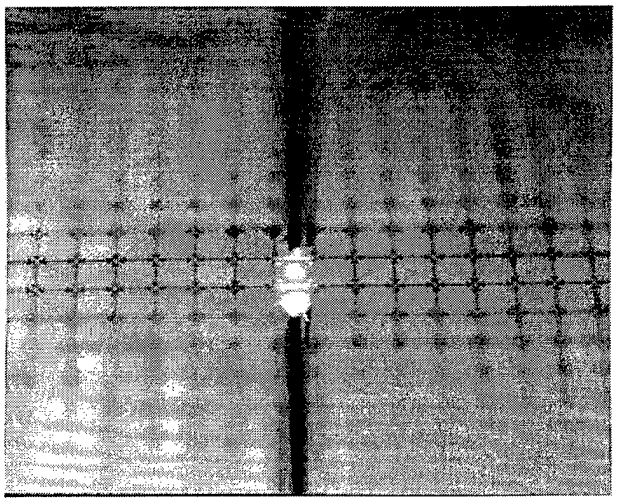

Figure 7. *Aluminum coated SLM pixel array, (1.05 mm)^2, showing flexure etch pattern. Fiber optic probe used for frequency response measurements also shown.*

spatially redistribute the outputs from the ASIC driver to match the bonding pads on the backside of the SLM. The ASIC chip is attached to the interconnect substrate using a solder bump flip-chip bond. The Si-SLM is attached to the opposite side using conductive polymeric bumps. The ceramic substrate's thermal expansion coefficient is closely matched to that of silicon to reduce stress on the bump bonds due to temperature changes.

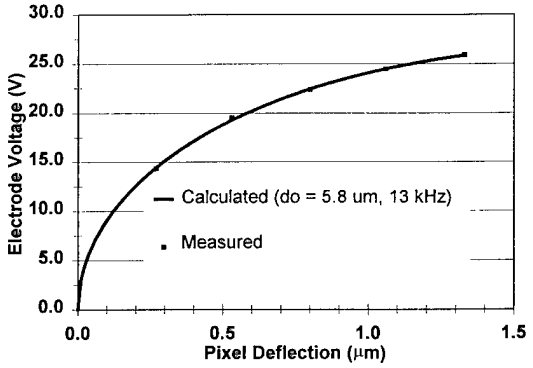

Figure 8. *Plot of deflection vs voltage for Si-SLM pixel.*

Discussion

The frequency and voltage response of several Si-SLM's have been measured and agree well with calculated values. The flatness of the pixels after flexure etch was found to be a strong function of the uniformity of the boron doping in the diaphragm wafer's epitaxial layer. A special etch sequence during thinning was used to remove the upper and lower boundaries of the epitaxial

diaphragm to leave a region of constant boron doping. Also, any high temperature processing on the diaphragm wafer prior to thinning was avoided because the processes precipitated defects in the epitaxial layer. The defects produced a non-uniform stress distribution (and hence pixel bowing) in the diaphragm.

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[2] U.S. Patent # 5,170,283, Dec. 1992.

Compensated Imaging by Real-Time Holography with Optically Addressed Spatial Light Modulators

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Abstract

"Compensated imaging by real-time holography corrects for aberrations in telescope imaging systems and allows scaling to large apertures using lightweight, low-optical-quality primary mirrors. This application leads to unique requirements for optically addressed spatial light modulators."

Key Words

Aberration compensation, Spatial light modulators, Holographic recording materials, Adaptive optics.

Introduction

Conventional telescope imaging systems are prone to image degradation resulting from several aberrating mechanisms. These mechanisms include atmospheric turbulence, misalignment of telescope optics and primary mirror distortions. Furthermore, engineering challenges associated with fabricating, transporting and manipulating large-aperture optics limit the size of high-optical-quality primary mirrors manufactured for telescope systems. This in turn limits both the resolution and light gathering ability of present day ground-based and space-based telescope systems.

In recent years real-time adaptive imaging schemes have been developed for the purpose of compensating aberrations due to atmospheric turbulence above ground-based astronomical telescope systems [1,2]. The turbulence-induced aberration introduces a spatially varying optical path deviation (OPD) which may be compensated by introducing an equal and opposite OPD. Conventional adaptive systems rely on deformable mirrors to introduce a compensating propagation path. A wavefront sensor and computer system characterize the aberrated wavefront and drive actuators on the flexible mirror, thereby restoring the image. Since optical path is the product of physical pathlength and refractive index, one can also achieve aberration compensation via spatial modulation of the refractive index. Consequently, electrically addressed liquid-crystal phase modulators are under development as low-cost high resolution replacements for the deformable mirrors [3,4].

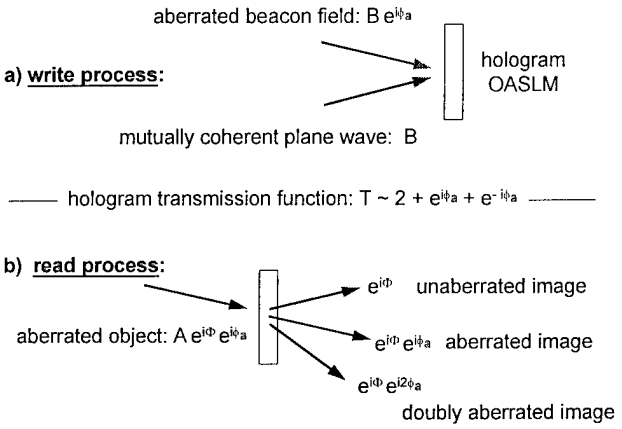

Figure 1. Aberration compensation by holographic phase subtraction.

Optical path correction schemes may also be applied to the problem of compensating aberrations in large lightweight low-optical-quality primary mirrors in space-based telescopes. One disadvantage of the OPD correction scheme in this application is the weight and complexity associated with the wavefront sensor and control electronics. In this work, we describe the application of optically addressed spatial light modulators (OASLM's) to an alternative technique for compensated imaging that eliminates the need for the wavefront analyzer, computer

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processor, and adaptive controls. This "all-optical" technique makes use of holographic phase subtraction, [5-7] where the OASLM acts as a real-time holographic recording medium that allows compensation of dynamic aberrations [8]. The phase-subtraction geometry is illustrated in Fig. 1. A beacon wavefront, of amplitude B, probes the phase aberration, ϕ_a, where $\phi_a=(2\pi/\lambda)$OPD and λ is the wavelength of the beacon laser. The aberrated beacon field, $Be^{i\phi_a}$, interferes with a mutually coherent plane wave, also of amplitude B, to produce a hologram as shown in Fig. 1a. For the case of an amplitude hologram, the hologram transmission function, which is proportional to the squared modulus of the illuminating field, is written as

$$T \sim 2 + e^{i\phi_a} + e^{-i\phi_a}.$$

Once written, the hologram is illuminated by the aberrated object field, $Ae^{i\Phi}e^{i\phi_a}$, where $Ae^{i\Phi}$ is the original undistorted object field. Mathematically, the diffraction is described by multiplying the aberrated object field by the hologram transmission function;

$$Ae^{i\Phi}e^{i\phi_a}\,T \sim 2\,e^{i\Phi}e^{i\phi_a} + e^{i\Phi}e^{i2\phi_a} + e^{i\Phi}.$$

This multiplication yields three terms. The first term, proportional to $e^{i\Phi}e^{i\phi_a}$, is the 0-order diffraction which is just the aberrated object field transmitted by the hologram. In the second term, proportional to $e^{i\Phi}e^{i2\phi_a}$, the complex phase distortions add yielding an object image with double the aberration. In the third term, the phase distortion terms have canceled leaving the complex phase $e^{i\Phi}$ describing the unaberrated object.

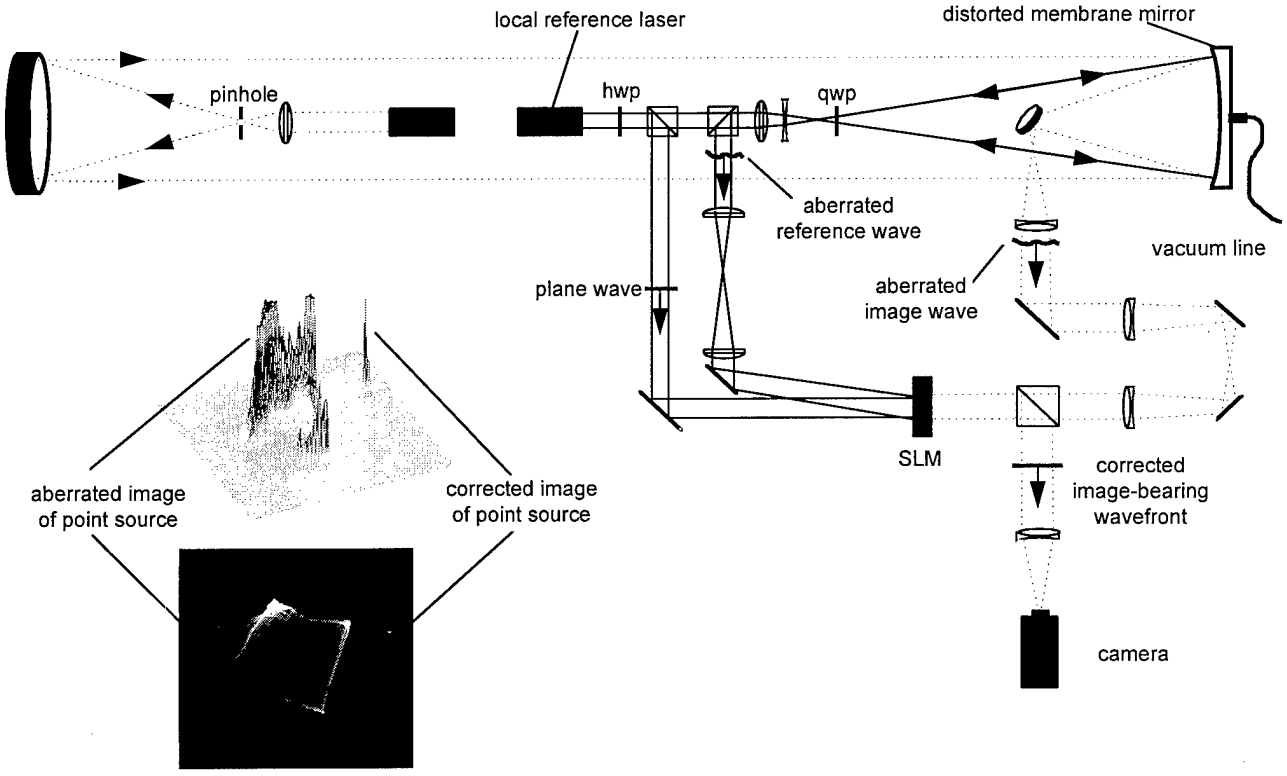

Figure 2. Experimental setup along with a two dimensional photograph and three-dimensional intensity contours of aberrated and corrected images of a point source imaged by a low-quality membrane optic using a real-time holographic phase subtraction technique. SLM spatial light modulator; hwp, half-wave plate; qwp, quarter-wave plate.

Experimental Demonstration

Recently, we presented the results of an experimental demonstration in which an OASLM is used as the real-time holographic medium in a compensated telescope geometry [9]. In this demonstration, near-diffraction-limited imaging was achieved using a membrane primary mirror with more than 100 waves of aberration. The experimental setup is shown in Fig. 2. An object point source at infinity is simulated by illuminating a 25 μm pinhole with the output from a helium neon laser operating at 543 nm, and collimating the transmitted light with a six-

inch diameter f/6 parabolic reflector. The collimated light is propagated to the compensated membrane mirror telescope. The membrane mirror consists of a high-reflectivity-coated four-micron-thick nitrocellulose membrane mounted to a vacuum flange and held under partial vacuum. A 5 mW green helium-neon laser acts as the reference beacon source. The laser output is expanded, directed through a null corrector lens arrangement and onto the primary mirror surface. The null corrector arrangement produces an f/6 parabolic wavefront. The membrane pressure is adjusted to approximately match the curvature of the membrane surface to the f/6 beacon wavefront. Consequently, the reference beam measures the deviation of the primary mirror surface from the ideal parabolic surface. The retroreflected light is recollimated by the null corrector and relayed to the "write" side of the OASLM where it interferes with a mutually coherent plane wave derived from the same laser. A Displaytech [13] ferroelectric OASLM operating at 300 Hz acts as the real-time hologram. The aberrated image-bearing light is relayed to the opposite side of the SLM where diffraction from the liquid-crystal layer occurs. Note in Fig. 2 that due to an internal reflection the OASLM generates diffracted light in the backward direction. The reflected/diffracted light is propagated to a camera located in an image plane for the pinhole. The zero-order aberrated beam and the first order corrected diffracted beam are shown in the lower left-hand corner of Fig. 2. Qualitatively, one can see that the degree of correction is very high.

In order to quantify the degree of correction, the image is magnified optically to produce a corrected image sufficiently large for a pixelated measurement of the spot size. A ray-trace analysis of the system, assuming a perfect f/6 parabolic primary mirror, indicates the diffraction limited spot size at the camera should be 75 μm. The compensated image is measured to be 120 μm in diameter or 1.6 times diffraction limited. The measured uncompensated image diameter is approximately 25 mm, or 330 times diffraction limited. Thus the degree of correction is greater than 200. While the degree of correction is very high, we did not achieve complete correction to the diffraction limit. This is most likely due to the fact that the large aberration leads to intensity interference fringe densities that are beyond the resolution of the OASLM. In this experiment, the write-beam crossing angle is approximately one-degree, corresponding to a fringe density of about 30 lines/mm The severe aberration leads to significantly higher fringe densities. The OASLM diffraction efficiency begins to decline from its maximum value at fringe densities greater than about 30 l/mm.

Optically Addressed Spatial Light Modulators as Real-Time Holographic Media

Figure 3 shows a schematic of the typical liquid-crystal OASLM architecture. The device consists of a large area amorphous-silicon photoconductor or photodiode and a ferroelectric or nematic liquid-crystal layer located between transparent electrodes. The electrodes are biased in the ~5 Volt range producing a field across the liquid-crystal region that depends on the local conductivity of the photoconductor. The holographic write beams produce an intensity interference pattern on the photoconductor. This leads to spatial modulation of the conductivity, and a corresponding spatial modulation of the field across the liquid-crystal layer. The liquid-crystal molecules reorient themselves according to the local field amplitude. The "read" beam is incident on the liquid-crystal side of the device. Ideally, a high-reflectivity mirror prevents the read light from illuminating the photoconductor. Consequently, the read beam passes through the liquid crystal, is reflected, and passes once again through the liquid crystal. The read beam will experience either phase or polarization modulation depending on the type of liquid-crystal medium and on the polarization properties of the incident read light.

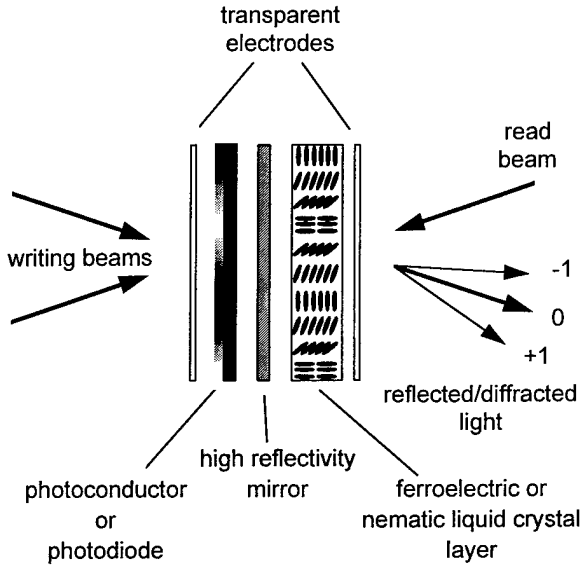

Figure 3. Schematic of the optically addressed spatial light modulator

Speed and Sensitivity

Early demonstrations of real-time holography were accomplished using nonlinear optical media as the holographic recording medium [10-12]. Nonlinear materials offer the advantages of high resolution and, in many cases, purely passive operation. That is, drive electronics and thermal stabilization are not required. One significant shortcoming however is the amount of laser

power that is typically required to modify the material's absorptive or dispersive response. Furthermore, the required laser intensity is typically inversely proportional to the material response time hence it is difficult to achieve both speed and sensitivity simultaneously.

The combination of write-beam sensitivity and reasonably high refresh rates make OASLM's very attractive for space-based telescope applications. OASLM devices typically operate with write-beam intensities near 50 $\mu W/cm^2$. Such intensities are easily achieved with minimal power and cooling requirements.

Hologram refresh rates range from ~30 Hz for nematic devices to >1 kHz for ferroelectric devices. Dynamic aberration compensation requires the OASLM to be operated at a refresh rate that is greater than the rate at which the aberration is changing. The operating speed requirement will be determined by the source of the time-dependence (e.g. mechanical vibrations or atmospheric turbulence) and is specific to a given application.

Optical Efficiency

For the purpose of compensated imaging, the net optical efficiency may be defined as the percentage of uncompensated, unpolarized image light that is converted into compensated image light. Thus, this definition includes any absorption and reflection losses associated with use of the OASLM. For light-sensitive imaging applications, the low optical efficiency achievable with commercially available OASLM's is a significant shortcoming. There are two primary contributions to the low net efficiency. First is the loss experienced by the image light upon reflection from the amorphous-silicon interface. Historically, [13] high reflectivity dielectric coatings on large area photodiodes were found to reduce the resolution and degrade the switching capabilities due to the added thickness and capacitance. Recently, [14] high-performance OASLM devices incorporating high-reflection coated photoconductors have become commercially available.

Diffraction Efficiency

The second source of optical loss is the first-order diffraction efficiency. Spatial light modulators are thin hologram devices. Typically, the nematic and ferroelectric liquid-crystal devices produce analog and binary modulation, respectively. Figure 4 shows the theoretical maximum first-order diffraction efficiencies for the four possible combinations of amplitude or phase and analog or binary thin holograms. Phase holograms yield the highest first-order diffraction efficiencies with the analog and binary phase gratings yielding 34% and 40%, respectively.

Since ferroelectric devices operate on the principle of polarization rotation, a polarizer/analyzer configuration is necessary to convert the polarization modulation into amplitude or phase modulation. When situated between orthogonal linear polarizers, the liquid-crystal layer can be oriented to produce either pure amplitude modulation, pure phase modulation, or a combination of both. When used with unpolarized read light, the polarizer/analyzer configuration is inherently lossy.

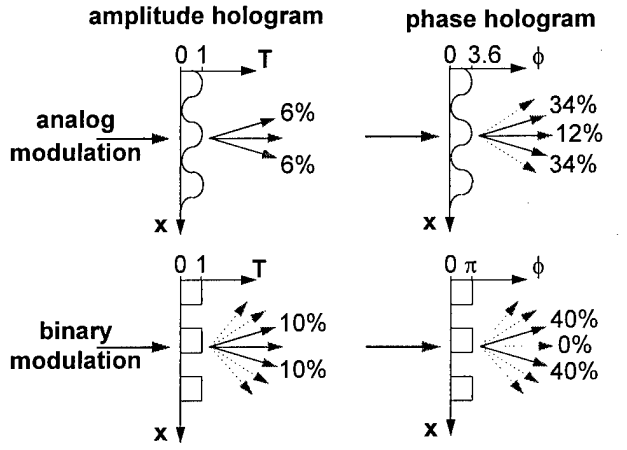

Figure 4. Maximum theoretical diffraction efficiencies for thin hologram diffraction media.

Figure 5 shows two possible orientations of a ferroelectric device with a molecular-tilt angle of $\theta=22.5^0$ and layer thickness designed to produce one-half wave of retardance. In Fig. 5a, pure amplitude modulation is generated by aligning the off-state molecular axis with the read-light polarization. In the off-state regions, the polarization state is preserved and the read light is blocked by the analyzer. In the optically activated portions of the liquid-crystal layer, the molecules undergo a discrete 2θ rotation and the read-beam polarization is rotated by 4θ or 90^0 and subsequently transmitted by the analyzer.

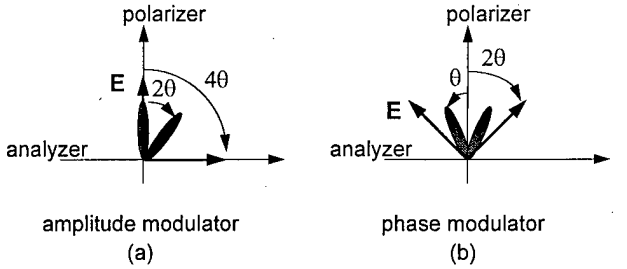

Figure 5. Ferroelectric liquid-crystal molecule with polarizer/analyzer arrangement oriented to induce (a) amplitude modulation and (b) phase modulation.

Pure phase modulation is generated, as shown if Fig. 5b, by aligning the off-state molecular axis at $-\theta$ relative to read-light polarization. In this case, the read-beam polarization is rotated -2θ by the off-state molecules and $+2\theta$ by the on-state molecules. The polarization

component of read light transmitted by the analyzer is discretely modulated in phase by π.

The ferroelectric OASLM used in Fig. 2 incorporates a liquid-crystal layer whose thickness is designed to produce a half-wave of retardance in double pass. In the optically activated portions of the liquid-crystal layer, the molecules undergo a discrete 20^0 rotation and the read-beam polarization is rotated by 40^0. With the polarizer/analyzer configuration shown in Fig. 2, the diffracted beam is generated by an amplitude-modulated field produced by the component of the 40-degree rotated light that is orthogonal to the incident read light. The maximum theoretical first-order diffraction efficiency for a binary amplitude grating is 10%. Owing to the 40-degree polarization rotation angle, only 64% of the diffracted light is aligned with the analyzer. Since this particular device incorporates an uncoated photodiode, the reflectivity at the amorphous-silicon/liquid-crystal boundary is only about 24%. Consequently, the maximum theoretical efficiency of this device is only about 1.5%. In this configuration the polarizer rejects 50% of unpolarized image light and thus further reduces the net efficiency to less than 1%.

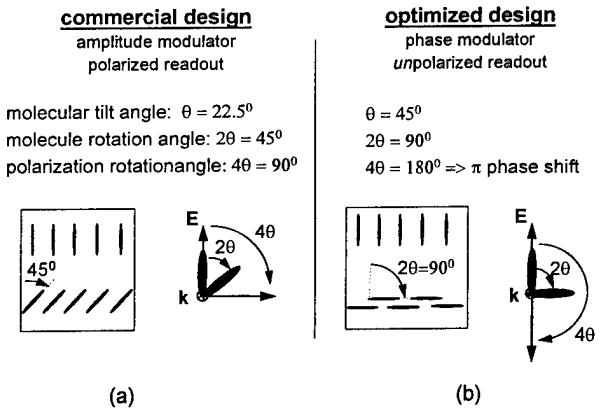

Figure 6. Commercially available (a) and proposed (b) ferroelectric liquid-crystal configuration for spatial light modulators.

Figure 6a shows the current technology in commercially available ferroelectric OASLM's. The device is optimized for use as an amplitude modulator and incorporates a liquid-crystal layer with a 22.5^0 molecular tilt angle. The corresponding polarization rotation angle of 90^0 in the read beam light is well suited to applications such as video displays and incoherent-to-coherent converters.

Figure 6b shows a variation of this OASLM design that is optimized for real-time holography (RTH) applications. In this case, a liquid-crystal molecular-tilt angle of 45^0 leads to a molecular rotation angle of 90^0 and a polarization rotation angle of 180^0. Thus light polarized along either axis of the original molecule orientation experiences π phase modulation. In principle, this device should yield a net efficiency of 40% with unpolarized light. High-tilt-angle ferroelectric liquid-crystal media exist, but generally lack the smectic-A phase that is required to achieve the necessary molecular alignment. Successful incorporation of high-tilt-angle media into OASLM architectures should significantly enhance their diffraction efficiencies and hence their usefulness in RTH.

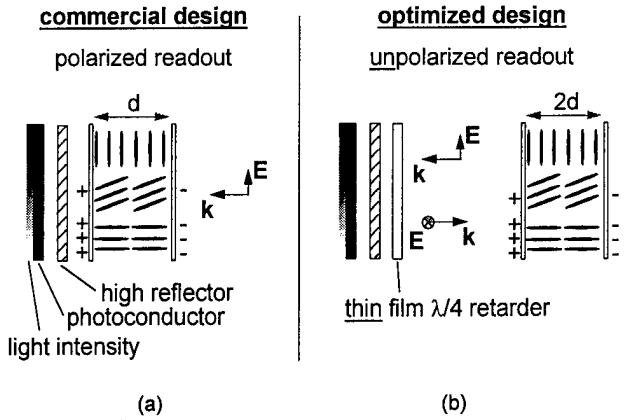

Figure 7. Commercially available (a) and proposed (b) nematic liquid-crystal spatial light modulator configurations.

Alternatively, commercially available [14] parallel aligned (PAL) nematic devices produce analog diffraction holograms with demonstrated efficiencies in excess of 30%. Unfortunately, the phase modulation occurs for only one linear polarization, reducing the overall diffraction efficiency to about 15% for unpolarized light. Figure 7a shows a schematic of the commercially available PAL nematic OASLM. In the absence of an applied voltage, the liquid-crystal molecules are aligned as shown. In the presence of an applied voltage, the molecules rotate to align themselves with the electric field. The degree of rotation is proportional to the voltage. Light polarized along the direction of the initial molecule orientation will experience a refractive index that varies with the applied voltage. Note that optimization as an amplitude modulator requires the read light to be polarized at 45^0 relative to the long axis of the unbiased molecules and the thickness to be such that the maximum phase retardance is π. Optimization as a phase hologram however requires the read light to be polarized along the long axis of the unbiased molecules and the thickness to be such that the maximum phase retardance is not π, but 3.6 in accordance with Fig. 4. Figure 7b shows a design modification that would lead to phase modulation for both polarization components. In this configuration, a thin film quarter wave plate has been added between the reflective layer and the liquid-crystal layer. A linearly polarized component of incident light will be rotated 90^0 in double passing the

quarter wave layer. Consequently, the linear polarization component aligned with the unbiased molecules will experience the phase grating on the first pass through the liquid-crystal layer. The orthogonal polarization will experience the phase grating on the return pass. The liquid-crystal layer must now be a factor-of-two thicker to achieve the same phase retardance in a single pass. This concept has been demonstrated using a parallel aligned nematic electrically addressed SLM with a conventional quarter wave plate and mirror, [15] but has not been demonstrated in an OASLM device.

Resolution

Electric field fringing effects in the photosensor, liquid-crystal and reflecting layers limit the optical fringe density that can effectively be translated into a phase hologram. Commercially available OASLM's typically experience reduced diffraction efficiencies at spatial frequencies greater than 20 to 30 l/mm. This in turn limits the severity of aberration that can be corrected in this application. The required resolution is determined by both the severity of the aberration and amount of demagnification that occurs in propagating the beacon light from the primary mirror to the pupil plane containing the OASLM. Improving the resolution to > 100 l/mm while maintaining maximum diffraction efficiency should make these devices adequate for a range of interesting applications.

Table 1. OASLM performance characteristics.

	commercially available	**desired for RTH**
speed	FLC: > 1 kHz NLC: 30 Hz	1 kHz
sensitivity	40 μW/cm2	40 μW/cm2
resolution	30 l/mm	> 100 l/mm
net optical efficiency (unpolarized light)	FLC: < 10% NLC: 15%	>30%
aperture	25 mm	> 25 mm

Conclusions

The current focus of the commercial OASLM market seems to be on video display applications. The requirements for this application are close, but not identical, to those for RTH. In order for RTH to be competitive with conventional adaptive imaging, improvements in OASLM efficiency and resolution are essential. Efficiencies of 30% to 40% are theoretically possible and would make RTH competitive with conventional OPD correction techniques. Table 1 summarizes the capabilities of commercially available OASLM's and the performance characteristics required for holographically compensated imaging.

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Viewgraph

High - resolution LCTV-SLM and its application to holography

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Comments for viewgraphs

Fig. 1

This figure shows a schematic diagram of light modulation using a unit LC cell. LC molecules are surface aligned by surface anchoring method between two glass substrates and the directions of LC molecules are gradually twisted along the Z axis. LC molecules has dielectric anisotropy so that the refractive index between long and short axis is different.

The direction of the linearly polarized light will rotate along the LC molecules after passing through the LC cell. In this case, optical pass becomes ned. As LC molecules are very sensitive to electric fields, they are aligned along the fields while sufficient voltage is applied to the cell and no rotation of the incident light will occur and then the optical pass becomes nod. With the precise control of the applied field, intermediates states can be realized. Therefore, this cell can works as an amplitude modulator combined with polarizers and as a phase modulator without an output polarizer. Please note that as an amplitude modulator, phase should be also modulated. As phase modulators, it is ideal to use homogeneous LC cell that the LC molecules are not twisted.

Fig. 2

This figure shows the classification of LCDs and they are mainly classified as matrix addressing and optical addressing that incorporates the photo-conductive material. Our interests are matrix addressing and it classified to TFT with independent switching gates and TFD without independent gates. We are focused on TN and Homogeneous LCDs with MIM diodes as TFD.

This figure shows the matrix addressing of each pixel. The timing pulse comes serial to row electrodes and data signals come parallel to column electrodes and each intersection point contacted through LCs works as a pixel. To use the switching devices, we can drive the each pixel more independently compared to passive addressing without SW devices.

Fig. 3

This figure shows the structure and electrical characteristics of MIM diodes. The MIM structure is a thin film insulator sandwiched between conductive layers and then work as bi-direction diodes. This is an equivalent circuit connected serial with LC cell. To inject charges sufficiently and then hold them in the LC cell, the low capacitance and high charge transfer rates of the MIM and high impedance of the LCs are important factors. This graph is a V-I characteristics of MIM. We consider this Vth. as switching voltage.

Fig. 4

This figure shows the LC cell structure with MIM diodes and its fabrication process using only two masks. Fist Ta sputtering and mask patterning to fabricate conductor, then anodic oxidation to fabricate insulator and ITO sputtering and masking to fabricate electrodes with additional function of the conductor. So the MIM bi - diodes fabricated in this process has non symmetric characteristics so we have to compensate using double MIM or non symmetric driving. In case of 3 mask process, Ta sputterring and masking before ITO patterning.

Fig. 5, 6

This is a photograph of a pixel with an MIM diode. This circled area is a MIM area.

This graph shows the typical V-I characteristics of 2 and 3 mask MIM diodes. Please note that the Y axis is a log scale. We can see that Vth. of 2 mask process is non symmetric but higher than that of 3 mask process that will lead the high driving abilities.

Fig. 7, Table 1

This is a photograph of our typical SLMs and its specifications are shown in the table. Type B has a more fine pixel but type A has a more large number of pixels. We can drive the SLM easily by composite video signals from CCD or VCR. From the photo that we can see the ICs are directly bounded on the glass substrates called COG technology. To use this technology, the number of FPC connectors are dramatically reduced.

Fig. 8, Table 2

This photo is one portion of driving ICs and these are contact point arrays. This is a sectional view of the contact point. The ICs and ITO electrodes of an LC cell are electrically contact through these points. This table shows the data IC specifications and we can realize 22 μ m connection pitches in other words 22 μ m pixel pitches.

Fig. 9

This is a typical sectional diagram of our LCDs. We can see from the diagram that the optical flatness is very good. In case of 1 inch diagonal panels, the flatness is $\lambda/4$. The problem is that the XY matrix electrodes works as diffraction gratings due to the index mismatching between ITO and alignment layer. These are power spectrum of the LCDs. We can see the spectrum of matrix electrodes.

Fig. 10

To investigate the difference between TN and Homogeneous LCDs for holograms, we measure the beam spot profiles of power spectrum of LCD gratings with binary modulations. This is an measuring optics. From the results, the spot size become small and side lobe are increased using the 90 deg. TN - LCDs. In case of homogeneous LCDs, the spot profile is same as optics itself because of no modulation of incident linear polarization.

Fig. 11

This figure shows the rectangle phase grating with a phase delay of ϕ and it is mathematically represented as eq. (1) and (2). Eq. (3) is its Fourier spectrum. From eq. (3), main factors of 0 and 1 st order are represented by these equations. Both orders are modulated to the phase of ϕ, but 1 st order has a component of π modulation. This is the key to the polarization modulations.

Fig. 12, 13

This is a sectional diagram of binary phase gratings using TN LCDs. Voltages are applied according to the grating patterns. The direction of the polarization vector rotate to θ according to the intensity of the applied voltage. Naturally, maximum value of θ is 90 deg. ϕ means a phase delay. These are graphs of the polarization vector of 1 st and 0 order. In 1 st order, the phase of one component jumps to π. We can clearly see that the result polarization vector becomes different. In case of 0 order, the result starts from linear polarization of the X and then rotate and become elliptic. In case of 1 st order, it started from linear polarization of Y states and rotate and become elliptic quickly. Please not that this phenomena will not occur in homogeneous LCDs.

Fig. 14

Those are experimental results of polarization modulation between 1 st and 0 order light. As expected, 0 order start from X and linear and 1 st order start from Y and liner. With voltage increases, both rotate and 1 st order become elliptic quickly.

Fig. 15

Those are simulated results and they are almost fit to the experiments. But we neglect the influence of birefringent effects of LCDs. From these results, we can remove the 0 order light using polarization filtering and show its result later.

Fig. 16

This figure shows the optics for electro-holography. The optics is almost equal to the conventional optical holography but the CCD and the LCTV-SLM are used instead for photographic films. As recording, the laser beams divided into two beams, one is called a reference beam and it travels CCD directly. The other beam called an object beam hit the object and then diffracted to the CCD. Those two beams will interfere on the CCD and make the holograms that incorporates 3D information of the object. The angle between these two beams on the CCD is set almost zero so that the career spatial frequency of the hologram is very low according to the resolution limit of the CCD and LCTV-SLM. The object is imaged on the CCD by this imaging lens making this hologram as an image hologram that can reconstruct by incoherent light. The bandwidth of the holograms are limited by this aperture.

On reconstruction, the holograms are transferred and displayed on the LCTV-SLM that is illuminated by collimated laser beam. Because of the low career spatial frequency of the hologram, the direction of the 1 st and 0 order light is almost the same. So the spatial filtering technique is used to remove 0 order light that has no information of the objects. Power spectrum of the LCTV-SLM is recorded on this mask. We can see reconstructed image through this mask.

Fig. 17

This figure shows typical spatial frequency response of our electro-holography. Please note that this includes the overall response of the CCD, LCTV-SLM, and their driving electronics. X axis shows spatial frequency of the LCTV-SLM and Y axis shows normalized diffraction efficiency. According to the pure phase modulation characteristics, the efficiency using the homogeneous LCD is the best.

Fig. 18

This is a photo of the object. Its size is about 10 mm. This is a hologram displayed on the CRT monitor. This is an image hologram, so that we can see the shape of the object. The career spatial frequency is set to 5 [lp/mm] and its bandwidth is set to 30 [lp/mm]. This is a reconstructed image using homogeneous LCD and this is its binary modulation. We can see the brighter image. This is using a TN LCD. We can see clear images thank to the spatial filtering technique. But the low limit of the spatial frequency of the hologram, image quality is not so good. So that it is difficult to catch the substantial difference of each image. Further more, it is also difficult to catch the 3D information. As electro-holography, while object is moving also the image is moving in real time. But the image is disappeared during the moving periods. Importance of the results is that our SLM has an ability to apply 3D holograms and this is a first step to electro -holography using the LCTV-SLM.

Fig. 19, 20, 21, Table 3

Fig. 19 shows the result of polarization filtering to TN LCD gratings. We can see that the 0 order light is almost removed. We apply this technique to our electro holography system and results are on fig. 20. We can see the image with polarization filtering. Fig. 21 and table 3 show our latest research products.

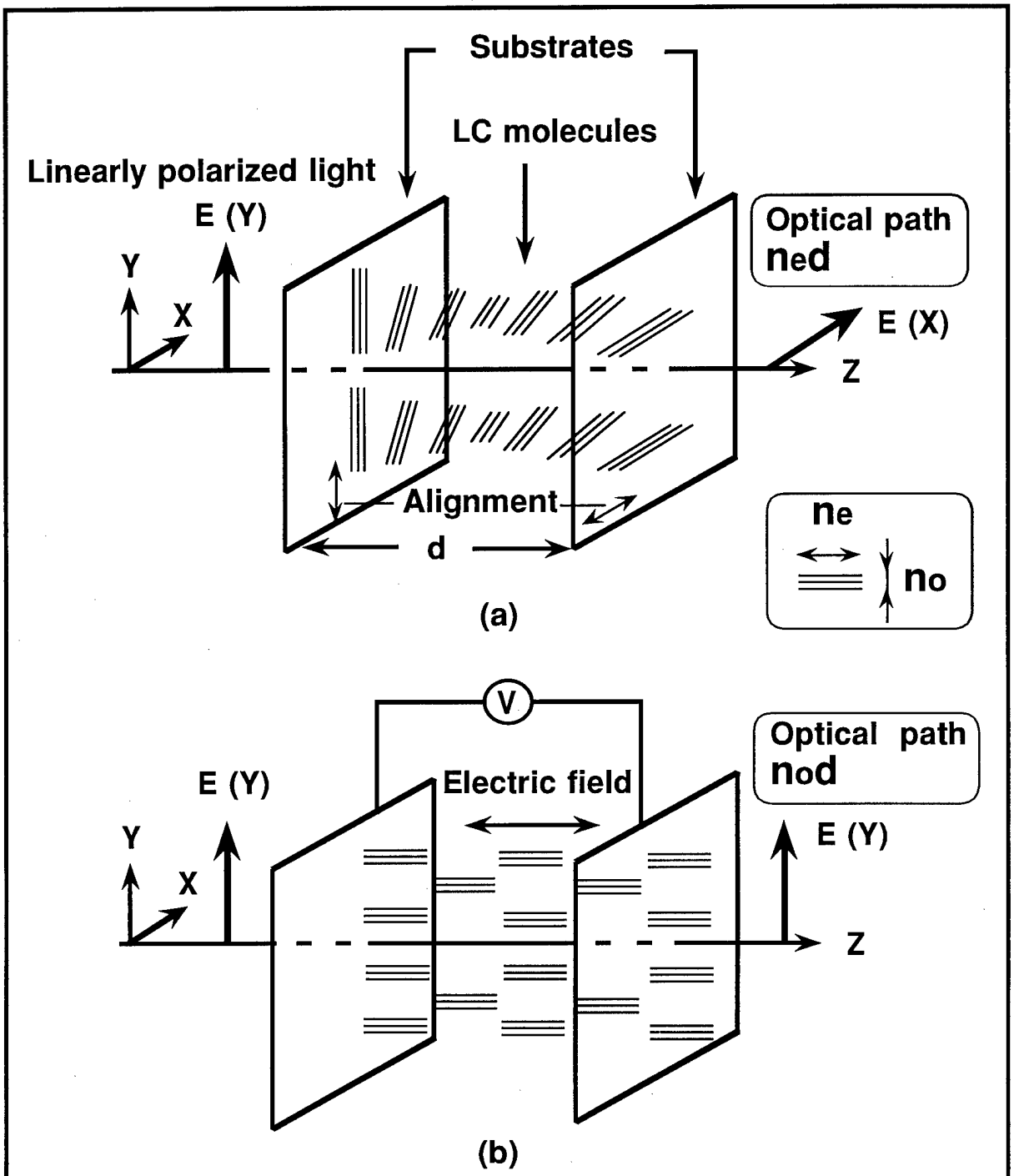


Fig. 1 A schematic diagram of complex amplitude modulation of light using a 90 deg. TN liquid crystal cell.

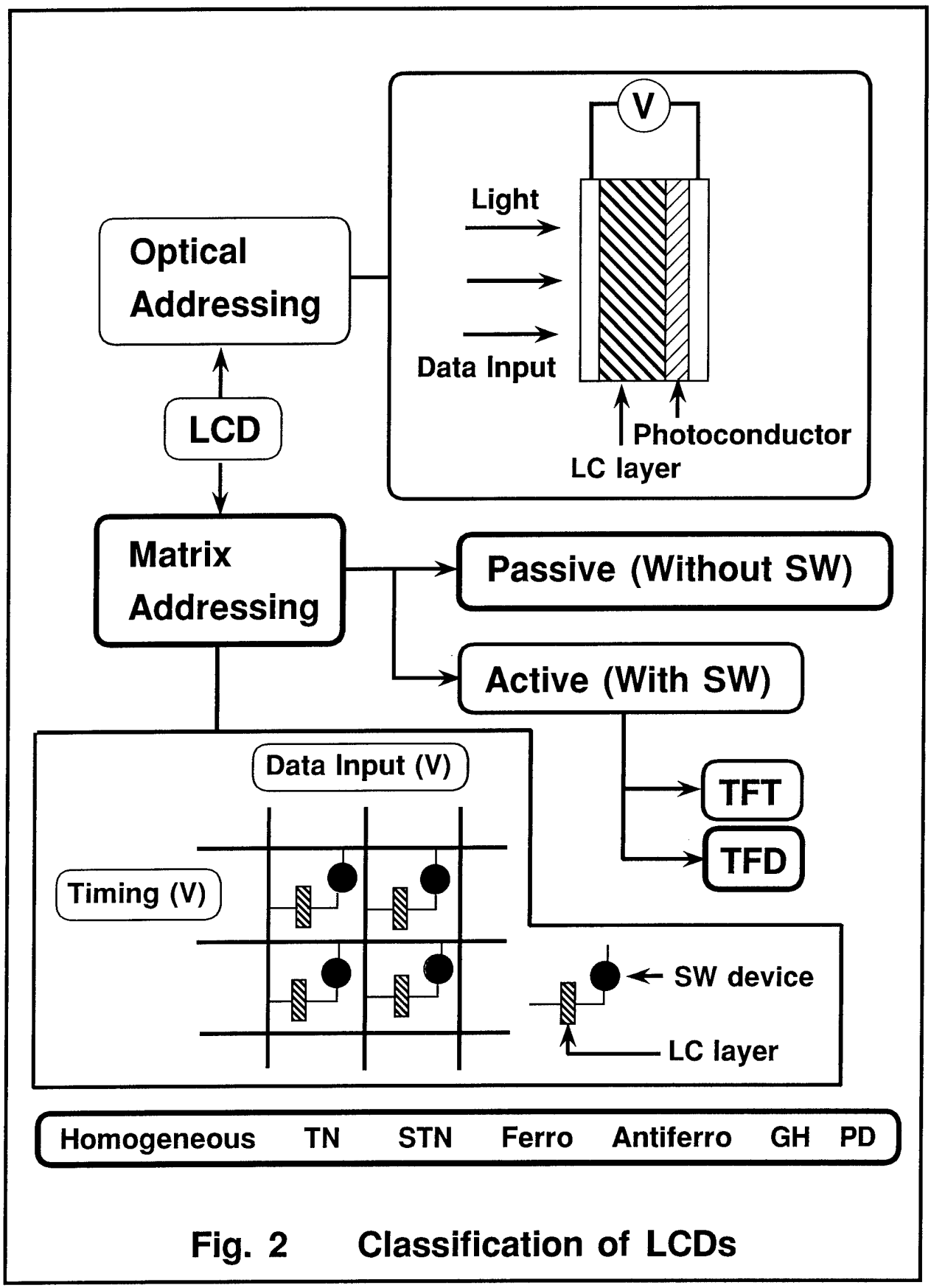


Fig. 2 Classification of LCDs

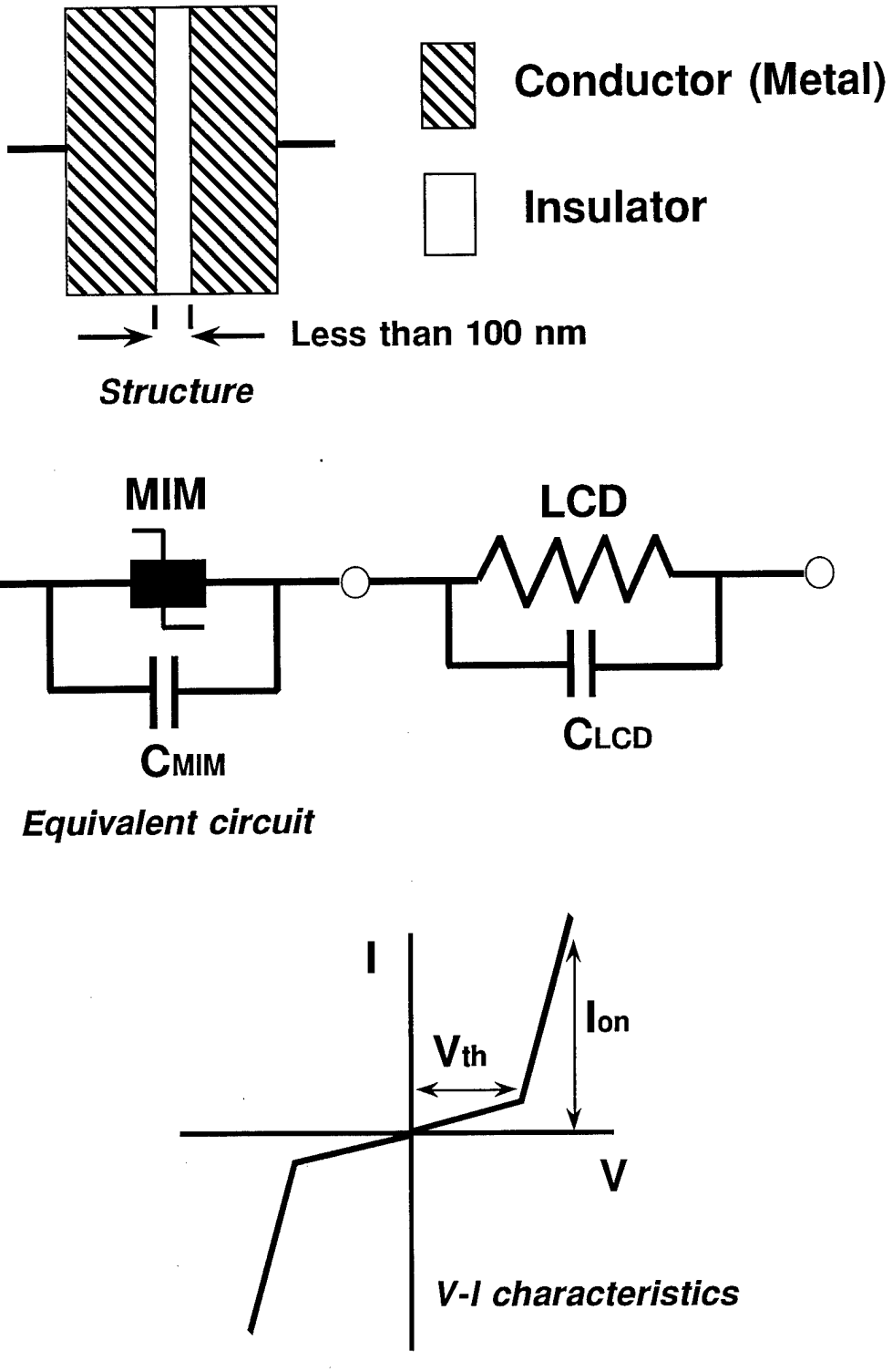


Fig. 3 MIM diode and its characteristics

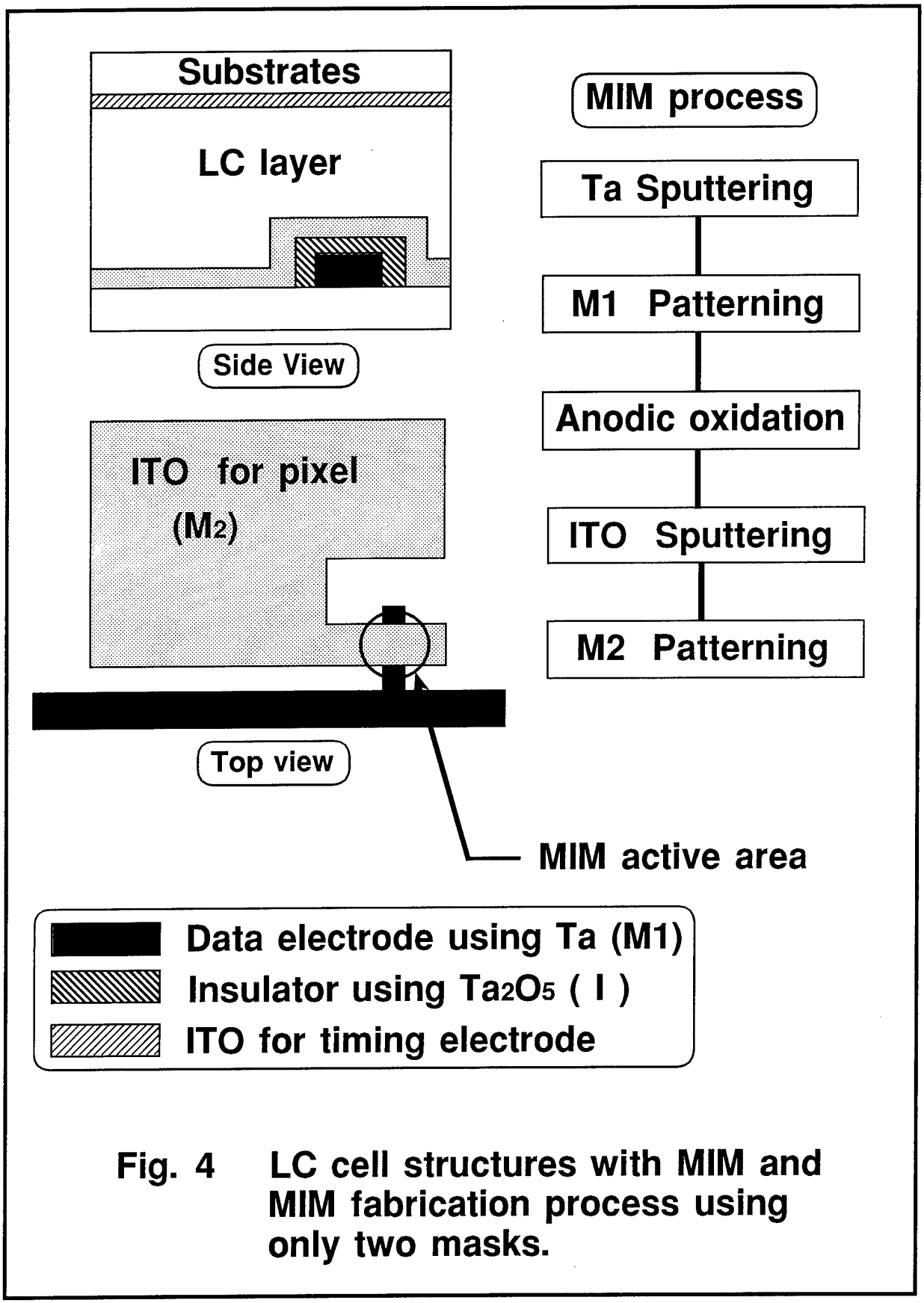


Fig. 4 LC cell structures with MIM and MIM fabrication process using only two masks.

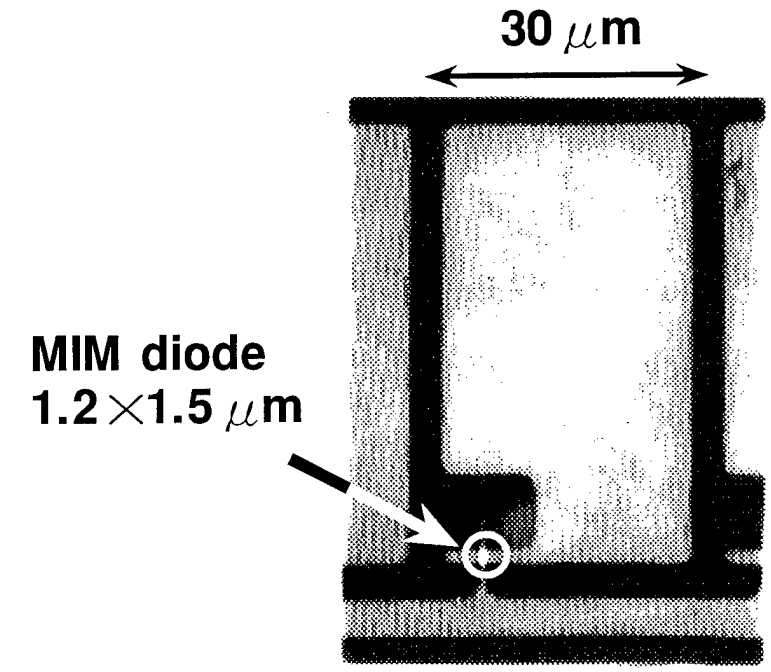


Fig. 5 Photograph of a pixel with an MIM diode

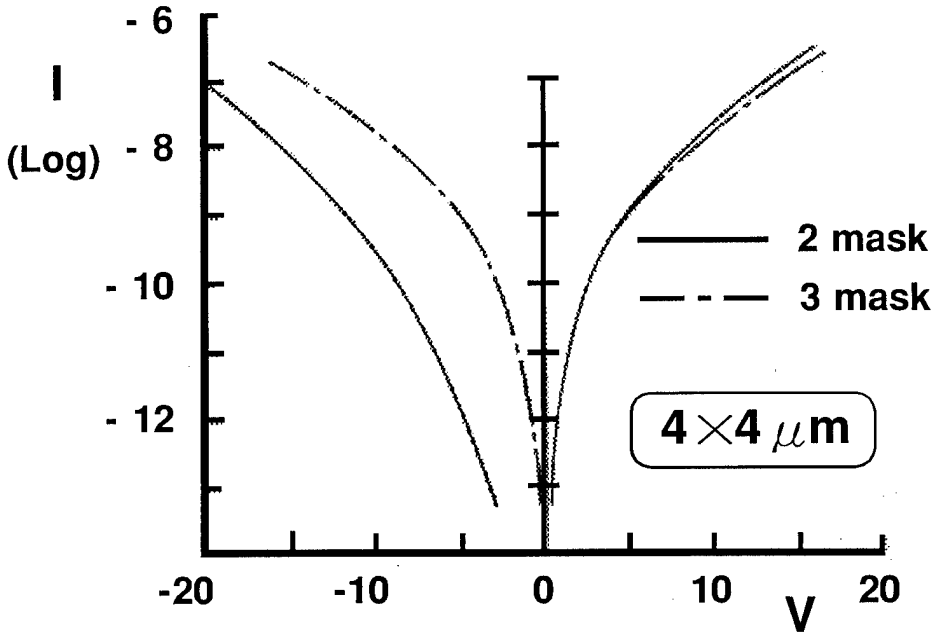


Fig. 6 V-I characteristics of 2 and 3 mask MIM diode

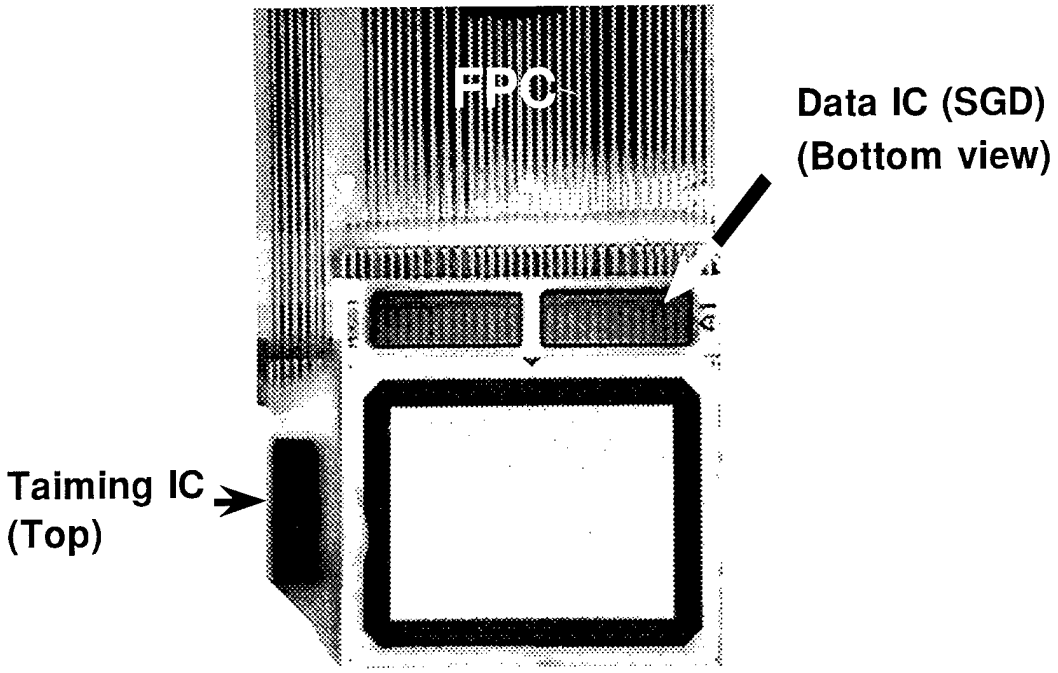


Fig. 7 A photograph of the LCTV-SLM

Table 1 Specifications of the LCTV-SLMs

Type	A	B
Displaying area	19.4×14.4 [mm]	14.4×10.8
Number of pixels	648×240	480×240
Pixel pitch	30×60 [μm]	30×45
MIM size	1.2×1.5 [μm]	←
Cell gap	3 or 4 [μm]	←
Δn (n_e-n_o)	0.148	0.1
Fill factor	61 %	48 %
LC mode	90 or 0 deg. TN	←
Grey scale	16 or 32	←
Interface	Composite Video	←

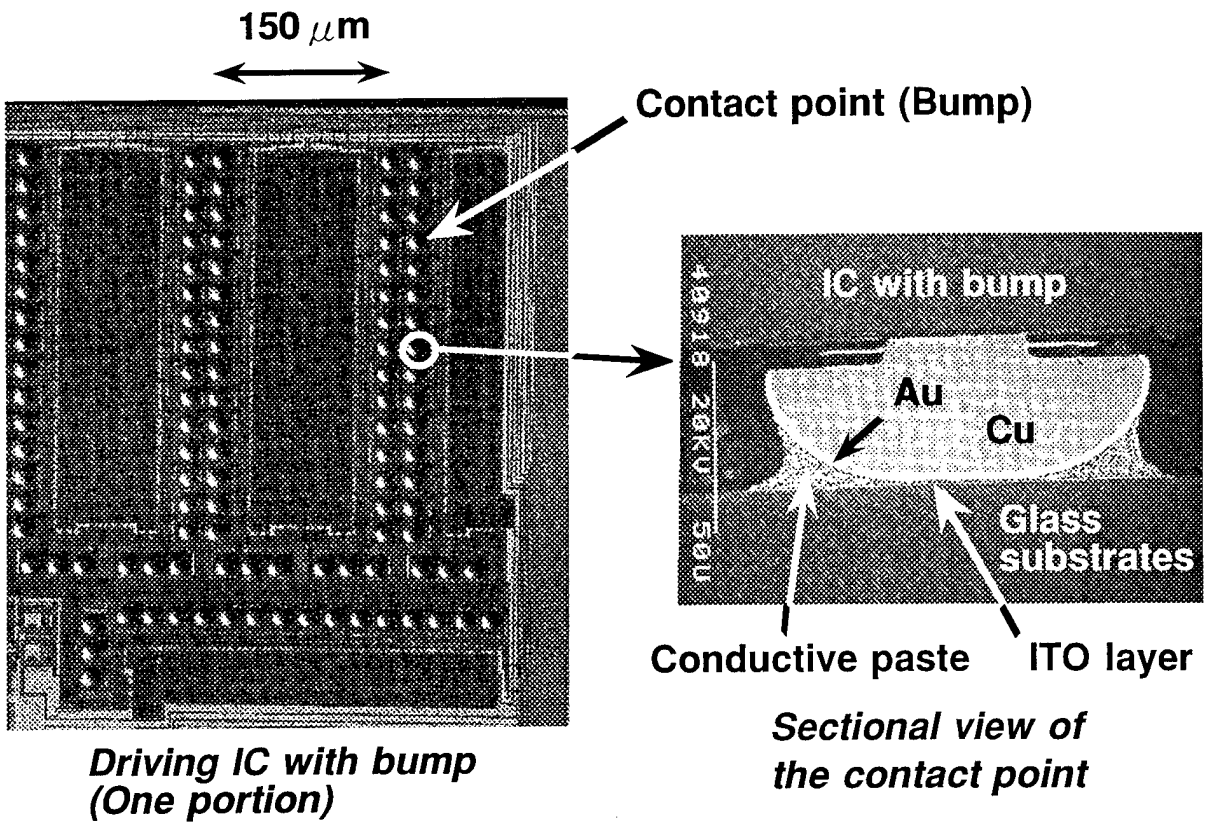
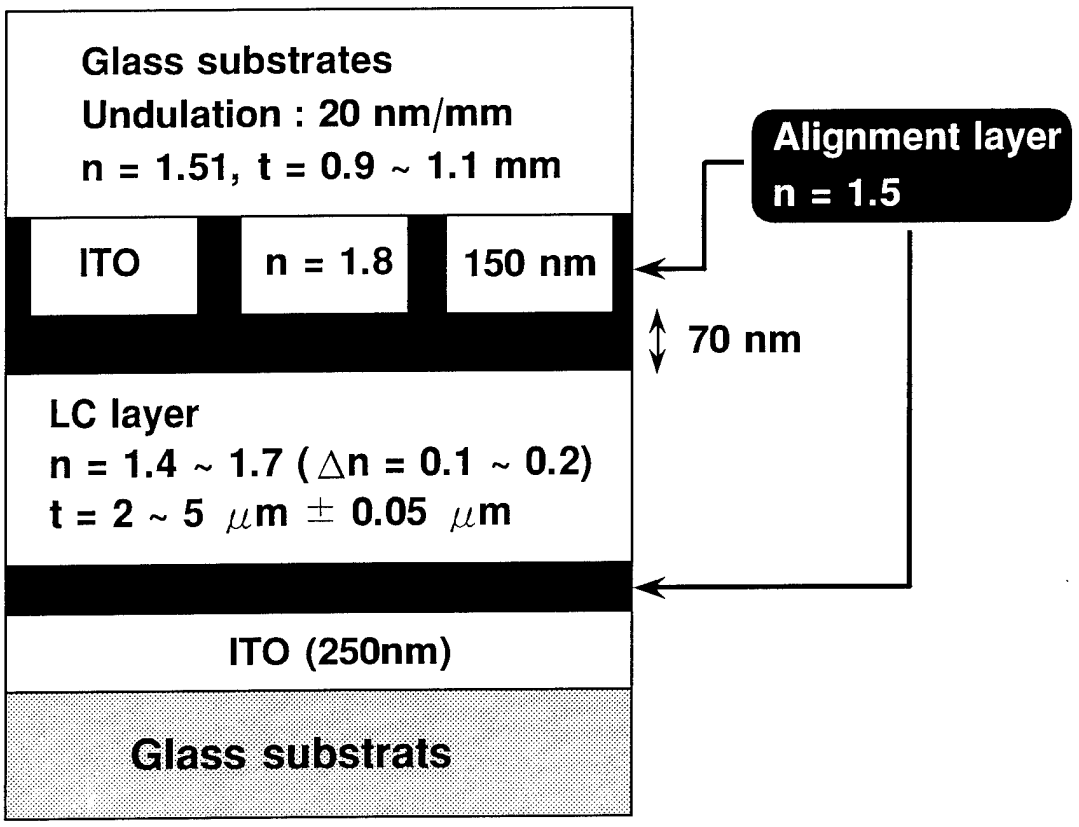


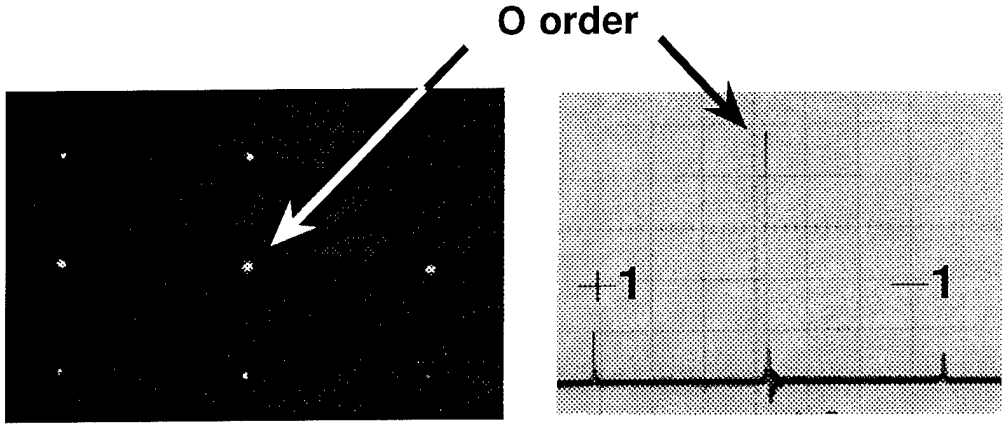
Fig. 8 COG technology

Table 2 Data IC specifications

Size	14.4 × 2.7 [mm]
Number of connection	650 or 324
Connection pitch	22 [μm]
Output voltage	Max 10 [V]
Clock	Max 25 [MHz]

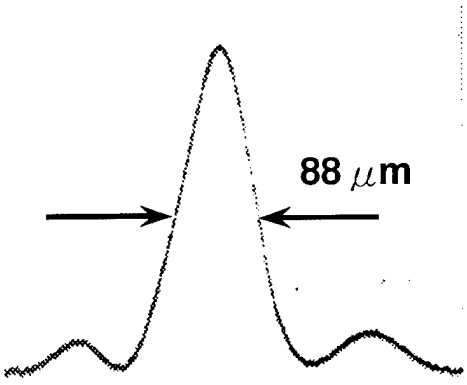


Sectional diagram

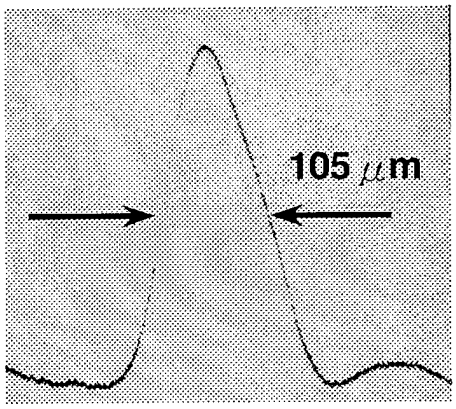


Power spectrum

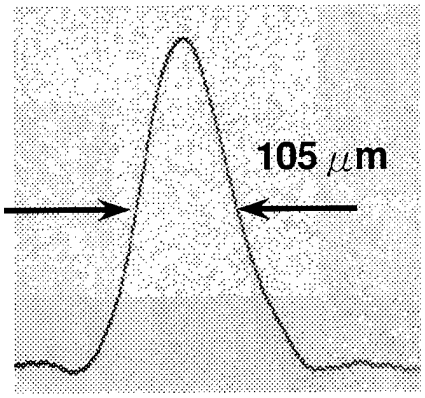
Fig. 9 Optical properties of Matrix LCDs



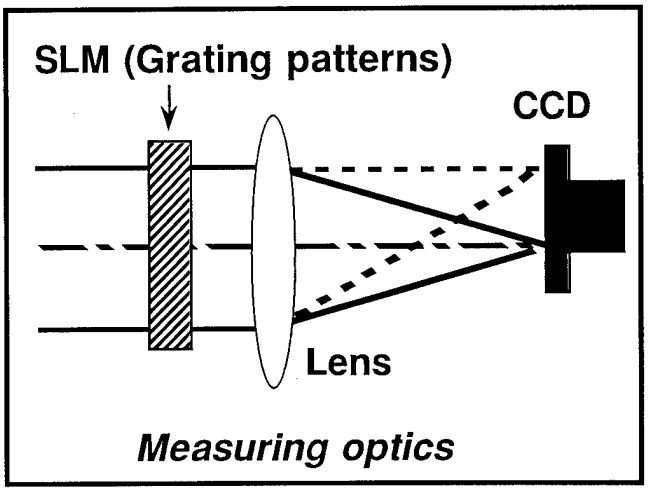
90 deg. TN-LCD



Homogeneous LCD



Ref. Without LCD



Measuring optics

Fig. 10 Beam spot profiles of power spectrum using LCD gratings (Binary modulation) and its measuring optics

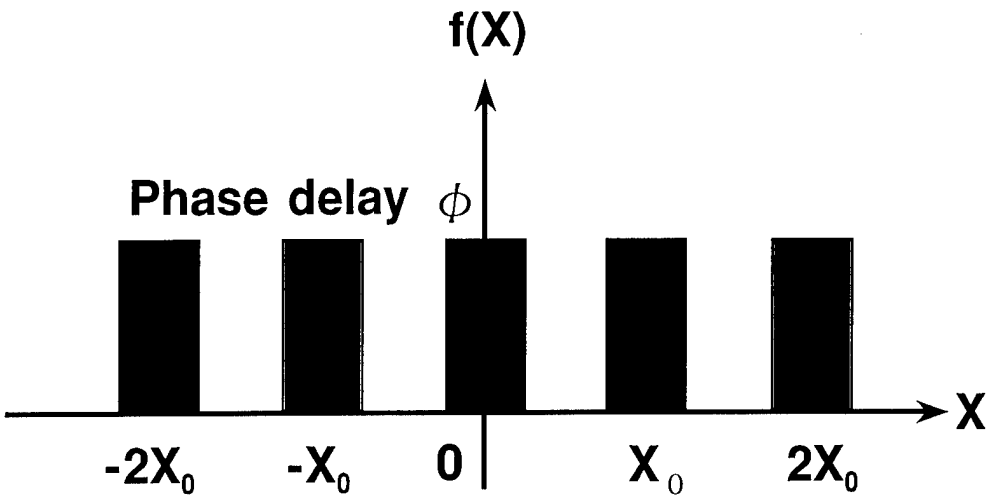


Fig. 11 Rectangle phase grating (Infinite aperture)

$$f(X) = \phi \ \mathrm{rect}\left(2X / X_0 \right) * X_0^{-1} \mathrm{comb}\left(X / X_0 \right) \quad \text{— (1)}$$

($*$: ***Convolution***)

$$h(X) = \exp\left[i \, f(X) \right] \quad (i : \textit{Complex unit}) \quad \text{—— (2)}$$

$$H(\xi) = \mathcal{F}\left[h(X)\right] \quad (\mathcal{F} : \textit{Fourier Transform})$$

$$= 0.5 \ \mathrm{sinc}\left(\xi / 2\xi_0 \right) \Sigma_n \, \delta(\xi - n\xi_0)$$

$$\times \{ \exp(i \, \phi) - 1 \} + \delta(\xi) \quad \text{—— (3)}$$

$$(\xi_0 = 1 / X_0)$$

From the eq. (3)

0 order : exp (i ϕ) + 1 (1 = exp (i 0))

1 order : exp (i ϕ) - 1 (- 1 = exp (i π))

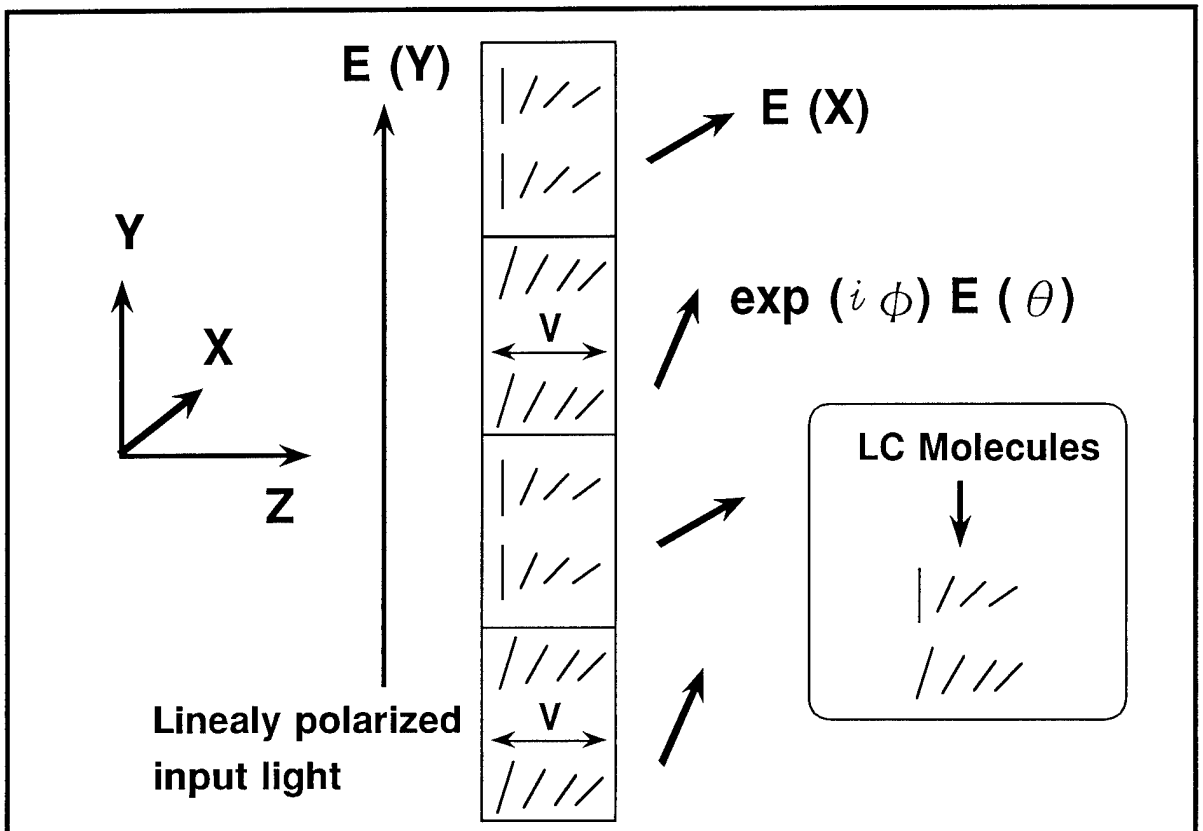


Fig. 12 Binary phase gratings using 90 deg. TN - LCDs (Sectional diagram)

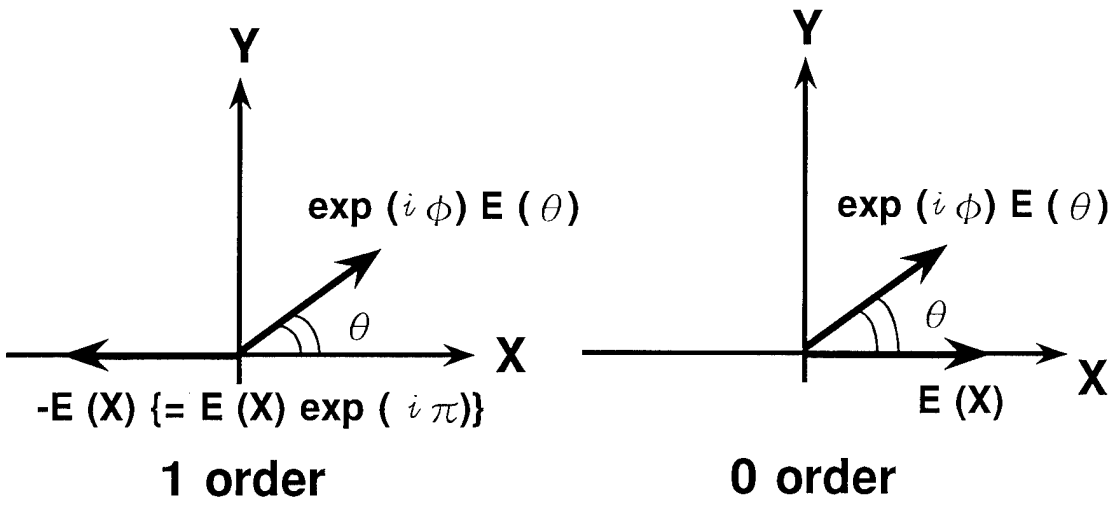


Fig. 13 Polarization vector of the diffracted light

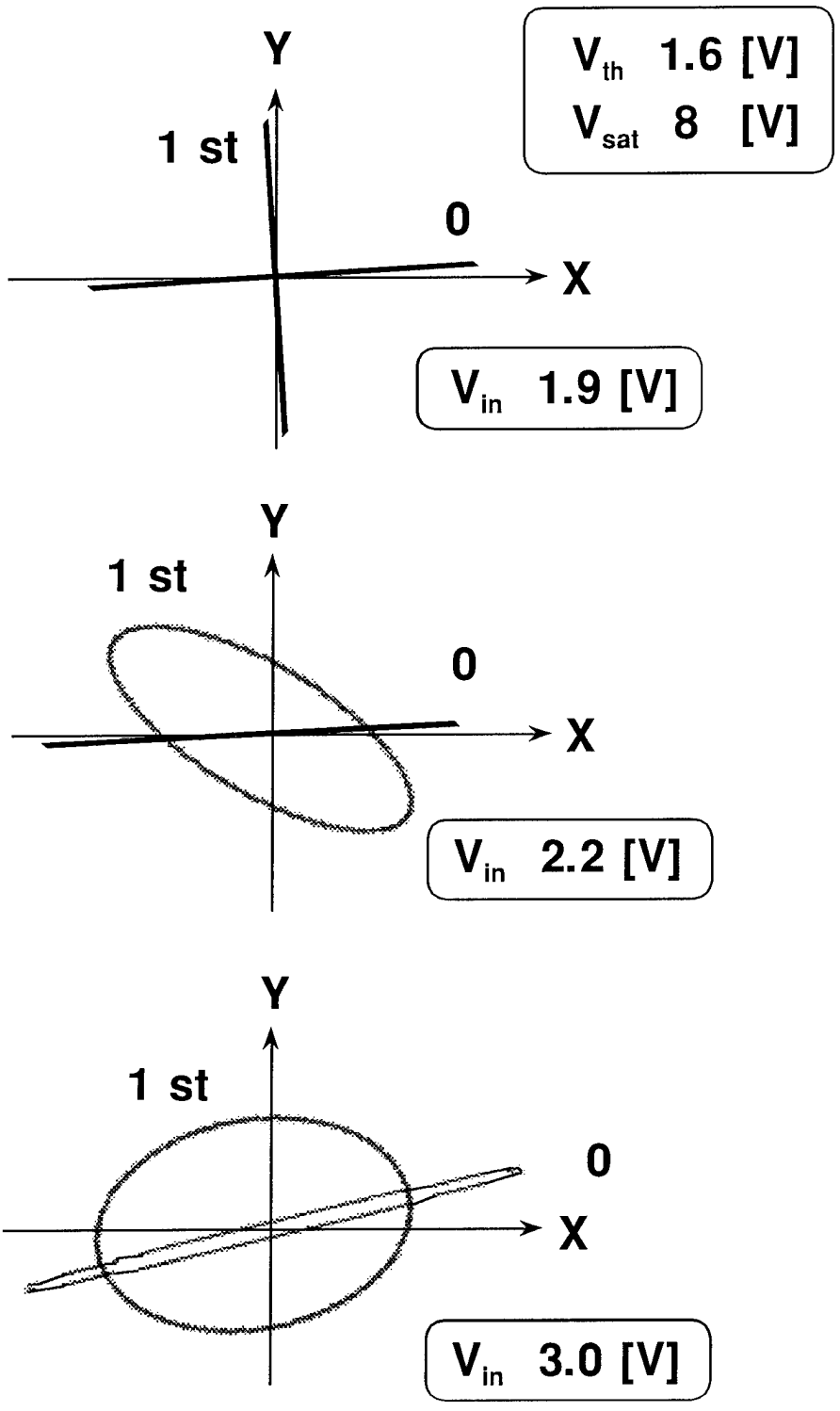
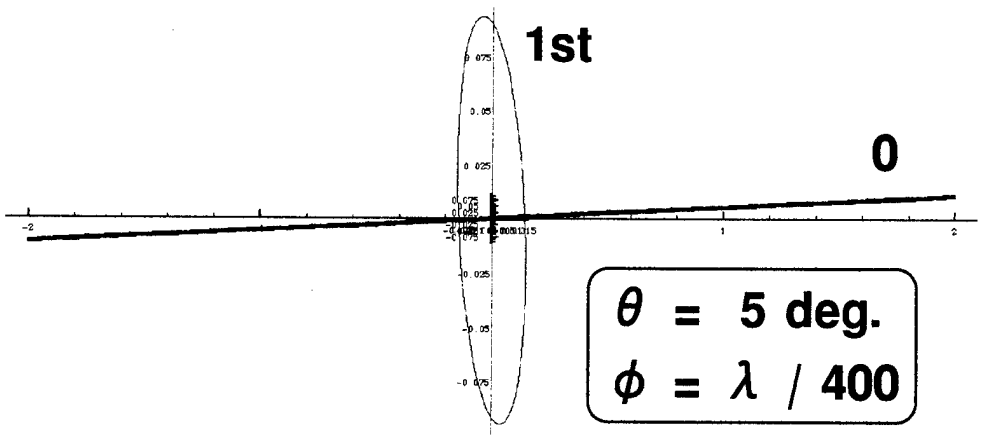
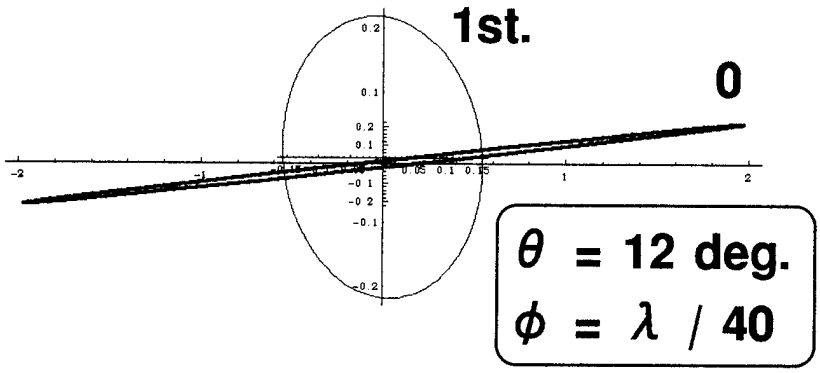


Fig. 14 Experimental results of polarization vector modulated by TN - LCD gratings





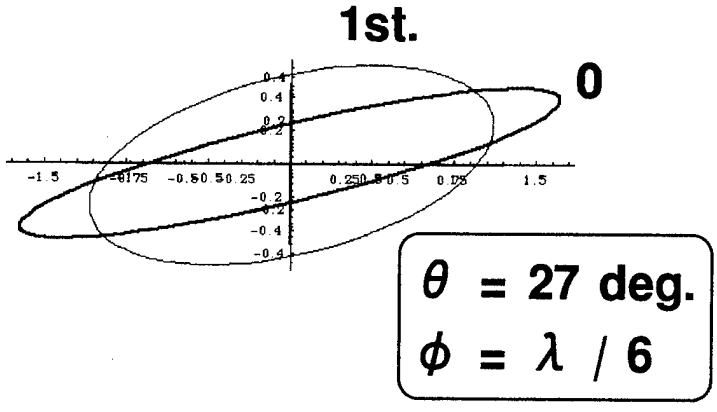


Fig. 15 Simulated results of polarization vector modulated by TN - LCD gratings

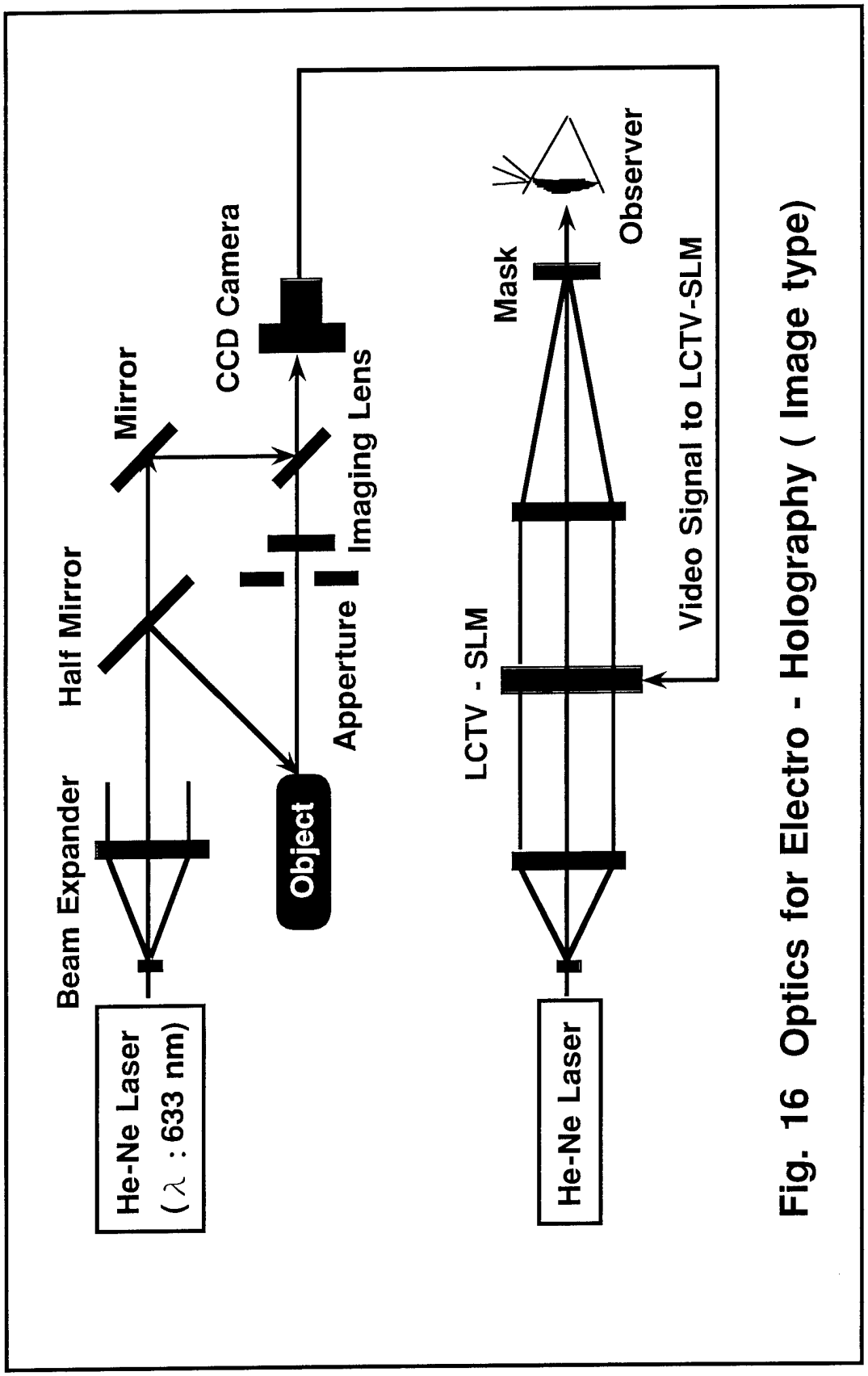


Fig. 16 Optics for Electro - Holography (Image type)

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Viewgraph

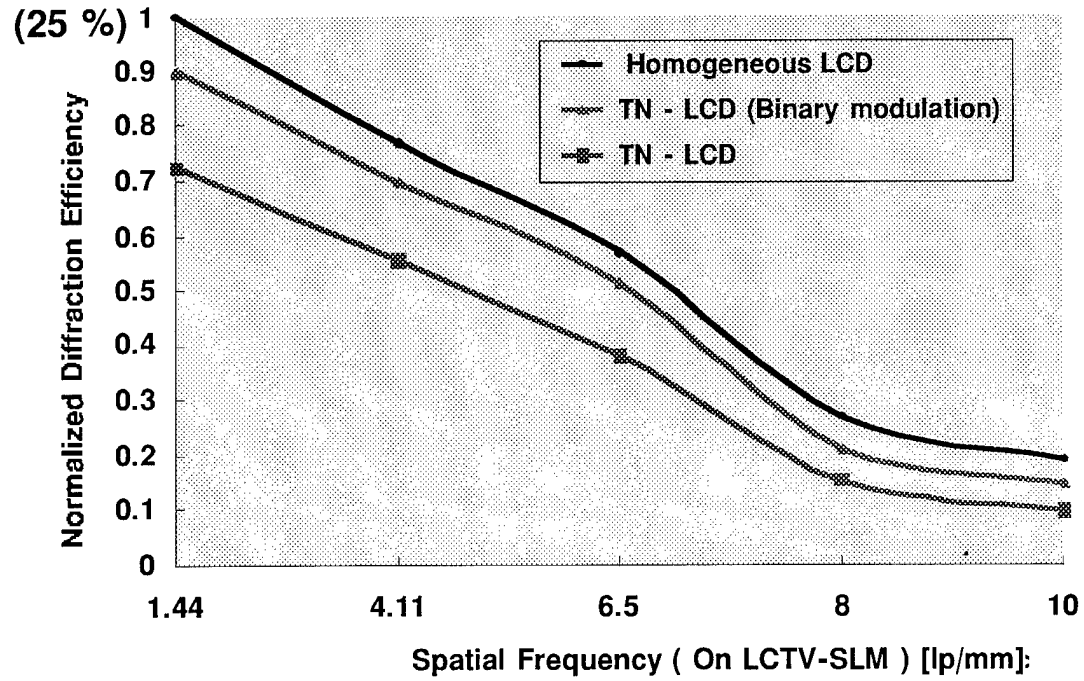
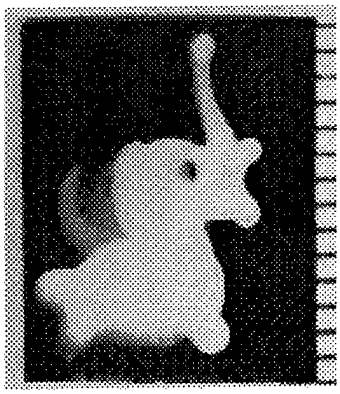
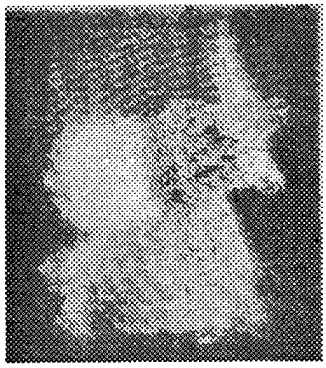


Fig. 17 Typical spatial frequency responce of the electro-holography system using an LCTV-SLM

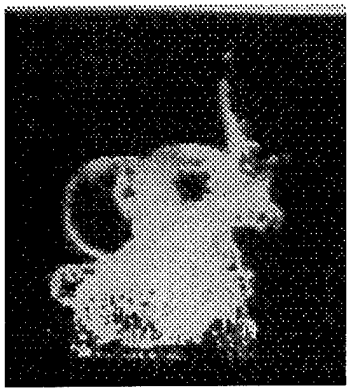


An object

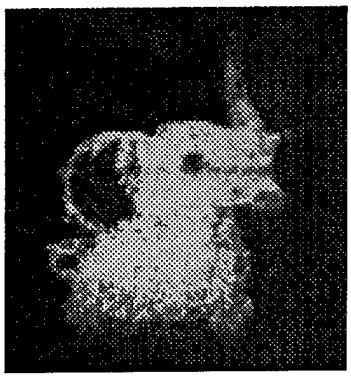


Its hologram
(Image type)

A reconstructed image using homogeneous LCDs



A reconstructed image using homogeneous LCDs with binary modulation



A reconstructed image using 90 deg. TN - LCDs

Fig. 18 Experimental results of erectro holography using LCTV - SLMs

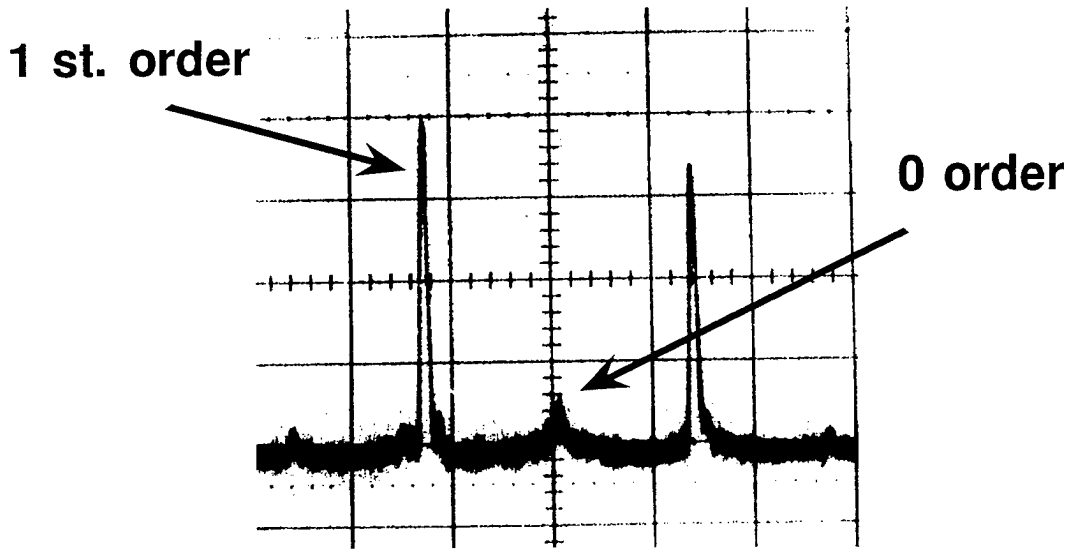
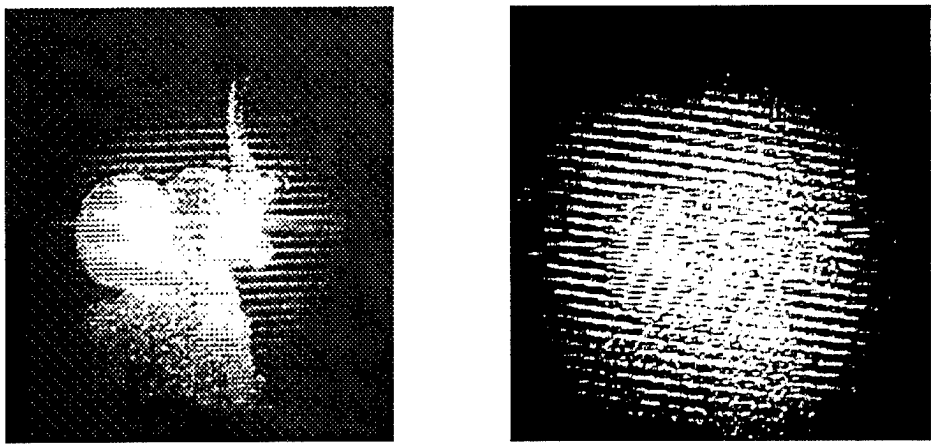


Fig. 19 Power spectrum of TN - LCD gratings using polarization filtering



(a) **(b)**

Fig. 20 Reconstructed images from LCD holograms (a) with polarization filtering and (b) without polarization filtering

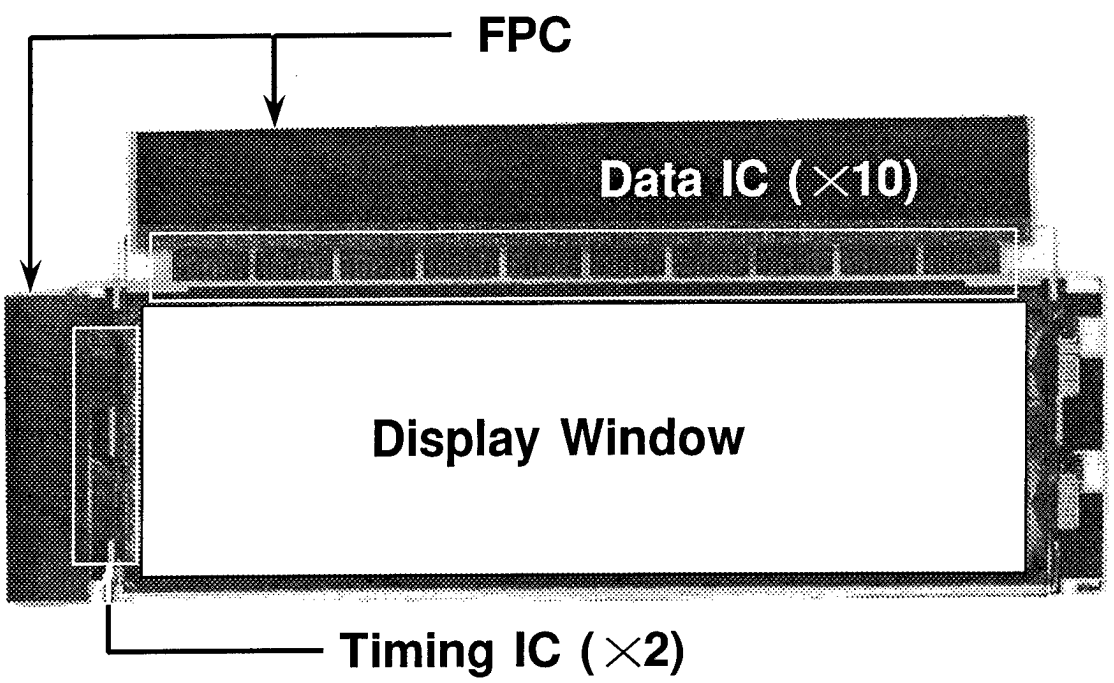


Fig. 21 A photograph of the LCTV - SLM

Table 3 Specifications of the LCTV-SLM

Type	A	B
Displaying area	115×69 [mm]	40×40
Number of pixels	3200×960	960×960
Pixel pitch	36×72 [μm]	42×42
Drive	MIM	←
LC mode	TN or Parallel	←
Interface	Digital	←

Summary

Liquid crytal devices are suitable devices for SLMs because of thier strong dielectric anisotoropy and high - sensitivity to electric fields

The high - resolution LCTV - SLMs using MIM active matrix technology have developed and they could apply 3D - holographic devices

Properties of LCD gratings were investigated and the results could apply polarization filtering to remove 0 order light

3 M-pixel LCTVs using MIM technology were demonstrated

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A planarized LCOS display for projection applications

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Abstract

We have constructed a 640 x 512 pixel Liquid Crystal on Silicon microdisplay. We shall describe the application driving the device development, the display device and the technology enhancements implemented for this application.

Topics: Active-Matrix Liquid-Crystal Displays, Display Systems, Planarization

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Geoffrey Burdge and Sadik C. Esener (eds.)

A planarized LCOS display for projection applications

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(303) 492-3260

Introduction

Liquid Crystal on Silicon (LCOS) spatial light modulators (SLM's) and microdisplays are made by placing a thin layer of liquid crystal directly on top of a silicon chip. We have constructed a high speed 256 by 256 binary SLM which uses a ferroelectric liquid crystal as the light modulating layer [1]. We have also recently constructed a high speed distorted helix effect analog 128 by 128 SLM [2] and a high voltage 128 by 128 analog SLM using the electroclinic effect in BDH764E [3]. This work has been motivated by the performance requirements of coherent applications which typically include high frame rate, small pixel pitch and good diffraction efficiency into a single (zeroth) diffracted order. These devices have been successfully used in optical correlators and holographic interconnect systems [4].

Liquid Crystal on Silicon Microdisplays

The requirements for a projection display system emphasise different aspects of the device design. For example, in the automotive Head Up Display (HUD) application which is motivating our current device development [5], we illuminate the liquid crystal on silicon device with over two orders of magnitude more optical power than in an optical correlator. This difference is important for the device design since photogenerated charges in the silicon substrate cause leakage currents which in turn lead to loss of image contrast. On our binary 256 by 256 device, which was optimized for single–order diffraction efficiency rather than optical power handling, the image begins to degrade at $\approx 30\text{mW/cm}^2$ of visible light illumination at 25,000 frames per second electronic refresh rate.

In other respects, LCOS technology is well suited to display applications. The small size of the device can lead to a compact image engine for systems with packaging constraints and the high frame rates (kHz) available lend themselves for use in time–sequential color and/or grey–scale schemes. We present results from a 640 x 512 color microdisplay designed for this HUD application.

Active-matrix backplane

The microdisplay's active-matrix backplane contains 640 x 512 DRAM-style pixels fabricated in a 1.2 μm CMOS process. The pixel pitch is 21.4 μm, giving the display a 0.7" diagonal active area. CMOS circuitry was used for on-chip clocking and control, shift registers, and test structures. The backplane was designed for a nominal electronic refresh rate of 8,000 frames per second.

The display is intended for field sequential color operation and was designed to operate in either digital or analog image display mode. In digital mode, the display is

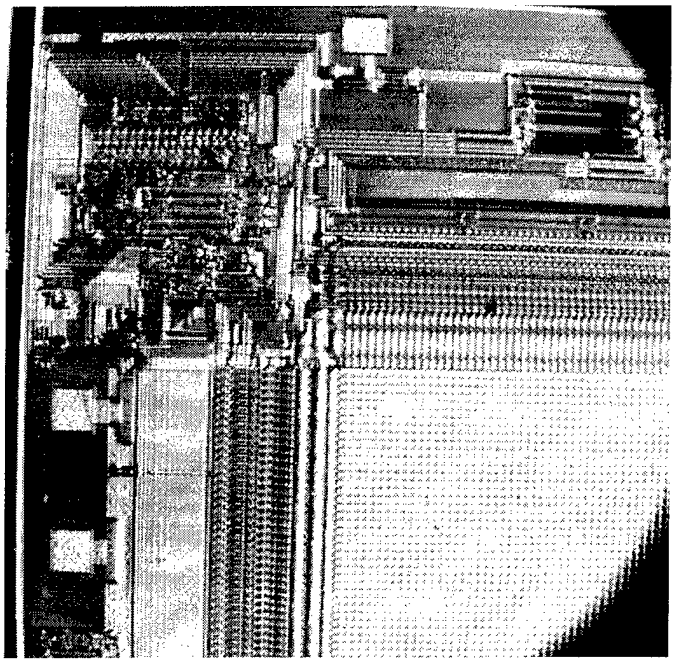

Figure 1: Photograph of the upper right corner of a planarized 640 x 512 pixel LCOS microdisplay.

capable of 9-bit total (3-bit per color) color at 100 Hz frame rate. In analog mode, the device provides 16 gray levels at 60 Hz frame rate.

Alignment marks were also fabricated on the wafer to facilitate the planarization post-processing. The first die have been packaged and electrical testing of the devices is underway. Figure 1 is a photograph of a corner of a planarized 640 x 512 pixel LCOS device.

Backplane post-processing

In planarizing a silicon backplane, a flat dielectric layer is formed above the device circuitry. The flat dielectric layer provides several benefits for image display devices. Finer resolution lithography is possible on the flatter surface, thus reducing the separation between pixel mirrors and increasing the pixel aperture ratio. High reflectivity metal can be deposited on top of the dielectric layer to form the device's mirrors. Increases in pixel aperture ratio and reflectivity improve the device's optical efficiency while simultaneously creating better light shielding of the underlying pixel circuitry. In addition, the extra metal layer allows for underlying metal layers to be utilized as overlapping, interpixel shielding as well as low resistance addressing lines. Low resistance address lines are important for increasing display resolution while maintaining the frame rate and pixel pitch. For example, metal2 (sheet resistance $\approx 0.036\ \Omega$ per square) can be used for pixel data and select addressing lines in this three-metal process in place of polysilicon (sheet resistance $\approx 22\ \Omega$ per square). The signal propagation delay, t_l, along a long transmission wire is approximated by,

$$t_l = \frac{R_s c l^2}{2w} \tag{1}$$

Table 1: BCB planarization results summary

BCB layer thickness	2.248 +/- 0.039 μm
Ave dry etch rate ($SF_6 + O_2$)	0.25 μm per min
Patterned via diameter	$2\mu m$
Etched via diameter	$\approx 3.6\mu m$
Average via resistance	0.75Ω per via
Pixel aperture ratio	84 %
Pixel flat-fill factor	82 %
Pixel reflectivity	87 %

where R_s is the material sheet resistance, c is the line capacitance per unit length, l is the length of the wire, and w is the width of the wire [6]. For similar line capacitances, this implies a reduction in signal delay for metal address lines of two orders in magnitude as compared to identically sized polysilicon address lines. The use of metal address and data lines allows larger, higher resolution displays to maintain high frame rates.

The planarizing dielectric layer also hides complex pixel structures (e.g. SRAM elements, see [9]), providing enhanced display functionality without contributing to light scattering by nonuniform pixel structures. Finally, planarization appears to improve liquid crystal alignment layer uniformity, thus presenting a more uniform image to the observer's eye [8].

The planarization method we have pursued employs spin-coating Benzocyclobutene (BCB or Cyclotene by tradename [7]), a polymeric resin from the Dow Chemical Company, onto the silicon substrate. The resin is thermally cured, vias are dry etched, metal is deposited, and then patterned to produce upper layer mirrors. Thermal curing of the BCB can be rapidly performed (in 5 minutes). The local planarity of BCB is very good (a single BCB coat can reduce the substrate step height by an order of magnitude) and global planarity is acceptable for HUD applications.

Post-processing of the backplane was performed under the NSF-sponsored National Nanofabrication Users Network program at Stanford University. Test wafers with via chains and large mirror arrays were fabricated first to verify the process parameters and uniformity.

Table 1 summarizes the results of our planarization efforts. The average coating thickness measured at five points per wafer over six metal-on-silicon test wafers is 2.248 +/- 0.039 μm. Vias are dry etched in the BCB layer using $CF_4 + O_2$ (average etch rate 0.21 μm per minute) or $SF_6 + O_2$ gas chemistries (0.25 μm per minute). For a 2 μm patterned via diameter, the resulting via diameter after dry etching is $\approx 3.6\mu m$. The average resistance measured over 1000 vias in a via chain is 0.75 Ω per via. 5,000 angstroms of pure aluminum is then deposited as the upper mirror layer. The aluminum is dry etched in a chlorine-based gas chemistry. The resulting mirror separation is $\approx 1.8\mu m$, resulting in an 84 % fill-factor for 21.4 μm pixels.

Conclusions

We presented results on a 640 x 512 pixel liquid-crystal-over-silicon (LCOS) microdisplay intended for projection applications. The backplane was designed to operate in digital (9-bit total field sequential color at 100 Hz frame rate) or analog modes (16 gray levels

per color at 60 Hz frame rate). Electrical testing of the backplane is underway. A spin-cast resin method of planarizing LCOS backplanes was developed. The method provides excellent dielectric layer uniformity, reasonable dry etch rates, good via diameters, low via resistances, and high pixel fill-factor. The planarization and post-processing improves device parameters such as optical efficiency and light shielding while maintaining high frame rates with increasing device resolution and size.

Acknowledgements

This work is supported by the National Science Foundation and Ford Motor Company through the Optoelectronic Computing Systems Center at the University of Colorado at Boulder and the Nanofabrication Facility at Stanford University. The authors would like to thank the Dow Chemical Company for supplying materials and technical assistance in the planarization work. We would also like to thank the staff at the Stanford Nanofabrication Facility for their support and technical expertise during the post-processing.

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Image Processing and Optical Storage in a Resonator with an OASLM

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Abstract

It is demonstrated that optical information can be stored and processed in resonators which include an OASLM and show a bistable behavior.

Keywords

Analog optical image processing, spatial light modulators, photorefractive materials, optical data storage, interferometry

Introduction

Optically addressable spatial light modulators (OASLM's) are not only of use for the introduction of an incoherent intensity distribution to a coherent optical system, but also to realize optical image processing and storage if the same coherent beam is used to write and to read out the OASLM.
In our contribution we report investigations on several optical systems, where the information that was read out coherently from a OASLM is processed by an optical system and then fed back to the rear side of the OASLM. Similar systems have been described in the literature for example to compensate wavefront aberrations in adaptive optics [1], or as a Fabry-Perot type OASLM with internal feedback [2]. We want to demonstrate the image processing and storage capabilities of such systems and will show how both amplitude and phase of a beam can be used for the processing.

Interferometrically Controlled Feedback

The optical arrangement is sketched in Fig.1. The feedback is realized with the help of a Michelson interferometer. The interference pattern formed by one beam reflected at a mirror and a second beam that reads out the OASLM is imaged onto the rear side of this element. So the resulting interference intensity will influence the interference pattern.

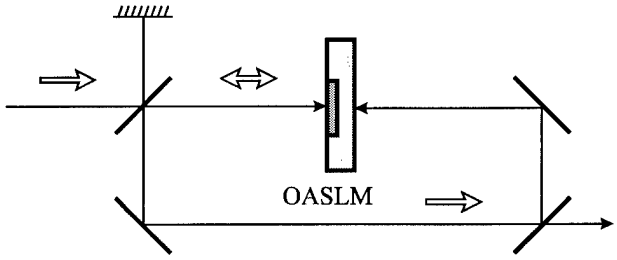

Fig. 1 Michelson interferometer with feedback

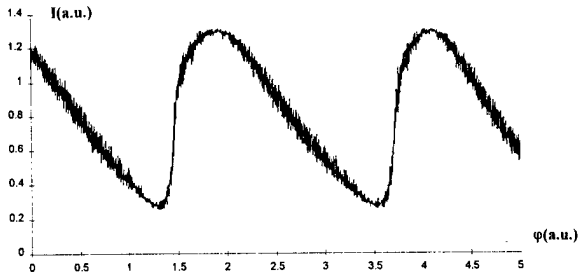

Fig. 2 Interference fringes obtained with the feedback interferometer, according to eq.(1)

With $\kappa(I)$ being the intensity-to-phase transfer characteristics of the OASLM and φ the phase of the beam reflected at the mirror (which can be easily adjusted by shifting the mirror with a piezo actuator), the interference is given by

$$I = I_0\left[1 + m\cos(\varphi - \kappa(I))\right] \qquad (1)$$

Fig. 2 shows an experimental result with an obvious steepening of the slopes of the sine function due to the feed-

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back. This effect will be the subject of further investigations since the phase sensitivity of the interferometer is increased considerably at the steeper slopes. Unfortunately, the used OASLM was not sensitive enough (i.e. the phase shift that could be obtained optically was too small) to yield a saw-tooth function. Such a curve we expect from eq.(1) in the case of a linear transfer curve of the OASLM without saturation effects in a certain intensity range. However, if the arrangement works as desired, we obtain a technique for an all-optical phase (mod 2π)-to-intensity conversion. In addition, such a system is expected to react sensitively to small changes of the input intensity.

Polarization Controlled Feedback

If a birefringent film such as nematic liquid crystals is used for phase modulation, the intensity at the rear side causes a rotation of the polarization plane of the reading beam. The polarizing beam splitter (PBS) transmits only those components where the angle of polarization was rotated by the OASLM [3,4]. The setup is shown schematically in Fig. 3. The OASLM is rotated by 45° by the optical axis with respect to the plane polarization of the light that is transmitted by the PBS.

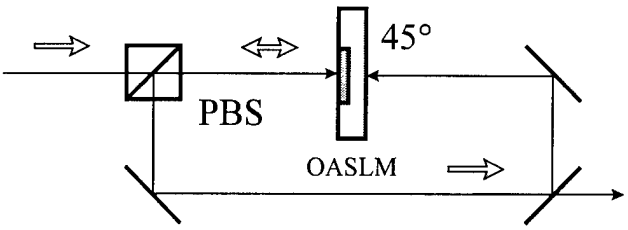

Fig. 3 Feedback controlled by a polarizing beam splitter (PBS). The OASLM is rotated by 45° with respect to the optical axis

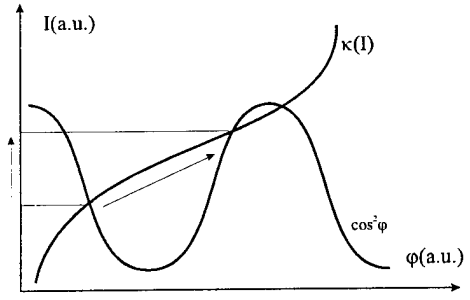

Fig. 4 Graphic solution of eq(2). The points of intersection correspond to solutions of the equation. For an appropriate $\kappa(I)$ an bistable or multistable behavior is obtained

The Jones formalism delivers the intensity after the PBS as

$$I = I_0 \cos^2\left(\varphi_0 + \kappa(I)\right) \qquad (2)$$

with a constant phase term φ_0 given by the AC voltage at the OASLM and the optically induced phase change $\kappa(I)$ that was measured in a preliminary experiment. The behavior of such a system can be easily understood with the help of a graphic solution [2] of these equations (Fig. 4).

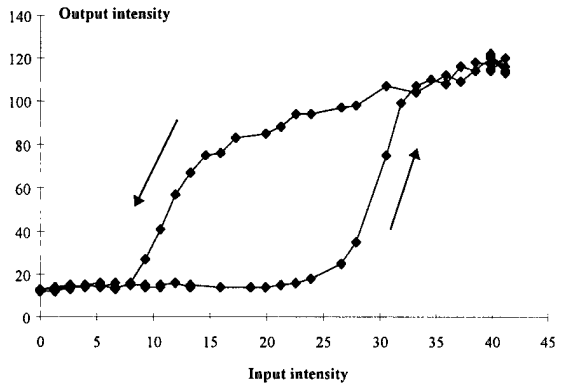

Fig. 5 Hysteresis obtained for a varying incident intensity

If the intensity that falls onto the system and reads out the OASLM is varied and the intensity within the loop is measured, a hysteresis is obtained. So, introducing an external intensity distribution to the rear side of the OASLM, the system can switch to a different state. So this distribution can be stored in the feedback system. Since the system has to decide whether an intensity value is large enough to cause a switch or not, a (multiple) threshold operation is carried out to the external intensity distribution.

Novelty Filter Feedback

In [5] we reported observations of transverse optical structures observed in a resonator as shown in Fig. 6 where a photorefractive novelty filter [6] is used to control the feedback to the OASLM.

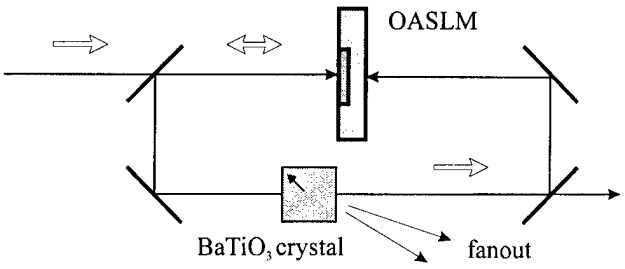

Fig. 6 Feedback controlled by a photorefractive novelty filter

Besides this effect, that such an arrangement is able to store an external intensity distribution (Fig. 7) for a time period given by the response time of the photorefractive barium titanate crystal. The external intensity was imaged to the rear side of the OASLM for only 0.8ms.

Fig. 7 Optical storage of an incoherent intensity distribution

A graphic solution (Fig. 8) is obtained in the same way such as in Fig. 4 with a phase transfer characteristics obtained in [7] that is valid for a time range much shorter than the photorefractive response time. Again the points of intersection of the two curves show the solutions of the system and how an external intensity can switch the intensity within the resonator to a higher value.

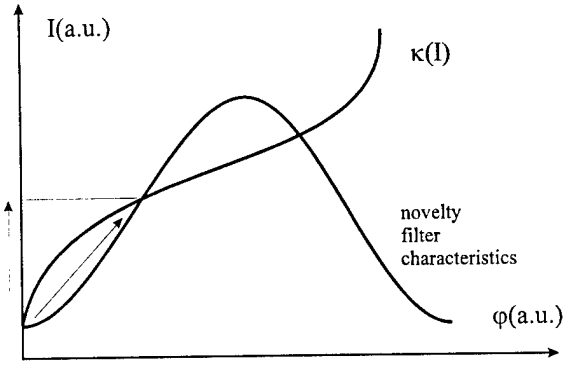

Fig. 8 Graphic solution for the setup of Fig. 6.
(novelty filter phase transfer characteristics [7])

Finally the system can be considered as a technique for the temporary magnification of transient phase changes of the input beam. Since for such phase changes the novelty filter characteristics is shift slightly to the left (Fig. 8), the obtained points of intersection show that the phase of the beam that leaves the OASLM is enhanced with respect to the input phase value.

Conclusions

Closed loop systems with an OASLM and a feedback controlling element can exhibit a nonlinear behavior for cw light in the $mWcm^{-2}$ range. It was demonstrated that such optical arrangements can serve as a linear phase-to-intensity converter, for optical image processing such as for thresholding, and for optical storage not in a sensitive medium but in a bistable optical arrangement.
Though the described effects were demonstrated with a nematic liquid crystal OASLM, in most cases any other type of OASLM with a sufficient phase shift can be used. Only for the experiments with the polarization controlled feedback an OASLM is needed where the writing beam changes the birefringence and, this way, the polarization of the reading beam.

Acknowledgment

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On the Storage Capacity of Electrically Addressable SLMs in Coherent Optical Information Processing Systems

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Abstract

The development of electrically addressable spatial light modulators (EASLMs) is leading to the implementation of new opto-electronic information processing devices, where the optical function can be switched. Applications such as optical image processing, free-space communications or holographic pattern generation have been described in literature. The amount of information which can be processed in coherent optical systems depends on the storage properties of modulators. However, only few publications deal with this topic [1,2,3].

In this paper, the storage properties of an EASLM in a coherent optical system and the transmission of information in this system are expressed in terms of information theory. It is demonstrated that the restriction of an EASLM to fixed modulation schemes may seriously disable an error-free processing of information due to strong noise effects. These noise effects are described by measures of information theory. We focus on coding methods of diffractive optics to reduce the noise energy in optical signal waves which carry information. The correspondence of these methods to channel coding methods known from communication theory is stressed. Finally, the storage capacity of an EASLM is analysed in a numerical simulation experiment.

Key Words

Spatial light modulators, diffractive optics, optical information processing, information theory.

EASLMs in Diffractive Optics

EASLMs are characterized by a pixelated microstructure, where the optical properties of each pixel can be electrically controlled. The lateral pixel size of currently available EASLMs ranges from 20 to 100 microns, and thus it is much larger than the wavelength of visible light. If an EASLM is illuminated with coherent light, due to the micropixel structure, it behaves as diffractive optical element. In this case, the optical function of the EASLM is basically specified by the pixelated transmission function which corresponds to a certain diffracted wave.

The effect of an EASLM on a coherent illumination wave can be expressed in terms of diffraction theory. It is helpful to simplify this formalism by restriction to scalar theory [4]. In the case of EASLMs, this is allowed for two reasons. First, the pixel structures of an EASLM are large compared to the wavelength of the used illumination. Secondly, EASLMs behave as thin optical media. Hence, and due to the pixel structure, the transmission function of an EASLM can be described by

$$G(x_0, x_1) = \mathrm{rect}_{\Delta x}(x_0, x_1) * T(x_0, x_1) \qquad (1)$$

denoting the convolution of the discrete transmission function

$$T(x_0, x_1) = \sum_{k,l=0}^{N-1} T(k\Delta x, l\Delta x)\, \delta(x_0 - k\Delta x, x_1 - l\Delta x) \qquad (2)$$

with a rectagular pixel function $\mathrm{rect}(x_0, x_1)$ of lateral size Δx in both directions. δ denotes the Dirac function. The values of T are complex and restricted to a certain modulation domain which depends on the technical properties of an EASLM. Figure 1 depicts the modulation of an illumination wave S by an EASLM and the subsequent wave propagation in a schematic view. Using the argument that an EASLM is a thin optical element, the modulated wave U can be expressed

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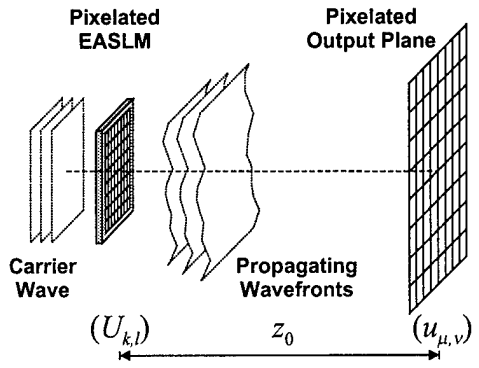

Figure 1. A pixelated EASLM with the discrete transmission function $(U_{k,l})$ generates a diffracted wave which is specified by vector components $u_{\mu,\nu}$ on a sampling grid.

simply by the product

$$U(x_0, x_1) = S(x_0, x_1)\, T(x_0, x_1)\,. \qquad (3)$$

This wave propagates in free space and forms a diffracted wave u which can be optically processed or detected by a sensor. In order to determine the shape of a diffracted wave in a specified plane the diffraction integral has to be solved. However, since the pixel structures of an EASLM are large compared to the wavelength, the maximum diffraction angle is quite small. Consequently, the diffracted wave is well expressed by the Fresnel integral in a near field or by the Fraunhofer integral in a far field region.

According to figure 1, the diffracted wave is completely specified on a sampling grid as well as the transmission function of the modulator. Thus, instead of integral equations, the corresponding summation equations can be used to determine the complex amplitude of the diffracted wave on the grid points. If the modulated wave right behind the EASLM is defined by the twodimensional complex vector $\mathbf{U} = (U_{k,l})$, $k, l = 0, \ldots, N-1$, the corresponding diffracted wave in a distance z_0 is completely specified by the Fresnel transform vector $\mathbf{u} = \mathrm{FrT}[\mathbf{U}]$ with

$$u_{\mu,\nu} = \sum_{k,l=0}^{N-1} U_{k,l} e^{i\frac{2\pi}{\lambda z_0}|\Delta\tilde{x}(\mu,\nu) - \Delta x(k,l)|^2}\,, \qquad (4)$$

$\mu, \nu = 0, \ldots, N-1$. Δx and $\Delta\tilde{x}$ denote the sampling spacings in the plane of the EASLM and the output plane in a distance z_0, respectively. The vectors (k, l) and (μ, ν) run through all sampling points in the corresponding planes. If the sampling condition

$$\Delta\tilde{x}\,\Delta x = \frac{\lambda z_0}{N} \qquad (5)$$

is considered, the Fresnel transform according to (4) is an invertable linear operator [5]. Complex amplitudes between the sample points $u_{\mu,\nu}$ result from interpolation effects which will not be discussed here.

In analogy to the above examinations, the diffracted wave in the far field is described by the Fourier transform vector $\mathbf{u} = \mathrm{FT}[\mathbf{U}]$ with

$$u_{\mu,\nu} = \sum_{k,l=0}^{N-1} U_{k,l}\, e^{-i\frac{2\pi}{\lambda f}\frac{k\mu - l\nu}{N}}\,. \qquad (6)$$

f denotes the focal length of a Fourier transform lens that is usually applied to generate far field diffracted waves. In the Fourier case, the sampling condition (5) is fulfilled with $z_0 = f$.

In coherent information processing, optical functions are implemented via diffracted waves. A diffractive element is used to generate a certain diffracted wave and so to perform a desired function. EASLMs give the opportunity to implement computer-generated transmission functions of diffractive elements by direct adressing of the modulator pixels. Different functions can be achieved by addressing the pixels with different information defining the transmission function or correspondingly the diffracted wave.

EASLM as Planar Storage Medium

A computer-generated transmission function is digitally represented by a two-dimensional vector data structure and stored in a computer memory. The information of the vector components specifies amplitude or phase values which can be dynamically mapped onto the pixel matrix of an EASLM. This mapping can be interpreted as computer memory access, where a section of the computer memory is copied to the EASLM. To account for this, the EASLM is a storage medium which is characterized by an electrical write-in and an optical read-out mechanism. The read-out is performed in parallel by illuminating the EASLM with an optical carrier wave. This process is usually denoted as modulation of the carrier wave. A modulated wave carries the information of a computer-generated transmission function and can be used to implement an optical function. The capability of an EASLM to implement different optical functions strongly depends on its storage capacity.

The storage capacity C of an EASLM determines the maximum number of bits which can be correctly read out per time interval. Considering an EASLM as thin optical element, according to equation (3), a modulated wave right behind the EASLM carries the information introduced by the EASLM pixels. Thus if an EASLM is characterized by an array of N^2 pixels and a modulation alphabet D containing $|D|$ modulation values, the capacity is given by

$$C = N^2 \log_2 |D| \quad \text{bits} \qquad (7)$$

per pixel frame. This value determines an upper limit without consideration of any noise effects. However, such effects may occur during the free-space transmission of the information-carrying signal wave or due to technical inadequacies of the EASLM [6,5].

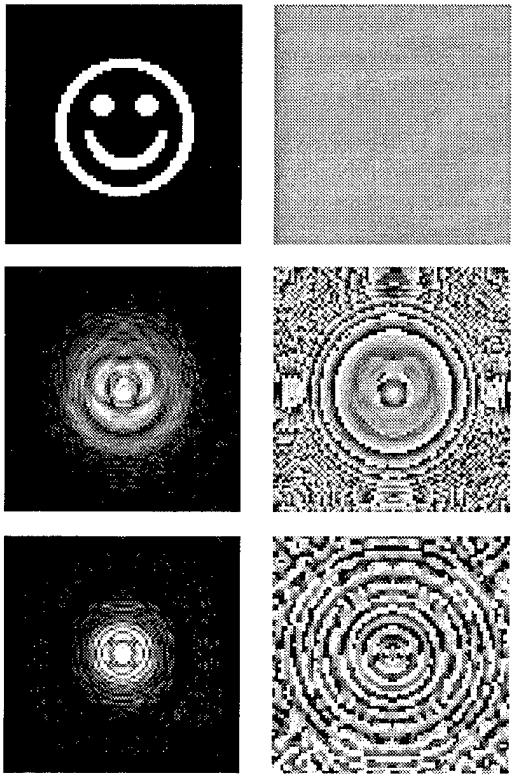

Figure 2. Equivalent representations of an information vector with its amplitude to the left and its phase to the right. The binary vector in (top) is invertably transformed into complex-valued vectors applying a Fresnel operator (middle) and a Fourier operator (bottom).

Free-space Transmission of Information

EASLMs are used to modulate in parallel digital information, coded as amplitude or phase values, onto a carrier wave. Right behind the EASLM a digital information vector $\mathbf{U}$ is represented by discrete modulation values located on a sampling grid. The information propagates with its carrier wave through free space and changes its representation continuously with the distance covered due to wave-physical effects. As already motivated before, the propagation of the modulated wave U is adequately described by the Fresnel integral. In correspondence with this integral the discrete Fresnel operator (4) determines the complex amplitudes of the propagated wave u on a sampling grid of a plane in a distance z_0. If the sampling condition (5) is fulfilled, the discrete Fresnel operator is invertable. In this case, the sample vector $\mathbf{U}$ of the modulated wave U is invertably transformed into a vector $\mathbf{u}$. Consequently, both vectors $\mathbf{U}$ and $\mathbf{u}$ represent the same information. The complex amplitudes between the sample values $u_{\mu,\nu}$ of a propagated wave u do not give any additional information since they also result from a linear combination of the values $U_{k,l}$. We draw the fundamental

conlusion: The information of a modulated carrier wave is preserved by the wave propagation process and can be identified on a sampling grid which is specified by the sampling condition (5).

Figure 2 demonstrates an example of three equivalent representations of the same information vector that differs only due to the application of discrete wave propagation operators. In the upper row the information vector $\mathbf{U}$ is specified by an array of 55×55 samples with binary amplitudes (left) and constant phase (right). The illustrative example shows a binary smiley the information of which amounts to 3025 bits. This information can be used to address an EASLM and so to modulate a carrier wave. The effect of wave propagation can be numerically simulated on the basis of equations (4) and (6). In our example, we assumed a pixel size of $\Delta x = 30\mu$m in the EASLM plane, the wavelength $\lambda = 633$nm, and condition (5). The information vector $\mathbf{u}$ of the propagated wave u in the near field distance $z_0 = 200$mm in shown in the middle row. Another representation of the information depicted in the bottom row appears in the far field.

Compared to the original information vector $\mathbf{U}$ the propagated vectors $\mathbf{u}$ look very complicated since each vector component is not any longer a binary value but a complex value of a continuous domain. The impression that a complex vector $\mathbf{u}$ might carry more information than the original vector $\mathbf{U}$ is deceptive. Using the inverse propagation operator $\mathbf{U}$ can be directly reduced to $\mathbf{u}$ confirming that the information vectors, as in figure 2, are equivalent and carry the same amount of information.

Information Processing and Detection

In coherent optical systems, information processing or detection is performed via diffracted signal waves in a specified plane which we call the output plane. It is essential that the diffracted wave has a certain shape in order to perform a desired optical function or to show an information vector such as the smiley in figure 2. Hence, it is sensible to define the information vector of a coherent optical signal in the output plane. From a specified information vector, generated by a diffracted wave, the corresponding transmission function of the

EASLM is derived by an inverse wave propagation operator. This point of view implies a different meaning of the storage capacity of the EASLM. We redefine the storage capacity by the maximum number of bits which are correctly received in the output plane per time interval. If no noise effects occur, its value is given by

$$C = N^2 \log_2 |S| \quad \text{bits}\,, \tag{8}$$

where S represents the finite alphabet of information symbols. Note, that in general $D \neq S$.

Noise Effects of EASLMs

In most cases, the transmission function, derived from a discrete information vector by an inverse propagation operator, is complex-valued. This can be directly confirmed by the example in figure 2, where a binary information vector is transformed into equivalent complex vectors. The resulting problem is that there is no EASLM available which is capable to implement arbitrary complex transmission functions [7]. Depending on its techical properties an EASLM is restricted to a certain modulation domain

$$D \subset \mathbb{C}_{\leq 1} = \{x \in \mathbb{C} : |x| \leq 1\}\,. \tag{9}$$

The implementation of a complex vector $\mathbf{U}$ by an EASLM which is restricted to a modulation domain D can be mathematically modeled by the projected vector

$$\bar{\mathbf{U}} = \mathrm{P}_D[\mathbf{U}] = \mathbf{U} + \mathbf{N}\,, \tag{10}$$

where the projection operator P_D is characterized by the norming condition

$$\bar{\mathbf{U}} \in D^{N\times N} \wedge \|\bar{\mathbf{U}} - \mathbf{U}\|_2 = \min\,. \tag{11}$$

P_D minimizes the additive projection noise $\mathbf{N}$ but in general the occurance of noise cannot be avoided. Due to its restricted modulation characteristics, an EASLM itself can be a "noise source" leading to a noisy information vector

$$\mathrm{FT}[\bar{\mathbf{U}}] = \mathbf{u} + \mathbf{n} \tag{12}$$

in the output plane. Noise effects in an optical system go together with a loss of information or equivalently with a decrease of storage capacity.

Projection noise may have serious consequences on the quality of an information vector of a diffracted wave. This is demonstrated by the example in figure 3, where the complex transmission function of the binary signal in figure 2 has been computed by an inverse Fourier operator and projected onto its phase. Such a phase-only transmission function, shown to the left, can be well implemented by an EASLM. However, the image

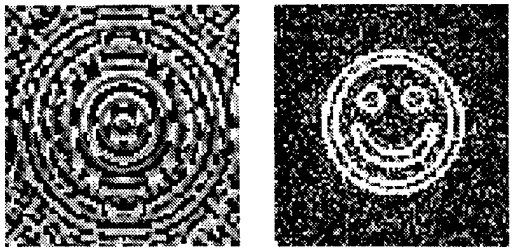

Figure 3. The projection of a complex transmission function onto its phase (left) leads to strong projection noise in the information vector of the diffracted wave (right).

of the binary signal in the far field is strongly distorted by additive noise as depicted to the right. Obviously, there are pixels the gray value of which has changed from bright to dark and vice versa.

Theory of Noisy Information Transmission

The additive noise which is introduced by the projection P_D can be numerically determined if the information vector, the propagation operator, and the modulation domain D are specified. However, it has to be emphasized that the noise vector $\mathbf{n}$ differs with each information vector $\mathbf{u}$. As a consequence, a general examination of the storage capacity of an EASLM can only lead to an average limit. We apply methods of information theory [8,9,5] to express the loss of information due to noise effects and so to derive the storage capacity.

From an information-theoretical point of view, an EASLM is an information source which generates information vectors $\mathbf{u}$ in the output plane of an optical system. Each vector component is an element of a finite signal alphabet $S = \{s_0, \ldots, s_{q-1}\}$, where each signal s_j, $j = 0, \ldots, q-1$, is assumed to occur statistically independently with a certain probability $p(s_j)$ and $\sum_j p(s_j) = 1$ holds. So, the EASLM is characterized by its source entropy

$$K(S) = -N^2 \sum_{j=0}^{|S|-1} p(s_j) \log_2 p(s_j) \tag{13}$$

determining the average information of an information vector.

The influence of the noise effects, due the restricted modulation characteristic of an EASLM, can be interpreted as the uncertainty about the correctness of a detected information vector. This quantity is expressed by the equivocal entropy

$$K(S|\bar{S}) = N^2\, E\left[\log_2 \frac{1}{p(s_i|\bar{s}_j)}\right]\,. \tag{14}$$

The argument of the expectation E determines the information of the event that a symbol s_i is the original information signal but $\bar{s}_j$ is detected due to noise. For the sake of simplicity it can be assumed that the alphabet $\bar{S}$ of the detected signals is equal to S.

The difference between source and equivocal entropy, the mutual information

$$I(S,\bar{S}) = K(S) - K(S|\bar{S})\,, \qquad (15)$$

is the amount of correctly transmitted information which can be evaluated in the detection plane. The maximum mutual information

$$C = \max I(S,\bar{S}) \qquad (16)$$

is known as channel capacity. In the context of this paper, C gives an upper bound of the storage capacity of an EASLM. Evidently, a statement about a representative value of $I(S,\bar{S})$ has to be achieved by consideration of sufficiently many information vectors.

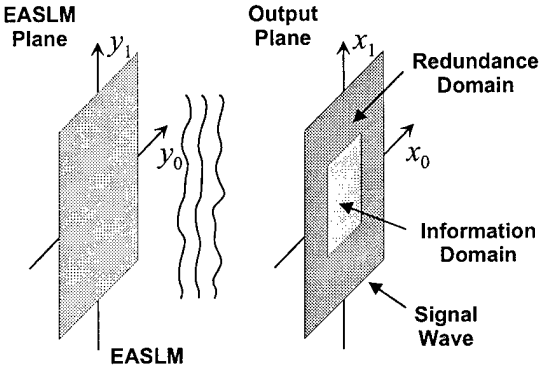

Figure 4. Concept of a redundant optical signal wave. The signal wave, located in the output plane, consists of separated information and redundance domains. In contrast, information and redundance are mixed in the transmission function in the EASLM plane.

Redundant Coding of Information

A basic aim of coding theory [9] is to develop methods to optimize the mutual information in communication systems. Efficient coding schemes are already used for the detection or correction of bit errors occuring due to noise on the transmission channel. These coding schemes are based on the introduction of redundant symbols which are used to control the correctness of information symbols. Interestingly, the basic idea of redundant coding can also be used to diminish the projection noise of an EASLM.

Different coding methods from diffractive optics are known, where parameters of freedom are introduced in order to adapt the discrete transmission vector **U** to a specified modulation domain D [10,12,11,13]. The parameters of freedom are redundant signal values comparable to the control symbols of an error correcting code. In figure 4, the concept of a redundant optical signal wave is depicted. The signal wave, representing a diffracted wave in the output plane, is partitioned in an information and a redundance domain. The aim of a coding procedure is to define the redundance with respect to the information in a smart way so that the resulting coded signal wave corresponds to a transmission function which fulfills the modulation restriction of the EASLM in good approximation. As a result, additive projection noise is reduced. In summary, this basic effect of a redundant coding scheme is sketched in figure 5. It should be mentioned that in some applications only the amplitude of the signal wave is used to carry information. In this case, also the phase parameters represent redundance which can be used to code the signal wave.

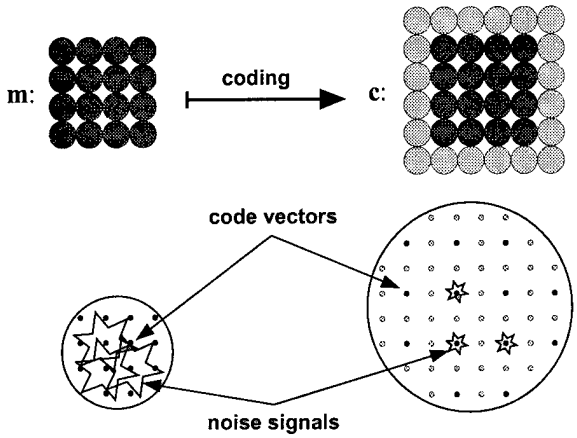

Figure 5. Block-encoding scheme for optical signals. The encoded signals are characterized by low additive projection noise.

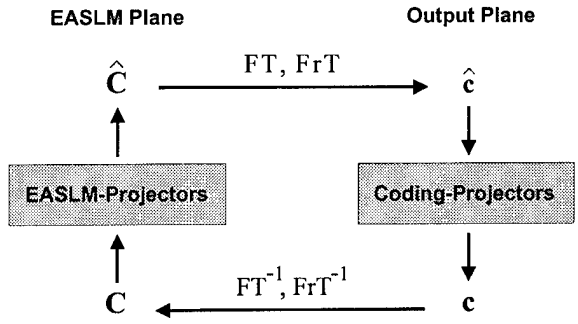

Figure 6. Concept of an iterative coding method.

The most efficient and widely used coding methods in diffractive optics are based on iterative opti-

mization strategies [11,10,13]. The principle of these coding methods is represented by the flow diagram in figure 6. Following the directions of the arrows, the iteration moves back and forth between the representation domains of the coded signal wave c and the corresponding transmission function C. In both domains projection operations are performed on the one hand to adapt C to the modulation restrictions of the EASLM and on the other hand to diminish the noise effects in the information block of the signal wave. The redundant parameters are developed during the iteration so that a merit function such as the mutual information in (15) is optimized. This aim can be achieved by a minimization of the energy of the projection noise.

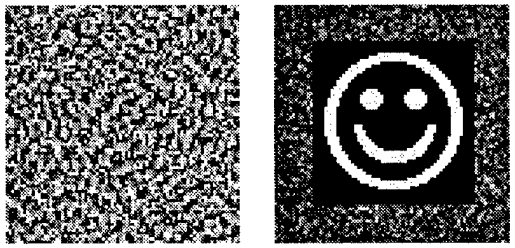

Figure 7. Result of an iterative coding procedure. The obtained transmission function (left) for a phase-only EASLM generates the desired information vetor (right) in the far field.

Figure 7 demonstrates the effectiveness of an iterative coding method as it is described in [13]. In this example, the binary signal, shown in figure 2, has been coded to be generated in the far field by a phase-only EASLM. According to figure 5, the block of 55×55 binary information samples has been embedded in a larger block of 80×80 samples. Thus 3375 redundant symbols have been available to optimize the merit function. Comparing the results of figure 3 and figure 7, it becomes obvious that coding methods from diffractive optics optimize the mutual information in the output plane and with it the storage capacity of an EASLM.

Storage Capacity of EASLM – An Example

The storage capacity of an EASLM in a coherent optical system is limited by the maximum mutual information. This quantity is difficult to determine since the coding results may differ for different information vectors. However, empirical examinations show that if information vectors consist of equally distributed signal components and, to account for this, have the same energy, the coding results are very similar with respect to projection noise. From information theory it is known that Huffman's coding method [8,9] can be used to code digital information to obtain the desired statistical distribution of signal components. If information vectors are coded by applying Huffman's method the iterative coding methods of diffractive optics show very similar results with respect to the noise energy as merit function. In this case, a general statement on the storage capacity can be derived by numerical simulations.

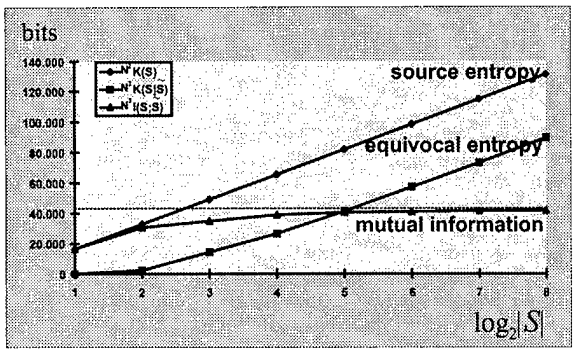

Figure 8. Progress of source entropy, equivocal entropy, and mutual information for $N = 128$ and increasing alphabet size $|S|$.

The aim of a simple simulation experiment was to derive the capacity of an EASLM with 128×128 pixels and a phase-only modulation domain

$$D = \{x \in \mathbb{C} : |x| = 1\}\,. \tag{17}$$

According to figure 1, the EASLM is capable of generating diffraction waves which are specified on a samling grid with 128×128 sample values. Thus the information vector of the signal wave has at maximum 128×128 components. In the simulation experiment, such information vectors with equally distributed and quantized amplitude signal components have been generated. An iterative coding scheme according to [13] has been used to code the information vectors in 100 iteration cycles, where free phase parameters served as redundance [6,5]. For each coded vector, the mutual information $I(S, \bar{S})$ have been computed according to equation (15), where $S = \bar{S}$ had been assumd. By taking many information vectors into account, the value of the mutual information $I(S, \bar{S})$ converged quickly to a limit. In order to find the capacity of the EASLM, $I(S, \bar{S})$ has been computed for an increasing number $|S|$ of equally quantized amplitude signals.

The results of the simulation experiment are summarized by the diagram in figure 8 showing the progress of source entropy, equivocal entropy, and mutual information for an increasing alphabet size $|S|$. The source entropy which is linearly growing with the logarithm of $|S|$ represents the absolute upper limit of the storage capacity stated by equation (8). An increasing alphabet size corresponds with with a finer quantization of signal

amplitudes. However, the finer a quantization is performed the more signal errors occur due to noise effects. This phenomenon is expressed by the progress of equivocal entropy in figure 8. Asymptotically, the equivocal entropy behaves like the source entropy. In account to this, the mutual information converges against an upper limit which is identified as storage capacity of the EASLM considering projection noise. It should be kept in mind that the values of the information measures depend on the coding procedure and the number of its iteration cycles.

Conclusion

The application of EASLMs in coherent optical systems for information processing purposes is becoming very attractive due to remarkable advances in EASLM technology. The performance of such systems is characterized by the amount of information that can be stored, transmitted, or processed per time interval. so theoretical methods to measure information introduced by an EASLM are helpful to characterize and optimize the system performance.

In this paper, we focused on the storage properties of EASLMs in coherent optical systems. Considering paraxial diffraction theory, it has been explained that information modulated onto a carrier wave by an EASLM is preserved by the wave propagation and can be identified on a sampling grid. The storage capacity of an EASLM has been defined as the maximum number of bits which can be correctly evaluated from a diffracted wave in the output plane of a system. Information which is specified in a domain of the diffracted wave usually corresponds to a complex transmission function to be implemented by an EASLM. However, currently available EASLMs are restricted to a limited set of modulation values. As a consequence, strong noise effects may occur and reduce the storage capacity of an EASLM. The loss of capacity has been stressed in terms of information theory. Additionally, it has been demonstrated that redundant coding methods from diffraction theory can be used to diminish these noise effects and improve the storage capacity.

Finally, in a simple example, the storage capacity of a specified coherent system with one EASLM has been examined assuming a certain coding scheme. The presented results are strongly related to the discussed example and its boundary conditions. However, it is possible to adapt the proposed analysis methods to other system parametrizations.

Acknowledgments

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Smart pixels for optical wireless applications

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Abstract

Most smart pixel systems use optical channels that are highly directed; Care is taken to use efficient optical paths that transfer as much energy as possible from source to detector. In this paper we describe the use of highly inefficient 'loosely directed' optical channels in wireless local area networks, and how smart pixel integration techniques can be applied to such systems. An overview of the system and its operation is presented. Techniques for meeting eyesafety regulations at the transmitter are discussed, as well as receiver design issues.

Keywords

Optical communications
Optoelectronics
Vertical cavity surface emitting lasers
Diffractive optics

Introduction

There is a growing interest in providing wireless data networking within buildings, to allow flexible, low cost networks that can be quickly installed and reconfigured. Static data cabling is expensive to install, and older buildings do not contain the necessary duct networks, so the possibility of wireless networks is extremely attractive. RF wireless LANs products are the main commercial interest in this area. There are, however problems with these radio LANs: The spectrum is highly regulated so the data rates are limited by this regulation. The cards have high power dissipation, and components are relatively expensive.

Free space optical links have many advantages over radio channels. The optical spectrum is subject only to eye safety regulation, and the bandwidth of the optical channel means data rates into the Gbit/s range are possible. Components are relatively inexpensive, and have low power consumption [1-6]. 'Point and shoot' optical links that conform to the Infra Red Data Association (IRDA) are routinely fitted to laptop computers and increasingly integrated with printers and other peripherals. These ports offer data transfer at up to 4Mb/s. At higher data rates there has been academic interest and several products operating at ethernet data rates [1-6].

Optical channels can generally be classified as diffuse, or line of sight (LOS). Diffuse links diffuse Lambertian emitters that fill the coverage volume with optical power. This creates robust channels that cannot be blocked by an obstacle between source and detector; In this situation an alternative path exists (perhaps due to a reflection off a wall). The problem with this approach is that each of the multipaths has a different propagation distance, creating a dispersive optical channel. An estimate of the unequalised bandwidth-distance product of a typical channel is given in [4] as 260 Mb.m/s . Diffuse systems operating at 50 and a possible extension to 100 Mb/s have been reported [6,7], and these use equalisation to overcome the dispersive channel.

Fast optical channels must therefore be line-of-sight, if this complex equalisation is to be avoided. The coverage of a single channel is a function of the power flux density that can be provided at the receiver by the source, so that a compromise between a single source above the room providing flood illumination, and a large number of low power line of sight channels must be found.

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Systems that use relatively high power transmitters and large cells have been demonstrated at 155Mb/s [8], and a 1Gbit/s tracked architecture has been shown to be feasible [9,10]. This latter architecture used tracking of a mobile and a solid state beam-steering antenna to cover the space. The system we envisage builds on this, but removes the acquisition time involved in a tracking process.

In this paper we describe a cellular optical network that uses vertical cavity surface emitting lasers to provide high bandwidth optical links to terminals in a room, using a number of small cells of coverage. This architecture uses transceivers, and incorporates control functions that are well suited to a smart pixel integration technology.

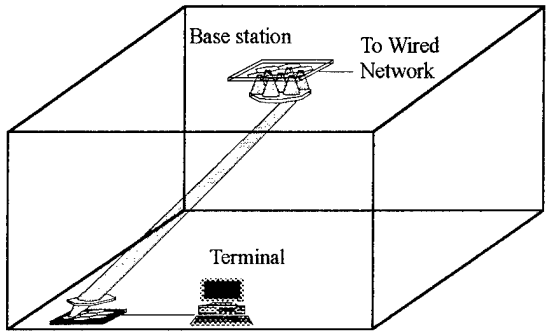


Figure 1. *Free space optical network*

Overview

Figure 1 shows a diagram of the proposed architecture. A Base Station (BS) is located above the coverage area, and this contains an optical transmitter and receiver. The transmitter uses an array of semiconductor sources which emit normal to the surface of the array. These are likely to be either Vertical Cavity Surface Emitting Lasers (VCSELs) or resonant cavity LED's (RCLEDs). Each source emits light which passes through a short focal length lens that deviates the beam according to how far the source is displaced from the optical axis of the system. This position-angle mapping allows the space to be covered by an array of cells, each illuminated by a single source.

The Terminal or Mobile Station (MS) is identical to the base station. The receiver section that is shown in the diagram uses a system of lenses to focus light onto one element of a photodetector array, creating a angle-sensing detector array. The photodiode detects the radiation, and transmitted data is recovered from this. The position of the active detector indicates the angle of the incoming beam. Segmenting the detector into an array also narrows the capture angle of the receiver (by keeping only one element active) thus reducing the noise from background illumination.

The cells are designed to be on a hexagonal pitch, and a hexagonal pitch source array will be used. The optical systems perform a position-angle mapping in the transmit antenna and the inverse at the receiver, which implies the topology of transmitter and receiver array should be the same.

The systems we envisage will operate at data rates of 155Mbits to up to 1Gbit/s. Calculations have shown that realistic receiver designs require approximately -30dBm of incident optical power to support data rates of this order. In the next section we analyse the transmitter and receiver components in more detail and discuss methods of meeting this demand.

System components

Transmitter

The receiver plane power flux density should be approximately -30dBm/cm^2 for operation at >150Mbits/s. This corresponds to a 6.4mW point source evenly illuminating each 1m diameter hexagonal cell. This is a major barrier to using these free space optical channels, as this is an order of magnitude larger than Class 1 eye safety Accessible Emission Limits (AELs) at typical wavelengths. Table 1 summarises the eyesafety limits at a number of wavelengths.

Wavelength	Point source Accessible Emission Limit (AEL) (Note 1)	Diffuse source Emission limit (Note 2)
λ=850nm	0.24mW	2.2mW
λ=980nm	0.43mW	3.9mW
λ=1300nm	0.48mW	4.4mW
λ=1500nm	10mW	10mW
1.AEL is equal to power passing through a 50mm aperture 100mm from the optical antenna. In most cases AEL=Emitted power.		
2.AEL is equal to power passing through a 50mm aperture 100mm from the antenna. Collection system has an NA=0.1 (this condition often increases the allowed *emitted* power substantially. i.e. by a factor $(0.5/0.1)^2$ for a source beam angle of 0.5)		

Table 1. *AELs for laser sources*

Several methods for meeting the Class 1 limits have been identified. Above 1400nm eyesafe operation is almost assured, as the water in the cornea of the eye absorbs radiation and prevents focusing on the retina. The system requires surface normal emitters at these wavelengths, but VCSELs operating at these long wavelength are not available. Resonant cavity LEDs (RCLEDs) [11] have the potential to operate at this wavelength, due to their simpler structure, and devices have been demonstrated at 980 and 1300nm. Work on 1500nm designs is progressing. RCLEDs are expected to show efficiencies of around 5% and modulation bandwidths of 100's of MHz, and appear to be an attractive source for long wavelength, low cost systems.

The optical 'antenna' consists of an array of surface normal emitters combined with beamsteering optics, as shown in figure 2 . This uses an array of point sources on a hexagonal array of pitch 250 μm, with a beam angle typical of a RCLED (NA=0.1) in combination with commercially available singlets that form a short focal length combination. A combination of custom and commercial software is used to model the propagation of light from the emitters, which are assumed Gaussian, to the receiver plane. Figure 3 shows a typical result for a BS 2m above the receiver plane using 19 0dBm sources. The -42dBm contour would be the limit of the operating region, and the plot shows that there is a 6dB variation in power flux density with all transmitters on. This could be reduced by varying the power that each device transmits, which is to be avoided due to added circuit complexity, or using modified optics or an irregular pitch array. Work on the development of RCLEDs at eyesafe wavelengths (>1400nm) is continuing, and we consider operation at these longer wavelengths to be the most desirable option, due to the ease in meeting safety considerations.

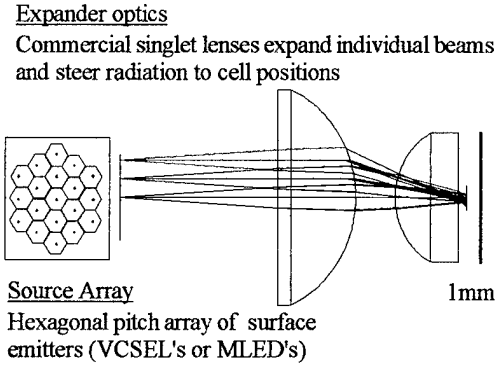


Figure 2. *Transmit antenna*

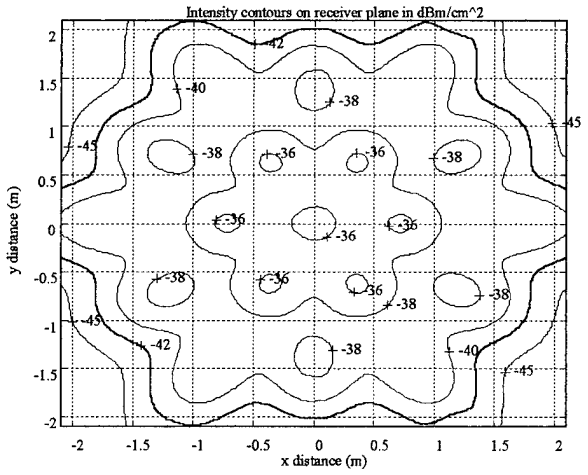


Figure 3. *Intensity contours in receiver plane. Diagram shows contours for a hexagonal array (250mm pitch) of 19 1mW Gaussian beam profile sources 2m above receiver plane. Intensity is calculated over area normal to local ray direction (i.e. facing transmitter array).*

At wavelengths below 1400nm meeting the eye safety limits becomes more difficult, and the effective radiance of sources needs to be reduced by a factor of about 25 to meet eye safety limits. The use of a Holographic Optical Element (HOE) as a shaped diffuser was demonstrated by a group at BT labs who demonstrated a diffuse system over a 2x2 m cell with a single laser diode source [5]. The HOE diffracts the incoming radiation into the required far field pattern, so that at each point on the element light is scattered into a range of angles. The effective source is the illuminated area on the diffuser, as the eye cannot focus back to the actual source. Figure 3 shows a diffuser design that would meet this requirement. An array of diffusers can be introduced approximately 15mm from the front of the antenna described earlier. The refractive optics performs most of the routing functions and the diffuser array shapes the cell illumination. This approach puts heavy demands on the holographic design and fabrication of the diffractive element. The emitted power sets the area of diffuser required to achieve Class 1 eyesafe operation, and an area of approximately 5x5mm is required to emit 25 times the AEL. These diffusers require wavelength order feature size, and therefore even single diffusers are high space bandwidth product elements.

The etch depth of the holographic element must be carefully controlled, as the zero order undiffracted beam is subject to the point source (rather than diffuse) AELs. In the diffuser array the beams enter

the hologram at varying angles, which means that the etch depth must vary across the array.
Work on holographic diffusers is being pursued in collaboration with the Chalmers University of technology.

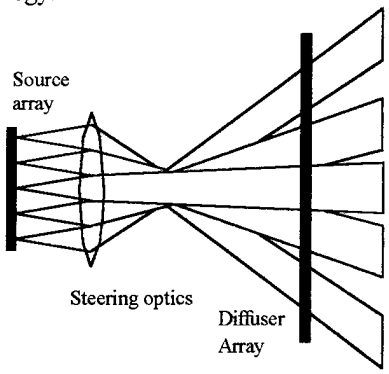
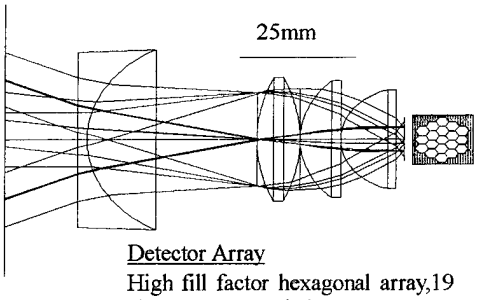


Figure 4. *Modified eyesafe antenna for operation below 1400nm.*

Receiver Optics
Receives beam and focuses onto hexagonal detector array. Design uses commercially available singlets.



Detector Array
High fill factor hexagonal array,19 elements, 2mm pitch.

Figure 5. *Receiver optics*

Receiver

The receive antenna and associated circuitry offer significant challenges in terms of optical and electrical design, and integration of the components into a compact structure.

Figure 5 shows an initial optical design for the receiver. Light from the base station enters the optics as a parallel beam of light at an angle dependent on the position of the terminal within the coverage area. The light is focused on one element of a hexagonal pitch array, which is paired with an equivalent uplink transmitter. This ensures that the uplink will automatically return at the correct azimuth and elevation.

The use of a detector array with the optical system allows a wide collection area to be combined with a small angular field of view, as only one detector is active at once, restricting the range of the input angles. The receiver optical system must meet several conflicting requirements: It must have a large collection area, over a wide range of input beam angles, and must focus this radiation to as small an output spot as possible. The optical design shown uses commercially available AR coated singlet lenses, and is designed to focus at least $1cm^2$ of power flux density onto the appropriate detector at the receiver plane at angles up to 40 degrees either side of the optical axis Work on an optimised design using aspheric plastic optical element is underway, and it is expected that this will be folded to reduce the volume of the receiver.

One of the major sources of interference in free space optical channels is the interference due to background illumination. Daylight can induce DC photocurrents, and fluorescent light fittings can induce significant interference components up to 1MHz [12].

Receiver designs for these systems are AC coupled to reduce the effect of the photocurrent fro m this background noise. Optical filtering can also used to reduce the optical bandwidth of the system [3]. The other technique we are investigating is to grow semiconductor layers in the receiver photodetectors with the correct bandgap to provide a short wavelength cut-off, and use the natural detector roll off in responsivity for the high cut-off. This principle has been demonstrated at 980nm using a combination of an AR coated GaAs wafer and a Silicon detector, providing a bandwidth of 100nm or so with little angular dependence [13]. We are presently designing InGaAsP detector structures to achieve this at longer (1300 and 1500nm) wavelengths.

Smart Pixel Implementation

Figure 6 shows a block diagram of the functions the transceiver must perform, in its simplest form. Each local transceiver pair launches and receives light from the same angular cone (corresponding to a cell) and forms the basic 'smart pixel'. This contains laser driver circuitry, and some of the receiver circuitry. This is likely to be a preamplifier and main amplifier, with Automatic Gain Control. The AGC amplifier boost the signals to the input level where clock recovery and data decision circuits can be used.

As there are many pixels simultaneously receiving data the transceiver must pass the strongest received signal to the recovery circuits and discard the rest. There are several methods of combining these signals, and our initial approach will be to use the AGC control signals from the amplifiers as an indication of signal strength and to route the strongest signal to the data recovery circuit. The clock recovery and decision circuits are global functions, and would be implemented separately from the pixels, at least

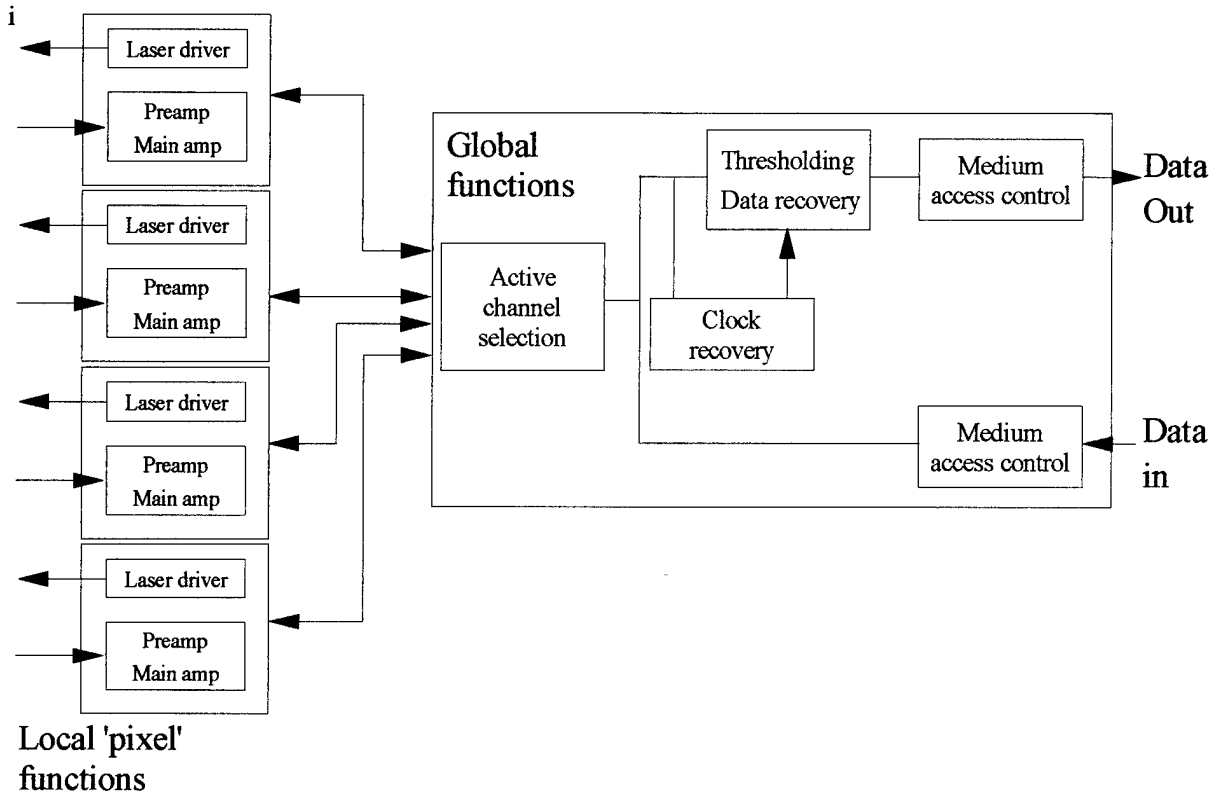


Figure 6. *Block diagram of Smart pixel implementation*

nitially. The transmission acknowledge signals, and other aspects of the medium access control would also be implemented at this level

In more sophisticated systems each pixel would be a complete transceiver unit and receive and output digital data from the terminal. The global task is then to choose the best digital (rather than analogue signal). In the BS this would be an advantage, as each pixel could function as an autonomous downlink, increasing the aggregate bandwidth of the system. In the terminal this is less advantageous as there is only one smart pixel active at any one time. At present we are investigating the sort of division between the tasks that is straightforward to implement and makes efficient use of the components. The restricted user model that we are considering means that simple transceiver pixels with global (i.e.) a single data and clock recovery circuit is most likely.

The intention is to use a custom integrated circuit to implement the electronics, and to flip-chip bond receiver and transmitter devices to this. Optical components would then be integrated with these components. Our aim is to use a hybrid of diffractive and refractive components to create a compact transceiver that is suitable for manufacture.

System operation

User model

At present the model of the type of use of the network has been restricted, although the antenna designs allow for a great deal of flexibility. The model we have used is that of a wired ethernet type system, with static terminals within the space, that can be repositioned. There is no allowance made for portable terminals that can roam within the network, as this requires handover between illumination cells, although we believe this could be implemented at a later date. Terminals have to be configured once they enter the system, in a similar way to a wired ethernet.

Initially the system will use a single downlink channel, and each uplink getting time divided access to a single output from the base station, again for compatibility with ethernet. The intention is to increase the complexity of the base station to allow multiple downlinks, and increase the aggregate bandwidth at some future date.

Link model

The link protocol we envisage is a relatively short length data packet sent from the transmitter, with an acknowledge signal sent back from the receiver. In the case of the downlink the BS transmits to the MS, using previous knowledge of its position, or using all

transmitter downlinks (There is only one downlink, but turning off transmitters that transmit to unoccupied cells saves power, and reduces the chances of multipaths). The MS receives power from a particular angle, depending on the relative positions of the two transceivers. This power is focused onto a particular detector. The MS transmits acknowledge on the paired uplink VCSEL if the signal is intended for it, and it is received correctly. The BS receives the acknowledge signal and knows the data has been correctly received. Any blocking results in the acknowledge not being transmitted or not received, so the link is robust.

Blocking

The major problem with any system that uses line of sight links is blocking, and the only means to reduce the problem are by correct placing of the BS and MS. The BS is above the coverage area and the MS would most likely be on top of the monitor of the workstation. Blocking occurs when both the channel is active, and the path is blocked, so a model of the probability of the channel being active is required, as well as a model of the blocker being in line with the BS to MS path.

A number of models to describe the probability of a blocker (usually a person) being in a particular position in the space have been formulated. These use a range of assumptions i.e. the blocker is equally likely to be anywhere in the room, more likely to be around the edge etc., and from these the probability of geometrical channel blockage is obtained.

The probability of a channel being active is dependent on the type of traffic in the network, the Medium Access Control (MAC) protocols, and the data rate supported. A number of models have been combined with the blocker models to calculate worst case blocking probabilities. These range from less than 2% for a single blocker, to 6% for 2 blockers in the room. These are preliminary, and necessarily theoretical results, but indicate that blocking is unlikely to be a major problem.

Demonstrator

A demonstrator system is currently being fabricated using commercially available components and a reduced square cellular architecture. The design is to cover an area approximately 2x2m in extent using 16 overlapping square cells, with a bit rate of 20Mbits/s. Commercial ethernet IC's will be used to provide network protocols and line coding, the optical links being a replacement for coaxial cables. A 4x4 array of 850 nm VCSELs forms the source array. These emit up to 2mW in a single transverse mode, and are modulated using a laser driver IC. Initially the illumination will be the natural shape of the VCSEL devices, and the system will not be eyesafe until a diffuser is introduced at a later stage. Commercial singlet lenses are used to create an optical antenna, using the design illustrated in figure 2. Figure 4 shows the antenna optical system, that uses commercial singlet lenses.

The receiver uses an array of 16 2.5x2.5mm square Silicon PIN diodes, and a simple transimpedance receiver design [13]. At present 20Mbit/s designs have been tested using a single Silicon PIN diode, and work on the 16 receiver channels for the demonstrator are underway.

Discussion and Conclusions

The work we present here covers several aspects of the problems with optical wireless networks and their potential solutions. The eyesafety of the transmitter and the design of the receiver appear to represent the major challenges, and we are working in both these areas. Longer wavelength microcavity devices are an attractive solution, and holographic diffuser elements have the potential to provide a solution at shorter wavelengths. The problem of noise from daylight and other ambient optical noise is being addressed using tailored semiconductor devices to narrow the optical bandwidth, and AC coupled receivers to block DC photocurrent.

The system we describe here is relatively complex, and its viability is dependent on the ability to integrate the components into a compact transceiver at relatively low cost. A 'smart pixel' approach to grouping functionality, and integration and fabrication techniques offers the potential to provide this. Work on a hybrid transceiver implementation is progressing, with the aim of creating a suitable pixel design.

There is a rapidly growing demand for wireless LANs, and optical wireless can provide this facility, with a large potential bandwidth that is relatively free of regulation. Free space links are attractive for providing high bandwidth channels, and smart pixels are an attractive topology for controlling these relatively 'undirected' wireless links.

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The following bibliography is intended to provide a list of landmark papers and relevant patents for the reader who is interested in spatial light modulator technology. The list is by no means exhaustive. It was inspired from the extensive book edited by Efron on spatial light modulators, and from the US Department of Commerce Patent Database (1976-1997) which does not include foreign patents. A few World Wide Web addresses have been included so that the reader can quickly refer to commercial spatial light modulator vendors. This bibliography follows the four major subject groupings of this TOPS volume (VLSI-based SLMs, Integration and Packaging Techniques, SLM Materials and Structures, and SLM Applications) listing first books, second journal articles, third US patents and finally URLs for each category.

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