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13. ABSTRACT *(Maximum 200 words)*

This is the final report of the National Benchmark Program in Microelectronic Systems Design Automation, launched in 1994 with seed grants from ACM SIGDA and from SRC, a 3-year SRC contract, a 2-year SEMATECH contract, and a 3-year DARPA contract. This project was initiated on the premise that by leveraging the evolving technologies of the Internet, one can greatly improve the ad hoc benchmarking efforts of the past decade. Specifically, using the Internet, we have laid the groundwork for collaborative efforts of researchers from university and industry to engage in the following three major projects:

(1) internet-based benchmark data synthesis and archival workflows: conceiving and sharing new data to evaluate existing and new algorithms;
(2) internet-based algorithm and tool evaluation workflows: supporting not only user-transparent algorithm and tool encapsulation but also adopting and adapting the proven 'design of experiments' methodology to execute a series of collaborative and peer-reviewed benchmarking experiments with existing and new algorithms;
(3) internet-based statistical evaluation and results archival workflows: organizing tables of results to support various standardized forms of results evaluation and database archival of result summaries.

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National Benchmark Program in Microelectronic Systems Design Automation

Final Progress Report

Franc Brglez

30 December 1997

Army Research Office
PO Box 12211
Research Triangle Park, NC 27709-2211

Research Agreement DAAH04-94-G-0280

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Context of the Project

Background. This is the final report of the *National Benchmark Program in Microelectronic Systems Design Automation*, launched in 1994 with seed grants from ACM SIGDA and from SRC, a 3-year SRC contract, a 2-year SEMATECH contract, and a 3-year DARPA contract. The program was highly leveraged in the sense that it could not have sustained itself without the continued support from all agencies.

The motivation for this effort arose from recognition that the highly popular benchmarking efforts (measured in terms of published results, citations, and retrievals from the MCNC server since ISCAS'85) may benefit researchers, sponsors, and the EDA industry at large – provided these efforts were structured in a manner to actively engage participating partners from industry, represented by member companies of SRC and SEMATECH. It became clear in 1993 that MCNC was no longer providing the leadership it did in this effort since 1985 (with a team of volunteering professionals at MCNC and other research labs in industry).

Primary Anticipated Results. The premise for founding the Collaborative Benchmarking Laboratory (CBL) at NCSU was to bring together a critical mass of graduate students and industry participants – the latter in the form of short-term assignments of technical leaders from member companies of SRC, SEMATECH, and others, who would have the means and the ways of injecting new sources of next generation benchmarks[1]. These were to be critically tested and evaluated by graduate students at CBL as part of their *published* thesis projects – subject to peer review, to be followed by an open posting of benchmarks and first results. The design of experiments would support a measure of statistical inference such that pre-assigned confidence levels of experimental results would be an integral part of the peer-reviewed reporting guidelines.

In addition to supporting the release of new benchmarks, the infrastructure of CBL was to support a high-capacity web-site, a user-reconfigurable software environment to conduct collaborative peer-reviewed benchmarking experiments using the Web, and a database of *published results* on the Web. Here, participants would submit, via the Web, results of their experiments, along with citations of the respective publications, and be provided the capability of querying the database on the Web for 'best results' in a given category.

Current Status. CBL was awarded a major contract by DARPA in August 1997 – as a Principal Investigator in a 21-month $1,317,623 national-level collaborative project, 'Vela Project: Globally Distributed Microsystem Design -Proof-of-Concept'. The project is structured to engage the CBL team with 11 co-PIs at 7 sites, including leading researchers and students from Stanford U., UC Berkeley, UC Santa Barbara, MIT, and MSU. The project status and updates are available at http://www.cbl.ncsu.edu/vela/. An article from EE Times under http://www.techweb.com/se/directlink.cgi?EET19970616S0001 discusses the first demos of the early prototype presented during the DAC'97 (also reprinted in this report).

CBL is now part of the NCSU Computer Science Department in a modern office environment on the NCSU Centennial Campus. It supports its own file/web server with seven workstations and has added a powerful *compute server* and a 36,000 Mb disk pack, and four additional workstations as a part of the $60,000 equipment upgrade from the current DARPA grant. There is now sufficient office space and an *advanced collaborative computing environment* to support an infusion of technical leaders from member companies of SRC, SEMATECH, and others, on short-term assignments to CBL – who in turn may lend the kind of support to CBL in terms of benchmarks that did not materialize during the build-up-from-ground-zero phase of CBL's first three years (which included two moves of our lab furniture and computers).

Technologies Transferred. The most tangible technology transfer took place when National Semiconductor Corporation hired our consultant on the reconfigurable benchmarking environment project, funded by DARPA and SEMATECH. A major breakthrough of this project is the first-time, first-generation capability to synthesize a large number of graph equivalence classes with a large number of graph samples in each class. Specifically, we can now synthesize classes of *wiring signature-invariant* (WSI) and *entropy signature-invariant* (ESI) circuit mutants. We are certain that the availability of such classes will change the way the research community in CAD and computer science designs and reports on experiments that benchmark graph-based algorithms.

[1] All of the non-trivial-size benchmarks in use today came from anonymous sources in industry.

Contents

1 Problem Description

The popular but ad hoc benchmarking efforts, measured in number of citations and published results in leading electronic design automation conferences and journals, have raised expectations from program sponsors, university researchers, and the industry at large. This project was initiated on the premise that by leveraging the evolving technologies of the Internet, one can greatly improve the ad hoc benchmarking efforts of the past decade. Specifically, using the Internet, we have envisioned a scenario where we could bring together collaborative efforts of researchers from university and industry to engage in the following three major projects:

(1) *internet-based benchmark data synthesis and archival workflows:* conceiving and sharing new data to evaluate existing and new algorithms;

(2) *internet-based algorithm and tool evaluation workflows:* supporting not only user-transparent algorithm and tool encapsulation but also adopting and adapting the proven 'design of experiments' methodology to execute a series of collaborative and peer-reviewed benchmarking experiments with existing and new algorithms;

(3) *internet-based statistical evaluation and results archival workflows:* organizing tables of results to support various standardized forms of results evaluation and database archival of result summaries.

Project **(1)** and part of project **(3)** have been funded by SRC; both are briefly described in the *Related Projects* Section of this report. Project **(2)** has in part been funded by SEMATECH and mostly by DARPA; it is briefly described in the Section *REUBEN Project Summaries and Results* of this report. Project **(3)** has in part been funded by DARPA. *REUBEN* is an acronym and stands for *RE*usable *U*ser-reconfigurable *B*enchmarking *EN*vironment. We use the acronym frequently to point to objectives and techniques that have been developed as a major deliverable of Project **(2)**.

Key Challenges for REUBEN. While one may argue that REUBEN can *also* be viewed as a CAD framework capable of handling a comprehensive VLSI design flow, this was not the objective in this project. Such elusive objectives have been pursued extensively by researchers during the past decade. Rather, we limited our objectives towards the creation of an internet-based environment that supports

- generic workflow composition and reconfiguration while accessing and executing programs, data, and computing resources across the Internet;
- synchronous and asynchronous peer-to-peer interaction between members of any team during workflow composition and execution;
- synchronous and asynchronous peer-to-workflow interaction between any team member and any object in the workflow;
- a library of program and data nodes, such that editing the workflow and its execution is as intuitive as the hierarchical schematic design capture and simulation;
- creation of representative examples of multi-site multi-user applications to demonstrate that the proposed workflow implementation does provide a user-friendly paradigm for distributed and collaborative team benchmarking experiments and design.

2 Project Summaries and Results

The major goal of this project was to provide an infrastructure for collaborative composition and execution of workflows to support a series of collaborative benchmarking experiments using the Internet. Co-funded by SEMATECH, the project started with an experienced consultant (Dr. Kris Kozminski) and reached its first phase with an early technology transfer – the hiring of Dr. Kozminski by National Semiconductor Corporation in November 1995. This technology transfer took place soon after the successful first year research review of the project, attended also by the representative from National Semiconductor Corporation.

The project, as described in this report, has been completed by three students, one of them graduating with a MS degree. We highlight their contributions in terms of prime tasks and topics assigned to each student:

1. Distributed Workflow Computing and Design on the Internet;
2. Collaborative Workflow Computing, Recording, and Playback on the Internet;
3. Design of Benchmarking Experiments and Algorithm Evaluators.

Section *Publications and Technical Reports* provides a complete lists of publications, technical reports, and theses related to this project. We refer to their respective titles in the project summaries below. Section *Related Projects* provides details about the complementary projects, supported by SRC and SEMATECH.

When students started these projects, they also started their first semester in the graduate school. Consequently, their course load factor was initially high. Only during the summer of 1997 would most, but not all, students be free of the coursework and fully devote themselves to the research projects.

2.1 Distributed Workflow Computing and Design on the Internet

The project student prime is Hemang Lavana (PhD, ECE, NCSU). This project started during Summer of 1995. We provide highlights of his contributions, as part of the overall team effort, by briefly commenting on titles listed in the Section *Publications and Technical Reports*:

- **Executable Workflows: A Paradigm for Collaborative Design on the Internet.** This paper is the first formal description of the REUBEN project, the motivatation and its capabilities, published in the prestigious Design Automation Conference and Exhibition in Anaheim, CA. Concurrent with publication and presentation at the conference, our team featured well-received real-time REUBEN demos in the University Booth for the duration of the conference (including real-time collaborative sessions with the home CBL team in Raleigh, NC). A vivid description of the demo was recorded and published in a 2.5 page article in EE Times on June 16, 1997. In the next section of this report, we reprint a version of this article as we retrieved it from the Internet. The article is of particular interest since it also brings into focus the work on the REUBEN project as it relates to the currently DARPA-funded *Vela Project – Globally Distributed Microsystem Design: Proof-of-Concept* featured under http://www.cbl.ncsu.edu/vela/.

- **Internet-based Workflows: A Paradigm for Dynamically Reconfigurable Desktop Environments.** This paper received attention in the Proceedings of GROUP'97, where the theme of the conference was *The integration of multiple computer-based tools and technologies.* The abstract below summarizes the contribution of the paper.

  The Internet-based desktop environment as defined in this paper consists of a cross-platform browser, a number of server icons (host nodes), a number of application icons (program nodes) and a number of data icons (file nodes). In contrast to typical desktops of today, where data icons may be dragged and dropped onto application icons for execution, this environment allows (1) user-defined and reconfigurable execution sequences *by creating dependency edges between program nodes (application icons) and file nodes (data icons); (2)* data-dependent execution sequences *by dynamic scheduling of path as well as loop executions; (3)* host-transparency *as to the location of applications and data (both can reside on any host with a unique IP address).*

  We argue that the Internet-based workflow paradigm is suitable for creation of reconfigurable desktop environments. The summary of 450 Internet-based experiments demonstrates (1) the value of making the desktop recordable, and (2) the feasibility of rendering it collaborative.

- **OmniDesk and OmniFlows: A Platform-Independent Executable and User- Reconfigurable Desktops and Workflows on the Internet.** The REUBEN project started before web-browsers became ubiquitious. Currently, a user must run Xwindows to execute REUBEN. While feasible to execute REUBEN on a Mac or a PC workstation, execution on a UNIX workstation is more typical. This technical report (under review) outlines an approach to supporting the user interface developed for REUBEN and extending it for platform independence – i.e. a user on any hardware platform that supports a web-browser will be able to access and execute REUBEN-like workflows. This report is the blueprint for 'future work' to be performed and tested as part of the Vela Project. The abstract below summarizes the contribution of this technical report (now under review).

  Today, web-browsers provide a convenient access to the Internet while (1) increasing the number of useful desktop functions, and, (2) reducing platform dependence on the operating system of the host. This report introduces OmniDesk, *implemented as an applet, that creates a user-configurable desktop within the web-browser window. User can place any number of objects onto the OmniDesk, ranging from windows that display the contents of a directory or a file on a remote host, to* OmniFlow *applets that can execute any sequence of user-defined and data-dependent tasks. Identical versions of OmniDesk and a variety of OmniFlow class libraries can be mirrored on several Web sites or can be installed locally for faster access and execution.*

  An OmniFlow is a user-created directed dependency graph of data, program, decision, and OmniFlow nodes. Data and program nodes may reside anywhere on the Internet. The proposed approach has a number of advantages over the current html-form-based execution of CGI programs and applets. Most significantly, the OmniFlow captures, hierarchically, any number of user-defined and data-dependent task sequences, including ones that have cycles – a feature that would be impractical to implement with current html-form-based approaches. The data and program node configurations consist of one-time-only form entries which can be used and re-used in any number of OmniFlows.

  The initial experiments demonstrate the feasibility and advantages of the proposed approach. These include user-configurable OmniFlows of distributed data and distributed university and commercial software, each executable within the web-browser's OmniDesk window.

- **REUBEN-1.0 User Guide: A Reconfigurable Collaborative Workflow Execution, Recording, and Playback for the Internet.** As REUBEN evolved, the REUBEN user guide has been revised several times. The version 1.0 we are currently posting on the web for public access reflects a frozen version that we have tested with various distributed workflows as part of this project. These workflows include encapsulation of commercial and university tools to support realistic design- and benchmarking-oriented tasks as already described in earlier publications. Access to several workflows has been provided through the Web at http://www.cbl.ncsu.edu/demos/.

  User Guide and related software are scheduled for a public domain web-based release on CBL server by February 1998.

- **PosterNotes-1.0 User Guide: A Collaborative Web-based Discussion Forum and Subscription Utility.** We created PosterNotes with features that combine those of mailing lists, newsgroups, and the Web. The main purpose of PosterNotes is to facilitate and support *threaded communication* among the members of our team as well as the Internet-based collaborators and peers.

  Currently, the PosterNotes Manager supports the setup for four distinctive types of archives: (1) public discussion group archives, (2) collaborative archives, (3) CBL's group archives, (4) CBL's individual user archives. Anyone can subscribe/unsubscribe to any of the public discussion group archives. Other archives are password protected. Subscribers to the group(s) of their choice receive, every 24 hours, a headers-only list of any new posting(s). Postings can be made via regular e-mail, or through the web-browser.

  Postings via the web-browser can be public or anonymous. By posting replies through the Web, PosterNotes can display and archive the thread of all discussions. We expect that the ease of optional anonymous postings will encourage useful, but moderated, voluntary reviews, questions, and answers concerning posted technical reports, papers, and benchmarking experiments, both before and after their publication. For more information on existing discussion groups in public domain, see http://www.cbl.ncsu.edu/DiscussionGroups/.

  User Guide and related software are scheduled for a public domain web-based release on CBL server by Janunary 1998.

2.2 Collaborative Workflow Computing, Recording, and Playback on the Internet

The project student prime has been Amit Khetawat (MS, ECE, NCSU). This project started in the Fall of 1995. He completed the MS thesis in May 1997 and is now working with IBM. We provide highlights of his contributions, as part of the overall team effort, by briefly commenting on titles listed in the Section *Publications and Technical Reports*:

- **Recording and Playback of Collaborative Desktops on the Internet.** The motivation to enhance REUBEN with a recording and playback capability arose when confronted with documentation of user interface as it relates to editing and execution tasks. The abstract below summarizes the contribution of this technical report (now under review).

  This report presents a Tcl/Tk recording/playback architecture and implementation that records, plays back and executes a Tcl/Tk collaborative internet-based desktop. Specifically, the desktop

brings together distributed data, application workflows, and teams into collaborative sessions in which the control of the desktop editing and execution is shared. A typical workflow invokes distributed tools and data to support the design of microelectronic systems.

We argue that recording and playback of collaborative user interactions can have a wide-range of applications, such as: 'keeping minutes' of interactive discussions, clicks of menu-specific commands associated with different tools on the shared desktop, user-entered data and control inputs, user-queried data outputs, support for automated software documentation, tutorials, collaborative playback of tutorials and solutions recorded earlier, etc.

The summary of 540 internet-based experiments, each relying on RecordTaker *and* PlaybackMaker *to record, playback, and execute* ReubenDesktop *configurations from local, cross-state, and cross-country servers, demonstrates the effectiveness of the proposed concepts and implementation.*

- **Collaborative Computing on the Internet**. This is the title of Amit's MS thesis. The abstract below summarizes key contributions of this thesis.

  The Internet and the on-going evolution of the World-Wide Web is expected to evolve into a network without technologic, geographic or time barriers - a network over which partners, customers and employees can collaborate at any time, from anywhere, with anyone. The research in this thesis is driven by the requirements of a user-reconfigurable distributed workflow environment REUBEN, prototyped in Tcl/Tk, whose goal is to introduce and to support collaborative peer-reviewed benchmarking experiments in EDA (Electronic Design Automation) on the Internet.

  This thesis addresses issues that arise when a peer group, distributed in time and space, uses the Internet to configure and execute a distributed workflow of applications and tasks. The thesis provides solutions and Tcl/Tk implementations to support

  - *peer-to-peer communication/control of distributed software and computing resources over the Internet, including REUBEN;*
  - *recording and playback of interactive execution of Tcl/Tk applications and collaborative sessions, including REUBEN.*

  internet-based experiments, ranging from collaborative benchmarking applications to interactive tutorials, demonstrate the scope of distributed-team collaborative projects, and the utility of single-user and tutor-student recording and playback sessions.

2.3 Design of Benchmarking Experiments and Algorithm Evaluators

The project student prime is Nevin Kapur (MS, ECE, NCSU). This project started during Summer of 1996. His primary task is to demonstrate the feasibility of internet-based workflows to design benchmarking experiments with distributed users. We provide highlights of his contributions, as part of the overall team effort, by briefly commenting on titles listed in the Section *Publications and Technical Reports*:

- **Towards A New Benchmarking Paradigm in EDA: Analysis of Equivalence Class Mutant Circuit Distributions**. This paper documents the first series of experiments with *wiring signature-invariant* mutant circuits, introduced in the Section on *Related Projects*. The

experiments were conducted jointly by Nevin Kapur and Debabrata Ghosh and published in the International Symposium on Physical Design held during April 1997. The abstract below summarizes key contributions of this paper.

Today, typical experiments that report 'performance' of EDA algorithms are based on isolated instances of circuit benchmarks. In this paper, we design and report results of experiments that use a large number of sample circuits *from several* equivalence classes. *We consider a number of known circuit benchmarks and construct large samples of circuits that belong to the same equivalence class. Specifically, we examine properties of the recently introduced equivalence class of signature-invariant* mutants $\eta_i \in \mathcal{N}_{\sigma 0}(i > 0)$, *where the signature* σ_0 *is based on a* single reference circuit η_0.

The main goals of the experiments in this paper are: (1) to introduce a methodology that objectively measures the performance of algorithms used repeatedly in typical EDA tools, (2) to critically examine data sets that can be or should be used to support such a methodology. We argue that the proposed selection of mutants from the respective equivalence class represents an important set of benchmarks since we can consistently show that design objectives, being optimized by various algorithms, behave as random variables and give rise to well-defined distributions of circuit mutants.

- **Optimization of Placements Driven by the Cost of Wire Crossing**. This technical report (under review) introduces new cost placement functions, a universal placement evaluation tool, and a new placement algorithm to demonstrate a new series of experiments with *wiring signature-invariant* mutant circuits, introduced in the Section on *Related Projects*. The abstract below summarizes key contributions of this report.

  We conjecture that good column-based placements can be produced by minimizing two *wire crossing numbers: (1) the total wire crossing of all edges between cells in the wiring channel, and (2) the maximum wire crossing on the imaginary cutlines that separate cells on the opposite ends of the channels. We leverage the canonical form of the multi-level bipartite directed graph to formalize a unit-grid model that allows us to define and evalutate parameters such as total wire crossing, critical wire crossing, total wire length, critical wire length, critical wire density, total wire density, as well as height, width, and area of the embedded graph.*

  We implemented a prototype placement algorithm `TOCO` *that minimizes the cost of wire crossing, and a universal unit-grid based placement evaluator* `place_eval`. *We have designed a number of statistical experiments to demonstrate the feasibility and the promise of the proposed approach.*

  Open web-based access to `place_eval` for execution on the CBL server is planned for February 1998.

3 A Project Review by EE Times, June 16, 1997

This article appeared following demos of our DARPA-sponsored Reuben Project in the University Booth of the 1997 Design Automation Conference and Exhibition, June 9–13, 1997. The original article at http://www.techweb.com/se/directlink.cgi?EET19970616S0001 is still available. The article provides the background on DARPA-sponsored REUBEN and WELD projects as they relate to the current DARPA-sponsored Vela Project. We reprint the article in its original form below. Readers may note that a minor amount of the information about the Vela participants is quoted incorrectly. Full up-to-date details about the Vela Project can be found on the Vela home page at http://www.cbl.ncsu.edu/vela/.

EE Times (June 16, 1997), Issue: 958, Section: News

Vela project could chart new course for engineering on the Net – Web-based design hoists new sail

Richard Goering and Peter Clarke

Anaheim, Calif. - The feasibility of large-scale collaborative design over the Internet will be put to the test over the next two years in a government-funded joint project among two companies, a research institute and multiple universities. Named Vela, after a sail on the Argonauts' ship, the project will leverage Reuben and Weld, two university Web-based efforts that were demonstrated here last week at the Design Automation Conference (DAC).

Starting in September, Vela will tap eight design teams, spread out over 13 locations, to design a complex, multimedia processor chip. The 21-month project is funded by the Defense Advanced Research Projects Agency (Darpa).

Such efforts as Vela, Reuben (the Re-Usable Benchmarking Environment) and Weld (Web-based Electronic Design) may help define a new era of electronic design in which tools, models and data are accessible from any remote location, with real-time communication among design-team members. They also may challenge current EDA business models by making pay-per-use schemes feasible over the Net.

The stated goal of Vela, as described at the project's World Wide Web site, is proof of concept for a globally distributed processor design. Tools, libraries and personnel will be located across the United States. One of the project's goals will be a demonstration at next year's DAC.

Schools participating in the project include the University of California at Berkeley, the University of Southern California, the University of California at Santa Cruz, North Carolina State University, the Massachusetts Institute of Technology, Mississippi State University and Rutgers University. Other participants are the SCRA research institute (Charleston, S. C.), Data Flux Systems (Berkeley) and FTL Systems (Rochester, Minn.)

The project has a wide range of proposed deliverables. UC Berkeley, which is developing Weld, will provide an updated version of that technology with a Java-based specification charts editor; Java-based tool design visualization and collaboration; and a Java-based interface to an object-management tool. Reuben developer North Carolina State University (Raleigh) will provide a user-configurable, globally distributed collaborative workflow design environment based on Reuben; limited-time licensing access to commercial EDA tools; and peer-reviewed benchmarking contests.

FTL Systems will provide an eight-way parallel-processing version of its Auriga VHDL simulation environment and make it available as a service on the Web. SCRA will develop C++ and Java interfaces to Mentor Graphics' VHDL simulation tools.

Other proposed deliverables include a floor-planner tool that can support Web-based design; sets of models and performance-and power-analysis tools; a target cell library based on MIT's 0.18-micron Spice process; a library of blocks, including core processors, multimedia accelerators and memories; and real-time communication, including video and audio teleconferencing. The Vela project Web site is located at www.cbl.ncsu.edu/vela.

Prototype projects. Much of the expertise needed for Vela has already been developed in Reuben and Weld. Weld received considerable attention at last year's DAC but lost much of its funding in a wide-ranging cutback from one of several Darpa offices.

"We had a three-year grant which was planned to run until the end of next year. We need more money, but it's not clear where it will come from," said Richard Newton, professor of electrical engineering and computer science at Berkeley.

The Weld team nonetheless demonstrated progress at this year's DAC, including point-tool additions and the development of a generic model for Web transactions and data transfers. Newton's group also participates in Vela, which is funded with new Darpa money.

Weld researchers are writing application-programming-interface definitions, which they plan to publish so that others can write tools and translators that could be launched on the Net to work cooperatively with Berkeley's tools.

New point tools include a finite state-machine editor, called SpecChart Editor, that generates Verilog, VHDL or Java; a synthesis tool called SIS; a model checking and equivalency checking tool called VIS; and a distributed tool-flow manager. The Synopsys Design Compiler synthesis tool, which was part of last year's demo, is still available within the Weld environment.

There is also a place-and-route Java applet, which recently won "applet of the week" accolades on Gamelan, a Web site at which developers present Java applets.

The road map for the project is based on a proxy-based architecture that the team has defined in the past year. The proxies are the means by which requests for services would be put on the Net and data transferred among tools and users.

The developers believe the architecture is sufficiently general to allow transactions that might constitute the financial negotiations before a design element is completed. The user could put out a request for bids for a piece of work-say, synthesis of RTL code to the gate level-receive a bid and accept it before sending the RTL file and receiving an EDIF net-list. The proxies are also designed to include encryption for protecting intellectual property and proprietary design data.

Alternatively, the proxy architecture could be used on a corporate intranet for scheduling work among design tools. A user would launch his data on the Net and not know whether the tool processing the data was in the same building, a different state or a different country.

Work on the database and data-representation technology that will allow new and legacy tools to communicate has centered so far on the Berkeley-developed OCT data representation. Newton said the team plans to "start evaluating the IBM data model."

So far the Weld team has tested its technology on the the university intranet, though the team says the work's basis in Internet Protocol and socket communications makes the tryout equivalent to a multisite Internet run.

Next year, the work will be widened to include multiple third-party tools written to the Weld APIs. Newton said the funding will come from a Darpa grant that had not been cut. "There should be a first-cut demo at DAC '98 and a full-blown demonstration at DAC 1999," he said.

Back at this year's DAC, the North Carolina researchers working on the Reuben project offered an impressive demonstration at this year's conference, showing an ability not only to access programs and data remotely but also to provide real-time communication among team members. Reuben is controlled by an executable workflow diagram based on Petri nets.

"Our motivation is to allow any program anywhere to execute collaboratively, and we have done that," said Frank Brglez, research professor at North Carolina State. "Nobody else has anything close."

Brglez said Weld allows users to transfer data between nodes but doesn't provide the level of interactivity and feedback allowed by Reuben. But he acknowledged that Reuben is based on Tcl/Tk interfaces, while Weld, which launched later, is based on Java.

Stretched by the Web.

Reuben started as a "reconfigurable benchmarking framework" that would compare the performance or results of different programs. But the concept expanded when the World Wide Web came into widespread use.

Today, Reuben permits workflow composition and reconfiguration while accessing and executing programs, data, and computing resources across the Internet; allows real-time communications among team members; and permits interaction between any team member and any object in the workflow. Users can view programs remotely, and Reuben can play back and record any transactions.

Brglez acknowledged that sending large design files over the Internet could create bandwidth problems, but he said users can send compressed files with Java applications to expand them on the other side. And he expressed confidence that adequate encryption mechanisms will be available to protect commercial IP over open systems such as Reuben and Vela.

Reuben was funded by Darpa, Sematech and the Semiconductor Research Corp. (SRC) and is now coming to the end of its three-year project phase. The next challenge for Brglez and his students is participation in Vela.

4 Summaries of Related Projects

The major goals of related projects, supported by SRC and SEMATECH, were: (1) assemble, create, and archive *data* for the experiments, (2) design of experiments that not only verify the integrity of archived data but also demonstrate a methodology for verifiable and consistent experiments by other researchers, and (3) create a database environment that supports user-entry and query of 'best reported results'. This section complements the earlier *Project Summaries and Results* Section.

The projects, as described in this report, are being completed by three students; one of them has just graduated with a MS degree. We highlight their contributions in terms of prime tasks and topics assigned to each student:

1. Design of Web-based Database for Archival and Retrieval of 'Best Results';
2. Synthesis of WSI Circuit Mutants – Applications to Benchmarking;
3. Synthesis of ESI Circuit Mutants – Applications to Benchmarking.

Here WSI refers to *wiring signature-invariant* circuit mutants, and ESI refers to *entropy signature-invariant* circuit mutants. Both concepts are explained in more detail in the publications listed in *Publications and Technical Reports* Section. We refer to their respective titles in the project summaries below. When students started these projects, they also started their first semester in the graduate school (except for Justin Harlow). Consequently, their course load factor was initially high. Only during the summer of 1997 would most, but not all, students be free of the coursework and fully devote themselves to the research projects.

4.1 Design of Web-based Database for Archival and Retrieval of 'Best Results'

The project student prime is Adel ElMessiry (MS, ECE, NCSU). This project started in the Spring of 1996. He completed his MS thesis in December 1997 and is now working with a local database company.

- **Agent-Based Publish and Query Information System Design for the Internet.** This is the title of Adel's MS thesis. The abstract below summarizes key contributions of this thesis.

  The major goal of research in this thesis is to prototype a web-based information system MABIC *(Multi-Agent Benchmark Information Center) that supports (1) peer-submitted publication of results summarizing benchmarking experiments in EDA (Electronic Design Automation), and (2) intelligent means of retrieval, analysis, and report generation of such results. Major accomplishments of this thesis include:*

  - *agent-based network interfaces to a public domain relational database engine.*
  - *standardized entry, via the Web, of not only the typical bibliographical fields such as AuthorName, Publisher, Publication, Year, etc. but also* standardized entry of tabulated results of experiments.
  - *automated and easy to administer workflow processing of user-submitted data entries into the* shadow database *and a safe switchover procedure to the* public database.

- *efficient relational database schema, given the span of benchmarking result types.*
- *GUI classes with an extensible range of agent-based queries: from simple author-list-only to complex methods (based on data content, e.g. result quality – only papers with figure of merit exceeding a threshold are retrieved).*
- *effective filtering, based on user-selected graphing and statistical evaluation of cumulative results, for dynamic generation of reports on results of experiments.*

The MABIC implementation relies on applets in JAVA, CGI scripts using Perl, and dynamic generation of SQL commands. Except for SQL, these are representative of the state-of-the-art web-based technologies today.

User Guide and related software are scheduled for a public domain web-based release on CBL server by February 1998.

The database is undergoing final testing for the initial integrity of its data and will be accessible on the Web from CBL's home by the end of January 1998.

4.2 Synthesis of WSI Circuit Mutants – Applications to Benchmarking

The project student prime is Debabrata Ghosh (PhD, ECE, NCSU). This project started during Summer of 1995.

A major breakthrough of this project is the first-time, first-generation capability to synthesize a large number of graph equivalence classes with a large number of graph samples in each class. Specifically, we synthesize the class of *wiring signature-invariant* (WSI) circuit mutants. We expect that the availability of such classes will change the way the research community in CAD and computer science designs and reports on experiments that benchmark graph-based algorithms.

- **Synthesis of Wiring Signature-Invariant Equivalence Class Circuit Mutants and Applications to Benchmarking**. This paper will be presented during the Design Automation and Test Conference – Europe in February 1998 (DATE'98). The abstract below summarizes key contributions of this paper.

  This paper formalizes the synthesis process of wiring signature-invariant (WSI) combinational circuit mutants. The wiring signature σ_0 is defined by a reference circuit *η_0, which itself is modeled as a canonical form of a directed bipartite graph. A wiring perturbation γ induces a* perturbed reference circuit *η_γ. A number of mutant circuits η_{γ_i} can be resynthesized from the perturbed circuit η_γ. The mutants of interest are the ones that belong to the wiring-signature-invariant equivalence class $\mathcal{N}_{\sigma 0}$, i.e. the mutants $\eta_{\gamma_i} \in \mathcal{N}_{\sigma 0}$.*

  Circuit mutants $\eta_{\gamma_i} \in \mathcal{N}_{\sigma 0}$ have a number of useful properties, such as the same *number of I/Os, the* same *number of cell nodes, the* same *number of cell node pins distributed across the* same *number of cell node levels. For any wiring perturbation γ, the size of the wiring-signature-invariant equivalence class is huge. Notably, circuits in this class are* not random, *although for* unbiased *testing and benchmarking purposes, mutant selections from this class are typically random.*

  For each reference circuit, we synthesized eight equivalence subclasses of circuit mutants, based on 0 to 100% perturbation. Each subclass contains 100 randomly chosen mutant circuits, each listed in a different random order. The 14,400 benchmarking experiments with 3200

mutants in 4 equivalence classes, covering 13 typical EDA algorithms, demonstrate that an unbiased random selection of such circuits can lead to statistically meaningful differentiation and improvements of existing and new algorithms.

Open web-based access to `mutate` for execution on the CBL server is planned for January 1998.

This is the second publication in the series of experiments with WSI mutant classes. The experiments were conducted jointly by Debabrata Ghosh, Nevin Kapur, and Justin Harlow. The first series of experiments with these mutants was conducted by Nevin Kapur and Debabrata Ghosh as described in the previous section and published in the International Symposium on Physical Design during April 1997.

4.3 Synthesis of ESI Circuit Mutants – Applications to Benchmarking

The project student prime is Justin Harlow (PhD, ECE, Duke U.). This project started during Fall of 1996. Similarly to wiring signature-invariant mutants generated as part of D. Ghosh's project, the synthesis of *entropy signature-invariant* (ESI) circuit mutants represents a major breaktrough. Again, we have the first-time, first-generation capability to synthesize a large number of graph equivalence classes with a large number of graph samples in each class – now by maintaining the invariance of a circuit's entropy. The availability of such classes will again change the way the research community in CAD and computer science designs and reports on experiments that benchmark graph-based algorithms, in particular the algorithms related to logic minimization, test generation, and verification.

- **Synthesis of Entropy Signature-Invariant Equivalence Class Circuit Mutants.** This technical report (under review) introduces a new class of circuit mutants and demonstrates their applicability to analyzing the performance of Binary Decision Diagram (BDD) ordering algorithms in particular. The abstract below provides a concise summary of current contributions.

  Despite more than a decade of experience with the use of standardized benchmark circuits, meaningful comparisons of EDA algorithms remain elusive. In this paper, we introduce an entirely new methodology for characterizing the performance of Binary Decision Diagram (BDD) software. Our method involves the synthesis of large equivalence classes of Entropy–Signature Invariant (ESI) circuits, based on a known reference circuit. We demonstrate that such classes induce controllable distributions of BDD algorithm performance, which provide the foundation for statistically significant comparison of different algorithms.

5 Publications and Technical Reports

We have divided the list of publications and technical reports into three sections. The first two sections correspond to sections described in this report earlier. The last section lists the thesis projects that have been completed during the last three years.

- reconfigurable benchmarking environment and experiments;
- related projects;
- M.S. and Ph.D. theses projects.

In each section, publications and technical reports are listed in a reverse chronological order. The joint publications include not only the students directly supported from the project grants but also the PhD students and former PhD students I advised recently.

Hardcopies of 1997/98 representative publications listed in this report have been submitted, with this report, to the sponsor. *All of the listed publications, including two MS and three PhD theses, can be retrieved from the Web under http://www.cbl.ncsu.edu/publications/.* Many of these publications are available on the Web in two formats: `postscript` (as a single document), and `html` for easy navigation and review from the Web. Most of the publications have hyperlinks to related talks that have been given on the subject; again, in `postscript` and `html` formats.

5.1 Reconfigurable Benchmarking Environment and Experiments

1. A. Khetawat, H. Lavana, and F. Brglez. Internet-based Workflows: A Paradigm for Dynamically Reconfigurable Desktop Environments. In *ACM Proceedings of the Int. Conference on Supporting Group Work*, November 1997. **Three hardcopies submitted with this report.**
2. H. Lavana, A. Khetawat, F. Brglez, and K. Kozminski. Executable Workflows: A Paradigm for Collaborative Design on the Internet. In *Proceedings of the 34th Design Automation Conference*, June 1997. **Three hardcopies submitted with this report.**
3. N. Kapur, D. Ghosh, and F. Brglez. Towards A New Benchmarking Paradigm in EDA: Analysis of Equivalence Class Mutant Circuit Distributions. In *ACM International Symposium on Physical Design*, April 1997. **Three hardcopies submitted with this report.**
4. H. Lavana and F. Brglez. OmniDesk and OmniFlows: A Platform-Independent Executable and User-Reconfigurable Desktops and Workflows on the Internet. Technical Report 1997-TR@CBL-05-Lavana, CBL, CS Dept., NCSU, Box 7550, Raleigh, NC 27695, October 1997. **Three hardcopies submitted with this report.**
5. A. Khetawat, H. Lavana, and F. Brglez. Recording and Playback of Collaborative Desktops on the Internet. Technical Report 1997-TR@CBL-06-Khetawat, CBL, CS Dept., NCSU, Box 7550, Raleigh, NC 27695, October 1997. **Three hardcopies submitted with this report.**
6. N. Kapur and F. Brglez. Optimization of Placements Driven by the Cost of Wire Crossing. Technical Report 1997-TR@CBL-08-Kapur, CBL, CS Dept., NCSU, Box 7550, Raleigh, NC 27695, November 1997. **Three hardcopies submitted with this report.**

7. H. Lavana, A. Khetawat, L. Ringland, and F. Brglez. REUBEN-1.0 User Guide: A Reconfigurable Collaborative Workflow Execution, Recording, and Playback for the Internet. User Guide 1997-UG@CBL-Reuben-1.0, CBL, CS Dept., NCSU, Box 7550, Raleigh, NC 27695, December 1997.

8. H. Lavana, A. ElMessiry, L. Ringland, and F. Brglez. PosterNotes-1.0 User Guide: A Collaborative Web-based Discussion Forum and Subscription Utility. User Guide 1997-UG@CBL-PosterNotes-1.0, CBL, CS Dept., NCSU, Box 7550, Raleigh, NC 27695, December 1997.

5.2 Related Projects

1. D. Ghosh, N. Kapur, J. Harlow, and F. Brglez. Synthesis of Wiring Signature-Invariant Equivalence Class Circuit Mutants and Applications to Benchmarking. In *Design Automation & Test - Europe (DATE'98)*, February 1998. **Three hardcopies submitted with this report.**

2. J. Harlow and F. Brglez. Synthesis of ESI Equivalence Class Combinational Circuit Mutants. Technical Report 1997-TR@CBL-07-Harlow, CBL, CS Dept., NCSU, Box 7550, Raleigh, NC 27695, November 1997. **Three hardcopies submitted with this report.**

3. S. Bhattacharya, S. Dey, and F. Brglez. Effects of Resource Sharing on Circuit Delay: An Assignment Algorithm for Clock Period Optimization. *Transactions on Design Automation of Electronic Systems*, 1998.

4. S. Bhattacharya, S. Dey, and F. Brglez. Fast True Delay Estimation During High Level Synthesis. *IEEE Transactions on Computer-Aided Design*, September 1996.

5. R. Kužnar and F. Brglez. PROP: A Recursive Paradigm for Area-Efficient and Performance Oriented Partitioning of Large FPGA Netlists . In *IEEE International Conference on Computer-Aided Design*, pages 644–649, November 1995.

6. C. Gloster and F. Brglez. Partial Scan Selection for User-Specific Fault Coverage. In *European Design Automation Conference*, pages 111–116, September 1995.

7. A. Žemva and F. Brglez. Detectable Perturbations: A Paradigm for Technology Specific Multi-Fault Test Generation. In *VLSI Test Symposium*, pages 350–357, April 1995.

8. S. Bhattacharya, S. Dey, and F. Brglez. Provably Correct High-Level Timing Analysis without Path Sensitization. In *IEEE International Conference on Computer-Aided Design*, pages 736–742, November 1994.

9. R. Kužnar, F. Brglez, and B. Zajc. A Unified Cost Model for Min-Cut Partitioning with Replication Applied to Optimization of Large Heterogeneous FPGA Partitions. In *European Design Automation Conference*, pages 271–276, September 1994.

10. A. Žemva, F. Brglez, K. Kozminski, and B. Zajc. A Functionality Fault Model: Feasibility and Applications. In *The European Design and Test Conference*, pages 152–158, February 1994.

11. B. Rohfleisch and F. Brglez. Introduction of Permissible Bridges with Application to Logic Optimization after Technology Mapping. In *The European Design and Test Conference*, pages 87–93, February 1994.

12. R. Kužnar, F. Brglez, and B. Zajc. Multi-way Netlist Partitioning into Heterogeneous FPGAs and Minimization of Total Device Cost and Interconnect. In *ACM/IEEE 31st Design Automation Conference*, pages 238–243, June 1994.

13. S. Bhattacharya, S. Dey, and F. Brglez. Clock Period Optimization During Resource Sharing and Assignment. In *ACM/IEEE 31st Design Automation Conference*, pages 195–200, June 1994.

14. S. Bhattacharya, S. Dey, and F. Brglez. Clock Period Optimization During Resource Sharing and Assignment. In *ACM/IEEE 31st Design Automation Conference*, pages 195–200, June 1994.

5.3 M.S. and Ph.D. Theses Projects

1. Adel ElMessiry. Agent-Based Publish and Query Information System Design for the Internet. Master's thesis, Electrical and Computer Engineering, North Carolina State University, Raleigh, N.C., December 1997. **Single hardcopy submitted with this report.**

2. Amit Khetawat. Collaborative Computing on the Internet. Master's thesis, Electrical and Computer Engineering, North Carolina State University, Raleigh, N.C., May 1997. **Single hardcopy submitted with this report.**

3. R. Kužnar. *Partitioning and Optimization of Digital Integrated Circuits.* PhD thesis, Electrical and Computer Engineering, University of Ljubljana, Ljubljana, Slovenia, October 1996.

4. A. Žemva. *Testing and Optimization of Digital Integrated Circuits.* PhD thesis, Electrical and Computer Engineering, University of Ljubljana, Ljubljana, Slovenia, October 1996.

5. S. Bhattacharya. *Hardware Synthesis of Conditional Intensive Behavioral Specifications: Scheduling, Assignment, True Delay Estimation and RT-Level Optimizations.* PhD thesis, Computer Science, Duke University, Durham, N.C., 1995.

6 Project Participants

In order to keep CBL operational, funding must be sustained for 12 months for the principal investigator (Franc Brglez, since January 1994) and the technical assistant (Lucy Ringland, since June 1995). The effort of both has been funded from grants and contracts issued by ACM/SIGDA, SRC, SEMATECH, and DARPA.

Students engaged in the DARPA-funded projects described in this report include:

1. Amit Khetawat (MS program in ECE/NCSU, funded by DARPA, September 1995 – May 1997. Completed MS thesis in May 1997, now with IBM).
2. Hemang Lavana (PhD program in ECE/NCSU, funded by DARPA, June 1995– August 1997). Now with the DARPA-funded Vela Project.
3. Nevin Kapur (MS program in ECE/NCSU, funded by DARPA, July 1996 – August 1997). Now with the DARPA-funded Vela Project.

Students engaged in the DARPA- and SCR-funded projects described in this report include:

1. Adel ElMessiry (MS program in ECE, funded by DARPA and SRC, January 1996 – August 1997. Completed MS thesis in December 1997, now in a co-op program with a local company).

Students engaged in the SCR- and National Semiconductor-funded projects described in this report include:

1. Debrabata Ghosh (PhD program in ECE/NCSU, funded by SRC, June 1995 –)
2. Justin Harlow III (PhD program in ECE/Duke U., funded by National Semiconductor Corporation)

Earlier contributors to DARPA, SRC, and SEMATECH projects include:

1. Maitreya Sengupta (quit PhD program in ECE/NCSU, funded by SRC, June 1994 – July 1995)
2. Bruce Duewer (MS program in ECE/NCSU, funded by DARPA, Summer 1995)
3. Kris Kozminski (part-time consultant, 1995, funded by SEMATECH)
4. Stephen Shaeffer (part-time UNIX support, 1994-95, funded by DARPA)
5. Surendar Chandra (part-time UNIX support, 1996, funded by DARPA)