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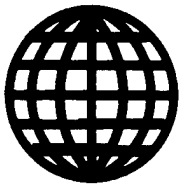


FOREIGN BROADCAST INFORMATION SERVICE

JPRS Report

Science & Technology

Japan

OEIC/OPTICAL INTERCONNECTION MINI-WORKSHOP

JPRS-JST-93-021
12 JULY 1993

SCIENCE & TECHNOLOGY
JAPAN

OEIC/OPTICAL INTERCONNECTION MINI-WORKSHOP

936C1034 Tokyo HIKARI SANGYO GIJUTSU SHINKO KYOKAI in Japanese Mar 93 pp 1-55

[Preprints from OEIC/Optical Interconnection Mini-Workshop held 24 March 93, sponsored by the Optical Industry Technology Promotion Association and OEIC Roundtable.]

CONTENTS

National Projects, OEIC/Optical Interconnection

936C1034A Tokyo HIKARI SANGYO GIJUTSU SHINKO KYOKAI in Japanese Mar 93 pp 1-8

[Article by Hiroyoshi Yajima, Electrotechnical Laboratory, Agency of Industrial Science and Technology]

[Text] The Ministry of International Trade and Industry started a large-scale project called "Instrumentation and Control Systems Applying Optics" in 1979 and has been promoting research and development (R&D) with optical electronic integrated circuits (OEIC) at its center. The image of OEIC was one in which light emitting and receiving elements and transistors such as field effect transistors (FETs) were integrated with optical relay as the model.

This was the first attempt to integrate different kinds of devices and was naturally a difficult one. The Optical Technology Cooperative Laboratory was established, and the advanced process technologies necessary for OEIC were vigorously developed. This trend was succeeded by Optoelectronics Technical Research, Ltd., as the invested business of the base center even after the completion of the project. Process research aimed at quantum OEIC is being carried out there.

However, needs for OEIC have not been growing in the field of optical relaying technology as anticipated originally. The slow rise in the construction of highly advanced optical networks including the subscriber systems is making the needs for OEIC nontransparent, though the optical communication networks are being serviced satisfactorily for trunkline systems. As long as equivalent performance can be realized inexpensively by the combination of individual components, needs for OEIC will not arise. In the information processing systems bottlenecks in the flow of signals are arising within the systems as an enlargement of the scale, high-density packaging and superparallelization of systems are promoted. The object of optical interconnection is the realization of technologies that smooth the flow of signals within information processing systems by the use of light. Realization of inter- and intraboard and inter- and intrachip optical interconnection will create new needs for OEIC.

The object of the Real World Computing (RWC) program started by MITI in 1992 is research and development in both aspects of soft- and hardware aimed at achieving flexible information processing.

Optical technology is a segment of the RWC program intended for R&D of optical interconnection technology, optical neural systems, and optical digital systems. To achieve flexible information processing, it will become necessary to actively use the two information media of electrons and light, particularly in hardware. In that connection, it will be a rational choice from system to device levels to assign the flow and processing of information to light and electrons, respectively.

The image of OEIC is also being diversified from the level of unifying the existing light that emits and receives elements and transistors to one in which such a light is mounted on large-scale integration (LSI) itself, or waveguides, optical and electronic elements are unified, or the like. The most advanced concept of OEIC is integrated basic functional devices with combined optical and electronic elements. From the materials viewpoint, OEICs having the conventional compound semiconductor, silicon and dielectric substrates as the base are being considered.

As mentioned above, the importance of OEIC, which will be the nucleus of the optoelectronic information processing field, is expected to become increasingly high in the future, and it is anticipated that new developments will take place in both the needs and seeds of OEIC. Nonetheless, it is true under the current situation that a gap still exists between the user side and the device supply side.

To break through the current circumstance, the RWC program is attempting to create a broker system that negotiates between the user side and the foundry side that supplies the devices. It is expected that such an attempt will become a detonator for the OEIC industry.

[Biography] Hiroyoshi Yajima

Education:

Graduated from the Department of Electrical Engineering, Faculty of Engineering, Keio University, 1964.

Completed the doctorate course at Keio University, 1969.

Employment:

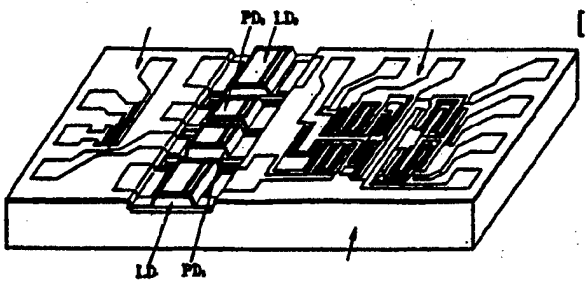
Employed by Electrotechnical Laboratory, MITI, 1969; has been engaged in research on optical waveguides, optical integrated circuits (ICs), and semiconductor lasers.

Appointed leader, Optical Information Group, Optical Technology Department, Electrotechnical Laboratory, MITI, 1988.

Appointed head, Optical Technology Department, Electrotechnical Laboratory, 1992.

Member, Japan Society of Applied Physics and IEEE.

OEIC



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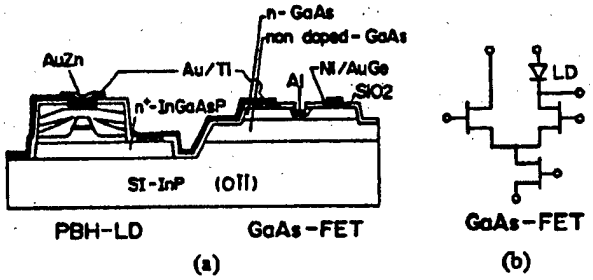

Figure 15. (a) Cross section and (b) circuit diagram for GaAs-on-InP heterostructure transmitter [42].

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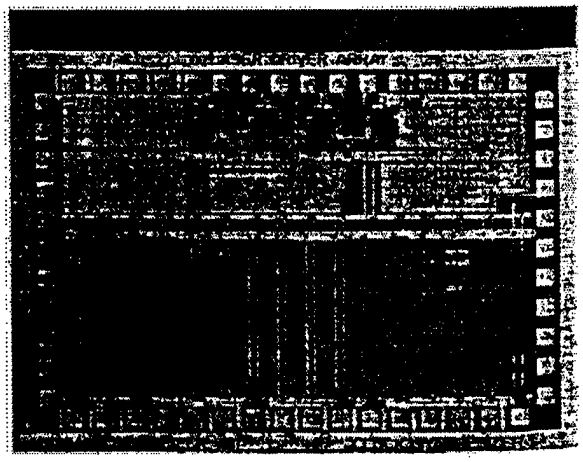

Figure 5. Transmitter chip photograph showing the four laser modulator and bias circuits (top center), PLL clock synthesizer (lower right), and serializer circuit (lower left).

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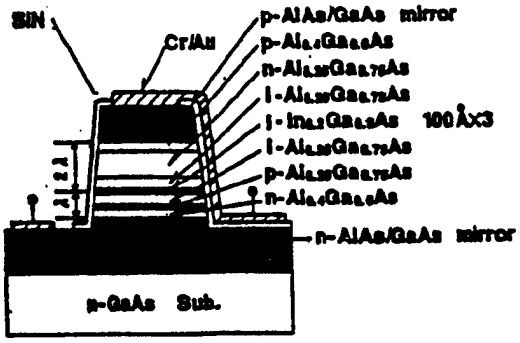

Figure 22 VSTEP[27]

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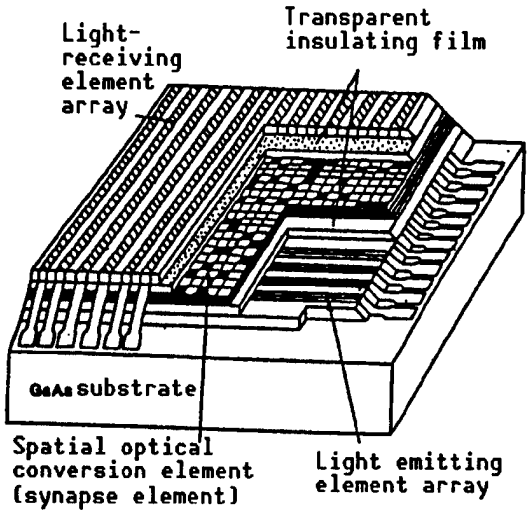

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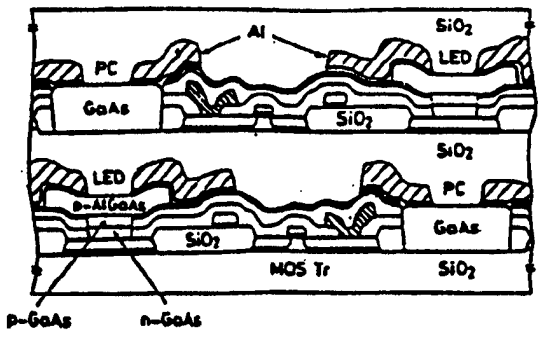

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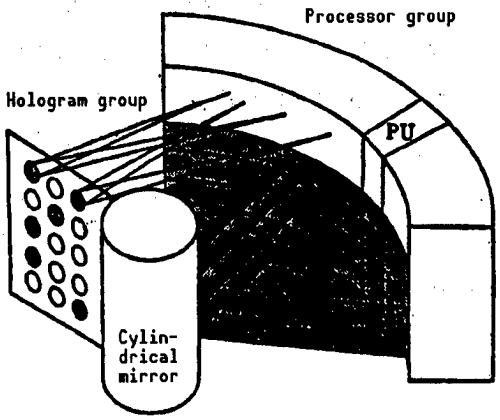
OPTICAL INTERCONNECTION AND ITS APPLICATION COMPUTER TECHNOLOGY AND OPTICAL BUS



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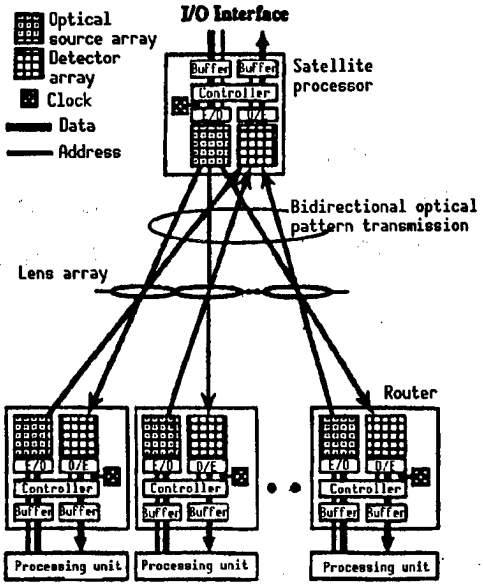

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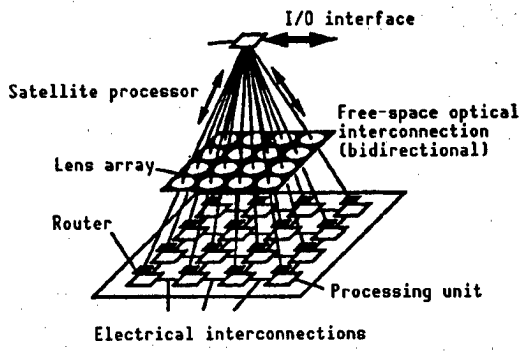

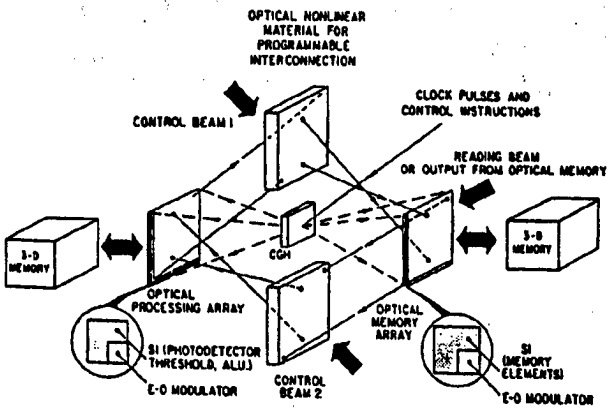

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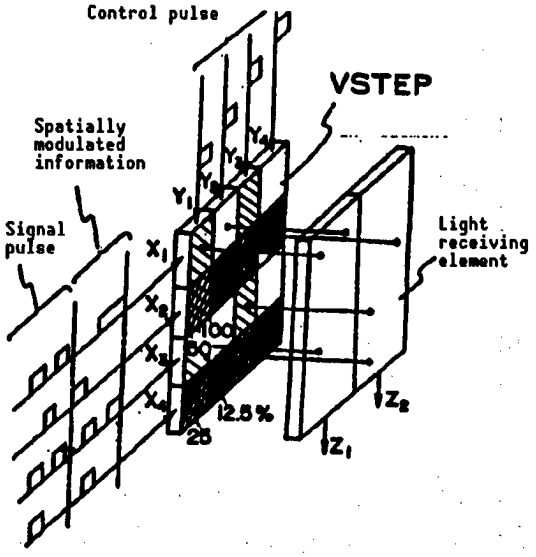
OPTICAL SWITCHING NETWORKS



Crossbar Exchange by
VSTEP [27]

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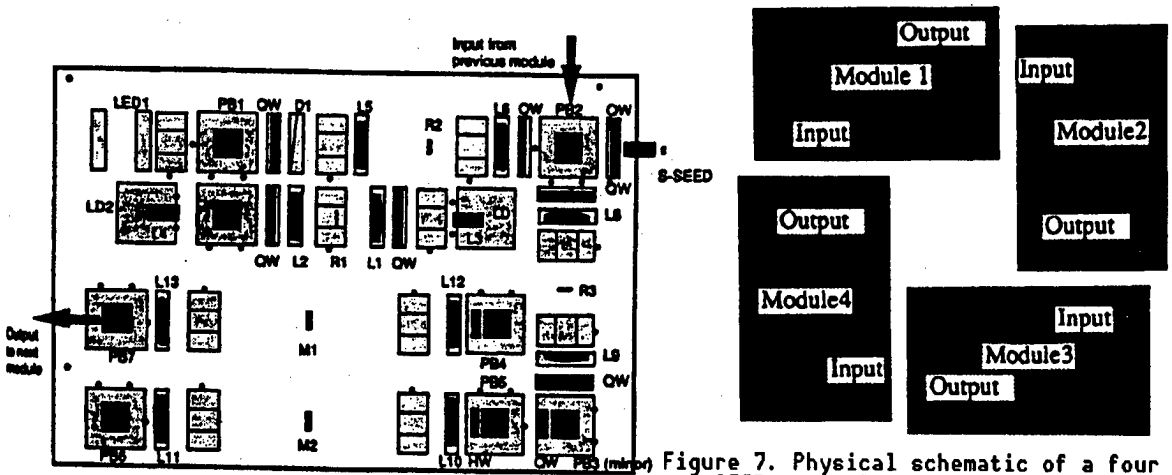


Figure 7. Physical schematic of a four S-SEED array loop showing arrangement of the modules

Table II. VLSI Technology Assumptions

Process technology	1.2 μm CMOS double-level metal
Minimum feature size (λ_c)	0.6 μm
Supply voltage (V_c)	5 V
Wire pitch (W)	2.4 μm
Wire capacitance (C_{im})	2 pF/cm
Wire resistance (R_{im})	375 Ω/cm
Gate capacitance (C_o)	8 fF
Gate resistance (R_o)	8,000 Ω
Duty cycle (K_t)	50%
Switching element speed (F_{pc})	100 MHz
Transistors/switching element (M)	130 transistors
Switch width/height (P)	1
Area/transistor (A_o)	20 μm x 10 μm
% gates switching simultaneously (K_s)	25%

Table III. Optoelectronic Technology Assumptions

Process technology	Transmission mode MQW integrated with 1.2 mm CMOS and Si p-i-n detectors
CMOS technology	See Table II.
CGH technology	E-beam fabricated CGH
E-beam min. feature size (d_{min})	0.5 μm
Optical wavelength (λ)	850 nm
No. of CGH phase levels (Φ)	4
CGH efficiency (η_d)	81%
MQW modulator size (δ)	5 μm x 5 μm
MQW drive voltage (V_m)	5 V
MQW capacitance (C_m)	20 fF
MQW efficiency (η_m)	40%
Min. detector power (P_{det})	40 μw @ 100 MHz
Detector size (δ_{det})	20 μm x 20 μm
Detector amplifier bias current (I_{bias})	20 μA
Detector efficiency (η_{det})	80%
Detector amplifier area (A_{da})	4,000 μm^2
Detector amplifier power (P_{da})	100 μw @ 100 MHz

Optical Digital System

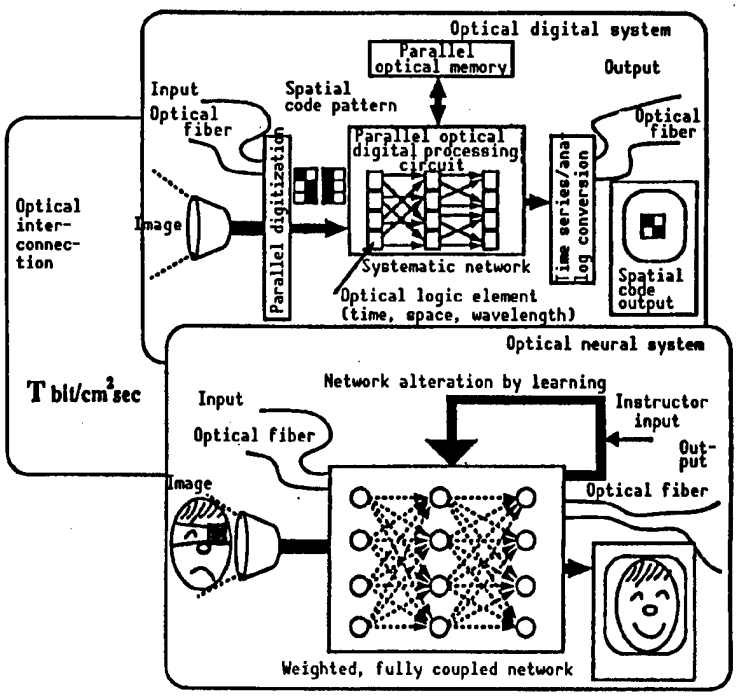
R&D of technologies for processing spatial information and wavelength information with specified spread represented by image information, based on the conventional logic arithmetic principle while keeping the parallel nature of light alive.

Optical Interconnection

Solves the problem of wiring bottleneck possessed by present-day computer through R&D of technology aimed at increasing information transmission by the use of large capacity and ultrafast characteristics of light, and of optical interconnection technology utilizing the parallel nature and controlability of light.

Optical Neural System

R&D of systems which carry out flexible information processing, such as learning and association processing, by realizing huge connections among neurons by means of light and utilizing physical properties characteristic of light.



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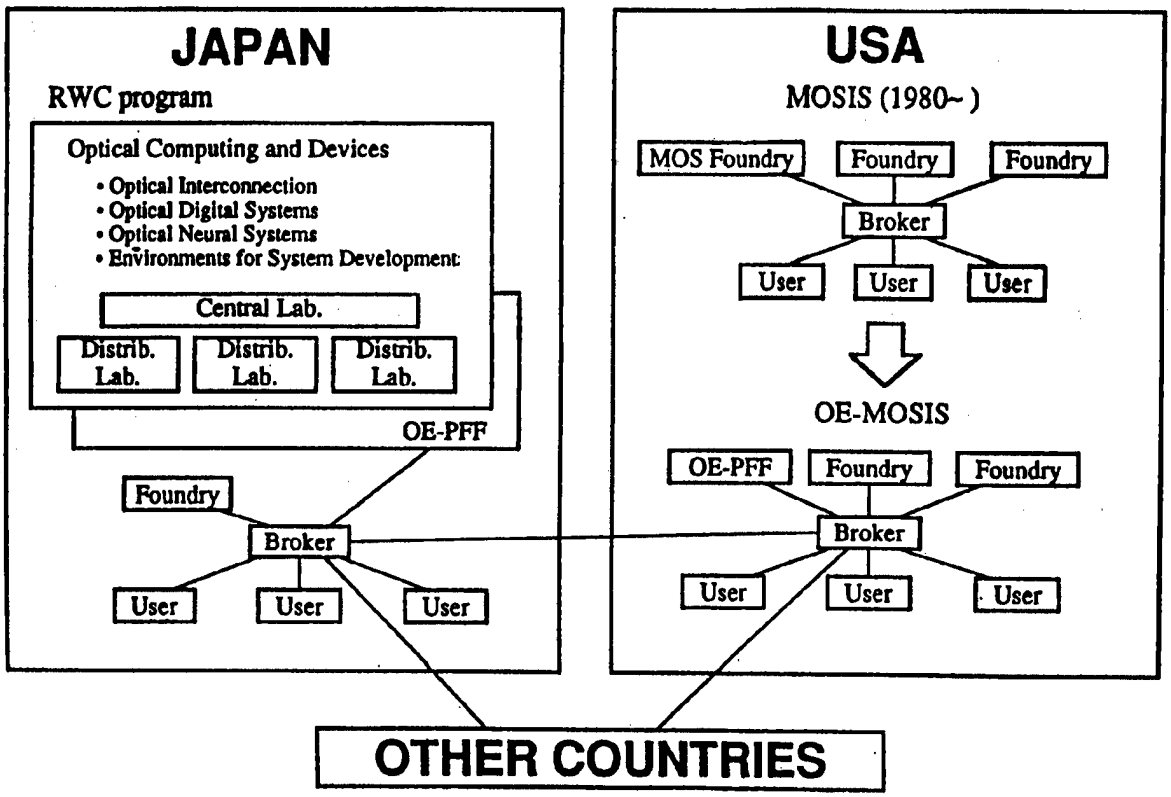


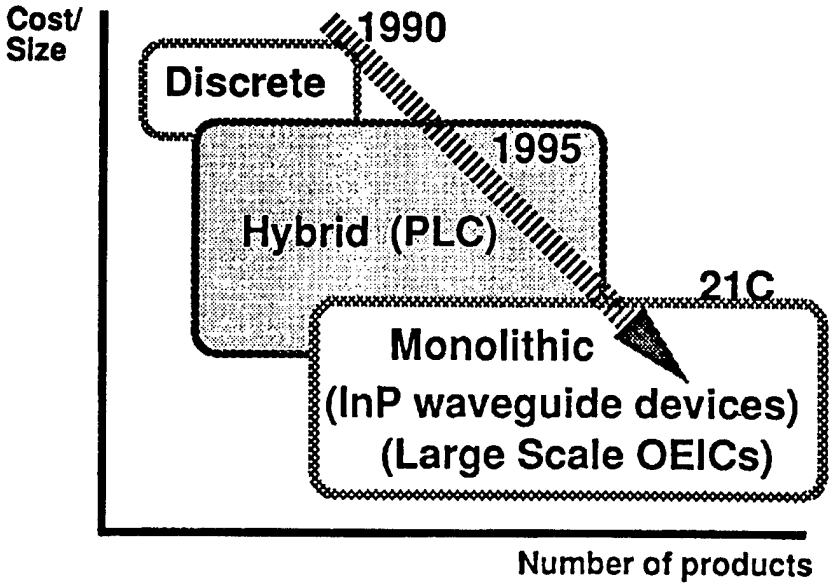
Optical Subscriber System, OEIC

936C1034B Tokyo HIKARI SANGYO GIJUTSU SHINKO KYOKAI in Japanese Mar 93
pp 9-16

[Article by Junichi Yoshida, NTT Optoelectronics Laboratories]

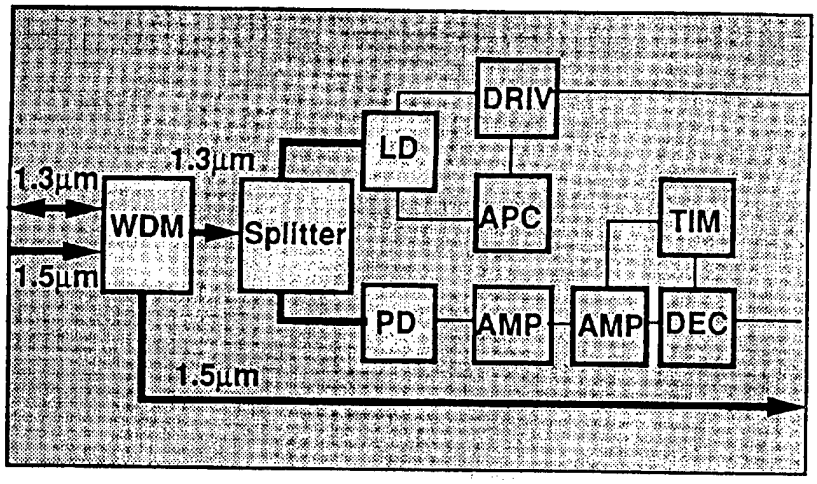
[Text] As revealed by such terms as fiber-to-the-floor (FTTF), fiber-to-the-curb (FTTC), and fiber-to-the-home (FTTH), optical subscriber systems are bringing optical fibers into the office and home and are being studied actively inside and outside the country as systems that can deal with the increase in demands resulting from the diversification and advancement of future communication services. Every country considers its own system configuration in view of trade-offs with cost-effectiveness. In Japan, a network of passive double star (PDS) configurations is currently under examination.[1] In this system, wavelength multiplexed transmission, which uses 1.3 μm of light for low rate bidirectional transmission and 1.5 μm of light for wideband transmission dedicated to outgoing services is being considered. In economizing on systems, it is mandatory to economize optical modules for which integration of optical components is indispensable. From this standpoint, we grasped integration as a means of economizing optical modules, selected hybrid optical integration as the most realistic means at the present stage, and applied it to 1.3 μm/1.5 μm WDM transmission/reception optical modules. A planar light circuit (PLC) was employed in order to achieve wavelength multiplexed wave multiplexing/demultiplexing functions, and a semiconductor laser and a detector were integrated on it in hybrid manner[2] to achieve functions and characteristics required by the system. In addition, monolithic integration of the light receiving system will be taken up in view of the adaptation to future systems, and will also touch upon the current status and the principal technical issues of the pin-FET light receiving integrated circuit.

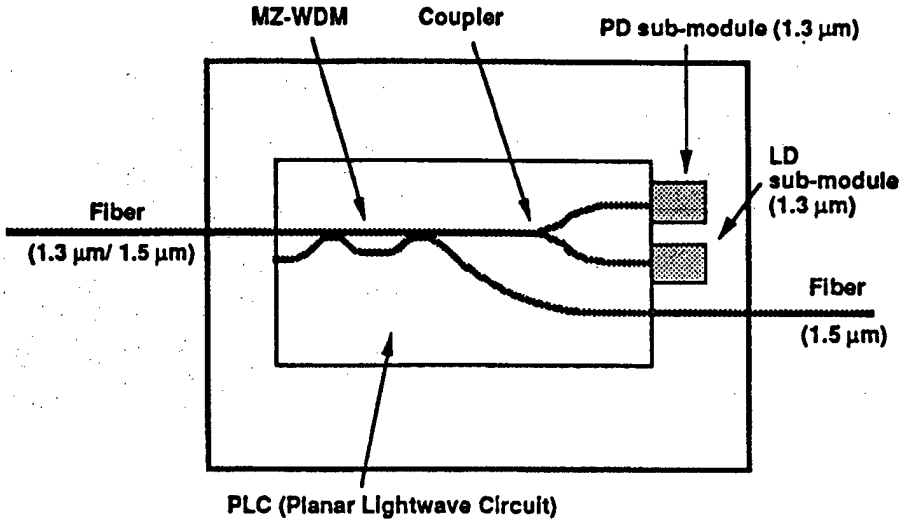
Strategies to Achieve Compact /Cost-Effective Optical Modules

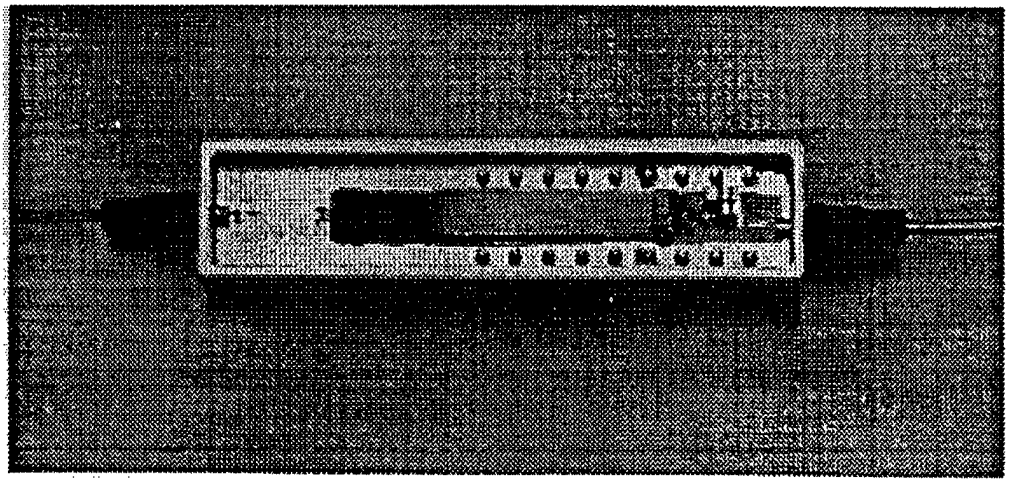


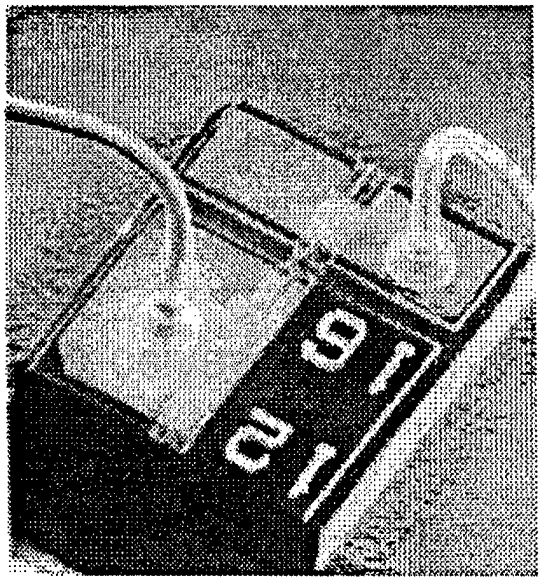
Overview of Optical Module Functions

- Time compressed multiplexing (TCM) signal : 1.3 μm
- One-way video signal : 1.5 μm



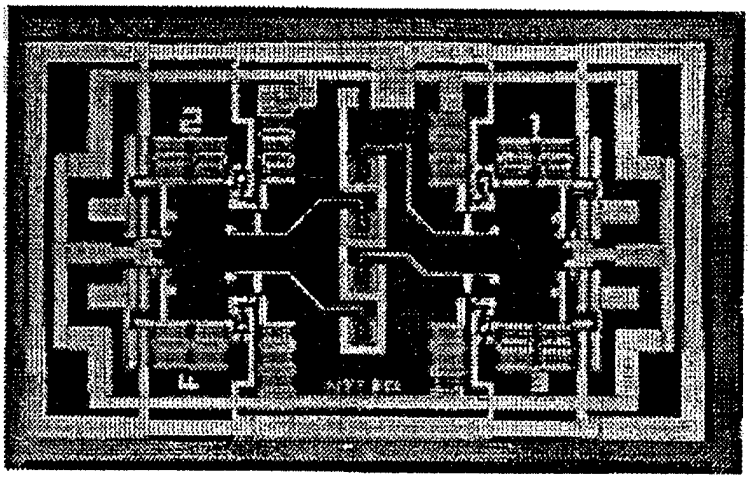


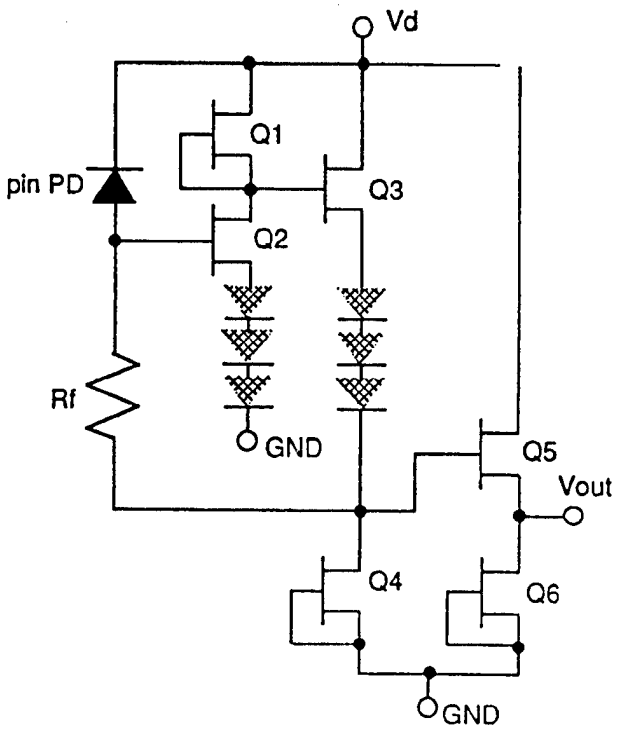




Laser Diode With Monolithically Integrated Monitor-Photodiode

- To reduce the number of components
- Permits lower laser submodule assembly costs
- Laser diode and monitor-photodiode
- Dry etching technology

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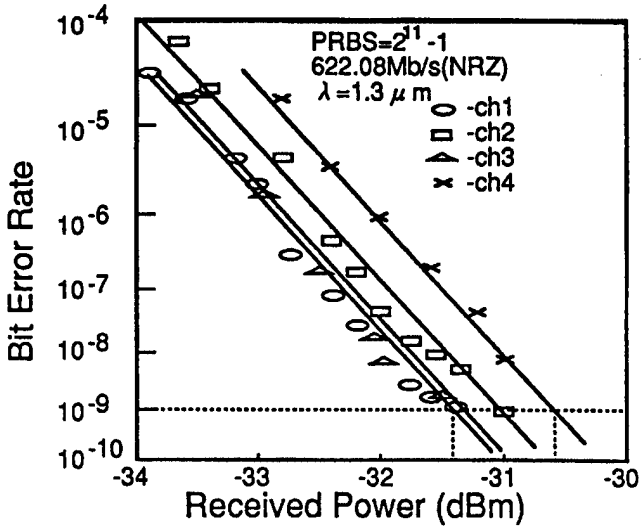

[Biography] Junichi Yoshida

Education:

Graduated from the Department of Electrical Engineering, Faculty of Engineering, Keio University, 1971.

Completed the masters' course at Keio University, 1973.

Employment:

Employed by NTT in 1973 and worked at Musashino Electrical Communication Laboratory.

Researched high output DFB laser, semiconductor lasers for analog transmission, reliability of semiconductor lasers, and photodiode for optical communications, etc.

Appointed head, Optoelectronic Integration Research Group, Optoelectronics Laboratories, 1989.

Appointed director, Research Planning Department, Optoelectronics Laboratories, 1991.

Membership:

Committee member, International Working Group, IEC International Electrical Standards Forum, since 1982.

Deputy international director, SC47C (Council for Optical Devices and display Devices), since 1991.

Member, Institute of Electronic Information and Communication Engineers of Japan and the Japan Society of Applied Physics. Senior member, IEEE.

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Packaging Technology for ULSI--Update, Outlook of Electrical Interconnection

936C1034C Tokyo HIKARI SANGYO GIJUTSU SHINKO KYOKAI in Japanese Mar 93
pp 17-24

[Article by Teruo Kusaka, ULSI Device Development Laboratory, NEC]

[Text] 1. Introduction

Enhancement of the integration level and operating speed of Si chips and putting them into a system will be continued into the future for some time. The interconnection of the chips is a task that must be done in response to the changes in the chips and will continue to be important in the future. In this article, we present an update and future outlook of the interconnection between the chips by means of electrical signals that is being used currently.

2. Interconnection Hierarchy and Signal

From devices to systems, interconnection forms hierarchies. As shown in Figure 1, from the chip side to the system side, these hierarchies consist of 1) local wirings which interconnect adjacent transistors and adjacent unit circuits (gates, cells); 2) global wirings which interconnect remote components within a chip; 3) large-scale integration (LSI) package/printed wiring board (PWB) which interconnect chips; 4) intraframe interconnection which connects one board to another; 5) intraframe cables which interconnect frames; and 6) communication transmission lines which interconnect systems.

As indicated in Figure 1, the interconnection length from hierarchy (1) to (6) becomes longer and the cost per interconnection becomes higher. From this viewpoint, in constructing a system it is advantageous functionally as well as economically to enhance the level of integration of chips and shift the functions into chips or to the side nearer to the chips. Shifts of this kind have continuously been effected in the past. It will be continued in the future until the enhancement of the level of integration of chips becomes unprofitable. The technology of refined patterning of chips, which has been the driving force for enhancing the level of integration, will be developed to achieve a quarter-micrometer.

At present, the signals used for each interconnection are electric signals for chips, the peripheral equipment, and optical signals by means of optical

Hierarchy		Common name	Length (m)	Cost (Fold)	Present	Future
Intra-chip	Proximity	Local wiring	10^{-3}	10^{-2}	Electrical	Electrical
	Distance	Global wiring	10^{-2}		Electrical	Electrical ?
Interchip		LSI package/PWB	10^{-1}	(Reference)	Electrical	Electrical/ optical
Interboard		Intraframe wiring	10^{0}	10^{1}	Electrical/ optical	Electrical/ optical
Interframe		Coaxial cable	10^{1}	10^{2}	Electrical/ optical	–
Intersystem		Transmission line	$10^{2} \sim 10^{7}$	(Outside the comparison)	Optical (electrical)	Optical (electrical)

Figure 1. Interconnection Hierarchy and Signal

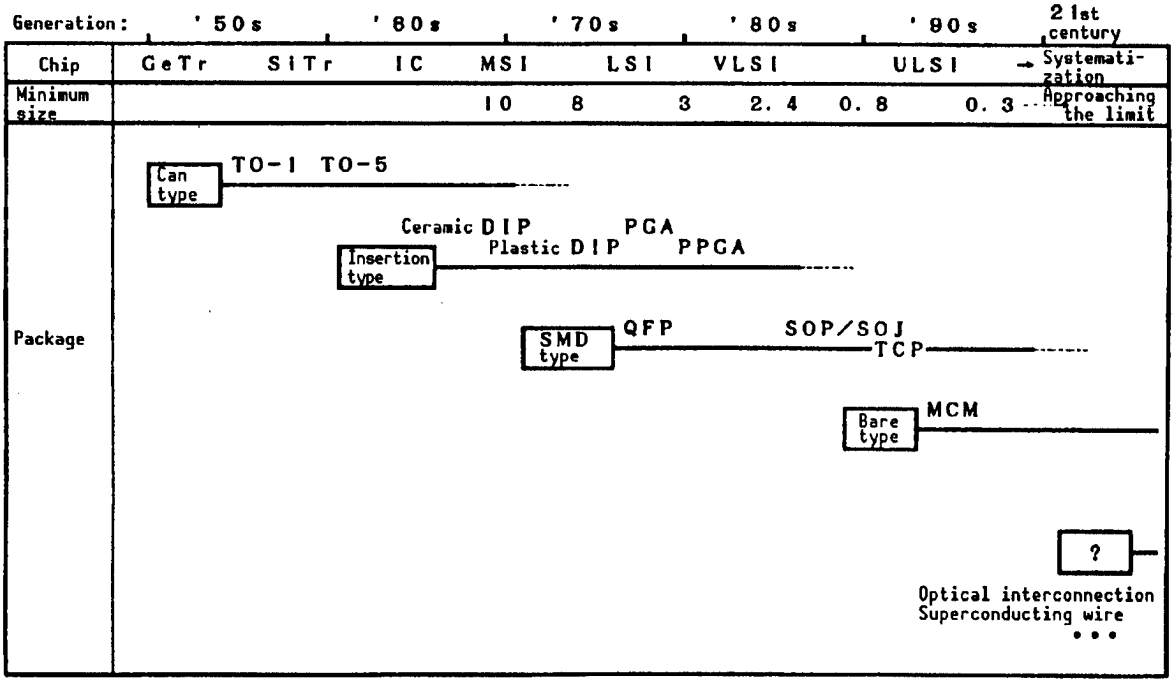


Figure 2. Changes of LSI Packaging

fibers primarily for the trunk transmission lines, as shown in Figure 1. Although electric signals are mainly used between boards and frames that come in between the above-mentioned two, optical signals are also being used for them. The optical signals will be increasingly used in the future judging from the fact that 1) the development of optical devices will advance and the product series will become more abundant, 2) the price of these products will

be reduced according to the popularization, and 3) high-speed signal processing will be required more than ever. Note, however, that the advantages of electrical interconnection will persist since the unit circuits on the chip (reference example: cell size of a quarter-micron dynamic random access memory (DRAM) is of the order of 0.6 μm^2) are electrical systems.

3. Changes in LSI Packaging

Corresponding to the remarkable improvements in the level of integration and the operating speed of the chips, the packaging of LSI has undergone changes from can type to insertion type to surfaced mounted devices (SMDs) since the 1950s. In recent years, requirements are moving towards changes for more pins, higher density, higher operating speed, and lower heat resistance.

Technical investigations about novel packaging technologies aimed at post-SMD type by imagining measures to meet the future situation have already been started. Although various approaches are currently being proposed, no definite version has yet been established. Of these, multichip packaging (MCP) is considered most significant. In MCP, a bare chip is connected directly to another bare chip, making it possible to realize 1) reduction of signal delay, 2) improvement of the withstanding capability to switching noise, and 3) increase of packaging density. The essential point of MCP resides in the connection without the intermediary of packages, the aspect of which is generically termed bare type by the author's group (Figure 2). The multichip module in the figure corresponds to the product production mode of MCP.

The present ultralarge-scale integration (ULSI) technology is trying to pursue the SMD type, or single chip packaging (SCP) in a wide sense, to the limit. In its front region, the limitation of SCP is being felt realistically, and quickening to the bare type has already begun.

Full-scale development of the bare type has just been started, and it is too early for people at this author's work level to examine the next-generation packaging mode, though its appearance is undoubted. As candidate elemental technologies for the post-bare chip type they might be beyond the ordinary electrical connection, such as optical interconnection or high-critical temperature superconducting wire, etc. (see the figure).

4. Nature of Bare Type Interconnection

In recent years, diversified investigations on MCP have been reported, Since it is too broad to discuss in its entirety, this workshop will be limited to Si-on-Si packaging and three-dimensional packaging as examples.

4.1 Si-on-Si Packaging

This packaging uses an Si wafer as the circuit substrate, which existed as a concept since the beginning of the 1980s, but was actually initiated by Japanese groups around 1985.[1] The idea spread to the United States around 1987, propagated to Europe in the early 1990s, and is now becoming a worldwide development topic (the time referred to is based on publication dates in

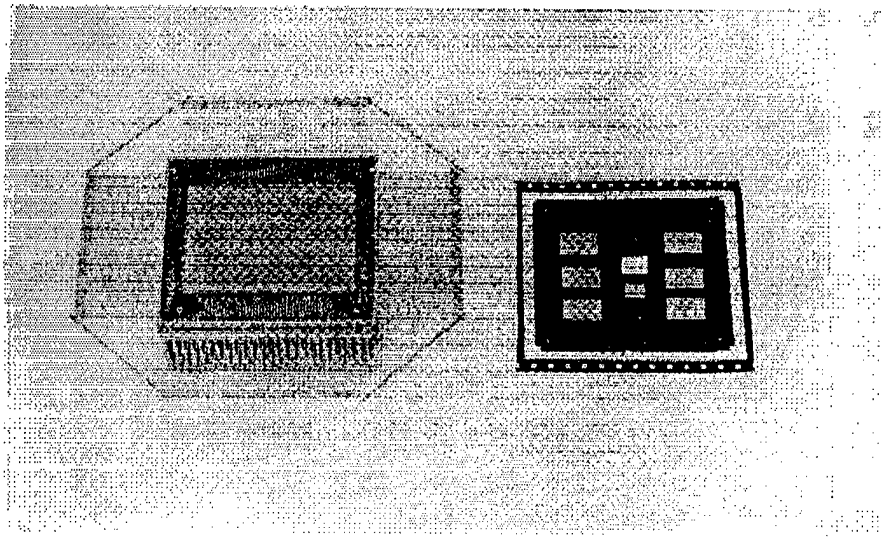
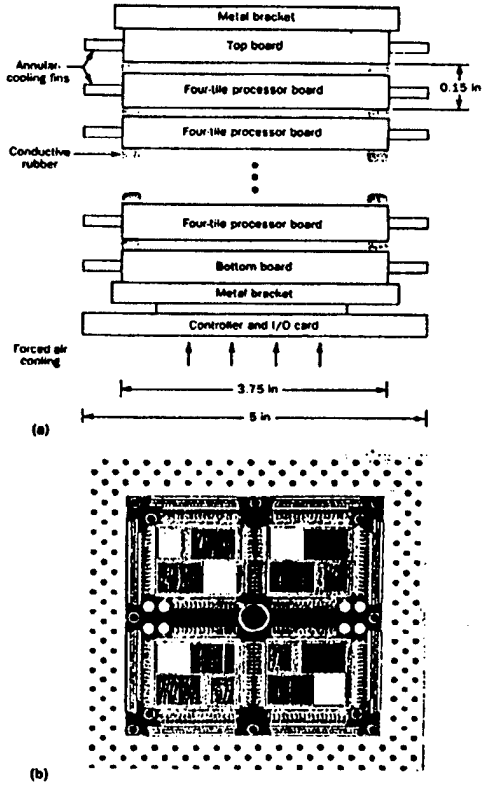


Figure 3. Si-on-Si Packaging



AT&T Bell Laboratories

- 800MFLOPS
- 200Watts

Figure 4. Packaging Example of Multiprocessor

technical meetings). The technical features include: 1) coefficients of thermal expansion are matched between the chip and circuit substrate, and thick and short connections, namely, a low inductance and low resistance chip connection, are also applicable to large-sized chips; 2) its wiring process resembles that of chips, and through active utilization of its technical resources, fine geometry and multilayering of wirings can be facilitated, and high-density wiring formation will become advantageous; 3) the connection length and propagation delay time can thereby be reduced; and 4) the heat conductivity of Si is high at 1.47 W/cm°C (comparable to that of AlN) and is suitable for heat dissipation, etc. A development example of Si-on-Si packaging is shown in Figure 3.[2]

4.2 Three-Dimensional Packaging

Compact and high-performance system hardware can be obtained by packaging the Si circuit substrate three-dimensionally as a functional unit. Several examples of basic investigation have already been reported. The one shown in Figure 4 will be described.[3]

The packaging is formed by mounting four Si circuit substrates, each loaded with a flip-chip, by bonding them on a ceramic board as if bonding tiles. These boards are further stacked to form a three-dimensional package. The periphery of the board is also used as a radiating fins and has holes for passing cooled air. The electrical connection between the Si circuit substrate and the board is done by means of metallic leads. The overall size of the board is 5 inches (127 mm square) and the size of the body part is 3.75 inches (95.3 mm square). The system consists of eight pieces of board, where the connection between the boards is accomplished by pressure bonding a conductive rubber piece. According to the report, it was possible in this way to trial manufacture a parallel processor with a peak performance of 800 million floating operations per second (MFLOPS). The thickness of a single board is 0.15 inch (3.8 mm), and the thickness of the eight-piece stack is 1.2 inches (30.5 mm). It was reported that the power consumption of the processor as a whole is less than 200 W, and it is possible to cool the system by radiating fins in the periphery of the boards. The eventual target is a parallel processor of 1 trillion floating operations per second (TFLOPS).

5. Outlook for Electrical Interconnection--What Is Its Limit?

The bare type packaging, or MCP, is still in the "budding" stage as a technology and is developing with the expectation to break through the limitation of the existing packaging (SCP). It is difficult to clearly define its limit until more time is spent and a situation is realized in which development of various specific products can be executed on a regular business level. In the course of product development, various pieces of past "retrospective knowledge" will have to be incorporated.

What can be said about the Si-on-Si packaging, which will survive until the last moment in view of its high operating speed, is that the stray inductance of the connection bump is about 0.01 nH and that the connection length to the adjacent chip on the circuit substrate is about the value obtained by adding

0.5 mm to the length of one side of the chip if the distance between the central points of the chips is to be the representative value. Stray capacitance and stray resistance corresponding to the above-mentioned dimensions exist. As the system speed is raised, stronger restrictions are imposed on the dimensions of the wirings because of crosstalk and impedance matching.

From these observations and the heat radiation (higher density of the package resulting in higher density of heat generation), there is no doubt that the present electrical connection between the chips will sooner or later be limited. However, it is not clear when this will occur.

6. Conclusion

In the long term, there will be movement towards LSI packages that include systems, and, further, will be constructed as a system-on-chip. This means that a high-performance processor will be placed on the desk of each person. These processors will naturally be linked to form a network. In order to interconnect a large number of processors at high speed, optical interconnection will be advantageous in terms of communication speed and information quantity to be transmitted. If each processor on the desk is put in the form of one chip, then the interconnection between the processors will be assimilated into interconnection between the chips. Due to such a circumstance, there is a possibility in the future that the interconnection between the chips will be performed by means of optical interconnection.

[Biography] Teruo Kusaka

Graduated from Faculty of Engineering, Tokushima University, 1968.

Employed by NEC, 1968. Assigned to Semiconductor Department and engaged in research on development of high breakdown voltage LSIs for digital exchange subscriber circuits.

Reassigned to Device Development Laboratory, NEC, 1987.

Reassigned to ULSI Device Development Laboratory, NEC, 1992.

Currently researching ULSI packaging technologies.

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2. Kusaka, T., et al., "A Silicon-on-Silicon Packaging Technology for Advanced ULSI Chips," Proceedings of 43rd ECTC, 1983, to be published.

3. Blonder, G.E., et al., "Interconnection Processes and Materials," AT&T TECH. JOURNAL., Vol 69 No 6, 1990, p 46.

Electrooptical Mixed Packaging Technology

936C1034D Tokyo HIKARI SANGYO GIJUTSU SHINKO KYOKAI in Japanese Mar 93 pp 25-30

[Article by Takao Edahiro, NTT Interdisciplinary Research Laboratory]

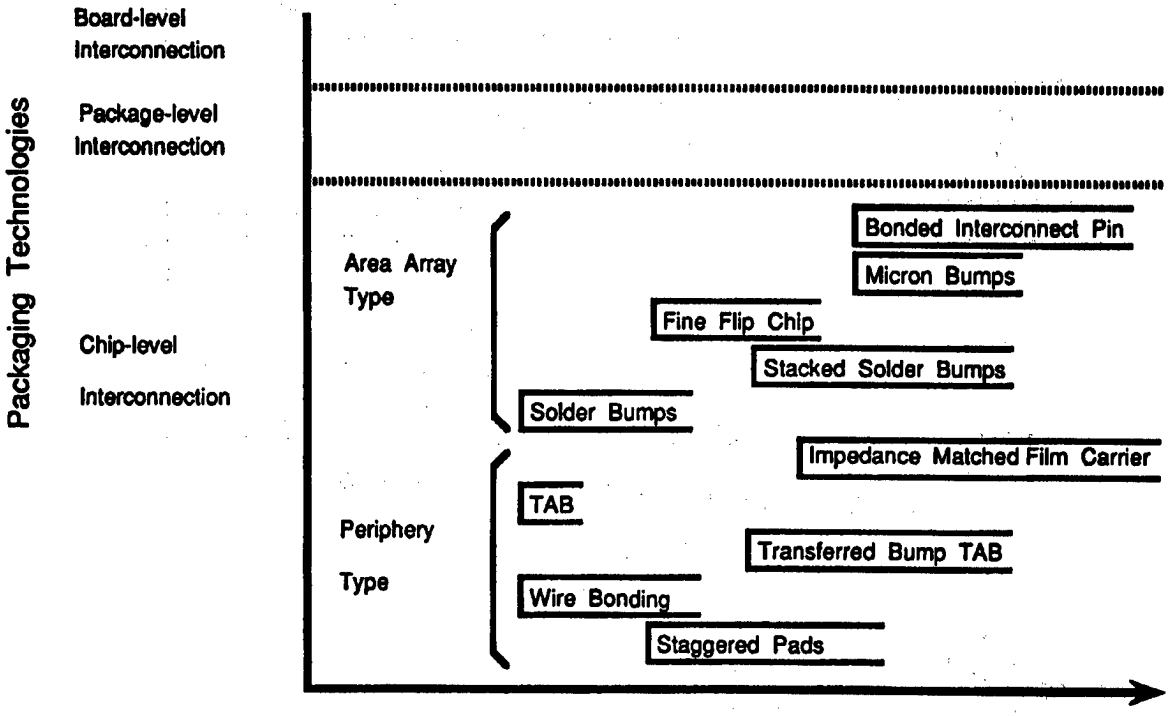
[Text] **Summary**

The B-ISDN is expected to achieve high speed and wideband communication. In order to provide such services, it is necessary to improve the transmission capacity of communication equipment, and investigations of optical interconnection technology, which enables signal transmission mainly between equipment and between modules within equipment by means of optical fibers, are in progress. In addition, applications of optical interconnection between chips by means of optical waveguides are also under investigation in order to eliminate bottlenecks of electrical wiring within modules. Among these movements, the development of high-speed and high-density electrooptical mixed packaging technology that can deal with the progress of high-density integration of the electronic devices is indispensable.

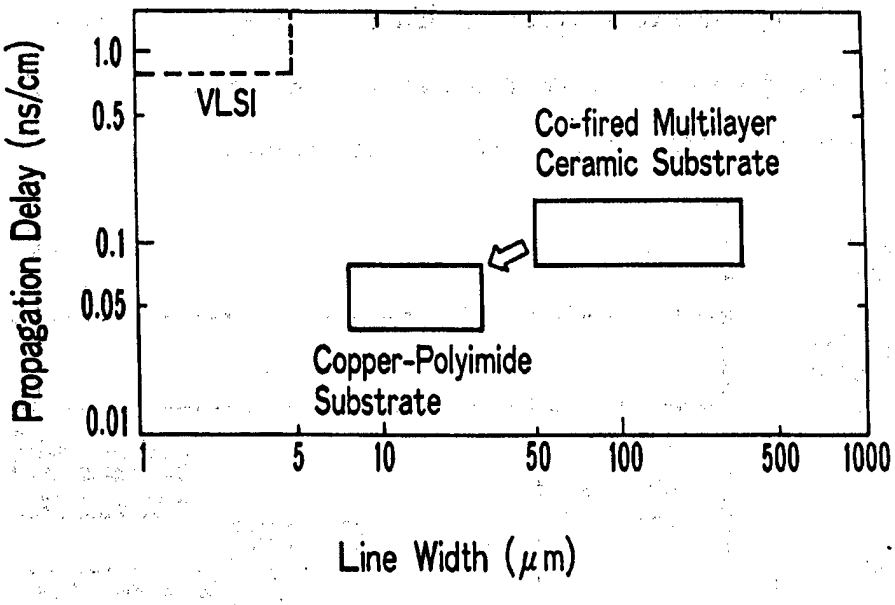
From this viewpoint, we will present in this lecture, the latest high-speed and high-density electrooptical mixed multichip moduling technology centered around the electrooptical mixed-wiring board, in which copper polyimide, high-speed multilayer wiring and optical waveguides are unified.

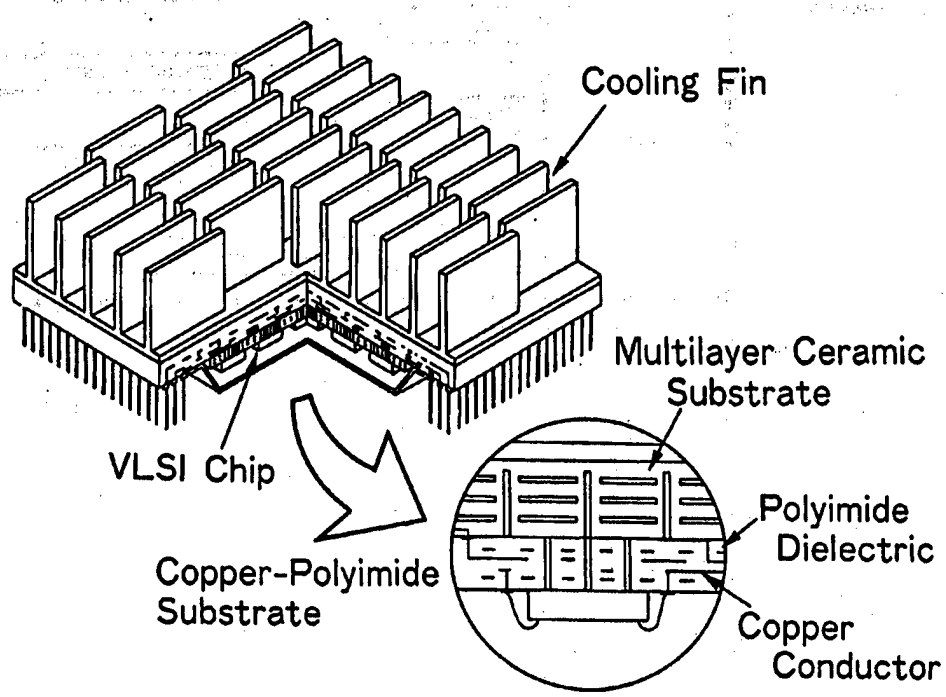
Condition Required for Future Electrooptical Mixed Packaging Technology

- High-speed electrical wiring board technology: Gb/s class
- High-precision optical interconnection technology: ±1 μm
- Unification of electrical and optical wirings

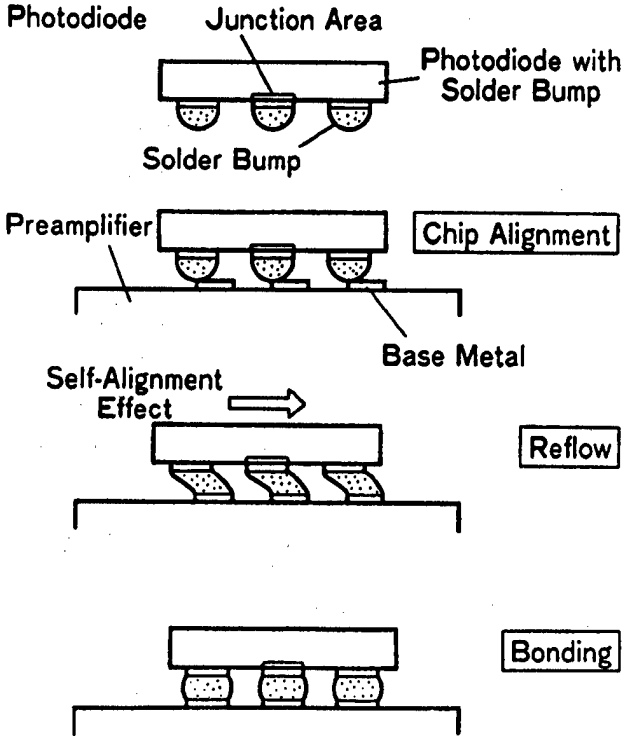


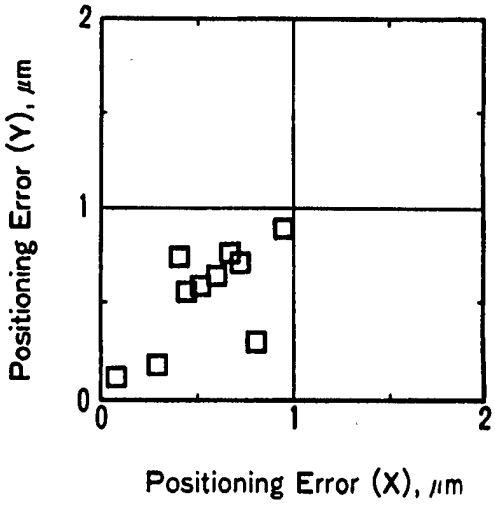
MCM Utilizing Copper-Polyimide Wiring Board Technology

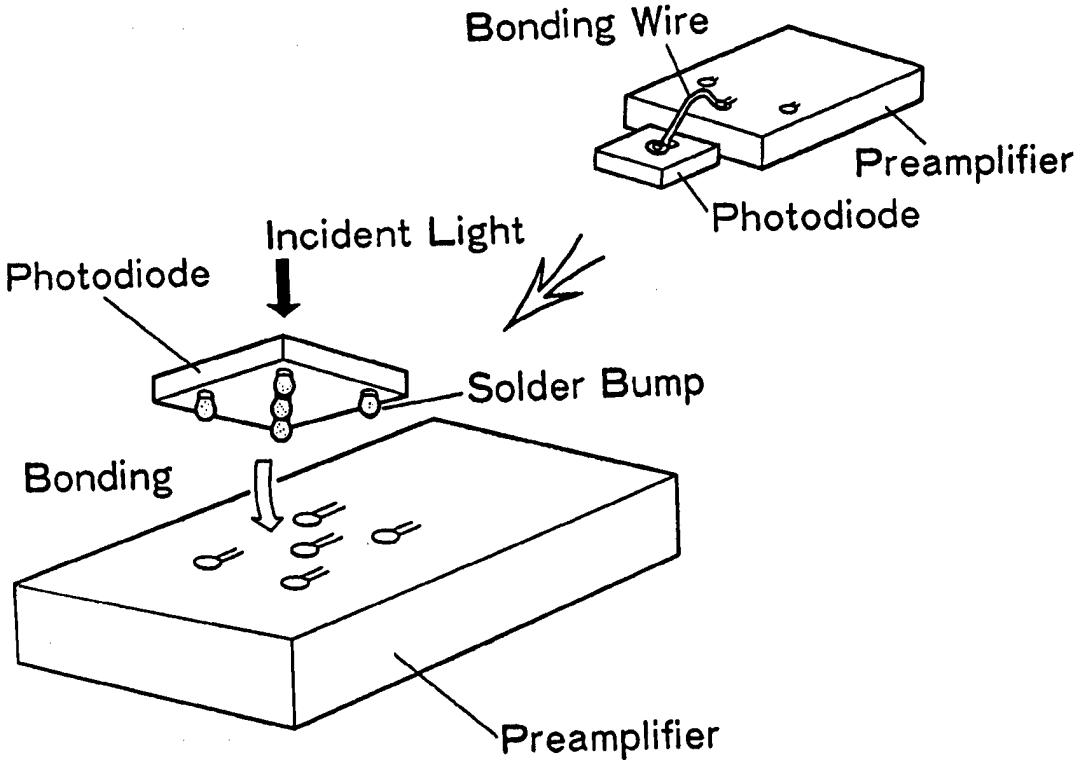


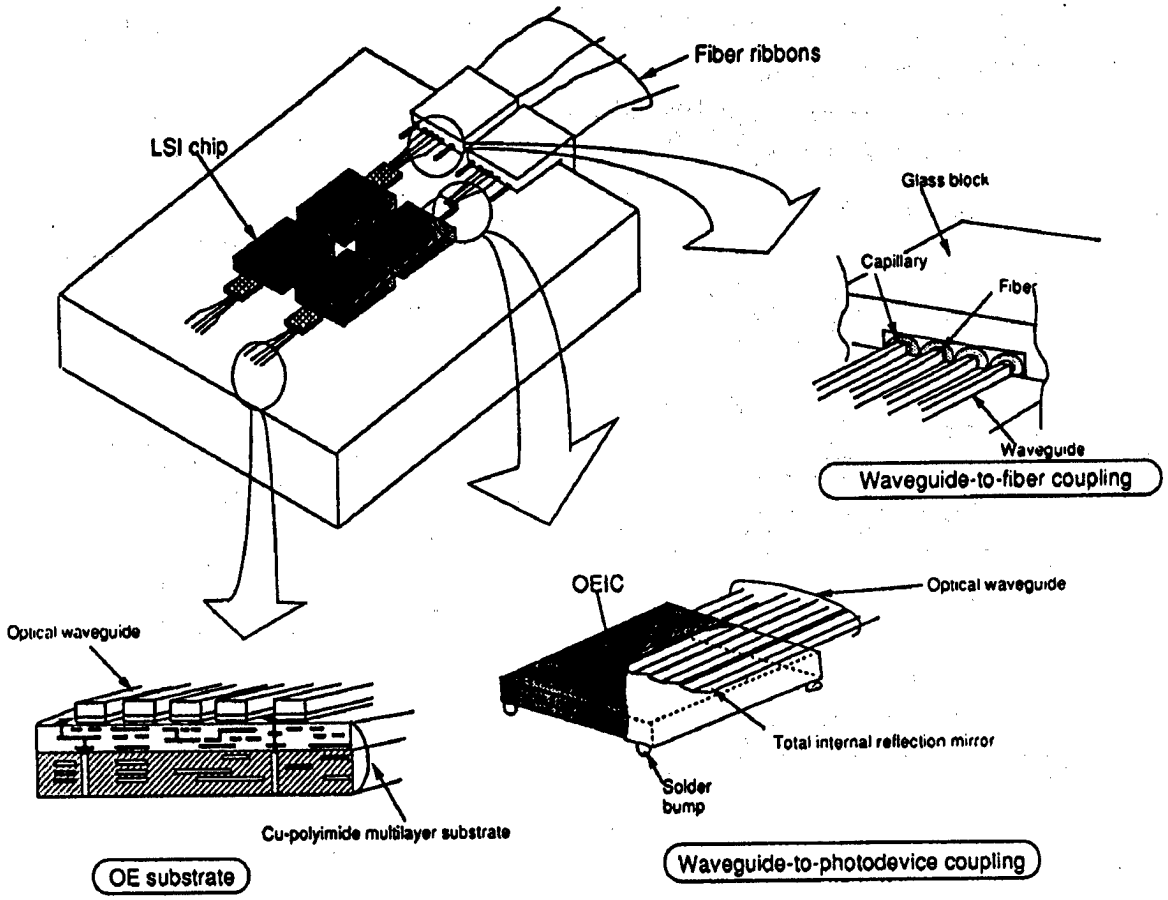


Photodetector Module Utilizing Solder Bump Technology









Electrooptical Mixed Packaging Technology

- High-speed electrical wiring board technology

  Copper polyimide wiring board

- High-precision alignment technology

  Solder bump technology

- Optical waveguide technology

  Unification technology with electrical wirings → Electrooptical mixed wiring board

  Optical interconnection technology with optical elements → Mirror coupling

  Optical interconnections technology with optical fibers

[Biography] Takao Edahiro

Born in Hoten, Manchuria, 1943.

Graduated from the Department of Electrical Engineering, Faculty of Engineering, Osaka University, 1966.

Completed the masters' course, Graduate School of Engineering, Osaka University, 1968.

Employed by NTT (Electrical Communication Laboratory), 1968.

Worked at NTT overseas office, New York, 1983–1986.

Dispatched to Verisys Inc., 1990–1992.

Appointed director, NTT, Interdisciplinary Research Laboratory, December 1992. During this period researched optical fibers and waveguides.

Conferred Doctor of Engineering, Osaka University: Research on optical fibers.

Received the Achievement Award and Paper Award from the Institute of Electrical Communication Engineers of Japan.

Awarded Official Commendation of the Director and received Kajii Award from NTT.

Optical Mount Technology

936C1034E Tokyo HIKARI SANGYO GIJUTSU SHINKO KYOKAI in Japanese Mar 93
pp 31-39

[Article by Teiji Uchida, Development Laboratory, Tokai University]

[Text] **1. Introduction**

According to statistics put out by the Optical Industry Technology Society, the domestic production scale of the optical industry in 1992 is estimated to have reached about ¥3.68 trillion. In the meantime, optoelectronics has been making steady progress in research and development (R&D) relating to performance, but is facing a serious manufacturing technological barrier in that the technologies for adjustment, assembly, mounting, etc., of optical devices cannot follow the increase in production quantity. This author has been pointing out this problem since around 1988.[1] Particularly conspicuous is the fact that research and development of mount technology of optical devices has hardly been carried out compared to standardization on the level of optical elements and devices. The following presents an outlook on optical mount technology.

2. Hierarchy in Optical Mount Technology

In discussing optical mount technology, it is necessary to clarify the hierarchical structure of optical mounting. A hierarchical configuration prepared based on the literature is shown in Figure 1.[2,3] The concept concerning optical interconnection for each hierarchy is summarized in Table 1.

2.1 First Hierarchy Optical Interconnection: Element Level

2.1.1 Two-dimensional E-LSI

The necessity for introduction of optical interconnection is not clear-cut.

2.1.2 Three-dimensional E-LSI

The interlayer optical interconnection of a monolithic three-dimensional LSI is a long-term problem. In electrical three-dimensional LSI projects, the perspective was not bright. On a short-term basis it may be possible to apply a few interconnections for optical space between laminated chips.

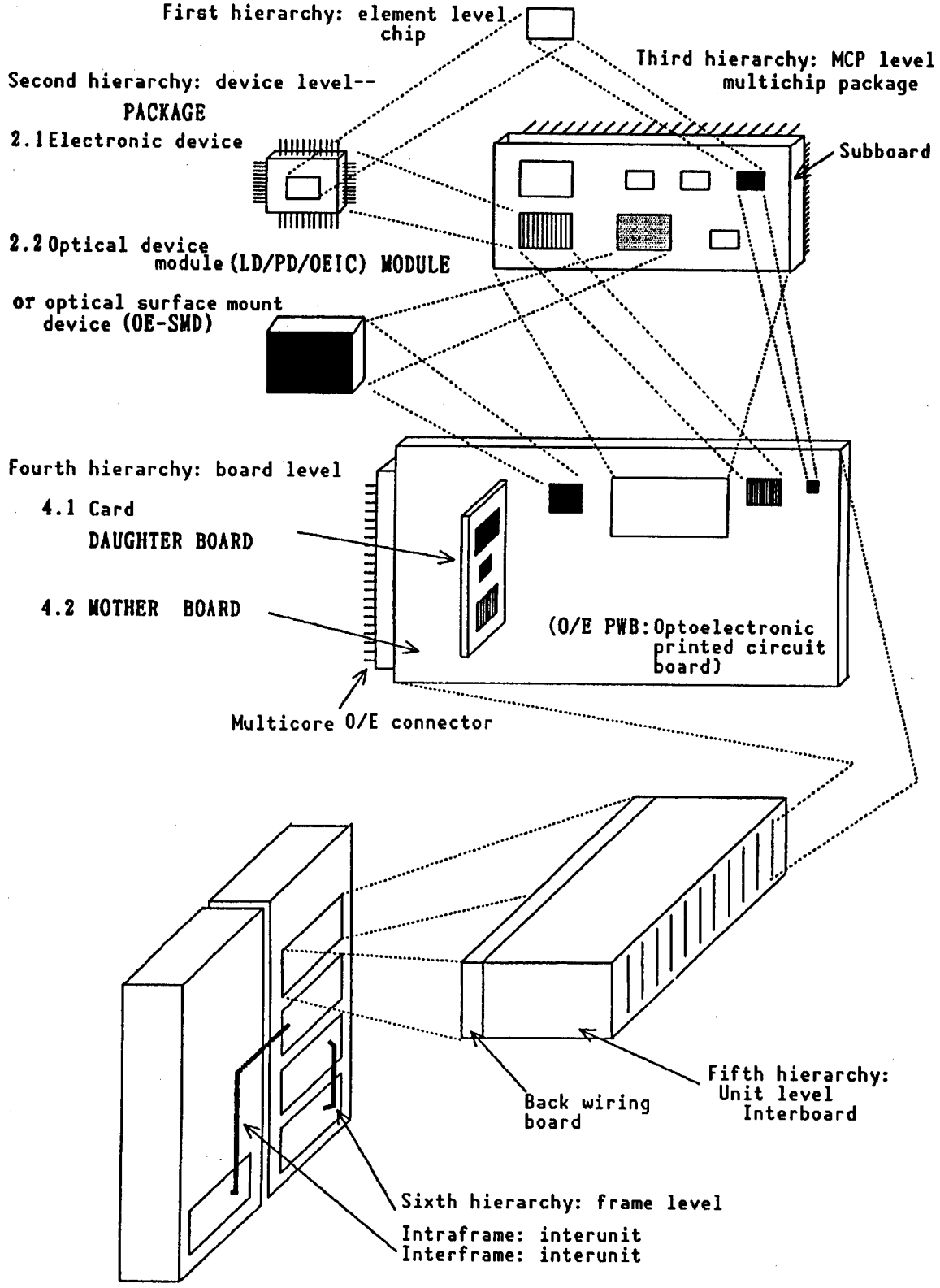


Figure 1. Interconnection Hierarchy in Optical Mount Technology

Table 1. Update and Future Estimate of Optical Interconnection Technology

	Present	Future forecast
1st layer— Chip level	Nothing	Intrachip optical coupling?
2nd layer— Device level	Microoptics Pigtail system	MO/PLC on SEMICON. (Si/InP/GaAs) Optical connection between O-SMD/Chip
3rd layer— MCP level	LN/glass WG Pigtail system	Above + O-SMT
4th layer— Card/board level	Pigtail system Optical fiber/ cable	O-SMT (O-SMD/O-PWB)
5th layer— Unit level: Interboard	Multicore O/E connector Optical fiber/ cable	Optical spatial connection? Topological optical inter-connection Back plane: Optical flat cable/ O/PWB
6th layer— Frame level: interunit	Above	Optical fiber/cable

Note: MO: microoptics; PLC: planar lightwave circuit
Back plane: back plane wiring board

2.2 Second Hierarchy Optical Interconnection: Device Level

As a device within a package, installation of a plurality of elements on a semiconductor substrate (MO/PLC or SEMICON: Si/InP/GaAs)[4,5,6] ceramic has been studied and considered promising. However, this is limited to dimensions that can be accommodated within a package, and it is difficult in cost-effectiveness to achieve one with card/board level dimensions.

2.2.1 Horizontal light input/output type

As shown in Figure 2, the optical interconnection with the chip is done by microoptics, and the take-out from the device is generally done according to the fiber-pigtail system. However, when the input/output number is large, such as in the star coupler of the subscriber system, optical exchange, and optical information processing, the fiber-pigtail connection has poor matching with the future automatic assembler, and difficulties arise in cost-effectiveness including the possibility of breakage and the dimensions, which correspond to the electrical wirings of the past electron tube era.

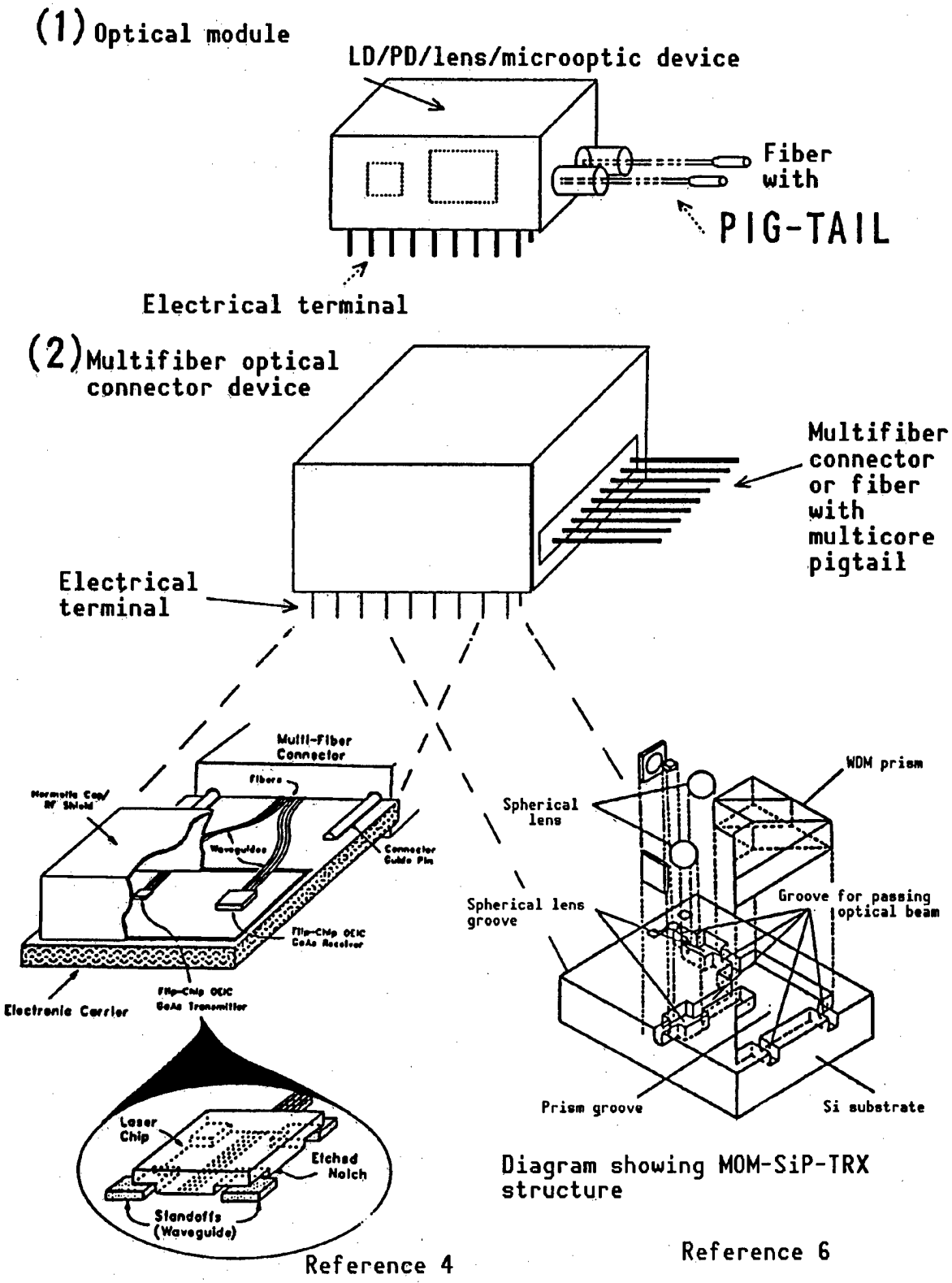


Figure 2. Horizontal Light Input/Output Type Devices

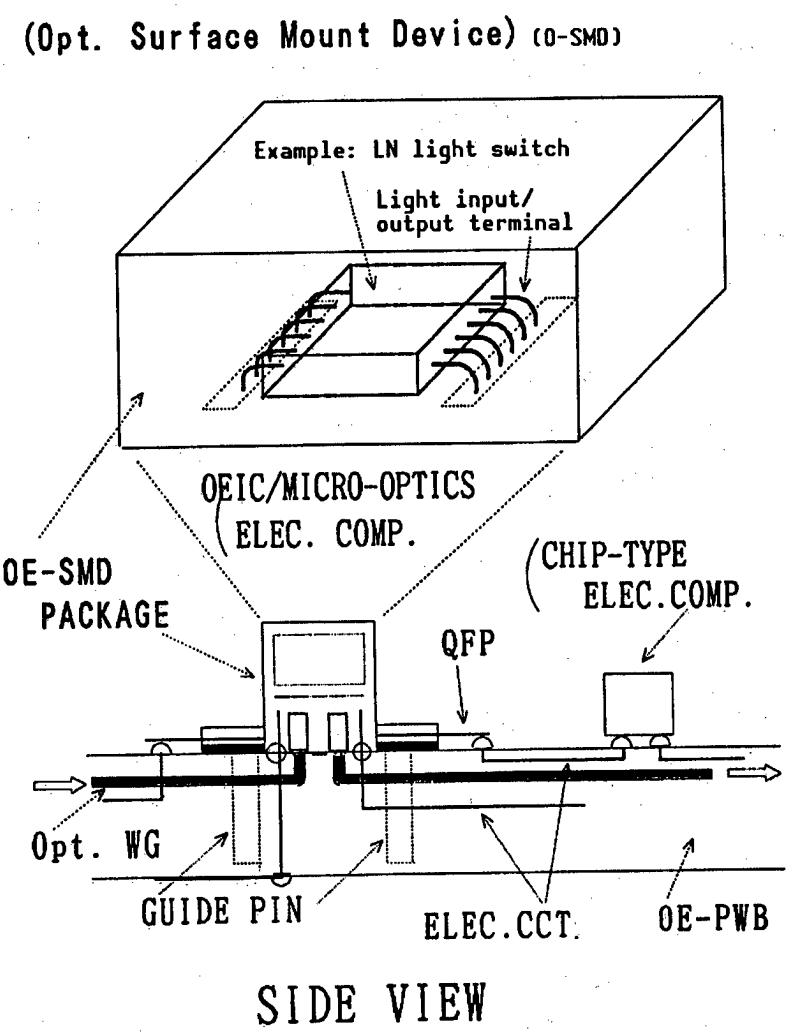


Figure 3. Vertical Light Input/Output Type

2.2.2 Vertical light input/output type

In order to avoid the fiber-pigtail system, one has to adopt the optical surface mounting system as shown in Figure 3.[1,7]

2.3 Third Hierarchy Optical Interconnection: Multichip Level

When a large number of electrical LSIs are arrayed on a ceramic substrate as seen in a large or supercomputer, use of a light guide for connecting separate chips may be considered. It is suitable to transmit signals of several hundred MHz to several GHz. Moreover, it will be an object of application of optical surface mount technology in the future.

2.4 Fourth Hierarchy Optical Interconnection: Card/Board Level

At present the practice is to mount optical devices/modules, etc. of fiber-pigtail type on the board. If this trend continues towards optical exchange and information processing as optical technology advances from the subscriber system, the surface of the board will be covered with optical fibers, which will give rise to serious problems in view of operability, dimensions, failure rate, cost-effectiveness, etc. In spite of this, the fourth hierarchy (including part of the third hierarchy), namely, the mounting of optical devices on the card/board has hardly been investigated. In this sense, this author has been proposing optical surface mount technology (O-SMT) as shown in Figures 3-7.[1,7] The basic idea is to provide mount technology that does not require adjustment by assigning respective standardized interfaces to opto-electronic surface mount devices (OE-SMDs) and optoelectronic printed wiring boards (OE-PWBs). The first point to be noted in OE-PWB is to embed the optical waveguide below the surface in order to avoid the surface's influence. In addition, it is desirable to have a structure free from irregularities as much as possible. A multilayered optical printed wiring board may be constructed by, for example, laminating single-layered, glass waveguide substrates. Further, a composite substrate formed by laminating an optical printed wiring board on a multilayered ceramic substrate for electrical wiring may also be realistic. It should be mentioned that the semiconductor substrate may not be suitable in view of its size and cost-effectiveness. In the electrical field, surface mount technology (SMT) and the automatic assembling device are being used widely in household, communication, and information processing equipment.

2.5 Fifth Hierarchy Optical Interconnection: Unit Level

A back plane board is generally considered suitable for interconnection between boards. Although a multifiber optical connector and optical fiber/cables are used at present, introduction of the OE-PWB technology will be anticipated if it makes sufficient progress.

For interconnection between the optical switching board, topological interconnection which optically connects two boards that intersect orthogonally is used.[8] In addition, interconnection of boards by means of optical spatial interconnection is being attempted but has problems such as optical alignment and crosstalk.

2.6 Sixth Hierarchy Optical Interconnection: Frame Level

For interconnection between units, the multifiber optical connector and optical fiber/cable will remain as the mainstream.

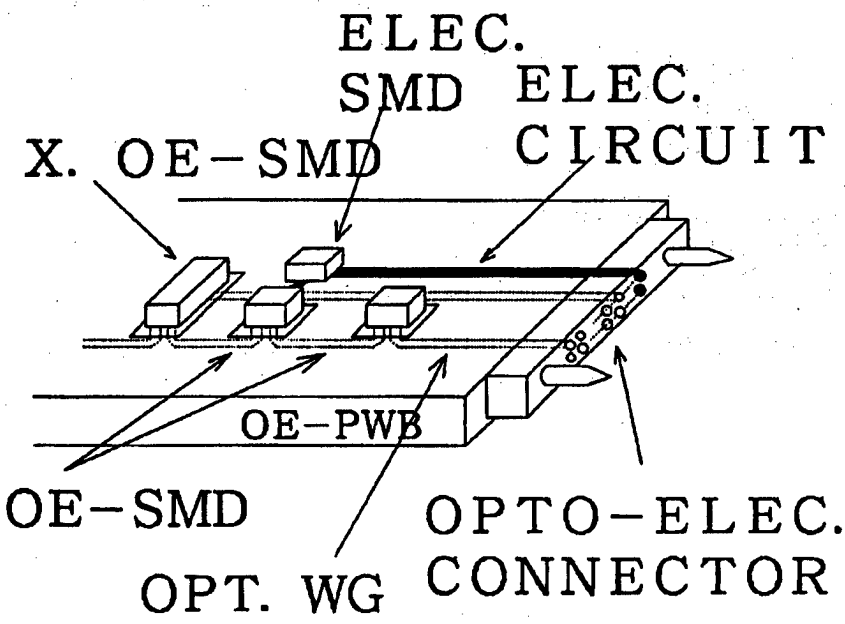
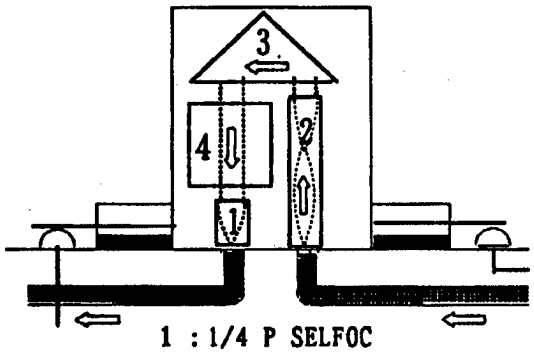


Figure 4. Basic Structure of Optical SMT



1 : 1/4 P SELFOC
2 : 3/4 P SELFOC
3 : Right angle prism
4 : Polarization independent optical isolator

Figure 5. Optical Isolator SMD

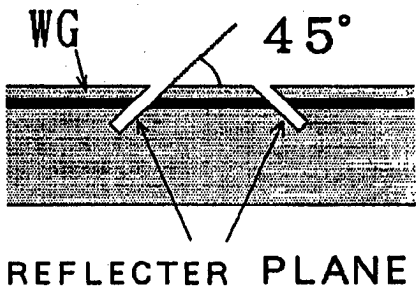


Figure 6. Turn-Up Reflector Made by Cutting Machine

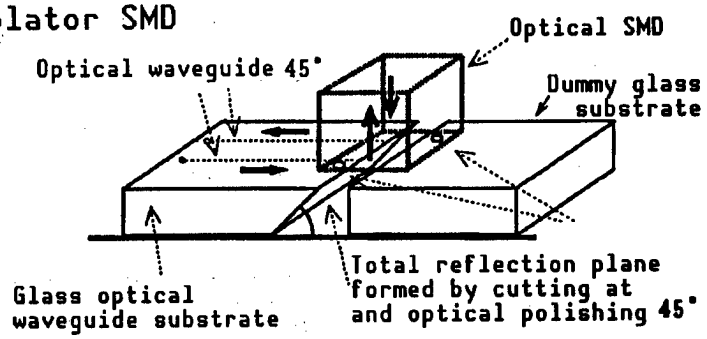


Figure 7. Mounting of Optical SMD on Glass Optical PWB

3. Other Types of Optical Interconnection

3.1 Stacked Optical Interconnection

When optical exchange, optical information processing, etc., make advances in the future, a configuration in which optical devices as shown in Figure 8 are aligned in cascade will be required. However, in the case of stacked transparent types, problems such as reflection, loss, optical axis adjustment will become obstacles. Moreover, when a doubly refractive medium is involved, it will become very expensive. Research on holographic memory in the latter half of the 1960s failed because of these obstacles. A device of stacked optical regeneration type (optical regeneration is carried out in each layer) will alleviate the above-mentioned problems. Needless to say, optically guided interconnection is preferred to spatial interconnection.

3.2 Planar Reflection Type

Use of a planar reflection substrate, as shown in Figure 9, for example, is proposed for a mother board.[9,10] However, when surface influence, optical path deviation due to substrate deformation, increase of background noise in the substrate due to increase in the number of optical signals, etc., are considered, this type seems to be applicable only when the number of optical interconnections is small.

3.3 Stacked Reflection Type

The type shown in Figure 10[11] may be thought basically the same as the planar reflection type, though certain improvement is visible. The reader is referred to many special issues on optical interconnection.[12]

4. Conclusion

Many cases have been seen in recent years including the case of optical interconnection, in which an increase in productivity demands a heterogeneous technology. In mount technology, in particular, concurrent engineering, which simultaneously advances research in the enhancement of performance and pursuit of production technology is indispensable. It is believed that the key to the practical application is the establishment of a technology that has excellent consistency with the existing production process, especially cost-effectiveness, which maximally excludes manual intervention.

In the above, the author has presented his personal judgment and prejudice. However, he expects that a practical optical mount technology will be developed.

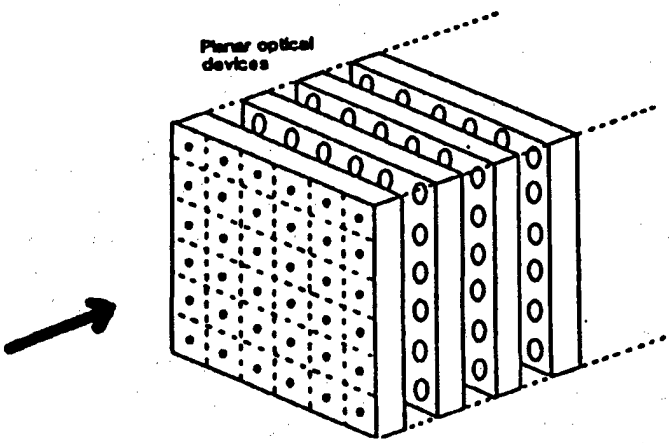
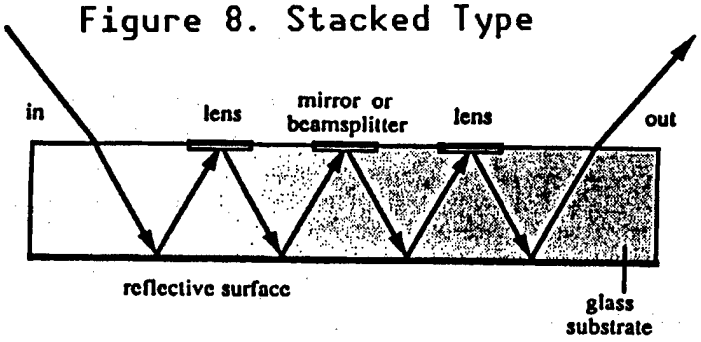
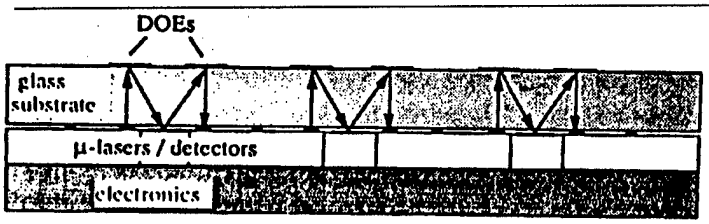


Figure 8. Stacked Type

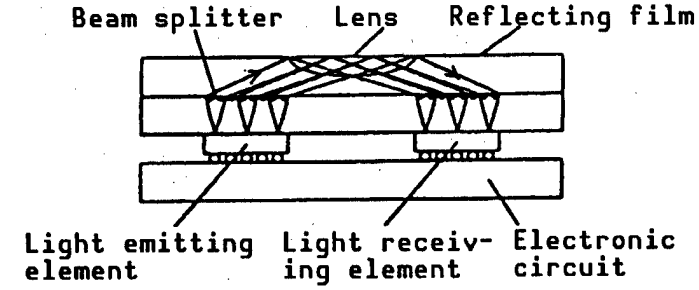


Planar optical 4f-imaging system.



Integration of planar optics and with microlasers and electronics (DOE: diffractive optical element).

Figure 9. Planar Reflection Type[9,10]



Configuration of stacked reflection module

Figure 10. Planar Stacked Type[11]

[Biography] Teiji Uchida

Education:

Graduated from Department of Electrical Engineering, Faculty of Engineering, Tokyo University, 1954.

Studied at Graduate School, Department of Science, Grenoble University, France, 1960.

Awarded Ingenieur-Docteur, Grenoble University, 1962; Awarded Doctor of Engineering, Tokyo University, 1967.

Employment:

NEC, 1954, R&D on wideband microwave communications.

Invited by French government to study as an engineering student, 1960.

Appointed director, Laser Device Development Headquarters, NEC, 1976; concurrently appointed director, newly-established Optoelectronics Laboratory, 1980.

Appointed professor, Development Technology Research Laboratory, Tokai University, 1988.

Research:

Clarification of mode synchronization phenomenon of lasers, 1964-67
R&D of Selfoc optical fiber and proposals of microoptics concept, 1968-75
Accomplishment in management of R&D of optical fiber communications and optical devices, 1975-80
Contributed as chairman or vice chairman on Japanese part of international conferences of CLEA, CLEO, IQEC, IOOC, OEC, MOC, etc., and proposed optical surface mount technology (SMT), 1980-91.

Awards:

1973 Achievement Award of Institute of Electrical Communications Engineers of Japan
First Microoptics Award at MOC '89 in Tokyo, 1989.

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5. Kawachi, M., et al., ELECTRON. LETT., Vol 19, 1983, pp 583-584.

6. Miyakawa, et al., 1992 Fall Meeting of Institute of Electronics Information Communication Engineers of Japan, C-213.

7. Uchida, T., et al., JJAP, Vol 31, May 1992, Part 1, No. 5B, pp 1652-1655; Meeting of Institute of Electronics Information Communication Engineers Japan, Fall 1990, C-189/Spring 1991, C-283/Fall 1001, C-158/Spring 1992, C-270/Fall 1992, C-214/to be presented in spring 1993.

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9. Jahans, J., et al., OC'90 (Optical Computing), 10B4.

10. Parker, J.W., PS'91, (Photonic Switching), WC1-3.

11. Kawai, et al., 1992 Spring Meeting of Institute of Electronics Information Communication Engineers, Japan, SC-3-6.

12. Special issues on optical interconnection: Japan Soc. Appl. Phys., Opt. Soc. Japan: Special Seminar on Microoptics IX, May 1992; Optical Industry Technology Foundation: U-OEIC Forum Report, May 1992; TECHNICAL REPORT OF INSTITUTE OF ELECTRONIC INFORMATION COMMUNICATION ENGINEERS, JAPAN, Vol J75-C-1, No 5, May 1992; OPTOELECTRONICS, June 1992, pp 55-106; and J. JAPAN ASSOCIATION OF APPLIED PHYSICS, Vol 62, January 1993, pp 2-9.

Trends of OEIC/Optical Interconnection From Patents Viewpoint

936C1034F Tokyo HIKARI SANGYO GIJUTSU SHINKO KYOKAI in Japanese Mar 93 pp 41-42c

[Article by Kusuyata Shimamoto, director, Shimamoto International Patent Office]

[Text] 1. Trends in OEIC/optical interconnection patent applications

2. Trends in field of optical interconnection patent applications

3. Trends in optical interconnection patent applications by foreign enterprises

4. Trends in optical interconnection patent applications by Japanese enterprises

5. Problems in optical interconnection as seen through patent applications

[Biography] Kusuyata Shimamoto

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Home Address: 508 Asahi Toranomon Mansion, 3-18-6 Toranomon, Minato-ku, Tokyo 105.

Graduated from Department of Fine Arts, Tokyo Fine Arts and Music University, 1956.

Employed by Patent Office as examiner, 1956.
Resigned from adjudicator, Patent Office, 1973.
Independent patent attorney, 1972-1979.
Director, Japan Science Promotion Foundation, 1979.

Table 1. Optical Computational Devices (Neurocomputers) (G06E1/00~3/00)

Order	Name of enterprise	1990	1991	1992	Total
1	NTT	16	13	10	39
2	NEC	10	16	3	29
3	Ricoh	6	8	12	26
4	Sanyo Electric	9	6	6	21
5	Sumitomo Cement	1	8	6	15
6	Nippon Sheet Glass	1	3	9	13
7	Matsushita Electric Industrial	2	3	7	12
8	Hitachi	2	2	3	7
9	Hamamatsu Photonics	1	3	3	7
10	Seiko Electric Industry	1	1	5	7
11	Fujitsu	2	4		6
12	AT&T	1	3	1	5
13	Hughes Aircraft		3	1	4
14	Canon			4	4
15	Boeing	3	1		4
16	JVC	1	1	1	3
17	STC		3		3
18	Sharp			2	2
19	Olympus Optical		1	1	2
20	Toshiba			2	2
Other Japanese enterprises		1	4	3	8
Other foreign enterprises		5	2	3	10
Total		62	85	83	230
No. of participating enterprises		20	23	23	
Cumulative No. of participating enterprises			29	37	

Table 2. No. by Enterprise of Optical Logic Element Patents Laid Open (G02F3/00~3/02)

Order	Name of enterprise	1989~90	1991	1992	Total
1	NTT	55	32	35	122
2	NEC	65	21	9	95
3	Fujitsu	29	21	6	56
4	Ricoh	12	14	28	54
5	Matsushita Electric Industrial	6	14	23	43
6	Mitsubishi Electric	16	5	9	30
7	Sumitomo Cement	3	9	8	20
8	Hitachi	7	6	4	17
9	AT&T	9	4	2	15
10	Hamamatsu Photonics	6	7	1	14
11	British Telecommunications	10	1		11
12	Seiko Electronic Industrial	1	3	4	8
13	Optoelectronic Technology Research	3	4	1	8
14	Seiko Epson	6	2		8
15	Nippon Sheet Glass	2	2	3	7
16	Toshiba	3		3	6
17	Canon	4		2	6
18	NHK	3	3		6
19	AIST	2	1	1	4
20	Mitsui Toatsu Chemicals			3	3
Other Japanese enterprises		6	15	8	29
Other individuals		2			2
Other foreign enterprises		13	6	3	22
Total		266	172	158	596
No. of participating enterprises		52	32	27	
Cumulative No. of participating enterprises		38	51	60	

Table 3. No. by Technology of Light Guide Related Patents Laid Open (G02B6/00)

ID symbol		1989~90	1991	Total	1992
	Light guide	419	225	644	
301	Structure for guiding light	15	69	84	82
306	Filter	36	15	51	16
311	Attenuator	31	9	40	22
316	Isolator	2	7	9	9
321	Optical delay element	4	10	14	5
326	Light radiator	27	26	53	15
331	Illumination	61	65	126	
333		5	12	17	
334		2	11	13	
335			7	7	
336	Sealing/laying	100	83	183	
341	Sealing structure of fiber penetration part	18	5	23	
346	Laying of fiber to substrate	5	4	9	
351	Laying of cable	83	65	148	
356	Manufacturing method	387	125	512	
361	Manufacturing method of plastic clad fiber	3	4	7	
366	Manufacturing method of plastic fiber	73	33	106	
371	Manufacturing method of crystal fiber	28	8	36	
376	Material	83	45	128	
386	Material of plastic clad fiber	42	19	61	
391	Material of plastic fiber	133	43	176	
396	Material of crystal fiber	18	6	24	
Total		1,575	896	2,471	1,536 [sic]

Table 4. Electromagnetic Waves Other Than Radio Waves (Electrical transmission method using light) H04B10/00~10.24

Order	Name of enterprise	1992
1	NEC	159
2	Fujitsu	92
3	NTT	74
4	Matsushita Electric Industrial	67
5	Sony	55
6	Canon	51
7	Toshiba	45
8	Hitachi, Ltd.	36
9	Hitachi Cable	33
10	Mitsubishi Electric	32
11	Oki Electric Industrial	25
12	Sumitomo Electric Industries	23
13	Sharp	10
14	Matsushita Electric Works	10
15	Sanyo Electric	9
16	Shimadzu	7
17	Seiko Electric Industry	6
18	JVC	6
19	Furukawa Electric	5
20	Asahi Electronics Laboratory	5
Total		750

Table 5. Technologies Related to Optical Computation Device: No. of Patents Laid Open by Patent Classification

No. of inventors and relevant technology classifications

International patent classification	90	91	92	No. of inventors	No. of relevant technological classifications
G06E1-00	40	62	23		
1-02		1	4		
1-04	4	1	2		
1-06			4		
3-00	18	21	50		
Total	62	85	83		

Title of the invention Optical interconnection device

(21) Patent application number H1-277861

(22) Patent application date October 25, H1 (1989)

Inventor: Atsushi Ota, c/o Central Research Laboratory, Mitsubishi Electric Corp., 1-1,8-chome, Tsukaguchi-Honmachi, Amagasaki, Hyogo Prefecture
Inventor: Kazuo Kyuma, c/o Central Research Laboratory, Mitsubishi Electric Corp., 1-1,8-chome, Tsukaguchi-ahonmachin, Amagasaki, Hyogo Prefecture
Applicant: Mitsubishi Electric Corp. 2-3,2-chome, Marunouchi, Chiyoda-ku, Tokyo

Figure 1

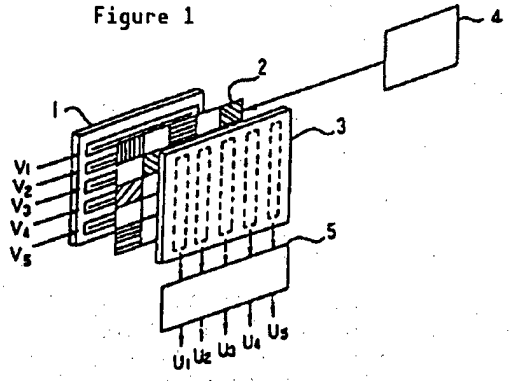
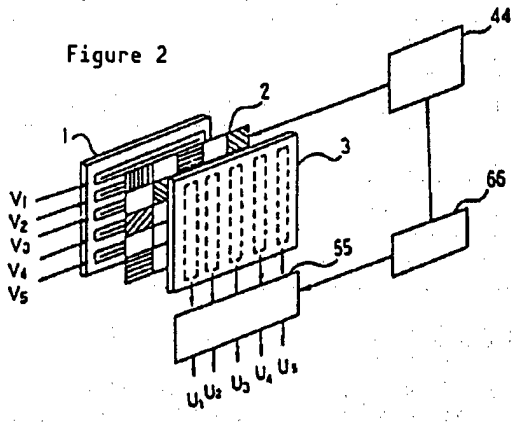
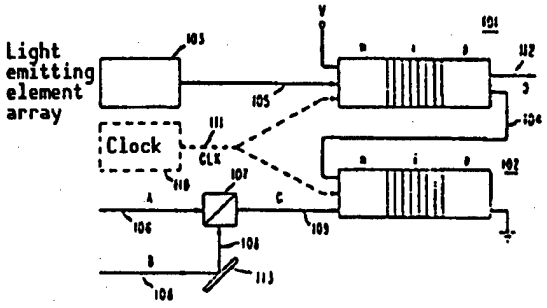


Figure 2



1: Light emitting element array
2: Spatial light receiving and modulating element
3: Light receiving element array
4: Frequency modulating means
5: Frequency discriminating means
44: Temporal receiving and modulating means
55: Time discriminating means
66: Clock

Patent Laid Open H3-18834



(AT&T)

Patent Laid Open H3-208012

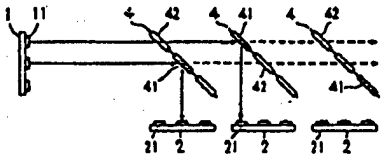
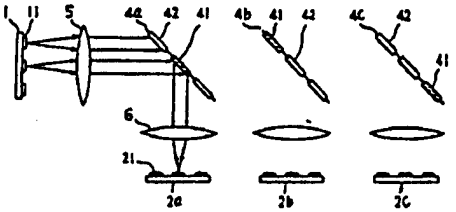
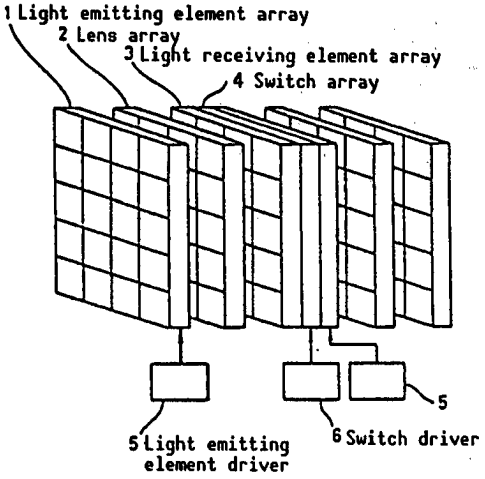


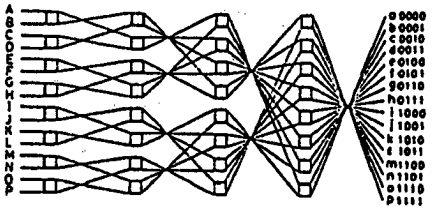
Diagram showing the principle of transmitting optical signal according to this invention



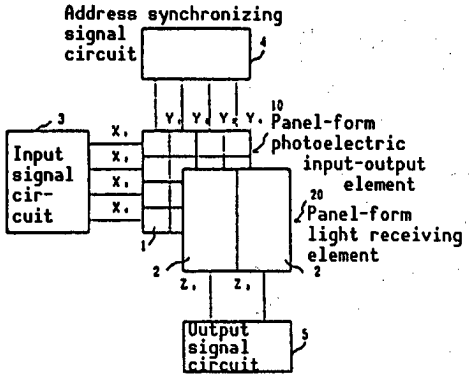
Schematic diagram showing modifications of light signal transmitting method according to this invention

Patent Laid Open H3-144612 (NEC)

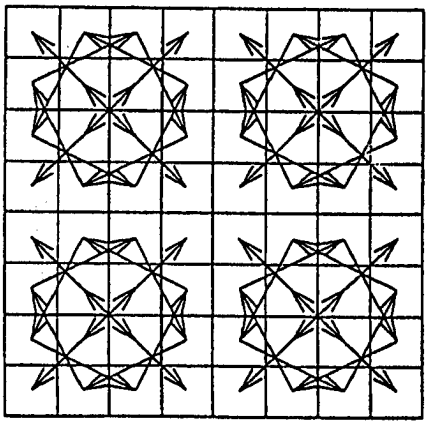




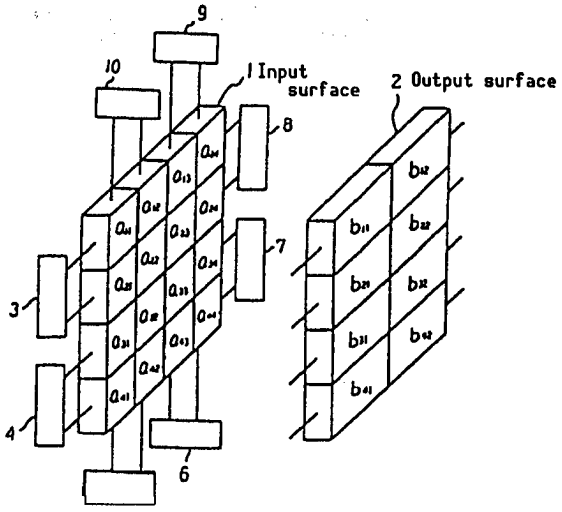
Patent Laid Open H3-94317 (NEC)



Patent Laid Open H2-266016 (NEC)



Patent Laid Open H3-244296 (NEC)



Optical Interconnection Technology Utilizing Space

936C1034G Tokyo HIKARI SANGYO GIJUTSU SHINKO KYOKAI in Japanese Mar 93
pp 43-48

[Article by Takao Matsumoto, NTT Transmission Systems Laboratories]

[Text] If one attempts to maximally utilize the potentiality of light in communication systems, then there is expected development of new optical technologies that make advantageous use of spatial characteristics of light such as 1) noninductiveness, 2) capability of realizing crossed connections; 3) capability of realizing collective connection of two-dimensional signals, etc. In recent years, hardware using multichannel and intricate connections exemplified by neural networks is being investigated in many laboratories, where optical technologies of the above-mentioned kinds will become important. This article will present an update and technical issues of optical interconnection ins pace, centered around the work of this author's group.

1. Application to Parallel Processing Systems

In optical interconnection in space within a parallel processing system, several hierarchies from within the chip to between the boards need to be considered. Judging from the problems involved in actual equipment and existing technical level, it seems appropriate to apply the technology first to interconnection between the boards. This author and his collaborators actually trial manufactured a parallel processing system to which is applied interboard, spatial, optical interconnection technology and evaluated the systems:

a. System of manual switching type (→ COSINE-I).
b. System of automatic switching type by liquid crystal optical switch (→ COSINE-II).
c. System of direct connection type to adjacent board (→ COSINE-III).

2. Adaptation to Node Processing Part of Communication Network

a. Cross Connection

In the communication network, a cross connection switch is used for path switching within a node. Along with the increase in operating speed of the communication network, a cross connection switch is required which

can deal with high-speed paths. Adaptation of spatial optical interconnection that facilitates high-speed and multichannel operation to this area can be considered. (→ Multichannel two-dimensional liquid crystal optical switch).

b. Multiple Access Network

At locations where optical signals are congested, as at the fiber branch point in the star-type LAN, it is possible to make the optical circuit small by adopting spatial optical interconnection. (→ MANDALA).

c. Neural Network for Signal Processing

For signal processing within a node such as the routing of packet signals, use of neural network can be considered for reaching high speed. Spatial optical interconnection may be utilized in order to solve the congestion problem of connections in a neural network. (→ Neuroutin).

3. Problems in the Realization of Optical Interconnection in Multidimensional Space

In spatial optical interconnection, multidimensional optical circuits play an important role. In discussing future two- and three-dimensional optical circuits, the following items need to be considered:

a. Type and technical problems of multidimensional optical circuits.
b. Method for realization of multidimensional optical circuits.
c. Fusion of light and electricity.

[Biography] Takao Matsumoto

Graduated from Faculty of Engineering, Osaka University, 1972.

Completed masters' course, Faculty of Engineering, Osaka University, 1974.

Employed by NTT, 1974. Assigned to Yokosuka Electrotechnical Laboratory.

Received Achievement Award from Institute of Electrical Communications Engineers of Japan, 1980

Awarded Doctor of Engineering, 1980.

Assigned to NTT First Laboratory of Communication Networks, 1985; reassigned to NTT Transmission Systems Laboratories, 1987.

Received Best Paper Award of IEEE ICCD'90, 1990.

Currently researching optical signal processing technology.

Member, Papers Committee, Electronic Information and Communication Engineers of Japan.

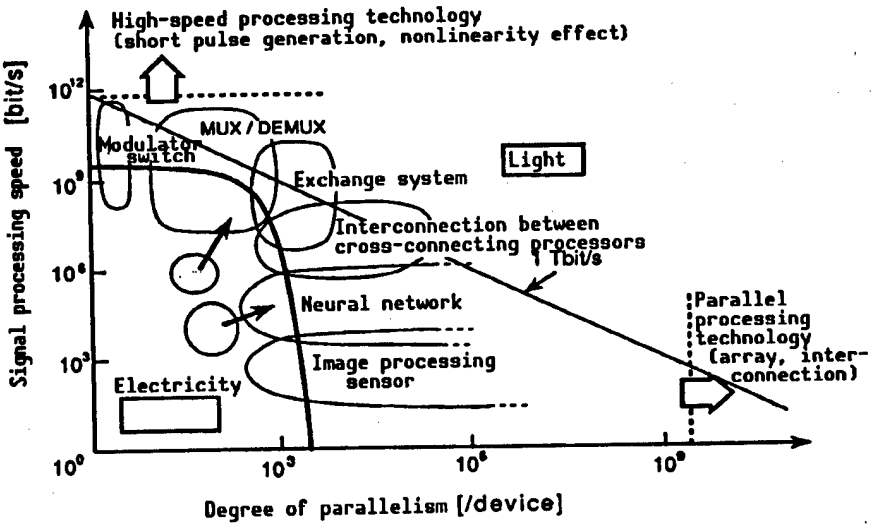


Figure 1. Potentiality of Light Signal Processing Technology

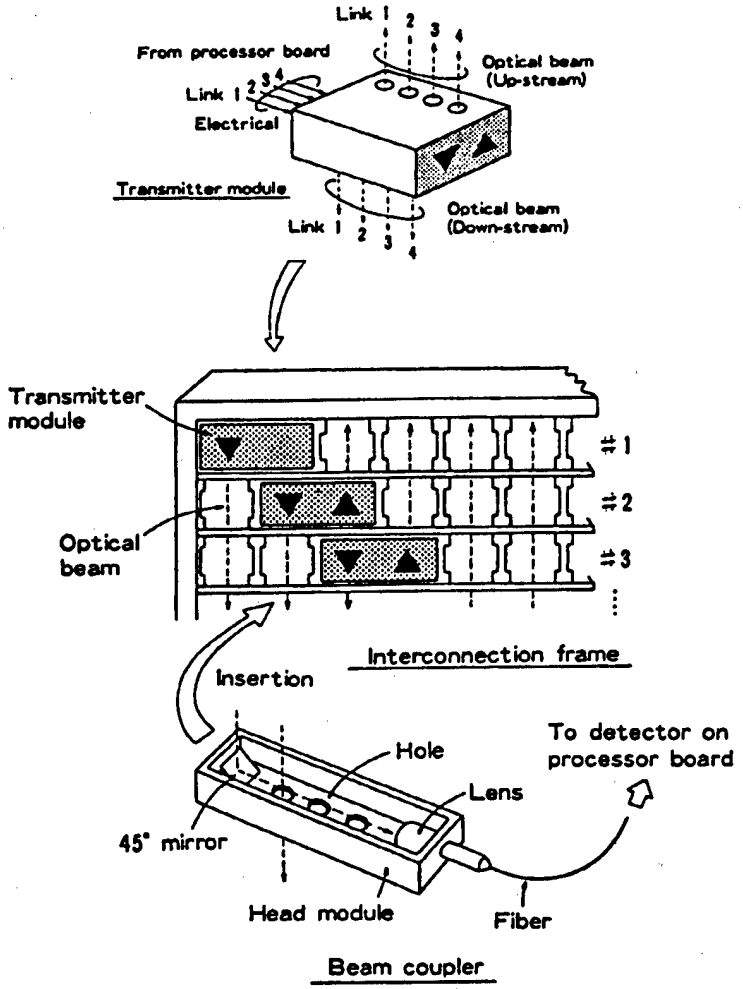


Figure 2. Structure of Optical Interconnection Part in COSINE-I

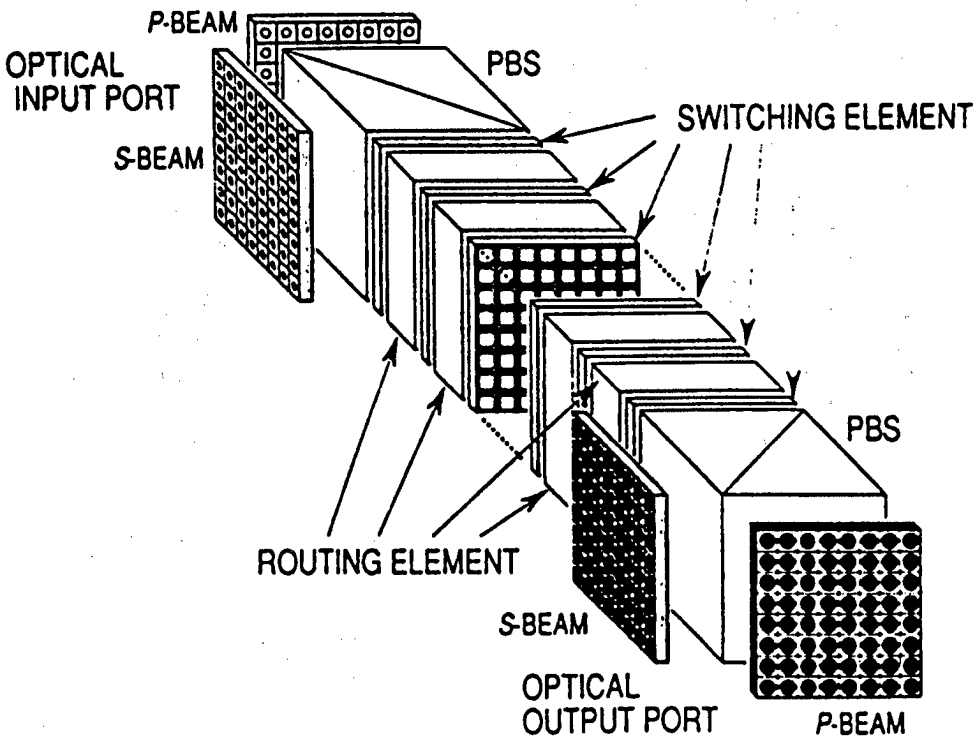


Figure 3. 128-Channel Two-Dimensional Array Type Spatial Optical Switch

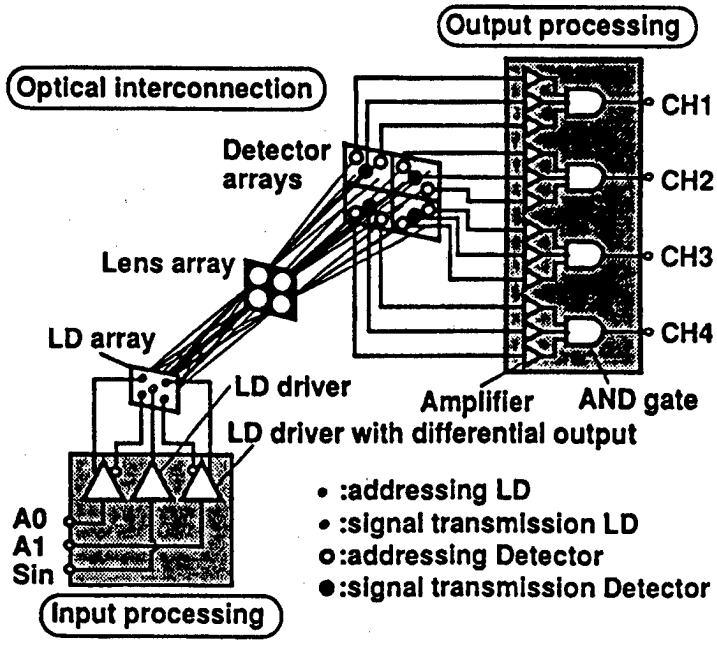


Figure 4. Optical Interconnection Utilizing Array Elements (LISA)

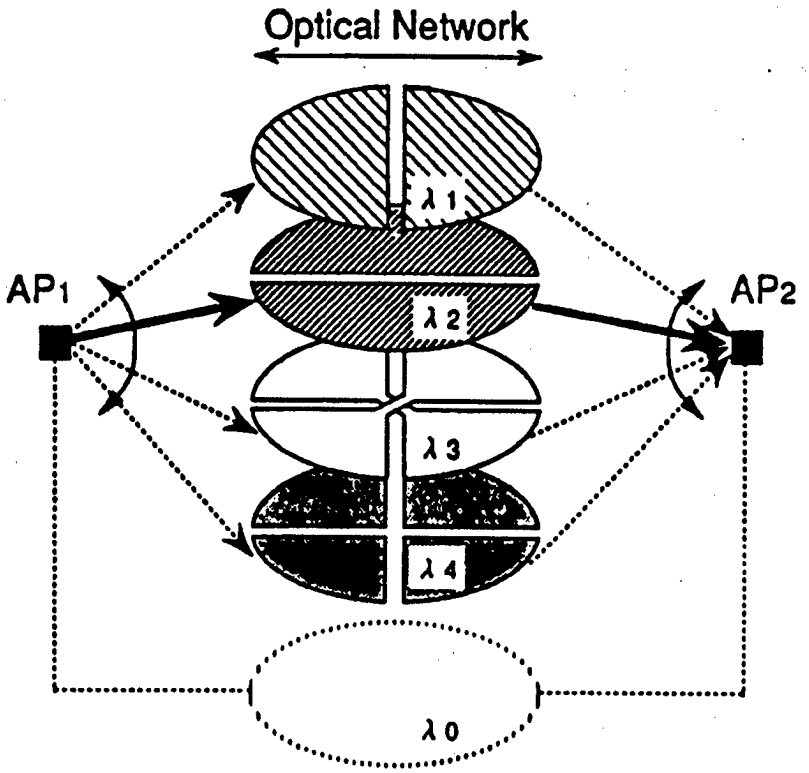


Figure 5. Conceptual Diagram for MANDALA (N = 4)

Table 1. Modes and Technical Problems of Multi-dimensional Optical Circuits

Mode of optical circuit	Technical problem			
	Rendering wide band, high sensitivity, high output, and low noise	Rendering low crosstalk, multichannel, high density, uniform characteristic	Realization of surface input/output and elimination of interconnection width with outside	Elimination of internal interconnection width and heat radiation
0-dimensional single body	◄►			
1-dimensional	◄►	◄►		
2-dimensional	◄►	◄►	◄►	
3-dimensional	◄►	◄►	◄►	◄►

Table 2. Development of Spatial Optical Interconnection

Generation	Kind of interconnection	Use
First generation	Parallel interconnection	Point-to-point signal transmission
Second generation	Distributed interconnection	Clock distribution, signal distribution
Third generation	Selective interconnection	Routing, bus

Table 3. Comparison Between Electricity and Light for Realizing Multi-dimensional Optical Circuit

Comparison item		Electricity	Light
Potentiality	Band	o	●
	Speed	o	●
	Reflection	Δ	o
	Induction	Δ	●
	Processing function	●	Δ
Realization of system/ device	Making circuit small	o	Δ
	Collectivity of interconnections	Δ	o
	Necessity for additional circuit (photoelectric and impedance conversion)	o	Δ
Utility	Mass productivity	●	x
	Stability	●	Δ
	Maturity of technology	●	Δ
	Weight	Δ	o

●: Especially excellent
o: Relatively excellent
Δ: Relatively poor
x: Especially poor

References

1. Matsumoto, T., Sakano, T., Noguchi, K., and Sawabe, T., "Computer Systems Employing Reconfigurable Board-to-Board Free-Space Optical Interconnections: COSINE-1 and -3," Proc. ICCD'90, 1990, pp 426-429.

2. Sakano, Noguchi, and Matsumoto, "Three-Dimensional Processor Array COSINE-III Utilizing Interboard Spatial Optical Interconnection," scheduled for presentation 1993 spring meeting of Institute of Communication Engineers of Japan.

3. Noguchi, K., Sakano, T., and Matsumoto, T., "A Rearrangeable Multichannel Free-Space Optical Switch Based on Multistage Network Configuration," IEEE J. OF LT, Vol 9 No 12, 1991, pp 1726-1732.

4. Sakano, T., Noguchi, K., and Matsumoto, T., "Novel Free-Space Optical Interconnection Architecture Employing Array Devices," ELECTRON. LETT., Vol 27 No 6, 1991, pp 515-516.

5. Matsumoto, "Multiple Access Optical Network Architecture: MANDALA," Tech. Reports of Inst. of Commun. Engineers, Japan, OCS92-77, 1993-02.

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Microoptics, Optical Interconnection

936C1034H Tokyo HIKARI SANGYO GIJUTSU SHINKO KYOKAI in Japanese Mar 93 pp 49-55

[Article by Kenjiro Hamanaka, Tsukuba Laboratory, Nippon Sheet Glass Co., Ltd.]

[Text] **Introduction**

In an attempt to achieve an optical system using various optical functional elements such as surface emitting laser and SLM, an important task is how to combine these active elements with passive elements such as microlens arrays and HOE to obtain a module. In this publication, centered around our work and from the standpoint of the microoptical element, we will discuss optical device technology and integrated packaging technology necessary for achieving free-space optical interconnection by imagining the execution of optical computation and large-scale optical exchange through the complicated interconnection of two-dimensional pattern information.

1. Stacked Optical System

A free-space optical system has difficult problems such as 1) precise alignment adjustment of six axes—x, y, z, θx, θy, θz—for each component of the optical system; 2) down-sizing; 3) securing reliability against temperature change, vibrations, etc.; and 4) automation for assembling individual components. Stacked integration of optical components is effective as a means of solving these problems, and for this purpose, a distributed index of a refraction-type lens with flat surfaces is suitable.[1] In that case, to achieve optical interconnection between two-dimensional patterns, there is a method of achieving this by means of a microlens array and carrying it out by using one lens. Which one is preferable is decided according to the system configuration and the specifications of the device employed. For the former, a planar microlens (PML)[1,2] is effective, while for the latter, optical bus interconnection system (OBIS),[3] which uses selfoc microlenses (SMLs), is expected to be useful. Discussion of the features of each will follow.

2. Planar Microlens

For connection between fiber arrays or between a fiber array and a light-emitting and -receiving element, the parallel optical interconnection, which uses PML for each channel, is effective. PMLs are manufactured by the combination of photolithography and ion exchange technology and provide a high precision alignment with optical semiconductor element array. Optical interconnection using a lens array is a configuration suitable for large-scale parallel execution of optical interconnection for each pixel or for carrying out connection and arithmetic between adjacent pixels.

3. Integrated Optical System OBIS

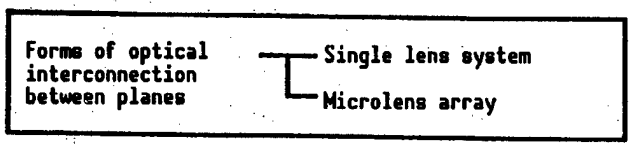
On the other hand, for the insertion of prisms between planes or for connection with distant pixels, optical interconnection for every pixel using lens array results in limitation of the pixel on the in-plane level of integration due to the influence of diffraction. In such a case, image formation of a two-dimensional pattern by means of one lens gives rise to a larger effective numerical analysis (NA) and is often advantageous in raising the level of integration. However, its realization needs an appropriate packaging technology, which integrates a bulky optical system. We proposed the integrated optical system OBIS as one such method.[3] An optical mother board with multiple stages of unmagnified conjugate imaging planes is manufactured using SMLs, and the optical device is inserted and fixed in conformity with the shape of the groove between SMLs. The alignment adjustment is reduced to that for three axes within the plane so that it is possible to construct a compact stabilized optical system. In addition, for the refractive element (SML), it is possible to make the aberration low over the wider image plane compared with DOE and to obtain a larger space bandwidth product. It is possible to increase separation between the planes while maintaining stability of the structure and apply the technology to complicated interconnection that includes connection to distant pixels.

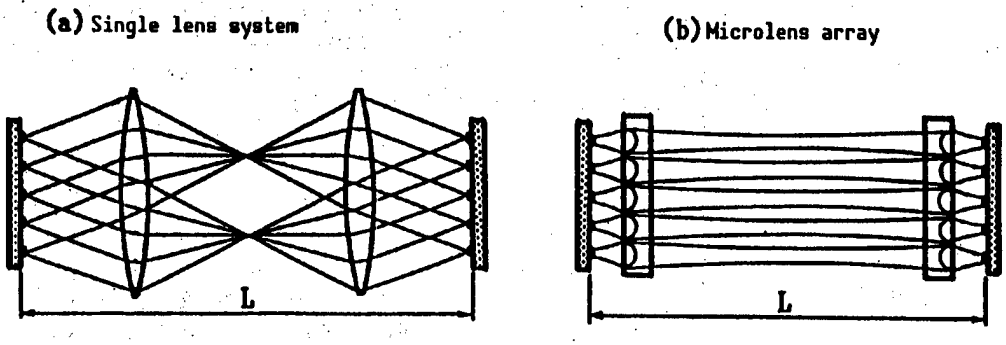
[Biography] Kenjiro Hamanaka

Graduated from Department of Science, Gakishuin University, 1981.

Employed by Nippon Sheet Glass Co., Ltd.; assigned to Tsukuba Laboratory, 1987.

Received Best Paper Award at Microoptics Conference (Japan Society of Applied Physics), 1991.



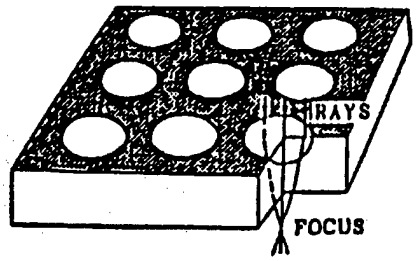


Comparison of features

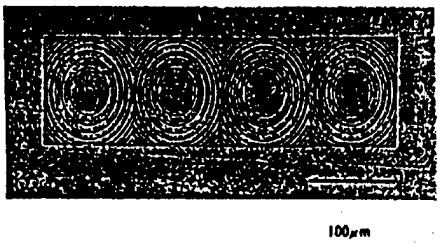
Large	Comparison of features	Small
Large	Distance between planes	Small
Off-axis aberration of lens	Dominant factor of resolving power	Diffraction and spherical aberration of lens
Somewhat lax	Tolerance for positional deviation	Severe
Large	Base bandwidth product	Small
Dense arrays	Smart pixel	Dilute arrays
Interconnection to distant pixel possible	Interconnectability	1:1 connection to proximity pixel
Depends on NA of lens	Light utilization efficiency	Depends on NA of lens
Basically nonexistent	Crosstalk between pixels	Needs to be investigated
Needs to be considered	Angular dependence of inserted element	No need to consider
No difference in principle	Possibility of integration	No difference in principle

Forms of imaging element
- Refractive optical elements
- Diffractive optical elements

(a) ROE



(b) DOE

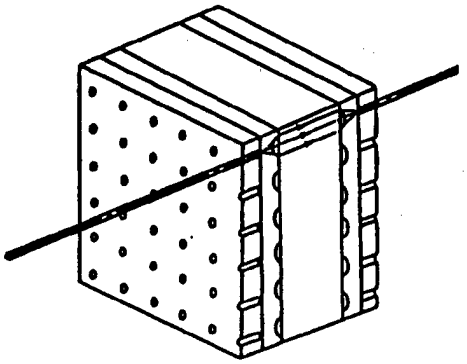


Comparison of features

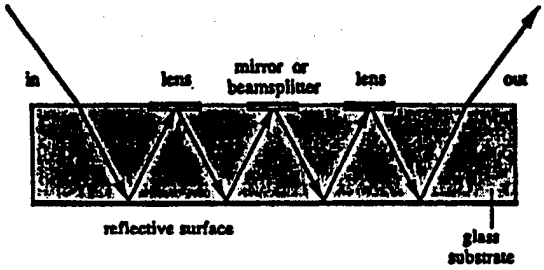
Molding, ion exchange and photolithography	Product technology	Photolithography and molding
Difficult	Rendering aberration free	Easy for a single point
Possible to reduce	Off-axis aberration	Large
Somewhat lax	Width of allowable positional deviation	Severe
Small	Wavelength dependence	Large
100%	Light utilization efficiency	70~90%
Small	Noise of stray light	Needs to be considered
Basically imaging alone	Additional function	High degree of freedom
No difference in principle	Possibility of integration	No difference in principle

Forms of integration
- Stacked planar optics
- Planar optics

(a) Stacked planar optics



(b) Planar optics

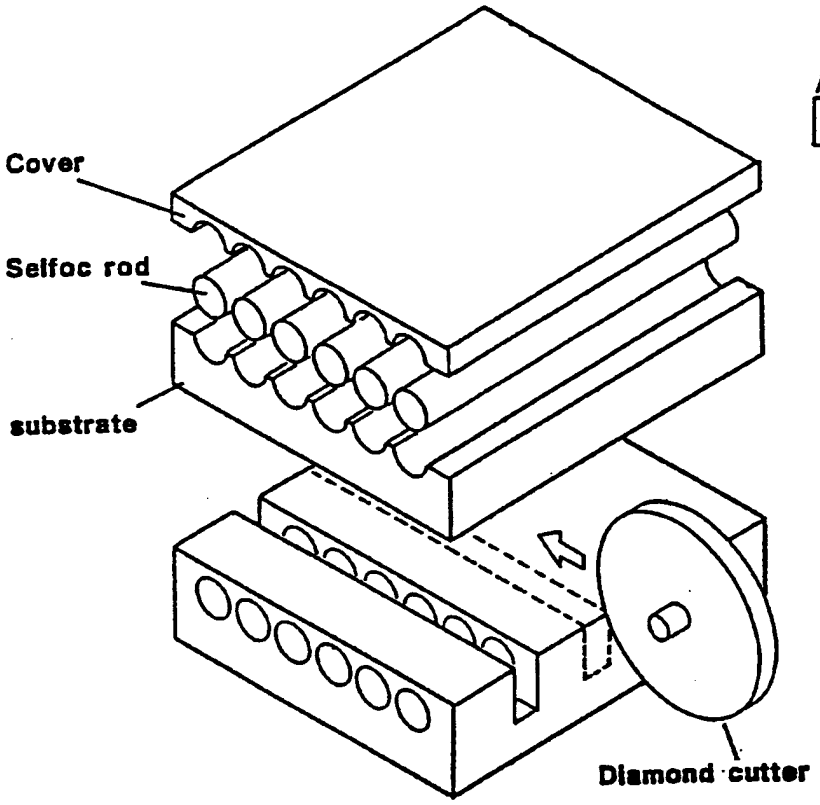


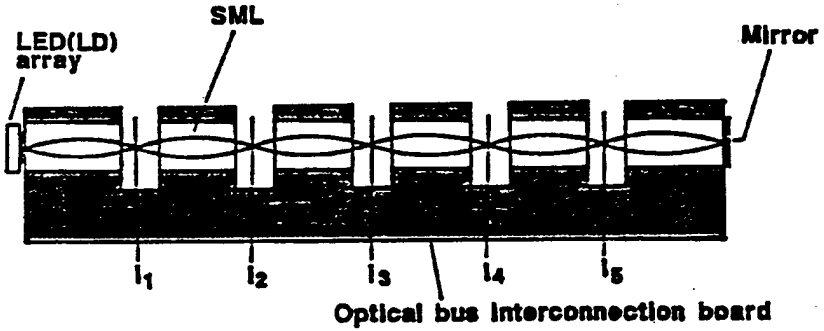
Comparison of features

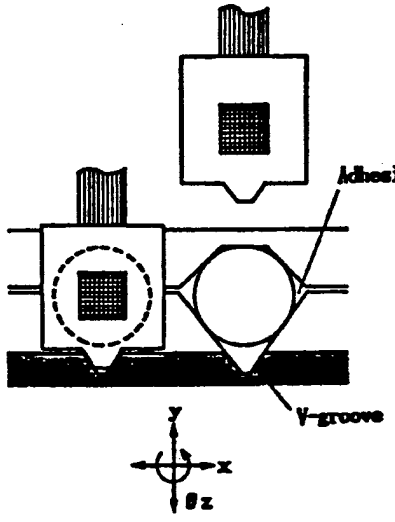
Bonding, photolithography	Product technology	Photolithography
Needs other technologies	Consistency with semiconductor manufacturing process	Good
General spherical lens	Lens design	Need to impart astigmatism
Somewhat lax	Tolerance for errors in lens manufacture	Severe
Somewhat lax	Tolerance for wavelength variation	Severe
Basically required	Positional adjustment between parts	Carried out only collectively
Somewhat lax	Required precision for substrate	Severe
Could be improved	Resolving power	Difficult to improve

Optical bus interconnection system using SMLs

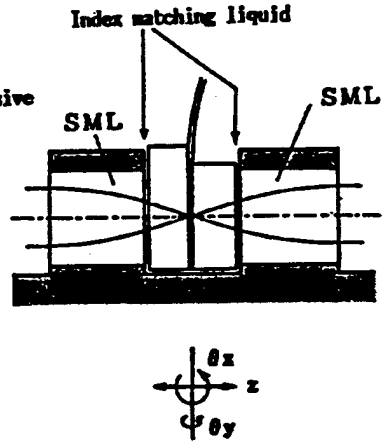
NSG
NIPPON SHEET GLASS







Alignment on x, y, and θz can be neglected by using V-groove.



Alignment on z, θx and θy can be neglected by contacting SML facets.

Approach to NSG

"Manufacture of Refractive Index Distributed Type Microlens Array by Ion Exchange Method"

1. Microlens array x Refractive optical elements x Stacked integration

   = Planar microlens

2. Single lens system x Refractive optical elements x Stacked integration

   = Optical interconnection board using selfoc lenses

References

1. Iga, K., et al., APPL. OPT., Vol 21, 1982, p 3456.
2. Oikawa, M., et al., APPL. OPT., Vol 29, 1990, p 4064.
3. Hamanaka, K., JPN. J. APPL. PHYS., Vol 31, 1992, p 1656.

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