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THAAD HARDWARE-IN-THE-LOOP SIGNAL INJECTION HARDWARE TECHNICAL DESCRIPTION

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13. ABSTRACT *(Maximum 200 Words)*

This report provides background information on the Theater High Altitude Air Defense (THAAD) Missile System and a technical description of a signal injection card built for the THAAD Hardware-in-the-Loop (HWIL) Missile Simulation located in the Imaging Infrared System Simulation 2 (IRSS2) Facility of U.S. Army Aviation and Missile Command's (USAMCOM's) Advanced Simulation Center (ASC). The Signal Injection Card gives the THAAD HWIL missile simulation the capability to test the missile's Integrated Avionics Package (IAP) in a closed loop HWIL IAP-only missile simulation with a simulated Infrared (IR) seeker. Schematics and timing diagrams are included to aid in the technical description of the signal injection card.

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I. INTRODUCTION

In order to properly test the Theater High Altitude Air Defense (THAAD) missile's flight computer, referred to as the Integrated Avionics Package (IAP) hereafter, in a closed-loop Hardware-in-the-Loop (HWIL) missile simulation scenario it was necessary to fabricate and integrate an interface between the IAP and Infrared (IR) seeker for digital signal injection in the IAP-only HWIL missile simulation configuration. The signal injection interface would combine video signals generated from the dynamic and real-time Infrared Scene Generator (IRSG) Digital Video Interface's (DVI) interface (DVII) and status information from the Camera Emulator card located in the THAAD missile interface equipment rack (IER) and transmit this information to the THAAD Camera Monitor card in the IER. The Camera Monitor card would then pass this video and status data to the IAP via the IAP-to-IR seeker connector for closed loop HWIL IAP-only missile simulations in lieu of the THAAD IR seeker. The following two sections provide background information on the THAAD system and the THAAD I^2RSS2 HWIL missile simulation. A technical description of the signal injection interface using schematics and logic diagrams to explain its operation begins with Section IV.

II. THAAD System Description

The THAAD system makes up the upper tier of a two-tiered ground-based defense system against Theater Ballistic Missile (TBM) threats. THAAD provides broad surveillance and a large engagement capability, as part of the upper-tier portion of the multi-tiered TMD system. This provides the ability to defend against threats to wide areas, dispersed assets, and strategic assets (e.g. population centers, industrial facilities, and critical military assets).

THAAD engages at high altitudes to minimize damage caused by debris and chemical or nuclear munitions. The combination of high altitude and long-range intercept capability often provides multiple engagement (shoot-look-shoot) opportunities. The system is inter-operable with other U. S. Air Defense (AD) systems.

THAAD contains four major segments: i.e., the missile, the launcher, the THAAD radar, and BMC3I, as well as the system transportation. The THAAD Project Office (TPO) manages the four segments' development, while the system transportation is considered GFE. The fighting element will be the THAAD battery consisting of one BMC3I unit, 1 radar, 9 launchers, and 150 missile rounds. The batteries are organized into battalions. A battalion consists of four firing batteries and a headquarters battery.

A. BMC3I

The THAAD BMC3I segment has two primary functions: (1) it interfaces with external sensors and air defense systems to ensure effective, multi-tier air defense and (2) it provides connectivity between each of the THAAD segments.

At the firing battery level, the BMC3I segment consists of a Tactical Operations Center (TOC), two Launcher Control Stations (LCS) functioning as communications relays to remote sites, and a Sensor System Interface (SSI), which receives and preprocesses THAAD radar data from a remotely placed THAAD radar. A second option for radar deployment is collocation

with the BMC3I TOC shelters. The THAAD radar is connected to the THAAD BMC3I elements by dual optical fiber cables for mission data transfer to the TOC or SSI shelters. The TOC can control up to 18 THAAD launchers.

The THAAD firing battery has the capability for dispersed deployment operations on the battlefield to enhance weapon system survivability. For example, a TOC and collocated THAAD radar can be connected by optical fiber cables over a distance of up to 2 km. In addition to fiber-optic communications, the Tactical Operations Station (TOS) has Radio Frequency (RF) back-up capability. The path lengths for the netted/distributed communication links for TOS-to-launcher, TOS-to-LCS, LCS-to-launcher, and TOS-to-SSI communications are each limited to a maximum line-of-sight distance of 25km.

The THAAD system will interact with four groups of external systems: (1) Allied and Joint systems, including JTIDS-equipped aircraft, Tactical Air Control Systems (TACS), and Tactical Air Operations Center (TAOC), (2) Early Warning/Intelligence systems, including Airborne Warning and Control System (AWACS), Joint Surveillance Tracking and Acquisition Radar System (JSTARS), and Tactical Exploitation of National Capabilities (TENCAP), (3) Intra-Army systems, such as Corps SAM and Patriot, and (4) support systems, like Global Positioning System (GPS) and the Integrated Meteorological system (METS).

B. RADAR

The THAAD Radar is the primary sensor. It uses state-of-the-art radar technology to provide theater-wide surveillance, discrimination, and fire control for the weapon system. It has a mobile, single-faced, phased-array radar utilizing solid state transmit/receive modules. It has a separate power generation unit in addition to system cooling and electronic equipment control units.

The THAAD radar operates in X-band and provides early warning of threat TBM launches by detecting and acquiring targets at very long-ranges using autonomous horizon fence and volume search acquisition modes. The THAAD radar provides the update information to the THAAD missile for threat engagement and intercept. Additional functions performed by the THAAD radar include discrimination, target tracking, interceptor in-flight updates, and fire control. The radar provides the critical data to BMC3I that allows the THAAD system to perform kill assessments, to commit additional interceptors, or cue lower tier systems, such as Patriot and other TMD elements such as Corps SAM.

C. Launcher

The THAAD launcher contains a missile-round palletized loading system and electrical and electronic systems. The palletized loading system is based on the Army model M1075 truck. It provides transport, load handling, emplacement, launch, and reload capabilities for the THAAD missiles.

Lead acid batteries that are recharged by generator supply primary power for the system. Launch position is determined from global positioning system, which provides launch azimuth by a direction reference unit.

D. System Transportation

The THAAD weapon system is highly mobile, using standard Heavy Equipment Mobile Tactical Truck (HEMTT) prime movers for the radar, the Palletized Load System (PLS) truck for the launcher, and the High Mobility Multipurpose Wheeled Vehicles (HMMWV) for BMC3I elements. The weapon system is deployable to a theater of operations using a combination of C-130 and C-141 transport aircraft.

E. User Operational Evaluated System (UOES)

The THAAD Program will deliver a functional, developmental prototype system at the end of Dem/Val phase. Referred to as the THAAD UOES, this system will consist of 40 missiles with launchers, 2 BMC3I units, 2 THAAD raders, and associated support equipment. The THAAD UOES supports early operational assessment prior to entering EMD. It also satisfies the need for providing, in case of national emergency, a deployable prototype system by the mid-1990s in accordance with the Missile Defense Act of 1991.

F. Missile

The THAAD missile is a single-stage, solid-fueled missile. It has a strong, lightweight graphite-epoxy canister; a single-stage, solid-fueled booster, and a Kill Vehicle (KV) with a Mid-Wave Infrared (MWIR) passive homing seeker, an uncooled sapphire window, and an IAP.

The missile employs Thrust Vector Control (TVC) technology and Divert and Attitude Control Systems (DACS). Predicted intercept point and guidance presets are provided by the THAAD radar to the missile before launch. The missile receives in-flight updates, including a Target-Object-Map (TOM) for target designation and in-flight updates from the THAAD radar.

Terminal guidance data are provided by the IR seeker looking through the forward-mounted, uncooled window, which is protected by a shroud that separates prior to target acquisition by the seeker. The KV exhibits enhanced lethality by destroying incoming warheads using kinetic energy impact Hit-to-Kill (HTK).

III. THAAD HWIL Missile Simulation

The THAAD HWIL missile simulation is located in the Imaging Infrared System Simulation 2 (I^2RSS2) facility of U.S. Army Aviation and Missile Command (USAAMCOM) Missile Research, Development, and Engineering Center (MRDEC) Advanced Simulation Center (ASC) (Fig. 1). The I^2RSS2 HWIL facility provides a means of exercising the THAAD key missile guidance and control hardware and software (i.e. IR seeker and IAP) in simulated, real-time, and closed-looped flight, where the missile sensors are provided with input signals which make the THAAD system behave as though it were in actual operation. As a result, real-time THAAD HWIL simulations are made in repetitive, large volume run sets to evaluate missile performance against a variety of input sources and threats using deterministic and/or Monte Carlo techniques for statistical hit-point calculations. High performance real-time computers are used model the THAAD radar, launcher, and BMC4I segments and to control the target and countermeasure signatures and battlefield scenarios. The dynamic IRSG and Laser Diode Array Projector (LDAP) are used to provide real-time digital IR scenes via signal injection into the IAP flight computer or in-band radiated IR projected scenes into the IR seeker and onto IR detectors at the required THAAD frame rates, frame size, and resolution. THAAD Missile flight dynamics, responding to the commands issued by the IAP's guidance and control system hardware/software, are simulated in real-time to determine the missile trajectory, to calculate target intercept conditions, and assess interceptor-to-target hit-point accuracy and lethality. In addition, the I^2RSS HWIL facility is equipped with several other key HWIL subsystems: a 3 or 5-Degree-of-Freedom (DOF) Flight Motion Simulator (FMS), high performance real-time multiprocessor simulation computers for simulation facility control and missile/target dynamic motion 6-DOF simulation, environmental modeling computers, software, and databases, and real-time data collection, visualization, and analysis computers.

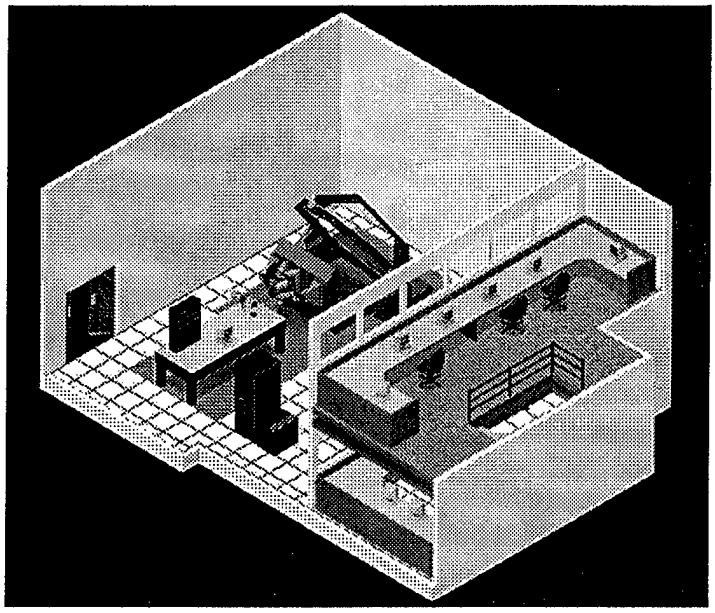


Figure 1. USAMCOM MRDEC Imaging Infrared Simulation System 2

The THAAD HWIL missile simulation facility began development in November 1994 and has been on-line since June 1996 supporting the THAAD Program Office. An IAP with IER was delivered by the contractor in June 1996 and is operational to support the IAP-only mode using digital signal injection HWIL simulations using the IRSG and the signal injection interface. A block diagram of the IAP-Only HWIL configuration is shown in Figure 2.

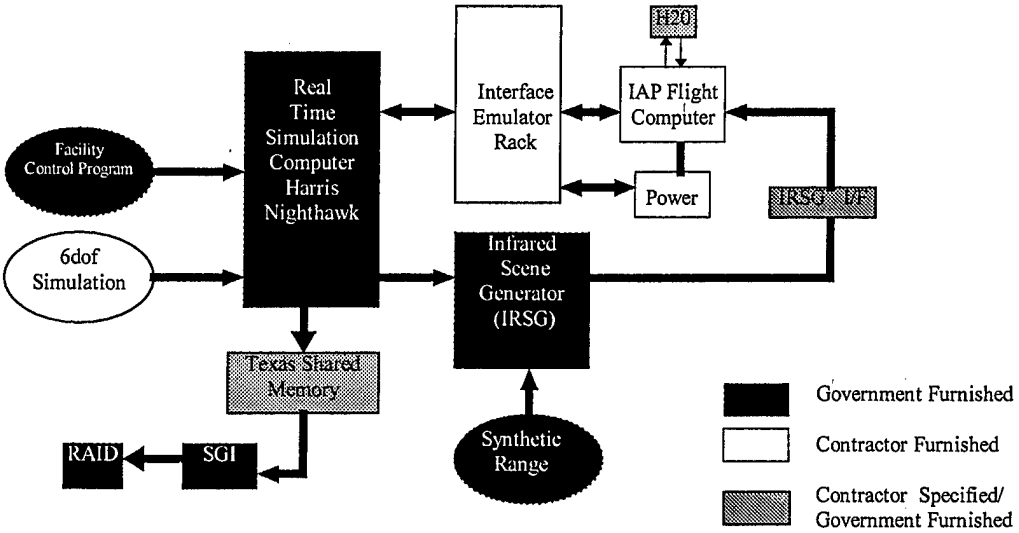


Figure 2. IAP-only I²RSS2 HWIL Interface Configuration

An InSb seeker is expected to be delivered to support flight test preparation and missile system performance studies via dynamic IR projection using the LDAP. A block diagram of the Seeker and IAP HWIL configuration is shown in Figure 3 .

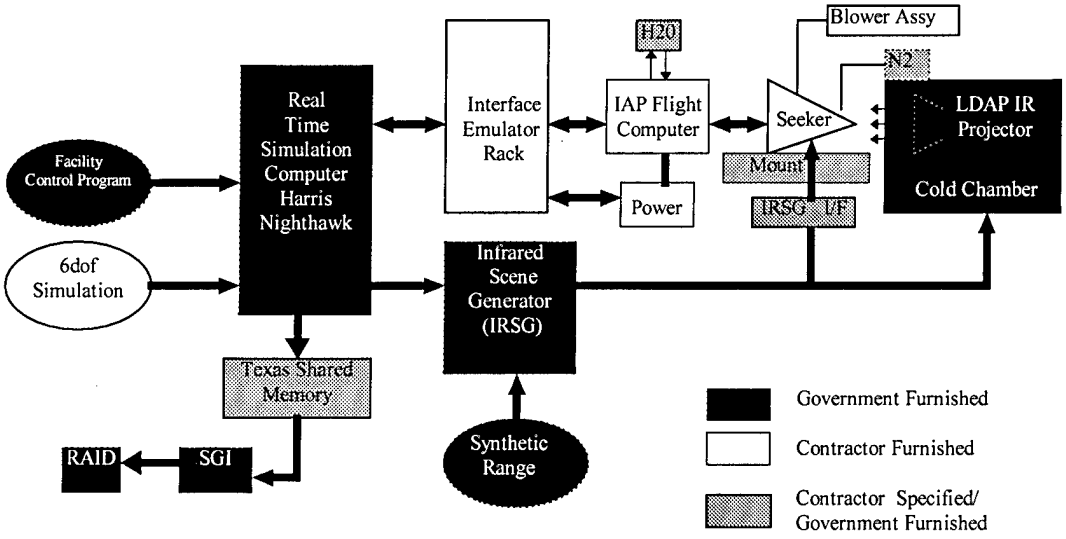


Figure 3. IR Seeker I²RSS2 HWIL Interface Configuration

Some examples of I²RSS2 HWIL simulation support include pre-flight predictions and post-flight analysis of Flight Test Vehicle (FTV) 6 and 7 in December 1995 and February 1996, respectively, and InSb image persistence studies for FTV08 in Jun-Jul 97 both using the IAP-only. In addition, IR projection studies using the LDAP was exercised with the entries of the Sensor Hand-over and Risk Reduction Program (SHaRRP) InSb camera, signal processor, and 2-axis gimbal hardware in October 1996 and September 1997. In summary, by utilizing the dynamic IR scene generator, signal injection interface, and LDAP, the THAAD I²RSS2 HWIL simulation can provide "value-added" THAAD missile performance simulation data using the real THAAD hardware and flight software, engaging simulated threat targets and scenarios in a real-time, closed-loop HWIL environment, second only to real flight test.

IV. SIGNAL INJECTION CARD OVERVIEW

In order to properly test the THAAD IAP in a closed-loop simulation scenario it was necessary to fabricate an interface which would combine video signals from the Silicon Graphics DVI interface and status information from the Camera Emulator card in the THAAD IER and transmit this information to the THAAD Camera Monitor card in the IER.

V. SIGNAL CONSTRAINTS

The signals from the DVI interface consist of five 12-bit words, 5 clock signals and an enable signal (YSIZEN). The status signals from the camera emulator card in the IER consists of a data stream of 12 bits, a valid data signal, a valid clock signal, a valid row signal, and a valid status signal.

A. DVI INTERFACE

The DVI interface sends information on five pixels simultaneously. Each pixel is designated by 12 bits. In addition, a clock signal accompanies each group of 12 bits so that there are a total of 65 signals necessary to specify the pixel information. This information is sent five pixels at a time so that if a row was 100 pixels wide, the pixel information in that row could be sent in the time it takes to send 20 clock pulses (Fig. 5). The first pixel of information sent from the DVI will represent the top left pixel of the picture (0,0 in Fig. 4). The DVI is capable of sending a frame 640 pixels x 640 pixels but the actual desired frame, sent to the IER, is smaller. (The DVI accomplishes this by essentially masking all the pixels in the 640 x 640 frame not wanted in the smaller frame.) Because this smaller frame (represented by the dotted line in Fig. 4) may lie anywhere within the 640 x 640 frame, a signal (YSIZEN) is sent by the DVI indicating where in the larger frame the smaller frame is located. The YSIZEN signal transitions from low to high when the DVI begins to send data at the first solid horizontal line (p0) of the desired frame. The YSIZEN signal returns to the low state when the DVI reaches the horizontal line under the last line of the smaller frame (p1) (Fig. 4). The YSIZEN signal, therefore, transitions from low to high and back once during each frame sent from the DVI.

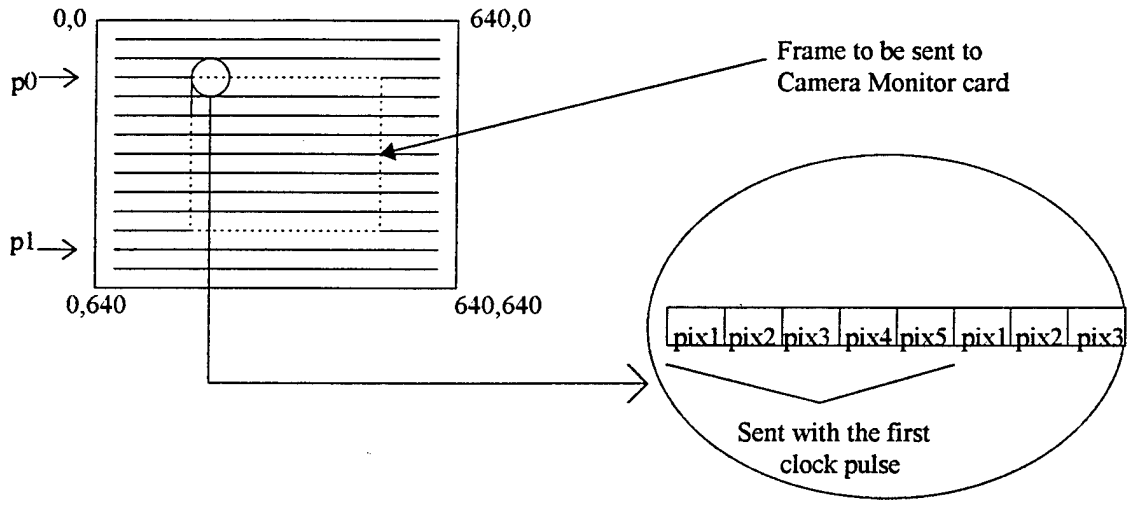


Figure 4. 640 x 640 Frame with the Desired Smaller Frame within its Boundaries.

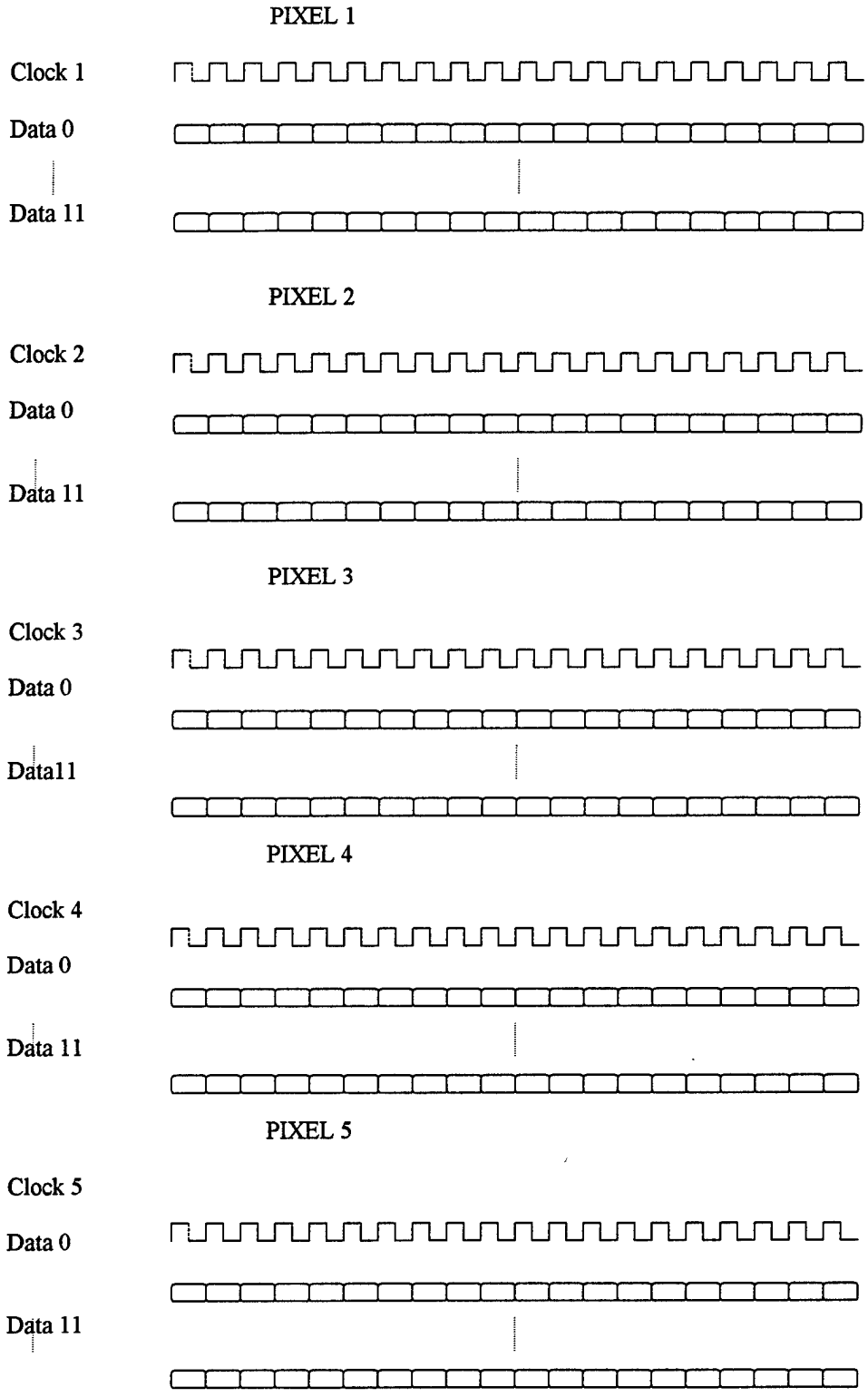


Figure 5. Timing Diagram for Clock and Data Information from DVI Interface.

B. CAMERA EMULATOR

The Camera Emulator card in the IER transmits 12 parallel data lines, which contain the pixel information. In addition, there is a clock (CLK), a valid data line (VALDAT), a valid status line (STATVAL), and a valid row line (ROWVAL) (Fig. 6). The data lines carry both the status word and the data word. This status word is approximately eight 12-bit words. During signal injection, the status information for a frame must be preserved and attached to the simulated video data information sent to the camera monitor card. In other words, the data normally sent from the camera emulator card to the camera monitor card is discarded during the injection process and replaced with video data from the simulation.

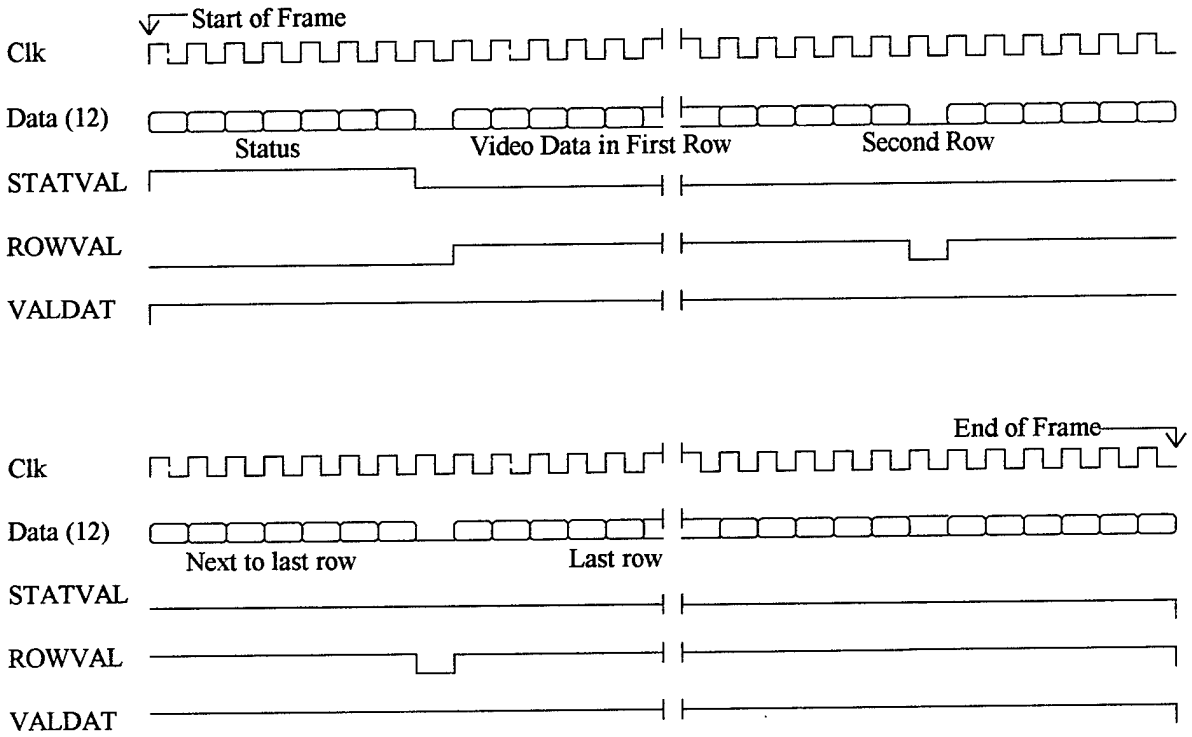


Figure 6. Timing Diagram of Status and Video Data to the Camera Monitor Card

The camera monitor card normally transmits a frame starting with the pixel in the lower right hand corner and finishing in the upper left corner. This pattern is exactly opposite of that sent by the DVI which sends pixel information starting in the upper left and finishing at the lower right corner of the frame. The signal injection card, therefore, must capture the incoming pixel information five pixels at a time and retransmit this information in reverse order one pixel at a time. The DVI transmits its video data at a rate of either 10 Mhz or 14 Mhz depending upon frame rate. The signal injection card must retransmit the data at 8 Mhz.

VI. SIGNAL INJECTION CARD TECHNICAL DESCRIPTION

A. Circuit Overview

The schematics for the signal injection card are provided in the Appendix to this report. The signal injection card receives status and data information from the Camera Emulator card and video data from the DVI card. The Signal Injection (SI) card stores every frame of video data from the DVI in two sets of dual-port Random Access Memory (RAM). Each set of RAM alternates capturing a frame of data. When the time comes to transmit a frame of video data, this frame comes from the last RAM to capture an entire frame. While this RAM is dumping its contents, the other RAM is reassigned the task of capturing every frame sent from the DVI. When the first RAM is through sending data, the two sets of RAM resume capturing alternating frames until it is time to send another frame. The two sets of RAM are able to work in this manner when the frame rate from the DVI is faster than the frame rate from the SI card to the Camera Monitor. This situation occurs at the beginning of a simulation run. As the run proceeds, the outgoing frame rate increases. Near the end of a run the two frame rates are identical, at which time, one set of RAM is sending out a frame while the other RAM is capturing the next frame to be sent. As was mentioned previously, the video data is transmitted from the SI card in reverse order, therefore, the first pixels of data stored by the RAM are the last sent to the Camera Monitor card and vice versa.

Incoming video data from the Camera Emulator card serves as the signal to the SI card to send the next frame of data. As each frame is sent from the Camera Emulator card, the SI card stores the status portion of the transmission in a First-In-First-Out Register (FIFO) and ignores the accompanying video data. After the status information is stored in the FIFO, the SI card sends this status word followed immediately by the video data word stored in RAM. The timing diagram of this status and video data to the Camera Monitor card is shown in Figure 6.

There is no external communication with the SI card other than the video data from the DVI and the Camera Emulator card. The SI card does contain a clear switch which should be depressed before each run.

B. Schematic Sheet 1 and 2

These two pages show the input connectors (Sheet 1) and the differential receivers for those incoming signals (Sheet 2).

C. Schematic Sheet 3

This sheet shows the circuit which generates the load pulse for the RAM. The incoming data rate from the DVI may be as fast as 14 Mhz which translates to a period of approximately 72 ns. The RAM used on the card (IDT-7026) requires a load pulse duration of at least 30 ns, therefore, a circuit was required which would allow for control of the length of the load pulse. This circuit is triggered by the presence of CLOCK_5 because the presence of this clock will always signal the transmission of part if not all of the first five pixel group in the frame needed by the Camera Monitor card. The only time during transmission of the smaller frame, that five pixels would not be sent, is at the start of a line. This is due to the fact that the DVI sends these five pixel groups from the start of a line 640 pixels wide. The start of the first line of the frame

needed by the Camera Monitor card may not coincide with the first pixel of the group of five, but may, for example, coincide with the third pixel. In this event, the clocks associated with the first two pixels in the first group of five to lie in this smaller frame would not be present. There would only be clocks associated with the last three pixels of the group. The clocks associated with the first two pixels would not begin until the second group of five was sent. (Fig. 7) In other words, a 640 x 640 pixel frame is sent by the DVI but the clock associated with each of the pixels is not active at the beginning of a line until the pixel falls in the frame needed by the Camera Monitor card.

At the end of a line, all 5 clocks will remain active even if part of the group of five falls past the end of a line in the smaller frame. For example, if the pixel at the end of a line in the smaller frame was the second in the group of five, the clocks associated with the third, fourth, and fifth pixels would remain active and then all five would go inactive together when the next group of five pixels was transmitted.

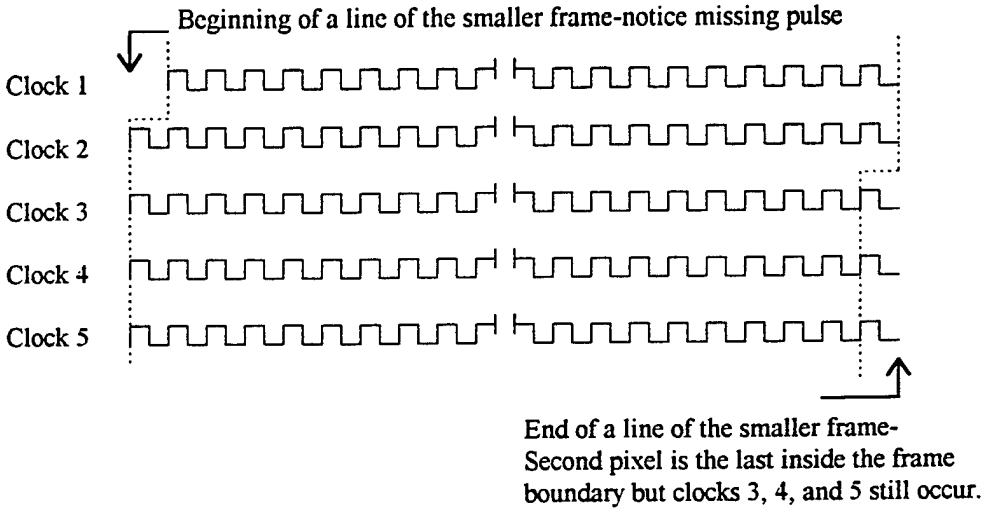


Figure 7. Example of Clocks Associated with the Five Pixels Groups in a Line of Video Data
(Valid Video Data Associated with Clocks is inside Dashed Lines)

The circuit on sheet 3 detects only clock 5 because if any pixel is active in a group of five, this clock will be present, therefore, it is used to generate the load strobe for the pixel data. The start of the clock pulse triggers the start of the load strobe, RAM_LD. The active low counterpart of RAM_LD is delayed 30 ns and used to terminate the RAM_LD pulse. The active low pulse on pin 1 of flip flop BJ10A, used to terminate this load pulse, must be short enough not to interfere with the next clock pulse coming in, Therefore, the length of this clear pulse is limited by the delay CP34. In addition, each time a RAM_LD pulse is generated, a clock pulse (WAC_CLK) is sent to the counters which generate the addresses for the RAM storing this pixel information. Figure 8 shows the relationship between the CLK_5 pulse, RAM_LD and the WAC_CLK.

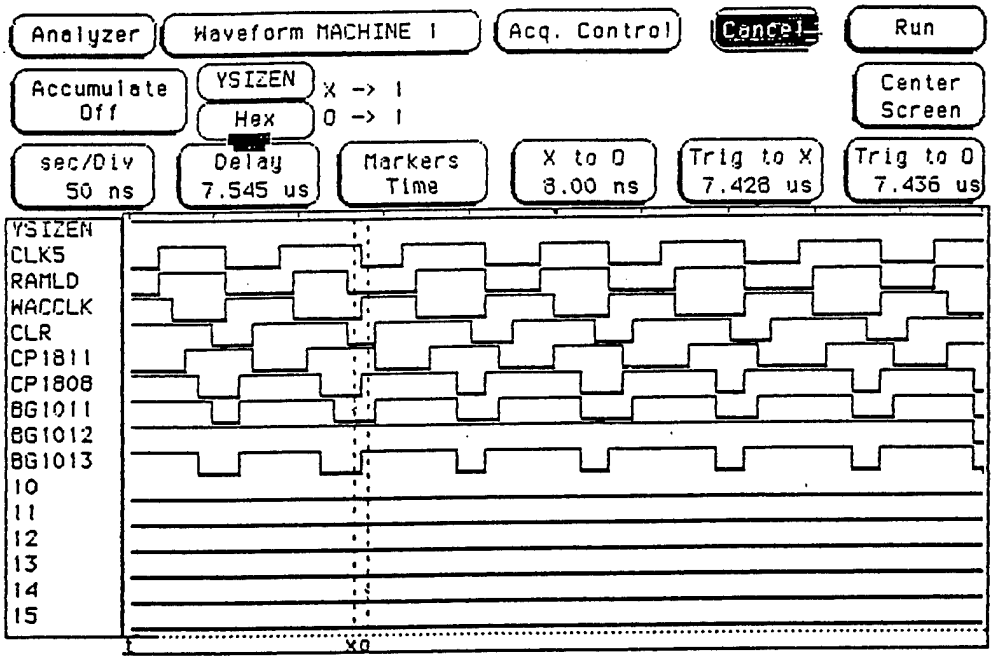


Figure 8. Timing Diagram of Circuit Shown on Sheet 3.

D. Schematic Sheets 4 through 8

These sheets show the RAM used to store the pixel information. Because the pixel information from the DVI is being sent at intervals as often as every 72 ns it became necessary to store each pixel in the group of five in its own RAM. Therefore, five separate groups of RAM are used. Because of the potential interrupt problems that may occur when one frame is being stored in RAM while the last frame is being written out of that same RAM, a situation that would inevitably happen many times during a simulation run, two separate RAM were used to capture each pixel in the group of five. Therefore, 10 RAM or 2 banks of five are used on the card. During normal operation, one frame is stored in one bank of RAM and the next frame is stored in the other bank. When one bank of RAM is reading out a frame of data, each incoming frame is being stored in the other RAM with the most recent frame overwriting the last. Only one bank at a time is given a write enable, therefore, of the two enable signals, BANK1_WEN and BANK2_WEN, only one may be low at a time. This low allows NOR gates BC01A or B to generate the pulse which enables the left port of one bank of RAM. Figures 9 and 10 show the relationship between the RAM_LD pulse and the RAM enable (CEL/1) and read (R/WL) strobes for the left port of RAM. DAL5 is a one of the data bits to the RAM and was set to toggle from pixel to pixel. ADR0 is address bit 0 on the left port of RAM.

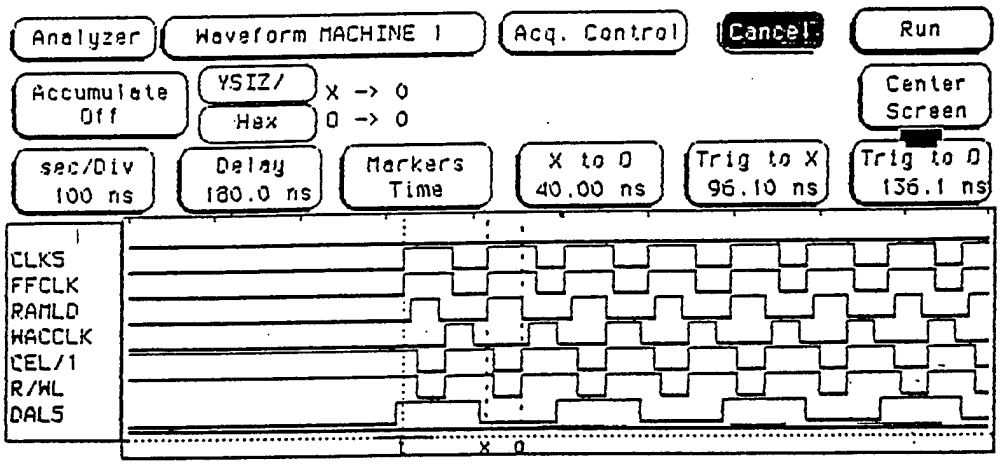


Figure 9. Timing diagram of Signals Accessing the Left Port of RAM

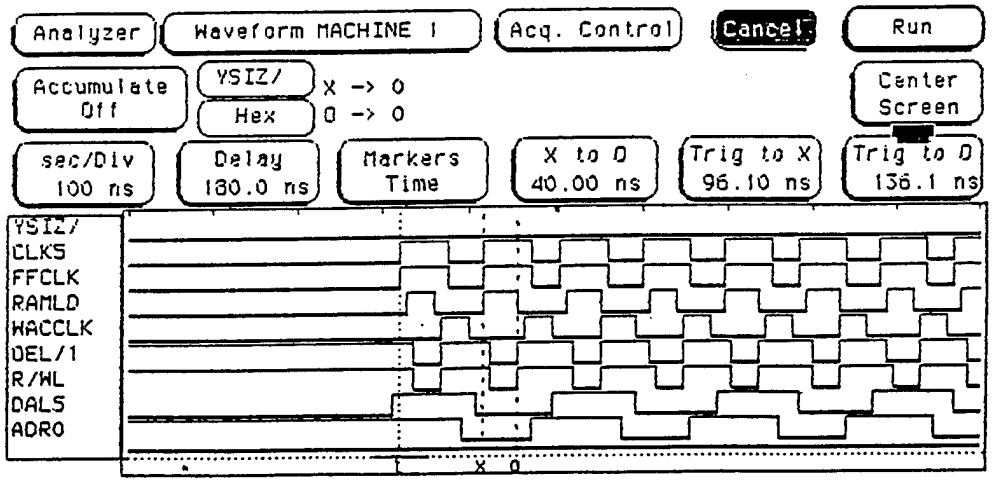


Figure 10. Timing Diagram Showing RAM Enable Pulses

E. Schematic Sheet 9

Circuits shown on this sheet perform three primary functions: (1) they control the toggle between BANK1_WEN and BANK2_WEN, the enable strobes for the two banks of RAM, (2) they generate the commands which prompt the FIFO to dump the status words, and (3) they generate several pulses which initiate the process of reading data from RAM.

1. Under circumstances in which successive frames of video data are being received by the SI card from the DVI, BANK1_WEN and BANK2_WEN simply toggle at the end of a capture of a frame of data as signaled by the transition from low to high of YSIZE_EN#. Refer to Figure 4 and Section V.A., for an explanation of YSIZE_EN. If the Camera Emulator card signals the SI card to send a frame of video data from RAM a clock will be seen on CE09 pin 3. This will force CE09A pin 6 low and inhibit the toggling of the two RAM enable signals from flip flop CE01B pins 8 and 9. If an inhibit occurs during the capture of a frame, toggling will not occur at the end of YSIZE_EN. If Bank A was enabled to capture the incoming frame at the time of the inhibit, Bank B will be the only RAM to contain the most recent, complete frame. Bank B will, therefore, remain disabled from the write process in order for it to transmit its frame of video data. Bank A will remain enabled for the write process and will capture each successive frame until the inhibit is removed on pin 5 of gate CA01B and normal toggling is resumed. The inhibit will remain until Bank B has completed transmitting its data.

The strobe, RAC_LD, loads the counters which generate the RAM addresses for the read process. Ordinarily this strobe occurs at the end of a frame but if the read process is still occurring at the time the frame ends, pin 2 of gate BT10A will be low which will inhibit the load strobe. This load strobe will instead be generated at the end of the next incoming frame.

2. READ_ST2 is an active high pulse which is generated once the card has captured an entire status word from the Camera Emulator card. Once this status word has been stored in a FIFO the SI card should immediately transmit this status word followed by the last complete frame of video data stored in RAM, to the Camera Monitor card. Before this transmission begins, a number of events must take place. Initially, three events must occur simultaneously. An active high level (OUT_EN) from flip flop CE09B pin 9 sets up the FIFOs to write, shift register CC17 must be enabled, and counter CA17 must be enabled.

Shift register CC17 generates an active high pulse which lasts for either five or eight clock pulses depending upon the length of time counter CA17 is enabled. (See Figures 11 and 12.) This register leads to the production of four signals. The first is VALSTAT# which acts as an inhibit signal to prevent the FIFO from storing an incoming status word while it is writing out the last word. UNCK is a series of either five or eight pulses which go to the FIFO to clock out the status word. VDATOUT and STATVAL are status lines generated on the SI card and sent to the Camera Monitor card. These lines are identical in function to the status lines VALDAT and STATVAL described in Section B.1 and Figure 3. They are necessary in order for the Camera Monitor card to properly interpret the incoming status and video data.

An active low level from flip flop CE09B-pin 8 enables counter CA17 to begin counting up to either five or eight depending upon the position of SPDT switch S1. When gate CT28A-pin 3 goes low, this pulse is delayed 40 ns and used to clear the shift register which terminates VALSTAT# and UNCK. The counter, therefore, is used to control the length of time the FIFO is accessed.

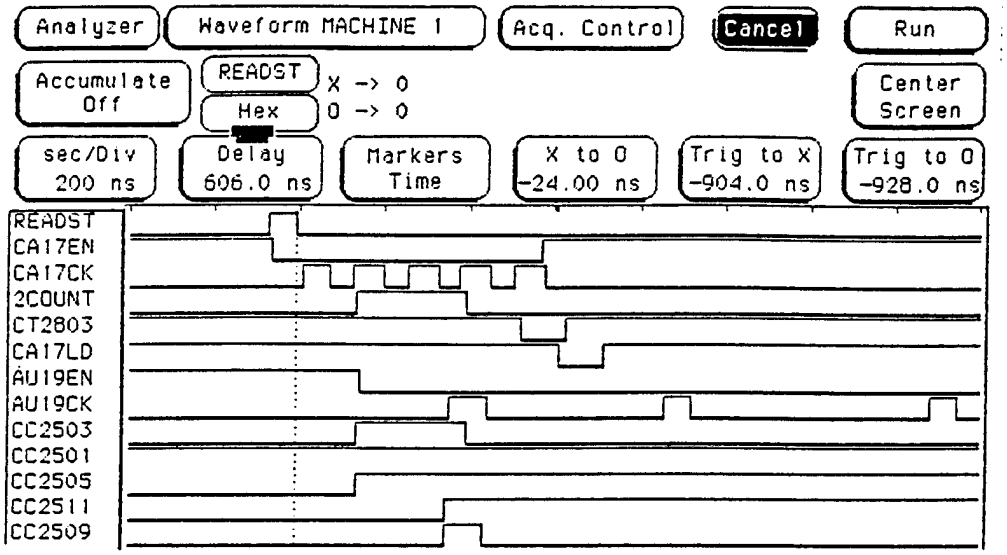


Figure 11. Generation of 5 Pulses.

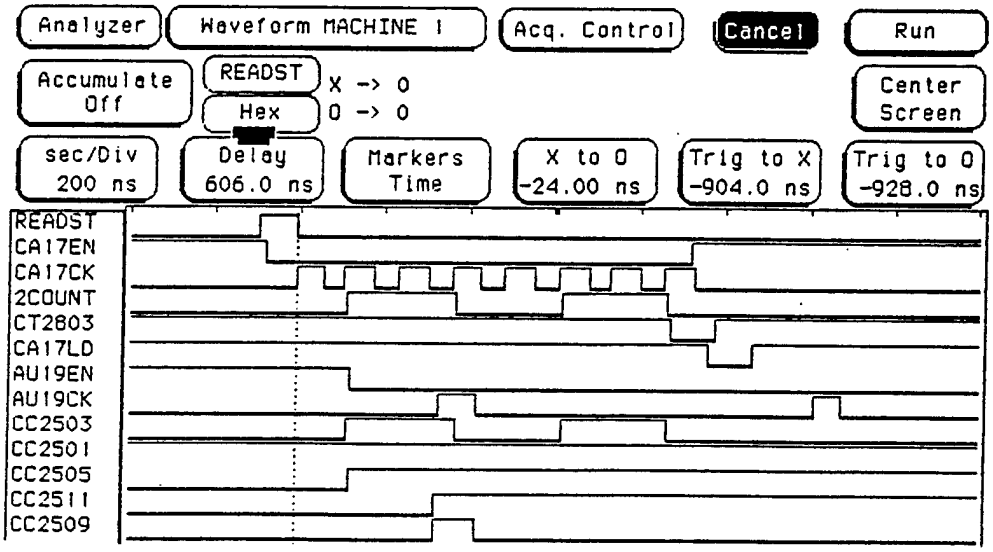


Figure 12. Generation of 8 Pulses

3. One hundred nanosecond delay, CP26, generates a pulse at pin 12 which is passed through multiplexer CL49. This pulse clocks flip-flop CE09A which initiates a series of events which lead to the transmission of the data stored in RAM. If switch S1 is selected to generate a status word size of eight, this pulse (ST) is routed to a counter (shown on sheet 14) which generates a delay. Once the delay has expired, an active high pulse (ST_DEL), is generated which clocks flip flop CE09A. The purpose and operation of this delay will be explained in section J, which pertains to Schematic Sheet 14. This flip-flop, in addition to generating the two inhibit signals discussed earlier in Section E.1., also generates an active low level which is seen on flip flop BJ10B at the rising edge of the next 8 Mhz clock pulse. Between transmission of frames of video data, RAC_EN is normally low and RAC_EN# is normally high. Just prior to accessing the video data from RAM these two signals are inverted by the low level from CE09A-pin 6. RAC_EN and RAC_EN# are used to enable a circuit shown on sheet 12 which controls the order in which the five banks of RAM are accessed. Flip-flop BJ10B is preset at the end of the frame by signal READSTOP# which returns RAC_EN to low and RAC_EN# to high.

F. Schematic Sheet 10

This sheet shows the registers which hold the data as it is accessed from RAM. These registers are all connected to a common output bus which leads to output registers. The data from RAM is clocked into these registers by a bit which is set in bit position 12 of RAM. Any 12-bit data word coming from the Camera Emulator card and stored in bit positions zero through 11 of RAM also has a zero stored in position 12. As the data is accessed from RAM, the zero in bit position 12 is inverted and used to enable and clock the register. Resistor pack AP54 provides the necessary pull up resistors for bit 12.

G. Schematic Sheet 11

This page shows the two sets of 14-bit counters used to address RAM. The Write counters address the left port of RAM and specifies which address will store each pixel in the incoming frame. The Write counters are incremented once for each CLOCK_5 coming in to the SI card. This write address is seen at the left port of all five sets of RAM, and both banks. This allows the first pixel, if it has an accompanying CLOCK_1, to be stored in address location one of the enabled bank of RAM A. Pixel two is stored in RAM B and so on. The five pixels in the second group are stored in address position two of the enabled bank of RAM A through E respectively. The write counters are loaded by either a Clear Pulse (CLR) or a pulse generated 200 ns after the end of each frame of video data.

The read counters address the right port of the RAM. The right port is used exclusively for reading data from RAM. After an entire frame of video data has been stored in RAM, the last value on the output of the write counters will be loaded into the read counters and used as a starting point for the read counters when they begin generating the read addresses. Unfortunately, this process is complicated by the fact that one additional CLOCK_5 pulse comes in from the DVI past the right edge of the desired smaller frame. This pulse over-increments the write counters by one. Before the read counters can be enabled, their starting count value must be decreased by one in order to compensate for the extra pulse. The 2COUNT pulse is used to generate this clock pulse. The read counters are synchronous counters meaning that they must be enabled in order for them to see a clock or generate an RCO pulse. The counters are asynchronous with respect to the load. The strobe 2COUNT is used to first enable the read

counters and then generate a single clock pulse which decrements the read counters by one. (Figs. 11 and 12.) Figure 13 shows the output of the read counters at the start of a frame. The initial count value in hex for a frame 256 x256 is 11 0100 0000 0001. After the clock pulse, generated by 2COUNT, the count becomes 11 0100 0000 0000 which is the correct starting address to begin accessing RAM. READSTOP# is generated when the read address counters decrement to zero at the end of a frame transmission. This pulse is used to disable counters and clear certain registers.

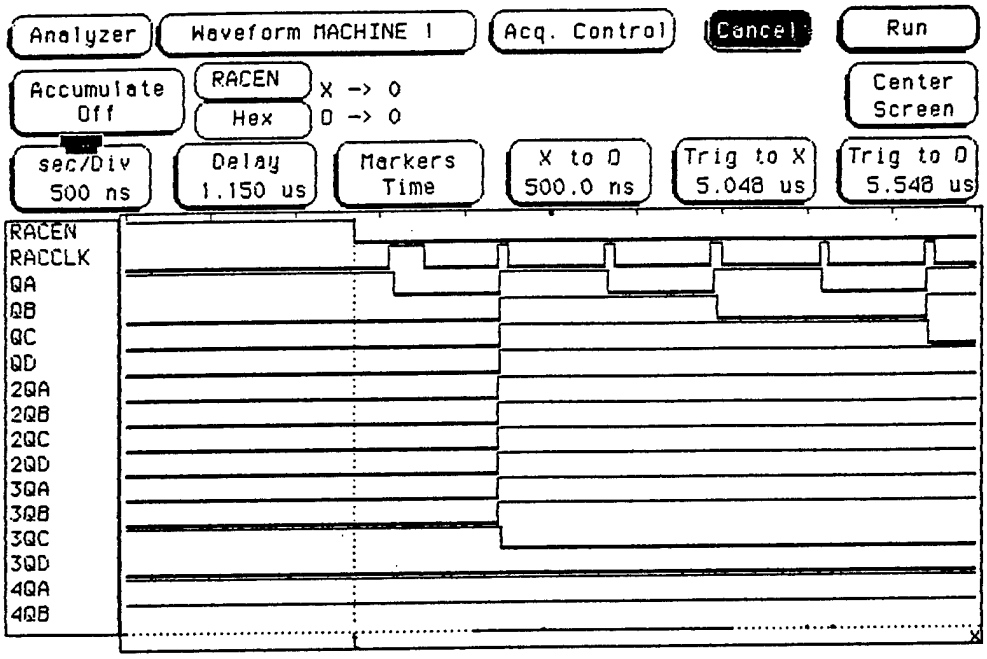


Figure 13. Starting Address from Read Counter at Start of Frame.

H. Schematic Sheet 12

The DVI sends a picture which starts in the upper left hand corner and scans from left to right and top to bottom. This is the order in which it is stored in RAM. The Camera Monitor card expects a picture which starts at the bottom left and scans right to left and bottom to top. The data in RAM must be accessed in the correct order to form the proper image, however, the process of retrieving this data is complicated by the fact that it was stored five pixels at a time in one of two banks of five sets of RAM and that the first pixel in each row (left side of frame) is not necessarily the first pixel in the group of five but may actually be any of the five. (In the example shown in Figure 4, the first line was shown to begin with pixel 1 only for the sake of simplicity. In reality, the first two pixels, for example, might not be within the boundaries of the smaller frame, therefore, the clocks associated with these two pixels would not be present and the data for the first two pixels would not be stored in RAM. In this case, there would only be three valid pixels out of a possible five at the beginning of each line.) The first pixel of the five to fall in the smaller frame will determine which RAM must be accessed first when reading back RAM. Should the frame width change during a simulation the first pixel in the frame may also change. The SI card must detect which pixel is first and use this information to control the order in which RAM is accessed during read back. The circuits shown on sheet 12 are responsible for accessing the correct bank of RAM and accessing RAM A through E in the correct order.

Counter BT34 is central to the circuits shown on sheet 12. The outputs of the counter feeds into a 3-to-8 decoder which generates pulses which will be used as enable strobes by the RAM. The counter is only allowed to count from one to five which produces the five strobes necessary for the five sets of RAM.

Initially the frame is 256 pixels long. Given a line length of 256, if the first pixel in the group of five is pixel A then the last pixel in the line will be an A pixel, if the first pixel is B then the last will be a B, etc. Remember that at the end of a line, if any of the five pixels lie outside of the frame, these pixels will still have clocks associated with them and will appear to the SI card as valid data. This data will be stored in RAM along with all other data but this bogus data will not be accessed during the read process.

If the counter starts counting from zero and counts to five, it will lead to the generation of five strobes from the 3-to-8 decoder. These five strobes will be routed through the two multiplexers to the two sets of five OR gates. Each set of gates feed RAM enable strobes to a corresponding bank of RAM. B1C/OE#1 through B1C/OE#5 are the enable strobes for bank 1 RAM 1 through 5, respectively. B2C/OE#1 through B2C/OE#5 provide the five enable strobes for bank 2. After routing through the multiplexer, the resulting order of the enable strobes will be A-E-D-C-B, therefore upon read back from RAM, the A pixel will be accessed first from the last address position in RAM that data was placed. (Pixels 1, 2, 3, 4, and 5 are obtained from RAM A, B, C, D, and E respectively. In this document, pixels 1, 2, 3, 4, and 5 are used interchangeably with pixels A, B, C, D, and E respectively.) Before pixel E is accessed, the read address counters must decrement by one. This is accomplished by clocking flip-flop CC41A which generates a 50 ns pulse (RACCLK) which clocks the read counters. Pixels E, D, C, and B are read next. The fifth strobe from the decoder reloads the counter and the process is repeated. If the first pixel in the line is B rather than A, then the first pixel to be read back must be the B pixel in the last RAM address to contain data. To access the B position first, the counters are loaded with a four rather than a zero and the counters generate the last strobe which will clock the B pixel from RAM and reload the counters with a zero. The counter resumes counting from one to five which will generate the five enable pulses in the desired order (A-E-D-C-B). The table below shows the initial number loaded into the counter to generate the correct initial RAM enable sequence.

Table 1. Counter Load Values Necessary for Accessing the First Pixel Correctly

FIRST PIXEL	NUMBER LOADED INTO COUNTER
A	0
B	4
C	3
D	2
E	1

The circuit to detect which pixel of the five will occur first, is shown on sheet 2 of the schematics labeled SI-Top in the Appendix. During a simulation run, the size of the frame sent from the DVI to the SI card changes to a smaller "windowed down" size. This smaller frame consists of lines of either 54 or 64 pixels depending upon whether the accompanying status information consists of five or eight words. The card must first sense when this new frame size

occurs and determine which pixel falls at the start of a line. When "windowing down" occurs the A port of the multiplexer is selected and the enable strobes from the decoder are re-routed which places the enable strobes in a different order. The counter is still loaded with values of zero through four to control the starting point of the counter in order to generate the correct starting enable sequence from the decoder.

The counter BT34 is loaded by strobes 2COUNT# and LD_COUNT#. 2COUNT# is generated at the beginning of a frame and LD_COUNT# is generated prior to accessing each line of video data from RAM. The counter is cleared when a CLR pulse is generated, when Q1, Q2, and Q3 are all zero, or when the fifth enable pulse is generated by the decoder.

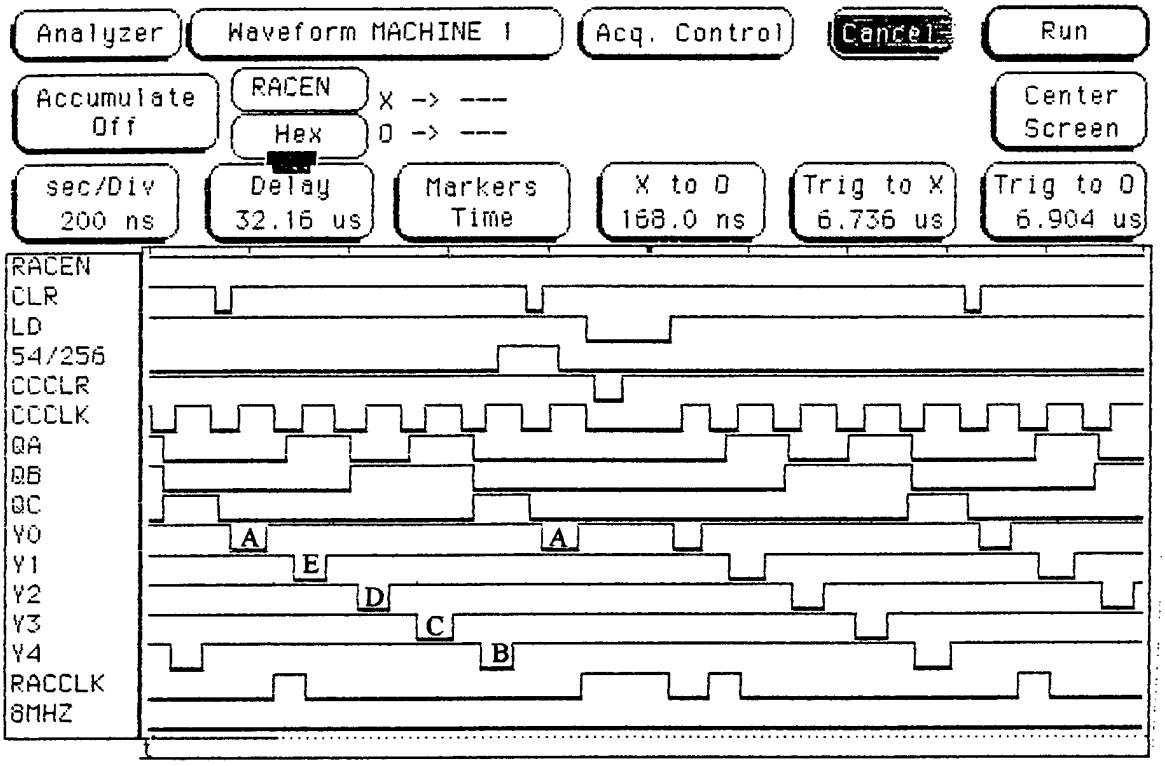


Figure 14. Timing Diagram of RAM Enable Circuit with Line Length of 256, First Pixel is A, at the End of the First Line of Video Data.

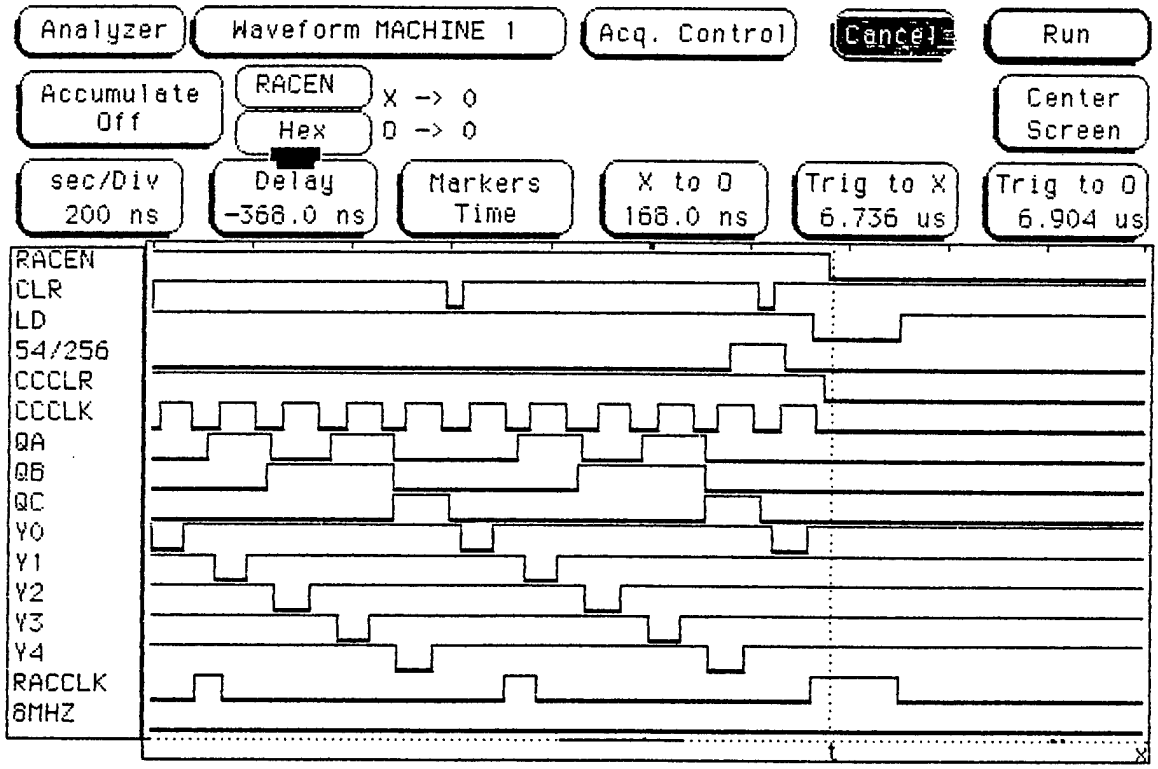


Figure 15. Timing Diagram of RAM Enable Circuit with Line Length of 256, First Pixel is A, at the End of the Frame of Video Data.

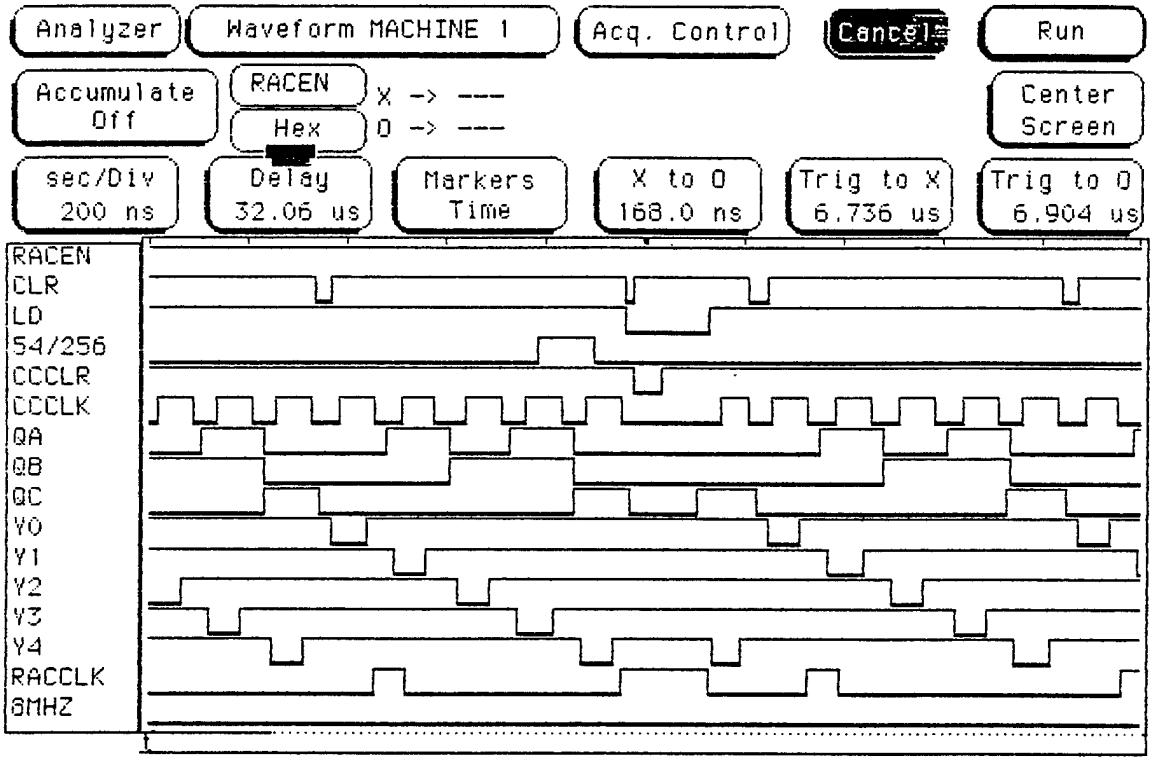


Figure 16. Timing Diagram of RAM Enable Circuit with Line Length of 256, First Pixel is B, at the End of the First Line of Video Data.

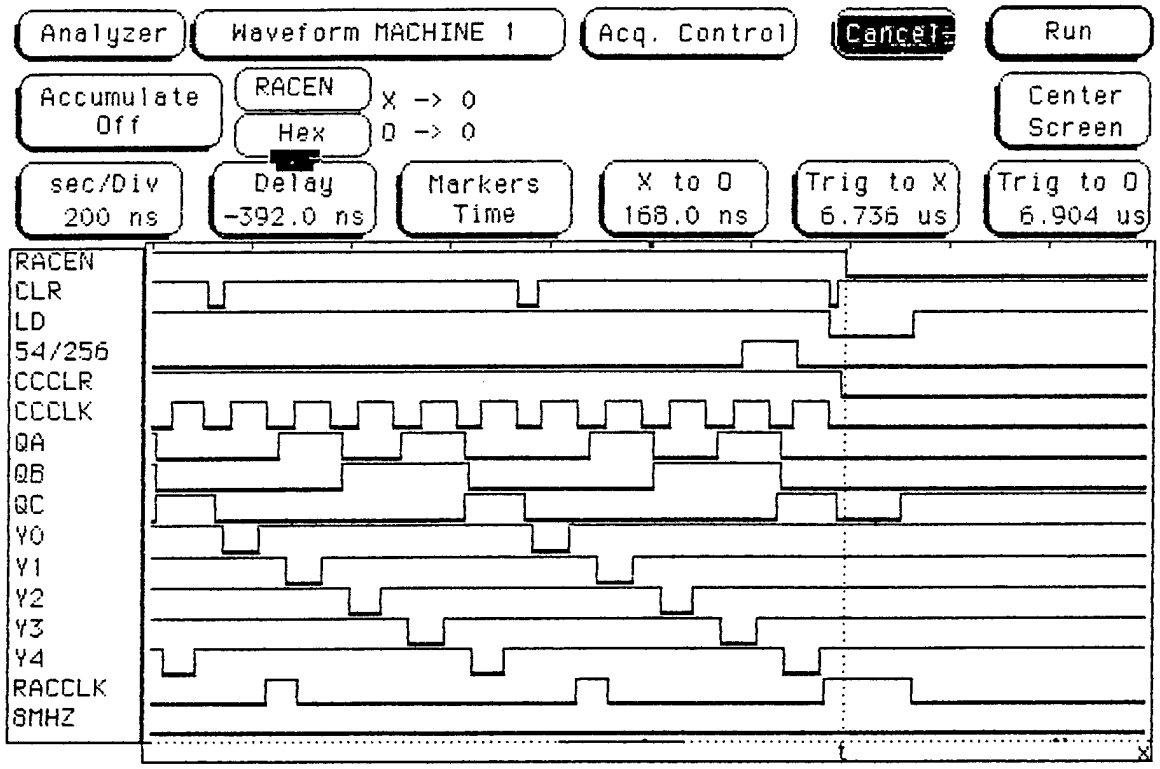


Figure 17. Timing Diagram of RAM Enable Circuit with Line Length of 256, First Pixel is B, at the End of the Frame of Video Data.

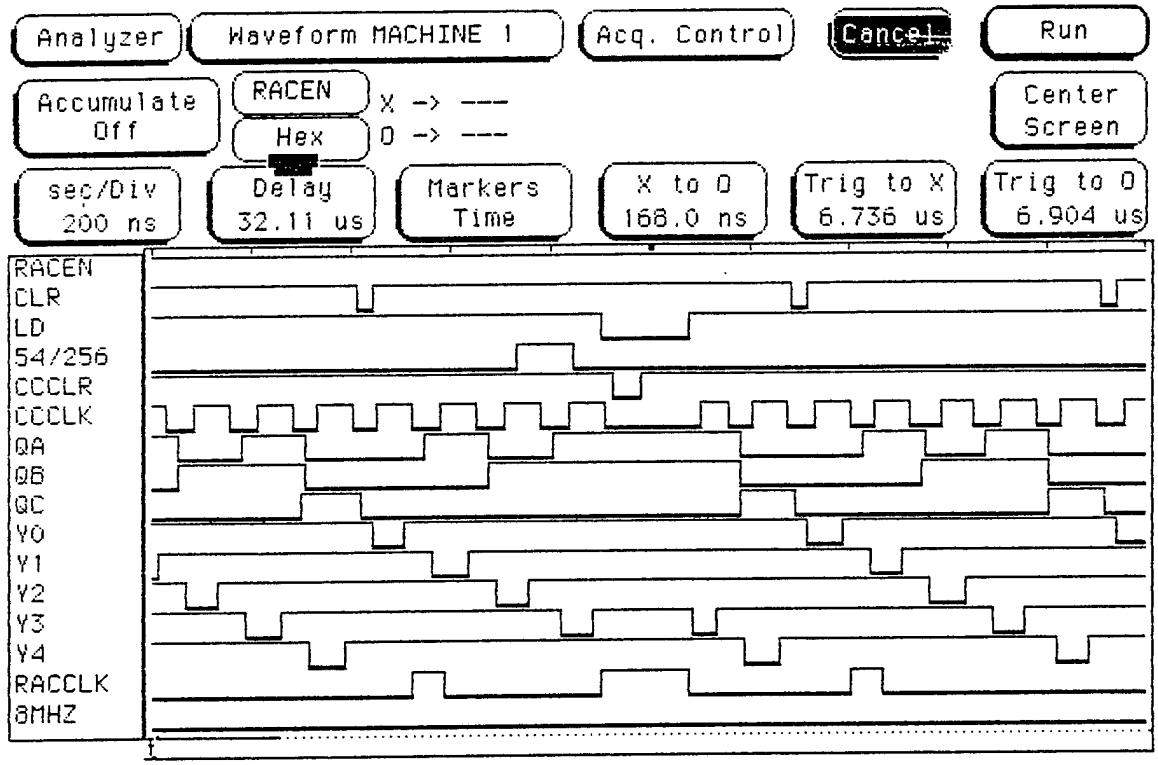


Figure 18. Timing Diagram of RAM Enable Circuit with Line Length of 256, First Pixel is C, at the End of the First Line of Video Data.

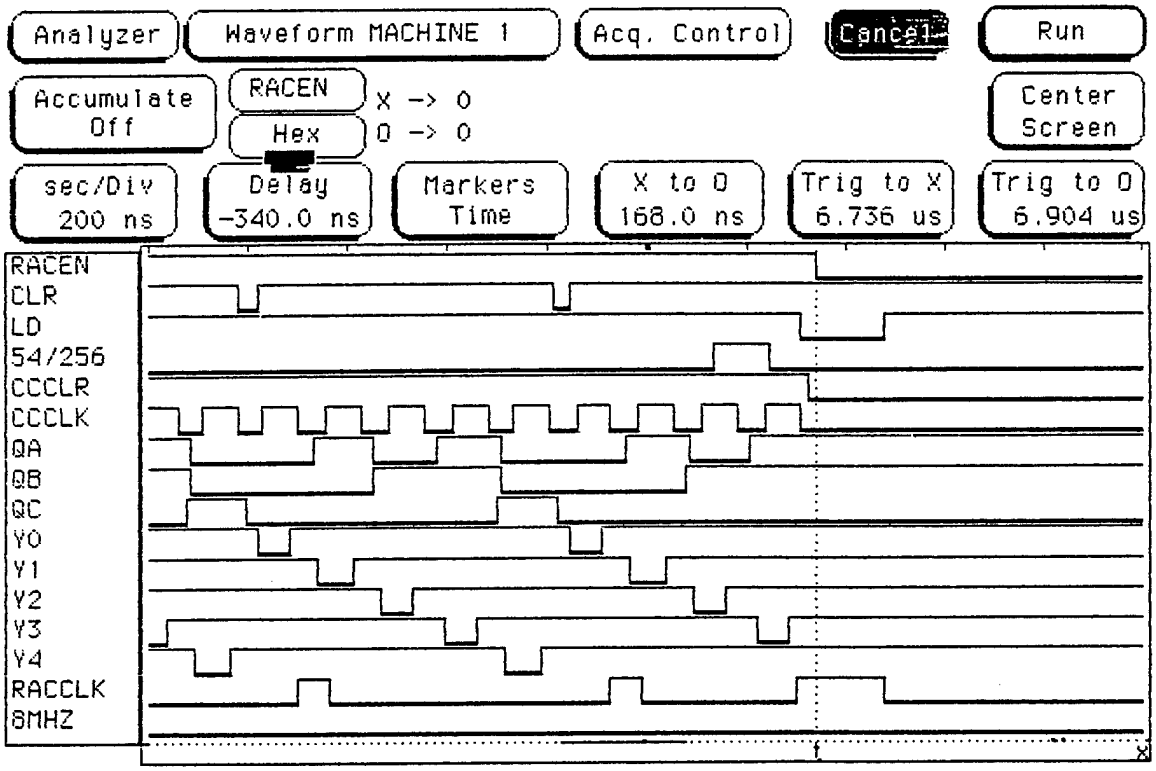


Figure 19. Timing Diagram of RAM Enable Circuit with Line Length of 256, First Pixel is C, at the End of the Frame of Video Data.

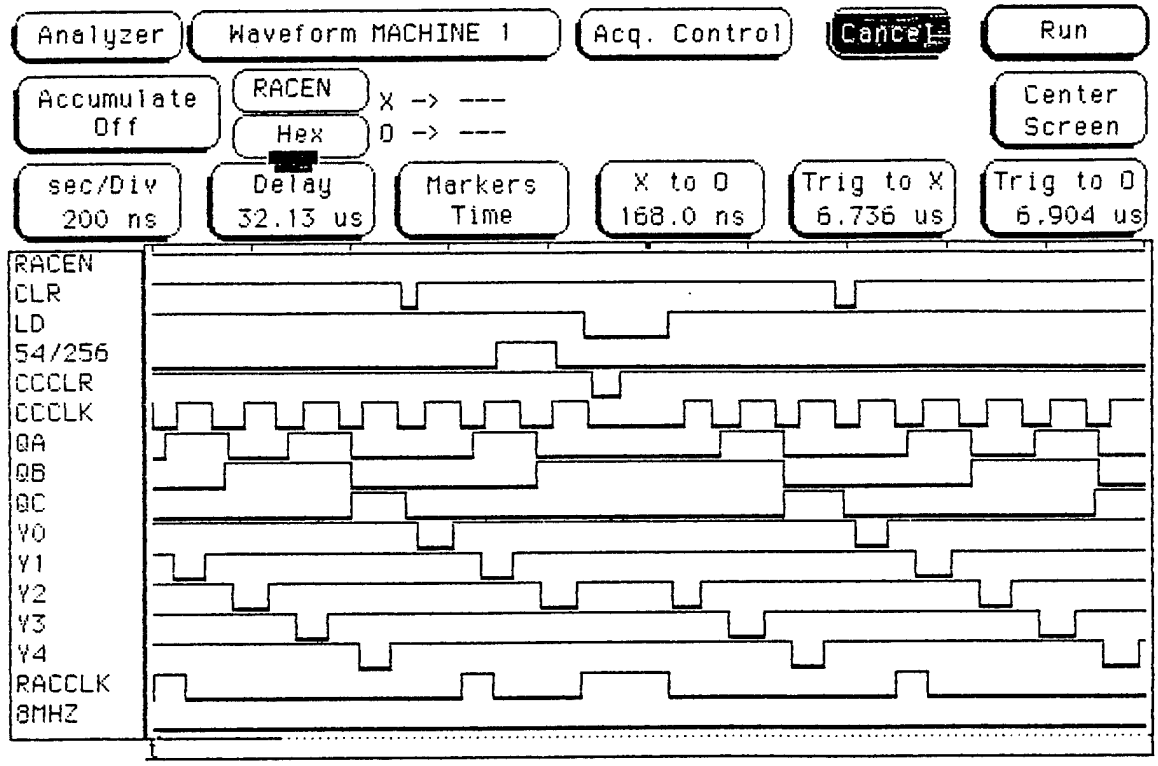


Figure 20. Timing Diagram of RAM Enable Circuit with Line Length of 256, First Pixel is D, at the End of the First Line of Video Data.

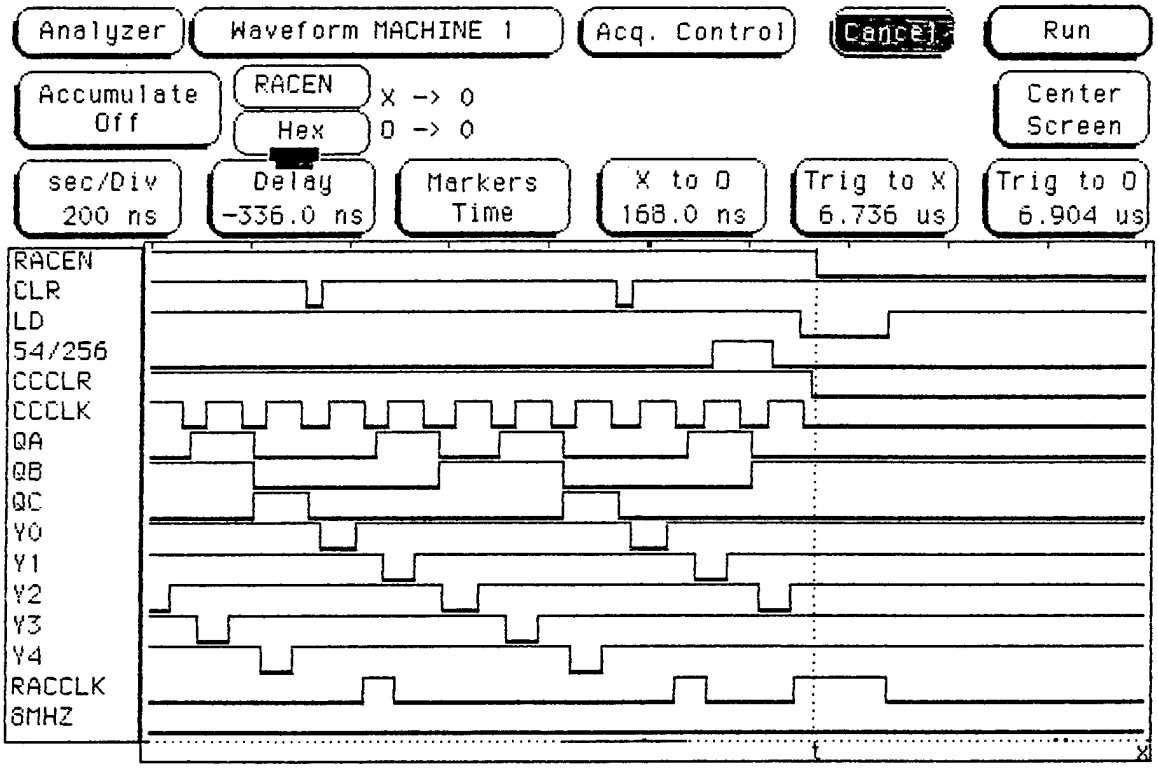


Figure 21. Timing Diagram of RAM Enable Circuit with Line Length of 256, First Pixel is D, at the End of the Frame of Video Data.

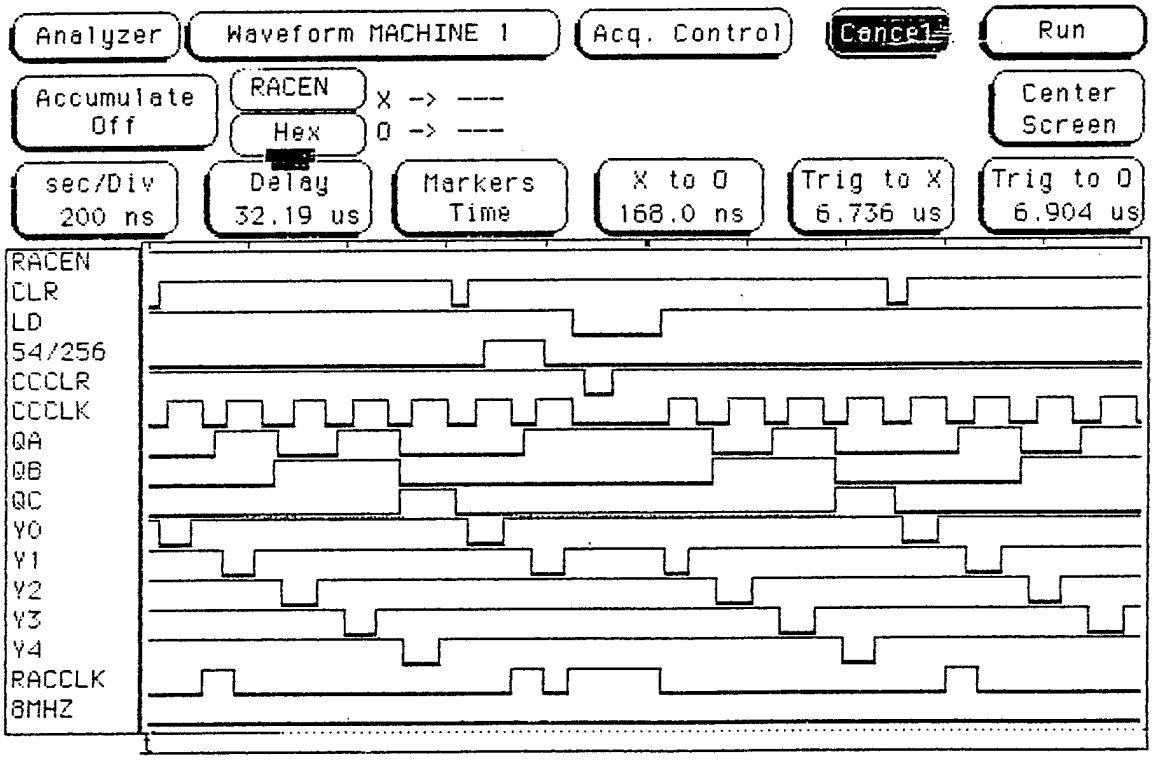


Figure 22. Timing Diagram of RAM Enable Circuit with Line Length of 256, First Pixel is E, at the End of the First Line of Video Data.

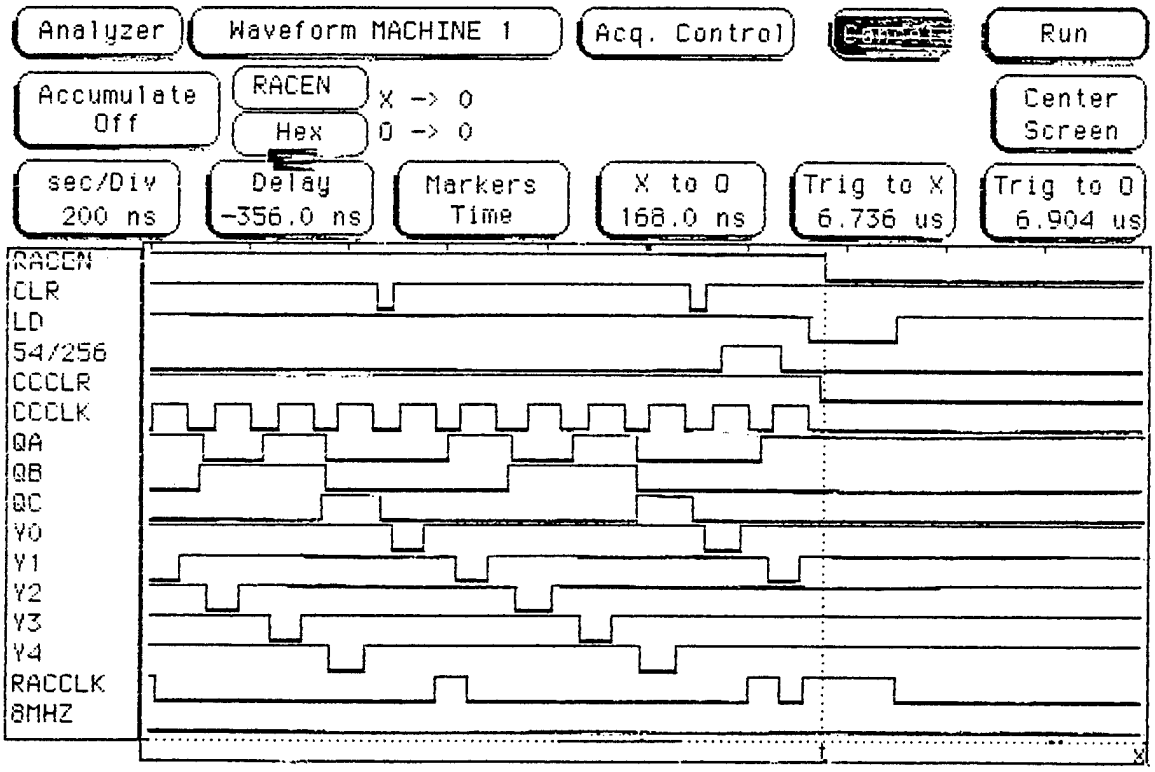


Figure 23. Timing Diagram of RAM Enable Circuit with Line Length of 256, First Pixel is E, at the End of the Frame of Video Data.

I. Schematic Sheet 13

This sheet shows the FIFO circuits which store the status words from the Camera Emulator card. Differential receivers are used to receive the 12 bits of status information, the valid status signal, STAT, and the clock, CLK. The relationship between the 12 bits of status information, the STATVAL signal and the CLK can be seen in Figure 6. The rising edge of the STAT signal generates a clear FIFO (FIFOCLR#) pulse (sheet 12) , a FIFO load enable (LDCKEN) (sheet 12) , forces NOSTAT# high, and generates a strobe which captures bits 6, 7, and 8 of status word one (Fig. 24). Bits 6, 7, and 8 of the first status word are stored in a register and decoded to determine the frame rate of the outgoing data. NOSTAT# is a level which is low until the first status word arrives. When NOSTAT# goes high it allows YSIZEN to generate the first READST2 pulse which prompts the FIFO's to transmit the status words (Fig. 25).

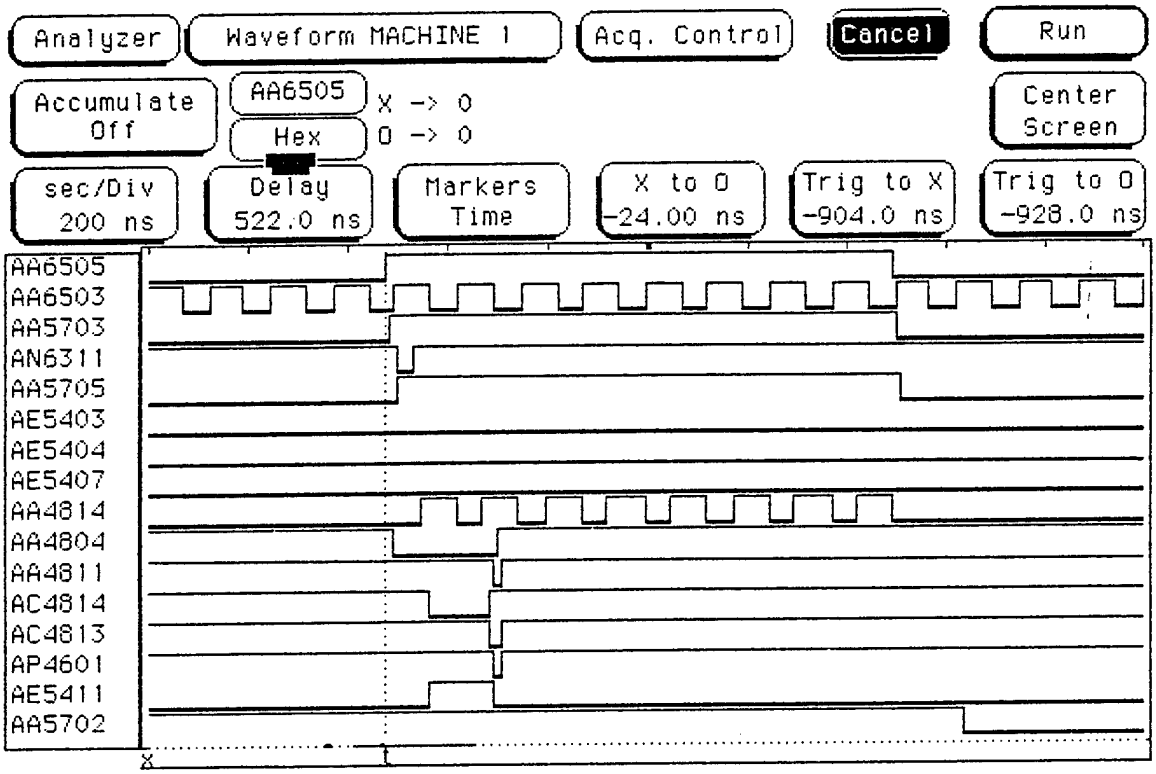


Figure 24. Loading FIFO with Status Words.

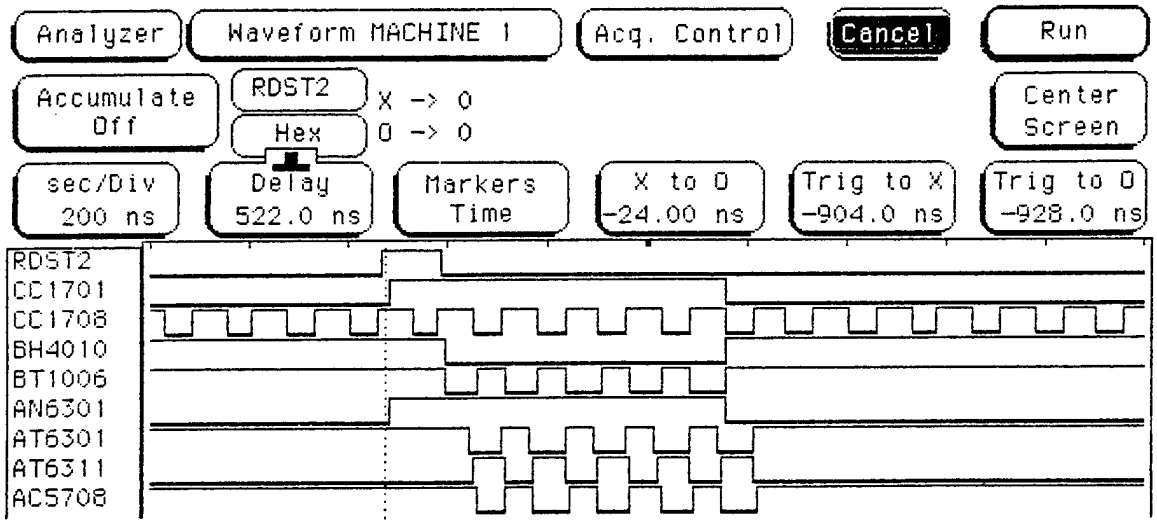


Figure 25. Transmitting Status Words from FIFO's.

Figure 25. Transmitting Status Words from FIFO's.

J. Schematic Sheet 14

When the SI card is selected to operate in the eight status word mode, it is necessary to have a delay between the end of the status words and the beginning of the data. This delay is approximately ((256 pixels per line - 8 status words) / 8,000,000 pixels per sec) + 1 clock pulse or about 32 usec for the larger frame size. For the smaller frame size. The delay is ((64 - 8)/8,000,000) + 1 clock pulse or 8 usec. Figures 26 through 29 show the operation of this counter. The value loaded into the counters is dependent upon the level of WINDDN as shown on sheet X-2.

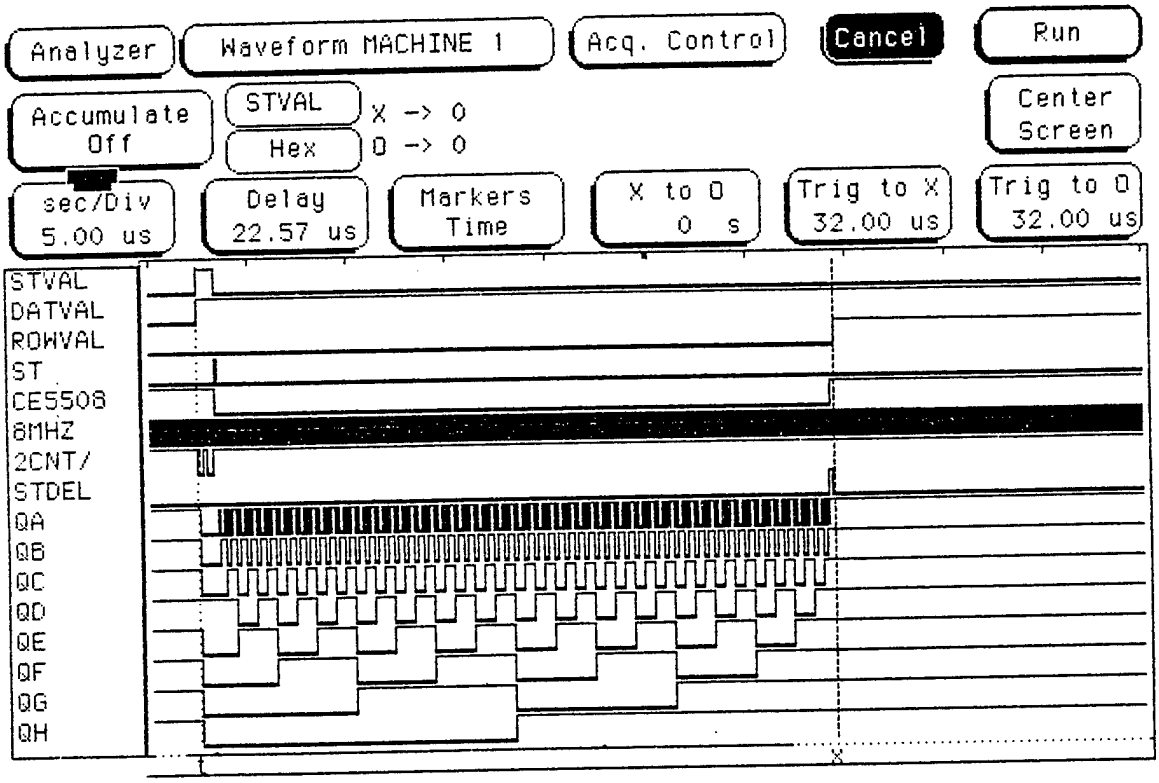


Figure 26. Counter Operation for a Line Length of 256.

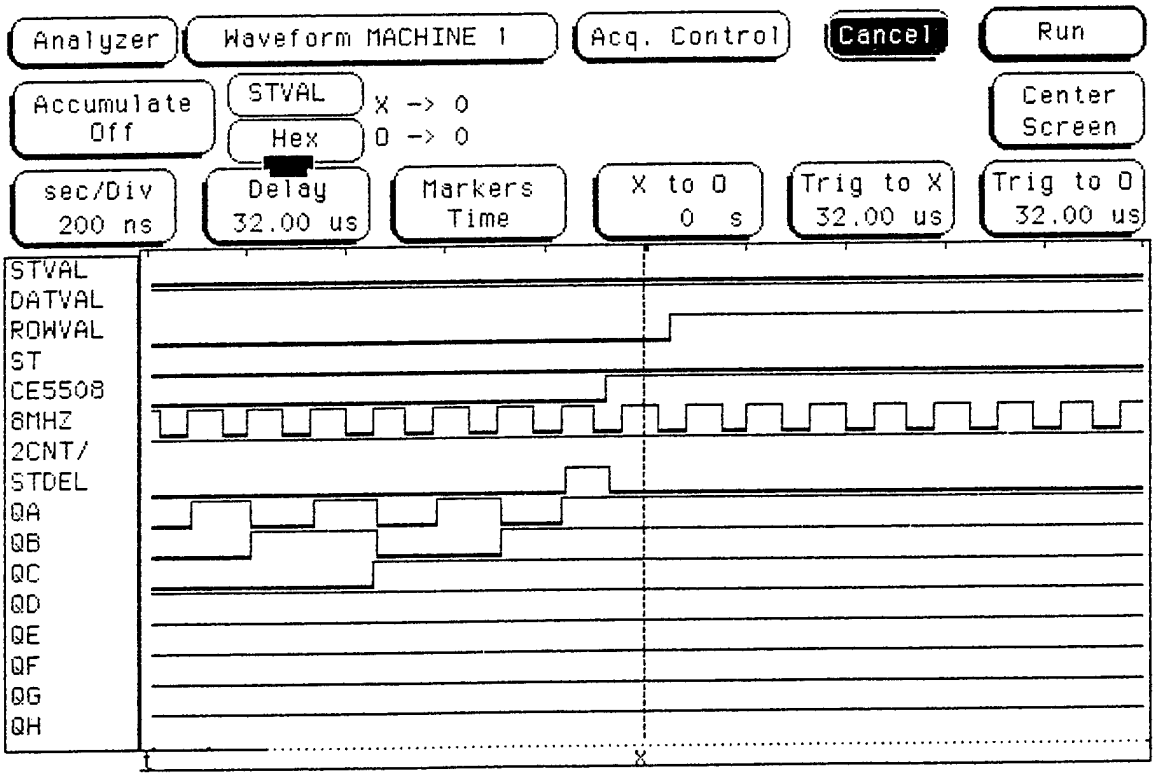


Figure 27. Counter Operation for a Line Length of 256. (Shows end of delay.)

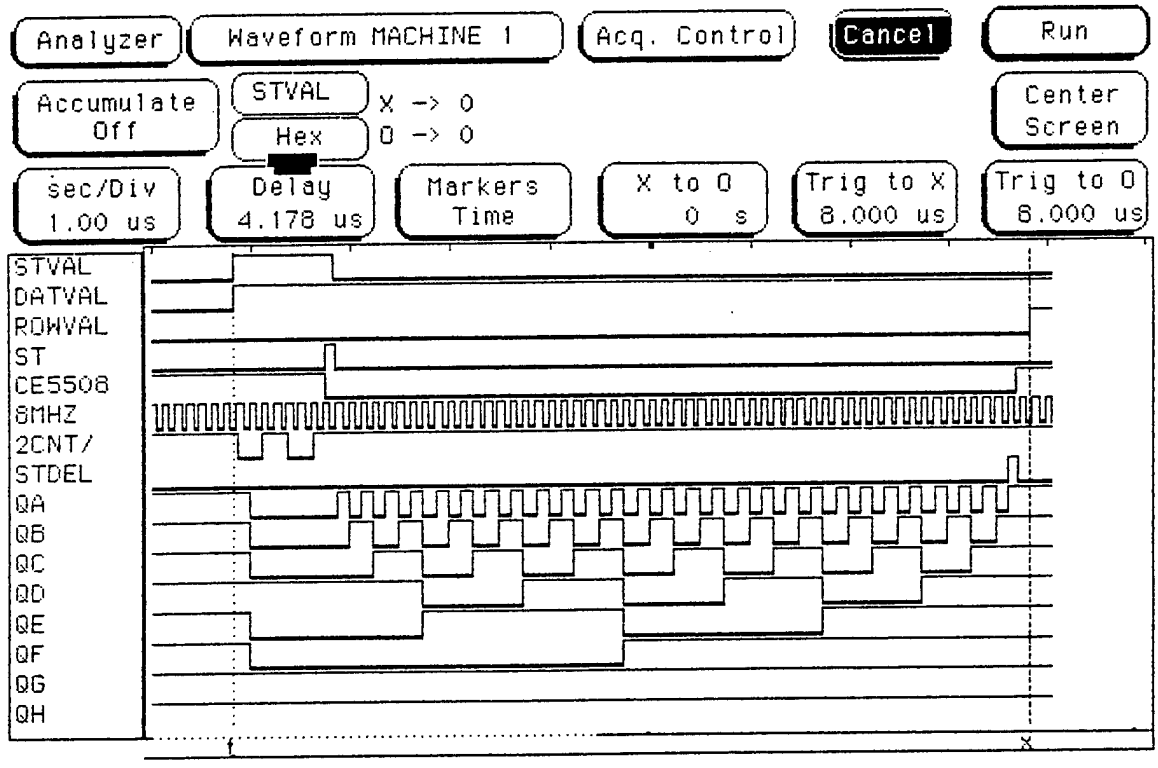


Figure 28. Counter Operation for a Line Length of 64.
(Loads 200, Counts to 255)

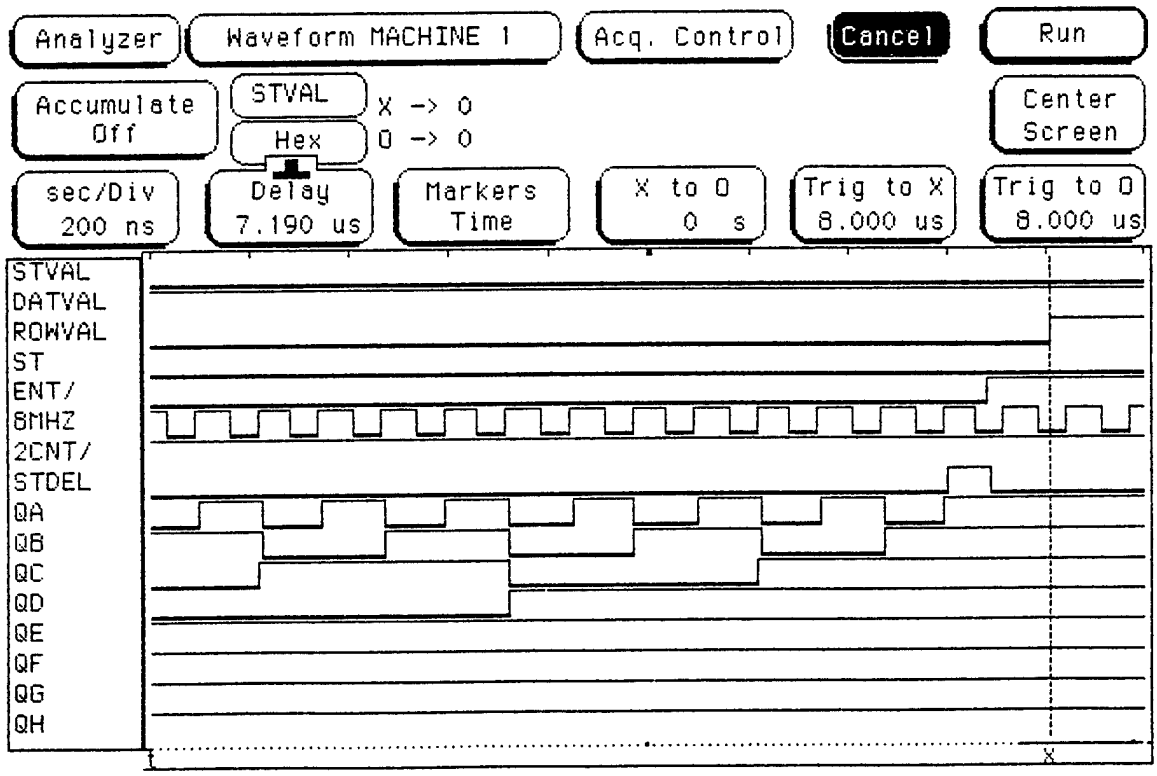


Figure 29. Counter Operation for a Line Length of 64.
(Shows end of delay.)

K. Schematic Sheet 15

All video data received from the Camera Emulator card while the YSIZE_EN signal is high, is stored in RAM. This includes the video data at the end of each row which falls outside the right boundary of the smaller frame. This data is unwanted and must be excluded when a frame is read from RAM. The SI card does this by accessing only the positions in RAM which contain valid pixel information. The counters shown on sheet 15 count the RAM enable pulses generated by the decoder shown on sheet 12. For frames of width 256, these column counters will count 256 enable pulses and then reload themselves and generate pulses LD_COUNT# and LD_COUNT. These two 100 ns pulses serve to reload the counter and disable the decoder shown on sheet 12. The column counter also controls the length of the VALID_ROW pulse (see Figure 6 on sheet 8). KILLVAL is used to terminate the VALID_ROW signal at the end of the frame. If the SI card has been instructed to capture and retransmit five status words there must be only one clock pulse between rows. If the card is capturing and sending eight status words, there must be two clock pulses between rows. This spacing between rows is controlled by adjusting the length of the LD_COUNT and LD_COUNT# pulses generated by flip flop CC49B. Delays CR41 and CV31 and multiplexer CT19 (on sheet 9) control this pulse length. Figures 22 and 23 show the spacing between rows for the five status word and eight status word modes respectively.

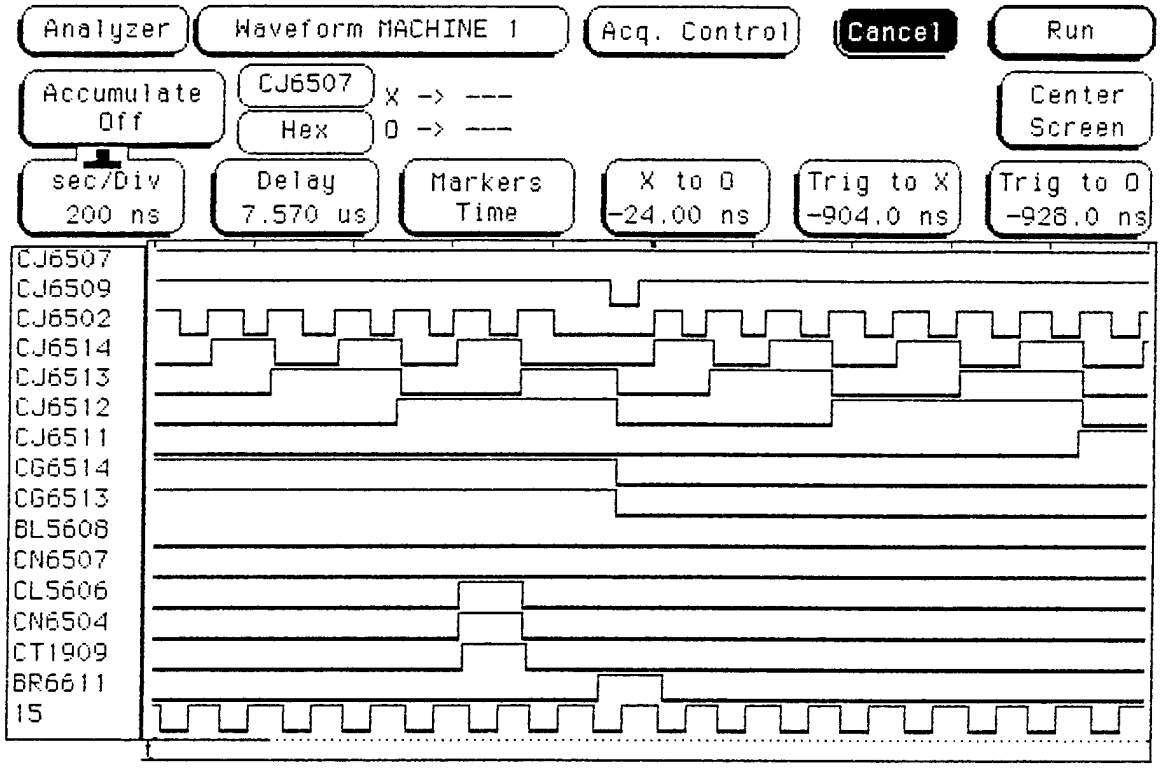


Figure 30. Spacing Between Rows when Transmitting 5 Status Words.

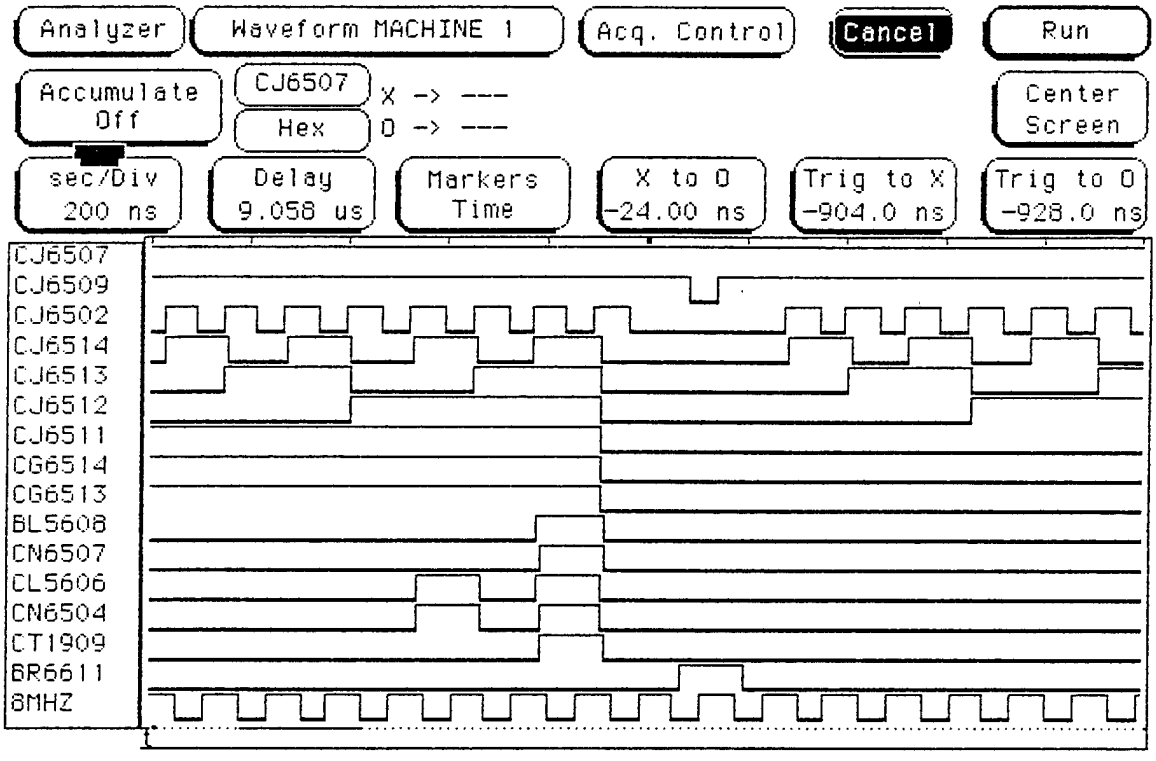


Figure 31. Spacing Between Rows when Transmitting 8 Status Words.

L. Schematic Sheet 16

Data from the RAM and the FIFOs are clocked into registers by either STATCLK# or VD#[1..5] pulses. STATCLK# clock in the status word from the FIFO while VD#[1..5] clock in data coming from the five sets of RAM. Timing of these clocks are critical with delay AL50 (shown on sheet 13) being used to adjust STATCLK# while CT01 adjusts the timing of pulses VD#1 through 5. Figures 22, 23, and 24 show timing diagrams for the 8 MHz clock, STATVAL, VDATOUT, and VALID_ROW signals sent to the Camera Monitor card.

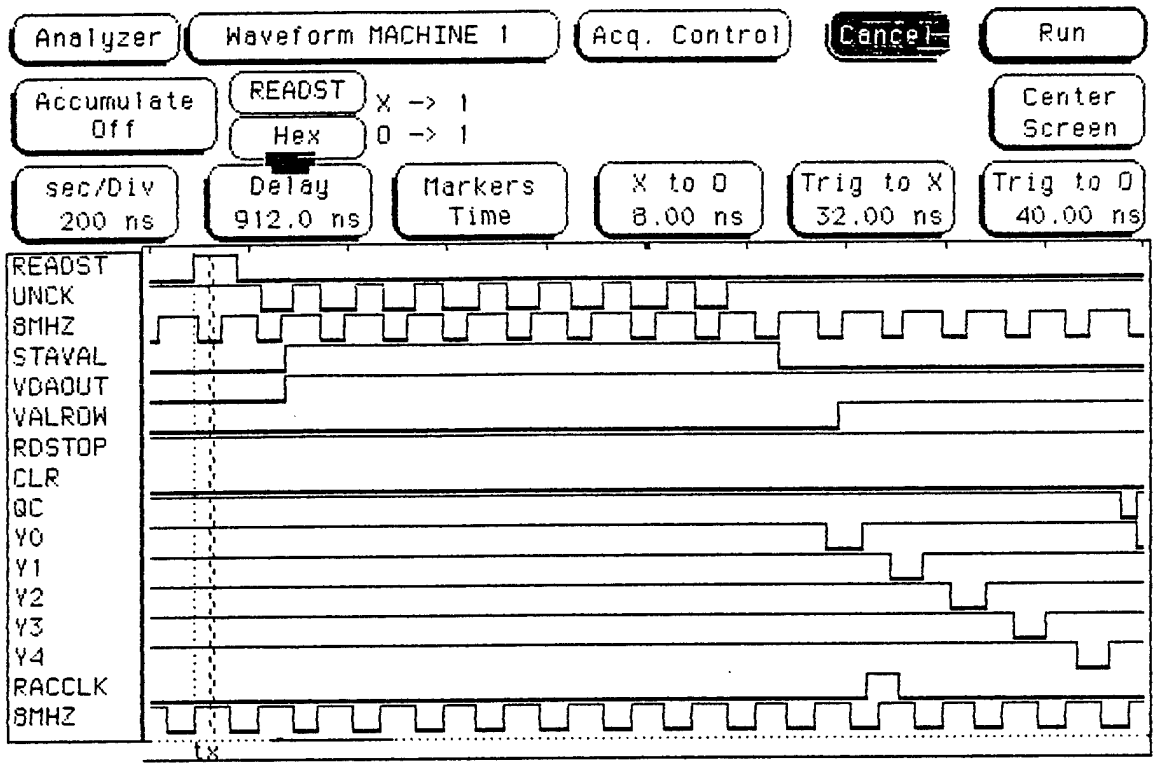


Figure 32. Timing Diagram of Data and Status Valid Lines at Start of Frame.

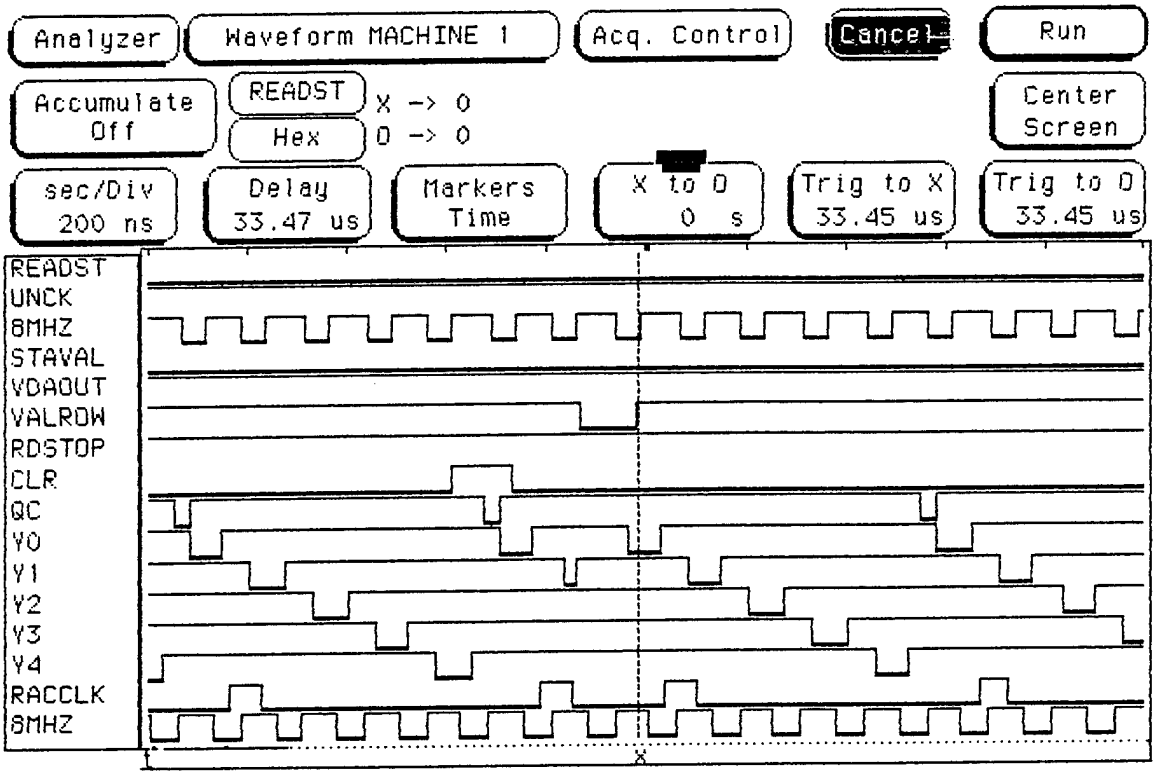


Figure 33. Timing Diagram of Data and Status Valid Lines at End of First Line

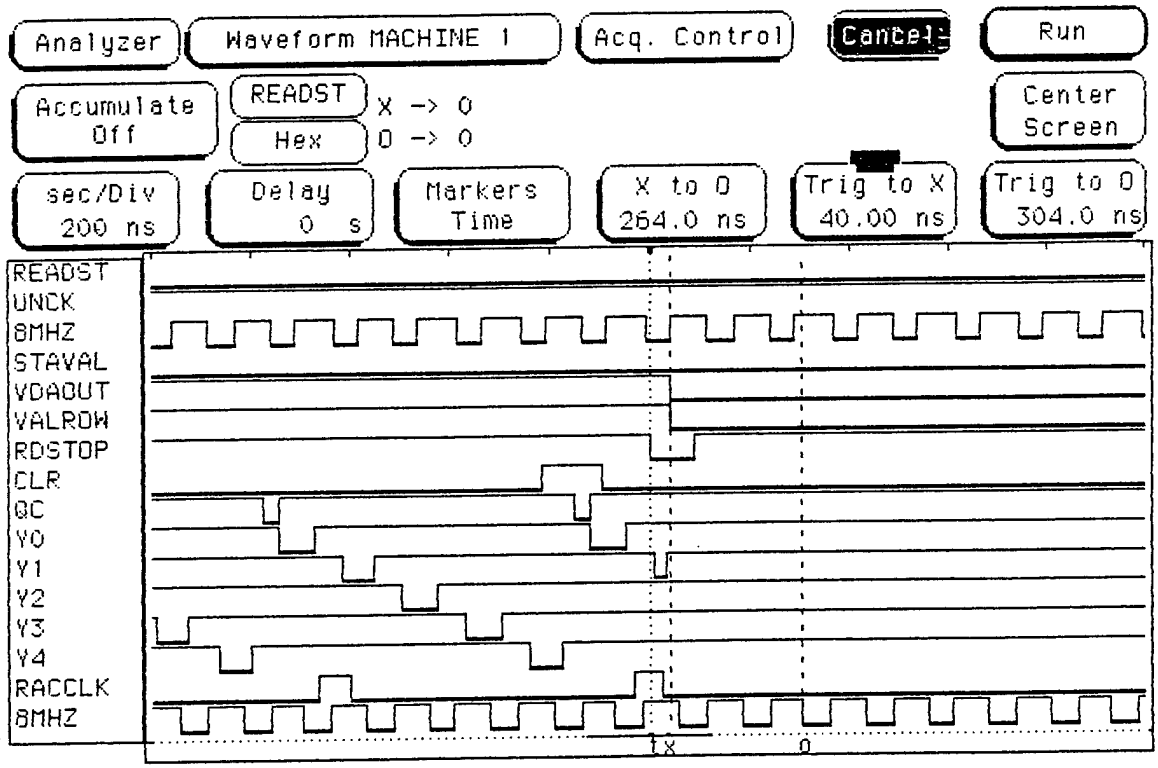


Figure 34. Timing Diagram of Data and Status Valid Lines at End of Frame.

M. Schematic Sheet 17 and Sheet X-1

Because of additional logic which needed to be added to the card and insufficient room for expansion, a second smaller card was attached to the primary card to house these circuits. Sheet 17 shows the connector from the primary to the secondary SI card and a small circuit which generates a one hundred nanosecond READ_ST2 pulse at the high to low transition of the STATVAL signal. Therefore, a new frame is sent to the Camera Monitor card each time a status word is received from the Camera Emulator card. Circuits shown on sheets 17 and X-1 work together to generate an inhibit signal (RE_ST_INH) which inhibits the generation of a READ_ST2 pulse from the time windowing down occurs until at least one entire frame has been received from the Camera Emulator card. This will ensure that the status word and frame information in the first video data after 'window down' will reflect the new smaller frame size.

This inhibit signal (RE_ST_INH) is initiated upon receiving the window down command from the incoming status word and is terminated after the completion of two events. First, a time interval of between 7 and 8 msec. must elapse as measured by counter CC65. When the window down command is received on the SI card, it is passed to software which controls the size of the frame being sent from the DVI. An 8 msec. delay was chosen to provide the software and the DVI with adequate time to change the frame size. Once the 8 msec. delay has expired, the counter enables flip flops BF35A and BF35B to begin 'watching' for the first complete YSIZE_EN pulse which is the second event which must occur before the inhibit is terminated. A complete YSIZE_EN indicates that the SI card has received an entire frame of video data at the smaller, windowed down size. Once this YSIZE_EN is received, a WD_RD_ST pulse is generated which terminates the inhibit and generates a READ_ST2 pulse which initiates the transmission of a new frame containing status and video data reflecting the new windowed down state. Timing diagrams showing the operation of these circuits can be seen in Figures 35 and 36.

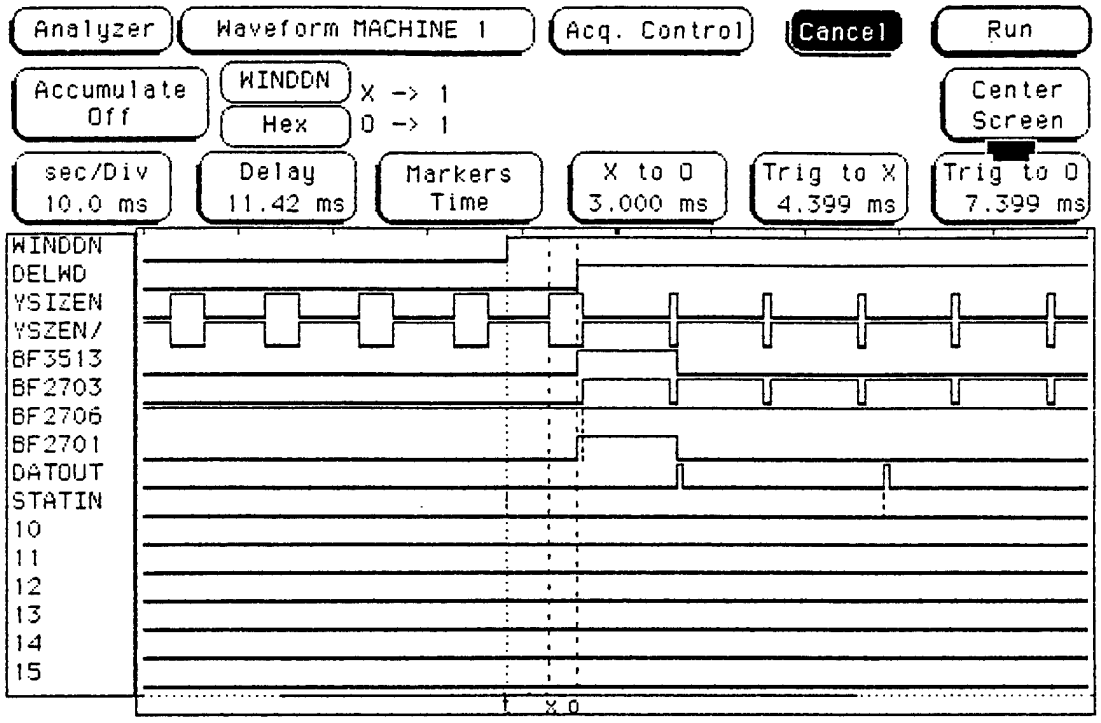


Figure 35. Timing Diagram of Read Start Inhibit Circuit. (Example 1)

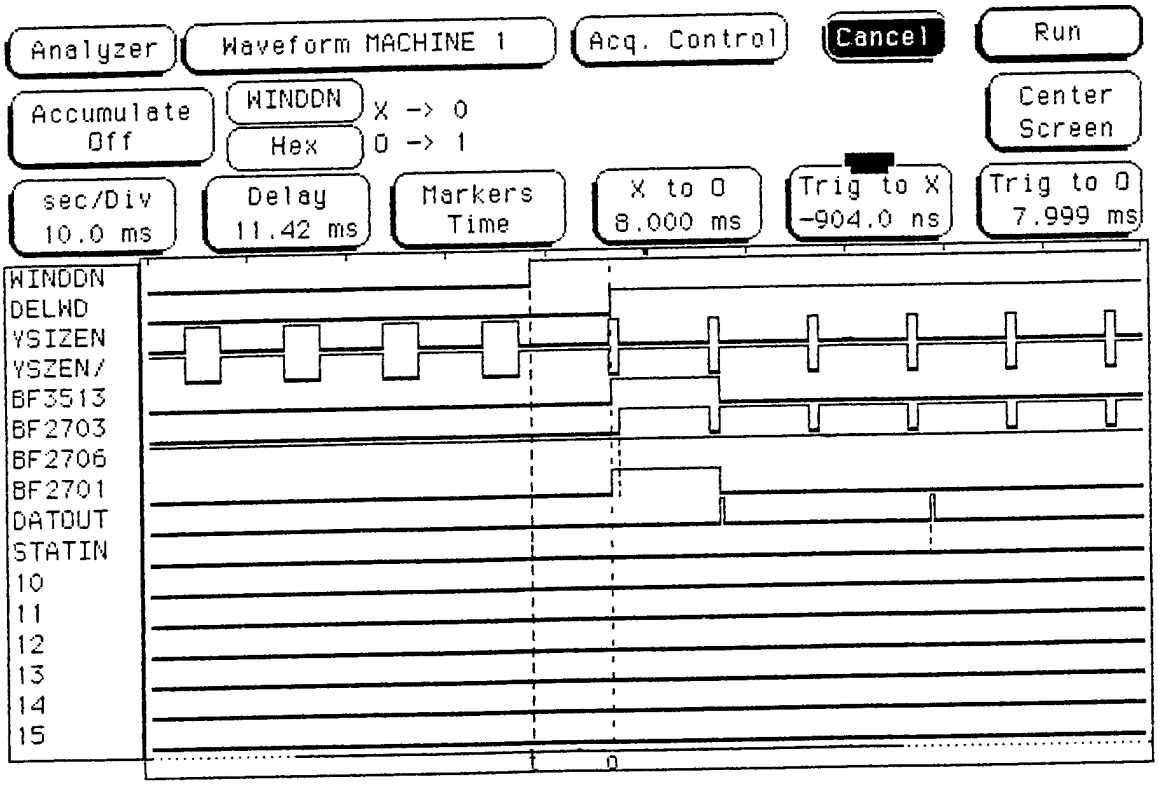


Figure 36. Timing Diagram of Read Start Inhibit Circuit. (Example 2)

Because the occurrence of the first frame after window down is determined by the arrival of the first complete frame and not the arrival of the status word, it is possible that a status word could be sent to the SI card while a frame was being sent out. This would lead to the generation of a READ_ST2 pulse and the card would try to send another frame while the last frame was being sent. To prevent this, flip flop CE55 pin 1 is held low if a status word is received while a frame is being sent. Because of the spacing between the incoming STATVAL signals and the outgoing frames, this should be the only time that flip flop CE55 would inhibit the generation of a frame.

Sheet X-1 also shows the circuits used to generate the clear (CLR) pulse and the pulse labeled ZZ#. ZZ# is discussed in the next section.

N. Schematic Sheet X-2

This sheet shows the circuit which determines which of the 5 clock pulses fall first within the boundary of a frame. (The significance of the 5 clock pulses and their association to the pixel data from the Camera Emulator card has been discussed previously.) If an arrangement of clock pulses as in Figure 7 on page 10 were received by the flip-flops shown of sheet X-2, flip flop BD43A would remain low while the other four flip-flops would transition high. The resulting word to the PAL (Programmable Array Logic) device would be 01111 for A, B, C , D, and E respectively. The PAL would interpret this five bit word and send a 100 (4 in hex) to the 74ALS161 counter shown on sheet 12. This value would serve as the starting count value for the counter during read back at the start of each row. The equations for the PAL are given below and on the schematic.

AA = (!A & !B & C & D & E) # (!A & !B & !C & !D & E)
BB = (!A & !B & C & D & E) # (!A & !B & !C & D & E)
CC = (!A & B & C & D & E)

Active low pulse ZZ# controls when the detection circuit samples the arrangement of the clock pulses. ZZ# clears the flip flops twice during a simulation, once at the very beginning and a second time immediately after the 8 msec. delay if no frame is being received from the DVI. If the DVI is sending a frame of data, ZZ# will be generated immediately after YSIZE_EN# transitions to high. ZZ# occurring at this time ensures that the 'first pulse' detection circuit will properly sense the first pulse of each line of the smaller frame.

O. Operational Modes

The SI card is designed to switch between several different modes depending upon frame size, row length and the number of status words. Multiplexers are used to separate the different parameters required for each mode.

The SI card samples the incoming status words from the Camera Emulator card to detect when the card should begin transmitting the smaller frame size. This detection circuit is shown on sheet 13. When the 'window down' condition is indicated, WINDDN# transitions to low which produces several changes. First, multiplexers (shown on sheets 12 and 15) are commanded to select the A port which changes the order in which the RAM is accessed. The B port selects RAM access strobes for the longer row associated with the larger frame size while the A port selects strobes for the shorter row associated with the smaller frame size. The order of the strobes must change, not because the length of the row changes but because the number of pixels in a row, when divided by five, have a different remainder. For example, a row with 258 pixels in it has a remainder of three, after dividing by five while a row with 57 has a remainder of two, after dividing by five. The RAM access order would be different for these two row lengths. The multiplexers CR65 and CN65 provide the different RAM access order. If on the other hand, one row contained 258 pixels and the windowed down row contained 63 pixels, the RAM access order would not change because the remainder in both cases would be three. The WINDDN# signal also immediately activates a circuit which causes the card to ignore all incoming frames from the Camera Emulator card for the next 7 to 8 msec. At the end of this time, the card will 'look' at the next complete frame and use this frame to detect which pixel is first in the row because the first pixel in the row may change after 'window down' occurs. These circuits are shown on sheets 17, X-1, and X-2.

Row length will vary depending upon frame size and the number of status words selected to accompany the transmitted video data. The SI card must keep count of the number of pixels of transmitted video data in each row because there must be separation between each row. The counters shown on sheet 15 count the transmitted pixels to ensure that each row is the proper length. Multiplexers CN65 (sheet 15) and CT19 (sheet 9) select the correct count value based upon frame size and number of status words.

A switch, S1, shown on sheet 9, selects the number of status words. If five status words are to be sent with the video data, there must be two clock pulses between transmitted rows and a space between the status word and the first transmitted row approximately equal to the transmission time of one row minus 5 clock pulses. This delay must occur for both the large and small frame sizes. If eight status words are to accompany each frame of video data, there is one

clock pulse between transmitted rows and only one clock pulse between the status word and the first row of video data. The number of status words is controlled by circuits shown on sheet 9. The spacing between rows is controlled by switching in and out fixed delays and varying the length of LD_COUNT shown on sheet 15. The variable delay between the status word and the first row is activated by switching multiplexer CL49 shown on sheet 9. The counter CN49 serves as the delay counting from a preset start value up to 255. The start value is determined from programmable 8-bit dip switches and multiplexers shown on sheet X-2. The delay counter is only enabled when the card is selected to generate five status words.

VII. CONCLUSION

This signal injection card has been built and has gone through a thorough checkout to prove that it is fully operational and that it transmits to the Camera Emulator card and the IAP an exact representation of the frame which the card receives from the DVI as well as an exact copy of the status information from the Camera Monitor card. This signal injection card has been used many times to transmit simulated run scenarios to the IAP for simulation testing. This card has given the THAAD Simulation Facility the capability of testing the THAAD IAP in a variety of different flight scenarios, in order to better understand the operation of the missile system as a whole.

LIST OF ABBREVIATIONS

AD	Air Defense
ADR	Address lines for RAM
ASC	Advanced Simulation Center
AWACS	Airborne Warning and Control System
BANK1_WEN	Signal which enables writing to Bank 1 of RAM
BANK2_WEN	Signal which enables writing to Bank 2 of RAM
CLK	Clock
CLR	Clear Pulse
CEL	Chip Enable Left - Enable pulse for left port of RAM
DACS	Divert and Attitude Control Systems
DOF	Degrees of Freedom
DVI	Digital Video Interface
FIFO	First in First out Register - used to hold the status words
FMS	Flight Motion Simulator
FTV	Flight Test Vehicle
GPS	Global Positioning System
HEMTT	Heavy Equipment Mobile Tactical Truck
HMMWW	High Mobility Multipurpose Wheeled Vehicle
HTK	Hit to Kill
HWIL	Hardware-in-the-Loop
IAP	Integrated Avionics Package
IER	Interface Equipment Rack
IR	Infrared
IRSG	Infrared Scene Generation
IRSS	Imaging Infrared System Simulation
JSTARS	Joint Surveillance Tracking and Acquisition Radar System
JTIDS	Joint Tactical Information Distribution System
KV	Kill Vehicle
LCS	Launcher Control Station
LDCKEN	Load Clock Enable
LDAP	Laser Diode Array Projector

LIST OF ABBREVIATIONS

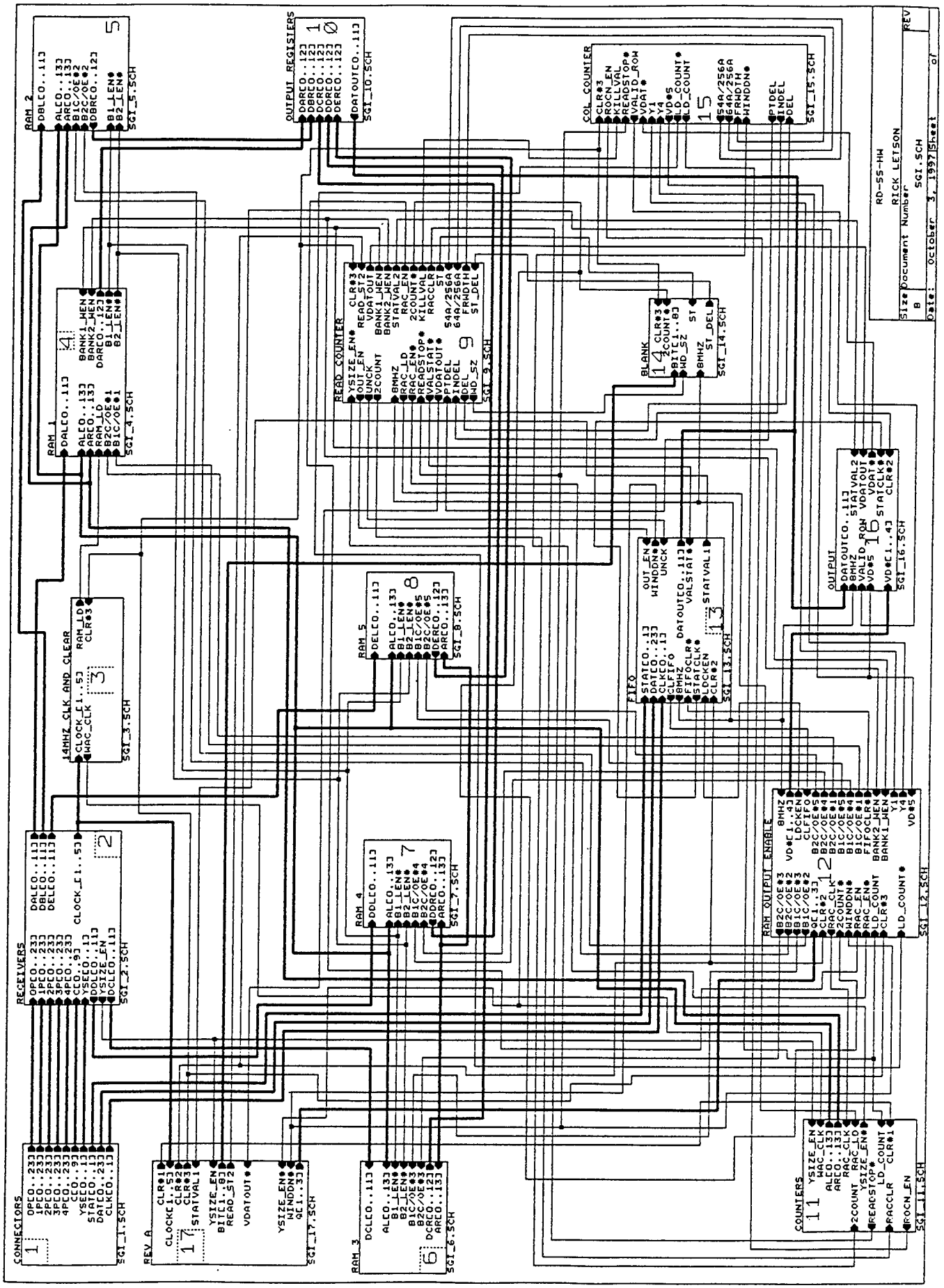
METS	Integrated Meteorological System
MRDEC	Missile Research, Development, and Engineering Center
MWIR	Mid Wave Infrared
PLS	Palletized Load System
RAC_CLK	Clock for the Read address counters
RAC_LD	Load strobe for the Read Address Counters
RAM	Random Access Memory
RAM_LD	RAM Load pulse
READ_ST2	Active high pulse which commands the card to send status and data
RF	Radio Frequency
ROWVAL	Row Valid - Signal which indicates the beginning and end of a row
R/WL	Read/Write strobe for RAM - Read is active high and write is active low
SI	Signal Injection
SHARP	Sensor Hand-over and Risk Reduction Program
SPDT	Single pole double throw switch
SSI	Sensor System Interface
STATVAL	Signal indicating valid status information
TAOC	Tactical Air Operation System
TACS	Tactical Air Control System
TBS	Theater Ballistic Missile
TENCAP	Tactical Exploitation of National Capabilities
THAAD	Theater High Altitude Area Defense
TOC	Tactical Operations Center
TOS	Tactical Operations Station
TOM	Target Object Map
TPO	THAAD Project Office
TVC	Thrust Vector Control
UNCK	Signal to clock data out of the FIFO
UOES	User Operational Evaluated System
USAMCOM	U.S. Army Aviation and Missile Command
VALSTAT	Valid Status signal
WAC_CLK	Write address counter clock - addresses the left port of RAM
WINDDN	Window Down
YSIZEN	Y size enable - Active high signal indicating data is being transmitted from the DVI

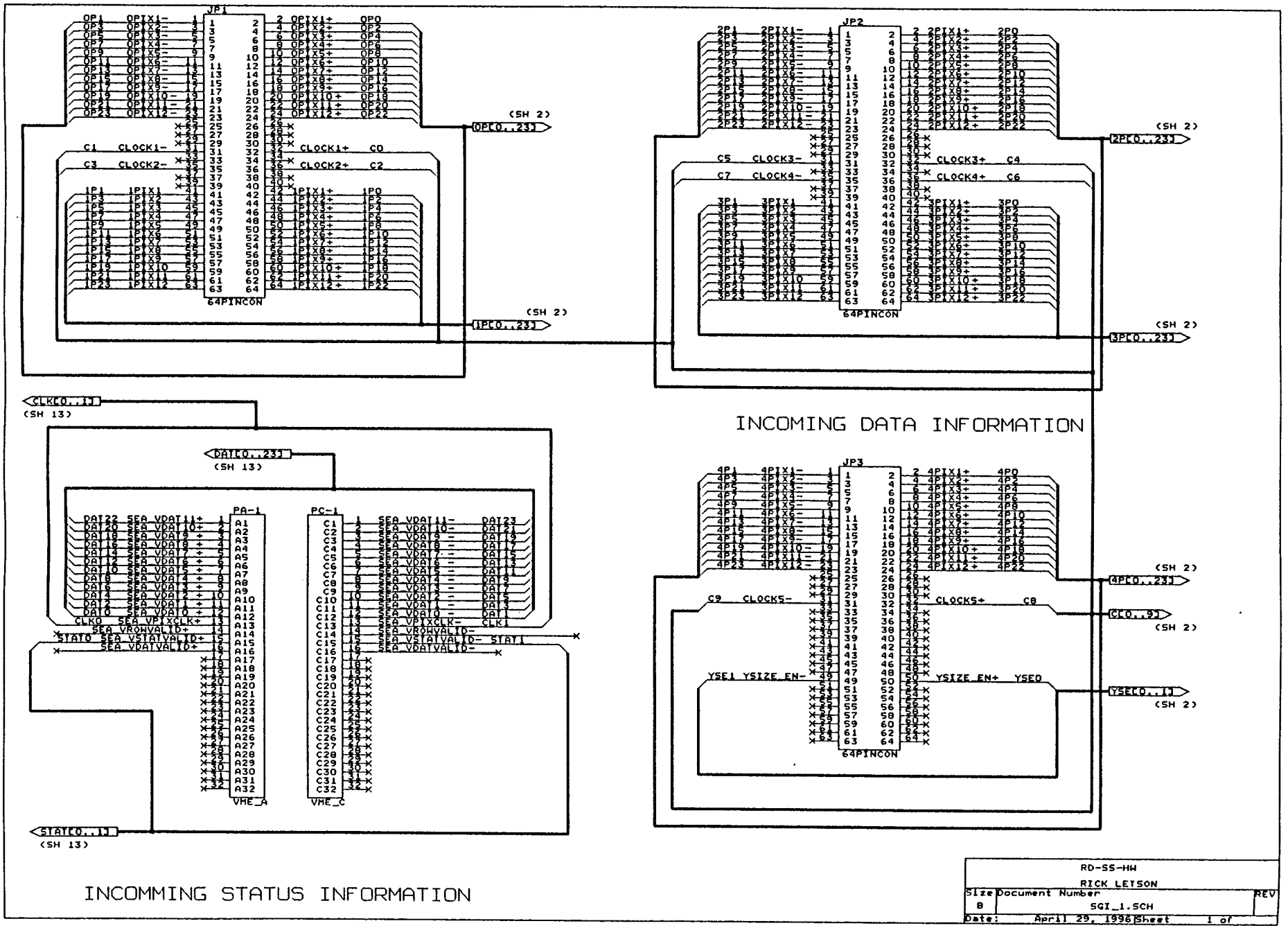
APPENDIX

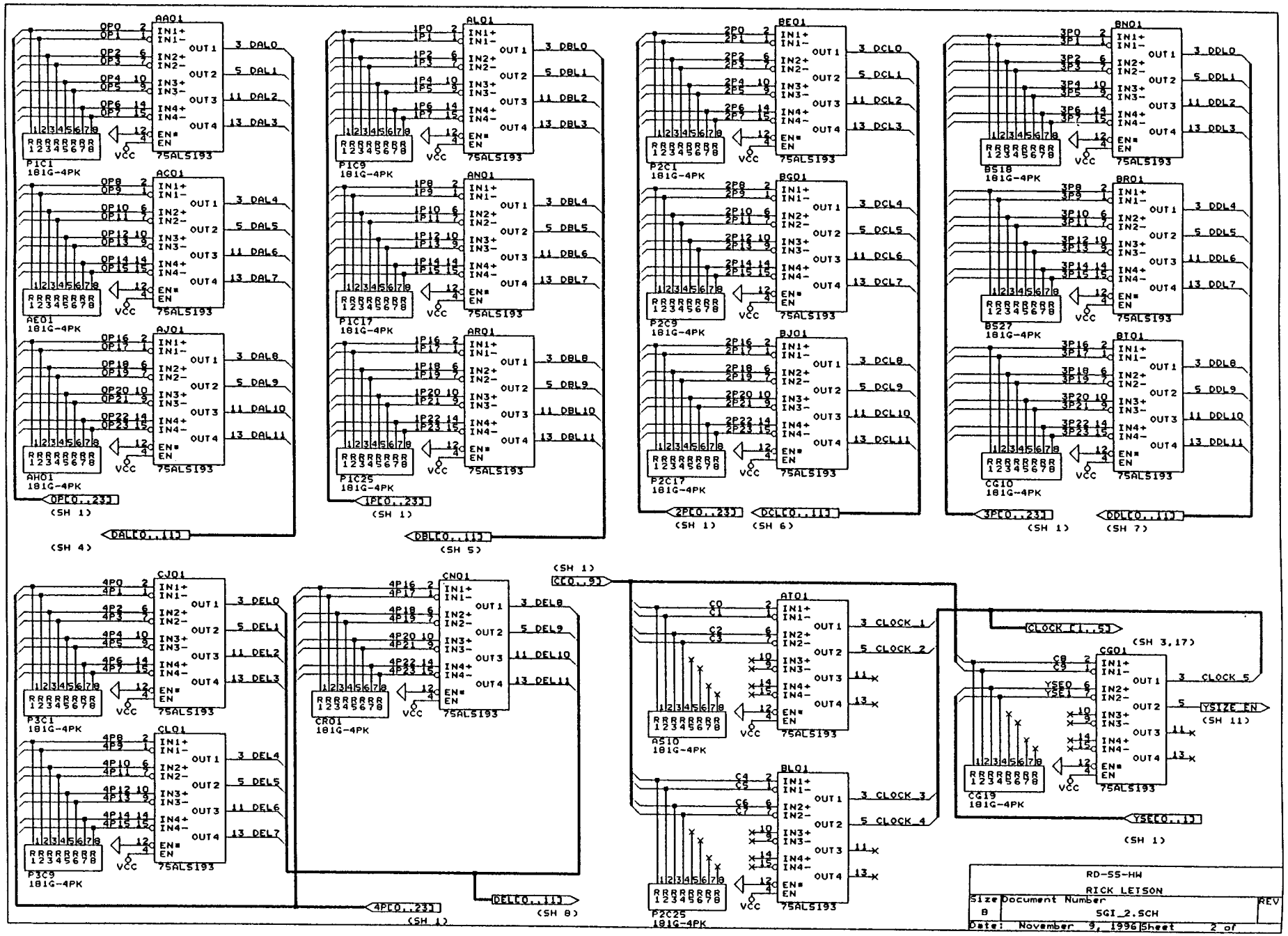
SCHEMATICS FOR THE THAAD SIGNAL INJECTION CARD

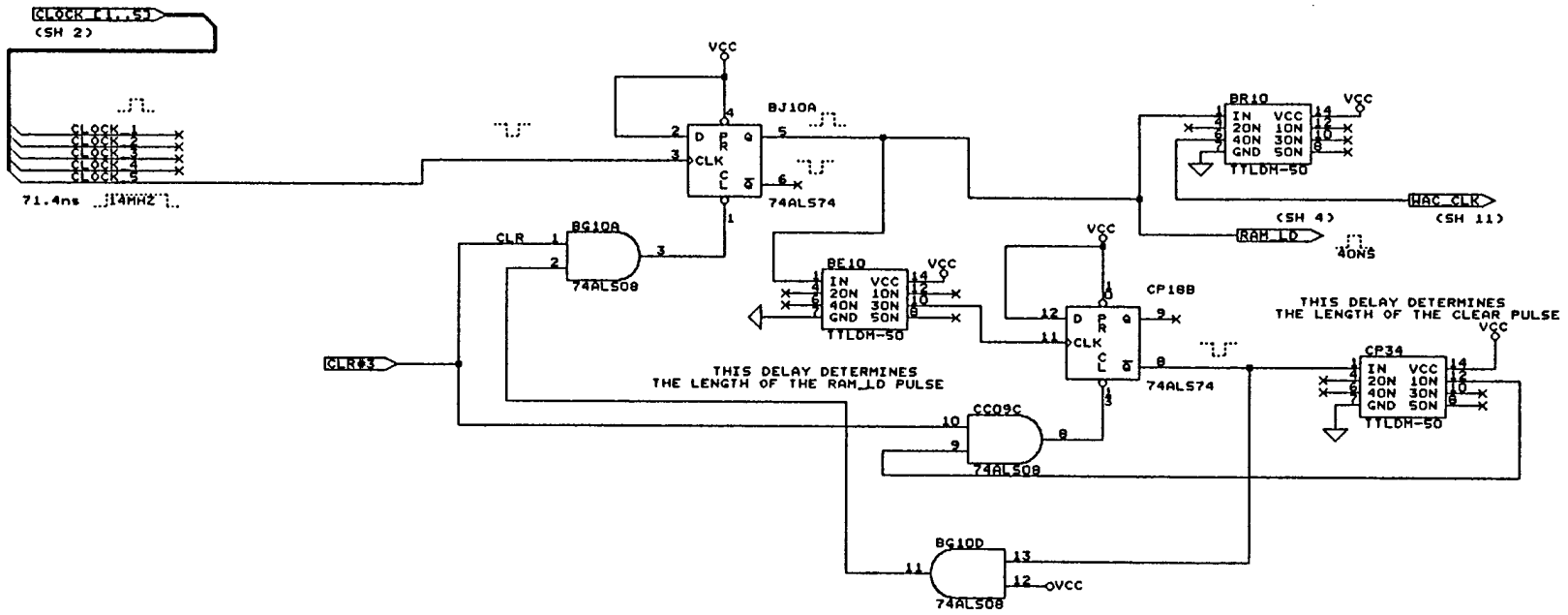
APPENDIX
SCHEMATICS FOR THE THAAD SIGNAL INJECTION CARD

Schematics for the Signal Injection card are included in the Appendix. They consist of a total of 21 pages including two root sheets showing the electrical connections for the two circuit cards which make up the Signal Injection card.

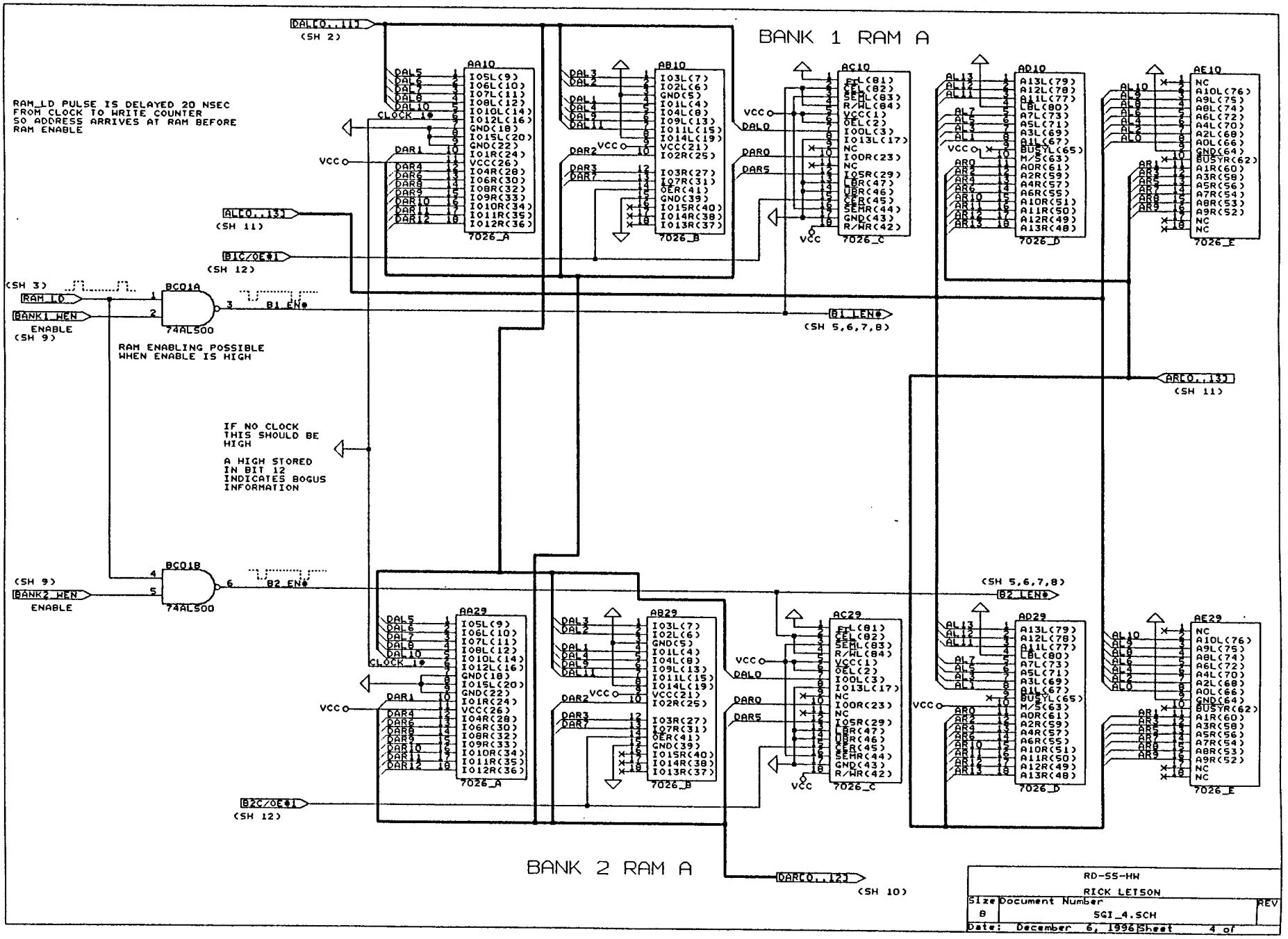


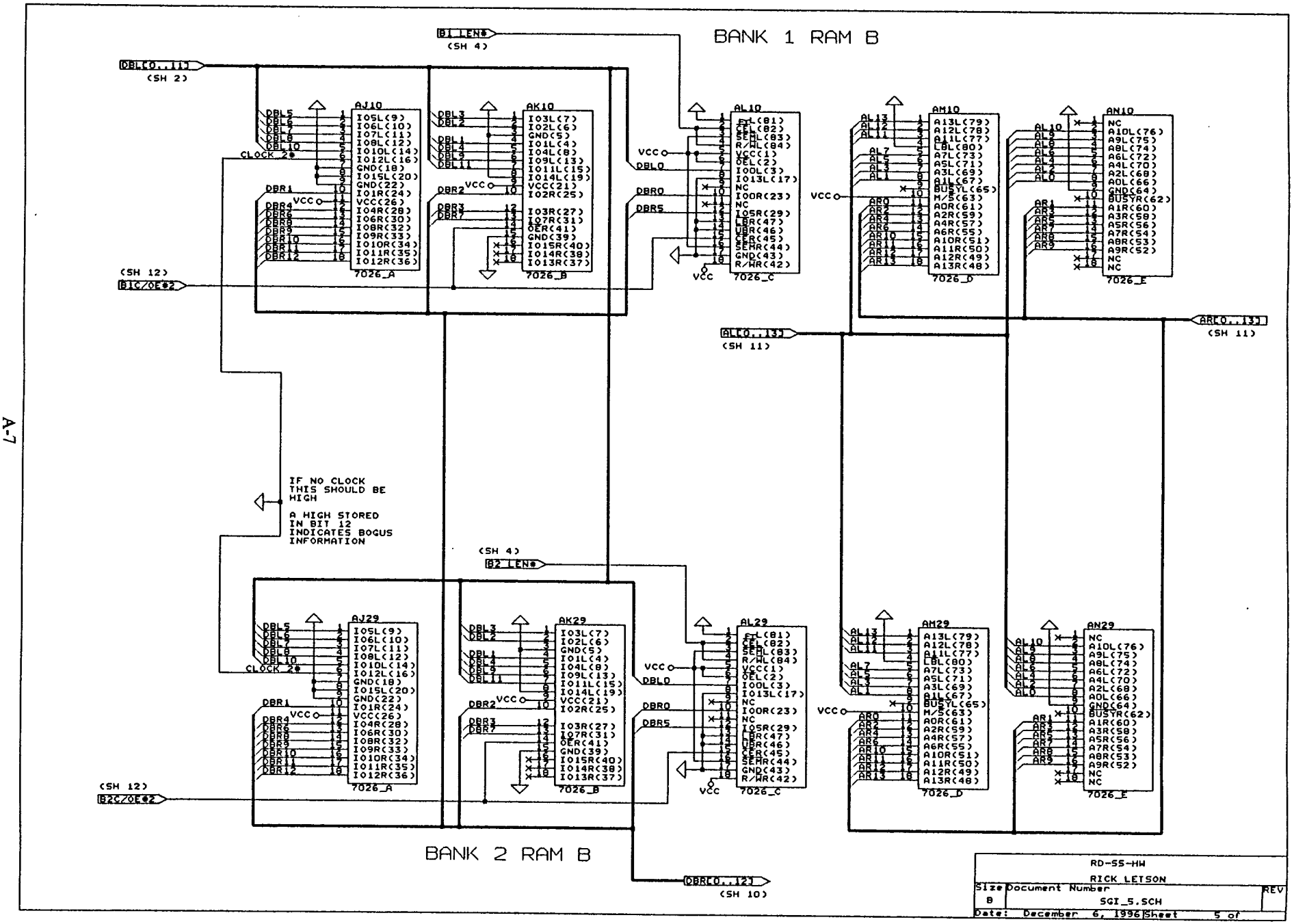

JP1
64PINCON
(SH 2)
0PI[0..23]
1PI[0..23]
JP2
2PI[0..23]
3PI[0..23]
INCOMING DATA INFORMATION
CLK[0..1]
(SH 13)
DAT[0..23]
PA-1
PC-1
VME_A
VME_C
STAT[0..1]
INCOMMING STATUS INFORMATION
JP3
4PI[0..23]
CLO..9]
YSE[0..1]
RD-SS-HW
RICK LEYSON
Size B
Document Number SGI_1.SCH
REV
Date: April 29, 1996 Sheet 1 of

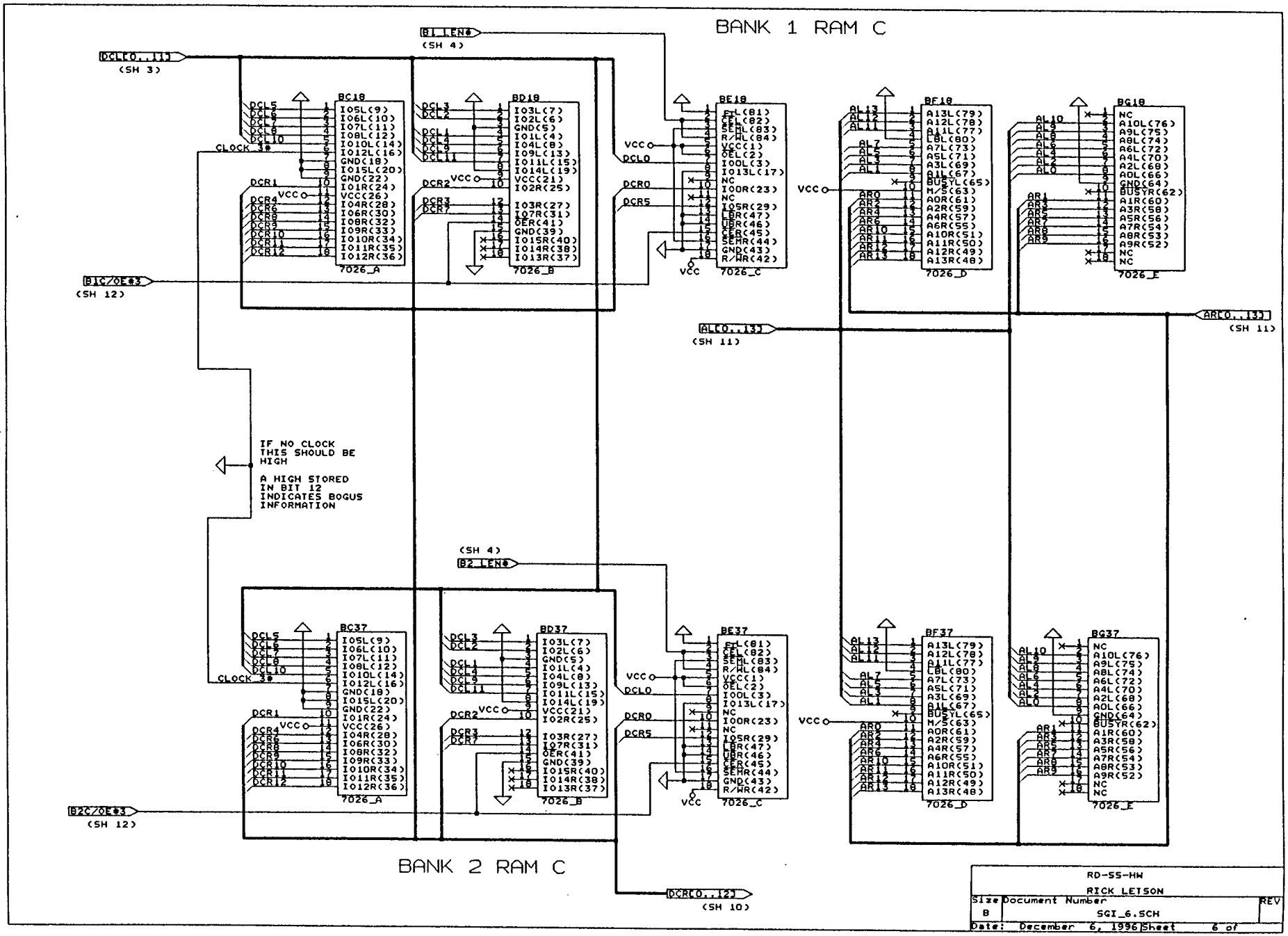

AA01
AC01
AE01
AG01
AH01
AL01
AN01
AQ01
AR01
BE01
BG01
BJ01
BN01
BR01
BT01
CG10
CG27
CJ01
CL01
CN01
CR01
AT01
AS10
BL01
CG01
CG19
P3C1
P3C9
P2C1
P2C9
P2C17
P2C25
PIC1
PIC9
PIC17
PIC25
75ALS193
181G-4PK
OPC0..23]
1PC0..23]
2PC0..23]
3PC0..23]
4PC0..23]
DALC0..11]
DBLC0..11]
DCLC0..11]
DDLC0..11]
DELC0..11]
CC0..9]
CLOCK [1..5]
YSEC0..1]
YSIZE_EN
(SH 1)
(SH 3,17)
(SH 4)
(SH 5)
(SH 6)
(SH 7)
(SH 8)
(SH 11)
RD-SS-HW
RICK LEISON
Size B
Document Number SGI_2.SCH
REV
Date: November 9, 1996
Sheet 2 of

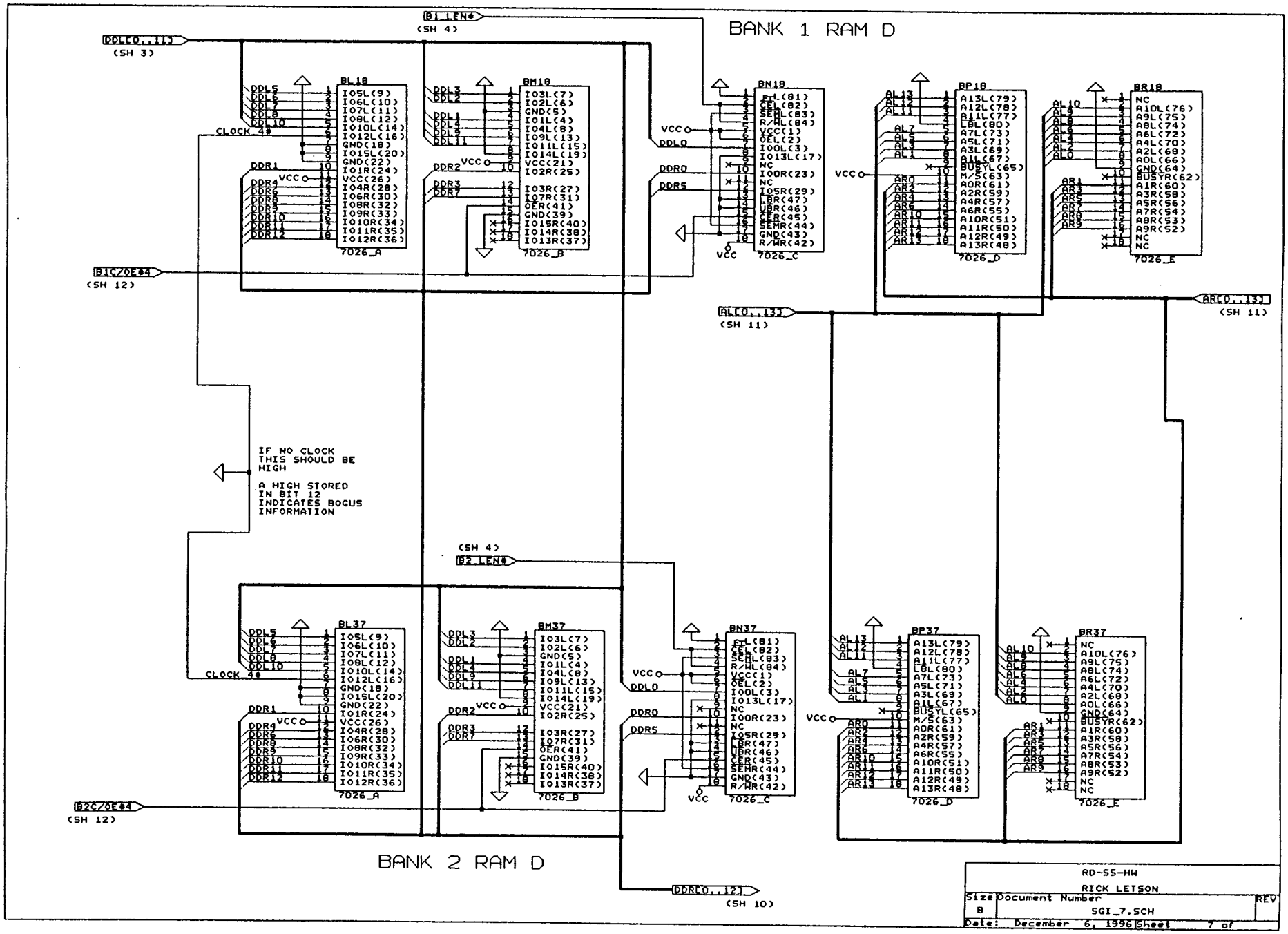


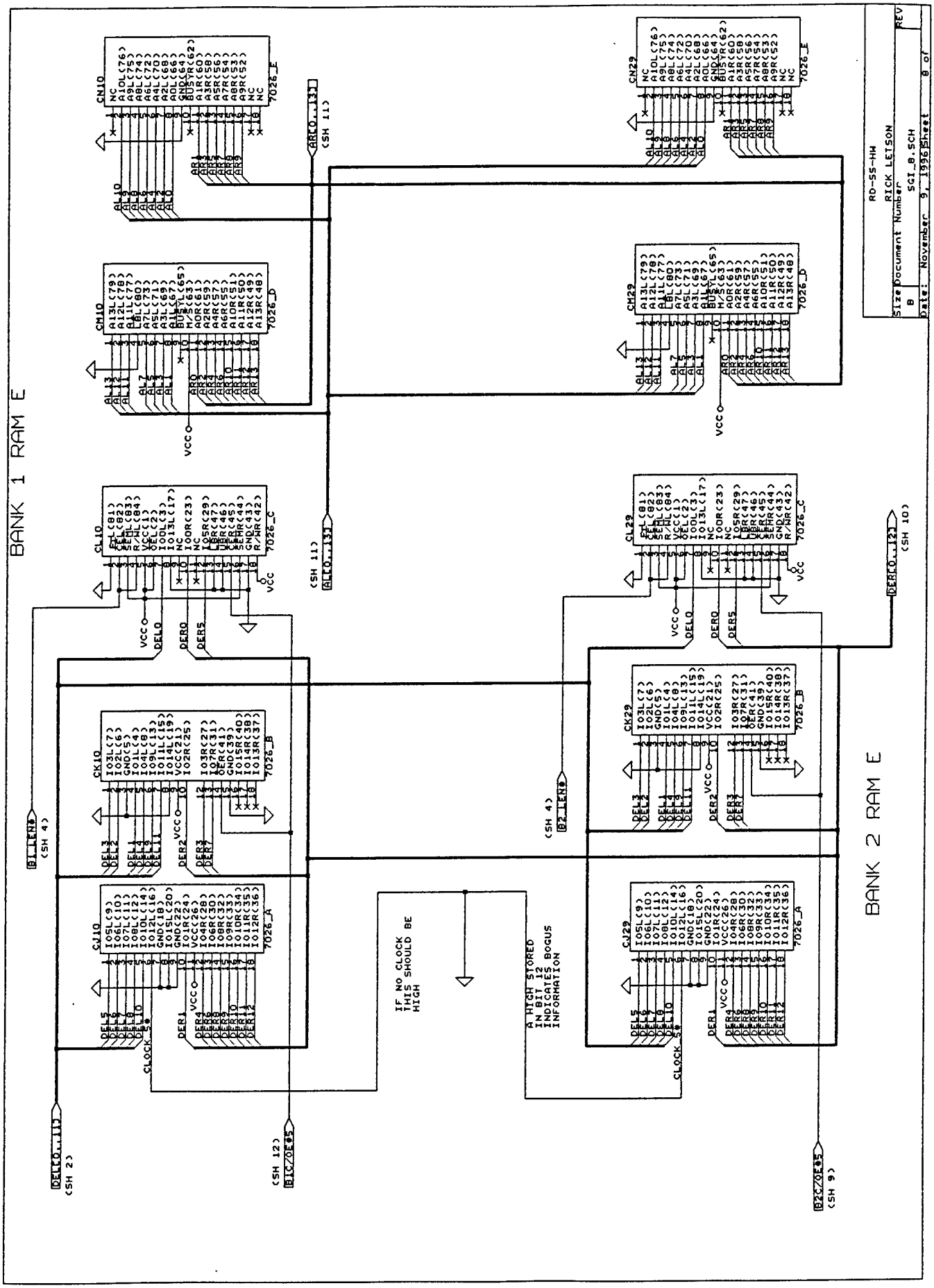
RD-SS-HW		
RICK LETSON		
Size: B	Document Number: SGI_3.SCH	REV
Date: October 30, 1997	Sheet 3 of	

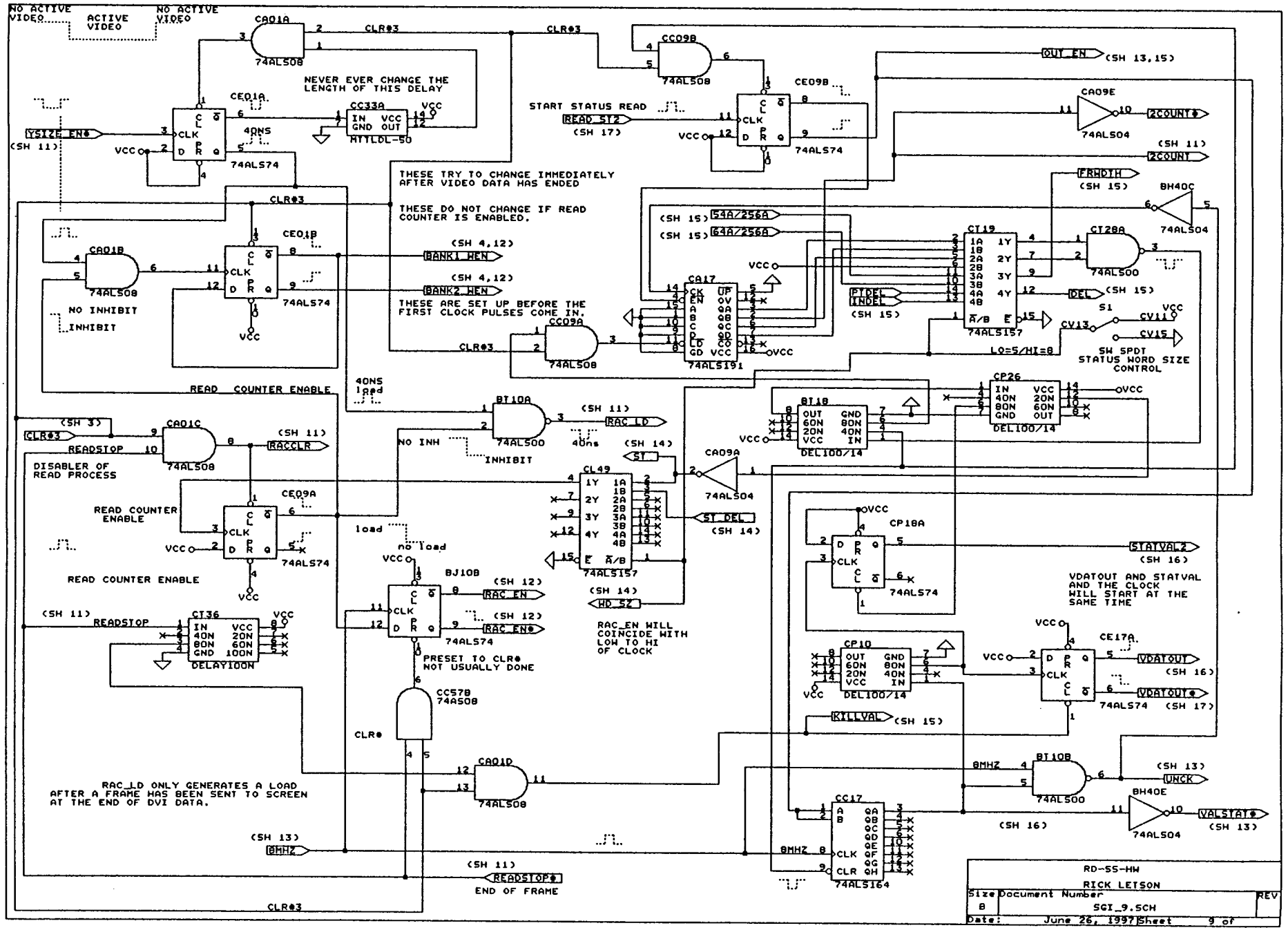

BANK 1 RAM A
BANK 2 RAM A
DAL[0..11]
(SH 2)
RAM_LD PULSE IS DELAYED 20 NSEC FROM CLOCK TO WRITE COUNTER SO ADDRESS ARRIVES AT RAM BEFORE RAM ENABLE
AA10
AB10
AC10
AD10
AE10
7026_A
7026_B
7026_C
7026_D
7026_E
VCC
CLOCK_1*
DAR1
DAR2
DAR3
DAL0
DAR0
DAR5
AL[0..13]
(SH 11)
B1C/OE*1
(SH 12)
(SH 3)
RAM_LD
BANK1_WEN
ENABLE
(SH 9)
BC01A
74AL500
B1_EN*
B1_LEN*
(SH 5,6,7,8)
RAM ENABLING POSSIBLE WHEN ENABLE IS HIGH
AR[0..13]
(SH 11)
IF NO CLOCK THIS SHOULD BE HIGH
A HIGH STORED IN BIT 12 INDICATES BOGUS INFORMATION
BC01B
BANK2_WEN
ENABLE
B2_EN*
B2_LEN*
AA29
AB29
AC29
AD29
AE29
B2C/OE*1
(SH 12)
DAR[0..12]
(SH 10)
RD-SS-HW
RICK LETSON
Size B
Document Number SGI_4.SCH
REV
Date: December 6, 1996
Sheet 4 of

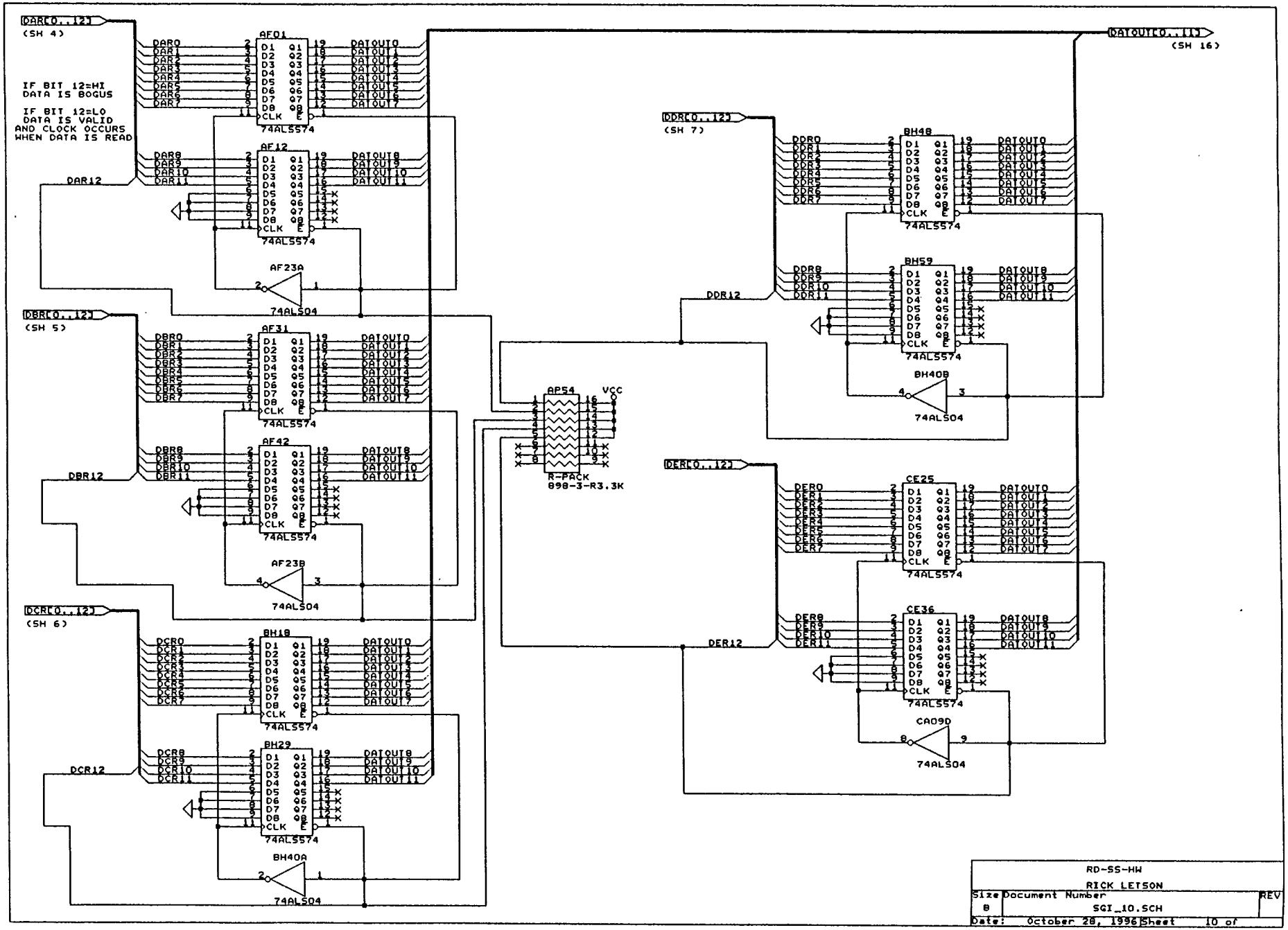

BANK 1 RAM B
B1_LEN#
(SH 4)
DBL[0..11]
(SH 2)
AJ10
AK10
AL10
AM10
AN10
7026_A
7026_B
7026_C
7026_D
7026_E
CLOCK_2#
VCC
DBL0
DBR0
DBR5
(SH 12)
B1C/0E#2
ALL[0..13]
(SH 11)
AR[0..13]
(SH 11)
IF NO CLOCK
THIS SHOULD BE
HIGH
A HIGH STORED
IN BIT 12
INDICATES BOGUS
INFORMATION
(SH 4)
B2_LEN#
AJ29
AK29
AL29
AM29
AN29
(SH 12)
B2C/0E#2
BANK 2 RAM B
DBR[0..12]
(SH 10)
RD-SS-HW
RICK LETSON
Size
B
Document Number
SGI_5.SCH
REV
Date: December 6, 1996
Sheet 5 of

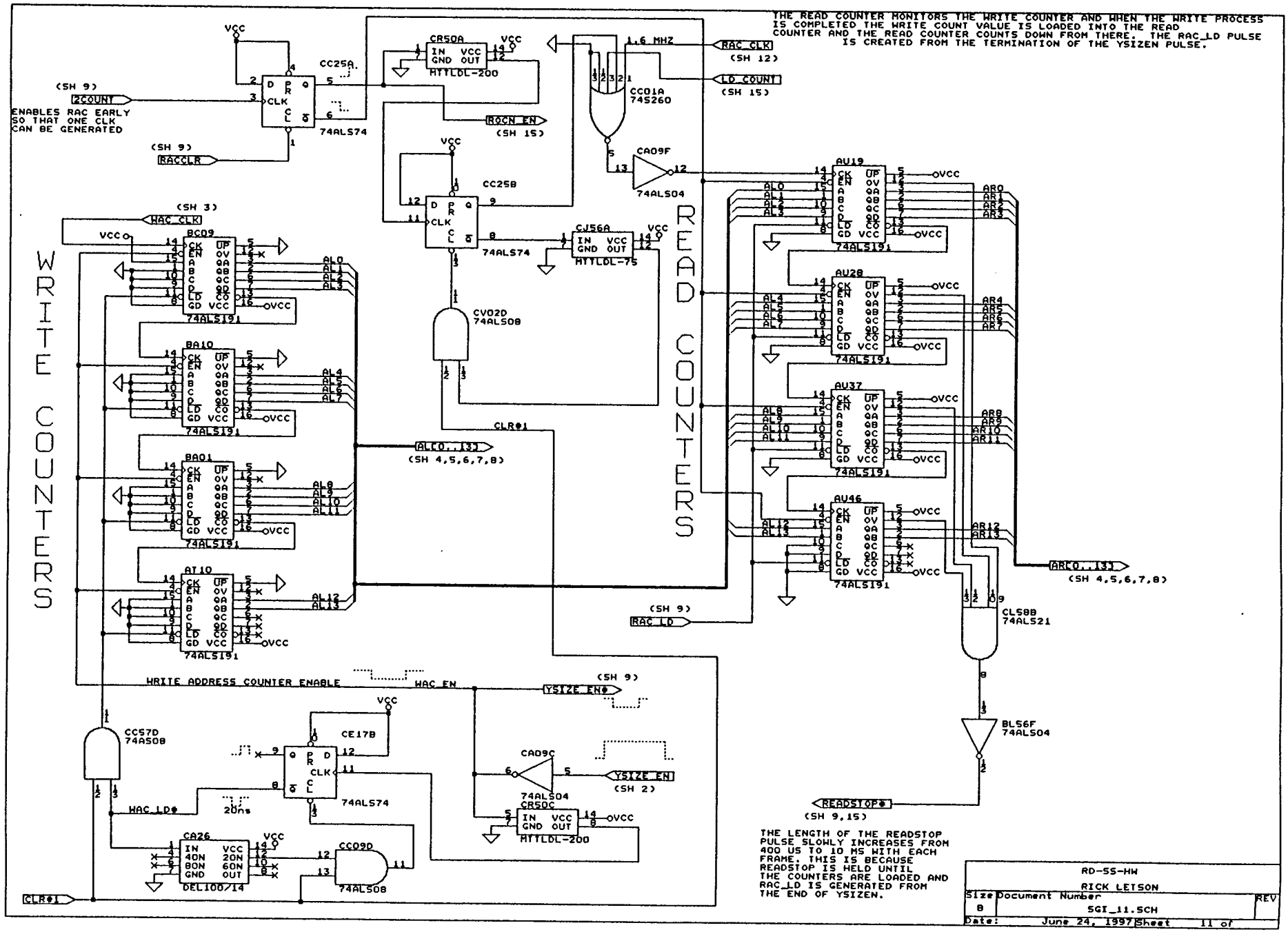

BANK 1 RAM C
B1_LEN#
(SH 4)
DCL[0..11]
(SH 3)
BC18
BD18
BE18
BF18
BG18
7026_A
7026_B
7026_C
7026_D
7026_E
CLOCK 3#
DCR1
DCR2
VCC
DCL0
DCR0
DCR5
B1C/OE#3
(SH 12)
AL[0..13]
(SH 11)
AR[0..13]
(SH 11)
IF NO CLOCK
THIS SHOULD BE
HIGH
A HIGH STORED
IN BIT 12
INDICATES BOGUS
INFORMATION
(SH 4)
B2_LEN#
BC37
BD37
BE37
BF37
BG37
B2C/OE#3
(SH 12)
BANK 2 RAM C
DCR[0..12]
(SH 10)
RD-SS-HW
RICK LETSON
Size B
Document Number
SGI_6.SCH
REV
Date: December 6, 1996 Sheet 6 of

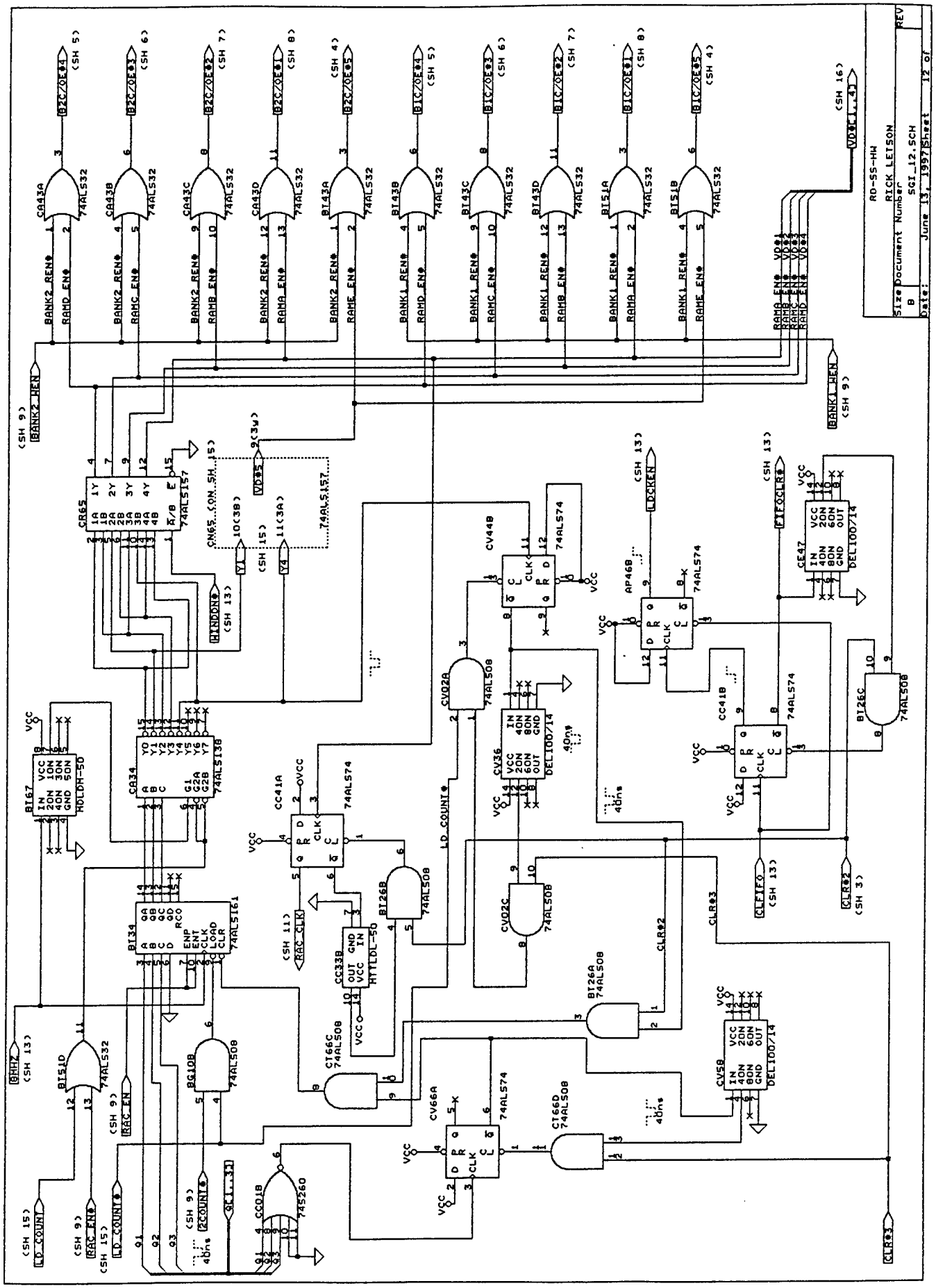

BANK 1 RAM D
B1_LEN#
(SH 4)
DDLC0..11
(SH 3)
BL18
BM18
BN18
BP18
BR18
7026_A
7026_B
7026_C
7026_D
7026_E
CLOCK_4#
VCC
DDLO
DDR0
DDR5
DDR1
DDR2
B1C70E#4
(SH 12)
ALC0..13
(SH 11)
ARC0..13
(SH 11)
IF NO CLOCK
THIS SHOULD BE
HIGH
A HIGH STORED
IN BIT 12
INDICATES BOGUS
INFORMATION
(SH 4)
B2_LEN#
BL37
BM37
BN37
BP37
BR37
B2C70E#4
(SH 12)
BANK 2 RAM D
DDRC0..12
(SH 10)
RD-SS-HW
RICK LETSON
Size B
Document Number SGI_7.SCH
REV
Date: December 6, 1996 Sheet 7 of

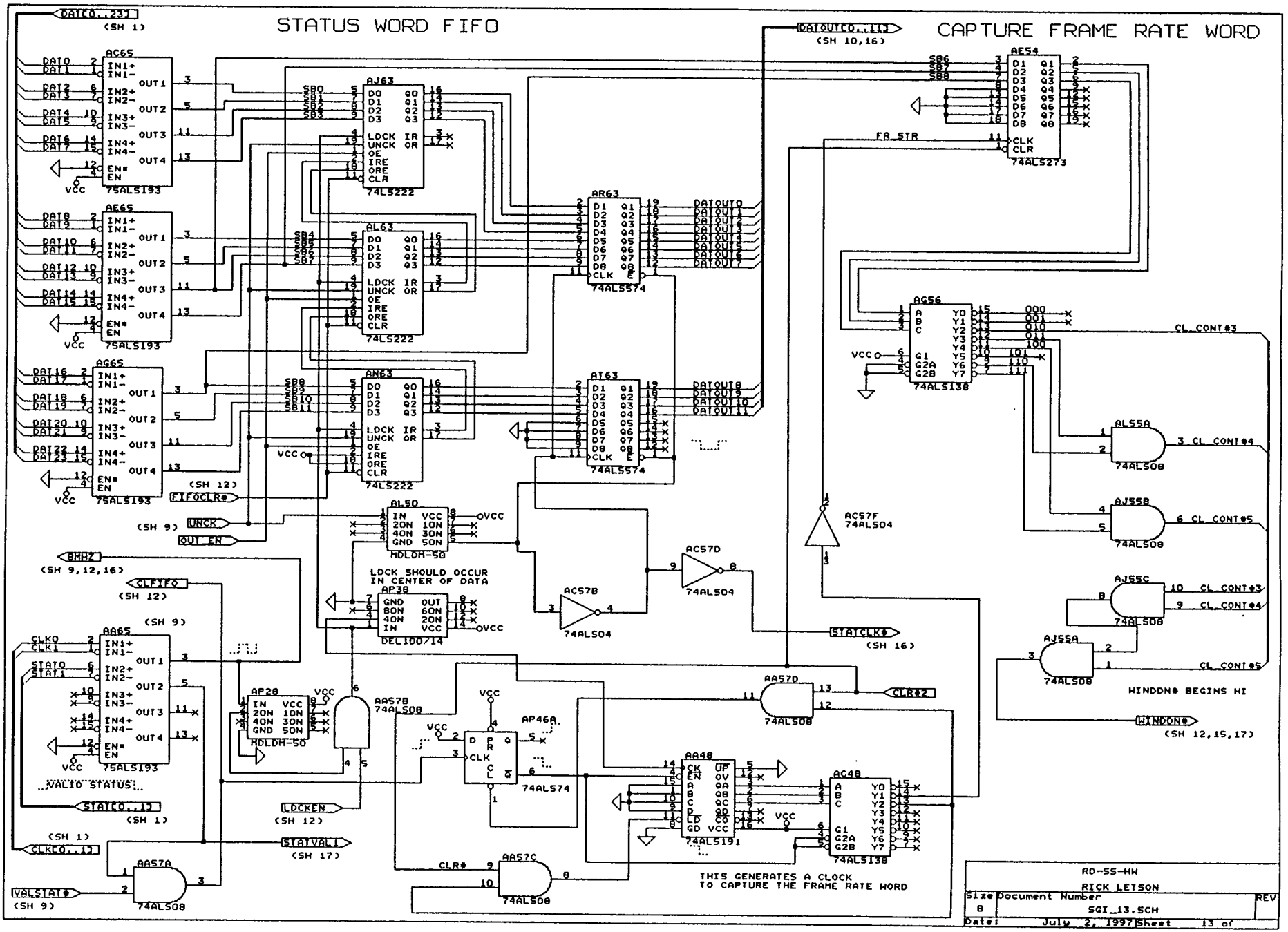

BANK 1 RAM E
BANK 2 RAM E
RD-55-HW
RICK LETSON
Size Document Number REV
B SCI_8.SCH
Date: November 9, 1996 Sheet 8 of
IF NO CLOCK
THIS SHOULD BE
HIGH
A HIGH STORED
IN BIT 12
INDICATES BOGUS
INFORMATION
7026_A
7026_B
7026_C
7026_D
7026_E

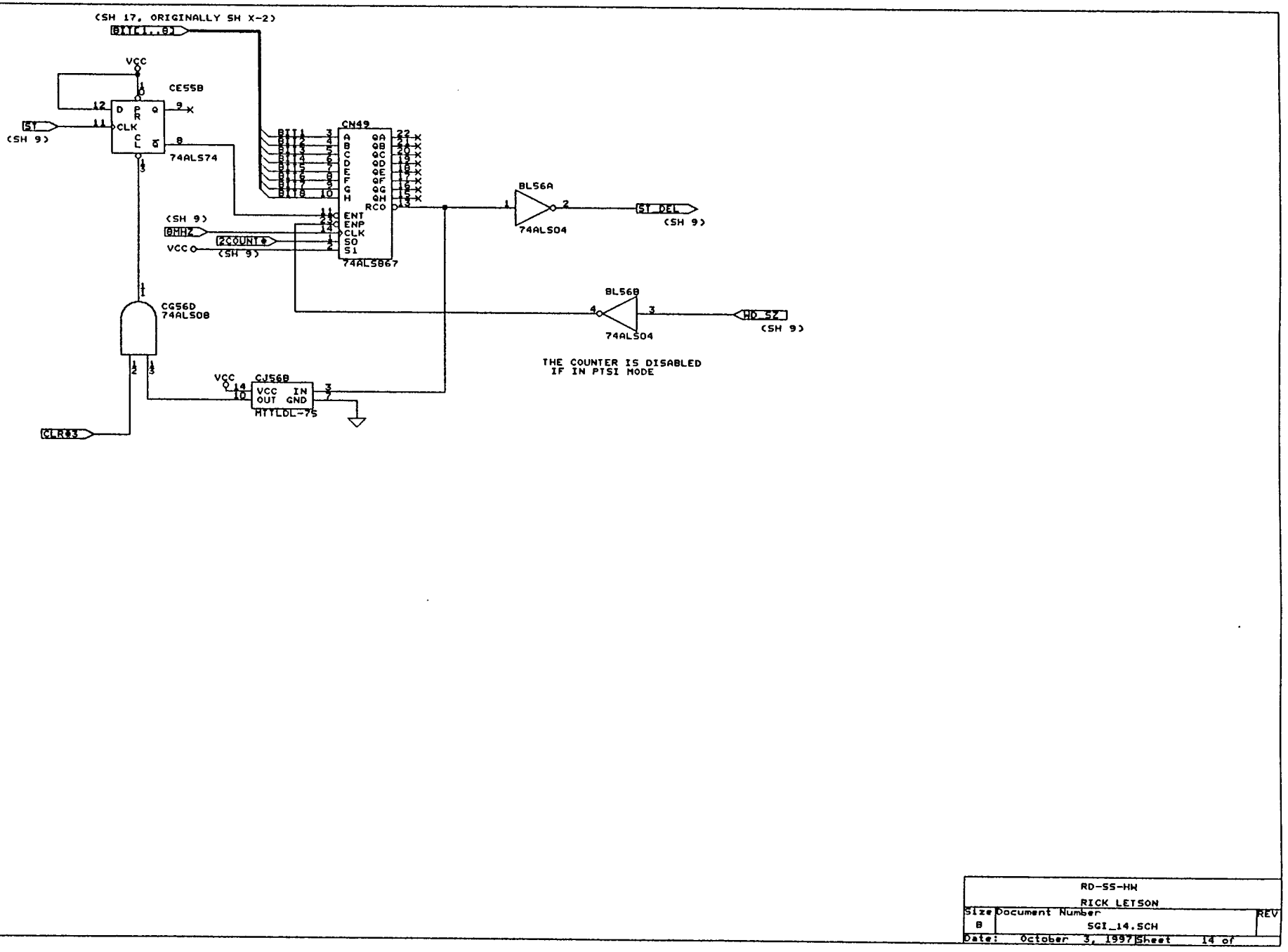

NO ACTIVE VIDEO
ACTIVE VIDEO
NO ACTIVE VIDEO
CA01A
74ALS08
CLR#3
NEVER EVER CHANGE THE LENGTH OF THIS DELAY
CE01A
CC33A
MTTLDL-50
40NS
74ALS74
VSIZE_EN#
(SH 11)
THESE TRY TO CHANGE IMMEDIATELY AFTER VIDEO DATA HAS ENDED
THESE DO NOT CHANGE IF READ COUNTER IS ENABLED.
CE01B
CA01B
NO INHIBIT
INHIBIT
BANK1_WEN
BANK2_WEN
(SH 4,12)
THESE ARE SET UP BEFORE THE FIRST CLOCK PULSES COME IN.
CC09A
READ COUNTER ENABLE
40NS load
BJ10A
RAC_LD
(SH 11)
NO INH
INHIBIT
CA01C
READSTOP
RACCLR
DISABLER OF READ PROCESS
(SH 3)
CLR#3
CE09A
READ COUNTER ENABLE
load
no load
BJ10B
RAC_EN
RAC_EN#
(SH 12)
PRESET TO CLR# NOT USUALLY DONE
CC57B
74AS08
CLR#
RAC_LD ONLY GENERATES A LOAD AFTER A FRAME HAS BEEN SENT TO SCREEN AT THE END OF DVI DATA.
CA01D
8MHZ
(SH 13)
READSTOP#
END OF FRAME
CT36
DELAY100N
CL49
74ALS157
ST
ST_DEL
HD_SZ
(SH 14)
RAC_EN WILL COINCIDE WITH LOW TO HI OF CLOCK
CC09B
START STATUS READ
READ_ST2
(SH 17)
CE09B
74ALS74
OUT_EN
(SH 13,15)
CA09E
2COUNT#
2COUNT
(SH 11)
FRMDTH
(SH 15)
BH40C
74ALS04
54A/256A
64A/256A
CA17
74ALS191
PTDEL
INDEL
CT19
CT28A
74ALS00
DEL
S1
CV11
CV13
CV15
SW SPDT STATUS WORD SIZE CONTROL
LO=5/HI=8
CP26
DEL100/14
BT18
CA09A
STATVAL2
CP18A
VDATOUT AND STATVAL AND THE CLOCK WILL START AT THE SAME TIME
CP10
CE17A
VDATOUT
VDATOUT#
KILLVAL
(SH 15)
CC17
74ALS164
BT10B
UNCK
BH40E
VALSTAT#
(SH 16)
RD-SS-HW
RICK LEISON
Size B
Document Number SGI_9.SCH
REV
Date: June 26, 1997 Sheet 9 of


DAR[0..12]
(SH 4)
IF BIT 12=HI
DATA IS BOGUS
IF BIT 12=LO
DATA IS VALID
AND CLOCK OCCURS
WHEN DATA IS READ
AF01
AF12
AF23A
74ALS574
74ALS04
DAR12
DBR[0..12]
(SH 5)
AF31
AF42
AF23B
DBR12
DCR[0..12]
(SH 6)
BH18
BH29
BH40A
DCR12
AP54
VCC
R-PACK
898-3-R3.3K
DATOUT[0..11]
(SH 16)
DDR[0..12]
(SH 7)
BH48
BH59
BH40B
DDR12
DER[0..12]
CE25
CE36
CA09D
DER12
RD-55-HW
RICK LETSON
Size
B
Document Number
SGI_10.SCH
REV
Date: October 28, 1996
Sheet 10 of


THE READ COUNTER MONITORS THE WRITE COUNTER AND WHEN THE WRITE PROCESS IS COMPLETED THE WRITE COUNT VALUE IS LOADED INTO THE READ COUNTER AND THE READ COUNTER COUNTS DOWN FROM THERE. THE RAC_LD PULSE IS CREATED FROM THE TERMINATION OF THE YSIZEN PULSE.
WRITE COUNTERS
READ COUNTERS
(SH 9) 2COUNT
ENABLES RAC EARLY SO THAT ONE CLK CAN BE GENERATED
(SH 9) RACCLR
CC25A
74ALS74
CR50A
MTTLDL-200
1.6 MHZ
CC01A 74S260
RAC_CLK (SH 12)
LD_COUNT (SH 15)
ROCN_EN (SH 15)
CA09F
74ALS04
CC25B
CJ56A
MTTLDL-75
CV02D 74ALS08
(SH 3) WAC_CLK
BC09
BA10
BA01
AI10
74ALS191
CLR#1
AL(0..13) (SH 4,5,6,7,8)
AU19
AU28
AU37
AU46
AR(0..13) (SH 4,5,6,7,8)
(SH 9) RAC_LD
CL58B 74ALS21
BL56F 74ALS04
READSTOP# (SH 9,15)
WRITE ADDRESS COUNTER ENABLE
WAC_EN
(SH 9) YSIZE_EN#
CC57D 74AS08
CE17B
CA09C
YSIZE_EN (SH 2)
WAC_LD#
20ns
CR50C
CA26
DEL100/14
CC09D 74ALS08
THE LENGTH OF THE READSTOP PULSE SLOWLY INCREASES FROM 400 US TO 10 MS WITH EACH FRAME. THIS IS BECAUSE READSTOP IS HELD UNTIL THE COUNTERS ARE LOADED AND RAC_LD IS GENERATED FROM THE END OF YSIZEN.
RD-SS-HW
RICK LETSON
Size B
Document Number SGI_11.SCH
REV
Date: June 24, 1997 Sheet 11 of

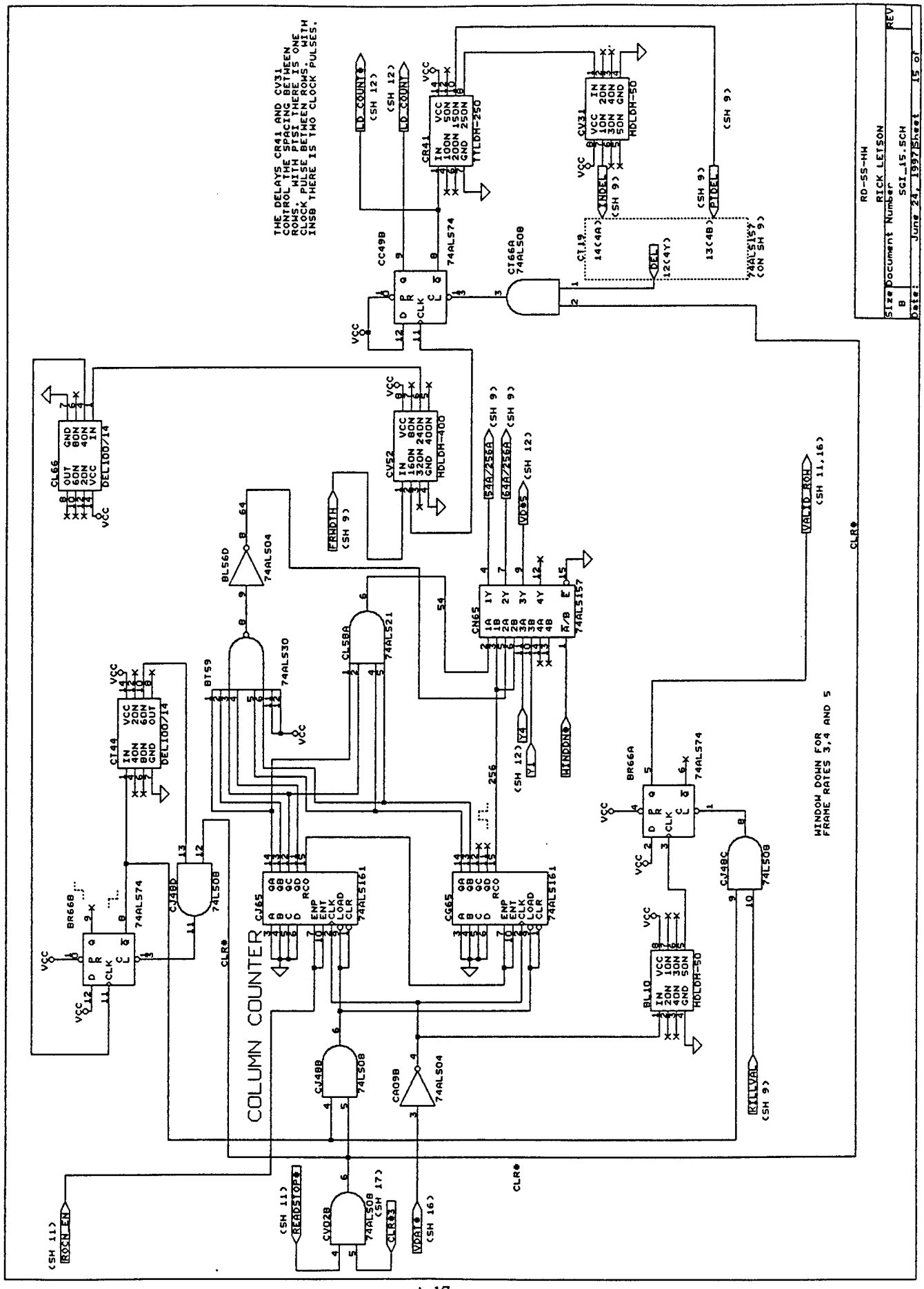


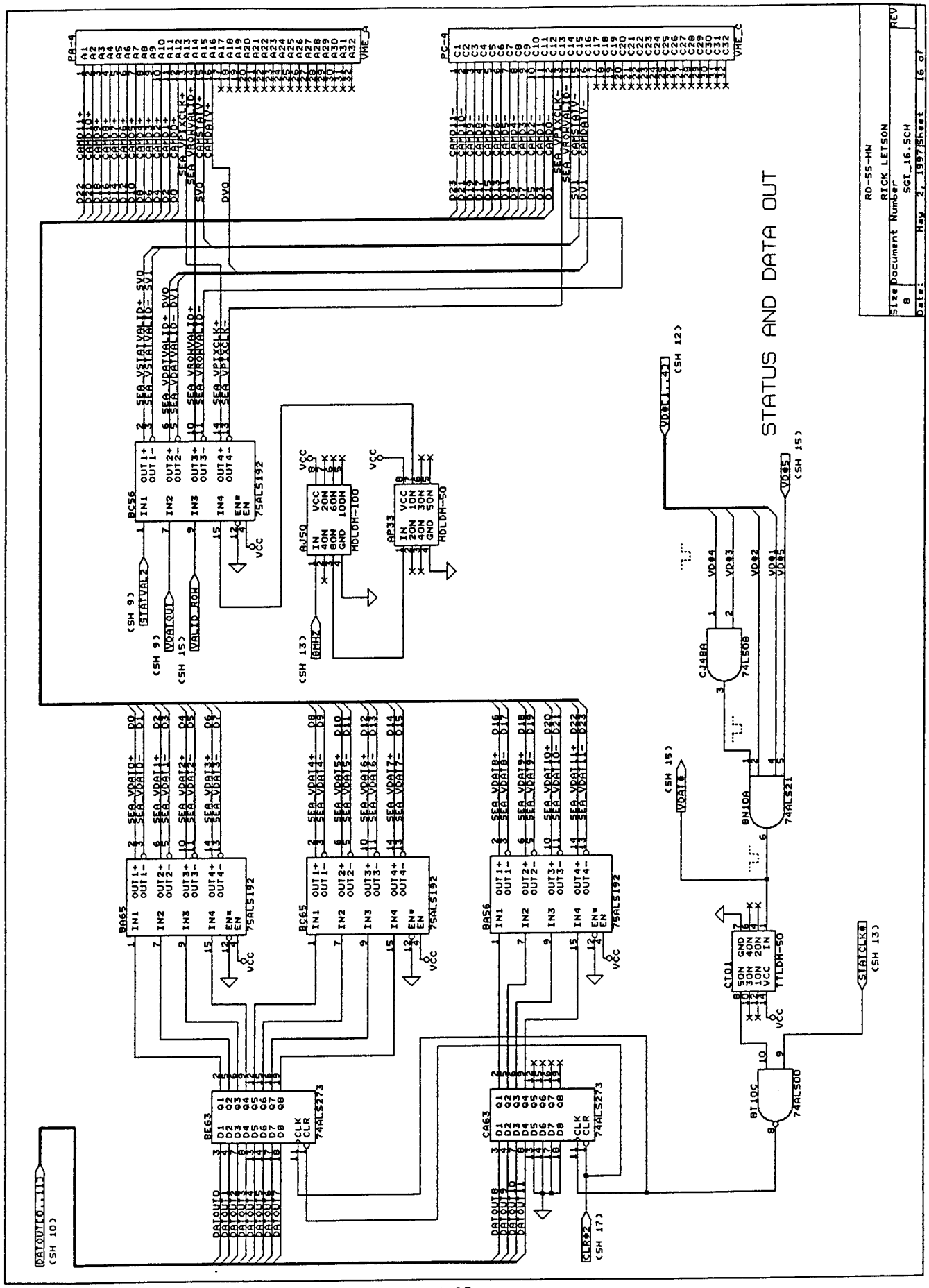

STATUS WORD FIFO
CAPTURE FRAME RATE WORD
DATI[0..23]
(SH 1)
DATOUT[0..11]
(SH 10,16)
74ALS193
74ALS222
74ALS574
74ALS273
74ALS138
74ALS08
74ALS04
74ALS191
74ALS574
FR_STR
CL_CONT#3
CL_CONT#4
CL_CONT#5
FIFOCLR#
(SH 12)
UNCK
(SH 9)
OUT_EN
BMHZ
(SH 9,12,16)
CLFYFO
(SH 12)
LDCK SHOULD OCCUR
IN CENTER OF DATA
DEL100/14
MDLDM-50
STATCLK#
(SH 16)
CLR#2
WINDON# BEGINS HI
WINDON#
(SH 12,15,17)
VALID STATUS
STAT[0..1]
(SH 1)
CLK[0..1]
(SH 1)
LDCKEN
(SH 12)
STATVAL
(SH 17)
VALSTAT#
(SH 9)
CLR#
THIS GENERATES A CLOCK
TO CAPTURE THE FRAME RATE WORD
RD-SS-HW
RICK LETSON
Size B
Document Number SGI_13.SCH
REV
Date: July 2, 1997 Sheet 13 of

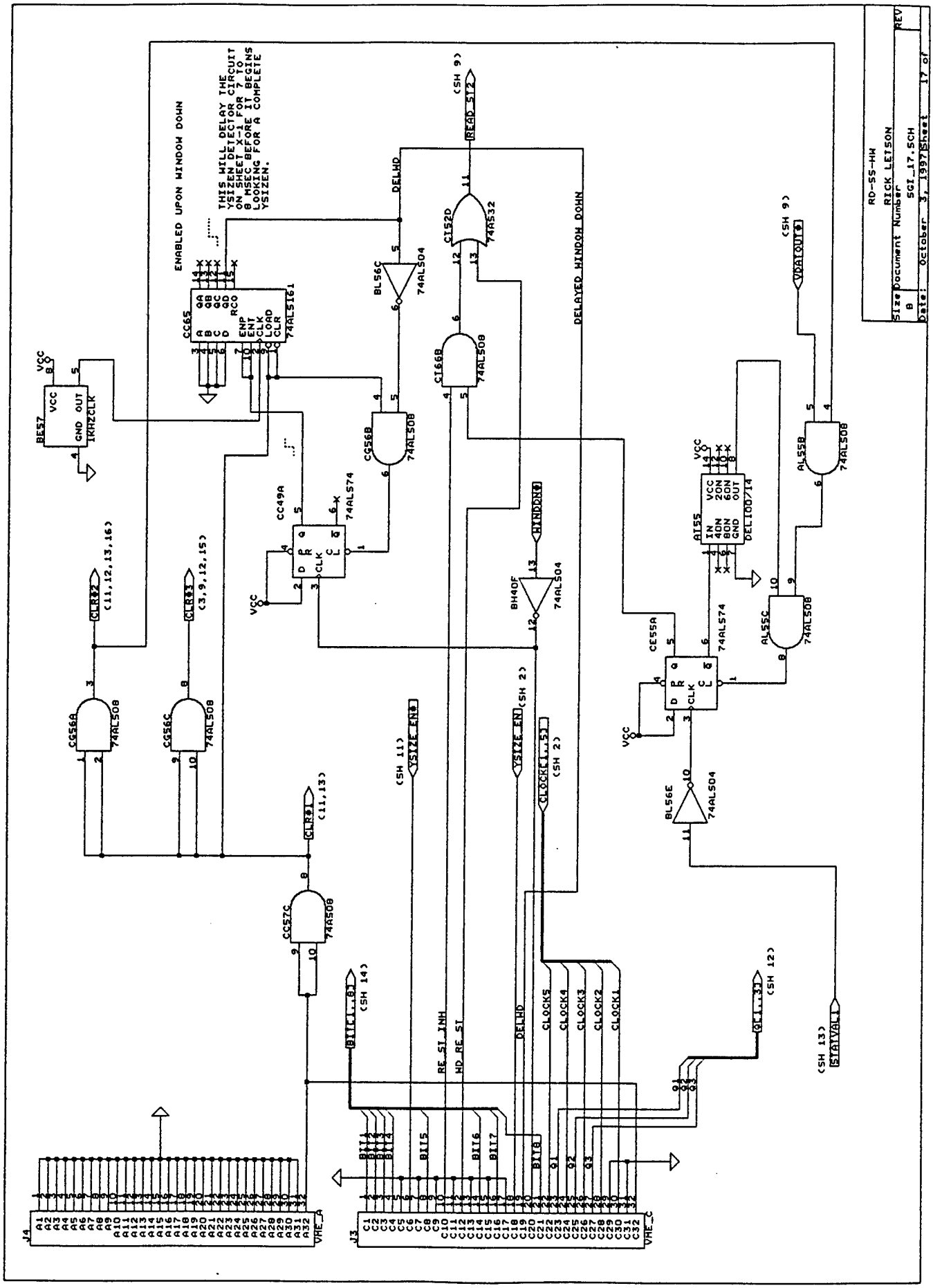


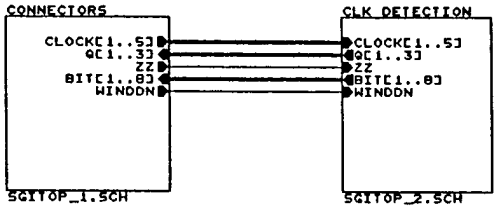
A-16

RD-SS-HW		
RICK LETSON		
Size B	Document Number SGI_14.SCH	REV
Date: October 3, 1997	Sheet 14 of	

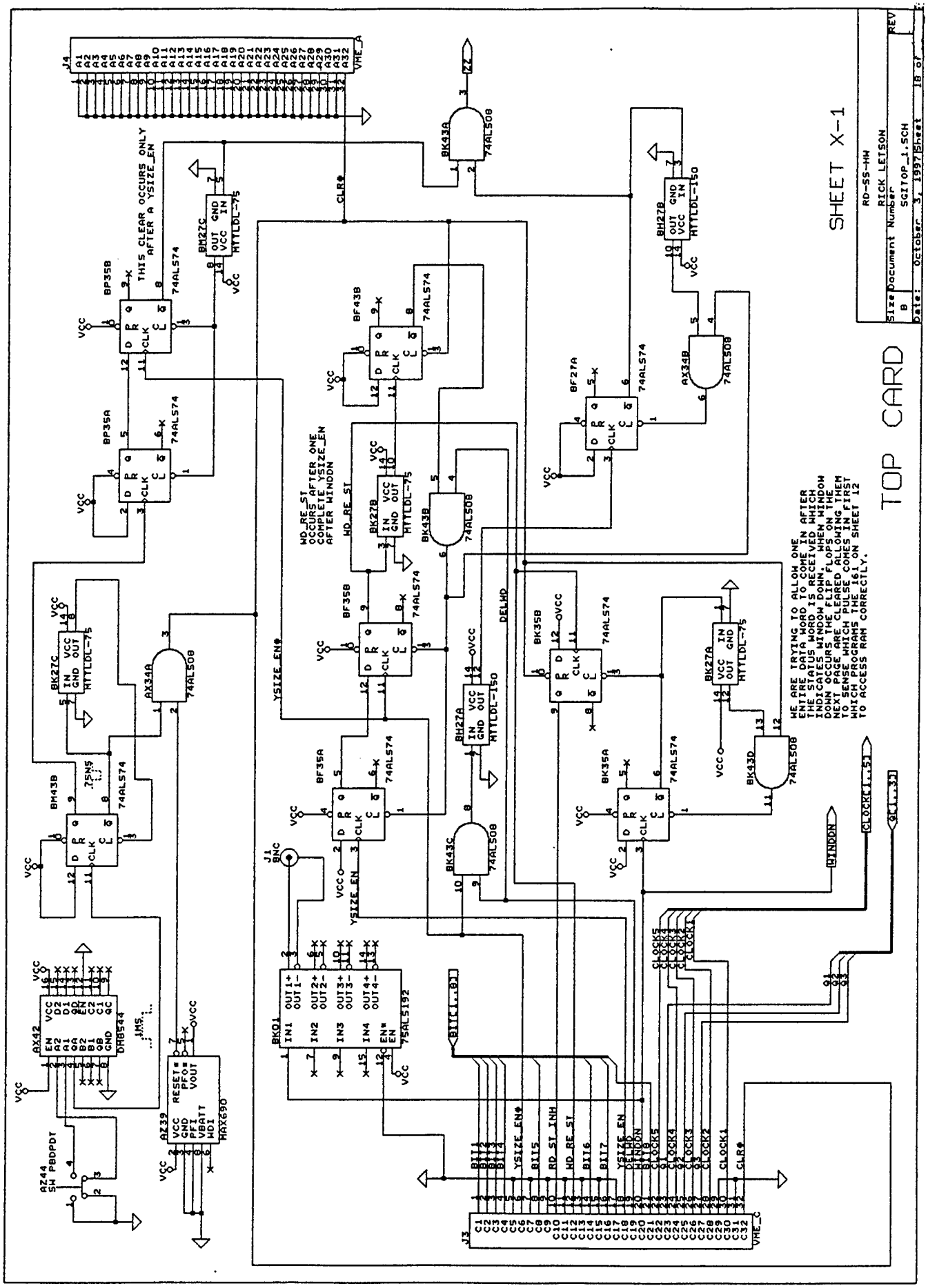

COLUMN COUNTER
THE DELAYS CR41 AND CV31 CONTROL THE SPACING BETWEEN ROWS. WITH PTSI THERE IS ONE CLOCK PULSE BETWEEN ROWS. WITH INSB THERE IS TWO CLOCK PULSES.
WINDOW DOWN FOR FRAME RATES 3,4 AND 5
RD-55-HW
RICK LEISON
Size: B
Document Number
SGI_15.SCH
Date: June 24, 1997
Sheet 15 of
REV
CJ65
CG65
CR41
CV31
CV52
CL58A
CN65
BT59
BL56D
CC49B
CI66A
CJ48B
CJ48C
CJ48D
CJ49B
CA09B
CV02B
CL66
CI44
BL10
BR66A
BR66B
CI19
74ALS161
74ALS574
74ALS521
74ALS530
74ALS157
74ALS504
74LS08
TTLDM-250
MDLDM-50
MDLDM-400
DELI00/14
LD COUNT*
LD COUNT
INDEL
PIXDEL
DEL
VALID ROW
CLR*
ROCN EN
READSTOP*
VDRT*
KILLVAL
HINDON*
FRMDTH
VCC
GND

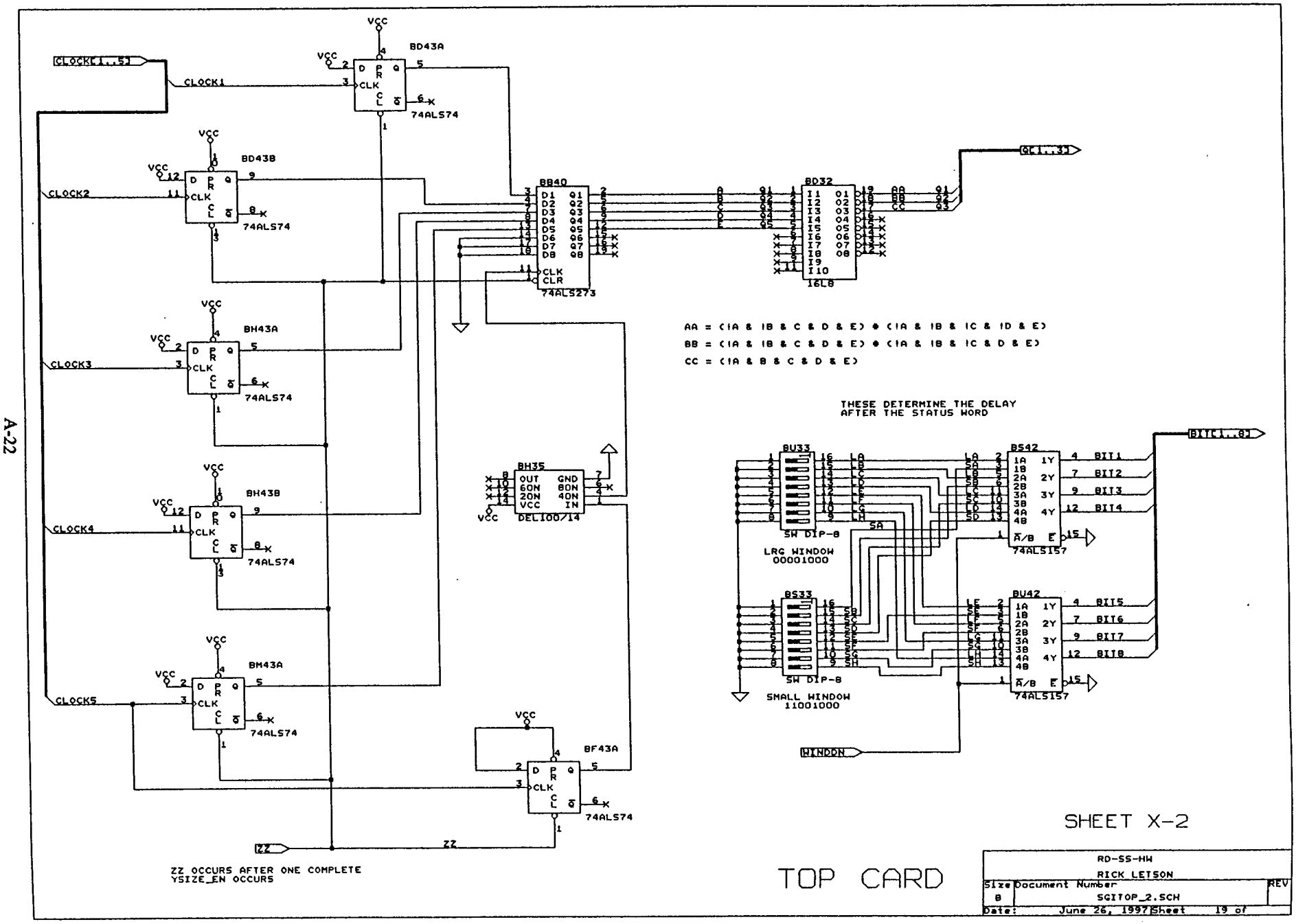

STATUS AND DATA OUT
RD-SS-HW
RICK LEITSON
SGI_16.SCH
Size: B
Document Number
REV
Date: May 2, 1997
Sheet 16 of


RD-SS-HW
RICK LETSON
Size Document Number REV
B SGI_17.SCH
Date: October 3, 1997 Sheet 17 of
ENABLED UPON WINDOW DOWN
THIS WILL DELAY THE YSIZEN DETECTOR CIRCUIT ON SHEET X-1 FOR 7 TO 8 MSEC BEFORE IT BEGINS LOOKING FOR A COMPLETE YSIZEN.
DELAYED WINDOW DOWN
READ_ST2
DELHD
WINDOWN
YSIZE_EN
CLOCK[1..5]
RE_SI_INH
MD_RE_ST
BIT[1..8]
STATVAL[1..3]
VOUT[0..3]
CLR#2
CLR#3
CLR#1
CC49A
CG56A
CG56B
CG56C
CG57C
CI52D
CI68B
BL56C
BH40F
BL56E
CE55A
AI55
AL55B
AL55C
74ALS74
74ALS08
74ALS04
74AS32
74ALS161
DELI00/14
VCC
IRMZCLK
J4
J3
VME_A
VME_C



RD-SS-HW		
RICK LETSON		
Size B	Document Number	REV
Date: June 25, 1997	Sheet of	


TOP CARD
SHEET X-1
RD-SS-HW
RICK LEITSON
SGITOP_1.SCH
October 3, 1997
WE ARE TRYING TO ALLOW ONE ENTIRE DATA WORD TO COME IN AFTER THE STATUS WORD IS RECEIVED WHICH INITIATES WINDOW. WHEN WINDOW GOES DOWN OCCURS THE FLIP-FLOPS IN NEXT PAGE ARE CLEARED ALLOWING THEM TO SENSE WHICH PULSE COMES IN FIRST WHICH PROGRAMS THE 161 ON SHEET 12 TO ACCESS RAM CORRECTLY.
THIS CLEAR OCCURS ONLY AFTER A YSIZE_EN
WD_RE_ST OCCURS AFTER ONE COMPLETE YSIZE_EN AFTER WINDOW
74ALS574
74ALS508
74ALS192
DM8544
MAX690
HTTLDL-75
HTTLDL-150


CLOCK[1..5]
CLOCK1
CLOCK2
CLOCK3
CLOCK4
CLOCK5
BD43A
BD43B
BH43A
BH43B
BM43A
BF43A
74ALS74
BB40
74ALS273
BD32
16L8
GI[1..3]
AA = (IA & IB & C & D & E) # (IA & IB & IC & ID & E)
BB = (IA & IB & C & D & E) # (IA & IB & IC & D & E)
CC = (IA & B & C & D & E)
BH35
DEL100/14
THESE DETERMINE THE DELAY
AFTER THE STATUS WORD
BU33
SW DIP-8
LRG WINDOW
00001000
BS42
74ALS157
BII[1..8]
BII1
BII2
BII3
BII4
BS33
SMALL WINDOW
11001000
BU42
BII5
BII6
BII7
BII8
WINDOW
ZZ
ZZ OCCURS AFTER ONE COMPLETE
YSIZE_EN OCCURS
TOP CARD
SHEET X-2
RD-SS-HW
RICK LEISON
Size B
Document Number
SGITOP_2.SCH
REV
Date: June 26, 1997
Sheet 19 of

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