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# IMPLEMENTATION OF THE MIMIC ROBUST DESIGN TECHNIQUE

David C. Williamson and Clare D. Thiem

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The impact of temperature on the performance of microwave/millimeter wave monolithic integrated circuits (MMICs) is examined in this report. Using simulation software resident at Rome Laboratory, engineers explored not only the temperature sensitivity of an actual circuit, but also the integration of the software. The Robust Design Initiative was conducted by Rome Laboratory under the auspices of the Defense Advanced Research and Project Agency/Tri-Service Microwave/Millimeter Wave Monolithic Integrated Circuits Program. All work described in this report was conducted in-house at Rome Laboratory.

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# PREFACE

The impact of temperature on the performance of microwave/millimeter wave monolithic integrated circuits (MMICs) is examined in this report. Using simulation software resident at Rome Laboratory, engineers explored not only the temperature sensitivity of an actual circuit, but also the integration of the software. The Robust Design Initiative was conducted by Rome Laboratory under the auspices of the Defense Advanced Research and Project Agency (DARPA) Tri-Service Microwave/Millimeter Wave Monolithic Integrated Circuits (MIMIC) Program. All work described in this report was conducted in-house at Rome Laboratory.

The authors would like to acknowledge the support provided by several individuals. From Lockheed Sanders, Mr. Michael Blum and Mr. John Heaton provided Rome Laboratory with the information from an actual MMIC application on which to focus this effort. Ms. Karen Heitkamp and Mr. Fred Sloan, also from Lockheed Sanders, provided clarification of the physical layout and the materials used in the transmit/receive module. Mr. Timothy Mayo from Ceramics Process Systems provided information on the material properties of Aluminum Silicon Carbide. Finally, from within Rome Laboratory, technical assistance was provided by Mr. Mark Stoklosa of the Design Analysis Branch.

## 0.0 EXECUTIVE SUMMARY

Temperature changes can cause parametric shifts in sensitive microwave/millimeter wave monolithic integrated circuit components leading to performance degradation and, in extreme cases, instability and device failure. Using in-house electrical computer aided design and finite element analysis software, an actual circuit suspected of having temperature sensitivity was examined. It was found that heat, generated by the active components within the chip, altered the values of two passive elements to the point where one of the circuit parameters did not meet the required specifications. Suggestions were then provided to the chip manufacturer to compensate for the simulated effects.

## 1.0 INTRODUCTION

Microwave/millimeter wave circuit technology has made great advancements with the advent of monolithic integration. Having both active and passive devices fabricated within the same substrate allows for low cost and miniaturization. Although much of the burden for design success has been lifted through the use of numerous microwave computer aided design (CAD) tools, including foundry element libraries and circuit optimization routines, designs suffering thermal defects are still being sent to fabrication. For operating frequencies under 1 GHz, a structure's sensitivity to small changes in temperature can be considered insignificant. As operating frequencies go beyond 1 GHz, and especially above 10 GHz, however, this sensitivity increases drastically. A circuit's performance is not only affected by large changes in ambient temperatures, but also by

localized thermal gradients within the circuit. Heat generated from an active structure subjects a greater number of elements to these thermal gradients. Temperature sensitive components suffer parametric shifts causing performance degradation and, in extreme cases, instability and device failure. This temperature sensitivity is the cause of jitters during pulse/transient conditions for some power amplifier designs [1]. Typically, these effects go unnoticed until after the device has been fabricated and test results reveal a problem.

Previous studies have been carried out to analyze heat flow within microwave and millimeter wave devices. Most of this work was conducted under the auspices of the Defense Advanced Research Project Agency (DARPA) Tri-Service Microwave/Millimeter Wave Monolithic Integrated Circuits (MIMIC) Program. Specifically, it has been determined that for microwave/millimeter wave monolithic integrated circuits (MMIC) devices, there is a significant amount of heat flow in three dimensions which potentially leads to widespread thermal gradients across the device [2]. Through the refinement of finite element thermal modeling techniques, this heat flow can be accurately modeled. Other unrelated studies have examined the affects of temperature on MMIC test structures. One such study revealed that both active and passive MMIC test structures exhibit a characteristic temperature dependency for certain parameters taken between 0°C and 160°C. It was expected that these results would prove to be useful in performing electrical simulations which use these devices. The results of these

earlier efforts provide the basis for a robust design technique which can be used to compensate for thermal effects before device fabrication .

## 1.1 OBJECTIVE

The objective of the Robust Design Initiative (RDI) was to demonstrate the influence of three-dimensional heat flow from active devices on the circuit performance of MMICs. Specifically, the change in performance due to the heating of passive elements neighboring active elements in power amplifiers. This was accomplished by utilizing electrical computer aided design (CAD) techniques in conjunction with finite element thermal modeling and test structure characterization. The results of the effort were used to provide feedback to circuit designers on the thermal stability of their circuit.

## 1.2 APPROACH

The approach taken was to select a device for modeling and simulation that was suspected of having instability problems due to temperature. Once selected, a corresponding electrical circuit description and a set of passive test (evaluation) structures were received from the manufacturer and characterized. Empirical equations, as functions of temperature, were then derived for these structures for use in electrical simulation. This was accomplished by characterizing the structures over temperature and also using existing MMIC test structure data. A sensitivity analysis was then performed to determine the critical components within the circuit. Circuit layout information,

sensitivity analysis results, and materials data were used to develop a physical model for finite element analysis (FEA). A steady state FEA was performed to determine the thermal characteristics for the device. These FEA results were then used as input to the electrical circuit description, and linear circuit analyses were performed. Results of these analyses were then used to determine the thermal stability of the device.

## 2.0 IMPLEMENTATION

Since the electrical CAD and FEA software already resided at Rome Laboratory, implementation of the approach was rather straightforward. Two engineers set aside a portion of one fiscal year to conduct the analyses contained in this report. A major hurdle was locating an actual device on which to base the various analyses conducted for this effort. The paragraphs that follow provide the details about how each step of the approach above was accomplished.

### 2.1 DEVICE SELECTION

A letter was sent to various MIMIC contractors soliciting support in the form of MMIC designs which they felt suffered from thermal instability. A design was received from Lockheed Sanders, headquartered in Nashua, New Hampshire, which was claimed to suffer from performance fluctuations due to temperature related phenomena. This device, called the DMS68-6, was a 6-18 GHz double-balanced wideband high power MMIC amplifier being integrated into the design of a transmit/receive (T/R) module. The layout

of this device is shown in Figure 2.1. This device was best suited for our analysis since a high power device provides a larger total heat dissipation than other devices (e.g. low noise amplifier, mixer, phase shifter, etc.).

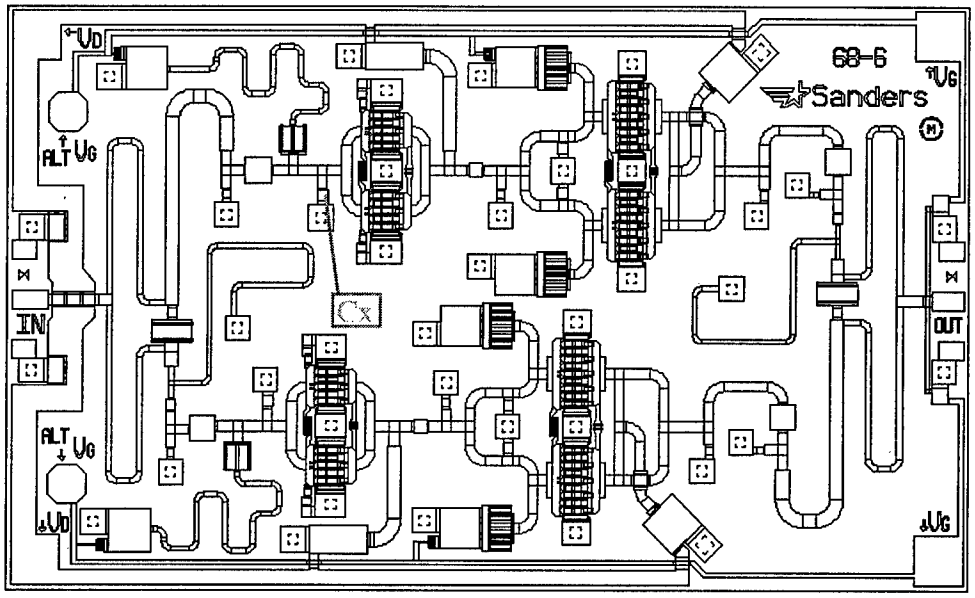


Figure 2.1. DMS68-6 Double-Balanced Wideband Power Amplifier

Lockheed Sanders provided the actual circuit dimensions in the form of a GDS2 manufacturing layout file (developed by the Calma Company) along with the electrical netlist (used for circuit simulation). Field effect transistor (FET) dimensions were also included except for the gate width and relative position in the channel. The FETs consisted of four "horseshoed-together" 800 μm periphery FETs at the input and four 1200 μm periphery FETs at the output. The power dissipated by each FET, normally biased at 1/2 Idss where Idss is approximately 275 mA per 100 μm with a drain voltage of 7 V, was calculated to be:

$$\left[\left(\frac{800\,\mu m}{2000\,\mu m}\right)\times 275\,mA\right]\times 7\,V = 0.77\,W \qquad \text{(Eq. 1.a.)}$$

$$\left[\left(\frac{1200\,\mu m}{2000\,\mu m}\right)\times 275\,mA\right]\times 7V = 1.155\,W \qquad \text{(Eq. 1.b.)}$$

which indicates a total power dissipation of 7.7 W total for the active devices populating the amplifier in Figure 2.1.

## 2.2 ELECTRICAL SIMULATION DEVELOPMENT

The electrical simulation portion of the RDI was conducted using commercially available microwave simulation software resident in-house at Rome Laboratory. This software, called Microwave Harmonica (MH), is written and distributed by Compact Software, headquartered in Paterson, New Jersey. MH is an industry standard CAD tool for the analysis of RF and microwave circuits and uses the method of harmonic balance for deriving its solutions for linear and nonlinear circuits. MH uses an electrical netlist circuit description (similar to that of SPICE) as input for simulation.

### 2.2.1 FILE CONVERSION

The electrical netlist file for the DMS68-6 was available from Lockheed Sanders in Libra format only. Libra, also an industry standard CAD tool which uses the method of harmonic balance for the analysis of RF and microwave circuits, is written and distributed by EEsof Inc., headquartered in Westlake Village, California. Because the syntax was not

directly compatible with the existing in-house microwave design tool syntax, MH, the netlist file, had to be converted. A Libra to MH conversion program was obtained from Compact Software. This program was only partially successful in converting the file. Node numbers were not properly assigned to their corresponding connection points. As a result, the circuit file was manually converted. This was done by re-creating the circuit using Serenade, the schematic editor tool from Compact Software.

Once the file was converted, a comparison was made between the Libra, MH, and measured S-parameter results (provided by Lockheed Sanders). The results show that the Libra and MH linear models are nearly identical to each other (see Figure 2.2.1). These differences are attributed to round-off errors and default conditions assumed by either simulator.

### 2.2.2 SENSITIVITY ANALYSIS

Because of the relative complexity of the circuit being analyzed, it was desired to reduce the number of elements modeled during the finite element analysis. Doing so would allow for shorter computation time and the elimination of unnecessary information. This was done by determining the critical elements within the circuit through sensitivity analysis. The critical elements were those circuit structures which had noticeable effect on device performance. The sensitivity analysis was performed by viewing each circuit element separately and varying their parameters by small increments while monitoring the

effects on the S-parameters and circuit stability (the rule of thumb used was; for a 2% change in element parameter value, there is at least a 0.25% in circuit parameter value). A typical result of this analysis is shown in Figure 2.2.2.a. Here the 0.551306 pF capacitor Cx (shown in Figure 2.1) is varied by 2% of its original value. The effect on circuit performance yields a change in input reflection (S11) of + or -1.8dB or + or -6.9% of the original value. As a result Cx is considered a critical element. All non-critical elements determined from this sensitivity analysis are indicated in Figure 2.2.2.b.

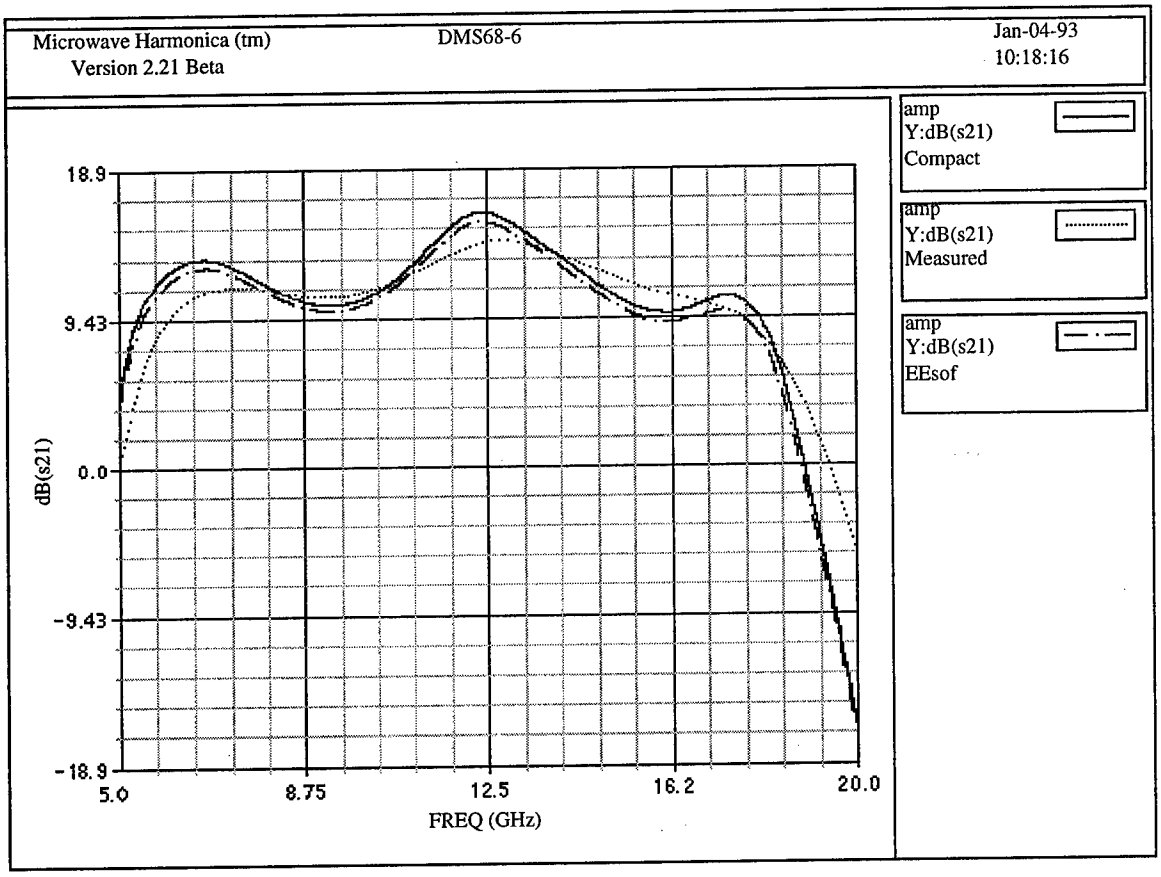


Figure 2.2.1. Comparison of Simulator Results

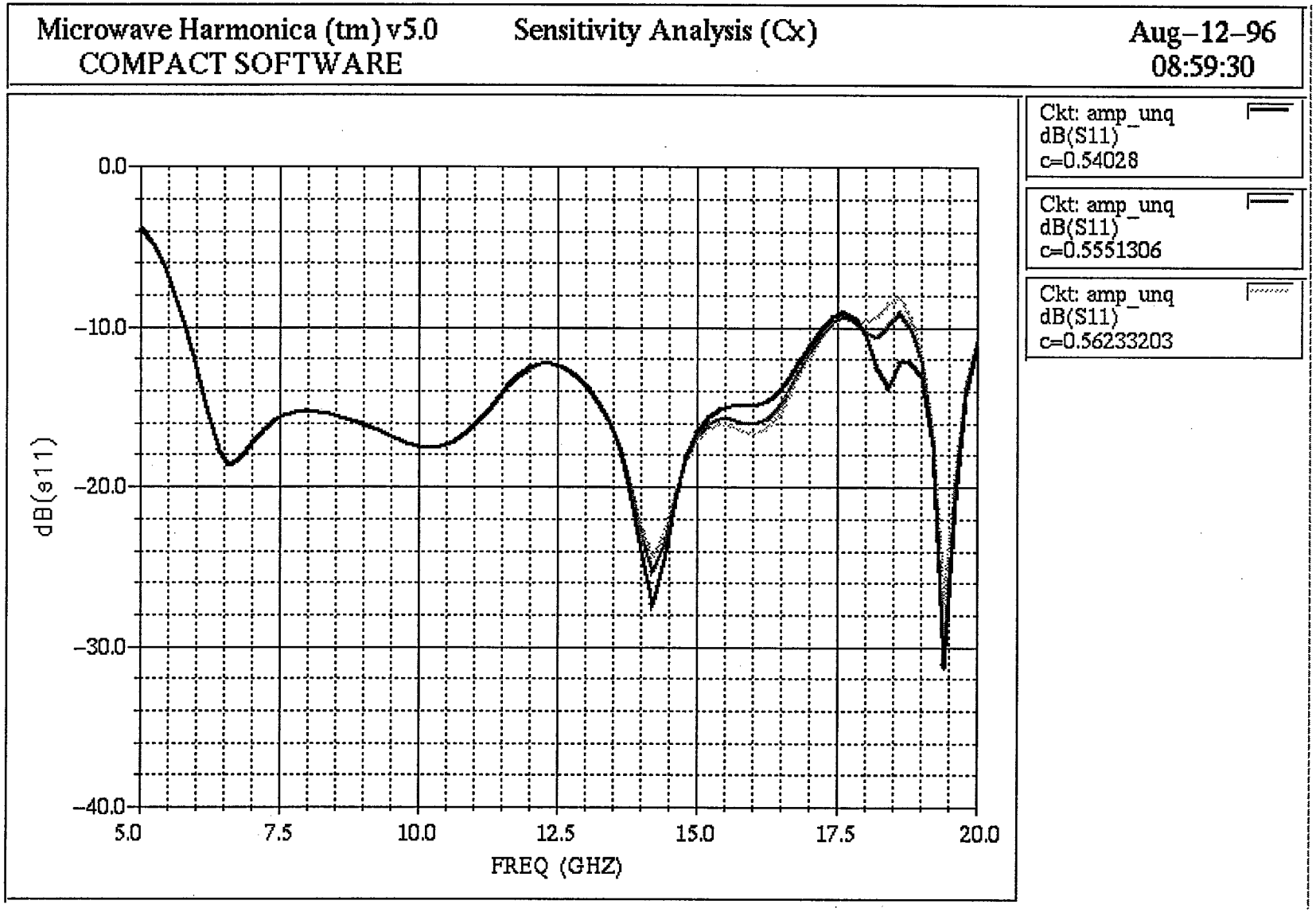


Figure 2.2.2.a. Circuit Sensitivity to Capacitor Cx

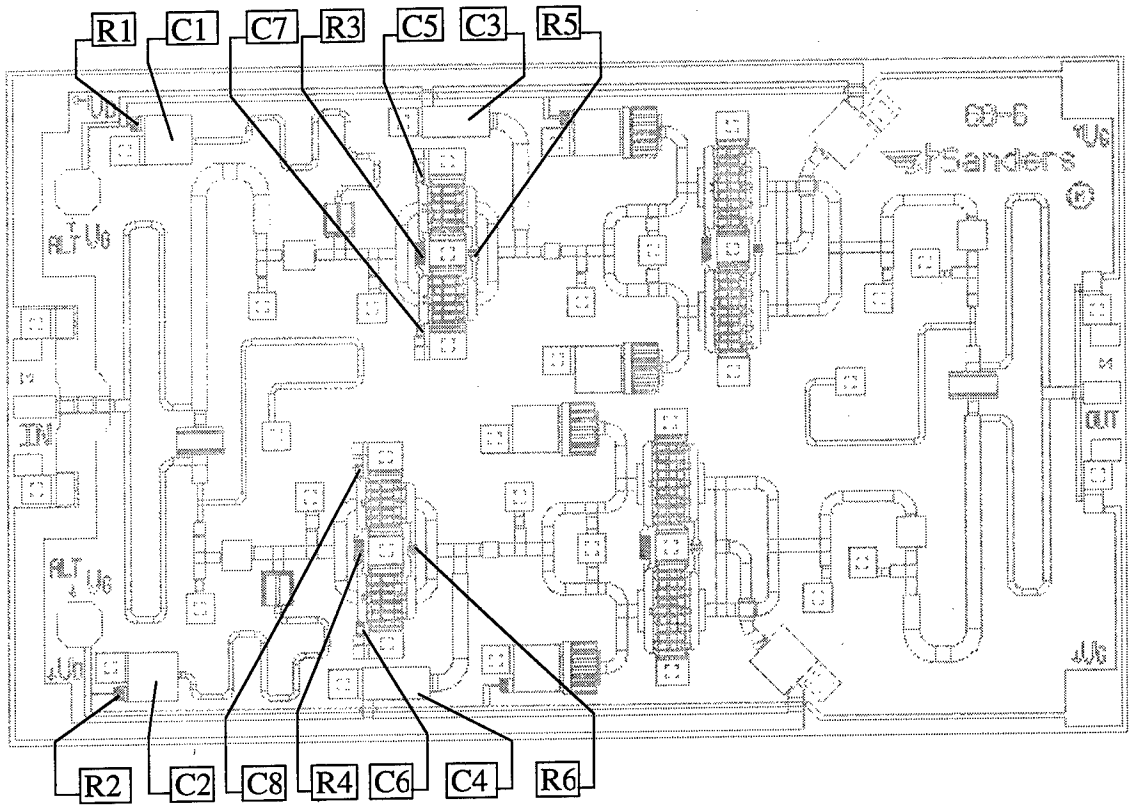


Figure 2.2.2.b. Non-Critical Elements Determined From Sensitivity Analysis

### 2.2.3 TEST STRUCTURE MEASUREMENT AND EQUATION DEVELOPMENT

In order to utilize the results from the finite element thermal analysis, temperature dependencies had to be determined for the critical elements. This was done by deriving empirical representations from existing MMIC test structure data and from characterization of test structures provided by Lockheed Sanders. Since the focus of this effort was on the influence of thermal gradients on circuit performance due to passive element heating, characterization of only the capacitor and resistor structures was needed.

Previous studies were performed to determine the affects of temperature on MMIC test structures. One study [3] revealed that both active and passive MMIC test structures

exhibit a characteristic temperature dependency for certain parameters taken between 0°C and 160°C. Of particular interest were the thin film resistor structures which were similar in composition to those used in the DMS68-6. Results of the study revealed the sheet resistance characteristics over temperature shown below.

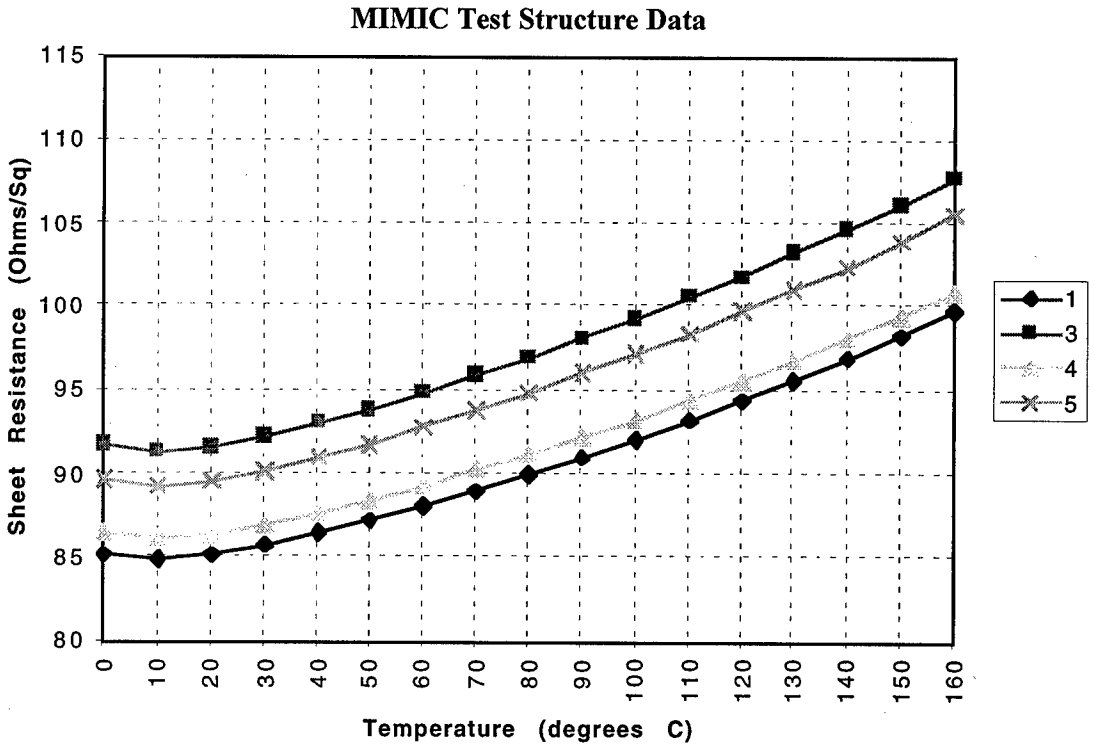


Figure 2.2.3.a. Characterization of Resistor Test Structures

Since this test structure data took on a linear form, the following generalized empirical approximation was used in describing resistance over temperature:

$$P(T_e) = aP(T_r)(T_e - 25°C) + P(T_r) \qquad \text{(Eq. 2)}$$

where: $P(T_r)$ = element parameter value at room temperature (25°C)
$T_e$ = element temperature (determined from FEA)
$P(T_e)$ = actual element parameter value
$a$ = temperature coefficient

Similarly, test structures received from Lockheed Sanders contained capacitor and FET structures used in the DMS68-6. From this set of test structures, two 5 pF metal-insulator-metal (MIM) capacitor structures were bonded in fixtures for DC characterization over temperature. The capacitance of these structures were measured from 25°C to 125°C. The results of this temperature characterization are shown in Figure 2.2.3.b. Using the same empirical approximation derived for resistance (Eq. 2), calculation of the average slope indicated a 4.628% variation in capacitance over 100°C (0.04628%/°C). This result was used as the temperature coefficient in the generalized empirical approximation (Eq. 2) for MIM capacitor structures in the DMS68-6.

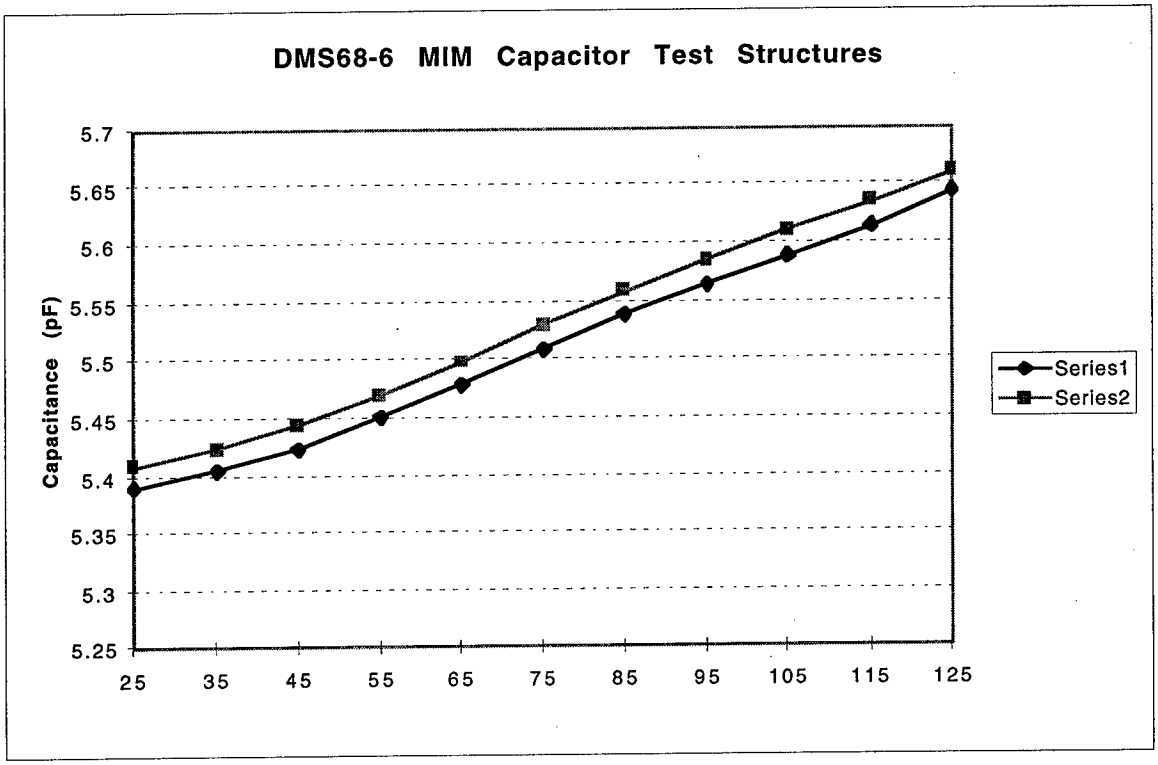


Figure 2.2.3.b. Characterization of MIM Capacitor Test Structures

Since no resistive structures were received from Lockheed Sanders, a temperature coefficient derived from the previous study (Figure 2.2.3.a) was used. Calculation of the average slope indicated a 10.101% variation in resistance over 100°C (0.10101%/°C). This result was used as the temperature coefficient in the generalized empirical approximation (Eq. 2) for resistor structures in the DMS68-6.

### 2.2.4 THE INTEGRATED NETLIST

Once the generalized empirical equations for the capacitor and resistor elements were derived, they were integrated into the electrical netlist circuit description. Each critical capacitor and resistor element description was replaced by the corresponding capacitance and resistance equation (Eq. 2) as illustrated in Figure 2.2.4.

```
.
.
.
viah1 137 0
*viah1#26 layout 3
cp23 17 116
*cp23#25 layout 0
cap 136 135 c = ((TC17 - 25) * 0.0004628 * 0.67pF) + 0.67pF
*mhcap2#18 layout 1
trl 20 142 w = 0.7334mil
*mhtrl1#14 layout 0
trl 16 17 w = 8mil p = 6mil
*mhtrl1#11 layout 0
res 15 16 r = ((TR10 - 25) * (0.0010101 * 8.3) + 8.3
*mhres#10 layout 0
m2t 141 143 142
*m2t#8 layout 0
.
.
.
```

Figure 2.2.4. Integrated Netlist Example.

The element temperatures (to be determined from FEA) for each element were given a unique variable name and listed at the beginning of the netlist. Once the FEA results were determined, actual temperature values were then assigned to these variables. At this point, the circuit description was complete and ready for input from the thermal analysis.

## 2.3 FINITE ELEMENT ANALYSIS

The thermal analysis portion of the RDI was conducted using commercially available FEA software resident in-house at Rome Laboratory. This software is called Numerically Integrated Elements for Structural Analysis (NISA), which is written and distributed by Engineering Mechanics Research Corporation (EMRC), headquartered in Troy, Michigan. This is a general purpose finite element code that has been successfully applied to MMICs and other microelectronic structures by Rome Laboratory engineers in the past [4,5]. A majority of the information used in the thermal analysis for this effort was supplied by Lockheed Sanders including: the physical description of the chip, the physical description of the transmit/receive (T/R) module which contains two of the DMS68-6 chips, heat dissipated by the field effect transistors, and some material data. Once the necessary information had been gathered, the next step was to build the necessary finite element models (FEMs).

### 2.3.1 MODELING

Two three-dimensional FEMs were used to conduct the thermal analysis for the RDI. The first FEM, shown in Figure 2.3.1.a., was of the portion of the T/R module that contained the two identical amplifier chips which dissipated the majority of the heat in the module. The relative position of the chips in the module is shown in Figure 2.3.1.b. The portion of the module in the Phase I model represents that part of the module which is a direct path from the heat source to the cold plate. This configuration represents a worse case scenario. The various features of the Phase 1 FEM are labeled in Figure 2.3.1.a. The second FEM is shown in Figure 2.3.1.c. The Phase 2 FEM is a substructure of the Phase 1 FEM representing only the gallium arsenide (GaAs) wideband power amplifier chip itself. Figure 2.3.1.c. shows a top down view, with respect to the chip, of the Phase 2 FEM. It was made up of elements of a much smaller size than those used in the Phase 1 FEM. Both active and passive components of the design are pointed out in Figure 2.3.1.c. Only those passive components that were found to have a potential temperature sensitivity, as determined by the sensitivity analysis discussed earlier in this report, were highlighted in the model. Once the FEMs were built, the appropriate material properties can then be inserted to fully define the physical structure being modeled.

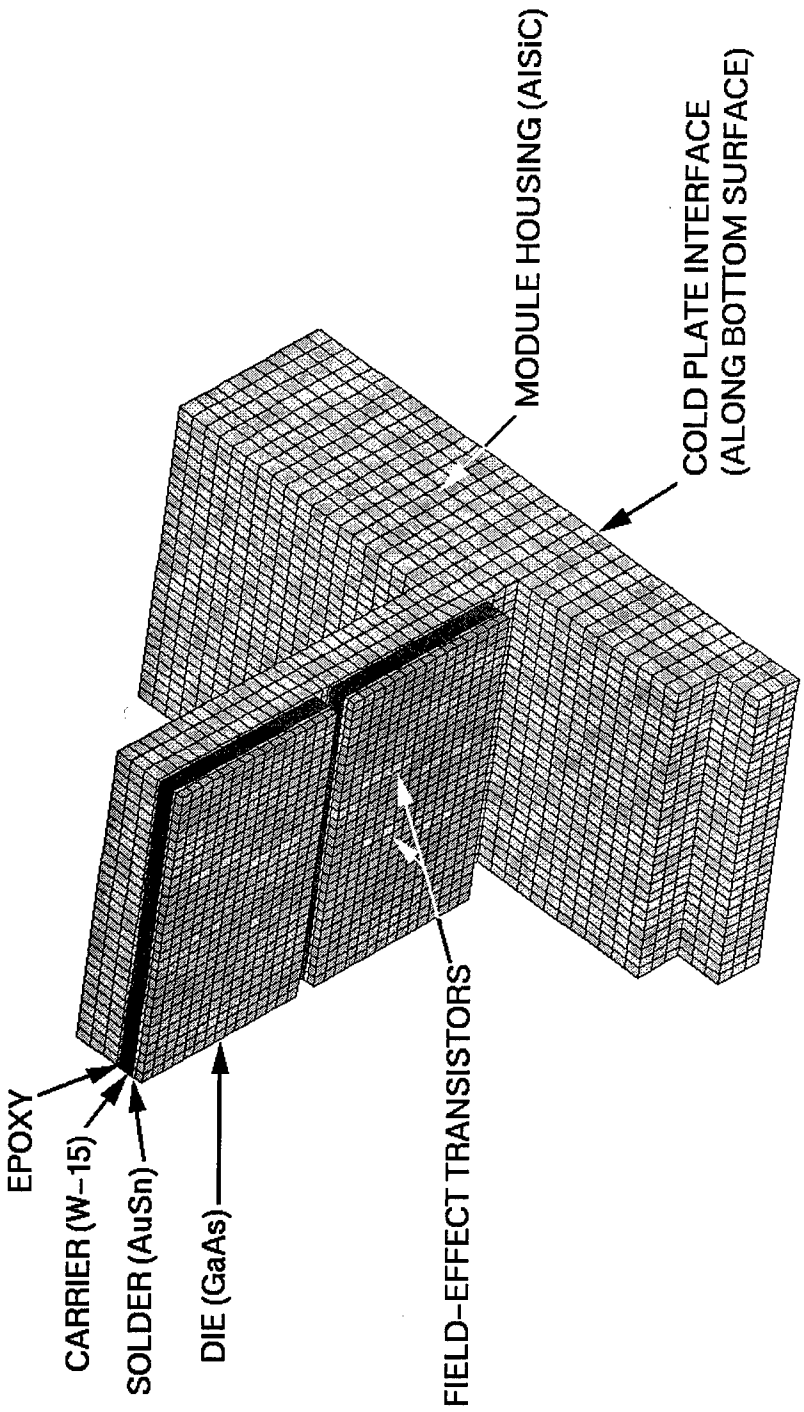


Figure 2.3.1.a. Phase 1 FEM

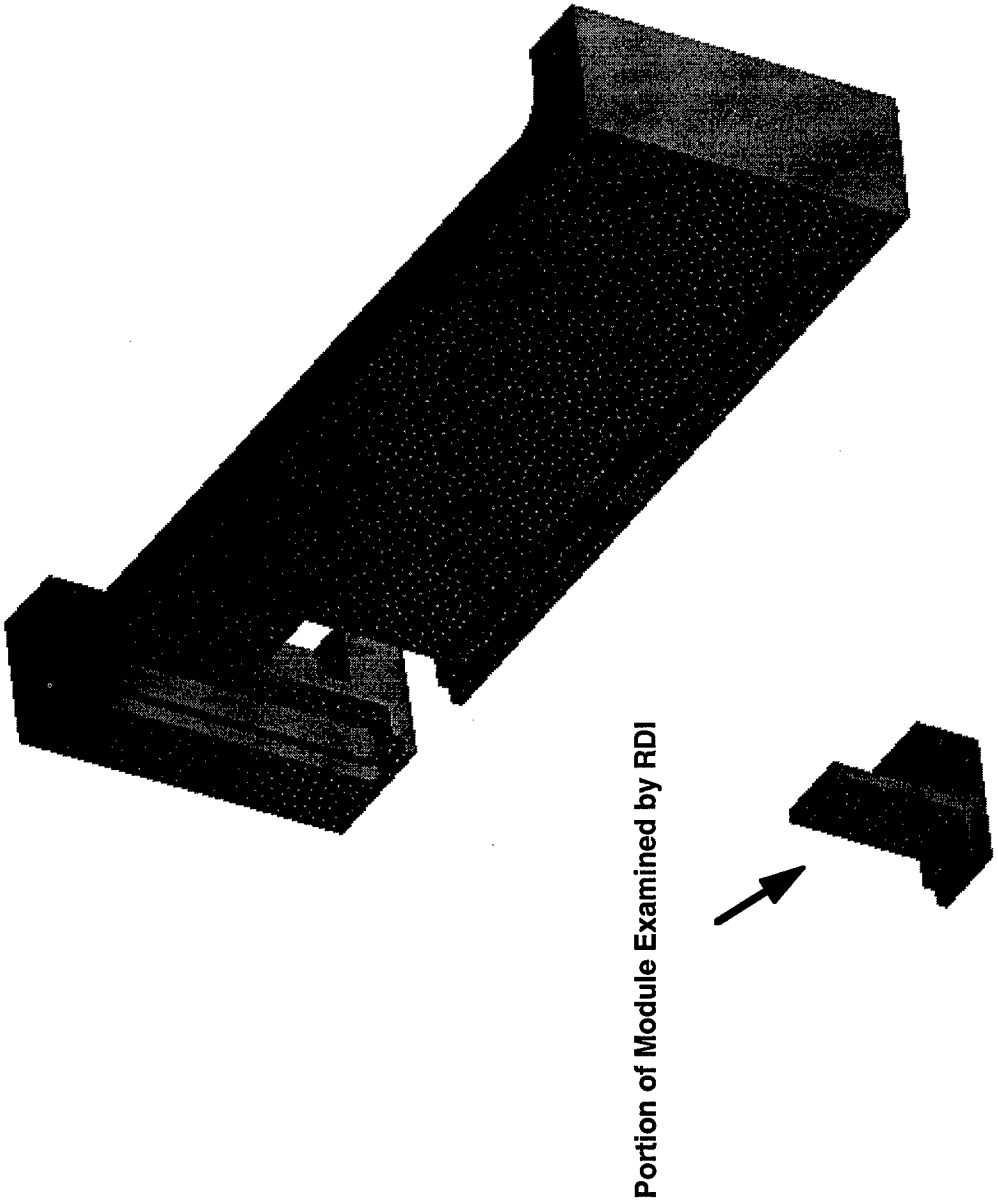


Figure 2.3.1.b. Illustration of Transmit/Receive Module

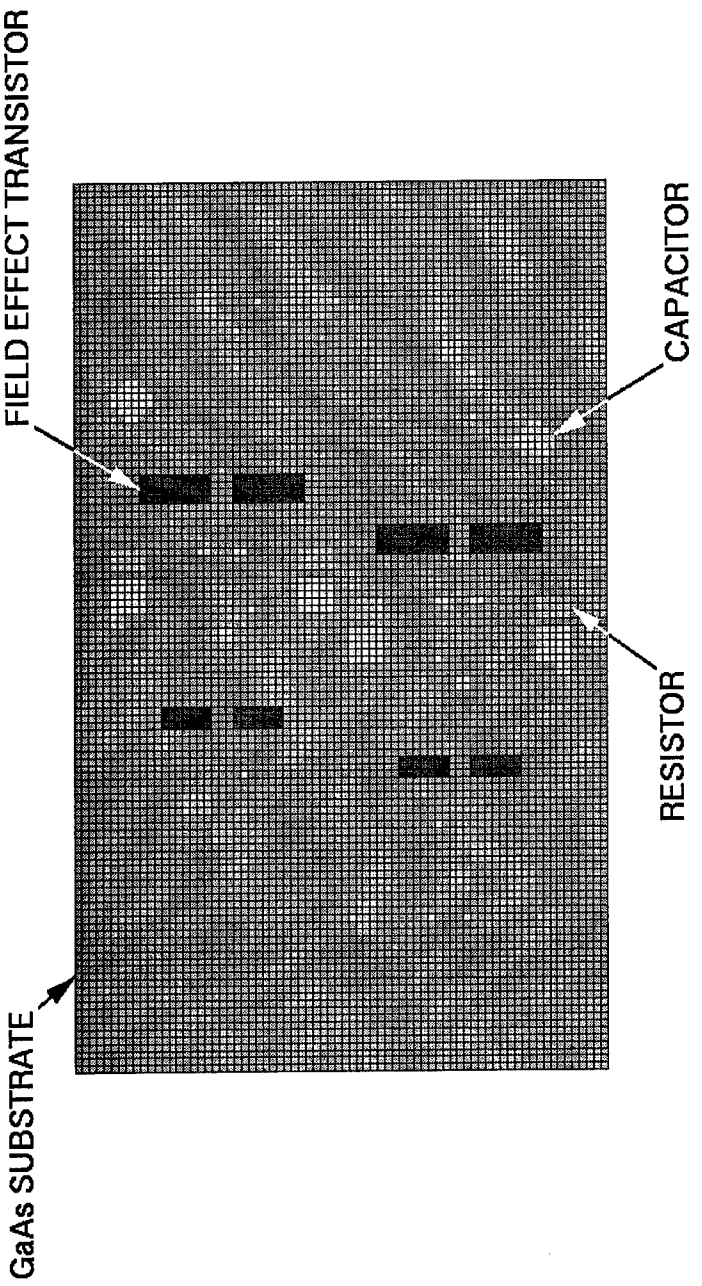


Figure 2.3.1.c. Top View of Phase 2 FEM

## 2.3.2 MATERIAL PROPERTIES

An effort was put forth to use the most accurate material information available at the time the analyses were conducted. The material properties used in the RDI thermal analyses are shown in Table 2.3.2.a. and were obtained from several sources. Thermal conductivity values for epoxy, carrier and gold-tin (AuSn) solder were supplied by Lockheed Sanders. Other analytical efforts at Rome Laboratory revealed the variability of the thermal conductivity of GaAs [6] resulting in the data shown in Table 2.3.2.b. being used in the RDI analyses. The thermal conductivity of Aluminum Silicon Carbide (AlSiC) used in the T/R module housing, the last material listed in Table 2.3.2.a., was based on information provided by the material's supplier, Ceramic Process Systems.

Table 2.3.2.a.

| RDI Material Properties | |
|---|---|
| Material | Thermal Conductivity (W/(μm*°C)) |
| Epoxy (HP35-175M) | 5.708E-03 |
| Carrier (W-15) | 1.854E-04 |
| Solder (AuSn) | 5.860E-05 |
| Die (GaAs) | See Table 2.3.2.b |
| Module Housing (AlSiC) | 1.600E-04 |

Table 2.3.2.b.

| Thermal Conductivity (k) for GaAs | |
|---|---|
| Temperature ( °C ) | k (E-5 W/(μm*°C)) |
| 20 | 4.75 |
| 30 | 4.40 |
| 40 | 4.15 |
| 70 | 3.67 |
| 100 | 3.34 |
| 130 | 3.04 |
| 160 | 2.84 |
| 300 | 2.16 |

The information contained in the tables above provided the last details necessary to define the physical aspects of the RDI FEMs. Once this aspect of model preparation was completed, effort could now be focused on conducting the thermal analyses.

## 2.3.3 STEADY STATE ANALYSIS

Steady state thermal analyses involving the Phase 1 and 2 FEMs, discussed earlier, were conducted to simulate the continuous wave operation of the T/R module. Prior to the analyses being conducted, however, two additional pieces of information were needed before the analytical runs could be initiated. First, the heat dissipated by the active components (the FETs pointed out earlier in Figures 2.3.1.a. and 2.3.1.c) were defined to provide the load conditions for the analyses. This was done by using a distributed flux to represent the 770 mW and 1,155 mW dissipated by each of the small and large FETs,

respectively. Second, a cold plate temperature of 50°C was applied along the bottom of the Phase 1 FEM, as shown earlier in Figure 2.3.1.a., to provide the boundary conditions for the Phase 1 analysis. Once these two pieces of information were determined, the actual analyses were conducted resulting in the thermal contours shown in the figures that follow.

Figure 2.3.3.a. shows the thermal contours for the Phase 1 analysis. It clearly illustrates the importance of three-dimensional thermal modeling. The two power amplifier chips, while being identical in design, were operating in different thermal environments. The results of the Phase 1 analysis were then used to provide the boundary conditions along the bottom of the FEM created for the Phase 2 analyses.

The Phase 2 analyses examined the upper and lower power amplifier chips individually. Figure 2.3.3.b. shows the thermal contours for the upper chip while Figure 2.3.3.c. shows the thermal contours for the lower chip. Note the different temperatures experienced by the two chips of the same design, subjected to the same load conditions, but located at different positions from the cold plate. These resulting temperatures were then passed on to be input variables for the electrical simulation runs for an integrated analysis.

## 2.4 INTEGRATED ANALYSIS

Using the temperature data obtained from the FEM analysis, an integrated electrical/thermal analysis was performed on the chip for both positions on the carrier.

To determine the temperatures of the critical elements, the thermal contours for the upper die (Figure 2.3.3.b) were overlaid on top of Figure 2.3.1.c. The value of the contour which fell at the center of the element was considered the temperature of that element. The same procedure was also used for determining the temperatures of the elements in the lower die (Figure 2.3.3.c). These values were then used in the electrical netlist as temperature variables , as described in Section 2.2.4.

### 2.4.1 COMBINED STEADY STATE ANALYSIS RESULTS

The results of the integrated electrical/thermal analysis are shown in Figures 2.4.1.a through 2.4.1.g. Parameters were analyzed for the chip in both the lower and upper position, as well as for both an even cold plate temperature (50°C) throughout the chip, and at room temperature. Results of the analysis indicate that there is a significant change in chip performance for each condition. Specifically, a large change is observed at the upper edge of the pass-band (~ 17.5 GHz to 18.5 GHz) for S11, S21,VSWR1, and VSWR2. The greatest changes are noticed for the chip mounted in the upper position (furthest from the cold plate) as would be expected.

The most significant impact is on VSWR1 (Figure 2.4.1.d) where the upper edge of the pass-band falls outside the required specifications (VSWR < 2) for both the lower and upper die as well as at 50°C. Through further analysis, it was determined that a large portion of the chip performance at the upper pass-band is driven by the pair of capacitors ( Cx1 and Cx2 in Figure 2.4.2) located in the input matching network of the

first stage. These capacitors are in close proximity to the active devices in the first stage. Thermal analysis showed that these capacitors are subject to local temperatures 29°C (lower die) and 50°C (upper die) above the cold plate temperature of 50°C when dissipating maximum power. These temperatures, combined with the dependency of the chip performance on the values of these capacitors, lead to the observed increase in VSWR1 as well as the changes in S11. In order to compensate for this effect, the capacitors Cx1 and Cx2 could be replaced by those of a lower capacitance so that at the elevated temperature (when the chip is on), their values will be as expected for room temperature operation.

It was also noted that the simulated performance becomes unstable for frequencies in the region between 8 GHz and 8.4 Ghz (see Figure 2.4.1.g). The origins of the observed spike in the stability around these frequencies appears to be inherent to the circuit design itself and not a factor of temperature.

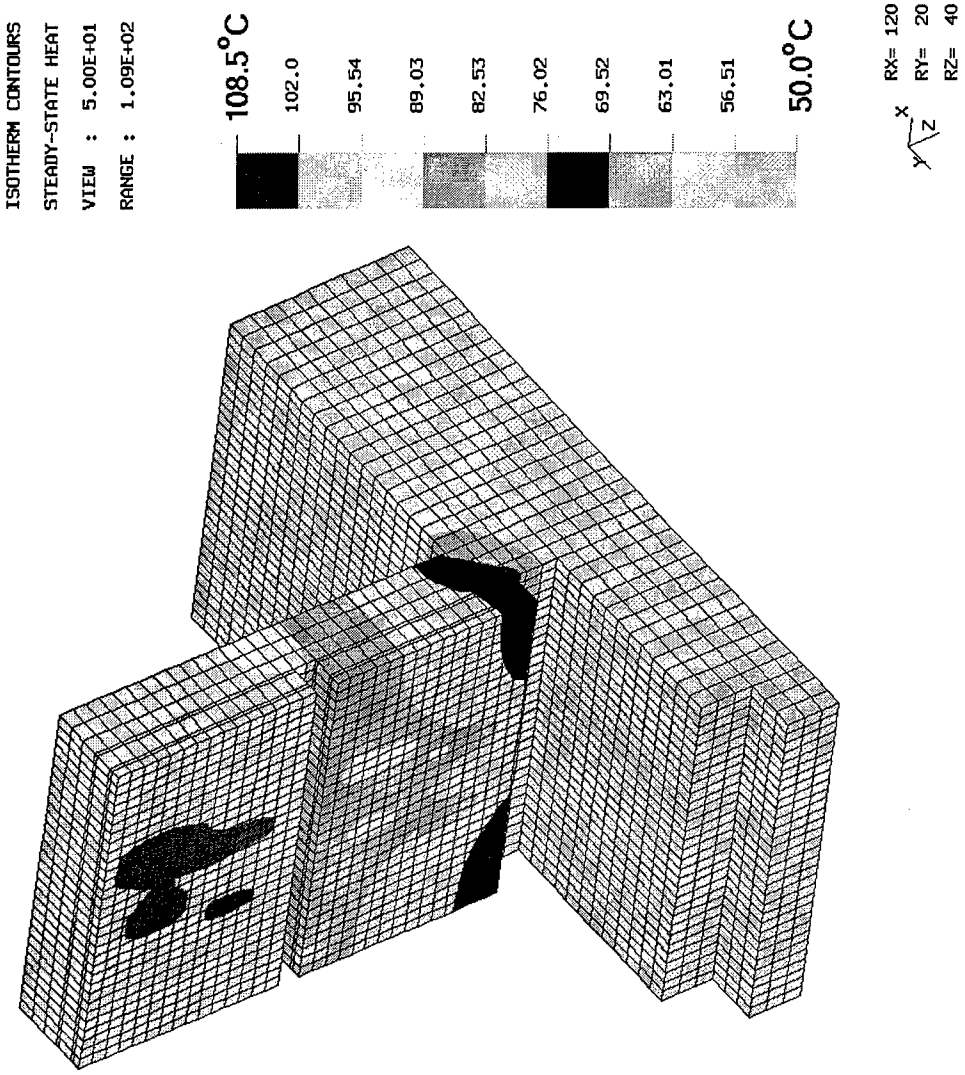


Figure 2.3.3.a. Resulting Thermal Contours for Phase 1

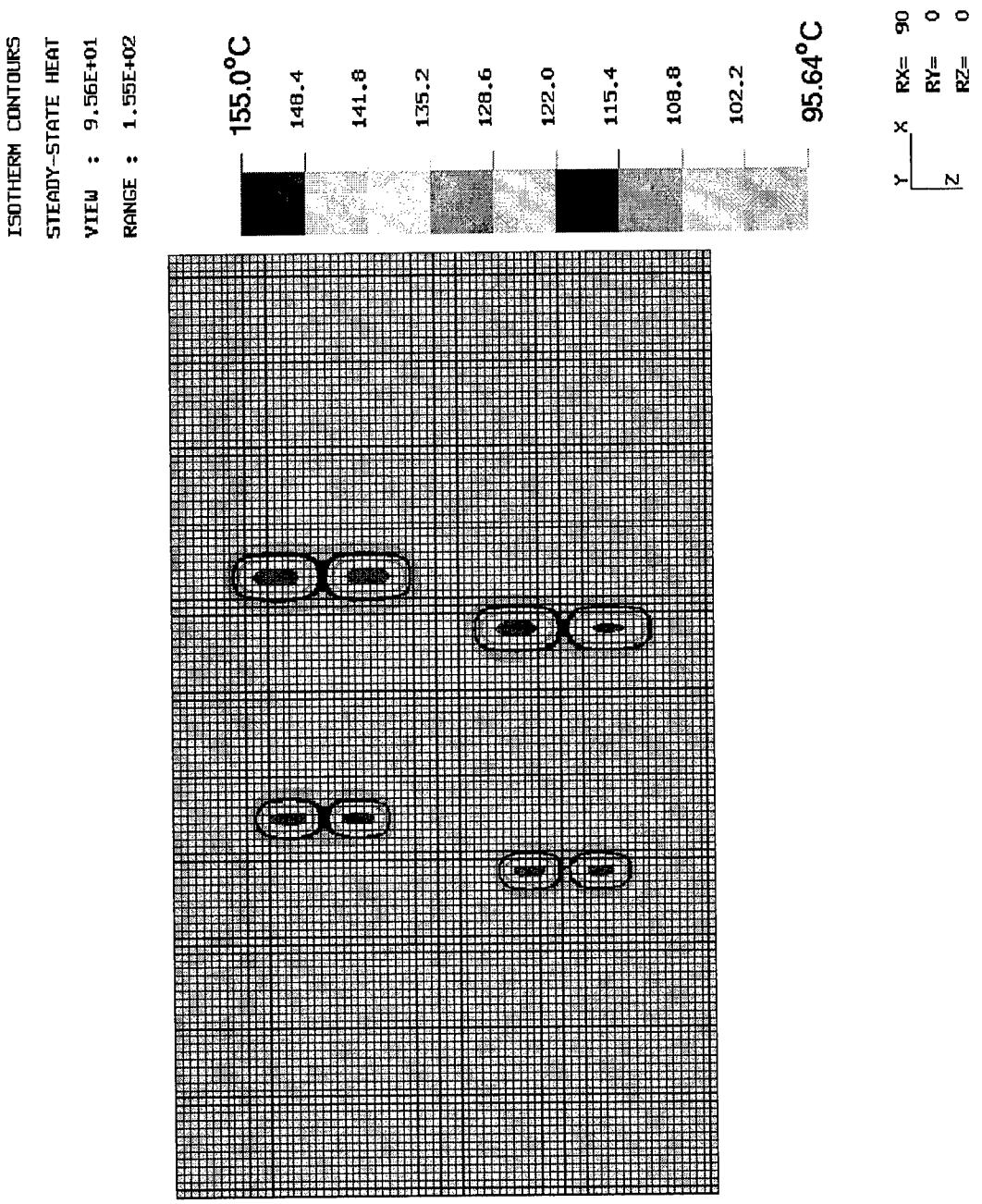


Figure 2.3.3.b. Resulting Thermal Contours on Upper Chip for Phase 2

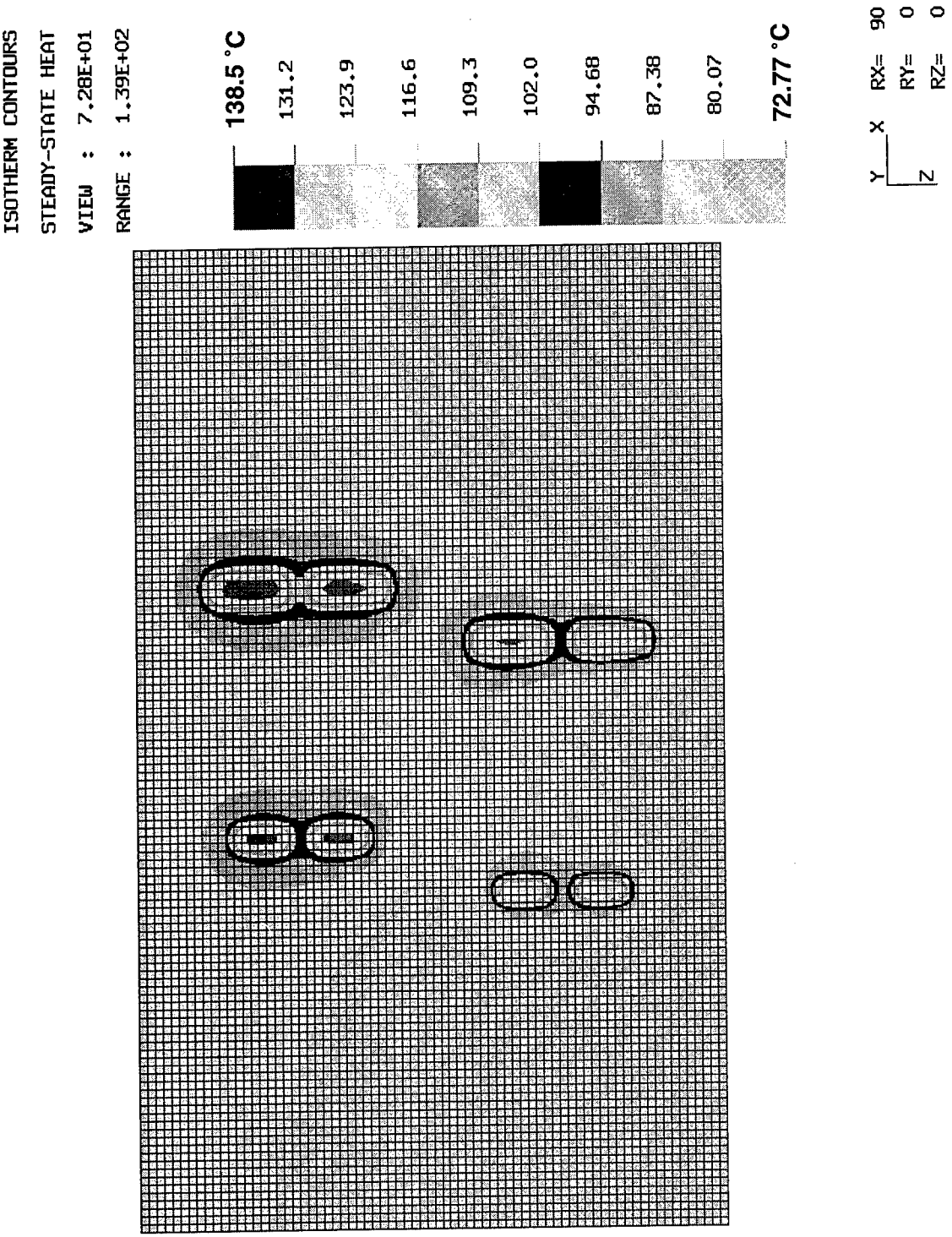


Figure 2.3.3.c. Resulting Thermal Contours on Lower Chip for Phase 2

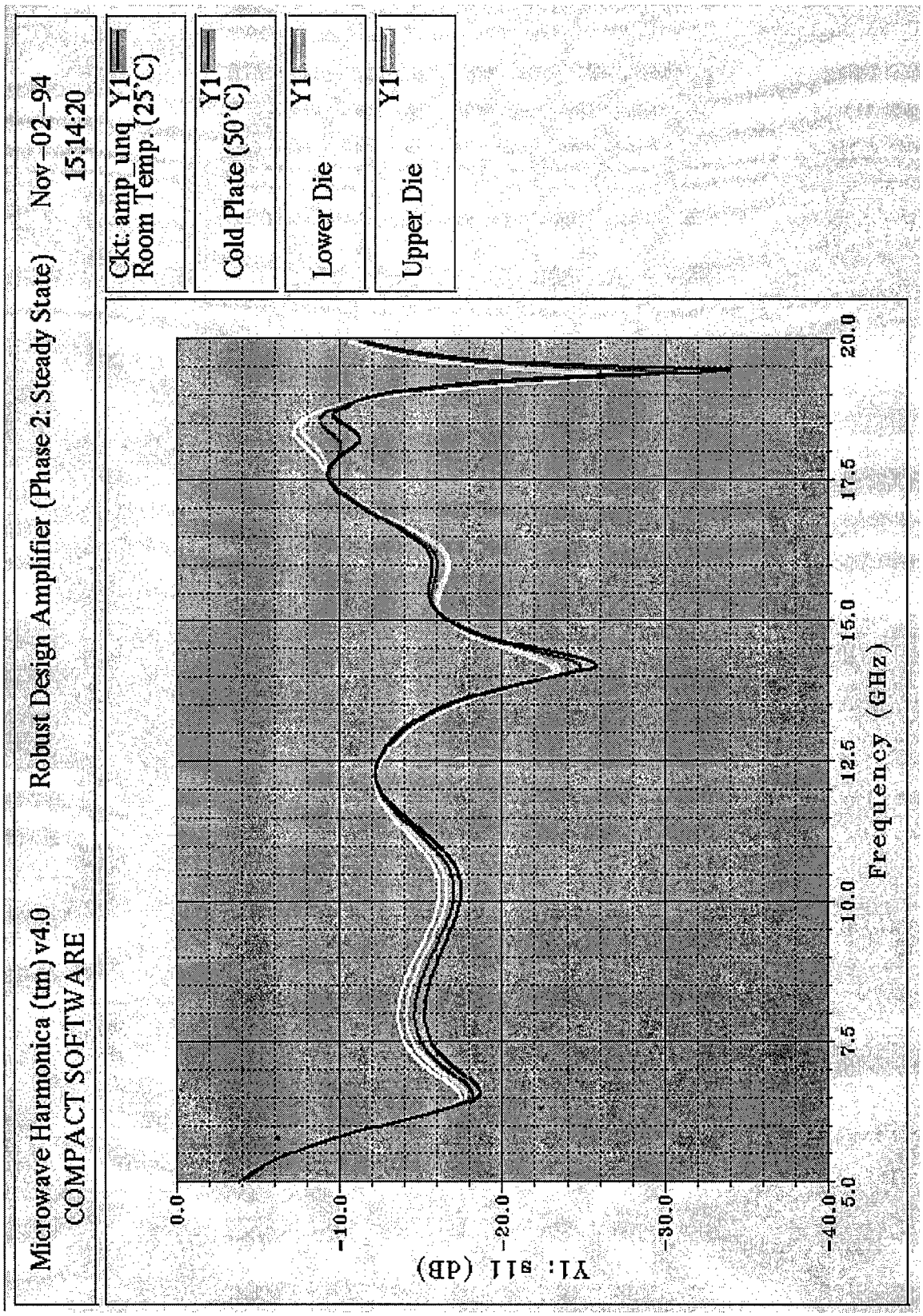


Figure 2.4.1.a. Input Reflection Coefficient (S11)

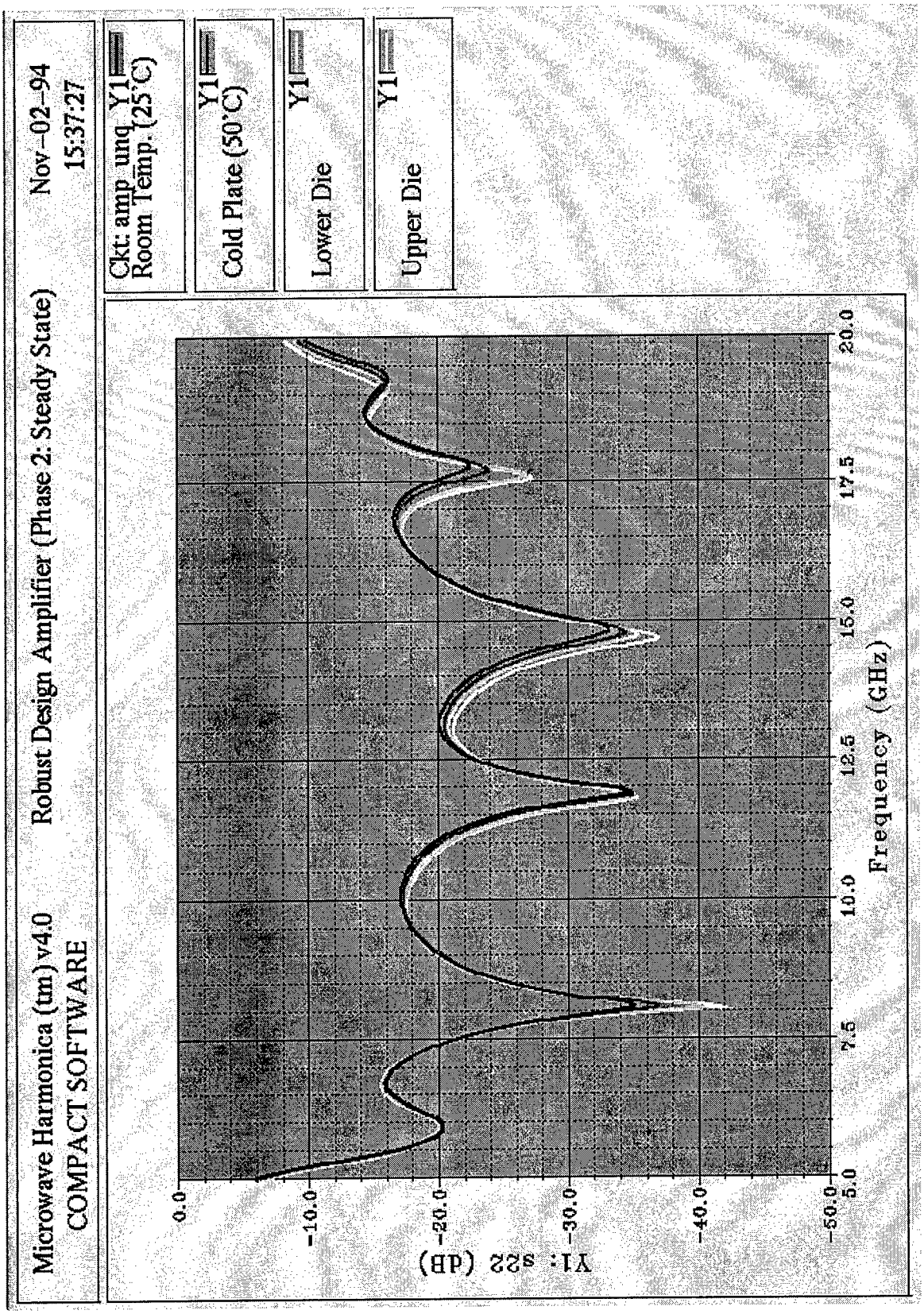


Figure 2.4.1.b. Output Reflection Coefficient (S22)

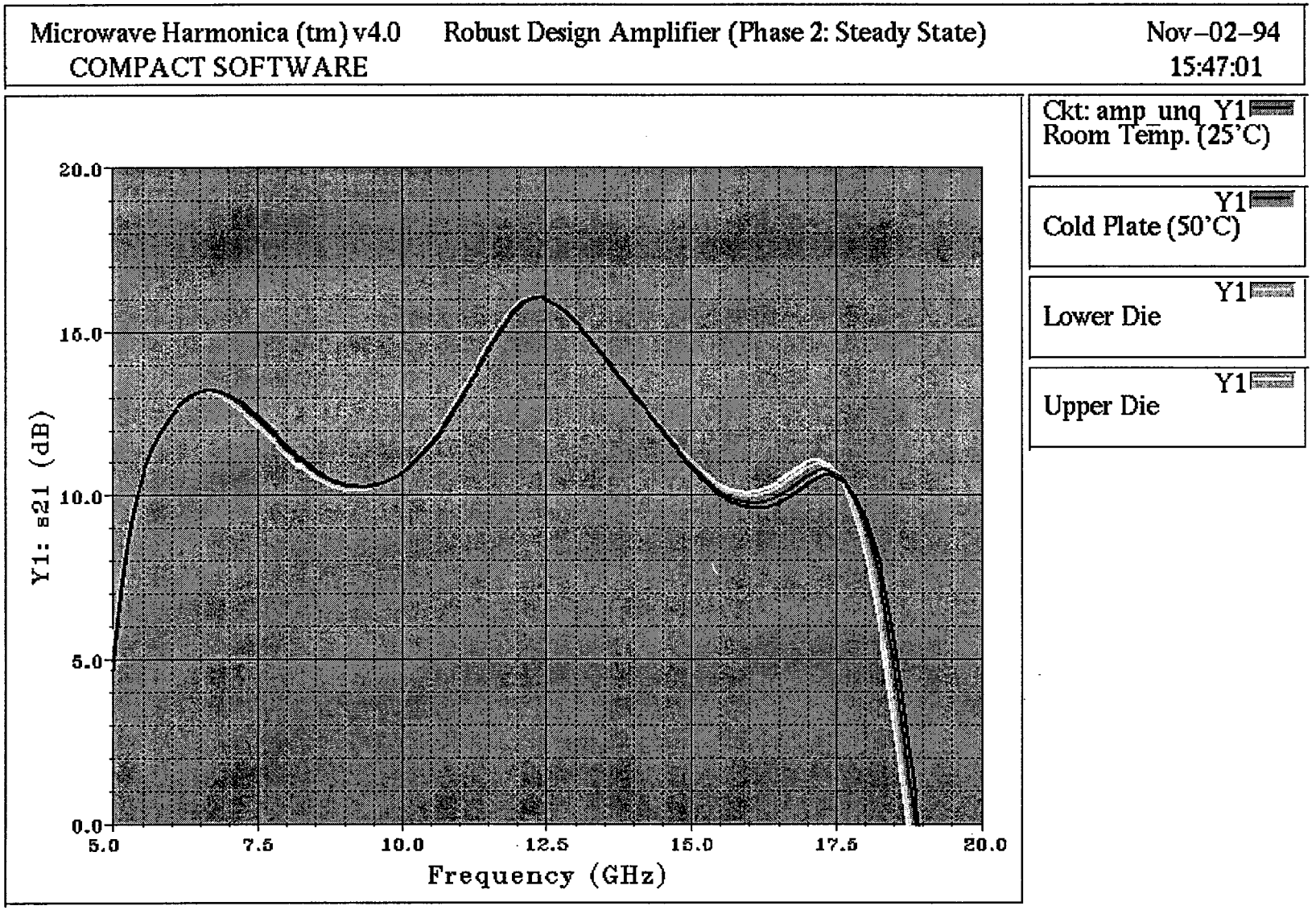


Figure 2.4.1.c. Gain (S21)

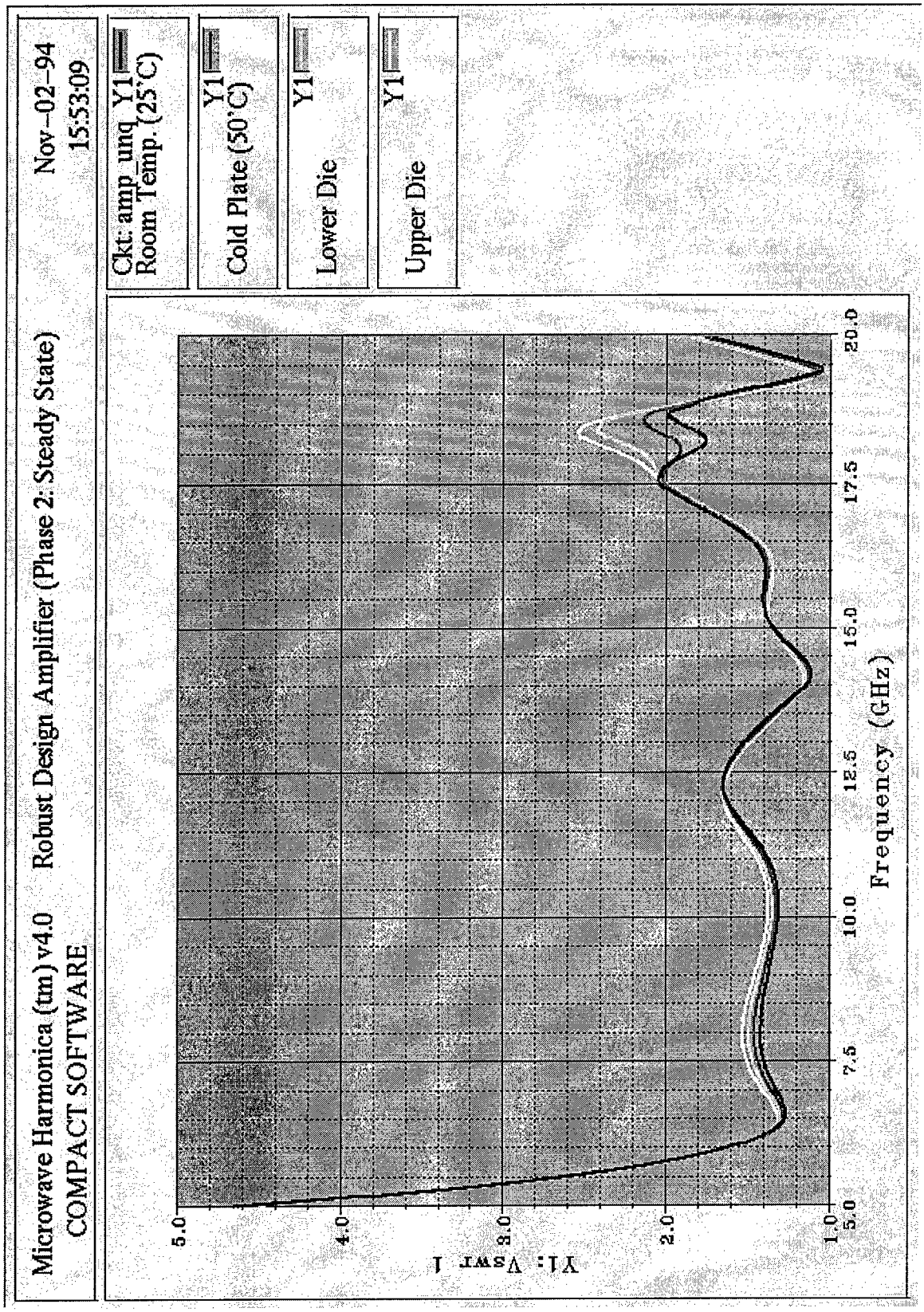


Figure 2.4.1.d. Input Voltage Standing Wave Ratio (VSWR1)

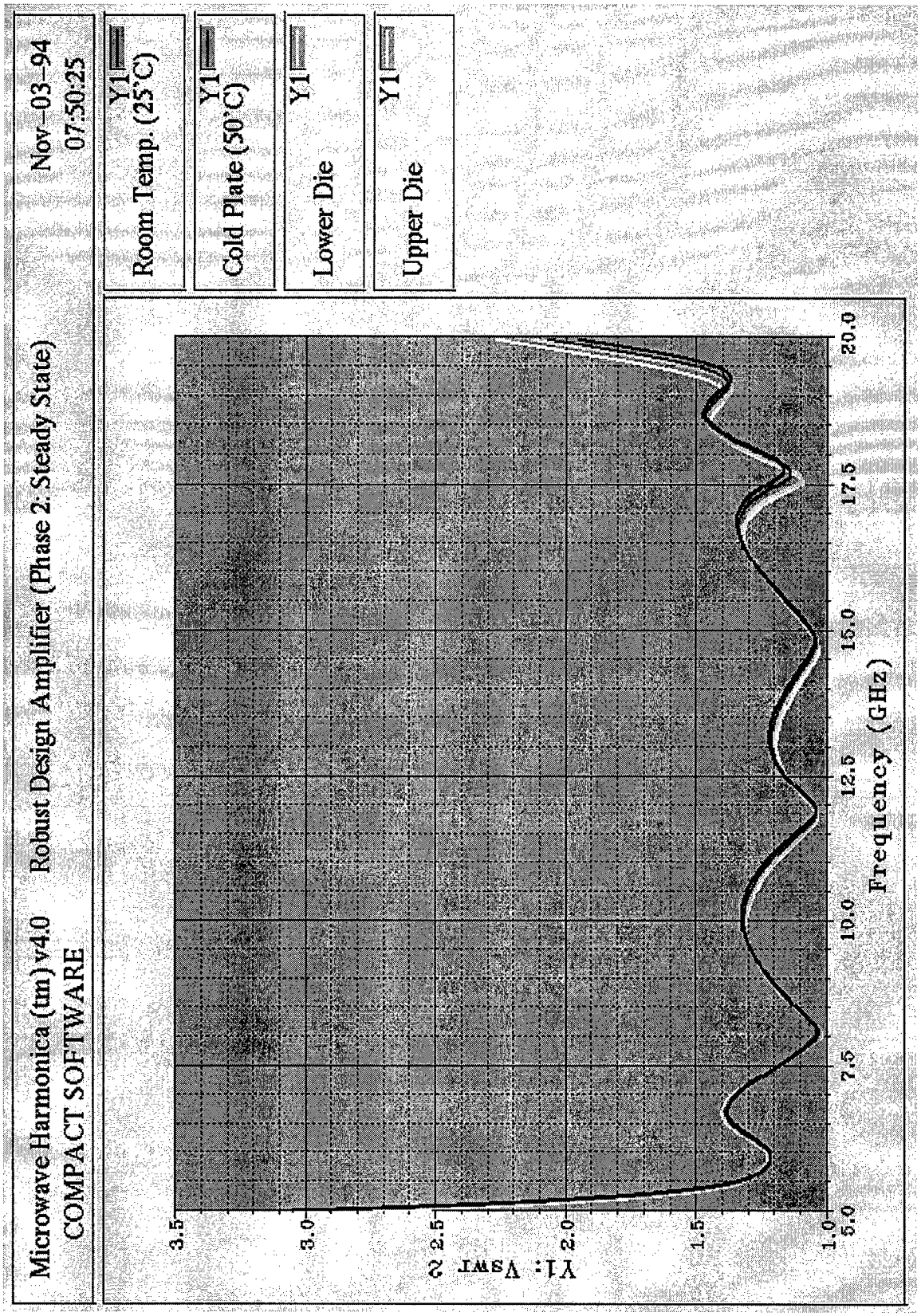


Figure 2.4.1.e. Output Voltage Standing Wave Ratio (VSWR2)

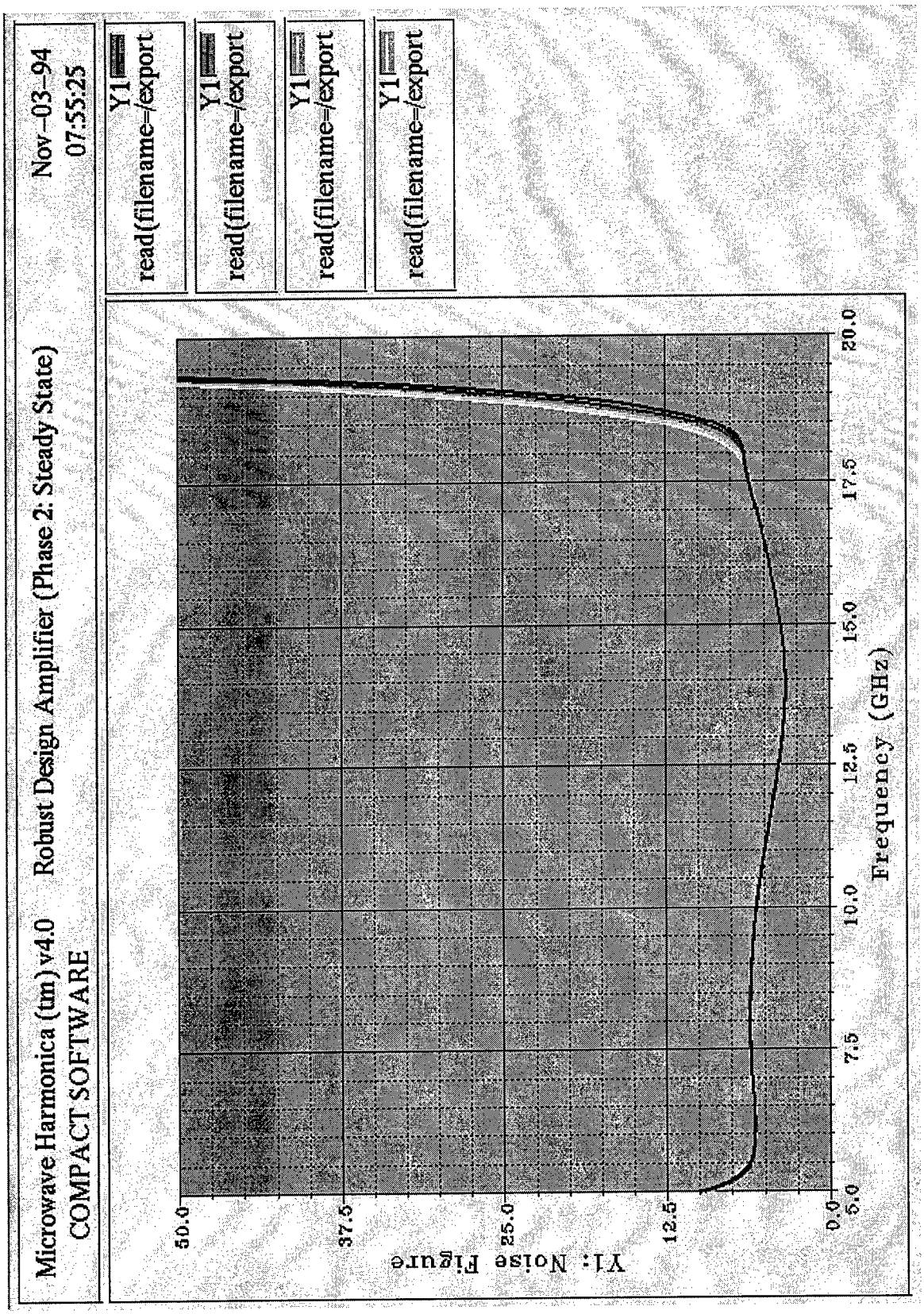


Figure 2.4.1.f. Noise Figure (NF)

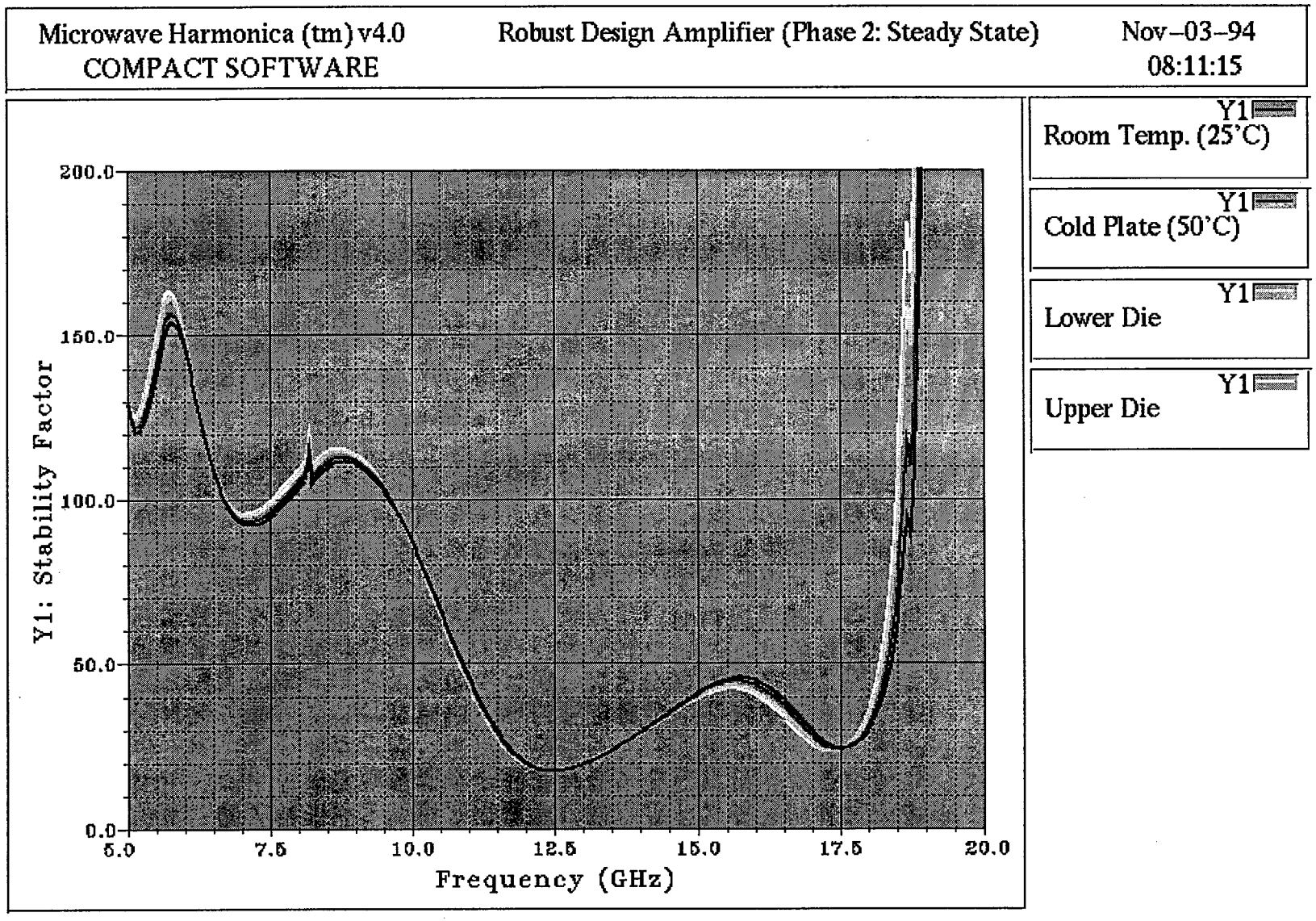


Figure 2.4.1.g. Stability Factor (K)

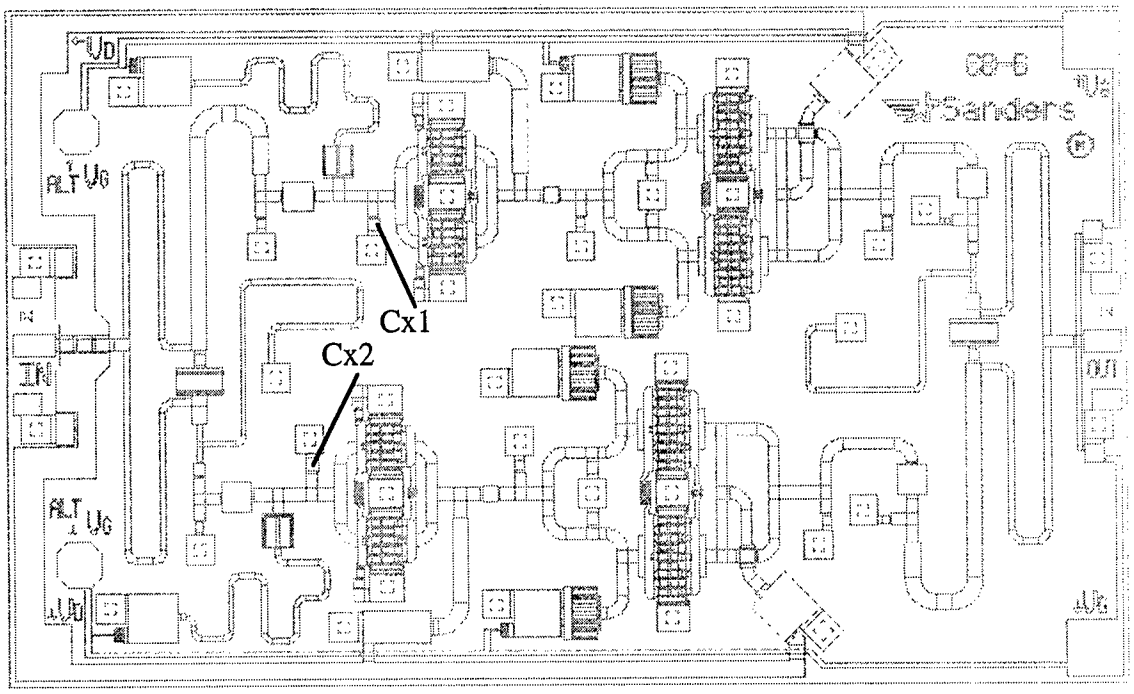


Figure 2.4.2. Capacitor Mismatch

## 3.0 CONCLUSIONS AND RECOMMENDATIONS

Through the utilization of electrical CAD techniques in conjunction with finite element thermal modeling, the influence of three-dimensional heat flow within a MMIC power amplifier chip has been demonstrated. It was found that heat, generated by the active components within the chip, altered the values of two passive elements to the point where one of the circuit parameters did not meet the required specifications. Suggestions were then provided to the chip manufacturer to compensate for the simulated effects.

In order to achieve a more efficient analysis procedure, further work is needed to automate the data transfer between the electrical simulations and the finite element thermal analysis. These include: 1) automatic translation of nodal temperature values

from the thermal model directly to the electrical netlist, and 2) modifying the layout geometry file for direct utilization for both thermal modeling and electrical simulation.

In the past, a special FORTRAN 77 program was written to place the thermal analysis results into the format required for the next analysis.[7] A similar approach could be applied to translating the thermal results into the proper netlist format, especially when a steady state thermal analysis is conducted. This will be more difficult to accomplish for transient thermal analyses. Even though transient analyses have been conducted in the past [2], an attempt to run a transient analysis on the Phase 1 model simulating the pulsed operation of the chip was unsuccessful. The analysis would crash during the run before any results could be obtained. It is believed that there was not enough hard drive space available for the analysis to run completely given the size of the model. Normally, an error message is written to the output file before the computer run is terminated if there is a problem with the input file or FEM. No error message was found in the output file after each attempt was made to run the transient analysis. The exact cause of the analysis failing to run was never determined before the allotted time for this effort came to an end. More work is needed to define the actual limitations of the in-house FEA software when used for conducting transient analyses.

Modification of the layout geometry file in order to provide utilization by both thermal modeling and electrical simulation will probably be a more difficult task. During this effort, it was determined that the layout geometry can currently be read by the in-house software, but provides more information than is required to build a FEM. Manually

manipulating the layout geometry in order to create a FEM was found to be a tedious process, and thus a good candidate for automation.

## 4.0 REFERENCES


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