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Superconducting logic circuits based on Jo phson junctions (JJ) are the fastest, lowest power solid state digital circuit technology known. Large scale integration of such circuits has also been demonstrated. By contrast, current superconducting memory circuits based on flux quantization are not equivalently advanced. Very dense memory chips have not been possible to date and seem unlikely to come without new invention. The goal of this project was to explore alternative approaches to memory that would be compatible with Josephson junction logic circuits and capable of much denser memory arrays. Five new approaches were investigated ranging from modification to the current approach, use of semiconductor CMOS and wholly new concepts based on new physical principles. Three of these were identified as worth pursuing. They are use of cooled CMOS, use of cryogenic hybrid JJ/CMOS memory concepts and a totally new magnetoresistive approach to memory based on the superconductor/ ferromagnet proximity effect.

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for a program on

SUPERCONDUCTING/SEMICONDUCTING HYBRIDS AND ADVANCE MEMORY CONCEPTS FOR SUPERCONDUCTING ELECTRONICS

under ONR URI Grant N00014-92-J-1886

For the period May 1, 1992 to September 30, 1997

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FINAL REPORT

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Overall Goal of the Project

Superconducting logic circuits based on Josephson junctions (JJ) are the fastest, lowest power solid-state digital circuit technology known. Large scale integration of such circuits has also been demonstrated. By contrast, current superconducting memory circuits based on flux quantization are not equivalently advanced. Very dense memory chips have not been possible to date and seem unlikely to come without new invention. The goal of this project was to explore alternative approaches to memory that would be compatible with Josephson junction logic circuits and capable of much denser memory arrays.

The various approaches explored are described below. Three approaches worth pursuing further were identified. They are use of cooled CMOS, use of cryogenic hybrid JJ/CMOS memory concepts and a totally new magnetoresistive approach to memory based on the superconductor/ ferromagnet proximity effect.

Approaches Explored

1) ***Kinetic inductance memory cells.*** A serious limitation of current JJ memory cells (based on the storage of magnetic flux in a superconducting ring) is the large size of the cells. This is a fundamental problem related to the magnitude of the flux quantum of superconductivity. The cells must exhibit a minimum magnetic inductance and hence be of a minimum physical size in order to store stably a flux quantum. This severely limits the density of the memory. An alternative approach was to use the kinetic inductance of a superconductor (associated with the kinetic energy of the superconducting electrons) as opposed to the familiar magnetic inductance to store a flux quantum. The advantage is that the kinetic inductance increases with decreasing physical size, whereas magnetic inductance decreases. This means much denser memories are possible in principle. Studies of this approach were carried out theoretically up to the chip level of design. A serious problem with this approach was uncovered. Without a magnetic inductance it is not possible to maintain isolation between the memory cell and the select and read/write lines. Ways around this problem were found, but only at the expense of very power-hungry circuits [1,2].

2) ***Ferromagnetic cores.*** As an alternative means of reducing the size of current JJ memory cells based on the storage of flux quanta, we also investigated the potential of ferromagnetic cores in the current JJ memory cells in order to achieve the needed inductance at a smaller physical size. This approach is the analog of the use of ferroelectric dielectrics in the capacitors of CMOS DRAMs in order to reduce their size. Also, since magnetic coupling is retained in this approach, there is no loss of isolation. The approach is not without some merit. The main remaining question is what the switching time will be. The switching time of ferromagnets is limited by the zero-field ferromagnetic resonance frequency (i.e., the Larmour frequency due to the intrinsic anisotropy of the material). For three-dimensional ferromagnets there is theoretical limit to the ferromagnetic resonance frequency [$f_r(\mu - 1) = 10^9$ Hz] known as Snoek's law. To get meaningful reductions in area $\mu > 5$ is required, in which case the speed is marginal. On the other hand, for two-dimensional magnets, Snoek's limit become formally infinite. Candidate two-dimensional materials were identified, but were not explored due to experimental limitations [see Felson undergraduate honors thesis.].

3) ***S/F Magnetoresistive Memory.*** In the course of this study, we conceived of an entirely new memory concept based on the superconducting/ ferromagnetic (S/F) proximity effect. Operationally the memory cell is very similar to a giant magnetoresistive (GMR) memory cell. It consists of one superconducting and two magnetic layers in a trilayer. The device is switched by changing the relative direction of the magnetization in the two magnetic layers, through the application of a small magnetic field. The physics of the device is completely different from that of GMR, however. It is based on the oscillatory decay of the superconducting pair wave function predicted to occur in the F layer of an S/F bilayer due to the influence of the exchange interaction on the Cooper pairs. Reversals of the magnetization in one of the two F layers, changes the details of the decaying pair wave function and thereby changes the transition temperature of the superconducting layer by virtue of the proximity effect. Hence, if the operating temperature is chosen appropriately, switching from the normal to the superconducting state can be achieved. The on-state resistance is governed by the normal state sheet resistance of the trilayer and therefore can be scaled to very small dimensions without undermining the operation or impedance level of the device. A complete theory of the operation of this device has been worked out, and we are seeking to continue work on this device under new funding [3,4].

4) ***Complementary Devices and Circuits.*** One of the main problems in single flux based superconducting circuits is the small circuit margins which limit the integration scale and fabrication yield. A limit on the number of devices on a chip may not be as critical for logic, but it is detrimental for memory. Devices with current gain larger than one can improve the circuit margins and hence yield and integration scale. Unfortunately, however, the devices with gain are larger in size for a given critical current density.

The basic idea behind the Complementary Josephson Junction (CJJ) logic family is to utilize the analogies between the operation of a semiconductor NFET and a Josephson gate with an isolated, inductive control line. One can see that the two devices are electrical duals of each other. If we can find the dual of a PFET in the JJ technology, we can build JJ circuits that are analogous to the successful CMOS circuits. Upon examination, one sees that the analog of a PFET is a JJ gate which has zero critical current when there is no input current and a finite (larger than the bias current) critical current when there is an input current. One can implement such a device by (1) simply having an extra control line to bias the device at the node of its control characteristic, (2) utilizing π-junction SQUIDs or (3) utilizing the d-wave pairing symmetry of high temperature superconductors in an otherwise conventional SQUID. The devices should also have minimal off-state critical current in a wide region of control current values. This can be achieved by using sine-shaped junctions with a control line, although this off-state current will have to be very low to avoid problems in large memories at the system level.

Simple CJJ circuits were implemented using HYPRES 2.5kA/cm^2 Niobium technology with sine-shaped junctions. The inverters performed well with wide margins. Simulations indicate an unloaded ring oscillator delay of down to about 15 ps with a 30kA/cm^2 technology. We plan to test the ring oscillator and flip flop memory structures early next year under separate support. Due to the device size limitation, this approach is not expected to impact memory size limitation but the yield may be higher due to better circuit margins [5,6].

5) ***JJ/Cryo CMOS Hybrids.*** We explored the feasibility of constructing hybrid JJ/CMOS memories, in collaboration with Uttam Ghoshal and Professor Van Duzer's group at UC Berkeley. The basic idea of this approach was to use conventional CMOS storage cells to get manufacturable storage densities, but use JJ circuits in the periphery of the memory to speed up the access. Since sensing and driving out the cell data constitute nearly 50% of the total delay in a CMOS RAM, replacing it with JJ sensing allows for a potential doubling of the operating speed. JJ/CMOS level conversion, integration of JJ circuits on a CMOS chip, high speed CMOS decoder design and optimization of the CMOS operating condition are four key problems which need to be solved. Work on the first two of these problems has already been started at UCB. Borrowing techniques from the high speed CMOS SRAM world, we designed a prototype hybrid SRAM in the ORBIT 1.2 μm cryo-CMOS process, with a post-charge based decoder which was simulated to operate down to a cycle time close to 6 gate delays (a conventional SRAM operates at a cycle time close to 18 gate delays). Unfortunately, due to some processing problems with the CMOS portion, we did not get a chance to test the hybrid system. We also studied the problem of optimizing the operating conditions— specifically the temperature of such a hybrid system. We found that for the 1.2 μm process, a 25K operating temperature at 1.5V leads to comparable access times as 4K operation at 1V, while reducing the refrigeration requirement by an order of magnitude [7].

5) ***Cryogenic CMOS.*** Our study of the optimal operating condition for the hybrid system led us to think about the optimal temperature to run a cryogenic pure CMOS part. We measured some ring oscillators made in a low threshold voltage 0.25 μm process, with transistor thresholds close to 0.1V. Based on these measurements we can extrapolate the performance of a complete system at low temperatures. A CMOS memory that dissipates 1Watt running at 100MHz operating at room temperature will run at 130 MHz if cooled to 77 K. Unfortunately, the part and the cyrocooler will dissipate 13 Watts assuming the cooler achieves 20% of the efficiency of an ideal Carnot cooler. While a CMOS process optimized specifically for low temperature can yield a factor of two performance gains, the power overhead at cryo temperatures will be prohibitive in our judgement. What is more promising is to use coolers to keep the CMOS memories around RT (or slightly colder) where the cooling cost is modest. This can greatly improve speed and wire characteristics at more modest power costs [7].

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3. E.A. Demler, G.B. Arnold, M.R. Beasley, "Superconducting proximity effects in magnetic metals," *Phys. Rev. B*. **55**, 15174-15182 (1 June, 1997).

4. Sangjun Oh, D. Youm, and M.R. Beasley, "A New Superconductive Magnetoresistive Memory Element Using Controlled Exchange Interaction," *Appl. Phys. Lett*. 71, 236–2378 (10 Oct. 1997).

5. Esin Terzioglu, D. Gupta, and M.R. Beasley, "Complementary Josephson Junction Circuits," *IEEE Trans. on Applied Superconductivity* **7**, 3642–3645 (June 1997).

6. Esin Terzioglu and M.R. Beasley, "Complementary Josephson Junction Devices and Circuits: A Possible New Approach to Superconducting Electronics," submitted to *IEEE Trans. Applied Supercon.*

7. D. Gupta, B. Amrutur, E. Terzioglu, U. Ghoshal, M.R. Beasley, and M. Horowitz, "Optimization of Hybrid JJ/CMOS Memory Operating Temperatures," *IEEE Trans. on Applied Superconductivity* **7**, 3307–3310 (June 1997).

List of Publications Under This Program

1. George J. Chen, P. Rosenthal, M.R. Beasley, "Kinetic Inductance Memory Cell," *IEEE Trans. on Applied Superconductivity.* **2**, 95-100 (June 1992).

2. G.J. Chen, M.R. Beasley, M. Horowitz, and P. Rosenthal, "Nondestructive Readout Architecture for a Kinetic Inductance Memory Cell," *IEEE Trans. on Appl. Supercon.* **3**, 2702–2705 (March 1993).

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9. Esin Terzioglu and M.R. Beasley, "Complementary Josephson Junction Devices and Circuits: A Possible New Approach to Superconducting Electronics," submitted to *IEEE Trans. Applied Supercon.*

Theses

George J. Chen, Kinetic Inductance Memory Cell and Architecture for Superconducting Computers, PhD Thesis, Stanford University, 1993.

Wayne S. Felson, Ferromagnetic Inductance Josephson Memory, Undergraduate Honors Thesis, Stanford University, 1993.

Patent Disclosures

Invention and Technology Disclosure: S93-133
Title: Josephson Memory with Ferromagnetic Cores
Inventors: Wayne Felson, Malcolm Beasley, and George Chen

Invention and Technology Disclosure: S94-041
Title: Series Josephson Junction Arrays as a High Output Voltage Amplifier
Inventors: E. Terzioglu and M. R. Beasley

Invention and Technology Disclosure: S95-011
Title: Complementary Josephson Junction Devices and Circuits
Inventors: Esin Terzioglu and M. R. Beasley

Invention and Technology Disclosure: S97-022
Title: Superconducting Magnetoresistive Memory Element Using Controlled Exchange Interactions
Inventors: D. Youm and M. R. Beasley