International IEEE Workshop

on

Experimentally Based

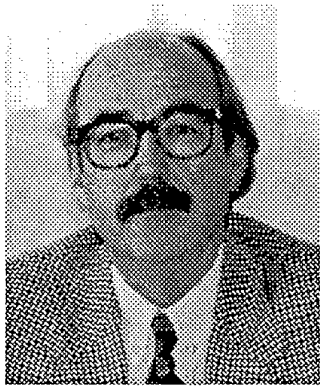
FET Device Modelling &

Related Nonlinear Circuit Design

17-18 July 1997, KASSEL, GERMANY

University of Kassel
Fachgebiet Hochfrequenztechnik (HFT)

July 17th - July 18th, 1997



WELCOME
TO THE UNIVERSITY OF KASSEL

Modern information technology is revolutionizing our current society. We have to give up familiar habits and open ourselves to the international community. Nowadays, 'Globalism' is a very common term symbolizing new technological challenges. Nevertheless, history has shown that new technological trends, though inherently having development risks, should be used to overcome future problems of mankind.

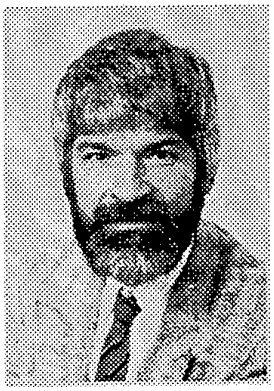
The workshop organized by the Fachgebiet Hochfrequenztechnik at our university will deal with one piece of jigsaw in modern information technology, and the large enrolment of participants from many countries in Europe and abroad shows me that the subjects under discussion are of great interest.

The University of Kassel is a young modern university, located just at the centre of unified Germany. It was founded in 1971 and offers a broad spectrum of subjects, ranging from the Humanities and Social Sciences to Engineering and Fine Arts. Its attractiveness is proved by the fact that the number of applicants has increased annually since its foundation: with 18 000 students the university has already by far surpasssed the size envisaged by its founders.

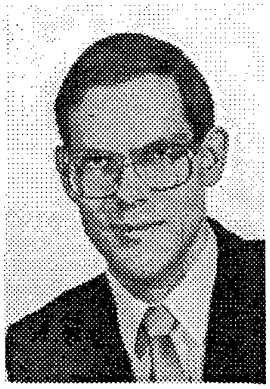
Innovation, *interdisciplinarity*, and *internationality* are key attributes of our University. Our international orientation in education will be strengthened next year when we offer a new masters course in Communications for qualified foreign Bachelor graduates. The course is being funded by the German Academic Exchange Service (DAAD).

I hope this workshop will be helpful in extending and deepening existing scientific cooperation and in starting new joint programs. I wish the workshop much success, and welcome you to our university.

Hans Brinckmann
President



FOREWORD



Welcome to the International Workshop of the German MTT/AP Joint Chapter dealing with FET device modelling and related nonlinear circuit design. The workshop is held in the new Science and Technology building of the Electrical Engineering Faculty of the University of Kassel. The workshop is primarily intended to sum up the present state-of-the-art and to discuss new emerging approaches and concepts in the microwave and millimeterwave CAD based upon the experimental modelling of unipolar III-V semiconductor devices and to evaluate prospects to various applications in e.g. future communication markets.

In the technical sessions, the program is focused on the most exciting key aspects of emerging measurement techniques, small-signal and large-signal equivalent circuit parameter extraction, device modeling concepts, experimental model verification, an outlook to optoelectronic features of FETs, and the hybrid and monolithic circuit design for diverse nonlinear applications as frequency multipliers and mixers. These topics are highlighted in several keynote and contributed papers of recognized authors from nearly all parts of the world. A poster session rounds off the program. Additionally, a panel session which deals with a critical review of the the state-of-the-art, perspectives for first-pass-success and actual issues, is offered for a highly-encouraged discussion including the audience. In a special measurement equipment exhibition, the new HP8510 XF network analyzer (coaxial one-band system up to 110 GHz) is presented for the first time in Europe.

Please enjoy the workshop by listening to the technical papers, engaging in discussions with your colleagues and friends and by participating the social events of the workshop. Regarding recreation and cultural activities, please take advantage of e.g. the Documenta Art Exhibition or visit Kassel's most famous landmark Herkules, Mountain Park Wilhelmshöhe, which is the largest one in Europe.

The institutions and companies named on the following page are acknowledged for their financial support. Particular thanks are expressed to the authors who make this FET modelling and CAD workshop attractive with their original contributions and who have spent time and money to make the workshop feasible.

Again, we welcome you to Kassel and look forward to a lively exchange of ideas among the attendees working on and around the topics of the workshop.

Günter Kompa **Friedbert van Raay**

Acknowledgement

The following institutions and companies
are gratefully acknowledged for their financial support
to this workshop:

European Research Office
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Böblingen, Germany

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Wiesbaden, Germany

WORKSHOP PROGRAM & TABLE OF CONTENTS

Wednesday, July 16th, 1997

Thursday, July 17th, 1997

Workshop Opening:

DC/ SS- Device Characterization & Parasitics

Poster Opening

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Brief Oral Presentation by Authors

12:15 pm - 12:35 pm **Coffee Break & Lunch Box Receipt**

Signal Waveform and Pulsed Measurement & Load Pull
Panel Session 12:35pm - 1:50 pm
Historical Review of Waveform Measurement Techniques, New Results and Future Perspectives

12:35 pm - 12:45 pm **Periodic Time-Domain Waveform Measurement System for Nonlinear Device Characterisation** **7.1 - 4**
V. Porra, K. Lehtinen, M. Sipilä
Helsinki University of Technology, Espoo, Finland.

12:45 pm - 12:55 pm **Vector Measurement of Harmonics in the Frequency Domain: Why, How and What Further?** **8.1 - 5**
Urs Lott
Swiss Federal Institute of Technology (ETH) Zürich, Switzerland

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B. Burchardt
isys, innovative Systeme GmbH, Hamburg, Germany

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F. van Raay, G. Kompa
University of Kassel, Germany

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R. Quéré, J. M. Nebus, J. P. Villotte, J. Obregon
IRCOM, Université de Limoges, France

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C. Gaquière
Institut d'Electronique et de Microélectronique du Nord, Villeneuve d'Ascq Cédex, France

Noise Measurement & Nonlinear Noise in FETs

3:15 pm - 3:35 pm **On-Wafer Noise Parameter Measurements at 60 GHz** **13.1 - 6**
M. Lahdes, M. Sipilä, J. Tuovinen
MilliLab, VTT Information Technology, Finland

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A. Cappy, F. Danneville, G. Dambrine
Institut d'Electronique et de Microélectronique du Nord, Villeneuve d'Ascq Cédex, France

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Optical Control of FETs

4:25 pm - 4:45 pm **Optical Control of HFETs** 15.1 - 6
A. Bangert, J. Rosenzweig, W. Bronner, K. Köhler
Fraunhofer-Institut für Angewandte Festkörperphysik, Freiburg, Germany
Hochschule für Technik, Wirtschaft und Kultur Leipzig, Germany

4:45 pm - 5:05 pm **Design and Fabrication of PINFETs for Optical Receivers** 16.1 - 5
M. M. Rao
Indian Institute of Technology, Madras, India

Nonlinear Modelling & Circuit Design

5:05 pm - 5:25 pm **Accurate Nonlinear Modeling Based on Reliable On-Wafer Characterization** 17.1 - 7
F. Lin, J. Cao
Institute of Microelectronics, Singapore

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Friday, July 18th, 1997

Nonlinear Modelling & Circuit Design

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I. Angelov, L. Bengtsson, M. Garcia, F. van Raay, G. Kompa
Chalmers University of Technology, Gothenburg, Sweden

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C. Rauscher
Naval Research Laboratory, Washington, DC, USA

10:05 am - 10:25 am **Procedure to Extract the Non-linear HEMT Model from Vectorial Non-linear Network Analyzer Measurements** 20.1 - 7
D. Schreurs, J. Verspecht, B. Nauwelaers, A. Van de Capelle, M. van Rossum
ESAT-TELEMIC, Heverlee, Belgium; HP-NMDG, Brussels, Belgium;
IMEC, Heverlee, Belgium

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11:45 am - 12:15 pm	**A New Technological Concept for Optimum Circuit Design at Microwave and Millimeterwave Frequencies** *E. Wasige, G. Kompa, F. van Raay, W. Scholz, I. W. Rangelow, F. Shi, R. Kassing, R. Meyer, M.-C. Amann* University of Kassel, Germany	**23.1 - 5**
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Panel Session: FET Measurement & Modelling - Critical Review of State-of-the-Art, Perspectives for First Pass Success, Current Issues

12:35 pm - 1:15 pm

Moderator: *M. Schlechtweg,* IAF

Speakers: *D. M. Brookbanks*, GMMT
S. Koßlowski, United Monolithic Semiconductors (UMS)
T. Meier, Siemens
D. Root, Hewlett-Packard
H. Sledzik, DASA

Discussion among Software Users and Suppliers & Technologists

Oral Session

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2:05 pm - 2:25 pm	**A Large-Signal HEMT Model for Resistive Mixer Design** *U. Schaper, A. Werthof* Siemens AG, Corporate Technology, Munich, Germany	**26.1 - 5**
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3:15 pm - 3:45 pm	**Short Contributions & Conclusions**	
3:45 pm	**End of Workshop**	

Poster Session

RELIABLE RF TECHNIQUES FOR EXTRACTING PARASITIC ELEMENTS IN MICROWAVE FET'S

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***Abstract*—In this work we have investigated different techniques for computing parasitic inductances from cold-FET measurements. When whole equations are used, the influence of parasitic resistances and capacitances is taken into account. It is found that only source inductance varies with the computation technique. On the other hand, from intrinsic element values, specially C_{DS}, a reliable procedure for parasitic extraction is proposed. Finally, after the frequency dispersion of intrinsic Y parameters, a suitable topology is also proposed to determine the small-signal equivalent circuit in the frequency range 0.045-20 GHz.**

I. INTRODUCTION

THE equivalent circuit of microwave PHEMT's is formed by parasitic and intrinsic elements. Intrinsic elements are computed after a de-embedding process, which is performed once all parasitic elements are extracted. Extensive work exist in the literature for parasitic resistances [1]-[3] estimation and recently, the agreement between DC and RF methods has been established [4]. As for parasitic inductances, source inductance may be very small for on-wafer transistors, and the classical cold-FET [5] technique predicts in some cases L_S negative values. To overcome this problem, the improved cold-FET technique [6] ($V_{GS} > V_{bi} > 0$ with open drain) takes into account the influence of parasitic resistances (R_S, R_D, R_G) and capacitances (C_{PG}, C_{PD}) so as to positive L_S values be obtained. Regarding parasitic capacitances, two models have been proposed [5], and [7]. Nevertheless, their performance in the parasitic inductance estimation has not been studied yet.

On the other hand, apart from reliable methods for evaluating parasitic elements, appropriate circuit topologies are also needed to obtain the best small-signal equivalent circuit model. Different circuit topologies have been put forward for microwave FET modeling [5]-[8], and [9]. The main differences among them rest in the parasitic capacitances location, which depends on the transistor geometry and on the transistor embedding medium. Fig. 1 shows the circuit topologies most frequently used for FET modeling up to 40 GHz.

The aim of this work is to investigate the influence of parasitic capacitances on the evaluation of parasitic inductances. The present paper is also focused on the variations of the small-signal equivalent circuit versus parasitic extraction techniques and versus circuit topologies.

II. EXTRACTION OF PARASITIC RESISTANCES AND INDUCTANCES

A. General Equations

Parasitic resistances and inductances are evaluated by means of an improved cold-FET technique [6]. This technique is based on Z parameters computed from the measurement of S parameters with both DC forward gate bias ($V_{GS} > V_{bi} > 0$, V_{bi} = built-in voltage) and floating drain for different I_{GS} gate currents. Under these conditions, equivalent circuits in Fig. 1 are reduced to the circuits depicted in Fig. 2. In the case of circuit topology shown in Fig. 2(a). the classical Dambrine's equations [5] have been expanded as follows [6]

$$Z_{11}(\omega) = \left\{(R_1+R_3)+\omega^2 C_{PG}(R_1+R_3)\left(L_S - C_{PD}R_3^2\right)\right\} + j\omega\left\{(L_S+L_G) - \left[C_{PD}R_3^2 + C_{PG}(R_1+R_3)^2\right]\right\} \quad (1)$$

$$Z_{12}(\omega) = \left\{R_3+\omega^2 L_S\left[C_{PD}(R_2+R_3)+C_{PG}(R_1+R_3)\right]\right\} + j\omega\left\{L_S - R_3\left[C_{PD}(R_2+R_3) + C_{PG}(R_1+R_3)\right]\right\} \quad (2)$$

$$Z_{22}(\omega) = \left\{(R_2+R_3)+\omega^2 C_{PD}(R_2+R_3)\left(L_S - C_{PG}R_3^2\right)\right\} + j\omega\left\{(L_S+L_D) - \left[C_{PG}R_3^2 + C_{PD}(R_2+R_3)^2\right]\right\} \quad (3)$$

where

$$R_1 = R_G - \frac{R_{CH}}{6} + \frac{n_S kT}{qI_{GS}} \quad (4)$$

$$R_2 = R_D + \frac{R_{CH}}{2} \quad (5)$$

$$R_3 = R_S + \frac{R_{CH}}{2} \quad (6)$$

and

ω angular frequency (rd/s): $\omega=2\pi f$
f frequency (Hz);
R_{CH} channel resistance under the gate (Ω);
n_S ideality factor of the real Schottky diode associated with the transistor under floating drain condition;
k Boltzmann constant (J/K);
T absolute temperature (K);
q electron charge (C).

In the present work we have found that the above expressions still hold for circuit topologies in Fig. 2(b) and 2(c). Therefore, equations (1)-(3) do not depend on circuit topology and are valid for floating drain configuration at $V_{GS} > V_{bi} > 0$.

B. Parasitic Resistances

Real parts of cold-FET Z parameters (1)-(3) are used for determining parasitic resistances as follows. At low frequencies (f < 5 GHz), terms in ω^2 can be neglected with respect to single or combinations of resistive terms R_1, R_2, and R_3. Then, at low frequencies, $\mathrm{Re}(Z_{ij})$ expressions turn equal to those reported by [5] and they depend, among parasitic elements, on parasitic resistances only. In addition, while $\mathrm{Re}(Z_{12})$ and $\mathrm{Re}(Z_{22})$ are bias independent, $\mathrm{Re}(Z_{11})$ depends on the inverse of gate-source forward bias current I_{GS} according to a straight line having a slope a equal to $a = n_S kT/q$ and a y-axis intercept $\mathrm{Re}(Z_{11})^*$ equal to

$$\mathrm{Re}(Z_{11})^* = R_S + R_G + \frac{R_{CH}}{3}. \tag{7}$$

Finally, if the channel resistance R_{CH} is neglected, parasitic resistances are derived from $\mathrm{Re}(Z_{ij})$ by [4],and [6].

$$R_S = \mathrm{Re}(Z_{12}) \tag{8}$$

$$R_D = \mathrm{Re}(Z_{22}) - \mathrm{Re}(Z_{12}) \tag{9}$$

$$R_G = \mathrm{Re}(Z_{11})^* - \mathrm{Re}(Z_{12}). \tag{10}$$

C. Parasitic Inductances

Concerning parasitic inductances, their calculation is achieved using imaginary parts of cold-FET Z parameters (1)-(3). If the influence of parasitic resistances and capacitances is ignored, $\mathrm{Im}(Z_{ij})$ expressions are reduced to those put forward by [5]. These equations are bias independent and allow to compute parasitic inductances very easily.

However, the use of simplified $\mathrm{Im}(Z_{ij})$ expressions is not always possible. Indeed, when small values of L_S are expected, *e.g.* in the case of coplanar transistors, the classical Dambrine's equations may result in L_S negative values. This may be why some authors [10], and [11] take $L_S = 0$.

To overcome this problem, the influence of parasitic resistances and capacitances has to be taken into account and the use of extended expressions (1)-(3) is advised. Parasitic inductances are then computed as follows

$$L_S = \frac{\mathrm{Im}(Z_{12})}{\omega} + A_S \tag{11}$$

$$L_D = \frac{\mathrm{Im}(Z_{22}) - \mathrm{Im}(Z_{12})}{\omega} + A_D \tag{12}$$

$$L_G = \frac{\mathrm{Im}(Z_{11}) - \mathrm{Im}(Z_{12})}{\omega} + A_G \tag{13}$$

where A_S, A_D, and A_G are given by

$$A_S = R_3\left[C_{PD}(R_2 + R_3) + C_{PG}(R_1 + R_3)\right] \tag{14}$$

$$A_D = C_{PD}R_2(R_2 + R_3) - C_{PG}R_1R_3 \tag{15}$$

$$A_G = C_{PG}R_1(R_1 + R_3) - C_{PD}R_2R_3. \tag{16}$$

It should be noticed that for simplified equations reported by Dambrine *et al.* [5], $A_S = A_D = A_G = 0$.

III. Extraction of Parasitic Capacitances

Parasitic capacitances determination is based on Y parameters computed from the measurement of S parameters at DC gate bias beyond the pinch-off voltage V_P and with both source and drain grounding ($V_{DS} = 0$).

Since drain and source electrodes are at the same potential, the depletion zone under the gate is expected to be uniform and symmetrical. According to this hypothesis two models [5], and [7] have been developed for estimating C_{PG} and C_{PD} capacitances.

A. Dambrine's Model [5]

These authors assume that under pinch-off condition with $V_{DS} = 0$, the depletion zone beneath the gate can be modeled by two equal capacitors C_b placed on both sides of the gate. The equivalent circuit corresponding to this model is shown in Fig. 3. If the influence of parasitic resistances and inductances on $\mathrm{Im}(Y_{ij})$ are neglected (f < 10 GHz), C_{PG} and C_{PD} are computed as follows

$$C_{PG} = \frac{\mathrm{Im}(Y_{11}) + 2\,\mathrm{Im}(Y_{12})}{\omega} \tag{17}$$

$$C_{PD} = \frac{\mathrm{Im}(Y_{22}) + \mathrm{Im}(Y_{12})}{\omega}. \tag{18}$$

B. White's Model [7]

In order to FET symmetry be preserved when biasing at $V_{DS} = 0$ and $V_{GS} > |V_P|$, White [7] suggest that the depletion zone under the gate can be modeled by three equal capacitors $(C_b)'$ connected to gate, source and drain electrodes. The equivalent circuit resulting from this model is depicted in Fig. 4. If the influence of parasitic resistances and inductances on $\mathrm{Im}(Y_{ij})$ are ignored (f < 10 GHz), C_{PG} and C_{PD} are given by

$$C_{PG} = \frac{\mathrm{Im}(Y_{11}) + 2\,\mathrm{Im}(Y_{12})}{\omega} \quad (19)$$

$$C_{PD} = \frac{\mathrm{Im}(Y_{22}) + 2\,\mathrm{Im}(Y_{12})}{\omega}. \quad (20)$$

C. Comparison between Models

From (17) and (19) it is noticed that both models yield exactly the same value for the input parasitic capacitance C_{PG}. Regarding the output parasitic capacitance C_{PD}, values from Dambrine's model are larger than those from White's model ($\mathrm{Im}(Y_{12}) < 0$).

On the other hand, when similar values are obtained for Y_{11} and Y_{22} parameters, White's model predicts also similar values for C_{PG} and C_{PD} capacitances. On the contrary, according to Dambrine's model if $Y_{11} \cong Y_{22}$ then $C_{PD} > C_{PG}$.

IV. Results

Three parasitic extraction procedures along with three circuit topologies were investigated in this work.

For all procedures, resistances were estimated after Section II [6]. Concerning other elements, procedures are as follows

- #1 inductances from simplified equations and capacitances from Dambrine's model (procedure by [5] but with floating drain for cold-FET measurements);
- # 2 inductances from whole equations and capacitances from Dambrine's model (procedure by [6]);
- #3 inductances from whole equations and capacitances from White's model (procedure proposed in this work).

As for circuit topologies, referred to as Topo 1, Topo 2 and Topo 3, they are illustrated in Fig. 1(a), Fig. 1(b), and Fig. 1(c) respectively.

A. Measurements

Two transistors supplied by Hewlett-Packard were used in this study. Both are on-wafer n^+GaAs / $In_{0.25}Ga_{0.75}As$ / $n^+Al_{0.28}Ga_{0.72}As$ PHEMT's with a gate length of L_g = 0.25 μm. The first transistor, referred to as F4x25, is arranged with 4 fingers of 25 μm width, while the second transistor, referred to as F2x60, is arranged with 2 fingers of 60 μm width.

Both transistors were used to compare different parasitic extraction techniques with each other. However, transistor F4x25 was used only to determine the intrinsic transistor elements.

Prior to RF measurements in the frequency range 0.45 - 20 GHz, a LRM calibration was performed on the HP8510C network analyzer using Picoprobes® (model 50A-GSG-150-P) as well as ISS standards from Cascade Microtech®.

For all measurements, the average of 120 measurement points was adopted.

Concerning floating drain settings for cold-FET measurements, a low input excitation power was used, typically 0 dBm.

B. Determination of Parasitic Elements

In the first place, Z parameters were computed from cold-FET measurements at open drain configuration for gate forward currents I_{GS} ranging from 10 to 15 mA. Then, $\mathrm{Re}(Z_{ij})$ were used to determine parasitic resistances according to the procedure outlined in Section II.A. The variations against frequency of $\mathrm{Re}(Z_{ij})$ are plotted in Fig. 5(a),and 5(c). In addition, the plot of $\mathrm{Re}(Z_{11})$ versus $(1/I_{GS})$ is shown in Fig. 6. As expected by the theory, a straight line is observed. Parasitic resistances are reported in Table 1.

In a second step, Y parameters were calculated from measurements carried out at V_{DS} = 0 V for different gate bias -3.5 V < V_{GS} < -2.4 V (V_P = -1 V). Then, $\mathrm{Im}(Y_{ij})$ were used for evaluating parasitic capacitances after Dambrine's model and White's model too. Fig. 7 shows $\mathrm{Im}(Y_{ij})$ as a function of frequency. It is noticed that at low frequencies (f < 12 GHz) $\mathrm{Im}(Y_{11})$ almost equals $\mathrm{Im}(Y_{22})$, which agrees with the symmetry condition observed by White [7].

Parasitic capacitance values using Dambrine's and White's models are summarized in Table 2. No bias dependence of C_{PG} nor C_{PD} values is discernible for either models. On the other hand, while White's model estimates similar values of C_{PG} and C_{PD}, Dambrine's model results in larger C_{PD} values than those of C_{PG}, approximately twice as large.

Finally, cold-FET Z parameters were taken up again. This time, $\mathrm{Im}(Z_{ij})$ were used to compute parasitic inductances in accordance with simplified or whole equations (11)-(13). For Dambrine's model (simplified equations), A_S, A_D, and A_G coefficients equal zero. Regarding whole equations, the latter coefficients were calculated after (14)-(16) with the help of parasitic resistances and inductances.

Curves of $\mathrm{Im}(Z_{ij})$ versus frequency are plotted in Fig. 5(b), and 5(d), and parasitic inductance values are reported on Table 3. It is noted that inductance values are constant within ±5% as a function of different extraction procedures, except for L_S inductance. In this case, values may be twice as large as each other, or even they may turn negative (procedure #1 for F2x60).

C. Performance of parasitic extraction procedures in the evaluation of intrinsic elements

In a first step, intrinsic elements for Topo 1-3 were determined from Y^{IN}_{ij} parameters using the Berroth and Bosh de-embedding equations [12]. Their values are reported on Tables 4 - 6 for parasitic extraction procedures #1 - #3 respectively. Small discrepancies are noticed for intrinsic elements, except for C_{DS}, R_i, and τ.

which depend strongly on parasitic extraction procedure and / or topology. Concerning C_{DS} capacitance, regardless of topology, procedures #1 and #2 lead to negative values, while procedure #3 results in positive values. Therefore, procedure #3 seems to be more suited to parasitic extraction.

In a second step, circuit topology operation limit was established from the frequency dispersion yield for real parts of intrinsic transistor Y parameters Y^{IN}_{ij}. These parameters were calculated after a de-embedding process from S parameters measured at $V_{GS} = 0$ V and $V_{DS} = 3$ V. Fig. 8 shows $\mathrm{Re}(Y^{IN}_{ij})$ as a function of frequency for parasitic extraction procedure # 3 and for Topo 1-3. No dispersion is observed on any $\mathrm{Re}(Y^{IN}_{ij})$ for Topo 1 in the whole frequency range. On the contrary, Topo 2 and 3 bring about $\mathrm{Re}(Y^{IN}_{21})$ variations at frequencies greater than 15 GHz. Hence, in this work Topo 1 seems to be more appropriate for transistor modeling at frequencies up to 20 GHz.

V. Conclusion

The influence of parasitic resistances and capacitances on parasitic inductance computation is only discernible on L_S inductance.

Our results suggest that best estimations are obtained from White's model for C_{PG} and C_{PD}, and from whole expressions (11)-(13) for L_S, L_D, and L_G (procedure #3).

Concerning circuit topologies it is found that Topo 1 is the more appropriated for modeling the transistor up to 20 GHz.

Errors between measured and modeled S parameters are shown in Fig. 9 for procedure #3 and Topo 1. Errors are within 2% for S_{11}, S_{21}, S_{22} and within 5% for S_{12}.

Acknowledgment

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Element	F4x25	F2x60
R_S (Ω)	5.1	3.9
R_D (Ω)	7.1	6.2
R_G (Ω)	1.1	2.9

Table 1. Parasitic resistances measured at $V_{GS} > V_{bi} > 0$ with open drain.

Element	F4x25 [1] / [7]	F2x60 [1] / [7]
C_{PG} (fF)	33 / 33	15.5 / 15.5
C_{PD} (fF)	55 / 32.8	39 / 14.59

Table 2. Parasitic capacitances measured at V_{DS} = 0 V and $V_{GS} > |V_P|$.

Element	F4x25 (a) / (b) / (c)	F2x60 (a) / (b) / (c)
L_S (pH)	3.7 / 8.5 / 7.2	-0.36 / 1.74 / 0.84
L_D (pH)	38.7 / 37 / 43	41 / 39 / 42
L_G (pH)	44 / 42 / 46	48 / 46 / 49

Table 3. Parasitic inductances measured at $V_{GS} > V_{bi} > 0$ with open drain. (a) procedure #1, (b) procedure #2, and (b) procedure #3.

	I_{DS} = 35 mA	V_{DS} = 3 V	V_{GS} = 0 V
Element	Topo 1	Topo 2	Topo 3
C_{GS} (fF)	113.3	112.9	115.5
C_{GD} (fF)	11.66	11.8	11.83
C_{DS} (fF)	-19.64	-19.76	-19.34
R_i (Ω)	2.195	-1.761	1.954
g_{DS} (mS)	2.63	2.58	2.69
g_m (mS)	47.63	47.53	48.41
τ (ps)	0.865	0.917	0.81

Table 4. Intrinsic element values for different topologies according to parasitic extraction procedure #1. Data for transistor F4x25 (L_g = 0.25 µm).

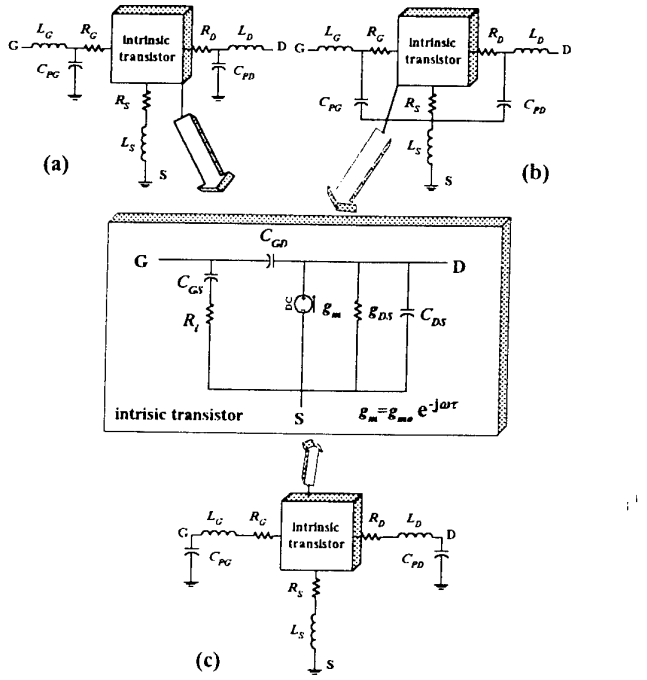

Fig. 1. Circuit topologies investigated in this work. (a) Topo 1, (b) Topo 2, and (c) Topo 3.

	I_{DS} = 35 mA	V_{DS} = 3 V	V_{GS} = 0 V
Element	Topo 1	Topo 2	Topo 3
C_{GS} (fF)	113	112.7	111.5
C_{GD} (fF)	11.66	11.96	11.81
C_{DS} (fF)	-18.99	-19.28	-18.61
R_i (Ω)	-0.037	-1.038	-0.267
g_{DS} (mS)	2.65	2.539	2.7
g_m (mS)	47.76	47.54	48.47
τ (ps)	0.887	1.08	0.875

Table 5. Intrinsic element values for different topologies according to parasitic extraction procedure #2. Data for transistor F4x25 (L_g = 0.25 µm).

	I_{DS} = 35 mA	V_{DS} = 3 V	V_{GS} = 0 V
Element	Topo 1	Topo 2	Topo 3
C_{GS} (fF)	113	112.3	115.1
C_{GD} (fF)	11.68	11.86	11.82
C_{DS} (fF)	9.74	9.49	10.22
R_i (Ω)	0.377	-0.466	0.104
g_{DS} (mS)	2.62	2.56	2.661
g_m (mS)	47.47	47.28	48.07
τ (ps)	0.55	0.657	0.544

Table 6. Intrinsic element values for different topologies according to parasitic extraction procedure #3. Data for transistor F4x25 (L_g = 0.25 µm).

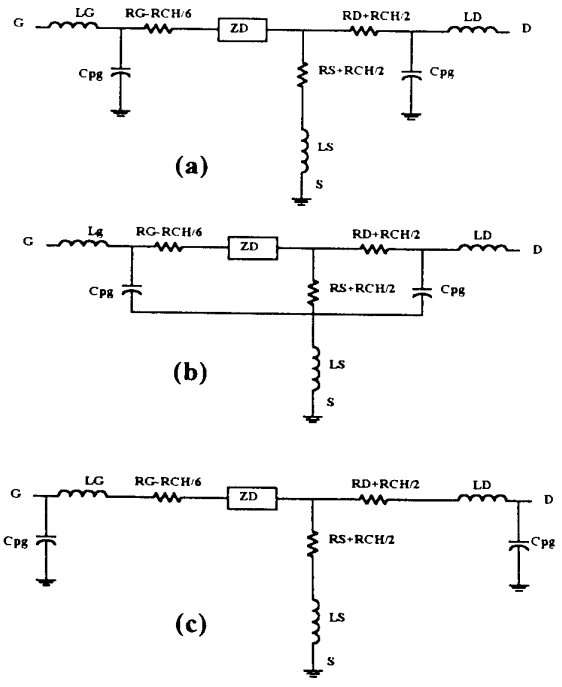

Fig. 2. Small-signal equivalent circuit for measurements with floating drain at $V_{GS} > V_{bi} > 0$. (a) Topo 1, (b) Topo 2, and (c) Topo 3.

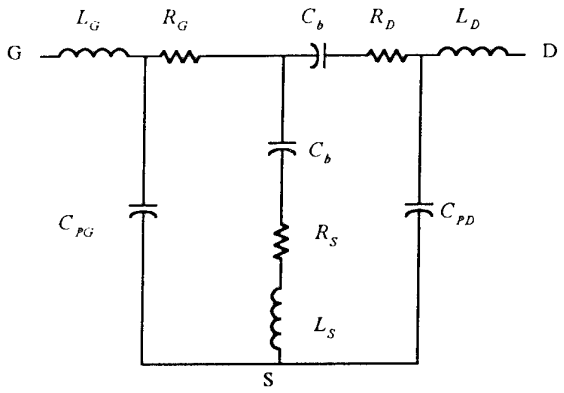

Fig. 3. Small-signal equivalent circuit for measurements at $V_{DS} = 0$ and $V_{GS} > |V_P|$). Dambrine's model [5].

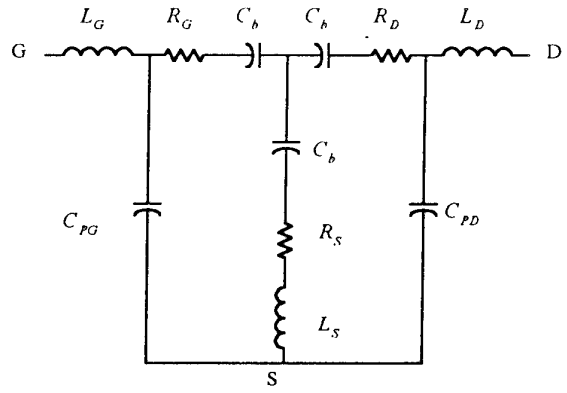

Fig. 4. Small-signal equivalent circuit for measurements at $V_{DS} = 0$ and $V_{GS} > |V_P|$). White's model [7].

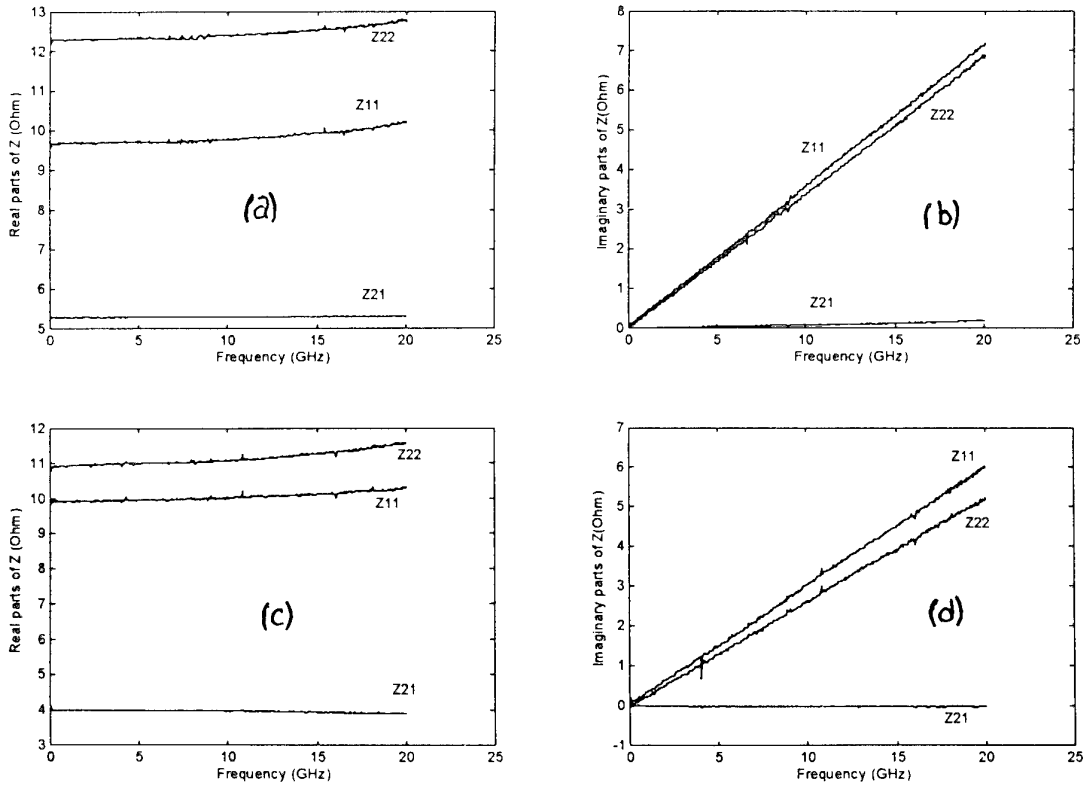

Fig. 5. Real and imaginary parts of Z parameters versus frequency. Measurements with floating drain at $V_{GS} > V_{bi} > 0$. (a), (b) Transistor F4x25 and (c), (d) transistor F2x60.

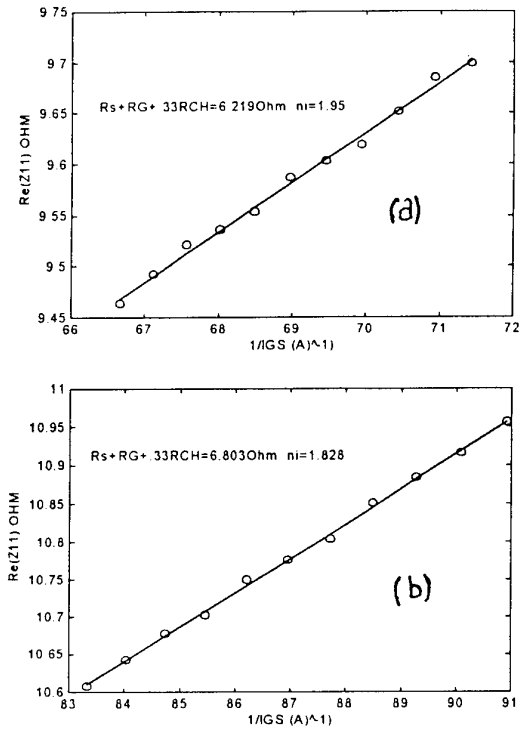

Fig. 6. Real part of Z_{11} versus frequency. Measurements with floating drain at $V_{GS} > V_{bi} > 0$. (a) Transistor F4x25 and (b) transistor F2x60.

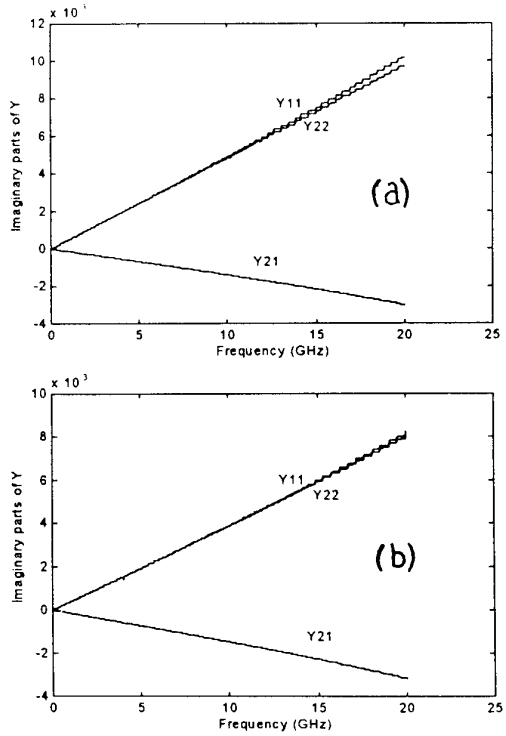

Fig. 7. Imaginary parts of Y parameters against frequency. Measurements at $V_{DS} = 0$ and $V_{GS} > |V_P|$). (a) Transistor F4x25 and (b) transistor F2x60.

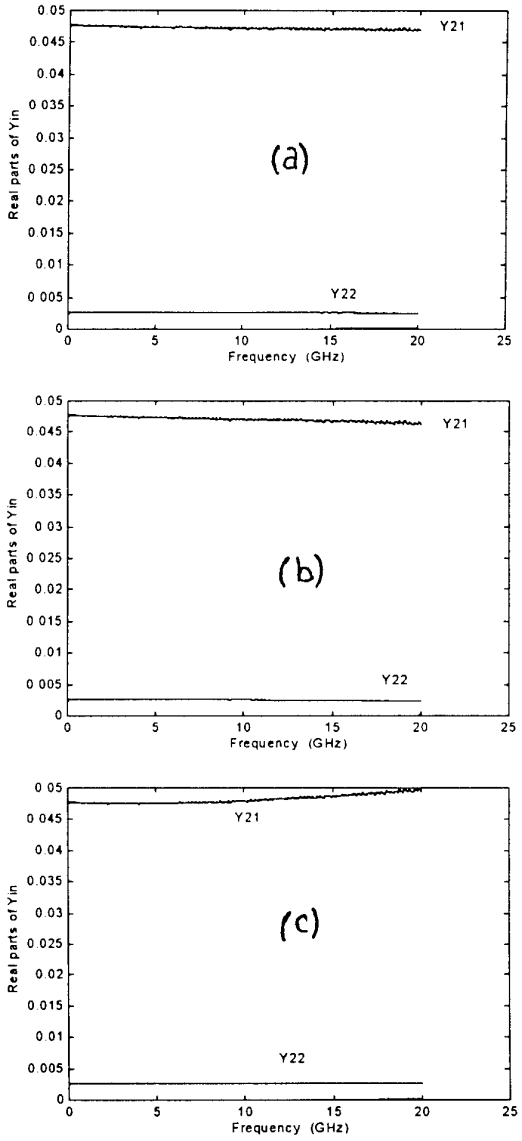

Fig. 8. Frequency dispersion of intrinsic Y parameter real parts for different circuit topologies. (a) Topo 1, (b) Topo 2, and (c) Topo 3. Calculations were carried out for transistor F4x25 using parasitic extraction procedure #3.

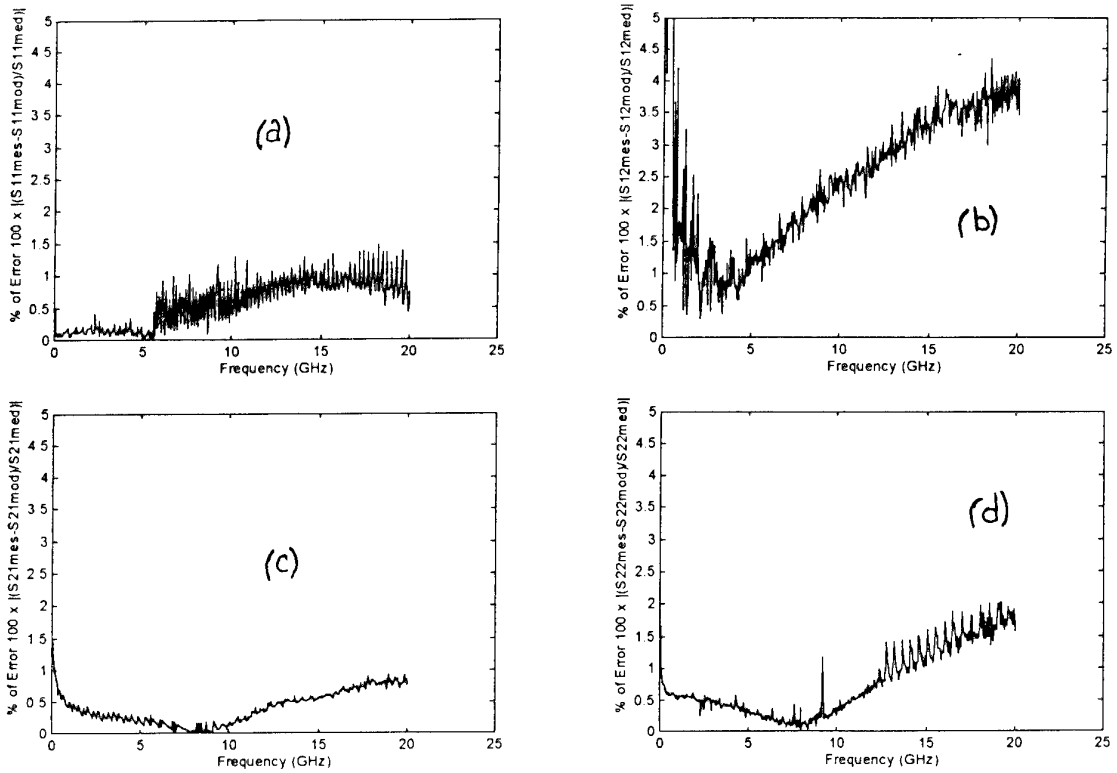

Fig. 9. Percent errors versus frequency for S parameters. (a) S_{11}, (b) S_{12}, (c) S_{21}, (d) S_{22}. Calculations were carried out for transistor F4x25 using parasitic extraction procedure #3 and circuit topology Topo1.

A New Method for the Determination of the Multi-bias Gate Inductance and Drain Resistance of a FET from Measured S-parameters

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Abstract

A new method is proposed to evaluate the gate inductance and drain resistance directly from the S-parameters of a GaAs FET transistor. By using the overall Z-parameters and their respective derivatives, the gate inductance and drain resistance are, for the first time, expressed as explicit equations in terms of the multi-bias Z-parameters. These expressions result in both a reduction in the number of unknown variables and a smaller search space for optimization. The proposed method is tested on a 1x40μm GaAs FET. Good agreement between measured and simulated S-parameters from 1 -20GHz is achieved.

I. Introduction

An accurate determination of the small-signal equivalent circuit parameters of a microwave GaAs FET plays a very crucial role in the nonlinear modeling of the device. The exact knowledge of the extrinsic elements is important for obtaining the accuracy of the whole equivalent circuit because the calculated values of the bias-dependent intrinsic equivalent circuit depend on the extrinsic elements. The equations for the bias-dependence intrinsic elements have already been derived by many authors [1-5]. However, a few authors [3,5] have managed to derive the bias-dependence of one of the extrinsic elements while other authors [1-4] have simplified the equivalent circuit and postulated that the extrinsic elements are bias-invariant. This assumption can greatly simplify the small-signal equivalent circuit, but adds more burden to the final extraction of the bias-dependent intrinsic non-linear elements.

Generally, the conventional approach of obtaining the extrinsic elements is through the "passive" measurements, where the FET is biased similar to a diode with zero drain voltage. An alternative small-signal hybrid-pi model [6-7] is then proposed to fit the measured results. The validity of this model is questionable as this alternate model, which is a simplified, one dimensional model, is based on the assumption that there exists symmetry and homogeneity in the gate-source region. The assumption of bias independence is not justified for the parasitic R_s and R_d. The source and drain resistances consist of three parts: The first and second parts describe the resistances between the calibration plane and the device as well as the contact resistance and may be assumed to be constant, too. The third part, however, describes the resistance between the source or drain contact at one side and the beginning of the space charge region below the gate at the other side, which changes with dc-bias due to the two-dimensional charge control. A significant variation of source and drain resistances with drain and gate voltages has been numerically shown by Tsung et. al. [11] and experimentally verified by Byun et. al. [12]. Besides, it is not possible to extract, from dc-measurements, R_g which models the resistivity per unit length of the gate transmission line.

Therefore, the determination of the small-signal equivalent circuit element entails firstly the accurate extraction of the extrinsic elements. It is thus the intention of this paper to present the bias-dependent expressions of the gate inductance and drain resistance using only the measured S-parameters of the device. The precise knowledge of the bias-dependence of the gate inductance and drain resistance in terms of the remaining extrinsic elements gives more insight into the device and enables a further improvement of the technological process. In this paper, a novel method of extracting all the bias-dependent parameters of the small-signal equivalent circuit is presented. This novel method is subsequently used to model a 1x40μm GaAs FET. Good agreement between the calculated and measured S-parameters from 1-20GHz is obtained.

II. The Detailed Derivation

The adopted small-signal equivalent circuit is as depicted in Figure 1. The extrinsic elements are found outside the dashed-box of Figure 1. The pad capacitances, C_{pgs} and C_{pds}, are omitted in this equivalent circuit for ease of explanation. They are subsequently added and explained in the last paragraph of this section.

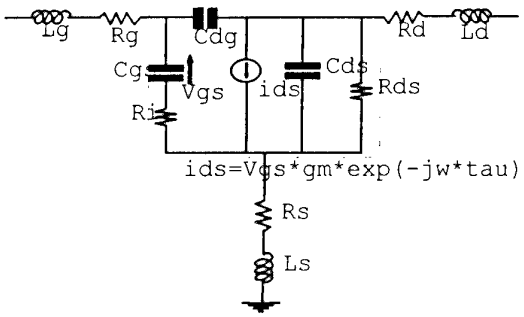

Figure 1: Equivalent circuit of GaAs MESFET. The dashed-box contained the intrinsic part of the device.

The intrinsic elements are related to the extrinsic elements by the following expressions:

$$\Delta\begin{bmatrix} \frac{j\omega C_{gs}}{1+j\omega C_{gs}R_i}+j\omega C_{dg} & -j\omega C_{dg} \\ \frac{g_m e^{-j\omega\tau}}{1+j\omega C_{gs}R_i}-j\omega C_{dg} & g_{ds}+j\omega\left(C_{dg}+C_{ds}\right)\end{bmatrix}$$
$$=\begin{bmatrix} Z_{22_r}+jZ_{22_i} & -\left(Z_{12_r}+jZ_{12_i}\right) \\ -\left(Z_{21_r}+jZ_{21_i}\right) & Z_{11_r}+jZ_{11_i}\end{bmatrix}+$$
$$\begin{bmatrix} -\left(R_d+R_i\right)-j\omega\left(L_d+L_i\right) & R_i+j\omega L_i \\ R_i+j\omega L_i & -\left(R_i+R_g\right)-j\omega\left(L_i+L_g\right)\end{bmatrix}, \quad (1)$$

where

$$\Delta=\Delta_r+j\Delta_i, \quad (2)$$
$$=R_g\left(R_g+R_i-Z_{11_r}\right)-\omega L_d\left(\omega L_i+\omega L_g-Z_{11_i}\right)+\eta_1+$$
$$j\left[R_d\left(\omega L_g+\omega L_i-Z_{11_i}\right)+\omega L_d\left(R_g+R_i-Z_{11_r}\right)+\eta_2\right], \quad (3)$$
$$\eta_1=R_g\left(R_i-Z_{22_r}\right)-R_i\left(Z_{11_r}-Z_{12_r}-Z_{21_r}+Z_{22_r}\right)-$$
$$\omega L_g\left(\omega L_i-Z_{22_i}\right)+\omega L_i\left(Z_{11_i}-Z_{12_i}-Z_{21_i}+Z_{22_i}\right)$$
$$-Z_{11_r}Z_{22_r}+Z_{12_r}Z_{21_r}+Z_{11_i}Z_{22_i}-Z_{12_i}Z_{21_i}, \quad (4)$$
$$\eta_2=\left[R_g\left(\omega L_i-Z_{22_i}\right)+R_i\left(-Z_{11_i}+Z_{12_i}+Z_{21_i}-Z_{22_i}\right)+\right.$$
$$\omega L_g\left(R_i-Z_{22_r}\right)-\omega L_i\left(Z_{11_r}-Z_{12_r}-Z_{21_r}+Z_{22_r}\right)$$
$$\left.+Z_{11_i}Z_{22_r}-Z_{21_i}Z_{12_r}-Z_{12_i}Z_{21_r}+Z_{22_i}Z_{11_r}\right], \quad (5)$$

Z is the total measured Z-parameters of the device and subscripts r and i denote respectively the real and imaginary terms. Through the second matrix elements of equation (1), we obtain respectively from the imaginary and real terms

$$C_{dg}=\frac{1}{\omega}\left[\frac{\Delta_i\left(R_i-Z_{12_r}\right)-\Delta_r\left(\omega L_i-Z_{12_i}\right)}{\Delta_r^2+\Delta_i^2}\right]=\frac{R_i-Z_{12_r}}{\Delta_i\omega}, \quad (6)$$

and

$$\Delta_r\left(R_i-Z_{12_r}\right)+\Delta_i\left(\omega L_i-Z_{12_i}\right)=0. \quad (7)$$

The second equality of equation (6) is obtained using equation (7). Eliminating jwC_{dg} from the first matrix elements of equation (1) with the second matrix elements, we get

$$\frac{j\omega C_{gs}}{1+j\omega C_{gs}R_i}=\frac{\left(\Delta_r-j\Delta_i\right)\left[Z_{22_r}-Z_{12_r}-R_d+j\left(Z_{22_i}-Z_{12_i}-\omega L_d\right)\right]}{|\Delta|^2}. \quad (8)$$

By equating the real and imaginary terms of equation (8), and using equation (7), we arrive at the following expression after manipulations

$$\omega C_{gs}R_i=$$
$$\frac{\left(\omega L_i-Z_{12_i}\right)\left(Z_{22_r}-Z_{12_r}-R_d\right)+\left(Z_{12_r}-R_i\right)\left(Z_{22_i}-Z_{12_i}-\omega L_d\right)}{\left(\omega L_i-Z_{12_i}\right)\left(Z_{22_i}-Z_{12_i}-\omega L_d\right)-\left(Z_{12_r}-R_i\right)\left(Z_{22_r}-Z_{12_r}-R_d\right)}. \quad (9)$$

From equations (9) and (8), we see that

$$1+j\omega C_{gs}R_i=\frac{\Delta_r\left(Z_{22_i}-Z_{12_i}-\omega L_d\right)-\Delta_i\left(Z_{22_r}-Z_{12_r}-R_d\right)}{\Delta_r\left(Z_{22_i}-Z_{12_i}-\omega L_d\right)-\Delta_i\left(Z_{22_r}-Z_{12_r}-R_d\right)}+$$
$$\frac{+j\left[\Delta_r\left(Z_{22_r}-Z_{12_r}-R_d\right)+\Delta_i\left(Z_{22_i}-Z_{12_i}-\omega L_d\right)\right]}{\Delta_r\left(Z_{22_i}-Z_{12_i}-\omega L_d\right)-\Delta_i\left(Z_{22_r}-Z_{12_r}-R_d\right)}. \quad (10)$$

Using equations (7), (8) and (10), both C_{gs} and R_i can be respectively found to be

$$C_{gs}=$$
$$C_{dg}\left[\frac{\left(Z_{22_i}-Z_{12_i}-\omega L_d\right)^2+\left(Z_{22_r}-Z_{12_r}-R_d\right)^2}{\left(R_i-Z_{12_r}\right)\left(Z_{22_r}-Z_{12_r}-R_d\right)-\left(\omega L_S-Z_{12_i}\right)\left(Z_{22_i}-Z_{12_i}-\omega L_d\right)}\right], \quad (11)$$

and

$$R_i=\frac{1}{\omega C_{dg}}$$
$$\left[\frac{\left(Z_{22_i}-Z_{12_i}-\omega L_d\right)\left(R_i-Z_{12_r}\right)-\left(Z_{22_r}-Z_{12_r}-R_d\right)\left(\omega L_i-Z_{12_i}\right)}{\left(Z_{22_i}-Z_{12_i}-\omega L_d\right)^2+\left(Z_{22_r}-Z_{12_r}-R_d\right)^2}\right]. \quad (12)$$

Similarly, from the fourth matrix elements of equations (1), (6) and (7), both g_{ds} and C_{ds} can respectively be given as

$$g_{ds}=$$
$$\omega C_{dg}\left[\frac{\left(R_i-Z_{12_r}\right)\left(Z_{11_r}-Z_{12_i}-\omega L_g\right)-\left(\omega L_i-Z_{12_i}\right)\left(Z_{11_i}-Z_{12_r}-R_g\right)}{\left(R_i-Z_{12_r}\right)^2+\left(\omega L_i-Z_{12_i}\right)^2}\right], \quad (13)$$

and

$$C_{ds}=$$
$$C_{dg}\left[\frac{\left(R_i-Z_{12_r}\right)\left(Z_{11_i}-Z_{12_i}-R_g\right)-\left(\omega L_i-Z_{12_i}\right)\left(Z_{11_r}-Z_{12_r}-\omega L_g\right)}{\left(R_i-Z_{12_r}\right)^2+\left(\omega L_i-Z_{12_i}\right)^2}\right], \quad (14)$$

The g_m and τ, which are found by using equations (1), (7) and (10), are respectively given as

$$g_m = \frac{\omega C_{gs}\sqrt{(Z_{12r}-Z_{21r})^2+(Z_{12i}-Z_{21i})^2}}{\sqrt{(R_s-Z_{12r})^2+(\omega L_s-Z_{12i})^2}}\sqrt{1+\omega^2 C_{gs}^2 R_s^2}\,, \tag{15}$$

and

$$\tau = \frac{-1}{\omega}\left[\tan^{-1}\left(\frac{Z_{12i}-Z_{21i}}{Z_{12r}-Z_{21r}}\right)+\tan^{-1}\left(\omega C_{gs}R_s\right)+\tan^{-1}\left(\frac{R_s-Z_{12r}}{\omega L_s-Z_{12i}}\right)\right]. \tag{16}$$

Since there are a total of eight expressions in equation (1), we should be able to derive eight explicit equations. Seven explicit expressions, namely, equations (6), and (11) to (16), that relate the unknown variables to the total Z-parameters have already been derived. The missing explicit expression can be solved through equation (7) for the unknown R_d. It is given as

$$R_s = \frac{\omega L_d\left((R_s-Z_{12r})(\omega L_s+\omega L_g-Z_{11i})-(\omega L_s-Z_{12i})(R_g+R_s-Z_{11r})\right)}{(R_g+R_s-Z_{11r})(R_s-Z_{12r})+(\omega L_s-Z_{12i})(\omega L_s+\omega L_g-Z_{11i})}+ \frac{-\eta_1(R_s-Z_{12r})-\eta_2(\omega L_s-Z_{12i})}{(R_g+R_s-Z_{11r})(R_s-Z_{12r})+(\omega L_s-Z_{12i})(\omega L_s+\omega L_g-Z_{11i})}. \tag{17}$$

Equation (17) is new and has not been reported in the literature. In the conventional optimization approach [1-2,9-10], the values of the extrinsic elements are taken to be of the same accuracy and can assume wide initial guesses. This large variation in the initial guesses, as seen by equation (17), can result in non-physical or local-minimum solutions. Equation (17), which is exact, shows the correlation among all the extrinsic elements, and for some large values of the other extrinsic elements, R_d can become negative. By having this equation, the search space is thus reduced.

So far, we have fully utilized equation (1) to obtain expressions that explicitly relate the extrinsic elements to the intrinsic elements. Nothing is mentioned about how the 5 extrinsic elements should be or equivalently related to the overall Z-parameters. To alleviate this problem, the derivative of the real and imaginary terms of equation (1) *with respect to frequency*, which provides additional 8 equations, can be utilized. The derivative of the real and imaginary parts of the overall Z-parameters with respect to frequency can be obtained by interpolation or measurements. As the equivalent circuit elements must be valid for each measurement frequency, the derivative of the intrinsic and extrinsic elements with respect to frequency should be zero. Alternatively, we are saying that the equivalent circuit elements are *independent of frequency*. We are able to take the derivative of the real and imaginary terms of the overall Z-parameters because the matrix equations found in (1) for both the real and imaginary terms are continuous functions. Since these equations are highly complex, for brevity, only some useful equations are shown in this paper.

After some tedious mathematical manipulations, the expression that relates L_g to the other unknown variables, namely, R_s, L_s and L_d is obtained by solving the following set of equation, which is given as:

$$L_g = \frac{a_{11}b_2 - a_{21}b_1}{a_{11}a_{22}-a_{12}a_{21}}, \tag{18}$$

where

$$a_{11} = (R_s-Z_{12r})(\omega Z'_{12i}+2(R_s-Z_{12r}))+ (\omega L_s-Z_{12i})(2\omega L_s-3Z_{12i}+\omega Z'_{12r}), \tag{19}$$

$$a_{12} = \omega\left[\left(R_s-Z_{12r}\right)\left(Z_{12i}-\omega Z'_{12i}\right)+\left(\omega L_s-Z_{12i}\right)\omega Z'_{12r}\right], \tag{20}$$

$$a_{21} = (\omega L_s-Z_{12i})(2(Z_{12r}-R_s)-\omega Z'_{12r})-(R_s-Z_{12r})(Z_{12i}-\omega Z'_{12i}), \tag{21}$$

$$a_{22} = \omega\left[(R_s-Z_{12r})(2(R_s-Z_{12r})+\omega Z'_{12r})-(\omega L_s-Z_{12i})(Z_{12i}-\omega Z'_{12i})\right], \tag{22}$$

$$b_1 = \left[(R_s-Z_{12r})^2+(\omega L_s-Z_{12i})^2\right](\omega Z'_{11r}-Z_{11r}+R_s)- (\omega L_s-Z_{12i})(R_s-Z_{12r})(Z_{11i}-Z_{12i})+ (\omega L_s-Z_{12i})^2(Z_{11r}-Z_{12r})-(R_s-Z_{12r})(Z_{11r}-R_s)(Z_{12i}-R_s-\omega Z'_{12i})+ (R_s-Z_{12r})(Z_{11i}-\omega L_s)(Z_{12r}-\omega Z'_{12i})- (Z_{11r}-R_s)(Z_{12i}-\omega Z'_{12i})(\omega L_s-Z_{12r})- (\omega L_s-Z_{12i})(Z_{11i}-\omega L_s)(Z_{12r}-R_s-\omega Z'_{12r}), \tag{23}$$

$$b_2 = \left[(R_s-Z_{12r})^2+(\omega L_s-Z_{12i})^2\right](\omega Z'_{11i}-Z_{11i})+(R_s-Z_{12r})^2(Z_{11i}-Z_{12i})- (\omega L_s-Z_{12i})(Z_{11r}-Z_{12r})(R_s-Z_{12r})+ (\omega L_s-Z_{12i})(Z_{11r}-R_s)(Z_{12r}-\omega Z'_{12r}-R_s)- (\omega L_s-Z_{12i})(Z_{11i}-\omega L_s)(Z_{12r}-\omega Z'_{12i})- (R_s-Z_{12r})(Z_{11r}-R_s)(Z_{12i}-\omega Z'_{12i})- (R_s-Z_{12r})(Z_{11i}-\omega L_s)(Z_{12r}-R_s-\omega Z'_{12r}). \tag{24}$$

The superscript prime denotes the operator $\partial/\partial\omega$, and subscripts r and i denote the real and imaginary terms. For the ease of implementation, L_d, R_g, R_s and L_s have been taken, instead, as the unknown variables for

optimization even though they can be expressed as analytical functions using the remaining derivative equations. This is because except for L_g, all the other extrinsic elements are found to be very sensitive to the numerical errors contributed by the derivatives.

All the expressions as derived in equations (1) to (24) are not confined solely to the equivalent circuit as shown in Figure 1. To include the pad capacitances, the following transformations as given in equations (1) to (24) should be taken:

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \frac{1}{\left[(Y_{11} - j\omega C_{pg})(Y_{22} - j\omega C_{pd}) - Y_{12}Y_{21}\right]} \begin{bmatrix} Y_{22} - j\omega C_{pd} & -Y_{12} \\ -Y_{21} & Y_{11} - j\omega C_{pg} \end{bmatrix}, \quad (25)$$

where Y_{ij} with i,j=1,2 is the total Y-parameters of the device.

III The New Algorithm

The conventional approach usually does not check circuit validity and determines extrinsic and intrinsic elements simultaneously. Extrinsic elements determined in this way often invalidate the circuit when the operating bias is changed, and often additional measurements performed at pinch-off, DC, low frequency, and cold state are required to narrow down the search [1-2,9-10].

Our method is an extension of K. Shirakawa's approach [4] in that the intrinsic elements as well as some of the extrinsic elements are used as an optimization criteria. The first objective function for our approach is presented as

$$\varepsilon_1^{\varepsilon}(R_s, R_g, L_s, L_d) = \frac{1}{N-1} \sum_{i=0}^{N-1} \left| \rho_k f_k(\omega_i, R_s, R_g, L_s, L_d) - \overline{\sum_{j=0}^{N-1} \rho_k f_k(\omega_j, R_s, R_g, L_s, L_d)} \right|^2, \quad (26)$$

where functions f_k with k varying from 0 to 8 represent respectively the equations (6), (7), (11), (12), (13), (14), (15), (16), and (17), N is the total number of frequency points, ρ_k is a normalizing factor to make f_k varying between 0 and 1, and the overbar indicates the mean value. We have intentionally omitted equation (18) in equation (26) so as to eliminate numerical error during our objective function computation. For stable calculation, the discrepancy between the measured and calculated S-parameters must also be checked. For this reason, the mean values of equations (6) to (7), and (11) to (18) are used to evaluated a second objective function given as

$$\varepsilon_2(R_s, R_g, L_s, L_d) = \sum_{p=1}^{2}\sum_{q=1}^{2}\sum_{i=0}^{N-1} \sigma_{pq} \left| S_{pq}^{m}(\omega_i, R_s, R_g, L_s, L_d) - \bar{S}_{pq}^{c}(R_s, R_g, L_s, L_d) \right|, \quad (27)$$

where superscripts c and m denote respectively the calculated and measured S-parameters, σ_{pq} (arbitrarily fixed at 0.5) is the weighting factor and the overbar indicates that the mean values of f_0 to f_8 are used to compute the S-parameters. By taking the mean values of f_0 to f_8, we are actually saying that the global solution occurs at the mean values of these functions. The extended error vector is then composed of

$$\varepsilon(R_s, R_g, L_s, L_d) = \begin{bmatrix} \varepsilon_1^{\varepsilon}(R_s, R_g, L_s, L_d) \\ \varepsilon_2(R_s, R_g, L_s, L_d) \end{bmatrix}. \quad (28)$$

By selectively assigning values for the remaining extrinsic parameters, namely, R_s, R_g, L_s, and L_d, the elements of equations (6) to (18) can then be evaluated by iteration. The method as proposed by Yanagawa et. al. [3] can be used to generate the initial guesses for R_s, R_g, L_s, and L_d. These initial guesses are then used in equations (6) to (18), and (26) to (28). The pad capacitances can be included for optimization but they are only optimized with the pinch-off S-parameters, and, for convenience, are maintained constant at these values for other biased S-parameters. R_s, R_g, L_s, and L_d are optimized for all biased S-parameters. This new algorithm, which is fully based on the measured multi-biased S-parameters, does not assume a different circuit topology at pinch-off and thus is exact in nature.

IV Experiments, Results And Discussions

The flow-chart for this new iterative algorithm is presented in Figure 2. First, the pinch-off S-parameters are utilized in the optimization. The initial guesses for C_{pgs}, C_{pds}, R_s, R_g, L_s, and L_d are used to compute the remaining extrinsic and intrinsic parameters. Next, the extended error vector, ε, is estimated from (28). The parameters, C_{pgs}, C_{pds}, R_g, R_s, L_s, and L_d, are subsequently updated to reduce ε using the Levenberg-Marquart method. Once the error ε is sufficiently small, the next biased S-

parameters are utilized. C_{pgs} and C_{pds} are maintained at their pinch-off values and the remaining unknowns, namely, R_s, R_g, L_s, and L_d are then optimized. The algorithm is stopped when all the multi-bias unknown variables, R_s, R_g, L_s, and L_d, are extracted for all the biased S-parameters. A Matlab program is written based on the iterative flow-chart.

Since the algorithm is heavily dependent on the derivatives of the Y-parameters (if equation (25) is used) or Z-parameters (if C_{pgs} and C_{pds} are not included), more points are needed to ensure an accurate estimation of the gradients at turning points of the curves. The gradient of the Y-parameters can be computed by

$$\frac{dY_i}{d\omega} = \frac{Y_i(f+\Delta f) - Y_i(f-\Delta f)}{4\Delta f\pi}, \qquad (29)$$

where i denotes either the real or imaginary terms and Δf is taken as 10^{-9}. This new technique eliminates the additional measurements required, and thus is an advantage over the conventional approach [1-10].

The new method is tested on a 1x40μm GaAs FET, and the simulated and measured S-parameters are given in Figures 3(a) to 3(d). As noted, good agreement is obtained for the simulated and measured results.

The validity of the extracted equivalent circuit elements is confirmed by the invariance of the elements' values with frequency. Figure 4 shows the C_{gs} dependence on the gate and drain bias whereas Figure 5 shows the R_s dependence on the drain bias with variation in the gate voltages. More results will be presented in the workshop.

V Conclusions

A novel method for extracting the small-signal equivalent circuit elements has been proposed. For the first time, the bias dependence drain resistance and gate inductance expressions are derived. The new method results in a smaller search space and a reduction in the number of unknown variables for optimization. Good agreement between the measured and simulated S-parameters for a 1x40μm GaAs FET has been obtained.

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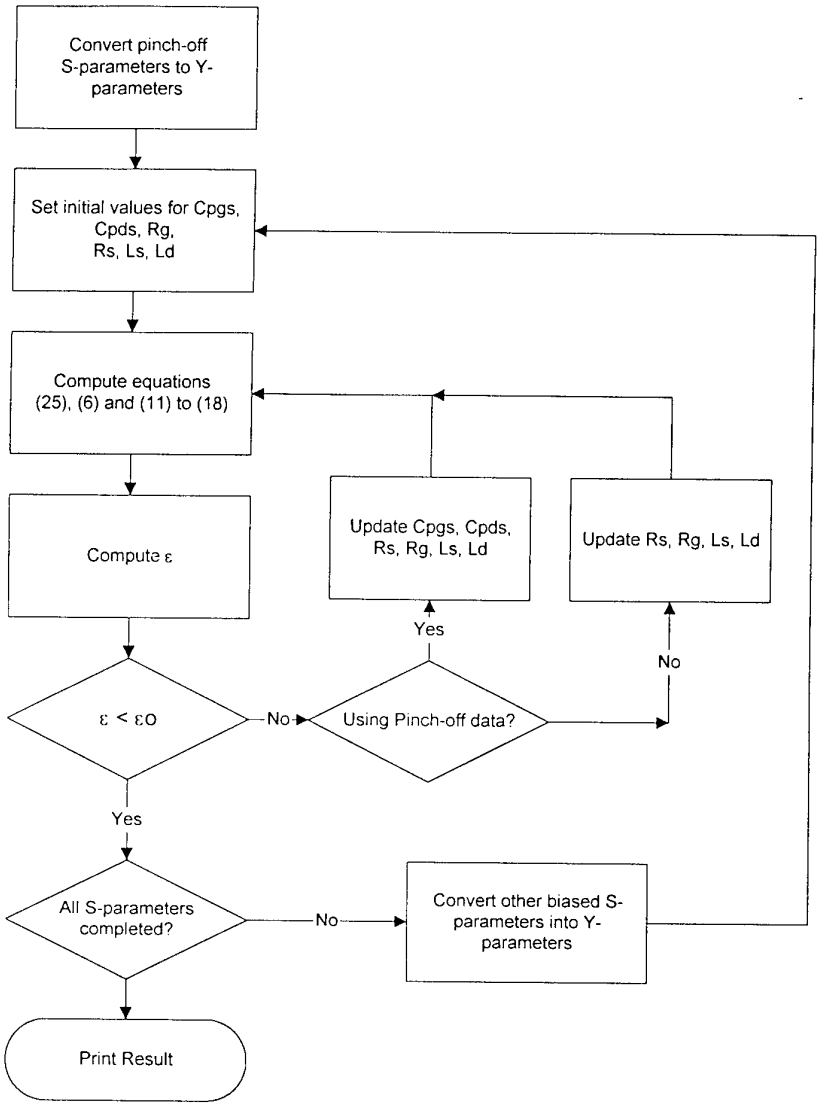

Figure 2 Algorithm

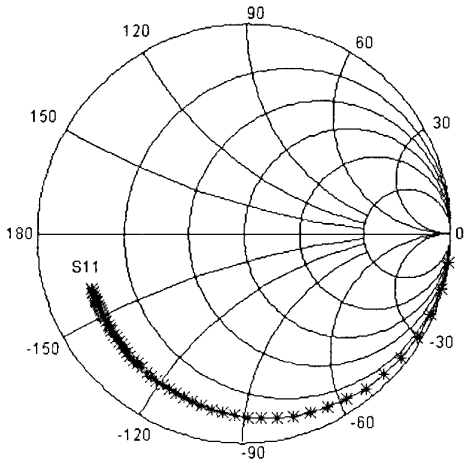

Figure 3(a): S11 parameters of 400μm GaAs MESFET. Frequency: 0.5 to 26.5 GHz. Bias: V_{ds}=8V, I_{ds}=0.6I_{dss}. Solid-line: Simulated values. Asterisk: Measured values.

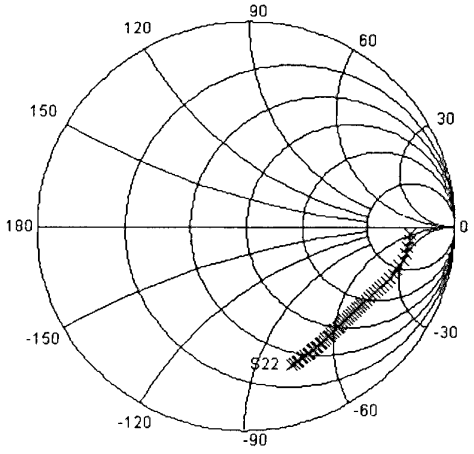

Figure 3(b): S22 parameters of 400μm GaAs MESFET. Frequency: 0.5 to 26.5 GHz. Bias: V_{ds}=8V,I_{ds}=0.6I_{dss}. Solid-line: Simulated values. Crosses: Measured values.

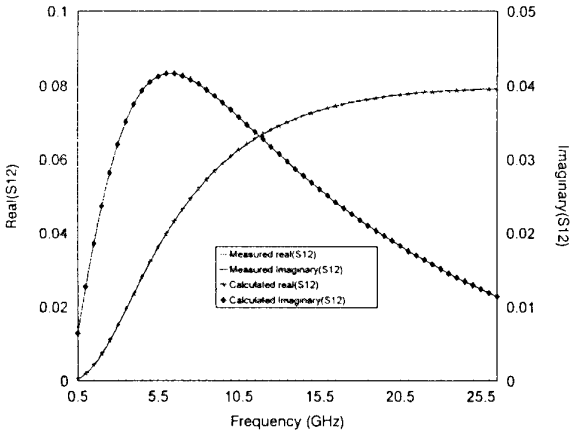

Figure 3(c): Real and imaginary parts of S_{12} (gate width=400μm). Bias: V_{ds}=8V,I_{ds}=0.6I_{dss}

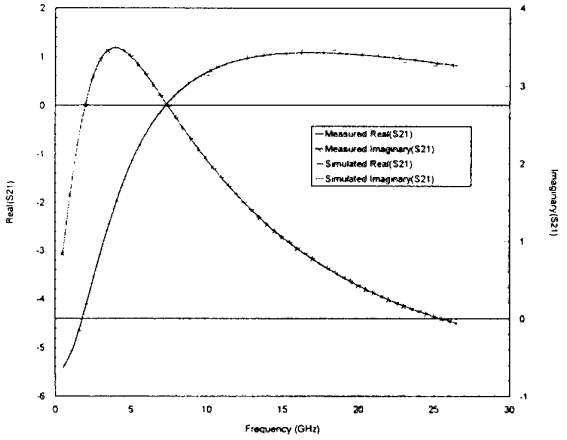

Figure 3(d): Real and imaginary parts of S_{21} (gate width=400μm). Bias: V_{ds}=8V,I_{ds}=0.6I_{dss}

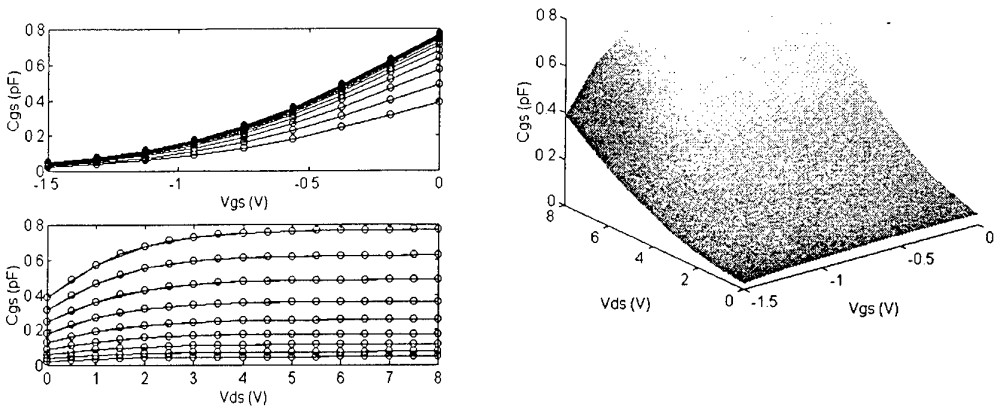

Figure 4 C_{gs} dependence on gate (-1.5 to 0 V) and drain bias (0 to 8V)

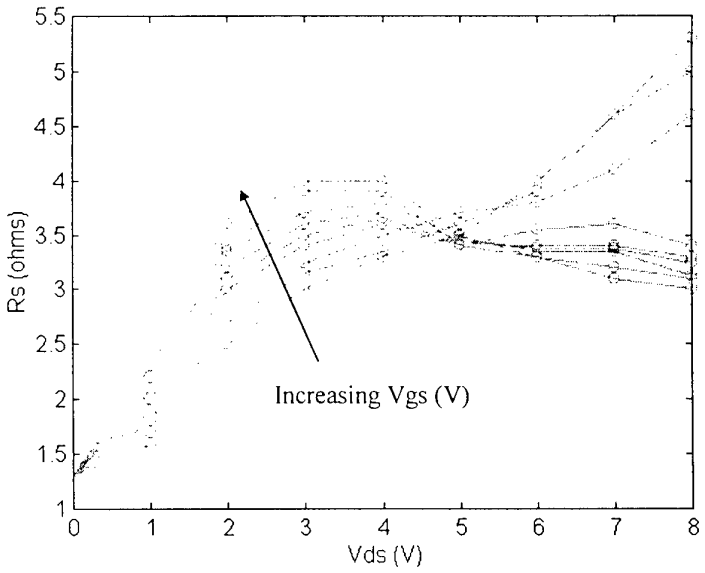

Figure 5 R_s dependence on drain and gate voltages.
(Gate voltages varying from -1.5 to 0 V)

A simplified approach to determine a small signal equivalent circuit up to 60 GHz.

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Abstract

In this paper, we present a simplified approach to determine a small signal equivalent circuit up 60 GHz. Our study is based on the knowledge of the influence of the extrinsic parameters on the intrinsic one. We have obtained a good agreement between measured and calculated S parameters without optimisation procedure. We have also performed S parameters with three different test sets which show the difficulty to use V-band S parameter measurements to determine the equivalent circuit. Errors of measurement have been equally analysed, to point out the additional problems of extracting a small signal equivalent circuit in millimeterwave.

Introduction

The design of MMIC's needs a correct model for the passive components, but also a good description of the device behaviour. For this reason, an accurate equivalent circuit of the device is required and must be validated in all the frequency bandwidth. In this paper, we will focus on the determination of the small signal equivalent circuit up to millimeterwave. Indeed, the field of new applications increases at these frequencies, and in the same time, dimensions of the active part of the device decrease to obtain better performances. This explain why, for a 0.1µm PHEMT, the order of magnitude of intrinsic and extrinsic parameters becomes similar. In these conditions, the influence and thus the determination of extrinsic parameters becomes more crucial for applications at high frequency.

Moreover, at millimeterwave, difficulties such as quality of calibration and capabilities of the network analyser to measure some very small quantities are more marked than at lower frequencies. To overcome and understand these difficulties, we purpose in this contribution a study based on the determination of the small signal equivalent circuit up to 60 GHz.

In the first part, we will discuss about the influence of the extrinsic parameters on the intrinsic one. We will deduce, by this way, the small signal equivalent circuit of our device. The second part will be devoted to measurements realised with three different test-sets. Finally, in the third part, we will speak about errors of measurement and their influences on the determination of the equivalent circuit.

As tested devices, we have used in this work lattice matched InP HEMT's (2×0.2×50 μm^2) from our laboratory [1]. The device has a peak transconductance of 700 mS/mm and a current density of 500 mA/mm when biased at a Vds=1.5 V. The current gain cut-off frequency (f_T) is 90 GHz and the maximum available gain at 60 GHz is 9.5 dB.

Influence of the extrinsic parameters on the intrinsic one

In this first part, we discuss about the influence of the parasitic elements on the intrinsic elements. The determination of the extrinsic parameters becomes more crucial for applications at high frequency due to the

reduction of the gate length and drain source spacing. For these reasons, the order of magnitude of the intrinsic and extrinsic elements becomes similar . For our study, we assume that the lumped model shown in figure 1 is valid over the whole frequency range of measurements. In this case, the intrinsic elements must be independent of the frequency. However, it is not always the case with the classical extracted parasitic elements [2]. So, many authors use algorithms of optimisation to modify the parasitic elements to obtain intrinsic elements independent of the frequency [3]. In fact, a rigorous determination of the parasitic elements avoids such optimisation softwares.

Some extrinsic elements are more important than others because they modify the linearity of the intrinsic elements instead of a shift of the curve. The most influent extrinsic parameters are the inductances Lg and Ls, the resistance Rs and the pad capacitances Cpd and Cpgd. The inductance Lg greatly modifies the slope of gm and Cgs, and also influences the slope of Gd and Rgd with less signification. As example we present figure 2 the evolution of the transconductance gm versus the frequency from 1 to 50 GHz for several values of Lg. We establish that a slight modification of Lg (around 10% of the optimum value of 49 pH) involves a modification of the behaviour of gm at high frequency. It has been noted that the source inductance Ls influences the slope of gm, Gd, Cgd, Cgs and Rgd. The resistance Rs shifts the values of gm, Gd, Cgs, Ri and Cds, and only changes the slope of Cgd. We have also noted that for high values of Rs (around 7 Ω and more), the slope of Gd and Rgd are equally modified, but, these values can't be considered as physically acceptable for our devices. The influence of Rs on the evolution of Cgd and Ri is presented figures 3 and 4 respectively. Finally, the drain pad capacitance Cpd modifies the slope of Gd, Cgs, Rgd and shifts the values of Cds and τ. The Cpgd capacitance only modifies the slope of Cgd and Rgd. The intrinsic parameters have demonstrated less sensibility to the other extrinsic elements. Indeed, an important variation (around 50%) of the measured values of Ld, Rd, Rg and Cpg doesn't modify significantly the intrinsic parameters. We present (table 1) the measured values using the classical method [2] and the values obtained by our method for the equivalent circuit at Vds=2 V and Vgs=0V. On the table 2, we resume the influence of each extrinsic parameter on the intrinsic one. This table has been obtained by increasing of 50% each extrinsic parameters and evaluating the variation produced on the intrinsic elements. We have noted "S" when we have obtained a shift of the curve, and "M" when the slope was modified. The additional letters "L" and "G" were added to balance the variation.

	Gm	Gd	Cgs	Cgd	Ri	Rgd	Cds	τ
Rs	S	S	S	M	S	S	S	
Rg					S	LM		
Rd								
Cpg	LM		LM			LM		S
Cpd		GM	GM			GM	S	LS
Ls	M	M	M	M	S	LM	S	
Lg	GM	LM	M			LM		
Ld					LS			LS
Cpgd			S	M		M		

S : Shift L : Less modify

M : Modify the slope G : Great modify

Table 2 : influence of each extrinsic parameter on the intrinsic one.

With the knowledge of the influence of each parasitic element, it is possible to obtain intrinsic parameters independent of the frequency without optimisation criteria and thus keeping a more physical approach. We present on the figure 5 and 6 respectively a comparison between the measured and calculated S parameters from 1 to 75 GHz and on the maximum stable gain (MSG) or maximum available gain (MAG). We obtain a good agreement between measured and calculated parameters and specially at the frequency where the device becomes stable. We use this criteria (unstable/stable transition frequency ; k=1,) to distinguish two equivalent circuits which give S parameters measured and calculated similar.

Measurements with different test sets

To know the influence of the bandwidth measurement on the determination of the small signal equivalent circuit, we have performed S parameter measurements with three different test sets that covered the three bandwidths [0.25 ; 40 GHz], [0.25 ; 50 GHz] and [50 ; 75 GHz]. We present on the figure 7, the evolution of gm for the three bandwidths. The extractions are performed with the same extrinsic parameters determined, as described in the first part, in the 1 to 50 GHz band. We see that in V band, intrinsic parameters become dependant of the frequency. So, we decided to modify the parasitic parameters to obtain intrinsic elements independent of the frequency. But, in these conditions, we obtain a new equivalent circuit for each bandwidth of measurement. In conclusion, we decided to don't use V-band measurements to extract the equivalent circuit. We just use them to compare S parameters (Figure 5) or quantities which are directly calculated from them like gains MSG and MAG (Figure 6).

Measurement errors

To verify the validity of our measurement, we have performed twice S parameters measurement with at each time a new calibration, and this on the three bandwidths. Moreover, the quality of calibration has been checked before measurements. So, we could determine a relative error Er defined as $Er = \frac{\left|(S_{11meas1} - S_{11meas2})\right|}{S_{11meas1}}$ where $S_{11meas1}$ means the first measurement of S_{11} and $S_{11meas2}$ the second one. For example, we present on the figure 8 and 9 respectively, the relative errors on the phase of S_{21} and on the magnitude of S_{22}. We obtain a relative error on the magnitude of S_{22} which increases at the end of the 1-40 GHz and 1-50 GHz bands. Concerning the phase of S_{21}, a very important relative error in V-Band is obtained. It is possible to consider that Er less than 5% can validate the measurements. But, if Er is around 10% it means that the measurement is not enough precise. We believe that is due do the quality of the test set and calibration. That's contribute to the difficulty of extracting an equivalent circuit in millimeterwave.

Conclusion

In this paper, we have presented a simplified approach to determine a small signal equivalent circuit up to 60 GHz. This approach is based on the influence of the extrinsic parameters on the intrinsic one. This method gives good agreement between measured and calculated S parameters without optimisation criteria. A good agreement was also obtained on the MSG and MAG, specially at the frequency transition where the device becomes unconditionally stable.

Measurements have been also realised with 3 different test sets and have shown that V band measurements can't be used to extract an equivalent circuit.

Finally, random measurement errors due to the calibration and test sets quality can't be ignored. In fact, that's at high frequency that the evolution of the intrinsic elements become significant and that's also at high frequency that measurement errors are more important. That's contribute to the difficulty of extracting an equivalent circuit in millimeterwave. This explain why we have decided to extract the equivalent circuit with S parameters measured until 50 GHz and extrapolated it until 60 GHz.

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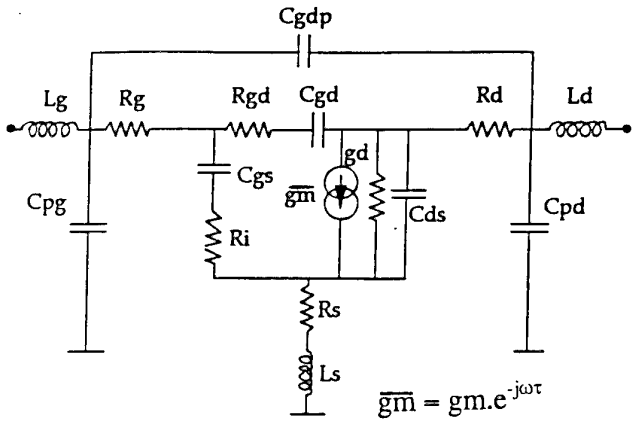

Fig.1 : Small signal equivalent circuit

	Rs (Ω)	Rg (Ω)	Rd (Ω)	Ls (pH)	Lg (pH)	Ld (pH)	Cpg (fF)	Cpd (fF)	Cpgd (fF)
Classical method	3.4	5	3.4	7	52	50	17	36	
our method	3	2	3.4	10	50	54	16	16	4

gm (mS)	Gd (mS)	Cgs (fF)	Cgd (fF)	Ri (Ω)	Rgd (Ω)	Cds (fF)	τ (ps)
84.2	3.0	145.7	5.2	3.8	433.4	19.7	0.60

Table 1 : Extrinsic and intrinsic values determined using our method at Vds=2V and Vgs=0V. The device is a 2×0.2×50 μm² HEMT.

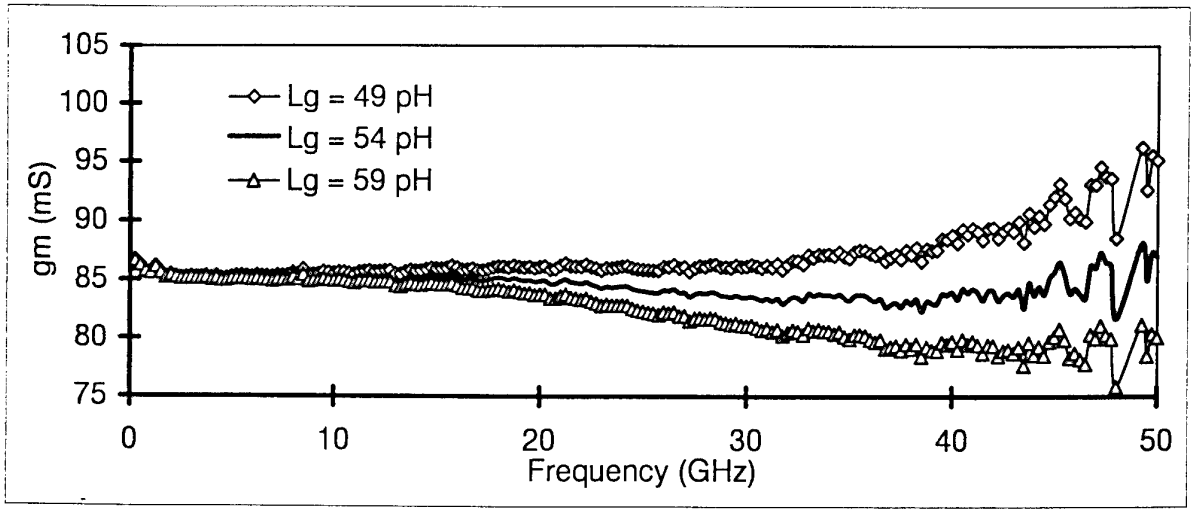

Fig.2 : Evolution of gm for different values of Lg (W=100 μm)

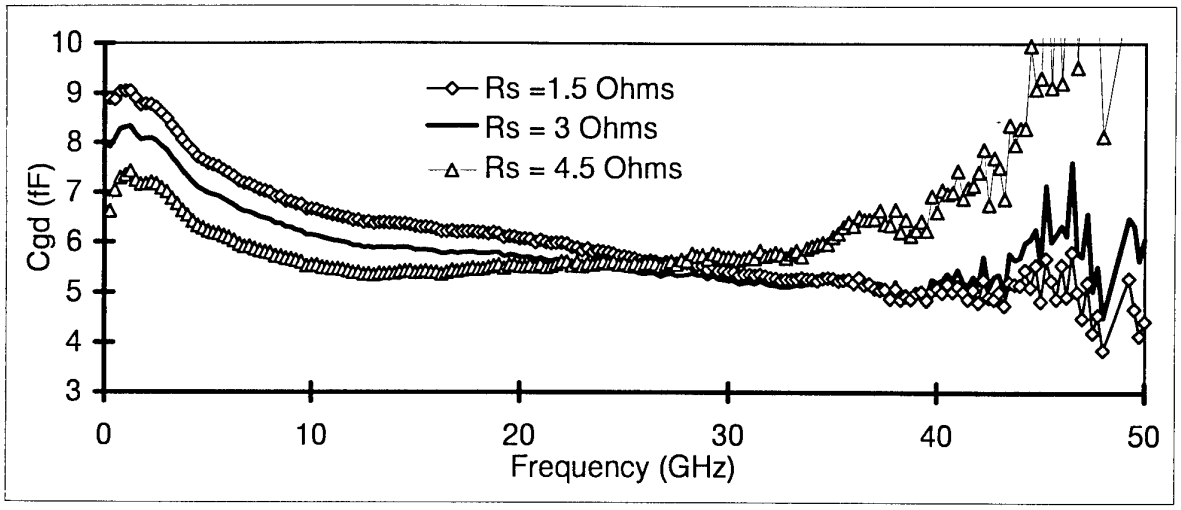

Fig.3 : Evolution of Cgd for different values of Rs (W=100 µm)

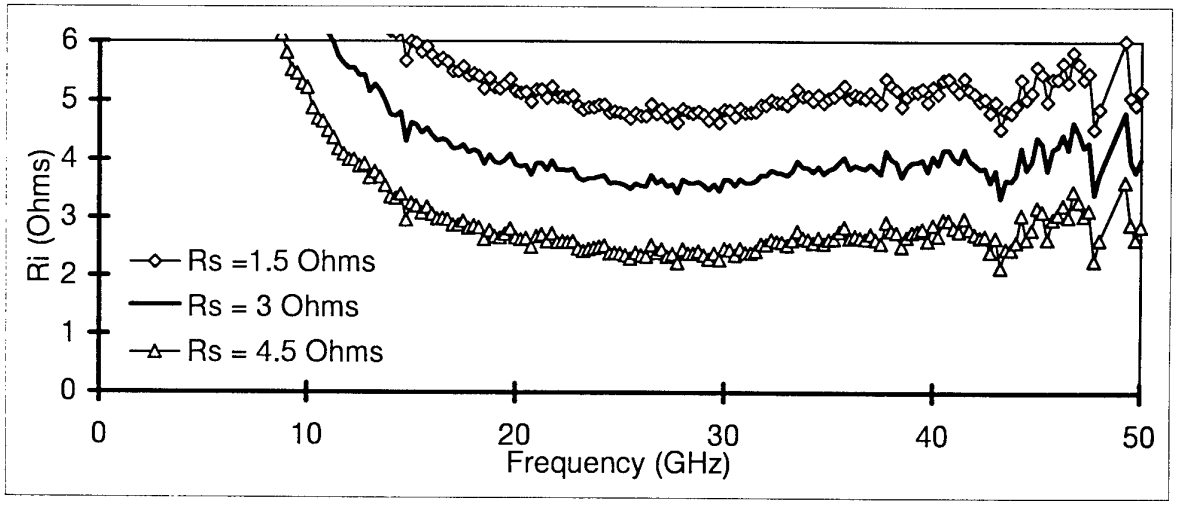

Fig.4 : Evolution of Ri for different values of Rs (W=100 µm)

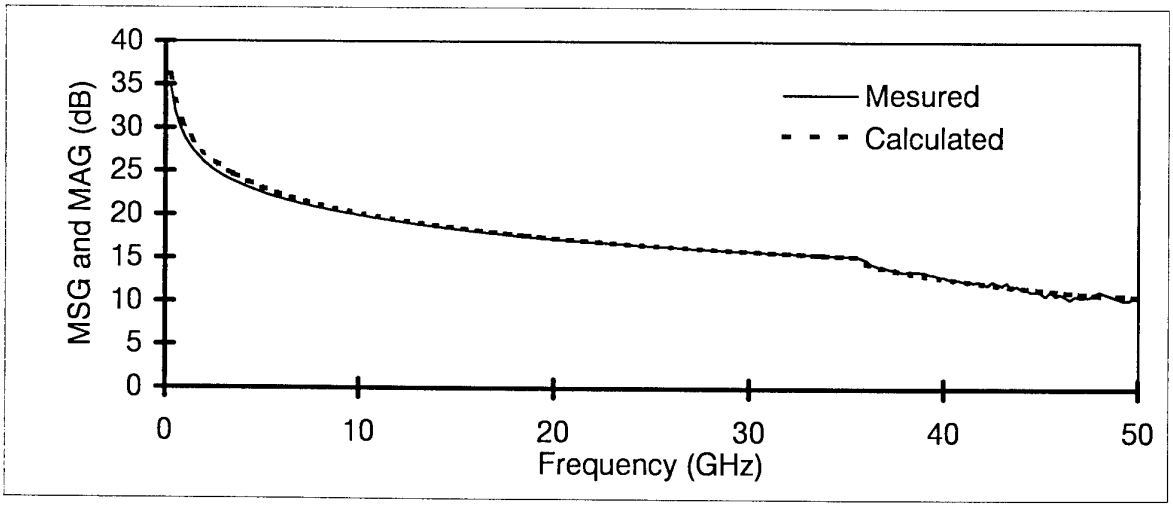

Fig.6 : Comparison between mesured and calculated gains up to 50 GHz

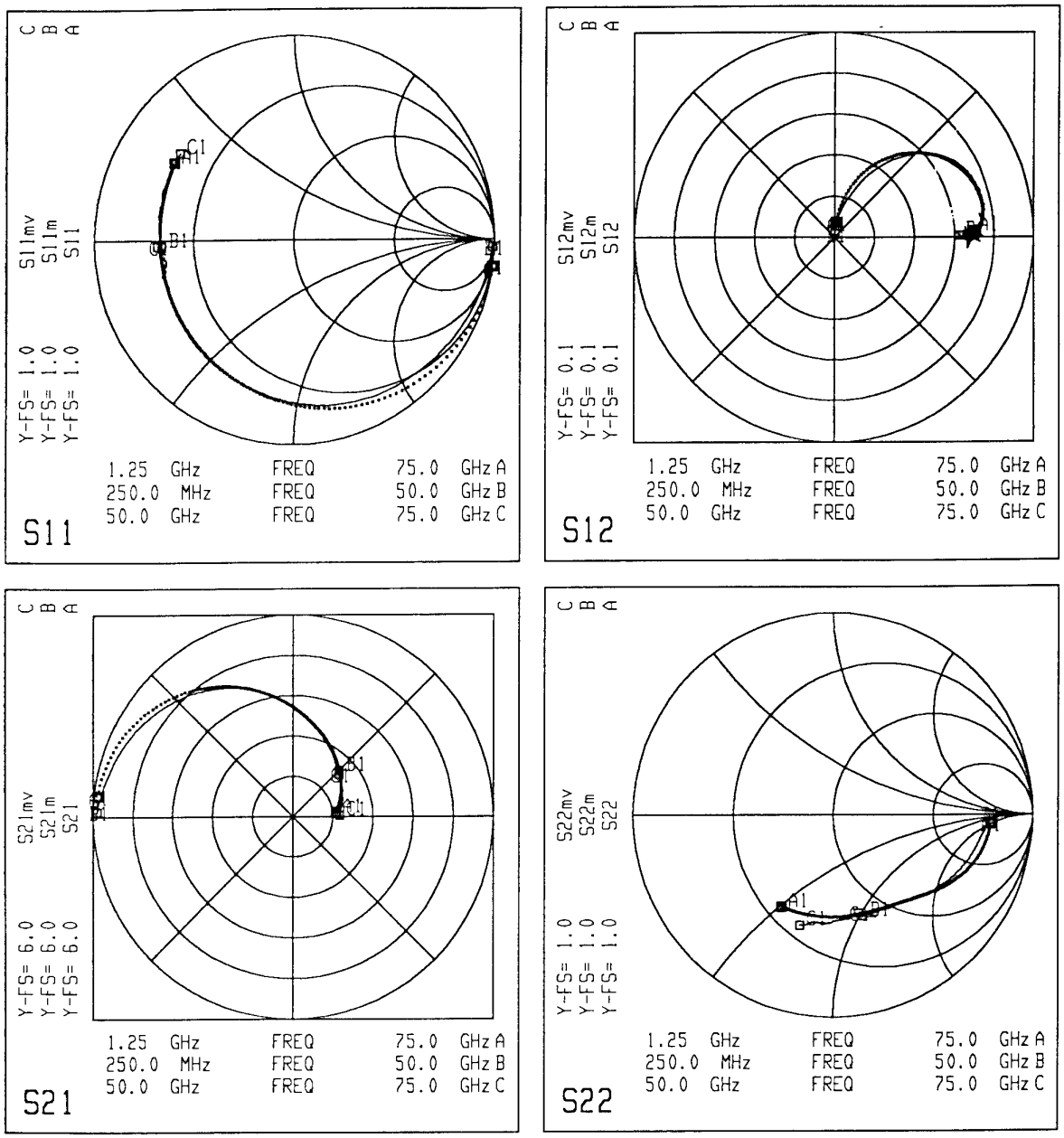

Fig.5 : Comparison between measured (connected) and calculated (disconnected) S parameters from 1 to 50 GHz

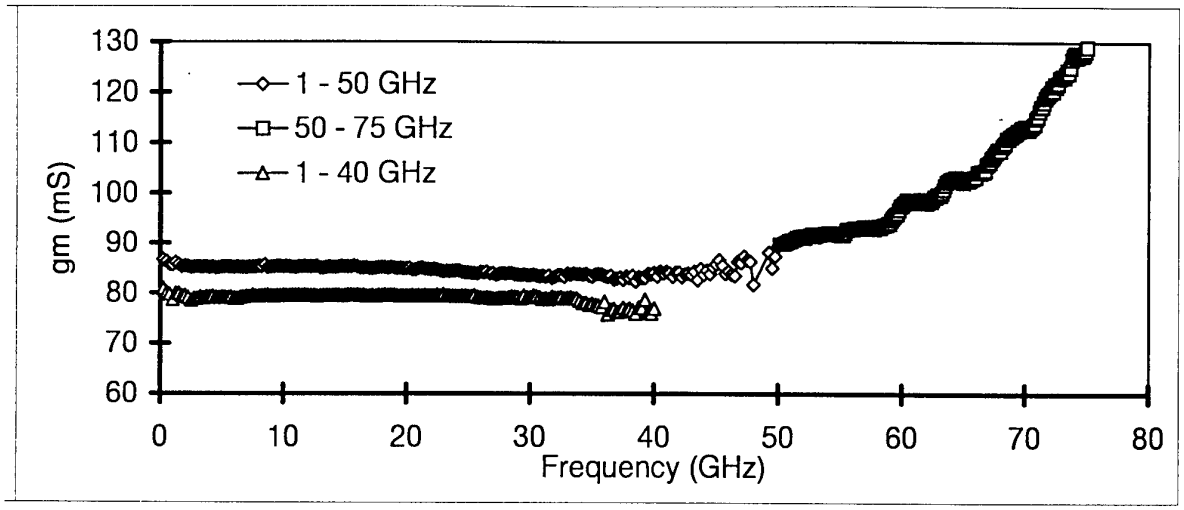

Fig.7 : Evolution of gm determined in the 3 bandwidths

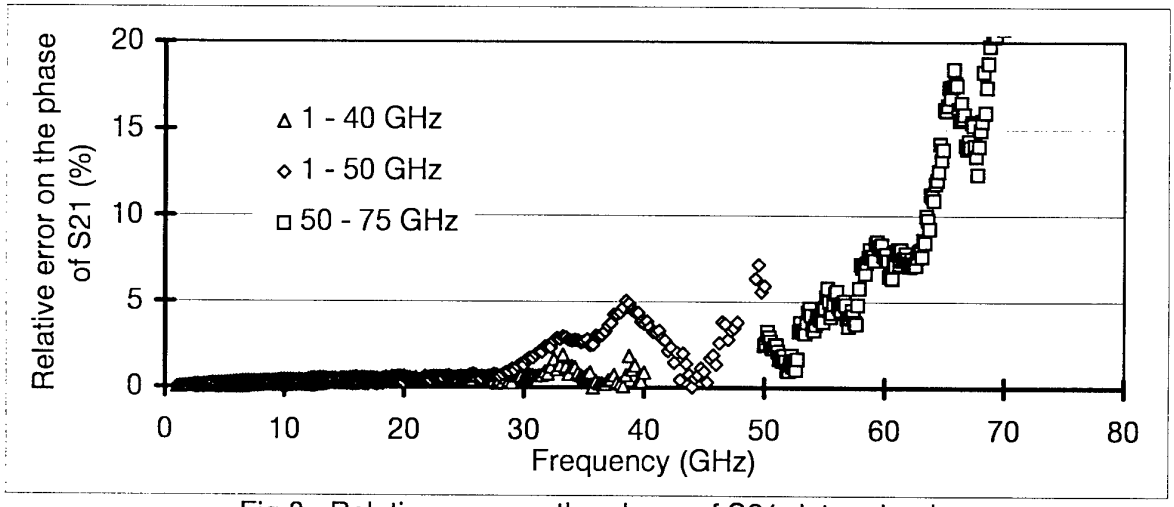

Fig.8 : Relative error on the phase of S21 determined in the 3 bandwidths

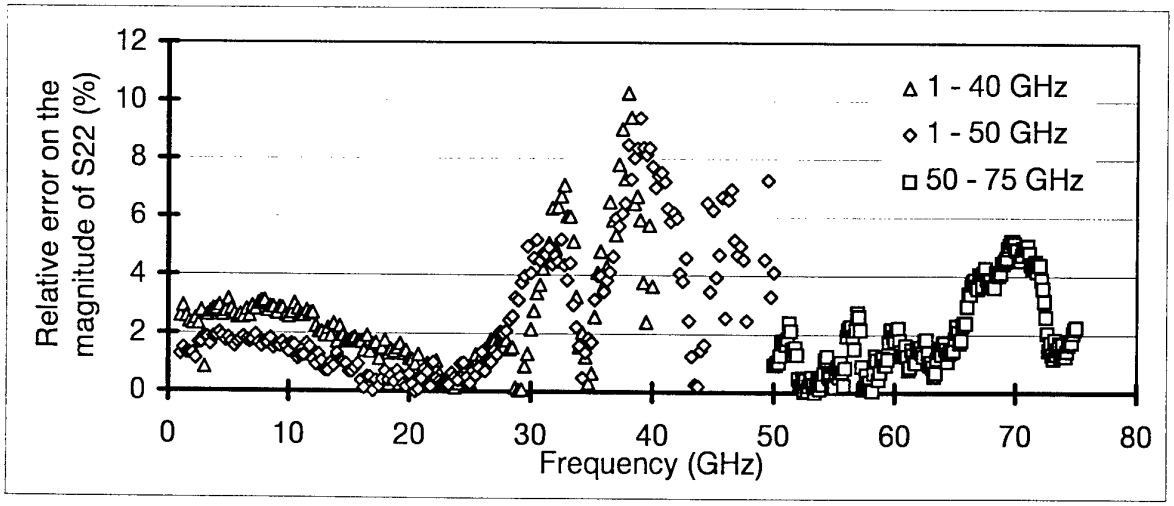

Fig.9 : Relative error on the magnitude of S22 determined in the 3 bandwidths

A NEW OPTIMIZATION STRATEGY BASED ON THE THEORY OF EVOLUTION FOR THE RF-MODELING OF HFET

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ABSTRACT – A new optimization strategy, the *Strategy of Evolution*, which is based on the *Theory of Evolution*, is presented. This way of optimization results in finding the global optimum in case of high-dimensional, complex and not analytically solvable problems. The capability of the *Strategy of Evolution* is demonstrated by the comparison of measured and modeled RF-parameters of InP-**H**etero-structure **F**ield-**E**ffect **T**ransistors (HFET).

I. INTRODUCTION

For the development, design and simulation of microwave circuits it is essential to provide exact yet simple models for the description of the single device behaviour. Today, there are a lot of approaches for the modeling of the high frequency behaviour of Heterostructure Field-Effect Transistors (HFET) showing an excellent agreement between measured and modeled scattering or high frequency noise parameters. But only some of these models (e.g. [1-6]) use physically relevant small-signal equivalent elements. Including additional physical phenomena, the number of parameters as small-signal equivalent elements and noise temperatures or noise currents, resp., increases. Usually it is not possible to determine the elements analytically. Deterministic and/or stochastic methods as for example the *Gradient-* or *the Monte Carlo method* have to be used for optimization. The *Gradient method* strongly depends on the starting values of the optimization and may lead only to a local but not the global optimum. Stochastic strategies are very time consuming and do not result in the global optimum in any case. A good compromise is the use of the *Simulated Evolution* in form of *Genetic Algorithms* [7-9] or the *Strategy of Evolution* (SE) [10-13] (see fig. 1) which is discussed in more detail in this paper.

II. THE USED HFET-MODEL

Fig. 2 shows the used small-signal- and RF-noise-equivalent circuit of HFET [1]. This model includes impact ionization in the channel as well as gate-leakage current for both small-signal- and RF-noise-behaviour.

Additional small-signal elements are used to model both phenomena in case of the RF-behaviour of the HFET. The parallel resistances between gate-source (R_{pgs}) and gate-drain (R_{pgd}), resp., consider a gate-leakage current. Impact ionization can be described with the help of an additional voltage controlled (v_{dg}) current source ($g_{m,im}$) and a RC-combination (R_{im}, C_{im}) parallel to the output resistance. In total there are 21 elements for the description of the small-signal behaviour (fig. 2).

The RF-noise of the intrinsic HFET is modeled with four noise parameters: three equivalent noise temperatures (T_g, T_p and T_d) and the equivalent impact ionization noise current i_{im} (fig. 2). The noise temperatures of the extrinsic resistances are set to the ambient temperature. After finding the small-signal equivalent elements, the four noise parameters can be optimized.

III. The *Strategy of Evolution*

The SE is based on the *Theory of Evolution* and considers the three most important elements of this theory: the *mutation of the genotype*, the *recombination of the genetic information* and the *selection on the basis of the individuals fitness*. The advantage of SE is the combination of deterministic (*selection* and *recombination*) and stochastic (*mutation*) search procedures. The individuals of one population are represented by n-dimensional real vectors with n, the number of parameters which have to be optimized. There are a lot of different methods for the *Strategy of Evolution*. We have used the $(\mu/\rho+\lambda)$-strategy. ρ individuals are *selected* out of μ parent-individuals at the current generation for *recombination*. This *selection* happens by chance with the same probability for every parent-individual. Now the ρ selected new parents *recombine* and generate λ descendant-individuals. The descendants *mutate* by chance with standard probability. Next all individuals, the μ old parents and the λ descendants are assessed and the μ best adjusted individuals are accepted as the new parent-individuals of the following generation. Fig. 3 shows an example for the described strategy.

The quality or fitness of the best fitted individum never decreases because good fitted parent-individuals survive and become parent-individuals of the next generation. In contrast, using other strategies, the fitness of the best fitted individual can decrease. For example in case of the $(\mu/\rho,\lambda)$-strategy only the λ new descendant-individuals are assessed and μ of them, the best adjusted, are choosen for the new parents of the following generation. The fitness of the best individuum in dependence on generation is shown in fig. 4 for both strategies.

The algorithm described above continues until a limit is reached. For example this criterion is a maximum generation number or a defined error value between modeled and measured parameters.

Different ways of *recombination*, *selection* and *mutation* are discussed for the *Strategy of Evolution* [14]. Special emphasis lies on the *mutation* of the descendants. Because a local optimum will be left due to the *mutation* and the SE only will be finished after finding the global optimum. A second advantage is the high efficiency of the new procedures with respect to high-dimensional and very complex optimization problems. As a result these procedure is extremely fast and absolutely independent of the starting-values.

IV. Results

Fig. 5 and fig. 6 demonstrate the validity and performance of the *Strategy of Evolution* for the extraction of the small-signal equivalent elements as well as the noise parameters of the consistent small-signal and noise-equivalent circuit of InP-HFET. Due to the high number of high frequency parameters and the complexity of the noise equations, no analytical solution of the problem can be found. An optimization with SE is highly appropriate and the excellent agreement between measured and modeled values is clearly demonstrated. Fig. 5 shows the measured and modeled scattering-parameters in a frequency range from 45 MHz up to 40 GHz. Tab. 1 lists the optimized values of the equivalent elements, the bias condition and the geometry of the examined HFET.

The noise measurements take place at the same bias condition. The results show the same excellent agreement between measured and modelled values (fig. 6). The optimized values of the noise temperatures and the noise current are given in table 2.

Bias dependent investigations of the model demonstrate the capability of SE for the extraction of physically relevant values for all model parameters.

V. Conclusion

The *Strategy of Evolution* is a valuable tool for numerous applications which require the solution of more dimensional problems where analytical solving is not appropriate. This is demonstrated for the consistent small-signal and noise-equivalent circuit of InP-HFET. Further SE can be used for all complex and high-dimensional optimization problems, is absolutely independent of the starting values and leads to good results.

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FIGURES

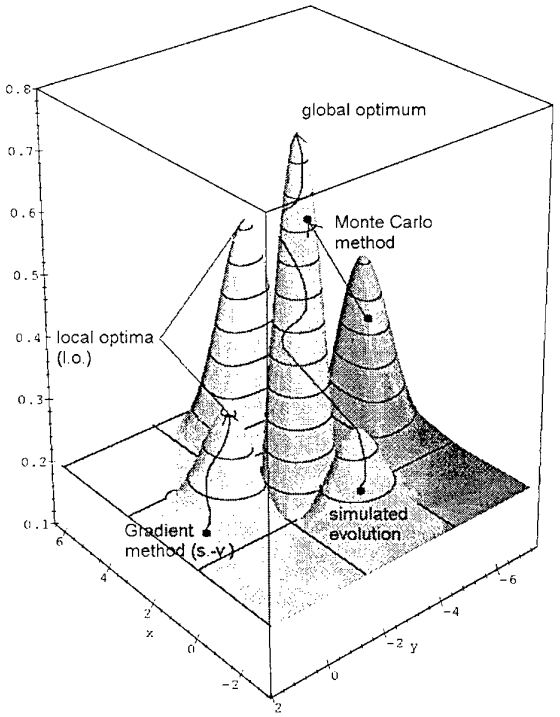

Fig. 1: Comparison of different optimization methods.

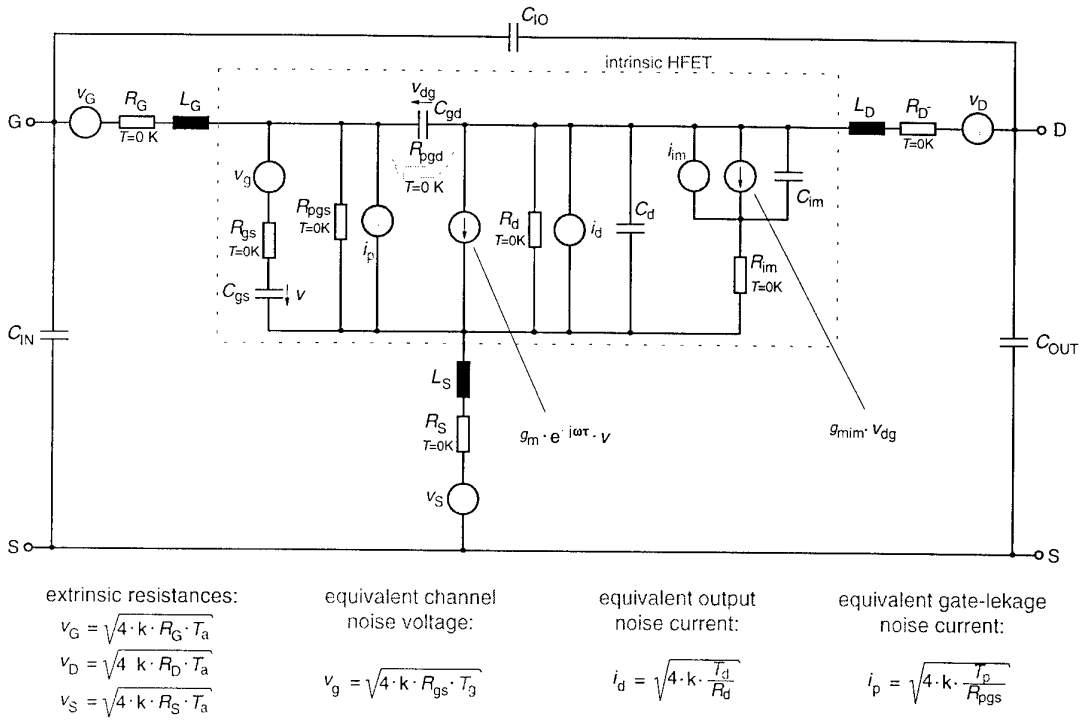

Fig. 2: Small-signal- and RF-noise-equivalent circuit of HFET.

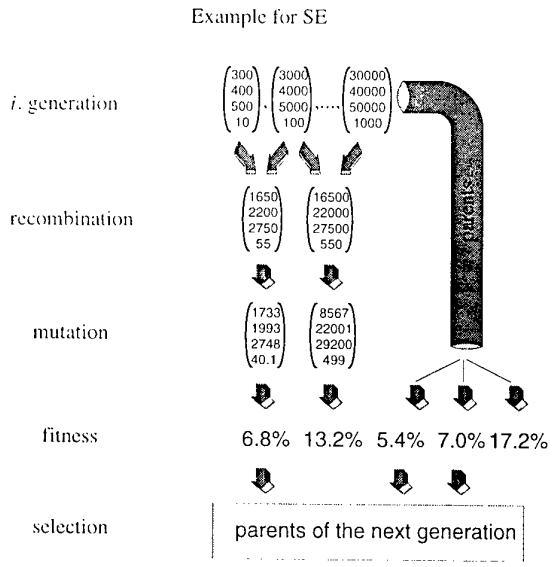

Fig. 3: Example for the $(\mu/\rho+\lambda)$-strategy.

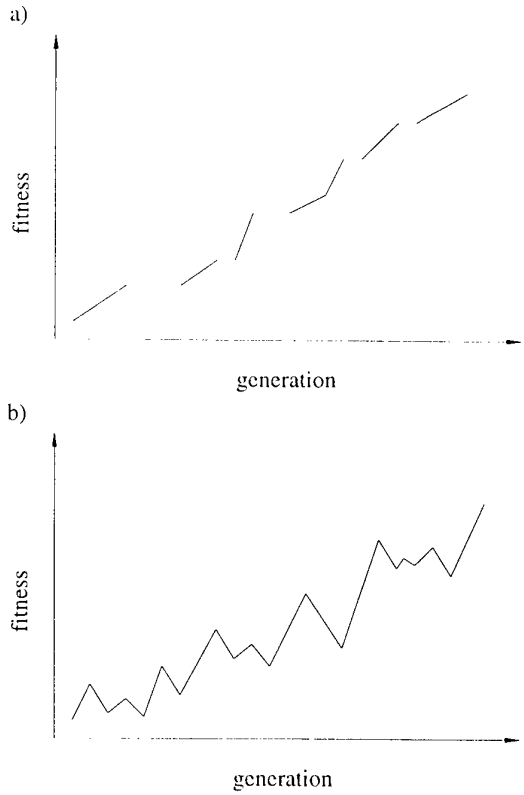

Fig. 4: Fitness in dependence on the generation for the a) $(\mu/\rho+\lambda)$-strategy and b) $(\mu/\rho,\lambda)$-strategy.

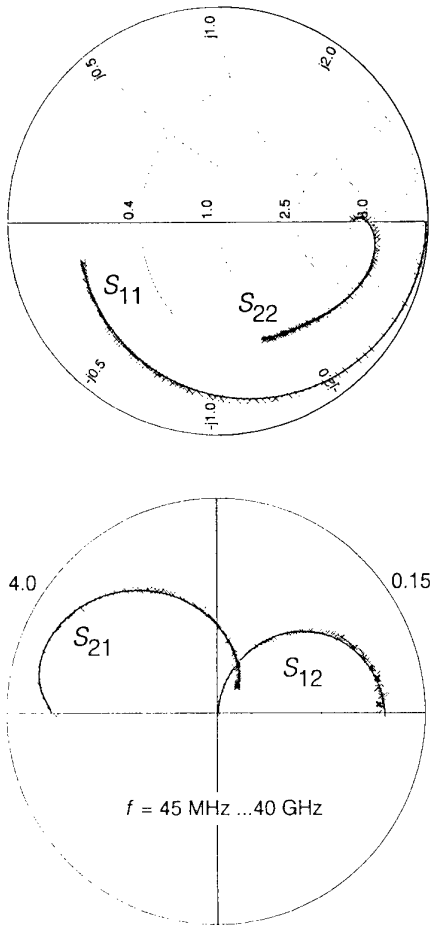

Fig. 5: Measured (×) and modeled (-) scattering parameters of an HFET in dependence on frequency *f*.

bias condition:

V_{DS} = 1.5 V	V_{GS} = 0.0 V
I_{DS} = 31.8 mA	I_G = -18 µA

geometry:

L_G = 0.7 µm
W_G = 80 µm

small-signal equivalent elements:

C_{IN} = 14.2 fF	C_{OUT} = 28.2 fF	C_{IO} = 4 fF
R_G = 3 Ω	R_S = 8 Ω	R_D = 10.0 Ω
L_G = 63.1 pH	L_S = 3.8 pH	L_D = 152 pH
R_{gs} = 2.8 Ω	R_{pgs} = 12000 Ω	C_{gs} = 210.5 fF
R_{ds} = 420 Ω	R_{pgd} = 70686 Ω	C_{ds} = 8.19 fF
C_{gd} = 9.5 fF	g_m = 69 mS	τ = 0.22 ps
R_{im} = 38000 Ω	$g_{m,im}$ = 4.26 mS	C_{im} = 1.42 fF

Tab. 1: Bias condition, geometry and optimized small-signal equivalent elements for the examined HFET.

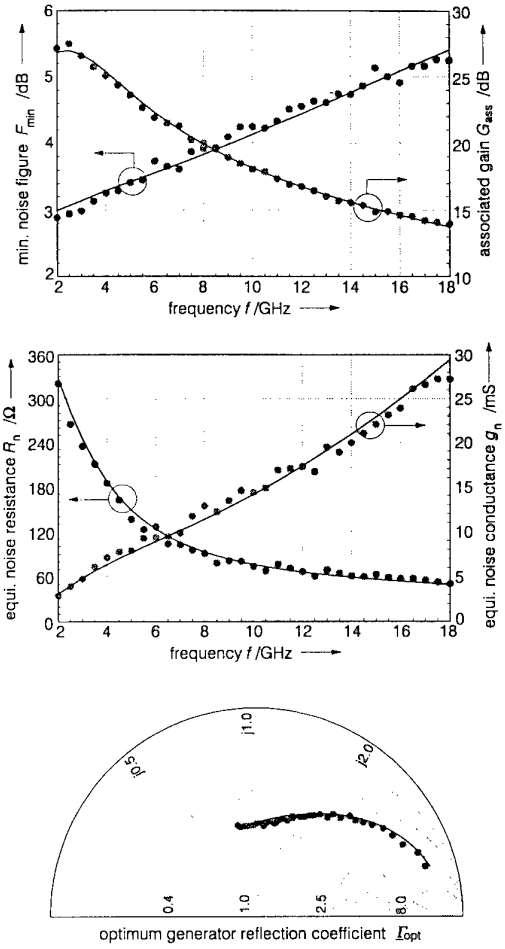

Fig. 6: Measured (•) and modeled (-) equivalent noise parameters of an InP-HFET: F_{min}, G_{ass}, R_n, g_n and Γ_{opt} in dependence on frequency *f*.

noise parameter:

ambient temperature:
T_a = 300 K

equi. channel noise temperature:
T_g = 4014.9 K

equi. output noise temperature:
T_d = 18007.84 K

equi. gate-leakage noise temperature:
T_p = 918.65 K

equi. impact ionization noise current:
i_{im} = 166 pA

Tab. 2: Optimized noise parameters for the examined HFET.

Extraction of FET and HEMT parasitic parameters

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Abstract

This review paper examines the theoretical basis for the parasitic parameters in the standard equivalent circuit models, and summarizes practical methods to extract the source, gate, and drain resistances, inductances, and pad capacitances for a wide variety of FET and HEMT technologies. Results for different test layouts are discussed, correlations between source and drain resistances for many FETs are shown, and we show how to extract the contact resistance to the 2d gas in HEMTs.

1.Introduction

The standard equivalent circuit model for a FET or HEMT consists of at least 16 equivalent circuit parameters (ECPs). As shown in several papers, if one can ascertain at least 9 parasitic parameters (R_s, R_d, R_g, L_s, L_d, L_g, C_{pg}, C_{pd}, and C_{pf} in Fig.1c.), at any gate and drain bias, the measured S -parameters can be converted to intrinsic Y parameters from which one can solve for at least seven intrinsic "hot-FET" ECPs, g_m, C_{gs}, C_{gd}, C_{ds}, τ, R_i, R_{ds} and sometimes R_{gs}[1,2].

So why do we use such a complicated model? A simpler equivalent circuit model would consist of just the extrinsic Y matrix (Fig.1.d), where we assume all of the parasitic resistances, inductances, and capacitances are zero. The direct extraction process works the same way, but the resulting ECPs are extrinsic, e.g. g_m would be equal to approximately $g_{m,int}/(1+g_{m,int}R_s)$, where $g_{m,int}$ is obtained in the 16-parameter EC model. It turns out that the extrinsic hot FET parameters are also nearly independent of frequency in normal biasing and that the S-parameter fits are often nearly as good.

There are four reasons to make this extraction: (1) the resulting hot-FET parameters are scaleable with the FET width, e.g. g_m and the capacitances scale linearly with width and the resistances scale inversely with the width, allowing the ECPs to be used for more cases than the FET that was measured. (2) The inductances and parasitic capacitances are generally not part of the FET embedded in a circuit which would be connected to the outside world or other FETs using transmission lines which the circuit simulator attempts to construct and is different from the layout used in the test measurement. (3) The intrinsic f_t values are higher when the parasitic capacitances are removed. (4) Finally the most important reason is that the large-signal models are often formulated in terms of the intrinsic gate and drain voltages. For example the gate capacitances vary as $1/\sqrt{1-V_g/V_{bi}}$, which becomes large when V_g approaches the Schottky barrier height V_{bi}~0. 8V for GaAs. With increasing drain voltage, the intrinsic gate voltages vary as V_g-$I_{ds}R_s$, so that although an applied gate potential of 0.8V at V_{ds}=0 gives a large gate capacitance, at V_{ds}~2V, the capacitance is much smaller.

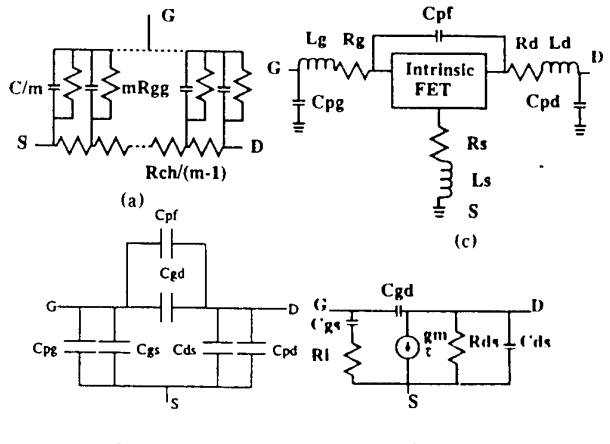


Fig.1. (a) EC for a distributed gate, (b) pinched FET, (c)Standard EC showing parasitic elements, (d) Intrinsic FET Y parameters or Extrinsic EC if all parasitic ECPs are zero

Given this commitment to the 16-parameter EC model, this paper summarizes my experience with extracting FET and HEMT parasitic parameters for a wide variety technologies over the past six years. Gateway Modeling supports an S-parameter Equivalent Circuit Analyzer, SPECIAL, and has made use of this program to analyze FET and HEMT equivalent circuits for a wide variety of technologies, obtained through the US MIMIC program as well as through close relationships with individual foundries such as Gigabit Logic, TriQuint Semiconductor, Cray Computer, Motorola, Texas Instruments, Wright Laboratory, and many others. Starting from a general expression for the cold FET Z parameters, one can use several different extraction approaches, depending on the applied biases, and in our experience, different approaches are applicable to different technologies.

This paper is organized as follows. Section 2 examines the theoretical basis for the standard EC model. Section 3 summarizes different approaches to extracting the parasitic resistances and inductances for different technologies and Section 4 summarizes approaches to extracting the parasitic capacitances. Finally Section 5 examines results, and Section 6 has the conclusions.

2.The basis of the standard equivalent circuit model

At zero drain bias, the FET Z parameters are given by

$$\begin{aligned} Z_{11} &= R_g + R_s + \alpha_g R_{ch} + R_{gs} / (1 + j\omega R_{gs} C_{gs}) \\ &\quad + j\omega(L_s + L_g) \\ Z_{12} &= Z_{21} = R_s + \alpha R_{ch} + j\omega L_s \qquad (1) \\ Z_{22} &= R_s + R_d + 2\alpha R_{ch} + j\omega(L_s + L_d) \end{aligned}$$

where R_{ch} is the channel resistance (R_{ds} at zero drain bias), and α_g and α depend on the gate current and R_{ch}. This section derives this expression.

2.1.Transverse effects

The FET or HEMT is a three dimensional device. While the intrinsic Y parameters scale linearly with the FET width and the source and drain resistances scale inversely, R_g, L_d, and L_g vary as the width W divided by $3n^2$, n being the number of fingers. Also extrinsic contributions to these parameters are often present, coming from regions away from the active FET fingers (connections to the test pads). The intrinsic gate

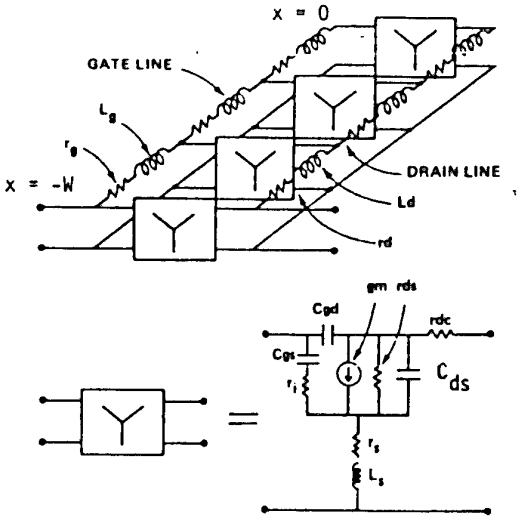


Fig.2. Transverse distributed EC [3]

resistance and gate and drain inductances can be derived from a distributed FET model like that shown in Fig.2. Here we break the single-finger FET up into several regions along the gate width which are connected by resistors and inductances. The drain resistance is generally negligible because the FET drain contacts are generally very wide and thick, but the gate resistance and inductances are important. Full expressions for the Y and Z parameters are derived by Larue et.al.[3]. One can show that if $(Rg+j\omega Lg)\omega(Cgs+Cgd)$ and $j\omega Ldj\omega(Cds+Cgd)$ are small (at $V_{ds}=0$ where $g_m=0$), one obtains $R_g=\rho_g W/3$, $L_g=\rho_{lg}W/3$, and $L_d=\rho_{ld}W/3$, where ρ_g, ρ_{lg}, and ρ_{ld} are the gate resistance and inductances per unit length. When one deploys more than one finger, these parameters scale as n^{-2}, where one factor of n comes from having n fingers in parallel and the other because each finger is W/n in length. This approximation is less valid when the gate is highly resistive, such as may occur when one deploys WSix gates without gold shunts in self-aligned FET technologies. Reference [4] shows that this approximation works well up to 110GHz.

2.2. Extrinsic effects

The FET is embedded in a test layout when S parameters are measured. I generally measure S parameters on wafer using coplanar layouts. This test setup can be viewed as a transmission line from the gate pad to active fingers and one from the fingers to the drain pad, which adds an extrinsic pad capacitance and inductance to port 1 and 2. On the gate side, this

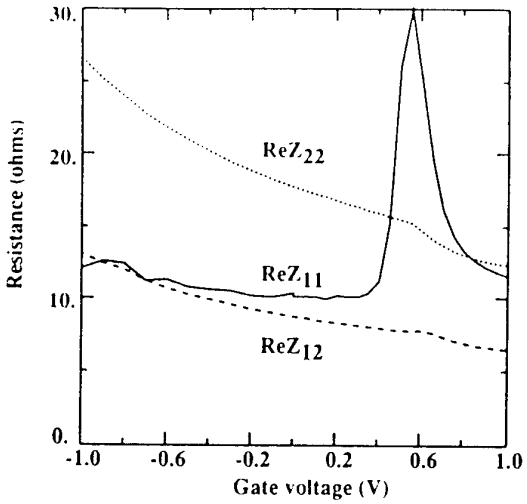


Fig.3. ReZ parameters for a 1.2μm gate length MESFET

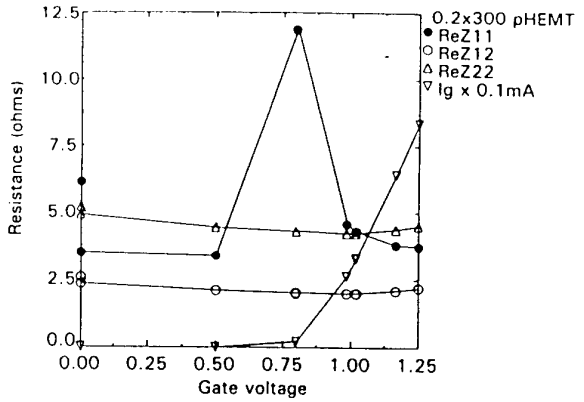


Fig.4. ReZ parameters and I_g for a 0.2x300μm² pHEMT

gives contributions to L_g and C_{pg} to the EC. On the drain side it gives L_d and C_{pd}.

When the S-parameter measurement system is calibrated, we define the source inductance to be zero in the through measurement, so the measured source inductance is in essence a measure of the difference between the test layout inductance and the through layout. The closer the test layout looks like a through, the smaller will be the source inductance. I show in Sect.5, asymmetric test layouts which have very large source inductances. Most coplanar layouts give inductances of the order of -5 to 5pH. In my view negative source inductances are not an issue, since they are simply a function of the difference between the cal layout and the test layout.

2.3 Source and drain resistances

In the Fukui approximation[5], the source resistance for recessed-etched MESFETs with no selective n^+ implants is given by

$$R_s = (r_c + R_{n+}L_{n+} + R_{n-}L_{n-})/W \qquad (2)$$

where r_c is the contact resistance (assuming the contacts are wider than the transfer length[5]), R_{n+} and R_{n-} are the sheet resistances of the unetched and etched regions of the FET and L_{n+} and L_{n-} are the lengths of each of these regions. Generally the distance between the edge of the gate and the bottom of the trench is less than 0.2μm, so the bottom of the trench is fully depleted and therefore L_{n-} is ignored.

The source and drain resistances are slightly bias dependent. At zero drain bias, reducing the gate bias causes the depletion region to bulge laterally which reduces L_{n+} and therefore the source and drain resistances. Increasing the drain bias causes L_{n+} on the drain side to decrease which reduces R_n.
The effect is not large because R_{n+} in the unetched regions of the FET is small so the depletion region extension is kept small in relationship to the total gate-source or drain-source distance (~1μm). The main reason for ignoring the bias dependence is that the large signal models require fixed source and drain resistances, and since one of the main reasons for extracting these parameters is to accommodate the large-signal models, we must make R_s and R_d constant.

2.4.The distributed gate

Along the gate length we can break the gate up into several sections, as shown in Fig.1a., where we have a parallel gate-to-source resistance and capacitance connected by several components of the channel resistance[6,7]. When one forward biases the gate with very high gate current the capacitance is effectively shunted, and the gate-source resistance varies as NkT/qI_g, N being the ideality factor, kT/q the thermal voltage, and I_g the gate current. If the resistance of each of these sections becomes smaller than the channel resistance, most of the gate to source current will flow through the end resistors, avoiding the channel resistance. Also source-to-drain current will flow up the

outside resistors and be shunted by the gate metal from the channel resistance. The α factors in Eq.(1) depend of the ratio of the channel resistance to the gate-source resistance. If this ratio is large, the alpha factors vanish, though an impractical gate current is required for this to happen. At small gate currents, the α_g=1/3 and α=1/2.

2.5. Real Z parameters for FETs and HEMTs

Figures 3 and 4 show how ReZ_{11}, ReZ_{12}, and ReZ_{22} vary with gate bias[6]. For the 1.2μm-gate length FET, at V_g<0.8V, the resistances decrease with increasing bias because R_{ch} is decreasing. In this case $\omega R_{gs}C_{gs}$ is very large so the R_{gs} term shows up in the imaginary part of the Z parameters. At V_g=0.8V, R_{gs} decreases very rapidly because I_g increases, and in this region Z_{11} is a complicated function of frequency. The average over frequency is shown in Figs. 3 and 4, which is not meaningful in this region. For V_g>0.8V, $\omega R_{gs}C_{gs}$<<1, so the decrease in ReZ_{11} is due to the fall off in R_{gs} with increasing I_g. The fall offs in Z_{12} and Z_{22} are due to the alpha factors. In MESFETs at very high biases the α factors do not continue to decrease, but increase. This is partly due to thermal effects, for the large gate currents cause the temperature to increase.

In HEMTs, the α factor effects on the Z parameters are not observed (Fig.4 being typical of a wide variety of HEMTs we have examined). I believe this is due to the high fields beneath the gate which comes from the band offsets, but this has not been proven.

2.6. Parasitic capacitances

As discussed above, the parasitic gate and drain capacitances C_{pg} and C_{pd} come from the inter-connections between the test pads and the active fingers and in the pads themselves. As more fingers are added, these two parasitic capacitances increase, because more interconnect metal is added.

C_{pf} is an additional pad capacitance in parallel with C_{gd}. This capacitance probably comes from the ends of the fingers in symmetric layouts where the gate and drain lines come close together, or near the T gate intersection in T layouts.

3. Extraction of parasitic resistances and inductances

There are six major methods to extract the parasitic resistances and inductances, with minor variations:

1. Pinched FET measurements[8]: Bias at V_g<V_{th} (the pinchoff voltage at zero drain bias) and V_{ds}=0. In this case the RF current mainly goes through the capacitances and inductances and the channel resistance drops out of these equations. Also the R_{gs} term appears in the imaginary parts of the Z parameters, so one has ReZ_{11}=R_g+R_s, ReZ_{12}=R_s, and ReZ_{22}=R_d+R_s.One does not get the inductances; additional measurements are needed for those.
2. Zero bias. Bias at V_g~0 to 0.5V, V_{ds}=0. The α factors in this case are 1/3 and 1/2 and the R_{gs} term is not present in ReZ_{11}, so in the real parts one has three equations in four unknowns. The minor variations involve what one does to set the fourth unknown: set R_{ch}, R_s, R_d, R_g, or some ratio like R_{ch}/ReZ_{12}. R_d is not really independent of R_s so setting R_s and R_d is the same. R_g can be set from end-to-end gate resistance measurements the process engineers regularly do and a knowledge of the width and number of fingers, but errors magnify. Setting R_{ch} equal to zero is not unreasonable, especially for small gate-length HEMTs, but for larger gate lengths, negative R_i values sometimes result. At these biases ImZ_{22}/ω and ImZ_{12}/ω values are generally independent of frequency, and give L_s and L_d, but ImZ_{11} has a $1/\omega C_{gs}$ contribution. One can least squares fit ImZ_{11} to ωL-$1/\omega C$, and thereby extract L_g=L-L_s.
3. Low Gate currents. Bias at V_g~V_{bi}, V_{ds}=0. At this bias, one can fit Z_{11} to $R+j\omega L+R_{gs}/(1+j\omega R_{gs}C_{gs})$ and thereby extract L_g=L-L_s, R_{gs}, and R=R_g+R_{ch}/3+R_s, and follow the same procedure as method 2. While this region should be avoided if possible, in some HEMTs we have found that it is not possible to force sufficient gate current to achieve the forward bias condition where L_g is cleanly separated from C_{gs}.
4. Forward bias. V_g>V_{bi}, V_{ds}=0. At these biases the R_{gs} term is purely real and adds to ReZ_{11} and the three inductances can be uniquely separated from the ImZ parameters. However, one then has 3 equations in 5 unknowns for the real parts. R_{gs} can be obtained separately by deriving the gate ideality factor from the gate currents at lower bias and using the measured gate current, but even when this is done, one still has the problem of method 2 of getting 4 unknowns from 3 equations.

5. Alpha method[6]. Use 2 to 3 gate biases at $V_g > V_{bi}$ and $V_{ds}=0$. Measure ReZ_{11}, ReZ_{12}, and ReZ_{22} versus gate current, and solve for the 5 parameters given theoretical α functions of R_{ch}/R_{gs} making use of the measured gate currents. In this method, since one also varies ReZ_{11} versus I_g, one can extract the gate current ideality factor at the same time, without needing a separate measurement. Table I shows how this method works. Here we measured the S parameters at V_g=0.8, 1.0, and 1.2V (very standard biases for MESFETs), and observe that they all decrease with increasing gate voltage or gate current. (If they do not, the method cannot be used.) The program searches for a value of the ideality factor N and the channel resistance which makes the average slope of R_s and R_g equal to zero.
6. Hot FET biases. It is possible to use an optimizer to extract the parasitic resistances and inductances from a single S-parameter measurement, which is a technique used in the past. The S parameters are generally not sensitive to the drain resistances and inductances so the physical meaning of the parameters is doubtful. Also if multiple biases are optimized, one is likely to end up with bias dependent, physically unmeaningful parasitic resistances and inductances, which are not useful in the large signal models.
7. R_s and R_d can also be obtained from DC end-resistance measurements[9], which also have uncertainties due to contributions from R_{ch}. While such measurements are nearly equivalent to S-parameter measurements, they generally cannot be made using the same probes because of the necessity of floating the source, therefore it is less convenient to make the DC measurements and correlate them back to the RF results. The DC measurements do not address the problem of extracting the inductances.

Our experience with these methods is as follows:

1. We have never found a FET or HEMT where the pinched measurements work, though in theory they should. When we make cold FET extractions, we plot the resistances versus frequency and average over frequency. The extracted pinched FET resistances depend strongly on frequency and the standard deviations in the averages often exceed 100%. Even if the resistance versus frequency variations are small, the extracted resistances are very sensitive to the magnitudes of the pad capacitances, so careful determinations of the pad capacitances must also be made.
2. The alpha method works about 80% of the time for MESFETs and never works for HEMTs. The alpha method is adequate when insufficient information is known about the MESFET to compute R_{ch} or R_g in method 2.
3. In production, if one wants to track parasitic parameters from wafer to wafer or FET to FET, the alpha method does give sufficiently consistent values of R_{ch} and is time consuming because it requires more measurements. We therefore recommend method 2 where R_{ch} is fixed to a value which could be derived from a single α measurement and which stays fixed as long as the FET width and length are the same. From FET to FET there may be variations in R_{ch}, due to etch depth variations or gate lithography, but these variations will be absorbed into variations in R_s, R_d, and the intrinsic parameters. Remember that since we can fit the S-parameters equally well with all parameters equal to zero, assuming that the process variations in R_{ch} are zero will not affect the accuracy of the S-parameter fits.
4. For short-gate-length HEMTs, using method 2 and assuming R_{ch}=0 is often a good approximation. pHEMTs have very high mobilities in the channel, high charge, and small gate lengths, so it is possible to get R_{ch} values as low as 0.05ohm-mm, compared to typical source resistances of the order of 0.5ohm-mm. One must still make a forward bias measurement to get the gate inductances. In some HEMTs, we could not force enough gate current, therefore had to use method 3 to extract the gate inductance.
5. Finally there is the point that forward bias measurements sometimes damage the FET or HEMT. FET gate biases of the order of 1.3V give 100mA currents, which corresponds to an immense current density in $0.2 \times 0.2 \mu m^2$ rectangular gates, but not in T gates or FETs with large lengths. The low-noise technologies strive to achieve low gate resistances by making the gate areas large, which reduces the transverse gate current densities. Nevertheless, we have experienced in two technologies cases where we did not get the same ECPs before and after forward biasing.

Table I. α method extraction

V_g	ReZ_{11}	ReZ_{12}	α	R_s
0.8	12.05	5.74	0.45	3.59
1.0	9.27	5.33	0.39	3.50
1.2	8.77	5.17	0.33	35.9
Final R_{ch}=4.74, N=1.31, R_s slope=0.0000, R_g=3.19				

4. Pad capacitance determinations

Most pad-capacitance extraction methods measure pinched-FET S-parameters at $V_g<V_{th}$ and $V_{ds}=0$. The measured S-parameters are converted to Y parameters which depend on six capacitances (Fig.1b):

$$C_{pg}+C_{gs}=(ImY_{11}-ImY_{12})/\omega,\ C_{gd}+C_{pf}=ImY_{12}/\omega,$$
$$C_{pd}+C_{ds}=(ImY_{22}-ImY_{12})/\omega \quad (3)$$

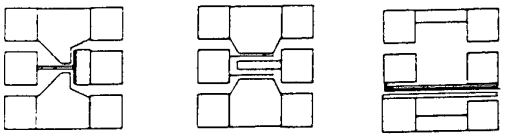
so the extraction problem becomes one of solving three equations in six unknowns. There are four approaches to this:

1. Since C_{gs}, C_{gd}, and C_{ds} scale linearly with the FET width, measure FETs of different widths but the same number of fingers and fit the capacitances to linear functions of W, the intercepts being the pad capacitances. This procedure can be repeated for FETs with different numbers of fingers n, and the intercepts can be fit to linear functions of n allowing scaleable FET models to be generated for any FET layout and width.
2. Since the fringe capacitances C_{gs} and C_{gd} are guaranteed to be the same at $V_{ds}=0$ and $V_g<V_{ds}$, C_{pf} is often small, one can get C_{pg} from the difference ImY_{11}-$2ImY_{12}$. Furthermore in symmetric layouts (see below), often C_{pd} and C_{pg} are similar, therefore one can put C_{pd}~C_{pg}.
3. Measure zero width FETs, where all of the test pad interconnections are present but the active fingers are absent.
4. Measure dummy FETs where the active fingers are made inactive by implant damage.

Our experience with these techniques is as follows:

1. Method 1 is best if one can persuade the foundries to construct FETs with different widths but the same number of fingers. (Foundries who are serious about developing scaleable device models do this.)
2. Method 2 is the best one can do if only a single FET can be measured. The errors in the pad capacitances are thereby absorbed into the active FET capacitances, C_{gs}, C_{gd}, and C_{ds}, which then may not scale linearly with width, but the S-parameter fits are about the same.
3. We have no experience with measuring zero-width FETs though we have compared on-wafer open measurements (structures with just the test pads but no interconnections to the fingers) with results of method 1: the open pad measurement does not give the same pad capacitances because the interconnects are absent.
4. Dummy FETs still give values of C_{gs}, C_{gd}, and C_{ds} that scale with width, which are not the same as the active FET capacitances, but are not negligible, therefore this method does not solve the problem of extracting 6 capacitances from 3 measurements[6].

Table 2: Layouts and typical ECPs



ECP	coplanar T	Symmetric	Asymmetric
L_s	4	-0.2	0.07W+76
L_d	32	31	0.114W+14
L_g	42	39	0.1W+69
C_{pg}	28	3n+24	17
C_{pd}	8	4n+16	31
C_{pf}	9	1.5n+1.3	9
R_g	.0031W+0.5	$0.043W/3n^2$+ 0.47	0.56+0.0169W

W in μm, C in fF, L in pH, R in ohms; n: number of fingers

5. Results

Table 2 shows three generic layouts we have measured many times and typical values of the inductances, gate resistance and pad capacitances. The T layouts are common test layouts, although the symmetric layouts more closely approximate the FET layouts in active circuits. The highly asymmetric layout was designed originally for DC measurements, and the pad layout was made compatible with RF measurements as an after thought. This structure has very large inductances. For the symmetric layout we measured FETs with 2,4,6, and 8 fingers, therefore could fit the pad capacitances to linear functions of the number of fingers. Although the inductances should scale as W/n^2, the scaling is rarely observed, for the inductances are dominated by interconnect values. One can show, using standard microstrip formulas for ρ_{lg} and ρ_{ld}, that the expected active-FET inductances for two or more fingers are very small compared to what is observed.

Under the US MIMIC program, we measured up to 100 FETs per wafer on many wafers in an attempt to understand the relationship between process and device variations. One important variation is in the gate

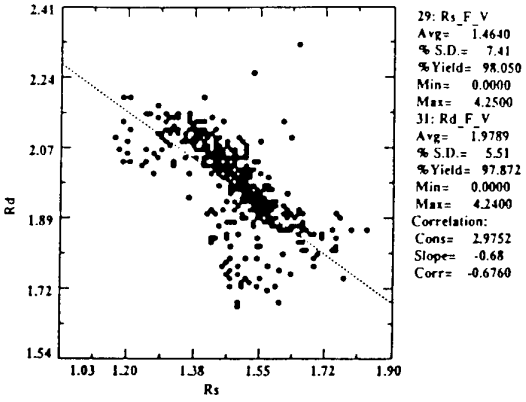


Fig.5a. R_s versus R_d for FETs on a single wafer

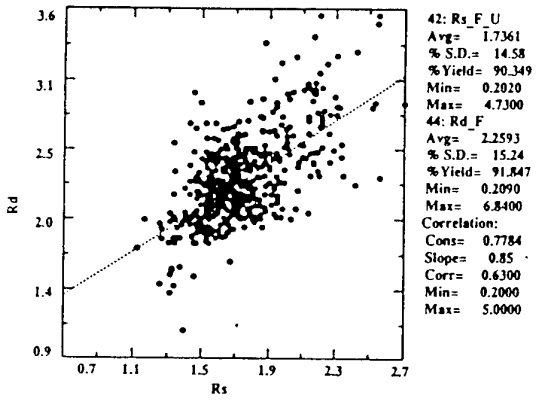


Fig.5b. R_s versus R_d for FETs on twelve wafers.

placement using contact lithography in the period 1989 to 1991. Information about the gate placement can be obtained the difference ReZ_{22}-$2ReZ_{12}$ =R_d-R_s, which is independent of any assumption made about R_{ch}. If the source and drain contact resistances are the same and the R_n. contributions are neglected, one can show using the Fukui approximation that L_{gs}-L_{gd}~(R_d-R_s)/R_{n+}, therefore distributions of the gate placement accuracy can be mapped. This method works only in T and single-finger layouts. In the symmetric layouts, when the gate is closer to the source on one finger it is further on another, therefore the effects are washed out. Figure 5a shows typical correlations between R_s and R_d for a single wafer from one foundry. Figure 5b shows correlations for the same foundry where we include data for many different wafers. In this case the contact resistance variations from FET to FET which contribute equally to R_s and R_d are greater than the alignment variations, so the correlations become positive.

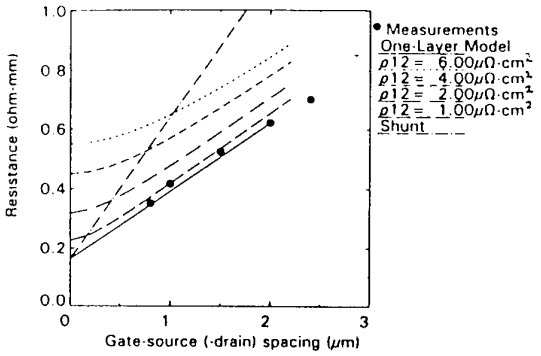


Fig.6. R_s and R_d versus the gate-source or gate-drain distance for pHEMTs with several models

Figure 6 shows how pHEMT source and drain resistances scale with the gate-source or drain-source distances. Here we constructed three HEMTs with fixed source-drain spacings and varied the gate-source distance, so three data points in Fig.6 give R_s versus L_{gs} and the other three R_d versus L_{gd}. For MESFETs, the resistance-versus-spacing slope is the sheet resistance of the unetched region of the FET and the intercept is the contact resistance, both of which can be determined equally well using the DC transmission-line method[10]. For HEMTs, these measurements allow us to obtain information about the contact resistance to the 2d gas. As shown in Fig.6, if the contact resistance to the 2d gas ρ_{12} is greater than about $2x10^{-6}$ohm-cm^2, the resistances increase. This pHEMT has a very small 2d gas contact resistance because the AlGaAs layer is thin and highly planar doped, so that the electron concentration in the AlGaAs layer is greater than 10^{16}cm^{-3}. If one increases the barrier height of the cap-high-bandgap-channel junctions, the high-bandgap material will have fewer carriers, which increases the contact resistance to the 2d gas. This is the case in InP/InAlAs/InGaAs HEMTs where the InP/InAlAs and InAlAs/InGaAs barrier heights are very large. In these HEMTs it is possible that the connection to the 2d gas is made in the alloyed contact region, in which case the slope of the resistance versus spacing would give the sheet resistance in the 2d gas ("shunt" in Fig.6).

6. Conclusions

This review has tried to summarize my experience with parasitic resistance, inductance, and pad capacitance extractions for a wide variety of FET and HEMT technologies. While similar methods have been used by others in some cases, I apologize for not including comprehensive references to other work. The general conclusions are these: no single method is guaranteed to work for every technology. A flexible extraction program that can make use of several different methods is best, and until one knows for sure which method will work make cold FET measurements at several biases (Vg~0, 0.5, 0.8, 1.0, 1.2V, and pinched) so that the methods can be compared. In production, when may wafers are measured one can get by with making a single pinched FET and cold FET S-parameter measurement, using fixed values, usually of R_{ch}.

These methods give scaleable active FET models for use in circuit simulators, though usually the pad capacitances and the inductances, which are not part of FET in the active circuit are not required. Such methods also allow unique determinations like the gate-source alignment accuracy and the contact resistance to the 2d gas to be determined.

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Frequency-Dependent Measurement Error Analysis and Refined FET Model Parameter Extraction including Bias-Dependent Series Resistors

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Abstract - The extraction of physically meaningful equivalent circuits of FET devices from S-parameter measurements on the basis of optimization strategies is impeded by the local minimum problem which is becoming more severe with extended broadband equivalent circuits of FETs needed for reliable microwave and millimeterwave circuit design. A novel concept and fundamental requirements on measured S-parameter data for successful parameter extraction are presented. Accurate effective correlating capacitances and inductances are determined from pinch-off S-parameter data. Regarding the distributed nature of the broadband equivalent circuit, well-defined initial values for the gate-, drain-, and source-inductance are derived in dependence on estimated distribution of the effective capacitances on the gate and drain side. Optimization is based on a random search technique with adaptive starting interval sizes. An improved Simplex algorithm is used for multi-frequency data fitting. The new extraction concept converges very fast. Human intervention for guess of suitable initial element values is omitted. Nearly all model elements are consistently extracted. However, due to S-parameter measurement uncertainties stable but not always physically meaningful values for the resistances R_s and R_d are obtained. This special extraction problem is solved by using only two S parameter data sets, one at a fixed low frequency controlling the effective capacitance and inductance and the other is scanned over the upper measured frequency range mainly controlling the parameter distribution and the relatively insensitive resistances. An upper frequency is fixed within a measurement interval that reveals confidential (i.e. physically meaningful) parameter values. The extracted bias-dependence of R_s for a wire-bonded 0.4 μm gate-length MESFET and a 0.15 μm gate-length HEMT reflects the expected physical properties.

I. INTRODUCTION

Accurate small-signal parameter extraction of microwave and millimeterwave FET models is very important for an efficient nonlinear device modeling approach. The topology of common FET lumped element equivalent circuits can be partitioned into a linear extrinsic part covering the device parasitics, and a nonlinear intrinsic one which models the active region. Knowing the parasitics the nonlinear device modelling process is tremendously simplified and restricted to the inner part with a reduced number of model elements [1].

The problem of small-signal model parameter extraction from S-parameter measurements has been widely discussed in the literature for a long time ([2]-[16]). Various procedures have been proposed focussing on the consistent extraction of model elements. Nevertheless, the question remains whether the derived values are physically relevant. This applies especially to the less sensitive model parameters like the gate-, source-, and drain-resistance (R_g, R_s, R_d), and the resistive elements in series with the gate-source and the gate-drain capacitance (R_i, R_{gd}). The validity of the equivalent circuit is commonly deduced from the frequency dependence of the extracted model parameters [17]. Our own experience has shown that frequency dependence can be obtained with different kinds of model topologies [18]. Hence, the physical relevance of extracted R_s and R_d elements seems to be an additional issue. Confirmation of the extraction accuracy or physical relevance is often concluded from non-negative or non-zero extracted element values, and R_s being equal or smaller than R_d in the saturated regime. Small variations in the model topology or model complexity may result in a significant change of the resistance values. The observed topology dependence of extracted element values makes physical validation of the extracted results more difficult.

Model parameter extraction is primarily based on the measured data. The degree of accuracy of the device database manifests itself in all subsequent steps in the modeling process and the final circuit design. The measurement database is therefore a key factor in the complex parameter extraction procedure which strongly dominates the confidence and usefulness of extracted parameters ([1],[19]). An analysis of the extracted results in relation to the measurement database reveals a strong correlation between measurement uncertainties and accuracy or reliability of the extracted model parameters. With this knowledge, some well-known fundamental problems in the small-signal model parameter extraction process

migth become transparent, so that specific optimization of the entire modelling process can be performed. To the best to our knowledge, only a few authors have devoted efforts to the severe influence of measurement on the extraction process and analyzed the accuracy of derived model elements on the basis of given measurement uncertainties (e.g. [15]).

II. ACCURATE MEASUREMENT - BASIS OF SUCCESSFUL EXTRACTION

Measurements should be performed with utmost care. As will be shown, extraction should not rely on S-parameter data measured at a large number of frequency points. Only a few points (at least two points), if measurement uncertainty is very low, might give more reliable results. The evaluation of measured data with respect to the utility for parameter extraction assumes some experience and expert knowledge in this field. Hence, it is sometimes advisable to repeat the experiment and to refine the measurement technique and extraction method instead of working with obvously faulty S-parameter data, and to become frustrated over the intensive extraction effort. To pre-empt the frustrating experience, it is very important to analyze the potential measurement errors in advance before starting with the final extraction process. Model parameter extraction can only be performed on a database which may be accepted with some confidence to be a reliable description of the device properties and not dominated by instrument errors or operator manipulation.

The attainable accuracy of device data is restricted to the performance of the coaxial measurement system used, mostly a vector network analyzer (VNA), and in particular to the calibration method applied to characterize the transition from the coaxial to the planar transmission line for 'in-fixture' and 'on-wafer' measurements. As is described in Ref. [20] system calibration is performed in two steps, i.e. network analyzer calibration is prior to the entire system calibration. This is well suited to distinguish between the residual calibration errors due to the VNA and the errors resulting from the coaxial-to-planar transmission line transition. The potential sources of VNA measurement errors are well documented in Ref. [21]. The overall system performance specifications consider the different kinds of error sources such as systematic, random, and drift errors. Systematic errors result from stable imperfections and inaccuracies associated with the calibration standards and measuring instrument hardware. Random errors result from the normal variations which are characteristic of a given process. Drift errors are considered to be time or temperature dependent performance characteristics. Once the instrument calibration is completed residual (post-calibration) errors become noticeable [21]. Residual errors result from the imperfections in the calibration standards, the connector interface, the interconnecting cables and the instrumentation. For systematic errors magnitude and phase uncertainty specification is performed on a worst case vector basis, which means that the total effect of such erros is summed up by conventional addition [15]. Experience shows that the actually measured errors are usually much lower than defined instrument specifications. Hence, simple estimation of model parameter extraction uncertainty on the basis of overall measuring instrument performance specifications does not deal completely with the realistic capabilities in the parameter extraction process (see e.g. Ref. [7]). Therefore, Vidkjaer [15] proposes a more distinct error analysis with respect to device modelling tasks. Instrument uncertainty is derived from a detailed analysis of the nature of all potential error sources, and in particular, whether they are correlated or not rather than on systematic or random distinction. Finally, as is outlined in Ref. [21], the operator error focussing on improper connection technique, connector dimensions, and contact surfaces might be the largest error in the data acquisition.

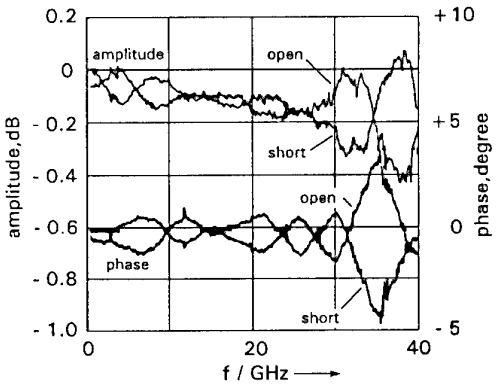

Fig. 1 Calibration verification of the HP 8510 with an coaxial offset short and open (phase compensation for the additional offset length included).

Fig. 1 illustrates the residual errors measured [23] with a VNA of type HP 8510 [22] using coaxial SOLT calibration. Commonly, calibration verification is performed with a coaxial offset short or/and open standard. As discussed before, due to imperfections of the descriptions of the calibration standards, and an assumed error model of the measuring system, residual systematic errors remain after the correction. These manifest themselves as ripples in the recorded frequency-dependent amplitude and phase of the measured offset calibration standards. From the ripple distance a length of about 16 mm can be estimated for the used offset (airline). The crossovers due to the approximate anti-phase shift between short- and open-

circuit ripples give error-corrected true values for the measured standards. The drop of the crossing points with frequency is caused by the offset transmission loss. Due to this reference the residual systematic error of amplitude and phase is extremely low up to about 30 GHz. At higher frequencies the amplitude and phase error increases to about 0.52 dB, and 4 degrees respectively.

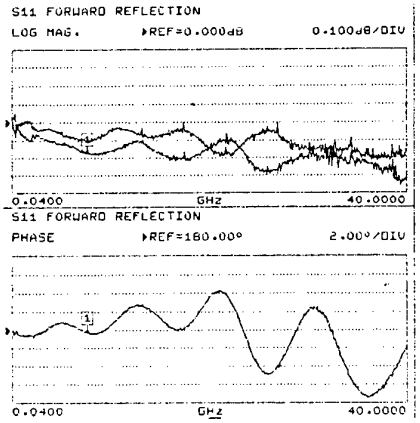

Fig. 2 Amplitude and phase calibration verification of a 40 GHz Wiltron system.

Fig. 2 illustrates a similar verification result for the Wiltron 40 GHz VNA system Model 360 [24]. It can be seen that the ripples representing the amplitude errors are close to the lower frequency data given in Fig. 1 over the whole bandwidth. The residual systematic phase errors, however, are relatively large, and reach values up to 7 degrees.

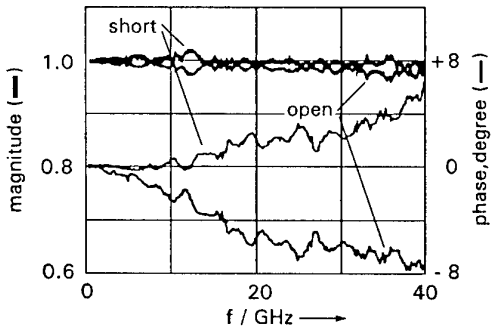

Fig. 3 Measured reflection coefficient of of an open and short in microstrip technique.

Regarding in-fixture meassurement additional errors are contributed by the test fixture. We developed our own apparatus and calibration procedure [20]. Fig. 3 illustrates the calibration verification result including the system errors of the used VNA (see Fig. 1). The ripples are attributed to the length of microstrip lines being 1 inch. It can be seen that a maximum amplitude error of 0.02 is observed for frequencies less than 30 GHz. Above, errors up to 0.06 have been measured. The phase error with respect to the mean straight lines is within about 2 degrees up to 30 GHz. Above, error values up to about 4 degrees can be attained. As seen before the amplitude and phase errors of the short are in antiphase of those for the open circuit.

In the following some examples of significant measurement errors in conjunction with FET device characterization will be discussed. Different kinds of measurement errors and their potential disastrous influence on the model parameter extraction process in particular with respect to low-valued resistances will be illustrated.

Recently, measurement systems have been developed making S-parameter measurement possible over a broad frequency range from 45 MHz up to about 118 GHz [25]. Calibration is performed in three different frequency bands, 45MHz - 50 GHz, 50 - 75 GHz, and 75 - 118 GHz. The lower band uses coaxial technique, whereas the latter ones waveguide technique.

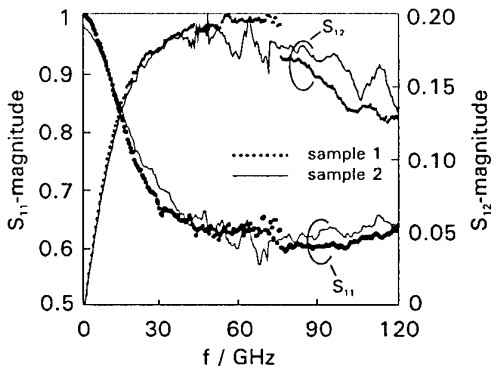

Fig. 4 Measured response of different samples of a 0.15 μm T-gate HEMT (IAF).

Fig. 4 shows the measured response of two samples of a 0.15 μm gate-length HEMT fabricated at the Fraunhofer Institute of Applied Solid State Physics (IAF). As can be seen the recorded data for sample 1 show a sharp inconsistency in the trace at the transition of the middle to the upper frequency band which is totally unreasonable and unexpected from the device performance. Such illegitimate error [26] which may have resulted in this case from faulty calibration of the used equipment, can be dealt with immediately. Generally, it is recommended to repeat and to improve the experiment before extraction if obviously incorrect data points have been measured. Calibration should be successfully refined until the measured data can be accepted by visual inspection with some confidence to be a reliable response of the device. This has successfully been attained with the measured data of sample 2, showing a smooth transition between the different calibration regimes. As will be shown the fast oscillating ripples, though they are undesired, may be controlled to a large extent by the new extraction strategy proposed in this paper. It is assumed that the recently presented

broadband single-connection vector network analyzer HP 8510XF [27], which covers 45 MHz to 110 GHz in one sweep and single connection (i.e. with no band breaks) will eliminate the discussed calibration errors.

It is assumed that the ripples in the trace of S_{11} in Fig. 4 mainly originate in the incomplete calibration of the probe-tip-to-transmission-line transition and the transition from the coplanar line to the shielded line on the probe for which a distance less than 1 mm could be roughly estimated by visual inspection which is consistent with the measurement based estimation of about 0.7 mm.

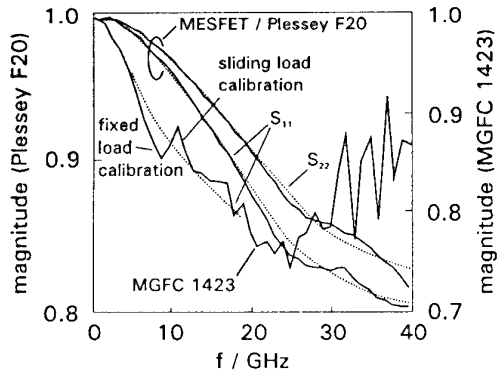

Fig. 5 Illustration of existing measurement errors.

Fig. 5 shows typical device data measured with the 40 GHz HP 8510 system. Regarding the traces for the wire-bonded MESFET MGFC1423 biased at (V_{GS}= -2.0V, V_{DS}=0V) it can be seen that the measured trace shows a slight inconsistency at 10 GHz which originates in the frequency dependent properties of the different calibration standards used. At lower frequencies a 50 ohm chip resistor is used as fixed load, showing increasing load mismatch with growing frequency. The electrical length of the surface ferrite absorber used as a sliding load at frequencies above 10 GHz determines the matching properties. Improved load matching is given with growing frequency. Looking at the scale of the diagram such measurement errors would hardly be noticeable in Smith-Chart representation, and, hence, seem to be without any serious effect on the extraction process. 'Reasonable match' between calculated and measured device response [36] may be convenient for the extraction of highly sensitive model parameters, however, this is not true for the resistive elements.

On-wafer measurements exhibit due to shorter length of transmission lines internal multi-reflections with slow-moving undulations. If in this case the device response is measured in a limited frequency interval, there is a temptation to accept the faulty data partly as true values. Fig. 5 shows the measured magnitude of S_{11} and S_{22} for a MESFET fabricated at the Plessey foundry (2x100 μm, V_{GS}=-2.0V, V_{DS}=0V). Up to about 25 GHz the traces are clear and may be accepted with some confidence to be reliable results. However, as is indicated by the mean-valued dotted line of the slowly varying measured data, extraction based on such a limited frequency range would yield model parameter values having no physical relevance at all.

III. UNIFIED FET MODEL TOPOLOGY

Under small signal conditions the electrical properties of the FET device are equivalently described by a linear 2-port (or 3-port) characterized by the scattering coefficients. Following the various physical effects within the device, an equivalent physics related network can be deduced comprising resistors, inductors, capacitors and voltage controlled current and charge sources, and diodes as well. The model element values are found by fitting the simulated response to measured data.

A variety of model topologies are known from literature (e.g. [7],[25],[28],[37],[38]). It has been found that a minimum number of model elements is necessary to permit a satisfying fit of measured and simulated response. Often the standard 15-element model is used. Our experience shows that the extracted model parameter values depend on the chosen equivalent network topology. Often obviously unphysical values (e.g. negative resistances) are extracted. The multi-bias extraction approach ([1], [16]) applied to the standard 15-element model, commonly supplies R_g values which tend to be overestimated with respect to R_s and R_d. Often the value of R_s is much smaller than expected from device geometry and material considerations.

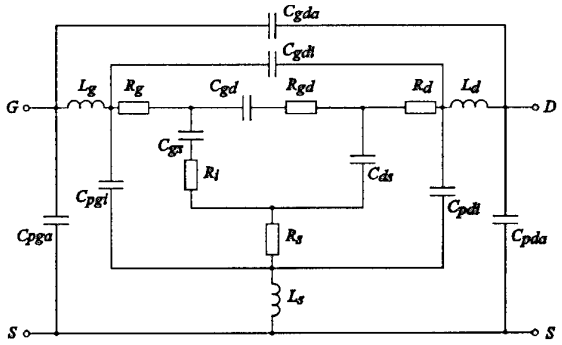

Fig. 6 Broadband pinched-FET equivalent circuit.

How can we emerge from the topology dilemma? The topology of the device should reflect the following technological device regions: inner active part with the voltage-controlled sources, intermediate part comprising the main device parasitics such like interelectrode capacitors and electrode inductors, and outer part describing the capacitive pad area of the device and the actual probe-to-device-connection. Fig. 6 shows the proposed topology under pinched-off condition with 17 model elements. Regarding the

saturated regime the circuit is to be completed by the drain current source and channel conductance both in parallel to the drain-source capacitance C_{ds}. We have tested the topology with different devices using both in-fixture and on-wafer measurements. Table I summarizes the investigated FET devices.

PRODUCT/ FOUNDRY	TYPE	L_g (μm)	w (μm)	MEAS.
MGFC 1423	MESFET	0.4	300	in-fixt.
JS 8902-AS	HEMT	0.3	200	on-wafer
Plessey	MESFET	0.5	100	in-fixt.
IAF	HEMT	0.3	100	on-wafer
IAF	HEMT	0.15	100	on-wafer

Table I Investigated FET devices.

As will be shown the distributed nature of the gate-source and drain-source capacitances of the pinched-FET model is very useful e.g. to fit the measured data of the 0.15 μm gate-length (0.12 μm was measured for the investigated device) IAF-HEMT up to 120 GHz. Most of the published FET models can simply be derived from the proposed one by excluding appropriate elements.

IV. DETERMINATION OF EFFECTIVE CAPACITANCES AND INDUCTANCES FROM PINCH-OFF MEASUREMENTS

For lower frequencies an effective gate-source capacitance C'_{gs}, gate-drain capacitance C'_{gd}, and drain-source capacitance C'_{ds} can be evaluated from measured data (Fig. 7). C'_{gs} has three components (see Fig. 6): a component C_{pga} due to the external test pads, a component C_{pgi} due to the fringe capacitance of the innerelectrode metallization pattern, and a part C_{gs} that is bias-dependent and due to the active FET. Similar splitting of the effective values can be considered for C'_{gd} and C'_{ds} too. This can be written as follows

$$C'_{gs} = C_{gs} + C_{pgi} + C_{pga} \quad (1)$$

$$C'_{ds} = C_{ds} + C_{pdi} + C_{pda} \quad (2)$$

$$C'_{gd} = C_{gd} + C_{gdi} + C_{gda} \quad (3)$$

In a single measurement it is not possible to separate the three components. It should be noted that the primed effective gate-, drain- and source inductances are not equal to L_g, L_d, and L_s in Fig. 6. The inductance values in the distributed model depend strongly on the distribution of the effective capacitances.

Our experience is that for the various investigated

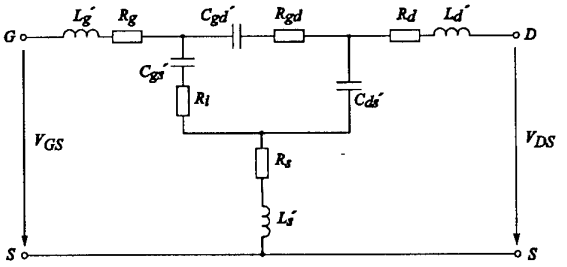

Fig. 7 Pinched-FET equivalent circuit with effective capacitances and inductances.

devices (wire-bonded, probe tip contacted) the generalized topology which is of distributed nature at the input and output port describes the electrical properties for all investigated devices excellently. Moreover, it includes many topology variations proposed in the literature. Indeed, the splitting of the effective capacitances into three separate capacitors, which are generally required for broadband data fitting, depends on the given device construction. Simplification is possible in particular cases.

As the probability of trapping into a local minimum is increased with increased number of optimizable parameters, complex structures as given in Fig. 6 are commonly avoided. Nevertheless, the extractor should be able to output element values within confidential limits, i.e. values which can be accepted by physical inspection of some elements. This should also be true with the more insensitive resistors. Because the pad capacitances associated with C_{gd} are generally small we assume

$$C_{gdi} = C_{gda} = 0 \quad (4)$$

and with (3) it follows

$$C'_{gd} = C_{gd} \quad (5)$$

In a pinched FET the gate-source capacitance C_{gs} equals the gate-drain capacitance C_{gd},

$$C_{gs} = C_{gd} \quad (6)$$

Fig. 8 shows the pinch-off model finally used.

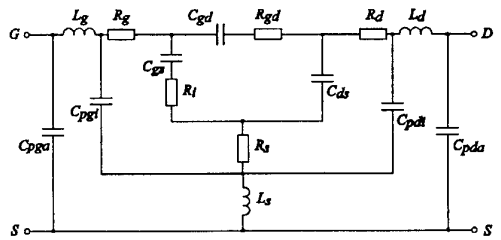

Fig. 8 Used distributed pinch-off model for the FET device.

For frequencies tending to zero ($f \rightarrow 0$) the equivalent network of the device behaves like a capacitive network (Fig. 9). The effects of the series resistances and inductances become negligible compared to the capacitances ([29], [39]). Calculating the Y-parameters from the scattering coefficients the

asymptotic approximation for f → 0 results in

$$Y_{11} = j\omega\,(C'_{gs} + C'_{gd}) \tag{7}$$

$$Y_{22} = j\omega\,(C'_{ds} + C'_{gd}) \tag{8}$$

$$Y_{12} = Y_{21} = -j\omega\,C'_{gd} \tag{9}$$

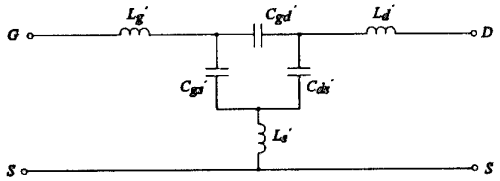

Fig. 9 Reactive pinched-off model with effective capacitances and inductances.

Experience shows that the effective capacitances can be determined from measured data in the lower frequency range with an upper frequency less than 10 GHz [39]. From (7) - (9) the effective capacitances can be calculated as

$$C'_{gd} = -\frac{Im\{Y_{12}\}}{\omega} \tag{10}$$

$$C'_{gs} = \frac{Im\{Y_{11}\} + Im\{Y_{12}\}}{\omega} \tag{11}$$

$$C'_{ds} = \frac{Im\{Y_{22}\} + Im\{Y_{12}\}}{\omega} \tag{12}$$

Fig. 10 shows the derived effective capacitances versus frequency for the 0.15 μm IAF-HEMT. Regarding the high resolution of the diagram scale, the effective capacitances can be evaluated very precisely, neglecting values below about 1 GHz.

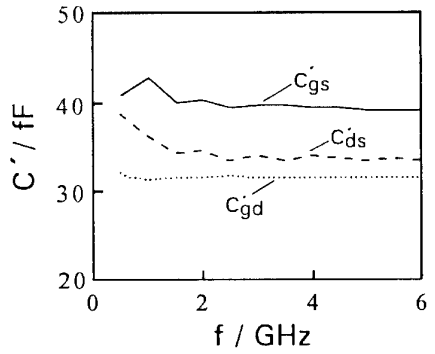

Fig. 10 Effective capacitances extracted for the 0.15 μm HEMT (IAF).

Fig. 11 illustrates the result for a wire-bonded FET chip of type MGFC1423. Also in this case the capacitances can be derived well from low-frequency measurements. The increase of C'_{gd} and C'_{gs} with frequency can be explained by the growing inductive influence.

As the effective capacitances are known, the effective inductances can be derived as follows. Considering Fig. 9 the capacitive π-network can be replaced by a T-network with the elements

$$C_g = C'_{gs} + C'_{gd} + C'_{gs}C'_{gd}/C'_{ds} \tag{13}$$

$$C_d = C'_{ds} + C'_{gd} + C'_{ds}C'_{gd}/C'_{gs} \tag{14}$$

$$C_s = C'_{gs} + C'_{ds} + C'_{gs}C'_{ds}/C'_{gd} \tag{15}$$

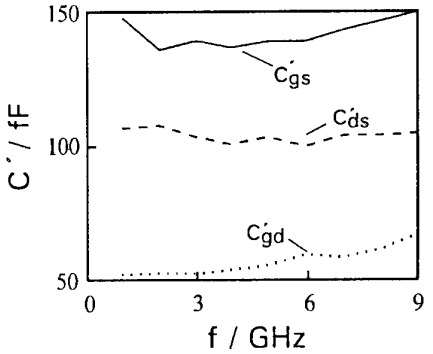

Fig. 11 Effective capacitances extracted for the 0.4 μm MESFET (MGFC1423).

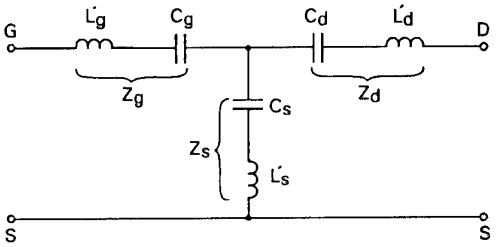

Fig. 12 T-type pinch-off model with effective parameters.

The primed effective series inductances can be derived from the Z-parameters (Fig. 12) as follows

$$L'_{\mu} = \frac{Im\{Z_{\mu}\}}{\omega} + \frac{1}{\omega^2 C_{\mu}}, \quad \mu=(g,d,s) \tag{16}$$

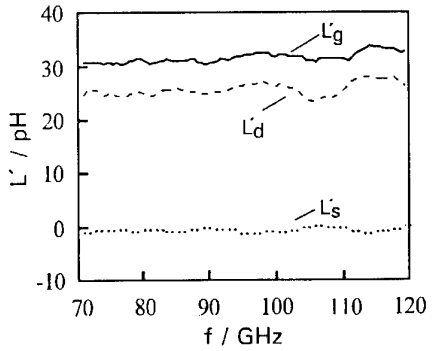

Fig. 13 Effective inductances extracted for the 0.15 μm HEMT (IAF).

Fig. 13 shows the derived effective inductances versus frequency for the 0.15 μm IAF-HEMT. The asymptotic values for f→0 can be well determined. The effective source inductance is evaluated to be about 0 pH. A problem may arise with devices which comprise relatively large external parasitic capacitances C_{pga} and C_{pda}. These can lead to parallel

resonance effects (see Fig. 14) within the measured frequency range which manifest themselves in a monotonous increase of the L'_μ values with frequency. Estimation of the parallel resonance frequency can be easily estimated.

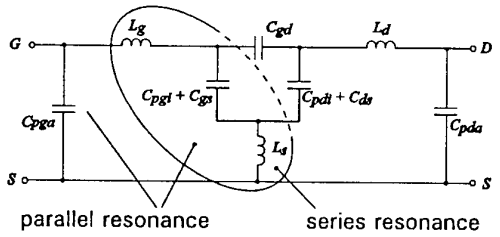

Fig. 14 Existence of parallel resonance at higher frequencies due to the external capacitances.

Considering Fig. 8, the circuit in Fig. 15 can be deduced under the following assumptions: i) the resistances are neglected, ii) the external capacitances are much smaller than the residual ones, and iii) known effective inductances are taken instead of the unprimed quantities for resonance frequency estimation.

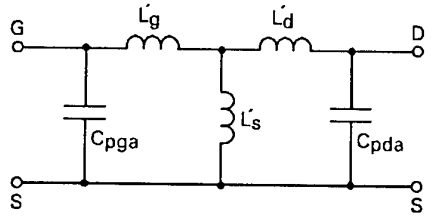

Fig. 15 Circuit for parallel resonance frequency estimation.

The inductive T-structure can be transformed into a π-structure (Fig. 16) with

$$L_{gd} = L'_g + L'_d + L'_g L'_d / L'_s \quad (17)$$

$$L_{gs} = L'_g + L'_s + L'_g L'_s / L'_d \quad (18)$$

$$L_{ds} = L'_d + L'_s + L'_d L'_s / L'_g \quad (19)$$

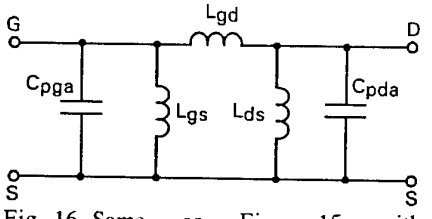

Fig. 16 Same as Fig. 15 with transformed T-structure.

L_{gd} turns out to be very large so that the parallel resonance frequencies at the input and output can be separately estimated. It turns out that the lowest parallel resonance existing with the 0.15μm-gate HEMT lies far beyond the measured frequency range of 118 GHz. However, regarding the wire-bonded MDFC1423, parallel resonance phenomena are already expected around 79 GHz.

Fig. 17 shows the derived effective inductances for the MGFC1423 device. The increase of the inductance with frequency can clearly be seen. At

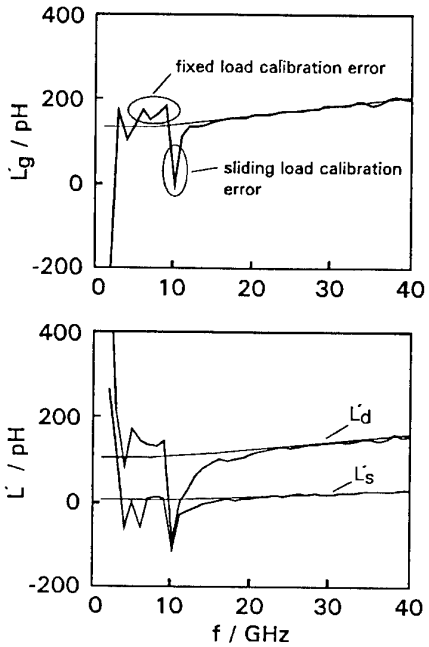

Fig. 17 Effective inductances extracted for the MESFET MGFC1423.

lower frequencies some irregularities arise which originate in the ill-defined calibration standards used (see Fig. 5). Therefore the shown difficulties can in principle be eliminated by further refinement of in-fixture calibration. However, as we will utilize the derived values only as starting quantities for the subsequent optimization process, approximation indicated by the thin solid line is entirely acceptable.

V. STARTING PARAMETER VALUES FOR THE DISTRIBUTED FET MODEL

To start optimization we assume that

$$C_{pga} = C_{pgi} = \frac{1}{2}\,(C'_{gs} - C_{gs}) = C_{pda} \quad (20)$$

$$C_{ds} = C_{pdi} = \frac{1}{2}\,(C'_{ds} - C_{pda}) \quad (21)$$

Eq. (20) means that the residual gate-source capacitance (i.e. effective gate-source capacitance minus gate-source capacitance) is distributed to the external and internal parasitic gate capacitor equally. Eq. (21) is similar to the first one concerning the distribution of the effective drain-source capacitance. As has been shown the effective gate-source and drain-drain capacitance can be determined very accurately from the Y-parameters with $f \to 0$. With the effective capacitance values known, the inductance values of L_g, L_d, and L_s can approximately be derived from the effective inductive quantities taking into account the defined capacitance distribution, i.e. the

model inductances L_g, L_d, and L_s depend both on the related primed inductances and the distributed capacitive gate-source and drain-source network. The model inductances L_g, L_d, and L_s can be estimated to be

$$L_\mu \approx L'_\mu \frac{1 + q_{c,\mu}}{1 - \frac{q_{c,\mu}}{1 + q_{c,\mu}}} \tag{22}$$

where $q_{c,\mu}$ (μ=(g,d)) defines the ratio of the external capacitance C_{pga} and the sum of the capacitances (C_{pgi} + C_{gs}), and the ratio of C_{pda} and (C_{pdi} + C_{ds}) respectively. For $q_{c,\mu} \ll 1$, eq. (22) gives

$$L_\mu \approx (1 + 2q_{c,\mu}) L'_\mu \tag{23}$$

With (20) and (21), $q_{c,\mu} < 1$. The estimation of L_s from known effective values L'_s is based on the following relation

$$L_s \approx L'_s \left(\frac{1 + q_{c,g}}{1 - \frac{q_{c,g}}{1 + q_{c,g}}} \right)^2 \cdot \left(\frac{1 + q_{c,d}}{1 - \frac{q_{c,d}}{1 + q_{c,d}}} \right)^2 \tag{24}$$

If we approximate $C_{ds} \approx C_{pdi} \approx C_{pda}$, the last squared term becomes 3.16 and

$$L_s \approx 3.16 \left(\frac{1 + q_{c,g}}{1 - \frac{q_{c,g}}{1 + q_{c,g}}} \right)^2 L'_s \tag{25}$$

For the 0.15 μm HEMT the values for $q_{c,g}$ and $q_{c,d}$ are 0.10, and 0.13 respectively. Hence, from eqs. (22) - (25) the inductances can be derived: $L_g \approx 1.20\ L'_g$, $L_d \approx 1.26\ L'_d$, and $L_s \approx 4.40\ L'_s$. These are only small corrections because of the low values of the external parasitic capacitance. For the MGFC1423 MESFET the capacitance distribution factors have been calculated as $q_{c,g} \approx 0.22$ and $q_{c,d} \approx 0.30$, leading to the following inductance values: $L_g \approx 1.49\ L'_g$, $L_d \approx 1.69\ L'_d$, $L_s \approx 7.00\ L'_s$.

VI. RANDOM OPTIMIZATION WITH ADAPTIVE STARTING INTERVAL SIZES

Trapping into a local minimum is a fundmental problem in optimization procedures. It is well-known that the nearer the starting values of the model parameters are at the global minimum the lower the trapping probability. Because of measurement errors the global minimum will be noisy which means that extraction can only be performed with some degree of uncertainty. Furthermore, systematic errors can predominate so that any extraction effort may become unsuccessful though the extracted result for some parasitics may be reasonable.

The idea in this paper is to probe the object function near the expected minimum with a variety of carefully defined starting value vectors for the model elements. It is expected that the statistical evaluation of the extracted results will give essential information about the usefulness of the defined starting parameter values based on the derived effective model parameters, and the properties of the searched minimum.

Extraction has been carried out as follows. 100 starting vectors based on uniformly distributed random model parameters within $\pm$ 20% of the derived starting values. The series resistors R_g, R_s, and R_d varied from 1Ω to 5Ω. R_i and R_{gd} were chosen within 10 Ω and 30 Ω. Optimization was starting from each random vector using an improved Simplex algorithm with re-initialization to overcome the local minimum problem. The extracted parameter values are then plotted with respect to increasing residual error of the object function. Re-optimization is performed using reduced starting intervals according to the extracted value distribution of each parameter. After only a few adaption cycles of the interval sizes, the extraction of the parameters is stabilized.

Optimization for the FET model parameter extraction is based on the concept of multiplane data-fitting and bidirectional search as described in [16]. Data-fitting is performed not only in the external measurement reference plane, but also in the internal planes which include the internal π-network. Minimization of the objective function is based on a bidirectional search technique which decomposes the complex optimization problem into easy solvable sub-problems. Because of its known tolerance of large errors in microwave device modeling [30] the l_1-norm is used in the external reference plane. An objective function of l_2-norm is applied to the internal plane because of the necessity of calculating derivatives. Normalized l_1-norm in the external measurement reference plane is used with the objective function,

$$\|\epsilon\| = \frac{1}{4K} \sum_{i,j=1}^{2} \sum_{k=1}^{K} \frac{|Re(\Delta S_{ij,k})| + |Im(\Delta S_{ij,k})|}{m_{ij}} \tag{26}$$

where

$$\Delta S_{ij,k} = S_{ij}^m(f_k) - S_{ij}^c(\vec{p}, f_k)$$

$$m_{ij} = \max_k \left\{ |S_{ij}^m(f_k)| \right\},\ (i,j=1,2)$$

$S_{ij}^m(f_k)$ is the measured S-parameter at frequency f_k, $S_{ij}^c(\vec{p}, f_k)$ is the calculated corresponding S-parameter coefficient derived from extracted values of the model parameters, and $\vec{p}$ the vector of model parameters. K is the number of considered frequency points and m_{ij} the largest magnitude of the measured S-parameters

S_{ij}^{m}. The internal error-function is defined as follows. The branch admittances of the intrinsic π-structure are fitted to each branch element by means of l_2 data-fitting. It turns out that the model parameters can be analytically determined from the measured deembedded internal branch admittances. The error function of l_2-norm reads

$$\|\epsilon\|^2 = \sum_k (\tilde{f}_k z_k' x_1 - \tilde{f} x_2)^2 + \sum_k (\tilde{f} z_k'' x_1 - 1)^2 \tag{27}$$

with the dimensionless normalized variables

$$z_k = Z_k / Z_0 = z_k' + j z_k'' \tag{28}$$

$$\tilde{f}_k = f_k / f_0 \tag{29}$$

and

$$x_1 = 2\pi f_0 C Z_0 \tag{30}$$

$$x_2 = 2\pi f_0 R C \tag{31}$$

where f_0 and Z_0 are the normalization frequency and impedance (e.g. $f_0 = \max\{f_k\}$, $Z_0 = 50\Omega$). The minimum of the error function can be described as $\frac{\partial \|\epsilon\|^2}{\partial x_i} = 0$ (i=1,2,3). This leads to the following linear (2,2)-matrix equation

$$\begin{bmatrix} \sum_k \tilde{f}_k^2 |z_k|^2 & -\sum_k \tilde{f}_k^2 z_k' \\ -\sum_k \tilde{f}_k^2 z_k' & \sum_k \tilde{f}_k^2 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} -\sum_k \tilde{f}_k z_k'' \\ 0 \end{bmatrix} \tag{32}$$

From its solution and the relationship (30),(31) we have

$$R = Z_0 \frac{x_2}{x_1} \tag{33}$$

$$C = \frac{x_1}{2\pi f_0 Z_0} \tag{34}$$

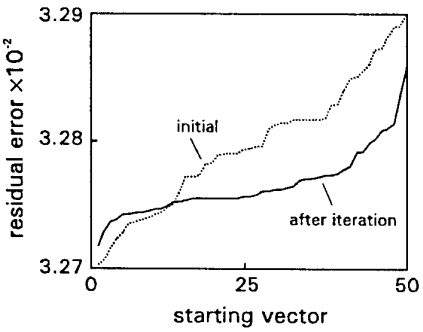

Fig. 18 Residual error of error function sorted according to size versus respective starting vector (MGFC1423).

Figs. 18-24 show the extraction results for the wire-bonded MGFC1423 device. It can be seen that the extraction based on the initial starting vector delivers highly consistent values for the separate gate-source capacitances (Fig. 19). Following iterative optimization based on adaptive reduction of parameter

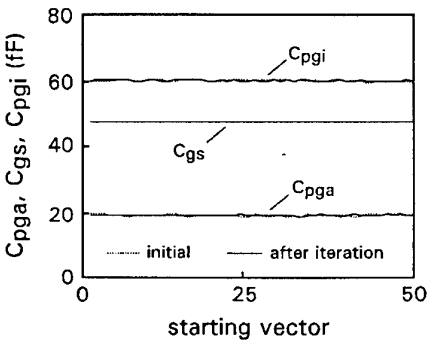

Fig. 19 Extracted individual capacitive elements at the gate-source port.

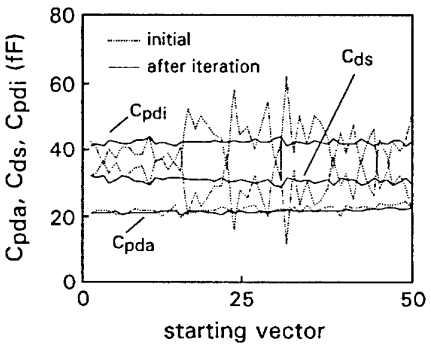

Fig. 20 Extracted individual capacitive elements at the drain-source port.

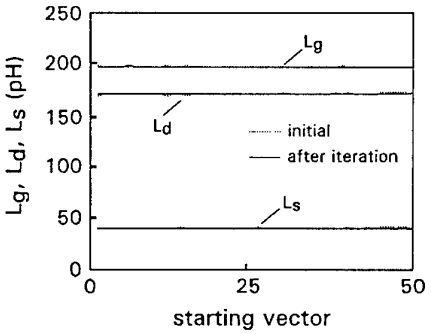

Fig. 21 Extracted inductances.

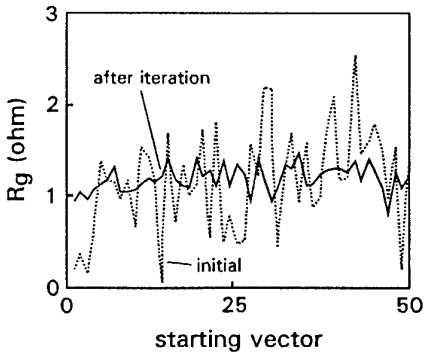

Fig. 22 Extracted gate-metallization resistance R_g.

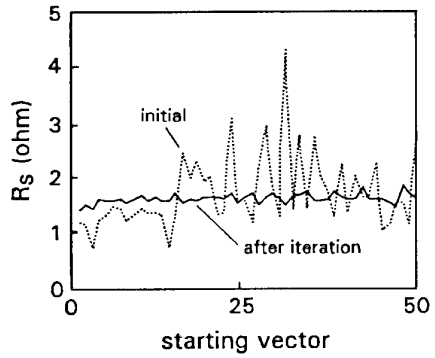

Fig. 23 Extracted source resistance R_s.

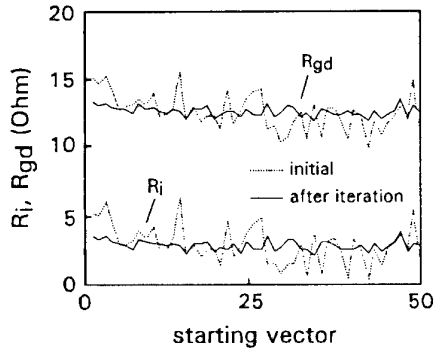

Fig. 24 Extracted values for R_i and R_{gd}.

interval sizes does not essentially improve the extracted values. The obtained traces of the inductances (Fig. 21) can be interpreted in a similar way. As can be seen in Fig. 20 the determination of the external capacitance C_{pda} is rather stable. Conversely, the residual part of the effective drain-source capacitance is initially not clearly related to C_{ds} and C_{pdi}. Some iteration cycles, however, clarify the situation. Regarding the resistances the values initially scatter strongly as expected.

Notice the extracted R_g value of 0.18 ohm for the best fit with a residual error value of 3.27E-2 for the initial starting vectors is truely unphysical. From the information of the manufacturer [23] the aluminium gate of the discussed device has a gate-length of 0.4μm, a gate-width of 260 μm, and a gate-thickness of 0.4 μm. Assuming a conductivity for aluminium between 33×10^6 S/cm (bulk material) and 19.6×10^6 S/cm (for typical MESFET gate structures [31]), the gate metallisation resistance value R_g is expected to be higher than 1.0 and highest 1.7 ohm, which is approximately found along the weakly increasing part of the error function in Fig. 18. Hence, also the best fit of the final extraction seems to be not very reliable with respect to the expected values.

Analyzing the recessed gate structure of the MGFC1423 device [23], and assuming that only the thinned channel under the gate will be depleted under pinch-off, minimum value of 0.3 ohm (contact resistance) and maximum value of 0.67 ohm may be expected. The extracted value of about 1.5 ohm (Fig. 23) cannot be really justified from the physical point of view.

Our experience shows that the best overall fit is not always the best fit for physically meaningful series resistances R_s and R_d. Best fit will be correct in a mathematical sense assuming that the measurement errors are uniformly distributed. It can be seen (Fig. 18) that the minimum of the residual error has also increased after iteration suppressing the unphysical R_g values in Fig. 22. The following Figs. 25-31 show the corresponding extraction for the IAF-HEMT.

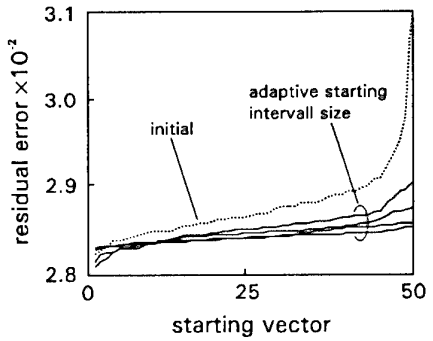

Fig. 25 Residual error of error function sorted according to size versus respective starting vector (0.15 μm HEMT).

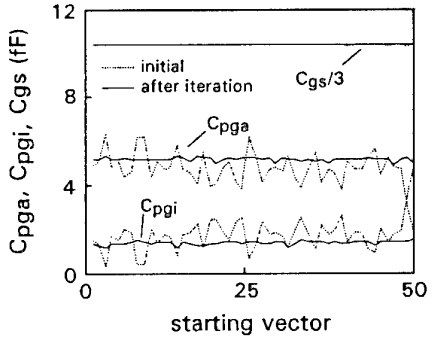

Fig. 26 Extracted individual capacitive elements at the gate-source port.

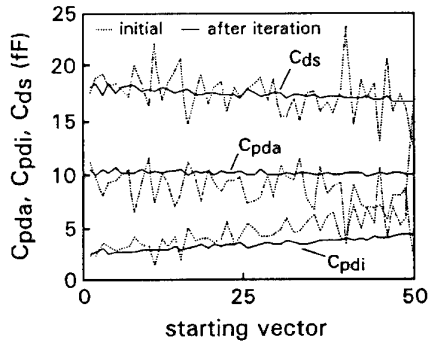

Fig. 27 Extracted individual capacitive elements at the drain-source port.

Considering the separate gate-source capacitances the initially extracted internal gate-source capacitance C_{gs} remains stable (practically the same) after optimization. Conversely, there is an interchange of value contributions between C_{pga} and C_{pgi}, which is

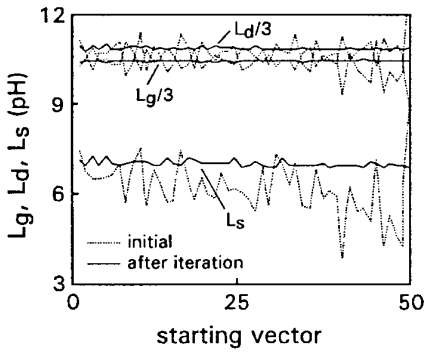

Fig. 28 Extracted inductances.

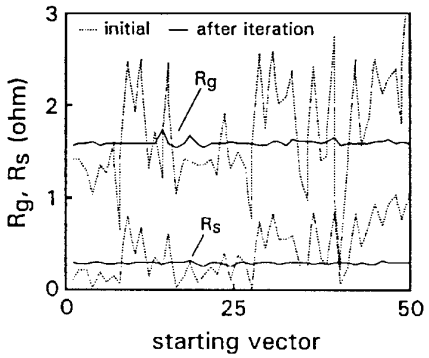

Fig. 29 Extracted gate-metallization resistance.

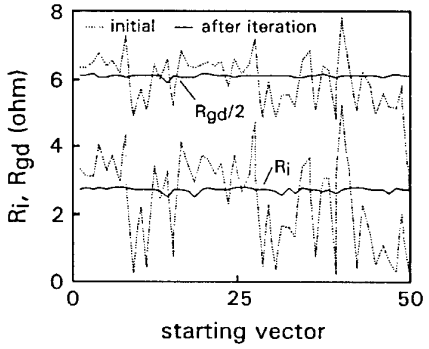

Fig. 30 Extracted source resistance R_s.

resolved during re-optimization with adaptive starting interval sizes. Analyzing the traces for the drain-side capacitances, the extraction shows some interaction between C_{ds} and C_{pda}. After some cycles of iteration C_{pda} turns out to be very stable, and there is some slight value interchange between C_{ds} and C_{pdi}. Fig. 28 indicates correlation between L_g and L_s. A value interchange is observed between both of these and L_d.

The extracted value for R_s being about 0.5 ohm seems to lie outside of the confidence limits. The contact resistance measured under gate forward condition is expected to be 0.15 Ω-mm, i.e. 1.5 ohm for a gate-length of 2x50 μm [32]. No exact data of the cross-section of the 3-layer (Ti-Pt-Au) T-gate was available. Nevertheless, geometry could be estimated from a e-beam microscope photo. Assuming a gold conductivity of 41×10^4 S/cm and a gate cross-section area of about 0.25 μm^2 a gate resistance of 0.8 Ω has been calculated. Assuming a conductivity reduction roughly in the order of 20% for evaporated material, an R_g value about 1 ohm is expected. Frequency dependent increase due to the skin-effect should also be discussed within the measured frequency range up to 118 GHz. Estimation results in an increase less than 10%, so that this effect is not further considered in this paper. In conclusion, the value of $R_g \approx 1.6$ ohm might be accepted, whereas the extracted R_s values are not acceptable.

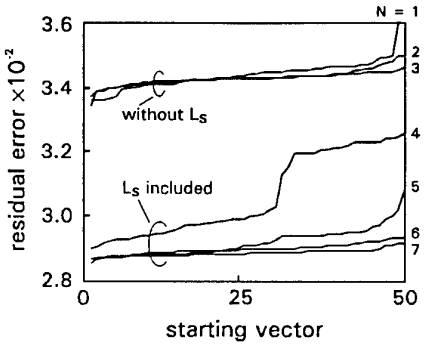

Fig. 31 Residual error of error function sorted according to size versus respective starting vector using arbitrarily chosen starting intervals (0.15 μm-gate HEMT).

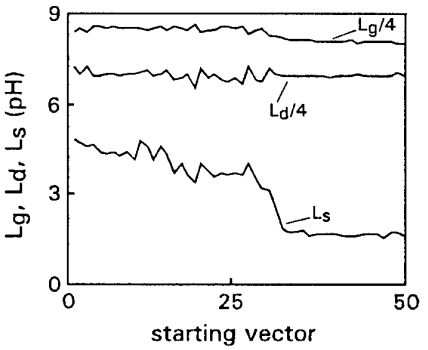

Fig. 32 Extracted inductances due to residual error trace N=4 (Fig. 31).

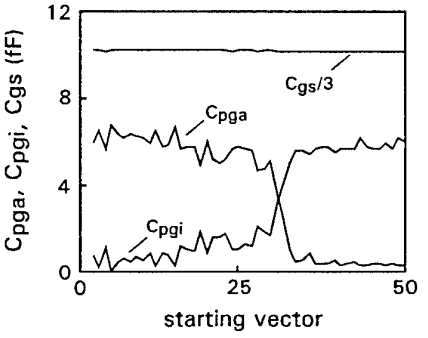

Fig. 33 Extracted partial capacitances at the gate-side due to residual error trace N=4.

Figs. 31-35 illustrate a result based on the usual definition of uncorrelated and very large starting value intervals for the capacitive and inductive elements [18]. The source inductance was first neglected. The residual error stabilized around

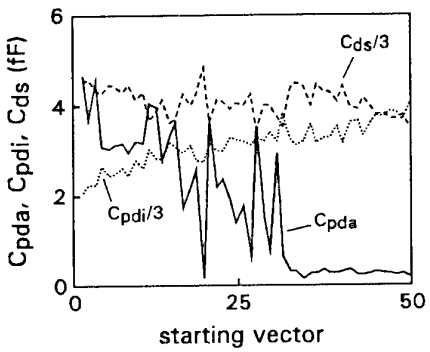

Fig. 34 Extracted partial capacitances at the drain-side due to the residual error trace N=4.

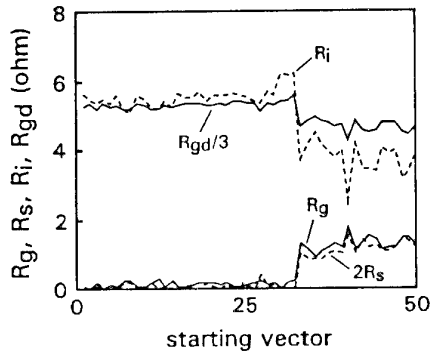

Fig. 35 Extracted resistances due to the residual error trace N=4.

0.034. The inclusion of L_s (1.0-5.0 pH) drastically reduced the residual errors. A very pronounced step-like rise can be observed in the residual error trace. Figs. 32-35 show the corresponding intermediate results. The abrupt change in the residual error function manifests itself in strong parameter value shifts among the capacitances and inductances. This has not been observed with extraction using well-defined starting vectors as described in Sections IV and V. From Fig. 35 it is obvious that following minimum residual error as best fit would lead to a zero-value R_g. To re-start the optimization new starting vectors have been defined taking into account only the upper part of the extracted results.

VII. FREQUENCY SCANNING FOR ERROR-SENSITIVE MODEL PARAMETER EXTRACTION

Standard extraction methods are aimed at reaching the best fit between simulated and measured scattering coefficients at a large number of frequency points. As has been discussed before, the values of most of the model elements can satisfactorily be determined. However, all resistances (especially R_s, R_d, R_g, and R_{gd}) are generally extracted with large uncertainty. Often zero-values for R_s and R_d are derived from pinch-off which is entirely unphysical with respect to the minimum value of the contact resistance. Fig. 36 makes this situation transparent. In this case extraction has been performed in a saturated bias point taking into account all values of the parasitics extracted from pinch-off except for R_s and R_d. Internal elements have then been analytically determined for different resistance values.

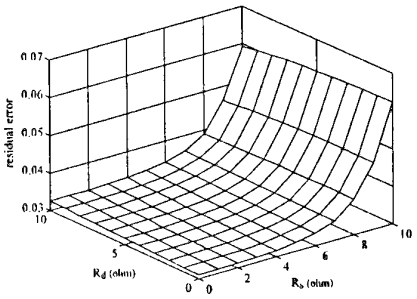

Fig. 36 Residual error versus R_s and R_d for measured S-parameters (0.15 μm HEMT).

Fig. 36 shows the residual error function value in dependence of chosen fixed values for R_s and R_d. As can be seen, no global minimum with R_s and $R_d > 0$ can be recognized. In this case the extractor would deliver zero-values for the resistances. If no minimum resistance values are defined (unconstrained optimization) negative values would have been extracted. It can be shown that due to the present measurement errors commonly the suberror-functions $S_{\mu\nu}$ ($\mu,\nu=1,2$) indicate no absolute minima too. It can be concluded that the common extraction method taking into account measured S-parameter data at numerous frequencies over a broadband frequency range is, due to present measurement errors, not very practical to extract reasonable R_s and R_d values. Fig. 37 shows the result based on synthetic device data. In this case a minimum of the residual error function is clearly seen for the chosen $R_s = R_d = 5$ ohm. Regarding the R_s dependence the residual error increases rapidly for values above the correct value, whereas below the sensitivity is very weak. The dependence of R_d is extremely weak so that R_d was primarily chosen equal to R_s.

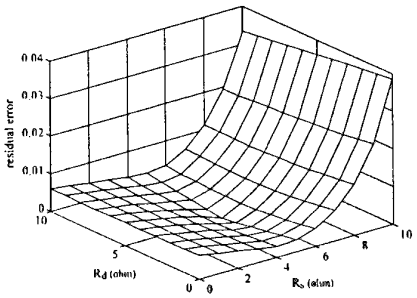

Fig. 37 Residual error versus R_s and R_d using synthetic S-parameters ($R_{s0}=R_{d0}=5\Omega$).

If fixed values are chosen for R_s and R_d, the

internal elements can be extracted from the S-parameter set at any measured frequency point. We used two frequencies, a fixed one in the lower frequency range (e.g. 0.5 or 1.0 GHz), where the internal capacitances are of strong influence on the device response. As can be shown the determination of R_s and R_d needs very high frequencies. A second upper frequency is scanned over the measured frequency band. The quasi-analytical determination in dependence of assumed R_s and R_d values has been performed as described in Ref. [16].

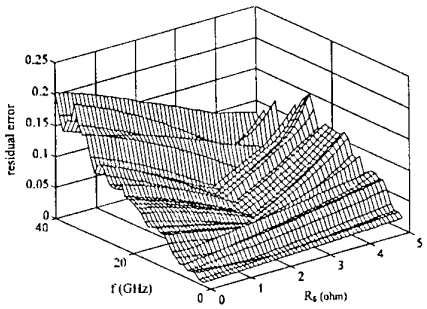

Fig. 38 R_s-dependent residual error for scanned upper frequency (MGFC1423).

Fig. 38 shows the result for the frequency-dependent minimum of the error function value versus R_s. Because of low influence of R_d on the device response, R_d was primarily set equal to R_s. Because of the higher R_s value at the given operating point (V_{GS}=-0.5V, V_{DS}=3.0V) the sensitivity of R_s on the residual error is much higher with increasing frequency. As is expected, no realistic values can be recognized at lower frequencies up to about 10 GHz. Above about 30 GHz, there is no clear information about R_s. However, in the middle frequency range, a very striking behaviour of the error function can be observed. We have investigated for this frequency range the location of the minimum of each suberror-function. We chose a frequency of 16 GHz, at which the minima of the four suberror functions were located at the same value of R_s.

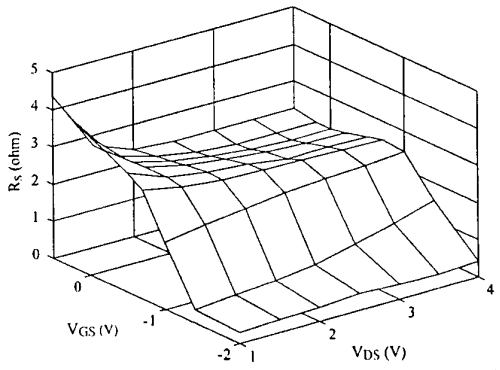

Fig. 39 Bias-dependence of R_s at a frequency of 16 GHz for the MESFET MGFC1423.

Fig. 39 shows the result for the bias-dependent R_s. In the saturation region (V_{GS}>-1V) R_s turns out to be rather bias-independent approximately 2.5 ohm. Towards lower gate-source voltages R_s decreases strongly due to lateral extension of the depletion region [33]. At pinch-off R_s turns out to be about 0.4 ohm which is in the order of the assumed contact resistance of 0.3 ohm. In view of these investigations, we conclude that the extracted R_s values from broadband overall data fitting (see Fig. 23) will commonly not reflect any physical meaning. The extracted values are effective ones which are strongly influenced by measurement uncertainties.

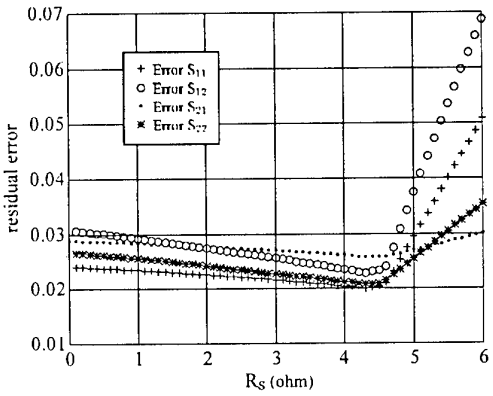

Fig. 40 Residual value of the suberror functions versus R_s for f=117 GHz (0.15 μm HEMT).

Figs. 40 and 41 show similar results given for the 0.15μm-IAF-HEMT. Fig. 40 shows the suberror function versus the scanned value of R_s from 0 ohm to 6 ohm at a frequency of 117 GHz. A clear minimum exists for all curves at the same R_s value of 4.25 ohm. Such concurrent conditions imply small measurement uncertainties. In other cases the minima would have different values. With the frequency fixed, the bias-dependent device model elements have been determined (Fig. 41). With regard to R_s the very opposite is now found in comparison to the previously discussed MESFET (Fig. 39). Now the resistance increases towards pinch-off. At a typical bias point in

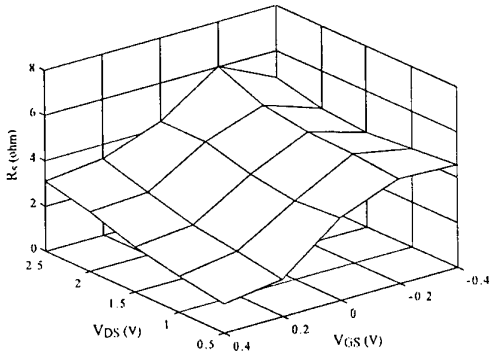

Fig. 41 Bias-dependence of R_s (extracted at 117 GHz) for the 0.15μm T-gate HEMT (IAF).

the saturated region (V_{GS}=0V, V_{DS}=2.5V) an R_s

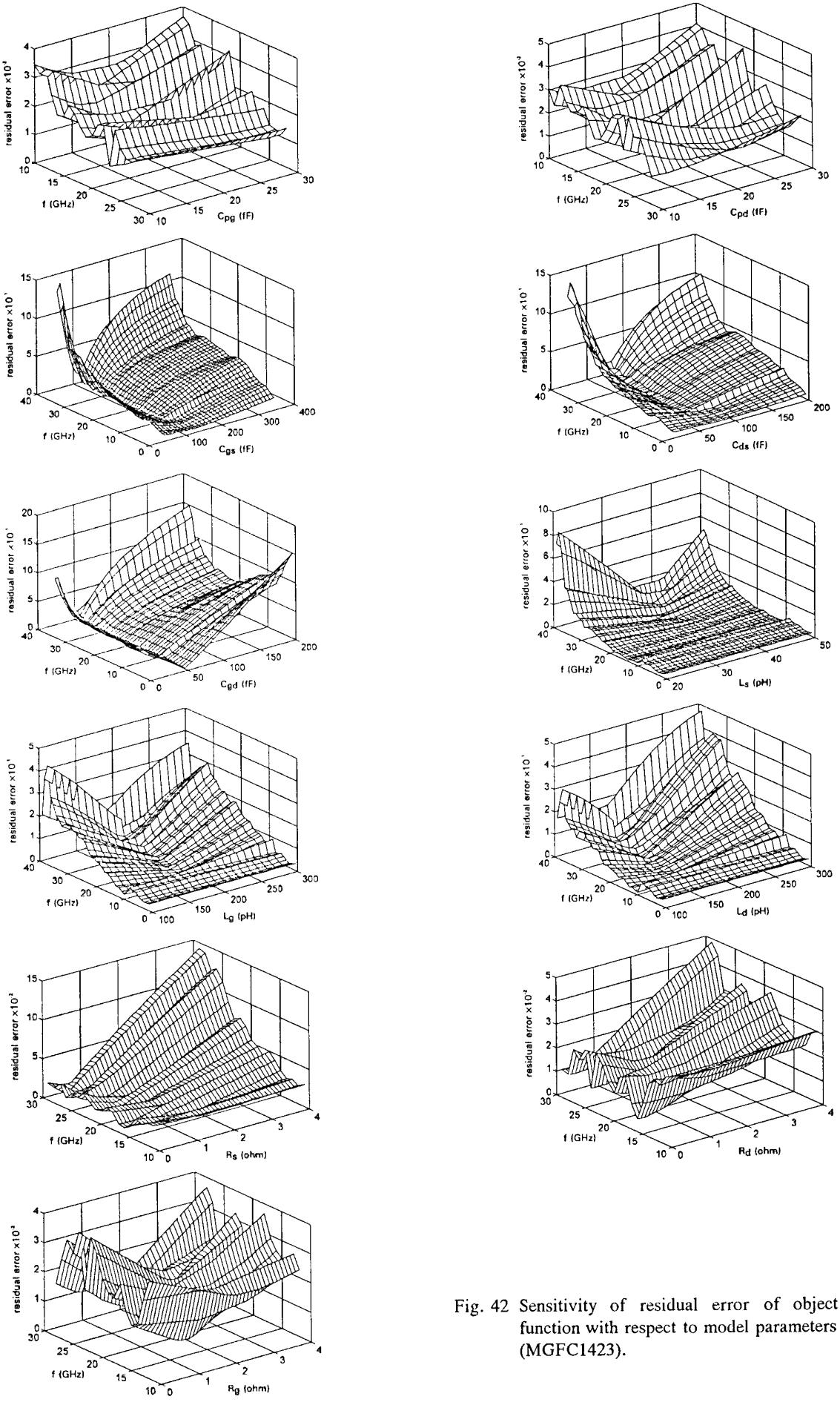

Fig. 42 Sensitivity of residual error of object function with respect to model parameters (MGFC1423).

value of 4.2 ohm has been extracted which correlates well with the expected value in the order of 3.5 ohm [32]. It can be seen that at pinch-off (V_{GS} = -0.4V) an R_s value of 4.4 ohm is extracted, including contact and residual 2-D channel resistance. The estimation of the series resistances of HEMTs is not trivial due to the multilayer structure of the source and drain regions [34] which leads to an interaction between the cap layer conductivity, the channel conductivity and the tunneling conductance [35]. With respect to available data a minimum value of of 1.4 ohm has been evaluated for (V_{GS}=0.4V, V_{DS}=0.5V).

In completion Fig. 42 presents an entire set of graphs showing the sensitivity of model parameters (MGFC1423) with respect to the residual error of object function under pinch-off (compare Fig. 38). Although extraction has only be applied to the standard 15-element model in this case, the results are a positive demonstration that R_s and R_d can be extracted separately [40]. Furthermore, the plot of R_g confirms that the gate metallization resistance can be reliably determined by overall data fitting as was already stated in Sect. VI.

VIII. CONCLUSIONS

Problems well-known in the measurement based device modelling have been illuminated. It has been concluded that before starting the final model parameter extraction process very careful analysis of the measured device data should be performed in order to ensure extraction with confidential results. Common random optimization using arbitrarily defined starting model parameter value intervals may give rise to very strong changes of the parameters during the extraction process. This enlarges the risk to terminate in a local minimum with partly unphysical model parameter elements. We have proposed a new concept for the FET device modelling based on well-defined starting values both for the capacitive and inductive parameters derived from pinch-off measurements. The inherent correlative properties of the starting values of the optimizable parameters lead to very fast and stable convergence of the optimization using parameter value intervals with adaptive size. It is shown that confidential (physically meaningful) information about the less sensitive resistive model elements is almost hopeless. Hence, refinement of the extraction has been obtained using only a fixed lower frequency and second one, which is scanned over the measured frequency range. The extracted values of the resistances clearly indicate confidential measurement regimes with less measurement uncertainties. Using these frequencies satisfying extraction has been performed both in the pinch-off and saturation region. This has been shown in an exemplary fashion by the extracted bias-dependent series resistances.

AKNOWLEDGEMENT

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Periodic Time Domain Waveform Measurement System for Non-Linear Device Characterization

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Abstract: The paper recalls the main results of a study of time domain device characterization and modelling carried out in1986-88 at Helsinki University of Technology.[1] The measurements were performed in the time domain using a high speed sampling oscilloscope. The results were Fourier transformed into the frequency domain to correct the error caused by the linear embedding. The corrected harmonic voltages and currents were combined again in the time domain to produce the actual voltage and current waveforms at the device terminals. The measured results were used for non-linear characterization and modelling of UHF bipolar power transistors used in mobile phones.

Introduction

In the study of non-linear semiconductor devices, the best insight into the device behavior is often gained when the device operation is described in the time domain. At low frequencies the experimental time domain information is easily obtainable using conventional oscilloscopes. At microwave frequencies, high speed sampling oscilloscopes provide equivalent waveform information, but the device behavior is greatly distorted by the dynamic properties of the transistor embedding. In this paper we describe a time and frequency domain system developed in 1986-1988 at HUT for accurate measurement of periodic high frequency voltage and current waveforms. The vector error correction algorithm allows one to take into account and correct the errors caused by losses, mismatches and other imperfections of the measurement system. The system can be constructed using standard, commercially available equipment.

System description

The measurement system for 2-port devices can be seen in Fig. 1. Let us suppose that we want to measure the periodic input and output current and voltage waveforms of a microwave transistor in the non-linear region. The generator part feeds an adjustable sinusoidal input wave

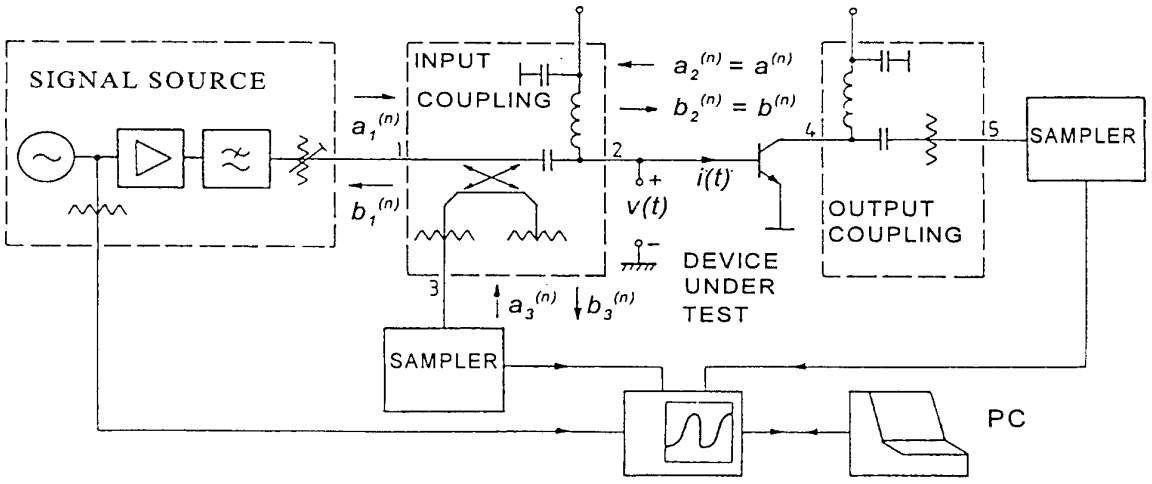

Figure 1 *Time domain waveform measurement system developed at HUT in 1986-88[1]*

which is incident on the device under test (DUT), and powerful enough to drive it into the non-linear region. This gives rise to distorted voltage and current waveforms at the ports of the device. By using a fast sampling oscilloscope, the distorted reflected wave is measured at port 3 of the input coupling network. The transmitted output waveform is simultaneously measured at port 5 of the output coupling network. When the S-parameters of the input and output coupling networks, and the reflection factors of the sampling heads and other terminations are known at fundamental and harmonic frequencies, the accurate nonsinusoidal device waveforms can be determined numerically using the algorithm described in the references[1]. The fundamental incident wave a_1 is first determined by a calibration procedure using a known linear 2-port as DUT. Then, all harmonic waves are calculated assuming that they originate in the non-linearities of the DUT. Finally, the harmonic voltages and currents are obtained from the complex wave amplitudes and combined into the actual terminal voltages and currents.

Waveform determination

The periodic voltages and currents at the device input and output ports can be understood to consist of fundamental and harmonic incident and reflected waves $a_1^{(n)}$, $a_2^{(n)}$ and $b_1^{(n)}$ $b_2^{(n)}$ traveling into and out of the ports 1 and 2 of the non-linear DUT. The normalized wave variables of the input port are defined as follows:

$$a_1^{(n)} = \frac{V_1^{(n)} + Z_0 I_1^{(n)}}{2\sqrt{2Z_0}}; \quad b_1^{(n)} = \frac{V_1^{(n)} - Z_0 I_1^{(n)}}{2\sqrt{2Z_0}}$$

Similar expressions are found for port 2 using subscript 2 in the equations. Here Z_0 is the reference impedance (here Z_0=50Ω for all harmonics), n is the order of the harmonic, and $V^{(n)}$ and $I^{(n)}$ are the complex n'th Fourier coefficients (peak values) of the input voltage and current of the DUT. The goal is to determine these coefficients to obtain the DUT input and output waveforms. The wave variables are normalized so that the power carried by each wave at each frequency is simply $|a_n^{(n)}|^2$ or $|b_n^{(n)}|^2$. At each frequency, the RF properties of both input and output linear coupling networks (directional couplers, cables, connectors etc.) are described by a 3-dimensional scattering matrix consisting of the measured scattering parameters of the coupling network at all harmonics (n) of the frequency. Ideally, the following simplifying assumptions have to be made:

1) The generator and the sampling heads are perfectly matched for all nω of importance making $|a_3^{(n)}|^2 = 0$ for all $n \geq 1$. If this is not the case, the sampling head reflections can be accounted for, if all scattering parameters of the coupling networks are known.
2) The generator harmonic output is negligible. If there are higher harmonics, these can be taken into account by a more elaborate analysis. The distortion can also be reduced by a low-pass coupling network. Under these assumptions we can take $|a_n^{(n)}|^2 = 0$ for $n \geq 1$.
3) The sampling head gain is independent of frequency and its phase response is linear. If the assumption is not valid, the transfer functions of the sampling heads can be included in the scattering properties of the coupling networks.
4) The sampling heads are operated in the linear region. This can be guaranteed by using attenuators in the coupling networks. Non-linearities of the sampling heads distort the incident wave into the DUT and produce higher incident wave harmonics. These can not be easily distinguished from the harmonics produced by the DUT.
5) The input and output bias ports are sufficiently isolated from the RF ports , so that their terminations do not affect the S-parameters of the coupling networks.
6) The load presented by the DUT does not pull the generator output. Sufficient amount of attenuation or an isolator at the generator output may be necessary to ensure this.

7) The DUT is stable under large signal excitation; i.e. it does not sustain oscillations at frequencies other than $n\omega$.The validity of this assumption can be usually checked by a spectrum analyzer at ports 3 and 5. Careful measurements are needed because the oscillation of the DUT may be injection locked to the input frequency, and therefore, the oscillations may not always be visible in the spectrum.

To obtain the DUT input waveforms the periodic voltage $v_3(t)$ at port 3 is measured. Its complex Fourier coefficients are obtained from the measurement results using the discrete Fourier transform (for M samples):

$$V_3^{(n)} = \frac{1}{M}\sum_{m=0}^{M-1} v_3\left(\frac{mT}{M}\right)\exp\left(-\frac{j2\pi nm}{M}\right)$$

Here $T=2\pi/\omega$ is the signal period. Voltage $v_3(t)$ is measured at intervals T/M, $m=2N+1$, where N is the highist order of harmonics considered. The corresponding scattering variables are given by

$$b_3^{(n)} = V_3^{(n)}/\sqrt{2Z_0}$$

The first harmonic complex reflection coefficient of the DUT is defined as the complex ratio of the first harmonic wave amplitudes b and a $\rho=b^{(1)}/a^{(1)} = b/a$ (superscripts omitted) as shown in the simplified scattering flow graph of Fig. 2.

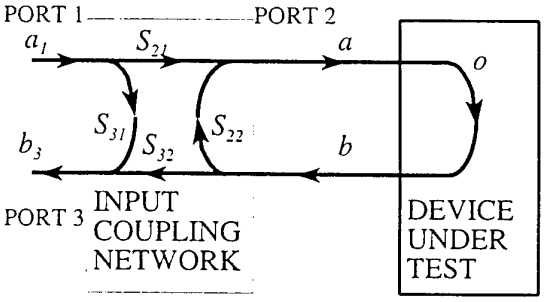

Figure 2 *Fundamental frequency wave variables in the input waveform measurements[1]*

From Figure 2, this reflection coefficient is easily seen to be

$$\rho = \frac{b_3 - S_{31}a_1}{S_{32}S_{21}a_1 + S_{22}(b_3 - S_{31}a_1)}$$

Because b_3 can be measured from port 3, and the scattering coefficients are known from the coupling circuit measurements, the only remaining unknown variable is the incident wave a_1 at port 1. If we now replace the DUT by a known linear calibration reflection coefficient ρ_c and measure the output wave b_{3c}, the unknown incident wave can be obtained as

$$a_1 = \frac{b_{3c}(1 - S_{22}\rho_c)}{S_{31} + (S_{32}S_{21} - S_{22}S_{31})\rho_c}$$

The result shows that the system has to be calibrated using the same generator output power by replacing the DUT with a known reflection coefficient and measuring the corresponding sinusoidal fundamental frequency wave $b_{3c}^{(1)} = b_{3c}$ at port 3. Practical considerations determine which calibration standard is the best (matched load, short circuit etc.).

When the value of the fundamental reflection coefficient ρ is determined, the incident and reflected fundamental waves a and b at the input port of the DUT can easily be shown to be

$$b = \frac{b_3 - S_{31}a_1}{S_{32}}; \quad a = \frac{b}{\rho}$$

Assuming the generator to be free of harmonics, the reflected and incident higher harmonic waves at the DUT input are ($n > 1$)

$$b^{(n)} = \frac{b_3^{(n)}}{S_{32}^{(n)}}; \quad a^{(n)} = S_{22}^{(n)}\, b^{(n)}$$

Finally, all complex voltage and current amplitudes can be determined:

$$V^{(n)} = \sqrt{2Z_0}(a^{(n)} + b^{(n)}); \quad I^{(n)} = \sqrt{\frac{2}{Z_0}}(a^{(n)} - b^{(n)})$$

The total time-domain voltages $v(t)$ and currents $i(t)$ at time points mT/M are obtained by combining the sinusoidal harmonic components.

The output voltages and currents are found by a similar procedure from the measured voltage at port 5 in Fig. 1.

Measurements

A sampling oscilloscope with a bandwidth of 14GHz was used in the measurement system. For N=5 harmonics the highest fundamental frequency would be 2.8GHz. In the present study, the measurement frequency was 0.9GHz. The number of harmonics was taken very high N=56 to avoid aliasing error. Several bipolar UHF power transistors were measured. Typical base voltage and current waveforms are shown in Figures 3 and 4.

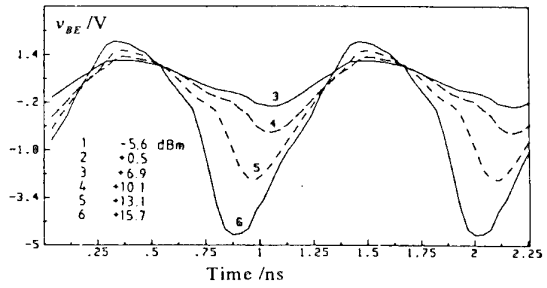

Figure 3 *Base voltage waveform of an UHF bipolar power transistor with input power as a parameter[1].*

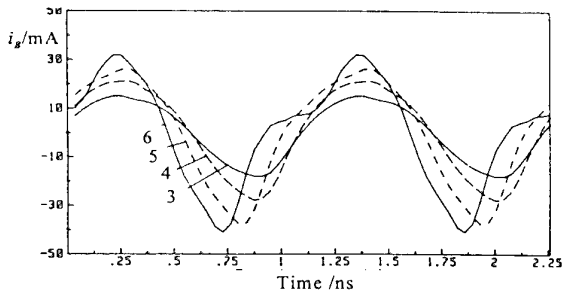

Figure 4 *Base current waveforms for cases 3, 4, 5 and 6 in Fig. 3[1].*

Discussion

The benefit of the non-linear time domain characterization is the information on dispersive dynamics obtained through the amplitudes and phases of the harmonics. A weakness of this measurement system is the limited dynamic range and accuracy of the sampling oscilloscopes, and the complicated nature of the measurement error after Fourier transform calculations. An improved measurement system based on the use of a microwave transition analyzer has been reported by Kompa *et al.*[2]. The time domain measurements improve non-linear transistor modelling if the measurement bandwidth is wide and there is a strong non-linearity giving raise to many strong harmonics.

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VECTOR MEASUREMENT OF HARMONICS IN THE FREQUENCY DOMAIN: WHY, HOW AND WHAT FURTHER ?

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Abstract

Vector measurements of harmonics in the frequency domain were developed about 10 years ago. This paper summarizes some reasons which led to the development of the vector harmonic measurement system, its advantages and drawbacks. Applications of harmonics measurements for device modeling are briefly discussed.

Introduction

Today, measurements of harmonics on nonlinear devices are most often done with systems based on the Microwave Transition Analyzer (MTA) [1]. However, there were and still are reasons to do harmonics measurements with instruments based on the frequency domain.

In this paper, apart from a brief historical review, the following points will be focused more closely:

- WHY do we want to measure harmonics in the frequency domain,
- HOW can these measurements be done,
- WHAT further use can be made of those harmonics measurements.

The last point is of course applicable to all kinds of harmonics measurements, with whatever system they have been made.

Historical Perspective

The question: "What are harmonics measurements useful for?" often stands at the beginning of such measurements. About ten years ago, the goal was to better model the nonlinear characteristics of GaAs MESFETs [2].

The ultimate goal of most RF device models is to have a nonlinear model which is valid over the whole operating region of the device.
For modeling a MESFET, the standard procedure is first making DC parameter measurements, followed by small signal S-parameter measurements at different bias points.
Then one of the available nonlinear models is selected to work with. Popular models include:

- the Curtice quadratic or cubic model [3],
- the Statz model [4],
- "improved" Statz models, e.g. the TOM family of models [5].

After selecting a model, the DC I/V curves are first fit manually to the measured values. The elements of a small signal equivalent circuit model with a similar topology to the nonlinear model are then optimized according to the measured S-parameters, either manually or by a computer program.

What are the drawbacks of this widely used procedure:

- elaborate DC measurements are necessary even if no RF designer is really interested in DC values other than the power consumption of the circuit under normal bias conditions,
- the power dissipation in the device under DC measurements is different from the microwave operating conditions,
- in MESFET or HEMT device models, these DC measurements cause modeling difficulties. Parameters such as the transconductance g_m, the drain source resistance R_{DS} or elements related to substrate effects show marked differences when measured at DC or low kHz frequencies compared with microwave measurements.

Important new approaches such as the Root model [6] were found later to partly overcome the DC characterization problems. Extracting a Root model however needs a lot of measurement points and is therefore time consuming.

A thorough discussion of this modeling problem is beyond the scope of this paper, but the goal of making nonlinear RF device models based on

- a *small number* of
- *RF measurements* only,
- in a RF test environment similar to the final circuit

was one of the reasons to start the work on vector harmonics measurements. The device under test (DUT) mainly considered in the following is therefore a GaAs MESFET.

WHY measure harmonics in the frequency domain?

The idea to do vector harmonics measurements in the frequency domain [7] came up shortly before the MTA was put on sale.
Before that, waveform measurements in the time domain were usually done with oscilloscopes at lower microwave frequencies. The standard setup shown in Fig. 1 was plagued by several deficiencies:

a) low sensitivity because of the large noise bandwidth of the sampling head,
b) unknown phase response of the sampling circuit,
c) trigger jitter resulting in poor accuracy at frequencies above approximately 3 GHz.

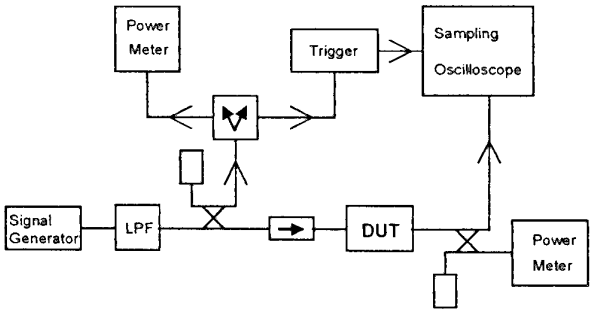

Fig. 1: Waveform measurement system based on a sampling scope

The measurement errors introduced by the linear microwave hardware can be corrected as shown in [8,9].
In contrast, the large noise bandwidth (point a)) is a fundamental problem of all time domain measurement systems. The drawbacks listed under b) and c), however, could later be reduced by better instrumentation such as the MTA [10]. A more detailed comparison of nonlinear device measurement systems in use at the end of the 1980's can be found in [11].
In the waveform measurement system of Fig. 1, Fourier theory tells that there are only components at $n \cdot f_{in}$ ($n = 0,1,2,...$) appearing at the output of the DUT, f_{in} being the input frequency to the DUT (Fig. 2). This is true for any DUT which is not self oscillating.

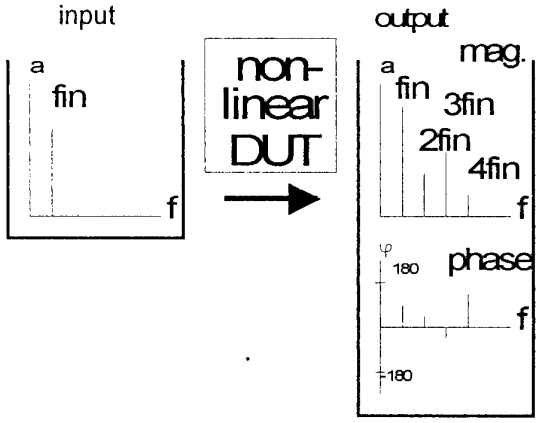

Fig. 2: Principle of measuring harmonics in the frequency domain

To reduce the high broadband noise level, one solution is to measure the harmonics in the frequency domain with a frequency selective instrument. A setup including a standard vector network analyzer (VNA) can be used for this as shown below.

HOW to measure harmonics in the frequency domain?

The vector harmonic measurement system shown in Fig. 3 has been developed between 1986 to 1988 [7].

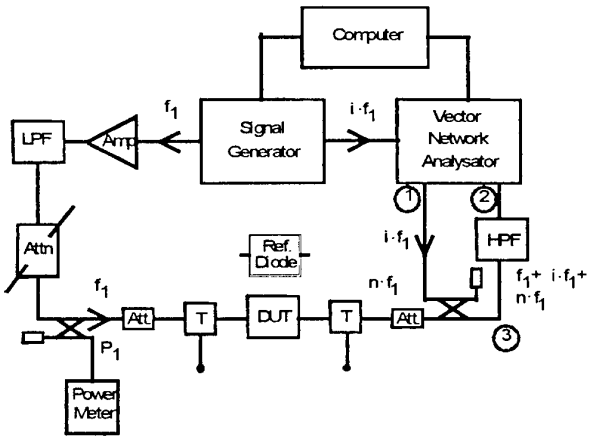

Fig. 3: Setup for measuring magnitude and phase of harmonics ("vector harmonics") in the frequency domain

The key features of this setup are:

- a standard vector network analyzer is used for measuring magnitude and phase of selected harmonics at the output of the DUT,
- it needs a phase-stable reference signal at $n \cdot f_{in}$ in addition to the fundamental signal f_{in} exciting the DUT,
- additional filters can be used to limit the broadband noise and to protect the network analyzer from overload due to a strong fundamental signal,
- the measurement range is limited by the VNA frequency range, the number of reference harmonics available and the bandwidth performance of the phase calibration device.

The system of Fig. 3 gives no a priori relation between the phase of the fundamental signal and the phases of the harmonics.

To fix this relation, a *phase reference circuit* can be used. Such a device should have a much larger bandwidth than the typical DUT. A high-speed Schottky diode proved to be well suited as a reference device [12]. It is an almost ideal limiter, clipping the top of the sine wave and thereby generating a well-defined spectrum of harmonics. The diode used in 1987 was a commercial beam-lead GaAs Schottky diode with a cut-off frequency of 2.5 THz (Marconi DC 1346).
The reference diode is mounted between a 50 Ω through line and ground (Fig. 4).

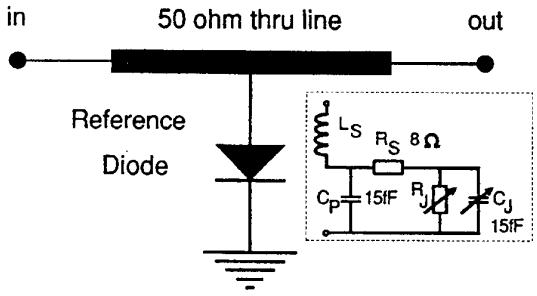

Fig. 4: The reference circuit for phase measurement using a diode with its RF equivalent circuit

Apart from using a diode with very low capacitance and series resistance, the mounting parasitics must be kept to a minimum. For this, the reference circuit was built on 0.254 mm thick Duroid (ε_r = 2.2), mounted in a fixture with K-connectors (Fig. 5).

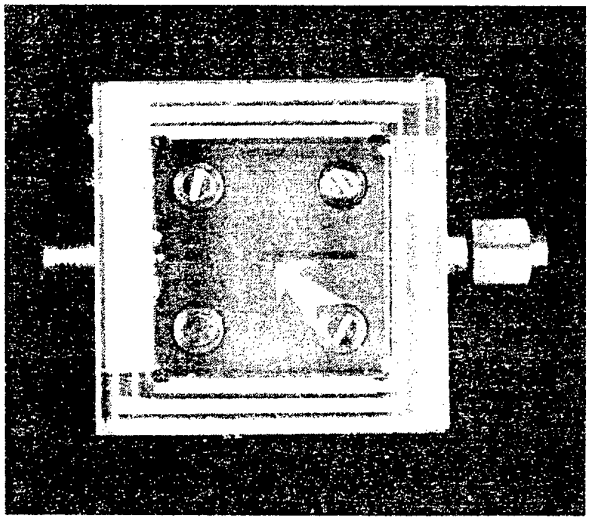

Fig. 5: Photograph of the reference circuit, the arrow points to the beam lead diode (substrate size 2.5 cm x 2.5 cm)

The reference device was simulated with SPICE. The simulation showed that the deviation of the phase from ideal is less than 9° at 15 GHZ and less than 16° for the 4th harmonic at 20 GHz, as shown in Fig. 6. The ideal phase relation at the reference diode can be calculated from the Fourier series of a clipped sine wave [13].

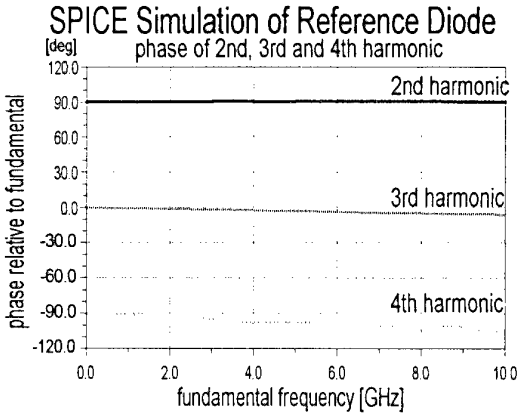

Fig. 6: The simulated phase for the reference diode circuit (Figs. 4 and 5) including mounting parasitics

For the phase calibration, the diode reference circuit is first measured in place of the DUT. Thereafter, the DUT is measured.
Then, using the ideal phase relation, the measured raw phase data are corrected [12]. Furthermore, the differences in length between the reference circuit and the DUT test fixture to be taken into account, too.

When all phase relations are corrected, the time domain waveform at the output of the DUT can be calculated (Fig. 7).

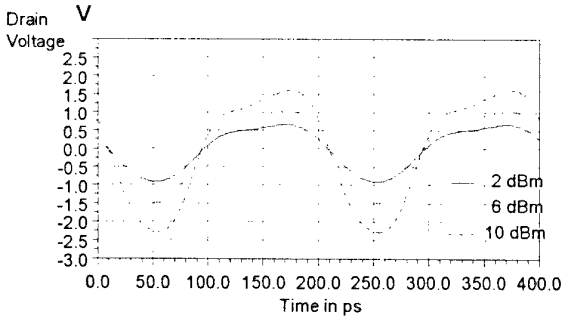

Fig. 7: Drain voltage of a MESFET NE71083 calculated from vector harmonics measurements (f_{in} = 5 GHz, U_D = 3 V, I_D = 5 mA)

Fig. 8 shows a comparison of a magnitude measurement at 15 GHz with a direct power measurement using a power meter and filters.

Further examples of measured results can be found in [2, 12].

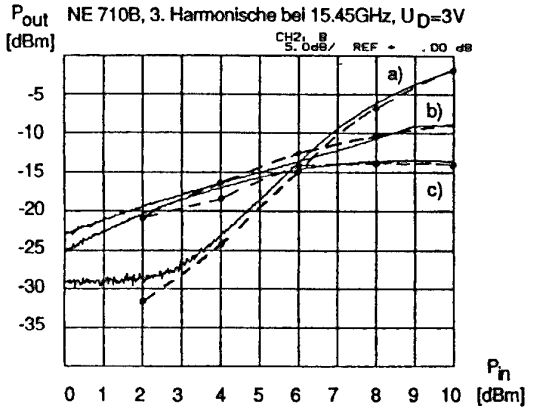

Fig. 8 [2]: Comparison of the magnitude of the 3rd harmonic measured with the vector harmonics system (broken line) and a direct power measurement, DUT: NE71083,
U_D = 3 V, gate bias voltage:
a) 0 V
b) -1 V
c) ≈ - 0.45 V (I_D = 5 mA)

Compared with time domain measurements using an oscilloscope or a MTA, the frequency domain method has the following main advantages:

- higher accuracy for low level harmonics because of the smaller noise bandwidth,
- no trigger jitter,
- no unknown sampling head response,
- higher maximum measurement frequency than the 1980's oscilloscopes. This is no longer true for the MTA.

The disadvantages are, again compared mainly with the MTA:

- more complex measurement setup,
- forward measurements only,
- need for a reference device,
- frequency range and number of measured harmonics is limited and strongly dependent on the equipment.

Finally it should be noted that a reference circuit as shown in Figs. 4 and 5 could be used as a verification device in a time domain waveform measurement system, too.

WHAT can vector harmonics measurements be used for?

When the vector harmonics measurement system was developed, the hope was that it would help in finding a fast and easy way to make nonlinear RF models of active devices.
Partially this goal could be reached by using harmonics measurements for fine-tuning of nonlinear device models. However, DC measurements and small signal S-parameters were still needed in the modeling process.
Thus it is not clear at present if the goal of making a nonlinear device model directly from a small number of RF only measurements can be reached using harmonics measurements.

Other applications for vector harmonics measurements include the characterization of frequency multiplier circuits and high efficiency power amplifier stages.

Conclusions

Vector harmonics measurements in the frequency domain have shown good accuracy compared with direct time domain measurements. However, the measurement setup is considerably more complex than one based on the MTA.

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Harmonics Measurement with a Homodyne Vector Network Analyzer and Potential Novel Applications

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Abstract

For device characterization under large signal excitation the time domain measurement as well as the frequency domain measurement are established and applied meanwhile. A new technique is the application of a homodyne vector network analyzer (hVNA) to this kind of measurement problems. This paper demonstrates the new technique and proposes how to extend the measurement system to measure the tranfer chracteristic of frequency converting devices.

I. Introduction

In the past different approaches were done for device characterization under large signal excitation. A very straight forward technique is sampling the electrical voltage or current of the device response and comparing it to its stimulating signal, i.e. operating in the time domain. This technique is commonly cited as time domain network analysis (TDNA). By extending the operating range of the device under test (DUT) to higher frequencies it is more difficult to achieve accurate measurement results.

Some restrictions to this technique are the lowpass behaviour of such a measurement system, phase stability of the sampling unit and the dynamic range. The resolution in dynamic range of amplitude limits the correctness of the distorted portions of the DUT's output signal. For weak nonlinear responses of the DUT the magnitudes of the harmonics and/or spurious are several 10 dB below the signal of the fundamental frequency. This makes it difficult to separate them.

Further more at higher frequencies the generator and the load of the measurement system are not perfectly impedance matched, as well as the directivity of the couplers connected to input and output ports of the DUT is not infinite.

In addition the bias networks in the system setup can not be longer treated as ideal. So the complete system requires a calibration procedure as used in conventional vector network analyzer measurement techniques, and this must be done for each desired frequency (harmonic/spurious) separately. The system errors are eliminated by transforming the sampled voltage or current

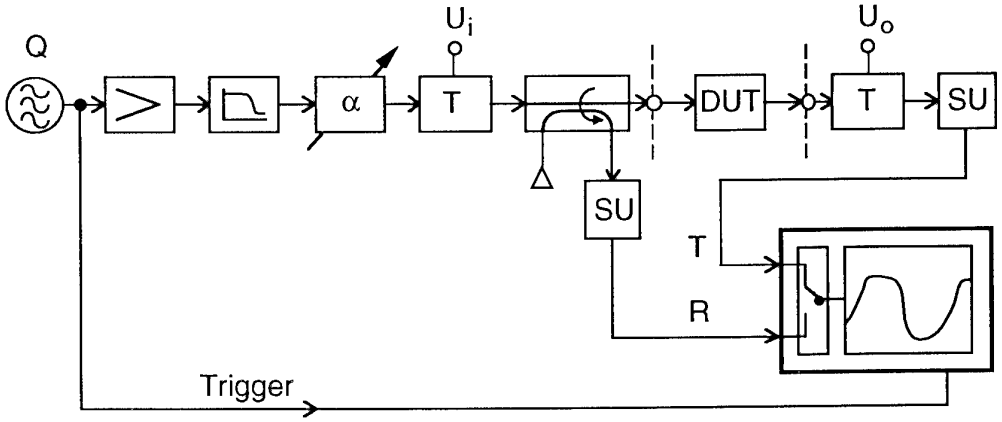

Fig. 1: Time Domain Network Analysis (TDNA) setup with microwave source (Q), bias networks (T), and sampling units (SU)

waveforms into the frequency domain, applying the system error correction and transforming the result back into the time domain. A typical setup of such a system is shown in Fig. 1.

Another method for device characterization with the benefits of higher dynamic range at the frequencies of the harmonics/spurious generated by the DUT is using a system with a homodyne vector network analyzer (hVNA). By this one overcomes the difficulties of signal locking, and triggering the sampling unit. This system is described in the following paper and sketched in Fig. 2.

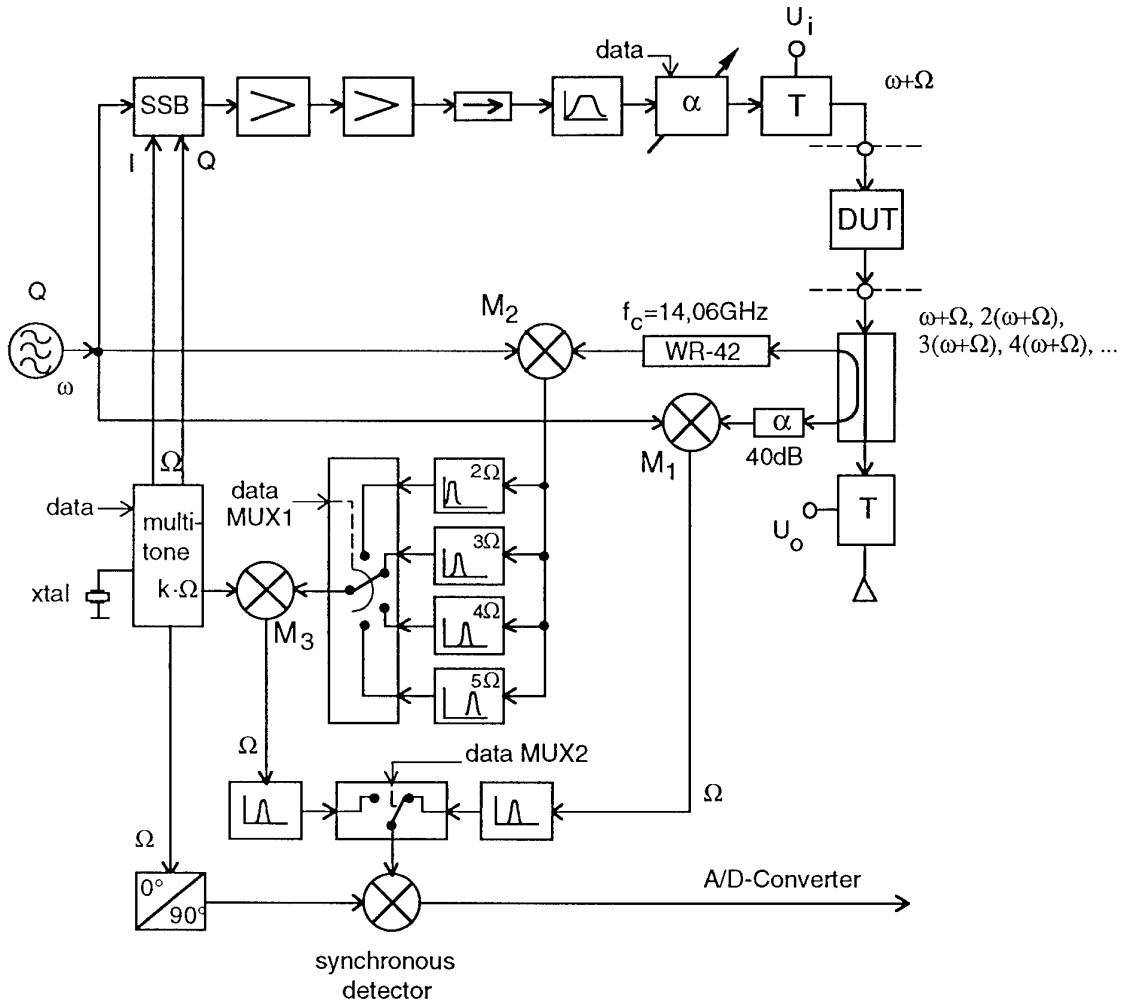

Fig. 2: Frequency Domain Network Analysis (FDNA)

II. The measurement system

The output signal of the single microwave source operating at ω is splitted into two separate pathes. As shown in Fig. 2 the upper signal path feeds a single-sideband-modulator (SSB) which shifts the rf-signal by the amount of the modulation frequency Ω to the output frequency (ω+Ω) (upper sideband). The suppression of the lower sideband and the carrier is better than 40 dB and 20 dB respectively. This modulation technique previously was described in [1] and [2].

A low frequency computer-controlled multi-tone generator acts as a modulation source for the SSB-modulator for the required I and Q input signals. The authors of [3, 4, 1, 5] describe the complete technique of broadband operation of such SSB-modulators.

Now the frequency shifted rf-signal is amplified to the desired highest power level one needs as stimulus for the device under test (DUT). For lower rf-power excitation or power sweeps one can adjust the variable attenuator.

The isolator in the path between removes load dependencies of the power amplifier.

Since the power amplifier itself generates harmonics at $n\cdot(\omega+\Omega)\,|_{n>1}$, these harmonics are blanked out by the inserted bandpass filter.

At the output port of the DUT the full harmonic spectrum generated by the nonlinear device passes a broadband coupling network and is terminated by a broadband microwave load. For load pull measurements this load can be replaced. A small amount of the harmonic signal passes the coupling network and enters the pathes toward the downconverters M_1 and M_2. M_1 is a single balanced mixer and converts the signal at the fundamental frequency of the harmonic spectrum into the intermediate which has the same frequency as the I and Q signals of the SSB-modulator. The adjacent filter and multiplexer MUX_2 as well as the synchronous detector and the applied signal sampling technique are the same as in conventional homodyne vector network analyzers. For proper signal leveling we placed an attenuator in front of M_1.

At input frequencies higher than $(\omega+\Omega)$ the mixer M_1 has a high conversion loss, so this IF represents the DUT output signal at fundamental frequency only. At least any remaining spurious will not pass the following bandpass filter section.

In the second output branch of the coupling network towards the downconverter M_2 the WR-42 rectangular waveguide suppresses the signal at fundamental frequency. Since the desired measurement system operates in the X-band, a cutoff frequency of 14.06 GHz was chosen. Any other kind of highpass filter with a sufficient suppression of the fundamental signal might replace this waveguide section. By means of a harmonic mixer as a downconverter M_2 all higher harmonics $n\cdot(\omega+\Omega)\,|_{n>1}$ appear in the IF as an overlapping spectrum and each carrierer represents both amplitude and phase of the harmonic spectrum of the DUT's output signal. The following table list their relationships, where ω is the pump frequency of the harmonic mixer:

$2\cdot(\omega+\Omega) \rightarrow 2\Omega$ (case 2),
$3\cdot(\omega+\Omega) \rightarrow 3\Omega$ (case 3),
$4\cdot(\omega+\Omega) \rightarrow 4\Omega$ (case 4),
$5\cdot(\omega+\Omega) \rightarrow 5\Omega$ (case 5)

A set of low frequency filters split these carriers and pass them to different input ports of a signal multiplexer. Finally mixer M_3 converts the switched through signal into a second IF with a frequency equal to the frequency of the IF at the output port of mixer M_1 . This requirement is fullfilled when the beat frequency of mixer M_3 is chosen as

3Ω for detecting	2Ω (case 2), or
	4Ω (case 4),
4Ω for detecting	3Ω (case 3), or
	5Ω (case 5).

For investigations of higher degree harmonics the set of filters, multiplexer pathes and beat frequencies for M_3 can be extended easily. Since the detection of 2Ω and 4Ω as well as the combination of 3Ω and 5Ω use the same beat frequency, one has to keep in mind that the synchronous detector samples the complex conjugate values in case 2 and case 3, and that the filter suppression in conjunction to the channel isolation of the multiplexer must be sufficiant high enough.

The beat frequency of mixer M_3 is locked coherent to the modulation signals I and Q of the SSB modulator and by this the phase references of all signals are constant and reproducable inside the complete measurement setup, except of the dependencies of temperature drifts in the rf-sections, as all other mesurement techniques such as the TDNA underlies too.

III. Calibration

For calibrated measurements the overall transfer function of the measurement system has to be determined. The measured voltage at the synchronous detector follows as $M_n = H_n\cdot A_n\,|_{n\geq 1}$, where H_n is the transfer function of the system at the desired harmonic. The phasors A_n are the Fourier components of the output voltage of the nonlinear DUT.

Assuming perfect isolation of the signal switches MUX_1 and MUX_2, sufficient off-band suppression of the bandpass filters, and no crosstalk between the different pathes one can calculate the parameters H_n by normalizing the measures M_n to a known set of A_n. This technique was introduced in [6] and uses the calculated response of a test circuit with a Schottky-diode. For our purpose we calculated the voltage waveform of the calibration device with a computer program based on the harmonic balanced method. A sketch of the test fixture and the calibration device is shown in Fig. 3.

The calbration device is embedded between the reference planes A' and B' and consists of a short microstrip transmission line shunted in the

midth of the length by a Schottky-diode to ground. The carbon films left and right to the reference planes guarantee a broadband impedance matching toward generator and load.

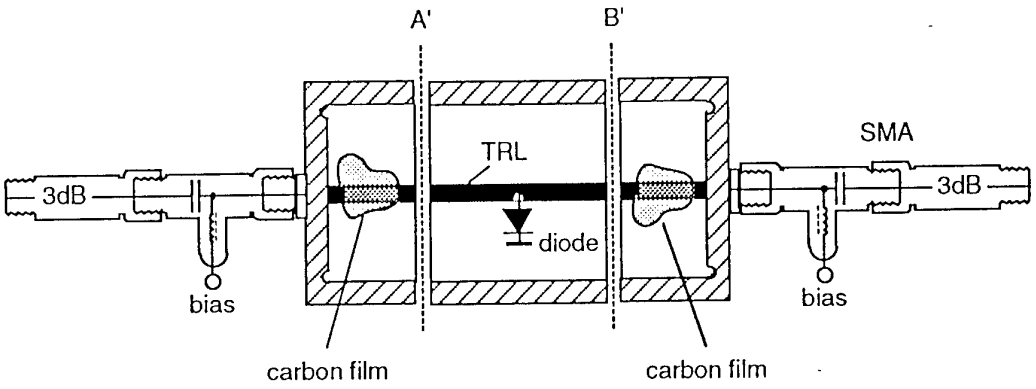

Fig. 3: Sketch of the test fixture with inserted calibration device in between reference planes A' and B'

IV. Measurements

The response of the calibration device at 10.5 GHz (n=1) was measured with a power sweep ranging from approx. -25 dBm to +15 dBm, applied to the input ports of the DUT. For each harmonic the measured data are first normalized to the calculated results at +15 dBm input power and plotted together with a set of data of a computer simulation of the power sweep response.

Figure 4 illustrates a good agreement between calculations (marker '+') and measurements (solid line) of magnitude and phase for n=1 (10.5 GHz) and magnitude for n=2, 3 and 5 (21.0 GHz, 31.5 GHz and 52.5 GHz, respectively).

More at all these measurement results express the high dynamic range the homodyne measurement system covers. The very good agreement between measurement and simulation for n=5 (52.5 GHz) over such a wide dynamic range should be noted.

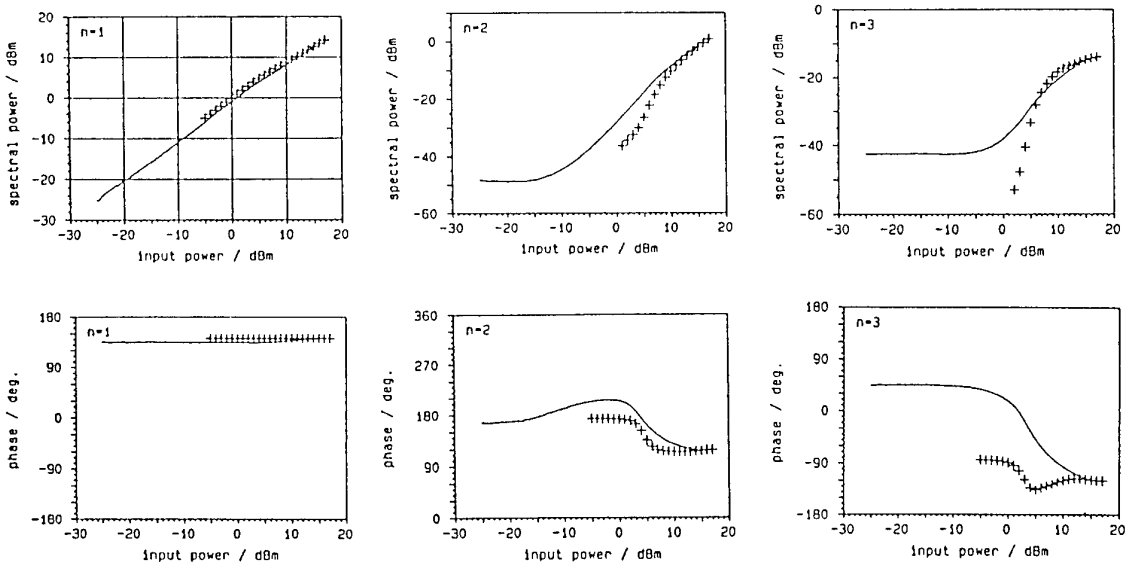

Fig. 4: Plot of measurements and simulation for the calibration device at 10.5 GHz (n=1), ..., 31.5 GHz (n=3)

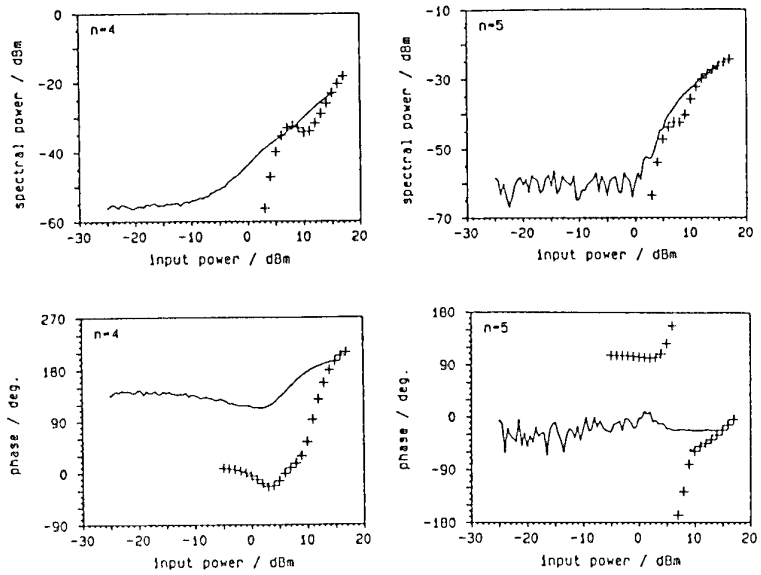

Fig. 4: continued
Plot of measurements and simulation for the calibration device at 42 GHz (n=4) and 52.5 GHz (n=5)

V. Measurement of frequency converting devices

As long as the DUT does not convert the stimulating signal ($\omega+\Omega$) into another frequency band, the detected signal in the IF-channels are a set of multiples of the system frequency Ω. If the DUT itself converts the stimulus to the frequency band $((\omega+\Omega)+\Delta)$ the detected frequency spectrum in the IF-channels appears as $n\cdot(\Omega+\Delta)\,|_{n>1}$. In order to work with an IF frequency of Ω at the output port of downconverter M_3 (see Fig. 2) the pump frequency of this downconverter must be equal to $((n-1)\cdot\Omega+n\cdot\Delta)\,|_{n\geq 1}$ (upper sideband detection) or $((n+1)\cdot\Omega+n\cdot\Delta)\,|_{n\geq 1}$ (lower sideband detection). This requires the flexibility of a programmable output frequency $k\cdot\Omega$ of the multi-tone generator where k is not longer an integer. For $(k\cdot\Omega)$ up to a few megahertz the multi-tone generator described in the appendix fulfills this requirement, when EPROM #3 is replaced by a RAM-device which holds the sampling data of the required voltage waveforms. For different values of k a microcomputer/-controller can calculated the requested data and load them into this RAM previous to the measurement procedure. Furthermore the set of bandpass filters in front of signal switch MUX_3 must be substituted by one electronically adjustable bandpass filter and signal switch MUX_3 is obsolete.

VI. Conclusion

Harmonics measurement of signal waveforms generated by nonlinear microwave devices has been demonstrated. The presented technique uses a homodyne vector network analyzer and it profits from the advantages of homodyne measurement systems compared to other techniques. Such as the necessity of only a single microwave source, the absence of any phase jitter problems and its straight forward and robust implementation makes it to a favourite candidate for the measurement systems in semiconductor production and quality control. Compared to other frequency domain VNA techniques, this measurement system does not need any special requirements of the microwave source, neither additional subharmonics output nor PLL systems or any other kind of sets of synthesized oscillators. The highest detectable harmonic of the investigated spectrum directly depends on the conversion efficiency of the harmonic mixer used in the measurement system. Furthermore the proposed technique to measure frequency converting devices makes the homodyne measurement technique interesting to a wide field of applications.

Appendix

The following section describes the principle function of the multi-tone generator several times

referenced to in this paper. A more detailled explanation was reported in [7].

The basic idea of the signal generator is converting binary data stored in a nonvolatile memory device into an analogue output voltage. If the binary data reperesent a data set of a sinusoid, then a periodically read and conversion

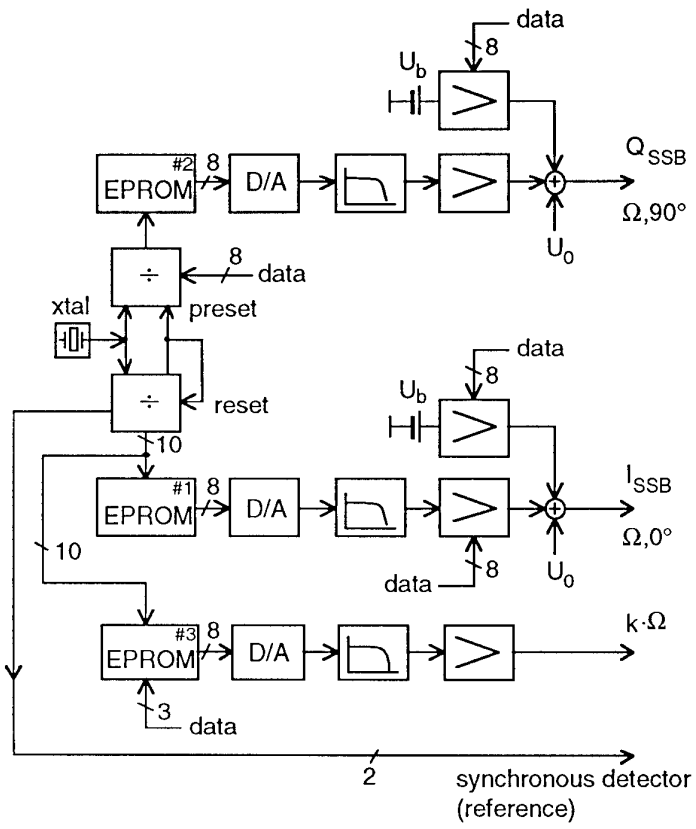

Fig. 5: Overview of the multi-tone generator

of these data into an analogue value results in a sinusoidal voltage function. Its output frequency is the reciprocal of the time period multiplied by the periodicity of the data in the memory device.

As shown in Fig. 5 a binary counter addresses the memory device Eprom #1 and its data output is converted into the analogue output at port I_{SSB}. A special analogue circuit allows the superposition of a DC voltage to this AC waveform.

Most of the circuit blocks of the function generator with the output Q_{SSB} are identical to the circuit blocks of I_{SSB}. Except the binary counter is a preset type and its starting value is loaded whenever the binary counter for Eprom #1 turns around.

This starting value allows a predefined time offset between the roots of the two voltage waveforms, for instance a quarter of the period of the sinusoid.

The third waveform generator in Fig. 5 generates a waveform which is represented by the data set stored in Eprom #3. This memory device is addressed in parallel to Eprom #1 and holds data of a sinusoid with multiples of the frequency of the data sets stored in Eprom #1 and Eprom #2.

Compared to conventional direct digital systems (DDS) this generator allows programming a precise phase offset between the two outputs of Eproms #1 and #2 with any phase number different to 90° and a coherent and reproducable phase coupling between the output waveforms of Eprom #1 and #3.

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Combination of Waveform and Load-Pull Measurements

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Abstract

A new large-signal measurement system combining waveform and load-pull characterization is presented. The setup comprises a double-reflectometer testset and a microwave transition analyzer as fundamental and harmonic receiver. The system calibration can be of TRL or modified SOLT type. This setup permits a complete description of the harmonic amplitude and phase spectra under arbitrary loading conditions of the DUT. Future prospects of the system are highlighted.

Introduction

Modern microwave CAD tools are assisted by highly accurate measurement techniques, which are useful for final circuit design check and verification. The load-pull measurement technique is in use in different modern variations, e.g. active and / or harmonic load-pull [1 - 6]. In the last years, waveform measurement systems were proposed [7,8,9,17], which were used for harmonic amplitude and phase measurement of microwave transistors in a 50Ω environment. Recent systems of this type use a microwave transition analyzer (HP 71500A) as fundamental and harmonic receiver [7, 10]. These systems are capable of a complete characterization of the nonlinear behaviour of active devices, but the one-path two-port setup does not permit reflective load conditions. The motivation to combine the waveform and load-pull concepts can be illustrated by the following practical examples. The first is "waveform tuning", e.g. finding the optimum load conditions of an FET device for fundamental and higher harmonics with respect to maximum output power or best efficiency. The other is the characterization or model verification of power devices for extreme operating conditions such as high-reflective loading, e.g. in conjunction with the investigation of breakdown phenomena which may occur in the case of an ohmic high-impedance load line. Both cases require fundamental and harmonic tuning. Therefore, a "full-two-port" waveform and load-pull measurement system is presented which enables a complete and fully error-corrected characterization of nonlinear devices under arbitrary load conditions.

Hardware Description

Fig. 1 illustrates the block diagram of the measurement setup. The system is based on a 20 GHz synthesizer, a double-reflectometer testset hardware and the microwave transition analyzer (MTA) as receiver. The four reflectometer monitor outputs are multiplexed to the MTA input channels via a simple switch matrix. For optimum hardware performance, both reflectometers are mounted directly on top of the probe arms for on wafer measurements, but in-fixture or coaxial measurements are possible, as well. The synthesizer output is fed to the reflectometers of the DUT test ports via a "source/load module" which is configured in accordance to the actual measurement application. With respect to the MTA and reflectometer specifications, the harmonic frequency limit of the system is 40 GHz. In our present setup, the maximum fundamental input

power to the DUT is about 6 dBm without using amplifiers in the source configuration. With respect to the power capability of the test set components, measurements with RF power levels up to 1 W (CW) are possible. The attenuators in front of the switch MUX protect the receiver channels of the MTA from input overload and ensure their operation in the linear region below -10 dBm. These attenuators can be replaced by step attenuators which are switched simultaneously to make e.g. power sweep measurements over large input power ranges (-10 dBm to +30 dBm) feasible. Fig. 2 shows a photograph of the present realization of the measurement system.

The system is compatible with all common load configurations. For example, the following tuning circuits (fig. 3, see also [12],[13]) may be incorporated into the source/load module: For passive fundamental load-pull, the source signal is fed to reflectometer 1, reflectometer 2 is connected to e.g. a double-srew tuner, or a step attenuator with a variable delay line with a short at the output (fig 3a). Passive harmonic tuning requires filters or more complicated tuner systems. Due to line and reflectometer attenuation, passive tuning is incapable of covering the whole smith chart up to total reflection. This well-known problem is avoided by the active tuning circuits. Two possible realizations of the most common fundamental active tuners are depicted in fig. 3b: "reflection type" and "split-signal type". The latter has a rather good protection against oscillation due to the buffer or power amplifier in the load path towards reflectometer 2, while the reflection loop tends to oscillate in the case of strong reflecting DUTs. An active harmonic load-pull configuration of the split-signal type uses power splitters and frequency multipliers to divide the signal into harmonic branches and variable attenuators and phase shifters for tuning each harmonic [13]. The load signal is built up with power combiners (or e.g. diplexer / triplexer filters for high-power applications).

Source tuning is possible as well. Only the harmonic input loading conditions are of special interest, because any source tuning which leads to actual fundamental wave quantities $a_{1,1}$ and $b_{1,1}$ at the DUT input is equivalent to an ideal source which stimulates the DUT with the input wave $b_{q1}=a_{1,1}$, and both cases lead to the same operating conditions of the DUT. Harmonic source tuning may be achieved with similiar configurations as for load-pull.

Electronic load modules (ELMs) have been realized in the lower GHz range [14] and may be used in the measurement system, as well. This enables fast, electronic tuning without any mechanical parts, which is advantageous e.g. in automatic load-pull contour measurements. We intend to add an ELM to our system as a future development. A possible ELM block diagram is given in fig. 3c. IQ modulators are used for magnitude and phase adjustment, the second harmonic is generated in a push-pull doubler circuit. For an equally-spaced fundamental frequency schedule, a line with an electrical length of an odd multiple of a quarter-wavelength can be used to generate the Q signal for all frequencies of interest. For measurements within any octave band, a 0°/90° 3 dB-hybrid can be used instead. The fundamental and second harmonic signals can be combined with an active circuit or a passive diplexer. The ELM will operate at rather low power levels, the necessary output power can be achieved e.g. with a commercial broadband amplifier.

System Error Model

The error model (fig. 4a) is derived for a generalized hardware configuration. The source and load configuration is described by the virtual stimuli E_1 and E_2 at the reflectometer inputs. Each reflectometer is described by four error parameters e_{ij} and $C_{1,2}$. These 8 terms describe the extension of the 7-term black-box model of a two-port S-parameter (or wave-ratio) measurement system to magnitude and phase spectra measurement. The error model illustrates the MUX signal paths which are necessary for measurement and calibration. It can be shown that the tracking of these paths can be described within the testset and receiver tracking parameters besides the parameter S_{a3T}, which is needed for the return load measurement. The

parameters S_R and S_T are the tracking errors (e.g. the sampling aperture) of the test and reference receiver channels. The system error model is also valid for a four-channel receiver, but then the value of S_{a3T} is 1.

The above-mentioned step attenuators can be installed either in front of the four MUX inputs or directly in front of the MTA input channels. In both cases, the same representation of these attenuators in the error model is valid. Each attenuator is described by a single complex tracking error for each attenuation setting. Assuming that the 0 dB setting of the attenuators is included in the normal system error parameters, we get a maximum of 12 additional tracking parameters for three different attenuator settings (e.g.10, 20 and 30 dB) even in the case of four attenuators or a four-channel system. With remote control of the attenuators, a simple additional single-connection calibration measurement can be performed which yields these parameters (see below).

It should be emphasized that the source and load configurations are independent from the error model. The error model and the system calibration describe only the testset components (reflectometer and MUX) and the receiver channels. Therefore, the source and load configuration can be built up in accordance to actual measurement needs without re-calibration of the system.

Calibration Procedure

The system calibration is based on a TRL or modified SOLT type "full two-port" network analyzer procedure which yields the parameters e_{ij} and the ratio C_1/C_2. For SOLT, the forward and reverse return load ratios a_3/a_0 and a_0/a_3 are included in the "thru" standard measurement. The six measured wave ratios of the "Thru" are converted into the "raw" scattering matrix $[S_{THRU}]$, which has the following relationship to the parameters e_{ij} and C_1,C_2 referring to the error model:

$$[S_{THRU}] = \begin{bmatrix} e_{00} + \frac{e_{01}\, e_{22}}{1 - e_{11}\, e_{22}} & \frac{e_{01}}{1 - e_{11}\, e_{22}} \cdot \frac{C_1}{C_2} \\ \frac{e_{32}}{1 - e_{11}\, e_{22}} \cdot \frac{C_2}{C_1} & e_{33} + \frac{e_{32}\, e_{11}}{1 - e_{11}\, e_{22}} \end{bmatrix} \quad (1)$$

The product $S_{Thru,21} \bullet S_{Thru,12}$ is independent of C_1 and C_2 . This reduces the determination of the parameters e_{ij} to the formula of the THLR in-fixture calibration proposed in [11]. In contrast to the classic SOLT procedure, short and open are unknown reflective standards in this modified algorithm. From short and open measurements, only the ratio e_{32}/e_{01} is calculated. e_{00} and e_{33} are derived directly from sliding-load and / or fixed load measurements, while the remaining parameters are obtained from the "thru" measurement data [11]. We applied this modified SOLT calibration technique in a frequency range from 1 to 40 GHz and achieved a ratio measurement accuracy comparable to that of an HP8510/8516 network analyzer system. Instead of the modified SOLT procedure, any other full-two-port procedure which yields the seven parameters mentioned in step 1 of table 1 is applicable (e.g. TRL, LRM, etc.).

For the present setup, the same additional measurements for coupler tracking, receiver ratio tracking and reference channel sampling aperture are applied as in the "one-path" two-port system described earlier [7]. These measurements are performed on one port only. In comparison to the setup in [7], one additional calibration step is needed which evaluates the MUX tracking path S_{a3T}. With a short standard connected instead of the source E_2, the wave ratios b_3/a_0, b_3/a_3 and a_3/a_0 are measured. This step can be omitted in the case of a four-channel receiver.

To perform the calibration, the source and load configuration is replaced with a coax switch for automatic two-port measurements. Table 1 summarizes this coaxial calibration procedure. The error correction algorithm divides the measured wave spectra by the receiver tracking errors which gives the waves in the reflectometer output plane. The waves in the DUT reference

planes are obtained from a bilinear transform of the reflectometer output waves at each port. With the S-parameters of the wafer probes or the ports of the test fixture known from a THLR calibration [11], the measured wave spectra can be transformed to the on-wafer or microstrip DUT reference planes.

The two-step procedure is advantageous for in-fixture measurements. For on-wafer measurements, a one-step calibration method has been defined. Because of the lack of an on-wafer power standard and a planar receiver input reference plane, a simple coaxial one-port SOL and receiver and coupler tracking calibration procedure is added to an usual two-port on-wafer calibration routine which yields the error terms e_{ij} and the coupler tracking ratio C_1/C_2. The sequence (table 2) is as follows: At first, a coaxial one-port (SOL) calibration is performed at the test port 1. A sliding load is not necessary, because the coaxial reference plane is established only for the subsequent directional coupler and receiver tracking measurements, which are identical to the steps 2,3, and 4 of table 1. Next, an on-wafer full-two-port calibration is performed (modified SOLT, TRL, LRM etc. are feasible). For our two-channel receiver configuration, the on-wafer "thru" measurement is repeated with a short connected to the output of the reflectometer at port 2, to evaluate the MUX tracking error S_{a3T}.

The evaluation of the error terms from the one-step calibration procedure is as follows: Fig. 4b depicts two equivalent descriptions of the error model of port 1 with the on-wafer and the coaxial reference plane. The quantities e_{ij} and C_1 are the coaxial error terms and the dashed quantities e'_{ij} and C'_1 are the on-wafer ones and the S_{ij} are the S-parameters of the wafer probe at port 1. The e'_{ij} terms and the ratio of the coupler tracking errors in the on-wafer reference plane, C'_1/C'_2, are obtained from the planar two-port calibration. The coaxial one-port and receiver tracking calibration yields the e_{ij} values and C_1 and $|S_R|$ and the receiver ratio tracking S_T/S_R. For both error models in fig. 4b, the bilinear transform of the waves a_p, b_p to a_0, b_0 can be written. A comparison of the 4 coefficients of both formulations of this transform results in simultaneous equations for S_{ij} and C'_1 with e_{ij}, e'_{ij} and C_1 already known. These equations can be rearranged to a set of formulae which gives C'_1. For direct error correction to the on-wafer reference planes, the parameters e'_{ij} and C'_1/C'_2 and S_T/S_R and $|S_R|$, $|S_T|$ and S_{a3T} are used.

If the optional step attenuators are used, an additional calibration step is required to evaluate the corresponding tracking errors which have been defined in the error model section. This procedure is defined as follows: With the (coaxial or on-wafer) "thru" calibration standard connected, a forward transmission measurement (wave ratio b_3/a_0) is performed. At a 0 dB setting of the attenuator in the a_0 (reference wave) signal path, complex ratio measurement values are taken for all non-zero settings of the attenuator in the b_3 (transmitted wave) signal path, and vice versa. If four attenuators in front of the MUX are installed or if a four-channel receiver is implemented, a reverse transmission measurement (wave ratio b_0/a_3) is carried out for the same attenuator settings in the reverse measurement paths. All calibration steps - including the attenuator tracking calibration - can be performed with a broadband microwave synthesized source with only a few mW output power. For measurements, the source and load configuration can be changed to incorporate a high-power source or amplifiers operating within the frequency range of interest.

Load-Pull Measurement Software

An example of a state-of-the art load-pull-hardware and software is described in [15]. In our case, the most interesting feature is "waveform tuning". A highly flexible load-pull software subsystem is being developed as a part of the measurement and calibration system software. Load-pull and/or source-pull of the fundamental and harmonics is feasible according to the setting of a formal tuner vector. The actual tuner Hardware configuration affects only the tuner control subroutine and the setting of the tuner hardware parameters at the startup of the load-pull routine. Adaption to different tuner hardware is rather simple. Two arbitrary, formal step sweep parameters and a variable definition

of the desired DUT operating conditions in the "load-pull goal" subroutine enable e.g. the scanning of the load reflection plane or the tracing of load-pull contours and waveform tuning. The software is organized in five hierarchical levels (fig. 5). The sequential schematic (fig. 6) illustrates the main manual and automatic tuning and measurement procedures which are supported.

Application Example

The system was realized in an entire-automatic, computer-controlled setup. As a demonstration of fundamental load-pull, power sweep measurements on a 0.3 µm PHEMT power device with double-recess asymmetric gate (which was manufactured by the Fraunhofer-Institute for Applied Solid-State Physics, Freiburg) were performed at 10 GHz with a passive load tuner adjusted towards optimum effective fundamental output power and to approximately 50 Ω load. The input drive level (up to 25 dBm at 10 GHz) was maintained with a commercial power amplifier between the RF source and the reflectometer input port. The RF power at the DUT's on-wafer input reference plane is precisely adjusted by means of a software leveling loop. In figs. 7 and 8, the time-domain waveforms and trajectories at input and output are displayed for several input power levels and both afore-mentioned operating conditions. These error-corrected data refer to the on-wafer device reference planes.

In the tuned condition, the effective fundamental output power of the device is going towards 1W/mm at 10 GHz input frequency. It can be seen from the Id(Vds) trajectory that the 50 Ω load line doesn't result in the optimum drain voltage swing. The load trajectory is not an ideal line because of the reflections within the port 2 reflectometer, especially for the higher harmonics. Of course, harmonic tuning would be required to remove this reflections. While the 50 Ω load line reaches up to Vds=15 V, a maximum voltage of 20 V is observed for the tuned operation. The blow-up of the trajectory describes the reactance which compensates the output parasitics of the device. In addition, this reactance explains the negative instantaneous drain currents which occur when the device is pinched off by the gate voltage swing. For the 50 Ω load condition, the current swing stops at the zero current line. The input Ig(Vgs) trajectories illustrate the gate charging current (or the nonlinear gate-source capacitance) and the gate-source diode characteristic. The gate voltage range of the "tuned" measurement is larger than in the 50 Ω load case because a higher RF input power was applied (25 dBm instead of 22 dBm). In both cases, no breakdown effects are visible. If breakdown would occur, it is expected that e.g. the minimum momentary value of the drain current at device pinch-off increases for the highest power levels and / or the instantaneous gate current value at the negative Vgs peak becomes negative. It seems that breakdown is more critical at lower operating frequencies, because in that case the maximum of Vds coincides with the negative peak of Vgs, resulting in a high peak in the gate-drain voltage which may cause breakdown. For comparison, such a drain-gate breakdown operating condition is illustrated in fig. 9, showing the input (Ig vs. Vgs) and transfer (Id vs. Vgs) trajectories of an in-fixture measurement of a medium power MESFET chip (Toshiba JS 8836) within a 50 Ω environment at 1.5 GHz for different input power levels.

Future Developments

With respect to modern millimeter wave active devices, a frequency extension of the measurement system is of great interest (e.g. up to about 100 GHz). This requires sampling receivers (harmonic mixers) and reflectometers with good performance and low insertion loss with frequency coverage from the lower GHz range (e.g. X-Band) to the millimeter wave range (e.g. up to 100 GHz). This could be combined with a frequency-domain processing and evaluation of the IF signal as proposed in [16], which leads to an increased dynamic range without averaging. The harmonic phase calibration of the sampling receiver is expected to become more critical in the millimeter wave

range. Concepts for harmonic phase calibration are described in [17,8], but must be adapted to the millimeter wave range.

For the characterization of high power devices and circuits, e.g. in the frequency range up to 20 GHz for mobile and satellite applications, an extension to higher power levels above 1W is of interest, especially in combination with pulsed-RF or two-tone test (intermodulation measurement) capabilities. For pulsed RF, the receiver capabilities (e.g. dynamic range) are the critical point, while for two-tone setups a repeatable snchronization of the sources must be achieved.

Regarding the load-pull feature of the measurement system, electronic load modules (ELMs, e.g. [14]) are promising for automatic harmonic load- or source-pull optimization, as has been discussed above. ELMs should be investigated for higher frequencies.

Conclusion

A double-reflectometer large-signal waveform measurement system which can be used for various load-pull applications was presented. The system was realized with 40 GHz hardware components. The combination of waveform measurement and the load-pull concept leads to a complete description of the nonlinear harmonic behaviour of active two-port devices for arbitrary load conditions. The measurement accuracy is assured by a "full-two-port" calibration procedure and is comparable to vector network measurements. Further work will concentrate on the extension of the frequency range, adding pulsed-RF and IM measurement capablities, the expansion to higher power levels and the investigation of electronic source/load modules.

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Step #	Description	Extracted Parameters
1	Full-Two-Port Sequence (TRL or modified SOLT) Complex Ratio Measurement	**e00,e01,e11, e22,e32,e33** **C1/C2**
2	Short at testport 1 with interchanged RX Channels Complex Ratio Measurement	Receiver Ratio Tracking
3	Test-RX connected to Testport 1 Complex Ratio Measurement	Coupler Tracking C1
4	Power Meter at Testport 1 Reference Channel Amplitude Measurement	Sampling Aperture S_R
5	Thru Connection with Short as Forward Return Load Complex Ratio of b3/a0, b3/a3, a3/a0 (can be omitted for 4-channel Receiver)	MUX Tracking Coefficient S_{a3T}

Tab. 1: Coaxial Calibration Sequence

Step #	Description	Extracted Parameters
1	**Coaxial** One-Port SOL-Sequence (Short, Open, Fixed Load) Complex Ratio Measurement	**e00,e01,e11**
2	Short at testport 1 with interchanged RX Channels Complex Ratio Measurement	Receiver Ratio Tracking
3	Test-RX connected to Testport 1 Complex Ratio Measurement	Coupler Tracking C1
4	Power Meter at Testport 1 Reference Channel Amplitude Measurement	Sampling Aperture S_R
5	**"On-wafer"**-Full-Two-Port Sequence (LRM, TRL or modified SOLT) Complex Ratio Measurement	**e'00,e'01,e'11, e'22,e'32,e'33** **C'1/C'2**
6	**"on-wafer"**-Thru Connection with Short as Forward Return Load Complex Ratio of b3/a0, b3/a3, a3/a0 (can be omitted for 4-channel Receiver)	MUX Tracking Coefficient S_{a3T}

Tab. 2: On-wafer One-Step Calibration Sequence

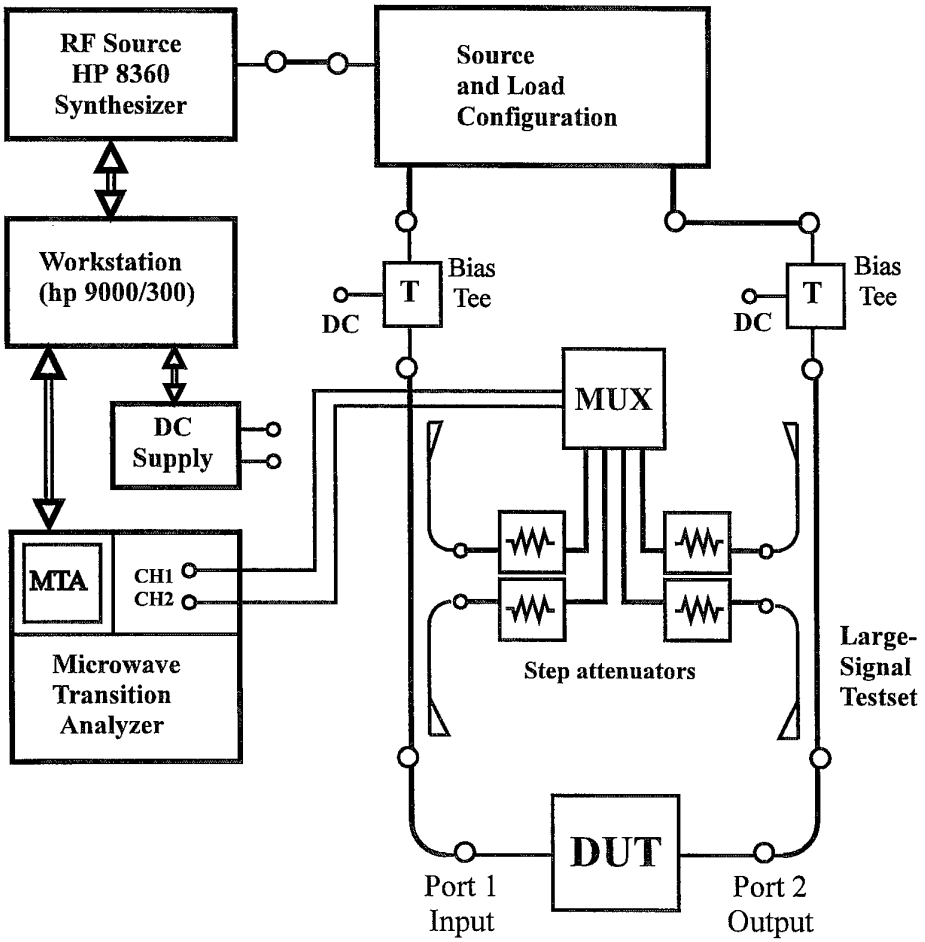

Fig. 1: Block diagram of the measurement setup.

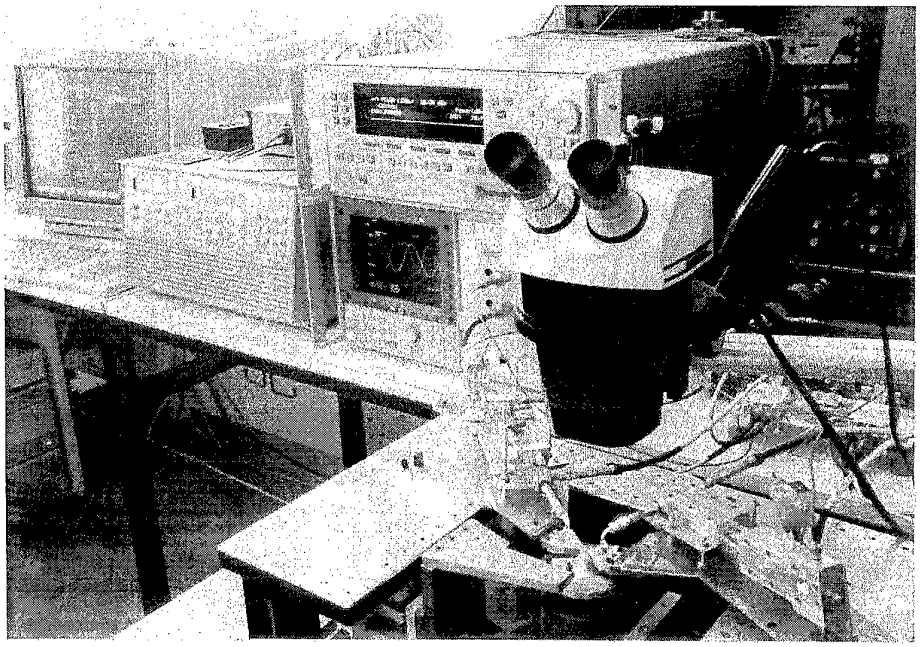

Fig. 2: Photograph of the measurement setup.

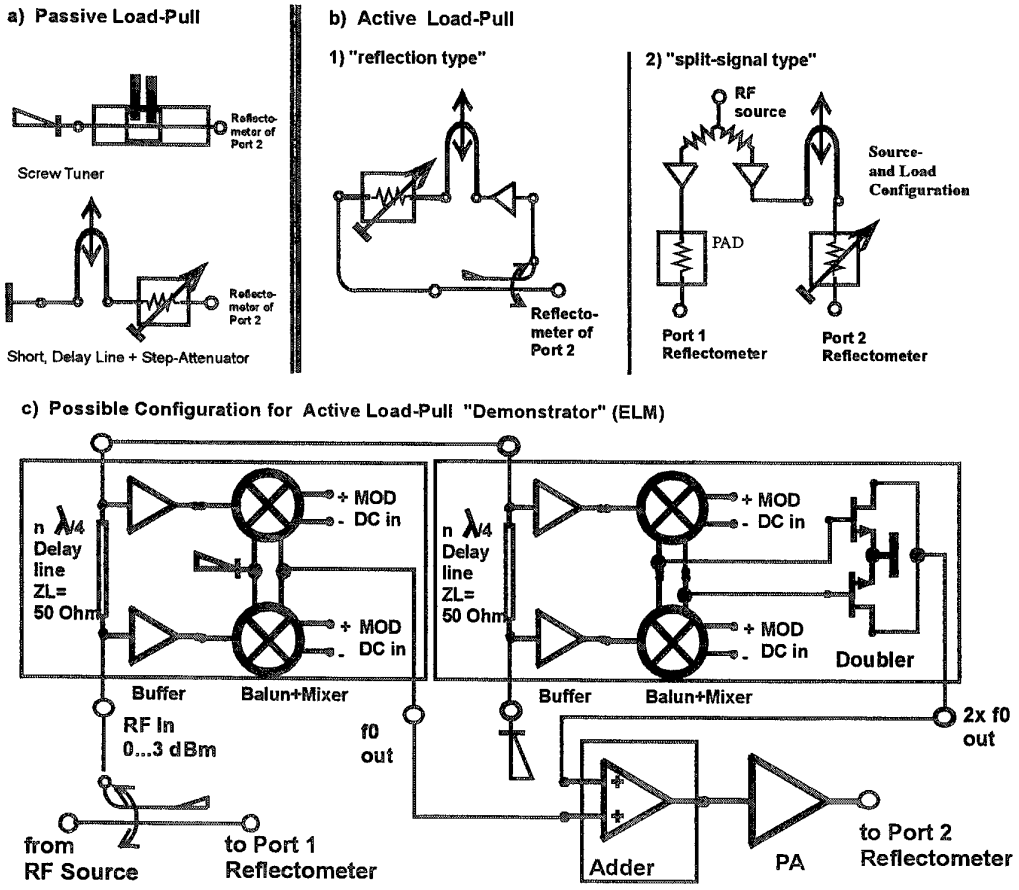

Fig. 3: Load configuration examples

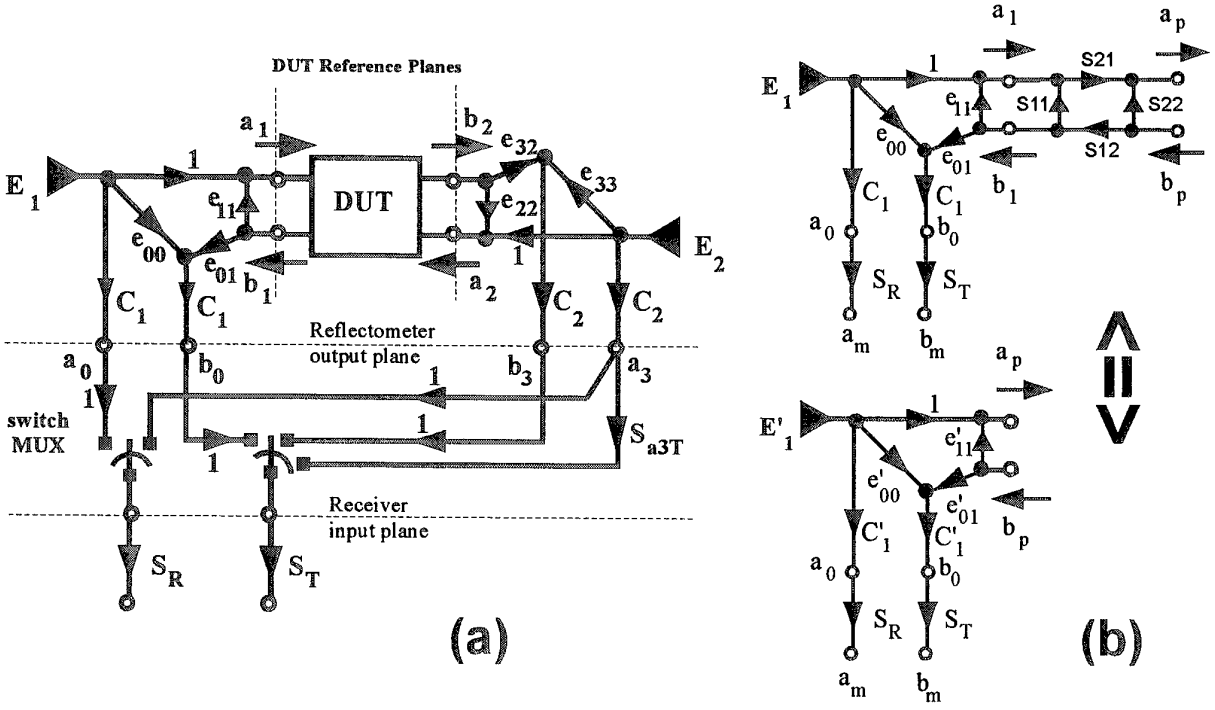

Fig. 4: a) Error model of the measurement system
b) Coaxial and on-wafer error term definition for port 1

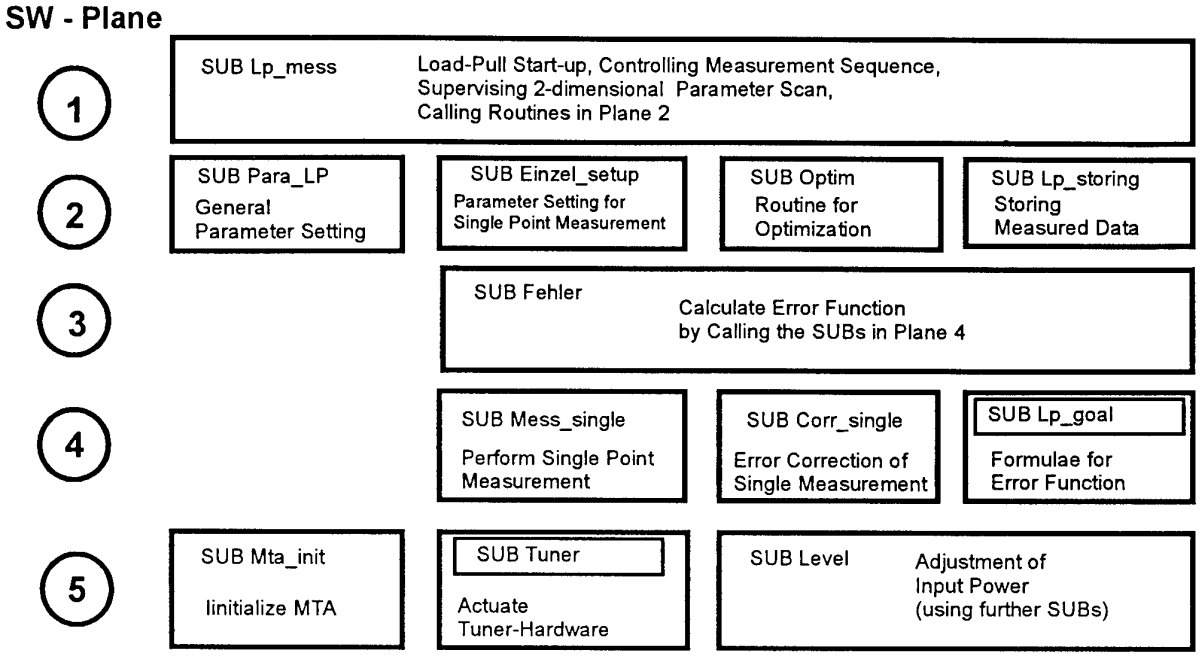

Fig. 5: Load-pull software: Structure diagram

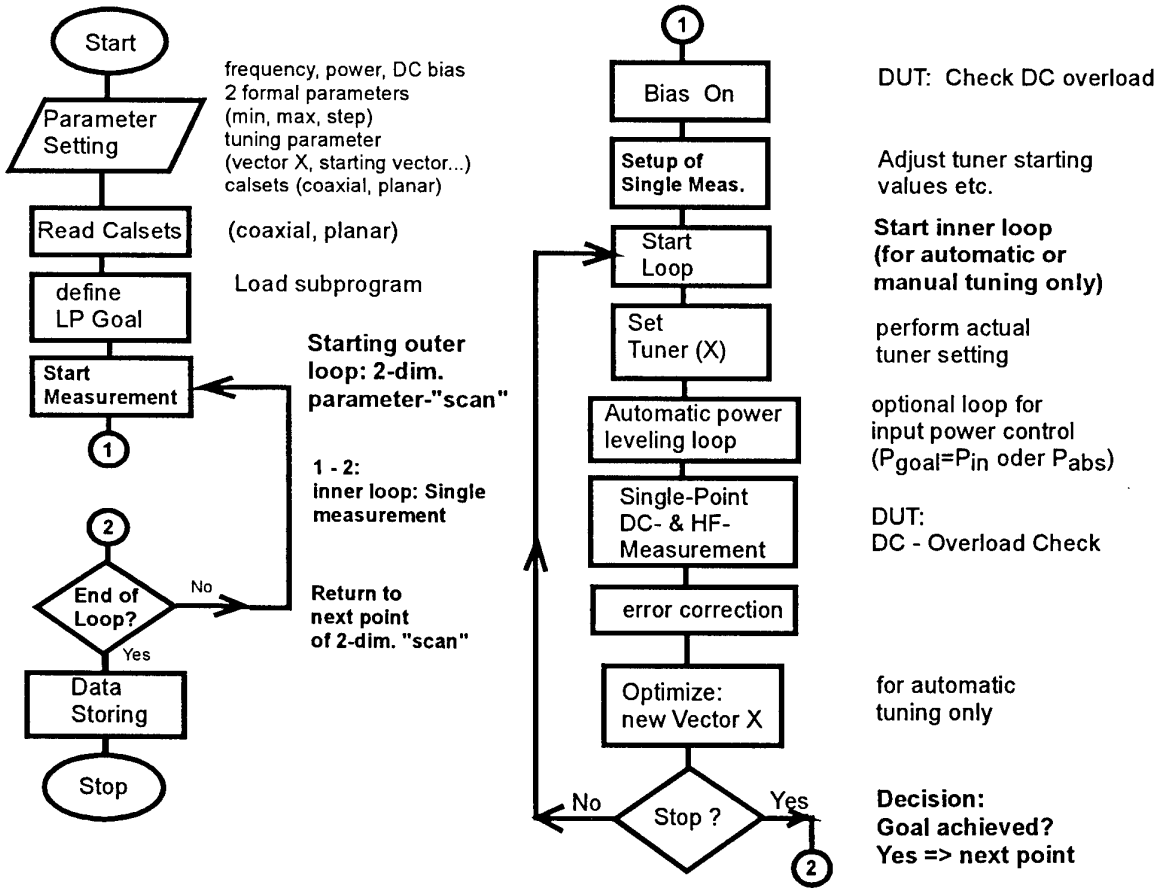

Fig. 5: Load-pull software: Sequential schematic

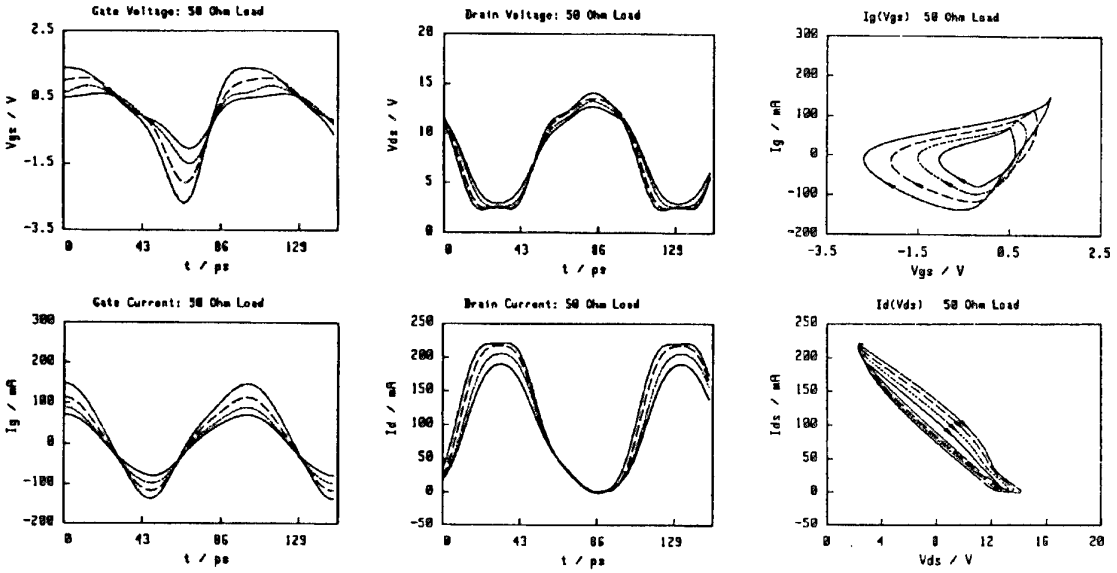

Fig. 7: Input and load trajectories and voltage and current waveforms of 0.3 µm PHEMT with 50 Ω loading at 10 GHz and 16, 18, 20 and 22 dBm input power. DC bias point: V_{GS}=0.0 V, V_{DS}=8.6 V.

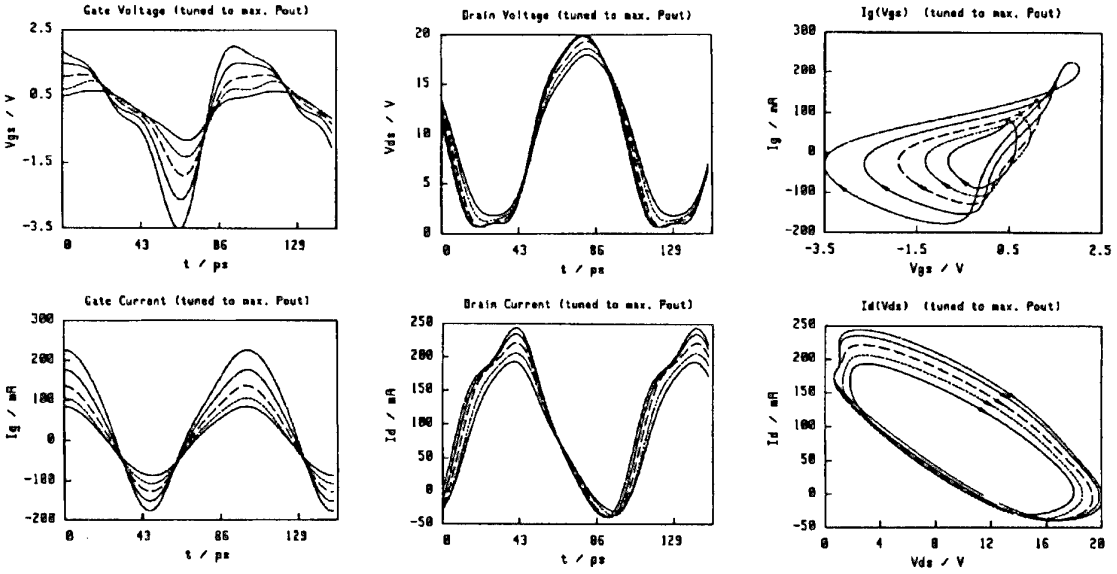

Fig. 8: Input and load trajectories and voltage and current waveforms of 0.3 µm PHEMT tuned to max. output power at 10 GHz and 17, 19, 21, 23 and 25 dBm. DC bias point: V_{GS}=0.09V, V_{DS}=10V.

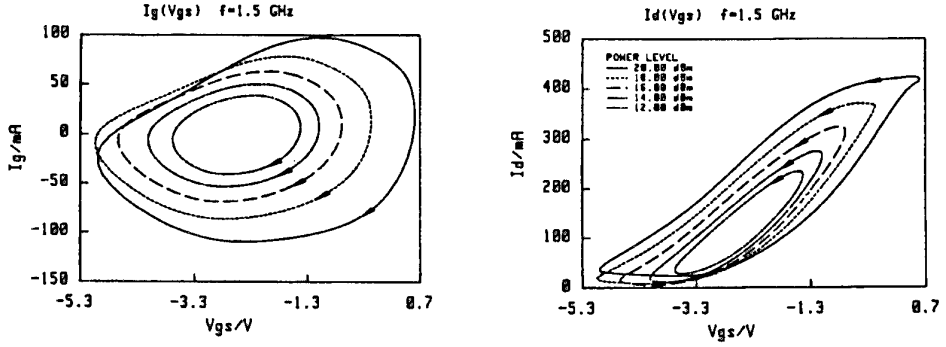

Fig. 9: Input and transfer trajectories of a Toshiba JS8836 medium power MESFET chip at 1.5 GHz and 12, 14, 16, 18, and 20 dBm input.

A COMPLETE, MEASUREMENT BASED,METHODOLOGY FOR THE EXTRACTION AND VERIFICATION OF NONLINEAR MODELS OF ACTIVE DEVICES

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1- Introduction

The availability of reliable NonLinear (NL), large signal models of active devices is one of the major challenge of the nonlinear CAD of microwave and RF circuits. Indeed, circuit performance prediction is highly dependent on the quality of the NL models. So during the last few years a considerable attention has been paid to the development of new models as well as new characterization techniques.

Those new models are either Physics Based (PB) [1],[2], Equivalent Circuit (EC) [3] or blackbox (BB) [4],[5] models. All these models rely on a number of assumptions and are established through a reduced set of data. Those data are obtained either from device physics and geometry or from measurements performed on sample devices. This has implied the development of new measurement techniques in order to overcome the problems linked with behaviors of devices such as self heating, frequency dispersion due to trapping effects or non quasi static effects encountered at higher frequencies.

Classical measurements techniques are based upon DC current voltage (I-V) characterization combined with multibias [S] parameters measurements. More recently, pulsed [6],[7],[8] and large signal [9],[10],[11] , characterization techniques have allowed to overcome the main drawbacks of DC measurements. All those techniques are actually well known and have been widely reported in the litterature. NL models can be extracted from those measurements using optimization algorithms or direct extraction techniques

The reliability of the models obtained has to be checked so that they provide accurate results when included into CAD software. This is the model verification step of the modelling process. This is often the weak point of the models proposed. Indeed model verification requires, on one hand to reproduce the measurements performed to extract the model and on the other hand to be consistent with large signal measurements in the presence of arbitrary input signals. This latter condition implies the development of new large signal characterization methods. For power applications those methods are essentially based upon load pull measurements either in the frequency domain or in the time domain.

The whole NL modeling process of active devices is summarized in fig-1 where the verification of the model appears as a final fundamental step. The aim of this paper is to present the main requirements for models characterization and extraction as awell as for an in depth model verification. This verification includes DC I-V curves and S-parameters checking, low frequency and high frequency derivatives of nonlinearities consistency checking,.and large signal measurements checking. Those latter measurements are based on a one-tone or multitone multiharmonic load pull measurement system.

In section 2 a review of measurement based models will be given while in section three the model verification process will be described.

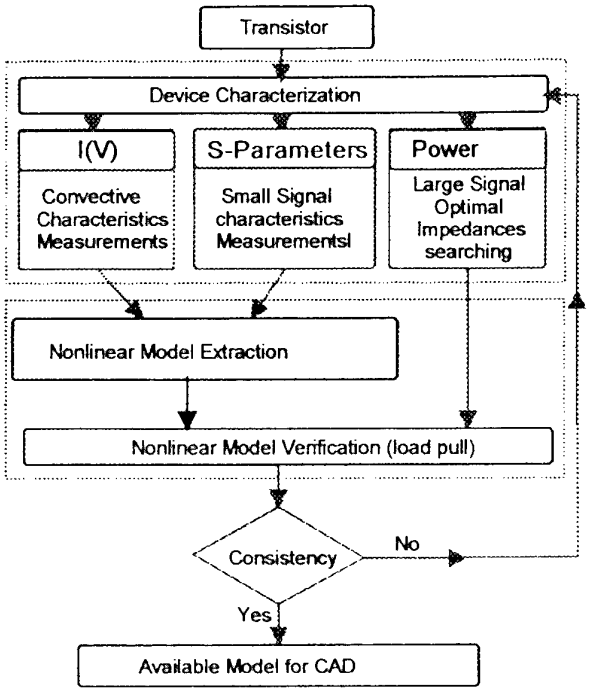


Fig-1: Summary of the whole modeling process

2- Measurement based models

2-1 Measurement set-up

Microwave devices exhibit a number of uncontrolled effects when measured under DC conditions. Those effects are mainly due to self heating and traps for FET devices. Self heating effects are present in all power devices while trapping effects mainly affect FET behavior. A well tried method to keep temperature and traps effects under control during the measuring of power devices is to perform pulsed measurements.

The principle of the technique is illustrated in fig-2. Shorts pulses arising from a DC quiescent state, are applied to both ports of the device. Input and output currents and voltages and S-parameters are simultaneously measured in the whole working range of the device. As the duration of the pulses is much lower than the thermal and traps time constants, the thermal state as well as the trapping state of the transistor are fixed by the quiescent bias point. This point can also be adjusted in order to extract thermal behavior of the device. In fig 3-a and 3-b the comparison between DC measurements and pulsed measurements of a PHEMT and a Si BJT transistors are shown respectively.

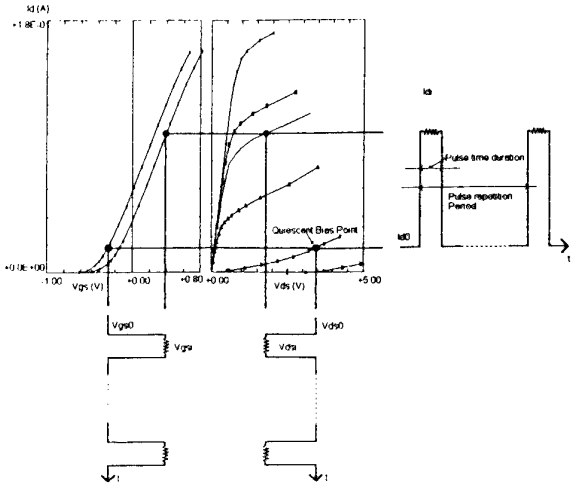


Fig-2 Principle of pulsed measurements.

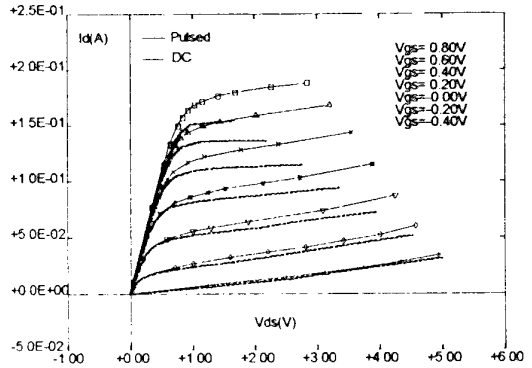


Fig 3-a I-V Characteristics of a 4x75x0.25µm² PHEMT

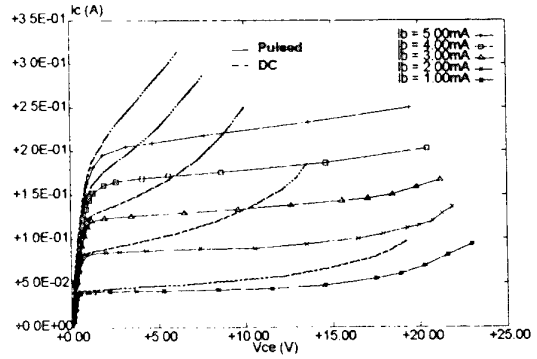


Fig 3-b I-V Characteristics of a Si BJT Transistor

2-2 Model topologies and extraction.

In the EC circuit modeling approach, once the measurements have been performed, nonlinear elements must be extracted for a chosen model

topology. The choice of this topology is crucial for the model accuracy as it determines the ability of the model to take into account parasitics effects or Non quasi static effects. Classical model topologies of FET devices and Bipolar devices are shown in fig 4 and fig-5. After the determination of parasitic access elements that are supposed to be bias independent, the extraction of nonlinear elements can be made either from optimization routines [12] or by direct extraction[13]. Moreover mathematical representation of nonlinear elements can be made by analytical functions or by look-up tables [14],[15] Finally the NL model has to be implemented in a CAD software.

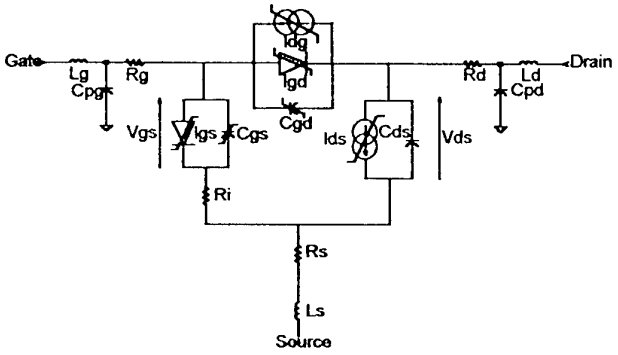


Fig-4 FET classical Equivalent circuit

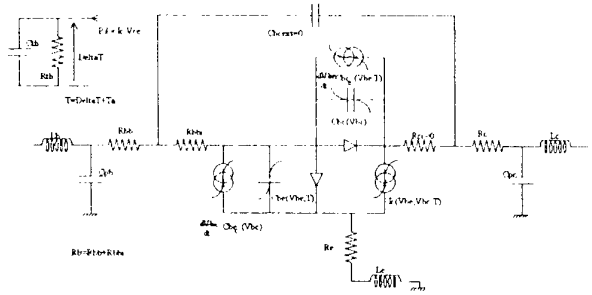


Fig-5 Model topology of a microwave Bipolar transistor (HBT).

2-3 Electrothermal model

Device temperature has to be known for reliable designs of microwave circuits. This implies the availability of an electrothermal model. In this model the device temperature appears as a third independent variable. In order to fully characterize the device two kinds of data must be taken from measurements : electrical data at a set of various temperatures, and thermal data concerning the thermal flow in the device. Among various microwave devices HBT are known to be very sensitive to thermal phenomena, so the electrothermal model extraction will be given for a 240µm² GaInP/GaAs HBT processed at Thomson LCR..

At first a set of isothermal characteristics as shown in fig-6 is measured for various temperatures. Measurements include I(V) and S parameters so a complete nonlinear model can be extracted at each temperature. This allows to take into account the variations of the non linear parameters versus the device temperature.

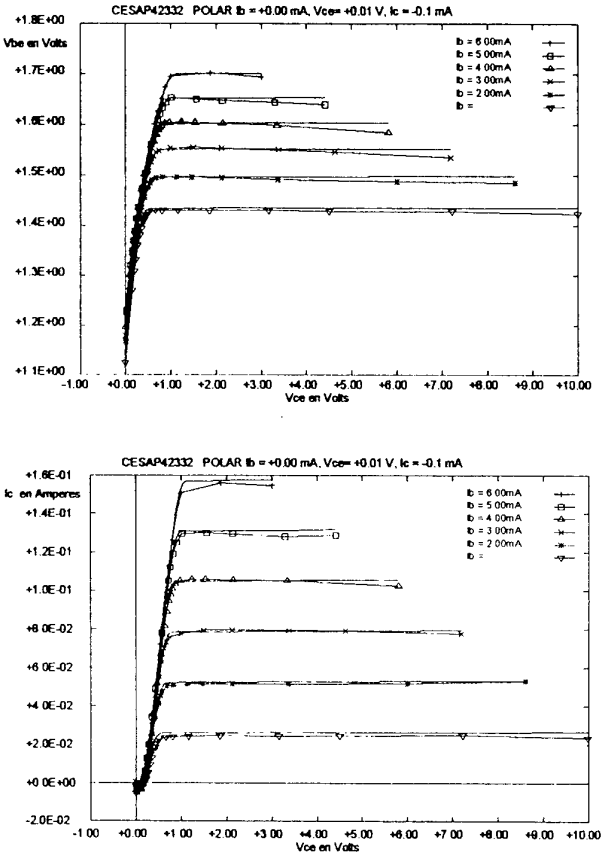


Fig-6 Isothermal 240µm² GaInP/GaAs HBT Input and output characteristics

An example of the thermal modelling of the base-emitter capacitance is given in fig-7. Isothermal nonlinear variations of the C_{BE} capacitance are given for various temperatures. Those temperatures are fixed either by DC biasing the device either by putting it in a thermal enclosure. A representation of the capacitance extracted from DC-bias S-parameters measurements is also given on the fig-6, where the wild variations of this element versus V_{BE}.appear. This is due to the fact that the device temperature changes during the measurement process. I

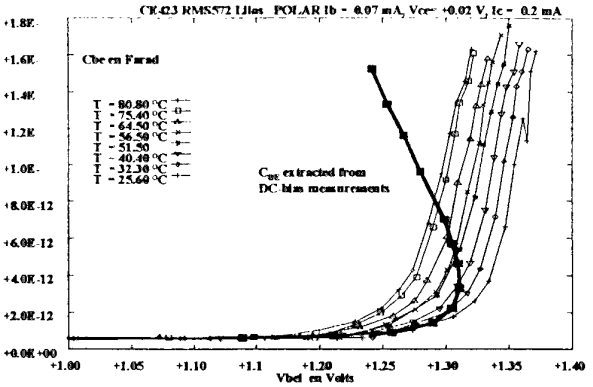


Fig-7 Isothermal and DC-Bias variation of the Base-Emitter capacitance.

In order to complete the isothermal model the thermal characteristics of the device must be measured. The simplest representation of the thermal behavior can be represented by a thermal resistance and capacitance. To determine the thermal resistance the collector current is measured under isothermal conditions and in DC conditions for a constant V_{CE} bias voltage. Then the DC characteristic is superimposed on isothermal characteristics as shown in fig-8. The intersections of these characteristics allow to derive a temperature elevation versus dissipated power curve. Thus the nonlinear thermal resistance is obtained.

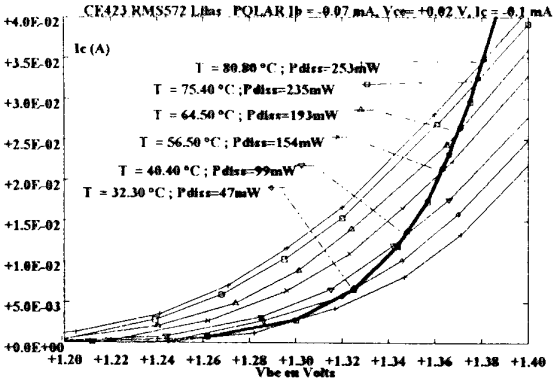


Fig-8 R_{th} determination from isothermal and DC measurements.

It should be noticed that the same approach can be applied to FET devices provided the trapping effects are fully controlled.

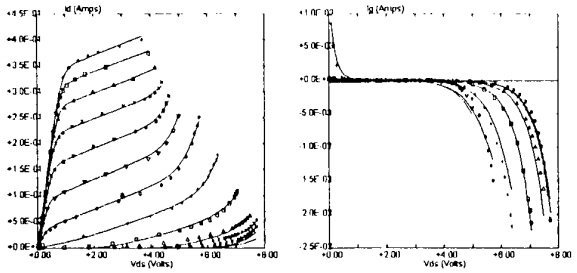
3- Model verification

The verification of the model must include several types of simulations and measurements. First of all I-V and [S]-parameters must be checked by simulating the S-parameters with the NL model. After that a number of large signal measurements must be performed in order to investigate the behavior of the device in a configuration that has not be used for the extraction of the model.

3-1 I-V and small signal Verification

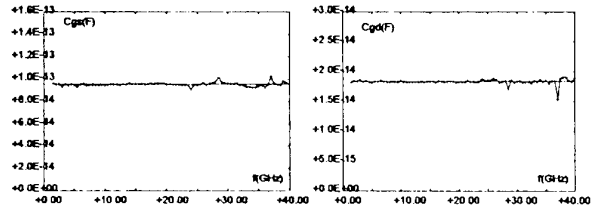
This is the first verification to be made. Checking the I-V characteristics can be performed either on the pulsed characteristics for temperature independent characteristics or in the DC regime in order to verify the electrothermal model including the value of the thermal resistance. One important point for the I-V verification is to simultaneously check the input and output characteristics. Such verifications are shown in fig-9 for a $600\times0.25\mu m^2$ PHEMT.

[S]-parameters verification has to be performed for both the linear model which is used for extraction and the linearized NL model. When checking the linear small signal model the validity of the topology chosen can be adressed by plotting the variations of the intrinsic elements of the EC versus the frequency when they are computed at each frequency by closed form formula. Indeed one requirement for the validity of an EC model is that the constitutive elements of the circuit are not frequency dispersive. Moreover it must be noted that this condition ensures a very good fit of S-parameters data. For FETs this condition is well verified for frequencies up to 40GHz using the classical model. Fig 10-a, 10-b 10-c and 10-d show the values of C_{gs}, C_{gd}, G_m, and G_d of a $0.15\times 50\mu m^2$ coplanar PHEMT extracted from pulsed S parameters up to 40GHz versus frequency. It can be noted that these elements are frequency independent, thus enforcing the validity of the topology chosen.

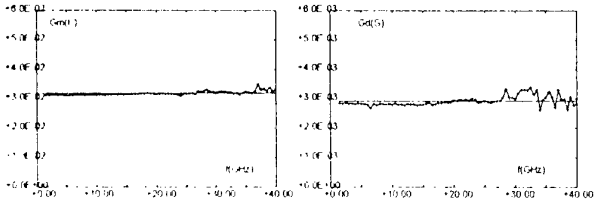


a) Id(A) b)Ig(A)

Fig- 9 Output and Input I-V verification for a 0.25 x600 μm² PHEMT . -1.2V<Vgs<1.0V step=0.2V. Points are measurements, lines are simulation

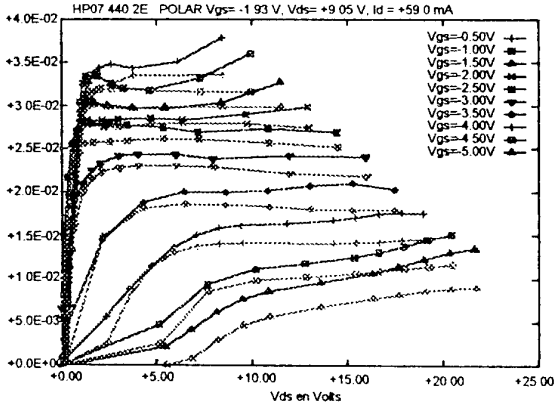


a)Cgs(F) b) Cgd(F)

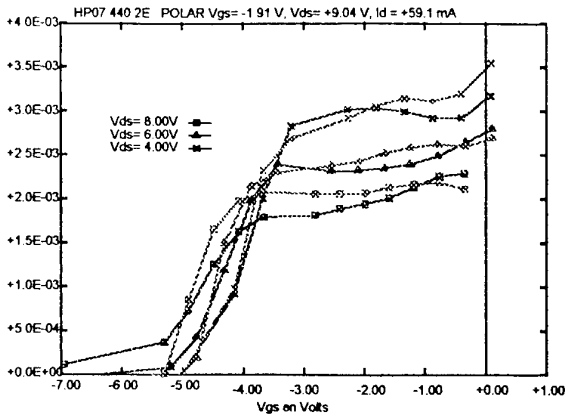


c) Gm(S) d) Gd(S)

Fig-10 Plots of the values of the EQ intrinsic elements obtained by direct extraction from pulsed S parameters measurements (1Ghz-40GHz).



a) Gm (S)



b)

Fig-11 Comparison of the a) Transconductance and b) output conductance obtained from I-V and RF characteristics for a 400x0.7μm² power MESFET.

Finally another important point to check is the consistency between I-V derivatives G_m and G_d and the same quantities obtained from S-parameters measurements. This implies the use of pulsed measurements. Such comparison is given in fig-11 for a 4×100×0.7 μm² MESFET, where a good consistency between I-V and RF model is observed.

3-2 Large signal verification

In the verification process two kinds of large signal validations can be performed. The first one consists in comparing the measurements realized on the manufactured MMIC with simulated results. Although this is the final goal of the modeling action, it is not the best suited for active device model verification. Indeed in this kind of verification, because of the complexity of the circuit and of the possible inaccuracies of passive element models, it is very difficult to identify the eventual reasons for discrepancies if they are observed. So, for testing model reliability, large signal load pull measurements are preferable.

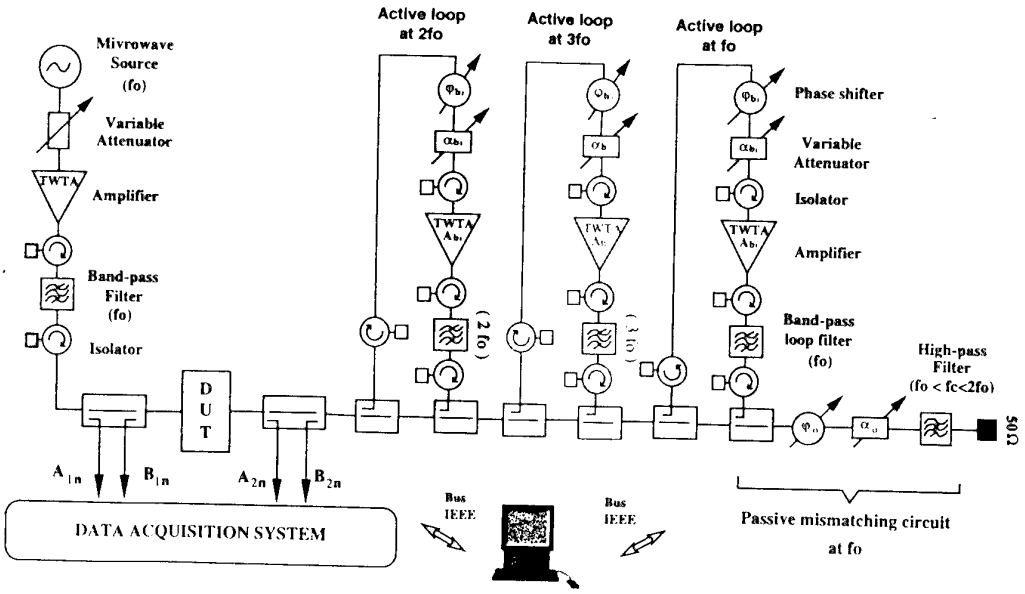


Fig-12 Multiharmonic Frequency Domain and Time domain load-pull system

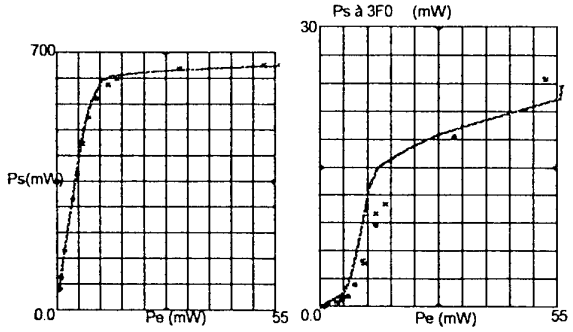
Load pull measurements are well suited for the validation of nonlinear electrothermal models as they are of prime importance for investigation of power saturation mechanisms. Moreover the effects of load impedances at harmonics on the performances of transistors in terms of Added Power (AP) and Power Added Efficiency (PAE) can be investigated. The load pull system we have developped [16] is based on the principle of the active loop technique shown in fig-12. The use of three separate active loops allows a simultaneous synthesis of load impedances at the first three harmonics coming out of the transistor tested. It has to be noticed that the synthesis of load impedances at each harmonic is fully independent of the load at other harmonics. This makes the characterization procedure easy and efficient. Moreover, highly reactive load impedances at harmonics two and three (closed to the edge of the Smith Chart), which are required to improve the performances of transistors in terms of AP and PAE, can be synthetized.

This set-up can be coupled either to a four channel Vectorial Network Analyser (VNA) or a four channel Vectorial Nonlinear Network Analyser (VNNA). In the first case if the VNA can be configured in a receiver operating mode load impedances at harmonics can be adjusted and measured, and power levels can be measured at the first three harmonics. In fig-13 we have compared the measured and simulated large signal performances of a 1200×0.5μm² power HFET at 1.8GHz [17]. For this transistor at an input power of 15.5mW the measured and simulated performances were the following:

Electrical Performances	Simulated	Measured
Output power mW(f0)	631	625
Output power mW (3f0)	16	12
Input Impedance Ω (f0)	8.7-j73	8.6-j66
Gain (dB)	16.1	16,05
PAE %	69.8	71.5
DC Drain Current (mA)	126	122

Furthermore if a two tone signal drives the DUT, power levels of intermodulation products can be very accurately determined as the system is fully calibrated in the reference plane of the DUT. Fig-13 shows the comparison between measured and simulated results for a 240μm² GaInP/GaAs HBT driven by a two-tone signal ($f_{1,2}$ = 2.2GHz ± 50Khz). A good agreement between measured and

simulated data can be observed. Such a characterization procedure which is performed under a non constant envelope microwave signal is a keypoint to claim the robustness of NL models.



a) b)

Fig-13 Power transfer characteristic at a) 1.8GHz and b) 5.4GHz for the HFET 0.5×1200 µm² for load impedances:
Zl(f0)=45-j3.9Ω ; Zl(2f0)=3.4+j9Ω ;
Zl(3f0)=16.5-j24.5 Ω

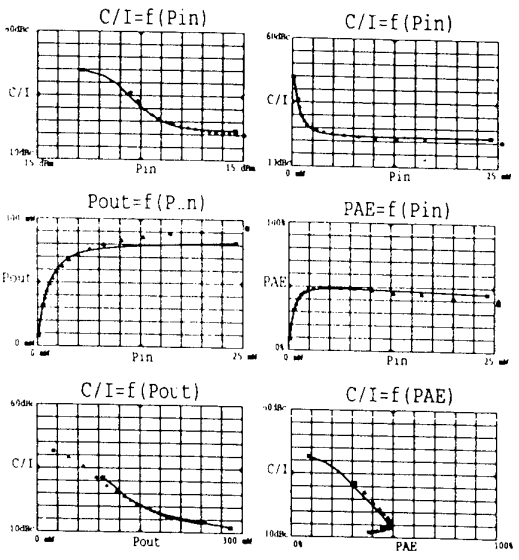


Fig-14 Measured and modelled C/I for a class AB 240µm² GaInP/GaAs HBT. Load impedances have been optimized for maximum AP

Nowadays, the need for Time domain waveforms measurements is more and more emerging . They provide a fundamental tool for model verification. Such measurements require the use of a specific Data Acquisition unit based on the principle of coherent frequency compression and translation of microwave signals [18] . Appropriate phase and amplitude calibration procedures are necessary to get error corrected, absolute complex power waves and to extract time domain I-V waveforms at both ports of the device simultaneously.

Furthermore, by monitoring load impedances at harmonics, I-V waveforms can be experimentally optimized to reach the maximum performances of the transistor tested. Fig-15 shows the waveform measurements of a 0.7×600µm² MESFET operating in class F at 1.8GHz. For this transistor a PAE of 84% was obtained.

Fig-16 shows the comparison of measured and simulated I-V waveforms for a 240µm² GaInP/GaAs HBT at 8.1GHz with a 50Ω load.Three harmonics (16.2 and 24.3 GHz) were taken into account to represent the I-V waveforms. Simulated data were obtained using a newly developped electrothermal model.

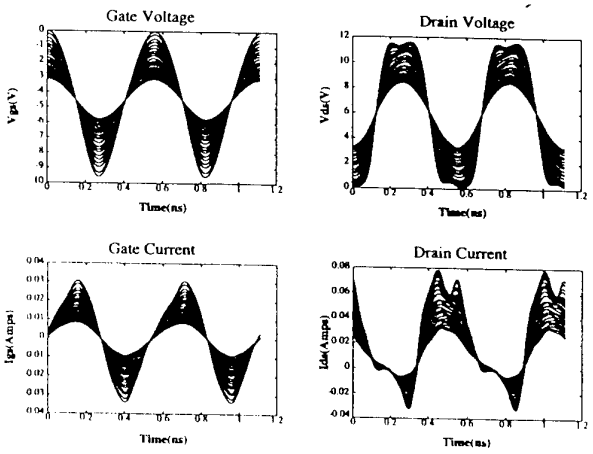


Fig-15 Optimized waveforms for a 0.7×600µm² MESFET at fo=1.8GHz ; Zl=130+j72Ω
Bias point : Vgso=-4.4V, Idso=7mA, Vdso=6V

This system is also capable of measuring time domain waveforms at both ports of any transistor driven by a two-tone excitation. In that case the visualization of I-V waveforms allows a novel approach for the analysis of carrier and enveloppe distorsion. The measurements of a 240µm² HBT are given in Fig-17. It has to be noted that a frequency scale normalization has to be applied so that the enveloppe carrier at frequency 100KHz includes only 20 periods of the RF carrier. In that case a deep insight into the carrier and enveloppe distorsion is obtained.

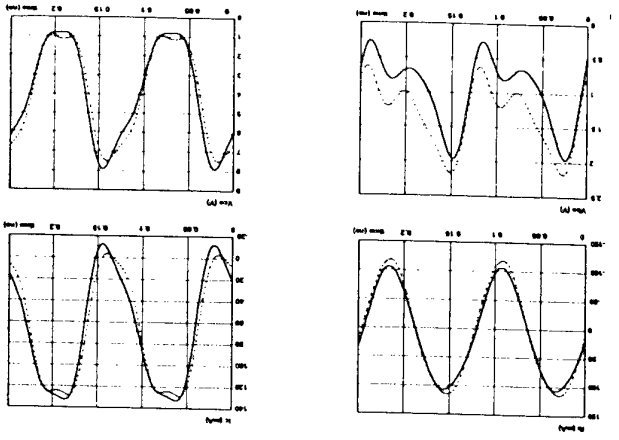


Fig-16 Comparison between measured (dotted lines) and modelled extrinsic voltages at both ports of a 240µm² GaInP/GaAs HBT.
Fo= 8.1GHz, Vceo=4V, Ico=68mA, Pi=29.7mW

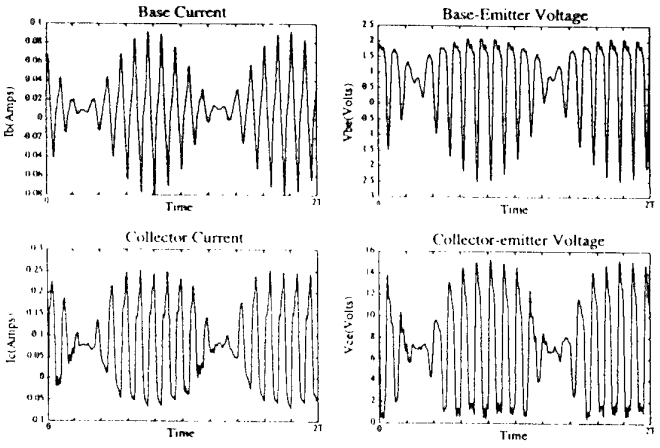


Fig-17 Waveforms of a 240µm² HBT measured under two-tone excitation
f1=1.7995GHz ; f2=1.8005GHz, Zl=47+j17Ω

4- Conclusion

Nonlinear modelling of Active devices still represent a complex task. On one hand, new techniques such as pulsed measurements techniques have been developped to enhancethe accuracy of the model extraction, on the other hand novel large signal measurement procedure (Time domain) has been developped to provide a better insight into the operation mode of the transistor. A complete set of characterization techniques for I-V small signal and large signal measurements has been presented. All these techniques allow to complete all the steps of the modelling process including an in-depth verification of the large signal behavior of the devices which is absolutely necessary to provide reliable NL models.

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InP and GaAs power HEMT characterization with a Ka band active load pull system

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Introduction

The development of television, phone, automotive applications results in an increasing demand for millimeter wave range power devices and integrated circuits. DC measurements and S parameter measurements alone are not sufficient to qualify transistors regarding microwave output power. It is desirable to use on wafer testing to check the large signal performance of the device. For this purpose load pull measurement setups have been developed using vector error correction techniques to provide accurate load reflection coefficient and RF power data for the measured device. The present paper gives an overview on this topic. It starts with key factors responsible for their power limitations. After that the characteristics of various types of bench passive or active will be described with a comparison of the main limitations. Finally some results relevant to GaAs and InP devices will be given with an analysis which will illustrate the first part of the presentation.

Power key factors

High power performances require high drain current and high drain source breakdown voltage. This condition alone is not sufficient because good power added efficiency requires also to have a power gain as high as possible and as constant as possible over the whole dynamic excursion.

A drain current density of about 1 A can be achieved with the heterojunctions systems. The double heterojunction pseudomorphic HEMT with planar doping associated with one or two channels is to date the must popular and efficient structure [1]. From this point of view the AlInAs/GaInAs/InP lattice matched or mismatched are well suited. Drain current density of about 1.5 A/mm is easily obtained with a pinch off voltage which is not too high (around - 2V) [2].

Breakdown voltage is much more difficult to achieve, because it generally implies a subtle trade-off between several factors, and that is more and more critical as the operating frequency increases. The breakdown voltage is essentially fixed by the electric field at the gate corner towards the drain, which activates physical phenomena. Impact ionisation dominates at open channel and tunnelling effect plays a major role near and under pinch off conditions [3]. The first solution to improve breakdown voltage can be achieved by simply making a wide recess. This device exhibits good reverse breakdown voltage and small signal microwave performances. However the power microwave performances of this device (presented in the last part) are largely inferior to what can be expect from DC and small signal characteristics. This behaviour is attributed to surface states which play the role of parasitic gate and undermine the I(V) characteristics under large signal conditions [4]. It is clear that ensuring HEMT's to be candidate for power applications, requires that effect of parasitic gating by excess surface charges must be screened from channel electrons [5,6]. This can be accomplished by modifying the recess, using a double recessed gate process, and adding charge screen layers [7]. This topologies allowed the simultaneous achievement of high power added efficiency and high power density which established record performance for power PHEMTs up to Ku band, to our knowledge. Effectively it becomes very difficult to determine the right dimensions of the topology in Ka band and higher. At the present time, the first devices with a double recess start appearing in Ka band [8] owing to an important improvement of the technological gate recess combining wet and dry etching techniques with an etch stop layer. It was found that such a topology not only results in a large drain voltage capability but also in an increase in drain delay and, consequently, in a decrease of the operating frequency [9]. So in this frequency range an important limitation lies in having a high breakdown voltage without sacrificing efficiency and gain.

The devices linearity are essentially fixed by the variations with the gate source voltage of input/output capacitances, transconductance and output conductance [10]. But in millimeter wave range we have noted that the occurrence of power saturation is strongly correlated with

a sudden increase of the average gate current [11]. So the best device is the one which allows a linear increase of the power level without premature starting of forward or reverse gatecurrent [12]. The higher output power densities and efficiencies at millimeter wave frequencies for discrete transistors are often obtained with small gate width devices. Unfortunately, to raise the power level it is necessary to increase the total gate width, which induces significant degradation in gain, efficiency and power density due to :

- signal attenuation along the gate width [13]
- phase variations between different gate fingers
- increased parasitic capacitance and source inductance [14].

The most important effect is that related to the source inductance of the airbridge used to interconnect the different source pads. Indeed, in this case, Ls varies nearly linearly versus the total gate width [15]. The reduction of this effect passes through the use of individual source via holes, but at the price of more technological complication. An other important point to underline is the reduction of the S12 feedback magnitude in this case, which gives rise to a nearly unilateral device, and greatly simplifies matching circuit design [16].

The power benches

DC measurements and small signal microwave measurements alone are not sufficient to qualify transistors in terms of microwave output power. For this purpose large signal microwave measurement setups have been developed. Effectively at the beginning these systems were dedicated for finding the optimal load impedance for some working conditions (maximum output power or added efficiency). Today there are also other applications like an accurate validation of the non linear models. Two kinds of benches are classically used to study the device under power conditions.

Firstly the passive systems, where mechanical tuners are used. The main advantages are minor risk of oscillations, strictly linear behaviour and independent adjustment of magnitude and phase of the load. The main drawback is the limitation of the maximum load reflection coefficient which be simulated at the output of the device. Several societies market tuners covering the 0.8 to 100 Ghz range.

Secondly, the active systems which are divided in two families based either on the TAKAYAMA principle or on the active loop principle. The main advantage of these benches is the no limitation of the load magnitude presented at the device compared to passive systems. But, at the opposite, these systems are more expensive and more difficult to use (risk of oscillation, difficulty to keep constant the output load versus the injected power level by example). A comprehensive and fair comparison between active and passive systems was given by Muller et al [17].

In our labs, an active load pull system has been used based on the TAKAYAMA principle in Ka band (26-40 GHz), with a specific procedure [18]. Its simplified block diagram is shown in figure 1. The major part of the system makes use of wave guides. Two TWTA's are necessary to obtain enough power level to synthesise any load impedance at the output of the device whatever its total gate width and whatever the power level under investigation. The core of the measurement system includes a Wiltron 360B network analyser, a 3630 frequency down converter and an outside transfer switch. This transfer switch is the key component which allows to use the system either as a Sij parameter measurement set up or as a power active load pull system. See References [18, 19] for power and impedances vectorial calibration. The use of the bench is as follows :

Firstly, the bench is used as a classical vector network analyser to determine the scattering parameters of the DUT at the bias power conditions. This allows to determine the optimal load pull area (where the device presents an interesting gain) and also to avoid instability zones. Secondly, the operator chooses the load pull configuration and the interesting area, (define by the user) is described automatically, at different injected power levels. This area can be shifted if the optimal load impedance moves with the injected power level. Moreover the gate current is systematically checked and always limited at a density fixed by the operator. The studied zone is automatically reduced depending on the gate current magnitude in order to avoid damage of the device. Some examples will be presented in the next part.

Some results

The first device is a PHEMT, with two delta doped planes in order to provide enough drain current. A schematic representation of the device is presented figure 2. The gate is offset in the recess towards the source, in order to improve the high breakdown voltage and not to degrade the access source resistance and transconductance [20]. In this case the breakdown voltage in gate drain diode configuration is around 10 V and the drain current density is 650 mA/mm. From these characteristics the potential output power in class A is 800 mW/mm. However, the power results do not come up to our expectation and a premature compression occurs, accompanied by a decrease of the drain current. The maximum power results are the same whatever the drain source bias 3, 4 or 5 volts in class A (Fig. 3). A maximum power density of 260mW/mm at 5.5 dB of compression

and a power added efficiency of 15% has been reached at 30 GHz. This effect is assumed to be due to the surface effect in the immediate vicinity of the gate at the drain side. A pulsed I-V (Fig. 4) has been performed and has confirmed this assumption.

To overcome this limitation a double recessed topology can be realised. An asymmetrical double recess power MESFET is presented (Fig. 5). The static and pulse I-V characteristics were compared so as to evidence how the second recess prevents surface states from degradation of the device performances. These excellent results have been confirmed by power measurements performed in class A at 18 GHz and Vds = 8 V: 0,53 W/mm output power (Fig. 6) with and associated power added efficiency of 40 % and 10 dB linear gain, with a 8x75 µm (600 µm) gate width have been obtained. This corresponds to our knowledge to the state of the art performance for 0,3 µm gate length MESFET's. This kind of topology is widely used in frequency up to Ku band, but unfortunately at higher frequency it is difficult to well determine the dimensions and then again it is difficult to control the optimal dimensions. At the present time some compagnies like RAYTHEON by example are undertaking the realisation of these structures for applications in Ka and Q band.

In our labs we have carry out some simulations to determine the optimal doping densities and device structure with a single recess in Ka band. In order to combine, high breakdown voltage, high drain current and good microwave performance. This study has been performed with a 1D model which is used for charge control calculation and a 2D simulation for breakdown analysis [21]. Of all the processing issues relevant to power transistors, the gate recess step (including the channel recess) is, to our opinion, the most critical. The gate to recess edge spacing is indeed the key parameter and must be sufficiently large to preserve a good breakdown behaviour but not so large as to cause the previous problem. This compromise is achieved here with a selective reactive ion etching (RIE). The main problem with this processing step is the small time of the cap layer etching. On the other hand and more a chamber must be dedicated for this step. As it is impossible in our labs it is very difficult to reproduce this step from one wafer to the other.

The device with a 2x35x0,3 μm^2 gate, exhibits an intrinsic transconductance as high as 720 mS/mm, a maximum current density of around 1 A/mm and delivers a state of the art output power density of 1 W/mm with 5,7 dB linear gain and 38 % power added efficiency at 33 GHz (Fig. 7) [11].

In order to present some other possibilities of our system, we will compare the evolutions of the optimal power load impedances versus the injected power level for two devices on InP and GaAs substrates respectively, with the same total gate width and gate length (2x50x0,2 μm^2) at 38 GHz. We establish a more important phase shift of the optimal power load impedance for the InP device than for the GaAs device at a same level of power gain compression (Fig. 8). This kind of behaviour has always been met up to now. At the present time, small signal scattering parameters versus V_{gs} but also V_{ds} are measured, in order to try to find a correlation between these evolutions and the electrical equivalent small signal schemes. Our system allows also to mesure the S'_{11} parameter, which is very important for the designer. From this point of view, a more important evolution of the S'_{11} parameter versus the injected power level is established (Fig. 9) in class Abcompared to class A whatever the kind of substrate (InP or GaAs). The last example presented concerns a total gate width (8x50x0,3 μm^2) on GaAs substrate at 35 GHz, where the optimal power load impedance is near the edge of the smith chart. It will be impossible to realise this optimal impedance with a passive tuner. On this figure (Fig. 10) we report power gain and power added efficiency circles at a constant injected power level as well as the behaviour of the average gate current. All these behaviours are very interesting because they allow to perform some analysis. These results show a strong dependency of the average gate current versus the presented load impedances. Such a behaviour may be interpreted on the basis of different shapes and positions of the dynamic load line in the I-V characteristics [12]. These gate current evolutions are mainly fixed by the DC bias point, the load impedance and the input power level.

Active devices on InP substrate are well suited to microwave application in the V-band and upper, due to their high microwave performances. For all that, a classic power bench on wafer with probes and waveguide tuners has been realised to check these power behaviours in the V-band. An original strain compensated structure layer has been achieved in our labs to obtain a high current density (1,5 A/mm) in order to achieve good power results for an application which requires a low bias voltage (2 V in this case). The results obtained are interesting for a gate length of 0,25 µm : an output power density of 370 mW/mm with a power added efficiency of 28,3 % and a associated gain of 5,2 dB (Fig. 11).

Conclusion :

An original active load pull system, has been developed in the 26-40 GHz band. It permits to accurately extract all gains, all power levels and impedances of interest for a given device even for large total gate width. This system combined with pulsed I(V) and S parameters is a complete set of analysis which allows to make links between physical effects and power measurements. In

these conditions we have the possibilities to perform reverse technological engineering in order to improve the design of our devices (recess topologies or development effects). Furthermore all these informations are very important to robustly verify the validity of non linear models and so, it is a very interesting tool for MMIC design.

Acknowledgements

The author wish to thank B. Bonte, E. Bourcier, S. Piotrowicz, D. Théron, B. Boudart, S. Trassaert, M. Zaknoune, Y. Crosnier for their cooperation during the preparation of this paper and Thomson TCS, IAF Freiburg for providing specific devices.

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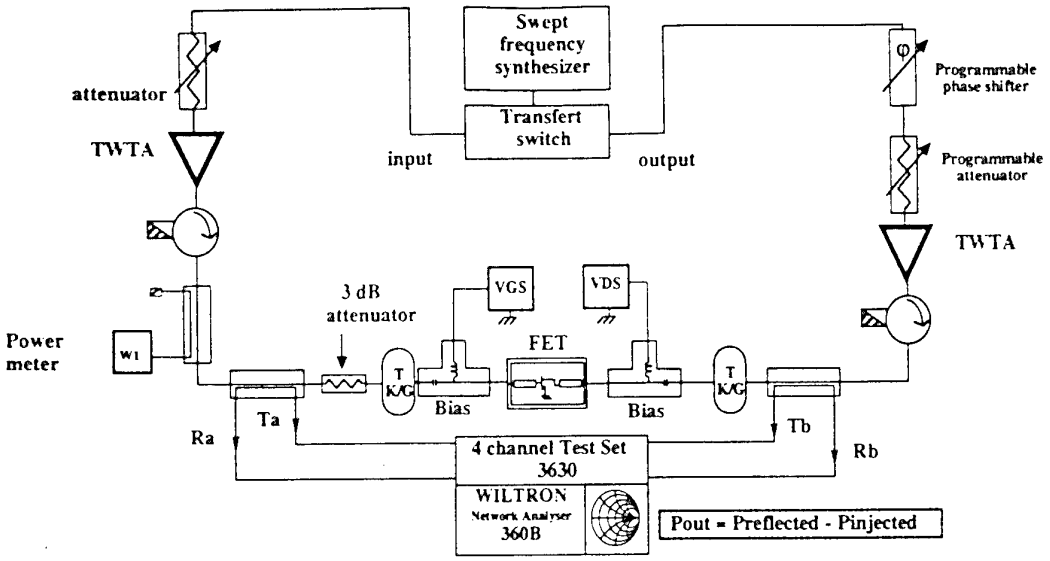

Figure 1 : Simplified block diagram of the active load pull system in the Ka band.

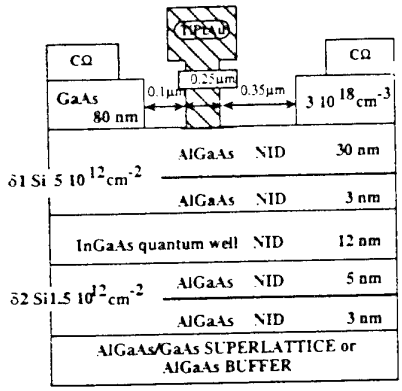

Figure 2 : Schematic representation of the asymetrical simple wide recess P HEMT.

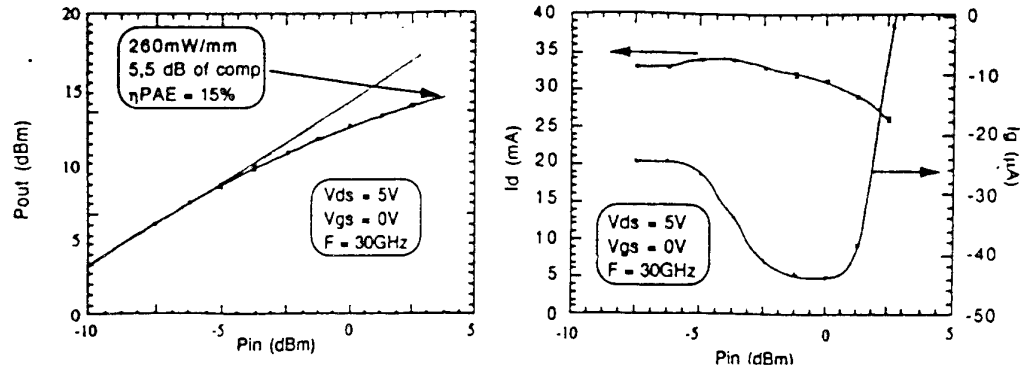

Figure 3 : Output power versus input power at 30 GHz for the 2x50x0,25 µm^2 total gate width (V_{DS} = 5 V, V_{gs} = 0 V) PHEMT with an asymetrical simple recess as shown in Figure 2

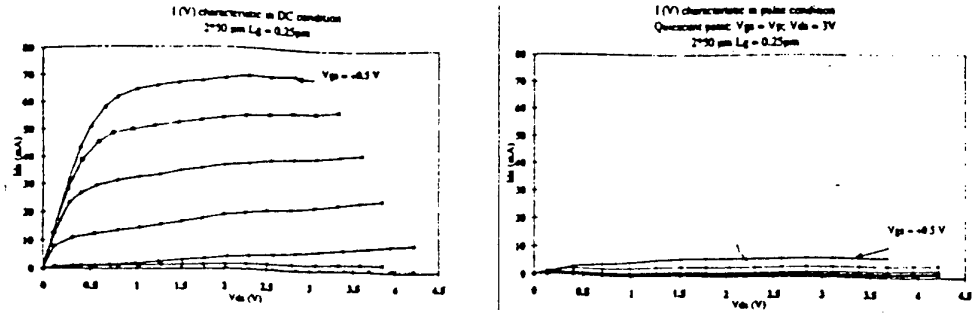

Figure 4 : Drain current characteristics in pulse (a) and static (b) measurement of the asymetrical simple recess PHEMT shown in Figure 2.

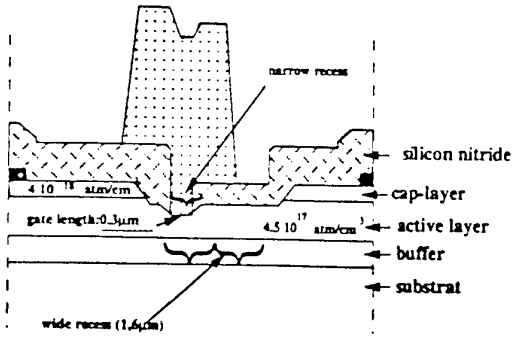

Figure 5 : Schematic representation of the double recessed power MESFET.

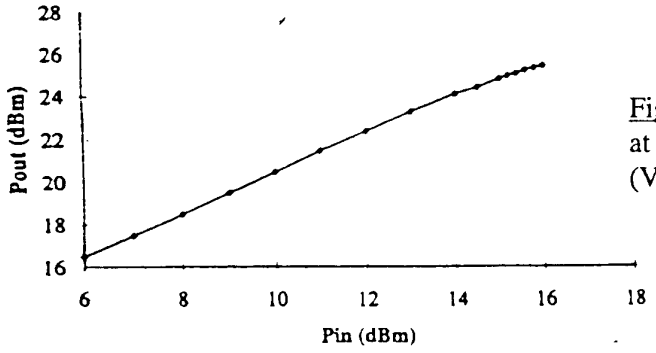

Figure 6 : Output power versus input power at 18 GHz for the 8x75x0,3 μm^2 total gate width (V_{DS} = 8 V, V_{gs} = - 1 V). MESFET shown in Figure 5.

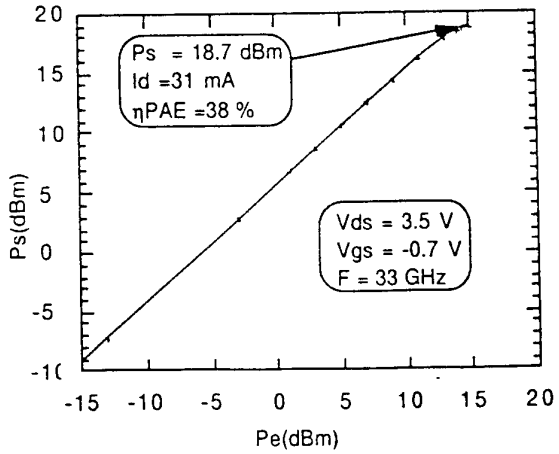

Figure 7 : Output power versus input power at 33 GH for the 2x35x0,3 μm^2 total gate width (V_{DS} = 8 V, V_{gs} = - 1 V). PHEMT with an optimal RIE recess.

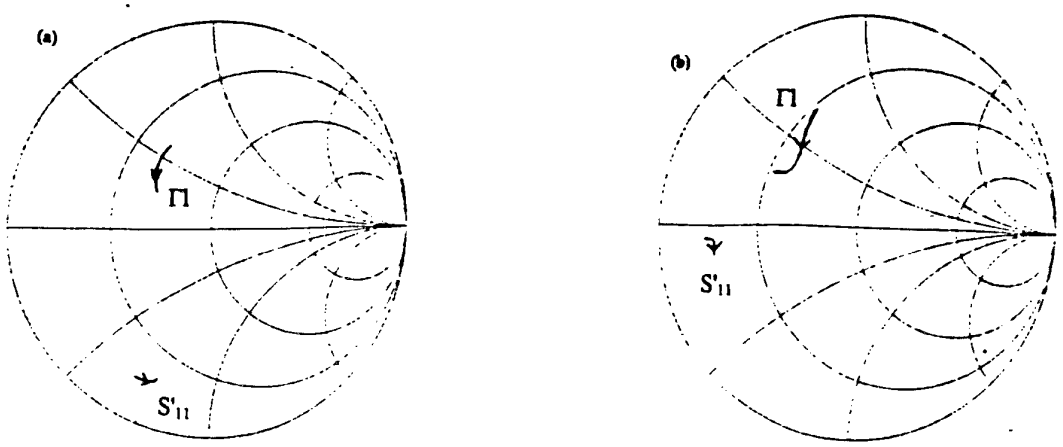

Figure 8 : Behaviour of the optimal power load impedance versus the injected power level for a GaAs substrate HEMT (a) and for a InP substrate HEMT (b) biased in class A at 38 GHz.

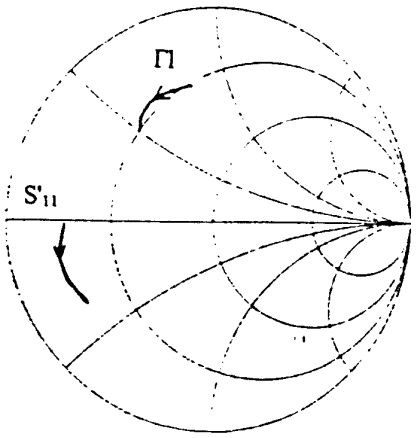

Figure 9 : Evolution of the S'_{11} parameter versus the injected power level for a HEMT device biased in class B at 38 GHz.

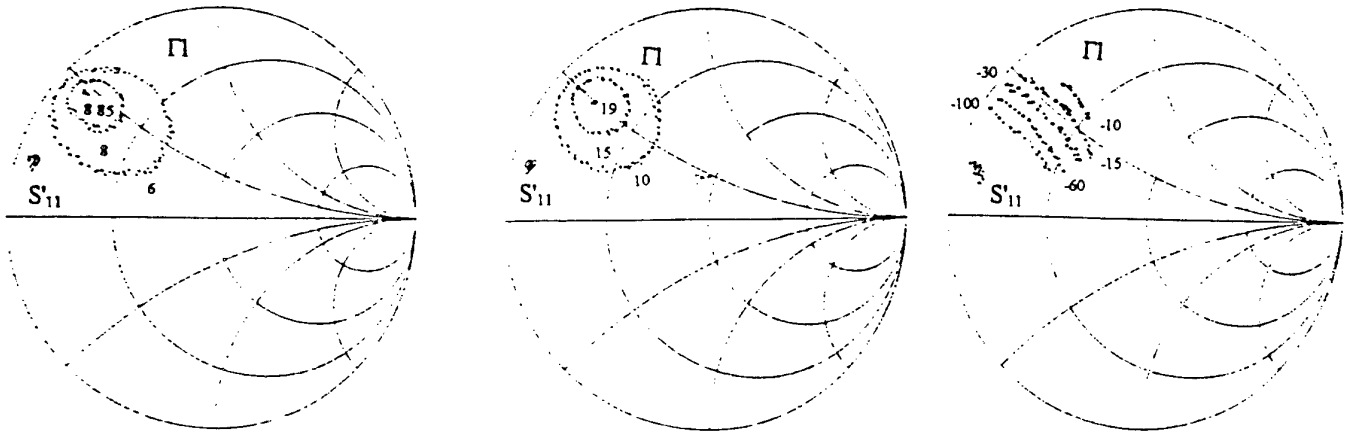

Figure 10 : Evolution of power gain circles, power added efficiency circles and constant gate current loci, at a constant injected power level at 35 Ghz for a 8x50x0,3 μm^2 PHEMT

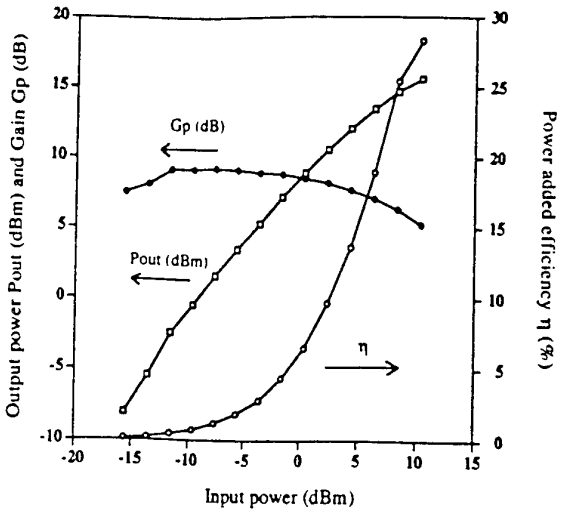

Figure 11 : Power characteristics at 60 GHz at V_{ds} = 2 V and V_{gs} = - 1.5 V, with a classical linear power bench, for an InP HEMT.

On-Wafer Noise Parameter Measurements at 60 GHz

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Abstract: A measurement setup for noise characterization of active devices at 60 GHz range has been designed and built. The cold-source method is used. Both S- and noise parameters can be measured with the setup. A description of the measurement method and setup is shown, as well as, the measurement results of an InP HEMT at 58-62 GHz are presented.

Introduction

Both noise and S-parameters are needed for optimum amplifier design. Usually noise parameters at mm-wave frequencies are not given by the transistor manufacturer or they are extrapolated from lower frequencies. To validate the extrapolation or the noise model used in design, direct noise parameter measurements are necessary. This paper presents a measurement system which allows simultaneous on-wafer noise and scattering parameter measurements at the 60 GHz range. S-parameter measurement frequency range is 50-75 GHz and noise parameter measurement range is 58-62 GHz. In a direct noise parameter measurement different source impedancies are presented to the device under test (DUT) and corresponding noise figures are measured. There are four unknown noise parameters F_{min}, R_n, Γ_{opt} (magnitude and phase) so a minimum of four measurements are required. However, in order to minimize the effects of the measurement errors, additional measurements are done and curve fitting is applied. Cold-source measurement method [1] is used to measure the noise parameters of the DUT. The technique presented in [2] has been improved. New technique [3] corrects effects of reflection coefficient difference of the noise source between on and off states. A further improvement takes into account losses of the passive network between the DUT and the receiver [3]. Only a simple 1-port tuner is needed in this method. Due to losses between the DUT and the tuner the highest DUT source reflection coefficient magnitude is about 0.7.

The measurement setup

Major components of the noise parameter measurement setup are presented in Figure 1. The whole setup is controlled by a PC which is connected to measurement instrumentation via GP-IB bus. The data acquisition and necessary calculations are done by software written in-house. An automatic vector network analyzer (VNA) is used for system characterization and S-parameter measurements of DUT. A schematic of the setup is shown in Figure 2.

By including two waveguide switches both noise- and S-parameters measurements and the receiver calibration can be done without breaking any connections. This means that the receiver can be calibrated any time during long measurement sessions to reduce the effects of drifting. Also an uncalibrated 1-port tuner can be used.

The receiver is shown in Figure 3. The first IF is selected so, that the image frequency is

lower than the cut-off frequency of the WR-15 waveguide enabling SSB noise measurements. The LNA is a 6-stage PHEMT amplifier designed at VTT [4]. A frequency synthesizer is used for clean LO signal with easy frequency control. Due to the low output power level of the synthesizer a biasable mixer is used. The second stage of the receiver is a commercial satellite down converter. A noise figure meter is used for the noise power detection. It has a noise bandwidth of 5 MHz.

Additional instruments are power sources, which provide the correct bias for the receiver components and the DUT.

System characterization

Before the actual noise measurement are carried out, the test system must be fully characterized. Characterization includes measurements of passive networks between reference planes A-B, C-E, D-E, reflection coefficients of the receiver and noise-source (both hot and cold states). Passive networks A-B and C-E cannot be measured directly with the VNA since they are non-insertable. To characterize these VNA is first calibrated to reference planes A and E, shown in Figure 4, and it is connected to the tuner and the receiver ports of the switches. Then an on-wafer 2-port LRM calibration is conducted to the reference planes B and C. The two sets of error coefficients are called from the VNA to the controlling PC and the S_{11}, $S_{12}S_{21}$ and S_{22} of the passive networks are calculated. The passive network D-E and the reflection coefficients can be measured conventionally with the VNA. The VNA is connected to the measurement system as shown in Figure 2 and a 1-port calibration is conducted to reference plane A via switch 1. After the calibration the tuner is connected to port 1 of the switch 1.

Calibration of the receiver

The receiver is calibrated in two steps. The gain-bandwidth constant kBG is measured by connecting the noise source to the receiver via switch 2. Noise power is measured with the source on and off at all the measurement frequencies.

$$kBG = \frac{P_{Hm} - P_{Cm}}{\left(\left[T_H G_{aH} + (1 - G_{aH})T_a\right] \cdot M_H\right) - T_a M_C}, \qquad (1)$$

where P_{Hm} and P_{Cm} are measured hot and cold noise powers respectively, T_H is the noise temperature of the hot source, T_a is the ambient temperature, G_{aH} is the available gain of the passive network between reference planes D-E when the noise source is on, and M_H and M_C are corresponding mismatch coefficients of on and off states. The available gain G_{aH} and the mismatch coefficients are used to calculate the effective noise temperatures at the receiver port. The second step is the determination of the receiver noise figure. The receiver has an isolator in the input port, so the noise figure of the receiver is independent of the source impedance. The receiver noise figure can be calculated from the kBG measurements,

$$F = \frac{\left(\left[T_H G_{aH} + (1 - G_{aH})T_a\right] \cdot M_H\right) - YT_a M_C}{T_0(Y - 1)} + 1, \qquad (2)$$

where T_0 is standard temperature of 290 K and Y is

$$Y = \frac{P_{Hm}}{P_{Cm}}. \qquad (3)$$

If an isolator is not included, the receiver noise figure is dependent of source impedance and receiver noise parameters must be determined as presented in [2].

Noise measurements

After the system characterization and the receiver calibration the setup is set for noise

measurements. The configuration is presented in Figure 2. The DUT is placed into the probe station and set to the operating point of interest. The VNA is switched to the DUT and the 2-port S-parameters are measured. Noise figure measurements are done in two steps. First the VNA is connected to tuner via switch 1, tuner is set and its reflection coefficient is measured. Then the tuner is switched to the DUT and noise power is measured as a function of the frequency. The procedure is repeated for all the selected source impedance points. The noise figure of the entire system is given by

$$F_{tot,i} = \frac{P_i\left|1 - S_{11}\Gamma_i\right|^2\left|1 - \Gamma_s\Gamma_{rcv}\right|^2\left|1 - S_{11OUT}\Gamma_2\right|^2}{T_0 kBG\left|S_{21}\right|^2\left(1 - \left|\Gamma_i\right|^2\right)\left|S_{21OUT}\right|^2} - \frac{T_a}{T_0} + 1 \qquad i = 1,2,3... \tag{4}$$

where P_i is the measured noise power, Γ_i is the source reflection coefficient of the DUT, S_{ij} are the S-parameters of the DUT, S_{ijOUT} are the S-parameters of the output network C-E and Γ_2 is the output reflection coefficient of the DUT. The actual source reflection coefficient Γ_i seen by the DUT calculated from the measured reflection coefficient at the tuner reference plane A and the S-parameter data of A-B network acquired during the system characterization. The noise figure of the DUT is calculated using the Friis formula [5] as follows,

$$F_{DUT} = F_{tot} - \frac{F_{rcv} - G_{aOUT}}{G_{aDUT}G_{aOUT}}, \tag{5}$$

where F_{rcv} in the noise figure of the receiver, G_{aDUT} is the available gain of the DUT, G_{aOUT} is the available gain of the output network C-E. As a result we get the noise behavior of the DUT as a function of source impedance. The noise parameters are extracted using the least-squares fitting method [6] for all the measurement frequencies.

Measurement results

The results of an InP HEMT are shown in Figures 5 through 8. Three measurements are presented, the same chip was tested with three different source impedance constellations. The number of source impedance points used was 5, 7, and 9. Increasing the number of points did not affect the results. The points were set symmetrically around the center of the Smith chart. The Γ_i constellation of the second (7 points) measurement at 60 GHz is shown in Figure 9. The HEMT was set to operating point V_{ds} = 1.5 V and I_{ds} = 9 mA. The results indicate a good repeatability. To check the consistency of the measurement data and the least-squares fitting method, noise figure was plotted as a function of

$$\left|Y_s - Y_{opt}\right|^2 / G_s, \tag{6}$$

where Y_s is the source admittance, G_s is the source conductance and Y_{opt} is the calculated optimum source admittance, where the minimum noise figure is achieved. The plot presents fitting at three different frequencies and is presented in Figure 10. The plot shows a good fit and consistent data.

Conclusions

An on-wafer noise parameter measurement system has been designed and built. The cold-source method was used to measure the noise parameters of an InP HEMT. Previously presented method has been improved by including the effects of reflection coefficient difference between noise source cold and hot states, and the losses of the output network. By relocating the switch 1 a simple uncalibrated 1-port tuner can be used. The measurement results between 58-62 GHz are presented.

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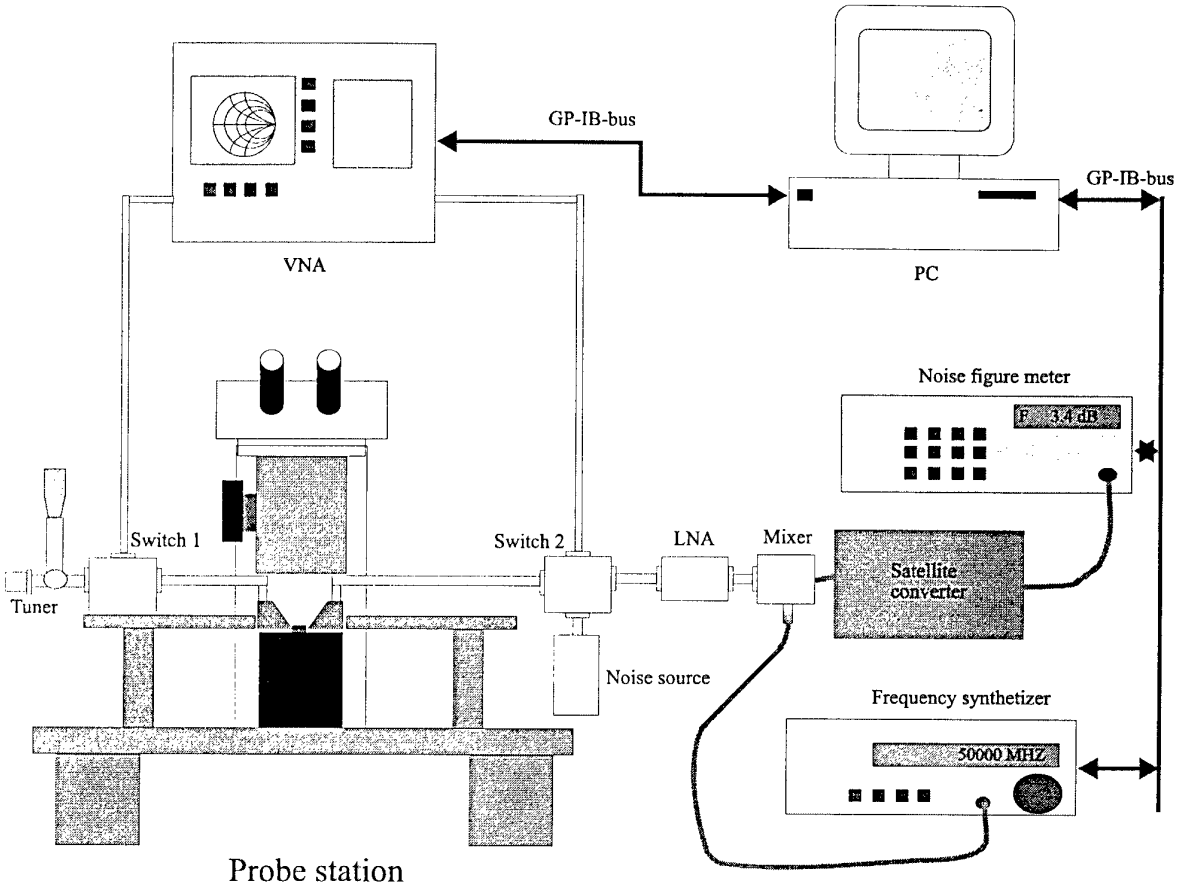

Fig.1: Noise parameters measurement system.

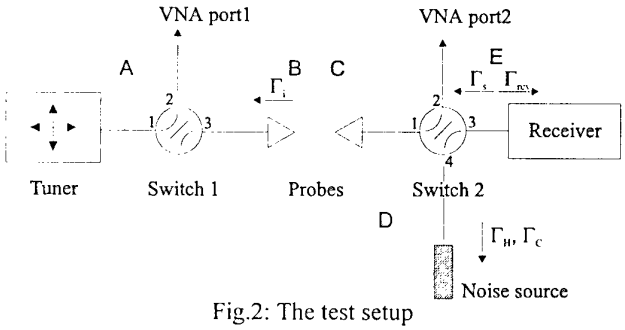

Fig.2: The test setup

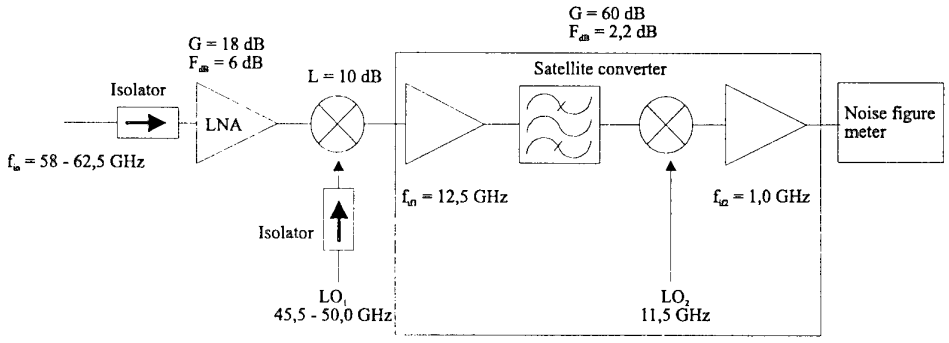

Fig.3: The receiver

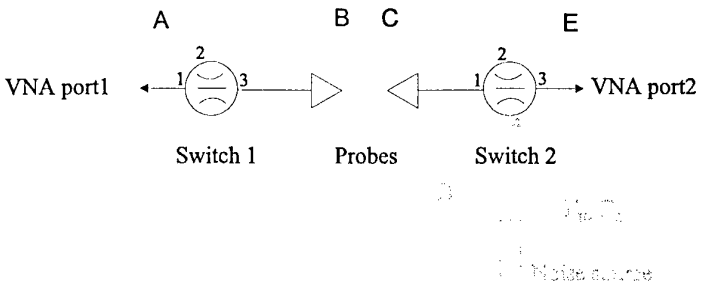

Fig.4: Configuration for characterization of non-insertable networks.

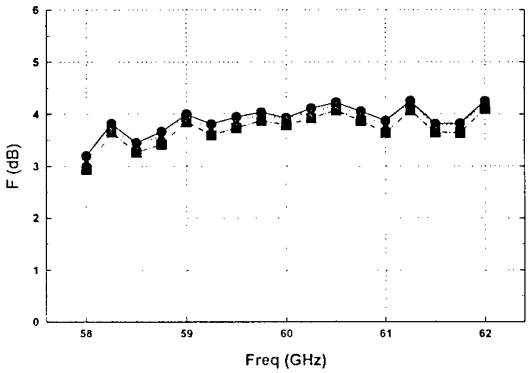

Fig.5: Measured minimum noise figure F_{min}.

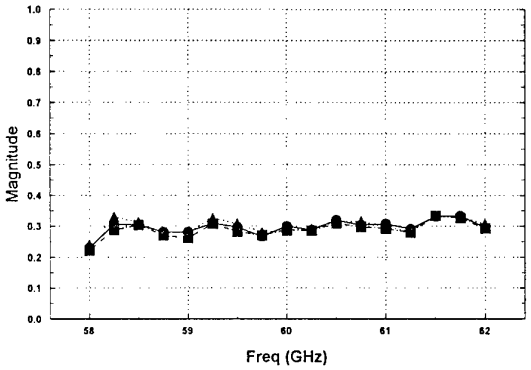

Fig.7: Measured magnitude of Γ_{opt}.

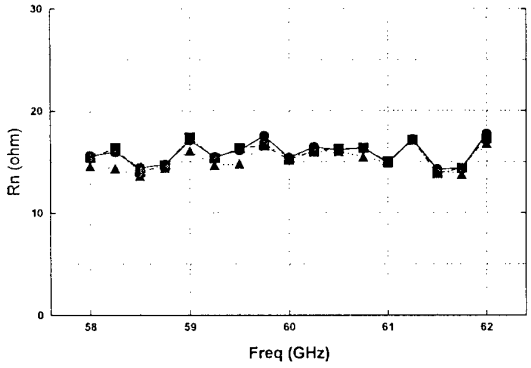

Fig.6: Measured noise resistance R_n.

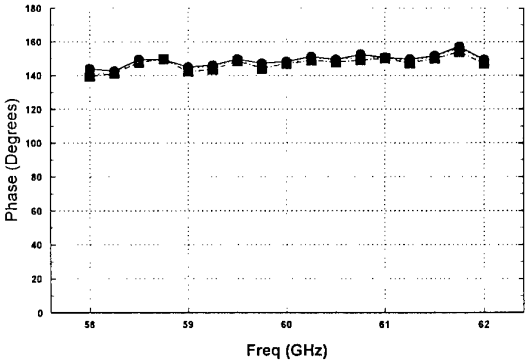

Fig.8: Measured phase of Γ_{opt}.

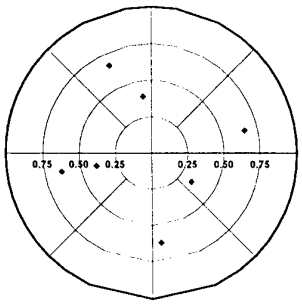

Fig.9: Γ_i constellation at 60 GHz of the second measurement (7 points).

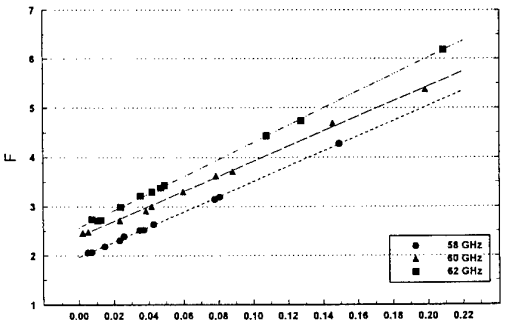

Fig.10: Scattering of the measurement data from the best fit curve. Eq.(6) is the x-axel.

NOISE MODELLING IN LINEAR AND NONLINEAR DEVICES

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Abstract

This paper presents a review of the techniques and models that can be used for the noise performance calculation of devices under linear and nonlinear operation.

1-Introduction

In physics and electrical engineering one often encounters fluctuating signals generated in electrical devices and circuits. These fluctuating signals called 'noise' are due to random events that modify the average number and/or the avarage velocity of carriers. These fluctuating signals have a great influence on the performance of linear circuits like amplifiers as well as on nonlinear circuits like mixers ans oscillators. Fortunately reliable techniques are available to described the noise behaviour of linear and nonlinear devices and circuits. The aim of this paper is to review the noise modelling techniques that can be used for devices under linear and nonlinear operations.

2-Noise modelling in linear devices

Figure (1) shows a DC biased device. Let us consider a small volume dV located at point $\underline{r}$ in the device. The fluctuations of the current density $\underline{j}(\underline{r})$ at point $\underline{r}$, that are due to the fluctuations of carrier density and carrier velocity, induces voltage fluctuations at any point $\underline{r}'$ of the device and consequently at the electrodes. It should be noted that **only** the current and voltage fluctuations at the electrode can be measured The voltage fluctuations at electrode M, resulting form the current density fluctuations at $\underline{r}$ depends on two factors :

- the strengh of the fluctuation at $\underline{r}$ (local or microscopic noise source)
- the device stucture between $\underline{r}$ and M (impedance field).

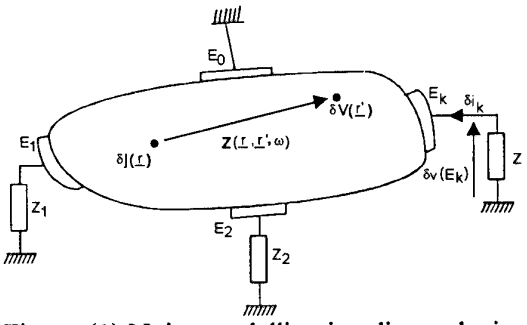

Figure (1) Noise modelling in a linear device

So, for the noise modelling in a linear device, we have to know the microscopic noise processes involved and the device stucture (material, doping...). At a given electrode, the total noise voltage (or total noise current), due to all the microscopic noise sources located in the device, is obtained by integration over the whole device. This total noise voltage is referred to as the **macroscopic** noise source. When the macroscopic noise sources are known, the calculation of the noise performance (noise

figure, noise resistance and optimum impedance for an amplifier....) can be carried out by simple circuit manipulations(Rothe, 1956).

The macroscopic noise source calculation

In noise modelling, the main problem is to calculate the macroscopic noise current or noise voltage sources that characterize all the microscopic noise sources located in the device. Two methods can be used : the Langevin method (LM) and the impedance field method (IFM)(Van Vliet, 1975). Although it has been shown that these two methods are strictly equivalent (K.K Thornber, 1974) the latter is mostly used probably because the IFM is more suited for numerical analysis. For this reason, the IFM only will be described here.

Two dimensional formulation of the IFM

For two dimensional (2D) devices such as FETs or HBTs the calculation of the noise properties by using two dimensional modelling needs a 2D formulation for the IFM. Let us consider a 2D device with all electrodes but the i-th one are shorted, while the i-th is open. A small current density $\delta\underline{J}(\underline{r}, \omega)$ located at $\underline{r}$ produce a noise voltage $\delta V(\underline{r}')$ at $\underline{r}'$ given by:

$$\delta v(\underline{r}', \omega) = \underline{z}(\underline{r},\underline{r}'\omega).\ \delta\underline{J}(\underline{r}, \omega)d^3r \quad (1)$$

$\underline{z}(\underline{r},\underline{r}', \omega)$ is just a form of Green's function (Linear problem). Assuming that the noise sources are spatially uncorrelated, the power spectrum of the current density fluctuation is given by :

$$S_{kj}(\underline{r},\underline{r}', \omega) = \delta J_i(\underline{r})\delta J_k(\underline{r}') = K_{\delta j}(\underline{r}, \omega)\,\delta(\underline{r}-\underline{r}') \quad (2)$$

with (Van Vliet 1975) $K_{\delta j}(r, \omega) = 2q^2 [\ D(\omega)+ D^{T*}(\omega)\ ]n_0(r)$ (3)

where T* stands for « transpose conjugate » tensor. From (1), the power and cross spectra of the macroscopic noise voltage sources are given

$$S_{eiei} = \int\underline{z}(\underline{r}_i,\underline{r}, \omega)K_{\delta j}(r, \omega)\underline{z}^{T*}(\underline{r}_i,\underline{r}, \omega)d^3r$$

$$S_{eiej} = \int\underline{z}(\underline{r}_j,\underline{r}, \omega)K_{\delta j}(r, \omega)\underline{z}^{T*}(\underline{r}_j,\underline{r}, \omega)d^3r$$

In these expressions, the vector Green's function $\underline{z}(\underline{r}_i,\underline{r},\omega)$ is no else that the impedance field $\nabla_r Z(\underline{r}_i,\underline{r})$. A powerful method to compute the 2D impedance field proposed by Ghione (Ghione , 1993) is based on the adjoint approach.

Noise modelling using the Monte-Carlo method

Monte-Carlo techniques are very useful, not only to calculate the properties of homogeneous semiconductors but also to calculate the macroscopic noise sources. As a matter of fact, a device modelling using the Monte Carlo method provides, at each time t, the instantaneous current i(t) including the diffusion noise. The Fourrier transform of the current fluctuation autocorrelation function $\overline{\Delta i(t)\Delta i(t+\tau)}$ where $\Delta i(t)= i(t)-\bar{I}$ provides the spectral density of the current fluctuations. However, two problems have to be solved. Firsty, the observation time can be very long if the frequency of operation is small (10 Ghz ~ 100ps!). Secondly, the Monte carlo technique introduces some numerical noise related to the time and space discretization scheme and to the number of particles introduced in the simulation. In order to give reliable results, the time and space meshes have to be small and the number of simulated particles has to be high which gives rise to problems related to the memory occupancy and computation time. For this reason, only few results have been published till now but interresting results concerning the MESFET noise modeling were recently obtained (Gonzales, 1995).

The MESFET and HEMT noise performance

From a general point of view, MESFETs and HEMTs are considered as two port. So, they can be represented by four noise parameters. These noise parameters can be either NF_{min},R_n and Y_{opt} or two correlated noise sources. The noise sources can be either current or voltage noise sources and simple transform formula can be found to pass from one representation to another one. For the manipulation of the noise sources in two port, it is convenient to use the noise correlation matrix technique (Hillbrand 1976).

The calculation of NF_{min},R_n and Y_{opt} is straighforward if the macroscopic noises and their correlation are known. In a first step, the two port is described using a chain representation. This representation is characterized by two noise sources i_n and e_n located at the input of the noiseless two port. Let $[C_{ic}]$ be the corresponding noise correlation matrix, we have

$$[C_{ci}]=\begin{bmatrix} \overline{e_n^2} & \overline{e_n.i_n^*} \\ \overline{i_n.e_n^*} & \overline{i_n^2} \end{bmatrix}=$$

$$4kT_0\Delta f \begin{bmatrix} Rn & \frac{NF\min-1}{2}-RnYopt^* \\ \frac{NF\min-1}{2}-RnYopt & |Yopt|^2 Rn \end{bmatrix}$$

In conclusion, a complete characterization of a noisy linear two port needs four parameters. These four noise parameters can be two correlated the noise sources or the minimum noise figure, the noise resistance and the optimum generator admittance. The modelling of the noise performance of any two port needs the following steps :

(i) calculation of the DC characteristics
(ii) calculation of the AC performance
(iii)introduction of the microscopic noise processes. Calculation of the impedance field and calculation of the macroscopic noise sources and correlation for given gate and drain terminations.
(iv)transformation of the noise sources into two sources e_n and i_n located at the input of the noiseless two-port.
(v)calculation of the four noise parameters NF_{min}, R_n and Y_{opt}.

MESFET and HEMT noise models

In order to reduce the number of noise parameters, it is possible to define some noise models that are based on the specific device behaviour for particular gate and drain terminations. According to the pioneering work of A. Van Der Ziel (Van Der Ziel, 1962,1963)), the specific structure of field effect devices allows us to reduce the number of independent noise parameters. For instance, the real part of the complex correlation coefficient between the gate and drain noise current sources can be neglected with respect to the imaginary part. This feature is due to the capacitive coupling between the active channel and the gate electrode (Cappy 1985,1988) As a consequence, three noise parameters, for instance the dimensionless parameters P, R and C are sufficient to describe the FET noise performance. More recently M. Pospieszalski (Pospieszalski, 1989) proposed a two-parameter-noise-model. In this model, it is assumed that for FETs, the gate noise voltage source is not correlated with the drain noise current source. So, the FET noise performance can be described by two "equivalent noise temperatures" T_g and T_d. This approximation was first derived from experiments and its validity was recently establishes usind a physical noise model (Danneville,1996). Since the gate temperature T_g is close to the ambient temperature, Pospeszalski's noise model is in agreement with the work of Gupta et al (Gupta, 1987,1988) which shows a good agreement over a wide frequency range between the measured noise parameters and those predicted from the equivalent circuit and a single frequency-

independent constant. It should be noted that Pospieszalski's two-parameter-noise-model and Gupta's one-parameter-noise-model can be easily connected to Van Der Ziel three-parameter-noise-model .

3-Noise modelling in device under nonlinear operation

For the design of high performance nonlinear circuits, it is of primary importance to develop nonlinear noise modelling. In fact, nonlinear is a very general term. In this part, it will be restricted to a time periodic large signal steady state of fundamental angular frequency ω_0. This noise analysis in a device under nonlinear operation is useful to understand the noise physics as well to develop models for the calculation of the noise figure of mixers or the spectral purity (PM-noise) of oscillators (Edson, 1960; Dragonne, 1968; Kurokawa 1968; Kerr, 1978; Siweris 1985; Rizzoli, 1989,1994; Heinen, 1991; Anzill , 1993).

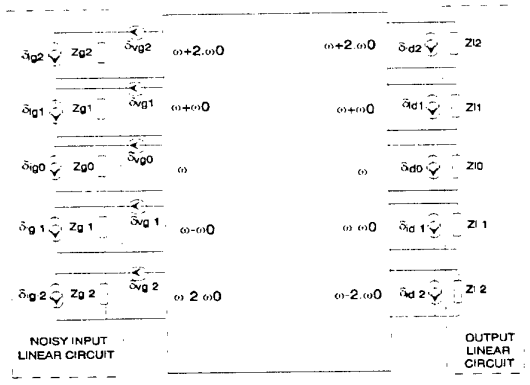

Fig 3. Representation of a noisy nonlinear two-port

It should be first emphasized that the noise signal are always very small as compared to the other signals. In that sense, a noise analysis is always a linear analysis. If we consider small deviations of the large signal steady state of fundamental angular frequency ω_0, the nonlinear device can be replaced by a noiseless linear multifrequency network described by its conversion matrix $[C_Y]$.For a noise description of a nonlinear device, a noise source has to be added at each port of the linear multifrequency network (Dragonne, 1968; Kerr, 1978,Rizzoli,1994).

From a noise point of view, the noise correlation matrix $[C'_N]$ completely describes the nonlinear device:

$$\left[C'_N\right]=\begin{bmatrix}\left[\overline{i_{1,k}\cdot i^*_{1,\ell}}\right] & \left[\overline{i_{1,k}\cdot i^*_{2,\ell}}\right]\\ \left[\overline{i_{2,k}\cdot i^*_{1,\ell}}\right] & \left[\overline{i_{2,k}\cdot i^*_{2,\ell}}\right]\end{bmatrix}$$

with $-n_h \le k \le n_h$ and $-n_h \le k \le n_h$.

Note that the size of $[C'_N]$ is $4x(2.n_h+1)x(2.n_h+1)$ that is $10x10$ for $n_h = 2$. In order to determine $[C'_N]$, a generalization of the IFM can be used as follows.

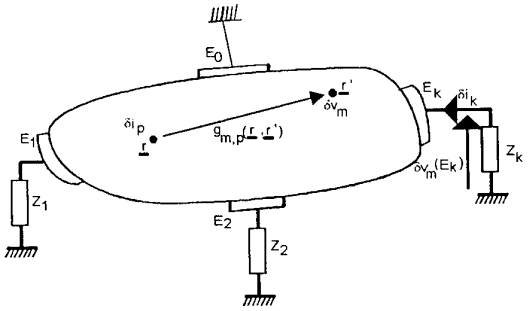

Figure 2 Noise analysis of a device under nonlinear operation

Let us consider a nonlinear device with several electrodes E_k (Fig.2). Each electrode is connected to a linear circuit. The device is driven by a large signal of fundamental angular frequency ω_o. We suppose that the large signal steady state is known. Due to the large signal, the physical quantities such as the current density $j(\underline{r},t)$, the electrostatic potential $v(\underline{r},t)$ and the carrier density $n(\underline{r},t)$ are periodic functions of fundamental frequency ω_o at any point of the device. For small perturbations of the steady state, the device can be replaced by a linear multifrequency network described by its conversion matrix.

Let us now consider a noise source $\delta i_p(\underline{r})$ at angular frequency $\omega+p\omega_0$ located in a volume $d\Omega$ at a point $\underline{r}$ in the device. At any point $\underline{r}'$ of the device, $\delta i_p(\underline{r})$ produces a noise voltage $\delta v_m(\underline{r}')$ at angular frequency $\omega+m\,\omega_0$ given by

$$\delta v_m(\underline{r}') = \sum_p g_{m,p}(\underline{r}',\underline{r}) i_p(\underline{r}) d\Omega \qquad (4)$$

$g_{m,p}(\underline{r},\underline{r}')$ can be calculated after development in Fourier series and linearization of the set of nonlinear differential equations describing the device. $g_{m,p}(\underline{r},\underline{r}')$ is just a form of Green's function and can be deduced from a perturbation analysis of the large signal steady state as long as a physical description of the device is known. Formula (4) can be applied at any point and especially at the device electrodes E_k. Assuming spatially uncorrelated noise sources, the cross-spectrum $<\delta V_m(\underline{r}')\delta V_n^*(\underline{r}')>$ can be deduced from (4) and integration over the entire device

$$\left\langle \delta V_m(\underline{r}') \delta V^*{}_n(r') \right\rangle = \sum_p \sum_s \int_\Omega g_{m,p}(\underline{r},\underline{r}') \left\langle \delta i_p(\underline{r}) \delta i_s^*(\underline{r}) \right\rangle g_{n,s}^*(\underline{r},\underline{r}') d\Omega \qquad (5)$$

This expression is valid for any $\underline{r}'$ and so it can be applied for any electrode. Formula (5) can be considered as a generalized form of Shockley's impedance field method to devices under non linear operation . At this step, a discussion on the cross-spectrum $<\delta i_p(\underline{r})\delta i^*_s(\underline{r})>$ is necessary.

(i) microscopic white noise sources

For the microscopic white noise sources (i.e. thermal noise, diffusion noise), the time constant associated to the noise process (typ. 10^{-13} s) is much smaller than the period of the large signal. The magnitude of the noise sources follows the time dependent state variables. The microscopic high frequency noise sources are modulated by the large signal and a noise power can be generated at any angular frequency $\omega+p.\omega_0$. In linear operation, the cross-spectrum $<\delta i_p(\underline{r})\delta i^*_s(\underline{r})>$ is given by (Nougier 1981,1991):

$$\left\langle \delta i_p(\underline{r}) \delta i_s^*(\underline{r}') \right\rangle = 4 q^2 \Delta f \, D(\underline{r}) n(\underline{r}) \delta(\underline{r} - \underline{r}') \delta_p^s \qquad (6)$$

where $D(\underline{r})$ is the diffusivity, $n(\underline{r})$ the carrier density and δ_p^s is the Kronecker's symbol (δ_p^s = 0 if s ≠ p and δ_p^s =1 if s = p). Under nonlinear operation the product $D(\underline{r}).n(\underline{r})$ is a periodic function of fundamental angular frequency ω_0. Assuming that the random function $\delta i(t)$ is simply modulated by the large signal, the cross spectrum $<\delta i_p(\underline{r})\delta i_s^*(\underline{r})>$ is given by (Dragonne, 1968) :

$$\left\langle \delta i_p(\underline{r}) \delta i_s^*(\underline{r}') \right\rangle = 4q^2 \Delta f \, H_{p-s} \delta(\underline{r} - \underline{r}') \qquad (7)$$

where H_{p-s} is the $(p\text{-}s)^{th}$ harmonic of the function $D(\underline{r},t).n(\underline{r},t)$. These coefficients are given by the large signal analysis.

(ii) microscopic low frequency noise sources

For the microscopic low frequency noise sources (i.e. generation-recombination noise, flicker noise) the situation is very different. The time constant associated to the noise process (typ. 10^{-3}-10^{-6} s) is much larger than the period of the large signal. The magnitude of the noise sources only depends on the DC value of the state variables. The microscopic low frequency noise sources are not modulated by the large signal. Formula (5) becomes :

$$\left\langle \delta V_m(\underline{r}') \delta V^*{}_n(r') \right\rangle = \int_\Omega g_{m,0}(\underline{r},\underline{r}') \left\langle \delta i_0(\underline{r}) \delta i_0^*(\underline{r}) \right\rangle g_{n,0}^*(\underline{r},\underline{r}') d\Omega$$

So, due to the frequency conversion, represented in (5) by the terms $g_{m,0}$ and $g_{n,0}$, that takes place in the device , the microscopic low frequency noise sources at frequency ω produce noise voltage at the electrodes at the frequencies $\omega+n.\omega_0$.

For the generation-recombination noise the cross-spectral density of the current density is given by:

$$< \delta j_0 \delta j_0^* >= K \frac{1}{1+\omega^2\tau^2}$$

In the case of flicker noise, the location of the noise sources is difficult. Part of this noise comes from the bulk (i.e. depleted layer, the conductive channel) and part of the surface. So, it is not simple to calculate the frequency conversion coefficient $g_{m,0}(\underline{r},\underline{r'})$ and additional work connected to experiments is still necessary. This point is important for the modeling of the PM noise of oscillators.

In summary, a noise analysis in a nonlinear device can be summerized as follows.
(i) calculation of the large signal steady state using HB technique for instance
(ii) Linearization and calculation of the conversion matrix
(iii) introduction of the microscopic noise processes. Calculation of the impedance field and calculation of the macroscopic noise sources and correlation for the nonlinear steady state.
(iv) calculation of the noise performance that is the noise figure for a mixer or the phase noise for an oscillator

4-Conclusion

The noise modelling of device under either linear or nonlinear operation can be carried out using Schockley impedance field method. This method can be used to define noise models as well as to study the device noise physics. A considerable amount of work was done to define reliable noise models for MESFETs and HEMTs under linear operation . On the contrary, no model exists to described the noise properties of devices under nonlinear operation which render difficult the design of low noise mixers and low phase noise oscillators. A lot of work has still to be done in this field!

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Optical Control of HFETs

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Abstract

During the last years, the Heterostructure Field Effect Transistor (HFET) has become of growing interest as an optical detector. Different models for description of the optical behaviour of HFETs are known from the literature. We show that the validity of the proposed models are strongly dependent on the actual device and process technology, respectively. The optical response of HFET devices can vary drastically with the incident average optical power and the applied drain-to-source voltage. Experimental results and reasons for this behaviour are given below.

Introduction

The gap between microwave and optics is getting smaller year by year. In monolithic integrated optoelectronic receiver circuits, high speed photodetectors with a high responsivity are needed. Another demand is a low-cost production with a high reliability and high yield, respectively. So, the number of process steps in production has to be kept low. This led a number of researchers [1] to the idea to use the active device itself as a photodetector, because it is already available without any further process steps.

In the year 1977, Baack et al. [2] suggested to use a GaAs MESFET as a high speed optical detector. Numerous different applications for such a detector have been proposed and examined. To implement such a detector in a circuit a model to describe the optical detection behaviour is needed. From the measurement of the optical response of the transistor [3], many information can be obtained.

Intensive investigations have been done to describe the optical behaviour of MESFETs and HFETs. The microwave performance of optically illuminated FET devices can be characterised by s-parameter measurements followed by the determination of the equivalent circuit elements. To get an idea of the optical performance, an analytical approach by solving the one-dimensional Poisson equation is adequate. Different approaches for modelling the behaviour of an optical FET detector have been presented in the literature [4-6]. However, these models were not able to describe the measured behaviour of the devices presented here.

During experiments we found a strong dependence of the slope of the optical response on the incident optical average power. The reason for this behaviour is found to be the trap dependent amplification of the incident optical signals by the photoconductor formed by the buffer layer of the HFET. Another remarkable fact was a strong dependence of the optical response on the applied drain-to-source bias voltage of the transistor. This can also be explained by the amplification of the primarily generated photocurrent by traps in the buffer layer of the transistor. The occupation time of these traps can strongly depend on the applied voltage.

As it was shown [7], traps may play a major role in the process of detection of optical radiation by MESFETs and HFETs. Different types of traps lead to different corner frequencies in the optical response. The basic mechanism behind the amplification caused by the presence of traps is called photoconductive gain. It has been shown earlier that the gain of each type of trap can strongly depend on the environmental conditions, e.g. the amount of incident average optical power [8-9] or the applied drain-to-

source bias voltage V_{DS} [10]. An empirical model will be given to describe the experimentally observed behaviour.

HFET Structure

The pseudomorphic HFETs were fabricated in the Fraunhofer Institute for Applied Solid State Physics in Freiburg, Germany [11]. The layers were grown on a s.i. 2" GaAs wafer by MBE. The vertical structure (Fig. 1) is as follows: a GaAs buffer including an AlGaAs/GaAs superlattice, a 10 nm $In_{0.25}Ga_{0.75}As$ channel, a 5 nm $Al_{0.2}Ga_{0.8}As$ spacer followed by a 1.7 nm wide GaAs quantum well with δ-doping embedded in the middle, and a 20 nm $Al_{0.2}Ga_{0.8}As$ layer. For the electron confinement, on the top of these layers follows the vertical structure for the formation of the FETs which consists of a 3 nm GaAs layer and a 3 nm $Al_{0.2}Ga_{0.8}As$ etch stop covered by a 30 nm n^+-GaAs cap layer.

The lateral structure of the device was realised by a dry etching process for the recess gates. The Ti/Pt/Au gate metallization is placed in the recess on the GaAs layer. The gate length is 0.25 µm and the gate width of the measured devices is 2x100 µm. The drain and source electrodes were evaporated on the n^+-GaAs cap layer. These ohmic contacts were alloyed down to the buffer layer above the superlattice. The source to drain spacing is 1.25 µm.

Dependence of the Optical Response on the Incident Average Optical Power

The HFETs were tested on-wafer. The device was illuminated by the end of a single mode fibre pigtailed to an Ortel SL1210C diode laser (λ = 840 nm). The laser was biased by a precision current source. The laser current was modulated by a superimposed rf signal produced by a generator. A reference signal of this rf-generator is fed to one channel of a sampling oscilloscope. The other channel is connected to the drain electrode of the HFET via a bias-T to measure the output voltage V_{out}. The drain bias voltage V_{DS} = 2 V is also connected to the HFET via the bias-T. The gate electrode is grounded (V_{GS} = 0 V).

During our experiments on direct optically injection locked oscillators, we found a dependence of the locking range on the distance between the end of the fibre and the device. The locking range increased with decreasing distance, due to a better coupling of the light into the active regions of the device. Astonishingly, the dc drain current decreased by closer illumination. This behaviour was also observed with a single HFET in the experimental setup. The relative optical response of the HFET is depicted in Fig. 2. The only parameter that has been varied was the distance h between the end of the fibre and the wafer. The strong decrease in the response for frequencies below 80 kHz is due to the bias-T. Above a modulation frequency of approximately 200 kHz the output voltage V_{out} is higher in the case of the short illumination distance of approximately h_1 = 1 µm. Below a frequency of 200 kHz the device behaves vice versa. Another remarkable fact is the slope of the response that changes with the distance of illumination. In a long distance of illumination (h_2 = 1 mm) the response decreases with approximately 6 dB per decade. The short illumination distance leads to a response that can be divided in four regions with different slopes.

The behaviour can be explained by traps in the buffer layer of the HFET. The major part of the relevant absorption of the light takes place in the buffer layer (GaAs buffer I). The light generated electron hole pairs are separated by the applied drain source voltage V_{DS}. While some carriers, e.g. the holes, are trapped in different kinds of traps with different energy levels and different characteristic capture times, the other kind of carriers may be taken from the ohmic contact. This leads to an amplification, which is known as gain of photoconductors with traps. Because of the different kinds of traps, there are different knee frequencies in the response [7]. The amplification by these processes depends on the number of traps being available. If the incident average optical power (dc-light) is increased (e.g. by decreasing the distance of illumination) more and more traps are occupied by carriers generated by the dc-light, so that they cannot contribute to the amplification of the modulated light. Fig. 3 gives the dependence of the output

voltage V_{out} on the average optical input power P_L (h = 1 mm, V_{DS} = 2 V, f = 100 kHz), showing a strong decrease in the output signal voltage by increasing the average optical power. The optical response in a distance of h = 150 µm is given in Fig. 4. Here, the output signal also shows a strong decrease with increasing average optical power. Furthermore, the slope of the response is changing while the dc-light is varied. A simple model (Fig. 5) consisting of superimposed current amplifiers is able to describe the observed behaviour. The measured response as it is shown in Fig. 6 for a short distance operation can be simulated very well by our model.

Dependence of the Optical Response on the Applied Voltage

Again, the HFETs were tested on-wafer. The experimental setup is depicted in Fig. 7. The device was illuminated by the end of a single mode fibre pigtailed to an Ortel SL1210C laser diode (λ = 840 nm).

The illumination situation and the setup are similar to the on mentioned above. The drain bias voltage V_{DS} is also connected to the HFET via the bias-T. The gate electrode is grounded via a 50 Ω resistor (V_{GS} = 0 V). The distance between the end of the fibre and the wafer was 150 µm. The average optical output power of the laser was 1.6 mW.

During our measurements of the optical response of a pseudomorphic HFET-photodetector, we observed a dependence of the response on the drain bias voltage V_{DS}. Fig. 8 shows the measured responses for V_{DS} = 2 V and V_{DS} = 4 V, respectively.

The low frequency cutoff (f < 100 kHz) is due to the bias-T in the setup. Below a frequency of approximately 4 MHz, there is a strong difference in the slope of the two curves. In case of V_{DS} = 4 V, the response of the optical HFET detector at a frequency of 100 kHz is approximately 5 dB less than at V_{DS} = 2 V. This behaviour was confirmed by measuring the output signal V_{out} at a fixed generator frequency (f = 100 kHz), while the drain bias voltage was varied continuously (Fig. 9). At a voltage of V_{DS} ≈ 2.3 V the output signal has a maximum.

The i-v characteristics of the device in the dark and under illumination also show a strong dependence of the optically generated current I^*_{DS} on the applied drain-to-source bias voltage (Fig. 10). The gate voltage was V_{GS} = -0.8 V ... +0.6 V. The distance between the end of the fibre and the wafer was 1 mm. The optical output power at the tip of the fibre was 1.6 mW. While there is a slight kink effect in the drain current without light, this effect vanishes under illumination. A closer look at the output conductance $G_{DS} = \partial I_{DS}/\partial V_{DS}$ confirms this estimation. The curves depicted in Fig. 11 are calculated from i-v characteristics at a gate bias of V_{GS} = 0 V. The local maximum in G_{DS} at approximately 2 V indicates that the kink effect is present in the dark. It disappears under illumination.

Different kinds of traps in the device are responsible for a frequency dependent amplification of the primarily generated photocurrent [7, 12]. It is supposed that holes trapped by these traps are compensated by electrons which are continuously supplied by the ohmic contact, necessarily leading to an increase of the measurable drain source current. The existence of different kinds of traps with different energy levels and different characteristic occupation times result in superimposed responses versus frequency with regions of different slopes.

Different effects (e.g. temperature, intensity of light, and applied voltage) influence the number of traps being available for the amplification of the primarily generated photocurrent. If these traps are occupied by other than optically generated holes, these traps will not contribute to a photoconductive gain and therefore reduce the gain. In [13-14], it is postulated that the kink effect in the output i-v characteristic of the HFET arises from impact ionisation in the 2-DEG. The holes generated in this case move to the buffer layer and travel to the drain electrode. On their way, they may be trapped in the buffer, leading to the described reduction of gain. The Poole-Frenkel effect is another reason for the decrease of the gain. The decrease of the activation energy of the trap due to an applied voltage (here: V_{DS}) may lead to a reduction of

the characteristic occupation time of the trap and, thus, to a reduction of the gain.

It is difficult to give an analytical model for the observed detection behaviour. Too many parameters concerning the traps are unknown or drifting. In [9], Romero et al. Reported about an analytical model for the photodetection mechanisms in HFETs. With some of their devices, a dependence of the response on the optical average power was also observed. The variation of the low frequency gain was explained by the variation of the hole lifetime. To apply this model to our transistors, the presence of different variable lifetimes or capture times, respectively, have to be taken into account.

Conclusion

The presented results show that there can be a strong difference between the optical dc and rf response caused by the amplification process based on an photoconductor with traps and ohmic contacts. At frequencies above 1 GHz, however, these amplifications vanish and it is recommendable to illuminate the optical HFET detector from a short distance or to focus it on the active regions.

A strong dependence of the optical response on the drain source bias voltage was observed. This behaviour was also explained by amplification processes caused by traps. These processes may be saturated or decreased by several other effects leading to a reduction of the gain.

With a very simple model the dependence of the optical response on the average optical power and the drain-to-source voltage can be described. A very well suited model [9] has to be extended by different trap capture times to be applicable to the characterised HFETs.

Acknowledgement

The authors would like to thank T. Jakobus for his expert technology management. Special thanks are due to R. Bosch and M. Ludwig for their assistance in characterising the devices. One of the authors (A.B.) wishes to thank all his former colleagues at the Fraunhofer Institute (IAF) in Freiburg for the instructive and pleasant past years.

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Figures

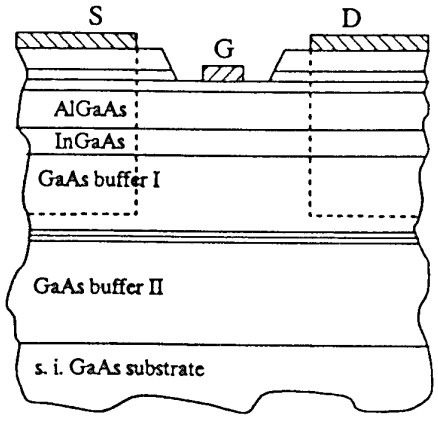

Fig. 1: Layer structure of the HFET.

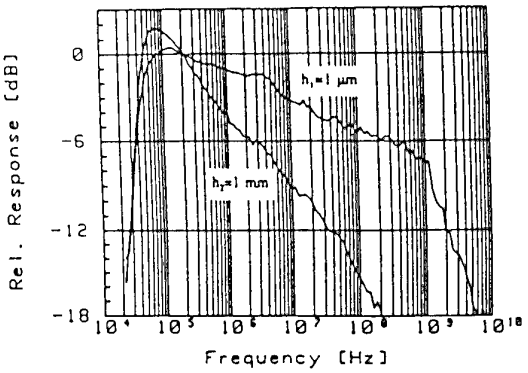

Fig. 2: Optical response of the HFET in different distances of illumination.

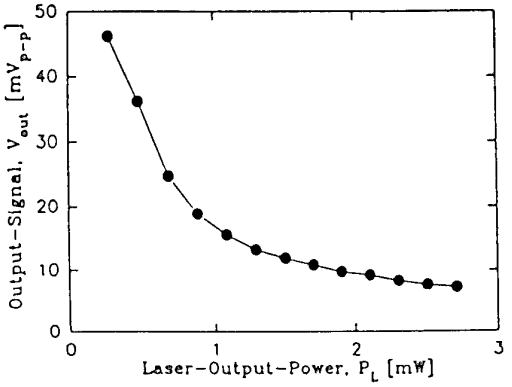

Fig. 3: Output signal of HFET vs. Laser output power.

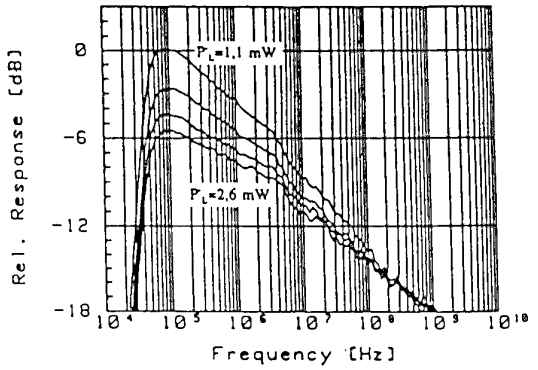

Fig. 4: Optical response of the HFET with the average laser output power as parameter.

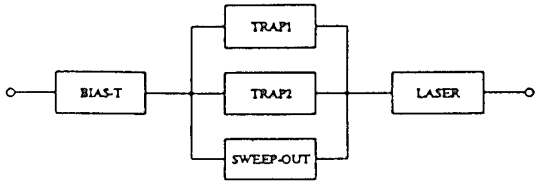

Fig. 5: Model to describe the different slopes in the optical response of the HFET.

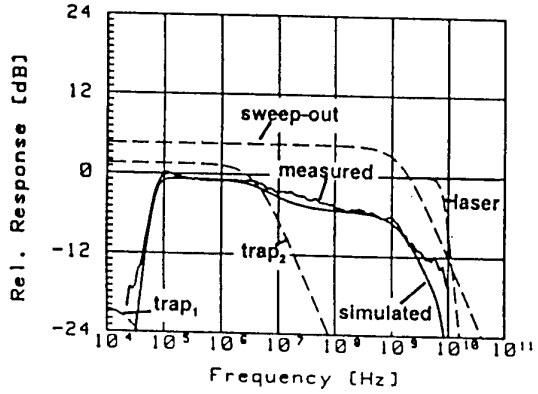

Fig. 6: Comparison between calculated and measured response.

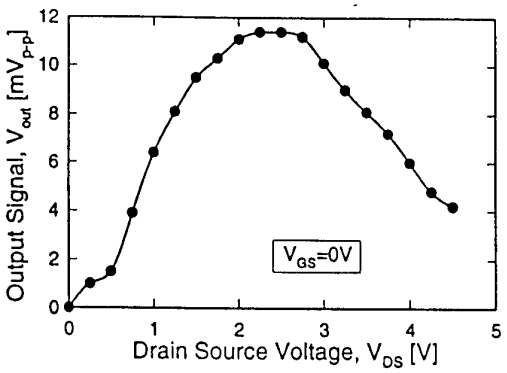

Fig. 9: Output signal V_{out} of the HFET vs. Drain source voltage V_{DS}.

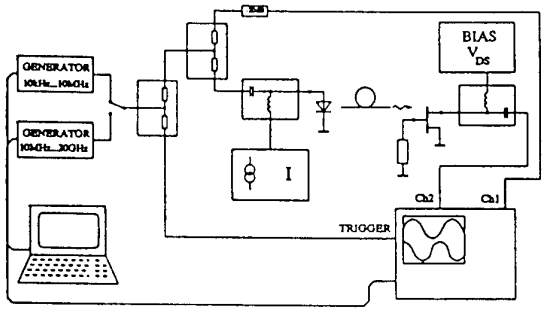

Fig. 7: Experimental setup

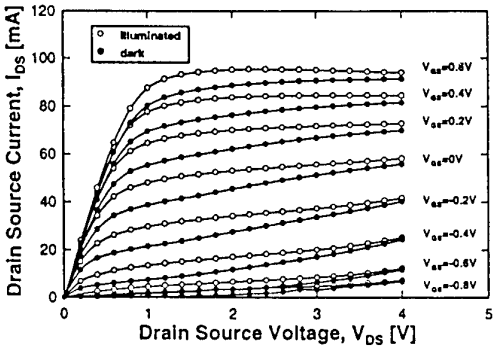

Fig. 10: DC i-v characteristics of the pseudomorphic HFET.

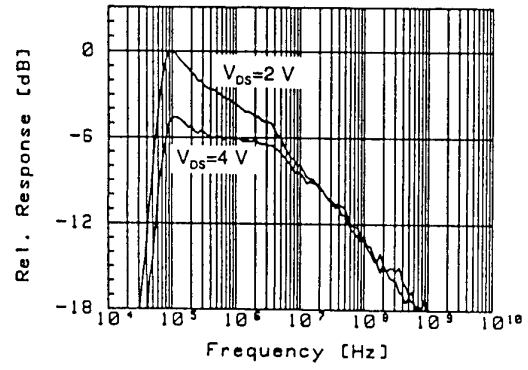

Fig. 8: Optical response of the HFET at different drain source voltages V_{DS}.

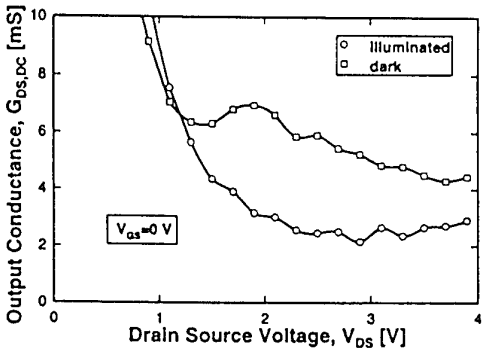

Fig. 11: Output conductance G_{DS} vs. Drain-to-source voltage V_{DS}.

Design and Fabrication of PINFETs for Optical Receivers

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Abstract

The deployment of high-speed optical fiber transmission systems has increased the need for an effective interface between optical fiber and optical receiver electronics. Optical communication systems with data rates ranging upto 10 Gb/s and higher require optical receivers with low noise and high speed of response. In this paper, the design considerations and structural details of PINFETS based on the state of the art will be presented.

I Introduction

An optical receiver basically consists of a photodetector and a low noise electronic preamplifier attached to it. These two components can be achieved in a hybrid or integrated mode. Currently the emphasis is on the development of device structures and fabrication technologies which give wide bandwidth, high gain and high speed. The integrated approach is proving to be more suitable to achieve the above specifications. The block diagram of a photoreceiver is shown in Fig. 1.

II Photodetector

It is a device which converts the received optical power into electrical signal. Light intensity at the end of an optical link is very low (typically nW to pW). The basic requirements of a photodetector are: (1) high conversion efficiency at the operating wavelength range. (2) high speed of response to prevent distortion. (3) minimum additional noise must be introduced.

From the VI characteristics of a p-n junction we find that current increases linearly with optical power in the reverse biased mode. So a reverse biased p-n junction can be used as a photodetector. The important parameters of a photodetector are: (1) cutoff wavelength (2) absorption coefficient (3) quantum efficiency & (4) responsivity.

The response time of a photodiode depends on (1) carrier diffusion time (2) carrier transit time & (3) junction capacitance interacting with external load resistance. To reduce the carrier diffusion time we have to use a p+ region considerably less than a diffusion length. But quantum efficiency comes down with reduction in size of the absorbing layer. So there is a trade-off between quantum efficiency and transit time.

A reverse biased p-n junction suffers from the problems of high junction capacitance and large diffusion time. So a p-i-n structure is preferred as the capacitance is reduced due to the intrinsic layer. Its structure is simpler and more stable.

InGaAs is the preferred material for detectors operating at long wavelengths (1.3μm to 1.7μm) due to its low bandgap and small leakage current. The proportions of In and Ga can alter the bandgap. For example $In_{0.53}Ga_{0.47}As$ has a band gap of 0.47 eV which gives a cutoff wavelength of 1.65μm. Its other advantages are high electron mobility & low voltage operation.

III Pre - Amplifiers

They are basically of two types: (1) high input impedance and (2) transimpedance. For the former, bandwidth is low due to which a compensation network is required at the output. The transimpedance preamplifier is preferred for its high bandwidth due to negative feedback. It also has a high dynamic range and no compensation network is required.

A minimum signal to noise ratio is required at the output of an optical receiver. The noise sources in amplifiers include: (1) Thermal noise associated with the channel conductance (2) Shot noise associated with the gate leakage current & (3) Induced gate noise due to charge fluctuations in the depletion layer width. The noise sources in the photodetector include: (1) quantum noise (2) thermally generated dark current & (3) surface leakage current.

IV Opto Electronic Integrated Circuits (OEIC)

Monolithically integrated photoreceivers are being investigated intensively due to their potential for reducing the size and cost of optical receivers. They also provide greater reliability, easier manufacturability and assembly, high gain & high sensitivity. The real challenge lies in the growth of dissimilar device types (detectors & preamplifiers) on a single substrate. The p-i-n detector requires thick absorbing InGaAs layer while the FET requires a thin layer. Also the current flow is vertical in the p-i-n photodiode but horizontal in the FET.

The photodiodes must be optimised for high responsivity, low capacitance and high speed. The design of transistors must be optimised to suppress short channel effects and to reduce output conductance and gate source capacitance. The optimum designs of the p-i-n photodiode and the JFET in the OEIC are considered separately.

V Design of p-i-n diode

The cross-sectional view of a p-i-n diode is shown in Fig. 2. The top illuminated structure is preferred as it allows easier coupling of light into the device and easier packaging of the overall receiver. The layer thicknesses are important design parameters. The thickness of the absorbing p-type layer is governed by a trade-off between sheet resistance and diffusion time. The heavily doped n type layer is made of InP as it simplifies fabrication process. The transparency of InP at the operating wavelength prevents absorption in this layer. For a data rate of 10 Gb/s, the photodiode capacitance must be below 50 fF and the temporal response (determined by transit time and RC loading effects) must be below 20 ps. These two effects are contradicting. If we reduce the thickness of the depletion region to reduce the transit time, we increase the photodiode capacitance. The thickness affects the quantum efficiency. All these factors must be optimised.

VI Performance of Photodetector

A plot of cut-off frequency and quantum efficiency is given in Fig. 3. From the graph, we see that for thin depletion regions the capacitance is large and the bandwidth is dominated by RC effects. For thick depletion regions, the bandwidth is dominated by transit time effects. At point A, the speed of response is good but the quantum efficiency is very low. At point B, the speed of response is limited but the quantum efficiency is high.

VII Device structure of FET

JFET transistors with bulk channels are chosen due to their fabrication compatibility with p-i-n photodiodes. InGaAs grown lattice matched to InP is the material of choice. The cross section through the JFET with the step doped channel doping profile is shown in Fig. 4. The channel is composed of (a) an undoped InGaAs spacer

section characterised with a background doping Ns. (b) a highly doped InGaAs channel section with doping level Nc. The undoped spacer is introduced in order to minimise band to band tunneling at the gate pn junction. To achieve low contact resistance, the drain and source contacts are deposited through windows etched in the undoped layer. Compared to conventional uniform doped channel JFETs, these have improved cut off frequencies. The gate field is reduced due to which the gate leakage current reduces.

VIII Idealized Model of JFET

An idealized model of the JFET used for analysis is shown in Fig. 5. In region 1, the gradual channel approximation is employed i.e the superposition of longitudinal and transverse fields. In region 2, the two-dimensional Poisson's equation is used to determine the field and potential distributions.

The fabrication technologies used are: (1) Liquid Phase Epitaxy (LPE) (2) Vapour Phase Epitaxy (VPE) (3) Molecular Beam Epitaxy (MBE) (4) Low pressure metal organic vapour phase epitaxy (LP-MOVPE). Of these, the LP-MOVPE technology is preferred because of the ability to produce wide area uniform growth and abrupt junction profiles. The cross-sectional view of the integrated photoreceiver is given in Fig. 6.

The sensitivities at different bit rates are compiled in Fig. 7. For comparison, the performance of the best hybrid receivers is also indicated in the plot.

IX Conclusions

OEIC receivers offer high sensitivities and are highly feasible. Achievement of monolithic integration where the photodiode layers are grown on top of the transistor layers allow individual optimisation of photodiodes and JFETs. The photodiodes are optimised for high efficiency, high speed of response and low capacitance. The JFETs are optimised for low output conductance, low gate leakage current and high transconductance. By introducing voltage adjustable feedback, fabrication tolerances can be overcome to operate over a wide range of bit rates. Power dissipation can also be minimised. These low cost high performance photoreceivers are likely to be used in a wide range of applications concerning optical communication systems.

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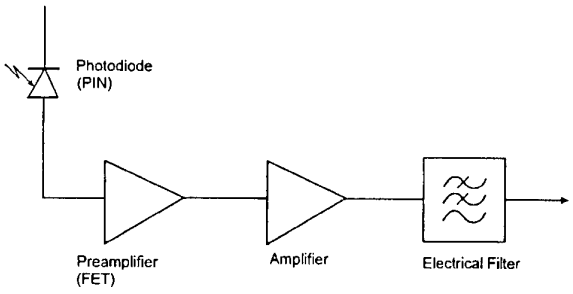

Figure 1. The block diagram of an optical receiver.

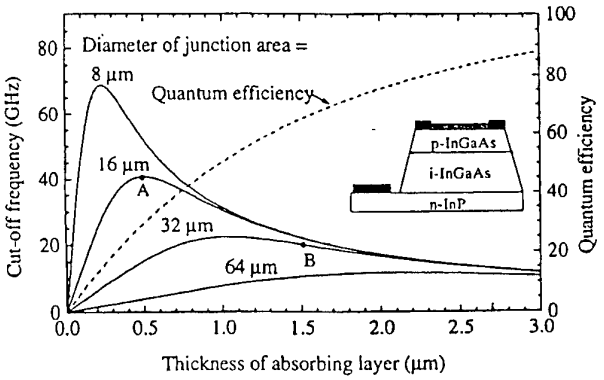

Fig. 3. Cut-off frequency and quantum efficiency versus width of depleted layer for various diameters of top illuminated InGaAs/InP photodiodes. After [1].

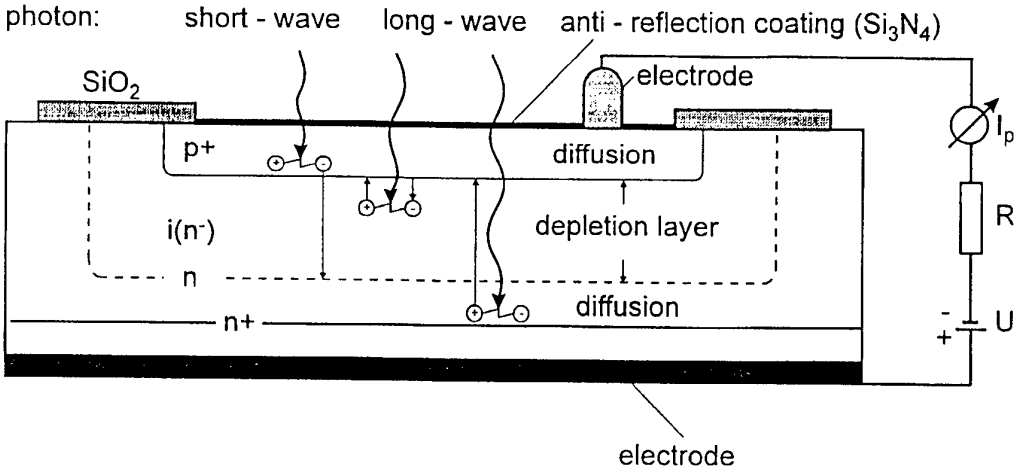

Figure 2. The cross sectional view of a p-i-n diode.

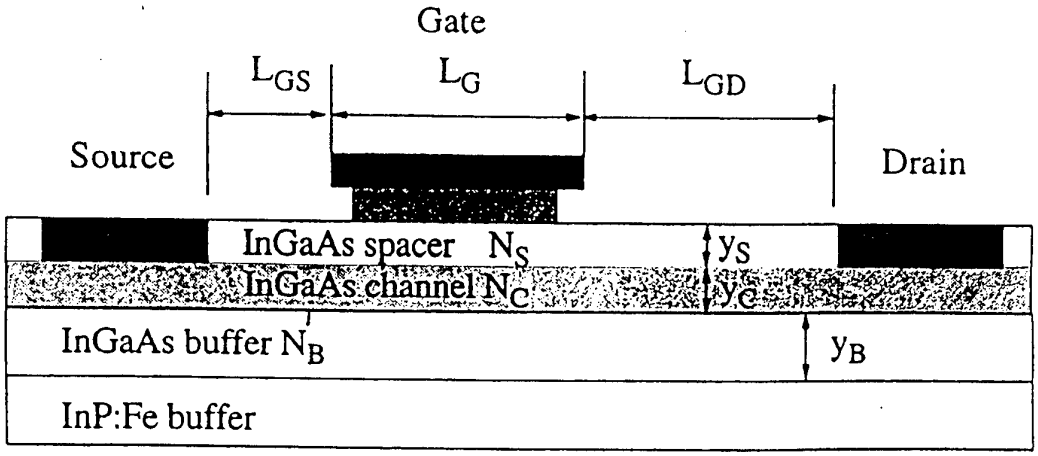

Figure 4. Cross sectional view of the InGaAs JFET with step doped channel doping profile. After [1].

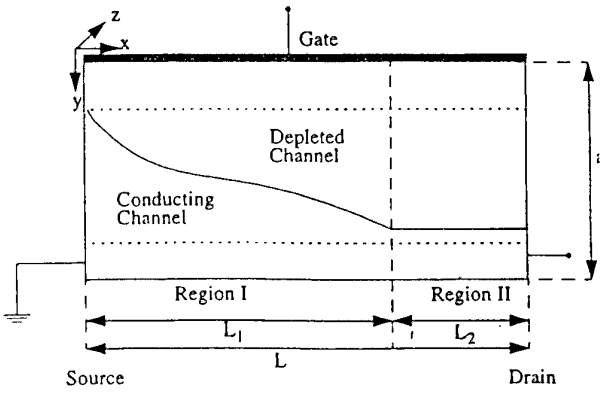

Figure 5. Idealized model of the JFET. After [1].

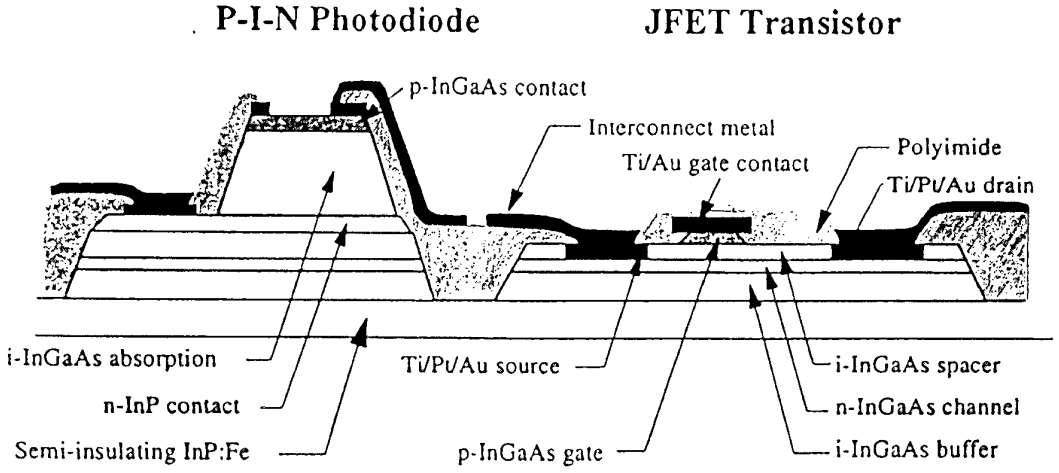

Figure 6. Cross sectional view of InGaAs/InP p-i-n JFET Integrated Receivers. After [1].

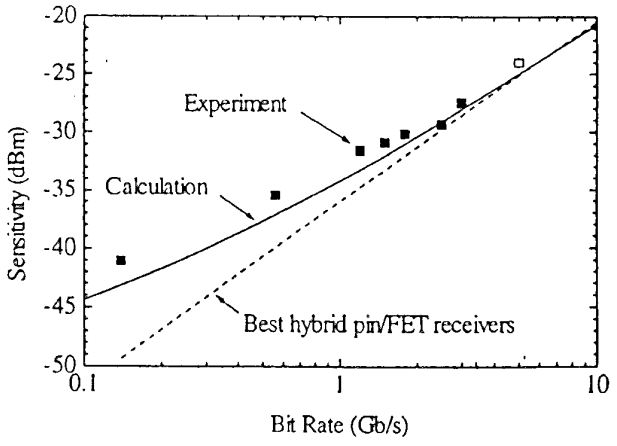

Figure 7. Sensitivities at different bitrates. After [1].

Accurate Nonlinear Modeling Based on Reliable On-Wafer Characterization

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Abstract

This paper presents some results of our accurate GaAs FET modeling approach based on reliable on-wafer characterization for the development of RFICs. An experimental modeling approach with conservative charge and current sources extraction is studied. Then an analytical extraction of bias dependent gate and source resistances from measured multi-bias S-parameters is presented. Finally, a new empirical model for GaAs FET is introduced. Results are presented and compared with the state-of-the-art models in conventional DC, S-parameter and harmonic performance.

I. Introduction

With the emerging wireless communication market, MMICs have found their way into the commercial market and will continue to grow in this area. These new markets of radio frequency ICs (RFICs) require design of high performance circuits and modules at low cost. This target is achievable by cutting down the design iteration with employing advanced CAD tools extensively and aiming at "first-pass" design success. To be successful in this approach, accurate and well-tested device models for both active and passive components are fundamental. Moreover, accurate models must be obtained from reliable real-world device characterization and model parameter extraction. To provide reliable device models for the RFIC design and to improve model accuracy constantly, the Institute of Microelectronics (IME) in Singapore has recently established an advanced RF modeling system consisting of Cascade Summit Probing, HP 8510C VNA with MDS & IC-CAP software and Focus Microwave automatic tuners etc. (Fig. 1) [1]. Currently, RFIC chip set for 1.9 GHz PCS/PHS handsets has been successfully developed with first-pass using OKI Electric Industry (Tokyo, Japan) GaAs process. The chip set includes low noise amplifier, down-converter, up-converter, power-amplifier and switch. The challenging single chip solution for RFIC transceivers is on-going. This paper presents some of our new efforts and results in accurate RF device modeling approaches based on reliable on-wafer real-world characterization. In addition to the extraction and comparison of commercially available device models such as Curtice Cubic [2], HP Root [3] and HP EEFET3 [4], we also developed our own empirical model for GaAs FET nonlinear circuit simulation.

II. Experimental Modeling

For the reason of its excellent small signal data-fitting and technology-independent advantages, quasi-static experimental modeling approach which was first proposed by Willing and Rauscher in 1979 [5] has gained great interest and intensive research has been carried out in the last decade. Prof. Kompa and his group are very active in this area [6,7]. Currently only HP Root model which belongs to experimental modeling is commercially available in CAD. Motivated by its theoretically high accuracy, our primary research on nonlinear model development was focused on this technique.

The major difficulties in applying the experimental modeling technique is the consistency problem, such as the unique determination of bias dependent small-signal model parameters and the consistent correlation between small-signal and large-signal model elements. An effort was made to solve this persistent problem. The approach is summarized as follows:

Firstly, improved consistent nonlinear and linear FET models as shown in Fig. 2 and Fig. 3 are constructed. The small-signal equivalent circuit is derived consistently from the nonlinear model. Compared to publications, the improvement was made by including an important parameter τ, the transit time delay under the gate [8]. Then the bias-dependent intrinsic small-signal model elements are extracted by multi-plane data-fitting technique [9]. The next step is the generation of nonlinear current and charge sources from the multi-bias small-signal elements. Usually this will be carried out by direct integral of extracted small-signal elements. However, we have experienced that it is quite path de-

pendent. For example, Fig. 4 shows the different results of drain source current obtained by two different integral paths where path 1 starts from (0,0) passing $(0,V_d)$ to (V_g,V_d) and path 2 starts from (0,0) passing $(V_g,0)$ to (V_g,V_d). This is because the multi-bias small-signal model elements which are directly extracted from S-parameters are not conservative. To overcome this conservation problem by integration, we use the spline function for each nonlinear source. The coefficients of spline function are determined by an optimization procedure which minimizes the difference between the extracted small-signal elements and the derivations of the spline function [10]. In this way, promised nonlinear current and charge sources are obtained which fit the measurements quite well. For example, Fig. 5 shows the nonlinear drain source current generated which agrees well with the pulsed measurement. However, the application of this technique in CAD for RFICs is very limited. First of all, it is quite time consuming and a large data-base is required. Moreover it is difficult to include the scaling feature which is important for RFIC design and some process information related parameters such as pinch-off voltage are not included in the model. There is little room for any improvement if the modeling result is not satisfactory. Furthermore, based on our experience with HP Root model, this kind of nonlinear model is only valid for the common source configuration operating in normal bias condition. This is because the data-base is obtained in such a condition.

III. Bias Dependent R_g and R_s

Accurate determination of the extrinsic series parasitics is extremely important for an accurate device modeling. There are several techniques reported in the literature to measure and extract those parasitic resistances from different operating conditions [11-15]. However, these techniques would generate different results if careful study is performed. For a modeling engineer, it is common use to select a compromised value according to his experience in the practice of parameter extraction. All of the techniques are based on one assumption that the extrinsic series resistances are bias independent. However, it is physically understood that the parasitic resistances are bias dependent [16]. Bias dependent resistances are also reported from numerical simulation and dc measurement or optimization extraction [17,18]. In order to have a high quality picture of this bias dependent behavior, we have applied the multi-plane data-fitting technique [8] to extract the bias dependent R_s and R_g from measured S-parameters. To avoid the optimization inherent local minimum problem and to get an unique solution analytically, we have modified the standard 15-element small signal equivalent circuit as shown in Fig. 6. The basic modification in the equivalent circuit is removing the channel resistance R_i by introducing a new time delay parameter τ_m $(=C_{gs} R_i)$ in the voltage controlled current source. Thus the effect of R_i is considered separately in the bias dependent R_g and τ_m. With this simplification, the analytical extraction of intrinsic elements is possible to include R_g and R_s uniquely from the measured multi-bias S-parameters. Fig. 7 and Fig. 8 show the analytical extracted gate and source resistances for a 0.5-μm MESFET. These figures clearly show the bias-dependent behavior of the resistances. It is interesting to note that R_s and R_g approach the fixed values of 1.7 Ω and 6 Ω when gate is biased around pinch-off. These fixed values are mainly contributed by ohmic contact resistance and gate metallization as well as the bulk resistance in the active N-layer. As gate bias increases, the channel begins to conduct current and depletion region decreases. Thus the bulk resistance increases which increases the R_g and R_s. A relatively stable area for both resistances is the saturation region (V_{gs}=-1.5 to 0 V, V_{ds}=1.75 to 3 V in this case). In this region the resistances are relatively less sensitive to the bias voltages. Our results show that the resistances extracted at pinch-off or cold condition or forward condition are far from those extracted at saturation region. This would explain why different techniques currently applied or reported from some specific bias condition are not consistent with each other. Basically all the values extracted at specific conditions can only be used as a reference. They should be carefully examined before they are further used in de-embedding. The reliable values are obtained from saturation region.

IV. A New Empirical Model

Based on the experience obtained from above mentioned modeling research work and in performing model parameter extraction for the Curtice Cubic model, HP Root model and EEFET3 model using commercial modeling software IC-CAP for a variety of GaAs FETs, HEMTs, pHEMTs and DH-pHEMTs, we have recently developed our own empirical model for GaAs FETs in nonlinear circuit simulation. Our experience shows that empirical models are much easier to implement for CAD application than the data-based models. Moreover, it is the only way to implement user-defined model in commercial CAD tools, such as MDS or Libra. The motivation of developing the empirical model is driven by the fact that the existing models may not satisfy the demands of a variety of circuits. For example, all the existing MESFET models in MDS cannot correctly predict the behavior of FET across pinch-off for SPDT switch application.

Our new empirical model uses the same equivalent circuit as that of EEFET3 as shown in Fig. 9. For the drain current, we have simplified the EEFET3 model with less empirical model parameters but keeping comparable accuracy based on the reliable on-wafer

characterization data for a variety of transistor types. The drain current source is proposed as follows:

$$I_d = I_{dso} \bullet (1-\cos\theta)^Q \bullet \tanh(\alpha V_{ds}), \quad (1)$$

$$\theta = 1 - V_{gs}/V_T, \quad (2)$$

$$V_T = V_{T0} - \gamma V_{ds}, \quad (3)$$

$$I_{ds}(V_{gs}, V_{ds}) = \frac{I_d}{1 + p_{eff} V_{ds} I_d}, \quad (4)$$

where I_d is the drain current before incorporating into the thermal model, V_{gs} and V_{ds} are the intrinsic gate and drain voltages. I_{ds} is the drain current after it is incorporated into the thermal model. I_{dso}, V_{TO}, Q, α, γ and p_{eff} are the model fitting parameters. $(1 - \cos\theta)^Q$ is used to model the non-square law behavior of the drain current with respect to the gate voltage.

It is noticeable that the characteristic of I_{ds}~V_{gs} is neither a pure quadratic law near pinch-off nor a linear law at larger drain current. These effects have not been accurately described in previous models [2,19-22]. To improve the accuracy, a cosine function in our model is adopted together with the exponent function to represent the relationship of the drain current with respect to the gate voltage. This new function enables not only a good global fit to the measured characteristics, but also a good tracking on the higher order behavior of the device. The exponent parameter Q is adjustable to fit the non-square law dependence of the characteristic of I_{ds}~V_{gs}. Another benefit of employing the cosine function to describe the characteristic of I_{ds}~V_{gs} is in its smooth transitions when $V_{gs}=V_T$ and $V_{gs}/V_T=(1-\pi/2)$. These smooth transitions could be used to represent the transition of characteristics of I_{ds}~V_{gs} at pinch-off and forward gate.

To improve the output conductance fit at the low currents, the pinch-off potential V_T is modified to account for a drain-source voltage dependence by introducing a factor γ. Such modification is useful to eliminate the cut-off of the drain current existing in Curtice Cubic, Curtice-Quadratic and Statz models. The approach has been noted by the previous workers [21,22]. The thermal effects are described by incorporating Canfield thermal model [23] in our model.

Frequency dispersion model $I_{db}(V_{gs}, V_{ds})$ is constructed in a similar way as that of EEFET3. Small-signal RF transconductance and output conductance are used in model parameter extraction.

For the gate charge model, we have modified the Statz charge model [20] by introducing a new exponent parameter Z replacing the square-law dependence on V_{gs} and V_{ds} in Statz model. The new charge model Q_g is given by

$$Q_g(V_{gs}, V_{ds}) = C_{gs0} \frac{V_{bi}}{1-Z} \left[1 - \left(1 - \frac{V_{new}}{V_{bi}} \right)^{1-Z} \right] + C_{gd0} V_{eff2}. \quad (5)$$

The gate capacitances C_{gs} and C_{gd} are given by

$$C_{gs} = \left(\frac{C_{gs0} K_2 K_1}{(1 - V_{new}/V_{bi})^Z} + C_{gd0} K_3 \right) \quad (6)$$

$$C_{gd} = \left(\frac{C_{gs0} K_3 K_1}{(1 - V_{new}/V_{bi})^Z} + C_{gd0} K_2 \right) \quad (7)$$

where K_1, K_2, K_3, V_{eff2}, V_{new}, C_{gs0}, C_{gd0}, and V_{bi} are same as those in Statz model [20]. Z is the new model parameter. If Z is set to be 0.5, the model is resembled back to Statz model.

The principle for the gate forward conduction and breakdown model follows EEFET3 [4].

The above described new empirical model has been implemented and tested in HP IC-CAP for model parameter extraction and in MDS for nonlinear circuit simulation. Fig. 10 - Fig. 13 are some plots which clearly demonstrate the capability and accuracy of our model in comparison with other well known models.

V. Conclusions

Recent effort of accurate device modeling for RFIC design carried out at the Institute of Microelectronics, Singapore is reviewed. Some typical modeling results are presented for (i) a consistent large and small signal model based on experimental modeling approach; (ii) bias dependent R_g and R_s extraction and analysis from multi-bias S-parameters; and (iii) a new empirical model for GaAs FETs which features using simple expressions with fewer model parameters to predict accurate linear and nonlinear device performance.

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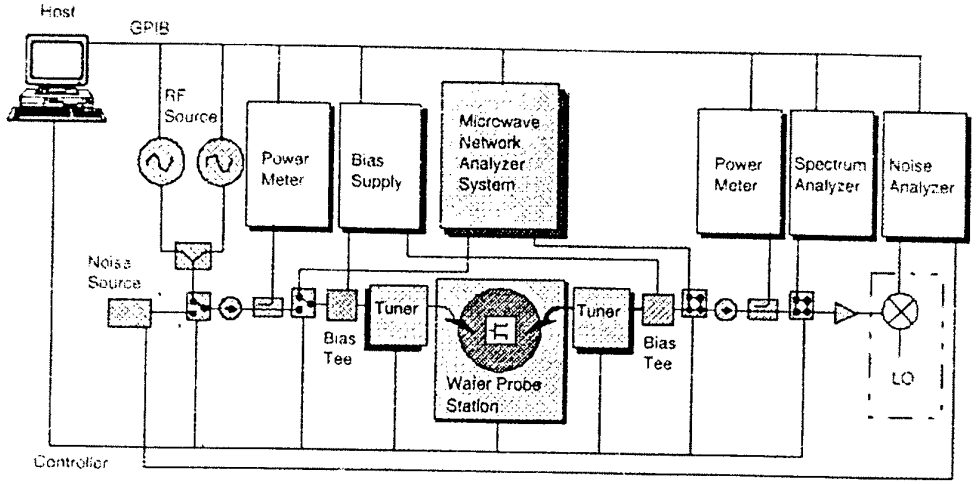

Figure 1: RF Modeling system established in IME.

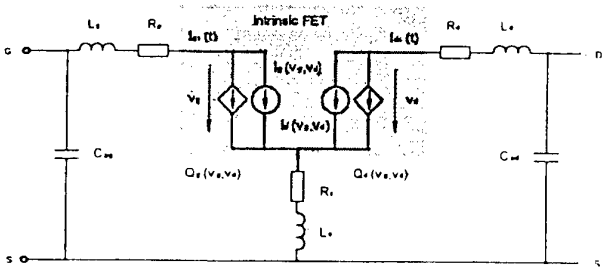

Figure 2: Proposed charge and current source conservative FET model including parasitic elements

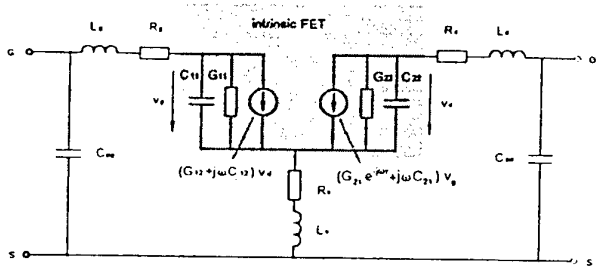

Figure 3: Small signal equivalent circuit derived consistently from Figure 2.

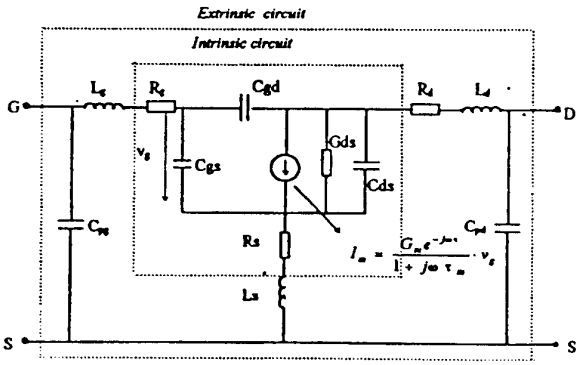

Figure 6: Simplified FET small signal equivalent circuit where R_s and R_g are assumed to be bias-dependent

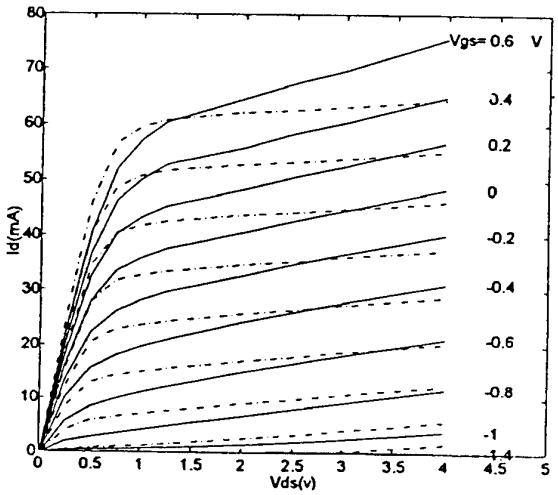

Figure 4: The instantaneous drain current calculated by integration method with different integral paths.

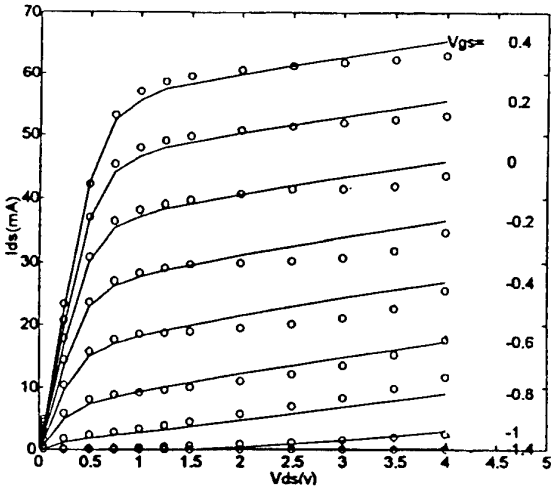

Figure 5: Large signal drain current obtained as proposed approach. The dots denote the measured data.

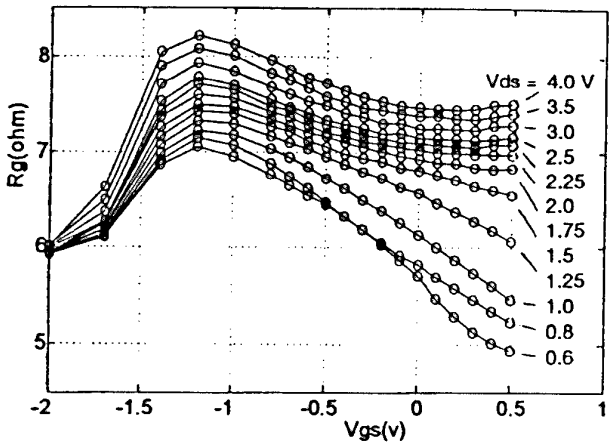

Figure 7: Extracted gate resistance of a 0.5 µm (100x2) GaAs MESFET as function of bias conditions

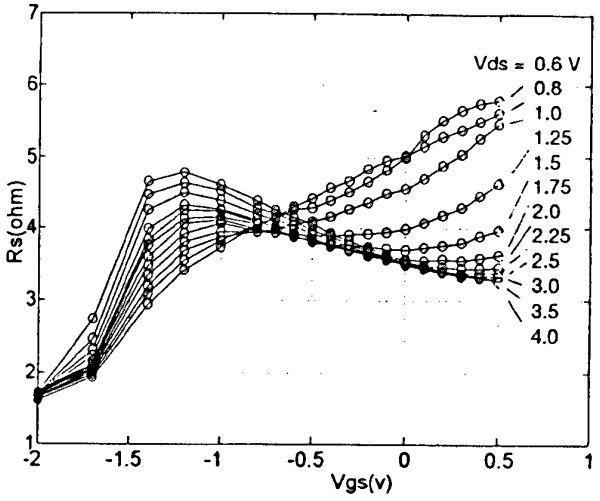

Figure 8: Extracted source resistance of a 0.5 µm (100x2) GaAs MESFET as function of bias conditions

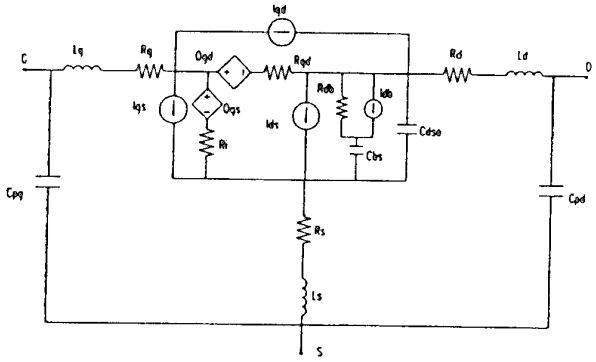

Figure 9: Our new empirical model uses the same equivalent circuit as that of EEFET3

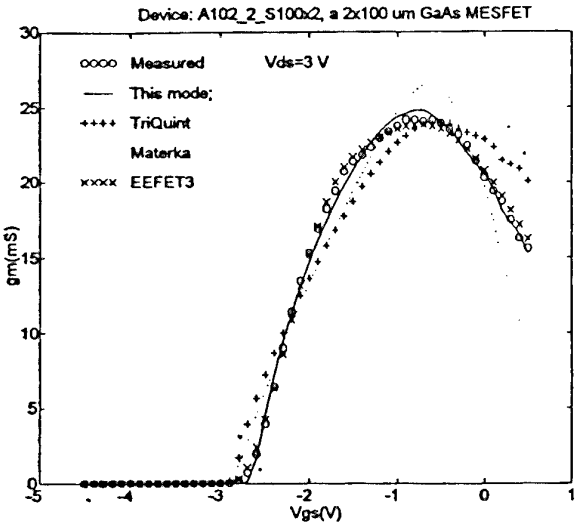

Figure 10: Measured and simulated transconductance gm using ours, Materka, TriQuint and EEFET3 models for a 0.5 µm (100x2) GaAs MESFET.

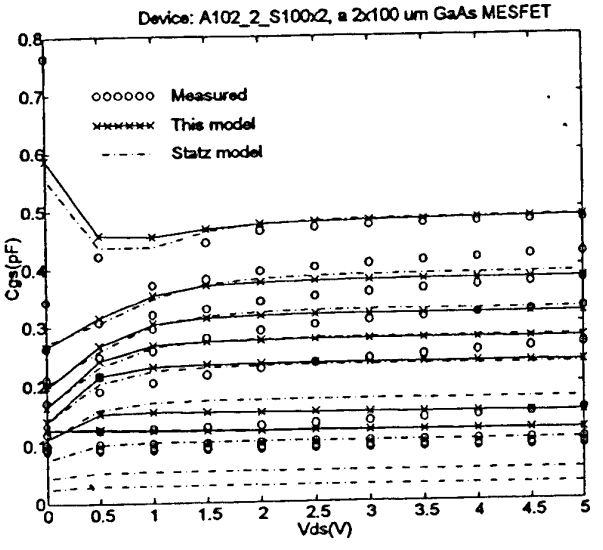

Figure 11: Measured and simulated transconductance Cgs compared with Statz model for a 0.5 µm (100x2) GaAs MESFET (Z=0.53).

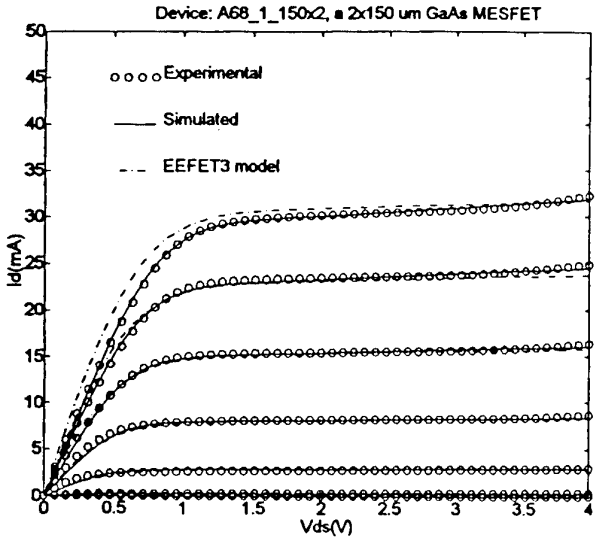

Figure 12: Experimental and Simulated I/V curves for a 0.5 µm (75x2) GaAs MESFET. Vgs = -1.0 to 0.5 V (0.25 V intervals).

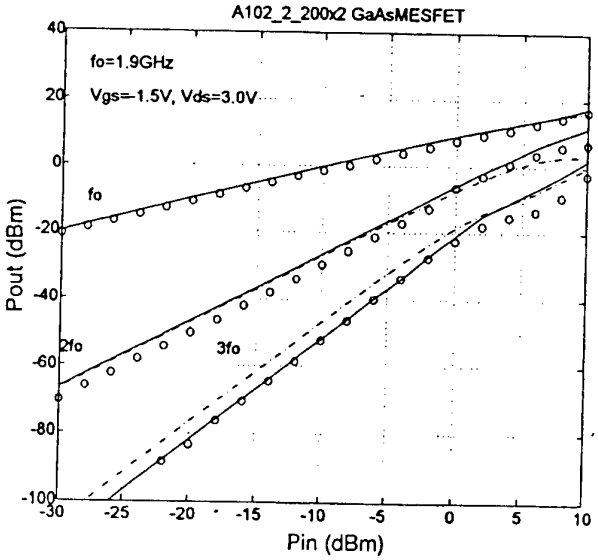

Figure 13: Experimental and simulated P_{in}/P_{out} behavior for the first three harmonics using our model and EEFET3 for a 0.5 µm (200x2) GaAs MESFET device.

Extensions and model verification of the Chalmers Nonlinear HEMT and MESFET Model

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ABSTRACT

The ability to simulate temperature, dispersion and soft-breakdown effects was added to the Chalmers non-linear model for HEMTs and MESFETs. DC, pulsed DC, low frequency (10 Hz-10 MHz), RF and small signal S-parameter measurements (1-18 GHz) have been made on a large number of commercial HEMT and MESFET devices from different manufacturers in the temperature range 17-400K in order to evaluate the validity of the model extensions.

INTRODUCTION

It is well known that a large signal model extracted from experimental DC data does not fully describe the transistors' behaviour at RF. For example, there is a discrepancy between the DC and RF transconductance as well as output conductance due to temperature and dispersion effects. A common explanation is that traps and surface states in the semiconductor affect the performance of the device. These effects should be considered in the design of circuits like power amplifiers, cryogenic amplifiers, etc. Better large signal models can be extracted if the DC characteristics are measured by pulsed measurements. If the pulses are kept short the traps will not affect the device characteristics. The pulse period should be shorter than the mean life time of the traps. For cryogenic applications the DC characteristics have to be made at operating temperature to make the extraction of accurate models possible. Soft breakdown, a non destructive drain current breakdown for high drain voltages, can be observed for some HEMTs and MESFETs. Transistors operating in this region should be modelled in such a way as to take this into account.

THE MODEL

The equation for the drain-source current in the Chalmers model is [1]:

$$I_{ds} = I_{pk}(1+\tanh(\Psi))\tanh(\alpha V_{ds})(1+\lambda V_{ds}) \quad (1)$$

Ψ is in general a power series function centred at V_{pk} and with a variable V_{gs}, i.e.:

$$\psi = P_1(V_{gs}-V_{pk}) + P_2(V_{gs}-V_{pk})^2 + P_3(V_{gs}-V_{pk})^3 \ldots \quad (2)$$

where I_{pk} is the drain current and V_{pk} the gate voltage at which the maximum of the transconductance occurs, λ is the channel length modulation parameter and α is the saturation voltage parameter. As a first approach we choose P_1 as $P_{1s}=g_{ms}/I_{pks}$, where g_{ms} and I_{pks} are measured in the saturated current region. Since the limit of the function $1+\tanh(\Psi)$ is 2 then I_{pk} should be equal or larger than: $0.5I_{max}/(1+\lambda V_{ds})$

Actually the drain term $(1+\lambda V_{ds})$ is the first term of the power series of the exponential dependence of the drain current vs. drain voltage, which in our opinion better describe the behavior of the drain current:

$$I_{ds} = I_{pk}(1+\tanh(\Psi))\tanh(\alpha V_{ds})e^{\lambda V_{ds}} \quad (1b)$$

We found that the model worked well using the first term of the function Ψ because P_1 is the only coefficient defining the transconductance value at V_{pk}. If the derivative of the drain current, g_m, is asymmetrical, then 2-3 terms can be added in Ψ. Note that neither P_2 nor P_3 affects the transconductance at V_{pk}. P_2 makes the derivative of the drain current asymmetrical and P_3 changes the drain current values at voltages V_{gs} close to pinch off.

In the case of large gate and drain voltage swing the coefficient α can not be assumed constant. For MESFETs this dependence is not so strong, but for HEMTs α changes rapidly with the gate voltage. Good correspondence between model and measured results at drain voltages below 1.5V and at small drain currents I_{ds} can be reached by using the following expression for α:

$$\alpha = \alpha_r + \alpha_1[1+\tanh(\psi)] \quad (3)$$

where α_1 is constant and α_r is the residual value of α at pinch off. For HEMTs, α_r is usually very small(0.05- 0.2) A good starting point in the extraction process for α_s and λ is to use the values obtained from the $I_{ds}(V_{ds})$ characteristics at positive gate voltages V_{gs}=0.2-0.4 V

When the device operates in the saturated region, P_1 and V_{pk} can be considered constant too. The global behaviour of the transistor can be described by the following expressions for V_{pk} and P_1 :

$$V_{pk}(V_{ds}) = V_{pk0} + (V_{pks}-V_{pk0})\tanh(\alpha V_{ds}) \quad (4)$$

$$P_1(V_{ds}) = P_{1s}\left[1+(\frac{P_{10}}{P_{1s}}-1)\frac{1}{\cosh^2(BV_{ds})}\right] \quad (5)$$

where V_{pk0} and V_{pks} are V_{pk} measured at V_{ds} close to zero and in the saturated region, respectively, $P_{10}=g_{mo}/I_{pk0}$ at V_{ds} close to zero and B is a fitting parameter ($B\approx 1.5\alpha$).

If necessary the model can be made symmetric, i.e. it will be possible to interchange the V_{gs} and V_{gd}. Then the total current is composed from two currents- one modeling the drain current at positive drain voltages and the other at negative. The functions ψ should be changed also:

$$I_{dsp} = 0.5I_{pk}(1+\tanh(\Psi_p))(1+\tanh(\alpha V_{ds}))(1+\lambda V_{dg}) \quad (1c)$$
$$I_{dsp} = 0.5I_{pk}(1+\tanh(\Psi_n))(1-\tanh(\alpha V_{ds}))(1-\lambda V_{gs})$$
$$I_{ds} = I_{dsp} - I_{dsn}$$
$$\psi_p = P_1\left(V_{gs}-V_{pks}\right)+P_2\left(V_{gs}-V_{pks}\right)^2+P_3\left(V_{gs}-V_{pks}\right)^3\ldots \quad (2b)$$
$$\psi_n = P_1\left(V_{gd}-V_{pks}\right)+P_2\left(V_{gd}-V_{pks}\right)^2+P_3\left(V_{gd}-V_{pks}\right)^3\ldots$$

The symmetric model is quite accurate but the execution time is nearly twice longer.

MEASUREMENTS AND MEASUREMENT SET-UP

We made measurements on a number of samples from different commercial MESFET and HEMT device manufacturers[1] in order to investigate how temperature and dispersion effects influence the devices' performance. DC- and S-parameters of the packaged devices were measured in a Maury MT-950 transistor fixture and in a specially developed microstrip fixture for the temperature range 17-400 K. A Cryogenics Model 350 Refrigerator was used to cool down the transistors and a Lake Shore temperature controller for keeping the temperature stable. A HP4195A VNA was used for measuring low frequency S-parameters (10 Hz-500 MHz) of the transistors and a Wiltron 360B for the measurements in the frequency range 0.1-18 GHz. The equivalent circuit of the transistor shown in Fig. 1 was used to model the packaged transistors. The parasitic parameters L_g, L_d, L_s, C_p etc. were fixed at the values extracted from the S-parameter measurements at V_{ds}=0 V at room temperature. R_g, R_d, R_s were extracted from DC and cold FET S-parameter measurements as a function of the temperature [2]. The component values of the cold FET small signal equivalent circuit were extracted by using our own extraction program MILOU, but similar results were obtained with MDS (Hewlett-Packard), Scout and Microwave Harmonica (Compact Software). Pulsed DC, RF (10 Hz-10 MHz) and S-parameter measurements were performed to find the frequency dispersion of the transconductance and the output conductance of the device [3-7,10,13]. DC-parameters were measured by using a HP 4145B parameter analyzer. The devices are usually pulsed for a short period (1 ms) into the active region and are then held in the passive (cut-off) region for the rest of the period (typically 1 ms). In our DC measurement set up with HP4145B a 5 second pause was used between each measured trace in order to allow cooling of the device between the sweeps.

[1]NEC32684 (NEC), FHX15FA (Fujitsu), MGF4317D, MGF1404 and, MGF1303B (Mitsubishi) named NEC3, FHX15, MGF4, MGF14 and MGF3 respectively. The first three devices are HEMTs and the last two are MESFETs.

DISPERSION MODELLING

In Fig. 2, 3 measured frequency dependencies of I_{ds} and g_m extracted from DC, pulsed and RF measurements are presented. The measured difference between the DC transconductance and the transconductance values, extracted from pulsed DC, RF and S-parameters was small (about 5-10%) for most of the new HEMT devices. We noticed a small increase of the transconductance (2-4%) at high frequencies in some devices compared with the DC value (FHX15, MGF4317D). For the MESFET devices we measured we found that the RF value was always lower than the DC value and that there were some devices for which the dispersion effects were quite substantial, i.e. MGF1404 (a decrease of nearly 25%), Fig 3.

Two approaches were used in modelling the device dispersion: analytical , in which the dispersion phenomenon is incorporated into the equation for the drain current in the large signal model and an approach, where the equivalent circuit is extended with components that model the dispersion effect. The two approaches have both advantages and disadvantages. The equivalent circuit approach is simpler, since it is easy to incorporate it into HB simulators, but not so accurate as the analytical approach.

At operating frequency much lower than one divided by the trapping time constant (typically in the millisecond range), the transconductance, $g_m(w)$, and the channel conductance, $G_{ds}(w)$, equal the DC value. At high frequencies, when the traps are frozen, the transconductance and the channel conductance reach their RF values. Using the formulation in [9,10] the drain current consists of three parts:

$$I_{ds,RF}[V_{gs}(t),V_{ds}(t)] = I_{ds,DC}[V_{gs}(t),V_{ds}(t)] + \\ +\Delta I_{ds}[V_{gs}(t),V_{ds}(t)]+\Delta\bar{I}_{ds}[V_{gs}(t),V_{ds}(t)] \quad (6)$$

The first term is the quasi- static I-V characteristics of an ideal dispersionless device. The extra terms are the contributions from the instantaneous transconductance and channel conductance dispersion. This type of I_{ds},RF dependence can be modelled with a frequency dependent factor, P_{1d}:

$$P_1 = P_{1d}P_{1s}[1+(\frac{P_{10}}{P_{1s}}-1)\frac{1}{\cosh^2(BV_{ds})}] \quad (7)$$

The dispersion effects of the g_m can be taken into account by using the frequency dependence proposed in [3] and this can be incorporated in the model as:

$$P_{1d} = \frac{P_{1srf}}{P_{1sdc}}+\frac{P_{1sdc}-P_{1srf}}{P_{1sdc}}\frac{1}{1+\left(f/f_{tr}\right)^2} \quad (8)$$

or

$$P_{1d} = \frac{P_{1srf}}{P_{1sdc}} + \frac{P_{1sdc} - P_{1srf}}{P_{1sdc}} \sum_{n=1}^{N} \frac{K_n}{\cosh\left(f/f_{tr,n}\right)^2} \qquad (9)$$

P_{1sdc} is the P_{1s} measured at DC for saturation drain voltages, P_{1srf} is extracted from the RF measurements and $f_{tr,1},...f_{tr,n}$ are the corner frequencies for the dispersion effects. This approach works well in the frequency domain. One way to incorporate this dependence directly into a HB simulator is to treat the dispersion part, P_{1d} , as a constant. Then it is possible to obtain good results in simulating DC and S-parameters. Another way is to use a time domain operator, *d/dt* , in P_{1d} similar to the approach used in [9].

The values of the output resistances $R_{dst} = r_{ch} + R_d + R_s$ were extracted directly from RF data by using an HP 4195A VNA at 100 MHz and an HP 4145B Parameter Analyzer at DC respectively. In Fig. 4 measured DC data and RF data for two HEMTs - MGF4317D and NEC32684 -are shown. The RF values of the output resistance R_{dst} are much lower than the DC values for NEC32684. For other HEMTs, i.e. MGF4317D, the difference between the RF and DC values is much smaller. Explanations for this behaviour are given in [3,6,7,10]. It is interesting to see that at high positive gate voltages, when the current is large, the DC values of R_{dst} can reach negative values. The reason for this is self heating. The RF output resistance, R_{dst}, decreases monotonically with the increase of the gate voltage, as described by the model. Negative R_{dst} is not observed at RF, since in small signal S-parameter measurements the transistor operates under isothermal conditions. Above the gate voltage, at which the DC values of R_{dst} start to increase, pulsed DC measurements should be made because the self heating effects can not be neglected. In Fig. 4 the frequency dependence of the output drain to source resistance R_{dst} is shown. For some transistors, i.e. MGF1303B, there are probably two different trapping processes with different corner frequencies. An RC-series circuit (R_c,C_{rf}) was used to model the low frequency dispersion of the output conductance. By adjusting the λ values extracted from the DC measurements and the values of the RC-circuit it was possible to fit simulated to experimental data for both DC characteristics and S-parameters. If the frequency dependence of the output conductance is more complicated and it is important to model this behaviour, this can be done by adding an additional RC circuit in parallel with another time constant. A problem arising in using this approach is caused by the fact that in reality R_c is bias dependent, Fig. 5-7. At V_{gs} voltages close to the pinch off, the value of R_c is much higher then the value of R_c under active working conditions. Good correspondence between modelled and measured S-parameters can be reached by using the following expression for gate bias dependence of R_c:-> $R_c = R_{c0} + \frac{R_{cpof}}{1+\tanh(\psi)}$ where R_{c0} is the minimum value of R_c and R_{cpof} determines the value of R_c at the pinchoff.

A similar approach can be used to model the dispersion of the transconductance. The charging resistance R_i and source parasitic resistance R_s, which in reality are distributed, decrease the value of extrinsic transconductance. This can be modelled by using a DC and an RF part. For HEMTs a noticeable decrease of R_s was reported in the frequency range 1-30 GHz , that would lead to an increase of the RF transconductance. We obtained similar results for MGF4317D, FHX15 and other HEMTs. This can be modelled by adding a parallel branch to R_s, R_{srf} and C_{srf}. The time constant of this network should correspond to the dispersion constant of g_m. As R_{sf} is in parallel with R_s, an increase in the transconductance will be obtained at RF. The value of C_{srf} determines the time constant of the process.

The decrease of the transconductance for MESFETs can be described by adding a parallel branch, R_{irf} and C_{gsrf} in series, between the internal gate and source terminals. At frequencies higher than the corner frequencies for the dispersion effects the resistor R_{irf} shunts the input and effectively decreases the transconductance.The most important and critical moment in the parameter extraction is the determination of two main models parameters - I_{pk} and V_{pk}. The most common error in the extraction procedure is to perform the measurements with gate voltages not high enough to provide information about the maximum current I_{max}. We have found that if the measurements are performed at gate voltages high enough to give information about the maximum I_{ds} current, standard fitting programs like Scout and Kaleidagraph work well. Other problems are caused by instabilities in the transistor, dispersion and thermal heating. We have found it useful [11] to make Power Spectrum Measurements(PSM). Usually the first two harmonics give the necessary information about V_{pk} and I_{pk} - at V_{pk} the second harmonic is at its minimum and the first at its maximum (or close to it).

MTA analyzer is a very powerful tool which can be used to provide information about transistor behavior in a DC, S, and large signal modes of operation. The block diagram of the MTA system which is especially designed for large-signal waveform measurements is shown in fig.... This system yields the harmonic magnitude and phase spectra of the incident and reflected waves at both ports of the nonlinear DUT with respect to its planar reference planes. From the wave quantities, the voltage and current waveforms at the gate and the drain of the FET are calculated. More detailed information regarding this measurement system can be found in [14,15].

In fig. 10 and 11 the gate and drain voltage and current waveforms as measured with the MTA system are shown(points) .The modeled parameters are shown with the solid lines. In the fig. 10,12 the simulation is made with Rc =250 ohm which is typical for active bias conditions. The gate and drain voltages are reproduced quite well but in the drain current there is a flat part which can be explained with the AC current flowing through the Rc. This means that in the DC and S-parameter simulations we will have a good correspondence, but the large signal simulations i.e. saturated power, DC current under large signal excitations and power added efficiency will be erroneous. In the next figure,Fig. 11, 13 are shown the same bias conditions but in the simulations Rc is considered bias dependent. The correspondence is much better.

MODELING OF THE TEMPERATURE DEPENDENCE

The main parameters of the model - V_{pk0}, V_{pks}, I_{pk}, P_{1s}, P_{10}, l, V_{gs}, R_s, R_d, C_{gd}, C_{gs} - are also temperature dependent. To evaluate this temperature dependence several transistors from each of the types listed above were measured in the 17-400K temperature range. Temperature changes in model parameters for different HEMT and MESFET devices in the temperature range 17-400K are presented in Figs. 14-19. The voltages at which we have maximum transconductance, V_{pk0} and V_{pks}, increase linearly at low temperatures, Fig. 14. P_{1s} is almost independent of temperature, Fig. 17a, because of the nearly monotonous increase of both g_m and I_{pk}, Fig. 15, 16 at low temperatures. The changes of the transconductance are mainly due to I_{pks} increase at cryogenic temperatures. The largest change we monitored was the increase of the coefficient P_{10} at cryogenic temperatures, Fig. 17b. This observation is very important for circuits operating at low drain voltages, such as modulators, resistive mixers, etc. It means that it will be possible to reduce the power that the local oscillator must provide for the full drive of a resistive mixer at cryogenic temperatures. Slight increases of λ and α (Fig. 18a-b) for all transistors are observed at low temperatures.

The source parasitic resistance R_s decreases monotonically at low temperatures, Fig. 19. The changes of the capacitance C_{gs} and C_{gd} with temperature are very small, approximately 10÷20 % in the whole temperature interval 17K- 300K and can be modelled quite accurately with linear functions. Generally in the temperature range 150-400K the changes of the model parameters with temperature are usually smooth. These temperature changes variations can be modelled with good accuracy by using linear functions. Nearly all measured devices showed some unexpected behaviour in the temperature range 50-150K, i.e. a collapse of the I-V characteristics, significant kink effects, strange shapes of the transconductance curves, strange shape of I_{ds} vs V_{ds} dependencies at positive gate voltages, etc. At lower temperatures (17-50K) the transistor characteristics are smoother and more predictable performance has been monitored.

For small signal applications the drain current reduction caused by thermal heating effects can be neglected in most cases, but for medium and high power applications the dissipated power P_d is large enough to heat the transistor to temperature T and thus significantly change the model parameters [2]. At small power dissipation and constant temperature distribution in the channel the temperature rise $\Delta T=q(T_0)P_d$ can be considered linear, where $q(T_0)$ is the thermal impedance at ambient temperature T_0. The influence of self heating can be found by interactively solving nonlinear temperature equations at two temperatures, when thermal impedance $q(T_0)$, temperature change $\Delta T=T_2-T_1$ and P_d are given. This process is not straightforward, since the interdependence of the self heating processes and the trap occupancy problem cannot be independently controlled in a simple way. When an approximate linear solution is possible and trapping processes are not influenced by the temperature rise, the change of I_{ds} at DC can be modelled in these programs through different model parameter temperature dependencies and in a simpler form this can be expressed as [9]:

$$I_{dstem} = \frac{I_{ds}}{1 + K_t P_d} \tag{10}$$

where K_t is the thermal constant for the transistor that summarises the temperature changes of the different large signal model parameters influenced by the temperature rise under the total dissipated power $P_d \approx I_{ds}(t) \cdot V_{ds}(t)$. Since the temperature coefficients of the model different parameters are very small (in the order of 10^{-3}), this approximation usually works satisfactorily and can be easily incorporated in a harmonic balance simulator. Using such an approach it is possible to obtain information about the transistor temperature changes due to self heating. A better way to handle this problem is to define a thermal port where the device temperature is the analogous voltage across the thermal port and the dissipated power is the analogous port current. Then an arbitrary thermal circuit can be constructed externally to the device model [12].

SOFT BREAKDOWN MODELLING

For many HEMT devices it is possible to monitor an abrupt increase of the drain current well below the breakdown by increasing the drain voltage above some specific threshold V_{tr}. This is especially noticeable at gate voltages close to pinch off. Since the gate current I_{gs} is much lower than the drain current I_{ds}, the increase is not due to gate breakdown. It can be attributed to the increase of the positive hole charges in the substrate, which widens the channel thickness and leads to an abrupt increase of the drain current. The cause for this effect is not entirely clear but it can be partly explained with the trapping effects phenomena. The breakdown phenomenon is different at DC and RF. The occurrence of RF breakdown is more usual at higher drain voltages than at DC. Soft breakdown strongly influences the DC characteristics and output power of the device, therefore the operating point should be carefully selected. Due to the soft breakdown in some devices the increase of the drain voltage leads to the decrease of the output power . Two approaches for modelling these effects can be found in [9, 13]. For soft breakdown modelling we consider it preferable to use the exponential approach with some modifications. In our model the drain current equation is extended with a new term L_{sb}:

$$I_{ds} = I_{pk}(1 + \tanh(\Psi))\tanh(\alpha V_{ds})(1 + \lambda V_{ds} + L_{sb}) \tag{11}$$

$$L_{sb} = L_{sb0}[\exp(L_{sd1} V_{dgt} + \ldots) - 1] \tag{12}$$

$$V_{dgt} = \frac{V_{ds} - K_{trg} V_{gs} + V_{tr}}{V_{tr}} - 1 \tag{13}$$

$$L_{sd1} = L_{d1}(1 - L_{g1} V_{gs}) \tag{14}$$

where L_{sb0} and L_{sd1}, are the coefficients matching the drain current dependencies and V_{dgt} is a normalised coefficient that combines the gate and drain voltages. If equation 1.a is used to model the drain current then the sofbreacdowm model can be implemented in a easier way:

$$I_{ds} = I_{pk}(1+\tanh(\Psi))\tanh(\alpha V_{ds})e^{\lambda V_{ds} + L_{sd1}V_{dgt} + \ldots} \quad \text{(11a)}$$

If higher accuracy is needed more terms can be added to Eq. 11.

In Fig. 20 modelled and measured results for I_{ds} versus V_{ds} for MGF4317D are shown. Soft breakdown and self heating are included in the model (Eq. 11-14). Device parameters are listed in Table 1. Measured and modelled PSM for this device are shown in Fig. 21 and 22 respectively. The maximum output power is 18 dBm and the difference between measured and simulated first harmonic is less than 0.4 dB. The global mean error for the higher harmonics is less than 3 dB, Fig. 23. Figures 24 which show cross sections of the global PSM spectrum, visualise this in details. The difference between the simulated and experimental data for the higher harmonics at high drain voltages can be partially explained by the existence of a"kink" effect in the transistor. Another reason for the difference is that for simplicity we used only one term (L_{d1}) in the soft breakdown model.

CONCLUSIONS

Temperature, dispersion and soft breakdown effects found in HEMTs and MESFETs were investigated in the temperature range 17-400 K. We have shown that it is possible to extend the Chalmers nonlinear model with the ability to model these effects. The model extensions give a good correspondence between measurements and simulations.

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Table 1. MGF4317D: V_{ds}=4V, 300K, Device No. 2.

I_{pks} mA	V_{pks} V	V_{pk0} V	P_{1s} 1/v	P_{10} 1/v	B 1/v	P_2 $1/V^2$	P_3 $1/V^3$	l 1/v
46	0.03	-0.3	2.1	3.0	4	-1.0	1.0	0.15
a_1 1/v	a_r 1/v	L_{b0}	L_{d1} 1/v	L_{g1} 1/v	V_{tr} V	K_{trg} V	K_t 1/W	
2.1	0.05	0.016	1.6	0.7	1.9	1	0.25	

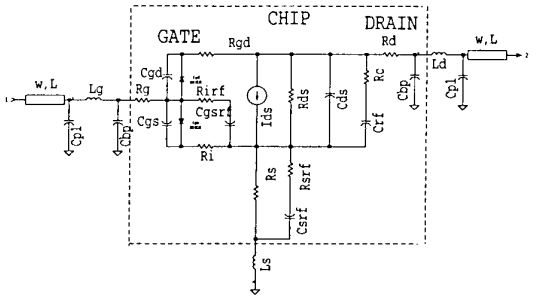

Fig. 1. Equivalent circuit of the HEMT.

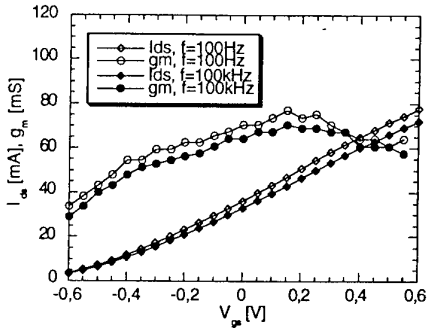

Fig. 2.Dispersion for MGF1404 from pulsed measurements

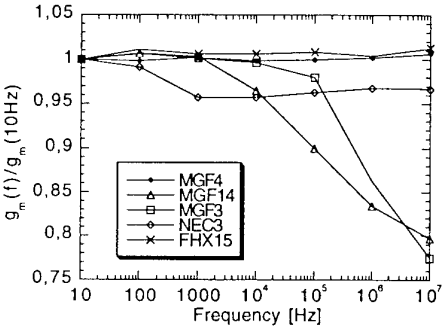

Fig. 3.Dispersion in the peak value of g_m

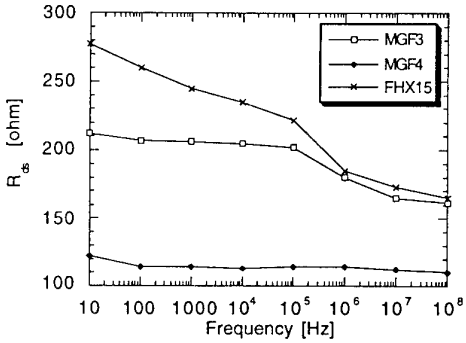

Fig. 4. R_{ds} as function of frequency, V_{ds}=2.0 V, V_{gs}=0.0 V.

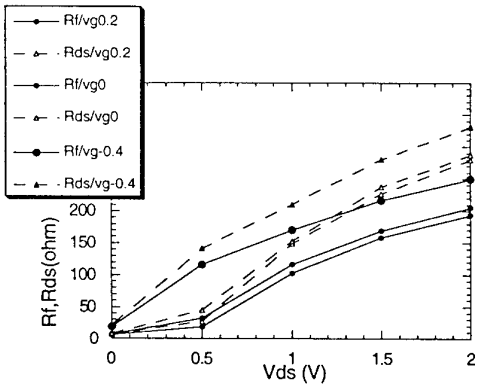

Fig. 5 R_{ds} and R_f vs. drain voltage

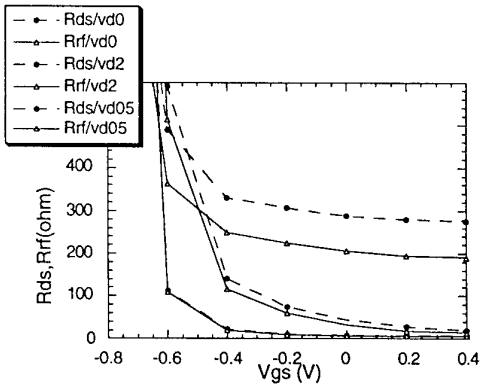

Fig. 6 R_{ds} and R_{rf} vs. gate voltage

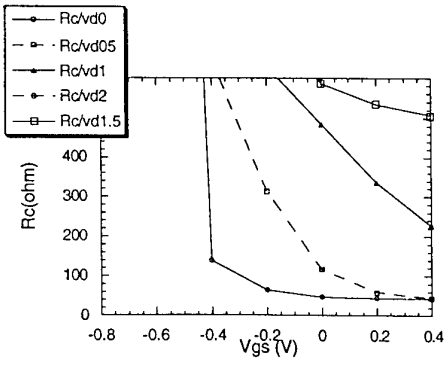

Fig. 7. R_c as function of V_{gs}

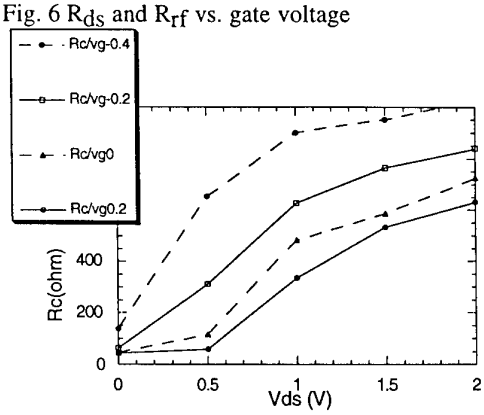

Fig. 8. R_c as function of V_{ds} .

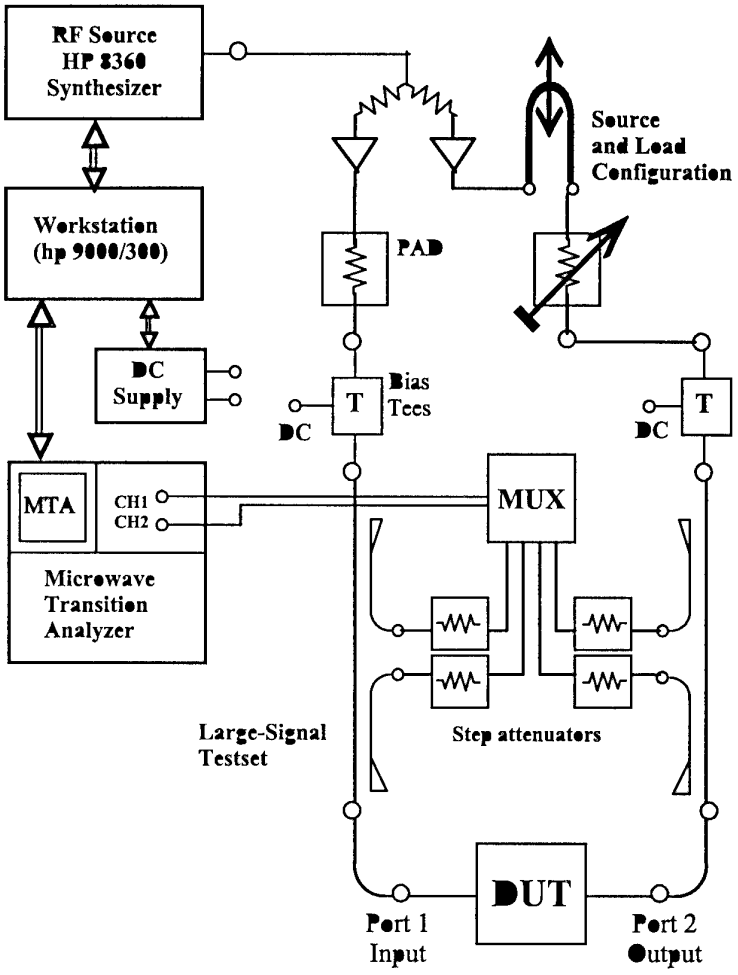
RF Source
HP 8360
Synthesizer
Workstation
(hp 9000/300)
DC
Supply
MTA
CH1
CH2
Microwave
Transition
Analyzer
Source
and Load
Configuration
PAD
T
Bias
Tees
DC
T
DC
MUX
Large-Signal
Testset
Step attenuators
DUT
Port 1
Input
Port 2
Output

Fig. 9a

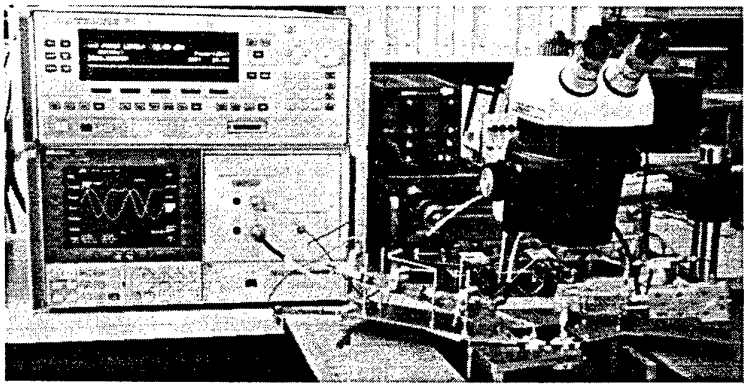

Fig. 9b

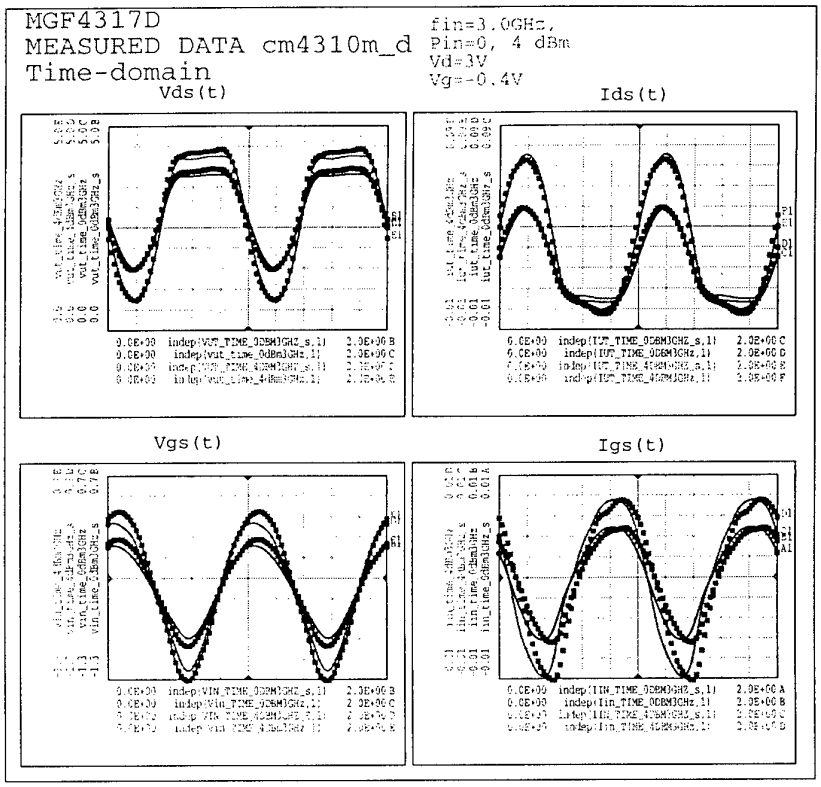

Fig. 10. Measured and simulated voltage and current waveforms. Rc =250 ohm

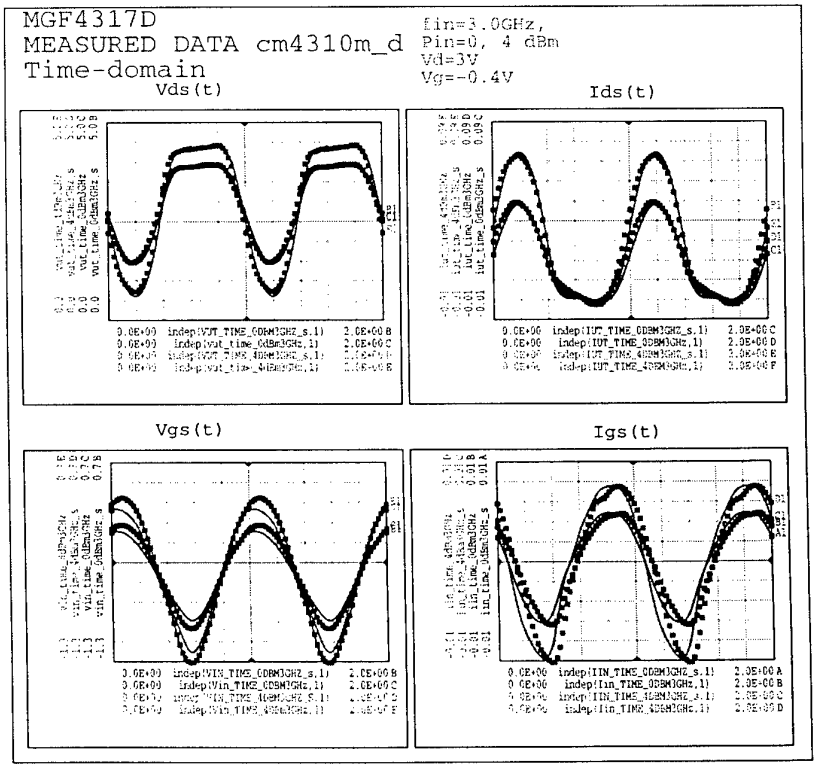

Fig. 11. Measured and simulated voltage and current waveforms. Rc=bias dependent

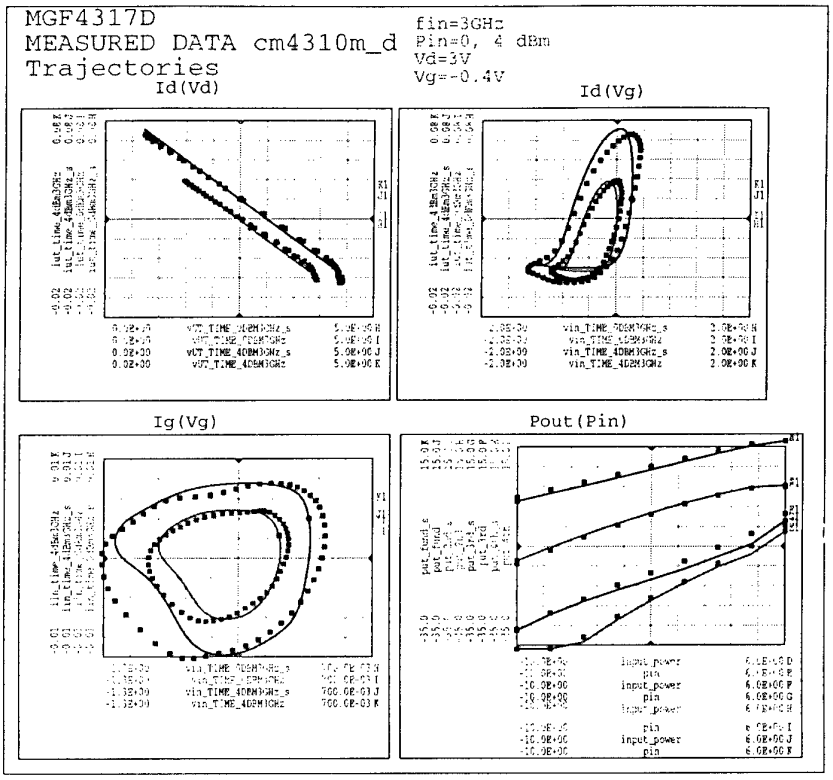

Fig. 12. Measured and simulated trajectories and harmonics. Rc =250 ohm

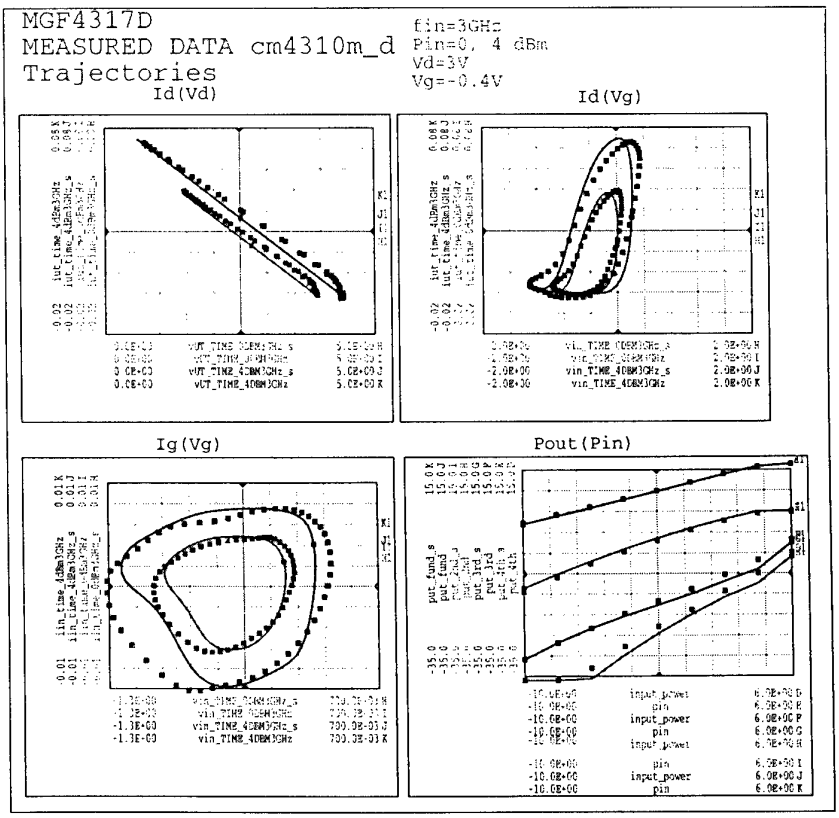

Fig. 13. Measured and simulated trajectories and harmonics. Rc =bias dependent

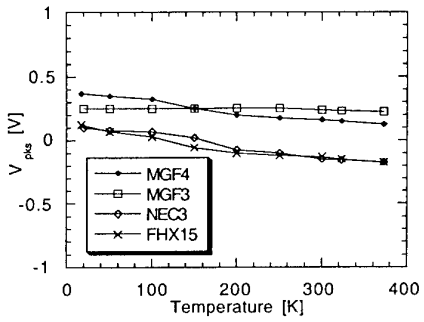

Fig. 14a. V_{pks} as function of temperature.

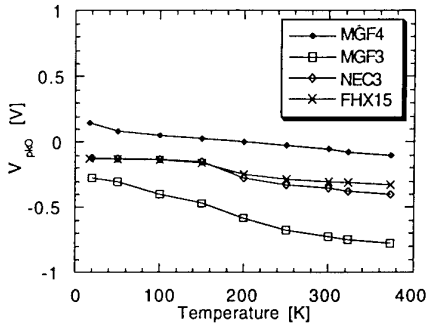

Fig. 14b. V_{pk0} as function of temperature.

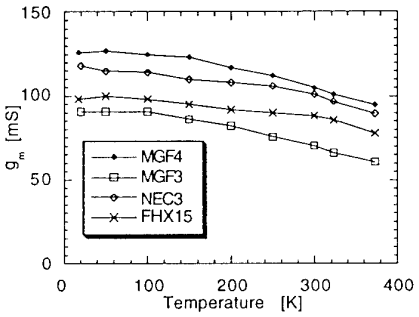

Fig. 15. The peak value of g_m as function of temperature.

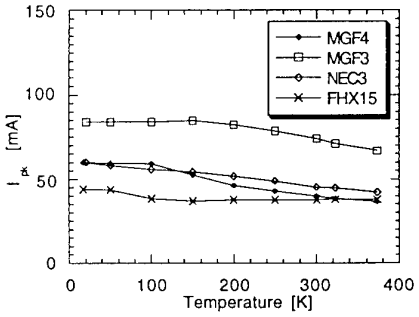

Fig. 16. I_{pk} as function of temperature.

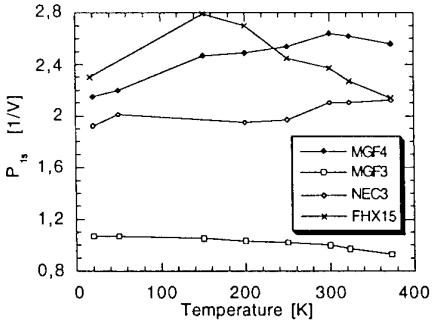

Fig. 17a. P_{1s} as function of temperature.

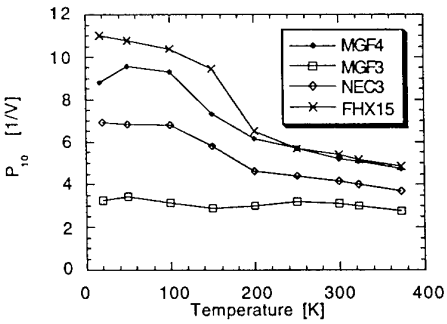

Fig. 17b. P_{10} as function of temperature.

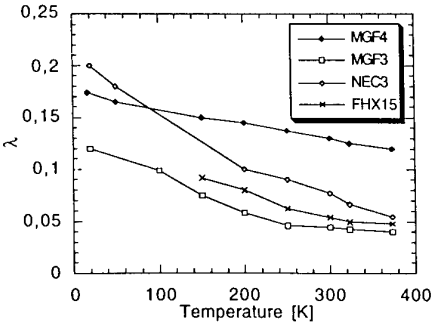

Fig. 18a. λ as function of temperature.

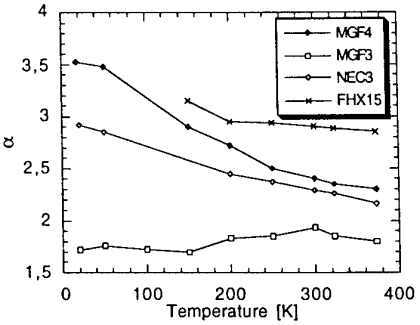

Fig. 18b. α as function of temperature.

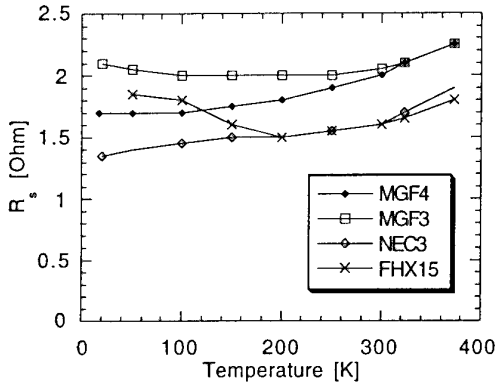

Fig. 19. R_S as function of temperature.

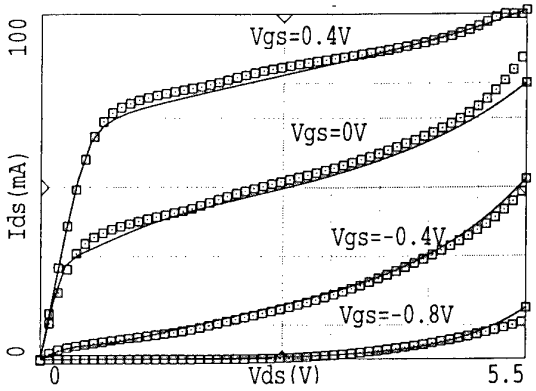

Fig. 20. Drain current I_{ds} as a function of drain V_{ds} for MGF4317D at 300K. V_{gs}=-0.8, -0.4, 0.0, 0.4V.

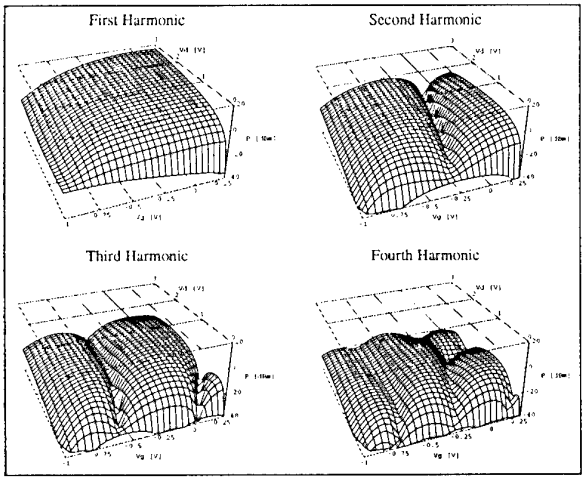

Fig. 21. Measured Power spectrumfor MGF4317

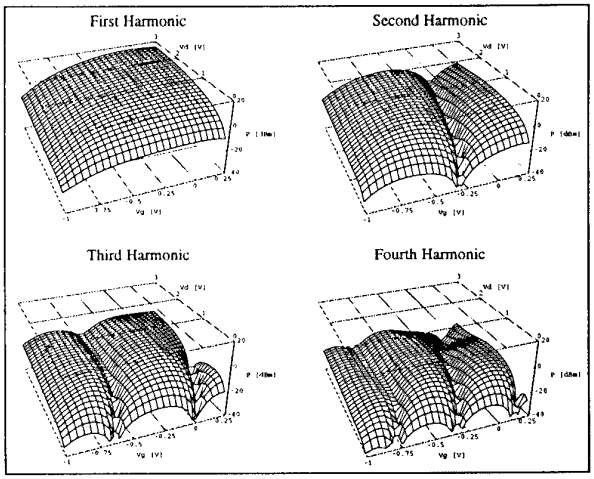

Fig. 22. Simulated Power spectrum for MGF4317

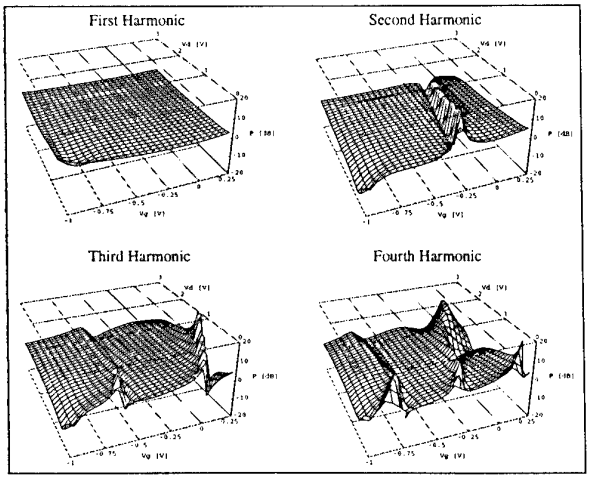

Fig. 23.The Chalmers model, error in the simulations.

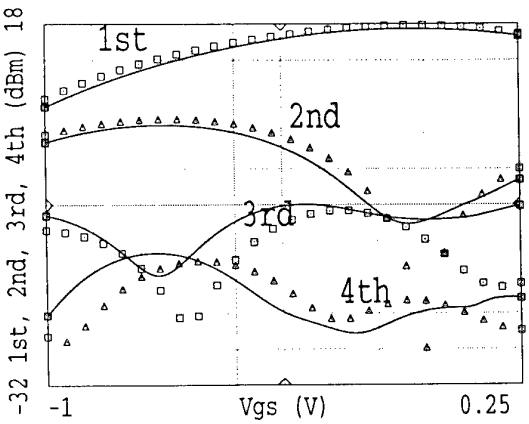

Fig. 24. Power spectrum as function of V_{gs},Vds=4 V

Quasi-Static Modeling of Microwave Field-Effect Transistors for Use in Nonlinear Circuit Design

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Abstract – Efforts to optimize the performance of microwave field-effect transistors have depended heavily on device models for guidance. Models have also been important in the design of transistor circuits, both for linear and nonlinear applications. The overview being presented reflects on the evolution of microwave field-effect transistor modeling, with focus on equivalent-circuit-based methods for use in large-signal circuit designs. A critical issue is finding a proper balance between accuracy of prediction and procedural efficiency in the face of complicating circumstances. These may arise from simple changes in temperature and optical illumination, or from more complex carrier trapping and impact ionization phenomena. Still, large-signal circuit designs can very often be carried out successfully by relying solely on techniques formulated in the frequency domain.

Introduction

Advances in the design and fabrication of semiconductor devices and circuits, over the years, have led to system components of smaller and smaller size performing functions of ever increasing complexity. This feat has been accompanied by steady improvements in performance and reliability, and significant reductions in cost. Progress, to a large extent, is attributable to broad-based efforts to refine semiconductor materials and processing techniques. Computer-aided simulation tools have also contributed substantially by offering ways to reliably interpret and predict semiconductor device characteristics, and have thereby provided guidance in devising improved device configurations and in streamlining procedures for the design of practical circuit realizations. A prerequisite for the use of these tools has been the availability of good semiconductor device models.

Supported by high-volume demand and decades of prominence, silicon-based homojunction bipolar transistor technology has remained the option of choice for low-frequency analog applications, offering attractive performance, cost effectiveness, and dependability. When appropriately designed, silicon homojunction transistors can operate up to frequencies in the lower microwave bands. With the help of GaAs- and InP-based heterojunction technologies, the frequency limits of bipolar transistors can be further extended through the mid-to-upper microwave frequency bands into the millimeterwave regime.

The field-effect transistor (FET) remains the backbone of the industry, however, with MESFET and HEMT variants among the most popular device configurations. Their reliance on majority carrier transport should, in principle, make them relatively easy to model. Aside from expected influences of parasitics, signal level, temperature, impact ionization, and optical illumination on device response characteristics, matters are often complicated by the additional presence of device parameter time-dependencies. The latter are most commonly observed in devices that are in early stages of development. Examples include FETs built from wide-bandgap materials, such as SiC and GaN, to withstand high power levels and high temperatures, and transistors made with channels of narrow-bandgap materials, such as InAs, to provide low-voltage, low-noise operation at room temperature. In these instances, models can fulfill an important role in helping to sort out observed anomalies and derive ways to reduce or eliminate their influence.

In the case of conventional GaAs- and InP-based devices, employed as workhorses in present-day applications, the role of device models is not so much to serve investigative purposes, as it is to provide accurate predictions of device performance in practical circuit applications. The ability to predict accurately is facilitated by the fact that, in devices of mature status, proper precautions have often been taken to subdue anomalous behavior. This reduces model complexity to a minimum, with remaining emphasis centered on correct representation of temperature dependencies and device

nonlinear effects. To deal with the latter, simulations are normally performed in the time domain. Although available computer-based tools make this task less frustrating than it used to be, the optimization of circuit performance in the nonlinear regime can still be a rather tedious task, even with the assistance of efficient harmonic-balance techniques that confine time-domain formulations to nonlinear equivalent circuit elements. In situations, however, where only fundamental-frequency behavior is of interest, nonlinear circuit design problems can often be solved by relying entirely on frequency-domain-based linearization methods, allowing conventional microwave circuit analysis and synthesis techniques to be put to effective use.

The Quasi-Static Model

The first FETs to emerge onto the microwave scene were GaAs MESFETs for broadband, low-noise applications. Early modeling efforts remained subsequently focused on linear equivalent device representations. The models became widely employed both in the evaluation of device performance characteristics and in the derivation of new design procedures for small-signal amplifiers. Prompted by the need to address intermodulation concerns in such amplifiers, models were then generalized to also include nonlinear effects. As technological capabilities expanded, MESFETs found increased use in large-signal applications as well. Nonlinear models played, thereby, important roles in helping to understand device-circuit interactions and in optimizing the large-signal circuit responses of power amplifiers, oscillators, and frequency multipliers, without the cumbersome reliance on experiment-based procedures.

The most common approach to modeling FET nonlinear behavior is to replace designated linear model elements in a small-signal equivalent circuit, as depicted in Fig. 1, with voltage-dependent ones. The dominant nonlinear elements, aside from the two diodes D_{gs} and D_{gd}, are the transconductance G_m, the output conductance G_{ds}, the capacitors C_{gs} and C_{gd}, and the input resistor R_{gs}. In this configuration, the circuit element types define the model's frequency response, while parameterized element values allow for the inclusion of signal-amplitude dependencies. The list of equivalent circuit elements and variables can be expanded to also include temperature and optical effects, as well as impact ionization and carrier trapping phenomena.

A common assumption made with regard to model element dependencies on signal levels and bias voltages is for designated element values to be time-invariant functions of a limited number of controlling voltages. In the model of Fig. 1, those voltages are the ones appearing across the gate-source input capacitor and the device-intrinsic drain-source port, respectively. Pertinent element values still remain implicit functions of time through functional relationships to controlling voltages, but time is not permitted as an independent variable. This is referred to as the quasi-static assumption, a postulate central to many semiconductor modeling approaches. The principal benefit derived from this assumption is the ability to define functional relationships under low-frequency operating conditions, instead of having to rely on large-signal device characterization methods at microwave frequencies, which are more time-consuming.

Among the first approaches to be applied to the large-signal equivalent-circuit-based modeling of microwave FETs was a scheme to derive nonlinear model element descriptions from device small-signal scattering parameters measured as functions of both frequency and bias voltages [1]. The procedure involves fitting a linear equivalent circuit to the scattering parameters for each discrete bias voltage combination, establishing sets of voltage-dependent small-signal element values, with frequency dependencies of device properties accounted for through the selection of an appropriate equivalent-circuit topology and associated model element types. Based on the quasi-static assumption, relationships between small-signal element values and static bias voltages remain valid as high-frequency instantaneous voltages are substituted for static voltages. This permits the large-signal current-voltage relationships of nonlinear model elements to be defined through simple differential equations that relate the voltage-dependent small-signal element values to corresponding large-signal instantaneous quantities.

The technique is straightforward to implement, in that it does not require special microwave instrumentation beyond the availability of a vector network analyzer. Once a device is characterized, analytical expressions can be employed to describe model-element current-voltage relationships for subsequent use in computer-aided circuit design procedures [2], [3]. The limitations of underlying assumptions must be duly recognized, however. Concerns relate to the manner in which bias-dependent device information is acquired. This pertains, in particular, to differences in thermal conditions between device operation in a practical circuit environment, where device-intrinsic temperatures are presumed to be invariant over a high-frequency cycle, and device operation during bias-dependent scattering parameter measurements, where temperatures may be allowed to stabilize with each new bias voltage setting. Measured static drain-source current-voltage characteristics for constant gate voltages thus often exhibit negative slopes against applied drain-source voltage, posturing as negative resistance effects that are seldom real. Current-voltage characteristics measured on a point-by-point basis must hence be corrected for thermal influences in order to accurately represent high-frequency dynamic conditions.

Similar concerns apply to optical illumination of an FET. Light incident on the device can generate carrier pairs within the device structure. The carrier pairs produce both photoconductive effects by increasing the number of carriers in the channel, and photovoltaic effects through modulation of the depletion region under the gate [4]. Such effects result in equivalent-circuit element values that change, to varying degrees, with incident light intensity. The most significant changes relate to drain-source current flow. They can be modeled, to a first-order approximation, by generalizing the standard equivalent-circuit current generator to include a light-intensity-proportional term. Due to different dynamics associated with holes and electrons, this term will exhibit a distinct frequency-based signature.

As demonstrated later, optical effects may be put to constructive use in the demodulation of optical-carrier-based microwave and millimeterwave signals. They may also be utilized in the diagnosis of anomalous device behavior related to carrier trapping. The dramatic influence light can have on static device current-voltage characteristics is illustrated in Fig. 2, where, in the case of an experimental wide-bandgap GaN microwave MESFET, trap-impaired operation of the transistor is restored to normal through illumination with low-intensity light [5].

Another relevant issue to consider is impact ionization. While gate forward conduction, as represented by the two diodes in Fig. 1, limits drain-source voltage swings at one extreme, impact ionization is responsible for containing voltage excursions at the other extreme and deserves proper respect at all stages of the modeling process. Related phenomena are normally not all that difficult to represent, although their effects can go well beyond simple clipping of voltage waveforms. To illustrate this, Fig. 3 shows the small-signal output reflection coefficient as a function of frequency and drain-source bias voltage of a HEMT with a channel made from narrow-bandgap InAs material [6]. Impact ionization associated with narrow-bandgap materials constitutes one of the disadvantages of using such materials to achieve low-voltage operation at room temperature. A noteworthy feature of the plotted response is its inductive behavior. To account for this, the equivalent circuit of Fig. 1 may be extended to include an inductor-resistor series combination at the intrinsic device output port.

The most serious challenge to the quasi-static assumption comes from transconductance and output conductance dispersion caused by carrier trapping centers located at the transistor semiconductor layer boundaries and in the layers themselves [7]. Provided in Figs. 4 and 5 are illustrations of such effects as they pertain to an experimental GaN transistor [8]. Trapping effects are typically confined to frequencies below 1 MHz, and hence do not tend to pose a serious problem to circuit operation at microwave frequencies. They also don't compromise the validity of the quasi-static model at microwave frequencies, provided the time-invariant model parameters are chosen to accurately reproduce high-frequency device behavior, and the existence of merely a fictitious low-frequency model response is acceptable.

In the common situation, where, for the sake of expediency, nonlinear current-voltage relationships are derived solely from static information, low-frequency dispersion effects, if present, can have a serious impact on a model's ability to accurately predict high-frequency device behavior. To circumvent the dilemma, pulsed device excitation signals can be employed in the determination of model-element current-voltage relationships, taking care to excite the device under test only at frequencies above the dispersion regime, while keeping thermal considerations in mind [9]. The occasional need for a model that can span the entire useful frequency range of a given device, including the dispersion regime, can be satisfied through extensions to the basic quasi-static approach [10], [11].

Increased model generality, to cope with effects ranging from simple temperature and light dependencies to more intricate impact ionization and trapping phenomena, is achieved at the expense of elevated model complexity and increased computational effort. In the end, it is actual circuit performance that counts, and care should be taken to assess model accuracy requirements against design uncertainties introduced by real-world conditions. When seen in context, some of the mentioned issues may represent merely second-order phenomena, especially in view of continuing advances in device materials and processing. Such advances include the uses of improved passivation and buffering schemes. They have resulted in considerable reductions in trapping effects which are the causes of transconductance and output conductance dispersion phenomena and are often responsible for excessive, time-dependent responsivity to light.

With appropriate awareness of inherent limitations, quasi-static models in their simplest forms still remain useful tools for projecting large-signal performance characteristics of microwave FETs in practical circuit environments. Among the most important conclusions drawn from early quasi-static modeling efforts [12] was the identification of transconductance and output conductance model elements as the ones predominantly associated with nonlinear device behavior. This led to simplified, systematic circuit design methodologies for optimizing large-signal circuit performance characteristics that focused solely on the two dominant device nonlinearities. The resistive nature of the nonlinearities allowed design procedures to be derived which could be conveniently based in the frequency domain, thereby making efficient use of established linear network analysis and synthesis techniques. Examples of such procedures

include methods that deal with the design of power amplifiers, single-frequency and varactor-tuned oscillators, and frequency multipliers. With models generalized to also include light-induced effects on the drain-source current flow, optical carrier demodulation may be added to the list of applications.

Circuit Applications

One of the first applications of quasi-static nonlinear FET models involved the design of broadband microwave power amplifiers for optimum large-signal gain performance. The objective was to provide a practicable alternative to inefficient experiment-based trial-and-error methods, and also circumvent the need to acquire and process load-pull information. A simple, yet effective design approach derives from the observation that voltage-dependent device transconductance and output conductance are mainly responsible for gain saturation and port impedance changes with signal drive level [13]. The aim is to achieve, under elevated signal level conditions, broadband fundamental-frequency conjugate impedance matching conditions at the transistor output port, while relying on suitable input matching circuitry to neutralize the intrinsic device gain roll-off with frequency. This choice rarely poses a real constraint, due to a natural tendency to avoid deliberate impedance mismatches at the device output port where most of the nonlinear device-circuit interactions occur. Conjugate output matching conditions imply a frequency-independent, resistive load line in the current-voltage plane of the intrinsic drain-source port. This, in turn, establishes a direct relationship between the fundamental-frequency components of the two controlling voltages indicated in the equivalent circuit of Fig. 1, permitting device nonlinearities to be conveniently expressed in terms of a single independent voltage variable.

With the fundamental-frequency component of the drain-source voltage selected as the independent variable, large-signal-equivalent element values, which are functions of this one variable, can be assigned to both transconductance and output conductance. The result is a linearized model with output-voltage-dependent element values. For a predetermined signal drive level, the linearization substitutes, locally, constant-gain-circles for non-circular load-pull contours, with the approximation maintaining usefulness over ranges of near-conjugate output matching conditions encountered in practical amplifiers. Element voltage dependencies can be easily derived through reoptimization of equivalent-circuit transconductance and output conductance values to conform, at each drive level, with measured large-signal available gain and affiliated reflection coefficient values. The crux is that large-signal measurements need only be performed at a single reference frequency, due to the frequency invariance of the element voltage relationships. The equivalent circuit model automatically provides pertinent frequency dependencies. Once a desired output voltage level, or corresponding output power level, has been chosen, the design of a large-signal amplifier is readily accomplished with the help of established frequency-domain synthesis techniques.

As an example, the equivalent large-signal values for the transconductance and the output conductance of a MESFET are plotted in Fig. 6 as functions of signal drive level expressed in terms of output power. With the equivalent element values derived at an arbitrarily chosen reference frequency of 8.5 GHz, Fig. 7 demonstrates how the linearized device model is able to accurately predict gain as a function of power level at 12 GHz. Experimental amplifier circuits, designed in accordance with the outlined method, showed equally good correlation between predicted and measured large-signal gain as a function of frequency.

Another area, where the quasi-static approach to FET modeling has led to streamlined circuit development procedures is in the design of fixed-frequency and voltage-tuned oscillators. As indicated in Fig. 8, the construction of an oscillator basically involves the design of a three-port coupling network, with ports connected to an external load and to the transistor gate-source and drain-source ports, respectively. Early design methods relied solely on small-signal device information. Although such methods were capable of predicting frequencies of oscillation with reasonable accuracy, they did not adequately address power-related concerns. A method was subsequently derived that relied on a quasi-static model understanding of device-circuit interactions in oscillators to formulate conditions for optimal large-signal performance [14]. There are two principal conditions that need to be met. They comprise a fundamental-frequency conjugate impedance match at the intrinsic drain-source port of the device, and adequate drain-to-gate feedback. Whereas the latter is determined by frequency stability considerations, the drain-source impedance matching conditions are described by a resistive load line in the transistor's dynamic current-voltage plane, chosen to deliver optimum net output power to an external load, as illustrated in Fig. 9. The matching conditions resemble those encountered in the design of power amplifiers, striving to maximize the product of drain-source voltage and current swings.

As in the power amplifier case, the design of an oscillator can be carried out entirely in the frequency domain, using conventional synthesis techniques in conjunction with a linearized quasi-static transistor model. Nonlinearities are again assumed to be confined to transconductance and output conductance elements, as described by their dynamic drain-source current-voltage characteristics. These are used to determine the optimum load-line slope, and can often be approximated with

sufficient accuracy based on knowledge of the static device current-voltage characteristics. Depending on the situation, the static characteristics may have to be corrected for the effects of temperature and carrier trapping. With the load line and the drain-to-gate feedback ratio defined, the circuit design task reduces to the synthesis of a linear two-port prototype coupling network with a total of four degrees of design freedom. The prototype network, as indicated in Fig. 10, consists of either a T- or Π-arrangement of two lumped reactances and one complex-valued impedance which incorporates the external load of the original three-port coupling network. The prototype network is subsequently converted into a microwave circuit realization of the sought-after three-port coupling network.

The same basic approach applies to the design of frequency-tuned oscillators, with the difference that fixed-frequency procedures must be repeated for a representative set of oscillation frequencies within the tuning bandwidth of interest to determine optimum prototype element values as a function of tuned frequency. The two prototype reactances generally exhibit negative slopes when plotted against oscillation frequency and have to be implemented with varactors or YIG-devices. The complex-valued prototype element is realized in the actual circuit as a reactive two-port network terminated with the external load.

Field-effect transistors also make good frequency doublers, which can be employed to extend microwave signal generation beyond the normal frequency range limits of fundamental-frequency oscillation [15]. To maximize conversion efficiency, static bias conditions must be chosen so as to best exploit quadratic device nonlinearities. Again, the dominant nonlinearities – and the only ones that need to be accounted for in most practical applications – are those associated with transconductance and output conductance elements in the device equivalent circuit. The full-fledged nonlinear nature of the doubler design problem, however, renders earlier-discussed linearization schemes no longer tractable. Harmonic-balance approaches are normally resorted to, used in conjunction with a device model that has validity across the spectrum of relevant signal frequencies.

Microwave FETs can also perform dual roles as efficient oscillator-doublers. Circuits of this type comprise oscillators with device ports terminated in reactive impedances at all but the second harmonic of the oscillation frequency [15]. In addition, FETs can also be employed as optical detectors, exploiting the light sensitivity of device characteristics to recover high-frequency modulation signals from optical carriers. There is particular interest in the use of 1.3-μm-wavelength light which offers minimum signal dispersion and near-minimum attenuation in stepped-index single-mode optical fibers. The key is finding a transistor made from channel materials with bandgap energies small enough to absorb light of this wavelength. Although microwave transistors suitable for detection of shorter-wavelength light are quite readily available, devices with materials configurations suitable for 1.3-μm operation are typically designed for applications at high millimeterwave frequencies and possess semiconductor layer thicknesses that are considerably smaller than the light absorption length, yielding inefficient optical detection.

Shown in Fig. 11, as proof of concept, is the response of an InP-based millimeterwave HEMT to incident 1.3-μm light, exhibiting the typically observed frequency dependence that results from differing participation among holes and electrons [16]. Responsivity could be readily increased by resorting to a custom-designed JFET structure with an InGaAs channel. To further illustrate the versatility of the microwave field-effect transistor, a 40-GHz heterodyne optical receiver was implemented that relies on a single InP-based HEMT in a four-function role to simultaneously provide optical carrier demodulation, self-generation of a local oscillation signal, internal frequency doubling thereof, and signal downconversion to a lower intermediate frequency. The design of the circuit was accomplished with the help of a quasi-static model representation of the transistor, confining nonlinearities to the two main voltage-dependent equivalent-circuit elements. The measured receiver response to optical excitation of variable modulation frequency is depicted in Fig. 12 for a constant incident optical signal level. The individual curve segments correspond to the direct-detection band, the two side bands of the local oscillation signal, and the lower sideband of its second harmonic, respectively.

Conclusions

With the microwave FET, in its varying forms of implementation, having achieved a position of prominence over the years, the ability to accurately predict device performance in both linear and nonlinear circuit settings has remained an area of focused research efforts. Starting out from a basic quasi-static nonlinear modeling approach, refinements and additions have progressively evolved to include influences of temperature, impact ionization, carrier trapping, and optical illumination. Modeling techniques have developed to the point where considerable sophistication can be brought to bear in applications that demand it. There still remains, however, a wide range of circuit design problems, for which the basic quasi-static approach can be put to good use, without unduly compromising accuracy.

Acknowledgment

The author wishes to thank his colleague, Dr. W. Kruppa, for many valuable comments and suggestions.

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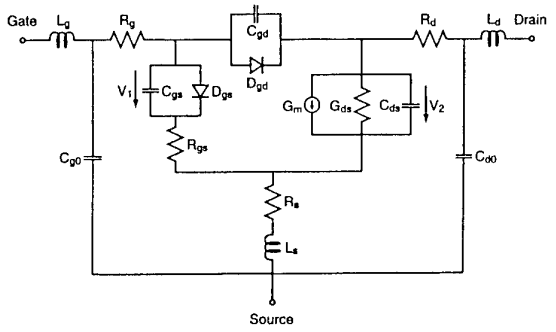

Fig. 1. Nonlinear equivalent-circuit model of a microwave FET.

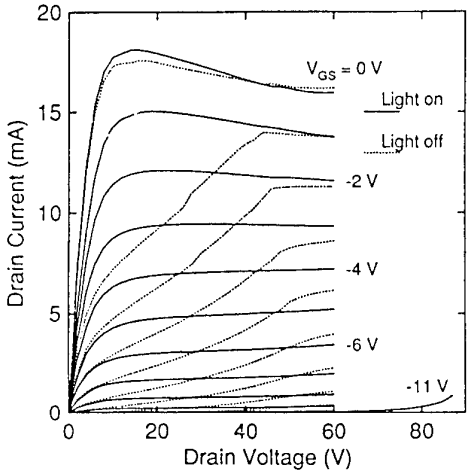

Fig. 2. Output static current-voltage characteristics of an experimental GaN FET, with and without optical illumination.

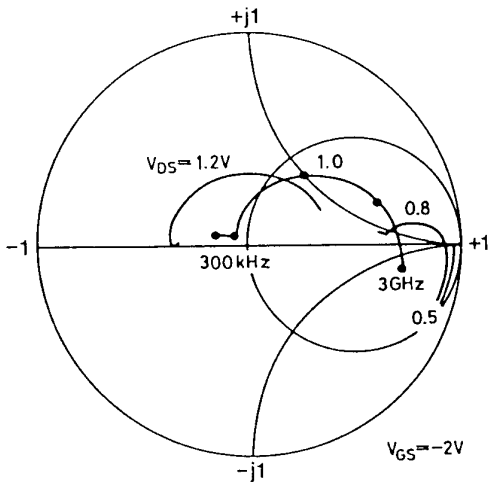

Fig. 3. Output reflection coefficient, plotted as a function of frequency and drain-source bias voltage, for an experimental HEMT with a narrow-bandgap InAs channel.

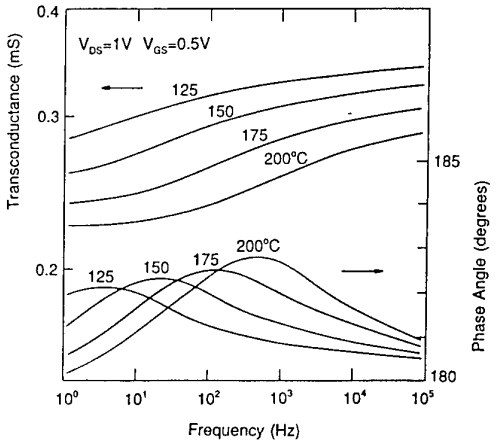

Fig. 4. Transconductance and associated phase angle for an experimental GaN FET, plotted as functions of frequency and temperature.

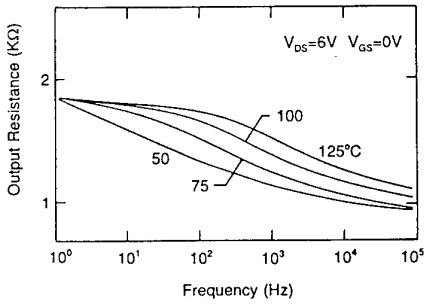

Fig. 5. Output resistance dispersion of the GaN heterojunction FET, plotted as a function of frequency and temperature.

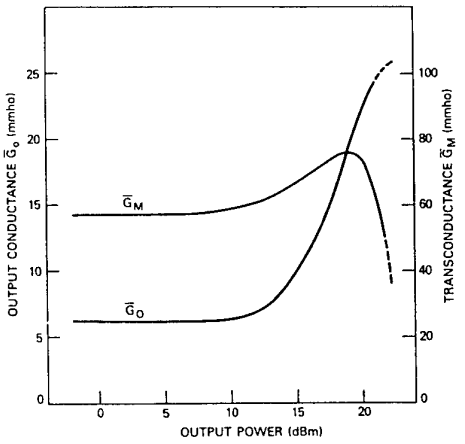

Fig. 6. Large-signal-equivalent transconductance and output conductance of a GaAs FET as functions of fundamental-frequency output signal power.

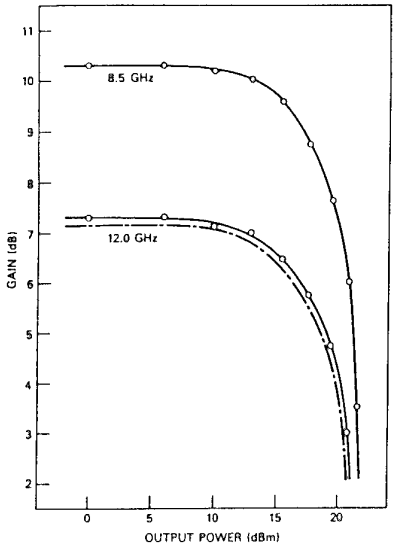

Fig. 7. Gain versus fundamental-frequency output power for a GaAs FET:
——— measured, — — — predicted.

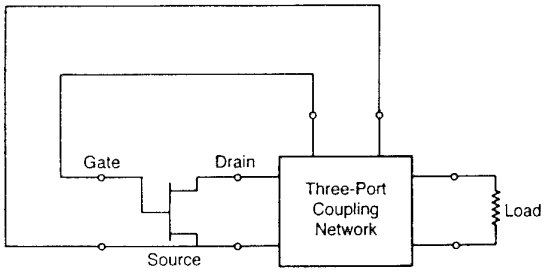

Fig. 8. Schematic of a microwave FET oscillator.

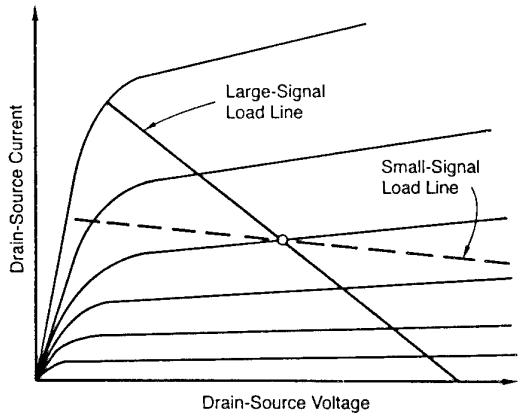

Fig. 9. Large-signal and small-signal load lines superimposed on the dynamic output current-voltage characteristics of a microwave FET.

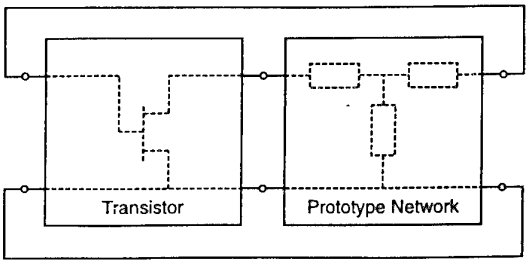

Fig. 10. Prototype circuit for a microwave FET oscillator.

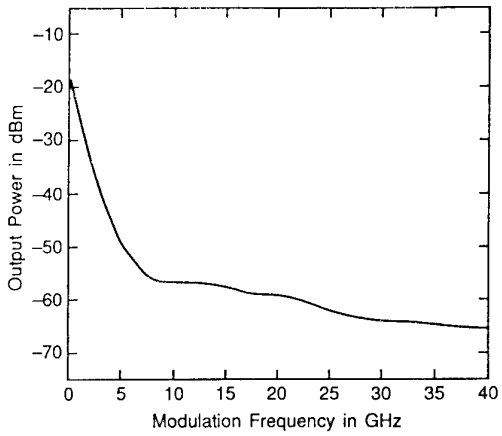

Fig. 11. Photodetection characteristics of an InP-based microwave transistor for 6 dBm of incident 1.3-μm-wavelength optical power.

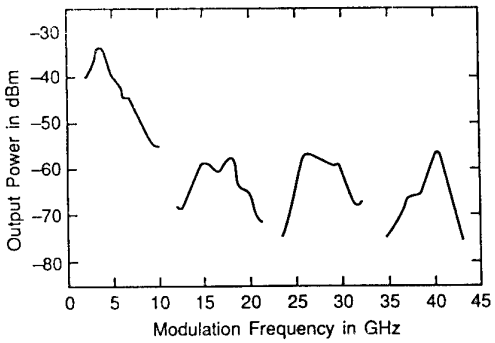

Fig. 12. Response of an InP-transistor-based heterodyne receiver to 6.5 dBm of incident 1.3-μm-wavelength optical power, plotted as a function of modulation frequency.

Procedure to extract the non-linear HEMT model from vectorial non-linear network analyzer measurements

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Abstract

Non-linear models for microwave and millimetre devices are commonly based on DC and S-parameter measurements, due to the absence of vectorial large-signal measurements in the past. At present, accurate prototype measurement systems are being developed, which implies that new non-linear modelling techniques can be explored. We will present a method that allows the direct extraction of the state-functions of a HEMT.

I. Introduction

An accurate description of the non-linear behaviour of electronic components is mandatory for adequate circuit design. A common technique to acquire the non-linear model of diodes and transistors is to make a small-signal approximation of the non-linear state-functions at different bias points [1]. This technique requires a large amount of S-parameter measurements. The minimum number of required measurements can be significantly reduced by extracting the state-functions directly from large-signal measurements. Due to the recent availability of measurement systems that allow the simultaneous measurement of both the amplitude and the phase of the harmonics of the travelling voltage waves [2,3], new modelling methods can be developed. Previously, methods have been presented which rely partially on linear measurements [4] or which are only valid at relatively low input powers so that the bias-dependency of the time constants doesn't come into play [5]. It is the aim however to extract directly all the charge and current state-functions, as has been demonstrated for a one-port [6].

This article will describe the procedure to determine the complete quasi-static non-linear model of a two-port device. The theoretical analysis will be developed in Section II. We will show in Section III that the efficiency of the method is strongly determined by the choice of the excitation signals. The proposed method will be illustrated on a HEMT in Section IV. Finally, the conclusions will be drawn in Section V.

II. Direct extraction of the state-functions

The purpose of this analysis is the direct extraction of the state-functions from vectorial non-linear network analyzer measurements. We concentrate to the particular example of a HEMT, but a similar analysis can be developed for other microwave and millimetre wave non-linear components.

The intrinsic quasi-static non-linear HEMT model is shown in Figure 1. It consists of the parallel connection of a charge source $Q_i\left(V_1(t), V_2(t)\right)$ and a current source $I_i\left(V_1(t), V_2(t)\right)$ with i=1,2 both at the gate-source terminal (port 1) and at the drain-source terminal (port 2). The incident and the scattered travelling voltage waves are measured at the extrinsic device plane. After de-embedding the extrinsic elements, the intrinsic terminal currents I_{mi} and voltages V_i with $i = 1, 2$ can be calculated. This two-port can be described by the following equations in the time domain:

$$I_{m1}(t) = I_1\left(V_1(t), V_2(t)\right) + \frac{\partial Q_1\left(V_1(t), V_2(t)\right)}{\partial t} \quad (1)$$

$$I_{m2}(t) = I_2\left(V_1(t), V_2(t)\right) + \frac{\partial Q_2\left(V_1(t), V_2(t)\right)}{\partial t} \quad (2)$$

and in the frequency domain:

$$\mathcal{F}(I_{m1}(t)) = \mathcal{F}\left(I_1\left(V_1(t), V_2(t)\right)\right) + j\Omega\mathcal{F}\left(Q_1\left(V_1(t), V_2(t)\right)\right) \quad (3)$$

$$\mathcal{F}(I_{m2}(t)) = \mathcal{F}\left(I_2\left(V_1(t), V_2(t)\right)\right) + j\Omega\mathcal{F}\left(Q_2\left(V_1(t), V_2(t)\right)\right) \quad (4)$$

where $\mathcal{F}$ stands for the Fourier series, which is valid when the excitation is a single-tone signal, and with the diagonal matrix $\Omega = diag\left\{0\ \omega_0\ 2\omega_0\ \ldots\ H\omega_0\right\}$ with ω_0 the fundamental pulsation and H the number of measured harmonics.

According to the frequency domain Equations (3) and (4), there are at each port H complex equations and $2H$ complex unknowns. This could be solved by

performing two measurements at two different fundamental pulsations but where both the spectra $\mathcal{F}(V_1(t))$ and $\mathcal{F}(V_2(t))$ have to be kept fixed. In practice, it is not straightforward to implement this method, because it is difficult to impose the constant spectrum $\mathcal{F}(V_1(t))$ and $\mathcal{F}(V_2(t))$. A reason is that the considered $V_1(t)$ and $V_2(t)$ are defined at the intrinsic device plane, since the parasitic elements have been deembedded. More important is that in reality not $V_1(t)$ and $V_2(t)$ is applied but the travelling voltage wave $a_1(t)$. When using a one-tone synthesiser, the amplitude at the fundamental frequency f_0 of $\mathcal{F}(V_1(t))$ can be adjusted by sweeping the power of the synthesiser. The corresponding amplitude at f_0 of $\mathcal{F}(V_2(t))$ is determined by the physics of the device. Since we want to reduce the number of necessary measurements to deduce the complete non-linear model, we have to cover a larger part of the considered bias range within one large-signal measurement. This can be done by increasing the incident power, but this implies that the higher harmonics of $\mathcal{F}(V_1(t))$ and $\mathcal{F}(V_2(t))$ become significant. In this case, the single-tone synthesiser is not sufficient to define the complete spectrum. A solution is the use of a broadband multi-sine source [7], which allows the control of both amplitude and phase of the harmonics. Since these multi-sine sources are not widely used, it would require additional hardware and development time to have a versatile instrument dedicated for this purpose.
By defining

$$C_{ij}\left(V_1(t), V_2(t)\right) = \frac{\partial Q_i\left(V_1(t), V_2(t)\right)}{\partial V_j(t)} \tag{5}$$

with $i, j = 1, 2$, Equations (1) and (2) can be rewritten as:

$$I_{m1}(t) = I_1\left(V_1(t), V_2(t)\right) + \sum_{j=1}^{2} C_{1j}\left(V_1(t), V_2(t)\right) \frac{dV_j(t)}{dt} \tag{6}$$

$$I_{m2}(t) = I_2\left(V_1(t), V_2(t)\right) + \sum_{j=1}^{2} C_{2j}\left(V_1(t), V_2(t)\right) \frac{dV_j(t)}{dt} \tag{7}$$

These are 2 equations and 6 unknowns.

This set of equations can be solved by performing three large-signal measurements at three different pulsations, when only a single-tone a_1 is applied. At time points t_1, t_2, t_3 where instantaneously $V_1(t_1) = V_1(t_2) = V_1(t_3)$, $V_2(t_1) = V_2(t_2) = V_2(t_3)$, $\frac{dV_1(t_1)}{dt} \neq \frac{dV_1(t_2)}{dt} \neq \frac{dV_1(t_3)}{dt}$ and $\frac{dV_2(t_1)}{dt} \neq \frac{dV_2(t_2)}{dt} \neq \frac{dV_2(t_3)}{dt}$, the Equations (6) and (7) can be solved.

The need for three independent measurements increases significantly the minimum number of vectorial non-linear network analyzer measurements to be taken in order to generate a complete non-linear model. This implies that the minimum number of required measurements will not be significantly less compared to the number of bias points at which S-parameter measurements are performed in the common non-linear model generation procedure. Therefore, it is mandatory to exploit all the degrees of freedom in the VNLNA measurement set-up to reach an excellent coverage of the $(V_1 - V_2)$ bias plane within one measurement.

III. Optimal coverage of the state-variables plane

In the preceding analysis, only a single-tone signal was applied to port 1. At a fixed fundamental frequency, the degrees of freedom are only the DC gate-source (V_{10}) and gate-drain (V_{20}) bias conditions and the incident power level. This limits the bias range which can be covered in one large-signal measurement. Due to the inverter characteristic of a HEMT, it is not possible to cover sets of high V_1 and V_2 values or low V_1 and V_2 values. A better coverage of the $(V_1 - V_2)$ bias plane can be obtained by engineering properly the applied signals at port 1 and port 2, given the actual DUT [8]. Indeed, the present VNLNA measurement set-up allows to inject simultaneously signals at both port 1 and 2. With only one additional single-tone synthesiser, the magnitude, phase and frequency of a_2 can be varied. By varying the phase of a_2 relative to the phase of a_1, a better coverage of the $(V_1 - V_2)$ plane can be obtained. This is illustrated in Figure 2, where the time domain waveform of V_2 is shown as a function of the time domain waveform of V_1 for no a_2 present and for the phase of a_2 being 0° and 30°. It is important to note that this is equivalent to the electronic variation of the load presented to the transistor. In other terms, the same effect can be obtained by performing load-pull measurements by which the fixed 50 Ω load is replaced by a variable load [9]. Furthermore, by applying a frequency shift to a_2 relative to a_1, intermodulation products are generated which results in a $V_2(t)$ time domain waveform versus $V_1(t)$ time domain waveform that will cross more different values of (V_1, V_2) within one measurement sweep, compared to a single-tone a_1. This is demonstrated in Figure 3.

An example which combines both techniques, which are phase variations and frequency shifts, will be presented in the next Section.

Ultimately, it is the goal to design one multi-tone multi-port signal that passes three times through each (V_1, V_2) point with three different time derivatives of V_1 and V_2. Theoretically, one large-signal measurement would then be necessary to get the non-linear model for the HEMT.

IV. Practical example: GaAs PHEMT

We demonstrate the potential of the decomposition of the travelling voltage waves into the non-linear state-functions on a GaAs PHEMT with 0.2 μm gate length and 100 μm gate width. In order to distinguish

clearly the capacitive effects, a high fundamental frequency is required. To maximise the number of bias points covered by one large-signal measurement, the input powers of both a_1 and a_2 should be large. This will involve a high number of non-negligible harmonics and intermodulation products to be measured. It is not possible to combine these two requirements, given the current 25 GHz bandwidth of the VNLNA measurement system. An extraction from actual VNLNA measurements on a single-gate HEMT would require a number of VNLNA measurements comparable to the number of necessary S-parameter measurements in the adaptive Root model [10]. Therefore, we have simulated the non-linear HEMT model by harmonic balance (HB) analysis. The non-linear state-functions are calculated from the time domain waveforms and compared with the state-functions derived from S-parameter measurements. The algorithm has been implemented in Mathematica. The first task is to find an excitation to optimise the coverage of the $(V_1 - V_2)$ bias plane. To be able to solve the Equations (6) and (7), the $V_2(t)$ time domain waveform as a function of the $V_1(t)$ time domain waveform has to cross at least three times each square defined by $(V_1 - \Delta V_1, V_2 - \Delta V_2)$ and $(V_1 + \Delta V_1, V_2 + \Delta V_2)$ with Δ an infinitesimal small voltage offset. For a good solvability, the three associated time derivatives of V_1 and V_2 have to be significantly distinct. Several excitation schemes can be investigated and compared in terms of hardware requirements, acquisition speed and accuracy. The example given here is to show at which bias points the state-functions can be evaluated with only four non-linear simulations. Therefore, we have applied a travelling voltage wave a_1 of 4 dBm at f_0 equal to 6 GHz and a travelling voltage wave a_2 of 12 dBm at f_0 equal to 5.9 GHz. The DC bias conditions are $V_{10} = 0.4\ V$ and V_{20}= 1 V. The phase of a_1 has been kept fixed to 0°, while the phase of a_2 has taken the values of 0°, 30°, 45° and 90°. The HB analysis calculates ten harmonics and intermodulation products. The covered bias range using these conditions is shown in Figure 4. Using only these four simulations, we have calculated the state-functions on a 50 mV grid for V_1 and a 100 mV grid for V_2. Neglecting I_1 (or I_{gs}) and considering the integrability conditions [11], the necessary (V_1, V_2) dependent functions are C_{22} (or C_{ds}) (Figure 5), I_2 (or I_{ds}) (Figure 6) and C_{11} (or C_{gs}) (Figure 7). Each Figure compares the values obtained from S-parameter measurements and those obtained by the HB-simulation and which satisfy the solvability conditions.

We observe that four large-signal measurements are not sufficient to describe accurately the complete bias plane. However, the main purpose of this practical example is to demonstrate the basic principle of extracting the non-linear state-functions directly from large-signal measurements. The good agreement obtained between the S-parameter measurements and HB-analysis based state-functions validates the theory.

V. Conclusions

The complete non-linear quasi-static model of a HEMT can directly be extracted from vectorial non-linear network analyzer measurements. Compared to a S-parameter measurements based non-linear model, the minimum number of required measurements is several orders of magnitude smaller, providing the degrees of freedom of the VNLNA have been well exploited. The technique to directly generate non-linear models from vectorial large-signal measurements is not limited to HEMTs, but offers a valuable prospect and an innovative approach to efficiently generate non-linear models for a wide spectrum of components which are used in microwave and millimetre wave applications.

Acknowledgements

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The authors express their gratitude to the complete staff of the division TELEMIC, the group HP-NMDG and the MMIC processing group at IMEC. D. Schreurs is supported by the National Fund for Scientific Research as a Research Assistant.

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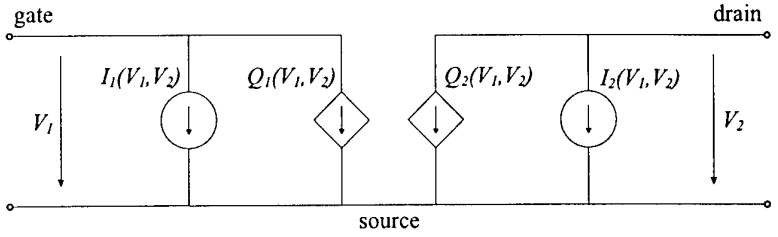

Figure 1: Intrinsic quasi-static non-linear HEMT model.

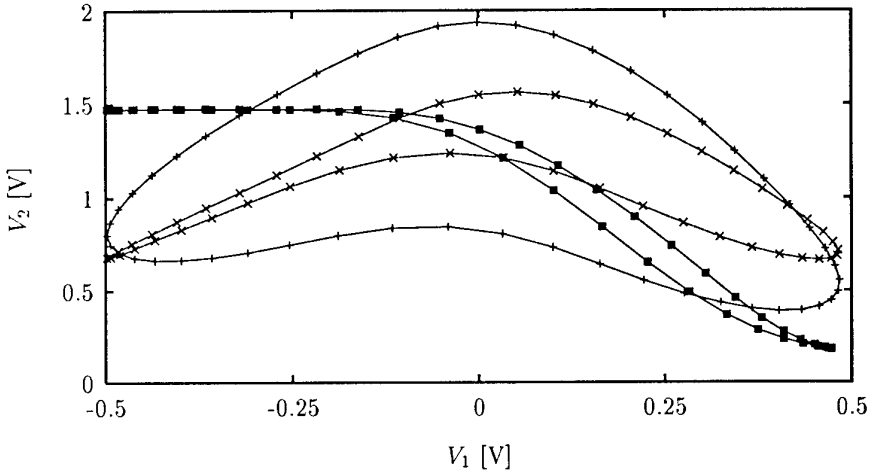

Figure 2: Coverage of the (V_1, V_2) plane by injecting a_1= -2 dBm 0° and no a_2 (▪), a_2= 3 dBm 0° (x) and a_2= 3 dBm 30° (+) at f_0= 6 GHz.

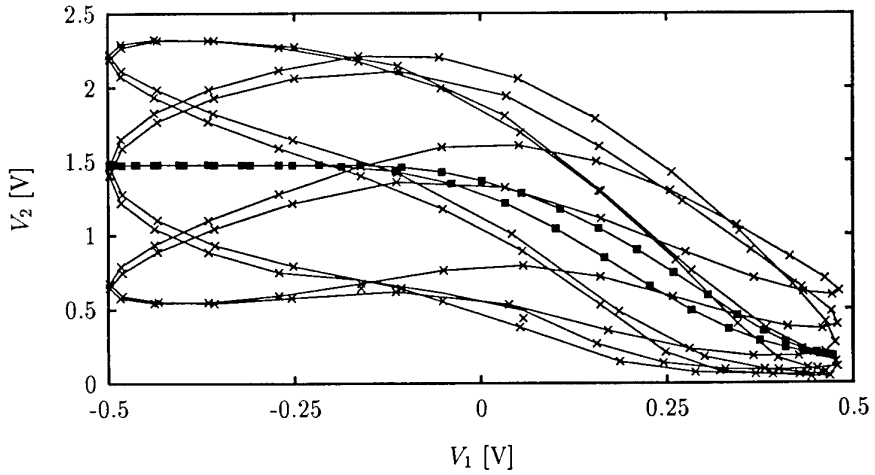

Figure 3: Coverage of the (V_1, V_2) plane by injecting a_1= -2 dBm at f_0=6 GHz combined with no a_2 (▪) and a_2= 3 dBm at f_0=5 GHz (x).

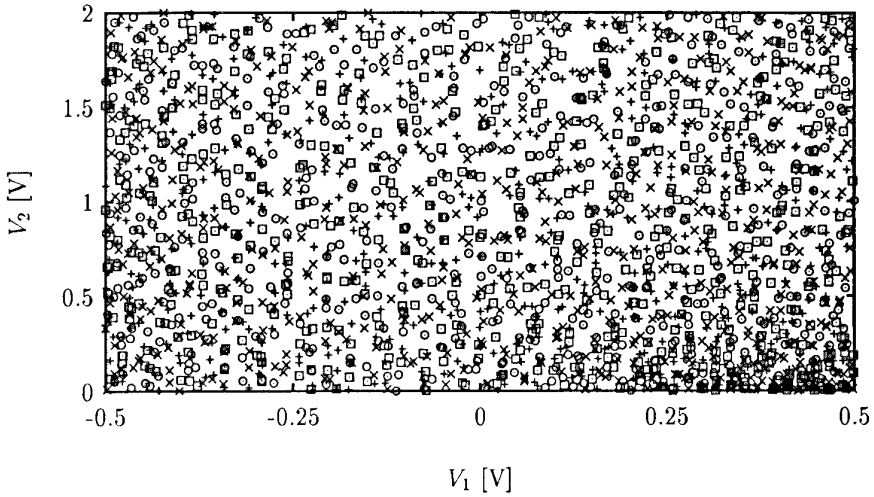

Figure 4: Coverage of the (V_1, V_2) plane by injecting $\phi(a_1) = 0°$ and $\phi(a_2) = 0°$ (+), $\phi(a_2) = 30°$ (x), $\phi(a_2) = 45°$ (□) and $\phi(a_2) = 90°$ (○).

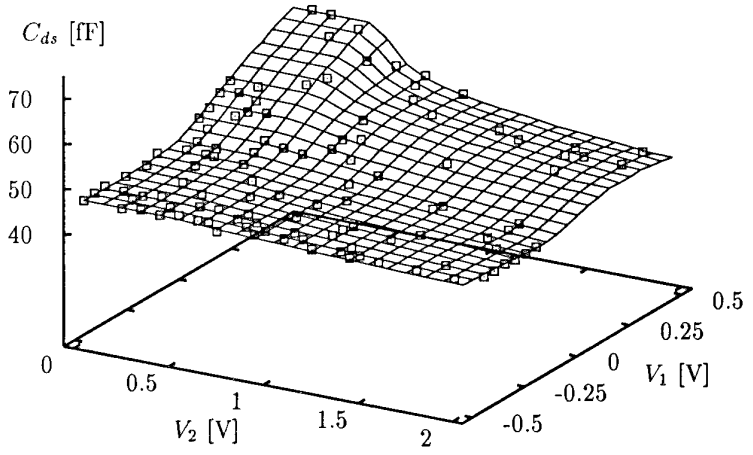

Figure 5: C_{ds} of a 100 μm GaAs PHEMT extracted from S-parameters (—) and from HB-simulations (□).

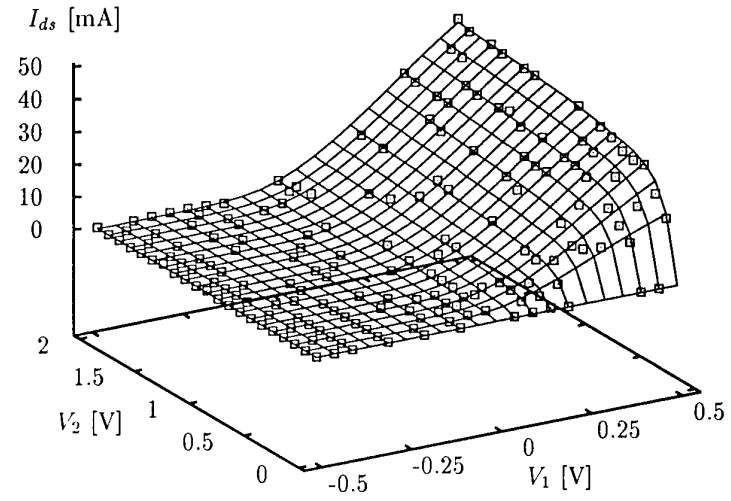

Figure 6: I_{ds} of a 100 μm GaAs PHEMT extracted from S-parameters (—) and from HB-simulations (□).

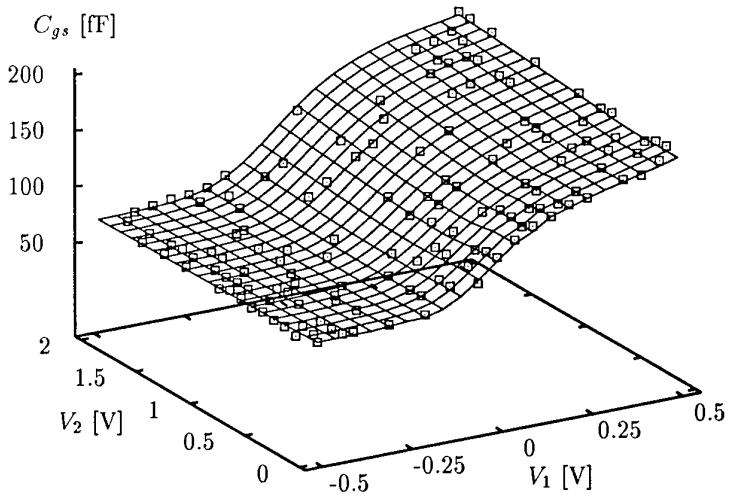

Figure 7: C_{gs} of a 100 μm GaAs PHEMT extracted from S-parameters (—) and from HB-simulations (□).

Experimental research in table-based FET models

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Abstract

This paper deals with some aspects related to the extraction and experimental verification of table-based models. Considering several nonquasi-static approaches, a quick and accurate measurement approach for model extraction is proposed. Model consistency and scaling with gatewidth has been taking into account. Model verification has been performed under dc, small and large-signal excitations for P-HEMT devices.

Introduction

Many applications, such as mobile and satellite communications, require high performance MMICs in which high power and efficiency are leading goals. As a consequence, nonlinear models are required in the CAD of those circuits that can provide accurate predictions under large RF signal excitations. Accuracy in empirical nonlinear models is related with model formulation and device characterization. Table-based approaches have demonstrated their ability to give an accurate and detailed nonlinear prediction. They can be considered as a general modelling tool for different devices and technologies [1-9].

From a practical point of view, models should be computationally efficient and also the characterization process has to be quick and easy to perform. Since accuracy and time consumption in device model generation is very important, the extraction of several table-based approaches and their experimental validation will be considered.

Modelling Approach

Consider initially the modelling approach proposed by Root et al. [3]. This approach uses a nonquasi-static current formulation to model low-frequency dispersion in the output, and a quasi-static formulation for charges. Based on that model, but using nonquasi-static charges, we will also consider an approach developed by the authors [8]. This approach is further simplified through the use of linear delays. A general expression for current at i-th terminal in both models is

$$I_i(t) = \left[1 + \tau_x \frac{d}{dt}\right]^{-1} I_i^{low}(V_{GS}, V_{DS}) + \left[1 + \tau_x \frac{d}{dt}\right]^{-1} \tau_x \frac{d}{dt} I_i^{high}(V_{GS}, V_{DS}) + \frac{dQ_i(t)}{dt} \quad (1)$$

In this equation Q_i is the charge relation at i-th terminal, quasi-static in Root approach and nonquasi-static in our approach. Expression (1) is the result of considering the low-frequency dispersion modelling applied to the input and output of the device. Even in the case of a neglectable dispersion in the input, as we have observed, it is interesting to consider an unique general formulation for both ports.

In the case $\omega\tau_x >> 1$, after model linearization with respect to gate-source and drain-source voltages, we obtain the following small-signal (common-source) Y-parameters:

Root approach [3]: $Y_{ik} = g_{ik}^{ac} + j\omega c_{ik}$ (2)

Our approach [8]: $Y_{ik} = g_{ik}^{ac} + \omega^2 \tau_i c_{ik} + j\omega c_{ik}$ (3)

As can be seen, the latter approach includes a correction term in the real part of the Y-parameters, which provides for an increased bandwidth over the initial Root approach. Model generation from data is performed as described in [3,8]. Uniqueness of the model requires that some relations hold [3,10], and those have also been checked by the authors. These approaches can be scaled with gatewidth.

Device Characterization and Model Extraction

These models can be extracted from *direct* and *indirect* RF nonlinear measurements [11,12,17]. Considering the extraction from dc and indirect RF methods (small signal data vs. bias), we find different choices. One is the classical way, i.e. *S-parameters*

frequency scans at different bias points. This method is very time consuming since for an accurate nonlinear characterization we need to measure a dense set of bias points. The number of points can be decreased using *adaptive measurements*, collecting more points where nonlinearities are stronger [3]. An alternative solution, we propose, is using *S-parameters single-frequency bias-scan measurements* (rf Bias Scans or simply Bias Scan) [13]. A single Bias Scan can be performed at the same speed as a single frequency scan, but in this case collecting nonlinear information (at a single frequency) at, for example, 51 bias points instead of just one. This measurement mode allows the extraction of these models from a set of different Bias Scans in a shorter time, providing for detailed nonlinear characterization. Only dc data (dc Bias Scans) and some extra frequency scans (for extracting the external parasitic network) need to be additionally performed.

In this work, we have used that measurement strategy (i.e. dc and rf Bias Scans) for model extraction. Dc data have been used in both models to generate the low-frequency large-signal currents and to perform the voltage referencing to the intrinsic level [14,15]. Dc voltage drops in bias tees have been accounted for. This measurement approach is ideally suited to the Root approach because that model can be directly extracted at single frequency (see eq. 2). In our proposal, since τ_i is linear, we can further simplify model extraction and use mainly single-frequency Bias Scan data. At low frequencies ($\omega\tau_x >> 1$ and $\omega\tau_i << 1$), current and charge relations can be extracted at a single frequency while τ_i can be obtained from a single Bias Scan at several frequencies or a single frequency scan at just a single bias point (using, in both cases, frequency dependent y-parameters experimental data to fit eq. 3 [8,10]). We have chosen the first option because having the delay information extracted at 51 bias points enables us to find a more accurate effective value of these parameters than considering only the information extracted at a single bias point.

It is also important to check rf model consistency [10,15]. Figure 1 shows the evaluation of the consistency relations for the extrinsic device (in this case a P-MODFET) in the whole I-V range. It is important to note that we have also checked the relations corresponding to the high-frequency input current (not shown in [15]). We have concluded, as in [15], that they *approximately* hold not only in the output but also in the input of the device, both for the rf large-signal currents and charges. However, because of this "approximate" behaviour (originated by inherent mathematical errors related with the numerical processing, measurement uncertainties and influence of low-frequency dispersion) we have observed that rf model extraction is approximately path-independent for devices with relatively small low-frequency dispersion effect (see figure 2) and strongly path-dependent for devices with wild dispersion behaviour. With this problem in mind, we have developed an extraction software that interactively allows the user to choose and check different integration paths and boundary conditions during measurement, thus allowing to improve accuracy during extraction [13]. Applying this approach, we have determined that using mainly Gate Scans for model extraction it is possible to get very accurate results for y_{21} and y_{11} at expense of some inaccuracies (in the forward regime) in the two remaining parameters (figure 3a) [10]. In the case of using mainly Drain Scans we find accurate results for y_{12} and y_{22} (figure3b).

Experimental Model Verification

These models have been generated for GaAs-based δ-doped P-HEMT devices fabricated at Fraunhofer Institut (IAF, Freiburg, Germany). For extracting intrinsic rf current and charge nonlinear relations in both models we have used bias scans at 2 GHz. For extracting τ_i values in our approach, measurements were performed in the range 0.5 to 40-50 GHz for devices considered in this work. A rough estimation of τ_i could also be obtained from classical linear models; for example, τ_g can be obtained from $r_i * c_{gs}$ product. In this case, it is possible then to substitute the bias scans measurements at different frequencies by an optimization process performed in the simulator.

Large-signal measurements have been done using an on-wafer vector-calibrated large-signal measurement system described in [16]. Both models were easily implemented in MDS using SDDs [10], and simulated under dc, small and large-signal excitations.

If we extract the quasi-static charge model at different frequencies, intrinsic high-frequency currents are strongly frequency dependent (fig.4a) while quasi-static charges are approximately frequency independent (fig. 4b). This implies the necessity, at least up to first order, of a correction term in the real part of the simulated Y-parameters (eq. 3) over Root initial approach (eq. 2). Figure 5 shows that our quadratic additional term is sufficient to model the devices over a bandwidth extending to at least their f_T values [18].

It is also interesting to check whether our approach can be properly scaled with gatewidth. Of course, to prove it, first we must be sure that technology is scalable (e.g. comparing gatewidth-normalized dc I-V curves from devices having different widths), and that we are using proper scaling rules for device parasitics (e.g. checking parasitics with linear models for different gatewidths). Nonlinear model scalability can be checked comparing gatewidth-normalized current and charge large-signal relations from devices having different widths. Figure 6 shows an example of such a comparison for 2x60μm and 2x30μm devices. As can be seen, large-signal high-frequency drain currents are scalable with gatewidth in both models considered in this paper. As a result, figure 7 shows the good agreement between the S-parameters obtained using our model (extracted for a 2x60μm device and scaled to a 2x30μm device) and from measurements for a 2x30μm device.

Figure 8 compares measured and simulated, using our approach, output power levels versus input power for the fundamental (16 GHz), second (32 GHz) and third harmonics (48 GHz, in the limit of the MTA measurement capability). Similar excellent results have also been obtained in the range of fundamental frequencies from 2 to 20 GHz. We have observed that not only the RF global behaviour can be perfectly predicted using our approach but also the RF dynamic behaviour and the static dc bias point [18].

Conclusions

In this paper we have discussed several aspects related with FET table-based model extraction and verification. S-parameters Bias Scans measurements have been used in this work as a valuable tool for an accurate nonlinear extraction. Model consistency, scaling with gatewidth and the importance of including nonquasi-static charges in nonlinear models to increase model bandwidth have also been considered.

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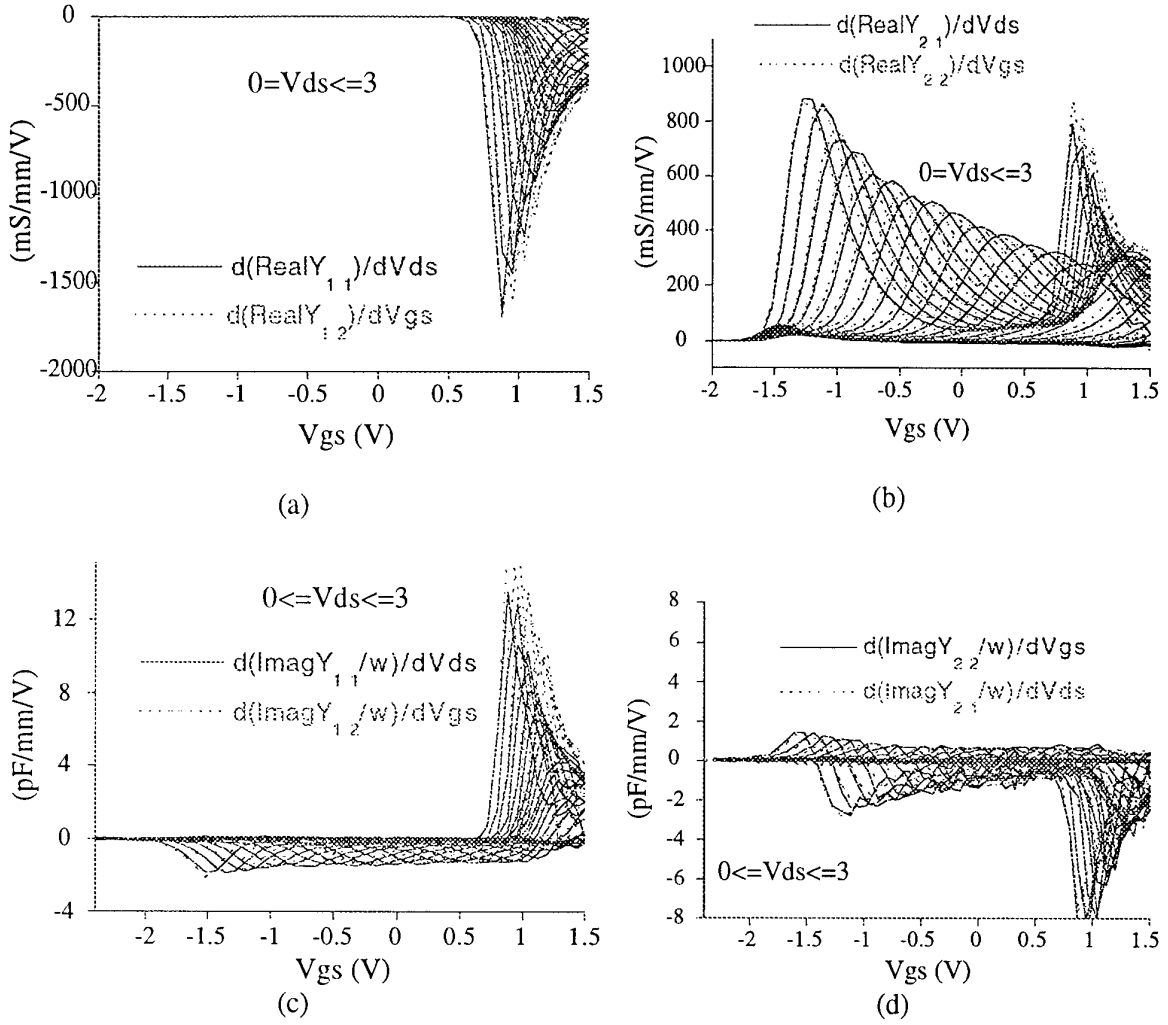


Figure 1. Model consistency checking vs. bias. Rf data have been measured at 2 GHz. Transistor: 100x0.6 μm^2. (a) Checking of equations involved in conservation of I_g^{high} ; (b) I_d^{high}; (c) Q_g, and (d) Q_d.

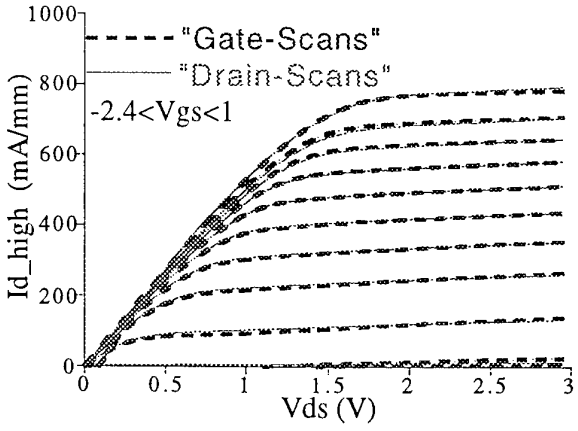
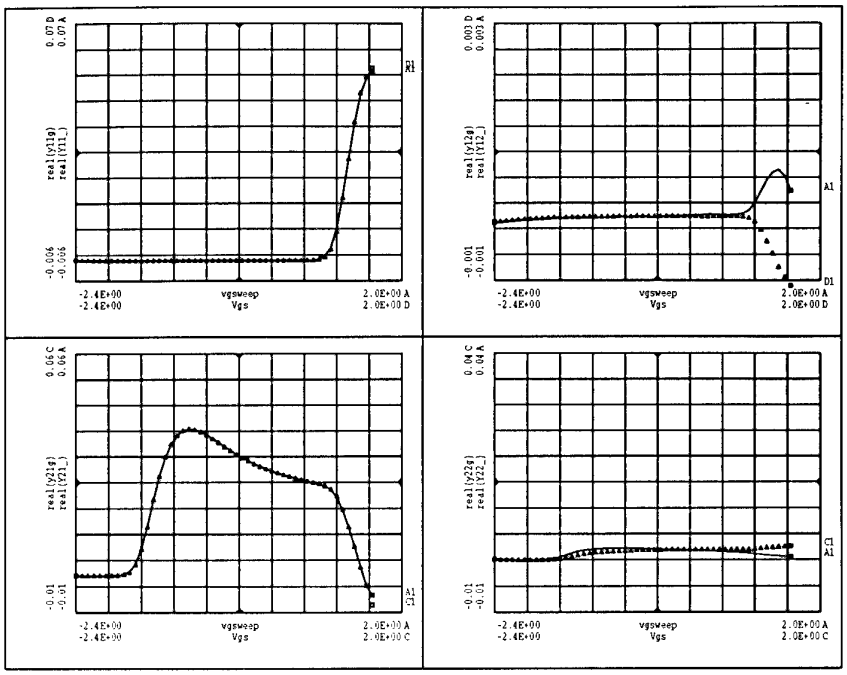
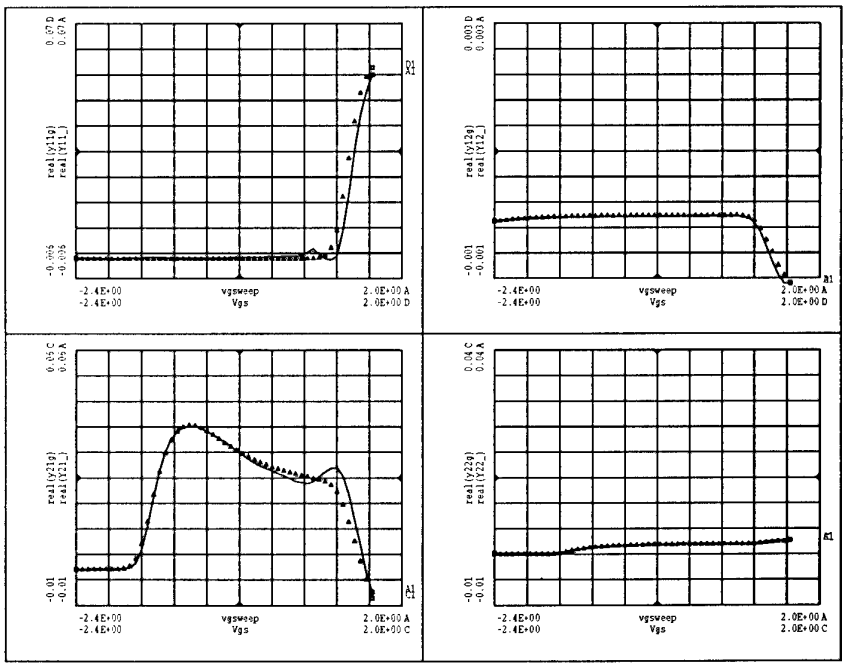


Figure 2. Intrinsic high-frequency drain current relation, I_d^{high}, obtained using a set of Drain Scans and Gate Scans for model generation. Transistor: 100x0.6 μm^2 P-HEMT. Bias Scans have been performed at 2 GHz.



(a)



(b)

Figure 3. Comparison between measured (triangles) and simulated (line) extrinsic real parts of the Y-parameters at 2 GHz (in Siemens). (a) The model has been obtained using a set of Gate Scans; (b) The model has been obtained using a set of Drain Scans. Transistor: 100x0.6 μm^2 MODFET. Bias Scans have been performed at 2 GHz.

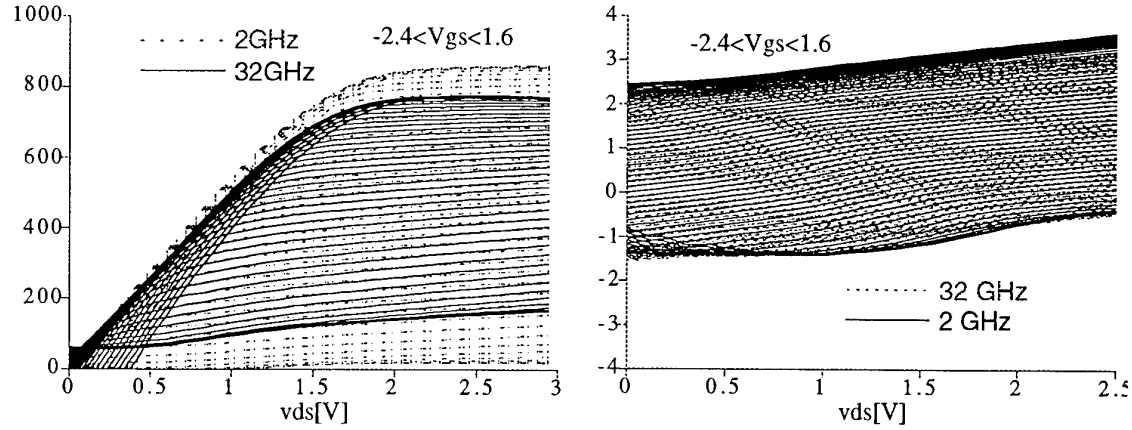


Figure 4. Intrinsic high-frequency drain constitutive relations extracted at 2 and 32 GHz for the quasi-static charge model. FET: 0.6x100 μm^2. It is important to note that this device has a f_T value of about 30 GHz. (a) Current relation in mA/mm (b) Charge relation in pF/mm.

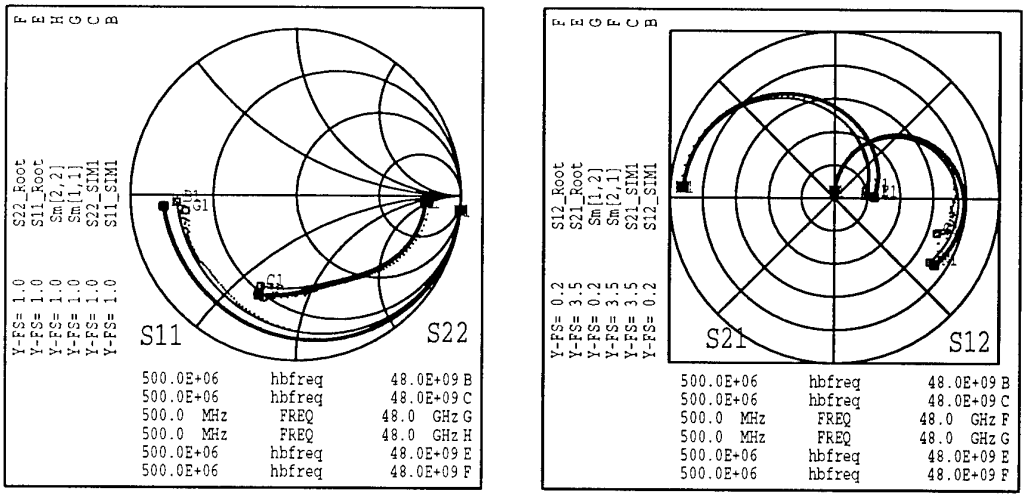


Figure 5. S-parameters vs. frequency in the range 0.5-48 GHz. FET: 0.6x100 μm^2. Bias point: Vgs0=-0.5 V, Vds0=2 V. Measurements (dotted), simulation using Root model (thick line) and simulation with our approach (thin line).

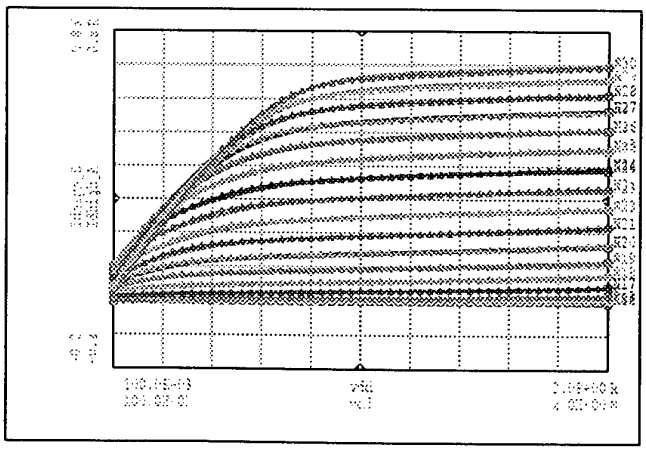


Figure 6. Comparison between intrinsic high-frequency drain current relations (in A/mm) for 2x30μm (triangles) and 2x60μm (line) gatewidth devices. Extracted at 2 GHz.

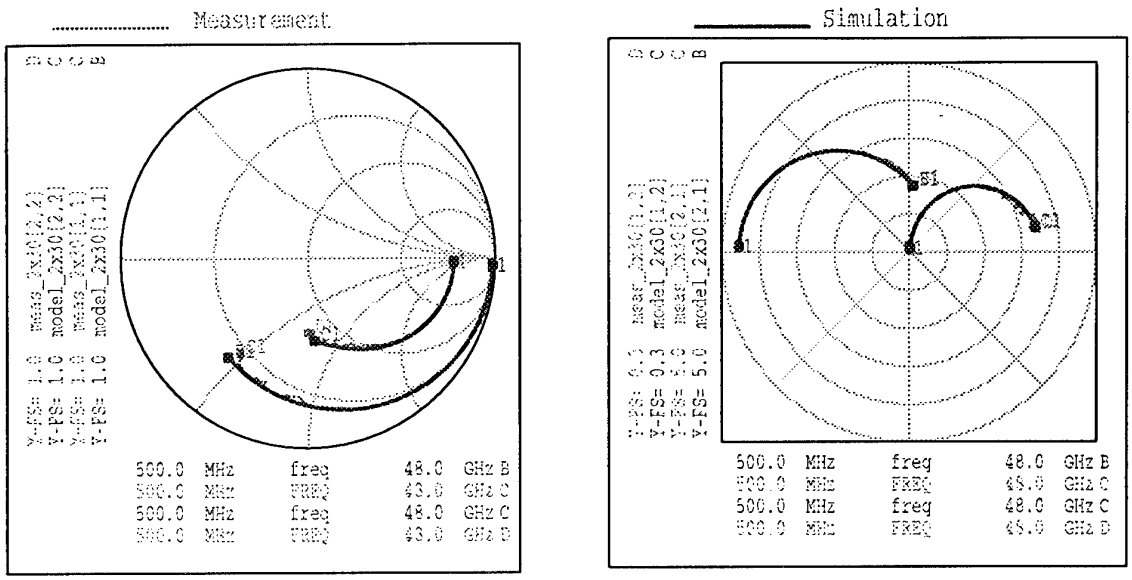


Figure 7. Comparison between measured and simulated S-parameters for a 2x30 µm (Lg=0.15 µm). P-HEMT. Bias point : Vgs0=0.45 V , Vds0=1.5 V. The nonquasi-static charge model (proposed by the authors) has been extracted for a 120µm gatewidth device and scaled to a gatewidth of 60µm. Frequency range from 0.5 to 48 GHz.

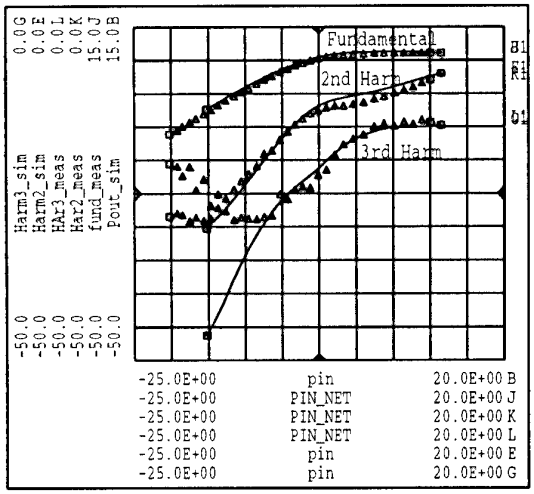


Figure 8. Measurements (triangles) and simulations (line). Fundamental power in dBm and harmonics in dBc. FET: 0.15x120 µm^2. Bias point: Vgs0=0.3 V, Vds0=1 V. Fundamental frequency: 16 GHz.

NOVEL EXPERIMENTALLY-BASED MODELING FOR MESFETS HAVING COMPLEX DISPERSION EFFECTS

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ABSTRACT Conventional experimentally-based models for MESFET assumes frequency-independencies of the port IV and QV characteristics of the device intrinsic part and a valid path-independence in integration of the characteristics. In real devices, it may not be the case. This paper reports a novel experimentally-based model to account for the RF dispersion effects and presents a solution for a path-dependence problem. The model can exactly simulate nonlinear DC performance and small-signal S-parameters as well as large-signal response. An example is given to show its capability of simulating complex DC and RF characteristics which show local negative conductance at RF frequency. Measured large-signal waveforms further verify the model.

INTRODUCTION

Experimentally-based models such as Root model have been successfully used to model highly nonlinear characteristics of MESFETs, HEMTs and Diodes[1,2,3]. They are essentially an experimentally-based approach and are therefore, technology-independent. However, conventional models assume no RF-frequency dependencies which are not valid in most cases. In a real device, simple PI shaped topology of a device equivalent circuit is inaccurate due to additional 2D effects such as Gunn domain. A modified complex equivalent circuit generally causes the port currents and charges to be frequency-dependent which has been a challenge for experimentally-based modeling. Physics-based modeling can handle the RF-dispersion effects. However, it requires deep understanding in device physics and good technology of parameter extraction which is prohibitively involved when the characteristics become more complex and therefore hinders its application.

To develop an experimentally-based model it requires path-independence in integration of the measured 2-D bias-dependent small-signal Y parameters with respect to the port voltages. However, the path-independence requirement is seldom to be met due to well-known low-frequency dispersion effects such as trapping effects at surface and substrate. Along different paths, the trapping or detrapping contributes to the small-signal parameters in different way resulting in path-dependence in integration.

There have been tens of analytical nonlinear models for MESFETs and HEMTs and most of them have been incorporated into commercial harmonics-balance softwares, such as LIBRA[4]. We found that many of them, when incorporated into harmonics-balance softwares, the respective charge terms are almost not integrable from respective capacitance and it is often that approximation expressions must be utilized resulting in inconsistency between large-

signal and small-signal models.

We report for first time, an experimentally-based model approach which is capable of simultaneously modeling any nonlinear and dispersive elements, and which solves the problem of path-dependence in integration. The technique proposed is inherently self-consistent for simultaneous fitting of dc, large-signal and small-signal characteristics, because the model is constructed merely from measured S-parameters at various frequency. In this technique, RF-frequency dependencies are approximated by a polynomial development of the integrated currents and charges in terms of frequency which can be readily represented by a phenomeno-logical equivalent circuit constructed via synthesis. Also the path-dependence-caused complications are taken into account by utilizing two models extracted from integration along two-distinct paths and then combined into a single one by signal flow control, as explained below.

APPROACH

F.Filicori el al[4] proved that the instantaneous currents across a nonlinear and dispersive element can be described by superimposing a steady-state dc-related term with a term which is a Fourier-transform from the product of device frequency-dependent Y-parameters and port voltages.

$$i(t)=F_{DC}(v(t))+\sum_{p=-P}^{+P} Y(v(t),\omega_p)V_p e^{j\omega_p t}$$

where F_{DC} is a non-memory current term corresponding to dc IV characteristics. The second term describes the contribution of diviation of RF swing from DC curves. Y represents voltage and frequency dependent admittance. Based on his theory one can obtain by integration the current and charge terms respectively from the in-phase components and quadrant components of Y-parameters and assume that the integration in a 2-d plane is path-independent. The assumption is valid providing the "memory time" for the device is small comparing to the signal period.

It is worthy to point out two observations. First, in general the integrated results, namely the port currents and charges are not frequency independent. Figure 1 and 2 shows respectively, for example, the drain current and gate current at three different frequencies. Secondly, the integration can be path dependent due to long-memory-time effects such as trapping or thermal effects. Figure 3 compares the integrated drain current along a counter-clock-wise path with the one along a clockwise path. Along the counterclockwise path one integrates Gds with respect to Vd for a Vg below pinch-off and then integrates Gm with respect to Vg to the end point. For this path, Gm or Y21 values are most informative. For the clockwise path, integration of Gm is first performed at Vd=0 with respect to Vg and, then integration of Gds with respect to Vd to the specified point. For this path, Gds values are most important. One can see the difference of integrated results. The curves of the first one show more negative slopes at a saturation region and a smaller Idss in overall comparing to second path results.

To model the dispersive behavior, we propose a polynomial development of each current and charge component in terms of frequency by the use of

$$I(V_g,V_d,\omega)=i_{DC}(V_g,V_d)+\omega^2 i_2(V_g,V_d)$$
$$j\omega Q(V_g,V_d,\omega)=j\omega(Q_o(V_g,V_d)-\omega^2 Q_3(V_g,V_d)$$

The nonlinear 2-D coefficients can be obtained by performing regressions at each measuring bias point. In this way we were

able to separate the dispersive effects from the nonlinear dependencies. One may take more higher order terms in development of frequency polynomial series, depending on the accuracy for dispersion required. These nonlinear and dispersive terms were then represented by an equivalent circuit containing three MESFETs in parallel with several linear control currents or voltage sources as shown in figure 4. All MESFETs and linear elements were implemented with a coded senior element in LIBRA[4] to facilitate small-signal and large-signal simulation. The three nonlinear elements, basic FET , dispersive FET, and low-frequency dispersive FET, are designed to accommodate simulations over time scales that differ by orders of magnitude. The control sources and capacitances are used to account for frequency dependencies. The circuit representation for polynomial development was constructed by synthesis technique. The low-frequency MESFET model absorbs the difference between the dc I-V data and that extrapolated from frequency-dependent I-V characteristics to dc. To account for different trapping effects, the time constant of low-frequency dispersive MESFET may be adjusted by varying the capacitance that is connected to it.

Figure 5 shows the idea how to deal with the path-dependence issue. Since the two particular paths are primarily associated with two distinct sets of parameters, one being Gm and Cgs, the other being Gds and Cdg, we can construct an equivalent circuit consisting of two models, one being obtained along a counter-clock-wise path in Vg versus Vd plane to account for forward response or simulating S11 and S21 in small-signal case, the other being extracted along a clockwise path to simulate backward response, or, S22 and S12 for small signal case. At the junction of the input and output ports, virtual one-way controllers are added for signal flowing control.

RESULTS

The MESFET under study is an implanted device directly on a semi-insulating substrate. The dc characteristics, as seen from figure 4, show some kinks at the region of higher gate voltages and after drain current saturation. Negative conductance can also be seen. Peculiar gate current with peaks around zero gate voltage region is also noticed.

The MESFET's S-parameters were taken at 748 bias points to cover the drain voltage from zero to 6 V and gate voltage from -1.3 V below pinch-off to 0.6 V close to gate conduction. Magnitude large than one in S22 was observed in the region of $Vg \geq 0$ and $Vd = 2$ to 4 V which is also shown as negative conductance in dc characteristics, indicating it is RF-negative-conductance.

After integration of the real part and imaginary part of the Y-parameters in the 2-D Vg-Vd plane along two distinct paths at selected frequencies, f=0.7, 1.7, 3.7, 7.7 and 15.7 GHz respectively, we obtained two look-up-table-based models, each having port currents and port charges as function of Vg and Vd. Regression was, then performed at each measurement bias point to obtain the polynomial development of the currents and charges as function of frequency. The coded senior file first reads all the look-up-table regression data and calculate the values of port currents and charges as well as their derivatives with respect to the port voltages by a 4-terms bivariate interpolation.

Figure 6 shows the simulated dc curves verses measured data. They are exactly the same and cover every detail of local nolinearities. Kinks are evident and well-simulated at higher gate voltage and medium drain voltage. Correspondingly, there are reverse gate current peaks around $Vg = 0$ and $Vd \geq 2.5$ V(not shown). Small-

signal response are calculated at a set of bias points. Figure 7 shows the results at Vd=2.75 V and Vg=0.4 V where a negative output conductance appears. Both modeled and measured data show the magnitude of S22 to be larger than 1 indicating negative conductance. The frequency behavior is in good agreement with the measured one. Figure 8 and 9 show respectively the measured and simulated large-signal contours in output and input I-V planes at four input power levels and f=2 GHz. The results also show good agreement in terms of the swing region and waveforms. For higher input-power there was a problem with convergency, probably due to a poor extrapolation beyond the measured region.

CONCLUSIONS

Due to complex nature of MESFETs and HEMTs associated with trapping effects, it becomes extremely difficult to develop an accurate physics-based model or a regular experimentally-based model. The model proposed in this paper may provide a solution. It is inherently consistent between the large-signal and the small-signal modeling. Using a polynomial development, we successfully model an element which is simultaneously dependent on port voltages and frequency. A proposal is also made to bypass the problem of path-dependence in integration of characteristics, caused by low-frequency dispersion. The model uses the concept of signal flow control to model forward and backward small-signal and large-signal response respectively and therefore, provides a robotic way to simulate complex characteristics of real devices. The model can be used to evaluate the effects of MESFET anormalies such as gate- and drain-lags which are critical for wireless communication applications.

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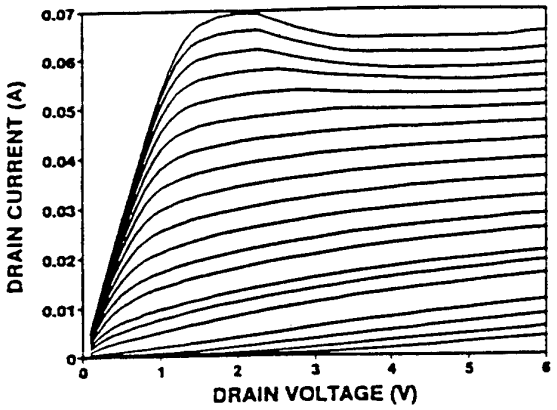

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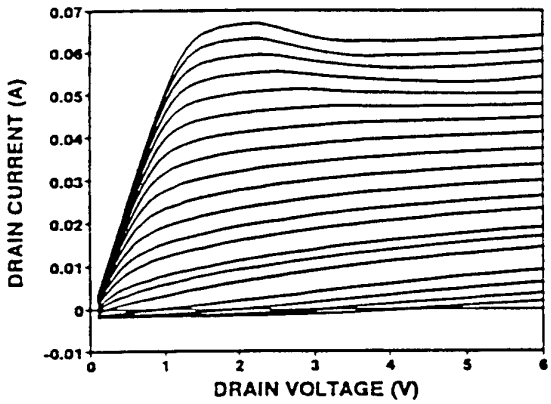

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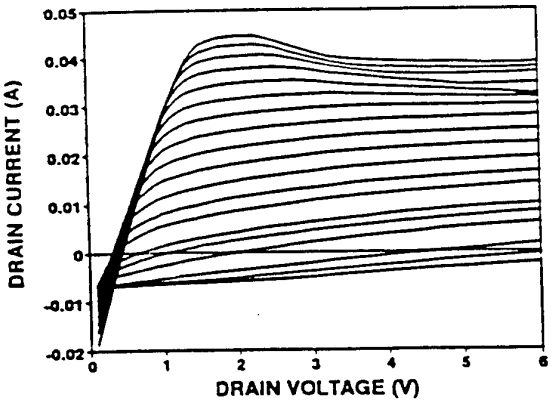
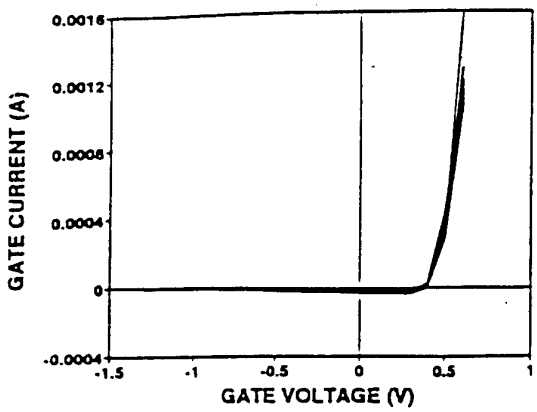


(c)

Figure 1 Integrated drain curves at (a) 0.7, (b) 3.7, *and (c) 15.7 Ghz*.Vg=0.6,0.5,..-1.3 V top down.



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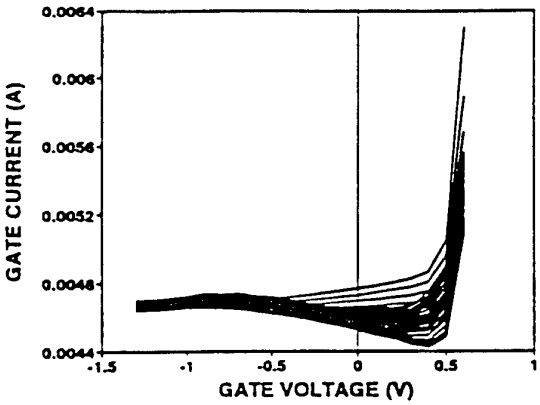

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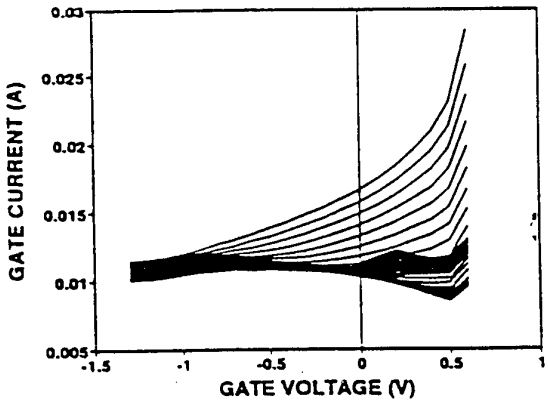

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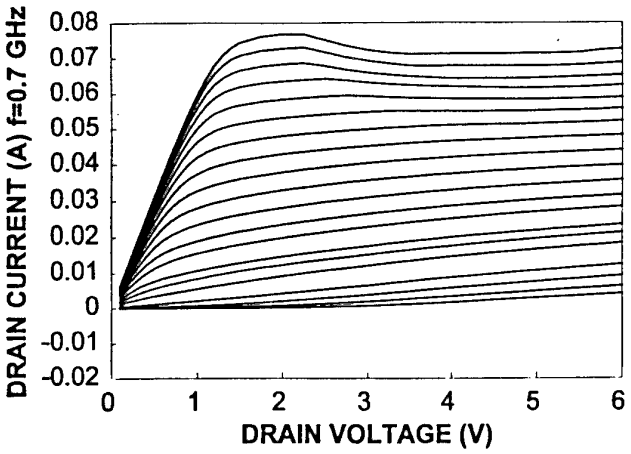
Figure 2 Integrated gate curves at (a) 0.7, (b) 3.7, and (c) *15.7 Ghz. Vd=0,0.1..6 V.*



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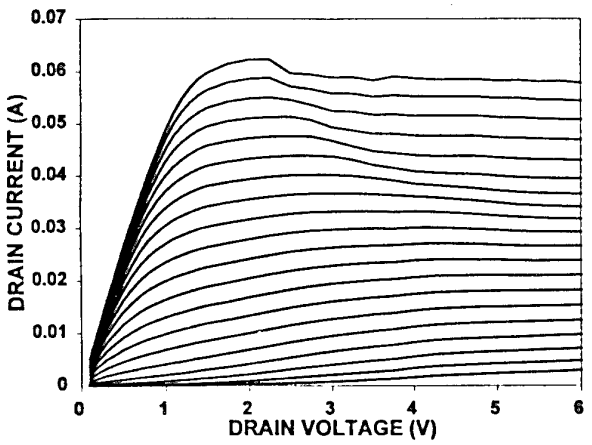


(b)

Figure 3. Integrated RF Id vs Vd curves along clockwise(a) and counter-clockwise path(b) on Vg vs Vd plane. f=0.2 Ghz

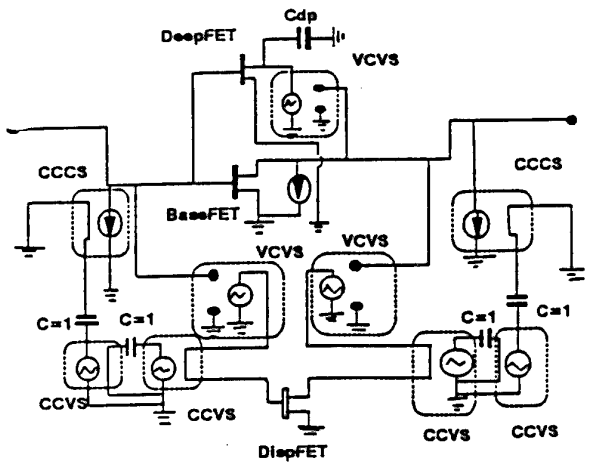


Figure 4. Equivalent cirucit to account for RF-dispersion

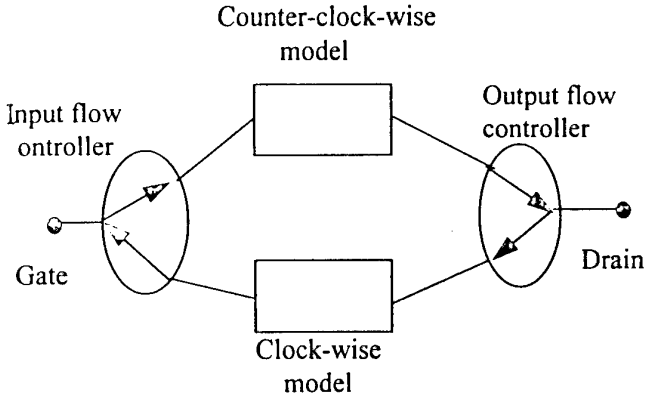


Figure 5. Diagram of the signal-flow control with two models incorporated.

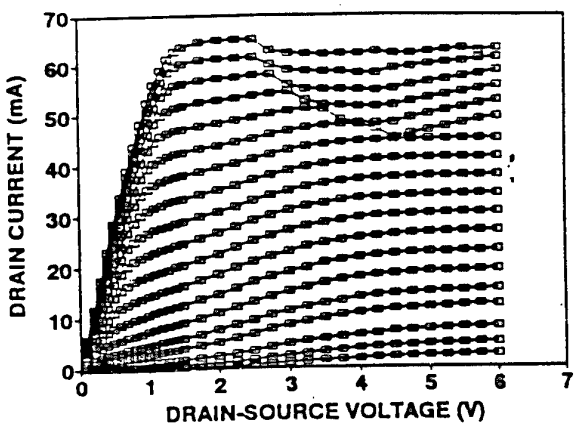
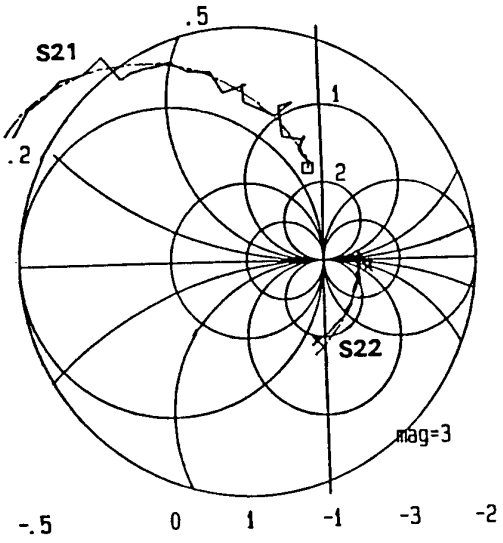


Figure 6. Modeled (line) versus measured (□) dc characteristics.



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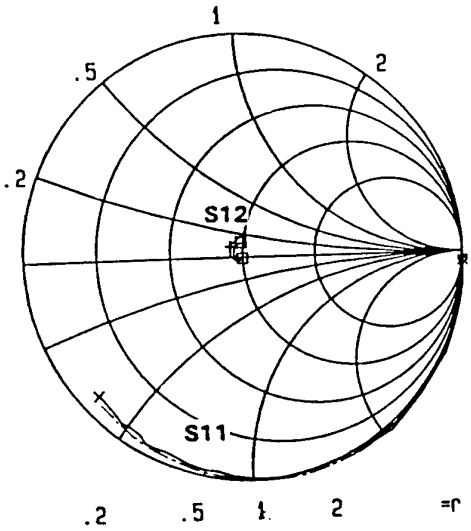
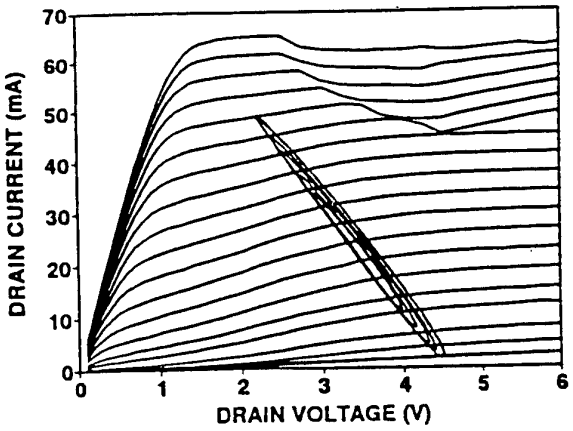


(b)

Figure 7. Modeled vs. measured *S21, S22* (a) and *S11, S12* (b) at Vd=2.75 V Vg=-0.4 V. – Measured, -·- Modeld



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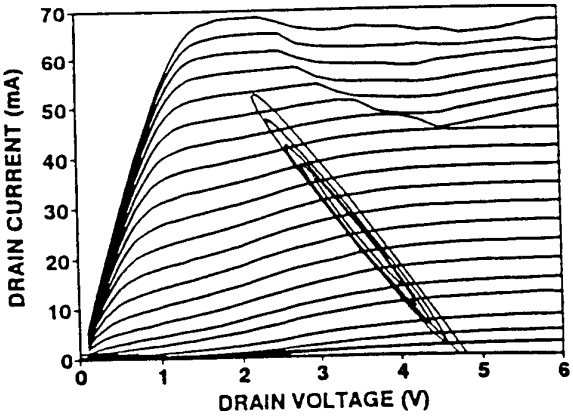

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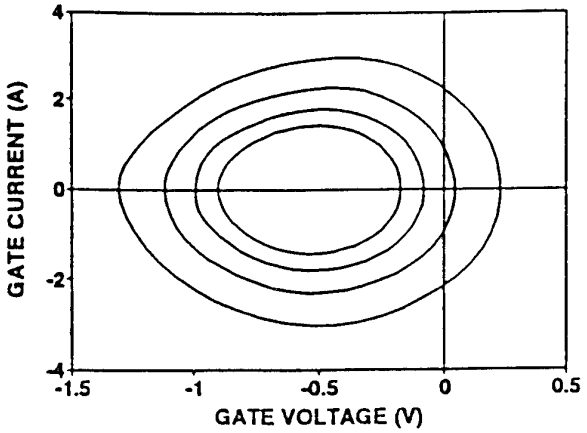
Figure 8. Modeled (a) vs measured (b) Drain contours. *Pin=-2,0,2* and *4* dBm, Vd=3.5 V Vg=-0.5 V.



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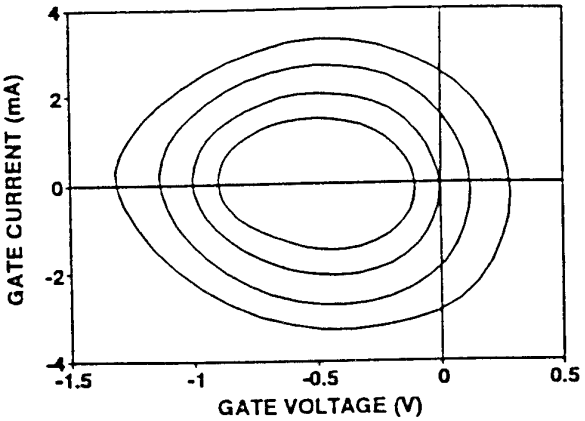

(b)

Figure 9 Modeled (a) vs measured (b) gate contours. *Pin=-2,0,2*,and *4* dBm, Vd=3.5 V, Vg=-0.5 V.

A NEW TECHNOLOGICAL CONCEPT FOR OPTIMUM CIRCUIT DESIGN AT MICROWAVE AND MILLIMETERWAVE FREQUENCIES

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ABSTRACT

Accurate characterization and modeling of microwave active devices is a fundamental requirement for reliable microwave circuit design. A new technological approach based on planar integration of commercial GaAs FETs in chip form in high resistivity silicon substrates is aimed at fully exploiting this requirement. The technology uses airbridge interconnections, permits accurate on-wafer characterization of embedded active devices of any contact pad structure and thereafter the fabrication of the final circuit based on the measured data and using the characterized device. Basics of this new technology, a summary of the technological processes and preliminary results are presented.

I. INTRODUCTION

The availability of low-cost and reproducible microwave and millimeter-wave circuits is of great importance to systems in the future. A promising way to achieve these requirements are integrated circuits based on silicon substrate [2], [10], [13]. Microwave devices such FETs suitable for applications in this frequency range are, however, based on GaAs because of its superior electrical performance. Consequently, GaAs based device technologies, e.g. for MESFETs and HEMTs, are well developed. Commercial HEMT chips covering frequencies beyond 60 GHz are available [9]. Generally, hybrid technologies have therefore been used for many different applications as a good compromise between cost and performance e.g. [1], [3].

In the classical hybrid integration approach, active devices are mounted on top of the substrate and the interconnections are made by bonding wires. Such interconnections are not reproducible and at microwave frequencies exhibit undesirable parasitic inductances which degrade and limit the circuit performance and bandwidth respectively. A technology that circumvents these limitations is Flip Chip bonding [1], [8], [14]. Devices are manufactured with suitable bonding pads leading to very short and reproducible interconnections. However, a large number of microwave devices, either low-noise or low-power do not have bump contacts and must be bonded [3]. Planar interconnect technologies focusing specifically on low-power microwave devices have been reported [5], [6]. The proposed technologies also require very short interconnections which, however, must be carried out in a bonding step.

This paper presents a novel hybrid technology whereby GaAs FET devices

are integrated in a silicon substrate in a planar position and interconnections made by employing air bridge technology as in monolithic circuits. The approach takes advantage of the conventional silicon micromachining technology, thin film technology and, as active devices, commercially available GaAs FETs in chip form. The high resistivity silicon substrate serves as a basis for realizing distributed passive coplanar components. More importantly, the technology allows for re-usability of characterized active devices in final circuits.

II. PLANAR HYBRID TECHNOLOGY

The proposed technology is based on two main steps, namely planar integration of the GaAs FETs in Si substrate and thin film/air bridge interconnections of the embedded chip to the rest of the circuit.

a) Planar Embedding Technique

This is the first and most important technological step. The aim here is to make an opening in a substrate and then glue an active device in it such that a plane surface between the active device and substrate results. This must be attained to guarantee for the successful subsequent processing associated with lithography and metallization.

Two possibilities, wet etching or dry etching, exist for micromachining of silicon. Dry etching with inductively coupled plasma and cryo-temperature of the substrate allows the etching of grooves with vertical sidewalls and etching rates up to 2 to 4 μm/min. (Fig. 1) [12]. Although the cross-sectional dimensions of an opening for a chip can be exactly defined, the etching depth is difficult to control without laser interferometry. Wet etching of silicon (with <100> crystal orientation) results in slanting sidewalls. The resulting gap between a mounted chip and silicon is impossible to planarize [15]. A technique based on wet etching of openings in Si and using a planarization adhesive film was therefore developed.

Fig. 2 shows a summary of the procedure developed for high precision mounting of chips in a substrate. A silicon substrate is etched in KOH solution at the required opening positions. Next, an adhesive film is spanned with care to cover the opening. A chip is then introduced face down into the substrate and positioned on the adhesive film. The gaps between the chip and the substrate are filled out with an epoxy resin or polyimide. After the glue dries up, the adhesive film is pulled away leaving a plane surface. A surface planarity of less than 2 μm has been achieved. A scan of the surface profile across an embedded chip and the surrounding substrate area is shown in fig. 3. A typical low-noise microwave transistor chip has dimensions of the order 350x400x100 μm which calls for very fine handling. Although similar techniques have been proposed for multi-chip modules in general [4], [7], [11], they have not yet been investigated for microwave applications.

b) Interconnection Technology

The interconnections to the embedded active device are realized by using air bridge technology. This technology offers low parasitic interconnect capacitance and low inductance. Furthermore, this technique eliminates uncertainty that may be caused by the small non-planarity of the surface. A cheaper technology based on aluminium rather than standard gold plated bridges has been developed. Fig. 4 depicts a schematic diagram of this air bridge fabrication technique.

First a thick layer of photoresist is spun on the substrate and patterned. After a careful bake of the resist for removing all solvents a 2 μm thick aluminium layer is evaporated under rotating/swaying motion of the substrate for uniform covering of the resist slopes/edges. Then a second

layer of photoresist is spun on and patterned. The extra aluminium is etched away and finally the resist stripped leaving stable air bridges. Fig. 5 shows scanning electron micrographs of test air bridges. The aluminium thickness is 2 μm and the headroom width is 6 μm.

III. RE-USABILITY OF ACCURATELY CHARACTERIZED ACTIVE DEVICES

The new technology offers a unique opportunity to investigate long-standing uncertainties in microwave circuit design. The difficulties in reaching the goal of first pass success designs include tolerances in device parameters and non-reproducible interconnections in hybrid circuits. Efforts to accurately characterize and model single active devices are therefore not fully exploited. This is due to the inability to remove the device from the test fixture and bond it again in the final circuit [15]. As such there is need for more comprehensive validation tools (focusing on the active devices) for microwave design techniques since at the moment discrepancies between simulation and measurement may always be justified. On the other hand, models for passive components (e.g. microstrip) are well-developed and accurate, and the recent availability of 3D simulators makes it possible to also accurately model complex passive structures.

An important step in validating the various strategies involved in the design of microwave circuits is therefore the fabrication of a circuit incorporating a previously characterized active device. This strategy eliminates tolerances associated with device parameters, such as in the design of frequency doublers where small changes in the pinch-off voltage can adversely affect circuit performance. Or in microwave oscillator design, small changes in the bondwire inductance (length) lead to significant shifts in the frequency of oscillation [6]. Secondly, by employing air-bridge technology for interconnections, uncertainties associated with the usual bondwire interconnections are also eliminated. This strategy can therefore eventually lead to establishing reliable models and design techniques, i.e. a validation tool for microwave circuit design.

On the basis of the proposed technology, a coplanar micro-test-fixture for active devices having any contact/bond pad structure was proposed [15]. This fixture allows, in principle, the re-usability of accurately characterized active devices in final circuits. Three technological processes are currently under investigation to optimize re-usability of characterized and modeled devices. The first method is based on direct writing using e-beam lithography. The active device is first of all characterized and after the final circuit is designed, the Si wafer with the embedded chip is spun with photoresist and the passive structures (distributed coplanar components) are then written with e-beam lithography. The second method is similar to the first one but uses conventional lithography whereby contact between the wafer and mask is avoided. Problems associated with poor coverage of resist around the airbridge interconnections have to be solved for both methods. A more promising method is to use aluminium air-bridge interconnections. Since the active devices have gold contact pads, by using gold for the first metallization layer for the passive components, the aluminium air-bridges required for the micro-test-fixture can be selectively etched away after transistor characterization. The distributed passive components can then be realized using conventional contact lithography before air-bridge interconnections to the active device and at the coplanar discontinuities are

fabricated. Fig. 5 shows a GaAs MESFET (MGFC 1402 from Mitsubishi) embedded in a Si substrate with air-bridge interconnections.

IV. CONCLUSIONS

A low-cost planar hybrid technology (quasi-monolithic technology) for microwave circuits has been described. GaAs FET devices have been integrated in a quasi-monolithic manner in silicon substrates. Planar, very short and reproducible interconnections complete the simple assembly with excellent microwave performances at low-cost. The technology presents a unique opportunity to track down on problems associated with device and interconnection tolerances that currently plague microwave circuit design.

V. REFERENCES

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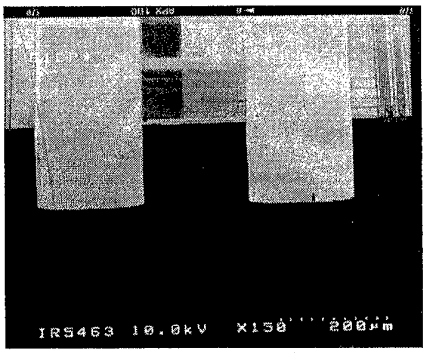

Fig. 1: Cross-section of grooves etched with SF_6/O_2 plasma at a substrate temperature of -100°C.

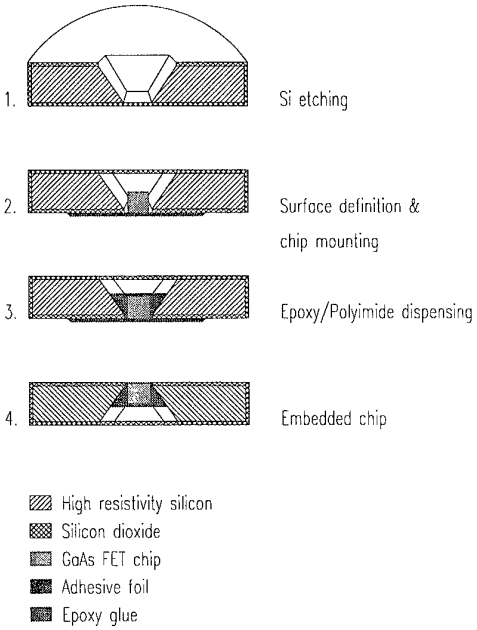

Fig. 2: Procedure for high precision integration of GaAs FETs in Si substrate.

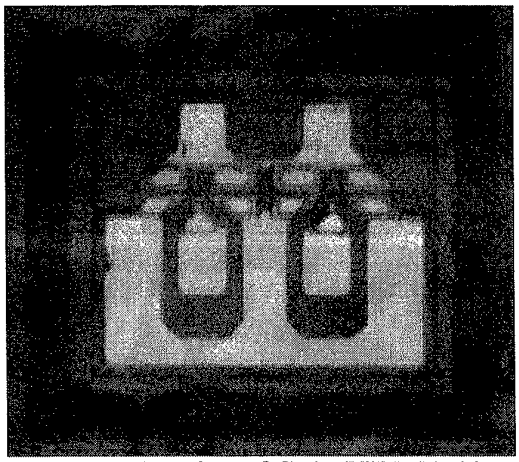

Fig. 3: (a) Top view of GaAs PHEMT chip mounted in a Si Substrate.

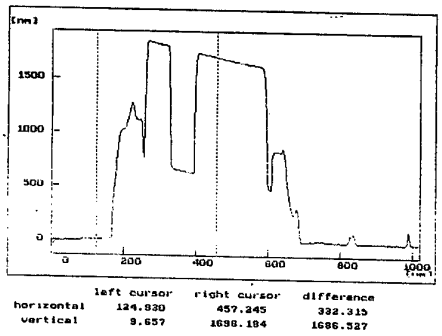

Fig. 3: (b) Profilometer scan of the chip in (a)

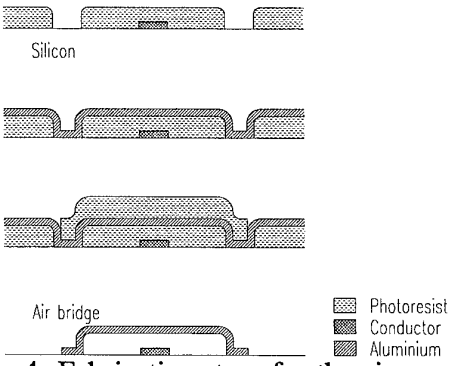

Fig.4: Fabrication steps for the air bridges.

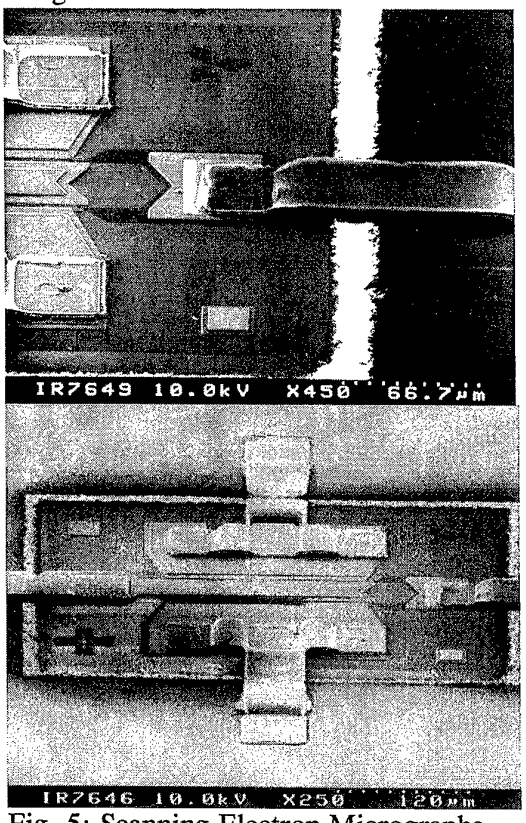

Fig. 5: Scanning Electron Micrographs (SEM) of air bridge interconnections between a GaAs FET (Mitsubishi MGFC 1402) and coplanar pads on silicon.

A new method for large signal FET simulation used in MMIC frequency multipliers

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ABSTRACT

This paper describes a new method for nonlinear transistor modeling. Starting from the usual small signal equivalent circuit of a FET a large signal equivalent circuit has been developed. The method has been implemented into a spline based FET model for HP-EEsofs "Libra" and verified by utilizing linear and nonlinear measurements. The accuracy of the model has been tested in a monolithic integrated frequency multiplier design. This strongly nonlinear circuit converts a 5 GHz input signal up to 25 GHz. Measurements and simulated results show excellent agreement.

THE NEW LARGE SIGNAL EQUIVALENT CIRCUIT

In many FET models there are two problems: One can not fit a DC output characteristics as well as the intrinsic Gds for high frequencies simultaneously [1] and second determining a charge of a capacitance which depends on two bias voltages by a partial integration introduces transcapacitances to the small signal equivalent circuit [1,2]. This is due to preserve the consistence between small and large signal equivalent circuit. Both problems are solved with our new model, which is based on the well known 15 element equivalent circuitry [3,4]. For a harmonic balance simulation the charge of each nonlinear capacitance has to be calculated as:

$$Q_1(v_1) = \int_0^V C(\tilde{v}_1)\,d\tilde{v}_1 \quad . \qquad (1)$$

However, the charge of a capacitance depending on two voltages is a function of the integration path:

$$Q_2(v_1, v_2) = \iint_{V_1,V_2} C(\tilde{v}_1, \tilde{v}_2)\,d\tilde{v}_1 d\tilde{v}_2 \,. \qquad (2)$$

Therefore, a significant discrepancy between small and large signal simulation for low input power can often be noticed. For low input power, the large signal model must turn into the small signal model [2,5]. In our new model the capacitances have been transformed into their equivalent current sources:

$$i = \frac{\partial Q_2(v_1, v_2)}{\partial t} = C'(v_1, v_2) \cdot \frac{\partial v_1}{\partial t} \,. \qquad (3)$$

Since there is no DC current through a capacitance, C' is called a parametric capacitance. It can be shown, that $C'(v_1,v_2)$ is nearly identical to the small signal capacitance $C(V_1,V_2)$ [6].

Fig. 1 shows the agreement between the small signal and large signal model for small (-30dBm) input powers for the scattering parameter s_{21} of the simulated FET device. All other S-parameters and all phases are in perfect agreement, too. The resulting large signal equivalent circuit is shown in fig. 2.

The first step of extracting the model's elements is to measure S-parameters and the DC I-V curves. After determining the FETs extrinsic elements the intrinsic elements are calculated in the usual way [3,4],

except that the bias dependence of V_{gs} and V_{ds} is introduced. Then the intrinsic conductance G is calculated by optimizing the S-matrix of the intrinsic FET. The following optimization of the three intrinsic capacitances and the conductance G does not have any influence on the static model's quality, because of the capacitance C. The following steps are a deembedding of the voltages and calculating the splines before saving the "Libra" simulation file.

MEASUREMENT VS. SIMULATION

The model has been verified on various MESFETs and HEMTs. To demonstrate the models applicability to a 6 finger 20µm unit gatewidth HEMT (T6x20), the simulation of I-V curves and small signal S-parameter, as well as a simulation of a frequency times 5 multiplier are compared to measurements (fig. 3,4,8,9). In addition, an error grid, containing the frequency-average complex difference between small signal S-parameter measurement and simulation for each bias point, is given in fig. 5.

APPLICATION EXAMPLE: A FREQUENCY TIMES 5 MULTIPLIER

A frequency times five multiplier was analyzed using the proposed model. The realized MMIC in coplanar line technique shows a conversion loss of about 7 dB in the input frequency range of 4.7 GHz to 5.3 GHz utilizing a two stage design with 0.25 µm HEMT technology. The first stage provides the frequency conversion by making use of the nonlinearity of a transistor driven into saturation. To accomplish this, an available input power of 5 to 10 dBm was necessary for obtaining a satisfying conversion performance. The transistors gate bias point was chosen to be 0 V and the drain bias was 3 V. The second stage, with the same bias condition, serves as a buffer amplifier and matching network. While Fig. 6 shows the simplified circuit representation of the multiplier, fig. 7 depicts a chip photography of the MMIC. The fabricated MMIC was evaluated using on wafer measurements of small signal s-parameters and nonlinear power measurements. In fig. 8 the 5th harmonic output power of the input signals between 4.7 GHz and 5.3 GHz are presented. There is a very good agreement between simulation and measurement especially at higher input levels.
Also the 3rd harmonic output frequency is modelled with excellent agreement as can be seen from fig. 9.

SUMMARY

A new method for nonlinear transistor modeling has been proposed. It has several advantages compared to other methods:

- small and large signal simulation results are identical for small input power,
- very good agreement between simulation and measurement for small signal, large signal and static simulation,
- validity for all bias points,
- complete extraction and simulation within a very short time.

The validity of the proposed model was proven by means of a MMIC frequency times five multiplier. Measured results are in excellent agreement with simulated data.

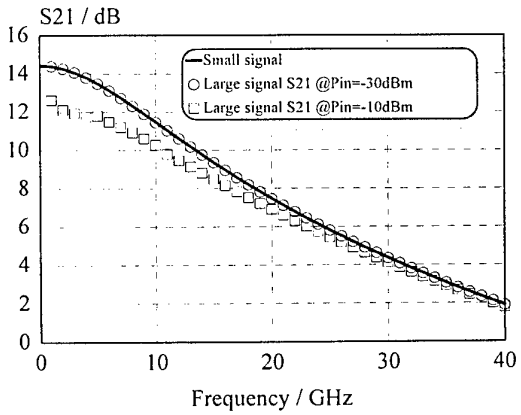
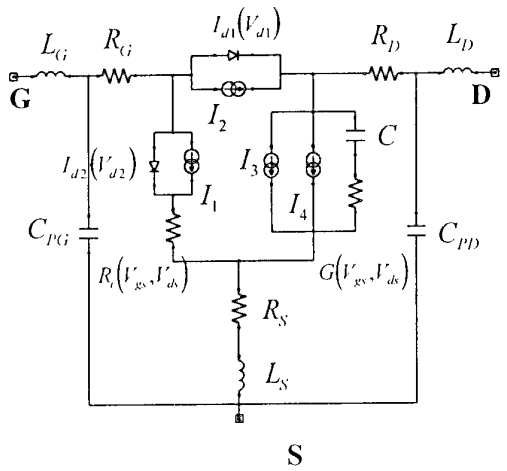


Fig. 1: Comparison between small signal and large signal model.



where

$$I_1 = C_{gs}\left(V_{gs},V_{ds}\right)\cdot \dot{v}_{gs}$$

$$I_2 = C_{gd}\left(V_{gs},V_{ds}\right)\cdot \dot{v}_{gd}$$

$$I_3 = C_{ds}\left(V_{gs},V_{ds}\right)\cdot \dot{v}_{ds}$$

$$I_4 = I_{ds}\left(V_{gs},V_{ds}\right)$$

Fig. 2: The new large signal equivalent circuit.

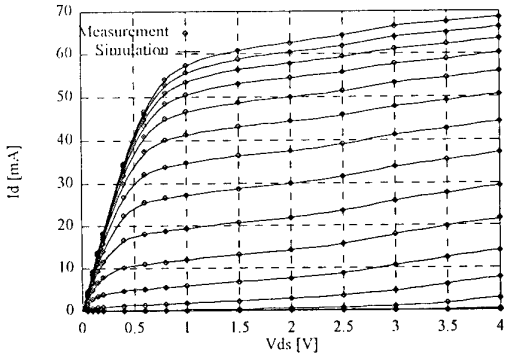


Fig. 3: Forward IV-curves simulation vs. measurement for V_{gs}=-0.8V..0.8V.

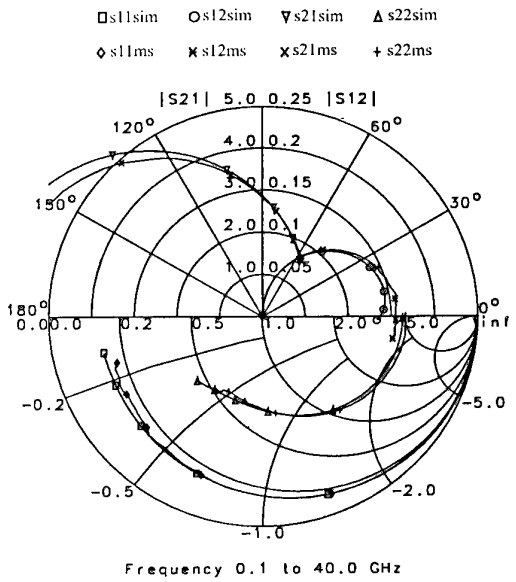


Fig. 4: U_{gs}=0V, U_{ds}=3V, error=0.04 (see fig. 8), without optimization.

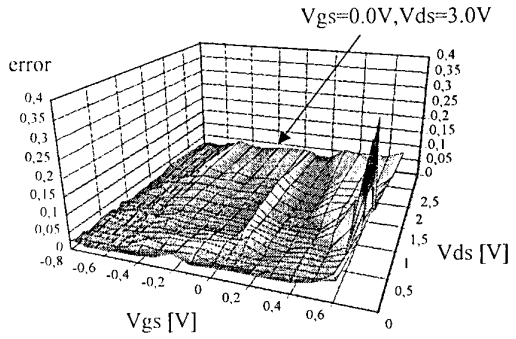


Fig. 5: Error grid for small signal simulation vs. measurement.

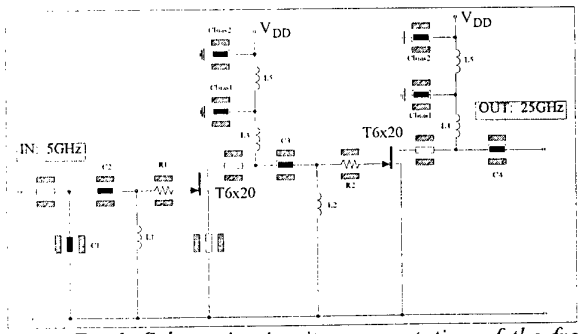


Fig.6: Schematic circuit representation of the frequency multiplier.

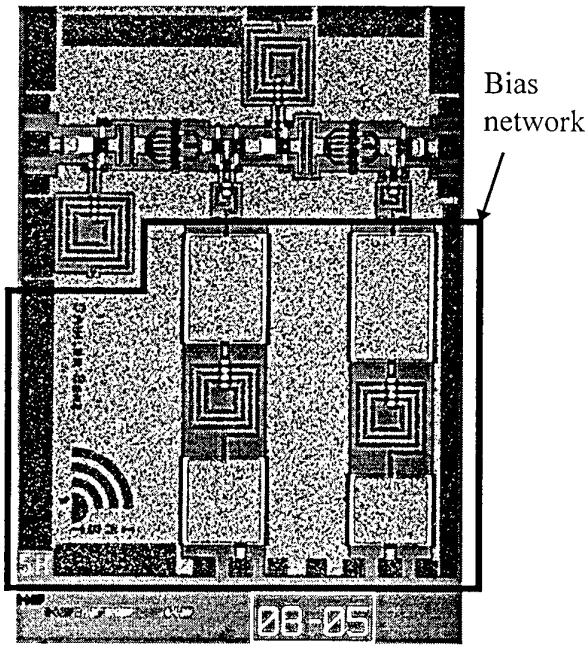


Fig.7: Chip photography of the realized multiplier.

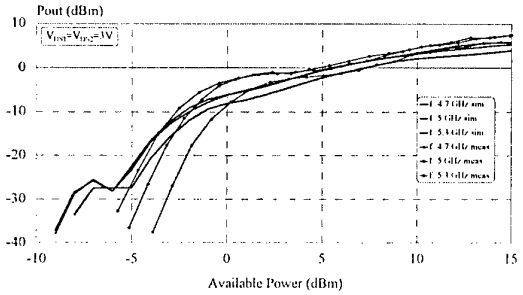


Fig. 8: Measured and simulated output power of the 5th harmonic frequency vs. input power. Fundamental input frequency varies between 4.7 GHz and 5.3 GHz.

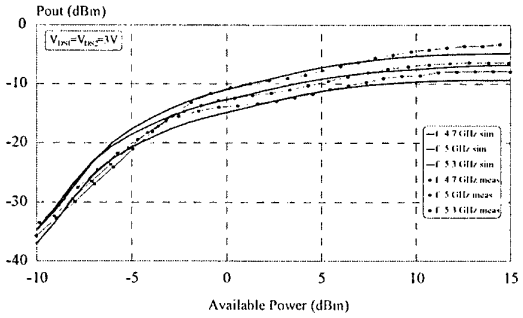


Fig. 9: Measured and simulated output power of the 3rd harmonic frequency vs. input power. Fundamental input frequency varies between 4.7 GHz and 5.3 GHz

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Design of Low Phase Noise MMIC PHEMT based VCO

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Abstract

Low frequency noise in Pseudomorphic HEMTs has been investigated under different bias conditions and bias dependent LF noise model is derived. A monolithic varactor tunable oscillator was designed and experimental phase noise results are reported. The lowest measured phase noise at frequency carrier 24.4GHz was -89dBc/Hz @ 100KHz. The impact of LF noise on phase noise due to the upconversion process is investigated using the pushing analysis and HB simulations.

I. Introduction

Many applications in the frequency range above 20GHz such as radars and communication systems or sensors, require low phase noise mm-wave sources. This noise is primarily due to the up-conversion of the low frequency noise in the active devices (commonly referred to as 1/f noise) to the operating frequency. HBTs with their low LF noise have shown best phase noise performance in microwave oscillators. However, low phase noise can be achieved in the PHEMT oscillator due to its low up-conversion factor [1]. Moreover, the high cutoff frequency f_T of PHEMTs makes them the active devices of choice in many millimeterwave applications.

In order to provide more predictable phase noise performance, it is necessary to have an accurate bias dependent LF noise model. As result, the LF noise of PHEMTs was measured and bias dependent behaviour is modeled using a current controlled noise current source at the drain terminal.

In the second step, a fully monolothic PHEMT VCO was designed using an appropriate nonlinear approach based on the optimisation of the intrinsic load cycles [2]. The evaluation of the phase noise, referred to as modulation noise [3], which is analyzed in terms of LF noise multiplied by the oscillator pushing factor provides a satisfactorily agreement with measurements. Best phase noise data of -89dBc/Hz @ 100KHz at carrier frequency 24.4 GHz was obtained.

II. Low Frequency Noise Characterization and Modeling

Baseband noise measurements on Pseudomorphic HEMT device featuring 4x30µm gate width and 0.2µm gate length have been carried out from 10Hz to 100KHz to determine the bias dependent low frequency noise spectra.

The measured low frequency noise associated to the drain current shows fundamental $f^{-\alpha}$ noise with α=1.1 and two generation-recombinition (g-r) noise components. Each g-r noise process (Lorentzian spectrum) is related to a particular trap or defect characterized by a discret energy level E_a and a time constant τ.

Further investigations of low noise spectra at different temperatures will provide useful informations to the identification and understanding of g-r noise foreboded at room temperature[4].

The bias dependence of the LF noise characteristics was measured. The devices were biased at different gate-source (Vgs) and drain-source (Vds) voltages for this purpose. The drain-source voltages were selected to cover the saturation regime from 1V to 2V.

The analytical description of LF noise behaviour versus bias conditions is given by the following expression :

$$S_i(f) = \frac{\beta I_{ds}^{\gamma} + \mu}{f^{\alpha}} + \sum_{i=1}^{2} \frac{\left(\beta_i I_{ds}^{\gamma_i} + \mu_i\right)\left(fo_i I_{ds}^{Xo_i}\right)^{-1}}{1 + \left(\frac{f}{fo_i I_{ds}^{Xo_i}}\right)^2}$$

where I_{ds} is the drain-source current.

We have reported in figure -1-, the frequency evolution of the output current noise versus bias conditions. We can notice a good agreement between measured and calculated noise.

In order to analyze the impact of the LF noise properties on the phase noise of microwave oscillator, we have realized a K-band monolithic varactor tunable oscillator (VCO) based on PHEMT transistor and oscillator phase noise measurements have been carried out.

III. Design and fabrication of VCO

The voltage controlled oscillator using 0.2x120 μm^2 PHEMT is designed under series feedback topology (fig. 2). A tuning varactor diode in series with an inductor L_g at the gate terminal for realizing wideband VCOs, and a source capacitance C_s are the feedback elements featuring a negative resistance at the drain terminal over the desired oscillation frequency range. The values of L_g and C_s were optimized in order to get a near ideal load cycles form over the tuning voltage (fig. 3), and consequently reduce the upconversion noise mechanisms due to the nonlinearities of the transistor. The optimum load cycle should have a minimum area (minimum reactive power), non distorted, and featuring the largest Ids and Vds swings.

The oscillator circuit is designed using the PML large signal models of HEMTs and varactor diodes, and simulated with the commercial microwave software HP-MDS.

The circuit is fabricated using 0.2µm gate length Pseudomorphic HEMT GaAlAs/GaInAs/GaAs technology from Philips Microwave Limeil Foundry. The unit current gain frequency (f_t) is 62 GHz, and the minimum noise figure is 0.9 dB at 12 GHz with an associated gain of 11.5 dB. The technology further includes via-holes, epitaxial resistors and MIM capacitors. The substrate height is 100µm.

Fig. 4 shows a circuit layout. The chip size is 1.5 mm by 2 mm.

IV. Performance of VCO

The RF performances were measured in a low insertion loss microstrip test fixture. The monolithic circuit exhibits a tuning bandwidth of more than 3 GHz (22.4-25.8 GHz) with a high sensitivity of 4.5 GHz/V (fig. 5). The measured output power is about 6 dBm.

The VCO characteristics and performance data are resumed in table 1.

To investigate the oscillator phase noise performances, the single sideband frequency modulation noise, normalized to 1 Hz bandwidth, was measured with a test set based on the concept of down-converting the phase noise using a clean reference source (phase detector method).

The measured phase noise £(f_m) from 1 Hz to 100 KHz is less than -80 dBc/Hz @ 100 KHz over frequency range. As example, the fig. 6 shows a phase noise £(100K) of -89 at carrier frequency of 24.4 GHz. The slope of the measured £(f_m) curve is about -30 dB/decade. The results show that, in our measurement range, the phase noise is due to the dominate upconversion process of LF noise.

Fig. 8 shows a comparison of phase noise performance of some VCOs, including the present one, at 100KHz carrier offset, over 14 to 37 GHz [5-11].

The value of -89 dBc/Hz @ 100KHz at 24.4GHz is the lowest phase noise level reported for K-band VCOs.

V. Phase Noise Modeling

An evaluation of the LF noise contribution to the oscillator phase noise is provided from the pushing analysis which is based on the Kurokawa approach[12] extended to include LF noise[13]. The phase noise £(f_m) model is given by :

$$£(f_m) = \frac{1}{2}\left[\frac{e_n(f_m)}{f_m}\left(\frac{\partial f_0}{\partial V_{gs}}\right)\right]^2$$

where $\partial f_o/\partial V_{gs}$ is the sensitivity of the carrier frequency with respect to the gate bias (pushing factor); $e_n(f_m)$ is the input noise voltage source featuring a spectral density $S_v(f_m) = S_i(f_m)/g_m^2$ where $S_i(f_m)$ is the drain noise current spectra and g_m is the transconductance at baseband frequency f_m.

The LF gate current noise source contribution is negligible. Basically at 10 KHz, this noise has

usually been observed to be less than $Si_g(f)=10^{-24}$ A^2/Hz [14-15].
In fig. 7, we have reported the calculated phase noise using the measured gate pushing factor at oscillation frequency of 24.4 and 25.2 GHz. The calculated data results in £(100KHz)= -86 and -82 dBc/Hz respectively compared to the measured £(100KHz)=-89 and -83 dBc/Hz. Also, we calculated phase noise level of -82 dBc/Hz @ 100kHz at carrier frequencies 22.4 and measured -80 dBc/Hz.
We can notice that the calculated phase noise using a pushing type analysis provides a satisfactorily agreement with the measured results at different transistor bias operating points and different varactor voltage.
Nevertheless, some discrepencies occur between simulated and measured phase noise. A possible explanation is rely on the self-biasing of the FET under nonlinear oscillation.

VI. Conclusion

Low phase noise K-band monolithic VCO, using PHEMT technology, has been realized. The design approach is based on the nonlinear optimisation procedure. Best £(f_m) obtained was -89 dBc/Hz at a 100 KHz offset. For the simulation purposes, to accuratly evaluate the phase noise, a bias dependent LF noise model is required.

Acknowledgement

The authors would like to thank B. BYZERY, R. LEBLANC, and P. TALBOT from Philips Microwave Limeil, FRANCE, for their contribution to MMIC circuit realizations, Dr. G. POST, from cnet-bagneux, for low frequency noise PHEMT characterizations, Pr. GROSLAMBERT, from LPMO-Besençon, for phase noise measurements and ENSEA microwave team for their support.

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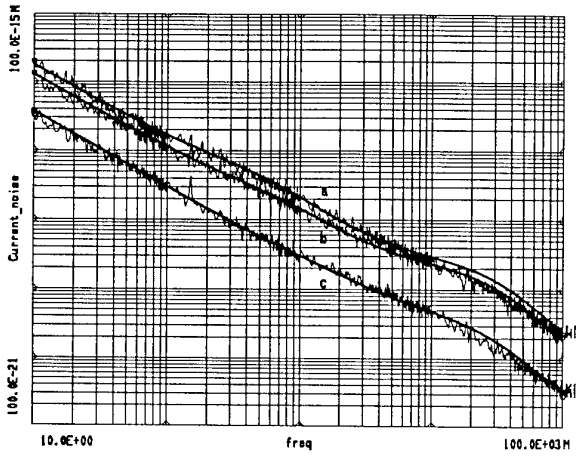


Fig. 1: measured and modeled LF noise under different Vgs bias conditions (Vds=2V) a) Ids=18mA b) Ids=10mA c)Ids=1.8mA

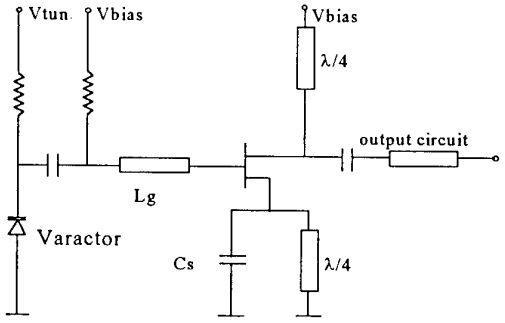


Fig. 2 : schematic of VCO

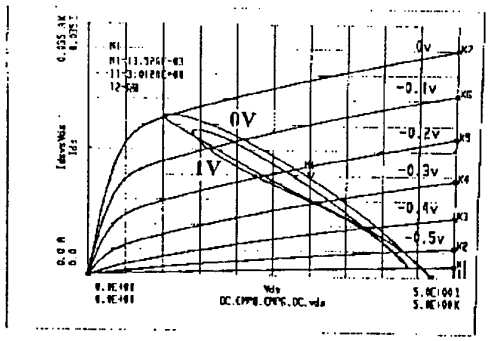


Fig. 3: Load cycles form with two values of V_c at Idss/2

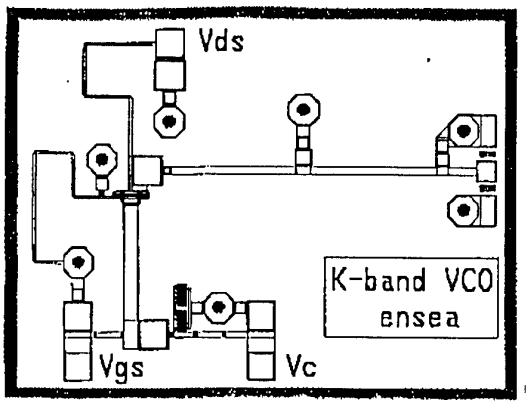


Fig. 4: Layout of the monolithic circuit (chip size: 2*1.5 mm^2)

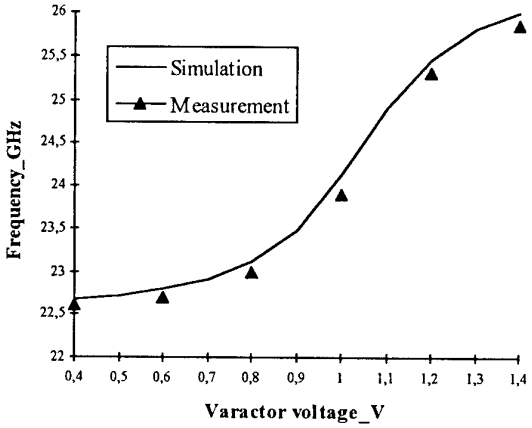


Fig.5 : Oscillation frequency vs. control voltage

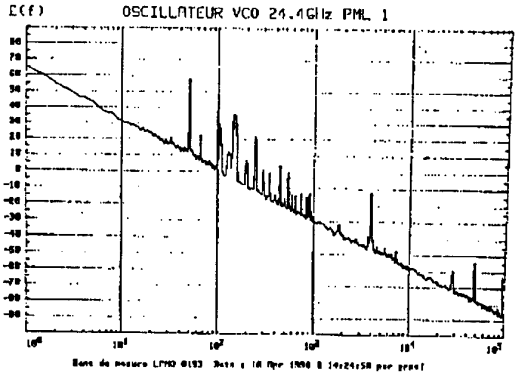
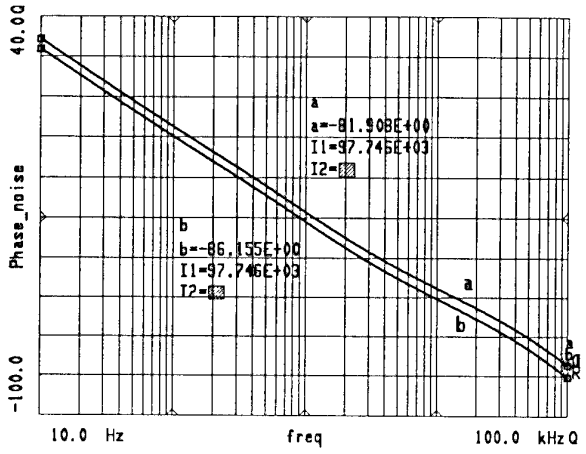


Fig. 6: Phase Noise (-89dBc/Hz @ 100KHz)



Performance	Unity	Value
Output power	dBm	6
Tuning bandwidth	Ghz - (%)	3.4 - (14)
Tuning sensitivity	GHz/V	4.5
Lowest phase noise @ 100 KHz	dBc/Hz	-89
dc power consumption	mW	54
Efficiency	%	7.5
Freq. pushing drain bias	MHz/V	153
Power pushing drain bias	mW/V	1.87
Freq. pushing gate bias	MHz/V	300

Tab.1 : Performance of VCO.

Fig. 7 : calculated £(f_m) at : a) 25.2GHz b) 24.4GHz

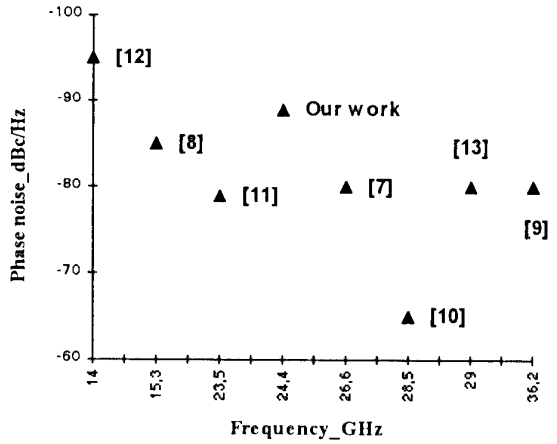


Fig. 8: some relevant published oscillators phase noise data at 100KHz off carrier

Large-Signal HEMT Model for Resistive Mixer Design

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Abstract

A simplified large-signal HEMT model for the design of resistive mixers in the millimeter wave frequency range is presented. The modelled gate charge depends on the gate voltage only. A second model with the gate charge depending on gate and drain voltages is used for comparison. It is shown that the charge conserving simplified model is completely sufficient to describe the conversion gain of a resistive mixer as a function of input power, bias level and compression. The simulated results are compared with measurements demonstrating 11.5 dB conversion loss of a 76-77 GHz resistive HEMT mixer MMIC for an automotive collision avoidance radar.

Introduction

Schottky diode mixers are commonly used in current microwave systems. They have relatively poor inter-modulation and spurious response properties due to their strong nonlinear characteristic and require high local oscillator power. There is an increasing use of HEMTs in modern MMIC mixer designs. The advantages in comparison with diode mixers are manifold and depend on the configuration. HEMTs can be used as mixing elements in the active or passive mode both requiring less local oscillator power than diode mixers. The active gate mixer [1] can have conversion gain. The resistive mixer [2] has the advantages of lower noise figure, better intermodulation properties and low DC power consumption.

The design of HEMT mixers requires accurate large-signal FET models for the transition between pinch-off and saturation (active mixer) or the ohmic region (resistive mixer). Most HEMT mixer designs [1, 3, 4, 5] are based on well known large-signal FET models for example [6] which were mainly developed for the operation in the saturation region. They can not accurately model the HEMT in the ohmic region. An alternative approach is to simplify the large-signal model for a resistive mixer application and to neglect the drain voltage dependence of the nonlinear elements [7]. A single balanced resistive mixer was selected to be a promising component in a chip set for an automotive collision avoidance radar at 76-77 GHz due to its noise characteristic and low local oscillator power consumption.

HEMT large-signal model for resistive mixer design

The resistive mixer MMIC was designed for the Siemens HEMT 110 process. The gate of the delta-doped DH-PHEMT is manufactured using optical projection lithography and sidewall spacer process (gate length $l_G \approx 130$ nm) offering much higher throughput compared to e-beam lithography. Typical DC and RF data are an extrinsic transconductance of 700 mS/mm, a full channel current close to 600 mA/mm and a current gain cutoff frequency of about f_T=110 GHz and a power gain cutoff frequency f_{max} of approximately 210 GHz.

The drain current generator of the model has to describe precisely the measured current in the ohmic region also for slightly negative drain voltages. Additionally the resulting output conductance of the modelled DC characteristic should match the output channel conductance extracted from measured S-parameters. An analytical function for the drain current generator

$$I_{ds}(V_{gs}, V_{ds}) = I_{pk}(1+\tanh(\Psi))(1+\lambda V_{ds})\tanh(\alpha V_{ds}),$$
$$\Psi = P_1(V_{gs}-V_{pk}) + P_2(V_{gs}-V_{pk})^2 + \ldots + P_5(V_{gs}-V_{pk})^5,$$
$$V_{pk} = V_p + \gamma V_{ds} \qquad (1)$$

published in [8] is used to model the DC characteristic. Figure 1 shows the measured and simulated DC characteristic of a Siemens HEMT 110 with 2x40 µm gate width for drain voltages in the range from -0.1 V to 1 V.

The parasitic resistances of the network analyzer test set are a part of the measurement and not deembedded in figure 1. The agreement between measurement and simulation of the DC drain current generator characteristic is excellent in the ohmic region and the extrapolation for slightly negative drain voltages is reasonable.

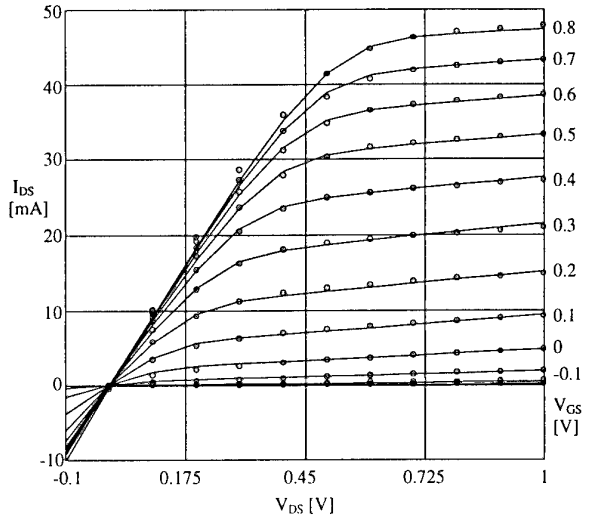

Fig. 1: Measured (o) and simulated (—) DC characteristic of the drain current generator

The conversion loss of a resistive mixer depends on the ratio of maximum and minimum output conductance. The HEMT 110 output channel conductance extracted from measured S-parameters and calculated from the drain current generator equation (1) for V_{ds}=0 V are depicted in figure 2. There is no significant frequency dispersion of the output channel conductance for V_{ds}=0 V.

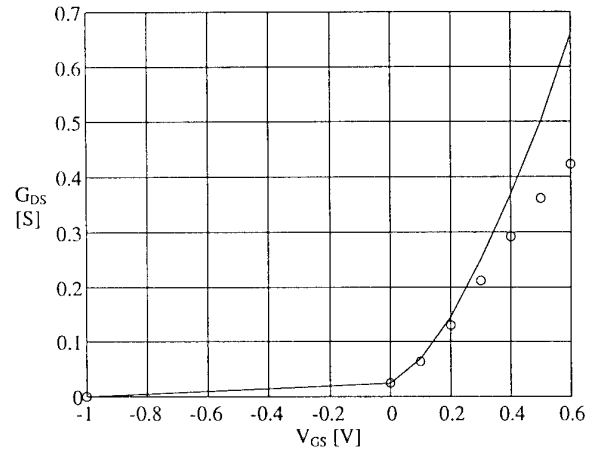

Fig. 2: Output channel conductance extracted from S-parameters (—) and calculated (o) for V_{ds}=0 V

The gate-source bias voltage and local oscillator power of a HEMT resistive mixer are usually adjusted in a way that the gate diode is not conducting. Nevertheless the diode characteristic is implemented in the HEMT large-signal model to avoid possible unreliable simulation results. The measured and simulated DC characteristic of the gate current using a Schottky diode model is depicted in figure 3.

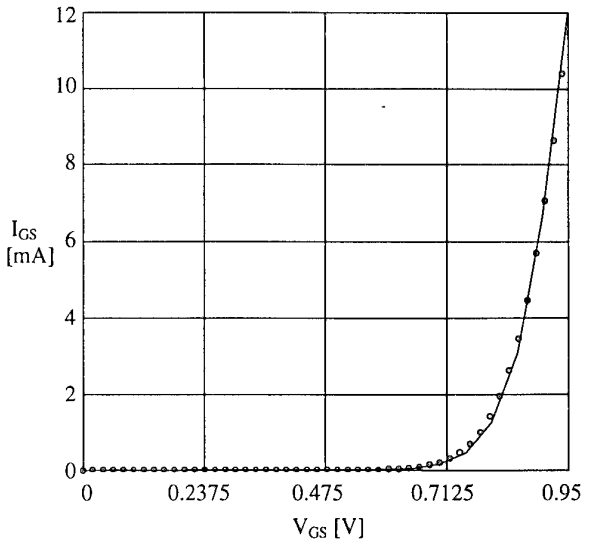

Fig. 3: Measured and simulated gate current for V_{ds}=0 V

The C_{gs} and C_{gd} capacitor characteristics are modelled using two different methods both preserving charge conservation. The first capacitor model neglects the drain voltage dependence of C_{gs} and C_{gd}. This is valid for resistive mixer design because the gate voltage dependence of the capacitors is more important than the drain voltage dependence (V_{ds}≈0 V) in this specific application. The capacitor characteristics are modelled by the tanh-functions:

$$C_{gs}(V_{gs}) = Q_{g0} + Q_{g1}\left[1 + \tanh\left\{Q_{g2}\left(V_{gs} - V_0\right)\right\}\right] \qquad (2)$$

$$C_{gd}(V_{gs}) = Q_{g0} + Q_{g3}\left[1 - \tanh\left\{Q_{g4}\left(-V_{gs} + V_0\right)\right\}\right] \qquad (3)$$

The C_{gs} and C_{gd} characteristics extracted from measured S-parameters for V_{ds}=0 V and modelled using equations (2) and (3) are depicted in figure 4.

The parameters of the C_{gs}- and C_{gd}-functions are different since they rely on the capacitance values extracted from S-parameters.

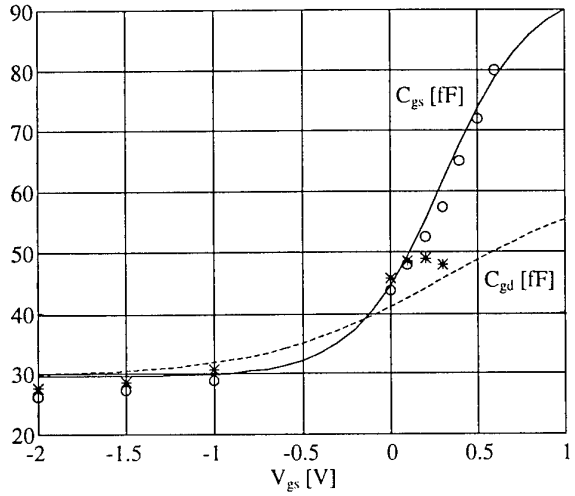

Fig. 4: C_{gs} (o) and C_{gd} (*) extracted from S-parameters and modelled for V_{ds}=0 V

The total gate charge consists of the two charges

$$Q_{gs}(V_{gs}) = Q_{g0}\left(V_{gs} - V_0\right) + Q_{g1}\left[\left(V_{gs} - V_0\right) + \frac{1}{Q_{g2}} \ln\left\{\cosh\left(Q_{g2}\left(V_{gs} - V_0\right)\right)\right\}\right] \quad (4)$$

$$Q_{gd}(V_{gs}) = Q_{g0}\left(-V_{gs} + V_0\right) + Q_{g3}\left[\left(-V_{gs} + V_0\right) - \frac{1}{Q_{g4}} \ln\left\{\cosh\left(Q_{g4}\left(-V_{gs} + V_0\right)\right)\right\}\right] \quad (5)$$

which result from the integration of C_{gs} and C_{gd} with respect to V_{gs}. The parameter Q_{g0} is the common basic capacitance of C_{gs} and C_{gd}. Q_{g1} and Q_{g3} determine the capacitances for high positive values of V_{gs}. Q_{g2} (Q_{g4}) is the parameter for the slope of C_{gs} (C_{gd}) at V_{gs}=V_0. V_0 is the turning point of the tanh function. The charge equations and the drain current function have been implemented in the Hewlett Packard Microwave Design System using a three port symbolic defined device.

The second capacitor model for C_{gs} and C_{gd} was published in [9]. It is based on the assumption that the gate charge can be modelled using the equation:

$$Q_g(V_{gs}, V_{ds}) = a(\ln(\cosh(b\,w))/b + w)(d\,\ln(\cosh(V_{ds})) + 1) + e(V_{gs} - V_{ds}/2),$$
$$w = (V_{gs} - V_1) - \tanh(c\,V_{ds})/(2\,c) \quad (6)$$

The gate charge divides into equal charges in the direction to gate-source (Q_{gs}) and gate-drain (Q_{gd}) for V_{ds}=0 V. The gate charge splits up in two different Q_{gs} and Q_{gd} charges for $V_{ds}\neq$0 V as proposed in [10].

The qualitative verification of model [9] is based on a comparison between the extracted and simulated capacitor characteristics as a function of V_{DS} and V_{GS}. The capacitors C_{gs} and C_{gd} of a Siemens HEMT 110 with 2x40 µm gate width were extracted at multiple bias points using an analytical extraction method [11]. The bias dependent characteristics are depicted in figures 5 and 6. The increase of C_{gs} above 80 fF for V_{DS}=0 V is assumed to be a consequence of the extraction due to the conducting Schottky diode.

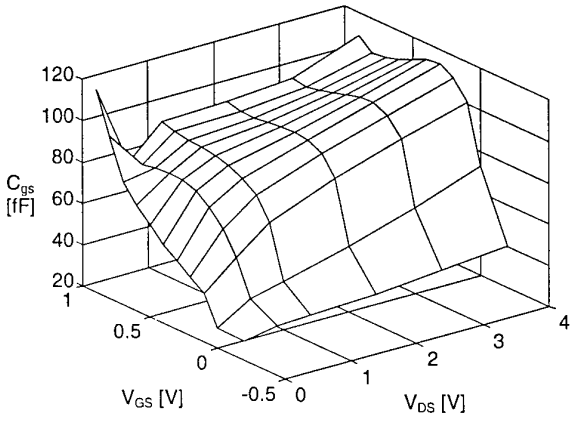

Fig. 5: C_{gs} extracted from measured S-parameter

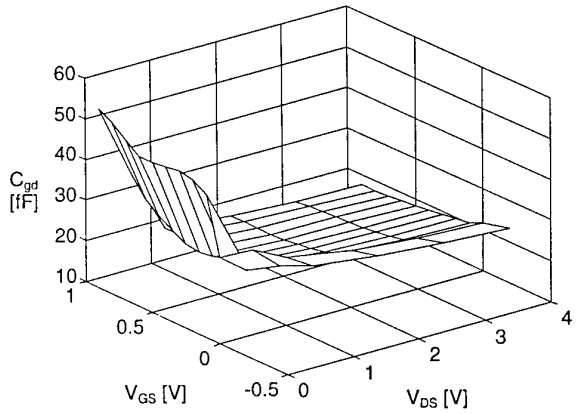

Fig. 6: C_{gd} extracted from measured S-parameters

The coefficients of equation (6) for the gate charge were extracted from measured S-parameters of multiple bias points. The extraction was focused on the modelling of the ohmic region which resulted in a relaxed approximation of the capacitor characteristics in the saturation region. The calculated characteristics using the model published in [9] are shown in figures 7 and 8. The approximation of C_{gs} and C_{gd} compared to the extracted capacitance values is excellent in the ohmic region. Both capacitors have equal values for V_{ds}=0 V.

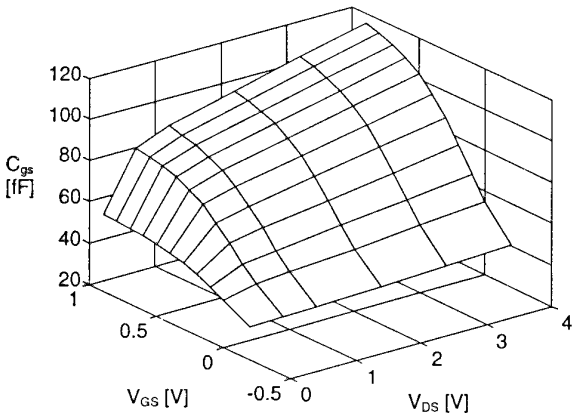

Figure 7: Modelled C_{gs} characteristic

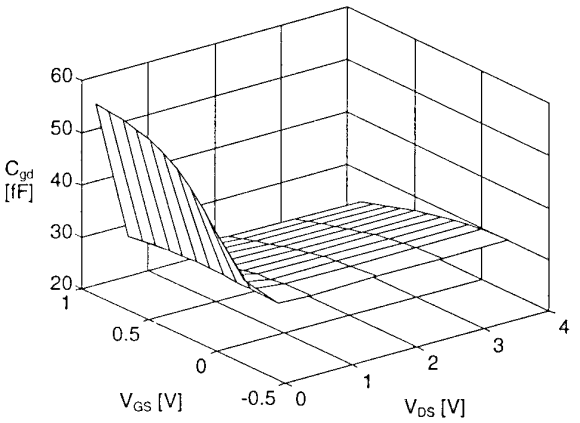

Figure 8: Modelled C_{gd} characteristic

Resistive Mixer Design

A single balanced 76-77 GHz resistive mixer was designed based on the improved large-signal HEMT models. The MMIC circuit is realized in coplanar technology, the principle circuit is shown in figure 9. Two HEMTs with a single gate finger of 30 µm width are balanced by a λ/2 transmission line at the gate electrodes. The local oscillator power is applied via a matching network to the balanced gate electrodes. The rf signal is fed to the matched drain electrodes. The phase shifted intermediate frequency signals are capacitively coupled out from the source electrodes. The HEMTs are realized in the Siemens double-hetero pseudomorphic HEMT 110 technology.

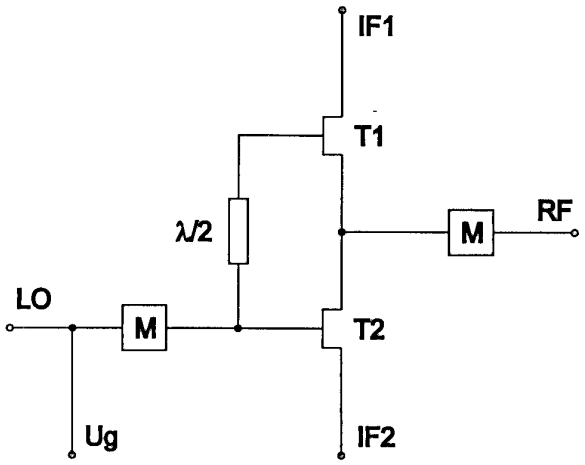

Figure 9: Principle circuit of balanced resistive mixer

Measurement Results

Measured and simulated conversion gain versus local oscillator power are shown in figure 10. The two intermediate frequency signals are externally combined during the measurements. For the comparison with the combined measured signals 3 dB are added to the simulated conversion gain from one intermediate frequency signal.

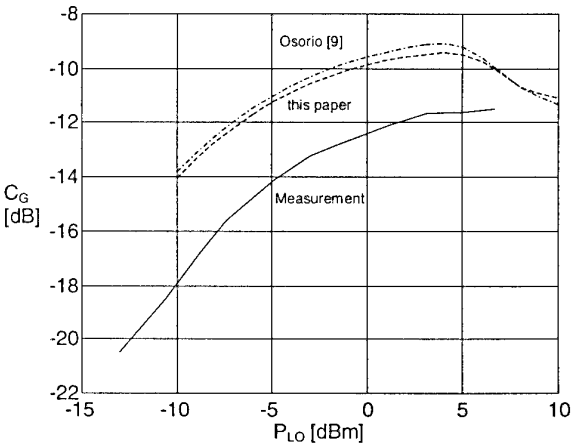

Figure 10: Measured and simulated conversion gain versus local oscillator power

The measured and simulated bias dependence of the conversion gain are depicted in figure 11. The measured and simulated 1 dB compression point of the conversion gain appeares at the rf-power of -1 dBm for a local oscillator power level of +3 dBm. At a lower oscillator power level of -4 dBm the 1 dB compression point occurs at -5 dBm.

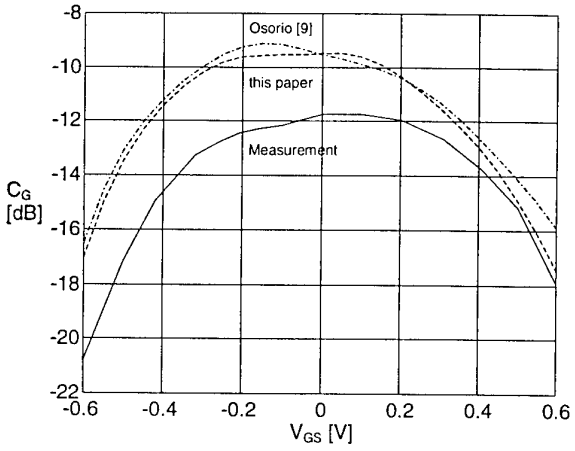

Fig. 11: Measured and simulated conversion gain versus gate bias voltage

Both models give almost equal results compared to each other. The overall behaviour of the conversion gain dependence on local oscillator power level, bias level and rf-power level is accurately described by both models. The simulated conversion gain is about 2 dB higher than the measured values at the rf-frequency of 77 GHz and the intermediate frequency of 100 kHz. The measured conversion gain of -11.5 dB can be enhanced if the impedances of the intermediate frequency ports are better matched.

Conclusion

Resistive mixers operate in the ohmic region of a transistor. Existing large-signal HEMT models give only an approximate description of the ohmic region which is not accurate for a resistive mixer design. Two large-signal HEMT models are investigated for the mixer design in the millimeter wave frequency range. The charge conservation is obeyed in both models. The gate charge of a simplified model presented here depends only on the gate voltage. The gate charge of a second model [9] depends on gate and drain voltages. Both models lead to almost equal results. The simplified model is therefor completely sufficient for an accurate description of the resistive mixer properties.

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A physics-based non-linear FET model including dispersion and high gate-forward currents

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Abstract

A physics-based large-signal FET and HEMT model has been implemented in a commercial HB simulator. The model precisely describes the low-frequency dispersion effects as well as the diode conduction case. Its equivalent circuit elements are described by data tables instead of approximating analytical functions. The validity of the concept is proved in the analysis of an MMIC frequency doubler from 12 to 24 GHz.

I. Introduction

Tough market competition drives semiconductor companies to permanent optimisation of their circuits' performances with respect to price. While developing new transistor technologies is long-term and rather expensive, direct improvements can be gained by using existing transistors optimally. To achieve this goal, highly-accurate large-signal models are needed, especially in non-linear circuits such as frequency multipliers, oscillators or power amplifiers.

Various large-signal models [1-3] have been proposed that are based on equivalent circuits with element values extracted from DC- and S-parameter measurements. These wide-spread models describe the bias-dependence of their equivalent-circuit elements with empirical equations, whose non-physical parameters are obtained by data-fitting. While this allowed for easy implementation in first-day harmonic-balance (HB) simulators, it sacrifices accuracy to a strong degree. Also, these simple models ignore low-frequency dispersion effects.

Our table-based dispersive FET-model solves the trade-off between ease-of-use and accuracy by means of spline-interpolation from two-dimensional tables for the constitutive equivalent circuit elements. The dispersion of the drain-source current generator is modelled by an expression that combines DC- with RF-quantities, considering the influence of the waveform. We so obtain a technology-independent model, whose validity for HEMTs we prove here, while its applicability for MESFETs is demonstrated in [7].

II. Model description

The model is straightforwardly derived from the well-accepted small-signal model (Fig. 1) under consideration of the device physics. The equivalent circuit includes the gate-forward mode via the two conductors G_{gs} and G_{gd}. The symmetric model (R_i *and* R_{gd}) consists of an intrinsic circuit, whose element values are different for every single bias point. The extrinsic circuit includes the resistances R_g, R_s, and R_d, as well as the parasitic capacitances and inductances that model the effects of the embedding test structure used for on-wafer S-parameter measurements.

The derivation of the model parameters is simple. S-parameter measurements are the basis for the extraction of the small-signal equivalent circuit [4-7]. The state-functions are obtained by integrating over the small-signal quantities. Two special integration paths are chosen to average measurement errors and to improve integrability [8].

Charge sources

The large-signal topology (Fig. 2) maintains the structure of the small-signal equivalent circuit. Two charge sources are used symmetrically to the gate incorporating the effect of the three capacitances. The charges at the bias point $\vec{V} = (V_{gs}, V_{ds})^T$ are obtained via path-independent integration [8] over the small-signal quantities, starting from an arbitrary vector $\vec{V}_0 = (V_{gs0}, V_{ds0})^T$:

$$Q_{gs}(\vec{V}) = \int_{\vec{V}_0}^{\vec{V}} (C_{gs}, C_{ds}) d\vec{v} \qquad (1)$$

$$Q_{gd}(\vec{V}) = \int_{\vec{V}_0}^{\vec{V}} (-C_{ds} - C_{gd}, C_{gd}) d\vec{v} \qquad (2)$$

The symmetric topology is superior to the conventional one [9-11], where Q_{gs} and Q_{ds} are used, and is motivated by device physics. It allows to maintain the non-linear loading resistances R_i and R_{gd} in the circuit instead of using time-delay constants [9,10] that do not occur in the small-signal circuit [12,13].

In Fig. 3, the normalised charges are given exemplarily for an 0.3 µm HEMT [19]. The little circles in the drawing locate the arbitrary integration starting point $\vec{V}_0$, while the points in the upper right corner were not measurable because of their too high power dissipation.

Dispersion modelling

The frequency dependence of transconductance G_m and output conductance G_{ds} is called low-frequency dispersion, as the transition region between the high-frequency behaviour (index "RF") and the quasi-DC behaviour (index "DC") lies in the kilohertz range. The early "quasi-DC" approximation of the drain-source current generator [1-3] did not yet cover dispersion:

$$I_{ds}(t) \approx I_{ds,DC}(\vec{V}(t)) = I_{ds,DC}(\vec{V}_0) + \int_{\vec{V}_0}^{\vec{V}(t)} \vec{G}_{DC} d\vec{v} \qquad (3)$$

with $\vec{V}(t) = (V_{gs}(t), V_{ds}(t))^T$ being the present vector of the intrinsic voltages, $\vec{V}_0(t)$ the quiescent bias point, $I_{ds,DC}$ the DC I/V-characteristic and $\vec{G}_{DC}(\vec{v}) = (G_{m,DC}(\vec{v}), G_{ds,DC}(\vec{v}))$.

Equation 3 has very soon been modified to the "quasi-static" description by Rauscher and Willing [14], taking dispersion into account by using the RF-conductances $\vec{G}_{RF}$:

$$I_{ds}(t) \approx I_{ds,DC}(\vec{V}(t)) + I_{corr}(\vec{V}(t), \vec{V}_0) = I_{ds,DC}(\vec{V}_0) + \int_{\vec{V}_0}^{\vec{V}(t)} \vec{G}_{RF} d\vec{v} \qquad (4)$$

with the correction current defined as:

$$I_{corr}(\vec{V}(t), \vec{V}_0) = \int_{\vec{V}_0}^{\vec{V}(t)} (\vec{G}_{RF} - \vec{G}_{DC}) d\vec{v} \qquad (5)$$

In [14], $\vec{V}_0(t)$ was chosen as $(0V, 0V)^T$, which however led to unnecessarily long integration paths. A better description of the dispersive current source has been identified in [15]:

$$I_{ds}(t) = I_{ds,DC}(\vec{V}(t)) + I_{corr}(t) - \overline{I_{corr}(t)} \qquad (6)$$

where the time-averaged value of $I_{corr}(t)$ is subtracted, and where V_{gs} is delayed by the time constant τ. While this formula has been found empirically for strongly dispersive HEMT devices, we have proven this to be equivalent to

$$I_{ds}(t) = DC\left\{I_{ds,DC}(\vec{V}(t))\right\} + AC\left\{\int_{\vec{V}_0}^{\vec{V}(t)} \vec{G}_{RF} d\vec{v}\right\} = DC\{I_{ds,DC}\} + AC\{I_{ds,RF}\} \qquad (7)$$

This presentation is intuitive, as it shows that the DC-flow is solely defined by the DC-characteristic, and the AC-flow solely by the RF-values of the conductances, that are extracted from measured S-parameters. Clearly, the large-signal current I_{ds} depends only on the values of $I_{ds,DC}$ and $I_{ds,RF}$ that are reached dynamically by the voltage vector, and not on an arbitrary quiescent bias point $\vec{V}_0$ or the time-averaged point $\overline{\vec{V}(t)}$, that loose their significance for large-signal excitations. Equation 7 takes

directly the trajectory of the voltages and thereby the shape of the waveform into account, eliminating thus the simplifying assumption, that some sort of averaged point of the voltage trajectory is required [16].

Fig. 4 gives the difference quantities $G_{m,RF}$ - $G_{m,DC}$ and $G_{ds,RF}$ - $G_{ds,DC}$ of the IAF-HEMT technology [19]. For the 2*50 µm transistor used in the frequency doubler, the difference transconductance $G_{m,RF}$ - $G_{m,DC}$ was up to 10 mS, for a maximum value of about 60 mS for $G_{m,DC}$.

Diode modelling

The gate-forward conduction is a major phenomenon limiting the input voltage swing. Its incorporation is therefore a key requirement for a complete large-signal model. Generally, two ideal diodes are considered whose parameters (ideality factor n and reverse saturation current I_{ss}) are fitted to optimally approximate the measured DC-characteristics. This approach is justified, since the diodes are non-dispersive.

In Fig. 5, the measured *static* gate current is given on a logarithmic scale. A slow increase of I_g with V_{ds} for $V_{ds} > 1V$ can be observed which is not explainable with the simple diode model. This increase occurs with both HEMTs and MESFETs and is due to the increase of the device temperature in the *static* (as opposed to *pulsed*) DC-measurements.

To model this effect, first of all the temperature voltage $U_T = kT_x/q$ has to be related to the channel temperature T_x (and not the ambient temperature T_0). The channel temperature itself is determined in a first order approximation as

$$T_x = T_o + R_{therm} * P_{diss}\,, \qquad (8)$$

with P_{diss} being the time-averaged dissipated power in large-signal applications. While the thermal resistance R_{therm} is idealised to be constant, the thermal capacitance can be omitted in steady-state high-frequency modelling (the resulting time constant is several orders of magnitude higher than the signal period).

The complete temperature dependence of the diode current (e.g. [17]) is therefore applicable to dynamic excitations:

$$I_{diode} = I_{ss}(T_x)\left(e^{\frac{V_{gs}}{nU_T(T_x)}} - 1\right) \qquad (9)$$

$$I_{ss}(T_x) = I_{sso}T_x^{\,2}e^{\frac{-V_{go}}{U_T(T_x)}} \qquad (10)$$

The 4 parameters (n, I_{sso}, R_{therm}, and the Schottky junction barrier height V_{go}) required to fully describe the diode behaviour are obtained by fitting $\log(I_g)$ simultaneously for several measurement points.

Fig. 6 shows the input current vs. input voltage trajectory of an 0.5 µm MESFET [7]. When the diode conduction sets on, the input voltage is clipped, which is well reproduced in the large-signal simulations.

III. Model implementation

The model has been implemented on the user-level of the commercial HB simulator MDS [18], without the need to develop special C-code subroutines, nor to access IC-CAP extensions.

While the constant extrinsic elements are described in the frequency domain in an HB simulation, the intrinsic elements are dependent on the momentary voltages and are thus time-dependent. In the MDS simulator, time-dependent, i.e. non-linear relations are inserted using "symbolically defined devices" (SDDs), where equations describe the currents and voltages at various ports in the time domain.

The large-signal model (Fig. 7) is implemented using a 7-port SDD, 5 of which describe the intrinsic topology of the transistor. The remaining 2 ports sense the temperature $T_x(t)$, that is needed for the diode modelling, and $V_{gs}(t-\tau)$, with τ being a function of $V_{gs}(t)$ and $V_{ds}(t)$.

The current I(t) through the charge sources is defined as:

$$I_Q(t) = \frac{dQ(\vec{V}(t))}{dt} \qquad (11)$$

which inherently ensures charge conservation and absence of DC-current. The derivative of above formula is calculated in the frequency domain by means of multiplication with the predefined "weighting function" no. 1, viz $j\omega$.

For every point of time, the equivalent circuit element values are determined by spline-interpolation from the two-dimensional look-up tables, with $V_{gs}(t)$ and $V_{ds}(t)$ being the indices. In MDS this is accomplished with "dataset variables". The look-up tables are stored in a single data set, which is read into MDS as a citi-file. A MATLAB routine has been developed that creates the look-up tables from DC- and S-parameter measurements using equations specified in [8].

The implementation of the dispersive current source is similar to that proposed by Root [9], and only separates between low-frequency and high-frequency behaviour. The cut-off angular frequency is arbitrarily set to $1s^{-1}$ (cf. Eqn. 7):

$$I_{ds}(\omega) = \frac{1}{1+j\omega} I_{ds,DC}(\omega) + \frac{j\omega}{1+j\omega} I_{ds,RF}(\omega) \qquad (12)$$

While the partial currents $I_{ds,DC}$ and $I_{ds,RF}$ are evaluated in the time domain, the respective low/high pass filtering is carried out in the frequency domain using self-defined weighting functions.

IV. Application to a monolithic frequency doubler

An MMIC frequency doubler (Fig. 8) from 12 to 24 GHz has been designed in the 0.3 µm AlGaAs HEMT technology from FhG-IAF [19] accessible via EuroPractice.

The frequency doubler has been measured on-wafer using an advanced waveform measurement set-up [20] based on the microwave transition analyzer HP-70802A. Measurements and simulations were carried out for various fundamental frequencies and input-powers (Fig. 9). The doubler features a maximum conversion gain of -2 dB for an input power of 2 dBm, and a maximum output power of 2 dBm.

The agreement between simulation and measurement is far more precise than reported earlier in [11]. Due to better models for the passive components [21], the problem of the remaining frequency shift observed in [11] is now also resolved. Since all sweeps (Fig. 9) show excellent agreement for the fundamental, the desired doubled frequency and also the third harmonic, this new modelling approach is successfully validated.

V. Conclusion

In this paper, the theory, derivation, and implementation of a table-based non-linear FET model have been presented. This physics-based large-signal model contains symmetrical charge sources delayed via loading resistors as well as a precise description of the diode currents and the low-frequency dispersion. The accuracy of this approach has been demonstrated in an MMIC frequency doubler analysis.

Acknowledgements

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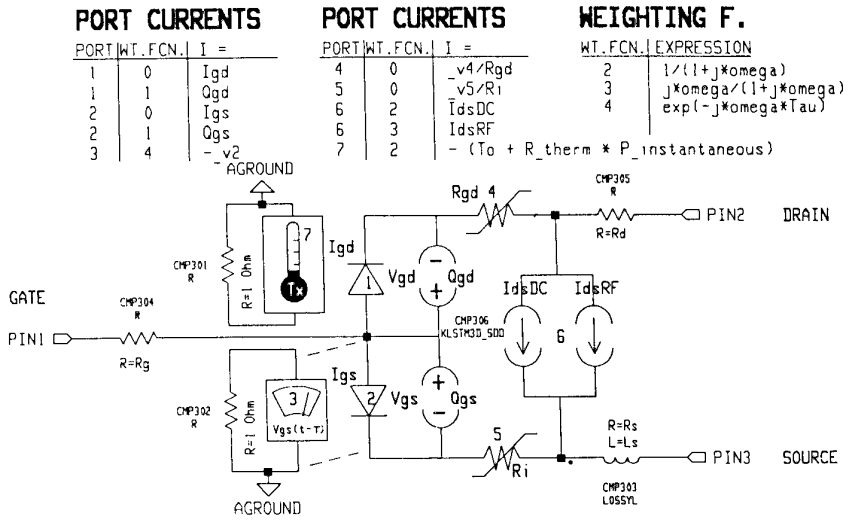


Fig. 7 Implementation of the large-signal model on a simulator circuit page

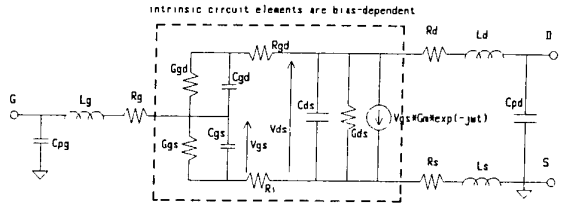


Fig. 1 Complete 18 element symmetric small-signal equivalent circuit

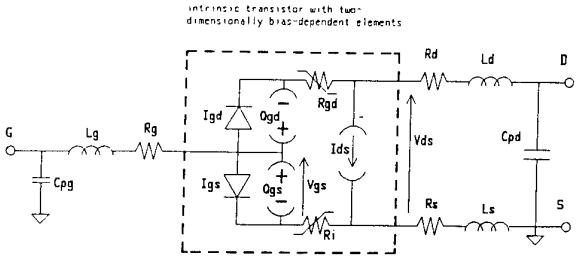
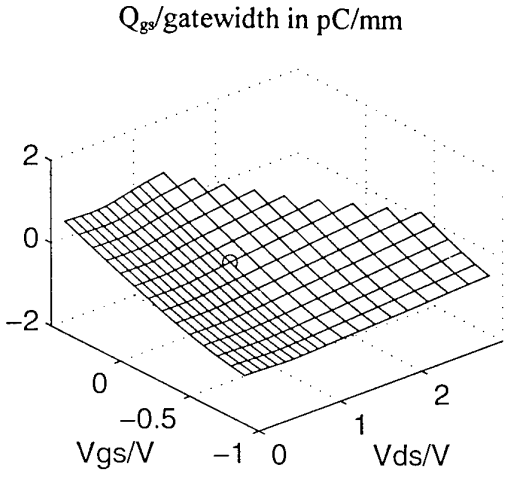
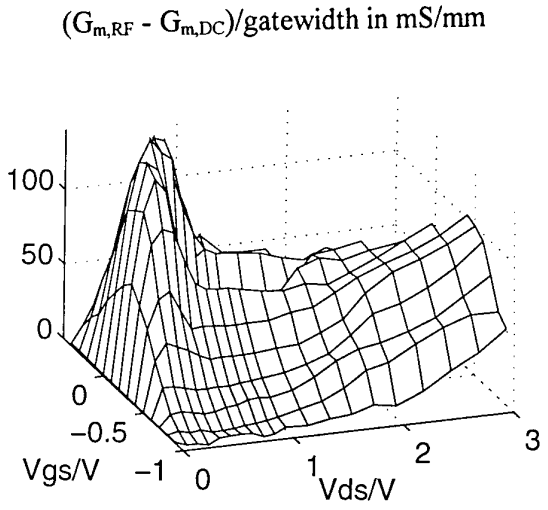
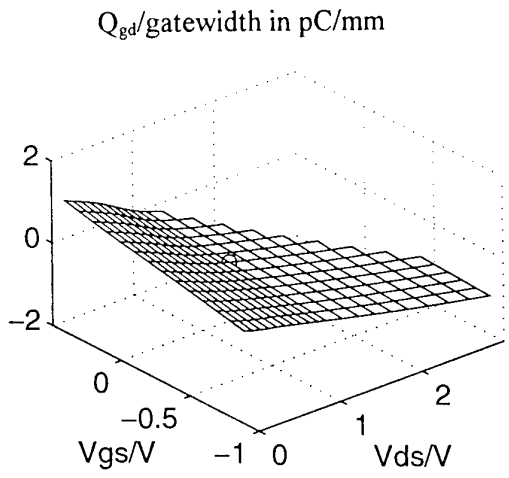


Fig. 2 Large-signal equivalent circuit







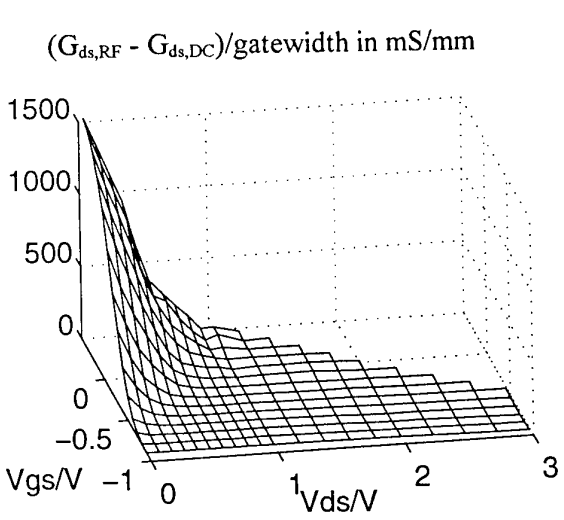


Fig. 3 Charge sources of the used 0.3 µm AlGaAs HEMT

Fig. 4 Difference quantities of dispersion of the 0.3 µm AlGaAs HEMT

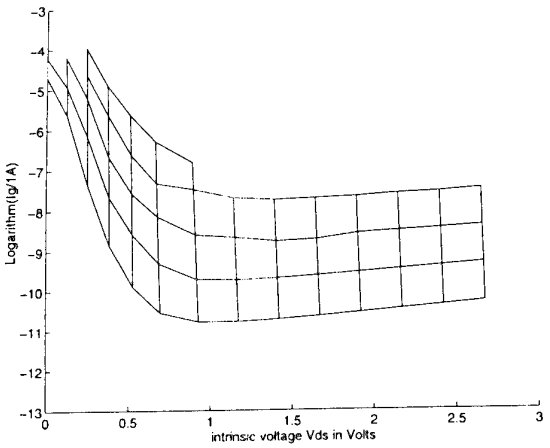


Fig. 5 Gate current of the 0.3 µm AlGaAs HEMT on a logarithmic scale

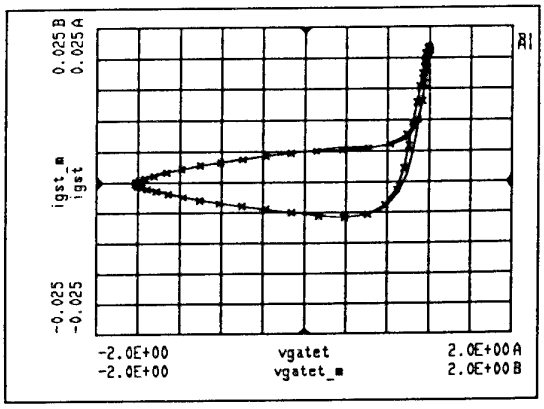


Fig. 6 Input trajectory of a 4x75 µm GEC F20 MESFET (V_{gs}=0V, V_{ds}=4V, P_{in}=10dBm) fundamental frequency = 1 GHz
crosses: measurements, lines: simulations

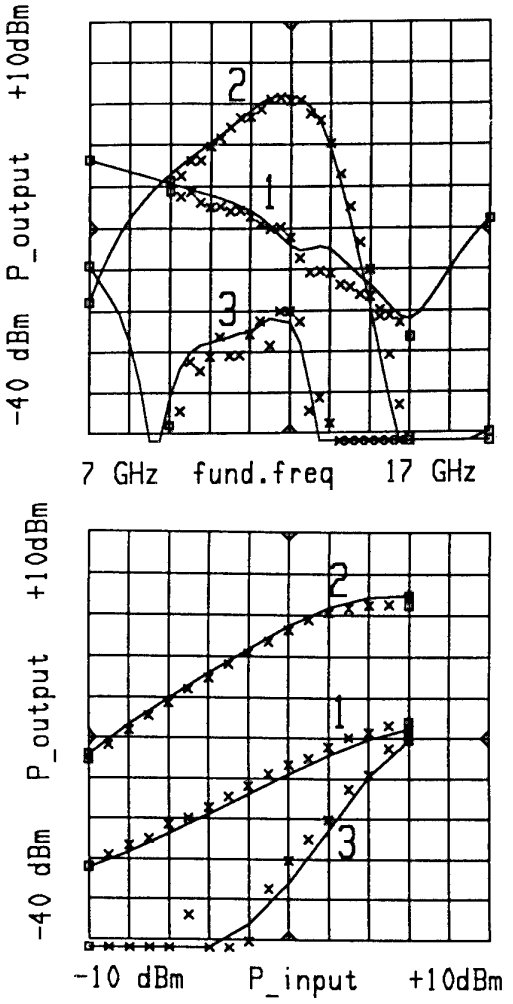


Fig. 9 Sweeps vs. fundamental frequency (top) and vs. input power (down);
output power of the fundamental (1), desired doubled (2) and tripled (3) wave;
crosses: measurements, lines: simulations

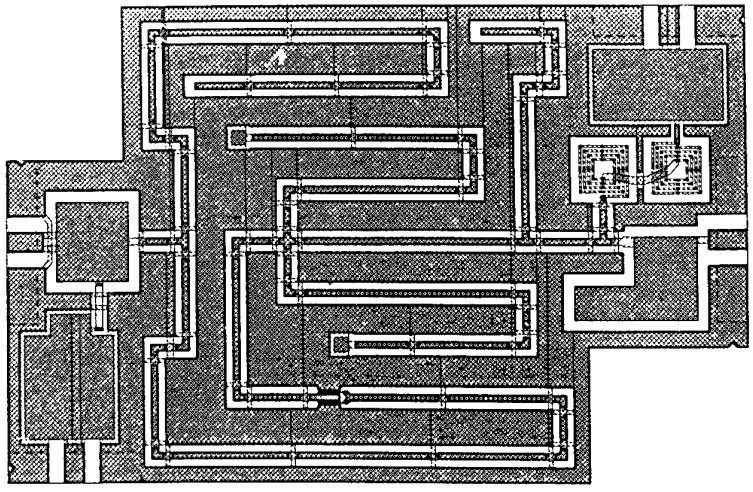


Fig. 8 Layout of the MMIC frequency doubler

Direct Nonlinear FET Parameter Extraction Using Large-Signal Waveform Measurements

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Abstract

A method is presented which permits a direct nonlinear FET parameter extraction of the drain current generator and gate source capacitor from large-signal waveform measurements. The large-signal RF drain current generator characteristics are extracted for a MESFET, HEMT and power MESFET. Significant differences between the DC and large-signal RF characteristics are observed and traced back to low frequency dispersion and thermal effects of the nonlinear drain current generator. This method can be used for the analysis of FET nonlinearities and the improvement of large-signal FET models.

Introduction

The first pass success design of nonlinear microwave circuits requires reliable large-signal FET models. The parameters of large-signal FET models which are implemented in commercially available circuit simulators are usually extracted from the measured FET DC-characteristics and S-parameters [1]. Approximations of the nonlinear characteristics with analytical functions and the neglection of frequency dispersion in the drain current generator can lead to inaccurate simulation results [2]. Dispersion effects can approximately be considered if the coefficients of the analytical function for the drain current generator characteristic are optimized to match the measured DC-characteristic and S-parameters simultaneously [3]. The accuracy of this simultaneous fitting depends on the degree of frequency dispersion in the FET under investigation.

Normally the FET large-signal characteristic is predicted with a model which was extracted from measured DC and S-parameters. The reverse way is followed in this paper. The FET voltage and current waveforms were precisely measured under large-signal RF excitation. The measured voltage and current spectra were transformed through the parasitic FET equivalent circuit elements and used to analyse the characteristics of the FET nonlinear drain current generator and gate-source capacitor characteristics which are effective under large-signal RF excitation.

Nonlinear Deembedding Procedure

The fundamental data of the nonlinear extraction method are the measured DC characteristics, the S-parameters of multiple DC bias points and the voltage and current spectra measured in the outer FET reference planes (V_{GS}, V_{DS}, Figure 1) for different DC bias points, RF input power levels and fundamental frequencies. The FET voltage and current spectra ($\underline{V_{GS}}$, $\underline{I_{GS}}$, $\underline{V_{DS}}$, $\underline{I_{DS}}$) were measured in a large-signal waveform measurement system [4] with 40 GHz harmonic bandwidth. The FET small signal equivalent circuit elements were obtained by a consistent extraction method described in [5]. The bias dependent small signal equivalent circuit elements (g_m, R_{ds}, C_{gs}, C_{gd}, τ, R_i) were extracted from the measured S-parameters of multiple DC bias points, interpolated with 2-d spline functions and transformed to the inner FET reference plane V_{gs} and V_{ds}.

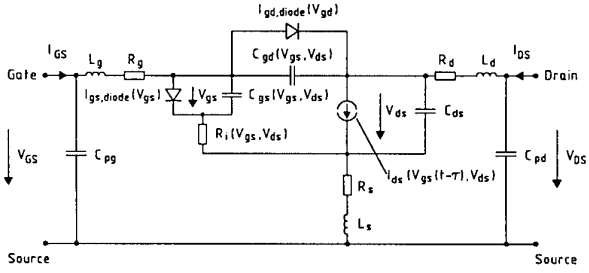

Figure 1: FET large-signal equivalent circuit model

The transformation of the measured voltage and current spectra from the outer FET (Fig. 1) to the inner reference plane (Fig. 2) starts with a deembedding of the bias independent equivalent circuit elements (R_g, R_d, R_s, L_g, L_d, L_s, C_{pg}, C_{pd}, C_{ds}). The measured spectra are transformed for each DC bias point, RF input power level and frequency component, marked with the index i.

$$\underline{I'_{GS_i}} = \underline{I_{GS_i}} - j\omega_i C_{pg} \underline{V_{GS_i}} \quad (1)$$

$$\underline{I''_{DS_i}} = \underline{I_{DS_i}} - j\omega_i C_{pd} \underline{V_{DS_i}} \quad (2)$$

$$\underline{V'_{GS_i}} = \underline{V_{GS_i}} - (R_g + j\omega_i L_g)\underline{I'_{GS_i}} - (R_s + j\omega_i L_s)(\underline{I'_{GS_i}} + \underline{I''_{DS_i}}) \quad (3)$$

$$\underline{V_{ds_i}} = \underline{V_{DS_i}} - (R_d + j\omega_i L_d)\underline{I''_{DS_i}} - (R_s + j\omega_i L_s)(\underline{I'_{GS_i}} + \underline{I''_{DS_i}}) \quad (4)$$

$$\underline{I'_{DS_i}} = \underline{I''_{DS_i}} - j\omega_i C_{ds}\underline{V_{ds_i}} \quad (5)$$

After the transformation, the measured spectra ($\underline{V'_{GS}}$, $\underline{V_{ds}}$, $\underline{I'_{GS}}$, $\underline{I'_{DS}}$) of the nonlinear inner part of the FET equivalent circuit model (Figure 2) are available. The complexity and topology of the bias independent equivalent circuit elements depends on the FET under investigation and is no limiting factor for the proposed method.

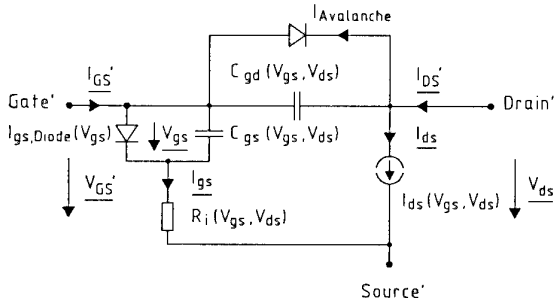

Figure 2: Nonlinear inner part of the FET equivalent circuit model

The gate source diode is approximated with the PN diode model. The corresponding parameters are first extracted from DC measurements. In a second step the ideality factor n has been optimized to match the complex gate current spectra measured under gate forward operating conditions. The function

$$0 = \underline{I'_{GS}} + C_{gd}(V_{gs},V_{ds})\frac{d(V_{ds} - \underline{V'_{GS}})}{dt} - C_{gs}(V_{gs},V_{ds})\frac{dV_{gs}}{dt} - I_{SS}(e^{\frac{qV_{gs}}{nkT}} - 1) \quad (6)$$

is solved for different DC bias points and RF input power levels using harmonic balance analysis. The measured current and voltage spectra $\underline{I'_{GS}}$, $\underline{V'_{GS}}$, $\underline{V_{ds}}$ as well as the bias dependent equivalent circuit elements C_{gs}, R_i and C_{gd} are used for the calculation.

With the parameters of the gate source diode and the bias dependent incremental values of C_{gs} and R_i, the control voltage V_{gs} over the gate source capacitor C_{gs} can be derived from the measured gate voltage spectra $\underline{V'_{GS}}$ with a harmonic balance solution of the equation

$$V_{gs} = V'_{GS} - R_i(V_{gs},V_{ds})I_{gs}. \quad (7)$$

The current $I_{gs,Cgs}$ through the gate source capacitor C_{gs} can be calculated from the measured gate current spectra $\underline{I'_{GS}}$ with a deembedding of the gate drain capacitor C_{gd} and the gate source diode,

$$I_{gs,C_{gs}}(V_{gs},V_{ds}) = \underline{I'_{GS}}(V_{gs},V_{ds}) + C_{gd}(V_{gs},V_{ds})\frac{d(V_{ds} - \underline{V'_{GS}})}{dt} - I_{gs,Diode}(V_{gs}). \quad (8)$$

The current of the gate drain capacitor is calculated as the product of the bias dependent incremental C_{gd} values with the derivative of the measured drain gate voltage with respect to the time. The characteristic of the gate source capacitor is calculated from the deembedded measured gate voltage and current spectra using the equation

$$C_{gs}(V_{gs},V_{ds}) = \frac{I_{gs,C_{gs}}(V_{gs},V_{ds})}{dV_{gs}/dt}. \quad (9)$$

The measured drain current spectra $\underline{I'_{DS}}$ are corrected for the current through the feedback capacitor C_{gd},

$$I_{ds}(V_{gs},V_{ds}) = \underline{I'_{DS}}(V_{gs},V_{ds}) - C_{gd}(V_{gs},V_{ds})\frac{d(V_{ds} - \underline{V'_{GS}})}{dt}. \quad (10)$$

The effect of the control voltage V_{gs} on the drain current generator is taken into account by a nonlinear time delay $\tau(V_{gs},V_{ds})$. The control voltage

$$V_{gs}(t_i - \tau(V_{gs}(t_i),V_{ds}(t_i))) = F^{-1}\left(\underline{V_{gs}}\, e^{-j\omega\tau(V_{gs}(t_i),V_{ds}(t_i))}\right) \quad (11)$$

can be calculated in the time domain for each time sample t_i.

The construction of the nonlinear RF drain current generator and gate source capacitor characteristics has been accomplished by analyzing the deembedded signal waveforms for different RF input power levels and DC bias points. An example of the gate and drain voltages as well as the drain current signal waveforms is depicted in figure 3. The measured signal waveform of the gate voltage has a defined value of for example V_{gs}=0 V at the time points t_1 and t_2. The corresponding instantaneous values of the drain voltage and current can be read from the signal waveforms at these time points. The characteristic of the drain current generator can be extracted from large-signal waveform measurements if this procedure is repeated for different RF input power levels and DC bias points. These characteristics have been found as being significant under large-signal operating

conditions. They can be directly implemented or utilized to analyze the validity of large-signal FET models.

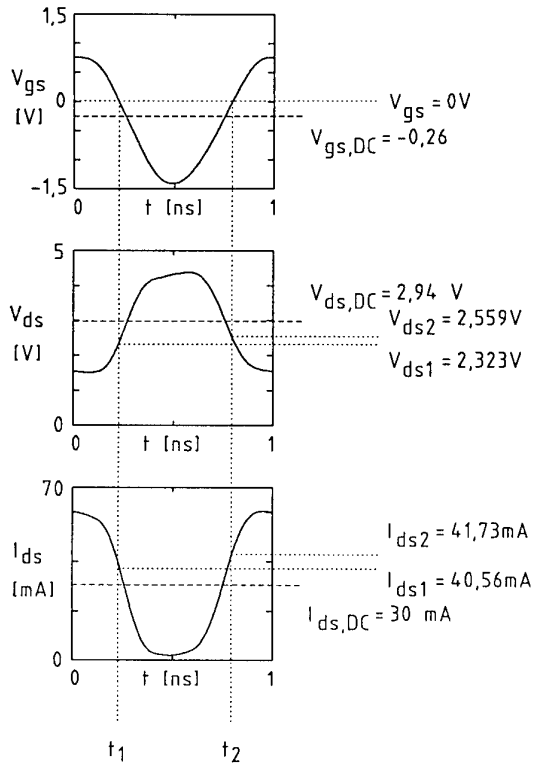

Figure 3: Measured signal waveforms in the inner FET reference plane (MESFET FSX03, f_0=1 GHz, P_{in}=7 dBm)

MESFET FSX03

The voltage and current spectra of a GaAs-MESFET of type Fujitsu FSX03 were measured for 102 different DC bias points/input power level combinations [6]. The measurements are based on a fundamental frequency of 1 GHz, a constant DC gate bias voltage ($V_{GS,DC}$=-0.8 V), 6 DC drain bias voltages ($V_{DS,DC}$=1.5 V, ...(0.5)..., 4 V) and 17 RF input power levels (P_{in}=-9 dBm, ...(1)..., 7 dBm). The solid lines in figure 4 are the bias dependent characteristic of the gate-source capacitor extracted from S-parameters for defined values of the gate source control voltage. The dots are the corresponding values of the gate source capacitor extracted from large-signal waveform measurements. Both extraction methods result in comparable values for the gate source capacitor in the vicinity of the gate bias voltage ($V_{GS,DC}$=-0.8 V) and low RF input power levels. The measurement accuracy and the number of harmonics are limiting factors for the extraction of reactive elements from large-signal waveform measurements. The time derivative of the gate source voltage is necessary for the calculation of the capacitor using equation 9.

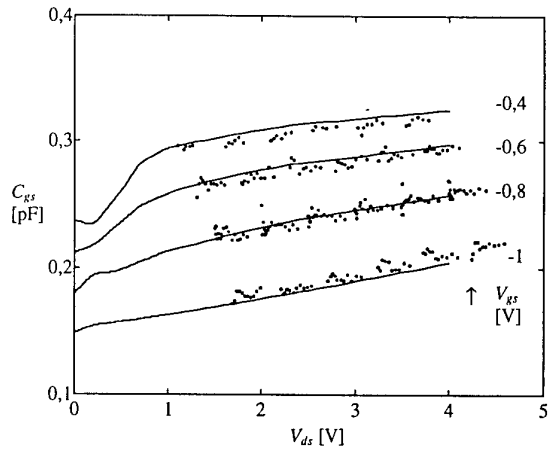

Figure 4: Extracted gate-source capacitor from S-parameters (—) and large-signal waveform measurements (····)

Figure 5 shows the measured DC and RF characteristics of the nonlinear drain current generator for defined inner gate voltages under the same RF measurement conditions as in figure 4.

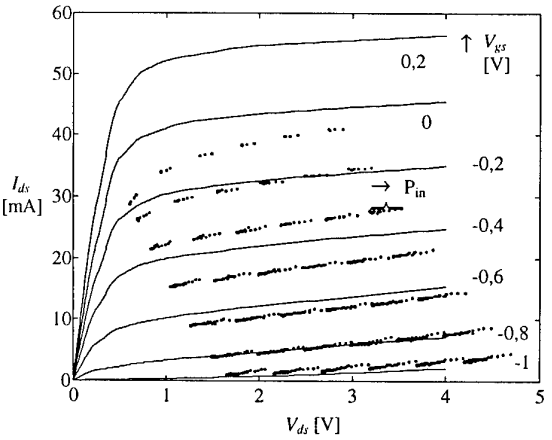

Fig. 5: Measured DC (—) and RF (····) characteristics of the nonlinear MESFET drain current generator (FSX03, $V_{GS,DC}$=-0.8 V)

The grouping of I_{ds} values for every defined gate voltage follows from the selected six drain DC bias voltages. The widening of each group is a result of an input power dependent DC bias point shift. The RF behaviour agrees with the DC characteristic only for instantaneous gate voltages in the vicinity of the gate bias value (V_{gs}=0.8 V). An increasing deviation can be observed with growing difference between instantaneous and DC bias voltages which can be traced back to low frequency dispersion phenomena. The difference between the RF and DC transconductance of the MESFET FSX03 drain current generator is depicted in Figure 6. The important effect in this case is that the RF transconductance is lower than the DC transconductance. This leads to a compression of the drain current characteristic under RF large-signal stimulus

in comparison with the DC characteristic. The maximum transconductance is $g_{m,RF}$=50 mS for this FET. The measured RF characteristics of the nonlinear drain current generator result from a superposition of the DC current in the bias point and a RF current that can be calculated from an integral of the incremental bias dependent RF transconductance $g_{m,RF}$ and output conductance $G_{ds,RF}$ in the V_{gs} and V_{ds} voltage plane from the DC bias point to the instantaneous V_{gs} and V_{ds} values. The integral of the RF transconductance is the important one in the case of this MESFET designed for low power applications due to the low output conductance.

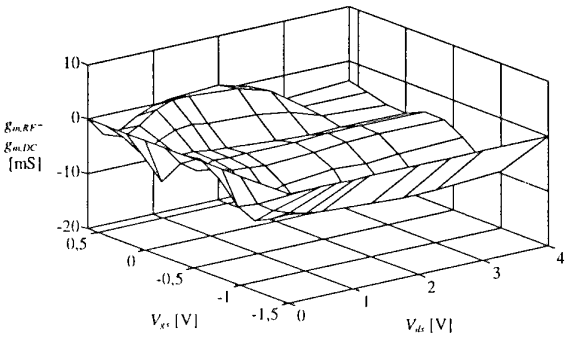

Figure 6: Difference between the MESFET RF and DC transconductance

The large-signal waveform measurements were repeated under the same operating conditions, except the gate bias voltage was changed ($V_{GS,DC}$=-0.2 V). The DC and large-signal RF characteristic of the drain current generator is shown in Figure 7.

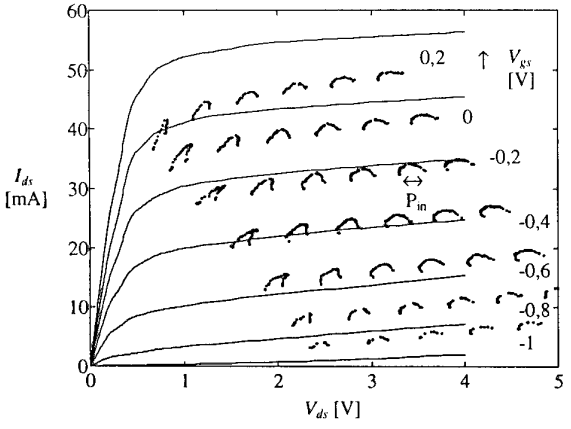

Fig. 7: Measured DC (—) and RF (····) characteristics of the nonlinear MESFET drain current generator (FSX03, $V_{GS,DC}$=-0.2 V)

DC and RF characteristic are approximately identical only in the vicinity of the gate bias voltage (V_{gs}=-0.2 V). A comparison of figures 5 and 7 shows that a different DC bias point results in a change of the nonlinear drain current generator characteristic which is effective under large-signal RF excitation. This bias point dependence can also be found using pulsed DC measurements [7]. The RF drain current generator characteristic of the MESFET shows only a weak dependence on the RF input power level due to the input power dependent shift of the DC bias point.

HEMT JS8902

Similar measurements were carried out on a HEMT of type Toshiba JS8902 for the operating conditions f_0=1 GHz, $V_{GS,DC}$=0 V, $V_{DS,DC}$=1.5 V, ...(0.5)..., 4 V, P_{in}=-10 dBm, ...(1)..., 6 dBm. Figure 8 shows the measured DC and RF characteristics of the nonlinear drain current generator for defined inner gate voltages.

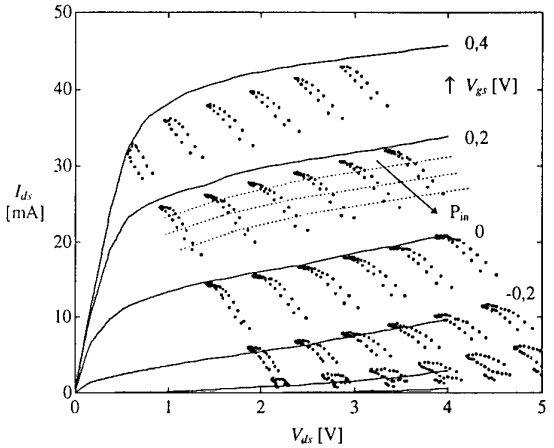

Fig. 8: Measured DC (—) and RF (····) characteristics of the nonlinear HEMT drain current generator (JS8902, $V_{GS,DC}$=0 V)

The DC and RF currents agree for low RF input power levels (V_{gs}=0 V) as it has been observed with the MESFET. Conversely to the MESFET results, the measured RF current of the HEMT nonlinear drain current generator is strongly dependent on the RF input power, it decreases with increasing input power levels. This characteristic is indicated in figure 8 for the gate voltage V_{gs}=0,2 V. The RF input power dependence of the drain current generator is not implemented in large-signal FET models which are based on analytical functions and is not measurable with pulsed DC. The reason for this input power dependence can be explained with the differences between the RF and DC transconductance of the HEMT drain current generator shown in figure 9. This difference of the transconductances is approximately a linear function with respect to V_{gs}. It increases from pinch-off to a maximum at positive gate voltages where the parasitic MESFET channel conduction occures. This steep linear characteristic of the transconductance dispersion results in a strong RF input power dependent DC bias point shift. The integral of the steep linear transconductance dispersion with respect to V_{gs} is a quadratic function which has a significant RF input power dependent contribution to the DC drain current. The maximum transconductance of this FET is $g_{m,RF}$=70 mS for

V_{gs}=0.2 V in the saturation region. The RF input power dependence is implemented in a consistent formulation for the nonlinear drain current generator presented in [8, 9].

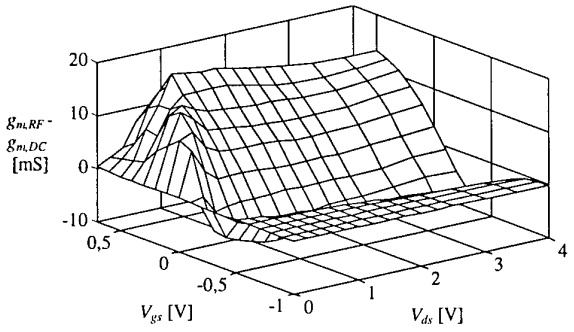

Figure 9: Difference between the HEMT RF and DC transconductance

Power MESFET JS8836

The voltage and current spectra of a power GaAs MESFET of type Toshiba JS8836 were measured at a fundamental frequency of 3 GHz and the operating conditions $V_{GS,DC}$=-2.5 V, $V_{DS,DC}$=8 V and different RF input power levels (P_{in}=10 dBm, ...(1)..., 23 dBm) [9]. Figure 10 shows the measured DC and the extracted RF characteristics of the nonlinear power MESFET drain current generator for defined inner gate voltages.

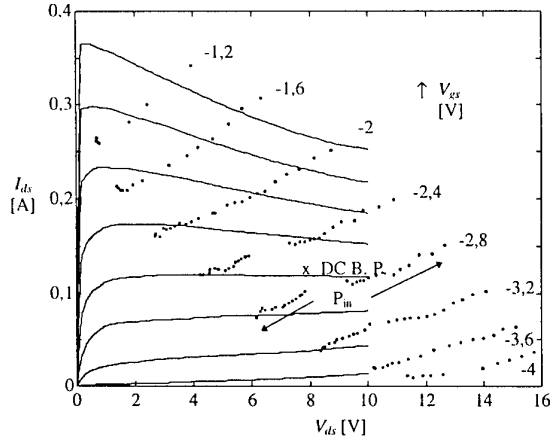

Fig. 10: Measured DC (—) and RF (····) characteristics of the nonlinear power MESFET drain current generator (JS8836, $V_{GS,DC}$=-2.5 V, $V_{DS,DC}$=8 V)

The negative channel conductance of the DC characteristic for higher gate voltages does not appear in the RF characteristic, because the FET channel temperature is approximately constant during the CW-RF excitation. The RF drain current is comparable with the DC characteristic only for instantaneous voltages near the gate and drain bias values and low RF input power levels. A strong deviation can be observed with growing difference between instantaneous and bias voltages which originates in temperature and low frequency dispersion phenomena. The I_{ds}-V_{ds} cross marked traces in figure 11 represent the results obtained under similar measurement conditions due to figure 10 with the exception that the DC drain bias voltage was changed to $V_{DS,DC}$=6 V. The dependence of the RF characteristics on the DC drain bias voltage originates in the relatively high and bias dependent power MESFET output conductance $G_{ds,RF}$. This effect is less visible in FETs designed for low power applications because of their lower output conductance.

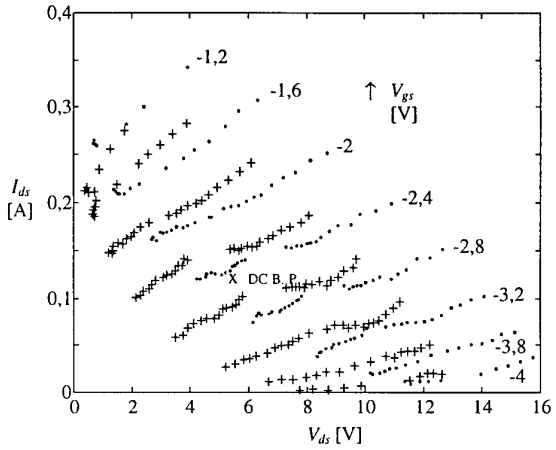

Fig. 11: Measured RF characteristics of the nonlinear power MESFET drain current generator (JS8836, $V_{GS,DC}$=-2.5 V, $V_{DS,DC}$=8 V (····), $V_{DS,DC}$=6 V (+++))

The integrals from the DC bias point to the instantaneous voltages V_{gs}, V_{ds} over the RF transconductance $g_{m,RF}$ respectively the output conductance $G_{ds,RF}$ have comparable values in the case of this power MESFET. The implementation of the DC characteristic in a large-signal FET model and the neglection of low frequency dispersion and thermal effects could lead to erroneous circuit simulation results.

Conclusion

A method is presented for the direct extraction of the nonlinear FET drain current generator and gate source capacitor from large-signal waveform measurements. Significant differences between the DC and RF characteristics of the drain current generator were found and traced back to low frequency dispersion and thermal effects. The dispersion of the transconductance g_m is the essential effect for the MESFET FSX03. The HEMT JS8902 has a specific characteristic of the transconductance frequency dispersion which results in an additional strong RF input power dependence of the nonlinear RF drain current generator characteristic. The accurate modelling of the power MESFET JS8836 requires the additional consideration of output conductance frequency dispersion and thermal effects. The direct nonlinear FET parameter extraction method can be a valuable instrument for the analysis of the effective high frequency FET nonlinearities and the improvement of large signal FET models.

Acknowledgement

The contents of this paper originates during my work as an assistent of Prof. Dr. G. Kompa in the department of high frequency engineering at the university of Kassel. Dr. F. van Raay developped the large-signal waveform measurement system and performed the nonlinear measurements. The FET small signal parameter extraction method was developped by Dr. F. Lin.

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Low Noise FET Frequency Doubler Design Using (P)HEMT and MESFET Technologies

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Abstract

We designed frequency doublers using 0.5μm D-MESFET, 0.3μm E-HEMT and 0.2μm D-PHEMT process. The E-HEMT doubler required lowest input power to achieve conversion gain saturation , which is a precondition for the low noise performance of the signal source. The noise conversion factors, AM/AM and AM/PM, were measured with good correspondence to simulations. The second harmonic conversion loss of the 40GHz HEMT doublers was 2-5 dB and output power +2dBm. The 20GHz MESFET doubler had P_{out}=+5dBm and a minimum conversion loss of 4dB.

1. Introduction

Monolithic integration of millimetre wave signal sources is a critical requirement for various millimetre wave systems. The main advantages are size, weight, reliability and compatibility with monolithically integrated transmitter/receiver units (single chip or MCM systems). A versatile option for millimetre wave oscillator is the use of a frequency multiplier and a microwave oscillator. Typically the phase noise performance is improved because of the use of silicon technology in the oscillator and the realisation of phase locking is less complicated [1].

Low noise signal sources are required in modern telecommunication and radar systems. Therefore, the conversion of oscillator noise to the amplitude and phase noise of a frequency doubler should be minimised. Ideally only the phase noise of the oscillator causes phase modulation in the frequency doubler. In this case the PM/PM conversion factor is 2 deg/deg. The amplitude noise will be unaffected (AM/AM = 1 dB/dB) and will not contribute to the phase noise of the frequency doubler [2]. The practical frequency doubler is a nonlinear device which multiplies or limits the amplitude noise. The amplitude noise is also converted into phase noise (AM/PM) due to the nonlinear response of the frequency doubler. A low noise CW oscillator has typically very low AM noise, while the AM may increase considerably in FM, FSK and pulsed operation. The phase noise in the frequency doubler may also increase e.g. due to the upconversion of the $1/f$ noise of the FET [3].

2. Design methodology

The frequency doublers were designed using conventional single-stage, common-source FET configuration [3]. The FET was biased in saturation region, but close to pinch-off. This is the typical biasing of a class-B power amplifier. The drain of the FET was shorted at the fundamental frequency f_0 by using a quarter-wave open stub. This filtering rejected the f_0 and $3f_0$ signals and did not attenuate the $2f_0$ signal. The FET has internal linear feed-back on the second harmonic frequency, which deteriorates the performance of the frequency doubler [4]. To eliminate the effect of the feed-back, the $2f_0$ signal was shorted on the gate of the FET by using a $\lambda_g/2$ shorted stub. This stub presented a high impedance to the f_0 input signal. The Q-values of the parallel stubs depended on the characteristic impedances of the transmission lines in the stubs. To achieve wide bandwidth performance, low Q-value, low impedance stubs were needed. Different transmission line technologies posed limitations to the achievable characteristic impedance in reasonable circuit area. Figure 1 shows the schematic of the circuits.

The preliminary matching of frequency doublers was performed using linear analysis. The doubler circuit was analysed in the previously described configuration. Conjugate matching to 50Ω at fundamental frequency was designed to the input of the frequency doubler. At the output the reactive part was conjugatively matched at the $2f_0$ frequency and the resistive load was calculated for maximum output power [3]. We optimised these matching networks using large-signal harmonic balance analysis to obtain the required conversion gain. The matching networks did not have an effect on the impedances presented to the FET at the other significant harmonic

frequencies due to presence of the shorting stubs at the gate and drain of the FET.

3. Non-linear transistor model

We performed the simulation of the frequency doublers using different FET nonlinear models. The 20GHz D-MESFET frequency doubler was simulated using Curtice cubic [5], Tajima [6] and Materka [7] models. The 40GHz frequency doublers were simulated using foundry proprietary model [8] and Berroth model [9]. These models were implemented in APLAC[10] and MDS[11] circuit simulator softwares.

The frequency doubling in these circuits was based on the pulse formation of the drain current I_{ds}, which has been shown to be more important for the creation of the harmonic components than the nonlinearity of g_m or g_d [12]. The I_{ds} may be approximated by a half wave rectified cosine signal and described as fourier series of the f_0 and harmonic frequencies of f_0. The fourier coefficient of the second harmonic $2f_0$ is 21.2 % of the peak value of I_{ds} [3]. Thus the most significant requirement for the drain current modelling was the correct prediction of drain current pulse maximum value. The simulated output power in conversion gain saturation was close to the true value, if the I_{dss} value of the FET and the model corresponded well. When the input power was decreased from the conversion gain saturation value, the importance of correct threshold voltage in the simulation model was emphasised. The simulation error caused by change in V_t is demonstrated in Figure 2 [13].

The Schottky-contact of the gate-metal was the second nonlinear component in a FET. The change of the contact capacitance is nonlinear and also the forward conduction of the contact limits very nonlinearly the gate voltage swing. The accurate modelling of the capacitance change as a function of voltages over the contact is critical for example in intermodulation simulations [14]. However, in our frequency doublers the gate capacitance nonlinearity does not contribute significantly to the second harmonic generation [12]. It was important that the very low junction capacitance close to the pinch-off condition of the FET was modelled accurately. This enabled the accurate conjugate matching of the high Q-value (narrow bandwidth) FET input. We did not employ the forward conduction of the gate contact due to the high DC power consumption and suspected degradation of device reliability, although this type of frequency doublers have been reported [15].

4. Comparison of technologies

The main difference in the three device technologies is the achievable drain current with gate voltage swing above threshold voltage. We measured the DC drain current as a function of the gate voltage from the 100μm E-HEMT (Fraunhofer Institut process) and the 90μm D-PHEMT (Philips D02AH process) devices in saturation (V_{ds}=2V) and normalised the results to device size and threshold voltage (Figure 3). The E-HEMT has higher g_m close to threshold voltage and therefore the I_{ds} is 35% greater than the I_{ds} of the D-PHEMT. As a consequence the E-HEMT had capability for higher second harmonic output power at low input power levels, when the drain current pulse duty cycle was constant. Additional advantage was the single supply operation of the E-HEMT. The 300μm D-MESFET (GEC-Marconi F20 process) had the lowest relative g_m and largest gate contact capacitance C_{gs}, so it was best suited for microwave frequency doubling.

We designed the passive filtering and matching networks on the MMICs using inductors, microstrips or CPW transmission lines. Inductors required the lowest chip area, but the resonance frequencies of the inductors were close to 20GHz. Microstrips were easy to apply in these designs, because the microstrip models are implemented in simulation softwares. The CPW lines and discontinuities have to be characterised specifically for certain dimensions [16]. CPW lines required less area, because the coupling between adjacent lines was reduced by the ground planes and the change of characteristic impedance was done by modifying the centre conductor width. A low impedance microstrip would require a very large area due to the width of the microstrip.

5. Measurement results

The responses of the processed 40GHz frequency doublers at f_0 and $2f_0$ are shown in Figures 4-7 [17]. Figure 4 shows the CPW technology, 2x50μm E-HEMT device, circuit response as a function of input power. Circuit processing was performed at Fraunhofer Institut in Freiburg, Germany. We analysed the processed circuits by measuring the DC-characteristics of the E-HEMT and resonant frequencies of the CPW filter stubs. As a result, the smaller than 5% errors in stub resonant frequencies and the -0.1 V change in the V_t of the FET were taken into account in simulations. The circuit response as a function of input frequency is shown in Figure 5. We obtained wide-bandwidth f_0 signal rejection by using a Z_0 = 50Ω stubs in the filtering networks.

The analysis measurements for microstrip, 6x15μm D-PHEMT frequency doubler showed similar deviations in V_t and filtering stub resonant frequencies. This circuit was processed at Philips Limeil facility in France. The V_t of the PHEMT was -0.15 V lower than expected in the simulation model. The simulated response in Figure 6 is significantly closer to measured results than the one in

Figure 2. The frequency response is show in Figure 7. The characteristic impedance of these microstrip filtering stubs was 90Ω and thus the f_0 signal rejection bandwidth is not as wide as in Figure 5.

For the 4x75μm D-MESFET 20GHz frequency doubler we measured the second harmonic amplitude and phase as a function of fundamental frequency input power. The circuit was processed using F20 process at GEC-Marconi, Caswell, U.K.. The local derivatives of these curves are the amplitude (AM/AM) and phase (AM/PM) conversion coefficients. At low input power levels the amplitude noise was increased according to simulations (Figure 8) and measurements (Figure 9). At high input power levels the amplitude noise is limited as expected. The AM/PM coefficient steadily degrades as input power is increased (Figure 10). However, at output power saturation there is a small input power range where the AM/PM conversion is totally eliminated. This result suggests that the phase noise varies strongly in the conversion gain saturation if AM level is high in the input signal.

6. Conclusion

Efficient millimetre wave signal generation for application in MCM transmit/receive units was demonstrated using D-PHEMT and E-HEMT GaAs technologies. The use of CPW technology in E-HEMT doubler had a cost advantage due to the lower required circuit area and the single-side processing (via-holes for grounding are not necessary). The E-HEMT frequency doubler required less input power for conversion gain saturation, where the low AM noise performance is achieved. The AM/AM and AM/PM conversion coefficients of the 20GHz D-MESFET frequency doubler were simulated and measured. We obtained good correspondence between different nonlinear MESFET models and measured results. This study provides valuable information for the design of low noise signal sources to be used in telecommunication and radar applications.

7. Acknowledgement

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8. References

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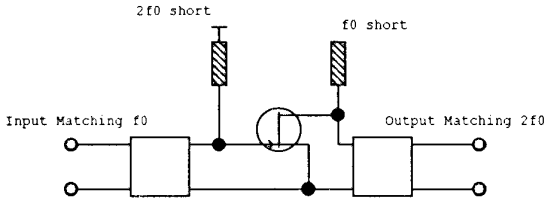

Figure 1. Circuit schematic of the single-stage, common source frequency doubler.

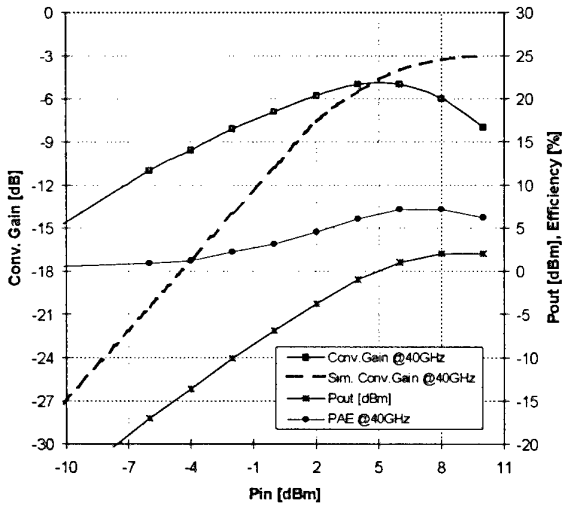

Figure 2. Simulation and measurement of 40GHz D-PHEMT frequency doubler. The V_t of the simulated FET is 0.15V higher than the V_t of the actual measured FET.

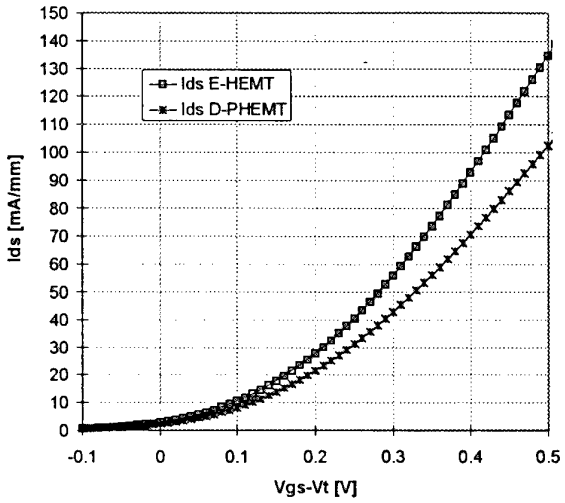

Figure 3. The measured drain current of the FETs in saturation region as a function of gate voltage above V_t. The D-MESFET current would be below 20mA/mm at these gate voltage values.

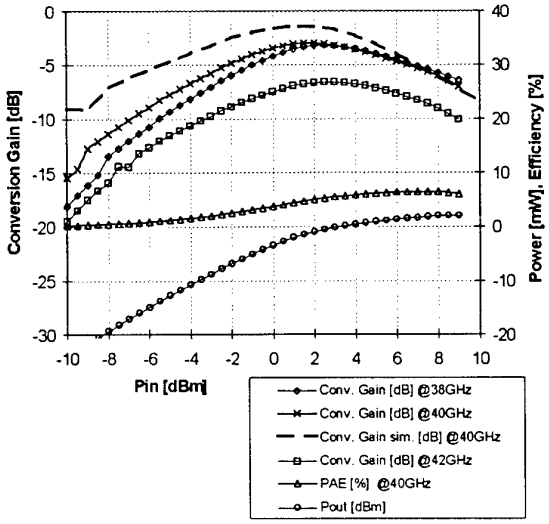

Figure 4. Measured and simulated $2f_0$ conversion gain as a function of input power. The PAE is calculated by dividing the second harmonic output power (Pout) with the sum of DC power and f_0 input power.

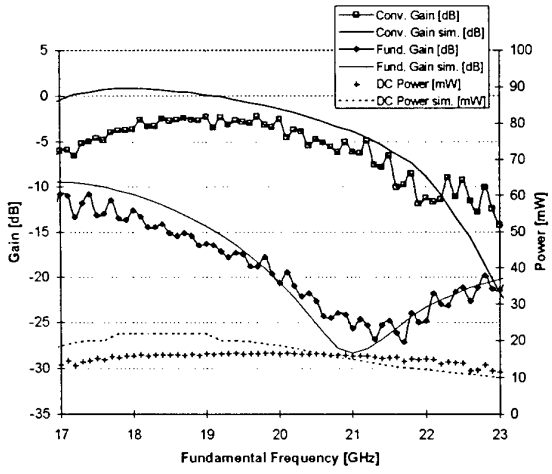

Figure 5. Measured and simulated $2f_0$ conversion gain and f_0 gain for the CPW E-HEMT frequency doubler as a function of input signal frequency. The DC power consumption was also measured and simulated.

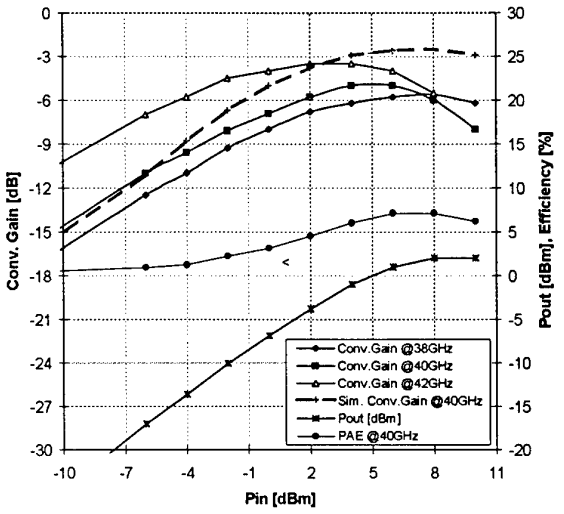

Figure 6. Measured and simulated $2f_0$ conversion gain as a function of input power for the microstrip D-PHEMT frequency doubler.

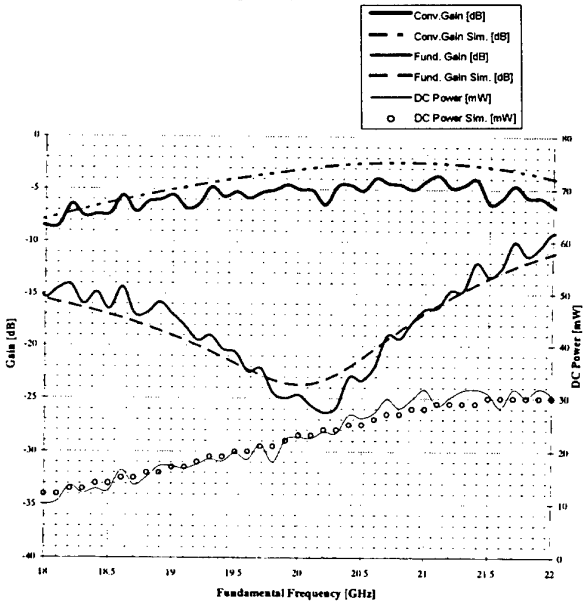

Figure 7. Measured and simulated $2f_0$ conversion gain and f_0 gain for the microstrip D-PHEMT frequency doubler as a function of input signal frequency.

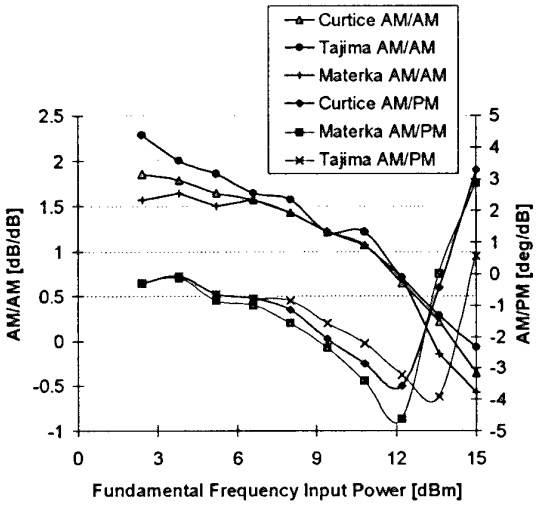

Figure 8. Simulated AM/AM and AM/PM noise conversion factors for the 20GHz D-MESFET frequency doubler.

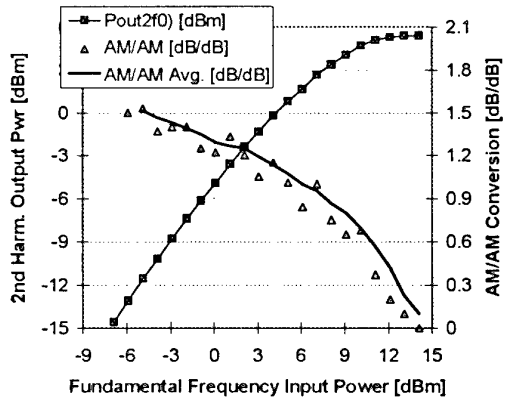

Figure 9. Measured AM/AM noise conversion factors for the 20 GHz D-MESFET frequency doubler

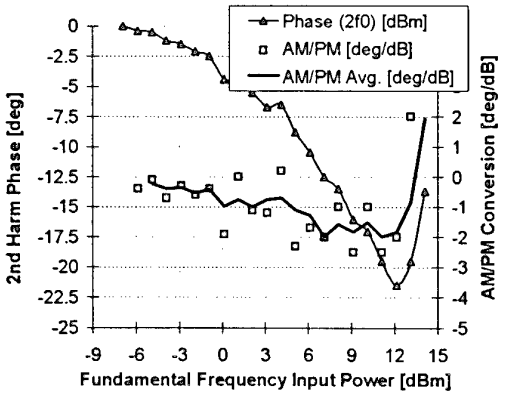

Figure 10. Measured AM/PM noise conversion factors for the 20 GHz D-MESFET frequency doubler.

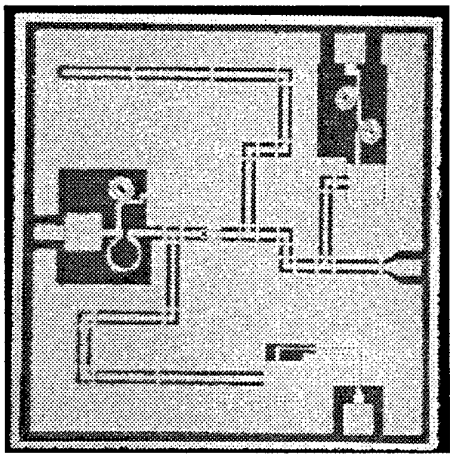

Figure 11. Photograph of the CPW E-HEMT frequency doubler. Chip size is 1.4x1.4 mm^2.

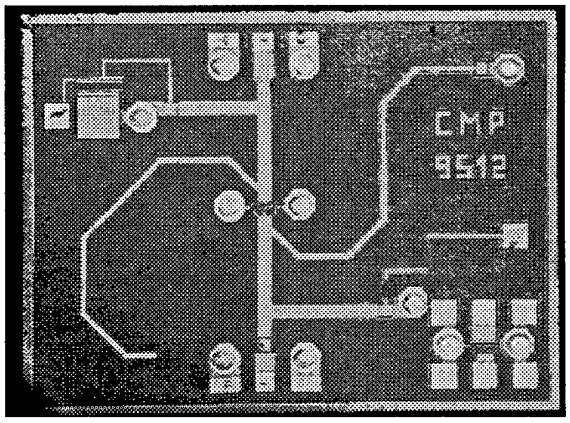

Figure 12. Photograph of the microstrip D-PHEMT frequency doubler. Chip size is 1.4x1.9 mm^2.

A Technique to improve the Power Added Efficiency of Coplanar MMIC Power Amplifiers

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Abstract

A technique for realizing high efficiency operation of miniaturized Coplanar MMIC Power Amplifiers at 1.8 GHz is presented. By using a lumped series resonant circuit tuned to the second harmonic frequency at the output circuit, the Power Added Efficiency is improved by 8 %, without any drastical change in the chip size.

Introduction

To improve the efficiency of microwave power amplifiers, the tuning of the output circuit at the harmonic frequencies (terminating the second harmonic with a short circuit and the third harmonic with an open circuit) is well known [1].

Several techniques to terminate the second harmonic with a short circuit, while keeping optimal matching conditions at the fundamental frequency are published [2], [3], [4]. Many autors use a λ/4-transmission line instead of a large inductor in the output bias network. This technique has some drawbacks. First, the bias networks with a λ/4-transmission line have no broadband properties and second, the λ/4-transmission line occupies too much space at L- and S-Band frequencies, which makes a realization, impossible in miniaturized MMIC Power Amplifiers. Instead of using a λ/4-transmission line in the bias network, it is more convenient in MMIC Power Amplifiers to use an additional lumped series resonant circuit tuned to the second harmonic frequency to reduce the chip size, while keeping the power added efficiency high.

Design Technique

The power-added efficiency of a power amplifier can be brought theoretically to 100%, if the amplifier is biased to Class-B mode and at the same time a harmonic tuning is forseen at the output circuit [1]. The aim of the harmonic tuning is to obtain a rectangular output voltage waveform, which decreases the power dissipation on the transistor together with the half sinewave current waveform of class-B mode.

In this Class-F mode of operation, the optimum load impedance at the fundamental frequency will be matched to 50 Ohms. The second harmonic component will be short circuited to supress the second harmonic component in the voltage waveform, thus approximating the rectangular shape. The third harmonic will be open circuited, which causes a flattening of rectangular voltage waveform. Generally, the small increase in power-added efficiency due to open circuiting of the third harmonic is compensated by the losses of the

additional elements added to the output circuit, so that no remarkable improvement in PAE can be achieved. On the other hand, the increase in PAE due to shortening the second harmonic is great [3].

The harmonic tuning, using lumped elements at the output of a MESFET power amplifier is shown schematically in Fig 1. The output equivalent circuit of the MESFET can be approximatedwith the parallel-circuit of R_{ds} and C_{ds}. The drain-source resistance R_{ds} and the drain-source capacitance C_{ds} are nonlinear functions of the drain-source bias voltage V_{ds} and gate-source bias voltage V_{gs}.

The optimum load conditions for the maximum output power will be first determined by a series of load-pull measurements and simulations. The optimum load at the output of the FET will be matched to 50 Ohms output impedance through an "output matching network" at the fundamental frequency.

The power-added efficiency and output power of this circuit can be inceased by adding a series resonant circuit tuned to the second harmonic frequency. In this case all even harmonic components will be shortend, thus approximating a rectangular output voltage waveform. In order to maintain the matching conditions at fundamental frequency after adding the series resonant circuit, a parallel resonant circuit tuned to the fundamental frequency must be added, which causes open circuiting the fundamental frequency component. The FET's internal output capacitance C_{ds} can be used in this case, without any additional element, as can be seen in Fig.1.

Theoretically, the necessary values of C_S and L_S for this purpose can be expressed in terms of C_{ds}. In Practice, it is more straightforward to choose C_S freely and to optimize L_S to achieve this goal.

Realization

To demonstrate the validity of this technique, two Coplanar MMIC Single-Stage Power Amplifiers at 1.8 GHz were realized (Fig. 2 and 3), by using a multi-finger GaAs MESFET with w_g = 8x40 µm and l_g = 0.5 µm and the technology of [7] as foundary. The chip sizes of the amplifiers are 2.00 x 1.25 mm² and 2.00 x 1.70 mm² respectively. The only difference between these two amplifiers is that, the second one (Class-F Amplifier) has an additional series resonant circuit, which is used to shorten the second harmonic component in order to improve the efficiency. Both amplifiers are biased in Class-AB mode (Drain bias current approximately 10% of I_{dss}) with a low drain voltage of V_{ds} = 3V, in order to reduce the DC losses.

Both amplifiers were simulated with HP-EEsof Libra, by using the nonlinear Curtice Cubic Model for the FET. The coplanar lines, MIM capacitors and the spiral inductors were calculated by using a quasi-static finite difference method [5].

The comparison between the simulated and the measured output powers and power added efficiencies of both amplifiers are illustrated in Fig. 4 and 5. The measured output power of the first amplifier (Class-AB) at an input power of 11 dBm is 16 dBm with a power added efficiency of 38 %. The output power of the second amplifier (Class -F) at the same drive level is 17 dBm with a power added efficiency of 46 %.
A 8% more PAE is achieved in Class-F amplifier compared to the Class-AB case.
The output impedance seen at the output of the FET is shown for Class-AB and for Class-F in Fig. 6 and Fig.7 simultaneously. In Class-AB case , the FET output is nearly matched to 50 Ohms at each harmonic frequency. In Class-F case, the value of the output impedance at the second harmonic frequency is very small, i.e. near to short circuit.

Conclusion

By using a series resonant circuit tuned to the second harmonic frequency, approximately 8% more power added efficiency has been achieved, without any drastical change in the circuit topology and chip size.

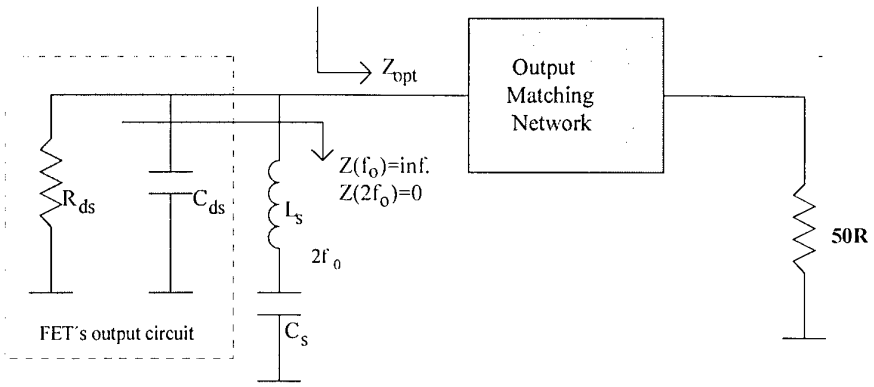

Fig. 1: *Harmonic Tuning at the output of a FET amplifier*

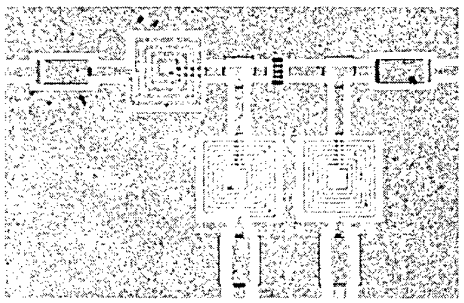

***Fig. 2**: Class-AB Amplifier*

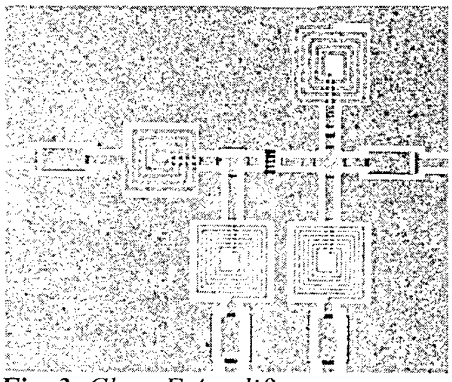

***Fig. 3:** Class-F Amplifier*

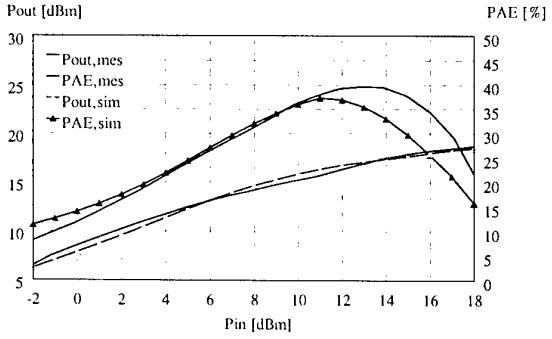

***Fig. 4:** Output Power and PAE (Class-AB)*

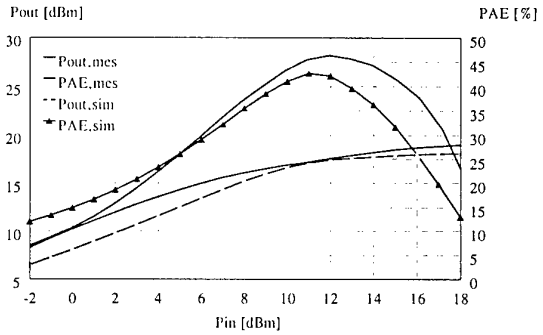

***Fig. 4:** Output Power and PAE (Class-F)*

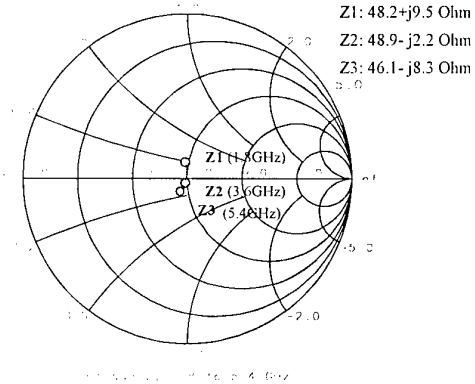

***Fig. 6:** Output Impedance (Class-AB)*

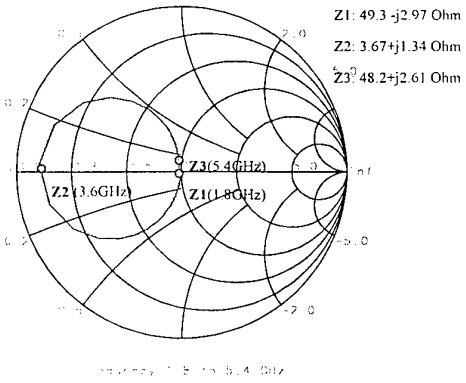

***Fig. 7:** Output Impedance (Class-F)*

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Design and realization of an hybrid X band power amplifier

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Abstract

This paper deals with the design, realisation and measurements of a single stage hybrid X band power amplifier. A design approach based on a linear transistor model has allowed the simplification of the design methodology and the realization of several layouts in a very short time. 575 mW/mm of saturation output power density with a 39 % of power added efficiency has been then obtained at 9.7 GHz. A "reverse simulation" has been carried out by using a non linear model in order to validate the power performances achieved here, and moreover, to establish what improvements could be expected by performing the design with such model.

Technology

The circuits have been realised in microstrip hybrid technology on a 254 µm alumina substrate, with a thin NiCr holding layer and a 4 µm conductive gold layer.

The pseudomorphic HEMT active devices have also been fabricated in our laboratories. Their basic structure consist of a GaAs and InGaAs double quantum well heterostructure FET's epilayer (Figure 1), which allows to reach a good compromise between breakdown voltage, drain current and linearity [1]. Devices used for our circuits have a total gate width of 400 µm, with 8 interdigitated fingers, a drain source spacing of 1.5 µm and a gate length of 0.2 µm. A double air bridge is used to interconnect the source pads (Figure 2).

Amplifier Design

Because of the linear approach, a maximum gain amplifier has been designed and a simple methodology has been applied as follows:

- The active device is modelled by a S parameters box, obtained with on wafer measurements (bias near Class A). It is then forced to be stable (K>1) at the working frequency by the padding method [2]. For all of that a serial NiCr resistance has been added at the drain side. An accurate estimate of gate, drain and source bonding wire values has allowed not only to determinate the value of this resistance but also to avoid frequency shift in circuit response.

- Conjugate impedance matching is then possible. Optimum load and source impedances are obtained by line/stub matching networks in order to reach the maximum available gain.

- Finally, tee bias networks optimised separately are added to the amplifier to provide DC supply but, also, to avoid oscillation at lower frequencies. A NiCr resistive element is placed in parallel with the DC source to attenuate these undesired frequencies. The bias networks can also be optimised to control, partially, the total stability and bandwidth of the circuit.

Once the amplifier design has been finished it is necessary to check the stability conditions at the input and output planes of transistor [2] (Figure 3), that is, to verify:

$$\mathrm{Re}(Z_s + Z_{IN}) > 0 \qquad (1)$$

$$\mathrm{Re}(Z_{OUT} + Z_L) > 0 \qquad (2)$$

By using this procedure several circuits have been designed with different bandwidths. A circuit has also been realised with via-holes for the grounding instead of bonding wires. This allows to avoid bonding uncertainty in the design and a less restricted circuit layout. Some of these layouts are presented in Figure 4.

Amplifier Performances

The hybrid MIC amplifiers have been mounted on a gold-plated test fixture (Figure 5) for scattering parameters and power measurements in 50 Ω termination systems. Some results that have been possible to obtain are now presented.

For the scattering parameters characterisation a TRL calibration is realized with the internal procedure of the

HP85107 vectorial network analyser. Figure 6 shows the good agreement reached between measured and simulated scattering parameters for one of the realised circuits (circuit 1, Figure 4). At 9.9 GHz, a $S_{11} = S_{22} = -16$ dB and a $S_{21} = 8.1$ dB have been measured for this circuit (bias point near Class A, Vds = 3 V, Vgs = -1 V). Better bandwidths have been also obtained for other circuits with lower transmission parameters. And similar results were found for via-holes grounding technology circuits.

For the power measurements a classical scalar power normalisation is realized. Figure 7 presents the power performances achieved for circuit 1, at the same frequency and bias conditions, with our linear design method: 300 mW/mm at 1 dB of compression and 450 mW/mm at saturation of output power, 7.6 dB of linear gain, and a maximum of 20 % power added efficiency (PAE). These results are very satisfactory taking into account the low drain source bias voltage. Lastly, acceptable noise figure (F) has also been measured for this circuit at 9.9 GHz (Table 1).

This circuit has still been measured with short-circuited drain resistance. In this situation, the amplifier still keeps under stable operation and better results are obtained (Figure 8): 23.6 dBm of saturation output power (575 mW/mm) with 39 % of PAE, and 9.3 dB of linear gain. Bias point was Vds = 3.5 V, Vgs = -1.8 V, and F = 9.7 GHz. The output power has also been studied as a function of frequency. A 2.4 GHz 0.5-dB bandwidth has been achieved for a maximum output power of 21.4 dBm (input power equal to 13 dBm).

Even better bandwidth results have been measured with other circuits. A 4 GHz 0.5-dB bandwidth has been obtained with a minimum output power of 19.75 dBm and 8.2 dB of linear gain (Vds = 3 V, Vgs = -1 V).

Power Amplifier Design

Next, the design of a power amplifier based on a non linear model of transistor will be considered in order to evaluate the improvements that we could expect in output power density.

This non linear model has been developed in our laboratory. Figure 9 shows the good fit reached between the DC characteristic simulation and the measure points. Its non linear validity has been checked using a comparison between the obtained power measurements and the "reverse simulation" of circuits achieved using such model and fixing the load impedance with the values determined by the linear approach (Figure 7).

At this point, the non linear approach power amplifier design has been finally carried out using this model. In order to compare results with the linear approach design the same bias conditions (Vds = 3 V; Vgs = -1 V) and frequency (F = 9.9 GHz) have been chosen for input/output impedance optimisation. The simulation results have proved that about 2 dBm of added output power could be expected for this circuit approach (at 1 dB of compression) with respect to the output power obtained for the circuit based on the linear approach (Figure 10).

Conclusion

A single stage hybrid X band power amplifier has been achieved and good power results have been obtained by using only a linear model of transistor for the design and performing a simple methodology. These results have been possible due to the accurate estimate of bonding wire values and the special care taken to prevent low frequency oscillations. The high linearity of the hybrid HEMT active device has also contributed. However, the main result is certainly the improvement of design time compared to classical non linear design approach, and taking into account the satisfactory level of the resulting power performances.

These experimental power results have been validated with a "reverse simulation" carried out using a developed non linear model of transistor. And finally, a non linear approach power amplifier design using this model has been achieved, with 2 dBm of added output power respect of linear approach.

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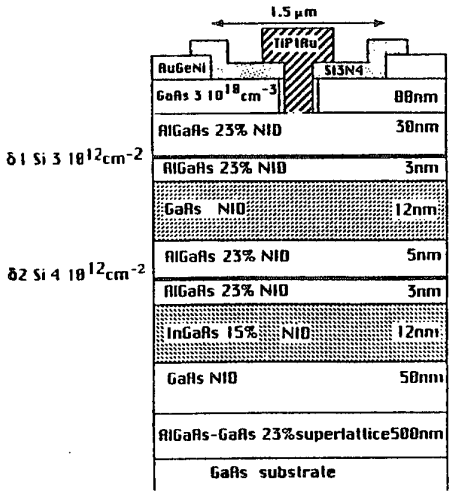

Figure 1. The epilayer used for active devices.

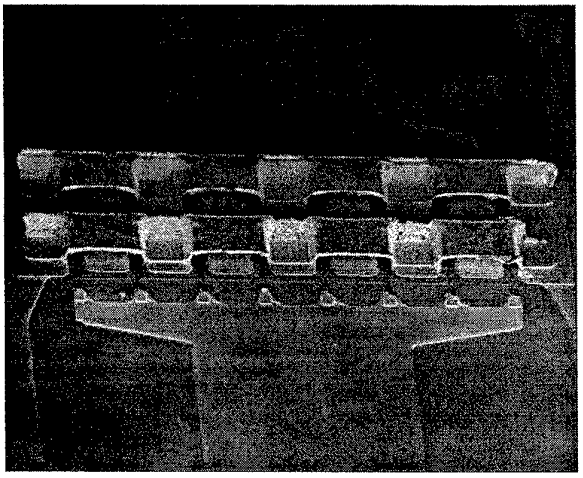

Figure 2. Top of 8*50 µm HEMT device.

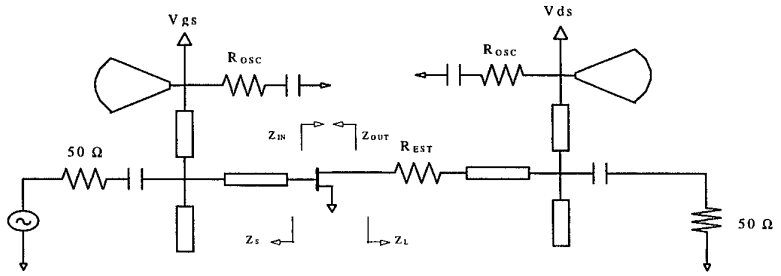

Figure 3. Typical electrical schematic of power amplifier.

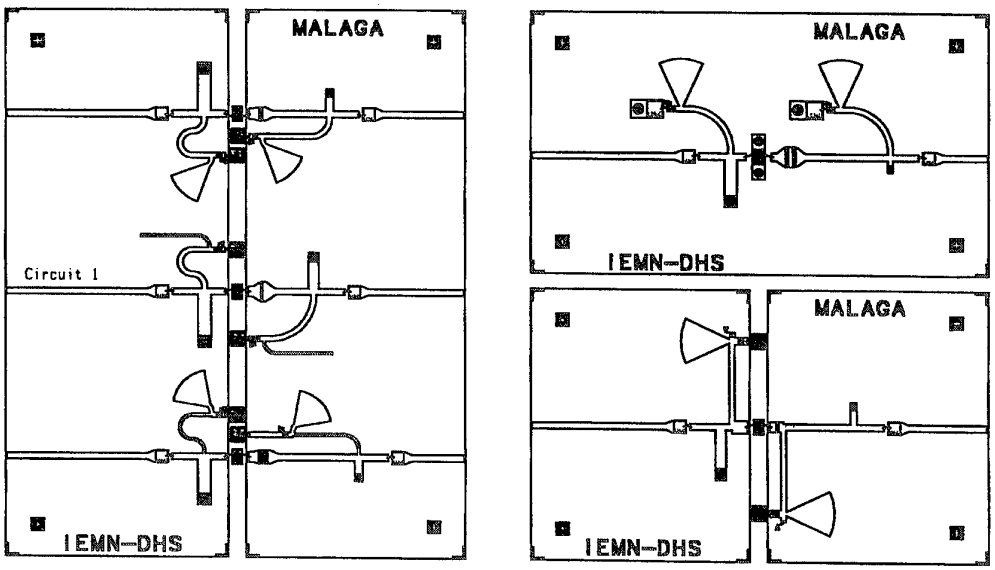

Figure 4. Some realised circuits layouts.

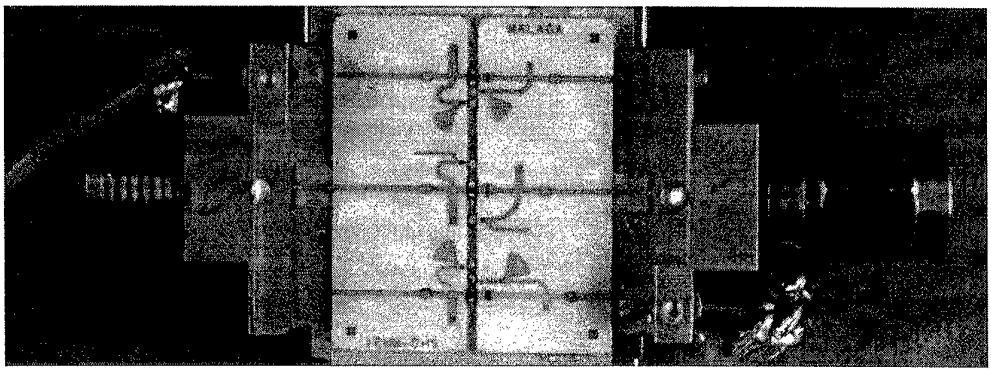

Figure 5. Power amplifier assembly.

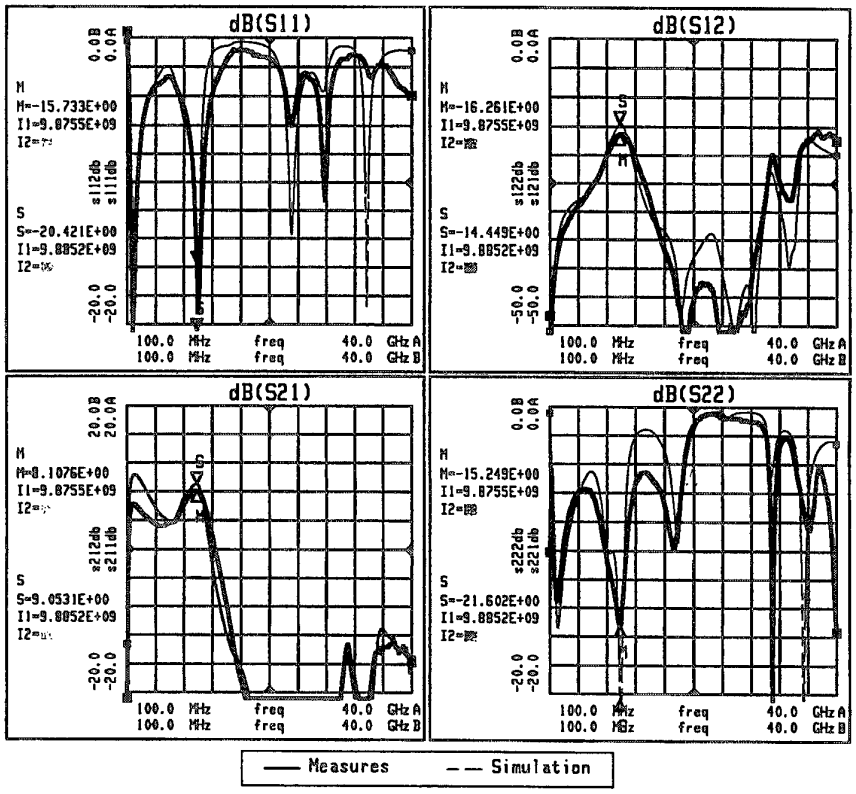

Figure 6. Typical measured and simulated Scattering parameters of the hybrid amplifier.

Vds (v)	Vgs (v)	F (dB)	S_{11} (dB)	S_{12} (dB)	S_{21} (dB)	S_{22} (dB)
3	-1	5.3	-16	-17	8.1	-16
2.2	-2	2.4	-18	-15	8.0	-14

Table 1. Typical noise figure of circuits.

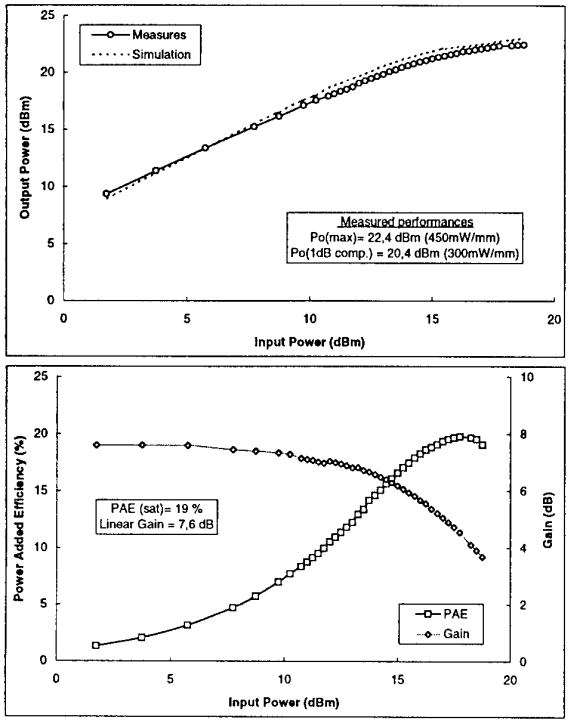

Figure 7. Power performances of the amplifier based on linear approach. Simulation comparison. (9.9 GHz; Vds = 3 V, Vgs = -1 V)

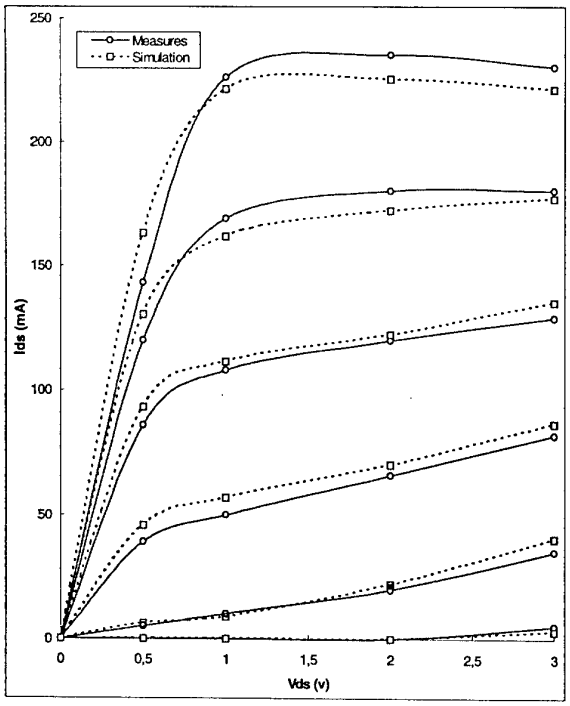

Figure 9. Non Linear model of HEMT device. (DC Ids/Vds characteristic).

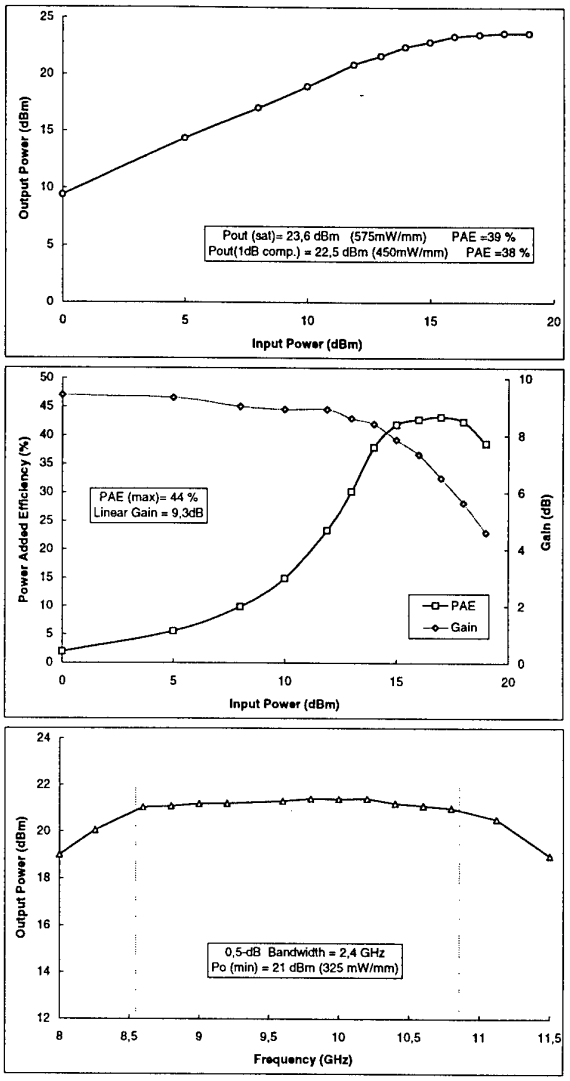

Figure 8. Power performances of the amplifier based on linear approach with short-circuited stabilisation resistance. (9.7 GHz; Vds = 3.5 V, Vgs = -1.8 V).

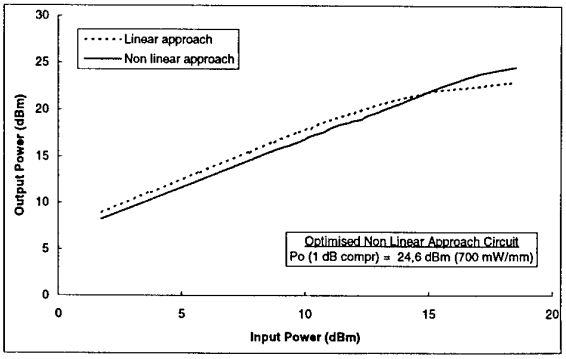

Figure 10. Comparison of power results between linear and non linear approach amplifiers.

Extraction of Linear Small Signal and Nonlinear Large Signal Models for GaAs-FETs and HEMTs Using a Windows Based Software.

Kevni Büyüktas *
Markus Hofbauer **
Rudolf Kohl **

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** Dornier Satellitensysteme GmbH

Abstract

A software called EXTRAKTOR was developed at the Fachhochschule München together with Dornier Satellitensysteme GmbH to extract the linear small signal and nonlinear large signal models for GaAs-FET and HEMT devices [1]. The software contains new algorithms to compute the parasitic elements. The user interface is programmed in Borland Pascal for Windows to provide the most comfortable handling. Only minimum standard hard- and software is required, such as PC386 and Windows 3.1 or higher.

Introduction

Microwave circuit designers rely on circuit modelling more and more. One of the driving forces is the expanding role of monolithic microwave integrated circuits (MMICs). Describing real world microwave transistors by means of models with high accuracy is a non-trivial task. The major problem is to find within a reasonable space of time, and, consequently within a reasonable financial budget, that equivalent circuit configuration which adequately describes the active device. Thus, the primary objective of the work presented in this paper was to develop a software tool, that allows to determine small - and large signal model parameters from a set of measured MESFET or HEMT S-parameters in a very time efficient and comfortable manner using the graphic tools provided by Windows.

Extraction Program

The program EXTRAKTOR is able to extract

- small signal equivalent circuit element values,
- nonlinear model parameters for three commonly used models (Curtice, Curtice-Ettenberg and Statz),
- and, independently of the above mentioned large signal model, two different nonlinear capacity models.

Several numerical and graphical outputs enable the user to control online the instantaneous extraction results and to guide the program manually into certain directions to predict the most probable and accurate results. As an example, two graphical outputs are provided in Figures 1 and 2.

A new and compact algorithm, which considers the parasitic elements shown in Figure 3, was developed for the extraction of the small signal equivalent circuit parameters. The extraction requires only S-parameter measurements at least three different bias points. No DC-measurements need to be performed to troublesome extract the parasitic resistances. No optimization routines are needed to predict the extrinsic inductances and pad capacitances.

That part of EXTRAKTOR which deals with small signal equivalent circuits is divided into the two sections

- single-bias parameter extraction
- and multi-bias parameter extraction.

While the mathematical algorithm is the same for both sections, the user has a lot of possibilities to control and to influence the

program-flow in case of the single-bias-extraction. A S-parameter file generated from measurements at the bias point (Vds, Vgs) of interest forms, together with an unbiased (Vds=0V, Vgs=0V) and a pinched (Vds=0V, Vgs<Vpinch off) S-parameter file, the input to the extraction routine. From the pinched and the unbiased data the parasitic resistances and inductances of the extrinsic FET as well as the pad capacitances of the gate- and drain-contact areas are extracted. Subtracting the parasitic elements from the biased S-parameters, the intrinsic equivalent circuit elements can be computed. For all element values a mean value over frequency is computed. On request each value can be plotted over frequency. The user can now either confirm the computed mean value or override it by a manual input. Afterwards a new extraction using the fixed values can be started.

The multi-bias-extraction computes the intrinsic equivalent circuit elements for several S-parameter sets, measured at different bias points. The extrinsic parasitic element values can either be entered manually via the dialog window shown in Figure 4 or they can be extracted from the two previously mentioned pinched and unbiased S-parameter files. The resulting equivalent circuit element values can be written into a file, which can later on be used as input to the large signal extraction routine.

This multi-bias data file contains the bias dependent small signal equivalent circuit element values (Ids, gds, gm, Cgs, Cgd). The nonlinear extraction algorithm optimizes the parameter values of the previously mentioned nonlinear models to fit the modelled results to the values given in the multi-bias data file. Therefore the user can choose between three algorithms or combine them to get the best fitting between measured and extracted results. The optimization procedures can be performed independently either for the DC-parameters (Ids, gm, gds) or for the bias dependent capacitances (Cgs, Cgd). Figure 5 represent the program dialog for the nonlinear extraction routine.

Conclusion

The applied intrinsic transistor models promise for excellent accuracy for frequencies up to and even higher than 40 GHz. With the currently implemented parasitic element model, high accuracy is even expected for real world transistors. Practical verifications at S- and Ku-Band [1], [2] have demonstrated high agreement between measured and modelled transistor data. This applies for low power, as well as for high power GaAs-FETs.

The graphical Windows user interface makes the EXTRAKTOR program an easy to use tool.

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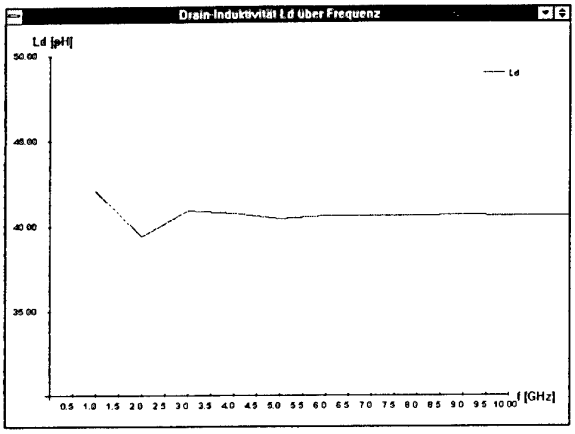

Figure 1: Graphical Display for Small Signal Parameter Extraction

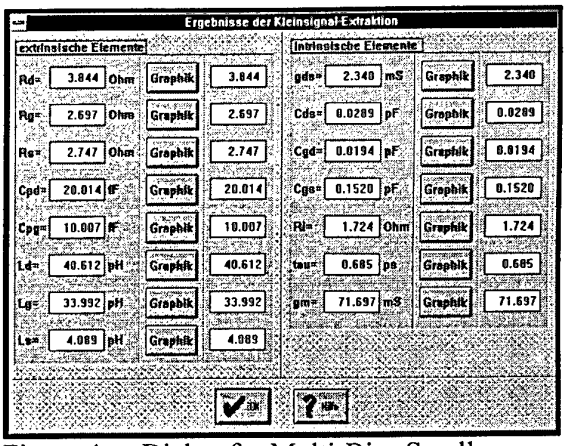

Figure 4: Dialog for Multi-Bias Small Signal Extraction

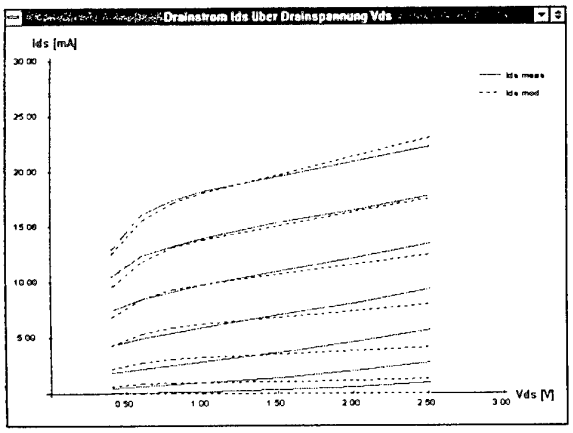

Figure 2: Graphical Display for Large Signal Parameter Extraction

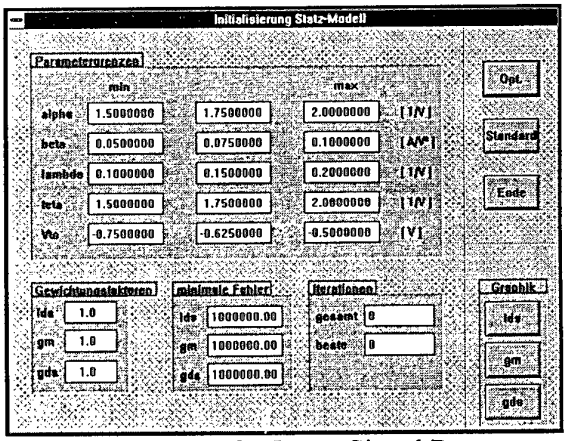

Figure 5: Dialog for Large Signal Parameter Extraction

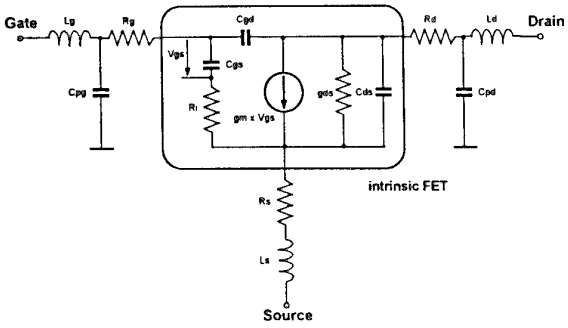

Figure 3: Small Signal Equivalent Circuit Including Parasitics

MTR/2 Correction Method for FET Measurements based on a 4-port Error Model Including Crosstalks

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Abstract

The accuracy of vector network analyzer measurements is enhanced by calibrating the measurement system. If crosstalk is significant, a 16-term error model which usually needs 4 fully-known calibration standards is applied. A new calibration-correction method suitable for reciprocal test fixtures on MMIC wafer probe measurement or microstrip test fixtures has been developed. It covers all crosstalk but only 2.5 full known calibration standards are necessary.

Introduction

The accuracy of a vector network analyzer (VNA) can be enhanced by calibrating the system at the reference planes of measurement. The calibration provides a repeatable representation of the measurement system and should remove most of the system errors. A 16-term error model covers all possible crosstalks and 4 fully-known calibration standards are required for its determination [1]. This demand is rather strong and impractical. An attempt to decrease the number of necessary calibration elements was made in [2]. This calibration needs only one fully-known calibration standard and knowledge of the wavelength. Other calibration elements are determined in the calibration process. However the procedure is only an approximate one and is valid only for minorl crosstalk.

It is the purpose of this paper to present a new calibration procedure which accounts for all of the systematic errors in an open air test fixture such as MMIC wafer probes or a microstrip test fixture. The new method requires only full knowledge of two and half calibration elements without any other limitations.

General theory

The theoretical background for calibration of error 2n-ports is given in [3]. Fig. 1 shows a 4-port error flow graph for a test fixture with crosstalk. Ports 1 and 4 correspond to VNA terminals and ports 2 and 3 represent terminals for the device under test (DUT) or calibration element connection. The error flow graph may be represented in terms of cascading T-parameters as

$$\begin{pmatrix} b_1 \\ b_4 \\ a_1 \\ a_4 \end{pmatrix} = (T).\begin{pmatrix} a_2 \\ a_3 \\ b_2 \\ b_3 \end{pmatrix} \qquad (1)$$

where

$$(T) = \begin{pmatrix} T_1 & T_2 \\ T_3 & T_4 \end{pmatrix} = \begin{pmatrix} T_{11} & T_{12} & T_{13} & T_{14} \\ T_{21} & T_{22} & T_{23} & T_{24} \\ T_{31} & T_{32} & T_{33} & T_{34} \\ T_{41} & T_{42} & T_{43} & T_{44} \end{pmatrix}$$

or in terms of scattering s-parameters as

$$\begin{pmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{33} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{pmatrix} \qquad (2)$$

The measured s^m and the actual s^a s-parameters of the DUT or calibration element are defined as

$$\begin{pmatrix} b_1 \\ b_4 \end{pmatrix} = s^m \cdot \begin{pmatrix} a_1 \\ a_4 \end{pmatrix}, \quad s^m = \begin{pmatrix} s^m_{11} & s^m_{12} \\ s^m_{21} & s^m_{22} \end{pmatrix} \qquad (3)$$

$$\begin{pmatrix} a_2 \\ a_3 \end{pmatrix} = s^m \cdot \begin{pmatrix} b_2 \\ b_3 \end{pmatrix} \quad s^a = \begin{pmatrix} s^a_{11} & s^a_{12} \\ s^a_{21} & s^a_{22} \end{pmatrix} \qquad (4)$$

The equations (1) can be rearranged to the form of (2) and the reciprocity condition $s_{ij} = s_{ji}$ then applied. This yields the relations for T_i submatrixes

$$(T_1) = (T_2).(T_4)^{-1}.(T_3) + \left((T_4)^{-1}\right) \qquad (5)$$

and additional conditions

$$-T_{13}.T_{34} + T_{14}.T_{33} = T_{23}.T_{44} - T_{24}.T_{43} \qquad (6)$$

$$T_{44}.T_{32} - T_{34}.T_{42} = -T_{43}.T_{31} + T_{33}.T_{41} \qquad (7)$$

By applying the definitions of s^m and s^a, (3), (4) to (1), the relations between s^m, s^a and T_i can be obtained, see [1], [3].

$$s^m = (T_1.s^a + T_2).(T_3.s^a + T_4)^{-1} \qquad (8)$$

$$T_1.s^a + T_2 - s^m.T_3.s^a - s^m.T_4 = 0 \qquad (9)$$

$$s^a = (T_1 - s^m.T_3)^{-1}.(s^m.T_4 - T_2) \qquad (10)$$

The "sandwich" matrix product $s^m.T_3.s^a$ in (9) can be broken, applying the Kronecker tensor product $A \otimes B$ of two matrices A and B and "row-stacking" operator RS(A), [3]. For 3 measured calibration standards this yields

$$\begin{aligned} &\left(I \otimes \left(s^{ai}\right)^T\right).RS(T_1) + RS(T_2) \quad - \\ &- \left(s^{mi} \otimes \left(s^{ai}\right)^T\right).RS(T_3) \quad - \\ &- \left(s^{mi} \otimes I\right).RS(T_4) = |0| \end{aligned} \qquad (11)$$

i=1,2,3 and I is a unit matrix.

The advantage of (11) is that it forms a set of linear equations for four column vector $RS(T_i)$, i=1, .. ,4. Seeing that (11) is a homogeneous system, three fully-known measured calibration standards are sufficient to find a solution for three $RS(T_i)$. One $RS(T_i)$ may be chosen arbitrarily, [3]. A proper choice such as T_4=I simplifies the solution of (11). Further simplification is possible with proper calibration standards. For example fully-known match-match and thru connection two-ports can be considered. The third calibration standard such as open-open or short-short does not need to be fully-known. The conditions of its symmetry and zero transmission are sufficient. Its $s^a_{11} = s^a_{22}$ are determined in the process of calibration if (6) or (7) is used.

By applying these conditions to (11), the three unknowns T_1, T_2, T_3 can be determined in a laborious but straightforward way.

Once determined, T_1, T_2, T_3, T_4 can be used in (10) to determine corrected (actual) s-parameters from measured ones.

Conclusion

A new MTR/2 (Match, Thru,1/2 of Reflect) 16-term calibration-correction method for VNA measurements has been theoretically developed. The method requires only two fully-known calibration two-ports such as match-match and thru connection. The third reflective calibration element must have zero transmission. Its symmetrical reflection is determined in the process of calibration.

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Microwave Transistor Data: Catalogue vs. Measured.

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Abstract

An experimental study of the influence of the mounting on microwave packaged transistor parameters was performed. A Hewlett Packard FET ATF 13284 and a HEMPT ATF 35376 were used for the study. Their scattering parameters in the 2 - 18 GHz frequency band were measured in different test fixtures in a coplanar waveguide (CPW), and microstrip line structures. Measurement correction methods were applied. Basic transistor parameters were calculated and compared.

Measurement conditions

Scattering parameters were measured by a HP 8410-PC Controlling system and a Wiltron vector network analyzer. The first system is a PC upgrade of the HP 8410 vector network analyzer developed by the authors, which enables automatic measurement with applications of standard calibration and correction methods for coaxial, waveguide and microstrip transmission lines [1]. Fig.1 shows packages of the two tested transistors.

Two types of test fixtures were used for measurement. The first, the microstrip test fixture, was developed by the authors. It is a universal test fixture which can be set up for different types of transistor packages. The set-ups for 2 mm and 3 mm packages were used with 50Ω microstrip lines on a 0.635 mm thick alumina substrate. The measurement reference planes were at the edges of the substrates separated by a 2.2 mm resp. 3.2 mm wide slot where transistors were put in. Calibrations were made in the measurement reference planes with a microstrip sliding load, open and short at the edges of the substrates and microstrip thru line. The arrows in Fig. 1 show the position of the measurement reference planes.

A Wiltron universal test fixture and a Wiltron vector network analyzer were used for measurement in the 50 Ω CPW structure on a soft substrate with ε_r = 10.8. The LLR calibration method was applied. The dashed lines in Fig. 1 mark the positions of the reference planes at the edge of the transistor package.

Measurement results

ATF 13284 was measured in a 2 mm and 3 mm test fixture set-up. The reference planes of measurement and the ground connections of the source were at the edge of the package in the case of the 2 mm set-up. In the 3 mm test fixture set-up, parts of the package tab terminals, 0.5 mm in length, between the edge of the package and the reference planes of the measurement, respectively, the ground connections of the source, were connected.

Corresponding measured s-parameters for the 2 mm set up, see Fig.2, are at first glance very similar to the catalogue parameters. However, basic transistor parameters like the stability

factor, the maximum achievable power gain or the maximum stable gain show a slight degradation, see Tab.1.

Fig. 2 also shows that although the s-parameter traces corresponding to the 3 mm set up are still quite similar to the catalogue ones, the basic transistor parameters are strongly influenced. The transistor is not stable even at the highest frequency of the band.

ATF 35376 was measured in the 2 mm and 3 mm microstrip test fixture set-ups and in the coplanar waveguide test fixture. In the 2 mm test fixture set-ups a part of the package tab terminals 0.2 mm in length were connected between the package and the measurement reference planes at the edges of the substrates, resp. between the package and the source ground connections. The corresponding length of the package tab terminals for the 3 mm test fixture set-up was 0.7 mm. In the case of the coplanar test fixture the reference measurement planes and the source ground connections were at the edge of the package, see the dashed line in Fig. 1.

Fig. 3 shows a significant change in s-parameters for the 2 mm test fixture set-up and a dramatic change for the 3 mm set up. The basic transistor parameters are also strongly influenced, see Tab. 2.

Surprising results were obtained with the coplanar test fixture. (This measurement was performed only in the 8-18 GHz frequency band!) In spite of zero length of the package tab terminals between the edge of the package and the measurement reference plane, resp. the source ground connections, the s-parameters were strongly different from the catalogue parameters, while the basic transistor parameters presented negligible changes. The s-parameter changes were probably caused by the substrate under the transistor, which resulted in the increasing parasitics of the package.

Conclusion

Strong influence of the mounting on microwave packaged transistor parameters was demonstrated. In the microstrip structure and frequencies above several GHz, even as small a length as 0.2 mm of the package tab terminals significantly changes the s-parameters of the transistor and degrades its basic parameters.

The mounting in the CPW structure significantly influences transistor s-parameters, even if zero package tab terminal length is used.

These quantitative results are very important for microwave designers. They imply that even in the era of CAD modelling the experimental verification of catalogue transistor data in the structure used for a design still remains essential.

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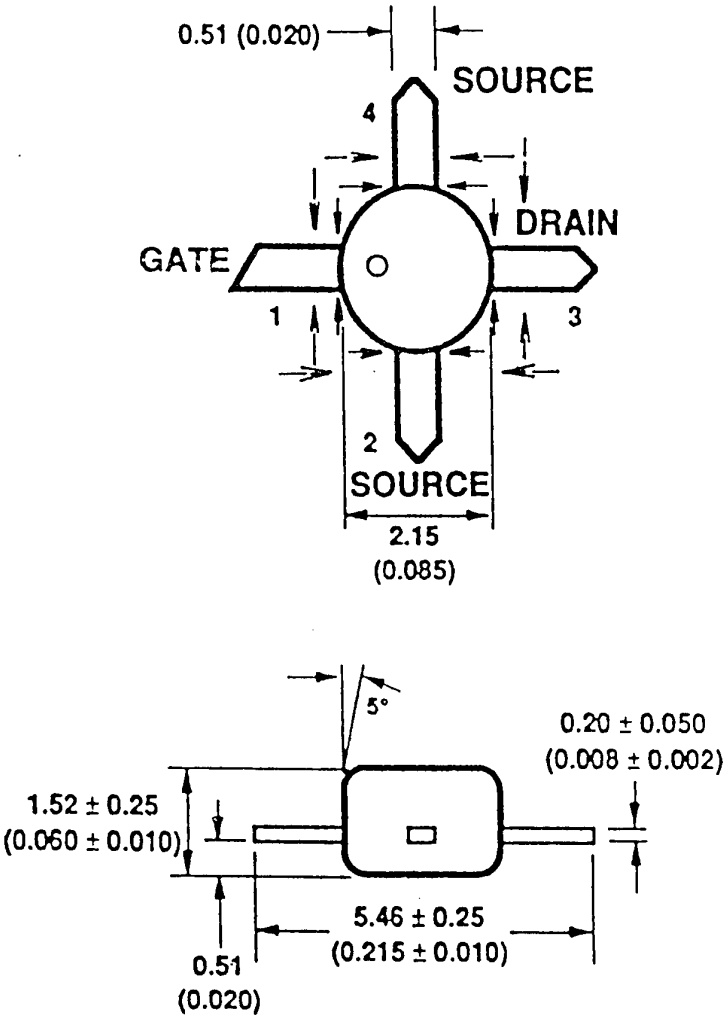
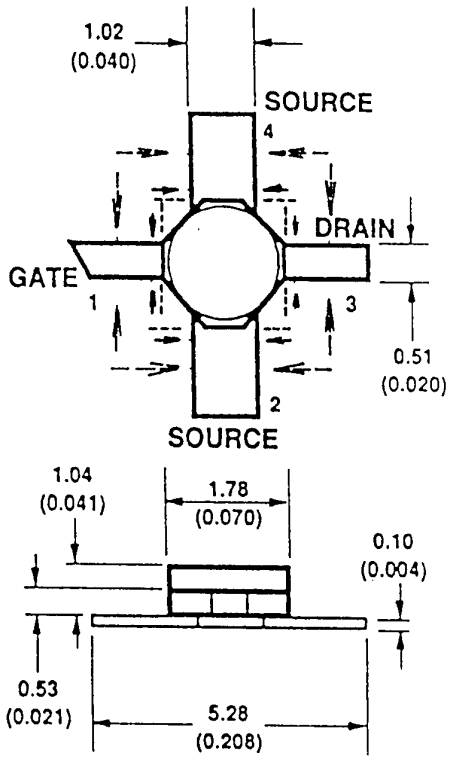
ATF 13284



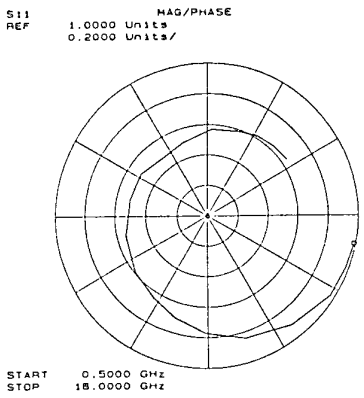
ATF 35376



DIMENSIONS ARE IN MILLIMETERS (INCHES)

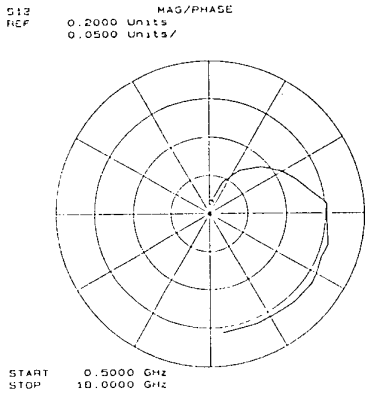
Fig. 1. Positions of the measurement reference planes.

ATF 13284 2.5V 20 mA
diameter of the package 2 mm

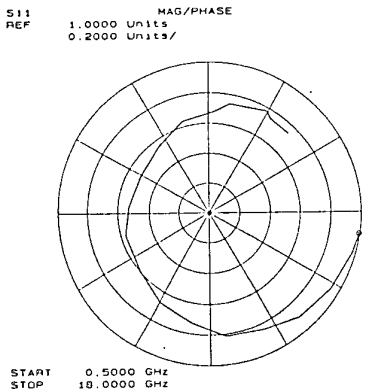


catalogue data

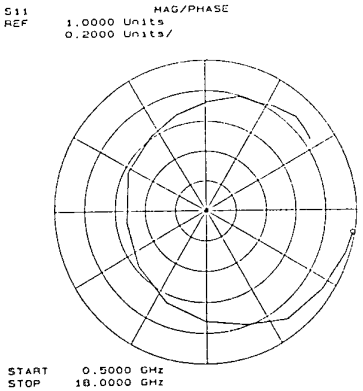
ATF 13284 2.5V 20 mA
diameter of the package 2 mm



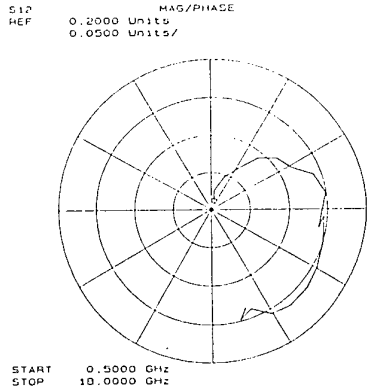
catalogue data



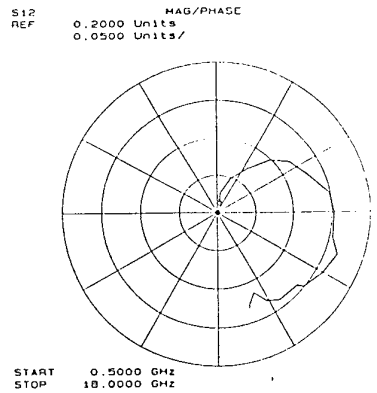
measured data in 2 mm
microstrip test fixture



measured data in 3 mm
microstrip test fixture



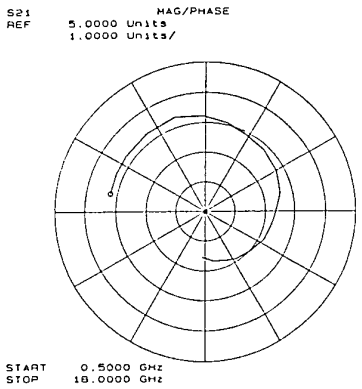
measured data in 2 mm
microstrip test fixture



measured data in 3 mm
microstrip test fixture

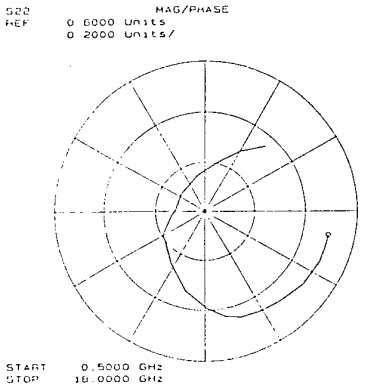
Fig. 2a. The s-parameters of ATF 13284.

ATF 13284 2.5V 20 mA
diameter of the package 2 mm



catalogue data

ATF 13284 2.5V 20 mA
diameter of the package 2 mm



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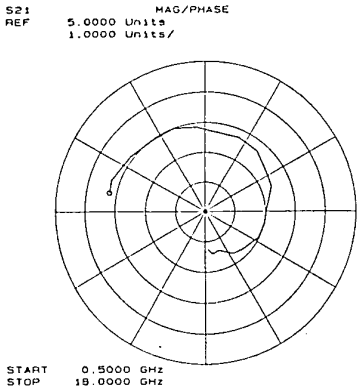
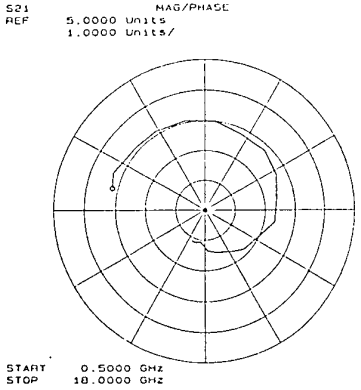
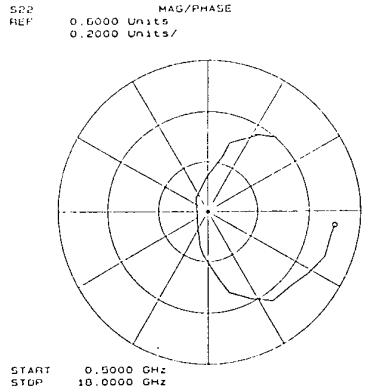


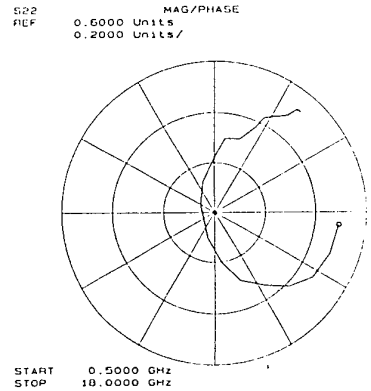
measured data in 2 mm
microstrip test fixture



measured data in 3 mm
microstrip test fixture



measured data in 2 mm
microstrip test fixture



measured data in 3 mm
microstrip test fixture

Fig. 2b. The s-parameters of ATF 13284.

ATF 13284 2.5V 20 mA

Stability factor

freq.	catalogue	CPW	microstrip 2 mm	microstrip 3 mm
2	0,23		0,41	0,49
3	0,39		0,49	0,52
4	0,51		0,59	0,69
5	0,61		0,59	0,81
6	0,69		0,77	0,9
7	0,78		0,79	0,96
8	0,8		0,92	1,05
9	0,89		1,12	1,07
10	0,96		1,15	0,99
11	1,07		1,3	1,02
12	1,17		1,23	0,97
13	1,16		1,08	0,94
14	1,14		1,07	0,93
15	1,19		0,93	0,81
16	1,22		1,08	0,87
17	1,23		1,01	0,76
18	1,23		1,31	0,78

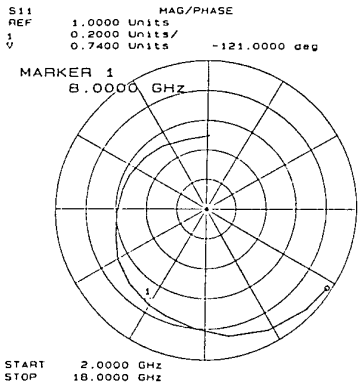
ATF 13284 2.5V 20 mA

Gamax [dB], Gsmax [dB]

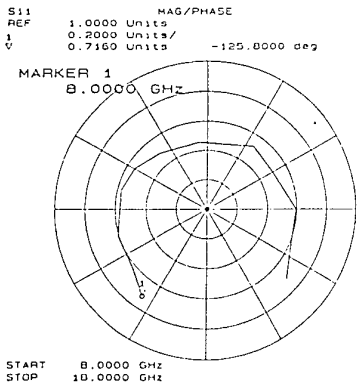
freq.	catalogue	CPW	microstrip 2 mm	microstrip 3 mm
2	18,6		18,11	18
3	16,8		16,57	16,46
4	15,63		15,13	14,94
5	14,72		14,19	14,09
6	14,06		13,64	13,37
7	13,46		12,93	12,78
8	12,7		12,54	10,99
9	12,53		10,22	10,33
10	12,12		9,74	11,48
11	10,13		8,08	10,16
12	9,04		8,25	10,85
13	8,88		9,17	10,66
14	8,74		8,78	10,18
15	8,14		8,52	10,13
16	7,76		8,21	9,64
17	7,42		9,11	9,39
18	6,97		6,29	9,28

Tab. 1. Basic parameters of ATF 13284 in different test fixtures.

ATF 35376 1.5V 20 mA
diameter of the package 1.8 mm

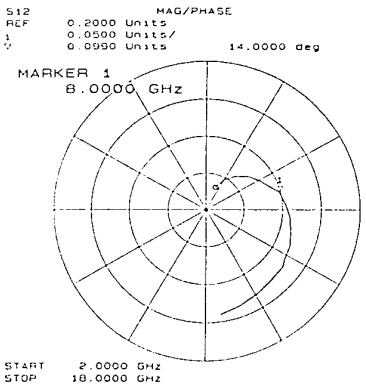


catalogue data

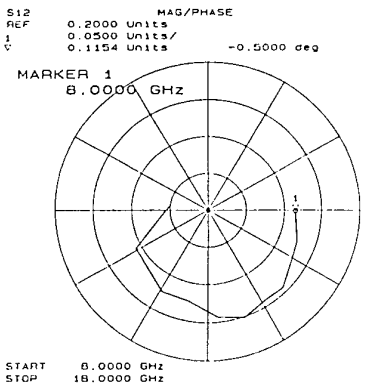


measured data in
CPW test fixture

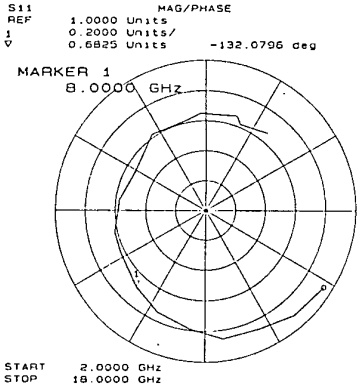
ATF 35376 1.5V 20 mA
diameter of the package 1.8 mm



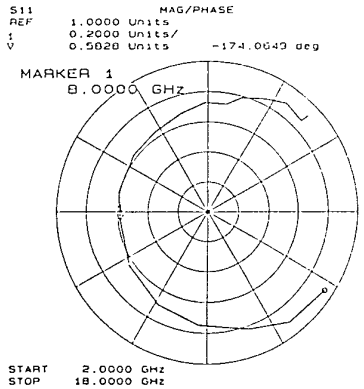
catalogue data



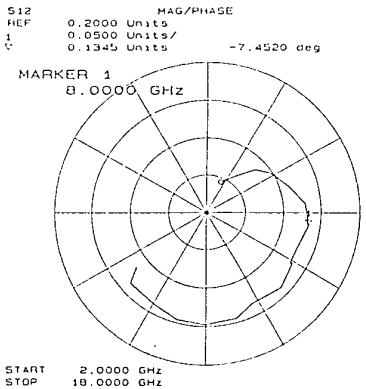
measured data in
CPW test fixture



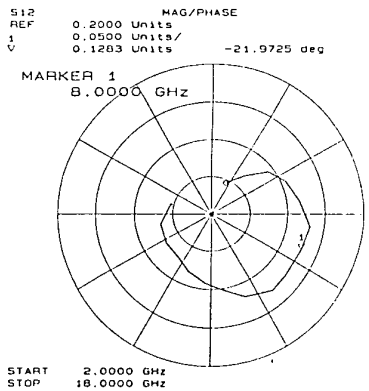
measured data in 2 mm
microstrip test fixture



measured data in 3 mm
microstrip test fixture



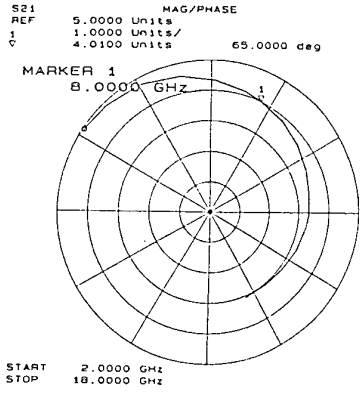
measured data in 2 mm
microstrip test fixture



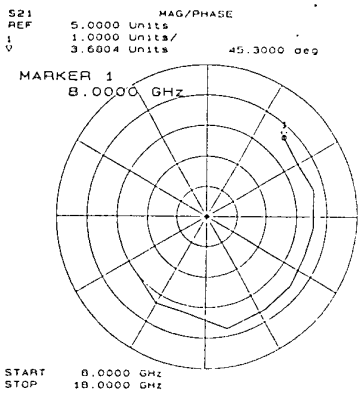
measured data in 3 mm
microstrip test fixture

Fig. 3a. The s-parameters of ATF 35376.

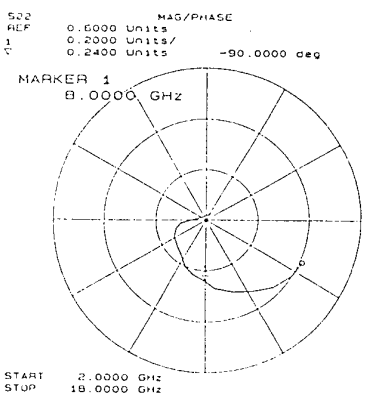
ATF 35376 1.5V 20 mA
diameter of the package 1.8 mm



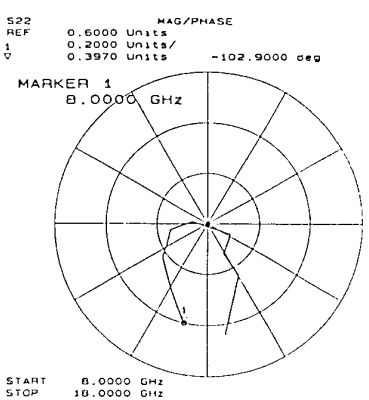
catalogue data



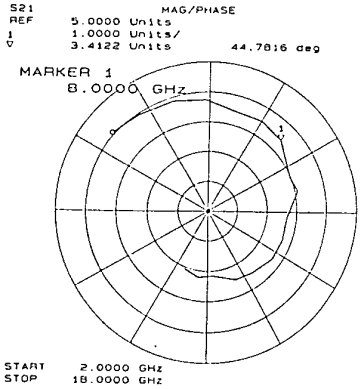
measured data in
CPW test fixture



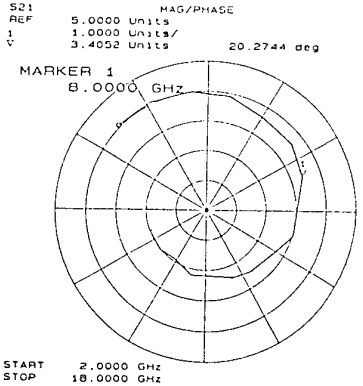
catalogue data



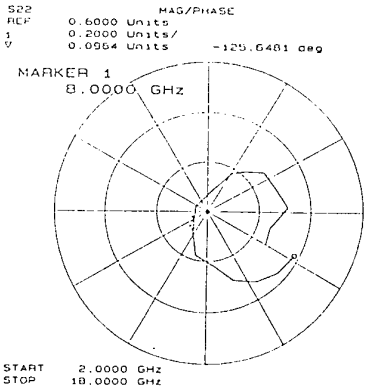
measured data in
CPW test fixture



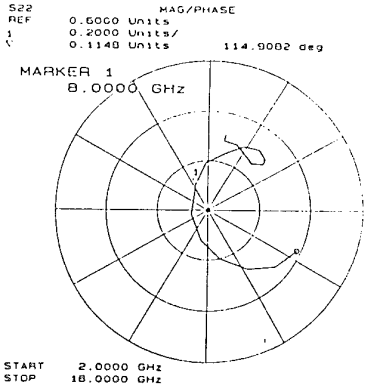
measured data in 2 mm
microstrip test fixture



measured data in 3 mm
microstrip test fixture



measured data in 2 mm
microstrip test fixture



measured data in 3 mm
microstrip test fixture

Fig. 3b. The s-parameters of ATF 35376.

ATF 35376 1.5V 20 mA

Stability factor

freq.	catalogue	CPW	microstrip 2 mm	microstrip 3 mm
2	0,22		0,39	0,42
3	0,27		0,42	0,45
4	0,37		0,5	0,62
5	0,48		0,5	0,71
6	0,6		0,64	0,78
7	0,66		0,67	0,83
8	0,68	0,68	0,78	0,93
9	0,73	0,87	0,96	0,93
10	0,8	0,87	0,94	0,9
11	0,9	0,85	1,05	0,97
12	0,94	0,9	1,1	0,99
13	0,96	0,93	0,92	0,98
14	0,97	0,99	0,93	1,15
15	1,02	1,05	0,88	1,01
16	1,08	1,18	0,96	0,9
17	1,12	1,16	1,05	0,69
18	1,08	1,65	1,19	0,86

ATF 35376 1.5V 20 mA

Gamax [dB], Gsmax [dB]

freq.	catalogue	CPW	microstrip 2 mm	microstrip 3 mm
2	21,76		19,59	19,48
3	20,16		18,09	17,93
4	19		16,55	16,38
5	17,97		15,8	15,63
6	17,24		14,93	14,91
7	16,58		14,34	14,38
8	16,08	15,04	14,04	14,24
9	15,71	14,48	13,69	13,78
10	15,29	13,74	14,57	13,71
11	14,91	13,95	11,52	13,58
12	14,52	13,94	11,13	13,96
13	14,34	13,81	12,7	14,15
14	14,16	14,07	12,34	11,95
15	13,09	13,5	12,27	14,25
16	12,07	11,6	11,95	14,4
17	11,47	12,5	10,7	14,8
18	11,63	12,98	9,79	15,71

Tab. 2. Basic parameters of ATF 35376 in different test fixtures.

Noise and small-signal characterization of GaAs FETs in the multistate radiometer system

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Abstract - The paper presents an application of a novel noise approach, called the multistate radiometry [7], to simultaneous noise and small-signal characterization of microwave transistors. This is achieved using the cold source technique and a multistate radiometer (MSR) [8]. The MSR, calibrated first using several impedance and noise temperature standards, measures both the noise temperatures and the reflection coefficients of the device connected to its port. This enables one to determine the transistor scattering and noise parameters. Due to the general scheme of this technique, the measurements can be carried out automatically in a broadband frequency range.

Introduction

There is a constant interest in measuring noise characteristics of transistors and microwave monolithic integrated circuits (MMICs), particularly those to be applied in front ends of RF and microwave receivers. The noise characterization is typically understood as the determination the four noise parameters of two-port devices. Today for high volume manufacturing of microwave devices, such a characterization needs to be realized automatically in broad frequency range like signal characterization performed by modern vector network analyzers. In reality, however, the noise measurements remain still an awkward job that takes a lot of time and requires high skills. This is certainly because the noise measurement techniques and technology have not been evolving much for many years.

The noise metrology at RF and microwaves is commonly based on total power radiometer as the instrument measuring the spectral power density of device noise. The measurements are, unfortunately, obscured by the internal noise of the receiver circuitry and the mismatch at the radiometer input. To make the contribution of the internal noise be independent on the impedance of the device under test (DUT), a ferrite isolator is commonly put at the radiometer input [1]. Once the isolation is perfect, this contribution can be easily subtracted from the measurements. Although this solution provides today highest measurement accuracy, standards laboratories benefit from [1], it can not be readily exploited in very broad frequency range, due to narrowband properties of the ferrite devices.

Since the radiometer measures the delivered noise power instead of the available one, the mismatch has to be known to arrive at the noise temperature. This vital problem can be alleviated a bit with the circulator technique [2], which applies noise injection from the matched arm of the circulator to determine scalar reflection coefficient of the DUT and thus evaluate the mismatch. This technique was utilized directly for the noise characterization of Schottky barrier diodes [3]. Unfortunately, measurement errors of the circulator technique might be serious, unless the circulator is ideal and the noise source for the injection perfectly matched. Since these requirements cannot be met over a broad frequency range, this technique does not fully meet requirements of automatic measurement technology.

In consequence, unisolated total power radiometer is now the only means capable of very broadband noise characterization. Its measurements must be, however, corrected for the input mismatch and the noise contribution of the receiver. Since some small-signal parameters of the DUT and the radiometer are required for that purpose, most of the contemporary noise measurement systems is equipped with a vector reflectometer [1] or network analyzer [4]. This

unsophisticated solution entails, unfortunately, higher expenses for both the system instrumentation and its exploitation that is not intensive enough, because the noise and signal measuring instrumentation can not operate concurrently. This, of course, increases costs of device testing, which are of high importance to semiconductor manufacturers. Moreover, measuring highly nonlinear devices may be difficult, because the signal stimulus have to be reduced much to avoid errors caused by overdriving.

The problems, mentioned above, might be solved alternatively using only noise measuring instrumentation, since noise measurements comprise also the information on both the radiometer and the DUT small-signal parameters [5],[6], i.e. the impedance of a one-port or the scattering parameters of a two-port. There is a method that utilizes more intensively noise figure measurements to determine both the noise and scattering parameters of microwave transistors [6]. For this purpose, it employs a typical source-pull technique and a specific measurement system whose parameters are being changed with a step attenuator to evaluate the DUT available power gain. Unfortunately, this technique requires perfect ferrite isolation of the attenuator and must by supported by an additional vector reflectometer measuring the output reflection coefficient of the DUT.

A breakthrough in the current noise metrology may be initiated up with an original noise measurement technique introduced very recently in [7]-[9]. According to [7], the measurement tasks realized with a total power radiometer can be split into two complementary categories; the noise unterminating and the noise de-embedding. The former one means the characterization of the radiometer response using several known impedance and noise temperature standards, while the last one indicates the characterization of an unknown one-port device on the basis of the noise powers measured consecutively with several known radiometers. This observation has led to a fresh idea of the multistate total power radiometer, as an applicable instrument to perform such measurements. In consequence, the novel noise approach, based on this instrument and the techniques of unterminating and de-embedding, has gained the name of the multistate radiometry. It has been implemented in the first multistate radiometer (MSR) built up at the Warsaw University of Technology (WUT) [8]. Through processing only noise level measurements, this new tool is not only capable of gauging the noise temperature, but for the first time yields also the complex reflection coefficient of one-port microwave devices. Recently, its usefulness to noise characterization of microwawe transistors has been proved [15].

This paper shows some fresh applications of the MSR to characterization of low-noise GaAs FETs in broad frequency range. The design of the MSR and the principle of its operation along with the techniques of the MSR calibration and the accuracy enhancement are presented too. Some aspects and conclusions related to potential applications of the multistate radiometry in semiconductor metrology are discussed.

Multistate radiometer

The multistate radiometer (MSR) has been based on a total power radiometer which was built in house to realize high accuracy noise measurements. Its heart is a superheterodyne microwave receiver that tuned from 0.1 to 4.3 GHz gauges the noise in two 1 MHz sidebands. These sidebands can be placed very close each other by proper adjustment of the IF frequency from 1 to 30 MHz. The noise power levels are measured in the receiver with the uncertainty ± 0.01 dB, thanks to a microprocessor control of high precision step attenuators and processing the output signal from a true square-law detector [10].

The injection of correlated noise waves at the input, proposed in [7], has been implemented to achieve multistate operation of the radiometer. To this end the radiometer was equipped with a noise injection circuit inserted between the radiometer input and the DUT, as shown in Fig.1. This circuit, composed of a directional coupler, a switched noise source and a multistate termination provides different noise excitation conditions for the DUT [8].

The operation of the MSR can be easily explained if the coupler is assumed to be ideal, and the noise source as well as the radiometer are perfectly matched ($\Gamma_i=0$). With the noise source on there are two different paths by which the traveling noise waves reach the radiometer input. The first wave is transmitted to the multistate termination through the coupled line and reflected back appears at the output of the main coupler line. The other wave, injected into the main line due to coupling, travels towards the DUT and then is reflected back. Thus the both mutually correlated noise waves interfere at the radiometer input and contribute to the total noise power gauged at the radiometer output. Considering

other uncorrelated noise contributions from the DUT and the radiometer, the power level indication is [8]:

$$p \sim T_i |\Gamma + \Gamma_l|^2 + (T + T_{er})(1 - |\Gamma|^2) \quad (1)$$

where T_i is the temperature of the noise injected into the measurement channel, Γ_l stands for the reflection coefficient of the multistate termination, T_{er} denotes the effective input noise temperature of the radiometer, while T and Γ are the noise temperature and the reflection coefficient of the DUT, respectively.

Due to the interference of the correlated noise waves, the MSR can be classified as an interferometric instrument, like a six-port [11] or multistate reflectometer [12]. This fundamental analogy, shown first in [7], has several implications for the operation of the instrument. It can be easily seen that once T_i dominates much over T and T_{er}, (1) portrays a paraboloid over the complex Γ plane with its minimum at the point $\Gamma \approx -\Gamma_l$. Since this interpretation adheres well to that one known from the six-port theory, the position of the minimum can be called as the q-point. Following this analogy further on, it is well known from [11] that the distribution of the q-points on the Γ plane predetermines the measurement accuracy of the interferometric instruments. Thus, to provide broadband operation of the MSR, distributions of the reflection coefficient Γ_l, realized by switching the multistate termination, were optimized in the frequency range from 0.4 to 5.0 GHz [13].

The determination of the DUT reflection coefficient can be done in the same manner as for the other interferometric instruments, i.e. from an intersection of at least three circles, each being the locus of the constant noise power measured in a different state with the noise source on. In consequence, the multistate radiometry can be treated as an extension of the interferometric technique for very low signal excitations [7]. The specific features of the MSR is, however, the noise excitation of the measurement circuit and the fourth measurement state with the noise source switched off, which is necessary to determine the DUT noise temperature.

Calibration of the multistate radiometer

The technique for the complete characterization of a total power radiometer using a set of impedance and noise temperature standards [9] can be easily adapted to the calibration of the MSR. Generally, the response of the instrument in a particular state can be represented by seven real parameters; three describing the gain and four the noise [7,9]. They can be determined using the general 8-term linear model that allow to write down a radiometer readout in the following form [9]:

$$\begin{bmatrix} p q & -q \end{bmatrix} \cdot \begin{bmatrix} \beta_g \\ \beta_n \end{bmatrix} = T_{ef} \quad (2)$$

where q is a row vector comprising known coefficients:

$$q_1 = 1 - |\Gamma|^2 \qquad q_2 = 1 + |\Gamma|^2$$
$$q_3 = 2\,\mathrm{Re}\Gamma \qquad q_4 = 2\,\mathrm{Im}\Gamma ,$$

$T_{ef} = Tq_1$ denotes the effective noise temperature of a standard applied and β_g and β_n are unknown vectors containing the gain and noise parameters of the receiver [7,9], respectively.

Although seven known impedance standards with one being of a distinctive noise temperature is sufficient for the calibration [7,9], more standards allow reducing effects of random errors on the parameters to be identified. This can be easily fulfilled using the cold-source technique [4],[5] with a set of passive impedance standards at room temperature, named the 'cold' ones, and only one 'hot' noise standard, being typically a switched-on semiconductor noise source.

In general, an overdetermined set of $N>7$ equations (2) is acquired from the calibration [9]:

$$X \cdot \beta = y \quad (3)$$

where the matrix X is composed of the coefficients defined by (2), $\beta^T = \begin{bmatrix} \beta_g^T & \beta_n^T \end{bmatrix}$ is the vector of the unknown parameters and $y = [T_{ef1}\ T_{ef2}\ \ldots\ T_{efN}]^T$. It can be solved for β parameters using a least squares method with the constraint accounting for an inherent relationship between elements of vector β_g [7,9]:

$$\beta_{g2}^2 - \beta_{g1}^2 - \beta_{g3}^2 - \beta_{g4}^2 = \beta_g^T D_g \beta_g = 0 \quad (4)$$

where the matrix $D_g = \mathrm{diag}\{-1, 1, -1, -1\}$. The solution was described in [9].

By successive repeating this procedure for all the states used by the MSR, relevant sets of seven calibration parameters are procured. Since at least four such states are necessary to realize the MSR measurement [7], the minimum of 28 parameters enables one to de-embed a DUT.

Device de-embedding

The de-embedding of the three unknown parameters of the DUT can be also based on a linear model derived from (2) [9]:

$$\boldsymbol{u}\,\beta_d = v \tag{5}$$

where the vector $\beta_d = \left[T_{ef} \;\; \mathrm{Re}\Gamma \;\; \mathrm{Im}\Gamma \;\; |\Gamma|^2\right]^T$ comprises the DUT parameters, while the row vector $\boldsymbol{u}$ and the variable v are defined by the indication p and the parameters β:

$u_1 = 1 \qquad u_2 = -2(p\beta_{g3} - \beta_{n3})$

$u_3 = -2(p\beta_{g4} - \beta_{n4})$

$u_4 = p(\beta_{g1} - \beta_{g2}) - \beta_{n1} + \beta_{n2}$

$v = p(\beta_{g1} + \beta_{g2}) - \beta_{n1} - \beta_{n2}$.

Since the vector β_d comprises four components instead of three, one of them may be expressed by the others

$$\beta_{d4} - \beta_{d2}^2 - \beta_{d3}^2 = \beta_d^T \boldsymbol{D}_d \beta_d + \beta_d^T \boldsymbol{d}_d = 0 \tag{6}$$

where

$\boldsymbol{D}_d = \mathrm{diag}\{0, -1, -1, 0\}$ and $\boldsymbol{d}_d = [0 \;\; 0 \;\; 0 \;\; 1]^T$.

Although four power readouts taken in different radiometer states is sufficient to unambiguously determine the parameters of DUT [7], more states help to reduce the effects of random measurement errors. Generally for $M \geq 4$ states, one gets the matrix equation:

$$\boldsymbol{U}\,\beta_d = v \tag{7}$$

where $\boldsymbol{U}$ is composed of the row vectors $\boldsymbol{u}$ and $v = [v_1 \;\; v_2 \;\; \ldots \;\; v_M]^T$. This equation can be solved for β_d using a constrained least squares optimization based on the following objective function:

$$L(\beta_d, \lambda) = (v - \boldsymbol{U}\beta_d)^T \boldsymbol{W} (v - \boldsymbol{U}\beta_d) - \lambda \beta_d{}^T \boldsymbol{D}_d \beta_d - \lambda \beta_d{}^T \boldsymbol{d}_d \tag{8}$$

where $\boldsymbol{W}$ denotes a diagonal weight matrix and λ is the Lagrangian multiplier. The calculations may be carried out in a similar way as presented in [9].

Characterization of two-ports with the MSR

The multistate radiometry may be easily applied to the noise and small-signal characterization of two-port devices too. This task can be accomplished with a 'source-pull' technique and the MSR attached to the output of the DUT, as shown in Fig.2. In this configuration, the MSR measures both the noise temperature and the output reflection coefficient for each input terminations presented sequentially to the DUT input. It should be emphasized that because of the noise de-embedding technique realized in the MSR, one gets rid off the noise contribution of the instrument and can observe only the net output noise of the DUT. This means that the MSR performs as an ideal noiseless power meter scaled in temperature units. In consequence, the Friis correction for the second stage noise is not needed any more.

The on-line measurement of the output noise temperature and associated reflection coefficient bear an opportunity to determine a useful type of small-signal and noise characteristics of the DUT by referring the measurements to an arbitrary impedance. For example, one can represent the noise measurements in terms of the available power using the output noise temperature or the power absorbed in the standard termination when applying the effective output noise temperature T_{oef}. The last one is particularly beneficial for the DUT characterization, since this meets one of the conditions the scattering parameters are defined at. Thus utilizing the model and the unterminating technique, described in this paper, one obtains the four noise parameters of the DUT and its input reflection coefficient $\Gamma_i = s_{11}$ along with the insertion gain:

$$G_i = T_{or}(\beta_{g1} + \beta_{g2})^{-1} = |s_{21}|^2 \tag{9}$$

Other scattering parameters, i.e. s_{22} and the product $s_{12}s_{21}$ can be determined from the dependance of the output reflection coefficient:

$$\Gamma_o(\Gamma) = s_{22} + s_{12}s_{21}\frac{\Gamma}{1 - s_{11}\Gamma} \tag{10}$$

Using (10), those parameters can be easily fit to the measurements yielded by the MSR. Although in this characterization, $\arg(s_{12})$ and $\arg(s_{21})$ can not be separated each other, the seven real numbers representing the scattering matrix with the four noise

parameters are sufficient to model microwave transistors as well as design low-noise amplifiers.

Experimental results

First experiments with the characterization of passive devices and noise sources using the MSR revealed that the measurement uncertainty of the reflection coefficient is comparable to that of VNA [8],[9],[14]. Also, the reproducibility of the noise temperature measurement is pretty good [8],[14], so the uncertainty of the noise temperature standard, used to calibrate the MSR, might be of primary importance. Now regular tracing the measurement accuracy of the calibrated system relies on the measurements of several verification devices as a noise temperature standard and a few precision impedance standards taken from a VNA calibration kit. Repeating this measurements many times has enabled a statistical analysis of the MSR measurement errors and a discovery that thermal drifts are their most significant source [14].

At the next stage, the MSR system was applied to characterize GaAs FETs using the cold-source technique [4],[5]. For that purpose, a mechanical tuner was utilized to realize 10 - 12 'cold' terminations and the HP noise source as the 'hot' one. From the MSR measurements, the noise and the scattering parameters of the transistor were determined using the method described earlier. The results of the noise unterminating, obtained at 2 GHz, are shown in Table 1. The transistor noise parameters are represented by: T_{eo} - the minimum effective input noise temperature, Γ_{on} - the optimum source reflection coefficient and T_N - the temperature scaling the rate $T_e(\Gamma)$ increases when detuning from the minimum [9]. where SE denotes the standard error in dB assessed from residuals of this technique [9]. It should be emphasized that the results are in a fair agreement with the Pospieszalski's noise model for which the relationship $T_N \approx 2T_{eo}$ should hold at low frequency end [16]. The transistor noise parameters T_{eo} and T_N are plotted in Fig.3 versus the bias current I_D for different frequencies.

The scattering parameters acquired from the MSR were compared with those measured by a VNA. Their agreement was very good at all frequencies. Exemplary results obtained for 2 GHz are shown in Fig.4 to Fig.7. Small discrepancies, evident at the low current end in the magnitude of s_{21} (Fig.4) and in s_{11} (Fig.5), can be attributed to a high signal stimulus during the measurement with the VNA, although the power was kept at -20 dBm. The MSR results are, of course, to be free of this effect.

Conclusions

The multistate radiometer (MSR) presented in this paper is an original noise measuring instrument that for the first time realizes the simultaneous noise and vector analysis of networks. It has been based on an RF total power radiometer with a noise injection circuit at the input to provide different noise excitation conditions for the DUT. In consequence, the MSR yields the noise temperature and the reflection coefficient of one-port devices, and the four noise and scattering parameters of two-port devices. For the operation, it must be calibrated first with at least six impedance standards being at room temperature and at least one noise standard having a distinct noise temperature than the others. Since the calibration and accuracy enhancement techniques, employed for this task, stem from a general model describing all major sources of measurement error, ferrite isolation at the radiometer input is not needed any more and therefore the MSR can be tuned in very wide frequency range. All this results in the potential of very broadband automatic characterization of networks using the MSR.

Additional costs of converting a total power radiometer into the MSR are exceptionally low as compared with the price of an extra VNA to be employed for small-signal characterization of DUTs. The noise injection circuit can be realized in a easy way using an inexpensive noise diode, a directional coupler and a simple circuit of the multistate termination switched using e.g. PIN diodes. Thus the costs of device testing can be reduced by a great amount, however one must take into account that due to different states realized in the MSR, the time of measurement may be at least four times longer than needed for a typical noise characterization.

Extremely low power of the noise excitation is a very important advantage of the MSR. Even for a large bandwidth of the input circuit, e.g. 10 GHz, this power hardly approaches the nW range (-60 to -50 dBm). This feature makes the MSR very useful to the characterization of highly nonlinear semiconductor devices as, eg. Schottky diodes, transistors and MMICs, whose measurement results may suffer much from too large signal excitation. The experimental results, presented here, evidence clearly superiority of the MSR in such situations.

The power of the noise excitation can not be, of course, too low in comparison with the noise contributions of the DUT and the receiver, which both constitute a constant noise floor for the MSR measurement. However, on the contrary to signal measuring instruments, the accuracy of the MSR measurement does not suffer dramatically when the excitation approaches the noise floor, since the model applied do account correctly for all the noise contributions measured. Consequently, the signal parameters are measured by the MSR with the accuracy similar to that provided by VNA but at much higher signal level.

As follows from this paper, the multistate radiometry can begin a development of novel noise measurement techniques and technology for semiconductor devices. Particularly, the MSR can be applied to testing MMICs at a reduced cost. Further applications of the MSR may be associated with cryogenics that have been a field of an intensive research now. Since cooling down allows to reduce the noise floor and the excitation, the cryogenic MSR is supposed to set world records in lowest levels of the excitation utilized ever for measurement of the complex impedance. This feature might be of high importance for more precise measuring of circuits with very sensitive Josephson and SIS junctions.

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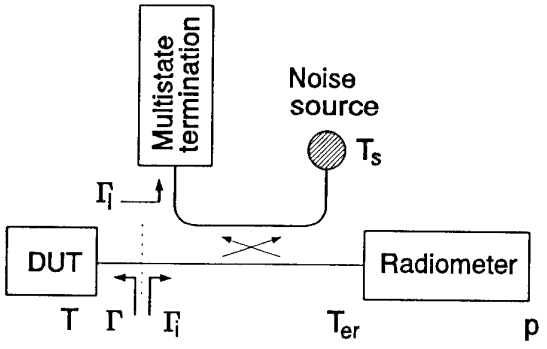

Fig.1. Block diagram of the multistate radiometer.

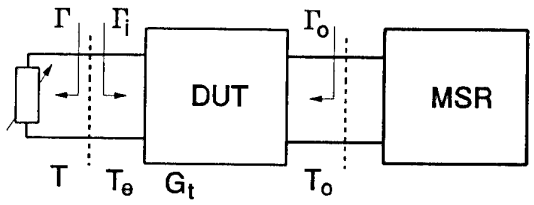

Fig.2. Characterization of a two-port device in the multistate radiometer system.

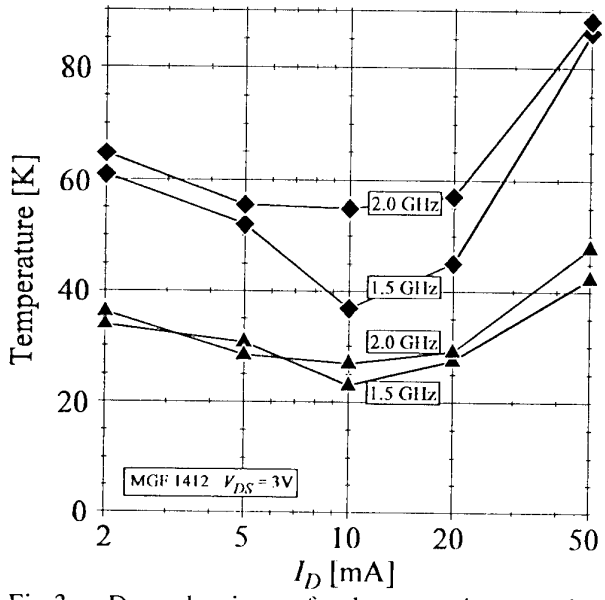

Fig.3. Dependencies of the transistor noise parameters: ▲ - T_{eo} and ◆ - T_N on the bias current I_D at two different frequencies.

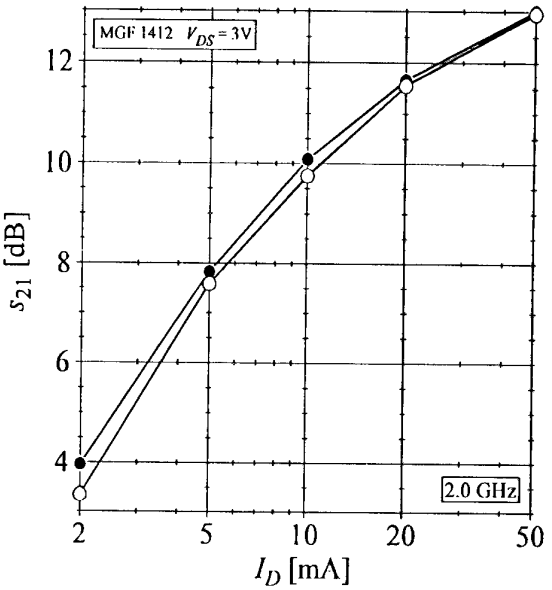

Fig.4. Dependence of s_{21} on the bias current I_D measured at 2 GHz with: ● - MSR, ○ - VNA.

Table 1. Parameters of a GaAs FET measured by the MSR.

MGF 1412/11-09 VDS=3 V F=2.0 GHz Ta=296 K IF 10 BAND M1
Test: 03/26/97 18:50 by MSS

ID	Teo	TN	Γon		S21	S11		SE
[mA]	[K]	[K]	mag	ang	[dB]	mag	ang	[dB]
2.0	36.1	64.6	0.899	34.1	4.02	0.971	-41.8	.008
5.0	28.5	55.7	0.866	34.8	7.90	0.965	-46.2	.006
10.0	26.9	54.9	0.837	35.7	10.15	0.957	-49.7	.007
20.0	29.0	57.1	0.824	38.7	11.73	0.951	-53.2	.007
50.0	47.8	88.0	0.804	46.6	13.07	0.940	-58.0	.007

Processed: 06/02/97 19.40 method: L1

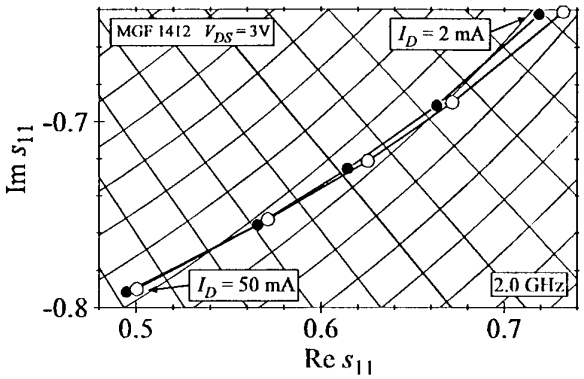

Fig.5. Dependence of s_{11} on the bias current I_D measured at 2 GHz with: ● - MSR, ○ - VNA.

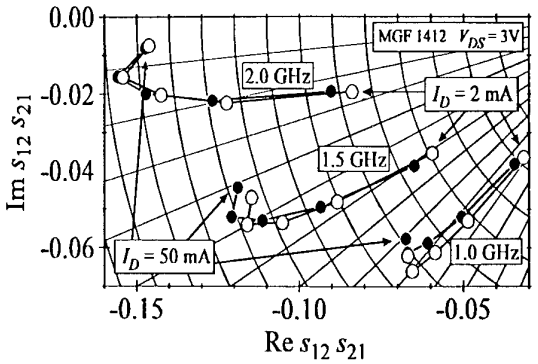

Fig.6. Dependence of the product $s_{12}s_{21}$ on the bias current I_D measured at several frequencies with: ● - MSR, ○ - VNA.

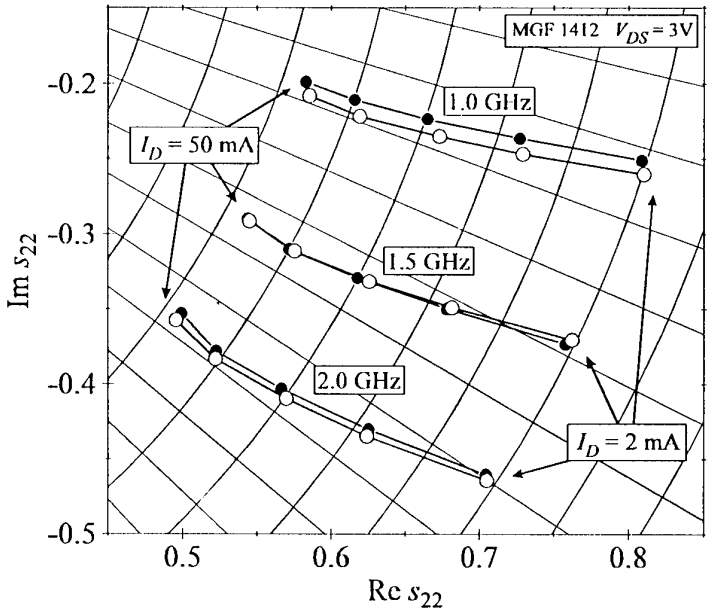

Fig.7. Dependence of s_{22} on the bias current I_D measured at several frequencies using: ● - MSR, ○ - VNA.

Extraction of Small-Signal and Noise Model Parameters for Dual-Gate MESFET

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Abstract: *A procedure for extracting the parameters of dual-gate MESFET model is described in this paper. The procedure is implemented in standard microwave circuit simulator Libra. Several small-signal dual-gate MESFET models are considered and discussed. Noise performance of dual-gate MESFET is modelled by four noise sources. In this way, noise parameters prediction over a wide frequency range can be done. In addition, a way to including the correlation between the noise sources is proposed.*

1. Introduction

The dual-gate MESFET (DG-MESFET) includes a second gate between the first gate and the drain [1]. The transconductance of the first gate can be controlled by the additional gate, enabling in this way the automatic gain control. Thanks to this, DG-MESFET can be applied for the input amplifier of a receiver, which may have to accommodate a large range of RF input levels. Additional advantage of existence of the second gate, when it is grounded for the RF signal, is the increase of the stability and maximal available gain.

Several different DG-MESFET models have been proposed in the literature, depending of the purposes. A small-signal linear model was recommended in the paper [2]. In [3] a small-signal model, which includes non-linear effects of some elements, was developed. Large-signal models are presented in several papers [4],[5].

For the amplifying applications, the noise performance of DG-MESFET is important. In these cases, for the design purposes, DG-MESFET noise parameters over the specified frequency range should be known. Because of that, the goal of this paper is the obtaining of a general model that will be able to describe both: signal as well as noise behaviour.

Noise model of Pospieszalski [6] for single-gate MESFET seems to be very practical for CAD applications. It is based on introducing two uncorrelated noise sources, a voltage source at the gate and a current source at the drain. Two corresponding equivalent temperatures, T_g and T_d, are assigned to the device intrinsic equivalent circuit. In [7] the authors of this paper have developed a procedure for MESFET noise parameters prediction based on Pospieszalski's approach. In [8] the authors have proposed a model for DG-MESFET which includes four uncorrelated noise sources. In this paper, the extraction of parameters of DG-MESFET general small-signal and noise model is extensively investigated and discussed. In addition, a further improvement of proposed DG-MESFET model by introducing the correlation between noise sources is proposed.

2. DG-MESFET Small-Signal Models of Different Complexity

The small-signal equivalent circuit parameters' extraction based on the experimentally determined S-parameters is a procedure, which usually can be applied to the standard MESFETs without problems. However, in the case of DG-MESFET a problem appears with the large number of elements having to be optimised. Our first goal was to consider several equivalent circuits with different number of elements and examine its suitability to represent small-signal performance. For this purpose, the powerful optimising possibilities of commercial program package Libra for analysis and design of microwave circuits, [9], was used. The reason for using this software is that it is available to the most of microwave circuit designers in the world.

Commonly, DG-MESFET is considered as the cascade of two standard MESFETs, as shown in Fig. 1. First, we considered a very simple model consisting of two MESFETs with identical element values [10]. Although the total number of unknown values is much reduced in this way, the optimisation does not give well results. A reasonable explanation is that two FET parts are internally biased differently and therefore the values of equivalent circuit elements should be different.

Further, two models are simultaneously considered, both having different element values in two FET parts. In

the simplified model, shown in Fig. 2, all parasitic elements except the feedback capacitances C_{gd1} and C_{gd2} are neglected. In this case the number of variable parameters was 14. The second model is more complex, involving all parasitic elements, as shown in Fig.3. The number of variable parameters of this model is 28.

For investigations we have chosen a commercially available DG-MESFET NE25139 manufactured by NEC. Device data are given in frequency range from 0.5 GHz to 4 GHz and refer to the next bias conditions: V_{ds}= 5V, I_{ds}= 10 mA, V_{g2s}= 0V. The optimisation was performed by using program Libra with the demand that model S-parameters correspond to measured device S-parameters. Great attention was paid to the choice of starting parameter values, especially in the case of complex circuit with the large number of variable parameters. The influence of this choice to the results was investigated. It was concluded that starting values for DG-MESFET equivalent circuit can be taken from the ranges of typical element values for standard, single-gate MESFET. These typical values are, for example: C_{gs1},C_{gs2}=(0.15-0.4)pF, r_{gs1},r_{gs2}=(2-10)Ω, C_{gd1},C_{gd2}=(0.01-0.03)pF, g_{ds1}, g_{ds2}=(0.002-0.004)S, C_{ds1},C_{ds2}=(0.05-0.1)pF, g_{m1},g_{m2} =(20-40)mS, τ_1,τ_2=(0.001-10)ps, R_{g1},R_{g2}=(0.5-3)Ω, R_s, R_d=(1-5)Ω, L_s,L_{g1},L_{g2},L_d=(0.1-0.9)nH. The remaining parasitic elements can take following values: R_{12}= (0.1-10)Ω, C_{g1g2},C_{g1d},C_{g2},C_d=(0.001-0.01)pF.

After extraction of model parameters in both cases, for simplified and complex equivalent circuits, S-parameters for NE25139 are calculated and compared to the available measured data. The results are shown in Fig.4 and Fig.5, respectively. It can be observed that the agreement between simulated and experimental data is much better in the case of complex model. Obviously, neglecting of parasitic elements gives a less appropriate model. It should be pointed that the great number of model elements, referred often as disadvantage in extraction procedure, is not a much serious problem when a powerful optimiser is used and the starting values are properly chosen.

The similar investigation was done for DG-MESFET MGF1100 manufactured by MITSUBISHI, in frequency range from 0.5 GHz to 8 GHz. Also, it was concluded that by using the complex model small-signal device behaviour could be successfully simulated.

3. Dual-Gate MESFET Model Including Noise Sources

On the basis of previous investigation, complex equivalent circuit shown in Fig.3 is chosen for further consideration. Our next step was obtaining a DG-MESFET noise model, which was done by incorporating the equivalent noise sources. Starting assumption was that noise sources could be including in the similar way as for single-gate MESFET [6]-[8]. Using this approach, a gate noise voltage and a drain noise current are added to each intrinsic circuit of both standard MESFETs connected in cascade (e_{gs1} , i_{ds1} to the first MESFET and e_{gs2} , i_{ds2} to the second MESFET). The remaining part of circuit is the same as one on Fig.3. The complete signal and noise model with four noise sources e_{gs1}, i_{ds1}, e_{gs2} and i_{ds2} is shown in Fig.6, where the intrinsic circuits are denoted by dotted boxes. The effect of noise sources is expressed through appropriate equivalent noise temperatures T_{g1}, T_{d1}, T_{g2} and T_{d2} , respectively, in the following way:

$$\left\langle \left| e_{gs1,2} \right|^2 \right\rangle = 4kBr_{gs1,2}T_{g1,2}, \tag{1}$$

$$\left\langle \left| i_{ds1,2} \right|^2 \right\rangle = 4kBg_{ds1,2}T_{d1,2}. \tag{2}$$

where k is Boltzmann constant, B is incremental bandwidth and $\langle\ \rangle$ indicates time average.

Starting from the admittance noise representation and assuming that the correlation between the noise voltage source and noise current source is negligible, the expressions for noise parameters of a single-gate MESFET intrinsic circuit can be derived [6],[7]. On the basis of that, the noise parameters for each of two intrinsic circuits of the DG-MESFET are formulated [8]. Minimum noise figure $F_{min1,2}$, optimum source impedance $Z_{opt1,2}$, corresponding optimum reflection coefficient $\Gamma_{opt1,2}$ and equivalent noise resistance $R_{n1,2}$ (Z_0 is reference impedance, T_0 is room temperature) are expressed as the functions of circuit elements and equivalent temperatures,

$$F_{\min 1,2} = 10\log\left[2\frac{\omega C_{gs1,2}}{g_{m1,2}T_o} \times \sqrt{r_{gs1,2}g_{ds1,2}T_{g1,2}T_{d1,2} + \left(\frac{\omega C_{gs1,2} r_{gs1,2} g_{ds1,2} T_{d1,2}}{g_{m1,2}} \right)^2 + \frac{2\omega^2 C_{gs1,2}^2 r_{gs1,2} g_{ds1,2} T_{d1,2}}{g_{m1,2}^2 T_o} + 1} \right], \tag{3}$$

$$R_{n1,2} = \frac{T_{g1,2}}{T_o} r_{gs1,2} + \frac{T_{d1,2} g_{ds1,2}}{T_o g_{m1,2}^2} \left(1 + \omega^2 C_{gs1,2}^2 r_{gs1,2}^2 \right) \tag{4}$$

$$Z_{opt1,2} = \sqrt{\left(\frac{g_{m1,2}}{\omega C_{gs1,2}} \right)^2 \frac{r_{gs1,2} T_{g1,2}}{g_{ds1,2} T_{d1,2}} + r_{gs1,2}^2} + j\frac{1}{\omega C_{gs1,2}} \tag{5}$$

$$\Gamma_{opt1,2} = \left(Z_{opt1,2} - Z_0 \right) / \left(Z_{opt1,2} + Z_0 \right), \tag{6}$$

The procedure for obtaining of the model elements includes the following steps:

- The equations expressing noise parameters (3)-(6) are defined for each of two intrinsic circuits. These equations are described within the EQN block of program package Libra.
- The intrinsic equivalent circuit for each of two MESFETs is defined in CKT block of Libra and the noise parameter values obtained by equations (3)-(6) are assigned to defined intrinsic circuits by the instruction NPAR.
- In addition, the topology of entire DG-MESFET is described within the CKT block by adding the remaining equivalent circuit elements. Then, S-parameters and noise parameters of whole model can be calculated in frequency range required.
- At the end, the optimisation procedure is applied. All equivalent circuit elements including temperatures T_{g1}, T_{d1}, T_{g2} and T_{d2} are optimised. The optimisation goal is that the simulated and measured S and noise parameters agree as well as possible.

The DG-MESFET modelling by using complex equivalent circuit has been done for transistor NE25139. The starting values are chosen as described in previous paragraph. The equivalent circuit element values obtained after optimisation are given in Table 1.

The noise parameter characteristics of NE25139 obtained by the circuit simulator using the proposed model (denoted by MOD) are given in final results referring to dual-gate MESFET noise parameter characteristics are shown in Fig.7, (a)-(d). In addition, the noise characteristics are given which are based on the manufacturer's measured data (MER) at several frequencies. It can be observed that the agreement is very well over the full frequency range. Therefore, the model presented here can properly represent noise performance of DG-MESFET.

4. DG-MESFET Model Including Noise Sources and Correlation

In the approach presented in [6] from which we started in developing the DG-MESFET model, the correlation between two noise sources is ignored. The correlation between voltage source at the gate and current source at the drain is really small, but there are some opinions that it is not negligible at higher frequencies [11]. Because of that, a possibility of including the correlations between sources e_{gs1} and i_{ds1}, as well as between e_{gs2} and i_{ds2} in the DG-MESFET model is considered.

Correlation coefficient between two noise sources in intrinsic circuit of single-gate MESFET can be expressed as

$$\rho_{cor} = |\rho_{cor}|e^{j\varphi_{cor}} = \left\langle e_{gs} i_{ds}^{*} \right\rangle \Big/ \sqrt{\left\langle |e_{gs}|^2 \right\rangle \left\langle |i_{ds}|^2 \right\rangle} \quad (7)$$

Starting from (1) and (2) we derived the full expressions without any approximation for all the noise parameters: minimum noise figure F_{min}, noise resistance R_n and optimum impedance Z_{opt} as functions of T_g, T_d and ρ_{cor}. These expressions are given by (8)-(10),

$$F_{\min} = 10\log\left\{1 + \frac{2\omega C_{gs}}{g_m T_0}\left[r_{gs} g_{ds} T_g T_d + (\omega C_{gs} r_{gs} g_{ds} T_d)^2 \Big/ g_m^2 - |\rho_{cor}|^2 P_1^2 + 2\omega C_{gs} r_{gs} g_{ds} T_d |\rho_{cor}| P_2 / g_m\right]^{1/2} + 2\omega^2 C_{gs}^2 r_{gs} g_{ds} T_d \Big/ g_m^2 T_0 + 2\omega C_{gs} |\rho_{cor}| P_2 / g_m T_0\right\} \quad (8)$$

$$R_n = r_{gs} T_g / T_0 + g_{ds} T_d \left(1 + \omega^2 C_{gs}^2 r_{gs}^2\right) \Big/ T_0 g_m^2 + 2|\rho_{cor}|\left(P_1 + \omega C_{gs} r_{gs} P_2\right) \Big/ T_0 g_m \quad (9)$$

$$Z_{opt} = \sqrt{r_{gs}^2 + \frac{g_m^2}{\omega^2 C_{gs}^2}\left(\frac{r_{gs} T_g}{g_{ds} T_d} - \frac{|\rho_{cor}|^2 P_1^2}{g_{ds}^2 T_d^2}\right) + \frac{2 g_m r_{gs} |\rho_{cor}| P_2}{\omega C_{gs} g_{ds} T_d}} + j\left(\frac{1}{\omega C_{gs}} + \frac{g_m |\rho_{cor}| P_1}{\omega C_{gs} g_{ds} T_d}\right) \quad (10)$$

where

$$P_1 = \sqrt{r_{gs} g_{ds} T_g T_d}\cos[\varphi_{cor} - \omega\tau],$$
$$P_2 = \sqrt{r_{gs} g_{ds} T_g T_d}\sin[\varphi_{cor} - \omega\tau].$$

The including the correlation to the DG-MESFET model considered above can be done in the following way: The equations (3)-(5) should be replaced by equations (8)-(10) for both parts of model. The total number of parameters that should be extracted is increased in this way, because there are two new parameters, ρ_{cor1} and ρ_{cor2}. On the other hand, by using these exact expressions without any approximation, some improvement of noise parameters prediction has to be expected.

5. Conclusion

For the small-signal applications, the double-gate MESFET can be successfully modelled by an equivalent circuit based on the cascade of two standard MESFETs equivalent circuits with added parasitic elements. With the aim to model the noise performance, the equivalent noise sources are inserted into both FET parts. For extraction of model parameters the powerful optimisation routine of a standard microwave circuit simulator is used. It is concluded, that successful extraction can be done when the starting values are taken from the single-gate MESFET typical values. The agreement between the simulation results and measured data for S-parameters as well as for noise parameters was very well in all examples. The signal and noise model obtained in this way can be used for frequency extrapolation of S- and noise parameters. A further improvement of this model is suggested by including the correlation between noise sources.

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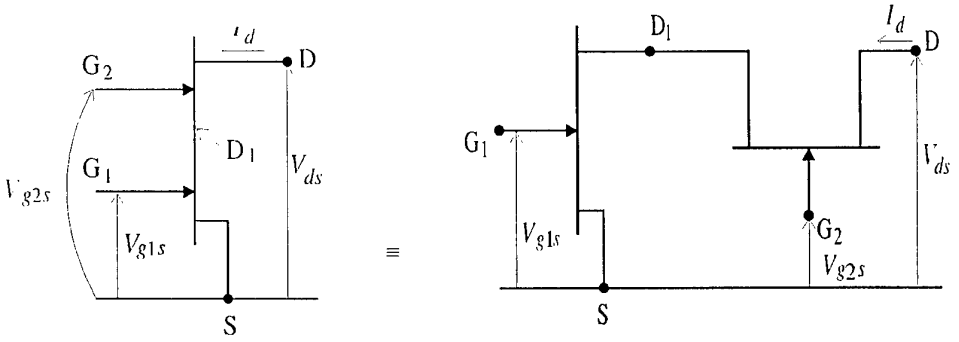


Fig. 1. DG-MESFET as a cascade of two standard MESFETs

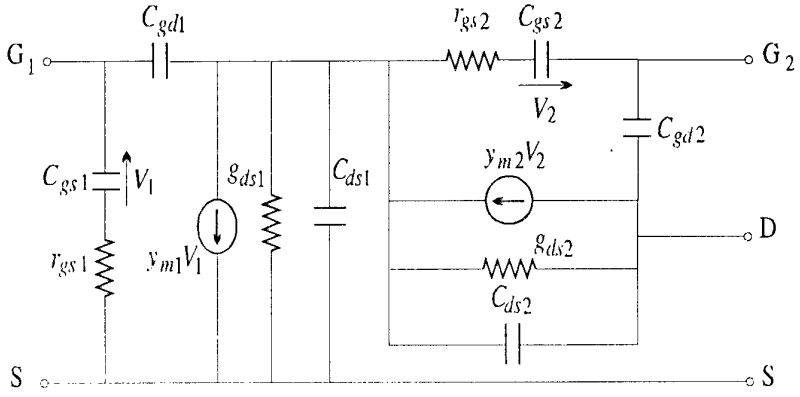


Fig. 2. Simplified DG-MESFET equivalent circuit ($y_{m1}=g_{m1}e^{-j\omega\tau_1}$, $y_{m2}=g_{m2}e^{-j\omega\tau_2}$)

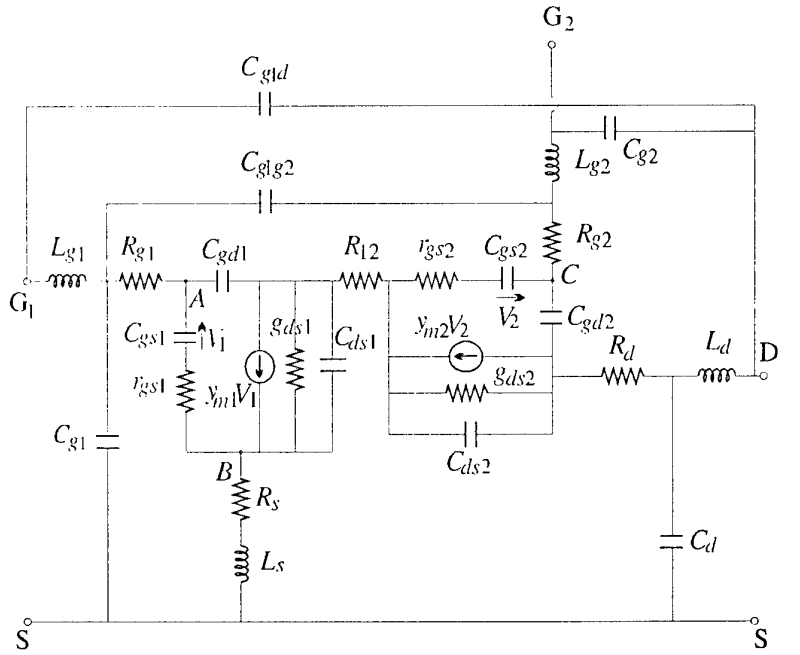
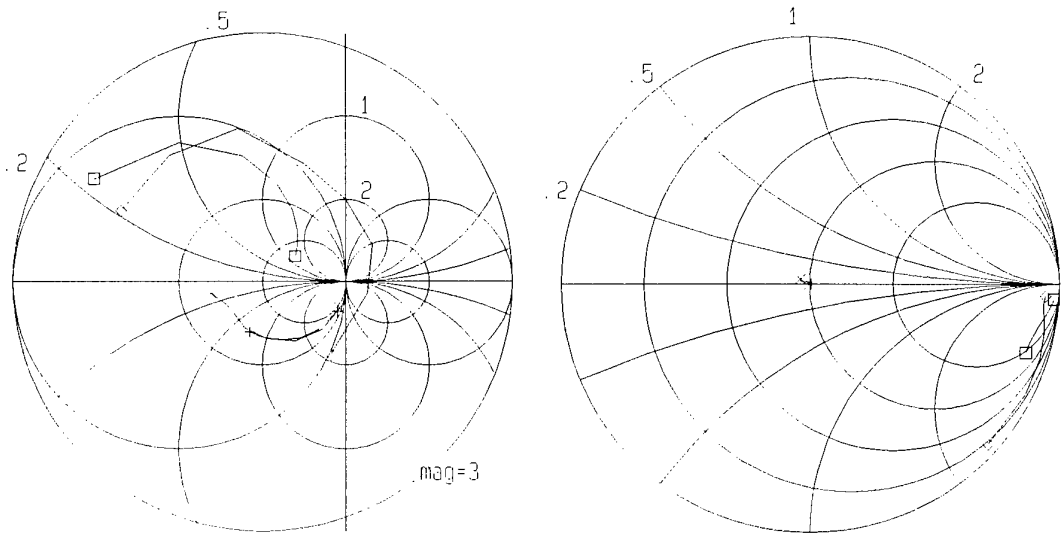


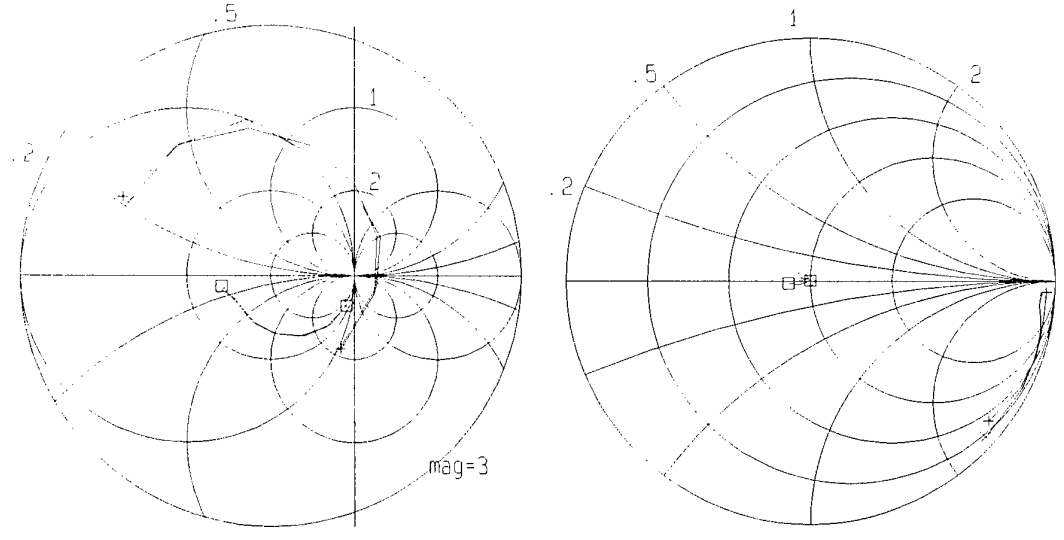
Fig.3. DG-MESFET complex small-signal model



a)
S_{11} (X - measured, + - simulated)
S_{21} (◊ - measured, □ - simulated)

b)
S_{22} (◊ - measured, □ - simulated)
S_{12} (X - measured, + - simulated)

Fig.4. Comparison of simulated S-parameters for model in Fig.2 with measured data



a)
S_{11} (◊ - measured, □ - simulated)
S_{21} (X - measured, + - simulated)

b)
S_{22} (X - measured, + - simulated)
S_{12} (◊ - measured, □ - simulated)

Fig. 5. Comparison of simulated S-parameters for model in Fig.3 with measured data

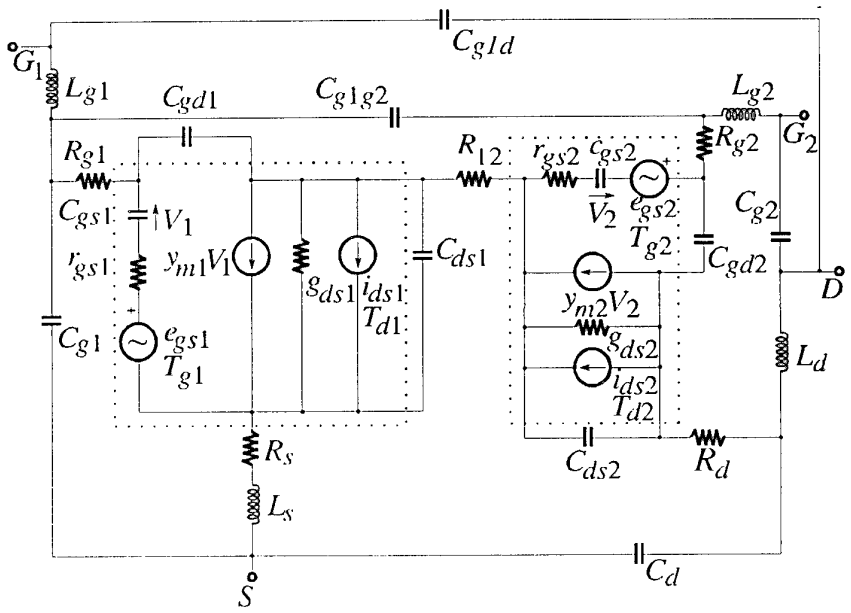
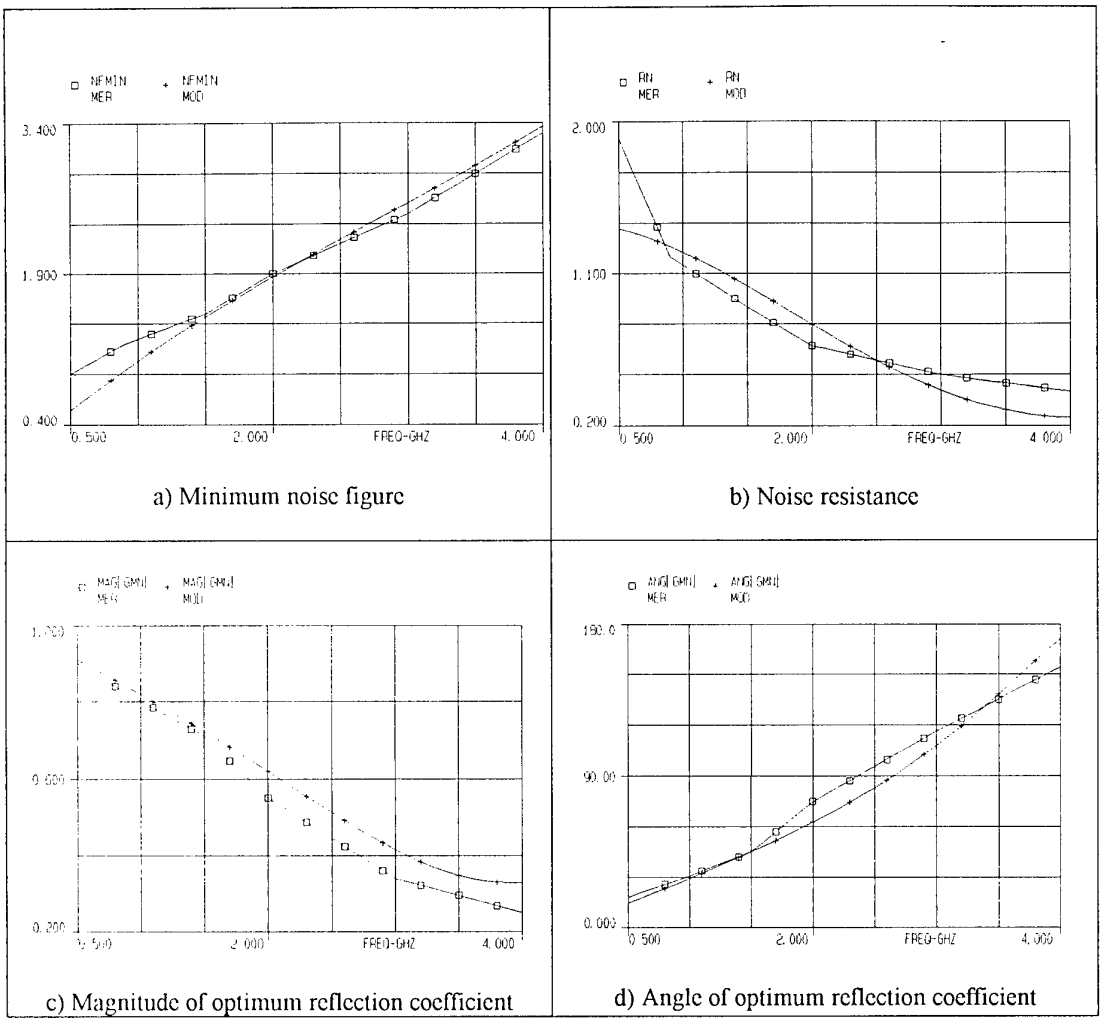


Fig.6 *DG-MESFET noise model*

Table 1. *Values of extracted parameters for DG-MESFET NE25139*

Elements		FET1	FET2
τ	(ps)	3.548	1.194
g_m	(S)	0.0296	0.0048
C_{gs}	(pF)	0.492	0.269
r_{gs}	(Ω)	5.394	5.049
r_{ds}	(Ω)	490.16	555.70
C_{gd}	(pF)	0.0336	0.0462
C_{ds}	(pF)	0.0689	0.0867

Common elem.		
L_{g1}	(nH)	1.680
R_{g1}	(Ω)	2.7666
L_{g2}	(nH)	3.938
R_{g2}	(Ω)	2.494
L_s	(nH)	1.646
R_s	(Ω)	2.934
L_d	(nH)	3.304
R_d	(Ω)	2.454
C_{g1g2}	(pF)	0.0277
C_{g1}	(pF)	0.551
R_{12}	(Ω)	0.990
C_{g1d}	(fF)	0.06
C_d	(fF)	1.7
C_{g2}	(fF)	4.618



a) Minimum noise figure

b) Noise resistance

c) Magnitude of optimum reflection coefficient

d) Angle of optimum reflection coefficient

Fig. 7 *Simulated noise characteristics based on proposed model (MOD) compared with measured data (MER)*

Package Modelling Based on RF Measurements

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Abstract: In cooperation with a semiconductor manufacturer small outline packages (SOP) for BiCMOS circuits were characterized. The model generation for 16-pin ceramic and plastic SOP16 packages is based on S-parameter measurements up to 10 GHz. The maximum operation frequency of active devices is assumed to be 4 GHz, therefore the validity of the package parasitics shall be restricted to that upper frequency limit as well. The parameters of the equivalent circuit network are fitted by means of a CAD program.

Introduction

The developement of semiconductor electronics has caused a continous trend towards higher signal frequencies and clock rates. Signals and of course higher order harmonics reach microwave frequencies; the electrical behaviour of a circuit is effected by transmission lines and device parasitics. Modern RF circuit design requires more exact models for all active and passive circuit components, including the parasitics of a package. Therefore it is important to know the influence of bond wires, leads, crosstalk and radiation prior to chip design. To make parasitics available to the circuit designer, a lumped-element equivalent circuit network is developed.

An equivalent circuit network can be derived either from measurements or simulations. The measurement of scattering (S) parameters by a network analyzer is an exact and reliable way of characterizing RF properties, while the multiport package is described by one- and two-port measurements. Measured data of the investigated package can be the basis for a model. The model parameters are numerically optimized to fit the frequency response of the original package.

An other way of modelling is electromagnetic field simulation based on Maxwell's equations. This is the only possible method when a new package is designed. Parameters can be derived directly from fields or data can be obtained for curve fitting. Creating a numerical model requires precise knowledge of physical dimensions and material constants. Errors result from differences between reality and field model, from field solution process and from parameter extraction. In order to minimize modelling errors and to prove the model by comparison with measured data, the model described in this paper is based on S-parameter measurements.

Circuit Model

The topology of the equivalent circuit is chosen in correspondence with the physical structure of the package. Fig. 1 shows the SOP16 package.

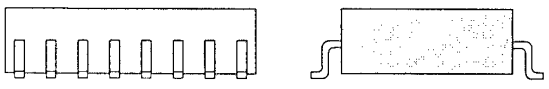

Fig. 1: SOP16 / CSOP16 Package

The more detailed the circuit is formed, the more elements can be adjusted and the more couplings can be modelled, and as a result more potential

resonant frequencies will exist. But with a growing number of parameters, the model accuracy is not automatically increased. The first reason is the mathematical problem of finding the optimum of a nonlinear function. Even modern algorithms become ineffectiv if the number of parameters exceeds 10 to 20. Extensive effort is necessary to derive start values and appropriate variable ranges. The second reason is that a more complex model with a larger quantity of lumped elements will not necessarily give us a better representation of the real three dimensional continous structure. In the case of numerical parameter fitting, this effect sometimes leads to solutions with non-physical parameter values, but better error functions.

Nevertheless the circuit network should be reduced to lumped RLC elements. If the equivalent circuit is created by means of a modern frequency-domain harmonic-balance circuit simulator, transmission lines, coupled lines, and other dispersive elements with appropriate electrical properties are available.

But in designing analog integrated circuits (ICs) time domain simulators with limited two-pole elements are commonly used. Only capacitors, inductors, resistors and mutual inductances are permitted to form a universal circuit model. The number of circuit elements depends on the frequency response to be modelled and on the upper frequency limit. Fig. 2 depicts the model of the SOP16 / CSOP16 packages used for parameter extraction.

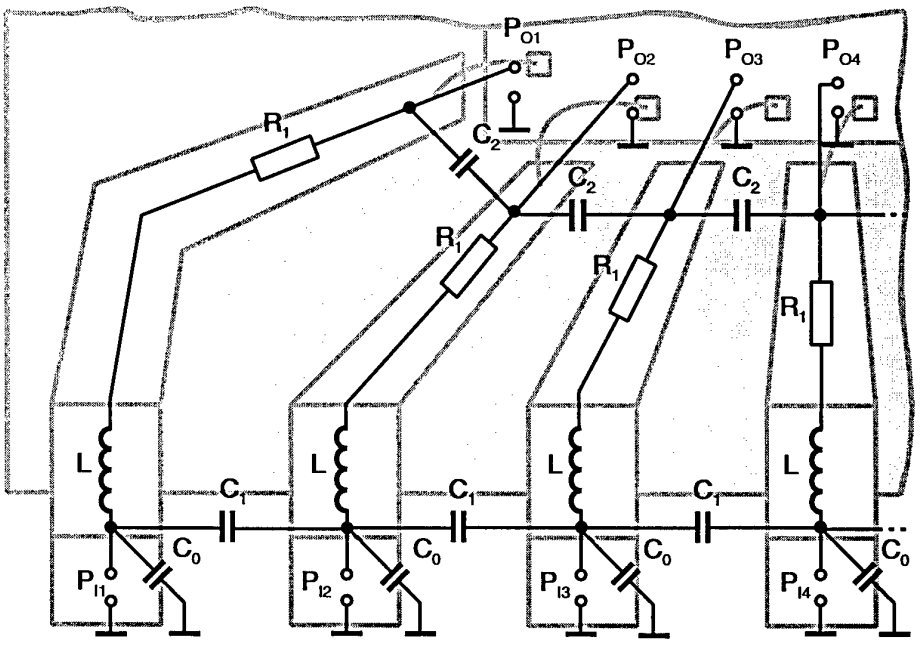

Fig. 2: Package and corresponding equivalent circuit

Measurement Setup

The IC package to be measured has been placed on top of a waferprober chuck. So it was possible to guarantee well-defined positioning and contact reliability. Though the pitch of 1.27 mm is rather large, the handling of the device and probes is a key problem. In order to assure the same field and boundary conditions as on a printed circuit board (PCB), the IC was fixed to a piece of PCB material at the center of its body by means of epoxy resin. The metallization of the carrier was not connected to RF ground. A comparison to an

RF-grounded metallization has shown no significant difference. The size of the quadratic carrier board (ε_r = 4, h = 1.5 mm) has been varied between 30 mm and 60 mm to exclude patch resonances.

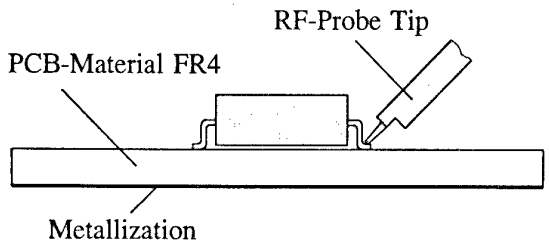

Fig. 3: Package measurement setup

The package and the surrounding parts are shown schematically in Fig. 3. The device is contacted by RF probe tips. These probes have a ground-signal-ground (GSG) structure similar to a coplanar waveguide. The distance between the contacts is 1.27 mm, according to the actual pitch of the package. The signal line on both sides is guided by a ground line to reduce fringing. This geometry supports high accuracy but unfortunately makes it impossible to contact neighbouring pins. Two probe tips are connected to a network analyzer. Short, open and load standards in GSG structure are used to perform a two-port vector calibration of the analyzer.

Standard Chips

Calibrating the network analyzer delivers reference planes at the top of the probe tips. It was necessary to place well known standards inside the IC, in order to get information about the package itself. These standard elements were fabricated in thin film technology on 0.25 mm Al_2O_3 ceramic substrate. Two different chip layouts were designed to meet the requirement to have always the same bond wire layout. The 2-mm square chip contains open-short-load structures as well as a through line and internal probe tip patches. The chips were bonded with 33-µm wires into the CSOP16 (Al-bonds) and SOP16 (Au-bonds) packages. Load elements have been laser trimmed to ±1 % accuracy. Both calibration chips are shown in Fig. 4 and Fig. 5. An RF signal applied to the probe tip passes through the package and bond wire to the internal bond pad like a "normal" signal (as in any application specific circuit).. All mentioned elements including coupling to ground and coupling between each other become part of the package model. The standard elements of the calibration chip have rather small dimensions and can be considered as ideal elements. Model parameters can be fitted by comparing measured data with the probe tip reference plane to ideal open-short-load elements.

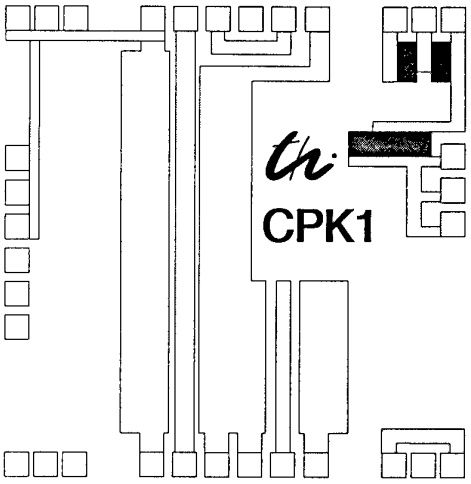

Fig. 4: Calibration Standard Chip CPK1

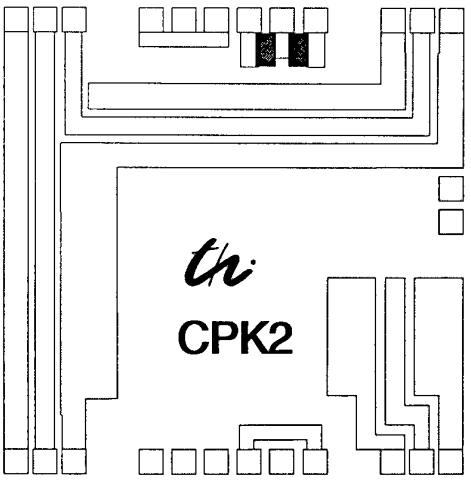

Fig. 5: Calibration Standard Chip CPK2

Parameter Optimization

All parameters of the equivalent circuit network have been determined based on measured data.

The circuit model (Fig. 2) contains a set of elements for each pin. The results of the measurements have shown that the relatively large complexity can be reduced significantly. A common set of parameter values can be chosen for all inner pins of the package because the S-parameters reveal only slight differences. Deviations in frequency response occurred for the four outer pins only. This is due to a different pin and bond wire geometry. The final circuit model for both packages consists of two sets of parasitic elements - one set for the inner pins and a second one for the outer pins.

Measured S-Parameters

Typical measured data for the frequency range of 100 MHz to 10.1 GHz are shown in Fig. 6. The reflection coefficients for GSG-contacted plastic SOP16 package with test chips inside are plotted. There is a significant deviation from ideality, especially for open structures. Ceramic CSOP16 packages have larger deviations and lower resonant frequencies. With our relatively simple equivalent circuit network, we are able to model continous curves, but not resonant effects (which are visible at higher frequencies). For that reason the model optimization has been limited to 4 GHz.

Results

The circuit model in the presented form is exclusively based on measured data obtained with two-port ground-signal-ground probes. The coupling across two or more pins has not been considered yet. Ground C_0 and coupling capacitor C_1 (Fig. 2) are lumped together. Further investigation has to extend measurements to ground-signal structures and should add field simulation results to the database.

We have used the Microwave Design System (MDS) RF simulator from Hewlett Packard to determine the parameter set of the present model. Initial parameter values have been derived by minimizing a least square error term for short, open or load S-parameters. The final optimization was done with an unweighted overall sum of error functions within the frequency range between 100 MHz and 4 GHz. Several combinations of stochastic and gradient search algorithms were tested to check the stability of the optimization algorithm, with the result that stable parameter sets were found.

The equivalent circuit network parameters for the ceramic CSOP16 package are as follows:

Inner Pins	Outer Pins
R_1 = 1.04 Ω	R_1 = 1.80 Ω
C_1 = 207 fF	C_1 = 456 fF
C_2 = 163 fF	C_2 = 229 fF
L = 2.07 nH	L = 3.77 nH

For the plastic SOP16 package we find the following element values:

Inner Pins	Outer Pins
R_1 = 0.87 Ω	R_1 = 1.81 Ω
C_1 = 116 fF	C_1 = 275 fF
C_2 = 144 fF	C_2 = 255 fF
L = 2.01 nH	L = 3.02 nH

Fig. 7 and Fig. 8 show measured and modelled frequency responses from 100 MHz to 4 GHz for plastic SOP16 and ceramic CSOP16 packages as well as the resulting differences.

Acknowledgment

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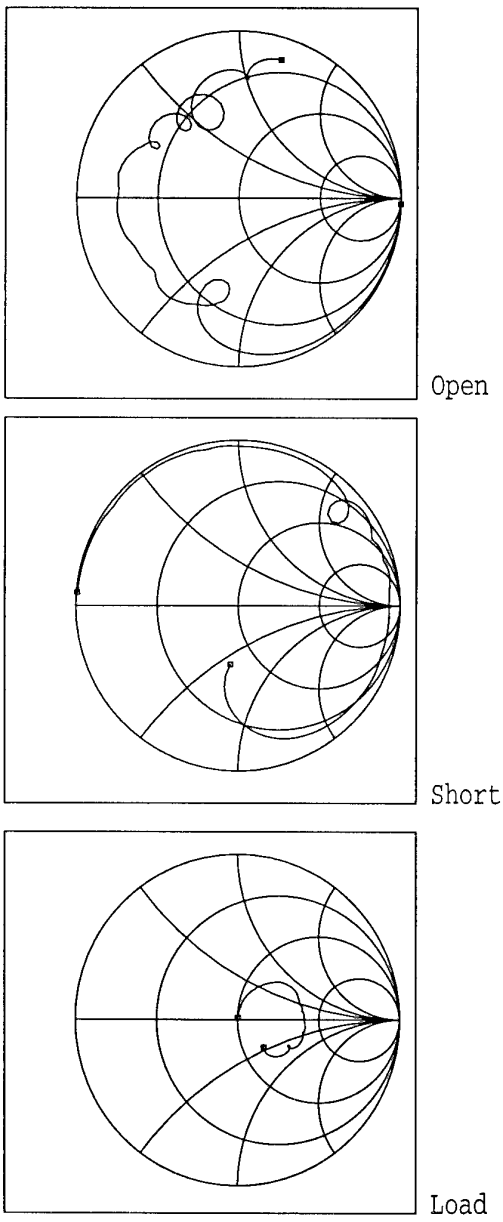

Fig. 6: Measured reflection coefficients for plastic SOP16 open, short and load elements (100 MHz to 10.1 GHz)

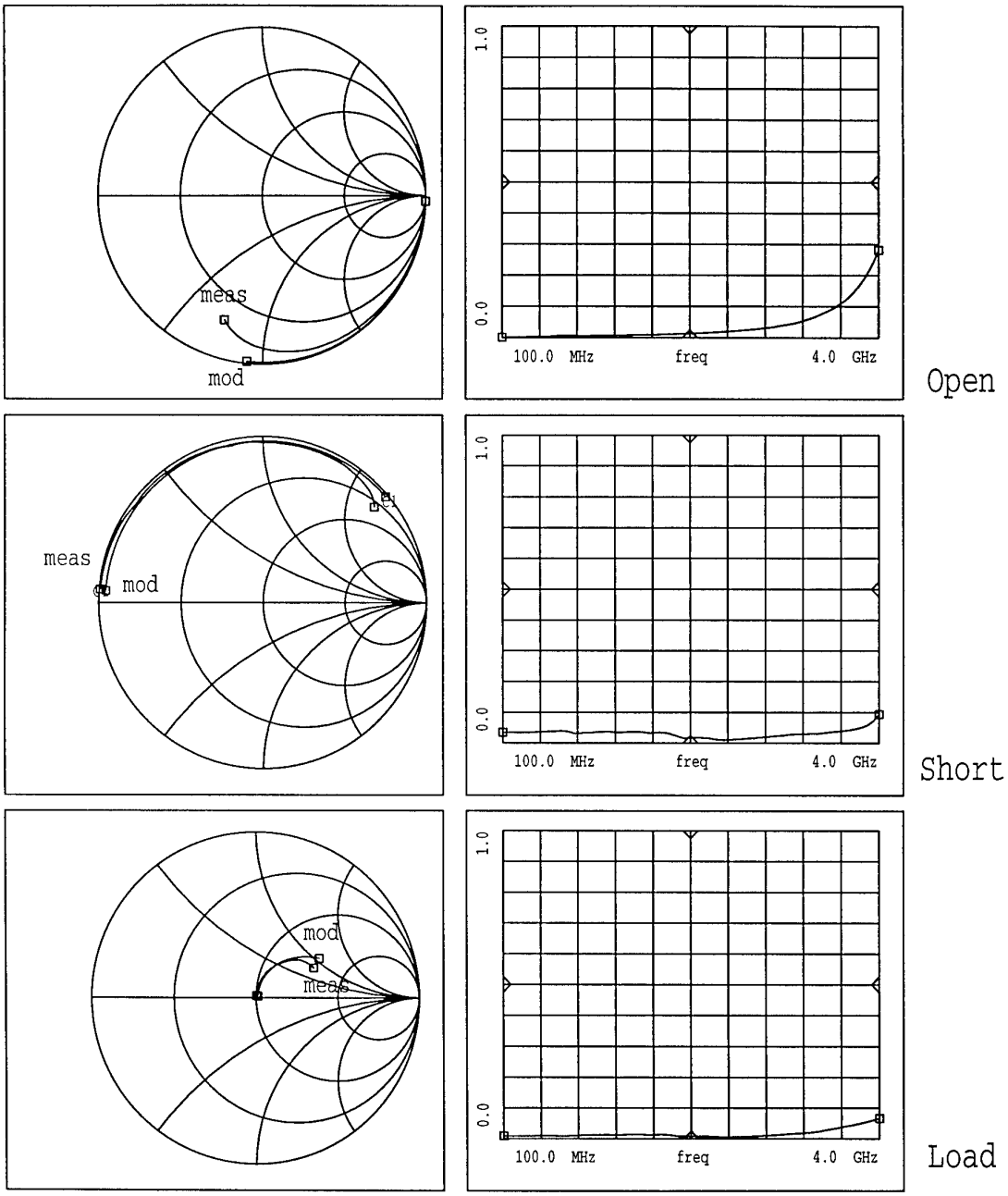

Fig. 7: Comparison between measured and modelled plastic SOP16 open, short and load elements (S_{11} and modelling error abs(S_{11mod} - S_{11meas}) between 100 MHz to 4 GHz)

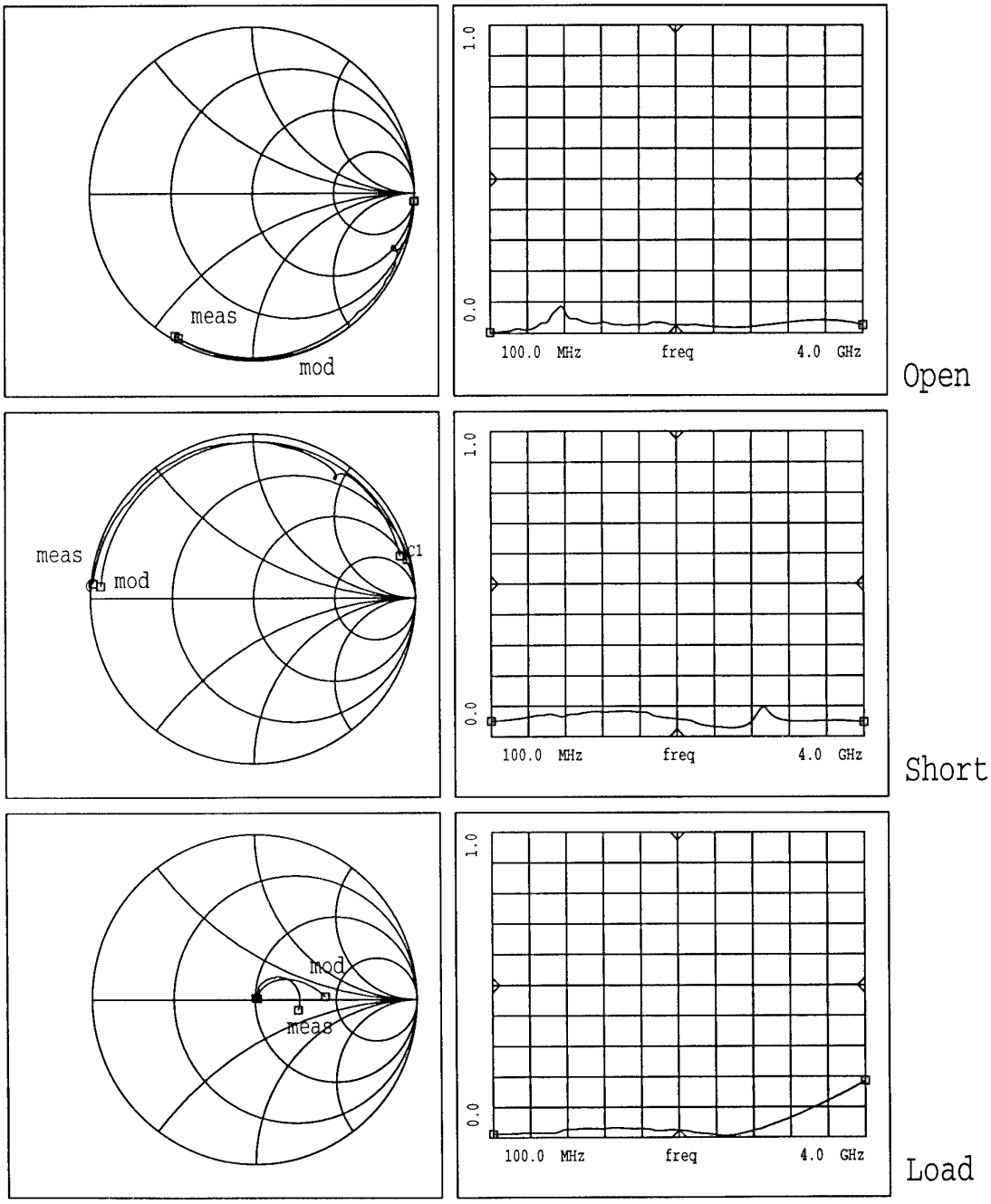

Fig. 8: Comparison between measured and modelled ceramic CSOP16 open, short and load elements (S_{11} and modelling error abs(S_{11mod} - S_{11meas}) between 100 MHz to 4 GHz)

Rigorous Numerical Simulation and Modeling of Coplanar Discontinuities

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Abstract

A Finite-Difference method in the frequency domain (FDFD) is extended in order to analyze typical MMIC (monolithic microwave integrated circuit) structures including dielectric and metallic loss effects. The FDFD scheme is based on polygonal grids in order to approximate non-cartesian material contours efficiently. The method is applied to different coplanar waveguide (CPW) structures, namely the short end, an air bridge and a circular right angle bend. Simple physical models are presented which describe the scattering behavior.

Introduction

In the last few years, the coplanar waveguide (CPW) concept has gained more and more attention as an alternative to the conventional microstrip line. Since the ground conductors of a CPW are available at the front side of the substrate, no backside process is required in general. This leads to reduced costs. Furthermore, it is not necessary to decrease the thickness of the substrate, since the characteristic impedance of a CPW does not significantly depend on the substrate thickness. Finally, CPW MMICs (monolithic microwave integrated circuits) can be contacted by wafer probers which makes measurements comparatively simple. All these advantages have lead to an intensive use of the CPW technology. However, up to now only few analyses and models have been presented for CPW discontinuities which are realistic for MMIC applications.

For a reliable design of MMICs the use of CAD methods is inevitable. Therefore, not only the active devices, but also the the passive components of the circuit have to be modeled accurately. This paper concentrates on the analysis and modeling of passive CPW discontinuities.

Due to increasing operating frequencies and higher integration, conductor loss effects become more important. Therefore, both, finite metallization thicknesses and realistic conductivities will be taken into account in this paper. Since for CPWs the skin depth is of the same order of magnitude as the conductor thickness it is not possible to apply simple approximations [1], e.g. surface impedance methods. Consequently, it is desirable to have a powerful tool enabling one to make a full-wave analysis of arbitrary lossy structures in order to allow an accurate circuit simulation.

The Numerical Method

The method presented here is based on the Finite-Difference method in the frequency domain which was already used in [2, 3] to analyze the scattering behavior of several lossless MMIC discontinuities. Since the method uses a discretization of the considered domain, almost arbitrarily shaped structures can be analyzed. The aim of the analysis is the

computation of the scattering matrix of different waveguide discontinuities. The Finite-Difference procedure is performed in the frequency domain, since the scattering matrix is a frequency domain quantity. Therefore, no discrete fourier transform is needed which would introduce additional numerical errors. A second advantage of the frequency domain is that one can easily separate the different modes of propagation which is much more difficult in the time domain.

The FDFD method is extended to the lossy case by introducing a complex permittivity. Thus, the current distribution inside the metallizations is found by discretizing the conductors sufficiently and is not approximated by surface impedance concepts. For the analysis of the scattering behavior of a 3D-structure two different calculations have to be performed:

- First, the homogeneous waveguides attached to the discontinuity have to be considered which serve as ports of the three-dimensional structure. This analysis leads to a complex eigenvalue problem (in the lossless case only real matrices occur).
- The scattering behavior of the discontinuity is given by a three-dimensional boundary-value problem. It leads to a sparse complex system of linear equations. This system is solved for different excitations which subsequently allows the computation of the scattering matrix of the structure.

In addition to the consideration of lossy materials a second feature was implemented in the FDFD method. One can show that the efficiency of conventional Finite-Difference methods which are based on cartesian grids decreases significantly if the material contours do not match the grid lines. Therefore, an extension of the method was developed which permits the use of polygonal grids in both two and three dimensions. Although the polygonal grids have to fulfill some restrictions in order to construct an orthogonal dual grid, large classes of structures can be analyzed very efficiently with such grid types. As an example, fig. 1 shows a polygonal grid which can be used to approximate circular material contours.

Numerical Results

In the following the FDFD results for both, homogeneous CPWs and different CPW discontinuities will be presented. The physical effects will be examined and for some structures simple models will be given.

Homogeneous CPW

First of all, the homogeneous coplanar waveguide (cross-section of fig. 2) is analyzed. For the homogeneous CPW and for all further discontinuities the following dimensions and material parameters are assumed which are typical for MMIC applications: The metallizations consist of Au with a conductivity of $\kappa = 3 \cdot 10^7\ \Omega^{-1}\ m^{-1}$ and a thickness of $t = 3\ \mu m$. The width of the center conductor is $w = 20\ \mu m$, the slot width is $s = 15\ \mu m$. The ground metallizations are at least $w_g = 150\ \mu m$ wide. GaAs is used as substrate ($\epsilon_r = 12.9$, $\tan\delta = 3 \cdot 10^{-4}$).

In fig. 3 the Finite-Difference results of the relative effective permittivity $\epsilon_{r,eff}$ are compared with those obtained by an analytical method [4]. Fig. 4 shows the same comparison for the attenuation constant α and figures 5 and 6 for the complex characteristic impedance Z_L. The results of the two methods show good agreement. This is a verification for the numerical method. The rising values of $\epsilon_{r,eff}$, $Re(Z_L)$ and $Im(-Z_L)$ for decreasing frequencies occur mainly due to an increase of the inductance [1]. The small deviations between the FDFD-analysis and the model which can be observed at high frequencies can be explained with a slight dispersion which is not considered in the analytical model [4].

Short end

A simple CPW short end as shown in fig. 2 is analyzed. The scattering behavior of a CPW short end is usually described by a length-extension $l_{ext,\beta}$ [5]. The length-extension

$$l_{ext,\beta} = -\frac{\varphi}{2\beta}$$

is defined as the length difference between a real short stub (see reference plane in fig. 2) and an ideal one where the two reflection coefficients have the same phase. φ is the phase of the reflection coefficient r. The modulus of r is equal to one if losses and radiation are neglected. However, if realistic metallic and dielectric losses are introduced, the reflection coefficient decreases. To describe this behavior, a second length-extension

$$l_{ext,\alpha} = -\frac{\ln|r|}{2\alpha}$$

can be defined. These parameters were chosen because both length-extensions are almost constant over a wide frequency range.

The values of $l_{ext,\beta}$ and $l_{ext,\alpha}$, computed with the FDFD method, are presented in figures 7 and 8 for $d = w + 2s = 50\ \mu m$.

As it is shown in fig. 7, the length extension $l_{ext,\beta}$ increases for decreasing frequencies. This result is interesting since it differs from the lossless case [5]. Similar to the homogeneous line, this can be explained with an increase of the inductance for decreasing frequencies. A reasonable equivalent circuit for a lossy CPW short end is shown in fig. 9. For frequencies f higher than 10 GHz, the external inductance L_{ext} remains almost constant, whereas the internal inductance L_{int} decreases with $\sqrt{f}^{-1}$ [6]. The resistance R is equal to the imaginary part of the impedance of the internal inductance: $R = 2\pi f L_{int}$. For $0 < f < 100\ GHz$, $d = 50\mu m$, $t = 3\ \mu m$ and the considered materials the following modeling formulas hold:

$$\frac{R}{\sqrt{f/GHz}} = \left(6.3 + 0.25\frac{s}{\mu m}\right) m\Omega$$

$$L_{ext} = \left(0.35 + 0.13\frac{s}{\mu m}\right) pH \qquad (1)$$

Air bridge type A

In MMICs based on CPW technology air bridges are of high importance for suppressing the parasitic slotline (SL) mode and for biasing. Since the slotline mode is excited at many locations in the MMIC, the use of a large number of air bridges is inevitable. This means that the scattering behavior of the air bridges can play a significant role even if the parasitic effect of a single air bridge is relatively small.

Therefore, the scattering behavior of a commonly used type of air bridge is analyzed here including dielectric loss and conductor loss effects. The geometry of the bridge is shown in fig. 10. Due to the fabrication process, those metallizations which are located under the bridge usually have a small thickness t_b since this metallic layer is only evaporated and not strengthened by a plating process. Consequently, this leads to higher losses in these parts of the element.

Figure 11 shows the frequency behavior of the modulus of the reflection coefficient $|S_{11}|$ and the phase of the transmission coefficient $arg(S_{21})$ for the CPW mode. It can be seen that both $|S_{11}|$ and $arg(S_{21})$ show a linear behavior versus frequency. The reflection increases if the bridge length l_b is increased. A variation of the metallization thickness t_b under the bridge does not influence the reflection significantly as it is also indicated in figure 11. However, it is important to know that for $f = 100\ GHz$, $l_b = 40\ \mu m$ and $t_b = 0.2\ \mu m$, which are realistic MMIC dimensions, a reflection coefficient $|S_{11}| \approx 0.09$ (-21 dB) is reached. This demonstrates that the reflection may have a significant influence on the overall circuit performance.

Figure 12 presents an analysis of reflected power and ohmic loss in the device assuming that the incident wave corresponds to a

power of 100 %. Since the reflection coefficient is proportional to frequency, the reflected power is proportional to f^2. In contrast to this, the ohmic loss approximately shows a $\sqrt{f}$-behavior for frequencies $f > 10\ GHz$ due to skin effect (differences are due to the reduced size of the center conductor in which skin effect cannot be observed). It can be seen that the amount of insertion loss due to ohmic loss dominates over the reflected power, especially if realistically small values for t_b are assumed. Therefore, the ohmic loss of this circuit element should not be neglected (insertion loss $\approx 0.1\ dB$).

Figure 12 also presents the sum of ohmic loss and reflected power. This quantity is of interest since it represents the amount of input power which is lost on the transmission path. Obviously, its values are in the range of few percent. This means that in typical MMICs where many air bridges are used the circuit performance can be influenced in a noticeable way.

Due to the limited space, a model for air bridge type A cannot be presented here. However, such a model was already presented in [7]. For this model, the bridge is divided into homogeneous parts. These parts are then considered as transmission lines. Based on further field theoretical investigations, the inductance, the capacitance and the resistance of these transmission lines can be described by closed formulas. The power fractions which are obtained with such a model are compared with the FDFD results in fig. 12. A good agreement can be observed.

Circular right-angle bend

Fig. 13 shows the top-view of a circular CPW right-angle bend. In this case, the structure was analyzed neglecting both dielectric and metallic losses. This is justified because the attenuation does not differ significantly from that of a homogeneous CPW with the same length.

Furthermore, the main effect is different: If only the desired CPW mode is excited at one port of the bend, the parasitic slotline (SL) mode will occur at the other port, too. Obviously, a mode conversion between the two ports exists. This mode conversion which was calculated my means of the FDFD-method using a polygonal grid is shown in fig. 14 for different geometries of the CPW.

The observed mode conversion can be explained by a simple model. The excitation of the CPW mode can be described by two waves in the two slots which have the same phase. Assuming that the waves in the two slots propagate independently, a phase difference will occur at the other port due to the length-difference Δl of the two slots. If one considers the average length of each slot one gets $\Delta l = \frac{\pi}{2}(w+s)$ for the circular bend. If one introduces some further approximations, one obtains the following formula for the mode conversion:

$$|S_{SL2,CPW1}| \approx sin\left(\beta\frac{\Delta l}{2}\right) \qquad (2)$$

with

$$\beta = \frac{\omega}{c_0}\sqrt{\epsilon_{r,eff}}, \quad \epsilon_{r,eff} = \frac{\epsilon_r + 1}{2}$$

Due to the model, same values for $w+s$ lead to a quantitatively similar mode conversion. This is verified in fig. 14 for $w+s = 35\ \mu m$. Fig. 15 shows a comparison between the modeling formula (2) and the FDFD-simulation for different values of the center conductor width. One can see that the mode conversion can be mainly described by this approximation.

Conclusions

The Finite-Difference method in the frequency domain (FDFD) which had been shown to give reliable results for almost arbitrarily shaped structures was expanded in order to allow the analysis of structures with lossy materials. Furthermore, polygonal grids

were introduced in order to increase the efficiency for structures whose material contours do not match cartesian grid lines.

First, a homogeneous coplanar waveguide (CPW) was analyzed. The results were compared with a quasi-static analytical model [4]. The good agreement of the results shows that the extended FDFD-method is suitable for the full-wave analysis of lossy MMIC-structures.

The scattering behavior of different CPW discontinuities was analyzed afterwards. Physical effects could be observed which are already well known from homogeneous waveguides. For example, the overall inductance increases for decreasing frequencies due to a change in the magnetic field. For sufficiently high frequencies, the skin-effect leads to a $\sqrt{f}$-dependency of the ohmic resistance and a $1/\sqrt{f}$-dependency of the inner inductance. It was shown that the ohmic loss effects can influence the scattering behavior of the passive components significantly.

For the simple short end and the circular right-angle bend, simple modeling formulas could be given. For the analyzed air-bridge a model is available which could not be presented here due to the limited space of this paper. A good agreement between the models and the corresponding FDFD simulation was observed.

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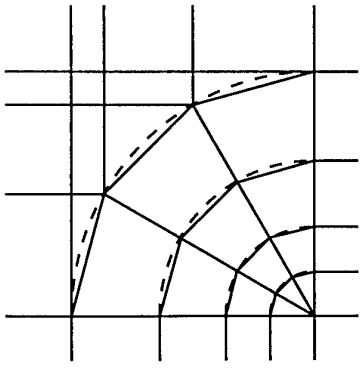

Figure 1: Polygonal grid for circular structures

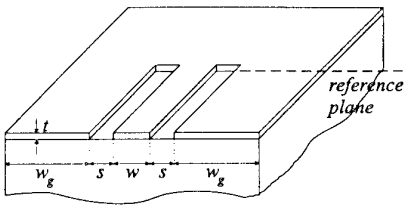

Figure 2: CPW short stub

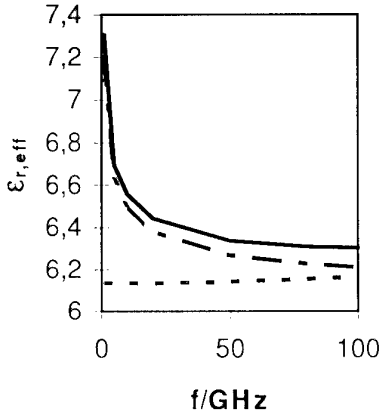

Figure 3: Relative effective permittivity
——— : FDFD
- - - - - : model [4]
· · · · · : FDFD, losses neglected

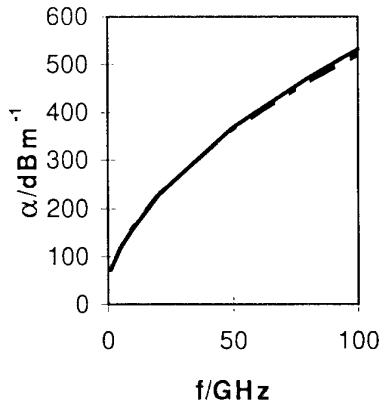

Figure 4: Attenuation constant
——— : FDFD
- - - - - : model [4]

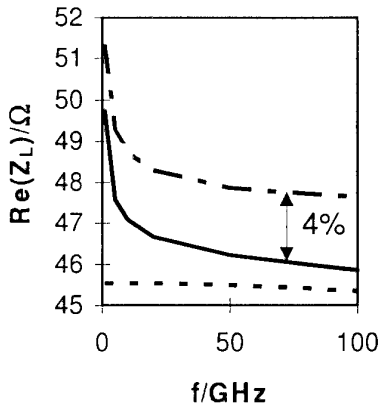

Figure 5: Real part of the characteristic impedance
——— : FDFD
- - - - - : model [4]
· · · · · : FDFD, losses neglected

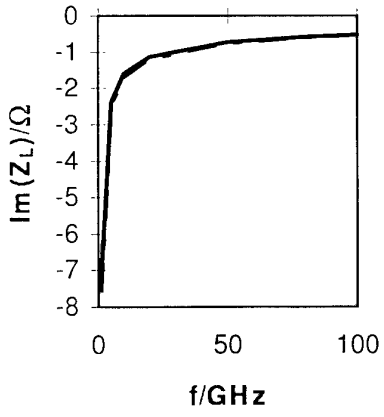

Figure 6: Imaginary part of the characteristic impedance
——— : FDFD
- - - - - : model [4]

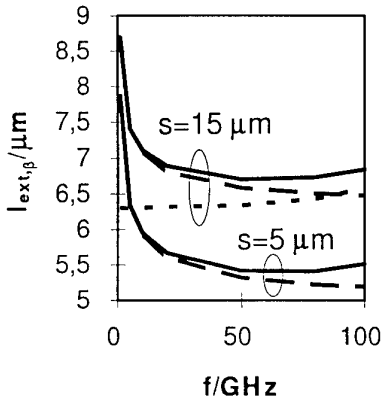

Figure 7: Length extension $l_{ext,\beta}$ for short stub
——— : FDFD
– – – – : modeling formula (1)
· · · · · : FDFD, losses neglected

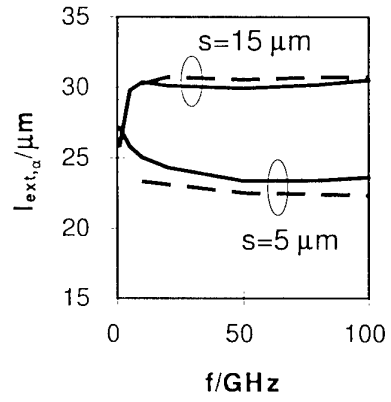

Figure 8: Length extension $l_{ext,\alpha}$ for short stub
——— : FDFD
– – – – : modeling formula (1)

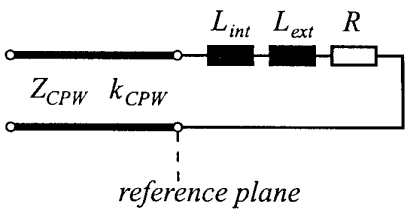

Figure 9: Equivalent circuit for the CPW short end

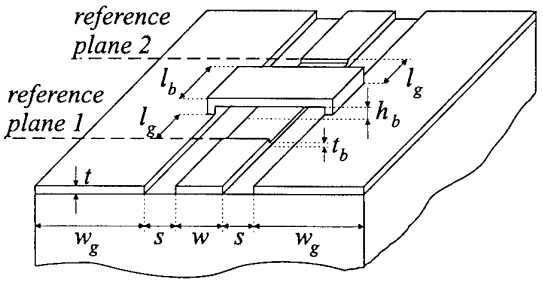

Figure 10: Air bridge type A

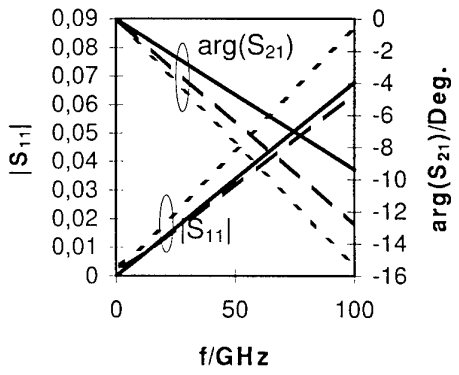

Figure 11: Scattering coefficients of air bridge type A
——— : $t_b = 3\ \mu m$, $l_b = 30\ \mu m$
– – – – : $t_b = 0.2\ \mu m$, $l_b = 30\ \mu m$, $l_g = 5\ \mu m$
· · · · · : $t_b = 0.2\ \mu m$, $l_b = 40\ \mu m$, $l_g = 5\ \mu m$

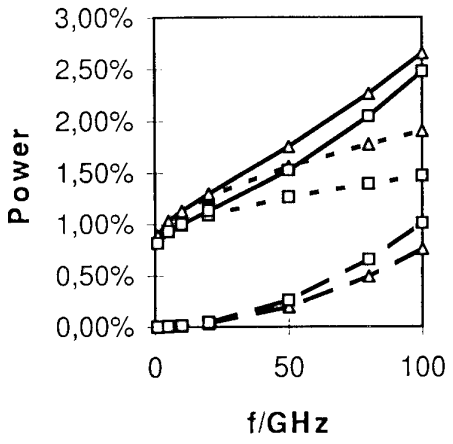

Figure 12: Reflected power and ohmic loss of air bridge type A ($l_b = 40\ \mu m$, $l_g = 5\ \mu m$, $t_b = 0.2\ \mu m$)

———	:	reflected power ($\|S_{11}\|^2$)
· · · · ·	:	ohmic loss $(1 - \|S_{11}\|^2 - \|S_{21}\|^2)$
- - - -	:	sum of both $(1 - \|S_{21}\|^2)$
△	:	FDFD
□	:	model

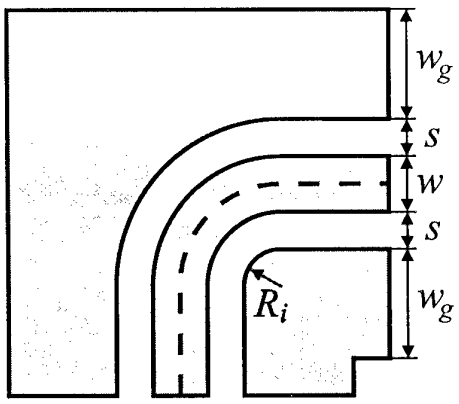

Figure 13: Circular CPW right-angle bend

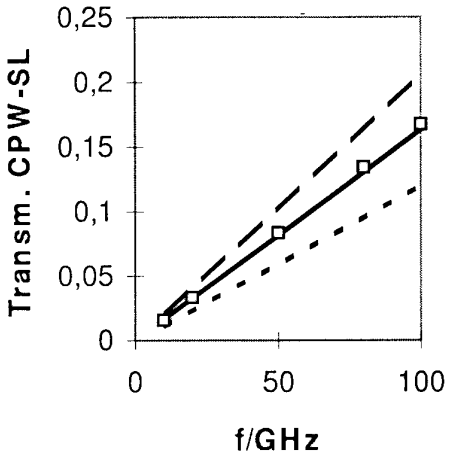

Figure 14: Mode conversion between the two ports ($R_i = 25\ \mu m$)

· · · · ·	:	$s = 10\ \mu m$, $w = 15\ \mu m$
———	:	$s = 10\ \mu m$, $w = 25\ \mu m$
- - - -	:	$s = 10\ \mu m$, $w = 35\ \mu m$
□	:	$s = 15\ \mu m$, $w = 20\ \mu m$

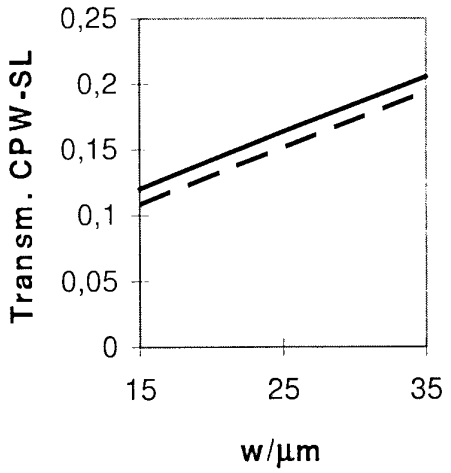

Figure 15: Mode conversion between the two ports ($f = 100\ GHz$, $s = 10\ \mu m$, $R_i = 25\ \mu m$)

———	:	FDFD
- - - -	:	modeling formula (2)

In-depth analysis of monolithic 12 GHz MESFET amplifier

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Abstract

In this paper, the discrepancy of simulated and measured response characteristics of a small-signal 12 GHz MMIC amplifier in the GEC F20 technology [14] is analysed in detail. To this end, the used 4x75µm 0.5µm MESFET was extensively modelled using and contrasting various extraction methods for the intrinsic and extrinsic elements. A table-based large-signal model [3] was also derived and verified with waveform measurements. It is found, that with the precise model of the active device we employed, the overall accuracy is severely limited by inadequacies of the models for the passive components [1], especially in the non-linear case.

I. Introduction

The specific advantages of monolithic circuits in high frequency applications with respect to cost, reliability and performance are well known. Since a post-production tuning of MMICs is not possible as with hybrid circuits, the design has to be fully CAD-oriented [1]. Optimisations for gain or input/output matching do not longer need experimental iterations, but are fully integrated into modern design software. To this end, a vast number of passive and active devices needs to be characterised and reliably modelled.

"Right first time" designs give a competitive advantage in time to market, and are nowadays nearly taken for granted for linear applications using established technologies with gate lengths above 0.3 µm [2]. This, however, is not the case for more recent, sometimes still experimental technologies (0.1-0.15µm), especially when characterisation data is sparse.

In this project, we have designed a small-signal 12 GHz monolithic amplifier (Fig. 1) in the GEC F20 technology [14], together with test structures of the transistor (Fig. 3) and the passive matching networks. The active device was extensively characterised and precisely modelled. Various methods were applied to accurately determine the extrinsic elements, as well as to extract the intrinsic elements of the standard 15 element small-signal equivalent model. From the bias-dependent small-signal equivalent circuit we then derived a table-based dispersive large-signal model [3]. By comparing it in harmonic-balance simulations to large-signal waveform measurements [4] we were able to prove its correctness.

The measured characteristics of this first-iteration amplifier did not fit well the design specification for the input reflection factor. Using a "divide and conquer" method to locate the fault, we have characterised and modelled the subcircuits and the transistor. Initially suspecting the active device, we have modelled it carefully and proved that the foundry's transistor model used in the design phase was correct.

A following rigorous analysis of the passive component library has revealed that the reason for failing the small-signal specifications was an erroneous capacitor model. While the amplifier was primarily developed for small-signal applications, we have also investigated its non-linear characteristics. For reliable large-signal

simulations we have shown that it is essential to employ passive models that are valid up to the highest occuring harmonics [1]. In the context of harmonic balance simulations, it is insufficient to have passive models that are only applicable up to their self-resonance frequencies or the transit frequency of the related transistor technology.

II. Amplifier design

The monolithic amplifier was designed to yield a maximal, yet stable gain, while being matched to 50 Ω at both input and output. Since the transistor is not absolutely stable at the design frequency of 12 GHz, an approach similar to Edwards et al. [5] was used to obtain initial source- and load-reflection factors. Reactive matching networks were synthesised with ideal capacitors and inductors, since distributed elements are prohibitively large at this frequency. They were consequentially replaced within the simulator environment by the foundry models for the real elements, that include the parasitics. Their final dimensions were obtained via optimisation to meet the design specification, and differed markedly from the ideal values. The determination of the right number of turns for the inductors was especially challenging, since integer numbers can not be optimised. The $1mm^2$ small layout of the 1-stage amplifier with integrated matching and bias-network is given in figure 1.

III. Extraction of the extrinsic elements

Using the EuroPractice multi-project wafer programme, we have produced a quantity of 40 amplifiers and transistors. DC-characterisations revealed that the threshold voltage varied significantly between them, viz. up to 0.4V between devices from different wafers. An amplifier/transistor pair coming from the same wafer and reticule and that had similar DC-characteristics was selected for further examination.

The extrinsic elements of the used small-signal equivalent circuit (Fig. 2) are supposed to be bias-independent. The parasitic capacitances and inductances can be related to the pad capacitance and the microstrip line inductance of the embedding circuitry (Fig. 3). S-parameters were measured on-wafer up to 40 GHz using GSG-probes.

Four different methods were applied to obtain approximate values for the extrinsic elements. They are all based on "cold" (V_{DS} = 0V) S-parameter measurements with V_{GS} being biased either for gate-forward conduction or for complete pinch-off. The extraction results (Table 1) differ significantly, since the approaches are based on different bias points and assumptions.

Dambrine's method

The classic method proposed by Dambrine et al. [6] extracts the series inductances and resistances from forward-bias measurements, and the parallel capacitances from pinch-off measurements. The parasitic capacitances are overestimated by this method, as is well known [7-10], since it ignores C_{ds} next to setting C_{gs} = C_{gd} in its pinch-off equivalent circuit.

Since the cold device is reciprocal, only three equations are obtained to determine the four resistances R_s, R_d, R_g and the channel resistance R_{ch}. Here we followed an approach only valid for short gate length HEMTs [11], in that we assumed R_{ch} to be very small and set it to zero [8]. This leads, of course, to overestimated resistances values.

Yanagawa's method

The method proposed by Yanagawa et al. [12] omits the parasitic capacitances completely, and derives the remaining extrinsic elements solely from pinch-off data. The advantage is that the gate-forward measurements can be avoided, that might deteriorate the device. The bond pad capacitances can be neglected if they are much smaller than the intrinsic capacitances, which is only the case for medium- or high-power transistors with large gate peripheries. The infringement of this condition is reflected most obviously in the non-physical value obtained for the source inductance L_s.

Lin's method: starting values

In the multi-bias algorithm proposed by Lin and Kompa [13], starting values for the extrinsic elements are obtained solely from pinch-off data as in Yanagawa's method, but with the parasitic capacitances included here. In the simplex-algorithm the two capacitances are optimised while the remaining internal T-structure is calculated. The inductance values obtained are more consistent with Dambrine's method when compared to the values given by Yanagawa's method.

The resistance values obtained with Lin's and Yanagawa's methods are similar, since both methods extract from pinch-off data. However, since the resistive part of the Z-parameters is much smaller than the reactive one at this biasing situation, it is difficult to precisely determine the series resistances. In particular, the value obtained here for the source resistance R_s is lower than the estimated contact resistance.

The parasitic capacitances estimated with Lin's method are much smaller than the overestimated values obtained with Dambrine's method. Even though both methods are based on the same pinch-off measurement, this is not surprising, since Lin's method does not simplify the intrinsic capacitances.

Lin's method: multi-bias optimisation

After determination of initial estimates for the extrinsic elements, the multi-bias algorithm [13] optimises these eight elements for several bias points simultaneously. Here, the optimisation was done to fit the S-parameter from one cold pinch-off bias point and two saturation bias points.

The multi-bias results are very reasonable. The device's symmetry is reflected in the similarity of L_g and L_d, R_s and R_d, and C_{pg} and C_{pd}. The inductance values are near to the ones extracted from gate-forward measurements. The resistances R_s and R_d are larger than the estimated contact resistance, while R_g is just about the value given by the foundry [14]. The parasitic capacitance value is supported by the foundry's model for the contact pad.

IV. Extraction of the intrinsic elements

Once the extrinsic elements of the 15-element equivalent circuit model (Fig. 2) are known, the intrinsic elements can be calculated using different methods. In this paragraph, the extrinsic elements determined beforehand with the multi-bias method are used. Three analytical methods [15, 16, 6] were applied to calculate the intrinsic elements as a function of frequency (and for each bias point).

Berroth's equations [15]

The equations proposed by Berroth and Bosch in 1991 [15] are the most complete, as they include the diode conductivities as well as the resistance R_{gd} in addition to the standard 15-element equivalent circuit (Fig. 2).

Figure 4 shows the calculated element values as a function of frequency for a typical class A amplifier bias point. Two topologies for the parasitic reactive elements are contrasted: one is as in Fig. 2, the other has the parasitic inductances and capacitances interchanged. Since the extrinsic elements were determined for the topology given in Fig. 2, the intrinsic elements calculated for this topology are much less variable with frequency (broken line in Fig. 4).

All intrinsic elements (the output conductance G_{ds} to a lesser degree) are very constant with frequency, which is an indication of the usefulness of the values of the extrinsic elements. The resistive elements R_i and R_{gd} are difficult to determine at low frequencies, since the angle and magnitude uncertainties in the S_{11} and S_{22} parameters are translated into a high uncertainty in the real part of the Z-parameters. Therefore, the average value is taken omitting the values calculated for the elements below 5 GHz.

Since the resistance R_{gd} is in series with the small feed-back capacitance C_{gd}, it has of all the equivalent circuit elements the smallest influence on the measured S-parameters. Therefore, its

determination is very delicate. Here, non-physical negative and frequency dependent values were obtained.

Berroth's earlier equations [16]

In an earlier publication, Berroth and Bosch did not yet include the diode conductivities nor R_{gd}. The intrinsic elements as determined with these equations are given in Table 2 for a typical saturation bias point. For such bias points, were no gate-forward current appears, the values obtained are practically identical to those from the complete equations in [15]. Since with [15] R_{gd} can not be sharply determined in our case, the complete equations do not bring any particular advantage here.

The S-parameters of the equivalent circuit from Fig. 2 with the element values from Tables 1 and 2 were calculated and are given in Fig. 5 together with the measured data. The agreement is very satisfying up to K-band. The observed behaviour at higher frequencies can be reproduced when a more complex extrinsic network is used to model the via holes and the distributed nature of the lines as well [17].

Dambrine's equations [6]

The equations proposed by Dambrine et al. were additionally used, since they were the historic basis of Berroth's and Bosch's work. Dambrine et al. use some low frequency approximations in their equations, which lead as a consequence to more frequency dependent intrinsic element values. Therefore, the values have to be averaged on the lower part of the frequency band (here less than 10 GHz). As explained above, R_i has to be treated separately, since it can be accurate determined only for frequencies above 5 GHz. The values determined such differ from Berroth's values by up to 5%.

V. Large-signal model

Once all the equivalent circuit elements are known for every bias point, the underlying state functions can be determined using path integrals [18]. Since the physical dependence of the state functions is on the voltages at the intrinsic planes, the bias dependent intrinsic elements have first to be represented in data tables as a function of the internal voltages.

The large-signal model used here (see [3] for a detailed description) is table-based and includes low-frequency dispersion as well as temperature-sensitive diodes. It is implemented in a commercial CAD tool and applicable in harmonic balance simulations.

Large-signal measurements

The transistor has been measured on wafer under large-signal excitations using an advanced waveform measurement set-up [4] based on the microwave transition analyser HP 71500A. It allows to simultaneously measure amplitude and phase of the fundamental frequency and its harmonics. Sweeps have been made with respect to gate-bias, fundamental frequency, and input power.

Verification of large-signal model

Figure 6 contains the measured and simulated waveforms of voltages and currents at the gate and drain for one exemplary situation. The agreement is quite satisfying when considering that the modelled and the measured transistor were from different wafers. The gate forward conduction that limits V_{GS} and I_{DS} is very well reproduced by the model due to the implementation of the gate-source and gate-drain diodes. The good overall agreement between simulation and measurement proves the correctness of the various steps in the modelling procedure.

Passive component model frequency range

The reason for the remaining slight discrepancies are very likely to be found in the uncertainty of the higher harmonic terminations to the non-linear device's input and output. Within the harmonic balance simulation, a number of seven harmonics has been chosen, which corresponds to a maximal simulation frequency of 84 GHz. Clearly, for precise non-linear high frequency modelling, the passive component models have

to be valid up to the highest occuring harmonic, which, however, is still generally not the case [1].

VI. Amplifier performance

The measured performance of the amplifier is given in Fig. 7 (boxes). Its behaviour with respect to the input match at the design frequency 12 GHz is out of the specifications. Since the previous work has proved that the active device is correctly modelled, the passive networks were then examined in more detail. Using a "divide and conquer" method, the fault was located in an erroneous capacitance model used during the design phase.

Fig. 7 shows good agreement between measurements and simulations using the large-signal model for all four S-parameters. The apparent loop in the simulated S_{22} at about 35 GHz is due to the indetermined impedance at the drain bias voltage supply port.

VII. Conclusion

In this paper we have elucidated various methods to extract the small signal equivalent circuit of a transistor. The results obtained were carefully contrasted for both the extrinsic and intrinsic elements. An advanced large-signal dispersive table-based model was finally derived and verified on the basis of transistor large-signal measurements as well as in the analysis of an MMIC amplifier. The precise modelling also of the passive components has been shown to be important for the overall simulation reliability.

Acknowledgements

We should like to thank our colleague Dr. van Raay for his kind support with the large-signal measurements.

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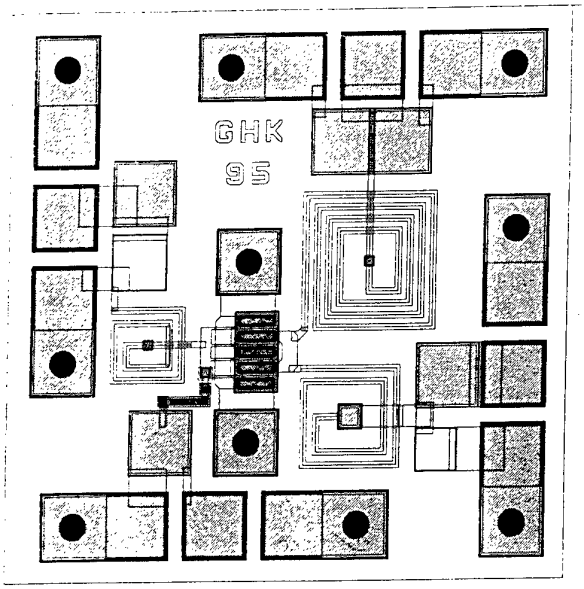

Fig. 1 Layout of the 12 GHz GEC F20 amplifier (scale 1:75)

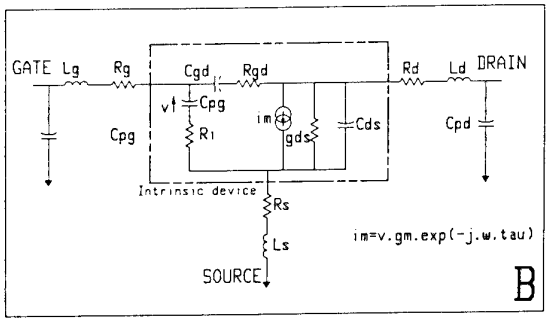

Fig. 2 Used small-signal equivalent circuit of the MESFET

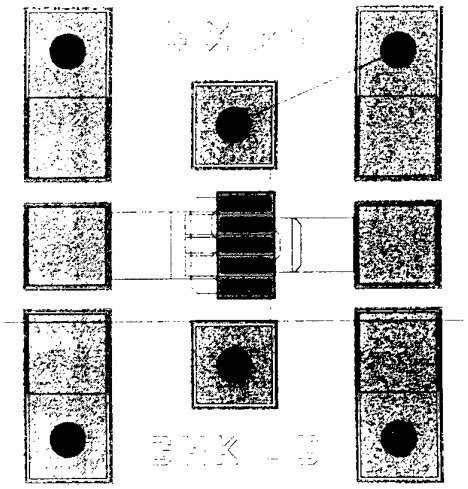

Fig. 3 Layout of the 4x75µm 0.5µm GEC F20 MESFET (1:100)

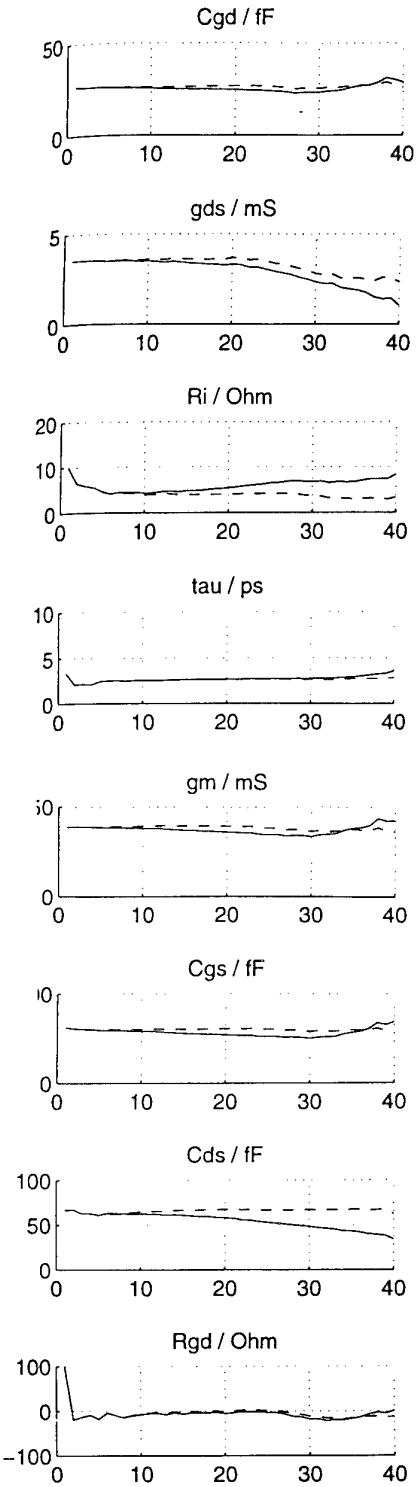

Fig. 4 Intrinsic element values vs. frequency using equations proposed in [15] (Broken line: topology as in Fig. 2, continuous line: position of parasitic inductances and capacitances interchanged, V_{DS} = 5 V, V_{GS} = -0.3 V)

	Dambrine [6]	Yanagawa [12]	Lin [13]	
			starting values	multi bias results
Inductances	forward-bias	pinch-off	pinch-off	multiple biases
L_g	101 pH	72 pH	97 pH	102 pH
L_s	4.5 pH	-9.2 pH	0.5 pH	7.0 pH
L_d	102 pH	61 pH	82 pH	88 pH
Resistances	forward-bias	pinch-off	pinch-off	multiple biases
R_g	1.4 Ω	2.1 Ω	2.5 Ω	1.67 Ω
R_s	4.7 Ω	0.53 Ω	0.80 Ω	1.99 Ω
R_d	5.2 Ω	2.5 Ω	2.6 Ω	2.06 Ω
Capacitances	pinch-off		pinch-off	multiple biases
C_{pg}	88 fF	omitted	38 fF	44 fF
C_{pd}	95 fF		29 fF	40 fF

Table 1 Summary of the extraction of the extrinsic elements

C_{gd}	C_{gs}	C_{ds}	R_i	G_m	G_{ds}	τ
(fF)			(Ω)	(mS)		(ps)
26	303	65	4.03	39.3	3.57	2.59

Table 2 Intrinsic element values calculated using [16] (V_{DS} = 5 V, V_{GS} = -0.3 V)

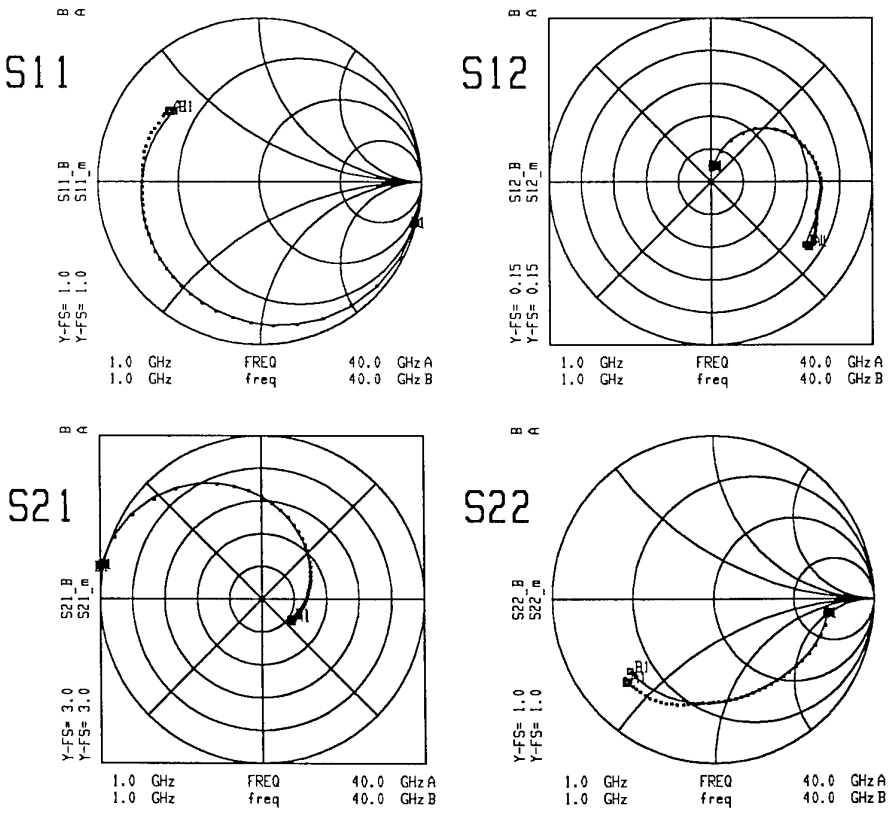

Fig. 5 S-parameters of the 4x75µm MESFET from 1 to 40 GHz in 1 GHz steps (V_{DS} = 5 V, V_{GS} = -0.3 V) Measurements: dots, Simulation with values extracted according to [16]: lines

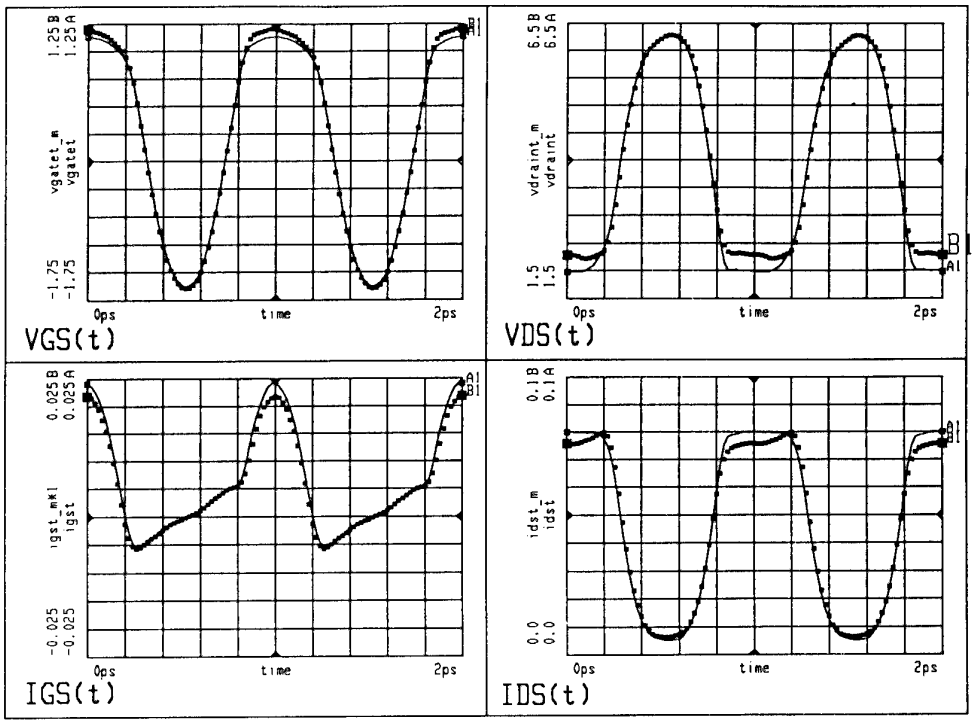

Fig. 6 Waveforms of voltage and current at the gate and drain of the GEC 4x75 μm MESFET (V_{DS} = 4 V, V_{GS} = 0 V, f_0 = 1 GHz, P_{in} = 10 dBm)
Measurements: dots, Simulations: lines

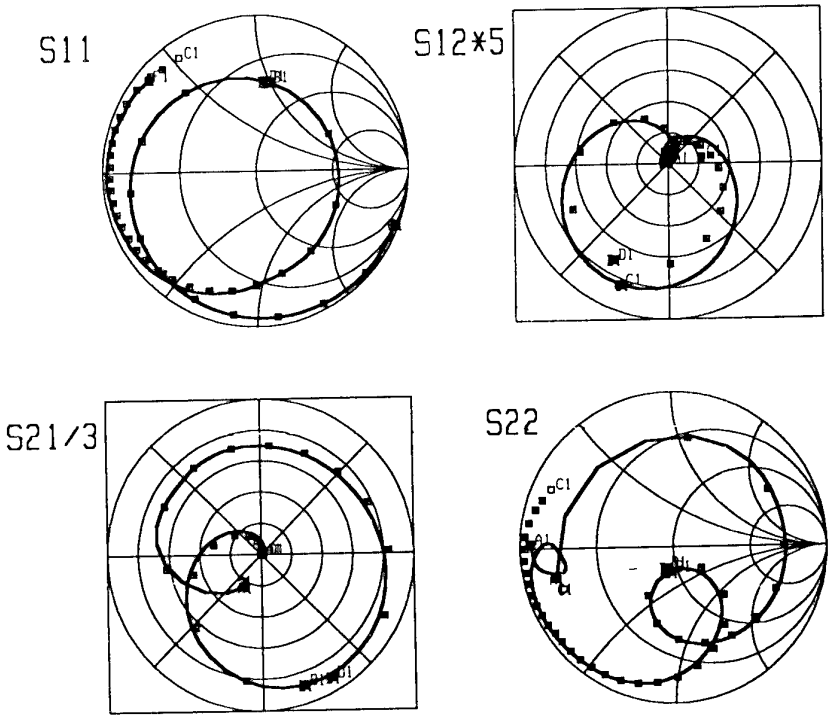

Fig. 7 S-parameters of the amplifier from 1 to 40 GHz in 1 GHz steps with markers added at 12 GHz (V_{DS} = 5V, V_{GS} = -0.3V)
Measurements: boxes, Simulations with large-signal model: lines

AN ANALYTICAL MODELPARAMETER EXTRACTION PROCEDURE FOR GaAs FETs BASED ON LEAST SQUARES APPROXIMATION

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ABSTRACT

An analytical procedure for determining **all** the small-signal equivalent circuit elements of GaAs FETs under active bias conditions has been developed. The extraction problem is first considered as a fitting problem which is analytically solved using the method of least squares by modeling the measured data using rational functions. The equivalent circuit elements are then directly calculated from coefficients of the rational functions. First extraction results show very good agreement between measurement and simulation.

I. INTRODUCTION

Accurate small-signal parameter extraction of microwave FET models is an essential tool for reliable nonlinear device modeling and microwave circuit design [1]. Numerous methods have been proposed for extraction of the model parameters. These methods can be broadly classified into optimization e.g. [2] and cold/hot modeling techniques [3], [4]. The limitations of both approaches such as non-unique solutions for optimization based techniques, the critical gate forward bias operation and the parasitic MESFET operation for HEMTs for cold/hot modeling approaches are still points of discussion [5], [6]. While the former methods can be used on „hot" S-parameters, the physical relevance of the extracted values, especially the parasitic resistances is still an open question. The latter method does not correspond to the actual operating conditions and assumes, in addition, that all the parasitic resistances are constant.

A semi-analytical extraction procedure at active bias conditions was recently proposed to circumvent limitations of the standard approaches [7]. The method requires only one optimization variable to first of all determine the series resistance Rs. The other elements are then sequentially derived. Approaches to develop a fully analytical model element extraction procedure at hot operating points have been investigated [8]. Theoretical considerations considering an FET equivalent circuit as having only two linear independent terminal current-voltage relations result in a system of ill-conditioned equations. This requires highly accurate measurement and broadband characterization techniques to yield useful extraction results.

Extraction on the basis of rational function approximation of the measured S-parameters using the method of least squares was to the best of the authors knowledge first reported by Nagatomo et. al. [9]. By empirically determining the order of numerator and denominator of the rational functions, measured S-parameters could be accurately reproduced. However, an extraction procedure based on their approach requires many assumptions such as the parasitic resistances being much smaller than Z_0, the normalizing impedance of the S parameters, usually 50 ohms. The intrinsic elements are approximated from the extracted coefficients and serve as the starting vector for an optimization routine.

This paper reports on an analytical extraction procedure for determining **all** the equivalent circuit elements of a GaAs FET at active bias conditions. The approach redefines the model element extraction problem by first using the method of least squares to fit the chosen

equivalent circuit topology, defined explicitly by its S-,Y-, or Z-parameters as rational functions of frequency, to the measured data. The numerators and denominators of the rational functions are of known orders and the coefficients are known explicitly in terms of the equivalent circuit elements. Individual elements can then be easily determined from the coefficients of the rational functions directly. Alternatively, by taking advantage of the chosen topology, extraction of the parasitics reduces to simple polynomial division.

II. PROBLEM DEFINITION AND FORMULATION OF THE SOLUTION

Let a frequency dependent measured parameter $C(j\omega)$ be expressible as a rational function as given in eqn. 2.1.

$$C(j\omega) = \frac{A(j\omega)}{B(j\omega)} \qquad (2.1)$$

where

$$A(j\omega) = \sum_{i=0}^{M} \alpha_i (j\omega)^i \qquad \text{and}$$

$$B(j\omega) = 1 + \sum_{j=1}^{N} \beta_j (j\omega)^j \qquad (2.2)$$

are polynomials in frequency, $j\omega$.

The first aim of modeling is to determine the set of coefficients, $\{\alpha_i\}$and $\{\beta_j\}$, such that the rational functions represent the measured data. This can be done using least squares formulation as follows: Using eqn. (2.1), an error function, $\varepsilon(j\omega_f)$, can be defined over all the measured frequencies, ω_f, using the method of least squares as follows

$$\varepsilon = \sum_{\omega_f} \left| A(j\omega_f) - B(j\omega_f) C(j\omega_f) \right|^2 \qquad (2.3)$$

The coefficients $\{\alpha_i$ and $\beta_j\}$ which minimize ε can be solved by simultaneously solving eqn (2.4) and eqn. (2.5).

$$\frac{\partial \varepsilon}{\partial \alpha_m} = 0 \qquad (2.4)$$

$$\frac{\partial \varepsilon}{\partial \beta_n} = 0 \qquad (2.5)$$

After numerous algebraic manipulations, eqn. (2.4) and eqn. (2.5) can be re-written as follows

$$\sum_{\omega_f} \begin{bmatrix} \left(\mathrm{Re}\sum_{i=0}^{M}\left[(j\omega_f)^i(-j\omega_f)^m\right]\right) & -\left(\mathrm{Re}\sum_{j=1}^{N}\left[C(j\omega_f)^j(-j\omega_f)^m\right]\right) \\ \left(\mathrm{Re}\sum_{i=0}^{M}\left[(j\omega_f)^i(-j\omega_f)^n C^*\right]\right) & -\left(\mathrm{Re}\sum_{j=1}^{N}\left|C\right|^2\left[(j\omega_f)^j(-j\omega_f)^n\right]\right) \end{bmatrix} \begin{bmatrix} \alpha_i \\ \beta_j \end{bmatrix}$$

$$= \sum_{\omega_f} \begin{bmatrix} \mathrm{Re}\, C\left[(-j\omega_f)^m\right] \\ \mathrm{Re}\left|C\right|^2\left[(-j\omega_f)^n\right] \end{bmatrix} \qquad (2.6)$$

Equation (2.6) is a system of linear equations which can be analytically solved to yield the required coefficients. By carefully choosing the form of the measured parameter, for GaAs FETs either S-, Y- or Z-parameters, and/or appropriately scaling the frequency, a system of well-conditioned equations can be obtained and a precise determination of the coefficients is possible. It can also be noticed that this system of equations consists of only real parts of different expressions involving the measured parameter and frequency. This can be utilized to minimize numerical noise thereby improving the accuracy in determining the coefficients.

III. EXTRACTION PROCEDURE

The determination of the model parameter elements is done sequentially. First of all, the parallel parasitic capacitances are calculated and de-embedded from the measured data. Next, the series parasitics are calculated and also de-embedded. The intrinsic elements are then calculated using hot modeling [1]. In the second step, it is also possible to directly calculate the intrinsic elements instead of using hot modeling. In both the steps, the measured or de-embedded (measured) data is represented by a set of calculated coefficients from which the model elements are evaluated.

A description of the procedure used to determine the series parasitics and the intrinsic FET is first presented since the rational functions used to determine the parasitic capacitances have many and very long expressions of the coefficients and not suitable for illustrating the concept. Consider now the common equivalent circuit for a GaAs FET shown in Fig. 1. After the parallel parasitic capacitances are determined and de-

embedded, the measured data is converted to Z-parameters and the corresponding coefficients of the rational functions determined using the algorithm given in sec. 2

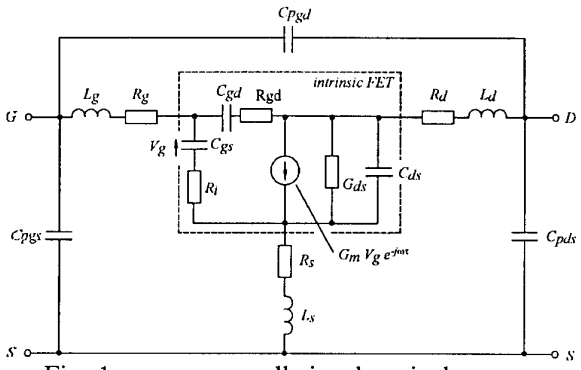


Fig. 1: common small-signal equivalent circuit of a GaAs FET

The coefficients are related to the circuit elements as follows: The Z parameters of the rest of the circuit are derived using circuit analysis yielding

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} Z_g + Z_s + \frac{Y_{ds}+Y_{gd}}{\Delta Y} & Z_s + \frac{Y_{gd}}{\Delta Y} \\ Z_s + \frac{Y_{gd}-Y_{gm}}{\Delta Y} & Z_d + Z_s + \frac{Y_{gs}+Y_{gd}}{\Delta Y} \end{bmatrix} \quad (3.1)$$

where

$$Y_{gs} = \frac{1}{R_i + \frac{1}{j\omega C_{gs}}} \quad (3.2)$$

$$Y_{gd} = \frac{1}{R_{gd} + \frac{1}{j\omega C_{gd}}} \quad (3.3)$$

$$Y_{gm} = \frac{G_m e^{-j\omega\tau}}{1 + j\omega R_i C_{gs}} \quad (3.4)$$

$$Y_{ds} = \frac{1}{R_{ds}} + j\omega C_{ds} \quad (3.5)$$

$$\Delta Y = (Y_{gs} + Y_{gd})(Y_{ds} + Y_{gd}) + Y_{gd}(Y_{gm} - Y_{gd}) \quad (3.6)$$

By subtracting Z_{12} from Z_{11}, Z_{21} and Z_{22} gives the following compact matrix

$$\begin{bmatrix} Z_{11} - Z_{12} & Z_{12} \\ Z_{21} - Z_{12} & Z_{22} - Z_{12} \end{bmatrix} = \begin{bmatrix} Z_g + \frac{Y_{ds}}{\Delta Y} & Z_s + \frac{Y_{gd}}{\Delta Y} \\ \frac{-Y_{gm}}{\Delta Y} & Z_d + \frac{Y_{gs}}{\Delta Y} \end{bmatrix} \quad (3.7)$$

The exponential term in eqn. 3.4 can be approximated by the first two terms of its power series expansion allowing a complete description of the derived equations as rational functions of frequency. All the steps can be evaluated symbolically with the help of a mathematical software package such as MATHEMATICA [11] to explicitly determine the coefficients of the resulting rational functions. For example, Z_{12} can be explicitly written as

```
Z12 = (Cgd*Rds + Cgd*Rs + Cgs*Rs +
Cgd*Gm*Rds*Rs + Cgd*Ls*x + Cgs*Ls*x
+ Cgd*Gm*Ls*Rds*x +
Cgd*Cgs*Rds*Ri*x + Cds*Cgd*Rds*Rs*x
+ Cds*Cgs*Rds*Rs*x +
Cgd*Cgs*Rds*Rs*x + Cgd*Cgs*Rgd*Rs*x
+          Cgd*Cgs*Ri*Rs*x -
Cgd*Gm*Rds*Rs*Tau*x +
Cds*Cgd*Ls*Rds*x^2 +
Cds*Cgs*Ls*Rds*x^2 +
Cgd*Cgs*Ls*Rds*x^2 +
Cgd*Cgs*Ls*Rgd*x^2 +
Cgd*Cgs*Ls*Ri*x^2 +
Cds*Cgd*Cgs*Rds*Rgd*Rs*x^2 +
Cds*Cgd*Cgs*Rds*Ri*Rs*x^2 -
Cgd*Gm*Ls*Rds*Tau*x^2 +
Cds*Cgd*Cgs*Ls*Rds*Rgd*x^3 +
Cds*Cgd*Cgs*Ls*Rds*Ri*x^3)/        (Cgd
+ Cgs + Cgd*Gm*Rds + Cds*Cgd*Rds*x
+ Cds*Cgs*Rds*x + Cgd*Cgs*Rds*x +
Cgd*Cgs*Rgd*x + Cgd*Cgs*Ri*x -
Cgd*Gm*Rds*Tau*x +
Cds*Cgd*Cgs*Rds*Rgd*x^2 +
Cds*Cgd*Cgs*Rds*Ri*x^2)                (3.8)
```

whereby $x = j\omega$.

Note that in this case the degree of the numerator and denominator polynomials is 3 and 2 respectively, and the polynomial coefficients are explicitly expressed in terms of the equivalent circuit elements. Therefore, by setting M=3 and N=2 and applying eqn. (2.6) on the measured Z_{12}, coefficients having a one-to-one correspondence to products of equivalent circuit elements can be calculated. All the measured 4 parameters in eqn. (3.7) are usually simultaneously considered using a correspondingly expanded version of eqn. (2.6). An analytical derivation of all the individual equivalent circuit elements from the coefficients of eqn. (3.7) is given in the appendix 1.

A somewhat more straightforward extraction is based on the fact that given two polynomials p(x) and q(x), one can always uniquely write

$$\frac{p(x)}{q(x)} = a(x) + \frac{b(x)}{q(x)} \qquad (3.9)$$

where the degree of b(x) is less than the degree of q(x). Analyzing eqn. (3.1) or (3.7) shows that the series impedances can be analytically evaluated on the basis of polynomial division, whereby a(x) corresponds to the parasitic impedances. Coming back to the parasitic capacitances, the Y-parameters of the complete equivalent circuit can also be written in the form of eqn. (3.9) whereby a(x) again corresponds to $x(C_{pgs} + C_{pgd})$, $x(C_{pds} + C_{pgd})$ and $-xC_{pgd}$. The intrinsic elements could then be evaluated analytically using hot modeling.

IV. RESULTS AND DISCUSSION

Extraction software is under development using the commercial mathematical software package, MATLAB [10]. The described extraction procedure was first validated using fictitious S-parameter data and has now been tested on measured MESFET and HEMT S-parameter data. Simulated data show that measured microwave FET data can accurately be reproduced using rational functions determined on the basis of least squares approximation. Fig. 2 shows excellent agreement between measured and modeled S-parameters (1-40 GHz) for a 0.5x2x150 μm GaAs MESFET. The modeled parameters have been calculated from coefficients of the rational functions. This is an alternative to using measured data directly in circuit design since it requires only a few coefficients (33 coefficients for the Y-parameter representation) to completely characterize the microwave behaviour of a device. In addition, the least squares formulation results in smoothed curves as compared to discrete measured data.

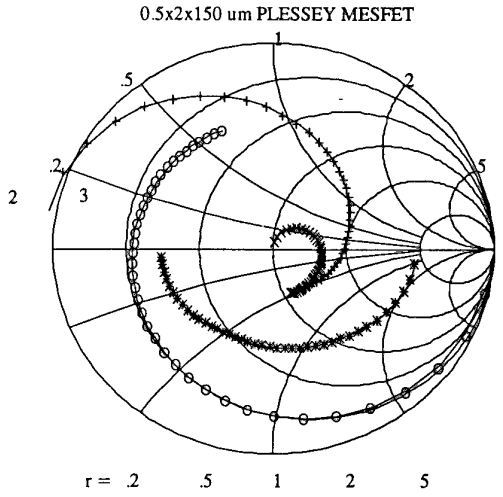


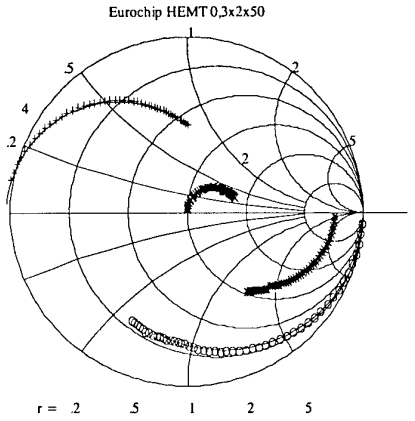
Fig. 2: Measured and Modeled S-parameters (1-40 GHz) for a 0.5x2x150 μm GaAs MESFET, V_{GS}=-0.4V, V_{DS}=3.0V. Crosses/Circles: measured values; lines: simulated values using the calculated coefficients.

First extraction results for on-wafer S-parameter measurements of a 0.5x2x150 μm GaAs MESFET (Plessey) and a 0.3x2x50 μm doubled pulse doped quantum well heterostructure FET, DPD-QW-HFET (HEMT), are given in table 1. Fig. 3 shows a comparison between measured and simulated S-parameters. Good agreement between measurement and simulation can be seen. Furthermore, the values of the extracted elements, in particular the parasitic resistances, seem to agree quite well with their physical basis.

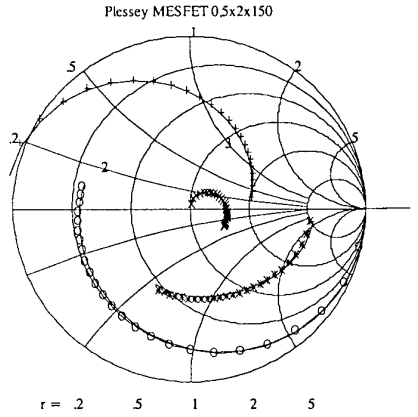
TABLE 1
EQUIVALENT CIRCUIT ELEMENTS

Element	0.5x2x150 μm MESFET Vds=3.0V, Vgs=-0.4V	0.3x2x50 μm HEMT Vds=2.0V, Vgs=0V
Cpgs (fF)	24.144	-
Cpds (fF)	21.481	-
Cpgd (fF)	0.9945	-
Rg (Ω)	7.8357	6.7612
Rd (Ω)	3.0294	3.3751
Rs (Ω)	1.8506	2.8005
Lg (pH)	157.2	32.217
Ld (pH)	176.4	6.8118

Ls (pH)	2.4	0
Cgs (fF)	282.61	145.29
Cgd (fF)	23.631	19.463
Cds (fF)	72.552	30.107
Ri (Ω)	1.6711	1.1294
Rgd (Ω)	0	27.412
Gds (mS)	3.7711	2.0723
Gm (mS)	40.12	51.398
τ (pS)	1.9307	0.90434



(a)



(b)

Fig. 3: A comparison of measured and modeled S-parameters (1-26 GHz). Crosses/Circles: measured values; lines: simulated values using the equivalent circuit.

V. CONCLUSIONS

A procedure for analytically determining all elements of a GaAs FET at active bias conditions has been described. The extraction problem is first of all considered as a fitting problem which is analytically solved using the method of least squares by modeling the measured data using rational functions. The equivalent circuit elements are then directly calculated from coefficients of the rational functions. First extraction results show that this approach results in excellent fitting of the measured parameters, gives physically meaningful equivalent circuit elements and seems to overcome many limitations associated with present extraction techniques. Further work should establish optimum choice of measured parameters and frequency scaling for reliable extraction.

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APPENDIX 1

The coefficients of the Zij polynomials are as follows:

Z11

$$\frac{1}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_0^{11}$$

$$R_g + \frac{C_{ds}R_{ds}+C_{gd}R_{gd}+C_{gs}R_i}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_1^{11}$$

$$L_g + b_1 R_g + \frac{C_{ds}R_{ds}C_{gd}R_{gd}+C_{ds}R_{ds}C_{gs}R_i+C_{gd}R_{gd}C_{gs}R_i}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_2^{11}$$

$$b_1 L_g + b_2 R_g + \frac{C_{ds}R_{ds}C_{gd}R_{gd}C_{gs}R_i}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_3^{11}$$

$$b_2 L_g = a_4^{11}$$

Z12

$$R_s + \frac{C_{gd}R_{ds}}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_0^{12}$$

$$L_s + b_1 R_s + \frac{C_{gd}R_{ds}C_{gs}R_i}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_1^{12}$$

$$b_1 L_s + b_2 R_s = a_2^{12}$$

$$b_2 L_s = a_3^{12}$$

Z21

$$\frac{g_m R_{ds}}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_0^{21}$$

$$\frac{C_{gd}g_m R_{ds}R_{gd}+C_{gs}g_m R_{ds}R_i - g_m R_{ds}\tau}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_1^{21}$$

$$\frac{C_{gd}C_{gs}g_m R_{ds}R_{gd}R_i - C_{gd}g_m R_{ds}R_{gd}\tau - C_{gs}g_m R_{ds}R_i\tau}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_2^{21}$$

$$\frac{C_{gd}C_{gs}g_m R_{ds}R_{gd}R_i\tau}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_3^{21}$$

Z22

$$R_d + \frac{C_{gs}R_{ds}}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_0^{22}$$

$$L_d + b_1 R_d + \frac{C_{gd}R_{gd}C_{gs}R_{ds}}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_1^{22}$$

$$b_1 L_d + b_2 R_d = a_2^{22}$$

$$b_2 L_d = a_3^{22}$$

The equivalent circuit elements, both the series parasitics and the intrinsic elements, can be calculated from the following formulae:

$$\frac{C_{gs}R_{ds}}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_0^{22} - R_d$$

$$\frac{C_{gd}R_{ds}}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_0^{12} - R_s$$

$$\frac{C_{ds}R_{ds}}{C_{gd}+C_{gs}+C_{gd}g_m R_{ds}} = a_1^{11} - R_g - a_0^{11}(C_{gd}R_{gd}+C_{gs}R_i$$

$$C_{gd}R_{gd} = \frac{a_1^{22} - L_d - b_1 R_d}{a_0^{22} - R_d} = X_{gd}$$

$$C_{gs}R_i = \frac{a_1^{12} - L_s - b_1 R_s}{a_0^{12} - R_s} = X_i$$

$$b_1 L_g + b_2 R_g + \frac{C_{ds} R_{ds} C_{gd} R_{gd} C_{gs} R_i}{C_{gd} + C_{gs} + C_{gd} g_m R_{ds}} = a_3^{11}$$

$$b_2 R_g + \left(a_1^{11} - R_g - a_0^{11}\left(C_{gd} R_{gd} + C_{gs} R_i\right)\right) C_{gd} R_{gd} C_{gs} R_i = a_3^{11} - b_1 L_g$$

$$R_g = \frac{a_3^{11} - b_1 L_g - \left(a_1^{11} - a_0^{11}\left(C_{gd} R_{gd} + C_{gs} R_i\right)\right) C_{gd} R_{gd} C_{gs} R_i}{b_2 - C_{gd} R_{gd} C_{gs} R_i}$$

$$L_g = \frac{a_4^{11}}{b_2}$$

$$L_s = \frac{a_3^{12}}{b_2}$$

$$L_d = \frac{a_3^{22}}{b_2}$$

$$R_d = \frac{a_2^{22} - b_1 L_d}{b_2}$$

$$R_s = \frac{a_2^{12} - b_1 L_s}{b_2}$$

$$R_g = \frac{a_3^{11} - b_1 L_g - \left(a_1^{11} - a_0^{11}\left(X_{gd} + X_i\right)\right) X_{gd} X_i}{b_2 - X_{gd} X_i}$$

$$\frac{C_{gs} R_{ds}}{C_{gd} R_{ds}} = \frac{a_0^{22} - R_d}{a_0^{12} - R_s} = A \rightarrow C_{gs} = A C_{gd}$$

$$\frac{C_{gd} R_{ds}}{C_{gd} + C_{gs} + C_{gd} g_m R_{ds}} = \frac{C_{gd} R_{ds}}{C_{gd} + A C_{gd} + C_{gd} g_m R_{ds}} = a_0^{12} - R_s$$

$$R_{ds} = \left(a_0^{12} - R_s\right)\left(1 + A + g_m R_{ds}\right)$$

$$g_m R_{ds} = \frac{a_0^{21}}{a_0^{11}}$$

$$R_{ds} = \left(a_0^{12} - R_s\right)\left(1 + A + \frac{a_0^{21}}{a_0^{11}}\right)$$

$$g_m = \frac{a_0^{21}}{a_0^{11}} \frac{1}{R_{ds}}$$

$$C_{gs} = \frac{1}{R_{ds}} \frac{a_0^{22} - R_d}{a_0^{11}}$$

$$C_{gd} = \frac{1}{R_{ds}} \frac{a_0^{12} - R_s}{a_0^{11}}$$

$$C_{ds} = \frac{1}{R_{ds}} \frac{a_1^{11} - R_g - a_0^{11}\left(X_{gd} + X_i\right)}{a_0^{11}}$$

$$R_{gd} = \frac{X_{gd}}{C_{gd}} = \frac{a_1^{22} - L_d - b_1 R_d}{\left(a_0^{22} - R_d\right) C_{gd}}$$

$$R_i = \frac{X_i}{C_{gs}} = \frac{a_1^{12} - L_s - b_1 R_s}{\left(a_0^{12} - R_s\right) C_{gs}}$$

$$\tau = X_{gd} + X_i - \frac{a_1^{21}}{a_0^{21}}$$

AN ANALYTICAL DESIGN PROCEDURE FOR MICROWAVE OSCILLATORS BASED ON S-PARAMETERS

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ABSTRACT

This paper reports on a method for calculating a series type transistor oscillator circuit directly from the S-parameters. The feedback network and the resonator network are calculated for maximum instability in the input plane of the transistor and for maximum output reflection coefficient, respectively. The load network is calculated by imposing the oscillation condition in the resonator-transistor plane and determining the minimum load reflection coefficient. No optimization steps are necessary. Experimental results confirm validity of the procedure.

I. INTRODUCTION

Microwave sources are key components in a wide range of microwave applications ranging from sensors, radar to satellite communications. Despite advances in the large signal modeling of microwave active devices (e.g. FETs) microwave oscillators are still largely designed based on linear techniques. Linear design techniques are simple to use and can deliver satisfactory results, for example accurate prediction of the oscillation frequency. Design procedures for maximization and/or prediction of the output power based on small-signal parameters have been proposed [7]. However, accurate power prediction is only possible by employing non-linear techniques. Large signal analysis and design techniques are more time consuming, require expensive CAD and accurate non-linear models which may not always be easy to extract. In addition, many large signal design techniques are used only to determine the oscillator load network whereas the feedback and terminating (resonator) networks are determined (or used as start values for optimization) using the classical linear techniques. e.g. [1]. Other large signal design procedures based on large signal S- or Y-parameters seem to be unpopular due to requiring expensive large signal measurement setups or inaccuracies in large signal models [5].

The most commonly used linear technique is the negative resistance approach which is based on the optimization of the feedback network to minimize the stability factor of the transistor (or attain a stability factor less than one) and optimization of the terminating network to maximize the output reflection coefficient. The real and imaginary parts of the load impedance are chosen for delivery of maximum output power and for resonance respectively [3].

Clearly, the precise determination of the optimum oscillator networks, especially the feedback and the terminating networks, is necessary for all common design techniques. An analytical determination of the terminating network based on graphical illustrations has been proposed [9]. This paper presents exact formulae derived from S-parameters and based on the input and output reflection factors for determining the feedback, terminating and load networks. No optimization steps are necessary. The condition for resonance is imposed in the resonator-active device plane thereby

minimizing coupling and enhancing power delivery to the load network.

II. DESIGN PROCEDURE

A block diagram of a microwave transistor oscillator is shown in Fig. 1. The transistor can be described by its scattering parameters from which the oscillator network is derived. It is standard practice that only the actual output loading is dissipative, therefore only the load network is a complex impedance whereas the other two networks are considered to be only reactive.

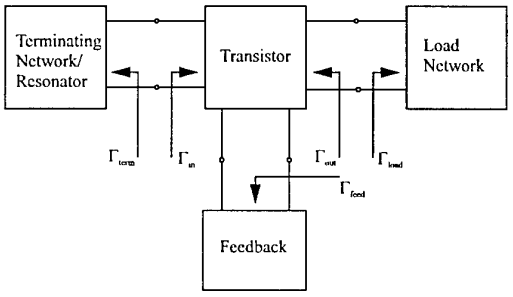

Fig. 1: Block diagram of a series feedback transistor oscillator circuit

a) Calculating the feedback and the terminating impedances

The feedback network is usually determined by optimization for a stability factor less than one or minimum stability factor of the active device. This network may also be determined by maximizing $|S_{11}|$ or $|S_{22}|$ as this increases instability (for values greater than one) in the input or output plane respectively [4]. Using $|S_{11}|$ as an example, the maximum value of $|Sij|$ may be determined analytically as follows

$$S_{11} = S_{11}^{'} + \frac{S_{13}^{'} S_{31}^{'} \Gamma_{feed}}{1 - S_{33}^{'} \Gamma_{feed}} \qquad (1)$$

whereby $\Gamma_{feed} = \frac{jX_{feed} - Z_0}{jX_{feed} + Z_0} = e^{j\arg(\Gamma_{feed})}$

and $S_{ij}^{'}$ are 3 port S parameters (which are directly derived from the measured 2 port parameters).

The maximum value of $|S_{11}|$ is maximized by putting

$$\frac{d|S_{11}|}{dX_{feed}} = 0 \qquad (2)$$

which results in a quadratic equation in X_{feed}. Hence, the feedback network can be easily calculated.

Having calculated the feedback network, new two-port S parameters are calculated from which the terminating network is now determined. The terminating or resonator network is determined so as to maximize the output reflection coefficient, $|\Gamma_{out}|$. This network is calculated in the same way as the feedback network. The output reflection coefficient is given by the following equation

$$\Gamma_{out} = S_{22} + \frac{S_{12} S_{21} \Gamma_{term}}{1 - S_{11} \Gamma_{term}} \qquad (3)$$

whereby $\Gamma_{term} = \frac{jX_{term} - Z_0}{jX_{term} + Z_0} = e^{j\arg(\Gamma_{term})}$

The terminating is calculated by again putting

$$\frac{d|\Gamma_{out}|}{dX_{term}} = 0 \qquad (4)$$

which similarly leads to a quadratic equation in X_{term}.

b) Calculating the load impedance

The reflection coefficient at the load can be expressed in terms of the scattering parameters and the input reflection coefficient as follows:

$$\Gamma_{load} = \frac{S_{11} - \Gamma_{in}}{\Delta - S_{22} \Gamma_{in}} \qquad (5)$$

whereby $\Delta = S_{11} S_{22} - S_{12} S_{21}$

and $\Gamma_{in} = |\Gamma_{in}| e^{j\arg(\Gamma_{in})}$

In order to minimize reflections from the load and thereby optimize delivery of generated power to the load, $|\Gamma_{load}|$ is kept to a minimum. The oscillation conditions can be fulfilled at the input port of the transistor (in the resonator-transistor plane) by imposing the following condition:

$$\arg(\Gamma_{in}) = -\arg(\Gamma_{term}) \qquad (6)$$

whereby $\arg(\Gamma_{term})$ is determined from eqn. (4).

The load network can then calculated by considering the following equation

$$\frac{d|\Gamma_{load}|}{d|\Gamma_{in}|} = 0 \qquad (7)$$

which also leads to a quadratic equation in $|\Gamma_{in}|$. Whereas eqns. (2), (4) and (7) may be solved by hand, the use of a symbolic mathematical software package such as MATHEMATICA [10] diminishes this effort.

III. LINEAR SIMULATION AND EXPERIMENTAL VERIFICATION

Starting with S-parameter data and the quadratic equations resulting from eqns. (2), (4) and (7) several microwave oscillator circuits have been designed. The designs were simulated using Microwave Design System (MDS) from HP. Fig.2 shows the layout of a 10.8 GHz microstrip oscillator. The feedback network is a shorted transmission line, the terminating network an open microstrip line and the output network is matched to a 50 ohm load using a series matching network.

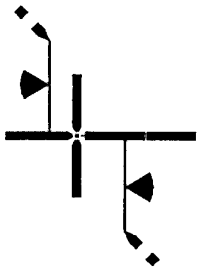

Fig.2 Layout of a 10.8 GHz series type microstrip oscillator.

Conventional startup conditions, i.e. for the negative resistance approach, the negative conductance approach and the reflection coefficient approach, are tested at all the three oscillator ports. In addition, the recently proposed Nyquist stability criterion for microwave oscillators [8], the Kurokawa stability test [6] and the stability tests developed for the reflection coefficient approach [2] verify the design. The tests are carried out for frequencies up to more than twice the design frequency. A 10.8 GHz oscillator delivering 11 dBm output power shows the validity of the design procedure.

IV. CONCLUSIONS

A simple and efficient analytical approach to the design of microwave oscillators has been proposed. The embedding circuit impedances of an oscillator are sequentially calculated from measured two-port small-signal parameters. Experimental results confirm validity of the proposed technique.

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Measurement and Physics Table-based Nonlinear CAD MSM Photodiode Model

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ABSTRACT

This paper presents a novel nonlinear model of a MSM photodiode. It is based on a network synthesis approach of the complex analytical frequency response function which characterizes the generation of electron-hole pairs and the drift of carriers in the depletion layer. The elements of the derived RLC equivalent network directly correlate to the physical parameters such as electron and hole transit times. The new nonlinear lumped-element model can be easily implemented in commercial CAD software like Microwave Design System (MDS) [1]. This model is used to simulate the nonlinear transient pulse analysis. The simulation shows excellent agreement with experimental results.

INTRODUCTION

The GaAs metal-semiconductor-metal (MSM) photodiode is known as an ultrafast device which is very attractive for high speed optoelectronic applications [2]. The reliability of the design severely depends on the performance of the available nonlinear model of the photodiode. Regarding the design of optical receivers, e.g. for the detection of ultrashort pulses in laser radar systems with high signal dynamics, an accurate nonlinear model of the photodiode is indispensable. In Fig. 1, the MSM photodiode is described as a 2-port which comprises an optical input and an electrical output port. $P^{i}_{opt}(t)$ and $P^{r}_{opt}(t)$ are the incident and the reflected modulated optical power signals at the optical port 1. The state functions at the electrical port 2 are $V_2(t)$ and $I_2(t)$. A nonlinear equivalent circuit model has been developed and used for CAD pulse transient simulation. It consists of a physics-based part which describes the optoelectronic conversion and is modeled as a simple RLC network and an electrical network with nonlinear current and charge sources similar to well known microwave FET modelling approaches [e.g. 3,4,5]. Using

$$H_n(\omega)=\frac{e^{-j\omega\tau_n}-1}{-j\omega\tau_n}-\frac{e^{-j\omega\tau_n}(j\omega\tau_n+1)-1}{(\omega\tau_n)^2}$$

$$H_p(\omega)=\frac{e^{-j\omega\tau_p}-1}{-j\omega\tau_p}-\frac{e^{-j\omega\tau_p}(j\omega\tau_p+1)-1}{(\omega\tau_p)^2}$$

the optoelectronic conversion transfer function can be written as [6]:

$$H(\omega)=H_n(\omega)+H_p(\omega) \qquad (1)$$

where $H_n(\omega)$ and $H_p(\omega)$ are the electron and hole transit times (τ_n and τ_p) dependent transfer functions, respectively. $H(\omega)$ is the total transfer function. In this paper we will show that, using a network synthesis approach, the transfer function can be modelled as a simple RLC network. The derived lumped-element RLC network (Fig. 2) can easily be implemented in common CAD systems.

MODEL DESCRIPTION

Eq. (1) can be reformulated as follows:

$$H(\omega)=\frac{e^{-j\omega\tau_n}-1}{(j\omega\tau_n)^2}+\frac{1}{j\omega\tau_n}+\frac{e^{-j\omega\tau_p}-1}{(j\omega\tau_p)^2}+\frac{1}{j\omega\tau_p} \qquad (2)$$

The exponential terms are expanded into Taylor series and truncated after the fourth power. This can be rewritten as follows

$$H(\omega)\approx 1-2\left(\frac{\tau_n+\tau_p}{12}\right)j\omega+3\left(\frac{\tau_n+\tau_p}{12}\right)^2(j\omega)^2+$$

$$+\frac{1}{48}(\tau_n-\tau_p)^2(j\omega)^2 \qquad (3)$$

The last term in eq. (3) is very small and can be neglected. Thus, eq. (3) is considered as a third power truncated Taylor series of the following expression:

$$H(\omega)\approx\frac{1}{\left[1+\frac{1}{12}(\tau_n+\tau_p)j\omega\right]^2} \qquad (4)$$

with $$H(\omega) = \frac{R \cdot I_i(\omega)}{V_1(\omega)}$$

As can be seen from Fig. 2, very good approximation is given for lower frequencies up to 25 GHz.
A lumped-element RLC circuit can now be derived from eq.(4) (Fig. 3), with :

$$L = \frac{2}{k} R(\tau_n + \tau_p) \quad \text{and} \quad C = \frac{1}{2kR}(\tau_n + \tau_p)$$

where R=1 Ω and k is a dimensionless fitting parameter. The final complete model of the MSM photodiode is given in Fig. 4. For CAD implementation the optical input power is normalized to $V_1 = P^i_{opt}/1A$.

MODEL IMPLEMENTATION

First, the small signal elements are extracted from the measured bias dependent electrical reflection coefficient [5]. The nonlinear current and charge sources are obtained by twodimensional integration over the known small signal quantities. They are presented in Figs. 5-7. Their bias dependent values are implemented in MDS7 as Citi-Files (two-dimensional look-up tables). The nonlinear elements are modeled in MDS as a six port symbolically defined device (SDD) and the residual linear elements as a lumped elements circuit. Fig. 8 shows the MDS circuit page of the implemented photodiode model. All parameters needed for the simulation are in the circuit page. The data for the bias dependent elements are spline-interpoled from data-set variables. The relation between the different parameters are implemented as equtions. This model is used for a transient pulse simulation. It can be used for DC or RF- simulation, too. Dispersion is not considered in this implemention.

EXPERIMENTAL RESULTS

For transient pulse simulation the following parameter values are used:

$$\tau_n = \frac{W}{v_n} \quad \text{and} \quad \tau_p = \frac{W}{v_p}$$

where W = 1.5 µm is the effective thickness of the depletion layer and v_n = 0.76 10^5 m/s, v_p = 0.11 10^5 m/s are the chosen electron-/hole drift velocities for GaAs photodetectors [7] (v_p is fitted). The bias independent model elements are $L_p \approx$ 640 pH and $C_p \approx$ 4 pF. The fitting parameter k = 9.8, and R_{load} = 50 Ω. The pulseshape of the used optical input pulse (Fig. 9) is detected with a streak camera and implemented in MDS as a piecewise linear transient pulse. The curves S1, S2 and S3 in Fig. 10 are the simulated pulse responses for different peak values of the optical input power: 0.63 mW, 0.69 mW and 0.75 mW, respectively (bias point: $P_{opt,DC}$= 0 mW, V_2=8 V). M1, M2, M3 (Fig.11) are measured pulse responses corresponding to the simulated pulses S1, S2 and S3, respectively. For a pulse measurement we have used a DHIL (double heterostructure injection laser diode) [8] as an ultrashort optical pulse source using a pumping modulation technique. The pumping current is supplied by the pulse generator 10.000A from Picosecond Puls Labs. As detector under test MSM photodiode (60 x 60 µm) is used [9]. The measured and simulated pulse responses are in good agreement. Only the trailing part of the pulse is somewhat different. This is due to the choice of the values for the electron and particularly the hole transit time. This difference can be eliminated by CAD parameter optimization or by extraction of the time parameters from the measurement [6]. Fig. 12 shows the simulated influence of the hole drift time on the pulseshape.

CONCLUSION

In this paper, a nonlinear table-based CAD-model for MSM photodiodes has been proposed. It has been shown that the optoelectronic conversion transfer function, which describes the generation and transport of carriers in the depletion layer can simply be modelled by a lumped RLC low pass circuit. Based on the CAD nonlinear model, transient pulse simulations have been performed. We have shown that the CAD model gives good agreement with the measurements.

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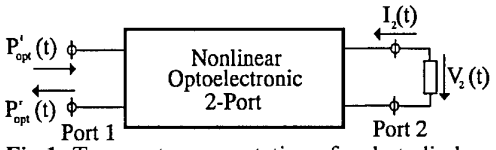

Fig.1: Two port representation of a photodiode

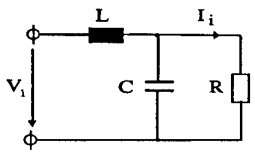

Fig. 3: Equivalent description of eq. (4) by RLC network ($V_1 = P^{i}_{opt}/1A$)

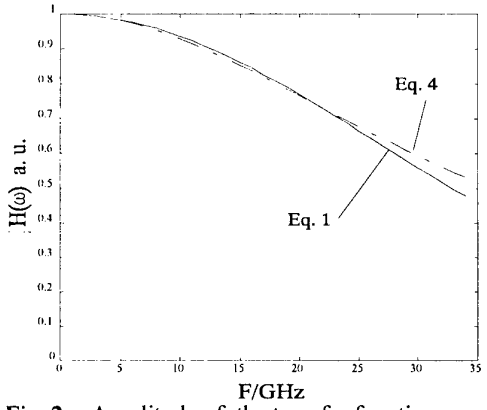

Fig. 2a: Amplitude of the transfer function of a MSM photodiode

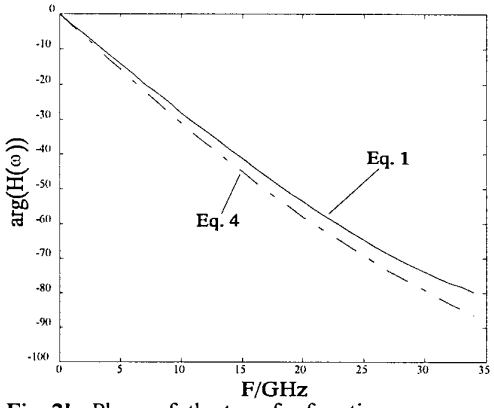

Fig. 2b: Phase of the transfer function of a MSM photodiode

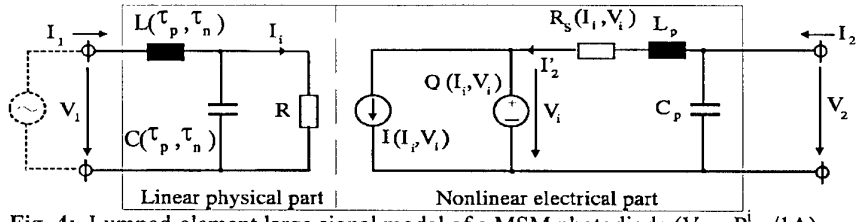

Fig. 4: Lumped-element large signal model of a MSM photodiode ($V_1 = P^{i}_{opt}/1A$)

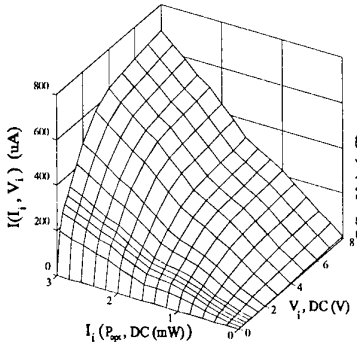

Fig. 5: Current source $I(I_i,V_i)$

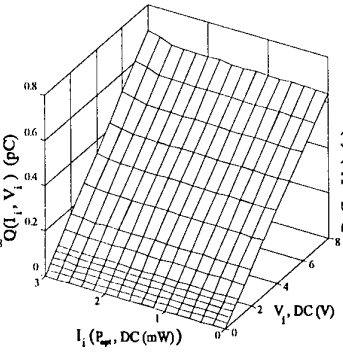

Fig. 6: Charge source $Q(I_i,V_i)$

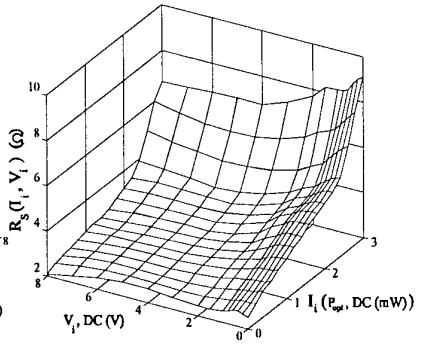

Fig. 7: Nonlinear series resistance $R_S(I_i,V_i)$

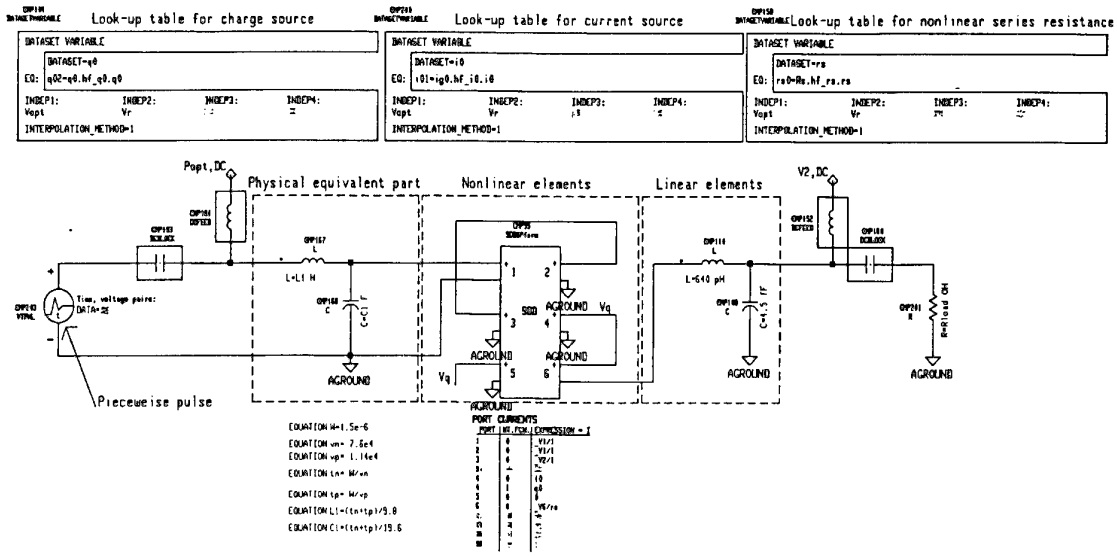

Fig. 8: MDS implemented nonlinear MSM photodiode model

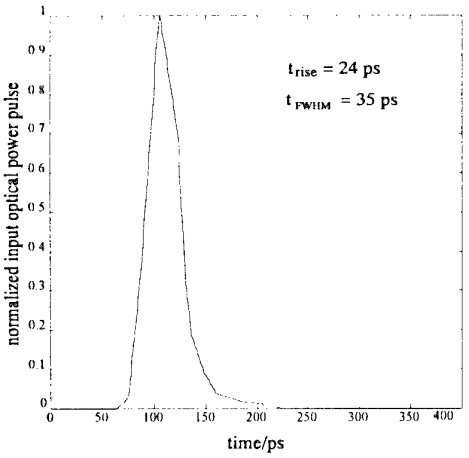

Fig. 9: Measured optical input pulse

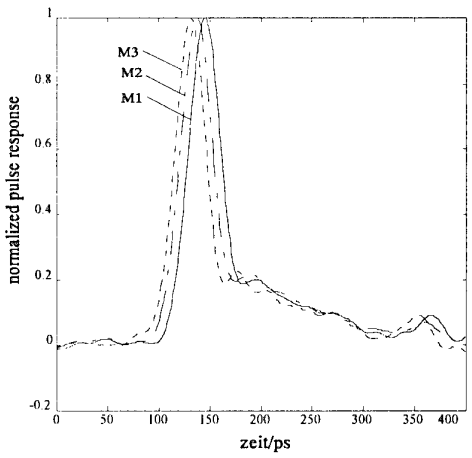

Fig. 11: Measured pulse response

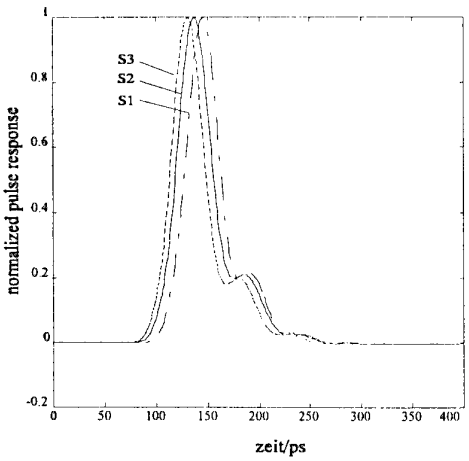

Fig. 10: Simulated pulse response

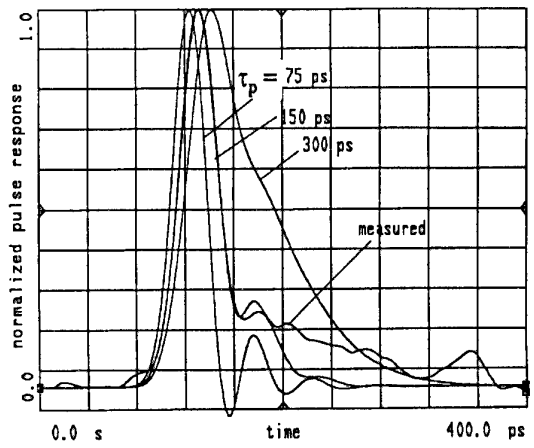

Fig. 12: Hole drift time influence of the pulse response

Numerical Transient Simulation of SH Laser Diodes under Strong and Highly Dynamic Carrier Injection

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ABSTRACT

Strong and highly dynamic carrier injection into a single heterostructure (SH) laser diode has been proven to be an easy method of generating powerful picosecond laser pulses. To understand this effect in detail, a thoroughly simulation of the device is done. Starting from Maxwell's equations and using established physical models for the current density, the carrier mobility, recombination, absorption and the refractive index, a set of coupled nonlinear inhomogenous partial differential equations is solved self-consistently using a finite difference scheme.

I. INTRODUCTION

The purpose of device simulation is: first to understand the device behavior in detail, and second to be able to optimize the performance or a special effect [1]. The pure experimentally optimization would be cumbersome and expensive, whereas the simulation uses virtual devices and is able to find an optimum solution. Every important variable can be calculated, especially inside the device, where it cannot be directly measured. This leads to the possibility of analyzing the influence of single parameters on the device characteristics.

There are two categories of device models: physical device models and equivalent circuit models [2]. Since the goal of this work is a detailed understanding of the physical effects inside the device, a physical device model is chosen. This model is one-dimensional, the spatial coordinate is parallel to the direction of current flow.

There are several publications about physical device simulation of semiconductor laser diodes, each one with its own advantages [3-5]. This simulator has been developed especially for SH laser diodes, which will be briefly described in section II. The physical effects that are to be explained theoretically with the simulator are shown in section III. The physical models and their mathematical descriptions that are used here are demonstrated in section IV. Eventually, first results are given in section V.

II. LASER DIODE STRUCTURE

The investigation is limited on multilayer structures with a Fabry-Perot cavity. An example of such a structure with typical geometric size is shown in Fig. 1. Due to the SH structure, index-guiding of the optical field is quite weak at the pn-junction. This property is important for the method of generating picosecond pulses, as will be described in section III. The active zone is quite large (150µm x 2µm), which leads to the possibility of emitting high optical power.

Commercial laser diodes (e.g. LD-60 and LD-62 from Laser Diode Labs, USA) have been manufactured using LPE, self-made laser diodes [11] were grown by MBE.

A description of the diode structure is used as input for the simulator. The following parameters are used:

- cavity length,
- mirror reflectance,
- thickness and doping for each layer
- material data such as band gap, relative permittivity, and electron affinity.

III. PULSE GENERATION

A new pumping current modulation scheme for semiconductor laser diodes with large active area has been developed [12]. Laser pulses with FWHM of 40 ps and 140 watts have been generated. These are used for sensor applications, e.g. in high ranging resolution laser radar systems [13]. The aim of this work is to establish a reasonable theoretical model for the pulse generation using the above mentioned pumping current modulation scheme.

Mainly AlGaAs-GaAs SH laser diodes have been investigated. In Fig. 2 the energy band diagram under forward bias (a) and the real part of the complex

refractive index (b) is shown. Under normal operating conditions, i.e. at moderate pumping currents, the concentration of the injected carriers in the center p-layer will not remarkably change the index profile of the asymmetric optical waveguide. In this case, at room temperature, an emission wavelength of about 904nm is expected for the investigated laser diodes.

However, as is indicated by the dashed line in Fig. 2b, very strong carrier injection attributes to a considerable negative contribution to the real part of the refractive index so that the commonly observed laser mode is weakened or even nearly suppressed. Regarding the dynamics, this operating condition can only be attained if the starting phase of the carrier injection is sufficiently fast, so that the index profile is considerably changed within the normal time delay of lasing being about 2.5ns. Typical rise time of the used pumping current is about 2ns and FWHM=3.4ns. Then, still keeping up carrier injection gives rise to a further increase of the gain in the laser active area, so that the threshold of the next higher order transversal mode is reached. After an additional delay time of roughly 1.5ns, which is needed for the gain to increase, the laser radiates a very powerful and short single pulse at shorter wavelengths. Theoretical investigations show, that the refractive index profile at λ=904nm has been changed so that index guiding is no longer possible. The optical field is only weakly guided by the gain in the active area. However, at λ=885nm, index guiding is still possible, and the gain is much higher than at greater wavelengths, so the optical intensity of the new mode is considerably higher.

Laser pulses with an optical peak power of 128W and pulse duration of 32ps have been obtained with a 2.032µm x 76.2µm emitting area, which exceeds the rated optical power by a factor of 55. A laser diode with an emitting area twice as large delivers 253W and a FWHM of 44ps. The pulses in Fig. 3 have been measured with a 60 GHz photodetector from New Focus, Inc.

IV. PHYSICAL DEVICE MODEL

A. The equations

For the time dependent case, Maxwell's equations in their complete form have to be used:

$$rot\ \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} \tag{1}$$

$$rot\ \vec{E} = -\frac{\partial \vec{B}}{\partial t} \tag{2}$$

$$div\ \vec{B} = 0 \tag{3}$$

$$div\ \vec{D} = \rho \tag{4}$$

Together with the material equations for isotropic and linear materials,

$$\vec{D} = \varepsilon \vec{E} \tag{5}$$

$$\vec{B} = \mu \vec{H} \tag{6}$$

it is sufficient to consider only eq. (1) and (2), since for the time dependent case eq. (3) and (4) are then automatically fulfilled. The electromagnetic fields can be calculated using both a vector potential A and a scalar potential φ [2]:

$$\Delta \vec{A} - \varepsilon_0 \varepsilon_r \mu_0 \frac{\partial^2 \vec{A}}{\partial t^2} = -\mu_0 \vec{J} \tag{7}$$

$$div\ \vec{A} = -\varepsilon_0 \varepsilon_r \mu_0 \frac{\partial \varphi}{\partial t} \tag{8}$$

$$\Delta \varphi - \varepsilon_0 \varepsilon_r \mu_0 \frac{\partial^2 \varphi}{\partial t^2} = -\frac{\rho}{\varepsilon_0 \varepsilon_r} \tag{9}$$

Compared with the steady-state case, it can be seen in eq. (9), that the scalar potential cannot follow the temporal change of the space charge ρ in an infinite small amount of time. This would be the case if the time derivative is neglected in (9). That would mean, that the steady-state case is reached immediately. The error of this assumption is small, if the space charge varies slowly with the time. Here we are interested in picosecond phenomena, so we must not neglect the time derivative in (9).

The electric field can be calculated as follows, whereas the magnetic field is not considered any further:

$$\vec{E} = -\frac{\partial \vec{A}}{\partial t} - grad\ \varphi \tag{10}$$

The space charge ρ contains ionized impurities and free carriers. The density of ionized impurities is assumed to equal the appropriate doping density, since the temperature is around 300K or even higher and the doping levels are quite high. Fermi-Dirac statistics are used to calculate the carrier concentrations as a function of the energetic difference between the corresponding quasifermi level and band edge:

$$n_{3D} = N_C \frac{2}{\sqrt{\pi}} F_{1/2}\left(\frac{W_{Fn} - W_C}{kT}\right) \tag{11}$$

$$N_C = \frac{2}{h^3}\sqrt{\left(2\pi\ m_n^* kT\right)^3} \tag{12}$$

$$p_{3D} = N_V \frac{2}{\sqrt{\pi}} F_{1/2}\left(\frac{W_V - W_{Fp}}{kT}\right) \tag{13}$$

$$N_V = \frac{2}{h^3}\sqrt{\left(2\pi\ m_p^* kT\right)^3} \tag{14}$$

The Fermi-Integral $F_{1/2}$ cannot be calculated in closed form. The approximation used here can be found in [6].

The index 3D means, that these carriers reside in bands with continuous energy levels with no restriction in motion. In a quantum well for example, the carriers cannot move out of the well without additional energy. They are referred to as 2D-carriers. Their concentration cannot be calculated using Fermi-Dirac statistics, because they are on discrete energy levels rather than on continuous ones. To calculate the 2D-carrier density, capture and escape rates into and out of a quantum well have to be formulated as a continuity equation. Another, but less thoroughly method is to solve Schrödingers equation and use:

$$n_{2D} = \frac{m_n^* kT}{\pi \hbar^2} \sum_v \left|\psi_v^{(n)}\right|^2 \ln\left(1+\exp\left(\frac{W_{Fn}-W_v}{kT}\right)\right) \quad (15)$$

$$p_{2D} = \frac{m_p^* kT}{\pi \hbar^2} \sum_v \left|\psi_v^{(p)}\right|^2 \ln\left(1+\exp\left(\frac{W_v-W_{Fp}}{kT}\right)\right) \quad (16)$$

The continuity equations for charge conservation can be directly derived from (1) and (4):

$$\frac{\partial n_{3D}}{\partial t} = \frac{1}{q} div\, \vec{J}_n - R \quad (17)$$

$$\frac{\partial p_{3D}}{\partial t} = -\frac{1}{q} div\, \vec{J}_p - R \quad (18)$$

In homostructures, the equations (7), (9), (17) and (18) are used to calculate A, φ, n_{3D} and p_{3D}. Eq. (11) and (13) are used to determine the quasifermi levels. In heterostructures, the continuity equations (17) and (18) have to be expanded to include 2D to 3D carrier exchange. Then, eq. (15) and (16) may be used for the calculation of the quasifermi levels. This task is quite cumbersome, therefore a linear approximation of the quasifermi levels inside a quantum well is made instead. The quantum well is in general quite narrow (around 10 to 50 nm), so the current is considered to be constant in this area. That means, that recombination inside the quantum well is neglected here. Using the model for the current density, where the current density is proportional to the gradient of the quasifermi level, a linear fit is a good choice. However, one has to ensure, that the current is continuous at the heterointerface. This means, that the calculation of the carrier density inside the quantum well depends on the approximation made previously.

Using (11) and (13) for the calculation of the gradient of the quasifermi levels, the current density model becomes:

$$\vec{J}_n = \mu_n\, n_{3D}\, grad(W_{Fn}) \quad (19)$$

$$\vec{J}_p = \mu_p\, p_{3D}\, grad(W_{Fp}) \quad (20)$$

$$\vec{J}_n = q\mu_n \left(\frac{F_{1/2(\eta_n)}}{F_{-1/2(\eta_n)}} U_T grad\, n + n\vec{E}\right) \quad ,\eta_n = \frac{W_C - W_{Fn}}{kT} \quad (21)$$

$$\vec{J}_p = -q\mu_p \left(\frac{F_{1/2(\eta_p)}}{F_{-1/2(\eta_p)}} U_T grad\, p - p\vec{E}\right) \quad ,\eta_p = \frac{W_{Fp} - W_V}{kT} \quad (22)$$

The carrier mobility model contains temperature dependence, ionized impurity dependence and electric field dependence as is proposed in [2] and [6].

The model for the recombination parameter R, that is used in (17) and (18), contains thermal recombination (Schockley-Read-Hall model, [5]), Auger recombination [2], impact ionization [2], spontaneous recombination [4] and stimulated recombination [4]:

$$R_{STIM}\big|_i = \int_{W_{min}}^{W_{max}} \sum_a \frac{c_0}{n_{eff,a}} g(\hbar\omega_a)\big|_i \frac{\left\|E_{opt}\right\|^2\Big|_i}{\int_x \left\|E_{opt}\right\|^2 dx} S_a dW \quad (23)$$

The stimulated recombination is to be calculated as a function of the spacial coordinate x. Since the photon density S_a for the a-th mode is a scalar value independent of x, the spacial distribution of the photon density has to be determined via the intensity of the optical field. This is obtained by solving the wave equation, which will be explained later. In contrast to the photon density, the stimulated recombination is not energy-dependent, therefore it must be integrated over the energy range of positive photon density defined by W_{min} and W_{max}, respectively.

g is the material gain or the negative absorption parameter, which can be calculated from:

$$g(\hbar\omega) = -\frac{\sqrt{2}\left|M_T\right|^2 q^2 m_r^{3/2}}{\pi^2 m_0^2 \hbar^2 \sqrt{\varepsilon_r c_0 \varepsilon_0 \omega \tau_{in}}} \int_0^\infty \frac{W^{1/2}}{\left(W + W_g - \hbar\omega\right)^2 + \left(\hbar/\tau_{in}\right)^2} \left[f_V\left(W_V - \frac{m_n^*}{m_n^*+m_p^*}W\right) - f_C\left(W_C + \frac{m_p^*}{m_n^*+m_p^*}W\right)\right] dW \quad (24)$$

The intraband relaxation time τ_{in} is assumed to be 0.1ps. The matrix element can be estimated as:

$$\left|M_T\right|^2 = \frac{m_0 W_g}{6}\left(\frac{m_0}{m_e} - 1\right)\left(\frac{W_g + \Delta}{W_g + \frac{2}{3}\Delta}\right) \quad (25)$$

where Δ is the split-off energy. The reduced effective mass is:

$$\frac{1}{m_r} = \frac{1}{m_n^*} + \frac{1}{m_p^*} \quad (26)$$

The Fermi distribution functions are:

$$f_V = \left[1+\exp\left(\frac{W-W_{Fp}}{kT}\right)\right]^{-1} \quad (27)$$

$$f_C = \left[1+\exp\left(\frac{W-W_{Fn}}{kT}\right)\right]^{-1} \quad (28)$$

The influence of the carrier density on the bandgap are taken into account like in [7]:

$$\Delta W_g = \frac{\kappa}{\varepsilon_{r,stat}}\left(1+\frac{\max(n,p)}{n_{crit}}\right)^{1/3} \quad (29)$$

$$\text{using } \kappa = \begin{cases} 0.11 & \text{for p-GaAs} \\ 0.125 & \text{for n-GaAs} \\ 0.14 & \text{for e/h Plasma} \end{cases}$$

$$n_{crit} = 7*10^{16} cm^{-3}$$

Equation (24) is only valid for homostructures or in other words outside quantum wells. Several models exist for the calculation of the material gain inside quantum wells. Analytical formulas are explained in [8]. The most important thing is that the influence of the carrier densities on the gain is included in the model.

The photon density is calculated from the rate-equation:

$$\frac{\partial S_a}{\partial t} = \frac{c_0}{n_a}\left(G_{m,a} - \alpha_{ab,a} - \alpha_{fc,a} - \alpha_m\right) \quad (30)$$

The modal gain for the a-th mode is:

$$G_{m,a} = \frac{\int g_a \left|\vec{E}_{opt,a}\right|^2 dx}{\int \left|\vec{E}_{opt,a}\right|^2 dx} \quad (31)$$

The loss mechanisms are absorption loss, which is already included in eq. (31), free carrier loss and mirror loss, respectively:

$$\alpha_{fc,a} = \frac{\int \alpha'_{fc} \left|\vec{E}_{opt,a}\right|^2 dx}{\int \left|\vec{E}_{opt,a}\right|^2 dx} \quad ,\alpha'_{fc} = 3\cdot 10^{-18} cm^2 n_{3D} + 7\cdot 10^{-18} cm^2 p_{3D} \tag{32}$$

$$\alpha_m = \frac{1}{2L_c} \ln \frac{1}{R_1 R_2} \tag{33}$$

R_1 and R_2 are the mirror front and rear facet reflectances, which are assumed to be constant and independent of frequency. L_c is the cavity length.

The modes of the optical field $E_{opt,a}$ are a solution of the optical wave equation. Since the frequency of the bias E-field is far smaller then that of the optical E-field, the resulting field can be written as the sum of both parts [9]. This permits the separated calculation of the optical field. The wave equation can be derived from Maxwell's equations:

$$\Delta \underline{\vec{E}} + k_0^2 \underline{n}^2 \underline{\vec{E}} = \vec{0} \quad , k_0 = \frac{\omega}{c_0} \tag{34}$$

Special attention is given to the modelling of the complex refractive index, since the influence of the injected carriers is to be investigated:

$$\underline{n} = n'_{(\omega)} - j n''_{(\omega)} = \frac{1}{k_0}\left(\beta_{(\omega)} - j\frac{\alpha_{(\omega)}}{2}\right) = \underline{\varepsilon}_r^{1/2} \tag{35}$$

The imaginary part of the refractive index can be directly related to the absorption parameter. The phase parameter β is unknown, so the real part of n cannot be directly determined. The refractive index is a complex value only in the frequency domain, whereas the physical refractive index must be real in the time domain. Non-complex functions in the time domain are symmetric in the frequency domain. For causal systems, there is a well defined relationship between the real- and imaginary part of the Fourier transformed function, known as Hilbert transformation. Using these two features, the Kramers-Kronig integral can be derived:

$$n'_{(\omega)} = \frac{2}{\pi} P\int_0^\infty \frac{\hbar\omega' n''_{(\omega')}}{(\hbar\omega')^2 - (\hbar\omega)^2} d(\hbar\omega') \tag{36}$$

The carrier induced change of the refractive index is written as:

$$\underline{n}_{(\omega,n,p,T)} = \underline{n}_{pure(\omega,T)} - \Delta\underline{n}_{(\omega,n,p,T)} \tag{37}$$

$$\Delta n''_{(\omega)} = \frac{\Delta\alpha_{(\omega)} c_0}{2\omega} \qquad \Delta n'_{(\omega)} = \frac{2}{\pi} P\int_0^\infty \frac{\hbar\omega' \Delta n''_{(\omega')}}{(\hbar\omega')^2 - (\hbar\omega)^2} d(\hbar\omega')$$

$$\alpha_{(\omega,n,p,T)} = \alpha_{pure(\omega,T)} - \Delta\alpha_{(\omega,n,p,T)} \tag{38}$$

Data about the absorption and refractive index for pure (undoped) material can be found e.g. in [9].

Refractive index changes due to carrier injection can be divided into three effects: bandfilling, bandgap shrinkage and free carrier absorption (plasma effect) [10]. The first two are already included in the computation of the absorption, the third is modelled as:

$$\Delta n'_{Plasma} = -\frac{q^2}{2\varepsilon_0 \sqrt{\varepsilon_{r,stat}}}\left(\frac{n_{3D}}{m_n^*} + \frac{p_{3D}}{m_p^*}\right) \tag{39}$$

and has to be added to the Kramers-Kronig integral. Fig. 4 and 5 show the calculated change in the refractive index for various carrier densities.

Using the zigzag-ray model for the optical field inside the waveguide [9], the optical modes and their cut-off frequencies can be determined by solving the eigenvalue problem (34). The refractive index is considered to be piecewise constant, so that a position dependent refractive index can be considered using boundary conditions for the electromagnetic field, which is separated into TE- and TM-modes.

B. Solving the equations

The equations (7), (9), (17), (18), (30) and (34) form a coupled system of nonlinear partial differential equations, containing all the above mentioned models for the current density, carrier mobility, carrier density, recombination, absorption, etc. An analytic solution can only be acquired for extremely simplifying assumptions. To avoid this, the system is solved numerically using a self-consistent algorithm. This requires a discretization of all the independent variables, which are the space coordinate and the time. In this work, the finite difference scheme is used, because the coordinate system is rectangular and the model is one-dimensional. The differential equations are transformed into difference equations using:

$$\left.\frac{\partial f^{(t)}}{\partial x}\right|_i = \frac{f_{i+1}^{(t)} - f_{i-1}^{(t)}}{x_{i+1} - x_{i-1}} \tag{40}$$

$$\left.\frac{\partial^2 f^{(t)}}{\partial x^2}\right|_i = \frac{2}{x_{i+1} - x_{i-1}}\left(\frac{f_{i+1}^{(t)} - f_i^{(t)}}{x_{i+1} - x_i} - \frac{f_i^{(t)} - f_{i-1}^{(t)}}{x_i - x_{i-1}}\right) \tag{41}$$

$$\left.\frac{\partial f_i}{\partial t}\right|_{t+\frac{\Delta t}{2}} = \frac{f_i^{(t+\Delta t)} - f_i^{(t)}}{\Delta t} \tag{42}$$

$$\left.\frac{\partial^2 f_i}{\partial t^2}\right|_t = \frac{2}{\Delta t^2}\left(f_i^{(t+\Delta t)} + f_i^{(t-\Delta t)} - 2f_i^{(t)}\right) \tag{43}$$

Note that the grid spacing is non-uniform, which gives the possibility to define a coarse grid in regions with only little changes in the dependent variables (e.g. potential φ) and a fine grid in the neigborhood of pn-junctions or heterointerfaces. In contrast to that the time steps are constant. The grid and the time step have to be carefully chosen in order to ensure convergence of the algorithm. Even the rate of convergence depends largely on this choice. Unfortunately there is no general rule for defining these quantities, they are a matter of experience.

Note that the first derivative with respect to time is not calculated at time point t but on a middle point between the current and the next time step. This requires the application of the Crank-Nicholson scheme in the equations (10), (17) and (18), where all quantities but the time derivatives have to be linearly interpolated to compute the value at the time step $t+\Delta t/2$. This is not done in (30), because the wave equation as an eigenvalue problem is solved decoupled of (9),.(17) and (18).

Boundary and initial conditions have to be known. The starting point of all calculations is the thermal equilibrium state of the device, which is calculated using a steady-state version of the program (no external voltage or current applied). Boundary conditions have to be formulated for the electric potential φ, the vector potential A and the carrier concentrations n and p. These quantities, except the potential φ are supposed to stay always at equilibrium, that means:

$$\varphi|_{x=0} = V_{ext} \quad , \quad A_x|_{x=0} = 0 \tag{44}$$

$$n_{3D}|_{x=0} = n_{3D,0}|_{x=0} \quad , \quad p_{3D}|_{x=0} = p_{3D,0}|_{x=0}$$

$$\varphi|_{x=x\max} = 0 \quad , \quad A_x|_{x=x\max} = 0 \tag{45}$$

$$n_{3D}|_{x=x\max} = n_{3D,0}|_{x=x\max} \quad , \quad p_{3D}|_{x=x\max} = p_{3D,0}|_{x=x\max}$$

The boundary condition of the potential φ means that the device is voltage controlled. If the device is to be current driven, the boundary condition has to be changed until the total current density at the boundary equals the injected current density before advancing to the next time step.

V. FIRST RESULTS

Since the computer program for the calculation algorithm is still under construction, only a few results will be given. Optimization of a laser structure using simulated results will be published in the future.

Fig. 6 shows the carrier concentration inside the device under forward bias. Since the optical field is only weakly confined at the pn-junction, most of the stimulated recombination takes place at the right hand side of the active zone. The influence of the carrier density on the refractive index profile for two different wavelengths can be seen in Fig. 7. Index-guiding at λ=904nm has been disabled, so this mode can only be guided due to the gain, that is quite low at this energy as can be seen in Fig. 8. For λ=885nm index-guiding is still possible and the material gain is quite high. Fig. 9 shows the modal gain for a steady-state carrier concentration shown in Fig. 6. If the modal gain for a specific mode exceeds the total loss, the photon density for this wavelength is increased, else decreased. Note, that the frequency dependence of the total loss (without absorption loss!) is neglegible. The calculated photon density can be seen in Fig. 10. If the photon density is plotted over time, than the light pulse can be seen. If it is plotted over the wavelength, the spectrum of the laser light is obtained.

If the rotation of the elektric field is assumed to be zero, then the current density is overestimated, especially if the external bias varies faster than 1 Volt per microsecond, as is shown in Fig. 11. For bias signals with a weaker time-dependence, the vector potential A can be neglected and poisson's equation (9) reduces to the steady-state fomulation without the second order time-derivative. However, if the bias changes rapidly with time, the complete formulation of Maxwell's equations must be considered, that means an additional equation for the vector potential A has to be solved.

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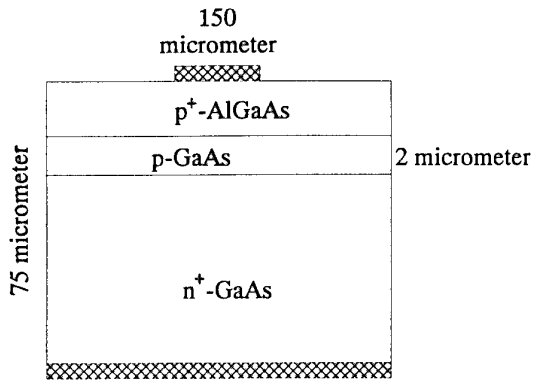

Fig. 1: Typical structure of a three layer laser diode.

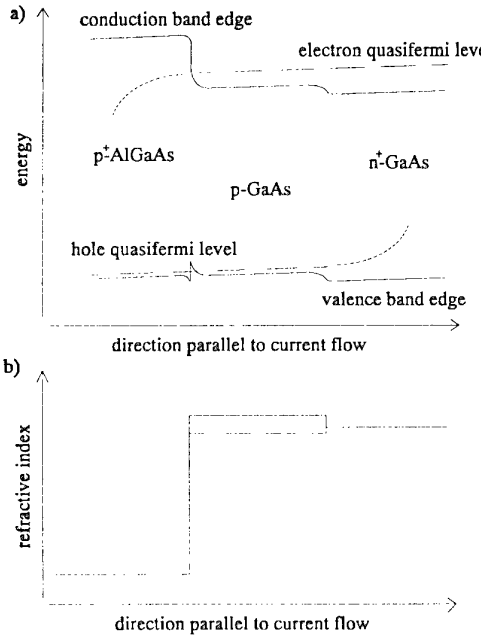

Fig. 2: Band diagram and refractive index profile of a three layer laser diode under forward bias.

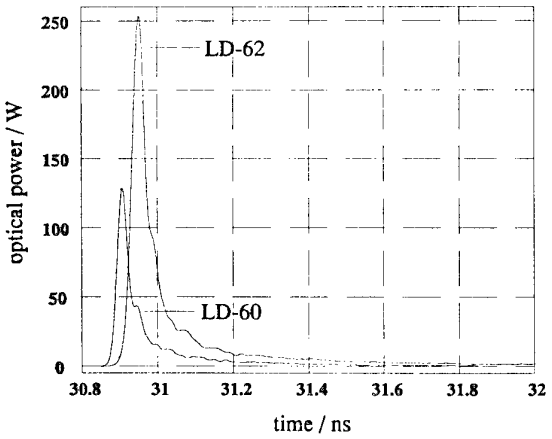

Fig. 3: Measured laser pulses of LD-60 (128 watts peak power) and LD-62 (253 watts peak power).

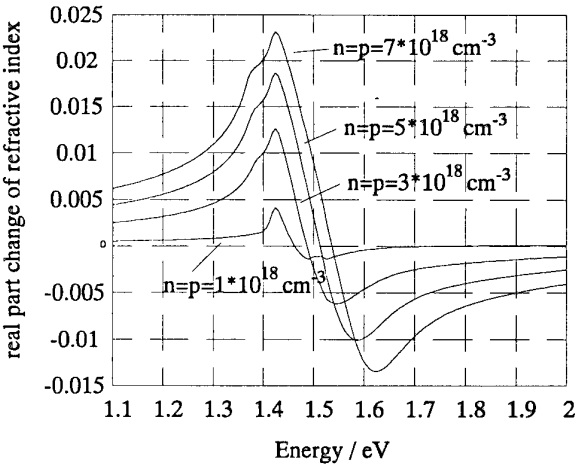

Fig. 4: Change in the real part of the complex refractive index for different carrier densities.

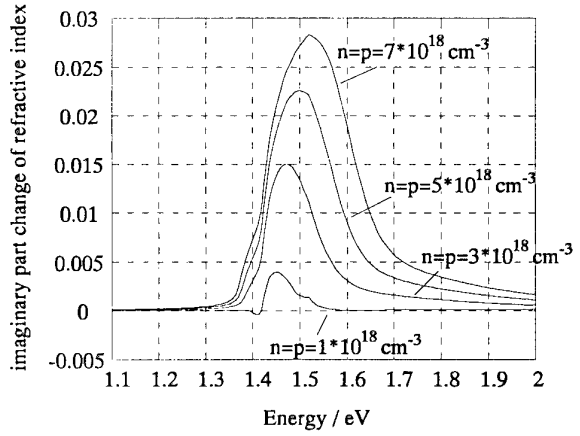

Fig. 5: Change in the imaginary part of the complex refractive index for different carrier densities.

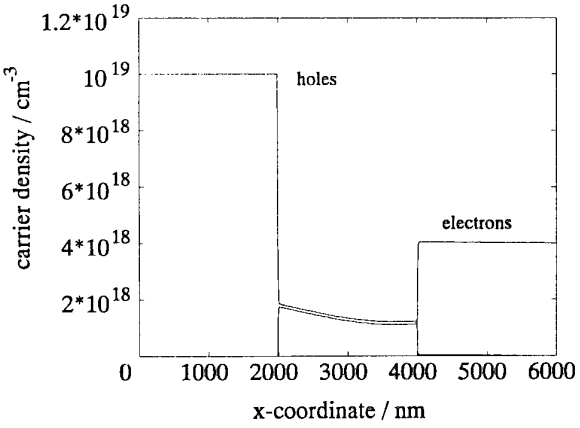

Fig. 6: Carrier concentrations under forward bias.

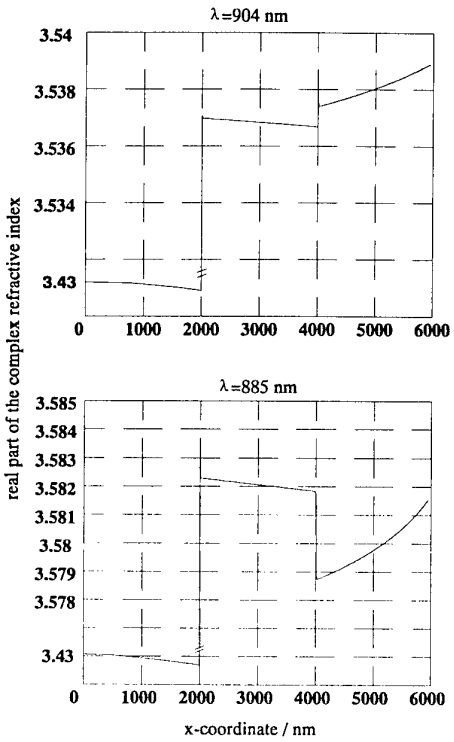

Fig. 7: Refractive index profile for two different modes.

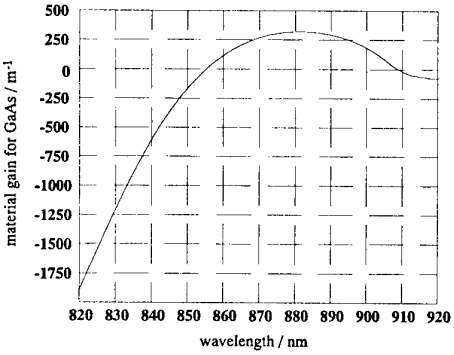

Fig. 8: Material gain profile for a carrier density of $n=p=3.2*10^{18}$ cm^{-3} in the active layer.

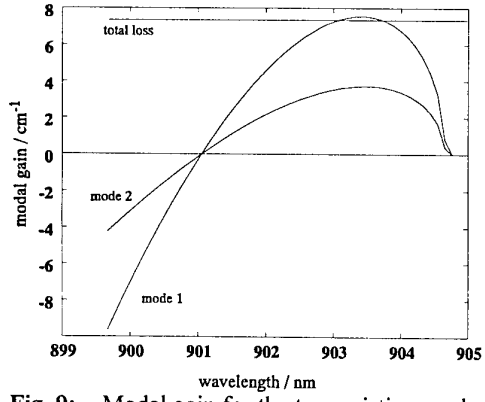

Fig. 9: Modal gain for the two existing modes and total loss.

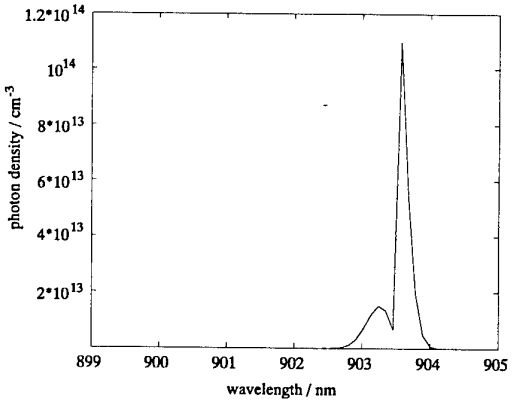

Fig. 10: Photon density calculated using Fig. 9.

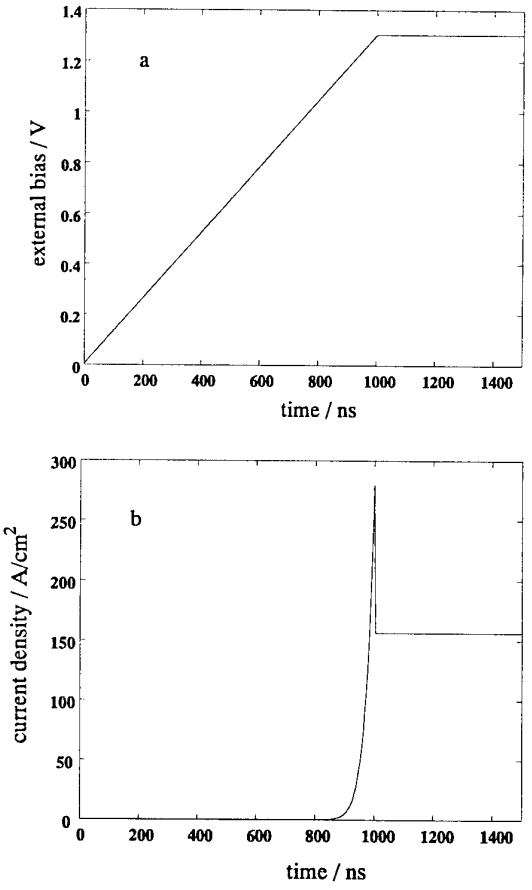

Fig. 11: a) time-dependent bias
b) related current density calculated assuming rot E = 0, which leads to an overestimation compared to the current density for constant bias.

Modelling, Simulation and Optimization of Ultrafast Semiconductor Lasers and Nonlinear Photodetectors for Laser Radar Sensors with Micrometer Accuracy

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ABSTRACT

A high resolution laser radar useful for object scanning, profile measurements, level control and many other applications has been set up. Using powerful picosecond pulses and highly sensitive avalanche photodiodes, surfaces with low reflectivity can be scanned as well. The distance measurement uncertainty is less than 300µm. The spot size is less than 1mm, which gives a lateral resolution of around 0.5mm. Eye-safety laser condition class 1 if fulfilled although a relatively high pulse repetition frequency (PRF=40kHz) is used. The scanned objects can be visualized in various ways, e.g. 3D-wireframe or 2D-contour.

I. INTRODUCTION

It is known that microwave radars generally exhibit a relatively large divergence of transmitted beam. This makes them less suited for precise imaging purposes. Operating at optical frequencies, the beam divergence angle can be made very small resulting in high angular resolution (e.g. [1]). In contrast to photographic imaging, where only a twodimensional projection of the object is obtained, a radar system is capable of achieving complete 3D information of the scene. With high resolution in both the lateral and normal direction, this system of vision is useful for many applications.

The kind of information that can be acquired, can be separated into two categories [2]: Distance information (position, orientation and shape can be extracted through postprocessing) and reflectance information. One method of measuring these information is the time-of-flight technique. The basic principle is easy and well known, since almost everyone has listened for the time-delay of lightning and the associated thunder in order to determine the distance of a thunderstorm. In our case we are not using acoustic waves but optical waves. A focused laser beam from the laser transmitter is directed towards the target via scanning mirrors. The signal is reflected back to the scanning mirrors and then collected and focussed by the receiver optics onto the photodetector. Using a reference signal which is directly coupled out from the transmitting beam, the time interval between the detected reference and reflected signal is proportional to the distance of the illuminated surface point on the target due to the constant velocity of propagation. For very large distances, the velocity might vary a bit due to atmospheric distortion so that error-correction must be performed, but here we will only consider short distances, e.g. up to 100 meters.

In order to ensure the practical usability of the radar system, the laser emission should be totally eye-save. This is achieved here using powerful but ultrashort (ps-range) laser pulses. Reliable detection of targets with low reflectance requires sufficiently high optical peak power of the transmitted laser pulses. Scanning of hot targets (e.g. 1200K) is difficult due to high background radiation which may significantly decrease the SNR [6].

A detailed description of the laser radar setup will be given in section II. Subsection A shows a block diagram of the system to explain the main components in general. Subsection B is about the laser transmitter and the method of pulse generation. Then, subsection C describes in detail the detector. Examples of scanned objects are given in Section III.

II. LASER RADAR SYSTEM

A. System Setup

Fig. 1 shows the block diagram of the realized pulsed laser radar for 3D-imaging. A 40 kHz quartz oscillator controls the pumping current generator which modulates the temperature-controlled semiconductor laser. The emitted laser beam is focussed onto the target by two biconvex lenses and deflected by a mirror and vibrating galvanometer scanner. As is known from Lagrange's theorem, to get the usually required measurement spot size of 1 mm it is necessary to use lasers with small emission stripes[3]. Therefore, in the discussed system different laser diodes with an emission stripe down to 76.2 µm (e. g. LD-60) are used.

The optical pulses are backscattered on the diffuse target surface. Part of the reflected optical power is received via the scanning mirror and the receiver optics by a fast

avalanche photodiode from Silicon Sensors, which has a response time of about 110 ps. For the determination of the target distance, which is related to the travelling time of the optical pulses, a reference signal is used. The detection of the trigger for the pumping current or the current pulse itself is unsuitable, because there are time uncertainties concerning the relationship between the current pulse and the emitted optical pulse. Therefore, an optical fiber is used which transmits a small amount of optical power from the transmitting laser diode to the optoelectronic receiver. Thus, two electrical pulses are obtained at the receiver output. The time interval between them correlates to the target distance.

The electrical pulses at the receiver output are transmitted via a bias network, which controls the DC operating point of the used photodiode, to the input of a sampling unit. This unit is triggered by the current pulse driving the laser diode. The sampling technique is used to circumvent expensive microwave time measurement units with extremely high time-resolution requirement of at least 6.7 ps corresponding to a 1 mm shift of range. A following analog-digital converter generates digitized pulse shapes which are transferred to a computer for final processing.

The position of any measured point on the object surface can be derived from the radial distance information, received from the A/D-converter, and the known angle position of the scanning mirror which is controlled by the computer. The measured data is visualized in various ways on a display.

B. Laser Transmitter

The laser transmitter consists of a single heterostructure (SH) semiconductor laser diode with a small driving circuit. Basically two mechanisms of generating ultrashort laser pulses exist: gain switching and Q-switching. No pulse compression techniques are considered here. For the Q-switching a saturable absorber is needed which can be produced using implantation of heavy ions [5]. In the case of gain switching a very short current pulse is needed to drive the laser diode. Due to dynamic effects and nonlinearities ultrashort laser pulses can be observed.

Fig. 2 shows a simplified circuit diagram of the used fast avalanche current pulse generator including the laser diode. The capacitor C_L is discharged through the diode if the transistor T is open. When T is closed, the capacitor is recharged due to the DC-Voltage U_B. The resistor R_M is for internal measurements only and can be left out for normal use.

Mainly AlGaAs-GaAs SH laser diodes have been investigated. In Fig. 3 the energy band diagram under forward bias (a) and the real part of the complex refractive index (b) is shown. Under normal operating conditions, i.e. at moderate pumping currents, the concentration of the injected carriers in the center p-layer will not remarkably change the index profile of the asymmetric optical waveguide. In this case, at room temperature, an emission wavelength of about 904nm is expected for the investigated laser diodes.

However, as is indicated by the dashed line in Fig. 3b, very strong carrier injection attributes to a considerable negative contribution to the real part of the refractive index so that the commonly observed laser mode is weakened or even nearly suppressed. Regarding the dynamics, this operating condition can only be attained if the starting phase of the carrier injection is sufficiently fast, so that the index profile is considerably changed within the normal time delay of lasing being about 2.5ns. Typical rise time of the used pumping current is about 2ns and FWHM=3.4ns. Then, still keeping up carrier injection gives rise to a further increase of the gain in the laser active area. Theoretical models using a quasi-static approach show, that due to these changes in the complex refractive index the threshold of the next higher order transversal mode is reached. After an additional delay time of roughly 1.5ns, which is needed for the gain to increase, the laser radiates a very powerful and short single pulse at shorter wavelengths. Theoretical investigations [6] show, that the refractive index profile at λ=904nm has been changed so that index guiding is no longer possible. The optical field is only weakly guided by the gain in the active area. However, at λ=885nm, index guiding is still possible, and the gain is much higher than at greater wavelengths, so the optical intensity of the new mode is considerably higher. A more detailed understanding using a full time-dependent approach is expected from further investigations.

Laser pulses with an optical peak power of 128W and pulse duration of 32ps have been obtained with a 2.032µm x 76.2µm emitting area, which exceeds the rated optical power by a factor of 55. A laser diode with an emitting area twice as large delivers 253W and a FWHM of 44ps. The pulses in Fig. 4 have been measured with a 60 GHz photodetector from New Focus, Inc. The electric signal was visualized using a 50 GHz sampling oscilloscope HP54120B. Since this oscilloscope requires a delay line in the used measurement setup, the optical pulses were damped and broadened. This means that they are in fact somewhat shorter than measured.

In order to reach even higher optical power, stack laser diodes have been investigated. The application of stack diodes has been demonstrated e.g. in [7]. However, in this case a problem occurs regarding very fast current pulse modulation, the delay time between pumping and lasing is different for the cascaded diodes. This leads to optical pulses with stepped leading pulse edges and isolated spikes (see Fig. 5), which make unique and precise time interval measurements impossible. In a particular case, the difference in delay time for the laser diodes is significantly large so that a burst of a few single pulses can evolve. The number of pulses is then equal to the number of diodes in the stack.

C. Detector Module

An important component of laser radar systems is the photoreceiver. A photoreceiver essentially consists of a photodetector, e.g. MSM-, PIN- or avalanche photodiode, followed by a low noise amplifier matched to it. The system performance is strongly influenced by the nonlinearities of the photoreceiver. Having accurate nonlinear models, error-correction of distorted received signals can be performed making time interval measurements more accurate.

One main problem in highly precise measurement originates in the nonlinearities of the used photodiodes. Using phase difference ranging, a phase uncertainty of about 55 degree has been observed under high dynamics of the receiving signal [8]. For PIN detectors more then 5 degree phase shifting versus input signal amplitude can be measured. In our application the high signal dynamic of the laser radar system leads to severe ranging errors caused by the nonlinearities of the used photodiode. Using an avalanche photodiode for signal detection utilizing pulse-travelling methods, Fig. 6 shows that the received optical pulse strongly depends on the input power. We can see that the time-significant point, defined in this case at 40% of the amplitude, varies with the input power value. An error- correction approach will be demonstrated on the basis of the GaAs metal-semiconductor-metal (MSM) photodiode. Considering this effect there is no principal difference between MSM-, PIN- or avalanche photodiodes [10]. The MSM photodiode is known as an ultrafast device and very attractive for high speed optoelectronic applications (e.g. [9]). However, the reliable design of optical receivers for highly precise laser radar must take into account the appearing high signal dynamics which originate in the strong variation of the reflectance of the measured surfaces, i.e accurate nonlinear models for the used photodiodes are indispensable. Fig. 7 describes the generalized presentation of a photodiode as a 2-port with an optical input and an electrical output port. A nonlinear equivalent circuit model for a MSM photodiode has been developed and used for CAD pulse transient simulation. It consists of a physics-based part which describes the optoelectronic conversion and is modeled as a simple RLC network and an electrical network with nonlinear current and charge sources. Fig. 8 shows the large signal model of the MSM photodiode which can easily be implemented in common CAD systems. Our model has been implemented in Microwave Design system (MDS7) [11] and used to simulate the nonlinear transient pulse analysis. Fig. 9 shows pulse responses for different optical input power. For the simulation a triangular optical pulse is used with t_{rise} = 10 ps and t_{fall} = 20 ps. We can see that the pulse shape strongly depends on the optical input power. Regarding the leading edge of the pulses (Fig. 10), the time shift due to the different optical input power, at the defined significant level (50% trigger level), is illustrated. The time shift versus the input optical power is presented in Fig. 11. Note that the simulation based on the nonlinear CAD model shows strong influence of the optical input power on the pulsshape of the received signal and the location of the time significant point for time-interval measurement.

III. RESULTS

Fig. 12 shows the attained measurement uncertainty of the system at a distance of 1.5 meters using an avalanche photodetector. An uncertainty of less than ±300 µm has been obtained using averaging over 16 measurements for each grid point.

Figs. 13 and 14 show the scanned image of a plug for a wall-socket as reflectance image and 3D-wireframe respectively. For the reflectance image the difference in intensity of the reflected and the reference pulse is coded into a colortable from black (maximum difference) to white (minimum difference) for each pixel. Because of the fact that the scanning mirrors can be moved very accurately in very small steps, the pixel size can even be somewhat smaller than the spot size of the laser beam. For the 3D-wireframe the difference calculated from the time separation of the reflected and reference pulse of each raster points is plotted on the xy-plane.

The distance data can also be coded into a colortable. The result is shown in Fig. 15a, which also contains the reflectance image of the same object (Beethoven's head, Fig. 15c, here as a negative image for easier comparison with b). After calculating the (in this example horizontal) derivative of Fig. 15a, a gradient image is obtained as can be seen in Fig. 15b. The effect of a virtual light source from the left can be observed. The derivative of the distance uncertainty is very much larger than the uncertainty itself, so in this case the gradient image creates the impression of a stone texture on the object. To reduce this effect, various methods of filtering can be done. For example, using a Medianfilter will not smooth sharp edges in the image, only the noise is reduced.

IV. CONCLUSION

A high PRF eye-save laser radar for precise 2D and 3D imaging has been set up. The attained measurement uncertainty is less than 300 µm, the lateral resolution is around 0.5mm. The pumping current modulation scheme based on a fast 'superinjection' of carriers into the active zone of a SH laser diode leads to powerful single laser pulses. New and accurate design models for the photoreceiver have been developed, which allow error-correction of the time-jitter due to nonlinearities in the response time of the photodiode at high optical input power.

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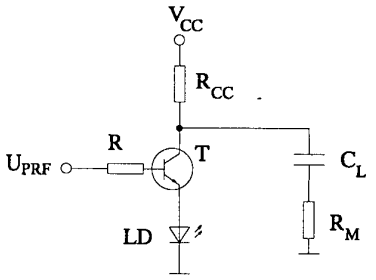

Fig. 2: Simplified circuit diagram of the used avalanche current pulse generator

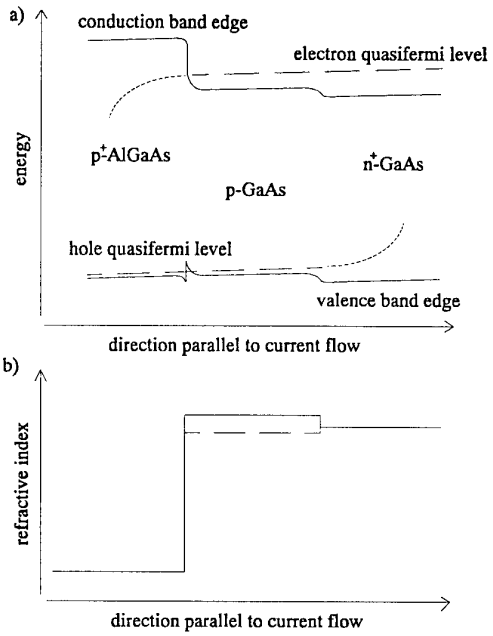

Fig. 3: Energy band diagram and real part of the complex refractive index (at λ=904 nm) under forward bias

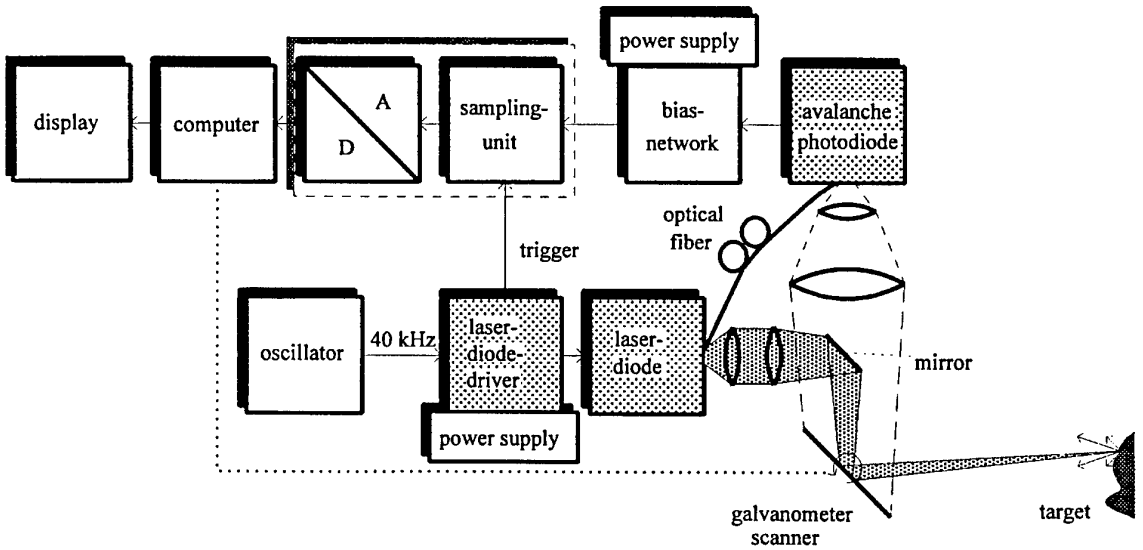

Fig. 1: Block diagram of the realized pulsed laser radar

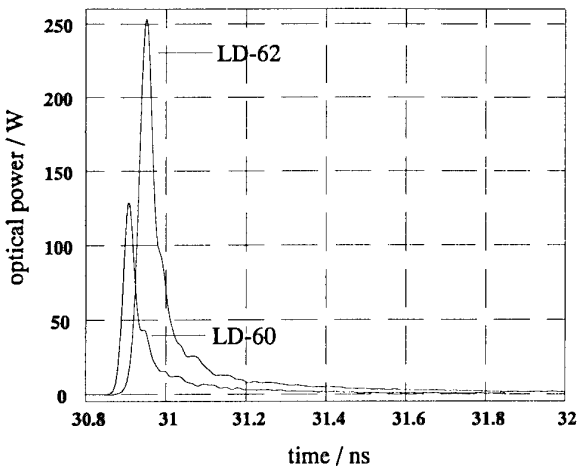

Fig. 4: Measured laser pulses of LD-60 (128 watts peak power, 32ps) and LD-62 (253 watts peak power, 44ps)

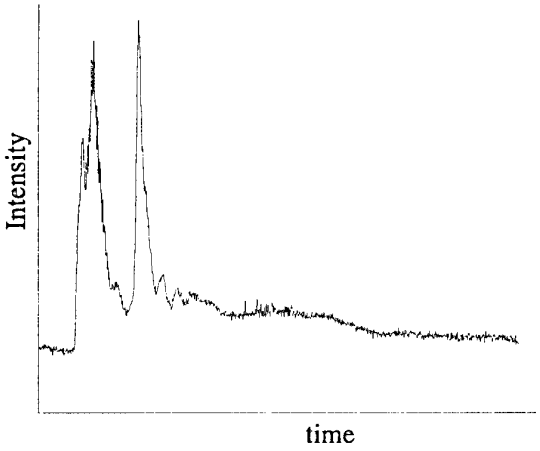

Fig. 5: Optical pulse of three stacked laser diodes, each of them having a different delay time

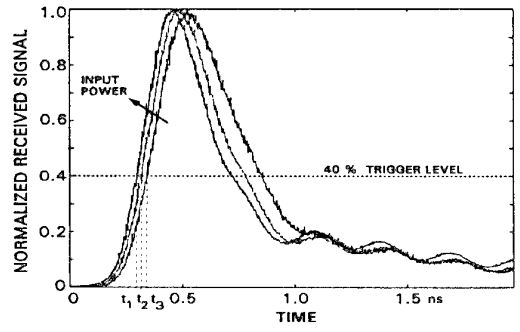

Fig. 6: Measured pulse response of a laser radar system for different optical input powers

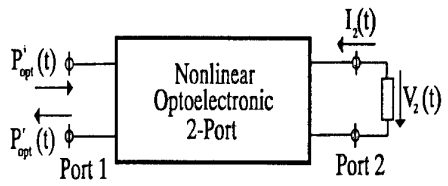

Fig. 7: Two port representation of the photodiode

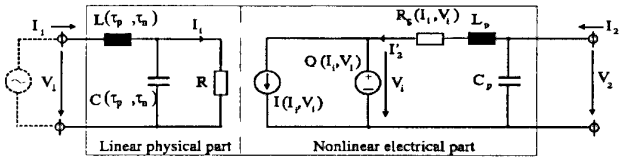

Fig. 8: Lumped-element large signal model of a MSM photodiode

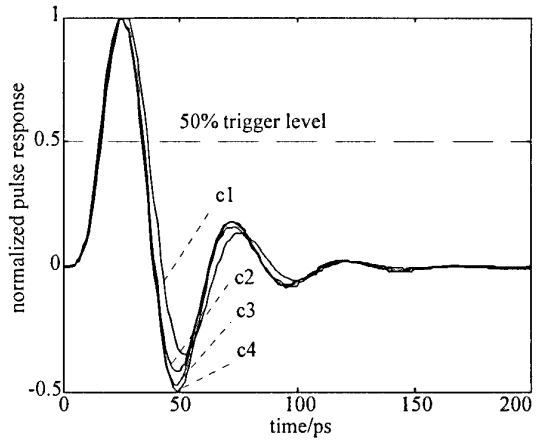

Fig. 9: Simulated pulse response for different optical input power

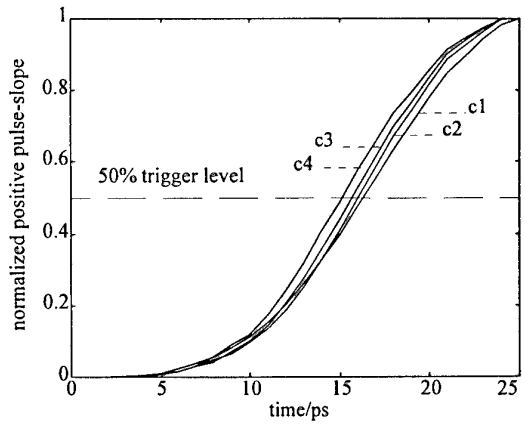

Fig. 10: Leading edge of the pulses showed in Fig. 9

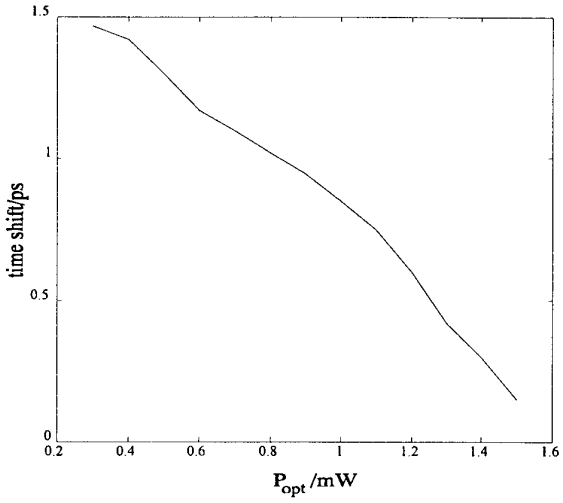

Fig. 11: Time shift versus optical input power

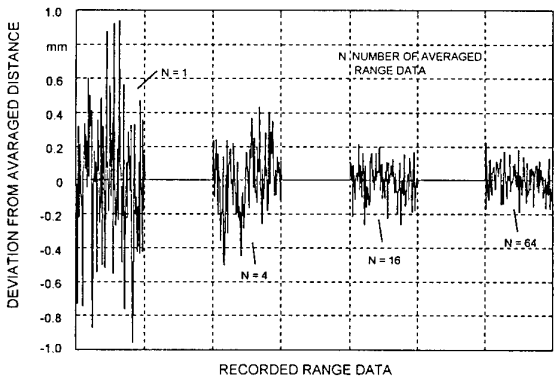

Fig. 12: Attained measurement uncertainty as a function of number of averaged range data. N=16 has been used for imaging

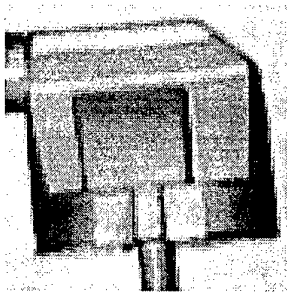

Fig. 13: Imaged plug for a wall-socket (contour). The size is 45 mm x 45 mm

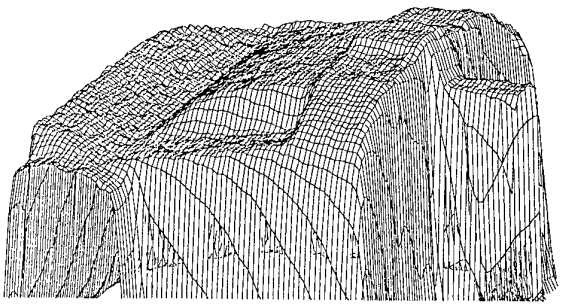

Fig. 14: Wireframe of the imaged plug viewed from the lower left corner of Fig. 13

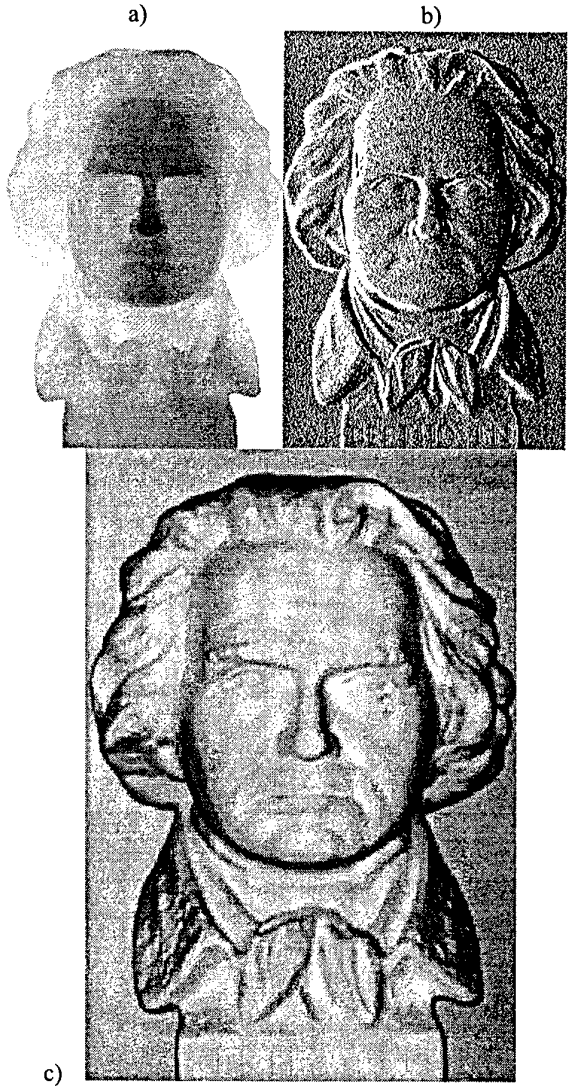

Fig. 15: Scanned image of Beethoven. The size is 130 x 190 mm
a) gray-scaled distance information
b) horizontal gradient of a)
c) reflectance image

Theoretical and Experimental Investigation of Coplanar MMIC Elements and Structures

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Abstract

Theoretical and experimental results for several coplanar waveguide (CPW) discontinuities and lumped elements are presented. The scattering parameters are calculated with powerful CAD-Tool HP/EEsof, Series IV, Version 6.1 including EM-Simulator Momentum and CPW element library Coplan, Version 2.1 (IMST). Theoretical simulations are compared with experimental results showing a very good agreement.

Introduction

The advantages of coplanar circuits compared to traditional microstrip circuits such as
- easy mounting of active and passive devices both in shunt and series connection,
- marginal dispersion effects and reduced losses,
- no need for via-holes

have led into a growing interest in coplanar circuit design. CPW is used more and more to realize MMIC components, but the lack of modeling tools which are required for a fast and low-price circuit development was an obstacle on this way for several years.

With powerful HP/EEsof Series IV [1] including CPW element library Coplan it is now possible to calculate nearly all kinds of discontinuities and lumped elements which are required for the design of microwave and millimeterwave components in MIC and MMIC technique.

The kernel of the CPW library Coplan is a 3D quasi-static finite difference calculation in the frequency domain. This method is applied to each of the elements in such a way, that a parametric description (equivalent circuit) of the elements results. Based on these results, a frequency dependent analysis is then started and S-parameters are calculated [2]. Due to the 3D approach, airbridges can be considered and the metalisation thickness can be taken into account during the calculations.

HP Momentum is based on a numerical electromagnetic technique called the method of moments. Circuits are assumed to be planar and in layout form but can include multi-layered substrate with vias [1].

Results

All presented CPW structures are designed and calculated at the Fachhochschule Gießen-Friedberg and fabricated at UMS (Ulm, Germany). Measurements were made at Daimler-Benz Aerospace (Ulm, Germany) with a commercial on-wafer probe using a vector network analyser from 45 MHz to 26 GHz.

The following substrate parameters are valid for all structures and simulations (Fig. 1): $\varepsilon_r = 13$, $h = 150\mu m$, $\tan\delta = 3 \cdot 10^{-4}$, $t = 3\mu m$, $\rho = 3.37 \cdot 10^{-6}\ \Omega cm$.

For verification of all CPW elements three main groups of structures were investigated:
1. discontinuities (e.g. short circuit, open circuit and step resonator)
2. Bends and junctions, including airbridges (e.g. bend, tee and cross resonators)
3. Lumped elements (e.g. inductors and capacitors).

Fig. 2 shows the calculated and measured magnitude and phase of S_{11} of a short and an open circuit. In both cases the theoretical and experimental results are closed within 0.3 dB in magnitude and 3° in phase in the full frequency range.

Fig. 3 depicts the theoretical and experimental results for S_{11} and S_{21} (magnitude and phase) of a step resonator. The measured and simulated results agree very good.

Experimental and theoretical results of two bends with different airbridges and a bend resonator are plotted in Fig. 4 and 5 for the frequency band up to 30 GHz. A very good agreement is observed for the results of both phase and magnitude of all three structures.

Fig. 6 shows the calculated and measured S-parameters (magnitude and phase) of a tee structure with a short circuited stub. The results of another tee structure with an open circuited stub are shown in Fig. 7. Again the theoretical and experimental results are very closed.

Fig. 8 depicts the calculated and measured S-parameters (magnitude and phase) of the cross structure with short circuited stubs. For this structure the agreement between simulation and measurement is outstanding.

Experimental and theoretical results of two spiral inductors are plotted in Fig. 9 and 10. A very good agreement is given for both phase and magnitude of S_{11} and S_{21} of these structures. Only in the case of 4.5 turns a slight difference between calculated and measured results is observed above 20 GHz.

Fig. 11 and 12 depict the calculated and measured S-parameters of two metal-insulator-metal (MIM) capacitors. Again a very good agreement is given for the results of both phase and magnitude behaviour of these elements.

Conclusions

A comprehensive comparison of measured and calculated results for different CPW discontinuities and lumped elements is given. The theoretical results were achieved with the HP/EEsof Series IV simulators (including Coplan and Momentum). It is shown that the theoretical and experimental results are in very close agreement.

Acknowledgements

All presented CPW structures were fabricated at UMS and measured at Daimler-Benz Aerospace. The authors would like to thank the responsible persons at these companies (particularly Dr. H.-P. Feldle) for their support. We also would like to thank HP/EEsof and IMST for making the Series IV simulator (including Coplan and Momentum) available for the simulation of the CPW structures.

References

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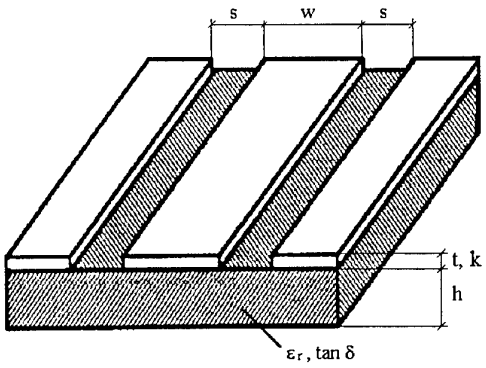


Fig.1: Substrate with parameters.

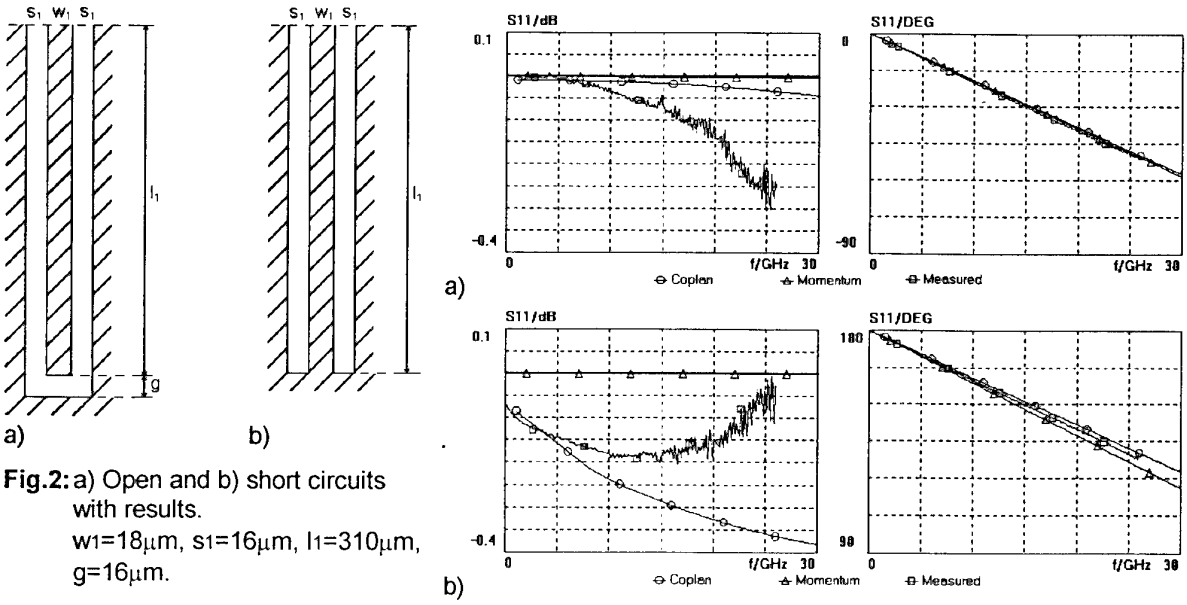
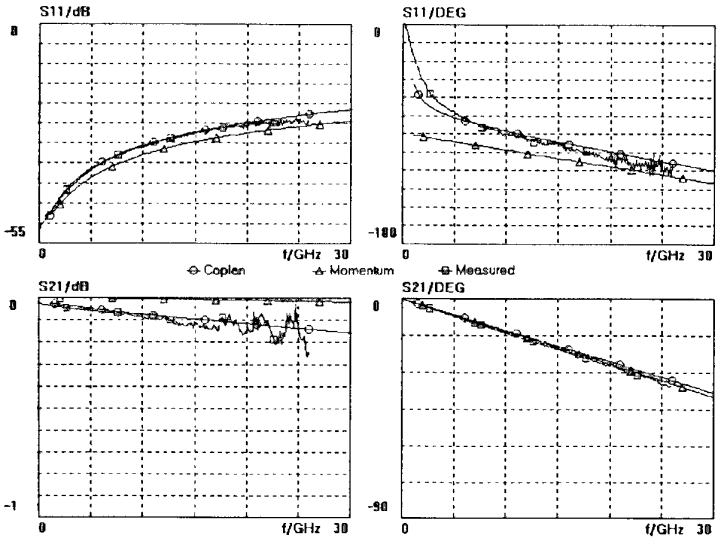


Fig.2: a) Open and b) short circuits with results.
w1=18μm, s1=16μm, l1=310μm, g=16μm.



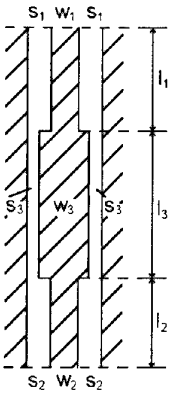


Fig.3: Step resonator with results.
w1=w2=18μm, s1=s2=16μm, w3=30μm, s3=10μm, l1=l2=96μm, l3=220μm.

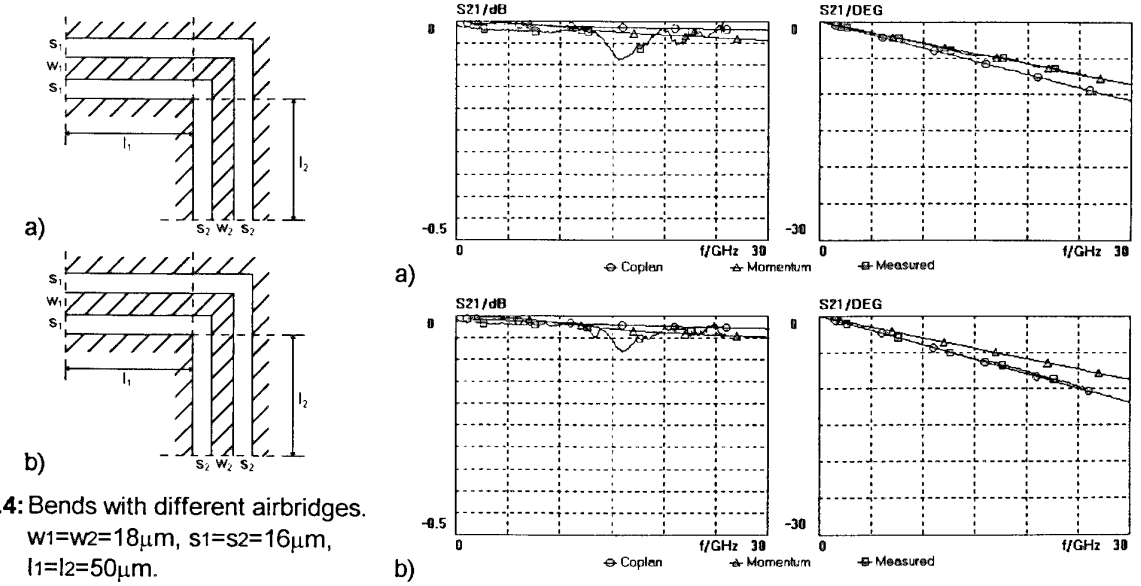
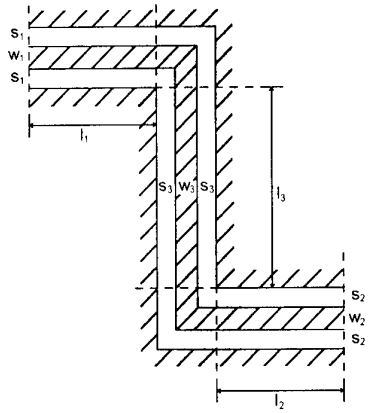


Fig.4: Bends with different airbridges.
w1=w2=18μm, s1=s2=16μm, l1=l2=50μm.



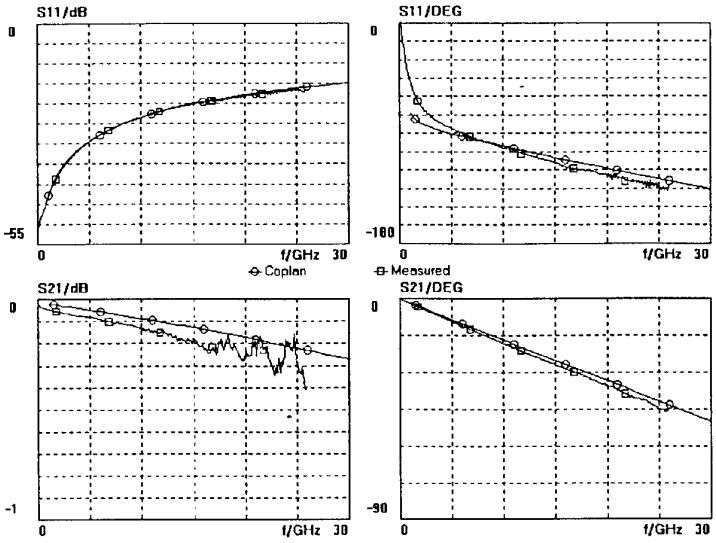
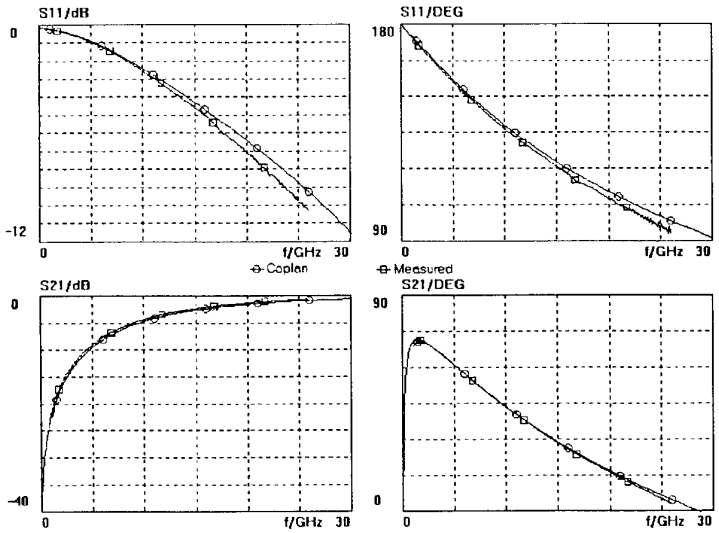


Fig.5: Bend resonator with results. $w_1=w_2=18\mu m$, $s_1=s_2=16\mu m$, $w_3=30\mu m$, $s_3=10\mu m$, $l_1=l_2=20\mu m$, $l_3=460\mu m$.



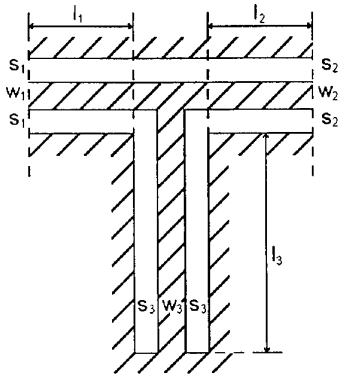
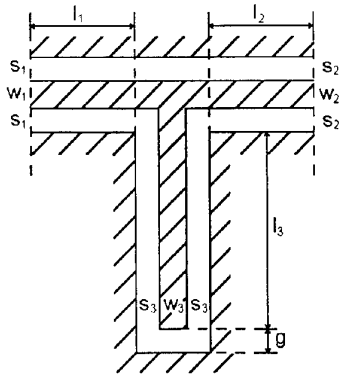


Fig.6: Tee structure with short circuited stub and results. $w_1=w_2=w_3=18\mu m$, $s_1=s_2=s_3=16\mu m$, $l_1=l_2=70\mu m$, $l_3=700\mu m$.



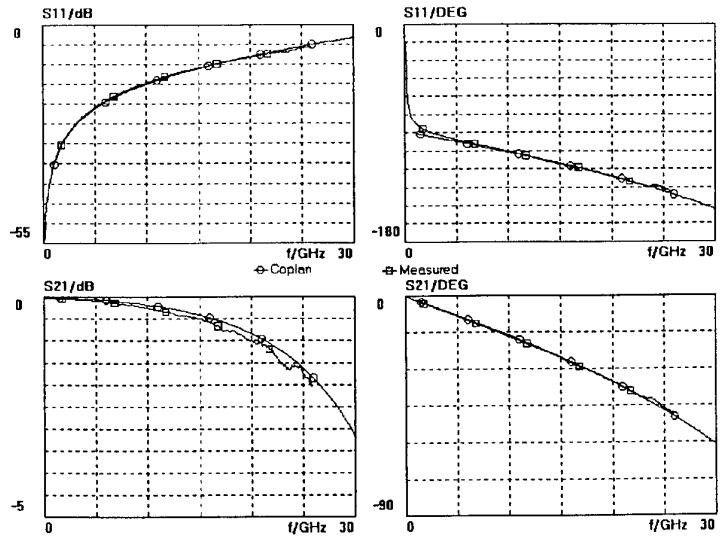
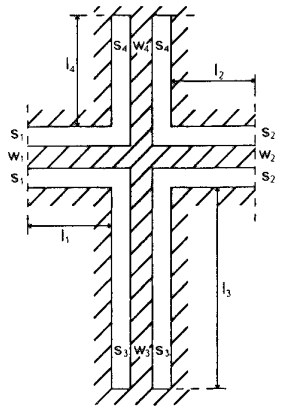


Fig.7: Tee structure with open circuited stub and results. $w_1=w_2=w_3=18\mu m$, $s_1=s_2=s_3=16\mu m$, $l_1=l_2=70\mu m$, $l_3=700\mu m$, $g=16\mu m$.



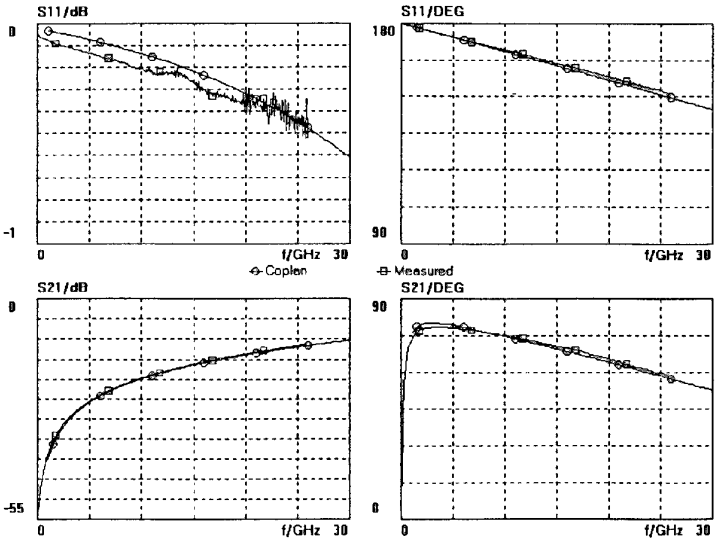
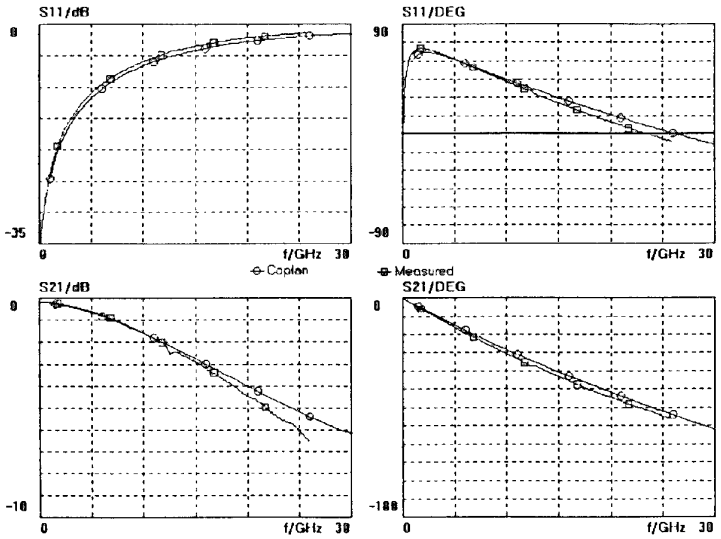


Fig.8: Cross structure with two short circuited stubs and results. $w_1=w_2=w_3=w_4=18\mu m$, $s_1=s_2=s_3=s_4=16\mu m$, $l_1=l_2=70\mu m$, $l_3=700\mu m$, $l_4=100\mu m$.



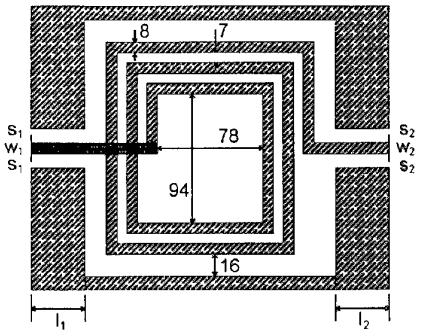


Fig.9: Spiral inductor with N=2.5 turns and results. $w_1=w_2=8\mu m$, $s_1=s_2=10\mu m$, $l_1=l_2=40\mu m$.

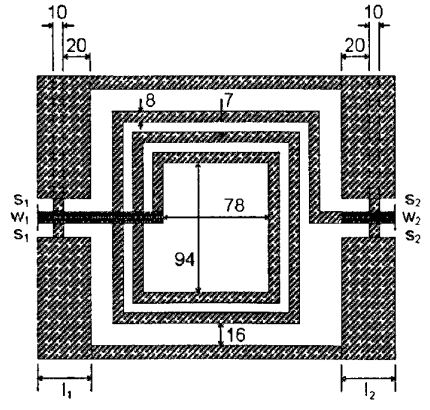
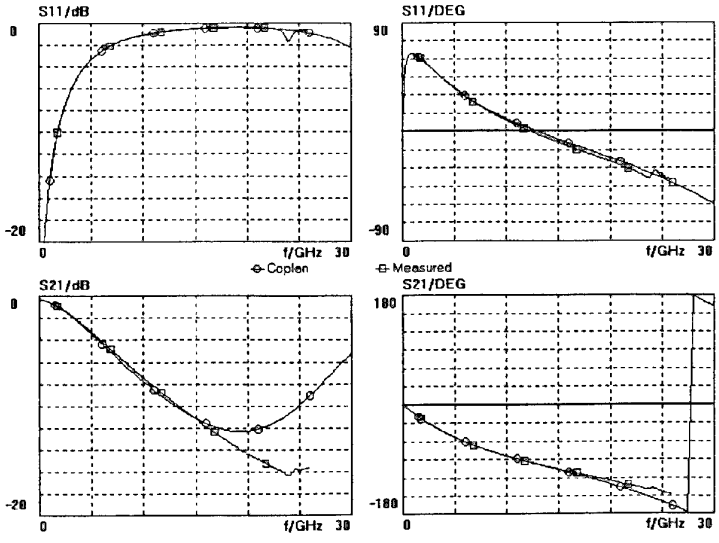
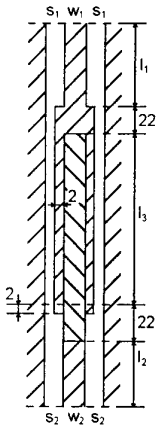


Fig.10: Spiral inductor with N=4.5 turns (incl. airbridges) and results. $w_1=w_2=8\mu m$, $s_1=s_2=10\mu m$, $l_1=l_2=40\mu m$.





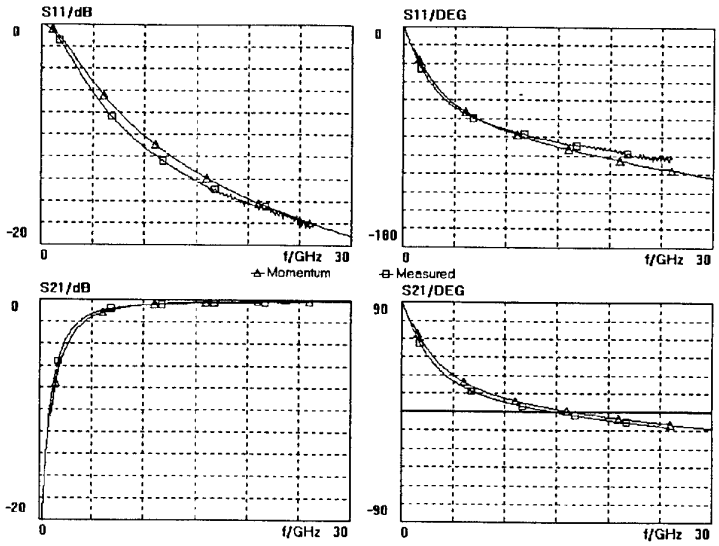
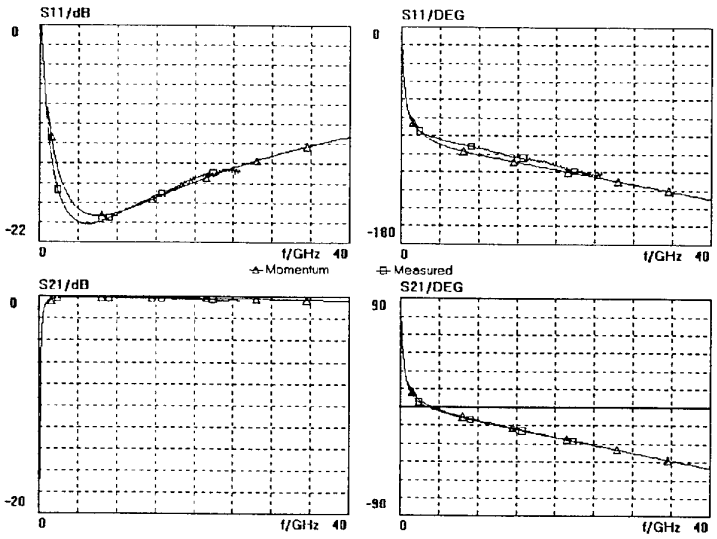


Fig.11: MIM capacitor with results. w1=w2=18μm, s1=s2=16μm, l1=l2=20μm, l3=100μm.



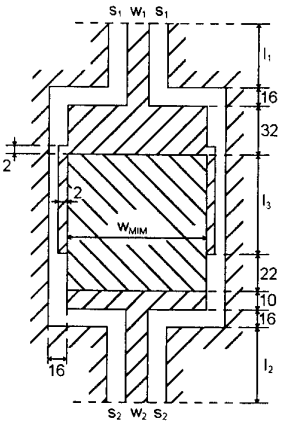


Fig.12: MIM capacitor with results. w1=w2=18μm, s1=s2=16μm, l1=l2=30μm, w_{MIM}=220μm, l3=70μm.

Scaling of FETs Using the Multi-Bias Extraction Procedure

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Abstract

The recently proposed multi-bias model parameter extraction procedure which uses only cold pinch-off and hot S parameter data has been applied to a 0.5 µm U-gate FET structure with variable gate width of 100-350 µm. The extracted results based on on-wafer S parameter measurements in a frequency range of 1-40 GHz clearly verify the expected scaling rules for the model parameters of a common 15-element FET model, the series resistors R_g, R_i, R_s, and R_d included.

I. Introduction

Optimizer based extraction procedures which use only measured S parameters generally yield no unique extraction solution because of the well known local minimum problem. Moreover, the solution for the model parameters is often not physically meaningful. Therefore, it is proposed to measure additional special test structures to determine the parasitics separately. Other approaches use FET measurements under special bias conditions, e.g. DC or cold FET in forward or pinch-off bias operation (e.g.[1,2,3]). This leads to simpler equivalent circuit topologies, and it is clear that the extraction uncertainty of the model parameter values is strongly reduced in these cases. However, as the experience has shown, the extracted values are generally not accurate enough to be used in a final mode of operation e.g. in the saturation region. Therefore, it would be very desirable to have an extraction algorithm available which allows a complete parameter extraction from hot S parameters in the given operating bias point.

The multi-bias extraction method, recently proposed [4,5], was developed for this purpose. Well-defined starting values for the model parameter extractor are derived from cold pinch-off S parameter data. Final extraction in the hot bias point includes the optimization of the parasitics for the best simultaneous fit to both the measured hot and cold pinch-off scattering coefficients. Preliminary investigations indicated that the procedure delivers a unique solution for all extracted model parameter values. In particular, it was found that the bulk resistance value of R_d was always larger than R_s in the FET saturation region, which emphasizes the physical meaning of the extracted results.

II. Measured FET Structure with Variable Gate Width and Extracted Results

In this paper, the multi-bias extraction procedure is applied to a U-gate MESFET with various gate widths. The gate length was 0.5 µm and the gate width varied in the range of 100 µm (2x50 µm) and 350 µm (2x175 µm). The width variation step was 50 µm. The devices were fabricated using the Plessey F20 foundry process.

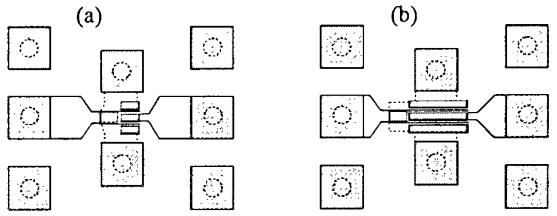

Fig. 1. Investigated simplified U-gate FET structures with various gate widths. Configuration (a) shows a minimum gate width of 100 µm (2x50 µm) and (b) a maximum gate width of 350 µm (2x175 µm).

Fig. 1 illustrates two simplified configurations of the investigated FET structure. Fig. 1a shows the device with the shortest gate width and Fig. 1b that with the longest gate width. The dimensions of the contact pads for probing were invariant.

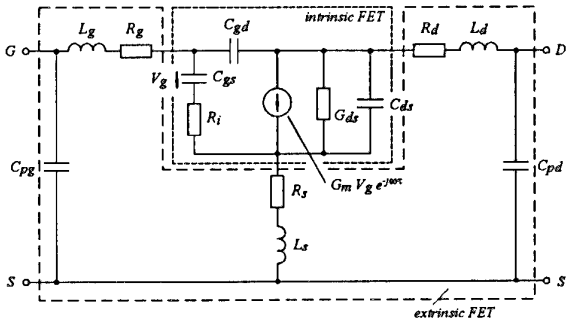

Fig. 2. Used common 15-element FET model topology for model parameter extraction.

Fig. 2 shows the used common 15-element FET model topology for model parameter extraction. The multi-bias extraction procedure based on two bias-points. V_{GS}=-0.3V and V_{DS}=3.0V was chosen for the saturation region, and V_{GS}=-1.5V and V_{DS}=0V for the pinch-off region, respectively. The S parameters were measured with a HP VNA 8510B in the frequency range of 1-40 GHz using a Cascade wafer prober (model 42).

Fig. 3 shows the extracted values of all internal model elements. Notice the low scattering of the separately extracted model element values versus gate width and the strong linear dependence except the carrier delay time τ. τ is constant for all gate widths due to the same bias condition and same propagation path of the carriers. The extrapolation of the extracted functions of G_m, G_{ds}, and C_{ds} cross the diagram origin, i.e. they are directly proportional to the gate width [5]. The extrapolation for zero gate width yields non-zero values for C_{gs} and C_{gd}, which originates in the special parasitic FET pattern configuration. R_i is generally known as a parameter, whose value is very difficult to be extracted; also in this case the multi-bias extractor delivers a unique linear dependence on the gate width.

In Fig. 4 the FET parasitics R_g, R_s, R_d, L_g, L_s, L_d, C_{pg}, and C_{pd} are plotted versus gate width. The functions of R_g, L_g, R_d, and R_s are as expected; the values are proportional to the gate width. Notice that the series resistances show again very low-scattered values. The extracted values for C_{pg} and C_{pd} reflect the variation in the pattern for different gate widths. C_{pd} decreases with increasing gate width, which originates in the continuous reduction of the wide pad length of the FET drain contact (Fig. 1). The plot for C_{pg} is more complex. The gate contact pad is shortened with increasing gate width which results in a reduction of the parasitic capacitance. Conversely, the increase of the gate width increases the gate-source stray capacitance. The diagram shows a slow effective growth of Cpg with the gate width. As can be intuitively derived from the metallization pattern of the source electrodes in Fig. 1, L_s decreases with growing gate width. An unexpected result has been obtained for the drain inductance L_d. With increasing gate width the inductance value is inversely proportional to the gate width. Therefore it is concluded that the growth of inductance originating in the increased geometric gate length is of minor influence. The distributed drain current normal to the gate fingers essentially contribute to the inductance value.

III. Conclusion

It has been shown that, investigating a 0.5 µm U-gate MESFET with variable gate width, the proposed multi-bias extractor using only S parameters in the saturation and pinch-off region delivers a unique solution for all model parameter element values of a common 15-element FET model. This is well demonstrated by the smooth traces of extracted model parameter values in dependence of the gate width The linear function of the internal element values (except τ), and external series resistances R_g, R_s, R_d and gate inductance L_g respectively, verifies the scaling feature of the investigated FET device with respect to the variation of the gate width. The parameter values for the extrapolated zero gate width gives further information about the FET parasitics.

Acknowledgement

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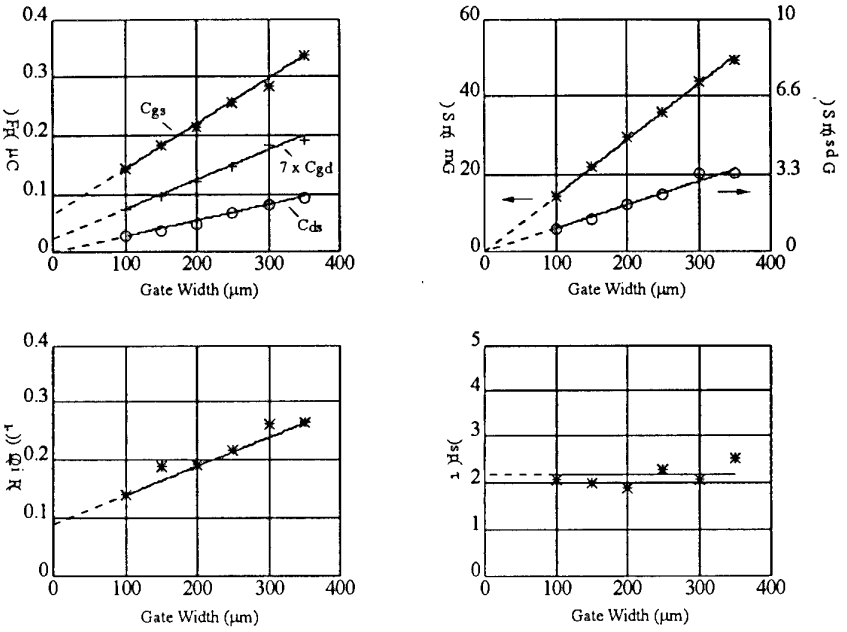

Fig. 3. Extracted internal model element values versus gate width ($\mu \in \{gs, gd, ds\}$).

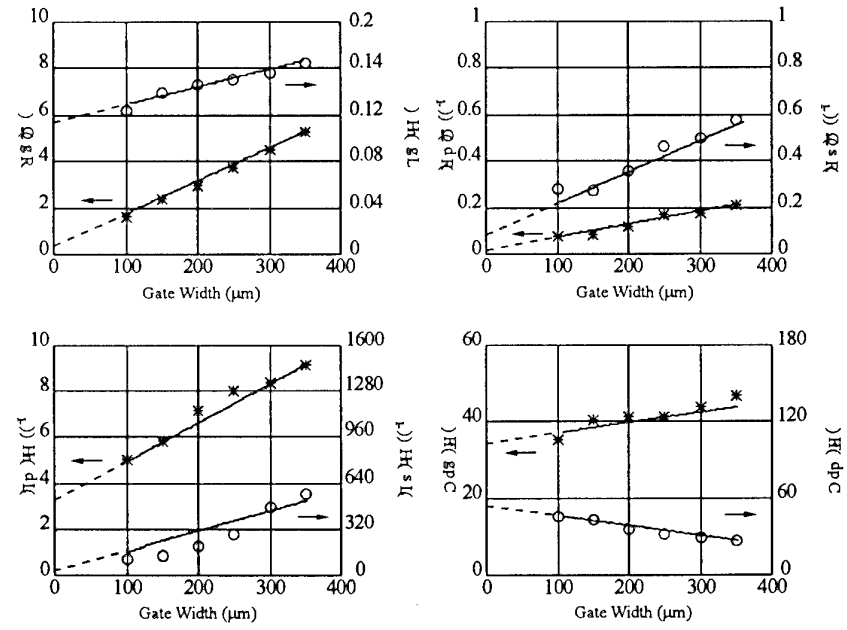

Fig. 4. Extracted external model element values versus gate width.