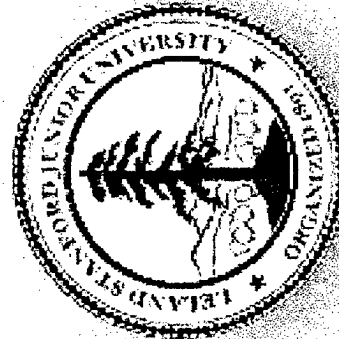


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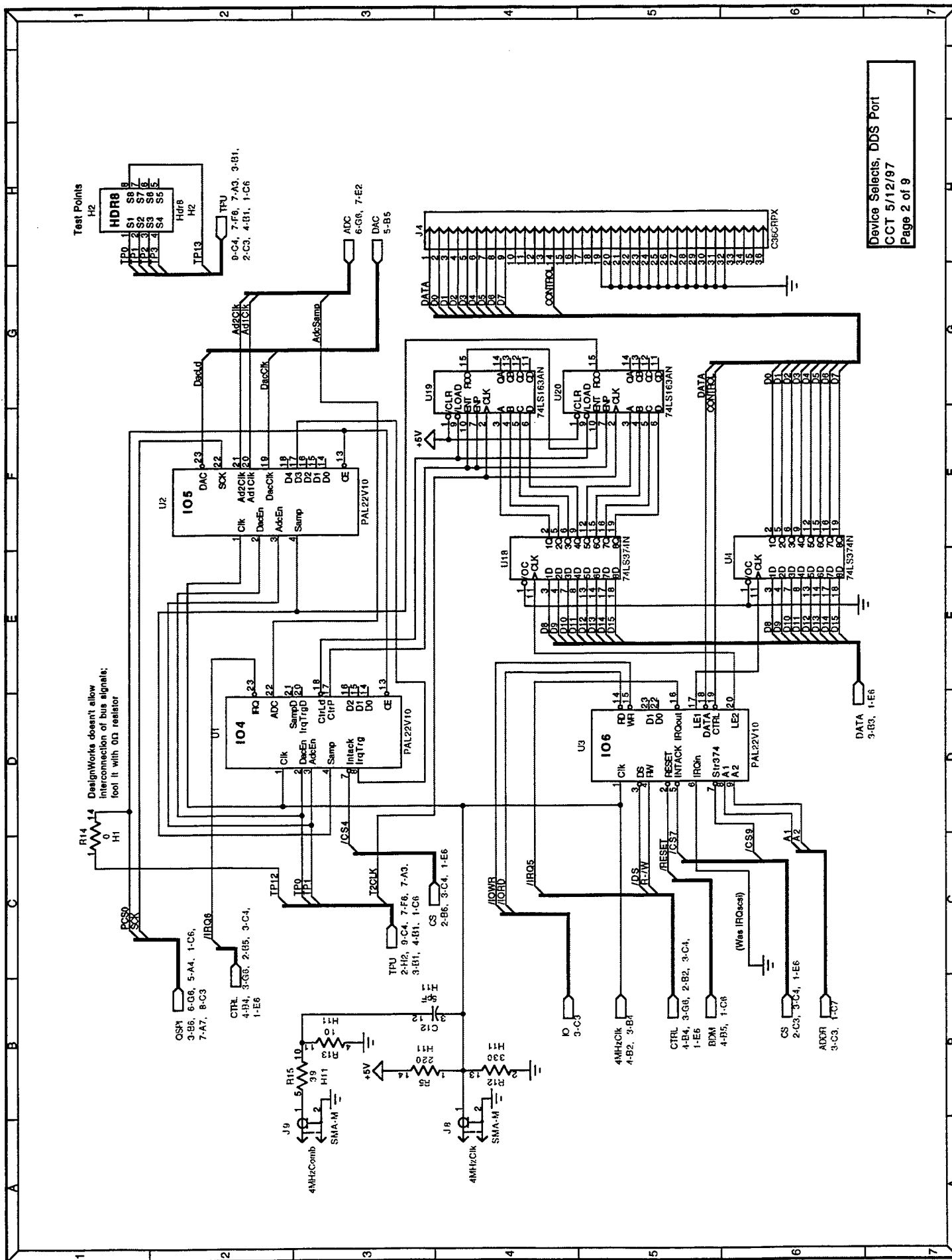


HF RADAR FINAL REPORT
University of Michigan Projects 032882 & 032887

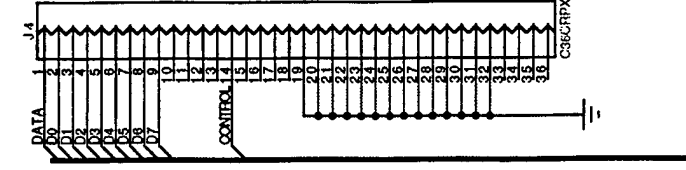
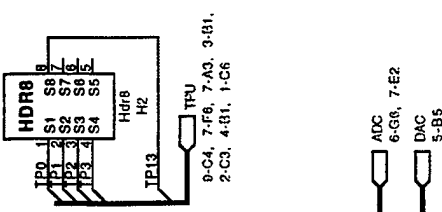
ONR GRANTS: N00014-95-1-0367 & N00014-95-1-0249

**SYSTEM
DOCUMENTATION
(STANFORD)**

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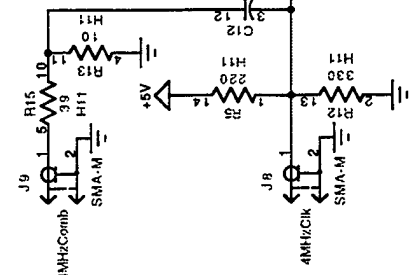


Test Points
H2

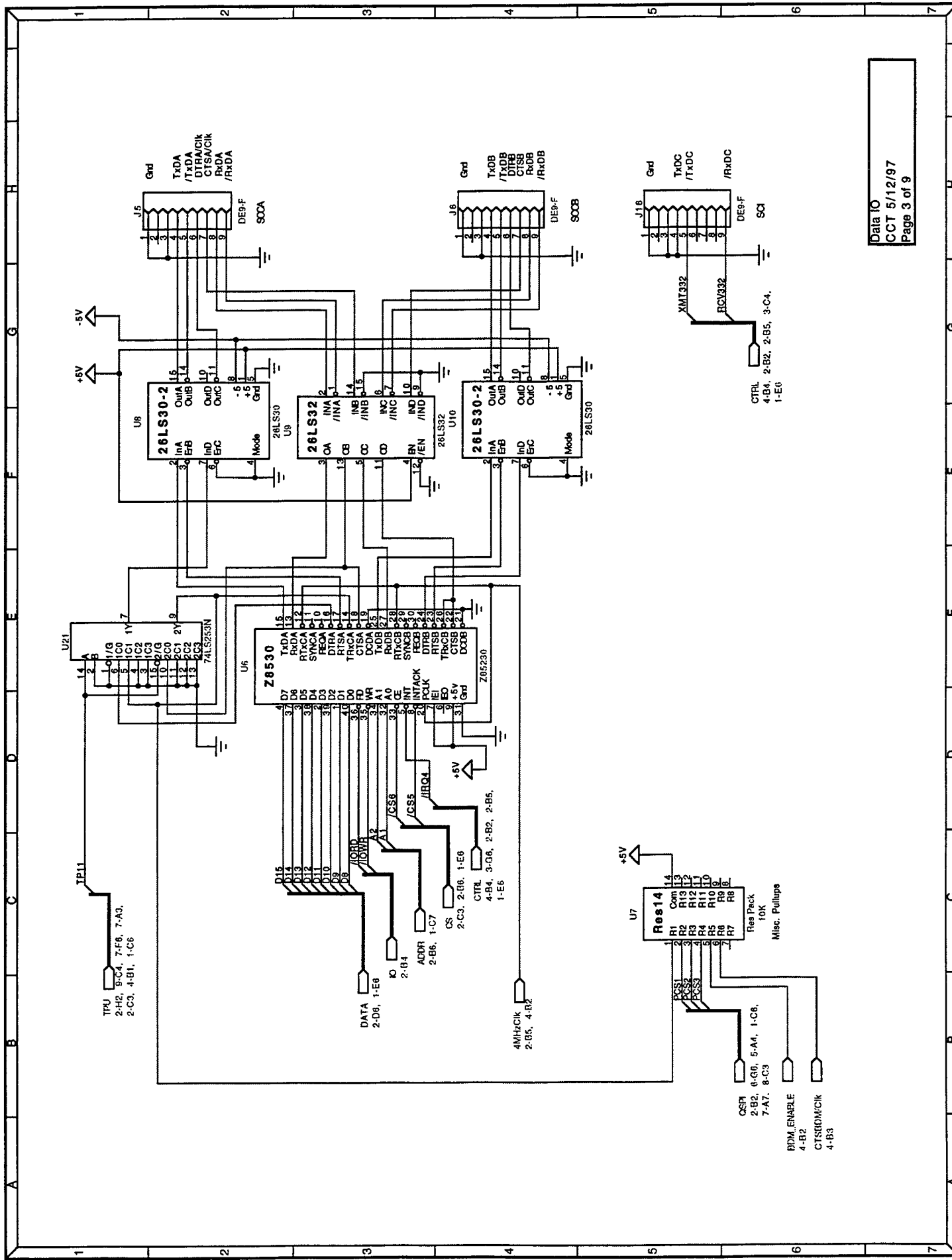


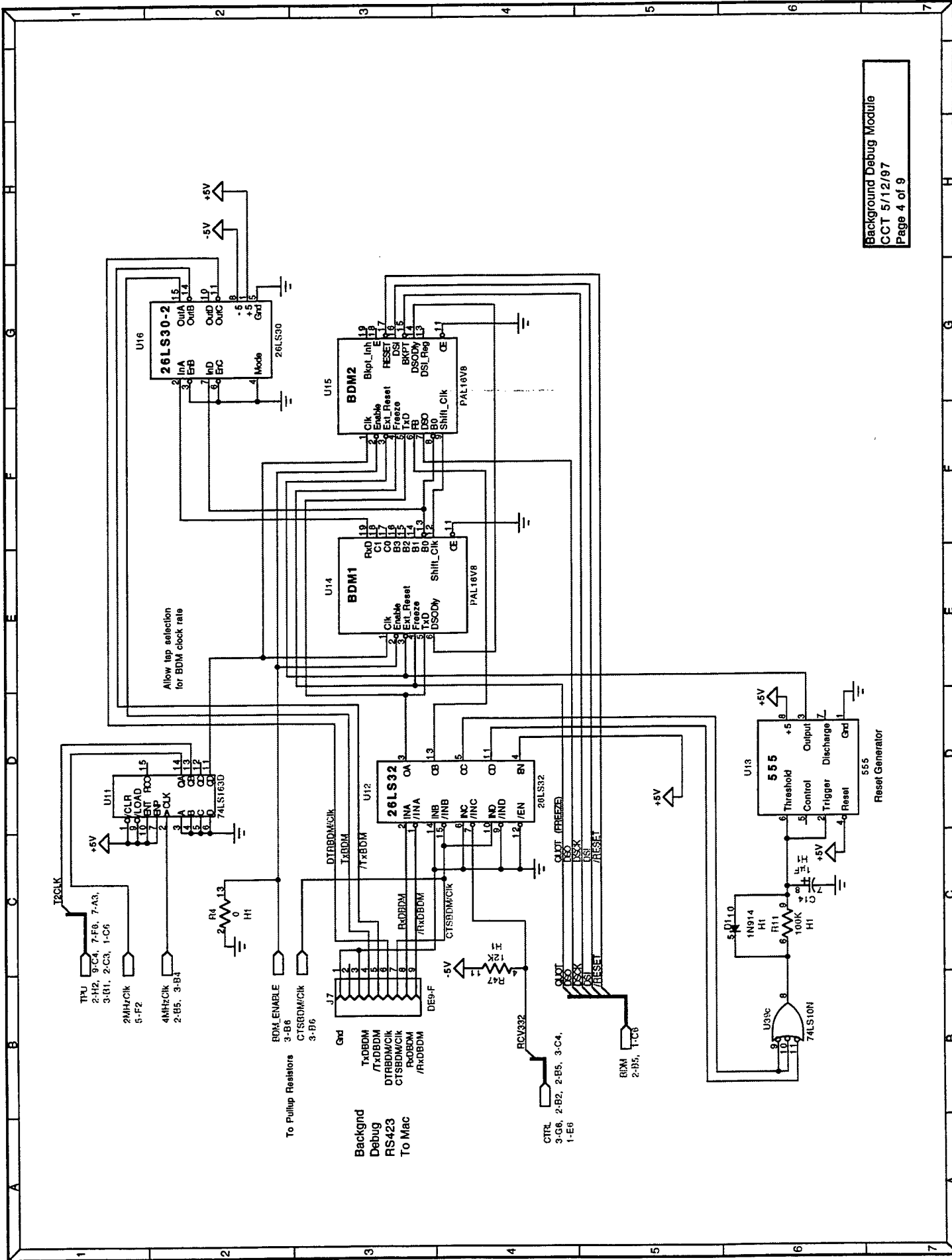
Device Selects, DDS Port
CCT 5/12/97
Page 2 of 9

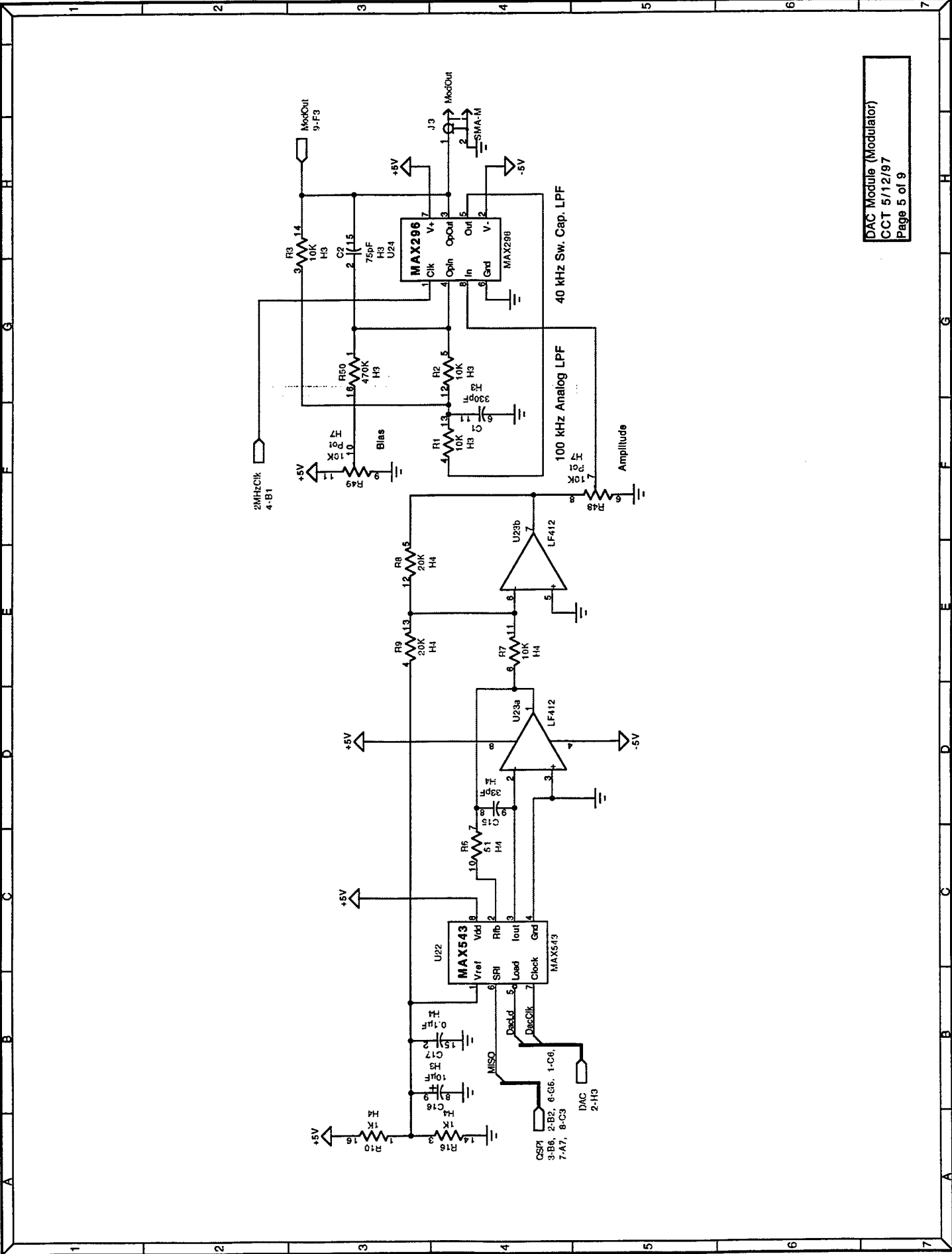
R14
1k
H1
DesignWorks doesn't allow interconnection of bus signals; fool it with 0Ω resistor.

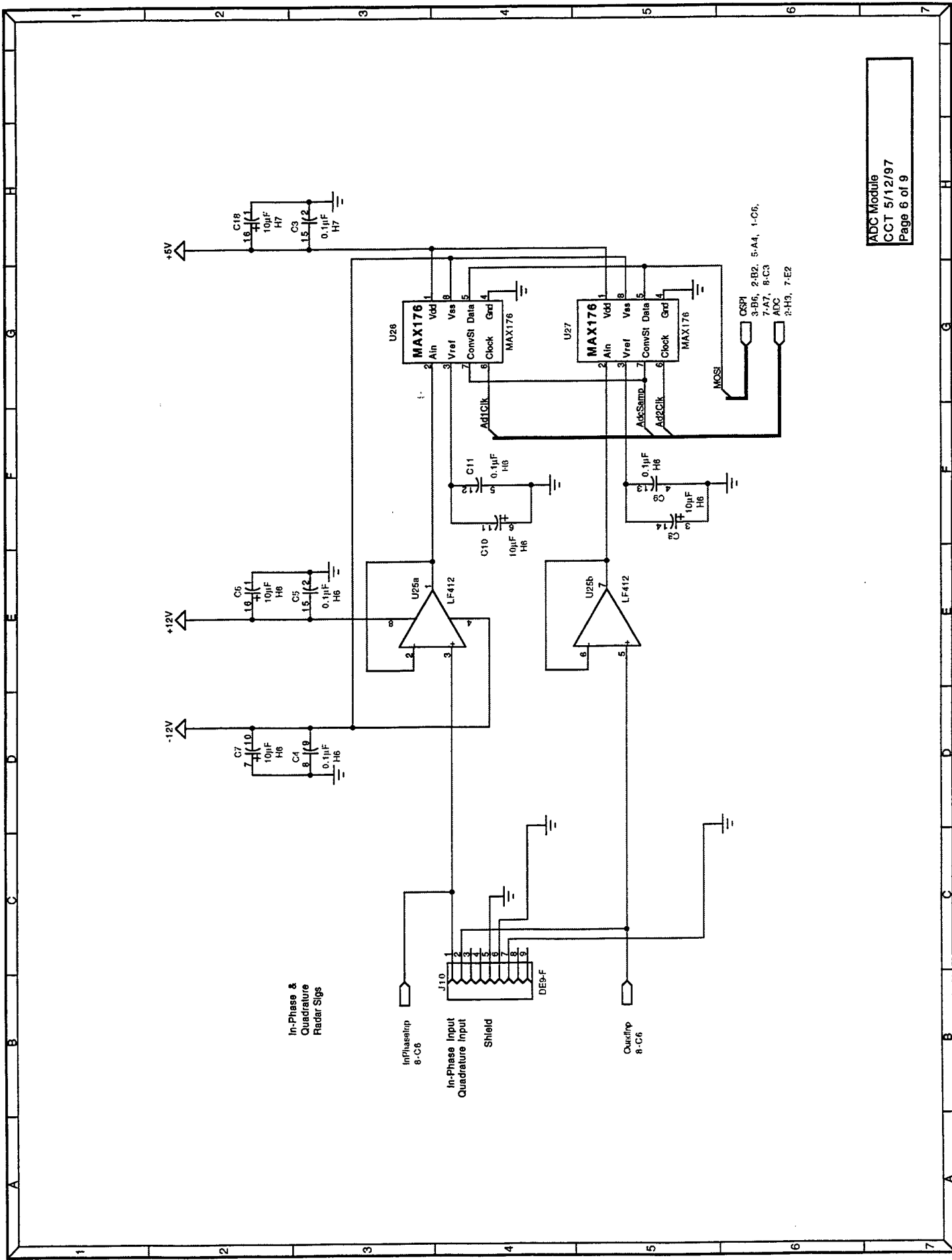


DATA
3-C3, 1-E6









In-Phase &
Quadrature
Radar Sigs

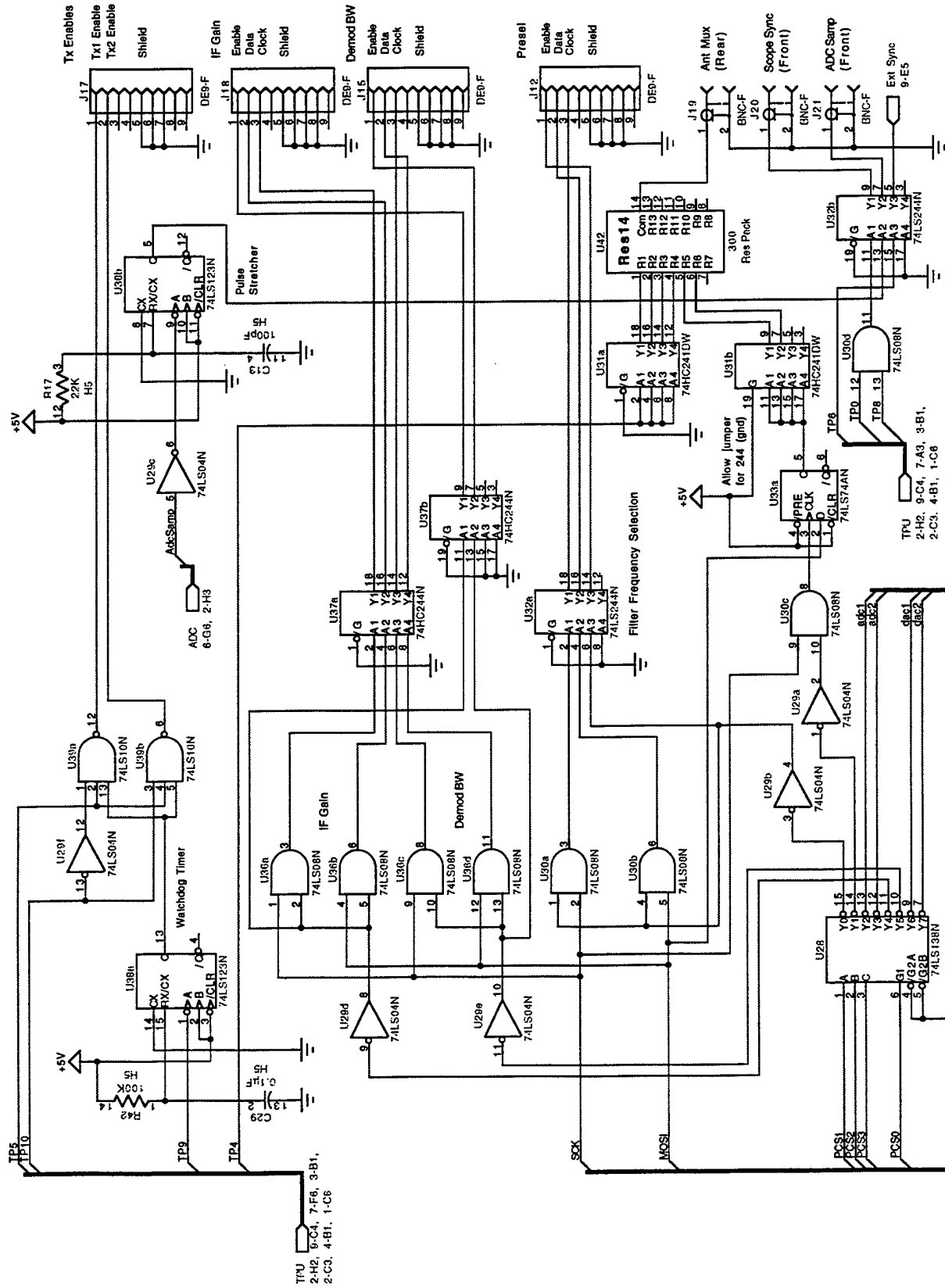
InPhaseInp
8-C6

In-Phase
Quadrature
Input

J10

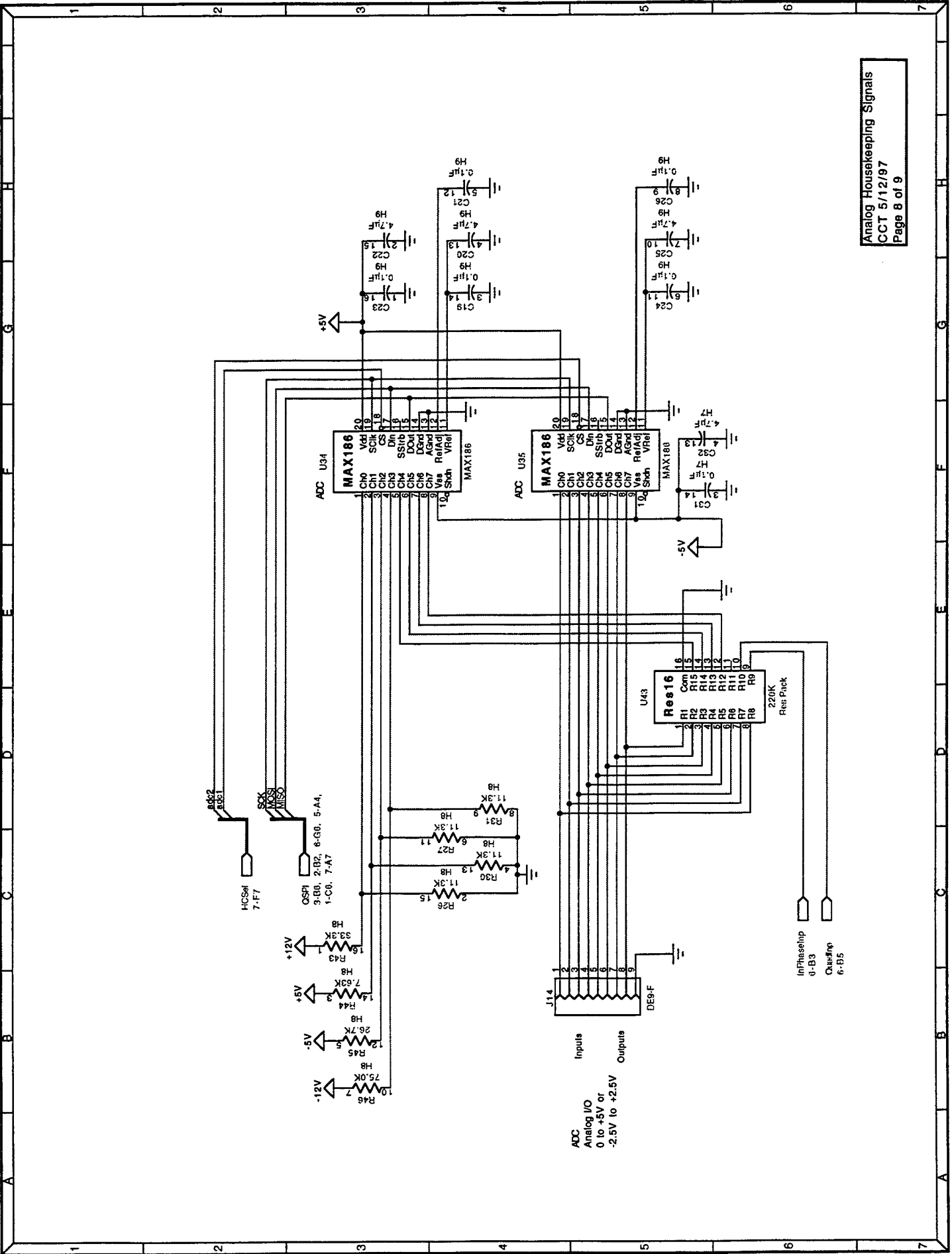
Shield

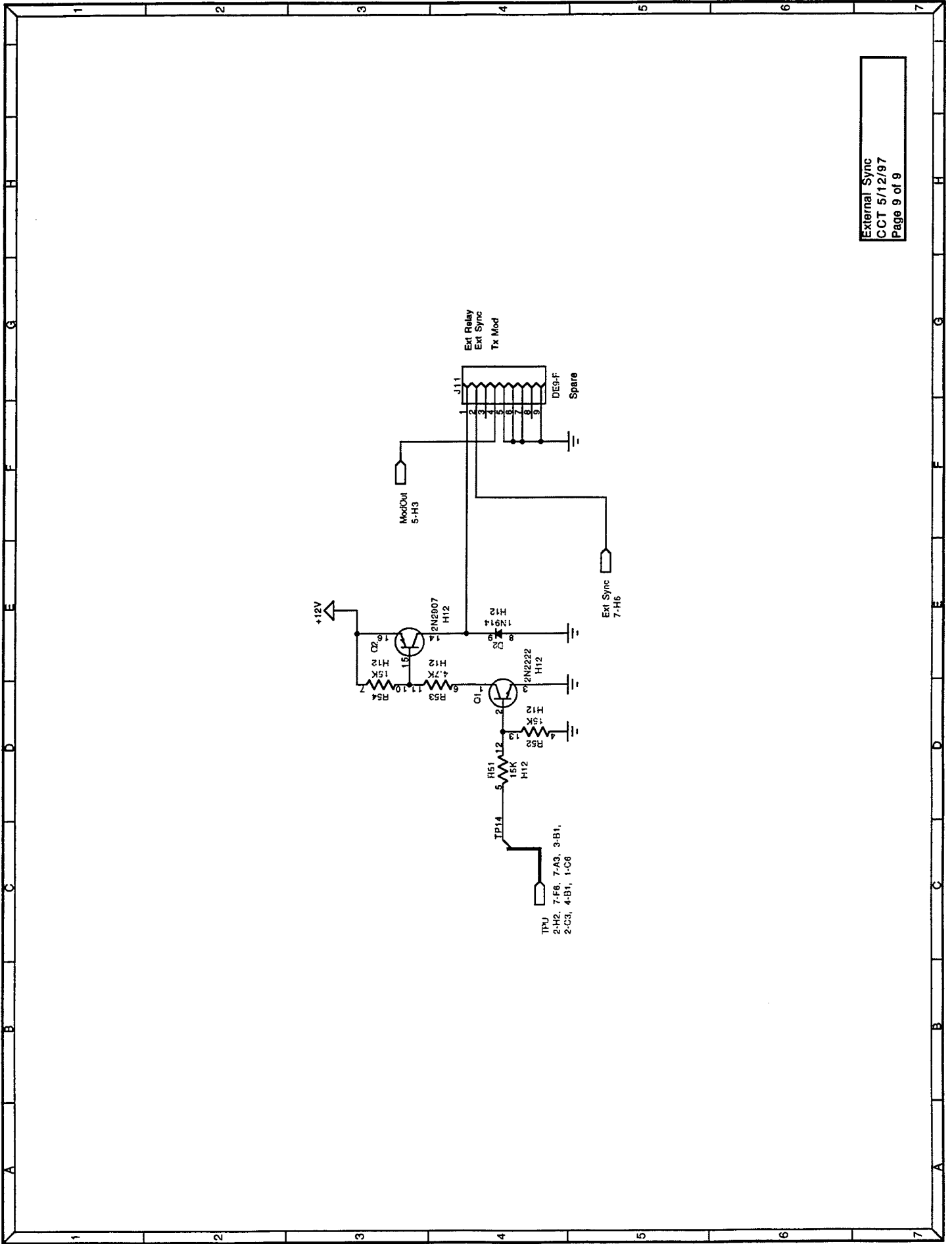
QuadInp
8-C6

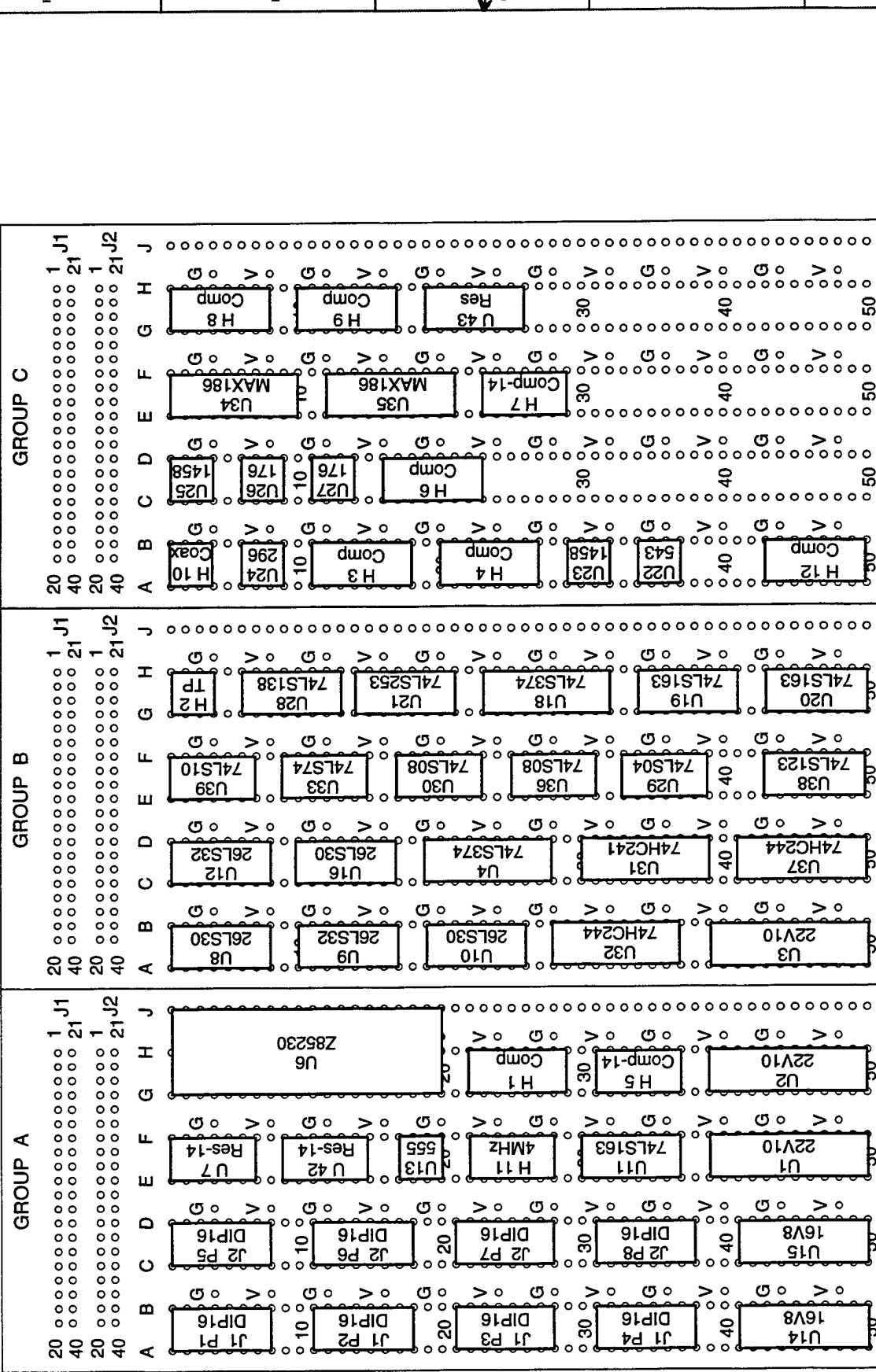


Digital Housekeeping Signals
CCT 5/12/97
Page 7 of 9

CS7 2-B2, 6-C6, 5-A4,
1-C6, 8-C3







STANFORD UNIVERSITY	68332 Field Exp Layout	DATE	1 of 1
68332 Field Experiment L/O		DRAWN	DATE
N000149510249		68332 Field Exp Layout	DATE

STANFORD UNIVERSITY

Net List
 Contoller
 Program: HF Radar
 Contract: N000149510249

NET NAME	PINS									
/CS4	P7-2	U1-7								
/CS5	P7-15	U6-8								
/CS6	P7-1	U6-33								
/CS7	P7-16	U3-5								
/CS9	P6-9	U3-7								
/DS	P8-14	U3-3								
/IORD	U3-14	U6-36								
/IOWR	U3-15	U6-35								
/IRQ4	P7-6	U6-5								
/IRQ5	P7-10	U3-16								
/IRQ6	P7-7	U1-23								
/RESET	P4-12	U3-2	U15-17							

STANFORD UNIVERSITY

Net List
Controller
Program: HF Radar
Contract: N000149510249

NET NAME	PINS									
CTSBDM/CIK	BJ2-23	U7-6	U12-10	U12-15						
D0	AJ1-39	U4-2								
D1	AJ1-38	U4-5								
D2	AJ1-37	U4-6								
D3	AJ1-36	U4-9								
D4	AJ1-35	U4-12								
D5	AJ1-34	U4-15								
D6	AJ1-33	U4-16								
D7	AJ1-32	U4-19								
D8	P5-7	U4-3	U6-40	U18-3						
D9	P5-10	U4-4	U6-1	U18-4						
D10	P5-8	U4-7	U6-39	U18-7						
D11	P5-9	U4-8	U6-2	U18-8						
D12	P6-1	U4-13	U6-38	U18-13						

NET NAME	PINS												
D13	P6-16	U4-14	U6-3	U18-14									
D14	P6-2	U4-17	U6-37	U18-17									
D15	P6-15	U4-18	U6-4	U18-18									
DATA	AJ1-40	U3-18											
DSCK	P4-13	U15-15											
DSI	P4-6	U15-16											
DSO	P4-11	U15-7											
DTRBDM/CIK	BJ2-24	U16-11											
DacCik	U2-19	U22-7											
DacLd	U2-23	U22-5											
Ext_Sync	BJ1-27	U32-5											
Ground	H3-6	H7-2	H6-8	H6-2	H6-1	H6-7	H6-3						
	H6-4	H6-6	H6-5	H5-11	H1-7	H3-8	H4-15						
	H7-1	H9-3	H9-4	H9-5	H9-2	H9-1	H9-6						
	H9-7	H9-8	H5-13	H7-3	H7-4	H12-8	P1-16						
	P1-1	P4-9	P4-8	P5-16	P5-1	P8-9	P8-8						

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Net List
 Contoller
 Program: HF Radar
 Contract: N000149510249

NET NAME	PINS									
SIG882	BJ2-32	U8-11								
SIG884	BJ2-10	U8-15								
SIG886	BJ2-27	U9-10								
SIG887	BJ2-25	U9-7								
SIG888	BJ2-26	U9-6								
SIG890	BJ2-31	U9-14								
SIG891	BJ2-29	U9-1								
SIG892	BJ2-30	U9-2								
SIG893	BJ2-28	U10-11								
SIG895	BJ2-5	U10-14								
SIG896	BJ2-6	U10-15								
SIG898	BJ2-9	U8-14								
SIG1302	U25-1	U25-2	U26-2							
SIG1318	H6-11	H6-12	U26-3							

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NET NAME	PINS								
SIG2078	U3-20	U18-11							
SIG2100	U1-8	U2-17							
SIG2110	U1-17	U19-7	U19-10	U20-7					
SIG2111	U1-18	U19-9	U20-9						
SIG2167	U3-17	U4-11							
SIG2183	U18-2	U19-3							
SIG2184	U18-5	U19-4							
SIG2185	U18-6	U19-5							
SIG2186	U18-9	U19-6							
SIG2187	U18-12	U20-3							
SIG2188	U18-15	U20-4							
SIG2189	U18-16	U20-5							
SIG2190	U18-19	U20-6							
SIG2212	U19-15	U20-10							

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Net List
 Controller
 Program: HF Radar
 Contract: N000149510249

NET NAME	PINS									
SIG2574	U28-15	U29-3								
SIG2575	U29-4	U30-1	U30-4	U32-6						
SIG2578	BJ1-31	U32-16								
SIG2580	U31-18	U42-1								
SIG2581	U31-16	U42-2								
SIG2582	U31-14	U42-3								
SIG2583	U31-12	U42-4								
SIG2585	U31-7	U42-6								
SIG2610	H9-14	H9-13	U34-11							
SIG2611	H9-12	U34-12								
SIG2612	H8-15	H8-16	U34-1							
SIG2613	H8-11	H8-12	U34-3							
SIG2616	H8-13	H8-14	U34-2							
SIG2617	H8-9	H8-10	U34-4							

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NET NAME	PINS									
SIG2622	H9-11	H9-10								
SIG2623	H9-9	U35-12								
SIG2644	U31-11	U31-13	U31-15	U31-17	U33-5					
SIG2646	U30-8	U33-3								
SIG2841	U36-11	U37-8								
SIG2843	U29-8	U36-2	U36-5	U37-11						
SIG2844	U36-3	U37-2								
SIG2847	U36-6	U37-4								
SIG2850	U36-8	U37-6								
SIG2856	BJ1-35	U37-12								
SIG2864	U28-11	U29-9								
SIG2880	U29-10	U36-10	U36-13	U37-13						
SIG2942	H5-2	H5-1	U38-15							
SIG2946	U38-13	U39-5	U39-13							

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Net List
 Controller
 Program: HF Radar
 Contract: N000149510249

NET NAME	PINS							
SIG2961	BJ2-40	U39-12						
SIG2967	U29-12	U39-1						
SIG2975	BJ2-39	U39-6						
SIG2995	BJ1-38	U37-18						
SIG2996	BJ1-40	U37-9						
SIG3006	BJ1-39	U37-16						
SIG3008	BJ1-34	U37-14						
SIG3012	BJ1-36	U37-7						
SIG3023	BJ1-30	U32-18						
SIG3024	BJ1-32	U32-14						
SIG3025	U32-13	U38-5						
SIG3028	AJ1-21	U32-9						
SIG3029	AJ1-22	U32-7						
SIG3049	U30-11	U32-11						

Net List
 Controller
 Program: HF Radar
 Contract: N000149510249

STANFORD UNIVERSITY

FSCM No.: 0TK73

Revision: X2
 Page 16 of 20

NET NAME	PINS									
SIG3167	CJ1-18	U35-8	U43-1							
SIG3168	U12-5	U39-9	U39-10							
SIG3173	U12-13	U15-6								
SIG3185	H1-8	H1-10	H1-9	U13-2	U13-6					
SIG3186	H1-5	H1-6	U39-8							
SIG3207	H4-5	H7-8	U23-7							
SIG3213	H7-10	H3-16								
SIG3215	H3-2	H3-5	H3-1	U24-4						
SIG3220	H12-1	H12-6								
SIG3223	H12-9	BJ1-28	H12-14							
SIG3226	H12-2	H12-12	H12-13							
SIG3228	H12-15	H12-11	H12-10							
SIG3284	CJ1-40	U35-1	U43-8							
SIG3285	CJ1-39	U35-2	U43-7							

Vesta SBC332 Family Hardware Manual

vesta technology, inc.

7100 W. 44th Ave, Suite 101, Wheat Ridge, CO 80033, (303) 422-8088, (303) 422-9800 (FAX)

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Vesta will repair without charge any assembly or defects on units returned within the original warranty period. Testing and repair of user-damaged units, or units with expired warranties will be charged based on time and materials.

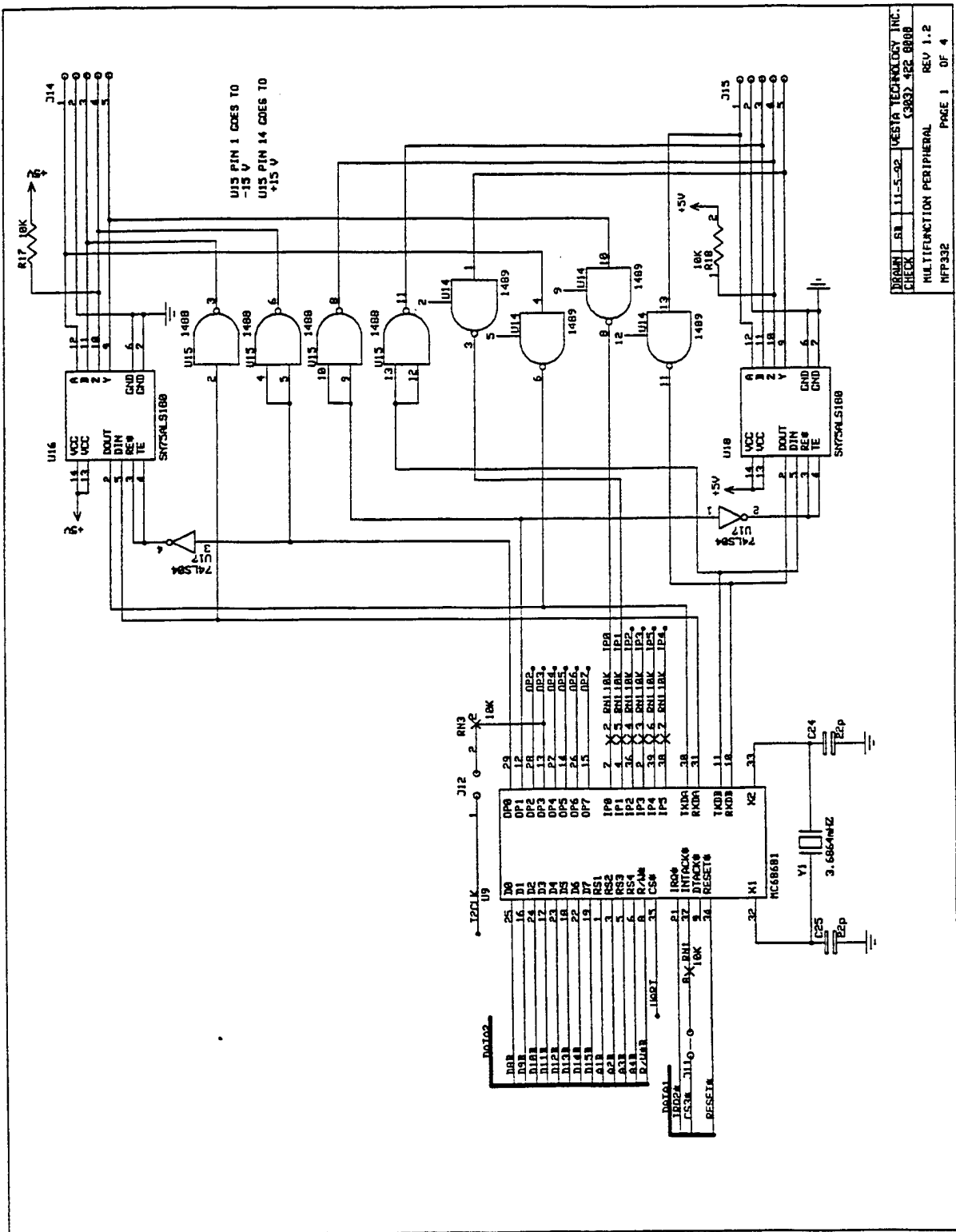
**SBC332 Hardware Manual Rev. 1.3
Board Rev. 1.2 Errata**

SBC332 Manual

Board Revision Level 1.2: TPU channels 1 and 5 are configured for use with the serial transceiver, U7. Unlike board revision 1.3, there is no jumper J12 to release TPU channel 1 from the serial transceiver. To provide this feature and free channel 1 for other use, remove the serial transceiver U7, bend pin 10 outward, and re-install U7. To release channel 5 from the serial transceiver, remove jumper J10. With both channels 1 and 5 released, all the TPU channels are available without restriction for the user in any functionality as described in the Motorola TPU documentation.

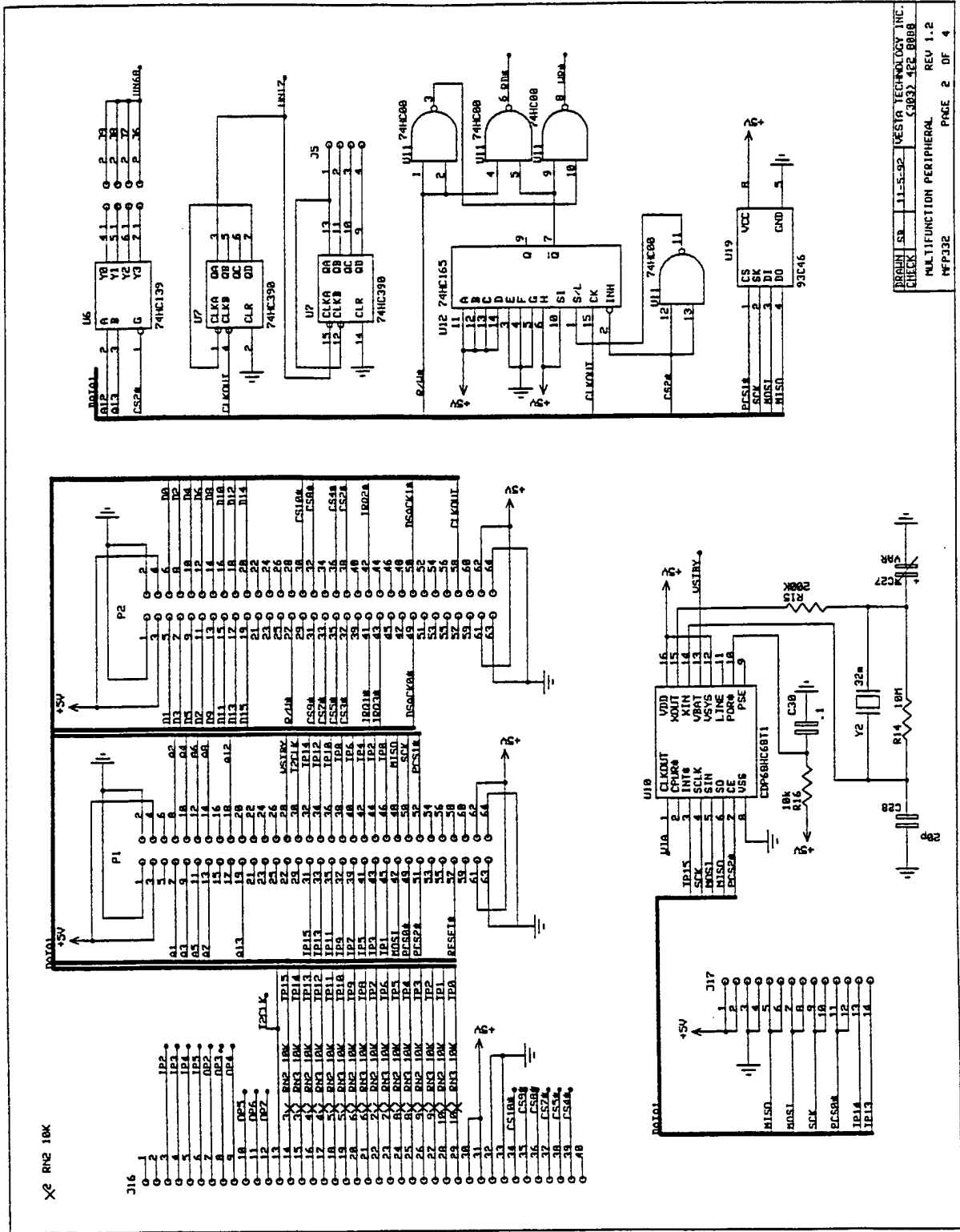
September 20, 1993

SCHEMATIC, PART 1

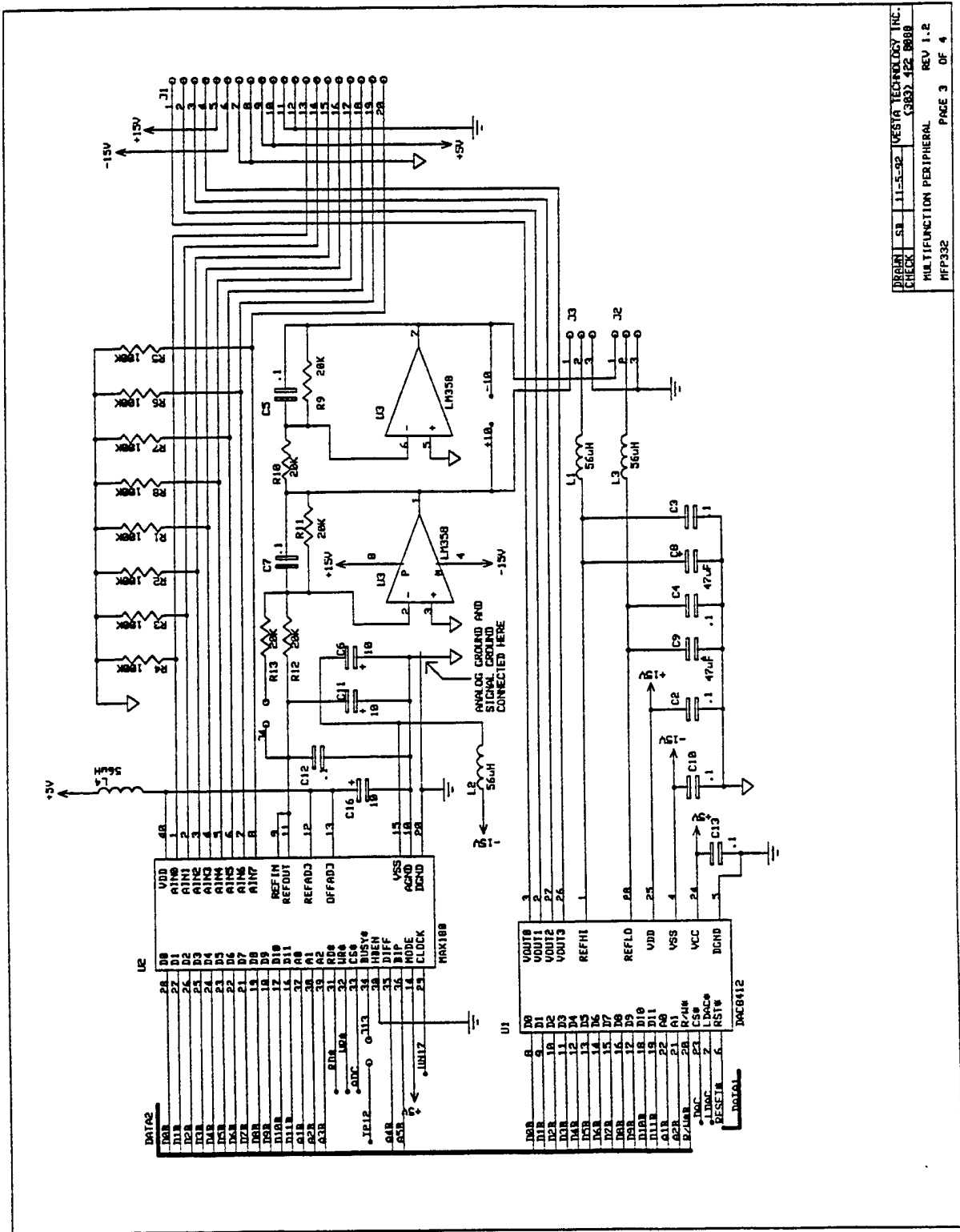


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 MULTIFUNCTION PERIPHERAL REV 1.2
 MFP332 PAGE 1 OF 4

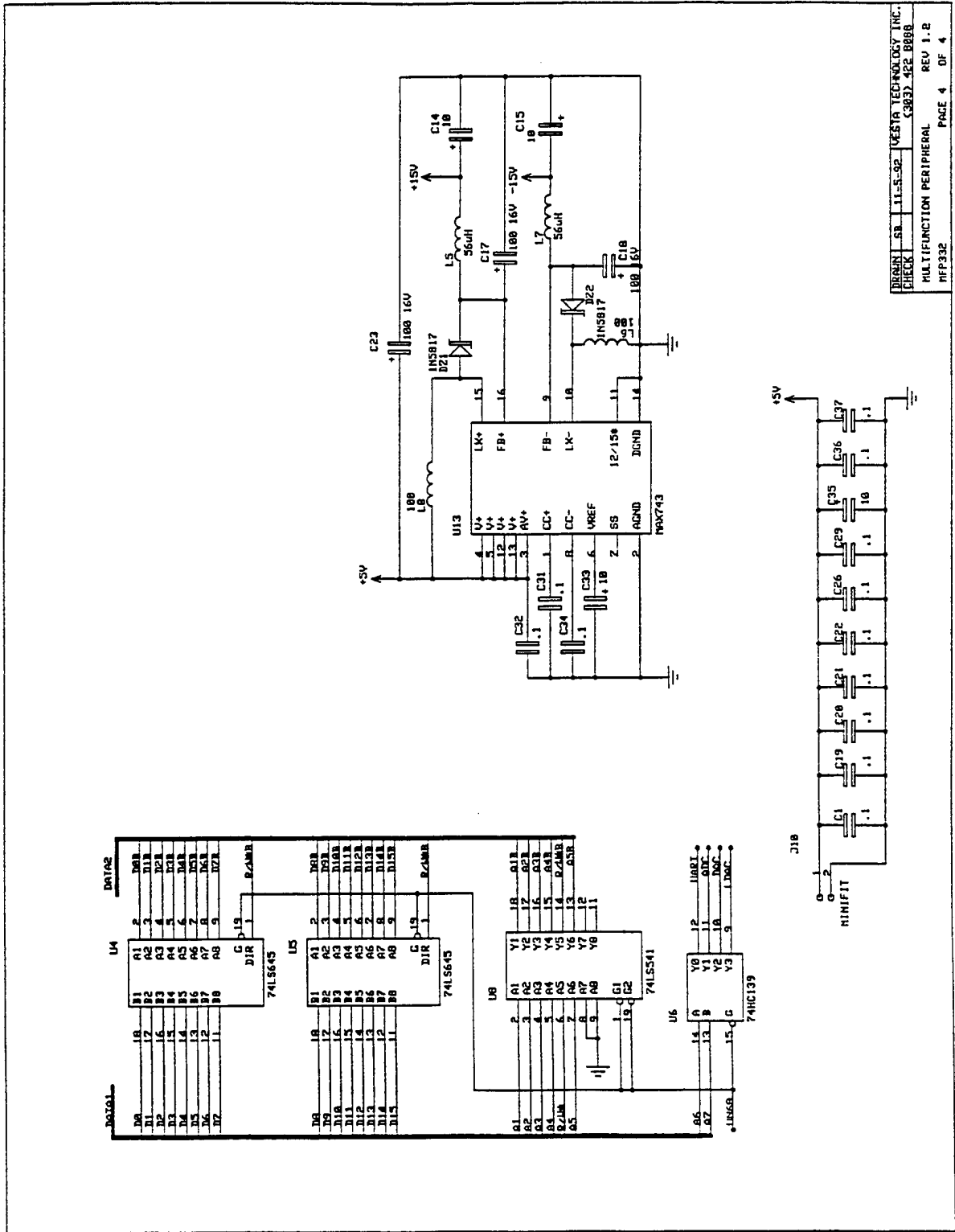
SCHEMATIC, PART 2



SCHEMATIC, PART 3



SCHEMATIC, PART 4



DESIGN CHECK SR 1.1-5-92 VESTA TECHNOLOGY INC. (303) 422-8088
 MULTIFUNCTION PERIPHERAL REV 1.2
 MFP332 PAGE 4 OF 4

The Use of 512k x 8 Pseudo-Static RAM Devices on the SBC332

It is possible to use 512kbyte pseudo-static RAM devices (psRAMs) on the SBC332 to obtain one megabyte of onboard RAM. There is a limitation which must be dealt with, however, and which has certain consequences. This limitation is that the psRAMs must be refreshed similarly to dynamic RAM devices. The refresh process requires reading each of the first 2kbytes of each device at least once every 32 milliseconds. The consequences are that the internal periodic interrupt timer (or some other interrupt source) is required to provide reliable invocation of the refresh function. Additionally, the overhead of refreshing the RAMs will cause the system to run slightly more slowly than when using fully-static RAMs.

Vesta Technology has written a short application program for VFSE-332 which will perform this refresh operation. It is found in the file PSEUDRAM.F on the utilities disk. In order to use psRAMs, this application must be placed into a pair of application EPROMs and configured as an autostart application. This means that you *must* have "normal" (static) RAM devices installed while you compile PSEUDRAM.F and save the new EPROM image. Once you have a new working set of EPROMs with this application autostarting, you can replace the static RAM devices with psRAMs.

If you are working in C or assembly, then you will have to incorporate the periodic refresh capability into your application code. The following assembly-language routine has been translated from VFSE-332 assembly format to Motorola assembly format. It has *not* been tested in this form.

```
PICR_value equ      $07FF          ; level 7 interrupts, vector $FF
PITR_value equ      $00F0          ; interrupt every 29.3 milliseconds
RAM_BASE equ       $100000        ; start of RAM for VFSE-332

refresh:
    movem.l    d0-d1/a0, -(a7)    ; preserve D0, D1, and A0
    move.l     #1024, d1          ; number of 32-bit words to read
    move.l     RAM_BASE, a0

refresh_loop:
    move.l     (a0)+, d0           ; read 2 bytes from each device
    dbra      d1, refresh_loop
    movem.l    (a7)+, d0-d1/a0    ; restore the scratch registers
    rte
```

The address of the label "refresh" must be placed into the exception vector number \$FF, and the periodic interrupt timer registers of the 68332 programmed with PICR_value and PITR_value. This code assumes that the 68332 is running at the full 16MHz clock speed. If you change the clock frequency of the 68332, you will have to change the PITR_value in order to keep interrupt occurring more often than once every 32 milliseconds.

Using this routine does require the use of the periodic interrupt timer capabilities of the 68332. If you need the periodic interrupt for other purposes, you will have to make the necessary modifications and compensations to allow the periodic interrupt timer to be shared by the functions, or you will have to provide some other manner of invoking the psRAM refresh.

vesta technology
SBC332

Revision 1. 3
April 16, 1993

Vesta Technology, Inc.
7100 W. 44th Ave
Wheat Ridge, CO 80033

(303) 422-8088 (voice)
(303) 422-9800 (FAX)

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The SBC332

The SBC332 is closely related to the original Motorola "Business Card Computer" (BCC). The SBC332 is designed as a complete standalone engine for high performance OEM products. The SBC332 also supports the Vesta **WRITE IT • RUN IT • ROM IT** easy development process. Consequently, the SBC332 has several advantages over the BCC.

- DIP socketed, readily-available byte-wide memory devices
- choice of onboard memory device (RAM and/or ROM) size
- Socketed microprocessor for easy replacement
- Onboard reset generator
- Continuous-cycling external watchdog timer
- Power supply monitor
- Internal RAM backed for one hour
- BCC-compatible external bus pinout
- **Low cost, productive development environment.**

P1 and P2 Installation

The two 64 position Dual Row Headers, P1 and P2, have been supplied separately. You have the option of installing these connectors on either the solder or component side of the the SBC332 depending on your mechanical mounting requirements. Please specify your desired production configuration when you reorder.

Please note that these connectors must be installed on the component side for the pin numbers to be consistent with insulation displacement cables. P1 and P2 must be mounted on the component side for attachment to any other Vesta standard product.

Quick Start

If you also purchased Vesta Forth Standard Edition for the SBC332 (VFSE-332), you can quickly bring up and test your Vesta SBC332. You need:

- A personal computer with text editor, communications program and serial port.
- An RS-232 cable from your computer to the SBC332 serial connector J5.
- A +5 Volt at 150 mA supply with cable to SBC332 power connector J1.
- Vesta Forth Standard Edition for the SBC332 (VFSE-332).

Turn on your personal computer. Start your favorite telecommunications program. Set the communications parameters for 8 data bits, no parity, 1 stop bit, 9600 baud.

Connect the serial cable to the SBC332 at J5 (See diagram on page 7). Pin 1 of J5 is marked with an silkscreened asterisk on the SBC332.

Apply power to J1. Ground (-) and positive (+) are silkscreened on the board.

J1

Pin	Description
1	+5 VDC at 150 mA
2	Ground return

J1 POWER CONNECTOR

Once the serial cable is connected properly and power applied to the SBC332, your personal computer communications program will display the sign on message:

```
Vesta Forth Standard Edition - SBC332
Generated: yyymmdd
```

on your screen. yyymmdd are numbers which indicate the revision date (year, month, and date) of the VFSE-332 EPROMs. If you do not see this or a similar message, check the power connection, and try reversing the serial cable at J5. Reapply power.

Once you see the sign-on prompt, you may interactively compose and test Forth programs directly on the SBC332. Alternatively Using a text editor (or a word processor in text mode) in conjunction with your communications program on your personal computer, you can also download text files. An EPROM programmer capable of programming 27C256 or larger EPROMs is all that it takes to complete your embedded system development environment.

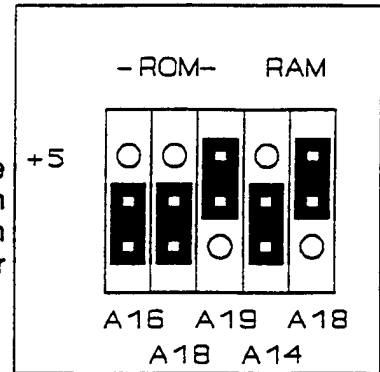
For more information on Vesta Forth Standard Edition, see the *Vesta Forth Standard Edition Manual*.

Memory

The SBC332 will accommodate either 32-pin or 28-pin byte-wide memory devices in 0.6" wide sockets. When 28-pin devices are inserted into the 32-position sockets, pins 1, 2, 31 and 32 of the socket should be empty.

Memory Selection

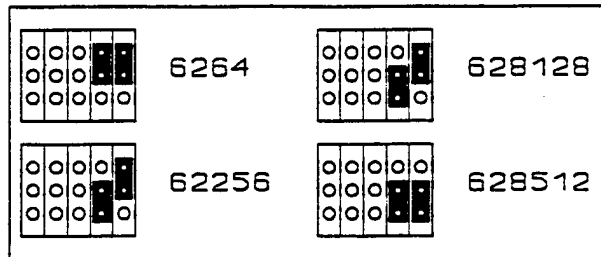
RAM and ROM devices of various capacities may be installed in the SBC332. In general, a few pins must be accommodated to switch between these sizes. Jumper block J2 allows a variety of devices and is shown in Figure 1. The orientation of the diagram is such that the dual-row header P2 would be to the right of the jumper block shown.



RAM

Sockets U6 (RAM HI) and U2 (RAM LO) contain 8k/32k/128k/512k static RAM integrated circuits in .6" wide DIP packages. The SBC332 requires two RAMs of equal capacity.

The figure at the right indicates Jumper J2 positions for the various devices. The table below summarizes the pins and their functions that must be changed to change RAM size. "Pin 28" and "pin 30" refer to a 32 pin DIP integrated circuit. Once again, the orientation of the diagram is such that the dual-row header P2 would be to the right of the jumper block(s) shown.



Size	Type	Pin 28	Pin 30
8k	6264	+5	+5
32k	62256	A14	+5
128k	628128	A14	+5
512k	628512	A14	A18

SRAM SIZES, TYPES AND VARIANT PIN DESCRIPTIONS

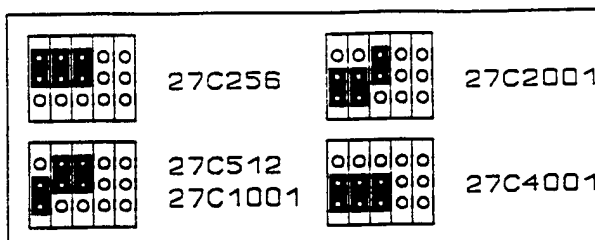
Pins 28 of both RAMs are connected to the fourth jumper position. Pins 30 of both RAMs are connected to the fifth jumper position.

ROM

Sockets U5 (ROM HI) and U1 (ROM LO) contain 32k/64k/128k/256k/512k byte wide EPROMs in 0.6" wide DIP packages. Again, two identical ROM devices must be installed.

The figure at the right indicates Jumper J2 positions for the several devices. Once again, the orientation of the diagram is such that the dual-row header P2 would be to the right of the jumper block(s) shown.

The table below shows the connections needed to accommodate these choices. "Pin 3", "pin 30" and "pin 31" refer to a 32 pin DIP integrated circuit. In some cases, such as when inserting a 28 pin device into a



32 pin socket, some integrated circuit pins are not connected. This is noted in the table as "nc". The jumper may be left unconnected or, alternatively, tied to +5.

Size	Type	Pin 3	Pin 30	Pin 31
32k	27C256	+5	+5	nc (+5)
64k	27C512	A16	+5	nc (+5)
128k	27C1001	A16	nc(+5)	+5
256k	27C2001	A16	A18	+5
512k	27C4001	A16	A18	A19

EPROM SIZES, TYPES AND VARIANT PIN DESCRIPTIONS

Pins 3 of both EPROMs are connected to the first jumper, pins 30 to the second jumper and pins 31 to the third jumper.

Battery Backed RAM

There are three choices of backup for the onboard RAM; an external battery, the onboard supercap or Dallas Semiconductor Smart Sockets. If an external battery is used, connect an appropriate sized battery pack to J6 and install a jumper on J7. If the onboard supercap is used to supply power to RAM during power down, install a jumper on J7.

J6

Pin	Description
1	Ground (Battery -)
2	External pwr for all RAM (Battery +)

BATTERY BACKUP CONNECTOR

Normally the supercap is used to provide backup power to the 2k bytes of internal RAM in the 68332 microprocessor. The supercap will support internal memory for approximately twenty-four (24) hour. Installing jumper J7 places the supercap in parallel with the external battery, thus connecting internal RAM to the external battery through a Schottky diode, and also connecting on-board external RAM to the supercap. In this situation, the supercap will preserve the 2k bytes of internal RAM and the two (2) external SRAMs on the SBC332 for approximately eight (8) hours. When a Vesta MFP332 with realtime clock option installed is connected to an SBC332, the realtime clock is always supercap-backed, regardless of jumpering state. In such cases, the time which the supercap will preserve the 2K bytes internal RAM and the external SBC332 SRAM plus keep the MFP332's realtime clock running is reduced to one (1) hours.

Note: All times given are approximate and conservative and probably vary with individual boards and super-capacitors.

J7

Pin	Description
1	Supercap
2	RAM socket power

SUPERCAP & BATTERY BACKUP JUMPER

Note: It is not possible to provide battery backup for 28-pin RAM devices. The battery backup capabilities of the SBC332 are restricted to 32-pin RAM devices.

The third option for battery backed RAM is to install Dallas Semiconductor DS1213D adaptor sockets into positions U2 and U6. Note that it is not necessary to battery back both sockets if your storage requirements are minimal. The maximum sized memory device that may be installed is limited to 128k bytes per socket due to an internal connection between pins 30 and 32 in the smart socket. This option will, however, battery back 28 pin devices.

Battery Backed Real Time Clock

The Dallas Semiconductor DS1216D may be installed under either RAM socket to provide both battery backed data storage and Real Time Clock function. The same 128k byte limitation exists as with the DS1213D.

Memory Speed

The SBC332 can accommodate many speeds of memory and peripheral devices. The 68332 microcontroller allows all chip selects generated by the 68332 to have up to 13 programmable wait states. When the microcontroller powers up, the boot EPROM's chip select, CSBOOT* is configured for thirteen (13) wait states. Vesta Forth Standard Edition (VFSE) promptly reprograms CSBOOT* and the SRAM chip selects CS0* and CS1* to have three (3) wait states. In conjunction with VFSE's reprogramming of SYNCR, the 68332 Clock Synthesizer Control Register, from the powerup 8.38 MHz to the top rate available (16.777 MHz at this writing), the maximum allowable access time for external memory dictates 200 nS access time devices or better.

If you are using a program development system other than VFSE, the number of wait states programmed into the chip selects and the clock rate programmed into the clock synthesizer circuitry may be under your control, in which case the following discussion still merits your attention.

Access time alone is not the sole determining factor in the timing requirements of the SBC332. The time to "Data Float" is also of concern to prevent bus contention during the next bus cycle. The 68332 will deactivate chip selects 15 nS before the end of a memory cycle. The next cycle chip select may be activated as soon as 15 nS into the next cycle. Therefore, peripheral chips must release their data bus drivers within 30 nS, otherwise bus contention may result from the previous cycle's selected chip lingering on the data bus while the currently selected chip is putting its data onto the bus. Usually the EPROMs will be the slowest component in the system to float the data bus. Adding wait states to the next bus cycle will give the bus time to settle down after the contentious period is resolved. Although data float times are generally not a purchasing parameter, it is usually true that the faster the access time, the faster the data float time.

One wait state has a duration of one clock cycle, which is approximately 60 nS at 16.78 MHz. With no wait states inserted, a peripheral must respond within 80 nS of activation of its chip select input. High temperature and low supply voltage worsen CMOS access times. Typical reduction to access times at 4.5

Volts and 70 degrees C. are as much as 40%. This is mentioned for your information during evaluation only, as published access times are worst case.

Watchdog Timer and Power Supply Monitor

The watchdog timer and power supply monitor will be strobed periodically by CS2* if J3 pins 1 and 2 are shorted. If CS2* is not strobed every 600 mS the DS1232 will reset the system. This watchdog timer will produce a continuous series of reset pulses until proper operation is restored.

The watchdog timer can be defeated by moving the shorting jumper on jumper J3 to pins 2 and 3. This can be useful during development. In this position, CLKOUT supplies the needed strobe signal.

The power supply monitor will cause a system reset to occur when the +5 supply is 10% or more out of tolerance. The system will be held in reset until proper supply tolerance is restored.

J3

Pin	Description
1	CS2*, output from 68332
2	Watchdog strobe, input to DS1232
3	CLKOUT, output from 68332

WATCHDOG STROBE JUMPER

Watchdog Timeout Period

Jumper J9 selects the watchdog timeout period as shown in the diagram.

J9

J9	Period
open	600 ms
1 - 2	1200 ms
2 -3	150 ms

Pushbutton Reset

A pushbutton reset function may be implemented by installing a momentary contact switch at J4.

J4

Pin	Description
1	Ground
2	Pushbutton reset input to DS1232

PUSHBUTTON RESET CONNECTOR

Serial Ports

The RS-232-level serial ports are available at J5. Port A is assigned to the MC68332 SCI channel. Port B is intended for a software UART implementation. Both channels are brought to RS-232 level by the LT1280 RS-232 transceiver in socket U7.

J5

Pin	I/O	Description
1	O	TxDA - RS-232
2	GND	GroundA
3	I	RxDA - RS-232
4	O	TxDB - RS-232
5	GND	GroundB
6	I	RxDB - RS-232

RS-232 SERIAL PORT CONNECTOR

Jumper J10 and Software Control of Serial Transceiver

Jumper J10 when installed allows TPU Channel 5 to enable and disable the serial transceiver under software control: when TPU5 is set logic-high, the LT1280 is enabled; when TPU5 is set low under software control, the LT1280 is disabled. (This feature is especially useful in conjunction with low-power operation, since the LT1280 enabled can draw current in the vicinity of 10 mA, as opposed to somewhat more than

1 μ A disabled.) Should it be desirable in the context of an application to use TPU Channel 5 for another purpose, jumper J10 may be removed, in which case the serial transceiver is automatically enabled by a pullup resistor. **Note:** *The SBC332 is shipped with jumper J10 removed. If jumper J10 is installed during development, please note that the powerup default of the MC68332 microcontroller is TPU5 low.*

Second Software Serial Port and Jumper J12

TPU Channel 4 serves as the Port B TxD input to the LT1280 RS-232 transceiver. TPU Channel 1 serves as the Port B RxD output. Vesta Forth Standard Edition features a full-source implementation of a second serial port utilizing these TPU channels.

Should it be desirable in the context of an application to use TPU Channels 1 and 4 for another purpose, losing use of the second asynchronous serial port, jumper J12 may be removed. Removing jumper J12 disconnects the transceiver output from TPU Channel 4. (It is not necessary to disconnect the transceiver input from TPU Channel 1 in order to be able to use TPU Channel 1 for a task other than the second asynchronous serial port.)

Background Mode Connector

J8 is available as the Motorola standard debugging interface.

J8

Pin	I/O	Description
1	I	Ground
2	I	DSCLK
3	I	Ground
4	O	QUOT
5	I/O	RESET*
6	O	DSI
7	O	Vcc
8	O	DSO

BACKGROUND MODE CONNECTOR

BCC Connectors

Every attempt has been made to conform to the standard set by Motorola's BCC (Business Card Computer) pinout. The only differences which exist are in the areas of programming the system EPROM in-place (which is impossible on the SBC332). The following tables show the pinouts of the two principal offboard connectors (P1 and P2) on the SBC332.

P1

Pin	I/O	Description	Pin	I/O	Description
1	-	Ground	2	-	Ground
3	-	Vcc	4	-	Vcc
5	-	no connection	6	O	A0
7	O	A1	8	O	A2
9	O	A3	10	O	A4
11	O	A5	12	O	A6
13	O	A7	14	O	A8
15	O	A9	16	O	A10
17	O	A11	18	O	A12
19	O	A13	20	O	A14
21	O	A15	22	O	A16
23	O	A17	24	O	A18
25	-	no connection	26	-	no connection
27	-	no connection	28	I	VSTBY
29	-	no connection	30	I	T2CLK
31	I/O	TP15	32	I/O	TP14
33	I/O	TP13	34	I/O	TP12
35	I/O	TP11	36	I/O	TP10
37	I/O	TP9	38	I/O	TP8
39	I/O	TP7	40	I/O	TP6
41	I/O	TP5	42	I/O	TP4
43	I/O	TP3	44	I/O	TP2
45	I/O	TP1	46	I/O	TP0
47	O (I)	MOSI	48	I (O)	MISO
49	O	PCSO	50	O	SCK
51	O	PCS2	52	O	PCS1
53	O	TxD	54	O	PCS3
55	I	DSCK	56	I	RxD
57	I/O	RESET*	58	O	QUOT
59	O	DSO	60	O	DSI
61	-	VCC	62	-	VCC
63	-	GND	64	-	GND

P2

Pin	I/O	Description	Pin	I/O	Description
1	-	Ground	2	-	Ground
3	-	Vcc	4	-	Vcc
5	I/O	D1	6	I/O	D0
7	I/O	D3	8	I/O	D2
9	I/O	D5	10	I/O	D4
11	I/O	D7	12	I/O	D6
13	I/O	D9	14	I/O	D8
15	I/O	D11	16	I/O	D10
17	I/O	D13	18	I/O	D12
19	I/O	D15	20	I/O	D14
21	-	no connection	22	-	no connection
23	-	no connection	24	O	XMT232
25	O	CSBOOT*	26	I	RCV232
27	O	R/W*	28	I	MODCK
29	I	TSC	30	O	CS10*
31	O	CS9*	32	O	CS8*
33	O	CS7*	34	O	CS6*
35	O	CS5*	36	O	CS4*
37	O	CS3*	38	O	CS2*
39	O	CS1*	40	O	CS0*
41	I	IRQ1*	42	I	IRQ2*
43	I	IRQ3*	44	I	IRQ4*
45	I	IRQ5*	46	I	IRQ6*
47	I	IRQ7*	48	I	BERR*
49	I	DSACK0*	50	I	DSACK1*
51	I	AVEC*	52	O	RMC*
53	O	DS*	54	O	AS*
55	O	SIZ0	56	O	SIZ1
57	-	no connection	58	O	CLKOUT
59	-	no connection	60	I/O	HALT*
61	-	Vcc	62	-	Vcc
63	-	Ground	64	-	Ground

Pin Usage Differences

The following pins differ in usage between the Motorola BCC and the Vesta Technology SBC332:

1. On connector P1, pins 25, 26, 27, and 29 are unconnected on the SBC332. On the BCC, they are used to provide the capability of programming the system EPROM in-place.
2. On connector P2, pins 21, 22, 23, and 57 are unconnected on the SBC332. On the BCC, they provide an interface via the platform board (PFB) to the BCCDI, a 68HC11-based single-board computer which also attaches to the PFB.

Other Differences between the Motorola BCC and the SBC332

Besides the connector differences mentioned elsewhere, the SBC332 uses a different configuration of chip select signals for accessing on-board RAM than is used by the BCC. The BCC controls all RAM read and write accesses using three chip-select lines: CS0*, CS1* and CS2*. The SBC332 uses the processor's R/W* signal for selecting read or write accesses to RAM, and therefore only required CS0* and CS1* for chip selection.

The specific configuration differences are as follows:

Signal	Board	Usage
CS0*	BCC SC332	Write access to the upper byte of a word. Read and write access to the upper byte of a word.
CS1*	BCC SBC332	Write access to the lower byte of a word. Read and write access to the lower byte of a word.
CS2*	BCC SBC332	Read access to both bytes of a word. Not used.

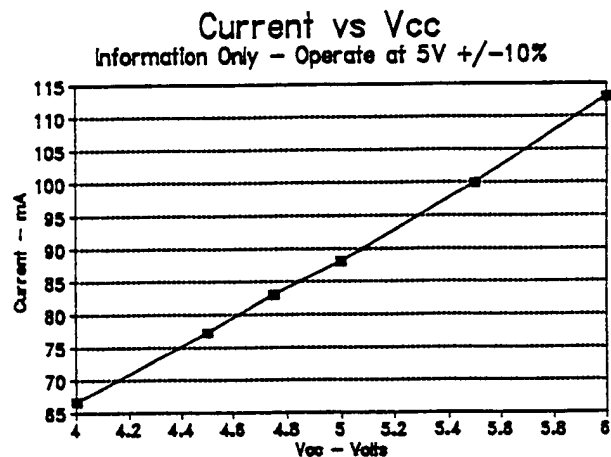
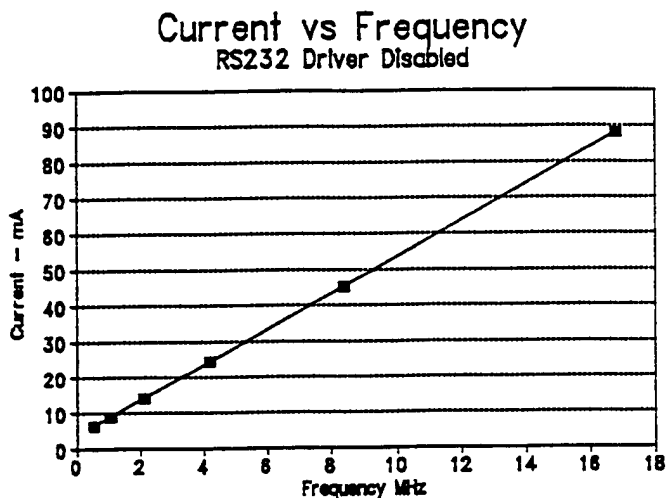
CHIP SELECT VARIANCE BCC ↔ SBC332

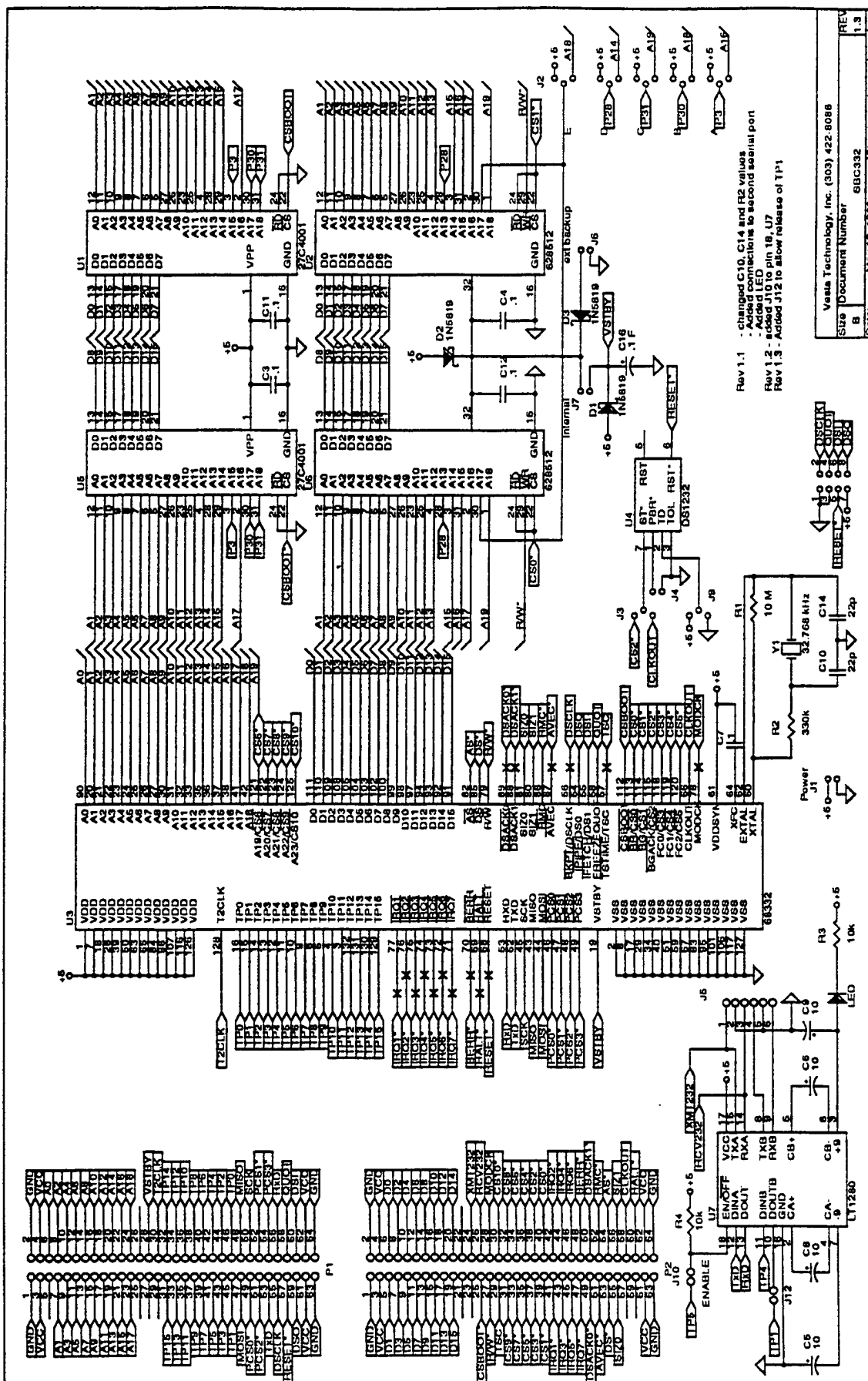
Power Consumption

The power requirement of the SBC332 is largely a function of the clock frequency. The graph titled **Current vs Frequency** shows this relationship at $V_{cc} = 5.00$ Volts. This data was obtained from a single unit of the latest revision of Motorola's MC68332. Earlier revisions of this microprocessor have evidenced up to 50% higher currents. The RS-232 driver was disabled during this test.

Entering low power stop mode decreases the current drain to less than 2 mA. Note that the external watchdog strobe will stop if the oscillator is stopped causing the system to be reset at the watchdog timeout period. If the watchdog input source is CLKOUT then the watchdog will not reset the board as long as the oscillator is running. During all modes of low power operation it is important that all inputs to P1 and P2 be terminated with pullup resistors. Unless this is done, up to 20 mA of leakage currents will be observed.

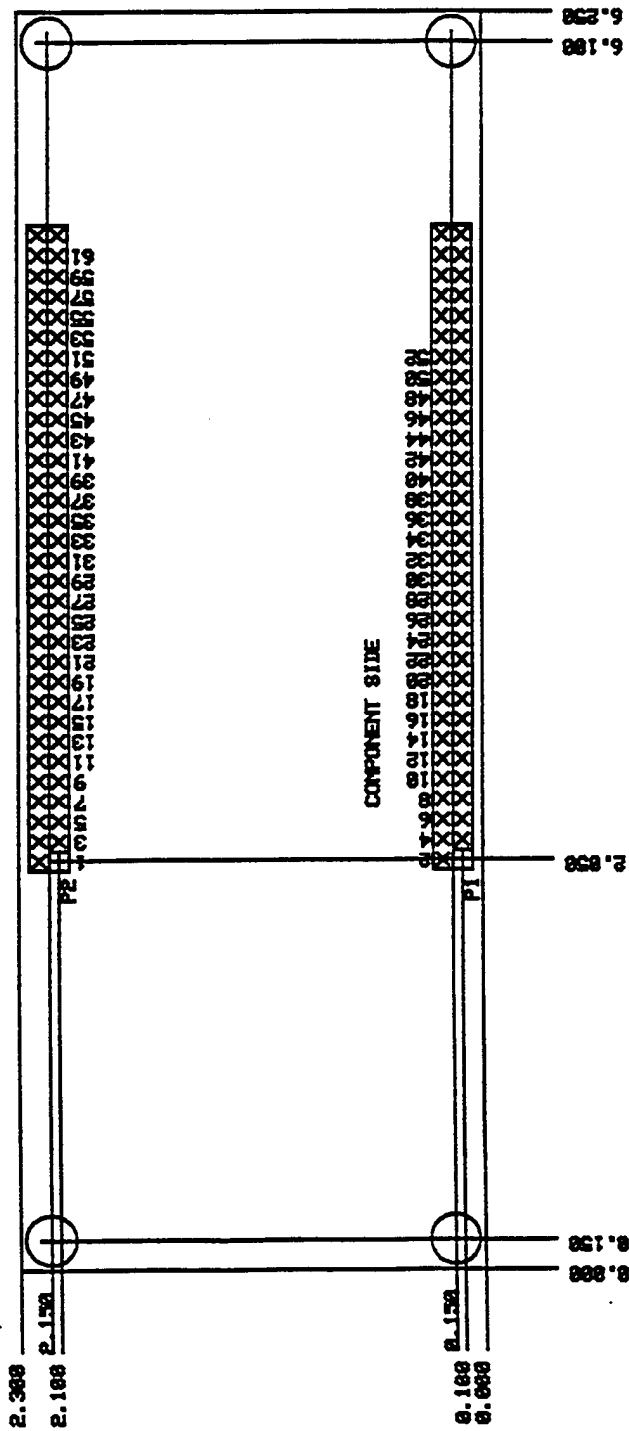
The power requirement is also a weak function of V_{cc} as shown in the graph titled **Current vs V_{cc}** . Please note that although the SBC332 appears to operate from 4 Volts to 6 Volts, the V_{cc} specification for all of the components is 4.75 Volts to 5.25 Volts.





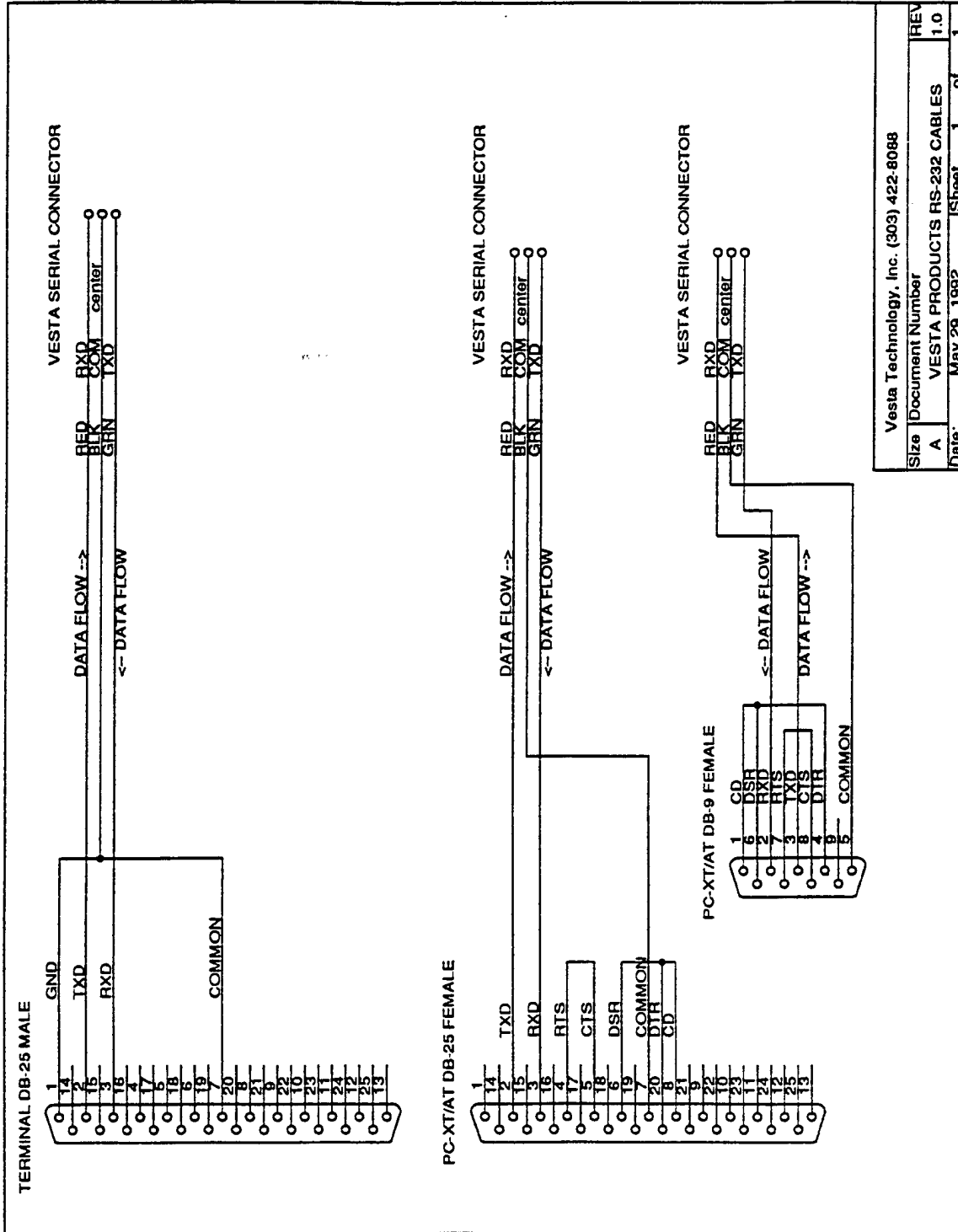
Rev 1.1 - changed C10, C14 and R2 values
 - Added connections to second serial port
 - Added LED
 Rev 1.2 - added J10 to pin 18, U7
 Rev 1.3 - Added J12 to allow release of TP1

REV	1.3
SIZE	8
Doc Number	SBC332
Date	Mar 12, 1993



Size and Mounting

RS-232 Cabling Diagram



Vesta Technology, Inc. (303) 422-8088

Size	Document Number	REV
A	VESTA PRODUCTS RS-232 CABLES	1.0
Date:	May 29, 1992	Sheet 1 of 1

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AD9955/PCB DDS Evaluation Board

AD9955/PCB

FEATURES

- IBM-Compatible PC for Test Control
- Standard Centronics Printer Cable
- SMB Connectors on Analog and Clock Inputs/Outputs
- Evaluates AD9713B and AD9721
- Test Software Included

GENERAL DESCRIPTION

The AD9955/PCB DDS Evaluation Board allows designers to evaluate the high performance AD97xx D/A Converters with a minimum amount of effort.

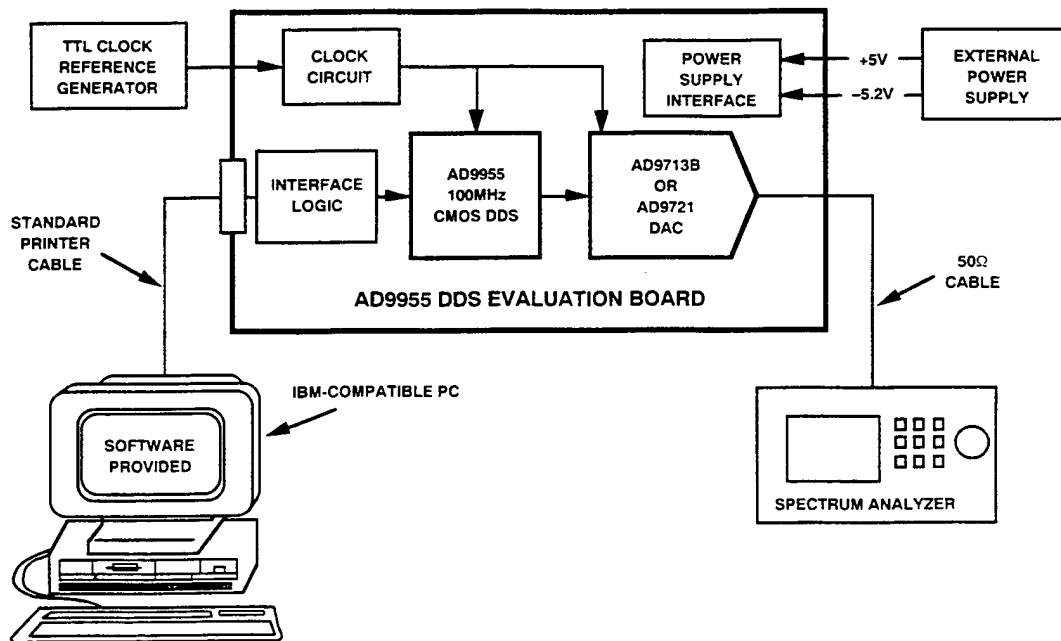
To prove these DACs will meet the user's waveform synthesis requirements, the only things needed are the AD9955/PCB DDS Evaluation Board, +5 V/-5.2 V power supplies, an IBM-compatible PC, a spectrum analyzer, and a TTL signal generator. The evaluation setup is shown below.

The DDS evaluation kit includes a populated, tested AD9955/PCB board; software which controls the tuning word for the input frequency through the parallel printer port; and one sample each of the AD9713B and AD9721 DACs.

The AD9713B and AD9721 are TTL-compatible DACs designed specifically for DDS, waveform reconstruction, and high resolution imaging applications. The AD9713B is a 12-bit, 80 MSPS device; the AD9721 is a 10-bit, 100 MSPS DAC. Both units feature low glitch and outstanding dynamic performance.

Testing of the DACs can be done by alternately installing them in sockets on the board; a model AD9955 Direct Digital Synthesizer is soldered in place.

The AD9955 is a CMOS 100 MHz device for frequency synthesis applications. It comprises a 32-bit phase accumulator and a 15-bit phase-to-12-bit-sine amplitude converter. Its control logic is CMOS compatible, and the clock input is TTL. CMOS outputs are latched on board and a data ready signal is available.



AD9955 DDS Evaluation Board Setup

REV. 0

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Telex: 924491 Cable: ANALOG NORWOODMASS

AD9955/PCB — SPECIFICATIONS

Typical Electrical Characteristics (Nominal power supplies; AD9721 installed; CLK = 80 MHz)

Characteristic	Typical Value	Units
-5.2 VD (Digital) Supply Current (TP1)	270	mA
-5.2 VA (Analog) Supply Current (TP2)	30	mA
-5.0 V Supply Current (TP3)	250	mA
AD9713B Output Voltage (J3 or J4, Terminated into 50 Ω Externally)	0 to -0.5	V
AD9721 Output Voltage (J5 or J6, Terminated into 50 Ω Externally)	0 to -0.5	V
TTL clock input HIGH (J2)	2.4 to 5	V
TTL clock input LOW (J2)	0.0 to 0.5	V

Using the AD9955/PCB DDS Evaluation Board

The AD9955/PCB evaluation kit is a test system designed to simplify the evaluation of the AD9713B 12-bit, 80 MSPS TTL DAC or the AD9721 10-bit, 100 MSPS TTL DAC when either is driven by the AD9955 100 MHz Direct Digital Synthesizer. Provisions to control the AD9955 from the printer port of an IBM-compatible PC are included, along with the necessary software. This data sheet provides information on operating the evaluation board; additional details are available from ADI/CLG Applications Engineering: (919) 668-9511.

Choosing a DAC

A sample of each DAC (AD9713BBN and AD9721BN, both are PDIPs) is included with the AD9955/PCB. One or the other is installed in the evaluation board by the user. The analog outputs of the DACs are available through SMB connectors (J3-J6). Cables and adapters for these connectors are available from Pasternack Enterprises [(714) 261-1920].

It is suggested that both DAC designs be evaluated to determine which converter will provide optimum performance (highest Spurious Free Dynamic Range) in the final application. The AD9713B fits into the pin sockets of U9, while the AD9721 fits into the pin sockets of U10. The DACs can be installed only one at a time since they share area in the layout.

Warning: Since both DACs are in 28-pin PDIPs, users should take care not to install the DAC in the wrong socket. Installation of either DAC in the wrong socket can result in device failure. Power should be off when installing the devices.

In general, the AD9713B will provide the best performance in applications which use update rates below 20 MSPS and analog output frequencies below 5 MHz. These applications tend to be limited by the linearity of the converter and will benefit from the 12-bit resolution of the AD9713B. Applications which use faster clock rates or generate analog outputs higher than 5 MHz will benefit from the ultralow switching transients of the AD9721.

Prototyping Area

An area near one edge of the board (marked "PROTO AREA") is intentionally left void of components to allow the user to add additional circuits to the evaluation test set. The wide strip on both sides of the PWB is connected to the internal ground plane, and the through holes are electrically isolated. J7 and J8 are provided to add additional SMA or SMB connectors for analog signals. Users may want to build custom analog filters for the DAC outputs, or add buffers and operational amplifiers used in the final applications.

XO vs. External Clock

The reference clock of the AD9955/PCB is normally provided by an external TTL signal applied to connector J2. This SMB connector is terminated into 50 Ω by R13. If desired, R13 can be removed and a standard TTL crystal oscillator can be installed in DIP socket Y1 to improve performance and/or simplify the evaluation process.

The reference clock is hardwired to the AD9955. Strap options installed during assembly also connect the reference clock directly to the clock inputs of the DACs (see E2-E4 below). The user may opt to remove these straps and clock the DACs with the data ready signal (DRDY) of the AD9955 (E1), or provide an external TTL compatible signal.

Power Supplies

Power for the AD9955/PCB must be provided externally through the pin connections TP1-TP4, as described in the Inputs/Outputs. It is suggested that the user solder leads to these pins and connect them to a low impedance, low noise, linear power supply. Two isolated holes of 0.15" diameter are located between the test points and the edge of the board; these can be used for wire wraps to provide stress relief for the power leads.

Current levels through the supplies are shown in the specification table. Although analog and digital -5.2 V power supplies are separated (this provides best performance), the user may opt to connect the two supplies during evaluation.

Controlling the AD9955/PCB

The AD9955/PCB is designed to allow control (frequency specification, reset, etc.) through the parallel printer port of a standard IBM-compatible PC. The user simply disconnects the printer cable from the printer and inserts it into edge connector J1 of the evaluation board.

The printer port provides information to the AD9955/PCB through eight data lines and two control lines. Data is latched into registers on the AD9955/PCB (U1-U7) and transferred to the AD9955.

A 5.25" floppy disk containing software to control the AD9955 is provided with the AD9955/PCB. This software was developed using Quick Basic from Microsoft, Inc. The original Quick Basic source code is provided in a file named A:\AD9955.BAS, which the user may view, run, or modify with the Quick Basic Software (not provided, available from Microsoft).

An executable version of this software is also provided, and can be executed from DOS by typing "a:\ad9955." The software prompts the user to provide the necessary information needed by the program. Additional information is included in a text file named a:\readme.doc.

AD9955/PCB BILL OF MATERIAL

Quantity	Description	Circuit Designation
6	Terminals	TP1-TP6
60	Pin Sockets (U9, U10, Y1)	NA
5	SMB PC Mount Connectors	J2-J6
1	36-Pin PC-Mount Connector	J1
28	0.1 μ F Chip Capacitors (Size 0805)	C1, C3-C6, C10-C11, C13-C22, C24-C27, C30-C32, C50-C53
3	10 μ F Capacitors	C23, C29, C33
12	130 Ω Chip Resistors	R1-R12
5	49.9 Ω Chip Resistors	R13, R18, R19, R21, R22
1	20 Ω Chip Resistor	R16
1	2 k Ω Chip Resistor	R14
1	7.5 k Ω Chip Resistor	R17
7	ALS 574 Octal Flip-Flops (SOIC)	U1-U7
1	AD9955KS Direct Digital Synthesizer	U8
1	AD9713BBN	U9
1	AD9721BN D/A Converter	U10

ORDERING GUIDE

Catalog Number	Description
AD9955/PCB	AD9955/PCB DDS Evaluation Kit, Assembled and Tested
AD9955/PWB	AD9955/PWB DDS Evaluation Board, PWB Only

Inputs/Outputs

Name	Description
J1	36-pin edge connector designed to mate with parallel printer port of IBM-compatible PC. Software provided with the AD9955/PCB allows the user to load data from a PC into the AD9955.
J2	SMB connector for external TTL input; R13 provides 50 Ω termination.
J3	SMB connection to the analog output of the AD9713B (U9, I _{OUT} , Pin 14).
J4	SMB connection to the complementary analog output of the AD9713B (U9, I _{OUT} , Pin 16).
J5	SMB connection to the analog output of the AD9721 (U10, I _{OUT} , Pin 20).
J6	SMB connection to the complementary analog output of the AD9721 (U10, I _{OUT} , Pin 21).
J7/J8	Optional locations for SMB connectors near prototyping area (connectors not included).
TP1	Pin connection for external -5.2 V digital power supply; nominally 270 mA.
TP2	Pin connection for external -5.2 V analog power supply; nominally 30 mA.
TP3	Pin connection for external +5 V power supply; nominally 250 mA with 80 MHz clock.
TP4	Pin connection for external ground reference.
TP5	Pin connection to monitor carry out (C _{OUT}) signal of AD9955 (Pin 61).
TP6	Optional pin connection for external -5.2 V analog power supply. Can be used to connect -5.2 V analog supply near DACs; not necessary to drive this pin under normal conditions.
E1	Optional through hole connection to data ready (DRDY) signal of the AD9955 (Pin 62).
E2	Through hole connection to the LATCH ENABLE (Pin 26) of the AD9713B; normally connected to E4 with external strap.
E3	Through hole connection to the CLOCK (Pin 11) of the AD9721; normally connected to E4 with external strap.
E4	Through hole connection to the master clock of the AD9955/PCB DDS Evaluation Board. Master clock may be provided by a user-installed TTL crystal oscillator (Y1) or an external TTL signal applied to J2.

AD9955/PCB

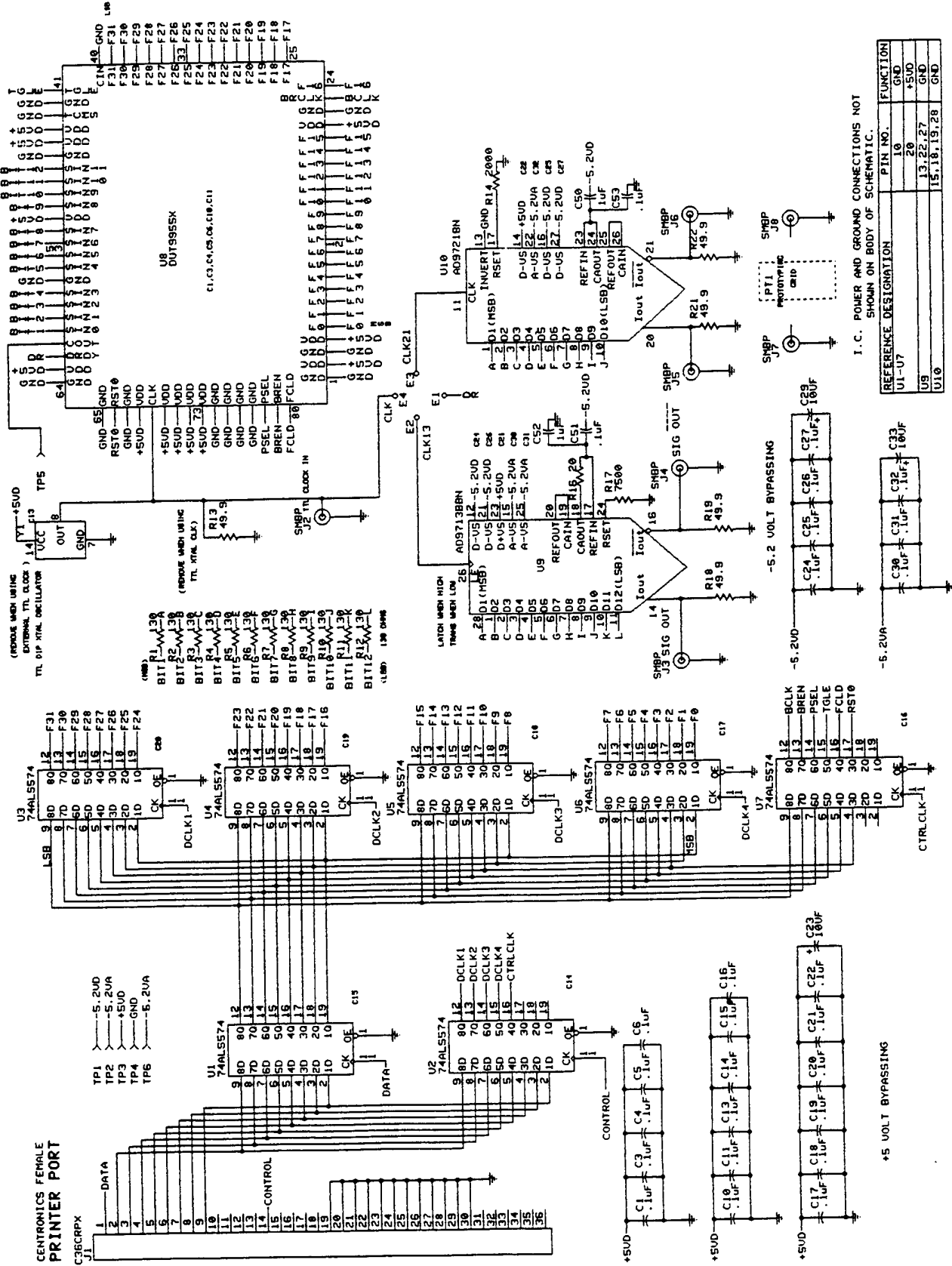
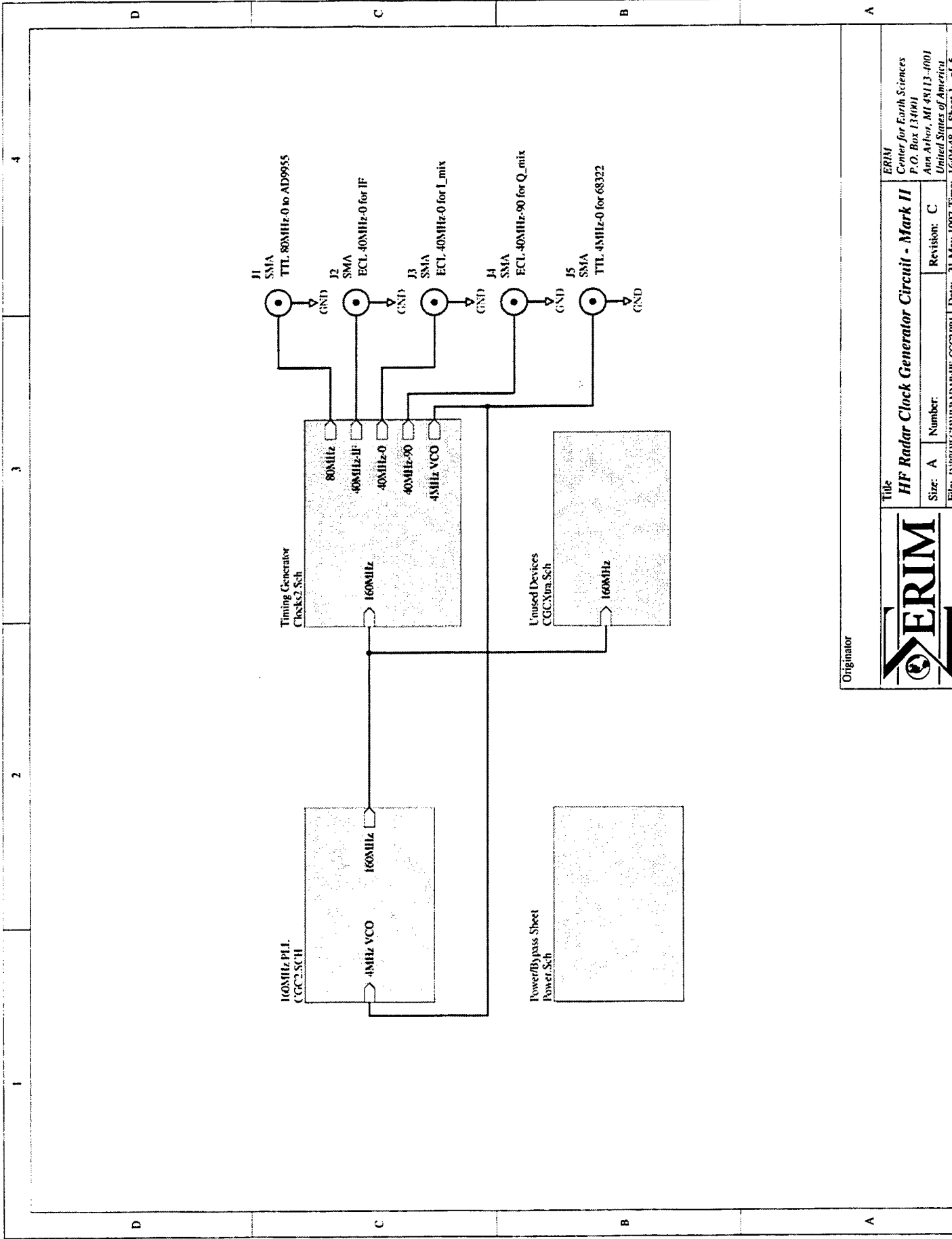


Figure 1.

I.C. POWER AND GROUND CONNECTIONS NOT SHOWN ON BODY OF SCHEMATIC.

REFERENCE DESIGNATION	FUNCTION
U1-U7	GND
U9	+5V
U10	GND
	15,18,19,28
	GND

**SYSTEM
DOCUMENTATION
(ERIM)**

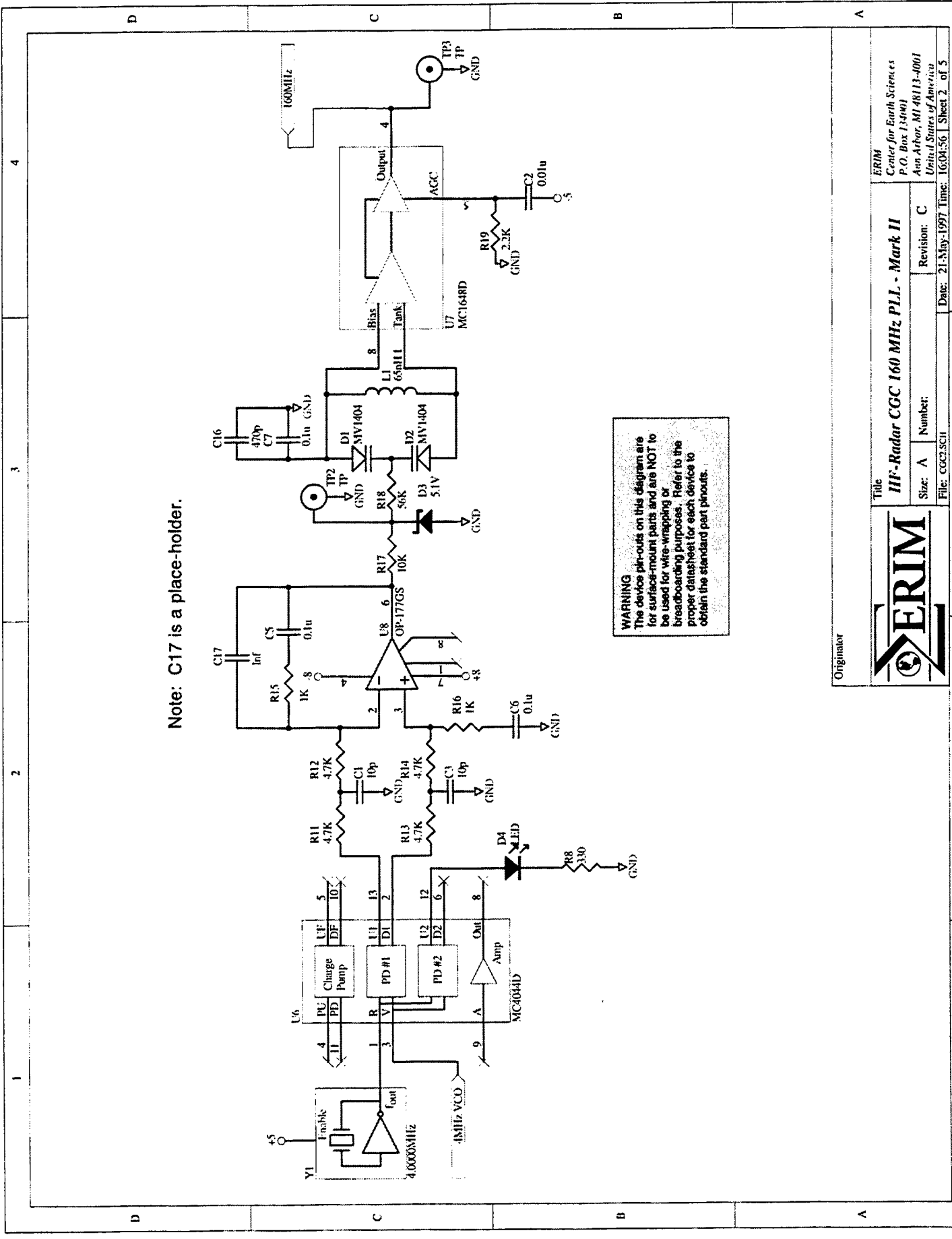


Originator



Title
HF Radar Clock Generator Circuit - Mark II
 Size: A Number: C
 File: D:\PROJECTS\SHIRKADAR\HF_CGC2.PRI Date: 21-May-1997 Time: 16:04:48 Sheet 1 of 5

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 16:04:48 Sheet 1 of 5



Note: C17 is a place-holder.

WARNING
 The device pin-outs on this diagram are for surface-mount parts and are NOT to be used for wire-wrapping or breadboarding purposes. Refer to the proper data sheet for each device to obtain the standard part pinouts.

Originator

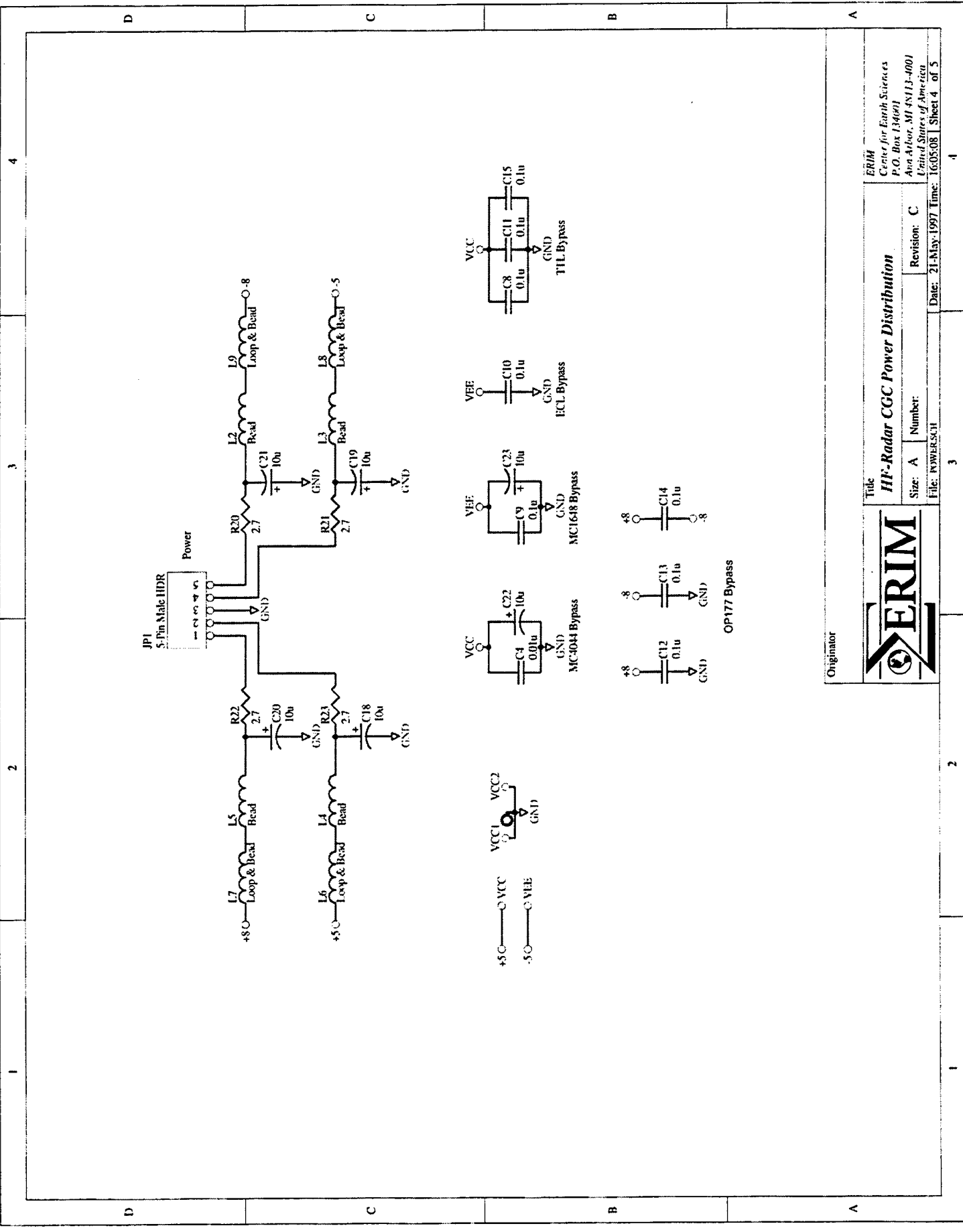
ERIM

Title: **HF-Radar CGC 160 MHz PLL - Mark II**

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 Ann Arbor, MI 48113-0001
 United States of America

Size: A Number: Revision: C

File: CGC2.SCH Date: 21-May-1997 Time: 16:04:56 Sheet 2 of 5



Originator



Title
HP-Radar CCG Power Distribution
 Size: A Number: Revision: C
 File: POWERSCHEM Date: 21-May-1997 Time: 16:05:08 Sheet 4 of 5

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4

3

2

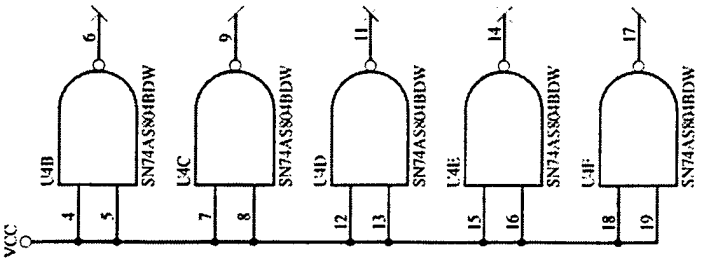
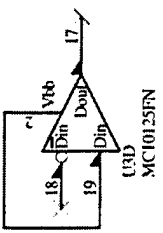
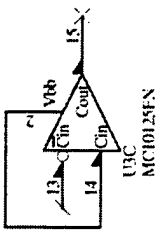
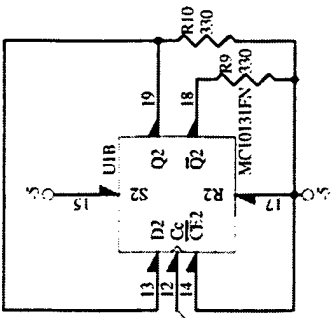
1

1

3

2

1



WARNING
 The device pin-outs on this diagram are for surface-mount parts and are NOT to be used for wire-wrapping or breadboarding purposes. Refer to the proper datasheet for each device to obtain the standard part pinouts.

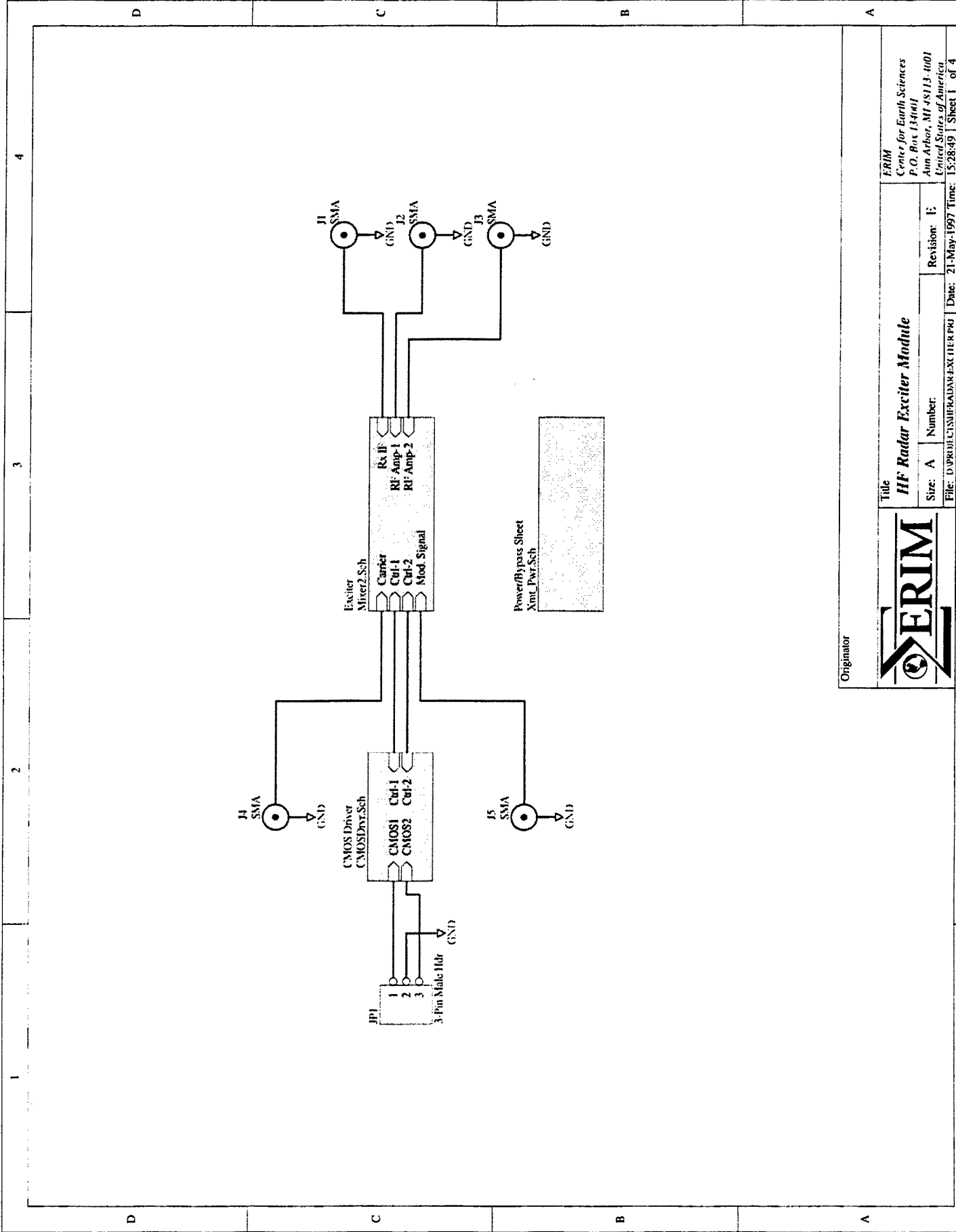
Originator



Title: **HF-Radar CGC Unused Devices**

Size: A Number: Revision: C
 File: CGCXBASCH Date: 21-May-1997 Time: 16:08:30 Sheet 5 of 5

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Originator



Title
HF Radar Exciter Module

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P.O. Box 134601
Ann Arbor, MI 48113-1001
United States of America

Size: A Number: Revision: E;

FILE: D:\PROJECTS\HFRA\RADAR\EXCITER\PRJ Date: 21-May-1997 Time: 15:28:49 Sheet 1 of 4

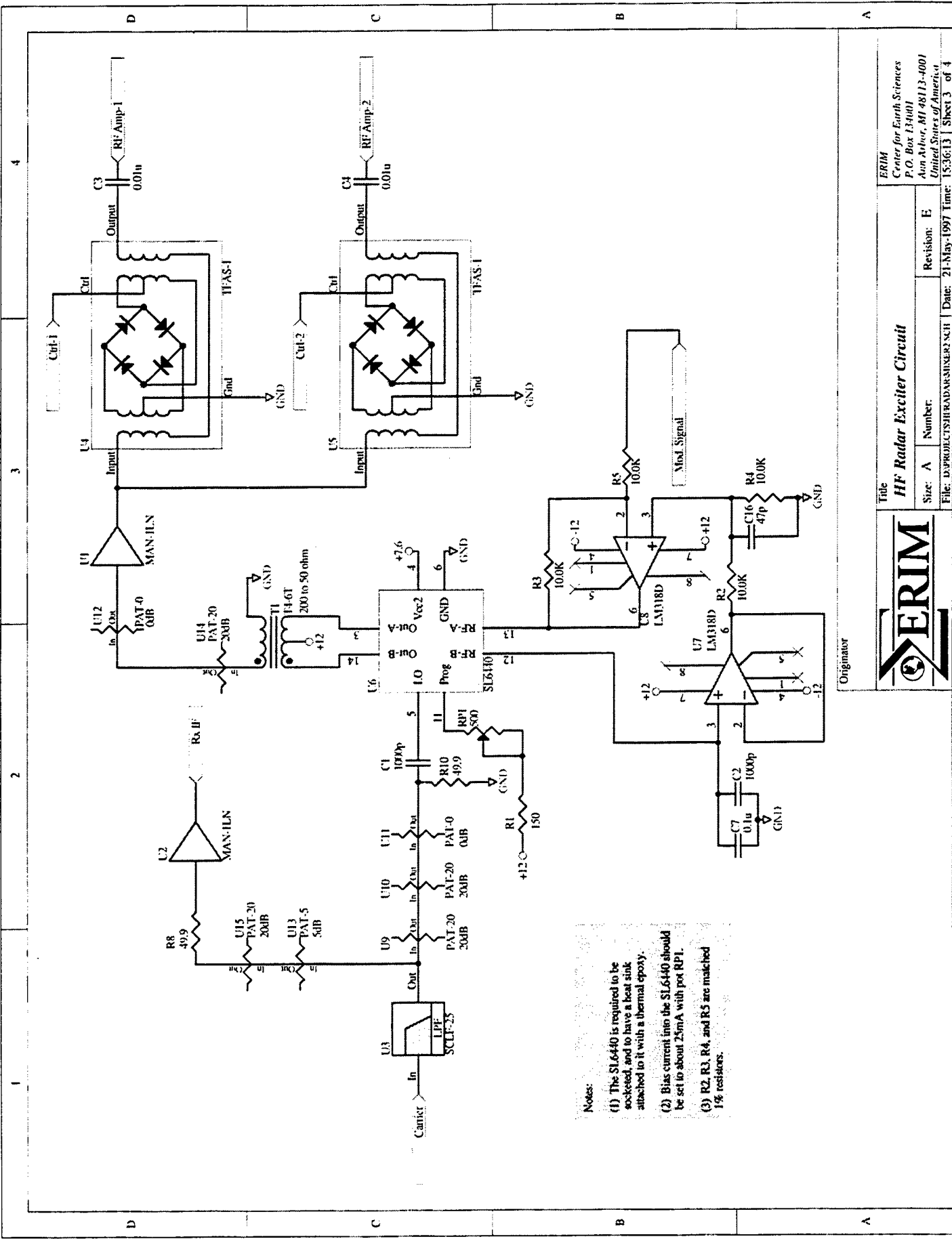


Originator



Title: **HF-Radar Exciter TFAS Ctrl Driver**
 Size: A Number: Revision: E
 File: D:\PROJECTS\RADAR\CHEMURVR\SCH Date: 21-May-1997 Time: 15:29:03 Sheet 2 of 4

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- Notes:
- (1) The SL6440 is required to be socketed, and to have a heat sink attached to it with a thermal epoxy.
 - (2) Bias current into the SL6440 should be set to about 25mA with pot R1.
 - (3) R2, R3, R4, and R5 are matched 1% resistors.

Originator



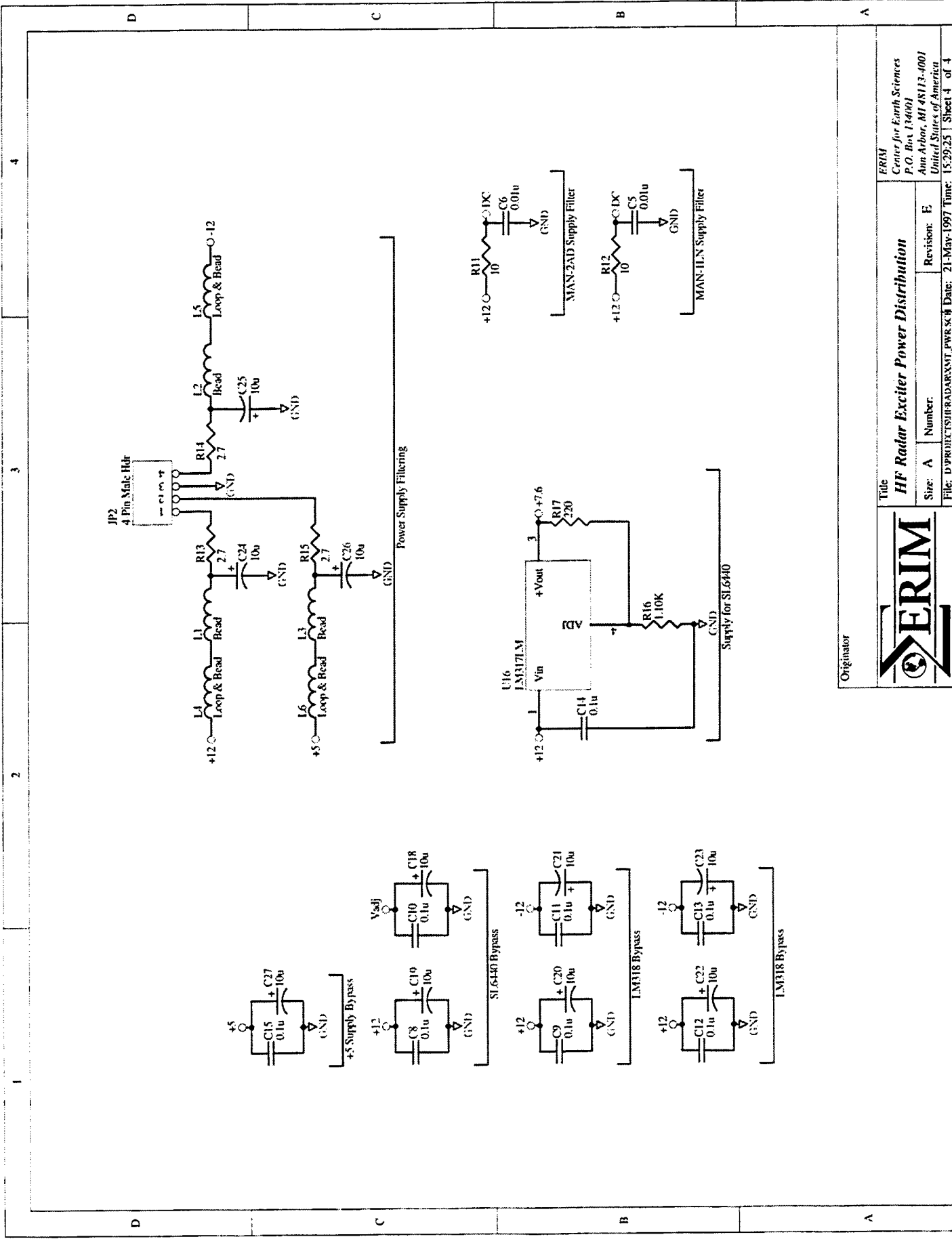
Title
HF Radar Exciter Circuit

Size: A Number: E

Revision: E

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United States of America

Date: 21-May-1997 Time: 15:36:13 Sheet 3 of 4



Originator



Title

HF Radar Exciter Power Distribution

Size: A

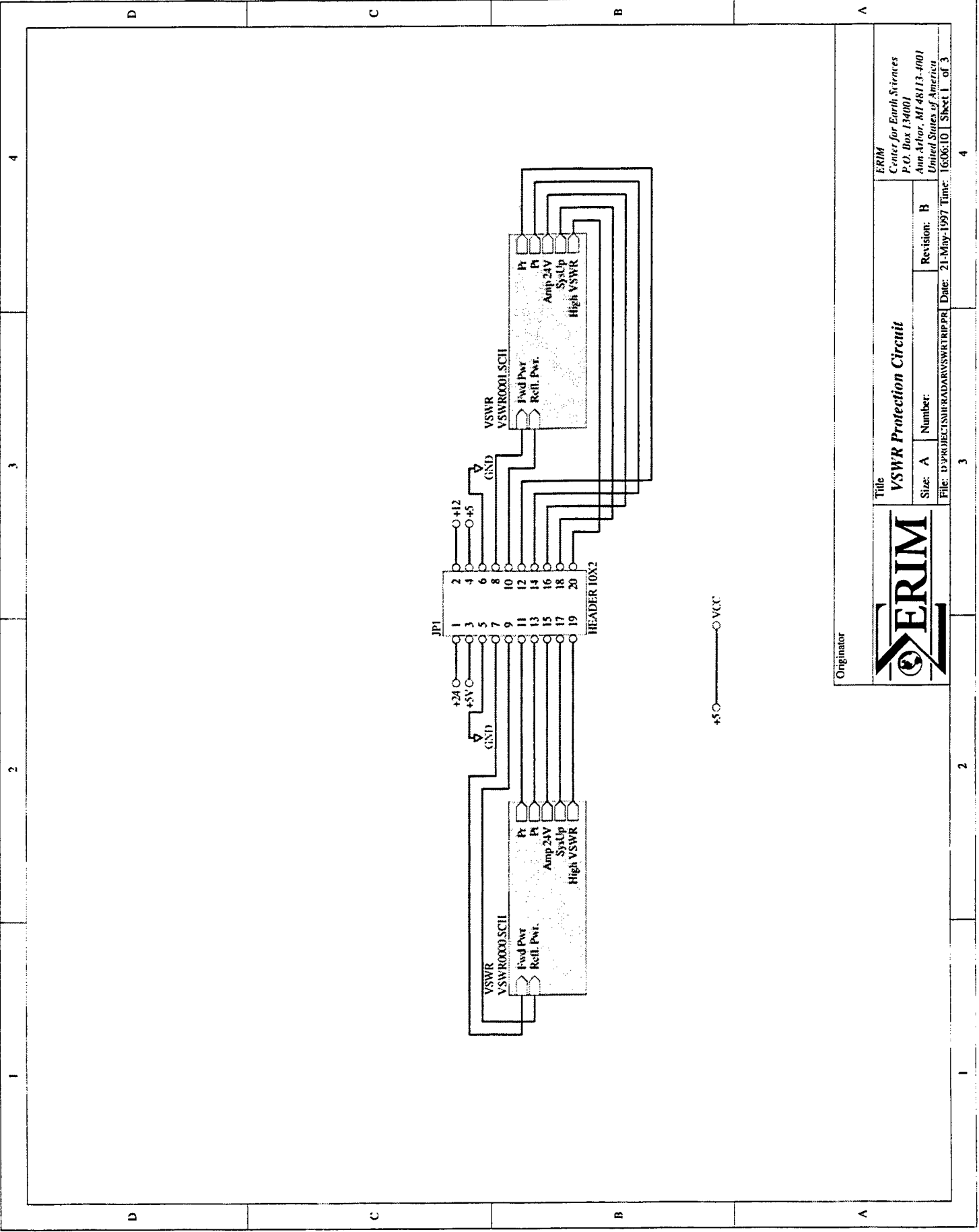
Number:

Revision: E

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File: D:\PROJECTS\HF-RADAR\XMT_PWK\KSP Date: 21-May-1997 Time: 15:29:25 Sheet 4 of 4



Originator



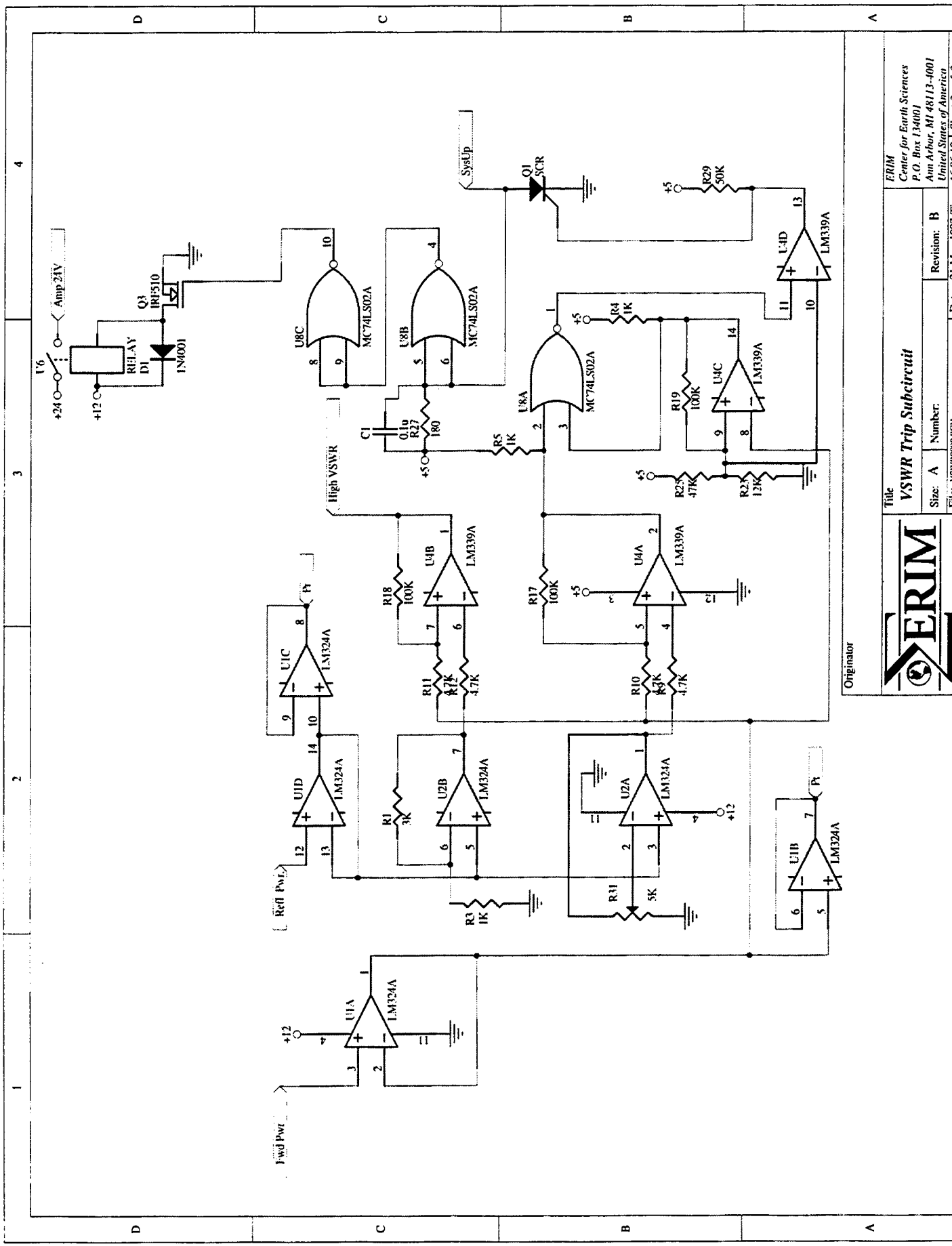
Title
VSWR Protection Circuit

Size: A Number: B

Revision: B

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P.O. Box 134001
Ann Arbor, MI 48113-4001
United States of America

File: D:\PROJECTS\RADAR\VSWR\TRIPPR Date: 21-May-1997 Time: 16:06:10 Sheet 1 of 3



Originator



Title
VSWR Trip Subcircuit

Size: A Number:
 Revision: B
 File: VSWR000.SCH

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 United States of America

Date: 21-May-1997 Time: 10:06:19 Sheet 2 of 3

4

3

2

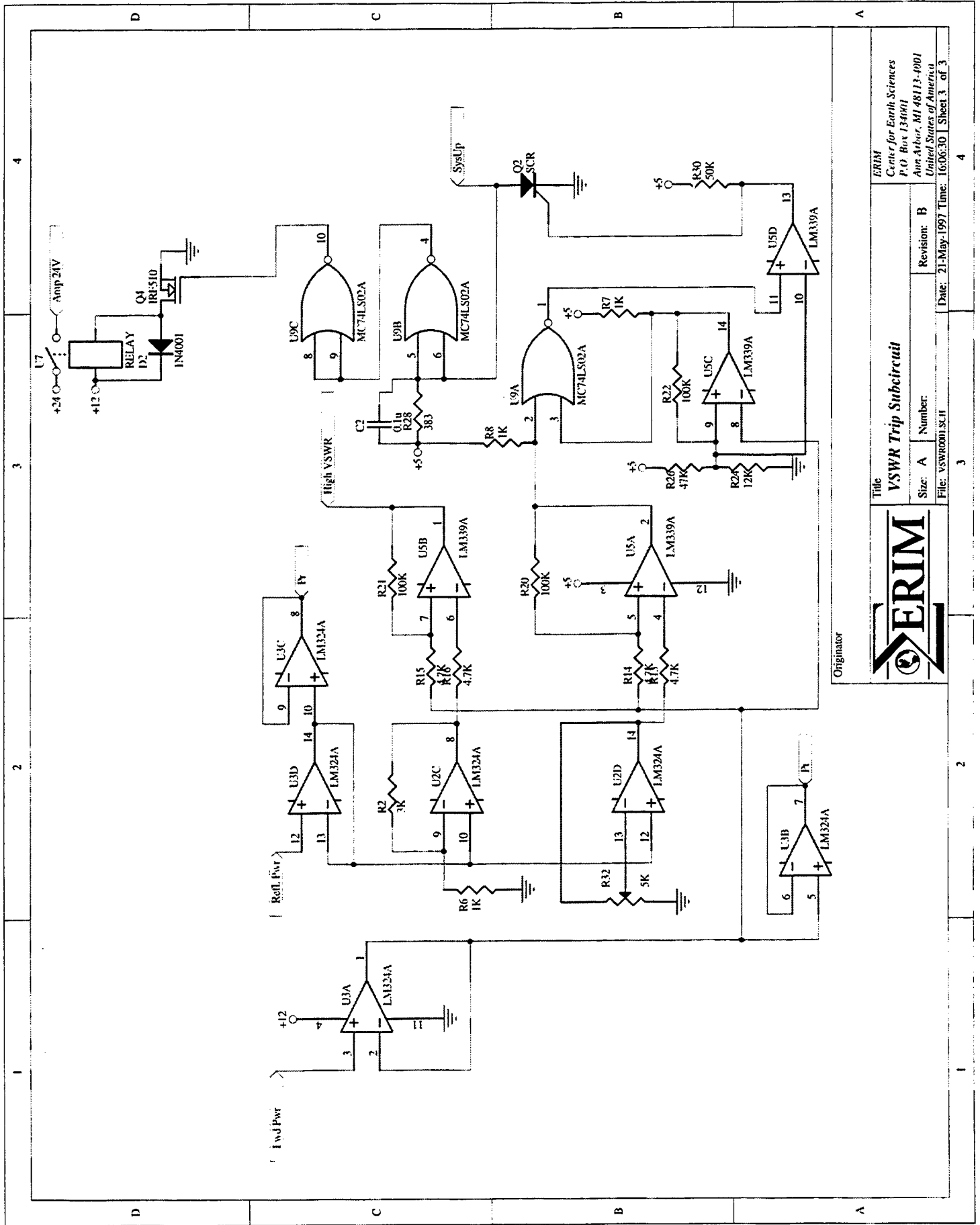
1

4

3

2

1



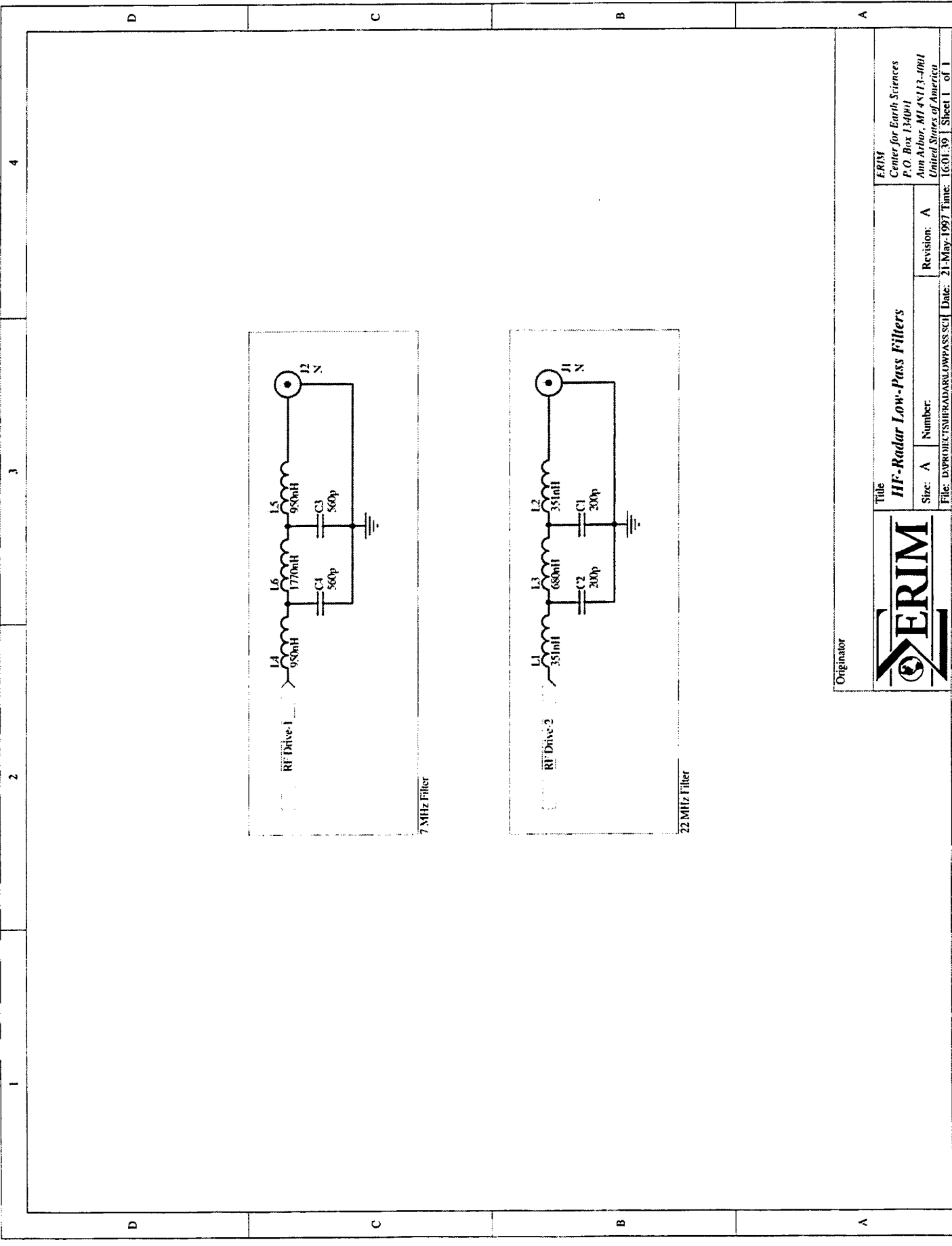
Originator



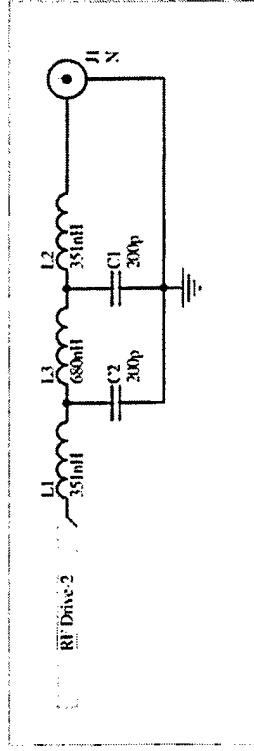
Title: VSWR Trip Subcircuit

Size: A Number: B
 File: VSWR001.SCH Date: 21-May-1997 Time: 16:06:30 Sheet 3 of 3

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 Ann Arbor, MI 48113-4001
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7 MHz Filter



22 MHz Filter

Originator



Title
HF-Radar Low-Pass Filters

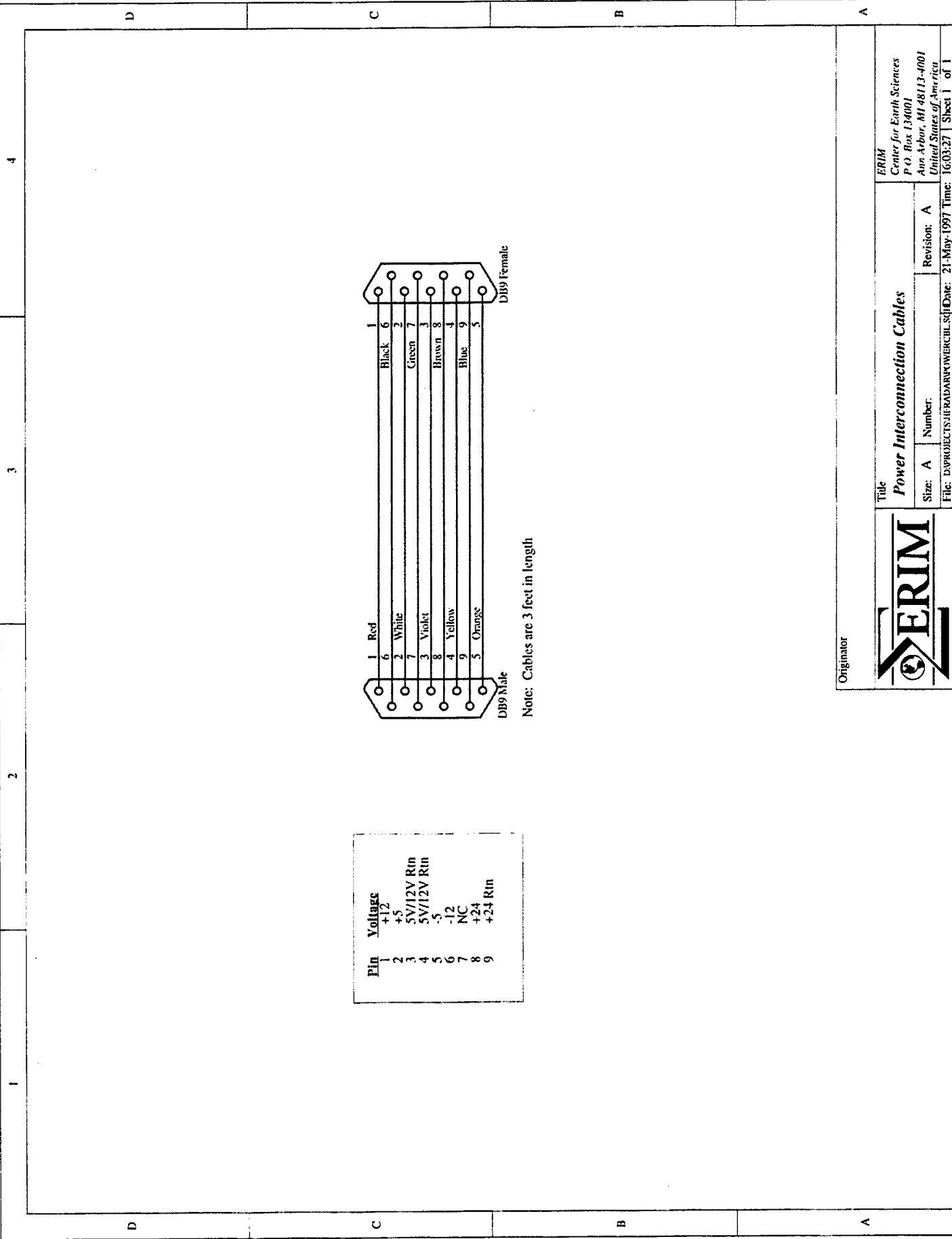
Spec: A

Number: A

Date: 21-May-1997 Time: 16:01:39

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Center for Earth Sciences
P.O. Box 134041
Ann Arbor, MI 48113-0041
United States of America

Sheet 1 of 1



Originator

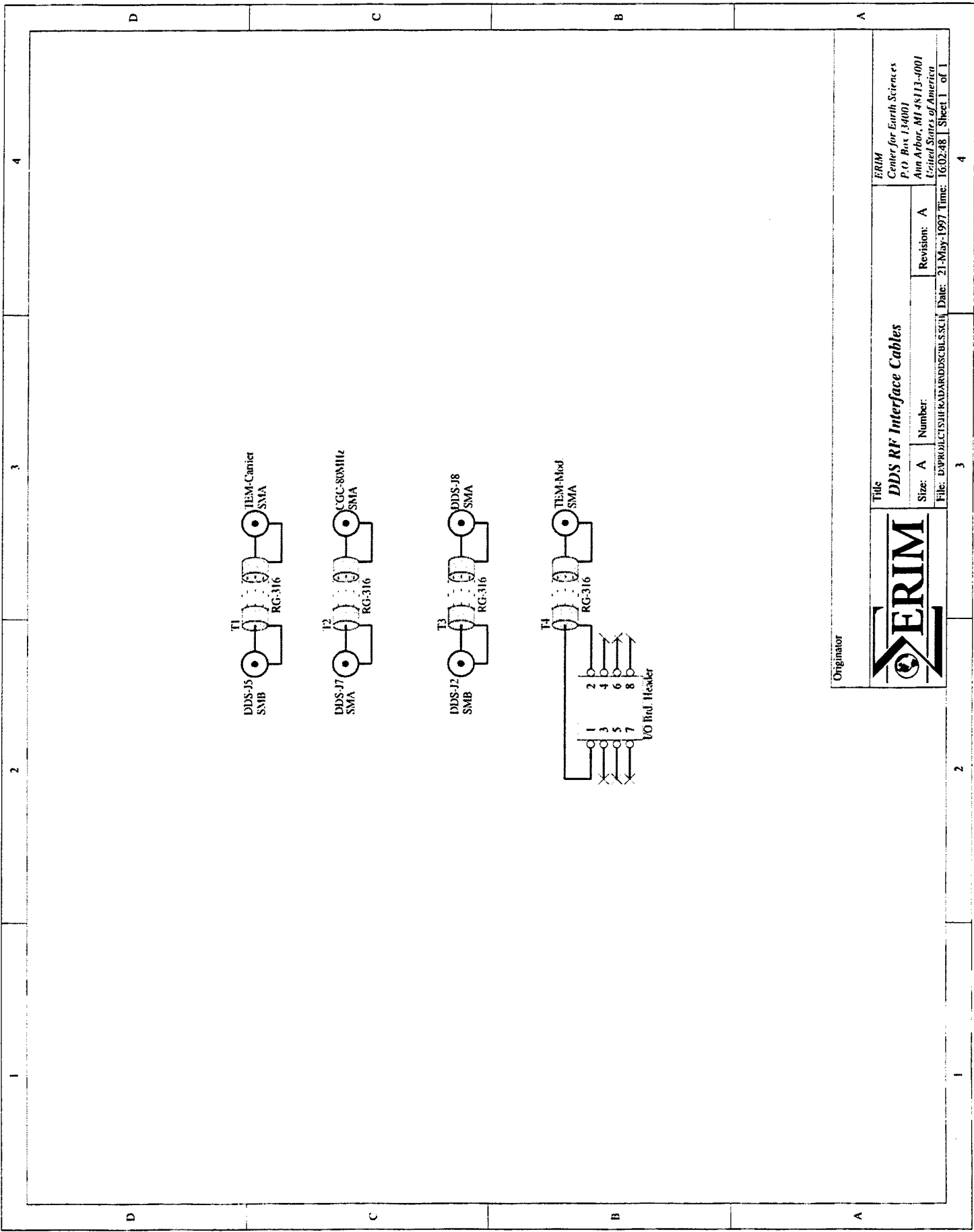


Title
Power Interconnection Cables

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Ann Arbor, MI 48113-4001
United States of America

Size: A Number: Revision: A

File: D:\PROJECTS\ERADAR\POWER\CABLE.SCP Date: 21-May-1997 Time: 16:03:27 Sheet 1 of 1



Originator



Title
DDS RF Interface Cables

Size: A Number: Revision: A
 Title: D:\PROJECTS\H\KADAR\DDS\BLS\SCU Date: 21-May-1997 Time: 16:02:48 Sheet 1 of 1

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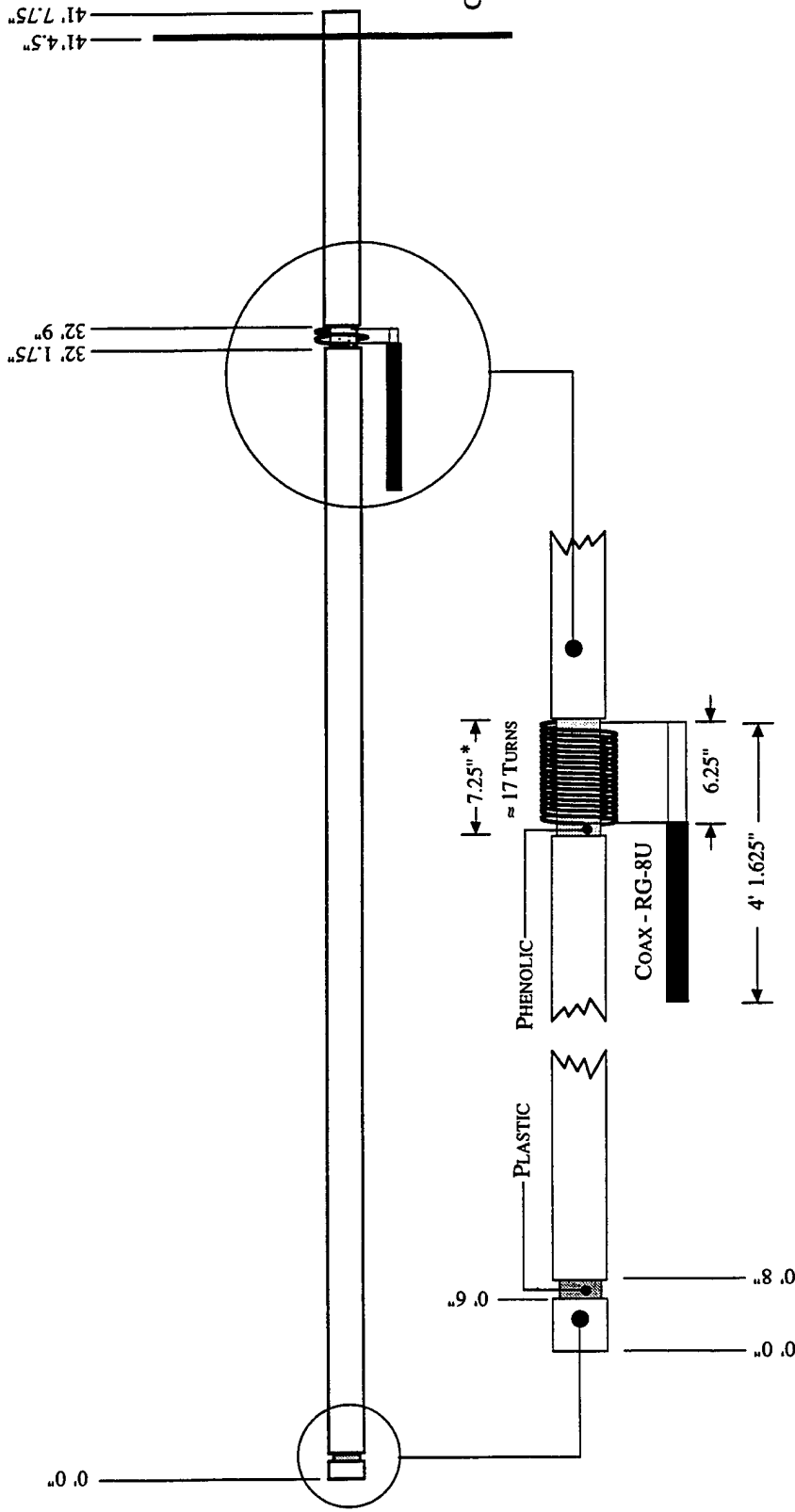
Vertical Monopole Antenna Assembly

Low Band Antenna (4.80 & 6.78 MHz)

- 1- Assembles using stainless steel clamps and inserts.
- 2- See diagram for length set points.
- 3- Trap inserts with RG-8 cable pointed toward ground
- 4- Trap conducting lines fit under cable clamps to make conduction.
- 5- Cable guide with three point mounting is included. The mount is placed immediately below the trap (See photo)
- 6- Capacitance hat fits at the top of the very top of antenna. The Capacitance hat is formed from two rod assemblies which are mounted orthogonally from each other.
- 7- Sixteen gauge wire is provided for the radials. Four $\frac{1}{4}$ wavelength radials are used for each band. Radials are placed every 90 degrees about the ground plate. Two sets of radials is accommodated on the ground plate. Radials connect to the ground plate using 10-32 screws. The ends of the radials are positioned using spikes (not provided - pick up on-site).
- 8- Radial lengths are 51 feet 3.2 inches, and 36 feet and 2.25 inches.

High Band Antenna (13.38 & 21.77 MHz)

- 1- Assembles using stainless steel clamps and inserts.
- 2- See diagram for length set points.
- 3- Trap inserts with RG-8 cable pointed toward sky
- 4- Trap conducting lines fit under cable clamps to make conduction.
- 5- Cable guide with three point mounting is included. The mount is placed immediately below the trap (See photo)
- 6- Sixteen gauge wire is provided for the radials. Four $\frac{1}{4}$ wavelength radials are used for each band. Radials are placed every 90 degrees about the ground plate. Two sets of radials is accommodated on the ground plate. Radials connect to the ground plate using 10-32 screws. The ends of the radials are positioned using spikes (not provided - pick up on-site).
- 7- Radial lengths are 18 feet 1.125 inches, and 11 feet and 3.45 inches.

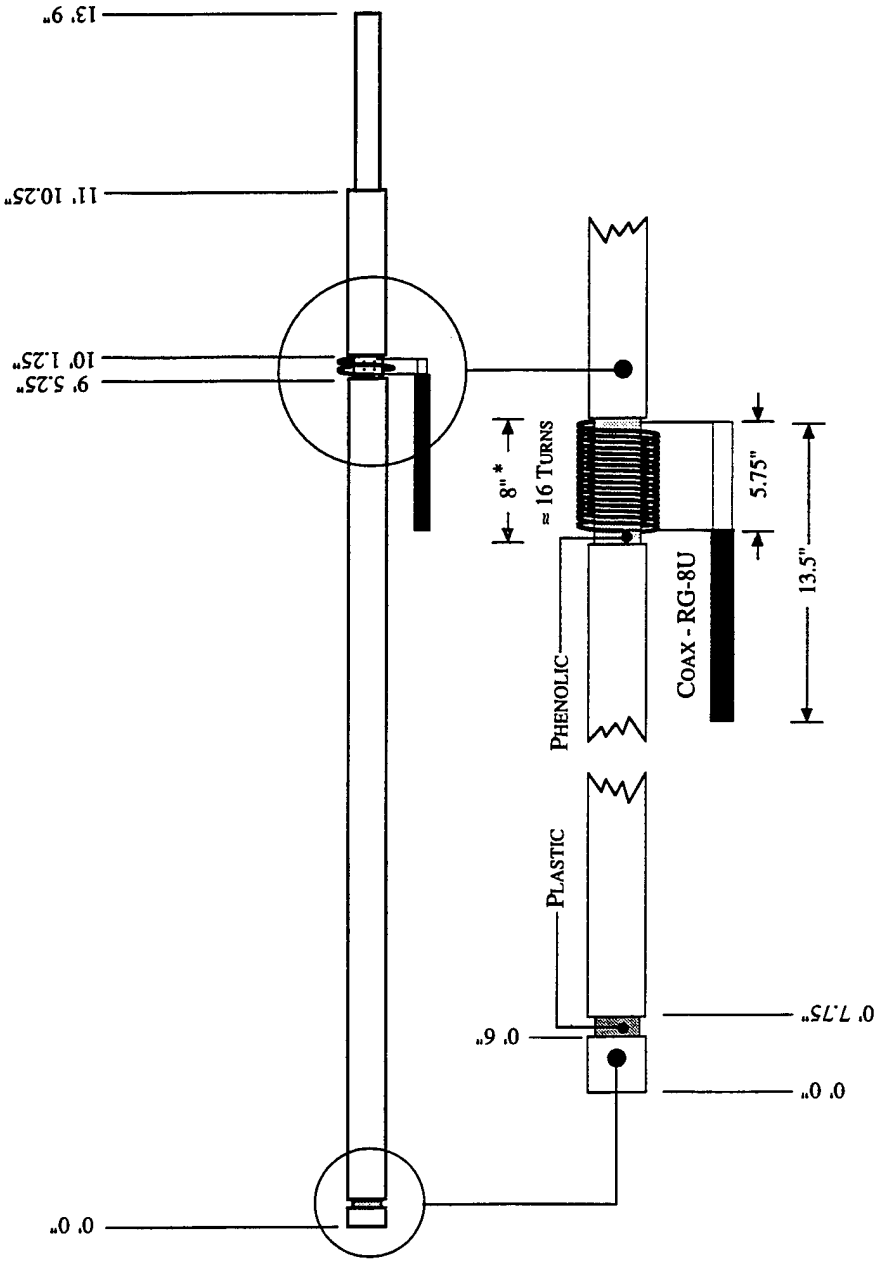


LOW BAND ANTENNA (4.80 & 6.78 MHz)

NOTES:

1. All sections of the antenna are aluminum except where noted.
2. All measurements were taken directly from the SNI antenna as deployed at Santa Cruz 1/24/97 except where noted by an asterisk (*).
3. Heights of objects in drawing have been exaggerated to enhance legibility.

Space Physics Research Laboratory College of Engineering University of Michigan		Ant Dimensions		Antenna Dimensions	
NO. 000149510249	REV. 0001	DATE 06-21-97	BY JGG/ENG	3 of 4	062-0085
DRAWN			RELEASE		
05-21-97 NS			05-21-97 NS		



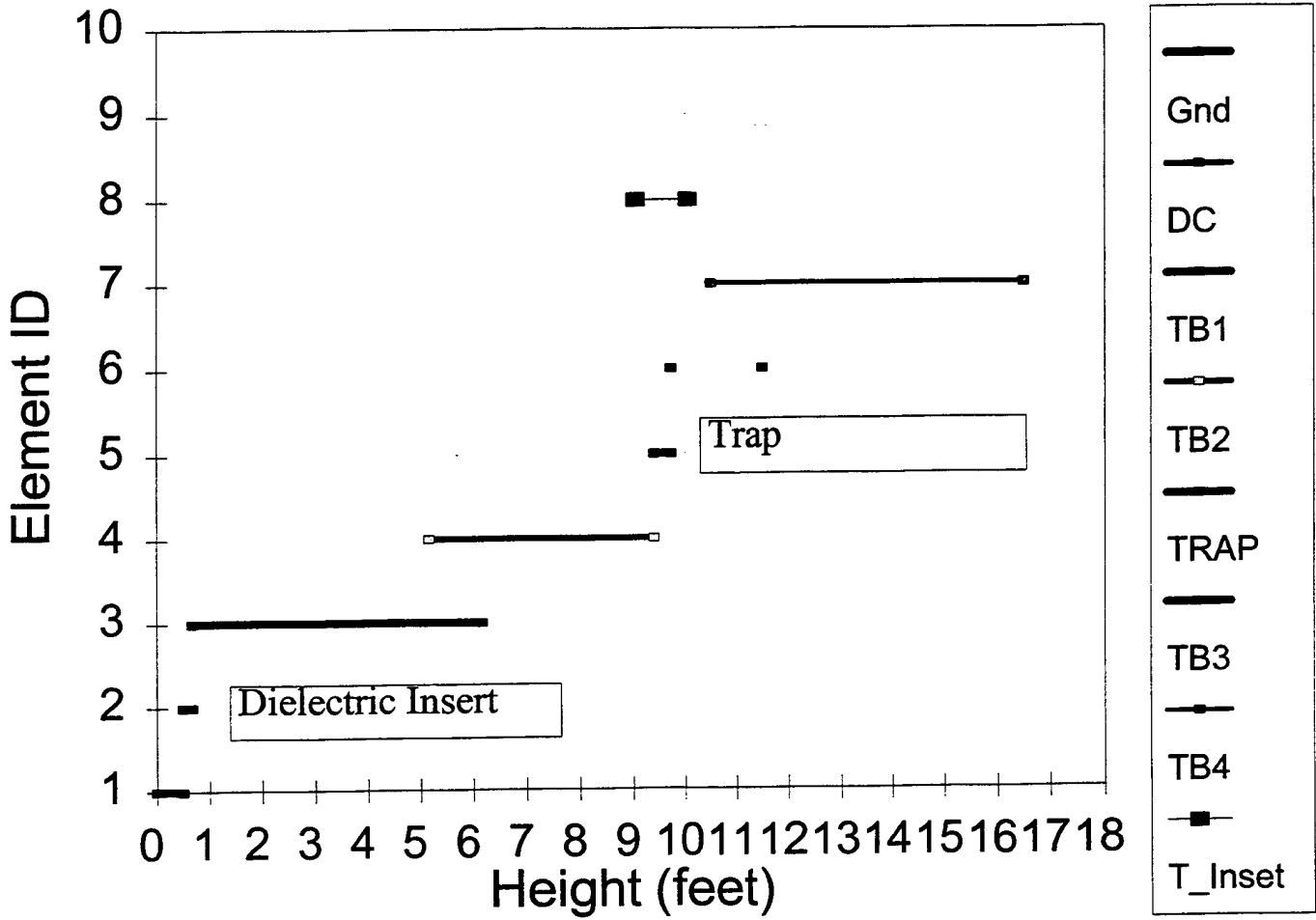
HIGH BAND ANTENNA (13.38 & 21.77 MHz)

NOTES:

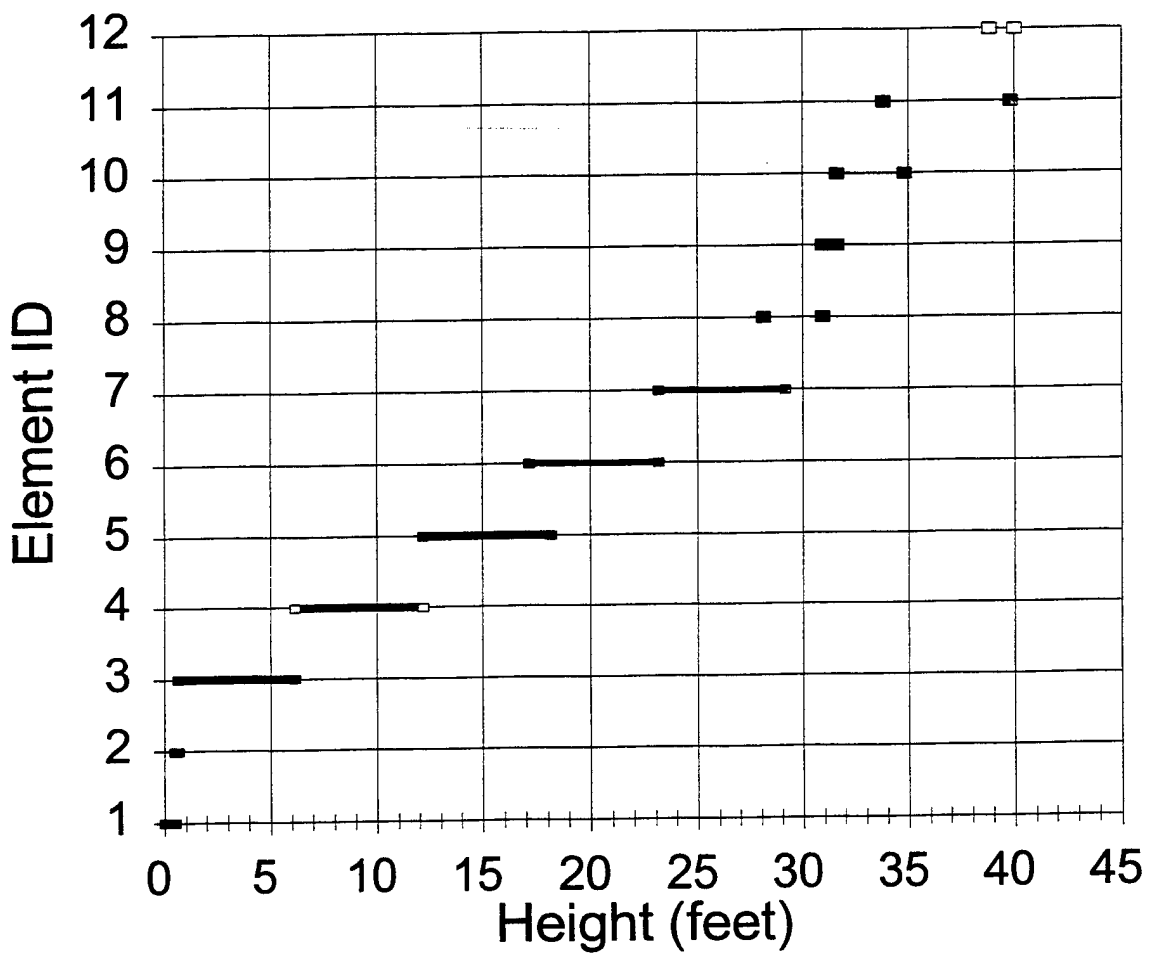
1. All sections of the antenna are aluminum except where noted.
2. All measurements were taken directly from the SNI antenna as deployed at Santa Cruz 1/24/97 except where noted by an asterisk (*).
3. Heights of objects in drawing have been exaggerated to enhance legibility.

Space Physics Research Laboratory College of Engineering University of Michigan		Antenna Dimensions	
PROJECT NUMBER	062-0085	DATE	4 of 4
PROJECT NUMBER	N000149510249	DATE	4 of 4
DATE	05-21-97 NS	RELEASE	COG ENG
DATE		DRAWN	
DATE		CHECKED	

High Band Antenna

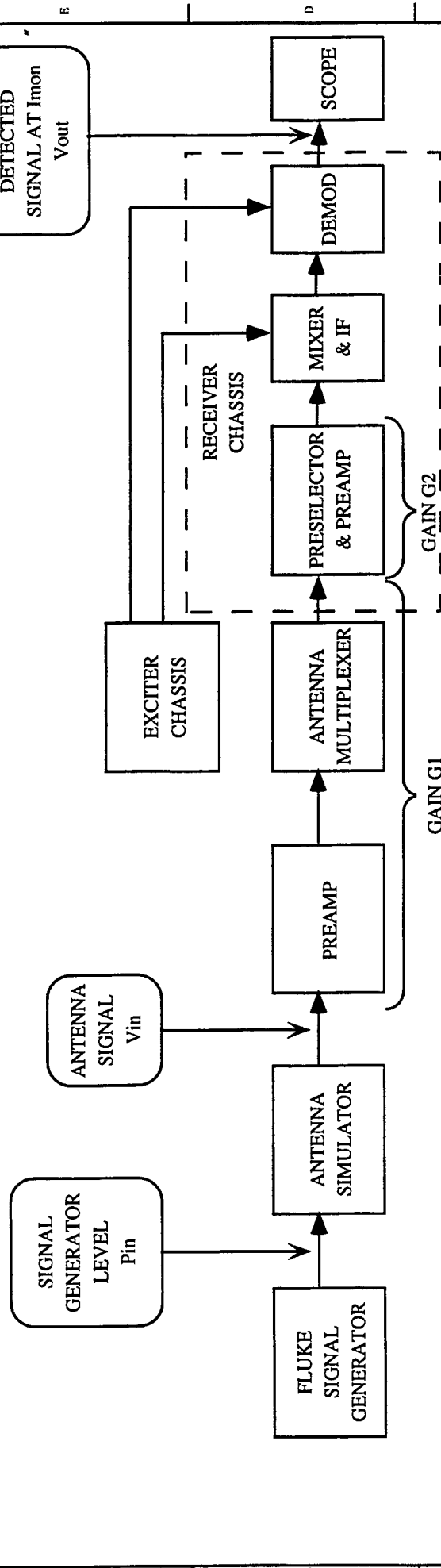


Low Band Antenna



- Gnd
- TB7
- TB8
- DC
- TB1
- TB2
- TB3
- TB4
- TB5
- TB6a
- Trap
- TB6b

**SYSTEM
PERFORMANCE
DATA**



SN 1 DATA (TAKEN 20 SEPT 1996)

TYPICAL SIGNAL LEVELS				
Pin dBm	Vin uV	Receiver Gain Code	Vout Volts P-P	
-80	1	1000	10	
-70	3	900	11	
-60	10	800	13	
-50	30	700	6	

NOTE: MINIMUM RECEIVER GAIN = 700, MAXIMUM USABLE RECEIVER GAIN = 1000

SN 2 DATA (TAKEN 9 MAY 1997)

TYPICAL SIGNAL LEVELS				
Pin dBm	Vin uV	Receiver Gain Code	Vout Volts P-P	
-77	1.66	1600	10	

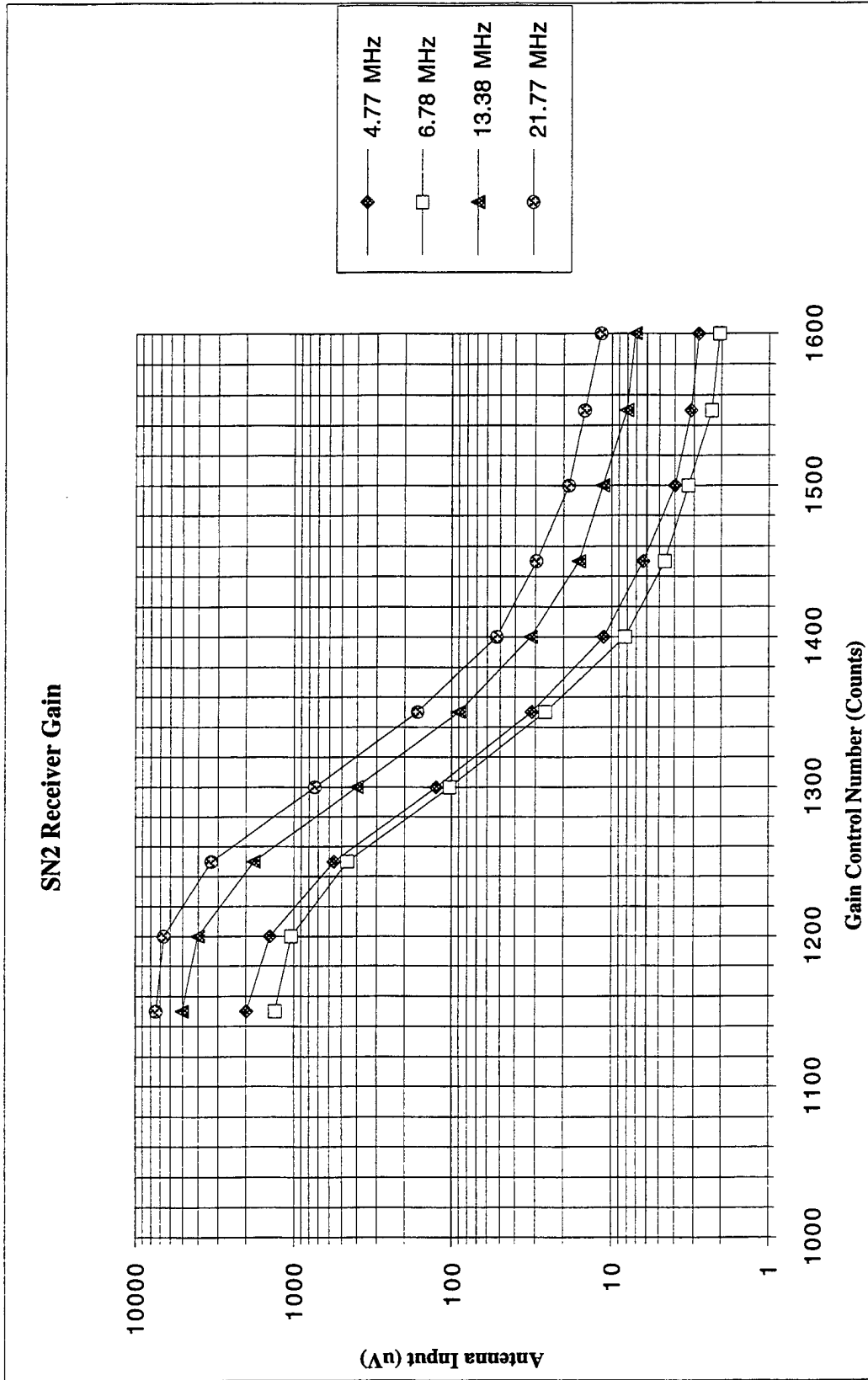
NOTE: MINIMUM RECEIVER GAIN = 1100, MAXIMUM USABLE RECEIVER GAIN = 1600

FREQ MHZ	GAIN		GAIN		G1 + G2 DB
	G1 DB	G2 DB	G1 DB	G2 DB	
4.77	17.2	16.8	17.8	16.8	34
6.78	17.9	17.8	17.8	17.8	35.7
13.38	11.7	14.2	14.2	14.2	25.9
21.77	8.3	15.3	15.3	15.3	23.6

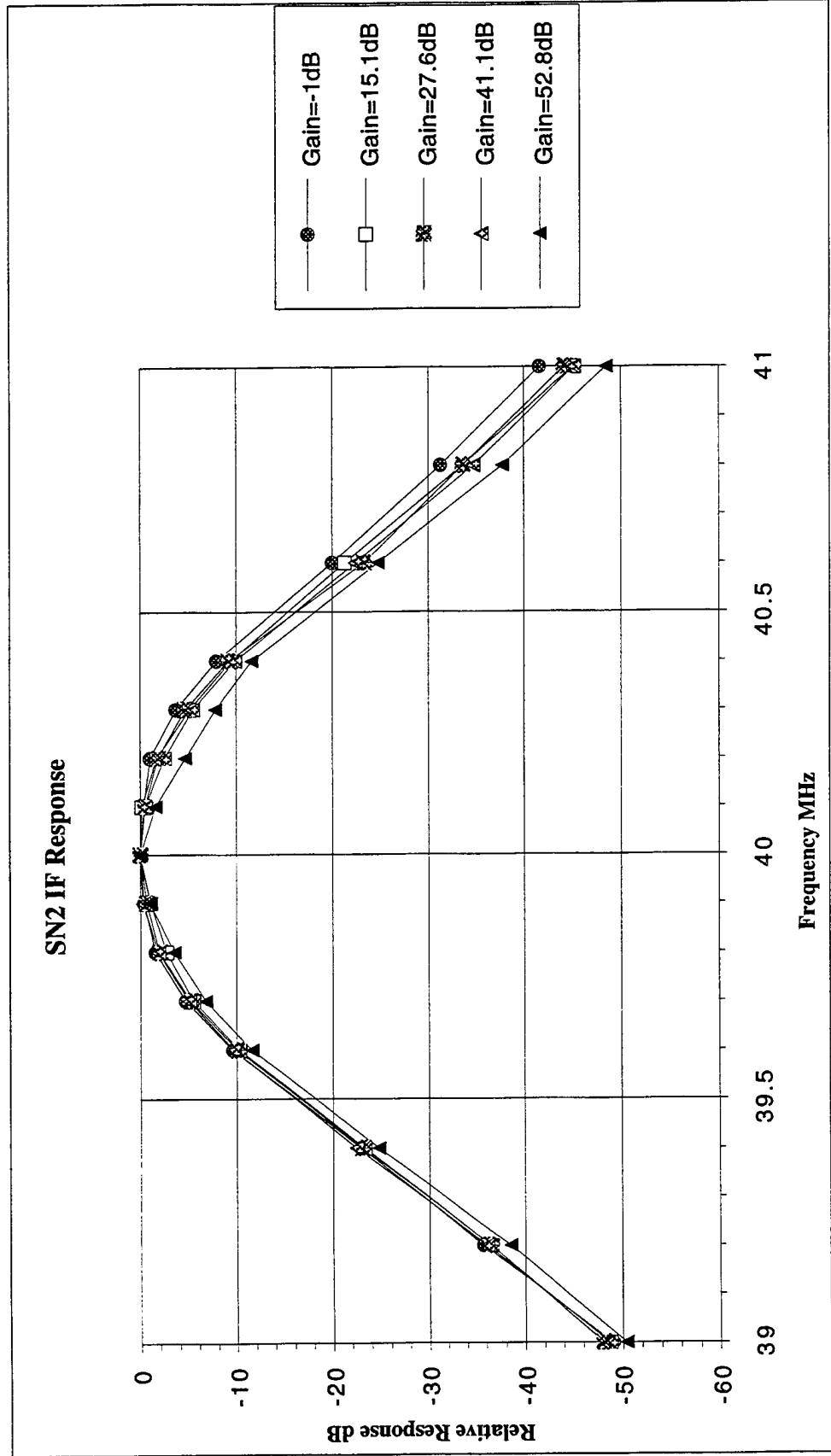
Space Physics Research Laboratory
College of Engineering
University of Michigan

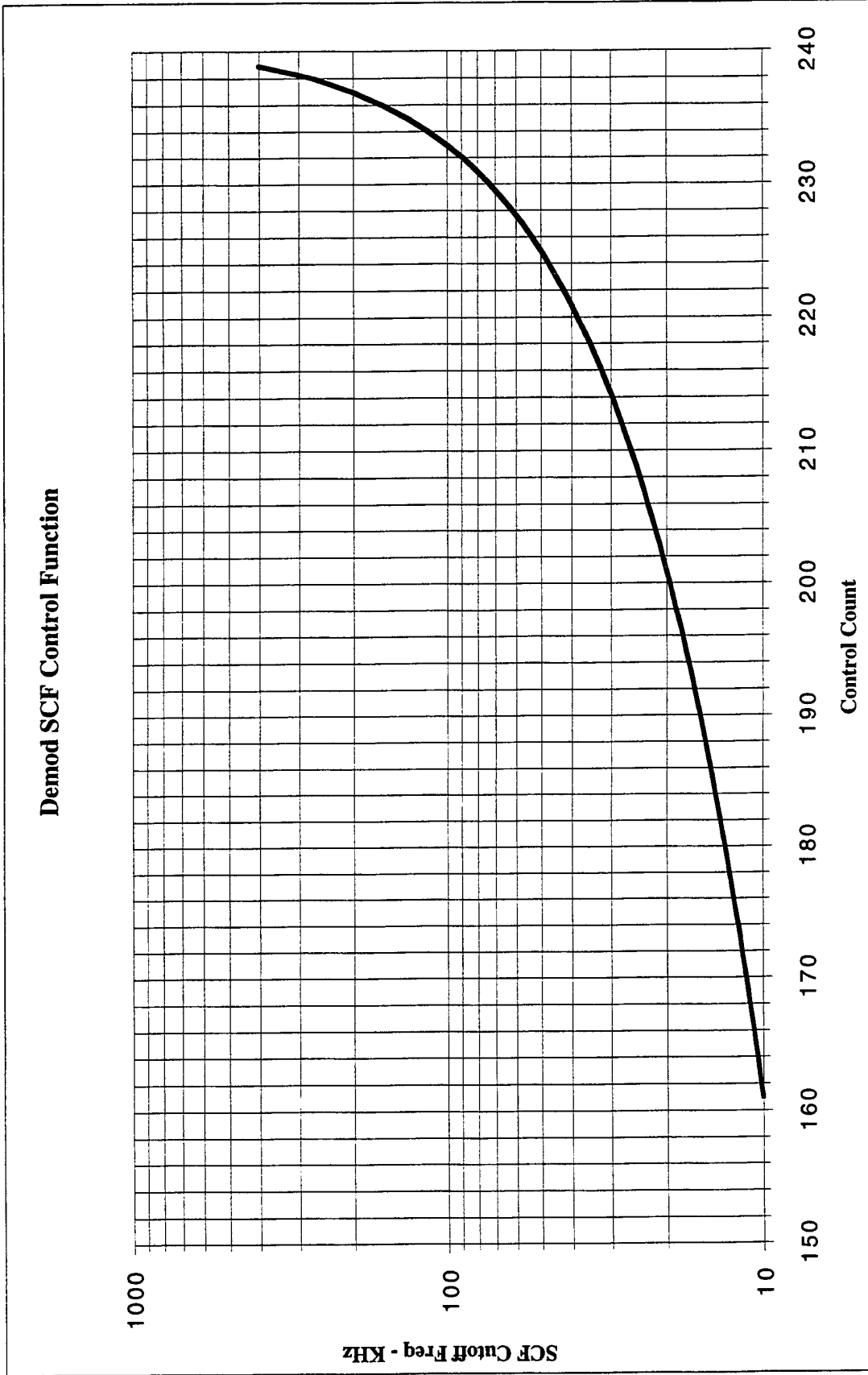
RECEIVER TRANSFER FCN

PROJECT: N000149510249
REV: Rcvr Xfer Function
DATE: 06-2-0160
DRAWN: 05-01-97 NS
RELEASE: 1X 1300 ENG

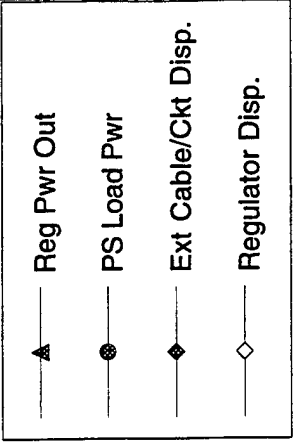
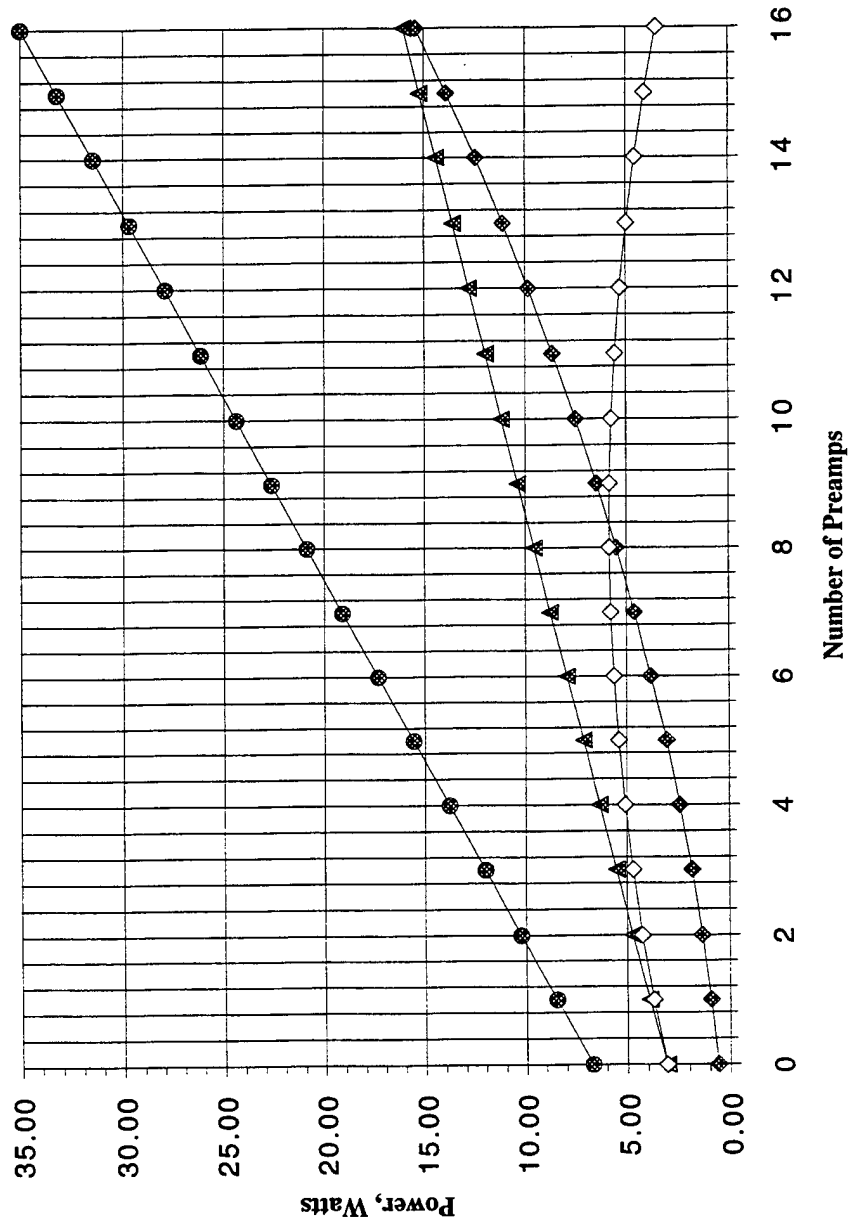


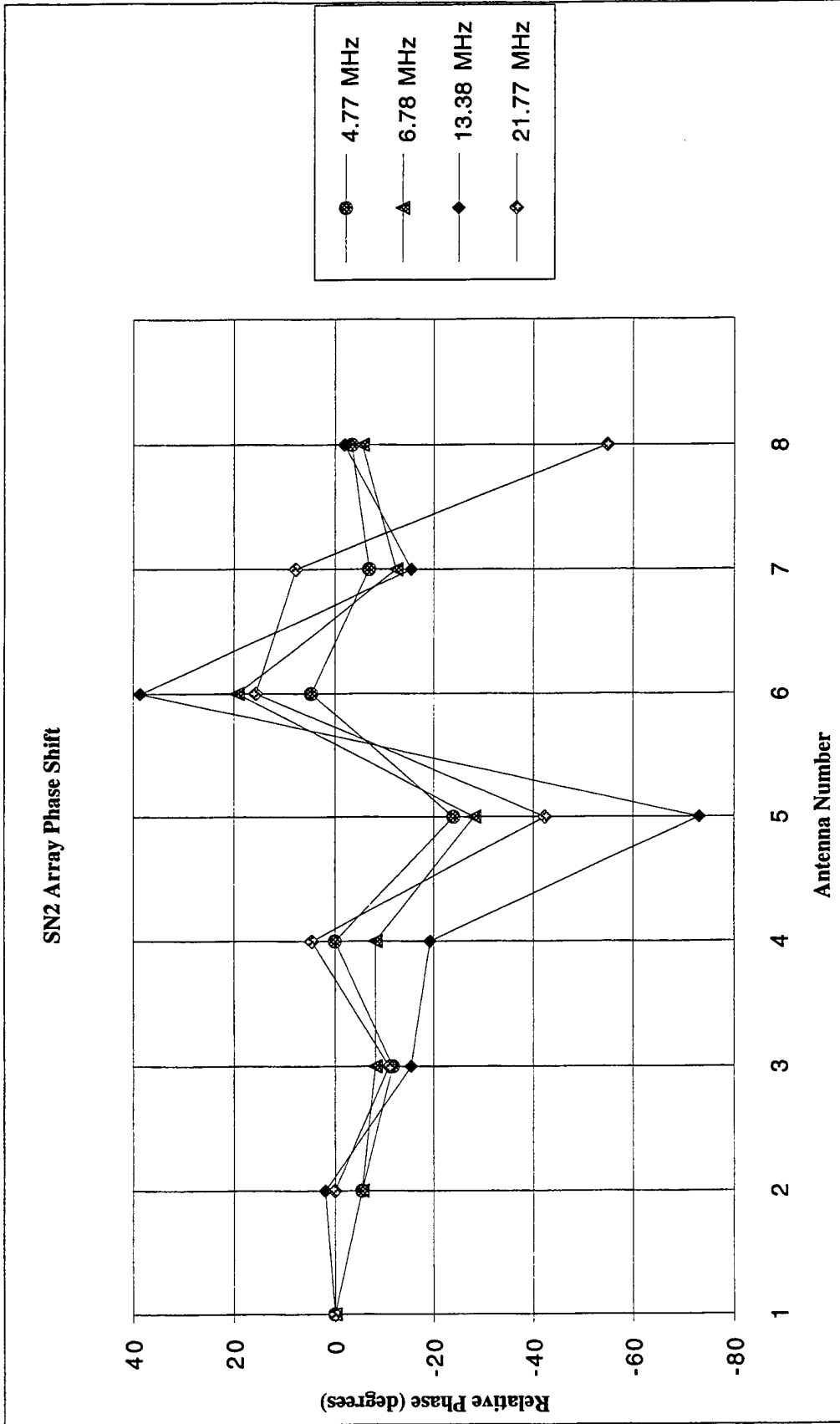
SN2 Gain Calibration Data		Front End Avg Gain													
Taken 1 May 97		Ant Terminals to Mix/IF J1													
Signal levels in chart		dB		MHz											
are for 10 v p-p output from															
demod/A-D interface		34		4.77											
		35.7		6.78											
		25.9		13.38											
		23.6		21.77											
Gain	4.77	4.77	4.77	6.78	6.78	6.78	6.78	13.38	13.38	13.38	13.38	21.77	21.77	21.77	21.77
Code	J1 Sig	Ant Sig	Ant Sig	J1 Sig	Ant Sig	Ant Sig	Ant Sig	J1 Sig	Ant Sig	Ant Sig	Ant Sig	J1 Sig	Ant Sig	Ant Sig	Ant Sig
	dBm	dBm	uV	dBm	dBm	uV	dBm	dBm	uV	dBm	uV	dBm	dBm	uV	uV
1150	-7	-41	1992.9	-9	-44.7	1301.6	-7	-32.9	5063.9	-6	-29.6	-6	-29.6	7404.3	7404.3
1200	-10	-44	1410.9	-11	-46.7	1033.9	-9	-34.9	4022.4	-7	-30.6	-7	-30.6	6599.1	6599.1
1250	-18	-52	561.7	-18	-53.7	461.8	-16	-41.9	1796.7	-13	-36.6	-13	-36.6	3307.4	3307.4
1300	-31	-65	125.7	-31	-66.7	103.4	-29	-54.9	402.2	-26	-49.6	-26	-49.6	740.4	740.4
1350	-43	-77	31.6	-43	-78.7	26.0	-42	-67.9	90.1	-39	-62.6	-39	-62.6	165.8	165.8
1400	-52	-86	11.2	-53	-88.7	8.2	-51	-76.9	32.0	-49	-72.6	-49	-72.6	52.4	52.4
1450	-57	-91	6.3	-58	-93.7	4.6	-57	-82.9	16.0	-54	-77.6	-54	-77.6	29.5	29.5
1500	-61	-95	4.0	-61	-96.7	3.3	-60	-85.9	11.3	-58	-81.6	-58	-81.6	18.6	18.6
1550	-63	-97	3.2	-64	-99.7	2.3	-63	-88.9	8.0	-60	-83.6	-60	-83.6	14.8	14.8
1600	-64	-98	2.8	-65	-100.7	2.1	-64	-89.9	7.2	-62	-85.6	-62	-85.6	11.7	11.7





Ant Mux Powers - 500ft Cables





5/12/97

PREAMP-SN1-FREQUENCY RESPONSE

