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There are two major parts in this report. The first part concentrates on the photoluminescence studies of SiGe layers grown on Si. The second part reports on the investigation of novel nonvolatile random access memory devices. For the first part, multiple exciton complexes confined in potential wells produced by alloy fluctuations are identified. It is found that the size of exciton complex is critically dependent of the size of potential well. The blue-shift of an optical transition line(D1) associated with dislocations is observed and correlated with Si-Ge interatomic diffusion at partial dislocation cores. For the second part, it is unambiguously determined that the band alignment is type-II at the interface of ZnCdSe and InP. Negative differential resistance is observed in a single hetero-interface well-barrier structure with a current peak-to-valley ratio of 30 at room temperature. A bi-resistance device using ZnCdMgSe/InP heterstructure was designed and demonstrated. A novel architecture is proposed for nonvolatile electrical random access memory based on the demonstrated bi-resistance device.

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Highlights of the significant work accomplished

* **Observation of biexcitons three-dimensionally confined in potential wells produced by alloy fluctuation in SiGe epilayers grown on Si substrates**

  The SiGe technology demands controllable crystal quality of SiGe epilayers grown on Si substrates. The photoluminescence (PL) method is a noninvasive method to characterize these layers. Using this method, multiple exciton complexes, confined in potential wells produced by alloy fluctuations, are identified. It is found that the size of exciton complex is critically dependent of the size of potential well. This dependence provides an useful method to characterize a SiGe layer.

  Part of this work has been published in Phys. Rev. B 55, 13058-13061,1997.

* **Correlation of nano-meter scale atomic motion with optical transitions in SiGe grown on Si substrates**

  To understand atomic motion on a nano-meter scale in strained SiGe layers is important for controlling the crystal quality of SiGe layers on Si substrate. This work clearly demonstrated that the blue-shift of an optical transition line (D1) has an one-to-one correlation with Si-Ge inter-atomic diffusion. The optical transition arises from localized electronic states associated with partial dislocations.

  Part of this work is recommended to publish in Appl. Phys. Lett..

* **Band alignment determination at the interface of ZnCdSe and InP**

  The II-VI semiconductor layers grown on lattice-matched InP are new epitaxial structures useful color display devices and other novel electronic devices. Using capacitance-voltage measurements, it is unambiguously determined that the band alignment is type-II at the interface of ZnCdSe and InP.

  This work was published in Appl. Phys. Lett. 69, 2300 (1996).

* **Observation of negative differential resistance (NDR) in a ZnCdSe/InP hetero-structure device**

  For the first time to my knowledge, negative differential resistance has been demonstrated in a single ZnCdSe/InP hetero-interface well-barrier structure. The current peak-to-valley ratio was measured to be 30 at room temperature.

  This work is recommended to publish in Appl. Phys. Lett..

* **Discovery of a new type of bi-resistance devices**

  An unique bi-resistance device using ZnCdMgSe/InP hetero-structure has been demonstrated. The ratio of high to low resistance is about 5 millions. The switching time from high-to-low and low-to-high was measured to be less than 100 ns. Part of this work was submitted to Appl. Phys. Lett. for publication.

* **New architecture design for solid state electrical random access memories (RAM) based on bi-resistance devices**

  A novel architecture is designed for nonvolatile electrical RAMs based on the recently discovered bi-resistance devices. This new architecture uses two diodes which can be integrated on the same InP substrate used for bi-resistance devices. A manuscript is written.

Comprehensive technical summary of each accomplishment

- **Observation of biexcitons three-dimensionally confined in potential wells produced by alloy fluctuation in SiGe epilayers grown on Si substrates**

Although the optical properties of $Si_{1-x}Ge_x$ alloys have been extensively studied, no experimental evidence for the existence of intrinsic biexcitons in $Si_{1-x}Ge_x$ alloys has been reported. The first experimental evidence is obtained for the existence of intrinsic three-dimensionally (3D) confined biexcitons in strain-relaxed $Si_{0.7}Ge_{0.3}$ layers grown on a step-wise graded buffer on Si(100) by ultra-high vacuum chemical vapor deposition (UHV/CVD). A calculation of the PL line shape based on a simple model is found to be in good agreement with experiment. From this theoretical fit, a binding energy is deduced to be 1.55 meV for the 3D-confined biexcitons, which is larger than 1.33 meV for a free biexciton in Si, indicative of quantum confinement effect.

A high-sensitivity PL apparatus was used for low temperature PL measurements. Photoluminescence was collected by a lens combination to enhance the collection efficiency. Samples were excited by an Ar^+ ion laser at normal incidence by one of three lines: 458, 488, or 514.5 nm with an excitation area of 1 mm^2. The samples were immersed in liquid or gaseous helium. The sample temperature was measured using a calibrated silicon diode and could be varied continuously between 1.7 to 300 K. PL was detected by a liquid-nitrogen-cooled Ge detector and analyzed by a computer-controlled Fourier transform spectrometer. Measured PL spectra were corrected for the system's spectral response using a blackbody radiator at a known temperature.

Data for one sample are reported here. This sample is a 3 μm-thick undoped $Si_{0.70}Ge_{0.30}$ layer which was grown on a step-wise graded buffer layer on a lightly boron-doped Si(001) substrate. A similar undoped sample, which shows the same spectral features as this one, has a background hole density of 6×10^{13} cm^{-3}, determined

by a Hall effect measurement at room temperature. The alloy composition and degree of strain relaxation of this sample were determined from double-crystal x-ray diffraction measurements. The average residual strain in sample is 0.0003.

Fig. 1 shows the evolution of the PL spectra in the spectral region of the no-phonon-assisted excitonic emission taken at 2 K, as a function of the photoexcitation power density (P_{exc}) using the 514.5 nm laser line.
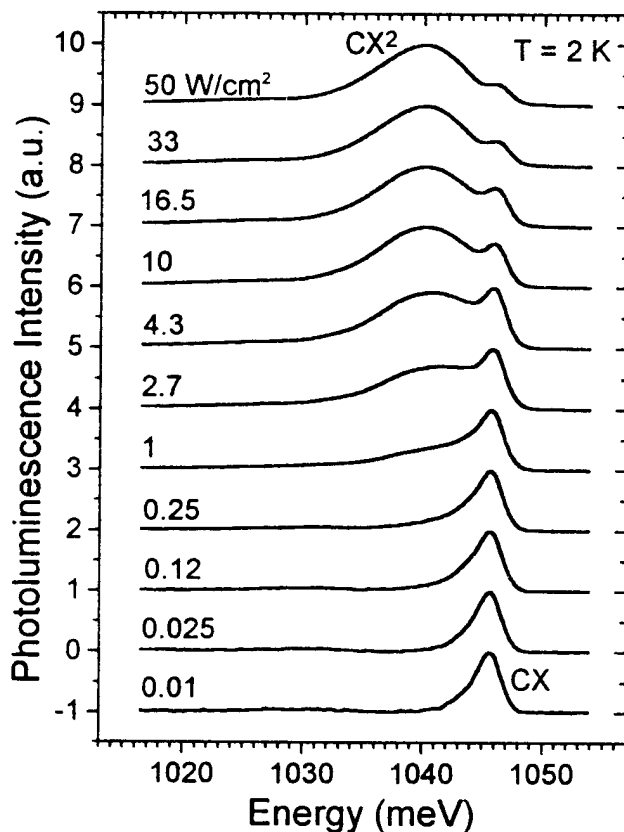

Fig. 1. PL spectra of SiGe/Si sample at 2 K using different excitation power densities. The peak centered at 1040 meV is due to confined biexciton emission. The peak at 1046 meV is due to confined exciton emission.

Upon increasing the excitation power density, the PL spectra change remarkably. When P_{exc} is between 0.01 and 1 W/cm^2, the dominant emission is a narrow peak at 1.0457

eV; another broad peak at 1.040 eV is dominant for P_{exc} from 1 to 50 W/cm^2. It is confirmed that the 1.0457 eV emission is from 3D confined excitons. It is also shown that the 1.040 eV peak is due to the annihilation of 3D-confined biexcitons (CX^2).

- **Correlation of nano-meter scale atomic motion with optical transitions in SiGe grown on Si substrates**

A crucial process in manufacturing semiconductor heterostructure devices is the epitaxial growth of one or more semiconductor layers on a crystalline substrate. Lattice mismatch between the epilayers and the substrate leads to strain in the epilayer, which modifies the optical and electronic properties of the epilayer, either desirable or to be avoided. If the strain becomes large enough, it can be relieved by forming various types of threading dislocations. Those dislocations give rise electronic states within the band gap of the epilayer. By measuring low temperature photoluminescence spectra, these electronic states (both energy position and the density of states) were investigated in SiGe layers grown on Si substrates for various different Ge compositions, different buffer layer, and different post-growth annealing conditions. It is found that the electronic states arising from a partial dislocation core can be controlled by the rearrangement of Ge atoms near the core through post-growth annealing. For the first time, a strong interaction of D1 and D2 states, characteristic of dislocations in Si and SiGe alloys has been observed. This strong interaction is manifested by the occurrence of energy level anti-crossing behavior when the photoluminescence emission peaks of D1 and D2 bands are measured as a function of annealing temperature. This important observation enables us to prove that the previous assumption (over last ten years) that the D1 emission band is a phonon-replica of D2 emission band is not justified.

- **Band alignment determination at the interface of ZnCdSe and InP**

For II-VI semiconductor device research, the quantum carrier confinement near Zn(0.61)Cd(0.39)Se/InP interface was observed using the capacitance-voltage technique.

From this observation, type II band alignment between ZnCdSe and InP is determined. The value of the conduction band offset at the Zn(0.61)Cd(0.39)Se/InP heterointerface is estimated to be - 120 meV. The type of band alignment and the value of the offset are favorable for using n+ InP substrates to fabricate entirely lattice-matched ZnCdSe based green-blue lasers.

The $Zn_xCd_{1-x}Se/InP$ heterostructure studied in this work was grown on a n^+ InP(001) substrate in a Riber 2300P molecular beam epitaxy system consisting of two growth chambers, one for growth of III-V's and other for the growth of II-VI layers, coupled by UHV transfer chambers. The InP layer was first grown on the substrate using a solid InP source as the phosphorus source. The InP layer exhibited a (2×4) RHEED patern suggesting a phosphorus termination surface. The sample was then transferred to the II-VI chamber where the ZnCdSe layer was grown. The epitaxy structure consists of a 1.08 ± 0.02 μm layer of $Zn_xCd_{1-x}Se$ and 50 nm InP buffer layer. Both layers were unintentionally doped. The layer thickness of ZnCdSe was measured by grooving the sample with a Philtec sectioner and the thickness of InP is estimated by the growth rate. The Zinc composition x = 0.61 was determined from the single crystal x-ray diffraction. The epitaxial layer was studied by photoluminescence. PL and x-ray diffraction data confirmed the good crystal quality. Schottky diodes were fabricated by depositing round-shaped Al contacts with a thickness of 3000 Å and a diameter of 2 mm using a high vacuum e-beam evaporator through a mask onto the $Zn_{0.61}Cd_{0.39}Se$ epilayer. Individual diodes are then cleaved from the wafer and bonded to a device holder. C-V measurements were performed in the dark at room temperature using a computerized HP4248A Precision LCR meter. Many diodes were measured and only a few could be reverse-biased to about 3 volts.
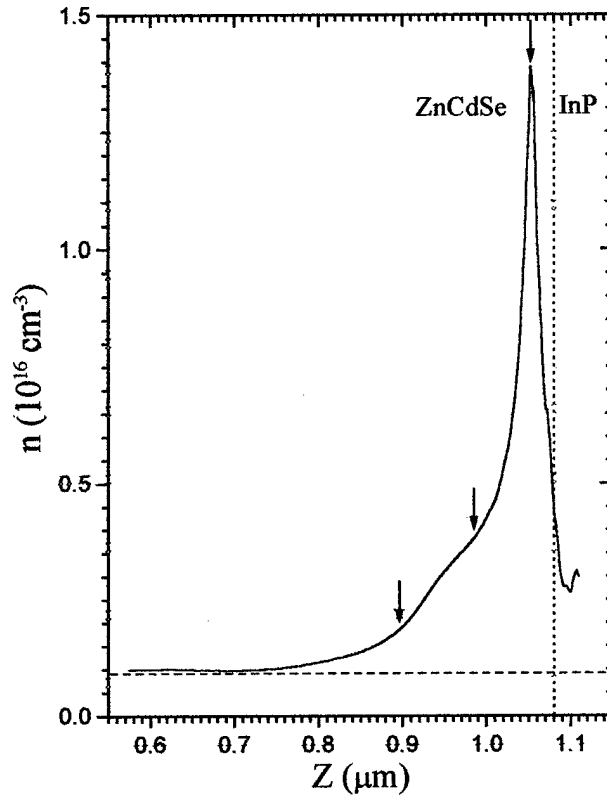
Fig.2. Capacitance-voltage profile of a $Al/ZnCdSe/n^+\text{-}InP(2\times10^{18}$ $cm^{-3})$ device. The depletion depth at zero bias is 0.57 µm. The heterointerface is located at 1.08 µm. The three downward arrows indicate the position-expectation values for the three subband states confined near the ZnCdSe/InP heterointerface.

Figure 2 shows the CV concentration, n(z), obtained from one of our best devices measured at 1 MHz. Several salient features in this CV profile can be described. First, there is an obvious concentration plateau (n_{ZnCdSe}) between 0.57 to 0.75 µm with a value of 1 x 10^{15} cm^{-3}. Second, the CV profile peaks at 1.05 µm and two additional shoulders on the CV profile can be identified at the positions of z = 0.90 and 0.98 µm. They are indicated in the figure by downward arrows. Third, the measured maximum concentration is in the ZnCdSe epitaxial layer side and very close to the ZnCdSe/InP heterointerface. The concentration then sharply decreases and eventually becomes not measurable by further increasing the reverse bias due to the increase of leakage current.

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- **Observation of negative differential resistance (NDR)**
  in a ZnCdSe/InP hetero-structure device

It is important to understand how efficiently electrons can be injected to an active region from a n^+-InP substrate for a successful realization of practical devices based on ZnCdMgSe/InP materials. The current-voltage(I-V) characteristics of an Al/ZnCdSe/n^+-InP device were measured from 77 K to room temperature. A strong negative differential resistance (NDR) under forward bias was observed for temperature higher than 145 K. The peak-to-valley current ratio at room temperature was measured to be 30. In the reverse bias region the device behaves as a Schottky diode. NDR devices based on resonant tunneling in double-barrier structures have attracted much interest since the pioneering work of Tsu, Esaki, and Chang at IBM. This new observation may render II-VI semiconductor compound structures grown on InP substrates technologically useful for millimeter-wave applications.

Devices were fabricated by depositing round-shaped Al contacts with a thickness of 3000 Å and a diameter of 2 mm using a high vacuum e-beam evaporator through a mask onto the $Zn_{0.61}Cd_{0.39}Se$ epilayer. Individual diodes were then cleaved from the wafer and bonded to a device holder for both I-V and C-V measurements. For low temperature measurements, the device was placed onto the cool finger of a cryostat. The I-V data were taken by a computerized HP4142B source/monitor unit.

Figure 3 shows the I-V characteristics obtained from one of our devices measured at room temperature. This device was also used for C-V measurements as described in the last section. There is an obvious strong resonant peak at $V_p = 0.554$ V with a peak current value of $I_p = 3.57$ mA and a deep valley at $V_v = 0.605$ V with a valley current of $I_v = 0.12$ mA. The peak-to-valley current ratio ($\gamma = I_p / I_v$) is 30.
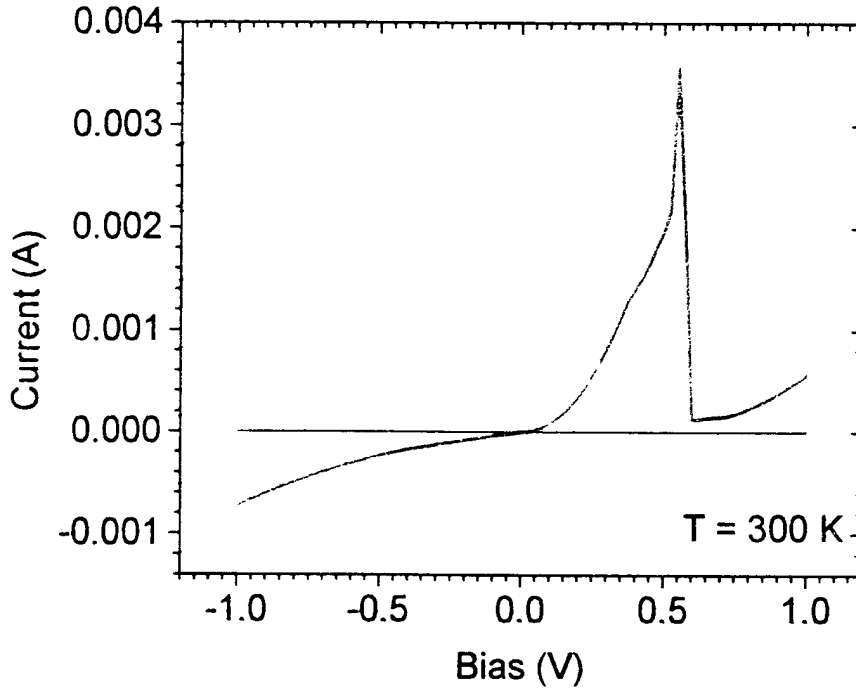
Fig.3. Current-voltage curve of the Al/ZnCdSe/InP(50 nm)/n$^+$-InP(2×10^{18} cm^{-3}) device at room temperature. The peak-to-valley current ratio is 30.

This γ value determines the maximum output power and dc-to-ac conversion efficiency when the device is used for millimeter-wave application. This is a remarkably high value for this resonant tunneling device in comparison with the γ value of 30 for the best studied double-barrier structure. Another figure of merit for a tunneling diode is the speed index, which is defined as the ratio of the peak current to the capacitance at the valley voltage, I_p/ C_v. A large speed index is required for fast switching. For the present device, the value for the speed index is 0.01 mA/pF. This value is about three orders of magnitude smaller than that of a Ge Esaki diode. Since I_p / C_v is proportional to the conductivity of ZnCdSe layer, the speed index can be substantially increased by intentional n-type doping of this layer.

• Discovery of a new type of bi-resistance devices

A new concept for semiconductor bi-resistance devices is proposed in which an unique combination of a Schottky junction with tunable barrier height and an adjacent electron quantum well is used. A proof-of-concept demonstration is given for such a class of bi-resistance devices using a ZnCdMgSe/InP heterostructure.

The devices were fabricated by depositing round-shaped Al contacts with a thickness of 3000 Å and a diameter ranging from 0.5 to 2 mm using a high vacuum evaporator through a mask onto the ZnCdSe(5nm)/ZnCdMgSe(0.75μm)/ZnCdSe(1nm)/InP(200 nm) epilayers grown on a n^+-InP substrate. Individual devices were then cleaved from the wafers and bonded to device holders for I-V measurements. The I-V data were taken at room temperature by a computerized HP4142B source/monitor unit.

The room temperature I-V data taken from a device fabricated from one wafer (A575) are displayed in Fig.4. The applied bias starts at -1.5 V and increases towards 1.5 V. The device is initially in a low resistance state. When the applied bias reaches slightly over 1 V, the current sharply jumps to a current value less than 1 nA. The device has made a transition from low to high resistance state. Moving continuously from ~ 1 to 1.5 V, the device stays at the high resistance state. The device remains at the high resistance state when the applied bias changes its moving direction from 1.5 toward -1.5 V. At about -1.5 V, the device switches back to the high resistance state. This I-V hysteresis can be repeated many times. The device can be either in the on- or off-state even when the applied bias is removed. The value of the current at 0.75 V is 1.218 mA for the on-state and 0.242 nA for the off-state. This remarkable current difference between the on- and off-state with a ratio of 5 millions at a given applied bias gives us a real possibility to develop a new solid state electrical memory technology based on this type of bi-resistance devices.
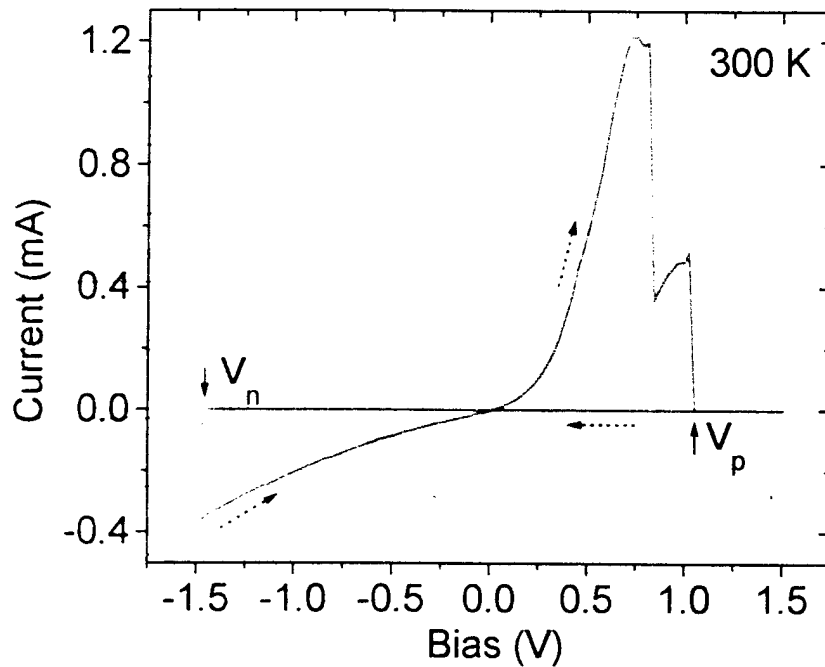
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Fig. 2. I-V curve of the Al/ZnCdSe(5nm)/ZnCdMgSe(0.75μm)/ZnCdSe(1nm)/InP(200 nm)/n⁺-InP device at room temperature.

The value of V_n at which the device makes a transition from the off-state to the on-state is in a range of -1.2 to - 2.5 V and the value of V_p at which the device makes a transition from the on-state to the off-state is in a range of 0.45 to 2 V. Both V_p and V_n depend on the detailed structure parameters and device temperature.

Preliminary transient experiments have been carried out to measure the speed of on-to-off and off-to-on switching. A narrow electrical pulse with a width of ~100 ns was applied to the bi-resistance device which is in series with a normal resistor. The device voltage [V_d (t)] was measured as a function of time using a LeCroy digital oscilloscope. A resolution limited short switching time of 100 ns was measured for the off-to-on transition. For the on-to-off transition, the switching time is about 100 ns.

- **New architecture design for solid state electrical random access memories (RAM) based on bi-resistance devices**

There are two main existing technologies for solid state electrical memories. One is the floating gate technology which produces Electrically Erasable Programmable Read Only Memories (EEPROM) and Flash Memories (FM). The other is the ferroelectric capacitor based technology which yields Ferroelectric Random Access Memories (FRAM). A new type of solid state electrical memory cell is proposed, which relies on the demonstrated bi-resistance device (BRD) as described in the last section. It has the following features: low operating voltage and current, no standby currents, direct fast overwrite capability, and integrable with high electron mobility InP or GaAs transistors and possibly with the main-stream Si transistors.

Based on the specific characteristics of the demonstrated BRD, a novel architecture of NRAM is designed. Different from any other RAM, no transistor is used in the memory cell matrix in this architecture. Because most chip area is occupied by memory cells, the density of the memory cell is intrinsically high. Up to now DRAM has the highest density, because its memory cell consists of only one transistor and one capacitor. For FRAM, although its memory cell also consists of one transistor and one capacitor, the density of FRAM is much lower than that of DRAM because the size of the ferroelectric capacitor is much larger than a normal capacitor. For the new design, since the size of the BRD can be as small as a normal integrated diode, the density of the Bi-Resistance based RAM (BRRAM) can be as high as DRAM.

Fig.5 shows the memory cell matrix of the BRRAM. Each memory cell consists of two normal diodes and one BRD. They are connected to three lines, two row lines and one column line. Using these three lines, each memory cell can be selected, read, and written . A conventional RAM structure uses a word line (row line) and a bit line to access each memory cell.
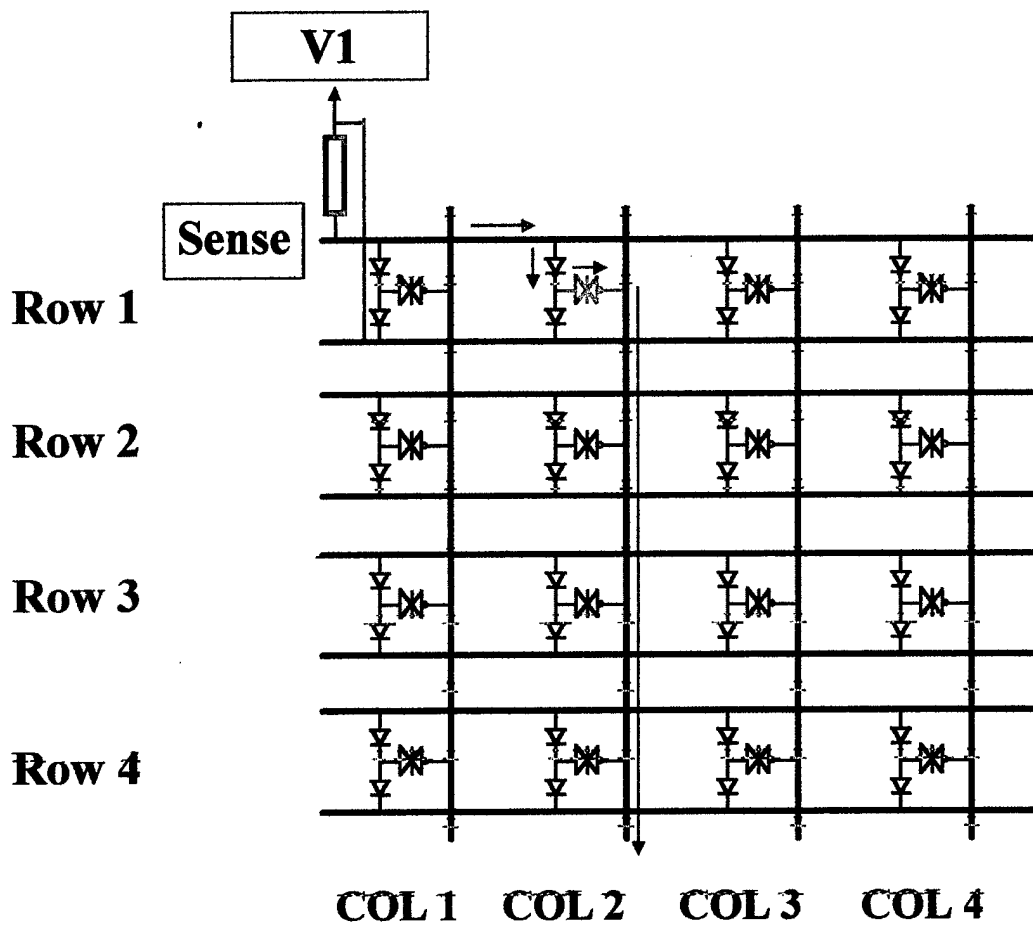
Fig.5.   Memory cell matrix of bi-resistant random access memory

In this architecture, two row lines are used, one is READ/WRITE0 line and the other is WRITE1 line. The column line is bit line. Each bit line is connected to a transition gate which allows two-way current flow. When one bit line is selected, this bit line is connected to ground, all other bit lines are in floating state.

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Haifeng Li (Graduate student)

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Publications:

1. "Observation of quantum carrier confinement near $Zn(0.61)Cd(0.39)Se/InP$ heterointerface", Kai Shum, L. Zeng, N. Dai, and M. C. Tamargo, Appl. Phys. Lett. **69**, 2300 (1996).

2. "Dislocation-related photoluminescence in strain-relaxed SiGe buffer layer structures" Kai Shum, P. M. Mooney, J. O. Chu, Mat. Res. Soc. Symp. Proc. **442**, 325 (1997).

3. "Quantum confined biexcitons in SiGe grown on Si(001)", Kai Shum, P. M. Mooney, L. P. Tilly, and J. O. Chu, Phys. Rev. **B 55**, 13058 (1997).

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