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This Silicon Optical Data Link Program was initiated as a three year effort to develop an monolithically integrated data link using standard silicon fabrication technology. The objectives were to create efficient emitter, waveguide and detector components, integrate the process sequence and demonstrate functionality. The program was prematurely terminated by AFOSR with approximately 50% of the anticipated support awarded. The results enabled by this grant, however, were quite significant. A process for increasing the light output from Si:Er LEDs by greater than 100-fold was demonstrated using UHV-CVD deposition. Our world record transmission through polycrystalline silicon waveguides at a wavelength of 1.54 microns was enhanced by more than two orders of magnitude by passivation of grain boundary defects. The smallest ever waveguide bends and 3dB splitters were fabricated and tested to show low loss. The responsivity of SiGe photodetectors was extended to 1.4 microns by employing bandgap reduction effects of alloying and strain. A key integration issue related to surface roughening by dislocation pile-up in misfit heterostructures was solved and a patent application was submitted. A discrete optical dta link was fabricated and analog voice transmission using silicon photons was demonstrated for the first time.

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SILICON OPTICAL DATA LINK

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SILICON OPTICAL DATA LINK

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Contents

Chapter 1

Executive Summary

This Silicon Optical Data Link program was initiated as a three year effort to develop an monolithically integrated data link using standard silicon fabrication technology. The objectives were to create efficient emitter, waveguide and detector components, integrate the process sequence and demonstrate functionality. The program was prematurely terminated by AFOSR with approximately 50% of the anticipated support awarded. The results enabled by this grant, however, were quite significant. A process for increasing the light output from Si:Er LEDs by greater than 100-fold was demonstrated using UHV-CVD deposition. Our world record transmission through polycrystalline silicon waveguides at a wavelength of 1.54 microns was enhanced by more than two orders of magnitude by passivation of grain boundary defects. The smallest ever waveguide bends and 3dB splitters were fabricated and tested to show low loss. The responsivity of SiGe photodetectors was extended to 1.4 microns by employing bandgap reduction effects of alloying and strain. A key integration issue related to surface roughening by dislocation pile-up in misfit heterostructures was solved and a patent application was submitted. A discrete optical data link was fabricated and analog voice transmission using silicon photons was demonstrated for the first time!

A key to efficient Si:Er light emitting diodes is control of nonradiative processed. These processes are both defect and chemistry related. For Si:Er a loss channel, internal to the 4f core electron manifold, is active. We identified two dominant loss mechanisms: an Auger (free electron) loss at T<200C and a phonon related mechanism at T>200C. We showed the phonon mechanism to result in ionization of free carriers by junction photocurrent spectroscopy. A special bias sequence for injection defeated losses associated with the Auger process. Ligand engineering reduced the phonon related losses and improved room temperature performance. We demonstrated a free space analog voice transmission function using silicon photons from the optimized LEDs. (Chapter 2)

The Er-O ligand configuration introduces donor states in silicon. These donors, as the gateway to Er excitation, affect device design and emission performance. We found a linear correlation between the integrated donor density and the light output. High temperature heat treatment results in outdiffusion of the donor profile and reduced light output. Optimized LED performance requires positioning of the Er-O donor profile within a diffusion length of the junction. (Chapter 3)

The Er-O implant process was optimized by TEM feedback of defect density as a function of implant and anneal process variables. Defects in the form of dislocation loops and precipitates formed at the positions of maximum damage and end-of-range for the Er and O species. Low energy implants, E<400keV, yielded enhanced light output with no residual damage and a reduced thermal budget. (Chapter 4)

Three organometallic precursor molecules were studied for optimization of the UHV-CVD process. $Er(TMHD)_3$ gave the best results. The key is a wide process window between vaporization and decomposition. The maximum light output and minimum defect density was found for Er concentrations of $5x10^{19}cm^{-3}$, eventhough x100 higher concentrations were achieved. (Chapter 5)

The transmission loss for polycrystalline silicon waveguides was reduced from 1000dB/cm to 35dB/cm by control of surface roughness. We reduced the losses further to 15dB/cm by hydrogen passivation of grain boundary absorption sites. This world record level of performance is sufficient for complex data link functions. (Chapter 6)

The high index difference between silicon (3.5) and silicon dioxide (1.5) provides a unique, highly confined medium for light. This high index difference enables routing with sharp turns and wide splitting angles. We fabricated and demonstrated world record performance of 90 degree bends with 2 micron turn radii and 0.1dB loss; and 3dB Y-splitters with emergent angles of 30 degrees and loss less than 2dB. These passive devices allow high density integration of data link components.. (Chapter 7)

Photodetectors for the λ=1.3-1.55μm range were constructed based on strain-balanced superlattices of Si/SiGe. Graded composition templates of fully relaxed $Si_{0.5}Ge_{0.5}$ were used for the epitaxial growth. A p-i-n photodetector with threading dislocation densities less than 10^6cm^{-2} showed charge collection efficiencies of greater than 50% with a responsivity of 3mA/W at λ=1.3μm. We simulated a variety of waveguide-detector coupling schemes to optimize the integrated link. (Chapter 8)

Dislocation pile-ups and surface roughness lead to nonplanarity of highly misfit interfaces and limit process integration. Miscut (001) wafers reduced both effects. We modeled the process and filed a patent application on the method. (Chapter 9)

Chapter 2

Erbium Doped Silicon for Light Emitting Devices

2.1 Introduction

In the past years, the development of silicon light emitters for optoelectronic applications have been the focus of extensive research. Erbium in silicon evolved as one of the most promising candidates for silicon light emission at room temperature. In 1983, Ennen et. al [1] demonstrated electroluminescence from erbium in silicon at 77 K. The next milestone towards room temperature luminescence was the observation that the Er luminescence is increased by more than two orders of magnitude in the presence of oxygen or other ligands[2,3]. Er and O co-implanted Si yielded the first room temperature photoluminescence (PL) of Er in Si [3] and soon afterwards room temperature electroluminescence (EL)[4,5] from LEDs.

During this progress it became obvious that a basic understanding of the excitation and deexcitation processes was needed. The excitation process is still not completely understood[6]. Furthermore, a backtransfer mechanism reduces the emission intensity by more than a factor of 100 at room temperature[2]. In the first part of this chapter we will discuss our latest results on these important processes. Since Er was introduced by ion implantation, an annealing step to remove lattice damage is necessary. The right annealing temperature and duration is critical for achieving optimum emission intensity. In order to integrate these devices with standard CMOS technology, a process flow that takes into account the thermal budget of the MOSFET devices and the LED has been developed. The second part of the chapter deals with the issue of device integration and we will show that MOSFET drivers and LEDs can be fabricated on a single chip.

2.2 Excitation and Deexcitation Processes

The excitation efficiency of erbium in silicon is controlled by different competing mechanisms. In Figure 2.1 these energy transfers are divided into four categories. After excess carrier generation excitons form due to the indirect band gap of silicon which results in a long carrier lifetime. Excitons then recombine in three different processes. The exciton-electron Auger recombination transfers the exciton energy to a free electron. Free and bound exciton radiative recombination is one recombination path for light emission from silicon. These exciton recombination processes compete with the intracenter Auger excitation which excites the lowest spin-orbit level, $^4I_{15/2}$, of the Er^{3+} 4f manifold. A state in the gap acts as a gateway for energy flow to and from the Er 4f-shell but has little overlap with the 4f-manifold wavefunctions. A direct correlation between Si:Er-O emission intensity and donor state introduction has been observed[7]. Once the 4f manifold is excited, two processes can occur to relax the excitation. Radiative recombination leads to the 1.54 μm emission, while the nonradiative backtransfer reduces the emission intensity. All processes before the erbium excitation, faster than the Er radiative recombination process, determine the pumping efficiency but do not influence the emission lifetime. For parallel processes after excitation, the fastest process dominates the emission lifetime. Therefore for a slow

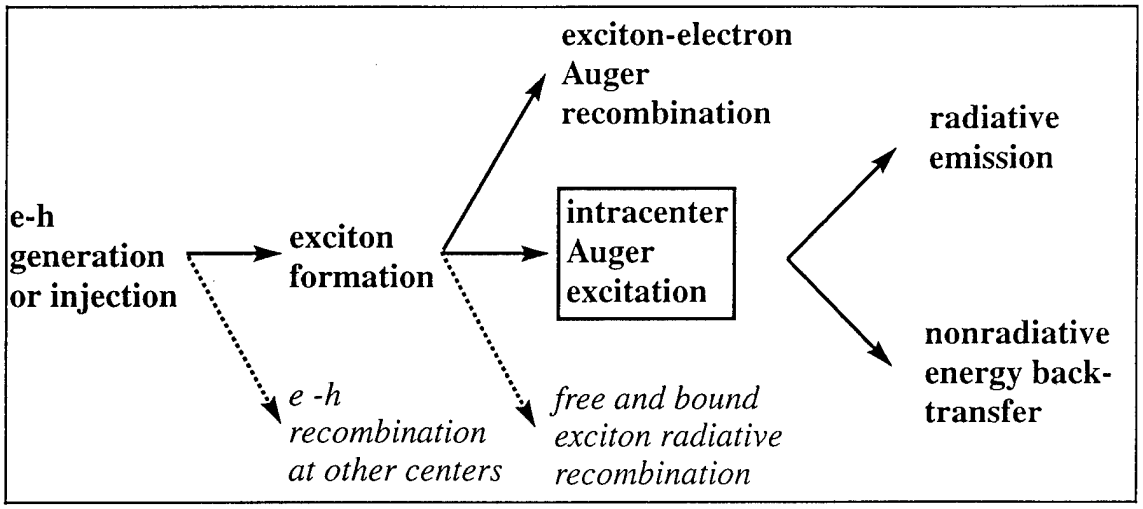

Figure 2.1. Energy flow of excitation and deexcitation processes in Si:Er

radiative process as is the case for excited erbium, a fast nonradiative backtransfer process will dominate the radiative lifetime of the emission. If there is no backtransfer process, any decrease in the radiative lifetime (increase in the photon emission rate) will increase the emission intensity.

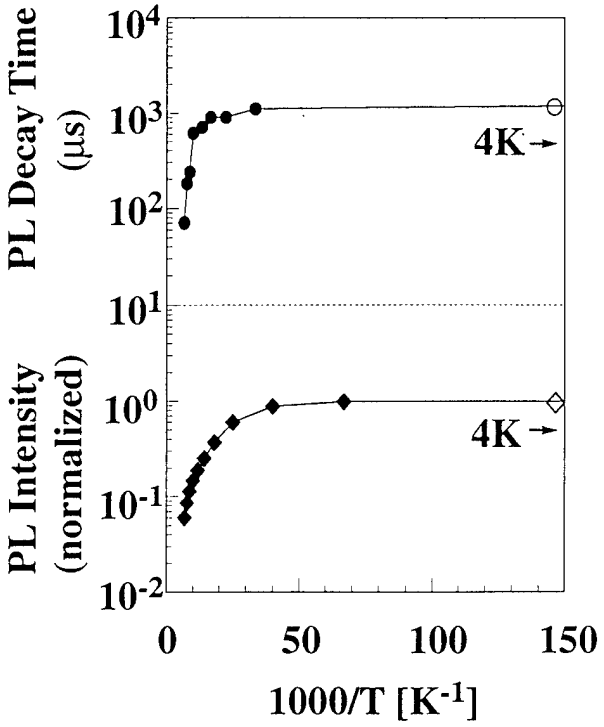

Figure 2.2. Dependency of PL Intensity and luminescence decay time on temperature

A measurement of luminescence lifetime and corresponding luminescence intensity for temperatures below 100K is shown in Figure 2.2. Both curves show a decrease with increasing temperature, which indicates the existence of a nonradiative energy backtransfer from the first excited state. Experiments on lifetime measurements of the emission dependence on the bias state of an electroluminescent device showed that with increasing forward bias the emission lifetime decreases[8]. During forward bias conditions, minority carriers are injected into the junction region. A reverse bias between injection pulses that depletes the junction area always yielded an emission lifetime above 500 μs, close to the observed Er lifetime of about 1 ms, while a forward bias decreased the emission lifetime to 70 μs and smaller. These experiments confirm the existence of an Auger process at low temperature (< 100 K), where free conduction band electrons absorb the energy of the excited 4f manifold and, therefore, compete with the radiative process.

In the higher temperature regime (> 100K) energy backtransfer through phonon processes dominates[9]. Figure 2.3 shows the results of junction photocurrent spectroscopy (JPCS) on an Si:Er LED. The LED was used as a photodetector and the spectral response of the current was measured. In Fig. 2.3 a) the JPCS response is compared with an electroluminescence spectrum of the LED. The comparison shows that the JPCS signal at

1.54 μm originates from Er^{3+}. This photocurrent can only be observed if the energy of the excited 4f manifold can be transferred to the conduction band electrons. The spectral response clearly shows the existence of a backtransfer from the excited erbium where the energy is transferred to a valence band electron. The temperature dependence of the photocurrent at 1.54 μm exhibits a temperature activated process with an activation energy of 170 meV (Fig. 2.3 b).

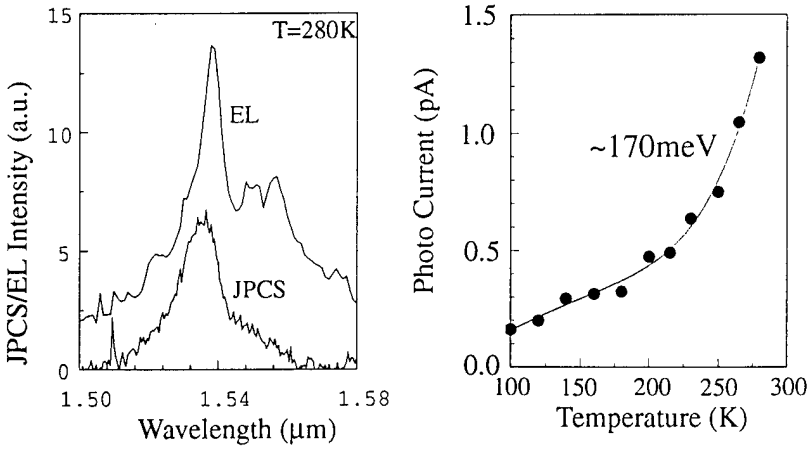

Figure 2.3. Junction photocurrent spectroscopy on a Si:Er LED. a) shows the JPCS spectrum compared to an EL spectrum from the same LED, b) shows the temperature behavior of the JPCS intensity.

The excitation and deexcitation can be described by the configuration coordinate diagram in Figure 2.4. E_g is the silicon bandgap, E_{4f} the energy of the first excited state of the Er 4f manifold, and E_A is the ionization energy for the erbium related donor state[7]. $[Si:Er^{3+}{}_{z/2}\text{-}O_x]^{+/0}$ decribes the Er-O complex with ground (z=15) and excited (z=13) 4f manifold. + and 0 indicate the ionized and neutral state, respectively. After excitation of a 4f manifold by photon absorption

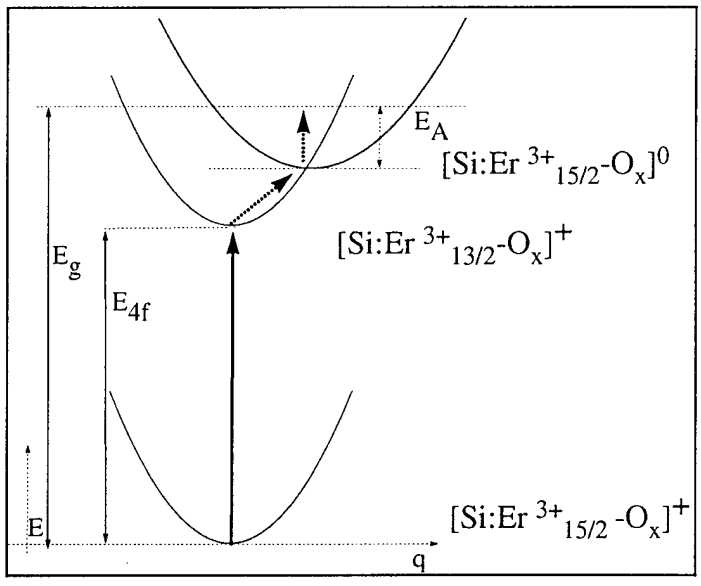

Figure 2.4. Configuration coordinate diagram of the excitation and de-excitation path at temperatures above 100K.

the relaxation can occur radiatively by emitting light at 1.54 μm or nonradiatively via an energy backtransfer. This nonradiative process occurs when the energy of the excited 4f manifold and an additional local phonon energy excite an electron resonantly to induce a transfer from the valence band to the erbium related donor state located about 160 meV below the conduction band[10]. The phonon energy necessary for this process is about 140 meV. Similar local phonon energies can be found in silicon, i.e. the 9 μm absorption band due to a local vibrational mode of interstitial oxygen in silicon. The photocurrent is detected when the electron is thermalized. The measured activation energy (170 meV) of the JPCS temperature dependence indicates that the thermalization is the bottleneck for the backtransfer process. A similar model for ytterbium in InP was suggested by Taguchi et al.[11].

2.3 LED Integration

Process incompatibility between Si CMOS and III-V semiconductors has been a major obstacle for the monolithic integration of Si electronics and compound semiconductor LEDs and other optoelectronic components. To demonstrate that Si:Er LEDs can be integrated with current Si VLSI technology, a circuit including a MOSFET driver in series with an Si:Er LED was processed in a CMOS process flow. For this purpose a twin-well CMOS baseline process was enhanced withadditional processing steps to incorporate monolithic LED processing.

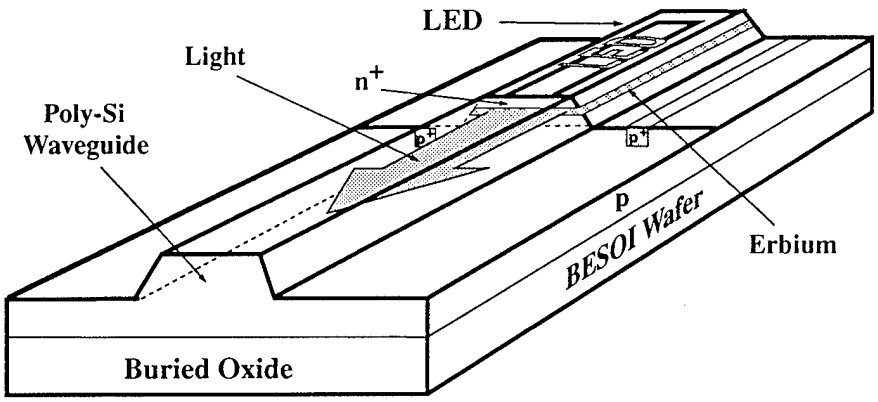

Figure 2.5. Integrated LED-waveguide design for edge emitting LED and multimode waveguide.

As starting material we used

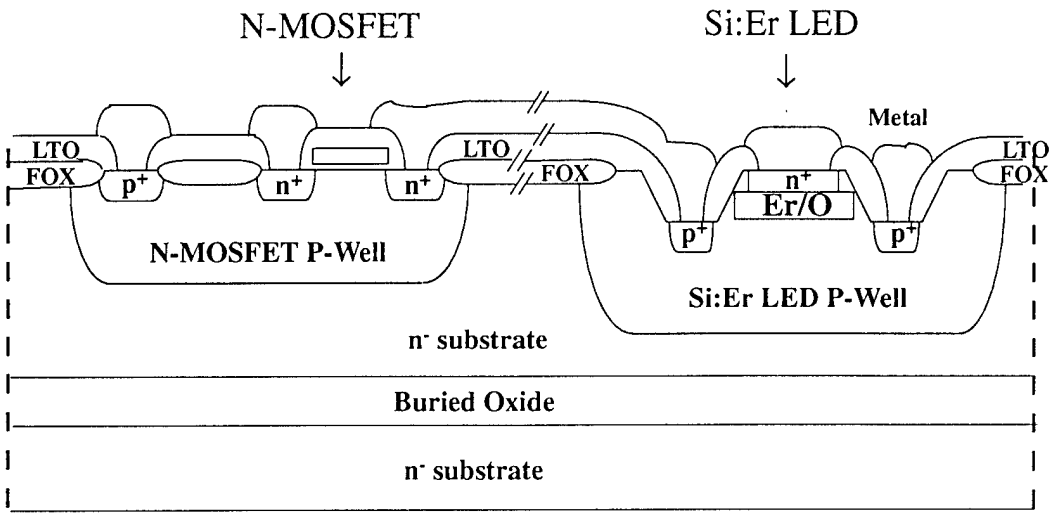

Figure 2.6. Process cross section of a LED - MOSFET integrated design fabricated due to CMOS design rules.

BESOI (Bonded and Etched-back Silicon-On-Insulator) wafers in order to utilize the integrated LED/waveguide design, shown in Figure 5. In this design the light emitted from the Si:Er LED couples longitudinally into a silicon waveguide without the typical coupling losses. This design is possible because silicon is transparent at $\lambda = 1.54$ μm. The SOI wafermaterial provides a single crystalline silicon top layer with a thickness of about 5 μm, which is necessary for the 4.5 MeV erbium implant and advantageous for waveguiding in an integrated waveguide structure. The large index difference between the crystalline silicon top-layer (n = 3.5) and the buried oxide (n = 1.5) provides light propagation with low loss. Simulations confirm that these structures can be used for multimode waveguiding.

Standard 2 micron design rules were used to ensure chip functionality. Figure 2.6 shows a process cross section of the integrated devices. A p-well was chosen for the LED because of the enhanced light emission intensity of Er in p-type Si. The p-well depth for the N-MOSFET is 4 μm with a boron concentration of $5x10^{16}cm^{-3}$ while the p-well depth for the LED is 5 μm to accommodate the LED mesa structure. The boron concentration is $1x10^{16}cm^{-3}$. The LED n^+ emitter was formed by an arsenic implant. The LED areas were

protected during MOS implants by photoresist. Duringthe field oxidation the LED area was protected by a nitrite. Er was implanted *after* the CMOS source/drain annealing to reduce the exposure of erbium to high temperatures which is detrimental to the luminescence intensity.

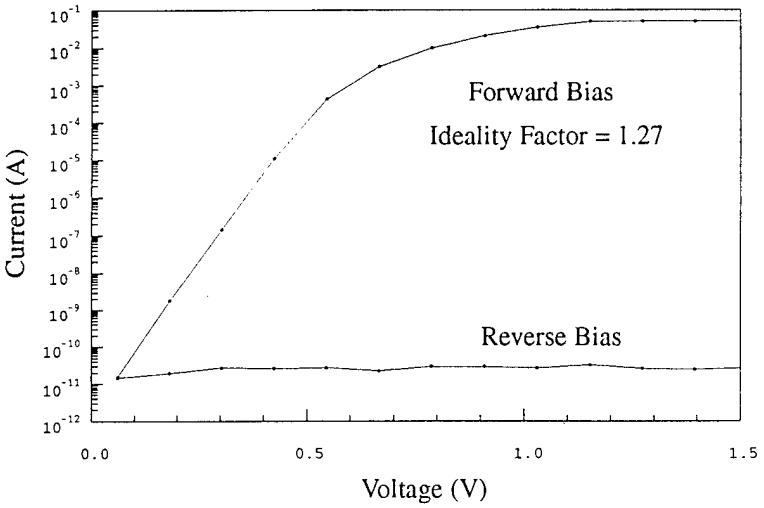

Figure 2.7. I-V characteristic of a Si:Er LED after CMOS processing.

The I-V characteristic of a typical Si:Er LED is shown in Figure 2.7. An ideality factor of 1.27 was measured. The observed I-V characteristics of the integrated LED was similar to that of previously fabricated discrete Si:Er LEDs of p-type Cz material. The high leakage current is most likely due to residual implantation damage like dislocations, observed in the EL spectrum of some LEDs.

Figure 2.8 shows typical LED light emission intensity vs. current density and gate

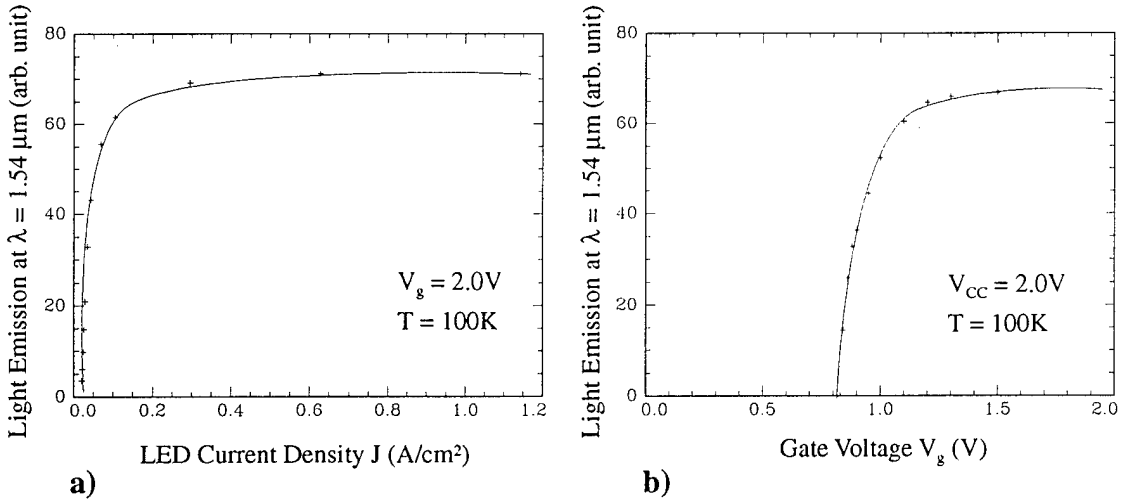

Figure 2.8. a) Er light emission intensity vs. drive current density.
b) Modulation of Er light output by MOSFET gate voltage.

voltage, in a) and b), respectively. The LED reaches saturation at current densities below 200mA/cm-2. The switching behavior of the gate is shown in Fig. 2.8 b). The minimum switching voltage necessary to turn the LED on is 1.3 V. At that voltage, maximum light output is reached. Therefore the light emission can be efficiently modulated by varying the gate voltage around a threshold voltage of 0.8 V. Both figures show that MOSFET and Er doped Si LED are successfully integrated, with expected performance for an Si:Er LED at 100K.

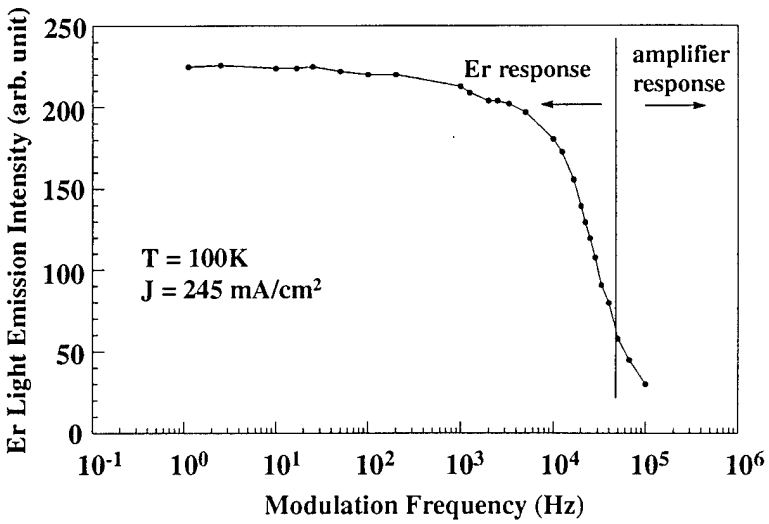

Figure 2.9 . Frequency response of a Si:Er LED. The amplifier response was limited to 20 μs.

The modulation speed of the LED is limited by the lifetime of the first excited state of Er^{3+}. At low temperatures this lifetime is about 1 ms. Palm et al.[8] showed that due to a nonradiative backtransfer the radiative lifetime falls below 100 μs at 100K. Therefore a modulation speed of 10 kHz should be attainable. The frequency response of the LED is shown in Figure 2.9. A fast liquid nitrogen cooled InGaAs detector was used for this measurement. The measurement system response time was limited by the current amplifier to 50 kHz. The amplifier response limit is indicated in the figure. As predicted we found a good response of the LED up to a modulation frequency of about 20 kHz.

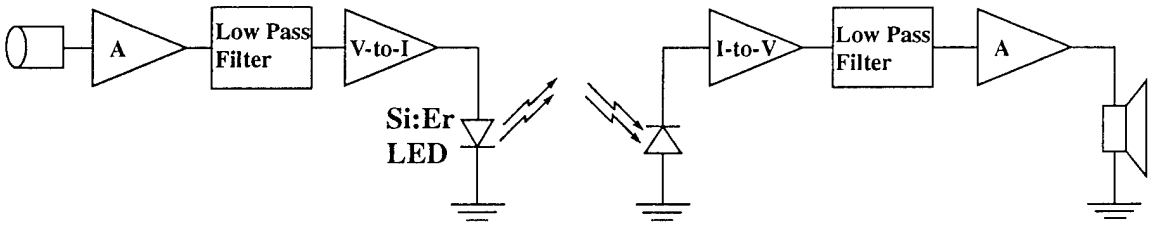

Figure 2.10. Optoelectronic infrared voice link utilizing surface-emitting Si:Er LED at variable temperatures for freespace signal transmission.

A modulation frequency of 20 kHz allows optical voice transmission by our implementation of a cooled Si:Er LED as the emitter and an InGaAs detector as the receiver. Figure 2.10 shows a diagram of the setup. Transmitter and receiver electronics were assembled on separate bread-boards. The light from the LED was collimated and refocussed by two lenses. Room light did not influence the transmission as a narrow optical band pass filter (λ = 1.54 μm, 30 nm bandwidth) was included in the optical path. The distance between lightsource and receiver was varied between 0.2 and 0.5 m. To demonstrate functionality, we used a standard amplitude modulation. Digital encoding and error determination and correction (EDC) of the voice signal will reduce the background noise significantly. The actual response of the system is shown in Figure 2.11. The signal trace was taken with a digital oscilloscope. A signal generator was used in place of the voice input source to supply a continuously variable frequency sine wave to the transmitter. Measurements were made of the output receiver response for two input frequencies, 500 Hz and 4 kHz. The resulting responses are shown in Fig. 2.11 a) and b), respectively. The output receiver noise is due to the large amplification on the detector side, the LED noise is not detectable. Voice transmissions are slightly distorted because of LED I-V non

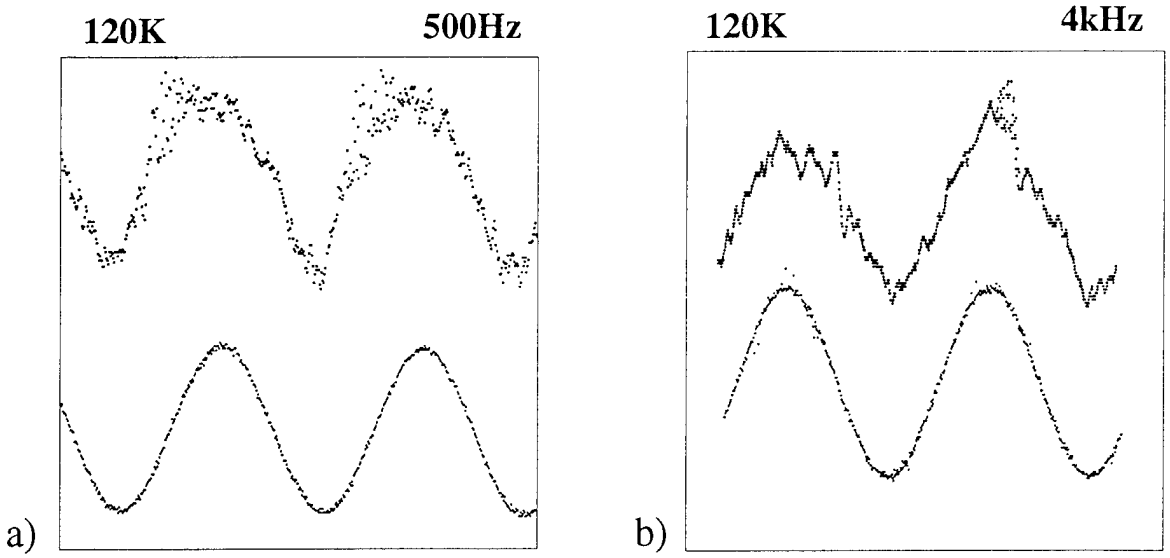

Figure 2.11. Optical transmission of a sine wave using a Si:Er LED. The lower sine wave shows the input signal, the output signal is shown in the upper trace. The signal was measured at 120K for 500 Hz (a) and 4 kHz (b).

linearities. This non-ideality is visible in the deformation of the sine wave after free space transmission.

2.4 Conclusions

We have shown that the nonradiative deexcitation of erbium involves two different processes depending on the temperature regime. Below 100 K an impurity-Auger process competes with the radiative recombination at $\lambda = 1.54\ \mu m$. The efficiency of this process depends on the carrier concentration in the active region of an LED. By reducing minority carriers this backtransfer can be nearly completely suppressed. Above 100K we find a phonon mediated process as the dominating non radiative recombination process of the excited erbium 4f manifold. Both excitation and deexcitation of Er^{3+} can be explained by electron capture of a donor state, correlated with the optically active Er-O complex, and an additional phonon emission or absorption, respectively.

The integration of an Si:Er LED with standard CMOS technology was demonstrated. A MOSFET driver and Si:Er LED were fabricated on a single chip. The frequency response of the LED showed that the LED can be operated below 20 kHz. The functionality of this LED-driver circuit was demonstrated by realizing

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Chapter 3

Optical and Electrical Study of Crystalline Silicon Coimplanted with Erbium and Oxygen

3.1 Introduction

The Si:Er system has received much attention since the sharp luminescence at a wavelength 1.54μm from the 4f shell of the $Si:Er^{3+}$ ion opens the possibility for Si-based optoelectronic applications. We have fabricated room temperature operating LED's based on the Si:Er system,[1] and we have demonstrated that the LED can be used as part of an optical voice link.[2] Er is usually coimplanted with other impurities such as O,C, and F due to their luminescence enhancement effect.[3,4] The Si:Er system suffers from a decrease in luminescence with increasing temperature in two distinct regimes as shown in Figure 3.1. Regime I shows a weak temperature dependence at temperatures from 4K to 100K while regime II reveals an activation energy of 160meV above 100K.[5] The temperature dependence of luminescence intensity is quite similar to that of excited $Si:Er^{3+}$ lifetime as demonstrated in Figure 3.2.[5] We have concluded that a non-radiative energy back transfer mechanism from excited $Si:Er^{3+}$ ions is responsible for thermal quenching of the luminescence at high temperatures. Our observations revealed that the impurity Auger effect accounts for the moderate decrease in the luminescence intensity in the first regime while phonon-mediated processes are responsible for the second regime. It is very important to understand the electronic states introduced by Er/O coimplantation because the excitation and relaxation processes of the Si:Er system are mediated by

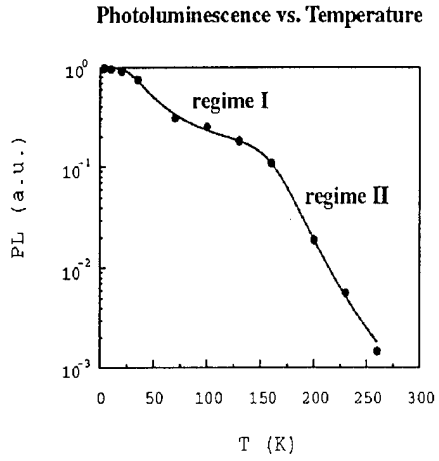

Figure 3.1 PL intensity of Er/O implanted Si is plotted against temperature. Two regimes are observed.

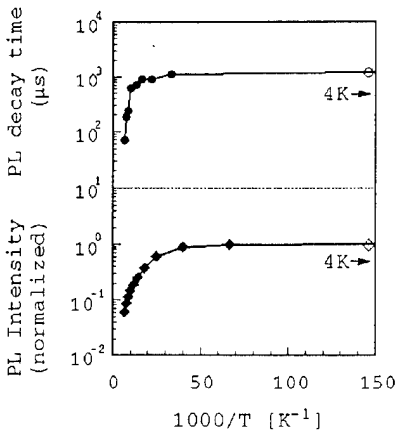

Figure 3.2 PL intensity and decay time are plotted against temperature for Er/O implanted Si.

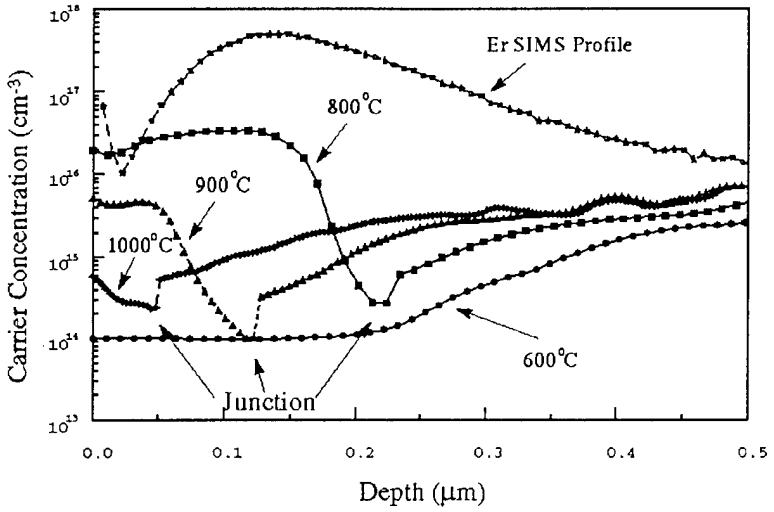

Figure 3.3 Donor distributions determined from spreading resistance profiling in Cz Si Er/O implanted and annealed at different temperatures. The Er SIMS profile is also shown as reference.

recombination centers in the silicon band gap. In this chapter, we address the questions of the electrical activity of Er/O defect states, their structure, and energy levels and we

present a model for the excitation and relaxation processes of $Si:Er^{3+}$ by correlating the electrical properties with the luminescence behavior of the Si:ErO system.

3.2 Experiments

Cz Si wafers were singly implanted with Er at 320KeV, 400KeV, and 4.5MeV. Subsequently, oxygen implantation was implemented at beam energies that match the O peak with the Er peak. The projected range for peak concentrations of $5x10^{17}cm^{-3}$ Er and $2x10^{18}cm^{-3}$ O are located at 0.1μm, 0.14μm, and 1.5μm from the surface, respectively, according to Secondary Ion Mass Spectroscopy (SIMS) profiles. The samples were subsequently annealed in a conventional quartz tube furnace at temperatures between 600°C and 1000°C under Ar ambient for 30 minutes. Spreading Resistance Profiling

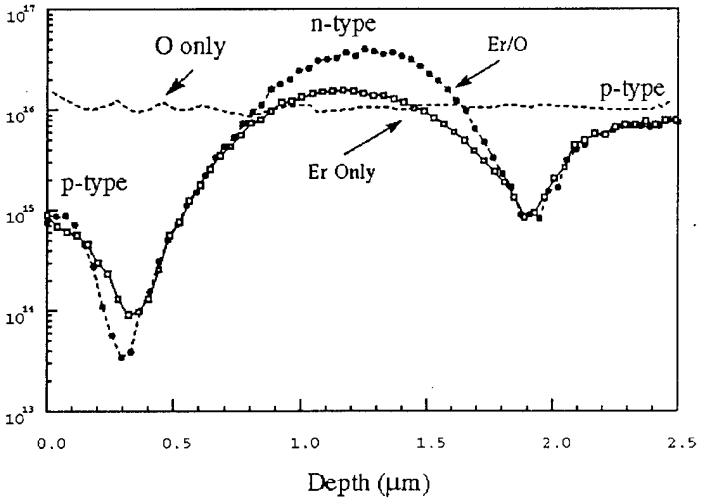

Figure 3.4 Distribution of donors in Cz Si after by O implantation only, Er implantation only and by Er/O coimplantation.

(SRP) measurements were made on p-type Cz Si (0.5-2Ωcm) that was Er/O implanted and annealed. CV measurements were carried out on n-type Cz Si (0.03-0.05Ωcm) after AuPd Schottky contacts were evaporated on n-type Cz Si samples. Hall effect measurements were performed on implantation-induced n-type layer in a p-type substrate.

3.3 Results and Discussion

The Spreading Resistance Profile (SRP) shown in Figure 3.3 confirms that donors are created by Er/O implantation. Three notable features are observed. First, the SRP for the 600°C annealed sample reflects the compensation by implantation damage, and the sample annealed at 800°C shows donor activation with the highest donor concentration. Second, even though one takes into account the observation that the Er SIMS artificially extends the profile to greater depths, the donor profile does not overlap with the Er profile for all the anneals, suggesting that Er by itself cannot explain donor behavior. Third, the donor profile shrinks and moves toward the surface with higher annealing temperatures, implying outdiffusion of donors.

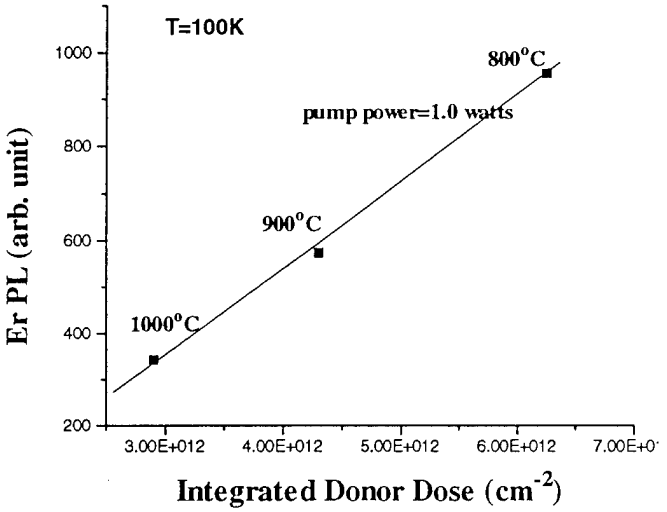

Figure 3.5 PL intensity as a function of integrated donors introduced by Er/O coimplantation.

To identify the defect structure of the donor associated with Er/O doping, several control experiments were carried out. The results are shown in Figure 3.4. Three 4.5MeV Er implanted Cz Si samples were annealed at 900°C after implantation with O only, Er only, and Er/O, respectively. No donor activity is observed for O implant only, while the donor density is lower in the Er implanted sample than in the Er/O implanted sample. The donor concentration continuously increases with increasing Er concentration

to $5x10^{16}cm^{-3}$ donors in Er implanted Cz p-type Si.[6] Based on these observations and the fact that abundant point defects such as Si interstitials and vacancies are generated in the implanted region, there are several possible defect structures for donors: (1) Er/O_x, (2) Er/point defects such as Si interstitial or vacancy, (3) O/point defects and (4) Er/O/point defects. To identify further the defect structure, we examined the correlation of PL intensity with total donors in the sample and found that the PL intensity is linearly proportional to the number of donors as shown in Figure 3.5. The linear relationship implies that the donor is directly related to the optically active center that involves $Si:Er^{3+}$. Therefore, Er must be a component of the donor complex, and the third possibility is eliminated.

To distinguish the donor structure among the rest of possible structures, we analyze the effective diffusivity of donors based on annealing temperature dependence of the donor profiles. Assuming complete activation of the donors at 800°C, one can make a rough estimate of the effective diffusivity of donors by considering the profile at 800°C as reference and taking $D_{donor}(T) = (\Delta x)^2/t$ where D_{donor}, T, Δx and t are donor diffusivity,

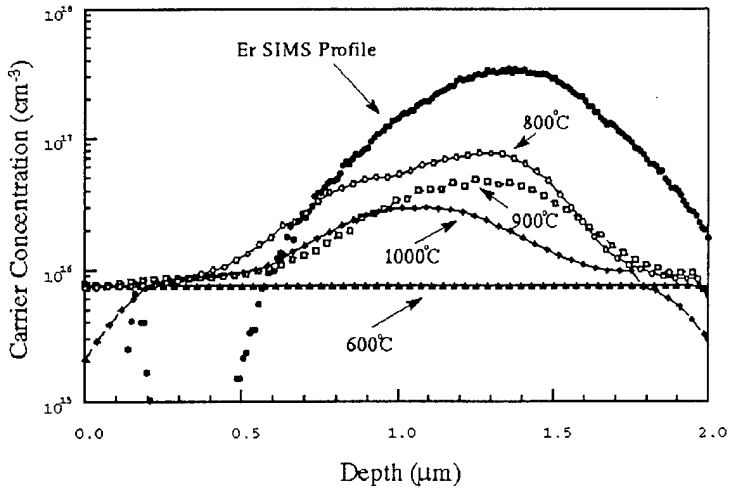

Figure 3.6 Donor profiles of 4.5MeV Er co-implanted with O from spreading resistance measurements at different annealing temperatures.

annealing temperature, position difference between reference and the profile at the given temperature, and annealing time, respectively. However, a more complete analysis should

consider the continued activation of donors at higher temperatures and evaluation of the complete donor profile. This work is in progress. We analyzed annealing temperature dependent donor profiles from the 4.5MeV Er implanted samples, which maintain the shape of donor profile at high temperatures as shown in Figure 3.6. The Δx was measured from donor peak to peak. D_{donor} at 900°C and 1000°C are $1.4x10^{-14}$ cm^2/s, and $3.5x10^{-13}$ cm^2/s, respectively. The activation energy for donor diffusion is estimated from the data to be 4.1eV.

To examine whether the donor outdiffusion is related to Er trap limited motion of oxygen, we model the effective diffusivity of donors with the Er trap limited diffusivity of oxygen, which can be expressed by the following equation [7]

$$D_{oxy,Er}=D_{oxy} * K/[Er]$$

where $D_{oxy,Er}$, D_{oxy}, and K are the Er trap-limited diffusivity of oxygen, oxygen diffusivity, and Er/O dissociation constant. The binding energy of the Er-O complex, E_b, can be reasonably approximated from the Coulombic interaction between the Er^{3+} ion and

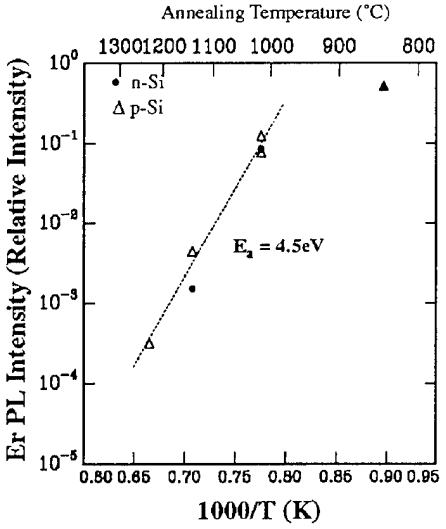

Figure 3.7 PL intensity from Er/O implanted Cz Si as a function of inverse of annealing temperature.

oxygen in silicon. Assuming a singly charged oxygen and an interatomic distance of 2.5Å, one can estimate E_b of 1.5eV. $D_{oxy,Er}$ is $1.3x10^3$*exp(-4.0eV/kT) with D_{oxy}=0.13*exp(-2.5eV/kT) cm^2/s,[9] $K=10^{22}$* exp(-1.5eV/kT), and [Er]= $5x10^{17}cm^{-3}$. The activation energy

and the value of $D_{oxy,Er}$ are calculated to be 4.0eV and $1.1x10^{-14}$ cm^2/s , respectively, which are quite close to the estimated values for D_{donor}. Furthermore, the activation energy for Er trap-limited motion of oxygen is close to the activation energy of the PL decrease by high temperature annealing shown in Figure 3.7. At temperatures greater than 1000°C, dissociation and outdiffusion of donors are dominant. Therefore, the outdiffusion of donors is correlated to the Er trap-limited motion of oxygen. We conclude that $[Si:ErO_x]^{0/+}$is the defect complex responsible for donors associated with Er/O doping.

We have measured the temperature dependence of diode capacitance and carrier concentration by Hall effect to determine the donor energy position in the gap. C vs.T measurements in Figure 3.8 shows the existence of two defect states. Carrier concentration vs. 1/T from Hall effect measurements reveals two activated ionization levels of 40meV and 160meV in Figure 3.9. Excitation of $Si:Er^{3+}$ ions results from trap-mediated recombination which is much more efficient than band-to-band recombination in the $Si:Er^{3+}$ excitation.[9] The donors at 0.16eV below the conduction band edge are most likely the gateway to $Si:Er^{3+}$ excitation. Due to indirect band gap of Si, the injected electrons and holes tend to form free excitons and bound excitons at $[Si:ErO_x]^{0/+}$centers. Both types of excitons can give their energy completely to electrons in the conduction band or phonons in the Si matrix . The e-h pairs bound to $[Si:ErO_x]^{0/+}$centers can excite

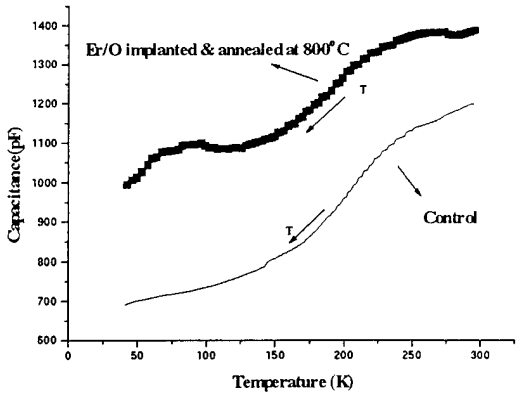

Figure 3.8 Temperature dependence of the capacitnace of a Schottky diode made out of n- type Si Er/O implanted and annealed at 800°C for 30mins.

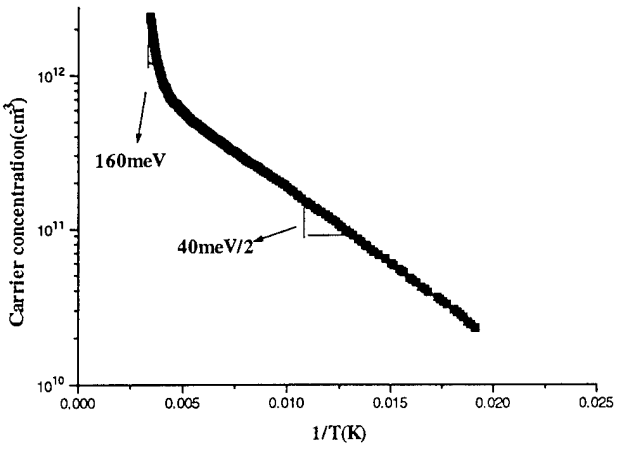

Figure 3.9 Carrier concentration by Hall effect measurement of n-region inverted by Er/O doping in Cz p-type Si is plotted with respect to 1/T.

$Si:Er^{3+}$ ions with the excess energy difference between the resonant excitation energy of $Si:Er^{3+}$ and the recombination energy of a bound exciton being transferred to nearby electrons or local phonons. Although free excitons can excite $Si:Er^{3+}$ ions, bound exciton recombination through the $[Si:ErO_x]^{0/+}$ centers in the band gap will make the Er excitation process much more efficient. More $[Si:ErO_x]^{0/+}$ centers will result in more excited $Si:Er^{3+}$, thus higher luminescence intensity. The excitation and relaxation processes of

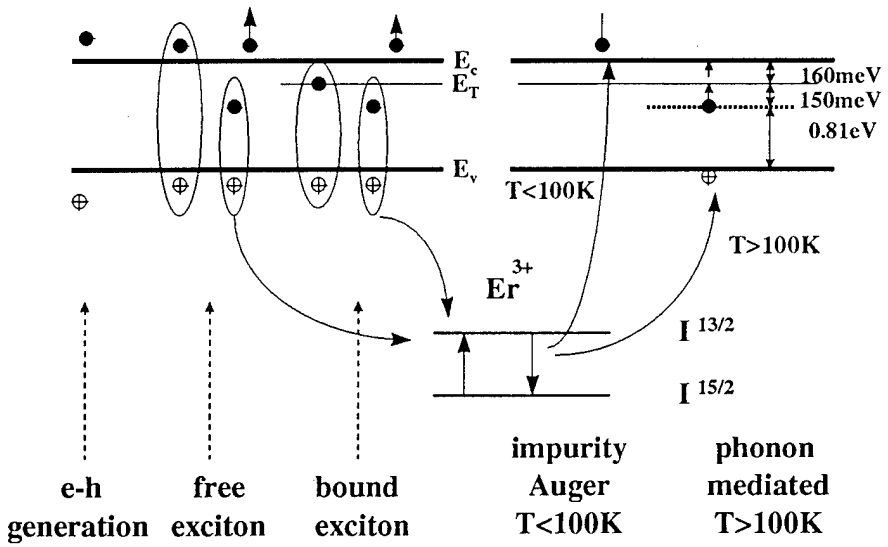

Figure 3.10 A model for excitation and relaxation of Er^{3+} in Si implanted with Er/O is schematically shown .

$Si:Er^{3+}$ ions are schematically demonstrated in Figure 3.10. The de-excitation of $Si:Er^{3+}$ can occur either radiatively or nonradiatively. Figure 3.2 shows that the excited $Si:Er^{3+}$ lifetime decreases together with the luminescence intensity as temperature rises. To explain this observation, there must be internal nonradiative de-excitation paths that are faster than the radiative path for excited $Si:Er^{3+}$. If an inefficient excitation process were responsible for the luminescence quenching, the correlation between the luminescence intensity and the luminescence decay time would not exist. Consequently, nonradiative energy back transfer is responsible for the luminescence thermal quenching.

Below 100K, the impurity Auger effect is dominant so that the back transfer energy flows to electrons as shown in Figure 3.10.[5] Figure 3.11 shows the dependence of the excited state decay time on the LED bias state following injection. Under reverse bias, no carriers are present and the $Si:Er^{3+}$ decay is longest. As carrier density increases to zero and forward bias, the excited state decays become shorter and shorter. This Auger loss at low temperatures has a weak temperature dependence.

Above 100K, the luminescence intensity decreases with increasing temperature with an activation energy of approximately 160meV. Junction photocurrent spectroscopy (JPCS). measurements were with light of wavelengths around 1.54μm and the corresponding photocurrent was measured. JPCS signal reaches a maximum value at the

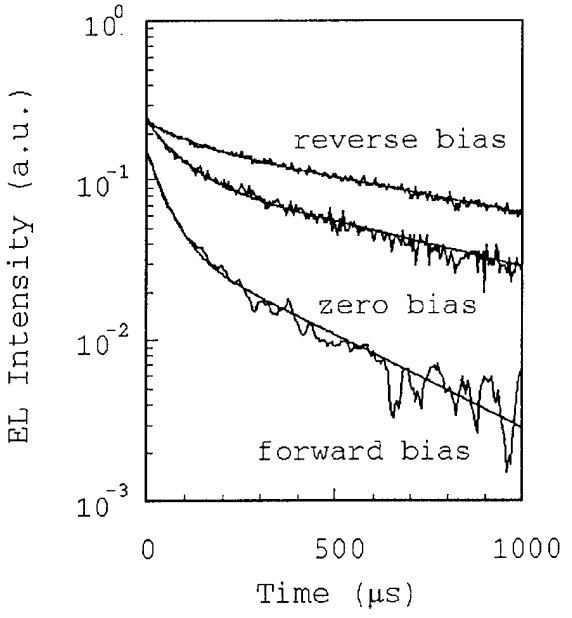

Figure 3.11 Bias dependent EL intensity decay time for an Er/O LED. The luminescence decay time decreases with increasing current.[6]

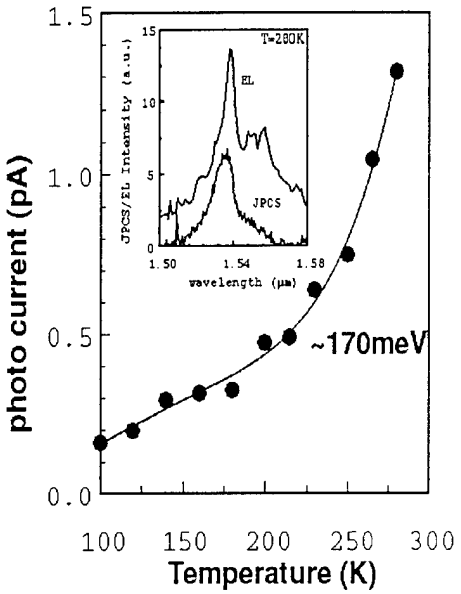

Figure 3.12 Junction photocurrent dependence on temperature for an Er/O LED. The inset shows wavelength dependent junction photocurrent.[6]

excitation wavelength of 1.54μm. Thus, excitation of the core 4f levels can result in valence electron excitation. The maximum junction photocurrent increases with temperature with the activation energy of 170meV as shown in Figure 3.12. Based on these observations, we propose a phonon-mediated nonradiative energy back transfer mechanism in which a charge transfer occurs through the $[Si:ErO_x]^{0/+}$ center. This nonradiative back transfer mechanism takes place in a series of two steps: unfilling the $[Si:ErO_x]^{0/+}$ centers by phonons and filling the $[Si:ErO_x]^{0/+}$ centers with electrons. Phonons provide the energy of about 150meV to the 0.8eV relaxation energy for $Si:Er^{3+}$ to excite an electron from the valence band to the empty $[Si:ErO_x]^{0/+}$ level at E_c-0.16eV. The electrons excited to the $[Si:ErO_x]^{0/+}$ level are further excited to the conduction band to yield a photocurrent. Phonon energies of about 160meV are required to fill and empty the $[Si:ErO_x]^{0/+}$ level. Further investigation is necessary to determine which step is rate-limiting. Nonetheless, it is clear that this energy back transfer is only possible with the aid of phonons and that it becomes more efficient with increasing temperature.

3.4 Conclusion

Both CV and SRP measurements show that Er/O implantation introduces donor levels in the band gap. Donors outdiffuse at high annealing temperatures and the donor

outdiffusion correlates to the Er-trap limited oxygen motion. $[Si:ErO_x]^{0/+}$ is proposed to be the defect complex responsible for the donor activity. Hall effect and temperature dependent capacitance measurements show two energy levels due to Er/O implantation, 40meV and 160meV. The linear correlation between PL intensity and integrated donors further supports that the $[Si:ErO_x]^{0/+}$ centers at E_c-160meV are the gateway to $Si:Er^{3+}$ excitation. Finally, we propose an impurity Auger mechanism below 100K to control luminescence thermal quenching and a phonon-mediated energy back transfer mechanism above 100K.

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Chapter 4

Defects in Erbium/Oxygen Implanted Silicon

4.1 Introduction

Erbium in silicon has attracted considerable interest because of its potential to give high-efficiency sharp luminescence at 1.54 μm which can be excited either optically or electronically [1,2] . This possibility inspires the long sought goal of integrating silicon optoelectronics with very large scale integration (VLSI) electronics to overcome high interconnection density and bandwidth limitations. In order to have strong luminescence, large amounts of optical active Er must be incorporated into the silicon lattice. Ligands, such as oxygen which has been found to significantly increase Er luminescence[2], also need to be incorporated to modify the local environment around Er[3].

Several techniques have been used to incorporate Er into silicon[4-9], but ion implantation, to date, has received the most attention due to its compatibility with IC technology. However, during the implantation process the crystalline lattice of the Si is damaged and an annealing at high temperature is necessary to repair the damage as well as to optically activate the dopant. The secondary defects, such as dislocations, dislocation loops and precipitates, could thus be induced upon annealing which then significantly inhibit the luminescence of Er in Si. Therefore, the optimal processing for the maximum luminescence cannot be realized unless the relationships between processing, structure and properties are thoroughly understood. The main focus of this paper, hence, is on fully understanding the defect behavior of Er/O implanted Si during the thermal annealing.

4.2 Experimental

Erbium was implanted into p-type Cz (100) silicon substrate at an energy of both 4.5 MeV and 400 keV with an implantation dose to produce a profile with an Er peak

concentration of 5 x 10^{17} cm^{-3} to establish whether implantation energy affects the defects. Oxygen was co-implanted to form a peak concentration of 3 x 10^{18} cm^{-3} spatially overlapping Er to form Er/O complexes. Samples were then annealed for 30 minutes in Ar ambient at different temperatures: 600, 800, 900 and 1000°C to examine the dependence of defects on annealing temperatures. An isothermal study at 900°C, which was previously determined to optimize luminescence, was done for times ranging from 15 minutes to 16 hours. Characterization for both as-implanted and annealed materials was conducted using cross-sectional transmission electron microscopy (XTEM), high resolution transmission electron microscopy (HRTEM) and secondary ion mass spectroscopy (SIMS).

4.3 Results and Discussion

Figure 4.1 shows the TEM cross-section images of 400 keV implanted (100)Si after annealing for 30 minutes at 800°C (Figure 4.1a) and 900°C (Figure 4.1b). No advanced secondary defects were observed in the sample although it was implanted in a depth of 1500 Å with peak concentrations of 5 x 10^{17} cm^{-3} and 3 x 10^{18} cm^{-3} for erbium and oxygen, respectively. This implied that either the implantation dose, hence the displacement damage density in the 400 keV implanted sample had not reached the critical value required for the formation of category I defects[10], or the surface-mediated annihilation dominated the annealing of defects.

Figure 1. XTEM week-beam images for 400 keV implanted (100)Si after annealing for 30 minutes at 800°C (a) and 900°C (b) , showing a defect-free material.

In sharp contrast, however, a variety of secondary defects consisting of dislocations, dislocation loops and precipitates are induced during annealing in 4.5 MeV implanted Si. The evolution from a supersaturation of point defects to a layer of dislocation loops with increasing temperatures in a range of 600 to 1000°C is presented in Figure 4.2. When the anneal was done at 600°C for 30 minutes, a population of randomly sized, cluster-like structures was observed as shown in Figure 4.2a. This defect feature is similar to the primary damage distributed in the clustering arrangements to minimize the number of dangling bonds. An 800°C anneal for the same duration resulted in a dissolution of these unstable clusters and a formation of a great number of dislocation loops (Figure 4.2b) and a few dislocations. These small dislocation loops, with an average size of 200 Å, are the predominant secondary defects; They were distributed over a wide depth range between 1.4 μm to 1.8 μm, which was deeper than the peak depth of the dopant distribution (the projected range R_p) of 1.35 μm as determined from the SIMS data. The dislocation loops continued to grow in size and distribute in a deeper layer as the annealing temperature was increased to 900°C, while narrowing in distribution depth (Figure 4.2c). After annealing at 1000°C for 30 minutes, these defects significantly coarsened to an average size of about 1500 Å, with a greatly reduced loop density (Figure 4.2d).

The shrinkage of the dislocation loop band with increasing temperatures was asymmetric; the upper half of the dislocation loop band was annihilated while the lower half of dislocation loops grew in size. This can be explained by the outdiffusion of point defects towards the surface, causing the annihilation of the upper half loop zone. At the same time, the indiffusion of point defects toward deeper layer does not have a sink. Therefore the coalescence of these defects led to growth of the loops in the lower half zone (see Figure 4.2).

Microstructural data for the buried loop band were derived from XTEM images, as illustrated by the set given in Figure 4.3 (a) and (b) which show the change of the dislocation loop bands in the 4.5 MeV implanted material annealed at 900°C for 10 hours and 16 hours, respectively. Isothermal annealing at 900°C revealed a symmetrical shrinkage of the first loop band along with a growth in size and reduction of loop density as annealing time increased for the 4.5 MeV implanted sample (compare Figure 4.2c to 4.3a and 4.3b). A second discrete band of dislocation loops formed in the deeper layers of the sample after longer periods of isothermal annealing mentioned above. Figure 4.3a shows the primary loop band (1st band) became narrow and the second loop zone started to appear. An annealing for six more hours caused an enlargement in the loop size and an

increase in loop numbers in the second loop band (Figure 4.3b). As a result, the second loop band became wider.

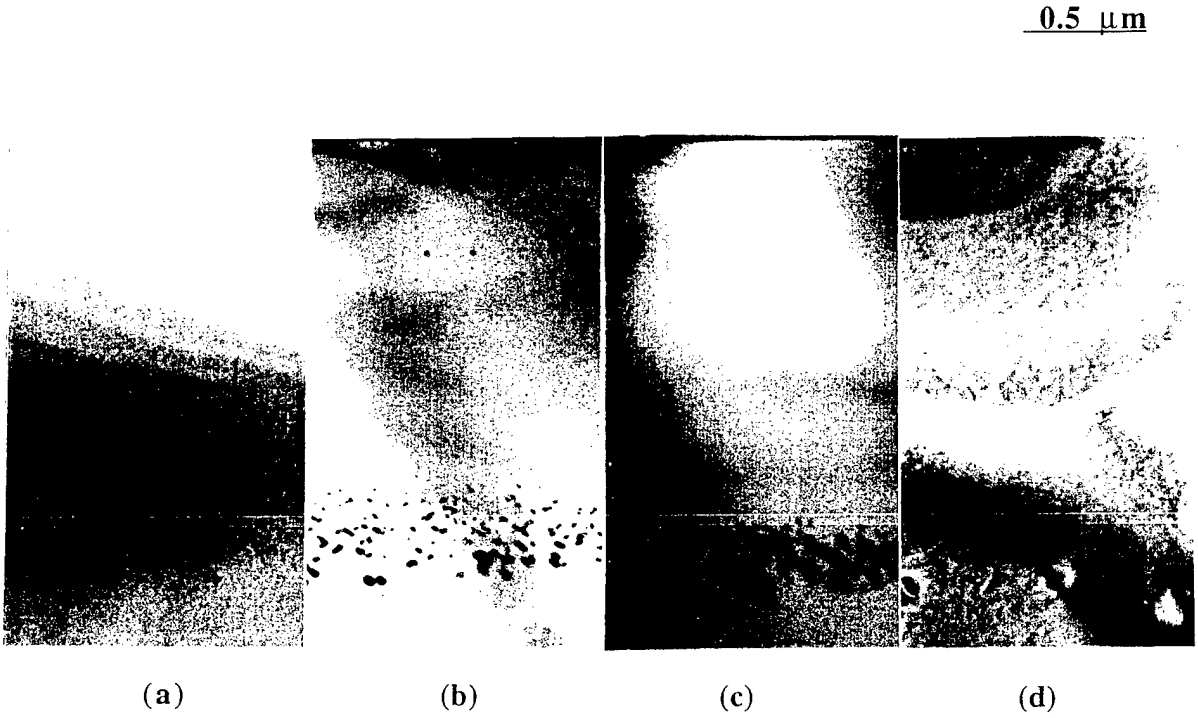


Figure 4.2. XTEM weak beam images demonstrating an evolution of the morphologies and distribution of defects for a 4.5 MeV Er/O implanted (100)Si sample after 30 minutes annealing at different temperatures: (a) 600°C, (b) 800°C, (c) 900°C and (e) 1000°C.

Reactions between dopants and defects has been closely investigated for the 4.5 MeV implanted Si. The SIMS profile of oxygen for the sample annealed at 900°C for 16 hours (Figure 4.3c) shows a well defined two peak feature that well matches the depths for two dislocation loop bands in the TEM image shown in Figure 4.3b. This feature forms a sharp contrast with the profile taken after a 15 minutes annealing which shows only one peak of oxygen distribution with a lower concentration of oxygen (dashed line in Figure 4.3c). The result documents that oxygen segregated into both defect bands which acted as a sink for oxygen during long-term annealing. The driving force for the migration of oxygen into the defect zone may be supersaturation of oxygen and strain cancellation at the dislocation cores. Erbium, however, was not gettered by the dislocation loops, which can

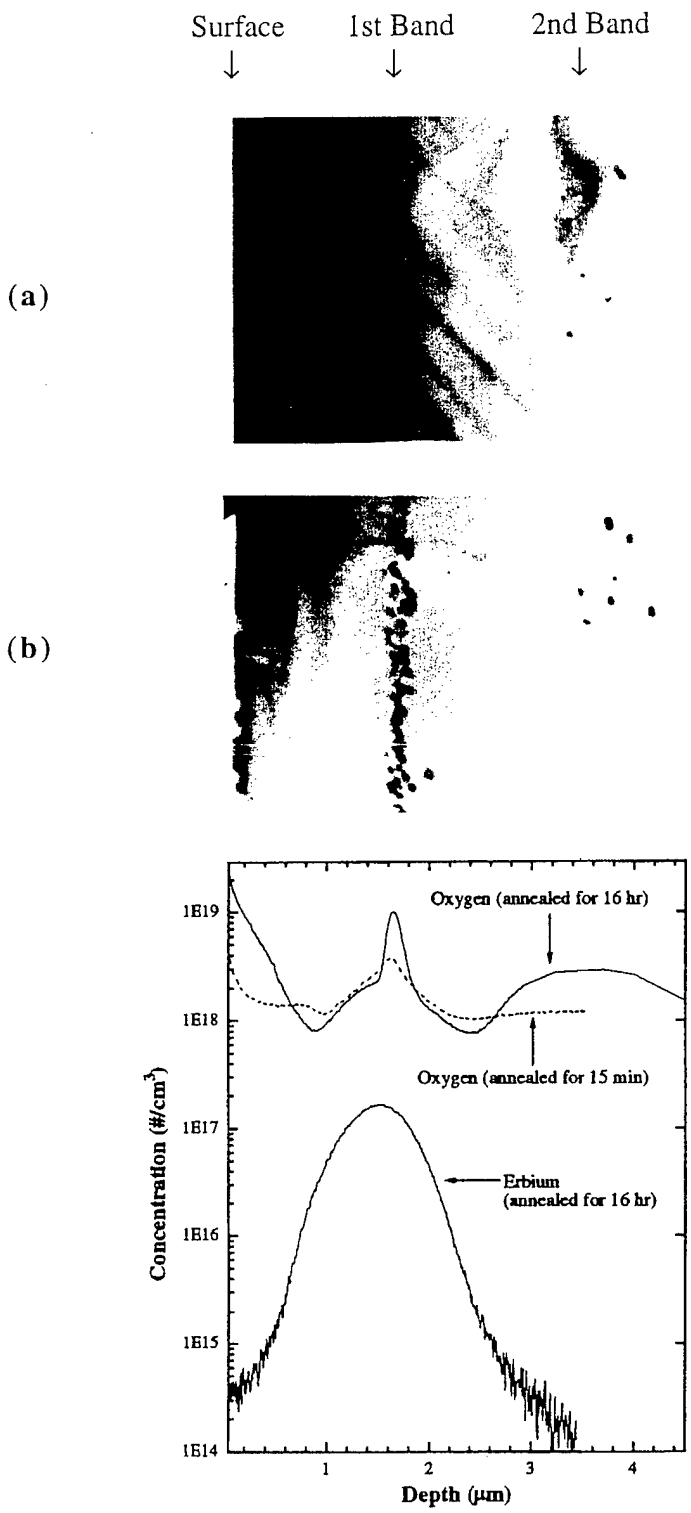


Figure 4.3. XTEM weak beam images taken after annealing at 900°C for 10 hours (a) and 16 hours (b), showing the development of a second loop band in the 4.5 MeV implanted (100)Si; SIMS profiles (c) documenting the segregation of oxygen into both loop bands in (b).

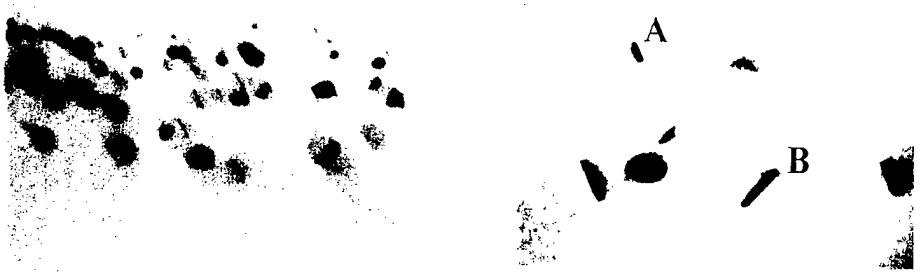
be evaluated from the symmetry of the erbium profile for the same sample annealed at 900°C for 16 hours (Figure 4.3c).

Comparison of the microstructures of the loops in the first loop band for the 4.5 MeV sample annealed at 900°C for a short-term and a long-term is shown in Figure 4.4a and 4.4b, respectively. The TEM contrast of the defects could be influenced by specimen tilting for the short-term annealing sample (Figure 4.4a) indicating that they were dislocation loops. The dislocation loops were identified to be Frank loops on {111} planes with a burgers vector of a/3<111>.

After a long-term, 16 hours annealing at 900°C, a significantly lower density of loop-like defects with much larger size were obtained, as shown in Figure 4.4b. Tilting of the sample showed that the coarsened loops still lay on {111} planes, but were visible in all reflections. The absence of a criterion of $\mathbf{g}\cdot\mathbf{b} = 0$, the absorption contrast at weekly diffraction orientations and the strong inside-outside contrast at Ò **g** are all consistent with these defects being precipitates. These precipitates can be basically divided into two types, as marked "A" and "B" respectively in Figure 4.3b, based on the contrast features for the same reflection. The small "A" type precipitates have a size of 250 Å, located in slightly shallow layers, while the larger "B" type precipitates have a size range between 500 - 600 Å, distributed at the bottom of the band.

Figure 4.5 represents a HRTEM image of a typical small "A" type precipitate (Figure 4.4b) along <011> in which the platelet image can be seen edge on. The precipitate took a platelet morphology with a habit plane of {111} and with a thickness normal to the plane below 10 Å. The structure of the precipitate is identical to the HRTEM image of Er precipitates reported in the Er implanted Si[11] which were believed to be $ErSi_2$. The coherent $ErSi_2$ has a hexagonal crystal structure and aligned with its [0001] axis parallel to <111> Si[12].

A HRTEM image of an isolated, typical larger "B" type precipitates (Figure 4.4b), revealed that the type of precipitates grew on {111} plane as displayed in Figure 4.6. Considering the evidence of segregation of oxygen into the loop area (Figure 4.3) and the identical shape between the primary loops (Figure 4.4a) and the final precipitates (Figure 4.4b), the "B" type precipitates were most likely oxygen precipitates, might be derived from oxygen precipitation and evolved from the Frank stacking faults. The nucleation of oxygen precipitates took place heterogeneously on existing dislocation loops which acted as a sink for oxygen interstitials.



(a) (b)

Figure 4.4. XTEM weak beam images, showing the different defects features in the 4.5 MeV implanted samples annealed at 900 °C for 30 minutes (a) and 16 hours (b).

Figure 4.5. HRTEM image of the platelet $ErSi_2$ precipitates observed from the <011> direction in the 4.5 MeV implanted (100)Si after annealing at 900°C for 16 hours. The $ErSi_2$ phase has a habit plane of {111}.

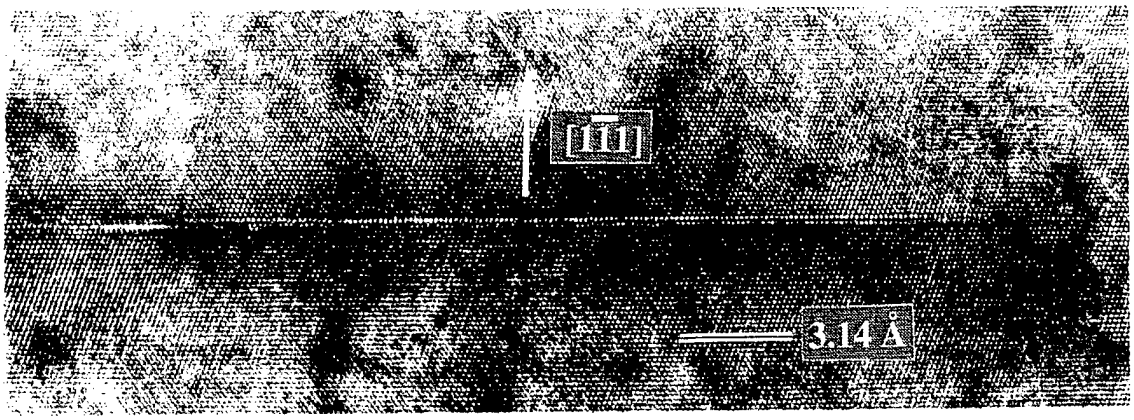


Figure 4.6. HRTEM image along <011> showing the plate-like oxygen precipitate on the{111} plane formed after annealing for 16 hours in the 4.5 MeV implanted sample.

4.4 Conclusions

A defect-free material was observed in the 400 KeV implanted sample annealed for 30 min. At 800 and 900°C. In sharp contrast, a variety of secondary defects consisting of dislocations, dislocation loops and precipitates are induced upon annealing in the 4.5 MeV Er/O implanted Si; The defects grew in size and distributed in a deeper layer as the temperature was increased. During the isothermal annealing at 900°C, as the primary dislocation loop zone shrank with an increased annealing time, a second loop zone formed in a deeper layer in the 4.5 MeV implanted samples. The oxygen tended to segregate into the dislocation loop zones, where platelet precipitates with habit planes of {111} were found during long-term annealing in the 4.5 MeV implants. Upon dissociating oxygen from erbium, platelet-like Er precipitates generated in the 4.5 MeV implants which were, most likely, $ErSi_2$ with a habit plane of {111}.

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Chapter 5

Properties of Ion Implanted and UHV-CVD Grown Si:Er

5.1 Introduction

Erbium-doped silicon has held the promise for silicon based optoelectronics since the first report of Er luminescence in 1983[1]. However, temperature quenching of luminescence is limiting the output power of Er:Si light emitting diodes at room temperature well below that needed for commercial devices [2]. Current research is focusing on two solutions to the problem; improving the processing of erbium-doped single crystalline silicon, or introducing erbium into other types of materials compatible with Si processing. These materials include amorphous Si, oxygen rich poly-Si(SIPOS), Si nanocrystals, and silicon based alloys [3]. This paper will deal exclusively with the single crystalline Si.

There are several points that need to be addressed in any Er-doped single crystal processing. In order to have strong luminescence, large amounts of optically active Er must be incorporated into the silicon lattice. Xie [4] has estimated that 10^{19} Er atoms/cm^3 are needed for device applications, which is approximately two orders of magnitude higher than the solubility limit. Ligands, which have been found to increase luminescence [5], also need to be incorporated around the erbium. This means that low thermal budget processes should be used to avoid precipitation and out diffusion of the ligands [6]. Damage caused by the introduction of the erbium complex must also be minimized to prevent non-radiative recombination pathways which reduce the pumping efficiency.

Several techniques have been used to incorporate Er into silicon [7-10], but ion implantation has, to date, received the most attention due to IC-processing compatibility. Early work employed high energy implantation (~4MeV) to achieve high doses of Er.

Anneals at 900° C for 30 minutes after the implant maximized luminescence by healing the implantation damage. At longer times, however, ligand out-diffusion dominates, and the luminescence is reduced. We have examined lower energy implantation (400 keV) and UHV-CVD in an attempt to reduce or eliminate damage and suppress the erbium complex dissociation.

5.2 Experiment

5.2.1 Ion Implantation

A standard ion implanter at an energy of 200 keV with doubly charged Er was used to make 400 keV erbium implants in Si (100) boron-doped substrates . Oxygen was co-implanted to overlap the peak concentration of the erbium. Processing studies were done to determine the optimum annealing schedule. Spreading resistance measurements, cross-sectional TEM, and secondary ion mass spectroscopy (SIMS) were used to characterize the material.

5.2.2 UHV-CVD

A hot wall UHV-CVD system was used to grow Er-doped Si (Figure 5.1). The reactor chamber is pumped by a turbomolecular pump which has a base pressure of $5x10^{-9}$ Torr. Partial pressures of oxidizing species such as water and oxygen are roughly $1x10^{-10}$ Torr. The process gases used are silane (SiH_4), 1% phosphine in H_2, 1% diborane in H_2, and H_2 as a carrier for the erbium metallorganic source. Two erbium sources were examined in this study; $Er(TMHD)_3$ and $Er(FOD)_3$ (Figure 5.2). The $Er(FOD)_3$ was loaded into a vacuum tight bubbler located in a dedicated furnace which sat in the gas delivery system. Temperature could be controlled to within 1°. A mass flow controller regulated the amount of hydrogen that flowed through the bubbler. For growth runs using $Er(TMHD)_3$, however, the powder was loaded directly into the chamber after initial growth of silicon. Coarse temperature regulation was maintained by the reactor's furnace as well as heating tapes.

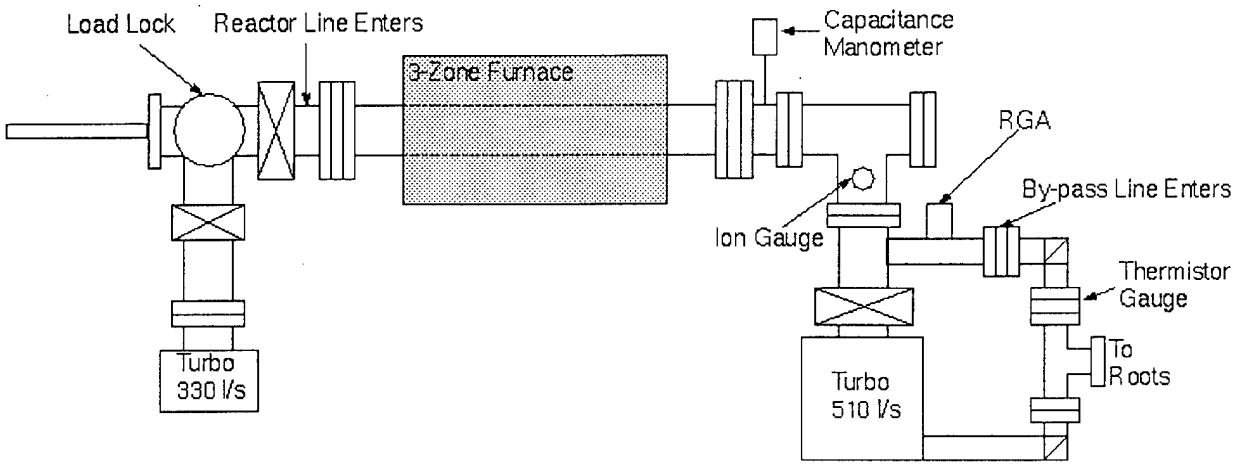

Figure 5.1. UHV-CVD reactor used in this experiment. The Er source either sits just inside the gate valve, or in the bubbler located in the gas manifold system.

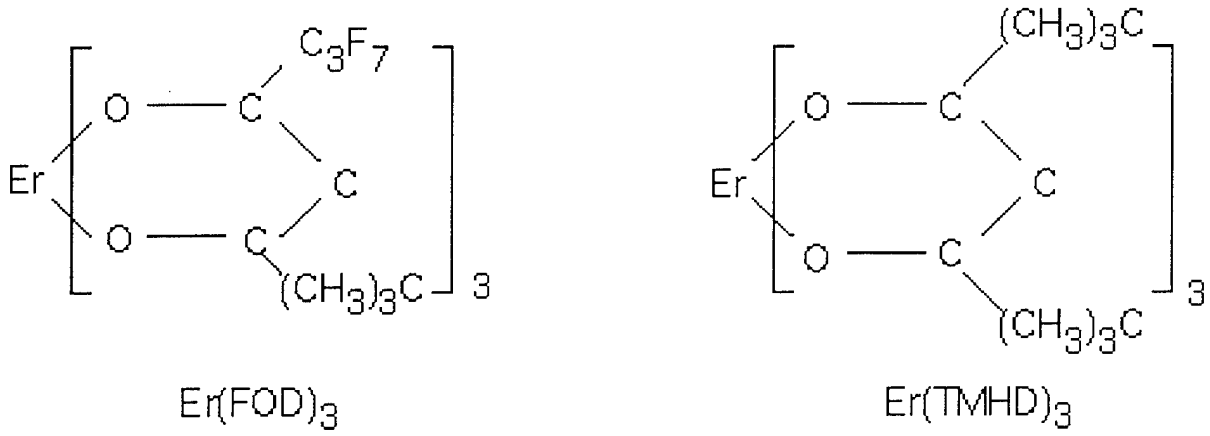

Figure 5.2. Structure of precursors used in this study. Each erbium is surrounded by 6 oxygen in the molecules. The $Er(FOD)_3$ can also contribute fluorine to the ligand field of erbium.

All samples were 100 mm Si (100) wafers. Although the system can handle 20 wafers at a time, only 4-5 wafers were loaded per run. They were cleaned in a hot piranha

solution for 10 minutes, then given an HF dip for 15 seconds before being transferred into the loadlock. Once the pressure had dropped to $1x10^{-6}$ Torr, the wafers were loaded into the reactor, where growth was initiated immediately. In all samples a doped buffer silicon film was grown prior to the Er-doped film. In some cases a complementary doped film was grown on top of the Er film to make a junction.

Growth temperatures were between 550 and 620° C, with run times varying from 30 minutes to 4 hours. SIMS and photoluminescence (PL) were used to characterize the films. The PL setup consisted of an Ar^+ laser, He cooled cryostat, spectrometer, and a liquid nitrogen cooled germanium detector. Standard lock-in techniques were used to improve the signal-to-noise ratio.

5.3 Results

Low energy implanted samples were annealed in an Ar ambient at 800, 900, and 1000° C for different times to determine the optimum PL. The best anneals were those done at 800° C for 30 minutes, which is lower in temperature than that required for the high energy implants. Cross-sectional TEM done after the anneal does not show any end-of-range secondary defect structure prevalent after high energy implantation. The internal quantum efficiency was three times higher than the high energy implanted samples. Spreading resistance measurements, SIMS, and PL done on low energy implanted Er/O annealed at different temperatures strongly suggest that this could be due to the number of electrically active donors that are created and survive to the end of the process. Figure 5.3 shows typical results of spreading resistance of high energy implants into a p-type Cz silicon wafer (low energy implantation profiles are identical). The carrier concentration was largest at the peak of the erbium implant in samples with both Er and O. Variations in annealing temperatures changed the spatial distribution and integrated concentration of the donors. A linear correlation between PL intensity and integrated donor dose (Figure 5.3) suggests that the luminescent Er centers are those which are in the electrically active Er/O donor state. The maximum PL comes from the sample with the highest integrated donor density which was annealed at the lowest temperature.

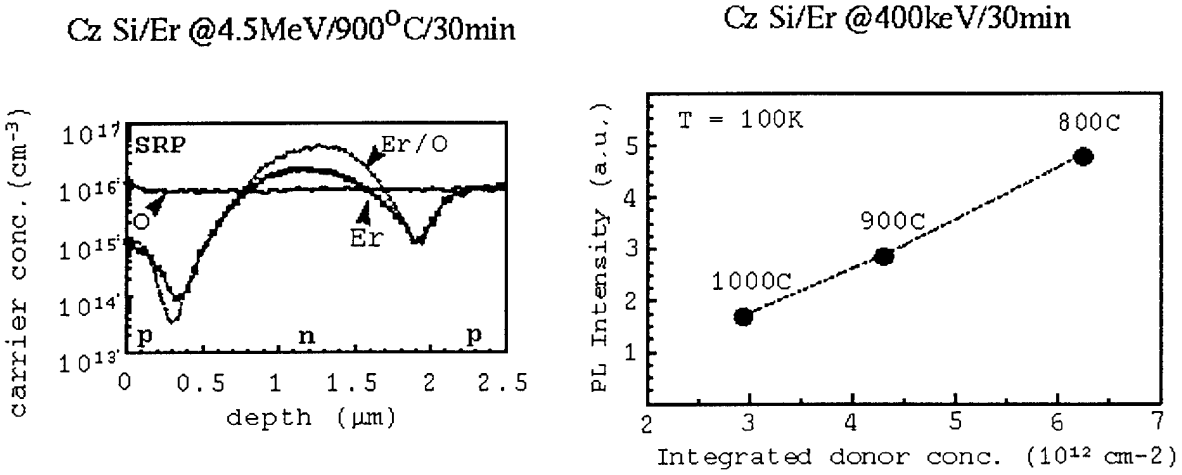

Figure 5.3 Spreading Resistance measurements of Er/O high energy implanted sample (left) show a maximum concentration near the projected range of the Er implant. This behavior is identical to low energy implants. By varying the annealing temperature, the donor distribution and PL intensity can be maximized.

Films grown by UHV-CVD were also examined by PL. Spectra of samples grown by both precursors are shown in Figure 5.4. The $Er(TMHD)_3$ sample has a spectrum similar to some high dose Er/O implanted samples, with one major peak at 1.537 μm. The $Er(FOD)_3$ spectrum clearly looks different with a broad higher energy background and an additional sharp peak at 1.54 μm. A broad background has also been seen in samples with high doses of fluorine in Er/F implants, suggesting the fluorine is the cause of the feature. A PL spectrum from a reference sample of ErF_3 powder was compared with this PL but no match for the sharp peak at 1.54 μm could be found. Further studies on these samples to determine the local environment are in progress.

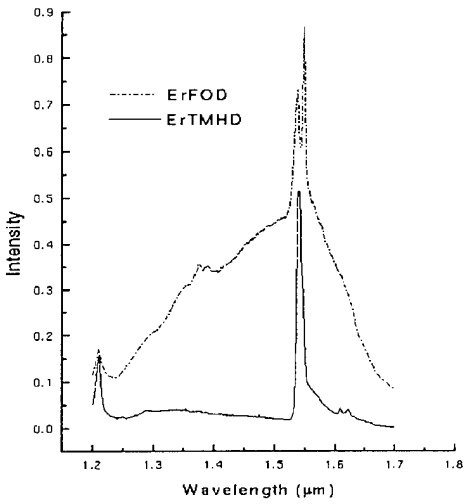

Figure 5.4. PL at 4 K with Ar^+ laser (488nm). doped

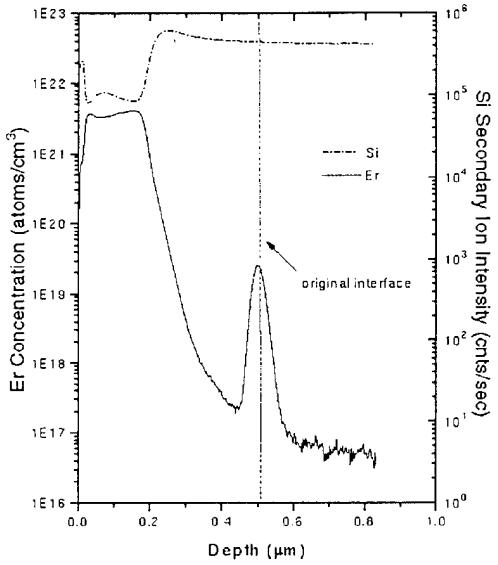

Figure 5.5. SIMS of Er:Si film with $Er(TMHD)_3$

SIMS was done on $Er(TMHD)_3$ samples to see how the molecule was being incorporated into the film. A representative sample is shown in Figure 5.5. The film has a concentration $4x10^{21}$ Er/cm^3 which is too high for good silicon film quality as the erbium adds strain to the lattice. This concentration is not unexpected as the control over Er flux in these samples was poor. Oxygen was incorporated in such high concentrations (>15%) that no quantitative figure could be given. Carbon reached levels of $10^{20}/cm^3$ as well, which has previously been a problem in a similar system [9] . This clearly shows that the precursor flux was too high. Erbium concentrations nearly 100 times lower are desired to have higher crystalline perfection and lower 'impurity' levels from other molecule fragments. The SIMS also shows that contamination from previous runs using this method of delivery is a significant problem, as the original interface has nearly monolayer coverages of precursor fragments.

Due to the high oxygen content in the films, it was possible that Er was incorporated into SiO_2 instead of Si. If that was the case then the PL would only be due to optical

pumping of the erbium. We varied the pump frequency of the Ar^+ laser and monitored the intensity of the 1.537 μm line, as seen in Figure 5.6. For convenience, PL of Er_2O_3 powder is included to show optical pumping behavior. The two vertical lines in the figure mark higher excited levels in the Er manifold which can be directly pumped. Samples grown from the two precursors do not show a response indicating optical pumping, meaning that photogenerated carriers must play a role in the excitation of the erbium.

A comparison of external quantum efficiencies was made among the high and low energy implants, as well as the CVD grown material. All samples were measured at 4 K at a power in which the material was in the linear regime. After normalizing for different pump powers and filters, and integrating the PL features due to Er, relative external quantum efficiencies were made. The UHV-CVD material doped with $Er(TMHD)_3$ was normalized to one. Under these conditions, the high energy implanted material was 35 times more efficient than the CVD material and twice as efficient as low energy implanted material. It must be re-emphasized that low energy implants had a higher quantum efficiency in electroluminescence at 100 K (not reported in this work). The low efficiency of the CVD material is not unexpected due to the quality the initial films.

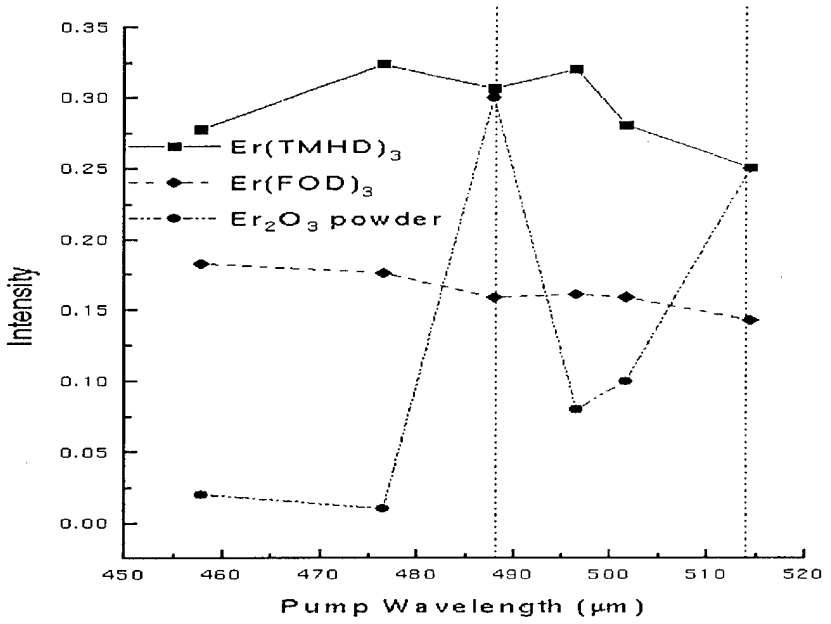

Figure 5.6 Intensity of 1.537 μm line as a function of excitation pump wavelength.

5.4 Conclusions

Low energy ion implantation has improved the crystalline quality of Er-doped silicon. This allows for lower annealing temperatures for lattice recovery and a more stable ligand environment for the Er. A corresponding increase in the quantum efficiency has been correlated to the integrated donor concentration of Er/O states. Even lower processing temperatures have been used in UHV-CVD to further stabilize the Er/ligand complex since no damage is created which needs high temperature recovery. Initial Er-doped films have shown strong luminescence but the incorporation rate has not been controlled enough for high crystal quality. Relative external quantum efficiencies of CVD grown films are about an order of magnitude below that of implanted material, but it is expected to increase once the Er concentration is reduced.

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Chapter 6

Low-Loss Polycrystalline Silicon Waveguides For Silicon Photonics

6.1 Introduction

Silicon photonic circuits are an attractive alternative for the future generations of microprocessors, since one can couple standard electronics with on-chip optical interconnects for information transfer and clock distribution. These interconnects offer the possibility of minimal crosstalk, low power dissipation and high speed data transfer. Since crosstalk and power consumption are greatly reduced, higher interconnection densities are achievable. Small propagation delays and load independent design allow minimization of clock skew.

Polycrystalline silicon (polySi) is a part of VLSI silicon processing technology being used for gate, source and drain contacts in CMOS structures and resistors and bipolar transistor emitters. Additionally, polySi has been considered for several applications where single crystallinity may be desirable, for example, Thin Film Transistors (TFTs) [2, 7, 10]. The main reason for the use of polySi is its ease of deposition in Low Pressure Chemical Vapor Deposition (LPCVD) furnaces on a variety of substrates.

Here we propose the use of polySi waveguides for optical interconnects. In comparison with Bonded and Etched Back Silicon On Insulator (BESOI) or Separation by IMplantation of OXygen (SIMOX), polySi waveguides permit more design flexibility since they are easier to fabricate and allow for multilevels of interconnection. They also offer the possibility of a wider range of cladding and core thicknesses. For example, one can adjust the SiO_2 cladding thickness easily unlike in SIMOX waveguides and one can vary the polySi core thickness easily unlike in BESOI waveguides. Therefore, although strip-waveguide structures using silicon-on-insulator (SOI) technology yield low cut-back losses of 1dB/cm [3] and Mach-Zehnder waveguide interferometers [11] in SOI material with insertion losses of 4.81dB have been demonstrated, polySi is preferred for the implementation of silicon optical interconnections.

In comparison with the Si_3N_4/SiO_2 waveguiding system, the polySi/SiO_2

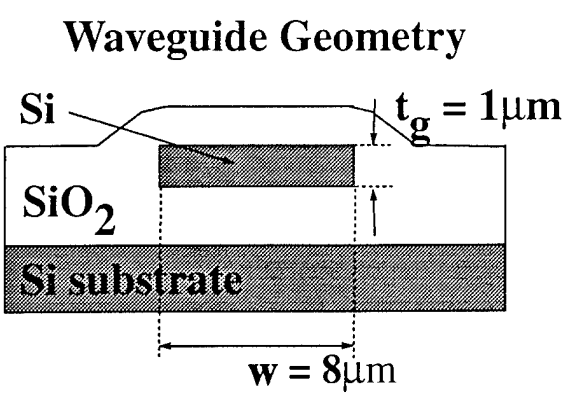

Figure 6.1: *The experimental strip waveguide structure used to measure transmission losses at λ=1.54μmin polySi.*

system confines light better because of its higher dielectric contrast. Single-mode waveguides require much smaller cross-sectional dimensions ($1\mu m^2$ compared to $1000\mu m^2$) and become possible due to the higher dielectric contrast of the polySi/SiO_2 system. However, just as carrier scattering and recombination contribute to losses in polySi electronic devices (for example TFTs), thereby leading to lower mobilities and gain, photon scattering and absorption losses limit the performance of photonic devices such as waveguides. In this work we evaluate the material properties of polySi in an attempt to lower the optical transmission losses measured in polySi strip waveguides. Materials characterization tools have been applied to define the contribution of the grains and grain boundaries to bulk scattering and absorption losses and to investigate the impact of film roughness on surface scattering losses.

6.2 Fabrication of the waveguides

LPCVD polySi films were deposited at 625°C and amorphous silicon films were deposited at 560°C and 580°C. The films were 1μm thick and were deposited on 3μm Low Temperature Oxide (LTO) on p-type silicon substrates. All the wafers were subsequently annealed for 16 hours at 600°C, to recrystallize the amorphous silicon. The wafers are labeled as 560, 580 and 625. One of the 625 polySi wafers was Chemo-Mechanically Polished (CMP) for 30 seconds on a WESTECH 372 polishing machine and is referred to as 625 CMP. The 560, 580, 625 and 625 CMP polySi wafers were patterned to obtain strip waveguides of width 8μm.

Figure 6.1 shows a schematic of the strip waveguide structure fabricated for measuring transmission losses at λ=1.54μm in polySi.

A blanket layer of 0.4μm LTO was deposited on the patterned waveguide as the top cladding layer to protect the waveguide surface during facet polishing. Unpatterned wafers were used for materials characterization. Both patterned and unpatterned wafers were then hydrogenated in an Electron-Cyclotron Res-

onance (ECR) plasma chamber at 600W power, 0.16mT operating pressure and 350°C temperature for 40 minutes.

Optical losses were obtained for the transmission of λ=1.54μm light through waveguides of lengths 2mm and 3mm. The output power is assumed to decrease exponentially with the length according to equation 6.1

$$P_1 = P_0 \exp(-\alpha l_1), \tag{6.1}$$

where α is the loss coefficient, P_1 is the output power from length l_1 and P_0 is the power injected into the waveguide. Transmission losses in the waveguide are isolated from the coupling losses by a cutback technique. The cutback technique involves taking the ratio of output power from length l_1 to that from length l_2, given by equation 6.2,

$$\frac{P_1}{P_2} = \exp[-\alpha(l_1 - l_2)], \tag{6.2}$$

to determine α [5], the loss coefficient. We measure a $\pm$3% variation in coupling efficiency for the waveguides and project a $\pm$5% error on the measured values of α.

RMS surface roughness was measured using tapping mode AFM. Measurement of reflectance using a CARY 5E spectrophotometer was used to confirm the results of the AFM. At λ=280nm optical transitions at the X point of the Brillouin zone causes a pronounced maximum in the reflectance of single crystal Si. A comparison of surface reflectance spectra from various types of polySi yield both, qualitative and quantitative information about roughness.

Cross-sectional and plan-view TEM images were used to determine the grain structure and size. For estimation of grain size we used two techniques, a line techinque [8, 4] and an area technique [1].

6.3 Transmission and absorption losses

A cutback loss measurement of the 625 polySi yielded 77dB/cm, consistent with previous measurements [3]. Loss mechanisms are scattering by the rough polySi surfaces, bulk scattering and/or absorption within the grains and grain boundaries. For 625, an RMS surface roughness of 20nm was obtained from the AFM measurement. Figure 6.2 shows the surface reflectance of several polySi samples as a function of wavelength in the UV regime. The reflectance from 625 and 580 is very low compared to that from single crystalline silicon in the entire UV regime. At λ=280nm the specular reflectance from 560 approaches that of polished single crystal Si. 625 CMP shows an increase in reflectance from a mere 10% to about 35%.

The bulk absorption and scattering phenomena depend on intrinsic properties of the polySi. Cross-sectional TEM (XTEM) images of 625 are compared

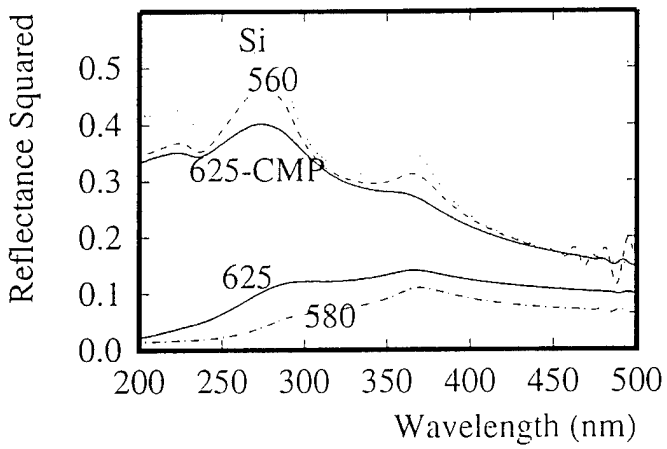

Figure 6.2: *Specular reflectance as a function of wavelength for several polySi samples. Also shown for reference are the positions of the reflectance peaks expected from a smooth surface such as a polished silicon wafer.*

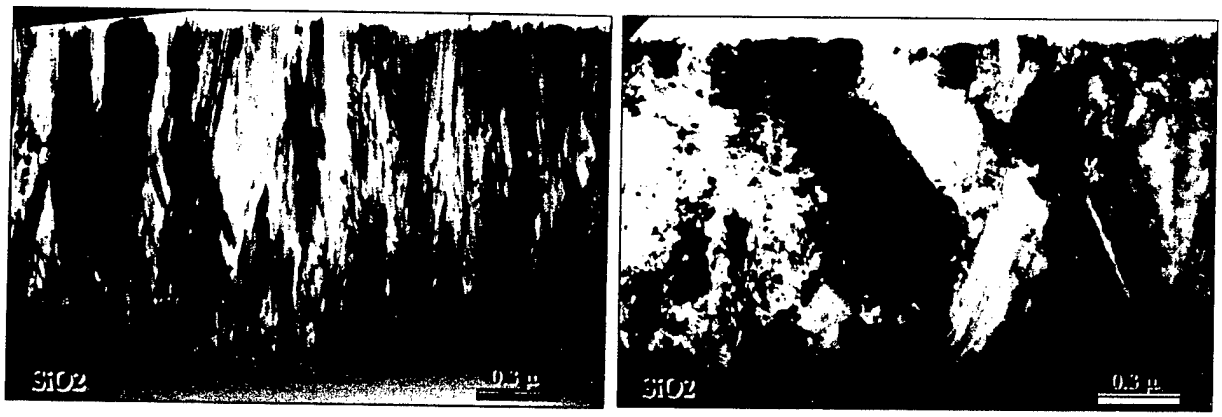

Figure 6.3: *Cross-sectional TEM images of 625°C (LHS) polySi and 560°C (RHS) recrystallized polySi.*

to those from 560 in Figure 6.3. The mean grain sizes are 0.18μm and 0.40μm, respectively. The small, columnar grains of 625 are structurally different from the larger non-columnar grains in 560. Table 6.1 summarizes the losses measured following different processing steps.

Table 6.1: *Measured and calculated losses in polySi waveguides as a function of processing conditions. (Error margins in loss measurements are ±5%).*

Sample Label	RMS roughness	Grain Size	Measured Loss	Calculated Surface Loss	Bulk Loss
	AFM (nm)	μm	dB/cm	dB/cm	dB/cm
560	3.7	0.40	37	1.5	35.5
560 ECR	3.7	0.40	15	1.5	13.5
580	14.9	0.25	71	24.0	47.0
625	20.1	0.18	77	43.6	33.4
625 CMP	6.8	0.18	35	5.0	30
625 CMP+ECR	6.8	0.18	16	5.0	11.0

Theoretical surface scattering losses calculated using an analysis developed by Tien [9] and detailed elsewhere [3] are also listed in the Table for easy reference. Most importantly, a comparison of the measured cutback losses between 625 CMP and 625 waveguides enables us to better differentiate between surface and bulk losses. The grain structure of the samples is the same but the surface is smoothed from 20.1nm in 625 to an RMS roughness of 6.8nm in 625 CMP.

The bulk loss of the 625 and 625 CMP samples are similar, corroborating the impact of surface roughness which contributes approximately 40dB/cm of loss. The surface roughness of 560 is about half of 625 CMP, and the grain size is about twice as large. Both of these factors should intuitively yield lower losses in 560 compared to 625 CMP. However the loss of 35dB/cm in 625 CMP is surprisingly close to the 37dB/cm loss measured in 560 waveguides, which indicates an apparent independence of measured loss on grain size. Following surface roughness reduction in 625 by CMP, the grain size independence on loss was further confirmed when hydrogenation of 560 and 625 CMP yielded similar loss values.

Figure 6.4(a) shows the dependence of grain size on deposition temperature and Figure 6.4(b) shows the bulk loss versus grain size. The figure shows that although grain size is larger for 560, the bulk loss is not strongly dependent on grain size in the 0.1μm to 0.4μm regime. Further investigation of losses for very large and very small grained polySi is planned. Also, residual-loss sources, such as from grain structure and orientation, degree of crystallinity,

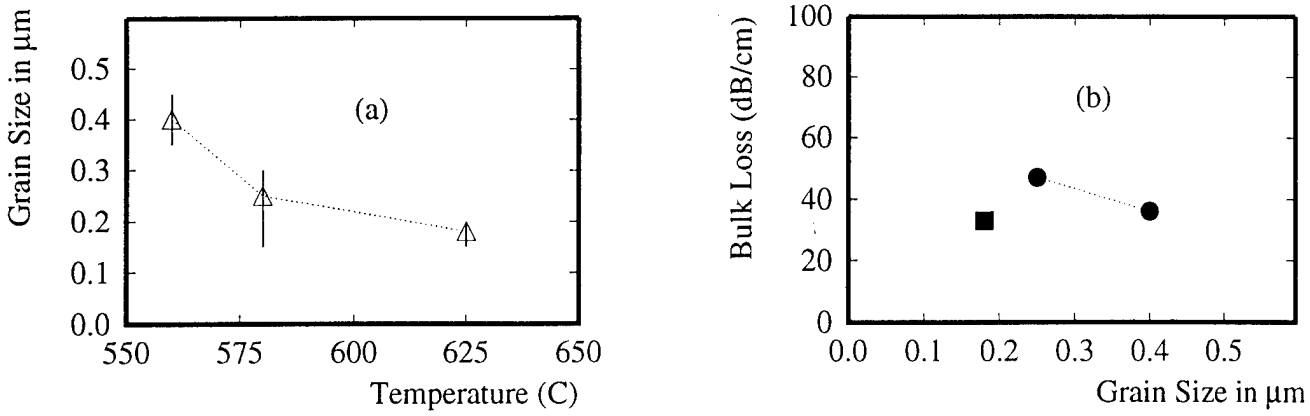

Figure 6.4: *Grain size in polySi as a function of deposition temperature (a) and bulk loss as a function of grain size (b).*

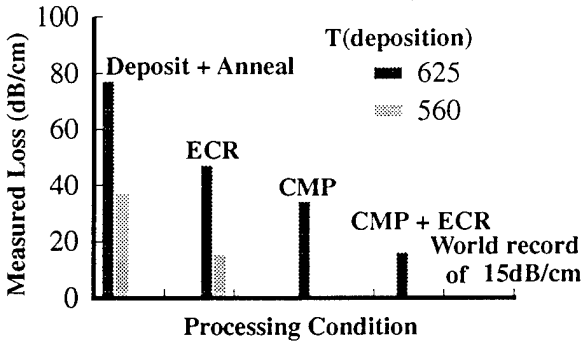

Figure 6.5: *A histogram summarizing the measured losses for* SiO_2*-clad, 8*μm *wide polySi strip waveguides at* λ*=1.54*μm.

film stress, and intra-grain defects, are currently being investigated.

6.4 Conclusions

A histogram which summarizes the measured loss as a function of processing condition for 625 and 560 polySi is shown in Figure 6.5. The loss in the as-annealed case is lower for 560 than 625. Loss measured in 625 CMP is similar to loss measured in 560 indicating the independence of grain size on losses. Additionally, this result shows that the surface scattering mechanism contributes a loss of about 40dB/cm for 625. The subsequent hydrogenation of both of these samples yields the lowest reported polySi loss values at a wavelength of 1.54μm of about 15dB/cm. The lowest value reported previously was 350dB/cm [6].

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Chapter 7

Small Radius Bends And Large Angle Splitters in SOI Waveguides

7.1 SOI Materials for waveguides

Several technologies exist for the manufacture of SOI materials. These technologies include SIMOX (separation by implantation of oxygen), BESOI (bond and etch back silicon on insulator), and Ultrabond (bonded wafers separated with hydrogen implants). Additionally, we have developed polycrystalline Si (polySi) as a lightguiding material [1, 2]. This paper compares the capabilities of the different SOI technologies for providing the required layer quality and thickness required for low-loss light guiding. Measurements of waveguides manufactured from the Ultrabond and polySi materials are presented.

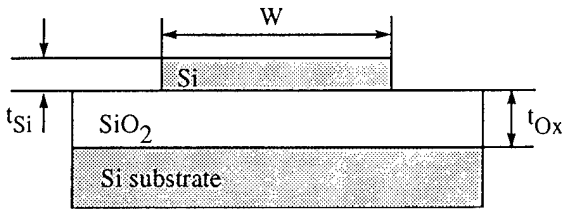

Figure 7.1: Cross-section of strip waveguide. t_{Si} is the guiding Si layer thickness, t_{ox} is the oxide thickness, w is the waveguide width.

7.1.1 Metrics for SOI substrates

The waveguides we are considering here are all of the strip configuration (see Figure 1). The requirements for low loss propagation in these structures are low doping in the guiding layer, adequate SiO_2 thickness (t_{ox}) to provide separation between the guiding layer and the substrate, thin Si thickness (t_{Si}) to allow single mode operation, high crystalline quality of the guiding layer, and low surface roughness to limit scattering. Table 1 summarizes the capabilities of the various SOI technologies in light of these metrics.

Substrate	t_{Si} (μm)	t_{ox} (μm)	N_c (cm^{-3})	N_{def} (cm^{-2})
SIMOX	0.2	<0.45	10^{15}	10^5
BESOI	>1.0	>1.0	10^{18}	—
Ultrabond	0.2	>1.0	10^{15}	10^5
PolySi	0.2	>1.0	—	poly

Table 7.1: Summary of SOI technology capabilities as substrates for Si strip waveguides. t_{Si} is the Si thickness, t_{ox} is the oxide thickness, N_c is the carrier concentration, and N_{def} is the defect concentration.

Free carrier absorption depends on doping levels and wavelength. At λ=1.54μm, doping levels must be kept low to inhibit losses to free carriers in the waveguides. To limit the loss to 1dB/cm, the required free carrier concentration cannot be above $\approx 10^{17}cm^{-3}$ [3]. Because of the etch-stop layer used for BESOI, it is difficult to achieve these low dopant levels.

For single mode operation, a guiding layer thickness (t_{Si}) of approximately 0.2μm is required. This layer thickness is easily achieved with SIMOX, Ultrabond, or polySi materials, but with BESOI layer uniformity is compromised with such thin silicon layers. Plasma etching can be used to precisely thin the BESOI, but these methods are prohibitively expensive.

The waveguide loss for single mode strip waveguides is a strong function of buried oxide thickness. This loss occurs because there is always an evanescent tail of the guided mode extending into the oxide. This tail allows the mode to leak into the high index substrate. Oxide thickness > 0.7μm is required to keep the waveguide losses lower than 1.0dB/cm [4]. Oxides of this thickness are readily achieved with all of the technologies with the exception of SIMOX, which is limited to approximately 0.45μm of oxide. The current trend with SIMOX is to improve the quality of thinner oxide layers and it is not obvious that any move toward thicker oxides will occur.

Crystalline quality in SIMOX, BESOI, and Ultrabond can be quite high. In SIMOX and Ultrabond the quality is reduced due to implantation induced defects. Defect concentrations of $10^5 cm^{-2}$ have been reported in both materials [5]. It is not obvious that this level of imperfection will have a significant impact on waveguide loss. PolySi can be considered highly defective crystalline material and these defects have been measured to contribute between 15 and 35 dB/cm depending on preparation conditions [1, 2].

The quality of the surfaces is critical in this high index contrast system. Surface roughness of 20nm rms has been shown to contribute 35dB/cm in polySi guides [1]. For all of the devices here, surface quality can usually be controlled to 3nm rms using chemical mechanical polishing (CMP). For the polySi waveguides, the roughness can also be controlled by depositing amorphous silicon and then annealing it into polySi: this avoids the CMP

step.

Given the above criteria, the most promising materials for submicron waveguides are the Ultrabond material and polySi. These technologies offer thick silicon dioxide layers with thin, uniform silicon layers. Ultrabond has the advantage of being lightly doped and of high crystalline quality. While the crystallinity is lower in the polySi material, it is available in standard silicon processing lines, can be deposited to form multilayer structures, and is a more flexible tool for prototyping.

Starting with the appropriate layer thicknesses (t_{Si}=0.2μm, t_{ox}=1.0μm), waveguides are fabricated using standard silicon processing techniques. These include photolithography and reactive ion etching. For the waveguide loss measurements presented here we use SF_6 to etch the silicon or polySi. The processing requires only one etch step for waveguide fabrication. Waveguides of width 8.0, 4.0, 2.0, and 1.0μm are patterned and are used to evaluate the quality of the guiding layer as well as to evaluate the effects of processing on the waveguide losses. Processed waveguides are then cut with a die saw and the facets are polished in preparation for testing.

7.1.2 Losses in Ultrabond and polycrystalline silicon guides

Loss measurements are determined using the cutback technique. Light from a laser diode is coupled into a waveguide using a conically tipped optical fiber. The throughput of the waveguide is measured. The transmitted power is measured for different waveguide lengths and the waveguide loss is determined using the following relation:

$$\alpha(dB/cm) = 4.343 \frac{1}{l_1 - l_2} ln \frac{P_2}{P_1} \tag{7.1}$$

Cutback measurement results for the Ultrabond and polySi samples processed at MIT are shown in Figure 2.

For large waveguides (w$\geq$4.0μm) the measurement indicates the quality of the bulk material as the the optical mode is confined primarily in the waveguide core. The Ultrabond waveguides show losses of 1dB/cm at these widths. Two different polySi measurements are shown. The first (labelled PolySi) is deposited as amorphous Si at 560°C and then annealed at 600°C for 16hrs to convert the amorphous Si to polySi. The PolySi-H is similar material that has been passivated with hydrogen. The bulk loss for the PolySi-H sample is 15dB/cm and represents the lowest loss reported for polySi waveguides.

As the waveguide width decreases, the optical mode interacts more strongly with the waveguide sidewalls. Imperfections on the sidewalls result in scattering. In this large Δn system the scattering can be large. For w = 1.0μm

Ultrabond guides, losses of 20dB/cm are measured and attributed to scattering from sidewalls. Also shown in Figure 2 is a calculation of loss due to sidewall roughness. This calculation approximates the sidewall imperfection by a periodic grating that couples the guided mode to radiation modes [6]. The trend towards higher loss at smaller width fits the measured trend well. Oscillations in the calculated data are a result of the perfect periodicity of the assumed grating. The sidewall roughness strongly depends on the processing technique and the loss depends on the square of the peak-to-valley roughness.

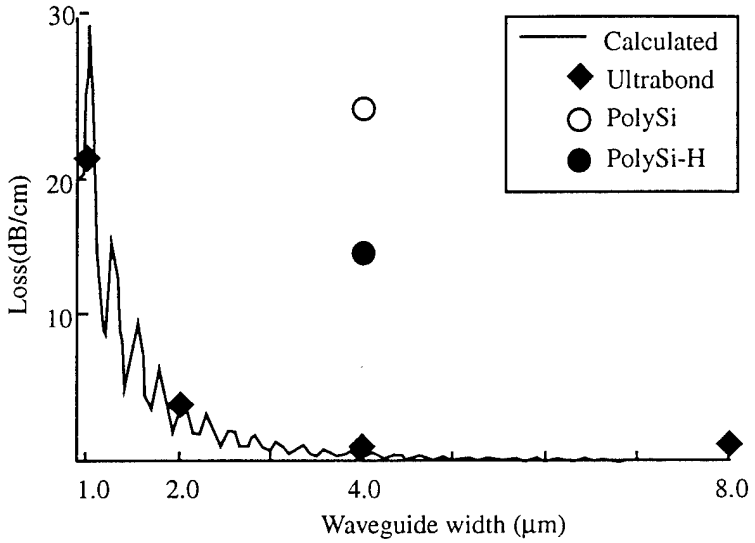

Figure 7.2: Loss measurements for strip guides of different widths. The calculated loss is due to edge roughness only.

7.2 Waveguide bends and splitters

The bend and splitter waveguide devices were processed by Hewlett Packard at their ULSI Laboratory. These samples consist of a 1.0μm deposited oxide on a standard 6" Si wafer. A 0.2μm amorphous Si film was deposited on the oxide at 560°C and then annealed at 900°C for 2 hrs. This HP process is not optimized for polySi waveguides. The waveguides are then patterned and etched using HBr/Cl_2. Bend radii from 1.0 to 100.0μm and Y-branch splitters from 0.5 to 20.0° half-angle were included on the mask. To evaluate the loss in these polySi waveguides, the transmission through a 100.0μm bend sample was compared to that of a straight waveguide sample. The large radius bend was assumed to induce no additional loss. Given the difference in length of the bent and straight guides, a loss of 110dB/cm was measured. This is a large value and does not represent the loss of optimized polySi guides. The fraction of this loss that is due to sidewall roughness is estimated by placing liquid

with n = 1.5 onto the waveguide and measuring the change in throughput as compared to an unclad guide. The scatter loss simulations show that this change in cladding index should result in a factor of 1.6 reduction of the loss in dB/cm. From this comparison we estimate the roughness loss to be 20dB/cm. This indicates a core loss of 90dB/cm which should be reducible to 15dB/cm with appropriate processing [2].

7.2.1 Bend analysis and experimental results

The high index contrast of the SOI material allows the miniaturization of passive waveguide devices such as bends and splitters. Figure 3 shows the calculated dependence of bend loss on radii. Two different methods of calculating bend loss were used, Marcuse's method [7] and Beam Propagation Method (BPM) calculations [4]. For large Δn systems, the BPM methods are required to accurately model the devices. Standard approximations, such as used by Marcuse, rely on small Δn to reduce the complexity of the solutions. Regardless of the method of performing the analysis, the loss associated with bends in these waveguides are always less than 1dB (the loss in dB/cm is multiplied by the bend length to get values in dB).

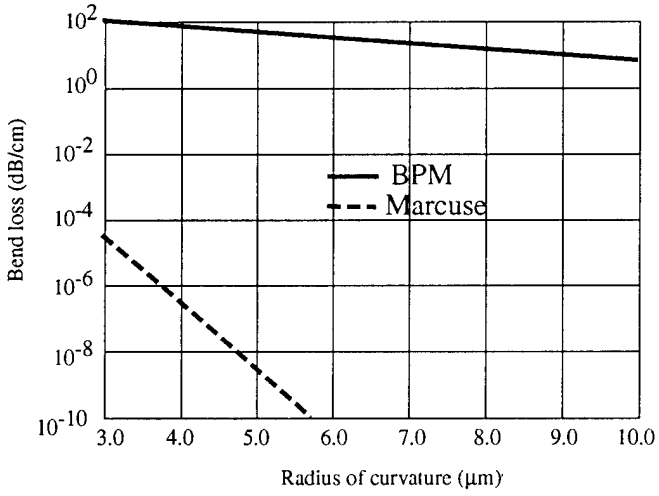

Figure 7.3: Calculated loss due to 90° waveguide bends.

To evaluate the bend losses, transmission through straight waveguides was measured and compared to waveguides with two 90° bends. To extract the bend loss it is necessary to take into account the difference in length of the bent and straight waveguides and remove the loss due to this difference. The data for waveguides with bends from 2.0 to 50.0μm radii is shown in Figure 4. At no point is the loss greater than 1dB, consistent with the calculations. It should be noted that the error bars on these measurements are on the order of 1dB, so no trend should be implied from the reported data. At no point does the bend loss approach 1dB/bend. This level of loss would be easily

detected with the test method used here. These results show that in this high index contrast system, bend radii of only 2.0μm can be used without inducing appreciable loss into the waveguide.

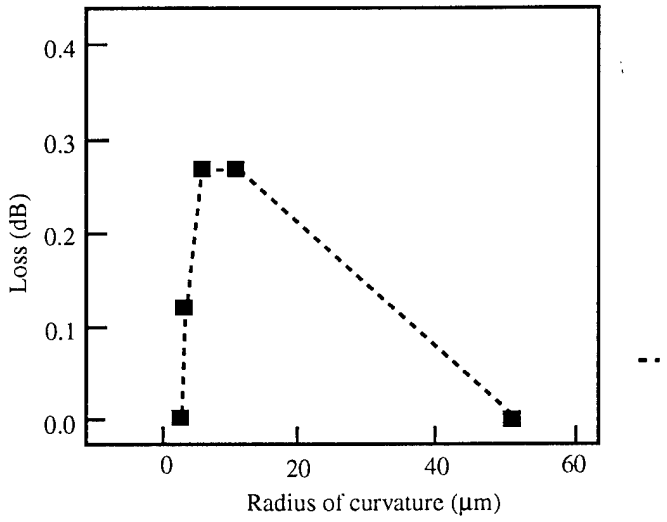

Figure 7.4: Measured loss due to 90° waveguide bends as a function of bend radius.

7.2.2 Splitter analysis and results

Waveguide splitter measurements and analysis have been presented by a number of groups [8, 9, 10]. The data primarily addresses low Δn systems such as SiO_2[8]. Data for these systems show losses of 1dB only if the half-angle of the splitter is kept below 1°. At 1° losses of ≈2.7dB were measured. The effective angle for waveguide splitting is defined as:

$$sin\theta_{eff} = \frac{sin\theta}{\sqrt{n_g^2 - n_s^2}} \tag{7.2}$$

In this relation n_g is the guide effective index and n_s is the substrate index [9]. The denominator on the right hand side is the numerical aperture of the waveguide. The numerical aperture for Si strip guides is ≈2.4 which effectively reduces the splitting angle. For low index contrast guides, the numerical aperture can be less than 1.0, leading to increased effective splitting angles and higher loss for a given angle splitter.

The Y-branch splitter losses are measured by coupling light through a split waveguide and measuring the light output at the two output ports. The sum of the outputs is compared to that of a straight waveguide. Results for splitting angles up to 15° half-angle are shown in Figure 5. Losses are less than 3dB even up to 15° splits, compared to 3dB for 1° splits measured in SiO_2 guides[8]. The losses are expected to depend strongly on the junction geometry, which is

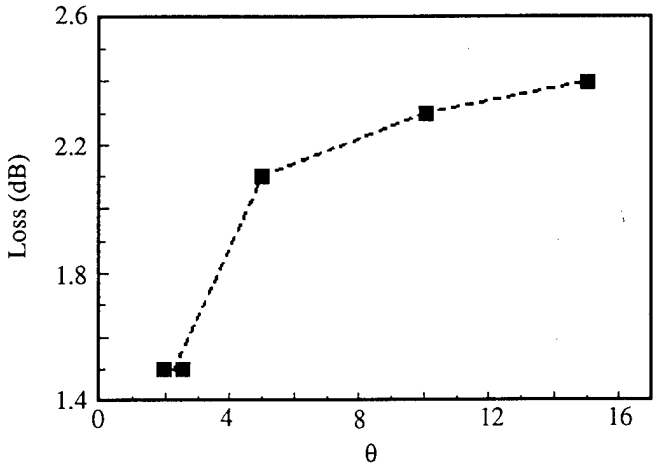

Figure 7.5: Measured loss due Y-branch power splitters as a function of the splitting half-angle.

more difficult to control for these small waveguides. However, because of the high confinement, waveguides need only be separated by 0.2μm before they no longer couple and can be bent away from each other.

7.3 Conclusions

This report contains our preliminary findings on the investigation of small radius bends and high angle splitters in SOI strip waveguides. These waveguides represent a new realm for integrated optics. Bend radii of 2.0μm are possible with losses less than 1dB. Y-branch power splitters with splitting angles of 15° are possible. The real estate required for integrated devices using these waveguide components is greatly reduced compared to more typical III-V or SiO_2 waveguide systems. While the losses here are comparatively large, the reduction in size of the integrated devices lowers the impact of this loss and low insertion losses are still possible. These devices are compatible with standard Si processing and can be considered for optical interconnection applications. Additionally, this technology allows integration of photonic circuits directly with their control electronics. Further work will be done to statistically verify the results presented here and to optimize the performance of the polySi used to manufacture these devices.

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Chapter 8

Polycrystalline Si Waveguides and GeSi Graded Buffer Photodetectors

8.1 Introduction

Each succeeding generation of silicon-based integrated circuits has placed higher demands on interconnection performance. The larger chip sizes, higher clock frequencies, and increased word sizes require high density interconnects. Reliability, cross-talk, power consumption, and clock skew concerns have led to the investigation of integrated optical interconnection architectures. The challenges of optical interconnection require the development of optical components that can be incorporated into Si-based electronics processing. The most fundamental of these components are the waveguide and photodetector. We have investigated the use of polycrystalline silicon (polySi) waveguides and $Si_{0.5}Ge_{0.5}$ relaxed buffer detectors for an integrated optical interconnect technology.

PolySi/SiO_2 waveguides have two important advantages over other waveguide materials systems: superior index contrast and processing flexibility. The Si/SiO_2 material system for on chip waveguiding offers the distinct advantage of high index contrast ($\Delta n=2$) which makes possible submicron waveguide dimensions. Other suggested waveguide materials systems such as glass waveguides or lightly-doped Si layers on Si require large cross sectional dimensions to adequately confine the light. Previous studies have concentrated on the use of SOI (silicon on insulator) material,[1] that utilizes critical wafer area required for electronic devices. The polySi has the unique advantage of permitting the deposition of multiple layers of polySi/SiO_2 and increased processing flexibility in terms of waveguide and cladding dimensions. While polySi films have clear advantages from the fabrication and design perspective, they are more

lossy than single crystalline waveguides because of the additional surface roughness and inter- and intra-grain defects.

Optical interconnect technology based on polySi waveguides requires photodetection at wavelengths longer than the bandedge of silicon. The silicon-germanium materials system is the most promising choice for photodetection at these longer wavelengths. The complete solid solubility and relatively small 4% lattice mismatch make a variety of strained and relaxed epitaxial films possible. Many investigations have been made using strained SiGe films grown directly on Si.[2, 3, 4] These films however are constrained in Ge fraction and thickness by critical thickness limitations.

In recent years, there have been significant improvements in the quality of SiGe relaxed films grown on relaxed buffers.[5, 6] These relaxed $Si_{1-x}Ge_x$ buffers have been shown to have relatively low threading dislocation density (10^4-10^6 cm^{-2}).[7] SiGe relaxed buffers can be used to increase the Ge fraction in the SiGe films used for photodetection at long wavelengths. Figure 8.1 shows the bandgap energy dependence on germanium fraction for relaxed $Si_{1-x}Ge_x$ alloys. Although the range of bandgap energies for SiGe alloys includes 0.95eV (1.3 μm), absorption for photon energies slightly above the bandgap is weak due to the indirect bandgap of all SiGe alloys. A relaxed $Si_{0.5}Ge_{0.5}$ buffer has been used to fabricate a P-I-N photodiode with functionality at λ=1.3 μm.

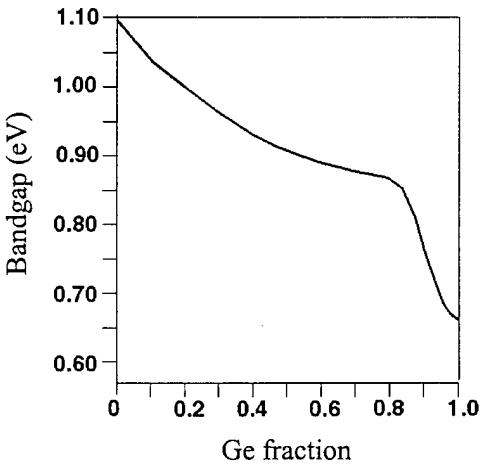

Fig. 8.1. Bandgap of relaxed GeSi alloys.

8.2 Polycrystalline Silicon Waveguides

8.2.1 Waveguide Processing

Low pressure chemical vapor deposition (LPCVD) polySi films were deposited at 625°C and amorphous silicon films were deposited at 560°C on a low temperature oxide (LTO) film of thickness greater than 1μm. All films were subsequently annealed to crystallize the amorphous silicon for 16h at 600°C. The deposited Si films were patterned into strip waveguides as shown in Figure 8.2. Atomic force
microscopy was used to show that the polySi films deposited at 625°C had greater rms surface roughness than the crystallized amorphous films (20.1 nm and 3.7 nm, respectively). Chemical mechanical polishing
(CMP) was used to reduce the surface roughness of the 625°C deposited polySi film to 6.8 nm. An electron-cyclotron resonance (ECR) hydrogen plasma was used to passivate dangling bond defects in the grain boundary region. An 1100°C, 16h anneal was performed on the 560°C deposited polySi in order to eliminate intra-grain defects and crystallize the residual amorphous regions in the material.

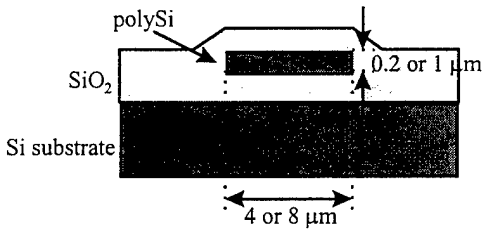

Fig. 8.2: Schematic of polySi waveguide cross section.

8.2.2 Optical Losses in PolySi Waveguides

A cutback technique was used to measure loss in the polySi waveguides. Transmitted 1.33 μm or 1.55 μm light was measured through waveguides of different lengths (1 to 3 mm). We use a laser diode source coupled into a single mode optical fiber which is butt-coupled to the waveguide. A CCD camera is used to image the waveguide output to insure that light has been coupled successfully. A power meter is used to determine transmitted power.

A systematic study of loss at λ=1.55 μm as a function of processing conditions has been reported elsewhere.[8, 9] The (8 μm x 1μm) polySi waveguides deposited at 625°C exhibit the highest loss of 77dB/cm at 1.55 μm; the 560°C deposited polySi losses are considerably lower (35dB/cm). The differences in loss are attributed to the greater surface roughness in the 625°C polySi film. When the rough polySi is chemically mechanically polished before patterning the surface roughness and loss become comparable to the 560°C deposited film. The ECR hydrogen plasma waveguides exhibited even lower losses. Figure 8.3 summarizes the losses at 1.55μm as a function of processing condition. The losses in

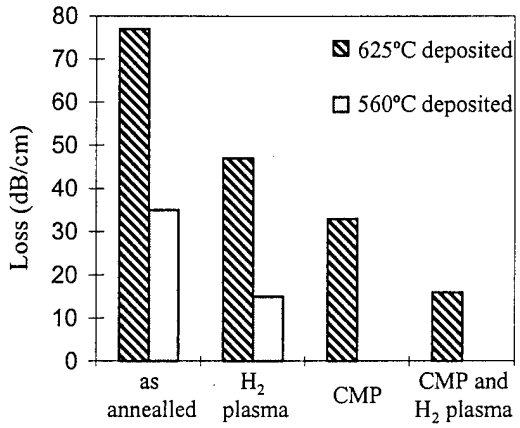

Fig. 8.3: The optical losses in polySi waveguides as a function of processing condition.

the 1100°C annealed polySi waveguides (4 μm x 0.2 μm) at 1.55 μm measured 11 dB/cm. These transmission losses are the lowest ever reported in polySi waveguides. The lower losses of the 1100°C polySi waveguides can in part be attributed to the smaller waveguide dimensions since a smaller fraction of the optical mode is contained in the lossy core. We evaluated the wavelength dependency of the optical power loss in the least lossy waveguides. Optical losses in the ECR hydrogen passivated 560°C deposited polySi and in the 1100°C have been measured. They are 13dB/cm and 16dB/cm at λ = 1.3μm, respectively. These losses for polySi waveguides are reported in Figure 8.4 as a function of wavelength and processing condition. The losses at 1.3μm are comparable to those at 1.55μm given our ±1dB error in our measurement.

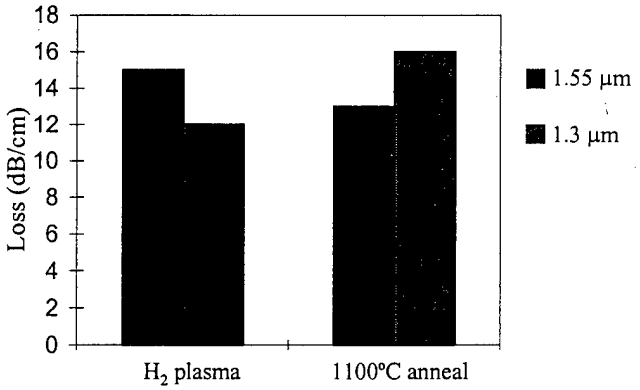

Fig. 8.4: The optical losses in polySi waveguides at 1.3 μm and 1.55μm.

8.3 Relaxed SiGe Photodetector

8.3.1 Processing

The $Si_{0.5}Ge_{0.5}$ graded buffer was grown by UHV-CVD using silane, germane, and diborane as source gases. The $Si_{0.5}Ge_{0.5}$ buffer was grown at 815°C with a grading rate of 10% Ge / μm in 3% Ge steps. The entire graded region and 1μm of the relaxed buffer cap was *in-situ* doped with boron at a concentration of approximately $10^{18}cm^{-3}$. An intrinsic cap of 3 μm was then grown at 610°C. To complete the P-I-N junction we used a 90 min. $POCl_3$ diffusion at 925°C to create an n^+ region. Spreading resistance analysis showed that the phosphorous diffusion created a 2 μm heavily doped ($\sim 10^{20}cm^{-3}$) cap, consuming much of the intrinsic region of the structure. Devices were formed by mesa etching down to the p^+ layer and depositing 2500Å of low temperature oxide (LTO). After opening contact holes in the oxide, Al was deposited, patterned, and sintered. The aluminum was patterned in a fingered structure to allow surface illumination of the detector.

8.3.2 Carrier Collection Efficiency

Carrier collection efficiency was measured using electron beam induced current (EBIC) on the unpatterened P-I-N material. For low acceleration voltages (< 20 kV) we measured the sample current using a current amplifier and a lock-in technique, at higher voltages

either the lock-in technique was used or the sample current was directly determined using a picoampmeter. The collection efficiency, η_{cc}, was determined by taking the ratio of the sample current, I_p, to the rate at which carriers are created in the sample, $I_{created}$:

$$I_{created} = \frac{I_b E(1-f)}{E_{eh}} \tag{8.1}$$

where I_b is the electron beam current, E is the electron beam energy, f is the reflected power (f = 0.08) and E_{eh} (3.2eV) is the energy it takes to ionize an electron-hole pair.[10] The penetration of the electron beam or depth of carrier excitation, R_e, is a function of electron beam energy, E (eV), and sample density, ρ (g/cm^3):[10]

$$R_e(cm) = \frac{(4.28 \times 10^{-6})}{\rho} E^{1.75} \tag{8.2}$$

Table 8.1 shows carrier collection efficiency, η_{cc}, and depth range of the electron beam excitation volume, R_e, at varying acceleration voltages. The very low carrier collection efficiencies for acceleration voltages under 20 kV is attributed to the thick n^+ cap on the sample. Because of the high doping of the n layer, thediffusion length of holes is estimated to be on the order of 10 nm which makes carrier collection at the junction very improbable. The sudden increase of the sample current at acceleration voltages above 20 kV represents the onset of excitation in the depletion width of the junction. In order to decouple the effects of the thick n^+ cap and determine the efficiency of the junction we calculated the fraction of carriers created beneath the 2 μm thick n^+ cap by integrating

Acceleration Voltage (kV)	Collection Efficiency (η_{eff})
10	1.8×10^{-6}
15	8.2×10^{-6}
17	2.58×10^{-5}
20	0.021
21	0.037
22	0.052
23	0.065
24	0.084
25	0.111
30	0.211

Table 8.1 Carrier collection efficiency of SiGe P-I-N photo-detector as a function of electron beam acceleration voltage.

the generation function given by:[10]

$$g_{(z)} = 0.6 + 6.21z - 12.40z^2 + 5.69z^3 \qquad (8.3)$$

where g is the carrier pair generation distribution function as a function of normalized depth z, ($z=x/R_e$).

The fraction of carriers created underneath the 2 μm thick n^+ cap, F, is determined by the integral of $g_{(z)}$ where the lower integration limit represents the normalized depth of the junction.

$$F = \int_{2/R_e(\mu m)}^{1} g_{(z)}dz \qquad (8.4)$$

The charge collection efficiency of the junction, $\eta_{junction}$, is determined by fitting the η_{cc} data as a function of acceleration voltage to a function of the form:

$$\eta_{cc} = \eta_{junction}F \qquad (8.5)$$

By excluding the dead layer effects of n+ cap we have determined that the efficiency of the junction is 50%. Figure 8.5 shows η_{cc}, F, and ($\eta_{junction}$ F) as a function of acceleration voltage. Possible reasons for the lower than 100% efficiency are the breakdown of the junction field region near dislocations or the proximity of the junction to the high dislocation density misfit region of the device.

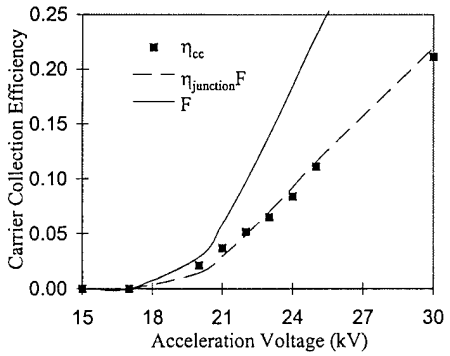

Fig. 8.5: Carrier collection efficiency, and fraction of carriers created beneath the n+ layer as a function of acceleration voltage. The dashed line, a fit to data, is of the solid line.

8.3.3 Responsivity

The spectral responsivity of the graded buffer photodetector was measured using a halogen lamp and a monchromator set to 60Å resolution. A power meter was used to calibrate the output of the halogen lamp and the monochromator. The current signal from the unbiased 4100 x 4100μm $Si_{0.5}Ge_{0.5}$ photodetector was amplified and measured using a lock-in technique. The spectral response of the $Si_{0.5}Ge_{0.5}$ graded buffer photodetector and a silicon photodiode are shown in Figure 8.6. The responsivity of the photodetector falls off at 1.3μm to 3 mA/W. The $Si_{0.5}Ge_{0.5}$ relaxed buffer photodetector has low responsivities at 1.3 μm because the absorption coefficient, α, at this wavelength is small ($\sim 10cm^{-1}$). The indirect bandgap of all SiGe alloys results in poor absorption at wavelengths just short of the bandedge. In order to achieve high a in SiGe alloys at 1.3μm the germanium fraction must be increased. Strain could also be used to further decrease the bandgap and hence increase absorption.

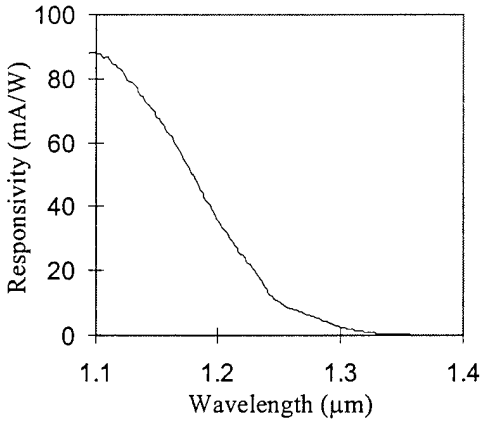

Fig. 8.6: Spectral Responsivity of $Si_{0.5}Ge_{0.5}$ graded buffer.
The response near the bandedge is weak due to poor absorption.

8.4 Waveguide-Photodetector Integration

The coupling efficiency of light from the polySi waveguide to the SiGe photodetector is key in evaluating the optical interconnect technology. The ability of the photodetector to collect light is determined by the product of (αL_{eff}), where L_{eff} is the effective absorption length in the active region of the device. We have used a beam propagation model to examine the coupling efficiency or L_{eff} of a monolithic polySi waveguide and $Si_{0.5}Ge_{0.5}$

photodetector optical circuit. The results show that the graded buffer reduces vertical confinement in the photodetector structure and a large fraction of the light is lost to the substrate in very short distances. Figure 8.7a shows a schematic of the geometry of the integrated structures and figure 8.7b, shows the propagated power as a function of distance into the detector. The propagated power falls to 10% in 8 μm. Thus a high efficiency device must use either a material with a high absorption coefficient (so that a higher fraction of the light is absorbed before it is lost to the substrate) or a more sophisticated design for coupling light from the waveguide into the photodetector.

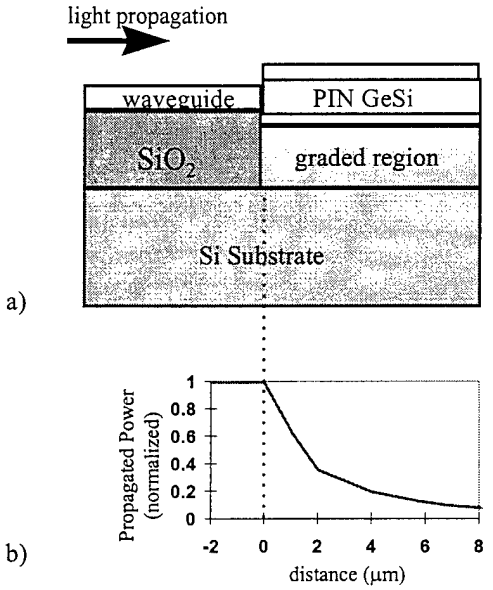

Fig. 8.7: a) Schematic of integrated polySi waveguide and SiGe P-I-N photodetector. b) Propagated power as a function of distance into the photodetector. The substantial loss in power is due to substrate losses.

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Chapter 9

Effect of Substrate Miscut on Si-Ge/Si Heterostructures

9.1 Introduction

A large lattice constant semiconductor epitaxially grown on silicon (Si) is a useful preliminary structure for microelectronics applications like III-V integration on Si [1] and for fabricating high mobility devices [2, 3]. Alloys of silicon and germanium (Si-Ge) grown on Si satisfy the lattice constant requirement and have been extensively studied in the past few years. As in all lattice-mismatched systems heteroepitaxial growth of Si-Ge/Si beyond the critical thickness [4] generally results in the formation of misfit and associated threading dislocations. Most applications do require Si-Ge layers much thicker than that imposed by the critical thickness limit and hence, a variety of techniques have been attempted to circumvent the threading dislocation problem [5]. One of the more successful approaches to fabricate relatively defect free Si-Ge/Si layers is the growth of relaxed graded structures. Totally relaxed Si-Ge layers with low threading dislocation densities have been successfully grown using this technique [6]. The utility of such structures in device applications has also been demonstrated [1].

Surface morphology and defect structure are key issues in utilizing these structures for electronic and opto-electronic applications. The strain fields associated with the misfit dislocations lead to the characteristic cross hatch pattern on the epilayer surface in lattice mismatched heteroepitaxy [1]. For (001) epitaxy, the cross hatch pattern occurs in form of trenches and ridges aligned along the two in-plane <110> directions. The cross hatch pattern has been observed in graded Si-Ge/Si [7, 8] and other lattice-mismatched

systems such as $In_xGa_{1-x}As$/GaAs [9,10], GaAsP/GaAs [11], GaAs/Si [12] and Ge_xSi_{1-x}/Si [13]. We note here that this cross hatch pattern is very different from the <100> oriented "surface ripples" that are observed [14, 15] in thin elastically strained Si-Ge/Si(001) epitaxial films. Under typical growth conditions, the surface ripples generally have a much shorter wavelength and originate from a thermodynamic equilibrium between surface roughness and misfit-induced elastic strain [16]. In slowly graded Si-Ge structures grown at fairly high temperatures, such as the samples discussed in this study, the epilayers relax easily forming misfit dislocations at the interface and hence the <100> oriented surface ripples are not observed. The predominant surface morphology effect that one observes is the <110> cross hatch pattern from the strain fields of the underlying long misfit dislocations.

In this study we show that even gradual roughness such as those present in slowly graded samples, leads to the formation of dislocation pile-ups in graded buffers under prolonged relaxation. The pile-ups increase the threading dislocation density in the relaxed Ge-Si/Si structures. We show that by growth on off-cut wafers, the surface roughness decreases drastically and the pile-up density decreases as well. We propose that threading dislocations are not easily blocked by non-parallel misfit dislocations. In addition, we have discovered that it is possible to form an alternative dislocation array to the 60° dislocation array normally present in graded relaxed mismatched heterostructures. We have observed in Ge rich regions of the graded Ge_xSi_{1-x} structures, a large number of edge dislocations of the type ½<110> as well as in-plane Burgers vectors of the type <100>. Four ½<110> edge dislocations and two <100> edge dislocations lead to a lower energy hexagonal dislocation network. Such a dislocation network, first reported in bulk silver bromide crystals [17], has not been characterized in lattice mismatched heteroepitaxial thin films. We show that favorable intersection of the {111} glide planes in the samples grown on the miscut substrates aid the dislocation reactions necessary to form this network.

This study clearly shows that miscut substrates provide a substantial improvement in the defect structure and surface morphology in Ge/Si-Ge(graded)/Si structures. In addition, growth on miscut substrates encourages the formation of a hexagonal

dislocation structure which may relax layers with improved surface morphologies and lower defect densities.

9.2 Experiment

Epitaxial films of $Ge/Ge_xSi_{1-x}/Si$ were grown on 2 inch (001) and (001) 6° off-cut (towards in-plane <110>) n-Si substrates using Ultra-high vacuum chemical vapor deposition (UHVCVD). Relaxed graded Ge_xSi_{1-x} films were typically grown between 800-900° C. The films were graded from pure Si (x=0) to pure Ge (x=1) at a constant grading rate of 10% Ge/μm. The grading rate of 10% Ge/μm was achieved by increasing the Ge content by ≈3.33% Ge in steps of ≈0.33 μm. A 2 μm uniform cap layer of pure Ge was grown above the graded region. The top 0.1 μm of the uniform cap layer was p-doped to create a p-i-n structure suitable for electron beam induced current (EBIC) characterization. $Ge_xSi_{1-x}/Si(001)$ films graded to 30% and 70% final Ge composition were also grown under similar growth conditions for comparison. The cap layer in each case had the same uniform Ge concentration as the final Ge % in the respective graded layers.

The surface morphology of the heterostructures was characterized using scanning electron microscopy (SEM) and atomic force microscopy (AFM). The rms roughness data was obtained from a number of 100μm x 100μm surface scans using contact mode AFM (Nanoscope III, Digital Instruments Inc.). The maximum trench depth of the cross hatch pattern was determined by the "section analysis" routine.

The dislocation structures were characterized primarily through (001) plan view TEM. The samples for observation were prepared by mechanical polishing from the Si substrate side to about 20 μm followed by argon ion beam milling. For observing the dislocation networks near the top of the graded Si-Ge region (Ge-rich), the sample was ion-milled primarily from the substrate side until electron transparency was obtained. For characterizing the Si-rich regions of the graded Si-Ge structure, the sample was milled from both the substrate side and the epilayer side.

Electron beam induced current (EBIC) was used to observe electrically active dislocations threading up through the uniform cap layer. The threading segments of

dislocations gliding on the {111} planes can interact with stress fields of pre-existing orthogonal misfit dislocations [18] and get trapped. Other factors like surface trenches can aid such blocking. This blocking can create dislocation pile-ups along trenches in the cross hatch pattern. These pile-ups were good recombination sites for charge carriers and showed a dark contrast along the trenches. The dislocation pile-ups are planar defects and their densities were characterized by the number of intersections per unit length of the sample surface. The density (no./cm) was determined by calculating the number of intersections of the dark contrast lines with random straight lines drawn on the EBIC micrographs.

9.3 Results and discussion

Fig. 9-1 shows the trend in threading dislocation density versus final Ge concentration in graded 10%Ge/μm layers. For this constant grading rate, one does not expect an increase in threading dislocation density unless there is a decrease in average misfit dislocation length [19]. Thus one possibility is that dislocation interactions that arrest dislocation motion must become more probable with thicker graded layers. In addition, the increase in threading dislocation density can be correlated to surface roughness and dislocation pile-up density. In the following sections, we first discuss our observation of surface morphology and pile-up density on on-axis wafers, followed by the effect of off-cut wafers on defect morphology.

9.3.1 (001) on-axis surface morphology

Early work showed that the surface cross hatch pattern was related to misfit dislocation strain fields [10]. The strain fields associated with threading dislocations also change the surface morphology [7]. Lattice mismatch strain itself, without the presence of dislocations, can roughen the surface if the growth temperature, sign and magnitude of the strain is adequate [20]. The unifying theme is that any event that can produce lattice strain will induce surface roughening if the temperature is high enough to allow enough surface diffusion to approach thermodynamic equilibrium. The surface roughness due to the cross hatch pattern in graded Si-Ge structures is primarily due to strain fields arising

from inhomogeneous distribution of misfit dislocations at each grading step interface [1]. The growing surface incorporates undulations (to minimize strain energy) in response to local strain field variations. The strain field variations from an array of misfit dislocations at each hetero-interface extend well beyond each Ge grading step (0.33μm). Thus, the cross hatch pattern at any instant during growth is the response of the surface to multiple overlapping strain fields. The formation of cross hatch pattern exposes higher index planes along the trenches. CVD growth subsequently leads to anisotropic growth effects and accentuates the surface roughness further.

Fig. 9-2 shows the effect of increasing final Ge content of the graded layer on the rms roughness of the top surface in Ge_xSi_{1-x}/Si films. Since all the graded layers were grown at 10% Ge/μm, different final Ge contents indicate that the graded regions in each structure have different thicknesses as well. With the increase of Ge content of the graded region, the rms roughness increases. This behavior was also observed by Hsu et al. [7] for Ge_xSi_{1-x}/Si samples grown using molecular beam epitaxy (MBE).

There are different mechanisms which can contribute to the increased roughness observed in Fig. 9-2. In all low-mismatched heterostructures, the cross hatch pattern contributes to an increase in surface roughness. It has been suggested that the cross hatch pattern is primarily due to formation of surface steps produced by gliding 60° dislocations [9, 13]. This proposition alone, however, does not explain the increase in rms roughness of the cross hatch pattern with increase in grading rate for equally relaxed graded Si-Ge structures [1, 7]. Nor can it explain difference in cross hatch morphology (long-wavelength surface undulations) due to growth temperature. Also, the surface roughness anisotropy along the two <110> directions (for growth on the off-cut substrate) cannot be explained by the surface step argument, since dislocations are introduced in equal numbers along both <110> directions. Surface step formation by gliding dislocations could affect the cross hatch appearance in the early stages of stress relaxation in partially relaxed graded Si-Ge films [8]. If surface diffusion is limited, for example at low growth temperatures, the steps produced by the dislocations will not migrate the distances necessary to achieve the equilibrium surface. In completely relaxed graded Si-Ge/Si structures grown at higher temperatures, where the equilibrium surface can be achieved,

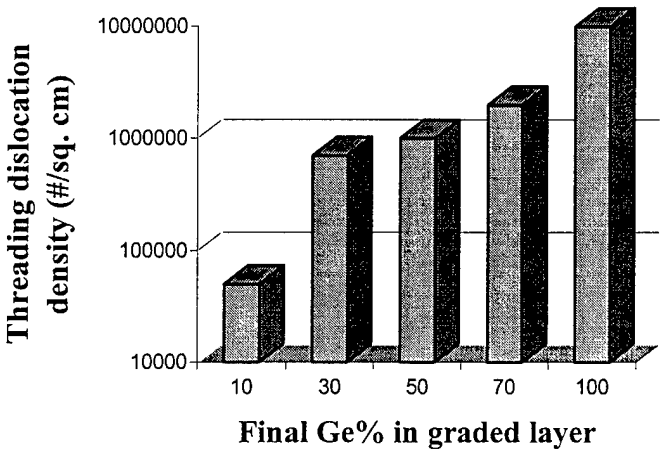


Fig. 9-1: A plot showing increase in threading dislocation density with increasing final Ge% in the graded layer.

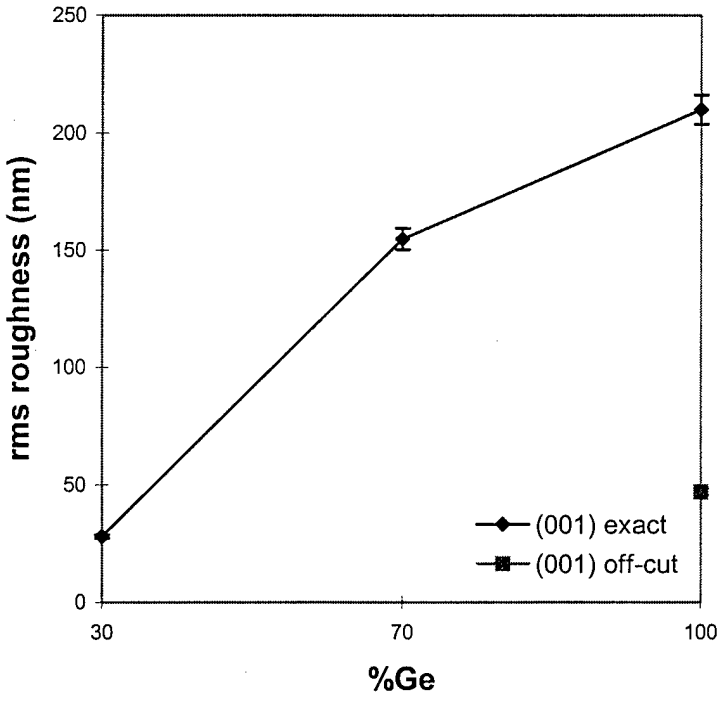


Fig. 9-2: A plot showing the increase in rms surface roughness with increase in the final Ge% of the graded layer.

strain field effects from underlying misfit dislocations coupled with anisotropic growth kinetics are predominantly responsible for cross hatch formation. In layers graded gradually from Si to pure Ge an additional feature appears in CVD grown material on on-axis wafers. Rare, deep trenches are observed on the surface that accounts for increased rms roughness of the samples (Fig. 9-3). Since they are absent in 10% Ge/μm graded layers grown to $Ge_{0.3}Si_{0.7}$, they must be related to a rare degenerative phenomenon in the relaxed graded region that occurs more frequently with increased grading rate. Previous work [21] indicates that dislocation pile-up formation due to work hardening (dislocation interaction) in the graded buffer is likely responsible for the deep trench formation, as discussed in the next section.

9.3.2 Formation of dislocation pile-ups

In this section we discuss the mechanisms behind the dislocation pile-up formation and the resulting trench formation that degrades the surface morphology in graded Ge_xSi_{1-x} structures graded to high Ge concentrations.

Work hardening occurs in heavily dislocated materials; in this case the graded region may experience work hardening if the dislocation density becomes very high. The microscopic origin of such work hardening is dislocation interaction. In mismatched interfaces, it has been shown that a threading dislocation can be blocked by a perpendicular interface misfit dislocation [18], since in a single heterostructure they are confined to a single plane. When a threading dislocation approaches a orthogonal misfit dislocation, the effective force moving the threading dislocation is reduced by the stress field of the orthogonal misfit dislocation [18, 22]. The stress field from the misfit dislocation decays as $\approx 1/r$ where r is the distance from the misfit dislocation. Thus, there is some area above the misfit dislocation where the stress field has decayed sufficiently that the force on the threading dislocation is not great enough for continued glide. Therefore, a threading dislocation segment must pass through a restricted channel, h^* , formed between the surface and the decay of the misfit stress field from the interface. Fig. 9-4 is plot of normalized channel width, h^*/h as a function of $(h/b)\varepsilon^*$, where h is the

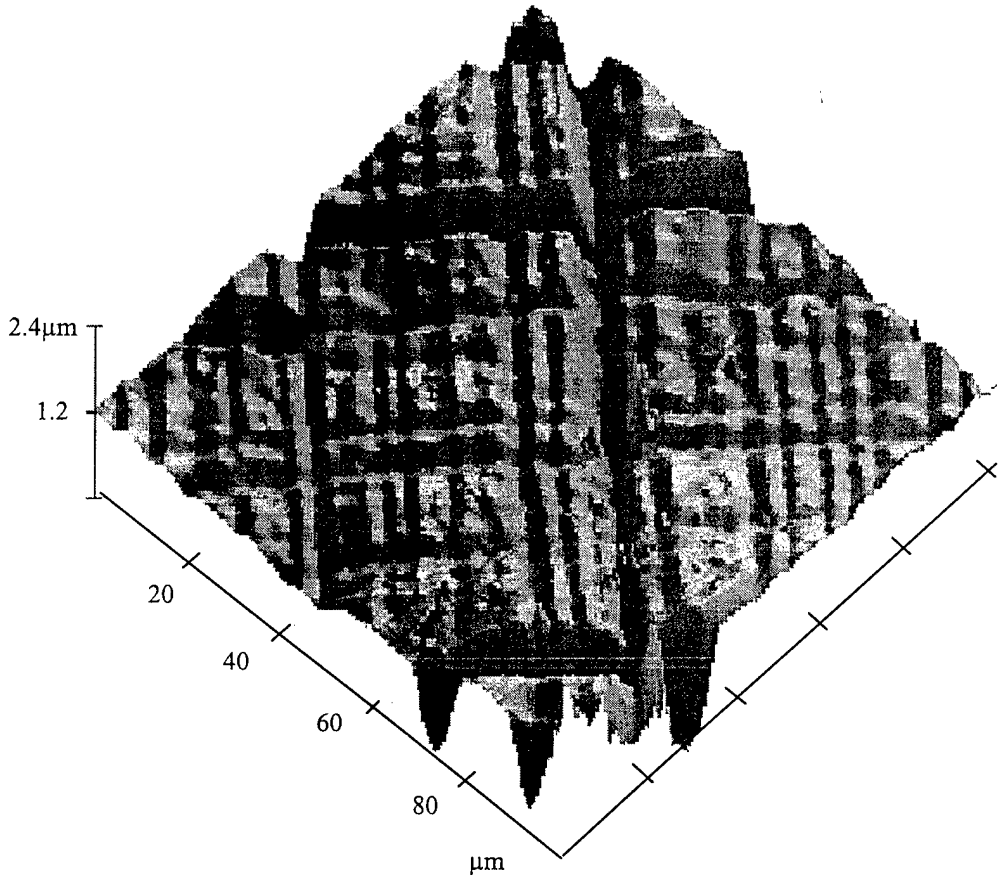


Fig. 9-3: An AFM image of the surface of UHVCVD grown relaxed graded Ge-Si sample graded up to 100%Ge on a Si(001) substrate. Deep trenches running along the two in-plane <110> directions account for the high rms roughness (≈210 nm).

height of the film and ε* is the background strain [22]. Referring to the plots in Fig. 9-4, for a background strain of ε* in a film thickness of h, h* is the channel width through which a threading segment must pass to overcome the stress field of the orthogonal dislocation.

For graded Ge_xSi_{1-x}/Si structures grown at 10%Ge/μm grading rate that the equilibrium critical thickness is ≈375 nm [1]. During growth of the graded layer, there is ≈375nm of graded Ge_xSi_{1-x} at the surface that is elastically strained at all times during the

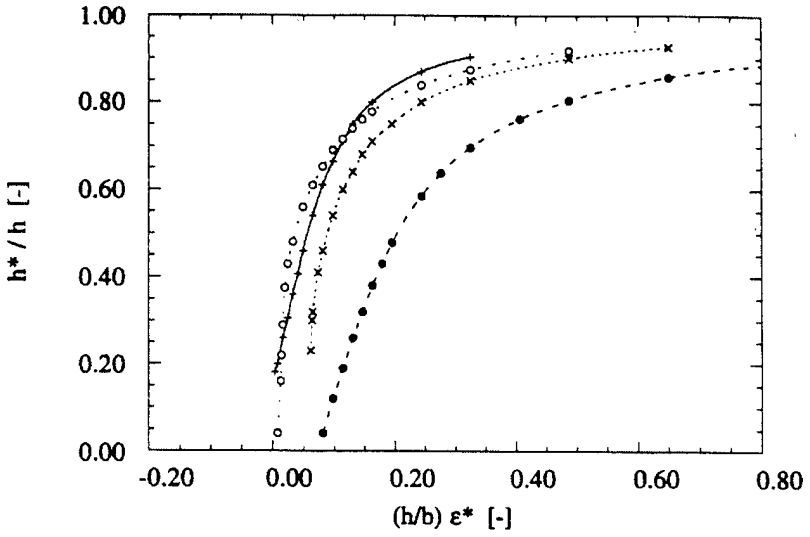


Fig. 9-4: A graph from Gillard et al. [22] showing a plot of h/h* versus (h/b)ε*, used to calculate h*/h ratio for graded Si-Ge/Si layers. The different curves are for different dislocation combinations. For the strains involved in our samples h*/h always tends to 1, irrespective of the dislocation combination chosen.

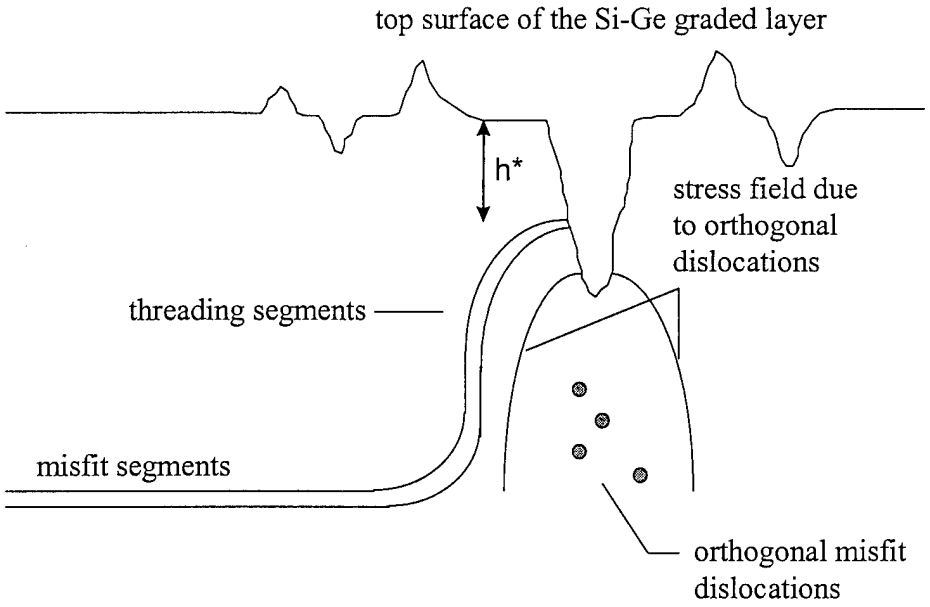


Fig. 9-5: A schematic showing the gliding dislocations interacting with existing dislocations and getting blocked at the trench side-walls.

process. In our growth experiments the grading rate of 10% Ge/μm was achieved by increasing the Ge content by ≈3.33% Ge in steps of ≈333 nm. Hence, each step in Ge is completely strained until the next step in concentration occurs, and the threading dislocation experiences approximately the same force as a single heterostructure 333 nm in thickness. The critical thickness is a strong function of the Ge grading rate and nearly independent of the final Ge% of the graded layer. Hence, the same critical thickness approximation can be applied to films graded to different final Ge% (at the same grading rate) in our experiments. The background strain ε* during graded layer growth for all films is therefore about ≈0.12% for the 3.33%Ge increase per step. Referring to Fig. 9-4, the h*/h ratio approaches unity under these conditions. Since the channel width, h*, is almost as thick as the epilayer, the gliding threading segment can easily overcome the strain field and blocking effect of any orthogonal misfit dislocation. Therefore, the blocking criterion of a single perpendicular dislocation cannot explain the formation of dislocation pile-ups in graded Ge_xSi_{1-x}/Si structures graded at a 10% Ge/μm grading rate. The blocking effect of orthogonal misfit dislocations is not large enough to counter the background strain in reasonably thick and moderately lattice-mismatched cases. To explain the formation of dislocation pile-ups in these graded structures, some other mechanism of dislocation blocking needs to be evoked.

Initially, some of the deeper regions in the cross hatch pattern can contribute to the blocking action of the gliding threading dislocation segments. Fig. 9-5 shows a schematic that explain the possible mechanism of dislocation blocking and subsequent dislocation pile-up formation in graded Ge_xSi_{1-x}/Si structures. Fig. 9-5 shows a threading segment of a gliding dislocation interacting and being blocked by the stress fields of pre-existing groups of orthogonal misfit dislocations. Such groups are known to exist in mismatch structures due to heterogeneous nucleation sources [23]. The strain fields from such a group create a deeper trough in the cross-hatch pattern. With this local decrease in thickness, threading dislocations get blocked since the channel width, h*, can decrease to zero from both the depression in the surface morphology and the stress fields from the orthogonal dislocations. Other gliding segments traveling on the same or parallel {111} planes could also be blocked, and previous blocked threading dislocations also aid in

subsequent blocking. Such an event can lead to a dislocation pile-up along a depression in the cross-hatch.

We note here that very pronounced deep ripple troughs [14], surface cusps [16], and surface depressions [24] have been identified as regions with reduced kinetic barriers to dislocation nucleation. Such events occur when the layers are heavily elastically strained (>1%) as mentioned previously. Recent TEM studies [25] have revealed that there is a direct correlation between the position of troughs and individual dislocations injected to relieve misfit in InGaAs/GaAs system. However, in slowly graded structures such sharp dislocation sources are not present initially, and the strain is nearly completely relaxed except for a small equilibrium strain at the surface. Thus, dislocation nucleation can not be initially producing the pile-up structures. At higher growth temperatures and continued roughening due to CVD growth, it is not inconceivable that such large surface features contribute to dislocation nucleation. However, it is unlikely that all of the surface trenches that could lead to nucleation would be deeper than the channel width, h*. Thus the blocking events must be responsible for dislocation pile-up formation. Using this hypothesis of dislocation blocking, we can make estimates of when blocking should occur.

Our experimental data shows that depth of the most deep surface trench from the cross hatch pattern increases with increase in final Ge% of the graded region as shown in Fig. 9-6. The thickness of the channel available for the threading dislocation, h*, is also plotted on the same graph. Note that h* is a function of grading rate only and not of the final Ge% of the graded region. In cases where the maximum trench depth is greater than h*, dislocation pile-ups can be expected. The farther above the "maximum trench depth" point is from the h* line, the more trenches can block dislocations and hence we expect a higher density of dislocation pile-ups. For each Ge grading rate, a plot such as Fig. 9-6 can be constructed. Such plots would allow one to predict the likelihood of dislocation pile-up formation in graded structures. The above analysis, though demonstrated for graded Si-Ge/Si structures, is applicable to any graded lattice-mismatched heteroepitaxial system.

The dislocation pile-up formation contributes to further degradation of the surface morphology. Threading segments of gliding dislocations terminate at or near the trench

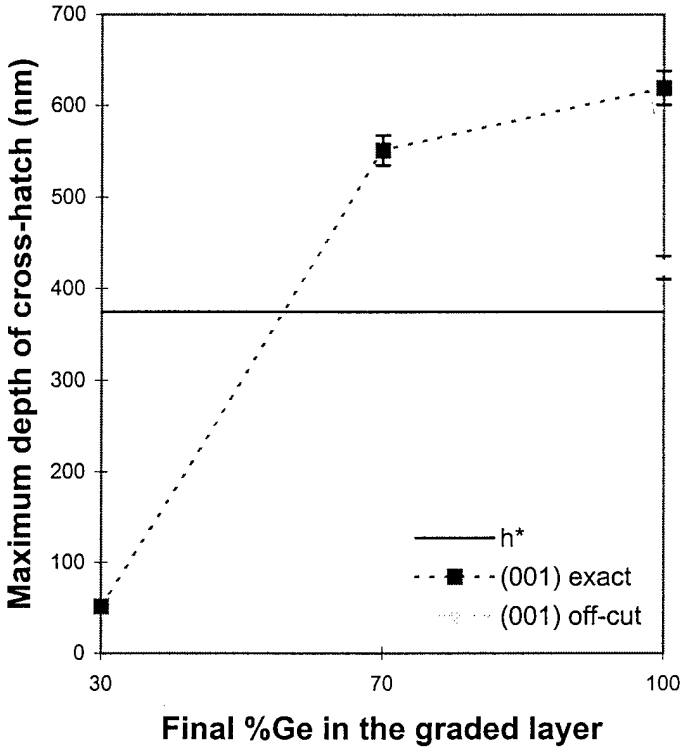


Fig. 9-6: A graph showing the variation of maximum trench depth of surface cross-hatch pattern with increase in final Ge% in the graded layer. Shown also is h* for 10% Ge/μm grading rate. Whenever the maximum trench depth is greater than h* , there is a high probability for forming dislocation pile-ups.

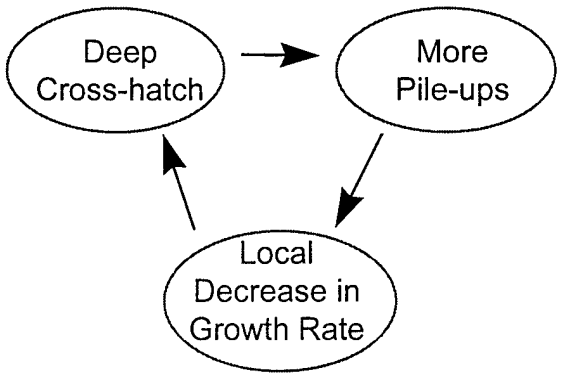


Fig. 9-7: A schematic diagram illustrating the vicious nature of interactions between surface morphology and dislocation pile-ups.

associated with the dislocation pile-up. The surface sites where the dislocations terminate are energetically unfavorable sites for adatoms diffusing on the growth surface. The growth rate at or near the trench is thereby further reduced. Such an effect increases the trench depths, making more gliding dislocations prone to blockage. The vicious nature of the interactions of the surface morphology and dislocation pile-up formation is summed up in a schematic sketch (Fig. 9-7). A correlation between rms roughness and dislocation pile-up density for $Ge/Ge_xSi_{1-x}/Si(001)$ samples (Fig. 9-8) along the two in-plane <110> directions agrees with the above analysis.

9.3.3 Effect of substrate miscut

In Fig. 9-2, the rms roughness for the 100% Ge sample grown on a Si(001) 6° off-cut substrate is drastically reduced compared to the on-axis sample. The reduced roughness is related to the lower pile-up density and crystal growth rates on different crystal surfaces. It was shown by L. Csepregi et. al. [26] that the growth rate for Si surfaces is highest for {001}, lowest for {111} and intermediate for {110}. The cross hatch pattern leads to the formation of planes tilted away from (001) growth surface, as described in the previous section. The surfaces oriented off the (001) have slower growth rates; thus a large differential in growth rates encourages even greater changes in growth rate, forming facets on the surface. Growth on a substrate that is miscut towards <110> implies that the difference in the growth rates along the trench side-walls and the average growth surface is less compared to growth on an exact (001) surface. Over prolonged growth, the miscut wafer case translates into reduced rms roughness of the growth surface. The above proposition can also explain the anisotropy of rms roughness along the two in-plane <110> directions for the off-cut sample. The in-plane <110> direction towards which the substrate was miscut showed a lower rms roughness than the orthogonal in-plane <110> direction (Fig. 9-8).

Another effect that contributes to the reduced rms roughness in the off-cut samples is the ease of formation of the edge dislocations with in-plane Burgers vector. Such dislocations as explained before, do not produce as severe strain field inhomogeneties at the growth surface as the mixed 60° dislocations. In addition if only

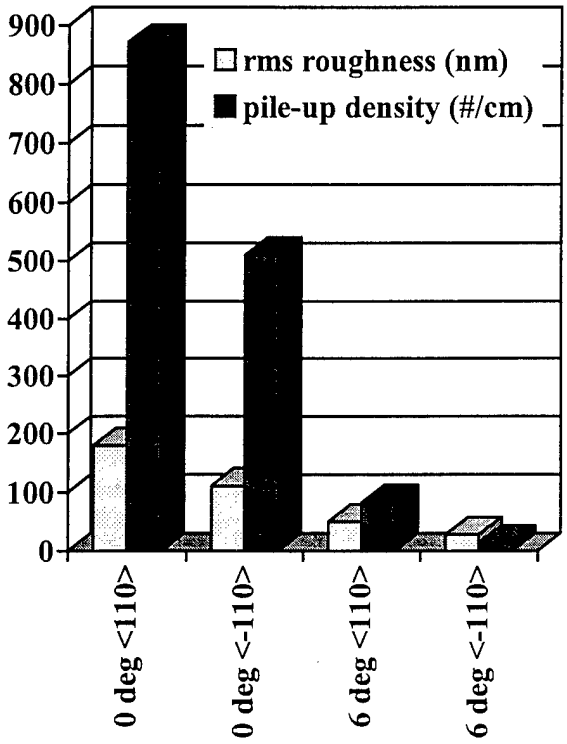
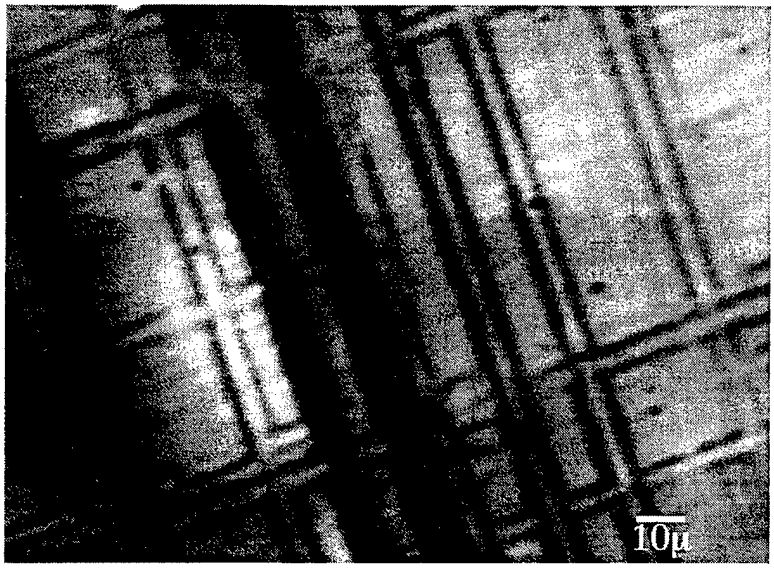


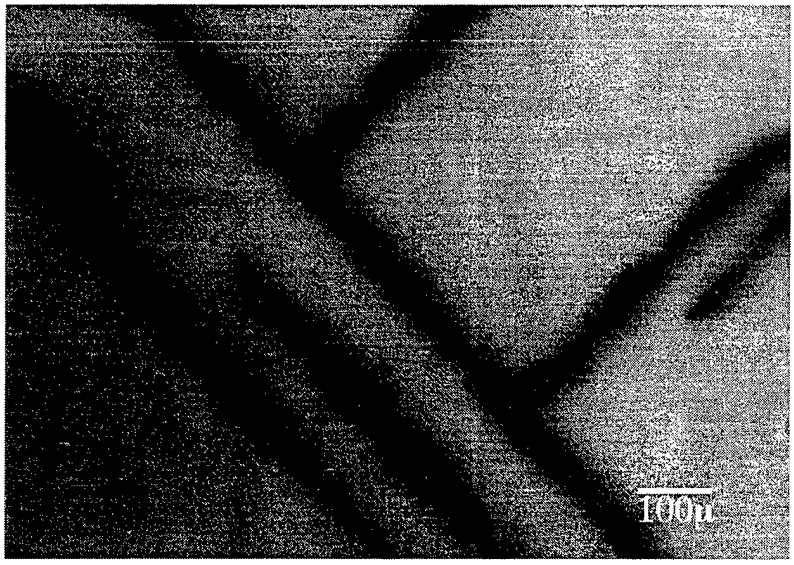
Fig. 9-8: A bar graph showing the correlation between the observed rms roughness and the dislocation pile-up density along the two in-plane <110> directions for 100% Ge graded samples grown on exact (001) and 6° off-cut (001) Si substrates.

edge type dislocations are present in a regular array, the strain fields from the neighboring dislocations will quickly annihilate, thus creating less residual strain fields at the surface of the growing epilayer.

Figs. 9-9a and 9-9b are plan-view EBIC images of 100% Ge graded-layer samples grown on Si(001) and Si(001) off-cut substrates respectively. There is a substantial reduction in dislocation pile-up density in the 100% Ge sample grown on the off-cut substrate, as expected from previous discussion. As evident from Fig. 9-6, there are fewer deep trenches that are capable of blocking gliding threading dislocations. Hence, it is not surprising that the dislocation pile-up density is extremely low for growth on the off-cut substrate. As shown in Fig. 9-8, there is also clear anisotropy in the dislocation pile-up density along the two in-plane <110> directions for the sample grown



(a)



(b)

Fig. 9-9: EBIC images of Si-Ge/Si samples graded up to 100%Ge grown on (a) Si(001) exact and (b) Si(001) 6° off-cut substrates.

on the off-cut substrate. The anisotropy in dislocation pile-up density follows the anisotropy of rms roughness. Reduced pile-up density will also reduce roughness since some of the spatially inhomogeneous strain fields are eliminated.

Kightley et al. [27] observed that in InGaAs layers grown on (001) off-cut (2° towards (010)) GaAs substrates, the 60° misfit dislocations did not lie exactly along the in-plane <110> directions. They observed that two 60° dislocations with the same line direction but gliding on different {111} planes would intersect each other due to the substrate miscut. Fig. 9-10 shows a schematic plan view of the 60° dislocation network on an on-axis and an off-cut wafer. Since the 60° dislocations are not parallel, a nucleation source cannot create long lines of parallel dislocations with the same Burgers vector. Thus, the dislocation contribution to the blocking picture (Fig. 9-5) is changed

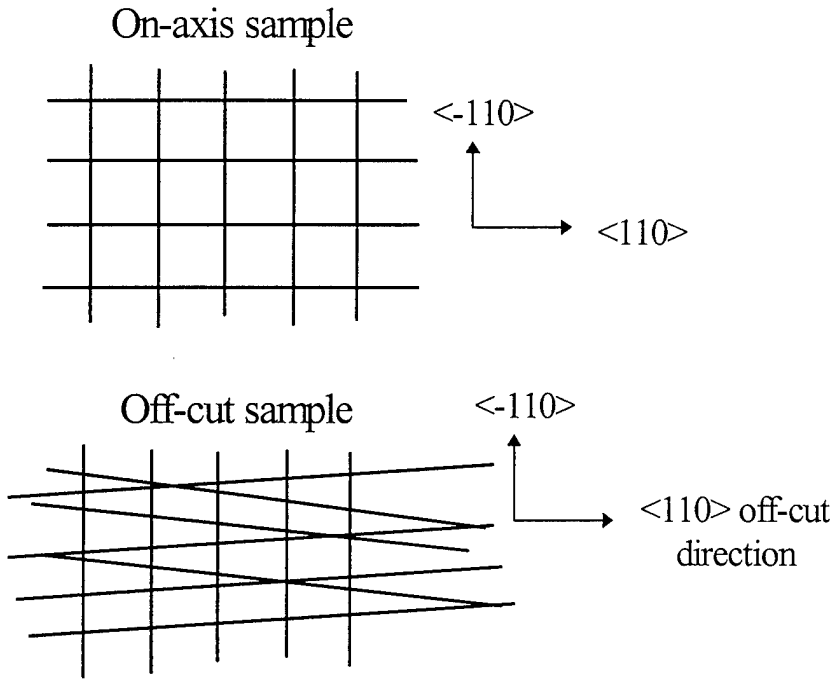
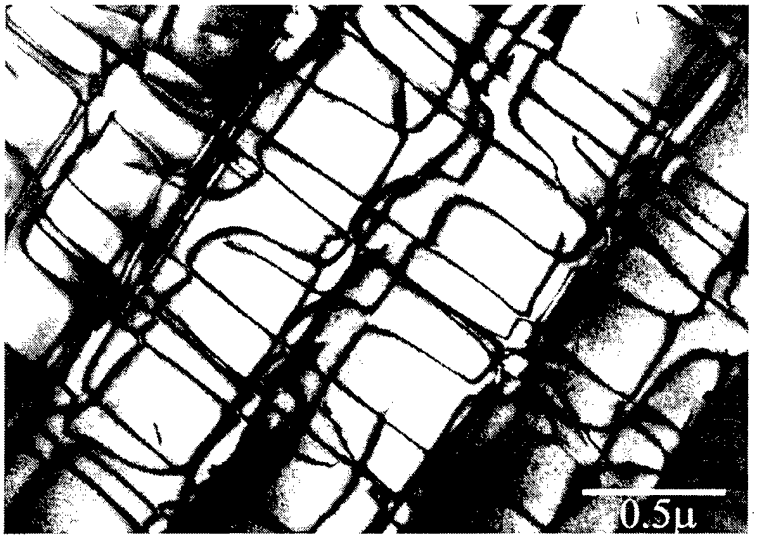


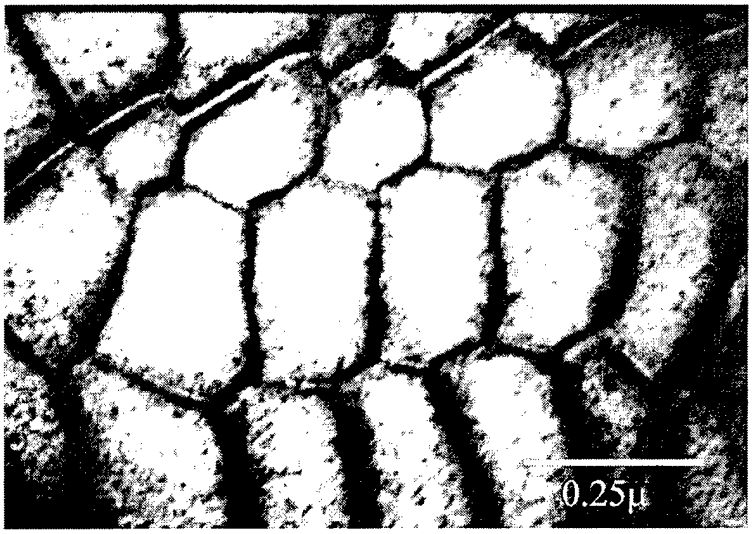
Fig. 9-10: A schematic showing a plan-view of the 60° dislocation network on an on-axis substrate and a substrate off-cut towards a <110> direction.

since a long wall of blocking stress fields is not created. In our growth experiments, the above proposition would be true only along one of the two <110> directions, since the miscut was towards a <110> direction. This hypothesis explains the anisotropy of pile-ups along the two <110> directions in the miscut sample.

9.3.4 Dislocation structure



(a)



(b)

Fig. 9-11: Plan view TEM micrographs of (a) Si-rich region of the graded structure showing an orthogonal array of 60° dislocations, (b) Ge-rich region of the graded structure showing a hexagonal network of edge dislocations.

It is well-known that low-mismatch, graded Si-Ge/Si(001) structures typically relax by the formation of 60° dislocations that glide down the various {111} planes to the (001)

interface [5, 23, 28]. The straight misfit segments of the 60° dislocations that relieve misfit lie along the two in-plane <110> directions at the (001) interface. Fig. 8-11a shows one such array of 60° dislocations existing in a (001) interface in the Si-rich region of the graded Si-Ge structure. Fig. 9-11b show a similar TEM micrograph taken from the Ge-rich region of the graded structure grown on a (001) off-cut substrate. A hexagonal network of dislocations is observed. A **g.b** analysis of the network revealed that it was made up of dislocations of the type ½<110>, ½<$\bar{1}$10> and <100>. Each node in the hexagonal network is formed by a <100> edge type dislocation and two reacting ½<110> edges. Such dislocation networks have also been observed by Hedges et al. [17] and Amelinckx [29] in bulk silver bromide (AgBr) and potassium chloride (KCl) crystals respectively. To our knowledge, such a dislocation structure has not been observed in heteroepitaxial thin film growth.

Two 60° dislocations with Burgers vectors of the type ½<101> and ½<011> can glide out of the (001) interface and react to form an edge dislocation of the type ½<110> [10, 30, 31]. Such reactions are favored since there is a large reduction in strain energy involved (b^2 criterion). However, the edge dislocations, lying in the (001) planes are sessile and can only react through a climb process. As the Ge content of the graded layer increases, the melting point of the Ge_xSi_{1-x} alloy decreases ($T_{m,Si}\approx1425°$ C, $T_{m,Ge}\approx940°$ C). Since the growth temperature is constant, the layer approaches the melting point as the GeSi content is increased to pure Ge. Vacancy diffusion increases as the growth temperature approaches the melting point and hence climb mechanisms, which are primarily vacancy diffusion based, can be activated. Thus the sessile edge dislocations can climb out of the (001) interface more easily as the Ge content of the graded layer increases. Edge dislocations of the type ½<110> (formed by reactions between 60° dislocations) can further react as shown :

$$\frac{1}{2}[110]+\frac{1}{2}[\bar{1}10]\rightarrow[010] \qquad (1)$$

$$\frac{1}{2}[110]+\frac{1}{2}[1\bar{1}0]\rightarrow[100] \qquad (2)$$

Such reactions, though energetically neutral using the elasticity theory, are favored since it leads to energy lowering due to the sharing of atomic misfit in the dislocation cores

[32]. Amelinckx [29] claims that very little external driving force is required for such reactions to proceed. In an orthogonal dislocation grid made up of dislocations of the kind ½<110> and ½<$\bar{1}$10>, reactions such as (1) and (2) can lead to a hexagonal network as observed in Fig. 8-11b. Since all the Burgers vectors of the network like in the (001) plane, they are 100% efficient in relieving the misfit strain unlike the 60° dislocations which are only 50% as efficient. Such a dislocation network is the lowest energy configuration possible at a mismatched interface. In the high Si regions of the graded Si-Ge structure, the difference in the growth temperature and the melting point of the alloy is large and therefore dislocation climb is not possible. In this case, the 60° network forms due to the kinetic barrier to climb (Fig. 9-11a)

TEM observations of the graded regions for the samples grown on exact (001) orientation revealed that the hexagonal network of dislocations do not form easily. In off-cut substrates, two 60° dislocations gliding on different {111} planes would intersect since their line directions in the (001) plane were off the exact <110> direction. Such intersections of 60° dislocations are favorable in their reaction to form an edge type dislocations [27]. The off-cut of the substrate increases the probability that a 60° dislocation would find the right 60° to react with. Thus, for samples on the off-cut substrates it would be easier for the ½<110> type edge dislocations to form. The presence of more ½<110> type edge dislocations implies that more reactions could occur and it is easier to form the low energy hexagonal network of dislocations. For samples grown on the (001) exact substrate, the formation of ½<110> type edges is more difficult and hence the formation of <100> dislocations is more difficult.

The new dislocation structure offers new degrees of freedom in designing relaxation processes. 60° dislocations are advantageous, since their introduction can be controlled at relatively low temperatures. However, it now appears that the subsequent elimination of the "extra" Burgers vector components is possible.

9.4 Conclusion

We have investigated the origin of dislocation pile-up formation and surface roughness in graded $Ge/Ge_xSi_{1-x}/Si$ layers. The effect of substrate off-cut on surface morphology,

dislocation pile-up formation and the dislocation structure was studied. Dislocation pile-ups originate from a combination of dislocation interaction and the effect of surface morphology. The samples grown on (001) off-cut substrates showed reduced surface roughness and a low dislocation pile-up density as compared to samples grown on (001) on-axis substrates. A model was proposed to explain the formation of dislocation pile-ups in graded structures. Applying both dislocation blocking criterion and studying the effect of maximum trench depth of the cross hatch pattern, led to predictions of dislocation pile-up formation. Off-cut wafers decrease the chance of dislocation pile-up formation, leading to lower threading dislocation densities and smoother surfaces. Additionally, reduced roughness is expected due to reduced growth rate anisotropy and the ease of formation of edge dislocations.

TEM studies revealed the presence of a novel hexagonal dislocation network consisting of edge dislocations with Burgers vector of the type ½<110>, ½<$\bar{1}$10> and <100> in the Ge-rich regions of the graded structure. The dislocation climb processes are active in the Ge-rich alloys since the growth temperature is closer to the melting point. This facilitates reactions necessary for the hexagonal network formation. In the off-cut samples favorable intersections of 60° dislocations aid the formation of ½<110> type edge dislocations and hence the <100> type as compared to the on-axis samples. The new dislocation structure offers opportunities to explore new processes which may eliminate spatially variant strain fields in relaxed epitaxial layers and reduce threading dislocation densities.

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