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LOW TEMPERATURE MATERIALS GROWTH AND PROCESSING DEVELOPMENT FOR FLAT PANEL DISPLAY TECHNOLOGY APPLICATIONS

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From: Director, Office of Naval Research, Seattle Regional Office, 1107 NE 45th St., Suite 350, Seattle, WA 98105
To: Defense Technical Center, Attn: P. Mawby, 8725 John J. Kingman Rd., Suite 0944, Ft. Belvoir, VA 22060-6218

Subj: RETURNED GRANTEE/CONTRACTOR TECHNICAL REPORTS

1. This confirms our conversations of 27 Feb 97 and 11 Jul 97. Enclosed are a number of technical reports which were returned to our agency for lack of clear distribution availability statement. This confirms that all reports are unclassified and are "APPROVED FOR PUBLIC RELEASE" with no restrictions.

2. Please contact me if you require additional information. My e-mail is *silverr@onr.navy.mil* and my phone is (206) 625-3196.

ROBERT J. SILVERMAN

FIELD EMITTER FLAT PANEL RESULTS

Anthony E Bell, Associate Professor

Graduate Assistants: Kit-sing Mak, Haibing Liu

I. SUMMARY

Objectives:

a) To understand the relative advantages and properties of diamond and graphite nanotubes as emission sources for FED displays.

b) To develop methods of growing uniform deposits of graphite (fullerene) nanotubes of nanometer scale diameters. It is believed that these field emitters will have the following properties:

1. Low turn-on voltages
2. Insensitivity to the vacuum ambient.
3. Inexpensive methods of preparation
4. A compatibility with other industrial efforts - e.g. that of S.I. Diamond Corp.

II. TECHNICAL REPORT

Method of Approach:

a) Measure the work function, using a geometry independent absolute method, of diamond, both doped and undoped diamond, in order to establish the claims of ultra-low work function of n-doped diamond substrates.

b) Grow graphite nanotubes on Fe nuclei seeded on Si wafers and characterize them by inserting them in a vacuum viewing apparatus with a phosphor screen in order to ascertain the uniformity of electron emission over an area 1 cm x 1 cm. The wafer is heavily doped in order to be electrically conductive and is miscut by 5 degrees so that there will be a uniform density of step edge defects capable of accommodating and attracting the vacuum deposited Fe nanometer scale nuclei on which to anchor the growing carbon nanotubes.

c) Study different methods of depositing nanotubes, including plasma techniques.

Results:

a) Diamond film work functions have been determined and appear to be approximately 4.5 eV. Hence there does not appear to be a low work function associated with the present undoped diamond films.

b) In recent attempts to grow nanotubes on a heated (700 C) nichrome wire subjected to a flux of sputtered graphite, a very thin diamond film was obtained together with a sparse distribution of nanotubes, as observed in a high resolution STEM. This result seems to confirm a speculation (one of SI Diamond's and of the present author's) that the reason for the low voltage turn-on of SI Diamond FEDs is the presence of randomly distributed nanotubes on the diamond surface. Indeed, the magnified images of SI

Diamond individual pixels indicates that light originates from randomly located mobile bright spots that could be caused by electron emission from long nanotubes that sway in the presence of a strong electric field. The nanotubes because of their extremely high aspect ratios are likely to be very flexible.

III. FUTURE EFFORT

Work for the next quarter:

- Calibration of the absolute retarding potential technique for measuring work function will be made by determining the work functions of n and p-doped silicon.
- A work function study of n-doped diamond will be made.
- Field emission evaluation of the new nanotubes will be performed

CHARACTERIZATION AND SIMULATION OF THIN FILM TRANSISTORS FOR TRANSIENT THERMAL PROCESSING

V. S. Rao Gudimetla, Assistant Professor

I. SUMMARY

The project goal is to make DC, AC, transient measurements on the TFTs, fabricated by Professor Sigmon and his group at Arizona State University using low temperature processing techniques. From these measurements, SPICE parameters will be extracted and these results will be used for process monitoring and device and process optimization for display applications. This work was started by Rao Gudimetla on 10/1/94 and this technical report is for the period 5/15/95 to 8/14/95.

II. TECHNICAL REPORT

During the above period, Rao Gudimetla did a NASA/ASEE Summer Faculty Fellowship at Marshal Space Flight Center at Huntsville, AL and was not supported by this grant. Hence, no effort was put towards the TFT work. However, starting from August 18, 1995, Rao Gudimetla is spending considerable time with Dr. Tom Sigmon's group at Lawrence Livermore National Lab (LLNL).

Since August 18th, we have started analyzing the I-V data from several TFTs fabricated at LLNL and spice modeling is being pursued. The goal is process optimization for better performance of the devices. Especially, we are investigating contact resistance and channel conductance. Since this work started about 3 weeks ago, no conclusions have yet been arrived at.

III. FUTURE EFFORT

1. Extensive data base collected on recently fabricated TFTs will be analyzed with the goal of optimizing the device performance.
2. The on-going work on the electrical properties of the grain boundary for use in developing a reliable SPICE model for TFTs will be completed.
3. Complete the transient measurements on LLNL TFTs.

EVALUATION OF PULSED UV-LASER GAS PHASE DOPING FOR FABRICATION OF HIGH PERFORMANCE POLYSILICON TFTs

Thomas Sigmon, Professor

I. SUMMARY

The primary purpose of this research effort is to investigate and characterize the use of Gas Immersion Laser Doping (GILD) for the fabrication of polysilicon thin-film transistors (TFTs). To achieve this goal we will fabricate poly-Si TFTs using both standard, industrially recognized doping and annealing processes in parallel with laser processing annealing. Previous quarter reports detailed the development of a TFT process flow based on an existing mask set available at Stanford University, the fabrication of conventional and laser processed NMOS TFTs, and the electrical testing of these TFTs. In Section II, this quarter's report identifies the major problems encountered in TFT Run 1, and how they will be avoided in TFT Run 2. A major effort this quarter was the development of a new mask set, specifically optimized for fabricating both conventional and laser processed TFTs, and is also outlined in Section II. Section III concludes by stating future efforts.

II. TECHNICAL REPORT

Having previously designed a TFT process flow, processed Run 1 for NMOS TFTs, and electrically tested the results, we are now able to identify the problem areas and propose solutions. The major problems encountered in Run 1 and their proposed solutions are listed in Table 1.

The mask set used for TFT Run 1 was borrowed from another research group at Stanford. This mask set had a lot of wasted (open) space, contained many devices that we were not interested in, and did not have melt pads for *in-situ* melt-time measurement during GILD processing. A new mask set was designed to remove these inefficiencies. Figure 1 shows the minimum geometries used in laying out each transistor. This new mask set was designed for either NMOS or PMOS coplanar, self-aligned poly-Si gate, TFTs. Eight levels are available for ultimate flexibility in fabricating both conventional and GILD processed TFTs within each die. Table 2 identifies the structures present on the GILD TFT mask set.

TABLE 1: PROPOSED SOLUTIONS TO PROBLEMS ENCOUNTERED IN TFT RUN 1

Problem/ Solution	Description
Problem 1	The laser energy fluences used in re-crystallizing the poly-Si active areas were too low to show any improvement in TFT electrical characteristics.
Solution 1	The laser processing parameters for poly-Si re-crystallization need to be studied in depth and optimized before committing to TFT Run 2.
Problem 2	The ion implanted and furnace annealed source and drain resistivities were essentially infinite (although the gate resistivities were fine.).
Solution 2	SIMS revealed that the implanted phosphorus was present in the source and drain regions, with a peak concentration of $4x10^{20}$ cm^{-3}. Possible reasons for high source and drain resistivities are insufficient furnace anneal time for dopant activation and high contact resistance resulting from a low surface dopant concentration. To avoid this problem in the future, longer annealing times will be used (i.e., 24 hours instead of 1 hour at 600 C), and TRIM simulations will be carried out to optimize the implant profiles
Problem 3	GILD source and drain resistivities were too high.
Solution 3	Optimize laser processing conditions to produce low resistivity poly-Si films, before committing to TFT Run 2.
Problem 4	The TFT mask set did not permit *in-situ* observation of melt time during laser processing. Inefficient use of wafer real-estate led to processing many wafers..
Solution 4	Develop a new mask set, optimized for fabricating both conventional and laser processed TFTs.

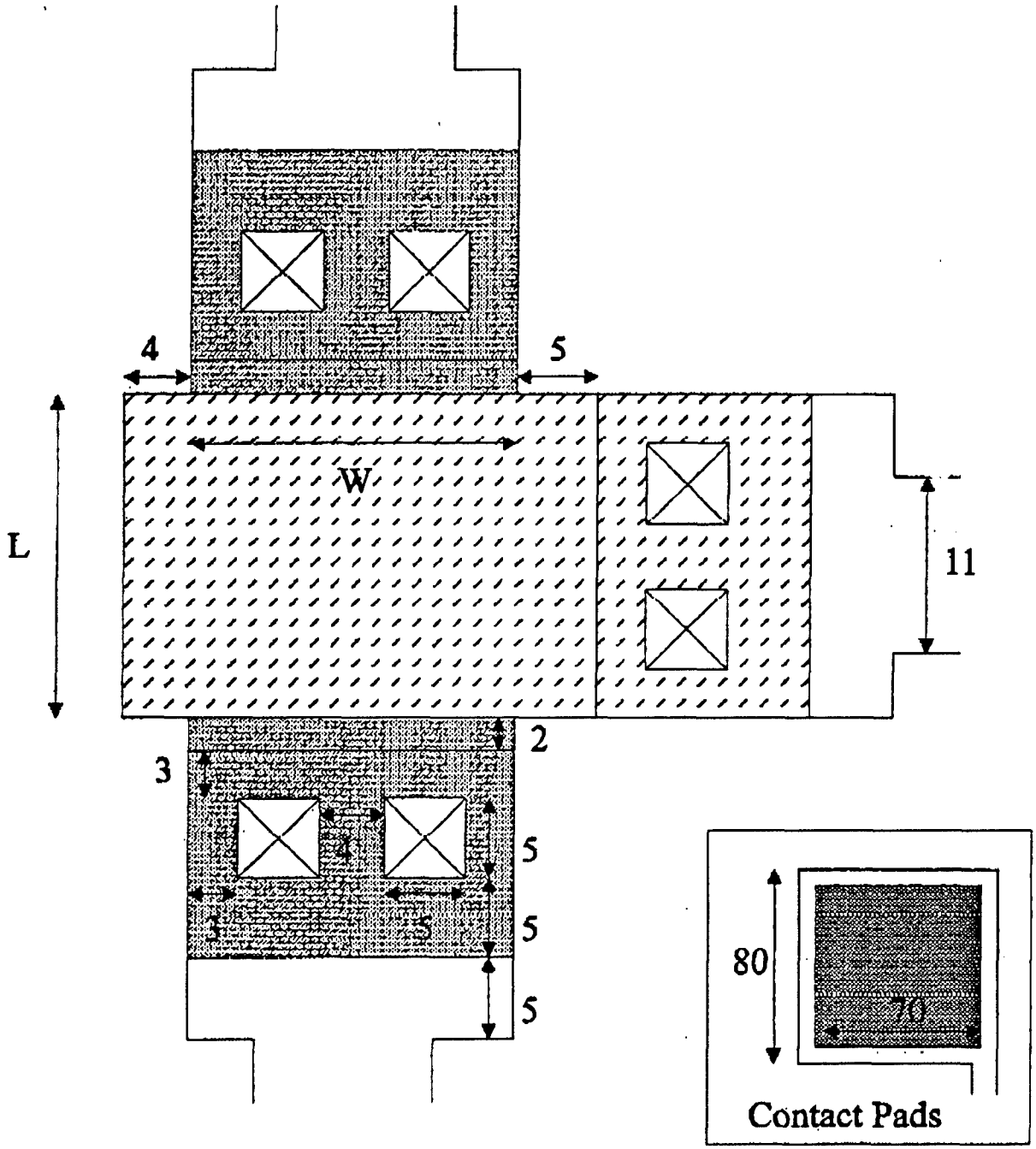

Figure 1 A Typical TFT as laid out in the new GILD TFT mask set, illustrating the minimum design geometries used.

TABLE 2: STRUCTURES PRESENT ON THE GILD TFT MASK SET

Structure	Geometry
TFTs	W/L = 20/2, 20/4, 20/6, 20/10, 20/20, 20/50, 50/2, 50/4, 50/6, 50/10, 50/20, 50/50, 10/2, 10/10, 200/10, 300/20
Van der Pauw	W/L = 11/15, 25.5/30
Kelvin	W/L = 5/7, 5/9, 5/13
Hall	2.5 mm square in S/D level
TEM	6 micron linewidths in S/D level
SEM	Various widths in several layers
Melt Pads	200 micron squares for S/D and Gate levels

III. FUTURE EFFORT

This quarter completed the first iteration of TFT runs. Feedback from this first run was used to evaluate and improve our TFT process for future runs. Goals for future quarters include the following:

i) Work on optimizing GILD processing conditions for laser re-crystallization of poly-Si thin films for minimizing defects.

ii) Work on optimizing GILD processing conditions for low-resistivity laser-doped poly-Si.

iii) Develop a set of characterization techniques to provide feedback between iterations for optimizing goals *i*) and *ii*).

iv) Having completed goals I) through iii), proceed with TFT Run 2.

THE ELECTROLUMINESCENT DEVICE GROUP

Principle Investigators: Raj Solanki and Reinhart Engelmann

Graduate Student: J. Ferguson

I. SUMMARY

The objective of our group is to demonstrate activatorless EL phosphors based on quantum structures. To achieve this objective, we are in process fabricating SrS/CdSe quantum well structures. The technique employed to grow these films is atomic layer epitaxy (ALE). In previous reports we have discussed growth of SrS. We feel confident with growth of this material. Therefore, during the last quarter our effort was directed towards achieving ALE of CdSe.

II. TECHNICAL REPORT

We have chosen elemental Cd and Se as the source materials for ALE of CdSe. The substrates for this phase of our investigation were glass plates, as well as GaAs and InP wafers. As with any new material grown via ALE, a whole set of growth parameters need to be determined. We also want to keep these parameters as close to SrS as possible so that both SrS and CdSe can be grown alternately on the same substrate without having to change the conditions. The ALE parameters that have be to optimized include the source temperatures, substrate temperature, source and nitrogen pulse widths, and the carrier gas flow rate. The source temperatures were initially chosen based on what has been reported in literature for growth of cubic CdSe in MBE reactors.

To date, we have obtained uniform films of polycrystalline CdSe on glass substrates. These films have hexagonal phase. This is shown in Figure 1 which is an x-ray diffraction pattern. However, for our proposed SrS/CdSe system there is a close lattice match between their cubic phase. Therefore, we have been varying the growth parameters of CdSe to produce the cubic phase. Growth of epitaxial cubic CdSe has been reported in literature on GaAs substrates using MBE. Our reason for utilizing the single crystal substrates is to determine the ALE parameters that will produce cubic phase of CdSe on GaAs and InP. So far we have determined conditions that produce a dominant (111) CdSe and much smaller hexagonal peaks (Figure 2), showing a mixed phase of CdSe. Work is continuing at present to eliminate the hexagonal phase.

III. FUTURE EFFORT

The pace of our work in the current phase of this investigation is considerably slower than normal due to the toxic nature of the sources. After every couple of depositions, all glass parts have to be cleaned with concentrated nitric acid. The handling of the glassware and the waste products is rather tedious and time consuming. At the end of this quarter, our goal is to complete optimizing CdSe grown conditions and start fabricating SrS/CdSe multilayered films.

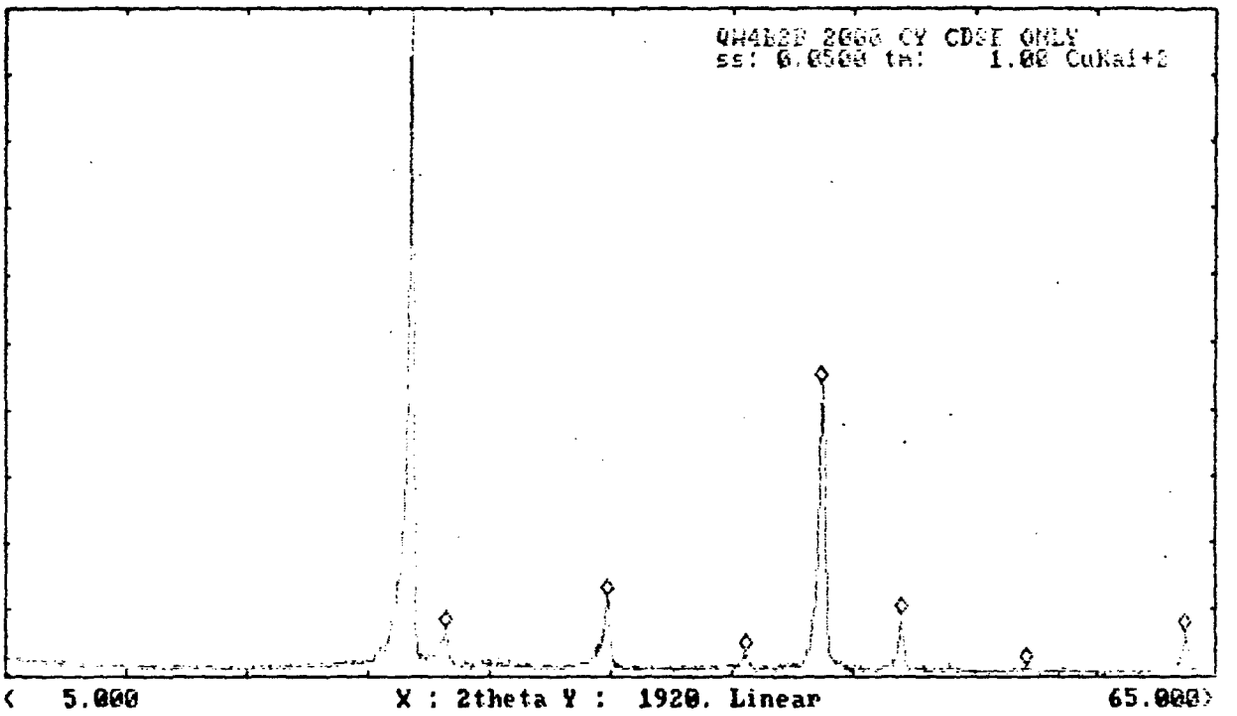

Figure 1. X-ray diffraction pattern of CdSe grown on glass plate.

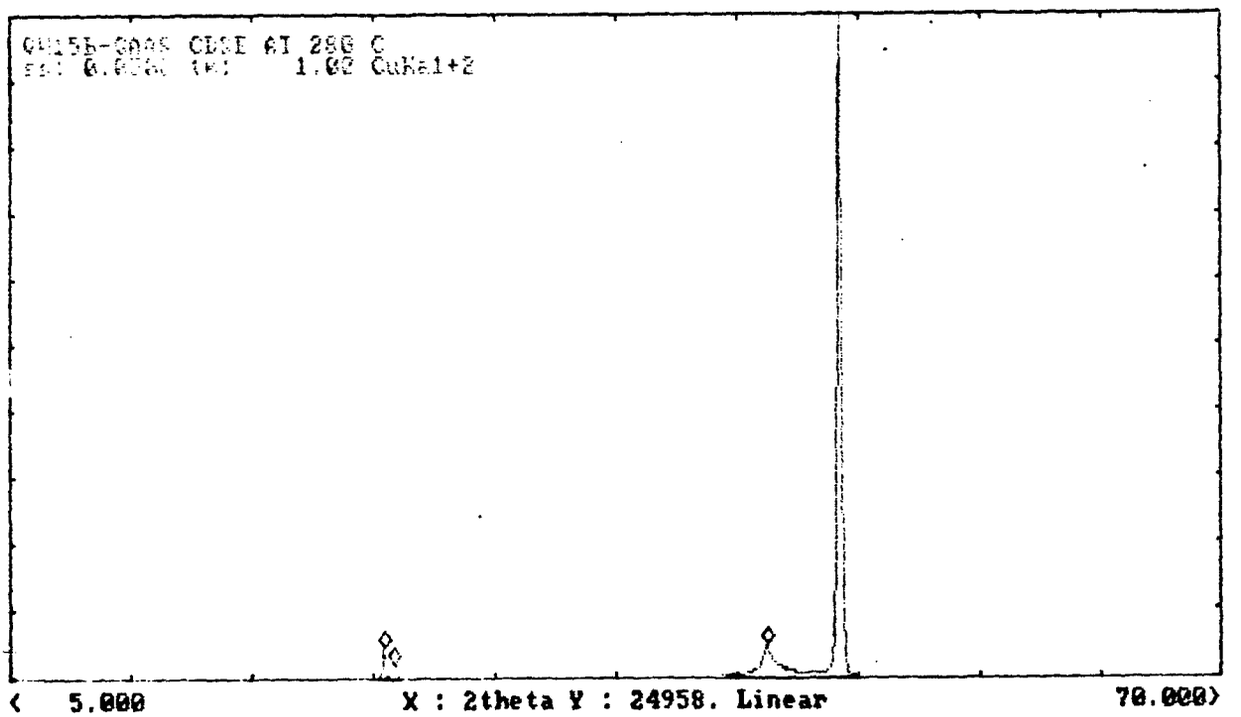

Figure 2. X-ray diffraction pattern of CdSe grown on GaAs wafer.