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ROME LABORATORY ANALYSIS OF COMPONENTS FOR ELECTRONIC TECHNOLOGIES FOR CLEANING IN 1996 AND BEYOND

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13. ABSTRACT (Maximum 200 words)

In the past, the manufacture of military microelectronics employed ozone depleting substances (ODS) during removal of solder fluxes from printed circuit (PC) boards. These ODS are environmentally unfriendly and were banned from use (Montreal Protocol) starting 1 Jan 96. Alternate flux removal technologies were studied by a Tri-Service, NASA, EPA, Industry, and Academia (GTRI) team. RL/ERDR was the Air Force representative on this team and was tasked with analysis of components from PC boards that had been processed with alternative cleaning methods and then stressed per test schedule. This effort served as a feasibility demonstration of producing reliable military microelectronics without the use of ODS. All boards in the test matrix were assembled with the different soldering technologies under study and were cleaned with the various chemistries proposed to replace ODS currently used. The matrix includes Mil, commercial, plastic and special ceramic coated dual NAND gates, Op-amps, and timer devices. Environmental Step-Stress (ESS) testing of boards was completed and selected parts removed for analysis at RL/ERDR. Within the limited scope of the examinations and testing, no clear cleaning chemistry dependent reliability or potential reliability problems were detected.

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SECTION I

PROGRAM OVERVIEW AND GENERAL CONCLUSIONS

I. OBJECTIVE: The objective of this effort was to perform detailed physical and electrical examination of devices employed in the "ELECTRONIC TECHNOLOGIES OR CLEANING IN 1996 & BEYOND" effort to evaluate solder flux cleaning processes that did not employ the use of Ozone Depleting Substances (ODS). This was to be accomplished by comparison of candidate processes to the baseline CFC process.

II. DESCRIPTION: The manufacture of military microelectronics currently employs ozone depleting substances(ODS) during removal of solder fluxes from printed circuit (PC) boards. These ODS are environmentally unfriendly and have been banned from use (Montreal Protocol) starting 1Jan96. Alternate flux removal technologies were studied by an ARPA funded Tri-Service, NASA, EPA, Industry, and Academia (Georgia Institute of Technology) team. RL/ERDR was the Air Force representative on this team and, as such, was tasked with analysis of components from PC boards that were processed with both industrial standard and alternative cleaning methods and then were subjected to temperature cycling for 20 cycles, from -45°C to +85°C at 15°C/minute with a 30 minute hold at each extreme followed by ESS (Environmental Stress Screening) per the program schedule of testing of seven cleaning chemistries (Table 1) under four separate temperature/humidity conditions (Table II) for 1000 hours and, due to time constraints, three others under one temperature/humidity condition (Table III) for only 672 hours. This effort served as a feasibility demonstration of producing reliable military microelectronics without the use of ODS and determined the feasibility of using commercial practices to produce military hardware. Technology developed during this effort is to be tailored to military, medical, and commercial applications.

III. ACCOMPLISHMENTS: Rome Laboratory/ERDR was able to provide RWOH Program devices to populate the test boards (contributors were Dow Corning and Wright Laboratory/MLSA) and recommended military and commerical control devices. Electrical and physical device analyses were performed on those devices stressed by temperature/humidity test condition B as well as an anomaly encountered during ESS. A report was forwarded to the Georgia Institute of Technology for inclusion in the overall effort report to ARPA. Rome Laboratory/ERDR will continue in-house efforts in order to perform more extensive device testing of ODS program devices.

Table I. SEVEN CHEMISTRIES TESTED UNDER ALL TEMP/HUMIDITY CONDITIONS

CFC(Control)
Semiaqueous A
Low Solids A
Water Soluble Flux A
Water Soluble Flux B
Low Solids B
Controlled Atmosphere

Table II. CHEMISTRIES TESTED TO TEMP/HUMIDITY CONDITION B

Hughes RADS*
Aqueous Detergent
Semiaqueous B

* Reactive Aqueous Defluxing System

Table III. TEST CONDITIONS

Condition	Temp, °C	RH
A	50	85
B	85	85
C	85	50
D	50	50

IV. PROCEDURE: The 85C/85% RH stressed devices (U19-U27), along with the only anomaly (Board SN 012, Part U23) detected during ESS testing, were selected for analysis (see Table IV). The 85C/85%RH test condition, in general, is the most stringent environmental stress applied to the program devices. The active device locations were populated by devices from the Reliability Without Hermeticity (RWOH) program that employed a special ceramic device overcoat in lieu of hermetic packaging, and commercial hermetic and plastic equivalents. Because of broken parts, missing parts, and limited availability of the RWOH parts, some portions of the test matrix, in particular the SEMIA, RADS, and DET chemistries, are incomplete. All devices were of the CMOS 4011 type. However, there were physical and packaging differences between the specially manufactured RWOH devices and the commercially procured version. All of the RWOH devices had been subjected to severe environmental test exposures along with having been soldered to RWOH test boards and then removed by desoldering prior to use in this effort. Table V details the test board component information. After removal of the parts from the test boards at Georgia Tech, the subject devices were delivered to Rome Laboratory. All devices were then visually inspected and electrically tested. The results of these examinations are found in Section II to this report. The devices were then examined for package seal integrity. Hermetic devices were leak tested per Test Method 1014(SEAL) of MIL-STD-883D (see Section III) while the plastic devices underwent acoustic analysis. The results of the plastic device testing, along with a brief description of the acoustic analysis procedure, appear in Section IV.

V. CONCLUSIONS: Within the limited scope of the examinations and testing, no clear cleaning chemistry dependent reliability or potential reliability problems were detected during Rome Laboratory analysis.

VI. FUTURE WORK: Remaining devices from the test matrix (U19-U27) components (85C/50%RH, 50C/85%RH, and 50C/50%RH) along with other active and passive devices from the remaining sections of the test boards for all stress conditions will be tested at Rome Laboratory in the future on a time available basis. If warranted, supplementary reports to this summary will be issued.

TABLE IV. 85C/85%RH PARTS FOR ANALYSIS

Serial Number	Component	Type	T/H	Chemistry	Rec'd RL
S/N 001	U19	CERAMIC S	85C/85%	CFC	Y= Yes
S/N 001	U20	CERAMIC A	85C/85%	CFC	Y
S/N 001	U21	RWOH S	85C/85%	CFC	Y
S/N 001	U22	RWOH A	85C/85%	CFC	Y
S/N 001	U23	PLASTIC S	85C/85%	CFC	Y
S/N 001	U24	PLASTIC A	85C/85%	CFC	Y
S/N 001	U25	RWOH	85C/85%	CFC	Y
S/N 001	U26	CERAMIC	85C/85%	CFC	Y
S/N 001	U27	PLASTIC	85C/85%	CFC	Y
S/N 012	U23	PLASTIC		CFC	FAILED
S/N 031	U19	PLASTIC S	85C/85%	CONTROL	Y
S/N 031	U20	PLASTIC A	85C/85%	CONTROL	Y
S/N 031	U21	RWOH S	85C/85%	CONTROL	Y
S/N 031	U22	RWOH A	85C/85%	CONTROL	Y
S/N 031	U23	CERAMIC S	85C/85%	CONTROL	Y
S/N 031	U24	CERAMIC A	85C/85%	CONTROL	Y
S/N 031	U25	RWOH	85C/85%	CONTROL	Y
S/N 031	U26	CERAMIC	85C/85%	CONTROL	BROKEN
S/N 031	U27	PLASTIC	85C/85%	CONTROL	Y
S/N 081	U19	PLASTIC S	85C/85%	SEMIB	MISSING
S/N 081	U20	PLASTIC A	85C/85%	SEMIB	MISSING
S/N 081	U21	RWOH S	85C/85%	SEMIB	Y
S/N 081	U22	RWOH A	85C/85%	SEMIB	Y
S/N 081	U23	CERAMIC S	85C/85%	SEMIB	Y
S/N 081	U24	CERAMIC A	85C/85%	SEMIB	Y
S/N 081	U25	RWOH	85C/85%	SEMIB	Y
S/N 081	U26	CERAMIC	85C/85%	SEMIB	Y
S/N 081	U27	PLASTIC	85C/85%	SEMIB	Y
S/N 090	U19	PLASTIC S	85C/85%	WSB	Y
S/N 090	U20	PLASTIC A	85C/85%	WSB	Y
S/N 090	U21	RWOH S	85C/85%	WSB	Y
S/N 090	U22	RWOH A	85C/85%	WSB	Y
S/N 090	U23	CERAMIC S	85C/85%	WSB	Y

TABLE IV(CONT.). 85C/85%RH PARTS FOR ANALYSIS

Serial Number	Component	Type	T/H	Chemistry	Rec'd RL
S/N 090	U24	CERAMIC A	85C/85%	WSB	Y
S/N 090	U25	RWOH	85C/85%	WSB	Y
S/N 090	U26	CERAMIC	85C/85%	WSB	Y
S/N 090	U27	PLASTIC	85C/85%	WSB	Y
S/N 109	U19	PLASTIC	85C/85%	SEMIA	Y
S/N 109	U20	CERAMIC	85C/85%	SEMIA	Y
S/N 111	U19	PLASTIC S	85C/85%	LOW RES	Y
S/N 111	U20	PLASTIC A	85C/85%	LOW RES	Y
S/N 111	U21	RWOH S	85C/85%	LOW RES	Y
S/N 111	U22	RWOH A	85C/85%	LOW RES	Y
S/N 111	U23	CERAMIC S	85C/85%	LOW RES	Y
S/N 111	U24	CERAMIC A	85C/85%	LOW RES	Y
S/N 111	U25	RWOH	85C/85%	LOW RES	Y
S/N 111	U26	CERAMIC	85C/85%	LOW RES	Y
S/N 111	U27	PLASTIC	85C/85%	LOW RES	Y
S/N 131	U19	PLASTIC S	85C/85%	WSA	Y
S/N 131	U20	PLASTIC A	85C/85%	WSA	Y
S/N 131	U21	RWOH S	85C/85%	WSA	Y
S/N 131	U22	RWOH A	85C/85%	WSA	Y
S/N 131	U23	CERAMIC S	85C/85%	WSA	Y
S/N 131	U24	CERAMIC A	85C/85%	WSA	Y
S/N 131	U25	RWOH	85C/85%	WSA	Y
S/N 131	U26	CERAMIC	85C/85%	WSA	Y
S/N 131	U27	PLASTIC	85C/85%	WSA	Y
S/N 191	U19	PLASTIC S	85C/85%	LRB	BROKEN
S/N 191	U20	PLASTIC A	85C/85%	LRB	Y
S/N 191	U21	RWOH S	85C/85%	LRB	Y
S/N 191	U22	RWOH A	85C/85%	LRB	Y
S/N 191	U23	CERAMIC S	85C/85%	LRB	Y
S/N 191	U24	CERAMIC A	85C/85%	LRB	Y
S/N 191	U25	RWOH	85C/85%	LRB	Y
S/N 191	U26	CERAMIC	85C/85%	LRB	Y
S/N 191	U27	PLASTIC	85C/85%	LRB	Y

TABLE IV(CONT.). 85C/85%RH PARTS FOR ANALYSIS

Serial Number	Component	Type	T/H	Chemistry	Rec'd RL
S/N 200	U19	RWOH	85C/85%	RADS	Y
S/N 200	U20	PLASTIC	85C/85%	RADS	Y
S/N 200	U21	CERAMIC	85C/85%	RADS	Y
S/N 200	U22	RWOH	85C/85%	RADS	Y
S/N 224	U19	PLASTIC	85C/85%	DET	Y
S/N 224	U20	CERAMIC	85C/85%	DET	Y

TABLE V. COMPONENT LOCATION & STRESS INFORMATION

COMPONENT INFORMATION FOR ALL BOARD S/N'S EXCEPT S/N 001

COMPONENT	TYPE	PACKAGE	STRESS
U19	RWOH(CONTROL) 4011(1)	Plastic	Salt Spray
U20	RWOH(CONTROL) 4011(1)	Plastic	Autoclave
U21	RWOH(COATED) 4011(1)	Plastic	Salt Spray
U22	RWOH(COATED) 4011(1)	Plastic	Autoclave
U23	RWOH(CONTROL) 4011(2)	SB Ceramic	Salt Spray
U24	RWOH(CONTROL) 4011(2)	SB Ceramic	Autoclave
U25	RWOH(COATED) 4011(1)	Plastic	None
U26	CD4011BMJ	Ceramic	None
U27	CD4011BCN	Plastic	None

(1) MM46B11 PDIP
(2) SIDE-BRAZED METAL LID DIP

COMPONENT INFORMATION FOR BOARD S/N 001

COMPONENT	TYPE	PACKAGE	STRESS
U19	RWOH(CONTROL) 4011(2)	SB Ceramic	Salt Spray
U20	RWOH(CONTROL) 4011(2)	SB Ceramic	Autoclave
U21	RWOH(COATED) 4011(1)	Plastic	Salt Spray
U22	RWOH(COATED) 4011(1)	Plastic	Autoclave
U23	RWOH(CONTROL) 4011(1)	Plastic	Salt Spray
U24	RWOH(CONTROL) 4011(1)	Plastic	Autoclave
U25	RWOH(COATED) 4011(1)	Plastic	None
U26	CD4011BMJ	Ceramic	None
U27	CD4011BCN	Plastic	None

(1) MM46B11 PDIP
(2) SIDE-BRAZED METAL LID DIP

STRESS **A**: Sequential Autoclave Exposure: 24 hours Autoclave @ 121°C, 100%RH, 1 atmg; plus 200 Temp cycles @ 150 to -65°C: followed by 1000 hours of Autoclave Exposure.

STRESS **B**: Sequential Salt Fog Exposure: 24 hours Autoclave @ 121°C, 100%RH, 1atmg; plus 1000 Temp cycles @ 150 to -65°C: followed by 24 hours of Salt Fog Exposure @ 35°C, 0.5% NaCl.

SECTION II

VISUAL INSPECTION AND ELECTRICAL TESTING OF ODS PARTS

This report summarizes the visual inspection and subsequent Automated Test Equipment (ATE) and Bench testing done on the ODS parts.

I. Visual Inspection:

All devices were inspected for any evidence of moisture ingress or damage which might have occurred due to differences in chemistries used or to the accelerated stress tests done on the devices. Detailed inspections were made for several devices and the results were noted on data sheets. The visual Inspection notes were handwritten and are not included in this report. Interested parties may contact the Rome Laboratory author for a copy of the notes. In general, there were only a few significant observations.

One observation was that several devices had bent, short, or missing external pins. These looked like they were damaged by the removal process (de-soldering from the boards on which they were mounted during ESS tests), and did not appear to be due to corrosion or stress related degradation. There could have been some damage during shipping also, as the devices were shipped in groups or singly in conductive antistatic bags, since the leads were not imbedded in foam or carriers to prevent damage. Some devices had via hole collars from the PC cards they were mounted in still attached to one or more leads.

Another observation was that many plastic encapsulated devices had broken plastic to metal meniscus area seals. Many of these also had discolorations emanating from the lead area out into the plastic around the leads. The discolorations may have been due to moisture penetration and the meniscus separations might have been due to temperature cycling during the stresses. However, some of these conditions might have been caused by heat and mechanical force during removal from the PC cards to which they were soldered during accelerated testing. This question could be resolved by inspecting any similar devices which have seen similar accelerated stress tests, but which have not been de-soldered, and by doing an experiment involving inspecting, soldering, removing, and inspecting some similar devices which have not seen stresses.

A third observation was that some devices had regions of brownish discoloration on metal areas close to the package. This is probably minor corrosion of the iron in the Kovar lead frame components. Some of the devices had seen considerable stress even before the ODS effort. One thing which could be done is to check whether there was more corrosion of those devices which had seen this additional prior stress.

II. Electrical Testing: All of the devices had been functionally tested while on the boards before shipping to RL, and they had all passed. After visual inspection at RL, all of the devices were ATE tested at room temperature. DC parametric and functional

tests were done using specification limits taken from mil-spec slash sheets for similar devices, even though there was a mixture of part quality grades. Several devices failed, but were later found to be ones which had broken or missing pins. Some of these, and others as well, had additional marginal measurements, e.g. input currents just over the 100pa limit or low output voltage just under the 0V lower limit used by the ATE test program.

The devices which had bent, broken, or pins missing and had shown problems during the first electrical test were then soldered into sockets and retested. Some passed all tests while others still had marginal measurements of some parameters. A curve tracer was then used to check whether the marginal Iin, Vin, or Iss measurements were over-ranged instead of just marginal. The results showed that there were no catastrophic failures, only very marginal ones.

None of the subject devices are true failures indicative of damage by the ODS program chemistry differences and life test stresses. Each had only one or a few marginal input current measurements (a 100pa limit was used in the test program) or output low voltages (for which 0.000v was the minimum limit used, and typical measured values were ≤2mv). The only suspect failed parameters involved input currents which were just above the 100pa compliance limit, or Vin measurements for which output levels measured -0.001v instead of the typical 0.002v.

Each of these marginal devices was checked on a curve tracer to see if there were any catastrophic failures which were really over-ranged rather than just above or below the limits. For each device, Iinl, Iinh and Iss was checked for each of the four binary states for each gate individually. This was done with Vdd=15v, using a manual switchbox. All of the measurements were less than about 200pa. During these measurements, the curve tracer was set to a 1na per division scale, and 100pa was resolvable. Although the output voltages were not checked during the curve tracer tests, none of the devices which had marginal Vout measurements had failed all the Vout tests for the same output (i.e. for different Vdd's) during the ATE tests. This proves that there were no opens or shorts at output pins, and suggests that the marginal measurements of -0.001mv were not significant. These devices are not failures, and there was no need to do further electrical testing.

One device was a 747 dual op-amp rather than a 40ll quad two input nand gate (SN 012,U23). This device was inadvertently included in the group of devices which were tested as 4011s, and it failed, as would be expected. Subsequently it was tested as a 747, and it appeared to be functional. Input offset voltages were measured for both op-amps in the package, and were OK. It was tested in an amplifier circuit with gain, and it operated properly. It was apparently not damaged by the testing as a 4011, and it is classified a retest OK. The ATE test report (SECTION IIA), Electrical Test Failures(SECTION IIB), and op-amp test report (SECTION IIC) follow.

SECTION IIA

ATE TEST REPORT:

OZONE

DEPLETING

SUBSTANCES

(ODS)

MICROCIRCUIT DEVICE

ELECTRICAL TEST RESULTS

UTILIZING

MIL-M-38510/05001 & MIL-M-38510/05051

1 DEVICE BACKGROUND INFORMATION

The Rome Laboratory/ERDD branch was requested by ERDR to perform electrical tests on a quantity of 68 microcircuit devices. These devices were sent to Rome Laboratory for analysis as part of an ongoing program to assess the effect of various chemical processes using non-ozone depleting substances in the system fabrication process.

2 DEVICE DESCRIPTION

ERDD was informed that the classification of the devices to be analyzed are Digital CMOS Microcircuits. The specific circuit type was identified as Quadruple 2-Input NAND Gates referenced as generic/industry device type 4011A and/or 4011B.

3 DEVICE ELECTRICAL TESTING PERFORMED

Based upon the initial information received on the device type to be electrically tested, ERDD established electrical testing based upon MIL-M-38510/05001 and MIL-M-38510/05051. Both standards are for Digital CMOS Microcircuits of the circuit type Quadruple 2-Input NAND Gate. MIL-M-38510/05001 covers generic/industry device type 4011A and MIL-M-38510/05051 covers generic/industry device type 4011B. An electrical test program was developed for testing these device types on the ERDD Teradyne J953 Automated Microcircuit Test System. One test program was utilized for electrical testing to both Military specifications. There were 25 distinct electrical test types performed on each of the 68 devices at a temperature of 25C.

TABLE 1 provides a listing of the electrical tests performed with the min and max limits utilized. In some cases the test limits, ranges and electrical tests contained in one specification differed with respect to the other. The test program developed attempted to encompass as many electrical tests as possible from both specifications. Therefore, limitations and/or ranges were expanded and electrical tests which may not have been required (specification dependent) were applied to all devices.

The test number field of TABLE 1 assigns a unique number to each electrical test performed. Notice that there is a range of test numbers associated with most of the electrical tests. This range represents the number of times that particular test is required to be performed on each device. As an example, the Vic (pos) electrical test is performed 8 times per device. The first test of Vic (pos) is assigned test number 2001, the second test of Vic (pos) is assigned test number 2002, etc. The repetition of an electrical test on a device is required to test multiple components and/or identical circuits within a device.

The device circuit column of TABLE 1 identifies which device type is applicable to the electrical test being conducted. For example, the Vic (pos) test is specified for both the 4011A and 4011B devices, whereas, the Voh4 electrical test is required only for the 4011B devices. Therefore, if a device such as a 4011A were to fail the Voh4 test, the device may not be considered a failure since the Voh4 test is only for the 4011B device. All 68 devices were subjected to the electrical tests as listed in TABLE1.

TABLE 1

Mil-M-38510/05001 & Mil-M-38510/05051 Tests and Limits

Tests Performed and Specification Limits Used @ 25C

Test	Test Number	Min	Max	Unit	Device Circuit
Vic (pos)	2001 - 2008	0.0	1.5	Vdc	4011A - 4011B
Vic (neg)	2111 - 2018	-1.5	0.0	Vdc	4011A - 4011B
Iddh	2021	0.0	80	mA	4011A - 4011B
Voh1	2031 - 2038	4.2	5.0	Vdc	4011A - 4011B
Voh2	2038 - 2045	4.95	5.5	Vdc	4011A - 4011B
Voh3	2051 - 2058	11.25	13.0	Vdc	4011A - 4011B
Voh4	2061 - 2068	14.95	16.0	Vdc	4011B
Vol1	2071 - 2074	0.0	0.5	Vdc	4011A
Vol2	2081 - 2084	0.0	0.05	Vdc	4011A - 4011B
Vol3	2091 - 2094	0.0	1.25	Vdc	4011A - 4011B
Vih1	2111 - 2114	0.0	0.5	Vdc	4011B
Vih2	2121 - 2124	0.0	1.0	Vdc	4011B
Vih3	2131 - 2134	0.0	1.5	Vdc	4011B
Vil1	2141 - 2152	4.5	5.5	Vdc	4011B
Vil2	2161 - 2172	9.0	10.0	Vdc	4011B
Vil3	2181 - 2192	13.5	15.0	Vdc	4011B
Iol1	2201 - 2204	0.51	1.5	mAdc	4011B
Iol2	2211 - 2214	3.4	10	mAdc	4011B
Ioh1	2221 - 2228	-1.5	-.510	mAdc	4011B
Ioh2	2231 - 2238	-10.0	-3.4	mAdc	4011B
Iih2	2241 - 2248	0.0	1.0	nA	4011A - 4011B
Iil1	2251 - 2258	-1.0	0.0	nA	4011A - 4011B
tPHL	2261 - 2268	10	200	ns	4011A - 4011B
tPLH	2271 - 2278	8	150	ns	4011A - 4011B
Functional	2281	N/A	N/A	N/A	4011A - 4011B

4 DEVICE PACKAGE VISUAL INSPECTION

A device package visual inspection was performed by ERDD after results of the electrical tests indicated that further investigation was needed. This inspection was for identifying the exact device circuit types (by means of package markings/identification), device packaging (by means of visual and/or package markings/identification) and device package condition. A summary of the device package visual inspection for identifying the device circuit types, associated quantities and device packaging is provided in TABLE 2.

TABLE 2

DEVICE PACKAGE INFORMATION

DEVICE PACKAGE IDENTIFICATION	QTY	DEVICE PACKAGING
UNKNOWN	14	14 PIN DIP CERAMIC METAL LID
NATIONAL 1892 MM46B11 CERAMIC CTG	23	14 PIN DIP CERAMIC
NATIONAL 1892 MM46B11 STANDARD	11	14 PIN DIP UNKNOWN
NATIONAL S2D9347A CD4011BMJ/883 QS	8	14 PIN DIP CERAMIC
NATIONAL P9342 CD4011BCN MM5611BN	10	14 PIN DIP PLASTIC
NATIONAL S2D9352D CD4011BMJ/883 QS	1	14 PIN DIP CERAMIC
NATIONAL S3B9346D LM747J/883	1	14 PIN DIP CERAMIC
SAMPLE TOTAL	**68**	

As TABLE 2 indicates, the device visual inspection showed that there were 7 different device package types identified. All devices were packaged in 14 pin dual-in-line packages (DIP) with a majority of the device packaging being hermetic material such as ceramic. However, it should be noted that the device packaging was mixed. Both ceramic and plastic device packages were present.

No device package identification markings were found on 14 devices. The device package identification for these devices has been labeled Unknown. It was assumed by ERDD from the electrical test results that these devices were of the Quadruple 2-

Input NAND Gate circuit type. The Unknown devices were also the only devices with a metal lid mounted on a ceramic casing. The device package identification was ink stamped on the metal lid, however, the markings were not legible. The ink stamp on these device samples is easily removed after handling or when heat is applied for extended periods of time such as when the device is operational.

There were 23 - National 1892 MM46B11 Ceramic CTG and 11 - National 1892 MM46B11 Standard devices. ERDD found that the National Part Type MM4611 is associated with MIL-M-38510/05001, however, ERDD was unable to match the MM46B11 package identifications with either a National or MIL-M-38510 Specification. It was *assumed* that the National 1892 MM46B11 Ceramic CTG is packaged in ceramic. However, it was uncertain about the device packaging of the National 1892 MM46B11 Standard. Because ERDD was unsure what "Standard" meant, these device packages were labeled as unknown. Further investigation is needed for identifying exactly what these devices and packaging are. From the results of the electrical tests performed, it was assumed these devices were Quadruple 2-Input NAND Gate circuit types.

There were 8 - National S2D9347A CD4011BMJ/883 QS, 10 - National P9342 CD4011BCN MM5611BN and 1 - National S2D9352D CD4011BMJ/883 QS devices. These devices are 4011B Quadruple 2-Input NAND Buffered B Series Gate circuit types and were electrically tested accordingly.

One device out of the 68 received was discovered to be a National S3B9346D LM747J/883 which is an Operational Amplifier circuit type. Results of the electrical testing performed as a 4011 device type indicate that this device was a total failure. The device package visual inspection confirmed that this device was not of the same classification as the others.

With the exception of the devices identified as unknown and the one device that was not of the same classification as the others, TABLE 2 and the electrical test results indicate that the remaining devices are of the generic/industry type 4011B. The electrical tests will also show that the devices labeled unknown should also be assumed to be of the 4011B device type.

During the device package visual inspection, the following package conditions were observed: Package discoloration due to heat, chipped casings, excessive solder on device lead pins, device lead pins with evidence of circuit board mounting pads and runs attached, device lead pin fatigue, device lead pins bent, device pin leads bent going into the device casing, device lead pins short in length, device lead pins missing, device package markings/identification not legible, and one instance of a 747 device type were observed.

The results of removing the devices from a circuit board can cause what was visually observed, and unfortunately in this case it has introduced some uncertainty about the effects of testing. For example, some device pins were bent and missing as received by Rome Laboratory. It is unknown whether the leads were excessively stressed by fatigue due to temperature cycling, or by removal from the boards. Some were definitely stressed by removal from the boards, since many devices had bent pins, pins which were shorter because they had been clipped, or pins which were broken off. Some device pins which were bent as received were straightened at Rome Laboratory and broke off during this one bend. The devices were received in groups loose inside conductive bags, so it is also unknown if they were damaged in transit or handling.

The devices each had a unique identification which seemed to identify the board and device location on that board. As an example, a device came from a board identified as SN001 and was located on that board in device location U19. A pattern was noticed by ERDD which indicated that specific devices were utilized for specific locations regardless of the board. As an example, location U25 always utilized device package identification, National 1892 MM46B11 ceramic CTG and U19 utilized device package identification, National 1892 MM46B11 Standard. There were some inconsistencies to this pattern but in general this was what was observed. If a pattern exists, this may suggest that there are electrical differences between the 7 device package identifications utilized on these boards.

TABLE 3 lists each device received by ERDD identified by the board and location on that board where the device resides. In addition, each device package identification is listed and a comment field listing the device lead pin condition prior to performing the electrical tests included. Note that TABLE 3 package comments may indicate that some of the device lead pins were identified as acceptable for electrical testing however, nearly all devices had lead pins that were short, bent, or missing.

Note: An asterisk in front of the system identification in TABLE 3 under the SYSTEM column denotes that the device experienced no electrical failures during the electrical testing. TABLE 3 will indicate that 27 of the 68 devices tested experienced no electrical failures.

TABLE 3			
DEVICE INVENTORY			
SYSTEM	LOC	DEVICE PACKAGE ID	PACKAGE NOTES
* SN001	U19	UNKNOWN	LEAD PINS OK TO TEST
SN001	U20	UNKNOWN	LEAD PINS OK TO TEST
SN001	U21	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
* SN001	U22	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
* SN001	U23	NAT 1892 MM46B11 STANDARD	LEAD PINS OK TO TEST
SN001	U24	NAT 1892 MM46B11 STANDARD	LEAD PINS OK TO TEST
* SN001	U25	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN001	U26	NAT S2D9347A CD4011BMJ/883 QS	LEAD PINS OK TO TEST
* SN001	U27	NAT P9342 CD4011BCN MM5611BN	LEAD PINS OK TO TEST
SN012	U23	NAT S3B9346D LM747J/883	LEAD PINS OK TO TEST
* SN031	U19	NAT 1892 MM46B11 STANDARD	LEAD PIN 7 MISSING
SN031	U20	NAT 1892 MM46B11 STANDARD	LEAD PINS OK TO TEST
SN031	U21	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN031	U22	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
* SN031	U23	UNKNOWN	PINS SHORT LENGTH
SN031	U24	UNKNOWN	TOO SHORT TO TEST
* SN031	U25	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN031	U27	NAT P9342 CD4011BCN MM5611BN	LEAD PIN 14 MISSING
* SN081	U21	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN081	U22	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN081	U23	UNKNOWN	LEAD PINS OK TO TEST
SN081	U24	UNKNOWN	LEAD PIN 7 MISSING
* SN081	U25	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN081	U26	NAT S2D9347A CD4011BMJ/883 QS	LEAD PINS OK TO TEST
* SN081	U27	NAT P9342 CD4011BCN MM5611BN	LEAD PINS OK TO TEST
SN081	U23	UNKNOWN	LEAD PINS OK TO TEST
SN081	U24	UNKNOWN	LEAD PIN 7 MISSING
* SN081	U25	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN081	U26	NAT S2D9347A CD4011BMJ/883 QS	LEAD PINS OK TO TEST
* SN081	U27	NAT P9342 CD4011BCN MM5611BN	LEAD PINS OK TO TEST
* SN090	U19	NAT 1892 MM46B11 STANDARD	LEAD PINS OK TO TEST
SN090	U20	NAT 1892 MM46B11 STANDARD	LEAD PINS OK TO TEST
* SN090	U21	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST

TABLE 3 (con't)			
DEVICE INVENTORY			
SN090	U22	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN090	U23	UNKNOWN	LEAD PINS SHORT
SN090	U24	UNKNOWN	LEAD PINS SHORT
SN090	U25	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN090	U26	NAT S2D9347A CD4011BMJ/883 QS	LEAD PINS OK TO TEST
* SN090	U27	NAT P9342 CD4011BCN MM5611BN	LEAD PINS OK TO TEST
* SN109	U19	NAT P9342 CD4011BCN MM5611BN	LEAD PINS OK TO TEST
SN109	U20	NAT S2D9347A CD4011BMJ/883 QS	LEAD PINS OK TO TEST
SN111	U19	NAT 1892 MM46B11 STANDARD	LEAD PINS OK TO TEST
* SN111	U20	NAT 1892 MM46B11 STANDARD	LEAD PIN 7 MISSING
* SN111	U21	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN111	U22	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN111	U23	UNKNOWN	PINS 7 & 8 MISSING
SN111	U24	UNKNOWN	LEAD PINS OK TO TEST
* SN111	U25	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN111	U26	NAT S2D9347A CD4011BMJ/883 QS	LEAD PINS OK TO TEST
* SN111	U27	NAT P9342 CD4011BCN MM5611BN	LEAD PINS OK TO TEST
SN131	U19	NAT 1892 MM46B11 STANDARD	PINS 5, 7 & 14 MISSING
SN131	U20	NAT 1892 MM46B11 STANDARD	LEAD PINS OK TO TEST
* SN131	U21	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN131	U22	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
* SN131	U23	UNKNOWN	LEAD PINS OK TO TEST
SN131	U24	UNKNOWN	LEAD PIN 7 MISSING
SN131	U25	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN131	U26	NAT S2D9347A CD4011BMJ/883 QS	LEAD PIN 1 MISSING
SN131	U27	NAT P9342 CD4011BCN MM5611BN	PINS 1 & 14 MISSING
SN191	U20	NAT 1892 MM46B11 STANDARD	LEAD PIN 7 MISSING
SN191	U21	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
* SN191	U22	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
SN191	U23	UNKNOWN	LEAD PIN 7 MISSING
* SN191	U24	UNKNOWN	LEAD PINS OK TO TEST
SN191	U25	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
* SN191	U26	NAT S2D9347A CD4011BMJ/883 QS	LEAD PINS OK TO TEST
SN191	U27	NAT P9342 CD4011BCN MM5611BN	LEAD PIN 1 MISSING
* SN200	U19	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
* SN200	U20	NAT P9342 CD4011BCN MM5611BN	1, 2, 7 & 14 MISSING

TABLE 3 (con't)			
DEVICE INVENTORY			
SN200	U21	NAT S2D9347A CD4011BMJ/883 QS	LEAD PINS OK TO TEST
SN200	U22	NAT 1892 MM46B11 CERAMIC CTG	LEAD PINS OK TO TEST
* SN224	U19	NAT P9342 CD4011BCN MM5611BN	LEAD PINS OK TO TEST
SN224	U20	NAT S2D9352D CD4011BMJ/883 QS	LEAD PINS OK TO TEST
TOTAL = 68			

5 DEVICE FAILURE SUMMARY

Table 4 summarizes the device failures that were detected while performing the electrical tests. There is a note under each electrical test performed as listed in TABLE 4 in the column labeled ELECTRICAL TEST which indicates the amount of times that particular test is required to be performed on each device. As an example, the Vic (pos) electrical test is performed 8 times per device. The number of test failures per device in TABLE 4 are the quantity of failures detected with respect to the limits shown in TABLE 1.

TABLE 4			
DEVICE FAILURE SUMMARY			
ELECTRICAL TEST	**FAILED SYSTEM**	**FAILED LOCATION**	**TEST FAILURES /DEVICE**
Vic (pos)	SN012	U23	5
(8 TESTS DONE PER DEVICE)	SN031	U24	1
Vic (neg)	SN012	U23	2
(8 TESTS DONE PER DEVICE)			
Voh1	SN012	U23	5
(8 TESTS DONE PER DEVICE)	SN031	U24	1
Voh2	SN012	U23	5
(8 TESTS DONE PER DEVICE)	SN031	U24	1
Voh3	SN012	U23	6
(8 TESTS DONE PER DEVICE)			

TABLE 4(cont.)			
DEVICE FAILURE SUMMARY			
ELECTRICAL TEST	**FAILED SYSTEM**	**FAILED LOCATION**	**TEST FAILURES /DEVICE**
Voh4	SN012	U23	8
(8 TESTS DONE PER DEVICE)			
Vol1	SN012	U23	4
(4 TESTS DONE PER DEVICE)			
Vol2	SN012	U23	4
(4 TESTS DONE PER DEVICE)	SN081	U22	1
	SN081	U24	1
	SN081	U26	1
	SN090	U22	2
	SN109	U20	1
	SN111	U24	1
Vol3	SN012	U23	4
(4 TESTS DONE PER DEVICE)	SN109	U20	1
Vih1	SN001	U21	1
(4 TESTS DONE PER DEVICE)	SN001	U26	1
	SN012	U23	4
	SN031	U20	1
	SN031	U27	1
	SN081	U22	1
	SN081	U23	1
	SN081	U24	1
	SN090	U22	1
	SN090	U23	1
	SN090	U24	1
	SN090	U25	1
	SN111	U19	1
	SN111	U22	2
	SN111	U24	2
	SN111	U26	1
	SN131	U19	1

TABLE 4(cont.)			
DEVICE FAILURE SUMMARY			
ELECTRICAL TEST	FAILED SYSTEM	FAILED LOCATION	TEST FAILURES /DEVICE
	SN131	U25	1
	SN131	U26	2
	SN131	U27	3
	SN191	U21	1
	SN191	U23	1
	SN191	U27	1
	SN200	U21	1
	SN200	U22	1
	SN224	U20	1
Vih2	SN012	U23	4
(4 TESTS DONE PER DEVICE)	SN031	U27	1
	SN081	U22	1
	SN081	U24	2
	SN090	U20	1
	SN090	U26	2
	SN111	U19	1
	SN111	U23	1
	SN131	U24	1
	SN191	U23	1
	SN191	U27	1
	SN224	U20	1
Vih3	SN012	U23	4
(4 TESTS DONE PER DEVICE)	SN031	U27	1
	SN090	U22	1
	SN090	U26	1
	SN111	U26	1
	SN131	U22	1
	SN131	U27	1
	SN191	U27	1
	SN200	U22	2
	SN224	U20	1

TABLE 4(cont.)			
DEVICE FAILURE SUMMARY			
ELECTRICAL TEST	**FAILED SYSTEM**	**FAILED LOCATION**	**TEST FAILURES /DEVICE**
Vil1	SN012	U23	9
(12 TESTS DONE PER DEVICE)	SN031	U24	1
Vil2	SN012	U23	12
(12 TESTS DONE PER DEVICE)	SN031	U24	1
Vil3	SN012	U23	12
(12 TESTS DONE PER DEVICE)			
Iol1	SN012	U23	4
(4 TESTS DONE PER DEVICE)			
Iol2	SN012	U23	4
(4 TESTS DONE PER DEVICE)			
Ioh1	SN012	U23	7
(8 TESTS DONE PER DEVICE)	SN031	U24	1
Ioh2	SN012	U23	8
(8 TESTS DONE PER DEVICE)	SN031	U24	1
Iih2	SN012	U23	6
(8 TESTS DONE PER DEVICE)	SN131	U26	1
Iil1	SN001	U20	1
(8 TESTS DONE PER DEVICE)	SN001	U24	1
	SN001	U26	1
	SN012	U23	6
	SN031	U20	1
	SN031	U21	1
	SN031	U22	1
	SN031	U24	1
	SN031	U27	1
	SN081	U22	1
	SN081	U24	1

TABLE 4(cont.)			
DEVICE FAILURE SUMMARY			
ELECTRICAL TEST	FAILED SYSTEM	FAILED LOCATION	TEST FAILURES /DEVICE
	SN081	U26	1
	SN090	U20	1
	SN090	U22	1
	SN090	U24	1
	SN090	U26	1
	SN109	U20	1
	SN111	U19	1
	SN111	U22	1
	SN111	U24	1
	SN111	U26	1
	SN131	U20	1
	SN131	U22	1
	SN131	U24	1
	SN131	U26	2
	SN131	U27	1
	SN191	U21	1
	SN191	U23	1
	SN191	U25	1
	SN191	U27	1
	SN200	U22	1
	SN224	U20	1
tPHL	SN012	U23	8
(8 TESTS DONE PER DEVICE)	SN031	U24	1
tPLH	SN012	U23	8
(8 TESTS DONE PER DEVICE)	SN031	U24	2
FUNCTIONAL	SN012	U23	1
(1 TESTS DONE PER DEVICE)	SN031	U24	1

6 CONCLUSIONS/RECOMMENDATIONS

The device failure summary of TABLE 4 indicates that there are two devices which failed the majority of the electrical tests performed. These devices are identified as SN012 U23 and SN031 U24. By eliminating these two devices no catastrophic device failures would be observed. It must be noted that these devices were only tested at a temperature of 25C. If these devices were to be subjected to stress due to temperature, more failures may be detected.

The electrical tests and device visual package inspection confirms that the device identified as SN012 U23 is of a different circuit type other than the expected Quadruple 2-Input NAND Gate. This device was identified to be a National S3B9346D LM747J/883 which is an Operational Amplifier circuit type which explains why it would fail tests meant for a Quadruple 2-Input NAND Gate. However, further investigation is needed if this device was mistakenly utilized in place of the 4011 device type required by the system.

The device SN031 U24 was identified as Unknown as noted in the device visual package inspection. The device visual package inspection also indicated that this device had short lead pin lengths which most likely were too short in length to properly fit into the test socket. If more data is required, ERDD recommends attaching (soldering) longer lead lengths to the existing leads and then perform a retest.

All devices passed the Functional test with the exception of the two mentioned above. The devices that passed this test plus all other electrical parametric tests were considered to be functioning properly. The remainder of the devices which passed the functional but were observed by ERDD to have one or more electrical test failures were classified as marginal. Table 4 indicates that most of the device failures detected were limited to one circuit within the device and in most cases that failure was the only one detected out of all the electrical tests performed. Regardless, these devices all passed functionally and is the reason why they were classified as marginal.

When only one device lead pin was missing, the test engineer made an attempt to place a wire into the test socket and press the wire against the lead that was missing while performing the electrical testing. In most cases this procedure was successful, however, in some cases it may have led to some of the marginal failures observed due to poor device lead contact with the test system electronics. This was only performed on devices where one lead pin was missing. ERDD recommends attaching (soldering) a lead pin if possible and then perform a retest.

ERDD performed a retest on a random sample of devices which had experienced electrical failures and as indicated by TABLE 3 had one or more lead pins missing. This random sample of devices that were retested are identified as SN031 U19,

SN031 U27, SN111 U20, SN131 U19, SN131 U27, SN191 U20, SN191 U27, and SN200 U20. Prior to retesting the device, lead pins that were missing were reattached by soldering wire when possible and then the devices were individually mounted on a socket. In some instances, the devices were soldered to the socket. Four of the eight devices after the retest experienced no electrical failures while the other four had a reduction in the electrical test failures observed. Another device identified as SN001 U22 was also retested after the device was placed into a socket. The device was reclassified from marginal to experiencing no failures.

SECTION II

ATTACHMENT IIB

ELECTRICAL TEST FAILURES

A. ELECTRICAL TEST FAILURES

This appendix lists all electrical test failures that were detected. Each electrical test performed has its own table that identifies the electrical failures detected by listing the board and location (which when both are combined is the identification of the device), the specific Test Number (as discussed previously), the Measured Value which is the actual value measured by the Teradyne J953 Automated Microcircuit Test System (the value which was not within the specification limits) and packaging information. A typical value is provided to indicate an approximate value observed by the devices which passed the electrical test.

A.1 Vic (pos) - Positive clamping Input to Vdd (Typical value = 825mV)

Vic (pos) FAILURES (TEST NO's 2001 - 2008)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2001	-819.3mV	CIRCUIT TYPE NOT 4011
SN012	U23	2002	2000.1mV	CIRCUIT TYPE NOT 4011
SN012	U23	2003	2000.1mV	CIRCUIT TYPE NOT 4011
SN012	U23	2007	2000.1mV	CIRCUIT TYPE NOT 4011
SN012	U23	2008	1587.2mV	CIRCUIT TYPE NOT 4011
SN031	U24	2005	2000.1mV	SHORT LEAD PIN LENGTH FOR TEST FIXTURE

A.2 Vic (neg) - Negative clamping Input to Vss (Typical value = -745mV)

Vic (neg) FAILURES (TEST NO's 2011 - 2018)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2012	1561.6mV	CIRCUIT TYPE NOT 4011
SN012	U23	2013	-2000.1mV	CIRCUIT TYPE NOT 4011

A.3 Iddh - Power supply current (Typical value = 20mA)

The current into the Vss supply terminal of an integrated circuit.

There were no failures.

A.4 Voh1 - High level output voltage (Typical value = 4.65V)

The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

Voh1 FAILURES (TEST NO's 2031 - 2038)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2034	3.825V	CIRCUIT TYPE NOT 4011
SN012	U23	2035	3.729V	CIRCUIT TYPE NOT 4011
SN012	U23	2036	3.668V	CIRCUIT TYPE NOT 4011
SN012	U23	2037	-4.599V	CIRCUIT TYPE NOT 4011
SN012	U23	2038	-4.597V	CIRCUIT TYPE NOT 4011
SN031	U24	2035	-0.050V	SHORT LEAD PIN LENGTH FOR TEST FIXTURE

A.5 Voh2 - High level output voltage (Typical value = 5V)

The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

Voh2 FAILURES (TEST NO's 2038 - 2045)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2041	3.828V	CIRCUIT TYPE NOT 4011
SN012	U23	2042	3.739V	CIRCUIT TYPE NOT 4011
SN012	U23	2043	3.678V	CIRCUIT TYPE NOT 4011
SN012	U23	2044	1.063V	CIRCUIT TYPE NOT 4011
SN012	U23	2045	0.589V	CIRCUIT TYPE NOT 4011
SN031	U24	2042	0.000V	SHORT LEAD PIN LENGTH FOR TEST FIXTURE

A.6 Voh3 - High level output voltage (Typical value = 12V)

The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

Voh3 FAILURES (TEST NO's 2051 - 2058)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2053	10.893V	CIRCUIT TYPE NOT 4011
SN012	U23	2054	10.697V	CIRCUIT TYPE NOT 4011
SN012	U23	2055	7.035V	CIRCUIT TYPE NOT 4011
SN012	U23	2056	1.265V	CIRCUIT TYPE NOT 4011
SN012	U23	2057	0.671V	CIRCUIT TYPE NOT 4011
SN012	U23	2058	0.457V	CIRCUIT TYPE NOT 4011

A.7 Voh4 - High level output voltage (Typical value = 14.1V (only for 4011B))

The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

Voh4 FAILURES (TEST NO's 2061 - 2068)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2061	0.004V	CIRCUIT TYPE NOT 4011
SN012	U23	2062	0.0010V	CIRCUIT TYPE NOT 4011
SN012	U23	2063	1.319V	CIRCUIT TYPE NOT 4011
SN012	U23	2064	0.005V	CIRCUIT TYPE NOT 4011
SN012	U23	2065	7.550V	CIRCUIT TYPE NOT 4011
SN012	U23	2066	0.956V	CIRCUIT TYPE NOT 4011
SN012	U23	2067	0.581V	CIRCUIT TYPE NOT 4011
SN012	U23	2068	0.418V	CIRCUIT TYPE NOT 4011

A.8 Vol1 - Low level output voltage (Typical value = 57mV (only for 4011A))

The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

Vol1 FAILURES (TEST NO's 2071 - 2074)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2071	2000.1mV	CIRCUIT TYPE NOT 4011
SN012	U23	2072	2000.1mV	CIRCUIT TYPE NOT 4011
SN012	U23	2073	2000.1mV	CIRCUIT TYPE NOT 4011
SN012	U23	2074	2000.1mV	CIRCUIT TYPE NOT 4011

A.9 Vol2 - Low level output voltage (Typical value = 2mV)

The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

Vol2 FAILURES (TEST NO's 2081 - 2084)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2081	2000.1mV	CIRCUIT TYPE NOT 4011
SN012	U23	2082	2000.1mV	CIRCUIT TYPE NOT 4011
SN012	U23	2083	2000.1mV	CIRCUIT TYPE NOT 4011
SN012	U23	2084	2000.1mV	CIRCUIT TYPE NOT 4011
SN081	U22	2084	-0.1mV	LEAD PINS OK FOR TESTING
SN081	U24	2082	-0.1mV	LEAD PIN 7 MISSING
SN081	U26	2081	-0.2mV	LEAD PINS OK FOR TESTING
SN090	U22	2081	-0.1mV	LEAD PINS OK FOR TESTING
SN090	U22	2082	-0.1mV	LEAD PINS OK FOR TESTING
SN109	U20	2081	-0.1mV	LEAD PINS OK FOR TESTING
SN111	U24	2083	-0.1mV	LEAD PINS OK FOR TESTING

A.10 Vol3 - Low level output voltage (Typical value = 2.5mV)

The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

Vol3 FAILURES (TEST NO's 2091 - 2094)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2091	2000.1mV	CIRCUIT TYPE NOT 4011
SN012	U23	2092	2000.1mV	CIRCUIT TYPE NOT 4011
SN012	U23	2093	2000.1mV	CIRCUIT TYPE NOT 4011
SN012	U23	2094	2000.1mV	CIRCUIT TYPE NOT 4011
SN109	U20	2094	-0.1mV	LEAD PINS OK FOR TESTING

A.11 Vih1 - Input high voltage (Typical value = .002V (only for 4011B))

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

Vih1 FAILURES (TEST NO's 2111 - 2114)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN001	U21	2112	-0.001V	LEAD PINS OK FOR TESTING
SN001	U26	2111	-0.001V	LEAD PINS OK FOR TESTING
SN012	U23	2111	3.837V	CIRCUIT TYPE NOT 4011
SN012	U23	2112	4.071V	CIRCUIT TYPE NOT 4011
SN012	U23	2113	3.152V	CIRCUIT TYPE NOT 4011
SN012	U23	2114	1.977V	CIRCUIT TYPE NOT 4011
SN031	U20	2114	-0.001V	LEAD PINS OK FOR TESTING
SN031	U27	2111	-0.001V	LEAD PIN 14 MISSING
SN081	U22	2111	-0.001V	LEAD PINS OK FOR TESTING
SN081	U23	2114	-0.001V	LEAD PINS OK FOR TESTING
SN081	U24	2111	-0.001V	LEAD PIN 7 MISSING
SN090	U22	2111	-0.001V	LEAD PINS OK FOR TESTING
SN090	U23	2114	-0.001V	LEAD PINS LENGTH SHORT
SN090	U24	2114	-0.001V	LEAD PINS LENGTH SHORT
SN090	U25	2114	-0.001V	LEAD PINS OK FOR TESTING
SN111	U19	2111	-0.001V	LEAD PINS OK FOR TESTING
SN111	U22	2112	-0.001V	LEAD PINS OK FOR TESTING

Vih1 FAILURES (TEST NO's 2111 - 2114) (cont.)				
SYSTEM	LOC	TEST NO.	MEASURED VALUE	PACKAGING INFO
SN111	U22	2114	-0.001V	LEAD PINS OK FOR TESTING
SN111	U24	2111	-0.001V	LEAD PINS OK FOR TESTING
SN111	U24	2113	-0.001V	LEAD PINS OK FOR TESTING
SN111	U26	2113	-0.001V	LEAD PINS OK FOR TESTING
SN131	U19	2112	-0.001V	LEAD PINS 5, 7, 14 MISSING
SN131	U25	2114	-0.001V	LEAD PINS OK FOR TESTING
SN131	U26	2111	-0.001V	LEAD PIN 1 MISSING
SN131	U26	2113	-0.001V	LEAD PIN 1 MISSING
SN131	U27	2112	-0.001V	LEAD PINS 1 & 14 MISSING
SN131	U27	2113	-0.001V	LEAD PINS 1 & 14 MISSING
SN131	U27	2114	-0.001V	LEAD PINS 1 & 14 MISSING
SN191	U21	2114	-0.001V	LEAD PINS OK FOR TESTING
SN191	U23	2111	-0.001V	LEAD PIN 7 MISSING
SN191	U27	2114	-0.001V	LEAD PIN 1 MISSING
SN200	U21	2111	-0.001V	LEAD PINS OK FOR TESTING
SN200	U22	2112	-0.001V	LEAD PINS OK FOR TESTING
SN224	U20	2114	-0.001V	LEAD PINS OK FOR TESTING

A.12 Vih2 - Input high voltage (Typical value = .002V (only for 4011B))

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

Vih2 FAILURES (TEST NO's 2121 - 2124)				
SYSTEM	LOC	TEST NO.	MEASURED VALUE	PACKAGING INFO
SN012	U23	2121	8.783V	CIRCUIT TYPE NOT 4011
SN012	U23	2122	8.813V	CIRCUIT TYPE NOT 4011
SN012	U23	2123	7.801V	CIRCUIT TYPE NOT 4011
SN012	U23	2124	2.349V	CIRCUIT TYPE NOT 4011
SN031	U27	2123	-0.001V	LEAD PIN 14 MISSING
SN081	U22	2123	-0.001V	LEAD PINS OK FOR TESTING
SN081	U24	2123	-0.001V	LEAD PIN 7 MISSING
SN081	U24	2124	-0.001V	LEAD PIN 7 MISSING
SN090	U20	2123	-0.001V	LEAD PINS OK FOR TESTING
SN090	U26	2123	-0.001V	LEAD PINS OK FOR TESTING

Vih2 FAILURES (TEST NO's 2121 - 2124) (cont.)				
SYSTEM	LOC	TEST NO.	MEASURED VALUE	PACKAGING INFO
SN090	U26	2124	-0.001V	LEAD PINS OK FOR TESTING
SN111	U19	2124	-0.001V	LEAD PINS OK FOR TESTING
SN111	U23	2122	-0.001V	LEAD PINS 7 & 8 MISSING
SN131	U24	2123	-0.001V	LEAD PIN 7 MISSING
SN191	U20	2124	-0.001V	LEAD PIN 7 MISSING
SN191	U23	2123	-0.001V	LEAD PIN 7 MISSING
SN224	U20	2124	-0.001V	LEAD PINS OK FOR TESTING

A.13 Vih3 - Input high voltage (Typical value = .002V (only for 4011B))

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

Vih3 FAILURES (TEST NO's 2131 - 2134)				
SYSTEM	LOC	TEST NO.	MEASURED VALUE	PACKAGING INFO
SN012	U23	2131	9.518V	CIRCUIT TYPE NOT 4011
SN012	U23	2132	10.852V	CIRCUIT TYPE NOT 4011
SN012	U23	2133	10.354V	CIRCUIT TYPE NOT 4011
SN012	U23	2134	2.488V	CIRCUIT TYPE NOT 4011
SN031	U27	2134	-0.001V	LEAD PIN 14 MISSING
SN090	U22	2131	-0.001V	LEAD PINS OK FOR TESTING
SN090	U26	2134	-0.001V	LEAD PINS OK FOR TESTING
SN111	U26	2133	-0.001V	LEAD PINS OK FOR TESTING
SN131	U22	2131	-0.001V	LEAD PINS OK FOR TESTING
SN131	U27	2131	-0.001V	LEAD PINS 1 & 14 MISSING
SN191	U27	2134	-0.001V	LEAD PIN 1 MISSING
SN224	U20	2132	-0.001V	LEAD PINS OK FOR TESTING

A.14 Vil1 - Input low voltage (Typical value = 4.92V (only for 4011B))

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

Vil1 FAILURES (TEST NO's 2141 - 2152)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2144	3.802V	CIRCUIT TYPE NOT 4011
SN012	U23	2145	4.280V	CIRCUIT TYPE NOT 4011
SN012	U23	2146	3.799V	CIRCUIT TYPE NOT 4011
SN012	U23	2147	3.518V	CIRCUIT TYPE NOT 4011
SN012	U23	2148	3.774V	CIRCUIT TYPE NOT 4011
SN012	U23	2149	3.677V	CIRCUIT TYPE NOT 4011
SN012	U23	2150	1.882V	CIRCUIT TYPE NOT 4011
SN012	U23	2151	0.908V	CIRCUIT TYPE NOT 4011
SN012	U23	2152	0.458V	CIRCUIT TYPE NOT 4011
SN031	U24	2148	0.002V	SHORT LEAD PIN LENGTH FOR TEST FIXTURE

A.15 Vil2 - Input low voltage (Typical value = 8.3V (only for 4011B))

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

Vil2 FAILURES (TEST NO's 2161 - 2172)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2161	8.792V	CIRCUIT TYPE NOT 4011
SN012	U23	2162	8.791V	CIRCUIT TYPE NOT 4011
SN012	U23	2163	8.790V	CIRCUIT TYPE NOT 4011
SN012	U23	2164	8.378V	CIRCUIT TYPE NOT 4011
SN012	U23	2165	8.821V	CIRCUIT TYPE NOT 4011
SN012	U23	2166	8.378V	CIRCUIT TYPE NOT 4011
SN012	U23	2167	7.722V	CIRCUIT TYPE NOT 4011
SN012	U23	2168	8.088V	CIRCUIT TYPE NOT 4011
SN012	U23	2169	8.056V	CIRCUIT TYPE NOT 4011
SN012	U23	2170	2.818V	CIRCUIT TYPE NOT 4011
SN012	U23	2171	1.084V	CIRCUIT TYPE NOT 4011
SN012	U23	2172	0.488V	CIRCUIT TYPE NOT 4011
SN031	U24	2168	0.001V	SHORT LEAD PIN LENGTH FOR TEST FIXTURE

A.16 Vil3 - Input low voltage (Typical value = 12.8V (only for 4011B))

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

Vil3 FAILURES (TEST NO's 2181 - 2192)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2181	11.084V	CIRCUIT TYPE NOT 4011
SN012	U23	2182	11.079V	CIRCUIT TYPE NOT 4011
SN012	U23	2183	11.079V	CIRCUIT TYPE NOT 4011
SN012	U23	2184	1.131V	CIRCUIT TYPE NOT 4011
SN012	U23	2185	1.369V	CIRCUIT TYPE NOT 4011
SN012	U23	2186	1.138V	CIRCUIT TYPE NOT 4011
SN012	U23	2197	1.152V	CIRCUIT TYPE NOT 4011
SN012	U23	2188	1.147V	CIRCUIT TYPE NOT 4011
SN012	U23	2189	1.188V	CIRCUIT TYPE NOT 4011
SN012	U23	2190	0.536V	CIRCUIT TYPE NOT 4011
SN012	U23	2191	0.355V	CIRCUIT TYPE NOT 4011
SN012	U23	2192	0.304V	CIRCUIT TYPE NOT 4011

A.17 Iol1 - Output low (sink) current (Typical value = 1155uA (only for 4011B))

The current into an output with input conditions applied that, according to the product specification, will establish a low level at the output.

Iol1 FAILURES (TEST NO's 2201 - 2204)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2201	-2000.1uA	CIRCUIT TYPE NOT 4011
SN012	U23	2202	-2000.1uA	CIRCUIT TYPE NOT 4011
SN012	U23	2203	-2000.1uA	CIRCUIT TYPE NOT 4011
SN012	U23	2204	0.1uA	CIRCUIT TYPE NOT 4011

A.18 Iol2 - Output low (sink) current (Typical value = 9ma (only for 4011B))

The current into an output with input conditions applied that, according to the product specification, will establish a low level at the output.

Iol2 FAILURES (TEST NO's 2211 - 2214)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2211	-20.001mA	CIRCUIT TYPE NOT 4011
SN012	U23	2212	-20.001mA	CIRCUIT TYPE NOT 4011
SN012	U23	2213	-20.001mA	CIRCUIT TYPE NOT 4011
SN012	U23	2214	0.002mA	CIRCUIT TYPE NOT 4011

A.19 Ioh1 - Output high (source) current (Typical value = -800uA (only for 4011B))

The current into an output with input conditions applied that, according to the product specification, will establish a high level at the output.

Ioh1 FAILURES (TEST NO's 2221 - 2228)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2221	-167.4uA	CIRCUIT TYPE NOT 4011
SN012	U23	2222	-169.1uA	CIRCUIT TYPE NOT 4011
SN012	U23	2223	2000.1uA	CIRCUIT TYPE NOT 4011
SN012	U23	2225	2000.1uA	CIRCUIT TYPE NOT 4011
SN012	U23	2226	2000.1uA	CIRCUIT TYPE NOT 4011
SN012	U23	2227	0.3uA	CIRCUIT TYPE NOT 4011
SN012	U23	2228	0.3uA	CIRCUIT TYPE NOT 4011
SN031	U24	2226	2000.1uA	SHORT LEAD PIN LENGTH FOR TEST FIXTURE

A.20 Ioh2 - Output high (source) current(Typical value = -2.6mA(only 4011B))

The current into an output with input conditions applied that, according to the product specification, will establish a high level at the output

Ioh2 FAILURES (TEST NO's 2231 - 2238)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2231	-1.218mA	CIRCUIT TYPE NOT 4011
SN012	U23	2232	-1.220mA	CIRCUIT TYPE NOT 4011
SN012	U23	2233	20.001mA	CIRCUIT TYPE NOT 4011
SN012	U23	2234	20.001mA	CIRCUIT TYPE NOT 4011
SN012	U23	2235	20.001mA	CIRCUIT TYPE NOT 4011
SN012	U23	2236	20.001mA	CIRCUIT TYPE NOT 4011
SN012	U23	2237	0.002mA	CIRCUIT TYPE NOT 4011
SN012	U23	2238	0.002mA	CIRCUIT TYPE NOT 4011
SN031	U24	2236	18.591mA	SHORT LEAD PIN LENGTH FOR TEST FIXTURE

A.21 Iih2 - Input leakage current high (typical value = 500pA)

The current into an input when a high-level voltage is applied to that input.

Iih2 FAILURES (TEST NO's 2241 - 2248)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2243	1.90nA	CIRCUIT TYPE NOT 4011
SN012	U23	2244	204nA	CIRCUIT TYPE NOT 4011
SN012	U23	2245	204nA	CIRCUIT TYPE NOT 4011
SN012	U23	2246	204nA	CIRCUIT TYPE NOT 4011
SN012	U23	2247	204nA	CIRCUIT TYPE NOT 4011
SN012	U23	2248	141nA	CIRCUIT TYPE NOT 4011
SN131	U26	2241	1.2nA	LEAD PIN 1 MISSING

A.22 Iil1 - Input leakage current low (Typical value = -100pA)

The current into an input when a low-level voltage is applied to that input.

Iil1 FAILURES (TEST NO's 2251 - 2258)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN001	U20	2252	100pA	LEAD PINS OK FOR TESTING
SN001	U24	2252	100pA	LEAD PINS OK FOR TESTING
SN001	U26	2252	100pA	LEAD PINS OK FOR TESTING
SN012	U23	2253	-1.80nA	CIRCUIT TYPE NOT 4011
SN012	U23	2254	204nA	CIRCUIT TYPE NOT 4011
SN012	U23	2255	204nA	CIRCUIT TYPE NOT 4011
SN012	U23	2256	204nA	CIRCUIT TYPE NOT 4011
SN012	U23	2257	204nA	CIRCUIT TYPE NOT 4011
SN012	U23	2258	204nA	CIRCUIT TYPE NOT 4011
SN031	U20	2252	100pA	LEAD PINS OK FOR TESTING
SN031	U21	2251	100pA	LEAD PINS OK FOR TESTING
SN031	U22	2252	100pA	LEAD PINS OK FOR TESTING
SN031	U24	2252	100pA	SHORT LEAD PIN LENGTH FOR TEST FIXTURE
SN031	U27	2252	100pA	LEAD PIN 14 MISSING
SN081	U22	2252	200pA	LEAD PINS OK FOR TESTING
SN081	U24	2252	100pA	LEAD PIN 7 MISSING
SN081	U26	2252	100pA	LEAD PINS OK FOR TESTING
SN090	U20	2252	200pA	LEAD PINS OK FOR TESTING
SN090	U22	2252	100pA	LEAD PINS OK FOR TESTING
SN090	U24	2252	100pA	LEAD PINS LENGTH SHORT
SN090	U26	2252	100pA	LEAD PINS OK FOR TESTING
SN109	U20	2252	100pA	LEAD PINS OK FOR TESTING
SN111	U19	2251	100pA	LEAD PINS OK FOR TESTING
SN111	U22	2252	100pA	LEAD PINS OK FOR TESTING
SN111	U24	2252	100pA	LEAD PINS OK FOR TESTING
SN111	U26	2252	100pA	LEAD PINS OK FOR TESTING
SN131	U20	2252	100pA	LEAD PINS OK FOR TESTING
SN131	U22	2252	200pA	LEAD PINS OK FOR TESTING
SN131	U24	2252	100pA	LEAD PIN 7 MISSING
SN131	U26	2251	4.70nA	LEAD PIN 1 MISSING
SN131	U26	2252	100pA	LEAD PIN 1 MISSING
SN131	U27	2252	100pA	LEAD PINS 1 & 14 MISSING

IiI1 FAILURES (TEST NO's 2251 - 2258) (cont.)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN191	U21	2252	100pA	LEAD PINS OK FOR TESTING
SN191	U23	2252	100pA	LEAD PIN 7 MISSING
SN191	U25	2252	100pA	LEAD PINS OK FOR TESTING
SN191	U27	2252	100pA	LEAD PIN 1 MISSING
SN200	U22	2252	100pA	LEAD PINS OK FOR TESTING
SN224	U20	2252	100pA	LEAD PINS OK FOR TESTING

A.23 tPHL - Propagation delay time high to low level (Typical value = 100ns)

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

tPHL FAILURES (TEST NO's 2261 - 2268)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2261	0.00SEC	CIRCUIT TYPE NOT 4011
SN012	U23	2262	0.00SEC	CIRCUIT TYPE NOT 4011
SN012	U23	2263	0.00SEC	CIRCUIT TYPE NOT 4011
SN012	U23	2264	0.00SEC	CIRCUIT TYPE NOT 4011
SN012	U23	2265	0.00SEC	CIRCUIT TYPE NOT 4011
SN012	U23	2266	0.00SEC	CIRCUIT TYPE NOT 4011
SN012	U23	2267	0.00SEC	CIRCUIT TYPE NOT 4011
SN012	U23	2268	0.00SEC	CIRCUIT TYPE NOT 4011
SN031	U24	2265	0.00SEC	SHORT LEAD PIN LENGTH FOR TEST FIXTURE

A.24 tPLH - Propagation delay time low to high level (Typical value = 100ns)

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

tPLH FAILURES (TEST NO's 2271 - 2278)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2271	0.00SEC	CIRCUIT TYPE NOT 4011
SN012	U23	2272	0.00SEC	CIRCUIT TYPE NOT 4011
SN012	U23	2273	0.00SEC	CIRCUIT TYPE NOT 4011
SN012	U23	2274	0.00SEC	CIRCUIT TYPE NOT 4011
SN012	U23	2275	0.00SEC	CIRCUIT TYPE NOT 4011
SN012	U23	2276	0.00SEC	CIRCUIT TYPE NOT 4011
SN012	U23	2277	0.00SEC	CIRCUIT TYPE NOT 4011
SN012	U23	2278	0.00SEC	CIRCUIT TYPE NOT 4011
SN031	U24	2275	0.00SEC	SHORT LEAD PIN LENGTH FOR TEST FIXTURE
SN031	U24	2276	0.00SEC	SHORT LEAD PIN LENGTH FOR TEST FIXTURE

A.25 Functional Test

FUNCTIONAL TEST FAILURES (TEST NO 2281)				
SYSTEM	**LOC**	**TEST NO.**	**MEASURED VALUE**	**PACKAGING INFO**
SN012	U23	2281	N/A	CIRCUIT TYPE NOT 4011
SN031	U24	2281	N/A	SHORT LEAD PIN LENGTH FOR TEST FIXTURE

SECTION II

ATTACHMENT C

ELECTRICAL TEST RESULTS LM747 OPERATIONAL AMPLIFIER

ELECTRICAL TEST RESULTS LM747 OPERATIONAL AMPLIFIER

A single LM747 (SN012 U23) operational amplifier manufactured by National Semiconductor was tested to verify electrical functionality. This device is part of the ODS effort and was classed as an electrical failure. No information was given regarding the test conditions and test circuit configuration.

The device package pinout is shown in Figure 1. This package contains two operational amplifiers and individual offset nulling circuitry.

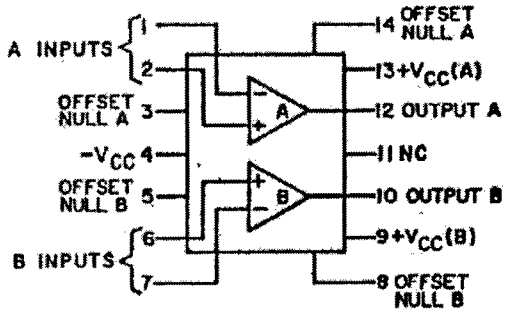


Figure 1: Package Pinout of LM747

The input offset voltage and input bias currents were measured for each of the operational amplifiers using the nulling amplifier test configuration from MIL-M-38510/10102 at +/- V_{CC} = +/- 20V. The electrical test results at 25°C shown below indicate that both devices pass the input offset voltage and current test.

	DUT A	DUT B	Limit
Input Offset Voltage (VIO)	0.328mv	0.104mv	+/- 3mv Max
Input Offset Current (+IIB)	70nA	18nA	110nA Max
Input Offset Current (-IIB)	57nA	9nA	110nA Max

The device was also tested using a classic feedback loop to the inverting input of the operational amplifier with a gain of 25. A 0.1 mV, 1 K Hz sinewave was sent to the inverting input of each device in-turn. The input and output were monitored using an oscilloscope, each device showed the correct amplitude and phase.

This device was determined to be functional under these conditions. The electrical test results will vary when different test conditions and test circuits are used. Additional information is required to determine if device failure only occurs under specific conditions.

SECTION III

HERMETICITY TESTING OF ODS PARTS

FINE AND GROSS LEAK TESTING OF ODS PROGRAM PARTS

PROCEDURE: Upon receipt at RL/ERDR, the subject devices were subjected to hermeticity testing in accordance with Test Method 1014, Test Condition A2 (Flexible helium fine leak test) and Test Condition C1 (gross leak bubble test), of MIL-STD-883D.

A. Fine Leak

1. System calibrated at 1.4×10^{-8} Std atm cc/sec air (error of 0.4×10^{-8} possible).
2. Helium bomb time 2 hours @ 45 psia. Dwell time of 5 minutes.
3. Reject limit > 5×10^{-8} atm cc/sec He.

B. Gross Leak

1. Bomb time in FC-72 fluid of 2 hours @ 75 psia.
2. Submersion in FC-43 fluid at 125°C for bubble detection.

RESULTS: The table below details results of hermeticity testing on the ODS parts. A steady stream of bubbles from between two pins along the lead frame was observed when gross testing S/N 220, part U21.

HERMETICITY TEST RESULTS

SN	Component	Type	T/H	Chemistry	Fine Leak	Gross Leak
S/N 001	U19	CERAMIC S	85C/85%	CFC	PASS	PASS
S/N 001	U20	CERAMIC A	85C/85%	CFC	PASS	PASS
S/N 001	U26	CERAMIC	85C/85%	CFC	PASS	PASS
S/N 012	U23	CERAMIC		CFC	PASS	PASS
S/N 031	U23	CERAMIC S	85C/85%	CONTROL	PASS	PASS
S/N 031	U24	CERAMIC A	85C/85%	CONTROL	PASS	PASS
S/N 081	U23	CERAMIC S	85C/85%	SEMIB	PASS	PASS
S/N 081	U24	CERAMIC A	85C/85%	SEMIB	PASS	PASS
S/N 081	U26	CERAMIC	85C/85%	SEMIB	PASS	PASS
S/N 090	U23	CERAMIC S	85C/85%	WSB	PASS	PASS
S/N 090	U24	CERAMIC A	85C/85%	WSB	PASS	PASS
S/N 090	U26	CERAMIC	85C/85%	WSB	PASS	PASS
S/N 109	U20	CERAMIC	85C/85%	SEMIA	PASS	PASS
S/N 111	U23	CERAMIC S	85C/85%	LOW RES	PASS	PASS

HERMETICITY TEST RESULTS(cont.)

SN	Component	Type	T/H	Chemistry	Fine Leak	Gross Leak
S/N 111	U24	CERAMIC A	85C/85%	LOW RES	PASS	PASS
S/N 111	U26	CERAMIC	85C/85%	LOW RES	PASS	PASS
S/N 131	U23	CERAMIC S	85C/85%	WSA	PASS	PASS
S/N 131	U24	CERAMIC A	85C/85%	WSA	PASS	PASS
S/N 131	U26	CERAMIC	85C/85%	WSA	PASS	PASS
S/N 191	U23	CERAMIC S	85C/85%	LRB	PASS	PASS
S/N 191	U24	CERAMIC A	85C/85%	LRB	PASS	PASS
S/N 191	U26	CERAMIC	85C/85%	LRB	PASS	PASS
S/N 200	U21	CERAMIC	85C/85%	RADS	FAIL	FAIL
S/N 224	U20	CERAMIC	85C/855	DET	PASS	PASS

SECTION IV

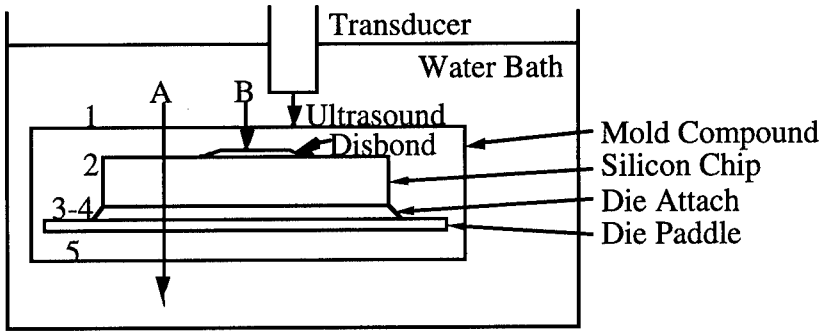
ACOUSTIC ANALYSIS OF ODS PARTS

Internal Analysis Using Scanning Acoustic Microscopy

The C-Mode Scanning Acoustic Microscope (C-SAM) is a nondestructive testing instrument for analyzing components or samples and produces high resolution, ultrasonic images of internal defects. The C-SAM is used for laboratory testing and quality control of devices, and material property and interface characterization of ceramics, metals, polymers and other composites. The C-SAM allows for the identification of internal features beneath the surface of a sample one plane at a time, enabling the discovery of hidden defects, such as poor bonding, delamination, voids and cracks.

In C-SAM analysis, the material or device to be examined is submerged in a coupling fluid, such as water or alcohol. Precise images are generated by rapidly scanning a piezoelectric transducer over the sample at a focused depth or interface. Short pulses of acoustic (ultrasound) energy, 10-150 MHz, are produced by the transducer. The higher frequencies, depending on the material being analyzed, produce higher resolution images. Ultrasound is reflected and transmitted at the interfaces between dissimilar materials. Echoes received by the transducer are analyzed on an oscilloscope and a CRT display. The echo amplitude and polarity are dependent on the material property (density and acoustic velocity) differences encountered at the interface and provide key information for performing the analysis. Comparisons of the amplitude and polarity provide the analyst information to distinguish between voids, delaminations, contaminants and good interfaces.

Plastic packages are typically analyzed using transducer frequencies between 10-30 MHz depending on the thickness of the package. Thick plastic packages result in attenuation loss of the ultrasound and difficulty using the higher frequencies. The image in Figure 1 is a schematic of a cross-section of a plastic package. Lines A and B are two ultrasound paths with the oscilloscope traces shown below. When ultrasound travels from a low to a high acoustic impedance material (see table), a positive echo results and vice versa for a high to low acoustic impedance interface. In trace A, the ultrasound travels from water to the mold compound which results in a positive echo. The next interface, mold compound/silicon die, also results in a positive echo. If we compare the second echoes from trace A and B, we notice a difference in the polarity. The second echo of trace B is negative due to the phase change of the ultrasound at the mold compound/disbond interface on the surface of the silicon die. Echoes 2, 3, and 4 for trace A are close together due to the acoustic velocity in silicon and echo 5 is small considering most of the ultrasound has been reflected at the previous interfaces. There aren't any echoes on trace B after echo 2 due to ultrasound being virtually impenetrable through a vacuum. Images in color or monochrome are produced from the amplitude and polarity of these traces and viewed on a CRT display.



Approximate Acoustic Impedance of Materials in Plastic Packages

Material	Kg/M2.S
Water	1.4
Mold Compound	6.7
Air	0.0
Silicon	19.7
Die Attach	5.1
Copper	41.8

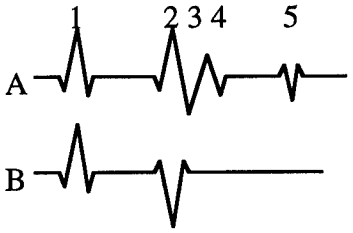


Figure 1. Ultrasound Echo Example Through a Plastic Package

Acoustic Analysis of 85/85 Plastic Parts

A total of 44 plastic encapsulated microcircuits (PEMs) were analyzed using the C-Mode Scanning Acoustic Microscope (C-SAM) to determine bonding integrity within the package. The following table charts the devices analyzed and their applicable stress and chemistry. Because the number of each part type with applicable chemistry is very limited, only general statements can be made. At this time, there is insufficient information to base any conclusions. The following observations were made:

Table 1. Samples Analyzed

CHEMISTRY / PART TYPE	CFC	CONTROL	SEMI B	WSB	SEMI A	LOW RES	WSA	LRB	RADS	DET
PLASTIC*	X	X	X	X	X	X	X	X	X	X
PLASTIC S	X	X		X		X	X			
PLASTIC A	X	X		X		X	X	X		
RWOH	X	X	X	X		X	X	X	2X	
RWOH S	X	X	X	X		X	X	X		
RWOH A	X	X	X	X		X	X	X		

*Note: The PLASTIC devices had a different lead frame and die paddle (smaller).

PART TYPE: There were no significant differences between the PLASTIC and the RWOH devices for the unstressed as well as the A, with the exception that the A(Sequential Autoclave Exposure) devices had significantly more delamination on the lead frame and die paddle. Alternatively, the RWOH S(Sequential Salt Fog Exposure) devices had less delamination than the PLASTIC S devices with the exception of the CONTROL device which was equal. The A devices had more delamination than the S devices with the exception of the CONTROL devices which exhibited the opposite behavior. The only conclusion that can be drawn is the delamination can be attributed to the stress applied. This could cause failure if there are any pathways for contamination from outside the package to the die surface that could cause corrosion. A die penetrant test could be used to determine whether any of the devices have open pathways to the die surface.

CHEMISTRY: There were no significant differences or trends with respect to chemistry.

PLASTIC vs RWOH: All the devices exhibited good bonding integrity at the lead frame, die surface and die paddle bottom. The RWOH devices have delaminations on the paddle surface around the die and the PLASTIC devices did not. However, the PLASTIC devices had a different paddle and lead frame than all of the other devices. In addition, the die paddle surface for all of the PEMs of the RWOH type was delaminated around the die. Figures 1 and 2 represent C-SAM images of each part type. The black area is a delamination at the mold compound/die paddle interface.

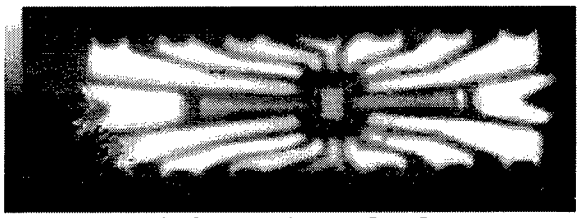


Figure 1. C-SAM of PLASTIC Device

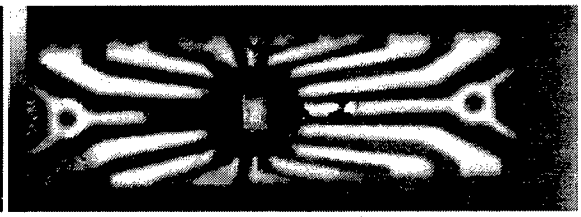


Figure 2. C-SAM of RWOH Device

PLASTIC S vs RWOH S: The PLASTIC S devices had more delamination than the RWOH S devices with the exception of the CONTROL device. However, there aren't enough devices to say if the RWOH devices would be more reliable. A lot of the devices exhibited delamination along the lead frame for pins 3, 4, 5, 10, 11 and 12 which is the shortest pathway to the die surface from outside the package. Figures 3 and 4 represent C-SAM images of each part type. The black areas are delaminations at the mold compound/lead frame or mold compound/die paddle interface.

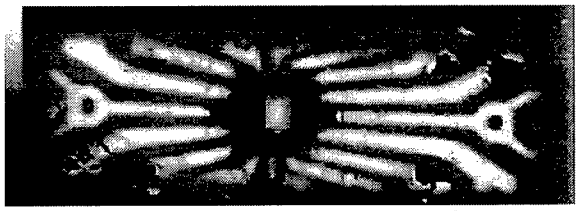


Figure 3. C-SAM of PLASTIC S Device

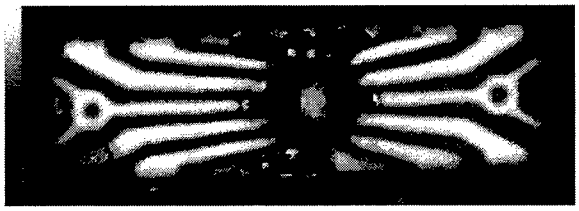


Figure 4. C-SAM of RWOH S Device

PLASTIC A vs RWOH A: The PLASTIC A and RWOH A devices exhibited the most delamination of all the devices. Many of the devices exhibited delamination along the lead frame for pins 3, 4, 5, 10, 11 and 12 which is the shortest pathway to the die surface from outside the package. This delamination could have a significant reliability effect if contamination can find its way to the die surface. Figures 5 and 6 represent C-SAM images of each part type. The black areas are delaminations at the mold compound/lead frame or mold compound/die paddle interface.

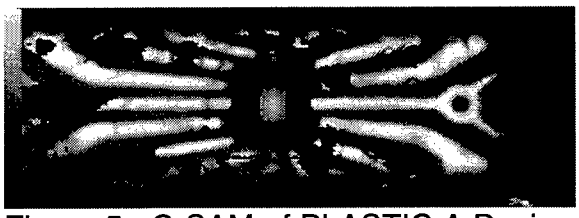


Figure 5. C-SAM of PLASTIC A Device

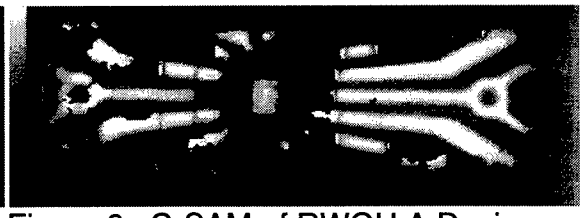


Figure 6. C-SAM of RWOH A Device

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