Final Technical Report

Atomic Layer Epitaxy of Group IV Materials: Surface Processes, Thin Films, Devices and Their Characterization

Supported under Grant #N00014-91-J-1416
Office of the Chief of Naval Research
Report for the period ending 9/30/96

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September, 1996

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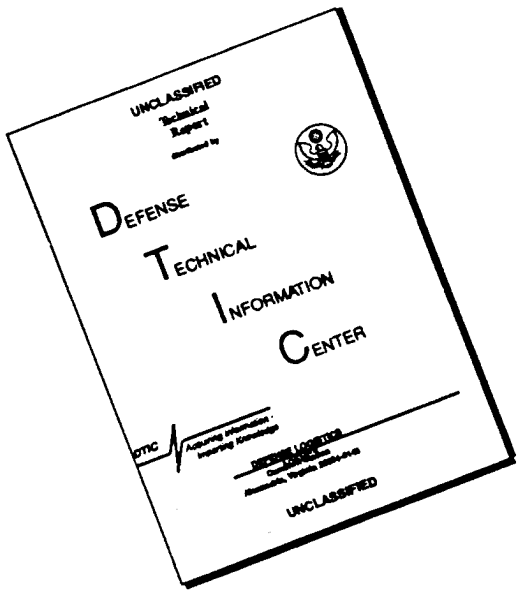

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	September, 1996	Final Technical

4. TITLE AND SUBTITLE
Atomic Layer Epitaxy of Group IV Materials: Surface Processes, Thin Films, Devices and Their Characterization

5. FUNDING NUMBERS
414v001---01
1114SS
N00179
N66005
4B855

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8. PERFORMING ORGANIZATION REPORT NUMBER
N00014-91-J-1416

9. SPONSORING/MONITORING AGENCY NAMES(S) AND ADDRESS(ES)
Sponsoring: ONR, Code 312, 800 N. Quincy, Arlington, VA 22217-5660
Monitoring: Administrative Contracting Officer, ONR, Regional Office Atlanta
101 Marietta Tower, Suite 2805
101 Marietta Street
Atlanta, GA 30323-0008

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for Public Release; Distribution Unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

The ALE technique has been employed to deposit monocrystalline 3C-SiC thin films at 860±10°C. Wafers containing heterojunction bipolar transistor structures have been completely processed and characterized. No transistor activity was detected in any of the HBT structures. Post growth oxidation anneals in argon followed or proceeded by oxygen environments improved both properties. However, the anneals in oxygen also resulted in the growth of a SiO_2 layer at the silicon interface which reduced the capacitance of the structure. An expression for the optimum oxidation time, τ, was developed as a function of the initial thicknesses of the deposited film. The films have large MOS capacitance but also have larger leakage currents compared to those of epitaxial CeO_2 films on Si(111) substrates. However, improved leakage and breakdown characteristics were obtained with annealing in forming gas. The growth parameter, α, the ratio of the growth rates on {100} and {111} facets for diamond films deposited on Si and Ti by microwave plasma CVD has been studied using SEM micrographs. Different morphologies were generated on Si under different deposition conditions. The value of α increased with decreasing temperature and increasing methane concentration, as expected. A value of α for Ti was not obtained due to the heavily twinned particles.

14. SUBJECT TERMS
ALE, atomic layer epitaxy, SiC, silicon carbide, HBTs, transistor activity, thin films, CeO_2, oxidation, annealing, pulsed laser ablation, CVD, chemical vapor deposition, diamond, silicon, titanium, growth parameter

15. NUMBER OF PAGES
34

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLAS	UNCLAS	UNCLAS	SAR

I. Introduction

Atomic layer epitaxy (ALE) is the sequential chemisorption of one or more elemental species or complexes within a time period or chemical environment in which only one monolayer of each species is chemisorbed on the surface of the growing film in each period of the sequence. The excess of a given reactant which is in the gas phase or only physisorbed is purged from the substrate surface region before this surface is exposed to a subsequent reactant. This latter reactant chemisorbs and undergoes reaction with the first reactant on the substrate surface resulting in the formation of a solid film. There are essentially two types of ALE which, for convenience, shall be called Type I and Type II.

In its early development in Finland, the Type I growth scenario frequently involved the deposition of more than one monolayer of the given species. However, at that time, ALE was considered possible only in those materials wherein the bond energies between like metal species and like nonmetal species were each less than that of the metal-nonmetal combination. Thus, even if multiple monolayers of a given element were produced, the material in excess of one monolayer could be sublimed by increasing the temperature and/or waiting for a sufficient period of time under vacuum. Under these chemical constraints, materials such as GaAs were initially thought to be improbable since the Ga-Ga bond strength exceeds that of the GaAs bond strength. However, the self-limiting layer-by-layer deposition of this material proved to be an early example of Type II ALE wherein the trimethylgallium (TMG) chemisorbed to the growing surface and effectively prevented additional adsorption of the incoming metalorganic molecules. The introduction of As, however caused an exchange with the chemisorbed TMG such that a gaseous side product was removed from the growing surface. Two alternating molecular species are also frequently used such that chemisorption of each species occurs sequentially and is accompanied by extraction, abstraction and exchange reactions to produce self-limiting layer-by-layer growth of an element, solid solution or a compound.

The Type II approach has been used primarily for growth of II–VI compounds [1–13]; however, recent studies have shown that it is also applicable for oxides [14–17], nitrides [18], III–V GaAs-based semiconductors [19–32] and silicon [33–35]. The advantages of ALE include monolayer thickness control, growth of abrupt interfaces, growth of uniform and graded solid solutions with controlled composition, reduction in macroscopic defects and uniform coverage over large areas. A commercial application which makes use of the last attribute is large area electroluminescent displays produced from II–VI materials. Two comprehensive reviews [36,6], one limited overview [37] and a book [38] devoted entirely to the subject of ALE have been published.

In this reporting period, investigations concerned with (1) deposition via ALE of 3C-SiC films and the fabrication and characterization of bipolar transistors on these films, (2) the

deposition, annealing and determination of the opitcal emission of CeO_2 epitaxial films on Si(100), (3) the determination of the growth parameter, α, for diamond films on Si and Ti.

The following sections introduce each topic, detail the experimental approaches, report the results to date and provide a discussion and a conclusion for each material. Each major section is self-contained with its own figures, tables and references.

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II. Atomic Layer Epitaxy of Silicon Carbide Films and Their Application in the Development of Bipolar Transistors

A. Introduction

The utilization of active β-SiC components in semiconductor structures could dramatically enhance the performance of integrated circuits and discrete devices. Two convenient, standard criteria for comparing the relative merits and capabilities of semiconductor materials are the Johnson's and Keye's figures of merit. The Johnson's figure of merit estimates the maximum performance to be expected of a semiconductor material in discrete bipolar transistors[1] while the Keye's rating assesses a material's suitability for high density integrated circuit applications[2]. β-SiC ranks far above Si in both criteria, with ratings 33.9 and 5.82 times higher than Si by the Johnson's and Keye's figures of merit, respectively. Although these ratings for β-SiC demonstrate that both discrete devices and integrated circuitry employing β-SiC components should attain levels of performance unachievable with device technologies based solely on Si, relatively few devices containing β-SiC components have been produced[4,5].

A significant barrier to the widespread exploitation of the capabilities of β-SiC is the lack of an advanced β-SiC processing infrastructure. The most expeditious route to devices accessing the performance increases possible with β-SiC would be the development of a thin-film deposition technique to allow the integration of β-SiC into the existing Si device fabrication infrastructure. Conventional chemical vapor deposition (CVD) techniques for producing heteroepitaxial β-SiC films on Si wafers require a carbonizing pretreatment and high deposition temperatures[6]. These requirements make β-SiC CVD processes incompatible with existing Si sub-micron architecture process routes. However, as shown in a previous report (June, 1994), atomic layer epitaxy offers the ability to deposit monocrystalline β-SiC films on Si(100) substrates at low temperatures without the carbonizing pretreatment and may serve as a vehicle to facilitate the introduction of β-SiC into selected devices structures.

The objective of this research is to extend the state-of-the-art regarding SiC thin film deposition and application via the employment of atomic layer epitaxy to deposit β-SiC films on select substrates. During this reporting period, work has continued with the fabrication of trenched heterojunction bipolar transistors (HBTs) employing a wide bandgap β-SiC emitter. The second batch of transistors has been completely processed. The following sections describe the fabrication steps followed in this work and the results of characterization of the resultant devices via electrical measurements and scanning electron microscopy (SEM).

B. Experimental Procedure

ALE Reactor. The ALE reactor employed in this research has not been significantly modified since it was described in detail in a previous report (June, 1993). To prevent mixing

of process gases, flowing Ar "curtains" divide the reactor into four radial quadrants through which isolated fluxes of Si_2H_6, C_2H_4, NH_3 and triethylaluminum ($Al(C_2H_5)_3$) may flow. The quadrant containing NH_3 also contains a W filament that may be heated to produce atomic hydrogen or to crack NH_3 depending on gas flow conditions. During deposition, heated samples can be rotated alternately between quadrants and exposed to the species present to form films in a layer-by-layer process. Due to the construction of the reactor, SiC films can be deposited and doped n- and p-type with N and Al, respectively.

Fabrication of Trenched HBTs. The six level mask system designed to produce HBTs was described in detail in a previous report (June, 1994). Each die contained four transistors: a planar HBT, two HBTs in trench structures and one HBT with a corrugated or "waffle iron" structure. The geometry of the latter devices were engineered to exploit the high degree of conformality possible with layer-by-layer deposited SiC films. The procedures followed in producing the devices are explained in detail in the last report (December, 1994).

Deposition. SiC films were deposited on partially processed wafers. Three samples, HBT 6–HBT 8, were processed under the conditions listed in Table I. Prior to etching of the SiC to define the emitters, the thickness of each film was determined via cross-sectional SEM observation.

Table I. SiC Deposition Conditions for Second Batch of HBTs

Process parameter	HBT 6	HBT 7	HBT 8
Sample temperature	850° C	870° C	850° C
Si_2H_6 flow/ H_2 carrier	0.8 / 300 sccm	0.8 sccm/ 300 sccm	2
C_2H_4 flow/ H_2 carrier	2 / 200 sccm	2 sccm/ 200 sccm	2
Ar curtain flow	200 sccm	200 sccm	0 sccm
H_2 across filament	100 sccm	100 sccm	3 sccm
Filament temperature	1700°C	1700° C	unheated
Pressure	1.5 Torr	1.5 Torr	$\approx 10^{-3}$ Torr
Rotational scheme	rotate through Si_2H_6 and C_2H_4, wait under fil. 30 s. rpt. 1500 times.	rotate continuously to complete one Si-C-fil. cycle every 13 s. rpt. 3000 times	5 s. under Si_2H_6, 5 s. under H_2, 5 s. under C_2H_4, 5 s. under H_2 rpt. 1100 times.
Film thickness	0.18 μm	0.32 μm	0.2 μm

Ni Contacts (N-Type SiC). Ni contacts were sputtered onto the films using a photolithography lift-off technique. The specifics of the lift-off technique were discussed in detail in a previous report (June, 1994). Sputtering conditions were power = 100 watts 13.56 MHz R.F. and 20 mTorr Ar ambient. The Ni deposition rate was ≈ 2000 Å/Hr. Contacts were then annealed in ~. Heatpulse rapid thermal annealer (RTA) with an Ar ambient at 1000° C for 20 sec.

Al Contacts (P-type Si). Al contacts were vacuum evaporated from pure Al shot (99.9999% pure). The deposited Al film was subsequently processed using conventional microelectronic fabrication techniques.

Electrical Characterization. I-V and I_C vs. V_{CE} characterizations were performed with a Hewlett Packard 4145A Semiconductor Parameter Analyzer. Ambient light was found to have a significant effect on measured factors, therefore, all data was collected under dark conditions. Typical contact points are indicated in Fig. 1. Emitter and base connections for testing were made with W probes while the collector contact was made with a large area silver paint electrode on the wafer backside after grinding.

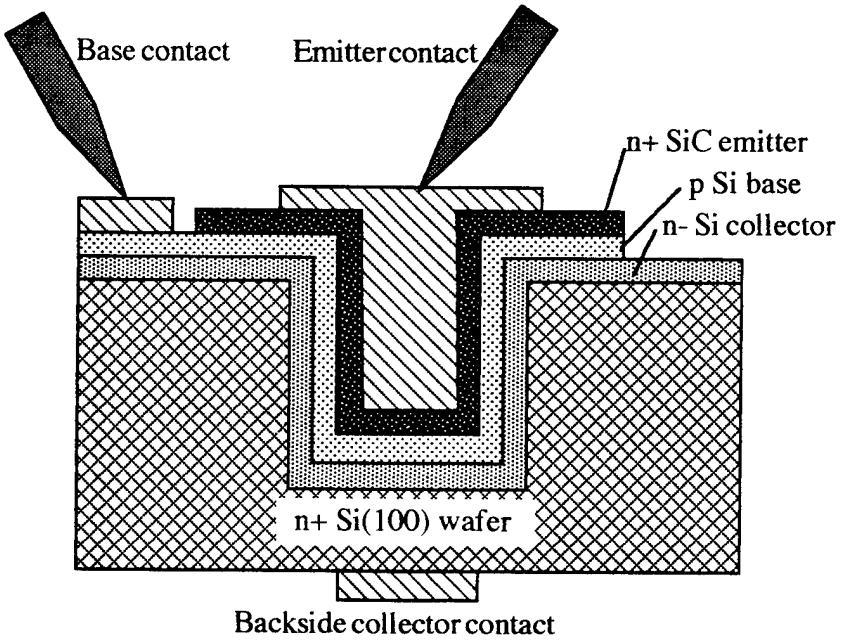
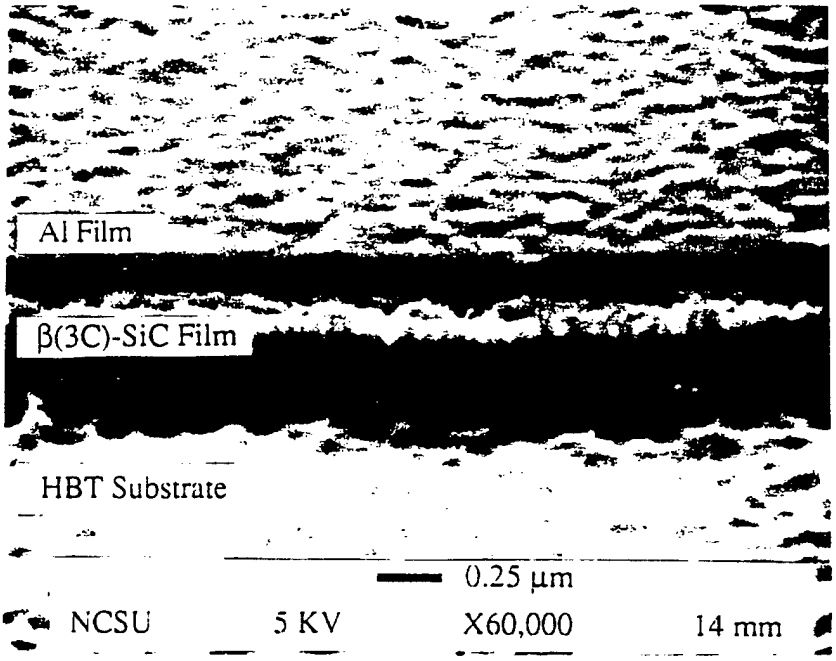


Figure 1. Testing contacts for electrical characterization of HBTs.

C. Results

The wafers in the second batch of HBT structures were denoted as: HBT 6, HBT 7 and HBT 8. The conditions under which the SiC films were deposited on these samples are tabulated in Table I. In general, these SiC films were thinner than those produced in the first batch of HBT structures in order to lessen the required accuracy of the SiC etch step.

Figure 2 is a SEM image of wafer HBT 6 taken after the SiC etch. The Al layer used to mask the SiC is visible in the image. There was some over-etching of the p-type Si base region on this wafer. The roughening of the Si surface is visible, although under-cutting of the emitter region is visible, it is not as excessive as reported previously (December, 1994). The excess etching in Fig. 2 is of the order of only 0.1 μm and did not result in the total removal of the base region which had an initial thickness of ≈ 1.5 μm.



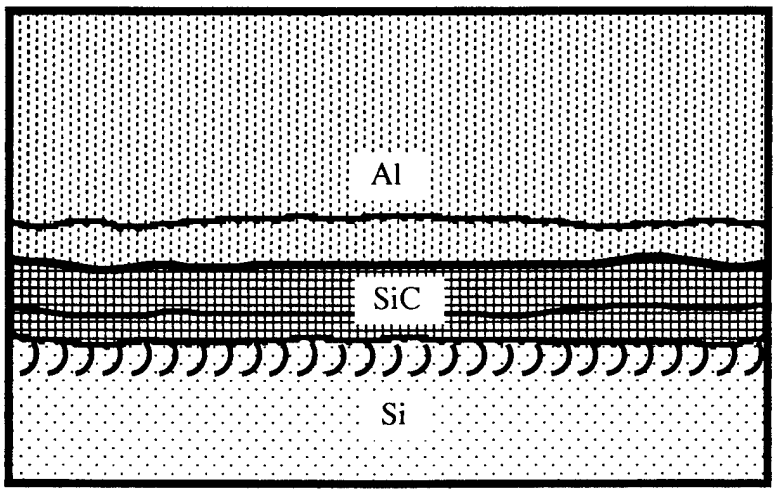


Figure 2. Wafer HBT 6 after etching of the SiC emitter layer.

Figures 3 and 4 are I-V curves generated across the emitter-base and the base-collector junctions, respectively, of a typical corrugated interface transistor on wafer HBT 6. Both junctions exhibited rectifying behavior. However, the emitter-base junction characterized in Fig. 3 was very leaky in reverse bias. This device had an active area of 28,700 μm^2, yielding a

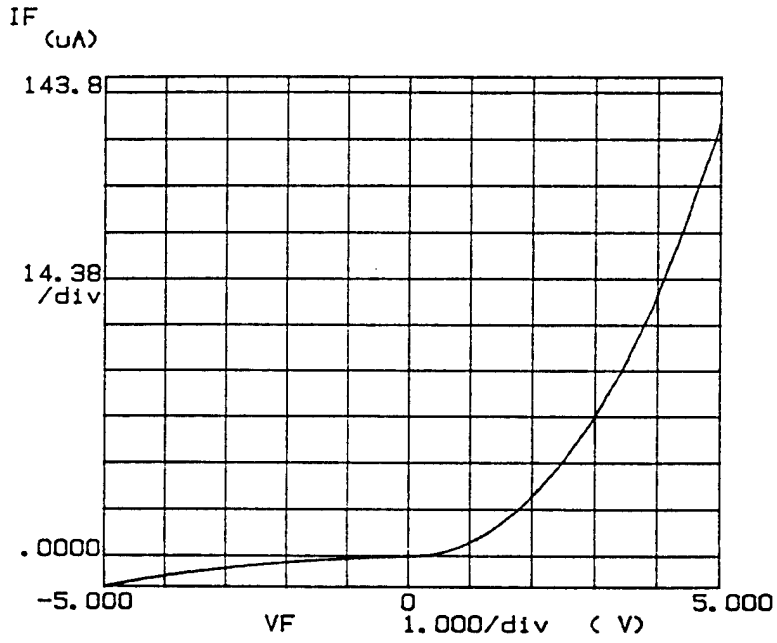


Figure 3. I-V characteristics of emitter-base junction of corrugated HBT on wafer HBT 6.

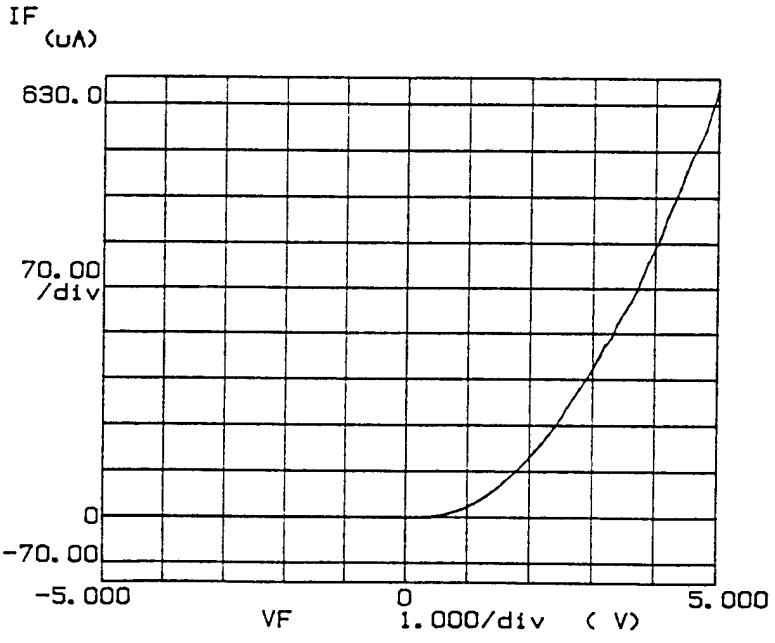


Figure 4. I-V characteristics of base-collector junction of corrugated HBT of wafer HBT 6.

reverse bias current density of 110 A cm^{-2} at -4.5 V. Good rectifying behavior across the base-collector junction and rectifying, but leaky behavior across the emitter-base junction were consistently observed on all three wafers of the second batch.

Figure 5 is a typical I_C vs. V_{CE} performance plot for a corrugated interface HBT on wafer HBT 6. In this plot I_C is determined as V_{CE} is varied from 0 to 5V while I_B is increased in 1 mA increments from 0 mA to 4 mA, yielding five separate curves. From this plot, there is no apparent gain in the transistors as I_C increases in each step by almost exactly the same value I_B increases. This behavior is similar to that observed for the transistors produces in the first batch of HBTs. Transistor activity was not observed in any of the devices produced in the second batch of HBTs.

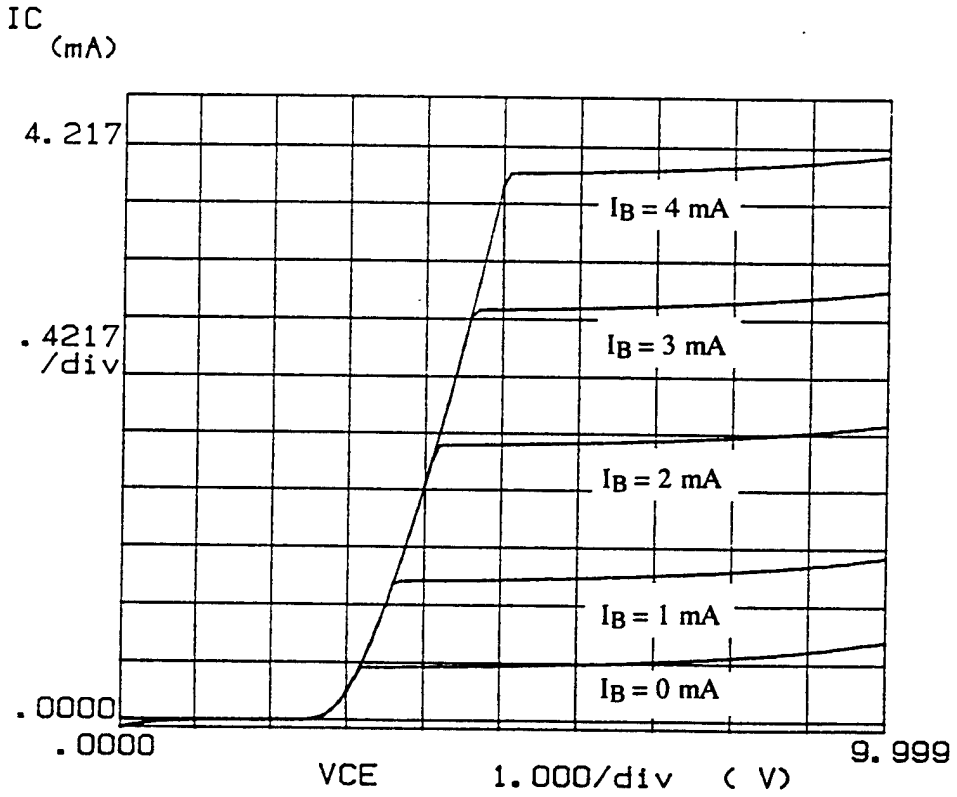


Figure 5. Typical I_C vs. V_{CE} behavior of a typical corrugated surface HBT in the second HBT batch at several I_B values.

D. Discussion

No transistor activity was observed in the second batch of HBTs. Two possible causes for the lack of performance were identified in the analysis of the first batch of HBTs: inaccurate etching of the SiC film deposited to form the emitters and too wide a base region. Examination of the wafers produced in the second batch after etching the SiC revealed that the etching was

performed accurately, removing all of the undesired SiC while only slightly etching the underlying p-type Si base region. The most probable cause of the absence of transistor activity was an excessive width of the base region.

Bipolar transistors usually operate by injecting minority carriers into the base region by forward biasing the emitter-base junction. If the minority carrier diffusion distance in the base is greater than the distance to the reverse biased base-collector junction, these carriers will eventually reach the collector region to contribute to I_C. However, if the base region is too wide for the carriers to transverse before recombining, the transistor becomes essentially two diodes sharing a common terminal. This was apparently the root flaw of the HBT structures developed in this work.

The collector and base regions of the HBT structures studied here were deposited by a commercial contractor. A spreading resistance profile of the deposited layers is presented in Fig. 6. Both the base region (p-type) and the collector region (lightly n-type) were much thicker than ordered. This is due to the complication of carrier migration during deposition. As these films were deposited at ≈1300°C, abrupt changes in carrier concentration are not possible

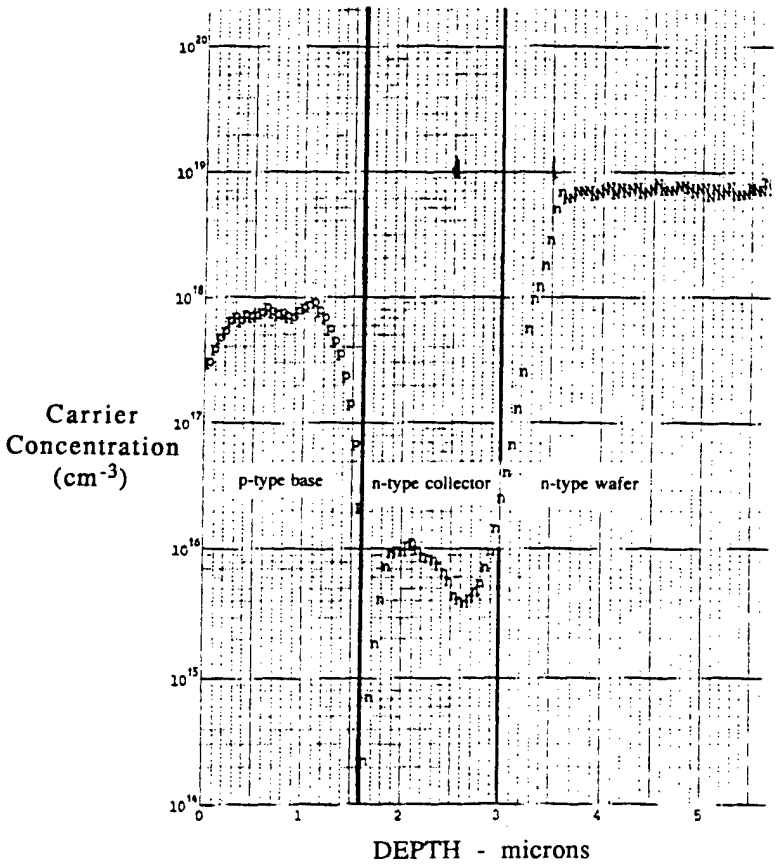


Figure 6. Spreading resistance profile of base and collector regions.

due to the diffusion of donors and acceptors. As a consequence, thicker films are necessary to achieve a relatively constant dopant level.

E. Conclusions

The second batch of devices was processed with thinner SiC films, reducing the required precision of the etching process. SEM examination of the second set of wafers indicated that the SiC was etched appropriately. However, none of the wafers in this second batch contained operational devices either. Electrical characterization of the latter devices revealed rectifying behavior at both the emitter-base and the base-collector junction. An excessive base width is hypothesized to be responsible for the lack of transistor behavior in the device structures. Due to the base region width, injected carriers recombined before reaching the base-collector junction. As a result, the transistors actually behaved as two independent p-n junctions that shared a p-terminal contact. Although a batch of devices with a thinner base region may have succeeded, this project was terminated.

F. Acknowledgements

The author would like to acknowledge John Palmour at CREE Research Inc., Durham, NC for his diligent efforts in performing the etching of the SiC films in this research.

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III. Oxidation Process and the Prediction of the Optimum Oxidation Time of $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si(111)$

A. Introduction

Cerium oxide (CeO_2) is a crystalline insulator. It is a promising material to realize the silicon-on-insulator (SOI) structure because it has a CaF_2-type cubic structure which is nearly lattice matched to Si with high dielectric constant (~26). The lattice misfit ($\Delta a/a$) is only 0.35%[1]. These values are considerably better than the respective values for other crystalline insulators such as CaF_2, sapphire, and spinel[2-4].

As previously reported, CeO_2 on Si has two distinct amorphous regions at the interface and the electrical properties of this structure can be improved by post-annealing in dry oxygen ambient[5,6]. In other words, altering the film structure from $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si$ to $CeO_2/SiO_2/Si$ greatly enhances the electrical properties. Unfortunately, this oxidation of the as-grown films increases the thickness of SiO_2. It is desirable to keep the SiO_2 thickness as thin as possible to maintain a large total capacitance.

In this report, oxidation models will be established for both $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si$ and $CeO_2/SiO_2/Si$. The investigation will examine how to meet the optimum oxidation time in order to arrive at maximum capacitance without an $\alpha\text{-}CeO_{2-x}$ layer.

B. Experimental Procedure

CeO_2 thin films have been grown on Si substrates using a UHV laser ablation system[5,6]. The base pressure was kept 10^{-8} Torr during the growth. The growth temperature was ~700°C, and post-annealing in dry oxygen ambient was applied. Both as-grown and annealed films were evaluated by high resolution transmission electron microscopy (HRTEM), Rutherford Back Scattering (RBS), and capacitance-voltage (C-V) measurements. The thickness of each film was determined from the TEM images.

The post oxidation in dry oxygen was exactly the same procedure as the standard oxidation of Si. The oxidation temperature was 900°C, and the oxidation times were 18 and 35 minutes[6]. Table I shows the thickness changes due to the oxidation as measured by TEM. From the experimental data in Table I, the following was deduced:

i) Initially, the oxidation and the O_2-diffusion processes were used mainly in converting $\alpha\text{-}CeO_{2-x}$ to CeO_2, thus reducing x_1 to zero and increasing x_o to its maximum steady value, i.e. $x_o(\text{final}) = x_o(\text{initial}) + x_1(\text{initial})$. This initial stage was expected to be carried out in time $t \approx \tau$, where τ in Table I was less than 18 minutes, as concluded from the TEM microstructure observation.

Table I. Experimental Data of Each Layer Thickness Before and After Oxidation

Oxidation time [min]	CeO_2 thickness x_o [Å]	α-CeO_{2-x} thickness x_1 [Å]	SiO_2 thickness x_2 [Å]
as-grown	181	37	26
18	218	0	70
35	218	0	192

ii) For $t < \tau$ the thickness of $SiO_2(x_2)$ did not change much from its initial value x_2(initial). This assumption was based in the smaller relative increase in SiO_2 layer thickness during the first 18 minutes of oxidation time relative to the next 17 minutes of further oxidation.

C. Diffusion Model

The calculations used in this study were based on the Deal-Grove oxidation model of SiO_2/Si structure[7]. This model was modified to study the O_2 diffusion in the CeO_2/SiO_2/Si structure and determine an expression for x_2 for $t > \tau$. The model was also expanded to consider the more complicated CeO_2/α-CeO_{2-x}/SiO_2/Si structure.

Oxidation for $CeO_2/SiO_2/Si(111)$. Figure 1 shows the O_2 concentration profiles and the fluxes considered in studying the O_2 diffusion process in the CeO_2/SiO_2/Si structure.

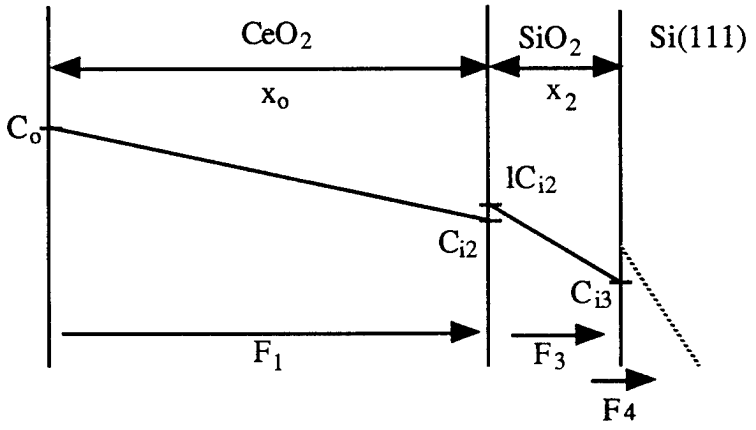

Figure 1. Schematic oxidation model for CeO_2/SiO_2/Si(111).

In this figure,

- x_o: thickness of CeO_2,
- x_2: thickness of SiO_2,
- F_1: oxygen flux in CeO_2,
- F_3: oxygen flux in SiO_2,
- F_4: oxygen flux through the SiO_2/Si interface,
- C_o: oxygen concentration at the CeO_2 surface,
- C_{i2}: oxygen concentration at the front surface of CeO_2/SiO_2 interface,
- C_{i3}: oxygen concentration at the SiO_2/Si interface, and
- l: segregation coefficient of oxygen at the CeO_2/SiO_2 interface.

The oxygen fluxes, $F_1 - F_4$, were as follows:

$$F_1 = D_o \frac{C_o - C_{i2}}{x_o},$$

$$F_3 = D_2 \frac{lC_{i2} - C_{i3}}{x_2},$$

$$F_4 = k_2 C_{i3},$$

where,

- D_o: diffusion constant of oxygen in CeO_2,
- D_2: diffusion constant of oxygen in SiO_2, and
- k_2: chemical reaction rate at SiO_2/Si interface.

Since the thickness of the Si substrate was too large compared with the other layers, the oxygen flux in Si substrate was almost zero. In the steady state of oxidation conditions, all the oxygen fluxes were equal, thus the oxygen concentration at SiO_2/Si, C_{i3}, was deduced from

$$C_{i3} = \frac{lC_o}{1 + \frac{lk_2 x_o}{D_o} + \frac{k_2 x_2}{D_2}}. \quad (1)$$

The SiO_2 growth rate was generally given as:

$$\frac{dx_2}{dt} = \frac{F_3}{N_2} = \frac{k_2 C_{i3}}{N_2}, \quad (2)$$

where,

N_2: the number of oxygen atoms incorporated into a unit volume of SiO_2.

Since x_o was assumed to be constant based on the experimental results, the integration of Eq. (2) with Eq. (1) led to the SiO_2 thickness as a function of time.

$$x_2 = \sqrt{\frac{2lD_2C_o}{N_2}(t-\tau)+\left(x_2^{\tau}+\frac{lD_2}{D_o}+\frac{D_2}{k_2}\right)^2}-\left(\frac{lD_2}{D_o}+\frac{D_2}{k_2}\right) \qquad (3)$$

The initial conditions used in Eq. (3) were as follows:

τ: oxidation time for the film structure to change from $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si$ to $CeO_2/SiO_2/Si$ (optimum oxidation time), and

x_2^{τ}: thickness of SiO_2 at $t = \tau$.

Equation (3) was valid for $t > \tau$. Using this solution and experimental data, the optimum oxidation time τ, i.e. the time required to recrystallize $\alpha\text{-}CeO_{2-x}$ without increasing the SiO_2 layer thickness, was deduced.

Oxidation for $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si(111)$. Figure 2 shows the schematic oxidation model for $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si$ with the same concept as the case above.

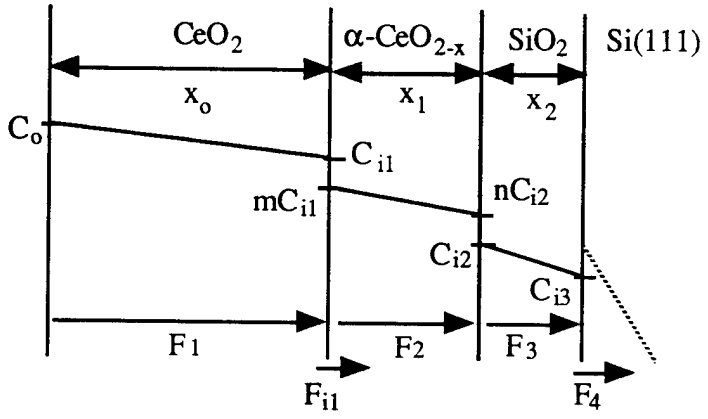

Figure 2. Schematic oxidation model for $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si(111)$.

The following extra parameters were used:

x_1: thickness of $\alpha\text{-}CeO_{2-x}$,

F_{i1}: oxygen flux at $CeO_2/\alpha\text{-}CeO_{2-x}$ interface,

F_2: oxygen flux in α-CeO_{2-x},

C_{i1}: oxygen concentration at the CeO_2/α-CeO_{2-x} interface,

m: segregation coefficient of oxygen at the CeO_2/α-CeO_{2-x} interface, and

n: segregation coefficient of oxygen at the α-CeO_{2-x}/SiO_2 interface.

The oxygen fluxes, $F_1 - F_4$, were as follows:

$$F_1 = D_o \frac{C_o - C_{i1}}{x_o}, \tag{4}$$

$$F_{i1} = k_1 C_{i1}, \tag{5}$$

$$F_2 = D_1 \frac{mC_{i1} - nC_{i2}}{x_1}, \tag{6}$$

$$F_3 = D_2 \frac{nC_{i2} - C_{i3}}{x_2}, \tag{7}$$

$$F_{i2} = k_2 C_{i3}, \tag{8}$$

where,

D_1: diffusion constant of oxygen in α-CeO_{2-x}, and

k_1: chemical reaction rate at CeO_2/α-CeO_{2-x} interface.

In the steady state oxidation conditions, the oxygen fluxes satisfied the following equations:

$$F_1 = F_{i1} + F_2, \tag{9}$$

and

$$F_2 = F_3 = F_4. \tag{10}$$

Substituting Eqs. (4)–(8) into Eqs. (9) and (10) gave

$$C_{i1} = \frac{C_o}{1 + \frac{k_1 x_o}{D_o} + \frac{mk_2 x_o / D_o}{k_2 x_1 / D_1 + n(1 + k_2 x_2 / D_2)}}, \tag{11}$$

and

$$C_{i3} = \frac{m}{\frac{k_2 x_1}{D_1} + n\left(1 + \frac{k_2 x_2}{D_2}\right)} \frac{C_o}{1 + \frac{k_1 x_o}{D_o} + \frac{mk_2 x_o / D_o}{k_2 x_1 / D_1 + n(1 + k_2 x_2 / D_2)}}. \tag{12}$$

The growth rates of CeO_2 and SiO_2 were as follows:

$$\frac{dx_o}{dt} = \frac{F_{i1}}{N_1} = \frac{k_1 C_{i1}}{N_1} \tag{13}$$

and

$$\frac{dx_2}{dt} = \frac{F_3}{N_2} = \frac{k_2 C_{i3}}{N_2}, \tag{2}$$

where,

N_1: the number of oxygen atoms incorporated into a unit volume of CeO_2.

Since the experimental data shown in Table I indicated that the sum of CeO_2 and α-CeO_{2-x} thicknesses did not change with oxidation, the thickness of α-CeO_{2-x} was given simply as

$$x_1 = x_0^{ini} + x_1^{ini} - x_0, \tag{14}$$

where,

x_0^{ini}: initial thickness of CeO_2, and

x_1^{ini}: initial thickness of α-CeO_{2-x}.

The differential Eqs. (13) and (2) had to be solved with Eqs. (11) and (12) in order to obtain CeO_2 and SiO_2 thicknesses as functions of time. However, the equations were too complex to solve mathematically. This research relied on an earlier assumption based on the data shown in Table I that most of the oxygen from the surface of CeO_2 was consumed at CeO_2/α-CeO_{2-x} interface. For $t<\tau$, this assumption seemed reasonable since the SiO_2 growth rate was much faster after the completion of α-CeO_{2-x} recrystallization ($t > \tau$) than before the completion ($t < \tau$). Using the oxidation models, this assumption was expressed as

$$F_{i1} \gg F_2 \tag{15}$$

and modified with Eqs. (7) and (8) as

$$k_1 \gg \frac{mk_2}{\frac{k_2 x_1}{D_1} + n\left(1 + \frac{k_2 x_2}{D_2}\right)}. \tag{15}'$$

Thus, Eqs. (11) and (12) were simplified as

$$C_{i1} \approx \frac{C_6}{1 + k_1 x_o / D_o}, \tag{11}'$$

$$C_{i3} \ll \frac{k_1}{k_2} \frac{C_o}{1 + k_1 x_o / D_o},$$

and

$$k_2 C_{i3} \ll k_1 C_{i1}. \qquad (12)'$$

The CeO_2 thickness as a function of time was achieved by the integration of Eqs. (13) and (11)′:

$$x_o = \sqrt{\frac{2D_o C_o}{N_1} t + \left(x_o^{ini} + D_o / k_1\right)^2} - D_o / k_1. \qquad (16)$$

Equation (12)′ implied that the SiO_2 growth was negligible while CeO_2 was growing by consuming the α-CeO_{2-x}. Thus,

$$x_2 = x_2^t = x_2^{ini} \quad \text{at } t < \tau, \qquad (17)$$

where x_2^{ini} was the initial thickness of SiO_2 in the as-grown material.

Equations (14), (16), and (17) were valid for $t < \tau$. The optimum oxidation time τ was obtained from Eq. (16) with $x_0 = x_0^{ini} + x_1^{ini}$ as

$$\tau = \frac{N_1}{2D_o C_o} x_1^{ini} \left(2x_o^{ini} + x_1^{ini} + 2D_o / k_1\right). \qquad (18)$$

By using this value τ, the optimum oxidation time for various initial thicknesses of CeO_2 and α-CeO_{2-x} was found. Since k_1 and C_o were unknown parameters, they were determined based on the experimental data as shown below.

D. Results and Considerations

The following physical constants were used in the above equations:

$D_o = 4.4 \times 10^{-9}$ cm^2/sec	Diffusion constant of oxygen in CeO_2[9],
$D_1 = 9.0 \times 10^{-8}$ cm^2/sec	Diffusion constant of oxygen in α-CeO_{2-x}[9],
$D_2 = 2.8 \times 10^{-9}$ cm^2/sec	Diffusion constant of oxygen in SiO_2[10],
$N_1 = 2.5 \times 10^{22}$ /cm^3	Quantity of Oxidant incorporated into CeO_2,
$N_2 = 2.2 \times 10^{22}$ /cm^3	Quantity of Oxidant incorporated into SiO_2, and
$k_2 = 2.2 \times 10^{-4}$ cm/sec	Chemical reaction rate of oxide formation at SiO_2/Si[7].

First, Eq. (3) was used with the data shown in Table I to obtain l, the segregation coefficient at the CeO_2/SiO_2 interface. Since Eq. (3) was valid for any $t > \tau$, data shown in Table I to obtain l was used and thus,

$$l = 2.7$$

was obtained.

In this report, $C_o = 6.0 \times 10^{16}$ /cm^3 was used which is oxygen concentration at the SiO_2 surface[11]. Then, using Eqs. (3) and (17), τ was obtained as

$$\tau = 11.6 \text{ min.}$$

This was the average value of τ calculated with t = 18 minutes and t = 35 minutes. Finally, using Eq. (18) with this τ resulted in

$$k_1 = 2.5 \times 10^{-4} \text{ cm/sec.}$$

Since this value was so close to the one of SiO_2/Si, it suggested that the approximation which was applied was reasonable. Using these values, variation of thicknesses of each layer with oxidation time was calculated and is shown in Fig. 3.

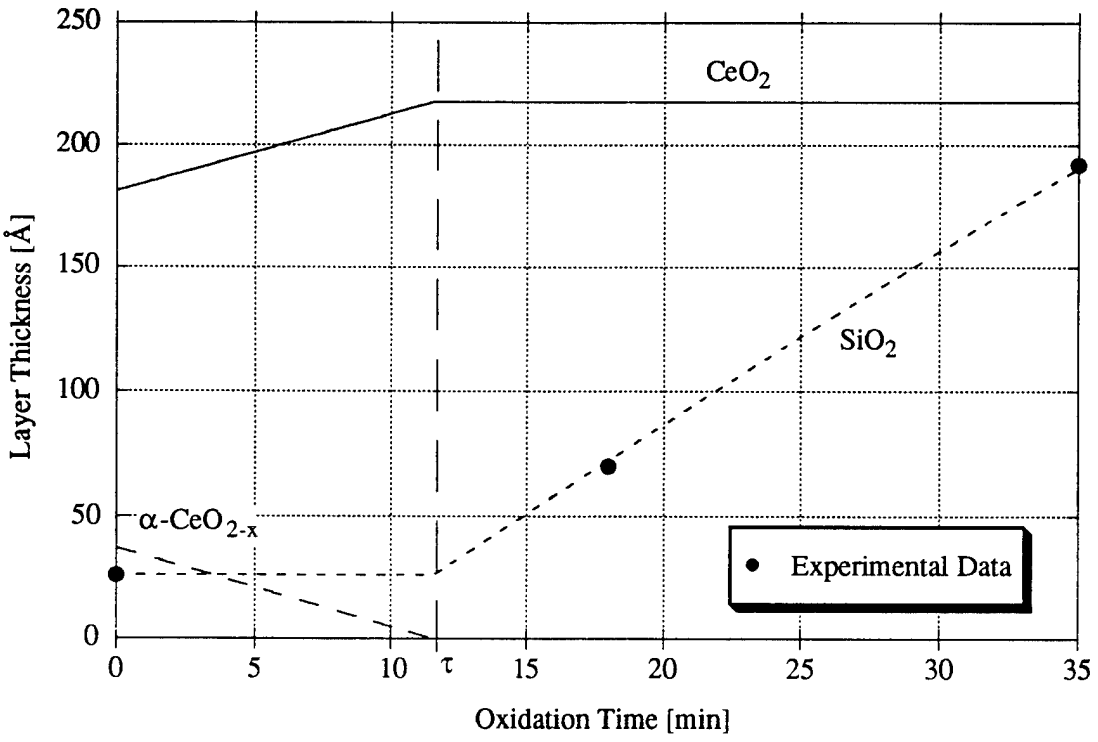

Figure 3. Time dependence of each layer thickness with oxidation as calculated by the approximation used in this report.

Data in Fig. 3 was obtained based on the approximation previously mentioned. However, the time dependence of thicknesses can also be obtained using fitting parameters by numerical calculation on Eqs. (11) and (12). The numerical approach can calculate SiO_2 growth during the recrystallization. Using the same parameters, the time dependence of thicknesses with fitting parameters m and n was obtained which was the segregation coefficients at the interfaces of $CeO_2/\alpha\text{-}CeO_{2-x}$ and $\alpha\text{-}CeO_{2-x}/SiO_2$, respectively. The results are shown in Fig. 4.

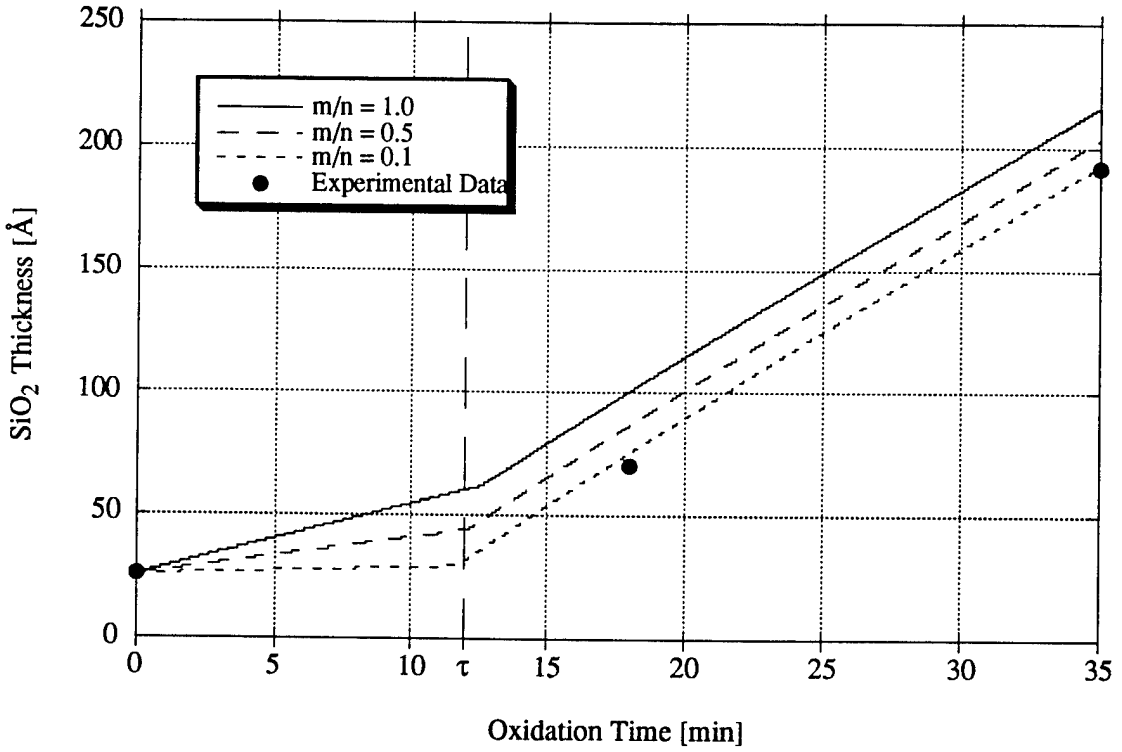

Figure 4. SiO_2 thickness changes with oxidation as calculated by the numerical calculation using m/n as fitting parameters.

From this figure, it was clear that if the ratio of m/n was close to zero, the calculation result closely reached that of the approximation based on experimental data. The large value of n was reasonable since $\alpha\text{-}CeO_{2-x}$ was eliminated much faster than SiO_2 growth. Other iteration can also be applied to the best fitting of data.

E. Conclusions

Oxidation models for $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si$ and $CeO_2/SiO_2/Si$ are proposed in order to obtain optimum oxidation time τ which gives the $CeO_2/SiO_2/Si$ structure with the thinnest SiO_2 thickness. An expression for τ was developed as a function of the initial thickness of the deposited film. The numerical calculation results also indicated the validity of the assumption.

F. Future Plans and Goals

It is planned to use the above calculations to predict the optimum oxidation time for different initial CeO_2 deposited films and the use of TEM, RBS and C-V to confirm the validity of the above model.

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IV. Properties of CeO_2 Films on Si(100) Substrates

A. Introduction

Thin films of CeO_2 deposited on silicon substrates may have the potential of providing MOS capacitor structures with a higher storage capacity compared to conventional SiO_2 films because of the higher relative dielectric constant (~ 26) of CeO_2 [1]. Epitaxial CeO_2 films deposited on Si(111) substrates by pulsed laser ablation of a CeO_2 target under UHV conditions at relatively high substrate temperatures in the range 550 to 750°C and annealed in different environments were previously investigated [2,3] and were shown to have improved electrical properties after annealing in oxygen at high temperature (900°C). This annealing was needed to reduce defects in the as-deposited films and retain their stoichiometry. This, however, resulted in the growth of an intermediate SiO_2 layer which increased the effective oxide thickness of MOS capacitors, and an optimization of the annealing time was generally needed [3]. Unlike other amorphous materials such as Ta_2O_5 [4], amorphous CeO_2 films have not been investigated for use in capacitor applications. These films can be deposited at lower temperatures which is expected to reduce oxygen deficiency and minimize the initial SiO_2 layer thickness of the films. Crystallization of these films on Si(100) substrates would be very interesting as a Silicon On Insulator (SOI) technology on Si(100) is preferred over a technology on Si(111) substrates for the lower density of surface states on (100) surfaces. This directly relates to a better performance of MOS devices fabricated on a (100) surface of an SOI substrate.

In this work, crystallization of CeO_2 films grown at low temperatures on Si(100) substrates was explored by rapid thermal annealing of a very thin film of CeO_2 grown at room temperature on an Si(100) substrate off-oriented by 4° in the <110> direction as enhanced partial crystallization of CeO_2 films grown by electron beam evaporation on such substrates was reported in the literature [5]. MOS capacitors were fabricated on the CeO_2 films deposited on silicon (100) substrates and characterized by C-V and I-V techniques.

B. Experimental Procedure

Five ohm-cm p-type Si(100) substrates off-oriented by 4° in the <110> direction were cleaned and degassed under UHV as previously described [2]. A preheat to 750°C for 10 minutes was carried out to evaporate contaminants from the silicon surface. The substrate temperature was then reduced to the growth temperature and pulsed laser ablation of a CeO_2 target (99.999% purity) was carried out under pressures lower than 5×10^{-8} Torr during the ablation. The growth temperatures were 20, 40 and 200°C.

Samples of films grown at 20°C of about 50 Å thickness were rapid thermally annealed in argon at 1000°C for 5 and 10 minutes and reloaded into the vacuum system to be examined by

RHEED. Samples of the films grown at 20 and 40°C were *ex situ* annealed in forming gas for 30 minutes at 500°C, and rapid thermally annealed in argon at 1000°C for 5 minutes. MOS capacitor structures were fabricated by evaporating aluminum dots onto the CeO_2 surface and the electrical properties of the films were investigated by C-V and I-V techniques. Films deposited at 200°C were *in situ* annealed at 750°C for 30 minutes. TEM revealed that partial coverage of the silicon surface took place at 200°C and no further work was done on these samples.

C. Results

Figure 1 shows the RHEED patterns observed of films of about 50 Å thickness grown at 20°C and rapid thermally annealed in argon at 1000°C for: (a) 5, and (b) 10 minutes. Figure 2 shows typical high frequency C-V characteristics obtained of as-grown, forming gas annealed ($N_2 + H_2$ for 30 min. at 500°C) and rapid thermally annealed (Ar for 5 min. at 1000°C) films of a thickness of about 300 Å. The breakdown voltages of capacitors fabricated on the as-grown films ranged from 2 to 13 volts with leakage currents of the order of 100 $\mu A/cm^2$ just before breakdown. For the forming gas annealed films, breakdown voltages between 8 and 14 volts were observed with almost the same leakage level before breakdown. For the rapid thermally annealed films lower breakdown voltages around 4 volts and higher leakage currents of about 500 $\mu A/cm^2$ were obtained.

D. Discussion

While the RHEED pattern in Fig.(a) indicates that the films were amorphous even after the RTA for 5 minutes, fading streaks appear in the pattern of Fig.(b) which can indicate a partial crystallization at the films surface after 10 minutes annealing. However, the patterns observed in some spots of the 10 minutes annealed films had bright rings which suggests that another technique is needed to achieve single-crystallization of the films on top of the Si(100) template.

As can be seen from Fig. 2(a), large accumulation capacitances were obtained from as-deposited amorphous films of CeO_2. The value of 2500 pF corresponds to an effective SiO_2 thickness of 8.5 nm of the MOS capacitors. The leakage level of these samples was, however, excessively high resulting in inclined C-V curves in accumulation and deep depletion under positive voltages as inversion charges had probably leaked through the films. Their breakdown voltages varied largely depending probably on the presence of local defects in the films. Forming gas annealing appears to improve the leakage characteristics. Leakage current effects on the C-V curves were less pronounced as can be seen from Fig. 2(b). The films had breakdown voltages which are larger and less scattered in value than those of as-grown films. The capacitance obtained in accumulation was slightly less due probably to the formation of a thin layer of SiO_2 by oxygen to the silicon surface. The annealing temperature which is 500°C

Figure 1(a). RHEED pattern observed of CeO_2 films of about 50 Å deposited at 20°C on Si(100) and rapid thermally annealed in argon at 1000°C for 5 minutes.

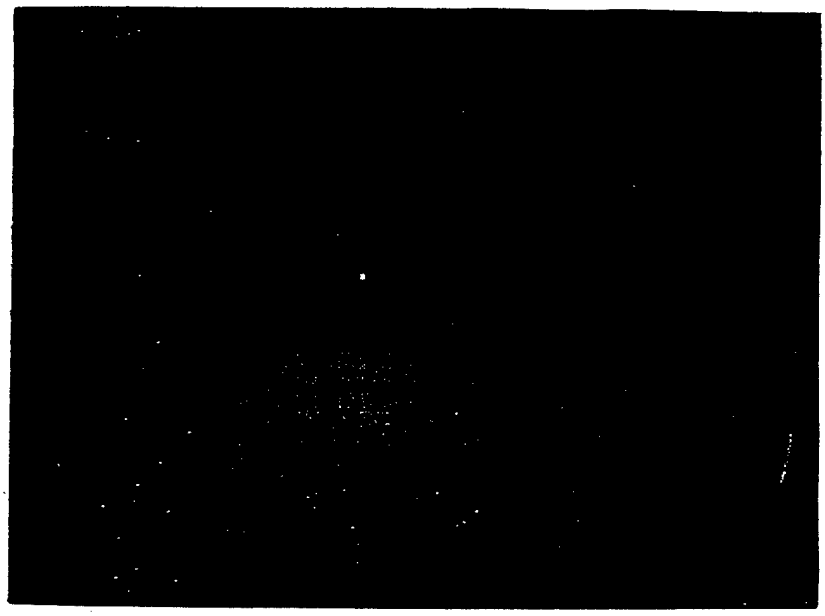

Figure 1(b). RHEED pattern observed of CeO_2 films of about 50 Å deposited at 20°C on Si(100) and rapid thermally annealed in argon at 1000°C for 10 minutes.

is lower than values where the stoichiometry of the films would be affected by a low partial pressure of oxygen in the annealing ambient [6,7]. However, still deep depletion of the silicon surface under positive biases was observed. Films exposed to rapid thermal annealing in argon at 1000°C for 5 minutes had degraded C-V characteristics as seen from Fig. 2(c). They did not reach a maximum capacitance in accumulation up to -10 volts as accumulation charges could have been leaking through the films. The leakage levels of these films were higher than those

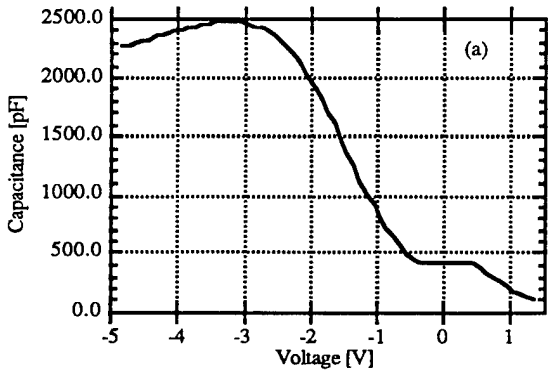

Fig. 2(a). High frequency C-V curves of MOS capacitors with 35 mils diameter fabricated on as-grown CeO_2 films with a thickness of about 300 Å deposited on Si(100) at 40°C, at a frequency of 100 KHz.

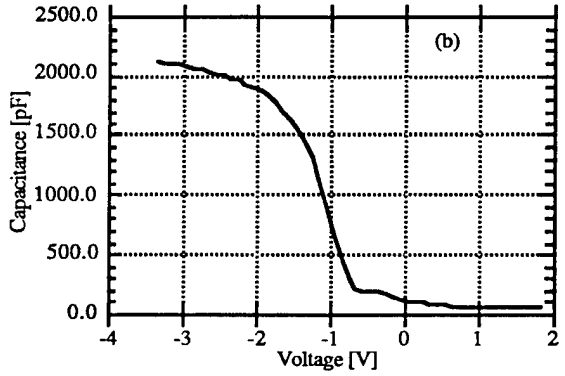

Fig. 2(b). High frequency C-V curves of MOS capacitors with 35 mils diameter fabricated on CeO_2 films with a thickness of about 300 Å deposited on Si(100) at 40°C and annealed in forming gas (N_2 + H_2) for 30 min at 500°C, at frequency of 1 MHz.

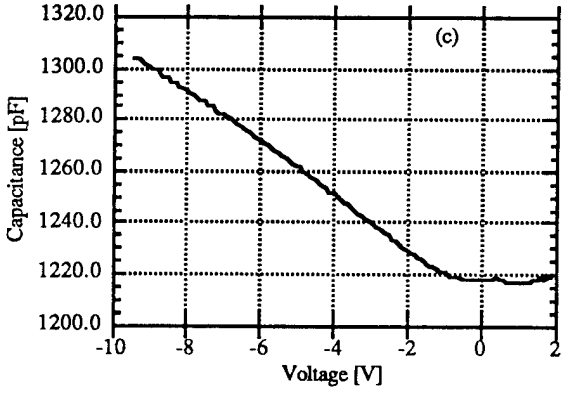

Fig. 2(c). High frequency C-V curves of MOS capacitors with 35 mils diameter fabricated on CeO_2 films with a thickness of about 300 Å deposited on Si(100) at 40°C and rapid thermally annealed in Ar for 5 min. at 1000°C, at a frequency of 100 KHz.

of as-deposited films and their breakdown voltages were lower than those of films annealed in forming gas at 500°C. This can be a result of partial crystallization of the films into polycrystalline CeO_2 or an increase in oxygen deficiency of the films with annealing.

E. Conclusions

Films of CeO_2 were deposited at lower temperatures on Si(100) substrates. Crystallization of very thin CeO_2 films deposited on 4° off-oriented Si(100) by rapid thermal annealing in an argon environment at 1000°C for 5 and 10 minutes was investigated. The RHEED patterns observed indicated partial crystallization at the films surface.

Samples of the deposited films were annealed in forming gas at 500°C for 30 minutes and rapid thermally annealed in argon at 100°C for 5 minutes. The as-grown and annealed samples were characterized by C-V and I-V techniques to explore their potential for use in MOS memory devices. Relatively high accumulation capacitance and high leakage currents were observed of as-grown films. Improved leakage and breakdown characteristics were obtained with forming gas annealing while the rapid thermal annealing resulted in enhanced leakage through the films.

E. Future Research Plans and Goals

Crystallization of CeO_2 films on Si(100) surfaces for a SOI technology on Si(100) substrates is very interesting and will be further investigated. Ways to reduce the leakage currents of as-deposited amorphous CeO_2 films on silicon substrates are also to be investigated. Characterization of MOS capacitors of epitaxial CeO_2 films on Si(111) substrates with optimized oxygen annealing times is now in progress and will soon be reported.

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V. Influence of Temperature and Methane Concentration on the Diamond Growth Parameter α on Silicon and Titanium Substrates

A. Introduction

Diamond has become an enticing candidate for high-power, high-frequency electronic device applications in high-temperature or chemically-harsh environments. However, to realize its true potential, single-crystal diamond films are needed. Although economically viable sizes and quantities of substrates for single-crystal diamond films are still not available, there has been significant progress on oriented diamond films [1-3]. Under certain growth conditions, strongly oriented diamond films can be obtained by taking advantage of the growth competition between differently oriented diamond grains [4]. In order to take advantage of the texture evolution process, it is essential to understand the growth parameter α which is given by the relative growth rates on {100} and {111} facets [5-7]. The growth parameter α can be represented by the simple formula, $\alpha = \sqrt{3}\ (V_{100}/V_{111})$ where V_{100} and V_{111} are the growth rates on the {100} and {111} faces, respectively.

To gain the precise information about the growth parameter α on silicon and titanium in our system, investigation of the dependence of the morphology of diamond films on methane concentration and deposition temperature was undertaken. After deposition, the morphology of each sample was examined by the scanning electron microscope (SEM). The values of α were determined by comparing the surface morphologies with the idiomorphic crystal shapes for different values of α described by Wild [6]. While there have been some experimental results of the growth parameter α on silicon, understanding the growth parameter α on titanium remains elusive. Investigating the α parameter space on titanium is desirable because of its potential application as an interlayer for diamond nucleation on otherwise "difficult to nucleate" materials, such as copper and steel. Also, comparison of "α maps" for silicon and titanium may elucidate some mechanisms of diamond growth.

B. Experimental Procedure

Substrate Preparation. The polycrystalline titanium samples were polished using progressively finer media. The polishing scheme started with 600 grit SiC, then 30μm and 6μm diamond powder and finished using a colloidal silica solution that polished by mechanical and chemical means. Following the polishing, the sample was cleaned by acetone, methanol, and isopropanol. The silicon (100) substrates were etched in dilute HF acid prior to insertion into the chamber.

Four-step Deposition Process. The four-step deposition process consisted of a hydrogen plasma clean, surface carburization, biased enhanced nucleation (BEN), and growth. Hydrogen plasma clean was performed for 30 minutes to remove any carbonaceous residue on

the substrates. Following the hydrogen plasma clean, the carburization step was undertaken for 30 minutes at 2% methane/hydrogen concentration at 25 Torr. After the carburization step, the samples were subjected to a nucleation step. At the nucleation step, the chamber pressure was reduced to 20 Torr and methane/hydrogen ratio was increased to 5%. Then a negative DC voltage, about -240 V, was applied to the substrate for 8 minutes. At the end of the biasing step, the bias voltage was terminated and the pressure was raised to 25 Torr. In the growth stage, the substrate position and methane/hydrogen concentration was changed to the desired point. Table I summarizes the system parameters for each step.

Table I. Summary of System Parameters

Parameters	H_2 Plasma Clean	Carburization	BEN	Growth
Power	600W	600W	600W	600W
Pressure	25 Torr	25 Torr	20 Torr	25 Torr
CH_4/H_2 ratio	-	2%	5%	varied
Bias Current	-	-	80 mA	-
Bias Voltage	-	-	-240V	-
Temperature	700°C	800°C	850°C	varied
Duration	30 minutes	30 minutes	8 minutes	16-17 hours

Growth Conditions. From previous experience, the following upper and lower limits on methane concentration (0.1%–1.0%) and deposition temperature (700°C–900°C) were chosen. In order to have the best representative data points, a statistical experimental design software package (Strategy) was used to determine the different deposition conditions within the limits. The resulting deposition was observed by SEM and isolated diamond particles were examined to determine the α value. Approximate α values were assigned using the idiomorphic crystal shapes described by Wild [6] and further discussed by Tamor [7]. Although a different chamber system and operating parameters were used, the diagram composed by both researchers gave a general gradient of α. The idiomorphic crystal shapes and α diagram composed by Wild is in Fig. 1. The value of α increased with decreasing deposition temperature and increasing methane concentration. Table II summarizes the five different deposition conditions.

C. Results and Discussion

Deposition on Silicon. Well-defined facets were observed at all deposition conditions, except for the low methane concentration and low temperature sample (Sample 4). The

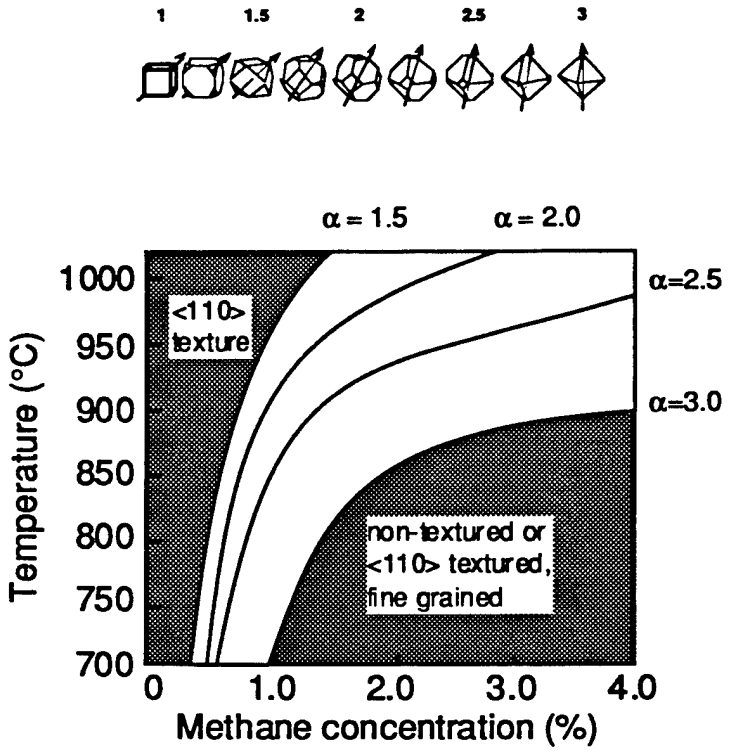


Figure 1. Idiomorphic crystal shapes and α diagram composed by Wild.

Table II. Deposition Conditions for Each Sample

Sample Number	CH_4%	Temperature
1	0.27	900±10
2	1.00	700±10
3	0.60	800±10
4	0.10	700±10
5	0.93	900±10

corresponding α value and SEM image of each sample is shown in Table III and Figs. 2(a-d), respectively. The diamond crystals on the Sample 1 showed cubo-octahedral shape morphology as in Fig. 2(a). Since adjacent (111) faces and adjacent (100) faces were touching, the corresponding α value was about 1.5. Figure 2(b) shows the crystal morphology of Sample 2 which had truncated-octahedral shaped crystals. Compared to the idiomorphic crystal shape for $\alpha = 2$, Sample 2 had slightly larger (100) faces. Thus, the α value for Sample 2 was determined to be about 2.2. Sample 3 had a similar particle morphology to Sample 2 (Figs. 2c and 2b, respectively), although the (100) faces appeared to cover more of the crystal surface

than in Sample 2. Therefore, the α value for Sample 3 should lie between 2.2 and 1.5 and a value of 2.0 was assigned. Sample 5 had a similar morphology to Sample 1 (i.e. adjacent (111) and adjacent (100) faces intersected at a point), corresponding to α value of 1.5. As expected, the gradient of α followed the same trend as discussed by Wild [6] and Tamor [7]. Alpha increased with decreasing deposition temperature and increasing methane concentration. Based on this preliminary evaluation, an initial α diagram for diamond growth on silicon is shown in Fig. 3.

Table III. Corresponding α Values for Each Sample

Sample Number	α Value on Si	α Value on Ti
1	1.5±0.1	heavily twined particles
2	2.2±0.1	"
3	2.0±0.1	"
4	heavily twined particles	"
5	1.5±0.1	"

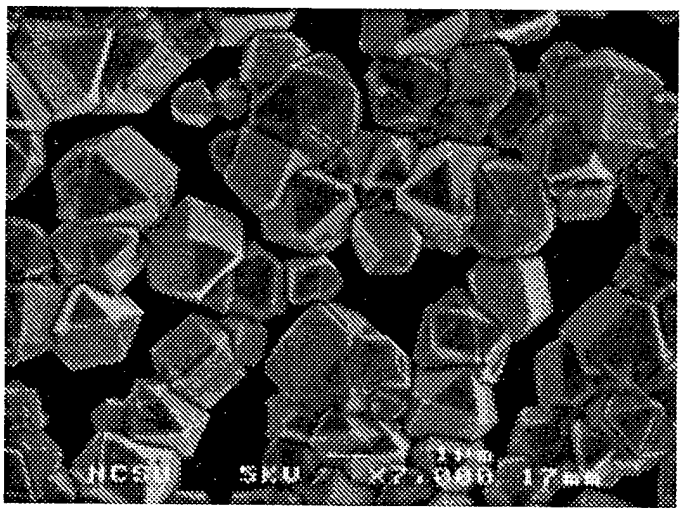
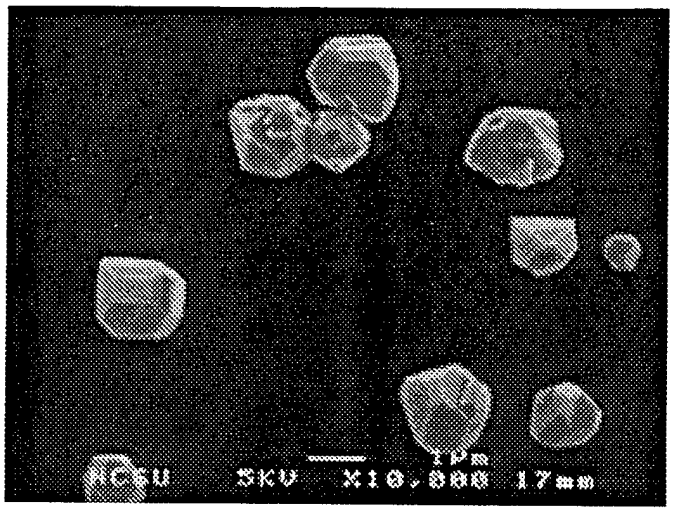
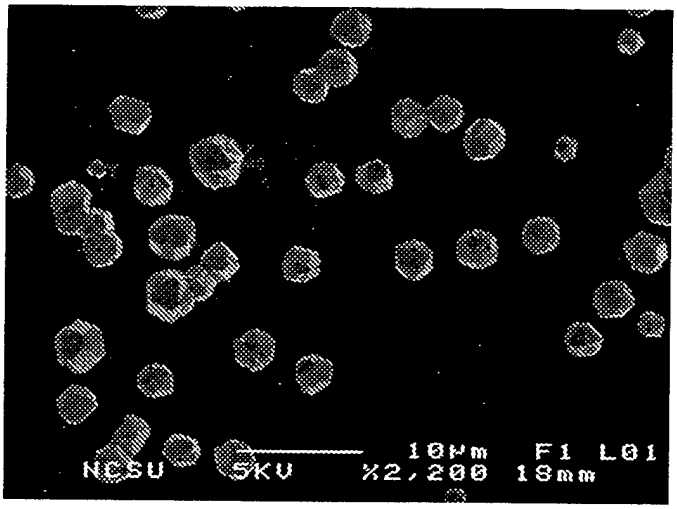


Figure 2(a). SEM image of Si Sample 1 ($CH_4\% = 0.27\%$, $T_{sub} = 900°C$).

(b)



(c)



(d)

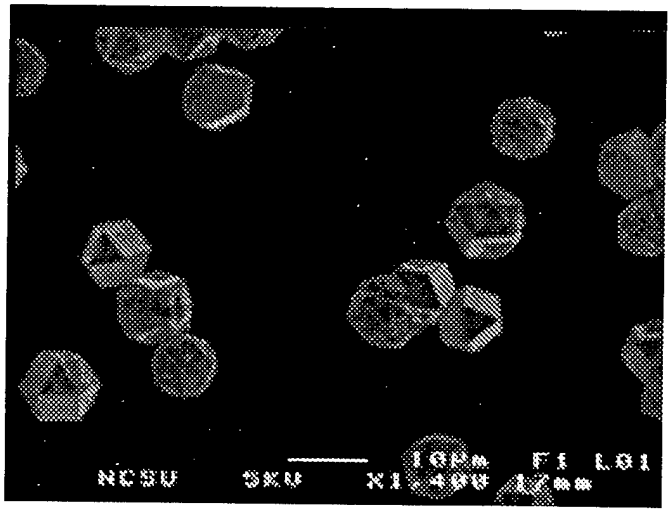


Figure 2 (b) SEM image of Si Sample 2 ($CH_4\%$ = 0.1%, T_{sub} = 700°C); (c) SEM image of Si Sample 3 ($CH_4\%$ = 0.6%, T_{sub} = 800°C); (d) SEM image of Si Sample 5 ($CH_4\%$ = 0.93%, T_{sub} = 900°C).

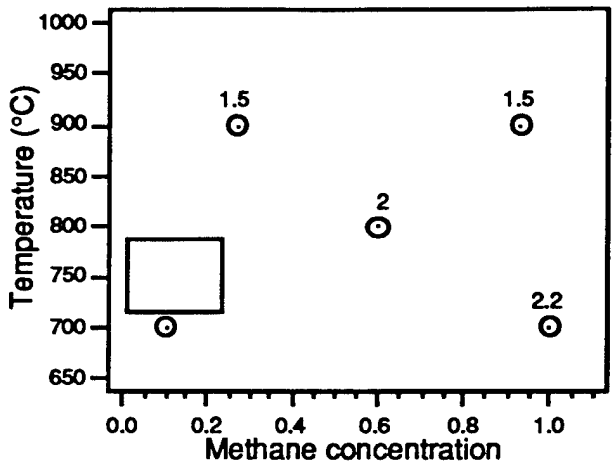


Figure 3. Alpha diagram for diamond growth on Si.

Deposition on Titanium. In the case of titanium, all of the samples had heavily twinned "cauliflower-like" morphologies as shown in Fig. 4. The absence of diamond particles with well-defined facets made determination of α impossible. In order to examine the growth parameter α on titanium, the twinning needed to be reduced as much as possible. There are several factors which may have contributed to the twinning of diamond on titanium: i) surface roughening after oxide removal, ii) hydride formation, iii) amorphous carbide formation, and iv) high surface mobility of carbon species. The first possible explanation for the twinning of diamond would be the surface roughening after oxide removal during the hydrogen plasma cleaning. Because titanium is a strong oxide former, substantial amount of oxide was likely formed during the substrate preparation stage. Since the interface between titanium and its oxide was probably not as smooth as the polished original surface, a rough surface would have resulted after etching by the hydrogen plasma. This rough surface may have contributed to the formation of twins in diamond. Another possible reason for heavy twinning can be found from its deposition environment. Throughout the deposition steps, titanium substrates were exposed to a hydrogen environment. Formation of a hydride could have occurred and would embrittle the titanium surface. As the substrate was heated by the plasma, differences in the thermal expansion coefficient may have caused cracking of the surface. These small cracks could have served as nucleating sites for non-uniform diamond particles and might have been responsible for heavily twined particles. The next factor may have been the formation of an amorphous carbide during the carburization step. Since amorphous carbide does not have long range order, it can easily contain defects that may contribute to the twinning. The last and more speculative reason would be the effect of surface mobility of carbon species on the titanium surface. Compared to silicon, titanium has much lower thermal conductivity; therefore, the surface temperature of titanium may have been higher than silicon. Since titanium might have had a

higher substrate temperature, the carbon species on titanium could migrate more easily, leading to a higher local carbon concentration. The higher carbon concentration would lead to twinning of the diamond crystals. Among the four factors, surface roughening after etching the titanium oxide layer, during the hydrogen plasma clean stage, is probably the most dominant factor, although further investigation is needed.

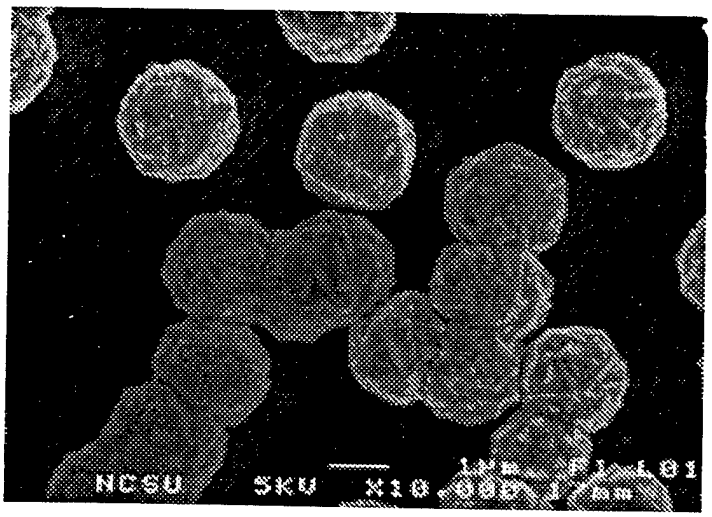


Figure 4. SEM image of typical diamond crystals on Ti.

D. Conclusions

The growth parameter α has been studied on silicon and titanium by investigating the dependence of films morphology on methane concentration and deposition temperature. On silicon, a range of α values was determined for diamond crystals deposited under a range of substrate temperature and methane concentration conditions. From this data, an initial α map was generated. The diagram confirmed the α gradient; the value of α increased with decreasing deposition temperature and increasing methane concentration. Under the same conditions, only heavily-twined diamond particles were found on the titanium substrates. Possible mechanisms which may have contributed to the twinning of diamond include surface roughening after oxide removal, hydride formation, amorphous carbide formation, and high surface mobility of carbon species. The surface roughening of the titanium after oxide etching is probably the most dominant factor.

E. Future Research Plans and Goals

In order to have a more detailed diagram, more samples with different methane concentrations and deposition temperatures need to be examined. The goal of this research is to grow highly oriented (100)-faceted diamond film on a silicon (100) substrate. On titanium substrate, since well-faceted diamond particles could not obtained, non-twined diamond

particles need to be nucleated in order to study the growth parameter α. To reduce the effects of surface oxide layer, it is planned to deposit a thin layer of titanium on silicon then transfer the sample to microwave plasma chemical vapor deposition system to grow diamond. Since the evaporation deposition system is connected to the microwave plasma chemical vapor deposition system, the sample can be transferred between two chambers without exposing it to air.

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