FR-10158

A Final Report for:

InP SOLAR CELL DEVELOPMENT ON INEXPENSIVE Si SUBSTRATES

Submitted under:

Phase I Contract No. N00014-94-C-2030

Submitted to:

Scientific Officer
Naval Research Laboratory
Attn: Dr. Geoffrey Summers Code: 6615
Ref: Contract N00014-94-C-2030
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Washington, DC 20375-5326

spire

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ABSTRACT

Indium phosphide (InP) solar cells were made on silicon (Si) wafers to take advantage of both the radiation-hardness properties of the InP solar cell and the light weight and cost savings of Si wafers compared to either InP or germanium (Ge) wafers. Calculations are presented which show that in very high radiation environments (*e.g.* van Allen proton belts), these cells can provide over twice as much EOL power density than GaAs/Ge or Si cells. Both P/N and N/P cell architectures were examined since each may have advantages depending on the radiation environment. N-on-P (N/P) InP-on-Si (InP/Si) 2 cm by 4 cm cells were made with one-sun air mass zero (AM0) beginning-of-life (BOL) efficiencies up to 12.5%. The average efficiency of fifteen (2 cm by 2 cm) InP/Si cells on 16 mil Si wafers sent to NASA-Lewis for independent efficiency verification was 12.3% (best cell 12.6%). Data are presented comparing 1 MeV electron and 3.9 MeV alpha particle irradiation showing relatively little cell power output degradation out to a very high fluence (less than 20% after a fluence of about 4×10^{16} 1 MeV electrons/cm^2, about 40X the "standard" fluence). N/P cells have better overall performance than P/N cells up to equivalent 1 MeV electron fluences of $\sim 3 \times 10^{16}$ cm^{-2}, or about 30X the current "standard" of 10^{15} 1 MeV electrons /cm^2. P/N cells had BOL efficiencies up to 9.9%, due to a lower photocurrent than N/P cells since a thin emitter is hard to obtain with high diffusivity zinc P-type dopant. However, for equivalent fluences in excess of 3×10^{16} 1 MeV electrons/cm^2, some proton irradiation data indicates that the P/N InP/Si cells may have more power output in this regime than their N/P counterparts.

1 EXECUTIVE SUMMARY

Indium phosphide (InP) solar cells were made on silicon (Si) substrates (wafers) to combine the exceptional radiation hardness[1,2] and high efficiency[3,4] (19% air mass zero AM0) of InP solar cells with inexpensive, strong, lightweight Si wafers for space power missions. InP solar cells degrade much less than GaAs and Si cells under high irradiation, making them uniquely suitable for long-duration radiation-belt missions. However, since InP wafers are fragile, thick (~20 mil) InP wafers are needed to avoid breakage. Cost, weight, and fragility of InP wafers have impeded InP cell use. InP cells on lightweight, strong, inexpensive Si wafers (InP/Si cells) are therefore of great interest. A lower beginning-of-life (BOL) efficiency due to dislocation defects is compensated by the lighter Si wafer. Si density (2.3 g/cm^3) is less than half that of InP (4.8 g/cm^3), gallium arsenide (GaAs) or germanium (Ge), and since Si is much stronger than InP, thinner wafers can be used. A 12.5% InP cell on a 16 mil Si wafer has 65% higher cell power density than a 19% InP cell on a 20 mil InP wafer at BOL. After heavy irradiation (>10^{16} 1 MeV electrons/cm^2), the end-of-life (EOL) efficiencies become similar, and the EOL cell power density is ~250% higher because InP/Si is lighter than a cell on an InP wafer. Si wafers are also inexpensive (~ 2% of the cost of InP wafers).

The Phase II tasks were:

- Optimize emitter and base dopants used in InP/Si cell to improve efficiency
- Optimize the InP/Si cell fabrication technology
- Deliver N/P and P/N InP cells to NRL for radiation studies
- Examine grading layers and dislocation reducing techniques to improve cell
- Examine the effects of Si wafer thickness on cell mechanical integrity
- Produce large area cells (2 cm by 4 cm) to demonstrate scale-up capability

In this Phase II, 286 InP cells and 1106 DLTS diodes on InP and Si wafers were delivered. The Phase II results for each of the above tasks were:

- Se 3 x 10^{19} cm^{-3} N-emitter and Zn 10^{17} cm^{-3} P-base gave highest efficiencies
- Alloyless contacts of Ti/Pt/Ag/Au to Si and Cr/Ag/Au to InP worked well
- 141 N/P and P/N test cells were delivered to NRL, instead of the 100 required
- Both InGaP grading layers and an InP thermal stress buffer were examined
- Cells were grown on 8, 12, 16, and 25 mil Si (only 8 mil wafers too thin)
- 2 x 4 cm^2, 12.5% AM0, 28°C, N/P InP/Si cells were made
- 1 x 1 cm^2 P/N InP/Si cells were made with efficiencies up to 9.9% AM0, 28°C

Other highlights of the Phase II program were:

- A unique (patent applied) InP thermal stress buffer was best at reducing dislocations
- InP/Si cells 8X larger than previous record-efficiency InP/Si cell were made
- Phase II InP/Si cells had 30% higher efficiency than the previous best InP/Si cells
- Phase II InP/Si cells had 60% higher efficiency than the previous Phase I InP/Si cells
- NASA tests of 15 2 x 2 cm^2 cells show average efficiency 12.3% (best cell 12.6%)
- The epitaxial process used for the Phase II cells does not need lattice-matched $In_XGa_{1-X}As$ or $In_XGa_{1-X}P$ materials and therefore should be very manufacturable

2 OVERVIEW

N/P InP-on-Si (InP/Si) cells were made to combine lightweight Si wafers (half the density of GaAs, Ge or InP) with the proven radiation-hardness of InP solar cells to achieve a high end-of life (EOL) power density. By making heteroepitaxial InP solar cells on Si (instead of InP) wafers, we are essentially trading off some beginning-of-life (BOL) efficiency (reduced due to InP/Si material dislocations) to increase the EOL power density by decreasing the substrate (wafer) weight by over 50%. Since the cells are very radiation-hard thin, top coverglasses can be used, and little backside shielding from the array material is needed to obtain high EOL power density. Since the InP cells are now also on light Si wafers, these light cells can better take advantage of new, lighter weight flex arrays.

The key idea which drove this work is the realization that the EOL efficiency of InP solar cells on Si wafers is similar to that of InP solar cells on InP wafers. At high radiation fluences, the minority carrier lifetime of cells on InP wafers becomes limited by radiation damage, and seems to become similar to InP cells on Si wafers where the lifetime is limited by dislocations due to the lattice-mismatched heteroepitaxial growth. Therefore, for high radiation missions, there is little efficiency penalty for placing the InP cell on a Si wafer instead of an InP wafer. However, there is a tremendous weight advantage if a thinner Si wafer can be used versus an InP wafer, since the Si is a much stronger material, and the Si density is half that of InP.

N-on-P (N/P) 1 x 1 cm^2 9.9% AM0 cells were the best[5,6] InP cells on Si wafers (InP/Si) prior to this program. In Phase I, Spire made 8.2% AM0 1 x 1 cm^2 P/N InP/Si cells. In Phase II, we improved this to 9.9%, so that P/N cells matched the previous best N/P cells. We also improved N/P InP/Si efficiency by 50% (to 12.5% AM0) on 8X larger cells (2 x 4 cm^2) than the prior best N/P cells. This improvement was made by reducing the dislocation density. Recombination at dislocations (defects which relieve stress due to the 8% InP/Si lattice-mismatch) is the main limit on efficiency.

The efficiency goal for 8% mismatch InP/Si cells is based on 4% mismatch InP/GaAs cells demonstrated by NREL. These cells[7,8] used an $In_XGa_{1-X}As$ grading layer and reported a 13.7% AM0 active area efficiency under a prismatic cover. Active area (*i.e.* busbar and contact area not counted) efficiency testing is not the standard for one-sun cells. Also, the prismatic coverglass, not now useful in space due to UV degradation, improved the efficiency by eliminating gridline shadow, and by allowing more and wider grids for minimal I^2R loss.

However, despite factors which complicate the comparison, this work showed that a hetero-epitaxial InP cell with a substantial dislocation density can achieve efficiency similar to standard Si space cells (*e.g.* 14% ASEC 2 Ω -cm BSR).

In Phase II, Spire achieved NASA-verified, total area (*i.e.* including busbar and pads) 12.6% AM0 efficiency, without prismatic cover, for the best InP/Si cell[9]. The cells use a simple thermal-stress InP buffer to lower dislocations, and are more manufacturable than cells using an $In_XGa_{1-X}As$ grade. These cells have beginning-of-life (BOL) efficiency and weight similar to Si, while end-of-life (EOL) efficiency should be much higher than Si or GaAs/Ge after heavy irradiation.

Figure 1 presents calculations showing that the EOL panel power density of 12.5% BOL InP cells on 16 mil Si wafers can be over twice as high as 20% BOL GaAs cells on very thin 5.5 mil Ge wafers in the most severe high radiation orbit (~5000 km, in the van Allen belt). This EOL power density (and not the BOL efficiency) is the key parameter for most communication satellite power systems flying in highly elliptical orbits or other high-radiation exposure missions. The calculation in Figure 1 was done assuming an optimized coverglass (either 3, 6, 12, 20 or 30 mils) for each particular cell type at each particular altitude (mission). The same panel substrate weight (1.2 kg/m^2) was assumed for all technologies. The backside effective coverglass thickness (panel substrate plus cell wafer) used was 38 mils for InP cells on 16 mil Si wafers, 30 mils for the 8 mil Si cells, and 35 mils for GaAs cells on 5.5 mil Ge.

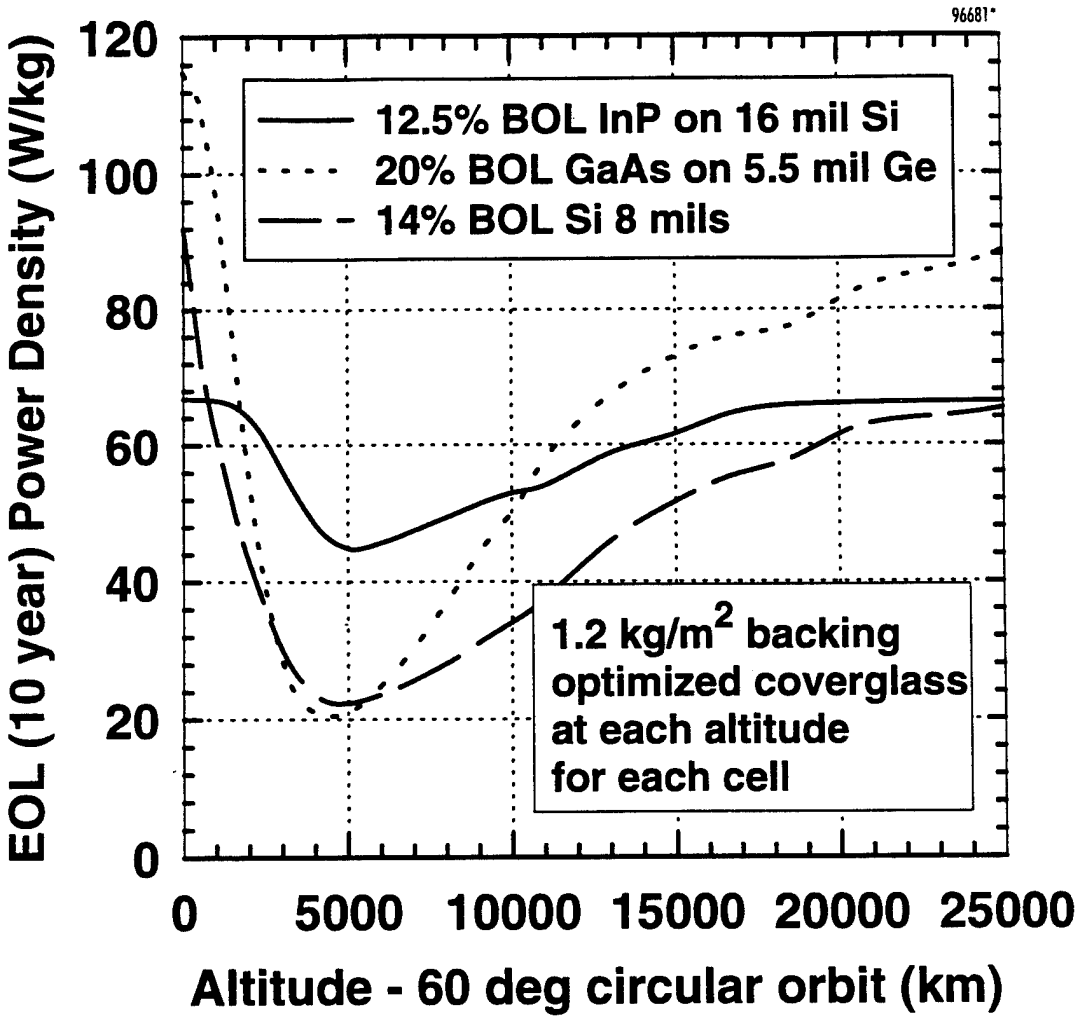

Figure 1 *Calculated end-of-life power density for 12.5% BOL InP cells on 16 mil Si wafers vs 20% BOL GaAs cells on 5.5 mil Ge wafers and 14% BOL Si cells on 8 mil wafers. All calculations were made with a coverglass optimized to the particular cell technology and orbit. All data assume a 1.2 kg/m^2 panel substrate. Figure shows a range of orbits (~2000 to 10000 km) where the present InP/Si cells have higher EOL power density than even advanced 20% GaAs cells on 5.5 mil Ge wafers.*

3 DISCUSSION OF P/N VS N/P InP CELLS

During Phase I, we concentrated on P/N cell development since Si atoms, out-diffusing from the Si wafer during the ~4 hour, 600°C epitaxial growth, would dope any III-V layer immediately adjacent to the Si wafer N-type. Therefore, a P/N design, in which the III-V layer adjacent to the Si wafer would be N-type, would be unaffected by the diffusing Si, while an N/P design, in which the adjacent layer is to be P-type, would have a blocking junction formed when this adjacent layer would be converted N-type by the diffusing Si atoms, resulting in a sandwich between the P-type Si wafer below it and the P-type III-V layers above it. In order to eliminate the blocking junction, a tunnel junction is added to an N/P cell design. However, even though a P/N InP/Si cell seems simpler, the P-type emitter of a P/N cell poses several difficulties versus N/P InP/Si cells (Table 1).

Table 1 *Comparison of n/p versus p/n InP cell properties.*

	N/P InP Cell	P/N InP Cell
Minimum Emitter Resistivity P: MO5-3596 N: MO5-3597	~ 0.00022 Ω-cm Max. doping: 5.1×10^{19} cm^{-3} 300K Mobility: 560 cm^2/V-s	~ 0.07 Ω-cm Max. doping: 1.4×10^{18} cm^{-3} 300K Mobility: 64 cm^2/V-s
Minimum Emitter Thickness	~300 Å same thickness as epilayer	~1000 Å thicker due to Zn diffusion
Emitter Thickness Control	negligible diffusion of Se-dopant; minimum emitter thickness limited by minimum growth time (~30s) due to Se "memory" effect	Zn has high diffusivity (~ 6×10^{-13} cm^2/s @600°C[10]); thickness limited by diffusion during InGaAs growth (400s for 0.3 μm contact cap)
Tunnel Junc. if on Si Wafer?	Yes	No
May Have More Power for Equivalent 1 MeV Fluence	less than ~3×10^{16} cm^{-2}	greater than ~3×10^{16} cm^{-2}
Best Cell on Si Wafer N/P: 5823-3427-2 P/N: 5803-3327-1	AM0 BOL Eff: 12.6% Voc: 756 mV Jsc: 31.7 mA/cm^2 FF: 72% 4 cm^2, NASA-test	AM0 BOL Eff: 9.9% Voc: 722 mV Jsc: 28.7 mA/cm^2 FF: 65% 1 cm^2, Spire-test
Best Cell on InP Wafer (Upper Limit for InP/Si Cell) N/P: 5367-6-1 P/N: 5646-2478-28	AM0 BOL Eff: 19.1% Jsc: 36.3 mA/cm^2 Voc: 876 mV FF: 82.4% 4 cm^2, NASA-test	AM0 BOL Eff: 16.9% Jsc: 33.5 mA/cm^2 Voc: 886 mV FF: 78.3% 0.25 cm^2, Spire-test

Emitter thickness is a critical parameter in cells without window layers (*i.e.* a higher bandgap passivating semiconductor on the emitter). A basic tradeoff exists for both P/N and N/P InP cells. A thinner emitter limits the number of carriers photogenerated in the emitter which can subsequently be lost to surface recombination, improving Jsc, while a thicker emitter lowers Jsc, but also lowers the I^2R loss due to the emitter layer sheet resistance, increasing the fill factor.

Table 1 shows the maximum N and P doping and mobility at that doping in InP by MOCVD. N/P InP cell BOL efficiency is higher than P/N because an N-emitter can be doped ~30X higher with ~10X higher mobility than holes, allowing a thin emitter with less I^2R and surface recombination loss. Emitter resistivity is ~300X higher for a P/N InP cell than an N/P cell, so that a more dense contact grid and a thicker emitter must be used to limit the I^2R loss; however, a denser grid means more light reflection loss, and a thicker emitter increases surface recombination loss, both of which lower Jsc. Also, the zinc (Zn) dopant in the P/N emitter has a high diffusivity, and it was challenging to understand and control the emitter thickness (Figure 2) in P/N cells.

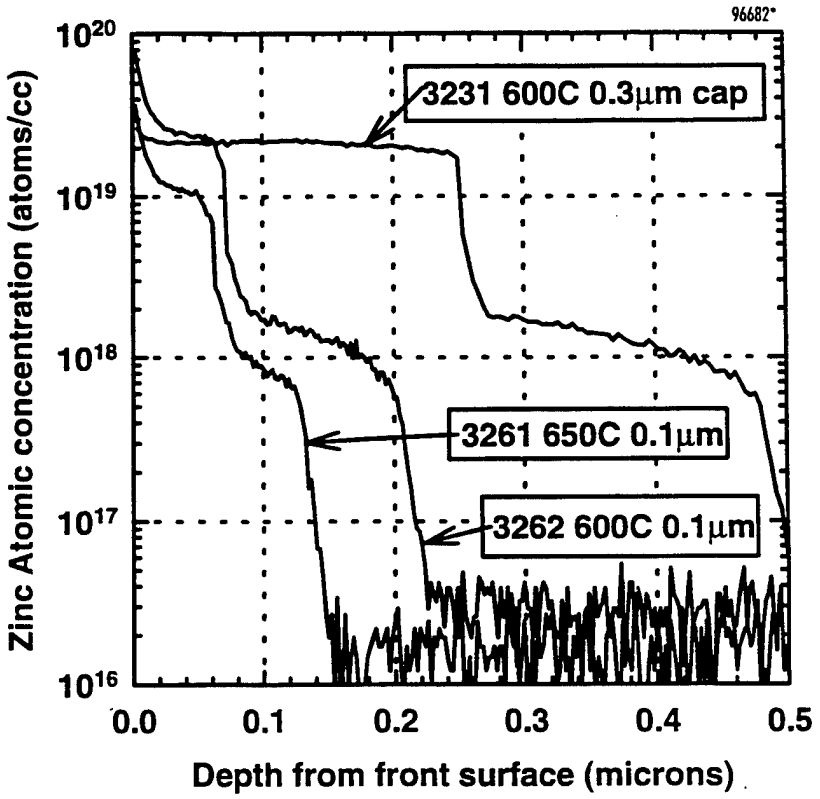

Figure 2 *Secondary ion mass spectroscopy (SIMS) profile of Zn in p/n InP cells on InP wafers. InP emitter thickness is controlled by zinc diffusion from InGaAs contact cap (initial flat area of each curve), and depends on cap thickness and growth temperature (in labels). Target cap thicknesses are offset ~ 500Å from SIMS data. At 600 °C, a 0.3 μm cap gave a ~2400Å InP emitter. One-third the diffusion time (0.1 μm cap) gave a ~1300Å InP emitter, in agreement with $(Dt)^{1/2}$ law. We were surprised a higher (650 °C) temperature gave a thinner (~ 1000Å) emitter, however. This effect may be due to either less Zn incorporation at 650 °C or a lower diffusion coefficient due to perhaps less defective material growth at the higher temperature.*

Figure 2 shows that even for higher quality InP cell material grown on InP wafers, in all cases the P-type Zn-doped InP region thickness (p-n junction depth) was controlled by the Zn diffusion and was about 1000Å at its thinnest (the 650°C curve), compared with the junction depth that was "expected" from the actual P-type InP epitaxially-grown layer thickness, which in all cases was only ~500Å. We noted in the caption of Figure 2 that we were surprised that a higher growth temperature resulted in less zinc diffusion. We received a second surprise when the InP P/N cells on Si wafers did not exhibit greater zinc diffusion than their counterparts on InP wafers. We expected more diffusion since the InP/Si cell material has about 10^7 dislocations/cm^2, and defects normally accelerate diffusion. However, Figure 3 shows a P/N InP/Si cell[11] grown at the same temperature and same InGaAs cap thickness as one of the Figure 2 curves. In both cases, the junction depth is ~2400Å, about the same.

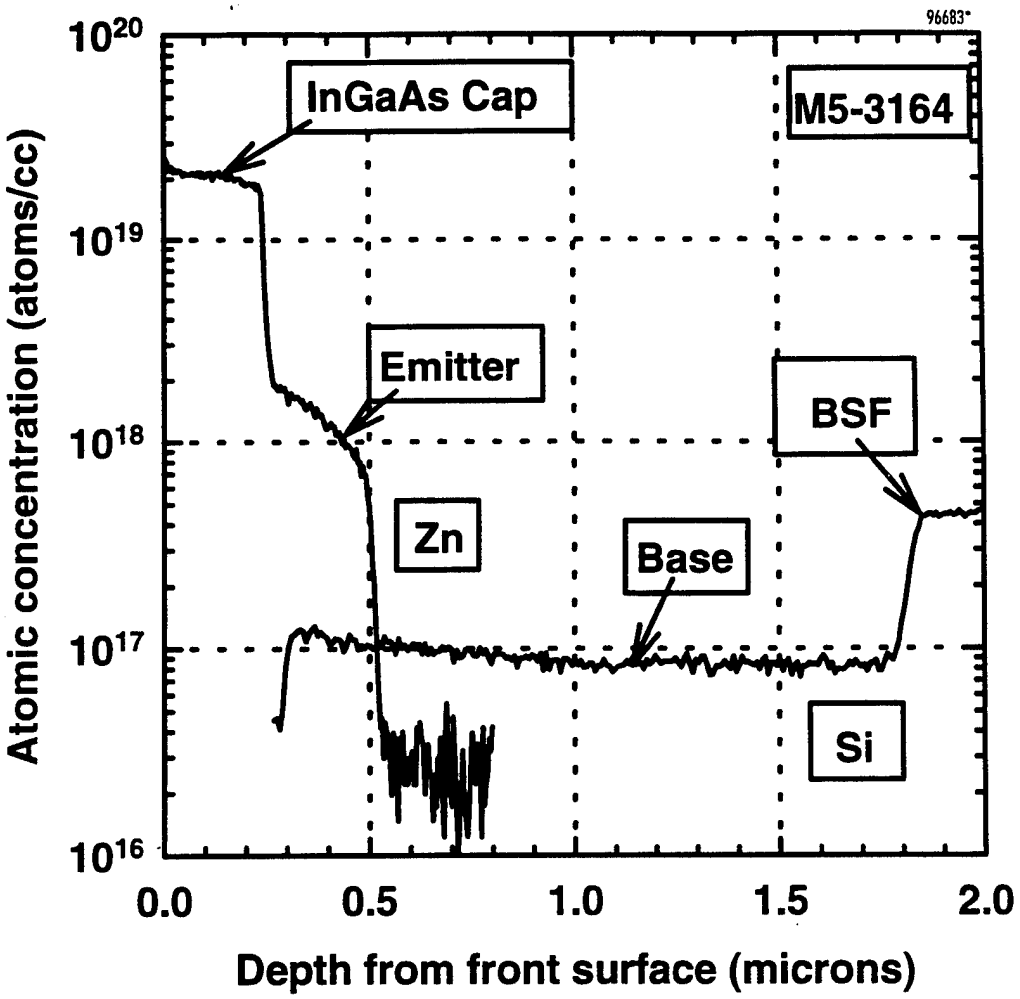

Figure 3 *SIMS profile of Zn (P-type dopant) and Si (N-type dopant) in P/N InP cell on Si wafer. Emitter thickness is about 2400Å, same as for corresponding (600 °C, 0.3μm cap) Zn profile on an InP wafer. It is remarkable that the Zn diffusion was not noticeably enhanced by the dislocations present in the InP/Si material.*

For the Phase I effort and about half the Phase II effort, Spire developed P/N InP/Si cells. Towards the middle of the Phase II, we compared, in a side-by-side controlled experiments, P/N InP/Si cells, which we had just spent over a year developing, and an N/P InP/Si cell with a tunnel junction which had no previous development. The data (Table 2) indicates the undeveloped N/P cells were significantly (about 10% relative) superior in efficiency than the P/N cells. Table 2 shows that the P/N cells had a only a 2% lower photocurrent than the N/P cells, but had a 10% lower fill factor. In fairness to the N/P cells, it should also be pointed out that the gridline spacing used for these cells was a denser grid (10 μm lines on 260 μm centers, 3.8% shadow) optimized entirely for the P/N cells. Although the same photomask set was used for the N/P cells, the N/P cells are optimal with a grid spacing half as dense as for the P/N cells (10 μm lines on 600 μm centers, 1.7%) so that the photocurrent for the N/P cells would be at least 4% greater than the P/N cells.

Table 2 *Data and epilayer structure for first p/n versus n/p InP/Si cell comparison.*

	11.0% AM0 N/P Cell Voc: 713 mV Jsc: 29.2 mA/cm^2 FF: 72% Cell ID: 5803-3318-12			**9.9% AM0 P/N Cell** Voc: 722 mV Jsc: 28.7 mA/cm^2 FF: 65% Cell ID: 5803-3327-1		
Growth Rate: ~6.4 Å/s	Doping cm^{-3}	Thickness μm	Comments 600C growth	Doping cm^{-3}	Thickness μm	Comments 650°C growth
InGaAs Cap	N Se $5x10^{19}$	0.12	not critical	P Zn 10^{19}	0.12	control emitter
InP Emitter	N Se $5x10^{19}$	0.04	5cc 60s	P Zn 10^{18}	0.06	100s
InP Base	P Zn $5x10^{16}$	3	background	N Si $2x10^{17}$	3	helps control junction depth
InP BSF	P Zn 10^{18}	0.5	max doping	N Se $5x10^{19}$	0.5	max doping
InP Dislocation Reduction	P Zn $3x10^{17}$	5	600°C buffer min Zn diff	N Si 10^{19}	5	675°C buffer
InGaAs TJ	P Zn 10^{19}	1	Zn diffusion	omitted	omitted	
InGaAs TJ	N Se $5x10^{19}$	1	max doping	omitted	omitted	
InP Buffer	N Se$5x10^{19}$ N Si 10^{19} N undoped	0.5 1 thin	initialize Se Si by Si wafer 60s spacer	N Si 10^{19} N undoped	1 thin	Si by Si wafer 60s spacer
GaAs Nucleation	N undoped	thin		N undoped	thin	
Si Wafer	N As 10^{19}	25 mils	4° off 100	N As 10^{19}	25 mils	4° off 100

In general, in this experiment (Table 2), we tried to keep the nucleation layer steps and thicknesses of the dislocation reduction buffer and cell the same, while allowing the rest of the structure to be optimized for whether a P/N or N/P cell was grown.

For the P/N cell, we had found a 650°C cell with a 0.12 μm InGaAs cap gave the best performance on an InP wafer (5646-2478, Table 1), and therefore used a similar cell on InP/Si. In addition, we expected that the defect-reduction buffer grown at 675°C should be better than a lower temperature 600°C buffer used in the N/P cell since the dislocations should annihilate each other more easily at the higher temperature (exponential activation energy). The P/N cell had an epitaxially grown emitter of about 600Å, but the actual junction depth was substantially larger (about 1000Å) due to the Zn diffusion from the InGaAs cap (*e.g.* Figures 2 and 3). A higher base doping was used in the P/N cell to help control the junction depth; the higher the base doping, the closer to the cell surface the Zn diffusion concentration equals the N-type base doping.

The N/P cell buffer was kept at 600°C, not 675°C, because of concern that, with the tunnel junction on the bottom of the buffer, a high temperature, thick 675°C buffer would cause the Zn in the InGaAs tunnel junction to diffuse, ruining its abruptness and widening its tunneling depletion width. The tunnel junction was placed at the bottom of the buffer, where the dislocation density was the greatest, so that the maximum number of dislocations would shunt the tunnel junction, making the junction even more ohmic. The tunnel junction did indeed work. Finally, use of a thin GaAs interface layer to enhance InP growth nucleation also seemed avoid the wafer bowing problem we had observed in Phase I with thick GaAs interfaces, as well as to improve the reproducibility of the InP/Si growths when grading layers were not used.

At the point in time when the above experiment was performed, there was no data to suggest that the P/N cell had more end-of-life (EOL) power output than the N/P cell at extremely high fluences (some proton irradiation data, mentioned later in this report, was measured after the end of this program at NRL by Walters). The N/P InP/Si cell, on its first "try," had clearly better BOL performance than the well-developed P/N cell, and we concluded that it would be better to include a tunnel junction and use proven, high-performance N-P InP cell designs rather than attempt to further understand and develop the P/N design. In the next section, we give a more detailed chronological summary of the experiments that generated the data that supported this decision.

4 SUMMARY OF SPIRE InP CELL EXPERIMENTAL LOTS

In this section, we summarize the purpose, results, and conclusions from all Phase II program InP cell lots. In addition, the final Phase I results are summarized, as well as results from three InP cell lots performed under other programs, but of direct interest to this program. All of the efficiency data discussed in this final report was taken at Spire and is one-sun, 25°C air mass zero (AM0) data, unless otherwise noted. We particularly note InP/Si cell testing performed at NASA-Lewis courtesy of Dave Brinker, since the NASA tests are considered the "official" tests for space cells.

Spire identifies cells with *a process lot number*, by which details of the cell processing can be traced (*e.g.* contacts, cell size, AR coatings), *an MOCVD growth run number*, by which details of the epilayers (*e.g.* doping, thickness) and substrate can be traced, a wafer ID number (which is redundant if a one-wafer MOCVD reactor was used to grow the material, but necessary if multiple wafers were grown in the same MOCVD run), and the cell ID number on the wafer. As an example, 5789-3262-35 refers to process lot 5789, which contains several wafers, one of which was grown during single-wafer MOCVD run 3262, with 35 identifying a particular cell on that wafer.

Lot 5685 - (Sept. 1993) Phase I P/N InP/Si cells

Purpose: Compare P/N InP/Si cells with $In_XGa_{1-X}P$ grading layers against simple buffer layers.

Results: Data are given in Table 3. All cells used 2000Å grown emitters. The two reactor process used (grow GaAs on Si in a low-oxygen reactor, then grow cell in second, higher-oxygen, phosphorous reactor) resulted in bowed "potato chip" wafers.

Table 3 *Comparison of p/n InP/Si cell with an InGaP grade versus a simple InP buffer.*

Ph I 1x1cm InP/Si cell Buffer/Grade	Avg. V_{OC} mV	Avg. J_{SC} mA/cm^2	Avg. FF %	Avg. Eff. %
8μ InGaP grade, 2μ GaAs/Si (best 8.2%)	710	24.4	65	7.4
8μ InP Buffer , 2μ GaAs/Si (best 7.9%)	700	22.6	69	7.3

Conclusions: InGaP grading did not reduce dislocation density better than an InP buffer layer.

Lots 5714 and 5715 - (Nov. 1993) NASA/BMDO Phase I P/N InP Cells on Ge

Purpose: Examine whether P/N InP/Ge cells, with a 4% mismatch between cell and wafer, work significantly better than P/N InP/Si cells with an 8% mismatch.

Results: 600°C P/N InP cells were made on Ge using a process similar to Phase I InP/Si cells. Only difference was the P/N InP cell was grown on GaAs-coated Ge wafers instead of GaAs-coated Si. Best cell data are shown in Table 4.

Table 4 *Effect of InGaP grade and InP buffer thickness on a p/n InP/Ge cell.*

Ph I 1x1cm InP/Ge Buffer/Grade	Avg. V_{OC} mV	Avg. J_{SC} mA/cm^2	Avg. FF %	Avg. Eff. %
8μm $In_XGa_{1-X}P$ on GaAs/Ge (13 cell avg)	742	22.7	64	7.8
8μm InP buffer on GaAs/Ge (8 cell avg)	745	23.2	64	8.1
4μm $In_XGa_{1-X}P$ on GaAs/Ge (6 cell avg)	721	23.6	60	7.4
2μm $In_XGa_{1-X}P$ on GaAs/Ge (22 cell avg)	686	23.4	58	6.5
2μm InP buffer on GaAs/Ge (9 cell avg)	802	24.5	60	8.6

Conclusions: No bow problem exists on Ge, indicating thermal mismatch between the 2 μm thick GaAs buffer and the Si wafer caused the bowing in Ph 1 InP/Si cells. The 8 μm thick data seems to show no significant difference between an $In_XGa_{1-X}P$ grading layer or a simple InP buffer. The 2 μm InP buffer data is puzzling; it seems to show that a 2 μm thick buffer can be as good or better than a cell on an 8 μm buffer.

Lots 5752 and 5753 - (April 1994) InGaP or InAlAs Windows for P/N and N/P InP Cells on InP

Purpose: Examine windows to reduce surface recombination and improve efficiency.

Results: See Table 5 and Figure 4. Since the P/N cell with the InAlAs has a higher Voc even though its Jsc is lower, the dark current has unquestionably been reduced.

Table 5 *Comparison of InAlAs and InGaP windows on p/n InP cell on InP wafers.*

ID, Cell Type, Window (1x1cm cells)	Avg. V_{OC} mV	Avg. J_{SC} mA/cm^2	Avg. FF %	Avg. Eff. %
5752-3035, N/P, No Window (control)	873	30.5	84.7	16.4
5752-3036, N/P, 1.8eV 500Å $In_{0.5}Ga_{0.5}P$	873	29.4	84.7	15.8
5752-3037, N/P, 1.5eV 500Å $In_{0.5}Al_{0.5}As$	874	29.2	85.3	15.9
5753-3042, P/N, No Window (control)	832	28.3	82.3	14.1
5753-3043, P/N, 1.8eV 500Å $In_{0.5}Ga_{0.5}P$	811	24.5	78.0	11.4
5753-3044, P/N, 1.5eV 500Å $In_{0.5}Al_{0.5}As$	863	25.9	82.9	13.5

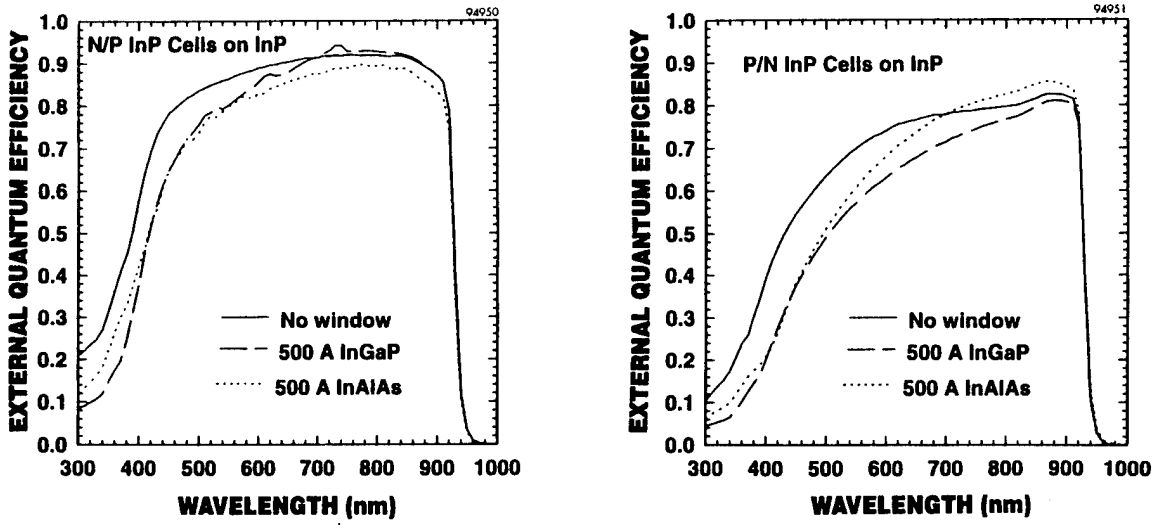

Figure 4 *Quantum efficiency of N/P and P/N InP cells without (control) and with 500Å $In_{0.49}Ga_{0.51}P$ or $In_{0.5}Al_{0.5}As$ windows.*

Conclusions: Although InAlAs passivates P/N InP noticeably, no efficiency increase was seen due to window absorption. Passivation effects are less noticeable in N/P cells with thin 300Å emitters (because less light is absorbed) than in P/N cells with 3000Å emitters.

Lot 5772 - (Aug. 1994) First Phase II P/N 600C InP/Si cells

Purpose: Establish a baseline for P/N InP/Si. Cells were made on 2μ InP buffers, which worked well for InP/Ge (Lot 5714) and are a manufacturable process, unlike grades, which had not worked well and require composition control of many ternary layers. A one-reactor growth was used to cut time and cost in half versus the two-reactor Ph 1 process. To avoid bow due to thermal mismatch between a 2μ GaAs interface and Si seen in Ph I (Lot 5685), we grew InP "directly" on Si with a thin GaAs interface.

Results: Although thin InP buffers worked well for 4% mismatch InP/Ge (Lot 5714), the low Voc's (Table 6) of these 8% mismatch InP/Si cells indicate a thick buffer is needed.

Table 6 *First P/N InP/Si cells grown in Navy Phase II.*

ID, grown InP emitter (1x1cm cells)	Avg. V_{OC} mV	Avg. J_{SC} mA/cm^2	Avg. FF %	Avg. Eff. %
3168, 250Å	555	21	51	4.4
3164, 500Å	535	20	50	4.0
3166, 1000Å	527	19	51	3.7
3171, 2000Å, should be 2/3 Jsc of 500Å	552	16	53	3.3

Conclusions: Thin GaAs interfaces did eliminate bowing. The less-than-expected sensitivity of Jsc to grown emitter layer thickness is our first indication Zn diffusion may dominate junction depth. Thicker InP buffers are needed to increase the Voc's.

Lot 5646 - (Aug. 1993) P/N InP Cells Grown for Radiovoltaic Battery Program

Purpose: Analyze why these P/N InP cells were 17% while our controls were often lower.

Results: See Table 7. SIMS data on a 650C cell showed, surprisingly, less Zn diffusion (and a shallower junction leading to the higher observed Jsc) than in a cell grown at 600°C.

Table 7 *Comparison of best Spire p/n InP cells on InP wafers from various programs.*

Comments (all data P/N InP best cell on InP wafer)	V_{OC} mV	J_{SC} mA/cm^2	FF %	Eff. %
5646-2478-30; 650°C growth; 2μ/hr growth; 0.1μ InGaAs cap	884	33.4	78	16.9
5753-3042-10; 650°C growth; 1μ/hr growth; 0.1μ InGaAs cap	834	29.4	82	14.7
5789-3262-35; 600°C growth; 1μ/hr growth; 0.1μ InGaAs cap	835	25.2	83	12.7

Conclusions: SIMS shows that growth of emitter layers less than ~1000Å are inconsequential, since the depth where the Zn diffusion from InGaAs cap equals N-type base doping is generally >1000Å for most conditions.

Lot 5789 - (Oct. 1994) Evaluate the Baseline Efficiency of P/N and N/P InP Cells on InP

Purpose: Deliver small (5 mm by 5 mm) InP cells to NRL for radiation experiments.

Results: 19% N/P cells and 14% P/N cells were made (best cell data in Table 8 below).

Table 8 *Effect of growth temperature and InGaAs cap thickness on InP on InP cells.*

Best Cell	Type	Temp C	Cap Å	Emit. Å	V_{OC} mV	J_{SC} mA/cm^2	FF %	Eff. %
3229-35	P/N	600	3000	500	846	21.7	85	11.3
3231-12	P/N	600	3000	250	848	21.8	86	11.6
3261-27	P/N	650	1000	250	808	27.8	83	13.7
3262-35	P/N	600	1000	250	835	25.2	83	12.7
3235-5	N/P	600	3000	250	877	35.5	86	19.6
3260-5	N/P	600	3000	400	880	35.3	84	19.1

Conclusions: 650°C growth was again better for P/N cells, which is counterintuitive, since more Zn diffusion and a deeper junction (less Jsc) should occur at higher temperature. SIMS also shows less diffusion at 650 vs. 600°C. We guess that either the Zn re-evaporates at the higher temperature so that less incorporates during growth, or that the 650°C material may have fewer defects than the 600°C material and therefore less diffusion.

Lot 5796 - (Nov. 1994) P/N InP/Si Cell Area Scale-Up and Buffer Experiments

Purpose: Try various buffers and grades to fix Lot 5772 problems, including dual temperature growth (DTG) InP and InGaAs buffers. Scale up to 2 x 4 cm^2.

Results: P/N cell efficiency low (Table 9) since these cells were grown at 600°C.

Table 9 *First 2 cm by 4 cm p/n InP/Si cells.*

2x4 cm cell ID, buffer description all layers grown at 600°C on thin GaAs/Si except as noted	Avg. V_{OC} mV	Avg. J_{SC} mA/cm^2	Avg. FF %	Avg. Eff. %
3287, 3μ 675/600 DTG InP, 1μ InP	633	26.2	48	5.8
3289, 2μ InP, 3μ 675 InP, 1μ InP	487	25.3	49	4.4
3290, 2μ InP, 3μ InGaAs, 4μ 675/600 DTG InGaAs, 1μ InP	580	26.3	40	4.4
3292, 2μ InP, 3μ 675 InP, 1μ InP, on thick 2μ GaAs/Si	712	25.6	51	6.8

Conclusions: Cell scale up no problem. Better efficiency than 5772, but still below expectations. Cells with thicker GaAs (despite bow) definitely look better in performance here.

Lot 5802 - (Nov. 1994) Optimize P/N InP Cell on InP Wafer Baseline Efficiency

Purpose: SIMS data of previous P/N cells shows emitter junction depth, a crucial parameter that controls Jsc, is not determined by the thickness of the epitaxial emitter layer grown, but rather is controlled by Zn diffusing into cell from the InGaAs contact cap layer. In this experiment, we vary the InGaAs cap thickness and growth temperature to attempt to optimize the Zn diffusion to give the best Jsc.

Results: P/N InP cell Jsc improved from 27 to 30 mA/cm^2 (Table 10). Efficiency improved to over 15% at 675°C. 675°C InP growth is more difficult due to indium re-evaporation than at lower temperatures.

Table 10 *Effect of InGaAs cap thickness and 650 vs. 675 °C growth on p/n InP cells on InP.*

Comments (5x5 mm P/N InP best cell on InP wafer)	V_{OC} mV	J_{SC} mA/cm^2	FF %	Eff. %
3312-7; 1000Å InGaAs cap; 650°C growth (avg. eff. 15.1%)	837	29.9	84	15.4
3313-15; 4000Å InGaAs cap; 650°C growth (avg. eff. 13.7%)	841	28.0	85	14.5
3314-2; 3000Å InGaAs cap; 675°C growth (avg. eff. 14.8%)	826	30.5	83	15.3

Conclusions: Junction depth of P/N cells can be controlled through InGaAs cap thickness, which acts as a solid state diffusion source for the zinc P-dopant. Cells made at 675°C gives best Jsc, in line with trend (*i.e.* 675°C cells give better Jsc than 650°C cells which give better Jsc than 600°C cells).

Lot 5803 - (Dec. 1994) Comparison of Optimized P/N vs. (First Try at) N/P InP/Si Cells

Purpose: N/P cells have high efficiency but need a tunnel junction (TJ). P/N efficiency is lower, but need no TJ. Which works best? A 5 μm InP buffer was used in both.

Results: N/P InP/Si cells had 10.6% average efficiency versus 9.7% for P/N cells (Table 11).

Table 11 *Comparison of p/n and n/p InP/Si cells.*

ID, cell temp., type, comments (1x1cm cells)	Avg. V_{OC} mV	Avg. J_{SC} mA/cm^2	Avg. FF %	Avg. (Best) Eff %
3318, 600°C N/P, thin GaAs/Si, TJ under 600°C buffer	703	29.5	70	10.6 (11.1)
3324, 650°C P/N, 3 μm GaAs/Si, 0.1 μm cap, 675°C buffer	729	24.7	73	9.5 (9.7)
3327, 650°C P/N, thin GaAs/Si, 0.3 μm cap, 675°C buffer	721	28.5	65	9.7 (9.9)

Conclusions: Good FF for N/P shows TJ worked. First-try N/P worked better than optimized P/N. Thin GaAs worked as well as thick GaAs, in contrast to Lot 5796.

Lot 5819 - (Jan. 1995) P/N vs N/P InP/Si DTG Cells

Purpose: 1) See if tunnel junction (TJ) works best if grown above or below buffer. 2) Confirm lot 5803 data that shows N/P cells better than P/N. 3) Examine thick versus thin-GaAs interface, reconciling lot 5796 (thick better) and 5803 (thin better) data.

Results: DTG improved N/P cell over simple buffer (lot 5803) by ~1% AM0 (Table 12).

Table 12 *Comparison of p/n and n/p InP/Si cells using improved DTG buffers.*

ID, cell temp., type, comments (1x1cm cells)	Avg. V_{OC} mV	Avg. J_{SC} mA/cm^2	Avg. FF %	Avg. Eff. %
3373, 600°C N/P, TJ atop 6μ 675/600 DTG, thin GaAs/Si	738	29.3	73	11.5
3376, 600°C N/P, TJ atop 6μ 675/600 DTG, thin GaAs/Si	736	28.9	72	11.2
3382, 600°C N/P, TJ atop 6μ 675/600 DTG, thick GaAs/Si	751	29.2	74	11.8
3371, 600°C N/P, 5μ 675/600 DTG on TJ, thin GaAs/Si	719	28.7	73	10.9
3374, 600°C N/P, 5μ 675/600 DTG on TJ, thin GaAs/Si	721	28.4	72	10.8
3378, 650°C P/N, 600Å emit, 6μ 675/600 DTG, thin GaAs/Si	691	25.1	58	7.4
3380, 650°C P/N, 0Å emit, 6μ 675/600 DTG, thin GaAs/Si	714	26.5	63	8.7

Conclusions: N/P cells again have higher efficiency than P/N. It seems better to have TJ on top of buffer (by ~0.5%). Cells on thick GaAs/Si may be better by ~0.5% AM0.

Lot 5827 - (Jan. 1995) Improved 2cm by 2cm N/P InP/Si Cells (NASA 60151 cell delivery)

Purpose: We optimized best N/P cell from 5819 and again compared grades and DTG layers.

Results: See Table 13. Best cell (3427-2) was 12.6% (761 mV, 31.8 mA/cm^2, 71%, NASA).

Table 13 *NASA-Lewis one-sun AM0 28°C data of Spire 2 x 2 cm n/p InP cells on 16 mil Si.*

ID, comments (2x2cm cells)	Avg. V_{OC} mV	Avg. J_{SC} mA/cm^2	Avg. Fill %	Avg. Eff %
3427 5 μm InP DTG Buffer	753	31.5	71.4	12.4
3428 5 μm InP DTG Buffer	756	31.5	71.0	12.4
3429 7 μm InGaAs Grade Expt	484	27.7	58.2	5.7
3430 5 μm InP DTG Buffer	757	31.0	71.2	12.2
3431 7 μm InGaP Grade Expt	722	29.3	65.3	10.1

Conclusions: Simple DTG buffers again work better than either InGaAs or InGaP grading layer.

Lot 5832 - (Feb. 1995) Optimize InP Growth Temperature and Emitter for N/P InP Cells on InP

Purpose: We wanted to examine performance of 650°C N/P InP cells. In previous work (Lots 5646 and 5789), Spire P/N InP cells grown at 650°C worked markedly better than P/N cell at 600°C. Most of this improvement was attributed to less zinc diffusion. However, it was possible some of the benefit was due to other factors, such as InP grown at 650°C InP having less defects and higher mobility than InP grown at 600°C InP. We also made some N/P cells with ~50% thinner emitters to see if Jsc can be profitably increased.

Results: 650°C cells were not better (Table 14) than 600°C N/P cells, unlike the P/N case.

Table 14 *Optimization experiment for n/p InP cells on InP wafers.*

ID, cell temp., comments (1x1cm cells)	Avg. V_{OC} mV	Avg. J_{SC} mA/cm^2	Avg. FF %	Avg. Eff. %
3425, N/P 650°C, 2μm/hr growth, 90s emitter (best 18.0%)	877	33.0	81	17.2
3424, N/P 600°C, 2μm/hr growth, 90s emitter (best 18.5%)	881	34.0	85	18.5
3451, N/P 600°C, 2μm/hr growth, 60s emitter (best 18.6%)	873	34.6	84	18.5
3414, N/P 600°C, 1μm/hr growth, 114s emitter (best 19.5%)	879	35.0	85	19.0
3417, N/P 650°C, 1μm/hr growth, 114s emitter (best 18.1%)	862	33.6	84	17.8

Conclusions: 600°C N/P cells are better than at 650°C by ~0.5%. Slower growth rates may increase efficiency by ~0.5%. A thinner emitter did not improve the cell efficiency overall.

Lots 5854 and 5855 - (April 1995) Optimization of DTG Buffers using 2x4cm N/P InP/Si Cells

Purpose: This lot examined the effects of buffer layer thickness on N/P InP/Si cell performance. Simple buffers (6, 4, and 2 μm thick), and DTG buffers using various cycle combinations were examined. Nominally, all upper cell layers are the same; the only difference between cells is the buffer layer used. All tunnel junctions were above the dislocation reduction grades or buffers.

Results: See Table 15 for average data from the 2 x 4cm cells on each wafer. No dramatic effects were seen for most treatments. Very good 2 x 4cm InP/Si cells were made (most in excess of 12%).

Conclusions: Thick InP buffers give ~10% relative higher efficiency (~1 AM0 percentage point) than buffers one-third the thickness. Thin GaAs nucleation layers give ~10% relative higher efficiency (~1% AM0) than 1μm GaAs layers. The best DTG process gives ~3% relative higher efficiency (~0.4% AM0) than a simple buffer.

Table 15 *Effect of various buffers on n/p InP cell on 25 mil Si wafers*

ID	Avg. V_{oc} mV	Avg. J_{sc} mA/cm^2	Avg. Fill %	Avg. η %	Comments
Effect of the thickness of the simple buffer layer on cell performance					
3517	739	31.6	71.2	12.1	6μ simple InP buffer, thin GaAs
3532	728	31.0	70.4	11.6	4μ simple InP buffer, thin GaAs
3524	716 .	30.3	69.3	10.9	2μ simple InP buffer, thin GaAs
Effect of 1μm GaAs interface versus thin GaAs interface					
3517	739	31.6	71.2	12.1	6μ simple InP buffer, thin GaAs
3534	746	30.6	68.0	11.3	6μ simple InP buffer, 1μ GaAs
3525	748	30.4	72.3	12.0	5.5μ total, 5 cycle 675/600 0.5μ DTG, thin GaAs
3539	747	30.6	68.2	11.3	5.5μ total, 5 cycle 675/600 0.5μ DTG, 1μ GaAs
3519	738	31.3	71.1	12.0	4μ total, 2 cycle 675/600 1μ DTG, thin GaAs
3535	662	28.0	64.6	8.7	4μ total, 2 cycle 675/600 1μ DTG, 1μ GaAs
Effect of increasing the number of DTG cycles while keeping total buffer layer thickness roughly constant					
3533	747 **753**	31.7 **31.2**	72.2 **72.8**	12.5 **12.5**	5.5μ total, 2 cycle 675/600 1.5μ DTG, thin GaAs **Bold data is NASA-Lewis Test Data for Cell**
3521	748	31.3	72.3	12.3	6μ total, 3 cycle 675/600 1.0μ DTG, thin GaAs
3525	748	30.4	72.3	12.0	5.5μ total, 5 cycle 675/600 0.5μ DTG, thin GaAs

5 DISCUSSION OF WAFER BOW AND STARTING DISLOCATION DENSITY

Heteroepitaxial growth of InP/Si involves a large, abrupt 8% change in lattice constant between the Si wafer (5.43Å) and the InP cell layers (5.87Å). In addition, a difference in thermal expansion coefficients exists between Si and InP (2.5×10^{-6} vs. 4.5×10^{-6} $\Delta L/L/C$ at 300K). Both of these differences create stress in the crystal. Lattice defects (dislocations) are generated in the epilayers to relieve this stress.

The 8% lattice-mismatch would "like to" mechanically bend the wafer edges down (convex, or bow up) since the lattice constant of the InP is higher. However, this effect does not occur since at the growth temperature (~600°C) the InP film almost completely relaxes by dislocation generation.

As the material is cooled from the growth temperature, the thermal expansion mismatch mechanically "wants to" bend the wafer so that the edges curl up (concave, or bow down) since the InP contracts faster than the Si (the InP is in tension). This results in additional dislocation generation, but the temperature is now lower and it is not as easy to relax the material.

In this program, we have used 16 and 25 mil [4 degree off to <111>] 3-inch Si (100) wafers without noticeable bowing for ~10 μm InP cell/buffers structures. The Si thickness determines how much the wafer bows (the radius of curvature is proportional to the **square** of the Si thickness "t"). From simple geometry, the bow is proportional to d^2/t^2, where "d" is the wafer diameter. For example, a 12 mil 4-inch Si wafers would have about 3.2X the bow of a 16 mil 3-inch wafer.

We now discuss the starting dislocation density. During the first ~ 10Å of growth, the material is too thin to generate enough strain to form dislocations (*i.e.* growth is pseudomorphic). However, after this, dislocations form at the growth surface and thread back to the Si interface, as well as upwards as growth continues. This dislocation density (~10^{12} cm^{-2}) is proportional to the number of atoms misaligned between substrate and epilayer. For large mismatch (2 to 8%), the density is so large that most dislocations annihilate each other (two dislocations meet and disappear when their stresses cancel) or combine (two dislocations meet and form one defect) within ~ 0.5 μm of the interface, typically lowering the threading dislocation density to ~10^{10} cm^{-2}, ~1% of the original total. This density is approximately independent of the lattice mismatch. For example, a 1 μm GaAs/Si layer (4% mismatch) has about the same dislocation density as 1 μm of InP/Si (8%).

Dislocation densities of 10^{10} are still too high for good cell performance, since dislocations act as minority carrier recombination centers. If one assumes the recombination velocity at the dislocation is infinite, the cell base diffusion length is the average spacing between dislocations. For example, a 10^{10} cm^{-2} dislocation density gives a 0.1 μm average spacing between dislocation lines (*i.e.* a 0.1 μm diffusion length according to our model), leading to low cell Jsc and Voc.

Empirically, InP is best grown on Si using a GaAs interface layer. If InP is directly grown on Si, a very high V/III ratio of gases are needed and a large amount of pyrophoric phosphorous is left coated on the belljar, susceptor and baseplate of the MOCVD reactor after growth. InP grows on GaAs wafers easily, and the idea of using a GaAs-coated Si wafer is a natural one. One question investigated in the program was whether growth of low-defect-density GaAs buffers was needed. Low-defect-density GaAs on Si wafers, used in Phase 1 cells, are normally grown by thermal cycling, which is time-consuming (4 to 5 hours) and expensive. In Phase I, we used two different reactors, one to grow low-defect GaAs/Si wafers in a phosphorous-free environment (eliminating some oxygen problems which made the growth on a Si wafer at high temperatures easier), and a second reactor to grow the InP-based cell on the GaAs/Si wafer. Since we wished to grow InP on top of the GaAs/Si, which introduces yet another InP/GaAs 4% lattice-mismatch (totaling 8% with the 4% GaAs/Si mismatch), lowering the defects to ~10^8 cm^{-2} in the GaAs seemed meaningless if we were to later introduce over 10X that number (>10^9 cm^{-2}) during InP growth on the GaAs/Si.

Since low defect density GaAs did not seem necessary, we pursued a process using an amorphous, very thin, GaAs layer that enabled us to use a single reactor to both nucleate the growth on the Si wafer and grow the InP cell. This process is twice as fast, and therefore less expensive, and more reproducible than the Phase I process. Our best InP/Si cells were eventually made using these thin GaAs wafers. This process has been referred to as "thin" GaAs/Si, or occasionally as "direct" growth of InP on Si, even though the very thin GaAs interface layer is still present. This process is discussed in more detail in a later section. Next, we discuss defect-reduction buffer layers and grading layers employed to further lower the dislocation density to the 10^7 to 10^8 cm^{-2} level.

6 DISCUSSION OF SIMPLE BUFFER LAYERS

Thicker buffer epilayers result in lower threading dislocation density than thin buffers. The main threading-dislocation-reduction effect is the annihilation of dislocations when they meet one another. The decrease in dislocation density is not linear with thickness because these annihilation and combination mechanisms are more effective with higher dislocation density. For example, a 4 μm buffer will not result in half the threading dislocation density of a 2 μm buffer.

Actual dislocation densities approximately follow "1/x"-type curves when the dislocation density is plotted versus buffer thickness. At first, a sharp reduction in dislocation density versus thickness is seen for relatively thin buffers, where the dislocation density is high and the chances of an interaction between dislocations is greater. For thicker buffers, the average spacing between dislocations increases and only a gradual decrease in dislocation density is seen with increasing thickness, since dislocation interactions are less likely. This 1/x relation holds over reasonable MOCVD buffer layer thicknesses. Simple buffers can result in a dislocation density of ~10^8 cm^{-2} for an InP/Si cell structure. However a goal of lower than 10^7 cm^{-2} is desired (Figure 5), although very difficult to achieve, for mismatches above 1%. Therefore, more elaborate steps, discussed in the following sections, were pursued.

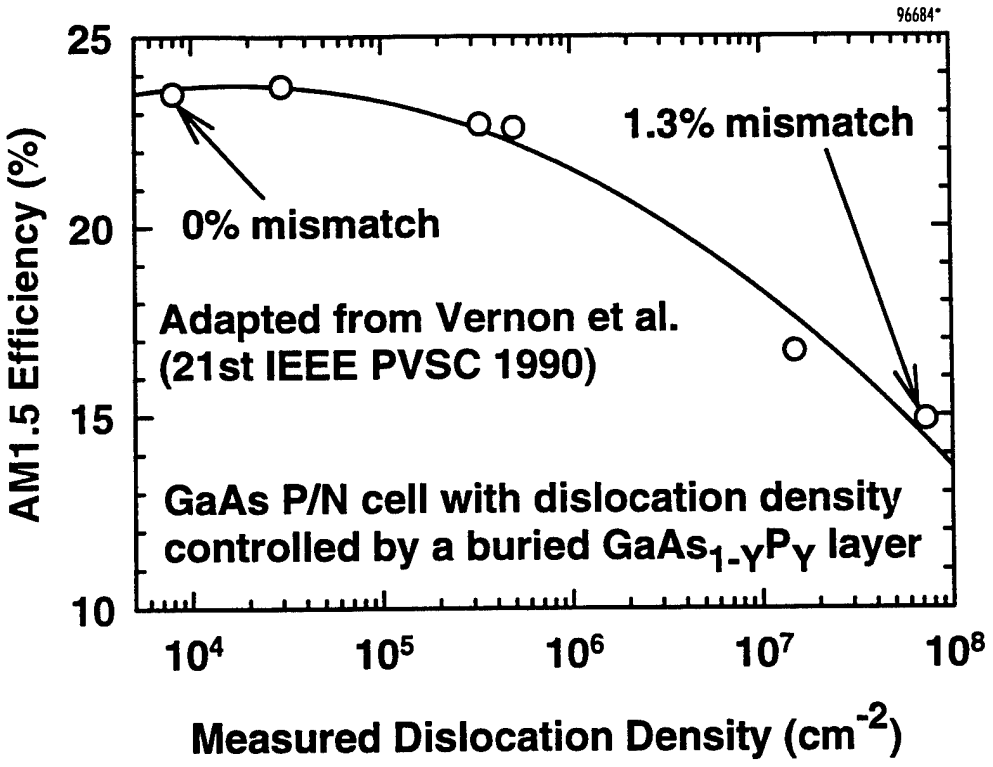

Figure 5 *P/N GaAs cell terrestrial efficiency versus dislocation density. Several GaAs cells were made, each with a buried lattice-mismatched GaAsP alloy layer of a different composition,[12] to introduce a different lattice mismatch and dislocation density into each cell. Dislocation densities were measured by cross-section TEM and EBIC. Data shows little degradation out to a defect level of 10^6 cm^{-2} and then a sharp drop.*

7 DISCUSSION OF GRADING LAYERS

Grading layers or "grades" are a series of layers between substrate and cell epilayers with lattice constants monotonically varying between those of the substrate and cell layers. Grades should be more effective than simple buffers in reducing dislocations in favorable cases, when the strain at the interface between successive grading layers can bend threading dislocations into misfit dislocations, allowing a lower dislocation density in the upper cell layers.

Thinner grades (~5 to 10 μm) can be used under compression than in tension because higher strains can be incorporated without cracking the compressed layers. A step grade is normally used for practical reasons (e.g. flow controllers are digitized to a minimum sccm gas flow, so that "linear" grades are approximated by a large number of steps). The composition (or grading rate) and thickness of each step layer are interdependent in the grade design since each affects the stress generated at the interface and therefore the density of propagating threading dislocations.

Previous to this program, Spire made 9.9% AM0 efficient, 8% mismatch, N/P InP/Si cells using an $In_XGa_{1-X}As$ grade which ramped down in temperature, ending at 600°C. Also, NREL had made 13.7% AM0 total-area efficiency (with a prismatic coverglass), 4% mismatch, N/P InP/GaAs cells using a 650°C $In_XGa_{1-X}As$ grade. The NREL cells had a dislocation density of ~10^7 cm^{-2}, about the best ever reported for a heteroepitaxial cell. According to our simple model, the average dislocation spacing (and diffusion length) for these 13.7% InP/GaAs cells was ~3 μm.

In Phase I, Spire investigated an $In_XGa_{1-X}P$ grade instead of $In_XGa_{1-X}As$, since we believed an $In_XGa_{1-X}P$ grade may be better than an $In_XGa_{1-X}As$ grade for two reasons. First, an $In_XGa_{1-X}As$ grade must end exactly at the lattice-matched $In_{0.53}Ga_{0.47}As$ composition or a new set of dislocations will be generated directly underneath the cell layers. With an $In_XGa_{1-X}P$ grade, the grade starts as $In_{0.49}Ga_{0.51}P$ lattice matched to GaAs, but the grade ends as InP, so that there is no chance at all of generating a new set of dislocations directly under the InP cell layers. If the starting composition is not exactly $In_{0.49}Ga_{0.51}P$, the dislocations generated would be no greater than the number already existing in the GaAs layer at that point from the 4% GaAs/Si mismatch, and the full thickness of the dislocation reducing grade would be above this layer.

Secondly, the $In_XGa_{1-X}P$ was expected to be better thermal-expansion-matched to InP, so that there may be fewer thermal mismatch dislocations as well, although this was of secondary concern since this number was not expected to be large compared to the number of dislocations generated by lattice-mismatch.

In Phase I, Spire made 8.2% efficient, P/N InP/Si cells using a 600°C $In_XGa_{1-X}P$ grade. The performance was not as high as expected. Some of the problem was the use of a P/N InP cell instead of the N/P InP cell, which we have discussed previously. However, it was also clear that the grading layer did not work as well as hoped; in fact, it seemed to be not any better than a simple InP buffer of the same thickness.

Although $In_XGa_{1-X}P$ grades were used in Phase I, in Phase II we realized $In_XGa_{1-X}P$ had a serious disadvantage compared to $In_XGa_{1-X}As$.

The relative hardness of the alloys making up the grade affect the dislocation reduction performance. Material hardness is a measure of yield strength, the strain at which the material deforms. The microscopic mechanism for deformation is the generation or movement of dislocations. If two materials of different hardness are strained against each other, such as $In_{0.5}Ga_{0.5}P$ and $In_{0.6}Ga_{0.4}P$, in two successive layers of the $In_X Ga_{1-X} P$ grade, the dislocations will tend to lie in the softer material, in this case the upper $In_{0.6}Ga_{0.4}P$ layer, making it difficult to stop threading dislocations from propagating upward since each successive layer has more indium and is softer.

In contrast, $In_XGa_{1-X}As$, up to about the 40% composition ($x<0.4$), is harder than either GaAs or a lesser indium composition $In_XGa_{1-X}As$ layer, so that dislocations cannot propagate as easily into each harder, successive, upper layer of the grade that is nearer to the cell layers. It seems odd that by adding more of a soft metal, indium, you can make an InGaAs harder; however, this is a well-known phenomena (*e.g.* tin, a soft metal, added to copper makes bronze, which is harder than both).

Empirically, low composition (< 30%) $In_XGa_{1-X}As$ grades are well behaved and give low defect densities even with 10% indium steps (0.8% strain steps). However, such grades ending at $In_XGa_{1-X}As$ compositions above 40% are defective, due to the higher composition $In_XGa_{1-X}As$ layers once again becoming softer than the layers underneath. As an example of this latter case, Spire $In_{0.72}Ga_{0.28}As$ thermophotovoltaic cells on InP wafers, which work very well despite a 1.8% mismatch, have $In_XGa_{1-X}As$ grades with twelve 0.15% steps over 4 μm, beginning at $In_{0.53}Ga_{0.47}As$ and ending at $In_{0.72}Ga_{0.28}As$. The same 0.15% grading rate was used in the NREL InP cell on GaAs wafers (4% mismatch) using an $In_XGa_{1-X}As$ 8 μm grade, which had a dislocation density of 10^7 cm^{-2}.

Also, after examining TEM cross-sections of the Spire and NREL $In_XGa_{1-X}As$ grades, we became convinced it was important to use the highest growth temperature possible to allow the dislocations to move easily in response to stresses in the material for either dislocation reducing grades *or buffer* layers. TEM cross-sections revealed that the Spire $In_XGa_{1-X}As$ grade had substantially more dislocations at its final 600°C steps than in the preceding higher temperature steps or than in the NREL 650°C $In_XGa_{1-X}As$ grade.

To summarize, we believe some "rules-of-thumb" for designing $In_XGa_{1-X}As$ grades are:

- use a high growth temperature (*e.g.* 650°C) to allow dislocations to move easily.
- use small grade steps (*e.g.* a 0.15% change in lattice constant per step from GaAs up to the final $In_{0.53}Ga_{0.47}As$) to: a) allow higher temperature growth of the grading layer, and b) so the final, softer, higher steps at the higher indium composition end of the grade, where the material again becomes softer compared to the step layer underneath, can retain two-dimensional growth and avoid tangling of dislocations that may occur if the step-to-step mismatch is too great.
- make sure the material in each successive grade step is harder than in the previous step since the dislocations tend to remain in the softer material (this should not be a problem for $In_XGa_{1-X}As$ grades up to $x \sim 0.4$).

However, in Phase II, we did not pursue $In_XGa_{1-X}As$ grades, since we were not able to grow good material on Si wafers with either an $In_XGa_{1-X}P$ (as in Phase 1) or an $In_XGa_{1-X}As$ grade (early in Phase II). Test runs had poor surfaces (hazy and not specular or shiny) with broad X-ray diffractometry peaks. We were able to grow good test structures with $In_XGa_{1-X}As$ on GaAs wafers, and, in unrelated work in the same time period, we grew very good $In_XGa_{1-X}As$ grades on InP wafers for 2% mismatch $In_{0.72}Ga_{0.28}As$ thermophotovoltaic cells, as well as good InP/Si wafers without $In_XGa_{1-X}As$ grades. The problem was confined to the case of a thick $In_XGa_{1-X}As$ layer on a Si wafer.

One common observation in cells with $In_XGa_{1-X}As$ grading layers that reduced the defect density significantly is that two-dimensional growth is necessary for effective compositional grading with reduced defect density; i.e. the surface the grading layer growth begins on should be specular (shiny). Unfortunately, the starting surface for the grades after a couple of microns of GaAs were grown on a Si wafer were hazy for the GaAs/Si wafers grown in this program. We now outline a qualitative theory that explains why a specular surface may be a necessary condition for a grading layer to be effective, proposed by Peter Colter of Spire.

When the $In_XGa_{1-X}As$ grade is not two-dimensional growth due to deposition of the grade on a poor (*i.e.* hazy) starting surface or due to selection of wrong grading parameters (*e.g.* large grade steps, low deposition temperature, too high a growth rate, *etc.*), the tilt of the epilayer varies with the local surface morphology and thus the epilayer is broken up into a mosaic of differently tilted areas, with relatively high densities of defects between them (Figure 6).

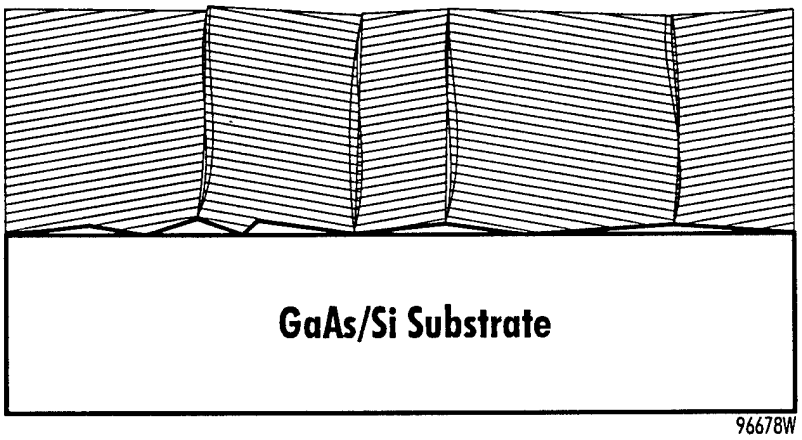

Figure 6 *Sketch of a "hazy" starting surface typical for our thicker GaAs interfaces grown on Si wafers. The GaAs/Si surface is irregular, leading to the $In_XGa_{1-X}As$ grading layer growing as a mosaic of terraces, each with a different tilt. The dislocations glide to the edge of the terraces, become tangled, and are then pinned, preventing them from gliding to the edge of the wafer.*

In this case, instead of the grade producing dislocations that will bend under the compressive stress and propagate parallel to the deposition plane until they terminate at the sidewalls of the crystal, these dislocations are pinned by the mosaic (planar defect) causing them to multiply and deflect upwards toward the cell epilayers. The surfaces of observed $In_XGa_{1-X}As$ graded layers on Si wafers appear to consist of a mosaic of terraces, which seems consistent with this interpretation.

If this interpretation is correct, it is unlikely that the performance of the InP/Si could be significantly improved by grading, since it was difficult for us to grow thick GaAs films on Si wafers reproducibly without haze. Therefore, another technique was tried, the dual temperature growth buffers to be discussed next.

8 DISCUSSION OF DIRECT INP/SI DEPOSITION AND DUAL TEMPERATURE GROWTH BUFFERS

The deposition of InP on Si by use of a thin GaAs nucleation layer and dual temperature growth (DTG) buffers is a novel, simple, reproducible, manufacturable, dislocation reduction process originated by Nasser Karam of Spire and implemented for the first time in this Navy Phase II. InP/Si cells with DTG buffers performed best of all the techniques tried during this program.

The growth of large volume, high quality InP on Si by MOCVD requires a manufacturable process that is reliable, robust and low cost. Therefore, the InP-based cell should be deposited on Si in a single MOCVD run that consists of a nucleation layer, InP buffer, and defect reduction layer followed by the cell structure. Figure 7 shows a generic sequence of the deposition process.

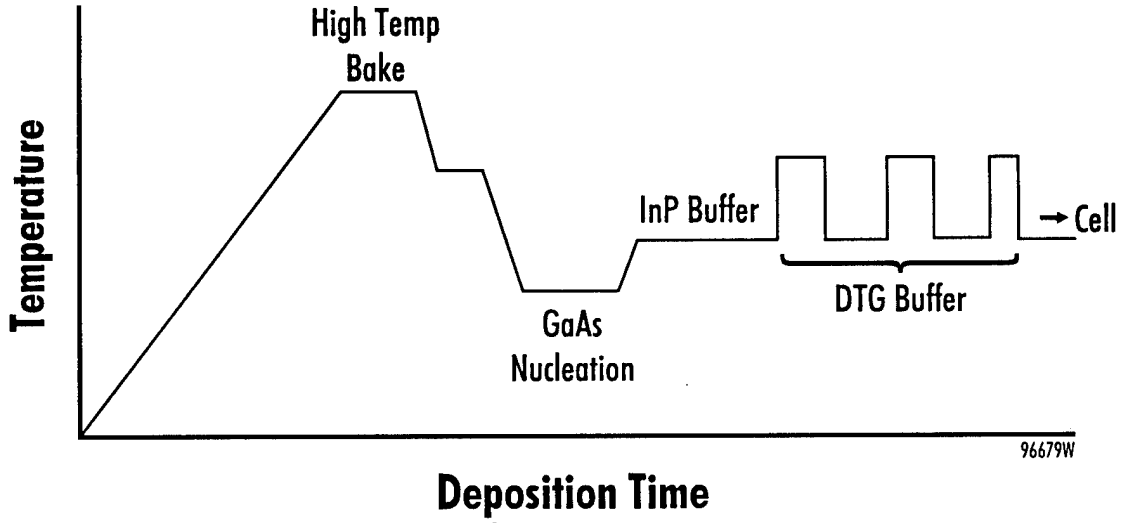

Figure 7 *Qualitative time versus growth temperature sequence for an InP/Si cell. Initial heatup to a high temperature removes oxide from Si surface; this is followed by a proprietary low-temperature thin GaAs nucleation layer followed by a heatup to a standard InP growth temperature (e.g. 600•C) to grow a buffer, followed by a thermal cycled growth of the dual-temperature growth buffer.*

The process starts with a high temperature bakeout of the Si substrate in hydrogen to remove the native oxide, followed by a surface passivation step using AsH_3, which insures the removal of the SiO_2 by reacting it with the atomic hydrogen liberated from the cracked AsH_3, covering the surface with As-Si bonds. Arsenic protects the virgin surface from reacting with impurities (*e.g.* C, O) and forms a monolayer. A thin GaAs initial "nucleation" film (a few nanometers thick) is subsequently deposited at low temperature to bridge the mismatch between InP and Si. This amorphous initial layer has to be thick enough to form a continuous film with minimum pin holes, yet thin enough to crystallize into a single crystal when the temperature of the substrate is raised to the conventional deposition temperature for InP. A buffer layer of InP, is subsequently deposited to serve as a foundation for the defect reduction film and the cell structure. At the surface of a 1 μm thick buffer, the dislocation density is believed to be in the mid 10^9 cm^{-2} range, as discussed in an earlier section. To further reduce this dislocation density, a new technique was employed.

The dual-temperature growth (DTG) defect reduction technique is a simple process that relies on the difference in the magnitude of strain resulting from the growth of two adjacent layers at different deposition temperatures. This built-in strain results in a force at the interface of the adjacent layers that can be used to bend the dislocations originating at the InP/Si interface parallel to the DTG layers and driving them out of the crystal away from the device. The force sign and magnitude are in general determined by the difference in the deposition temperature of the two adjacent layers, the layer thicknesses, the thermal expansion coefficient difference, and the lattice constant. However, although the latter two properties affect the strain, it is not necessary that the layers have a different thermal expansion coefficient or lattice constant to introduce some strain, as is the case for our specific application where the DTG buffer is made solely in InP. The magnitude of the force increases with layer thickness and with greater differences in the growth temperature of the adjacent layers of the DTG buffer.

A simple example is the case of growing two adjacent InP layers at different deposition temperatures. The initial InP film grown of the Si wafer is roughly stress-free at the growth temperature (*e.g.* 1 μm grown at 600°C). The next layer of the DTG buffer is grown, for example, 1μm thick at 675°C. The InP previously grown at 600°C is also heated up to the 675°C; however, this film is now stressed since it was sitting on top of a Si wafer with a different thermal expansion coefficient than InP. The new 675°C InP is now grown stress-free on top of this stressed InP layer (the layer that was grown at 600°C and is stress-free at that temperature). This makes a complete cycle of the DTG buffer. The growth temperature is then again lowered to 600°C to start the next cycle. At this temperature, the original InP grown at 600°C is again unstressed, while the InP grown at 675°C is now stressed. As this process is repeated, a series of InP layers are created which can contain substantial stress. After the DTG and cell growth are completely finished and the cell is cooled to room temperature, an additional, much greater, stress due to the thermal expansion mismatch between the Si and InP epilayers is uniformly distributed in the InP epilayers. However, the differential (non-uniform) stress between the InP layers still exists and it is this differential stress which is responsible for bending the dislocations and for any defect reduction seen when the DTG buffers are compared to simple single-temperature InP buffers.

Several combinations of DTG buffers were tried; cell data from these experiments are detailed in Table 15. Although the process has not been optimized, virtually all cells with a DTG buffer worked better than cells with a simple InP buffer of the same thickness, but the difference was modest (about 0.5 AM0 percentage points). All cells with DTG buffers worked much better (about 2 AM0 percentage points) than cells made with either $In_XGa_{1-X}P$ or $In_X Ga_{1-X}$ As grades (*e.g.* Table 13) whenever direct comparisons were made in this program. Figure 8 shows a diagram illustrating qualitatively how the DTG process reduces defects.

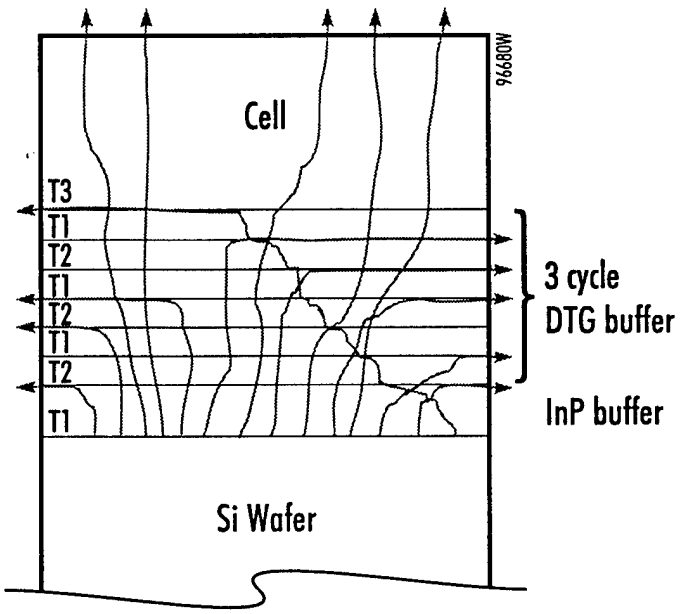

Figure 8 *Qualitative illustration of the DTG buffer bending threading dislocations out of the growth plane.*

9 DIFFUSION LENGTH IN INP/SI

The minority carrier electron base diffusion lengths in InP/Si were studied[13] by means of fitting, by non-linear regression, measured quantum efficiency data with an analytical model and extracting the diffusion length which allows the best fit between model parameters and the data. The quantum efficiency model used, described well by Hovel,[14] breaks up the total quantum efficiency into three components.

The first is from the cell emitter. In an N/P InP cell, the emitter is very thin (300Å) to limit light absorbed in the emitter which is subjected to a high front surface recombination loss (10^7 cm/s). The emitter (hole) diffusion length is in almost all conceivable cases larger than the emitter thickness. Therefore, the model results are virtually independent of emitter diffusion length. Emitter diffusion lengths of 10, 1, 0.1, or 0.05 μm give the same result as far as the quantum efficiency and the AM0 photocurrent are concerned since all of these lengths are in excess of the 300Å emitter thickness. This non-sensitivity of the photocurrent to emitter diffusion length makes the study of the base diffusion length much easier.

The second component that contributes to the quantum efficiency is the NP junction depletion space charge region (SCR). In the NP InP cell the emitter is heavily doped (> 10^{19} cm^{-3}) so that a one-sided step junction approximation is used to calculate the zero-bias SCR width in the base (doping $3x10^{17}$ cm^{-3}), which is about 630Å. To first order, the model assumes that any carriers photogenerated in the SCR are immediately collected and this component does not depend on either base or emitter diffusion lengths.

The third model component is from the base region of the solar cell, and the model is essentially similar to that of the emitter (but of opposite polarity and minority carrier types). The surface recombination velocity at the back of the 3 μm thick cell was taken to be 10^4 cm/s, but the results are very insensitive to this value, since the base diffusion lengths are all less than 1μm and very little is collected from 3 μm away from the junction.

Figure 9 shows the quantum efficiency of a 1x1 cm 12% InP/Si cell before irradiation.

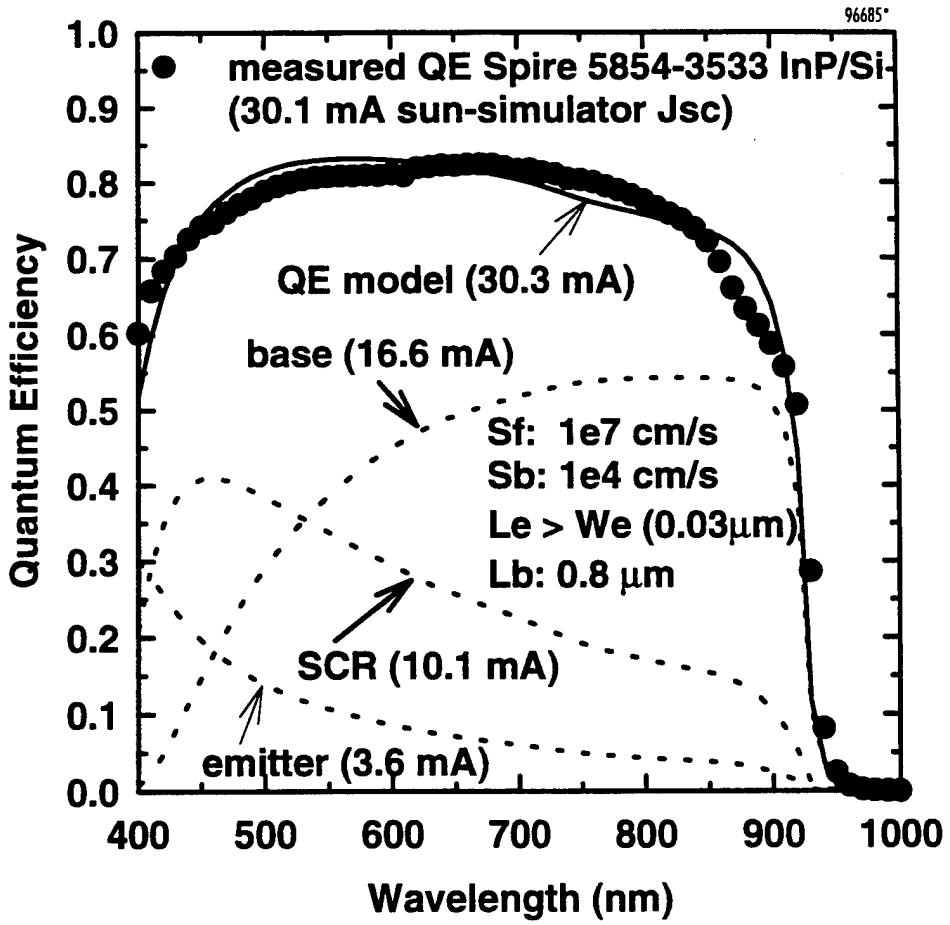

Figure 9 *Measured (black dots) and model (solid line) quantum efficiency before irradiation for a 12% N/P InP/Si cell. Solid line (equivalent to 30.3 mA AM0) is the sum of the three dotted lines, representing contributions from the base (16.6 mA), depletion space-charge region (SCR) (10.1 mA), and the emitter (3.6 mA). An electron base diffusion length of 0.8 μm fit the data.*

The AM0 photocurrent from the measured quantum efficiency and I-V measurements at one-sun on a sun simulator (set with a NASA-calibrated InP reference cell) agreed (30.1 mA). The quantum efficiency data were non-linear least squares fitted to the model using the Marquandt-Levenberg algorithm. The model fit is shown as the uppermost solid line, and when integrated against the AM0 power spectrum, gives a photocurrent of 30.3 mA, in close agreement with the measured data. The base (electron) diffusion length extracted at this point was 0.8 μm. The cell had not yet been irradiated; the diffusion length is lower than in homoepitaxial InP due to dislocation defects from the 8% lattice-mismatch in the heteroepitaxial InP/Si cell.

Using the above quantum efficiency (QE) model, the predicted photocurrent was obtained versus the base diffusion length (Figure 10). This curve is then used to estimate the diffusion length from the measured photocurrent. The key to our experiment is the assumption the emitter diffusion length, when irradiated, is always larger than the 300Å emitter thickness, and that the space charge region is to first-order constant under irradiation. With these assumptions, the base component of the quantum efficiency curve dominates the photocurrent degradation with irradiation (the other components stay relatively constant).

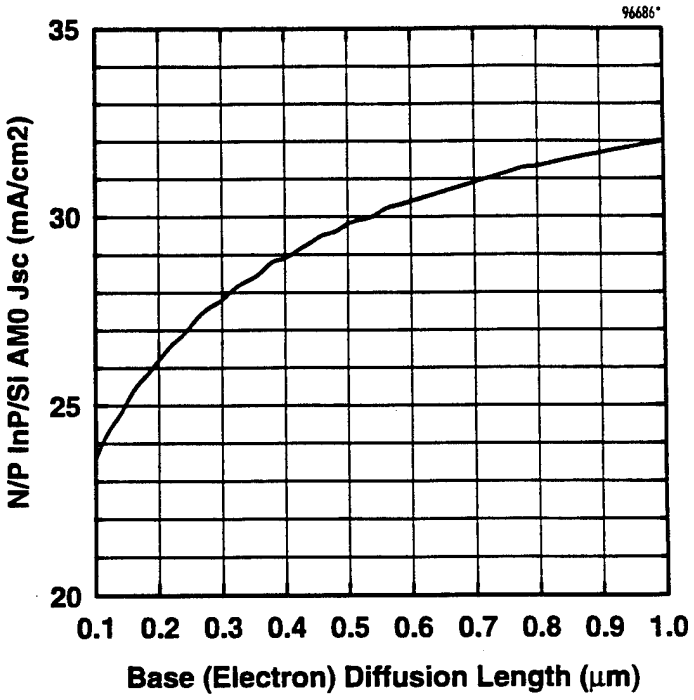

Figure 10 *Model AM0 photocurrent for an N/P InP/Si cell vs. base electron diffusion length.*

The AM0 I-Vs for the 12% AM0 BOL N/P InP/Si cell were measured from no irradiation to an equivalent fluence of 7.7 x 10^{16} 1 MeV electrons/cm^2, where the efficiency was 8%. The cells were irradiated by alpha particles from a 1 mCi Am-241 source. This alpha source is small, self contained, and delivered an equivalent fluence of 7.7 x 10^{16} 1 MeV electrons/cm^2 in only 333 hours. Damage in InP from alphas is accurately converted into 1 MeV electron equivalent fluence using the non-ionizing energy loss (NIEL) method[15,16]. For the source-cell distance used, the 3.9 MeV alpha flux was calculated as 1.03 x 10^6 α/cm^2/s. The calculated equivalent 1 MeV electron flux was 6.45 x 10^{10} electrons/cm^2/s.

Table 16 shows the equivalent 1 MeV fluence, the measured photocurrent, and the base diffusion lengths obtained from Figure 10.

Table 16 *Fluence vs. measured AM0 photocurrent and estimated base diffusion lengths.*

Eqv. 1 MeV Electron Fluence #/cm^2	AM0 Photocurrent mA/cm^2	Base (Electron) Diffusion Length (μm)
0	30.1	0.8
1.2×10^{14}	29.9	0.8
1.4×10^{15}	29.5	0.7
1.7×10^{16}	26.8	0.4
3.8×10^{16}	25.8	0.3
7.7×10^{16}	25.7	0.3

A standard empirical model for diffusion length versus fluence[17] was fit using Table 16 data (Figure 11). The model parameters are the unirradiated electron diffusion length Lo (0.8 μm, Figure 9) and K, the damage coefficient (4×10^{-8}). The fit is good except at the highest fluence; this may be due to radiation damage carrier removal effects changing the width of the space charge region; this effect was not included in our modeling.

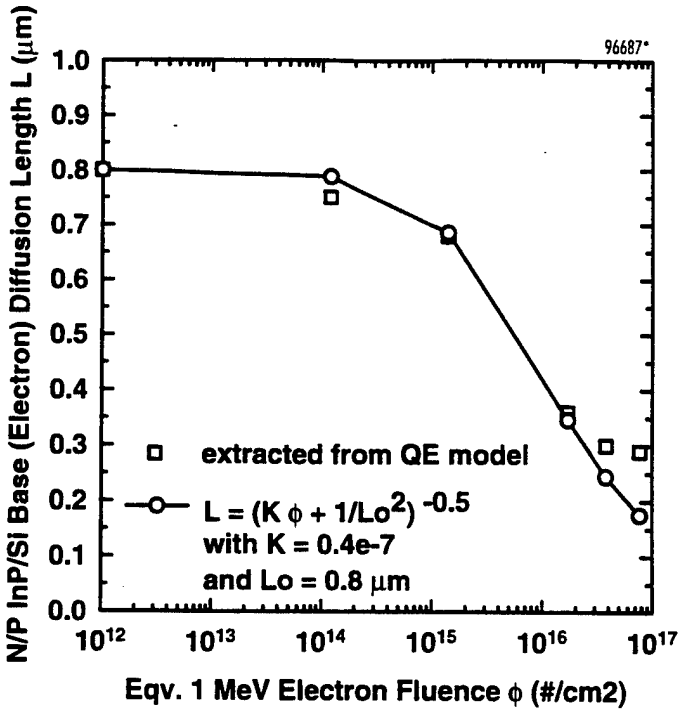

Figure 11 *Estimated base electron diffusion length vs. fluence for an N/P InP/Si cell.*

We could not measure the quantum efficiency after every irradiation due to some scheduling issues. However, to confirm the QE model and the diffusion lengths in Table 15 were still accurate after heavy irradiation, we measured the cell after the irradiations were all completed. The data is shown in Figure 12. The fit still agrees reasonably well with the measured sun-simulator photocurrent, although some discrepancy in form is evident, which, as mentioned previously, may be due to our lack of modeling the carrier removal effect in semiconductors at high irradiation.

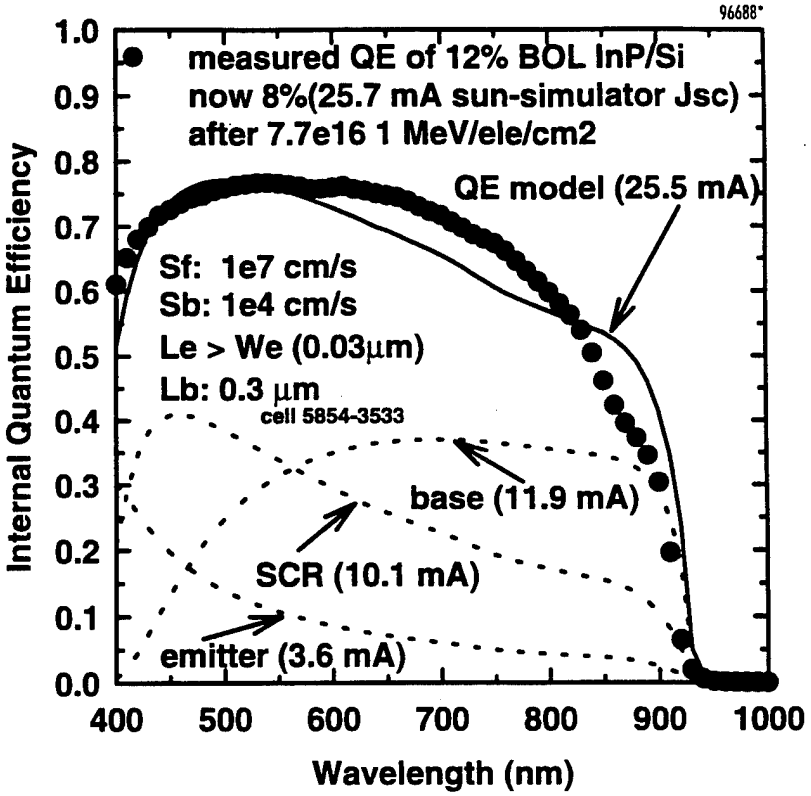

Figure 12 *Measured (black dots) and model (solid line) quantum efficiency after $7.7x10^{16}$ 1 MeV electrons (12% BOL N/P InP/Si cell is now 8%). Solid line (equivalent to 25.5 mA AM0) is the sum of the three dotted lines, representing contributions from the base (11.9 mA), depletion space-charge region (SCR) (10.1 mA), and the emitter (3.6 mA). An electron base diffusion length of 0.3 μm fit the data.*

The three dotted lines show quantum efficiency contributions predicted by the model from the base, emitter, and junction space charge region (SCR), which sum to the solid line. The base contributes the most photocurrent (about 16.6 mA/cm^2 of the 30 mA/cm^2 total), followed by the 650Å SCR (10.1 mA/cm^2) followed by the thin 250Å emitter (3.6 mA/cm^2). The hole diffusion length in the emitter (Le) is assumed to be greater than the 250Å emitter thickness (We). A non-linear regression of the data to the model was used to obtain the best fit for the front surface recombination velocity (Sf) and electron base diffusion length (Lb). The minority carrier electron base diffusion length obtained by the fit is ~0.8 μm. Since the electron mobility is about 20X the hole mobility, we estimate that the minority carrier hole emitter diffusion length is $0.8/(20)^{1/2}$ or ~0.2 μm. Therefore the approximation made in the model (We < Le) is consistent. The model is very insensitive to the back surface field (BSF) interface velocity Sb.

10 TUNNEL JUNCTION AND SERIES RESISTANCE DISCUSSION

In brief, the cell series resistance is believed to be limited by the tunnel junction to a value of about 0.5 Ω-cm^2. However, this value is fairly benign for one-sun cells. If the cell series resistance was eliminated entirely, the voltage at maximum power would be boosted from a 600 mV average to about 615 mV (30 mA/cm^2 x 0.5 Ω-cm^2), or a 12.5% cell would become about 12.8%.

We now discuss the cell tunnel junction in more detail. Use of a N/P cell requires the incorporation of a tunnel junction (see Table 2) since the III-V layer immediately above the Si wafer is autodoped n-type by diffusing Si atoms.

One problem associated with the P-side of the tunnel junction is that a highly-doped, abrupt junction is needed for tunneling, while Zn (the most commonly used P dopant in III-V semiconductors) is a rapid diffuser, resulting in a tendency to grade the junction and lower the maximum doping density.

In the Phase II Spire N/P cells, InGaAs was used for the tunnel junction both because of its lower bandgap and because of the difficulty in doping InP highly p-type (the maximum doping in P InP is ~3 x 10^{18} cm^{-3} while in P InGaAs it is ~3 x 10^{19} cm^{-3}). The junctions used in this program were composed of N$^+$ and P$^+$ InGaAs layers 1μm thick, allowing considerable movement of the pn junction by diffusion without leaving the highly doped layers.

We experimented placing the tunnel junction both above and below the InP dislocation-reducing buffer layer. Underneath this layer, the dislocation density is higher, and, presumably, the resistance may be decreased if dislocations shunt the tunnel junction. The disadvantage is that the tunnel junction doping transition should be very abrupt, and the additional 5μm of InP buffer grown above the tunnel junction would allow the zinc doping to diffuse further than if the tunnel junction were grown on top of the buffer. In practice, we did not see any difference between cells made with the tunnel junction above or below the buffer layer. Both structures produced adequate tunnel junctions for one-sun cells (see Table 12).

Results of a theoretical[18] calculation (Figure 13) show the estimated tunnel junction (TJ) resistance. Cells from Lot 5855 (Table 15) had a total series resistance (as determined from Voc-Isc versus V-I curve) ranging from ~0.1 to 1 Ω-cm^2. The P and N InGaAs doping for the tunnel junction in the cells was in the range of 10^{19} to 3x10^{19} cm^{-3}.

Figure 13 shows that the resistance is a steep function of the doping. The expected series resistance (Table 17) of the cell from the emitter and grid I^2R loss was ~0.07 Ω-cm^2. We theorize that the cells are dominated by the series resistance of the tunnel junction, and that the variation in series resistance of the cells observed is mainly due to doping fluctuations in the 1 to 3 x 10^{19} cm^{-3} range in the P and N InGaAs in the tunnel junction, ranging from a negligible effect (the cells with 0.1 Ω-cm^2 presumably were from wafers were the junction doping was in the higher 3 x 10^{19} cm^{-3} end of the range) to become the dominant series resistance factor (cells with resistances of 1 Ω-cm^2 were presumably from the low 1 x 10^{19} cm^{-3} end of the range).

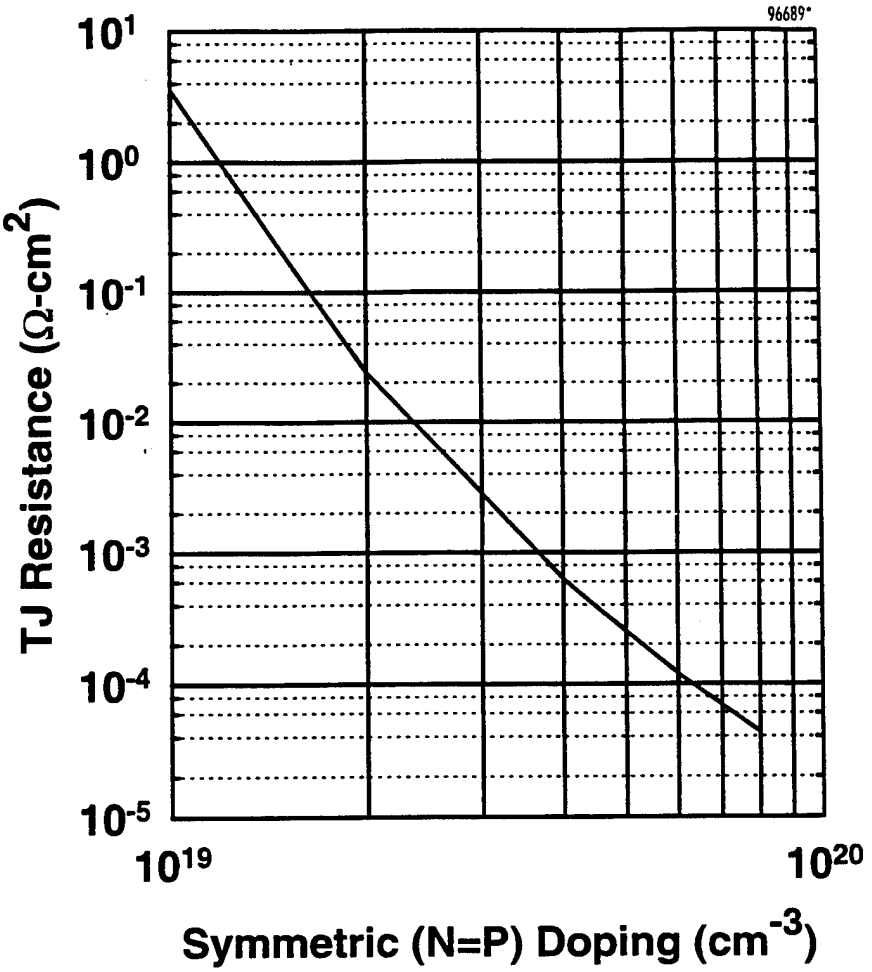

Figure 13 *Theoretical calculation of the InGaAs tunnel junction resistance used in the N/P InP/Si cells. Calculation assumes the doping in the N and P InGaAs is equal, which is approximately true in the actual devices.*

Table 17 *Estimated series resistance contributions for a 2 x 4 cm InP/Si cell.*

Lateral conduction through emitter layer to gridlines	15 mΩ	Measured Rsh 1500 Ω/square used; 300 μm gridline center-to-center spacing
Gridline metal to busbar	50 mΩ	Gold gridlines, 3μm high by 10 μm wide
Frontside contact	0.2 mΩ	Transmission-line model; contact $\rho \sim 4 \times 10^{-6}$ Ω-cm^2
Bulk Si wafer	~0 mΩ	25 mil, 0.005 Ω-cm wafer (4×10^{-5} Ω)
Backside contact	0.1 mΩ	$\rho \sim 10^{-6}$ Ω-cm^2
Total	65 mΩ	

One idea that may be worth pursuing in the future is to use a tunnel heterojunction of P-type InGaAs and N-type InP. This was tried by Keavney in the past, without good results. However, we have substantially increased the doping levels that can be obtained in InP and InGaAs since the Keavney cell. This structure may be more reproducible than a pure InGaAs homojunction, since the lower solubility of the Zn (10 times less) in the InP would prevent significant Zn diffusion out of the P InGaAs from occurring. The P InGaAs would be sandwiched between the P InP BSF of the cell and the N InP which forms the other half of the tunnel junction.

11 NASA-LEWIS-VERIFIED BOL CELL I-V DATA

Figure 14 shows a NASA-Lewis measurement (courtesy D. Brinker) of a Spire 2 x 4 cm N/P InP/Si cell with an epilayer structure similar to that shown in Table 2, but with a DTG InP buffer. This cell is about eight times larger and has a 20% better AM0 efficiency than any N/P InP/Si cell reported previously to this program. The average of fifteen similar 2 x 2 cm cells tested by NASA-Lewis is shown in Table 18, along with the best cell data.

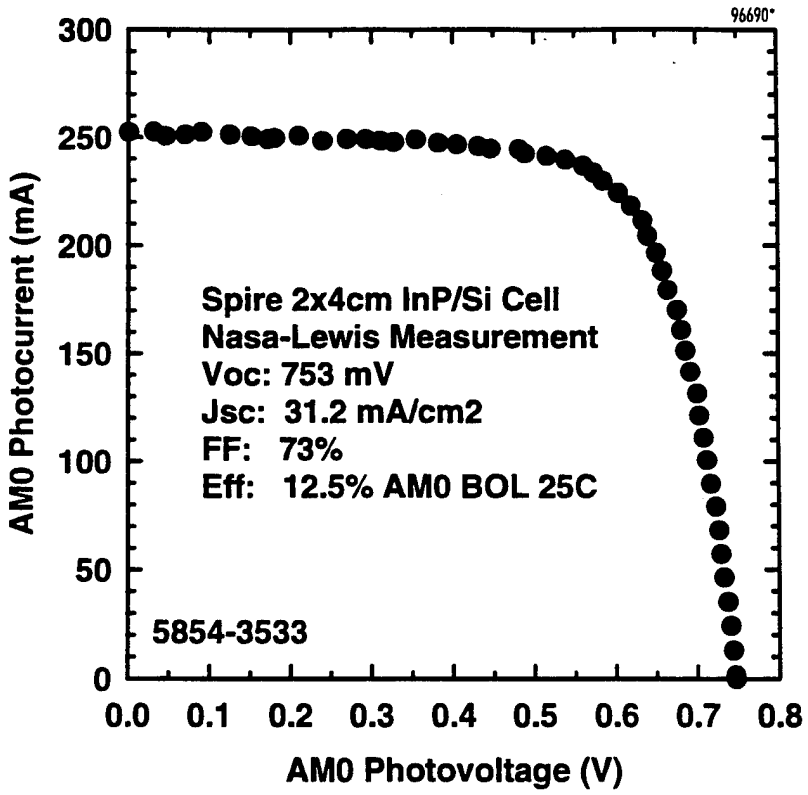

Figure 14 *AM0 I-V curve of an 8 cm² 12.5% Spire N/P InP/Si cell.*

Table 18 *Fifteen Spire n/p InP/Si 2 x 2 cm InP/Si cells.*

Wafer IDs 5827-3427,28,30	Voc (mV)	Jsc (mA/cm²)	Fill (%)	Eff. (%)
Average	755	31.3	71.2	12.3
Best Cell (3427-2)	761	31.8	71	12.6

12 1 MeV ELECTRON AND 3.9 MeV ALPHA PARTICLE DATA

Figure 15 shows the cell parameters of a 12% N/P InP/Si cell irradiated to a 1.2 x 10^{12} cm^{-2} fluence with 3.9 MeV alpha particles from a 1 mCi Am-241 source. Figure 16 shows actual 1 MeV electron irradiation data for a larger 2 x 4 cm N/P InP/Si cell.

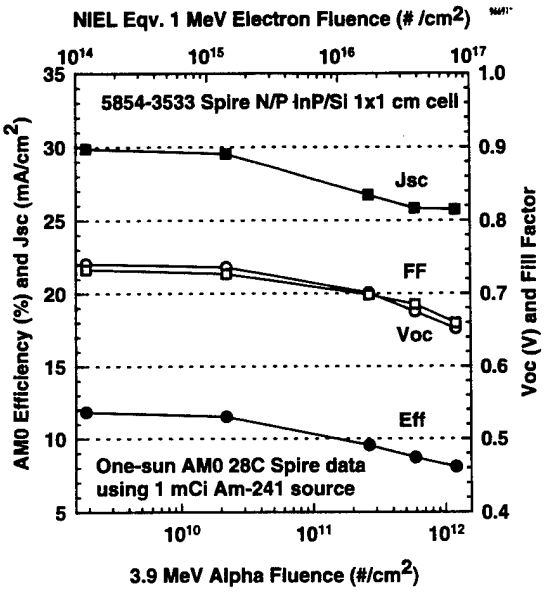

Figure 15 *Measured 3.9 MeV alpha data on a 12% BOL InP/Si 1x1 cm cell. Upper axis shows equivalent 1 MeV electron fluence by NIEL method.*

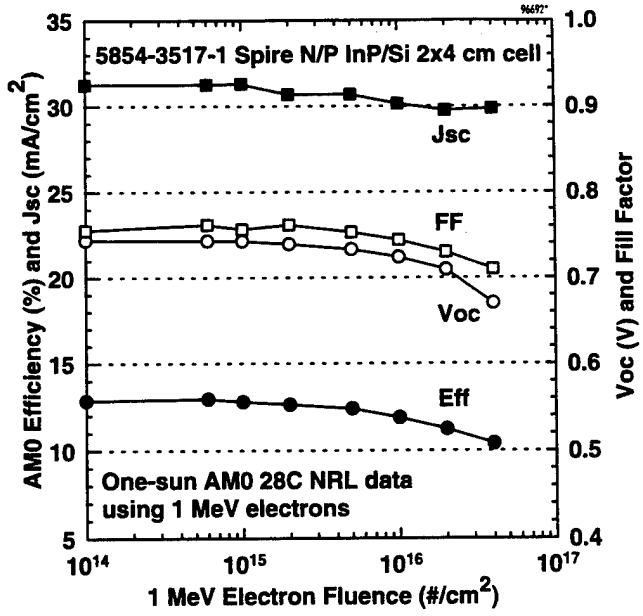

Figure 16 *Measured 1 MeV electron irradiation data on a 13% BOL 2 x 4 cm InP/Si cell.*

A 1 x 1 cm cell was used to enhance the irradiation uniformity from the small alpha source. The non-ionizing energy loss (NIEL) method was used to estimate the equivalent 1 MeV electron fluence (displayed on the upper axis) that would result in a similar displacement damage to the alpha fluence. The final fluence condition in both experiments was extremely high, about 40 to 80X higher than a typical "standard" 10^{15} 1 MeV electron fluence.

N/P InP/Si cell parameter data in Figures 15 and 16 are independent measurements performed at Spire with a 3.9 MeV alpha source (Figure 15) and at the Naval Research Laboratory (NRL) with 1 MeV electrons (Figure 16). The NIEL calculation done for Figure 15 (upper axis) allows the data to be compared in a fairly straightforward way (Table 19). In Table 19, the end-of-life (EOL) data is either actual 1 MeV electron irradiation out to a fluence of 4×10^{16} cm^{-2} or the alpha irradiation out to the NIEL-equivalent 1 MeV fluence. Since the alpha particles are much heavier and more damaging, the actual alpha fluence is less.

Table 19 *Comparison of alpha and electron irradiation data of n/p InP/Si cells.*

Cell ID	5854-3517-1	5854-3533
Size	2x4 cm	1x1 cm
BOL Voc (mV)	760	740
BOL Jsc (mA/cm^2)	31.3	30.1
BOL Fill (%)	76	74
BOL AM0 Eff (%)	12.9	12.0
Irradiation	1 MeV electron	3.9 MeV alpha
Fluence ($\#/cm^2$)	4×10^{16}	6.1×10^{11}
NIEL 1 MeV (ele/cm^2)	---------	3.8×10^{16}
EOL Voc (mV)	670	670
EOL Jsc (mA/cm^2)	29.9	25.8
EOL FF (%)	71	69
EOL AM0 Eff (%)	10.4	8.7
EOL/BOL Voc Ratio	0.88	0.91
EOL/BOL Jsc Ratio	0.96	0.86
EOL/BOL FF Ratio	0.93	0.93
EOL/BOL Eff Ratio	0.81	0.73

The Jsc EOL/BOL ratio degraded by 10% more under alpha irradiation than electron irradiation, which we do not fully understand. Overall, however, the agreement in EOL/BOL efficiency loss (27 vs 19%) is relatively good given the independent test and irradiation conditions. The efficiency loss of only 19 to 27% is impressive since the irradiation (4 x 10^{16} 1 MeV electrons/ cm^2) is about 40 times the value which is the standard EOL fluence condition (10^{15} 1 MeV electrons/ cm^2). Figures 17 and 18 show additional I-V and quantum efficiency data before and after irradiation.

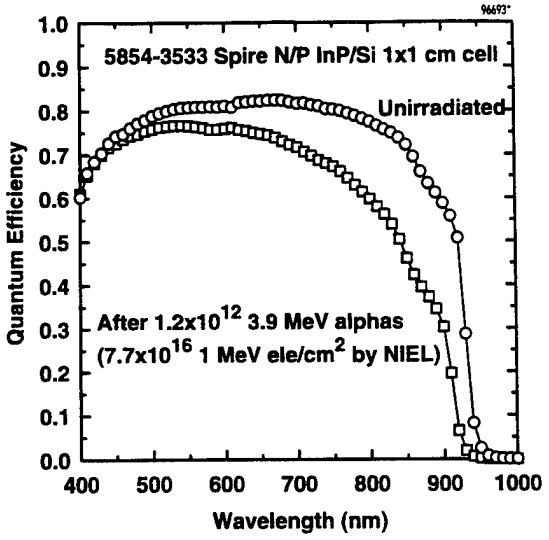

Figure 17 *InP/Si 2 x 4 cm cell I-V curves before and after various 1 MeV electron irradiation.*

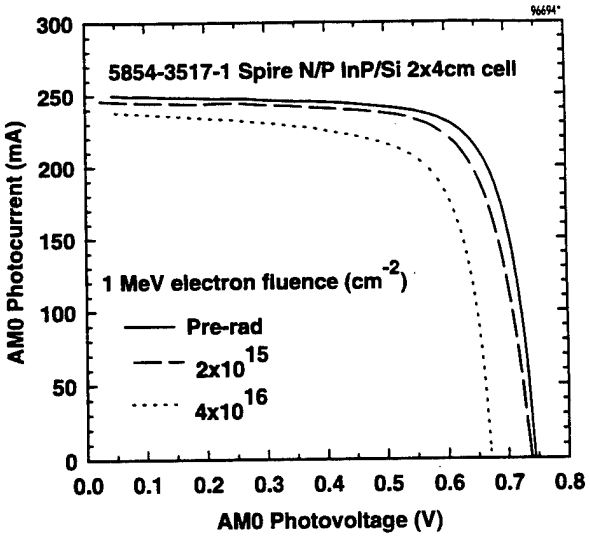

Figure 18 *InP/Si cell quantum efficiency data before and after 3.9 MeV alpha irradiation.*

Integrating the area under the curves of Figure 18 against the AM0 spectrum gave Jsc's which agreed very closely (± 0.3 mA) with our measured sun-simulator data before and after alpha irradiation, giving us confidence in the AM0 Jsc data for the alpha-irradiated cell.

Spire has also made P/N InP/Si cells which do not require the tunnel junction. Such P/N cells exhibit lower power output (by 20 to 30%) at BOL and over much of the fluence range examined to date. However, there is some evidence[19] that for 3 MeV proton fluences in excess of 8×10^{12} cm^{-2} P/N InP/Si cells may perform better than N/P InP/Si cells. This area is still under study, along with the effects of carrier removal at very high particle fluences.

13 CONCLUSIONS

N/P InP solar cells were made on Si wafers as thin as 16 mils with a BOL efficiency up to 12.6% (average 12.3%), with cell sizes up to 2 x 4 cm^2. The EOL efficiency after 4×10^{16} 1 MeV electrons/cm^2 was 10.4%. In contrast, GaAs/Ge cells after a fluence of only 1×10^{16} 1 MeV electrons have an efficiency[20] of ~6.6%.

The Si wafers were used to gain a decrease in weight and an increase in EOL power density (W/kg) since the Si wafers weigh about half that of InP. Although use of the Si wafers instead of InP wafers lowers the BOL efficiency from about 19% to 12.5% for the N/P InP cells, the EOL efficiency after high irradiation is similar for both cell types. Therfore, since the EOL efficiency is similar and the Si wafers weigh less, an increase in the EOL power density is obtained by use of the InP cells on Si wafers.

We have presented calculations showing that for many high radiation missions (between 2000 and 10000 km), panels with InP/Si cells can have over twice the panel power density of either GaAs/ Ge or Si cells.

Illuminated I-V and quantum efficiency data before and after high-fluence 1 MeV electron and 3.9 MeV alpha irradiations on these N/P InP/Si cells were compared, indicating that these cells have a fairly flat output power degradation curve. Since there is very little difference between BOL and EOL power output, demands on the power conditioning system should be much less than with other types of space cells now in use.

Finally, we estimate that the eventual cost of InP/Si cells will be similar to present GaAs/Ge cells since similar metalorganic chemical vapor deposition systems are used for epitaxial growth in both cases, as well as similar equipment for the cell fabrication. In addition, the Si wafers are much less expensive than Ge wafers.

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