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Adaptive Solutions, Inc.	N/A	Office of Naval Research

6c. ADDRESS (City, State, and ZIP Code)	7b. ADDRESS (City, State, and ZIP Code)
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High Performance Hardware and Software for Pattern Recognition and Image Processing

PERSONAL AUTHOR(S)
Wendell A. Henry

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			Image Processing

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Phase 3 Summary:

Work is in progress.

Option 1 Summary:

Work is in progress.

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At the time of this report, the project has been authorized to spend $1,997,949.00 for the Phase 1, 2, and 3 tasks plus the one optional task. The project has accumulated expenses of $1,806,631.00. Work on phases 1 and 2 are completed. Work on Phase 3 and the Optional task are in progress.

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22a. NAME OF RESPONSIBLE INDIVIDUAL Wendell Henry	22b. TELEPHONE (Include Area Code) (503) 690-1236	22c. OFFICE SYMBOL

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83 APR edition may be used until exhausted.
All other editions are obsolete.

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R & D Status Report

June 20, 1996

ARPA Order No.:

A407

Contractor:

Adaptive Solutions, Inc.

1400 NW Compton Drive, Suite 340

Beaverton, OR 97006

Contract No.:

N00014-93-C-0234

Contract Amount:

$1,997,949.00

Effective Date of Contract:

November 8, 1993

Expiration Date of Contract:

December 7, 1996

Principal Investigator:

Wendell A. Henry

Telephone Number:

(503) 690-1236

Title of Project:

High Performance Hardware and Software for Pattern Recognition and Image Processing

Title of Work:

R&D Status Report

Reporting Period:

March 1, 1996 through May 31, 1996

Disclaimer

Project Summary:

Phase 1 Objective:

Build PC/AT form-factor plug-in board using which implements the CNAPS architecture.

Phase 2 Objective:

Port CNAPS Software Development Kit to CNAPS PC board and Windows environment.

Phase 3 Objective:

Design and implement a C-callable function library which includes image processing and neural network functions, and executes on the Phase 1 CNAPS/PC board.

Option 1 Objective:

Design of portions of the next-generation CNAPS chip (X2).

Phase 1 summary:

Done.

Phase 2 Summary:

Done

Phase 3 Summary:

Work is in progress.

Option 1 Summary:

Work is in progress.

At the time of this report, the project has been authorized to spend $1,997,949.00 for the Phase 1, 2, and 3 tasks plus the one optional task. The project has accumulated expenses of $1,806,631.00. Work on phases 1 and 2 are completed. Work on Phase 3 and the Optional task are in progress.

The contract stipulates that $1,997,949.00 is required for the completion of all tasks in Phases 1, 2, 3 and the exercised option. No additional funding is required to complete all phases of the project.

During this reporting period Adaptive Solutions was granted a six month extension to the expiration date of the contract. The contract now expires on December 7, 1996 instead of the original date of June 7, 1996. This extension was required because Adaptive Solutions has not been able to staff the projects at the originally intended level. The reduced staffing level has resulted in a delay of project completions. No additional funding is required to complete the projects, just additional time.

Description of Progress:

The previous Project R&D Status Report stated the following as the objectives for this reporting period:

1. *Complete full X2 chip LVS & DRC.*

2. *Complete X2 chip parasitic extraction, back annotation, and resimulation.*

3. *Complete verification of the X2's interface with the C2 sequencer chip and its interface with board logic.*

4. *Complete tape out of the X2 chip.*

5. *Complete reticle generation for the X2.*

6. *Start processing of X2 first silicon at chip foundry.*

7. *Complete C2 design changes for higher performance (DRAM controller & stdio).*

8. *Complete C2 design changes for increased testability.*

9. *Complete two iterations of C2 through place-&-route with ASIC vendor.*

10. *Write chip test vectors.*

11. *Complete the initial version of the library manual. This manual will cover the linear algebra portion of the library, and serve as the model for adding the image processing and recognition portions, as they are completed.*

12. *Complete the implementation and coding of the recognition portion of the library.*

13. *Begin the incorporation of the recognition portion in the manual.*

14. *Begin the implementation and testing of the image processing portion of the library.*

The following sections discuss the specific progress made in this reporting period in the hardware and software areas towards the stated objectives.

Hardware

    Board Design:

        No changes to the CNAPS/PC board hardware design took place this reporting period.

    Board Testing:

        Production shipments of the CNAPS/PC board continued.

    X2 Array Chip Design:

        Status of planned tasks from last period:

Verilog simulation	Completed
LVS & DRC	Completed
Tape out	Completed
Package design	Completed
Reticle generation	Completed
First silicon start	Completed

The X2 completed final circuit and layout verification and the product was taped out. The simulations were run with back annotated parasitics, all interconnect variations of the processor node have been validated. The reticle generation and tape out paperwork was generated reviewed, and finalized. The GDS stream data was converted to MEBES data and reticles were generated. The first silicon lot was started at Sharp Corporation (Adaptive's foundry) in Japan. The current forecast is that Sharp will complete the first wafers on July 10, and Sharp will build the remaining reticles as needed in their mask shop.

The X2 and C2 timing requirements were reviewed in detail, some modifications were made to adjust the set up and hold times on the X2 control pins. A set of output buffer models were supplied to the board design group.

The package details were finalized and the first samples were released for fabrication. The first packages should be available in mid-July.

The testing load board and probe cards have been ordered or are in house for the testing of first silicon. Vendors for assembly and burn in have been selected, and quotations have been secured for these services. The characterization and test vector generation efforts are underway, as well as the final documentation of the chip.

X2 Sequencer Chip (C2) Design:

Design of the C2 continued during this reporting period. The integration of the DRAM Controller, Global Arbiter, and Program Memory Controller with the Sequencer logic of the C2 was completed. This was done to meet performance and timing requirements at the system level when operating at a frequency of 40 MHz.

In addition to the above design changes, the I/O facility of the Sequencer logic was redesigned to insure maximum input and output data rates. The redesign insures that input and output will each be able to achieve 40 MB/second and that concurrent input and output will achieve 80 MB/second.

Package and design rules were received from the ASIC vendor and incorporated into the C2 design.

Functional validation tests were written and run against the C2 design using the Verilog simulator. This simulation was done in the framework of a complete system level board design. Tests were used to validate the operation of the DRAM Controller and Arbiter in the presence of multiple bus masters. Likewise, validation tests were used to insure the proper operation of the Sequencer logic and program memory control. During this reporting period a large number of test programs were written from which test vectors will be extracted for chip testing by the ASIC vendor.

The C2 and X2 gate-level designs were merged and functional tests, using the Verilog simulator, were run to validate the interface between the C2 and the X2. These tests resulted in slight modifications to the timing of some of the X2 control pins. The final outcome of the merged C2 and X2 simulations was increased confidence that the two chips will be able to successfully operate together in a system at the 40 MHz design frequency.

A preliminary netlist of the C2 design was completed and passed on to Adaptive's

ASIC vendor for preliminary logic gate place and route. Feedback from the vendor after preliminary place and route with more accurate timing information will be used by the C2 design team to begin the analysis of internal critical timing paths to eliminate any and all timing violations.

Software

Design

Status of planned tasks from last period:

Library Specification	Completed
Basic linear algebra functions	Implementation & testing completed
Manual for linear algebra functions	Completed.
Classification functions	Implementation & testing completed
Manual for classification functions	In progress.
Image processing functions	In progress
Manual for linear algebra functions	In progress.

Implementation and Testing:

The C-Callable library is progressing well. The complete library will eventually consist of three portions: linear algebra, classification, and image processing.

The linear algebra portion, software and documentation, has been completed and was released for beta testing in May 1996. The linear algebra portion consists of 144 C-callable functions.

The implementation and testing of the recognition portion of the library has been completed. The classification portion consists of 35 C-callable functions. Incorporation of the classification portion into the Library Manual has begun.

The contents of the image processing portion has been defined. The implementation and testing of the image processing functions have begun.

Issues and/or Concerns

None.

Plans For Next Reporting Period:

During the next three months work will continue on Phase 3 of the contract and the exercised X2 chip development option. The following are expected to be achieved:

1. Complete the incorporation of the classification portion into the Library Manual.

2. Complete the implementation and testing of the image processing portion of the library.

3. Complete the incorporation of the image processing portion into the Library Manual.

4. Conduct additional testing of the fully integrated C-callable library to insure its robust-

ness.

5. Document X2 schematics.

6. Archive X2 database.

7. Develop X2 wafer test infrastructure.

8. Develop X2 assembly and burn-in infrastructure.

9. Develop X2 unit test infrastructure.

10. Continue validation of C2 chip design.

11. Generate C2 netlist and turn over to ASIC vendor.

Fiscal Status:

Amount currently provided on contract:	$1,997,949.00
Expenditures and commitments to date:	1,806,631.00
Funds required to complete work:	$191,318.00

Authorized Phase funding:	$1,997,949.00
Expenditures and commitments to date:	1,806,631.00
Authorized Phase funds remaining:	$191,318.00

At the time of this report, the project has expenditures and commitments totaling 90% of the funds allocated for the contract.

Wendell A. Henry   _6/20/96_
Wendell A. Henry   Date