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Over the course of this contract, we have focussed our effort on two important areas of optoelectronics technology: high power/high performance VCSELs and integration of optoelectronics components onto siliconsubstrates by a new technique called fludic assembly.

High multimode continuous-wave (cw) powers have been achieved from vertical-cavity surface emitting laser diodes (VCELs) without a heatsink.

Fluidic self-assembly (FSA) developed as a new technique which makes possible the integration of devices fabricated using dissimilar materials and processes.

A planar process has been developed that includes device isolation, bonding and contacting resultingin the first successful integration of VCELs onto Si by FSA.

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0. Introduction and Summary

Over the course of this contract, we have focussed our effort on two important areas of optoelectronic technology: high power/high performance VCSELs and integration of optoelectronic components onto silicon substrates by a new technique call fluidic assembly.

High multimode continuous-wave (cw) powers have been achieved from vertical-cavity surface-emitting laser diodes (VCSELs) without a heatsink. However, to our knowledge, single fundamental transverse mode powers have not exceeded 2.6 mW. We have quantitatively investigated the phenomena of the appearance of high-order transverse modes and has been attributed thermal lensing and spatial hole burning as causes of power limitation to these devices. External cavity provides a way to control the transverse modes of the surface-emitting laser diodes. Powers greater than 100mW pulsed and 2.4 mW cw in the lowest order (TEM_{00}) transverse mode are observed.

The longitudinal optical mode shift with temperature was measured in two vertical cavity surface-emitting laser (VCSEL) - type optical resonators with different GaAs and A1As layer structures. The measurements show distinct differences in the behavior of the cavities. From the data the thermal dependences of the indices of refraction of GaAs and A1As for wavelengths near $1\,\mu m$ were determined.

Substrate removal techniques are attractive for the integration of III-V compound semiconductor devices on Si for the integration optical and electronic devices, and on ther-

mally conducting substrates for heat sinking. We investigated the bonding of strained quantum well InGaAs vertical-cavity surface-emitting lasers on both Si and Cu substrates.

Fluidic self-assembly (FSA) is a new technique which makes possible the integration of devices fabricated using dissimilar materials and processes. The integration is accomplished by fluidically transporting trapezoidally shaped blocks made of one material into similarly shaped holes in a receptor substrate, we have performed a systematic study of the FSA integration efficiency which is presented below.

GaAs on Si has long been seen as a way to integrate GaAs optical devices with established Si electronics. unfortunately, the 4% lattice mismatch and the thermal expansion mismatch lead to high defect densities as well as residual thermal stress when GaAs films are grown heteroepitaxially. To avoid these problems, a self-assembly integration technique whereby lifted-off GaAs blocks suspended in liquid are allowed to fall into etched pits on a Si wafer. We demonstrate the quasi-monolithic integration of GaAs light-emitting diodes on Si wafers by a novel technique which utilizers fluid transport and shape differentiation

A planar process has been developed that includes device isolation, bonding and contacting resulting in the first successful integration of VCSELs onto Si by FSA.

The application of the FSA technique to integrate Si drivers on large area active matrix LCD display panels is also investigated.

1.1 Spatial hole burning and self-focusing in vertical-cavity surface-emitting laser diodes

High multimode continuous-wave (cw) powers have been achieved from vertical-cavity surface-emitting laser diodes (VCSELs) without a heatsink. However, to our knowledge, single fundamental transverse mode powers have not exceeded 2.6 mW. The appearance of high -order transverse modes has been attributed to thermal lensing and spatial hole burning, which depresses the gain in the center of the device while allowing it to rise at the edges. Because a local depression in the gain leads to a local increase in the real refractive index spatial hole burning can produce self-focusing effects if the induced index variation is at least comparable to that of other index guiding mechanisms. For this reason, highly index guided lasers, such as an etched post laser, may not exhibit significant self-focusing, but their mode size is necessarily small, which limits their single mode output powers. Weakly index guided lasers could potentially permit larger mode sizes, and hence, higher single mode powers. However, as we demonstrate experimentally and using a simple model, such lasers exhibit self-focusing, which causes the fundamental mode width to decrease with increasing mode power. This mode shrinkage limits the single mode power because the increased light intensity at the center of the device accelerates the hole burning process and this the appearance of higher-order modes.

The lasers studied were grown and fabricated in a way similar to what has been reported previously. They incorporate an active region of three pseudomorphic InGaAs quantum wells sandwiched between two high-reflectivity GaAs/AlGaAs distributed Bragg reflectors. Proton implantation provides carrier confinement and a gold top contact enhances the reflectivity of the top mirror. The output is through the n substrate, whose surface has

been antireflection coated. The lasers are "weakly index guided" due to thermal lensing, a transverse index guiding mechanism which dominates over gain guiding despite only moderate heating (10° C above room temperature at threshold).

We observed spatial hole burning in the spontaneous emission in a manner similar to that in Ref. 5, except that we employed spectral filtering to exclude resonant emission. Spontaneous emission was collected from a 35 X 35 μm laser at an angle of $\theta = 40°$ from the normal with a microscope objective. This tilt prevented light from the lasing modes from being collected and also blue shifted both the mirror stop band and the Fabry-Perot cavity resonance. A spectrally resolved one dimensional near field profile of the spontaneous emission was measured at the output of a spectrometer at a wavelength (1004nm) at which the mirror reflectivity is at a minimum and the intensity profile corresponds to the injected-carrier-density profile and hence, to the gain profile. Due to current spreading, the spontaneous-emission profile is radially symmetric with a nearly Gaussian radial variation below threshold.

For currents above threshold, the spontaneous-emission profiles are shown together with the corresponding laser output near fields (Fig. 1.1.1). The transverse modes are approximately Hermite-Gaussian in shape and separated by 0.06nm in wavelength. Just above threshold, only the fundamental mode lases. As the power increases, a hole burns in the carrier population near the middle [Fig. 1.1.1 (a)]. Eventually, the gain on the perimeter of the divide is great enough to support modes of the next higher order, TEM_{01} and TEM_{10}, which are nearly degenerate [Fig 1.1.1 (b)]. At still higher currents, the fundamental mode

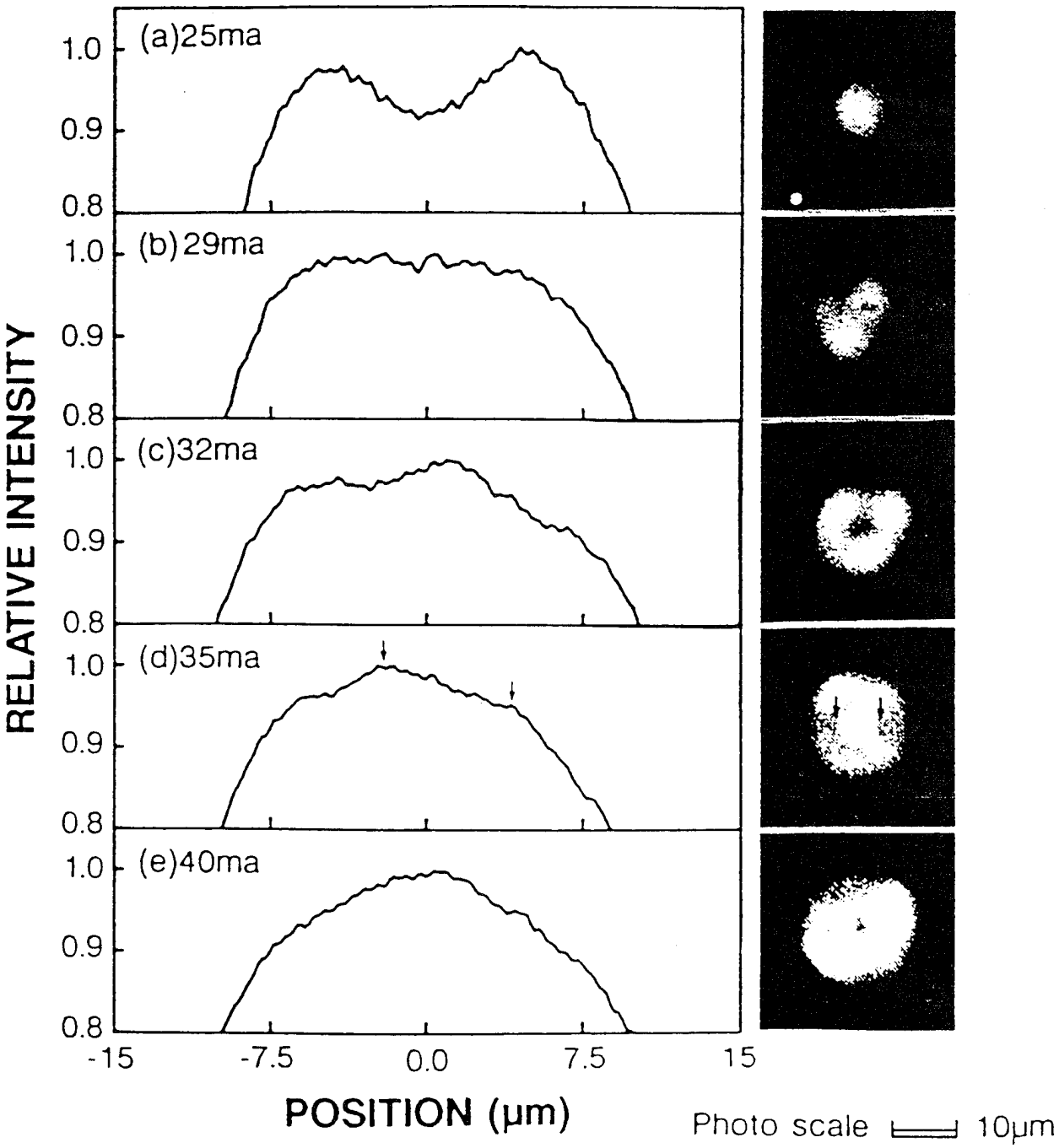
(a)25ma
(b) 29ma
(c)32ma
(d)35ma
(e)40ma
1.0
0.9
0.8
RELATIVE INTENSITY
-15
-7.5
0.0
7.5
15
POSITION (μm)
Photo scale
10μm

Fig. 1.1.1

ceases to lase, due to a coupled-cavity effect. A coupled cavity is formed with the substrate because the antireflection coating of the bottom surface is imperfect. As the current is increased, the transverse modes red shift and each mode dims as it passes through a frequency resonant in the substrate (at wavelengths spaced every $6\mathring{A}$). At 32mA only a "doughnut" mode lases, which comprises the TEM_{01}, TEM_{10}, and TEM_{11} modes [Fig. 1.1.1 (c)] and the gain is depressed around the edge of the injection region and peaks more sharply in the center. As the current is increased further, various superpositions of first-, second-, third-, and fourth-order modes appear [Fig 1.1.1(d) and (e)]. These modes combine to produce fairly uniform near-field patterns and gain profiles, but small peaks in the again profile, which correlate with dark regions in the near field, are still discernible in Fig 1.1.1 (d).

The depression of the spontaneous emission in Fig 1.1.1(a) corresponds to a depression of the gain and an increase in the refractive index, which leads to the self-focusing effect. If we assume that the transverse mode guiding is dominated by index guiding and ignore gain guiding, the for a quadratic change in index Δn over radius R the mode diameter is given by

$$W=\left[\frac{2}{\pi}\frac{1n}{\sqrt{2n}}\frac{2R\lambda}{\Delta n}\right]^{1/2}$$

We assume that the major contribution to Δn comes from thermal lensing at threshold and from self-focusing once a spatial hole has formed. using $W \approx 7$ μm [Fig. 1.1.1(a)]. Eq.

(1) predicts a change in index Δn =0.00023 over a radius R=W/2. The corresponding change in gain is $\Delta g = 4\pi\Delta n / (\lambda b \Gamma) = 250\ cm^{-1}$, where b=2 is the linewidth-enhancement factor and Γ =0.06 is the overlap of the optical mode with the active region. The change is -4% of the estimated gain difference between the center of the device and the lossy perimeter and is in good agreement with the -5% change in spontaneous emission over this same radius [Fig. 1.1.1 (a)].

To study self-focusing effects further we measured the mode width of a typical 20 X 20 μm device as a function of current. The mode diameter fluctuations shown in Fig. 1.1.2 are correlated to fluctuations in the fundamental mode power, which are produced by the substrate coupled-cavity effect. The fundamental mode of this laser is depressed at 18.8, 22.8, 25.5, and 28.5 mA and because self-focusing is power dependent, the fundamental mode size increases at these currents. During pulsed injection similar power and incident mode diameter fluctuations are observed in time as the modes red shift due to transient heating. In addition to these periodic fluctuations, self-focusing causes a rapid decrease in mode width with current above threshold (from 6.5μm at 16.5mA to 4.4μm at 18.2 mA). A correlation between out-put power and mode width is apparent in the L-q curve up until the point where the second-order mode starts lasing at 20.4mA (Fig.1.1.2).

At currents beyond 20.4 mA, the power in the fundamental mode fluctuates due to the coupled-cavity effect by its average value does not increase and the gradual decrease in average mode size is due to increasing thermal lensing. The temperature change from the center of the device to the perimeter is expected to follow $\Delta T \propto I^2$, and since $\Delta n \propto \Delta T$,

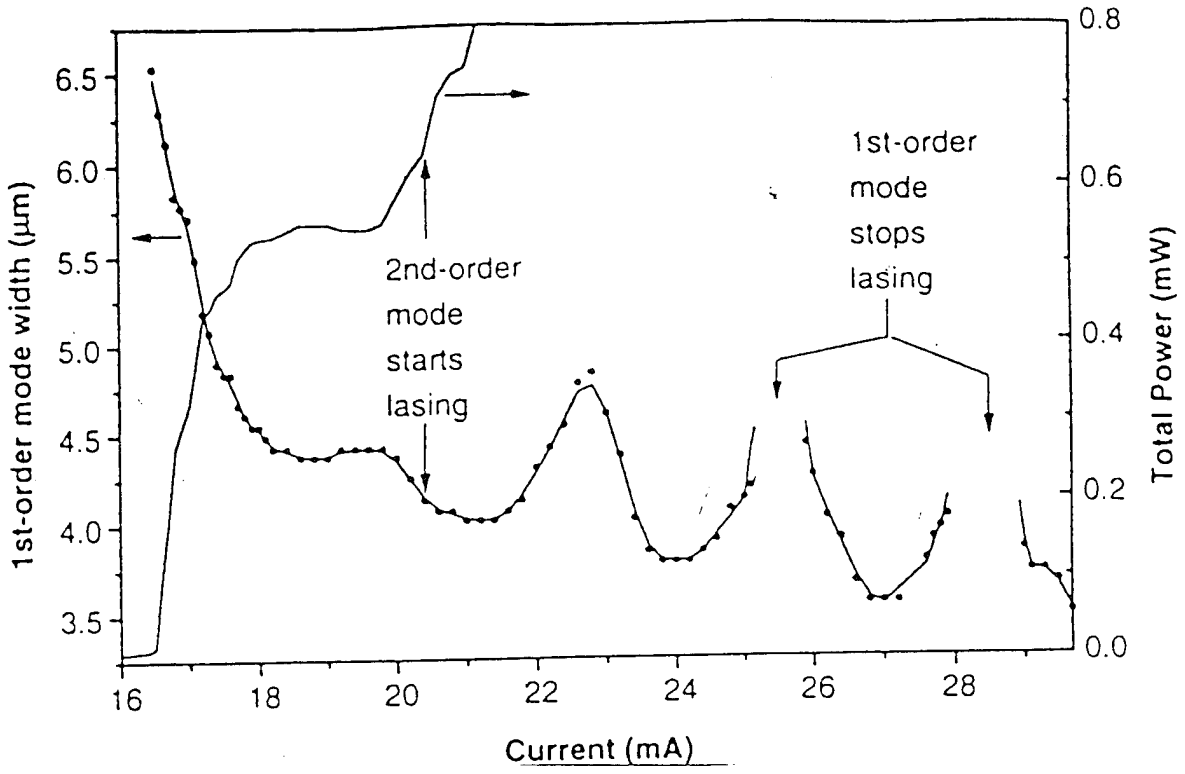

Fig. 1.1.2

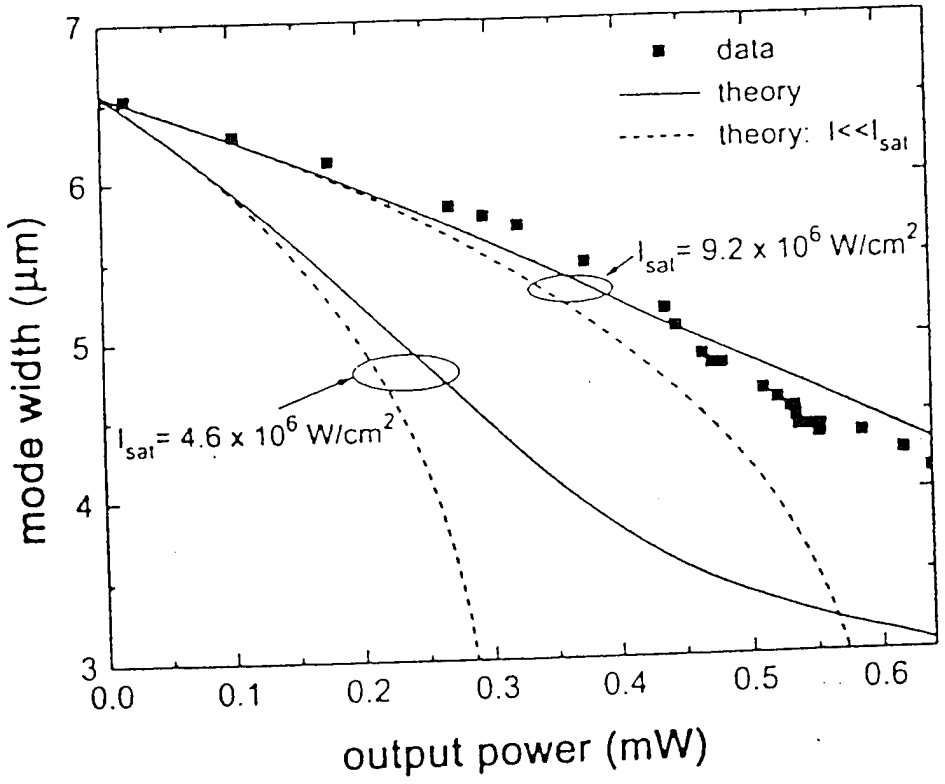

Fig. 1.1.3

we expect, using Eq. (1) that $W^{-2} \propto I$. From I=20.4 mA to I= 29.8 mA both the current and the average value of W^{-2} change by about 45%, consistent with a thermal lensing effect. On the other hand. thermal lensing alone could not produce the rapid mode shrinkage at threshold. As the current is raised 1% from 16.5 to 18.2 mA, W^{-2} changes by 118% and this rapid initial decrease in mode size is also observed under pulsed conditions when thermal effects are minimized. By causing the fundamental mode to contract, self focusing increases the intensity at the center of the active region and accelerates the hole burning process. The resultant rapid transition to multimode operation limits the single mode power to 0.64 mW.

The formation of a spatial hole at threshold and the attendant self-focusing can be modeled using an expression for the saturable gain which can be derived from the carrier rate equation, ignoring lateral diffusion effects which are small,

$$g(r) = \left[\frac{g_i \quad (r)}{1 + I(r)/I_{sat}} \right]$$

In Eq. (2) and subsequent equations, i represents optical intensity not current. $g(r)$ is the gain in the absence of stimulated emission, and I_{sat}=hvn/$\eta_{QW}\, g_N\, \tau$ is the saturation intensity.τ is the carrier lifetime, and g_N is the differential gain with respect to carrier density at threshold. Under heavy injection, the GaAs region surrounding the InGaAs quantum wells is heavily populated with carriers. These excess carriers serve as a reservoir to replenish carriers lost to stimulated emission. The term η_{QW} accounts for this fact and

can be as small as the ration of the thickness of the quantum wells alone to the thickness of the total active region (both quantum well and GaAs layers). If we assume that the corresponding induced index variation is parabolic, then $2\Delta n/R^2 = \lambda\, b\Gamma\, g''/4\pi$. These equations can be solved to find the mode width as a function of output power. Theoretical curves are compared to experiment in Fig 1.1.3 for several values of I_{sat}. A good fit is obtained for $I_{sat} = 9.2X10^6\ W/cm^2$. This value is obtained using $\pi_{QW} = 0.375$ and $g_N = 2 \times 10^{-16}\ cm^2$, which is somewhat lower than typical values quoted for InGaAs quantum wells but is not too unrealistic given the elevated device temperature and the fact that, in VCSELs the gain peak need not reside at the same energy as the lasing photon energy. In the limit $I_0 \ll I_{sat}$, a nonlinear refractive index can be defined $n_2 = \lambda b\, \Gamma\, g_{0th}/4\pi\, I_{sat}$ such that $n = n_0 + n_2 I$ and the mode width can be related to the power within the active region P (which is - 1000 x the output power). This is also plotted in Fig. 1.1.3. A laser with improved (i.e. higher) g_n, τ, and n_{QW} would have a larger value of n_2 and would unfortunately, exhibit greater self-focusing.

In conclusion, we measure spatial hole burning in weakly index guided VCSELs and show that spatial holes produce a significant lensing effect (self-focusing). Self focusing is shown to cause a power dependent decrease in fundamental mode size with pumping above threshold that leads to reduced efficiency and mode breakup, thereby limiting the maximum single mode power. Spatial hole burning alone would limit the single mode power, but the presence of self focusing makes the hole burning problem much worse.

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1.2 High single-transverse-mode output from external-cavity surface-emitting laser diodes

Room-temperature cw electrically pumped external-cavity surface-emitting laser diodes are reported. The external cavity provides a way to control the transverse modes of the surface-emitting laser diodes. Powers greater than 100mW pulsed and 2.4 mW cw in the lowest order (TEM_{00}) transversemode are reported. The surface-emitting laser diode was grown on a p-doped substrate, resulting in uniform current injection in devices as large as 100μm in diameter. To our knowledge, this is also the first report of a working surface-emitting laser diode grown on a p-type substrate.

Vertical-cavity surface-emitting laser diodes (SELDs) continue to be a topic of intense interest from the point of view of both applications and manufacturability. Recent results show that they can produce continuous wave (cw) output powers of over 10mW without heatsinking. A major problem with these devices is that, at high powers, they tend to lase in multiple transverse modes. To our knowledge, the maximum cw single-mode output power reported is only 2.6mW. The origin of multiple transverse mode behavior is a combination of thermal lensing spatial hole burning, self-focusing and nonuniform current injection. This fundamental problem limits the amount of power from a SELD that can be coupled into a single-mode fiber or focused into a diffraction limited spot. Multiple transverse modes also give rise to mode-partition noise, which has been shown to limit the usefulness of SELDs in high-speed communications.

In this letter, we demonstrate the use of an external cavity to maintain single transverse mode operation at all bias levels. The SELD is of standard construction except that the reflectance of the top mirror is reduced to 86% and the laser is coupled to an external cavity (Fig.1.2.1). The transverse modes in this configuration are determined primarily by the external cavity and controlled both by using an intracavity aperture and by adjusting the cavity length which changes the mode diameter. The aperture dilation and cavity length adjustments increase the diffraction loss of the higher-order modes more than that of the lowest order mode. If these losses are high enough, the higher order modes never reach lasing threshold. In order to minimize the overall loss in the external cavity, its was necessary to choose the top-emitting SELD structure, since substrate absorption leads to a large cavity loss, which cannot be tolerated in an external cavity configuration. Nonuniform pumping which typically becomes a problem, was overcomed by growing the laser on a p-doped substrate with the p-doped mirror at the bottom and the n-doped mirror at the top. The p-doped mirror accounts for most of the resistance of the device whereas the n-doped mirror has more uniform current injection than does the conventional structure. We observed no spatial nonuniformity in the spontaneous emission from devices as large as 100μm in diameter.

A schematic diagram of the SELD is given in Fig. 1.2.2. The device was grown by molecular beam epitaxy on a 2-in. substrate which was Zn-doped $1 \times 10^{19}\ cm^{-3}$. Growth conditions were similar to those for SELDs grown on n-doped substrates. The p-doped bottom Bragg mirror consists of 33 pairs of $Al_{0.9}Ga_{0.1}$As/GaAs quarterwave layers. The active region (designed for 980 nm lasing wavelength) consists of three undoped 8 nm

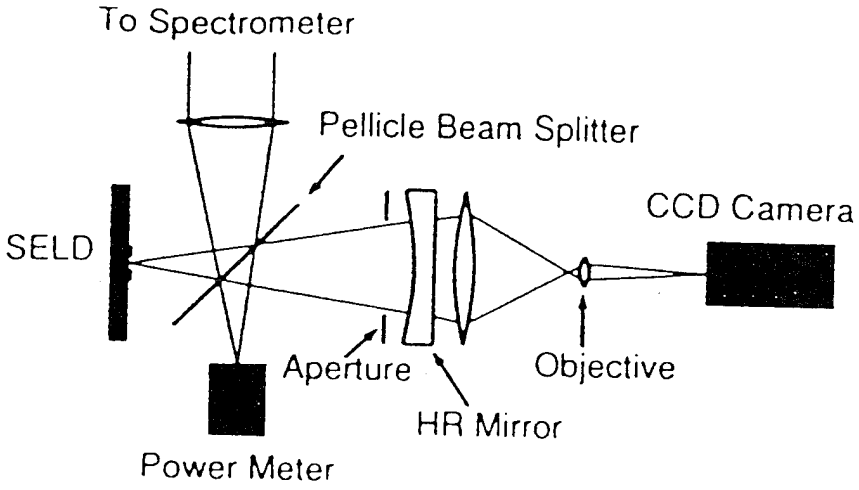

Fig. 1.2.1

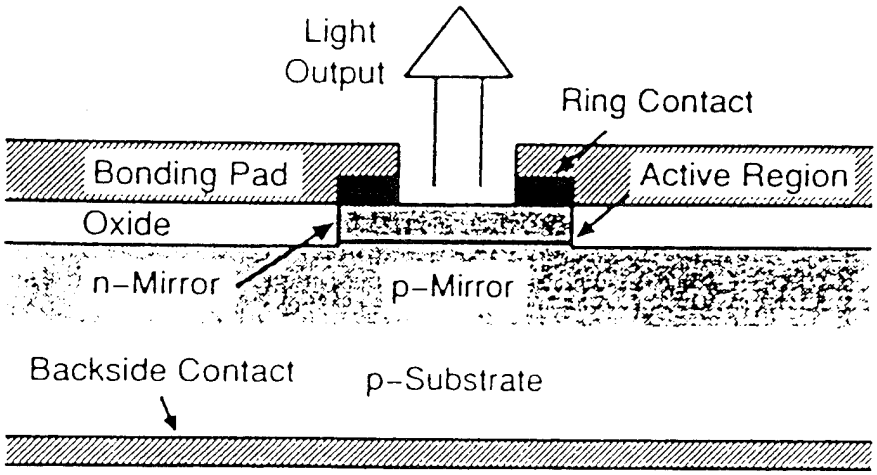

Fig. 1.2.2

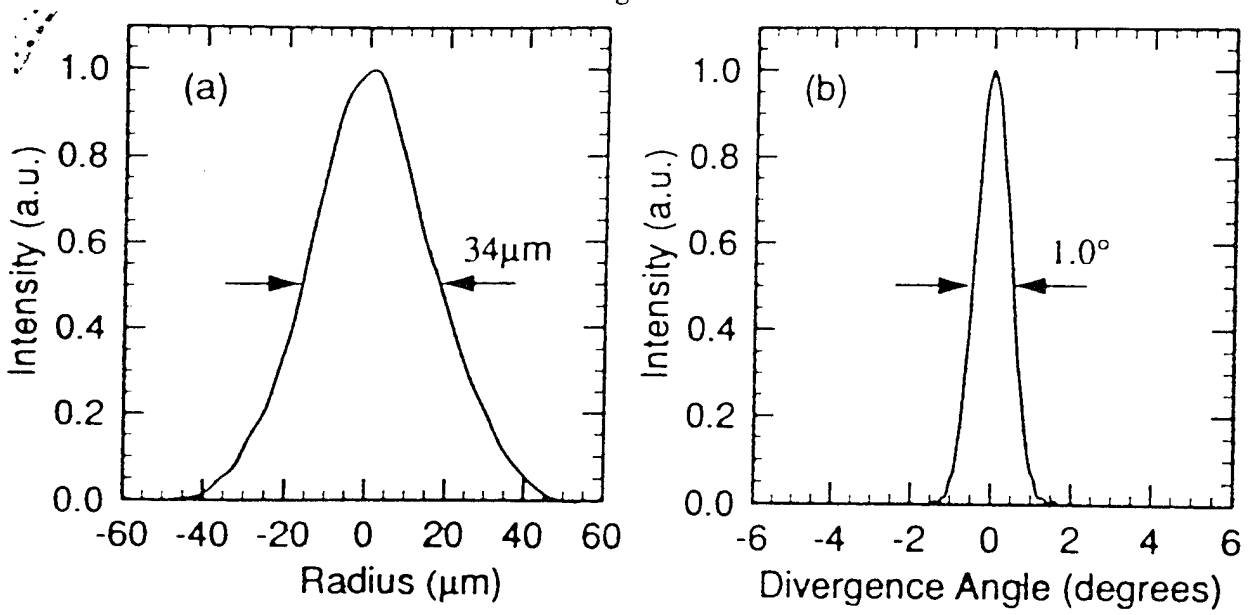

Fig. 1.2.3

$In_{0.2}Ga_{0.8}$ As quantum wells separated and surrounded by undoped 10nm GaAs barriers, centered in the peak of the standing wave by appropriate spacer layers. The n-doped top Bragg mirror consists of 7 pairs of $Al_{0.9}Ga_{0.1}$ as/GaAs quarter-wave by appropriate spacer layers. The theoretical reflectances of the bottom and top mirrors are 99.7% and 86%, respectively. Ring contacts of width $10\mu m$ and inner diameters ranging from 20 to $160\mu m$ were deposited to make ohmic contacts to the top mirror. Current confinement was provided by etching through the top mirror and gain region.

The experimental setup is shown schematically in Fig. 1.2.1. The external cavity is defined by the SELD on one end and a high reflectivity concave mirror (transmissions of 0.1%) with a radius of curvature of 10cm on the other end. In the cavity, the beam waist (near-field) is located at the SELD and the concave mirror is at a sufficient distance to be in the far-field. The external-cavity resonator has two regimes, the stable regime, where the cavity length is less than the radius of curvature of the mirror, and the unstable regime, where the cavity length is longer than the radius of curvature of the mirror. An adjustable aperture is placed inside the cavity in the far-field so that higher order modes with larger divergence angles can be cut off. Inside the cavity, a pellicle beam splitter provides output coupling which can be adjusted by changing the pellicle angle. The two beams from the pellicle are used to measure the output power and spectrum simultaneously. To view the SELD near-field, light passing through the high reflectivity mirror is reimaged, magnified within objective, and focused onto a CCD camera. With the objective removed, the far-field is incident on the camera.

A 100μm diameter laser had the highest multimode output power of 5.2mW (limited by heating) with a threshold current density of 810 A/cm^2 (threshold current densities for some devices were as low as 620 A/cm^2).For this result, the pellicle reflectance was 1.5% (roundtrip loss was 3%), the cavity length was slightly less than the radius of curvature (stable regime), and the aperture was opened all the way. When the intracavity aperture was closed down, the output became a single transverse mode. The highest single-mode power (2.4mW) was observed when the cavity length was set slightly longer than the radius of curvature of the mirror (unstable regime) and the aperture was open. The intensity profiles of the near- and far field at 2.4 mW are shown in Fig 1.2.3. the far-field full width at half maximum (FWHM) divergence angle of 1.0° is less than 1.3 times the diffraction limit for a Gaussian-amplitude near-field with FWHM of 34μm, assuming constant phase across the near-field. This configuration also gave the narrowest linewidth of 0.07 nm, centered near 985 nm. The L-I and V-I curves corresponding to the case when the cavity is aligned for maximum single-mode power are shown in Fig. 1.2.4.

To demonstrate that the external cavity configuration is capable of single-mode operation at high powers, we circumvented the heating limitation by pulsing the injection current of this device with a duty cycle of 0.1% We were able to achieve near single-transverse-mode (also less than 1.3 times diffraction limit) peak powers of over 100mW (limited by the voltage source). This result was achieved with a pellicle reflectance of 4.5%, the cavity in the stable regime, and the aperture closed down to approximately 0.5 cm. The pulsed L-I curve is shown in Fig. 1.2.5. With the pellicle reflectance set to the same value as was used for the cw measurements, the maximum peak power was 80mW.

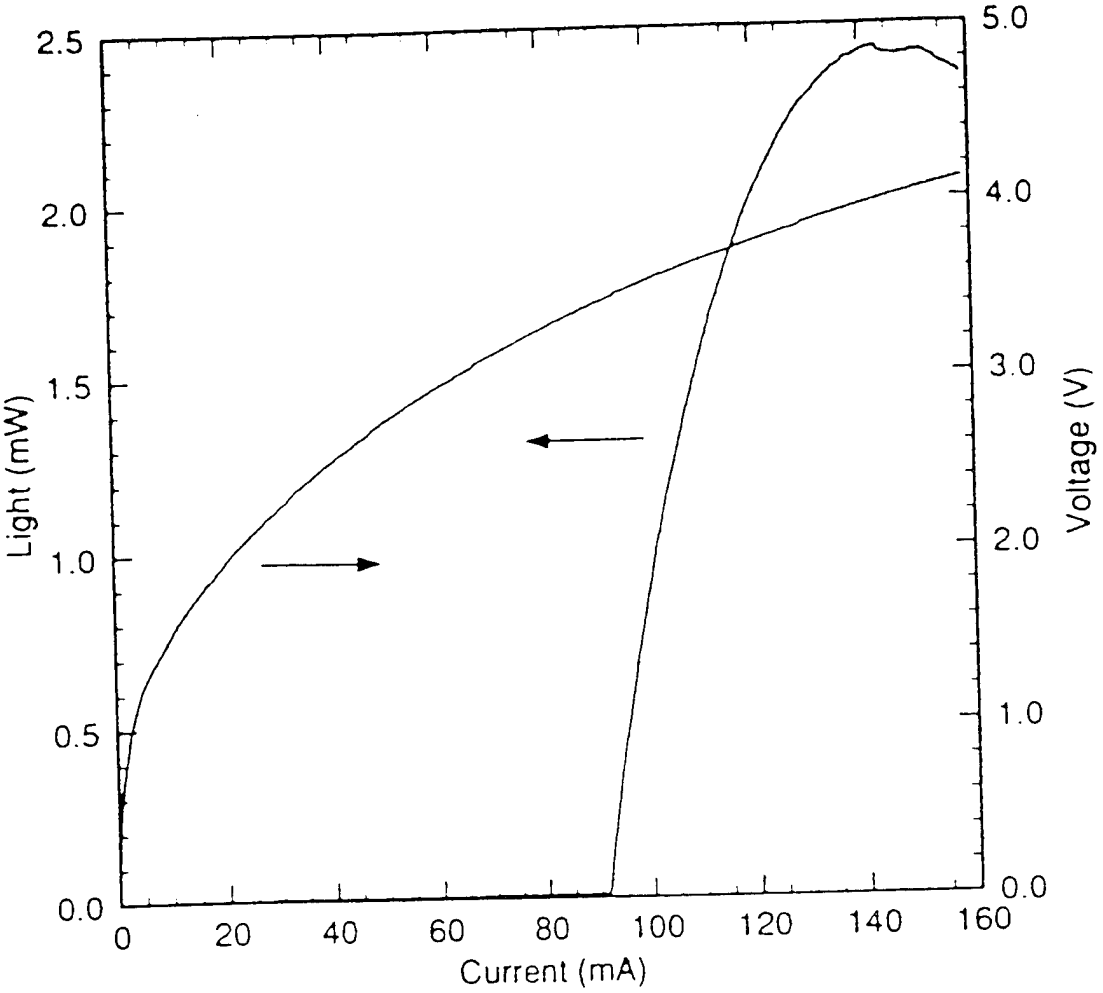
2.5
2.0
1.5
1.0
0.5
0.0
Light (mW)
5.0
4.0
3.0
2.0
1.0
0.0
Voltage (V)
0
20
40
60
80
100
120
140
160
Current (mA)

Fig. 1.2.4

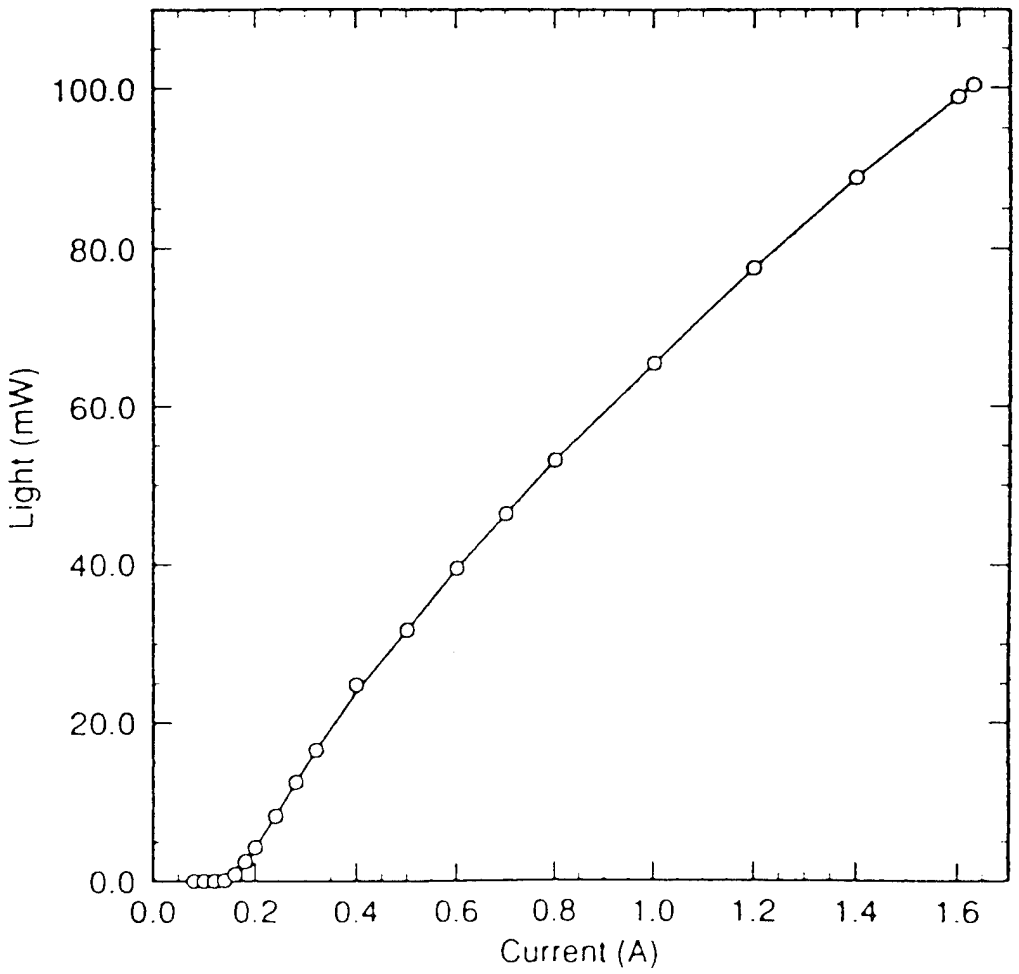
100.0
80.0
60.0
40.0
20.0
0.0
Light (mW)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
Current (A)

Fig. 1.2.5

The high pulsed powers of these devices clearly show that the limiting factor for cw operation is heating. If either the electrical or thermal resistance are reduced, or the efficiency increased, single-mode behavior ago all bias currents with higher cw power can be expected. This device has a maximum cw differential quantum efficiency of 8%. The efficiency is low primarily because the mode diameter (34μm) is considerably less than the pumped-area diameter (120μm). If the cavity length is adjusted to increase the mode diameter, the diffraction losses from the edges (ring contact) limit the efficiency. In order to make a more efficient device it is necessary to increase the ratio of the fundamental mode diameter to the pumped area diameter without increasing the diffraction loss of the mode.

In conclusion, we have demonstrated that an external cavity can be used to control the modes of a surface-emitting lasc and have achieved more than 100mW pulsed and 2.4 mW cw in a single transverse mode. This technique yields a single transverse mode that fills the entire device area despite any thermal lensing, spatial hole burning, or nonuniform current injection. We have also demonstrated the use of a p-type substrate for uniform current injection. Even better device performance can be expected from designs that reduce the heating and increase the efficiency.

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1.3 High single-mode output power from compact external microcavity surface-emitting laser diode

Transverse mode control is demonstrated in an electrically pumped surface-emitting laser diode coupled to an external microcavity with room-temperature single-mode powers reaching 2.0 mW continuous wave and 36.7 mW pulsed. The wavelength chirp is less than 0.044 nm for the pulsed resists. The external, microcavity is formed with a flat dielectric mirror placed less than 700μm from the wafer surface. Diffraction and spatial filtering in the external cavity provide high-order mode suppression and produce a large fundamental mode of width 30μm. This external cavity geometry readily lends itself top integration

High multimode continuous wave (cw) powers have been achieved from surface-emitting laser diodes (SELDs) without a heatsink. however, to our knowledge, single fundamental transverse mode powers have not exceeded 2.6mW. A single transverse mode can be maintained by making a device small, but, to achieve high powers, large area devices are required. high-order transverse modes arise due to a combination of thermal lensing, spatial hole burning, self-focusing, and nonuniform current injection. These effects all lead to cavity nonuniformities which prevent a large area uniform mode from lasing.

Recently, we demonstrated a device that overcame these problems, using an external cavity to determine the cavity modes. A curved dielectric mirror was placed 10 cm in front of a SELD in a near-concentric geometry. Although this configuration effectively maintains a single transverse mode, it has the drawback of not lending itself to integration. Here, we report an external cavity structure which employs a flat mirror placed less than 700μm from the SELD surface. This external "microcavity" structure is attractive because a single longitudinal mode lases, many lasers on the same chip can utilize the same mirror, and the structure is compact and lens itself to integration. In this letter we demonstrate the use of the external microcavity SELD to produce a large-area high-power fundamental mode.

The design and the semiconductor structure have been described elsewhere. The device incorporates an active region of three pseudomorphic $In_{0.2}Ga_{0.8}$As quantum wells sandwiched between two GaAs/$Al_{0.9}Ga_{0.1}$As distributed Bragg reflectors. The structure was grown on a p-doped substrate with the p-doped mirror on the bottom and the n-doped mirror on the top. A ring-shaped ohmic contact of inner diameter 80μm and outer diameter 100μm, makes electrical contact to the top n-type mirror. Because the p-doped mirror accounts for most of the resistance of the device whereas the n-doped mirror has high lateral conductivity, this "p-down" configuration results in nearly uniform current injection into large-area devices. The high reflectivity bottom mirror consists of 33 quarter-wave pairs. In order to achieve strong coupling to an external cavity, the top mirror consists of only seven pairs and has a theoretical reflectivity of 85.6%. Substrate coupled-cavity effects are minimized by the high reflectivity of the bottom mirror, the high free carrier

absorption in the p-type substrate and the roughness of the alloyed p-type ohmic contact on the bottom surface.

The SELD/external cavity configuration is shown schematically in Fig.1.3.1. The external cavity is formed by the uppermost semiconductor Bragg mirror of the SELD and a flat dielectric mirror positioned close to the surface of the diode. The dielectric mirror, which serves as an output coupler, consists of a 1 cm glass substrate with a 96% reflective coating on the front surface. The length of the external microcavity can be adjusted to within a micron in conjunction with a piezoelectric transducer (PZT). The position of this mirror affects the phase and frequency dispersion of the wave reflected from the external cavity back into the gain section. The total reflection is a maximum when the reflections from the topmost Bragg mirror and the external mirror add in phase (i.e. the external cavity is anti-resonant). Longitudinal modes exist with wavelength spacing $\Delta\lambda \approx \lambda^2/2L$, where L is the external cavity length.

With the mirror placed immediately in front of the SELD surface, the fundamental mode is observed to be small (20 μm in diameter) and positioned eccentrically within the ring contact (due to some gain nonuniformity). As the current is raised above threshold, higher-order modes soon appear. This behavior is similar to that observed in single-cavity large-area SELDs except that the laser favors transverse modes at wavelengths which are both strongly resonant in the main gain-region cavity and weakly resonant in the lossy external cavity.

As L is increased, diffraction in the external cavity leads to larger transverse modes and the losses for higher-order modes rise as they increasingly overlap with the ring contact,

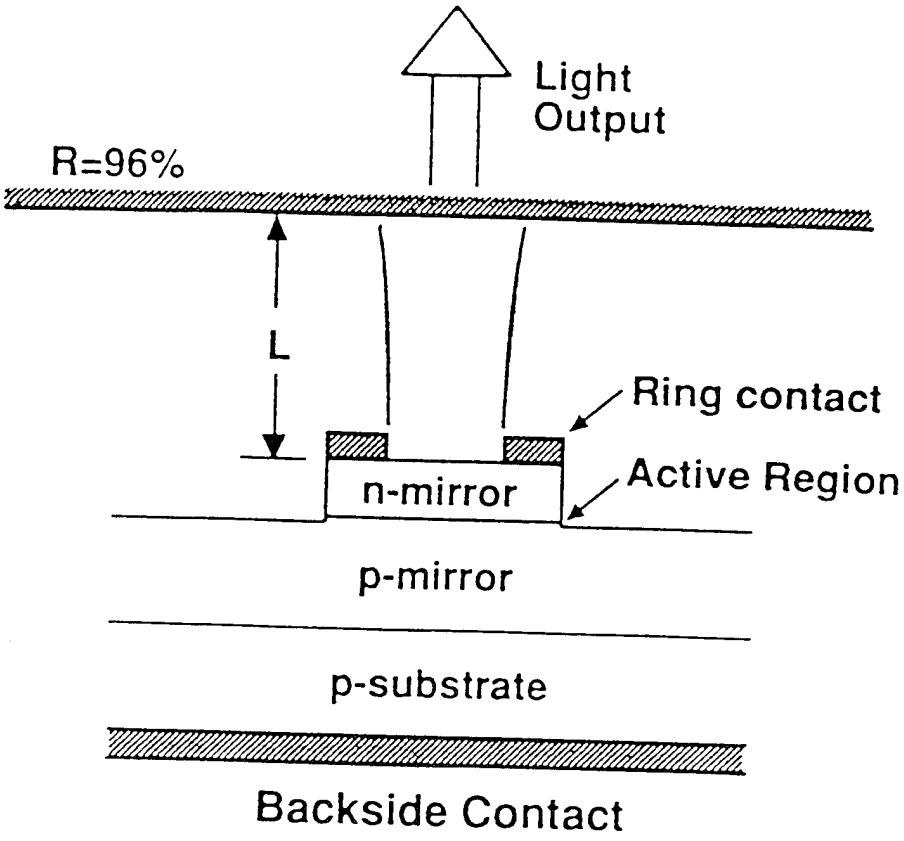

Fig. 1.3.1

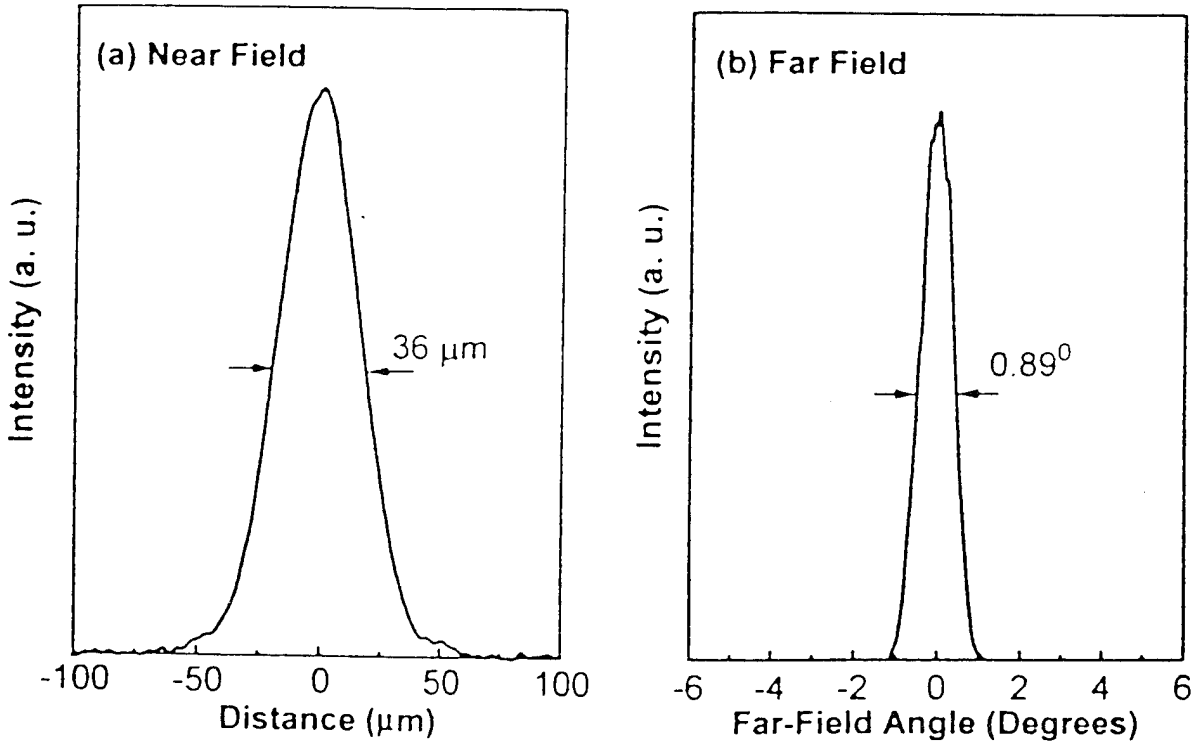

Fig. 1.3.2

which acts as an aperture. For $L > 280\mu m$, we obtain a large symmetric unpolarized fundamental mode which extends laterally to the ring contact. Second and higher-order modes are completely suppressed over the entire operating cw bias range. The single-mode near-field and far-field patterns for L= 280 μ m are shown in Fig. 1.3. 2. The far-field full width at half-maximum (FWHM) divergence angle of 0.89° is 1.3 times the diffraction limit for a gaussian-amplitude near-field with FWHM of 36 μ m, assuming constant phase across the near field. Contrary to what is observed in single-cavity SELDs, the mode size does not contract noticeably with increased injection current, for $L > 200\mu$ m, suggesting that the mode size is limited more by the ring-contact aperture than by thermal lensing or self-focusing.

The maximum single-mode cw power is achieved at L= 280 μ m is 2.0mW. The L-I curve (Fig. 1.3.3) exhibits jumps corresponding to longitudinal mode hops. The peak of the main-cavity Fabry-Perot mode red shifts as the current is increased and the diode heats, and from spectra taken at various currents (Fig.1.3.4), it is observed that the lasing wavelength remains fairly constant until the gain for an adjacent longitudinal mode exceeds that of the current longitudinal modes and a mode hop occurs. A small translation of the mirror merely shifts the position of the longitudinal modes and does not induce higher-order modes to lase. Higher-order modes, with wavelength spacing 0.050 nm are visible in the cw spectrum only when L is reduced below 280 μ m.

Mode hopping can be eliminated and higher powers achieved when the device is pulse injected with a 0.10% duty cycle to minimize heating. As seen in Fig. 1.3.5, the L-I curve no longer tolls off at 100mA. For L= 280 μ m, the second-order mode now reaches thresh

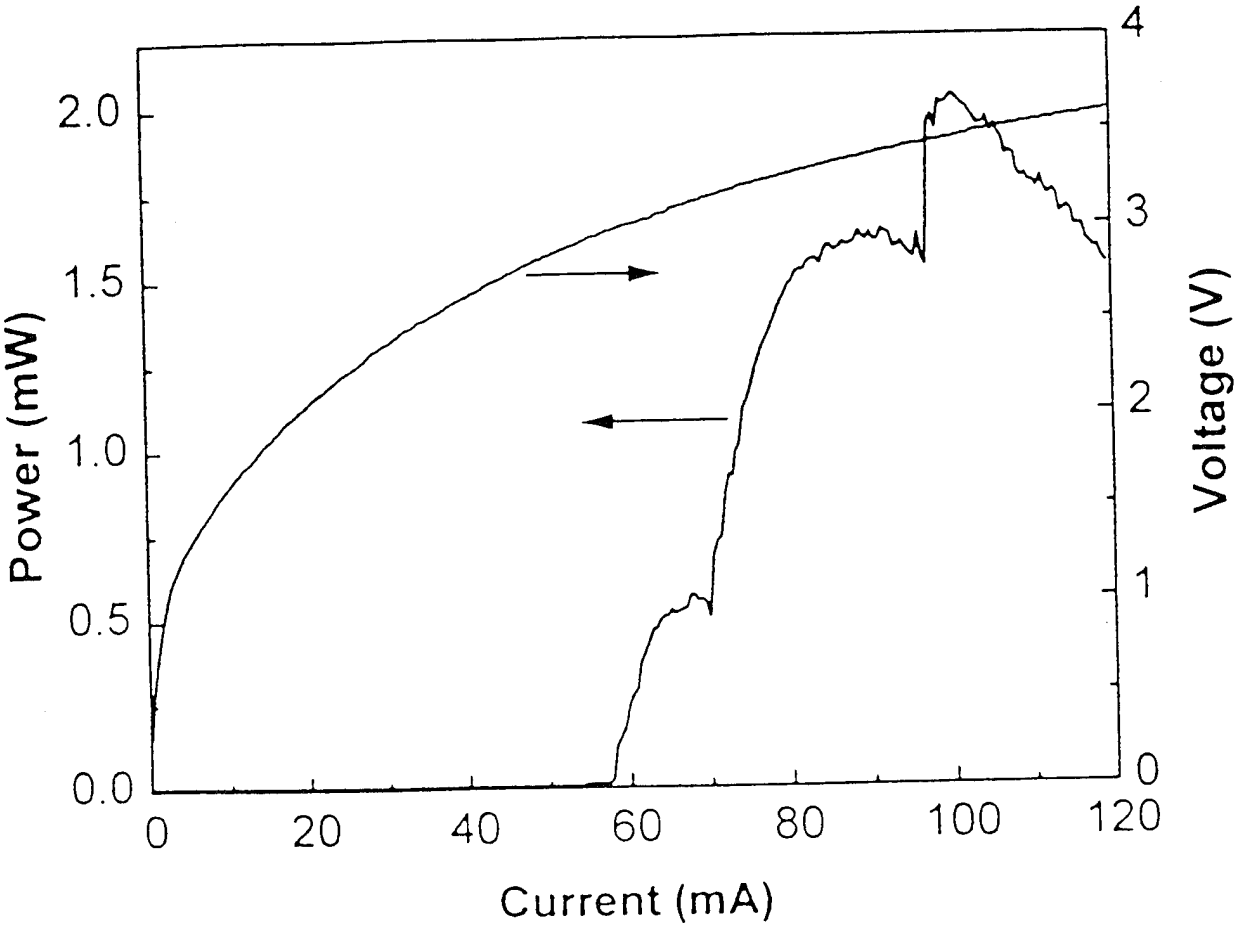

Fig. 1.3.3

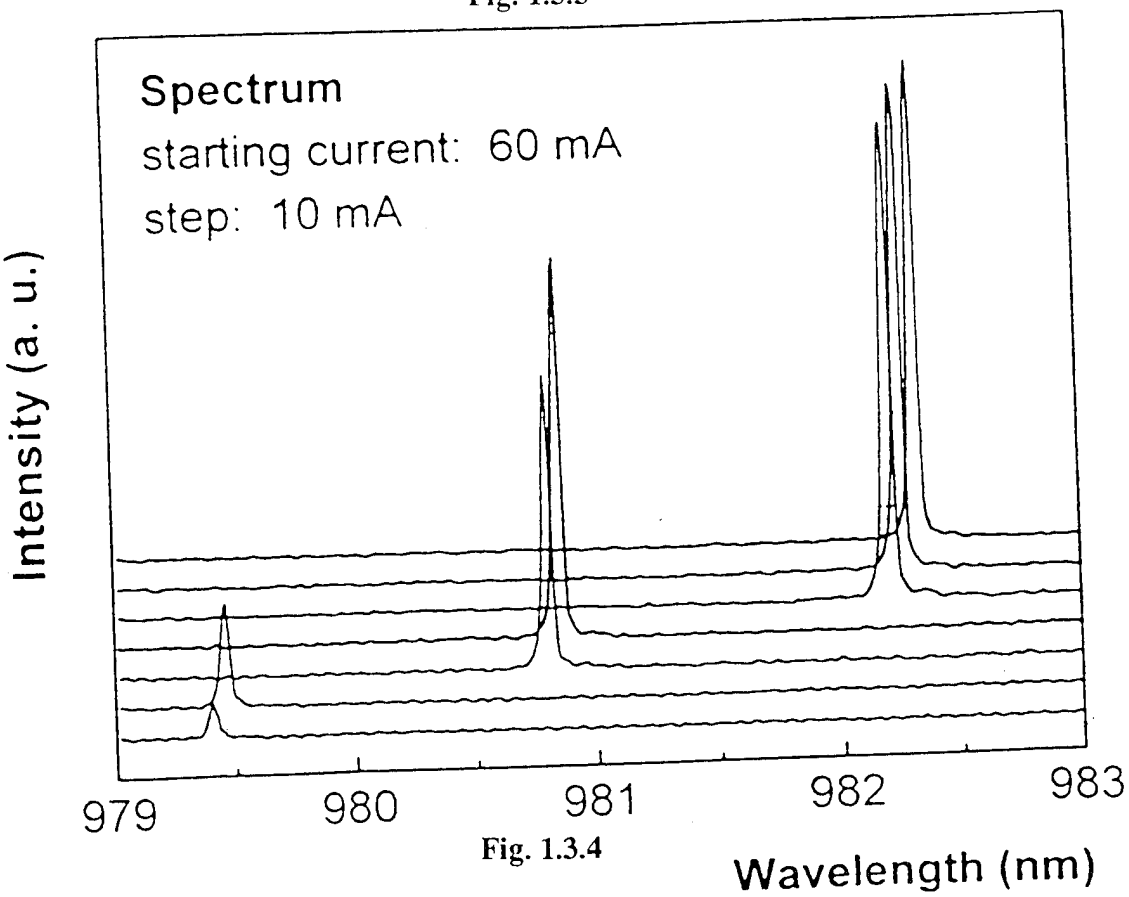

Fig. 1.3.4

old at 100mA, but its appearance can be delayed to higher currents by increasing L. A single-mode peak power of 36.7 mW is achieved $L = 686\mu m$. Because mode hopping does not occur, the L-I curves are smooth (Fig. 1.3.5). The external cavity largely determines the lasing wavelength so the frequency chirp is very small, For $0.1\mu s$ 600 mA current pulse, producing 36.7 mW peak optical power, the time integrated linewidth is only 0.044nm. This shows that the lasers can serve as stable sources if cw heating is reduced and/or the laser is modulated in such a way that its temperature does not fluctuate more than $3°C$.

In SELDs, the second-order mode is excited when spatial hole burning sufficiently reduces the gain in the center of the device relative to the edges. In the external cavity laser, moving the mirror further away increases the diffraction losses of the modes. If, as L is increased, the total losses of the second-order mode relative to the total losses of the fundamental increase, then the mode discrimination improves and a created spatial hole must be "burned" in the gain profile by the fundamental mode before the second-order mode reaches threshold. Improved mode discrimination is noted with increasing L up to $L = 686\mu m$ and the highest pulsed single mode power, 36.7 mW, is observed at this distance. Beyond this point, mode discrimination worsens.

The laser performance is currently limited by heating and spatial hole burning. Heating can be reduced by reducing either the electrical or thermal resistance of the device or by increasing its efficiency. The pulsed differential external quantum efficiency is only 12% because the mode diameter ($36\mu m$) is considerably less than the pumped area diameter ($100\mu m$). Future devices will have pumped areas comparable to the mode area. This

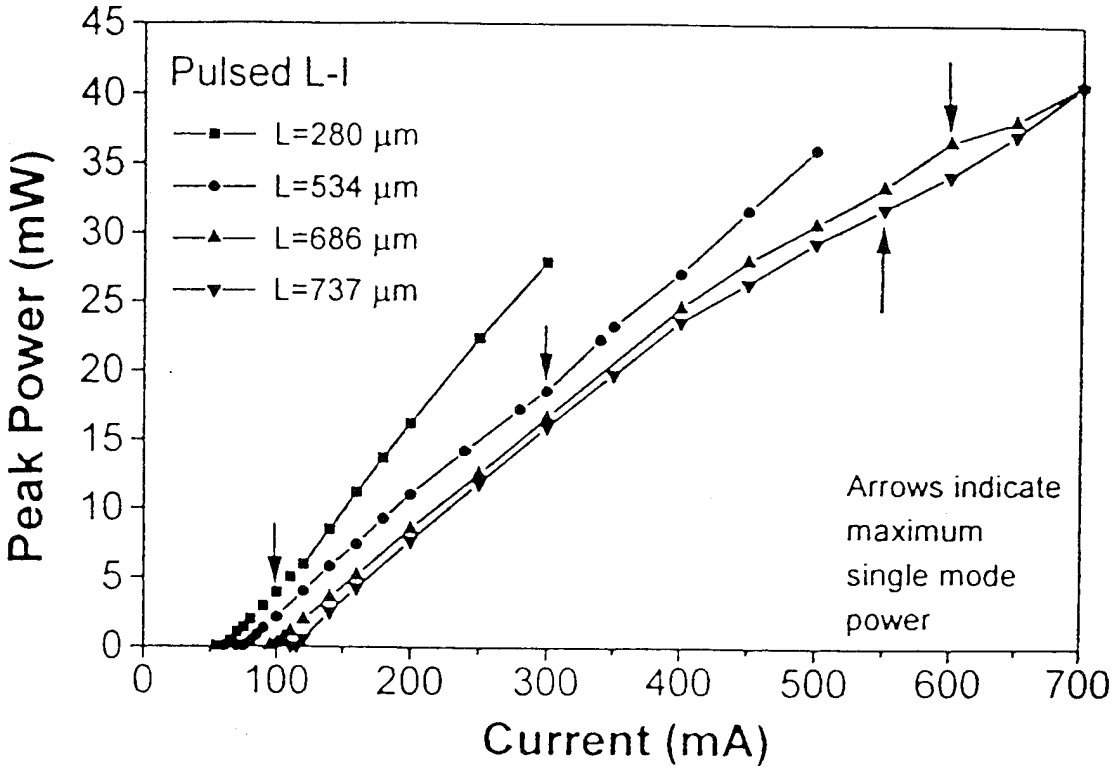

Fig. 1.3.5

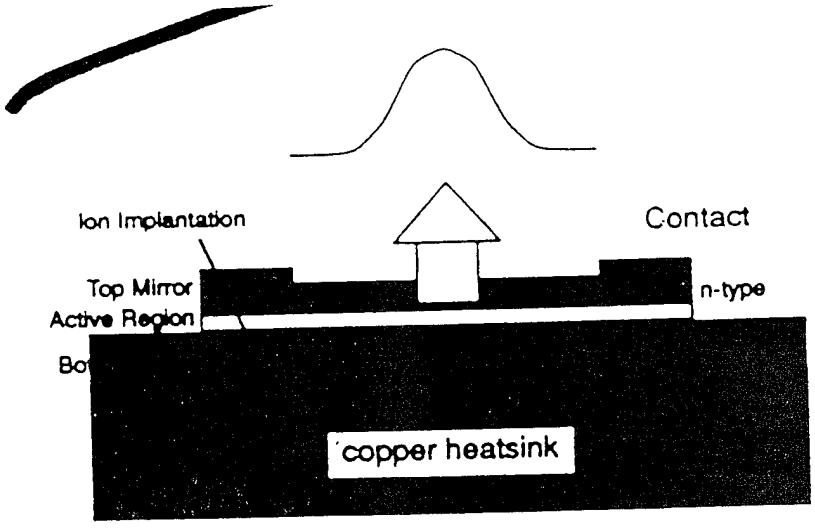

Fig. 1.4.1

change will both increase the quantum efficiency of the device and alleviate the spatial hole burning problem, thereby allowing higher single-mode cw powers to be reached.

In conclusion, we have demonstrated that an external microcavity can be used to control the transverse modes of a SELD and have achieved 36.7mW pulsed and 2.0mW cw in a single transverse mode. The mode is large, despite any thermal lensing or gain nonuniformities in the active region. Because the external cavity largely determines the lasing wavelength, this laser can serve as a narrow linewidth low-chirp source for optical communications. Since a stationary flat mirror is placed less than 700μm from the semiconductor surface, it can provide feedback to all devices on a chip simultaneously and can potentially be incorporated into the structure in an integrated fashion. The fundamental mode power achievable from this scheme should not be limited to current values and we expect improved performance from future devices.

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1.4 Heat-sinked external-cavity surface-emitting laser diodes

We have demonstrated the use of an external cavity to discriminate against higher order modes in surface-emitting laser diodes (SELDs) and cause the SELD to operate in the lowest order transverse mode for all bias. It was also stated that the limiting of the power to 2.5mW was due to two reasons. The first is the low efficiency of the laser due to the low ratio of the mode diameter (34μm) to the pumped are diameter (100μm). The second reason is that heating lowers the gain and therefore raises the threshold current.

We have designed a new structure which eliminates both these problems. The design involves growing the structure upside down and ion implanting for current confinement, then soldering the wafer to a copper substrate, removing the substrate and patterning the remaining thin SELD. More specifically the laser is grown with the p-mirror consisting of 15 $A1_{0.9}\,GA_{0.1}$ As and GaAs and GaAs quarter wave pairs on top of an active region and n mirror consisting of 7 $A1_9\,Ga_1$ As and GaAs quarter wave pairs which is all on top of a 1.2μm thick A1As etch stop layer. After removing the wafer from the MBE it is immediately evaporated with gold which forms part of the bottom mirror and the contact. After evaporation, deep (10μm) alignment marks are etched in the wager for future use. The wafer is then patterned with oxide, photoresist, and oxide for an ion implantation mask. After ion implantation, 100 A of chrome, .4μm of Ni, 1000 A of gold, 0.5μm of tin and 1000 A of gold were evaporated onto the substrate, The wafer was then cleaved up into 4 mm by 4 mm squares and placed on a copper substrate which was plated with 10μm of

gold. The wafer was held in contact to the copper with a force of approximately 10 N placed in an H_2 atmosphere furnace which was ramped up to 30 degrees.

After the bonding to copper, the wafer was them lapped down to 50μm and etched in an 100:6 $H_2O_s : NH_4OH$ selective etch. After reaching the A1As etch stop layer the wafer was dipped in concentrated HF for 20 seconds. Mesas were then etched and contacts evaporated yielding the structure shown schematically in Fig.1.4.1.

It was observed that this technique provided a strong and uniform bond between the GaAs and the copper substrate. In addition, the thermal resistance of these lasers was drastically reduced compared to the previous structure.

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1.5 Electrically-pumped external cavity surface-emitting laser diodes

Vertical-cavity surface-emitting laser diodes (SELDs) continue to be the topic of much research and recent results show that they can produce CW powers of above 10mW without heatsinking. For many applications, a major problem with SELDs is that they only operate in a single transverse mode at low powers. The reason for multiple transverse modes is a combination of the thermal lensing, spatial hole burning, and non-uniform cur-

rent injection. We demonstrate the use of an external cavity to maintain single transverse mode operation at all currents. More specifically we have reduce the reflectivity of the top mirror from above 99% to 85% and placed the SELD in an external cavity. The results in transverse modes controlled by the use of an aperture in the external cavity or by adjusting the cavity length. In order to provide more uniform current spreading, we designed a novel structure in which the SELD was grown on a p-doped substrate with the p-doped mirror on bottom and the n-doped mirror on top. We have observed that the current can spread uniformly over a device as large as 100μm in diameter.

The SELD was grown on a p-doped ($1 \times 10^{19}\ cm^{-3}$) substrate by molecular beam epitaxy. The p-doped bottom Bragg mirror consists of 33 pairs of $Al_9\ Ga_1$ As and GaAs quarter wave layers. A schematic diagram of the SELD is given in Fig. 1.5.1. Ring contacts of width 10μm were were deposited to make contact to the top mirror. Current confinement was provided by etching through the top mirror and gain region.

The experimental setup is shown schematically in Fig. 1.5.2. The external cavity is defined by the SELD on one end and a high reflectivity (HR) coated concave mirror (transmission =0.1%) with a focal length of 10 cm on the other end. A pellicle beam splitter was used inside the cavity for adjustable output coupling. Threshold current densities were as low as 620 A/cm^2 for some devices. The highest power of 2.4 mW into a single transverse mode (i.e. the far-field was a near diffraction -limited single lobe based on a Gaussian near-field) was observed with the cavity length set slightly longer than the focal length (unstable resonator). This configuration also gave the narrowest spectrum of width 0.07 nm. By pulsing this device with a duty cycle of 0.1% we were able to achieve near single-mode peak pow

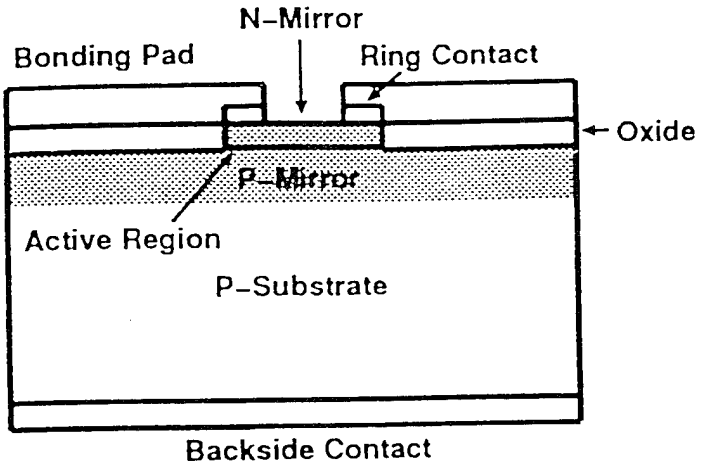


Fig. 1.5.1

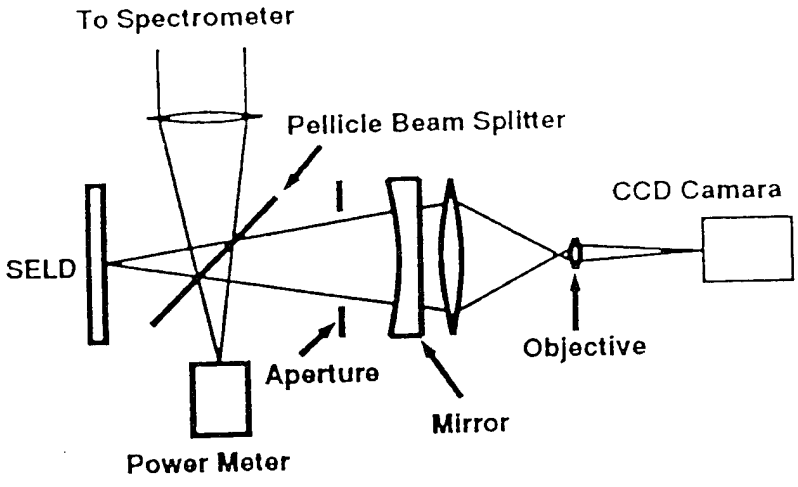
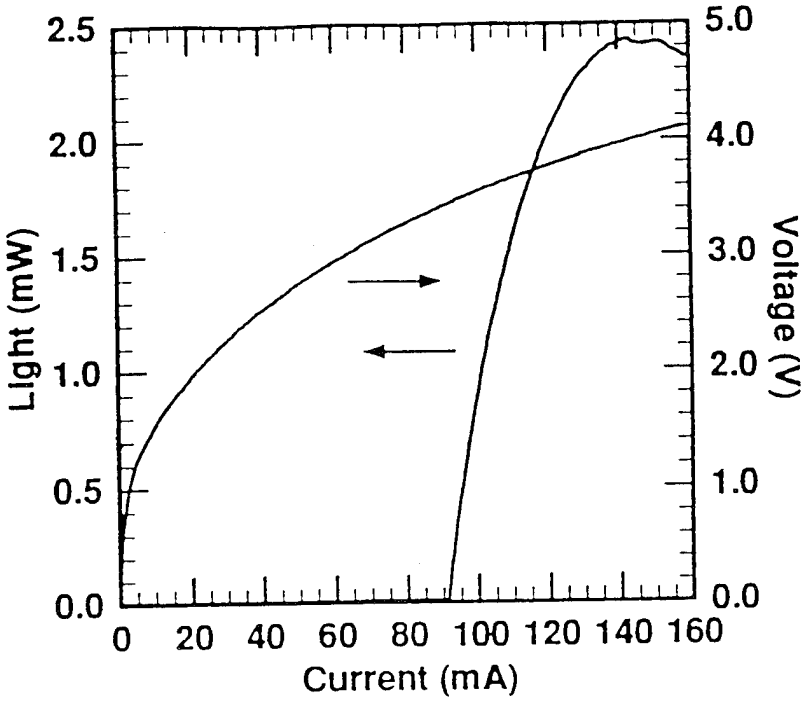


Fig. 1.5.2


2.5
2.0
1.5
1.0
0.5
0.0
Light (mW)
5.0
4.0
3.0
2.0
1.0
0.0
Voltage (V)
0 20 40 60 80 100 120 140 160
Current (mA)

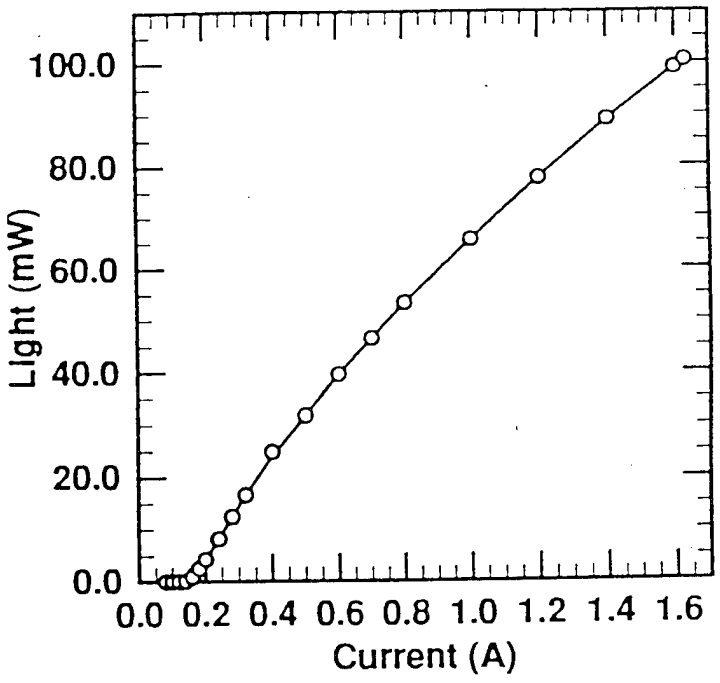

100.0
80.0
60.0
40.0
20.0
0.0
Light (mW)
0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6
Current (A)

Fig. 1.5.3

ers of over 100mW (fig.1.5.3b) with the cavity length set to slightly shorter than focal length (stable resonator) and the aperture closed down. The limit in pulsed power comes from the voltage source, not from the device.

We have also achieved similar results with a flat mirror placed < 100 μm from the diode. This configuration lends itself to integration.

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1.6 Thermal dependence of the refractive index of GaAs and A1As measured using semiconductor multilayer optical cavities

The longitudinal optical mode shift with temperature was measured in two vertical cavity surface- emitting laser (VCSEL) type optical resonators with different GaAs and A1As layer structures. The measurements show distinct differences in the behavior of the cavities. From the data the thermal dependences of the indices of refraction of GaAs and A1As for wavelengths near 1μm were determined to be $(2.67 \pm 0.07) \times 10^{-4}/°C$ and $(1.43 \pm 0.07\ \ 10^{-4}/°C$,respectively.

Vertical cavity surface-emitting lasers (VCSELs) have been widely touted for their potential applications in two dimensional arrays. By far the most common semiconductor material used for the fabrication of VCSELs is the A1GaAs system because of the large

refractive index difference between the lattice matched GaAs and AlAs binaries. The thermal characteristics of these devices are particularly important and have been addressed in some detail. The work covered in this section demonstrates that VCSEL-type passive optical cavities composed of different longitudinal optical mode shifts with temperature. From these shifts the thermal dependence of the index of refraction of GaAs and AlAs can be obtained for the wavelength and temperature range commonly used for VCSEL operation. Since there are no exposed AlAs layers in the structures, this method allows one to handle samples and to perform and repeat measurements without using a vacuum chamber or special ambient to prevent oxidation of the AlAs. The technique is not limited to GaAs/AlAs but can be used for other semiconductors or even amorphous dielectrics.

The two optical cavities used in this study were grown using a Varian Gen II molecular beam epitaxy system at a substrate temperature of $600°C$. The structures were designed to have a resonant wavelength of approximately 1 μm because wavelengths near this range are generated by InGaAs/GaAs strained QW lasers for pumping erbium and praseodymium doped fiber amplifiers. The first cavity (sample A) consisted of a central layer of 10λ GaAs surrounded by a top mirror of six $\lambda/4$ pairs of AlAs/GaAs [Fig.1.6.1 (a)]. The second optical cavity (sample B) had a 10λ central layer of AlAs surrounded by a top mirror of 6.5 pairs of GaAs/AlAs and a bottom mirror of 11 pairs of GaAs/AlAs [Fig. 1.6.1 (b)]. Theses cavities were grown with no intentional doping. The FWHMs of the designed resonances are 1.1nm for sample A and 1.0 nm for sample B. Thus the absolute peak of the resonance could be determined to $\pm 1A°$, which was the limit of the experimental apparatus.

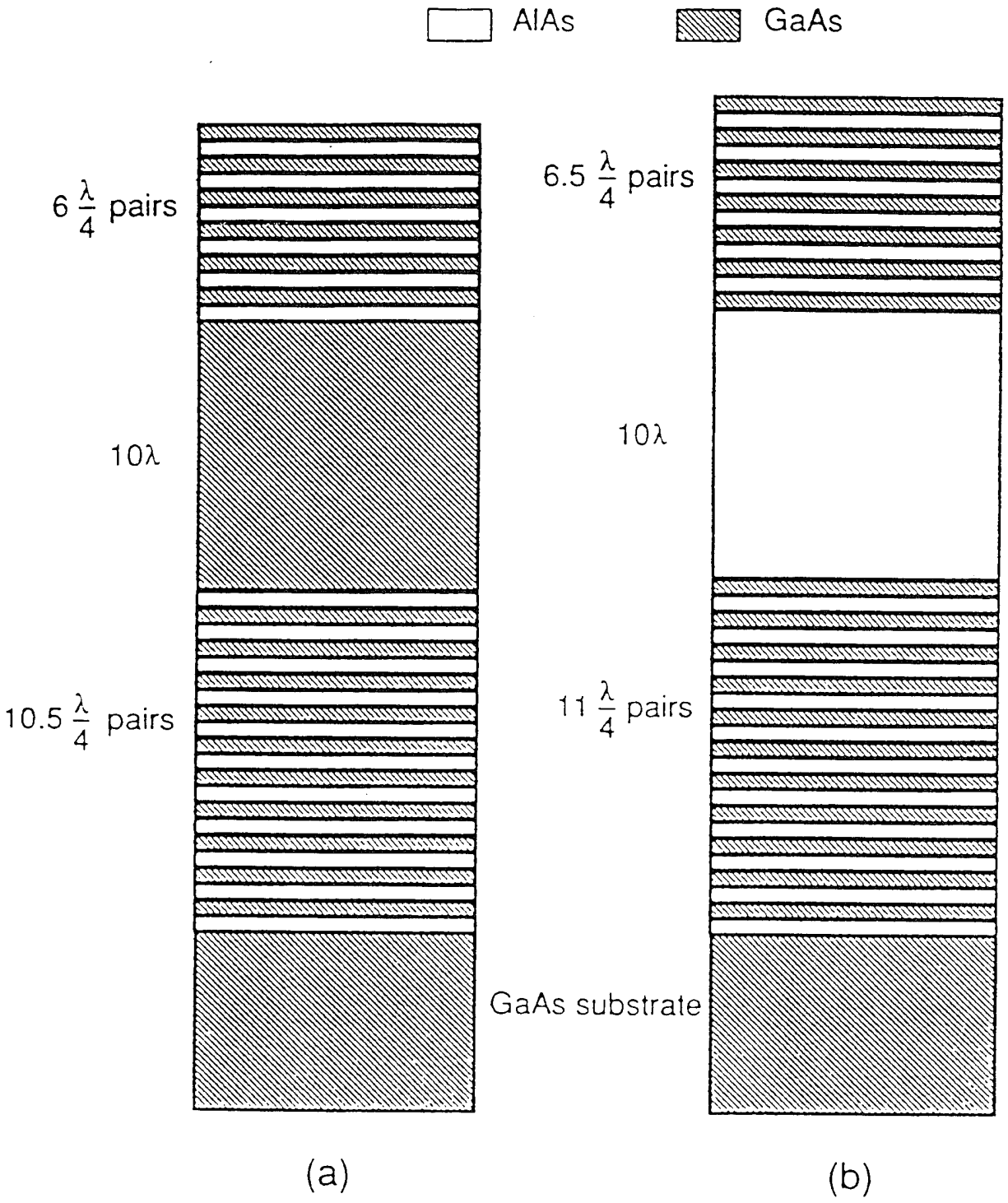
AlAs
GaAs
6 λ/4 pairs
10λ
10.5 λ/4 pairs
(a)
6.5 λ/4 pairs
10λ
11 λ/4 pairs
GaAs substrate
(b)

Fig. 1.6.1

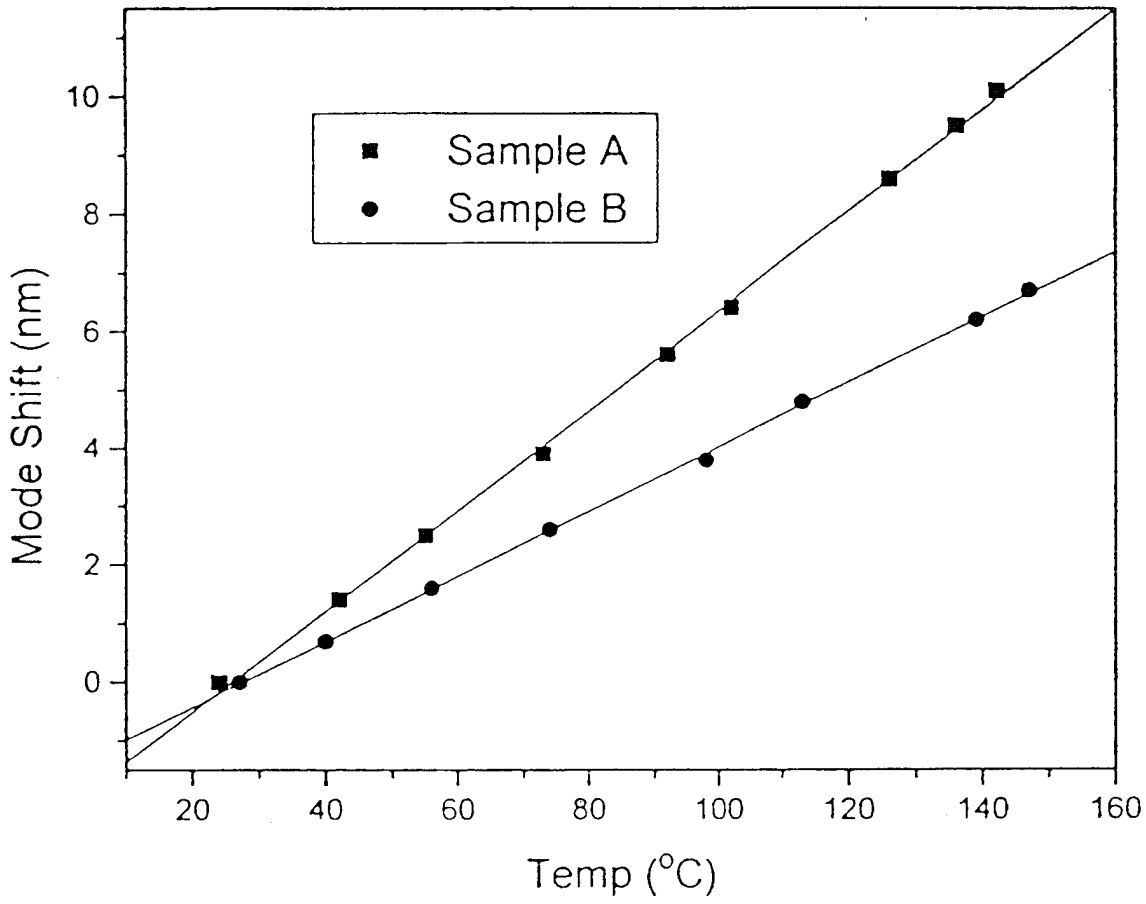
Sample A
Sample B
Mode Shift (nm)
Temp (°C)
0
2
4
6
8
10
20
40
60
80
100
120
140
160

Fig. 1.6.2

The optical mode shifts were determined using a thermally controlled but otherwise standard reflectivity measurement. The samples to be measured were placed on a copper sheet using a thin layer of silver paste. The copper sheet was placed on a hot plate. A surface probe was placed on a dummy sample also attached to the copper to constantly monitor sample temperature during the measurements. Tests showed that the temperature error of this configuration was approximately $\pm 1°C$.

A white light source was incident upon a spectrometer to select light of a single frequency. This monochromatic source was sent through a beam splitter. One half of the beam intensity was chopped and used as a reference beam and the remainder was chopped at a different frequency and focused onto the sample to be tested. The beam reflected from the sample and the reference beam were directed to a silicon detector whose signal was them sent to a lock-in amplifier. The ratio of the signal intensities of the two beams was taken as data.

The data shown in Fig. 1.6.2 were taken by ramping the sample temperatures in variable steps from room temperature to above 140° C. After the temperature stabilized at each step, a reflectivity versus wavelength corresponding to the Fabry-Perot resonance (minimum reflected intensity) was recorder. The mode shift data were determined by a least-squares fit. Structures A and B had mode shifts of 0.86 and 0.56 $A°/°C$, respectively, Since these cavities had long central regions there were actually three Fabry-Perot modes within the DBR stop bands. For example, sample A had modes at 9641, 9974 and 10338 $A°$. All three modes were tested and had the same thermal dependencies within experimental error. The data shown are for the center mode only.

In order to determine dn/dT for GaAs and AlAs from the experimental data, a transmission matrix simulation of both structures was used. Since it is not possible to deconstruct the overall transmission matrix of a structure into relations for n_{GaAs} (T) and n_{AlAs} (T)[4], an indirect approach was necessary. The refractive indices of GaAs and AlAs were taken to vary with temperature using assumed dn/dT's. The simulation program was then run over several temperatures and resulted in a thermal mode shift prediction. This prediction was compared to the experimental data. Corrections to the assumed dn/dT's for GaAs and AlAs were made based on how the predicted mode shifts for samples A and B compared to the measured values. For example, if the predicted mode shift of sample A was very high compared to its experimental value while that of sample B was close to its experimental value, then the assumed dn/dT of GaAs (which composes most of sample A) would be reduced substantially while that of AlAs would be changed only slightly. In this manner it was possible to incrementally approach the proper values for dn/dT of both GaAs and AlAs. Since the structures' resonant wavelengths change with temperature, it was necessary to take into consideration the wavelength dependence of the refractive index $dn/d\lambda$ such that

$$dn = \frac{dn}{d\lambda}\,\Delta\lambda + \frac{dn}{dT}\,\Delta T$$

This was done using the data from Ref. 5

The above simulations resulted in the following values for GaAs and AlAs material in the 9600-10300 A wavelength range and for temperatures between 25 and 150°C

$$\left[\frac{dn}{dT}\right]_{GaAs} = (2.67 \pm 0.07) \times 10^{-4} /°C,$$

$$\left[\frac{dn}{dT}\right]_{AlAs} = (1.43 \pm 0.07) \times 10^{-4} /°C$$

The maximum uncertainty listed comes from the spectral resolution of the resonant wavelength of the optical cavities. In future experiments the cavities could easily be designed for higher Q provided the available spectrometer has spectral resolution better than $\pm 1A°$. These values extend previous determinations of dn/dT for GaAs and $A1A^{6-10}$ to temperature and wavelength ranges common to edge-emitting and surface-emitting lasers with strained InGaAs/GaAs QW active regions.

The large differences in the optical mode shifts with temperature between samples A and B suggest that some control over mode behavior in VCSEL cavities can be obtained by varying the amount of aluminum in the semiconductor mirrors and cladding regions. Experimental data show that dn/dT for GaAs is somewhat higher for photon energies near that of the band gap. This suggests that GaAs/AlAs mirror VCSELs which operate at wavelengths close to the absorption edge of GaAs will have larger differences in dn/dT than those presented here.

To summarize, the thermal dependence of the refractive indices of GaAs and AlAs have been determined for the temperature and wavelength range commonly used in InGaAs/GaAs strained QW VCSELs. The experiment used two different GaAs/AlAs VCSEL-

type passive optical cavities in a temperature regulated reflectivity measurement. The large differences obtained for dn/dT between GaAs and AlAs imply that limited control over the lasing wavelength shift with temperature can be obtained in VCSEL structures.

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1.7 Molecular beam epitaxy growth method for vertical-cavity surface-emitting laser resonators based on substrate thermal emission

A molecular beam epitaxy (MBE) growth monitoring method is developed for distributed Bragg reflectors(DBRs) and vertical-cavity surface-emitting laser (VCSEL) resonators. The wavelength of the substrate thermal emission that corresponds to the optical cavity resonant wavelength is selected by a monochrometer and monitored during growth. This method allows VCSEL cavities of arbitrary design wavelength to be grown with a single control program. This report also presents a theoretical model for the technique which is

based on transmission matrices and simple thermal emission properties. Demonstrated reproducibility of the method is well within 1%.

Since its introduction in 1977, research on vertical-cavity surface-emitting lasers (VCSELs) has moved from laboratory demonstrations to determinations of manufacturability. One manufacturing question that remains is what is the best way to monitor the growth of Fabry-Perot cavities used in VCSELs. The resonant wavelengths of the devices need to be as close as possible to the design wavelength and as uniform as possible across the grown wafer.

In molecular beam epitaxy (MBE) systems, growth monitoring based on substrate thermal emission has been shown to provide accurate control for both general growths and VCSEL growths. Thermal emission techniques have the advantage that the monitoring apparatus is uncomplicated since no alignment of external sources is needed. In addition the substrate can be rotated continuously during growth which is necessary to insure uniform thickness across the wafer. However previous methods have relied on optical pyrometers to detect substrate emission. Pyrometers have a fixed response band and thus cannot be tuned to an optimal wavelength where the thermal emission characteristics of a device may be more easily monitored. This report demonstrates an independent thermal emission method for DBRs and VCSEL cavities which uses a monochrometer to select the cavity resonant wavelength of a VCSEL cavity of DBR. In this case, the emission oscillates during growth such that the individual quarter-wavelength($\left[\frac{\lambda}{4}\right]$) layers of the structure will begin and end on a maximum or minimum of the thermal emission intensity. Since computer determination of a maximum or minimum is relatively straightforward, automatic control is simple.

But more importantly, the same control program can be used to grow a given structure at any design wavelength by changing the monochrometer setting. This report also proposes a simple transmission matrix model to simulate the thermal emission of the VCSEL cavity. Accurate growth of passive VCSEL-type optical cavities is demonstrated using the method. The resonant wavelengths of the tested structures are well within 1 nm of design.

In order to model the thermal emission of a growing VCSEL cavity, we begin by considering a radiating body at thermal equilibrium. The absorptivity, a, is defined such that a= 1 for a perfect blackbody and a =0 for a perfect reflector. The reflectivity, r, is defined such that the reverse is true. Assuming that the body is thick enough that there is no transmission through it, then light of a wavelength, λ, incident upon the body must be absorbed or reflected. Written mathematically,

$$a(\lambda) + r(\lambda) = 1.$$

Kirchoff's law and detailed balance state that $a(\lambda) = e(\lambda)$, where e is the emissivity of the radiating body. Thus, the emission can be expressed as

$$e(\lambda) = 1 - r(\lambda).$$

For DBR or VCSEL cavity growths this means that the emission of a structure can be simulated with a standard transmission matrix reflectivity program. In our model the reflectivity of a structure is simulated at its resonant wavelength for every $20A°$ of material that will be grown. These reflectivity numbers are subtracted from one (to give the emission) and plotted as a function of thickness grown (or time grown). Fig. 1.7.1 is an example of this type of plot.

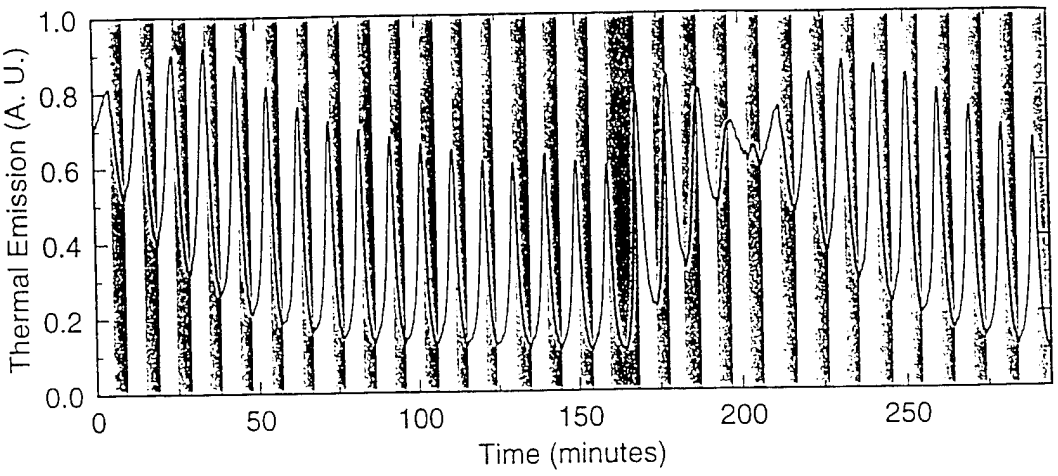

Fig. 1.7.1

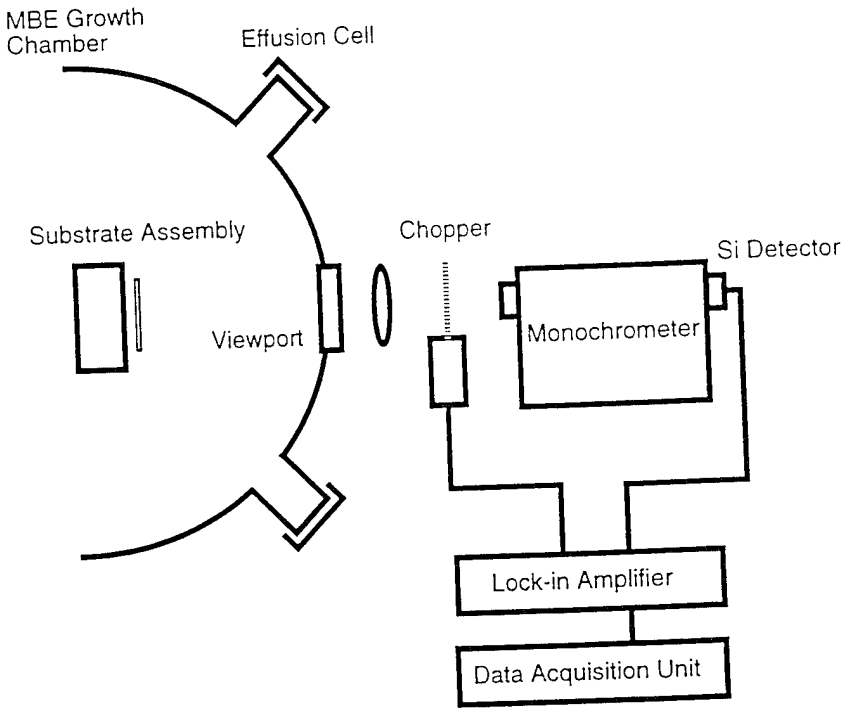

Fig. 1.7.2

At room temperature the relative VCSEL cavity emission, $e(\lambda)= 1- r(\lambda)$, would be extremely small after several DBR pairs had been grown, since a VCSEL mirror is designed to have high reflectivity at its resonant wavelength. However, the wavelengths λ_{gap}, corresponding to the band gap energies of both GaAs and A1As increase much faster with temperature than the cavity resonance, λ_{res}, which changes due to the temperature dependence of the refractive indices. For example, a structure designed for a λ_{res}=980nm at room temperature, will have a λ_{res} at MBE growth temperature $T \sim 600°C$) which is much shorter than λ_{gap} of GaAs at growth temperature. Thus the GaAs will absorb at λ_{res} A1As is still transparent due to its high bandgap. Since $e(\lambda)=a(\lambda)$, GaAs also emits at λ_{res}. If the absorption is high enough so that a clear thermal emission signal can be obtained, but low enough such that light from the first several layers near the surface can be transmitted through the surface with minimal absorption.

The optical cavities which are simulated and grown to test our method have a $17.5 \left[\frac{\lambda}{4}\right]$ pair A1As/GaAs bottom mirror, a $\frac{\lambda}{2}$ GaAs central layer, and a $13 \left[\frac{\lambda}{4}\right]$ pair A1As/GaAs top mirror. Fig. 1.7. 1 shows a simulated plot of the thermal emission during growth for a sample with λ_{res} = 1022nm at a growth temperature of $605°C$. For the following discussion of the plot, we will call the semiconductor to vacuum interface of the growing wafer to be the surface interface. At the beginning of the plot, the emission is that of the GaAs

substrate. The first $\frac{\lambda_{res}}{4}$ layer is A1As. During the growth of this layer, there is constructive interference of emission that has undergone a reflection from the surface interface and emission that has not. After a quarter-wavelength of A1As has been grown, the emission intensity reaches a local maximum so the MBE effusion cell for the A1 is closed and that for the Ga is opened. During the growth of the next quarter-wavelength (GaAS) layer, there is now a decrease in thermal emission intensity. The decrease is due to a destructive interference between emission that has undergone a reflection from the surface interface and emission that has not. The layer grows until a local minimum is reached. At that time the shutter for the Ga cell is closed and the shutter for the A1 is reopened. The oscillatory behavior of the thermal emission is repeated for each mirror pair. The oscillations have a period of half-wavelengths ($\frac{\lambda_{res}}{2}$).

The peaks in the envelope of the thermal emission oscillations increase for the first few mirror pairs and them decrease toward an asymptote until the $\frac{\lambda_{res}}{2}$ central layer. This can be understood by noting that at the peaks of the thermal emission oscillations, the phase shift of reflections from the surface interface and the phase shift of reflections from the growing Bragg mirror are 180 degrees out of phase. This means that the surface interface can be considered as one mirror in a Fabry-Perot cavity and the growing Bragg mirror without the surface interface can be considered as the second mirror. The surface interface has a reflectivity of about 30%. As the growing Bragg mirror increases in reflectivity from zero, the system approaches that of a symmetric and its reflectivity at resonance increases (emission decreases). The asymmetry does not become infinite because the absorption of

the GaAs layers prevents deep mirror pairs from contributing. The decrease in the minimums of the thermal emission envelope simply correspond to the gradually increasing reflectivity of the growing mirror limited by the absorption of the GaAs layers.

At the GaAs central layer, the emission begins to increase after the first quarter-wavelength of material. The oscillation peak is much higher after the full $\frac{\lambda_{res}}{2}$ layer because of the Fabry-Perot cavity effect. The absorbing surface layer is now thicker and thus the reflectivity of the bottom Bragg mirror is reduced towards the 30% of the surface interface. The Fabry-Perot cavity is more symmetric and its reflectivity at λ_{res} is lower (therefore its thermal emission is higher). Note that during the growth of the top mirror, there is an inflection point in the emission intensity, and the interface for the envelope peaks switches from being AlAs/GaAs to being GaAs/AlAs. The reverse is true for the envelope minimums. This inflection point is due to the half-wavelength central layer. Light reflected toward the surface from the layers beneath the central layer is out of phase with light reflected from the layers above the central layer.The inflection point occurs when reflections from the top of the mirror begin to dominate over those from the bottom mirror, In an actual growth, the inflection point must be dealt with be growing the pairs immediately surrounding it on a timed basis.

The fact that the emission of several mirror pairs contributes to the overall thermal signal is extremely beneficial because this behavior averages the phases of the individual interface reflections. Thus small errors in the shuttering times of the MBE sources will not strongly affect the final results of the growth. This phase averaging is analogous to the effects of the thermal motion of a crystal lattice in an x-ray diffraction measurement.

The experimental set-up is shown in Fig. 1.7.2. The thermal emission signal passes through a window in the MBE chamber Although repeated growths cause arsenic rich GaAs to build up on the window, since the window is nominally at room temperature during growth, the GaAs build-up will be transparent to the desired signal wavelength. The thermal signal is chopped and focused onto the slit of a monochrometer. The monochrometer is set at the wavelength to be monitored. A silicon detector detects the light transmitted through the monochrometer, and the electrical signal is sent to a lock-in amplifier whose voltage output is monitored by the MBE control system's data acquisition unit. The signal integration time of the lock-in amplifier is set to a value greater than or equal to the substrate rotation period to eliminate fluctuations in the thermal signal due to the rotation.

The first growth performed was a calibration growth. The monochrometer was set to 1035nm, and the previously described optical cavity was grown at a substrate temperature of $605°C$. At room temperature, the Fabry-Perot resonance of the sample was 997nm. To test the reproducibility of the method, the next growth was designed to have a resonance at room temperature of 984nm. The monochrometer was set to 1022nm, a difference of 13nm from the calibration setting, After growth, the actual resonant wavelength of the cavity at room temperature was 984.6nm, an accuracy of 0.006%. The measured emission plot for his sample is shown in Fig.1.7.3.

To summarize, the use of thermal emission at the optical resonance of a VCSEL type cavity (or DBR) has been demonstrated, Among the advantages of the technique are that the emission may be easily modeled using transmission matrices, growth control is simplified since effusion cell shuttering occurs on the extreme of the emission intensity oscillations and a single control program can be used to grow optical cavities of any design wave

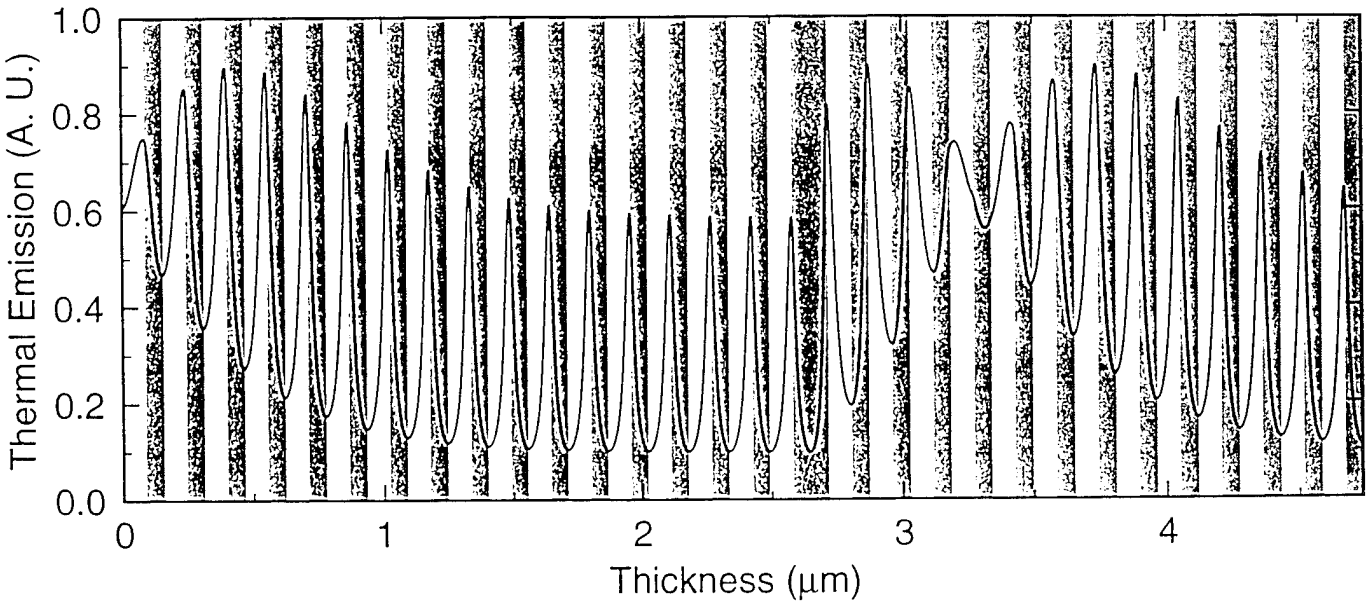

Fig. 1.7.3

length. A description of the real-time thermal emission during actual growths has been outlined. The demonstrated design accuracy of the method for VCSEL-type passive optical cavities is within 0.1%

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2.1 Integration of GaAs vertical cavity surface emitting laser on Si by substrate removal

Substrate removal techniques are attractive for the integration of III-V compound semiconductor devices on Si for the integration optical and electronic devices, and on thermally conducting substrates for heat sinking. Here we discuss the bonding of strained quantum well InGaAs vertical-cavity surface-emitting lasers on both Si and Cu substrates. The GaAs substrates are them removed by selective etching. Lasing was achieved with pulsed electrical pumping with $J_{th} = 2.5\ \mathrm{kA}/cm^2$. The performance characteristics of the Si and Cu bonded devices are compared.

The integration III-V optical devices on Si substrates shows great promise for optoelectronic communications. Work in this field includes heteroepitaxial growth and various bonding techniques. The integration of vertical-cavity surface-emitting lasers(VCSELs)

on Si has significant advantages over edge-emitting lasers for optoelectronic communications. Since the laser beam propagates perpendicular to the plane of the substrate, the geometry and alignment for chip-to-chip communication is much simpler. A two dimensional array of VCSELs can be integrated on Si to increase the number of communication channels. In addition, the chip area occupied by a VCSELs is relatively small compared to an edge emitter, In this letter we describe the successful integration of strained quantum well InGaAs VCSELs on both Si and Cu substrates using a GaAs substrate removal technique. The GaAs VCSEL structure is metallized and bonded to the Si substrate after growth. The GaAs substrate is then removed by selective chemical wet etching. Finally, the bonded GaAs film is metallized on the top(emitting) side and separate lasers are defined.

The VCSEL structure was grown by molecular beam epitaxy (MBE) on a 2 in. n-type (100) oriented GaAs wafer (Fig.2.1.1). Under the n-type Bragg mirrors, a 1 μm AlAs etch-stop layer was grown for the selective GaAs etch. Sixteen pairs of n-type Bragg mirrors were grown, providing 99.3% reflectance when phase matched to air. The active region consists of three 80 nm $In_{0.2}\,Ga_{0.8}$ As strained quantum wells with 100 nm GaAs barriers. Finally, 16 pairs of p-type Bragg mirrors were grown providing for 99.9% reflectance when phase matched to Au. The outer 50 nm of both the n-type and p-type phase matching GaAs layers were "delta" doped to provide ohmic electrical contacts. The wafer was grown at 12 rpm continuous rotation to maximize growth uniformity.

After the growth, the GaAs wafer was metallized with 200 nm of Au to make both the p=typed electrical contact and the bottom mirror. On top of the Au layer, 100nm of Pt was

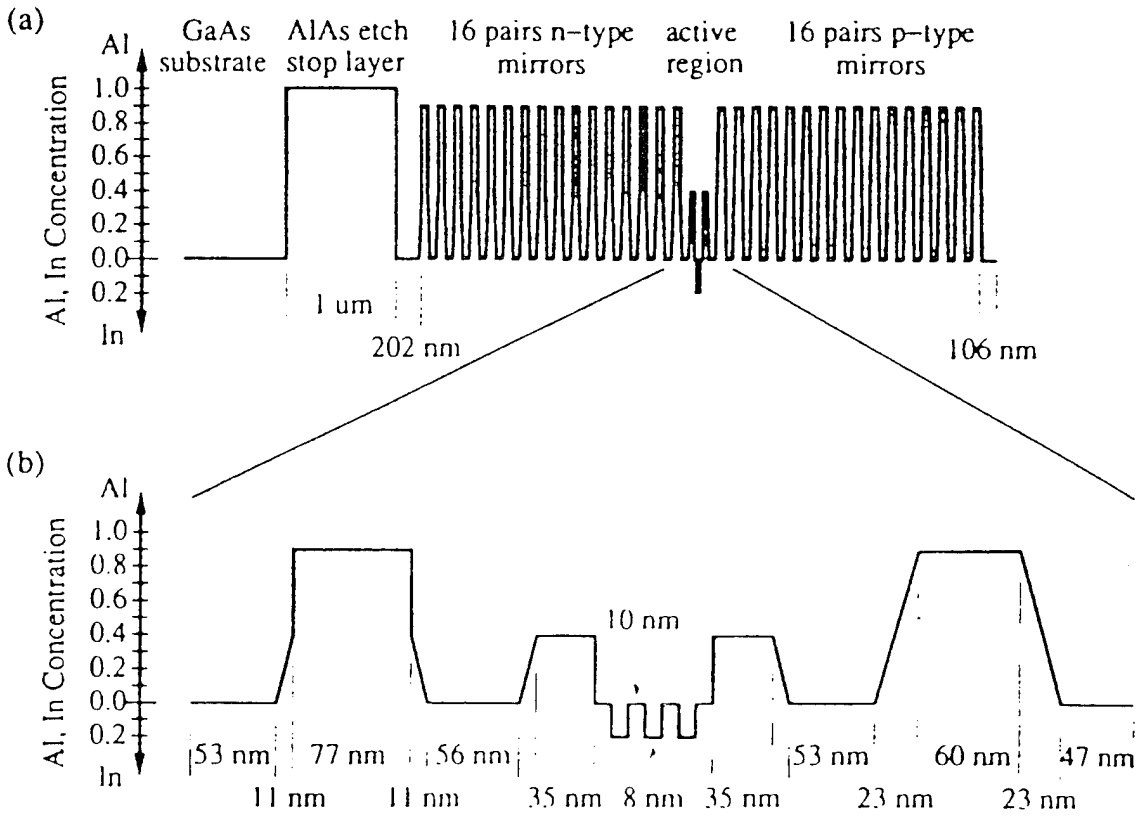
(a)
GaAs substrate
AlAs etch stop layer
16 pairs n–type mirrors
active region
16 pairs p–type mirrors
Al
1.0
0.8
0.6
0.4
0.2
0.0
0.2
In
Al, In Concentration
1 um
202 nm
106 nm
(b)
Al
1.0
0.8
0.6
0.4
0.2
0.0
0.2
In
Al, In Concentration
10 nm
53 nm
77 nm
56 nm
53 nm
60 nm
47 nm
11 nm
11 nm
35 nm
8 nm
35 nm
23 nm
23 nm

Fig. 2.1.1

sputtered. Then a second layer of Au (200nm) was evaporated. The second Au layer was necessary to form the alloy bond with In, and the Pt layer was required to serve as a barrier layer against In forming an alloy with the first Au layer and destroying the mirror.

On a Si wafer, 300 nm of Au and 1.5 μ m on In were evaporated. The Au layer served as an adhesion layer between In and Si. The .5 cm x 0,5 cm piece of the metallized GaAs wafer was placed on the Si samples and heated to 280° C to for, the Ai/In alloy bond. A 36 g weight was placed on top of the samples to exert approximately 1.4×10^5 dyn/cm^2 of pressure during heating.

The GaAs sample was then lapped down to 50 μ m and placed in $NH_4\,OH : H_2\,O_2$ (3:100) etch to selectively remove the remaining GaAs substrate, stopping at the 1 μ m AlAs etch-stop layer. The solution etches approximately 1 μ m/min at room temperature. However, it must be agitated continuously by a magnetic stirring rod or placed in an ultrasonic agitator. Otherwise, extremely nonuniform etching would result. The AlAs etch-stop layer was then removed by a 20 s dip in HF. The edges of the sample and the exposed In were protected by wax during the chemical etching.

Au/AuGe ring contacts were made by lift-off metallization which forms the top n-type contact and lasing aperature. Mesas were then etched down through the active region to profice carrier confinement and index guiding (fig 2.1.2).

Electroluminescence (EL) spectrum collected from a piece of the unbonded GaAs sample shows that the gain peak is located at 1010 nm with a width of 40 nm. Reflectance measurement on the substrate-removed GaAs film indicates that the Fabry-Perot mode is

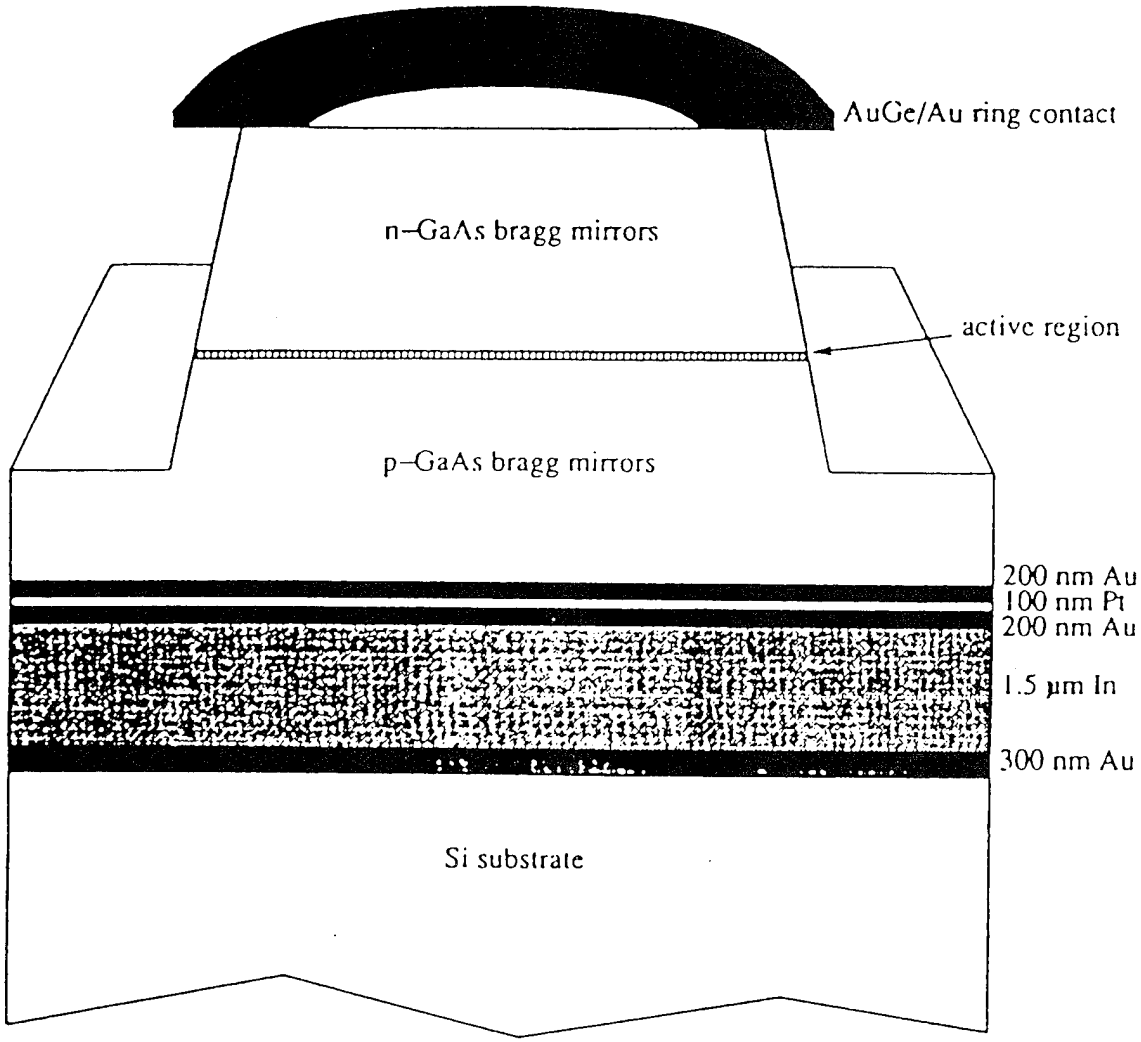
AuGe/Au ring contact
n–GaAs bragg mirrors
active region
p–GaAs bragg mirrors
200 nm Au
100 nm Pt
200 nm Au
1.5 μm In
300 nm Au
Si substrate

Fig. 2.1.2

located at 1014 nm at the center of the wafer. Reflectance measurement taken on a film processed from a part of the wafer located 0.5 cm away from the center shows a shift of the mode corresponding to a 1.4% radial growth variation due to variations in temperature and distance to the sources.

Pulsed operation of a 40μm-diameter laser bonded to Si shows a lasing threshold of I_{th}=80mA(j_{th}=6.5 kA/cm^2) and V_{th}=18.5 V (fig. 2.1.3). The pulse width is 300 ns at a period of 30μs, for a 1% duty cycle. The current-voltage (I-V) characteristics shows that the electrical diode turns on around 13 V. Thus, the additional voltage required to reach threshold was approximately 5 V. SIngle mode operation is obtained for a 10μm-diameter VCSEL bonded to Si.

Various tests were used to determine the cause of the high electrical diode turn-on voltage. it was determined by mesa etching that the high turn-on voltage occurred only after etching into the p=type mirrors. Characterizations of the metal contacts indicates that the high turn-on voltage was due to the p-type mirrors.

The p-type mirrors were designed with 2x10^{18} cm^{-2} Be doping. The high turn-on voltage is suspected to be due to problems that occurred during the molecular beam epitaxy (MBE) growth for example, the Be doping may be lower than expected. The large voltage drop leads to high heat generation in the structure that rapidly red shifts the gain peak away from the Fabry-Perot mode. Thus, very short pulse widths are required to minimize the heat generation, and high threshold currents are required to compete with the shifting gain peak and provide enough gain.

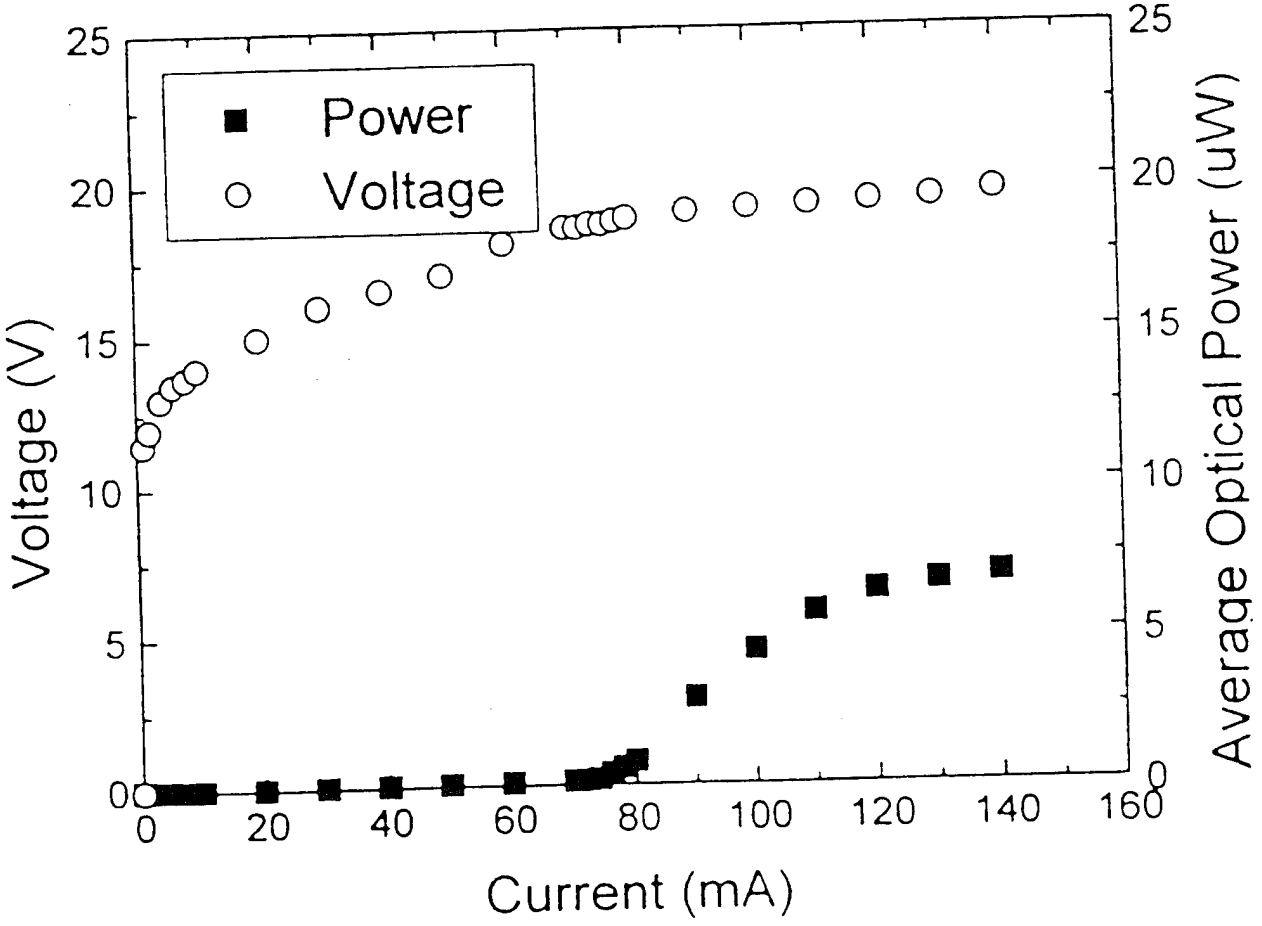
Power
Voltage
Voltage (V)
Average Optical Power (uW)
Current (mA)
0
5
10
15
20
25
0
20
40
60
80
100
120
140
160

Fig. 2.1.3

Pulsed operation of a 40-μm-diameter laser similarly bonded to a 0.5 in.X 0.5in.X0.125 in. Cu substrate indicates a much lower threshold current I_{th}=32 mA (J_{th}=2.5 kA/cm^2) with the same I-V characteristic as the GaAs on Si laser (fig 2.1.4). We were able to operated the Cu bonded laser at 3μs pulse width for a 10% duty cycle. The high thermal conductivity of Cu cools the VCSELs and reduces the amount of red shift in the gain peak. Therefore, the lasers can operated at much longer pulse widths because the generated heat is removed more efficiently. Lower threshold currents are required to operated the lasers due to the smaller red shift in the gain peak.

Because the high turn-on voltage is uniform on all devices fabricated from the same wafer, it is not caused by damage to the active region. Very little damage to the active region is expected to have occurred during the bonding and the substrate removal process. Indium is a very soft material which easily deforms to relieve stress during the bonding process. The active region is protected from the bonding surface and the substrate-removed surface by 2.5μm of p-type and n-type bragg mirrors that absorb possible damage. Work is in progress to grow lasers with better electrical characteristics, and to fabricate large area and high powered VCSELs on Cu and diamond substrates.

In conclusion, we have demonstrated the fabrication of GaAs VCSELs integrated on Si or Cu substrates by GaAs substrate removal. This is the first time a VCSEL had been integrated on a Si substrate with its substrate removed. The performance enhancement of GaAs VCSEls bonded on good thermal conductors(Cu) has also been demonstrated.

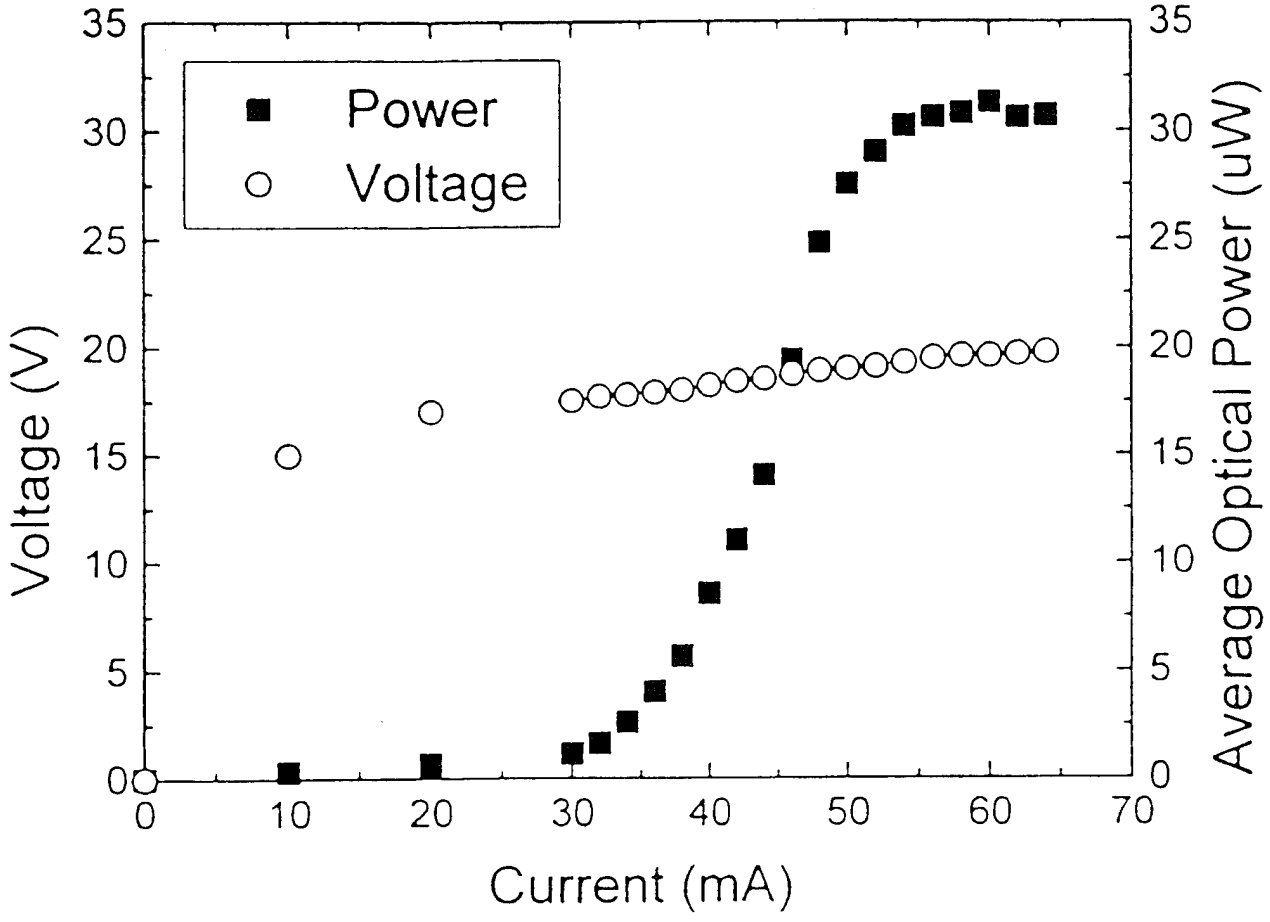
Power
Voltage
Voltage (V)
Average Optical Power (uW)
Current (mA)
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70

Fig. 2.1.4

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2.2 Fluidic Self-Assembly of Silicon Microstructures

2.2.1 Introduction ----- Fluidic self-assembly is a new technique which makes possible the integration of devices fabricated using dissimilar materials and processes. The integration is accomplished by fluidically transporting trapezoidally shaped blocks made of ore material into similarly shaped holes in a receptor substrate. In this report, a systematic study of the FSA integration efficiency is presented. Blocks and holes were formed from silicon using anisotropic etching. Two different sizes were considered: large blocks of dimension 1.0 mm x 1.2mm, and small blocks of dimension 150μm x 150μm. FSA was performed in either water or methanol using a bubble pump apparatus to recirculate blocks. FSA of large blocks resulted in 100% filling of a substrate containing 191 holes within 2.5 minutes. Similar experiments with small blocks and a substrate with a 64 x 64 array of holes yielded a fill ratio of 79% due to undesirable adhesion of blocks to the sub-

strate surface. Roughening the substrate resulted in a fill ratio of 90%. Also presented is a simple rate equation model of the FSA process, along with a discussion of which process parameters are important and how they can be optimized.

2.2.2 Background

The current trend toward an increased degree of functional integration on a single chip, module, or panel presents unique challenges in the areas of fabrication and packaging. A well-known recent example of this is the effort to achieve integration of optical and electronic devices on a single chip. Potentially important examples also lie in the area of multichip module (MCM) packaging and flat panel display(FPD) manufacturing.

The challenges associated with this type of integration derive mainly from the necessity of integrating the sometimes quite dissimilar materials which are best-suited to perform specific functions. For example in the case of optoelectronic integration, electronic devices are best implemented in silicon and optical devices in gallium arsenide. In the case of MCM's the ceramic or plastic package provides thermal isolation and structural support to modules fabricated in silicon. For active matrix liquid crystal FPD's semiconductor pixel drivers must be integrated onto glass substrates.

A variety of approaches to the integration of dissimilar materials have been explored, including heteroepitaxial growth [1], epitaxial liftoff[2], and robotic placement of parts[3]. However, there are limitations associated with each of these techniques. Heteroepitaxial growth onto a lattice mismatched substrate (e.g. GaAs on Si) can result in heavily defected epilayer with poor performance characteristics[1]. A second concern is one of economics: often, only a small area of the epitaxial material is required to make a small number of

devices: the remainder is etched away and hence wasted. Epitaxial liftoff techniques also suffer from this problem. Robotic assembly of parts is only efficient in some applications, when the size of the assembled parts is not too small and their number not too great.

2.2.3 Overview of Fluidic Self-Assembly

Recently, a promising new technique has been used to demonstrate efficient integration of dissimilar materials. This method, called fluidic self-assembly (FSA), involves the placement of devices fabricated onto specifically-shaped structures ("Blocks") of one material into similarly shaped receptacle holes made on a substrate of some other material [4-8]. The blocks are transported to holes by means of a carrier fluid. A schematic representation of the FSA process is shown in Figure 2.2.1. In concept, FSA is able to address many of the concerns described above. Since integration occurs after fabrication, devices can be made on compatible substrates, after which they are cut up into blocks. This results in improved material quality and device performance. In addition the entire substrate of block material can be patterned and cut into device structures. This large number of blocks can then be used to fill a small number of receptor sites on a given substrate, with the excess being stored for future use. Hence, FSA has the potential of being very cost effective.

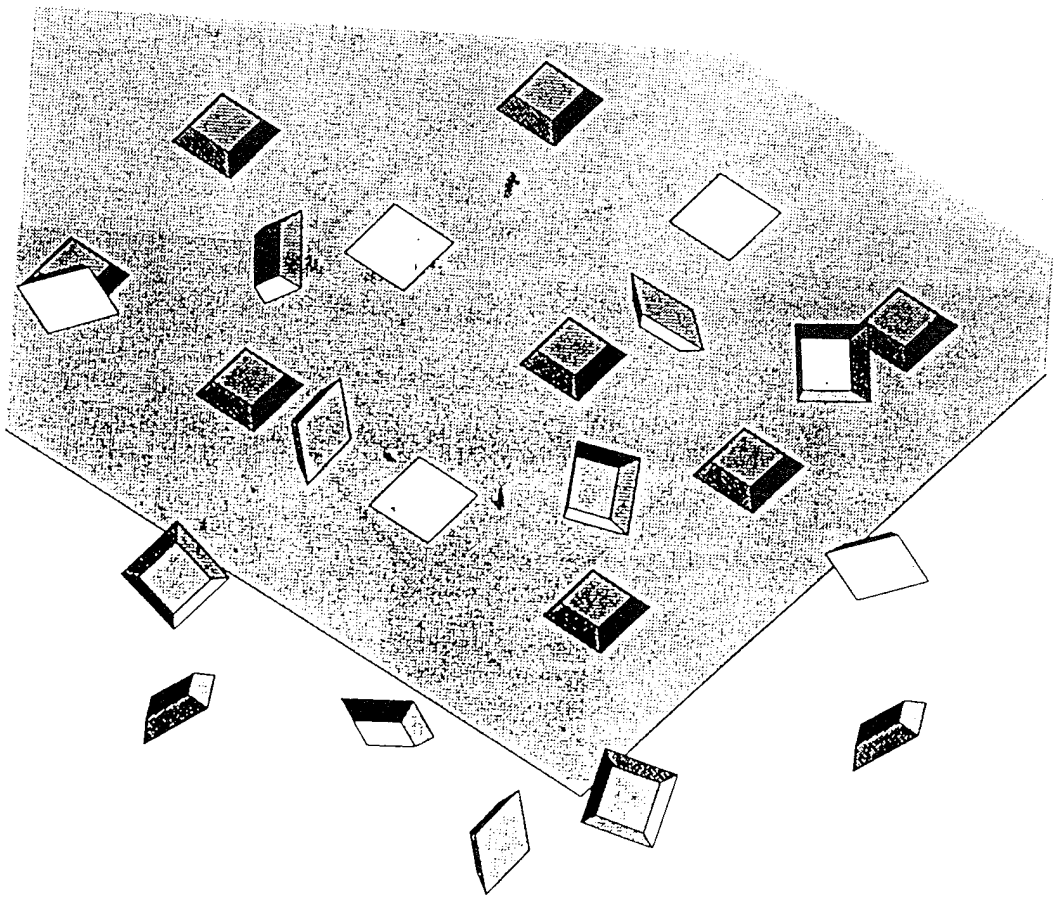

Fig. 2.2.1

FSA has previously been sued to successfully integrate GaAs light-emitting diodes [5], In GaAs photodetectors[6], and resonant tunneling diodes [7] onto silicon substrates. None of these devices can be easily fabricated directly in silicon. The GaAs devices were grown on GaAs substrates using molecular beam epitaxy. (MBE). A sacrificial A1As etch layer was grown first, followed by 10μm thick device layers. The devices were then cut into truncated pyramidal (trapezoidal) structures using photolithography and ion-milling. These structures were then released from their substrate by etching the sacrificial layer with hydrofluoric acid, from which they were transferred into ethanol. With ethanol as the transport fluid, blocks were finally dispersed over a silicon receptor substrate where they were assembled into holes formed by potassium hydroxide (KOH) etching.

The FSA concept can be extended to applications which require the integration of a large number of devices in dense arrays. An example of this would be the integration of single crystal silicon pixel drivers onto a large area glass substrate for FPD applications [8]. An application of this sort requires that practically 100% of the receptor hole array be filled successfully. In order to achieve this kind of efficiency, it is imperative to fully understand the dynamics by which FSA occurs and how the process can be enhanced. In the work presented here, the integration efficiency of trapezoidally-shaped Si blocks into dense hole arrays is systematically studied. For the purpose of simplified processing, the hole arrays were made in Si substrates.

Two different sizes of blocks(holes) were considered: 1mm x 1.2mm x 235 μm and 150μm x 150 μm x 35μm, as measured on the large area face. The purpose of this was to determine how the physical forces involved vary with dimension, as well as to evaluate the

utility of FSA for the aforementioned applications. For instance, the larger blocks may correspond in size to individual modules in a MCM package. The smaller blocks, on the other hand, begin to approach the size of an FPD pixel drive transistor. It may also be noted that the small blocks possess 4-fold symmetry while the large blocks possess only 2-fold symmetry.

The blocks were fabricated using anisotropic etching of Si by KOH. The slowest Si etch planes in KOH are the (111) planes, which form the slanted sides of the desired trapezoidal geometry. because(110) planes etch fastest in KOH, perfectly shaped trapezoidal mesas can only be obtained by employing a corner compensation technique first described by Buser, et al.[9]. A section of the mask pattern is shown schematically in Figure 2.2.2. As can be seen from the figure, not all of the Si area can be used to form blocks when using the corner compensation technique, the maximum being 50%. In order to obtain perfect mesas, the width of the compensation "streets" must be twice that of the mesa height. This in turn limits the dimensions of the top (small -area) and bottom (large-area) faces of the blocks to minimum values of $2\sqrt{2}d$ and $3\sqrt{2}d$, respectively. The large blocks in this experiment were made 0.2mm larger than the minimum bottom face dimension in one direction, while the smaller blocks are of minimum size.

The large blocks were fabricated using a 235μ m thick Si wafer with a single side polished. A 3000 A thick silicon nitride (Si_xN_x) mask layer was deposited on both sides of the wafer using CVD. The Si_xN_x on the polished side was then patterned with a mask similar to that shown in figure 2.2.2, and plasma etched using SF_6. After photoresist removal with an oxygen plasma, the substrate was placed into a 2:1 (by weight) water/KOH bath at

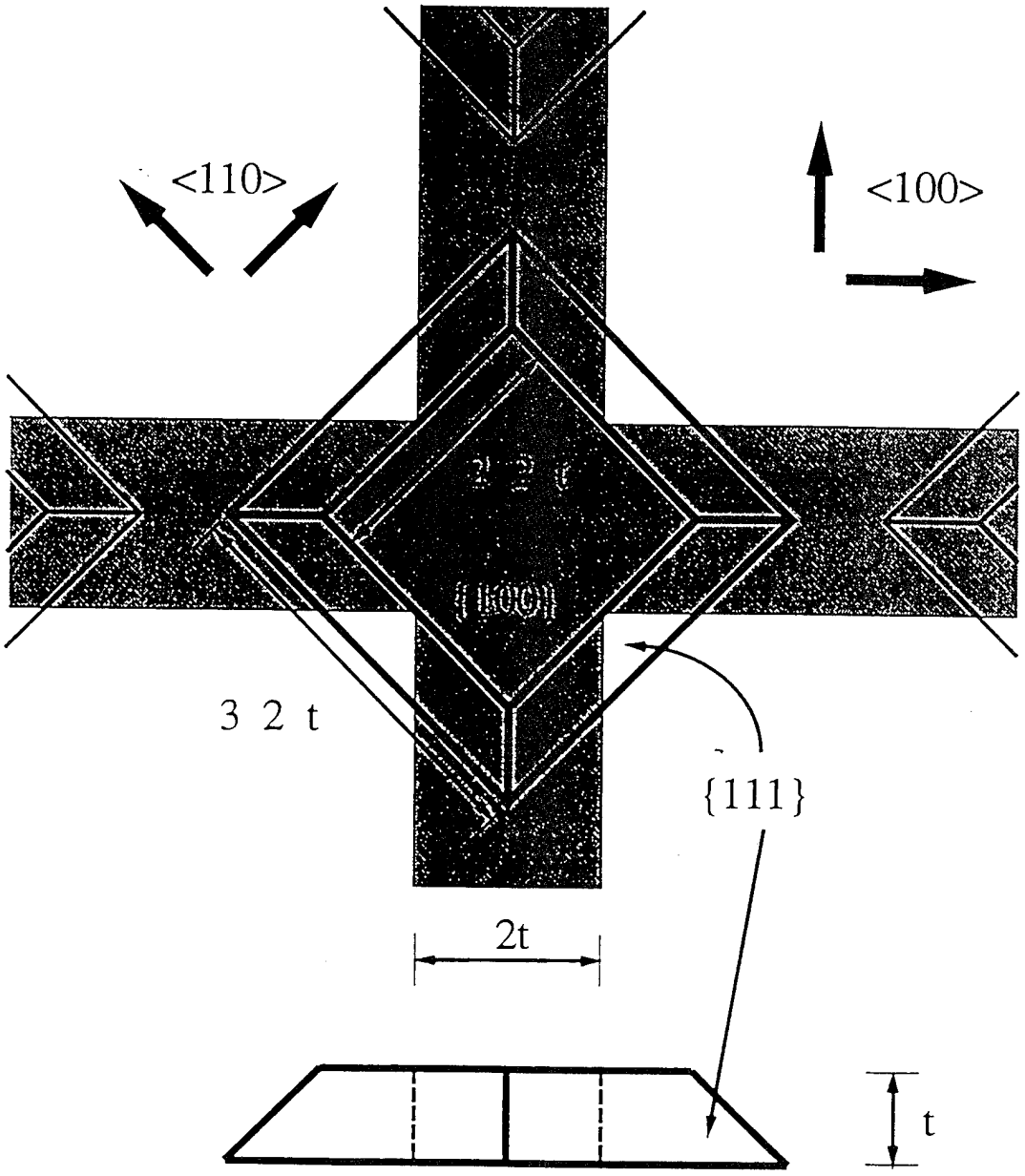

Fig. 2.2.2

80° C and etched all the way through to form trapezoidal blocks. Finally, the overlying SiN_x was etched away in concentrated HF, thereby releasing the blocks. The HF was carefully poured off and replaced with water, in which the blocks were stored.

For smaller block sizes, it becomes more difficult to handle extremely thin wafers. In this experiment, this difficulty was overcome by fabricating the small blocks out of silicon-on-insulator (SOI) wafers. These wafers consisted of a thick Si substrate covered by 4000 A of silicon dioxide (SiO_2) and 35 μm of Si. All processing steps were similar to those used for the large blocks, A photograph of the substrate just before the release step is shown in Figure 2.2.3. During the release step, the HF solution first etched the SiO_2 layer which lies below the blocks and then the SiN_x masking material. the small blocks were found to float in water, and hence were stored in methanol, in which they precipitated to the bottom.

In order to simplify the processing steps of making receptor holes, they were also fabricated on Si substrates, again using SiN_x masking and KOH etching. In this case the mask opening defined the large top dimension of the hole, which was the same as the large dimension of the block meant to fill it. The holes were etched to a depth corresponding to the thickness of the block. Because both the blocks and holes were formed using KOH etching of Si, the fit between them should be very precise. The SiN_x masking layer was not removed from any of the hole substrates used in this experiment.

The pattern of large holes used in these experiments is shown in Figure 2.2.4. it consists of 191 holes arranged in both sparse and dense arrays, and in a variety of orientations. Again,

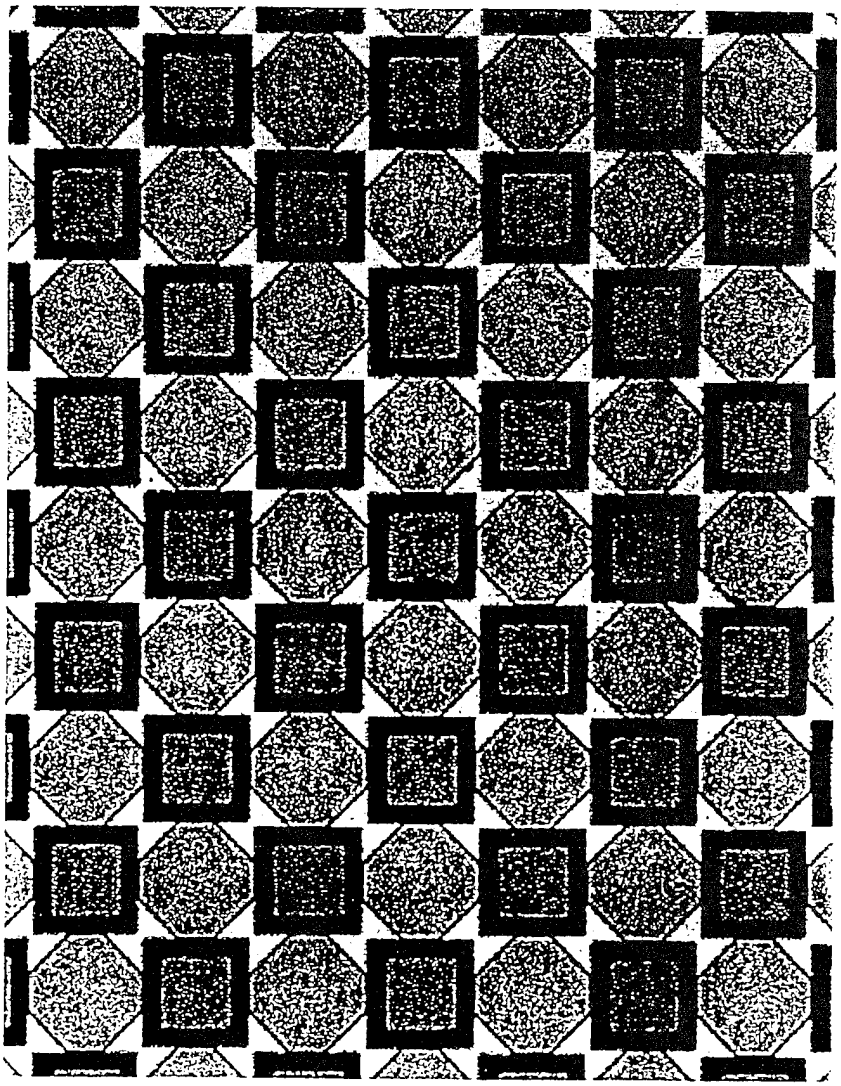

Fig. 2.2.3

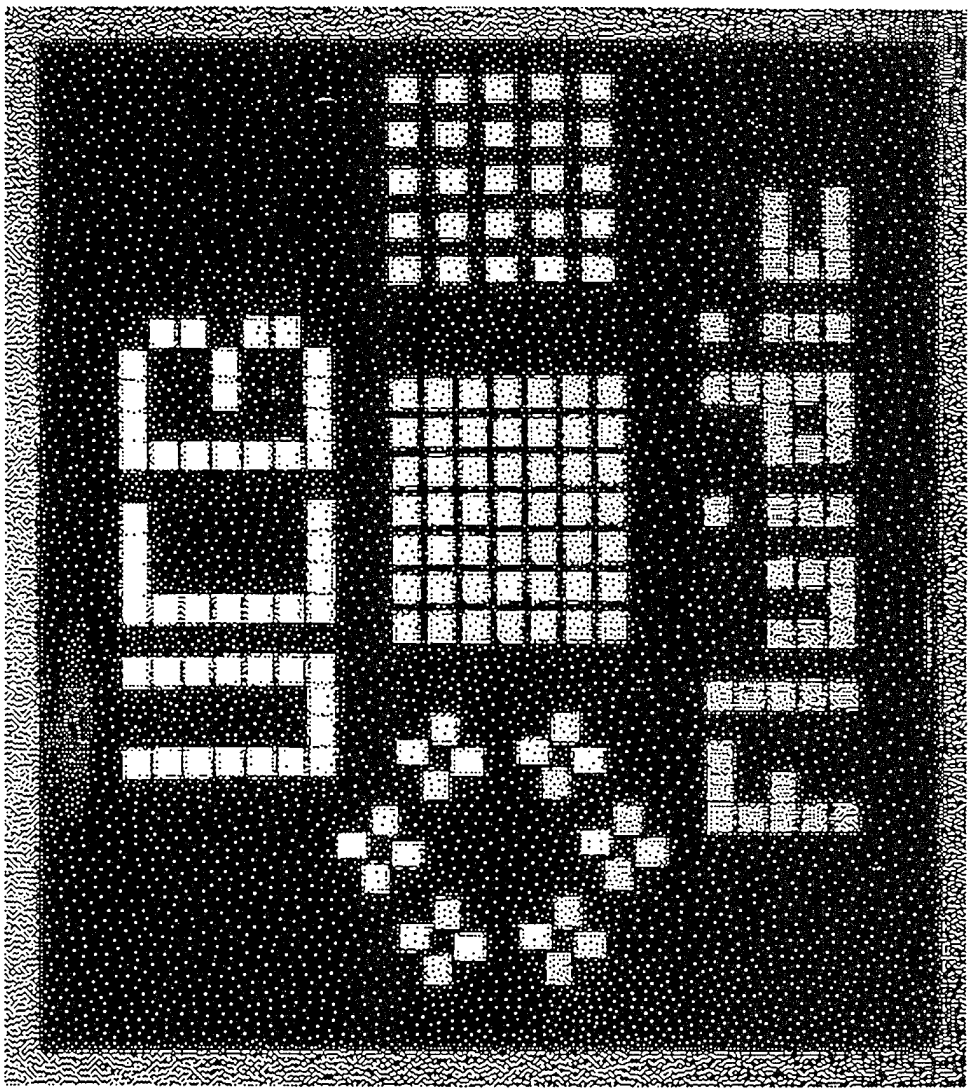

Fig. 2.2.4

such an arrangement may be typical of those found in MCM applications. For the small hole pattern, a 64 x 64 array with holes spaced 300 μm apart (area density = 1/9), was used. This pattern approximates the condition which would exist in the FPD driver application described above.

2.2.4 ASSEMBLY PROCESS

The key to the efficiency of the FSA technique lies in the assembly process itself. There are several factors which will affect how successfully blocks can be made to fill holes. One important variable, of course, is the number of blocks involved in the process. Empirically, it seems reasonable that the greater the number of blocks, the greater the fill ratio. Hence, a large number of blocks of each size were fabricated for this experiment: approximately 500 large blocks and 30,000 small blocks.

A second important factor is the liquid used to perform the fluidic transport. The liquid, if chosen appropriately, can play a role in reducing forces between solid objects, resulting in better block mobility across the surface of the substrate. Also important is the viscosity of the liquid, which can affect how blocks fall through it on their way to the substrate. The most straight forward choice of transport liquid is water. However, Si is hydrophobic, resulting in a tendency of blocks to float on the surface of water. This effect was not significant in the case of the large blocks which, because of their large mass, were observed to precipitate through the water. For this reason water was used to perform FSA experiments on the large blocks. The above effect was much more pronounced, however, for small blocks. Consequently, methanol, to which Si is not phobic, was used to perform FSA on these blocks.

Finally, it is clear that, under even the most ideal conditions not all blocks are able to fill a hole during a single pass across the substrate surface. moreover, not all of the holes in a substrate pattern are filled by a single pass of blocks over it. The efficiency of the process would therefore be greatly enhanced by continually recirculating blocks which have not filled a hole during a given pass. In our experiments, this was accomplished by using the "bubble pump" apparatus shown in Figure 2.2.5. The principle of operation of this apparatus is quite simple: nitrogen gas bubbles are introduced into the column on the right of the figure, causing an upward fluid flow which carries blocks collected at the bottom of the apparatus back up to the top. The rate of recirculation can be controlled by the nitrogen pressure. Each successive pass of blocks across the substrate surface is expected to increase the percentage of filled holes.

2.2.5 RESULTS

FSA experiments were conducted by placing a receptor substrate beneath the output spout near the top of the large the bubble pump, as shown in figure 2.2.5. Blocks were then deposited into the large cylinder and allowed to fall on the substrate surface. Those which did not fill a hole fell down tot the bottom of the cylinder, where they were funneled down into the path of the entering nitrogen bubbles. Blocks picked up by the resulting fluid flow were recirculated to the top starting the process over again.

The first experiments were conducted with approximately 500 large blocks using deionized water as the transport liquid. As the process progressed, it was observed that air bubbles began to attach to the surface of blocks and inside holes. These bubbles appeared to create barriers between block and hole surfaces resulting in reduced filling rates, Their

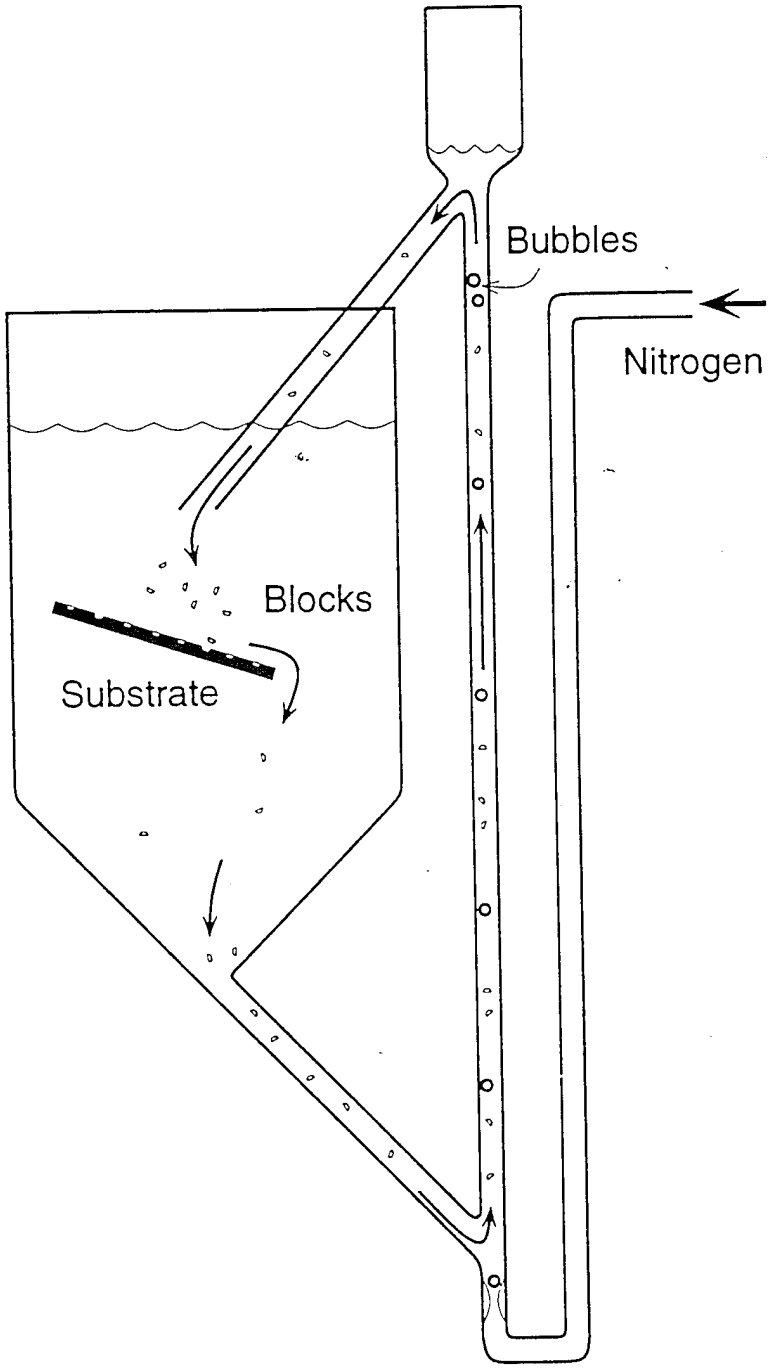

Fig. 2.2.5

presence was also attributed to the hydrophobic nature of Si, which prevented water from wetting Si surfaces. The difficulty was overcome by adding a small amount of alcohol-based surfactant (triton X-100) to the water, This surfactant changed the nature of the solid surfaces from hydrophobic to hydrophilic, resulting in a substantial reduction in bubble attachment.

FSA runs performed in this water/surfactant mixture consistently yielded 100% fill ratios (191/191) within three minutes. Blocks appeared to move very smoothly across the surface of the substrate with very little sticking. It was also observed that as blocks came out of the spout at the top, they always fell in the correct orientation with the small-area face of the trapezoid pointing downward. This parachute effect resulted in most of the blocks being properly oriented upon reaching a hole, Those blocks which did somehow flip over onto their large-area face were swept off the substrate. The results of five FSA runs are given in Table 1. The average time required for 100% filling was 145 seconds, with standard deviation of approximately 15 seconds. A completely filled substrate is shown in Figure 2.2.4.

TABLE 1.

Test No.	1	2	3	4	5
Time(sec)	155	168	125	130	145

Similar experiments were performed using 30,000 of the smaller sized blocks. In this case, methanol was used as the transport liquid. no surfactant was added. After approximately 15 minutes of recirculation, a fill ratio of 70% was achieved. The fill ratio became saturated at this value: an additional 30 minutes resulted in no improvement. During the FSA process, it was observed that many blocks oriented their large-area faces toward the substrate, and then stuck to its smooth flat surface. The result was unassembled blocks on

the surface, which created a physical barrier between incoming blocks and unfilled holes. A photograph of a partially- filled section of the substrate is shown in Figure 2.2.6. the undesirable adhesion of blocks to the substrate surface is clearly visible in the upper left corner of the figure.

Hence, it appears that there exists some type of surface force between the large-area face of the small blocks and the substrate surface, which does not significantly affect the large blocks. It may be recalled that the large blocks were fabricated from a Si wafer with the large-area faces of these blocks came from the unpolished side. The non-adhesion of these faces to the smooth surface of the hole substrate was most likely due to their roughness. The small blocks, on the other hand, were fabricated from a thin Si layer (of an SOI wafer), neither side of which is rough. One may therefore speculate that the sticking of these blocks to the substrate was caused by an adhesion force between smooth surfaces.

If this is indeed the case the adhesion may be reduced by roughening one or both of the surfaces. Since the large face of a block is facing upward when the block is properly placed in a hole, it is likely that there will be devices patterned onto this face for most applications, e.g. drive transistors for FPD's. Theses features will impart some roughness to the large face of the block, which should reduce adhesion. Alternatively, roughening the substrate would produce the same effect, although this is not acceptable for all applications. For simplicity of implementation in the present experiment, the small-hole receptor substrate was roughened to test the above hypothesis. This was done by first etching away the $Si N_x$ and then simply lapping the Si surface using $0.5 \mu m$ grit aluminum oxide pow

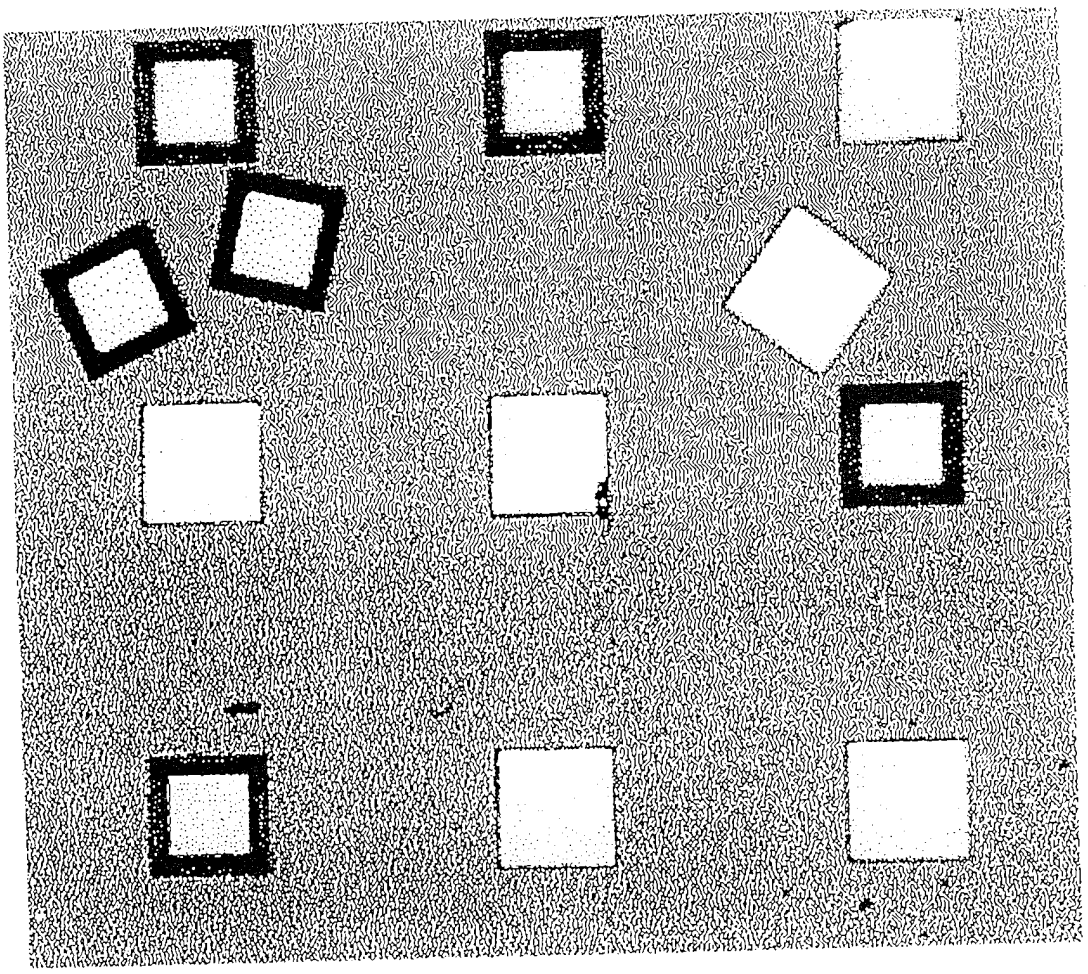

Fig. 2.2.6

der. This step left behind surface features of between 0.5 and 0.8 μm in height. A final cleaning in HF removed any excess powder from the surface and inside the holes.

The FSA experiment was now repeated with this lapped substrate. Sticking between blocks and the substrate was greatly reduced, resulting in better block mobility. The fill ratio reached 90% after 15 minutes, where it saturated. This clear improvement from the previous result indicates that surface adhesion between smooth surfaces is a primary consideration in FSA efficiency. However, the fact that the fill ratio once again saturated indicates that there are other factors involved. Observation of the substrate after further attempts showed that the same holes remained unfilled. Hence, there may have been some characteristic of these holes or their local environment, such as particle debris or nonuniformities, which prevented blocks from either reaching the holes or remaining stable once filled.

2.2.6 Theory and Discussion

In order to gain insight into the FSA process and how it can be improved, it is beneficial to quantify it. The process can be modeled on several different levels. In this section we first present a first-order model based on rate equation principles. This is followed by a more detailed discussion of the process parameters which affect yield, and ways in which this yield can be improved.

In order to apply a rate equation model, we begin by defining variables, The number of filled sites on the substrate is given by f. The total number of blocks and the number of blocks left in solution are given by N_b and n_b, respectively, with $N_b = n_b$ + f. Similarly,

the total number of holes and the number of empty holes are given by N_h and n_h, respectively, with $N_h = n_h + f$.

Phenomenologically, it is reasonable to assume that the filling rate R_1 is proportional to both the number of blocks left in solution and the number of available empty holes, whereas the emptying rate R_2 is proportional to only the number of filled holes. These assumptions can be stated mathematically as: $R_1 = C_1 n_b n_h$

$$R_2 = C_2 f$$

where C_1 and C_2 are proportionality constants. The net rate of filling at steady state is zero, which gives the equality $C_1 n_b n_h = C_2 f$

Substituting $n_h = N_h - f$ and rearranging, we obtain

$$\frac{x}{1-x} = \frac{C_1}{C_2} n_b = K n_b$$

where $x = \frac{f}{N_h}$ is the fill ratio and $K \equiv \frac{C_1}{C_2}$. This equation can be rearranged to give an expression for the fill ratio at steady state:

$$x = \frac{K n_b}{1 + K n_b}.$$

The above analysis clearly oversimplifies the problem by assuming linearity over the entire filling regime. There are, in fact, many complex effects lumped into C_1 and C_2,

which makes the process quite nonlinear. Nonetheless, the above equation is valuable because it quantifies many of the assumptions made previously about how to increase FSA efficiency. First, it can be seen that x approaches 1 as n_b becomes large, i.e. a large number of blocks in solution enhances the filling efficiency. The fill ratio also approaches 1 as K becomes very large. K can be maximized by making C_1 very large and/or making C_2 very small. C_1 is proportional to the probability that a single block goes into a single hole. Ways in which this might be accomplished include minimizing obstructed holes and improving block mobility. Hence, in the context of the model, roughening the substrate in effect causes C_1 to become larger. C_2, on the other hand, is proportional to the probability of a single block coming out of a hole. Its value can be reduced by ensuring that filled holes stay filled. Potential approaches to accomplishing this include minimizing turbulent fluid flow and other forces which tend to dislodge blocks, as well as enhancing adhesion between the block and hole surfaces.

The same adhesion force which creates problems when acting between blocks and the substrate surface can be beneficial when it acts between a block and the bottom of a hole. The bottom of the hole should therefore be made as smooth as possible in at least as large as those of the blocks. If the block is too large to fit properly, it will not make physical contact across the entire surface of the hole, resulting in greatly diminished adhesion.

It is quite apparent that this adhesion force between smooth surfaces plays a significant role in the FSA process. Most likely it is associated with a Van der Waals type of interaction. The strength of the Van der Waals attraction between two solid surfaces is known to be dependent upon the dielectric properties of the surfaces relative to each other and to the

transport medium[10]. Hence, it may be possible to improve the fill ratio through the use of appropriate surface coatings on the substrate plane and inside the holes, as well as a more careful choice of transport liquid. Further investigation into the importance of these factors is currently in progress.

2.2.7 CONCLUSION

In summary, we have demonstrated a new integration technique called fluidic self-assembly using two different sizes of trapezoidally-shaped silicon blocks. The efficiency of the process was found to be greatly enhanced through the use of a simple bubble pump to recirculate blocks. In every run, the larger blocks completely filled a substrate pattern (191 holes) within 2.5 minutes. Initial experiments with the smaller blocks, however, resulted in a saturation of the fill ratio at 70% after 15 minutes. This was due to the sticking of blocks to the substrate surface, which obstructed free blocks from unfilled holes. Roughening the substrate by lapping improved the fill ratio to 90%. A simple rate enation model was used to quantify the process and provide insights into improving its efficiency.

The results obtained in these experiments are very encouraging, in that reasonably high fill ratios were achieved without full optimization of process parameters. As more is learned about these factors and the physical forces involved, the fill efficiency will improve even further. This progression, couple with its inherent flexibility and economic advantage, should make FSA an extremely competitive integration technique over a broad range of applications.

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2.3 Integration of Fluidically Self-Assembled Optoelectronic

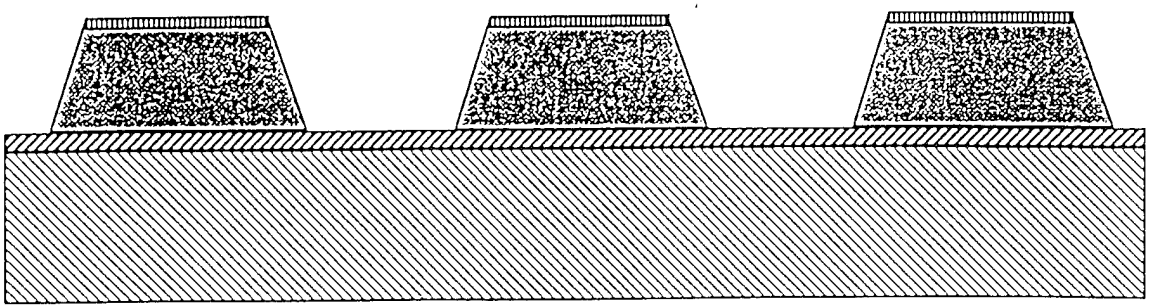
Fluidic self-assembly (FSA) is a technique for efficient wafer-scale placement of large numbers of small or microscopic devices into receptor sites etched in a substrate. This report demonstrates the first complete planar process for integrating optoelectronic devices on a silicon wafer using fluidic self-assembly. Methods for bonding the devices

into the receptor sites and subsequently contacting, planarizing, and interconnecting them are outlined.

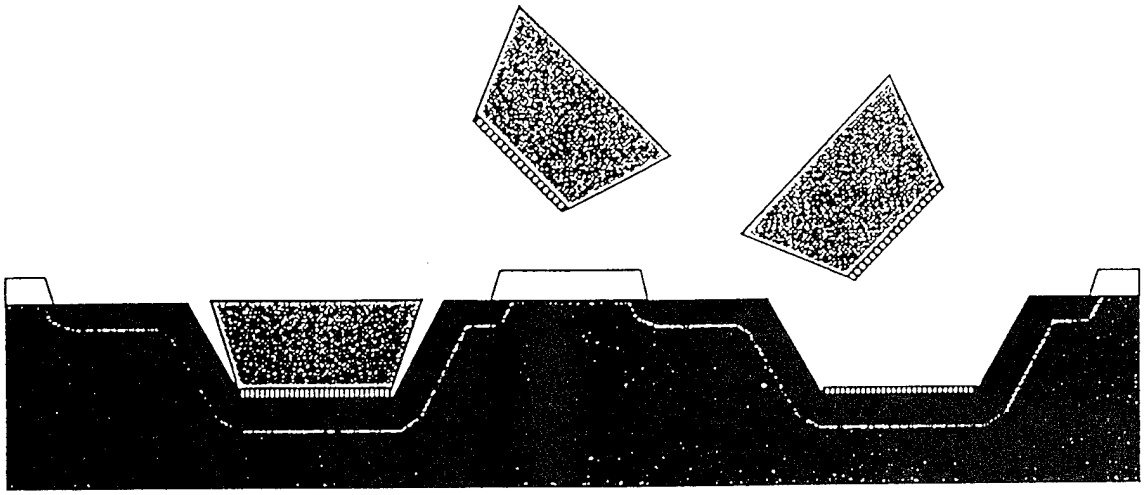
2.3.1 Introduction

Fluidic self-assembly (FSA), is a powerful process for integrating small or microscopic optical devices with different substrates. In this technique (see Fig. 2.3.1) the device units, or "blocks" are shaped to match receptor sites or "holes" that have been etched into the substrate. The blocks are suspended in a carrier liquid which is dispensed over the substrate. The blocks fall towards the receptor sites and with the assistance of fluid flow and acoustic vibration, self-orient into the holes or are removed from the substrate to be recirculated again. Assembly yields of over 90% have been demonstrated for FSA processes. FSA has potential applications to optical links where LEDs or vertical-cavity surface-emitting lasers (VCSELs) must be combined with silicon circuitry. It is also suited to situations where a large number of devices must be dispersed over a large area such as in flat panel displays and solar panels. These latter applications are difficult and expensive to implement using other integration methods such as epitaxial lift-off and micro-robotic assembly.

FSA has an additional advantage over many hybrid optoelectronic assembly techniques in that it can be completely planar. However, the process integration of such devices has many difficulties. In general, the shape of the assembled blocks will not perfectly match that of the holes due to process variations and the different material etching characteristics of the devices and substrates. Thus there will be small gaps around the devices, the depth of which will be on the order of the depth of the hole itself. Also methods of bonding the

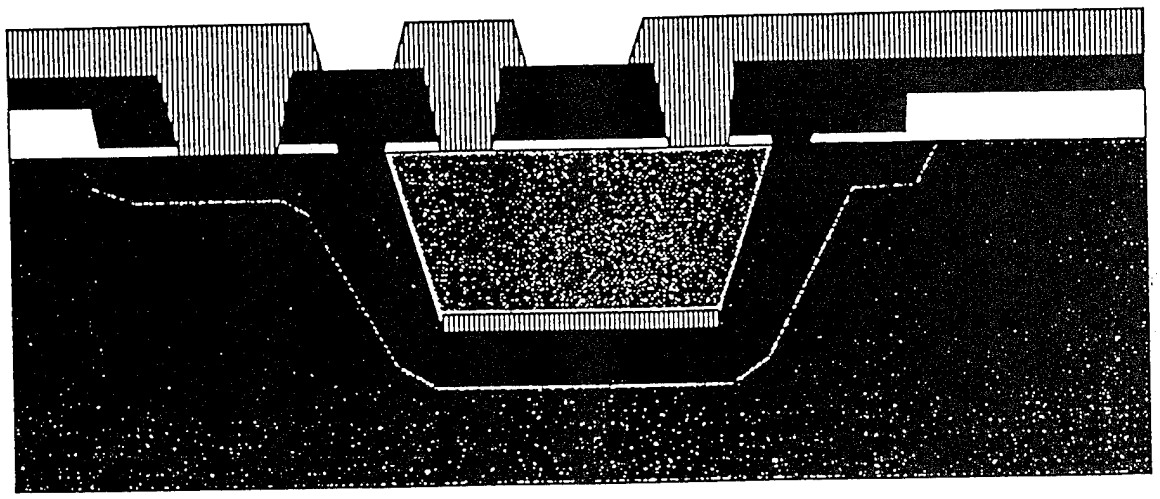


(a)



(b)

Fig. 2.3.1



(c)

GaAs AlAs LED Diffusion

Si Metal SiO_2 Polyimide

Fig. 2.3.1

blocks into the holes for subsequent processing, and methods to contact the bottoms of the blocks are required.

This work reports the first successful process for contacting bonding, planarizing and interconnecting fluidically self-assembled optical devices using standard silicon methods. Visible LEDs are used to describe the process, but other devices are straightforward to implement. Very recently, the first VCSELs integrated using FSA, whose performance will be described elsewhere, were implemented using the process described here.

2.3.2 Block Formation

The devices, or blocks, considered here are visible LEDs grown by molecular beam epitaxy. The growth begins with a 1.5 μm AlAs sacrificial layer. This layer is Be-doped p-type so that the devices can be tested prior to being released from the substrate. A 1000Å Be δ-doped GaAs contact layer is then grown followed by a p-type $Al_{0.3}Ga_{0.6}As$ carrier confinement layer. The active layer is 1000Å of undoped $Al_{0.3}Ga_{0.7}As$. A second $Al_{0.3}Ga_{0.6}As$ confinement layer is grown n-type followed by a 9.5 μm n-type GaAs layer.

After growth, an AuGe/Ni/Au contact is deposited, followed by a 500Å Cr/Ni barrier layer and 4000 A of Au. Using patterned Hoechst-Celanese Az4330 photoresist as a mask, an ion milling step forms the LEDs into trapezoidal blocks. The bocks are freed from the AlAs sacrificial layer in a 10:1 buffered HF (BHF) etch. The etch solution is then diluted with water and replaced with ethanol which serves as the carrier liquid used in the assembly. The dimensions of the blocks are given in Fig. 2.3.1.

2.3.3 Process Integration

The holes are formed on a p-type (100) silicon wafer. Using Si_3N_4 as a mask, a 1.5kg:3liter:1:liter KOH: H_2O :2-propanol etch is performed at 80° C to form approximately 11 μm deep holes with smooth trapezoidal sidewalls. KOH based etches expose the {111} planes of the silicon which are oriented at 54.7° to the (100) surface. This is different from the 65° angle of the ion milled GaAs blocks (Fig. 2.3.1.). Therefore the assembled blocks will have small (2-3 μm) gaps around them which will have to be planarized before interconnects can be made.

After the holes have been etched, the nitride is stripped and a 1 μm LPCVD SiO_2 layer is deposited to served as a diffusion mask. After a photolithography step, the oxide is etched away in selected areas. No special procedures are necessary during photolithography to expose the bottoms of the holes except that the exposure times are increased by about a factor of three. After lithography, phosphorus is diffused into the exposed silicon at 1000° C to form an n+layer as shown in Fig. 2.3.1. This layer serves as a conduction path from the bottom of the hole to the silicon surface. The residual SiO_2 layer which grew over the exposed silicon during the diffusion step is removed. The bulk of the LPCVD oxide is left on the substrate since the blocks will tend to stick to bare silicon during assembly but will be less likely to stick to SiO_2.

Contacting and bonding is accomplished with a 4000A/400A/7000A Al/Cr/Sn metallization in the bottom of the hole. The aluminum layer serves as a contact to silicon. The chromium layer provides a barrier and promotes adhesion of the time during the metal

definition etch. After the assembly procedure, the final metal (tin) will be in physical contact with the gold layer deposited on the bottoms of the blocks (see Fig, 2.3.1(b)). During a subsequent oxide deposition step, the tin is heated to near or above its melting point of 232° C. It diffused into the gold to form an alloy. When the temperature is lowered, the metal solidifies and forms a bond.

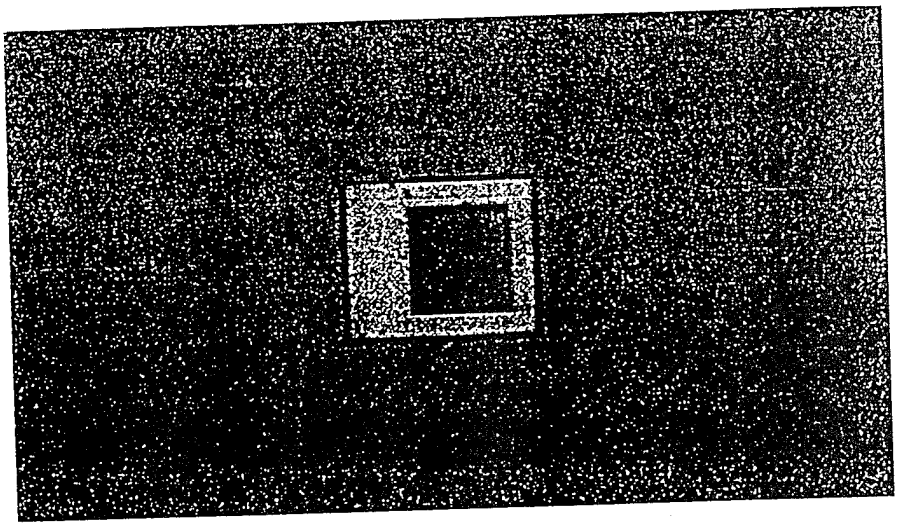
After metal deposition, the bottoms of the holes are masked with Sipley Microposit 1400-31 photoresist. Following 30 second dip in 10:1 H_2O:HC1 to remove he surface oxide layer, the tin is etched in Ashland Aluminum Etchant I. The chromium is removed in a short ion milling step and aluminum etchant removes the bottom aluminum layer. Afterwards, the photoresist is stripped from the substrates and a 300 second anneal at 400° C is performed. Alternately, a sinter can be done in an annealing tube after aluminum deposition, but before subsequent metallization and patterning. However, care must be taken not to create a p-type Al-doped silicon layer during the sinter.

At this point the substrate undergoes FSA. Since assembly yield is not a major concern for demonstrating our process, we use a simple technique, where the ethanol carrier fluid and blocks are merely poured over the substrate. While this method can lead to high local yields (>50% of holes filled), it leads to very low whole wafer yields (typically about 3%). Commercial processes would be more likely to utilize a recirculation scheme using a bubble pump which has led to whole wafer yields of 90% or better. Obtaining higher yields, such as those necessary for flat panel displays will require reductions in the surface interactions that occur during assembly. For example, large blocks (1.2mm x 1.0mm x 235 μm) will routinely fill with 100% yields while small blocks (<150 μm on a side) tend to stick to

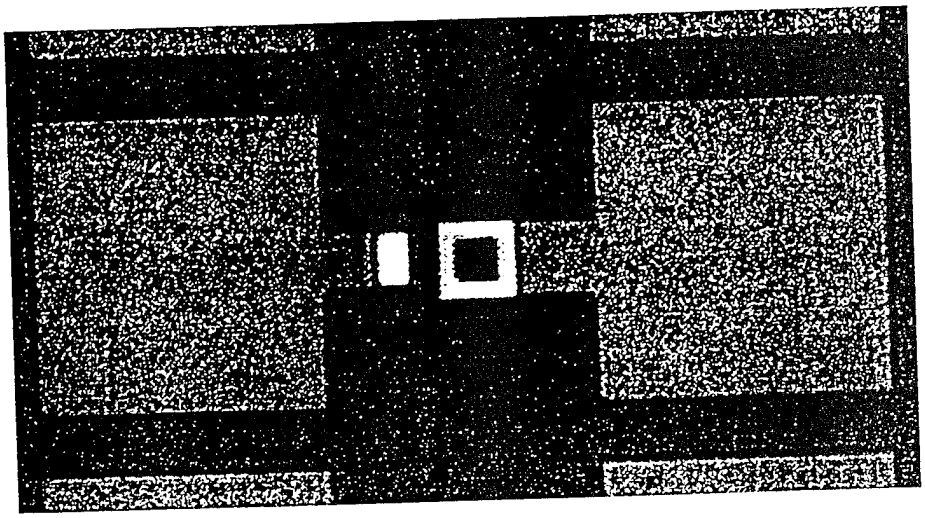
the substrate during FSA. This is due to the smaller mass(volume) of the blocks relative to the surface area exposed to the substrate. The small blocks must be agitated by strong fluid flow or acoustic vibration from a piezoelectric transducer mounted under the substrate, The intensity of the vibration or flow can be set such that improperly placed blocks (e.g. upside-down or misoriented blocks) are knocked out of the holes while properly placed blocks are not. The choice of carrier fluid and surface materials plays an important role as well. As mentioned previously, the GaAs blocks adhere more strongly to a bare silicon surface than they do to an SiO_2 surface. Work to optimize all of these conditions is actively underway.

After assembly (Fig 2.3.2(a)), the ethanol carrier fluid is evaporated in a bake oven at 70° C. A spin-dry or N_2 gas blow-dry cannot be used prior to bonding or the assembled blocks will be agitated and lost. The evaporation dry typically leads to no loss of blocks.

A 2000A PECVD SiO_2 layer is deposited at 300° C over the samples. This will serve as a plasma etch-stop layer in subsequent processing and it is also during the step that the blocks are bonded into place. The presence of the tin layer for bonding is crucial in the next step, in which polymide is spun over the sample. Test substrates which have been metallized with only aluminum in the bottoms of the holes show block-in -hole yield losses of over 70% over a given sample area (usually about 20 blocks). Substrates with the A1/Cr/Sn metallization show no losses. Three polymide spins and softbakes (2 min, at 135° C) are performed, and the polymide is then etched back to about 1.5 μm in a CF_4/O_s plasma. The degree of planarization depends only on the difference between the



(a)



(b)

Fig. 2.3.2

depth of the etched hole and the height of the block and metal layers. This is less than $\pm 1000\AA$ in well matched samples.

After planarization, a $CF_4\ O_s$ plasma etch followed by a 10:1 BHF dip form vias in the shape of a ring over the A1GaAs LED and a square over the n+ region of the silicon. 1.5μm of aluminum is then evaporated and selectively etched to create contacts and test pads. A 300 second anneal is performed at 400° C. The finished process is shown in Fig. 2.3.1(c) and Fig. 2.3.2(b). The turn-on voltage for the LEDs is 1.6V as shown in Fig. 2.3.3. The light emission is red and clearly visible to the unaided eye.

2.3.4 Conclusion

This report has demonstrated the feasibility of integration optoelectronic devices in a silicon-based process using fluidic self-assembly. Methods to isolate devices and provide a conduction path from the contact via to the bottom of the hole that can be accessed from the top side of the wafer have been presented. A low temperature AuSn alloying process was used to bond the devices into their receptor sites. Additionally techniques to planarize and interconnect the self-assembled devices have been outlined.

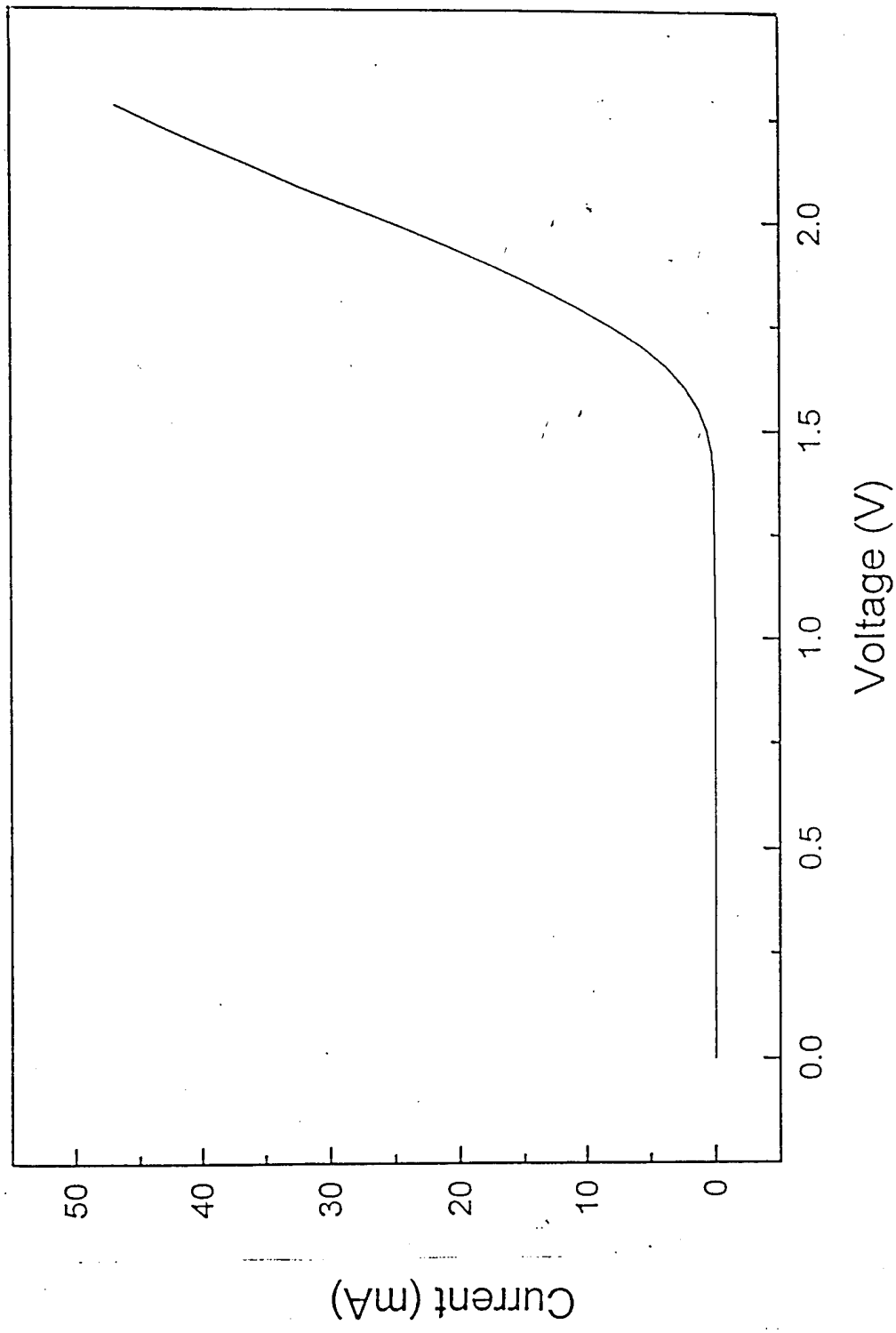


Fig. 2.3.3

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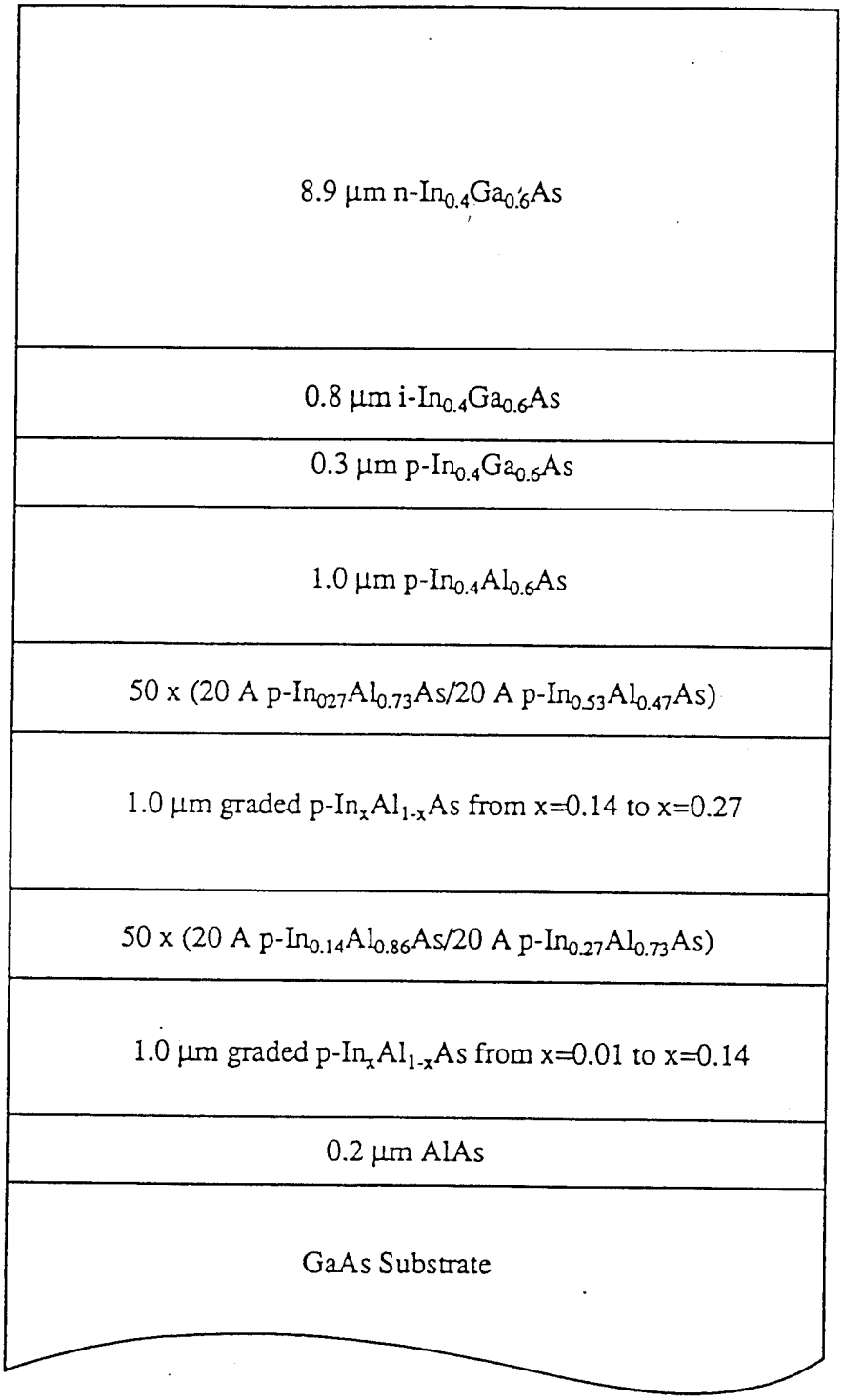
2.4 InGaAs and GaAs p-i-n Photodetectors Integrated onto a Si Substrate by Fluidic Self-Assembly

GaAs on Si has long been seen as a way to integrate GaAs optical devices with established Si electronics. unfortunately, the 4% lattice mismatch and the thermal expansion mismatch lead to high defect densities as well as residual thermal stress when GaAs films are grown heteroepitaxially. To avoid these problems, we developed a novel self-assembly integration technique whereby lifted-off GaAs blocks suspended in liquid are allowed to fall into etched pits on a Si wafer.

A device of interest is the photodetector, because it offers the opportunity to integrate GaAs-based detectors with Si circuitry to fabricate optical receivers. For sensitivity near the minimum dispersion and absorption silica fiber wavelengths, it is desirable to integrate $1.33\mu m$ and $1.55\mu m$ detectors onto Si. Generally, these devices are fabricated on InP substrates with either quaternary inGaAsP or ternary InGaAs layers as the active region of the *pin* diode. One would prefer to use InGaAs because it is much easier to grow than InGaAsP. Also, since GaAs substrate are less expensive and have better material quality, their use is preferred to the use of InP substrates.

In this work, we grew GaAs and InGaAs photodetectors. Fig. 2.4.1 shows the basic photodiode structure. Since InAs and GaAs are lattice-mismatched, strain is induced causing the formation of misfit dislocations. To reduce theses effects, the composition was graded from GaAs to $In_{0.27}Ga_{0.73}$ As over the span $2\mu m$. Strained layer superlattices were placed in the middle and at the end of the graded layer to filter out threading dislocations. The second superlattice had an average In alloy composition of 40% and served as the

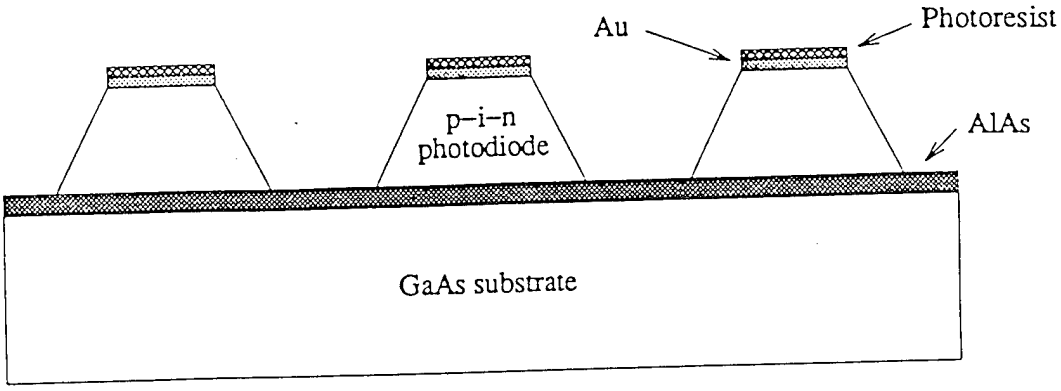

8.9 μm n-$In_{0.4}Ga_{0.6}As$
0.8 μm i-$In_{0.4}Ga_{0.6}As$
0.3 μm p-$In_{0.4}Ga_{0.6}As$
1.0 μm p-$In_{0.4}Al_{0.6}As$
50 x (20 A p-$In_{027}Al_{0.73}As$/20 A p-$In_{0.53}Al_{0.47}As$)
1.0 μm graded p-$In_xAl_{1-x}As$ from x=0.14 to x=0.27
50 x (20 A p-$In_{0.14}Al_{0.86}As$/20 A p-$In_{0.27}Al_{0.73}As$)
1.0 μm graded p-$In_xAl_{1-x}As$ from x=0.01 to x=0.14
0.2 μm AlAs
GaAs Substrate

under-lying substrate for the subsequent $In_{0.4}Ga_{0.6}$ As *pin* photodiode structure. To accommodate our process, the structure was grown on top of a 1.5μm A1As lift-off layer. In addition, the structure was grown to a total thickness of 10μm. For GaAs photodetectors, a GaAs pin structure was grown on top of the A1As lift-off layer. To remove the defect layers from the pin photodetectors, we grew a third structure in which the InGaAs graded layer was replaced by an InA1As graded layer. Since InA1As can be etched selectively, the InA1As graded layer can be used as the sacrificial layer, thereby removing this high defect density layer from the devices.

After growth, the backside contact was metallized and square blocks were formed on the top surface of the wafer (Fig. 2.4.2). The wafer was then bonded face-to-face onto an intermediate substrate using wax, and the GaAs substrate was removed. A second lithography step was used to form top-side ring contacts on the newly exposed surface. Finally, the blocks were freed from the wax and placed in a carrier liquid. The liquid was dispensed over a Si wafer to flow the blocks in the etched holes. 300μm x 100μm devices exhibited photocurrent an the dark currents around 7μ A. The photocurrent to dark current ratio for these devices was around 21.

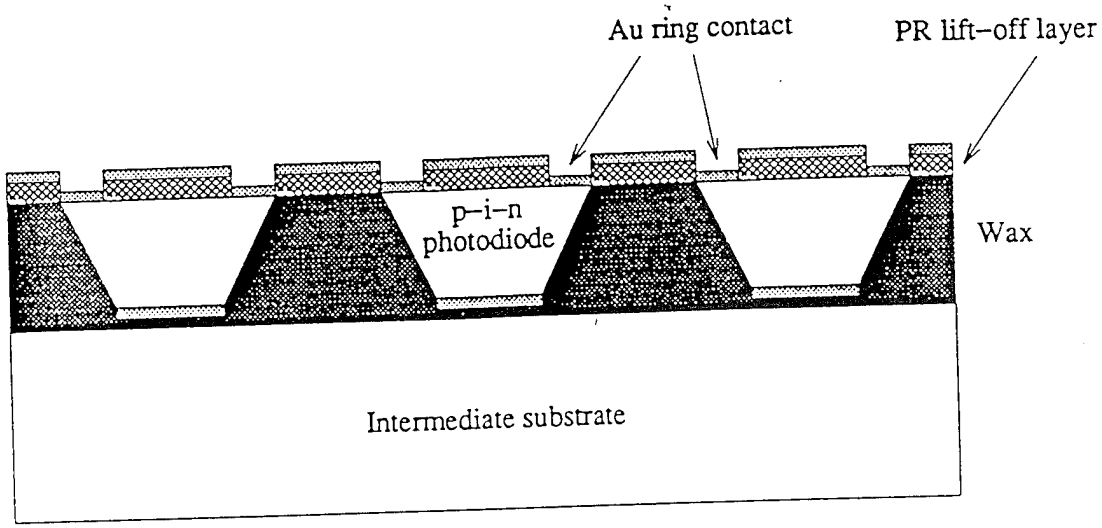
2.5 Fluidic Self-Assembly for the Integration of GaAs Light -Emitting Diodes on Si Substrates

The direct bandgaps of III-V compound semiconductor materials give them many useful optical properties not found in Si. Specifically, optical devices such as light emitting diodes, semiconductor lasers and efficient photodetectors can be made with these material

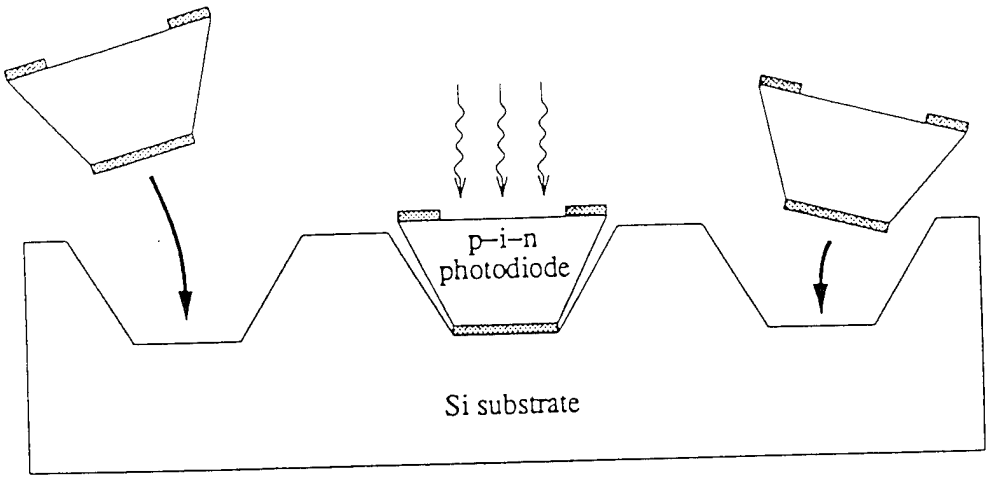


a) Backside lithography is performed, and blocks are formed.

Fig. 2.4.2



b) Wafer is flipped over, and bonded to an intermediate substrate.
Topside lithography and metallization is performed.



c) Blocks are freed from wax, and fluidically self-assembled.

Fig. 2.4.2

systems. The monolithic integration of GaAs optoelectronic devices on Si VSLI is very important for high-bandwidth optical communications.

In this report we demonstrate the quasi-monolithic integration of GaAs light-emitting diodes on Si wafers by a novel technique which utilizers fluid transport and shape differentiation. GaAs light-emitting diodes grown by molecular-beam epitaxy on top of an AlAs stop etch layer are patterned into trapezoidal mesas and freed from the GaAs substrate. Ring contacts are patterned on the top of the blocks for light output. Trapezoidal holes are etched into a Si wafer to act as receptors for the GaAs blocks. The GaAs devices are transferred into a carrier fluid and flowed over the Si wafer to integrate the blocks. The trapezoidal design ensured that the blocks are assembled into the holes in one vertical orientation and four possible azimuthal orientations.

The fluidic self-assembly integration has many advantages over other integration techniques such as heteroepitaxial growth [1]-[3] and wafer bonding [4]-[6]. On the order of one hundred optical emitters are required per Si VLSI chip for optoelectronic communications. However, with techniques such as epitaxial lift-off, the entire GaAs wafer area must be used to fabricate these devices. Since only a small fraction of the wafer area is used much of the expensive grown wafer is wasted.

Fluidic self-assembly allows the fabrication GaAs devices as densely packed as possible on the grown wafer to maximize the wafer area that is made into devices. Approximately 3 million devices can be made from a 2 inch GaAs wafer. The blocks can be dispensed over many Si wafers, because the unused blocks may be recycled. This gives great flexibility to

the integration process because the GaAs devices and Si circuitry can be processed separately prior to self-assembly.

An anisotropic etchant is used to make trapezoidal holes in Si. Ethylenediamine pyrocatechol(EDP) etches selectively with respect to Si crystallographic planes with greater than 100:1 selectivity over the {111} surfaces. The Si {111} planes are inclined 55° from the (100) oriented Si wafer surface. The etched surfaces are optically flat.

Square 24μm x 24μm openings were defined with photolithography on SiO_2 deposited on p-type (100) Si wafers. 10μm deep holes were then etched into the Si substrate using the wet chemical etch with SiO_2 as the mask. The etched holes were trapezoidal with 55° sidewall angles due to the anisotropy of the etch and the base of the holes measured 10 μm x 10μm.

The light-emitting diode structure was grown by molecular-beam epitaxy on a 2 inch n-type 9100) oriented GaAs wafer (Fig. 2.5.1). A 1.0-1.5 μm A1As;as was first grown on the GaAs substrate to act as the etch-stop layer during substrate removal. The A1As was doped n-type to facilitate testing of the light -emitting diodes. The light emitting diode structure consisted of a 100nm n+ GaAs cap layer, a 1μm n+$Al_{0.1}Ga_{0.9}As$ transparent layer, a 1 μm p active region and an 8μm p+ buffer layer. The entire structure had a thickness of 10μm to fill the height of the blocks. The p-n junction which was buried under the thick buffer layer, would be near the top of the integrated blocks in the fluid self-assembly process.

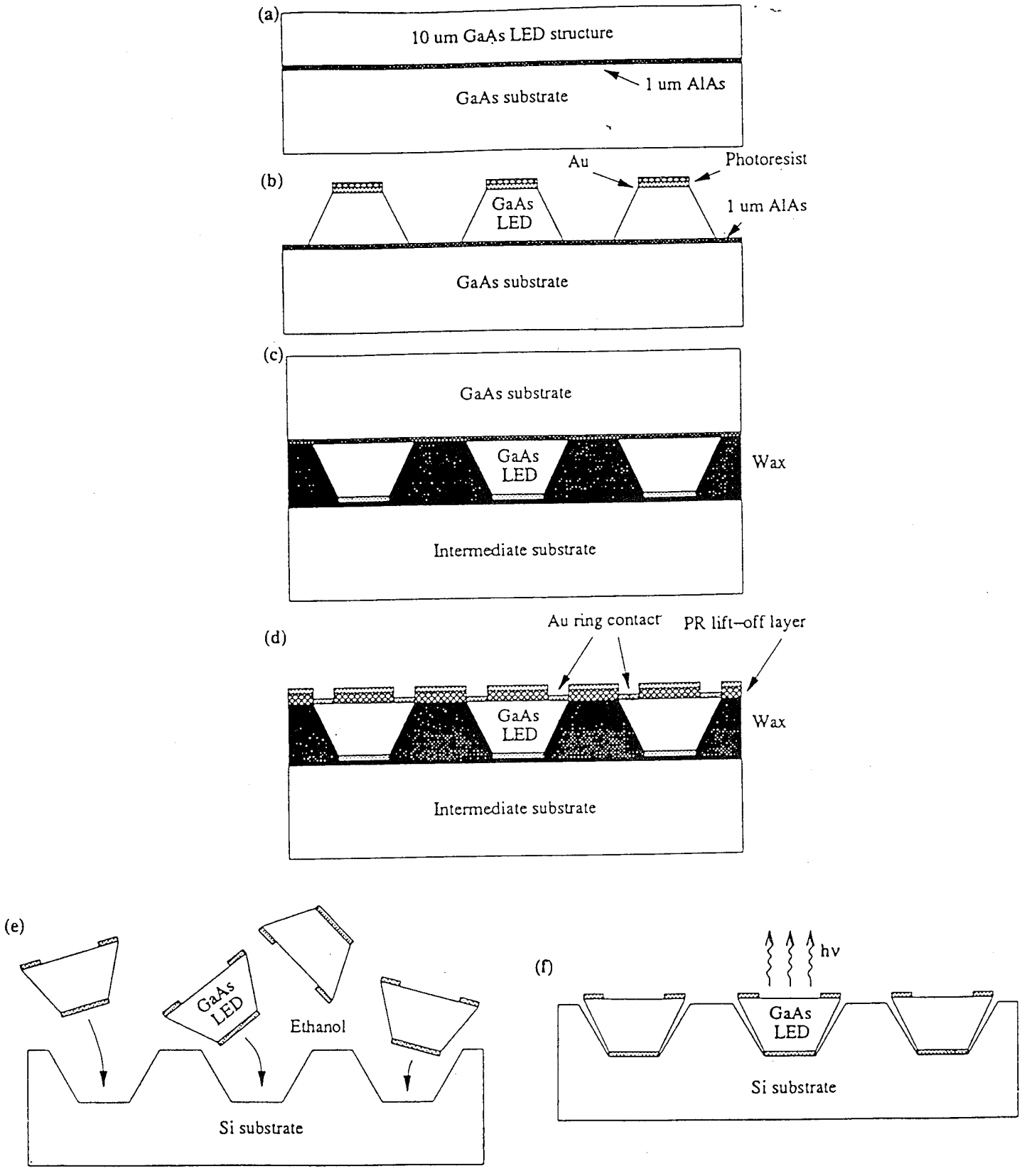

(a)
10 um GaAs LED structure
1 um AlAs
GaAs substrate
(b)
Au
Photoresist
GaAs LED
1 um AlAs
GaAs substrate
(c)
GaAs substrate
GaAs LED
Wax
Intermediate substrate
(d)
Au ring contact
PR lift-off layer
GaAs LED
Wax
Intermediate substrate
(e)
GaAs LED
Ethanol
Si substrate
(f)
hν
GaAs LED
Si substrate

Fig. 2.5.1

Ion milling was used to produce the trapezoidal GaAs mesas by etching the wafer down to the AlAs etch stop layer. Anisotropic GaAs wet etches typically produce sidewalls which slope inward on mask edges parallel to the [110] direction. The ion mill etches GaAs by physical sputtering which is not selective with respect to AlAs composition or doping profile, and produces the correct outward sloping profile in all directions. Square patterns of 4μm thick AZ4330 photoresist were defined on the grown wafer to protect the tops of the mesas during ion milling. The sidewall angles this produced were 68°. The base of the blocks were designed to be 10μm x 10μm to match the base of the holes. The tops of the blocks measured 18μm x 18μm.

The integrated light-emitting diodes must be metallized both on the top side to make the n-type contacts and on the bottom side to make the p-type contacts and on the bottom side of the blocks was metallized with Au immediately after the MBE growth when it was exposed at the surface of the wafer.

The top side of the light-emitting diodes requires a ring contact to provide an aperture for light output. The top contact can only be made after the substrate is removed when the top side of the blocks is exposed. After ion milling, the GaAs wafer containing the mesas was bonded to an intermediate substrate with a high-temperature wax which filled the gaps between the trapezoidal mesas. The remaining GaAs substrate was them lapped to 50μm and etched away by a selective GaAs etch that stopped at the AlAs etch -stop layer. A 10 second dip in HF was used to remove the remaining AlAs.

The top side of the GaAs blocks was now exposed and held on the rigid intermediate substrate. The wax that filled the gaps planarized the exposed surface for photolithography.

Gold ring contacts were made by lift-off metallization. The output apertures measured $7\mu m \times 7\mu m$.

The wax was dissolved with trichloroethane (TCA) to free the blocks, The solvent was then decanted and the blocks transferred into an inert carrier fluid that does not oxidize GaAs. The blocks can be stored in ethanol or methanol for several months without degradation. The carrier fluid containing the blocks was then dispensed over the host Si wafers with the etched holes to assemble the devices (Fig. 2.5.2).

Greater than 90% of the holes are correctly filled by the blocks while immersed in the carrier fluid because of the trapezoidal design. However, the surface tension of the evaporating fluid pulls some of the blocks out after they are properly placed into the holes, reducing the yield to 30-70% locally. Once the fluid dries, the blocks are attached to the substrate by van der Waal's forces between the blocks and the substrate. Suitable bonding materials such as In can be deposited on the base of the blocks or in the holes to provide a stronger bond to the substrate. Supercritical liquid evaporation using liquid CO_2 and methanol is being investigated as a way to remove the carrier fluid without surface tension.

The integrated light-emitting diodes successfully emit infrared radiation which is clearly visibly through an infrared viewer. In addition to light output from the ring contact aperture, light is also emitted from the sides of the trapezoidal blocks. This light is reflected from the sidewalls of the trapezoidal holes etched in Si and is also visible. The i-v characteristics of the integrated light-emitting diodes display typical GaAs p-n junction characteristics with approximately a 1V diode turn on voltage (Fig.2.5.3).

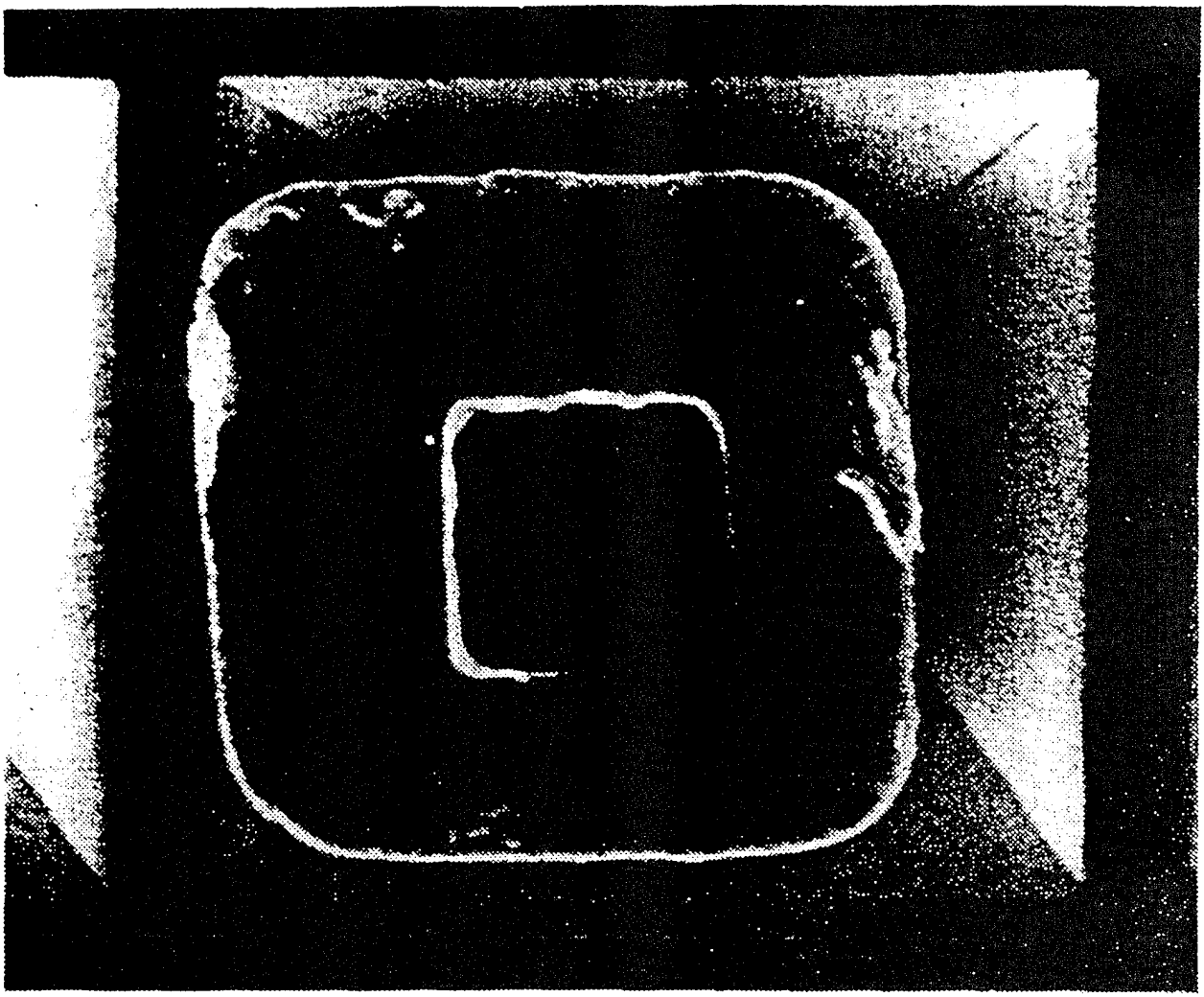


Fig. 2.5.2

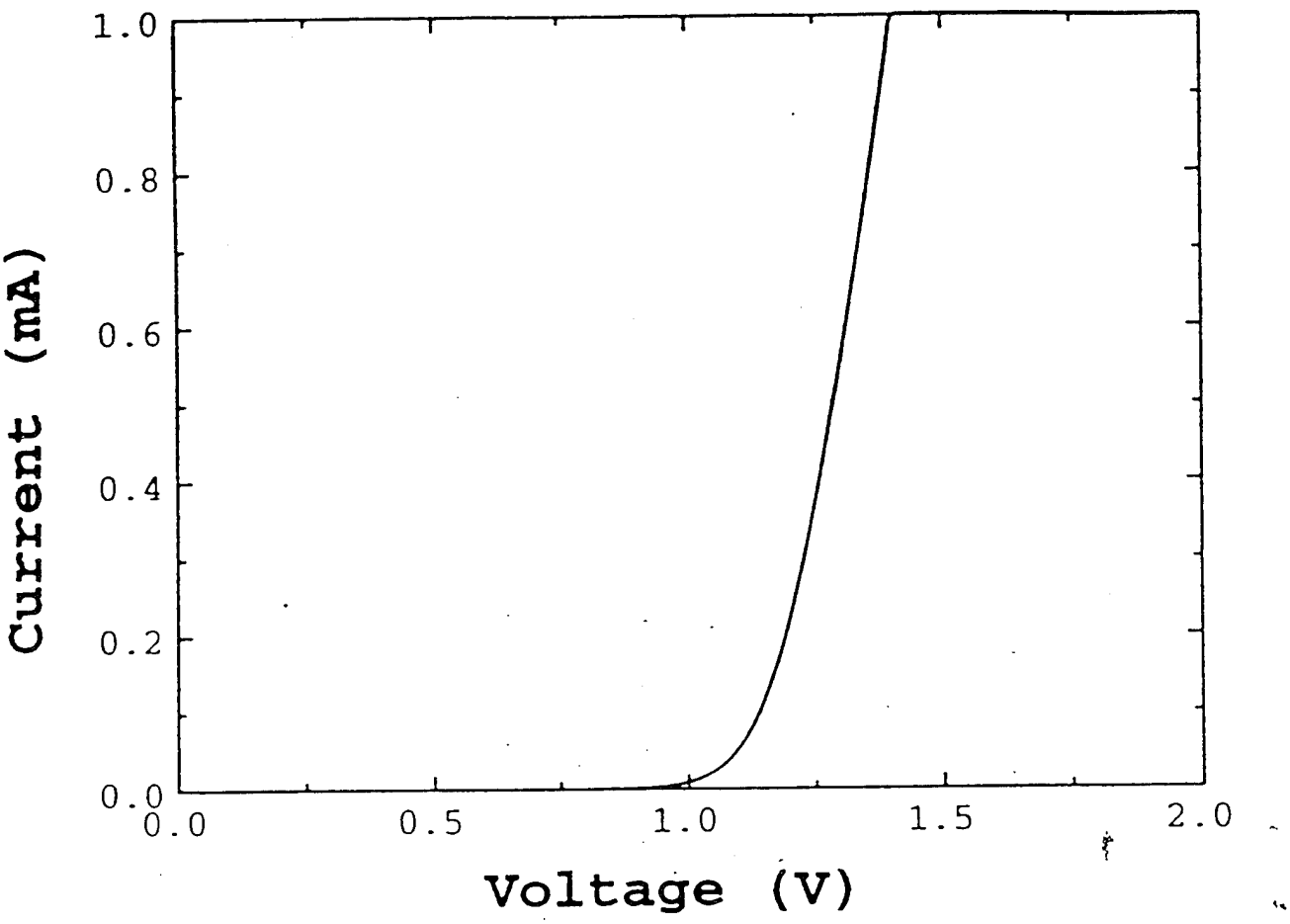


Fig. 2.5.3

After the assembly, no organic residue was observed on the surfaces of the wafer or the blocks.

Vertical-cavity surface-emitting lasers (VCSEL'S) can be integrated the same way for narrow-bandwidth high-power optical emitters. With 16 pairs of n-type and p-type bragg mirrors on each side of the active region, the height of the blocks is approximately 6 μm. The size of the output apertures can range from 5 μm x 5 μm to 10 μm x 10 μm. Care must be taken to protect the A1As regions in the bragg mirrors so they will not be attacked by HF after the substrate removal.

GaAs microwave devices can be similarly integrated onto Si. GaAs resonant-tunneling diodes have been successfully integrated using fluidic self-assembly and the results are presented elsewhere[7]. Work is in progress to use the same technology to fabricate and integrate heterojunction bipolar transistors and heterojunction field effect transistors.

In conclusion, we have demonstrated the fluidic self assembly process by integrating GaAs light-emitting diodes on Si wafers. Technology to metallized both sides of the devices have been developed and top-sid ring contact metallization have been performed for light output aperture. the integration of vertical-cavity surface-emitting lasers using this process is in progress,

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2.6 Fluidic Self-Assembly of InGaAs Vertical Cavity Surface Emitting Lasers onto Silicon

Introduction: Vertical cavity surface emitting lasers (VCSELs) are an attractive candidate for optoelectronic integrated circuits (OEICs). Not only do these devices have low threshold currents and high wallplug efficiencies[1], but they also are compact in size and can easily be fabricated into dense 2-D arrays. By integrating VCSELs with Si circuitry, high performance OEICs can be attained. Recently, fluidic self-assembly (FSA) has been presented as a technique for high yield (>90%) large volume optoelectronic integration. [2,3] In this process, devices are grown on GaAs and fabricated into trapezoidal blocks which are freed from the substrate into a carrier liquid. This solution is then dispensed over a Si receptor wafer which has correspondingly-shaped holes etched into it. Under the ensuing fluid transport, blocks self-assemble into the holes. This technique has advantages over other processes such as epitaxial liftoff in that it can perform rapid integration of large numbers of devices, make precision placement of discrete devices without alignment, make more efficient use of wafer material, and be compatible with a planar process flow. up until now, GaAs microstructures integrated in this manner have only been tested by direct probing. [4,5] This report presents a planar process flow that includes device isola-

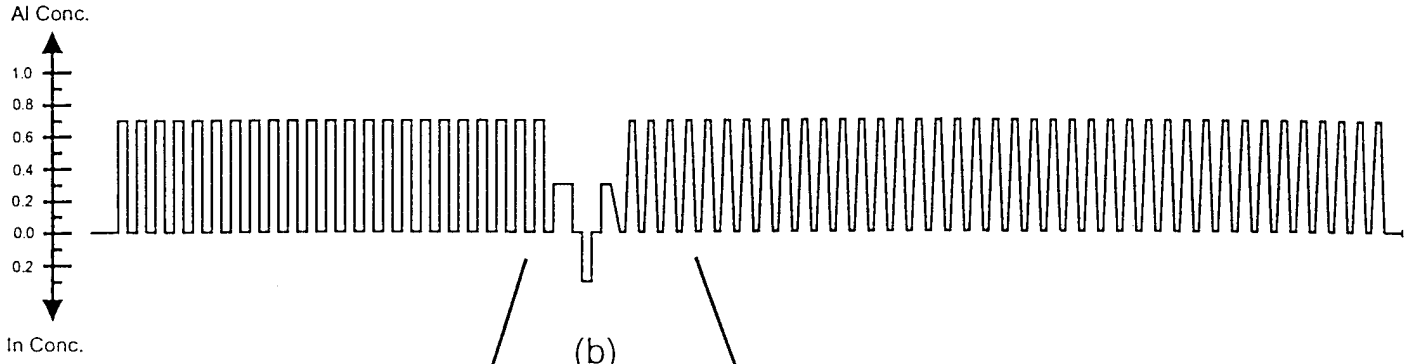
tion, bonding and contacting[6] resulting in the first successful integration of VCSELs onto Si by FSA.

Device fabrication: The VCSELs were designed to operate at 0.98 μm and were grown by MBE with a Varian Gen-II machine. Thermal emission measurements[7] were used to provide in situ monitoring of the growth rates. The Al content in the mirrors was chosen to be x=0.67 so that the total device thickness would be close to the 10μm depth of the hole. The laser structure (fig. 2.6.1) was grown on top of a 1.3μm-thick, AlAs sacrificial etch layer. These lasers were top-emitting with the n-mirror placed on top to give a more uniform current injection. Since the device layers are integrated upside-down onto Si, the n-mirror, which consists of 23 quarter-wavelength pairs of GaAs/AlGaAs, was grown first. The active region consisted of 3 x 75 $\AA$ $In_{0.2}Ga_{0.8}As$ quantum wells centered in a one-wavelength GaAs/AlGaAs pairs. Linear grading with excess doping was used in the p-mirror to reduce the series resistance. In both the n and p mirrors, the doping was lowered in the Bragg pairs nearest the active region to reduce the effects of free carrier absorption.

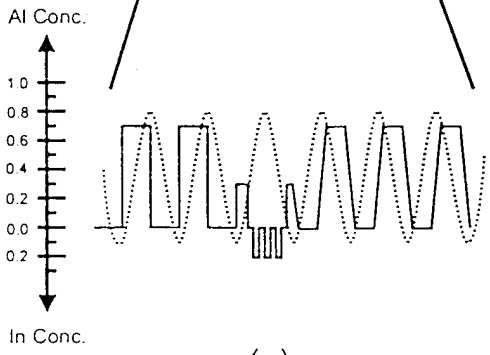
Following growth, the wafer was metallized with CrAu and ionmilled down to the AlAs layer for form 40 x 40 μm^2 trapezoidal blocks. [2] The wafer was then encased face-down in wax, and the substrate was removed using a combination of mechanical lapping and selective chemical etching (3:100 NH_4OH H_2O_2). The AlAs was removed with 5;1 BHF, and the blocks were freed from the wax with acetone. The blocks were then transferred into the carrier liquid, ethanol.


Doping (10^{18} cm^{-3})
10
8
6
4
2
0
Si-doping
Be-doping

(a)


Al Conc.
1.0
0.8
0.6
0.4
0.2
0.0
0.2
In Conc.

(b)


Al Conc.
1.0
0.8
0.6
0.4
0.2
0.0
0.2
In Conc.

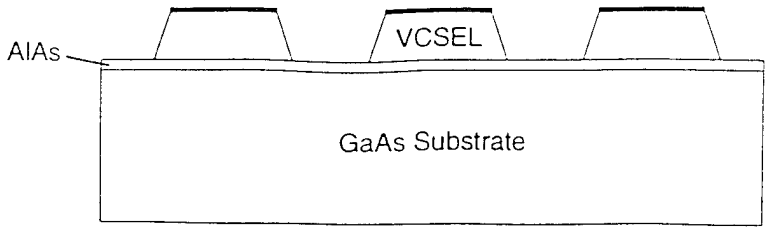
(c)

Fig. 2.6.1

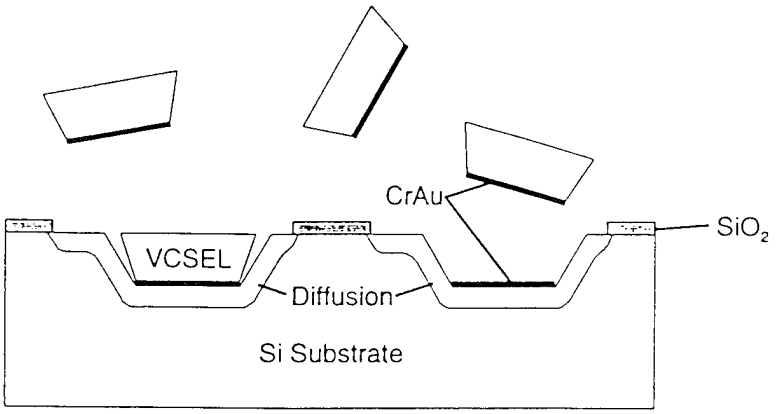
The integration and processing of the receptor wafer is discussed in more detail in Ref. [6]. For the receptor wafer 10 μm-deep holes were etched with a solution of KOH:H_2O:IPA at a temperature of 80° C. A diffusion step was performed to provide electrical isolation as well as contact to the bottom of the hole. Gold was then evaporated and patterned to form an actual bottom contact. This contact also served to bond the block into the hole after integration.

FSA was then carried out using a modified recirculation scheme. The wafer was placed into the beaker with the solution in it and a pipette was used to create fluid flow. Following integration, the solvent was evaporated, and the blocks were bonded into the hole by heating the wafer at 300° C for 5 min. Because the ion milling of the GaAs devices and the wet etching of the Si holes produce different sidewall angles, there will be small gaps (2-3 μm) around the integrated device (see Fig. 2.6.2(b) for a cross-sectional view). These gaps were eliminated by planarizing the wafer with polymide. After a etchback step, via holes were opened up. A final metallization/lithography step (auGe/Au) was performed to define the ring contacts and the bonding pads. Before testing the VCSELs the polymide and SiO_2 were removed from the center of the ring contact.

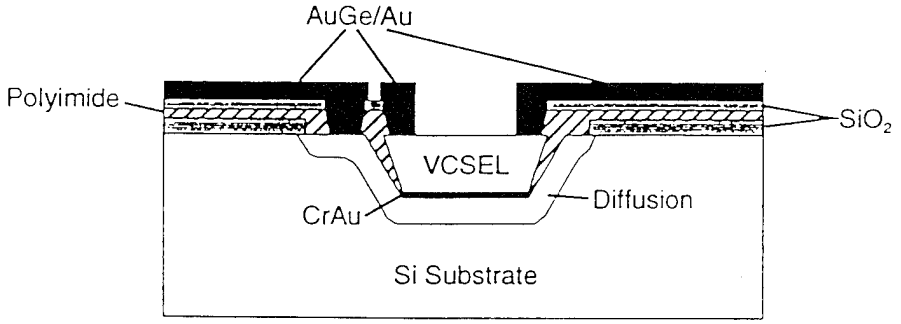
Characterization and discussion: The lasers were tested pulsed at 100KHz with a 1% duty cycle. All devices lased at 0.98 μm to within 1% accurate. The lowest I_{th} was found to be 75 mA with a $V_T = 2.9$ V. (Fig. 2.6.3) The best quantum efficiency was 6.6% with peak output powers greater than 1.5mW with no sign of toll over in the L-I plots. The series resistivity was 8 X $10^{-4}\ \Omega - cm^2$ indicating that the mirrors were fairly conductive. using


AlAs
VCSEL
GaAs Substrate

(a)


CrAu
SiO_2
VCSEL
Diffusion
Si Substrate

(b)


AuGe/Au
Polyimide
SiO_2
VCSEL
CrAu
Diffusion
Si Substrate

(c)

Fig. 2.6.2

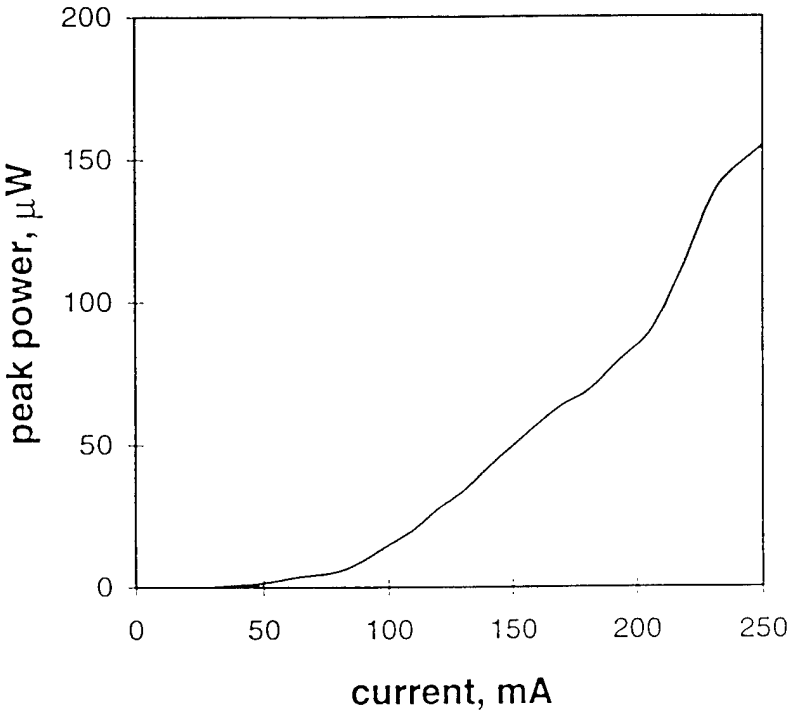


Fig. 2.6.3

a thermal shift of 0.6 K/$\AA$, the thermal resistance was calculated to be 0.5K/mW, which is comparable to VCSELs grown on GaAs.

As of yet neither the device structure nor the process flow has been optimized. We expect the use of a current confinement scheme such as selective oxidation [1] should greatly enhance the device performance. Also by using a lower temperature process, unwanted effects such as gold diffusion should be eliminated.

Conclusion: In summary, we have demonstrated the first successful integration of a VCSEL onto Si by FSA, Threshold currents as low as 75mA were measured for lasers operating pulsed at 0.98μm. Some process modifications have been proposed for improving device performance.

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2.7 New fabrication technique for the integration of large area optoelectronic display panels.

Large area liquid crustal display panels are very important for the fabrication of flat panel displays. however, multiplexing individual display lines limits the contrast of the LCD display because the individual pixels only remain on or off for a fraction of the frame cycle. This is especially severe in the case of high-definition television (HDTV) where the number of scan lines is greatly increased. Active-matrix displays in which each pixel has its own driving circuitry which latches the state of the pixel during the entire frame cycle provides a solution to this problem. However, with conventional technology the size of the Si wafer required to make the driving transistors is not sufficient.

A new technique for the integration of Si drivers on large area active matrix LCD display panels is proposed in this report. Si driving circuitry is fabricated on commercially available silicon-on-insular (SOI) substrates. The drivers are separated by a mesa etch down to the silicon dioxide layer beneath the wafer surface. They are then lifted-off the Si substrate by a sacrificial oxide etch. The circuitry on the top of the blocks is protected by a organic layer such as polyamide or photoresist during the oxide etch.

The freed devices are placed into an inert solution and flowed into holes made in a display panel to receive the devices. Electrical contacts are metallized on the panel to the drivers for each pixel. Finally, the liquid crystal layer is deposited and further processing is performed to make the large area display.

The advantage of this technique is that the Si drivers, which are small compared to the pixel size, can be fabricated densely packed on the available wafer area. They are separated. lifted-off the Si substrate, and integrated on a panel with a much larger area. The size of the display is no longer limited by the size of the Si wafer.

Drivers can be make ahead of time and collected from a large number of wafers for very large displays. Also, the solution containing the drivers can be reused so wafer area is not wasted. Light-emitting diodes and semiconductor lasers can also be integrated onto a flat panel display made of a (large) foreign substrate by this technique.