David Sarnoff Research Center
Subsidiary of SRI International

CERAMIC/METAL COMPOSITE CIRCUIT-BOARD-LEVEL TECHNOLOGY FOR APPLICATION SPECIFIC ELECTRONIC MODULES (ASEMs)

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TECHNICAL REPORT

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The David Sarnoff Research Center hereby certifies that, to the best of its knowledge and belief, the technical data delivered herewith under Contract No. DAAB07-94-C-C009 is complete, accurate, and complies with all requirements of the contract.

Date: 3/11/96

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Section I
WBS Task 2.1: Technology Transfer to Merchant Suppliers

A. TASK OBJECTIVE

Transfer the LTCC-M technology to a merchant circuit supplier, Alcoa Electronic Packaging, Inc. This task will require a steady supply of several custom glasses that were developed during the Phase 1 program. One or more glass producers will be qualified to supply materials to the David Sarnoff Research Center or its designee to produce LTCC-M circuit boards and packages. The Phase 1 technology will be interactively transferred to Alcoa Electronic Packaging, who will be qualified by the fabrication of test structures and technology demonstration modules.

B. INTRODUCTION

During Phase I of this Project all the glasses needed to fabricate LTCC-M substrates on Cu/Mo/Cu cores were formulated and prepared at Sarnoff. This enabled us to readily prepare small amounts of many different compositions needed to attain required attributes in the glasses. A commercial source for these glasses is needed to ensure their adequate supply to a manufacturing operation. We have identified SEM-COM, a merchant supplier of specialty glasses to the electronics industry as this source. The single-sided LTCC-M Technology Transfer to Alcoa Electronic Packaging was completed this past quarter. Rather than duplicate many of the processes developed at Sarnoff, Alcoa tried to implement LTCC-M on their existing equipment operating with minimal modification. This technology transfer was significantly impeded by the lack of a belt furnace at Alcoa.

C. DEVELOP COMMERCIAL GLASS SUPPLIER

Six (6) different glasses are used in LTCC-M. Table I.1 shows the status of the glasses melted by SEM-COM. Each one will be qualified through tests performed at Sarnoff. The qualification process will involve testing the important attributes of the glasses relevant to the successful fabrication of LTCC-M substrates.

Table I.1: Status of Glasses Melted by SEM-COM

Glass	LTCC-M Use	Melted by SEM-COM	Characterized	Qualified in LTCC-M
KU-14	Green Tape	✔	✔	✔
KU-6	Green Tape	✔	✔	✔
KU-8	Via Ink	✔	✔	✔
MSR-31	Glaze	✔	✔	✔
G-63	Top Conductor Ink	✔		
G-14	Cu/Mo/Cu Feedthroughs	✔		

Results:
1. KU-8 glass melted by SEM COM has been successfully formulated into a via ink that is compatible with the ABT-52 SC green tape.
2. SEM COM has melted glasses G-63 and G-14. These glasses will characterized and formulated into thick film ink next quarter.
3. Sarnoff has adapted both the green tape formulation and the LTCC-M processing to accommodate all SEM COM glasses that are listed as qualified. The aim of this portion of the program was to adapt the LTCC-M materials and their processing to glass processed with commercial equipment, rather than laboratory equipment.

D. TECHNOLOGY TRANSFER TO ALCOA

Summary by Process Sector

Key points describing the successful technology transfer areas, problem areas, diagnostic testing, relative comments, and a preliminary assessment on readiness for manufacturing are listed below by process sectors:

1. Glass Powders and Composition

- Alcoa purchased glasses, from SEM-COM, were found to be outside the initial Sarnoff specifications. The particle size range was changed by Sarnoff from -400 mesh to -200 mesh. Tapes made from these glasses were found to fire to light gray color. Analytical results by Corning did not reveal any impurities at levels above those normally detected. Sarnoff released these materials after their testing found no degradation in electrical performance.
- Glass characterization was completed to verify the compositions and to document key parameters such as softening point, transition temperature and crystallization behavior. Typically, close monitoring of incoming material characteristics would be pursued and correlated to actual performance in a product format prior to full manufacturing endorsement.
- The issues noted with camber, see Firing, suggest that further work on lot variations, crystal seeding, and thermal profile effects would be useful.

2. Tape Formulation and Casting

- Evaluation of the Sarnoff-specified tape composition showed it to be too weak and limp to process in a larger format with AEP manufacturing tooling. Incomplete release from the coated polyester carrier was also seen.
- Tapes made from the AEP proprietary organic formulation were found to have processing characteristics like that of the standard high alumina ceramic (punching, handling, etc.). The formulation results in a tape with 8.0 weight % organics compared to 8.44 weight % for the Sarnoff formulation. As-cast tape densities are larger for the modified composition. However, upon lamination similar densities are achieved.
- The Sarnoff materials adapted well to the AEP tape system and are thought to be easily scaleable to high volumes.

3. Paste Materials and Preparation

- All pastes were prepared according to the Sarnoff specifications. Modifications were made to comply with normal safety precautions - keeping solvents well below the flash point.

- All ink formulations were found to be acceptable for both printing and co-firing.
- Ink formulations were found to be acceptable for processing small builds using current microprocessor ground rules. Volume manufacturing could not be assessed in the scope of this work.

4. Lamination

- Lamination and co-lamination uses AEP proprietary tooling.
- Minor variations from the Sarnoff conditions were used.
- No major problems were found at lamination for the test designs with less metal loading. Those with full metal planes showed mixed results which are possible to resolve. Further work would be required to verify this.

5. Core Preparation

- Process consistency and reproducibility were found to be lacking in results from tests at Alcoa: coloration, bonding, and camber.
- Differences in nickel plating thickness and appearance were also discovered and further tested. Much of the effort was expended on a defective bath solution supplied by Technic. Additional effort was made to replicate thicknesses. duplication was assured after introducing weight gain as the key process monitor.
- One major problem area found was the lack of consistent reaction or bond of the glaze material with the oxidized nickel-plated metal core. A lighter colored green glaze was accompanied by either blistering or spalling of glaze or NiO from the nickel plating. The severity of this behavior varied widely, from complete debonding to an occasional isolated area barely detectable within the desired, uniform dark green oxide and reflowed glaze. Such variations were noted for parts plated in the same batch. This behavior has been observed on parts throughout the program on samples plated at Alcoa and Sarnoff and oxidized in Alcoa's programmable box furnace. The problem has been program-inhibiting at Alcoa.
- As expected, significant differences were found for the glass-ceramic crystalline phases present at the interface with the metal core as compared to bulk or free surface.
- Analytical tests did not reveal any chemical differences between the good and bad samples
- At room temperature, the appearance of the Alcoa bath indicates some undissolved material, while the Sarnoff bath is transparent (green). When heated to normal plating temperature, both baths are transparent (green). Hull cell tests did not reveal any differences between the baths in the normal plating current density region .
- Differences in the weight gained on oxidation were found to depend on where the plating was done. Sarnoff plated samples consistently gained more weight than Alcoa plated samples. No explanation for this has been found.
- Recent test results using higher temperatures for oxidation show encouraging results: lower incidence of the light green discoloration. Further effort should be invested here and on understanding the causes of the light green coloration.
- It is recommended that process window experiments be designed and conducted to evaluate the robustness of this system.

- Evaluation by Technic of the plating bath used at Alcoa revealed excessive levels of organic components. It is probable that this is the source of the light green coloration (after oxidation) observed on parts plated at Alcoa. A 2 - 4 hour carbon treatment was recommended to bring the bath back to specified levels. It is probable that the excess organics are high levels of the wetting agent. Experiments at Sarnoff intended to reproduce the undissolved appearance of the Alcoa bath indicate that the bath contains more than 15x the recommended addition of 20 cc/gal of wetting agent.

6. Firing

- Belt furnaces having turbulent air flows were recommended by Sarnoff for all firing and oxidizing steps. Since such furnaces were not available at either the Alcoa Technical Center or at the Alcoa Electronic Packaging Co., a programmable batch furnace was substituted.
- Sarnoff temperature profiles were approximated and Sarnoff supplied materials were fired as a control. Fired parts exhibited a small degree of corner lifting, and some camber.
- Slower heating rates were introduced in the binder removal range to assist firing of thicker microprocessor packages made with the modified tape formulation. Initially a slower ramp to 650°C was used with a 30 minute hold. Late in the program this hold point was lowered to 450°C to insure that premature silver densification was not occurring. No obvious binder removal problems or change in the camber was found. A profile of this slower heating ramp is shown in Figure I.1.
- While the slower heating ramp initially produced acceptable parts with the Sarnoff supplied control samples, parts made with Alcoa produced green tape and laminated by Alcoa exhibited unacceptably high camber. The camber direction was such that the coefficient of thermal expansion of the ceramic was greater than that of the Cu/Mo/Cu core.
- Parts fired at Sarnoff (in a belt furnace running the recommended profile) using Alcoa produced green tape exhibit an excellent fired appearance and acceptable camber.
- Parts fired at Sarnoff (in a belt furnace running the recommended profile) using Alcoa plated and oxidized (both standard and high temperature oxidation process) Cu/Mo/Cu, and Sarnoff produced green tape exhibit a very good appearance and acceptable camber. Neither blistering nor spalling of the glaze or Ni-oxide from the nickel plating were observed with these parts after firing.

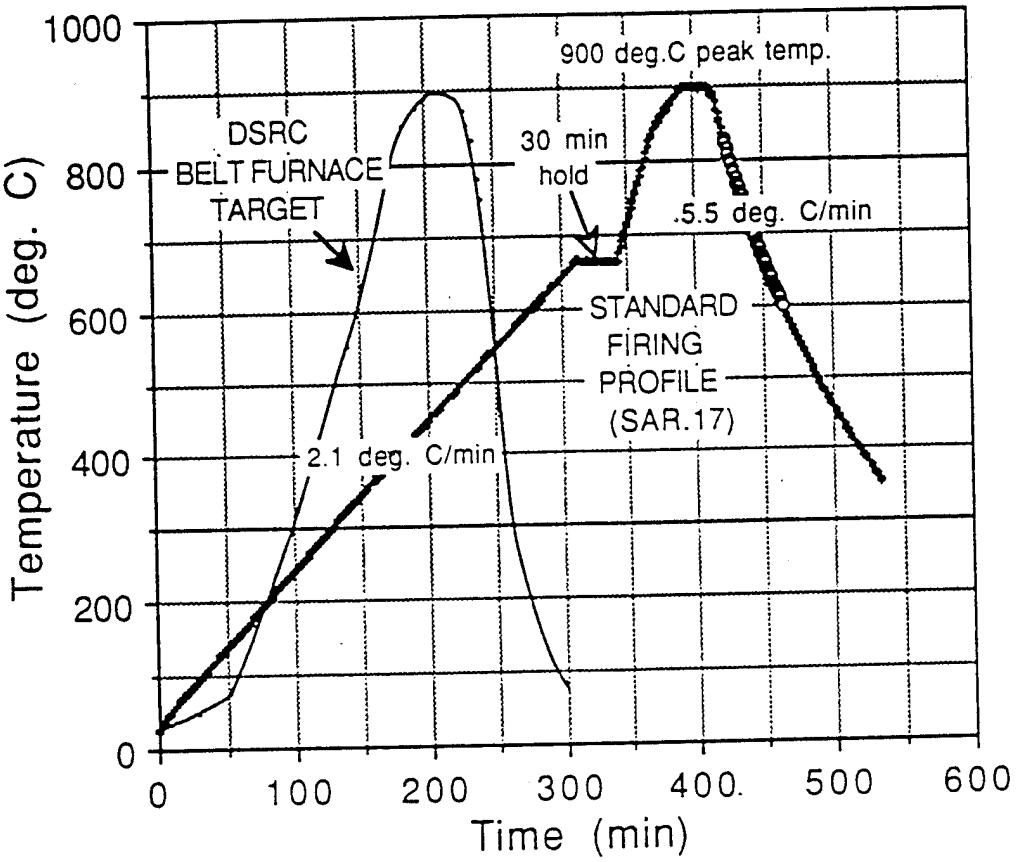

Figure I.1: Temperature profile used to fire samples in the programmable box furnace at Alcoa.

Conclusions

The major deviation from Sarnoff's recommended LTCC-M Process Specifications was the use of a programmable box furnace (convection air flow) to replace an 8 zone belt furnace having turbulent airflow. This departure resulted in samples having unacceptable camber, and is a likely to be a contributor to the blistering and spalling observed between the Ni and the Ni-oxide or the glaze. The other major contributor to the blistering and spalling Ni is the use of a plating bath having excessive levels of organics.

Another possible contributor to the camber problem is the proprietary lamination process used by Alcoa. Excess lamination pressure can also cause the type of camber observed in test samples made at Alcoa. Further experiments are required to determine whether lamination conditions played a significant role in causing the excessive camber observed at Alcoa.

To eliminate the programmable box furnace from the "manufacturing" cycle, Sarnoff fired samples having either Alcoa made tape on Sarnoff prepared Cu/Mo/Cu cores, or samples having Sarnoff made tape on Alcoa plated and oxidized Cu/Mo/Cu. In both cases, the fired samples exhibited very good appearance and camber. This conclusively shows that a programmable box furnace cannot be simply substituted for a belt furnace in demonstrating the robustness of a manufacturing process.

E. PLAN FOR NEXT QUARTER

- Complete qualification of glasses G-14 and G-63, melted by SEM-COM

Section II
WBS Task 2.2: Customize LTCC-M for Specific Applications

A. TASK OBJECTIVE

Extend the LTCC-M technology to meet any requirements of the technology demonstration modules, and any general packaging trends of the electronics industry.

B. INTRODUCTION

Progress is reported for three of the major technology extension areas of this Phase 2 program; namely the formation of precise cavities in LTCC-M substrates, development of high adhesion top conductor ink formulations, and the extension of LTCC-M to higher density circuits. The best known cavity packages are single chip packages such as DIPs, and Quad Flat Packs (QFPs) used for microprocessor packaging. In these and other packages, the dimensional tolerances of the needed cavities must be tightly controlled to specified values for reasons such as automatic device placement including wire bonding, minimizing and controlling the wire bond lengths, controlling the module profile after device placement, ensuring good thermal contact between the device and the substrate etc. In a conventional multilayer ceramic process, the x, y shrinkages are of the order of 15% during firing, so the individual green tape layers are punched to a known over size, determined empirically, to obtain the desired cavity size. Extensive work is reported for development of processing to produce cavities that replicate their punched size after firing.

To extend LTCC-M to higher density circuits, the reduced size of the component connection pads require increased adhesion of the top conductors to the ceramic. Thick film inks were developed last quarter that exhibited significantly improved top conductor adhesion. This quarter these inks have been undergoing reliability testing, and thus far there has been no decrease in the conductor adhesion. To increase the circuit density of LTCC-M substrates, thick film inks have been developed that can produce test structures having 4 mil diameter vias and 4 mil lines and spaces. We have begun fabrication and reliability testing of a high density test pattern featuring 4 lines and spaces combined with 4 mil vias. This pattern routes one or more 4 mil lines between 4 mil diameter vias.

C. OPTIMIZE CAVITY PROCESSING FOR LTCC-M TECHNOLOGY

Background:

Cavities in single chip and multichip ceramic packages may be needed for one or more of the following reasons:

1. To mount the device on a heat sink attached to the bottom of the substrate
2. To provide one or more levels of peripheral wire bond pads for device attachment
3. To lower the profile of the module (through the attachment of devices to recessed bond pads in the substrate.

In the previous two quarters, cavities of type 1 and type 2 morphologies (these morphologies are described below) were evaluated for LTCC-M.

Objectives:

- Develop a simple, robust, cost effective and manufacturable process for fabrication of complicated cavity patterns with high precision cavities.
- Extend studies to type 3 cavities and develop a process to achieve high precision cavity dimensions.
- All of the above should conform to the LTCC-M prototypes that will be fabricated under the scope this program.

Types of cavities:

With respect to stackings (laminates) of ceramic on the Cu-Mo-Cu metal core, three basic types of
cavity morphologies were evaluated:
(i) Type 1 cavity: In this cavity morphology, the cavities in the ceramic laminate extend all the way
down to the metal core, see Figure II.1.
(ii) Type 2 cavity: Here a flat laminate of ceramic is present between the metal core and the laminate with cavity, see Figure II.1.
(iii) Type 3 cavity: This is a tiered cavity morphology where two separate ceramic laminates are stacked on top of each other with different cavity sizes, see Figure II.1.

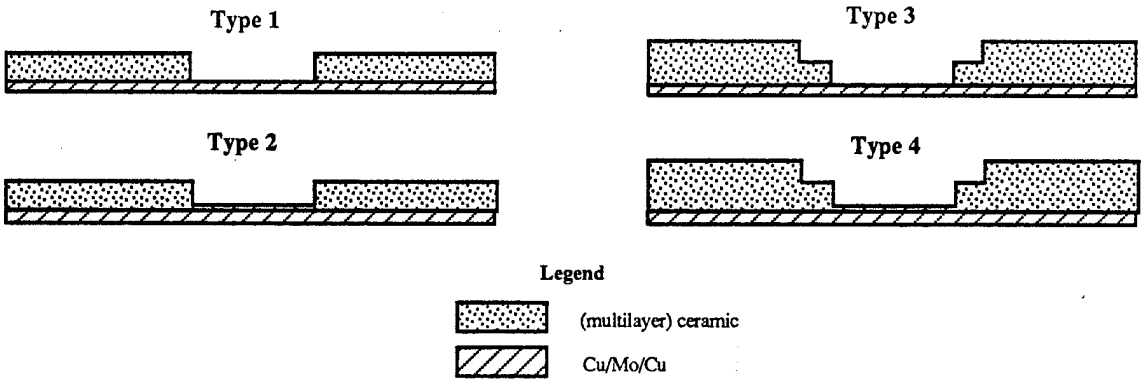

Figure II.1: Schematic illustrations of cavity types.

Major issues:

- Tight control of cavity dimensions of the cofired LTCC-M for 1, 2 and 3 cavity types.
- Optimize the use of LN-1 ink to fabricate high precision type 1, 2 and 3 cavity morphologies such that the prototypes can be easily fabricated using this process.

Approaches to solve the problems:

A large number of experiments were designed to tackle the above mentioned problems. Interest was shifted from LN-1 tape to LN-1 ink for various advantages such as being able to preferentially apply LN-1 not to expose areas of bond pads and that cavity precision remains identical with LN-1 tape or ink.
For a type 2 cavity morphology the following fabrication technique is now recommended for high precision cavities:

1. Laminate 3 layers of ABT-52 tape and with the top layer of tape printed with LN-1 ink as a blanket coat on top (all tapes unpunched) at 3000 LB load, after preheating for 1 min. at 185°F, for a total of 2 min., with 30 seconds on each side (rotation).
2. Punch out the Raytheon cavity pattern using the punch designed to do so. Measure cavity dimensions.
3. Make a second laminate with three layers of unpunched ABT-52 tapes at 3000 LB load, after preheating for 1 min. at 185°F, for a total of 2 min., with 30 seconds on each side (rotation).
4. Place the laminate from step 2 over the laminate from step 3 and laminate using regular (flat bottom and top) fixture at 1000 LB load after preheating for 1 min. at 185°F, for a total of 2 min., with 30 seconds on each side (rotation).
5. Trim off the edges using a shear and colaminate on the metal core at 600 LB load after preheating for 1 min. at 185°F, for a total of 2 min., with 30 seconds on each side (rotation). Measure cavity dimensions.
6. Fire in the belt furnace using the standard firing profile.
7. Measure cavity dimensions.

This procedure is schematically shown in Figure II.2.

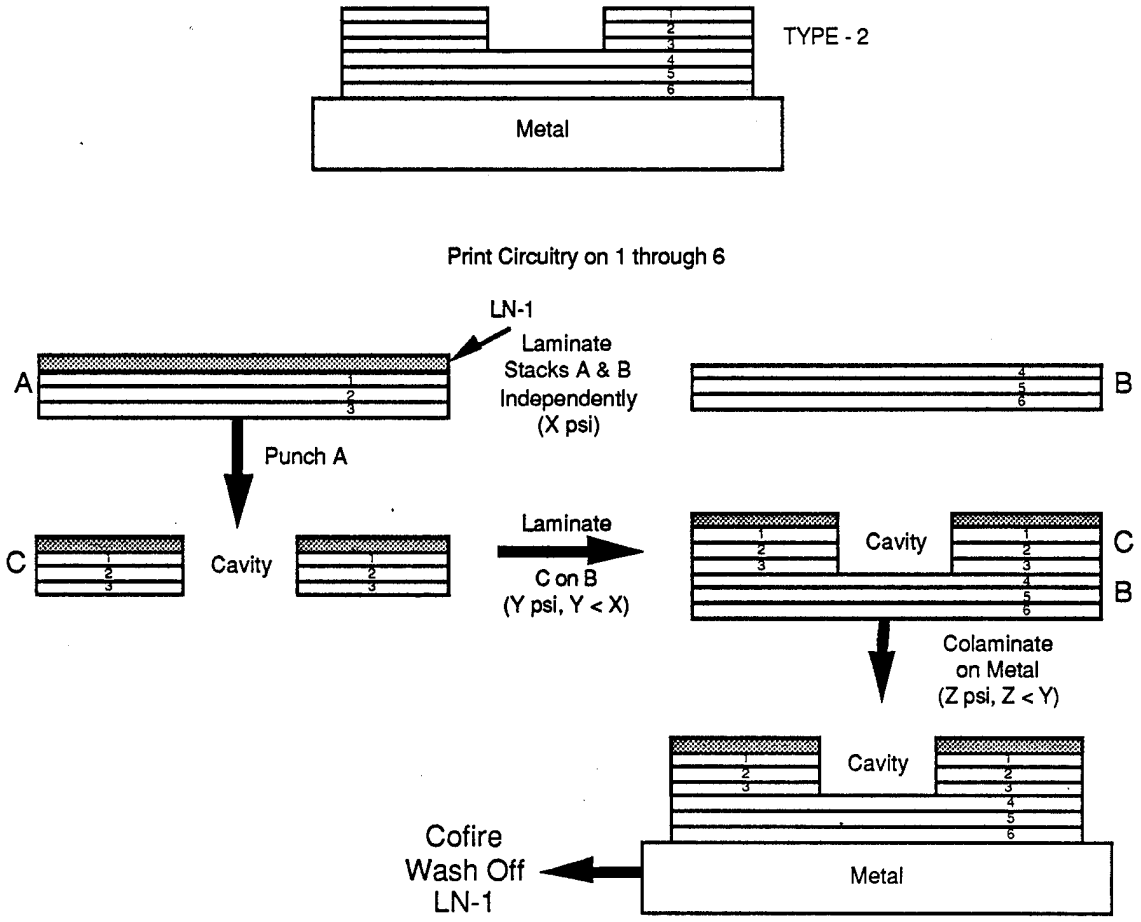

Figure II.2: Schematic illustration of new technique to form high precision type 2 cavities.

Experiments were conducted using Sarnoff prepared as well as Alcoa prepared green tape to test the universality of this new technique and the results were most encouraging. This technique was also extended to type 3 cavity morphology. The results are tabulated in the table below, with the error in the cofired dimensions being 1 standard deviation.

High Precision Cavity Dimensions

Type	Tape	Number of Cavities	Punched (mils)	Cofired (mils)
1	Sarnoff	24	225	226.91 ± 0.37
2	Sarnoff	24	225	227.29 ± 0.67
2	Alcoa	24	225	225.69 ± 0.27
3	Sarnoff	16	180	181.18 ± 0.51
		16	240	240.99 ± 0.50

We also discovered that cavity dimensions (X and Y dimensions) bears a direct correlation to other cavity (mechanical) defects.

Summary of accomplishments in cavity optimization

The following are the advantages of this new cavity fabrication technique:

- Tape Handling: Handling of individually punched tape is far more difficult than a punched laminate. The total number of cavity punching steps is reduced down to one.
- High Precision Cavities: Cavity precision achieved in this program represents the tightest of any MCM-C cavities. The dimensions are very tight, with the difference between the maximum and minimum cofired edge length being < 1 mil.
- The cavity mechanical defects are eliminated or minimized. As an example, lipping on the top surface of the cavity is practically eliminated. Profilometry measurements show that the lipping is < 1 μm on the top of the cavity.
- Very Low Expansions (< 1 %): This result is also very significant as can result in lower manufacturing yields.
- Always Expansion: Using this new technique, one always observes minimal expansion and never shrinkage relative to the punched cavity dimensions.
- Eliminate complex lamination tooling conventionally used for complex cavity morphologies.

D. HIGH ADHESION TOP CONDUCTORS

The top conductor adhesion measurements after thermal cycling (-55°C to +125°C) reported last quarter have been extended to still greater numbers of thermal cycles. Additionally, Ag thick film ink formulations having less glass than TC-6 and 7 and better fine lines printing characteristics were investigated this past quarter. After firing, the silver conductors were electrolessly plated with Ni and Au layers.

Top Conductor Reliability: Adhesion Data

Thermal Cycling Data (-55°C to +125°C)

The adhesion data for electrolessly plated silver top conductors is shown in Figure II.3. Both of these conductor formulations contain custom glasses that are resistant to etching by the plating baths. Prior to plating, the pads were etched for 3 - 5 seconds in an HF bath; this surface preparation was required to obtain satisfactory plating of these conductor formulations. All formulations show good adhesion of the conductor pad to the ceramic. After more than 800 thermal cycles between -55°C and +125°C, the data do not indicate any crack formation or loss of conductor adhesion. These tests will continue into next quarter.

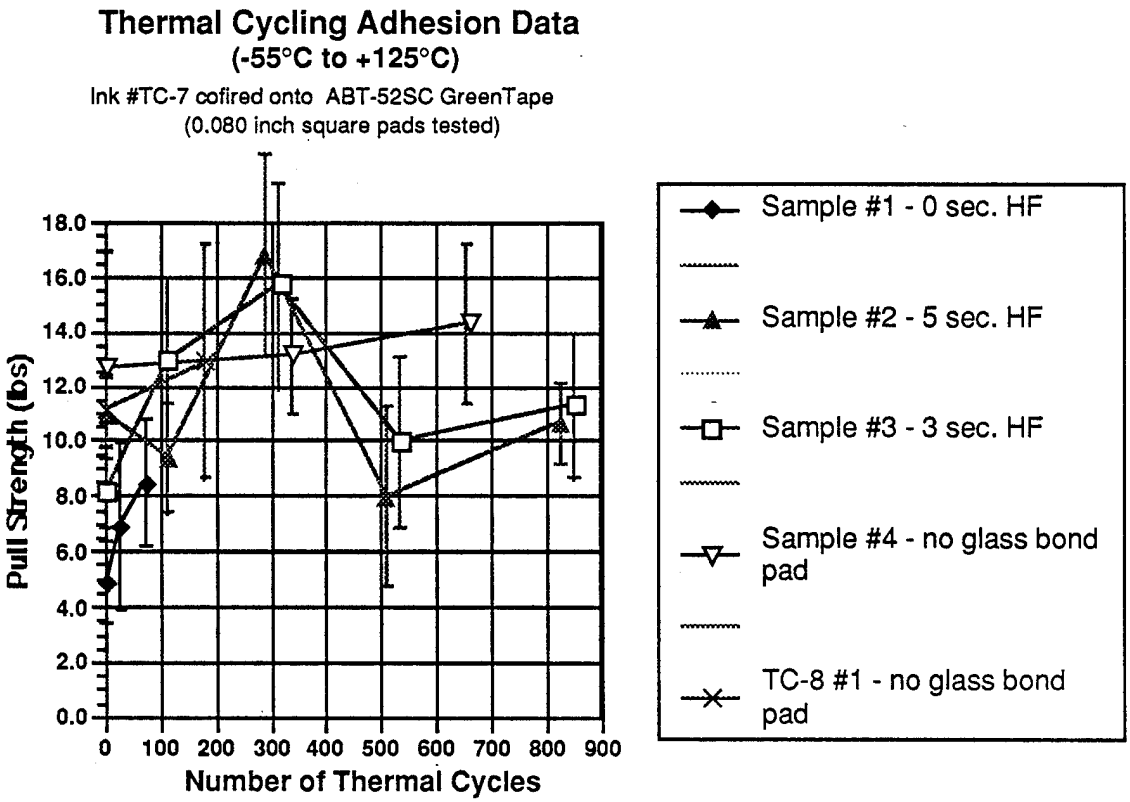

Figure II.3: Thermal cycling data for Au-plated silver thick film conductor formulations. Unless indicated, data refers to ink formulation TC-7

E. HIGH DENSITY CONDUCTOR PATTERNS

High Density Test Board Design

The 1-sided, 4-layer daisy chain test board design was modified for 4 mil diameter vias and 4 mil wide lines and spaces. The via patterns are the same as those of the original design, except that the hole diameters were changed from 8 to 4 mils. Fine lines (4 or 5 mil wide) were incorporated on all of the layers, either to connect the 4 mil vias or between the daisy chained vias; the features and dimensions of the new test board design are summarized in Table II.1. The Layer 1 (top metallization) pattern of the high density test board is shown in Figure II.4.

Table II.1: High Density Test Board Description

- 9 Daisy chains interconnecting a total of 978 vias
- High density region:

  4 mil diameter vias on 16 mil centers
  (1) 4 mil wide line between vias
  120 vias per chain

- Medium density region:

  4 mil diameter vias on 30 mil centers
  (2) 4 mil wide lines with 4 mil spaces between vias
  120 vias per chain

- Low density region:

  4 mil diameter vias on 42 mil centers
  (3) 4 mil wide lines with 4 mil spaces between vias
  84 vias/chain

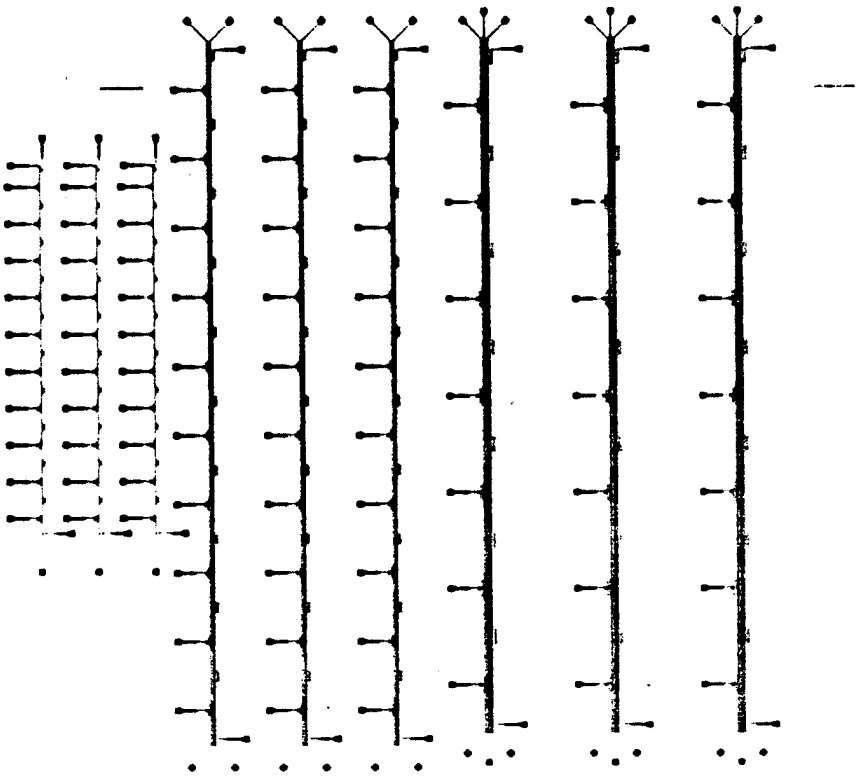

Figure II.4: High density test board top layer conductor pattern

4 mil Diameter Via Development

Additional via test parts were fabricated and evaluated using modified injection filling inks and the high density test pattern (~400 vias per layer). The via ink was modified to reduce the via bump heights after pressure filling and firing; the solids content was reduced slightly (relative to INJ-13 ink) and the cordierite filler material was removed. The modified pressure fill ink is designated INJ- 202B and its composition is given in Table II.2. High density via parts with 3-layers of stacked vias (~400 vias per layer) were fabricated using this ink with good results; the fired part had good via continuity and the via bump heights were < 2 mils.

Table II.2: INJ-202B Via Ink Composition

Function	Weight %
Ag Conductor	64.40
Glass Filler	16.10
Dispersant	2.54
Resin/Solvent	16.96

Top Conductor Ink Compatibility

The fine line printability of the top conductor ink (TC-10) and its compatibility with the via metallization were evaluated. Its fine line printability was good using the layer one pattern (Figure I) of the high density test board. A 36-hole pattern, 4-layer via test part was fabricated using 4 mil diameter injection filled vias (top 3 layers, INJ-202B ink) and with the TC-10 ink printed as 50 mil square pads over the top layer vias. After firing all of the vias had good continuity, indicating that the cofired top conductor ink/via interface has good integrity and conductivity. The top conductor ink composition is given in Table II.3.

Table II.3: Buried and Top Conductor Ink Compositions

Function	BC-110 Weight %	TC-10 Weight %
Silver Powder	40.32	36.35
Silver Flake	40.32	36.35
Glass #1		3.16
Glass #2		3.16
Copper Powder		0.57
Dispersant/Solvent	1.12	1.45
Resin/Solvent #1	9.12	9.48
Resin/Solvent #2	9.12	9.48

Fine Line Development

Printing tests with the BC103C flake Ag buried conductor ink and the fine line high density test board patterns revealed that the flake inks were inadequate for repetitive fine line printing; only 2 to 3 prints could be done before the screens became clogged with ink. Consequently, new buried conductor compositions, incorporating both the Ag flake material and a fine Ag powder, were formulated and tested. Inks with 50/50 and 75/25 mixes of the flake/powder combination were tested for printability and both were found to be far superior to the 100% flake inks. The 50/50 flake/powder ink, designated BC-110, was used for fabrication of the initial high density test boards; its composition is given in Table II.3.

High Density Test Board Fabrication/Evaluation

The first set of high density test boards were fabricated using green tape punched with 4 mil diameter holes and with the following materials: (1) INJ-202B via ink; (2) BC-110 buried conductor ink and (3) TC-10 top conductor ink. The high density via patterns were injection filled with good results; the vias were well filled and had slight bumps on the topsides after filling and drying. Many of the via-filled

layers form this first group of parts were used for fine line printing optimization; therefore, not all of the printed layers were perfect in terms of alignment and print quality. A print/flood printing technique was found to give the best results for repetitive printing of fine line patterns using both the buried and top conductor inks; flooding the screen in between prints minimized ink drying and screen clogging. Good alignment of the printed patterns to the filled vias was achieved and good layer-to-layer alignment in the stacked green tape structure was achieved without the use of any special techniques. Three parts from the first group were laminated and fired at 915°C with good results. For the most part, when good quality printed layers were used, the daisy chain continuity was good and no shorts were detected between lines or between lines and vias. One of the first (3) parts was tested for continuity and chain resistances and then put into temperature cycling (-55°C to +125°C). No degradation of the daisy chain resistances were detected after the first 30 test cycles. Additional parts will be fabricated for temperature cycling and 150°C temperature aging tests.

F. PLAN FOR NEXT QUARTER

- Continue reliability testing of Ag thick film top conductors
- Fabricate additional daisy chain test patterns having 4 mil vias connected to 4 mil lines with 4 mil spaces
- Continue reliability testing of 4 mil via test structures

Section III
WBS Task 2.3: Fabrication and Testing of Technology Demonstration Modules

A. TASK OBJECTIVE

The objective of this task is to design, fabricate, assemble, and test 4 different technology demonstration modules. These modules are: (1) an optoelectronic transceiver module, (2) a power amplifier package, (3) an advanced PCMCIA card, and (4) a Power Electronic Building Block (PEBB).

B. INTRODUCTION

The four technology demonstration vehicles planned for this program were chosen because each module had clear military applicability, and also met the requirements of the consumer marketplace. Table III.1 shows the application of each demonstration module to the needs of the US armed forces.

Table III.1:
Military Relevance of LTCC-M Technology Demonstration Vehicles

Prototype Application	Supporting Co.	Type	Military Relevance
Advanced PCMCIA Card (ORBCOMM Modem)	Contract change	Mixed Signal Module	1. Similar electronics needed for global tracking of high value and critical military materials and components (e.g. armaments) 2. Supports DoD: • Materials Command • Logistics Command • Transportation Command • "Total Asset Visibility" program 3. Technology applicable to the following: • NSA (R2) dual function PCMCIA card • Trackers • Message Terminals • CESEL • Special Forces replacement of high frequency radio systems (miniaturization) • Global extension of communications in Force 21 "Digital Battlefield" 4. Applies to Military Global Mobile Information Systems
High Power Motor Controller (Power Electronics Building Blocks)	Harris	High Power Single Chip Package	1. Supports US Navy Contract # N-00024-94-C-4088 (an Advanced Tech. Demo. with Naval Sea Systems Command) 2. Computer controlled Integrated Variable Speed Electric drive for ships (surface and subsurface) and tanks 3. Computer controlled Electric Actuators for airplanes, ships, and tanks 4. Auxilliary Power Unit Generators, Solid State Power Controllers for airplanes 5. Power Inverters and Converters for ships and airplanes
Optoelectronic Transceiver Module	AMP	MCM	1. Supports the construction of low cost broadband networks at military bases and installations. 2. Such networks support: • ATM based switching architectures • Transfer of large amounts of graphical and multimedia data • Digital signals • Encrypted signals 3. Supports ARPA contract "Manufacturable Low Cost Single-Mode Bi-directional Links for Fiber in the Loop Optical Networks" • Currently LTCC-M is the sole technology for this application
Power Amplifier Packages (microwave)	Raytheon	GaAs single chip package	1. Portable government cellular communications systems and wireless LANs 2. Applies to Military Global Mobile Information Systems

A general set of LTCC-M design guidelines has been communicated to all the circuit designers. Sarnoff has been closely working with all circuit designers to develop manufacturable designs.

C. OPTOELECTRONIC TRANSCEIVER MODULE

Under this program Sarnoff, and AMP will develop a package that will integrate an optoelectronic MCM, an optical fiber, several silicon devices, and several passive components. The goal of this program is to provide LTCC-M packages to AMP (for module assembly) by April, 1996.

Presently, the silicon devices have completed their redesign and have been qualified. The package has been revised to account for the new pinout of the devices, as well as incorporate several package modifications to reduce crosstalk and ease assembly. To meet the various design configurations of AMP, two similar packages were designed and will be fabricated together in a multi-up format. The decision to fabricate the "A" and "B" designs together minimizes the overall NRE costs for building this package. The revised package designs, shown in Figure III.1(a) and (b), have been signed off by AMP. After conversion into an AutoCad file, hard tools were designed and screen have been fabricated. Fabrication will commence when the green tape punching has been completed by an outside vendor.

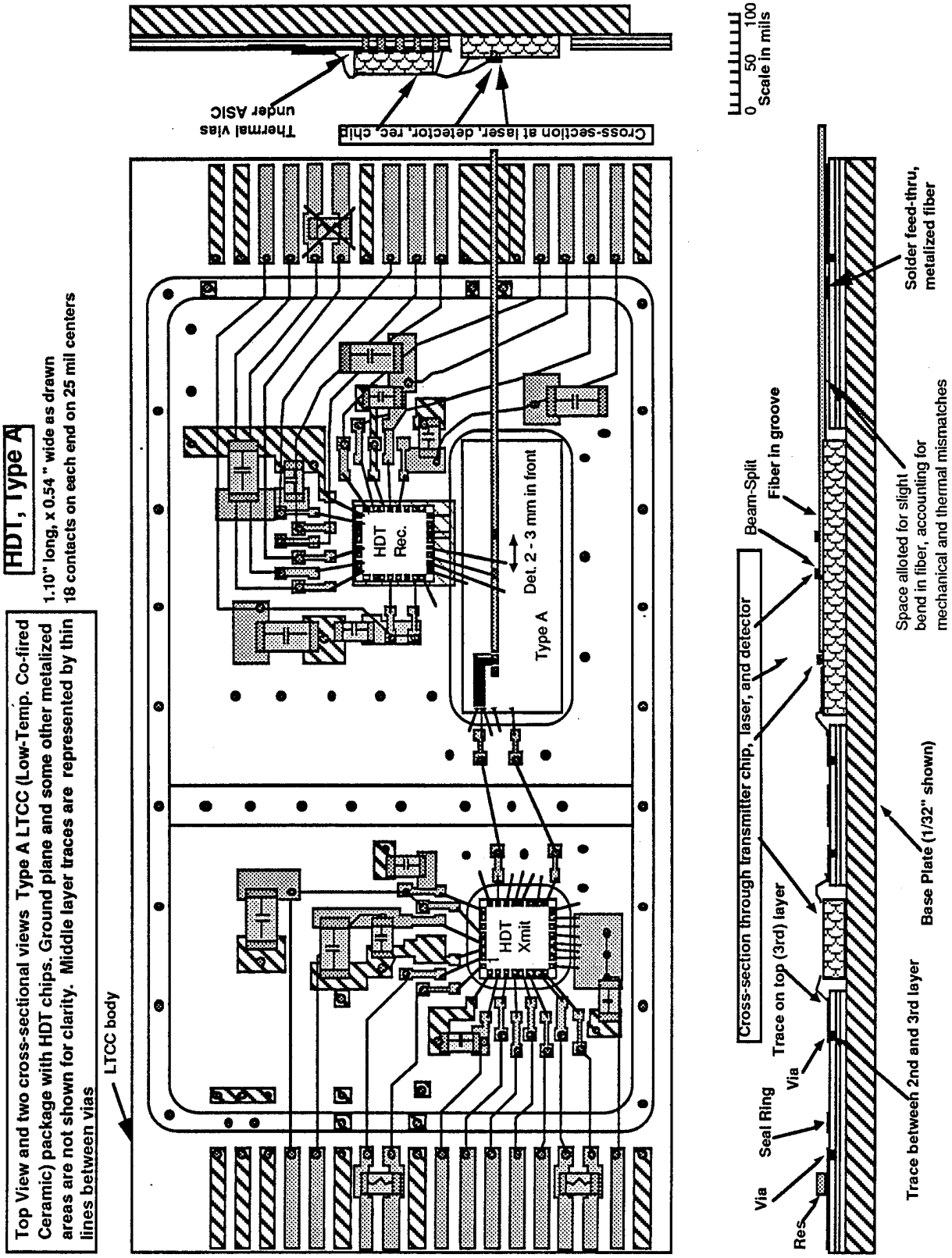

Figure III.1(a): Approved "A" design for the Optoelectronic Transceiver Module.

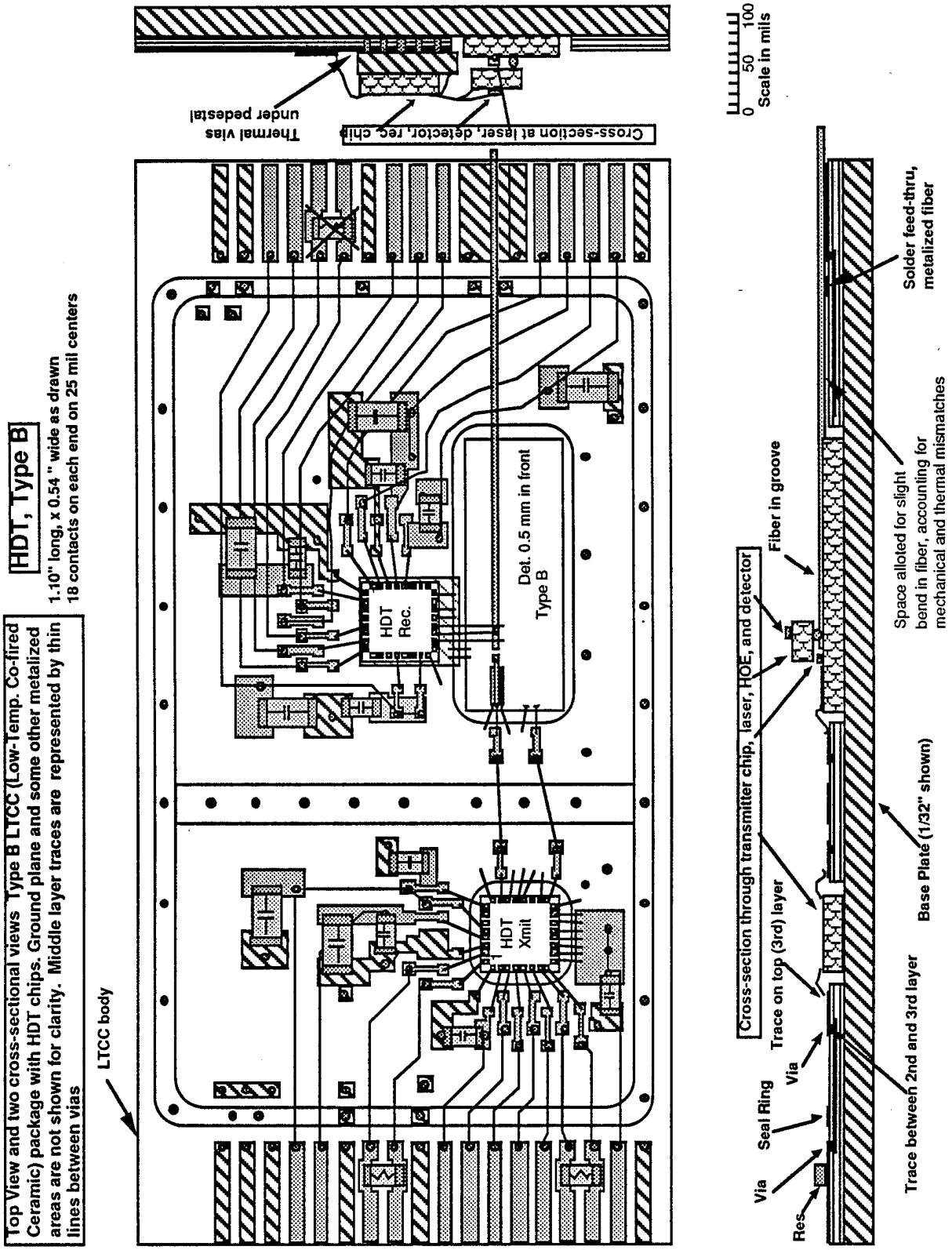

Figure III.1(b): Approved "B" design for the Optoelectronic Transceiver Module.

D. POWER AMPLIFIER PACKAGE

1. Task Objective

The objective of this task is to design, fabricate, assemble and test a low cost power amplifier package for a GaAs microwave device. The package will be designed, assembled and tested by Raytheon and fabricated by Sarnoff.

2. Introduction

This technology demonstration vehicle design was finalized during this past quarter. Vital to its design was the earlier design and fabrication of two test patterns, transmission lines and inductors. The 50Ω transmission lines fed out through a seal ring were measured from 2 to 50 GHz. The results are shown in Figure III.2. Design rules, critical for the fabrication of the prototype, were generated based on the information gained from these test patterns.

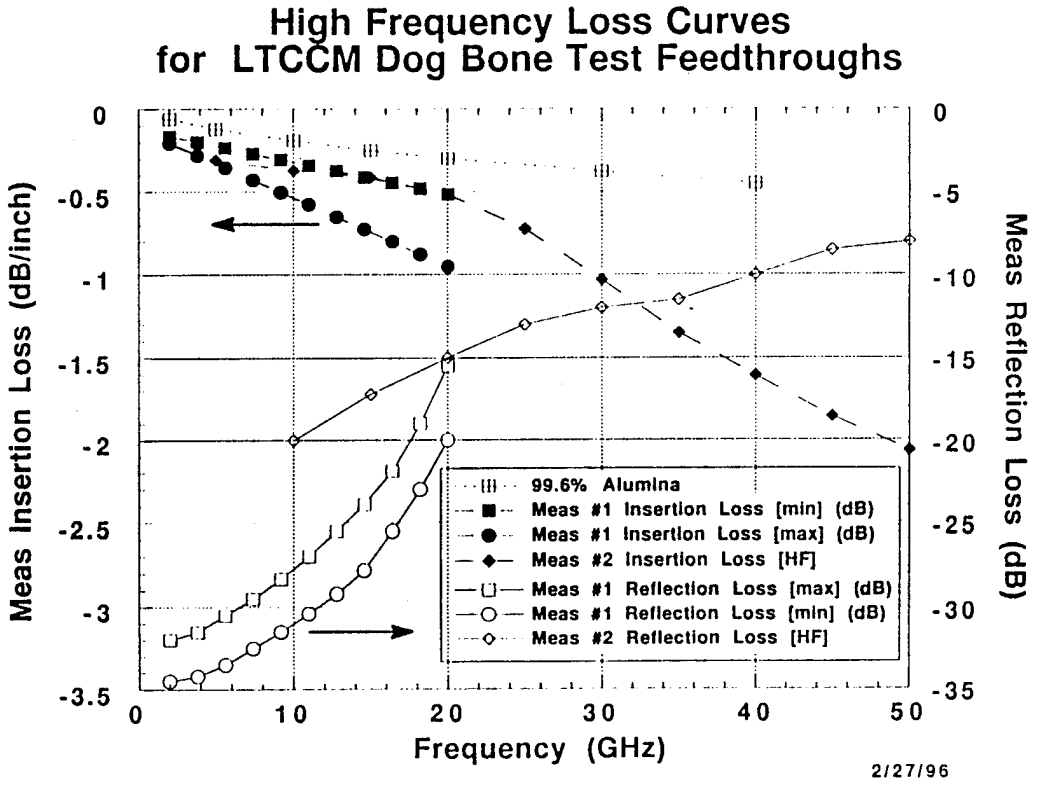

Figure III.2 High Frequency Loss Data for 50Ω transmission lines fed through a seal ring.

3. Inductor Test Circuits

As reported last quarter, inductor test circuits were fabricated but had not been tested. The inductor pattern consisted of 16 series inductors and 16 inductors connected to ground (shunt inductors). Series and shunt inductors are shown in Figures III.3 and III.4. The design values ranged from 2 to 34 nH. The line widths and spaces for all the inductors is 0.008". Six boards were fabricated at Sarnoff and three were sent to Raytheon for assembly and testing.

The series inductors were measured and their values were compared to the predicted data. As shown in Figure III.5, the measured results are very close the predicted values, especially for the larger value inductors. The self resonant frequencies ranged from approximately 1 GHz to 4.5 GHz, also shown in Figure III.5. The shunt inductors have not been measured.

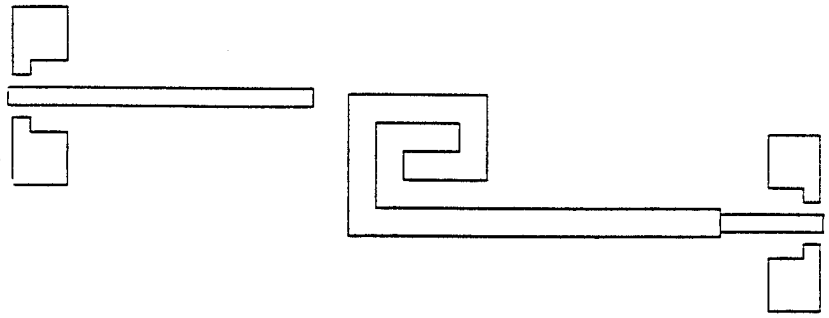

Figure III.3: Series Inductor.

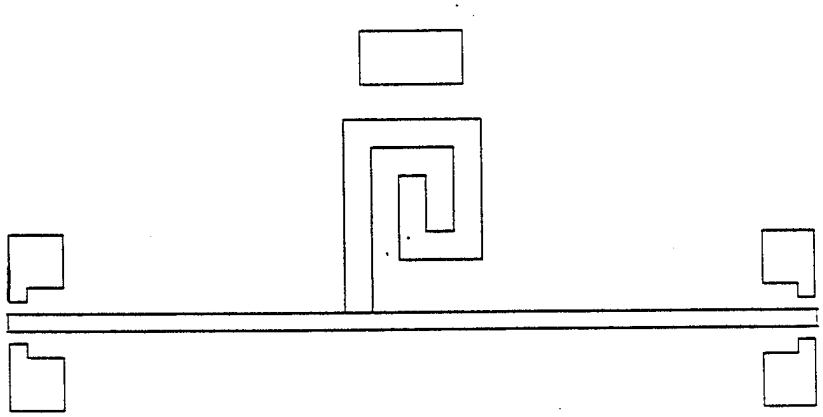

Figure III.4: Shunt Inductor.

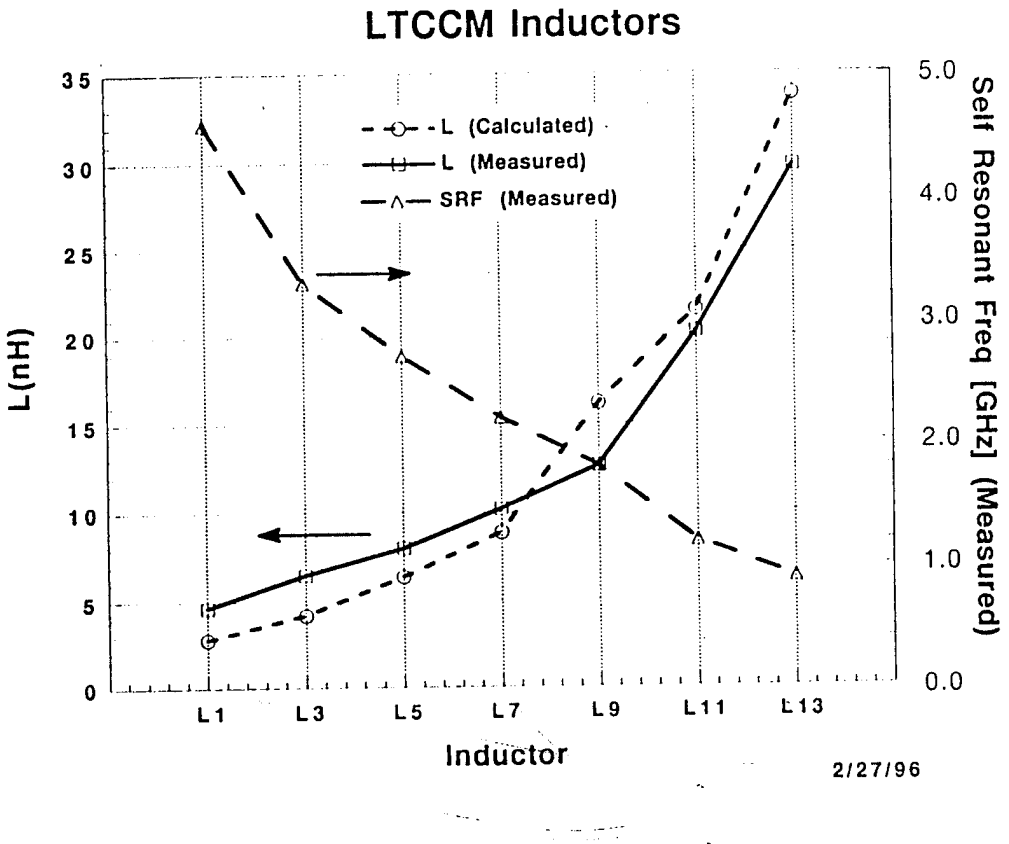

Figure III.5: Data measured for thick film series inductors.

4. Technology Demonstration Vehicle

A C-band power amplifier package has been chosen as the technology demonstration vehicle. The complete package is shown in Figure III.6. The size of the Cu/Mo/Cu base is approximately 1" x 1". Unlike the 50Ω line test package fabricated earlier in the program which used a Type 2 cavity, the C-band package requires a Type 3 cavity. A Type 3 cavity is a tiered cavity morphology where two separate laminates are stacked on top of each other with different cavity sizes. This is illustrated in Figure III.7 and III.8 which show the first and second laminates for the C-band package. The cavity for the bottom laminate extends all the way to the Cu/Mo/Cu base. The GaAs FET will be mounted in the cavity directly on the Cu/Mo/Cu.

An assembly test was performed to verify that the GaAs die attachment procedure would not conflict with the LTCC-M fabrication process. Typically GaAs die are attached in one of two ways, conductive epoxy for low power devices or Au-Sn solder for high power devices. Test boards with cavities from the 50Ω line package design were used. Actual GaAs chips and chip capacitors were attached using both methods mentioned above. The concern was for any thermal shock which might occur during the curing of the epoxy, 120°C for one hour, or soldering, 390°C. No delamination of the ceramic to the Cu/Mo/Cu base was observed.

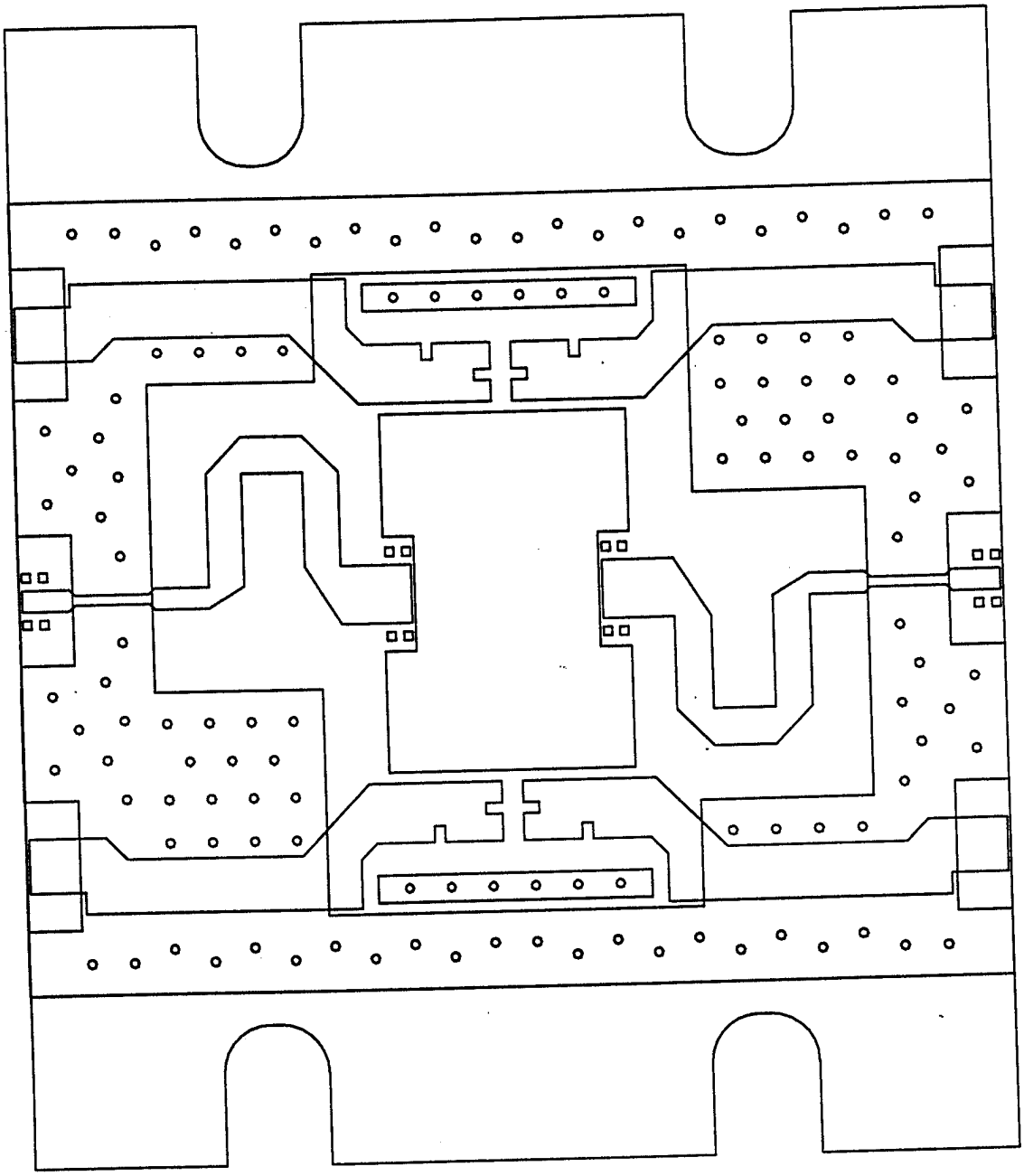

Figure III.6: C-Band package.

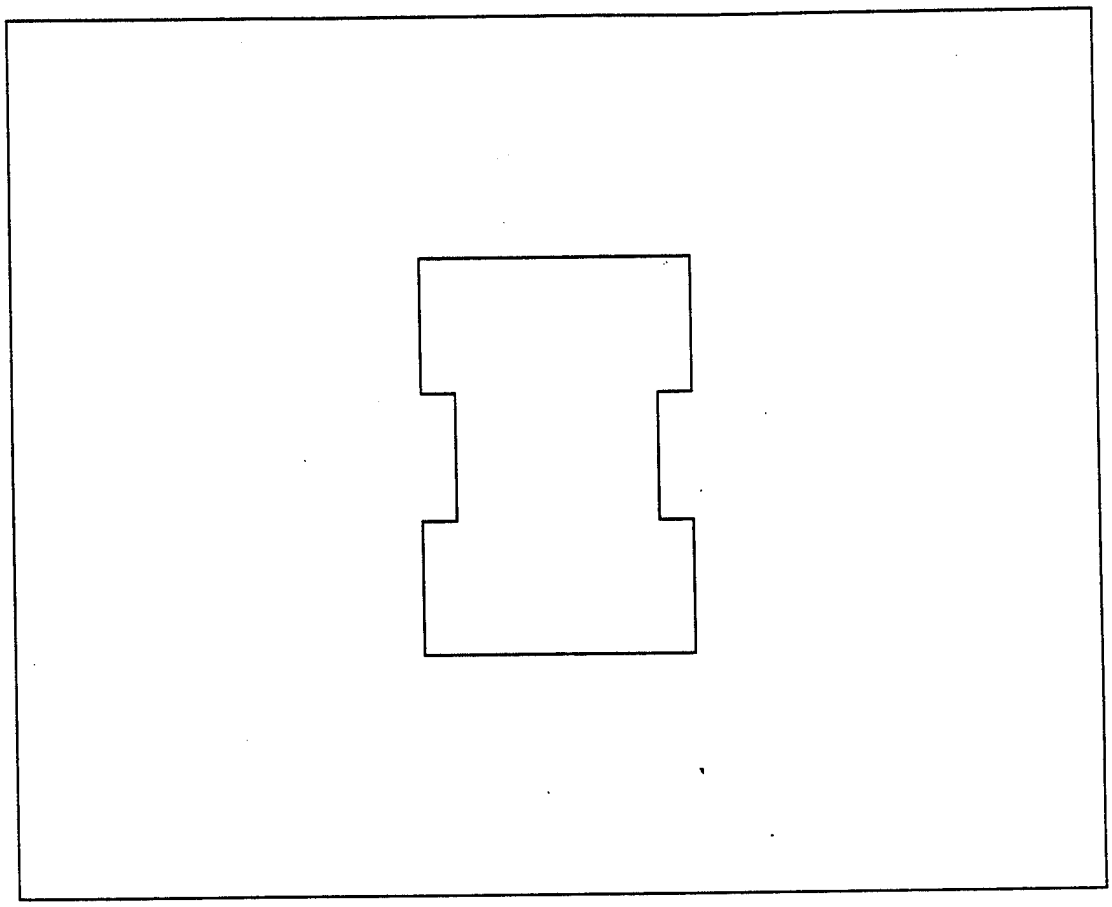

Figure III.7: C-Band 'lower' cavity pattern.

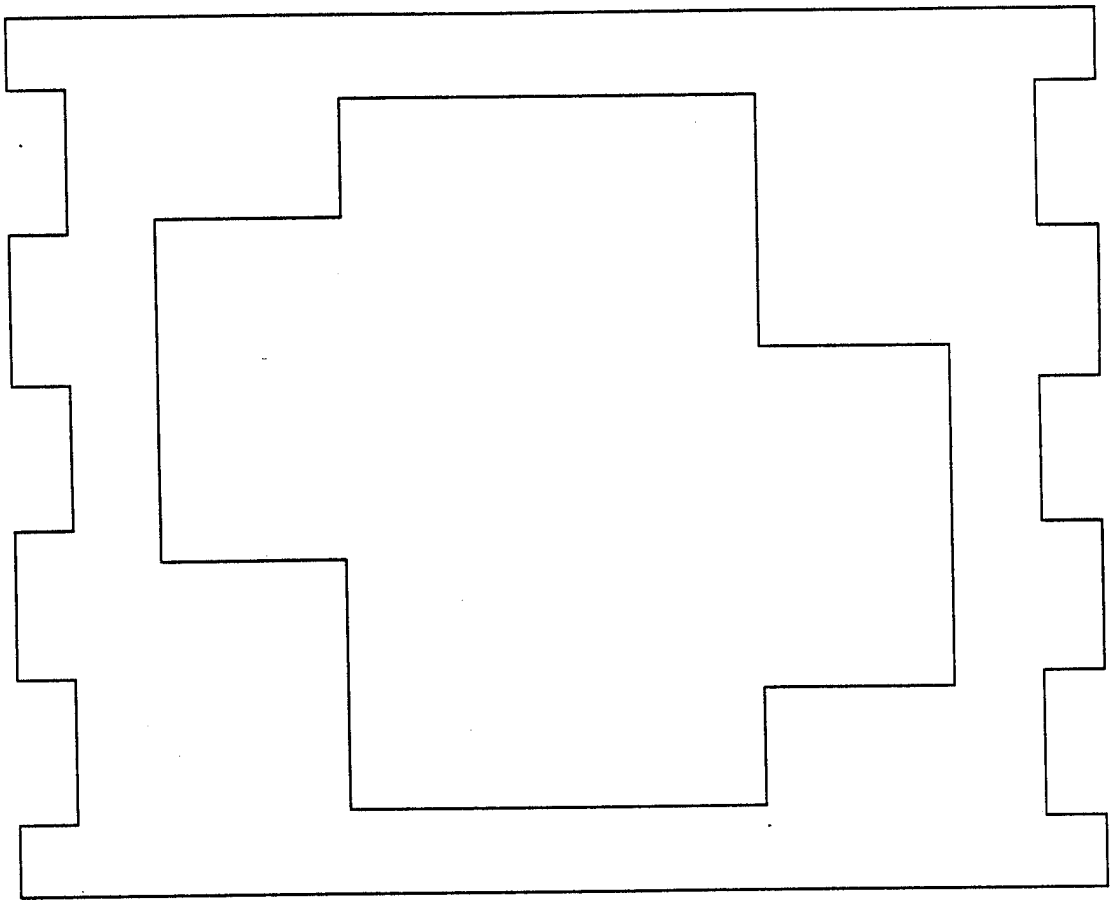

Figure III.8: C-Band 'upper' cavity pattern.

E. ADVANCED PCMCIA CARDS

Awaiting contract modification so design phase can begin.

F. POWER ELECTRONIC BUILDING BLOCKS (PEBB)

The objective of this task is to design, fabricate, assemble and test a low cost, PEBB "lid" in support of the U.S. Navy PEBB program. PEBB "lids" are high power device substrates that connect the power device to the control signals on a printed wiring board, yet are part of the thermal management system that draws the heat away from the device (and the printed wiring board). The "lid" package will be designed, assembled and tested by Harris and fabricated by Sarnoff.

Prior to design of the "lid" in LTCC-M, high voltage design rules must be established. Last quarter samples were supplied to Harris for measuring the high voltage breakdown strength of printed thick film AgPd conductors. These results are described below.

1. High Voltage Breakdown Data

As a part of the development effort for LTCC-M lid design rules for high voltage power electronic packaging applications an LTCC-M test substrate was designed, fabricated and tested. Specifically, the purpose of the effort was to determine the allowable distances between the metallized lands of power electrodes as function of device breakdown voltage ratings.

Description of the Test Vehicle

An LTCC-M substrate and its Ag/Pd co-fired metallization with Cu/Mo/Cu back plate was tested for its High Voltage Arcing characteristics. The LTCC-M high voltage test substrate consisted of a 6 layer, 0.25" thick LTCC co-fired over a 0.025" thick Cu-Mo-Cu plate with 0.0005" thick Ag/Pd top layer test pattern. The over all substrate size is 2.300" x 2.300". The test pattern consisted of an interdigitated lines with four different line spacings: 0.025", 0.050", 0.075", and 0.100". The approximate line length is 1.500" for all spacings.

Description of the test

The LTCC-M high voltage tests substrate was tested with a High Pot Tester-model #M120DC. The High Pot Tester is capable of applying 4000 V calibrated across its electrodes and it monitors the current level at 100 micro-ampere to determine the exact voltage of arcing. When the 100 micro-ampere current is registered across the high voltage electrodes the circuit under testing is considered unstable from high voltage arcing point of view.

All test circuits of the LTCC-M high voltage test vehicle were stressed as described above under two different test conditions.

1. In 14.7 psi, 70°F, and 40% RH room air.
2. Coated with 0.001" thick Dow Corning Sylgard 527 primerless silicone gel.

Results

The results of the high voltage arc resistance tests are tabulated below and displayed in Figure III.9.

Line Spacing (inch)	0.025	0.050	0.075	0.100
Arcing Voltage (V) - in air	2,455	2,840	3,200	4,010
Arcing Voltage (V) - coated with gel	>4000	>4000	>4000	>4000

The above results show that high voltage discrete power devices rated typically at 2000 V can be HTP packaged with LTCC-M lids having metallization patterns satisfying 100 V/mil criterion. However, the same test results also show that the design rules may be pushed to >160 V/mil if the package can be properly gelled to provide extra protection for dielectric breakdown.

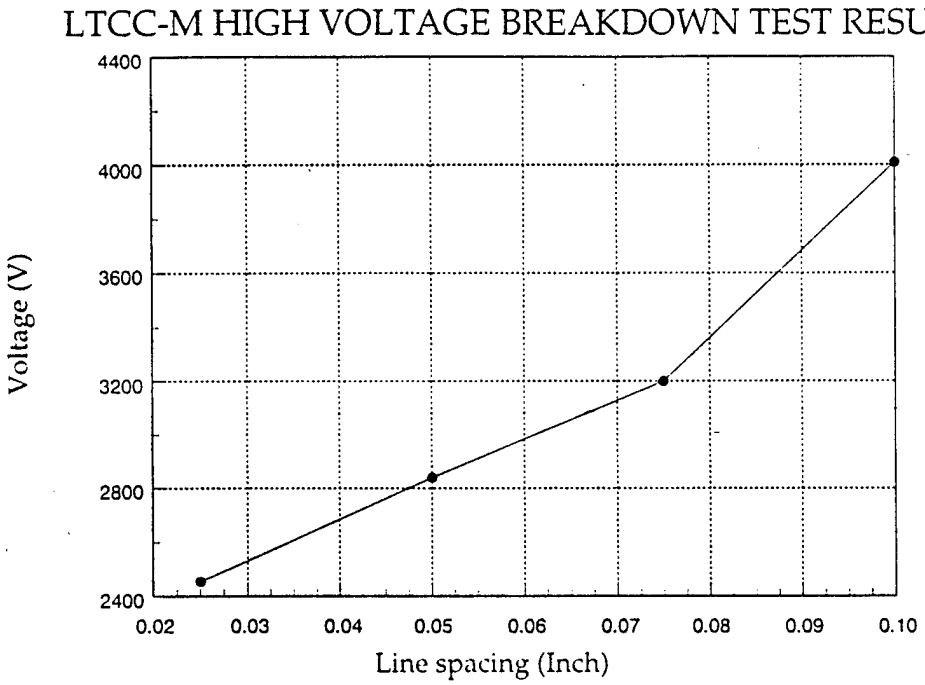

Figure 2. LTCC-M High Voltage test results

Figure III.9: LTCC-M High Voltage test.results

2. Patterning of Cu/Mo/Cu core after firing

The Cu/Mo/Cu core was patterned so that high voltage breakdown measurements could be made. Figure III.10 shows test pattern. These samples were prepared by Sarnoff for measurement by Harris. The surface high voltage breakdown data is expected next quarter. These samples were patterned by the elevated temperature etching procedure outlined below.

Last quarter an etching process was described for Cu/Mo/Cu cores, as depicted in Figure III.11. This quarter the process was extended to actual LTCC-M circuit boards having Ni-plated Cu/Mo/Cu, as illustrated in Figure III.12. In our initial trials with LTCC-M circuit boards, the Ni and Cu layers were removed with $FeCl_3$ or an acid mixture consisting of 1 HCl : 1 HNO_3 : 3 H_2O. The Mo is then removed by etching with an acid mixture consisting of 1 H_2SO_4 : 1 HNO_3 : 3 H_2O. Initially all acid mixtures were used at room temperatures. However it was noted that the etching varied significantly from sample to sample, and that there was severe undercutting of the gold etch mask. Additionally, it was noted that LTCC-M circuit boards developed a more etch resistant boundary layer between the Cu and the Mo. This is likely due to interdiffusion of the two materials during the cofiring operation. To overcome this etch resistant layer, the sulfuric acid containing mixture was heated. Figure III.13 shows the etch rate of metal cores of LTCC-M substrates as a function of bath temperature. When the bath temperature was raised above 60°C, the Mo etch bath would also etch the Cu and Ni at a high rates. Presently, controlling the bath temperature between 65 and 70°C, is allowing the LTCC-M metal cores to be patterned, without causing the Au etch mask to flake off.

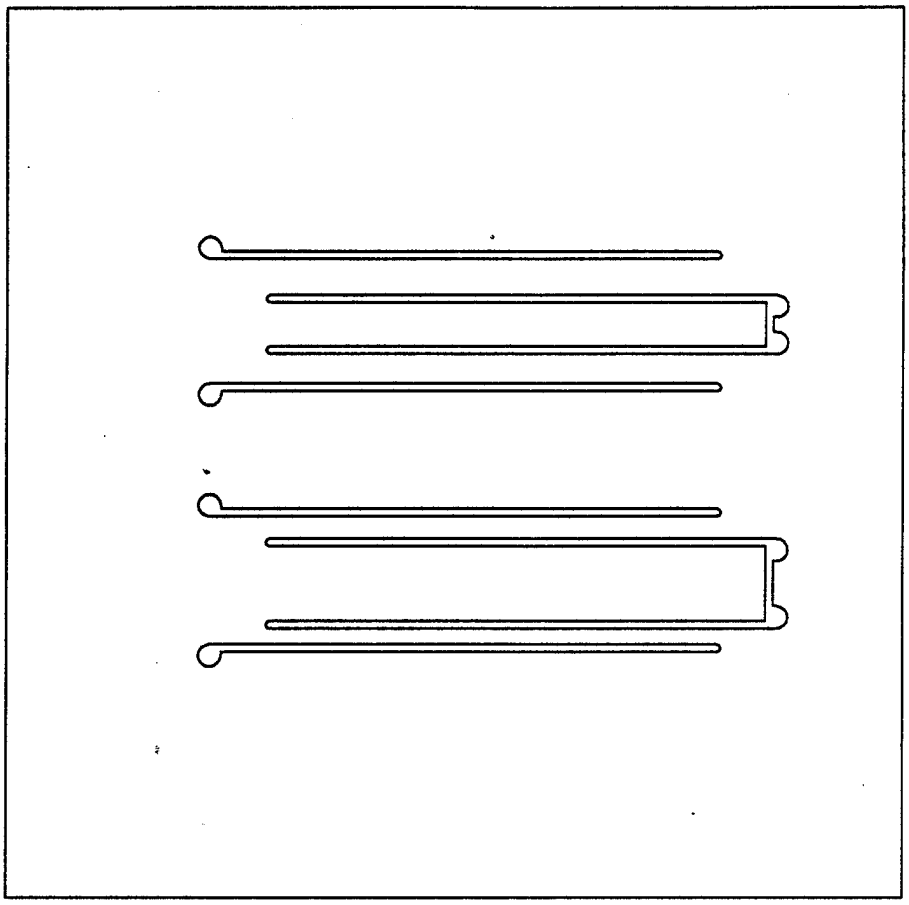

Figure III.10: High voltage test pattern

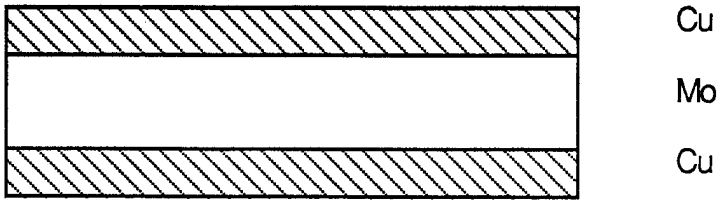

Figure III.11: Cross-section of test sample used last quarter

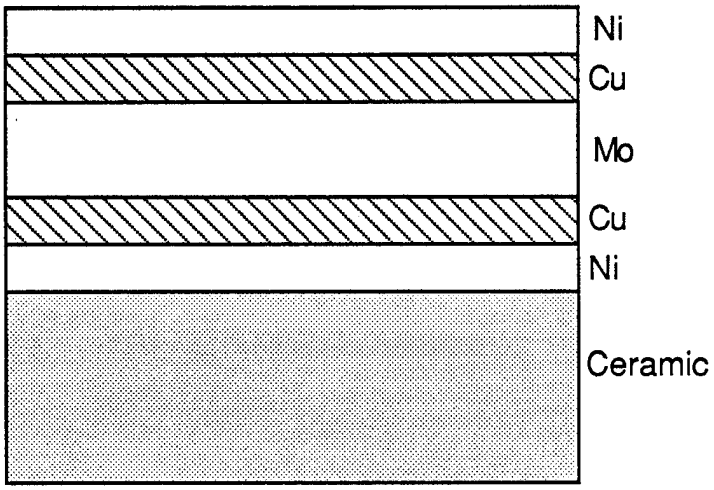

Figure III.12: Cross-section of LTCC-M sample

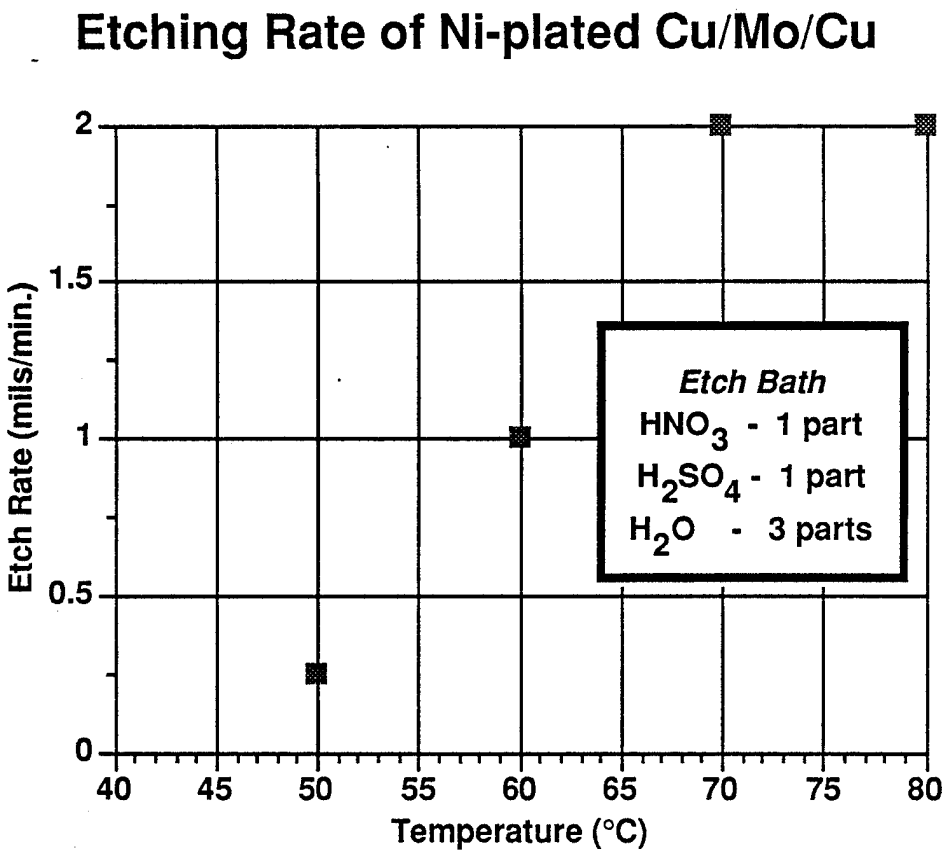

Figure III.13: Etch rate data for the metal core of an LTCC-M substrate

The PEBB lid was designed this past quarter. All tooling has been ordered, and delivery is expected to be complete in early April. At that point substrate fabrication can begin.

G. PLAN FOR NEXT QUARTER

Optoelectronic Transceiver Module

- Fabricate technology demonstration vehicle

Power Amplifier Package

- Order hard tooling
- Fabricate technology demonstration vehicle

Advanced PCMCIA Cards

- Complete design and layout
- Begin substrate fabrication

Power Electronic Building Blocks

- Complete etch mask design
- Fabricate technology demonstration vehicle

Section IV
Important Findings

A. TECHNOLOGY TRANSFER TO MERCHANT SUPPLIERS

- LTCC-M is a manufacturable technology when properly fired in a belt furnace.
- A programmable convection furnace cannot be readily substituted for a belt furnace with adequate (turbulent) airflow.
- Alcoa has demonstrated several LTCC-M process simplifications.
- LTCC-M material formulations and processing have been readily adapted to the glasses supplied by SEM-COM.

B. CUSTOMIZE LTCC-M FOR SPECIFIC APPLICATIONS

- A new cavity fabrication technique has been demonstrated that offers the following advantages:
    - Tape Handling: Handling of individually punched tape is far more difficult than a punched laminate. The total number of cavity punching steps is reduced down to one.
    - High Precision Cavities: Cavity precision achieved in this program represents the tightest of any MCM-C cavities. The dimensions are very tight, with the difference between the maximum and minimum cofired edge length being < 1 mil.
    - The cavity mechanical defects are eliminated or minimized. Profilometry measurements show that the lipping is < 1 μm on the top of the cavity.
    - Very Low Expansions (< 1 %): This result is also very significant as can result in lower manufacturing yields.
    - Always Expansion: Using this new technique, one always observes minimal expansion and never shrinkage relative to the punched cavity dimensions.
    - Eliminate complex lamination tooling conventionally used for complex cavity morphologies.
- Accelerated aging tests have shown high adhesion strengths for top conductors after more than 800 thermal cycles between -55°C and +125°C.
- Thick film spiral inductors have been printed with 4 mil wide lines.

C. FABRICATION AND TESTING OF TECHNOLOGY DEMONSTRATION MODULES

- Test structures of 50Ω transmission lines have measured by Raytheon and show good microwave properties into the mm-wave region.
- Thick film, spiral inductor test structures have been characterized by Raytheon at microwave frequencies; the data show good agreement with models, and exhibit self-resonant frequencies as high as 4.5GHz.

- The etching process developed for patterning 5 mil thick Cu/Mo/Cu, has been greatly accelerated and exhibits better feature control; it also shows promise for microwave applications.

Section V
Significant Developments

Alcoa Electronic Packaging, Inc. has announced their intent to exit the ceramic packaging business. Therefore, Sarnoff is examining other technology transfer options.

Section VI
Plan for Further Research

TECHNOLOGY TRANSFER TO MERCHANT SUPPLIERS

- Complete qualification of glasses G-14 and G-63, melted by SEM-COM

CUSTOMIZE LTCC-M FOR SPECIFIC APPLICATIONS

- Continue reliability testing of Ag thick film top conductors
- Fabricate additional daisy chain test patterns having 4 mil vias connected to 4 mil lines with 4 mil spaces
- Continue reliability testing of 4 mil via test structures

FABRICATION AND TESTING OF TECHNOLOGY DEMONSTRATION MODULES

Optoelectronic Transceiver Module

- Fabricate technology demonstration vehicle

Power Amplifier Package

- Order hard tooling
- Fabricate technology demonstration vehicle

Advanced PCMCIA Cards

- Complete design and layout
- Begin substrate fabrication

Power Electronic Building Blocks

- Complete etch mask design
- Fabricate technology demonstration vehicle

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The quarterly progress for the Ceramic/Metal Composite Circuit-Board-Level Technology for Application Specific Electronic Modules is described in this report. Data is reported for the following tasks: Technology Transfer to Merchant Suppliers, Customize LTCC-M for Specific Applications and Fabrication and Testing of Technology Demonstration Modules.

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