Cardiff School of Engineering
Electronics Division

5th European

University of Wales
Cardiff

HETEROSTRUCTURE TECHNOLOGY Workshop '95

17th - 19th September 1995
Aberdare Hall
CardiffWALES

HETEROSTRUCTURE TECHNOLOGY *Workshop*

Cardiff School of Engineering
University of Wales Cardiff

Sponsorship by the following is acknowledged

European Commission: Information Technology
European Research Office United States Army
Epitaxial Products International
Welsh Development Agency

CHAIRMEN
David Vernon Morgan
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ISBN1899337024

Printed and published by Graphic Services UWCC, P.O. Box 430, Cardiff CF1 3XT

HETEROSTRUCTURE TECHNOLOGY
WORKSHOP

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Workshop Programme

MONDAY 18th SEPTEMBER

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8.35 -10.30	SESSION A: Growth technology and characterisation
10.30-11.00	*Coffee*
11.00-12.30	SESSION B: Non- stoichiometric material applications
12.30-13.45	*Lunch*
13.45-15.20	SESSION C: Transistors I-HEMTs
15.20-15.50	*Tea*
15.50-17.30	SESSION D:Transistors II-HBTs
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TUESDAY 19th SEPTEMBER

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10.50-12.10	SESSION F: Device Technology
	CONCLUSION OF WORKSHOP
12.30	*Lunch and Departure*

HETEROSTRUCTURE TECHNOLOGY
WORKSHOP

SESSION A
Growth Technology and Characterisation

1 Technological elements for Diamond Electronics.
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2 Device quality InGaAs grown by MOVPE on Si(001)
H.H. Wehmann, G.P. Tang, A. Bartels, H. Iber and A. Schlachetzki.

3 MOCVD growth optimisation of InGaAs non-alloyed Ohmic contacts to n-GaAs
F. A. Amin, A.A. Rezazadah and S.W. Bland.

4 Pholuminescence and modelling of InAlAs-InGaAs channel-doped HFET material.
W.E. Leitch, B.H. Henle, E. Kohn and J Wood.

5 Highly sensitive Hall sensors using GaInAs/InAlAs pseudomorphic heterostructures.
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6 A Comparison of δ-doped quantum well structures for power FET applications.
J. M. Roberts, J.J. Harris and C. Roberts.

7 Local structural probes for surface analysis.
S.R. Burgess.

Technological elements for Diamond Electronics

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The mechanical, chemical and electronic properties of diamond are extraordinary. However, due to fundamental problems the device development lacks far behind that of most other semiconductors. Thus, diamond electronics will not easily be able to replace other electronic materials but will find applications, where the unique wide bandgap electronic behaviour is in one way or another connected to its excellent non-electronic properties , such as IR-transparency, thermal conductivity, elasticity, hardness and chemical inertness. Presently, there are five areas driving the technological developments:
Hard surfaces for mechanical use
Optical windows
Diamond tip field displays
Particle detectors for nuclear science
Thermistors, diodes and transistors for high temperature electronics

The first three applications use polycrystalline material or diamond/ graphite composites deposited on foreign substrates. This talk will focus on the use of monocrystalline substrates, growth of homoepitaxial layers and electronic device structures. These will determine the state of the art in performance. It will address problems and prospects for applications in the high temperature, power and sensing environment.

Diamond 100-oriented insulating as well as highly conductive substrates are commercially available (however, small in size) and the results presented here have been obtained on active homoepitaxially grown layers on these substrates.

The only active electronic dopants are boron, producing an acceptor with an activation energy of $\Delta E_a = 0.37$ meV above the valence band edge, and nitrogen, producing a number of deep donor levels, the most shallow one at $\Delta E_d = 1.6$ eV below the conduction band. The donor is therefore not active at room temperature and even the acceptor is not fully activated. Thus, carrier concentrations are highly temperature dependent. This is an advantage in the thermistor applications but needs to be eliminated in transistors. Experiments in this direction are discussed.
The second critical technological element is a high temperature stable contact technology for Ohmic as well as for control contacts such as Schottky diodes, MIS-diodes and p-n diodes. Diamond material may eventually be useful up to 900°C, where surface reconstruction may occur. Thus a contact technology is needed which can operate reliably at such temperatures. This limits the choice of materials. Here the temperature behaviour of Ohmics as well as Schottky contacts is discussed for a temperature of operation up to 600 °C (which is limited by the test set-up).
The devices presented are vertical Schottky diodes with a state of the art current switching ratio of the order of $I_F/I_R = 10^9$ and a mesa resistor fabricated on an insulating substrate suitable for implementation in a high temperature thermistor or FET structure.

DEVICE QUALITY INGAAS GROWN BY MOVPE ON SI(001)

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For the lattice-mismatched monolithic integration of $In_{0.53}Ga_{0.47}As$-based optoelectronic devices on Si substrates an optimized metalorganic vapourphase epitaxial (MOVPE) growth process is presented. The high quality of the active layer is demonstrated by various characterization methods.

Lattice-mismatched growth of III/V-compound semiconductors on Si opens up possibilities for monolithic integration of optoelectronic III/V-devices with Si-electronics. For its realization the differences in lattice constant (4% for GaAs and 8% for InP) and crystal symmetry (diamond – zincblende) as well as thermal expansion coefficient (164% for GaAs and 82% for InP) between layer and substrate has to be overcome. Since exactly orientated (001) substrates are mandatory in order to be compatible with Si-electronics, special care has to be taken to avoid the formation of antiphase domains [1]. The MOVPE growth process presented here was proven to be compatible with Si-MOS-technology [2]. As the direct growth of the ternary $In_{0.53}Ga_{0.47}As$ on Si is not possible by MOVPE, it is obvious to use InP as intermediate layer. However, apart from inevitable misfit and threading dislocations the main defects in InP-on-Si are microtwins. At the intersecting lines of these twinlamellae the surface morphology is disturbed causing growth defects in the following ternary layer. Since these two-dimensional defects hinder the motion of threading dislocations typical strings of etch pits can be seen on the InP-on-Si surface after Huber etching. On the other hand, in GaAs-on-Si the density of two-dimensional lattice defects is strongly reduced if three-dimensional growth is suppressed [3]. This was achieved by the small V/III-ratio of 4 during the growth of a 14 nm thick low-temperature (400 °C) buffer layer. Cross-section transmission electron microscopic (XTEM) investigations show this buffer as a homogeneous and uniform layer. Its optimum thickness and growth parameters were studied by means of spectroscopic ellipsometry similar to [4].

The buffer layer is followed by a 2.5 µm thick GaAs main layer grown at 700 °C and a V/III-ratio of 80. Its surface morphology strongly depends on the buffer quality and is best on that buffer whose optical properties are closest to GaAs-bulk. The step to InP again has to be carried out at

400 °C to avoid island growth. On the 80 nm thick InP buffer layer the InP main layer is grown at 640 °C to a thickness of 2.5 µm. The ensuing improvement is confirmed by a narrowing of (004) InP X-ray reflexes from 410 arcsec, when directly grown on Si, to 155 arcsec with GaAs intermediate layer. Although the density of microtwins traversing the whole layer could be greatly reduced the remaining lattice defects, mainly threading dislocations, deteriorate the growth of the InGaAs. These influences could be removed by inserting an InP/InGaAs superlattice (SL) consisting of 29 pairs of InP and InGaAs, each 6.6 nm thick. The surface is smoothened similar to [5].

The high crystallographic quality of the InGaAs-on-Si is demonstrated by its good surface morphology (Fig. 1). This is supported by a reduced width of the X-ray peak from 900 arcsec to 210 arcsec for a 1.8 µm thick InGaAs layer on InP-covered Si and on the optimized structure, respectively.

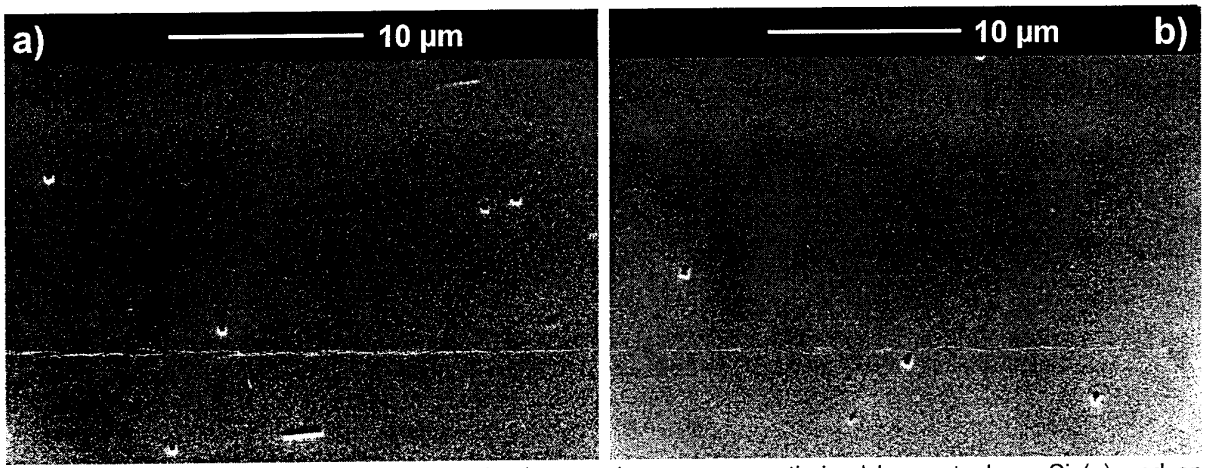

Fig. 1: Surface morphology of InGaAs simultaneously grown on optimized layer stack on Si (*a*) and on superlattice on InP (*b*).

To investigate the electronic properties of the lattice-mismatched layers we performed electrochemical capacitance-voltage profiling. The measured donor concentration in the GaAs layer is $3...4\times10^{15}$ cm^{-3}, whereas in the In-containing layers it is one order of magnitude higher. We found that a reduction of Si incorporation from the gasphase during growth, which is the main source besides interdiffusion from the heterointerface, can be accomplished by covering the Si substrate with SiO_2 [6].

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MOCVD growth optimisation of InGaAs non-alloyed ohmic contacts to n-GaAs

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Abstract: Traditionally, GaAs-based devices rely on ohmic contacts made to the n^+-GaAs cap layer, using metallization systems that incorporate doping constituents such as Ge. Since the Fermi level of GaAs is pinned at the metal-semiconductor interface at about 0.7-0.8eV, contact alloying is required to dope the cap layer to achieve low contact resistance. However, this technique causes bad surface morphology, loss of edge definition and lack of uniformity, making such contacts unsuitable for small geometry GaAs-based devices.

$In_{(x)}Ga_{(1-x)}As$ cap layer on n-GaAs is a non-alloyed contact system which is certainly favoured as a solution to the alloyed system. For InAs, the Fermi level is pinned in the conduction band, so effectively no barrier exists at the metal-semiconductor interface. As there is a large conduction band offset at the GaAs/InAs heterojunction interface, compositional grading from GaAs to InAs cap layer is necessary. Nevertheless, indium mole fraction graded from 0 to 0.5 is usually sufficient in practice for ohmic contact purposes, allowing one to obtain low resistance ohmic contacts without alloying. Since grading is essential and in addition, dislocations are usually generated in between the GaAs and the compositionally graded InGaAs layer, a high demand is placed upon the growth technology.

The best results that have been reported on InGaAs cap layers were grown using MBE since it is much easier to control the In composition in the graded layer to achieve a smooth conduction band profile. However, it is well known that for large volume production, it is more economic to use the MOCVD growth technique. The growth temperature in the MOCVD is critical, and we have carried out work to optimise these non-alloyed contacts by

by MOCVD at substrate temperatures of 600°C, 650°C and 700°C. End contact resistance TLM measurements on three samples were carried out using the Ni/AuGe/Ni/Au metallization system.

The variation of the specific contact resistance with substrate growth temperature has been studied. The results show that the best contact resistance was obtained for lowest growth temperature. The samples were then alloyed at various temperatures for 30 seconds using a rapid thermal alloying technique. Figure 1 depicts the variation of contact resistance with alloying temperature. It can be seen from this figure that the contact resistance is stable up to 350°C. After this temperature the contacts started to degrade probably due to the indiffusion of Au. The reliability in terms of the specific contact resistance degradation with respect to thermal stress for these contacts will be discussed.

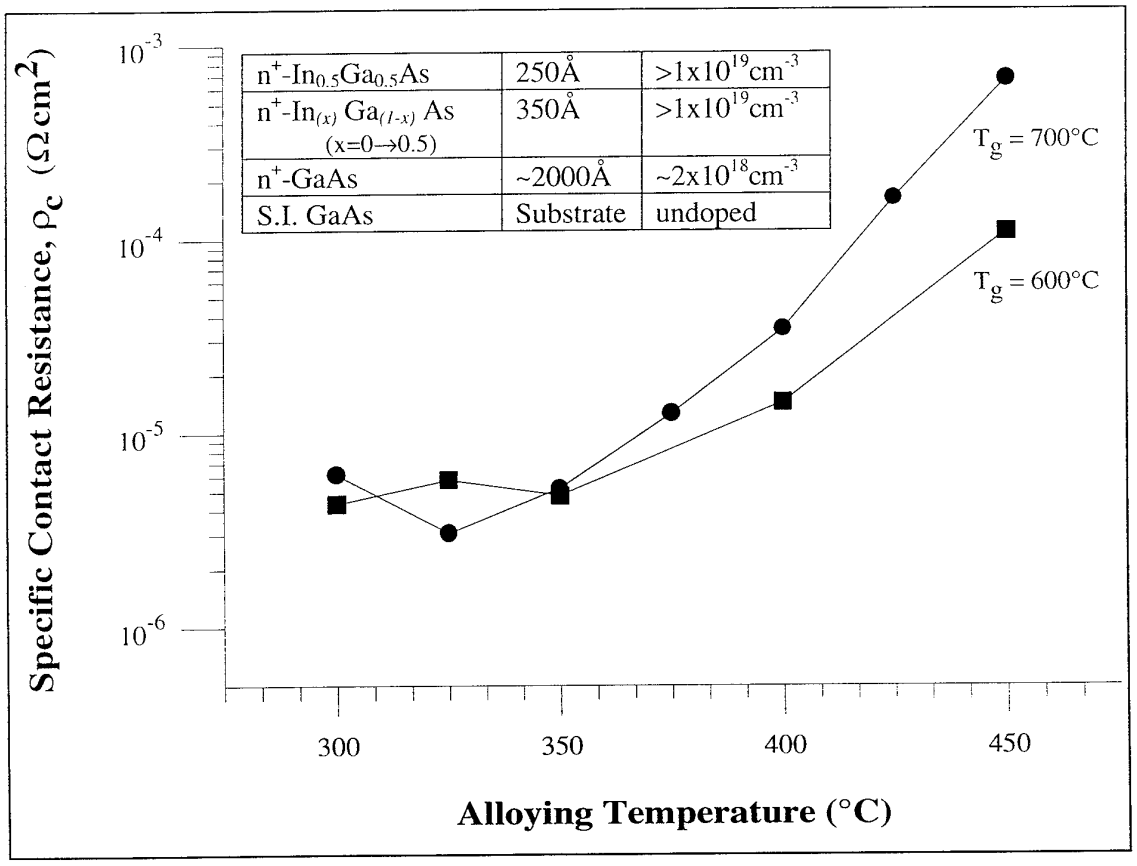

Figure 1: *Variation of contact resistance with alloying temperature using rapid thermal alloying for 30 seconds at each temperature*

Photoluminescence and Modelling of InAlAs-InGaAs Channel-Doped HFET Material

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The fabrication of Heterojunction Field-Effect Transistors (HFETs) requires stringent control of the crystal growth, and accurate models to optimize the device structure.

One of the most important design considerations in the growth of HFET material is the distribution of charge in the structure. The charge density in the channel must be maximized, whilst restricting the overspill into the barrier layers. In channel-doped HFETs, one attempts to maximize the channel charge density by introducing delta doping directly into the channel. In such highly-delta-doped structures, where the charge density in the delta-doping may exceeed 3e12 cm^{-2}, however, the measurement of the channel carrier density presents severe problems, and many conventional charge-control models, assuming a hydrogenic shallow level for the delta doping, underestimate the channel charge density by up to 50% as a result of carrier freeze-out [1]. Recent work on the modelling of the doping induced distortion to the conduction band density of states [2] suggests that a more appropriate model for these delta-doped-channel HFETs may be provided by assuming a complete ionization of the donors in the channel.

In the destructive conventional Hall technique, the measurement of the channel carrier density and mobility, independent of the charge in the supply layer and heavily-doped cap, is not possible. Techniques such as variable-field Hall measurement, and analysis techniques such as mobility spectrum analysis, provide useful information, but are unable to provide unambiguous measurement of channel carrier density. Similarly destructive Shubnikow-de Haas measurements provide accurate determination of the 2-dimensional electron gas density in the channel at low charge densities, but, at high charge densities and low channel mobilities, such as encountered in a doped-channel HFET, the oscillations are very weak. This is due to the strong dependence of the oscillation amplitude on the quantum time τ_q[3], which decreases rapidly with the ionized impurity scattering in such heavily-doped structures.

Photoluminescence analysis (PL), in contrast, gives a good measurement of the channel carrier concentration, and we have previously shown good agreement between the values of channel carrier concentration derived from PL, Hall, and Shubnikow-de Haas measurements in lightly doped structures [4,5]; here we show agreement between data from PL spectra and from a modified charge-control model for heavily doped structures.

In Figure (1), low temperature photoluminescence spectra from a single-sided-doped HEMT structure (a) with a doping of 8.6e12 cm^{-2}, and a channel-doped structure (b) with barrier doping of 5.7e12 and channel doping of 2.9e12 are depicted. Although the edge due to the n=1 transition is not depicted, peaks associated with the occupation of the n=2 and n=3 sub-bands are clearly seen. Values for the derived channel carrier density are tabulated in Table (1), together with the calculated values from the modified model assuming complete donor ionization in the channel.

Reasonable agreement is observed between the values obtained by the photoluminescence and those derived from the modified charge-control model for these structures. The values for the barrier doped structure are in better agreement than for the channel-doped structure: this is due to the lack of influence of the barrier delta on the channel density of states, whereas the channel-doped structure includes extra states in the channel at heavy doping.

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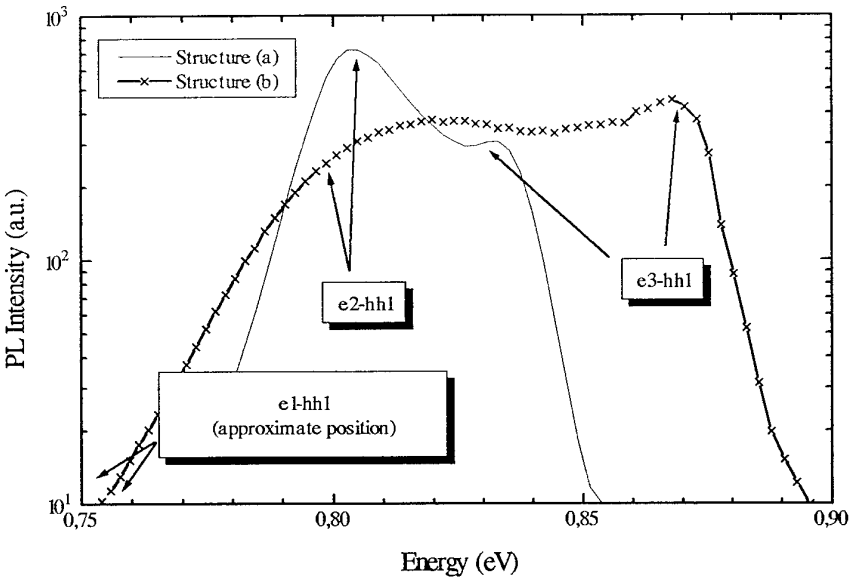

Figure (1): Photoluminescence Analysis of Heavily-Doped HFETs

Material	Barrier Doping	Channel Doping	PL	Model
(a) Barrier Doped	$8{,}6*10^{12}$	-	$(4{,}4\pm0{,}5)*10^{12}$	$4{,}69*10^{12}$
(b) Channel Doped	$5{,}7*10^{12}$	$2{,}9*10^{12}$	$(5{,}2\pm0{,}5)*10^{12}$	$5{,}90*10^{12}$

Table 1:
Channel Sheet Charge Density (in cm^{-2})

HIGHLY SENSITIVE HALL SENSORS USING GaInAs/InAlAs PSEUDOMORPHIC HETEROSTRUCTURES

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ABSTRACT

In this work, we propose solutions based on band gap engineering of III-V heterostructures to develop new types of magnetic sensors. The use of two-dimensional electron gas III-V pseudomorphic heterostructures seems to be an interesting solution to have both a high mobility and especially a low sheet carrier density. The latter condition is essential to obtain a high magnetic sensitivity. With a growth optimization of pseudomorphic $In_{0.75}Ga_{0.25}As/In_{0.48A}l_{0.52}As/InP$ heterostructures by molecular beam epitaxy, a low sheet carrier density of $9.84x10^{11}$ cm^{-2} at room temperature has been obtained. Two structures were realized with different layer thicknesses and Si doping (Figure 1).

$In_{0.53}Ga_{0.47}As$	70 Å	$n = 10^{18}$ cm^{-3}
InAlAs LM	L_B, N_B	
InAlAs LM	50 Å	nid
$In_{0.75}Ga_{0.25}As$	100 Å	nid
InAlAs LM	4000 Å	nid
InP S.I.	substrate	

Figure 1 : Cross-sectional view of the structure. (L_B : barrier thickness, N_B : barrier doping level, LM : lattice matched, nid : non intentionnally doped, S.I. : semi-insulating)

To understand better the influence of the heterostructure design on its electronic properties, a model involving the self-consistent solution of the Poisson and Schrödinger equations using Fermi-Dirac statistics has been developed. These results have been used to optimize the structure design.

A magnetic sensitivity of 580 V/AT with a temperature coefficent of -550 ppm/°C between -80°C and 85°C has been obtained. The device show good linearity against magnetic field in the investigation range (± 0.3 T) and also against the supply current (Figure 2 and 3).

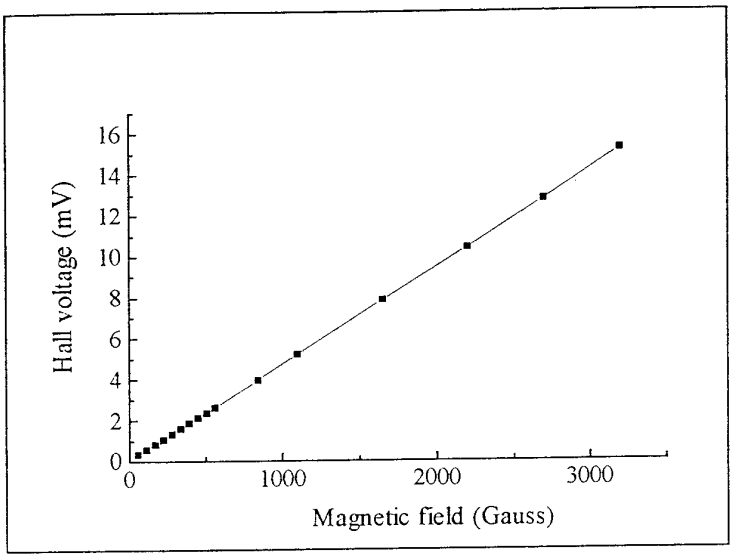

Figure 2 : Dependence of the Hall voltage on the magnetic field at a supply current of 100 μA

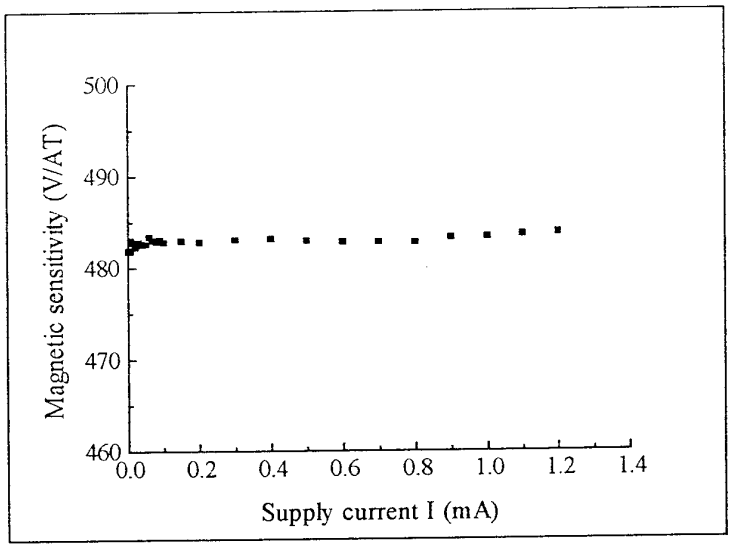

Figure 3 : Magnetic sensitivity against supply current at a magnetic field of 0.11 T

Voltage fluctuations across the Hall electrodes have been measured at zero magnetic field as a function of frequency. High signal-to-noise ratios corresponding to minimal magnetic field of 350 $nT/Hz^{1/2}$ at 100 Hz and 120 $nT/Hz^{1/2}$ at 1 kHz have been measured.

A COMPARISON OF ∂-DOPED QUANTUM WELL STRUCTURES FOR POWER FET APPLICATIONS

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We present a systematic study of the effects of material composition and Si ∂-doping plane position on the transport properties of several ∂-doped GaAs/AlGaAs and InGaAs/AlGaAs quantum well structures. The intention is to determine the design rules for a high carrier concentration, high mobility structure suitable for high frequency power FET applications.

Previous works on ∂-doped structures have generally shown low carrier mobilities due to the high levels of ionised impurity scattering present, a result of the spatial coincidence of the electrons and donors. Self-consistent Poisson-Schrödinger modelling suggests that by edge doping the quantum well an electron-donor separation is created which should decrease the ionised impurity scattering thus improving carrier mobilities. Such separations are further increased by compositionally grading the quantum well. Measurements indicate improvements in the low field carrier mobilities of up to 60% when these features are incorporated into a quantum well. The improvement in the mobility is accompanied by a 50% increase in the electron saturation drift velocity. Optimisation of these structures should produce further improvements in the mobility. Transport measurements also show a reduction of up to 40% in the carrier concentration in these structures due to Fermi level pinning; this is believed to be a result of DX centres or other Si-related states [1]. Results of the dependence of Fermi level pinning and carrier mobility on dopant configuration and quantum well composition will be presented.

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LOCAL STRUCTURAL PROBES FOR SURFACE ANALYSIS

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ABSTRACT

For the epitaxial growth of Ge on Si the 4.2% lattice mismatch leads to a Stranski-Krasanov growth mode i.e. the first few monolayers are in layer by layer growth mode followed by the formation of Ge islands. Often, by introducing a thin layer (≤ 1ML) of surfactant (arsenic, antimony or tellurium), thick epitaxial Ge layers can be grown on Si substrates. The use of tellurium as a surfactant to aid the growth of epitaxial germanium layers on Si(100) substrates is of great interest, as subsequent CdTe epilayers adopt a (100) orientation as opposed to the (111) orientation displayed when grown directly on Si(100). This system is particularly important for mercury cadmium telluride (MCT) devices on silicon, where the CdTe serves as a buffer layer for the growth of high quality MCT. Therefore, the technology developed for Si processing can be used for systems containing MCT devices. In epitaxial growth simple surface structural parameters, such as bond lengths and adsorption sites, are important prerequisites in order to understand the mechanisms of surfactant aided growth. In this work we present a structural study of the Te/Si(100) (1x1) surface phase using surface extended x-ray absorption fine structure (SEXAFS) and x-ray standing wave (XSW) spectroscopies

The (1x1) Te/Si(100) structure was generated by depositing a thick layer (~100Å) of CdTe onto a clean Si (2x1) double domain surface, and annealing the sample to 350°C. The SEXAFS results indicated that the Te atoms sat in 2-fold bridge sites directly above a fourth layer Si atom. The corresponding bond length was measured to be (2.52 ±0.05)Å. The XSW measurements of the (400) reflection gave a coherent position of (1.63±0.03)Å and a coherent fraction of 0.65. This is consistent with the breaking of the Si-Si dimers and thus, could be an example of the phenomena of adsorbate-induced dereconstruction of the surface. These results are compared with those of Bennet *et al* who examined a similar system using soft x-ray photoemission (SXPS) and the STM study ofYoshikawa et al.

HETEROSTUCTURE TECHNOLOGY
WORKSHOP

SESSION B
Non-stoichiometric material applications

1 Properties of semi-insulating MBE GaAs layers for device passivation.
J. Betko. A. Forster, M. Morric, M.Mars, J. Norvak and P. Kordos.

2 Electrical surface passivatoin of GaAs power MESFETS with Low-Temperature grown AlGaAs.
N. X. Nguyen, J. P. Ibbetson, W.N. Jiang and U.K. Mishra.

3 Low Temperature grown AlGaAs: A material to study the arsenic antisite defect absorption in an extended spectral range.
M. Ruff, D. Streb. S.U. Dankowski, P. Kiesel, M Kneissl, U.D. Keil, A.K. Verma and A. H. Dohler.

4 Electro-optic effects for above bandgap energies in Low Temperature grown GaAs.
S.U. Dankowski, D. Streb, M Ruff, P. Kiesel, U.D. Keil, B. Knupfer, M. Kneissl, N. Linder and G.H. Dohler.

5 Capacitance behaviour of Low Temperature grown GaAs/n- GaAS structures.
H. Thomas, J. K. Luo, D. Westwood and D.V. Morgan.

6 Recent Developments in HFET devices employing σ-LT-GaAs.
K.M. Lipka, M. Birk. H. Heinecke, J. Schneider, B. Splingart, R. Westphalen and E. Kohn.

Properties of semi-insulating MBE GaAs layers for device passivation

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Semi-insulating GaAs is often needed as a buffer or passivation layer and different preparation procedures are now under development. LT MBE GaAs (T_g = 200–300 °C) exhibit resistivity as high as 10^6 Ω cm after annealing [1]. Recently, it has been found that MBE GaAs deposited at 400–450 °C has comparable properties to SI bulk GaAs [2] with room temperature resistivity of ~10^7 Ω cm even in as-grown state [3]. However, detailed transport and insulating properties of such SI layers have not been studied yet.

We performed temperature dependent conductivity and Hall-effect measurements on MBE GaAs layers grown at temperatures in the range between 200 and 450 °C. Obtained results can be summarized as follows:

- It is necessary to separate the layers from their substrates in order to obtain correct conductivity and Hall-effect data because the sheet resistivity of the layer is much higher than that of the substrate. The method based on wet chemical etching, which allows to separate GaAs layers of thicknesses down up to 1μm, will be demonstrated.
- MBE GaAs layers grown at 400–450 °C exhibit SI properties with room temperature resistivity and Hall mobility of $7*10^6$ Ω cm and $6*10^3$ cm^2/V s, respectively. Similar donor level with an activation energy of 0.68 eV has been found in these layers as well as in as-grown and annealed LT GaAs (Fig. 1), which indicates that rather deep donors than arsenic precipitates are responsible for high resistivity of LT GaAs.
- MBE GaAs layers grown at 400–450 °C exhibit other breakdown behavior than LT GaAs. In 400–450 °C layers a sublinear region $I \sim U^{0.5}$ followed by a sharp breakdown exists while in LT GaAs a soft breakdown occurs (Fig. 2). The breakdown field of 400–450 °C layers is ~60 kV/cm, lower than that of LT GaAs but still higher than of SI bulk GaAs which indicates that the layer non-stoichiometry playes role at the insulating properties of GaAs.

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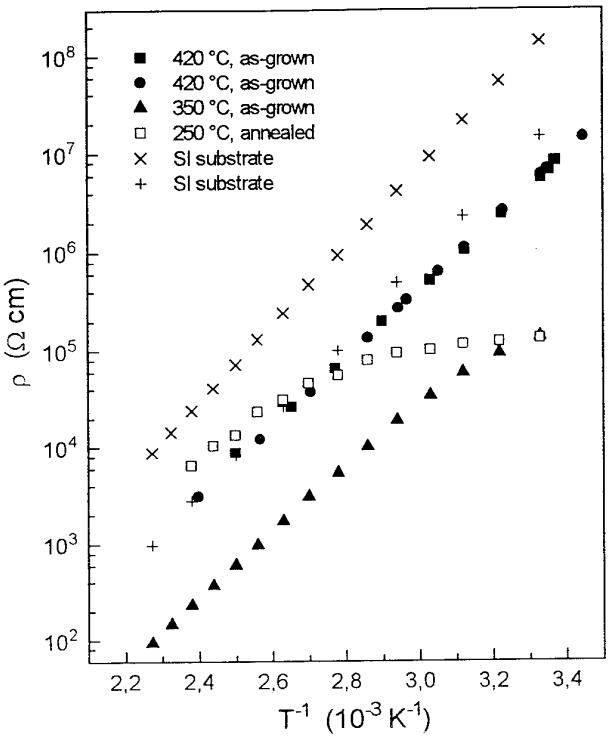

Fig. 1. Resistivity vs inverse temperature for GaAs layers grown at 420 °C in comparison with LT GaAs layers and SI bulk GaAs.

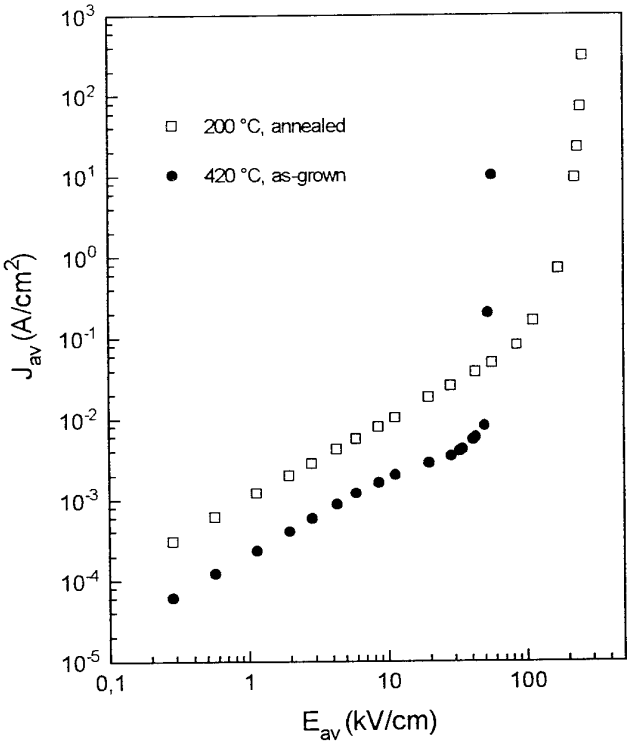

Fig. 2. Current density vs electric field for 420 °C grown GaAs layers and LT GaAs layers (T_g = 200 °C).

Electrical Surface Passivation of GaAs Power MESFETs with Low-Temperature-Grown (Al)GaAs

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Abstract

Theoretical studies have led to the conclusion that the surface plays a crucial role in the device characteristics of GaAs MESFETs. In particular, for microwave power MESFETs , the surface intimately influences the device's power performance via the breakdown voltage and device stability. Over the years, various surface passivation schemes have been investigated and applied to devices; currently, SiN is the standard passivant of GaAs FETs in industry. Although SiN is an effective environmental passivant (preventing the change of the surface properties due to environmental factors such as oxidation and humidity), it is not an electrical passivant (does not effectively terminate the dangling bonds on the surface), as schematically shown in Figure 1. Recent progress in the research of Low-Temperature-Grown(LTG) GaAs and related materials has demonstrated the effectiveness and suitability of these materials as electrical passivants in devices Record breakdown voltages and power performances have been achieved in GaAs MESFETs with LTG-(Al)GaAs surface passivation.

In this work, we report on the effects of LTG-passivations on the figures-of-merit for GaAs power MESFETs. Utilizing LTG-AlGaAs passivation, we have designed and fabricated state-of-the-art GaAs power MESFETs. The high performance abtained from these devices demonstrated the advantages that were gained in applying LTG material for surface passivation. A schematic cross-sectional profile of the epitaxial structure is shown in Figure 2. The device delivered 1W/mm at 4 GHz with a power-added-efficiency of 30% (Figure 3). The DC characteristics of the device (Figure 4) show a maximum drain current of 480 mA/mm and a gate-drain breakdown voltage of 20V.

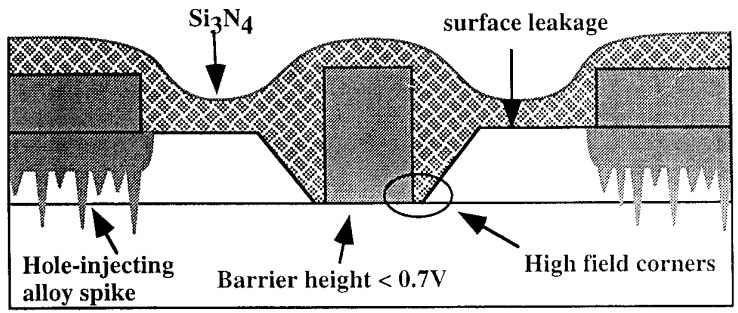

Figure 1 : Schematic cross-section of a nominal GaAs MESFET in industry with weaknesses.

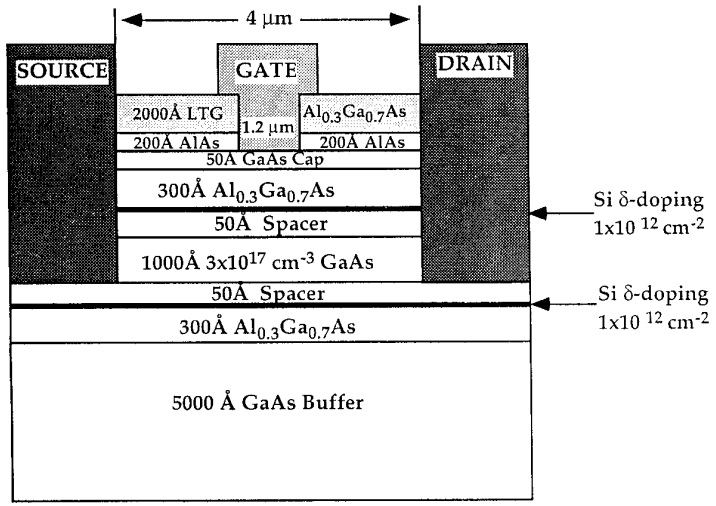

Figure 2 : Cross-section profile of a MESFET with LTG-AlGaAs passivation.

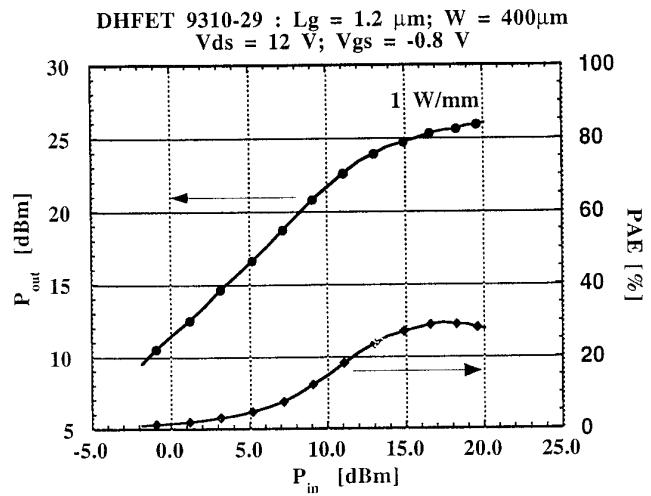

Figure 3 : On-wafer CW power performance measured at 4 GHz.

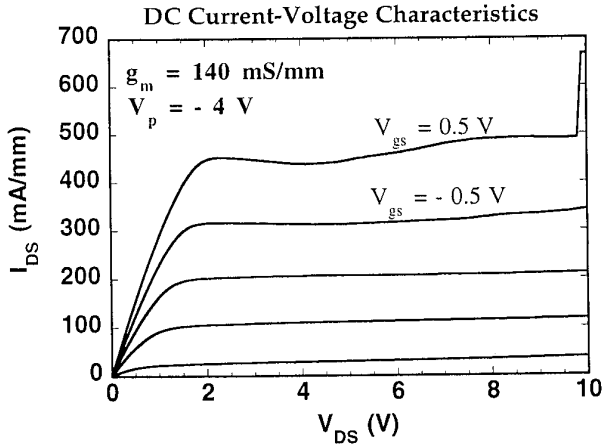

Figure 4 : DC device characteristics at room temperature

Low Temperature Grown (Al)GaAs - A Material to Study the Arsenic Antisite Defect Absorption in an Extended Spectral Range

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MBE-GaAs grown at low substrate temperatures (LT-GaAs) is known to exhibit outstanding properties, like femtosecond recombination life-times for photo-induced carriers in the as-grown state[1] and semi-insulating behaviour up to $10^7\Omega$cm after annealing[2]. These remarkable features make LT-GaAs and related materials like LT-AlGaAs very appealing for various applications like THz-spectroscopy and ultrafast photo-detectors[6]. Low substrate temperatures (180°C to 250°C) and Arsenic overpressure during MBE-growth cause up to 1% excess As (10^{20}cm^{-3}) in LT-materials[3] which leads to high concentrations of Arsenic-Antisite (As_{Ga}) defects. This defect is very similar to the well known EL2-defect observed in Liquid Encapsulated Czochralski (LEC) grown GaAs, but there is still a lack of clarity about its atomic structure and the mechanism of its metastable state.

One common technique to characterise the EL2-defect is to perform sub-bandgap infrared absorption (IRA) experiments. In contrast to LEC-grown GaAs the defect concentration in LT-(Al)GaAs is high enough to extend the IRA experiments to above bandgap energies by using very thin layers of LT-material. To separate these thin LT-layers from the GaAs substrate we used an epitaxial lift-off technique for the LT-GaAs samples (1.5μm thickness) and selective etching for the LT-AlGaAs samples (1μm thickness). For reference measurements we used a 1.5 μm thick standard MBE GaAs layer grown at 580 °C.

By annealing the LT-(Al)GaAs samples at temperatures from 400°C to 600°C in a rapid thermal annealer under N_2-atmosphere for one minute the EL2-like As_{Ga} defects convert into As-clusters[4].

Fig.1a and 1b show the results of the transmission measurements of both LT-samples performed over a broad spectral range (620nm to 1500nm) at room temperature. Below the respective bandgap energy the complete absorption is due the immense amount of defects created by the excess As. The fringes in this energy range are caused by interference effects of the air - LT-GaAs (LT-AlGaAs) - glass interfaces which acts like a Fabry-Pérot resonator. To weaken these Fabry-Pérot oscillations (FPO) we used a SiO anti reflection coating (ARC). With increasing annealing temperature the absorption in the sub-bandgap energy range vanishes. The shift of the FPO extrema towards higher energies indicates an annealing induced refractive index change ($\Delta n \approx 0.2$) which is reported elsewhere[5]. Even for energies above bandgap there is a decrease of absorption by annealing the samples.

Furthermore it can be seen that with increasing annealing temperature the absorption spectra of LT-GaAs become more similar to the spectrum of standard MBE GaAs. In particular the absorption edges at 1.42eV and 1.75eV (split-off band) become substantially sharper.

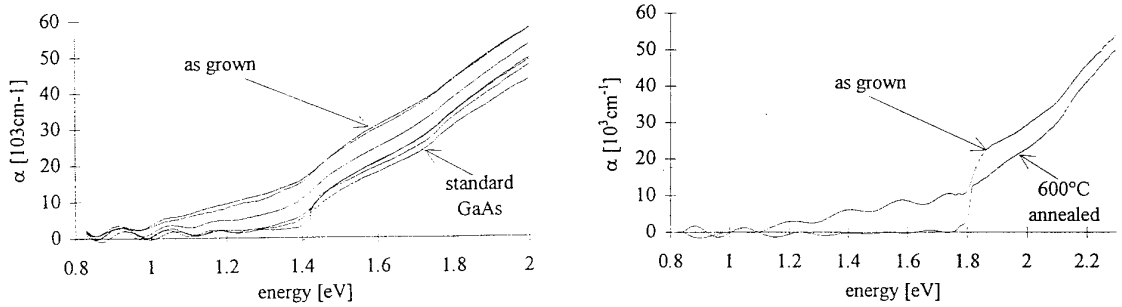

Fig.1 Absorption coefficient α of a) as grown, 400°C, 430°C, 470, 500°C and 600°C annealed LT-GaAs samples and of b) as grown and 600°C annealed LT-$Al_{0.3}Ga_{0.7}As$.

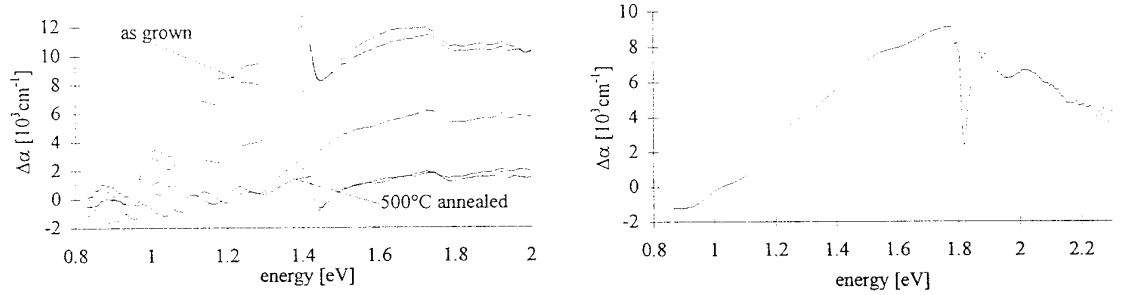

Fig.2 Absorption coefficient change Δα due to annealing a) relative to the 600°C annealed LT-GaAs sample and b) relative to the 600°C annealed LT-$Al_{0.3}Ga_{0.7}As$ sample.

Figure 2a shows the annealing induced absorption change Δα of the LT-GaAs samples relative to the 600°C annealed sample. The sharp band edge of the annealed sample leads to a broad peak of $\Delta\alpha \approx 12.000\ cm^{-1}$ at $\hbar\omega \approx 1.4eV$. The broadened band edge of the weakly annealed samples could be caused by a lattice strain induced broadened and shifted intracenter transition between the ground state EL2° and an excited state. This is confirmed also by the work of Kaminska et al.[3], who observed an enhanced bleaching efficiency of the EL2-like defect in as grown LT-GaAs at energies around 1.4eV. A slightly different behaviour is observed for the LT-AlGaAs samples shown in Fig.2b. The absorption change between the as-grown and the 600°C annealed sample reaches its maximum of $9.000cm^{-1}$ at the band-gap energy of 1.8eV.

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Electro-optic effects for above bandgap energies in low temperature grown GaAs

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We investigated room temperature electro-optic effects on LT-GaAs (low temperature grown) based MSM-Detectors (Metal-Semiconductor-Metal) which were lifted off from the substrate. Therefore we were able to observe Franz- Keldysh oscillations at the fundamental gap as well as at the gap between the split-off valence band and the conduction band. We obtained a transmission ratio of 1:1.3, corresponding to a change of the absorption coefficient of 2300cm^{-1} averaged over the total thickness. In agreement with theoretical expectations the absorption is clearly polarisation dependent at the fundamental gap, but only weakly at the split-off gap.

LT-GaAs is known as a material which is very suitable as a semi-insulating layer after annealing. It exhibits an eminent break through field larger than $5 \cdot 10^5$ V/cm, an extremely low lifetime of photoexcited carriers (<1ps) and a high specific resistance of up to 10^7 Ωcm. These properties predestine LT-GaAs as a material for fast MSM-photodetectors or modulators.

We observed the electro-optic Franz-Keldysh effect at MSM-detectors with interdigitated contacts having various finger spacings between 2µm and 14µm in transmission experiments for photon energies between 1.2eV and 2.0eV.

For our investigations we used a sample consisting of 1.5µm LT-GaAs grown at 250°C on a 50nm AlAs sacrificial layer. The substrate is semi-insulating GaAs. First we annealed the sample at 600°C for one minute in N_2-atmosphere lying face down on a GaAs substrate to avoid the evaporation of As. The annealing procedure renders LT-GaAs semi-insulating. After that we evaporated gold-titanium as MSM interdigital contacts onto the sample. To perform transmission measurements using photon energies far above the bandgap, we had to separate the LT-GaAs layer from the substrate by etching away the AlAs sacrificial layer using 10% HF.

After the preparation of the sample we performed transmission measurements at the location of the MSM-detectors as a function of wavelength for various electric fields and finger spacings. Figure 1a shows the change of the transmitted light for four different values of the applied electric field (33kV/cm, 66kV/cm, 100kV/cm, 133kV/cm). The values for the electric field are estimated roughly by dividing the applied voltage by the finger spacing. The transmission spectra show the field induced Franz-Keldysh absorption below and the Franz-Keldysh oscillations above the band gap. The values for the transmission changes are about 1:1.3 for E=133kV/cm, corresponding to an absorption change of 2300cm^{-1} averaged over the total thickness around the band gap. For higher photon energies the transmission spectra exhibit another, similar structure which is caused by the transitions from the split-off valence band to the conduction band (Figure 1b). At these energies the field induced transmission changes were about 375cm^{-1} and therefore almost one order of magnitude lower than the transmission changes at the fundamental band gap.

Figure 2a shows a logarithmic plot of the field induced absorption changes of the LT-GaAs layer for photon energies near the fundamental bandgap and for two directions of the polarisation. A clear difference between TE- and TM-polarised light is evident. This is due to the fact, that TM-polarised light is only interacting with the light hole (lh) band while the TE-polarised light is interacting with the lh-band and the heavy hole (hh) band.

For photon energies around the split-off band to conduction band transition (0.34eV above the fundamental gap) we observed no remarkable polarisation dependence of the Franz-Keldysh oscillations. Figure 2b shows a logarithmic plot of these absorption changes for two electric fields and different polarisations. Note the different scaling of the energy axes in Figure 2a and 2b. The minima of the absorption changes are at the same wavelengths for both kinds of polarisation within our accuracy of measurement. This is in agreement with theoretical considerations which do not predict a polarisation dependence of the Franz-Keldysh effect since both split-off holes and electrons are mostly isotropic.

We tried to verify these results with a reference sample consisting of a similar structure, but with a different top layer. The LT-GaAs layer was replaced by GaAs grown at the standard temperature of 580°C. These MSM-detector structures did not sustain the high electric fields we used for the LT-GaAs samples (up to 250kV/cm), so we were not able to observe any Franz-Keldysh effect at the split-off band transition energies.

In summary we observed electro-optical effects in thin layers of LT-GaAs for energies between 1.2eV and 2.0eV. The period of the Franz-Keldysh oscillations is polarisation dependent for the lh/hh-valence band to conduction band transitions and shows no dependence for the transition between split-off valence band and conduction band.

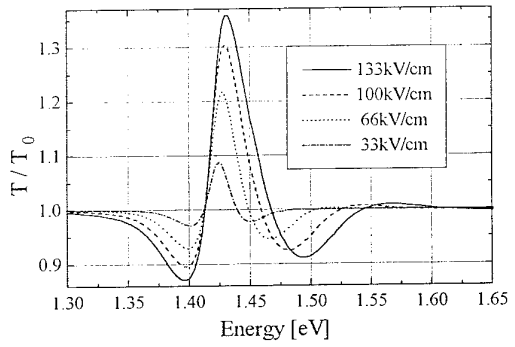

Figure 1a : T/T_0 spectra of the FKE for bandgap energies

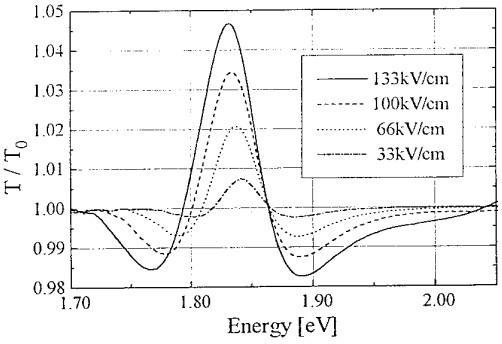

Figure 1b : T/T_0 spectra of the FKE for split-off band energies

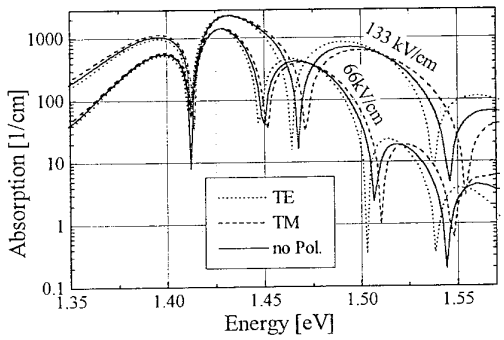

Figure 2a : Absorption spectra of the FKE for bandgap energies

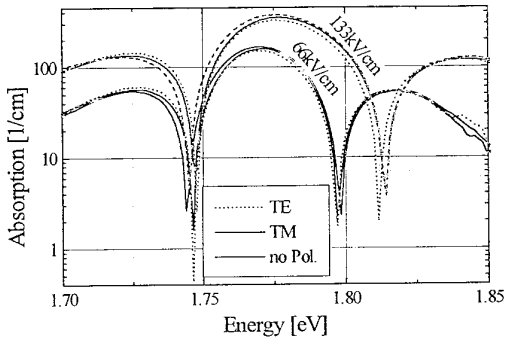

Figure 2b : Absorption spectra of the FKE for split-off band energies Note the different scaling of the energy axes in Figure 2a and 2b.

Capacitance Behaviour of Low-Temperature Grown GaAs/n-GaAs Structures

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Low-temperature (LT-) grown Gallium Arsenide offers potential for device applications as in field effect transistors (FETs),[1,2] as the passivation and insulator layer to improve device performance, and in the optical switch and detector as an active layer.[3] Although the transport properties and microstructures of LT-GaAs has been studied extensively, its effect on the capacitance of devices such as diodes and metal/LT-GaAs/n-GaAs MIS structures has attracted little attention. In this paper we report the observation of an anomalous capacitance behaviour from the metal/LT-GaAs/n-GaAs structure.

The test structure was the LT-GaAs/n-GaAs grown by MBE on n+-GaAs substrates. The n+-GaAs buffer layer was followed by a ~0.5μm n-GaAs layer doped with Si. The growth temperature was 630°C for both n-layers, and 200°C for the LT-GaAs of thickness ~100nm. An undoped AlAs diffusion barrier was also introduced between the n-GaAs and LT-GaAs layers for one type of sample with a thickness of 10nm, to study the effect of the LT-GaAs on the capacitance behaviour of the structure similar to the gate of GaAs-MISFETs. Thermal annealing was carried out in a Nitrogen ambient at 600°C for 10min. Non-alloy Ohmic contacts were made directly by evaporating Au/Ge/Ni for as-grown LT-GaAs, while it was alloyed at 400°C for annealed LT-GaAs structure. The main results are summarized as follows:

1) C-V_B measurements revealed a low barrier height with a value of 0.4eV for as-grown LT-GaAs structures, much lower than the surface pinning level. The Richardson plot $\log(I/T^2)$ vs. 1/T revealed a similar barrier height. Since the surface contact metal/LT-GaAs is Ohmic behaviour, the observed barrier therefore represents the barrier between the LT-GaAs and n-GaAs layer, implying that the Fermi-level in as-grown LT-GaAs is lower, in agreement with other observation.

2). Thermal annealing dramatically increased the potential between the LT-GaAs and n-GaAs. A Richardson plot gave a value of 0.75eV, similar to the surface potential of GaAs, while 1/C vs. V_B plots gave intercepts on voltage axis more than 1V for both samples, due to the change of the low resistivity of as-grown LT-GaAs to high resistivity after annealing, introducing a MIS-type structure.

3) Dependence of the capacitance and conductance on measurement temperature has been investigated. The capacitance of as-grown structures was found to decrease from 280pF slowly, followed by a steep decrease to a value of 165pF at ~200K, and thereafter remained almost unchanged for further decrease of the temperature. The conductance showed corresponding peaks, and moved to the low temperature region as the frequency was decreased. Arrhenius plots for the conductance peaks revealed an activation energy of 0.32eV.

4). Thermal annealing removed the step change of the capacitance in C-T plots, and the capacitance decrease slowly with decreasing the measurement temperature. The conductance peak in G-T plots disappeared, indicating a dramatic change of the LT-GaAs/n-GaAs structure after annealing.

5) An equivalent circuit has been established to explain the observed abnormal C-V behaviour. It demonstrate that the LT-GaAs layer can be represented by a parallel resistance R_L and capacitance C_L. At high temperature, as-grown LT-GaAs acts as a resistor with a small value. The measured C_o represents the depletion capacitance C_D in n-GaAs side. At low temperature the resistivity of the LT-GaAs increases by several orders, and the diode becomes a typical MIS structure and the output capacitance is that of the depletion region and the insulator in series, i.e. $1/C_o=1/C_D+1/C_L$.

The model predicts that the capacitance of a MIS diode with as-grown LT-GaAs will exhibit a frequency dependence in the range of 100M~1GHz at room temperature, thus a recess structure with a thin as-grown LT-GaAs dielectric under the gate is necessary for MISFETs, to avoid the frequency dispersion of the FET's characteristics.

This work was supported by the European Commission ESPRIT Project 6849 TAMPFETS.

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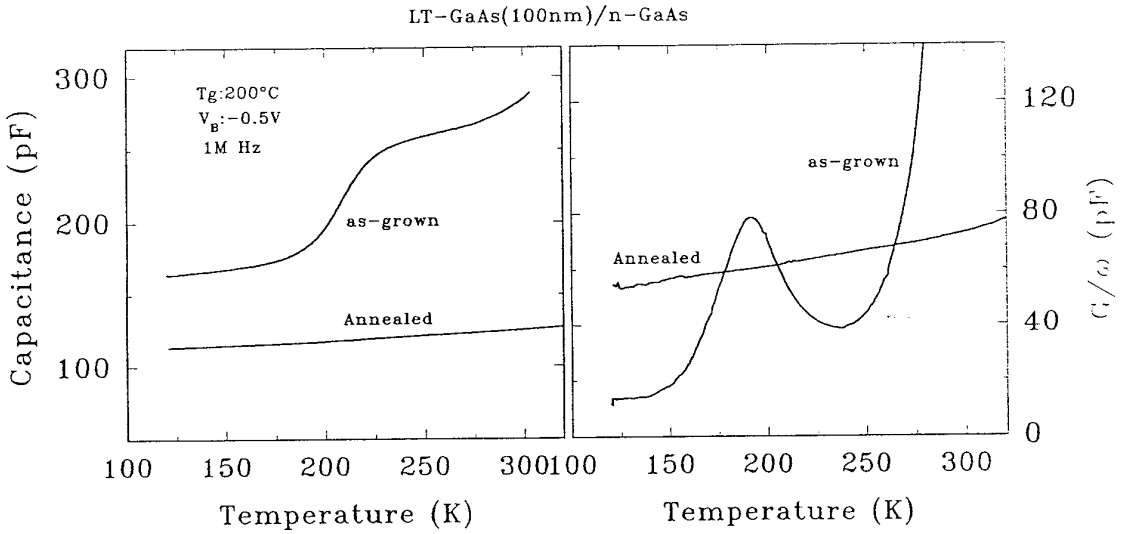

Recent Developments in HFET Devices Employing σ-LT-GaAs

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Abstract

σ-LT-GaAs HFETs, based on the lossy dielectric concept [1], have indicated a high power capability by very high drain source breakdown voltages in combination with high drain currents, clearly outside the Schottky limit [2]. 3.5W/mm RF power capability have been indicated by DC output characteristics [3]. In small signal operation 75GHz f_{max} values have been observed for 1μm gate length devices [4]. Those improvements are related to a field redistribution in the channel, initiated by a low gate drain leakage current crossing the σ-LT-GaAs surface layer. The high field region at the drain side of the gate, responsible for breakdown in Schottky gate FETs, is eliminated and an extended drift region results in an unusual low gate drain capacitance. Surprisingly the translation of the DC power capability into the RF regime is prevented by the input. The dielectric relaxation of the σ-LT-GaAs material results in a g_m dispersion in the MHz range [3] and above the dielectric relaxation frequency the drain current is limited by the breakdown of the σ-LT-GaAs layer [5].
In essence the benefit of the structure is found at the output, while the input introduces parasitic limitations. Therefore, based on the σ-LT-GaAs lossy dielectric FET, recess configurations have been developed preserving the lossy dielectric concept at the output and removing the specific limitations of the input by following structures:

(a) σ-LT-GaAs passivated MESFET, here the LT-GaAs is removed underneath the gate and a sidewall metalization of the gate recess ensures the complete passivation.

(b) Asymmetric σ-LT-GaAs MESFET, here the LT-GaAs layer is removed between gate and source and the gate metalization is directly deposited onto the channel or barrier material overlapping the LT-GaAs layer on the drain side as shown by figures 1 and 2.

Both concepts preserve the lossy dielectric concept between gate and drain identified by high drain source breakdown voltages, low output conductance and very high f_{max} values.

This work was supported by CEC Basic Research ESPRIT action 6849 (TAMPFETS).

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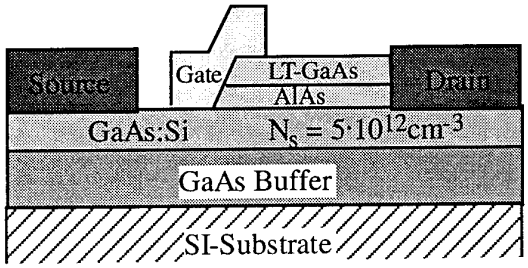

Figure 1: Cross section of assymetric recessed σ-LT-GaAs HFET

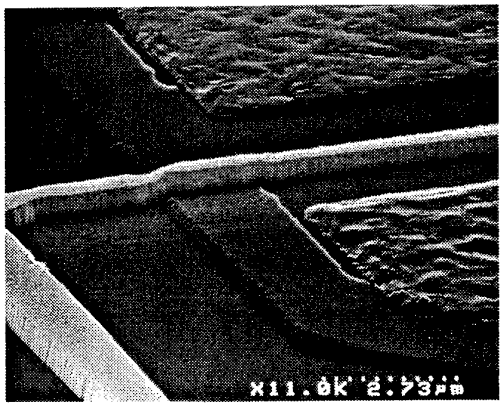

Figure 2: SEM photograph of assymetric σ-LT-GaAs HFET

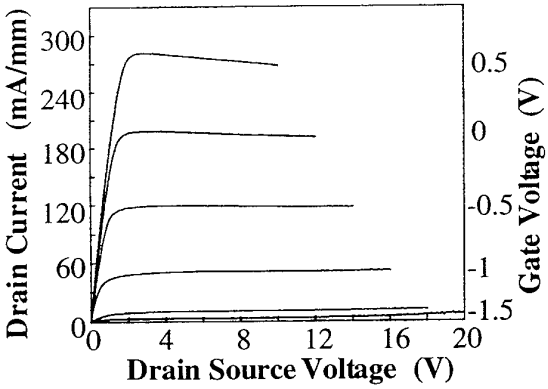

Figure 3: DC output characteristics of assymetrrc σ-LT-GaAs HFET indicating low output conductance

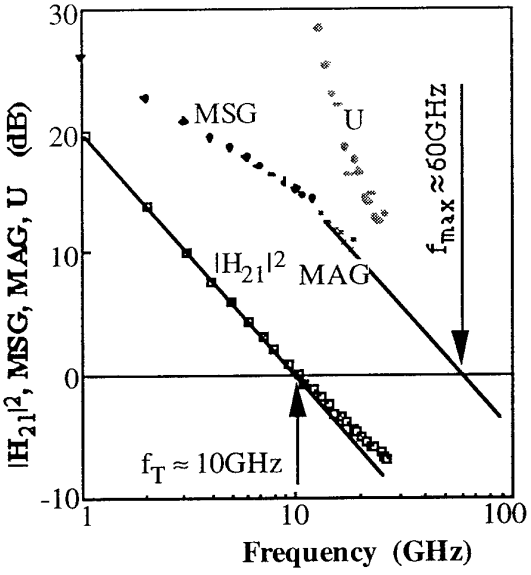

Figure 4: Small signal analysis of assymetric σ-LT-GaAs HFET indicating 10GHz f_T and 60GHz f_{max} from the MAG values. The unilateral gain indicates even higher values.

HETEROSTRUCTURE TECHNOLOGY
WORKSHOP

SESSION C
Transistors I-HEMTs

1 MMIC performance at mm-wave frequencies of HFETs: Device circuit considerations.
P.J.Tasker. INVITED TALK.

2 Comparison of the characteristics of 0.2μm InP HEMTs fabricated on "nearly identical " wafers.
W.Patrick, B.U.H. Klepser, M. Schefer, C. Bergamaschi and W. E. Leitch.

3 0.25μm gate length InP/InGaAs/InP pHEMT with a circular layout.
K. Schimpf, M. Marso, M. Hollfelder, A Van der Hart, P Kordos and H. Luth.

4 Characterisation of InAlAs/ InP HFETs.
G. Georgescu, F. Ducroquet, G, Guillot, K. Naft- Zerrard and G. Post.

5 GaInAs/AlInAs-HEMTs grown on optical waveguide layers for broadband low-noise amplifiers.
C.Schramm, A.Umbach, W.Passenberg, W.Schlaak, G.G. Mekonnen, W.Ebert and H.G.Bach

6 Hot electron degradation of pseudomorphic HEMTs.
P. Cova, R. Menozzi and F. Fantini.

"MMIC Performance at mm-wave frequencies of HFETs: Device/Circuit Considerations"

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In the past 10 years the performance of HFET's has improved significantly allowing f_T values over 100 GHz and f_{max} values over 250 GHz to be achieved on a regular basis. This has been made possible as a result of advancements in fabrication techniques, i.e. submicron gate lengths $L_g < 0.2\ \mu m$, and optimization of epitaxial growth techniques, i.e. heterojuction growth, pseudomorphic epitaxy of GaInAs on GaAs, lattice matched epitaxy on InP, etc.: *reduce intrinsic transit time by reducing transit distance and increasing electron velocity.*

The availability of these HFET structures, particularly the GaInAs pseudomorphic MODFET on GaAs and the AlGaAs/InGaAs lattice matched MODFET on InP, is making mm-wave MMICs feasible, thus stimulating the development of many new mm-wave systems, i.e. collision avoidance radar, traffic information systems, mobile communications, etc.. These systems, however, would like even better MMIC performance thus demanding further improved transistor performance. This is difficult to achieve if only a further reduction in intrinsic transit time is the goal, since i) it is very difficult to maintain the transistor scaling rules when further reducing the gate length < 0.1 μm and ii) further improvements in transport properties will require epitaxial growth of new materials.

Circuit techniques can be used as a alternative to further improve the *"transistor performance"* hence MMIC performance. A cascode unit cell, for example, can be constructed by integrating two transistors, one in conventional common source configuration the other in a common gate configuration. This two gate *"effective transistor structure"*, particularly in a coplanar waveguide MMICs, has a very similar size as the conventional one gate transistor structure and can be considered in MMIC design effectively as single transistor. While the cascode configuration has a slightly degraded f_T the f_{max} (measured around f_T) is typically doubled; increasing MMIC gain and performance. This *"transistor performance"* improvement is achieved by a reduction in both the effective feedback capacitance and output conductance. Cascade structures, for example, based on pseudomorphic MODFET structures, with an f_T = 120 GHz and f_{max} > 200 GHz, have demonstrated f_T values greater than 90 GHz with f_{max} values (measured around f_T) greater than 400 GHz. Broadband (TWAs) MMICs based on this *"effective transistor structure"* have achieved 9 dB of gain from 5 GHz to 80 GHz, while different narrow band (2-stage) MMICs have provided 30 dB gain at 83 GHz and 20 dB gain at 110 GHz respectively.

In conclusion, the optimization of MMIC performance at mm-wave frequencies requires the use not only of advanced fabrication and epitaxial growth techniques but also innovative device/circuit techniques.

Acknowledgement.
The work reported here was performed at the Fraunhofer Institute for Applied Solid State Physics, Freiburg, Germany. It involved the contribution of many coworkers all of which I would like to acknowledge, in particular, J. Braunstein, M. Schlechtweg, W. Reinert, A. Hülsmann, K. Köhler and W. Bronner.

Comparison of the characteristics of 0.2 µm InP HEMTs fabricated on "nearly identical" wafers.

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In our laboratory, a technology for InP-based HEMT devices and circuits has been developed. The devices are fabricated on layers grown by molecular beam epitaxy (MBE). Over a period of 3 years, six 2" wafers have been processed (the sample size is 7 x 7.5 mm giving a maximum of 32 runs per wafer). Table 1 shows the basic structure of the HEMTs.

Layer	Material	In content (%)	Doping (cm^{-3})	Thickness (Å)
Cap	GaInAs	53	5×10^{18}	100
Schottky	AlInAs	52		200
Donor	AlInAs	52	5×10^{18}	100
Spacer	AlInAs	52		30-50
Channel	GaInAs	53		500
Buffer	AlInAs	52		≥2500
Substrate	InP			

***Table 1:** Basic HEMT structure.*

The six wafers have only minor variations in the nominal structure (spacer and buffer thickness), so they are regarded as being "nearly identical." However, the devices show surprisingly different characteristics from wafer to wafer.

The materials properties of the six wafers (mobility, carrier concentration and sheet resistance) are shown in Fig. 1. Wafers #1, 6 and 7 are nominally identical (50 Å spacer, 4000 Å buffer). #8 and 9 have 30 and 40 Å spacers respectively and a 2500 Å buffer. #10 has a 30 Å spacer, 2500 Å buffer and 120 Å cap to reduce the sheet resistance of the structure. It can be seen that, with the exception of wafer #10, the material properties vary probably according to the process tolerances for MBE. The expected trends of higher carrier density and lower mobility for smaller spacer thickness were not obtained.

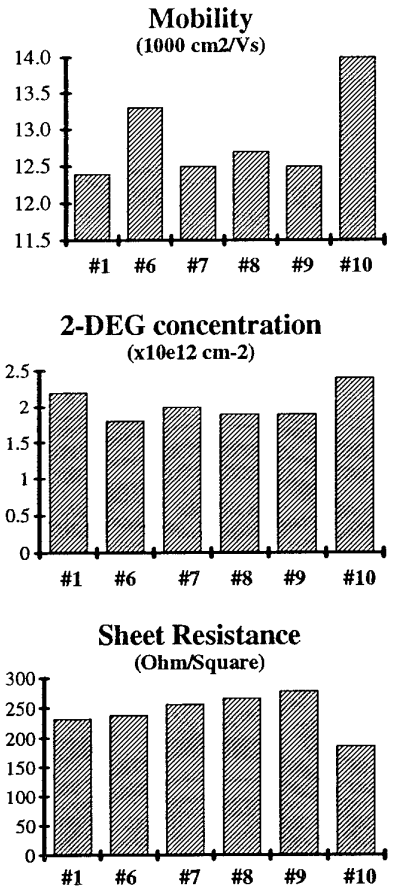

***Fig. 1:** Material Properties of the 6 HEMT wafers studied (room temperature Hall, TLM)*

However, from the six wafers, significant variations in device performance were obtained. Wafers 1 and 10 yielded the highest performance in terms of transconductance and cut-off frequency. In this respect wafers 6 to 9

yielded only mediocre results. Typically values of 600 mS/mm and 150 GHz, for g_m and f_T respectively, were measured on wafer #1 (for a gate length of 0.25 μm). The intermediate wafers yielded best values of 300-400 mS/mm and 100 to 120 GHz respectively, corresponding to a significant reduction in performance. On wafer #10, the device performance equalled or exceeded that for wafer #1, albeit with a reduced gate-length of 0.2 μm that was obtained through improvements in the process. It may be argued that the variations in device performance could arise from the fact that the technology has been continually improved from wafer to wafer. However, the best performance was obtained from the very first wafer using the first developed processes. It took several dozen device runs on 5 different wafers before the performance of devices on wafer #1 could be repeated.

Wafer #10 was grown with a specified sheet resistance of below 200 Ω/□. An increase in sheet carrier concentration with corresponding reduction in mobility was expected. However, it can be seen from the graph of Fig. 1 that the highest sheet carrier concentration AND the highest mobility of all wafers were measured on wafer #10. This result prompted us to carry out photoluminescence on the various wafers. The results are shown in Fig. 2.

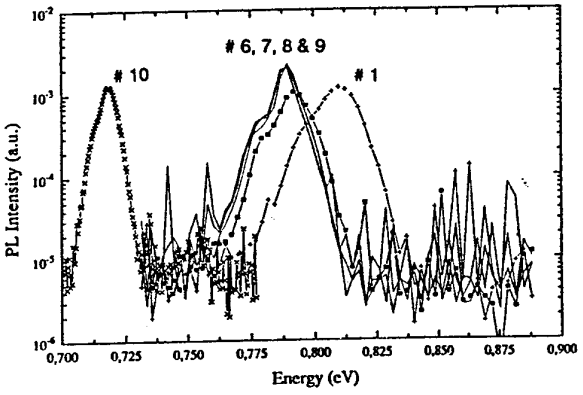

Fig 2: Photoluminescence of Wafers #1 and #6-10 (T = 2.2K, power = 5 mW)

This measurement shows that the PL peak for wafers 6-9 is around 0.79 eV which is a reasonable value for a lattice matched channel. However on wafer 1 and 10 the peaks are shifted to 0.81 eV and 0.71 eV respectively. These results imply strained channels (lower In content in #1 and higher In content in #10). The result for #1 could lie within the process tolerances, but for wafer 10 the peak at 0.71 eV implies an In content of around 70%. Such a high In concentration indicates a large lattice mismatch, which, for such a thick channel, would lead to crystal relaxation.
Further studies, such as DDX analysis, will have to be performed on wafer #10 to determine the true channel composition.

The fact remains, however, that for similar or very nearly identical HEMT structures, quite different device performance can be obtained. It cannot be assumed, even with MBE growth, that wafers with similar specifications, will turn out to have similar characteristics. However, these variations do not necessarily imply a reduction in device performance. Indeed our assumed "strained channel" devices provided us with a higher performance than our nominal "lattice matched" devices.

Acknowledgement: The authors wish to thank Hp. Meier for his assistance in processing the devices. The work is supported by the Swiss national research project LESIT and by Telecom PTT.

0.25 µm gate length InP/InGaAs/InP pHEMT with a circular layout

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1. Introduction

In the last years the development of the High Electron Mobility Transistor for millimetre-wave applications resulted in best RF performance with the material system InAlAs/InGaAs/InP [1]. Nevertheless, some problems arise, most of them are related to aluminum (photoconductivity [2], kink-effect [3], high leakage currents [4], ageing caused by oxidation of Al).
These problems can be avoided by the use of InP instead of InAlAs. A HEMT with 0.5µm gate length fabricated of the Al-free material system InP/InGaAs/InP was demonstrated [5]. We present a 0.25µm gate-length HEMT based on this material system with a circular layout.

2. Device fabrication

The layer structure was grown by low pressure MOVPE at 640 C and is depicted in Fig.1. Hall measurements yielded electron densities of 2.4e12 cm-2 and mobilities of 11.000 cm2/Vs at room temperature. The device processing consists of five steps: 1.) Mesa-formation by wet chemical etching. 2.) Formation of ohmic contacts (Ni/AuGe/Ni/Au) and alloying at 380 C for 90s. 3.) Definition of the gates with E-Beam-lithography and gate recess. 4.) Spinning on of polyimide and structuring by RIE with a Ti- mask. 5.) Formation of the contact pads for RF-characterization. Further information may be obtained from [7].

30nm	n-InGaAs (6e18cm^{-3})	Cap
15nm	p-InP (1.5e18cm^{-3})	Barrier
15nm	i-InP	Separation
10nm	n-InP (2.7e18cm^{-3})	1. Supply
7nm	i-InP	Spacer
8nm	i-InGaAs (80% InAs)	Channel
7nm	i-InP	Spacer
10nm	n-InP (1.5e18cm^{-3})	2. Supply
300nm	i-InP	Buffer
	s.i. InP	Substrate

Fig.1: Layer structure

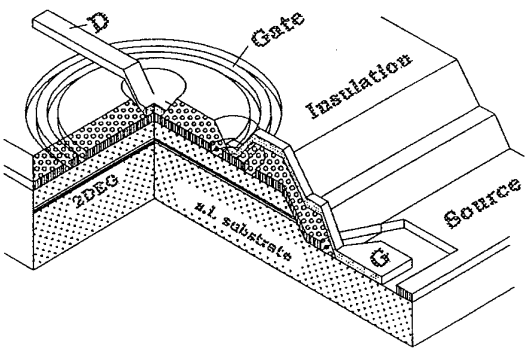

Fig.2 : View of a circular HEMT

3. The RoundHEMT

Because of the circular layout of our devices we call them „RoundHEMTs". The gate is formed as a closed ring. The area inside the gate is the drain contact and the area around the gate serves as source contact (Fig.2). This design makes it necessary to lead the gate and drain-pads across the source area over an insulator (polyimide). The gate ring is broadened for the contact pad.
The advantages of this design are the following:

1. There are no problems related to the mesa-edge (Leakage-currents [6], parasitic gate-capacitance and -resistance), because the electrical active area between source and drain is far away from the mesa-edge.

2. A breaking of the gate metal, which significantly reduces the device yield at very small gate lengths [1], does not lead to a complete failure of the device, because every point of the gate ring is connected to the pad by two ways.

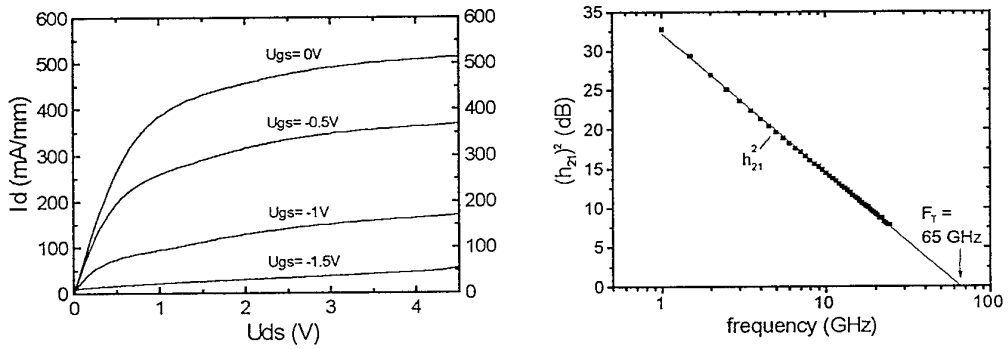

Fig.3 : I-V characteristics and RF measurement of a 0.25µm gate length device

4. Results and Discussion

Devices with a gate width of 100µm and gate lenghts in the range of 0.25µm to 1.1µm were fabricated as described above. The I-V-characteristics is shown in Fig.3. Our devices have a maximum transconductance of 600mS/mm and a threshhold-Voltage of -1.5V (Fig.3). The kink-effect can not be observed. The RF measurements yield a current gain cutoff frequency of f_T= 65 GHz for a 0.25µm gate-length device (Fig.3). Devices with a conventional linear layout yield a f_T= 80 GHz at the same gate length.

This reduced high frequency performance is caused by enhanced parasitic capacitances of the RoundHEMT. This can be deduced by an analysis of the equivalent circuit parameters. A plot of the gate capacitance (Cgs+Cgd) for different gate lengths indicates a capacitance independent of gate length of 72fF for the RoundHEMT, but only 50 fF for the conventional HEMT (Fig.4). This enhanced capacitance is related to the broadened gate area for the pads, a circle with a diameter of 6µm.Now we are trying to get a better RF performance of the RoundHEMT by a reduction of the diameter of this circle to 3µm.

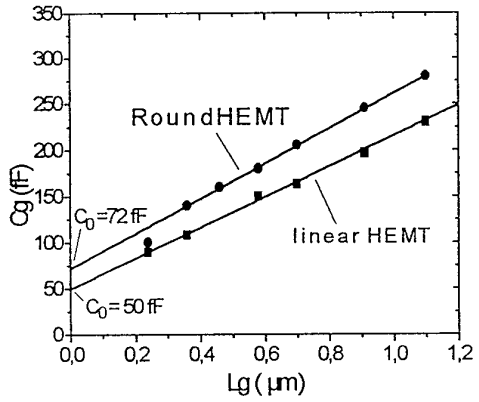

Fig. 4: Dependence of the gate capacitance on gate length for linear and circular HEMTs

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Characterisation of InAlAs/InP HFET

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There is a growing interest in the use of InP as the active channel layer in heterostructure field-effect transistors (HFET's) designed for low cost telecommunication photoreceivers, because of its saturation velocity and high transfer energy between valleys Γ and L. This is an alternative to the more popular InGaAs-based HFET structures which exhibit gate leakage related to avalanching in the low bandgap channel. Despite a very low gate current, a sensible amount of low frequency noise is present on the InP channel FET's. Because the deep-levels could have a contribution in the noise performances and in parasitic effects, we present a study of these defects by current transient spectroscopy (CTS).

The heterostuctures consist of a 15 nm n^+ $In_{0.53}Ga_{0.47}As$ cap ($n = 1*10^{19}$ cm^{-3}), a 50 nm undoped $In_{0.52}Al_{0.48}As$ Schottky layer, a 50 nm n^+ InP channel ($n=2\text{-}3*10^{17}$ cm^{-3}) and a buffer layer, all grown by MOCVD on a semi-insulated Fe doped InP substrate. The buffer consists either of a 30 nm undoped InAlAs layer or a 100 nm undoped InP spacer followed by a 200 nm Fe doped InP layer.

DC performances obtained on the HFETs are presented. For all structures, a kink effect appears and it increases at low temperatures. This current anomaly existing in the low drain voltage region could be explained by a trap model. The electrons get trapped in the deep levels in the InP layer or at the interfaces which can be with barrier and buffer. As the drain voltage is raised, the trapped electrons near the drain side are emitted, increasing the current level (fig. 1). We observe a drain current increase at $V_{ds} > V_{kink}$ at low temperatures attributed to the improvement in electron mobility.

Current transient spectroscopy characterisation has been made for these transistors. Six electron traps have been detected. The Arrhenius dependencies were used to find the parameters of these deep-levels (activation energy and capture cross-section, fig. 2). The localisation of these defects has been established by varying the level of the pulse applied on the gate.

The main trap 1 is observed systematically on all samples. This defect is located in the channel and identified to be related to a defect typical of InP grown by MOCVD. Defect 3 is detected in all cases and seems mainly located in the InAlAs barrier or at the channel/barrier interface. However, this trap is not known as a growth or impurity related InAlAs defect and seems to be related to the technology of the device. It has been fond that trap

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types 1 and 3 have a generation-recombination noise contribution superimposed on the 1/f noise spectrum. Defect 4 is detected in lower concentration and corresponds to the defect usually found in MOCVD InP. The three other deep levels has been found only in the InAlAs buffer HFETs and correspond to defects usually detected in MOCVD InAlAs bulk layer.

Further details of the possible origin of the main traps, mostly concerning trap 3, will be discussed in close relation with technological aspects.

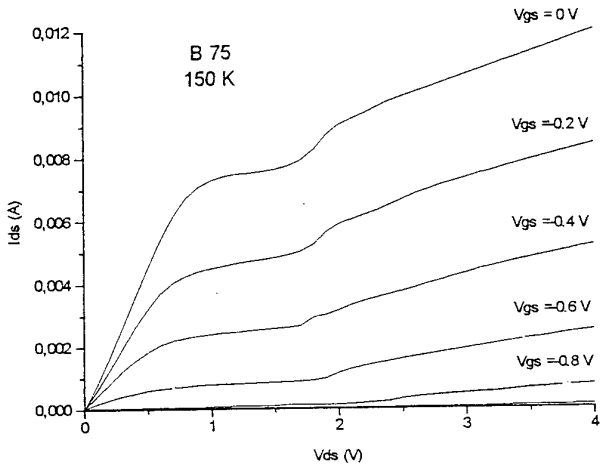
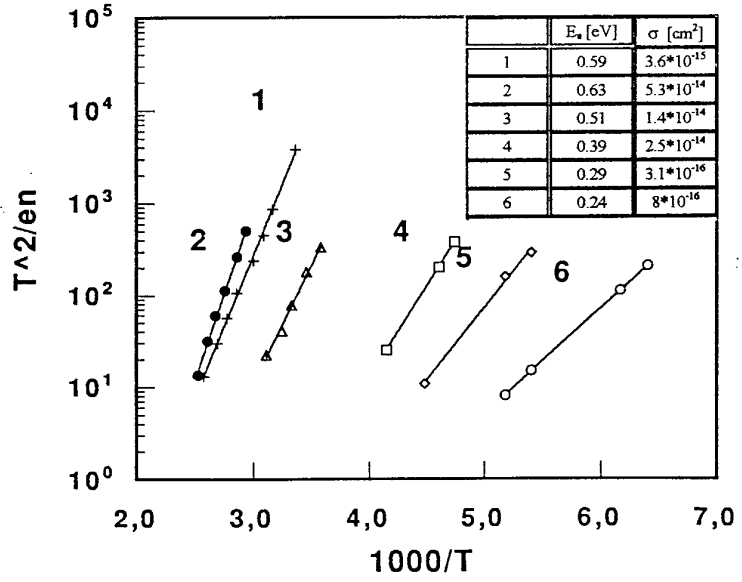


Fig. 1 Drain I-V characteristics measured at 150 K



	E_a [eV]	σ [cm^2]
1	0.59	$3.6*10^{-15}$
2	0.63	$5.3*10^{-14}$
3	0.51	$1.4*10^{-14}$
4	0.39	$2.5*10^{-14}$
5	0.29	$3.1*10^{-16}$
6	0.24	$8*10^{-16}$

Fig. 2 Arrhenius plot for the extraction of trap parameters in AlInAs/InP/AlInAs/InP HFET

GaInAs/AlInAs-HEMTs Grown on Optical Waveguide Layers for Broadband Low-Noise Amplifiers

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Photonic integrated circuits (PICs) are of great importance for future optical networks with their high performance capabilities. For optical networks in the 40 Gbit/s regime high bit rate optical receivers with high efficiency are necessary. We integrated GaInAs pin photodiodes with optical waveguides[1] to overcome the transit time vs. quantum efficiency problem in photodetectors. The integration of the electrical amplifier stages in the PICs avoids the microwave related mounting problems.

This work describes the development of GaInAs/AlInAs high electron mobility transistors (HEMTs) to be used in low-noise amplifier circuits as part of optical receiver PICs. An individual optimisation of the waveguide integrated photodiode and the HEMT is essential to achieve the desired ultra high speed performance. As an equal mesa height of the photodiode and the HEMT is necessary for sub-µm optical lithography, the HEMT layers have to be regrown on a semi-insulating slab waveguide after the local removal of the photodiode layer stack. Molecular beam epitaxy (MBE) is used for the HEMT layers, as it does not affect the previously grown layer structure due to the relatively low growth temperatures involved. However, MBE growth is very sensitive to surface contaminations on the InGaAsP:Fe waveguide layer resulting from preceding processing steps. Therefore, we processed HEMTs from layer stacks grown on InGaAsP:Fe using different sample preparation methods.

Among other techniques[2], wet chemical etching in $H_2SO_4 : H_2O_2 : H_2O$ was applied prior to the growth of a conventional HEMT layer structure with a superlattice buffer (Table 1, Sample 1). HEMTs were then fabricated using optical contact lithography for the gate definition, Ni/AuGe/Ni/Au as ohmic contact metallisation and Pt/Ti/Pt/Au as Schottky contact. In contrast to reference devices grown on epi-ready InP:Fe substrate the transistors show a considerable parallel conductance, which cannot be suppressed even at high negative gate voltages. The additional current is most probably caused by a conducting interface layer, as was indicated by SIMS measurements showing contaminations at the growth interface. Nevertheless, a transconductance of 245 mS/mm was obtained for devices with 1 µm gate length.

An improved cleaning procedure consists of UV-ozone oxidation of the surface and thermal desorption of the oxide layer in the MBE chamber. Devices grown using this technique with the layer structure listed in Table 1 (Sample 2) exhibited excellent pinch-off behaviour and a transconductance of 325 mS/mm (0.8 µm gate length), concomitantly a "clean" SIMS profile was obtained. The output characteristics of devices without and with UV-ozone treatment are shown in Fig. 1a and Fig. 1b respectively. Comparison with a reference sample grown on InP:Fe substrate reveals similar dc- and rf-performance, a slight kink observed at $V_{DS} \approx 1.25$ V results from the non-optimised low temperature AlInAs buffer beneath the HEMT active layers[3].

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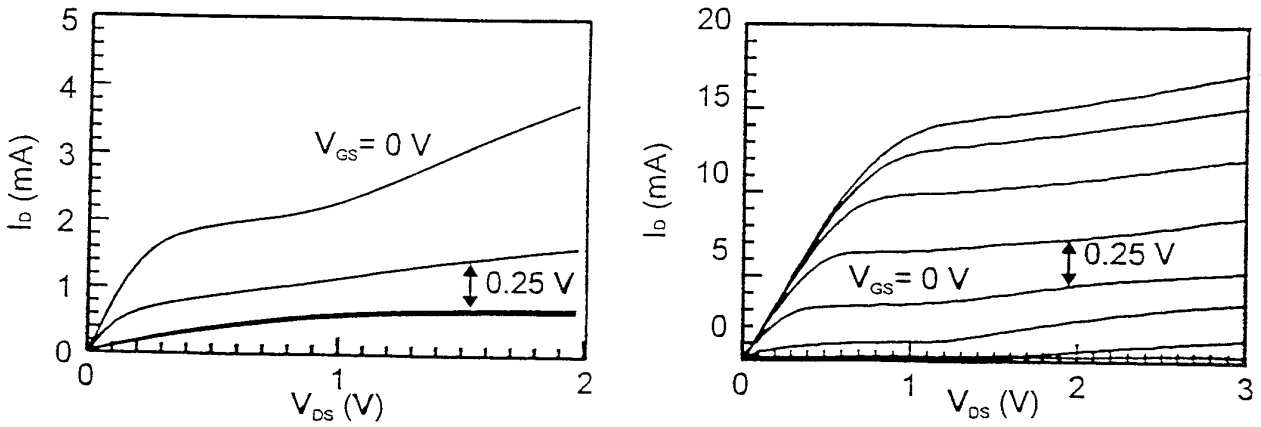
In conclusion, GaInAs/AlInAs-HEMTs regrown on optical waveguide layers were fabricated for the first time. These devices are suitable for use in high speed receiver PICs. A sample preparation with an UV-ozone process considerably reduces performance degradation caused by the regrowth scheme.

Table 1: Layer structure for regrown HEMTs on differently cleaned MOVPE waveguide layers

	Sample 1:	wet chem.		Sample 2:	UV-ozone	
	material	doping	thickness	material	doping	thickness
MBE - HEMT				GaInAs:Si	$1*10^{19}$ cm^{-3}	7.5 nm
	GaInAs:Si	$1*10^{18}$ cm^{-3}	12 nm	GaInAs	nid	5 nm
	AlInAs	nid	24 nm	AlInAs	nid	20 nm
	AlInAs:Si	$4*10^{18}$ cm^{-3}	12 nm	Si δ-doping	$3*10^{12}$cm^{-2}	
	AlInAs	nid	2 nm	AlInAs	nid	4 nm
	GaInAs	nid	32 nm	GaInAs	nid	32 nm
	GaInAs/AlInAs super-lattice		4 / 4 nm 80 nm	AlInAs, 520°C AlInAs, 400°C	nid nid	20 nm 235 nm
MOVPE - waveguide	InP:Fe	semi-isol.	350 nm	InP:Fe	semi-isol.	20 nm
	GaInAsP:Fe $\lambda_g = 1.06\ \mu m$	semi-isol.	1000 nm	GaInAsP:Fe $\lambda_g = 1.3\ \mu m$, GaInAsP:Fe $\lambda_g = 1.06\ \mu m$	semi-isol. semi-isol.	40 nm 600 nm
substrate	InP:Fe	semi-isol.	substrate	InP:Fe	semi-isol.	substrate



a) b)

Fig. 1: Output characteristics of HEMTs grown on MOVPE waveguide layers, Sample 2, $l_G = 0.8\ \mu m$, $w_G = 45\ \mu m$
a) without UV-ozone treatment
b) with UV-ozone cleaned.

HOT ELECTRON DEGRADATION OF PSEUDOMORPHIC HEMTs

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Microwave devices such as MESFETs and HEMTs when biased at high drain voltages undergo impact ionization induced by the high electric field in the region between gate and drain. These phenomena are particularly important for the long-term stability of short-channel devices. It is thus of great interest to study them, in particular for the submicrometric gate length devices required for microwave or millimiter-wave applications.

The aim of this work is to present a case study of hot electron effects in AlGaAs/InGaAs/GaAs pseudomorphic HEMTs (PHEMTs). Electrical characteristics are compared before and after the hot electron stress, and the degradation results are explained.

The devices we tested were commercial passivated PHEMTs suited for application in low noise amplifiers up to 20 GHz. Devices feature 0.25 μm gate length and a gate periphery of 200 μm. Typical values of minimum noise figure and associated gain at 12 GHz are 0.7 dB and 10 dB respectively.

The devices were characterized as received and after electrical stress cycles (at different temperatures) by means of DC measurements (V_{DS}-I_D, V_{DS}-I_G, both in the normal configuration and with source and drain swapped, V_{GS}-I_G, V_{GS}-I_D), C-V plots of the gate-source and gate-drain diodes and measurement of the source and drain access region resistance.

We have performed several electrical stress cycles with the devices biased under hot electrons conditions at different values of the drain bias (the data sheet maximum rating is $V_{DSmax} = 6\ V$).

The V_{DS}-I_D curves measured at room temperature, before and after a stress of 30 minutes at $V_{DS} = 6\ V$, $V_{GS} = 0$, are shown in Fig. 1.

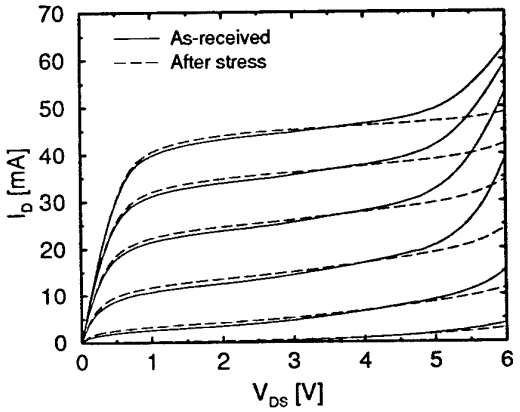

Figure 1: Output characteristics of one of the devices under test. Continuous line: I_D in an as-received device. Dashed lines: I_D after 30 minutes of stress at $V_{DS} = 6\ V$, $V_{GS} = 0$.

A marked decrease of I_D is observed at high V_{DS} in the post-stress characteristics: the sharp I_D increase with V_{DS} (at $V_{DS} \geq 5\ V$), due to impact ionization (soft breakdown conditions) is seen to disappear after the stress. This means that the gate-drain breakdown voltage is increased after the stress (*breakdown walkout*).

Table 1 shows the increase of the gate-drain breakdown voltage measured after two different hot electron stress cycles. Here the breakdown voltage is defined as the value corresponding to a gate current of 200 μA (1 mA/mm) at V_{GS}=0. The breakdown voltage drifts from about 4.5 V in the unstressed device to more than 5 V after 6 h at $V_{DS} = 4.5\ V$, $V_{GS} = 0$ and to about 5.8 V after an additional stress of 10 minutes at $V_{DS} = 6\ V$, V_{GS}=0.

This increase of the gate-drain breakdown voltage corresponds to a decrease of the gate current measured at high V_{DS} due to the impact-ionization generated holes. Fig. 2 shows how the

Condition	$V_{DSstr}[V]$	$T_{str}[min]$	$V_{br}[V]$
As-received	-	-	4.59
1° cycle	4.5	360	5.11
2° cycle	6.0	10	5.8

Table 1: Breakdown voltage (defined as the drain voltage needed to obtain $I_G = 200\ \mu A$ with $V_{GS} = 0$) in an as-received device and after two subsequent stress cycles (both at $V_{GS} = 0$).

gate current measured as a function of V_{DS}, at different values of V_{GS}, changes after a stress of 30 minutes at $V_{DS} = 6\ V$ and V_{GS}=0.

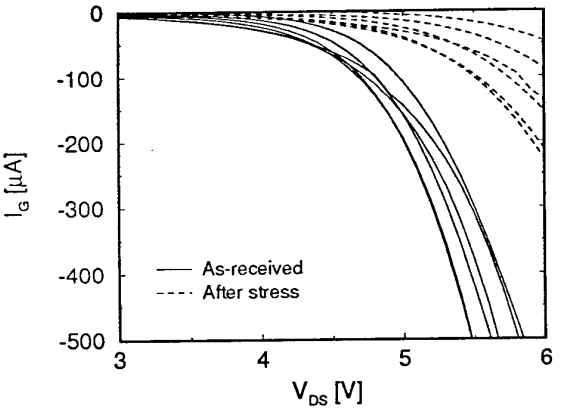

Figure 2: Gate current corresponding to the same conditions of Fig. 1.

The increase of the gate-drain breakdown voltage described so far is permanent, i.e. it cannot be recovered by storing the device at room temperature or at higher temperatures, independently of the storage time. Such breakdown walkout can be explained if we assume that the degradation mechanism caused by hot electrons is a creation of electron traps in the region between gate and drain. When filled with negative charge (e.g. by hot electrons), these traps expand the depletion region towards the drain, thus reducing the maximum electric field and increasing the breakdown voltage.

To investigate this possible explanation and to separate the hot electron effects taking place in the source-gate and gate-drain regions, we have measured the output characteristics of the device of Fig. 1 with source and drain swapped, both before and after the stress; no significant change is observed with respect to the pre-stress curves in this configuration, and the breakdown behavior is unmodified, pointing out that the degradation mechanism is located in the gate-drain region.

Moreover, we have observed an increase of the resistance of the drain access region (R_D) by about 17% after the stress, while on the source side a slight (4%) reduction of the access resistance (R_S) has been measured. The R_D increase is consistent with the idea that the stress develops a wider depletion region between gate and drain, while the decrease of R_S, together with the slight increase of I_D at low V_{DS} (see Fig. 1) can be attributed to trapping of positive charge under the gate, a mechanism that has been observed to take place during hot electron stresses of PHEMTs.

Furthermore, we have measured the capacitance of the gate diode as a function of gate-drain reverse voltage; after the hot electron stress of Fig. 1, it decreases by more than 10% in the whole voltage range, in agreement with the hypothesis of a wider gate depletion region after the hot electron stress.

With the purpose of investigating the temperature dependence of the hot electron damage we have finally performed the electrical stress at different temperatures. Three devices were tested at T_a=24 °C, 50 °C and 70 °C, respectively, while the remaining stress conditions were held constant (30 minutes at $V_{DS} = 6\ V$, V_{GS}=0). We have observed a decrease of the relative change of the gate current measured at $V_{DS} = 6\ V$, V_{GS}=0 (i.e. of the stress damage) from 84% to 71% as the stress temperature increases from 24 °C to 70 °C. This is consistent with the commonly observed phenomenon of reduced hot electron damage at high temperatures due to enhanced phonon scattering.

In conclusion, in this work we have described a set of experiments for the characterization of the hot electron degradation in commercial pseudomorphic HEMTs. For the devices under test we have found that the effect of the hot electron stress is a permanent increase of the gate-drain breakdown voltage (breakdown walkout).

The observed degradation mode can be attributed to trap-related phenomena, namely trap creation in the gate-drain region and capture of negative charge, yielding a localized widening of the gate depletion region and reduction of the peak electric field.

HETEROSTRUTURE TECHNOLGY
WORKSHOP

SESSION D
Transistors II-HBTs

1 Analysis of the temperature dependence of current gain in Heterojunction Bipolar Transistors.
C.M. S. Ng, P.A. Houston and H.K.Yow.

2 The effect of the base ideality factor on the temperature dependence of the current gain in HBTs.
D.E. Kren, A.A.Rezazadeh, M. A. Crouch and S. S. Gill.

3 Effect of polyimide passivation on InGaP/GaAs HBTs.
J. Masum, P. Parmiter, T. J. Hall and M. Crouch.

4 Electrical characterisation of Si-Ge based HBTs.
O.De. Barros, B. Letron, G. Girault-Matlakowski, G. Vincent and G. Bremond.

5 Application of Si/SiGe HBTs in mixers at X-band frequencies
R. Schnitzer, H. Erben and H. Schumacher.

6 SiGe -HeteroFET : Simulations of layer structures and results.
B.Rosen, S. Luthin, F. Schaffler, M. Gluck, U Konig and E. Kohn

7 Physical simulations of heterostructure devices :- Applications to device optimisation and to improvements of the knowledge on the device behaviour.
G. Salmer. INVITED TALK.

Analysis of the Temperature Dependence of Current Gain in Heterojunction Bipolar Transistors

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Heterojunction bipolar transistors (HBTs) are important devices for high power and high temperature applications. The operation of HBTs at high power is fundamentally limited by excessive internal heating within the device. Negative differential resistivity (NDR) is generally attributed to this internal heating but the exact mechanisms are not well understood. The current gain variation with ambient temperature is believed to be caused by the same mechanisms. An understanding of these mechanisms is therefore valuable to the device designer, particularly in high power applications.

We present here a consistent theory to explain the causes of NDR and current-gain/temperature variation in HBTs. An analytical expression which accounts for both the temperature variation of the collector current and base current has been derived. Each possible base current component: space charge region (SCR) recombination, interfacial recombination, surface recombination, reverse hole injection and base bulk recombination, is included in the analysis and its relative importance in different device structures and material systems assessed. Using this analytical expression, we can explain why NDR is observed in HBTs but not in Si transistors, and can identify the various contributions to the effect. The current-gain/temperature variations estimated from the analytical expression are in agreement with experimental plots and results from computer simulated Ebers-Moll plots which include the full temperature dependence of each base current contribution (figs. 1-3). The occurrence of NDR in heavily doped base HBTs at high current densities (fig 4) can also be explained using this theory.

At low current densities, SCR recombination in the emitter causes the large reduction in current gain with increasing temperature seen in figs. 1-3. In abrupt emitter HBTs, the $\Delta E_C/\Delta E_V$ partitioning ratio determines how reverse hole current affects the current gain with temperature at high current densities. The effects of grading in AlGaAs/GaAs HBTs are seen at high temperatures by comparing figs. 1 and 2. Also at high current densities, Auger type base bulk recombination with its negative temperature dependence of the recombination time can be responsible for NDR in heavily doped base devices (fig. 4).

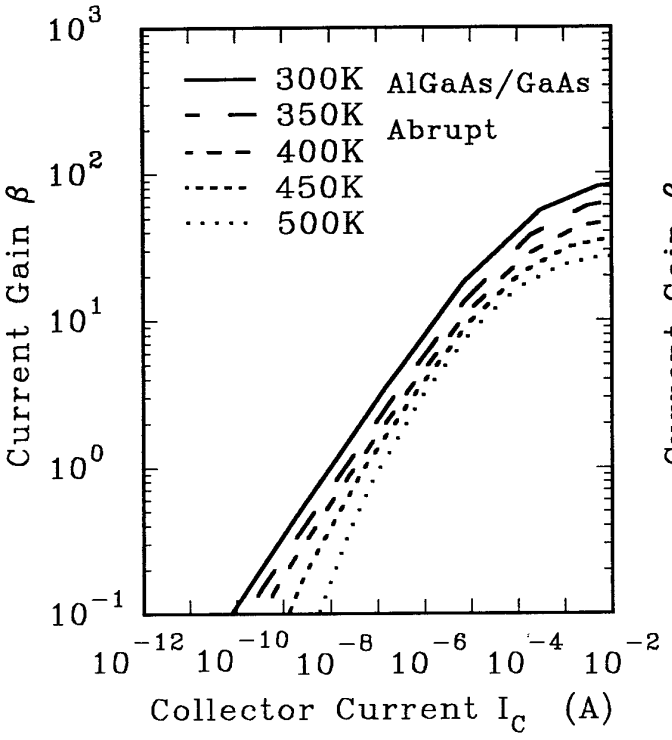

Fig 1: Simulated plot of current gain versus collector current at various temperatures for abrupt AlGaAs/GaAs HBT (Al 35%).

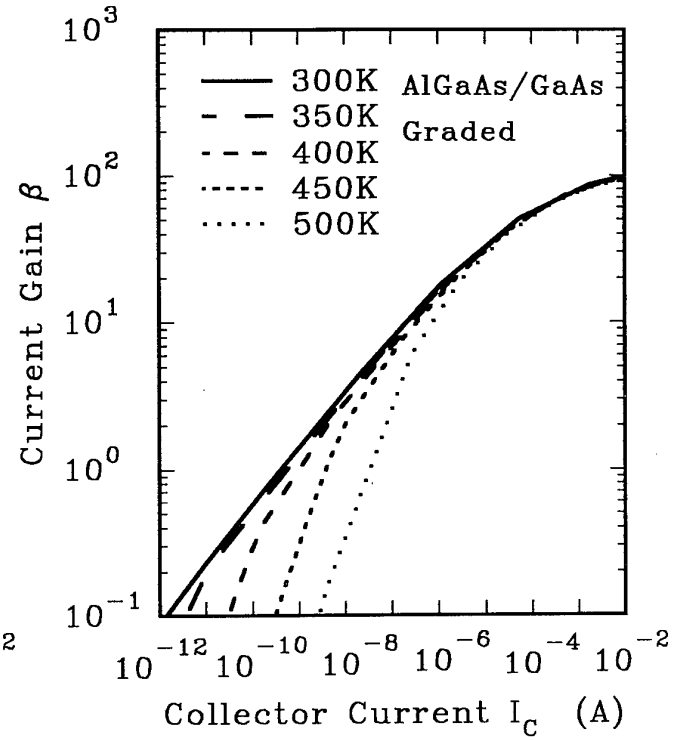

Fig 2: Equivalent plot for a graded device showing reduced temperature dependence at high current due to reduced reverse hole injection.

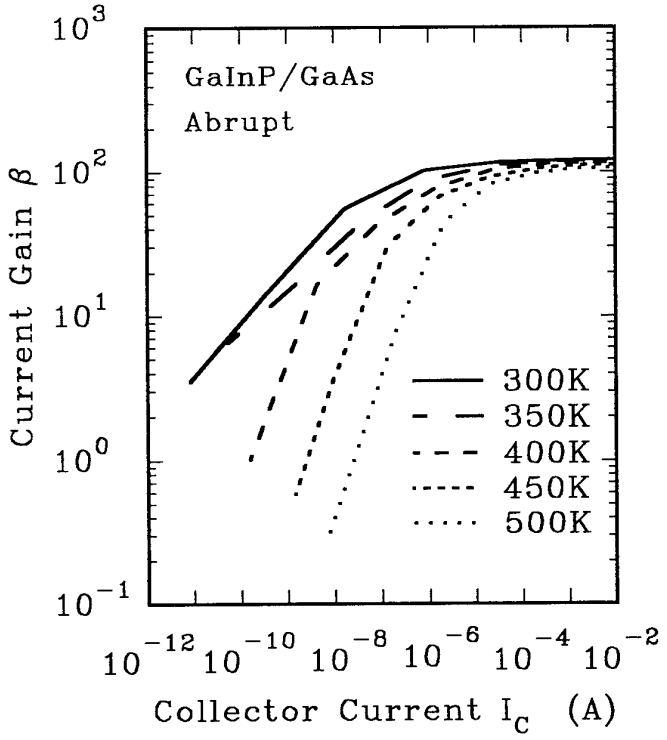

Fig 3: Simulated plot for an abrupt GaInP/GaAs HBT. Both abrupt and graded devices show negligible reverse hole injection due to the small $\Delta E_C/\Delta E_V$ ratio.

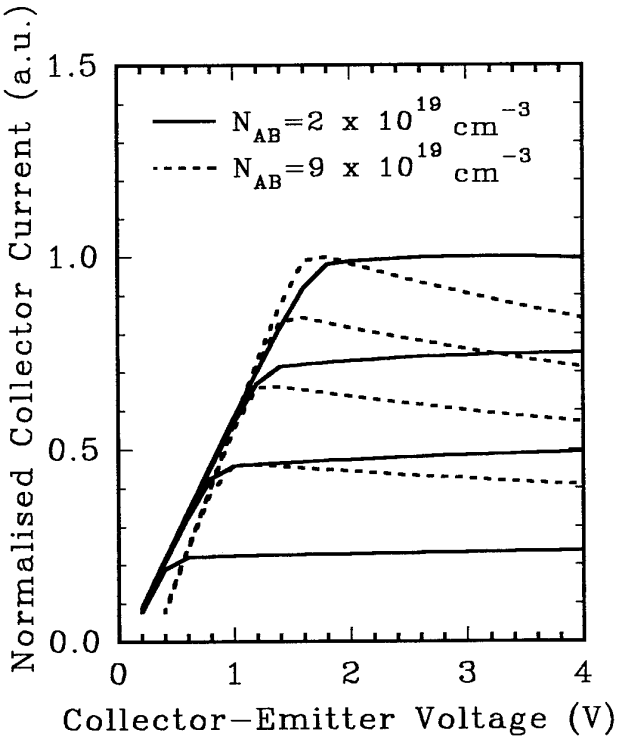

Fig 4: Simulations showing the effect of the dominant Auger recombination at high base doping in GaInP/GaAs HBTs.

The Effect of the Base Ideality Factor on the Temperature Dependence of Current Gain in HBTs

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Introduction: AlGaAs/GaAs HBTs are the most widely investigated devices and have demonstrated excellent device and circuit performance. Whilst there have been some publications regarding the current gain variations with temperature, there is little information on the detailed current gain dependence with temperature. This information is essential for HBT device optimisation in order to exploit fully the heterostructure concept for power and high temperature applications.

In this paper, we show in addition to the intrinsic emitter injection efficiency due to the heterojunction band gap discontinuity, the base bulk, space-charge region and surface recombination currents can also have a significant effect in controlling the temperature dependence of current gain in HBTs. A theoretical model based on drift-diffusion is employed to explain the experimental results. Good correlation has been obtained between the theoretical and experimental results.

N-p-n HBTs were fabricated on materials grown by MOCVD on undoped semi-insulating (100) oriented GaAs substrates at Epitaxial Products International Ltd of Cardiff, UK. The p-type and n-type dopants were carbon and silicon respectively. The structure for the InGaP/GaAs HBT is similar to that of the AlGaAs/GaAs HBTs except that the emitter/base junction is graded in the former case. Discrete HBTs with large lateral geometries were fabricated from the grown epitaxial layers using conventional photolithography processes and wet chemical etching.

From the data given in Fig. 1 it is seen that HBTs with a base ideality factor greater than unity have a larger gain reduction with temperature (device A and EET-A). In contrast, devices with a low base ideality factor (devices B and C) exhibit near temperature independent current gain. The near-unity base ideality factor indicates that the base current is primarily dominated by base bulk recombination. On the other hand an ideality factor close to 2 suggests that the current gain is dominated by emitter/base SCR recombination assuming no surface leakage.

In order to verify the observed experimental results and gain an insight into the current gain degradation, a theoretical model was employed to predict the variation of current gain with temperature. Fig. 2 shows the results of the modelling for the three graded AlGaAs/GaAs HBTs with varying interface trap density. It is clear from this figure that the HBT with no SCR recombination (N_{tI}=N_t=0) shows no variation of current gain with temperature. This data corresponds to the experimental results for the graded AlGaAs/GaAs HBT (device B) as shown in Fig. 1. However, devices with the interface trap concentration of $N_{tI} = 10^{11}cm^{-2}$ and above have greater reduction of current gain with temperature. This data suggests that HBTs with a high SCR recombination have a severe degradation of current gain with temperature. While for HBTs dominated by base bulk recombination the current gain is independent of the temperature. These results agree well with the experimental data given in Fig. 1 correlating the variation of the current gains with temperature.

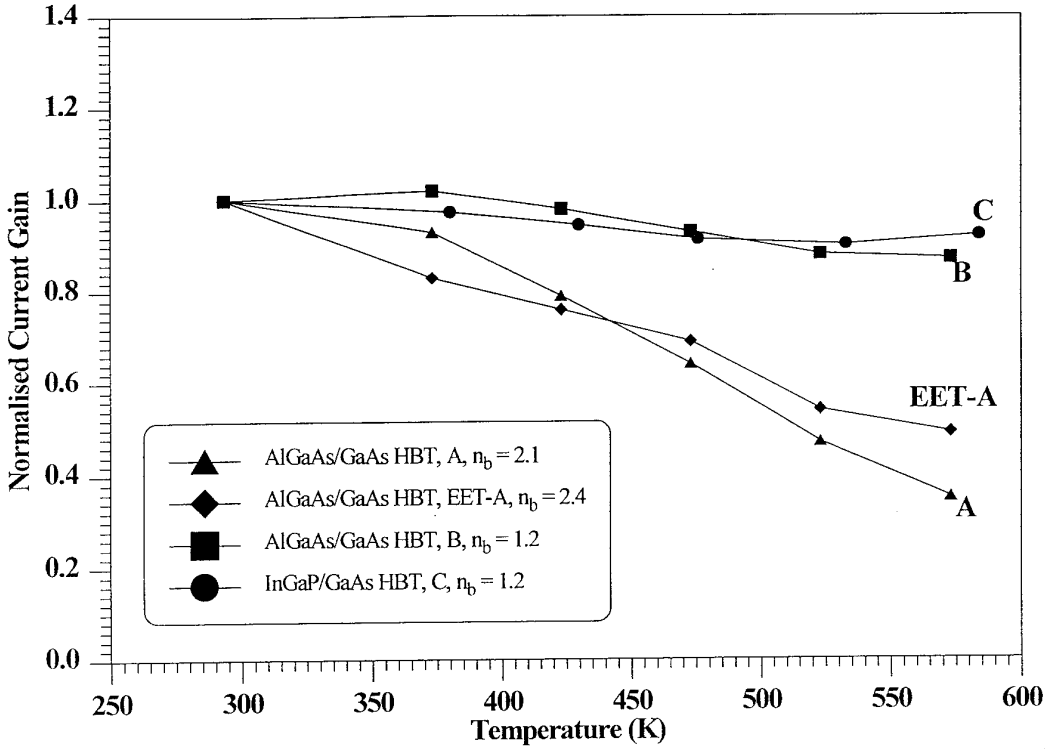

Fig 1. Measured normalised current gain verses temperature for various graded junction AlGaAs/GaAs *and* InGaP/GaAs *HBTs. EET-A is device A with an emitter edge-thinning design.*

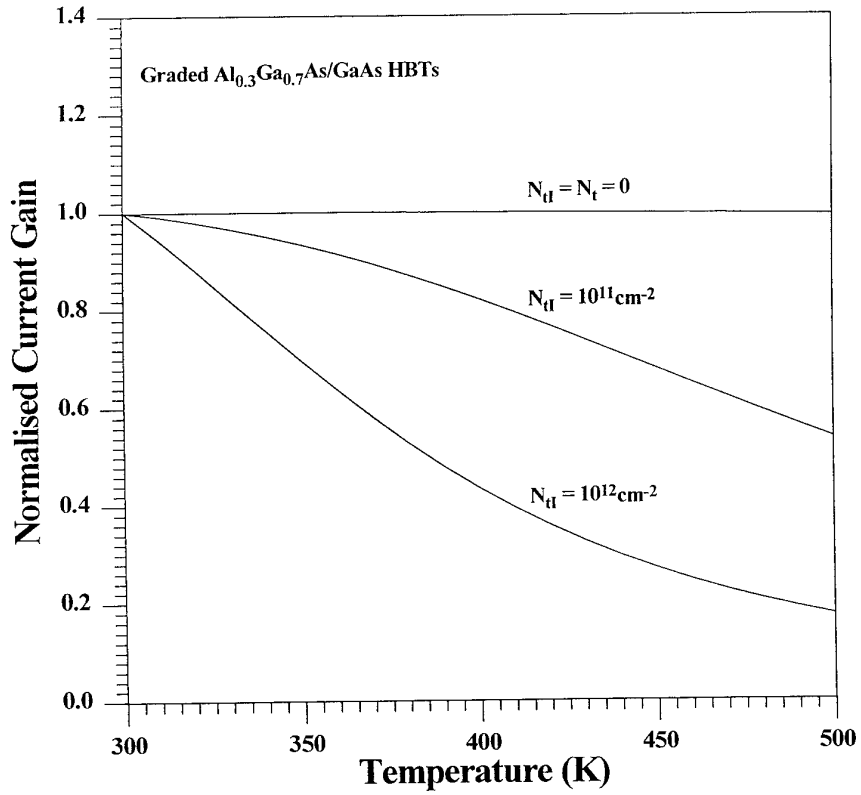

Fig 2. Modelled normalised current gain verses temperature for graded junction AlGaAs/GaAs HBTs with different interface trap densities, N_{tl}.

Effect of polyimide passivation on InGaP/GaAs Heterojunction Bipolar Transistors (HBTs)

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InGap/GaAs systems are preferable over AlGaAs/GaAs systems due to the large valence band discontinuity (0.29-0.33eV), small conduction band discontinuity (0.11-0.2eV) and InGaP system is less prone to surface oxidation than the AlGaAs system, because indium containing compounds are largely observed to have low surface states densities[1-2], resulting in lower surface recombination velocity in comparison to Al containing compounds. However, for both systems the extrinsic base is still the same, GaAs, which is well known to have large surface recombination velocity[3-5] resulting in both cases in collector leakage at low bias and base extrinsic surface recombination at high bias (V_{BE}>1.3).

The base current consists of recombination current in the quasi-neutral base; in the emitter base space-charge region (which includes both recombination in the bulk of the space-charge region and recombination at the heterointerface); hole current injected from the base into the emitter; surface recombination in the extrinsic base region and leakage current originating at the emitter perimeter. The collector current consists of the electron current injected across the heterointerface; and the leakage current, at the emitter-base periphery and at the base-collector periphery.

The heterointerface states are formed during growth, therefore, it is dependant on growth condition and temperature, yet the extrinsic surface states can be minimised via device passivation.

From experimental work it is observed that there exit a "dip" in the base current of the non-passivated InGaP/GaAs HBTs at forward bias less than 0.8V, its cause is attributed to competition in recombination between the surface and heterointerface. Figure 1 compares between the base current for passivated and

control (non-passivated sample that went through the same heat cycle as passivated) samples as a function V_{BE}. We demonstrate here the prevention of the "dip" formation and the reduction in base and collector leakage current via polyimide passivation.

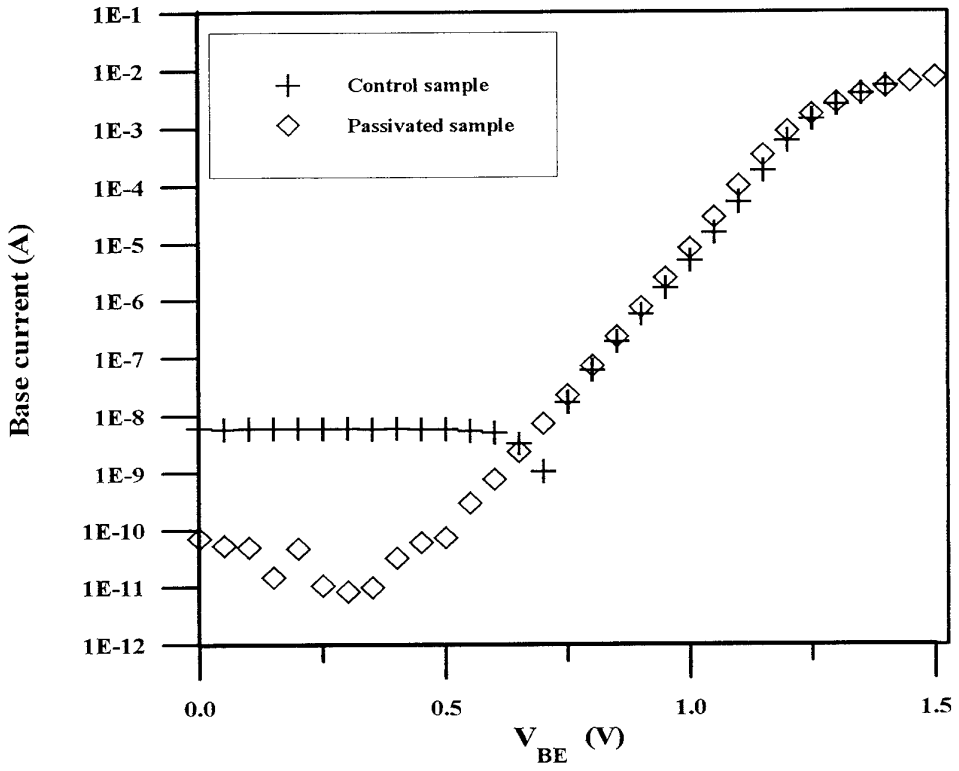

Figure 1. Plot of the base current as function of applied bias for passivated and control sample of InGaP/GaAs HBT at room temperature

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ELECTRICAL CHARACTERISATION OF SIGE BASED HETEROJUNCTION BIPOLAR TRANSISTORS.

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SiGe based heterojunction bipolar transistors (HBTs) performances are closely connected to the thin epitaxial base quality. Within the context of a SiGe-base BiCMOS process technology, epitaxially grown strained layers may suffer from a too high thermal budget, leading to a degradation of device performances.

This work reports electrical characterisation of an advanced single polysilicon CMOS compatible self-aligned heterojunction bipolar transistor with thin heavily doped rapid thermal chemical vapor deposited epitaxial SiGe base layers.

The analysis of static current characteristics concludes in the presence of two perimeter leakage currents, originating from the emitter-base junction along the field oxide (LOCOS) and from the junction along the PECVD SiO_2 sidewall spacer. The temperature dependance of the base current for HBTs without LOCOS shows an increase of the non-ideal component with decreasing temperature, and with an ideality factor larger than two. Furthermore, the reverse current of the emitter-base junction shows a component at low voltages that is not present for epitaxial Si-base pseudo-HBTs. These results may be explained by assuming the presence of defects in the epitaxial layers of the HBTs, allowing trap assisted tunneling and Poole-Frenkel enhanced recombination. In order to confirm this assumption, DLTS measurements have been performed on the emitter-base junction of SiGe HBTs and Si base pseudo-HBTs. The measurements show a transient behaviour corresponding to carrier emission from deep traps only in the case of SiGe base transistors.

European Heterostructure Technology Workshop '95, 17–19 September 1995, Cardiff

Application of Si/SiGe HBTs in Mixers at X–Band Frequencies

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Recent developments in SiGe devices and technology resulted in Si/SiGe heterojunction bipolar transistors (HBTs) with a transit frequency f_T of 116 GHz [1] and a maximum frequency of oscillation f_{max} of 120 GHz [2], respectively. Because of the small 1/f noise corner frequency in Si/SiGe HBTs [3], these devices are very attractive for oscillator and mixer applications.

In order to investigate the suitability of Si/SiGe HBTs as well as silicon based passive components, a single–balanced and an image–rejection mixer MMIC, which converts 10.3 GHz down to 435 MHz, was designed. Main part of this complex mixer circuit are two single balanced mixers. Both of these mixers are divided into two single–ended mixers combined by two 180° couplers. Additionally, a Wilkinson power splitter for the radio frequency (RF) signal and 90° couplers for the local oscillator (LO) signal at the input and the intermediate frequency (IF) signal at the output circuit will be used in an image–rejection mixer.

As can be seen, the mixer operation is mainly dependent on several couplers. Up to now, couplers were realized on semiinsulating GaAs or non–semiconducting substrates. Recently, researchers pay much more attention to silicon as a material for future integration of microwave components [4]. However, no experimental results for integrated couplers on high–resistive silicon substrates are available. Therefore, 90°– and 180°–coupler schemes for RF and IF frequencies were investigated. With respect to area consumption in an MMIC for IF frequencies (frequencies below 2 GHz) only couplers with lumped elements are usefull. For RF frequencies simulations have shown that reduced couplers were possible only at the expense of a degraded performance. Only conventional branch line couplers should be used due to the higher bandwidth performance.

Nevertheless, we have realized all types of reduced couplers for both RF and IF frequencies. For a frequency of 10.3 GHz we obtained in lumped element 180° couplers a insertion loss of 1.2 dB and a isolation of 24 dB at 1 GHz bandwidth. The layout of this coupler and the main frequency performance are summarized in figure 1 and 2, respectively. Lumped element 180° couplers at a frequency of 435 MHz delivers an insertion loss and isolation of 2.5 dB and 25 dB, respectively. The bandwidth for this couplers is 80 MHz.

Additionally, we have tested a single–ended mixer using double–measa type Si/SiGe HBTs. A germanium content of 30 % enables high base doping concentrations and hence a small base resistance

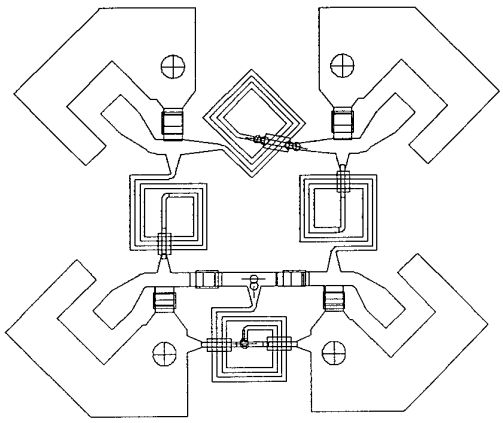

Figure 1: Layout of 10.3 GHz lumped element 180^o coupler for on–wafer measurements

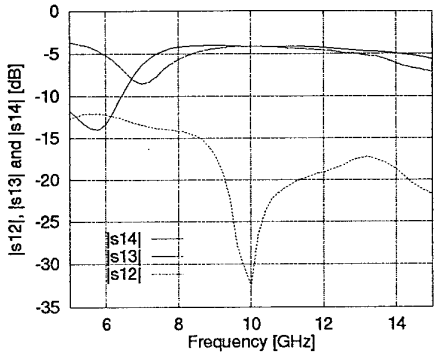

Figure 2: Measured frequency performance of an 10.3 GHz lumped element 180^o coupler

without any degradation in current gain. Typical values for the transit frequency and the maximum frequency of oscillation, derived form the unilateral gain are 42 GHz and 47 GHz, respectively. The transistors are embedded in a microstrip matching circuit on an RT/duroid 5880 with 250 μm substrate thickness. At a LO signal power of -5 dBm this circuit exhibits a conversion gain of 4.5 dB and a 1dB–compression point at -8 dBm. The mixer consumes a power of only 12 mW.

We have demonstrated a silicon based mixer design for a futural MMIC application for a frequency of 10.3 GHz. The mixer performance is mainly determined by the properties of the couplers. Consequently, several demands on technology, like reproducibility, adhesion of dielectric films, roughness of the silicon surface and the formation of via holes for microstrip circuit elements, arise from these passive components.

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SiGe-Hetero FET: Simulations of layer structures and results

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In this communication we report on the optimisation of n-type SiGe modulation doped field effect transistors (n-MODFET). In an n-MODFET electron confinement is achieved by growing a Si-channel under tensile strain onto a $Si_{1-x}Ge_x$ buffer. Due to a conduction band offset of 170meV ($Si_{0.7}Ge_{0.3}$) a twodimensional electron gas (2DEG) is created in the Si-channel. A highly doped $Si_{1-x}Ge_x$ supply layer acts as an electron source.This layer is separated from the Si-channel by a $Si_{1-x}Ge_x$ spacer in order to reduce ionized impurity scattering thus resulting in an enhance carrier mobility in the channel.
A general targetis to achieve both a high mobility and a high carrier density. One method to enhance the carrier density is the reduction of the spacer between channel and doping region, another one is to increase the doping concentration. In the first case a decrease of the carrier mobility caused by an increase of ionized impurity scattering occurs. The second method leads to a generation of a parallel channel due to the incomplete transfer of donor electrons into the Si-channel.
In order to find the best trade off between a high carrier density in the 2DEG and a minimized one in the parasitic channels, simulations of different layer structures have been performed. Within this simulations doping concentration, spacer width and the position of the supply layer were varied. After the theoretical optimisation the heterostructures are grown in a MBE system equipped with electron beam evaporators for Si and Ge and an effusion cell for the Sb doping.
In a first attempt a frontdoped geometry was considered. The principle layer structure is a 9nm Si channel on a SiGe-buffer followed by a 8nm SiGe-spacer, the 6nm SiGe-doping region with donor concentrations of about $8*10^{18}cm^{-3}$, a 5nm SiGe-cap spacer and a 5nm Si-cap layer. The Ge concentration is always 30% (Fig.1).
A Pt-Schottky-gate was considered on the Si-cap resulting in a Schottky barrier of 900 meV. The n-MODFET should be a normally off transistor. Fig.2 shows the carrier density versus the gate voltage. At zero gate bias the 2DEG and the doping region are depleted. With increasing gate voltage the channel is going to be filled while still no electrons are in the doping region. A further increase of U_g leads to a pronounced parallel channel in the doping layer. The maximum difference between the carrier density in the channel and in the doping region is calculated to $\Delta n(max)=0.5*10^{12}cm^{-2}$ (curve with open squares). Reducing the spacer width down to 3nm (open cycles) yields a $\Delta n(max)=1*10^{12}cm^{-2}$.
Higher $\Delta n(max)$ are achieved with a double sided doped configuration. An additional doping layer separated by a 3nm SiGe spacer is placed underneath the Si-channel. Typical doping levels are $8*10^{18}cm^{-3}$ for the front doping layer and only $1\text{-}2*10^{18}cm^{-3}$ for the back one in order to suppress a parallel channel. Fig.3 shows the density versus gate voltage for the double doped configuration. The back doping region is depleted almost completly for a doping level of $1*10^{18}cm^{-3}$ (open cycles). $\Delta n(max)$ is about $1.4*10^{12}cm^{-2}$. In going to higher doping levels ($3*10^{18}cm^{-3}$) $\Delta n(max)$ shows a small increase but there is always a pronounced parallel channel (curve with open squares). Applying a substrate bias of about 10mV/nm reduces the carrier density in the back doping layer and enhances the density in the Si-channel to $2\text{-}3*10^{12}cm^{-2}$.
Placing the doping region directly within the Si-channel yields the highest carrier densities. Although it is excepted to get a very low carrier mobility this doping technique may be of interest for short channel applications where only the saturation drift velocity is the important factor and not the mobility.
Some preliminary Hall measurements and device results will be presented in order to evaluate the feasibility of the simulations.

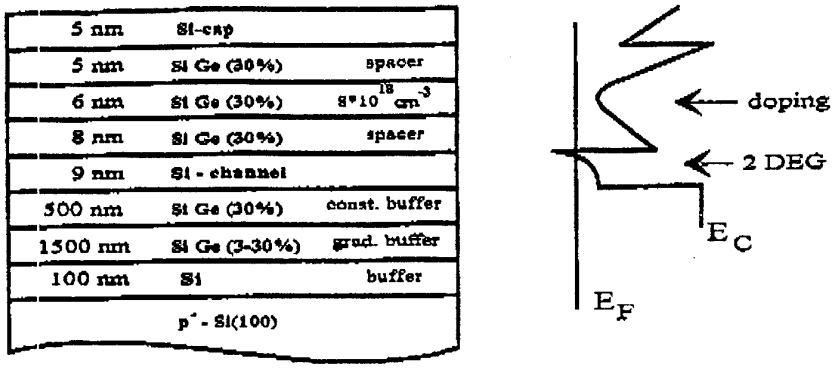

Fig.1: Layer structure for a frontsided doped SiGe n-MODFET

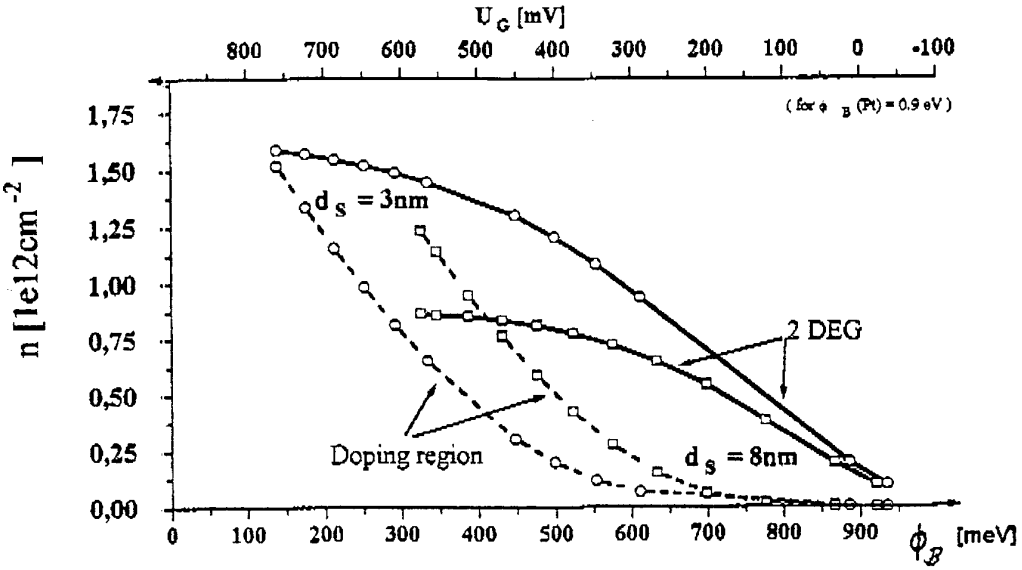

Fig.2: Calculated carrier density in the 2DEG and in the doping region for a front sided doped n-MODFET versus gate bias with two different spacer thicknesses

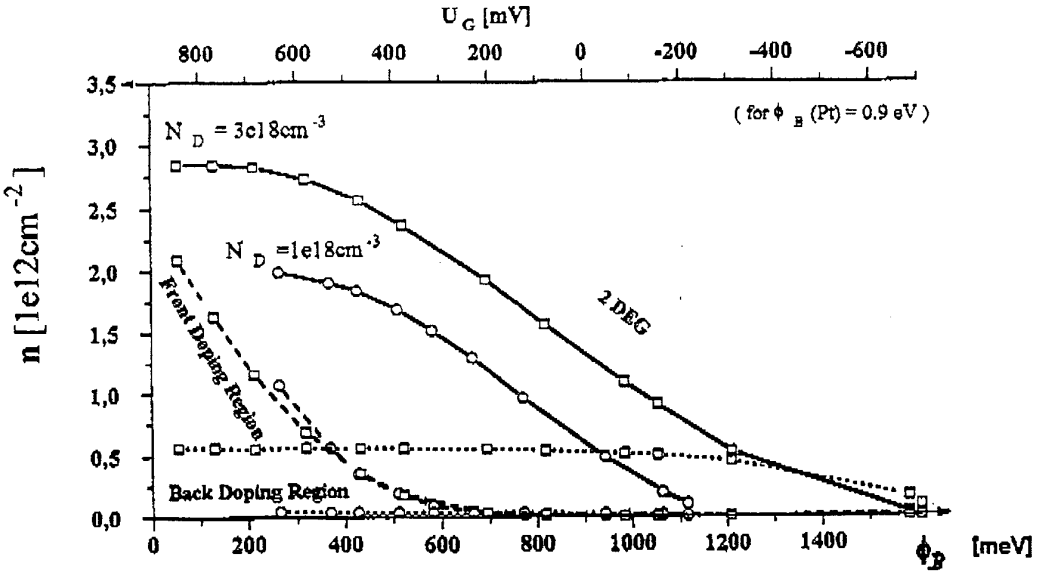

Fig. 3: Calculated carrier density in the 2DEG and in the doping regions for a double sided doped n-MODFET with two different back doping concentrations

Physical simulation of heterostructure devices. Application to device optimization and to improvements of the knowledge on the device behaviour

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The purpose of the paper is to show how physical simulations of heterostructure devices can be used for helping the designers to design optimized devices and to improve our knowledge on the device physical behaviour and main limitations.

First of all, different kinds of physical simulation methods will be briefly presented

- Monte Carlo or particle simulation tools ;
- 2D solutions of hydrodynamic and drift-diffusion equations ;
- Quasi 2D or one dimensional simplified model based on hydrodynamics or Schrödinger and Poisson equations.

The main advantages, drawbacks and respective domains of applications of these methods will be discussed.

Then, a lot of examples will be given :

- Contribution to the optimization of AlInAs/GaInAs HEMTs by using Monte Carlo simulation ;
- Influence of the recessed zone configuration of pseudomorphic HEMT's on the expected performance and breakdown behaviour (2D and quasi 2D model) ;
- Study of 2D effects in GaInP/GaAs HBT's under large signal conditions ;
- Breakdown behaviour and dispersion effect in LT GaAs MISFET's and consequences in the device optimization.

Some conclusions will be drawn for the future in term of capabilities of such methods, mainly with respect to the progress of computers and numerical methods.

HETEROSTRUCTURE TECHNOLOGY
WORKSHOP

SESSION E
Opto-electronic Applications

1 High speed opto-electronics, lasers, modulators and switches.
C. Ironside. INVITED TALK.

2 Carrier distribution and carrier leakage in $Ga_X In_{1-X} P/Al_y Ga_{1-y} InP$ visible emitting quantum well lasers.
P. M. Snowton, P Blood and P.J. Hulyer

3 Optically induced birefringence and spin polarisation relaxation in quantum wells.
T. Grevatt, R.E. Worsley and R.T. Harley.

4 The passivation of III-V semiconductors laser devices.
P.R.Dunstan..

5 Properties of InGaAs HEMT and photodetector prepared on an identical layer structure.
M. Horstmann, K. Schimpf, M Marso, A. Fox. H . Hardtdegen, H. Luth and P. Kordos.

6 Analysis and modelling of spectral response for GaAs Schotty diodes and InP/InGaAs HPTSs fabricated using transparent Indium Tin Oxide.
S.A. Basher and A. A. Rezazadeh.

7 ITO/AlGaInP LEDs:The effect of the variation of GaAs cap layer and cladding layer thickness on device performance.
Y. H. Aliyu, D. V. Morgan, H. Thomas and S.W.Bland.

High Speed Opto-electronics: lasers, modulators and switches

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The theme of this talk is high speed optoelectronics. In particular, results from three projects are considered as follows.

The monolithic modelocking of semiconductor lasers can produce picosecond pulses of light at repitition frequencies of up to 375 GHz. This is from a single chip device which is compact, reliable, robust and efficient.

The incorporation of a Resonant Tunnelling Diode in an optical waveguide provides both negative differential resistance from DC to several hundred GHz and electroabsorption. The possibility of making a high speed electroabsorption modulator from this structure is discussed.

All -optical swithching in semiconductor waveguides has been achieved for optical pulses as short as 150 fs with peak powers of around 40W

Carrier Distribution and Carrier Leakage in $Ga_xIn_{1-x}P$ / $Al_yGa_{1-y}InP$ Visible Emitting Quantum Well Lasers

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High temperature operation of GaInP / AlGaInP quantum well lasers is of interest due to the expected deployment of such lasers in short haul communication systems employing plastic fibres or waveguides.

Carrier leakage processes have a major impact on the behaviour of visible emitting GaInP quantum well lasers, particularly at high temperatures where laser threshold current increases dramatically as shown in figure 1. Lasers with a composition profile of the general form represented in figure 2 have been investigated by analysis of measurements of spontaneous emission spectra as functions of temperature and current allowing us to determine the distribution of carriers between well and barrier regions under lasing conditions. Combining this with threshold current data, we find that the chief source of carrier leakage is via the X-conduction band of the confining layers. Our measurements are in excellent agreement with recent band gap data and since this data shows that the X gap is insensitive to composition we can explain the otherwise counter intuitive improvement in threshold current of samples with a reduced waveguide aluminium content (y) that is apparent in figure 1.

We thank A.J. Moseley and D.J. Robbins for valuable discussions.
This work was done with the support of the DTI/EPSRC LINK Optoelectronics Programme, and the structures were grown by EPI Ltd., Cardiff.

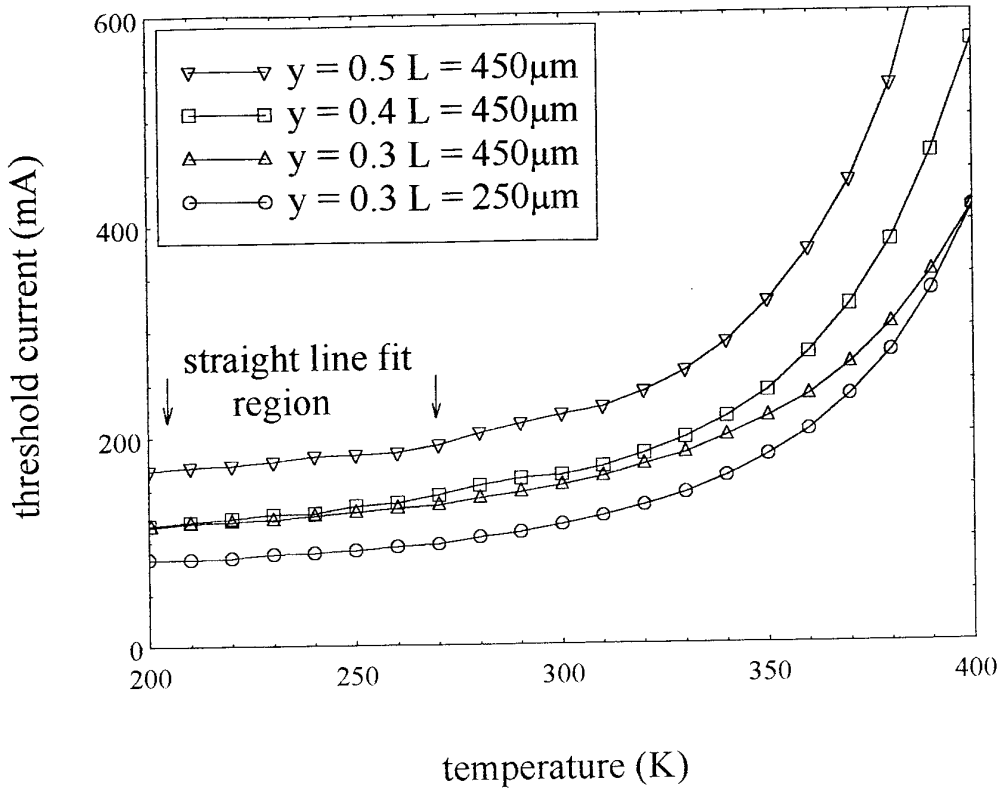

Figure 1: Threshold current measurements as a function of temperature for devices with y=0.3 (250μm and 450μm long), 0.4 (450μm long) and 0.5 (450μm long).

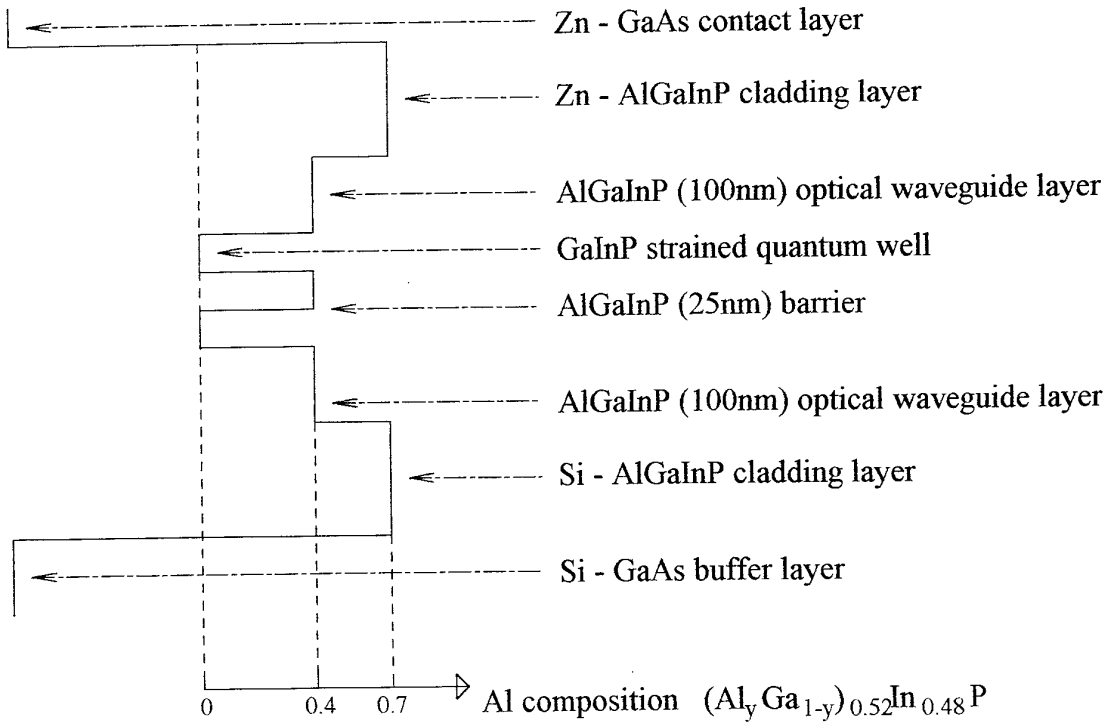

Figure 2: Composition profile of the laser structure used in this work

OPTICALLY INDUCED BIREFRINGENCE AND SPIN POLARISATION RELAXATION IN QUANTUM WELLS

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A great deal of work is currently being performed to develop suitable materials for high speed optoelectronic applications, such as, optical computers and switches. Due to their greatly enhanced optical nonlinearity, semiconductor heterostructures have attracted much investigation. The study of the ultrafast dynamics of a non-equilibrium carrier distribution in such materials is of both fundamental and technological interest. Recent developments in the field include picosecond all-optical switching using circularly polarised light in GaAs/AlGaAs multi-quantum well structures due to picosecond spin polarisation relaxation [1].

Traditionally, time-resolved four-wave mixing techniques have been used to investigate the coherence properties of carriers in semiconductor quantum wells [2] and it is now possible to study directly the dynamics of, for example, carrier scattering by phonons or defects. In this paper we wish to present a different type of measurement which may also be used to investigate coherent transients in heterostructures.

We consider the lowest energy heavy hole exciton transition in type I GaAs/AlGaAs multi-quantum well structures. The exciton state, when including the electron ($m_j = \pm 1/2$) and hole ($m_j = \pm 3/2$) spins, consists of two doublets characterised by different spin components for the particles, separated by the exchange energy. The lower of the two doublets is optically forbidden whereas the upper doublet is allowed and has eigenvectors corresponding to σ^+ and σ^- optical polarisation for light propagating along the growth axis.

Resonant excitation with a short pulse of linearly polarised light will generate equal populations of the two allowed exciton polarisations. These populations cause a nonlinear change in the optical response of the system which will decay in the exciton recombination time. However, initially the two populations will be coherent with the excitation pulse giving a net linear induced macroscopic polarisation in the sample. This will give a nonlinear birefringence with a unique axis defined by the exciting polarisation and will decay in the dephasing time of the excitons.

We have used a pump and probe, nonlinear reflection measurement to investigate these effects. We can obtain the exciton recombination time and the spin relaxation time by using circular polarisations for the pump and probe pulses. Linear pump polarisation is found to induce birefringence, as predicted, and we are able to investigate the temperature and exciton density dependence of the dephasing time.

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[2] See for example: *Coherent Optical Interactions in Semiconductors* Edited by R.T. Phillips NATO ASI Series, Plenum Press, New York and London (1994)

The Passivation of III-V semiconductor laser devices

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Abstract

High quality clean cleaved surfaces of GaAs and most III-V semiconductors are free of surface states in the fundamental band gap. However, imperfections such as steps, contaminants or defects can lead to band gap states which in turn can lead to high surface recombination rates. These states, together with phenomena such as effective band gap narrowing, can lead to rapid degradation in laser structures. In an attempt to increase the performance of semiconductor devices, research has increased substantially in the passivation of the surface gap states of III-V semiconductors. It is believed that surface gap states enhance the nonradiative recombination in laser devices. This occurs at laser facets and initiates a catastrophic optical degradation (COD) which thus kills the device.

Laser facet passivation offers a means by which these devices may be improved. The passivation of GaAs (110) is being investigated using several experimental techniques, x-ray photoelectron spectroscopy (XPS), scanning tunneling micropscopy (STM), scanning tunneling spectroscopy (STS), and capacitance-voltage measurements. Overlayers of silicon are being deposited and their reaction with GaAs monitored. The overlayers effect on the band structure of the GaAs has been studied, particularly from the aspect of band bending. The understanding of the physics and chemistry of the interface between the laser facet and the passivation coating is required for further device improvement.

Properties of InGaAs HEMT and photodetector prepared on an identical layer structure

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At the preparation of monolithically integrated photoreceivers a two-step epitaxy to form the photodetector and amplifier or a sequential growth with an isolating layer between them are used. In the last time considerable attention is given to the preparation of both devices on an identical layer structure. This procedure has been recently applied to pin-PD / HBT counterpart [1], but HEMTs show better microwave performance. We report the properties of InGaAs based HEMT and photodetector prepared on an identical epi-layer structure.

The devices are fabricated in the InP/InGaAs material system, without use of Al-containing layers, by LP-MOVPE growth [2]. Pseudomorphic HEMTs with different gate length from 1.5 μm down to 0.35 μm have been prepared - details can be found in [3]. The photodetectors consist of MSM double-Schottky barrier diodes above a 2DEG structure [4]. In this study an 150 nm thick lattice-matched InGaAs layer between InP barrier and InGaAs channel layers is used to establish a compromise between photodetector sensitivity and HEMT performance. DC and RF (130 MHz to 26.5 GHz) properties of both devices were evaluated.

Obtained results can be summarized as follows:

- The photodetector has a sensitivity of 0.4 A/W without an antireflection coating. The 1.3 μm pulse response FWHM with a finger spacing of 3 μm is ~60 ps (Fig. 1), which is the resolution limit of our RF lightwave test set.
- The HEMT has a cutoff frequency of 45 GHz and an f_{max} of 85 GHz at a gate length of 0.35 μm (Fig. 2), which are only slightly lower values than that of optimized discreet InGaAs HEMTs.
- The capabilities of InGaAs based HEMTs and MSM photodetectors realized on the same layer system with compatible processing steps are demonstrated. The two devices can easily be used for monolithically integrated photoreceivers.

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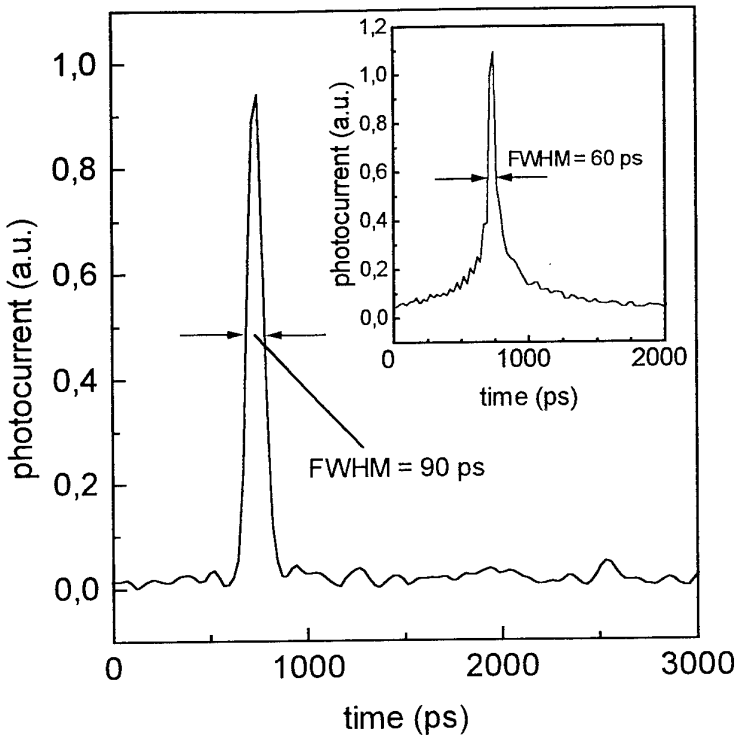

Fig. 1. The 1.3 μm pulse response of InGaAs MSM photodetector.

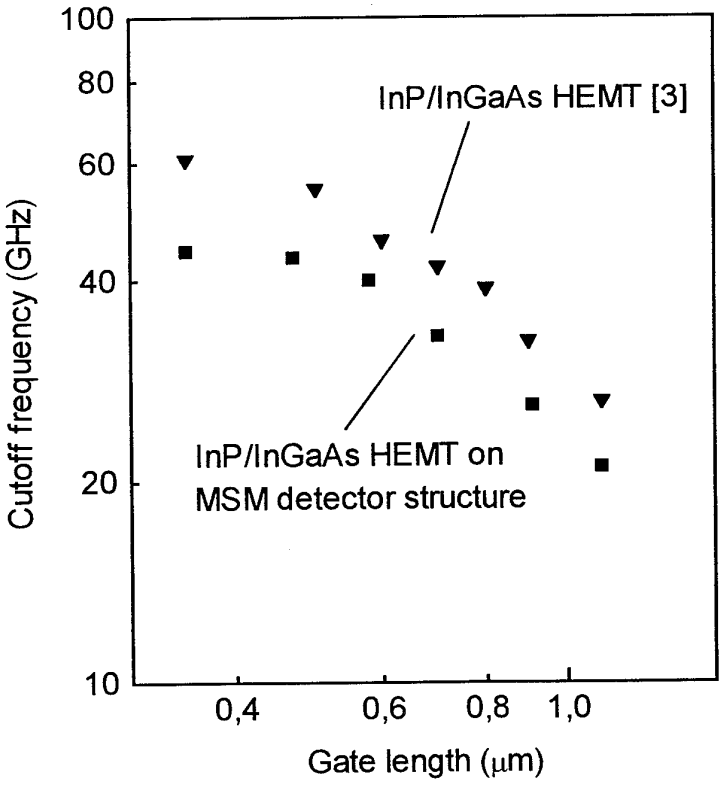

Fig. 2. Variation of f_T with gate length for InGaAs HEMTs

Analysis and Modeling of Spectral Response for GaAs Schottky diodes and InP/InGaAs HPTs fabricated using transparent Indium Tin Oxide

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Abstract:

Based on the principles of light transmission, absorption and reflection in different semiconductor materials, the spectral responses of two types of photo detectors fabricated from two different material systems were simulated : an ITO/n-GaAs Schottky photodiode and an ITO emitter contact InP/InGaAs heterojunction bipolar phototransistor (HPT). Extremely good correlation between the experiment and the model were obtain in both cases as shown in figures 1 and 2. Using this technique it is now possible to tailor yet a third device parameter in addition to the gain and the speed, namely the wavelength at which the responsivity is a maximum for a given optoelectronic device.

The fabrication and structural details of the Schottky diode and the HPT have been published elsewhere [1,2]. Device parameters such as the doping, the ITO and the semiconductor layer thickness as well as the material properties such as the absorption coefficient, α, the refractive indexes, n, and the generation efficiency were used from the literature for the purpose of simulation [3-6]. A 100% collection efficiency is assumed for any electron-hole pairs photogenerated inside a depletion region or within a diffusion length from it. The following basic equations were used to determine the amount of actual absorption in the active layer of the photo detector, thus the responsivity, R as a function of the wavelength, λ for the Schottky diode :

$$R(\lambda) = \Phi_o(\lambda) \times (1-R_1(\lambda)) \times T_{ITO}(\lambda) \times (1-R_2(\lambda)) \times \Phi_{abs}(\lambda) \quad (1)$$

where, at a given wavelength,

Φ_o = the flux incident at the air/ITO surface
R_1 = reflection caused at the air/ITO interface
T_{ITO} = transmission of ITO
R_2 = reflection caused at the ITO/GaAs interface
Φ_{abs} = flux absorbed in the semiconductor active layer

Thus for the HPT the above generic equation is used for each layer in succession with the appropriate values of α, n and the layer thickness to determine the theoretical absorption in them; in order to calculate the absorption in each layer, any reflection and absorption in previous interfaces (different refractive indexes) and layers is thus accounted for. Subsequently, the device responsivity is given by :

$$R_{HPT}(\lambda) = \Phi_{cap}(\lambda) + \Phi_{emitter}(\lambda) + \Phi_{collector}(\lambda) + \beta(\Phi_{base}(\lambda) + \Phi_{collector}(\lambda)) \quad (2)$$

where, at a given wavelength,

Φ_{cap} = flux absorbed in the (n^+ InGaAs) cap layer
$\Phi_{emitter}$ = flux absorbed in the (n InP) emitter
$\Phi_{collector}$ = flux absorbed in the (n InGaAs) collector
Φ_{base} = flux absorbed in the (p^+ InGaAs) base
β = DC common emitter current gain of the transistor

In both cases, and indeed for any other optoelectronic detector taking into account the appropriate device physics, the spectral, S_{Resp}, response can thus be found by integrating over the entire operational wavelength range :

$$S_{Resp} = \int R(\lambda)d\lambda \tag{3}$$

Any mismatch between the simulation and the measured data is due to the uncertainties in the literature, the lack of absolute device layer dimensions and non-linear effects of the monochromator around 800nm (Fig. 1) and the atmospheric absorption around 1400nm (Fig. 2).

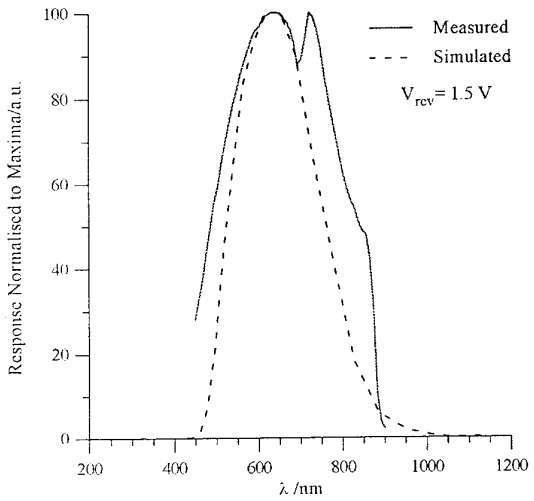

Figure 1 : Spectral response of ITO/n-GaAs Schottky photo diode

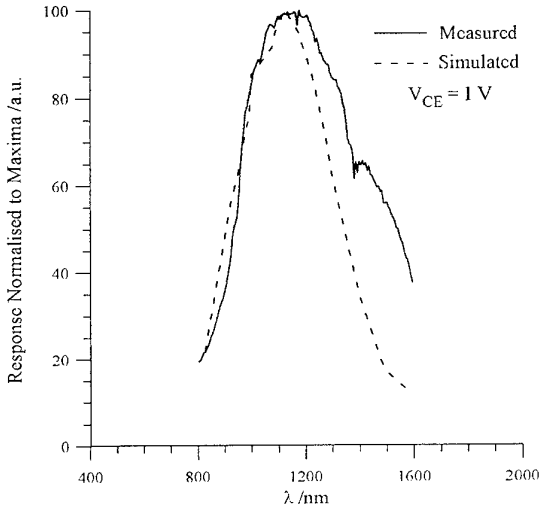

Figure 2 : Spectral response of ITO emitter contact InP/InGaAs HPT.

Acknowledgements :

S. A. Bashar would like to thank Prof. J. G. Swanson, Dr. S. E. Kanellopoulos and Dr. Q. H. Wang of King's College London for their valuable technical discussions.

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ITO/AlGaInP LEDs: The Effect of variation of top GaAs Cap layer and the cladding layer thicknesses on the device performance.

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AlGaInP light emitting diodes (LEDs) which have light output vastly superior to the existing technologies have been recently demonstrated[1]. AlGaInP quaternary alloy is lattice matched to GaAs, with a wide bandgap in which direct energy transitions occur in the spectral region between green and red. AlGaInP LEDs can be used for applications that require either high output power or low power consumption. Two key issues that affect the performances of these devices are the substrate absorption losses that limit the external efficiency of the LEDs and the growth of a high conductivity material on top of the DH layers that is necessary to spread the current out from the opaque top metal contact. The use of transparent conducting Indium-Tin-Oxide (ITO) as contact material seems promising due to its interesting combination of properties, namely visible transparency and high electrical conductivity. ITO/AlGaInP LEDs are expected to have light output superior to that of the standard LED with metal opaque contact. However, only a comparable performance was observed, with a marginally greater light output in the ITO devices by 10%[2]. To maximise light extraction from the active layer, it is necessary to optimise various design parameters in the DH structure.

This paper describes the effects of variation of top GaAs cap layer and the p-type AlGaInP cladding thicknesses on the performance of ITO/AlGaInP LEDs. AlGaInP layers were grown on n^+Gaas substrates by low pressure Metal Organic Chemical Vapour Deposition(MOCVD). The devices consist of a quaternary undoped active region bounded by a p and n-type AlGaInP cladding layers doped with Zn and Si respectively. The thicknesses of the upper p-type cladding layer was varied between 0.05 μm to 5.0 μm. The highly doped p-type GaAs cap layer (10^{19} cm^3) was also varied from

0.03 μm to 0.05 μm in order to study their effects on the performance of the LEDs. Transparent conducting ITO layer was deposited on the DH layers to expand the light emission area and hence improve the extraction by acting as a window layer. Metal bonding contacts were fabricated on the LEDs by depositing Au-Zn on the ITO and alloyed Au-Ge(Ni) contact to the n-type GaAs substrate. The sizes of the LEDs are 300 μm x 300 μm with 100 μm Au-Zn dot, which also used for external connection. A schematic diagram of the device structure is shown in Figure (1). The devices were characterised by Current-Voltage(I-V), Capacitance-Voltage(C-V), Light-Current(L-I) and Light-Voltage(L-V) and Spectral Response(S-R). Figure (2) shows a typical light output intensity versus the dc current characteristics for each combination of cladding layer and GaAs thicknesses (see table 1). It is observed that reducing the thickness of the highly doped p^+ GaAs cap layer from 0.05 μm to 0.03 μm causes a reduction in the light intensity by more than 40%. Increasing the thickness of the p-type AlGaInP cladding layer from 0.05 to 1.0 m reduced the light intensity by up to 20%. However, a significant improvement of light intensity was achieved by increasing the p-type p-type AlGaInP layer from 1.0 μm to 5.0 μm. This is attributed at least in part to the enhancement of emission through the sides of a thicker window layer. Total light output in LEDs has been shown to be a function of window thickness[3]. In summary the total light output in the LEDs have been shown to be dependent on the thickness of both the cladding layer and the highly doped p^+-GaAs cap layer.

Acknowledgements

We acknowledge the EPRSC and the Epitaxial Products International, St. Mellons, Cardiff UK for the support of this work.

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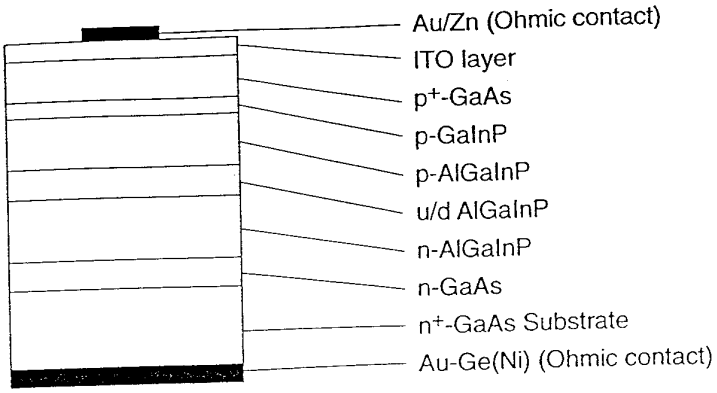
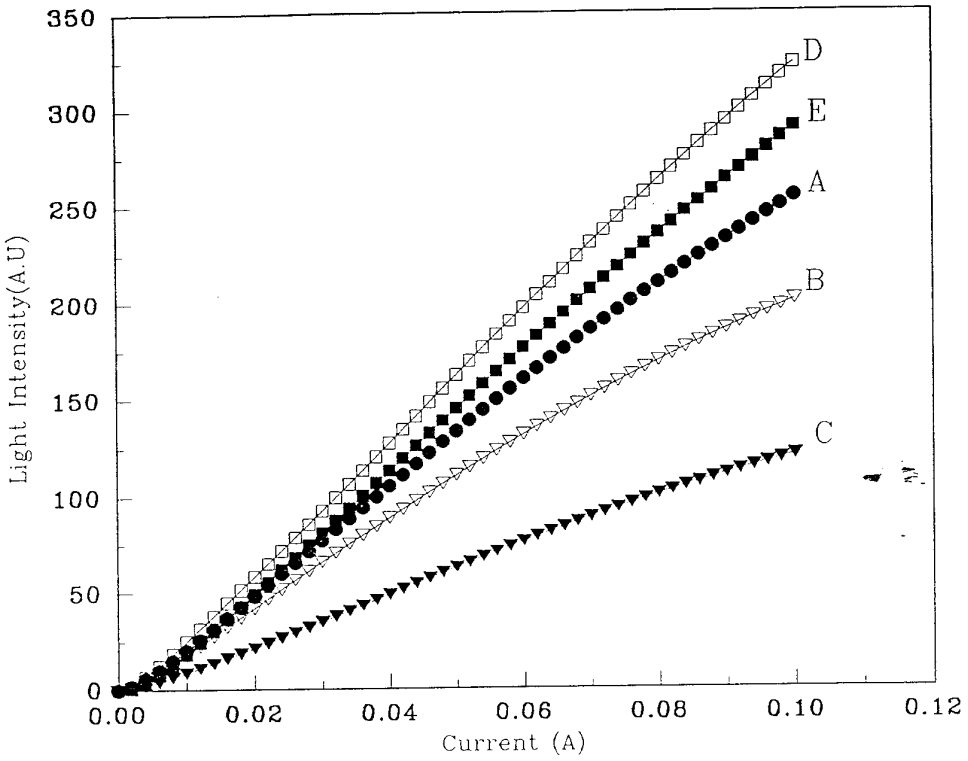


Figure 1: Schematic diagram of ITO/AlGaInP LED (not to scale)

Device No.	P^+GaAs cap layer (μm)	p-type cladding layer(μm)	n-type cladding layer(μm)	Contact type
A	0.05	0.5	0.5	ITO
B	0.05	1.0	1.0	ITO
C	0.03	1.0	1.0	ITO
D	0.05	5.0	1.0	ITO
E	0.05	5.0	1.0	non-ITO (standard)

TABLE (1) : Showing all combinations of GaAs cap layer and the n and p-type cladding layers thicknesses used in the device structures.



Figure(2) Light intensity results for the different device structures

HETEROSTRUCTURE TECHNOLGY
WORKSHOP

SESSION F
Device Technology

1 Planar integration of single and double barrier quantum devices.
E. Lheurette, P. Mounaix, P. Salzenstein, F. Millet and D. Lippens.

2 High Frequency (200-600 GHz) integration of quantum barrier devices in compound semiconductors grown by MBE.
D.P. Steenson, R.E. Miles and R.D. Pollard.

3 Airbridge technology for millimeter wave power FETs.
F.Diette, D. Theron, B. Bonte and Y. Crosnier.

4 A self-aligned process for complementary HFET IC fabrication.
J.F. Thiery, H. Fawaz, J-C Pesont and G. Salmer.

5 Selective wet etching of lattice matched InGaAs/InAlAs/InP metamorphic InGaAs/InAlAs/GaAs layers using Succinic Acid/ Hydrogen peroxide and Methyl - Succinic Acid/ Hydrogen peroxide solutions.
H. Fourre and A. Cappy.

5th European Heterostructure Technology Workshop, Cardiff, 17-19 September 1995

PLANAR INTEGRATION OF SINGLE AND DOUBLE BARRIER QUANTUM DEVICES

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$In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$/AlAs Single Barrier Varactors (SBV's) and $In_{0.53}Ga_{0.47}As$/AlAs double barrier Resonant Tunnelling Diodes (RTD's) were integrated in a planar configuration for probing the devices at the wafer level in order to assess their frequency capabilities. The technological process involves e-beam writing of pattern at submicron scale, double step mesa isolation by reactive ion etching and chemical etching, low resistance AuGeNi ohmic contact fabrication and electroplated air-bridges to interconnect the devices to the footprints of coplanar lines. A high degree of symmetry was found in the current-voltage characteristics of SBV's with low leakage current density up to 5 V where Fowler-Nordheim effects occur. This attests the quality of the epitaxy which was designed with a strained blocking AlAs barrier. RTD's exhibit simultaneously high peak current densities ($Jp = 1.75 \times 10^5$ A cm^{-2}) and peak-to-valley ratios (Jp/Jv = 5:1) which are the order of magnitude of the best results found in the literature. These tunnelling devices have been subsequently characterised with a network analyser up to 40 GHz. On one hand for SBV's, we have measured capacitance ratios (C_0/C_{sat}) equal to 3.5:1. On the other hand, thanks to the very low inductance of the interconnecting elements afforded by the integration, RTD's were found unconditionally stable over a large voltage range of the negative differential conductance region where the frequency dependence of the small-signal impedance was measured. Analysis of data permits us in a second stage to estimate the maximum oscillation frequency by tracking the resistive cut-off frequency. Submillimeter wave operation are expected on the basis of the extremely high current density and low access resistance (contact resistivity of 6×10^{-7} Ωcm^2) which compares favourably to the best results published for InGaAs-base quantum effect devices.

High Frequency (200-600GHz) Integration of Quantum Barrier Devices in Compound Semiconductors Grown by MBE

D.P. Steenson, R.E. Miles, R.D. Pollard
Microwave and Terahertz Technology Group, Dept of E & EE, Leeds University

The last ten years have seen the emergence of two and three terminal devices which depend on quantum mechanical tunnelling for their operation. Atomic layer control of the "active" region (afforded by MBE growth) permits accurate control of the tunnelling properties and hence the current-voltage and capacitance-voltage characteristics. In the specific case of devices based on double barriers, an enhancement of the tunnelling current over a range of biases leads to negative differential resistance (NDR) which can be used to generate power at frequencies as high as 712GHz. Quantum barrier devices (QBD's) can replace the Schottky devices in many applications where the extra degree of control of the current-voltage characteristics is advantageous. In applications such as sub-millimetre wave (room temperature) receivers QBD's exhibit excellent performance as odd-harmonic multipliers and sub-harmonic mixers. One such single (DBRTD) device has provided conversion gain at an intermediate frequency of 40MHz when mixing its self-generated signal at 10.94GHz with an incident signal of 10.9GHz.

Work is ongoing at the University of Leeds (in collaboration with the Universities of Nottingham, Bath and Reading) to incorporate these quantum barrier devices in both Planar and Waveguide circuits for operation at 100-600GHz. In order to realize the very small waveguide circuits for use at 600GHz, a novel on-wafer integrated waveguide approach has been pioneered at the University of Bath (Dr N. Cronin, Dept. of Physics) and efforts are being undertaken to incorporate the necessary components (mixers, oscillators and filters) to fabricate a down-converter at 200GHz and 600GHz. Device designs are proceeding along alternate paths (Waveguide and Planar) which depend on their eventual integrated application. At frequencies as high as 600GHz the device may behave more like a distributed circuit and studies of the electromagnetic fields in the vicinity of the "active" area's are being undertaken to evaluate the coupling of the incident radiation into and out from these regions of the device.

I shall present information regarding the fabrication of both planar and non-planar quantum barrier devices and their interaction with millimetre wave circuits.

Airbridge Technology For Millimeter Wave Power FET's

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Abstract:

High gate development FET's used for power application need interconnections between the source pads. These connections can be realised by via-holes or bridges.
The first method is very difficult to be implemented when the component size becomes very small. This is particularly the case when the FET's are planned to work at frequencies above 30GHz.

Hence, we are interested in the air bridge technology. Meanwhile, they have the disadvantage of introducing parasitic elements such as inductances and capacitances. Therefore, the optimisation of the geometry is required.

Our work starts by the technological effort in relationship with the bridge realisation reliability. The air bridges are made in two steps. The first one consists in defining the pillars by optical lithography. The second stage consists in defining the deck, also by optical lithography, after the deposition of a metallic film in order to optically separate the two photoresists. When the airbridge metallization is deposited, it remains to do the lift-off. It is during this last step that the principal problem appears. Indeed, the lift-off is difficult because the metallic film previously deposited make nibbles likely to short-circuit the components.

We have developed two processes. The first one uses evaporation and the second one uses electroplating. Both enable to avoid the nibble problem (photo. 1), are compatible with the use of the thick photoresist layers involved in the deck definition (fig. 2) and ensure the reliability. This process has been applied to air bridges with different size, width and height.

We have measured the capacitance at the drain side of structures with 2 to 12 gate fingers. The finger width is equal to 50µm. It appears for structures with 12 fingers that the capacitance can be reduced between 10 and 25fF lower according to the bridge configuration, when its height increases from 1 to 6µm.
We have also determined the source inductance for different structures. These inductances are strongly penalising at millimeter wave frequencies[1]. The evolution represented in fig. 3 shows minima for structures with two bridges.

Our study allows to master the technologies such that we obtain 100% of yield for the bridge realisation stage. It has also allowed to show the parasitic element evolution as a function of the bridge number and geometry, and to determine the optimal bridge configuration for power FET realisation in the millimeter wave range.

[1] : C.GAQUIERE et al "Analysis of the source inductance effect on the power performance of high development HEMT's in the Ka band" accepted for publication in IEEE Micowave Guided Wave Letters 1995

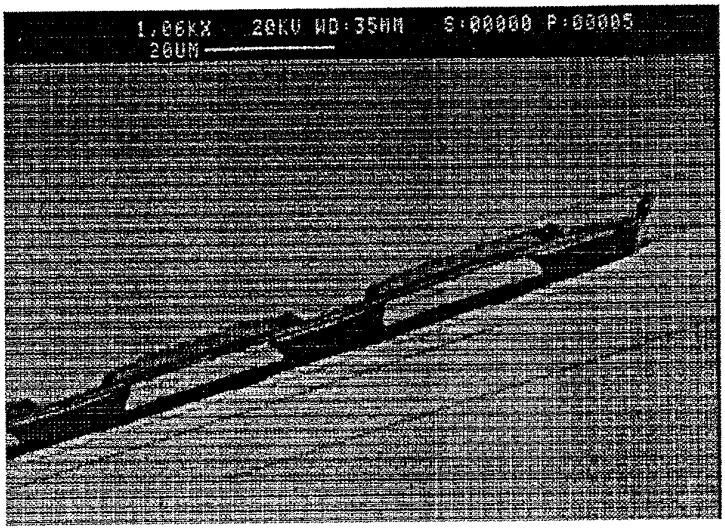

Photo.1 : SEM photography of bridge at 6µm high.

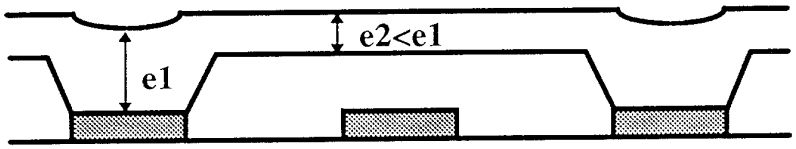

Fig.2 : Photoresist profile for the deck definition.

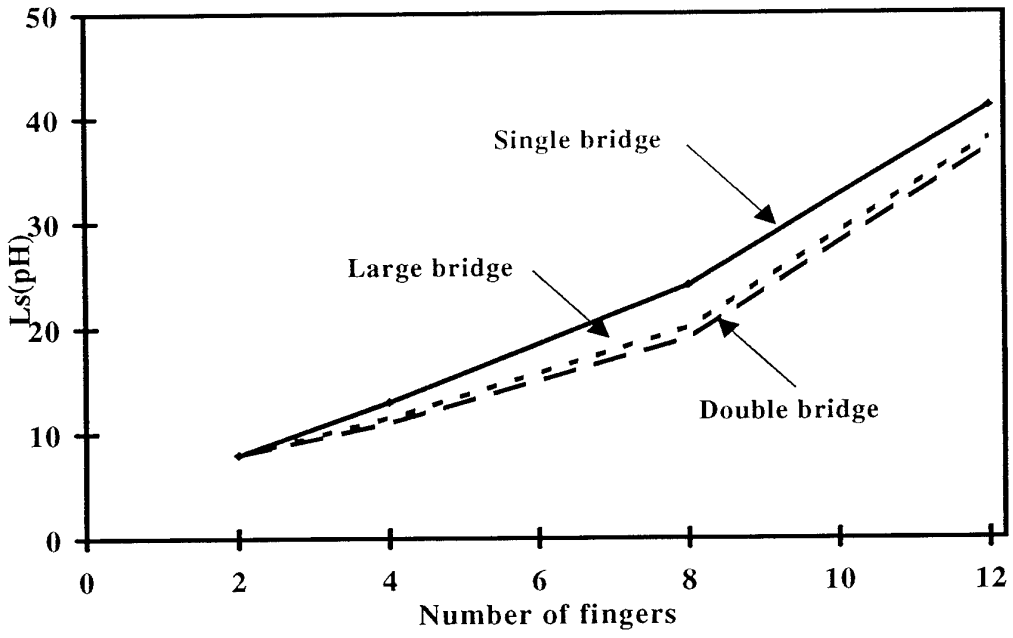

Fig.3 : Evolution of the inductances of source versus the number of the fingers and the geometry for decks at 6µm high.

A self-aligned process for complementary HFET IC's fabrication

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Future systems involved in information highways, fast computers or telecommunications, will require very high speed / ultra low power consumption digital IC's. In this domain, complementary GaAs structures exploit a better mobility and an ability to work at reduced voltages, and thus offer a serious advantage over the silicon CMOS[1]. The complementary pseudomorphic $Al_{0.75}GaAs$ / $In_{0.25}GaAs$ / GaAs Heterostructure Insulated Gate Field-Effect Transistor (HIGFET) structure has demonstrated interesting results[2,3]. We present a self-aligned complementary process for manufacturing N and P HIGFETs, and give some first technological results.

Figure 1 gives a schematic cross-section of the HIGFET epitaxial structure, and the self-aligned process is detailed in figure 2.

The first step consists in the sputtered WSi refractory Schottky gate deposition. Unlike gold-based metallizations, refractory metals are very robust to high temperatures induced by doping annealings, although they suffer from a higher resistivity. The gate patterning involves negative resist, e-beam lithography and reactive ion etching (RIE). In order to avoid lateral leakage current on surface, SiO_2 side-walls are formed by plasma-enhanced chemical vapor deposition and RIE. To prevent surface defects and to obtain a high doping at the surface, implantation is made through a cap of Si_3N_4 (table 2). For the n+ doping, we have optimized a Si double implantation consisting of two implants of 4.10^{13} cm^{-2} at 60 keV and 8.10^{13} cm^{-2} at 80 keV, and we have obtained a sheet resistance of 145 Ω/sq. For the p+ doping, a coimplantation of Mg (5.10^{14} cm^{-2} at 70 keV) and As (10^{14} cm^{-2} at 110 keV) lead to a sheet resistance of 450 Ω/sq. The wafer is capped with Si_3N_4 and annealed at 850 °C during 10s in order to activate both N and P implants.The Si_3N_4 cap is then removed by RIE. Ohmic contacts are deposited by e-beam evaporation (figure 3). A AuGe/Ni/Au n-type ohmic contact was optimized on our doped pseudomorphic structure and an excellent contact resistance of 0.07 Ω.mm was achieved after annealing at 420 °C during 10s (fig. 3a). A novel Au/Mn/Ni/Au p-type ohmic contact was demonstrated on GaAs and lead to an extremely low contact resistance of 0.02 Ω.mm after annealing at 380 °C during 40s (fig. 3b). This contact will be optimized on our structure. Finally, contacts are thickened by a Ti/Au metallization.

The complete technological process uses 9 mask levels and involves both e-beam and optical lithography. The epitaxial structure and almost all the steps were optimized and some significant results were obtained, by means of gate resistivity, side-walls, doping and ohmic contacts. Some N and P separate components measurements and complementary logic characteristics will be presented in a close future.

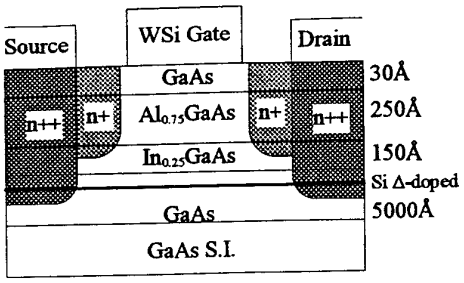

Figure 1 : Cross-section of the HIGFET epitaxial structure

Energy (keV)	Dose (cm^{-2})	Sheet resistance (Ω/sq)
60	$4.\ 10^{13}$	280
60	$4.\ 10^{13}$	145
80	$8.\ 10^{13}$	
40	$4.\ 10^{13}$	310
60	$4.\ 10^{13}$	
80	$8.\ 10^{13}$	

(a)

Energy (keV)	Dose (cm^{-2})	Sheet resistance (Ω/sq)
50	10^{14}	1140
50	10^{14}	720
70	10^{14}	
70	$2.\ 10^{14}$	560
70	$5.\ 10^{14}$	450

(b)

Table 1 : Sheet resistance of Si (a) and Mg (b) implants after annealing at 850°C during 10s

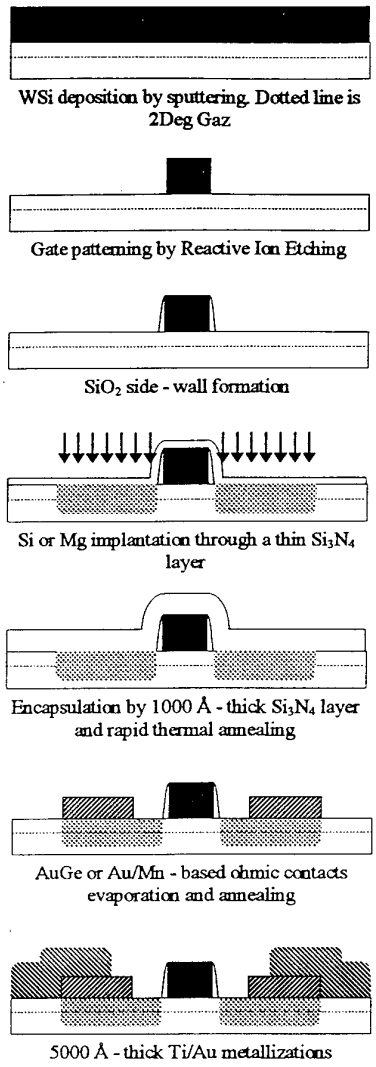

Figure 2 : Complementary process steps

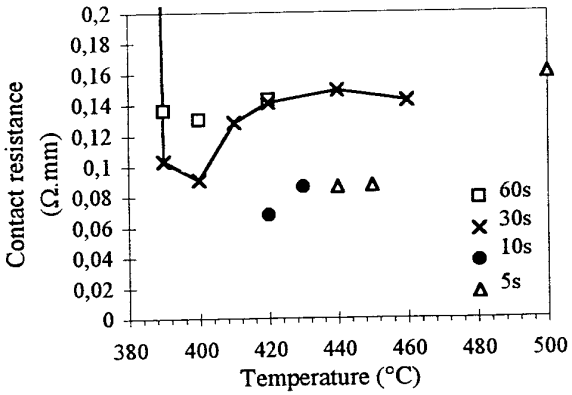

Figure 3a : Contact resistance of AuGe/Ni/Au ohmic contact on n-HIGFET structure after different annealings

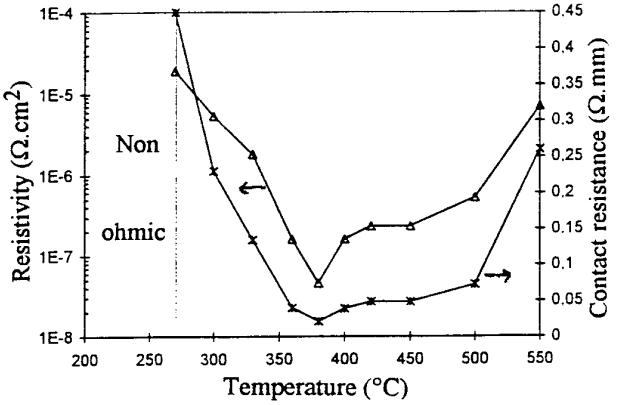

Figure 3b : Contact resistance and resistivity of p-GaAs/Au/Mn/Ni/Au ohmic contact after 40s annealing

REFERENCES:
1. J.K. Abrokwah et al., GaAs IC Symposium, p127, 1993
2. R.R. Daniels et al., IEDM, p236, 1991
3. J.K. Abrowah et al, GaAs IC Symposium, 1994

Selective Wet Etching of Latice-matched InGaAs/InAlAs/InP and Metamorphic InGaAs/InAlAs/GaAs layers using Succinic Acid/Hydrogen Peroxide and Methyl-Succinic Acid/Hydrogen Peroxide Solutions

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For the realization of HEMTs, an etching of the cap layer is usually performed prior to the gate realization. To improved the pinchoff voltage control and the process yield of GaInAs /AlInAs HEMTs, the selective wet etching of the InGaAs cap over the InAlAs Schottky layer is very well suited. According to previous work [1] wet chemical etching using succinic acid (SA) and methyl succinic acid (MSA) is investigated on metamorphic InGaAs/AlInAs layer on GaAs and InGaAs/AlInAs layer latice-matched on InP substrate. In this work, the etch rates, selectivities and etch profiles are investigated for different concentration volume ratios of succinic acid/hydrogen peroxide or methyl-succinic acid/hydrogen peroxide. Both acids have been regulated to a given pH (5 for Succinic acid, 3 for Methyl-succinic acid) by adding ammonium hydroxide (NH_4OH). The etches were performed at room temperature without stirring through a photoresist mask. It can be observed that the InAlAs etch rate depends on the Al mole fraction and decreases as the Al mole fraction increases (fig 1). The best obtained selectivities are 1030 with SA (pH=5) and 630 with MSA(pH=3) for metamorphic layers on GaAs. For latice-matched layer on InP, the measured selectivities are reduced to 70 with SA and 40 with MSA.

From these results we have chosen to analyse the under etch in short gate recess (0.1 µm and 0.2 µm) on InP latice-matched materials. The lateral width was measured after etching through a PMMA resist mask during 30 to 240 s using an Atomic Force Microscope. The measurements of the recess width were performed after removing of the resist. The solution which was used for this study is the SA/H_2O_2 30/6 which shows high selectivity (69) with a low InAlAs etch rate (fig 1). The sample used for this study is a lattice-matched HEMT epitaxial layer grown by GSMBE with a 100 Å InGaAs cap layer and a 250 Å InAlAs underlying Schottky layer. The lateral etch variation is linear with respect to the etch time and is greater than the measured vertical InGaAs etch rate (750 Å/min over 425 Å/min) (fig 2). We have also represented in this figure the measured depth of the recess versus time. It can be seen that the etch stops on the InAlAs Schottky layer. Moreover the SA etching solution does not erode the PMMA resist mask. In conclusion, the SA (pH=5)/H_2O_2 etching solution is suitable to realize the gate recess for latice-matched or metamorphic HEMTs using the same PMMA resist mask to etch the cap layer and to evaporate the gate metallization.

[1] : T.P.E. Broekaert and C.G. Fonstad, J.Electrochem. Soc, vol 139, No 8, 2306 (1992) Novel, Organic Acid-Based Etchants for InGaAlAs/InP Heterostructure Devices with AlAs Etch-Stop Layers

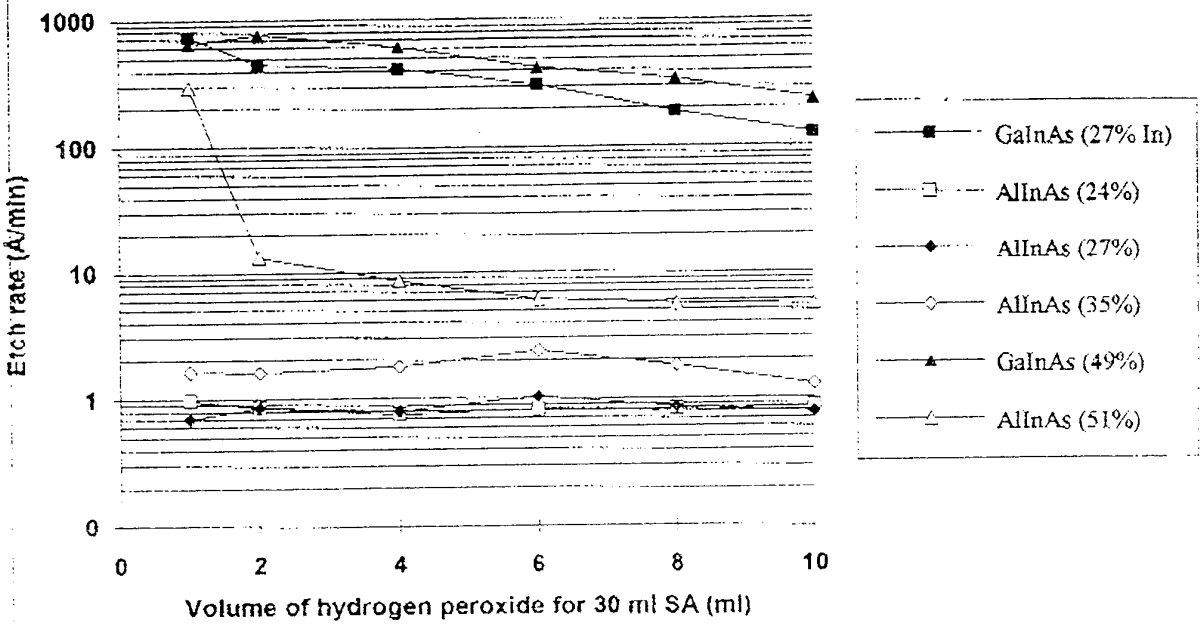

Fig 1 : Etch rate of lattice matched and metamorphic InGaAs and InAlAs with SA/H2O2 etching solution.

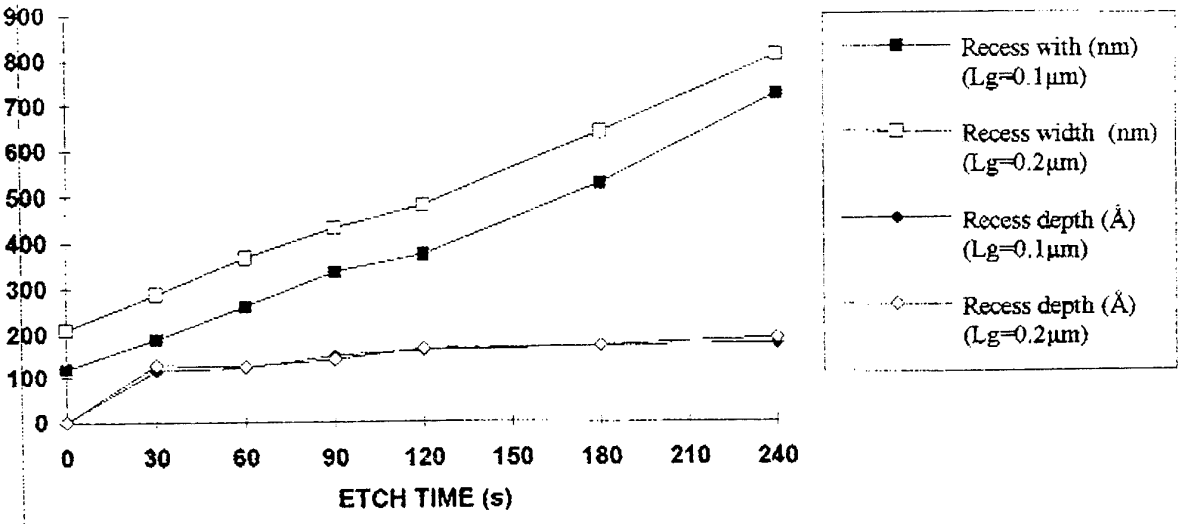

Fig 2 : Under resist ecth width and etch depth with SA/H2O2 etching solution