

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank) 2. REPORT DATE
1995 3. REPORT TYPE AND DATES COVERED

4. TITLE AND SUBTITLE
FD-TLM Simulation of Josephson Junction
Logic Circuits 5. FUNDING NUMBERS

6. AUTHOR(S)
Christopher G. Scutella

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
AFIT Students Attending:
Nebraska-LINCOLN 8. PERFORMING ORGANIZATION
REPORT NUMBER
95-148

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
DEPARTMENT OF THE AIR FORCE
AFIT/CI
2950 P STREET, BLDG 125
WRIGHT-PATTERSON AFB OH 45433-7765 10. SPONSORING / MONITORING
AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for Public Release IAW AFR 190-1
Distribution Unlimited
BRIAN D. Gauthier, MSgt, USAF
Chief Administration 12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

19960124 082

14. SUBJECT TERMS 15. NUMBER OF PAGES
131 16. PRICE CODE

17. SECURITY CLASSIFICATION
OF REPORT 18. SECURITY CLASSIFICATION
OF THIS PAGE 19. SECURITY CLASSIFICATION
OF ABSTRACT 20. LIMITATION OF ABSTRACT

FD-TLM SIMULATION OF JOSEPHSON JUNCTION LOGIC
CIRCUITS

by

Christopher G. Sentelle

Second Lieutenant, USAF

1995

130 Pages

Accession For	
NTIS	CRA&I ☒
DTIC	TAB ☐
Unannounced	☐
Justification	
By	
Distribution /	
Availability Codes	
Dist	Avail and/or Special
A-1	

Master of Science, Electrical Engineering
University of Nebraska-Lincoln

FD-TLM SIMULATION OF JOSEPHSON JUNCTION LOGIC CIRCUITS

Josephson junction (JJ) integrated circuits (ICs) are capable of operating at clock frequencies from 1 to 100 GHz. At these frequencies, analysis of signal propagation delay, crosstalk, dispersions, radiation, and reflections must be included to determine proper response of the circuit. Much effort is required in simulating high frequency behavior, where the cross-sectional dimensions of conductors are comparable to the signal wavelength, with conventional circuit simulation methods as SPICE. A simulation method capable of modeling high-frequency behavior by solving Maxwell's curl equations, the finite-difference transmission line matrix method (FD-TLM), is modified to model JJ logic circuits and provide simultaneous time-domain three-dimensional full-wave electromagnetic field and JJ device analysis. The FD-TLM method is further extended to model superconducting quantum interference devices (SQUIDs). Techniques for simulation and simulation results for a Josephson Atto-Weber switch (JAWS), a two-junction superconducting quantum interference device (SQUID), and a modified variable threshold logic (MVTL) gate are provided. Interconnection lengths are kept intentionally short so the FD-TLM simulations can be validated by conventional, low frequency, quasi-static analysis. The general behavior observed in FD-TLM simulation and good agreement with quasi-static conventional circuit simulation validate the FD-TLM method.

FD-TLM SIMULATION OF JOSEPHSON JUNCTION LOGIC CIRCUITS

Christopher G. Sentelle, MS

University of Nebraska, 1995

Advisor: Robert H. Voelker

Josephson junction (JJ) integrated circuits (ICs) are capable of operating at clock frequencies from 1 to 100 GHz. At these frequencies, analysis of signal propagation delay, crosstalk, dispersion, radiation, and reflections must be included to determine proper response of the circuit. Much effort is required in simulating high frequency behavior, where the cross-sectional dimensions of conductors are comparable to the signal wavelength, with conventional circuit simulation methods as SPICE. A simulation method capable of modeling high-frequency behavior by solving Maxwell's curl equations, the finite-difference transmission line matrix method (FD-TLM), is modified to model JJ logic circuits and provide simultaneous time-domain three-dimensional full-wave electromagnetic field and JJ device analysis. The FD-TLM method is further extended to model superconducting quantum interference devices (SQUIDs). Techniques for simulation and simulation results for a Josephson Atto-Weber switch (JAWS), a two-junction superconducting quantum interference device (SQUID), and a modified variable threshold logic (MVTL) gate are provided. Interconnection lengths are kept intentionally short so the FD-TLM simulations can be validated by conventional, low frequency, quasi-static analysis. The general behavior observed in FD-TLM simulation and good agreement with quasi-static conventional circuit simulation validate the FD-TLM method.

References

- [1] R. H. Voelker and R. J. Lomax, "Three-dimensional simulation of integrated circuits using a variable mesh TLM method," *Microwave and Opt. Technol. Lett.*, vol. 2, pp. 125-127, Apr. 1989.
- [2] M. Kamon, C. Smithhisler, and J. White, "FastHenry User's Guide," Research Laboratory of Electronics, Dept. of Elect. Engr. and Comp. Sci, Massachusetts Institute of Technology, Cambridge, MA, Sept. 13, 1994.
- [3] B. Johnson, *et al.*, "SPICE3 version 3e1 User's Manual," Dept. of Elect. Engr. and Comp. Sci., Univ. of California, Berkeley, CA, Apr. 1, 1991.
- [4] B. W. Char, *et al.*, *First Leaves: A Tutorial Introduction to Maple V*. New York: Springer-Verlag, 1992.
- [5] W. H. Press, S. A. Teukolsky, W. T. Vetterling, and B. P. Flannery, *Numerical Recipes in C*, 2nd ed. New York: Cambridge University Press, 1992.
- [6] S. Hasuo and T. Imamura, "Digital Logic Circuits," *Proceedings of the IEEE*, vol. 77, no. 8, pp. 1177-1190, Aug. 1989.
- [7] S. Takada, "Progress on Josephson Computer," *Nonlinear Superconductive Electronics and Josephson Devices*, Plenum Press: New York, 1991.

- [8] H. Jackel, W. Bachtold, "Computer-Simulation for Digital Josephson Devices and Circuits," *Circuit Analysis, Simulation and Design*. North-Holland: Elsevier Science Publishers, 1986
- [9] J. G. Rollins, "Numerical simulator for superconducting integrated circuits," *IEEE Trans. Computer-Aided Design*, vol. 10, pp. 245-251, Feb. 1991.
- [10] J. Clarke, "Principles and Applications of SQUIDs," *Proceedings of the IEEE*., vol. 77, no. 8, pp. 1208-1221, Aug. 1989.
- [11] T. P. Orlando and K. A. Delin, *Foundations of Applied Superconductivity*. Addison-Wesley Publishing Company: New York, 1991.
- [12] R. H. Voelker and C. G. Sentelle, "FD-TLM Modeling of Josephson Junction Circuits," *IEEE Microwave and Guided Wave Lett.*, vol. 5, pp. 137-138, May 1995.
- [13] T. VanDuzer and C. W. Turner, *Principles of Superconductive Devices and Circuits*. New York: Elsevier, 1981.
- [14] S. T. Ruggiero and D. A. Rudman, *Superconducting Devices*. Boston: Academic Press, 1990.
- [15] __, "A finite-difference transmission line matrix method incorporating a nonlinear device model," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 302-312, Mar. 1990.
- [16] R. H. Voelker and C. G. Sentelle, "Graphical modeling interface for FD-TLM electromagnetic field simulation of high-speed pulse propagation in active structures," in *Dig. 1994 IEEE AP-S Intl. Symp.*, Seattle, WA, June 1994, pp. 1120-1123.

- [17] G. Costabile, S. Pagano, N. F. Pedersen, and M. Russo, *Nonlinear Superconductive Electronics and Josephson Devices*. New York: Plenum Press, 1991.
- [18] M. A. Megahed, "Nonlinear Analysis of Microwave Superconductor Devices Using Full-Wave Electromagnetic Model," *IEEE Transactions on Microwave Theory and Techniques.*, vol. 43, no. 11, pp. 2590-2598, Nov. 1995.
- [19] C. G. Sentelle and R. H. Voelker, "FD-TLM Electromagnetic Field Simulation of High-Speed Josephson Junction Digital Logic Gates," *IEEE Transactions on Microwave Theory and Techniques.*, accepted for publication, Dec., 1995.

**FD-TLM SIMULATION OF JOSEPHSON JUNCTION LOGIC
CIRCUITS**

by

Christopher G. Sentelle

A THESIS

Presented to the Faculty of
The Graduate College at the University of Nebraska
In Partial Fulfillment of Requirements
For the Degree of Master of Science

Major: Electrical Engineering

Under the Supervision of Professor Robert H. Voelker

Lincoln, Nebraska

December, 1995

FD-TLM SIMULATION OF JOSEPHSON JUNCTION LOGIC CIRCUITS

Christopher G. Sentelle, MS

University of Nebraska, 1995

Advisor: Robert H. Voelker

Josephson junction (JJ) integrated circuits (ICs) are capable of operating at clock frequencies from 1 to 100 GHz. At these frequencies, analysis of signal propagation delay, crosstalk, dispersion, radiation, and reflections must be included to determine proper response of the circuit. Much effort is required in simulating high frequency behavior, where the cross-sectional dimensions of conductors are comparable to the signal wavelength, with conventional circuit simulation methods as SPICE. A simulation method capable of modeling high-frequency behavior by solving Maxwell's curl equations, the finite-difference transmission line matrix method (FD-TLM), is modified to model JJ logic circuits and provide simultaneous time-domain three-dimensional full-wave electromagnetic field and JJ device analysis. The FD-TLM method is further extended to model superconducting quantum interference devices (SQUIDs). Techniques for simulation and simulation results for a Josephson Atto-Weber switch (JAWS), a two-junction superconducting quantum interference device (SQUID), and a modified variable threshold logic (MVTL) gate are provided. Interconnection lengths are kept intentionally short so the FD-TLM simulations can be validated by conventional, low frequency, quasi-static analysis. The general behavior observed in FD-TLM simulation and good agreement with quasi-static conventional circuit simulation validate the FD-TLM method.

ACKNOWLEDGEMENTS

I would like to give special thanks to Dr. Rober H. Voelker for his support and encouragement during the term of this project. I would also like to thank Dr. Voelker for his understanding during my difficult semester in the fall of 1994. I would like to give thanks to Dr. Alexander and the Center for Electro-Optics for financial support during this project. I would like to thank my parents for their encouragement and understanding in my life. Finally, I would like to give special thanks to my wife for her unending understanding, support, and encouragment.

Table of Contents

1	Introduction	1
2	Background and Rationale	4
3	The FD-TLM Method for Josephson Junction Simulation	8
3.1	Modeling Linear Devices	12
3.2	Modeling Nonlinear Devices	14
4	Modeling the Josephson Junction	16
4.1	Characteristics of the Josephson Junction	16
4.2	Implementation of the Josephson Junction in the FD-TLM method .	21
5	Resistively Coupled Josephson Logic Circuits	31
5.1	Introduction	31
5.2	The JAWS circuit	32
5.2.1	FD-TLM implementation	34
5.2.2	Validation of FD-TLM results	38
6	Magnetically Coupled Josephson Logic Circuits	42
6.1	Introduction	42
6.2	DC SQUID Simulation	42

6.2.1	FD-TLM implementation	44
6.2.2	Validation of FD-TLM results	45
6.3	MVTL Simulation	47
6.3.1	FD-TLM implementation	48
6.3.2	Validation of the FD-TLM results	50
7	Conclusion	53
A	FORTTRAN Code for JJ Implementation	56
B	JAWS Simulation Data	65
B.1	FD-TLM Data Set	65
B.2	FastHenry Data Set	69
B.3	MAPLE V Results	70
B.4	C Code	73
C	2 JJ DC SQUID Simulation Data	79
C.1	FD-TLM Data Set	79
C.2	FastHenry Data Set	86
C.3	MAPLE V Results	88
C.4	C Code	96
D	MVTL Simulation Data	102
D.1	FD-TLM Data Set	102
D.2	FastHenry Data Set	109
D.3	MAPLE V Results	111
D.4	C Code	116

List of Figures

3.1	Depiction of divided three-dimensional space	10
3.2	Each cell in three-dimensional space	10
3.3	The E field node	11
3.4	The H field node	11
3.5	Equivalent circuit of the JJ showing current source.	15
4.1	DC current-voltage characteristics of the JJ	17
4.2	Equivalent circuit for the Josephson junction.	18
4.3	FD-TLM simulation for a single Josephson junction.	25
4.4	Depiction of the arrangement of JJs within the SQUID loop.	26
4.5	Total critical current versus flux for the SQUID	28
5.1	The JAWS logic gate.	32
5.2	Cross-section of layers used in fabrication of JJ ICs.	35
5.3	Placement of the E_y node in the tunneling barrier	35
5.4	JAWS layout used for FD-TLM simulation.	36
5.5	Results of simulation of the JAWS logic gate.	37
5.6	MAPLE is used to solve first order derivatives.	39
6.1	Equivalent circuit for the 2 JJ DC SQUID.	43
6.2	Physical layout of the DC SQUID.	44

6.3	Results of simulation of the DC SQUID logic gate.	45
6.4	Equivalent Circuit for the MVTL logic gate.	47
6.5	Physical layout of the MVTL circuit used in FD-TLM simulation. . .	49
6.6	Results of simulation of the MVTL logic gate.	50

Chapter 1

Introduction

The Josephson junction is a superconducting tunneling device that allows fabrication of logic gates with much lower power dissipation and much faster switching speeds than logic gates utilizing silicon or GaAs technology. Because Josephson junctions are capable of operating at much higher frequencies, circuit simulation is significantly more complex. Quasi-static conventional circuit becomes inaccurate at frequencies where the wavelength of the signal becomes comparable to the cross-sectional dimensions of the circuit layout. Thus, a full-wave simulation method must be found that is capable of modeling JJ circuits at high frequencies.

The full-wave finite-difference transmission line matrix (FD-TLM) method [1], completely models the time evolution of electromagnetic field interaction with different media and devices by solving Maxwell's curl equations. In this method, three dimensional space is divided into a set of nodes which are selectively modified to model material properties such as permittivity, permeability, and conductivity. Nonlinear devices are modeled in the method by altering the conductivity and permittivity of the nodes representing the device as a function of voltage and time.

The FD-TLM method, by solving Maxwell's curl equations, naturally simulates the operation of a circuit while simultaneously determining high frequency effects. The JJ is implemented as a nonlinear device in the method with conductivity and

permittivity that change with applied voltage and time. Substrates and interconnects are modeled by specifying the values of permeability, conductivity, and permittivity at the nodes representing them. The FD-TLM method can model JJ logic circuits as well as the substrate layers and insulating layers used to fabricate the logic circuit. Additionally, there is no need to extract parasitic component values since these are automatically simulated while solving Maxwell's equations. The FD-TLM method is discussed in Chapter 3.

Many logic circuits utilizing JJs use a property of JJs that arises when several JJs are placed in a superconducting loop. That is, two or more JJs placed in the same superconducting loop become quantum mechanically coupled with a relationship controlled by the presence of a magnetic flux within the superconducting loop. This configuration is referred to as a Superconducting Quantum Interference Device (SQUID).

The Josephson junction and SQUID are implemented in the FD-TLM method as described in Chapter 4. Chapter 5 discusses the resistively coupled Josephson logic gate which utilizes the characteristics of individual JJs while Chapter 6 discusses the magnetically coupled Josephson logic gate which utilizes magnetic coupling between several JJs placed in a superconducting loop.

The results from the FD-TLM method can be validated by observing the general logic operation obtained from the simulation. In addition, further validation is obtained by performing a conventional circuit simulation. A program *FastHenry* [2] is used to extract inductance values from the physical layout of the JJ logic gate. The inductance values are required to accurately simulate JJ circuits when using a conventional circuit simulation method. In contrast, the FD-TLM method does not require a separate inductance extraction since it solves Maxwell's curl equations rigorously.

Since methods such as SPICE [3] do not currently implement the JJ device, con-

ventional circuit simulation proceeds with nodal analysis of the equivalent circuit for the logic gate to obtain a set of simultaneous differential equations. MAPLE V [4] is used to symbolically solve these differential equations for the standard form where the first-order derivatives are on the left-hand side of the equations. Then, the new set of differential equations are solved numerically using a fifth-order Runge-Kutta [5] method, providing the response of the circuit with time. Validation of the FD-TLM method for each type of logic gate is discussed in Chapters 5 and 6.

Chapter 7 ends with a summary discussion of the results obtained from the simulation of all logic gates along with a statement on the ability of the FD-TLM method to simulate circuits incorporating JJ devices. Possible future work in this area will be discussed as well.

Chapter 2

Background and Rationale

Theoretically, superconducting digital logic gates should be capable of achieving high speeds with low power consumption. However, early superconducting digital circuits dating back to the 1950s utilized cryotrons and were slow by semiconductor standards. Cryotron digital circuits relied on the physical change between a superconducting and normal state to switch between a logic “1” and “0” [6]. Resultant switching times were a few microseconds. With superconducting digital technology unable to compete with semiconductor technology, further research was abandoned.

Research into the use of the Josephson junction (JJ) for superconducting digital logic circuits began in the mid-1960s. The Josephson junction utilizes tunneling of Cooper pairs, superconducting transport particles, across a thin tunneling barrier consisting of a non-superconductive material. Early JJs utilized lead alloy superconductors with SiO_2 as tunneling barriers. The tunneling barrier is designed to allow tunneling of Cooper pairs but also allow tunneling of normal electrons. As is typical for all superconductive materials, the JJ can only support up to a maximum superconducting current density. Once this current density is reached, the device switches to conduction of normal electrons through the thin barrier rather than conduction of superconducting Cooper pairs. In other words, the device switches between a superconducting and normal conducting state. This is done without, for example,

changing the temperature of the device meaning that much higher switching speeds can be obtained than with the cryotron.

Although JJ logic circuits exhibit high speed, low power performance, silicon ICs are still used in most applications today for several reasons. Research into JJs and superconducting ICs declined after a short burst in the 1960s due to the low, liquid Helium, temperatures required for operation, the inability to precisely control parameters of the JJ in fabrication, and the dramatic changes in parameters of the JJ with extended storage and temperature. As a consequence of the impracticality of use of JJs in IC circuits at the time, IBM discontinued research into JJ technology in 1983.

With the advent of Type II superconductors capable of operating at liquid nitrogen temperatures, JJs recently became more practical for digital logic ICs. In addition to operating at much higher temperatures, JJs using superconductive materials such as YBaCuO and Nb are much more stable than their predecessors in that their parameters such as critical current do not change significantly over time. Furthermore, it is easier to reproduce JJs with similar electrical properties on an IC with the newer superconductive materials.

Unfortunately, while several JJs can be fabricated with the same properties, it is still impossible to fabricate ICs with more than a few thousand JJs all having similar properties. Therefore, while small scale integration is feasible, it is still impossible to create superconducting ICs with the level of integration used in silicon technology. Furthermore, even though Josephson junction logic gates consume far less power and have much higher switching speeds than their counterparts in GaAs or silicon technology, the performance of GaAs and silicon technology is rapidly approaching that of JJ technology while remaining more economical.

Despite the stumbling blocks, research is still ongoing in the design of even faster

JJ logic gates. Many JJs being fabricated today have switching times as low as 2.5 ps. Furthermore, several 4-bit microprocessor architectures utilizing JJs have been fabricated and tested. Of particular note, in 1988, a team of researchers developed a 4-bit microprocessor using 2.5 μm Nb technology [7]. The processor consisted of a 64-bit Non-Destructive Read-Out (NDRO) RAM, an ALU, and control circuits using a total of 1841 Josephson junction gates. The microprocessor operated at a maximum clock frequency of 770 MHz.

Research is still ongoing in developing many types of logic gates utilizing the JJ. Research time and cost can be minimized given an ability to simulate JJ logic circuits before fabrication. Accurate circuit simulation reduces the amount of trial-and-error fabrication. In simulating JJs that can switch in only 2.5 ps, propagation delays, dispersion, reflections, and parasitic capacitance and inductance, must all be considered.

Many methods have been used to simulate JJ [8] circuits including a recent method where SPICE is extended to model JJs [9]. Rollins [9] provides a starting point for implementing JJ circuits in other simulation methods. However, in Rollins' approach, SPICE was used to simulate a JJ circuit with nanosecond switching times and was not developed to ensure proper modeling for higher clock frequencies. Additionally, the SPICE method presented by Rollins appears to omit several important parasitics including mutual inductance between the control line and superconducting loop, capacitance between the control line and superconducting loop, and capacitance between the circuit and the superconducting ground plane. However, stray capacitances and inductances can be extremely important as illustrated in [10]. Here it is emphasized that parasitic capacitance between the control line and superconducting loop can create resonances in a SQUID circuit.

In summary, the SPICE method, while simulating the characteristics of the JJ

itself rather well, is inept at modeling JJ logic circuits where the wavelength of the signals become comparable to the cross-sectional dimensions of conductors in the circuit. For instance, with the small voltage signal, approximately 2 mV, used in JJ logic circuits, electromagnetic noise may determine whether the circuit functions correctly. A method, then, must be used that is capable of solving Maxwell's equations to provide the full electromagnetic response of the circuit and its surrounding packaging.

Several methods exist which solve Maxwell's curl equations for electromagnetic fields. Most notably, the finite-difference time-domain (FD-TD) method which solves discretizes three dimensional space into a set of nodes and solves for Maxwell's curl equations in time and space using the "leap-frog" method for integrating the differential equations. The finite-difference transmission line matrix (FD-TLM) method works in a similar manner, however, this method solves for voltages and currents rather than electric and magnetic fields by using an analogy between transmission line equations and Maxwell's curl equations.

Chapter 3

The FD-TLM Method for Josephson Junction Simulation

Several methods exist for simulating the Josephson junction device. SPICE [9], for example, can be used to obtain the behavior of a Josephson junction logic circuit. Conventional circuit analysis methods such as SPICE are excellent for simulation of circuits including high speed circuits given that the parasitics such as inductance and capacitance are extracted from the physical chip layout or are supplied as part of the circuit for simulation. However, extraction of parasitic inductance and capacitance from a physical chip layout can be inaccurate and may only be correct for certain frequencies. Phenomena such as the skin effect, lumped versus distributed capacitance and inductance, dispersion, electromagnetic noise, and resonance within the IC package cannot be readily modeled in a SPICE simulation.

The FD-TD and FD-TLM methods, by solving Maxwell's curl equations, completely model the time-evolution of electromagnetic field interaction with different media and devices. As a result, high speed integrated circuits can be simulated as with the SPICE method while, in addition, simultaneously modeling distributed parasitic capacitance and inductance, dispersion, electromagnetic noise and reflections, and cavity resonance given the physical layout of materials and devices within the circuit.

While the FD-TD method solves Maxwell's curl equations directly using a differential equation integration technique, the FD-TLM method relies on an analogy between Maxwell's curl equations and the equations describing transmission lines. As a result, the FD-TLM method actually solves for voltages and currents that are propagated through space along interconnecting transmission lines instead of solving for magnetic and electric fields directly. Permittivity and permeability of free space become distributed capacitance and inductance, respectively, along the transmission lines.

Within the FD-TLM method [1], space is divided into a set of three dimensional nodes as depicted in Fig. 3.1 and along the faces of each cell, every E (electric) node is surrounded by an H (magnetic) field node in any of four directions and, similarly, every H field node is surrounded by four adjacent E field nodes (Fig 3.2). There are three electric field nodes for each dimension of space E_x , E_y , and E_z , as well as three magnetic field nodes H_x , H_y , and H_z , where each node in the FD-TLM space has a one-to-one correspondence with points discretizing space containing the structure to be modeled. The H-field and E-field nodes are connected through transmission lines having characteristic inductance and capacitance determined by free space permittivity and permeability. Each electric field node connects the two conductor transmission lines in a parallel fashion while the magnetic field nodes connect the transmission lines in series. Therefore, the E-field node is referred to as a shunt node (Fig 3.3) while the H-field nodes referred to as a series node (Fig 3.4).

Within the FD-TLM method, a variable mesh is used to change the relative distance between adjacent nodes as opposed to a uniform mesh where all of the nodes are equidistant in space. This allows fewer cells to be used for many types of circuit simulations, and, therefore shorter simulation time due to fewer number of nodes to

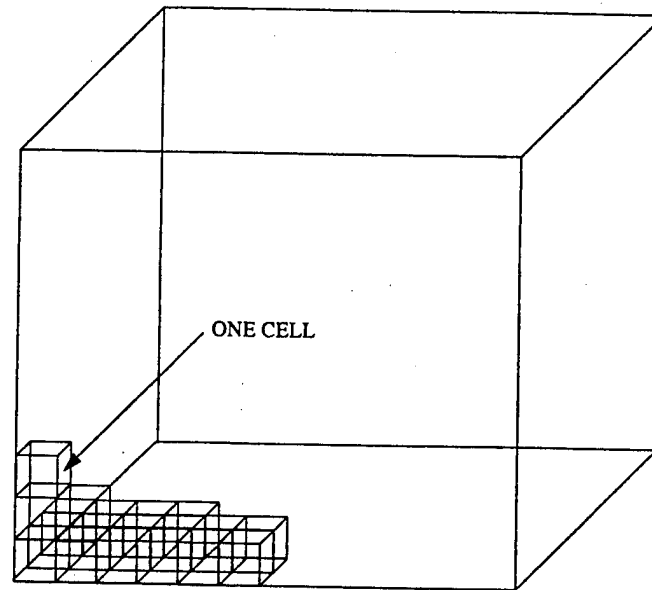


Figure 3.1: Depiction of three-dimensional space divided into cells.

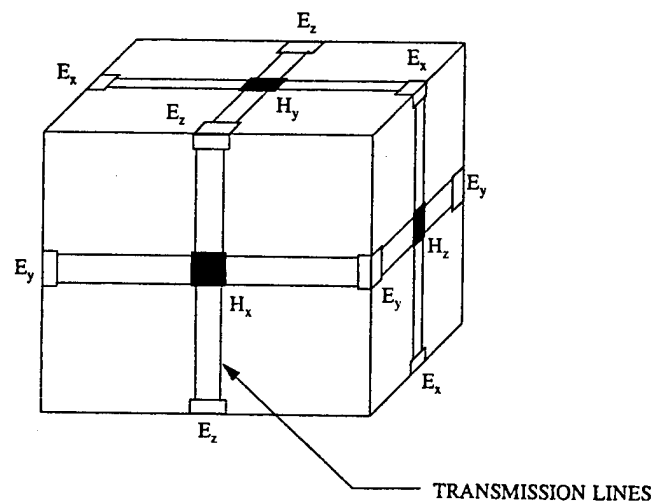


Figure 3.2: Each cell in space contains a set of nodes representing the magnetic and electric field nodes. Note that the nodes are on the surface of the cube and are connected with transmission lines.

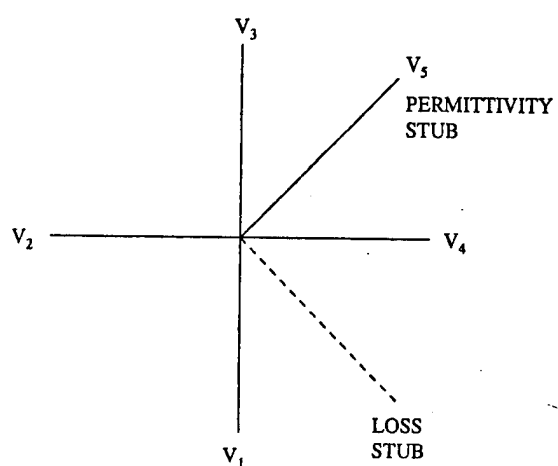


Figure 3.3: Depiction of the E-field shunt node where transmission lines are connected in a parallel fashion. Each line represents two conductors.

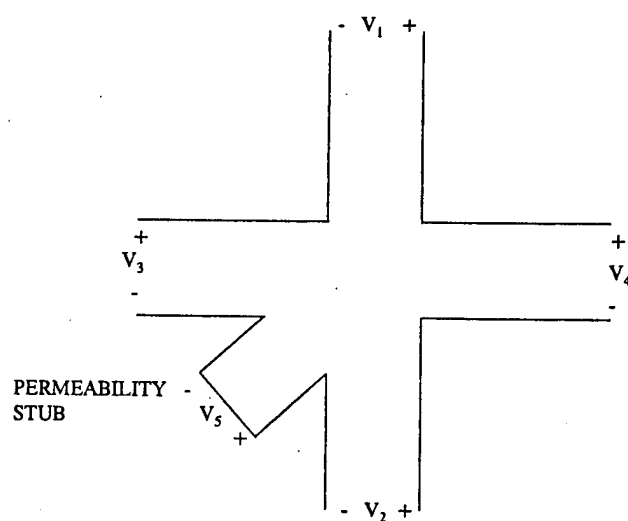


Figure 3.4: Depiction of the H-field series node where transmission lines are connected in a series fashion.

be calculated. To optimize simulation time and accuracy, a larger number of closely spaced cells are used in areas where fields are expected to have a larger spatial gradient, while a fewer number of widely spaced cells are used in the area, for example, between the circuit and the IC package. This is analagous to an ordinary differential equations solver method which uses smaller steps in the integration in places where the function changes most rapidly.

Simulation within the FD-TLM method begins by defining a signal which is applied to an electric field node or array of electric field nodes. This signal propagates along the transmission lines to the neighboring magnetic field nodes, where part of the signal is reflected back to the source E field nodes and part is transmitted along transmission lines connected to other E field nodes. The FD-TLM method alternates calculating E and H field nodes at each time as signals propagating at a certain velocity travel from the E field nodes to the H field nodes and vice versa. The propagation of signal pulses along the transmission lines and the scattering of pulses at the nodes models electromagnetic wave propagation. The voltage calculated across a shunt node corresponds to the electric field at that point in space and the current flowing through a series node corresponds to the magnetic field at that point in space.

3.1 Modeling Linear Devices

Linear devices such as capacitors, inductors, and resistors that maintain fixed values with applied voltage and time are easily modeled in the FD-TLM method [1]. Note the addition of a permittivity stub and loss stub to the E-field node and addition of a permeability stub to the H-field node in Fig. 3.3, and Fig. 3.4. These stubs are used to describe conductivity, permittivity, and permeability at each point in geometric space and, therefore, provide the means for describing layers of materials, resistors, and capacitors.

Resistors are implemented in the FD-TLM method by incorporating conductivity via the loss stubs for the E field nodes in the volume representing the resistor. Conductivity, σ , is calculated from resistance, R , using the relationship $R = \frac{L}{\sigma A}$ where the length of the resistor, L , is determined to be in the direction of current flow and A is the cross-sectional area perpendicular to current flow.

When setting the conductivity of the nodes in space representing a resistor, the region of influence for each node must be considered. That is, at a point between two adjacent nodes, the actual conductivity is an average of the conductivity at each node. As a result, while each node in the FD-TLM method can be thought of as representing a cell with dimensions specified by the spacing between adjacent nodes in each direction (see Fig. 3.1). the conductivity within the cell is not equal to the conductivity of the E_x , E_y , or E_z node, but, rather, is an average of the conductivities in adjacent nodes or of the nodes on the surface of the cell. The actual value of conductivity needed to implement a resistor, where (u, v, w) is the dimension of the (x, y, z) cell, is determined from

$$R_x = \frac{4u}{\sigma_x vw + \sigma_{x,j-1} v_{j-1} w + \sigma_{x,k-1} v w_{k-1} + \sigma_{x,j-1,k-1} v_{j-1} w_{k-1}}. \quad (3.1)$$

The subscripts i, j, k refer to the location of each cell (see Fig 3.1) where the H field nodes on the bottom, left side, and front of the cell (Fig 3.2) and the E field nodes on the bottom-left, bottom-front, and left-front of the cell (Fig 3.2) belong to the (i,j,k) cell and all other nodes belong to adjacent cells. The previous equation establishes a resistance in the x direction; however, conductivity can be specified differently for the x, y, or z direction at each cell allowing modeling of anisotropic materials.

Capacitors are implemented by altering the permittivity at a set of nodes. The determination of permittivity for implementation of the capacitor follows that of the resistor. The equation defining the capacitance value for an x-directed E field node is

$$C_x = \frac{\epsilon v w + \epsilon_{x,j-1} v_{j-1} w + \epsilon_{x,k-1} v w_{k-1} + \epsilon_{x,j-1,k-1} v_{j-1} w_{k-1}}{4u}. \quad (3.2)$$

Substrates and layers of material are common in ICs, and, therefore, the FD-TLM method must be capable of simulating these layers in order to properly model ICs. These layers are specified by setting the permittivity values of the nodes in the FD-TLM method corresponding to the materials.

3.2 Modeling Nonlinear Devices

Within a non-linear device, the current and voltage do not have a linear relationship meaning that the conductivity of the device is a function of the applied voltage. Furthermore, capacitance for the device may change with applied voltage as occurs for the diode or any P-N junction capacitance. Due to the relationship between voltage and current, a non-linear device cannot be implemented by specifying conductivity or permittivity in an input data set for the FD-TLM method. Instead, the FD-TLM method must be given a current-voltage (I-V) equation for the node representing the non-linear device. The FD-TLM method then uses the I-V equation to update the conductivity of the node representing the non-linear device as a function of the voltage or electric field at the node. Note that non-linear devices are implemented at E-field nodes.

Many non-linear devices, such as the Josephson junction, contain storage elements which may lead to a large negative conductivity. Within the FD-TLM method a voltage is calculated at each time step and, from this voltage, the current through the non-linear device and its conductance is calculated and implemented at the node for the next iteration. However, an analysis of the circuit equivalent for a non-linear device may reveal current sources which are capable of driving current in an active convention rather than passive convention with respect to voltage leading to negative

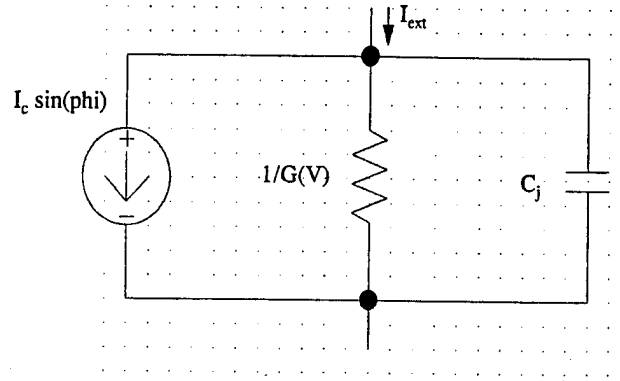


Figure 3.5: Equivalent circuit of the JJ showing current source.

conductivity at the node. Within the FD-TLM method, negative conductivity creates a large instability and resultant oscillations. As a result, the storage elements of such a device cannot be simulated as a changing conductivity at the electric field node. The I-V equation is modified, from the circuit equivalent, to contain all but the storage elements in question. The storage elements, specifically current sources, are modeled by updating the electric field at the electric field node representing the nonlinear device to reflect the current. Figure 3.5, shows the current source which is modeled by updating the value of the E field node at each iteration while the resistance $\frac{1}{G(V)}$ is modeled as a conductivity that changes with time and applied voltage, ie the value of the loss stub is changed at the E field node.

Non-linear capacitance as well as conductance can be implemented in the FD-TLM method by changing the permittivity at the node representing the device as a function of the present value of the electric field node. In the case of the Josephson junction, the capacitance is linear and is modeled as a constant permittivity.

Chapter 4

Modeling the Josephson Junction

4.1 Characteristics of the Josephson Junction

Before beginning with implementation of the JJ and the analysis of JJ logic gates, it is important to understand the characteristics of the device. Figure 4.1 shows the dc current-voltage characteristics of the Josephson junction.

There are two parts to the dc curve which combine to describe the superconducting tunneling current and single particle tunneling current. The superconducting tunneling current represents current in the zero voltage state (ZVS) of the device where current flows through the device with no associated voltage drop. Note that the current in the ZVS cannot exceed the critical current, I_c , in magnitude. If the current through the junction should exceed the critical current of the device, the device switches to another state commonly referred to as the high voltage state (HVS) shown as a jump from point 1 to point 2 in Fig. 4.1. A voltage develops across the junction in the HVS and follows the I-V characteristics of the single-particle tunneling curve. Typically, in the HVS, the voltage across the junction will equal the gap voltage V_{gap} , a JJ process parameters used to describe the JJ current-voltage relationship, with currents just above the critical current of the device. When current is decreased to a value below the critical current, instead of returning to the ZVS,

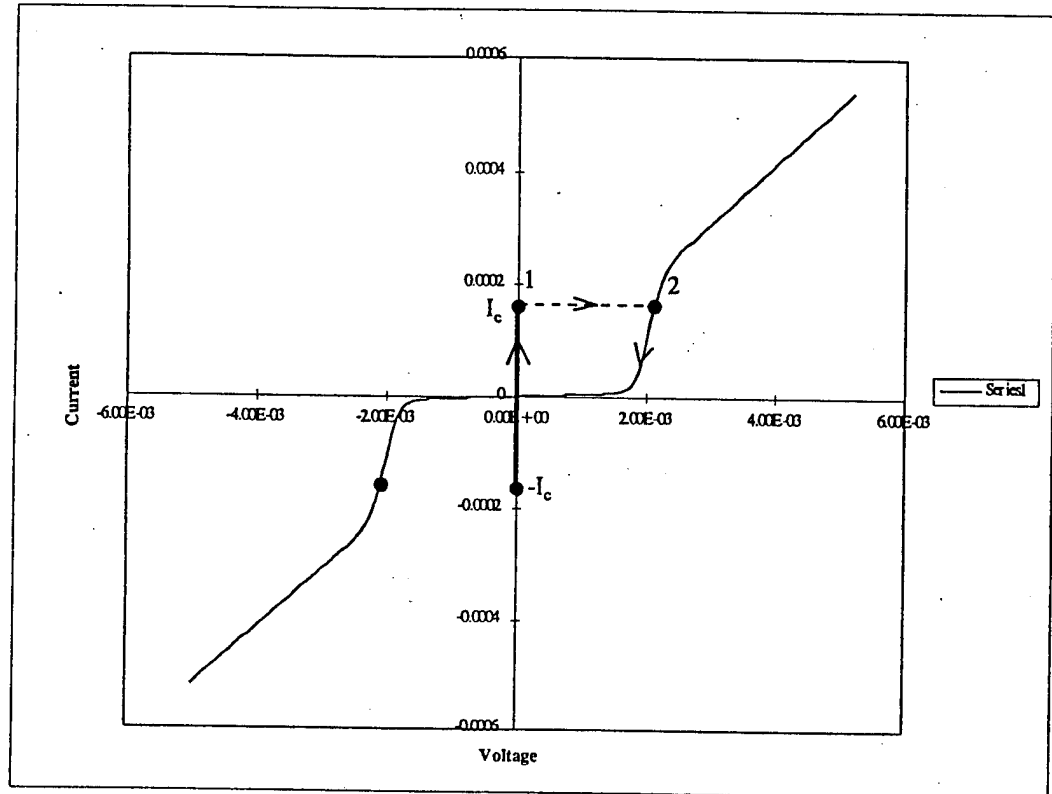


Figure 4.1: DC current-voltage characteristics of the Josephson junction. The vertical line at the $V=0$ line represents the ZVS and Cooper pair tunneling while the HVS curve or nonzero voltage curve represents single-particle tunneling.

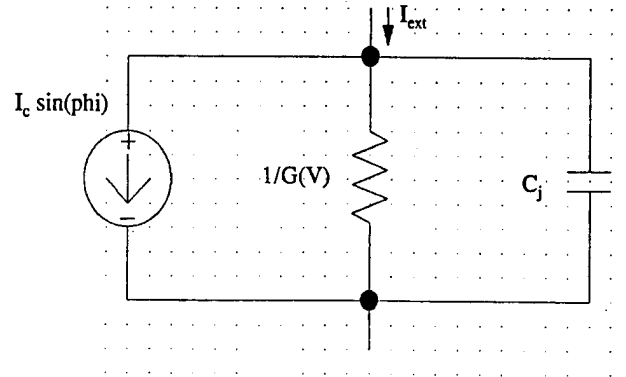


Figure 4.2: Equivalent circuit for the Josephson junction.

the device remains in the HVS and the I-V characteristics continue to follow the single-particle tunneling curve. The device does not return to the ZVS until current through the device is lowered to zero. As a result, the JJ has a hysteresis.

The dc I-V curve for the JJ is reconciled by the two fluid model of superconductivity [11]. The two fluid model provides the ability for both superconducting Cooper pairs and normal conducting electrons to contribute to current flow in the superconductor at any time. That is, normal conduction and superconduction can occur in tandem within the superconductor. This model explains many phenomena within the superconductor including the existence of resistance in the superconductor at very high frequencies, as well as how the JJ is capable of switching between tunneling of Cooper pairs and electrons to transition between a superconductive state and a resistive state.

The circuit equivalent for the Josephson junction is shown in Figure 4.2. Insight into the ac as well as dc characteristics of the JJ is gained by examining the equivalent circuit. This consists of three components, a current source which represents the tunneling of Cooper pairs, a resistance $\frac{1}{G(V)}$ which represents single particle tunneling, and a capacitor C_j which is the capacitance created by the tunneling barrier sandwiched between the superconductive electrodes. As seen from the equivalent

circuit, superconducting current with its zero associated voltage drop can only be represented by the current source. This is defined as

$$I = I_c \sin(\phi). \quad (4.1)$$

The JJ critical current is I_c and the phase ϕ , the quantum mechanical phase difference across the junction, is related to voltage across the junction by

$$\frac{d\phi}{dt} = P_o V. \quad (4.2)$$

The superconducting current can be rewritten as

$$I = I_c \sin(P_o \int V dt) \quad (4.3)$$

One interesting ac characteristic of the JJ can be seen immediately from (4.3). With a constant applied voltage, the current through the current source will oscillate at a frequency ω , where

$$\omega = \frac{d\phi}{dt} = P_o V. \quad (4.4)$$

The JJ current-voltage curve can be derived from the equivalent circuit. Observing Fig. 4.2, we start initially by assuming that the current through and the voltage across the device are zero. As an externally applied current is increased through the device, the current first flows through the capacitor which appears as a short. Then, as a voltage is developed across the capacitor, current begins to flow through the resistance $\frac{1}{G(V)}$. The voltage, generated by current flow through the capacitor and resistance, changes the current through the current source by (4.3). The voltage varies as the current begins to flow through the current source rather than the capacitor and resistor, and the entire process continues until all of the current is absorbed by the current source and there is no voltage drop across the junction. Thus, the JJ has remained in the ZVS. Once the system is stabilized, a change in externally applied current will repeat the entire process for the new current until, once again,

the current source absorbs all of the current. Thus, a change in externally applied current generates a temporary spike in voltage until the system stabilizes.

If the externally applied current through the junction is greater than the critical current, I_c , of the device, a voltage is generated across the capacitor and resistor as before; however, the current source cannot absorb all the externally applied current I_{ext} in that $I = I_c \sin(\phi)$ can never be equal to I_{ext} . Thus, some of the externally applied current must flow through the resistor, causing a voltage drop across the JJ. The JJ is now in the HVS and the current source oscillates at the frequency given by (4.4). Once in the HVS, the JJ merely behaves as a resistor since essentially all of the externally applied current flows through the resistor. The oscillating current from the current source is generally shorted by the capacitor in parallel; however, some of this current shows up as a small ripple in the output voltage and current of the device when in the HVS.

Earlier, it was noted that a hysteresis exists in the dc characteristics of the JJ. That is, the JJ, once in the HVS, is not capable of returning to the ZVS until the current through the device is returned to zero. This behavior can be explained considering the ac characteristics of the JJ, particularly that oscillations are created in the current source for a constantly applied voltage. When the JJ enters the HVS, a voltage of approximately 2 mV is developed. This creates a high frequency oscillation in the current source, as mentioned before, representing the energetic instability in the JJ for currents higher than the critical current of the device. As the externally applied current decreases below the critical current, a voltage of approximately 2 mV is still observed across the JJ which does not allow the current source to match the externally applied current even though the externally applied current may be less than the critical current. The only way to force the JJ back into the ZVS is to completely cut off the oscillations of the current source by reducing the externally

applied current to zero and subsequently the voltage across the junction to zero.

4.2 Implementation of the Josephson Junction in the FD-TLM method

The equivalent circuit of the JJ is used to determine the conductance as a function of voltage to implementing the JJ in the FD-TLM method. The capacitance for the JJ, C_j is not used in the conductivity calculation, but is implemented directly as a capacitance within the FD-TLM method following the method outlined in Chapter 3. The following equations are needed to determine the conductivity of the JJ as a function of voltage [9]

$$I = I_o \sin(\phi) + G(V) + C_j \frac{dV}{dt} \quad (4.5)$$

$$P_o V = \frac{d\phi}{dt} \quad (4.6)$$

$$G(V) = G_1 V + (I_1 + G_2 |V|) \left\{ \frac{1}{1 + \exp \frac{V_S - V}{V_t}} - \frac{1}{1 + \exp \frac{V_S + V}{V_t}} \right\} \quad (4.7)$$

where P_o is the plasma dampening frequency of the JJ, ϕ is the quantum mechanical phase difference for the Cooper pair particle across the junction and changes with time as a function of voltage according to (4.2), I_o is the critical current of the JJ, and $G(V)$ describes the single-particle tunneling curve. A discussion of the parameters for $G(V)$ is obtained from [13, 9] and are determined from the measured properties of the JJ after fabrication. With the current-voltage relationships of the JJ determined, the device can be implemented at an E-field node or array of E-field nodes by altering the conductivity at the node or nodes as a function of the value of the E-field as discussed in Chapter 3. However, as was discovered during the research stage, there are some problems inherent in modeling the JJ as a conductance using its equivalent circuit.

An analysis of the value of conductivity for the JJ with respect to time reveals a problem with simulating the JJ as just a conductivity which changes with time. Initially, the FD-TLM method begins by setting the conductivity of the node representing the JJ to zero. As signals develop within the FD-TLM method, a voltage will eventually be established across the JJ node due to the capacitance at the node and conductivity can begin to change accordingly. The problem arises when the JJ is in the ZVS since current must flow through the device with no associated voltage drop. This, indeed, occurs in the FD-TLM method as the current source within the circuit equivalent begins to absorb all of the input current. However, the conductivity of the node approaches infinity at this point. This immediately creates a problem in any numerical method, but, even if this problem is corrected by imposing a maximum value for conductivity and accepting the error, another problem still arises. With an infinite conductivity, any new currents through the JJ will have no effect on it since there is no longer any way to generate a voltage drop across the node, and, as a result, the JJ behaves merely as a shorted node. Finally, it is possible to have a situation where the current source in the circuit equivalent is directing current in an active rather than passive convention with respect to voltage. In other words, there is energy storage in the device and it is possible for the JJ to behave as a battery leading to a negative conductivity at the node. This creates instability within the FD-TLM method. Obviously, a different method must be used for implementing the JJ.

Instead of simulating the entire device as a node whose conductivity changes with time, only the resistance $\frac{1}{G(V)}$ is modeled as a conductivity at the E-field node. Capacitance is implemented as a linear capacitance using methods discussed in Chapter 3.

The current source, however, is incorporated in the FD-TLM method following a

procedure analogous to the implementation of a resonant tunneling diode [12]. That is, modify the value of the electric field at the E-field node representing the JJ by adding the time-averaged current source current expressed as

$$I_{save} = [I_S(V^{n+1}) + I_S(V^n)]/2, \quad (4.8)$$

where V^n represents voltage at the present time step, and V^{n+1} is the voltage at the next time step $(n+1)\tau$ where τ is the FD-TLM time step. Current $I_S(V^n)$ is calculated as $I_O \sin(\phi^n)$ where ϕ^n is the phase at time $n\tau$, the present time step, and is obtained by integrating (4.2) as the sum of the product $P_o V^n \tau$ at each time step. At the start of the simulation, the phase, ϕ , is initially zero. The new superconducting current, current through the current source, is found as

$$I_S(V^{n+1}) = I_S(V^n) + \frac{dI_S(V = V^n)}{dV} (V^{n+1} - V^n). \quad (4.9)$$

Using a truncated Taylor series, the derivative in the above expression is

$$\frac{dI_S(V = V^n)}{dV} = I_O \cos(\phi^n) P_o V^n \frac{\tau}{V^{n+1} - V^n}. \quad (4.10)$$

Incorporating the time-average JJ superconducting current yields the new FD-TLM equation for updating the electric field node voltage

$$\begin{aligned} V_z^{n+1} = & \left[1 - \frac{2Y_{Lzn}}{K} - \frac{Z_O}{K} I_O \cos(\phi^n) P_o \tau \right] V_z^n \\ & - \frac{2Z_O}{K} [I_{x,j-1}^{n+(1/2)} - I_x^{n+(1/2)} \\ & + I_y^{n+(1/2)} - I_{y,i-1}^{n+(1/2)} \\ & + I_O \sin(\phi^n)] \end{aligned} \quad (4.11)$$

where V_z^{n+1} and V_z^n are the shunt node voltages and the subscripted I are the currents flowing in neighboring series (magnetic field) nodes [12]. This equation is for an electric field node for z-directed electric fields. Analogous equations can be derived for electric field nodes in the x and y directions.

Conductivity for the node is calculated as $G(V)$ which will never be infinite since this represents normal current flow through the resistance of the JJ. The current source is modeled as a current source within the FD-TLM method rather than modeling it as part of the conductivity of the electric field node representing the JJ. Therefore, once the system is stable in the ZVS, all of the current through the JJ will be represented by the current source while maintaining a reasonable conductivity of the node as being $G(0)$ which is just the R_{gap} resistance, where R_{gap} is the equivalent resistance of the JJ in the HVS. For any additional applied current, the FD-TLM method responds by creating voltages across the capacitance and $G(V)$ to readjust the current source for the newly applied current. To summarize, this JJ model implementation never creates a short at the E field node and thus never becomes trapped in the ZVS, and lacks the instability of having negative conductivity, solving all of the problems associated with the original flawed modeling approach.

Figure 4.3 shows the typical simulation of a single JJ device with the FD-TLM method. In the simulation, a 5 mV pulse is in series with a 27.0 ohm resistor and the JJ, providing current greater than the critical current of the JJ. The voltage level and current through the circuit rises until the JJ enters the HVS and an output voltage is appears across the junction. Furthermore, the externally applied current decreases once the JJ is in the HVS showing that the JJ has switched from a superconducting state to a resistive state. The externally applied current is created by a voltage source in series with a resistor. Thus, when there is a non-zero voltage across the JJ, the circuit current decreases according to Kirchhoff's voltage law. The characteristic ripple created by the oscillating current source in the HVS can also be observed in both the voltage across the JJ and in the current through the JJ. Next, the voltage source is cut off in the circuit reducing the current to zero in the circuit while the JJ requires time to leave the HVS and settle back into the ZVS. Comparison to references

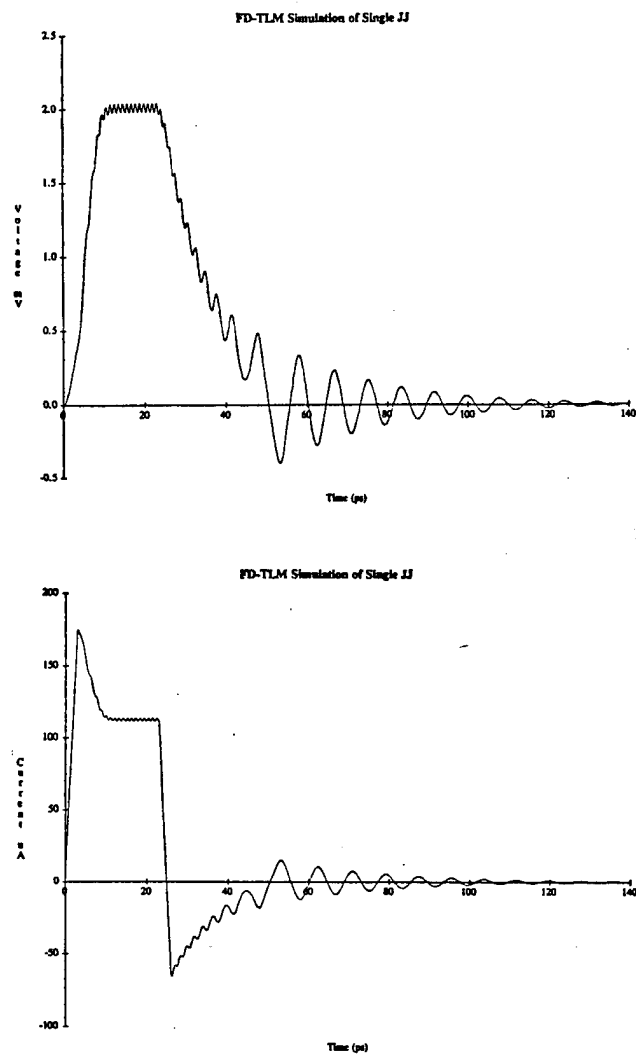


Figure 4.3: FD-TLM simulation for a single Josephson junction.

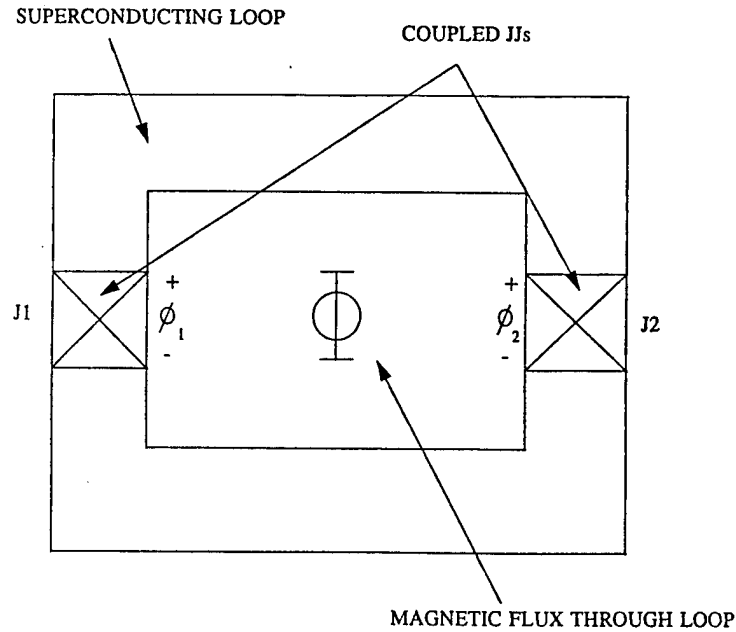


Figure 4.4: Depiction of the arrangement of JJs within the SQUID loop.

[13, 9], show that this is, indeed, the correct general behavior for the JJ. The single JJ was also modeled using conventional circuit simulation performed by solving the differential equations for the JJ using a fifth-order Runge-Kutta method (use of this method is discussed in the next chapter). Fig. 4.3 reveals good agreement between FD-TLM and conventional simulation validating the FD-TLM JJ modeling approach.

results of conventional circuit simulation

With the implementation of the JJ devices discussed so far, a wide variety of JJ logic circuits can be simulated with the FD-TLM method. However, when JJs are placed within a superconducting loop as depicted in Fig. 4.4, the two JJs become coupled as a result of the requirement that the flux through a superconducting loop is quantized. This configuration is referred to as a Superconducting Quantum Interference Device (SQUID). Within the SQUID loop, the JJs are coupled via the vector magnetic potential existing within the superconducting material forming the loop connecting the two JJs, or equivalently, via the magnetic flux passing through the loop. This flux forces a fixed phase change difference between the JJs to quantize

the flux through the loop. Therefore, instead of behaving independently, the phase of one JJ becomes a function of the phase across the other JJ. Since the phase across the junction determines the current through the junction as given by (4.1), the current flowing through one JJ becomes a function of the current traveling through the other JJ and is also a function of the magnetic flux passing through the SQUID loop.

Quantum mechanics must be used to determine the relationship between the JJ currents and the applied external magnetic flux. Consider a Cooper pair wave function that circulates through the SQUID loop and then integrate the phase of this wave function around the loop as described in [13]. This yields the following equation where a discontinuity of the phase occurs at the junction interface yielding,

$$\oint \nabla \theta \cdot dl = 2n\pi = \theta_1 + \theta_2 \quad (4.12)$$

where θ_1 is the phase across J_1 and θ_2 is the phase across J_2 , and the integration of the phase around the loop must be an integer multiple of 2π . Through the use of the gauge-invariant phase we obtain

$$\theta_2 = \theta_1 + \frac{2e}{\hbar} \oint A \cdot dl - 2n\pi, \quad (4.13)$$

which gives a relationship between phase and the magnetic potential vector. Use of Stokes' theorem relating the magnetic vector potential to flux gives the final equation for expressing the phase relationship between J_1 and J_2 for an externally applied flux

$$\theta_2 = \theta_1 - \frac{2\pi\Phi_e}{\Phi_o}, \quad (4.14)$$

where Φ_e is the externally applied flux through the loop and Φ_o is the flux quantum and is equal to 2.068×10^{-15} Wb/m². The total current through the SQUID is obtained from the following expression

$$I_T = I_{C1} \sin(\theta_1) + I_{C2} \sin\left(\theta_1 - \frac{2\pi\Phi_e}{\Phi_o}\right), \quad (4.15)$$

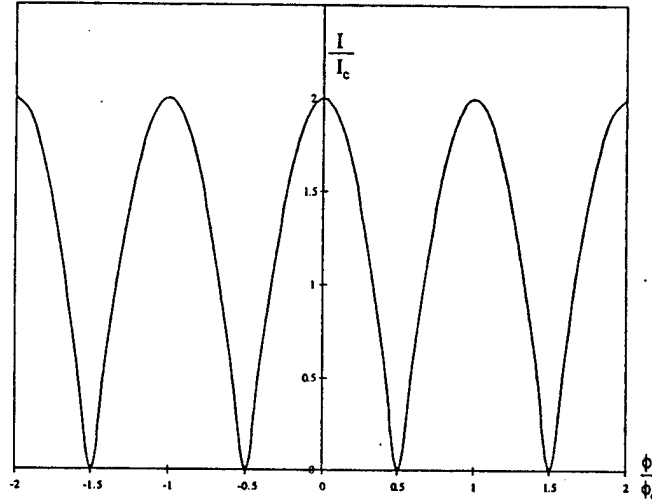


Figure 4.5: Total critical current versus applied flux for the symmetric SQUID.

which is used to determine the total critical current of the SQUID as a function of the applied flux by finding the phase which maximizes the total current at each value of flux. For the case of the SQUID where both JJs are identical and the SQUID loop is symmetric, a simple expression can be obtained for the total critical current

$$I_{TC}(\Phi_e) = 2I_{c1} \left| \cos \frac{\pi \Phi_e}{\Phi_0} \right|. \quad (4.16)$$

A plot of the total critical current versus applied flux is given in Fig. 4.5, in which the interference pattern formed classifies the SQUID as an interference device. Note that the critical current versus applied flux oscillates with increased flux rather than changing linearly. An applied flux equal to one-half of the flux quantum yields a total critical current of zero, and a flux equal to an integer multiple of the flux quantum yields the maximum critical current. Physically, this occurs due to the adjustment of JJ currents to keep an integer multiple of the flux quantum flowing through the loop.

An analytical expression for total critical current versus externally applied flux

was obtained for the case of the symmetric loop. A symmetric loop is one where the Josephson junctions have the same properties and are placed symmetrically within the loop. However, in the case where the loop is asymmetric, it is difficult to derive an analytical expression for total critical current. Instead, a numerical technique must be used which directly solves for the maximum allowable current through the SQUID at each value of applied magnetic flux.

It has been assumed that currents through the loop do not contribute to the magnetic flux through the loop when, in fact, they do. Inclusion of the contribution to magnetic flux in the loop from currents in the loop leads to a new expression for the JJ phases versus applied flux

$$\theta_2 = \theta_1 - \frac{2\pi(\Phi_e + L_2 I_2 - L_1 I_1)}{\Phi_o}, \quad (4.17)$$

where L_1 is the self-inductance for the side of the SQUID loop containing J_1 , L_2 is the self-inductance for the side of the loop containing J_2 , I_1 is the current through L_1 , and I_2 is the current through L_2 [13].

To make the expression for total critical current of the SQUID more complete, the effect of finite junction size can be included. Previously, we have assumed for purposes other than the calculation of critical current density and capacitance, that the junction is a point junction. However, with finite area, it is possible for magnetic flux to exist in the JJ tunneling barrier, altering the critical current of the JJ via the expression

$$I_C(\Phi) = I_C(0) \left| \frac{\sin(\pi\Phi/\Phi_o)}{(\pi\Phi/\Phi_o)} \right|, \quad (4.18)$$

where Φ is the flux contained within the Josephson tunneling area.

Considering these nonidealities, the expression for determining the total critical current for the SQUID loop as a function of externally applied magnetic flux can become unwieldy, requiring a numerical method for solution. This is where the FD-TLM method becomes advantageous.

To implement the SQUID in the FD-TLM method, a new model is created which will couple two JJs using the methods just described. That is, one JJ within the SQUID loop is allowed to vary freely as if acting alone according to the relationships (4.5,4.6,4.7). However, the second JJ in the loop specified with SQUID parameters given to the FD-TLM method adjusts its phase based upon a calculation of the flux through the surface area inside the loop and the phase of the JJ to which it is coupled. Here, instead of determining a function of total critical current versus applied flux and then treating the SQUID as a single JJ as is done in many methods [9], a coupling relation between the JJs within the loop is directly implemented. Since the value for externally applied flux is calculated by the summation of H field nodes, the self-induced flux described earlier is included since currents through the loop in the FD-TLM method will automatically create magnetic fields as a result of the solution of Maxwell's equations.

Chapter 5

Resistively Coupled Josephson Logic Circuits

5.1 Introduction

In the previous chapter, all of the concepts needed to implement a single JJ or a SQUID were covered along with a method for implementing the devices within the FD-TLM method. In this and the next chapter, emphasis is placed on logic circuits utilizing the JJs and validation of the simulation results from the FD-TLM method. The FD-TLM method as discussed in Chapter 3 solves Maxwell's equations for electric and magnetic fields points in discretized three-dimensional space at each time step within the numerical method. Within the discretized three-dimensional space, properties such as conductivity, permittivity, and permeability are specified for each point. As a result, to simulate a circuit, the FD-TLM method requires the physical properties and dimensions of the circuit as it would be fabricated. A CAD system such as MAGIC [4] could be altered to create a data set necessary for the FD-TLM method allowing a chip design to be analyzed quickly without component parasitic extraction.

One technique for simulating JJ logic circuits is to perform a SPICE [3] analysis with component values extracted from the physical layout of the circuit. Since a

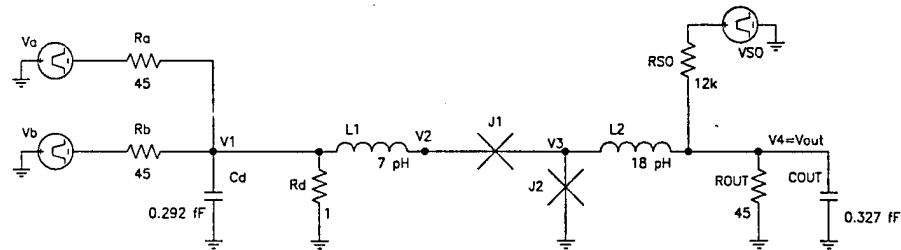


Figure 5.1: The JAWS logic gate.

version of SPICE modified to model JJs was not readily available, a conventional circuit analysis based on Kirchhoff's current law is used instead. It will be found that the FD-TLM method not only obtains good results, but often predicts the existence of additional parasitics or other phenomena omitted in conventional circuit analysis.

5.2 The JAWS circuit

The Josephson-Atto Weber Switch (JAWS) [14] will be the first JJ logic circuit to be analyzed with the FD-TLM method. This circuit is commonly referred to as resistively coupled Josephson logic (RCJL) in that the circuit switches output states from "low" to "high" by increasing the amount of current injected into the JJ devices beyond their critical current. A better understanding is obtained by analyzing the circuit for the JAWS logic gate (Fig. 5.1). Initially, both JJs within the circuit are in the ZVS and appear as "shorts". A steady-state biasing current is established by V_{so} and R_{so} in the circuit which flows through J_2 to ground. Voltage inputs V_a and V_b are applied at the input resistances R_a and R_b , respectively. Voltage applied

to the inputs creates additional current through J_2 . If the sum of the input currents and bias current exceeds the critical current of J_2 , J_2 will proceed to the HVS where it behaves as a resistance rather than a short. At this point, the 1Ω resistor, R_d , will have a much smaller resistance than the equivalent resistance of J_2 and the biasing current will flow through J_1 and then to ground through R_d while the input currents flow through R_d . Note that although J_2 is in the HVS at this point, there is still no output current flowing through R_{out} . This leads to the purpose of J_1 . J_1 has a critical current designed so that the sum of the input currents flowing through J_1 will not force J_1 into the HVS, while, in contrast, the biasing current flowing through J_1 will force J_1 into the HVS. Therefore, with the biasing current flowing through J_1 after J_2 has reached the HVS, J_1 proceeds to the HVS, forcing the input current to continue flowing through R_d while the biasing current now flows through R_{out} . As a result, the JJ logic circuit or JAWS circuit has gated "high". To return to a logic "low", the bias current and input currents must all be returned to zero due to the hysteresis of the JJ.

Josephson junction logic circuits operate on the principle of switching current among different paths. The JAWS gate is considered a resistively coupled logic gate because it relies on forcing a current through the JJ greater than its critical current to switch logic levels. Later, a discussion of magnetically coupled logic (MCJL) gates will clarify the distinction between RCJL and MCJL. Nevertheless, in this circuit, J_2 performs all the work in terms of switching the logic gate while J_1 isolates the input from the output, forcing the input current through R_d and the biasing current through the output resistor.

The JAWS logic gate can operate as either an AND gate or an OR gate depending on the value of the biasing current established through J_2 . This is performed by establishing the bias current using the relationship $I_a + I_b + I_{bias} > I_c$, where I_c is

the critical current of J_2 , and I_a and I_b are the input currents. The gate behaves as an OR gate when $I_a + I_{bias} > I_c$ or $I_b + I_{bias} > I_c$ and behaves as an AND gate only when $I_a + I_b + I_{bias} > I_c$ but with the constraints $I_b + I_{bias} < I_c$ and $I_a + I_{bias} < I_c$.

5.2.1 FD-TLM implementation

The *fdtgraph* [16] program was developed to create data sets for simulation of the various JJ logic circuits in the FD-TLM method. *Fdtgraph* is a mouse-driven graphical interface allowing the user to graphically layout the circuit. *Fdtgraph* then automatically creates the ASCII text data set required for the FD-TLM simulation of the circuit layout.

The JAWS circuit is simulated within a $50 \times 50 \times 50 \mu\text{m}^3$ (x, y, z) box filled with air dielectric with a grid spacing (spacing between points in space) of $1 \mu\text{m}$. The walls of the box are modeled using perfect conductors as boundary conditions, and the bottom of the box is used as a superconducting ground plane.

Fig. 5.2 shows the typical fabrication steps for JJ integrated circuits. This structure is simulated within the FD-TLM method; however, since the silicon substrate is used as a base for construction and electrical properties are the primary concern within circuit simulation, the silicon substrate is excluded from the layout within the FD-TLM method. Thus, the bottom surface of the box containing the circuit is used as the superconducting ground plane and a $2 \mu\text{m}$ thick layer of SiO_2 is used as the insulator between the ground plane and base electrodes or first layer of metal for the JJs. The tunneling barrier is implemented as a y-directed, the E_y field node, which has current-voltage characteristics representing that of the single JJ, centered in the area representing the JJ tunneling material as shown in Fig. 5.3.

Superconducting wiring is implemented as infinitely thin, perfectly-conducting segments of metal within the FD-TLM method. Interconnects are made intentionally

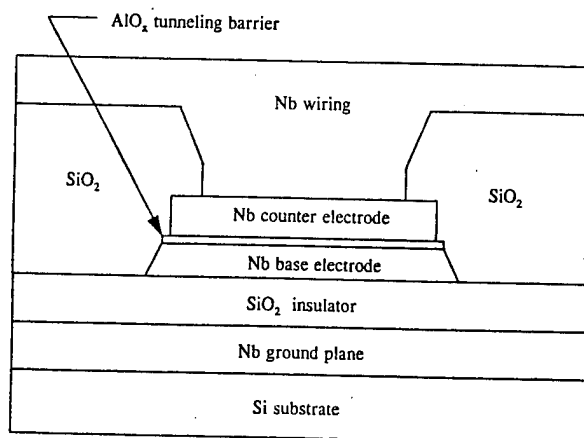


Figure 5.2: Cross-section of layers used in fabrication of JJ ICs.

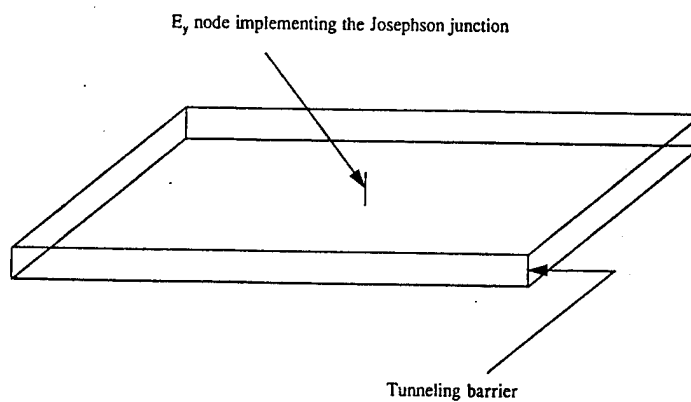


Figure 5.3: Depiction of the actual placement of the E_y node in the tunneling barrier used to simulate the JJ.

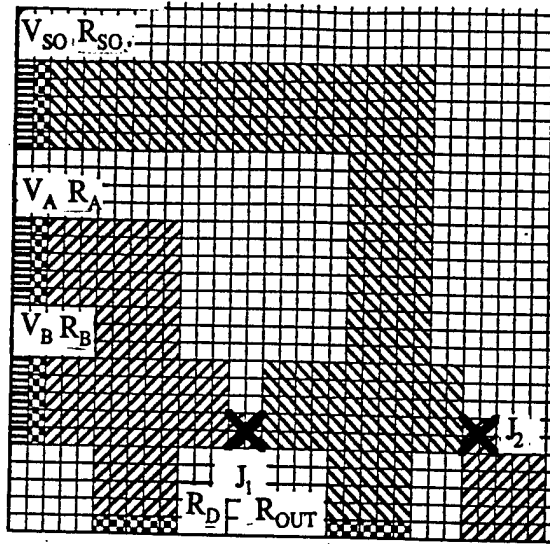


Figure 5.4: JAWS layout used for FD-TLM simulation.

short to reduce reflection and electromagnetic noise enabling comparison with conventional circuit analysis. The FD-TLM layout is shown in Fig. 5.4. The parameters are implemented following [12] $I_c = 0.1$ mA, $G_1 = 4.0$ mS, $I_1 = 0$ A, $G_2 = 0.1$ S, $V_s = 2.0$ mV, $V_t = 0.1$ mV, $P_o = 3.039 \times 10^{15}$ Wb $^{-1}$, and $C_j = 0.5$ pF for the JJ. Three voltage sources are implemented as shown in Fig. 5.1.

The entire simulation is performed for 350 ps with a 1.7 ps time step. The results of the FD-TLM simulation are shown in Fig. 5.5.

The biasing current was established to allow the JAWS logic gate to behave as an AND gate. In Fig. 5.5, the biasing current is established by V_{so} and, as soon as the system is stable, an input voltage of 2 mV is applied to input A. At this point, the output voltage remains at zero as J_2 absorbs all of the input current without triggering to the HVS. At a later time, while leaving the input at A “high” a 2 mV voltage is also applied to input B. At this point, with some delay, J_2 is triggered into the HVS and the gate goes “high”. A signal of approximately 1.7 mV is observed at the output which can be used as the input for a subsequent gate. From the results

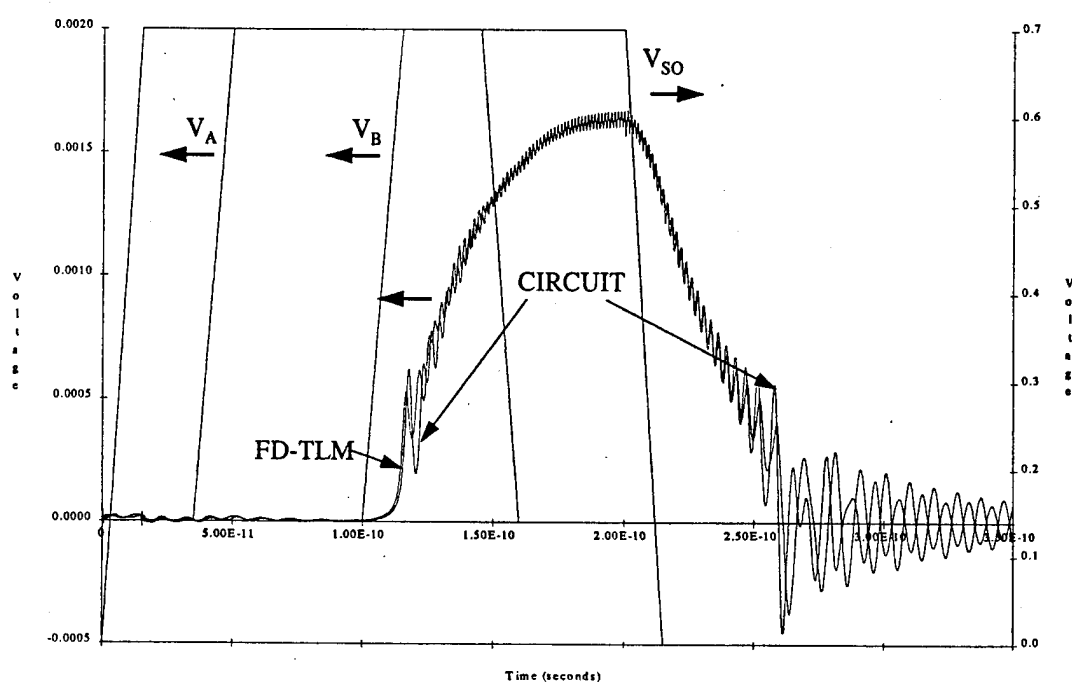


Figure 5.5: Results of simulation of the JAWS logic gate.

of simulation, it is seen that the FD-TLM simulation method provided the correct general behavior of the circuit.

5.2.2 Validation of FD-TLM results

Conventional circuit analysis is used to validate the FD-TLM results and, for the Josephson junction circuit, involves a three step process noting that SPICE version 3f.4 cannot model a JJ. Nodal analysis is performed on the circuit followed by a run through MAPLE to solve for a set of first order differential equations which are, then, solved using an numerical ordinary differential equation integration method.

First, nodal analysis is performed on the circuit to obtain a set of differential equations governing operation of the circuit. The following are the nodal equations for the JAWS circuit.

$$\begin{aligned}
 \frac{V_1 - V_A}{R_{IN}} + \frac{V_1 - V_E}{R_{IN}} + C_D \frac{dV_1}{dt} + \frac{V_1}{R_D} + I_1 &= 0 \\
 -I_1 + C_j \frac{d(V_2 - V_3)}{dt} + G_1(V_2 - V_3) + I_{C1} \sin(\phi_1) &= 0 \\
 \frac{V_3 - V_{SQ}}{R_{SQ}} + C_j \frac{dV_3}{dt} + G_1(V_3) + I_{C2} \sin(\phi_2) - C_j \frac{d(V_2 - V_3)}{dt} \\
 -G_1(V_2 - V_3) - I_{C1} \sin(\phi_1) + I_2 &= 0 \\
 -I_2 + C_{OUT} \frac{dV_4}{dt} + \frac{V_4}{R_{OUT}} &= 0 \\
 \frac{d\phi_1}{dt} &= P_O(V_2 - V_3) \\
 \frac{d\phi_2}{dt} &= P_O(V_3) \\
 V_1 - V_2 &= L_1 \frac{dI_1}{dt} \\
 V_3 - V_4 &= L_2 \frac{dI_2}{dt}
 \end{aligned} \tag{5.1}$$

MAPLE [4] is then used to solve for the first order derivatives of each variable (see Fig. 5.6) from (5.1).

Using Borland C/C++ version 4.0 on a PC, a program was written using the fifth-order Runge-Kutta adaptive time step routine [5] to solve the set of first-order differential equations (Appendix B). The fifth-order Runge-Kutta method is the pre-

```

> ans[1]:

$$\frac{\partial}{\partial t} \text{phi1}(t) = Po (V2(t) - V3(t))$$



---


> ans[2]:

$$\frac{\partial}{\partial t} \text{phi2}(t) = Po V3(t)$$



---


> ans[3]:

$$\frac{\partial}{\partial t} V1(t) = - \frac{2 Rd V1(t) - Rd Va(t) - Rd Vb(t) + V1(t) Rin + I1(t) Rin Rd}{Cd Rin Rd}$$



---


> ans[4]:

$$\frac{\partial}{\partial t} V2(t) = - (-2 I1(t) Rso + V3(t) - Vso(t) + G1(V3(t)) Rso + Ic2 \sin(\text{phi2}(t)) Rso + I2(t) Rso + G1(V2(t) - V3(t)) Rso + Ic1 \sin(\text{phi1}(t)) Rso) / (Cj Rso)$$



---


> ans[5]:

$$\frac{\partial}{\partial t} V3(t) = - \frac{-I1(t) Rso + V3(t) - Vso(t) + G1(V3(t)) Rso + Ic2 \sin(\text{phi2}(t)) Rso + I2(t) Rso}{Cj Rso}$$



---


> ans[6]:

$$\frac{\partial}{\partial t} V4(t) = \frac{I2(t) Rout - V4(t)}{Cout Rout}$$



---


> ans[7]:

$$\frac{\partial}{\partial t} I1(t) = - \frac{-V1(t) + V2(t)}{L1}$$



---


> ans[8]:

$$\frac{\partial}{\partial t} I2(t) = \frac{V3(t) - V4(t)}{L2}$$



---



```

Figure 5.6: MAPLE is used to solve first order derivatives.

ferred method for solving the ordinary differential equations, in this instance, since lookup tables are used to determine the values of input voltages at each time step and the input voltage curves are not smooth. The results for the Runge-Kutta method applied to the characteristic differential equations of the JAWS circuit are shown in Fig. 5.5 as well as the comparison to the simulation of the JAWS circuit with the FD-TLM method.

During the process of simulating the JAWS circuit with the Runge-Kutta method, it was discovered that a few parasitics automatically modeled by the FD-TLM method were not included in the conventional circuit analysis. Upon analysis of the differing results between the two methods, the inclusion of two inductors L_1 and L_2 within the conventional circuit analysis resulted in very close agreement between the FD-TLM and Runge-Kutta methods. The physical dimensions for the segments of conductors important for parasitic inductance determination were fed to the FastHenry program [2] which gave realistic values for inductances listed in Fig. 5.1. Capacitances C_d and C_{out} were added to the circuit to represent capacitance between the circuit and ground plane through the SiO_2 insulating layer. In this case, it was discovered that the FD-TLM method often predicts the existence of parasitics which might be overlooked in conventional circuit analysis.

Slight differences between the FD-TLM and conventional circuit analyses method can be attributed to slightly inaccurate extraction of the parasitic component values. For example, within the *FastHenry* inductance calculation program, the conductors were assumed to be 0.1 microns thick while the conductors are modeled as being infinitely thin in the FD-TLM method. Furthermore, instead of describing the entire superconductor wiring layout, only the physical dimensions and locations for conductors considered most important in determining parasitic inductance were included in the FastHenry data set. There is very close agreement between the FD-TLM

and circuit analyses, and the results agree with the general behavior expected which validates the FD-TLM method approach for simulating RCJL logic circuits.

Chapter 6

Magnetically Coupled Josephson Logic Circuits

6.1 Introduction

In chapter 5, FD-TLM simulations of resistively coupled Josephson logic circuits were performed and verified. However, as discussed in Chapter 4, MCJL circuits operate on a different principle than RCJL circuits requiring a different simulation method to include the dependence of critical current for the JJs as a function of externally applied flux. This chapter will show that the FD-TLM method is capable of implementing magnetically coupled Josephson logic circuits. Two different types of logic circuits will be analyzed, the DC SQUID and the (Modified Variable Threshold Logic) MVTL [14] circuit.

6.2 DC SQUID Simulation

The circuit for the 2 JJ DC SQUID is shown in Fig 6.1. This circuit is referred to as magnetically coupled Josephson logic (MCJL) as opposed to resistively coupled Josephson logic (RCJL) discussed for the JAWS circuit. The difference is that the MCJL circuit uses magnetic coupling to switch between the HVS and ZVS instead

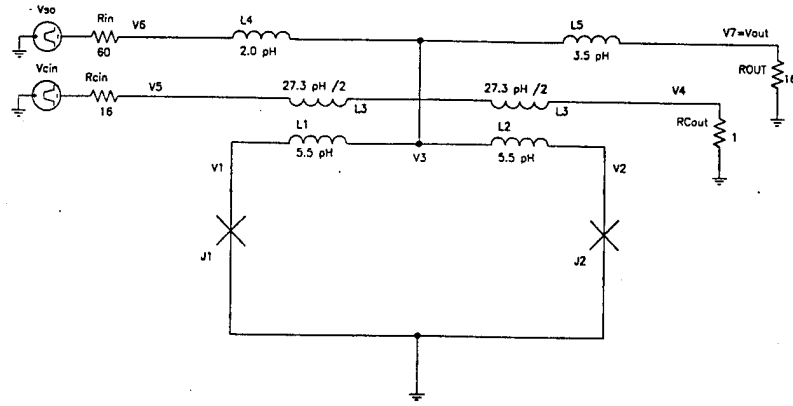


Figure 6.1: Equivalent circuit for the 2 JJ DC SQUID.

of current injection. This will be discussed in detail. The fundamental part of the two JJ DC SQUID logic gate is the SQUID loop which operates as discussed in Chapter 3. In Fig. 6.1, a biasing current is established by V_{so} with resistor R_{so} which will flow through the SQUID loop since, initially, both JJs are in the ZVS and appear as superconducting shorts.

Later, an input voltage V_{cin} is applied to the control line creating a current and, thus, a magnetic flux. The control line is magnetically coupled to the SQUID and creates the "external" flux which changes the total critical current of the SQUID loop. Switching of the SQUID to the HVS follows the basic procedure discussed in Chapter 3. If the current through the control line and, therefore, the externally applied flux, is high enough, the SQUID will no longer be capable of supporting the bias current as a superconducting current and the JJs within the loop will change to the HVS. As a result, the bias current will be shunted through the output resistance R_{out} and the gate will be in the "high" voltage state. To reset the SQUID to the ZVS (logic "low") from the HVS, the bias current established by V_{so} must be reduced to zero.

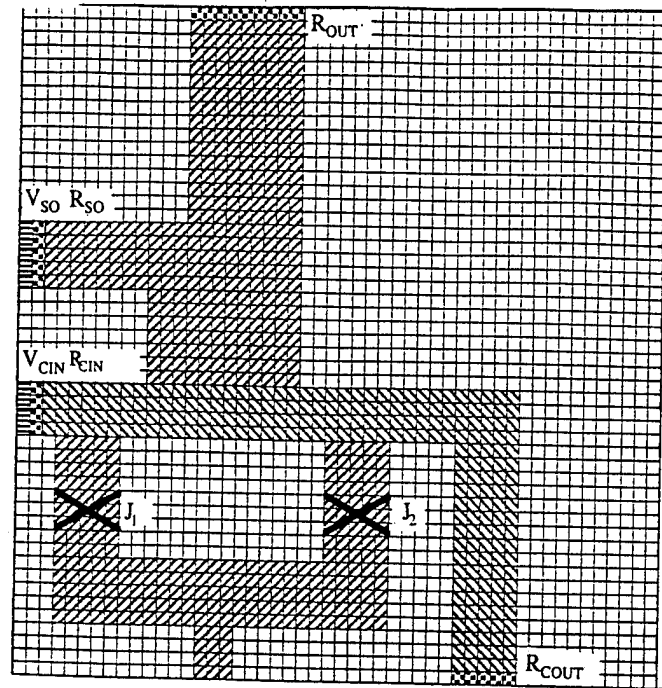


Figure 6.2: Physical layout of the DC SQUID.

6.2.1 FD-TLM implementation

Once again, *fdtgraph* is used to create the layout of the circuit and the data set for the FD-TLM method. The circuit layout is seen in Fig. 6.2. A $50 \times 50 \times 50 \text{ } \mu\text{m}^3$ (x, y, z) metal box is filled with air dielectric with perfectly-conducting boundary conditions for the walls of the box. Using the typical fabrication technique for JJ circuits the bottom of the box is used as the superconducting ground plane while a $3\text{-}\mu\text{m}$ -thick layer of SiO_2 is used between the ground plane and the base electrodes. All of the conductors are modeled as $1 \text{ } \mu\text{m}$ thick perfect conductors and are generally $5 \text{ } \mu\text{m}$ wide. The JJ parameters are the same as for the JAWS circuit discussed in the previous chapter and each JJ is implemented as a single node centered in the area to representing the tunneling barrier as before. Resistors are implemented following that of Chapter 3. Finally, voltage sources are implemented as shown in Fig. 6.1.

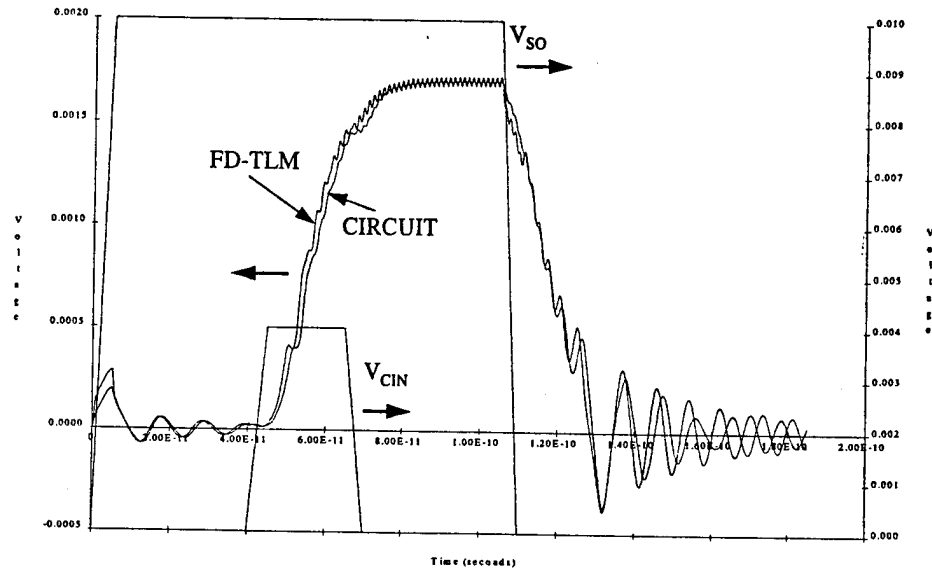


Figure 6.3: Results of simulation of the DC SQUID logic gate.

The simulation duration was 185ps and the time step was 1.7 fs. The results of the simulation are shown in Fig. 6.3.

During the simulation, as shown in Fig. 6.3, a voltage signal V_{so} is applied to generate a bias current through the SQUID loop. At this time, the output voltage remains zero, and, at a later time, a voltage is applied to the control line, V_{cin} creating a current. With a small delay, the output voltage increases to approximately 1.7 mV. When the input signal, V_{cin} returns to zero, the output voltage remains at 1.7 mV until V_{so} returns to zero. This follows the expected general behavior of the circuit validating the FD-TLM method.

6.2.2 Validation of FD-TLM results

The same procedure used for the JAWS circuit is used to validate the FD-TLM results for the two JJ DC SQUID. The circuit with labeled nodes as shown in Fig. 6.1 is

used for nodal analysis and to obtain the following set of equations.

$$\begin{aligned}
C_j \frac{dV_1}{dt} + I_c \sin(\phi_1) + G(V_1) - I_1 &= 0 \\
C_j \frac{dV_2}{dt} + I_c \sin(\phi_2) + G(V_2) - I_2 &= 0 \\
I_1 + I_2 - I_4 + I_5 &= 0 \\
\frac{V_4}{R_{COUT}} - I_3 &= 0 \\
I_3 + \frac{V_5 - V_{CLN}}{R_{CLN}} &= 0 \\
I_4 + \frac{V_6 - V_{SQ}}{R_{IN}} &= 0 \\
-I_5 + \frac{V_7}{R_{OUT}} &= 0 \\
V_3 - V_1 &= L_1 \frac{dI_1}{dt} - M_1 \frac{dI_3}{dt} \\
V_3 - V_2 &= L_2 \frac{dI_2}{dt} + M_2 \frac{dI_3}{dt} \\
V_5 - V_4 &= L_3 \frac{dI_3}{dt} - M_1 \frac{dI_1}{dt} + M_2 \frac{dI_2}{dt} \\
V_6 - V_3 &= L_4 \frac{dI_4}{dt} \\
V_3 - V_7 &= L_5 \frac{dI_5}{dt} \\
\frac{d\phi_1}{dt} &= P_O V_1 \\
\phi_2 &= \phi_1 - 2\pi(M_f I_3 + L_2 I_2 - L_1 I_1)/\Phi_O
\end{aligned} \tag{6.1}$$

All inductance values and mutual inductances were extracted from the layout by providing a description of the layout to the *FastHenry* program (see Appendix C). MAPLE was then used to solve the nodal equations for a set of first-order differential equations (see Appendix C). The fifth-order adaptive-time step Runge-Kutta method was used to solve the set of differential equations, the results of which are shown in Fig. 6.3. along with comparison to the results of the FD-TLM method. Excellent agreement between the two methods validates the FD-TLM method.

Several conventional circuit simulations of the SQUID were performed to judge the sensitivity of the circuit performance to changes in the values of parasitic components. Capacitance to ground and capacitance between the control line and SQUID loop were included in prior simulations and were found to have little effect on cir-

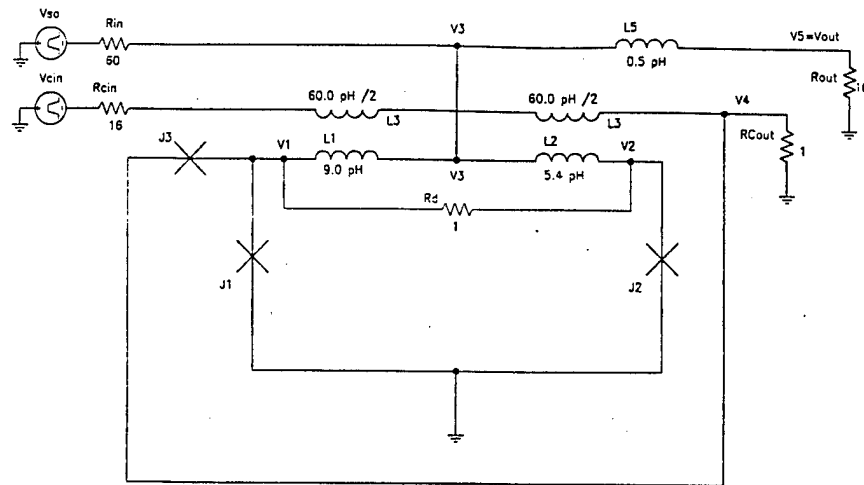


Figure 6.4: Equivalent Circuit for the MVTL logic gate.

circuit operation while different inductance values greatly altered the operation of the circuit. Minor differences in the results for the FD-TLM method and the conventional circuit simulation method can be attributed to slightly inaccurate values for the inductances extracted from the physical layout of the circuit.

6.3 MVTL Simulation

The MVTL circuit uses a combination of current injection, increasing current through the JJ to trigger the onset of the HVS, and magnetic coupling to lower the effective critical current of the SQUID loop. Fig. 6.4 shows this clearly, where the input current flows through the control line creating flux to lower the total critical current of the SQUID and, at the same time, is injected into the top of the SQUID loop to increase the current through the SQUID loop and force a more rapid transition to the HVS. The combination of current injection and magnetic coupling

is the key to giving the MVTL logic gate the fastest switching time of all the logic gates discussed.

Analyzing the operation of the MVTL circuit, a biasing current through the SQUID loop is established by the voltage source V_{so} . At this point, the total current through the SQUID loop is less than the total critical current, and the JJs remain in the ZVS, behaving as superconducting shorts. When an input signal is applied to the control line, the current creates a flux which, when coupled to the SQUID loop, lowers the total critical current of the SQUID loop. The input current flows to ground through J_3 and the SQUID loop, which are both in the ZVS. The reduction of total critical current and injection of additional current sends the SQUID into the HVS. At this point, the biasing current will flow through J_3 and R_{cout} to ground, and the input current caused by V_{cin} will flow through R_{cout} to ground. The biasing current has a larger value than the input current and will force J_3 into the HVS, which then steers the input current through R_{cout} , while the biasing current flows through the output resistance R_{out} . At this point, the MVTL circuit is in the logic "high" state. Due to the hysteresis of the JJs, the input and biasing currents must both be reduced to zero to allow the JJs to return to the ZVS and, thus, return the logic gate to a logic "low".

6.3.1 FD-TLM implementation

As before, the circuit is placed in a $50 \times 50 \times 50 \mu\text{m}^3$ (x, y, z) box filled with air and the walls of the box are modeled as perfect conductors. The bottom surface of the box is used as the superconducting ground plane and a $3 \mu\text{m}$ thick layer of SiO_2 is placed at the bottom of the box on which the rest of the circuit is modeled. All conductors are modeled as perfect conductors being $1 \mu\text{m}$ thick, and generally $5 \mu\text{m}$ wide. Fig 6.5. shows the physical layout of the circuit.

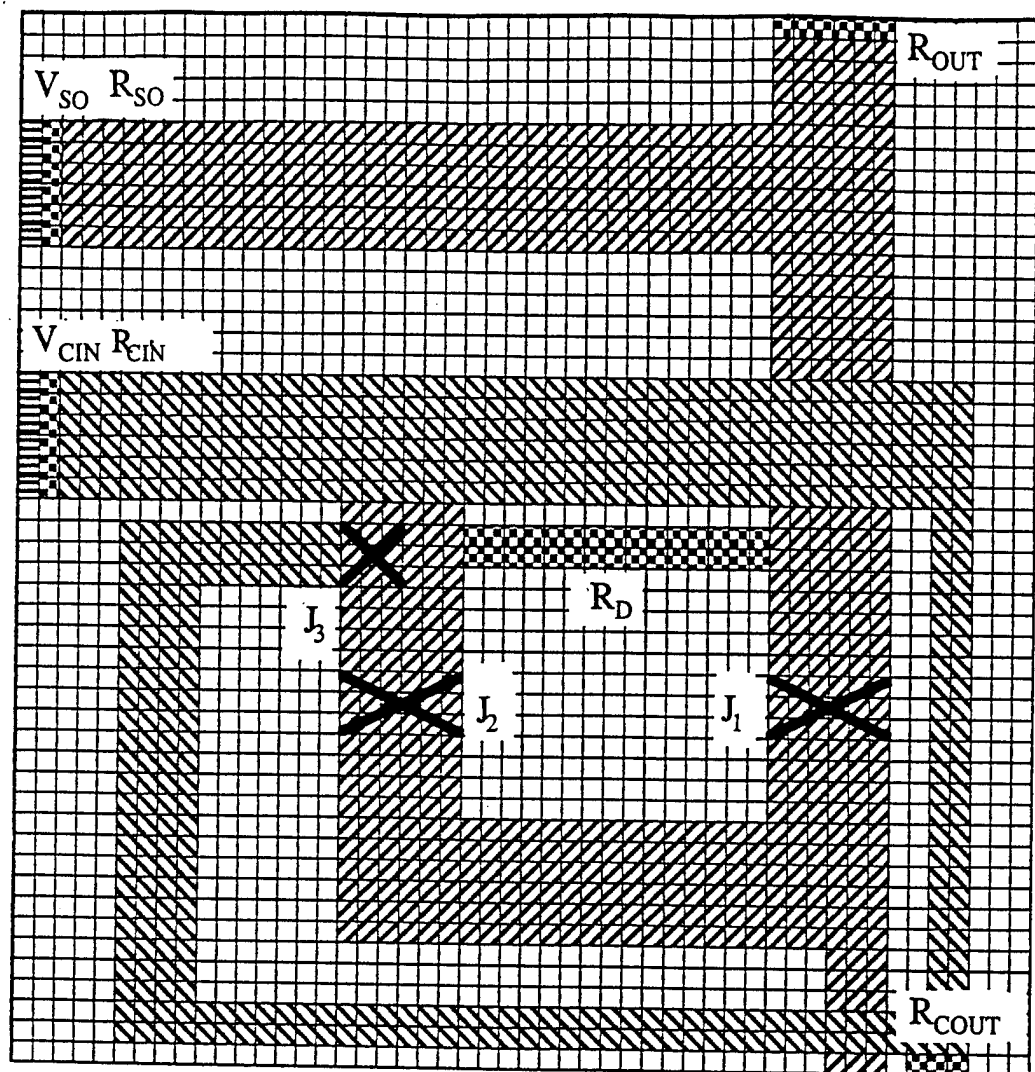


Figure 6.5: Physical layout of the MVTL circuit used in FD-TLM simulation.

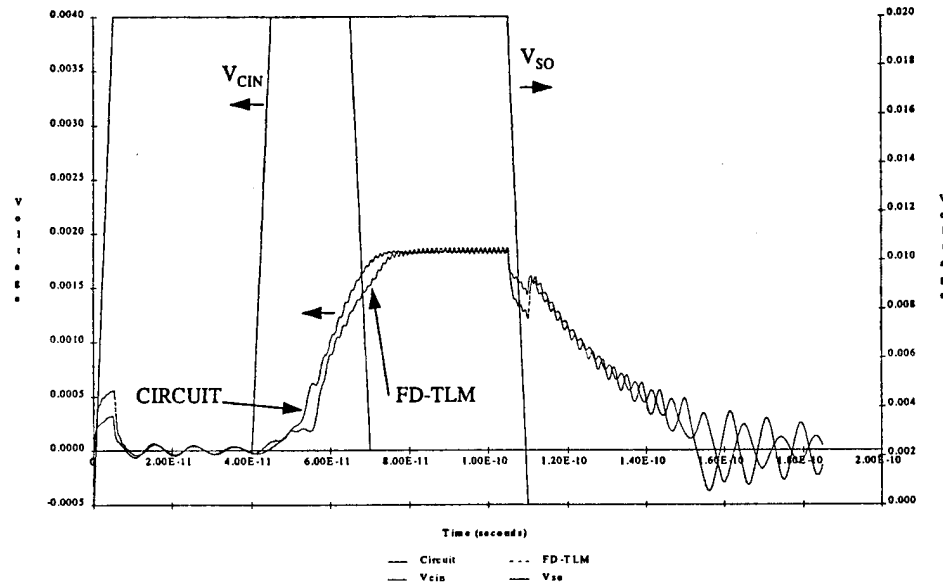


Figure 6.6: Results of simulation of the MVTL logic gate.

The voltage source waveforms are shown in Fig. 6.6. The JJs are implemented using the same parameters as before with the exception of J_2 having a critical current and junction capacitance three times that of J_1 and J_3 .

As before, the JJs are implemented as a node centered in the area representing the tunneling barrier of the JJ. Appendix D lists the FD-TLM data set describing the MVTL circuit. The simulation is performed for 185 ps with a 1.7 fs time step dictated by the $1 \mu\text{m}$ uniform grid spacing used in the FD-TLM method. FD-TLM method results are shown in Fig. 6.6.

6.3.2 Validation of the FD-TLM results

To perform conventional circuit analysis for comparison to the FD-TLM results, nodal analysis is performed on the circuit giving the following equations:

$$\begin{aligned}
& I_{C1}\sin(\phi_1) + C_{j1}\frac{dV_1}{dt} + G_1(V_1) + \frac{V_1-V_2}{R_D} \\
& -I_1 + I_{C3}\sin(\phi_3) + G_3(V_1 - V_4) + C_{j3}\frac{d(V_1-V_4)}{dt} = 0 \\
& I_{C2}\sin(\phi_2) + C_{j2}\frac{dV_2}{dt} + G_2(V_2) + \frac{V_2-V_1}{R_D} - I_2 = 0 \\
& I_1 + I_2 + \frac{V_3-V_{IN}}{R_{IN}} + I_4 = 0 \\
& \frac{V_4}{R_{COUT}} - I_3 - I_{C3}\sin(\phi_3) - G_3(V_1 - V_4) - C_{j3}\frac{d(V_1-V_4)}{dt} = 0 \\
& -I_4 + \frac{V_5}{R_{OUT}} = 0 \\
& I_3 = V_{CIN} - \frac{(L_3\frac{dI_3}{dt} - M_1\frac{dI_1}{dt} + M_2\frac{dI_2}{dt}) + V_4}{R_{CIN}} \tag{6.2} \\
& V_3 - V_1 = L_1\frac{dI_1}{dt} - M_1\frac{dI_3}{dt} \\
& V_3 - V_2 = L_2\frac{dI_2}{dt} + M_2\frac{dI_3}{dt} \\
& \frac{d\phi_1}{dt} = P_O V_1 \\
& \frac{d\phi_3}{dt} = P_O(V_1 - V_4) \\
& V_3 - V_5 = L_4\frac{dI_4}{dt} \\
& \phi_2 = \phi_1 - 2\pi(M_f I_3 + L_2 I_2 - L_1 I_1)/\Phi_O
\end{aligned}$$

Important pieces of the physical layout of the circuit used for the FD-TLM method are extracted and the physical dimensions and parameters were provided to the FastHenry program to calculate and extract the inductances and mutual inductances as well as the coupling between the control line and SQUID loop (see Appendix D). MAPLE is used to solve for a set of first-order differential equations (see Appendix D) and these equations were then solved using the fifth-order time-adaptive Runge-Kutta method. Results of this method are shown in Fig. 6.6 along with the FD-TLM method results.

Comparison of the FD-TLM method results and the Runge-Kutta results show excellent agreement therefore validating the FD-TLM method for modeling the MVTL circuit. Furthermore, the results for both the FD-TLM and Runge-Kutta methods agree with the expected logic functioning of the circuit described earlier. Minor differences can be attributed to inexact values for the inductances and magnetic coupling

calculated with *FastHenry* as well as parasitics that are modeled by the FD-TLM method and are omitted in the conventional circuit analysis.

Chapter 7

Conclusion

With the advent of high speed digital integrated circuits, analysis and design is becoming ever more difficult with the need for determination of the effects of propagation delay, crosstalk, dispersion, signal reflections, signal reflections from the package walls, radiation, and modal dispersion. Furthermore, additional parasitics must be analyzed at the higher operating speeds where the capacitances and inductances often need to be simulated as distributed rather than lumped components. JJ logic circuits can operate at frequencies from 1 GHz to 100 GHz necessitating consideration of high frequency electromagnetic effects just discussed.

Quasi-static simulation methods such as SPICE are inadequate at modeling JJ logic circuits since the cross-sectional dimensions of the circuit may be comparable to the wavelength of the signals involved. Furthermore, although a conventional circuit simulation method can analyze propagation delays, crosstalk, and parasitics, such analysis requires painstaking effort to extract the values of capacitances and inductances within the circuit.

The FD-TLM method allows an individual to describe the physical geometry of a JJ logic IC where the the parasitics are automatically modeled and separate extraction is not required. The FD-TLM method solves Maxwell's curl equations, as described in Chapter 3, allowing simultaneous simulation of the operation of the logic gate

and electromagnetic parasitics. As a result, the user can simulate a JJ logic circuit with confidence that the circuit being simulated will work as predicted. The only extraction required is that of the process parameter values for the JJ describing the current-voltage relationship of the JJ.

In Chapters 5 and 6 several different logic circuits were simulated and analyzed to validate the FD-TLM method for modeling JJ circuits. Before performing conventional circuit analysis, special care was taken in designing the FD-TLM layout so that parasitics which could not be simulated in conventional circuit analysis were minimized. This often required several trial and error simulations to reduce, for example, the lengths of conductors, or rearranging the geometry of the layout.

Upon examining the FD-TLM results, earlier statements concerning the utility of the FD-TLM method were substantiated. That is, the FD-TLM method often predicts the existence of parasitics omitted in conventional circuit simulation. Differing results between conventional circuit simulation and FD-TLM simulation usually indicated that not all parasitics had been included in the conventional circuit simulation. Adjusting the conventional circuit simulation to take these effects into account ultimately lead to close agreement between the two methods. As a result, the FD-TLM method often became a tool for learning details about the JJ and JJ logic circuit operation that are not discussed in reference papers and books.

The final results of Chapters 5 and 6 showed that the FD-TLM method is not only reliable for simulating JJ logic circuits, but that it is invaluable as well. In this thesis, effort was focused on simulating and validating the results of simulation for JJ logic circuits. The conclusion was that with proper incorporation of both dc and ac characteristics of the JJ device, any type of JJ circuit can be simulated correctly.

Simulations of JJ logic circuits using the FD-TLM method took approximately two hours on average. On the other hand, conventional circuit simulation using the

Runge-Kutta method often took approximately 15 minutes. The justification for using the FD-TLM method in this situation is that the FD-TLM method provides the full electromagnetic behavior of the circuit instead of using, possibly unjustified, quasi-static approximations. In addition, the process required to perform a nodal analysis for each circuit and extract the parasitic inductance and capacitance was far more time consuming than the two hour simulation time for FD-TLM simulation. With this new method for simulating Josephson junction circuits, it is possible for fabrication procedures to be directly converted to an FD-TLM data set for full electromagnetic simulation of the fabricated JJ IC circuit. This means that the FD-TLM method can be used to directly simulate a fabricated IC and determine problems with design as well as theoretical circuit operation.

Future work in this area includes extension of the FD-TLM method to model the skin effect in superconductivity where resistance exists at high frequencies within superconductors. The skin effect becomes important at frequencies above 100 GHz, and has already been modeled with the FD-TD method [18]. Future work may also include simulation of several types of JJ logic circuits appearing in print as well as simulation of chip packages. Ultimately, work should be pursued in collaboration with individuals performing fabrication of JJ IC circuits to compare FD-TLM simulation with real-time results to further validate the method.

Appendix A

FORTRAN Code for JJ Implementation

This section contains the portions of the FORTRAN source code for the FD-TLM method which was updated to model the Josephson junction (JJ) and SQUID.

```
C               PROGRAM FDVCUFOR
C   Modified March, 1995 by Christopher G. Sentelle
C
C   Josephson Junctions are specified by the following parameters:
C   JJIC, the critical current, JJPO, the plasma oscillation frequency
C   JJG1, subgap conductance (linear resistance), JJI1, JJG2, JJVS, and JJVT,
C   parameters based on manufacture of the Josephson Junction.
C   In order to include magnetic effects on the critical current,
C   we specify PHIO.
C   The equation describing non-SC conductance is taken from
C   Rollins, Greg J., "Numerical Simulator for Superconducting
C   Integrated Circuits", IEEE Trans. on Comp.-Aided Design,
C   Vol 10, No 2., p 246, Feb. 1991.
C
C   The Josephson Junction is specified by 'R' as the model indicator
C   and indicates implementation
C   of changing conductance specified by the Josephson Junction model at
C   the xyz location specified by the 'R' statement.
C
C   In addition to implementing the simulation of the JJ,
C   this version of the FDTLM program allows coupling of the
C   SQUID device by forcing a couple between two JJ's that are
C   connected in a superconductive ring. This method alters the
C   critical current of the JJ's based on the magnetic flux evident
C   in the loop. The following device card is used to specify a
C   Josephson Junction SQUID.
C
C   H  X1  X2  YPLN  Z1  Z2  JJ1  JJ2
```

```

C
C   where X1,X2,Z1, and Z2 specify the area of the superconducting ring.
C   JJ1 and JJ2 are the number specifiers for the JJ's that are affected
C   by the superconductive ring and are coupled. YPLN specifies the
C   location of the flux area
C
C
C   H  2 JJ SQUID coupling
C   R  Josephson Junction
C
C
C   Read DATA for the Josephson Junction Model
C   Josephson Junctions (R or r).
C
C
C   Get the X,Y,Z directions for the Josephson Junction
C
1000 CALL GETDAT(IXLO,FJUNK,AJUNK,ICURSR,AINPUT,1)
      IF ((IXLO .LT. 1) .OR. (IXLO .GT. NX)) THEN
          WRITE(8,160) AINPUT
          WRITE(8,482) IXLO,NX
          STOP
      ENDIF
C
      CALL GETDAT(IXHI,FJUNK,AJUNK,ICURSR,AINPUT,1)
      IF ((IXHI .LT. 1) .OR. (IXHI .GT. NX)) THEN
          WRITE(8,160) AINPUT
          WRITE(8,482) IXHI, NX
          STOP
      ENDIF
C
      CALL GETDAT(IYPOS,FJUNK,AJUNK,ICURSR,AINPUT,1)
      IF ((IYPOS .LT. 1) .OR. (IYPOS .GT. NY)) THEN
          WRITE(8,160) AINPUT
          WRITE(8,483) IYPOS,NY
          STOP
      ENDIF
C
      CALL GETDAT(IZLO,FJUNK,AJUNK,ICURSR,AINPUT,1)
      IF ((IZLO .LT. 1) .OR. (IZLO .GT. NZ)) THEN
          WRITE(8,160) AINPUT
          WRITE(8,484) IZLO, NZ
          STOP
      ENDIF
C
      CALL GETDAT(IZHI,FJUNK,AJUNK,ICURSR,AINPUT,1)
      IF ((IZHI .LT. 1) .OR. (IZHI .GT. NZ)) THEN
          WRITE(8,160) AINPUT
          WRITE(8,484) IZHI, NZ
          STOP
      ENDIF

```

```

C
C   Get the Plasma Frequency Po
C
C   CALL GETDAT(IJUNK,JJPO,AJUNK,ICURSR,AINPUT,2)
C
C   Get the Critical Current of the Josephson Junction
C
C   CALL GETDAT(IJUNK,JJIC,AJUNK,ICURSR,AINPUT,2)
C
C   Get the sub-gap conductance for the Josephson Junction
C
C   CALL GETDAT(IJUNK,JJG1,AJUNK,ICURSR,AINPUT,2)
C
C
C   CALL GETDAT(IJUNK,JJI1,AJUNK,ICURSR,AINPUT,2)
C
C   CALL GETDAT(IJUNK,JJG2,AJUNK,ICURSR,AINPUT,2)
C
C   CALL GETDAT(IJUNK,JJVS,AJUNK,ICURSR,AINPUT,2)
C
C   CALL GETDAT(IJUNK,JJVT,AJUNK,ICURSR,AINPUT,2)
C
C   CALL GETDAT(IJUNK,JJCJ,AJUNK,ICURSR,AINPUT,2)
C
C   CALL GETDAT(IJUNK,JJDEP,AJUNK,ICURSR,AINPUT,2)
C
C       NJJ = NJJ + 1
C
C   Check whether the array will overflow.
C
C       IF (NJJ .GT. LJJ) THEN
C           WRITE(8,160) AINPUT
C           WRITE(8,930) LJJ
930       FORMAT(' The number of Josephson Junctions ',
1           'is greater than'/'the array size LJJ = ',
2           I5,'. Increase LJJ and recompile. ')
C           STOP
C           ENDIF
C
C       IJJ(1,NJJ) = (IXHI+IXLO)/2
C       IJJ(2,NJJ) = IYPOS
C       IJJ(3,NJJ) = (IZHI+IZLO)/2
C       IJJ(4,NJJ) = IXLO
C       IJJ(5,NJJ) = IXHI
C       IJJ(6,NJJ) = IZLO
C       IJJ(7,NJJ) = IZHI
C
C       FJJ(1,NJJ) = JJPO
C       FJJ(2,NJJ) = JJIC
C       FJJ(3,NJJ) = JJG1
C       FJJ(4,NJJ) = JJI1

```

```

        FJJ(5,NJJ) = JJG2
        FJJ(6,NJJ) = JJVS
        FJJ(7,NJJ) = JJVT
        FJJ(8,NJJ) = JJCJ
        FJJ(10,NJJ) = JJDEP
        FJJ(13,NJJ) = ZERO
9999     FORMAT(G10.4)
9998     FORMAT(I5)
C
C
        GOTO 1500
C
C
C     Data Entry for the Squid Coupling Device.  Parameter 'H'
C
1200     NSQUID = NSQUID + 1
        IF ( NSQUID .GT. LSQUID ) THEN
            WRITE(8,160) AINPUT
            WRITE(8,1201) LSQUID
1201     FORMAT(' The number of Squids exceeds the maximum allowed ',I5)
            STOP
        ENDIF
        CALL GETDAT(IXLO,FJUNK,AJUNK,ICURSR,AINPUT,1)
        CALL GETDAT(IXHI,FJUNK,AJUNK,ICURSR,AINPUT,1)
        CALL GETDAT(IYPOS,FJUNK,AJUNK,ICURSR,AINPUT,1)
        CALL GETDAT(IZLO,FJUNK,AJUNK,ICURSR,AINPUT,1)
        CALL GETDAT(IZHI,FJUNK,AJUNK,ICURSR,AINPUT,1)
        CALL GETDAT(JJ1,FJUNK,AJUNK,ICURSR,AINPUT,1)
        CALL GETDAT(JJ2,FJUNK,AJUNK,ICURSR,AINPUT,1)
C
C     Check to be sure there are no obvious errors in the the device parameters
C
        IF ((IXLO .LT. 1) .OR. (IXLO .GT. NX)) THEN
            WRITE(8,160) AINPUT
            WRITE(8,482) NX
            STOP
        ENDIF
C
        IF ((IXHI .LT. 1) .OR. (IXHI .GT. NX)) THEN
            WRITE(8,160) AINPUT
            WRITE(8,482) NX
            STOP
        ENDIF
C
        IF ((IYPOS .LT. 1) .OR. (IYPOS .GT. NY)) THEN
            WRITE(8,160) AINPUT
            WRITE(8,482) NY
            STOP
        ENDIF
C
        IF ((IZLO .LT. 1) .OR. (IZHI .GT. NZ)) THEN

```

```

        WRITE(8,160) AINPUT
        WRITE(8,484) NZ
        STOP
    ENDIF
C
    IF ((IZHI .LT. 1) .OR. (IZHI .GT. NZ)) THEN
        WRITE(8,160) AINPUT
        WRITE(8,484) NZ
        STOP
    ENDIF
C
    IF ((JJ1 .GT. NJJ) .OR. (JJ2 .GT. NJJ)) THEN
        WRITE(8,160) AINPUT
        WRITE(8,1202)
1202    FORMAT('Specify JJs before specifying SQUID couplings..')
        STOP
    ENDIF
C
C    Place the information into the Squid array
C
    ISQUID(1,NSQUID) = IXLO
    ISQUID(2,NSQUID) = IXHI
    ISQUID(3,NSQUID) = IYPOS
    ISQUID(4,NSQUID) = IZLO
    ISQUID(5,NSQUID) = IZHI
    ISQUID(6,NSQUID) = JJ1
    ISQUID(7,NSQUID) = JJ2
    FJJ(13,JJ1) = ZERO
    FJJ(13,JJ2) = NSQUID
C
    GOTO 1500
C
C
C    ***** E field calculations
C
C$DOACROSS LOCAL(I,J,K)
    DO 5350 K = 1, NZ
        DO 5300 J = 1, NY
            DO 5250 I = 1, NX
                EX(I,J,K) = EXE(I,J,K)*EX(I,J,K) + EXH(I,J,K)*
1                (HZ(I,J,K) - HZ(I,J-1,K) + HY(I,J,K-1) - HY(I,J,K))
C
                EY(I,J,K) = EYE(I,J,K)*EY(I,J,K) + EYH(I,J,K)*
1                (HX(I,J,K) - HX(I,J,K-1) + HZ(I-1,J,K) - HZ(I,J,K))
C
                EZ(I,J,K) = EZE(I,J,K)*EZ(I,J,K) + EZH(I,J,K)*
1                (HY(I,J,K) - HY(I-1,J,K) + HX(I,J-1,K) - HX(I,J,K))
            5250    CONTINUE
        5300    CONTINUE
    5350    CONTINUE
C

```

```

C      Special FD-TLM Ey field equations are used for the JJ.
C
DO 5400 M=1, NJJ
    I = IJJ(1,M)
    J = IJJ(2,M)
    K = IJJ(3,M)
C
C      Calculate the old Ey electric field from the new Ey.
    EY(I,J,K) = (EY(I,J,K) - EYH(I,J,K)*
1          (HX(I,J,K)-HX(I,J,K-1)+HZ(I-1,J,K)-HZ(I,J,K)))
2          /EYE(I,J,K)
C
C      Calculate the JJ phase
    IF (FJJ(13,M) .EQ. ZERO) THEN
        FJJ(11,M) = FJJ(11,M) - FJJ(1,M)*DELTAT*EY(I,J,K)
    ELSE
        IXLO = ISQUID(1,FJJ(13,M))
        IXHI = ISQUID(2,FJJ(13,M))
        IYPOS = ISQUID(3,FJJ(13,M))
        IZLO = ISQUID(4,FJJ(13,M))
        IZHI = ISQUID(5,FJJ(13,M))
        JJ1 = ISQUID(6,FJJ(13,M))
        JJ2 = ISQUID(7,FJJ(13,M))
        FLUXJJ = ZERO
        DO 5500 J1 = IXLO, IXHI
            DO 5501 K1 = IZLO, IZHI
                FLUXJJ = FLUXJJ+UO*HY(J1,IYPOS,K1)*DELTAL*U(J1)
1                *W(K1)/V(IYPOS)
5501            CONTINUE
5500        CONTINUE
        FLUXJJ = TWO*PI*FLUXJJ/FLUXO
        FJJ(11,M) = FJJ(11,JJ1) - FLUXJJ
    ENDIF
C      Prevent phase overflow.
    IF (FJJ(11,M) .GT. (TWO*PI)) FJJ(11,M) = FJJ(11,M) - TWO*PI
C
C      Calculate the total flux magnitude at the JJ node
    FLUXJJX = ZERO
    FLUXJJZ = ZERO
C      DO 5401 I1=IJJ(4,M),IJJ(5,M)
C          FLUXJJZ = FLUXJJZ + HZ(I1,J,K)
C 5401 CONTINUE
C      DO 5402 I1 = IJJ(6,M),IJJ(7,M)
C          FLUXJJX = FLUXJJX + HX(I,J,I1)
C 5402 CONTINUE
C      FLUXJJZ = FLUXJJZ * UO * FJJ(10,M)
C      FLUXJJX = FLUXJJX * UO * FJJ(10,M)
C      FLUXJJ = SQRT(FLUXJJZ*FLUXJJZ+FLUXJJX*FLUXJJX)
C      IF (FLUXJJ .LT. 1.0D-200) THEN
C          FLUXJJ = ONE
C      ELSE

```

```

C      FLUXJJ = ABS(SIN(PI*FLUXJJ/FLUXO)/((PI*FLUXJJ)/FLUXO))
C      END IF
C      FLUXJJ = ONE
C
C
C      Calculate the JJ superconducting current including
C      critical current effects from the magnetic flux
C      FJJ(12,M) = FJJ(2,M)*SIN(FJJ(11,M))*FLUXJJ
C
C      Calculate the new Ey field including the effect of the JJ.
C      EY(I,J,K) = EY(I,J,K) * (EYE(I,J,K)
1          - HALF * EYH(I,J,K) * FJJ(2,M)
2          * COS(FJJ(11,M)) * FJJ(1,M)
3          * DELTAT)
4          + EYH(I,J,K) * (HX(I,J,K) - HX(I,J,K-1)
5          + HZ(I-1,J,K) - HZ(I,J,K)
6          + FJJ(12,M))
C
C      5400 CONTINUE
C
C      Update the Josephson Junction conductances, capacitances remain constant
C
C      Remember the following assignments
C      IJJ(1,I) = x position of JJ
C      IJJ(2,I) = y position of JJ
C      IJJ(3,I) = z position of JJ
C
C      FJJ(1,I) = Plasma Frequency Po
C      FJJ(2,I) = Critical Current IC
C      FJJ(3,I) = sub-gap conductance G1
C      FJJ(4,I) = I1 (parameter based on manufacture)
C      FJJ(5,I) = G2 (parameter based on manufacture)
C      FJJ(6,I) = VS (parameter based on manufacture)
C      FJJ(7,I) = VT (parameter based on manufacture)
C      FJJ(8,I) = Cj Capacitance of the JJ
C      FJJ(9,I) = node admittance without the Josephson Junction
C      FJJ(10,I) = Depth of Josephson Junction
C      FJJ(11,I) = phi for the JJ
C      FJJ(12,I) = IJ for the JJ
C      FJJ(13,I) = Boolean, Update phase based on voltage? Used for Squid couple
C
C      DO 6000 I = 1,NJJ
C
C      Calculate the voltage across the JJ.
C      VJJ = -EY(IJJ(1,I),IJJ(2,I),IJJ(3,I))
C
C      GJR = FJJ(3,I)*VJJ+(FJJ(4,I)+FJJ(5,I)*ABS(VJJ))*(1/(1+
1          EXP((FJJ(6,I)-VJJ)/FJJ(7,I)))-
2          1/(1+EXP((FJJ(6,I)+VJJ)/FJJ(7,I))))
C

```

```

C      Calculate conductance to give required current at specified V
      IF (VJJ .EQ. ZERO) THEN
        GJJ = ZERO
      ELSE
        GJJ = ZO*GJR/VJJ
      END IF

C
      YSJ = TWO*H*FJJ(8,I)/(EO*DELTAL)
      EYE(IJJ(1,I),IJJ(2,I),IJJ(3,I)) = ONE -
1      TWO*GJJ/(GJJ+FJJ(9,I)+YSJ)
      EYH(IJJ(1,I),IJJ(2,I),IJJ(3,I)) = TWO * ZO
1      /(GJJ+FJJ(9,I)+YSJ)

C
6000 CONTINUE

C
C      Calculations for coupling between JJ devices to form a two junction SQUID
C
C      ISQUID(1,I) = IXLO
C      ISQUID(2,I) = IXHI
C      ISQUID(3,I) = IZLO
C      ISQUID(4,I) = IZHI
C      ISQUID(5,I) = 1st Josephson Device to be linked
C      ISQUID(6,I) = 2nd Josephson Device to be linked
C
C      DO 6001 I = 1,NSQUID
C        IXLO = ISQUID(1,I)
C        IXHI = ISQUID(2,I)
C        IYPOS = ISQUID(3,I)
C        IZLO = ISQUID(4,I)
C        IZHI = ISQUID(5,I)
C        JJ1 = ISQUID(6,I)
C        JJ2 = ISQUID(7,I)
C        FLUXJJ = ZERO
C      We first calculate the flux, Hy going through the area
C      DO 6002 J = IXLO, IXHI
C        DO 6003 K = IZLO, IZHI
C          FLUXJJ = FLUXJJ+UO*HY(J,IYPOS,K)*DELTAL*U(J)*W(K)/V(IYPOS)
C 6003      CONTINUE
C 6002 CONTINUE
C      We will link the squid JJ's with the pi*flux/fluxo relationship
C      by adjusting the phase of the second JJ listed, JJ2
C      In a coupled squid, the only way to change the value of
C      the phase of the second JJ is by altering the first JJ or
C      altering the flux. This alteration is only performed at this
C      stage. In the main iterative loop, the phase for JJ2 of this couple
C      is not allowed to change. This routine will set its phase.
C
C      The next step will be to determine the phase differences
C
C      FLUXJJ = TWO*PI*FLUXJJ/FLUXO
C

```

```
C      We now adjust the coupled Josephson Junctions
C      FJJ(11,JJ2) = FJJ(11,JJ1)+FLUXJJ
C
C 6001 CONTINUE
```

Appendix B

JAWS Simulation Data

The section contains the FD-TLM Data Set, the *FastHenry* extraction data set, MAPLE V results, and the C program for performing the conventional circuit simulation for the JAWS circuit.

B.1 FD-TLM Data Set

NFRCJL5

T RCJL Josephson Junction Logic

*Generated by FDTGRAPH, copyright 1993, by Christopher G. Sentelle

*Data in format to be used by FD-TLM copyright by Dr. Robert H. Voelker

*University of Nebraska-Lincoln

*

*Modified for simtime and pulses on Sept 6, 1995

*

*Created on: Thu Jun 29 13:02:33 1995

*

* In this simulation, we try to reduce parasitic capacitance and inductance

* with a couple of methods. First, all of the conducting lines are

* made to be infinitely thin to take care of parasitic inductance.

* There should be little to no crosstalk in this circuit because

* everything is orthogonalized as much as possible. We also reduce

* the area of the JJs in order to try to reduce a capacitance that may

* be occurring between the junction overriding the capacitance we are

* trying to create via the Josephson Junction itself. We are also

* moving the entire circuit at a higher level, 2 microns from

* ground in order to reduce the parasitic capacitance to ground.

*

*Medium material used throughout

*Relative permittivity

E 1 50 1 25 1 50 1 1 1

```

*Conductivity throughout
L 1 50 1 25 1 50 0 0 0
*Magnetic susceptibility
M 1 50 1 25 1 50 0 0 0
*Relative permeability
U 1 50 1 25 1 50 1 1 1
*Add for a SiO2 substrate
E 1 50 1 2 1 50 3.5 3.5 3.5
* Josephson Junction #1
R 6 7 3 12 13 3.039e+15 7e-05 0.004 0 0.1 0.002 0.0001 5e-13 5e-11
* Josephson Junction #2
R 6 7 3 22 23 3.039e+15 0.0001 0.004 0 0.1 0.002 0.0001 5e-13 5e-11
*Infinitely Thin object, xz-plane Conductor
L 6 8 3 3 3 8 -1 -2 -1
L 9 9 3 3 3 8 -2 -2 -1
L 6 8 3 3 9 9 -1 -2 -2
*Infinitely Thin object, xz-plane Conductor
L 12 14 3 3 3 8 -1 -2 -1
L 15 15 3 3 3 8 -2 -2 -1
L 12 14 3 3 9 9 -1 -2 -2
*Infinitely Thin object, xz-plane Conductor
L 9 11 3 3 6 8 -1 -2 -1
L 12 12 3 3 6 8 -2 -2 -1
L 9 11 3 3 9 9 -1 -2 -2
*Infinitely Thin object, xz-plane Conductor
L 2 5 3 3 6 8 -1 -2 -1
L 6 6 3 3 6 8 -2 -2 -1
L 2 5 3 3 9 9 -1 -2 -2
*Infinitely Thin object, xz-plane Conductor
L 6 8 3 3 9 11 -1 -2 -1
L 9 9 3 3 9 11 -2 -2 -1
L 6 8 3 3 12 12 -1 -2 -2
*Infinitely Thin object, xz-plane Conductor
L 6 7 3 3 12 13 -1 -2 -1
L 8 8 3 3 12 13 -2 -2 -1
L 6 7 3 3 14 14 -1 -2 -2
*Infinitely Thin object, xz-plane Conductor
L 18 20 4 4 3 18 -1 -2 -1
L 21 21 4 4 3 18 -2 -2 -1
L 18 20 4 4 19 19 -1 -2 -2
*Infinitely Thin object, xz-plane Conductor
L 6 17 4 4 16 18 -1 -2 -1
L 18 18 4 4 16 18 -2 -2 -1
L 6 17 4 4 19 19 -1 -2 -2
*Infinitely Thin object, xz-plane Conductor
L 6 8 4 4 14 15 -1 -2 -1
L 9 9 4 4 14 15 -2 -2 -1
L 6 8 4 4 16 16 -1 -2 -2
*Infinitely Thin object, xz-plane Conductor
L 6 7 4 4 12 13 -1 -2 -1
L 8 8 4 4 12 13 -2 -2 -1

```

```

L 6 7 4 4 14 14 -1 -2 -2
*Infinitely Thin object, xz-plane Conductor
L 2 5 4 4 16 18 -1 -2 -1
L 6 6 4 4 16 18 -2 -2 -1
L 2 5 4 4 19 19 -1 -2 -2
*Infinitely Thin object, xz-plane Conductor
L 6 8 4 4 19 21 -1 -2 -1
L 9 9 4 4 19 21 -2 -2 -1
L 6 8 4 4 22 22 -1 -2 -2
*Infinitely Thin object, xz-plane Conductor
L 6 7 3 4 22 23 -1 -2 -1
L 8 8 3 4 22 23 -2 -2 -1
L 6 7 3 4 24 24 -1 -2 -2
*Infinitely Thin object, xz-plane Conductor
L 1 5 3 3 22 24 -1 -2 -1
L 6 6 3 3 22 24 -2 -2 -1
L 1 5 3 3 25 25 -1 -2 -2
* These values of resistance had to be corrected by hand.
*Infinitely Thin object, xz-plane Resistor 45 ohm z-directed
L 12 14 3 3 2 2 -2 -2 5555.56
L 15 15 3 3 2 2 -2 -2 5555.56
*Infinitely Thin object, xz-plane Resistor 45 ohm z-directed
L 6 8 3 3 2 2 -2 -2 5555.56
L 9 9 3 3 2 2 -2 -2 5555.56
*Infinitely Thin object, xz-plane Resistor 1 ohm
L 1 1 3 3 6 8 250000 -2 -2
L 1 1 3 3 9 9 250000 -2 -2
*Infinitely Thin object, xz-plane Resistor 12k ohms
L 18 20 4 4 2 2 -2 -2 20.8333
L 21 21 4 4 2 2 -2 -2 20.8333
*Infinitely Thin object, xz-plane Resistor 45 ohm x-directed
L 1 1 4 4 16 18 5555.56 -2 -2
L 1 1 4 4 19 19 5555.56 -2 -2
* 1 ps = 600 iterations
*
* Minimum Grid Spacing
A 1e-06
*
*Simulation time (ps) 300
S 210000
*Backup Interval (ps) 200
B 220000
*Plot Interval (ps) 0.1
P 60
*
* A Voltage Source
* A Pulse waveform
* Zero Initial Time 0(ps)
* Rise Time 15(ps)
* On Time 185(ps)
* Fall Time 15(ps)

```

```

* On Voltage -0.7
* Off Voltage 0
*
V P 18 21 4 4 1 1 Z 0 9000 111000 9000 -0.7 0
* A Voltage Source
* A Pulse waveform
* Zero Initial Time 35(ps)
* Rise Time 15(ps)
* On Time 30(ps)
* Fall Time 15(ps)
* On Voltage -0.002
* Off Voltage 0
*
V P 6 9 3 3 1 1 Z 21000 9000 57000 9000 -0.002 0
V P 12 15 3 3 1 1 Z 60000 9000 18000 9000 -0.002 0
*Voltage Paths
W Y 1 3 19 4
W Y 1 2 13 4
W Y 1 2 7 4
W Y 1 2 7 10
W Y 1 3 7 17
W Y 1 3 7 21
*
*Current Loops
J Z 17 21 3 5 4
J Z 11 15 2 4 4
J Z 5 9 2 4 4
J Z 5 9 2 4 10
J X 3 5 15 19 4
J X 2 4 21 25 3
* Variable Mesh Array
* Variable Mesh in the X direction
G X 1 50 1
* Variable Mesh in the Y direction
G Y 1 25 1
* Variable Mesh in the Z direction
G Z 1 50 1

```

B.2 FastHenry Data Set

This is the data set provided to the FastHenry program to determine the values of the two parasitic inductances in the JAWS circuit.

```
* Determination of inductances in the JAWS circuit for
* verification of simulation at home
* Performed on 18 July 1995
* Uses fasthenry
.Units um
* Use a high value for conductivity, Superconductor
.Default nhinc = 1 nwinc = 5 sigma=1.0e20 z=2.5 w=3 h=0.1
* Ground Plane
g1 x1=0 y1=0 z1=0
+ x2=50 y2=0 z2=0
+ x3=50 y3=50 z3=0
+ seg1=20 seg2=20
+ thick=1
* Setup for the system
N1 x=3 y=7
N2 x=24 y=7
N3 x=22.5 y=6
N4 x=22.5 y=2
*Connect the segments
E1 N1 N2
E2 N3 N4
*Make needed electrical connections between segments.
.equiv N2 N3
*Define output
.external N1 N4
.freq fmin=1e9 fmax=1e9 ndec=1
.end
```

B.3 MAPLE V Results

These are the results after using MAPLE V to solve the set of differential equations obtained from nodal analysis in terms of a set of first order derivatives of each variable.

```

> eqn1:=(V1(t)-Va(t))/Rin+(V1(t)-Vb(t))/Rin+Cd*diff(V1(t),t)+V1(t)
> /Rd+I1(t) = 0;

$$eqn1 := \frac{V1(t) - Va(t)}{Rin} + \frac{V1(t) - Vb(t)}{Rin} + Cd \left( \frac{\partial}{\partial t} V1(t) \right) + \frac{V1(t)}{Rd} + I1(t) = 0$$



---


> eqn2:=-I1(t)+Cj*diff(V2(t)-V3(t),t)+G1(V2(t)-V3(t))+Ic1*sin(phi1
> (t))=0;

$$eqn2 := -I1(t) + Cj \left( \left( \frac{\partial}{\partial t} V2(t) \right) - \left( \frac{\partial}{\partial t} V3(t) \right) \right) + G1(V2(t) - V3(t)) + Ic1 \sin(\phi1(t)) = 0$$



---


> eqn3:=(V3(t)-Vso(t))/Rso+Cj*diff(V3(t),t)+G1(V3(t))+Ic2*sin(phi2
> (t))-Cj*diff(V2(t)-V3(t),t)-G1(V2(t)-V3(t))-Ic1*sin(phi1(t))+I2(
> t)=0;

$$eqn3 := \frac{V3(t) - Vso(t)}{Rso} + Cj \left( \frac{\partial}{\partial t} V3(t) \right) + G1(V3(t)) + Ic2 \sin(\phi2(t)) - Cj \left( \left( \frac{\partial}{\partial t} V2(t) \right) - \left( \frac{\partial}{\partial t} V3(t) \right) \right) - G1(V2(t) - V3(t)) - Ic1 \sin(\phi1(t)) + I2(t) = 0$$



---


> eqn4:=-I2(t)+Cout*diff(V4(t),t)+V4(t)/Rout=0;

$$eqn4 := -I2(t) + Cout \left( \frac{\partial}{\partial t} V4(t) \right) + \frac{V4(t)}{Rout} = 0$$



---


> eqn5:=diff(phi1(t),t)=Po*(V2(t)-V3(t));

$$eqn5 := \frac{\partial}{\partial t} \phi1(t) = Po (V2(t) - V3(t))$$



---


> eqn6:=diff(phi2(t),t)=Po*V3(t);

$$eqn6 := \frac{\partial}{\partial t} \phi2(t) = Po V3(t)$$



---


> eqn7:=V1(t)-V2(t) = L1*diff(I1(t),t);

$$eqn7 := V1(t) - V2(t) = L1 \left( \frac{\partial}{\partial t} I1(t) \right)$$



---


> eqn8:=V3(t)-V4(t) = L2*diff(I2(t),t);

$$eqn8 := V3(t) - V4(t) = L2 \left( \frac{\partial}{\partial t} I2(t) \right)$$



---


> ans:=solve({eqn1,eqn2,eqn3,eqn4,eqn5,eqn6,eqn7,eqn8},{diff(V1(t),
> t),diff(V2(t),t),diff(V3(t),t),diff(V4(t),t),diff(I1(t),t),diff
> (I2(t),t),diff(phi1(t),t),diff(phi2(t),t))});

$$ans := \left\{ \frac{\partial}{\partial t} \phi1(t) = Po (V2(t) - V3(t)), \frac{\partial}{\partial t} \phi2(t) = Po V3(t), \right.$$


$$\frac{\partial}{\partial t} V1(t) = - \frac{2 Rd V1(t) - Rd Va(t) - Rd Vb(t) + V1(t) Rin + I1(t) Rin Rd}{Cd Rin Rd}, \frac{\partial}{\partial t} V2(t) = - ($$


$$-2 I1(t) Rso + V3(t) - Vso(t) + G1(V3(t)) Rso + Ic2 \sin(\phi2(t)) Rso + I2(t) Rso$$


$$+ G1(V2(t) - V3(t)) Rso + Ic1 \sin(\phi1(t)) Rso) / (Cj Rso), \frac{\partial}{\partial t} V3(t) =$$


$$\frac{-I1(t) Rso + V3(t) - Vso(t) + G1(V3(t)) Rso + Ic2 \sin(\phi2(t)) Rso + I2(t) Rso}{Cj Rso},$$


```

$$\left. \begin{aligned} \frac{\partial}{\partial t} V4(t) &= \frac{I2(t) Rout - V4(t)}{Cout Rout}, \frac{\partial}{\partial t} I1(t) = -\frac{-V1(t) + V2(t)}{L1}, \frac{\partial}{\partial t} I2(t) = \frac{V3(t) - V4(t)}{L2} \end{aligned} \right\}$$

> ans[1]:

$$\frac{\partial}{\partial t} \text{phi1}(t) = Po (V2(t) - V3(t))$$

> ans[2]:

$$\frac{\partial}{\partial t} \text{phi2}(t) = Po V3(t)$$

> ans[3]:

$$\frac{\partial}{\partial t} V1(t) = -\frac{2 Rd V1(t) - Rd Va(t) - Rd Vb(t) + V1(t) Rin + I1(t) Rin Rd}{Cd Rin Rd}$$

> ans[4]:

$$\begin{aligned} \frac{\partial}{\partial t} V2(t) &= -(-2 I1(t) Rso + V3(t) - Vso(t) + G1(V3(t)) Rso + Ic2 \sin(\text{phi2}(t)) Rso \\ &\quad + I2(t) Rso + G1(V2(t) - V3(t)) Rso + Ic1 \sin(\text{phi1}(t)) Rso) / (Cj Rso) \end{aligned}$$

> ans[5]:

$$\frac{\partial}{\partial t} V3(t) = -\frac{-I1(t) Rso + V3(t) - Vso(t) + G1(V3(t)) Rso + Ic2 \sin(\text{phi2}(t)) Rso + I2(t) Rso}{Cj Rso}$$

> ans[6]:

$$\frac{\partial}{\partial t} V4(t) = \frac{I2(t) Rout - V4(t)}{Cout Rout}$$

> ans[7]:

$$\frac{\partial}{\partial t} I1(t) = -\frac{-V1(t) + V2(t)}{L1}$$

> ans[8]:

$$\frac{\partial}{\partial t} I2(t) = \frac{V3(t) - V4(t)}{L2}$$

>

B.4 C Code

This is a portion of the C Code used to solve the set of first order differential equations provided by MAPLE using the Runge-Kutta fifth-order method. Conventional circuit simulation results are then obtained.

```
#include "nrutil.c"
#include "odeint.c"
#include "rkqs.c"
#include "rkck.c"
#include "linint.c"

#define NOVAR 8
#define Ic1 0.7e-4
#define Ic2 1.0e-4
#define Po 3.039e15
#define Cd 0.292e-15
#define Cout 0.327e-15
#define L1 7.0e-12
#define L2 18.00e-12
#define Cj1 7.0e-13
#define Cj2 7.0e-13
#define Cj 5.0e-13
#define Rd 1.0
#define Rso 12.0e3
#define Rin 45.0
#define Rout 45.0
#define Rl 45.0
#define PI 3.141592763
#define SIMTIM 350.0e-12
#define EPS 1.0e-2

int kmax=1200,kount;
float *xp,**yp,dxsav=3.0e-13;

float G1(float v)
{
    float g1=4e-3;
    float g2=0.1;
    float i1=0.0;
    float vs=2e-3;
    float vt=0.1e-3;
    float ans;

    ans = g1*v + (i1 + g2*fabs(v))*((1/(1+exp((vs-v)/vt))))
```

```

                                -(1/(1+exp((vs+v)/vt))));

    return ans;
}

float Vso(float t)
{
    float starttime = 0.0e-12;
    float risetime = 15.0e-12;
    float ontime = 185.0e-12;
    float falltime = 15.0e-12;
    float hicur = 0.7;

    if (t <= starttime)
        return 0.0;
    if ((t > starttime) && (t <= starttime + risetime))
        return (t - starttime) * hicur / risetime;
    if ((t > starttime + risetime) && (t <= starttime + risetime + ontime))
        return hicur;
    if ((t > starttime + risetime + ontime) && (t <= starttime
        + risetime + ontime + falltime))
        return (hicur - (t - (starttime + risetime + ontime))
        * hicur / falltime);
    else
        return 0.0;
}

float Va(float t)
{
    float starttime = 35.0e-12;
    float risetime = 15.0e-12;
    float ontime = 95.0e-12;
    float falltime = 15.0e-12;
    float hicur = 2.0e-3;

    if (t <= starttime)
        return 0.0;
    if ((t > starttime) && (t <= starttime + risetime))
        return (t - starttime) * hicur / risetime;
    if ((t > starttime + risetime) && (t <= starttime + risetime + ontime))
        return hicur;
    if ((t > starttime + risetime + ontime) && (t <= starttime + risetime + ontime
        + falltime))
        return (hicur - (t - (starttime + risetime + ontime))
        * hicur / falltime);
    else
        return 0.0;
}

float Vb(float t)
{
    float starttime = 100.0e-12;

```

```

float risetime = 15.0e-12;
float ontime = 30.0e-12;
float falltime = 15.0e-12;
float hicur = 2.0e-3;

if (t <= starttime)
    return 0.0;
if ((t > starttime) && (t <= starttime + risetime))
    return (t - starttime) * hicur / risetime;
if ((t > starttime + risetime) && (t <= starttime + risetime + ontime))
    return hicur;
if ((t > starttime + risetime + ontime) && (t <= starttime + risetime + ontime
    + falltime))
    return (hicur - (t - (starttime + risetime + ontime))
        * hicur / falltime);
else
    return 0.0;
}

```

```

void derive(float t, float yv[], float dydt[])
{
    int i;
    /* In this new system, the following variables apply:
    yv[1]=V1(t);
    yv[2]=V2(t);
    yv[3]=phi1(t);
    yv[3]=phi2(t);

    */

    float G1(float v);

    float Vso(float t);
    float Va(float t);
    float Vb(float t);

    /* The following set of equations include two inductors, one
    at the output in order to see if we can reduce oscillation
    magnitude in the output when the circuit is in HVS

    yv[1] = V1(t)
    yv[2] = V2(t)
    yv[3] = V3(t)
    yv[4] = V4(t)
    yv[5] = I1(t)
    yv[6] = I2(t)
    yv[7] = phi1(t)

```

```

        yv[8] = phi2(t)

    */

    dydt[1] = -(2.*Rd*yv[1]-Rd*Va(t)-Rd*Vb(t)+yv[1]*Rin
        +yv[5]*Rin*Rd)/(Cd*Rin*Rd);

    dydt[2] = -(-2.*yv[5]*Rso+yv[3]-Vso(t)+G1(yv[3])*Rso
        +Ic2*sin(yv[8])*Rso
        +yv[6]*Rso+G1(yv[2]-yv[3])*Rso+Ic1*sin(yv[7])*Rso)
        /(Cj*Rso);

    dydt[3] = -(-yv[5]*Rso+yv[3]-Vso(t)+G1(yv[3])*Rso+Ic2*sin(yv[8])*Rso
        +yv[6]*Rso)/(Cj*Rso);

    dydt[4] = (yv[6]*Rout-yv[4])/(Cout*Rout);

    dydt[5] = -(-yv[1]+yv[2])/L1;

    dydt[6] = (yv[3]-yv[4])/L2;

    dydt[7] = Po*(yv[2]-yv[3]);

    dydt[8] = Po*yv[3];

}

int main(){
    FILE *file;
    float *vstart;
    float result;
    int i;
    int nok, nbad;
    float ts;
    /* This next simulation will simulate the MVTLM circuit. Simulation
    will be performed with this system followed by simulation with the
    FDTLM method.

    The following configurations will be used.

    We shall drive a current through the system that is just under the
    maximum critical current of 2.0e-4 amps. We will then
    apply a control current to the control circuitry linked
    to our JJ's through the inductance L. This should alter
    the configuration of the system and create a HVS.

```

We shall analyze the input current, the currents through each JJ, and the voltage across each JJ to determine what state the system is in!

Later models will add the output resistance to shunt the current along with an input current through a voltage and a resistor. An inductance will be used later to model effects of the loop and its self inductance.

We want to see what the basic operation of the SQUID should be*/

```

printf("Allocating memory..\n");
xp = vector(1,kmax);
yp = matrix(1,NOVAR,1,kmax);
vstart = vector(1,NOVAR);

/*Clear the Matrices*/
printf("Clearing memory\n");
for(i=1;i<=NOVAR;i++){
    vstart[i]=0.0;
}
printf("Performing Runge Kutta 5th order adaptive integration.\n");
odeint(vstart,NOVAR,0.0,SIMTIM,EPS,1.0e-13,HMIN,&nok,
    &nbad,derive,rkqs);
printf("nok= %d nbad= %d\n",nok,nbad);
printf("Memory allocated = %fK\n", (kmax*NOVAR*sizeof(float)
    +kmax*sizeof(float))/1000.0);

printf("Simulation over, calculating and printing results\n");

/*Print Va results*/
file=fopen("jrcjlva.dat","w");
for(ts=0.0;ts<=SIMTIM;ts+=1.0e-13)
    fprintf(file,"%g %g\n",ts,Va(ts));
fclose(file);

/*Print Vb results*/
file=fopen("jrcjlvb.dat","w");
for(ts=0.0;ts<=SIMTIM;ts+=1.0e-13)
    fprintf(file,"%g %g\n",ts,Vb(ts));
fclose(file);

/*Print output results V1*/
file=fopen("jrcjlv1.dat","w");
for(i=1;i<=kount;i++)
    fprintf(file,"%g\n",yp[i][i]);

```

```

fclose(file);

    /*Print out the output current*/
    printf("Interpolating: Output current\n");
    file=fopen("jrcjlv2.dat","w");
    for(ts=0.0;ts<=SIMTIM;ts+=1.0e-13){
        linint(&xp[1],&yp[4][1],kount,ts,&result);
        fprintf(file,"%g %g\n",ts,result);
    }
    fclose(file);

    /*Print out the Vso*/
    file=fopen("jrcjlvo.dat","w");
    for(ts=0;ts<=SIMTIM;ts+=1.0e-13)
        fprintf(file,"%g %g\n",ts,Vso(ts));
    fclose(file);

    /*Print source current*/
    file=fopen("jrcjlcin.dat","w");
    for(i=1;i<=kount;i++)
        fprintf(file,"%g\n", (Vso(xp[i])-yp[2][i])/Rso);
    fclose(file);

    /*Print the time scale */
    file = fopen("timescal.dat","w");
    for(i=1;i<=kount;i++)
        fprintf(file,"%g\n",xp[i]);
    fclose(file);

    /*Determine shunted current*/

    printf("Done.....\n");

    return(0);
}

```

Appendix C

2 JJ DC SQUID Simulation Data

The section contains the FD-TLM Data Set, the *FastHenry* extraction data set, MAPLE V results, and the C program for performing the conventional circuit simulation for the 2 JJ DC SQUID circuit.

C.1 FD-TLM Data Set

```
NDATATEST
T 2 JJ Squid Simulation 8/7/95
*Generated by FDTGRAPH, copyright 1993, by Christopher G. Sentelle
*Data in format to be used by FD-TLM copyright by Dr. Robert H. Voelker
*University of Nebraska-Lincoln
*
*
*Created on: Mon Aug 7 14:42:20 1995
*Medium material used throughout
*Relative permittivity
E 1 50 1 50 1 50 1 1 1
*Conductivity throughout
L 1 50 1 50 1 50 0 0 0
*Magnetic susceptibility
M 1 50 1 50 1 50 0 0 0
*Relative permeability
U 1 50 1 50 1 50 1 1 1
*Add a SiO2 Substrate or Ground Plane Insulator
E 1 50 1 3 1 50 3.5 3.5
* Josephson Junction #1
R 11 15 3 4 8 3.039e+15 0.0001 0.004 0 0.1 0.002 0.0001 5e-13 5e-11
* Josephson Junction #2
R 11 15 3 25 29 3.039e+15 0.0001 0.004 0 0.1 0.002 0.0001 5e-13 5e-11
* Coupling device
```

```

H 10 18 4 9 24 1 2
*3 dimensional object, Superconductor
L 5 9 4 4 4 29 -1 -1 -1
*Top Surface
L 5 9 5 5 4 29 -1 -2 -1
L 10 10 5 5 4 29 -2 -2 -1
L 5 9 5 5 30 30 -1 -2 -2
*Right Side Surface
L 5 9 4 4 30 30 -1 -1 -2
L 10 10 4 4 30 30 -2 -1 -2
*Back Side Surface
L 10 10 4 4 4 29 -2 -1 -1
*3 dimensional object, Superconductor
L 10 15 4 4 25 29 -1 -1 -1
*Top Surface
L 10 15 5 5 25 29 -1 -2 -1
L 16 16 5 5 25 29 -2 -2 -1
L 10 15 5 5 30 30 -1 -2 -2
*Right Side Surface
L 10 15 4 4 30 30 -1 -1 -2
L 16 16 4 4 30 30 -2 -1 -2
*Back Side Surface
L 16 16 4 4 25 29 -2 -1 -1
*3 dimensional object, Superconductor
L 10 15 4 4 4 8 -1 -1 -1
*Top Surface
L 10 15 5 5 4 8 -1 -2 -1
L 16 16 5 5 4 8 -2 -2 -1
L 10 15 5 5 9 9 -1 -2 -2
*Right Side Surface
L 10 15 4 4 9 9 -1 -1 -2
L 16 16 4 4 9 9 -2 -1 -2
*Back Side Surface
L 16 16 4 4 4 8 -2 -1 -1
*3 dimensional object, Superconductor
L 17 22 4 4 25 29 -1 -1 -1
*Top Surface
L 17 22 5 5 25 29 -1 -2 -1
L 23 23 5 5 25 29 -2 -2 -1
L 17 22 5 5 30 30 -1 -2 -2
*Right Side Surface
L 17 22 4 4 30 30 -1 -1 -2
L 23 23 4 4 30 30 -2 -1 -2
*Back Side Surface
L 23 23 4 4 25 29 -2 -1 -1
*3 dimensional object, Superconductor
L 17 22 4 4 4 8 -1 -1 -1
*Top Surface
L 17 22 5 5 4 8 -1 -2 -1
L 23 23 5 5 4 8 -2 -2 -1
L 17 22 5 5 9 9 -1 -2 -2

```

```

*Right Side Surface
L 17 22 4 4 9 9 -1 -1 -2
L 23 23 4 4 9 9 -2 -1 -2
*Back Side Surface
L 23 23 4 4 4 8 -2 -1 -1
*3 dimensional object, Superconductor
L 19 22 4 4 9 24 -1 -1 -1
*Top Surface
L 19 22 5 5 9 24 -1 -2 -1
L 23 23 5 5 9 24 -2 -2 -1
L 19 22 5 5 25 25 -1 -2 -2
*Right Side Surface
L 19 22 4 4 25 25 -1 -1 -2
L 23 23 4 4 25 25 -2 -1 -2
*Back Side Surface
L 23 23 4 4 9 24 -2 -1 -1
*3 dimensional object, Superconductor
L 11 18 2 2 4 8 -1 -1 -1
*Top Surface
L 11 18 3 3 4 8 -1 -2 -1
L 19 19 3 3 4 8 -2 -2 -1
L 11 18 3 3 9 9 -1 -2 -2
*Right Side Surface
L 11 18 2 2 9 9 -1 -1 -2
L 19 19 2 2 9 9 -2 -1 -2
*Back Side Surface
L 19 19 2 2 4 8 -2 -1 -1
*3 dimensional object, Superconductor
L 11 18 2 2 25 29 -1 -1 -1
*Top Surface
L 11 18 3 3 25 29 -1 -2 -1
L 19 19 3 3 25 29 -2 -2 -1
L 11 18 3 3 30 30 -1 -2 -2
*Right Side Surface
L 11 18 2 2 30 30 -1 -1 -2
L 19 19 2 2 30 30 -2 -1 -2
*Back Side Surface
L 19 19 2 2 25 29 -2 -1 -1
*3 dimensional object, Superconductor
L 17 18 3 3 4 8 -1 -1 -1
*Top Surface
L 17 18 4 4 4 8 -1 -2 -1
L 19 19 4 4 4 8 -2 -2 -1
L 17 18 4 4 9 9 -1 -2 -2
*Right Side Surface
L 17 18 3 3 9 9 -1 -1 -2
L 19 19 3 3 9 9 -2 -1 -2
*Back Side Surface
L 19 19 3 3 4 8 -2 -1 -1
*3 dimensional object, Superconductor
L 17 18 3 3 25 29 -1 -1 -1

```

*Top Surface

L 17 18 4 4 25 29 -1 -2 -1

L 19 19 4 4 25 29 -2 -2 -1

L 17 18 4 4 30 30 -1 -2 -2

*Right Side Surface

L 17 18 3 3 30 30 -1 -1 -2

L 19 19 3 3 30 30 -2 -1 -2

*Back Side Surface

L 19 19 3 3 25 29 -2 -1 -1

*3 dimensional object, Superconductor

L 1 4 4 4 15 17 -1 -1 -1

*Top Surface

L 1 4 5 5 15 17 -1 -2 -1

L 5 5 5 5 15 17 -2 -2 -1

L 1 4 5 5 18 18 -1 -2 -2

*Right Side Surface

L 1 4 4 4 18 18 -1 -1 -2

L 5 5 4 4 18 18 -2 -1 -2

*Back Side Surface

L 5 5 4 4 15 17 -2 -1 -1

*3 dimensional object, Superconductor

L 23 34 4 4 11 22 -1 -1 -1

*Top Surface

L 23 34 5 5 11 22 -1 -2 -1

L 35 35 5 5 11 22 -2 -2 -1

L 23 34 5 5 23 23 -1 -2 -2

*Right Side Surface

L 23 34 4 4 23 23 -1 -1 -2

L 35 35 4 4 23 23 -2 -1 -2

*Back Side Surface

L 35 35 4 4 11 22 -2 -1 -1

*3 dimensional object, Superconductor

L 30 34 4 4 3 10 -1 -1 -1

*Top Surface

L 30 34 5 5 3 10 -1 -2 -1

L 35 35 5 5 3 10 -2 -2 -1

L 30 34 5 5 11 11 -1 -2 -2

*Right Side Surface

L 30 34 4 4 11 11 -1 -1 -2

L 35 35 4 4 11 11 -2 -1 -2

*Back Side Surface

L 35 35 4 4 3 10 -2 -1 -1

*3 dimensional object, Superconductor

L 35 49 4 4 14 22 -1 -1 -1

*Top Surface

L 35 49 5 5 14 22 -1 -2 -1

L 50 50 5 5 14 22 -2 -2 -1

L 35 49 5 5 23 23 -1 -2 -2

*Right Side Surface

L 35 49 4 4 23 23 -1 -1 -2

L 50 50 4 4 23 23 -2 -1 -2

```

*Back Side Surface
L 50 50 4 4 14 22 -2 -1 -1
*3 dimensional object, Superconductor
L 19 22 6 6 3 39 -1 -1 -1
*Top Surface
L 19 22 7 7 3 39 -1 -2 -1
L 23 23 7 7 3 39 -2 -2 -1
L 19 22 7 7 40 40 -1 -2 -2
*Right Side Surface
L 19 22 6 6 40 40 -1 -1 -2
L 23 23 6 6 40 40 -2 -1 -2
*Back Side Surface
L 23 23 6 6 3 39 -2 -1 -1
*3 dimensional object, Superconductor
L 2 18 6 6 35 39 -1 -1 -1
*Top Surface
L 2 18 7 7 35 39 -1 -2 -1
L 19 19 7 7 35 39 Back Side Surface
L 35 35 4 4 11 22 -2 -1 -1
*3 dimensional object, Superconductor
L 30 34 4 4 3 10 -1 -1 -1
*Top Surface
L 30 34 5 5 3 10 -1 -2 -1
L 35 35 5 5 3 10 -2 -2 -1
L 30 34 5 5 11 11 -1 -2 -2
*Right Side Surface
L 30 34 4 4 11 11 -1 -1 -2
L 35 35 4 4 11 11 -2 -1 -2
*Back Side Surface
L 35 35 4 4 3 10 -2 -1 -1
*3 dimensional object, Superconductor
L 35 49 4 4 14 22 -1 -1 -1
*Top Surface
L 35 49 5 5 14 22 -1 -2 -1
L 50 50 5 5 14 22 -2 -2 -1
L 35 49 5 5 23 23 -1 -2 -2
*Right Side Surface
L 35 49 4 4 23 23 -1 -1 -2
L 50 50 4 4 23 23 -2 -1 -2
*Back Side Surface
L 50 50 4 4 14 22 -2 -1 -1
*3 dimensional object, Superconductor
L 19 22 6 6 3 39 -1 -1 -1
*Top Surface
L 19 22 7 7 3 39 -1 -2 -1
L 23 23 7 7 3 39 -2 -2 -1
L 19 22 7 7 40 40 -1 -2 -2
*Right Side Surface
L 19 22 6 6 40 40 -1 -1 -2
L 23 23 6 6 40 40 -2 -1 -2
*Back Side Surface

```

```

L 23 23 6 6 3 39 -2 -1 -1
*3 dimensional object, Superconductor
L 2 18 6 6 35 39 -1 -1 -1
*Top Surface
L 2 18 7 7 35 39 -1 -2 -1
L 19 19 7 7 35 39 -2 -2 -1
L 2 18 7 7 40 40 -1 -2 -2
*Right Side Surface
L 2 18 6 6 40 40 -1 -1 -2
L 19 19 6 6 40 40 -2 -1 -2
*Back Side Surface
L 19 19 6 6 35 39 -2 -1 -1
* The following conductivity values were modified to
* inaccuracy of the Fdtgraph program..
*Infinitely Thin object, xz-plane SRC RES 60 OHMS
L 30 34 4 4 2 2 -2 -2 2777.78
L 35 35 4 4 2 2 -2 -2 2777.78
*Infinitely Thin object, xz-plane LOAD RES 16 OHM
L 50 50 4 4 14 22 6250 -2 -2
L 50 50 4 4 23 23 6250 -2 -2
*Infinitely Thin object, xz-plane CNTR SRC RES 16 OHMS
L 19 22 6 6 2 2 -2 -2 12500
L 23 23 6 6 2 2 -2 -2 12500
*Infinitely Thin object, xz-plane CNTR LOAD RES 1 OHM
L 1 1 6 6 35 39 166666.67 -2 -2
L 1 1 6 6 40 40 166666.67 -2 -2
* 1 ps = 600 iterations
*
* Minimum Grid Spacing
A 1e-06
*
*Simulation time (ps) 120
S 111000
*Backup Interval (ps) 130
B 120000
*Plot Interval (ps) 0.1
P 60
*
* A Voltage Source
* A Pulse waveform
* Zero Initial Time 0(ps)
* Rise Time 5(ps)
* On Time 100(ps)
* Fall Time 5(ps)
* On Voltage -0.01
* Off Voltage 0
*
V P 30 35 4 4 1 1 Z 0 3000 60000 3000 -0.01 0
* A Voltage Source
* A Pulse waveform
* Zero Initial Time 40(ps)

```

```
* Rise Time 5(ps)
* On Time 20(ps)
* Fall Time 5(ps)
* On Voltage -0.004
* Off Voltage 0
*
V P 19 23 6 6 1 1 Z 24000 3000 12000 3000 -0.004 0
*Voltage Paths
W Y 1 3 32 5
W Y 1 5 21 4
W Y 1 5 9 37
W Y 1 3 18 6
W Y 1 3 18 27
W Y 1 3 12 6
W Y 1 3 12 27
W Y 1 3 26 16
W Y 1 3 44 18
*
*Current Loops
J Z 29 35 3 5 5
J Z 18 23 5 7 4
J X 5 7 34 40 9
J X 3 5 3 9 18
J X 3 5 24 30 18
J X 3 5 3 9 12
J X 3 5 24 30 12
J X 3 5 10 23 26
J X 3 5 13 23 44
* Variable Mesh Array
* Variable Mesh in the X direction
G X 1 50 1
* Variable Mesh in the Y direction
G Y 1 50 1
* Variable Mesh in the Z direction
G Z 1 50 1
```

C.2 FastHenry Data Set

This is the data set provided to the FastHenry program to determine the values of the two parasitic inductances in the 2 JJ DC SQUID circuit.

```

*Determination of Inductance for Squid Loop
* August 7, 1995 , Christopher Sentelle
* Uses fasthenry
.Units um
* Use a high value for conductivity, Superconductor
.Default nhinc = 1 nwinc = 3 sigma=1.0e20 z=3 w=5 h=1
* Ground Plane
g1 x1=0 y1=0 z1=0
+ x2=55 y2=0 z2=0
+ x3=55 y3=55 z3=0
+ seg1=25 seg2=25
+ thick=1
* Setup for the system
* Squid Loop
N5 x=29.0 y=3.0
N6 x=31.0 y=5.5
N7 x=40.0 y=5.5
N8 x=42.5 y=3.0
N9 x=42.5 y=15.0
N10 x=42.5 y=17.0
N11 x=42.5 y=29.0
N12 x=40.0 y=26.5
N13 x=31.0 y=26.5
N14 x=29.0 y=29.0
N15 x=29.0 y=17.0
N16 x=29.0 y=15.0
* Control Line
N17 x=29.0 y=2.0 z=5.0
N18 x=29.0 y=39.0 z=5.0
N19 x=31.0 y=36.5 z=5.0
N20 x=48.0 y=36.5 z=5.0
*Connect the segments
* Squid Loop
E3 N16 N5 w=4
E4 N6 N7
E5 N8 N9
E6 N10 N11
E7 N12 N13
E8 N14 N15 w=4
* Control Line
E9 N17 N18 w=4
E10 N19 N20
* Added for Mf calculations
E11 N9 N10

```

```
*Make needed electrical connections between segments.  
.equiv N5 N6  
.equiv N7 N8  
.equiv N11 N12  
.equiv N13 N14  
.equiv N18 N19  
*Define output  
*Changed for Mf calculation  
.external N16 N15  
.external N17 N20  
.freq fmin=1e9 fmax=1e9 ndec=1  
.end
```

C.3 MAPLE V Results

These are the results after using MAPLE V to solve the set of differential equations obtained from nodal analysis in terms of a set of first order derivatives of each variable.

> eqn1:=Cj*diff(V1(t),t)+Ic*sin(phi1(t))+G(V1(t))-I1(t)=0;

$$eqn1 := Cj \left(\frac{\partial}{\partial t} V1(t) \right) + Ic \sin(\phi1(t)) + G(V1(t)) - I1(t) = 0$$

> eqn2:=Cj*diff(V2(t),t)+Ic*sin(phi1(t)-2*PI*(Mf*I3(t)+L2*I2(t)-L1*I1(t))/FLo)+G(V2(t))-I2(t)=0;

$$eqn2 := Cj \left(\frac{\partial}{\partial t} V2(t) \right) + Ic \sin \left(\phi1(t) - 2 \frac{\Pi (Mf I3(t) + L2 I2(t) - L1 I1(t))}{FLo} \right) + G(V2(t)) - I2(t) = 0$$

> eqn3:=I1(t)+I2(t)-I4(t)+I5(t)=0;

$$eqn3 := I1(t) + I2(t) - I4(t) + I5(t) = 0$$

> eqn4:=V4(t)/Rcout-I3(t)=0;

$$eqn4 := \frac{V4(t)}{Rcout} - I3(t) = 0$$

> eqn5:=I3(t)+(V5(t)-Vcin(t))/Rcin=0;

$$eqn5 := I3(t) + \frac{V5(t) - Vcin(t)}{Rcin} = 0$$

> eqn6:=I4(t)+(V6(t)-Vso(t))/Rin=0;

$$eqn6 := I4(t) + \frac{V6(t) - Vso(t)}{Rin} = 0$$

> eqn7:=-I5(t)+V7(t)/Rout=0;

$$eqn7 := -I5(t) + \frac{V7(t)}{Rout} = 0$$

> eqn8:=V3(t)-V1(t)=L1*diff(I1(t),t)-M1*diff(I3(t),t);

$$eqn8 := V3(t) - V1(t) = L1 \left(\frac{\partial}{\partial t} I1(t) \right) - M1 \left(\frac{\partial}{\partial t} I3(t) \right)$$

> eqn9:=V3(t)-V2(t)=L2*diff(I2(t),t)+M2*diff(I3(t),t);

$$eqn9 := V3(t) - V2(t) = L2 \left(\frac{\partial}{\partial t} I2(t) \right) + M2 \left(\frac{\partial}{\partial t} I3(t) \right)$$

> eqn10:=V5(t)-V4(t)=L3*diff(I3(t),t)-M1*diff(I1(t),t)+M2*diff(I2(t),t);

$$eqn10 := V5(t) - V4(t) = L3 \left(\frac{\partial}{\partial t} I3(t) \right) - M1 \left(\frac{\partial}{\partial t} I1(t) \right) + M2 \left(\frac{\partial}{\partial t} I2(t) \right)$$

> eqn11:=V6(t)-V3(t)=L4*diff(I4(t),t);

$$eqn11 := V6(t) - V3(t) = L4 \left(\frac{\partial}{\partial t} I4(t) \right)$$

> eqn12:=V3(t)-V7(t)=L5*diff(I5(t),t);

$$eqn12 := V3(t) - V7(t) = L5 \left(\frac{\partial}{\partial t} I5(t) \right)$$

> eqn13:=diff(phi1(t),t)=Po*V1(t);

$$eqn13 := \frac{\partial}{\partial t} \phi1(t) = Po V1(t)$$

```

> eqn10a:=subs({V5(t)=solve(eqn5,V5(t)),V4(t)=solve(eqn4,V4(t))},e
> qn10);
eqn10a:=

$$\left( I3(t) - \frac{Vcin(t)}{Rcin} \right) Rcin - I3(t) Rcout = L3 \left( \frac{\partial}{\partial t} I3(t) \right) - M1 \left( \frac{\partial}{\partial t} I1(t) \right) + M2 \left( \frac{\partial}{\partial t} I2(t) \right)$$

> eqn11a:=subs(V6(t)=solve(eqn6,V6(t)),eqn11);
eqn11a:=

$$\left( I4(t) - \frac{Vso(t)}{Rin} \right) Rin - V3(t) = L4 \left( \frac{\partial}{\partial t} I4(t) \right)$$

> eqn12a:=subs(V7(t)=solve(eqn7,V7(t)),eqn12);
eqn12a:=

$$V3(t) - I5(t) Rout = L5 \left( \frac{\partial}{\partial t} I5(t) \right)$$

> eqn1:

$$Cj \left( \frac{\partial}{\partial t} V1(t) \right) + Ic \sin(\text{phil}(t)) + G(V1(t)) - I1(t) = 0$$

> eqn2:

$$Cj \left( \frac{\partial}{\partial t} V2(t) \right) + Ic \sin \left( \text{phil}(t) - 2 \frac{\Pi (Mf I3(t) + L2 I2(t) - L1 I1(t))}{FLo} \right) + G(V2(t)) - I2(t) = 0$$

> eqn3:

$$I1(t) + I2(t) - I4(t) + I5(t) = 0$$

> eqn8:

$$V3(t) - V1(t) = L1 \left( \frac{\partial}{\partial t} I1(t) \right) - M1 \left( \frac{\partial}{\partial t} I3(t) \right)$$

> eqn9:

$$V3(t) - V2(t) = L2 \left( \frac{\partial}{\partial t} I2(t) \right) + M2 \left( \frac{\partial}{\partial t} I3(t) \right)$$

> eqn10a:

$$\left( I3(t) - \frac{Vcin(t)}{Rcin} \right) Rcin - I3(t) Rcout = L3 \left( \frac{\partial}{\partial t} I3(t) \right) - M1 \left( \frac{\partial}{\partial t} I1(t) \right) + M2 \left( \frac{\partial}{\partial t} I2(t) \right)$$

> eqn11a:

$$\left( I4(t) - \frac{Vso(t)}{Rin} \right) Rin - V3(t) = L4 \left( \frac{\partial}{\partial t} I4(t) \right)$$

> eqn12a:

$$V3(t) - I5(t) Rout = L5 \left( \frac{\partial}{\partial t} I5(t) \right)$$

> eqn8a:=subs(V3(t)=solve(eqn12a,V3(t)),eqn8);
eqn8a:=

$$I5(t) Rout + L5 \left( \frac{\partial}{\partial t} I5(t) \right) - V1(t) = L1 \left( \frac{\partial}{\partial t} I1(t) \right) - M1 \left( \frac{\partial}{\partial t} I3(t) \right)$$

> eqn9a:=subs(V3(t)=solve(eqn12a,V3(t)),eqn9);
eqn9a:=

$$I5(t) Rout + L5 \left( \frac{\partial}{\partial t} I5(t) \right) - V2(t) = L2 \left( \frac{\partial}{\partial t} I2(t) \right) + M2 \left( \frac{\partial}{\partial t} I3(t) \right)$$

> eqn11b:=subs(V3(t)=solve(eqn12a,V3(t)),eqn11a);

```

$$\text{eqn11b} := -\left(I4(t) - \frac{Vso(t)}{Rin}\right) Rin - I5(t) Rout - L5 \left(\frac{\partial}{\partial t} I5(t)\right) = L4 \left(\frac{\partial}{\partial t} I4(t)\right)$$

> eqn1;

$$Cj \left(\frac{\partial}{\partial t} V1(t)\right) + Ic \sin(\text{phil}(t)) + G(V1(t)) - I1(t) = 0$$

> eqn2;

$$Cj \left(\frac{\partial}{\partial t} V2(t)\right) + Ic \sin\left(\text{phil}(t) - 2 \frac{\Pi (Mf I3(t) + L2 I2(t) - L1 I1(t))}{FLo}\right) + G(V2(t)) - I2(t) = 0$$

> eqn3;

$$I1(t) + I2(t) - I4(t) + I5(t) = 0$$

> eqn8a;

$$I5(t) Rout + L5 \left(\frac{\partial}{\partial t} I5(t)\right) - V1(t) = L1 \left(\frac{\partial}{\partial t} I1(t)\right) - M1 \left(\frac{\partial}{\partial t} I3(t)\right)$$

> eqn9a;

$$I5(t) Rout + L5 \left(\frac{\partial}{\partial t} I5(t)\right) - V2(t) = L2 \left(\frac{\partial}{\partial t} I2(t)\right) + M2 \left(\frac{\partial}{\partial t} I3(t)\right)$$

> eqn10a;

$$-\left(I3(t) - \frac{Vcin(t)}{Rcin}\right) Rcin - I3(t) Rcout = L3 \left(\frac{\partial}{\partial t} I3(t)\right) - M1 \left(\frac{\partial}{\partial t} I1(t)\right) + M2 \left(\frac{\partial}{\partial t} I2(t)\right)$$

> eqn11b;

$$-\left(I4(t) - \frac{Vso(t)}{Rin}\right) Rin - I5(t) Rout - L5 \left(\frac{\partial}{\partial t} I5(t)\right) = L4 \left(\frac{\partial}{\partial t} I4(t)\right)$$

> eqn11c:=subs(I4(t)=solve(eqn3, I4(t)), eqn11b);

$$\text{eqn11c} := -\left(I1(t) + I2(t) + I5(t) - \frac{Vso(t)}{Rin}\right) Rin - I5(t) Rout - L5 \left(\frac{\partial}{\partial t} I5(t)\right) = L4 \left(\frac{\partial}{\partial t} I1(t) + I2(t) + I5(t)\right)$$

> eqn1;

$$Cj \left(\frac{\partial}{\partial t} V1(t)\right) + Ic \sin(\text{phil}(t)) + G(V1(t)) - I1(t) = 0$$

> eqn2;

$$Cj \left(\frac{\partial}{\partial t} V2(t)\right) + Ic \sin\left(\text{phil}(t) - 2 \frac{\Pi (Mf I3(t) + L2 I2(t) - L1 I1(t))}{FLo}\right) + G(V2(t)) - I2(t) = 0$$

> eqn8a;

$$I5(t) Rout + L5 \left(\frac{\partial}{\partial t} I5(t)\right) - V1(t) = L1 \left(\frac{\partial}{\partial t} I1(t)\right) - M1 \left(\frac{\partial}{\partial t} I3(t)\right)$$

> eqn9a;

$$I5(t) Rout + L5 \left(\frac{\partial}{\partial t} I5(t)\right) - V2(t) = L2 \left(\frac{\partial}{\partial t} I2(t)\right) + M2 \left(\frac{\partial}{\partial t} I3(t)\right)$$

> eqn10a;

$$\left(I_3(t) - \frac{V_{cin}(t)}{R_{cin}} \right) R_{cin} - I_3(t) R_{cout} = L_3 \left(\frac{\partial}{\partial t} I_3(t) \right) - M_1 \left(\frac{\partial}{\partial t} I_1(t) \right) + M_2 \left(\frac{\partial}{\partial t} I_2(t) \right)$$

> eqn11c;

$$\left(I_1(t) + I_2(t) + I_5(t) - \frac{V_{so}(t)}{R_{in}} \right) R_{in} - I_5(t) R_{out} - L_5 \left(\frac{\partial}{\partial t} I_5(t) \right) =$$

$$L_4 \left(\left(\frac{\partial}{\partial t} I_1(t) \right) + \left(\frac{\partial}{\partial t} I_2(t) \right) + \left(\frac{\partial}{\partial t} I_5(t) \right) \right)$$

> eqn13;

$$\frac{\partial}{\partial t} \text{phil}(t) = P_o V_1(t)$$

> ans:=solve({eqn1,eqn2,eqn8a,eqn9a,eqn10a,eqn11c,eqn13},{diff(V1(t),t),diff(V2(t),t),diff(I1(t),t),diff(I2(t),t),diff(I3(t),t),diff(I5(t),t),diff(phil(t),t))});

$$\text{ans} := \left\{ \begin{array}{l} \frac{\partial}{\partial t} \text{phil}(t) = P_o V_1(t), \frac{\partial}{\partial t} V_2(t) = \\ I_c \sin \left(\frac{-\text{phil}(t) F_{Lo} + 2 \Pi M_f I_3(t) + 2 \Pi L_2 I_2(t) - 2 \Pi L_1 I_1(t)}{F_{Lo}} \right) - G(V_2(t)) + I_2(t) \\ C_j \end{array} \right.$$

$$\frac{\partial}{\partial t} I_1(t) = \left(V_{so}(t) M_2^2 L_5 + L_5 L_4 M_2 I_3(t) R_{cout} - L_4 V_2(t) L_3 L_5 - L_5 L_4 M_2 V_{cin}(t) \right.$$

$$+ L_5 L_4 L_3 V_1(t) + L_5 L_4 M_2 I_3(t) R_{cin} + M_1 L_5 L_4 I_3(t) R_{cin} + M_1 L_5 L_4 I_3(t) R_{cout}$$

$$- M_1 L_5 M_2 I_1(t) R_{in} + M_1 L_5 M_2 V_{so}(t) - M_1 L_5 M_2 I_5(t) R_{in} - M_1 L_5 M_2 I_2(t) R_{in}$$

$$- M_1 L_5 L_4 V_{cin}(t) - L_5 M_2^2 V_1(t) + I_5(t) R_{in} L_3 L_5 L_2 + L_5 L_3 V_1(t) L_2$$

$$- I_1(t) R_{in} M_2^2 L_5 + I_1(t) R_{in} L_3 L_5 L_2 - I_2(t) R_{in} M_2^2 L_5 + L_5 I_3(t) R_{cout} M_1 L_2$$

$$+ L_5 I_3(t) R_{cin} M_1 L_2 - L_5 M_2 M_1 V_2(t) - L_5 V_{cin}(t) M_1 L_2 - V_{so}(t) L_3 L_5 L_2$$

$$+ I_2(t) R_{in} L_3 L_5 L_2 - I_5(t) R_{in} M_2^2 L_5 + M_1 L_4 M_2 I_5(t) R_{out} - M_2^2 L_4 V_1(t)$$

$$- M_2 M_1 L_4 V_2(t) + M_2^2 L_4 I_5(t) R_{out} + L_4 I_3(t) R_{cin} M_1 L_2 - L_4 V_{cin}(t) M_1 L_2$$

$$+ L_4 I_3(t) R_{cout} M_1 L_2 - L_4 L_3 I_5(t) R_{out} L_2 + L_4 L_3 V_1(t) L_2 \Big) / (\%1), \frac{\partial}{\partial t} I_3(t) = - \left(\right.$$

$$- L_5 L_4 I_3(t) R_{cout} L_2 - L_5 L_4 I_3(t) R_{cin} L_2 + M_2 L_1 L_5 V_2(t) - M_2 L_1 V_{so}(t) L_5$$

$$+ L_5 L_4 V_{cin}(t) L_2 + M_2 L_1 I_2(t) R_{in} L_5 + M_2 L_1 I_5(t) R_{in} L_5 + M_2 L_1 I_1(t) R_{in} L_5$$

$$- M_2 L_1 L_4 I_5(t) R_{out} + M_2 L_1 L_4 V_2(t) + L_4 M_1 I_5(t) R_{out} L_2 + L_5 M_1 V_{so}(t) L_2$$

$$+ L_5 M_2 L_4 V_2(t) - L_5 M_1 I_1(t) R_{in} L_2 - L_5 M_1 I_5(t) R_{in} L_2 + L_1 L_5 L_4 V_{cin}(t)$$

$$- V_1(t) M_1 L_5 L_2 - V_1(t) M_1 L_4 L_2 - V_1(t) M_1 L_5 L_4 - L_1 L_5 L_4 I_3(t) R_{cin}$$

$$- L_1 L_5 L_4 I_3(t) R_{cout} + L_1 L_4 V_{cin}(t) L_2 - L_1 L_5 I_3(t) R_{cout} L_2 - L_1 L_5 I_3(t) R_{cin} L_2$$

$$+ L_1 L_5 V_{cin}(t) L_2 - L_1 L_4 I_3(t) R_{cout} L_2 - L_1 L_4 I_3(t) R_{cin} L_2 - L_4 M_2 V_1(t) L_5$$

$$+ L_4 M_1 V_2(t) L_5 - L_5 M_1 I_2(t) R_{in} L_2 \Big) / (\%1), \frac{\partial}{\partial t} I_2(t) = \left(M_1^2 L_5 V_{so}(t) \right.$$

$$- M_1^2 V_2(t) L_5 - L_5 L_4 M_2 I_3(t) R_{cout} + L_5 L_3 L_1 I_1(t) R_{in} + L_4 V_2(t) L_3 L_5$$

$$\begin{aligned}
& -L5 L3 L1 V_{so}(t) + L5 L4 M2 V_{cin}(t) + V2(t) L3 L1 L5 + M2 L1 L5 V_{cin}(t) \\
& -L5 L4 L3 V1(t) + L5 L3 L1 I2(t) R_{in} - L5 L4 M2 I3(t) R_{cin} + L5 L3 L1 I5(t) R_{in} \\
& -M2 L1 L5 I3(t) R_{cout} - M2 L1 L5 I3(t) R_{cin} - M1^2 L5 I1(t) R_{in} - M1^2 L5 I2(t) R_{in} \\
& -M1^2 L5 I5(t) R_{in} - M1 L5 L4 I3(t) R_{cin} - M1 L5 L4 I3(t) R_{cout} - M1 L5 M2 I1(t) R_{in} \\
& + M1 L5 M2 V_{so}(t) - M1 L5 M2 I5(t) R_{in} - M1 M2 V1(t) L5 - M1 L5 M2 I2(t) R_{in} \\
& + M1 L5 L4 V_{cin}(t) - M1^2 L4 V2(t) + M1 L4 M2 I5(t) R_{out} + M1^2 L4 I5(t) R_{out} \\
& - M1 L4 M2 V1(t) - L3 L1 L4 I5(t) R_{out} + L3 L1 L4 V2(t) - L4 I3(t) R_{cin} M2 L1 \\
& + L4 V_{cin}(t) M2 L1 - L4 I3(t) R_{cout} M2 L1 \Big) / (\%1), \frac{\partial}{\partial t} I5(t) = \Big(M1^2 L4 V2(t) \\
& - 2 M1 L4 M2 I5(t) R_{out} - M1^2 L4 I5(t) R_{out} + M1^2 V_{so}(t) L2 + M2^2 L1 V_{so}(t) \\
& + M2^2 L4 V1(t) + M1 L4 M2 V1(t) + L3 L1 L4 I5(t) R_{out} - L3 L1 L4 V2(t) \\
& - M2^2 L1 I1(t) R_{in} - M2^2 L1 I2(t) R_{in} - M2^2 L1 I5(t) R_{in} - M2^2 L1 I5(t) R_{out} \\
& + M2 M1 L4 V2(t) - M2^2 L4 I5(t) R_{out} - M1^2 I1(t) R_{in} L2 - M1^2 I2(t) R_{in} L2 \\
& - M1^2 I5(t) R_{in} L2 - M1^2 I5(t) R_{out} L2 + L3 L1 I1(t) R_{in} L2 + L3 L1 I2(t) R_{in} L2 \\
& + L3 L1 I5(t) R_{in} L2 - L3 L1 V_{so}(t) L2 + L3 L1 I5(t) R_{out} L2 + L4 I3(t) R_{cin} M2 L1 \\
& - L4 I3(t) R_{cin} M1 L2 - L4 V_{cin}(t) M2 L1 + L4 V_{cin}(t) M1 L2 + L4 I3(t) R_{cout} M2 L1 \\
& - L4 I3(t) R_{cout} M1 L2 + L4 L3 I5(t) R_{out} L2 - L4 L3 V1(t) L2 \Big) / (\%1), \\
& \left. \frac{\partial}{\partial t} V1(t) = - \frac{I_c \sin(\text{phil}(t)) + G(V1(t)) - I1(t)}{C_j} \right\} \\
& \%1 := M1^2 L5 L4 + 2 M1 L5 L4 M2 - L3 L1 L5 L4 + M2^2 L1 L5 + M2^2 L1 L4 + M2^2 L5 L4 \\
& + M1^2 L5 L2 + M1^2 L4 L2 - L3 L1 L5 L2 - L3 L1 L4 L2 - L3 L5 L4 L2 \\
& > \text{ans}[1]; \\
& \frac{\partial}{\partial t} \text{phil}(t) = P_o V1(t) \\
& > \text{ans}[2]; \\
& \frac{\partial}{\partial t} V2(t) = \\
& \frac{I_c \sin\left(\frac{-\text{phil}(t) FLo + 2 \Pi Mf I3(t) + 2 \Pi L2 I2(t) - 2 \Pi L1 I1(t)}{FLo}\right) - G(V2(t)) + I2(t)}{C_j} \\
& > \text{ans}[3]; \\
& \frac{\partial}{\partial t} I1(t) = \Big(V_{so}(t) M2^2 L5 + L5 L4 M2 I3(t) R_{cout} - L4 V2(t) L3 L5 - L5 L4 M2 V_{cin}(t) \\
& + L5 L4 L3 V1(t) + L5 L4 M2 I3(t) R_{cin} + M1 L5 L4 I3(t) R_{cin} + M1 L5 L4 I3(t) R_{cout} \\
& - M1 L5 M2 I1(t) R_{in} + M1 L5 M2 V_{so}(t) - M1 L5 M2 I5(t) R_{in} - M1 L5 M2 I2(t) R_{in} \\
& - M1 L5 L4 V_{cin}(t) - L5 M2^2 V1(t) + I5(t) R_{in} L3 L5 L2 + L5 L3 V1(t) L2 \\
\end{aligned}$$

$$\begin{aligned}
& -I_1(t) R_{in} M_2^2 L_5 + I_1(t) R_{in} L_3 L_5 L_2 - I_2(t) R_{in} M_2^2 L_5 + L_5 I_3(t) R_{out} M_1 L_2 \\
& + L_5 I_3(t) R_{in} M_1 L_2 - L_5 M_2 M_1 V_2(t) - L_5 V_{cin}(t) M_1 L_2 - V_{so}(t) L_3 L_5 L_2 \\
& + I_2(t) R_{in} L_3 L_5 L_2 - I_5(t) R_{in} M_2^2 L_5 + M_1 L_4 M_2 I_5(t) R_{out} - M_2^2 L_4 V_1(t) \\
& - M_2 M_1 L_4 V_2(t) + M_2^2 L_4 I_5(t) R_{out} + L_4 I_3(t) R_{in} M_1 L_2 - L_4 V_{cin}(t) M_1 L_2 \\
& + L_4 I_3(t) R_{out} M_1 L_2 - L_4 L_3 I_5(t) R_{out} L_2 + L_4 L_3 V_1(t) L_2 \Big/ (M_1^2 L_5 L_4 \\
& + 2 M_1 L_5 L_4 M_2 - L_3 L_1 L_5 L_4 + M_2^2 L_1 L_5 + M_2^2 L_1 L_4 + M_2^2 L_5 L_4 + M_1^2 L_5 L_2 \\
& + M_1^2 L_4 L_2 - L_3 L_1 L_5 L_2 - L_3 L_1 L_4 L_2 - L_3 L_5 L_4 L_2)
\end{aligned}$$

> ans[4]:

$$\begin{aligned}
\frac{\partial}{\partial t} I_3(t) = & -(-L_5 L_4 I_3(t) R_{out} L_2 - L_5 L_4 I_3(t) R_{in} L_2 + M_2 L_1 L_5 V_2(t) \\
& - M_2 L_1 V_{so}(t) L_5 + L_5 L_4 V_{cin}(t) L_2 + M_2 L_1 I_2(t) R_{in} L_5 + M_2 L_1 I_5(t) R_{in} L_5 \\
& + M_2 L_1 I_1(t) R_{in} L_5 - M_2 L_1 L_4 I_5(t) R_{out} + M_2 L_1 L_4 V_2(t) + L_4 M_1 I_5(t) R_{out} L_2 \\
& + L_5 M_1 V_{so}(t) L_2 + L_5 M_2 L_4 V_2(t) - L_5 M_1 I_1(t) R_{in} L_2 - L_5 M_1 I_5(t) R_{in} L_2 \\
& + L_1 L_5 L_4 V_{cin}(t) - V_1(t) M_1 L_5 L_2 - V_1(t) M_1 L_4 L_2 - V_1(t) M_1 L_5 L_4 \\
& - L_1 L_5 L_4 I_3(t) R_{in} - L_1 L_5 L_4 I_3(t) R_{out} + L_1 L_4 V_{cin}(t) L_2 - L_1 L_5 I_3(t) R_{out} L_2 \\
& - L_1 L_5 I_3(t) R_{in} L_2 + L_1 L_5 V_{cin}(t) L_2 - L_1 L_4 I_3(t) R_{out} L_2 - L_1 L_4 I_3(t) R_{in} L_2 \\
& - L_4 M_2 V_1(t) L_5 + L_4 M_1 V_2(t) L_5 - L_5 M_1 I_2(t) R_{in} L_2) \Big/ (M_1^2 L_5 L_4 + 2 M_1 L_5 L_4 M_2 \\
& - L_3 L_1 L_5 L_4 + M_2^2 L_1 L_5 + M_2^2 L_1 L_4 + M_2^2 L_5 L_4 + M_1^2 L_5 L_2 + M_1^2 L_4 L_2 \\
& - L_3 L_1 L_5 L_2 - L_3 L_1 L_4 L_2 - L_3 L_5 L_4 L_2)
\end{aligned}$$

> ans[5]:

$$\begin{aligned}
\frac{\partial}{\partial t} I_2(t) = & (M_1^2 L_5 V_{so}(t) - M_1^2 V_2(t) L_5 - L_5 L_4 M_2 I_3(t) R_{out} + L_5 L_3 L_1 I_1(t) R_{in} \\
& + L_4 V_2(t) L_3 L_5 - L_5 L_3 L_1 V_{so}(t) + L_5 L_4 M_2 V_{cin}(t) + V_2(t) L_3 L_1 L_5 \\
& + M_2 L_1 L_5 V_{cin}(t) - L_5 L_4 L_3 V_1(t) + L_5 L_3 L_1 I_2(t) R_{in} - L_5 L_4 M_2 I_3(t) R_{in} \\
& + L_5 L_3 L_1 I_5(t) R_{in} - M_2 L_1 L_5 I_3(t) R_{out} - M_2 L_1 L_5 I_3(t) R_{in} - M_1^2 L_5 I_1(t) R_{in} \\
& - M_1^2 L_5 I_2(t) R_{in} - M_1^2 L_5 I_5(t) R_{in} - M_1 L_5 L_4 I_3(t) R_{in} - M_1 L_5 L_4 I_3(t) R_{out} \\
& - M_1 L_5 M_2 I_1(t) R_{in} + M_1 L_5 M_2 V_{so}(t) - M_1 L_5 M_2 I_5(t) R_{in} - M_1 M_2 V_1(t) L_5 \\
& - M_1 L_5 M_2 I_2(t) R_{in} + M_1 L_5 L_4 V_{cin}(t) - M_1^2 L_4 V_2(t) + M_1 L_4 M_2 I_5(t) R_{out} \\
& + M_1^2 L_4 I_5(t) R_{out} - M_1 L_4 M_2 V_1(t) - L_3 L_1 L_4 I_5(t) R_{out} + L_3 L_1 L_4 V_2(t) \\
& - L_4 I_3(t) R_{in} M_2 L_1 + L_4 V_{cin}(t) M_2 L_1 - L_4 I_3(t) R_{out} M_2 L_1) \Big/ (M_1^2 L_5 L_4 \\
& + 2 M_1 L_5 L_4 M_2 - L_3 L_1 L_5 L_4 + M_2^2 L_1 L_5 + M_2^2 L_1 L_4 + M_2^2 L_5 L_4 + M_1^2 L_5 L_2 \\
& + M_1^2 L_4 L_2 - L_3 L_1 L_5 L_2 - L_3 L_1 L_4 L_2 - L_3 L_5 L_4 L_2)
\end{aligned}$$

> ans[6]:

$$\frac{\partial}{\partial t} I_5(t) = (M_1^2 L_4 V_2(t) - 2 M_1 L_4 M_2 I_5(t) R_{out} - M_1^2 L_4 I_5(t) R_{out} + M_1^2 V_{so}(t) L_2$$

$$\begin{aligned}
& + M2^2 L1 Vso(t) + M2^2 L4 V1(t) + M1 L4 M2 V1(t) + L3 L1 L4 I5(t) Rout \\
& - L3 L1 L4 V2(t) - M2^2 L1 I1(t) Rin - M2^2 L1 I2(t) Rin - M2^2 L1 I5(t) Rin \\
& - M2^2 L1 I5(t) Rout + M2 M1 L4 V2(t) - M2^2 L4 I5(t) Rout - M1^2 I1(t) Rin L2 \\
& - M1^2 I2(t) Rin L2 - M1^2 I5(t) Rin L2 - M1^2 I5(t) Rout L2 + L3 L1 I1(t) Rin L2 \\
& + L3 L1 I2(t) Rin L2 + L3 L1 I5(t) Rin L2 - L3 L1 Vso(t) L2 + L3 L1 I5(t) Rout L2 \\
& + L4 I3(t) Rcin M2 L1 - L4 I3(t) Rcin M1 L2 - L4 Vcin(t) M2 L1 + L4 Vcin(t) M1 L2 \\
& + L4 I3(t) Rcout M2 L1 - L4 I3(t) Rcout M1 L2 + L4 L3 I5(t) Rout L2 - L4 L3 V1(t) L2 \Big) / \Big(\\
& M1^2 L5 L4 + 2 M1 L5 L4 M2 - L3 L1 L5 L4 + M2^2 L1 L5 + M2^2 L1 L4 + M2^2 L5 L4 \\
& + M1^2 L5 L2 + M1^2 L4 L2 - L3 L1 L5 L2 - L3 L1 L4 L2 - L3 L5 L4 L2 \Big)
\end{aligned}$$

> ans[7]:

$$\frac{\partial}{\partial t} V1(t) = - \frac{Ic \sin(\text{phil}(t)) + G(V1(t)) - I1(t)}{Cj}$$

>

>

C.4 C Code

This is a portion of the C Code used to solve the set of first order differential equations provided by MAPLE using the Runge-Kutta fifth-order method. Conventional circuit simulation results are then obtained.

```
#include "nrutil.c"
#include "odeint.c"
#include "rkqs.c"
#include "rkck.c"

#define NOVAR 6
#define L3 6.0e-12
#define L4 6.0e-12
#define M1 2.0e-12
#define M2 2.0e-12
#define Mf 6.068e-12
#define L1 8.39e-12
#define L2 8.39e-12
#define Ic 1.0e-6
#define G1 4.0e-3
#define I1 0.0
#define G2 0.1
#define Vs 2.0e-3
#define Vt 1.0e-4
#define Io 1.0e-4
#define Po 3.039e15
#define Cj 5.0e-13
#define Rcin 16.0
#define Rcout 1.0
#define Rin 60.0
#define Rout 16.0
#define FLo 2.068e-15
#define PLT 0.1e-12
#define PI 3.141592763
#define SIMTIM 120.0e-12
#define EPS 1.0e-2
```

```
int kmax=1300,kount;
float *xp,**yp,dxsav=1.0e-13;
```

```
float G(float v)
{
    float ans;
```

```

    ans = G1*v + (I1 + G2*fabs(v))*((1/(1+exp((Vs-v)/Vt)))
                                   -(1/(1+exp((Vs+v)/Vt))));
    return ans;
}

float Vso(float t)
{
    float starttime = 0.0e-12;
    float risetime = 5.0e-12;
    float ontime = 100.0e-12;
    float falltime = 5.0e-12;
    float hicur = 0.010;

    if (t <=starttime)
        return 0.0;
    if ((t>starttime) && (t<=starttime+risetime))
        return (t-starttime)*hicur/risetime;
    if ((t>starttime+risetime)&&(t<=starttime+risetime+ontime))
        return hicur;
    if((t>starttime+risetime+ontime)&&(t<=starttime+risetime
        +ontime+falltime))
        return (hicur - (t-(starttime+risetime+ontime))
            *hicur/falltime);
    else
        return 0.0;
}

float Vcin(float t)
{
    float starttime = 25.0e-12;
    float risetime = 5.0e-12;
    float ontime = 20.0e-12;
    float falltime = 5.0e-12;
    float hicur = 0.003;

    if (t <=starttime)
        return 0.0;
    if ((t>starttime) && (t<=starttime+risetime))
        return (t-starttime)*hicur/risetime;
    if ((t>starttime+risetime)&&(t<=starttime+risetime+ontime))
        return hicur;
    if((t>starttime+risetime+ontime)&&(t<=starttime+risetime+ontime
        +falltime))
        return (hicur - (t-(starttime+risetime+ontime))
            *hicur/falltime);
    else
        return 0.0;
}

```

```

void derive(float t, float yv[], float dydt[])
{
    int i;
    /*In this new system, the following variables apply:
        y[1]=V1
        y[2]=V2
        y[3]=I1
        y[4]=I2
        y[5]=phi1
    */
    float G(float v);
    float Vso(float t);
    float Vcin(float t);

    dydt[1]=-(Io*sin(yv[6])+G(yv[1])-yv[3])/Cj;
    dydt[2]=(Io*sin((-yv[6]*FLo+2*PI*(Mf*yv[5]+L2*yv[4]-L1*yv[3]))/FLo)-
        G(yv[2])+yv[4])/Cj;
    dydt[3]=-(M2*M2*Rout*Vso(t)+M2*M1*Rout*Vso(t)-M2*M1*Rout*yv[3]
        *Rin-M2*M1*Rout*yv[4]*Rin-M2*M2*yv[1]*Rin-M2*M2*yv[1]
        *Rout+L3*L2*yv[1]*Rin+L4*L2*Rout*yv[4]*Rin-
        L4*L2*Rout*Vso(t)+L4*L2*Rout*yv[3]*Rin+L4*L2*yv[1]*Rin
        +L4*L2*yv[1]*Rout-L3*L2*Rout*Vso(t)+L3*L2*Rout*yv[3]
        *Rin+L3*L2*Rout*yv[4]*Rin+L3*L2*yv[1]*Rout-M2*M2*Rout
        *yv[3]*Rin-M2*M2*Rout*yv[4]*Rin-M2*M1*yv[2]*Rin
        -M2*M1*yv[2]*Rout-Vcin(t)*L2*M1*Rin-Vcin(t)*L2*M1*Rout
        +yv[5]*Rcout*L2*M1*Rin+yv[5]*Rcout*L2*M1*Rout+yv[5]*Rcin
        *L2*M1*Rin+yv[5]*Rcin*L2*M1*Rout)/
        ((L2*L1*L4+L2*L1*L3-L2*M1*M1-L1*M2*M2)*(Rin+Rout));
    dydt[4]=-(M1*M1*yv[2]*Rin+M1*M1*Rout*Vso(t)-M1*M1*yv[2]*Rout
        +L1*L4*Rout*yv[3]*Rin-L1*L4*Rout*Vso(t)+L1*L4*Rout*yv[4]
        *Rin+L1*L4*yv[2]*Rin+L1*L4*yv[2]*Rout
        -L1*L3*Rout*Vso(t)+L1*L3*Rout*yv[3]*Rin+L1*L3*Rout
        *yv[4]*Rin+L1*L3*yv[2]*Rin+L1*L3*yv[2]*Rout-M1*M1*Rout
        *yv[3]*Rin-M1*M1*Rout*yv[4]*Rin+M2*M1*Rout*Vso(t)
        -M2*M1*Rout*yv[3]*Rin-M2*M1*Rout*yv[4]*Rin-M2*M1*yv[1]*Rin
        -M2*M1*yv[1]*Rout+M2*L1*Vcin(t)*Rin+M2*L1*Vcin(t)*Rout
        -M2*L1*yv[5]*Rcout*Rin-M2*L1*yv[5]*Rcout*Rout-M2*L1*yv[5]
        *Rcin*Rin-M2*L1*yv[5]*Rcin*Rout)
        /((L2*L1*L4+L2*L1*L3-L2*M1*M1-L1*M2*M2)*(Rin+Rout));
    dydt[5]=-(L2*M1*Rout*Vso(t)+L2*M1*Rout*yv[3]*Rin+L2*M1*Rout
        *yv[4]*Rin+L2*M1*yv[1]*Rin+L2*M1*yv[1]*Rout-L2*L1*Vcin(t)
        *Rin-L2*L1*Vcin(t)*Rout+L2*L1*yv[5]*Rcout*Rin+L2*L1*yv[5]
        *Rcout*Rout+L2*L1*yv[5]*Rcin*Rin+L2*L1*yv[5]*Rcin*Rout+Rout
        *Vso(t)*L1*M2-Rout*yv[3]*Rin*L1*M2-Rout*yv[4]*Rin*L1*M2
        -yv[2]*Rin*L1*M2-yv[2]*Rout*L1*M2)/((L2*L1*L4+
        L2*L1*L3-L2*M1*M1-L1*M2*M2)*(Rin+Rout));
    dydt[6]= Po*yv[1];
}

```

```

int main(){
    FILE *file;
    float *vstart = vector(1,NOVAR);
    float result;
    int i;
    int nok, nbad;
    /*Now we wish to merely step through the algorithm and determine
    a set of results. We will be using just a fourth order Runge-Kutta
    method as of now. I may change this later. We are merely
    solving the differential equations for a JJ pair assumed to be
    in the configuration of a squid. We can then view the results
    which will be placed in a file for viewing

```

The following configurations will be used.

We shall drive a current through the system that is just under the maximum critical current of $2.0e-4$ amps. We will then apply a control current to the control circuitry linked to our JJ's through the inductance L. This should alter the configuration of the system and create a HVS. We shall analyze the input current, the currents through each JJ, and the voltage across each JJ to determine what state the system is in!

Later models will add the output resistance to shunt the current along with an input current through a voltage and a resistor. An inductance will be used later to model effects of the loop and its self inductance.

We want to see what the basic operation of the SQUID should be*/

```

    xp = vector(1,kmax);
    yp = matrix(1,NOVAR,1,kmax);

    /*Clear the Matrices*/

    for(i=1;i<=NOVAR;i++){
        vstart[i]=0.0;
    }
    printf("Performing Runge Kutta 5th order adaptive integration.\n");
    odeint(vstart,NOVAR,0.0,SIMTIM,EPS,1.0e-13,1.0e-16,&nok,
        &nbad,derive,rkqs);
    printf("nok= %d nbad= %d\n",nok,nbad);

    printf("Simulation over, calculating and printing results\n");

```

```

/*We now should have our answer and we just need to print out*/
file = fopen("JJCONjj","w");
for(i=1;i<=kount;i++){
    fprintf(file,"%g %g\n",xp[i],yp[5][i]);
fclose(file);

/*Print out the input current */
file = fopen("JJINjj","w");
for(i=1;i<=kount;i++){
    result=(Vso(xp[i])-(Vso(xp[i])*Rout-Rin*Rout*(yp[3][i]
        +yp[4][i]))/(Rin+Rout))/Rin;
    fprintf(file,"%g %g\n",xp[i],result);
}
fclose(file);

/*Print out the output current*/
file = fopen("JJOUTjj","w");
for(i=1;i<=kount;i++){
    result=((Vso(xp[i])*Rout-Rin*Rout*(yp[3][i]+yp[4][i]))
        /(Rin+Rout))/Rout;
    fprintf(file,"%g %g\n",xp[i],result);
}
fclose(file);

/*Print out I1 */
file = fopen("JJI1jj","w");
for(i=0;i<=kount;i++){
    fprintf(file,"%g %g\n",xp[i],yp[3][i]);
fclose(file);

/*Print out I2*/
file = fopen("JJI2jj","w");
for(i=0;i<=kount;i++){
    fprintf(file,"%g %g\n",xp[i],yp[4][i]);
fclose(file);

/*Print out Itotal*/
file = fopen("JJITjj","w");
for(i=0;i<=kount;i++){
    fprintf(file,"%g %g\n",xp[i],yp[3][i]+yp[4][i]);
fclose(file);

/*Print out the total voltage */
file = fopen("JJVOLjj","w");
for(i=1;i<=kount;i++){
    fprintf(file,"%g %g\n",xp[i],Vso(xp[i]));
fclose(file);

printf("Done.....\n");

exit(0);

```

Chapter 4

MVTL Simulation Data

The section contains the FD-TLM Data Set, the *FastHenry* extraction data set, MAPLE V results, and the C program for performing the conventional circuit simulation for the MVTL circuit.

4.1 FD-TLM Data Set

NMVTL

T JJ MVTL Circuit

*Generated by FDTGRAPH, copyright 1993, by Christopher G. Sentelle

*Data in format to be used by FD-TLM copyright by Dr. Robert H. Voelker

*University of Nebraska-Lincoln

*

*

*Created on: Fri Aug 11 12:40:33 1995

*Medium material used throughout

*Relative permittivity

E 1 50 1 50 1 50 1 1 1

*Conductivity throughout

L 1 50 1 50 1 50 0 0 0

*Magnetic susceptibility

M 1 50 1 50 1 50 0 0 0

*Relative permeability

U 1 50 1 50 1 50 1 1 1

*Add an insulator of SiO2

E 1 50 1 3 1 50 3.5 3.5 3.5

*Substrate Materials

* Josephson Junction #1

R 17 19 3 17 22 3.039e+15 0.0001 0.004 0 0.1 0.002 0.0001 5e-13 5e-11

* Josephson Junction #2

R 17 19 3 38 43 3.039e+15 0.0003 0.012 0 0.3 0.002 0.0001 1.5e-12 5e-11

```

* Josephson Junction #3
R 23 26 5 18 21 3.039e+15 0.0001 0.004 0 0.1 0.002 0.0001 5e-13 5e-11
* Coupling H field
H 13 27 4 23 37 1 2
*3 dimensional object, Superconductor
L 28 33 4 4 17 43 -1 -1 -1
*Top Surface
L 28 33 5 5 17 43 -1 -2 -1
L 34 34 5 5 17 43 -2 -2 -1
L 28 33 5 5 44 44 -1 -2 -2
*Right Side Surface
L 28 33 4 4 44 44 -1 -1 -2
L 34 34 4 4 44 44 -2 -1 -2
*Back Side Surface
L 34 34 4 4 17 43 -2 -1 -1
*3 dimensional object, Superconductor
L 21 27 4 4 17 22 -1 -1 -1
*Top Surface
L 21 27 5 5 17 22 -1 -2 -1
L 28 28 5 5 17 22 -2 -2 -1
L 21 27 5 5 23 23 -1 -2 -2
*Right Side Surface
L 21 27 4 4 23 23 -1 -1 -2
L 28 28 4 4 23 23 -2 -1 -2
*Back Side Surface
L 28 28 4 4 17 22 -2 -1 -1
*3 dimensional object, Superconductor
L 21 27 4 4 38 43 -1 -1 -1
*Top Surface
L 21 27 5 5 38 43 -1 -2 -1
L 28 28 5 5 38 43 -2 -2 -1
L 21 27 5 5 44 44 -1 -2 -2
*Right Side Surface
L 21 27 4 4 44 44 -1 -1 -2
L 28 28 4 4 44 44 -2 -1 -2
*Back Side Surface
L 28 28 4 4 38 43 -2 -1 -1
*3 dimensional object, Superconductor
L 13 19 4 4 17 22 -1 -1 -1
*Top Surface
L 13 19 5 5 17 22 -1 -2 -1
L 20 20 5 5 17 22 -2 -2 -1
L 13 19 5 5 23 23 -1 -2 -2
*Right Side Surface
L 13 19 4 4 23 23 -1 -1 -2
L 20 20 4 4 23 23 -2 -1 -2
*Back Side Surface
L 20 20 4 4 17 22 -2 -1 -1
*3 dimensional object, Superconductor
L 13 19 4 4 38 43 -1 -1 -1
*Top Surface

```

```

L 13 19 5 5 38 43 -1 -2 -1
L 20 20 5 5 38 43 -2 -2 -1
L 13 19 5 5 44 44 -1 -2 -2
*Right Side Surface
L 13 19 4 4 44 44 -1 -1 -2
L 20 20 4 4 44 44 -2 -1 -2
*Back Side Surface
L 20 20 4 4 38 43 -2 -1 -1
*3 dimensional object, Superconductor
L 7 12 4 4 17 43 -1 -1 -1
*Top Surface
L 7 12 5 5 17 43 -1 -2 -1
L 13 13 5 5 17 43 -2 -2 -1
L 7 12 5 5 44 44 -1 -2 -2
*Right Side Surface
L 7 12 4 4 44 44 -1 -1 -2
L 13 13 4 4 44 44 -2 -1 -2
*Back Side Surface
L 13 13 4 4 17 43 -2 -1 -1
*3 dimensional object, Superconductor
L 21 21 3 3 17 22 -1 -1 -1
*Top Surface
L 21 21 4 4 17 22 -1 -2 -1
L 22 22 4 4 17 22 -2 -2 -1
L 21 21 4 4 23 23 -1 -2 -2
*Right Side Surface
L 21 21 3 3 23 23 -1 -1 -2
L 22 22 3 3 23 23 -2 -1 -2
*Back Side Surface
L 22 22 3 3 17 22 -2 -1 -1
*3 dimensional object, Superconductor
L 21 21 3 3 38 43 -1 -1 -1
*Top Surface
L 21 21 4 4 38 43 -1 -2 -1
L 22 22 4 4 38 43 -2 -2 -1
L 21 21 4 4 44 44 -1 -2 -2
*Right Side Surface
L 21 21 3 3 44 44 -1 -1 -2
L 22 22 3 3 44 44 -2 -1 -2
*Back Side Surface
L 22 22 3 3 38 43 -2 -1 -1
*3 dimensional object, Superconductor
L 17 21 2 2 17 22 -1 -1 -1
*Top Surface
L 17 21 3 3 17 22 -1 -2 -1
L 22 22 3 3 17 22 -2 -2 -1
L 17 21 3 3 23 23 -1 -2 -2
*Right Side Surface
L 17 21 2 2 23 23 -1 -1 -2
L 22 22 2 2 23 23 -2 -1 -2
*Back Side Surface

```

```

L 22 22 2 2 17 22 -2 -1 -1
*3 dimensional object, Superconductor
L 17 21 2 2 38 43 -1 -1 -1
*Top Surface
L 17 21 3 3 38 43 -1 -2 -1
L 22 22 3 3 38 43 -2 -2 -1
L 17 21 3 3 44 44 -1 -2 -2
*Right Side Surface
L 17 21 2 2 44 44 -1 -1 -2
L 22 22 2 2 44 44 -2 -1 -2
*Back Side Surface
L 22 22 2 2 38 43 -2 -1 -1
*Infinitely Thin object, xz-plane DAMP RES 1 OHM
L 25 26 4 4 23 37 -2 -2 5.0e+06
L 27 27 4 4 23 37 -2 -2 5.0e+06
*3 dimensional object, Superconductor
L 34 39 4 4 38 43 -1 -1 -1
*Top Surface
L 34 39 5 5 38 43 -1 -2 -1
L 40 40 5 5 38 43 -2 -2 -1
L 34 39 5 5 44 44 -1 -2 -2
*Right Side Surface
L 34 39 4 4 44 44 -1 -1 -2
L 40 40 4 4 44 44 -2 -1 -2
*Back Side Surface
L 40 40 4 4 38 43 -2 -1 -1
*3 dimensional object, Superconductor
L 40 45 4 4 3 43 -1 -1 -1
*Top Surface
L 40 45 5 5 3 43 -1 -2 -1
L 46 46 5 5 3 43 -2 -2 -1
L 40 45 5 5 44 44 -1 -2 -2
*Right Side Surface
L 40 45 4 4 44 44 -1 -1 -2
L 46 46 4 4 44 44 -2 -1 -2
*Back Side Surface
L 46 46 4 4 3 43 -2 -1 -1
*Infinitely Thin object, xz-plane SRC RES 60 OHMS
L 40 45 4 4 2 2 -2 -2 2380.95
L 46 46 4 4 2 2 -2 -2 2380.95
*3 dimensional object, Superconductor
L 46 49 4 4 38 43 -1 -1 -1
*Top Surface
L 46 49 5 5 38 43 -1 -2 -1
L 50 50 5 5 38 43 -2 -2 -1
L 46 49 5 5 44 44 -1 -2 -2
*Right Side Surface
L 46 49 4 4 44 44 -1 -1 -2
L 50 50 4 4 44 44 -2 -1 -2
*Back Side Surface
L 50 50 4 4 38 43 -2 -1 -1

```

*Infinitely Thin object, xz-plane LOAD RES 16 OHM

L 50 50 4 4 38 43 8928.57 -2 -2

L 50 50 4 4 44 44 8928.57 -2 -2

*3 dimensional object, Superconductor

L 28 33 6 6 3 47 -1 -1 -1

*Top Surface

L 28 33 7 7 3 47 -1 -2 -1

L 34 34 7 7 3 47 -2 -2 -1

L 28 33 7 7 48 48 -1 -2 -2

*Right Side Surface

L 28 33 6 6 48 48 -1 -1 -2

L 34 34 6 6 48 48 -2 -1 -2

*Back Side Surface

L 34 34 6 6 3 47 -2 -1 -1

*3 dimensional object, Superconductor

L 2 27 6 6 46 47 -1 -1 -1

*Top Surface

L 2 27 7 7 46 47 -1 -2 -1

L 28 28 7 7 46 47 -2 -2 -1

L 2 27 7 7 48 48 -1 -2 -2

*Right Side Surface

L 2 27 6 6 48 48 -1 -1 -2

L 28 28 6 6 48 48 -2 -1 -2

*Back Side Surface

L 28 28 6 6 46 47 -2 -1 -1

*3 dimensional object, Superconductor

L 2 3 6 6 6 45 -1 -1 -1

*Top Surface

L 2 3 7 7 6 45 -1 -2 -1

L 4 4 7 7 6 45 -2 -2 -1

L 2 3 7 7 46 46 -1 -2 -2

*Right Side Surface

L 2 3 6 6 46 46 -1 -1 -2

L 4 4 6 6 46 46 -2 -1 -2

*Back Side Surface

L 4 4 6 6 6 45 -2 -1 -1

*3 dimensional object, Superconductor

L 4 26 6 6 6 9 -1 -1 -1

*Top Surface

L 4 26 7 7 6 9 -1 -2 -1

L 27 27 7 7 6 9 -2 -2 -1

L 4 26 7 7 10 10 -1 -2 -2

*Right Side Surface

L 4 26 6 6 10 10 -1 -1 -2

L 27 27 6 6 10 10 -2 -1 -2

*Back Side Surface

L 27 27 6 6 6 9 -2 -1 -1

*3 dimensional object, Superconductor

L 24 26 6 6 10 17 -1 -1 -1

*Top Surface

L 24 26 7 7 10 17 -1 -2 -1

```

L 27 27 7 7 10 17 -2 -2 -1
L 24 26 7 7 18 18 -1 -2 -2
*Right Side Surface
L 24 26 6 6 18 18 -1 -1 -2
L 27 27 6 6 18 18 -2 -1 -2
*Back Side Surface
L 27 27 6 6 10 17 -2 -1 -1
*3 dimensional object, Superconductor
L 22 26 6 6 18 22 -1 -1 -1
*Top Surface
L 22 26 7 7 18 22 -1 -2 -1
L 27 27 7 7 18 22 -2 -2 -1
L 22 26 7 7 23 23 -1 -2 -2
*Right Side Surface
L 22 26 6 6 23 23 -1 -1 -2
L 27 27 6 6 23 23 -2 -1 -2
*Back Side Surface
L 27 27 6 6 18 22 -2 -1 -1
*Infinitely Thin object, xz-plane CNTR SRC RES 16 OHMS
L 28 33 6 6 2 2 -2 -2 8928.57
L 34 34 6 6 2 2 -2 -2 8928.57
*Infinitely Thin object, xz-plane CNTR LOAD RES 1 OHM
L 1 1 6 6 45 47 250000 -2 -2
L 1 1 6 6 48 48 250000 -2 -2
*3 dimensional object, Superconductor
L 1 6 4 4 38 43 -1 -1 -1
*Top Surface
L 1 6 5 5 38 43 -1 -2 -1
L 7 7 5 5 38 43 -2 -2 -1
L 1 6 5 5 44 44 -1 -2 -2
*Right Side Surface
L 1 6 4 4 44 44 -1 -1 -2
L 7 7 4 4 44 44 -2 -1 -2
*Back Side Surface
L 7 7 4 4 38 43 -2 -1 -1
* 1 ps = 600 iterations
*
* Minimum Grid Spacing
A 1e-06
*
*Simulation time (ps) 120
S 111000
*Backup Interval (ps) 125
B 120000
*Plot Interval (ps) 0.1
P 60
*
* A Voltage Source
* A Pulse waveform
* Zero Initial Time 0(ps)
* Rise Time 5(ps)

```

```

* On Time 100(ps)
* Fall Time 5(ps)
* On Voltage -0.02
* Off Voltage 0
*
V P 40 46 4 4 1 1 Z 0 3000 60000 3000 -0.02 0
* A Voltage Source
* A Pulse waveform
* Zero Initial Time 40(ps)
* Rise Time 5(ps)
* On Time 20(ps)
* Fall Time 5(ps)
* On Voltage -0.004
* Off Voltage 0
*
V P 28 34 6 6 1 1 Z 24000 3000 12000 3000 -0.004 0
*Voltage Paths
W Y 1 3 42 6
W Y 1 5 31 8
W Y 1 5 20 46
W Y 1 3 27 19
W Y 1 3 27 41
W Y 1 3 14 20
W Y 1 3 13 40
W Y 1 3 36 39
W Y 1 3 46 41
*
*Current Loops
J Z 39 46 3 5 6
J Z 27 34 5 7 8
J X 5 7 45 48 20
J X 3 5 16 23 27
J X 3 5 37 44 27
J X 3 5 16 23 14
J X 3 5 37 44 13
J X 3 5 37 44 36
J X 3 5 37 44 47
* Variable Mesh Array
* Variable Mesh in the X direction
G X 1 50 1
* Variable Mesh in the Y direction
G Y 1 50 1
* Variable Mesh in the Z direction
G Z 1 50 1

```

4.2 FastHenry Data Set

This is the data set provided to the FastHenry program to determine the values of the two parasitic inductances in the MVTL circuit.

```
*Determination of Inductance for Squid Loop
* June 2, 1995 , Christopher Sentelle
* Uses fasthenry
* This is the inductances used for fmvtl4.dat
* where the inductance values had been updated.
.Units um
* Use a high value for conductivity, Superconductor
.Default nhinc = 1 nwinc = 5 sigma=1.0e20 z=3 w=6 h=1
* Ground Plane
g1 x1=0 y1=0 z1=0
+ x2=50 y2=0 z2=0
+ x3=50 y3=50 z3=0
+ seg1=20 seg2=20
+ thick=1
* Setup for the system
* Squid Loop
N1 x=19 y=36
N2 x=19 y=16
N3 x=22 y=19
N4 x=37 y=19
N5 x=40 y=16
N6 x=40 y=36
N7 x=40 y=37
N8 x=40 y=43
N9 x=37 y=40
N10 x=22 y=40
N11 x=19 y=43
N12 x=19 y=37
E1 N1 N2
E2 N3 N4
E3 N5 N6
E4 N7 N8
E5 N9 N10
E6 N11 N12
.equiv N2 N3
.equiv N4 N5
.equiv N8 N9
.equiv N10 N11
*Control line
N13 x=19 y=2 z=5
N14 x=19 y=47 z=5
N15 x=22 y=46 z=5
N16 x=46 y=46 z=5
N17 x=47 y=47 z=5
```

```
N18 x=47 y=5 z=5
N19 x=46 y=7 z=5
N20 x=26 y=7 z=5
N21 x=24.5 y=5 z=5
N22 x=24.5 y=17 z=5
E7 N13 N14
E8 N15 N16 w=2
E9 N17 N18 w=2
E10 N19 N20 w=4
E11 N21 N22 w=3
* Used to determine Mf
E12 N6 N7
.equiv N14 N15
.equiv N16 N17
.equiv N18 N19
.equiv N20 N21
*Define External Ports
.external N1 N12
.external N13 N22
.freq fmin=1e9 fmax=1e9 ndec=1
.end
```

4.3 MAPLE V Results

These are the results after using MAPLE V to solve the set of differential equations obtained from nodal analysis in terms of a set of first order derivatives of each variable.

> eqn1:=Ic1*sin(phi1(t))+Cj1*diff(V1(t),t)+G1(V1(t))+(V1(t)-V2(t))
 > /Rd-I1(t)+Ic3*sin(phi3(t))+G3(V1(t)-V4(t))+Cj3*diff(V1(t)-V4(t),
 > t)=0;

$$\text{eqn1} := Ic1 \sin(\phi_1(t)) + Cj1 \left(\frac{\partial}{\partial t} V1(t) \right) + G1(V1(t)) + \frac{V1(t) - V2(t)}{Rd} - I1(t) \\ + Ic3 \sin(\phi_3(t)) + G3(V1(t) - V4(t)) + Cj3 \left(\left(\frac{\partial}{\partial t} V1(t) \right) - \left(\frac{\partial}{\partial t} V4(t) \right) \right) = 0$$

> eqn2:=Ic2*sin(phi1(t))-2*PI*(Mf*I3(t)+L2*I2(t)-L1*I1(t))/Flo)+Cj2
 > *diff(V2(t),t)+G2(V2(t))+(V2(t)-V1(t))/Rd-I2(t)=0;

$$\text{eqn2} := Ic2 \sin\left(\phi_1(t) - 2 \frac{\Pi (Mf I3(t) + L2 I2(t) - L1 I1(t))}{Flo}\right) + Cj2 \left(\frac{\partial}{\partial t} V2(t) \right) \\ + G2(V2(t)) + \frac{V2(t) - V1(t)}{Rd} - I2(t) = 0$$

> eqn3:=I1(t)+I2(t)+(V3(t)-Vin(t))/Rin+I4(t)=0;

$$\text{eqn3} := I1(t) + I2(t) + \frac{V3(t) - Vin(t)}{Rin} + I4(t) = 0$$

> eqn4:=V4(t)/Rcout-I3(t)-Ic3*sin(phi3(t))-G3(V1(t)-V4(t))-Cj3*diff
 > f(V1(t)-V4(t),t)=0;

$$\text{eqn4} := \frac{V4(t)}{Rcout} - I3(t) - Ic3 \sin(\phi_3(t)) - G3(V1(t) - V4(t)) - Cj3 \left(\left(\frac{\partial}{\partial t} V1(t) \right) - \left(\frac{\partial}{\partial t} V4(t) \right) \right) = 0$$

> eqn5:=-I4(t)+V5(t)/Rout=0;

$$\text{eqn5} := -I4(t) + \frac{V5(t)}{Rout} = 0$$

> eqn6:=I3(t)=(Vcin(t)-(L3*diff(I3(t),t)-M1*diff(I1(t),t)+M2*diff(
 > I2(t),t)+V4(t)))/Rcin;

$$\text{eqn6} := I3(t) = \frac{Vcin(t) - L3 \left(\frac{\partial}{\partial t} I3(t) \right) + M1 \left(\frac{\partial}{\partial t} I1(t) \right) - M2 \left(\frac{\partial}{\partial t} I2(t) \right) - V4(t)}{Rcin}$$

> eqn7:=V3(t)-V1(t)=L1*diff(I1(t),t)-M1*diff(I3(t),t);

$$\text{eqn7} := V3(t) - V1(t) = L1 \left(\frac{\partial}{\partial t} I1(t) \right) - M1 \left(\frac{\partial}{\partial t} I3(t) \right)$$

> eqn8:=V3(t)-V2(t)=L2*diff(I2(t),t)+M2*diff(I3(t),t);

$$\text{eqn8} := V3(t) - V2(t) = L2 \left(\frac{\partial}{\partial t} I2(t) \right) + M2 \left(\frac{\partial}{\partial t} I3(t) \right)$$

> eqn9:=diff(phi1(t),t)=Po*V1(t);

$$\text{eqn9} := \frac{\partial}{\partial t} \phi_1(t) = Po V1(t)$$

> eqn10:=diff(phi2(t),t)=Po*V2(t);

$$\text{eqn10} := \frac{\partial}{\partial t} \phi_2(t) = Po V2(t)$$

> eqn11:=diff(phi3(t),t)=Po*(V1(t)-V4(t));

```

eqn11 :=  $\frac{\partial}{\partial t} \text{phi3}(t) = Po (V1(t) - V4(t))$ 
> eqn12 := V3(t) - V5(t) = L4 * diff(I4(t), t);
eqn12 :=  $V3(t) - V5(t) = L4 \left( \frac{\partial}{\partial t} I4(t) \right)$ 
> aux1 := solve(eqn3, V3(t));
aux1 :=  $\left( I1(t) + I2(t) - \frac{Vin(t)}{Rin} + I4(t) \right) Rin$ 
> aux2 := solve(eqn5, V5(t));
aux2 :=  $I4(t) Rout$ 
> eqn7a := subs(V3(t)=aux1, eqn7);
eqn7a :=  $\left( I1(t) + I2(t) - \frac{Vin(t)}{Rin} + I4(t) \right) Rin - V1(t) = L1 \left( \frac{\partial}{\partial t} I1(t) \right) - M1 \left( \frac{\partial}{\partial t} I3(t) \right)$ 
> eqn8a := subs(V3(t)=aux1, eqn8);
eqn8a :=  $\left( I1(t) + I2(t) - \frac{Vin(t)}{Rin} + I4(t) \right) Rin - V2(t) = L2 \left( \frac{\partial}{\partial t} I2(t) \right) + M2 \left( \frac{\partial}{\partial t} I3(t) \right)$ 
> eqn12a := subs({V5(t)=aux2, V3(t)=aux1}, eqn12);
eqn12a :=  $\left( I1(t) + I2(t) - \frac{Vin(t)}{Rin} + I4(t) \right) Rin - I4(t) Rout = L4 \left( \frac{\partial}{\partial t} I4(t) \right)$ 
> ans := solve({eqn1, eqn2, eqn4, eqn6, eqn7a, eqn8a, eqn9, eqn11, eqn12a}, {
> diff(V1(t), t), diff(V2(t), t), diff(V4(t), t), diff(I1(t), t), diff(I2(
> t), t), diff(I3(t), t), diff(I4(t), t), diff(phi1(t), t), diff(phi3(t), t
> )});
ans :=  $\left\{ \frac{\partial}{\partial t} \text{phi1}(t) = Po V1(t), \frac{\partial}{\partial t} \text{phi3}(t) = Po (V1(t) - V4(t)), \frac{\partial}{\partial t} V4(t) = - \left( \right. \right.$ 
 $Cj3 Rcout Ic1 \sin(\text{phi1}(t)) Rd + Cj3 Rcout G1(V1(t)) Rd - Cj3 Rcout V2(t)$ 
 $+ Cj3 Rcout V1(t) - Cj3 Rcout I1(t) Rd + Cj3 Rd V4(t) - Cj3 Rd I3(t) Rcout$ 
 $+ Cj1 Rd V4(t) - Cj1 Rd I3(t) Rcout - Cj1 Rd Ic3 \sin(\text{phi3}(t)) Rcout$ 
 $- Cj1 Rd G3(V1(t) - V4(t)) Rcout \left. \right) / (Cj1 Rd Rcout Cj3), \frac{\partial}{\partial t} I1(t) = - \left( L2 M1 I3(t) Rcin \right.$ 
 $- L2 M1 Vcin(t) + L2 M1 V4(t) + L2 L3 I1(t) Rin + L2 L3 I2(t) Rin - L2 L3 Vin(t)$ 
 $+ L2 L3 I4(t) Rin + L2 L3 V1(t) - M2 I1(t) Rin M1 - M2 I2(t) Rin M1 + M2 Vin(t) M1$ 
 $- M2 I4(t) Rin M1 - M2 V2(t) M1 - M2^2 I1(t) Rin - M2^2 I2(t) Rin + M2^2 Vin(t)$ 
 $- M2^2 I4(t) Rin - M2^2 V1(t) \left. \right) / (-M2^2 L1 + L2 L3 L1 - L2 M1^2), \frac{\partial}{\partial t} I2(t) = - \left( \right.$ 
 $- I3(t) Rcin M2 L1 + M1^2 Vin(t) - M1^2 V2(t) + M2 Vin(t) M1 - M1 M2 V1(t)$ 
 $+ L3 L1 I1(t) Rin + L3 L1 I2(t) Rin - L3 L1 Vin(t) + L3 L1 I4(t) Rin + L3 L1 V2(t)$ 
 $- M1^2 I1(t) Rin - M1^2 I2(t) Rin - M1^2 I4(t) Rin - M2 I1(t) Rin M1 - M2 I2(t) Rin M1$ 
 $- M2 I4(t) Rin M1 + Vcin(t) M2 L1 - V4(t) M2 L1 \left. \right) / (-M2^2 L1 + L2 L3 L1 - L2 M1^2),$ 
 $\frac{\partial}{\partial t} I3(t) = - (-Vin(t) L2 M1 + V1(t) L2 M1 + L1 L2 I3(t) Rcin - L1 L2 Vcin(t))$ 

```

$$\begin{aligned}
& + L1 L2 V4(t) - L1 M2 I1(t) Rin - L1 M2 I2(t) Rin + L1 M2 Vin(t) - L1 M2 I4(t) Rin \\
& - L1 M2 V2(t) + I1(t) Rin L2 M1 + I2(t) Rin L2 M1 + I4(t) Rin L2 M1 \Big/ \Big(\\
& - M2^2 L1 + L2 L3 L1 - L2 M1^2 \Big), \frac{\partial}{\partial t} V1(t) = - (Rcout Ic1 \sin(\phi1(t)) Rd \\
& + Rcout G1(V1(t)) Rd - Rcout V2(t) + Rcout V1(t) - Rcout I1(t) Rd + Rd V4(t) \\
& - Rd I3(t) Rcout) / (Cj1 Rd Rcout), \frac{\partial}{\partial t} V2(t) = \Big(\\
& - Ic2 \sin \Big(\frac{\phi1(t) Flo - 2 \Pi Mf I3(t) - 2 \Pi L2 I2(t) + 2 \Pi L1 I1(t)}{Flo} \Big) Rd - G2(V2(t)) Rd \\
& - V2(t) + V1(t) + I2(t) Rd \Big) / (Cj2 Rd), \\
& \frac{\partial}{\partial t} I4(t) = - \frac{I1(t) Rin + I2(t) Rin - Vin(t) + I4(t) Rin + I4(t) Rout}{L4} \Big\}
\end{aligned}$$

> ans[1];

$$\frac{\partial}{\partial t} \phi1(t) = Po V1(t)$$

> ans[2];

$$\frac{\partial}{\partial t} \phi3(t) = Po (V1(t) - V4(t))$$

> ans[3];

$$\begin{aligned}
& \frac{\partial}{\partial t} V4(t) = - (Cj3 Rcout Ic1 \sin(\phi1(t)) Rd + Cj3 Rcout G1(V1(t)) Rd - Cj3 Rcout V2(t) \\
& + Cj3 Rcout V1(t) - Cj3 Rcout I1(t) Rd + Cj3 Rd V4(t) - Cj3 Rd I3(t) Rcout \\
& + Cj1 Rd V4(t) - Cj1 Rd I3(t) Rcout - Cj1 Rd Ic3 \sin(\phi3(t)) Rcout \\
& - Cj1 Rd G3(V1(t) - V4(t)) Rcout) / (Cj1 Rd Rcout Cj3)
\end{aligned}$$

> ans[4];

$$\begin{aligned}
& \frac{\partial}{\partial t} I1(t) = - \Big(L2 M1 I3(t) Rcin - L2 M1 Vcin(t) + L2 M1 V4(t) + L2 L3 I1(t) Rin \\
& + L2 L3 I2(t) Rin - L2 L3 Vin(t) + L2 L3 I4(t) Rin + L2 L3 V1(t) - M2 I1(t) Rin M1 \\
& - M2 I2(t) Rin M1 + M2 Vin(t) M1 - M2 I4(t) Rin M1 - M2 V2(t) M1 - M2^2 I1(t) Rin \\
& - M2^2 I2(t) Rin + M2^2 Vin(t) - M2^2 I4(t) Rin - M2^2 V1(t) \Big) / \Big(\\
& - M2^2 L1 + L2 L3 L1 - L2 M1^2 \Big)
\end{aligned}$$

> ans[5];

$$\begin{aligned}
& \frac{\partial}{\partial t} I2(t) = - \Big(-I3(t) Rcin M2 L1 + M1^2 Vin(t) - M1^2 V2(t) + M2 Vin(t) M1 - M1 M2 V1(t) \\
& + L3 L1 I1(t) Rin + L3 L1 I2(t) Rin - L3 L1 Vin(t) + L3 L1 I4(t) Rin + L3 L1 V2(t) \\
& - M1^2 I1(t) Rin - M1^2 I2(t) Rin - M1^2 I4(t) Rin - M2 I1(t) Rin M1 - M2 I2(t) Rin M1 \\
& - M2 I4(t) Rin M1 + Vcin(t) M2 L1 - V4(t) M2 L1 \Big) / \Big(-M2^2 L1 + L2 L3 L1 - L2 M1^2 \Big)
\end{aligned}$$

> ans[6];

$$\frac{\partial}{\partial t} I3(t) = \frac{-(-V_{in}(t) L2 M1 + V1(t) L2 M1 + L1 L2 I3(t) R_{cin} - L1 L2 V_{cin}(t) + L1 L2 V4(t) - L1 M2 I1(t) R_{in} - L1 M2 I2(t) R_{in} + L1 M2 V_{in}(t) - L1 M2 I4(t) R_{in} - L1 M2 V2(t) + I1(t) R_{in} L2 M1 + I2(t) R_{in} L2 M1 + I4(t) R_{in} L2 M1)}{(-M2^2 L1 + L2 L3 L1 - L2 M1^2)}$$

> ans[7]:

$$\frac{\partial}{\partial t} V1(t) = \frac{-(R_{cout} I_{c1} \sin(\phi1(t)) R_d + R_{cout} G1(V1(t)) R_d - R_{cout} V2(t) + R_{cout} V1(t) - R_{cout} I1(t) R_d + R_d V4(t) - R_d I3(t) R_{cout})}{(Cj1 R_d R_{cout})}$$

> ans[8]:

$$\frac{\partial}{\partial t} V2(t) = \left(-I_{c2} \sin\left(\frac{\phi1(t) Flo - 2 \Pi Mf I3(t) - 2 \Pi L2 I2(t) + 2 \Pi L1 I1(t)}{Flo} \right) R_d - G2(V2(t)) R_d - V2(t) + V1(t) + I2(t) R_d \right) / (Cj2 R_d)$$

> ans[9]:

$$\frac{\partial}{\partial t} I4(t) = - \frac{I1(t) R_{in} + I2(t) R_{in} - V_{in}(t) + I4(t) R_{in} + I4(t) R_{out}}{L4}$$

>

>

4.4 C Code

This is a portion of the C Code used to solve the set of first order differential equations provided by MAPLE using the Runge-Kutta fifth-order method. Conventional circuit simulation results are then obtained.

```
#include "nrutil.c"
#include "odeint.c"
#include "rkqs.c"
#include "rkck.c"

#define NOVAR 6
#define L3 6.0e-12
#define L4 6.0e-12
#define M1 2.0e-12
#define M2 2.0e-12
#define Mf 2.068e-12
#define L1 8.39e-12
#define L2 8.39e-12
#define Ic 1.0e-6
#define G1 4.0e-3
#define I1 0.0
#define G2 0.1
#define Vs 2.0e-3
#define Vt 1.0e-4
#define Io 1.0e-4
#define Po 3.039e15
#define Cj 5.0e-13
#define Rcin 17.78
#define Rcout 1.19
#define Rin 71.99
#define Rout 20.0
#define FLo 2.068e-15
#define TS 1.0e-15 /*One femtosecond shall be used*/
#define PLT 0.1e-12
#define PI 3.141592763
#define SIMTIM 180.0e-12
#define EPS 1.0e-2

int kmax=1300,kount;
float *xp,**yp,dxsav=1.0e-13;

float G(float v)
{
    float ans;
```

```

    ans = G1*v + (I1 + G2*fabs(v))*((1/(1+exp((Vs-v)/Vt)))
                                   -(1/(1+exp((Vs+v)/Vt))));
    return ans;
}

float Vso(float t)
{
    float starttime = 0.0e-12;
    float risetime = 5.0e-12;
    float ontime = 100.0e-12;
    float falltime = 5.0e-12;
    float hicur = 0.010;

    if (t <=starttime)
        return 0.0;
    if ((t>starttime) && (t<=starttime+risetime))
        return (t-starttime)*hicur/risetime;
    if ((t>starttime+risetime)&&(t<=starttime+risetime+ontime))
        return hicur;
    if((t>starttime+risetime+ontime)&&(t<=starttime+risetime+ontime
+falltime))
        return (hicur - (t-(starttime+risetime+ontime))*hicur
                /falltime);
    else
        return 0.0;
}

float Vcin(float t)
{
    float starttime = 30.0e-12;
    float risetime = 5.0e-12;
    float ontime = 20.0e-12;
    float falltime = 5.0e-12;
    float hicur = 0.003;

    if (t <=starttime)
        return 0.0;
    if ((t>starttime) && (t<=starttime+risetime))
        return (t-starttime)*hicur/risetime;
    if ((t>starttime+risetime)&&(t<=starttime+risetime+ontime))
        return hicur;
    if((t>starttime+risetime+ontime)&&(t<=starttime+risetime+ontime
+falltime))
        return (hicur - (t-(starttime+risetime+ontime))*hicur
                /falltime);
    else
        return 0.0;
}

```

```

void derive(float t, float yv[], float dydt[])
{
    int i;
    /*In this new system, the following variables apply:
    y[1]=V1
    y[2]=V2
    y[3]=V4
    y[4]=I1
    y[5]=I2
    y[6]=I3
    y[7]=phi1
    y[8]=phi3
    */
    float G(float v);
    float Vso(float t);
    float Vcin(float t);

    dydt[1]=(Rd*yv[6]*Rcout-Rd*G(yv[3]-yv[1])*Rcout-2.*Rd*yv[6]
        *sin(yv[8])*Rcout-Rd*yv[3]+Rcout*yv[4]*Rd+Rcout*yv[2]
        -Rcout*yv[1]-Rcout*G(yv[1])*Rd-Rcout*yv[4]*sin(yv[7])
        *Rd-Rcout*G(yv[1]-yv[3])*Rd)/(Cj1*Rcout*Rd);
    dydt[2]=-((-yv[5]*Rd+yv[2]-yv[1]+G(yv[2])*Rd+Ic2*sin((yv[7]*Flo-2
        *PI*(Mf*yv[6]-L2*yv[5]+L1*yv[4]))/Flo)*Rd)/(Cj2*Rd);
    dydt[3]=(Cj3*Rd*I3(t)*Rcout-Cj3*Rd*G(yv[3]-yv[1])*Rcout
        -2*Cj3*Rd*Ic3*sin(yv[8])*Rcout-Cj3*Rd*yv[3]+Cj3*Rcout
        *yv[4]*Rd+Cj3*Rcout*yv[2]-Cj3*Rcout*yv[1]-Cj3*Rcout
        *G(yv[1])*Rd-Cj3*Rcout*Ic1*sin(yv[7])*Rd
        -Cj3*Rcout*G(yv[1]-yv[3])*Rd+Cj1*Rd*yv[6]*Rcout-Cj1*Rd
        *G(yv[3]-yv[1])*Rcout-Cj1*Rd*Ic3*sin(yv[8])*Rcout-Cj1*Rd
        *yv[3])/(Cj1*Rcout*Rd*Cj3);
    dydt[4]=-((M1*L2*yv[6]*Rcin-M1*L2*Vcin(t)+M1*L2*yv[3]+M2*M1*yv[1]

}

int main(){
    FILE *file;
    float *vstart = vector(1,NOVAR);
    float result;
    int i;
    int nok, nbad;

    /* This next simulation will simulate the MVTL circuit. Simulation
    will be performed with this system followed by simulation with the
    FDTLM method.

    The following configurations will be used.

    We shall drive a current through the system that is just under the
    maximum critical current of 2.0e-4 amps. We will then apply a

```

control current to the control circuitry linked to our JJ's through the inductance L. This should alter the configuration of the system and create a HVS. We shall analyze the input current, the currents through each JJ, and the voltage across each JJ to determine what state the system is in!

Later models will add the output resistance to shunt the current along with an input current through a voltage and a resistor. An inductance will be used later to model effects of the loop and its self inductance.

We want to see what the basic operation of the SQUID should be*/

```

xp = vector(1,kmax);
yp = matrix(1,NOVAR,1,kmax);

/*Clear the Matrices*/

for(i=1;i<=NOVAR;i++){
    vstart[i]=0.0;
}
printf("Performing Runge Kutta 5th order adaptive integration.\n");
odeint(vstart,NOVAR,0.0,SIMTIM,EPS,1.0e-13,1.0e-16,&nok,
    &nbad,derive,rkqs);
printf("nok= %d nbad= %d\n",nok,nbad);

printf("Simulation over, calculating and printing results\n");
/*We now should have our answer and we just need to print out*/
file = fopen("JJCON","w");
for(i=1;i<=kount;i++){
    fprintf(file,"%g %g\n",xp[i],yp[5][i]);
}
fclose(file);

/*Print out the input current */
file = fopen("JJIN","w");
for(i=1;i<=kount;i++){
    result=(Vso(xp[i])-(Vso(xp[i])*Rout-Rin*Rout*(yp[3][i]
    +yp[4][i]))/(Rin+Rout))/Rin;
    fprintf(file,"%g %g\n",xp[i],result);
}
fclose(file);

/*Print out the output current*/
file = fopen("JJOUT","w");
for(i=1;i<=kount;i++){
    result=((Vso(xp[i])*Rout-Rin*Rout*(yp[3][i]+yp[4][i]))
    /(Rin+Rout))/Rout;

```

```

        fprintf(file,"%g %g\n",xp[i],result);
    }
    fclose(file);

    /*Print out I1 */
    file = fopen("JJI1","w");
    for(i=0;i<=kount;i++)
        fprintf(file,"%g %g\n",xp[i],yp[3][i]);
    fclose(file);

    /*Print out I2*/
    file = fopen("JJI2","w");
    for(i=0;i<=kount;i++)
        fprintf(file,"%g %g\n",xp[i],yp[4][i]);
    fclose(file);

    /*Print out Itotal*/
    file = fopen("JJIT","w");
    for(i=0;i<=kount;i++)
        fprintf(file,"%g %g\n",xp[i],yp[3][i]+yp[4][i]);
    fclose(file);

    /*Print out the total voltage */
    file = fopen("JJVOL","w");
    for(i=1;i<=kount;i++)
        fprintf(file,"%g %g\n",xp[i],Vso(xp[i]));
    fclose(file);

    printf("Done.....\n");

    exit(0);
}

```

References

- [1] R. H. Voelker and R. J. Lomax, "Three-dimensional simulation of integrated circuits using a variable mesh TLM method," *Microwave and Opt. Technol. Lett.*, vol. 2, pp. 125-127, Apr. 1989.
- [2] M. Kamon, C. Smithhisler, and J. White, "FastHenry User's Guide," Research Laboratory of Electronics, Dept. of Elect. Engr. and Comp. Sci, Massachusetts Institute of Technology, Cambridge, MA, Sept. 13, 1994.
- [3] B. Johnson, *et al.*, "SPICE3 version 3e1 User's Manual," Dept. of Elect. Engr. and Comp. Sci., Univ. of California, Berkeley, CA, Apr. 1, 1991.
- [4] B. W. Char, *et al.*, *First Leaves: A Tutorial Introduction to Maple V*. New York: Springer-Verlag, 1992.
- [5] W. H. Press, S. A. Teukolsky, W. T. Vetterling, and B. P. Flannery, *Numerical Recipes in C*, 2nd ed. New York: Cambridge University Press, 1992.
- [6] S. Hasuo and T. Imamura, "Digital Logic Circuits," *Proceedings of the IEEE*, vol. 77, no. 8, pp. 1177-1190, Aug. 1989.
- [7] S. Takada, "Progress on Josephson Computer," *Nonlinear Superconductive Electronics and Josephson Devices.*, Plenum Press: New York, 1991.

- [8] H. Jackel, W. Bachtold, "Computer-Simulation for Digital Josephson Devices and Circuits," *Circuit Analysis, Simulation and Design*. North-Holland: Elsevier Science Publishers, 1986
- [9] J. G. Rollins, "Numerical simulator for superconducting integrated circuits," *IEEE Trans. Computer-Aided Design*, vol. 10, pp. 245-251, Feb. 1991.
- [10] J. Clarke, "Principles and Applications of SQUIDs," *Proceedings of the IEEE*, vol. 77, no. 8, pp. 1208-1221, Aug. 1989.
- [11] T. P. Orlando and K. A. Delin, *Foundations of Applied Superconductivity*. Addison-Wesley Publishing Company: New York, 1991.
- [12] R. H. Voelker and C. G. Sentelle, "FD-TLM Modeling of Josephson Junction Circuits," *IEEE Microwave and Guided Wave Lett.*, vol. 5, pp. 137-138, May 1995.
- [13] T. VanDuzer and C. W. Turner, *Principles of Superconductive Devices and Circuits*. New York: Elsevier, 1981.
- [14] S. T. Ruggiero and D. A. Rudman, *Superconducting Devices*. Boston: Academic Press, 1990.
- [15] __, "A finite-difference transmission line matrix method incorporating a nonlinear device model," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 302-312, Mar. 1990.
- [16] R. H. Voelker and C. G. Sentelle, "Graphical modeling interface for FD-TLM electromagnetic field simulation of high-speed pulse propagation in active structures," in *Dig. 1994 IEEE AP-S Intl. Symp.*, Seattle, WA, June 1994, pp. 1120-1123.

- [17] G. Costabile, S. Pagano, N. F. Pedersen, and M. Russo, *Nonlinear Superconductive Electronics and Josephson Devices*. New York: Plenum Press, 1991.
- [18] M. A. Megahed, "Nonlinear Analysis of Microwave Superconductor Devices Using Full-Wave Electromagnetic Model," *IEEE Transactions on Microwave Theory and Techniques*., vol. 43, no. 11, pp. 2590-2598, Nov. 1995.
- [19] C. G. Sentelle and R. H. Voelker, "FD-TLM Electromagnetic Field Simulation of High-Speed Josephson Junction Digital Logic Gates," *IEEE Transactions on Microwave Theory and Techniques*., accepted for publication, Dec., 1995.