



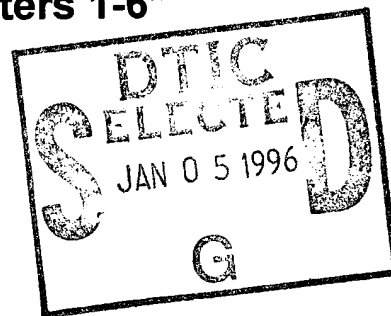
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**Transient Radiation Effects on Electronics (TREE)
Handbook**
Formerly "Design Handbook for TREE, Chapters 1-6"

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Defense Nuclear Agency
6801 Telegraph Road
Alexandria, VA 22303



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CHAPTER 1

INTRODUCTION

1.1 Objectives and Applicability

The objective of the *Transient Radiation Effects on Electronics (TREE) Handbook* is to (1) provide information about radiation effects on semiconductor devices and materials, (2) provide guidelines for microelectronic radiation-hardening technology, and (3) serve as a reference for radiation hardness assurance and microelectronic radiation testing.

The radiation environments addressed in this handbook include those produced by nuclear weapon effects (NWE) and natural space. The NWE environment includes x rays, gamma rays, and neutrons. The natural space environment includes protons and electrons trapped in the Van Allen belt, and neutrons, heavy ions, and cosmic rays found in space. Sections 1.3 and 1.4 describe these radiation environments (threats) and present information that will serve as background material for subsequent discussions of radiation effects as well as microelectronic radiation-hardening requirements.

In general, there are two basic effects to be considered: ionization and atomic displacement. X-ray, gamma-ray, electron, proton, and heavy-ion interactions result in ionizing effects. Atomic displacement effects are primarily the result of neutrons, protons, and heavy ions. These particles also produce ionization, but only as a secondary effect. Similarly, electrons and other charged particles can produce displacement effects.

This handbook is designed as a reference manual for individuals with scientific backgrounds (e.g., electronic and electrical engineers, physicists, electronic technicians) who do not possess in-depth knowledge of radiation effects on electronics and electro-optics. The handbook should

serve as a useful reference for program managers and system program officers (SPOs) who must manage the development of systems that have nuclear hardening and survivability requirements. In addition, the handbook can serve as a guide for making a qualitative assessment of a system's tolerance to radiation effects.

1.2 Handbook Organization

The information in this handbook is organized into seven chapters. Chapter 1 is an introduction to the subjects covered in this handbook. The environments of interest are described in summary form. These are the NWE and natural space environments. In addition, system development backgrounds and the system nuclear hardening requirements are discussed. Chapter 1 concludes with a section on nuclear specification development at the system level.

Chapter 2 discusses ionizing radiation dose effects on electronic devices and circuits. The chapter begins with radiation sources and their interaction with matter. Basic mechanisms of ionizing radiation effects on electronic materials are discussed. The chapter then addresses ionizing radiation dose effects on linear and digital integrated circuits fabricated from metal oxide semiconductor (MOS) and bipolar transistors. Additional sections describe nonvolatile memory technology and optical devices and optical fibers.

Chapter 3 presents ionizing dose rate effects in microelectronics. The effects of ionizing dose rate are presented for the same types of electronic devices and circuits as discussed in Chapter 2 for ionizing radiation dose. Transient upset and latchup phenomena in integrated circuits are also addressed. Chapter 3 concludes with a discussion of single-event phenomena (SEP).

Chapter 4 presents displacement damage effects on electronic devices and circuits. The basic mechanisms of atomic displacement are discussed in sufficient detail to aid the reader in calculating its effects on circuit design. The effects on silicon-based microelectronics, GaAs devices, optical devices, and silicon sensor arrays are then presented in more detail.

Chapter 5 covers the topics of component and circuit design. Hardening methods based on device selection are presented after a brief introduction to hardened design procedures. Specific hardening guidelines for linear and nonlinear circuits are given for displacement, ionizing radiation dose rate, ionizing radiation dose, and single-event effects (SEE). Basic analysis techniques and device models are discussed. Chapter 5 concludes with a discussion of system-level guidelines and the resources required for hardening. A final section briefly discusses the evaluation of existing systems.

Chapter 6 is concerned with radiation response testing and hardness assurance. A discussion of response testing includes information on test planning, testing guidelines, simulation facilities, and testing specifics for each environment as well as for combined environments. Radiation dosimetry considerations are also included. The hardness assurance section describes basic concepts, piece-part hardness assurance procedures and guidelines, hardness categories, design margin, and statistical concepts for hardening. Parts procurement and acceptance tests are also addressed. A list of standard documents and specifications for testing and parts procurement is included.

Chapter 7 contains the explanations for the acronyms and symbols used in the handbook, as well as a glossary defining the handbook's terminology.

1.3 Nuclear Weapon Effects Environments

The primary nuclear explosion outputs of concern in electronic systems are the neutrons, gamma rays, and x rays. These outputs also generate secondary radiations and electromagnetic pulse

(EMP) by interaction with the atmosphere, weapon debris, and system enclosures.

The *weapons designer* usually describes the nuclear explosion output in terms of energy, time, direction, and integrated totals for gamma rays, neutrons, and x rays. The *system designer* usually describes the radiation field as it impinges on the system in terms of energy per unit area, neutron fluence, gamma exposure, and pulse shape as affected by radiation transport through some intervening material. Finally, the *designer of the individual electronic piece part or circuit* is concerned with describing the radiation in units that are convenient for defining the radiation effect to be taken into account, in terms of energy deposition per unit mass or volume, such as 1-MeV equivalent neutron fluence, gamma dose, gamma dose rate, and radiation pulse shape.

Most of the energy released in a nuclear explosion heats the material of the nuclear device to temperatures of tens of millions of degrees. A fraction (0.1 to 10 percent) escapes promptly in the form of fast neutrons and prompt gamma rays. This intense thermal source radiates most of its energy in the form of x rays.

After the prompt radiations have been emitted from the nuclear explosion, a residue of hot, radioactive debris remains. Some of its energy continues to be radiated as thermal energy in the ultraviolet and visual regions of the spectrum. Subsequent radioactive decay of the debris produces lower intensity gamma rays as well as high-energy electrons. These electrons are particularly important for high-altitude nuclear detonations, which may inject the electrons into orbits trapped by the earth's magnetic field.

If the explosion occurs within or near the atmosphere, the prompt radiations interact with the atmosphere and produce secondary effects. The x rays are absorbed most strongly and, depending upon altitude, the air is heated by the interaction to produce an intense thermal source and a blast wave in the air. The neutrons interact with the atmosphere to produce secondary gamma rays. The

gamma rays interact to produce secondary electrons. These secondary electrons in turn interact with the air and produce additional electrons. The net result is negatively charged electrons flowing radially outward from the explosion, while the heavier ions remain behind. If the explosion occurs in a homogeneous (constant density) atmosphere, two shells of charge are created: an inner positive ion shell, and an outer negative electron shell. A large local electric field is created in the radial direction; however, under such conditions, no electromagnetic field is radiated away. In practice, the earth's magnetic field, the earth's surface, and other inhomogeneities will result in an EMP emanating from the source region.

The general time frame for the arrival of the various radiation components at the electronics package is important. For the purposes of electronic vulnerability, the prompt gamma radiation can be considered as a single pulse. Since the flight time for x rays and gamma rays of all energies equals the speed of light, unscattered photons arrive at the equipment with the same time distribution they had at the source, with a time delay of 3.33 $\mu\text{sec}/\text{km}$ from the weapon burst. The arrival of the gamma pulse approximately coincides with the unscattered prompt x rays.

The neutrons arrive after the initial gamma and x-ray radiation. Their arrival time depends on the neutron energy and the range to the receiver. The first neutrons to arrive are the unscattered 14-MeV neutrons. Their time of flight is 19.3 $\mu\text{sec}/\text{km}$; therefore, they will arrive 16 $\mu\text{sec}/\text{km}$ after photon arrival. The photons resulting from neutron inelastic scattering also begin to arrive at about this time. Within 32.8 $\mu\text{sec}/\text{km}$ (arrival time after photon arrival for 4-MeV neutrons), the photons resulting from neutron inelastic scattering is complete, since the inelastic-scatter contribution is negligible for lower-energy neutrons. Within 69.0 $\mu\text{sec}/\text{km}$, most of the unscattered 1-MeV neutrons will have been deposited. The photons resulting from neutron capture (or thermalization) typically will peak shortly after the arrival of the 1-MeV neutrons. Both the thermalization time and the capture time following

thermalization depend strongly on the interacting materials and the system configuration. All of the radiation of interest for transient radiation effects on electronics arrive at the equipment within 1 second.

Gamma rays interact with matter in three ways. In the Compton effect, the gamma ray collides with an electron and some of its energy is transferred to the electron. This energetic electron slows down through the scattering process, producing a large quantity of low-energy electrons. Secondary photons, which have less energy than gamma rays, are also created. The Compton process is the dominant ionization mechanism for electronic materials such as silicon. In the photoelectric effect, a photon, with energy somewhat greater than the binding energy of an electron in an atom, transfers all of its energy to the electron, which is then ejected from the atom. Since the photon involved in the photoelectric effect transfers all of its energy, it ceases to exist and is said to be absorbed. The third type of interaction is pair production. When a gamma-ray photon with energy in excess of 1.02 MeV passes near the nucleus of an atom, the photon may be converted into matter with the formation of an equally but oppositely charged pair of electrons. The positive electron soon interacts with a negative electron to form two photons, each having an energy of at least 0.51 MeV. In some cases, if the interaction takes place near the nucleus of a heavy atom, only one photon of about 1.02-MeV energy may be created. [For more details see EM-1, Chapter 8 (Kaul *et al.*, 1990)].

Fast neutrons can produce ionization indirectly. As neutrons undergo elastic and inelastic scattering as well as capture in a material, emitted gamma rays can cause ionization. In addition, collision of a neutron with an atom may impart sufficient energy to the atom for it to cause ionization. The 14-MeV neutrons arising from fusion reactions in a weapon are particularly important. Thermalized neutrons can also contribute ionization by neutron-capture gamma rays, particularly in those materials that undergo (n,α) and (n,p) reactions.

Once the charged particles are created by the ionization processes (either primary or secondary), they undergo various reactions. Coulomb collisions result in further ionization events. This process is very effective as long as the resultant progenies have energies greater than the ionization potential of the medium in which they move. Eventually, all the energy is dissipated by the creation of (almost) thermalized carriers (e.g., electrons, ions, holes). Meanwhile, the initial particle energy has been distributed over a volume encompassed by the primary and secondary particle ranges and some net charge displacement has occurred. The thermalized progenies are free to move in the material, scattering frequently and following a random-walk pattern. If the concentration of electric charge carriers throughout the material is not uniform and if no externally applied electric field is present, the carriers will move from regions of high concentration to regions of low concentration. This movement is known as diffusion and when it occurs, it is superimposed on the normal random movement. If an applied electric field is present, the carriers drift in the electric field while they undergo random scattering. If impurities or lattice defects are present in the material (as they always are in solid-state devices), carriers may be captured (trapped) and immobilized by impurity atoms and lattice defects (traps). Eventually, the trapped carriers will be annihilated by their mates (oppositely charged carriers) in a process called recombination. The net result of these processes is that the carriers diffuse and/or drift until they are trapped and (usually) recombined.

The free carriers produced during ionization respond to an applied electric field by producing a net drift current, the mechanism by which a material conducts electricity. Therefore, ionization induces a transient increase in conductivity.

Semiconductor devices employ both positively and negatively charged carriers. The characteristics of many such devices depend strongly upon the instantaneous concentration of minority carriers in various regions of the device. Since ionizing radiation creates large (and equal) numbers of

positively and negatively charged carriers, the concentration of minority carriers in the device is temporarily increased by ionizing radiation, and the electrical operation of the device may be adversely affected.

When free carriers are created in a semiconductor material and are trapped at impurity sites, many may not undergo recombination with their mates, which may be trapped elsewhere. In these cases, the material properties may be altered semipermanently, even though there is no net charge in the material. This ionization effect is known as charge trapping.

The chemical effects of ionization occur during the processes of trapping and recombination when sufficient energy is available to disrupt chemical bonds. When ionization is complete, permanent changes of physical and/or electrical properties may occur. The radiation dose required to cause such effects is typically larger than that normally encountered in TREE applications.

Displacement is an important phenomenon in crystalline materials, and it is a very important phenomenon in TREE because many electronic devices (e.g., transistors, diodes, integrated circuits) are constructed from crystalline semiconductors — primarily silicon and germanium. Lattice defects result from the displacement of atoms from their usual sites in crystal lattices. The simplest lattice defects, stable only at very low temperatures, are extra atoms inserted between lattice positions (interstitial) and unoccupied lattice positions (vacancies). At least part of the resultant damage to the material is stable and accounts for permanent property changes of irradiated crystalline materials.

The production of displacement damage in a crystalline solid is a complex process. An abbreviated description of this process is given below:

1. Radiation of an appropriate form enters the material, interacts with a lattice atom, and imparts to it a certain energy.
2. The target (recoil) atom leaves its lattice site, thus creating a vacancy, and collides with other lattice atoms.

3. Other atoms are displaced from their sites, creating yet more vacancies.
4. Eventually, most recoil atoms come to rest in interstitial positions, while a few fall into vacancies. Interstitials and vacancies are not stable at room temperature and eventually disappear or form more complex lattice defects.
5. The defects migrate through the crystal.
6. Eventually, the mobile defects are annihilated by recombination of vacancy-interstitial pairs, are immobilized by the formation of stable defect clusters with other impurities or lattice defects (either present in the original material or created by the irradiation), or escape to a free surface.
7. Meanwhile, the physical properties of the material are changed by the presence of the defects.

1.4 Natural Space Radiation Environment

In this section, the earth's space radiation environment is described in terms of trapped and nontrapped charged particles as relevant to effects on spacecraft electronics. The nature and magnitude of the spatial distribution and temporal variation in the trapped radiation environment are presented. Transiting cosmic rays of galactic and solar origin are described, and their interaction with the earth's magnetic field is considered. In terms of spacecraft electronics, accumulated damage from electron and proton exposure will limit system endurance. Transient effects from individual high-energy protons or cosmic rays can disrupt system operation, perhaps irreversibly.

The internal spacecraft radiation environment is described in terms of shielding effectiveness against the high-energy electrons, protons, and cosmic rays of the external environment. Exposure levels are presented in terms of ionizing radiation dose and particle fluence to permit comparison to electronic component damage sus-

ceptibility data. This will permit the assessment of the potential frequency or probability of critical effects in the electronics. Of particular importance are the limits in shielding effectiveness for high-energy electrons, protons, and cosmic rays.

The interactions between the space radiation environment and spacecraft electronics include those at the external surfaces as well as those within the internal electronics. Important effects at the external surfaces include degradation of solar cells and charging of dielectric material, which can result in transient-producing arc discharges. For these external effects, the characterization of the free-field electron and proton environment as a function of particle energy and time is important. The internal spacecraft radiation environment is defined by particle transport through the spacecraft structure and, when necessary, the shielding added to protect sensitive electronic piece parts. Important effects on the internal electronics are performance degradation resulting from energy deposition by accumulated ionization in semiconductor materials, accumulated atomic displacement damage in the crystal semiconductor by high-energy protons, and transient effects resulting from the ionization tracks from the interaction of a single cosmic ray or high-energy proton. Therefore, of particular interest for effects on the internal electronics are the total electron and proton exposure (i.e., fluence) and the time-dependent rate of high energy protons and cosmic rays (i.e., flux).

The earth's natural radiation environment consists of electrons, protons, and heavy ions that are either trapped by the earth's magnetic field, or that are transiting through the domains of the earth's artificial satellites. Trapped radiation and transiting radiation environments are discussed below [Subsections 1.4.1 and 1.4.2].

1.4.1 Trapped Radiation

As the earth sweeps through the solar wind, a geomagnetic cavity is formed by the earth's magnetic field, as shown in Figure 1-1, which defines the magnetosphere. The cavity is hemispherical on

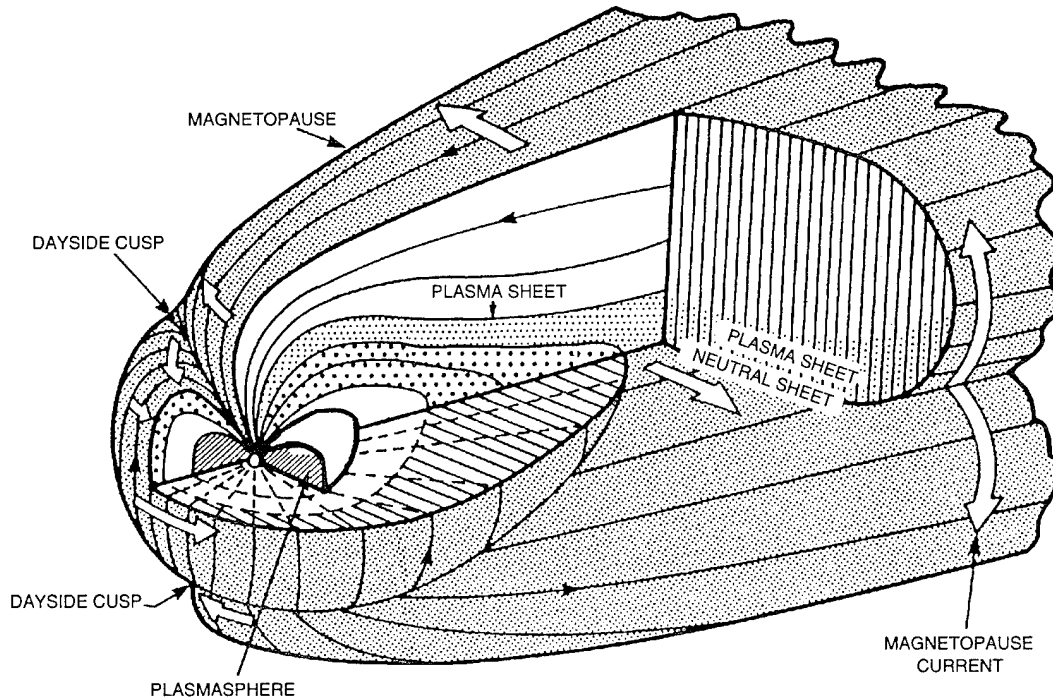


Figure 1-1. The geomagnetic cavity (Barraclough *et al.*, 1975; IAGA, 1986; Spjeldvik and Rothwell, 1983).

the sun side, with a boundary at approximately 10 to 12 earth radii ($R_e = 6,380$ km). On the night side, it is cylindrical, approximately $40 R_e$ in diameter. Because of the sweeping action of the solar wind, it extends over several hundred R_e in the antisolar direction. The main particle-trapping region, of specific interest here, is the cross-hatched area labeled plasmasphere.

The total magnetic field of the magnetosphere is defined in terms of two interacting and superimposed sources of internal and external origin. The internal field of the earth is thought to be caused by convective motion in the molten nickel-iron core of the planet, and by a residual permanent magnetism in the earth's crust. The external field is comprised of the sum-total effect of currents and fields set up in the magnetosphere by the solar wind. The internal field component of the earth's magnetic field exhibits gradual changes with time, characterized as secular variations (Barraclough *et al.*, 1975; IAGA, 1986). These temporal effects are also observed in the shrinking value of the earth's dipole moment and the drift in the location of the boreal (north) and austral (south) magnetic poles.

Superimposed on these slow internal changes are cyclic variations in the external field, whose magnitudes depend on the degree of perturbation experienced by the magnetosphere. Specifically, strong perturbations of the geomagnetic field are present in the outer magnetosphere and depend on local time (diurnal effects), season (tilt effects), and solar wind conditions (including solar flares) (Stassinopoulos and King, 1974). All of these affect the magnetospheric current systems, which in turn modify the local field values.

A characteristic of the geomagnetic field, of particular significance to space radiation effects in electronics, is the Brazilian or South Atlantic anomaly (SAA). This is primarily the result of the offset of the dipole term of the geomagnetic field by approximately 11 degrees from the earth's axis of rotation and its displacement of about 500 km toward the Western Pacific. The effect is an apparent depression of the magnetic field over the coast of Brazil. There, the Van Allen belt reaches lower altitudes, extending down into the atmosphere. The SAA is responsible for most of the trapped radiation received in low-earth orbits (LEO). In

contrast, on the opposite side of the globe, the Southeast-Asian anomaly displays correspondingly stronger field values, and the trapped-particle belts are located at higher altitudes.

1.4.1.1 Trapped Radiation Domains

The earth's magnetic field, above the dense atmosphere, is populated with trapped electrons, protons, and a small number of low-energy, heavy ions. These particles gyrate around and bounce along magnetic field lines and are reflected back and forth between pairs of conjugate mirror points (i.e., regions of maximum magnetic field strength along their trajectories) in opposite hemispheres. At the same time, because of their charge, electrons drift eastward around the earth, while protons and heavy ions drift westward. Figure 1-2 illustrates the spiral and drift motion of the trapped particles.

The magnetosphere can be divided into five domains for populating or visiting particle species, as shown in Figure 1-3. The strong dependence of trapped particle fluxes on altitude and latitude is expressed in terms of the McIlwain L parameter (McIlwain, 1961), where L is a dimensionless ratio

of the earth's radius, approximately equal to the geocentric distance of a field line in the geomagnetic equator. Also shown in Figure 1-3 are the domains mapped by using the dipole field equation:

$$R = L \cos^2 \Lambda, \quad (1.1)$$

(or R - L space), where R is the radial distance and L is the invariant latitude. It should be noted that the representation using L becomes increasingly invalid for equatorial distances greater than four times R_e because of the more complex particle motion in the geomagnetic field and the distortion of the geomagnetic cavity by solar wind interaction effects.

The indicated domain boundaries should be considered only as transitions, and not as actual lines. These boundaries are assumed for modeling purposes and, additionally, are used here for a qualitative picture of the charged-particle distribution. "Real" boundaries are diffused areas, varying with particle energy, and fluctuating in position due to magnetic perturbations, local time effects, solar cycle variations (minimum and maximum activity phases), and individual solar events.

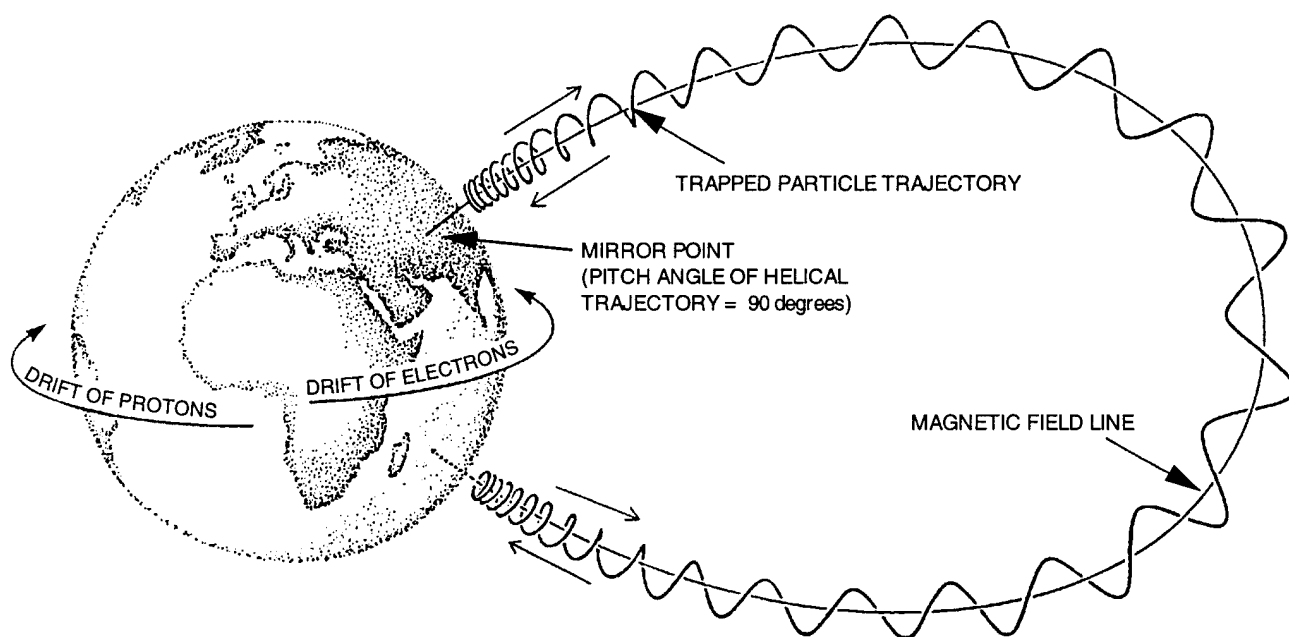


Figure 1-2. Trapped particle trajectory and drift motion (Spjeldvik and Rothwell, 1983).

Electrons. Energetic Van Allen belt electrons are distinguished into “inner zone” and “outer zone” populations. The volume of space occupied by the inner zone extends at the equator to about $2.4 R_e$. These domains are indicated in Figure 1-3 & 1-4 by region 1 for the inner zone electrons, and by regions 2 through 4 for the outer zone electrons. The $L = 2.8$ line is used to separate the inner and outer zone domains, while the termination of the outer zone at $L = 12$ is intended only to delineate the maximum outward extent of stable, or pseudoelectron, trapping. The region between $L = 2.5$ and 2.8 is called the “slot.” During magnetospherically quiet times, its electron density is very low. However, during magnetic storms, the electron flux in the slot may increase by several orders of magnitude.

The inner zone electrons are less severe compared to the outer zone electrons. Specifically, the outer zone has peak fluxes exceeding those of the inner zone by about an order of magnitude. Addi-

tionally, the outer-zone spectra extend to much higher energies (~ 7 MeV) than the inner-zone spectra (< 5 MeV). In this subsection, a detailed description of both the external and internal radiation environments is presented for LEO in the inner zone, and for geostationary earth orbits (GEO) within the outer zone.

Protons. Protons with energies greater than 10 MeV populate regions 1 and 2 with an approximate trapping boundary placed at $L = 3.8$, as shown in Figure 1-3. In contrast to electrons, the energetic trapped protons ($E > 1$ MeV) occupy a volume of space that varies inversely and monotonically with their energy, as shown in Figure 1-4. Consequently, these particles cannot be assigned to inner and outer zones. Figure 1-5 shows the proton flux intensities as a function of radial distance and energy. In low-earth orbits, the most intense and penetrating radiation is encountered in the form of protons in the SAA.

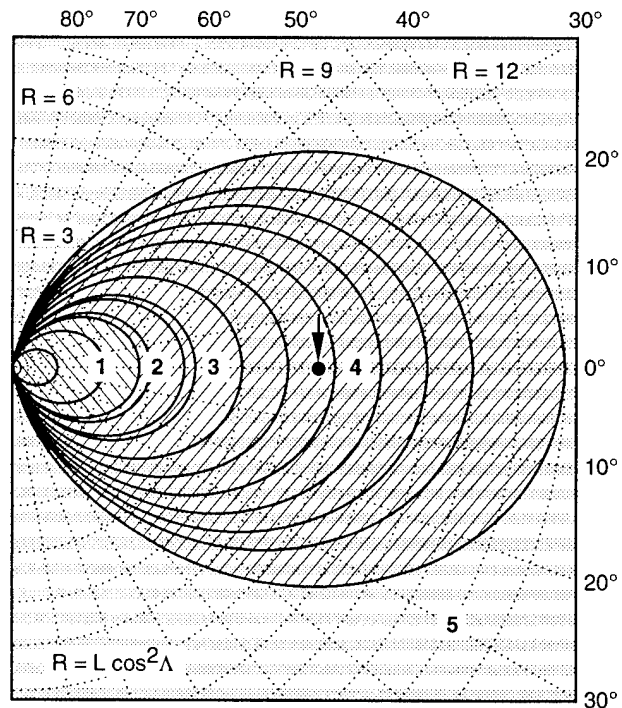
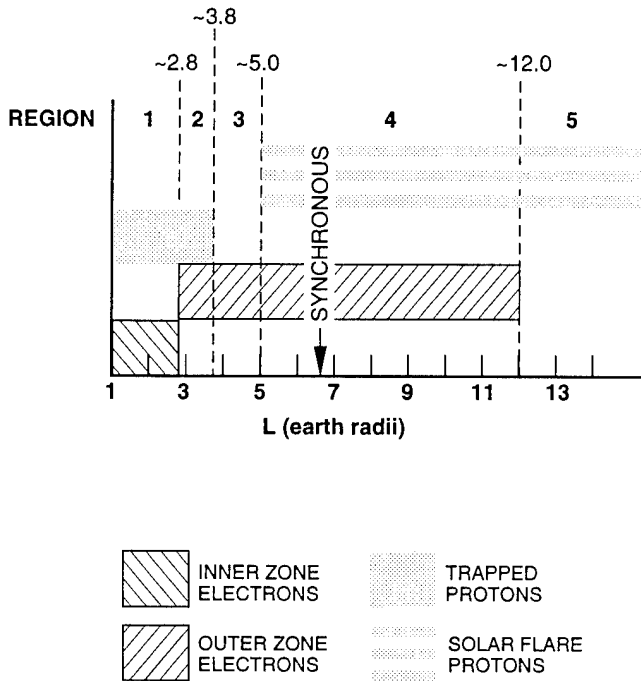


Figure 1-3. Charged-particle distribution in the magnetosphere (Stassinopoulos and Raymond, 1988).

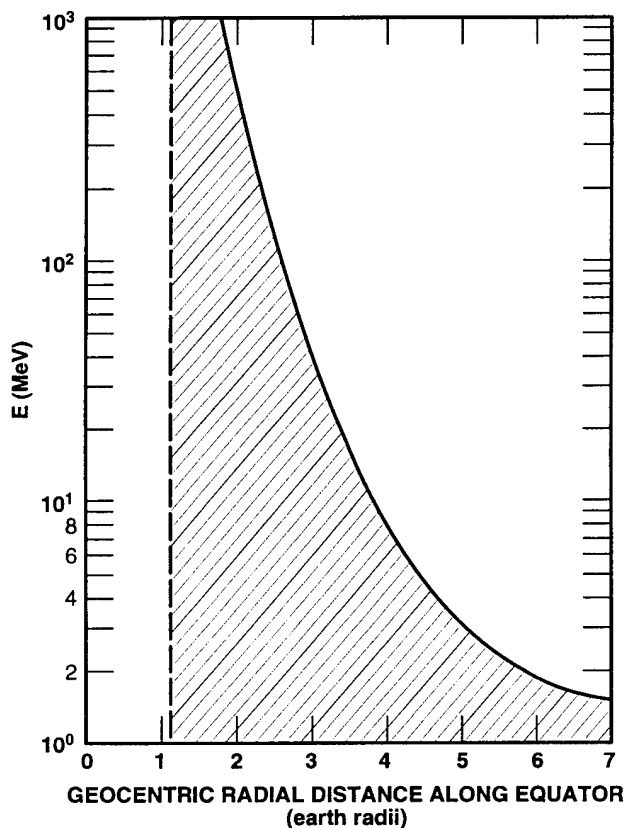


Figure 1-4. Trapped proton population as a function of energy (Stassinopoulos and Raymond, 1988).

1.4.1.2 Trapped Radiation Models

Available radiation measurements from space form the basis for models of the trapped electron and proton environment. These models have been developed by the U.S. National Space Science Data Center (NSSDC) at NASA's Goddard Space Flight Center. All models are constructed with several dozen data sets from a corresponding number of satellites, providing a wide spatial and a long temporal coverage.

The most recent models, AP8 for protons (Sawyer and Vette, 1976) and AE8 for electrons (NASA, n.d.), permit long-term average predictions of trapped particle fluxes encountered in any orbit; they currently constitute the best estimates for the trapped radiation belts. However, statistics associated with random fluctuations and short-term cyclical variations have been averaged out. The

solar cycle dependence is reflected by the average conditions for the solar minimum and solar maximum activity phases of the 11-year cycle.

The predictions of these models for LEO missions are presented in Figures 1-6 and 1-7. Figure 1-6 gives the integral proton spectra for a circular 500-km, 60-degree-inclination orbit, for both solar minimum and solar maximum conditions. The relative hardness of the LEO proton spectrum should be noted. Between 50 and 500 MeV, the proton flux decreases only by a factor of 4. Figure 1-7 presents the comparable data for the trapped electron environment.

The geosynchronous integral electron spectra, obtained from the AE8-MAX model, are plotted in Figure 1-8. Worst and best cases are shown, corresponding to "parking" longitudes at 160°W ($L = 7.0$), and 70°W ($L = 6.6$), respectively. The flux ratio between the worst and best cases is about 1.8 for electron energies greater than 1 MeV, and 2.3 for electron energies greater than 2 MeV.

The proton spectrum at GEO, in contrast to that of LEO, is very soft and essentially is depleted for proton energies greater than 1.75 MeV. Thus, trapped protons in GEO are stopped by very small material thicknesses (approximately 0.05 mm of aluminum) and are not of concern to the internal electronics.

1.4.1.3 Trapped Radiation Variations

The trapped particle fluxes respond to changes in the geomagnetic field induced by solar activity and, therefore, exhibit a strong dynamic behavior, especially in the outer belts. Satellite measurements in geosynchronous equatorial orbits have revealed a complicated temporal pattern consisting of the superposition of several cyclical variations in conjunction with sporadic fluctuations (Lanzerotti, Roberts, and Brown, 1967; Lin and Anderson, 1966; O'Brien, 1963). The main periodic variations include a diurnal cycle, which in GEO is characterized by order-of-magnitude electron flux changes, and the 11-year solar activity cycle.

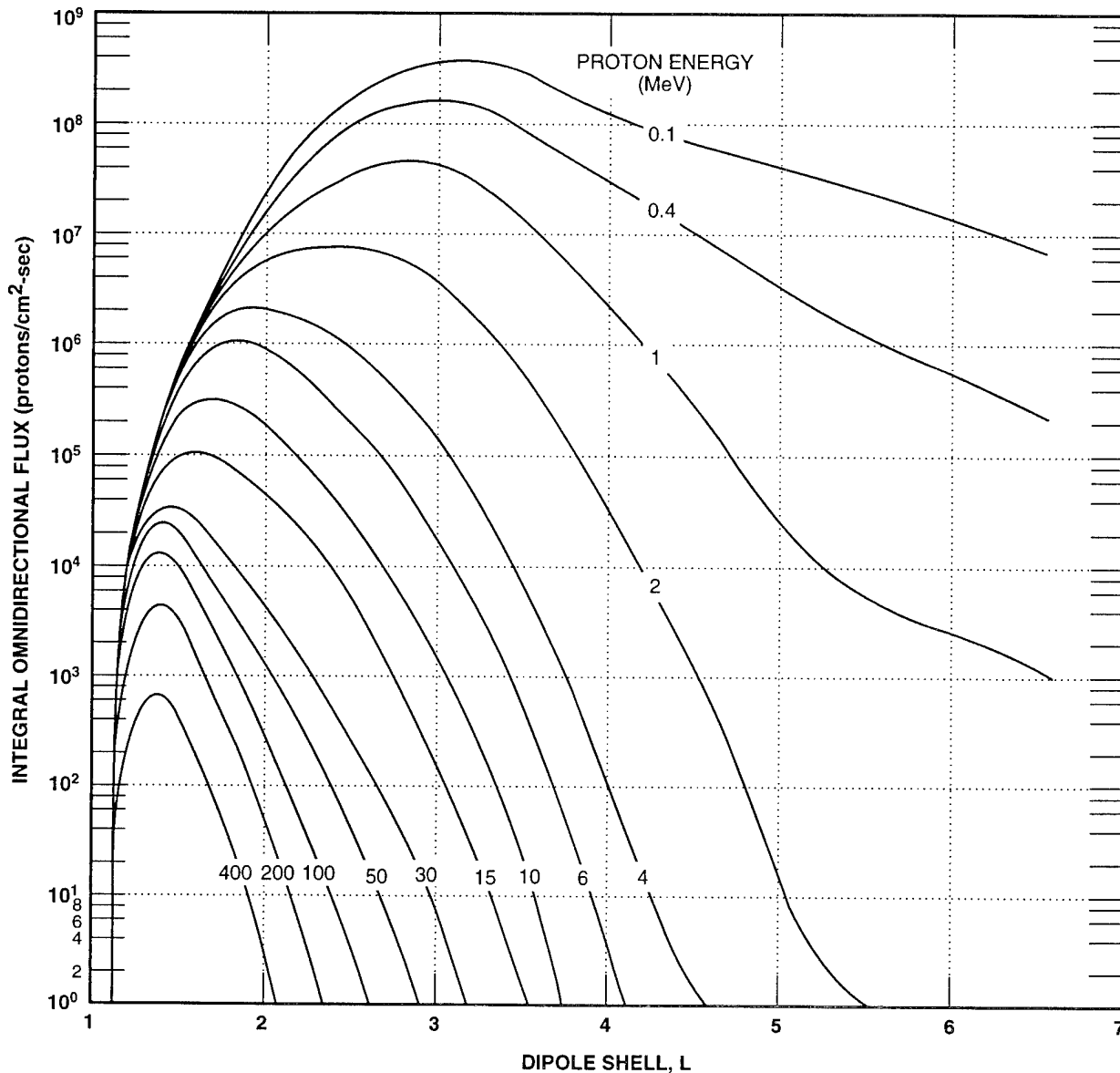


Figure 1-5. Equatorial radial profiles for proton fluxes (Stassinopoulos and Raymond, 1988).

Sporadic magnetic storms in GEO can produce a modulation of the electron flux above 50 keV by an order of magnitude within a period of less than 10 minutes (Lin and Anderson, 1966), and with a corresponding decay in days. Substorms, which are a common feature of the midnight-to-dawn sector of a GEO orbit, result in the injection of electrons with energies between 50 and 150 keV from the magnetospheric tail region.

Another important solar-activity-induced modulation of the trapped particle population, particu-

larly protons, occurs in the low-altitude regime of the magnetosphere. Here, during the active phase of the solar cycle, the increased energy output from the sun causes the atmosphere to expand, thereby raising the density of the atmospheric constituents normally encountered at heights between 200 and 1,000 km.

The solar-cycle variations observed in some areas of the trapped particle domain are functions of energy and magnetic parameter L . They gener-

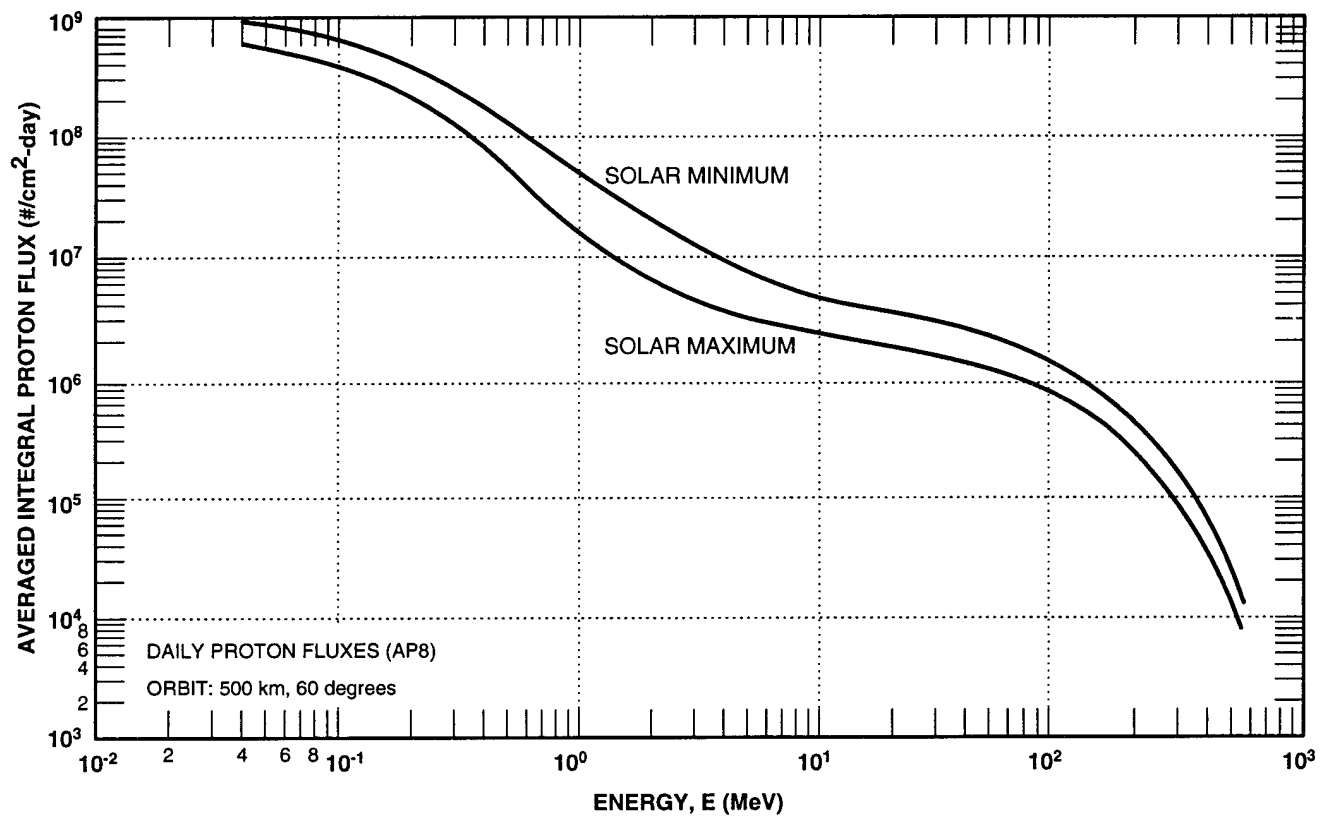


Figure 1-6. Low-earth orbit proton fluxes, composite spectra (Stassinopoulos and Raymond, 1988).

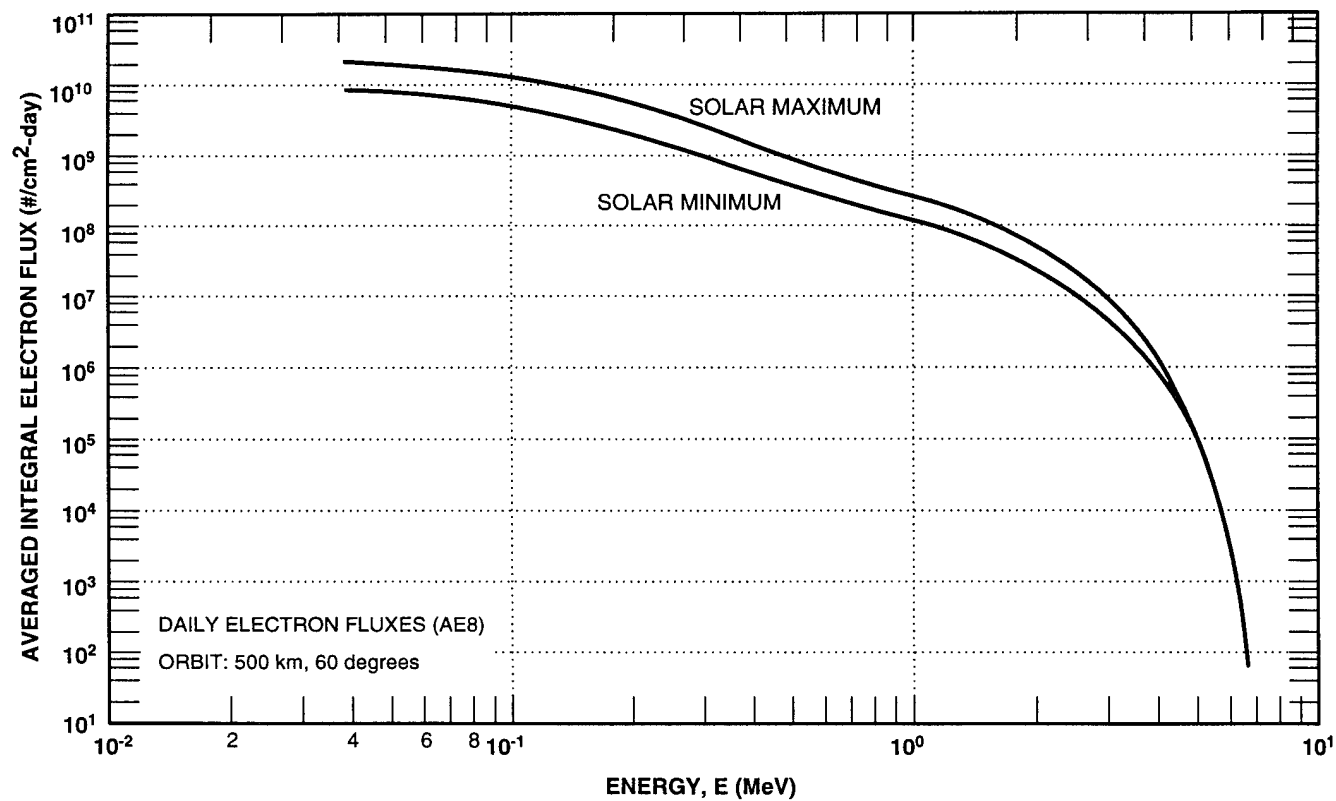


Figure 1-7. Low-earth orbit electron fluxes, composite spectra (Stassinopoulos and Raymond, 1988).

ally have opposite effects on each particle specie, particularly in the low-altitude regime:

	Solar Minimum	Solar Maximum
Electron Intensities	Lower	Higher
Proton Intensities	Higher	Lower

No solar-cycle changes of consequence have been measured in the heart of the proton trapping domain. No significant long-term variations, within current models, occur in the electron populations at geostationary altitudes. However, in the atmospheric cutoff regions, electron and proton populations may vary by as much as a factor of 5.

1.4.1.4 Flux-Free Time

As mentioned previously, the SAA is a region of trapped particle radiation close to the earth. Hence, for low-altitude, low-inclination orbits, the SAA is the most important factor in determining the level of radiation exposure for spacecraft. For LEO with higher inclinations (> 30 degrees) the protrusions of the outer-zone electron belts (the electron “horns”) in the midlatitude regions must also be considered. Of particular importance is the temporal distribution of the proton exposure, which determines the maximum rate of potential proton-induced single-event upsets (SEU) in electronics, as well as the periods during which no upsets are observed.

The intermittent exposure of LEO satellites to the trapped Van Allen belt radiation is illustrated for electrons in Figure 1-9 for a circular 900-km, 99-degree-inclination orbit during its worst pass through the SAA. Note in Figure 1-9 that even in a worst-case pass, there are time periods during which instantaneous electron fluxes above 0.5 MeV are below 1 particle/cm²-sec. The same periods are the “flux-free time” (FFT) intervals, which may occur over short orbit segments (partial FFT per period) or over the entire length of a revolution (total FFT per period). In terms of geomag-

netic geometry, FFT establishes the duration for which the trajectory lies outside the trapping domain of the corresponding particle species, evaluated at the given energies.

1.4.1.5 Artificial Enhancement

A severe hazard for space missions could be introduced by a high-altitude nuclear explosion. Such an effect would result in the injection into the magnetosphere of energetic electrons from the beta

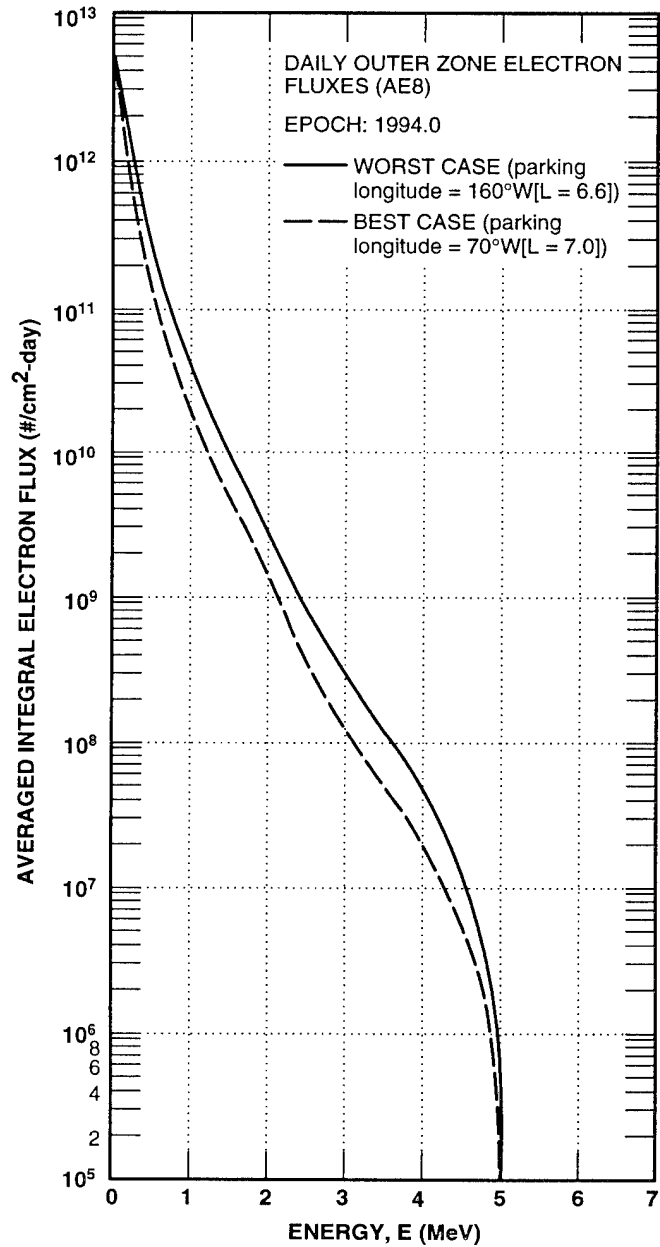


Figure 1-8. Geostationary electron spectra (Stassinopoulos and Raymond, 1988).

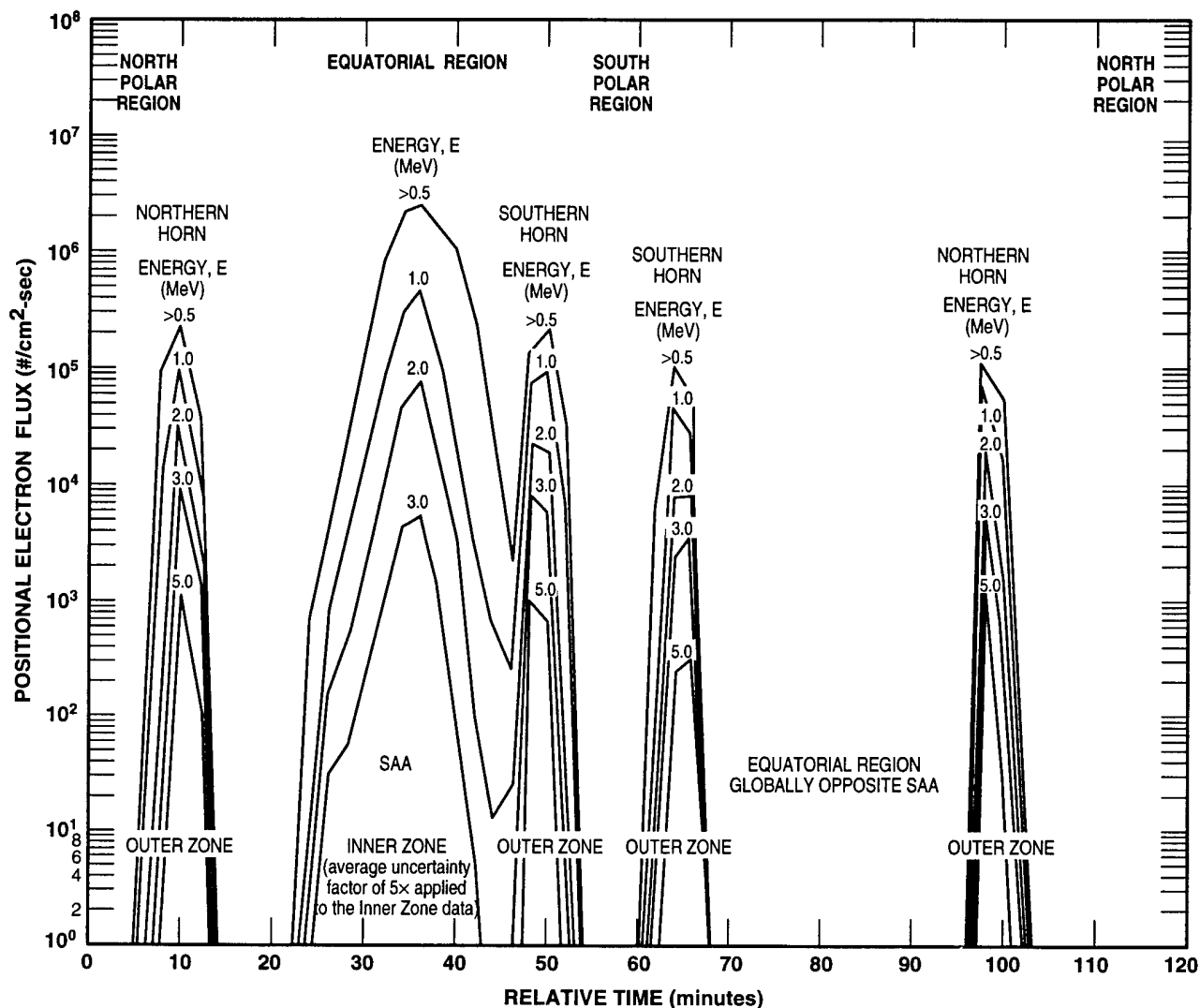


Figure 1-9. Electron flux profile for a worst-case pass through the South American anomaly; circular 900-km, 99-degree-inclination orbit (Stassinopoulos and Raymond, 1988).

decay of fission fragments. Subsequent trapping of the electrons in the magnetic field (Teague and Stassinopoulos, 1972) could produce an enhancement of the electron population by many orders of magnitude.

The principal hazard would be to LEO missions mainly because very stable trapping is expected, with anticipated lifetimes of up to 8 years (Teague and Stassinopoulos, 1972). Figure 1-10 shows the isochronal contours for the trapped electrons resulting from the Starfish atmospheric nuclear explosion over Johnston Island in the Pacific (July 1962). Typical nuclear enhanced electron doses as a function of LEO altitude (60° inclination) are

shown in Figure 1-11. Doses are given for 180 days behind a 100-mil aluminum slab shield. Doses are given for 20 kt, 100 kt, and 1.5 - 15 Mt nuclear detonations at optimum burst height over the equator. Nuclear bursts over other regions produce similar enhancement but with doses lower than those indicated in Figure 1-11 (Wenaas, 1991).

Depending on the location of the explosion, the injection could also produce a temporary enhancement of the electron environment at geostationary orbits. At GEO, the trapping would be less stable, with exponential decay periods of between 10 and 20 days. The apparent longevity (or conversely, the

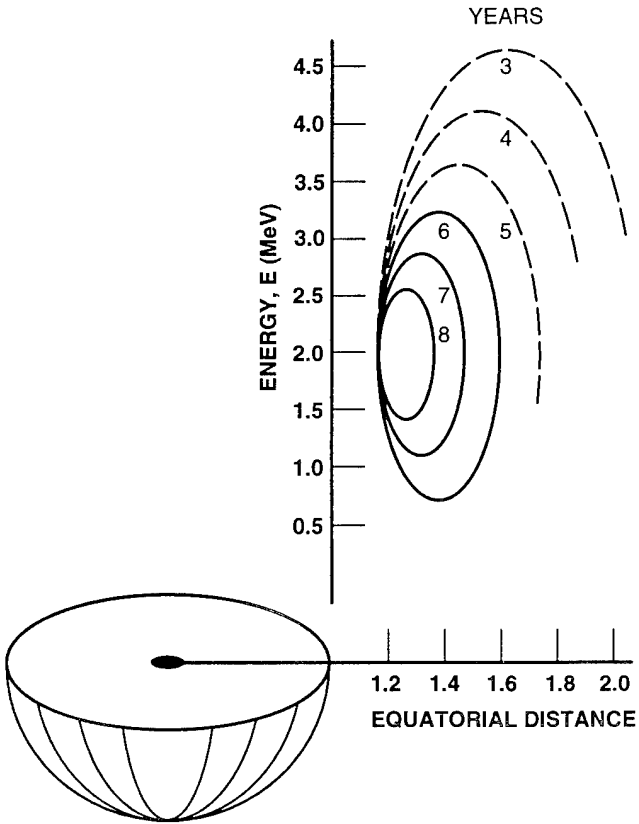


Figure 1-10. Isochronal contours for electron longevity following the Starfish nuclear detonation in July 1962 (Teague and Stassinopoulos, 1972).

decay rate) of such fission electrons depends to a large extent on the injection latitude and altitude; that is, it is a function of the magnetic dipole shell parameter L and, to a lesser degree, of magnetic field strength (Stassinopoulos and Verzariu, 1971). An example of nuclear-detonation induced dose enhancement at GEO orbits is shown in Figure 1-12 for a 100 kt burst and nuclear-saturated electron belts. While significant enhancement of the 180-day dose is noted for the case of saturated belts, near-earth nuclear detonations only add small doses to the natural radiation environment (Rogers, 1993).

For internal electronics, it is important to note that both the total ionizing exposure level and exposure dose rate are substantially increased by the artificially enhanced environment.

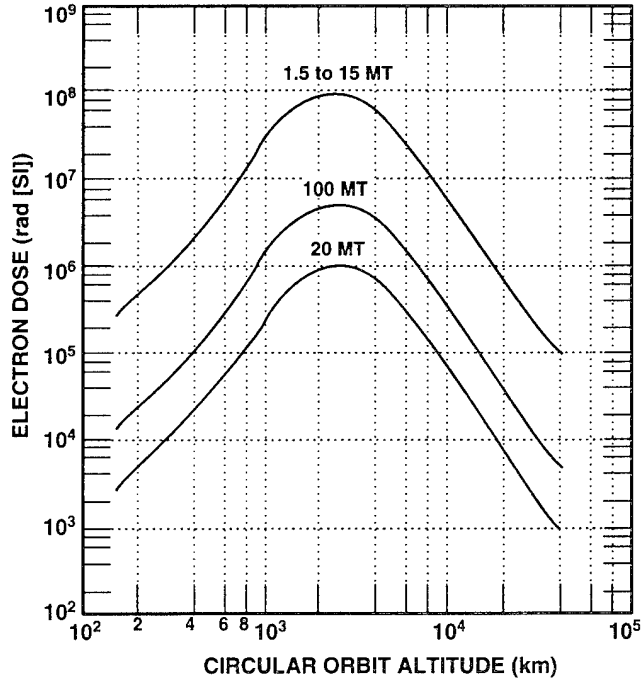


Figure 1-11. Electron dose (180 day) in LEO orbits as a function of altitude enhanced by the nuclear detonations shown (Wenaas, 1992).

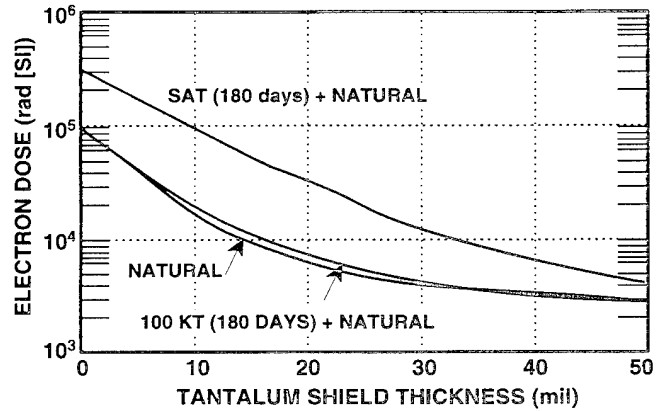


Figure 1-12. Ten-year doses in GEO orbit enhanced by a 100 kt nuclear burst with saturated belts. Doses are behind a 100 mil aluminum slab shield augmented by the Ta shielding shown (Rogers, 1993).

1.4.1.6 Emerging Radiation

In interacting with spacecraft materials, the electrons and protons of the trapped radiation belts are modified in intensity by shielding and in character through the production of secondary radiation. The secondary radiation can extend the penetration of the primary radiation and lead to an increase in

dose deposition over that of the attenuated incident radiation. The most significant secondary radiation is the bremsstrahlung, or "braking radiation," produced in the deceleration of electrons penetrating the spacecraft. This continuous x ray spectrum is emitted roughly in the direction of electron penetration and its mean energy is about one-third of the initial electron energy. The bremsstrahlung intensity depends linearly on the atomic number (Z) of the spacecraft material and on the square of the initial electron energy. Bremsstrahlung from energetic electrons populating the radiation belts is very penetrating, and thus difficult to attenuate, especially with the low- Z materials commonly used on spacecraft (e.g., aluminum). On the other hand, these low- Z materials tend to produce less bremsstrahlung.

Electrons and Bremsstrahlung. To illustrate, Figure 1-13 and 1-14 show the merging electron and bremsstrahlung spectra behind spherical aluminum shielding for the incident environment of a circular 500-km, 60-degree inclination orbit. As the curves of Figure 1-13 clearly indicate, the trapped electrons are effectively attenuated by the aluminum shield, and nearly all are stopped by thicknesses greater than 0.2 g/cm^2 , even at the highest electron energies. However, as shown in Figure 1-14, the bremsstrahlung flux levels for energies above 70 keV are not significantly affected by the aluminum shielding from 0.1 to 10 g/cm^2 . It is important to note, however, that above 100 keV, the photon fluxes are, on the average, over three orders of magnitude lower than the incident electron flux at corresponding energy levels.

Trapped Protons. The transport of trapped protons is illustrated in Figure 1-15, which shows the emerging proton spectra behind various spherical aluminum shield thicknesses for a circular 500-km, 60-degree-inclination orbit. As shown, the aluminum shielding is very effective for low energy protons, but ineffective for high-energy ($> 30 \text{ MeV}$) protons. The shielding effectiveness of low proton energies is important in reducing ionizing energy deposition in the internal electrons. On the other hand, hardening the proton spectra provides

little help in reducing potential proton-induced SEUs.

1.4.1.7 Ionizing Radiation Dose

To illustrate the ionizing dose exposure, daily dose values for LEO and GEO are presented in Figures 1-16 through 1-18. The materially attenuated doses and fluxes presented were calculated with state-of-the-art transport codes (Jordan, 1982; Seltzer, 1980).

Daily silicon doses in LEO at 500-km altitude and 60-degree inclination for solar minimum and maximum, are shown in Figure 1-16 for a two-sided (4π) exposure of aluminum slab shields, and for a solid spherical shield averaged over 15 orbits. The electron dose includes the bremsstrahlung contribution.

As discussed previously, the SAA is the primary contributor to doses accumulated by spacecraft in LEO. Figure 1-17 shows electron plus bremsstrahlung dose contours at an altitude of 500 km for a spherical aluminum shield thickness of 0.2 g/cm^2 . Superimposed on the world maps are the worst-case passes thorough the SAA for 28.5-, 57-, and 90-degree-inclination orbits. As mentioned previously, for low-inclination orbits (< 45 degrees), there are periods when complete revolutions are in flux-free time.

The corresponding electron-plus bremsstrahlung daily dose for an aluminum shield of solid-sphere geometry in GEO at the parking longitude, with the lowest average flux (70°W), is illustrated in Figure 1-18 in the form of a dose-depth curve. For the parking longitude with the large average flux (160°W), the dose behind a 2-g/cm^2 shielding thickness is a factor of about 1.7 higher; this is true for all shield geometries.

The ten-year total doses for some typical LEO and GEO orbits are shown in Figures 1-19 and 1-20. These curves are useful for estimating the total dose encounters for typical circular and elliptic orbits. These curves were calculated using the AP8 and AE8 models for spherical (Figure 1-19) and slab shielding conditions.

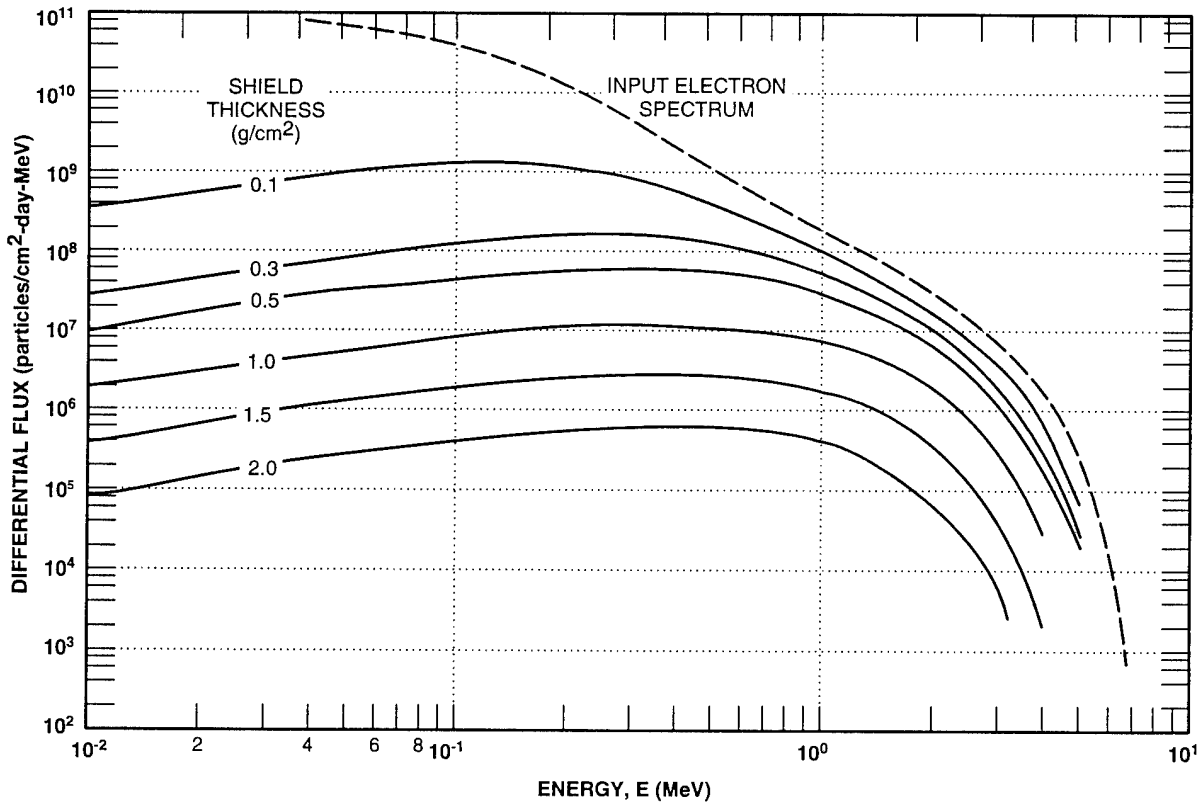


Figure 1-13. Emerging electron spectra behind various thicknesses of spherical aluminum shields; circular 500-km, 60-degree orbit at solar minimum, BL time = 1998.0 (Stassinopoulos and Raymond, 1988).

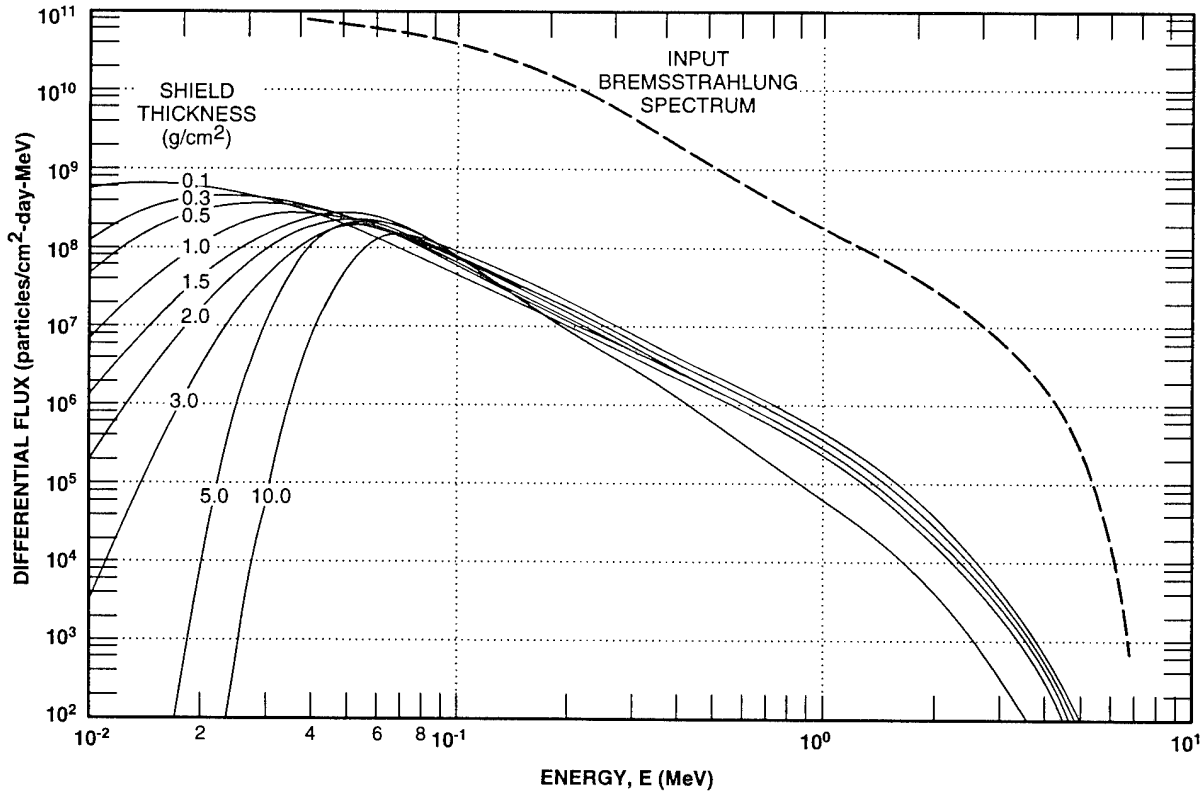


Figure 1-14. Emerging bremsstrahlung spectra behind various thicknesses of spherical aluminum shields; circular 500-km, 60-degree orbit at solar minimum, BL time = 1998.0 (Stassinopoulos and Raymond, 1988).

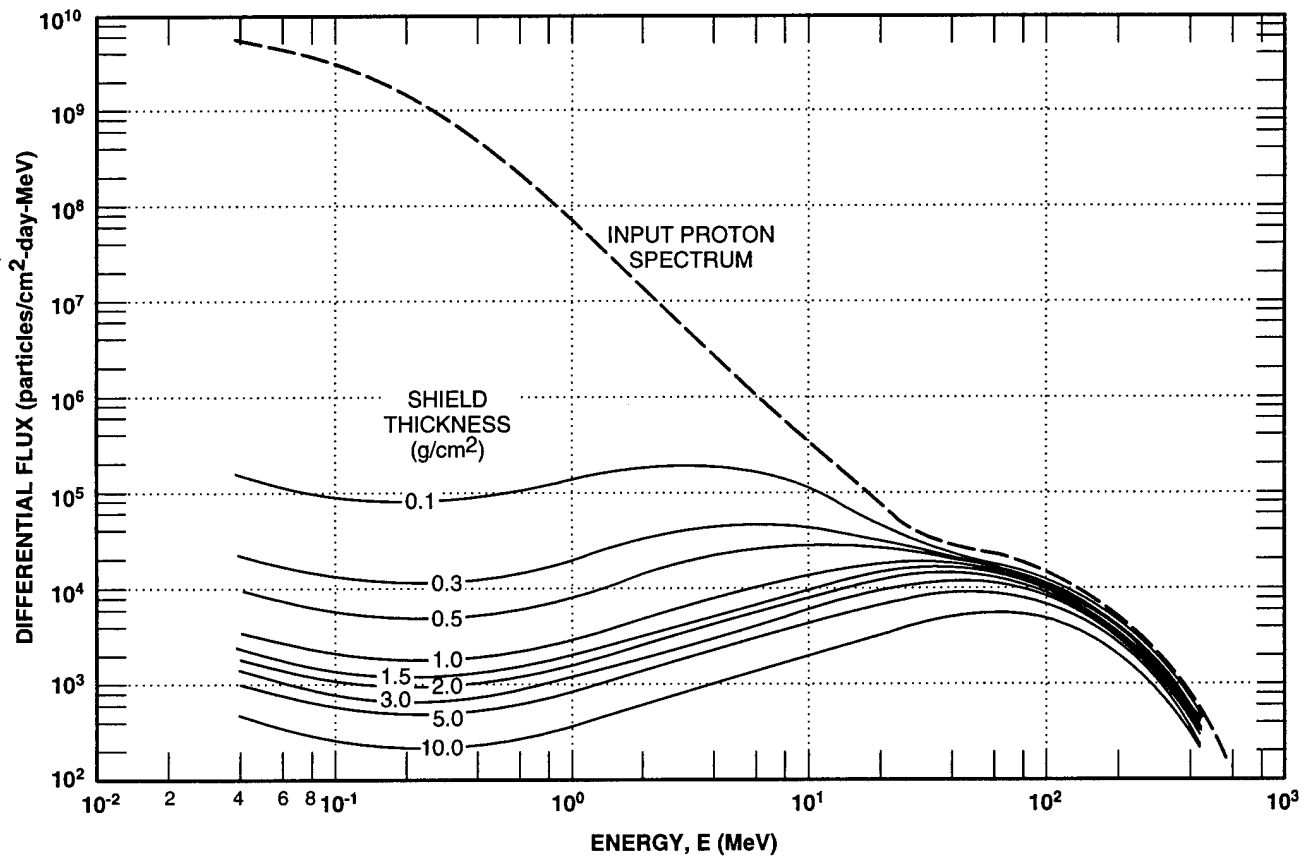


Figure 1-15. Emerging trapped proton spectra behind various thicknesses of spherical aluminum shields; circular 500-km, 60-degree orbit at solar minimum, BL time = 1998.0 (Stassinopoulos and Raymond, 1988).

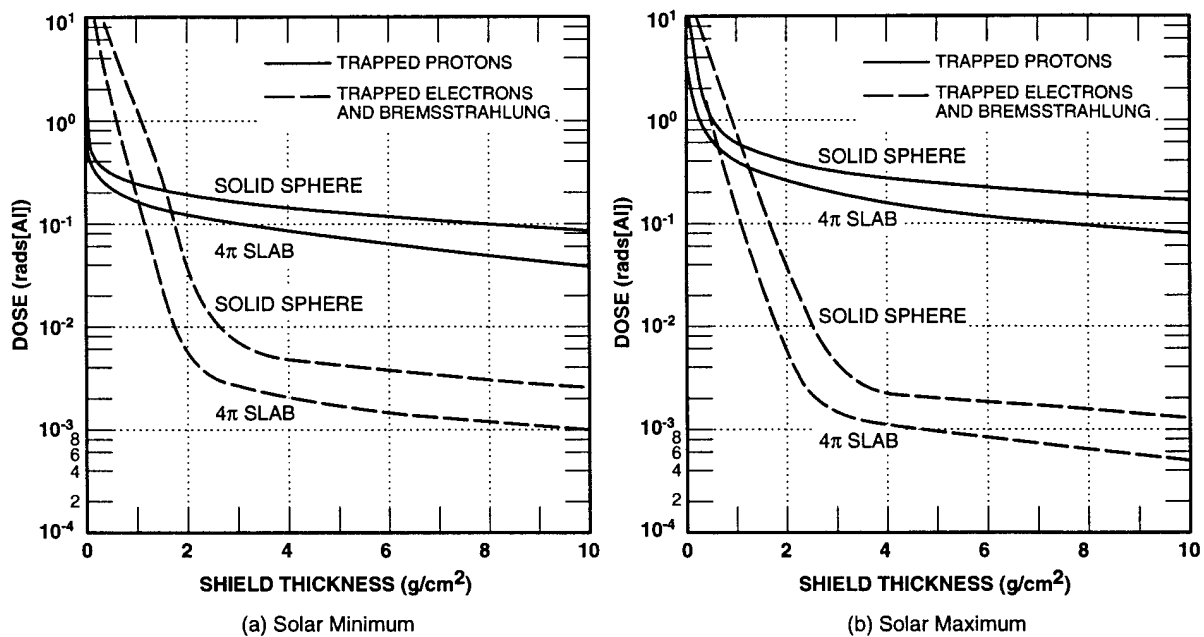


Figure 1-16. Daily doses for LEO (500-km, 60-degree orbit); silicon target, aluminum shield (Stassinopoulos and Raymond, 1988).

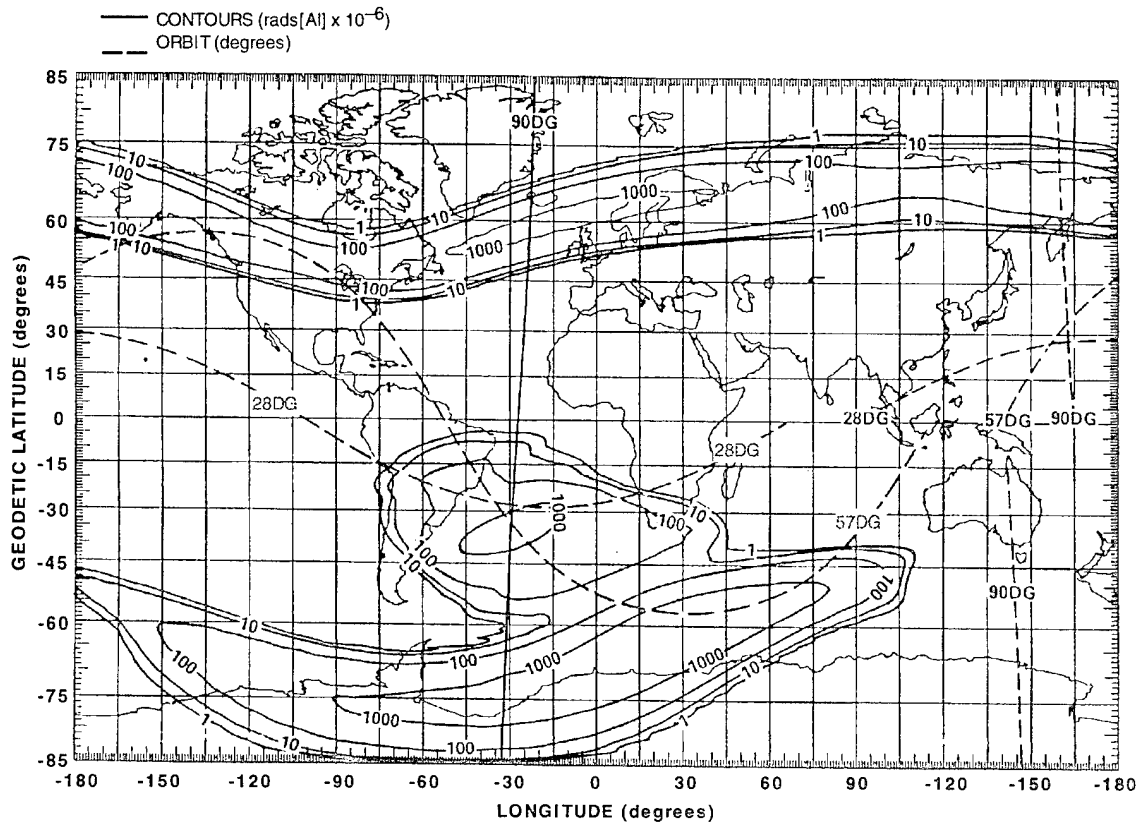


Figure 1-17. World map contours of total electron plus bremsstrahlung dose (rads/ μ sec) at 500-km altitude for a spherical aluminum shield thickness of 0.2 g/cm^2 , BL time = 1964 (Stassinopoulos, 1990).

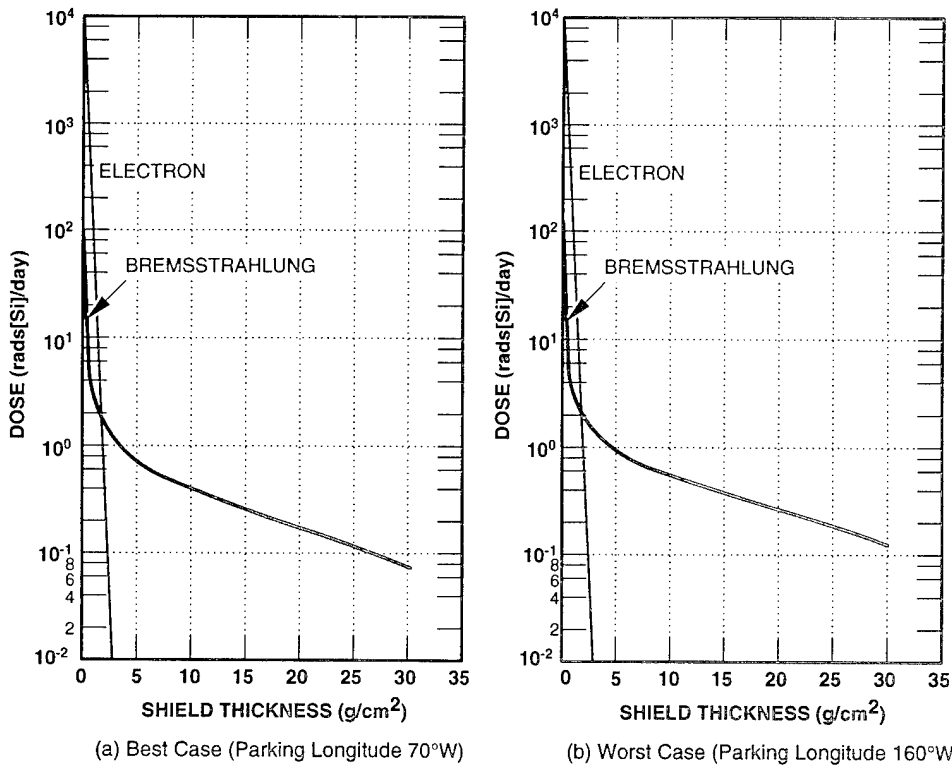


Figure 1-18. Daily electron doses for GEO for a silicon target behind solid-sphere aluminum shielding (Stassinopoulos and Raymond, 1988).

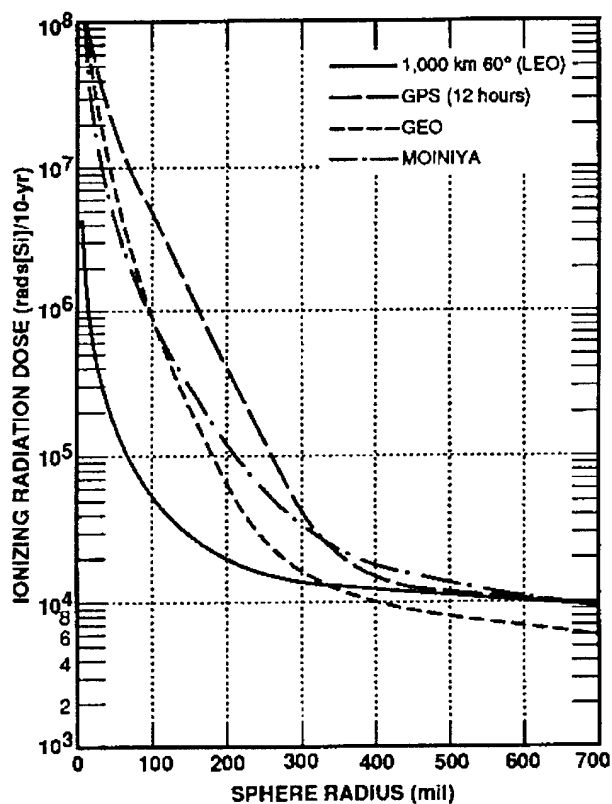


Figure 1-19. Ten year total dose for various typical orbits at the center of aluminum sphere based on AP8/AE8 models (Hopkins, 1993).

The topic of damage to semiconductor devices resulting from both ionizing and non-ionizing radiation events is covered in more detail in subsequent chapters of this handbook. However, a brief discussion of these effects is provided here to assist in understanding the discussion of both the natural space radiation environment and nuclear weapon effects on semiconductor devices.

1.4.1.8 Susceptibility of Electronics to Permanent Damage

The basic permanent damage mechanisms in semiconductor devices exposed to high-energy electrons and protons are accumulated ionization effects and atomic displacements in bulk semiconductors. Effects of electron exposure in virtually all modern microcircuits are dominated by accumulated ionization. Definition of the internal ionizing radiation environment in terms of rads(Si) is generally adequate. Failure levels resulting from accumulated ionization can be as low as approxi-

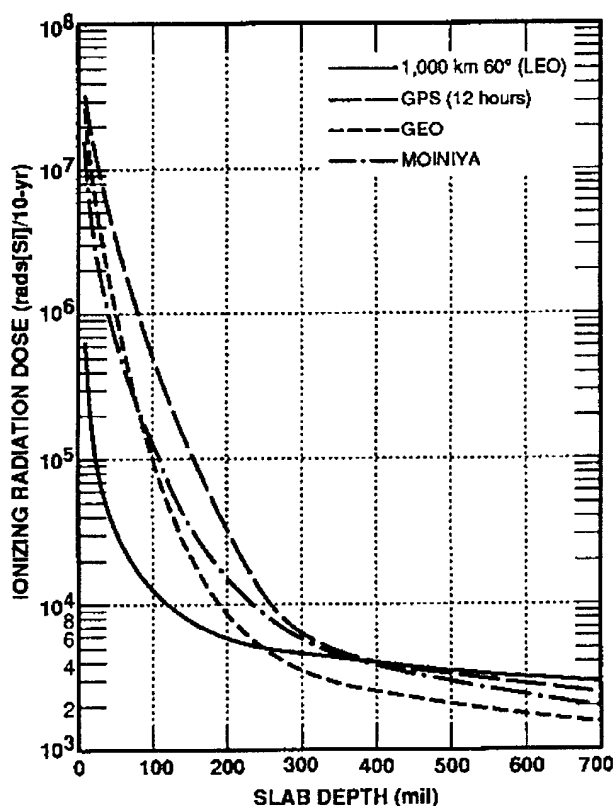


Figure 1-20. Ten year total dose for various orbits behind a semi-infinite slab based on AP8/AE8 models (Hopkins, 1993).

mately 1,000 rads(Si) for commercial microcircuits, or greater than 10 Mrads(Si) for hardened microcircuits.

Effects of proton exposure over the energy range of interest in the space environment include both ionization and displacement damage (Petersen, 1981). Failure levels resulting from proton-induced displacement damage can be as low as 1×10^{10} particles/cm² for sensitive bipolar analog microcircuits, power transistors, or CCD imagers. The definition of the proton environment for the internal electronics should include both the proton-induced ionization (in rads[Si]), and the internal proton fluence and energy spectra for displacement effects.

Single-Event Susceptibility of Electronics.

Single-event phenomena (SEP) in semiconductor electronics will be discussed in detail in Chapter 3 of this handbook. However, for the purposes of this discussion, SEP is defined as the nonperma-

ment upset of the state of an electronic circuit (e.g., $1 \text{ } \bar{A} \text{ } 0$ or $0 \text{ } \bar{A} \text{ } 1$) caused by the deposition of a critical amount of charge at the information node (e.g., memory cell or a bistable flip-flop).

The high-energy protons of the trapped space radiation environment can cause single-event effects (SEE) in modern semiconductor electronics. The proton energy threshold for these effects is approximately 10 MeV, with the cross section for nuclear reactions increasing substantially at 30 MeV and above (Raymond and Petersen, 1987). Typically, a nuclear reaction resulting in a single event occurs on the order of once every 100,000 protons. In terms of microcircuit susceptibility, for a 60-degree orbit, the maximum proton-induced upset rate occurs in the heart of the proton-trapping domain of the radiation belts at an altitude of approximately 2,600 km. It has been estimated that for electronics with "typical" shielding, the SEU rate could be as high as 0.1 upset/bit-day for susceptible microcircuit technologies, decreasing by at least five orders of magnitude for tolerant microcircuit technologies (Bendel and Petersen, 1983).

At low-altitude, low-inclination orbits, the proton-induced SEU rate is determined by passages through the SAA. During FFT, the electronics will be free from trapped-proton SEUs.

1.4.2 Transiting Radiation

The transiting radiation of the space radiation environment is composed of a solar contribution and a galactic contribution. Each is composed of high-energy protons and heavy ions. In terms of the spacecraft electronics, the dominant effects are those associated with the ionization tracks of single particles, as well as the effects of total accumulated ionization. As with the trapped radiation environment, the external environment will be presented, followed by a discussion of the internal environment, and finally transiting radiation effects in spacecraft electronics will be addressed.

1.4.2.1 Solar Cosmic Rays

Solar Flare Protons. Disturbed regions on the sun sporadically emit bursts of energetic charged

particles into interplanetary space. These solar energetic particle events (usually occurring in association with solar flares) are composed primarily of protons, with a minor constituent of alpha particles (5 to 10 percent), heavy ions, and electrons. The emission of protons from a solar energetic particle event can continue for as long as several days.

The time history of energetic solar flare particles as they arrive at the earth after the occurrence of the parent flare has several important characteristics. First, the particles arrive in tens of minutes to several hours (depending on their energy and point of origin on the sun); second, they peak within 2 hours to 1 day; and third, they decay within a few days to 1 week. It is important to note that the most energetic protons arrive at the earth in about 10 to 30 minutes.

Solar energetic particle event phenomenology is distinguished by ordinary events and anomalously large events. Anomalously large events are quite rare. Figure 1-21 shows the energetic solar flare proton events since 1956. As shown, three anomalously large events occurred during solar cycle 19, one during cycle 20, and none in cycle 21 (Goswami *et al.*, 1987). Anomalously large events are those having proton fluences $> 10^{10}$ particles/cm². They usually occur near the first and last year of the solar maximum phase. The prediction of anomalously large events was initially based on an empirical model (Stassinopoulos and King, 1974), and later on a probabilistic treatment involving modified Poisson statistics (King, 1974). A simple statistical predictive model for solar flares is provided by SOLPRO (Stassinopoulos, 1975), which is based exclusively on satellite spectral measurements that nearly cover solar cycle 20 entirely. This model predicts, for a given mission duration and a specified confidence level, the mission-integrated proton fluence spectrum from ordinary events and the expected number of anomalously large events with their event-integrated fluence spectra. In terms of proton fluence, since anomalously large events are rare, small-sample statistics are the only appropriate prediction technique. Thus, for spacecraft mission

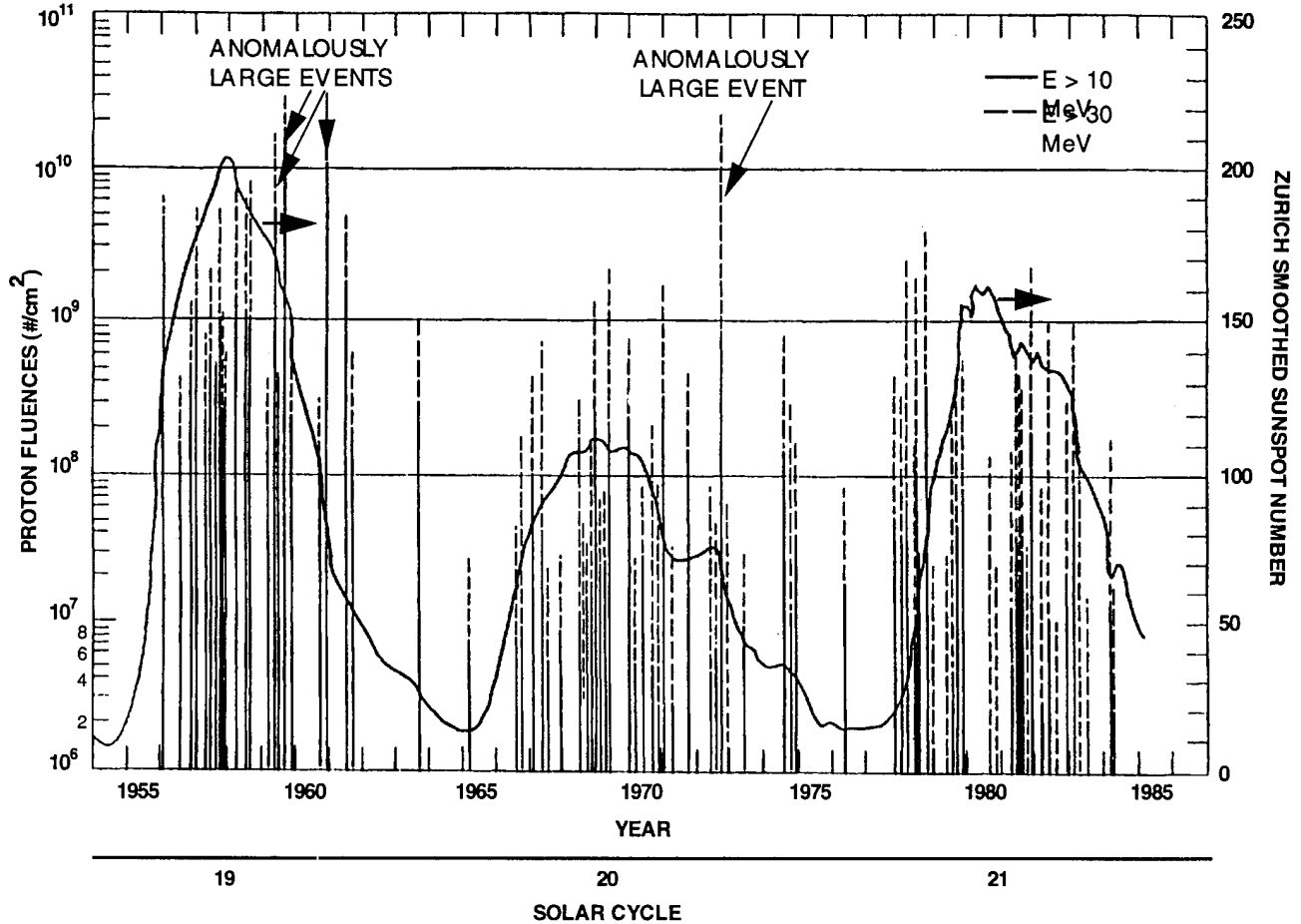


Figure 1-21. Solar flare proton events for solar cycles 19, 20, and 21 (Stassinopoulos and Raymond, 1988).

durations longer than one year, ordinary event fluences are insignificant because probability theory predicts the occurrence of at least one anomalously large event, even for a confidence level as low as 80 percent.

Solar Heavy Ions. For ordinary solar flare events, the relative abundance of the helium ions in the emitted particle fluxes is usually between 5 and 10 percent, while the fluxes of heavier ions are very small and significantly below the galactic background. However, during major solar events, the abundance of some heavy ions may increase rapidly by three or four orders of magnitude above the galactic background for periods of several hours to days. The increased flux of the heavy ions can have serious consequences in terms of an increased frequency of single-event effects within the spacecraft electronics.

1.4.2.2 Galactic Cosmic Rays

The region outside the solar system in the outer part of the galaxy is believed to be uniformly filled with cosmic rays, which consist of ~ 85 percent protons, ~ 14 percent alpha particles, and ~ 1 percent heavier nuclei. The galactic cosmic rays range in energy to greater than 10 GeV/nucleon. Figure 1-22 shows the spectral distributions for hydrogen, helium, carbon, and oxygen ions. The differential energy spectra of the cosmic rays near the earth tend to peak around 1 GeV/nucleon. Toward lower energies, the spectral shape is depressed by interactions with the solar wind and the interplanetary magnetic field. This reduction in flux becomes more pronounced during the active phase of the solar cycle. The total flux of cosmic-ray particles seen outside the magnetosphere at the distance of the earth from the sun (i.e., 1 astro-

nomical unit) is approximately $4/\text{cm}^2\text{-sec}$ (primarily composed of protons). For all practical purposes, the cosmic-ray flux can be considered as omnidirectional, except for very-low-altitude orbits, where the solid angle subtended by the earth defines a region free from these particles. Figure 1-23 shows the relative abundance of the galactic cosmic-ray ions. A model for these particles is provided in Adams, Silberg, and Tszo (1981).

1.4.2.3 Geomagnetic Shielding

Low-altitude earth orbits are essentially shielded from solar or galactic cosmic rays by the geomagnetic field up to inclinations of about 45 degrees. The earth's field acts as an energy filter, preventing particles with less than given momentum values from penetrating to certain altitude-latitude combi-

nations. Figures 1-24 and 1-25 show the total ion energy required to penetrate the magnetosphere in terms of the dipole parameter L . Figure 1-26 shows the effects of geomagnetic shielding on solar flare protons for high-inclination (greater than 60 degrees) LEO. Figure 1-27 shows the effect of shielding on cosmic-ray silicon atoms for LEO.

For GEO, magnetic shielding is relatively ineffective, and such orbits will be exposed to galactic cosmic-ray hydrogen of energies greater than about 60 MeV, and to heavier ions whose energy exceeds 15 MeV/nucleon.

1.4.2.4 Transport and Shielding

Transiting radiation and shielding evaluation require consideration of shield geometries and evaluation techniques, shield composition, target composition, and dose units.

Solar Flare Protons. Considerations of solar flare proton transport are similar to those previously discussed for trapped protons [Subsection

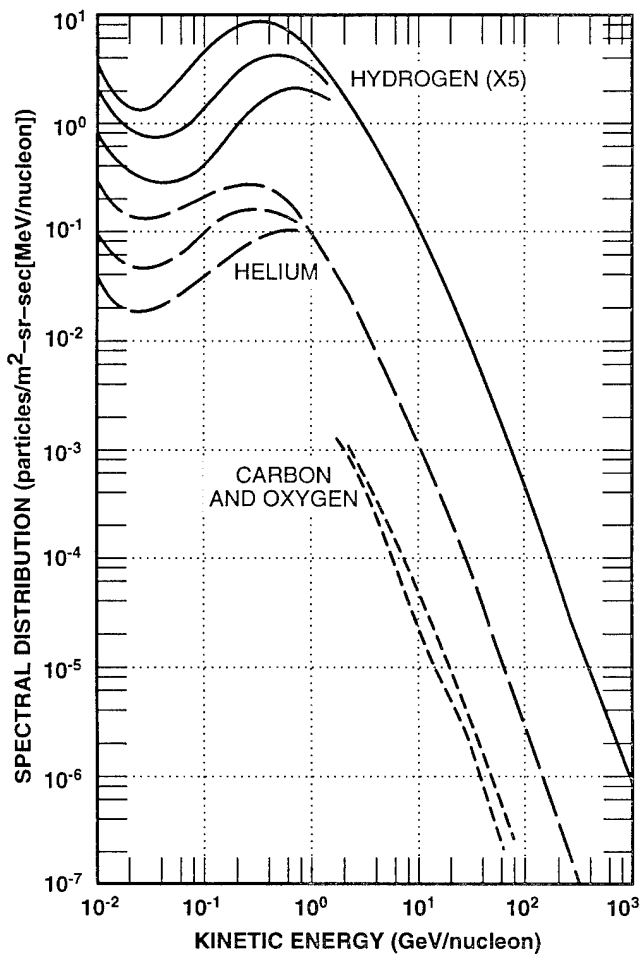


Figure 1-22. Cosmic-ray spectral distributions (Stassinopoulos and Raymond, 1988).

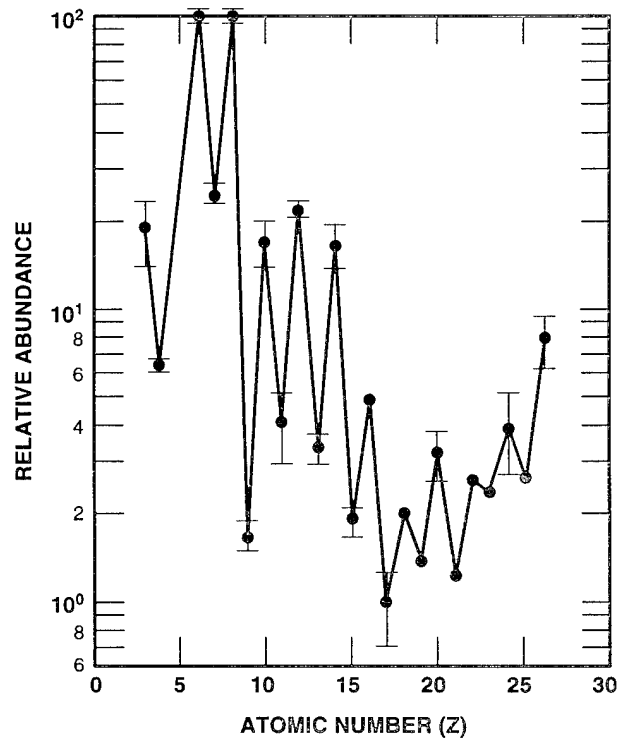


Figure 1-23. Relative abundance of nuclei in galactic cosmic radiation (Stassinopoulos and Raymond, 1988).

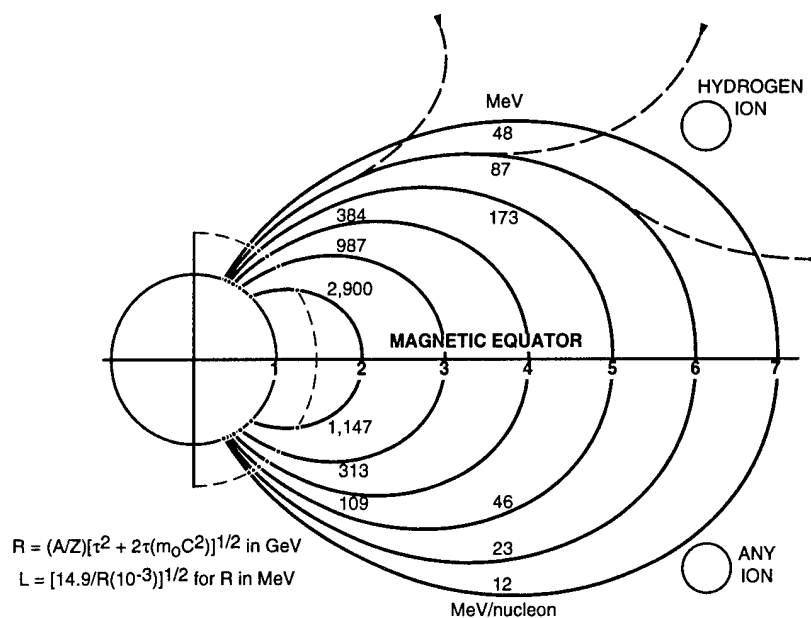


Figure 1-24. Contours of total energy required to penetrate the magnetosphere (Stassinopoulos and Raymond, 1988).

1.4.1.6, "Emerging Radiation"]. The materially attenuated emerging spectra reflect the shielding effect on the distribution of the solar flare protons, as shown in Figure 1-28. The proton fluxes in the 0.1- to 10-MeV range emerging behind spherical aluminum shields of 0.3- to 5-g/cm² thickness are substantial. Particularly relevant to single-particle event effects in electronics is the linear energy transfer (LET) in silicon, defined as the energy deposition per unit length in the active region of the semiconductor device. The LET spectrum for one anomalously large event behind spherical aluminum shields of two thicknesses is shown in Figure 1-29 for the interplanetary solar flare proton spectrum not attenuated by the magnetosphere. Stopping powers (dE/dx) were calculated from the classical equation (Bethe, 1920). The Bethe formula is accurate to about 20 percent at a few million electron volts per nucleon (Littmark and Zeiger, 1980). The error decreases at higher energies, where the assumptions of the Bethe formulation are increasingly valid. At energies below a few MeV per nucleon, the error increases due to unmodeled details of the energy-loss mechanisms.

In general, the ionization loss of a single proton is insufficient to cause a single-event effect in a semiconductor device. Observed single-event effects from proton exposures are the result of the energy deposition of particles produced by nuclear interactions of the incident proton with the target nucleus. The proton threshold energy for these nuclear interactions is approximately 30 MeV (Bendel and Petersen, 1983).

Galactic Cosmic Rays. Figure 1-30 shows the unattenuated interplanetary spectra for silicon cosmic-ray ions, the magnetospherically attenuated orbit-integrated spectra incident on the surface of the spacecraft, and the shielded spectra of emerging particles behind selected thickness of spherical aluminum geometries for a 600-km, 57-degree-inclination orbit. Differential particle fluxes are shown referenced to the left ordinate. The LET spectrum of the silicon ion as a function of energy is referenced to the right ordinate. The LET spectrum is important in defining the energy deposited by a single particle and evaluating subsequent single-event effects in the spacecraft electronics.

In passing through shielding material, nuclear reactions are induced by heavy ions with energies above an effective threshold of a few million electron volts per nucleon. These nuclear reactions provide a source of secondary radiation, both prompt and delayed. Above several hundred million electron volts per nucleon, nuclear reactions surpass atomic ionization as the main attenuation mechanism in material. At higher energies, the interaction of the incident particle tends to occur primarily with individual nucleons in the target

nucleus, and can lead to the ejection of several energetic protons and neutrons. This spallation process leaves the product nucleus highly excited, with de-excitation occurring through the evaporation of additional nucleons and the emission of gamma rays.

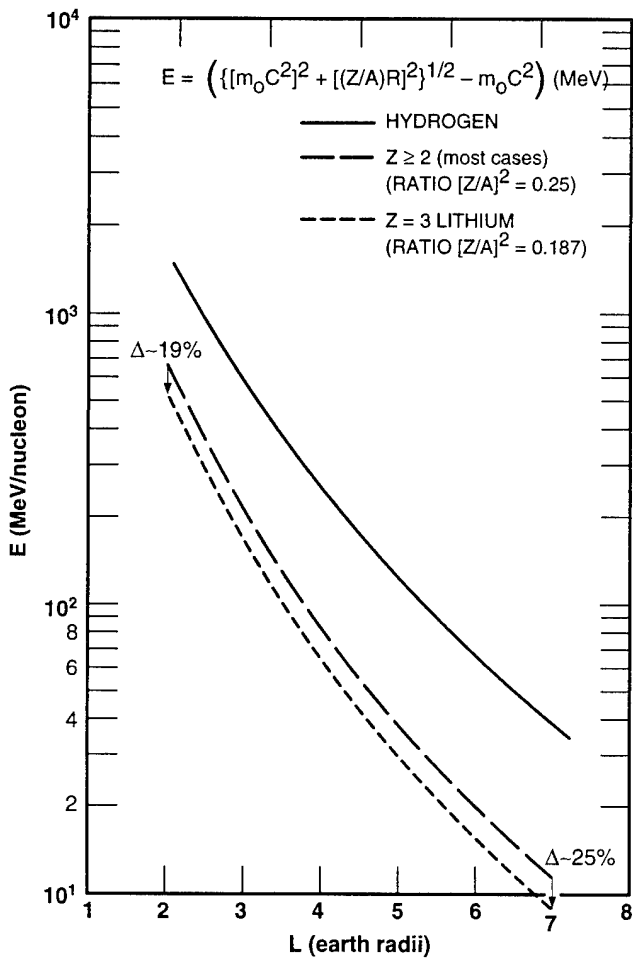


Figure 1-25. Total energy required to penetrate the magnetosphere (Stassinopoulos and Raymond, 1988).

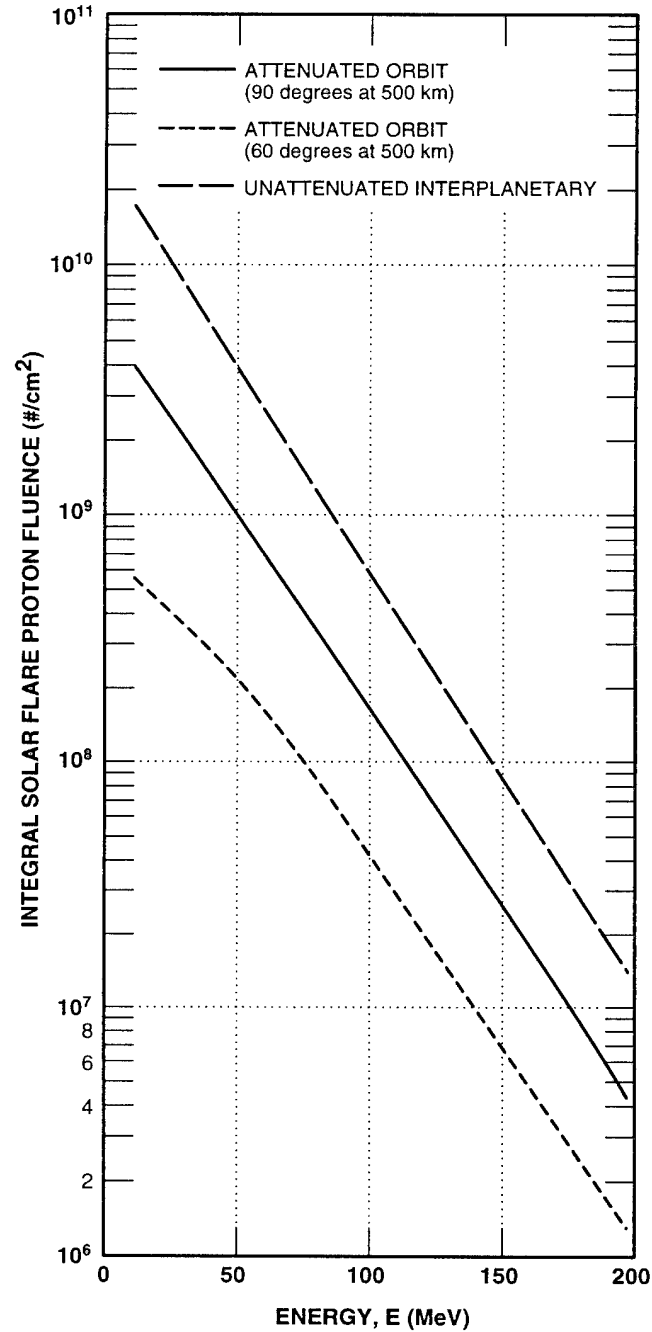


Figure 1-26. Magnetospheric attenuation of solar flare proton spectra for a 500-km high-inclination LEO (Stassinopoulos and Raymond, 1988).

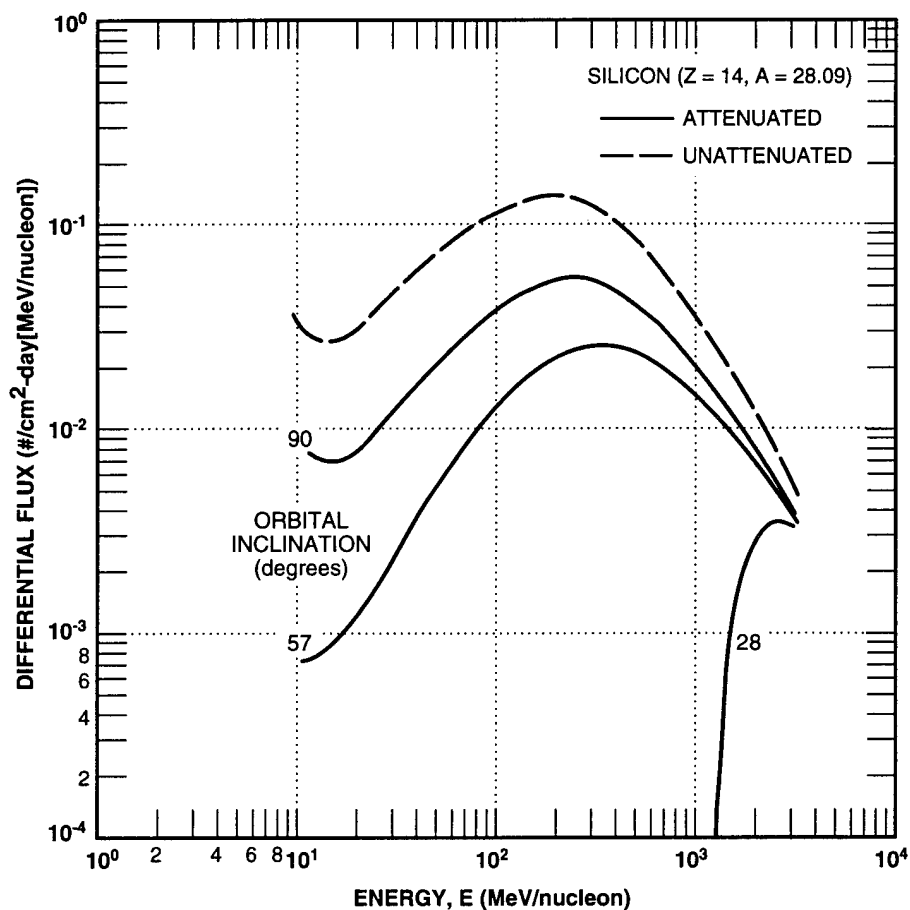


Figure 1-27. Magnetospheric attenuation of cosmic-ray silicon atoms for a 600-km LEO (Stassinopoulos and Raymond, 1988).

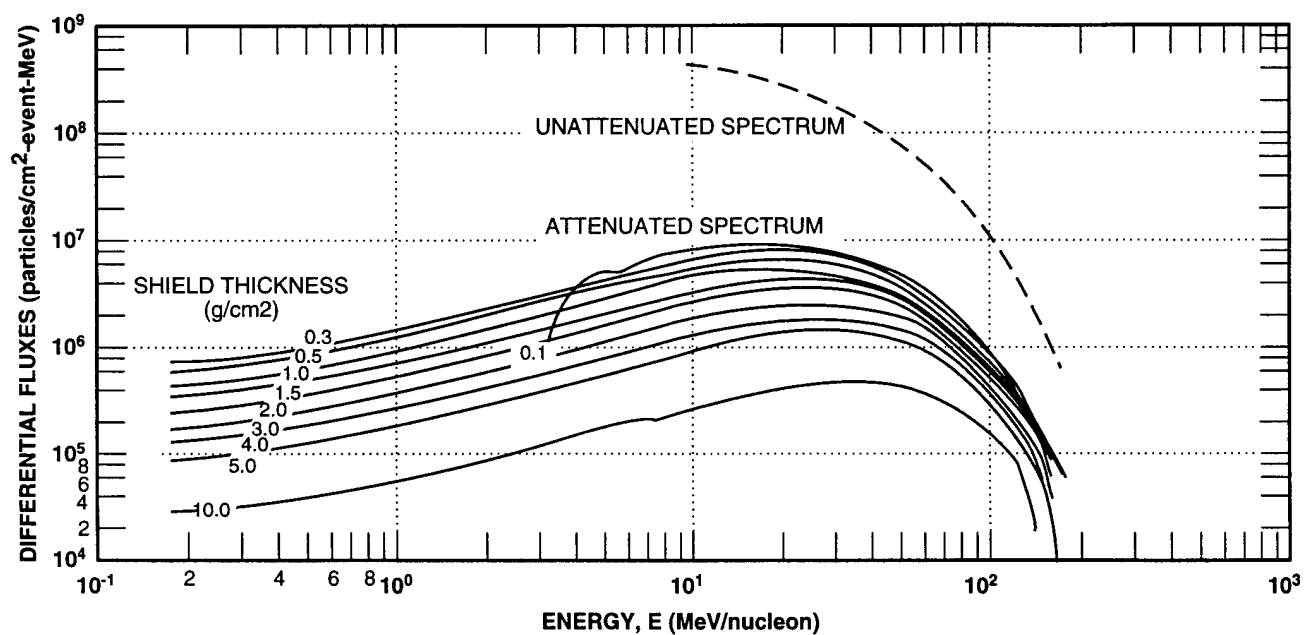


Figure 1-28. Emerging solar flare proton spectra behind various spherical aluminum shield thicknesses; circular 500-km, 60-degree-inclination orbit at solar minimum, BL time = 1998.0 (Stassinopoulos and Raymond, 1988).

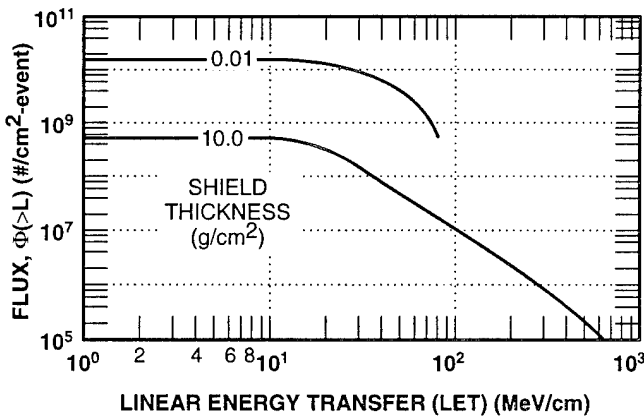


Figure 1-29. Integral LET spectra for the attenuated interplanetary spectrum during one anomalously large event; solar flare protons behind spherical aluminum shields, normal incidence (Stassinopoulos and Raymond, 1988).

For 400-MeV protons incident on aluminum, the average total nuclear emission is 4.8 nucleons, including 2.8 spallation nucleons with an average energy of 120 MeV (Haffner, 1967). The process can generate a rich variety of residual nuclei, especially in heavier elements, as a result of the multiplicity of statistically possible reaction paths (i.e., the specific number of protons and neutrons emitted). These product nuclei frequently are radioisotopes decaying by beta-ray emission with a variety of lifetimes.

Several important features are illustrated by the curves of Figure 1-30. First, there is substantial attenuation by the earth's magnetic field of all particles in the energy range of 10 to 10,000 MeV/nucleon. Second, there is an insignificant effect of thickness of material shielding in the energy range

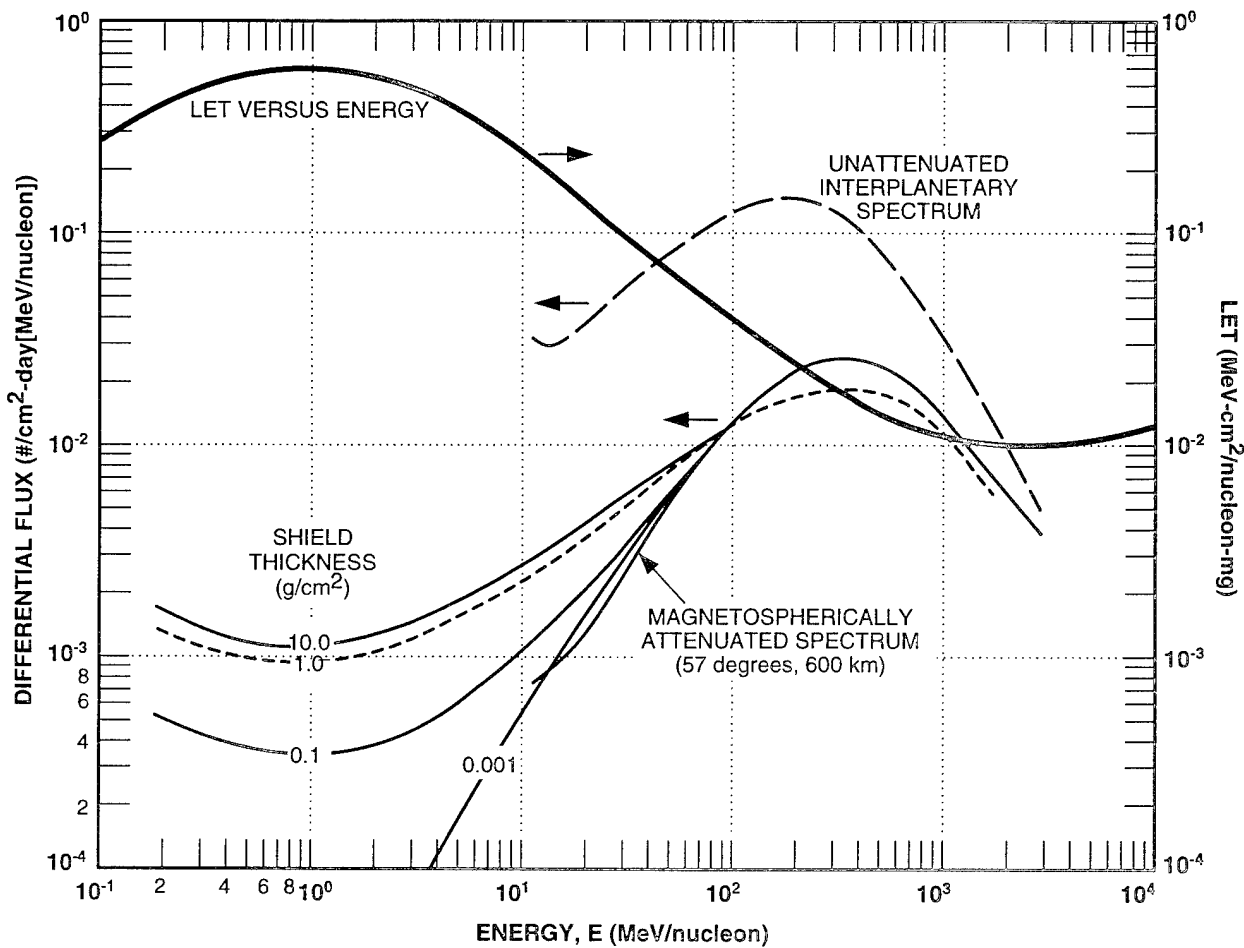


Figure 1-30. Galactic cosmic-ray solar spectra emerging behind spherical aluminum shields of various thicknesses; solar minimum (Stassinopoulos and Raymond, 1988).

from about 90 to 3,000 MeV/nucleon. Note that there is no substantial decrease in flux, even for aluminum shielding of 10 g/cm^2 (approximately 1.5 inches at 3,000 MeV/nucleon). Third, there is an unavoidable shield side effect of a significant increase in the low-energy (0.8 to 50 MeV/nucleon), high-LET fluxes for shield thicknesses greater than 0.1 g/cm^2 of aluminum. With increasing shield thicknesses, the population of high-energy ions decreases slightly, but with a resultant increase in the low-energy ions. Since the LET increases with decreasing energy in this range (heavy solid curve), the presence of the shield actually increases the severity of the environment to the internal electronics.

1.4.2.5 Ionizing Radiation Dose

In general, the ionizing radiation dose from the transiting radiation environment is insignificant compared to the trapped radiation environment. Particle fluxes from energetic solar flares are heavily attenuated by the geomagnetic field, which prevents their penetration to low orbital altitudes and inclinations. For a 500-km, 30-degree-inclination orbit, some penetration occurs. In contrast, a polar orbit experiences a substantial degree of exposure at any altitude.

In GEO, the geomagnetic shielding is relatively ineffective. Even so, the average yearly dose from ordinary events behind a 2-g/cm^2 spherical aluminum shield is quite small, approximately 18 rads(Si). In comparison, the event-integrated dose from an anomalously large flare at parking longitude of 70°W would be approximately 600 rads(Si)/event for the same shield and target, as shown in Figure 1-31. Tripling the shield thickness to 6 g/cm^2 would result in 300 rads(Si)/event.

1.4.2.6 Single-Event Susceptibility of Electronics

Single-event upset (SEU) effects in electronics from the transiting space radiation environment may be the result of either the energetic solar flare protons or cosmic rays. The nature of trapped proton-induced single-event effects (SEE) has been discussed previously [Subsection 1.4.1.8]. In general, the SEU rate due to transiting protons is

small compared to that due to cosmic rays, except for the occurrence of an anomalously large event. To cover the occurrence of such an event during the spacecraft mission, both the expected duration and fluence of the anomalously large event must be considered in the electronics design.

Generally, cosmic-ray induced SEE dominate proton-induced SEE, both at altitudes below 1,000 km and above 4,000 km for 60-degree circular orbits. For lower inclination orbits, the cosmic rays are shielded by the earth's magnetic field, causing the cosmic-ray upset level to decrease compared to the proton upset rate. Conversely, for higher inclination orbits, the relative upset rate of the cosmic

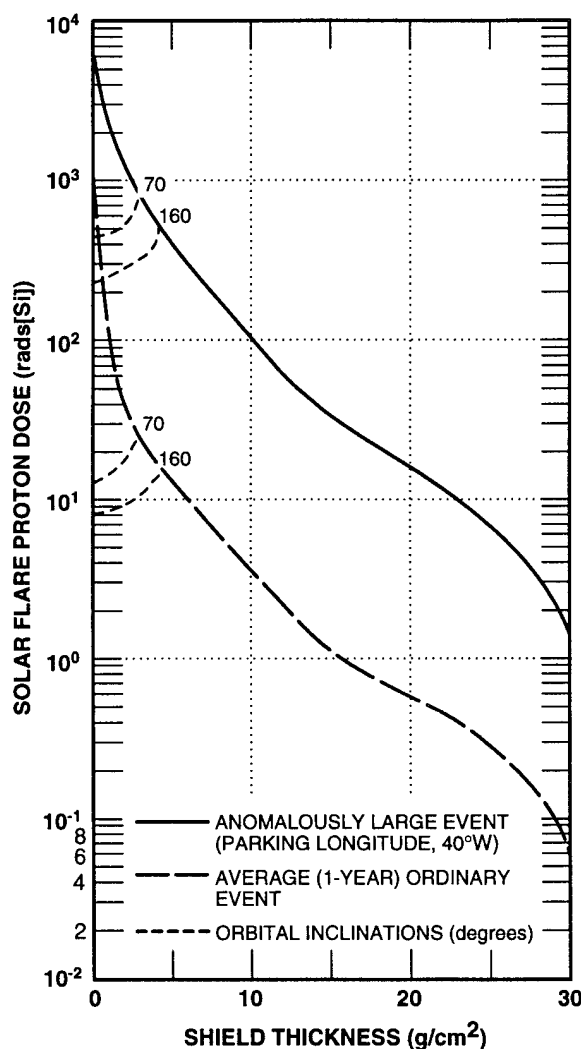


Figure 1-31. Unattenuated solar flare proton dose emerging behind spherical aluminum shielding (Stassinopoulos and Raymond, 1988).

rays increases. The variations in the spacecraft orbit, space radiation environment, and device susceptibility should be considered in estimating specific cosmic-ray/proton upset levels in support of spacecraft electronics design. The specification of the internal electronics environment should include the time-dependent proton flux and energy spectrum, the cosmic-ray LET spectrum, and the cosmic-ray spectrum by particle species and energy spectrum. The actual cosmic-ray spectrum can be a valuable supplement to the LET spectrum in those cases where more detail is necessary to support experimental characterization in ground-based laboratory facilities.

1.4.3 Conclusions

The richly diverse space radiation environment has been described in terms of its nature and variations with respect to the susceptibility of spacecraft electronics. The constraints of space radiation effects on spacecraft electronics design can be significant, but with careful component selection, shielding, and design, systems can be realized that are both of high performance and long endurance.

This section specifically addresses the earth's radiation environment, but magnetic fields and trapped radiation belts are not unique to the Earth. Jupiter, to be explored by the Galileo spacecraft, has a trapped radiation environment that is much more severe than that of Earth. Even in transit to the outer planets and beyond, galactic cosmic rays must be considered for their effects on electronics.

1.5 Systems Development Background

The purpose of this section is to provide a description of the various aspects of nuclear hardening and survivability (NH&S) system development. The various phases of system acquisition will be discussed, emphasizing how system survivability is factored into the various acquisition phases.

1.5.1 Hostile Threats

In developing a system for space, tactical, or strategic use many hostile environments must be mitigated so that the system can perform its mis-

sion. These environments encompass both the nuclear and the nonnuclear. Nuclear environments include the direct, or primary, radiation as well as the secondary environments and phenomena. The primary environments from a nuclear detonation are the neutrons, gamma rays, x rays, and fission products. Depending upon the scenario, these in turn produce, electromagnetic pulse (EMP) effects, high-altitude EMP (HEMP), magnetohydrodynamic EMP (MHDEMP), source-region EMP (SREMP), system-generated EMP (SGEMP), internal EMP (IEMP), electron-caused EMP (ECEMP), and dispersed EMP (DEMP), blast, shock, thermomechanical shock (TMS), and thermal radiation. If the mission of the system is in space, the natural radiations — electron, protons, and cosmic rays — must be considered. For some space systems, both the nuclear and the natural space environments must be considered.

For some missions, other natural phenomena, such as lightning, can be quite hostile. Other non-nuclear environments that may need to be considered include laser, high-powered microwave (HPM), electromagnetic interference (EMI), and several forms of kinetic energy (KE).

1.5.1.1 Nuclear Space Radiation

The primary radiations from a nuclear detonation manifest themselves in widely differing manners, depending upon where the detonation occurs. When the detonation is exoatmospheric, the radiation output essentially consists of x rays, gamma rays, neutrons, and fission products. In this instance, the x rays are the dominant output. Fortunately, x rays can be effectively shielded. For a space system with nuclear detonation survivability requirements, the x rays are often shielded to a level approximately equal to the level of the gamma rays, which cannot be effectively shielded. Neutrons are also effectively impossible to shield.

The primary radiations from an exoatmospheric nuclear detonation, in order of concern for system hardening in space, are x rays, gamma rays, neutrons, and enhanced trapped electrons (for satellites in some orbits). The secondary environments

created by the primary radiations include HEMP, MHDEMP, SGEMP, and ECEMP. Another phenomenon also associated with x rays is thermomechanical shock (TMS).

If the nuclear detonation is endoatmospheric, the environments are somewhat changed. The x rays are converted to airblast, but the gamma rays and neutrons remain because of their extreme penetrating capability. The dominant environment now depends upon parameters such as altitude and system mission (manned or unmanned).

1.5.1.2 Natural Space Radiation

For systems in space, the natural space environment, must be considered in addition to the radiation from the nuclear detonation. The natural radiations of interest are electrons, protons, and cosmic rays. The electrons and protons exist in a relatively wide range of energies.

The electron dose is dependent upon the orbit of the spacecraft because the highest concentrations of the electrons exist in the Van Allen belt, and the exposure will depend upon the length of the time the spacecraft spends in these belts.

Cosmic rays are usually very high-energy-ions that cause single-event phenomena (SEP). Shielding is not considered to be effective in eliminating SEP, so other methods such as device-hardening against SEP and/or error detection and correction (EDAC) must be utilized. For some space-based systems, SEP is the foremost hardening consideration.

1.5.2 Balanced Hardening Concept

It must be emphasized that a complete survivability program will generally include system threats other than nuclear or space radiation. Depending upon the system and other circumstances, these additional threat environments may be more stressing to the system than radiation. The amount of attention given to a particular threat environment should be both proportional to its relative importance and in consonance with hardening activities for other environments, necessitating a bal-

anced approach to hardening. For example, for a ground-based system, there is little value in providing extreme hardening measures for nuclear radiation while ignoring hardening against EMP. A complete discussion of hardness-verification and hardness-assurance activities for these other threats is beyond the scope of this chapter, but other reports and guidelines are available for this purpose. The important point is that the program manager and contractor ensure that comprehensive systems engineering analyses are performed to identify all survivability requirements and assign a proper level of hardening effort to each one.

1.5.3 Emphasis on Electronics

Although many design aspects must be considered when deriving the design specification for a hardened system, it quickly becomes evident that electronic devices must receive a great deal of attention. Historically, it has been recognized that semiconductor devices are usually the items most sensitive to the hostile radiation environments. Accordingly, they receive attention because they are necessary for generating the functions that enable the system to operate and perform its mission.

1.5.4 Life Cycle Survivability and Hardness

Survivability requirements do not cease with the completion of system design and verification. Survivability must be actively considered throughout the design's entire life cycle to ensure that the operational system retains the desired attributes.

Department of Defense (DoD) programs are considered to have life cycles composed of distinct phases. This concept is useful for any system, since it clearly defines milestones that must be met to ensure proper review of design feasibility.

Just as programs have defined phases encompassing particular tasks, the survivability life cycle may be viewed as a continuum of activities. Since these activities are a function of the overall program phase in which they occur, it is instructive to view them in the context of the phases of a major program and in relationship with each other. Figure 1-32 shows these relationships.

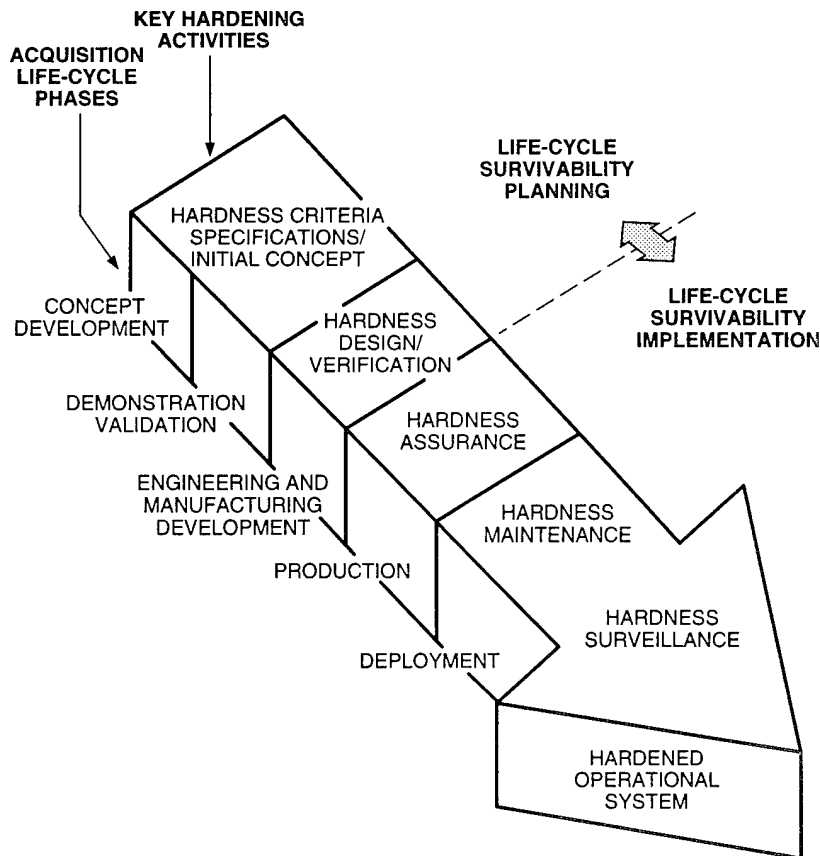


Figure 1-32. Life-cycle survivability program (Coppage, 1993).

The concept development (CD) phase requires development of the environment specifications, hardness criteria, and initial hardening concepts that match the overall system concept.

The demonstration validation (D/V) phase extends, refines, and verifies these items as the system concept is validated. It may include a hardness assessment of the preliminary design concepts. Historically, when the demonstration of the system concept was the focus of the D/V phase with no attention to survivability, the hardening program suffered or was more costly. Survivability must be considered early in the CD phase.

The engineering and manufacturing development (EMD) phase usually requires a large increase in hardening efforts. Detailed design of a hardened system and verification of the design hardness are major activities. They are often accompanied by hardening trade-off studies and numerous hardness tests.

Figure 1-32 shows hardness assurance (HA) occurring in the production phase. In accordance with its definition, HA activities assure production of a system as robust as that verified during EMD in the initial hardened design.

Figure 1-32 is greatly simplified; many other functions necessary for hardening and HA occur during the design phases shown in this figure. To help clarify this point, Figure 1-33 adds hardening and HA considerations along with system-development milestones. Notice that these considerations are present from the program initiations and continue throughout the life of the system.

As stated at the outset of this section, it is also necessary to remember that the hardening and HA program must be a part of the overall system development management structure. To emphasize this point, Figure 1-34 provides another perspective of the activities needed to develop a hardened system.

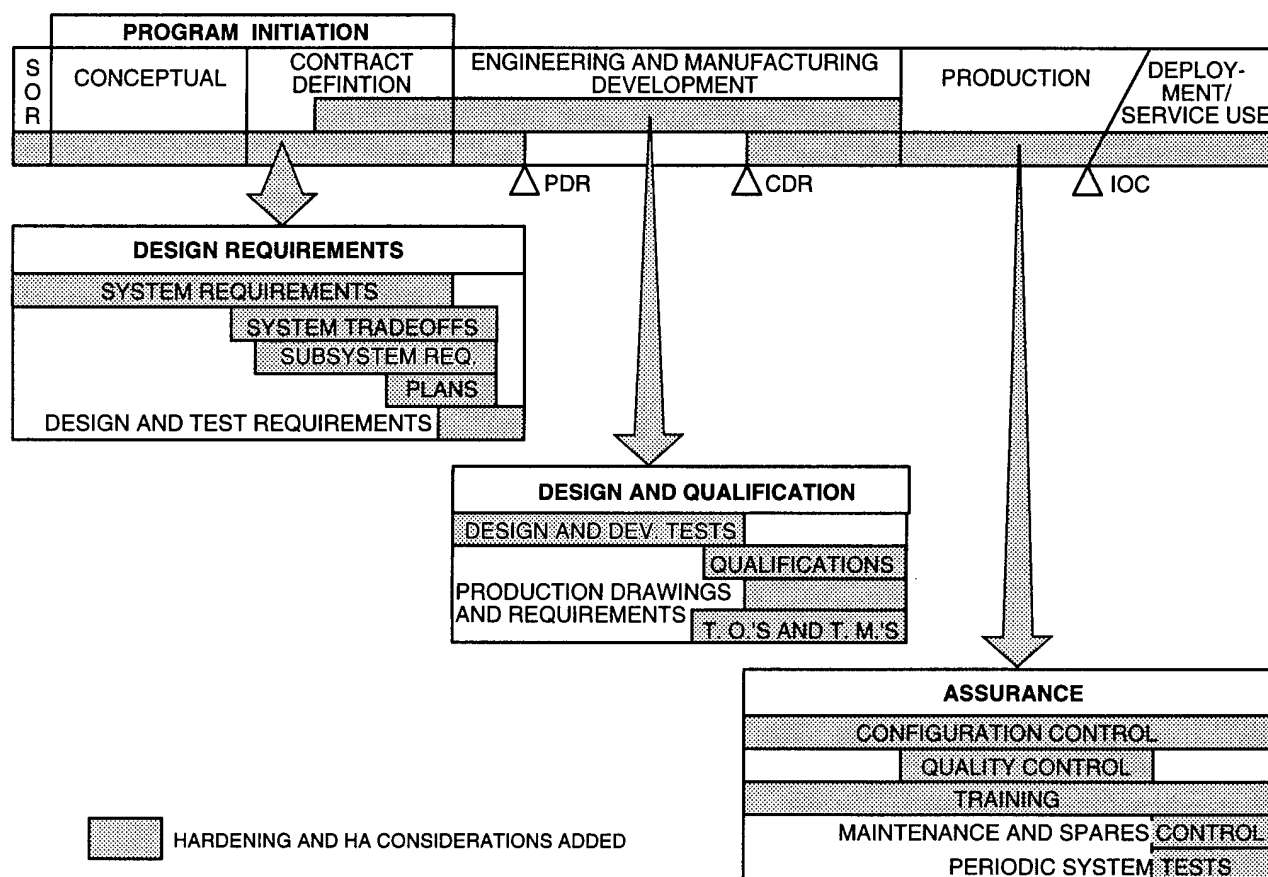


Figure 1-33. Hardening and hardness assurance (HA) incorporated into normal system development tasks (Coppage, 1993).

Finally, during deployment and operational use of the system, hardness maintenance (HM) and hardness surveillance (HS) are used to further guarantee the continuing hardness of the system once fielded. The HA procedures and controls must apply to the procurement of any repair parts used in HM.

1.6 System Nuclear Hardening and Survivability Requirements

This section provides a method for categorizing various types of systems as a function of mission and survivability requirements. This background information should provide a relative indication of the radiation-hardened microelectronic requirements for typical DoD systems.

Several general comments can be made concerning the NH&S requirements of systems and how these requirements translate to radiation-hardened microelectronic component specifications.

However, such a generalization requires that systems be separated into categories based on their use (e.g., tactical, space-communications, space-strategic, interceptor missile, intercontinental ballistic missile [ICBM], strategic-manned, etc.). Table 1-1 provides a summary of generic NH&S requirements for representative systems.

1.7 Nuclear Threat Environments and Nuclear Specification Development

This section explores in detail the development of nuclear threat environments and nuclear specification criteria. These two activities are part of the conceptual and validation phases of the system acquisition life cycle (Figure 1-34). Information that should be provided by the government in the statement of work (SOW) of a procurement action is outlined, and guidance is provided on the information required to define the various radiation threats, (e.g., ionizing radiation dose, dose-rate upset).

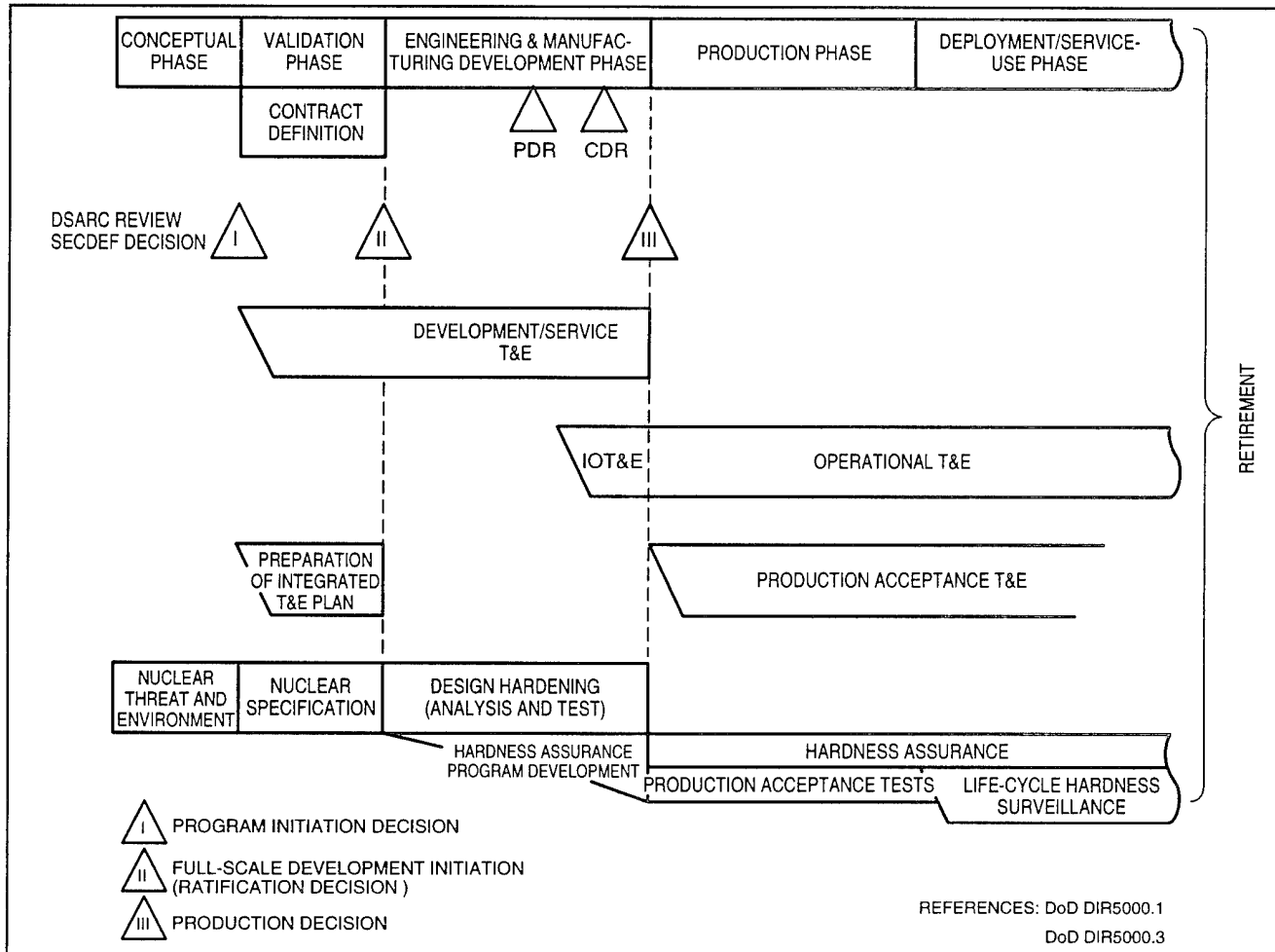


Figure 1-34. System acquisition life cycle for a hardened system (Coppage, 1993).

The SOW for a survivable electronic system must contain the nuclear hardness specifications along with the system performance specification and the other operating environments. The description of the nuclear weapon environments in which the system must be designed to operate is of overriding importance.

Usually, the electronic system developer need not be concerned with calculating the nuclear environment because the nuclear environment external to the system of interest is specified by the procuring agency. The translation of this information to the internal system environment is usually the responsibility of the system developer.

1.7.1 Minimum Adequate Hardness Specification

An adequate nuclear hardness specification for an electronic system should include at least the following:

1. A physically meaningful (unambiguous) definition of the external, or "free-field," nuclear environments to be survived.
2. A definition of the ionizing radiation attenuations and shielding, and/or buildup factors that apply to the system, or a definition of the modified nuclear environment to be encountered by the sys-

Table 1-1. NH&S requirements for representative systems.

System Category	Example Systems	Threat	Microelectronics Requirements	Exemplary Radiation Hardening Requirements
Space-Strategic	FEWS, GPS, MILSTAR Brilliant Eyes	NWE and natural space (ionizing radiation dose, dose-rate upset, single-event phenomena, neutron irradiation)	State-of-the-art 1M RAM, (32-bit microprocessors, 100k gate arrays, MIMIC communications link, discrete power transistors, etc.)	Ionizing radiation dose: ≥ 1 Mrad(Si) Transient upset: $> 1 \times 10^{11}$ rads(Si)/sec (critical memory) SEU: $\leq 1 \times 10^{-10}$ upset/bit-day Neutron irradiation: $\geq 1 \times 10^{12}$ n/cm ²
Space Communications	USN UHF and other communication satellites	Natural space (ionizing radiation dose and SEU)	Commercial near state-of-the-art radiation-tolerant devices with some specifically designed and fabricated rad-hard microelectronics (64k SRAMs, 16-bit microprocessors, 20k gate arrays, GaAs communication links)	Ionizing radiation dose ≥ 100 krad(Si) SEU: $\leq 1 \times 10^{-8}$ upsets/bit-day
Tactical and Strategic-Manned	B1 and B2 aircraft M1A1 tanks SINCGARS	NWE (ionizing radiation dose, neutron irradiation, dose-rate upset)	Commercial microelectronics suitable for reduced threats (e.g., no transient requirements); radiation-tolerant devices satisfactory for other threats (ULSIC SRAMs and DRAMs, 32-bit microprocessors, ULSIC gate arrays)	Ionizing radiation dose: < 10 krad(Si) Neutron irradiation: $\sim 10^{12}$ n/cm ² Transient upset: $\leq 1 \times 10^9$ rads(Si)/sec SEU: (may be specified for high-altitude aircraft)

tem. Both may be needed if the system being developed does not include its own facility or its shielding as part of the contracted effort.

3. A description of the system performance requirements in each operational mode at various times relative to the exposure to the nuclear environment.
4. A statement concerning hardness verification, qualification, and contract compliance demonstration methods, including system survival probabilities and associated confidence levels.
5. Statements regarding HA requirements in production and HM during and after deployment. These may be preliminary

statements calling for program plans to be developed by some later scheduled date.

6. A program plan establishing critical milestones and data requirements.

Items 1 and 2 are nuclear hardness criteria and the environment description; item 3 provides the system performance requirements. The remaining items assist in defining the hardness program.

1.7.2 Nuclear Environment Criteria Development

During the conceptual phases of a survivable system, the nuclear hardness criteria are developed and updated by operations analysis procedures. The mission requirements, enemy capabilities, and system

concept are combined as shown in Figure 1-35. Scenarios that “tell the story” of the system deployment are developed, estimating the results as a function of tactics and the enemy threat.

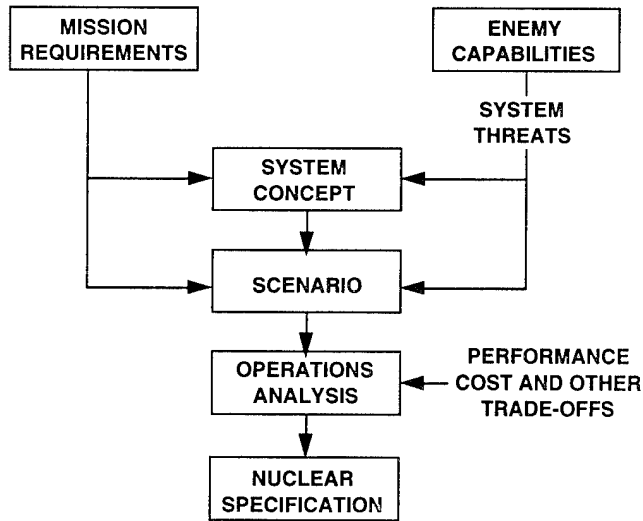


Figure 1-35. Simplified procedure for developing a nuclear hardness specification.

As part of the operations analysis, performance versus life cycle cost trade-off and feasibility studies are conducted. Nuclear hardness and survivability are among the trade-off parameters. The goal of this procedure is the development of: (1) the nuclear hardness specification requirements for the systems, and (2) the supporting documentation and rationales for these criteria.

The establishment of nuclear hardness criteria and nuclear specifications is a government responsibility. Major system contractors frequently will be involved in these early concept-formulation activities, but their involvement is of a supporting nature. In some cases, the system contractor will develop the first proposed nuclear hardness specification, particularly if that contractor has a major role in developing the system concept. In any case, it is desirable for the contractor to influence the preparation of the nuclear hardness specification. It is to the contractor's advantage to assure that the nuclear hardness impacts of his design approach are recognized by the procuring agency and

that appropriate consideration of those impacts are reflected in the nuclear hardness specification. A clear, firm specification forms the basis for fair competitive bidding, bid evaluation, and objective contractor performance compliance demonstration.

It is desirable that the operations analysis, which is the basis for a nuclear hardness specification, be documented and referenced, if not summarized, in the specification. This permits an intelligent evaluation of such issues as new system application, survivability shortcomings, or updated threats scenarios that arise during and after the system-design phase of the development program.

The interaction between the nuclear environment specification, system-performance criteria, and hardness-verification requirements deserves emphasis. The hardening costs can be affected strongly by specific demands on system performance during and after nuclear exposure. There is an important trade-off between the environment specification and verification requirements; augmented environment specifications (e.g., a contractually imposed safety margin) can be used to simplify the verification requirements (e.g., qualification tests), particularly the statistical aspects. This procedure is effective for systems with the lower-level criteria (tactical systems) in which unit cost is a strong factor and the hardness requirements are well within the state of the art technology.

1.7.3 Nuclear Environment Description

The nuclear weapon environment descriptions are the maxima, and/or envelopes, of the external nuclear environments the system must survive. These are “free-field” and “external” in the sense that they need not take account of system mitigation of this external environment. It is always understood that all environment levels lower than those specified must also be survived. The most important requirement for the environment description is that it be clear and complete, leaving nothing substantial to interpretation. From the system developer's viewpoint, it should define the en-

vironment in terms that can be correlated with known effects in the system so that it can serve as a basis for contract compliance demonstration.

During the nuclear hardness specification refinement in the contract definition phase, system and subsystem functional allocations are tentatively made by means of a system requirement analysis (SRA). Additionally, during the full-scale development phase, before preliminary design, the prime contractor or program manager may provide for a number of subcontractors to develop specific subsystems. This subcontracting arrangement also may be made before prime contract award. It is the prime contractor's responsibility, with program office approval, to interpret and redefine the nuclear hardness specifications as applicable for the subcontractors, so that the integrated system will meet its requirements at all system levels.

The hierarchy of the formulation of the subsystem specification is shown generically in Figure 1-36. The overall system specification (Level 1) may include a requirement for withstanding, for example, x-ray flux. However, at the major sub-

system level (Level 2), operational consideration may require that only one of the major subsystems survive x-ray flux (for example, Subsystem 1). The subsystem specification is then divided as necessary at Level 2. Furthermore, at Level 3, the system analysis may show that Sub-subsystem 1 does require an x-ray specification but that Sub-subsystem 1A does not. The specification at this level is again modified. This process continues until the lowest-level subsystem is reached.

The resulting nuclear hardness specifications to be addressed by the subcontractors are still external specifications as far as the subsystem is concerned, but generally are not the free-field environment. For example, when considering TREE, the prime contractor must account for various shielding interfaces that either attenuate or enhance nuclear radiation effects.

In addition to describing the radiation specification that the subsystem in question must survive, the prime contractor has the responsibility for defining the nuclear-induced environments at all subsystem interfaces, including such things as voltage transients

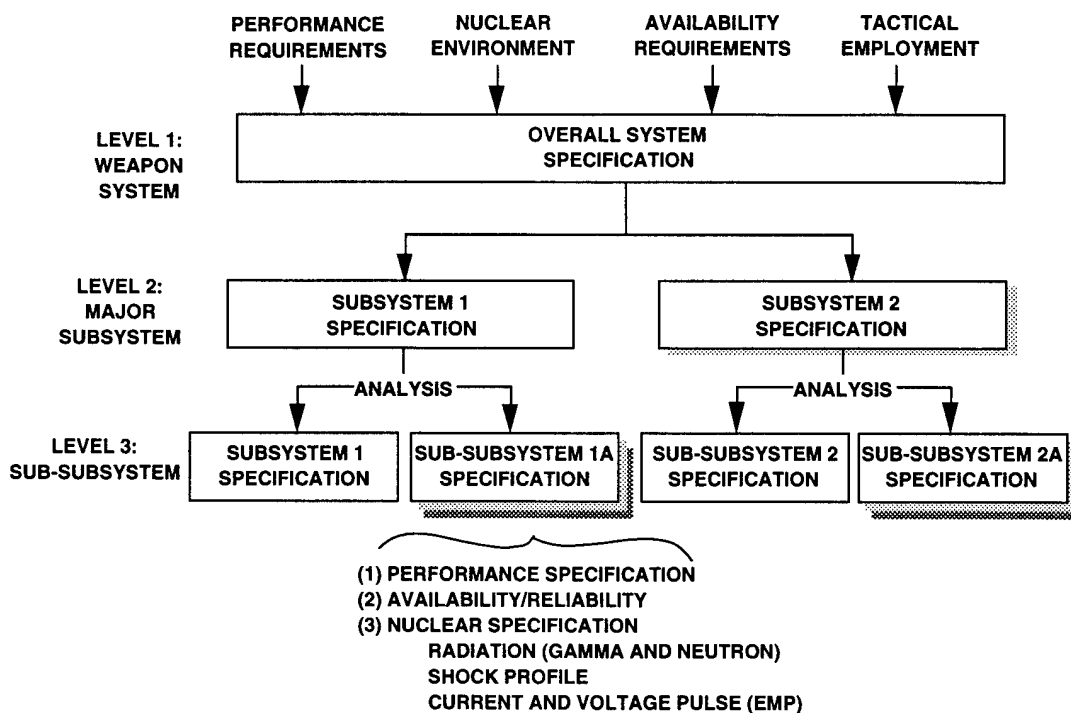


Figure 1-36. Weapon system specification tree.

at hard-wire (cable) interfaces, temperature transients at subsystem enclosures, and structural-impulse reactions that might be transmitted to various subsystems. These are difficult to define at this early stage and are frequently determined by the conservative application of data from other systems and good engineering judgment.

The parameters that must be specified to adequately describe the most important nuclear environments are discussed in Subsection 1.7.4. If these guidelines are followed, a clear definition of the nuclear hardness specification will result.

1.7.4 Nuclear Environment Specification at the System

The nuclear hardness specification for an electronic system must include physically clear (unambiguous), quantified descriptions of all environments that can affect the system performance and which the system is required to survive. The difference between the environment and the effects of the environment must be made clear. For example, neutron fluence and energy spectrum would be an environment, while the damage-equivalent fluence or an ionization dose value would be an effects-type description. Both could be given, for reasons to be discussed. The following subsections present the minimum information required in a nuclear specification of the design environment at the system.

1.7.4.1 Neutrons

A neutron hardness specification for a system should at least consist of the following:

1. A fluence value of neutrons above some threshold energy (n/cm^2).
2. A spectrum curve, table, or source description. Usually, the spectrum for all neutrons above the threshold of 10 keV is adequate for engineering purposes.
3. A time history of neutron flux and spectrum (if significant) for the scenario ($n/[cm^2\text{-sec}]$).

4. An effects equivalent fluence, consistent with the physical fluence and spectrum for the damage effects of interest or importance. The most common unit is the 1 MeV(Si) displacement equivalent fluence. Alternately, the means whereby the effects equivalent fluence is calculated from the spectrum can be specified.

The ionization effects of neutrons should also be included in the description of the delayed ionizing radiation environment.

1.7.4.2 Gamma Rays

It is adequate, and common practice, to specify prompt free-field gamma rays as an electron equilibrium absorbed dose, or dose rate, in silicon. Dose rate should be specified either with a pulse shape $rads(Si)/s$ versus time) or a peak rate and a pulse length for triangular or Gaussian representation.

1.7.4.3 X Rays

Because weapon-produced x rays interact quite strongly with system enclosures, it is essential that the description of a system's external free-field environment be given in terms of the incident radiation rather than energy disposition in electronics. Therefore, a specification of the x-ray energy fluence (cal/cm^2), the time history of the x-ray flux ($cal/[cm^2\text{-sec}]$ versus time), and x-ray energy spectra are required. The energy spectrum is often defined in terms of the photon output of one or more blackbody spectra with a characteristic temperature or energy. The system developer must determine the x-ray environment at specific points of interest in dose terms (i.e., $rads [Si]$ or $cal/g[Au]$) considering the system shielding and recognizing the nonequilibrium nature of the dose near interfaces.

Subcontractors or subsystem developers may receive x-ray specifications in dose units wherein the prime contractor has performed the needed

shielding calculation. It is vital that a clear distinction be made between electron equilibrium dose and actual dose near an interface.

1.7.4.4 Ionizing Radiation Dose

Ionizing radiation dose is stated independently in the nuclear hardness specification. Normally units of rads(Si) are used for the descriptions since no confusion arises in the interpretation of absorbed dose. Ionizing radiation dose is the sum of all ionizing radiation doses in the system due to neutrons, x rays, prompt gamma rays, delayed or secondary gamma rays, fission-product gamma rays, and trapped electrons (in some exoatmospheric situations). Electron ionizing dose is of importance in satellites and space systems. In addition, due to total ionizing validation time dependent effects (discussed in detail in Chapter 2), the dose rate of the ionizing radiation source (e.g., NWE, etc.) would be identified.

1.7.4.5 Nuclear EMP

An EMP specification should contain exterior free-field descriptions of the electric (E) and magnetic (H) fields in volts per meter and ampere-turns per meter, respectively, as functions of time or frequency, with polarization stated (or given as worst case for the system developer to design against). The E(t) and H(t) characteristics are different for high-altitude bursts and ground-level or atmospheric bursts, and a variety of threats may need to be considered in the specification.

For subsystem specifications, coupled currents, Thevenin or Norton equivalent sources, enclosure-shielding attenuation factors, and line-filter attenuations may be used to define the designer's tasks.

1.7.4.6 SGEMP

SGEMP may be specified in terms of external impinging photon flux and energy spectrum, in which case the system developer must account for the effect in the enclosure design (materials, shapes, shielding, etc.), and in selection of insensitive components or configurations. Alternatively, the procurement agency may specify the internal fields, if they are calculable. The reader is cau-

tioned that SGEMP effects and coupling coefficients are sometimes poorly defined.

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CHAPTER 2

IONIZING RADIATION EFFECTS*

2.1. Radiation Sources and Interaction With Matter

When an integrated circuit (IC) is exposed to a significant radiation environment, the electrical properties of its active components usually will be altered, resulting in circuit performance degradation or failure. In addition, for pulsed radiation, radiation-generated photocurrents can lead to transient circuit upset. The primary goal of the radiation effects community is to harden electronic systems subjected to radiation to prevent degradation, failure, or upset. Hardening may be accomplished by several different ways: on the device level processing, design, layout and material choice (e.g., silicon-on-insulator vice bulk technology are employed). On the system or subsystem level power strobing, circumvention, EDAC and design methods are used. In addition shielding can be used at the device, subsystem and/or system level.

In this chapter, the basic mechanisms of ionizing radiation on material (Si, SiO₂, etc.) and devices [metal-oxide-semiconductor (MOS) and bipolar technologies] are discussed. In addition, a brief discussion of ionizing radiation effects in gallium arsenide (GaAs), the simultaneous effects of ionizing radiation and temperature, and reliability problems in MOS field-effect-transistors (MOSFETs) will be presented.

The term "total dose," widely used to describe ionizing radiation effects, is not quite correct because of time-dependent effects. In this handbook, and particularly in this chapter, "ionizing radiation dose" is used instead of "total dose."

2.1.1 Sources and Types of Radiation

Electronic systems may be exposed to a variety of radiation sources and environments. Those environments of the most interest are space radiation and radiation from nuclear reactors and explosions. These environments have been the primary drivers of the work in radiation effects and hardening. The specific types of radiation and the irradiation scenarios associated with each of these environments differ widely. Therefore, when attempting to harden a particular electronics system, it is important to keep the specific application and potential radiation environment in mind. For example, systems to be used in space may have to withstand large radiation doses that are accumulated slowly over long periods of time, whereas electronics to be used in the vicinity of nuclear explosions must be hardened against radiation delivered in very short pulses at very high dose rates.

Other radiation sources to which electronic systems may be exposed include materials with radioactive contaminants, such as uranium and thorium. When incorporated into packaged ICs, these materials can produce isolated radiation events (e.g., alpha particle emissions), which can result in occasional transient upsets similar to single-event upsets (SEU) encountered in space radiation environments. Other radiation sources are the various irradiation tools used in the processing of modern small-scale, high-density ICs, which include ion-implantation machines, plasma-ion etching, and x-ray and electron-beam lithography tools. It is important that the radiation damage caused by these tools be minimized during processing. Finally, the various radiation simulators used both to study the fundamental nature of the interactions of radiation with matter and to simulate various

*Much of the material presented in this chapter is derived from McLean and Oldham (1987).

aspects of threat radiation environments of interest are discussed. These include such facilities as ^{60}Co cells, x-ray irradiators, particle accelerators [e.g., linear accelerators (LINAC)], flash x-ray (FXR) machines, and nuclear reactors.

The various radiation sources and/or environments give rise to a variety of irradiating species, with a wide variation in energy spectrum and time history. For example, nuclear explosions give rise primarily to x-rays, gamma-rays and neutrons, whereas the space environment consists essentially of a low-level, constant flux of energetic charged particles — electrons, protons, and heavy ions. The various types of irradiating species can be grouped into three major categories: (1) photons (x rays and gamma rays); (2) charged particles (electrons, protons, alpha particles, and heavy ions); and (3) neutrons. Cosmic rays encountered in the space environment consist of a variety of charged particles, generally with very high energies (>100 MeV). The neutron energy ranges of interest are the so-called high-energy range (tens of MeV down to 10 keV) and the thermal range ($\sim\text{kT}$).

The interaction of radiation with solid-material targets depends on a number of factors, namely, on the mass, charge state, and kinetic energy of the incident impinging particle, and on the atomic mass, atomic number (charge), and density of the target material. The specific types of interactions that occur between the primary particles and target atoms are listed below:

- Photons (\rightarrow high-energy secondary electrons)
 - Photoelectric effect
 - Compton scattering
 - Pair production
- Charged particles
 - Rutherford scattering
 - Nuclear interactions (heavy particles)
 - Coloumb interaction
- Neutrons
 - Elastic scattering
 - Inelastic scattering
 - Transmutation reactions.

These are addressed in the subsections that follow. Many references are available that discuss these interactions in great detail. A list of these is provided in the bibliography in chapter 7.

2.1.1.1 Photon Interactions

Photons interact with target atoms through the photoelectric effect, Compton scattering, and pair production, each interaction producing energetic free electrons. The energy range in which photoelectric collisions dominate depends on the atomic number (Z) of the material. Away from the electron shell absorption edges (where the interaction probability increases abruptly with increasing photon energy), the probability of a photoelectric interaction decreases with increasing photon energy and increases with Z . If the incident photon is energetic enough to emit an electron from the K-shell, then most (~ 80 percent) of the collisions are with K-shell electrons. In the photoelectric process, the incident photon energy is completely absorbed by the emitted electron (photoelectron). If a K-shell electron is involved, then an L-shell electron will drop into the remaining empty state. Either a characteristic x ray or a low-energy Auger electron is emitted from the L-shell, depending on the value of Z .

In contrast to the photoelectric effect, Compton scattering does not involve complete absorption of the incident photon. Figure 2-1 shows the region where Compton scattering is dominant. The incident photon gives up a portion of its energy to scatter an atomic electron, thereby creating an energetic Compton electron, and the lower-energy, scattered photon continues to travel in the target material.

The third type of photon interaction, pair production, has a threshold energy of 1.02 MeV. Above this energy, a photon striking a high- Z target may be completely absorbed and cause a positron/electron pair to form. [A positron has the same rest mass and charge as an electron, except that the charge is positive.]

Figure 2-1 illustrates the relative importance of the three photon interactions as a function of Z and photon energy. The solid lines correspond to equal-interaction cross sections for the neighboring ef-

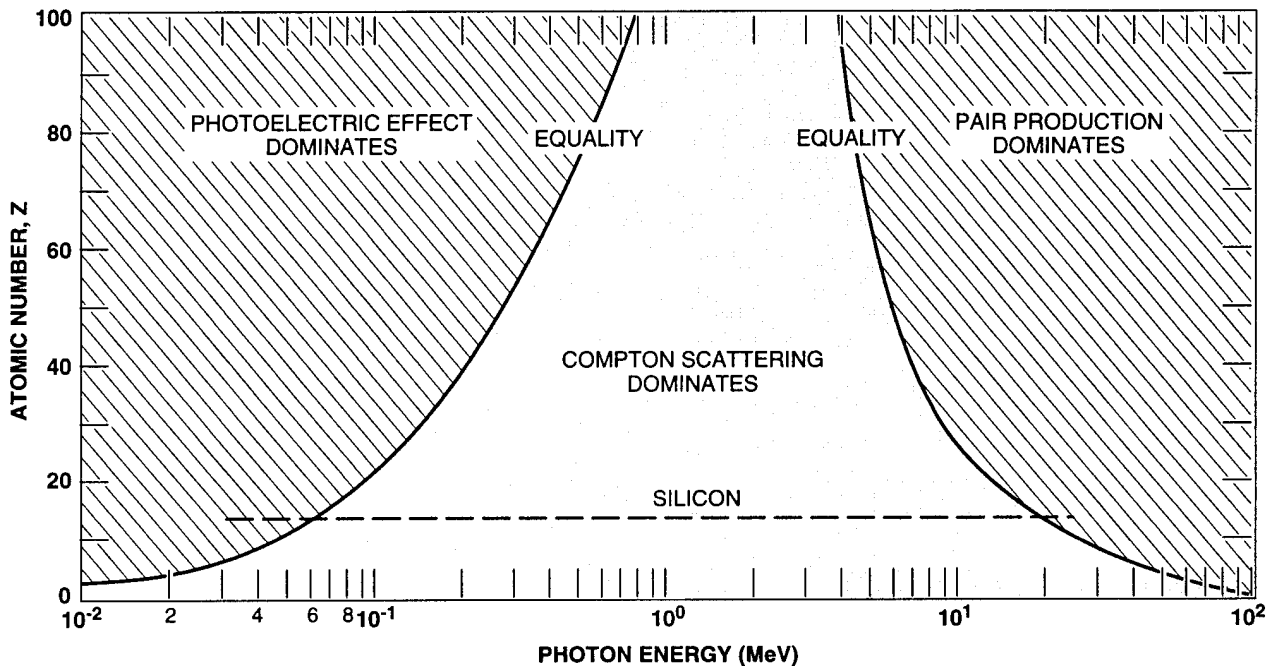


Figure 2-1. Relative importance of three photon interactions as a function of atomic number and photon energy (Evans, 1955).

fects. For silicon ($Z = 14$), the photoelectric effect dominates at energies below 50 keV and pair production dominates at energies above 20 MeV. Over the broad intervening energy range, Compton scattering dominates. In all three cases, however, the essential result of the photon interactions is the production of energetic secondary electrons (and positrons at very high photon energy), which then undergo subsequent charged-particle interactions. In other words, the primary energy transfer from the incident photons to the target occurs via the secondary electron interactions.

2.1.1.2 Charged-Particle Interactions

Charged particles incident on a target interact primarily by Rutherford scattering and Coulomb interaction. Rutherford scattering can cause both excitation and liberation (ionization) of atomic electrons. If their energies are high enough to overcome the Coulomb repulsion of the target nucleus, protons and other nuclear particles can undergo nuclear reactions with the target nucleus. For example, a proton can be absorbed by the nucleus to form a compound nucleus that can then, depending on the proton's energy, emit one or more neutrons, an alpha particle, or other nuclear particles.

Target material ionization is a major consequence of charged-particle interactions, especially for electrons and the lighter charged ions (protons, alphas). In semiconductors and insulators, ionization results in excess nonequilibrium densities of electrons and holes. The actual ionization processes associated with the passage of a single energetic charged particle through a solid is exceedingly complex, generating a number of high-energy secondary electrons with various energies and momenta, which subsequently produce further ionization, and so on in a cascade process. However, most of the final ionization events and most of the energy transfer occur through a single type of intermediate process involving the collective motions of many valence electrons in simple oscillatory motion against the background of positive ionic cores. (Because of the much larger masses, the ion cores can be considered stationary relative to the oscillating electrons.) These plasma vibrations, or plasmons as they are called in quantum mechanics jargon, are induced by the long-range nature of the Coulomb interaction, which extends over regions containing many atoms. The plasmon energies, corresponding to the resonance frequency

of the oscillations, are typically in the range from 10 to 20 eV for most solids, depending upon the number density of valence electrons. Following its creation, a plasmon decays rapidly (<1 psec) via excitation of a single electron/hole pair across the bandgap. The excess kinetic energy carried by the individual electrons and holes may result in one or two additional ionization events (depending upon the bandgap width), with the remainder of the energy being quickly dissipated as thermal lattice motion.

2.1.1.3 Neutron Interactions

Neutrons incident on a target undergo the following nuclear interactions: elastic scattering, inelastic scattering, and transmutation. In an elastic collision, the neutron gives up a portion of its energy to an atom of the target material, and can dislodge the atom from its lattice position. This process will occur as long as the imparted energy is greater than that required for displacement (~25 eV for most materials). The displaced atom is referred to as the primary recoil atom (or primary knock-on atom, PKA); it subsequently will lose energy to ionization and can also displace other lattice atoms.

Inelastic neutron scattering involves capture of the incident neutron by the nucleus of the target atom with subsequent emission of the neutron at a lower energy. Kinetic energy is lost in this process and the target nucleus is left in an excited state. The excited nucleus returns to its original state by the emission of a gamma ray. The kinetic energy of the emitted neutron is reduced, compared to the incident neutron, by the energy of the gamma ray. Inelastic neutron scattering can also cause displacement of the target atom to occur.

Transmutation involves capture of the incident neutron by the target nucleus and subsequent emission of another particle, such as a proton or an alpha particle. The remaining atom is thereby transmuted, i.e., converted from one element into another. The nuclear particle and the recoiling residual nucleus emitted from the transmutation reaction can also produce displaced atoms.

2.1.2 Ionization and Atomic Displacements

In spite of the seemingly complex interactions of radiation with matter, with the various dependencies of the interactions on the properties of the incident particle and target materials, in the end two essential effects on solid-state electronics are produced: (1) ionization (generation of electron/hole pairs), and (2) displacement damage (dislodging atoms from their normal lattice sites). As previously stated, particles passing through electronic materials generally deposit a portion of their energy into ionization and the remainder into atomic displacements. However, for most practical purposes, the situation is even simpler than this statement indicates. Specifically, for charged-particle irradiation, the primary modes of electronic device degradation occur as a result of ionization, even though a certain amount of atomic displacement can occur in general, especially for the heavier ions. Similarly, for high-energy neutron irradiation, the primary mechanisms for device degradation are attributed to atomic displacement damage, even though considerable ionization can be associated with neutron interactions. This simplified situation is summarized in Figure 2-2.

It must be recognized, however, that this is a simplification that applies to the commonly observed failure or degradation modes of most electronic devices. To be sure, there are situations or particular devices in which neutron-induced ionization can be significant, or in which displace-

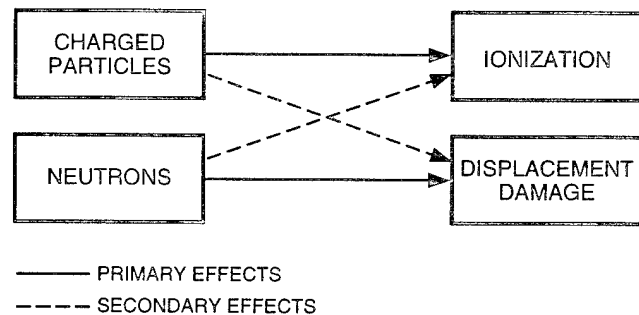


Figure 2-2. Schematic indicating primary radiation effects and secondary effects in electronic materials (McLean and Oldham, 1987).

ment damage associated with energetic charged-particle irradiation can be significant. For the topics to be covered here, ionization damage can essentially be associated with charged particles and displacement damage with neutrons.

2.1.3 Radiation Exposure Terminology

The commonly used terminology and units of radiation exposure and damage are presented here to enable quantification of the subsequent topics of this chapter. Table 2-1 highlights some of the important terminology and units of radiation exposure.

Flux is simply the particle current density incident on a particular area element expressed in number of particles/cm²-sec. Particle fluence is just the time integral of the flux over some period of time (e.g., over the time of a radiation pulse) expressed in units of particles/cm². The energy spectrum is simply the distribution of a particle fluence (or flux) over energy, e.g., particles/cm²-MeV.

Table 2-1. Important terminology and units of radiation exposure.

Type of Radiation Exposure	Units of Measure
Flux	particles/cm ² -sec
Fluence	particles/cm ²
Energy spectrum	particles/cm ² -MeV
Neutron fluence	n/cm ²
1-MeV equivalent neutron fluence	n/cm ²
Ionizing radiation	
Stopping power (linear energy transfer, $\rho^{-1} dE/dx$)	MeV-cm ² /g
Absorbed ionizing radiation dose (D, or γ)	rad(M) ^a
Ionizing dose rate ($\dot{\gamma}$, or $\dot{\times}$)	rad(M)/sec

Note:

^a1 rad = 100 ergs/g = 0.01 J/kg [SI units: 1 gray (Gy) = 100 rads = 1 J/kg]. M represents the target material of interest, typically silicon (Si) or silicon dioxide (SiO₂) for electronic components.

Neutron exposure of a sample is commonly given in terms of the neutron fluence (n/cm²). However, the amount of displacement damage from neutrons in a given material varies significantly with neutron energy. Therefore, in order to allow meaningful comparisons between experiments using different neutron energy spectra, neutron fluences are often expressed in terms of "normalized to" an equivalent 1-MeV neutron fluence, which is that fluence of 1-MeV neutrons that would produce the same electronic effect as the neutron spectrum used in a particular study.

For charged-particle exposure, the amount of energy that goes into ionization is given by the stopping power, or the linear energy transfer (LET) function $\rho^{-1} dE/dx$, commonly expressed in units of MeV-cm²/g. The stopping power has been tabulated for a number of target materials as a function of incident particle energy and atomic number. An example of the stopping power for electrons (Berger and Seltzer, 1966) and protons (Janni, 1966) incident on silicon is shown in Figure 2-3. The absorbed ionizing dose (D, or γ) is the integral over energy of the product of the particle energy spectrum and the stopping power. The commonly used unit of absorbed ionizing dose is the rad (radiation absorbed dose), where 1 rad is equal to the absorbed energy of 100 ergs/g of material. As a result, the energy loss per unit mass differs from one material to another, the material in which the dose is deposited must be specified when this unit is used, e.g., rads(Si) or rads(SiO₂). The Système International (or metric) SI unit of absorbed dose is the gray (Gy), which is equal to an absorbed energy of 1 J/kg, or 100 rads. However, the gray is rarely used by the radiation effects community. Finally, the ionizing dose rate ($\dot{\gamma}$) is usually expressed in rads(M)/sec, where M represents the target material of interest (e.g., Si, SiO₂).

2.1.4 Overview of Primary Radiation Effects on Electronic Materials

As discussed above, the dominant effects resulting from the interaction of radiation with electronic materials are ionization (primarily associated with charged-particle interactions) and atomic displacement damage (primarily associated

with high-energy neutron exposure). The major consequences of these effects are discussed here; the effects of atomic displacement damage are discussed in Chapter 4.

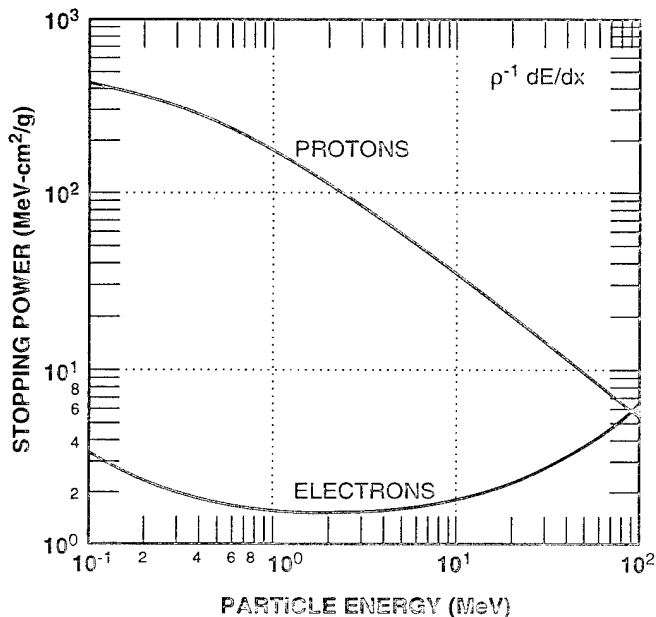


Figure 2-3. Stopping power versus particle energy for electrons and protons incident on silicon (Berger and Seltzer, 1966; Janni, 1966).

Figure 2-4 is a schematic of the ionization process in semiconductors and insulators. In Figure 2-4(a), an electron in the valence band is excited across the bandgap into a conduction band state, either as a direct result of interaction with an energetic charged particle or as the result of the decay of a plasmon excitation (the collective oscillation of a large number of valence-band electrons). Very rapidly (on the order of a picosecond), the excited electron in the conduction band and the hole left behind in the valence band lose their excess kinetic energy [Figure 2-4(b)] through lattice scattering and are "thermalized" in energy, falling to the vicinity of the conduction- and valence-band edges, respectively. Then, except for some fraction (small in semiconductors, possibly large in insulators) of the electron/hole pairs, which undergo what is called initial recombination, the electron and hole will be free to diffuse and drift (if electric fields are present) away from their point of generation

[Figure 2-4(c)] until they either undergo recombination elsewhere in the material, or are trapped at a localized trap (defect) site, or are collected at an electrode.

If an electric field is present, there will be net charge separation and, therefore, an electric current. These radiation-induced photocurrents can be a major problem in semiconductors, resulting in circuit upset or burnout. Associated with the passage of even a single energetic heavy particle (alphas, heavy ions), sufficient ionization may occur such that the current or collected charge may cause

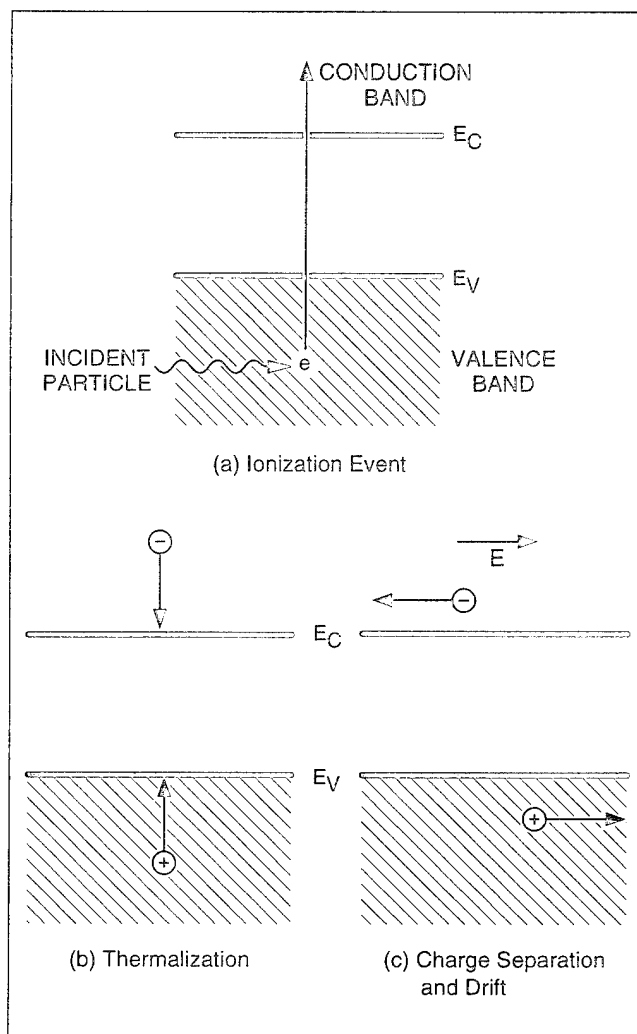


Figure 2-4. Schematic of ionization process in semiconductors and insulators; ionization leads to transient photocurrents and buildup of trapped charge (space-charge effects). [Effective measure of damage is charge yield per unit dose (electron/hole pairs per rad).] (McLean and Oldham, 1987)

an upset. In this case, upsets are referred to as single-event upsets, as opposed to bulk-ionization-induced photocurrents upsets. The currents associated with a single particle may also induce current latchup in some cases. Latchup is a specific type of device failure mode which is caused by the activation of a parasitic silicon-controlled-rectifier (SCR) structure contained in CMOS and some bipolar circuits. This SCR structure can only be deactivated by the removal of the excitation voltage. Prolonged activation of the SCR structure can result in circuit failure. Latchup can be caused by either dose-rate induced photocurrents or the charge deposited by a single ion strike. These problems are increasing in importance as the sizes of devices are scaled down, thus requiring less charge to cause upset.

In insulators (e.g., SiO_2), radiation-induced photocurrents are generally not a problem because of the much lower carrier mobilities and lower numbers of electron/hole pairs created. However, insulators generally contain relatively large densities of charge-trapping centers, where the radiation-induced charges can be trapped for long periods of time. The trapped charges can then generate internal space-charge electric fields, which in turn can lead to voltage offsets or shifts in device operating characteristics. If sufficient space-charge fields are generated, device failure may result. This is a major radiation effects problem in MOS devices. In addition, internal space-charge fields due to trapped charge in field oxides and passivation insulators can turn on parasitic current leakage paths in adjoining semiconductor materials. As device dimensions are scaled down, this also will become more of a problem in both MOS and bipolar technology circuits.

The amount of damage due to ionization is directly related to the charge yield per unit dose, i.e., number of electron/hole pairs generated per rad. This is true both for the magnitudes of the induced photocurrents (for pulsed irradiation) and for the amount of trapped-charge buildup for ionizing radiation dose effects. Table 2-2 lists the average ionization energy (E_p) required to generate a single electron/hole pair for several important electronic materials, as well as the initial charge pair density

per rad (g_0) deposited in the material. The latter quantity is obtained simply from the product of the material density and the deposited energy per rad ($1 \text{ rad} = 100 \text{ ergs/g} = 6.24 \times 10^{13} \text{ eV/g}$) divided by E_p . As noted earlier, in wide-bandgap insulators such as SiO_2 , significant initial (or immediate) recombination of the electron/hole pairs can occur before they can separate. The actual charge yield for charged particles is a function of the electric field and the line density of electron/hole pairs (number created per track length of the incident particle); the value of g_0 listed in Table 2-2 corresponds to the yield in the high field limit. For photons, the charge yield depends primarily on photon energy and the electric field.

Table 2-2. Electron/hole pair generation energies and pair densities generated by 1 rad (Srour, 1982 and 1983).

Material	Pair Generation Energy, E_p (eV)	Pair Density Generated per rad, g_0 (pairs/cm ³)
Silicon	3.6	4.0×10^{13}
Silicon dioxide	17	8.1×10^{13}
Gallium arsenide	-4.8	$\sim 7 \times 10^{13}$
Germanium	2.8	1.2×10^{14}

The primary effects of ionizing radiation on electronic materials discussed here are summarized below:

- Ionizing radiation dose (D): charge buildup effects (rads[Si] or rads[SiO₂])
 - Voltage offsets
 - Induced parasitic leakage currents
 - Speed (mobility) degradation
- Transient radiation effects: induced photocurrents or particle ionization
 - Transient upset ($\dot{\gamma}$) due to bulk semiconductor ionization (rads[Si]/sec)
 - Single-event upset due to energetic heavy ions (errors/bit-day)
 - Latchup

- Burnout
- Gate rupture.

The overall content of this list resembles the general form of a radiation specification that may be imposed on an electronic system required to operate in a given radiation environment. That is, the system may be required to survive or to be hardened against failure for given values of ionizing radiation dose (rads[Si] or rads(SiO₂)), dose rate (rads[Si]/sec), and SEU, usually expressed in terms of some maximum error rate per bit for the threat environment (e.g., errors/bit-day). Typical target values for radiation-hardened circuit are ionizing radiation dose to 1 Mrad, dose rate to 10⁹ rads/sec, and SEU to 10⁻⁸ error/bit-day.

2.1.5 Characteristics of Specific Radiation Environments

When defining a radiation survivability specification for an electronic system, the potential radiation environment must be considered. Some pertinent information concerning the three radiation environments of most practical interest (space, nuclear explosions, and nuclear reactors) is given in Table 2-3, (1) summarizing the quantitative characteristics of the various environments, (2) indicating the primary failure mechanism of ICs exposed to these environments, and (3) noting some of the radiation effects data. The various failure mechanisms are discussed in some detail in the remainder of this chapter.

Table 2-3. Characteristic radiation output and pertinent features of natural space, nuclear explosions, and nuclear reactors.

Natural Space	Nuclear Explosion	Nuclear Reactor
Environment		
Low ionizing dose rate (<<1 rad/sec)	High-dose-rate gamma flux ($\dot{\gamma} \geq 10^8$ rads/sec)	Steady-state neutron flux
Ionizing radiation dose ($\geq 10^5$ rads)	Ionizing radiation dose ($\geq 10^4$ rads)	Low to moderate ionizing dose rate (gamma rays)
High-energy electrons and protons trapped in the earth's magnetosphere	Delayed high-energy neutron flux (fluence $\geq 10^{13}$ n/cm ³)	
Galactic Cosmic Rays (GCR) - (electrons, protons, heavy ions)		
Solar Enhanced Particles (same as GCRs)		
Primary Failure Mechanisms		
Ionizing-radiation-dose-induced charge buildup	Ionizing-radiation-dose-induced charge buildup	Displacement damage
Single-event effects	Transient-photocurrent-induced upset and burnout Neutron displacement damage	Ionizing-radiation-dose-induced charge buildup
Test Simulators		
Low-dose-rate ionization sources: ⁶⁰ Co, x-ray tester	Ionization sources: flash x ray, LINAC electron beam (for dose rate); ⁶⁰ Co, x-ray tester (for ionizing data)	Nuclear reactor Moderate-dose-rate ionization sources: ⁶⁰ Co, x-ray tester
High-energy particle sources: proton and heavy-ion beams	Neutron source: nuclear reactor	

2.2 Basic Mechanisms of Ionizing Radiation Effects on Electronic Materials and Devices

In Section 2.1 it was noted that one of the major effects associated with radiation-induced ionization in electronic materials is trapped-charge buildup, which induces internal space-charge fields that interfere with the normal (designed) operations and control of devices. This problem is primarily associated with the insulating films used in modern IC technologies. The primary focus of work in this area over the past 20 years has addressed MOS technologies because of the importance of the charge-trapping effects in the thin silicon dioxide films employed in these technologies, both as gate oxides over the active semiconductor channel region and as isolation or passivation oxides. However, as device dimensions shrink, the ionizing radiation dose problem is of increasing concern for the bipolar technologies as well, in connection with trapped-charge-induced leakage paths near isolation or passivation oxides. For the purposes of discussing the pertinent physics, the ionizing radiation dose charging problem in SiO_2 gate oxides of MOS structures will be addressed. The basic mechanisms underlying charge trapping are the same in both gate and field passivation oxides, differing only in the circuit manifestations. In addition, a brief discussion of induced leakage current problems for both MOS and bipolar structures will be presented. In general, charging of the oxide regions can occur both within the bulk of the oxide films as well as at the interfaces between the oxides and the semiconductor regions.

Figure 2-5 shows a simple schematic of a MOSFET, in this case an n-channel device using a p-type Si substrate. When a bias potential is applied to the gate contact, an electric field exists across the gate-oxide region and into the silicon (Si) surface region immediately below the gate region. If the gate bias is sufficiently large and positive (for n-channel operation), the majority carriers (holes in p-type Si) will be repelled from or depleted in this surface region, and minority carriers (electrons) will be attracted to this region, forming what is called an inversion layer.

Additionally, if a potential difference is subsequently applied between the source and drain contacts [n⁺-doped regions in Figure 2-5], the inversion layer provides a low-resistance current channel for electrons to flow from the source to the drain. The device is then said to be turned on [Figure 2-5(a)], and the control-gate bias potential at which the channel just begins to conduct appreciable current is called the turn-on voltage, or threshold, of the device.

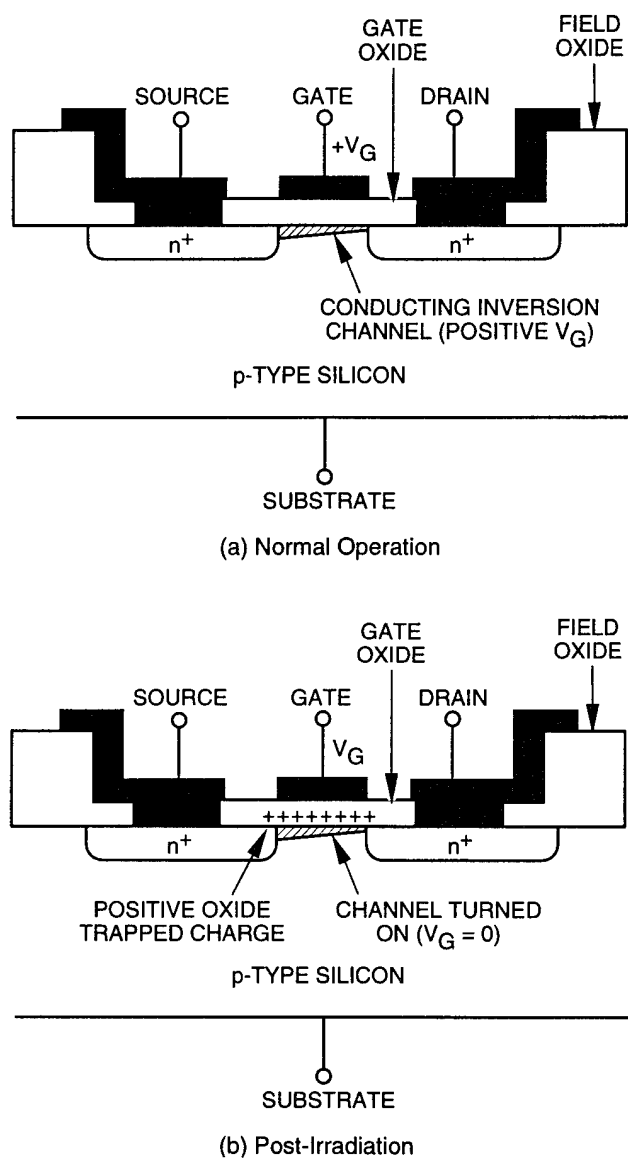


Figure 2-5. Schematic of n-channel MOSFET illustrating the basic effect of ionizing-radiation-dose-induced charging of the gate oxide (McLean and Oldham, 1987).

The ionizing radiation dose problem that occurs in this structure is then due to the radiation-induced charging (normally positive) in the thin gate-oxide region, which generates additional space-charge fields at the Si surface. These additional induced fields result in voltage offsets, or shifts, in the turn-on voltages of the devices, which lead to circuit degradation and failure. For example, for sufficiently large amounts of trapped positive charge for the device shown schematically in Figure 2-5, the device may be turned on even for zero applied gate bias [Figure 2-5(b)]. In this case, the device is said to have failed by “going into depletion mode.”

2.2.1 Radiation Response of MOS Structures

Figure 2-6 shows a schematic energy band diagram for an MOS structure where positive bias is applied to the gate, so that free electrons in the oxide layer will be swept toward the gate and holes will be attracted to the Si substrate. (In an energy band diagram — essentially equivalent to a potential energy diagram — electrons tend to fall downhill, whereas holes will float upward.) Also indicated in Figure 2-6 are the four basic processes contributing to the radiation response of such a system.

The part of an MOS structure that is most sensitive to ionizing radiation is the oxide insulating layer (SiO_2), which in present-day devices is generally less than 100 nm thick. When the radiation passes through the oxide, the deposited energy creates electron/hole pairs. In SiO_2 , the radiation-generated electrons are much more mobile than the holes, and they are swept out of the oxide (collected at the gate electrode) in times on the order of picoseconds (Hughes, 1973). However, in that first picosecond or two, some fraction of the electrons and holes will recombine. This fraction depends greatly on the applied field and on the energy and type of the incident particle. The holes that escape initial recombination are relatively immobile and remain behind near their points of generation, causing negative voltage shifts in the electrical characteristics of MOS devices, e.g., in threshold voltage (V_T) for MOSFETs, or in flatband voltage (V_{fb}) for MOS capacitors. These

initial processes of pair creation and prompt recombination, which determine the actual charge (hole) yield in the SiO_2 film and consequently the initial (maximum) voltage shift, constitute the first major factor of the MOSFET response.

Over a period of time extending typically, at room temperature, from 10^{-7} second to the order of seconds (but much longer at lower temperatures), the holes undergo a rather anomalous stochastic hopping transport through the oxide in response to any electric fields present [shown moving toward the Si substrate for the gate bias situation depicted in Figure 2-6]. This hole transport process, which is very dispersive in time, is the second major factor of the MOS response. The holes that reach the silicon substrate through the transport process and undergo recombination give rise to a short-term recovery in initial voltage shift. The transport process itself is sensitive to a number

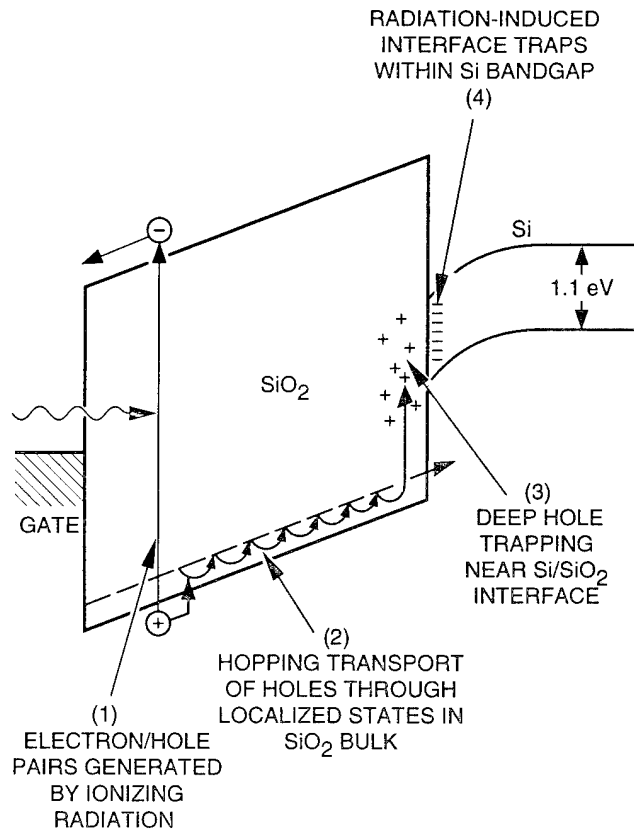


Figure 2-6. Schematic energy band diagram of SiO_2 MOS structure for positive gate bias (Srouf, 1983).

of variables, including applied voltage, temperature, oxide thickness, and (to a lesser extent) oxide process parameters (e.g., anneal temperature, etc.).

When the holes reach the SiO₂ interface (for positive applied gate bias), some fraction is captured in long-term trapping sites and causes a remnant negative voltage shift that is not sensitive to the silicon surface potential and persists in time for hours to years. This long-lived radiation-induced voltage shift component is the most commonly observed form of radiation damage in MOS devices. The long-term trapping of holes near the SiO₂/Si interface, as well as their subsequent annealing in time, constitutes the third major factor of MOS response indicated in Figures 2-6, 2-7, and 2-9. Hole trapping and annealing are very sensitive to the processing of the oxide and to other variables, such as field and temperature.

The fourth and final component of MOS response is that of a radiation-induced buildup of interface traps right at the SiO₂/Si interface. These are localized states with energy levels within the Si bandgap. Their occupancy is determined by the location of the Fermi level; consequently, the radiation-induced interface traps give rise to a voltage shift component that depends on the silicon surface potential. In general, there can be both prompt interface traps, present immediately after a radiation pulse, as well as a delayed time-dependent buildup of states, which can continue for thousands to tens of thousands of seconds at room temperature. Both the magnitude and nature (relative ratio of prompt and delayed components) of the interface traps are also highly dependent upon oxide processing, as well as upon other variables such as temperature and applied field (both magnitude and polarity).

A major electrical consequence of the radiation-induced charging of the SiO₂ film (including transporting holes, trapped holes, and interface traps) is a shift in pertinent voltage operating points for devices, such as in the threshold voltage V_T for a MOSFET. The threshold voltage is written:

$$V_T(t) = V_T^0 + \Delta V_T(t) \quad (2.1)$$

where V_T⁰ is the threshold voltage before irradiation and ΔV_T(t) is the time dependent voltage shift

following radiation exposure. The pre-irradiation threshold voltage is defined and its explicit expression is given in any textbook discussing MOS transistors (e.g., Sze, 1981). It depends upon temperature, gate-semiconductor work function difference, substrate doping density, oxide layer thickness, and substrate bias. There are also contributions to V_T from any fixed oxide charges and interface traps existing before irradiation.

Based on Figure 2-6 and its discussion, the radiation-induced threshold voltage shift can be subdivided into three components:

$$\Delta V_T(t) = \Delta V_{st}(t) + \Delta V_{ot}(t) + \Delta V_{it}(t) \quad (2.2)$$

where V_{st}(t) is the (short-term) contribution from the radiation-generated mobile holes transporting in the oxide bulk, V_{ot}(t) is due to the deep trapped holes near the interface, and V_{it}(t) is the contribution from the charged interface traps. Note that all three components are generally time dependent. They are given explicitly as:

$$\Delta V_{st}(t) = -\left(q/C_{ox}\right) \int_0^{t_{ox}} dx \left(x/t_{ox}\right) \times n_h(x,t) \quad (2.3a)$$

$$\Delta V_{ot}(t) = -\left(q/C_{ox}\right) \Delta N_{ot}(t) \quad (2.3b)$$

$$\Delta V_{it}(t) = -\Delta Q_{it}(t)/C_{ox} \quad (2.3c)$$

where q is the electronic charge, C_{ox} is the oxide capacitance per unit area (C_{ox} = ε_{ox}/t_{ox}), and t_{ox} is the oxide thickness (the subscript ox is the dielectric constant of the oxide). In Equation 2.3a, n_h(x,t) is the space- and time-dependent density of free (mobile) holes, and distance x in the oxide is measured relative to the gate/SiO₂ interface. In Equation 2.3b, N_{ot}(t) is the radiation-induced areal density of deep trapped holes near the SiO₂/Si interface; it is time dependent both because of its time-dependent buildup as the transporting holes reach the interface and because of its long-term annealing, which can extend out to years. In Equation 2.3c, the sign of the radiation-induced interface trapped charge Q_{it}(t) is unspecified because it can contribute either a net negative or net positive

charge, depending on the position of the Fermi level at the Si surface at inversion. [Usually, Q_{it} is negative for n-channel and positive for p-channel devices.] In general, a voltage offset is simply proportional to the first moment of the induced oxide charge relative to the gate interface. For the mobile hole distribution, Equation 2.3a retains this definition explicitly, since the transporting holes can be distributed through the bulk of the oxide. For both the long-term trapped holes and interface traps, $\langle x \rangle = t_{ox}$, with the resulting simplifications exhibited in Equations 2.3b and 2.3c. Positive charge induces a negative shift in V_T , and negative charge induces a positive shift.

To further aid in understanding some of the basic processes involved in the time-dependent response of MOS structures, Figure 2-7 illustrates the positions and magnitudes of the radiation-induced charges in the SiO_2 before and after an infinitesimally short radiation pulse. The processes depicted here include charge generation and initial recombination, hole transport, and long-term hole trapping. The annealing of the trapped holes and interface trap buildup are not included. Figure 2-8 illustrates the corresponding capacitance-voltage (C-V) curves schematically for an MOS capacitor for the times indicated in Figure 2-7.

The pre-irradiation condition ($t = 0^-$) is depicted in Figure 2-7(a) (no oxide charges), and the corresponding C-V curve is indicated by the $t = 0^-$ curve of Figure 2-8. At $t = 0$ [Figure 2-7(b)], the radiation pulse occurs, generating electron/hole pairs across the oxide bulk. In a time on the order of picoseconds ($t = 0^+$), some of the electron/hole pairs will recombine [Figure 2-7(c)], and the relatively highly mobile electrons will be transported toward the gate and be collected [Figure 2-7(d)]. The corresponding C-V curve is shifted far to the left in the negative voltage direction, as indicated by the curve labeled $t = 0^+$ in Figure 2-8. The magnitude of the flatband voltage shift $V_{fb}(0^+)$ is maximum at this time. Then the holes begin their relatively slow hopping transport toward the SiO_2/Si interface, where some fraction of them is captured in the long-term trapping sites. Figure 2-7(e) shows the intermediate situation at $t = t_1$, where

some holes are still being transported, some have reached the substrate and undergone recombination, and some have been trapped near the interface. Since a less positive charge remains in the oxide, the C-V curve has partially annealed back at $t = t_1$ in the positive voltage direction from its initial shifted position at $t = 0^+$. The final charge configuration ($t = t_2$) after completion of the hole transport is depicted in Figure 2-7(f), where only the long-term, trapped holes remain near the SiO_2/Si interface, giving rise to a long-term flatband voltage shift in the C-V characteristic, as indicated by the $t = t_2$ curve of Figure 2-8.

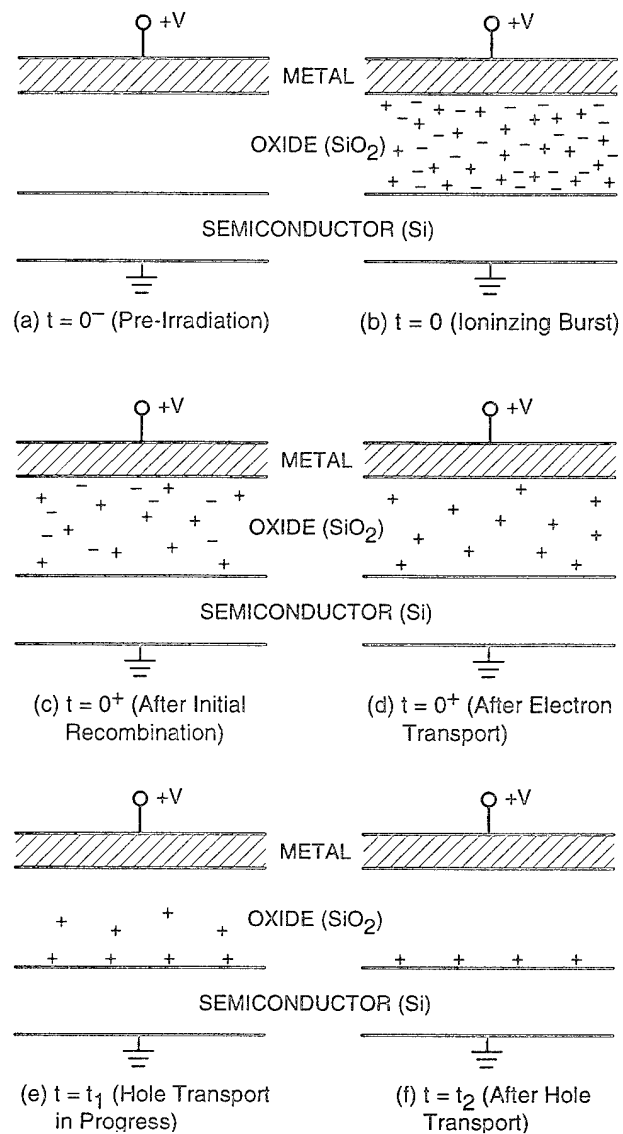


Figure 2-7. Illustration of recombination, transport, and trapping of carriers in SiO_2 films (Srouf, 1983).

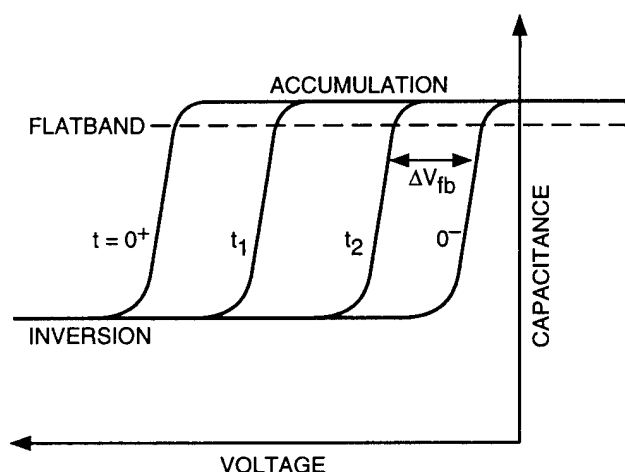


Figure 2-8. Capacitance-voltage curves corresponding to the conditions illustrated in Figure 2-7 (Srouf, 1983).

The overall actual situation is even more complicated than Figures 2-7 and 2-8 indicate. In general, long-term annealing of the deeply trapped holes is possible via tunneling of electrons from the Si substrate, which gives rise to a much slower recovery of the C-V curve near the pre-irradiation curve. In addition, radiation-induced interface traps can be present both immediately after irradiation ($t = 0^+$) as well as continuing to build up over long time periods. The interface traps not only contribute to the shift of device characteristics, but they also cause a distortion (stretchout) of the C-V or current-voltage (I-V) curves because the charge state of the traps is dependent upon the surface potential (and hence upon the applied bias).

A schematic, time-dependent recovery curve in Figure 2-9 depicts the radiation-induced shift in threshold voltage as a function of log-time from 10^{-6} to 10^8 seconds for a radiation-hardened n-channel MOSFET under positive gate bias at room temperature after exposure to a 1- μ sec ionizing radiation pulse. This figure is schematic in that real data are not shown (over the enormous time regime depicted), yet it is basically representative of the composite response of an actual hardened n-channel device. The figure relates the major features of the response of each of the primary processes indicated in Figure 2-6. The initial shift ΔV_T at 10^{-6} second, which is also the maximum shift, is determined mainly by the electron/hole

pair creation in the SiO_2 bulk and by the initial recombination processes. (However, some contributions from annealing by hole transport are possible during the pulse and from prompt interface-state production, which is low for a hardened oxide.) The short-term annealing shown occurring out to about 10^{-2} second is due to the hole transport process. The shift occurring at 10^{-2} second is primarily due to the deep hole trapping near the SiO_2/Si interface, which then anneals out slowly in time (approximately linearly with log-time), essentially out to infinite time [to 10^8 seconds in Figure 2-9].

The solid curve in Figure 2-9 corresponds to transport, trapping, and annealing of holes alone. In this situation, annealing includes: (1) short-term recovery, which occurs when the untrapped holes reach the substrate and recombine; and (2) long-term annealing (e.g., tunneling, etc.). In addition to long-term annealing of trapped holes, however, a buildup of radiation-induced interface traps may

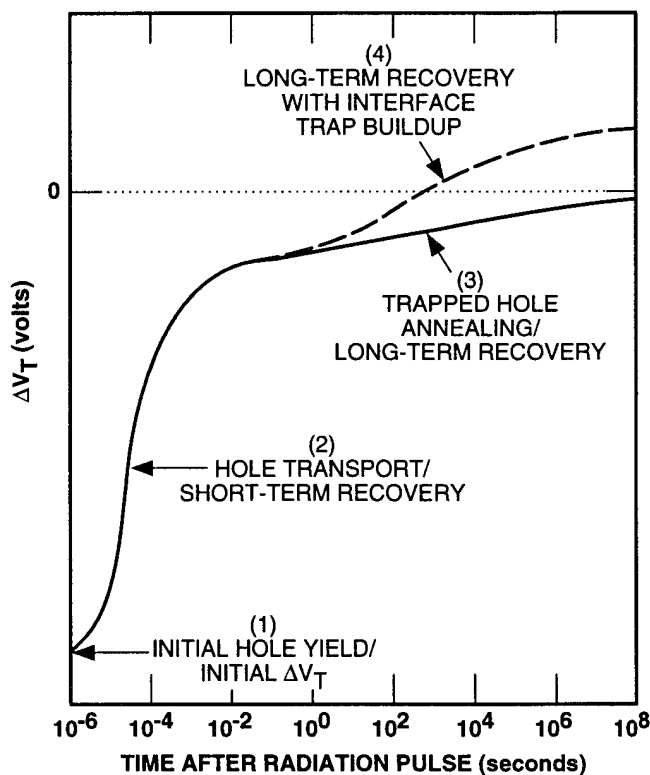


Figure 2-9. Schematic time-dependent threshold-voltage recovery of an n-channel MOSFET following pulsed irradiation, relating the major response features to underlying physical processes (McLean and Oldham, 1987).

occur, typically in the time regime between 10^{-2} and 10^3 seconds, as indicated by the dashed curve in Figure 2-9. [For an n-channel device, the interface-state contribution to ΔV_T is positive, corresponding to a net negative interface trapped charge at the threshold voltage.] If the interface trap contribution is relatively large, the threshold voltage may actually recover past its preirradiation value (i.e., ΔV_T positive), a phenomenon known as super-recovery, or rebound. This effect can also lead to circuit failure if it is sufficiently large. If a relatively large component of prompt interface traps is produced, then there would simply be an additional upward translation of the solid and/or dashed curves for all time. Again, because of the trapped positive charge annealing, super-recovery could occur.

In any case, because of the several different physical processes involved, each having different characteristic times, it is apparent that the overall time history of the recovery can be fairly complex, with important implications for testing procedures, hardness assurance, and resource prediction. In the simplest terms, it must be possible to extract from test data — usually over a very limited time regime and for a limited range of experimental conditions — the expected performance of an IC in a particular threat environment, which may involve a completely different time regime (perhaps orders of magnitude shorter or longer). Before addressing these issues, the basic physical processes responsible for the complex time history depicted in Figure 2-9 are discussed in further detail.

2.2.2 Physical Processes Underlying the Radiation Response of MOS Devices

In this subsection, more detail is given for each of the physical mechanisms described in Subsection 2.2.1 and displayed schematically in Figure 2-9. The intent is to provide the user with some familiarity with these processes by summarizing their major characteristics and indicating the main concepts used in their model descriptions.

2.2.2.1 Initial Hole Yield

The initial hole yield in the oxide determines the initial (maximum) voltage shifts of MOS devices

and sets the scale for the amount of damage (at any time) due to ionizing radiation. The two major factors that determine the initial hole density are the electron/hole pair creation energy and the field-dependent fraction of holes that escape the initial recombination processes. The initial value of the threshold voltage shift is then simply related to the initial hole density via the dose and geometric (oxide thickness) factors.

The electron/hole pair creation energy E_p for SiO_2 was determined by Ausman and McLean (1975) to be 18 ± 3 eV, based on the analysis of experimental data of Curtis, Srour, and Chiu (1974). This result has since been independently confirmed by others (Boesch and McGarrity, 1976; Sanders and Gregory, 1975), including a later, more accurate set of measurements and analysis by Benedetto and Boesch (1986), which establishes E_p to be 17 ± 1 eV.

From the value of E_p , the initial electron/hole pair density per unit dose is easily determined to be $8.1 \times 10^{12} \text{ cm}^{-3}/\text{rad}(\text{SiO}_2)$. This initial density, however, is quickly reduced by the initial recombination processes (occurring in picoseconds) before the electrons are swept out of the oxide and collected. The fraction of holes escaping initial recombination $f_v(E_{ox})$, which determines the final hole yield, is determined mainly by two factors: (1) the magnitude of the oxide electric field E_{ox} , which acts to separate the charge pairs; and (2) the initial line density of electron/hole pairs created by the incident radiation particle. The pair line density, which is determined by the linear energy transfer (LET) and therefore a function of the incident particle type and energy, is inversely proportional to the average separation distance between electron/hole pairs. Obviously, the closer the average spacing of the pairs, the more recombination that occurs for a given field and the less the final yield of holes.

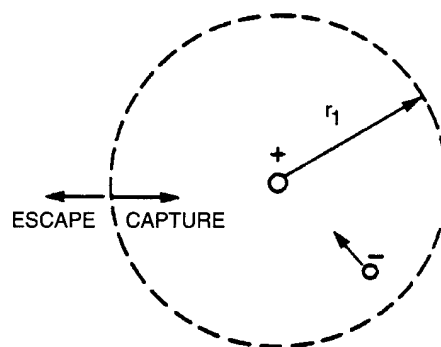
The initial recombination problem has not been solved analytically for arbitrary pair line density. However, analytic solutions do exist in the limiting cases, namely, where the charge pairs are far apart (geminate model) and the opposite, where the electron/hole pairs are very close together (columnar

model). The characteristic distance scale that distinguishes these cases is the thermalization radius of a single electron/hole pair, i.e., the average separation distance between an electron and hole of the same pair after they have dissipated their excess kinetic energy and reached thermal equilibrium energies. For SiO_2 , the average thermalization distance is about 8 nm (Ausman and McLean, 1975; Oldham, 1985).

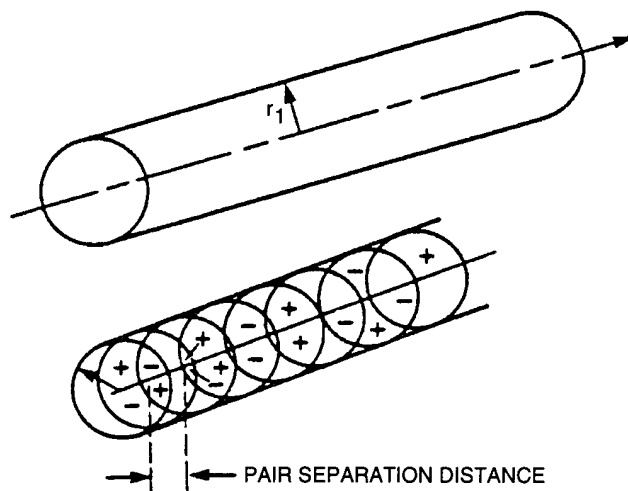
Figure 2-10 illustrates schematically the two limiting cases for which recombination models have been solved. For the geminate case [Figure 2-10(a)], the separation distance between pairs is much larger than the thermalization distance. Under such circumstances, only the recombination between the individual members of the same pair needs to be considered; i.e., it is only necessary to calculate the recombination probability of a single isolated charge pair whose members are attracted while, at the same time, they undergo both a drift motion (in opposite directions) in response to the local electric field and a random diffusive motion driven by the thermal fluctuations of the system.

Columnar recombination [Figure 2-10(b)] occurs when the average pair separation distance is much less than the thermalization distance. In this case, the individual electron/hole pairs lose their identity, and recombination must be considered between many electrons and holes lying in a cylindrical distribution around the track of the incident particle. Obviously, the probability of recombination of an individual carrier in this case is significantly greater than in the geminate model because of the enhanced probability of recombination encounters between opposite charges.

These models have been successfully applied to the initial recombination process in thermally grown SiO_2 films in recent years. For example, low-LET particles, such as high-energy electrons (including the high-energy secondary Compton electrons from ^{60}Co -gamma interactions), generate a sparse density of charge pairs along their tracks (for a 1-MeV electron, the average pair separation distance is about 50 nm), and the geminate model fits the results very well. On the other hand, very-high-LET particles, such as protons, alpha particles



(a) Geminate Model — Separate Electron/Hole Pairs



(b) Columnar Model — Overlapping Electron/Hole Pairs

Figure 2-10. Schematic diagrams indicating limiting pair separation distances for the geminate and columnar recombination models (McLean and Oldham, 1987).

and other heavier ions, generate high pair density along their tracks (for example, a 1-MeV proton generates, on average, an electron/hole pair about every 0.3 nm), and the columnar model successfully describes the experimental results. Many situations of practical interest fall in the transition region between these two models for the limiting cases of pair separation distance. However, the experimental results reflect a smooth continuous transition between the limiting cases. That is, intermediate cases show increasing columnar behavior (stronger recombination) as the density of electron/hole pairs is increased. Figure 2-11 is a compilation of a number of experimental results (Ausman and McLean, 1975; Benedetto and Boesch, 1986; Boesch and McGarrity, 1976; Curtis, Srour, and Chiu, 1974; Oldham and McGarrity, 1981) of the

fractional hole yield f_y versus electric field for a number of particles spanning the range from low to high LET. For these particle sources at a field of 1 MV/cm, the yield varies from almost 90 percent for low-LET particles (12-MeV electrons and ^{60}Co) to only about 6 percent for the high-LET 2-MeV alpha particles. This figure clearly shows that recombination is a real and often important effect when MOS responses to different radiation sources are compared.

Finally, knowing the initial pair volume density per rad ($g_0 = 8.1 \times 10^{12} \text{ cm}^{-3}/\text{rad}[\text{SiO}_2]$) and the fractional hole yield after recombination $f_y(E_{\text{ox}})$ [from Figure 2-11], the initial threshold (or flatband) voltage shift is easily obtained. Assuming a uniform generation density across the oxide layer, the total initial areal charge density of holes that escape recombination is $Q_h = q g_0 t_{\text{ox}} f_y(E_{\text{ox}})D$, where t_{ox} is the oxide thickness and D is the dose in rads(SiO_2). The initial threshold shift is related to Q_h as:

$$\Delta V_T(0^+) = \frac{\Delta Q_h}{2C_{\text{ox}}} \quad (2.4)$$

$$= \frac{[q g_0 t_{\text{ox}} f_y(E_{\text{ox}})D]}{2C_{\text{ox}}}$$

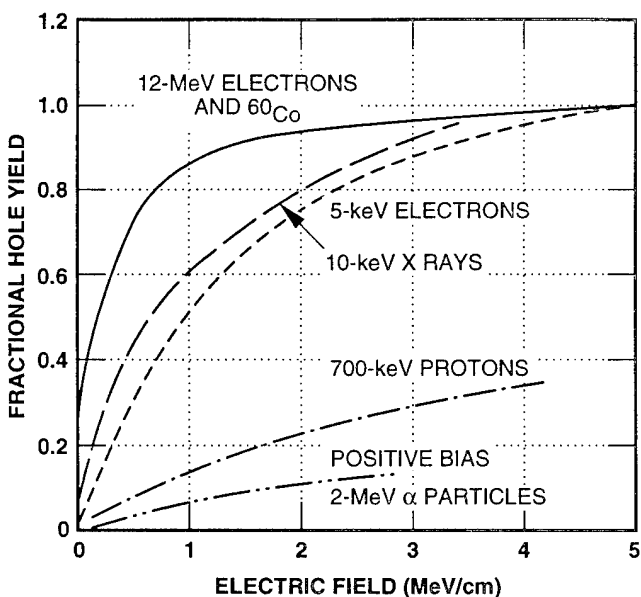


Figure 2-11. Experimentally measured fractional hole yield versus electric field (in SiO_2) for several incident particles (McLean and Oldham, 1987).

where $C_{\text{ox}} = \epsilon_{\text{ox}}/t_{\text{ox}}$. The factor of 2 comes from the fact that the centroid of a uniform charge density is $t_{\text{ox}}/2$, and a negative voltage shift is indicated corresponding to the positive sign of the induced charge. Finally, substituting for the constant factors in Equation 2.4:

$$-\Delta V_T(0^+) = 1.9 \times 10^{-8} t_{\text{ox}}^2 f_y(E_{\text{ox}})D \quad (2.5)$$

Here, the units of V_T are volts if t_{ox} is expressed in nanometers, and D is in rads(SiO_2). Equation 2.5 explicitly shows the dependence of the initial voltage shifts on oxide thickness squared, indicating a significant improvement in the radiation susceptibility of devices having thinner gate oxides.

2.2.2.2 Hole Transport

The transport of the holes through the SiO_2 oxide layer to the silicon substrate and their subsequent recombination there, which is responsible for the early-time recovery of V_T [Figure 2-9], has been studied extensively by several groups, including Boesch *et al.* (1975). This process has been found to exhibit some rather unusual properties; the principal ones are listed below:

1. It is highly dispersive in time, taking place over many decades in time following a radiation pulse.
2. It is universal in nature, meaning that changes in temperature, field, and thickness do not affect the shape or overall dispersion of the recovery curves when plotted in terms of log-time. Changes in these variables affect only the time scale for the recovery.
3. The transport is field activated.
4. At temperatures above about 140°K , the transport has an Arrhenius-type temperature activation dependence; below 140°K , the transport essentially becomes thermally nonactivated.
5. The characteristic recovery time, or hole transit time, has a strong superlinear power-law dependence on oxide thickness.

Many of these features, such as the dispersion in time, universality, and superlinear thickness dependence, can be directly attributed to a wide distribution of transit times of the individual holes through the material. The wide distribution of transit times is a result of a broad distribution of individual (microscopic) event times, which extend into the time range necessary for the fastest carriers to transit through the sample. In essence, while some carriers transit the sample very rapidly via a succession of rapid events (i.e., hops), other carriers are immobilized at some point for times on the order of, or greater than, the transit time of the fastest carriers. Such broad distributions of event times can be easily envisioned in two simple situations. First, in hopping transport, small fluctuations (due to disorder) in either the intersite hopping distance or in activation energy, or even in bond angles, can produce large variations in the hopping transfer integrals and hence lead to large variations in hopping times. Second, for transport mediated by traps (multiple trapping), in which the carriers move via normal band conduction between trapping events, relatively small variations in the trap energy level can lead to a broad distribution of release times from the traps. These simple models are indicated schematically in Figure 2-12.

The specific intersite hopping transfer mechanism seems most likely to be small polaron-like hopping of the holes between localized, shallow trap states having a random spatial distribution but separated by an average distance of 1 nm. [The

term polaron refers to the situation where the charge carrier (hole in our case) strongly interacts with the surrounding medium, inducing a significant distortion of the lattice or atom network in the immediate vicinity of the carrier (also sometimes referred to as self-trapping of the carrier).] As the carrier moves through the material via hopping, it carries with it the accompanying lattice distortion. The strongest evidence for the polaron hopping mechanism is the transition from thermally activated behavior above $\sim 140^\circ\text{K}$ to an essentially nonactivated transport at lower temperature.

Some of the salient features of hole transport are illustrated by the data sets shown in Figures 2-13 and 2-14. Figure 2-13 shows the effect of temperature and Figure 2-14 the effect of oxide electric field. These data are measurements of the flatband voltage shift versus log-time from 10^{-4} to 10^3 seconds following pulsed 12-MeV electron (LINAC) irradiation of MOS capacitors. The data in these figures are well normalized to the initial shifts $\Delta V_{fb}(0^+)$ immediately after the radiation pulse. The initial shifts are not those at the earliest measurement ($\sim 10^{-4}$ second), but rather are the calculated shifts before any transport occurs. The actual values of $\Delta V_{fb}(0^+)$ vary with dose, field, and thickness as described in Subsection 2.2.2.1. The data are plotted in the negative direction because the voltage shifts are negative, indicative of net positive charge induced in the oxide layer. Figure 2-13 shows the response for a series of temperatures between 125°K and 293°K at a single oxide field

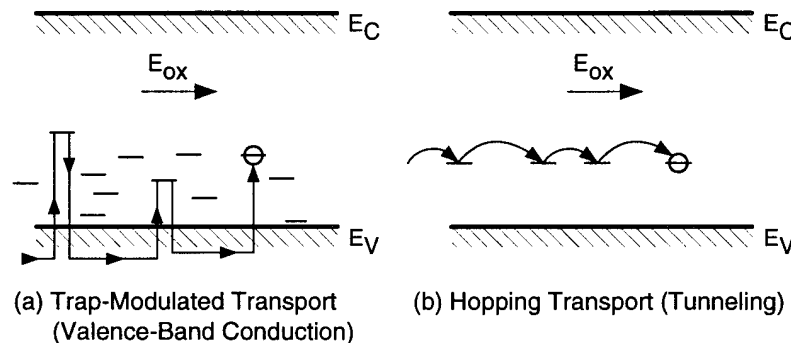


Figure 2-12. Schematic diagrams of the trapped-modulated and hopping transport models, both of which lead to large dispersion in carrier transit times (McLean and Oldham, 1987).

of 1 MV/cm. The strong temperature activation above 141°K is apparent; in fact, plotting the time, say, at which half-recovery occurs versus $1/T$ (Arrhenius-type plot) yields a straight line, the slope of which yields an activation energy of ~ 0.60 eV. Figure 2-14 shows the response at a constant temperature of 79°K with oxide field as a parameter in the range from 3 to 6 MV/cm.

The large amount of time dispersion is apparent in both Figures 2-13 and 2-14, with the recovery taking place over many decades in time (approximately 8 to 10 decades from start to finish). The universal feature of the transport is also evident in the data in that changes in an external parameter [temperature in Figure 2-13 and field in Figure 2-14] do not seem to have much effect on the shape of the recovery curves when log-time plotted. Rather, the major effect of changes in these parameters is simply to produce a rigid translation of the curves along the log-time axis; that is, only the time scale for the transport is affected and not the amount of dispersion. In fact, if these data are replotted in time units scaled to a characteristic recovery time (e.g., half-recovery time), the data for different parameter values essentially trace out the same universal curve. This is shown in Figure 2-15 for the temperature data of Figure 2-13, where the data for all temperatures in terms of

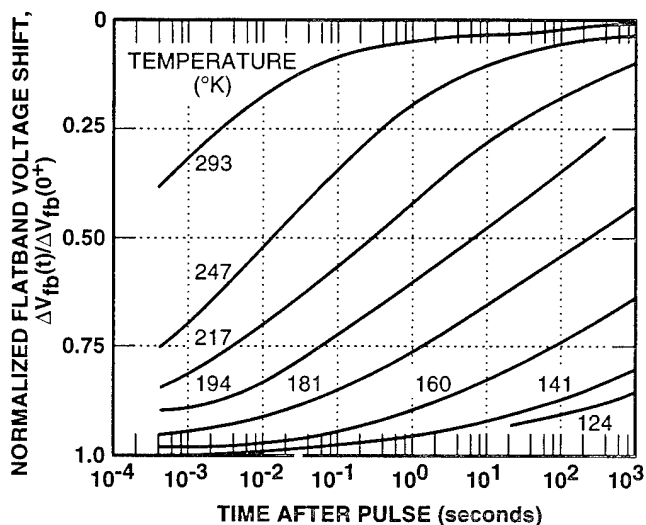


Figure 2-13. Normalized flatband voltage recovery data following pulsed 12-MeV LINAC electron irradiation of 96.5-nm oxide MOS capacitor under 1-MV/cm oxide field for various temperatures (Boesch *et al.*, 1978).

scaled time trace out a universal curve over ten or more decades in time. In several instances, data points from as many as five temperatures overlap to a considerable degree in the same region of scaled time.

The almost complete flatband recovery at late times and high temperatures in Figure 2-13 indicate very little long-term, or permanent, trapping of holes in this particular sample; a trapping fraction of < 2 percent is indicated by these data. Hence, this particular oxide is a "good" (i.e., clean, radiation-hard) oxide in which to analyze the hole transport, not complicated by effects associated with deep hole traps. Be aware that the deep hole-trapping fraction can vary greatly among different oxides, so care must be exercised when quantitatively characterizing hole transport properties if the trapping fraction is large.

Figures 2-13 and 2-14 indicate that little transport or recovery occurs at the lowest temperatures until relatively long times on the scale of the experiments. For example, at 80°K and for $E_{ox} = 3$ MV/cm, the recovery begins only after 10 seconds [Figure 2-14]. In fact, for $E_{ox} < 2$ MV/cm, essentially no recovery takes place at 80°K for times on the order of thousands of seconds; the holes remain frozen in place very near their point of generation.

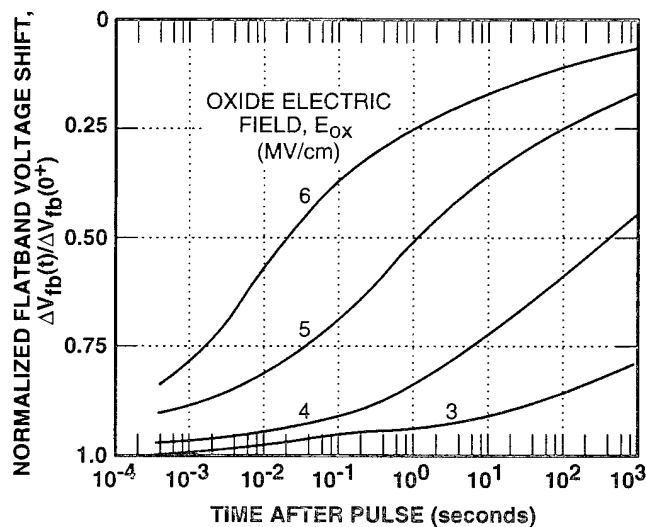


Figure 2-14. Normalized flatband voltage recovery data following pulsed LINAC electron-beam exposure for 96.5-nm oxide MOS capacitor at 80°K and for oxide fields from 3 to 6 MV/cm (McGarrity *et al.*, 1978).

This feature has been used in studies of the charge yield in SiO_2 (Boesch and McGarrity, 1976; Oldham and McGarrity, 1983; Sanders and Gregory, 1975). It also has severe implications for the operation of SiO_2 MOS devices at cryogenic temperatures if they are exposed to ionizing radiation. Indeed, there would be no short-term recovery of the devices, as is the case at room temperature [Figure 2-9]; the threshold voltage shift would remain essentially at its maximum initial value for all practical times.

2.2.2.3 Deep Hole Trapping and Annealing

Following exposure to ionizing radiation and after the radiation-generated holes have been transported through the oxide, MOS structures typically exhibit a negative voltage shift component ΔV_{ot} in their electrical characteristics (e.g., V_T , V_{fb}) that is not sensitive to silicon surface potential and persists for hours to years. This long-lived radiation effect component is the most commonly observed form of radiation damage in MOS devices and is attributed to the long-term trapping of some fraction of the radiation-generated holes in the oxide layer within ~ 10 nm of the SiO_2/Si interface. This effect generally dominates other radiation damage processes in MOS structures, including negative

charge (electron) trapping and interface-state buildup effects, unless specific device-processing changes are made to alter the oxide and consequently reduce the hole trapping or enhance the other effects.

Again, it must be stressed that radiation effects involving interface phenomena in general (hole trapping and long-term annealing [removal] of trapped holes, interface trap buildup) are all highly dependent upon oxide processing. The different effects vary by orders of magnitude for these phenomena among oxides of varying processing histories, in contrast to the bulk phenomena of charge pair generation, recombination, and hole transport, in which remarkably little variation is observed among thermal oxides of greatly different processing. Consequently, in terms of minimizing long-term damage effects associated with the interface phenomena, proper control of oxide (circuit) processing has been, and continues to be, a major thrust of radiation-hardening efforts.

The effect of processing on the fraction of holes that undergo deep, long-lived trapping is illustrated by the data shown in Figure 2-16. Here, the threshold voltage shifts versus ionizing radiation dose are plotted for two n-channel devices where the radia-

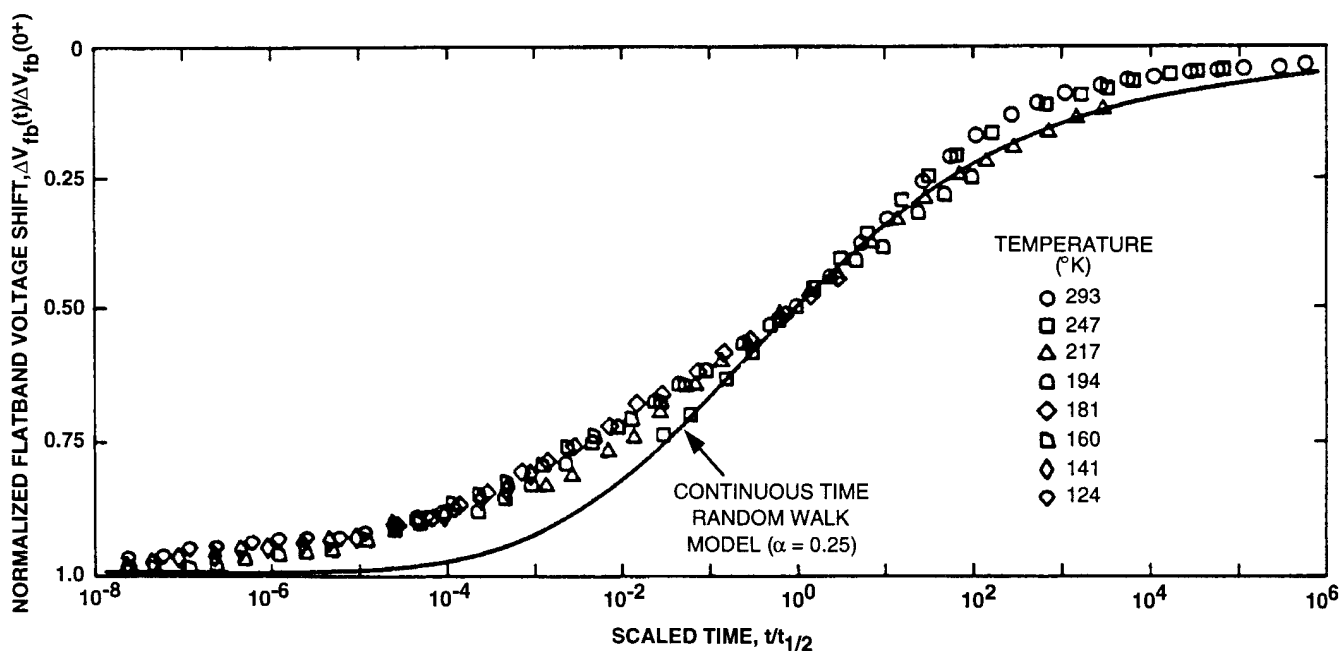


Figure 2-15. Normalized flatband voltage recovery data of Figure 2-13 ($E_{\text{ox}} = 1$ MV/cm) replotted with time scaled to half-recovery time, illustrating the universality of response with respect to temperature (McGarrity *et al.*, 1978).

tion hardness was varied by changing the high-temperature processing. The dose rate was 8×10^4 rads/min, and the measurements were obtained within 10 minutes of the exposure at each dose. Clearly, at each dose there is roughly an order-of-magnitude difference in the threshold voltage shift, which in turn is most likely due to an order-of-magnitude difference in the number of hole traps present in the two oxides. In general, the fraction of radiation-generated holes that undergo long-term deep trapping has been found to vary from as little as 1 or 2 percent for a good, hardened oxide, to the order of 10 to 20 percent for good-quality commercial oxides, and to as much as 50 to 70 percent in very soft commercial oxides.

Evidence concerning the location of the trapped holes is contained in Figure 2-17, which shows long-term flatband voltage shift ΔV_{fb} measured in MOS capacitors on n-type silicon irradiated to 1 Mrad(SiO_2) at gate voltages from -10 to $+10$ volts. The flatband shift for negative gate voltage V_G includes contributions from both the oxide-trapped charge and radiation-generated interface states, but the response is dominated by the trapped-hole component. The shift under positive V_G is much greater than that observed at equivalent negative V_G . From similar data, it has been inferred that the

positive oxide charge must be fairly mobile since it apparently moves rapidly toward, and is trapped near, the SiO_2/Si interface under positive bias and moves toward the gate under negative bias. If bulk trapping were involved rather than trapping near the interfaces, the shifts for positive and negative polarity for the same field magnitude would not differ nearly as much as the data in Figure 2-17. A great amount of other work indicates that the location of the long-term trapped holes under positive gate bias is generally within ~ 10 nm of the SiO_2/Si interface (Grove and Snow, 1966; Oldham, Lelis, and McLean, 1986).

In addition to the location of the trapped holes in the oxide within ~ 10 nm of the SiO_2/Si interface and the fact that the hole-trapping fraction is highly dependent on processing, other pertinent pieces of information concerning the characteristics of the hole traps — obtained from the work of many investigators over the years — include the following:

1. The number density of the hole traps typically lies in the range from 10^{18} to 10^{19} cm^{-3} (Boesch *et al.*, 1986; Grove and Snow, 1966), with the corresponding areal density ranging from 10^{12} to 10^{13} cm^{-2} .

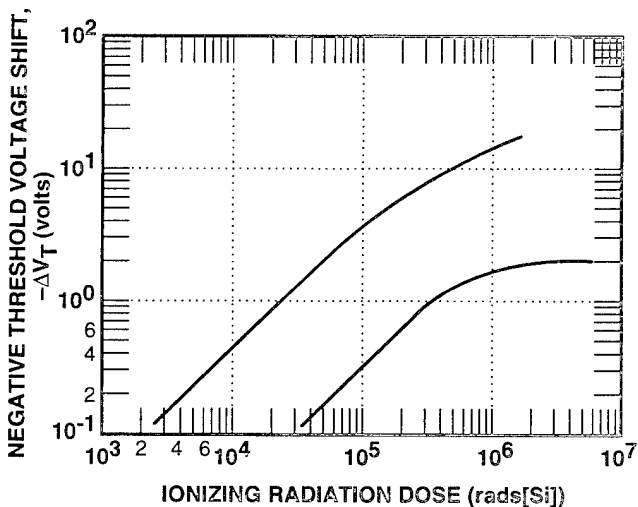


Figure 2-16. Effect of processing on hole trapping; threshold voltage shift versus ionizing radiation dose for two n-channel MOSFETs ($V_G = +10$ volts) receiving different high-temperature processing (Derbenwick and Sanders, 1977).

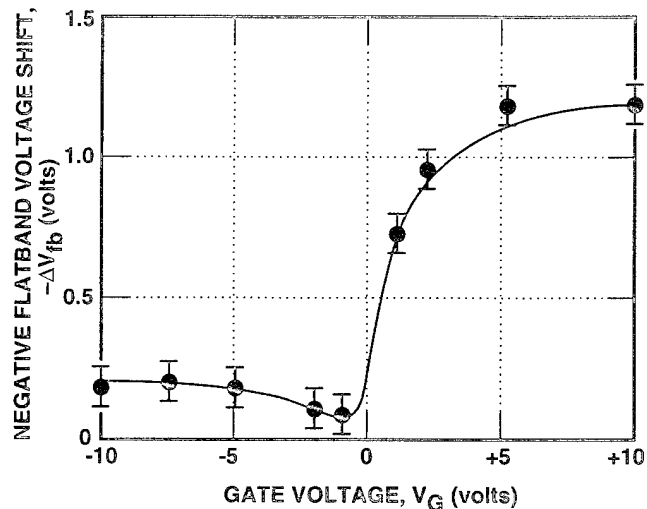


Figure 2-17. Bias dependence of radiation-induced voltage shift; flatband voltage shift versus gate voltage for a MOS capacitor following a 1-Mrad (SiO_2) exposure ($t_{ox} = 70$ nm) (Derbenwick and Gregory, 1975).

2. The cross section for hole trapping is usually found to be around 5×10^{-14} cm² for a 1-MV/cm oxide field (Aitken and Young, 1977; Boesch *et al.*, 1986).
3. The cross section decreases as $E_{ox}^{-1/2}$ for fields above 1 MV/cm in magnitude (Boesch and McLean, 1985; Dozier and Brown, 1980; Tzou, Sun, and Sah, 1983). For the data shown in Figure 2-16, the increase in V_{fb} as the bias is increased from zero is attributed to the increased yield of holes with increasing field; but the flattening of the curve for larger positive bias (and sometimes a turnaround has been observed) is probably due to the decreasing cross section for hole capture as the field increases above 1 MV/cm.
4. It is commonly observed (Boesch and McGarrity, 1976; Boesch *et al.*, 1986; Churchill, Collins, and Holmstrom, 1974; Collins, Holmstrom, and Churchill, 1979; Hughes and Seager, 1983) that the total number of trapped holes N_{ot} tends to a saturation level in the 1- to 10-Mrad dose range. Depending on specific circumstances, this is due to one or more operating factors, including trap filling (hard saturation), large space-charge effects to the point of field reversal in some regions of the oxide layer, and recombination of the trapped holes with radiation-generated electrons moving through the trapped-hole distribution.
5. Based upon an increasing accumulation of electron spin resonance (ESR) spectroscopy data (Lenahan and Dressendorfer, 1983; Marquardt and Sigel, 1975; Sigel *et al.*, 1974), the microscopic structure of the trapped holes seems to be the so-called E'_1 center, which is a trivalent silicon defect associated with an oxygen vacancy in the SiO₂ structure (Feigl, Fowler, and Yip, 1974; Griscom, 1984; Silsbee, 1961).

In essence, present evidence suggests the following model for the hole-trapping process. The SiO₂/Si interface region of MOS structures is characterized by high local strain and a deficiency of oxygen atoms, resulting in a number of strained Si-Si bonds (instead of normal Si-O-Si bonding configurations). A hole encountering such a strained bond may break the bond and recombine with one of the bonding electrons. The resulting positively charged structure relaxes to the E'_1 center configuration, with one of the Si atoms retaining the remaining electron from the broken bond and the positive charge residing with the other trivalent Si atom. Figure 2-18 shows a simple schematic of the trapping process.

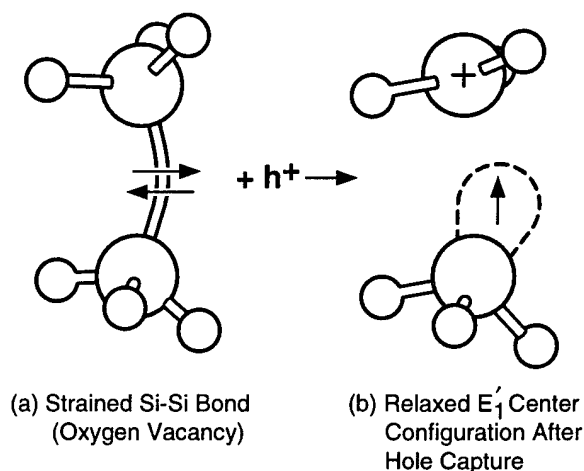


Figure 2-18. Schematic of hole-trapping process (Boesch, n.d.).

Regarding the question of the long-term stability of the deeply trapped holes, it is to be noted that the holes in deep traps in the SiO₂ layer of an MOS structure after irradiation are not truly "permanently" trapped. Instead, they are observed to disappear from the oxide over times from milliseconds to years. This discharge of the trapped holes, as commonly observed at or near room temperature, is the major contributor to the so-called "long-term annealing" of radiation damage in MOS devices. The annealing of the trapped holes has two manifestations that may reflect different hole-removal processes. The first is the slow, bias-dependent recovery of ΔV_{ot} , typically observed at normal device operating temperatures (-55 to 125°C , for instance). Aspects of this process have

been described through a tunneling model. The second is the relatively rapid and strongly temperature-dependent thermal detrapping or recombination of the holes observed when MOS structures are deliberately subjected to thermal annealing cycles at elevated temperatures (150 to 350°C). This process has been described through a thermal detrapping model. The focus of the discussion here is restricted to the “tunnel anneal” process, important at normal operating temperatures.

Figure 2-19 presents typical results for the time dependence of hole annealing at room temperature. Midgap voltage shift, ΔV_{mg} ($\sim V_{ot}$), is plotted as a function of time after irradiation for three n-channel MOSFET samples with different dry-oxide processing. The discharge of the trapped holes is roughly linear in $\log(t)$. This behavior is a hallmark of the hole-annealing process and has been used in convolution schemes for predicting the response of MOS devices under low-dose-rate irradiation conditions (Derbenwick and Sanders, 1977; Winokur, 1982; Winokur, Kerris, and Harper, 1983). Note that the three devices shown in Figure 2-19 have been irradiated to different doses to achieve roughly comparable shifts for the first measurements (20 krad for the soft samples, 90 krad for the intermediate samples, and 1 Mrad for the hard samples).

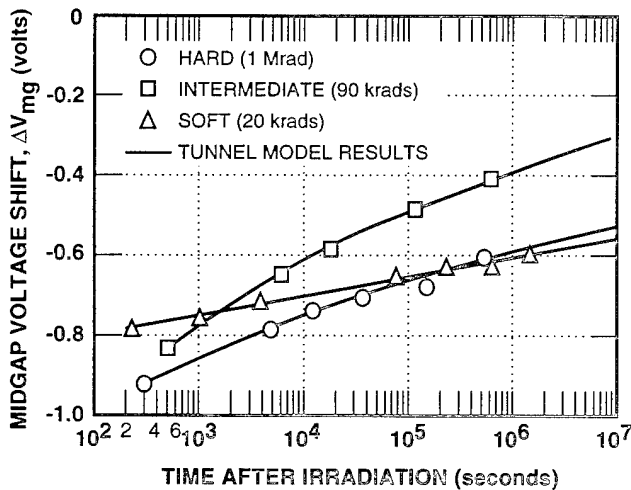


Figure 2-19. Long-term annealing data for three MOSFETs of varying radiation hardness; devices received the doses indicated to produce comparable initial shifts (Oldham, Lelis, and McLean, 1986).

Several investigators have suggested a tunneling process to explain the $\log(t)$ recovery and other aspects of hole annealing in MOS structures (Benedetto *et al.*, 1985; Boesch *et al.*, 1978; Manzini *et al.*, 1983; Oldham, Lelis, and McLean, 1986; Saks, Ancona, and Modolo, 1984). These models assume that electrons from the silicon substrate tunnel to, and recombine with, the trapped holes in the distribution of traps near the SiO_2/Si interface, as illustrated by the schematic diagrams in Figure 2-20. [Equivalently, the holes can be thought of as tunneling from the traps to the silicon valence band.] As a consequence of the exponential decay of the tunneling probability with distance into the SiO_2 , at a given time t the hole traps are emptying from the silicon at a depth $X_m(t)$ that increases logarithmically with time (McLean, 1976; Ross and Wallmark, 1969):

$$X_m(t) = \left(\frac{1}{2\beta} \right) \ln(t/t_0) \quad (2.8)$$

where β is the tunneling barrier height parameter and t_0 is the time-scale parameter. For distances only slightly greater than X_m , essentially all the traps remain full at time t ; for distances only slightly less than X_m , essentially all the traps have been emptied by tunneling. Thus, hole removal proceeds via a “tunneling front” that moves into the oxide with a “velocity” $\Delta X_m = 1.15/\beta$ per decade in time. [Manzini *et al.* (1983) and Benedetto *et al.* (1985) have found ΔX_m to be

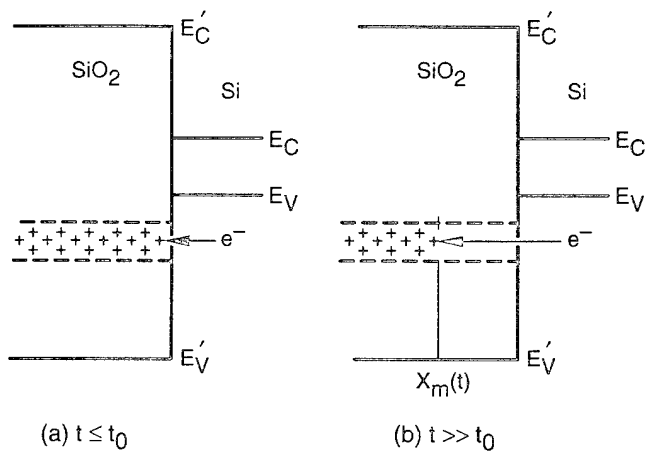


Figure 2-20. Schematic of trapped-hole removal by electron tunneling from silicon substrate (McLean and Oldham, 1987).

about 0.2 nm per decade.] For $X_m \ll t_{ox}$ and a uniform distribution of traps in the oxide within tunneling distance of the silicon, the resulting trapped-charge loss (and hence the decrease in ΔV_{ot}) at a given time due to the tunnel anneal is then proportional to X_m ; i.e., ΔV_{ot} decreases as $\ln(t)$. Thus, the tunneling model explains qualitatively the observed approximate $\log(t)$ anneal of the trapped holes.

What this simple model fails to do is describe the observed responses in detail. As shown in Figure 2-19, the annealing curves are not completely linear; the rate of annealing tends to decrease with time. This is to be expected, since the rate of annealing should approach zero as the amount of charge left to be removed (remaining ΔV_{ot}) approaches zero. The simple $\log(t)$ anneal arises from the assumption that the trapped holes are distributed uniformly into the oxide from the silicon interface. In reality, the hole trap density generally falls off with distance from the silicon. Oldham, Lelis, and McLean (1986) assumed an exponential falloff in occupied hole-trap density from the interface and incorporated this form into the appropriate expressions from tunneling theory, yielding the solid-line fits to the data as shown in Figure 2-19. An important conclusion from this analysis was that the trapped-hole distribution lies close to the SiO_2/Si interface in hard oxides (i.e., the distribution falls off relatively sharply from the interface), whereas it extends deeper into the oxide bulk for the soft oxides. This is apparently related to the size of the strained, oxygen-deficient region near the interface, a property highly dependent upon processing conditions. The fact that the tunneling rate depends exponentially on tunneling distance then explains the many orders of magnitude variation in long-term annealing rates among different oxides (Johnston and Roeske, 1986).

Additional aspects of the tunnel-anneal process are its dependencies upon temperature and oxide field. The temperature effect seems to be adequately explained (Manzini *et al.*, 1983) by a linear temperature dependence of the trap energy levels, $E_t(T) = E_t^0 - bT$, where $E_t^0 = 3.6$ eV and $b = 2.0$ meV/°K. The electric field dependence arises

from the field modification of the tunneling potential barrier height; a positive electric field has the effect of lowering the barrier to tunneling and thereby increases the rate of annealing.

2.2.2.4 Radiation-Induced Interface Traps

Interface traps N_{it} are localized electronic states located at or very near the SiO_2/Si interface, having their energy levels distributed within the Si bandgap. They can exchange charge with the Si conduction and valence bands. Their occupancy, or charge state, depends upon the position of the Fermi level at the interface, i.e., upon the value of the surface potential. The major effects of N_{it} in MOS systems are to (1) produce distortions in device characteristics (e.g., C-V or I-V) as the gate bias is varied, (2) shift the threshold voltage due to the net interface trapped charge at the turn-on or inversion point, and (3) introduce additional Coulomb scattering centers for carriers moving in the surface channel of a MOSFET, which degrade the carrier mobilities. Before irradiation, the area density of interface traps in good, modern devices is $\leq 10^{10}$ cm⁻²; for such a density, N_{it} effects normally are not much of a problem.

Upon irradiation, however, interface traps can build up to a significant level, resulting in discernible effects in devices. In general, two components of radiation-induced interface traps have been observed: (1) a prompt component present at the earliest measurements following an irradiation, and (2) a time-dependent component that can continue building up for thousands of seconds. The relative ratio of the two components can vary greatly, with one or the other dominating in a particular system. As a general statement, the delayed time-dependent N_{it} seems to dominate in metal (aluminum) gate devices (Winokur, McGarrity, and Boesch, 1976; Winokur *et al.*, 1977; Winokur *et al.*, 1979; Winokur and Boesch, 1980; Winokur, McLean, and Boesch, 1986), prompt N_{it} dominates in thick, steam oxides (as used as field oxides) (Boesch, 1982; Boesch and Taylor, 1984), and both components seem to be present in more or less comparable amounts in polysilicon gate devices (Schwank *et al.*, 1986) that are more representative of present-day technology.

An example illustrating the effect of the time-dependent N_{it} buildup is shown in Figure 2-21, which displays C-V traces of an aluminum-gate, dry-oxide MOS capacitor, both before irradiation and for a series of times from 0.04 to 400 seconds following a pulsed 200-krad(SiO_2) LINAC electron beam exposure. At the first measurement following irradiation (0.04 second), the C-V curve is simply shifted along the negative voltage axis without any discernible change in its shape compared to the pre-irradiation trace, indicative simply of a positive charge being induced in the oxide. The 0.4- and 4-second curves show a rigid shift back in the positive voltage direction with little change in shape because of a combination of the tail end of the hole transport process and the deep trapped-hole annealing. However, the significant stretchout seen to occur between 4 and 40 seconds becomes even greater at 400 seconds. This distortion is directly attributed to the delayed buildup of radiation-induced N_{it} .

Figure 2-22 shows the time-dependent buildup of interface trap density (for states with energies between midgap and inversion) for Al-gate, wet-oxide capacitors for a series of oxide fields be-

tween 1 and 6 MV/cm, from 2×10^0 to almost 10^5 seconds following pulsed LINAC irradiation. Note that the final N_{it} levels in this case are almost solely due to the time-dependent buildup process. There is obviously a strong field dependence on both the rate of buildup and the final value of N_{it} . For all fields, the buildup apparently begins on the order of seconds (the point at 1 second on Figure 2-22 is also the pre-irradiation N_{it} value), continuing for several hundred seconds at the highest field (6 MV/cm) before leveling off. For the lower field values (1 and 2 MV/cm), the generation rate is much lower, but N_{it} is still seen to be increasing even at the latest measurement times.

In Figure 2-23, the field dependence of the radiation-induced interface trap buildup is compared for three types of MOS capacitors: (1) aluminum gate, (2) polysilicon-gate samples receiving "typical Si-gate processing," and (3) special "hardened" Si-gate capacitors. Plotted in the figure is the increase in interface trap density between midgap and inversion following 1-Mrad(SiO_2) irradiation as a function of oxide electric field for both positive and negative polarities. ΔN_{it} contained both prompt and delayed time-dependent components

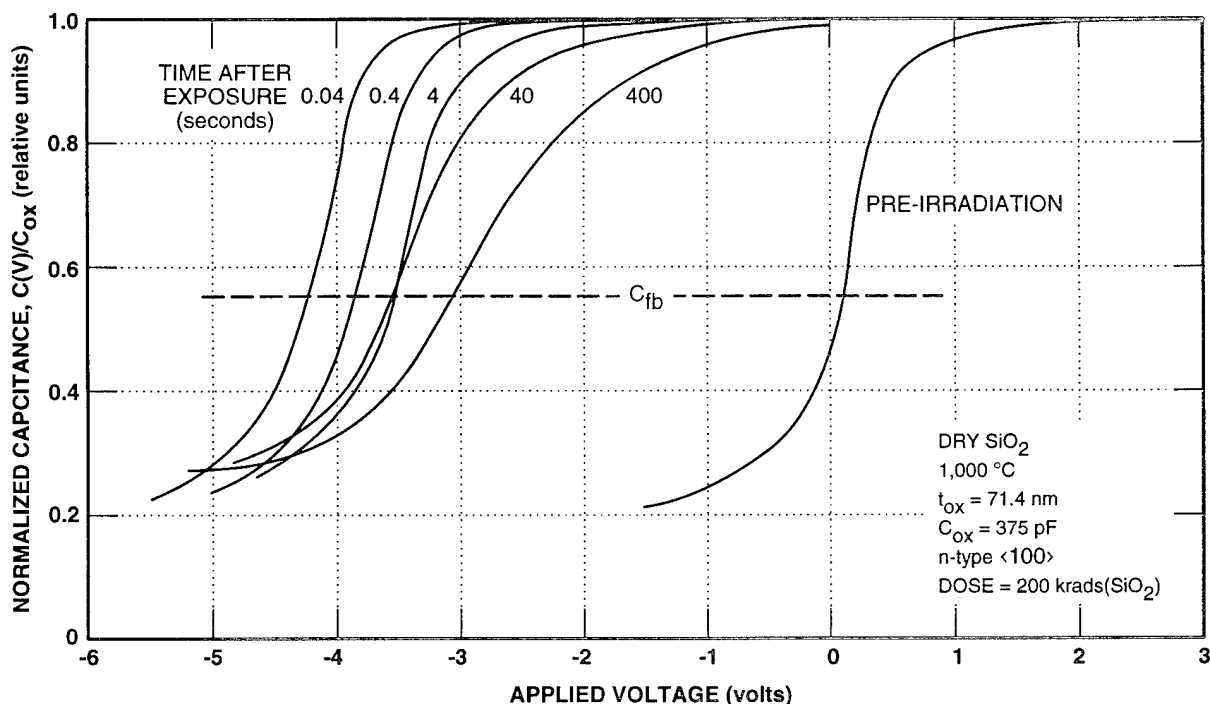


Figure 2-21. High-frequency 1-MHz C-V curves of MOS Al-gate capacitor at several times following pulsed electron beam irradiation (Winokur, McGarrity, and Boesch, 1976).

for the Si-gate samples. In all three samples, ΔN_{it} is much less under negative bias polarity than positive polarity [note the log scale for ΔN_{it}]. The N_{it} buildup for the Al-gate capacitors increases with increasing positive field, in general agreement with the earlier data of Figure 2-22. However, the Si-gate capacitors exhibit a rapid increase in N_{it} production for positive fields up to ~ 1 MV/cm, which peaks in the range from 1 to 2 MV/cm but then drops off somewhat at higher fields. It is clear that

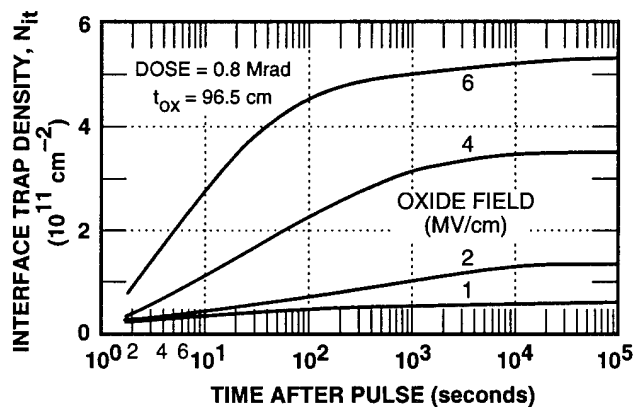


Figure 2-22. Integrated interface trap density between midgap and inversion surface potentials as a function of time following pulsed electron-beam (LINAC) exposure for several oxide field values; 0.8-Mrad dose, wet-oxide Al gate, $t_{ox} = 96.5$ nm (Winokur *et al.*, 1977).

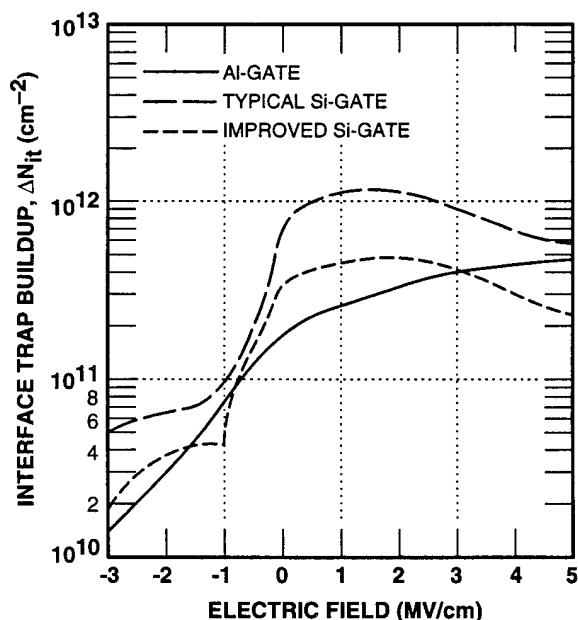


Figure 2-23. Oxide field dependence of radiation-induced interface trap buildup following 1-Mrad (SiO_2) irradiation in three MOS capacitors having different gate structures (Winokur *et al.*, 1985).

some qualitative differences exist in the mechanisms of N_{it} buildup in Al-gate and Si-gate systems. These differences are not understood at the present time, although they are likely to be associated with differences in the nature of the generation mechanisms for the prompt and delayed time-dependent components. Note also in Figure 2-23 that for normal operating fields of 1 to 2 MV/cm, ΔN_{it} for the typical commercial Si-gate process is about five times greater than that for the Al-gate samples. This increased ΔN_{it} is commonly observed for Si-gate technologies.

The discussion thus far has attempted to illustrate some of the major observations that have been made concerning the buildup of radiation-induced interface traps, such as the existence of prompt and delayed time-dependent components, the strong bias polarity effect, the dependence on the magnitude for positive fields, and the strong dependence on oxide processing, including the differences between aluminum-gate and polysilicon-gate structures. At the present time, the precise mechanisms responsible for the interface trap buildup are not well understood, and, in fact, the general area of SiO_2/Si interface traps and their generation under various stresses (radiation, high electric fields, hot-carrier injection, etc.) is a complex subject of intense current interest and debate. However, some observations concerning these phenomena include:

1. There is much evidence that N_{it} buildup is associated with the hole transport, trapping, and annealing processes (Boesch *et al.*, 1986; Lai, 1983; McGarrity *et al.*, 1978; Winokur, McGarrity, and Boesch, 1976; Winokur *et al.*, 1976, 1977, 1979; Winokur and Boesch, 1980; Winokur, McLean, and Boesch, 1986).
2. There may also be a strong correlation of the buildup with hydrogen or water content of the oxide; in fact, arguments have been made that the time-dependent buildup is associated with the release (during the hole-transport phase) and diffusion of hydrogen, or a water-related species, from the oxide bulk to the inter-

- face (Brown, 1985; Griscom, 1985; McLean, 1980; Revesz, 1977; Sah, 1976; Svensson, 1978).
3. The amount of interfacial strain, which is highly variable with processing, seems to be an important factor (EerNisse and Derbenwick, 1976; Grunthner, Grunthner, and Maserjian, 1982; Toyokawa *et al.*, 1986; Winokur, McLean, and Boesch, 1986; Zekeriya and Ma, 1984).
 4. The rate of buildup of the time-dependent N_{it} component increases with temperature; however, the final density at long times is essentially independent of temperature (McLean, 1980; Winokur *et al.*, 1977, 1979).
 5. Annealing of interface traps has not been observed at normal operating temperatures (Reed and Plummer, 1986); significant annealing occurs only for $T > 150^\circ\text{C}$.
 6. In many cases, a sublinear dependence of DN_{it} on dose ($\sim D^{2/3}$) has been observed, particularly for the delayed time-dependent component (Dozier and Brown, 1983; Naruke *et al.*, 1983; Winokur *et al.*, 1977; Winokur and Boesch, 1980).
 7. The magnitude of N_{it} buildup is generally observed to decrease with decreasing oxide thickness (Boesch *et al.*, 1978; Ma, 1975; Ma and Barker, 1974; Naruke *et al.*, 1983; Saks, Ancona, and Modolo, 1986; Viswanathan and Maserjian, 1976).
 8. The energy distributions of radiation-induced interface traps are commonly observed to be U-shaped, with a minimum near midgap and rising toward both the conduction and valence band edges (Sah, Sun, and Tzou, 1982; Winokur, McGarrity, and Boesch, 1976; Winokur *et al.*, 1977). However, the existence of intermediate structures, such as peaks, is the subject of debate (Knoll, Braunig, and Fahrner, 1982; Lenahan and Dressendorfer, 1984; Ma, 1975; Poindexter *et al.*, 1984).
 9. The interface traps seem to be amphoteric in nature, that is, they have a net negative charge (acceptor-like) when the Fermi level E_F at the surface is in the top half of the Si bandgap; they have net positive charge (donor-like) when E_F is in the bottom half of the bandgap; and they are charge neutral when E_F is near midgap (Knoll, Braunig, and Fahrner, 1982; Lenahan and Dressendorfer, 1984; Ma, Scoggan, and Leone, 1975; Poindexter *et al.*, 1984).
 10. Since the radiation-induced interface traps lie at or very near the SiO_2/Si interface, they introduce additional scattering centers for the conducting channel carriers in MOSFETs, especially when charged; these are in addition to the normal scattering from surface roughness, ionized dopants or other impurities in the surface region, and lattice vibrations (phonons).

2.3 Ionizing Radiation Dose Effects on Semiconductor Devices

The purpose of this section is to provide a brief summary [paraphrased from Rose, 1984] of the effect of ionizing radiation dose on a variety of semiconductor devices, e.g., diodes, transistors, MOS digital integrated circuits, and both linear and digital bipolar integrated circuits. In addition, a number of examples concerning the ionizing radiation dose hardness of these types of devices will be provided. The information presented here can be used as part of the semiconductor device selection criteria (e.g., technology and operating mode) for different applications (e.g., space satellite, strategic or interceptor missile, etc).

2.3.1 Effects on Diodes

2.3.1.1 Conventional Diodes

Ionizing radiation dose effects in switching and rectifying diodes appear as a change in the forward voltage V_F , leakage current I_R , and the breakdown voltage V_B . Parameter changes are not linear with cumulative dose. In general, the parameter changes are barely detectable at 10 krads(Si). At 100

krads(Si), the usual parameters of design importance, ΔV_F and ΔI_R , are less than 50 mV and 10 μ A, respectively.

2.3.1.2 Voltage-Reference Diodes

The parameter of interest voltage-reference diodes is reference (or zener) voltage V_Z . Figure 2-24 is a normalized scatter plot of change in zener voltage as a function of ionizing radiation dose. It can be seen that insignificant changes occur up to 10^2 krads(Si); between 10^2 and 10^3 krads(Si), changes of 0.1 to 1 percent are typical. The mechanism for the change is creation of inversion layers, which are dependent on doping concentration levels. Therefore, diodes that are heavily doped and have low breakdown voltages are not as sensitive to ionizing radiation dose as lightly doped devices with high breakdown voltages.

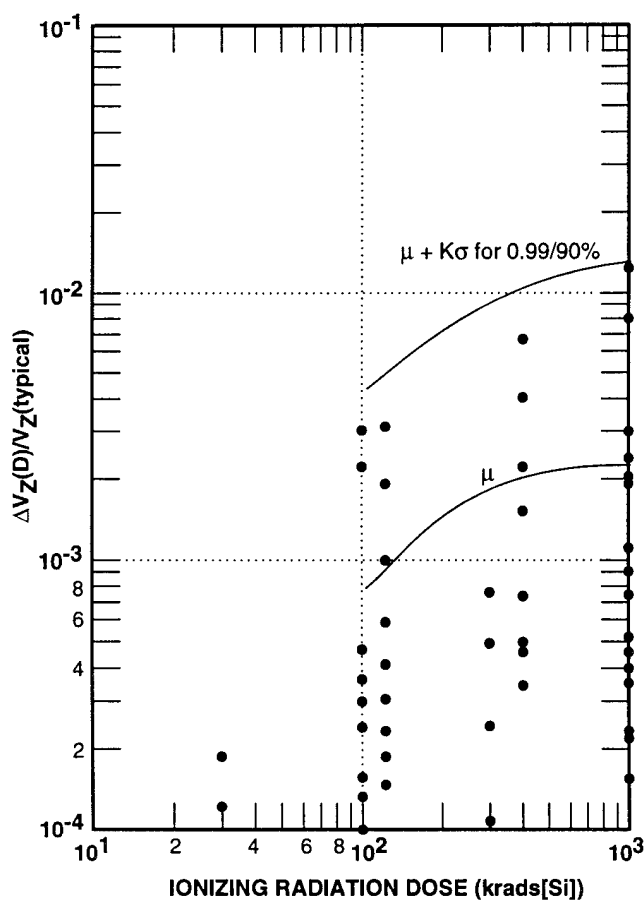


Figure 2-24. Normalized reference voltage change ΔV_Z for zener diodes at 25°C versus ionizing radiation dose [$\Delta V_Z(D)$ is the average change in V_Z for the given test sample] (Rose, 1984).

2.3.1.3 Microwave Diodes

Microwave diodes are inherently hard to ionizing radiation dose. Most device pre-irradiation parameters are unaffected at dose levels below 10^6 rads(Si) and show only small changes (a few percent) between 10^6 and 10^7 rads(Si).

2.3.2 Effects on Junction Field-Effect Transistors

The primary effect caused by ionizing radiation dose on junction field-effect transistors (JFETs) is increased leakage current between the reverse-biased gate and drain. This increased leakage current is caused by ionization-induced surface charge within the oxide. This surface charge, if sufficiently great, can invert the region. In the case of a heavily doped p-region, the oxide may saturate below a level sufficient to invert the surface. This saturation effect results in an increased reverse current, effectively shunting the bulk channel and causing pinch-off to appear less complete. The increased leakage current is similar to increased reverse leakage within pn diodes and therefore has comparable failure levels. Typical changes in increased leakage currents may be of one or more orders of magnitude between 10^6 and 10^9 rads(Si). However, even these large changes may not significantly affect circuit operation. For most applications, JFETs are inherently hard to ionizing radiation dose levels up to 10^7 rads(Si).

2.3.3 Effects on Bipolar Transistors

Bipolar transistors experience changes in their forward current gain h_{FE} , leakage currents I_{CBO} and I_{EBO} , and saturation voltage $V_{CE(SAT)}$ when exposed to ionizing radiation. The ionizing radiation dose causes leakage currents to increase, thereby degrading h_{FE} . Gain degradation is a function of collector-base bias voltage, as shown in Figure 2-25 for npn and pnp transistors. Low-current, high-gain transistors are more vulnerable to ionizing radiation effects than other transistors because surface current effects are more significant at low collector currents. The variation of h_{FE} as a function of collector current I_C and ionizing radiation dose is given for 2N2222A transistors in Figure 2-26. The error bars shown in the figure are

due to the variation of h_{FE} degradation from batch to batch of the same part. Figure 2-27 shows data for 2N2102 transistors taken from five different batches during a single day's run. In addition to h_{FE} , $V_{CE(SAT)}$ and I_{CBO} will both be affected by

ionizing radiation dose. These are generally of lesser significance, reflecting average changes of about 1 percent at 10^5 rads(Si) as shown in Figures 2-28 and 2-29.

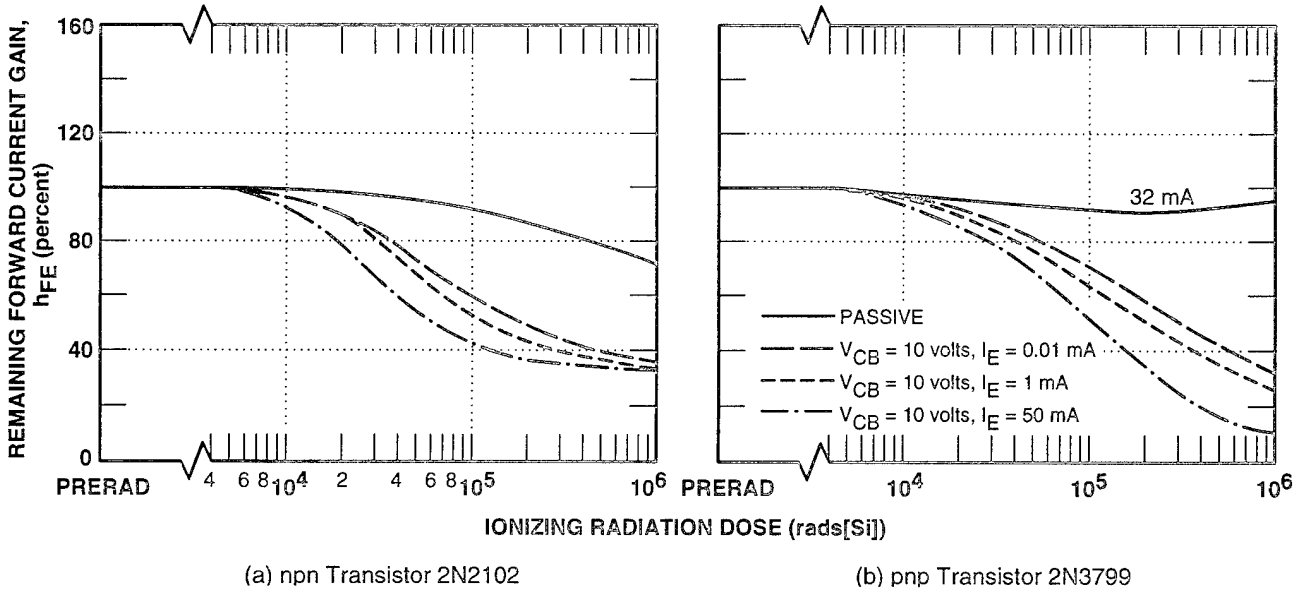


Figure 2-25. Ionizing-radiation-dose-induced h_{FE} degradation dependence on irradiation bias condition (Holmes-Siedle and Zaininger, 1968).

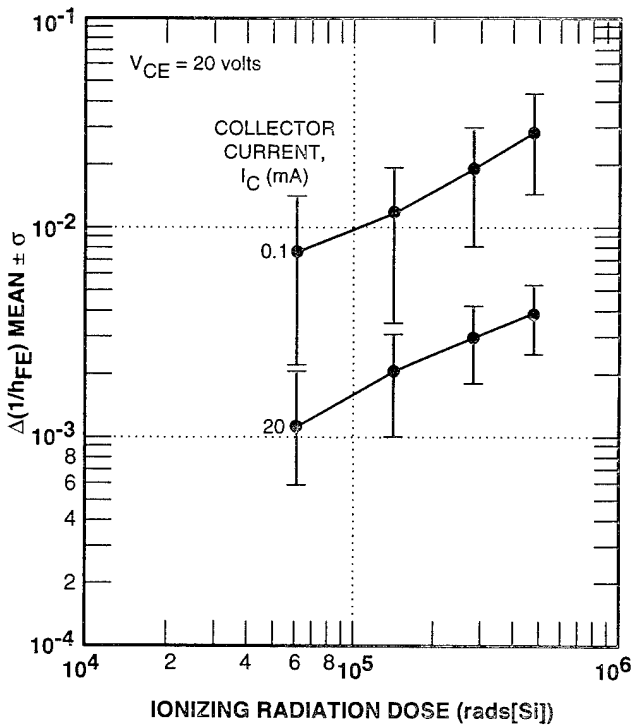


Figure 2-26. h_{FE} degradation for 2N2222 transistors (combined data of 34 devices for all tests by same manufacturer); $V_{CE} = 20$ volts (Price *et al.*, 1982).

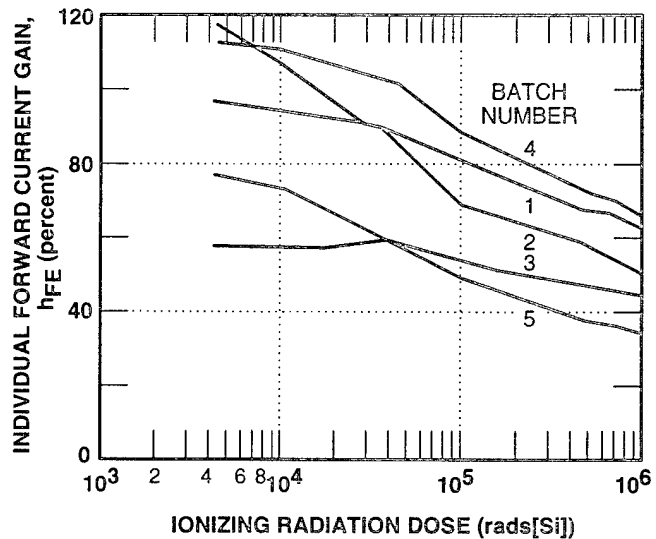


Figure 2-27. h_{FE} degradation for five identical 2N2102 transistors from same day's production (Holmes-Siedle and Zaininger, 1968).

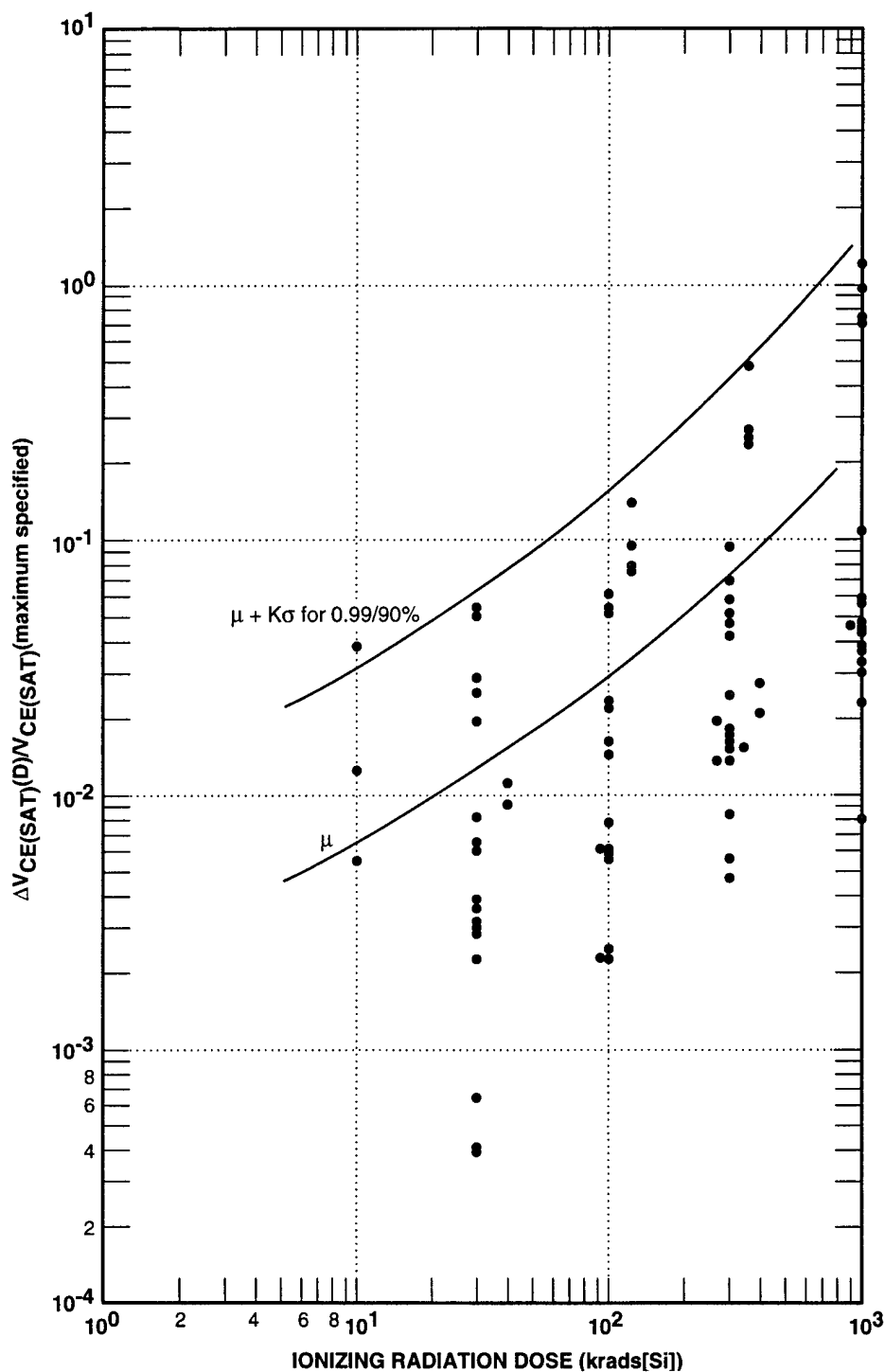


Figure 2-28. Normalized saturation voltage change $\Delta V_{CE(SAT)}$ for general-purpose transistors at 25°C versus ionizing radiation dose [$\Delta V_{CE(SAT)}(D)$ is the average change in $V_{CE(SAT)}$ for the given test sample] (Rose, 1984).

2.3.4 Effects on MOSFETs

MOS devices are generally the most sensitive electronic devices to ionizing radiation dose due to ionization-induced trapped charge in oxide and the generation of interface states, both of which cause

changes in the MOS transistors and ICs [as discussed in Section 2.2]. The effects on individual transistors are discussed here while these effects on MOS ICs are discussed in Section 2.5.

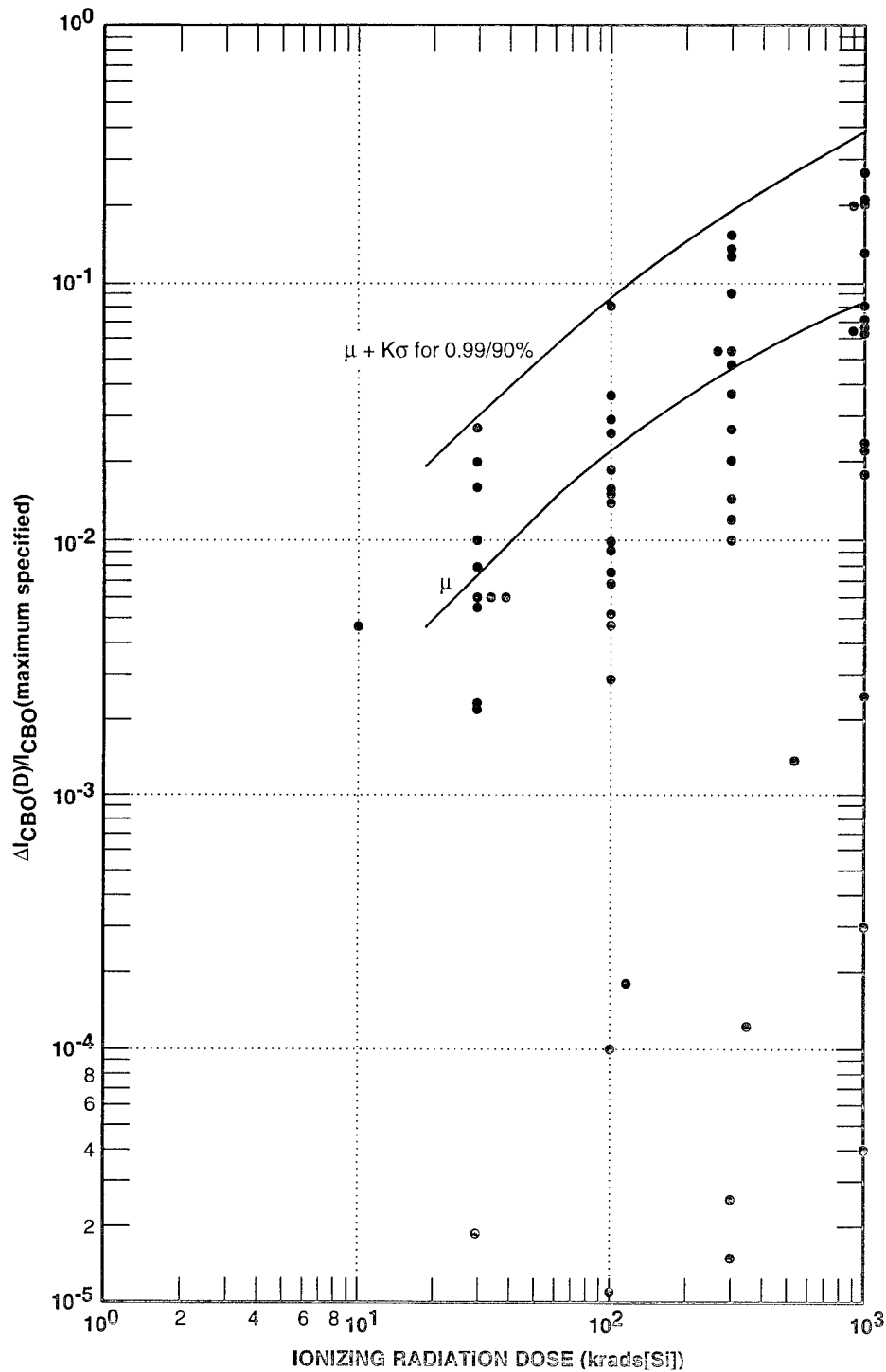


Figure 2-29. Normalized change in collector base cutoff current ΔI_{CBO} for general-purpose transistors at 25°C versus ionizing radiation dose [$\Delta I_{CBO}(D)$ is the average change in I_{CBO} for the given test sample] (Rose, 1984).

The primary effect on MOS transistors is the buildup of trapped charge in the gate oxide, which results in a threshold voltage shift. One of the current applications for MOSFETs is as a power switch for power-conditioning circuits. The ioniza-

tion-induced change in threshold voltage V_T for these types of devices varies greatly, as seen in Figure 2-30, with some devices exceeding the typical maximum gate threshold voltage near 10^4 rads(Si). Other devices showed much less degrada-

tion and were still within the manufacturer's specification beyond 10^5 rads(Si). These and similar data indicate the dependence of bias, process, and circuit design on the failure level for MOSFETs.

Proper design and part selection, however, will permit the usage of MOSFETs in circuits with ionizing radiation dose requirements up to 10^6 rads(Si).

Some MOSFET devices particularly those used for high-voltage switching applications exhibit strong rebound effects, i.e., post-irradiation biased operation can produce significant changes in the post-radiation threshold voltage. These effects can produce significant threshold shifts that are evident long after the radiation exposure is completed. Furthermore, these devices exhibit large variations in response when irradiated at different dose rates. Irradiated at different dose rates. Irradiation at low-dose rates (satellite applications) can produce large threshold voltage changes.

2.3.5 Effects on Four-Layer Devices

Ionizing radiation dose will have essentially the same effect as neutrons on four-layer devices. Ef-

fectively, the ionizing radiation dose degrades the equivalent transistor gains, which in turn require high gate trigger current I_{GT} . The observed failure threshold (50 percent increase in I_{GT}) has been in the range of 10^4 to 10^5 rads(Si), making SCRs one of the most sensitive discrete devices to ionizing radiation dose as well as to dose-rate and displacement damage effects.

2.3.6 Effects on Integrated Circuits

2.3.6.1 Bipolar Linear ICs

Bipolar linear ICs are moderately sensitive to ionizing radiation dose effects. Offset voltage V_{OS} , offset current I_{OS} , bias current I_b , and open-loop voltage gain A_{VOL} are some of the key parameters of operational amplifiers and comparators affected by ionizing radiation. The threshold for the appearance of parameter changes is about 10 krad(Si). Figure 2-31 depicts these parameter variations for a linear IC. In general, bias current changes are more pronounced than changes in other parameters. Usually, the mean ΔI_b (10 krad) is a small fraction of I_b (maximum). There are, however, isolated cases where significant changes

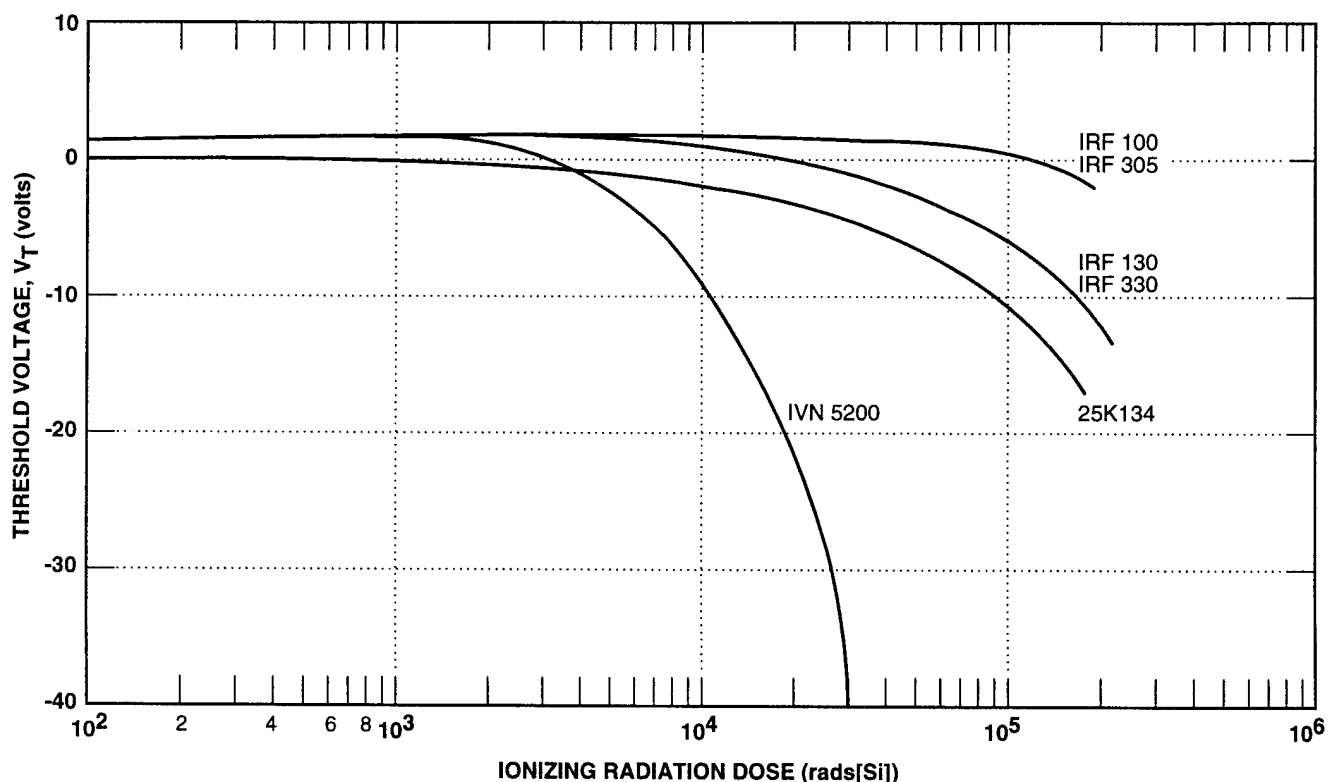


Figure 2-30. Ionizing radiation dose effects in field-effect transistors (Rose, 1984).

are observed at low doses. For example, the LM111F has a specification maximum I_b of 100 nA at 25°C and a measured mean ΔI_b of 98.6 nA at 10 krad(Si).

As with bipolar digital ICs, linear ICs built using oxide isolation exhibit significant leakage currents and failures at >10 krad(Si). Bipolar regulator ICs suffer from a loss of precision when their loop gains are degraded. Regulation changes are, however, barely detectable at 10 krad(Si). Radio Frequency (rf) bipolar linear ICs are less sensitive to ionizing radiation dose degradation; greater than 100 krad(Si) are required to produce observable effects.

2.3.6.2 Bipolar Digital ICs

Bipolar digital ICs, including all forms of transistor-transistor logic (TTL) are relatively insensitive to ionizing radiation dose effects. Most TTL ICs operate within their specification limit after 10^6 rads(Si). Bipolar devices built utilizing oxide isolation (LOCUS), such as Fairchild Advanced Schottky TTL (FAST), are susceptible to failure at levels not much greater than 10 krad(Si). The failures are a result of isolation leakage, and although process solutions are known to exist none have been incorporated by semiconductor manufacturers. However, advanced bipolar technologies like advanced low-power Schottky (ALS), current-mode logic (CML), and double-diffused have shown no appreciable degradation, even after 10^6

rad(Si). Emitter-coupled logic (ECL) circuits remain hard to levels in excess of 10^7 rads(Si). The approximate failure threshold ranges for these various technologies are shown in Figure 2-32.

2.3.6.3 MOS Digital ICs

MOS digital IC devices are most sensitive to ionizing radiation dose effects. The sensitivity is dependent on the particular MOS technology, complexity of the device, time history profile of ionizing radiation dose threat, bias, circuit performance requirements, and manufacturing process. The radiation response of MOSFETs and MOS ICs is discussed elsewhere in this chapter [see Sections 2.4 and 2.5] and will not be repeated here. However, a few comments are appropriate:

- Many commercial parts that are not explicitly designed to be radiation-hard are indeed radiation-resistant, i.e., failure levels ≥ 100 krad(SiO₂), and thus are suitable for either tactical or limited nonstrategic space applications.
- The trend to smaller feature size and increased integration density has improved the gate threshold voltage radiation response (due to thinner gate oxides) but degraded the leakage current response due to field oxide sensitivities.
- Insulating substrate technologies [e.g., silicon-on-sapphire (SOS), and silicon-on-insulator (SOI)], while demonstrating superior dose-rate and SEU response, have manifested several new ionizing radiation dose failure modes. These include side-wall leakage for mesa-type structures and back-channel leakage. Also, for planar designs, the more traditional tub-to-tub leakage (e.g., field-oxide inversion) and field-oxide (bird's beak) leakage paths still exist.

A brief comparison of various MOS integrated circuit ionizing radiation dose failure threshold ranges is shown in Figure 2-33.

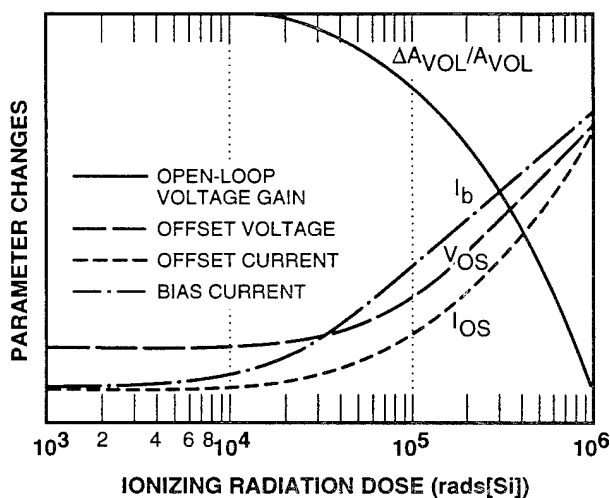


Figure 2-31. Linear IC parameter variations with ionizing radiation dose (Rose, 1984).

TECHNOLOGY	MANUFACTURER	IONIZING RADIATION DOSE (rads[Si])				
		10^4	10^5	10^6	10^7	10^8
STANDARD TTL	VARIOUS					
LOW-POWER SCHOTTKY TTL (LSTTL)	VARIOUS					
RAD-HARD LSTTL	VARIOUS, TEXAS INSTRUMENTS, HARRIS					
FAIRCHILD ADVANCED STTL	FAIRCHILD, MOTOROLA, SIGNETIC					
ADVANCED SCHOTTKY LOGIC (ASL)	TEXAS INSTRUMENTS					
INTEGRATED SCHOTTKY LOGIC (ISL)	RAYTHEON					
EMITTER-COUPLED LOGIC (ECL)	VARIOUS					

Figure 2-32. Ionizing radiation dose thresholds for digital bipolar integrated circuits (Rose, 1984).

TECHNOLOGY	MANUFACTURER	IONIZING RADIATION DOSE (rads[Si])				
		10^2	10^3	10^4	10^5	10^6
BULK CMOS	VARIOUS					
RAD-HARD CMOS	SANDIA, HARRIS, IBM, HONEYWELL					
HC MOS	NATIONAL, MOTOROLA, OTHERS					
CMOS/SOS	HARRIS					
RAD-HARD CMOS/SOS	HARRIS, MARCONI					
RAD-HARD CMOS/SOI	UNITED TECHNOLOGIES, HONEYWELL, TEXAS INSTRUMENTS					
HMOS I	INTEL					
HMOS II	INTEL					
HMOS III	INTEL					
DMOS	NEC					
MNOS HARDENED	SANDIA, NCR, SPERRY					
MNOS COMMERCIAL						

Figure 2-33. Ionizing radiation dose thresholds for MOS technologies (Rose, 1984).

2.4 Metal-Oxide-Semiconductor Field-Effect Transistor Ionizing Radiation Dose Response

In Subsection 2.1.2, the basic mechanisms of ionizing radiation effects were discussed. Building on the information provided there, this section addresses ionizing radiation effects on MOSFETs. Basically, the effects of ionizing radiation on MOSFETs result in:

- Threshold voltage (V_T) shifts
- Induced leakage currents
- Reductions in mobility.

Each of the effects is discussed below. In addition, second-order effects (i.e., hot-carrier degradation and surface recombination velocity) are discussed.

2.4.1 Threshold Voltage Shifts

As previously stated, the radiation-induced response is a summation of a variety of basic processes: initial hole yield, hole transport, deep hole trapping, short- and long-term annealing, and interface trap buildup. Characteristic time regimes are associated with each of these processes and each process is also a function of bias, temperature, oxide thickness, etc. Figure 2-34 depicts the time-dependent, radiation-induced threshold voltage response for an n-channel MOSFET, with the various characteristic time regimes (at room temperature) explicitly noted, and illustrates the various long-term recovery behaviors (recovery without ΔN_{it} , with prompt ΔN_{it} , and with time-dependent ΔN_{it} buildup). This overall effect is summarized by

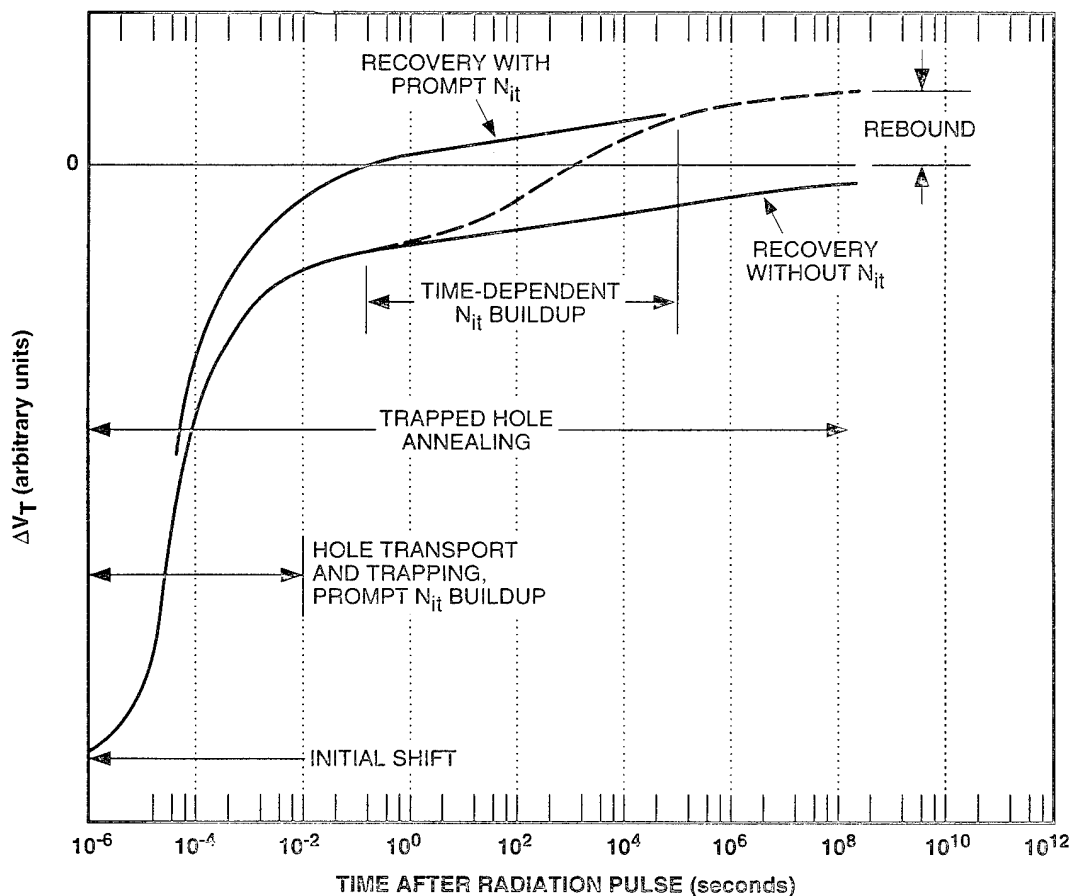


Figure 2-34. Schematic time-dependent threshold voltage recovery of an n-channel MOSFET following pulsed irradiation, indicating the room-temperature time regimes associated with the various basic physical processes and possible long-term responses (McLean and Oldham, 1987).

Equation 2.9. The influence of intrinsic (e.g., oxide morphology, etc.) factors in conjunction with extrinsic effects (e.g., bias, temperature, etc.) greatly complicates issues dealing with radiation testing, hardness assurance, and response prediction of circuits in a radiation environment. The result of the trapped positive charge (holes) for the n-channel MOSFET is to lower the threshold voltage, i.e., it drives the device into depletion, as shown in Figure 2-35(a), which depicted by a shift to the left for the threshold voltage and an increase in drain current I_D . In this case, a shift to the left indicates that a lower gate voltage is required to turn on the MOSFET. However, as interface trap density begins to increase the negative charge associated with this effect for n-channel devices, subtracts from the positive charge (hole traps) and the threshold voltage begins to turn around:

$$\Delta V_T = \Delta V_{ot} - \Delta V_{it} \quad (2.9)$$

The overall effect for the p-channel MOSFET is somewhat different. For this device, the trapped positive charge increases the threshold voltage, i.e., it drives the device into accumulation, as shown in Figure 2-35(b), and is also depicted by a shift to the left for the threshold voltage. However, in this situation, a shift to the left results in lower drain current since this change in V_T implies that a

higher (more negative) gate voltage is required to turn on the MOSFET. As the interface state density increases, the threshold voltage continues to increase. This occurs due to the amphoteric nature of interface traps or states, where, for a p-channel device, these traps have a positive charge. Thus, the p-channel device final threshold voltage will be the result of the sum of the trapped holes and interface states. This result differs from that for the n-channel device, where the final threshold voltage is the result of the difference between the trapped holes (positive charge) and the interface state density (negative charge).

2.4.1.1 Rebound Effects (Super-Recovery)

A more detailed discussion of the rebound (super-recovery) effect is presented here. Deeply trapped holes (ΔN_{ot}) anneal out over very long periods of time. Interface traps (ΔN_{it}) have not been observed to anneal out at normal operating temperatures. Furthermore, ΔN_{it} may continue to build up over time. Since, for an n-channel device under positive bias, the interface traps contribute net negative charge and therefore a positive contribution (ΔV_{it}) to the threshold voltage, these factors taken together may give rise to the phenomenon called super-recovery (Johnston, 1984), or rebound (Schwank *et al.*, 1984). Namely, at the end of an

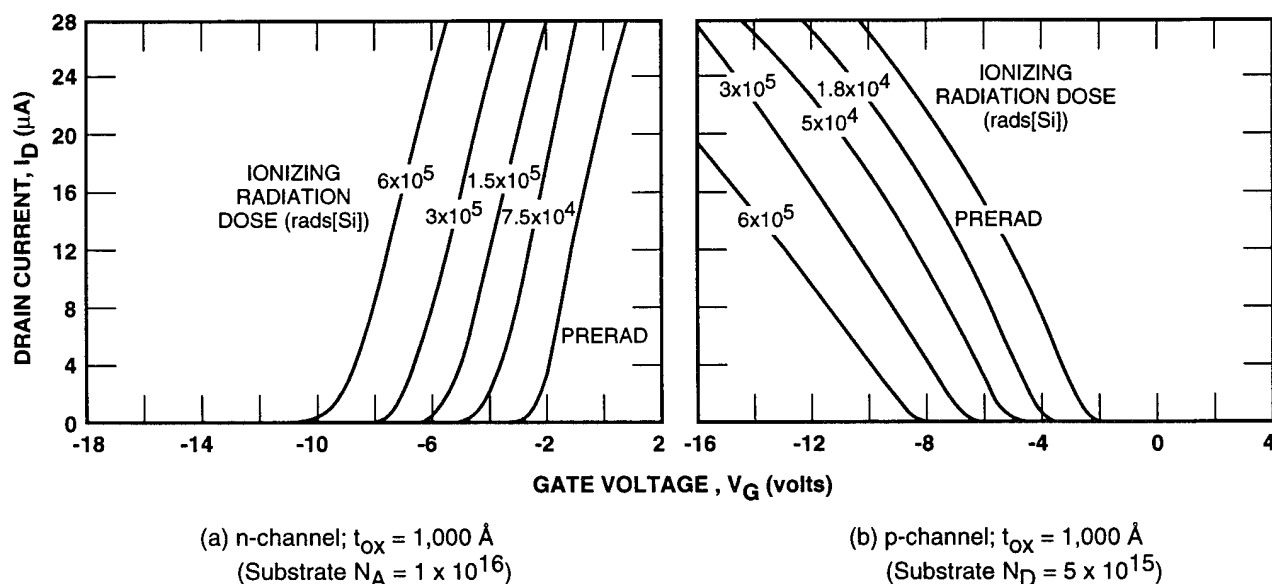


Figure 2-35. Radiation-induced threshold shift in enhancement MOSFET drain current versus gate voltage characteristics (King, 1979).

irradiation, the threshold voltage for an n-channel MOSFET is generally shifted negatively, since the (negative) voltage contribution ΔV_{ot} from the trapped holes usually dominates ΔV_{it} , at least for doses up to about 1 Mrad. However, as annealing of the trapped holes occurs and/or further buildup of the interface trapped charge occurs, the threshold voltage may actually anneal back to and past its initial pre-irradiation value; i.e., ΔV_T may go positive at some late time after cessation of the radiation. If the positive voltage excursion is sufficiently large, circuit failure may result from this effect. Super-recovery is clearly demonstrated by the data shown in Figure 2-36. Here, the threshold voltage of a polysilicon-gate n-channel MOSFET, as well as the separate components ΔV_{it} and ΔV_{ot} are plotted against time after exposure to 1 Mrad ^{60}Co irradiation that is completed in 1 hour. A gate bias of +10 volts was maintained during both irradiation and the anneal time. Data are shown for two temperatures, for 25°C and for 125°C (which accelerates the rate of hole annealing). At neither temperature is any annealing of ΔV_{it} observed, but

rather some slight increase in ΔV_{it} after cessation of the irradiation is discernible. The important point, of course, is that V_T , which is initially shifted negatively by about 1 volt at the end of the irradiation, returns in the positive direction far past its pre-irradiation value. In fact, after 100 hours of annealing at 125°C, ΔV_{ot} is completely annealed, leaving a final positive V_T shift of +2.5 volts, due entirely to interface trapped charge (most of which was already present at the end of irradiation).

Some interesting possibilities are associated with this effect. For example, a device may initially be in failure at the end of an irradiation because of a sufficiently large negative voltage shift; then, as the trapped holes anneal, the device may begin operating normally at some time and continue operating until the device fails again from too great a positive threshold voltage shift. Some hardening schemes in the past have attempted to rely on the compensation of trapped positive (hole) charge by net negative interface trapped charge. However, this type of hardening fix is risky at best,

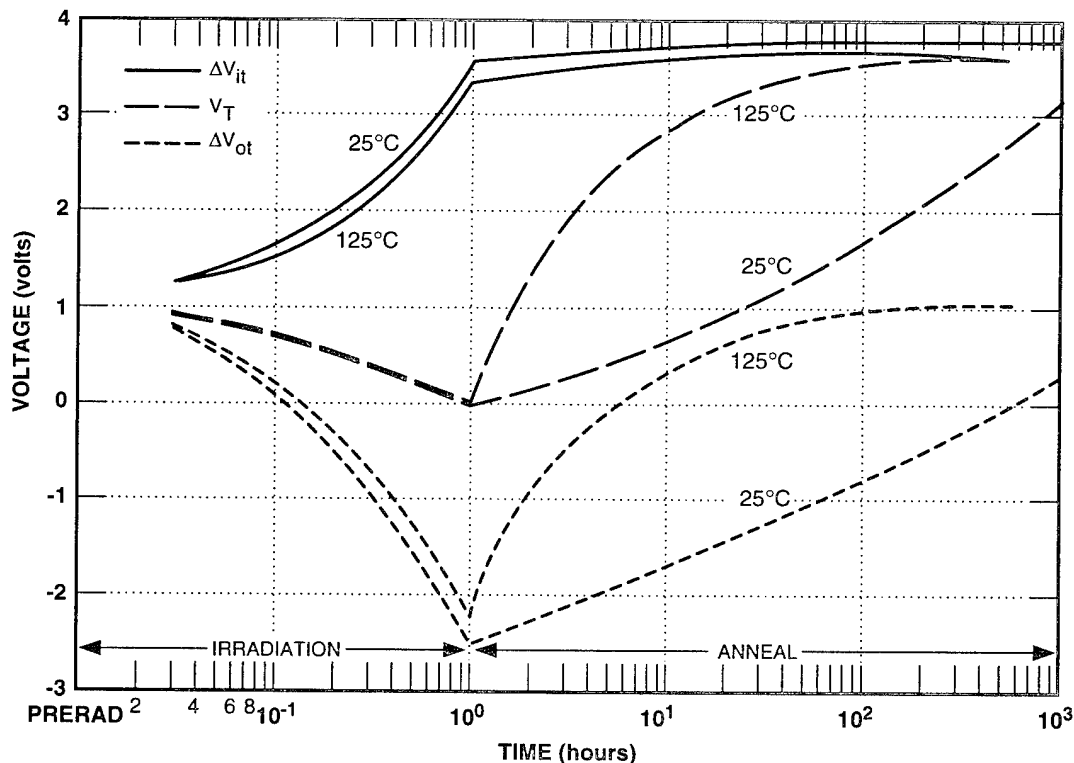


Figure 2-36. Threshold voltage shift of n-channel MOS transistor during 1 Mrad ^{60}Co irradiation and subsequent anneal; V_T separated into shifts due to interface trapped charge (V_{it}) and oxide trapped charge (V_{ot}) (Schwank *et al.*, 1984).

because the utmost control must be maintained over the oxide processing to avoid excessive radiation-induced N_{it} and consequent failure by rebound at long times. Such careful control of the processing is usually not possible in the long run for production lines. The optimum hardening approach is to minimize both ΔN_{ot} and ΔN_{it} (Winokur *et al.*, 1985). [A discussion of the implications of the behavior on testing considerations is provided in Chapter 6.]

2.4.1.2 Apparent Dose-Rate Effects

A related problem area is that of an apparent dose-rate effect (McLean and Oldham, 1987) on device response; i.e., measurements of device response (e.g., ΔV_T) at the end of irradiation to a fixed total dose, but delivered at different dose rates, usually will show different results. This is clearly a result of the complex time history of the response in which, for example, different amounts of trapped-hole annealing will occur during irradiation for different exposure times (to the same dose). To deal with this problem, the techniques of linear response theory have been used in the past. This type of analysis is valid as long as the system response is linear in dose. If the impulse response function $\Delta V_R(t)$ is known (say, the threshold voltage response to an infinitesimally short irradiation pulse), then the general response to an arbitrary irradiation described by the dose-rate function $\dot{\gamma}(t)$ may be obtained through the convolution integral:

$$\Delta V_T = \int_0^t dt' \dot{\gamma}(t') \Delta V_R(t-t') \quad (2.10)$$

A simple example for which this technique has been applied (Derbenwick and Sanders, 1977; Winokur, 1982; Winokur, Kerris, and Harper, 1983) is that for linear (log-time), trapped-hole annealing. In general, this approach has limited quantitative utility because of its nonlinear response, as discussed below.

2.4.1.3 Trapped-Hole Saturation Effects

The effect of trapped-hole saturation on radiation-induced threshold voltage shifts is discussed in this section. Subsection 2.4.1.2 [above] noted that apparent dose-rate effects, such as varying

amounts of trapped-hole annealing during irradiation exposure, can sometimes be handled with the convolution integrals of linear response theory. This approach is valid as long as the system response is linear in dose. Unfortunately, this is not always the case for situations of practical interest. For example, the number of trapped holes ΔN_{ot} tends to saturate for moderate to large dose rates at doses in the range from 1 to 10 Mrads(SiO_2) (Boesch and McGarrity, 1976; Boesch *et al.*, 1986; Churchill, Collins, and Holmstrom, 1974; Collins, Holmstrom, and Churchill, 1979; Hughes and Seager, 1983). This saturation may be due to one or more factors, including hard saturation due to trap filling, space-charge effects, or a balance between hole trapping and hole removal through tunnel anneal or recombination with radiation-induced electrons. An example of such an effect is illustrated by Figure 2-37, in which the threshold voltages for n- and p-channel MOSFETs are shown plotted versus ionizing radiation dose. The threshold voltage for the n-channel device first shifts negatively as the positive charge buildup due to trapped holes dominates the response. However, at doses >1 Mrad, a turnaround is observed, with V_T shifting back in the positive direction at increasing

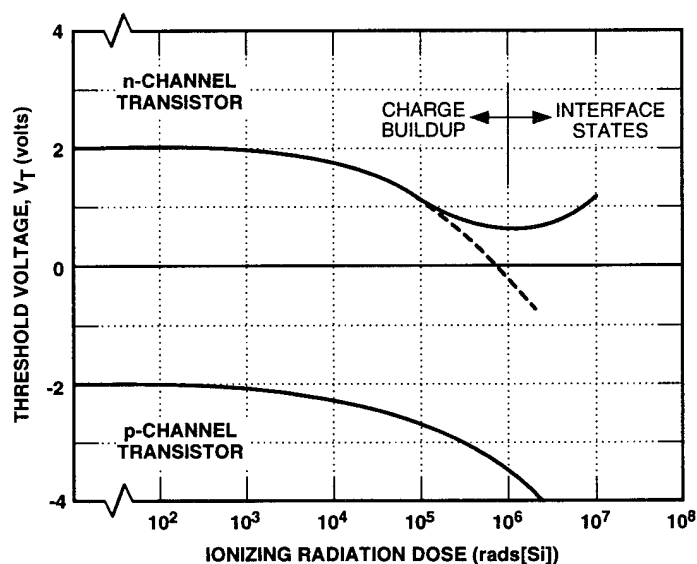


Figure 2-37. Threshold voltage versus ionizing radiation dose for irradiated n- and p-channel MOSFETs, illustrating the effect of hole-trapping saturation and continued interface trap buildup in n-channel devices (McLean and Oldham, 1987).

dose levels. This turnaround behavior is due to saturation of the trapped-hole density, while at the same time the interface trapped charge (negative for n-channel) continues to increase. For the p-channel device under negative gate bias, the interface states also contribute net positive charge, and there is a continued negative shift with dose in its threshold voltage.

2.4.2 Ionizing Radiation Dose Classification Scheme

Since a variety of MOSFET responses are possible due to the relative density of holes to interface states, a scheme to categorize the possible transistor responses has been developed by Boesch (1986). The scheme, depicted in Table 2-4, classifies oxide response as being one of four qualitative types, based, first, on low ΔN_{ot}^0 or high ΔN_{ot}^0 and, secondly, on whether $\Delta N_{it} \ll \Delta N_{ot}^0$ or ΔN_{it} is $\approx \Delta N_{ot}^0$. Here, ΔN_{ot}^0 is the oxide trapped-hole density present at the earliest measurement times of interest, before appreciable trapped-hole annealing occurs. Note that categories for $\Delta N_{it} \gg \Delta N_{ot}^0$ are not included since this case is not observed in practice. The table contains the general qualitative features of the response in each case. In practice,

Table 2-4. Categorization matrix of possible ionizing radiation dose response types for MOS devices, indicating qualitative features of response for each type (Boesch, 1986).

$\Delta N_{it} \ll \Delta N_{ot}^0$	$\Delta N_{it} \approx \Delta N_{ot}^0$
Low ΔN_{ot}^0	
Category 1	Category 3
No super-recovery Moderate log(t) recovery Negligible mobility degradation Hard	Some super-recovery Complex time history Some mobility degradation Hard
High ΔN_{ot}^0	
Category 2	Category 4
No super-recovery Weak log(t) recovery Possible mobility degradation Soft	Large super-recovery Complex time history Severe mobility degradation Soft

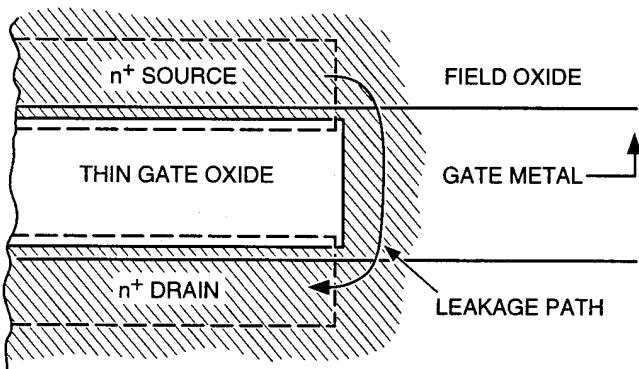
some oxides will fall into the grey zones between the categories, a problem inherent in any classification scheme.

2.4.3 Ionizing Radiation-Dose-Induced Leakage Currents

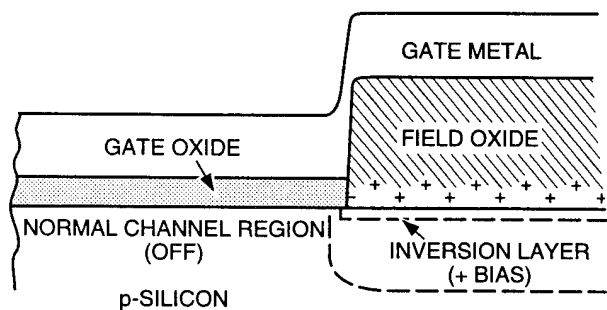
The discussion of the physical mechanisms underlying the radiation response of MOS devices has focused on the gate-oxide layer and on the consequences of trapped-charge buildup in these layers, primarily that of induced shifts in threshold voltages. However, identical physical processes leading to charge buildup also occur in the thicker oxides used in IC technologies. Instead of voltage shifts, the effects of charge buildup in these oxides in circuit operation involve the generation of undesirable parasitic current leakage paths. Specifically, charge buildup in field-, passivation-, or isolation-oxide regions can induce the formation of inversion channels in the surface regions of adjoining semiconductor regions, which, in the presence of any potential gradients (e.g., fringing fields), will result in parasitic current leakage paths. Leakage paths can be important failure modes, not only in bulk MOS technologies, but also in SOS and SOI structures, and even in bipolar technologies as well. Figure 2-38 is a schematic showing a possible induced leakage path in an MOS device structure. Shown are top [Figure 2-38(a)] and cross-section [Figure 2-38(b)] views of the device, indicating the various regions of the device. In particular, the field-oxide region covers the Si substrate outside the gate-oxide and normal source-drain channel regions. If sufficient radiation-induced charge buildup occurs in the field-oxide region, especially near the Si substrate, then an inversion layer can be formed in the substrate, as indicated in Figure 2-38(b), even with the normal channel turned off. This induced channel region under the field oxide then offers a low-resistivity current leakage path between the source and drain around the edge of the gate-oxide (normal channel) region, as shown in Figure 2-38(a). Note that the charge buildup in the field oxide near the substrate interface proceeds in exactly the same manner as in the gate oxide; namely, in response to positive voltages applied to the gate contact lines (or other

metal strip lines) over the field oxide, which drive the radiation-generated holes down toward the field-oxide/Si interface [Figure 2-38(b)]. Because the field-oxide layers are much thicker than the gate-oxide layers, the field magnitudes are much lower ($\sim 10^5$ V/cm, rather than 10^6 V/cm) in the field-oxide regions; however, the basic processes leading to the buildup are the same. Furthermore, the charge-generation volumes are considerably larger.

The schematic diagrams shown in Figure 2-38 do not accurately reflect the MOS structures of present-day technology, but the basic principle of the induced leakage current is nevertheless valid. Figure 2-39 shows a cross section of a more modern recessed field-oxide MOS structure. The leakage paths between source and drain in these structures are thought to be in the Si substrate under the so-called "bird's beak" region of the recessed field oxide, which is immediately adjacent to the gate-oxide channel region.



(a) Top View: Radiation-Induced Current Leakage Path due to Positive Charge Buildup



(b) Cross Section: Field-Oxide/Substrate Interface
Figure 2-38. Schematic of MOS device structure (McLean and Oldham, 1987).

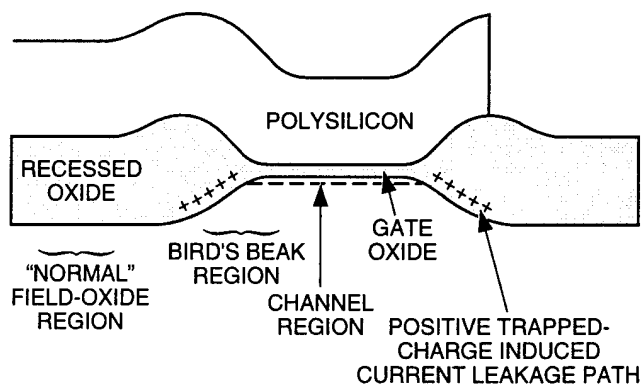


Figure 2-39. Modern, recessed field-oxide MOS structure indicating charge buildup and induced current leakage paths in the bird's beak regions of the device (McLean and Oldham, 1987).

Typically, the induced leakage currents under field oxides are studied with the aid of special test field-oxide transistors, in which the field-oxide material is used as a gate oxide in a normal MOS transistor configuration. Some post-irradiation subthreshold leakage current measurements are shown in Figure 2-40 for a device with a channel length of $1.0 \mu\text{m}$ and a channel width of $50 \mu\text{m}$. Results are shown after each of a series of 10-krad(SiO_2) LINAC pulses. Increases in leakage currents by at least several orders of magnitude are obtained. As

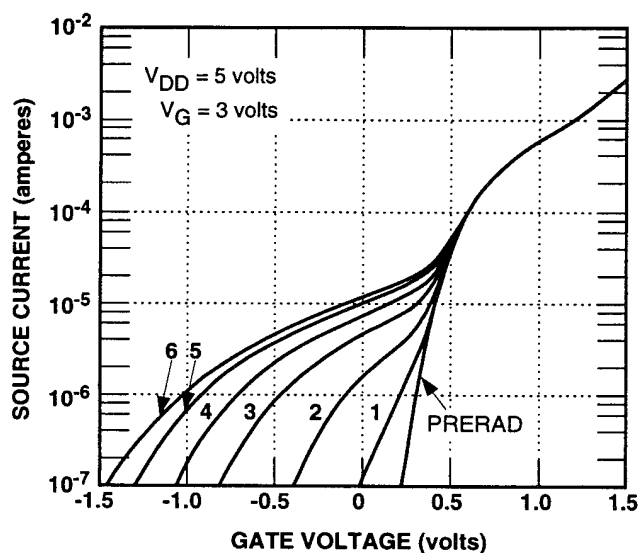


Figure 2-40. Radiation-induced increase in subthreshold leakage currents in n-channel field-oxide transistor test structure subjected to a series of 10-krad(SiO_2) pulses; $V_{DD} = 5$ volts (Boesch, n.d.).

channel length is reduced, the fringing fields in the field region between source and drain in an actual device configuration increase, which results in increased leakage currents.

As shown in Figure 2-38, the ionizing radiation dose hardness of the MOSFET is limited by the n-transistor leakage due to the positive charge accumulation in the field oxide. A method to mitigate this radiation-induced leakage path is shown in Figure 2-41, where boron has been implanted under the bird's beak region to prevent inversion; i.e., p-type material becomes n-type due to positive charge accumulation, and the source-to-drain leakage path is cut off. The use of a boron (p-type) implant is used in a variety of ways to suppress radiation-induced leakage.

Finally, insulating substrate technologies such as SOS and SOI suffer from so-called radiation-induced back-channel leakage. Figure 2-42 shows a simple schematic of an SOS structure [it could well be an SOI structure], indicating radiation-induced positive charge buildup in the sapphire substrate immediately under the active p-Si layer. The normal device channel occurs in the p-Si region next to the gate-oxide region. However, because of the positive charging of the sapphire substrate, an inversion layer can be induced on the back side of the p-Si region, resulting in back-channel leakage between source and drain. Figure 2-43 depicts the three components of an I-V curve for a mesa-type MOSFET structure used for SOS and many SOI designs. The normal I-V response of the

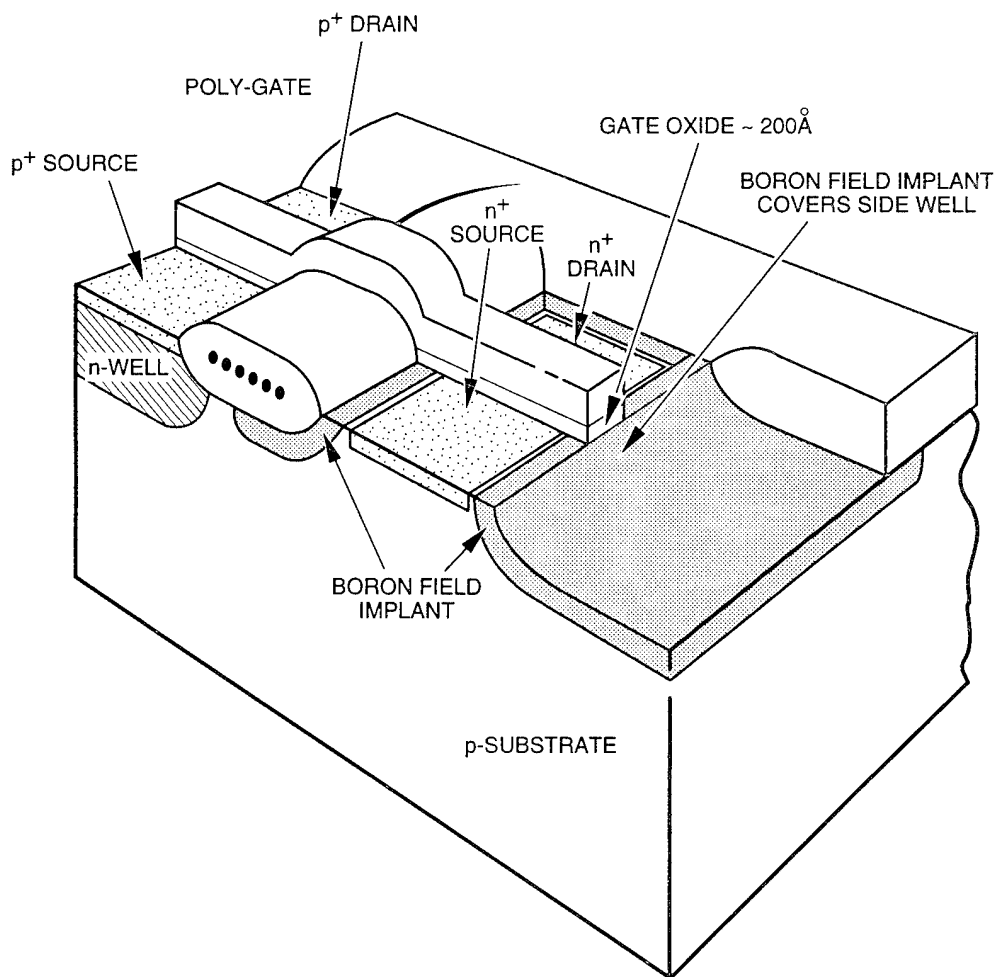


Figure 2-41. Cross section of hardened transistor demonstrating radiation-induced leakage path mitigation via boron implantation.

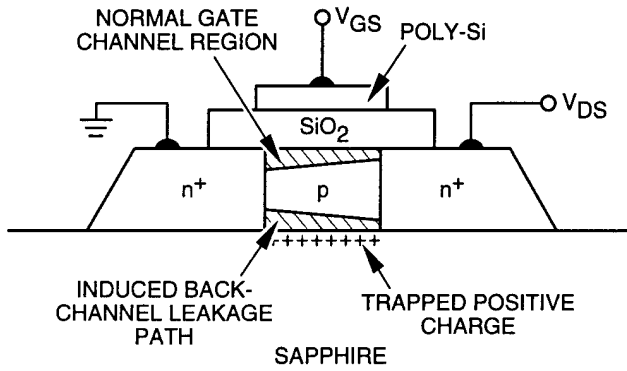


Figure 2-42. Schematic diagram illustrating back-channel current leakage in silicon-on-sapphire MOS transistor (McLean and Oldham, 1987).

MOSFETs is shown by the top transistor curve on the figure. [The effects of radiation on this component of the I-V response were discussed in Subsection 2.4.1.] However, two other radiation-induced

leakage paths and their effect on the I-V response are also shown in Figure 2-43. The back-channel leakage component has been discussed previously and is shown explicitly here. This component does not, in general, change the overall shape of the I-V response curve. However, the “floor” of the response is translated upward, i.e., the minimum value of leakage current will be higher after irradiation. The primary difference between the insulating substrate and bulk MOSFET configurations is the leakage current path identified as the side-wall transistor. This path is extremely complex and can be delineated into top, intermediate, and bottom or lower-edge side wall. This delineation is important since somewhat different radiation-hardening methods must be employed to mitigate each of these components. The most difficult of these three leakage paths to resolve has been the bottom or lower-edge side-wall component, which results from an interaction between the back channel and

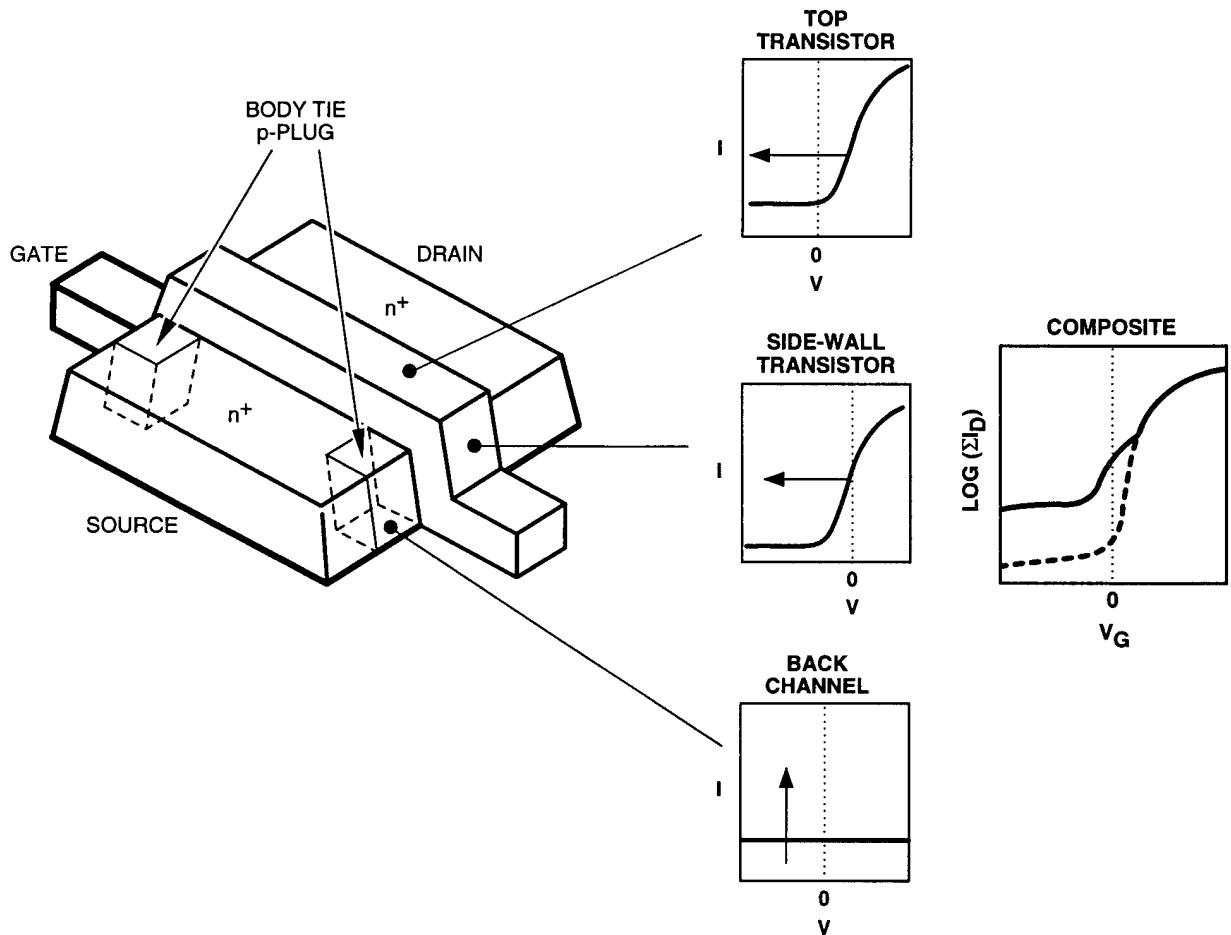


Figure 2-43. I-V curve components for an SOI transistor.

the lower edge, i.e., charge sharing (Schrankler *et al.*, 1985). Hence, charge accumulation at the back channel will impact the hardness of the lower-edge parasitic transistor.

Also, the ability to “dope” the edge (with boron for example) to prevent inversion can be compromised by material defects along the edge-substrate boundary that are caused by normal semiconductor processing, e.g., mesa formation by reactive ion etching. One method successfully employed for SOI MOSFETs to eliminate bottom side-wall leakage is to provide source-to-body ties on either side of the source [see Figure 2-43]. This is accomplished by use of a boron p-plug that contacts the buried layer. These ties are also required to eliminate floating-body effects (kinks) in SOI MOSFETs and improve transient upset hardness. It should be noted that this body-tie-to-source configuration is not employed in SOS technology. These effects are discussed in Chapter 3. In addition, the use of body ties is limited to MOSFETs, where the source and drain regions are defined. Thus, for pass-gate MOSFETs, which are bidirectional in that a signal can be transmitted from either end, source-to-body ties [shown in Figure 2-43] cannot be used and other radiation-hardening solutions must be employed. It is beyond the scope of this chapter to provide a complete discourse on the various methods used to obtain ionizing radiation dose hardness, but abbreviated information is provided here to indicate the scope and magnitude of this problem.

2.4.4 Gate-Oxide Radiation-Hardening Methods

Traditionally, gate-oxide radiation hardening, manifested as a reduction in the radiation-induced threshold voltage shift, is obtained by various processing methods, which include:

- Modifications to the gate-oxide process, such as controlling the amount of hydrogen in the ambient atmosphere, processing at temperatures below 900°C, use of specific chemical contaminants to provide recombination centers, and strict controls on process cleanliness

- Limiting post-gate process temperatures and eliminating other steps that could damage the gate oxide, e.g., post-gate fabrication channel implantation.

In addition, the current trend toward thinner gate oxides has also aided the hardening of gate oxides. Moreover, as gate-oxide thickness t_{ox} approaches the range of 150Å or less, it is anticipated that the primary concern in this area will be gate-oxide integrity and long-term reliability instead of radiation hardness. The following discussion expands on the effects of scaling on the radiation-induced response of gate oxides. Several benefits are gained when the gate-oxide layer is thinned. First, the initial shifts (ΔV_T) are reduced according to t_{ox}^2 and the long-term hole trapping N_{ot} scales accordingly in the linear regime. Second, the short-term recovery time (hole transit time) decreases as $\sim t_{ox}^4$. Third, the recovery time is further decreased if the gate potential is held constant as the gate-oxide thickness is reduced, resulting in a larger oxide field ($E_{ox} \sim V_G/t_{ox}$). The combined effect of all three factors is dramatically illustrated by the flatband voltage recovery data shown in Figure 2-44 for three thicknesses of as-grown oxide (37.6, 56.6, and 96.3 nm) exposed at 220°K to pulsed LINAC irradiation under constant 10-volt applied gate bias. The vertical slash marks indicate the 75-

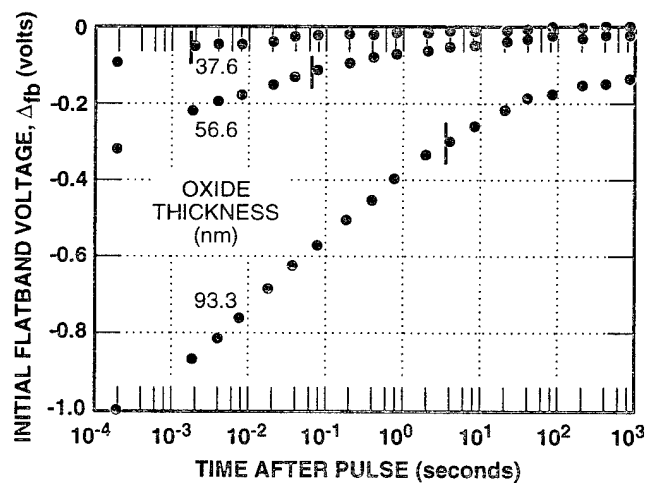


Figure 2-44. Flatband voltage recovery data at 220°K for three as-grown oxide MOS capacitor thicknesses under constant 10-volt applied gate bias [vertical bars indicate 75 percent recovery point] (Boesch *et al.*, 1978).

percent recovery point in each case. (These data are not normalized, so that the t_{ox}^2 reduction in the initial flatband voltage is also included). Under these conditions, thinning the oxide by a factor of ~ 2.5 leads to more than an order-of-magnitude reduction in the shifts for the entire time regime of the measurements.

Considering the effect on long-term deep hole trapping, first of all, ΔV_{ot} obviously scales in the same manner ($\sim t_{ox}^2$) as the initial shift. Next, if gate bias is constant, then the fraction of hole trapping decreases as $E_{ox}^{-1/2}$ for fields above 1 MV/cm; furthermore, the long-term annealing rate is somewhat enhanced with increasing field. But consider the scaling of t_{ox} down to and below 10 nm. For temperatures below $\sim 150^\circ\text{C}$, the tunneling of electrons from the Si substrate into the SiO_2 (where they recombine with the trapped holes) seems to be the process responsible for the long-term annealing of the oxide positive trapped charge. Referring to Figure 2-45, the time-dependent tunneling distance $X_m(t)$ associated with the tunnel annealing process lies in the range from 2 to 4 nm for practical times of interest — say from 10^{-3} to 10^1 seconds. Hence, for oxides with $t_{ox} < 10$ nm, enhanced hole removal can be expected to occur by electrons tunneling into the oxide from the gate electrode as well. In fact, the tunneling parameters would be roughly the same for polysilicon-gate material as for the Si substrate. This possibility of enhanced

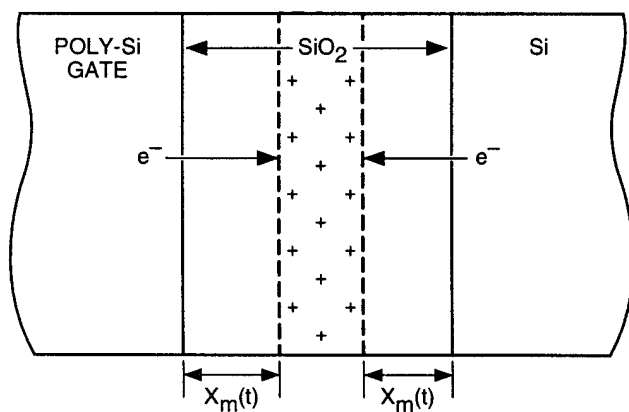


Figure 2-45. Model schematic of trapped hole removal in thin gate-oxide MOS structures by electron tunneling from both Si substrate and poly-Si gate (Benedetto and Boesch, 1986).

recovery by trapped hole recombination with tunneling electrons from both electrodes is indicated schematically in Figure 2-45.

It is quite clear from this discussion that very significant gains can be made in the radiation performance of MOSFET devices by thinning the gate-oxide layers. Unfortunately, as circuit integration density increases the gains realized in gate oxide radiation response must be tempered against increased issues with isolation density. This will require the development of new processing and design technology to mitigate these radiation induced failure modes, e.g., source-to-drain leakage along side walls, back channels, etc.

2.4.5 Ionizing Radiation Dose Effects on MOSFET Mobility

In general, effective MOSFET channel mobility tends to decrease with increasing radiation dose,

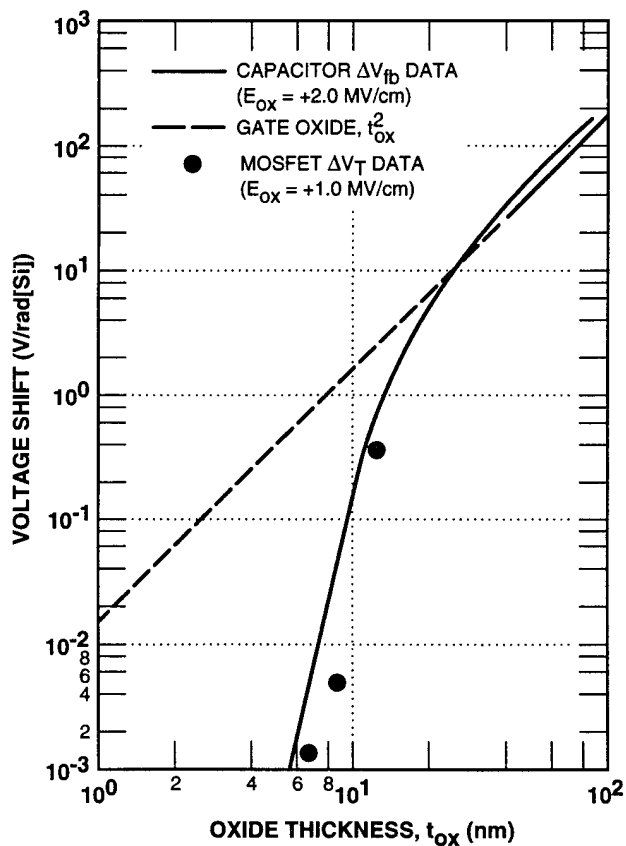


Figure 2-46. Threshold and flatband voltage shifts per Mrad(SiO_2) at 80°K (Boesch and McGarrity, 1976; Benedetto *et al.*, 1985; Saks, Anaconda, and Modolo, 1984).

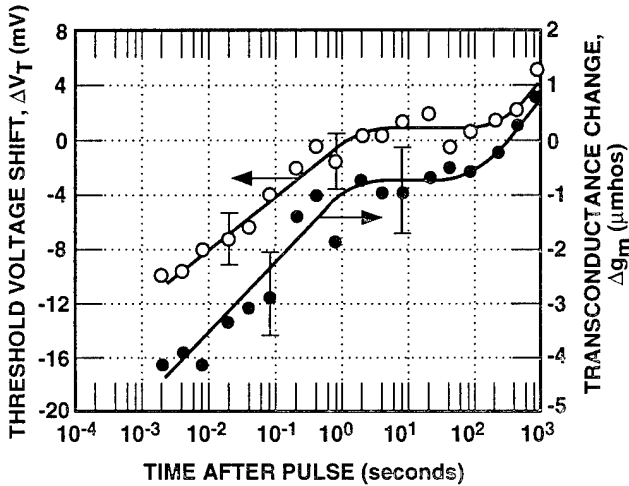


Figure 2-47. Recovery of threshold voltage shift and transconductance change following pulsed e-beam irradiation at 77°K for a MOSFET with a 5.3-nm gate oxide (Benedetto *et al.*, 1985).

which causes a decrease in current drive capability. Initial work in this area suggested that reductions in mobility were due to increased lattice and Coulomb scattering by charged interface traps and that the average surface mobility was proportional to $1/N_{it}$. Following the earlier work of Sun and

Plummer (1980), Galloway, Gaitan, and Russell (1984), and Galloway, Wilson, and Witte (1985), it was shown by Sexton and Schwank (1985) that mobility degradation can be fitted (over a wide range of experimental conditions) by the empirical relationship:

$$\mu(N_{it}) = \left[\frac{\mu_o}{1 + \alpha(\Delta N_{it})} \right], \quad (2.11)$$

where μ_o is the pre-irradiation value and $\alpha = (8 \pm 2) \times 10^{-13} \text{ cm}^2$. Mobility degradation, measured following irradiations of both n- and p-channel transistors under all bias conditions, is plotted in Figure 2-48. From first principles, radiation-induced decreases in mobility lead to reductions in subthreshold slope, transconductance, transistor drive, circuit speed, etc. The effect of a reduction in mobility, as previously stated, is to reduce the current drive capability (for a given $V_G - V_T$) of a transistor. This can be seen from:

$$I_D = \frac{Wk'}{L_{eff}} [2(V_G - V_T)V_D - V_D^2], \quad (2.12)$$

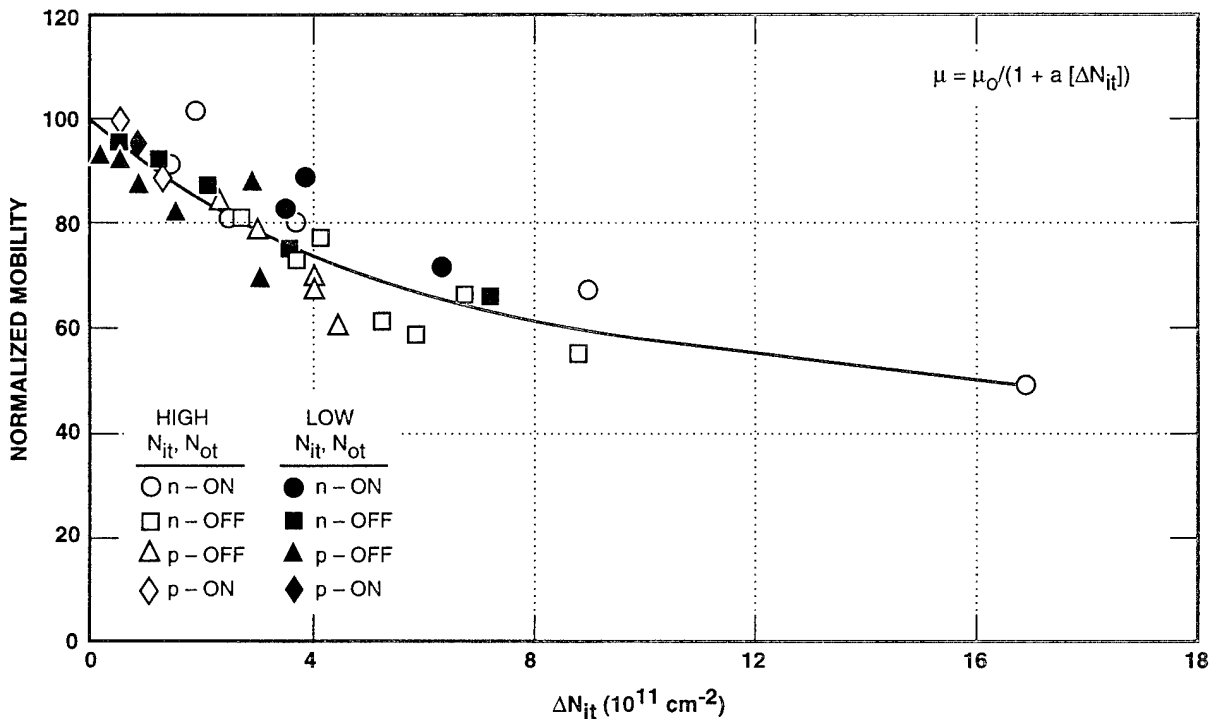


Figure 2-48. Normalized effective channel mobility as a function of radiation-induced interface trap density (Sexton and Schwank, 1985).

where:

W = channel width

$k' = (u_{\text{eff}} C_{\text{ox}})/2$

L_{eff} = effective channel length

V_G = gate voltage

V_R = threshold voltage

V_D = drain voltage.

This effect is shown in Figure 2-49.

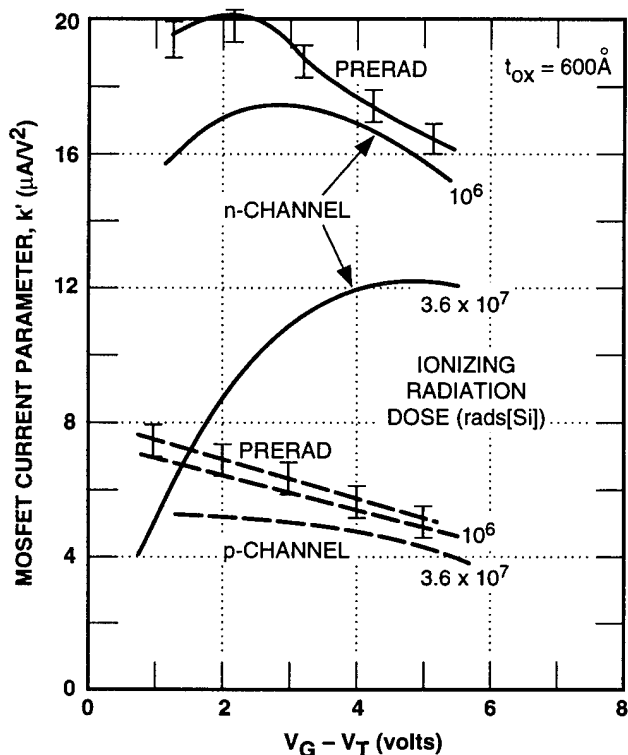


Figure 2-49. Ionizing radiation dose degradation of the parameter k' as a function of voltage for n- and p-channel transistors (Ports, 1980).

2.4.6 Other MOSFET Ionizing Radiation Dose Effects

Another consequence of interface trap buildup with irradiation is that the surface recombination velocity increases (Sivo, Hughes, and King, 1972; Snow, Grove, and Fitzgerald, 1967; Zaininger and Holmes-Siedle, 1967), leading to larger surface generation currents where junction edges are passivated by oxides; this effect is illustrated in Figure 2-50. Thus, junction leakage currents will tend to increase with radiation dose.

A second-order effect of radiation on transistor response occurs in the area of hot-carrier degradation. It has been shown that radiation increases the number of electron traps in an oxide. Trapped holes also exist after irradiation and it has been suggested that the recombination of electrons with previously trapped holes can lead to interface traps. Thus, it might be expected that after irradiation the hot-carrier response of MOS devices might be significantly worse than before irradiation, since a larger percentage of the electrons injected into the oxide as hot carriers might be trapped; also, interface traps might be more easily created. In support of this conjecture, larger positive threshold voltage shifts with hot-carrier stress have been reported for irradiated devices compared to virgin devices. Transistors with lightly doped drains to minimize hot-carrier effects were also shown to be degraded more by hot-carrier stress after irradiation than before. For devices that had been fabricated to be radiation-hard, the effect of irradiation on hot-carrier sensitivity was much smaller. In another study of radiation-hardened devices, the maximum linear transconductance degradation under hot-carrier stress was shown not to have been changed by previous irradiation. It then appears that by proper processing techniques the impact on subsequent hot-carrier degradation can be minimized.

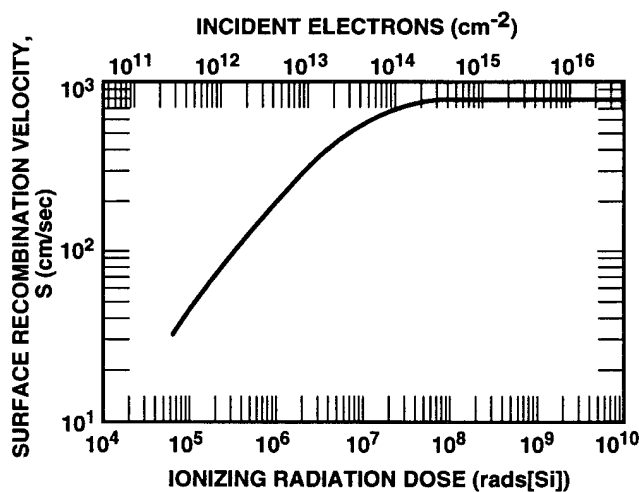


Figure 2-50. Surface recombination velocity of a depleted surface as a function of ionizing radiation dose [prerad value of $S = 5$ cm/sec] (Snow, Grove, and Fitzgerald, 1967).

2.5 Metal-Oxide-Semiconductor Integrated Circuit Ionizing Radiation Dose Response

In theory, the response of an IC to ionizing radiation dose should be predictable from a knowledge of individual transistor response. This section will build on the discussions of Subsections 2.3.3 and 2.3.4, which address the radiation response of individual bipolar and MOS transistors. In practice, making a quantitative estimate of the response of a complex IC is a formidable task because the transistors that comprise it can be biased at various potentials. The shifts in the transistor parameters depend on the applied bias (both pre- and post-irradiation) and the radiation dose rate, and the circuit response depends on these various combinations. Thus, in lieu of attempting to predict (or simulate) the complete IC response, critical parameters or timing paths will be identified and simulated/tested for worst-case conditions (Bhuva, Paulos, and Diehl, 1986).

The circuit parameters that are altered by ionizing radiation dose include power-supply currents, signal propagation times, input and output voltage levels, current drive capability, minimum and maximum functional frequencies, minimum power-supply voltage, and noise margin.

In addition, ionizing radiation dose can make circuits more susceptible to failure or further degradation caused by other environments, e.g., temperature, single-event upset, and transient radiation upset. Subsequent sections of this chapter will provide examples and further discussion of the effects of ionizing radiation dose on the above-noted circuit parameters.

2.5.1 Power-Supply Current

The power-supply current I_{DD} when a CMOS circuit is in standby mode is an important parameter of interest for many systems. I_{DD} increases markedly as the leakage current of individual transistors increases. In particular, the leakage current of an n-channel transistor will increase as its threshold voltage tends toward depletion mode with radiation, as shown in Figure 2-51. An increase in leakage current when the transistor

gate voltage is zero (and thus the transistor is OFF) translates directly into the static power-supply current I_{DD} as shown in Figure 2-52. Leakage current tends to decrease with time after irradiation as the n-channel threshold voltage increases. Leakage current also depends on the dose rate at which the radiation is received (since the negative n-channel threshold voltage shift is less at lower dose rates), as illustrated in Figure 2-53 for a 1-kbit SRAM. Other leakage currents (such as those from field-oxide regions) may in some circumstances also contribute to the overall circuit leakage. In addition to large changes in the standby current, significant changes can also be observed in the operating current of the part.

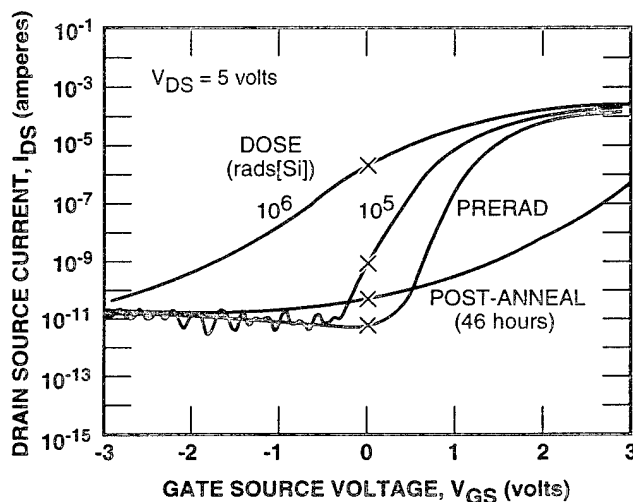


Figure 2-51. n-channel transistor subthreshold current characteristics; x indicates zero gate voltage intercept (Sexton and Schwank, 1985).

As stated, the response of an IC to ionizing radiation dose also depends on the state in which the circuit is irradiated. An example of this dependence is illustrated in Figure 2-54, which depicts the results of a test scenario designed to produce worst-case post-radiation power-supply leakage. In this example, worst-case leakage is engendered by irradiating a memory with one stored pattern (all ones) and measuring the post-irradiation leakage measured with its complement (all zeroes). During irradiation, the n-channel transistors that are ON

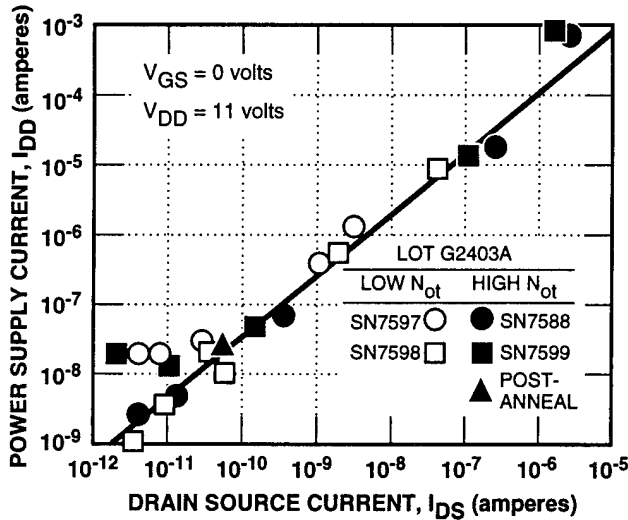


Figure 2-52. Integrated circuit standby power-supply current correlated with zero gate voltage transistor intercept [Figure 2-51] (Sexton and Schwank, 1985).

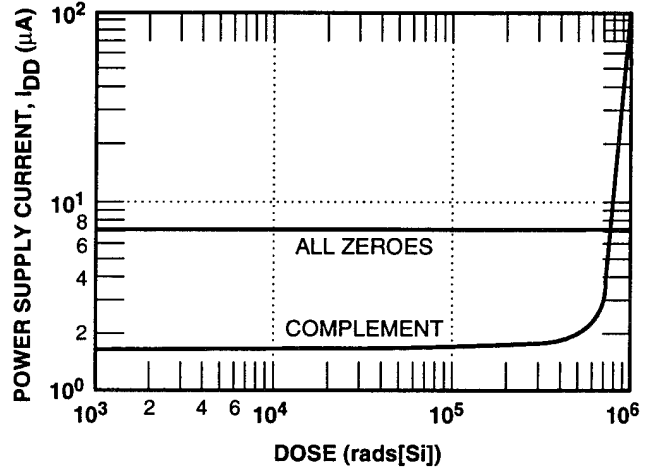


Figure 2-54. Standby power-supply current for a 16-kbit CMOS SRAM as a function of ionizing radiation dose for a test pattern that is the complement of that stored during irradiation; a noncomplemented pattern (all zeroes) is shown for comparison (Passow *et al.*, 1986).

have a maximum threshold voltage shift. The “not” pattern used for leakage current measurement will then cause the transistors that were biased ON during irradiation to be OFF so that subthreshold leakage (and parasitic field leakage) will be measured.

One final subject in this area is the effect of dose rate on ionizing radiation dose. This effect occurs because (1) at low dose rates, rebound, or recovery (gate-oxide positive charge annealing and interface state growth) occurs, causing circuit failures due to mobility-related issues (e.g., timing); (2) as the

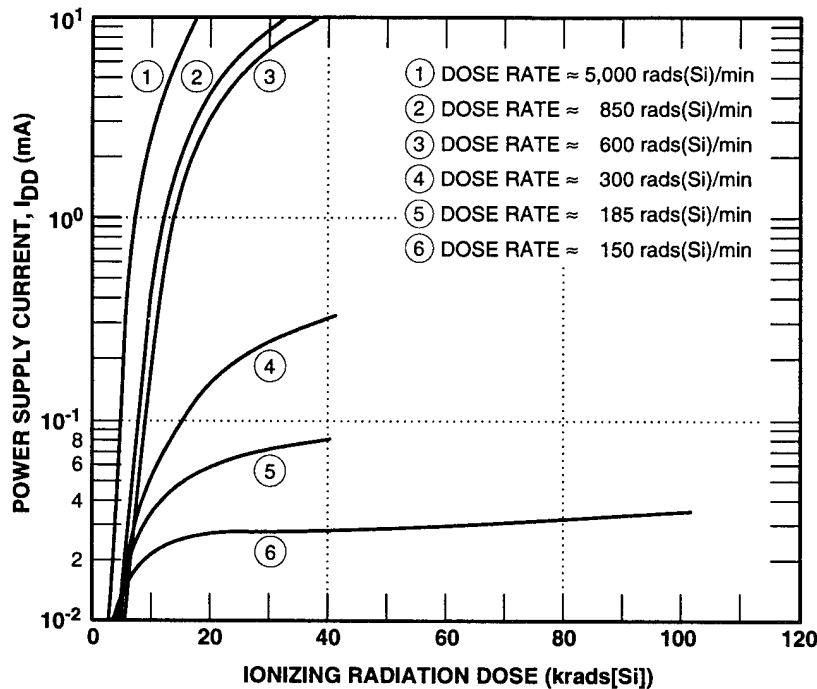


Figure 2-53. Standby power-supply current for a 1-kbit CMOS SRAM as a function of ionizing radiation dose (Abare, Huffman, and Moffett, 1982).

dose rate increases, the recovery is less complete and oxide trapped charge partially compensates the interface state (positive shift); and (3) as the dose rate continues to increase, the oxide trapped charge dominates and current-leakage-type failures result. This composite effect is depicted in Figure 2-55.

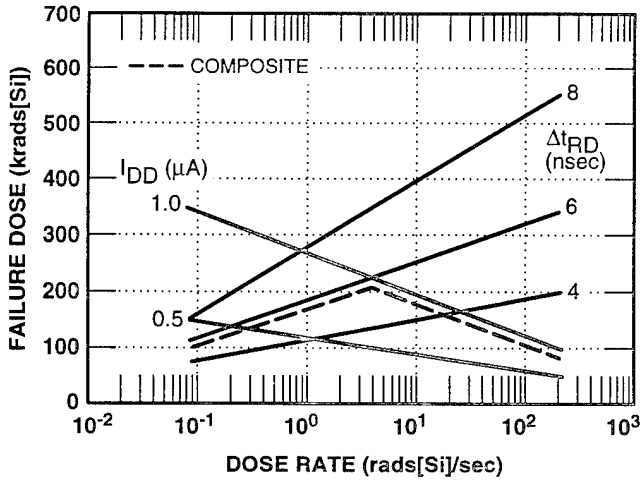


Figure 2-55. Ionizing radiation dose to cause failure for a Sandia SA3001 2-kbit CMOS SRAM as a function of dose rate. [Solid lines indicate the dose at each dose rate that will cause the indicated change in power-supply current (I_{DD}) or read access time (t_{RD}). Dashed line indicates the ionizing radiation dose at which the circuit will undergo a change of 1 mA in leakage current or a 6-nsec increase in read access time.] (Winokur *et al.*, 1986).

2.5.2 Circuit Timing Parameters

As discussed in Subsection 2.4.5, the effective transistor channel mobility decreases with increasing ionizing radiation dose. This effect, in conjunction with threshold voltage changes, impacts the time it takes to propagate a signal through a circuit.

The effect of radiation on the speed of CMOS integrated circuits can depend on the details of circuit fabrication, i.e., the various processes used in circuit manufacture. For fabrication processes that result in very little mobility degradation with radiation, the negative threshold voltage shift of the n-channel transistor can actually lead to improved performance in some parameters for some radiation dose levels. An example of this type of response for the read access time of a 16-kbit SRAM is shown in Figure 2-56. Over the dose range mea-

sured, the access time improves with radiation at all dose levels. (However, other parameters, such as power-supply leakage current, may still be degraded with radiation.)

For processes that have a larger interface trap buildup with irradiation, and thus more mobility degradation, the speed of the circuits tends to degrade with radiation. An example of this type of response for the read access time of another 16-kbit SRAM is shown in Figure 2-57, where the access time increases monotonically as the dose increases and as the devices rebound following the 200-krad(Si) irradiation.

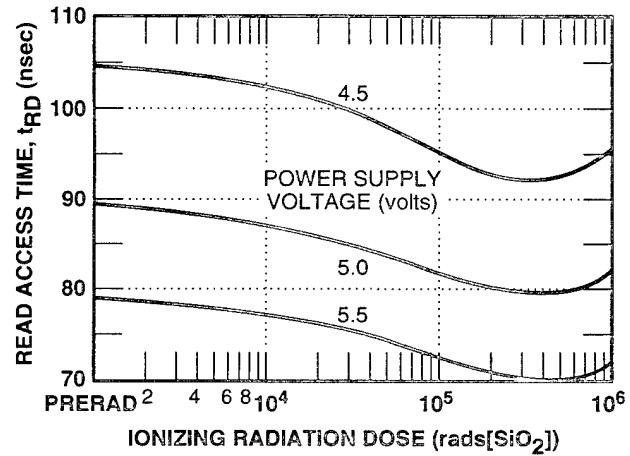


Figure 2-56. Read access time for a 16-kbit CMOS SRAM as a function of radiation dose for three power-supply voltages (Passow *et al.*, 1986).

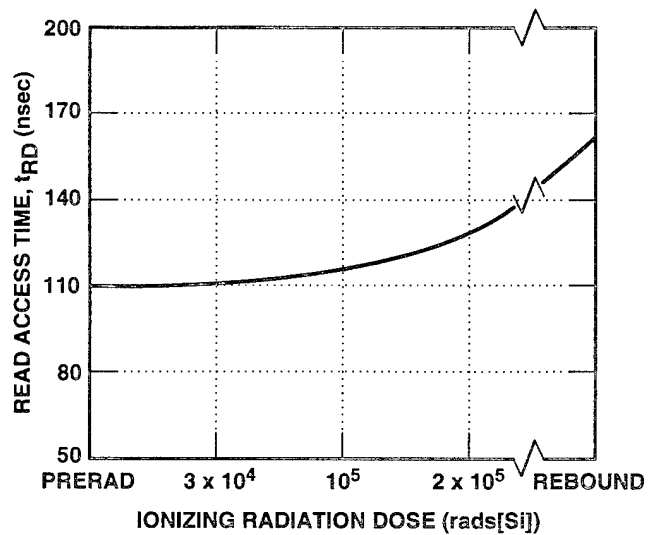


Figure 2-57. Read access time for a 16-kbit CMOS SRAM as a function of radiation dose and after rebound (a post-irradiation biased anneal) (Jones, n.d.).

Another response observed is intermediate between those shown in Figures 2-56 and 2-57, viz., the access time might improve at low ionizing radiation doses but be degraded at high ionizing ra-

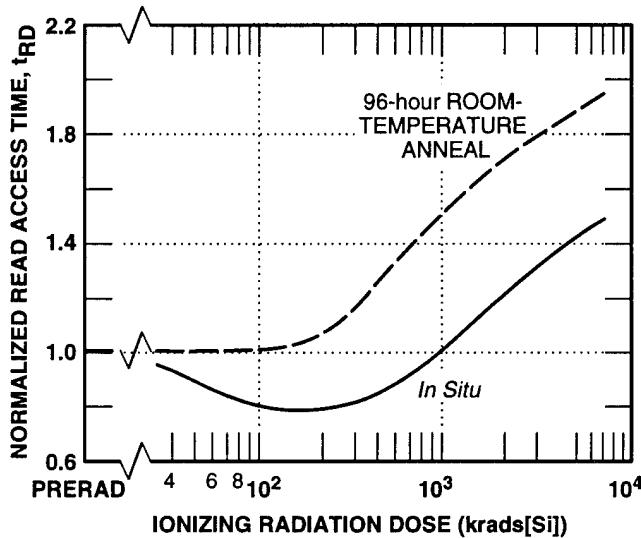


Figure 2-58. Normalized read access time for a 4-kbit CMOS SRAM as a function of radiation dose (Gingerich *et al.*, 1984).

diation doses. This is shown for measurements made soon after the completion of an irradiation in Figure 2-58.

The elapsed time from completion of irradiation to measurement of circuit parameters may affect measured response, as illustrated in Figure 2-58. If measurements are made many hours after the completion of the irradiation, the access time may degrade monotonically with radiation dose. The degradation observed for a particular ionizing radiation dose may depend on the dose rate of the radiation, as illustrated in Figure 2-59 for a 2-kbit SRAM. Here, the increase in read time is greater for radiation at the lower dose rate. Other RAM timing parameters, such as minimum write pulse width, generally show trends similar to the read access time for all of the above circumstances.

These differing characteristics in timing response can be due to differences in the way in which the circuits were biased during irradiation, in the manner in which the circuits were fabricated, in the time between completion of the radiation and testing of the circuit, and in the radiation dose rate. However, they can be understood

in terms of the differing individual transistor responses that occur as a function of dose, time, and dose rate, as discussed in previous sections.

Logic circuits may also show significant performance degradation with radiation. The maximum functional frequency for an 8-bit microprocessor as a function of radiation and rebound for two different processes is shown in Figure 2-60. Note that during the rebound test one of the microprocessors failed after a 50-hour anneal, indicating the importance of this type of testing for simulating space environments.

2.5.3 Input and Output Voltage and Current Parameters

Input voltage switching points (such as V_{IL} and V_{IH}) also change during irradiation, as would be expected since these parameters are closely linked to the threshold voltages of the transistors in the input stage. An example of the changes observed in input circuits for both CMOS and TTL input levels during irradiation and during a subsequent unbiased room-temperature anneal is provided in Figure 2-61. In this example, the switching levels decrease with radiation

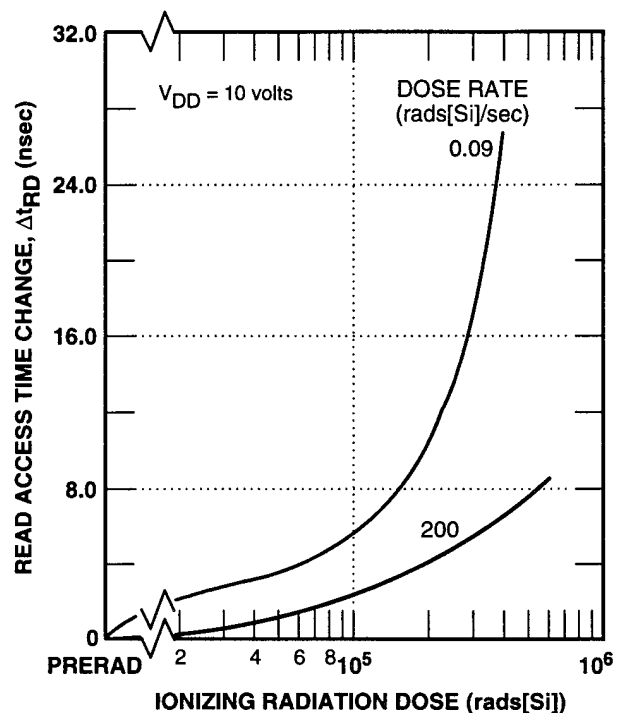


Figure 2-59. Change in read access time for a 2-kbit CMOS SRAM as a function of dose for two dose rates (Winokur *et al.*, 1986).

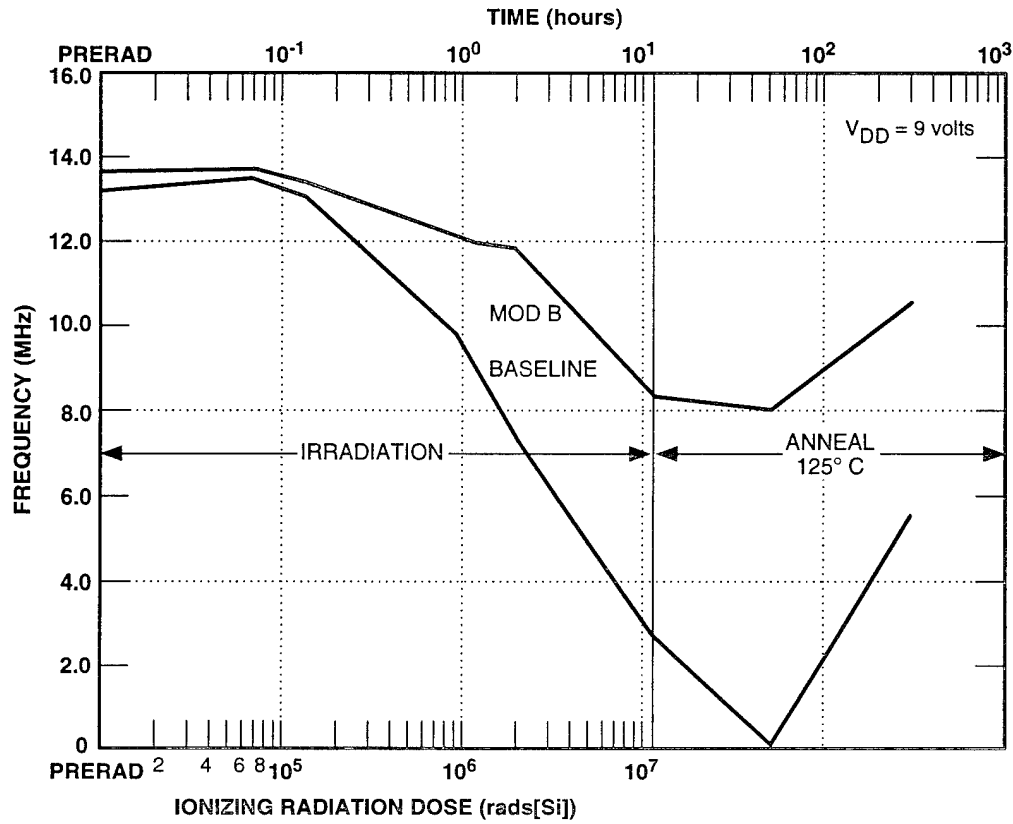


Figure 2-60. Maximum functional frequency for a microprocessor as a function of dose and anneal time for parts fabricated with two different processes (Sexton, n.d.).

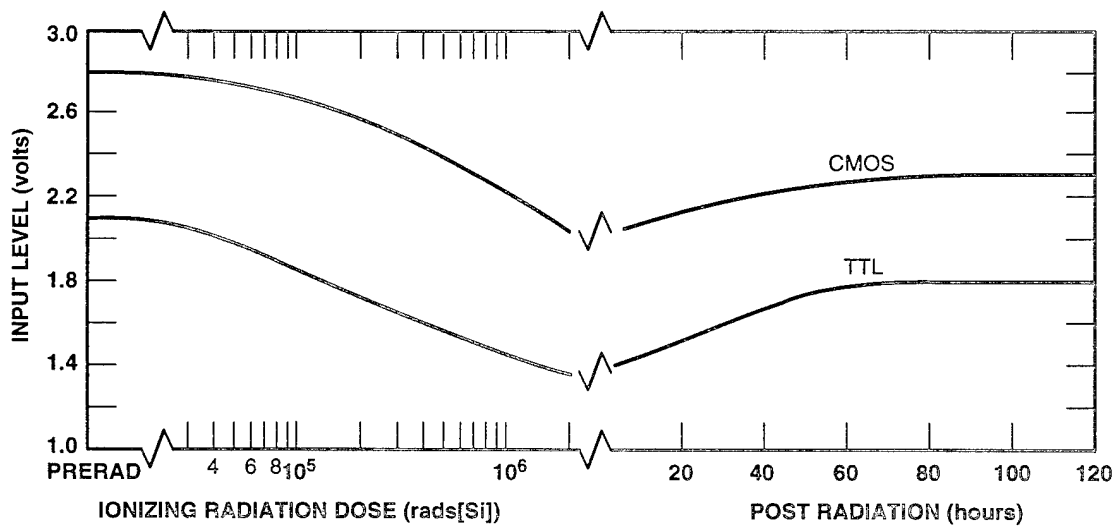


Figure 2-61. Input voltage switching points for CMOS and TTL buffers as a function of dose and post-radiation unbiased anneal at room temperature (Schroeder, Gingerich, and Bechtel, 1984).

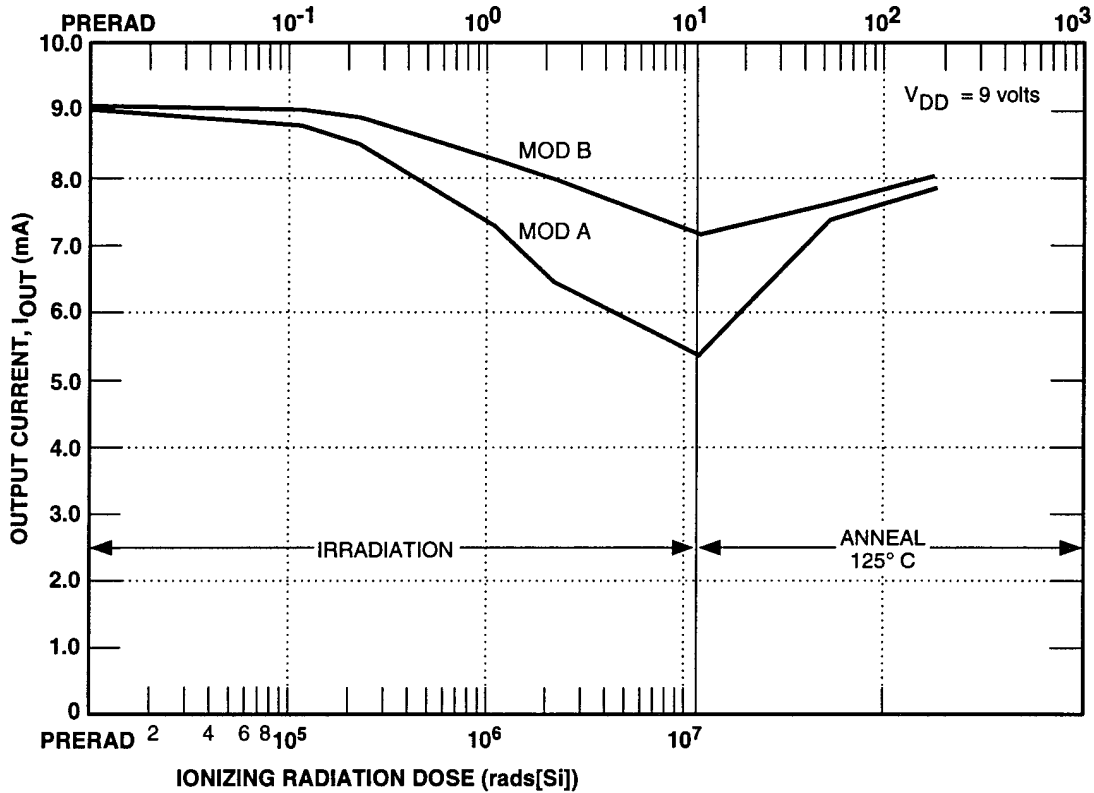


Figure 2-62. n-channel output buffer current drive as a function of radiation dose and post-irradiation biased anneal for parts fabricated with two different processes (Sexton, n.d.).

since the n-channel threshold voltage changes; the switching levels increase during the anneal as the transistor threshold voltages recover toward their pre-irradiation values. Output drive is directly linked to the degradation in individual transistor performance and thus shows similar response to that of a discrete transistor. An example of the degradation in n-channel output drive for two different processes as a function of radiation dose and rebound is shown in Figure 2-62.

Because of shifts in transistor threshold voltages, the minimum power-supply voltage at which circuits will operate (which must be greater than the magnitude of the n- and p-channel threshold voltages for a CMOS circuit) can change with radiation, often increasing as the dose increases. An example of this for a CMOS/SOS static shift register is given in Figure 2-63.

2.5.4 Minimum and Maximum Frequency Parameters

Dynamic circuits can experience an increase in minimum functional frequency due to increased

transistor leakage, in addition to the normal decrease in maximum functional frequency. This effect for a CMOS/SOS dynamic shift register is

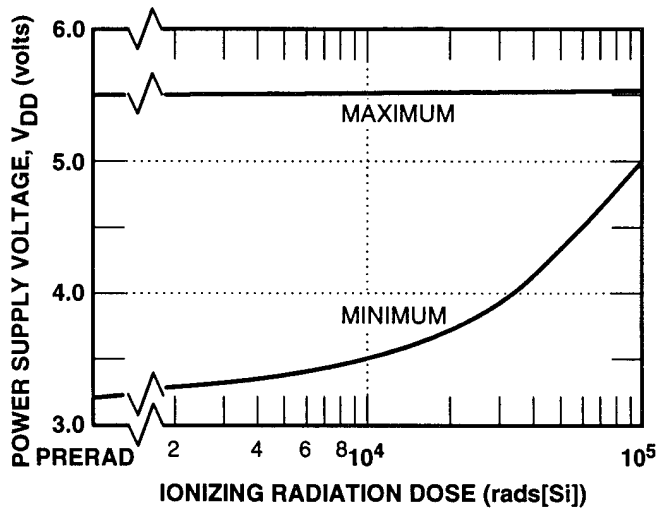


Figure 2-63. Maximum and minimum power-supply voltages at 5 MHz for a 64-bit, clocked CMOS/SOS static shift register as a function of radiation dose (Hatano and Doi, 1985).

illustrated in Figure 2-64. This effect is also observed with commercial microprocessors (which often contain dynamic nodes), causing them to be more radiation-tolerant when operated at high clock frequencies compared to low clock frequencies. Similarly, the increase in leakage with radiation leads to a decrease in hold time (or decrease in required refresh period) for dynamic RAMs (Myers, Danziger, and Soulanille, 1987; Sabnis, Nelson, and Billig, 1981).

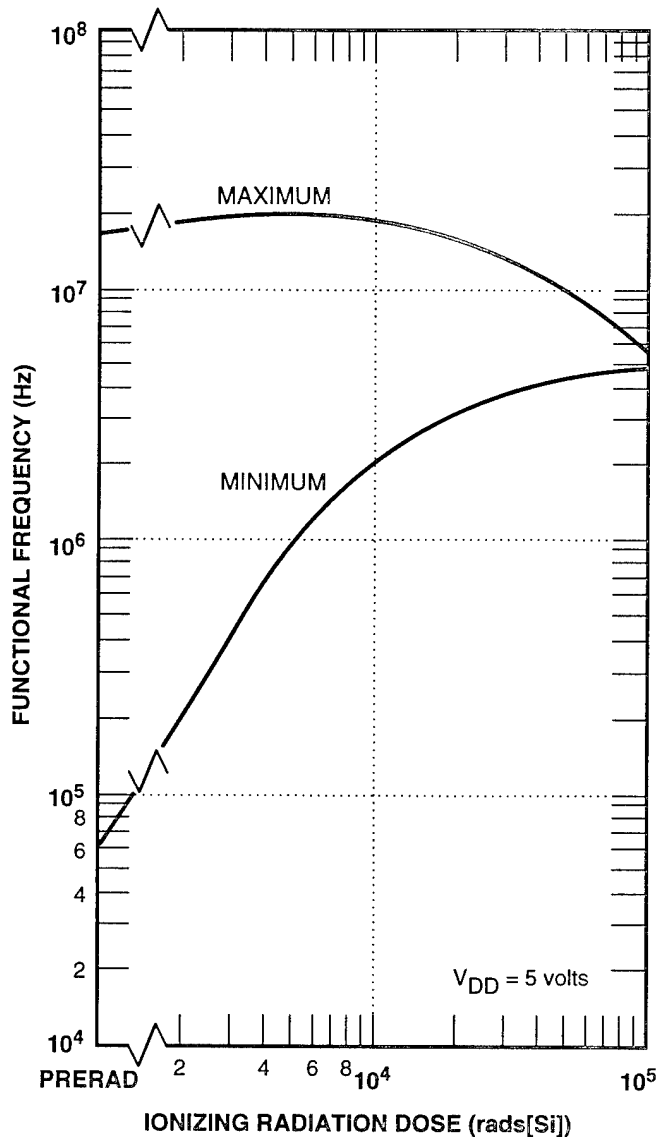


Figure 2-64. Maximum and minimum functional frequency at 5 volts for a clocked CMOS/SOS dynamic shift register with on-chip clock driver circuits as a function of radiation dose (Hatano and Doi, 1985).

2.5.5 Operating Margins Versus Ionizing Radiation Dose

In general, ionizing radiation dose tends to reduce operating margins in an MOS integrated circuit. Circuits designed for radiation hardness must account for more marked shifts, larger spreads, and greater nonuniformities in device parameters than those designed for operation in less severe environments. As an example of some of the factors involved in these effects, a few of the considerations pertaining to a static memory circuit will be discussed. The internal operating margins for sense circuitry in memories tend to decrease with increasing radiation dose. Figure 2-65 shows the main factors that determine the internal operating margins for the sense amplifier in a memory utilizing a CMOS memory cell with p-channel access

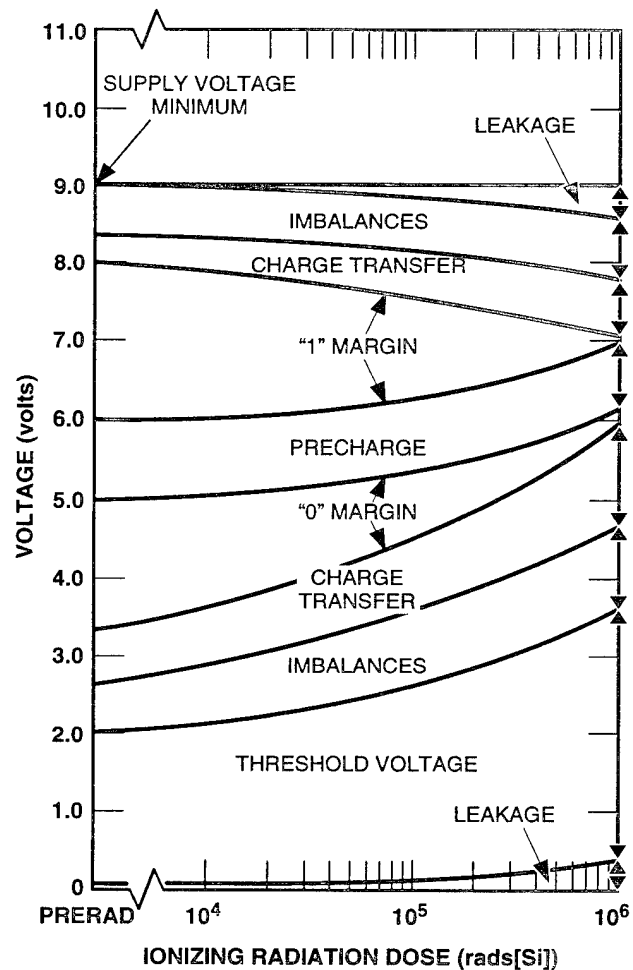


Figure 2-65. Principal features determining internal operating margins for a sense amplifier in a static memory circuit (Haraszti, 1978).

transistors and illustrates the changes that can occur as the dose increases. Initially, the margin for the sense amplifier to read a "1" is about 2 volts (from 6 to 8 volts) and that for reading "0" is about 1.7 volts (from 3.3 to 5 volts). Radiation-induced leakage currents reduce the logic "1" level and increase the logic "0" level in the cell by the amounts shown. With p-channel access transistors, the zero input to the sense circuitry is increased by the p-channel threshold voltage (≈ 1.9 volts pre-irradiation), which gets larger in magnitude as dose increases. Imbalances caused by offsets in the sense amplifier, and nonsymmetrical leakages and threshold voltages caused by the different shifts with radiation of transistors biased differently, can also serve to reduce the logic "1" level and increase the logic "0" level as dose increases. Charge transfer from the data and sense lines can cause transient reductions in the logic margin and must be considered for high-speed memory operation.

Variations in the precharge voltage from process, temperature, and radiation shifts can also reduce the "0" and "1" margins. For this example, these various factors all combine to reduce the margin of the sense amplifier to reading the logic states "1" or "0" to almost zero at 10^6 rads(Si); at this point, the sense amplifier will cease to be able to read the memory-cell contents correctly. This example assumed that both circuit- and process-hardening techniques were employed; with unhardened circuit design, the sense amplifier would be expected to fail from reduced operating margin at less than 20 krad(Si) (Haraszti, 1978). In addition to these effects on the sense amplifier circuitry, the fact that the transistors within the memory cell itself are biased differently during irradiation can lead to imbalances and preferred states from the memory cell. These internal imbalances cause the cell to be more vulnerable to upset by certain signals generated during the normal operation of the memory, which can lead to "read disturb" errors or other failure modes (Fleetwood *et al.*, 1986; Fleetwood and Dressendorfer, 1987).

The general reduction in operating margins caused by irradiation of integrated circuits means that the noise margins are reduced, thereby making

the circuits more susceptible to noise spikes caused by internal circuit operation or sources external to the integrated circuit.

2.5.6 Summary

As can be seen from the various examples provided in this section, the effect of ionizing radiation dose on MOS technology microelectronic devices is a relatively complex interaction of the irradiation level, dose rate, static and dynamic conditions of the circuit (both during and after irradiation), temperature, device processing, etc. In addition, a number of device parameters (e.g., leakage current, operating speed, input and output characteristics, etc.) must be considered separately to ascertain the effects of the irradiation on a specific device.

Also, although a device may be subject to parametric failure (e.g., leakage current specification is exceeded), functional failure may not occur until significantly higher levels (order of magnitude) of radiation are incurred. This fact exacerbates the problems associated with the determination of the level at which individual circuits cause system failure and must be addressed by the system designer.

As an indication of the complexity of the interaction of ionizing radiation dose with microelectronic devices, the effect of dose rate on failure levels is shown in Figure 2-66. The basic explanation for this effect is:

1. At low dose rates ($<10^{-1}$ rad/sec), the generation of interface state and annealing of trapped charge in the gate oxide dominate device response.
2. At mid-range dose rates (10^{-1} to 10^0 rad/sec), gate-oxide trapped charge and interface state generation (negative charge) compensate.
3. At high dose rates ($>10^0$ rad/sec), gate-oxide trapped-charge-induced failure modes dominate.

Three general classes of devices are generally encountered during the development of a system. These are: (1) radiation-hardened devices (e.g.,

space system applications), where trapped charge is generally the most significant problem and little interface state generation occurs; (2) radiation-resistant devices (not specifically fabricated for radiation robustness, but capable of operating at levels between 20 and 100 krad), where both charge trapping and interface state generation occur, but where charge trapping dominates (super-recovery is not generally expected); and (3) soft or commercial circuits capable of operation below 20 krad, where significant charge trapping and interface state generation should be anticipated in a radiation environment of 10 to 20 krad.

2.6 Ionizing Radiation Dose Effects on Bipolar Transistors

Prior to the introduction of MOSFETs, bipolar semiconductors were the dominant solid-state technology. Thus, this type of device is widely used in all types of military systems. However, since the introduction of CMOS technology a dramatic shift away from the use of bipolar integrated circuits has occurred. This shift can be attributed to the fact that CMOS devices require less power and can provide higher levels of integration density than bipolar devices.

Despite the attributes of CMOS technology, bipolar ICs are still used to some degree in almost all systems due to the fact that bipolar devices are ca-

pable of operating at higher speeds and can provide larger current drive than MOS technology devices. Also, bipolar devices are more suitable for implementing precision linear functions. In addition, the recent development of BICMOS, a class of integrated circuits that combines both bipolar and CMOS technology in a single circuit, permits the simultaneous optimization of both operating speed and power consumption. BICMOS technology has served to further perpetuate the life of bipolar technology through a number of new applications, e.g., very-high-speed cache memory, analog-to-digital converters, etc. Thus, despite the transcendence of CMOS technology for digital applications, the continuing use of bipolar technology for military applications is still of concern to designers. The effects of radiation on bipolar semiconductor devices are addressed here.

In general, ionizing radiation dose will affect bipolar devices in two ways: (1) reduction in current gain (β or h_{FE}), and (2) increased leakage currents. In addition, at extremely high levels of ionizing radiation (e.g., $\gg 1$ Mrad[Si]) bulk displacement damage (electron-induced atomic displacements) can occur. Electron displacement is similar to neutron displacement; since the effects of neutron irradiation are discussed in Chapter 4, no further discussion is provided here for bulk displacement damage.

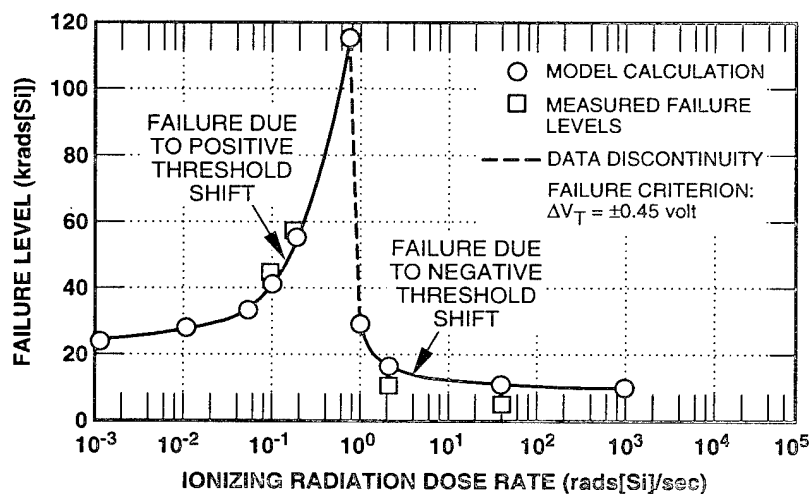


Figure 2-66. Dependence of circuit ionizing radiation dose failure level on dose rate (Johnston, 1984).

2.6.1 Current Gain Degradation

Basically, there are two distinct types of bipolar transistors. The first type of transistor is manufactured with a crystalline emitter in a planar structure [Figure 2-67]. However, advances in bipolar technology have led to the introduction of polysilicon (poly-Si) emitter devices [Figure 2-68], which have improved packing density and faster switching speed than the crystalline emitter transistors. From these cross-section sketches, it can be seen that the physical structure of the two types of transistors differ significantly, resulting in differences in their response to radiation. Although a detailed explanation of bipolar transistor operation is beyond the scope of this handbook, a variety of text books on this subject are available (e.g., Burger and Donovan, 1968; Messenger and Ash, 1986).

Ionizing radiation gain degradation in bipolar transistors has been studied extensively for crystalline emitter transistors (Gauthier and Nichols, 1983; Johnston and Plaag, 1987). Gain degradation has been determined to be the result of an increase in base current I_B due to (1) an increase in the surface recombination velocity caused by interface traps in the insulating oxide where the base and emitter-base depletion regions reach the surface, and (2) spreading of the field-induced depletion layer in the base region caused by oxide trapped charge. The oxide used to isolate the base and emitter contacts (called a spacer oxide in polysilicon transistors) is susceptible to the buildup of oxide trapped charge and interface states (Hart *et al.*, 1978). Moreover, interface states can de-

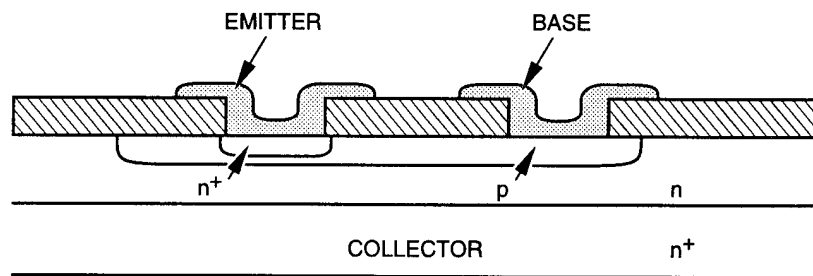


Figure 2-67. Crystalline emitter transistor cross section (Enlow *et al.*, 1991).

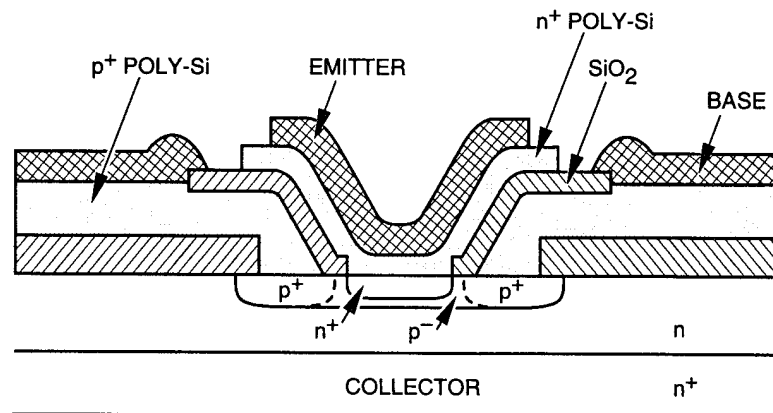


Figure 2-68. Polysilicon emitter transistor cross section (Enlow *et al.*, 1991).

grade the current gain β by increasing the surface recombination velocity S in both the base and emitter-base junction regions. The effect on bipolar transistor gain due to increased surface recombination velocity can be understood from Equation 2.13, which indicates that as S increases, β decreases

$$\frac{1}{\beta} = \frac{SA_s W}{D_B A_E} + \frac{\sigma_B W}{\sigma_E L_E} + \frac{1}{2} \left(\frac{W}{L_B} \right)^{1/2}, \quad (2.13)$$

where S and β are as defined above and

A_s	=	surface recombination area
W	=	base width
D_B	=	base doping
A_E	=	emitter area
σ_B	=	base conductivity
σ_E	=	emitter conductivity
L_E	=	emitter diffusion length
L_B	=	base diffusion length.

In addition, oxide trapped charge can deplete the lightly doped base regions near the oxide, increasing Shockley-Hall recombination. This trapped charge can eventually lead to conduction between the collector and emitter with no base drive. The base current can be depicted as:

$$I_B = \frac{I_s}{\beta_F} \exp\left(\frac{V}{V_B}\right) + I_{ss} \exp\left(\frac{V}{N_{ss} V_B}\right), \quad (2.14)$$

where

I_s	=	saturation current
β_F	=	preirradiation forward gain
V_{CE}	=	collector emitter voltage
V_B	=	base voltage
I_{ss}	=	surface saturation current
N_{ss}	=	ideality factor for surface recombination.

Radiation-induced degradation of polysilicon emitter transistors is also the result of an increase in interface traps in the oxide over the surface emitter-base junction. However, the depletion layer spreading found in crystalline emitter devices is

not present in polysilicon emitter transistors since the heavily doped extrinsic base region layer [p⁺-region shown in Figure 2-68] prevents any significant spread in the field-induced depletion layer (which can result from the trapped-charge buildup in the oxide). In crystalline emitter transistors, however, both effects are present due to the more lightly doped base region, resulting in an improvement in the performance of polysilicon emitter devices over the crystalline devices, as shown in Figure 2-69. Additionally, it has been noted (Jenkins *et al.*, 1991; Nowlin *et al.*, 1991) that ionizing radiation dose causes an increase in the base current. This is consistent with the premise that nonideal base currents are primarily due to increased recombination at the emitter periphery due to interface state density buildup in the surface oxide, leading to the observation that initially the base current is approximately in the ratio of emitter areas, and as the dose increases (where interface state density becomes significant) this ratio approaches that of the emitter perimeters. This is shown in Figure 2-70 for two different polysilicon emitter transistors. Thus, gain degradation due to ionizing radiation will not only be a function of the spacer oxide process but also of the device geometry. Additionally, recent work (Nowlin *et al.*, 1991) has indicated that a dose-rate

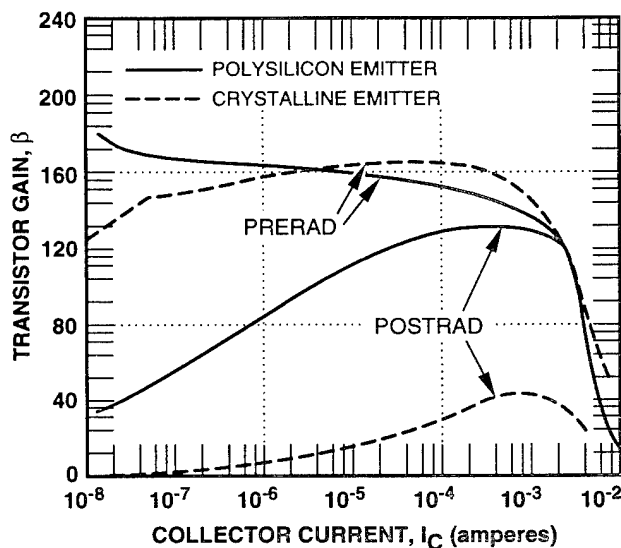


Figure 2-69. Gain degradation after exposure to an ionizing radiation dose of 250 krad(Si) (Nowlin *et al.*, 1991).

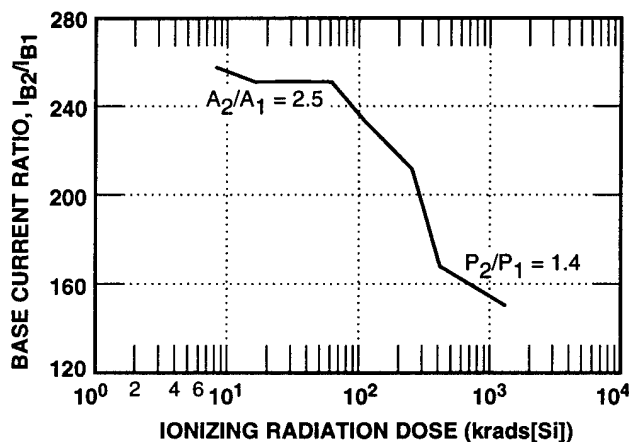
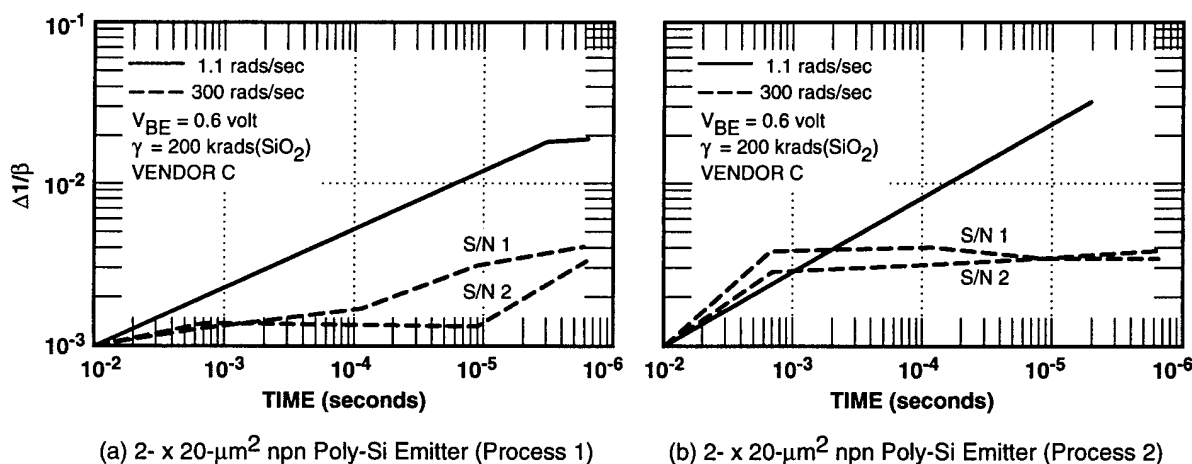


Figure 2-70. Ratio of base currents for two poly-Si emitter devices, illustrating that at low doses, base currents are approximately in the ratio of emitter areas (A), and at higher doses, the ratio approaches that of the perimeters (P) (Nowlin *et al.*, 1991).

effect may be present wherein a more significant ionizing radiation gain degradation is experienced at lower dose rates [see Figure 2-71]. This effect will impact radiation test strategies to ascertain worst-case device performance.

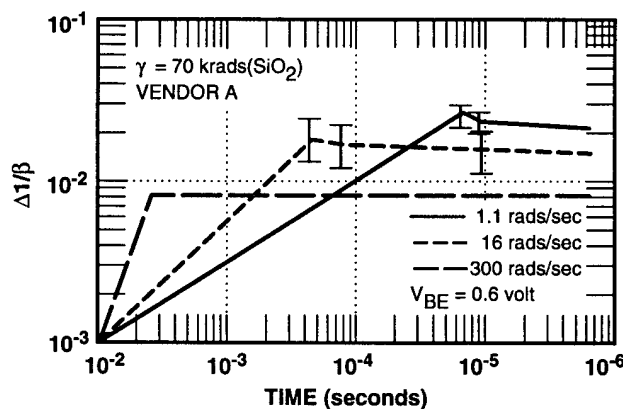
2.6.2 Radiation-Induced Leakage Currents

Ionizing radiation dose affects leakage current in bipolar transistors in two ways: (1) increased leakage between adjacent devices, and (2) increased collector-to-emitter leakage. The effects of ionizing radiation dose on the generation of device and device-to-device leakage currents are depicted in Figures 2-72 and 2-73. Figure 2-72 is a vertical cross section of a bipolar transistor that uses recessed field oxide (ROX) technology, which was



(a) 2 x 20- μm^2 n-p-n Poly-Si Emitter (Process 1)

(b) 2 x 20- μm^2 n-p-n Poly-Si Emitter (Process 2)



(c) 11- μm -Diameter p-n-p Crystalline Emitter

Figure 2-71. Change in $1/\beta$ as a function of dose rate [all data taken at room temperature; time measured from start of irradiation] (Enlow *et al.*, 1991).

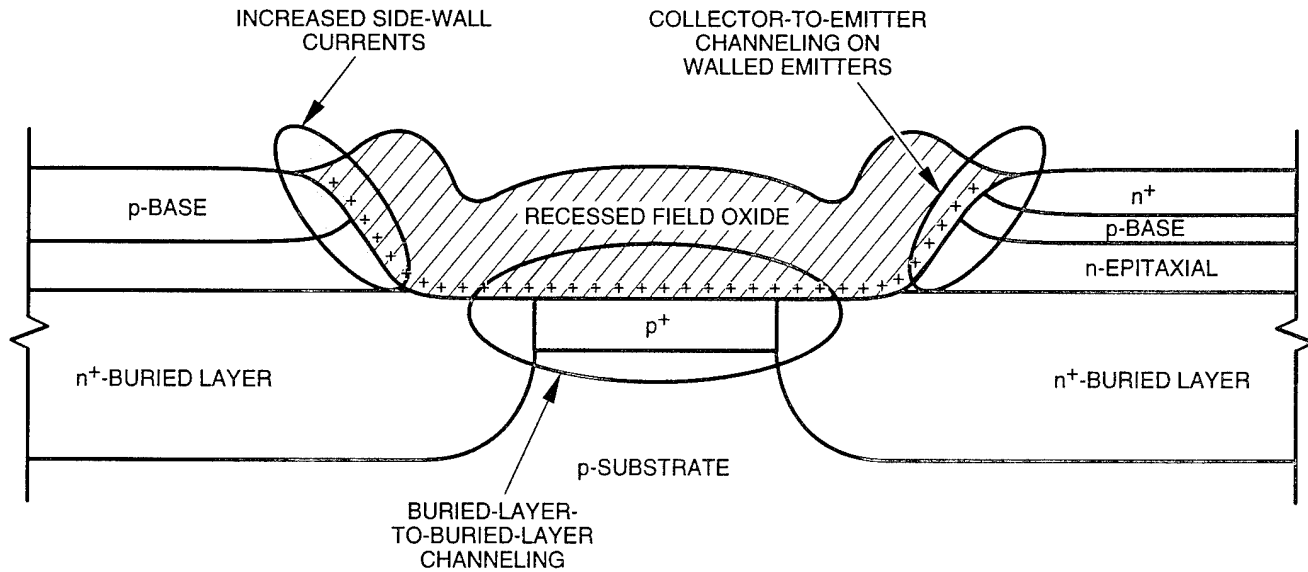


Figure 2-72. Regions of possible radiation-induced charge buildup and leakage currents in recessed-oxide, bipolar, walled emitter device (Pease, Emily, and Boesch, 1985).

introduced in the early 1970s and has become the most widely used isolation technique for both bipolar and MOS transistors, to obtain isolation between adjacent transistors. Figure 2-73 illustrates the effects of radiation on leakage current for bipolar transistors employing ROX technology.

The effects of ionizing radiation dose, i.e., hole trapping in the field oxide and the subsequent generation of interface states, result in several types of leakage current degradation in bipolar transistors, as shown in Figure 2-72. These can be grouped as (1) device-to-device leakage due to the

inversion of the p^+ -layer located beneath the ROX, or (2) leakage caused by the inversion of the base-region p -surface that contacts the ROX side wall due to trapped charge on the ROX surface. The time-dependent response of these effects is somewhat similar to that experienced in MOSFETs in that initially there is a buildup of charge, followed by annealing, and a subsequent interface state buildup, all of which are bias-, process-, and temperature-dependent.

2.7 Ionizing Radiation Dose Effects on Linear Bipolar Integrated Circuits

Linear bipolar ICs are briefly addressed here, separate from bipolar transistors [Section 2.6] because:

1. Currently, most linear IC applications are achieved with bipolar technology. However, it should be noted that MOS and BICMOS technology devices are becoming more widely used for linear applications.
2. Linear application ICs have failure modes distinctly different than digital ICs.

Bipolar linear ICs are sensitive to ionizing radiation dose effects. The primary parameters of concern are input bias current (I_b), input offset current

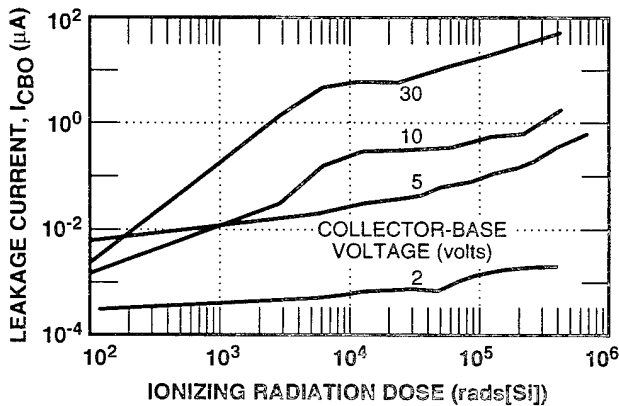


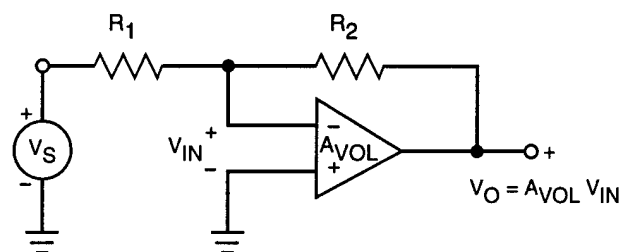
Figure 2-73. Effects of ionizing gamma dose on leakage current for a typical bipolar transistor (Johnston, 1980).

(I_{OS}), input offset voltage (V_{OS}), and open-loop voltage gain (A_{VOL}). However, for nonhardened commercial ICs, parameter changes can begin to occur at levels of around 10 krad(Si), as indicated by an increase in bias current. In general, bias current will increase before any changes in either input offset current or voltage occur. Moreover, it is usually changes in these two parameters, rather than the open-loop gain or input bias current, that actually cause IC failure.

A schematic diagram of an operational amplifier connected as an inverting-mode amplifier is shown in Figure 2-74. The output voltage equations as a function of *finite* [as opposed to *infinite*] open-loop gain, input offset current, and input offset voltage are provided. From these relationships, the effect of ionizing radiation dose, which lowers A_{VOL} and increases both I_{OS} and V_{OS} , can be qualitatively deduced. Moreover, since A_{VOL} is generally large (>90 dB), the effects of changes in I_{OS} and V_{OS} are usually more significant. Figure 2-75 depicts the effects of ionizing radiation dose on various IC parameters for an unhardened device.

In conclusion:

- At present, linear circuit applications are predominantly implemented with bipolar ICs. However, this trend is changing, with both MOS and BICMOS ICs accounting for a greater share of these applications.
- Bipolar linear application ICs fail in different ways than digital ICs, e.g., changes in I_{OS} and V_{OS} . However, failure modes common to both classes include increased input bias current and open-loop voltage gain degradation.
- In lieu of abrupt parametric failure modes, which occur in digital application ICs, analog circuits manifest parametric failures that can be application-specific, making the establishment of specific failure criteria difficult and thus impacting the development of a radiation hardness-assurance program.



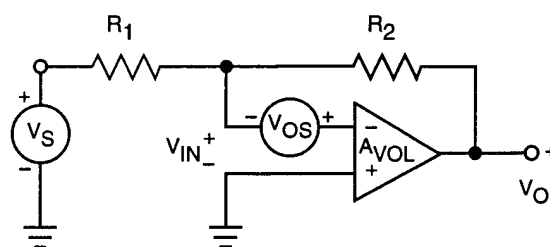
$$V_O = -\frac{V_S R_2}{R_1}$$

$$A_{VOL} = \infty$$

$$V_O = -\frac{V_S R_2}{R_1} \left[\frac{1}{1 + \frac{1}{A_{VOL}} \left(1 + \frac{R_2}{R_1}\right)} \right]$$

$$A_V \neq \infty$$

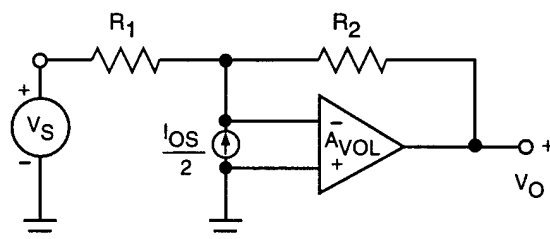
(a) Effects of Finite Open-Loop Voltage Gain



$$V_O = -\frac{V_S R_2}{R_1} - \left[1 + \frac{R_2}{R_1}\right] V_{OS}$$

$$A_{VOL} = \infty$$

(b) Effect of Input Offset Voltage



$$V_O = -\frac{V_S R_2}{R_1} + \frac{I_{OS}}{2} R_2$$

$$A_{VOL} = \infty$$

(c) Effect of Input Offset Current

Figure 2-74. Effect of finite open-loop voltage gain, input offset voltage, and input offset current on the performance of an operational amplifier.

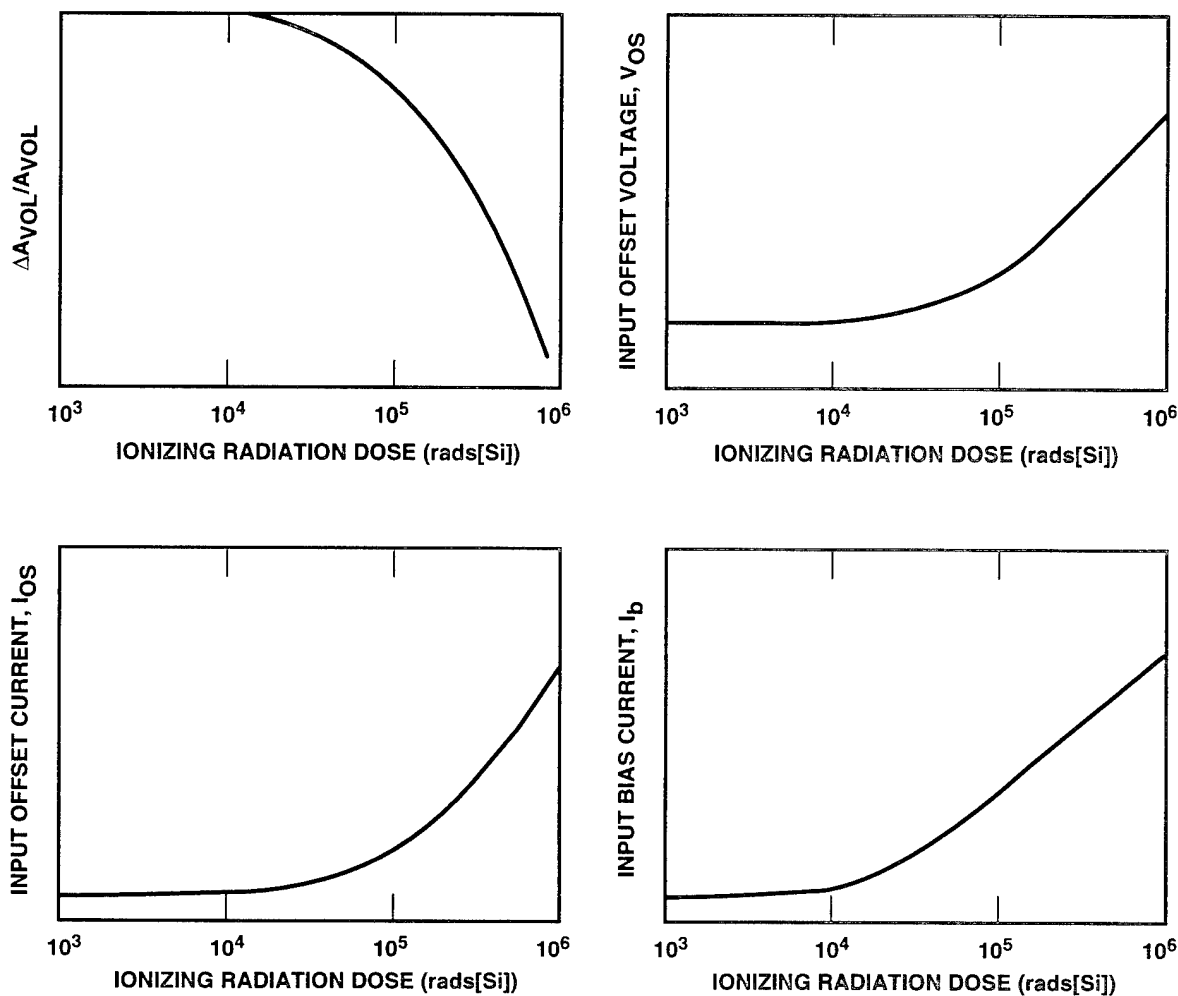


Figure 2-75. Linear IC parameter variation with ionizing radiation dose (Rose, 1984).

2.8 Ionizing Radiation Dose Effects on Gallium Arsenide

Gallium arsenide (GaAs) is a semiconducting crystalline material similar to Si; therefore, it is subject to the same basic ionizing radiation effects that occur in Si. However, some of the different consequences of radiation effects on the electrical characteristics of GaAs devices lead to qualitatively different radiation susceptibilities. The ionizing radiation dose hardness of GaAs devices is generally very good because GaAs technologies do not employ gate oxides. Neutron effects (displacement damage) are considerably smaller because lifetime degradation is generally unimportant in GaAs technologies [see Chapter 4]. Thus, it can be generally asserted that the ionizing radiation dose hardness of GaAs circuits is superior to the Si-based circuits. The ionizing radiation dose hardness level for present-day, state-of-the-art GaAs

devices is approximately 10^7 to 10^8 rads(GaAs). Each of the radiation susceptibility categories is discussed here in more detail for GaAs, indicating some of the primary radiation effects problems of concern (Zuleeg and Lehovc, 1980).

The insensitivity of GaAs to ionizing radiation dose, at least for permanent effects, is due to: (1) the absence of gate insulators in GaAs devices, and (2) the absence of parasitic current leakage paths under field or passivation insulators (due to the difficulty of inverting GaAs surface regions). This latter factor is a result of very high interface-state densities present (before irradiation) in all GaAs insulator interfaces; effectively, the Fermi level at an interface is pinned at a fixed constant value by the high N_{it} density. For precisely this reason, it has not been possible to fabricate high quality GaAs metal-insulator-semiconductor (MIS)

devices. [It should also be noted with respect to the first factor that Si JFET technology, which also does not use gate oxides, also enjoys a higher tolerance to total dose than other Si technologies.]

The high insensitivity of GaAs to ionizing radiation dose is clearly illustrated in Figure 2-76, which shows experimental results of drain source current I_{DS} versus gate voltage V_G for an enhance-

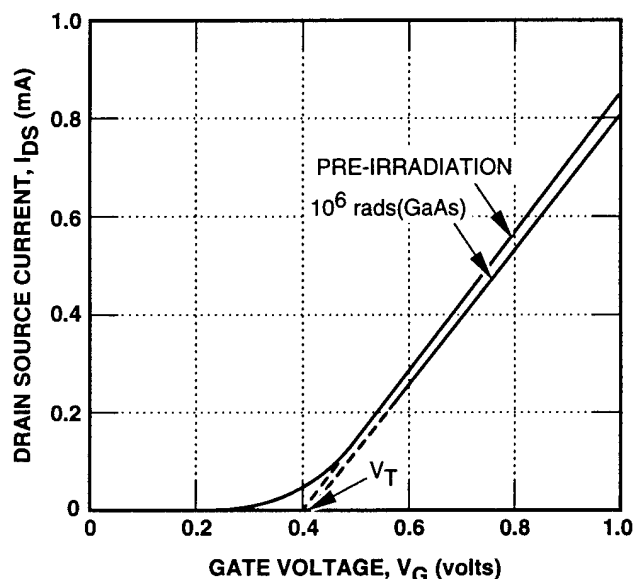


Figure 2-76. Effect of irradiation on the drain current-gate voltage characteristic of epitaxial GaAs JFET; channel region doping density, $10^{17}/\text{cm}^3$ (Zuleeg and Lehovc, 1980).

ment-mode GaAs JFET, before irradiation and after exposure to an ionizing radiation dose of 10^8 rads(GaAs). Before the irradiation, threshold voltage V_T was 0.40 volt, and it did not change significantly after irradiation.

Although GaAs devices are basically immune to long-term ionizing radiation dose effects, a transient effect has been observed that is associated with ionizing-radiation-induced charging of chromium-doped semi-insulating (SI) GaAs substrates, which are widely used in GaAs FET structures for isolation purposes. This substrate charging causes a reduction in the drain current I_{DS} of the transistor, with observed time constants as large as seconds; its effect on I_{DS} is depicted in Figure 2-77, which shows I_{DS} normalized to its pre-irradiation

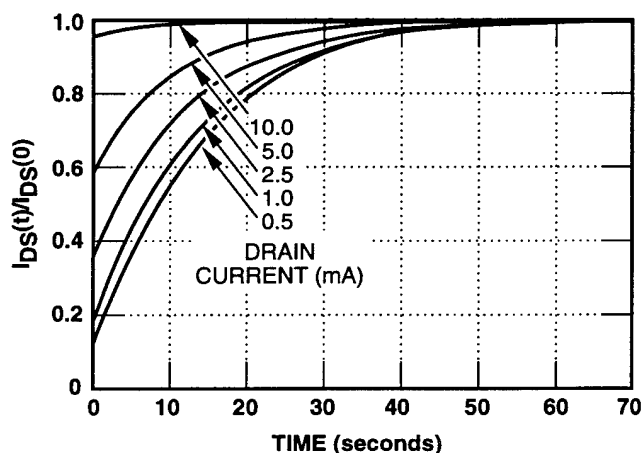


Figure 2-77. Pulsed radiation response characteristics at various levels of drain current for a GaAs JFET (Simons and King, 1979).

value plotted versus time following 100 rads(GaAs) of pulsed (3-nsec) 600-keV x-ray irradiation for a series of initial I_{DS} values. These I_{DS} transients are characterized by peak reductions in current amplitude ranging from 90 percent of the quiescent current at 0.5 mA to less than 5 percent at the 10-mA level. The recovery-time constants associated with these data range from 10 to 14 seconds.

A schematic model indicating the cause of the transient reduction in I_{DS} is shown in Figure 2-78. A net negative charging of the semi-insulating (SI) substrate is depicted, which induces a back-gate depletion region in the p-GaAs epitaxial layer (n-channel region) next to the interface with the substrate. This induced depletion region then reduces,

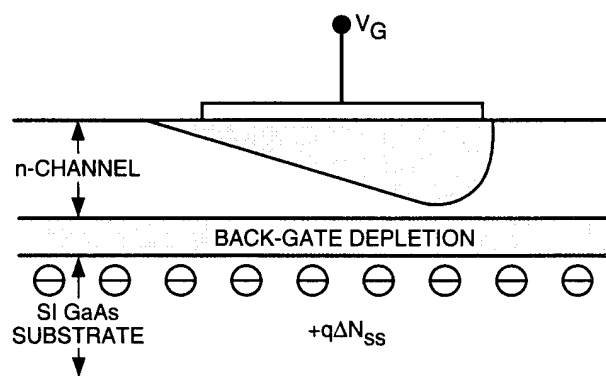


Figure 2-78. Schematic cross section of gate region GaAs JFET, indicating the effects of transient substrate charging (Anderson, Simons, and Tseng, 1986).

or pinches, the electron current flow in the n-channel. The substrate charging was attributed (Anderson, Simons, and Tseng, 1986; Simons and King, 1979) to electron trapping in deep trap levels associated with the chromium impurities. Based on the time constants for the discharge of the traps (recovery of I_{DS}), the energy level of the traps was determined to be ~ 0.8 eV. The transient charging problem can be avoided by using carefully prepared intrinsic SI GaAs substrates having low impurity concentrations (Zuleeg, Notthoff, and Troeger, 1982) or by the use of a conducting p-GaAs buffer layer (Anderson, Simons, and Tseng, 1986; Anderson *et al.*, 1982) between the active channel and SI substrate.

2.9 Power Semiconductor Devices and Integrated Circuits

This section addresses the effects of ionizing radiation dose on power semiconductor devices and integrated circuits.* However, before proceeding with a discussion of radiation effects in power semiconductor devices and ICs, several background subjects will be discussed to provide a context for understanding this class of ICs.

2.9.1 Power Distribution

A spacecraft system is used as an example here; however, this discussion can be generalized by substituting an alternate primary electrical power source for the solar-cell array.

All spacecraft, and virtually any other complex electromechanical system (e.g., tank, aircraft, etc.),

require a source of power and a means of converting that power into a form that can be utilized by the on-board electronic systems. Most earth-orbit satellites utilize large arrays of solar cells to convert sunlight to electrical power. The power is then bused at high voltage (270 volts) to a preprocessor that lowers the voltage to 28 volts and then on to a power supply that supplies regulated power to the on-board electronics, usually at ± 5 volts or +10 volts.

The conversion of power from 28 volts to 5 volts, or any other voltage, is performed by a dc-dc converter. The two ways to supply regulated power to spacecraft electronics are known as centralized and distributed architectures. In a centralized architecture [see Figure 2-79], 28-volt power is supplied to a single dc-dc converter, which then generates multiple outputs and buses the conditioned power to all the boards on the spacecraft.

A distributed architecture [Figure 2-80] buses the 28-volt power directly to each board, where an on-board dc-dc converter converts the power according to the needs of that particular board. Distributed power offers a number of significant system advantages. Since all busing to the boards is at a relatively high voltage, power losses are very low, using only moderately sized wire. Any voltage losses that occur during busing are inconsequential since regulation occurs directly on the board. The delivered power is virtually free from the noise and cross talk associated with busing regulated power through long wires. Each board is

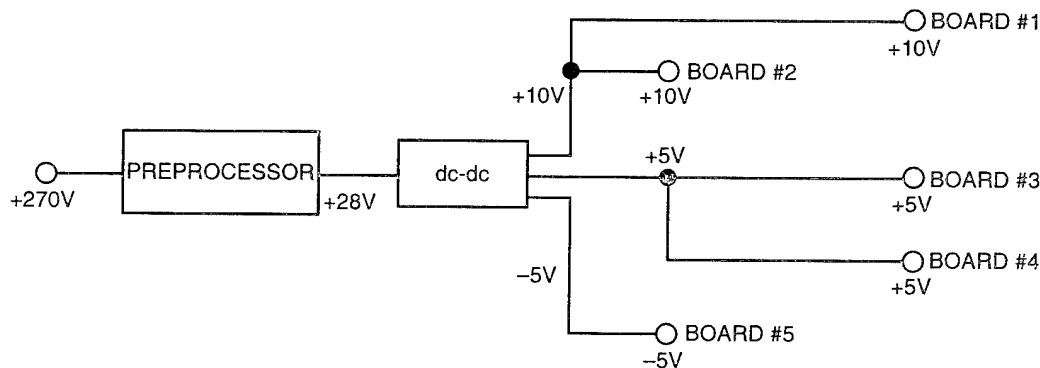


Figure 2-79. Centralized power architecture (Desko, 1991).

*This section is largely taken from Desko (1991).

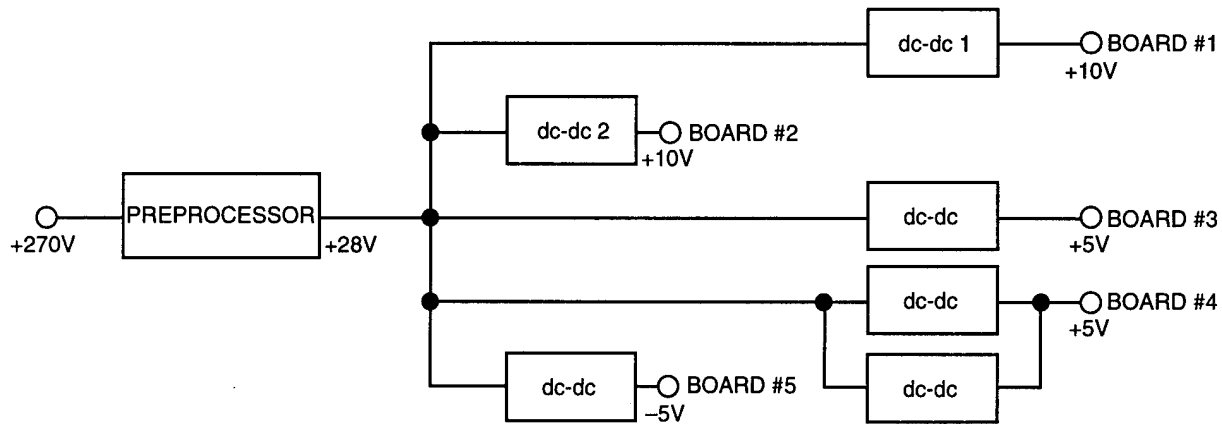


Figure 2-80. Distributed power architecture (Desko, 1991).

isolated from the fluctuating power demands of other boards. Each local supply has control circuitry to protect itself and the load it powers. A failure on one board can be isolated to protect the rest of the system. For critical circuits, redundancy can be provided. Since all power supplies dissipate heat, a distributed architecture aids in heat dissipation, which can be a critical factor in space where convective cooling is absent.

A distributed power system also increases the amount of monitoring and control possible. The power conditions on each circuit board can be monitored and individual circuit boards can be shut down to conserve power when not in use. System design flexibility is greatly enhanced since power needs are specified at the circuit-board level, not the system level. Also, circuit-board performance can be enhanced by selection of the optimum power supply for that particular board.

It is apparent that the advantages of a distributed power architecture are significant, especially for a space system. These advantages, however, are subject to some constraints. Each power-supply module must fit on a circuit board and take up minimal volume while supplying all the power needs of the circuit board. In addition, the weight must be minimized; the weight of all the local supplies should not be significantly greater than the weight of the centralized dc-dc converter. The local supply must indeed contain all the control circuitry previously described to protect both itself and its load as well as the rest of the system. Finally, a distributed power architecture typically

requires a high-performance dc-dc converter architecture and high-performance silicon devices and/or integrated circuits to obtain high power densities.

2.9.2 Power Semiconductor Device and IC Application

The objectives of the following discussion are to (1) provide an understanding of dc-dc converter operation, and (2) indicate the requirements placed on semiconductor devices based on the converter operation.

The requirement is to convert dc voltage obtained from the solar collectors, nuclear reactor, or radioactive thermal generator (RTG), which is preregulated to 28 volts, to regulated dc voltage (or voltages) to power the on-board electronic equipment. The system that delivers regulated dc voltage is referred to as a power supply and is composed of a dc-dc converter plus control circuitry. The dc-dc converters used in many commercial applications and in all space applications utilize an electrical isolation transformer to fully isolate the load and the source. However, the discussion will begin with a simple dc-dc converter with no isolation.

In dc-dc converters or power supplies, the dc output voltage must be controlled within some specified limits, while the input voltage and output load may fluctuate. This regulation of the output voltage is accomplished in a switch-mode power supply through the use of switches, as seen schematically in Figure 2-81. Ideally, these switches

are nondissipating and the efficiency of this method of conversion is very high — 80 to 90 percent. A switch-mode converter works by opening and closing the switches that supply voltage to the output. By controlling the ON and OFF durations, the desired average output voltage can be achieved, as seen in Figure 2-82. In this simple circuit, the average output voltage can be set anywhere from zero to V_{IN} since the average output voltage is given by:

$$\overline{V_{OUT}} = \frac{(V_{IN})(t_{ON})}{t_{ON} + t_{OFF}} \quad (2.15)$$

By using an L-C (inductor and capacitor) filter network, this square-wave output can be converted to a steady dc output of the desired value with the desired amount of output ripple, as seen in Figure 2-83. Methods other than switch-mode, such as a linear regulator, are available to obtain a regulated

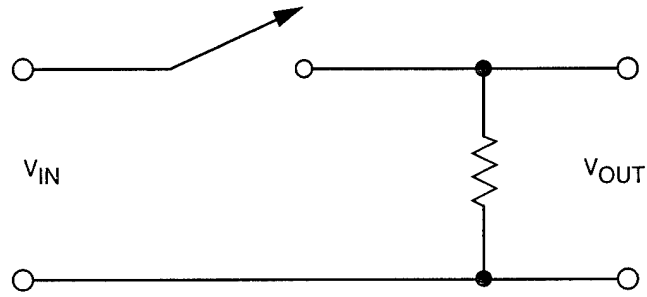


Figure 2-81. Switch-mode power supply schematic (Desko, 1991).

dc output. However, all other methods require the use of dissipative components, which significantly lower power-supply efficiency (by as much as 35 percent); and are unsuitable for space applications.

The most common method of controlling the output voltage is switching at a constant frequency and adjusting the ON duration of the switch (duty

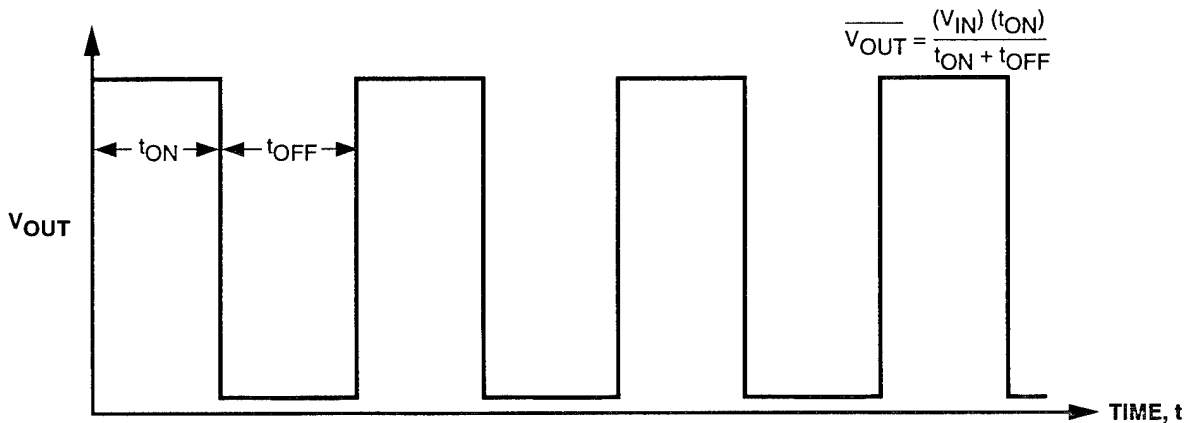


Figure 2-82. Output voltage of a switch-mode power supply (Desko, 1991).

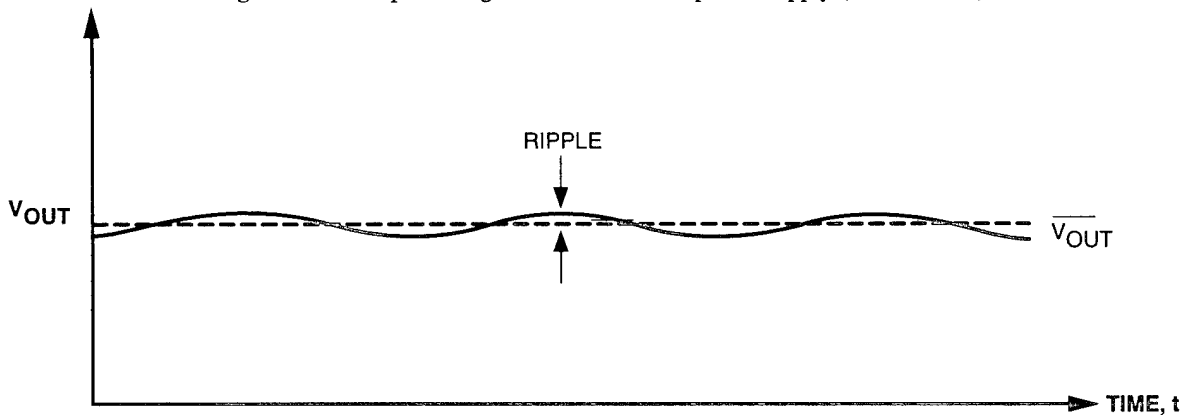


Figure 2-83. Output voltage of a switch-mode power supply using an L-C filter network (Desko, 1991).

cycle) to control the average dc output voltage, a method known as pulse-width modulation (PWM) switching. Other methods of control are possible for switch-mode controllers that are also referred to as PWM, such as switching at constant frequency and adjusting the OFF duration. Frequency-modulation (FM) switching is most common for resonant converters. For zero-voltage-switch resonant converters (where the voltage waveform crosses zero when the switch is turned ON), constant OFF-time/variable frequency control is used.

In a PWM converter, a control signal must be generated to control the duty cycle of the switch in order to obtain the desired value of output voltage. This control signal is generated by amplifying the difference between the actual dc output and the desired dc output and comparing it with a repetitive waveform such as a sawtooth. The block diagram and control signal waveforms are shown in Figures 2-84 and 2-85. The constant frequency,

square-wave output with frequency $1/t$ is sent to the switch. As the output varies from the desired voltage, the duty cycle varies to bring the output voltage back to the desired value. For a PWM supply, the switching frequency is typically a few kilohertz to a few hundred kilohertz. The error typically varies slowly with respect to the switching frequency, so excellent control of the output voltage is maintained.

Thus, it can be seen that by varying the duty cycle of a switch, any desired dc output voltage value can be obtained and controlled. In order to obtain a constant value of output voltage, an L-C filter network is used. No energy is dissipated in these passive elements since the voltage and current are always out of phase by 90 degrees; hence, power-supply efficiency remains unchanged. Also, a diode is added to provide a path for the inductor when the switch is opened. The resulting circuit is shown in Figure 2-86.

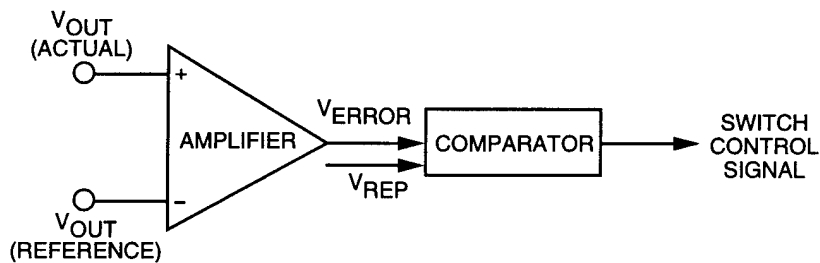


Figure 2-84. PWM control circuit block diagram (Desko, 1991).

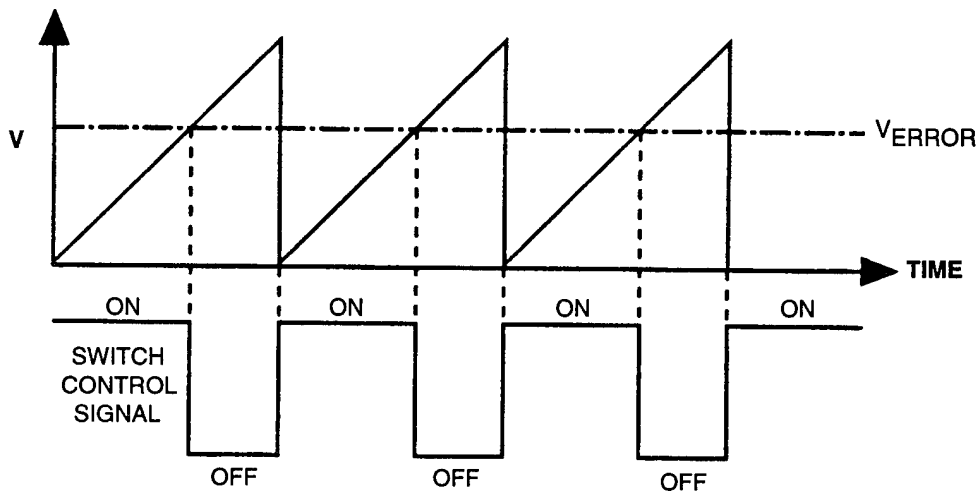


Figure 2-85. Control circuit waveforms (Desko, 1991).

When the switch is ON, the diode becomes reverse-biased and the input supplies energy to the load as well as the inductor. When the switch is OFF, the inductor current flows through the diode, transferring some of its stored energy to the load. Thus, using the fact that in steady state the average voltage across an inductor is zero:

$$(V_{IN} - V_{OUT})(t_{ON}) = (V_{OUT})(t_{OFF}) \quad (2.16)$$

$$\begin{aligned} V_{OUT}/V_{IN} &= t_{ON}/(t_{ON} + t_{OFF}) \\ &= \text{duty cycle} \end{aligned} \quad (2.17)$$

Assuming no power loss, i.e.,

$$(I_{IN})(V_{IN}) = (I_{OUT})(V_{OUT}) \quad (2.18)$$

then

$$I_{OUT}/I_{IN} = 1/\text{duty cycle} \quad (2.19)$$

Thus, for this circuit, the output voltage varies directly with duty cycle while the output current varies inversely with duty cycle.

The circuit configuration of switch, diode, and passive elements is referred to as the circuit topology. The topology shown in Figure 2-86 is known as a buck, or step-down, converter. This topology can only deliver an output voltage that is less than the input voltage. This is one of the two basic converter topologies used for dc-dc converters. The other basic converter topology is the boost, or step-up, converter. All other topologies, and there are many, are either combinations of, or variations on, these two.

As its name implies, the step-up converter can deliver an output voltage that is higher than the input voltage [see Figure 2-87]. When the switch is

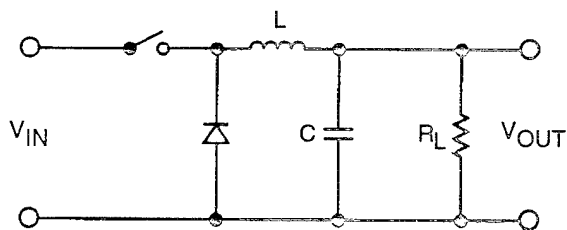


Figure 2-86. Step-down (buck) converter schematic (Desko, 1991).

ON, the diode is reverse-biased, isolating the output stage. The input supplies energy to the inductor. When the switch is OFF, the output stage receives energy from the inductor as well as the input. Once again, since the average voltage across the inductor in steady state is zero:

$$(V_{IN})(t_{ON}) + (V_{IN} - V_{OUT})(t_{OFF}) = 0 \quad (2.20)$$

or

$$V_{OUT}/V_{IN} = 1/(1 - \text{duty cycle}) \quad (2.21)$$

Assuming no power loss in the circuit,

$$(I_{IN})(V_{IN}) = (I_{OUT})(V_{OUT}) \quad (2.22)$$

yielding

$$I_{OUT} = I_{IN}(1 - \text{duty cycle}) \quad (2.23)$$

This topology boosts the voltage and lowers the current.

The discussion thus far has focused on direct dc-dc conversion without isolation. As mentioned earlier, for space and many other applications, isolation of the input and output is essential and is carried out using an isolation transformer. In this type of converter, the high-frequency output from the switch of the basic PWM is applied as an ac input to the primary of an isolation transformer. The ac output from the secondary of the isolation transformer is then rectified and filtered to produce the desired value of output voltage. The added weight of the transformer can be reduced by using as high a switching frequency as possible. The turns ratio, $N_1:N_2$, of the transformer may also be used to step up or step down the output voltage.

Implementing isolation in a step-down converter topology results in the idealized circuit shown in

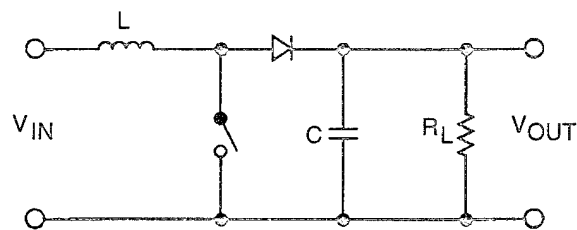


Figure 2-87. Step-up (boost) converter schematic (Desko, 1991).

Figure 2-88. Taking into account the transformer turns ratio for the step-down converter gives

$$V_{OUT}/V_{IN} = (N_2/N_1)(\text{duty cycle}) \quad , \quad (2.24)$$

which is similar to the earlier result for a nonisolated step-down converter. To achieve full isolation in the power supply, the PWM control

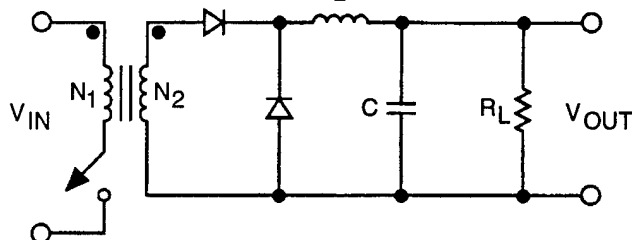


Figure 2-88. Step-down converter with isolation (Desko, 1991).

signal from the secondary side to the primary side must also be isolated. This is accomplished using one or more isolation transformers.

The isolation transformers and the passive elements, capacitors and inductor, comprise most of the volume and weight of the power supply. By going to a higher switching frequency in a PWM power supply, smaller transformers and passive elements can be used, which lower the weight and volume and hence increase the power density of the power supply. For a space system, using the highest frequency possible is desirable in order to achieve high power densities. For a PWM converter, the frequency upper limit is approximately 500 kHz because of the switching losses, which increase linearly with frequency. Above this frequency, the efficiency of the power supply begins to decrease significantly, lowering its overall power density.

All switches experience some switching losses since no switch can turn on or turn off instantaneously. During this switching period, it is possible to have voltage across the switch as well as current flowing through the switch, which results in power dissipation during each switching cycle. As the switching frequency increases, the switching losses increase. However, these switching losses would be insignificant, allowing operation at very high

frequencies, if it were not for the load inductances present in the power supply. The load inductances tend to cause both voltage and current overshoot during switching and to produce a phase shift between the current and voltage waveforms. The inductive load increases the power loss and sets the upper switching limit at approximately 500 kHz. In addition to switching losses, the large current and voltage overshoots and large power dissipation in the switch can severely stress the switch. Additionally, because of the square-wave nature of the switch waveforms, which generate high-frequency harmonics, electromagnetic interference (EMI) can be substantial in a system using a high-frequency PWM power supply. These practical limitations are overcome by using more complex converter topologies. However, these other configurations represent variations of the basic buck or boost topologies.

The implementation of the dc-dc converter requires two distinctly different types of circuit or device technology. One is a device type that can serve as the power switch with two modes of operation: (1) full conduction, passing current with very low power dissipation; and (2) OFF mode, blocking current flow with very low leakage. The second type is a low-signal-level circuit that controls the power switch and provides other required alarm and/or control signals needed for device protection, etc. Each of these device types will be discussed.

2.9.3 Power Semiconductor Devices

In general, it is desirable to use the highest switching speeds possible because of the large weight and volume savings and the resulting increase in power density. Moreover, the megahertz or near-megahertz frequency switching used in these converters requires a high level of performance from the switch in terms of switching speed, in addition to the requirements for high OFF-state breakdown voltage and low ON-state resistance (to reduce conducting losses). The only power semiconductor device that can meet these requirements today is the power MOSFET. By applying a control signal to the power MOSFET gate

terminal, it is possible to realize switching speeds up to 20 MHz, block up to 500 volts in the OFF state, and experience minimal conduction losses in the ON state. In addition, the extremely high impedance of the gate allows for very simple control circuitry.

Many types of power semiconductor devices are used today as switches in power electronics. The list of devices includes (in addition to the power MOSFET): the bipolar junction transistor (BJT), the insulated gate bipolar transistor (IGBT), diodes (both bipolar and Schottky) and thyristor-type devices (four-layer pnpn structures) such as the SCR and the gate turn-off (GTO) thyristor. However, with the exception of the power MOSFET, for one reason or another these devices are inadequate for the task at hand.

The power BJT, developed in the 1950s, is a very mature technology and for many years it was the only power semiconductor device available for high-speed switching. However, the maximum switching speed is only about 50 kHz due to its long turn-on and turn-off times. As mentioned earlier, power is dissipated during these intervals. Above 50 kHz, these transition times become a significant fraction of the switch period and efficiency plummets. Also, the control circuitry is very complex and expensive compared to an MOS device, because a BJT is a current-controlled device and requires large control currents. The IGBT is simply a combination of a MOSFET and a BJT, which allows easier control circuitry. However, switching speeds are even slower than for a BJT.

The SCR and GTO thyristors are inappropriate for the application addressed here. The SCR, somewhat like the diode, is not a fully controllable switch. The SCR can be turned on by a control signal, but it can only be turned off by the action of the circuit in which it is connected. The GTO is fully controllable; however, the currents required for turn-off are very high and switching speed is extremely slow.

The power MOSFET has only been commercially available for power electronics applications since the early 1980s. These devices evolved from

MOS IC technology and were developed in response to the deficiencies of the power BJT. A cross-section view of a discrete n-channel power MOSFET is shown in Figure 2-89. The device structure is referred to as a double-diffused MOS (DMOS) structure because both the p-body and the n⁺ source diffusions are self-aligned with respect to the edge of the polysilicon gate. The symbol for this device is shown in Figure 2-90. It is a three-terminal device consisting of a gate, source, and drain electrode. The gate is composed of polycrystalline silicon or some other refractory material and is separated from the underlying, lightly doped, n-type, single-crystal silicon by an insulating material such as silicon dioxide. The source electrode is connected to both the n⁺- and p-body diffusions, thereby shorting them together. The drain is connected to the n⁺-diffusion on the back side of the silicon. The lightly doped, n-type region between the p-body diffusion and the back-side n⁺-region is known as the drift region. The smallest functioning DMOS structure, shown in Figure 2-89(a), is referred to as a unit cell.

Conduction between the n-type source and drain regions is prevented by the intervening p-type body region when the gate-source electrode voltage V_{GS} is less than the threshold voltage V_T . When a positive voltage greater than the threshold voltage is applied to the gate electrode, an n-type inversion region forms under the gate electrode, allowing conduction between the n-type source and drain regions [see Figure 2-89(a)]. Hence, switching occurs by applying a control signal to the gate electrode. Since the gate is insulated from the underlying silicon, the control signal is basically a bias voltage with no steady-state current flow. However, some current must be supplied to the gate to charge and discharge the input gate capacitance during switching. In the OFF state, with zero gate bias ($V_{GS} = 0$), this device can support a large positive drain-to-source voltage, V_{DS} , which is supported by the reverse-biased n-/p-body diode [see Figure 2-89(b)]. The maximum blocking voltage is determined by the breakdown voltage of this diode and, to first order, depends on the doping level of the drift region — the lighter the doping,

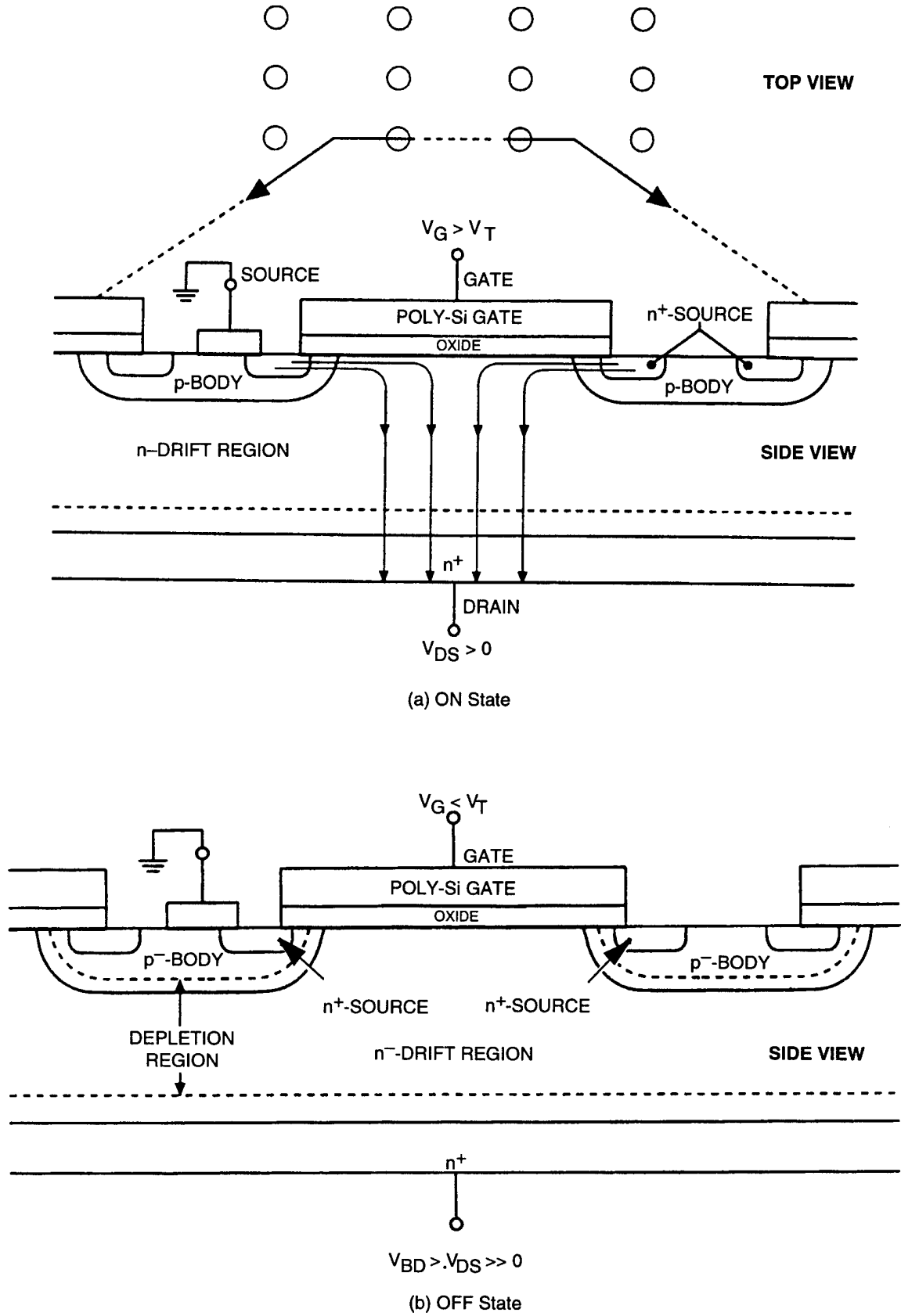


Figure 2-89. Cross section of a double-diffused MOS (DMOS) structure (Desko, 1991).

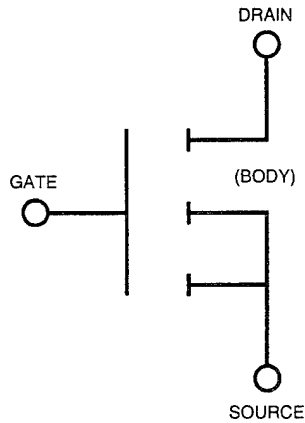


Figure 2-90. Symbol for a DMOS device (Desko, 1991).

the higher the breakdown voltage. In the ON state, with $V_{GS} > V_T$ and $V_{DS} > 0$, a current appears at the drain electrode. ON-state conduction losses occur because of the finite resistance R_{ON} between the drain and source, arising primarily from the lightly doped drift region. To reduce the drain-source resistance, the drift region is usually made as thin as possible, which is usually the n-/p-body depletion width at the rated breakdown voltage plus some safety factor. Further reductions in R_{ON} require increased device area. The I-V characteristics for a power MOSFET or DMOS are shown in Figures 2-91 and 2-92. The threshold voltage, above which the device is turned on, is typically 2 to 5 volts.

2.9.4 Power Integrated Circuits

As mentioned, additional circuitry is required to control the switching cycle or frequency of the switch in order to maintain the output voltage at the required level. The circuit blocks required for this include operational amplifiers (op-amps), comparators, timing logic, drivers, inverters, oscillators, and others; the list is extensive. A block diagram illustrating one particular control circuit architecture is shown in Figure 2-93. The control signal is generated on the secondary side, using the amplified error signal, and sent across an isolation transformer to the driver circuit, which then turns the switch on and off.

The control circuit shown in Figure 2-93 was designed to generate a variable-frequency control

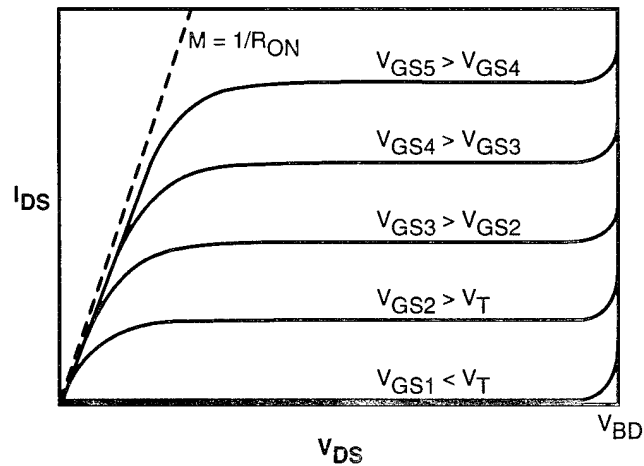


Figure 2-91. DMOS output characteristics (Desko, 1991).

signal for a resonant converter. The dc output voltage and reference voltage pass through an error amplifier. The output is inverted and then converted from a voltage signal to a current signal. This signal then passes through a monostable multivibrator where a digital control signal is generated. The digital signal passes across an isolation transformer to some timing logic and then on to an additional monostable oscillator where the final gate control signal is generated. This control signal is then routed to the power MOSFET gate through a driver circuit. The driver circuit is necessary to charge and discharge the gate capacitance during each switching cycle. The monostable oscillator shown in the figure is used to generate feedback to the secondary side. This circuit requires two additional small isolation transformers. This

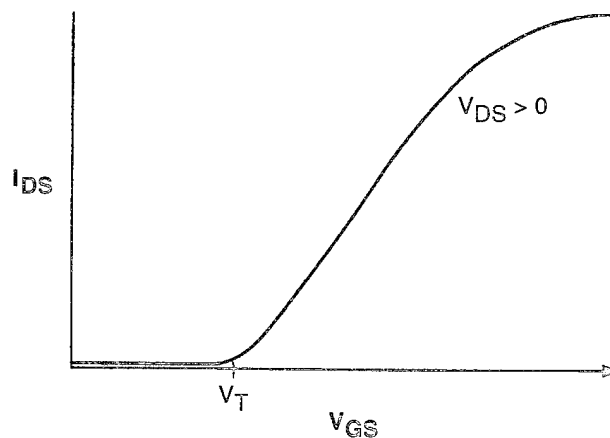


Figure 2-92. DMOS transfer characteristics (transconductance) (Desko, 1991).

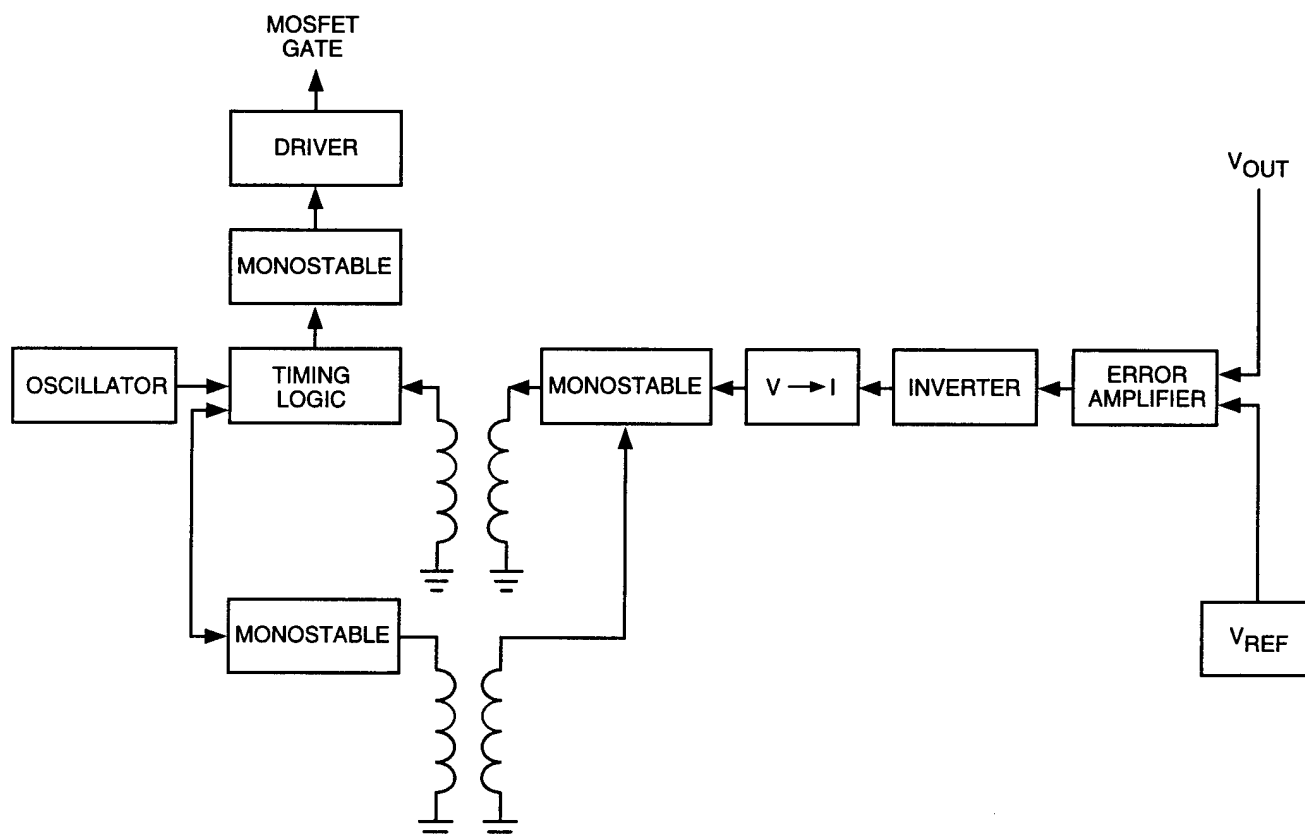


Figure 2-93. Resonant converter control circuit (Desko, 1991).

control circuit is a simplified version of a control circuit designed for space applications. The number of circuit blocks shown are only a fraction of the number actually used. Additional circuit blocks are needed to protect the power supply from a variety of conditions that could damage it.

Although the control circuit and power device (switch) can be implemented using a separate IC chip for each function, a significant penalty in added weight, volume, and power consumption, as well as a reduction in reliability, will be accrued using this approach. Thus, a class of ICs known as "smart-power" ICs (or PICs) that integrates all of the required functions has been developed. Since PIC technology requires the integration of power MOS (DMOS) devices with CMOS, BJT, zener diodes, and resistors, PICs are considered separately for this discussion. In addition, the integration of a DMOS device on a single chip with CMOS and BJT devices requires, in almost all cases, that the terminals of the power device be accessible on one side of the chip. Thus, for such

an application the DMOS configuration shown in Figure 2-89(a) is unsuitable. However, several alternate configurations exist.

One approach uses a lateral drift region instead of the vertical drift region to electrically isolate this high-voltage device from the other devices using junction isolation (JI). Cross sections of two possible lateral DMOS structures are shown in Figure 2-94. The long lateral drift region supports the voltage in the OFF state. The lightly doped p-type substrate used for these structures is fully compatible with the current practice of using p-type starting wafers for very-large-scale ICs (VLSICs). The main drawback of this approach is that for high-voltage applications, a large amount of area is taken solely for the purpose of electrically isolating devices.

Another approach utilized is dielectric isolation (DI), wherein a buried, wrap-around region allows the drain region to be contacted on the silicon top surface [see Figure 2-95]. Devices are thereby electrically isolated from each other by the buried-

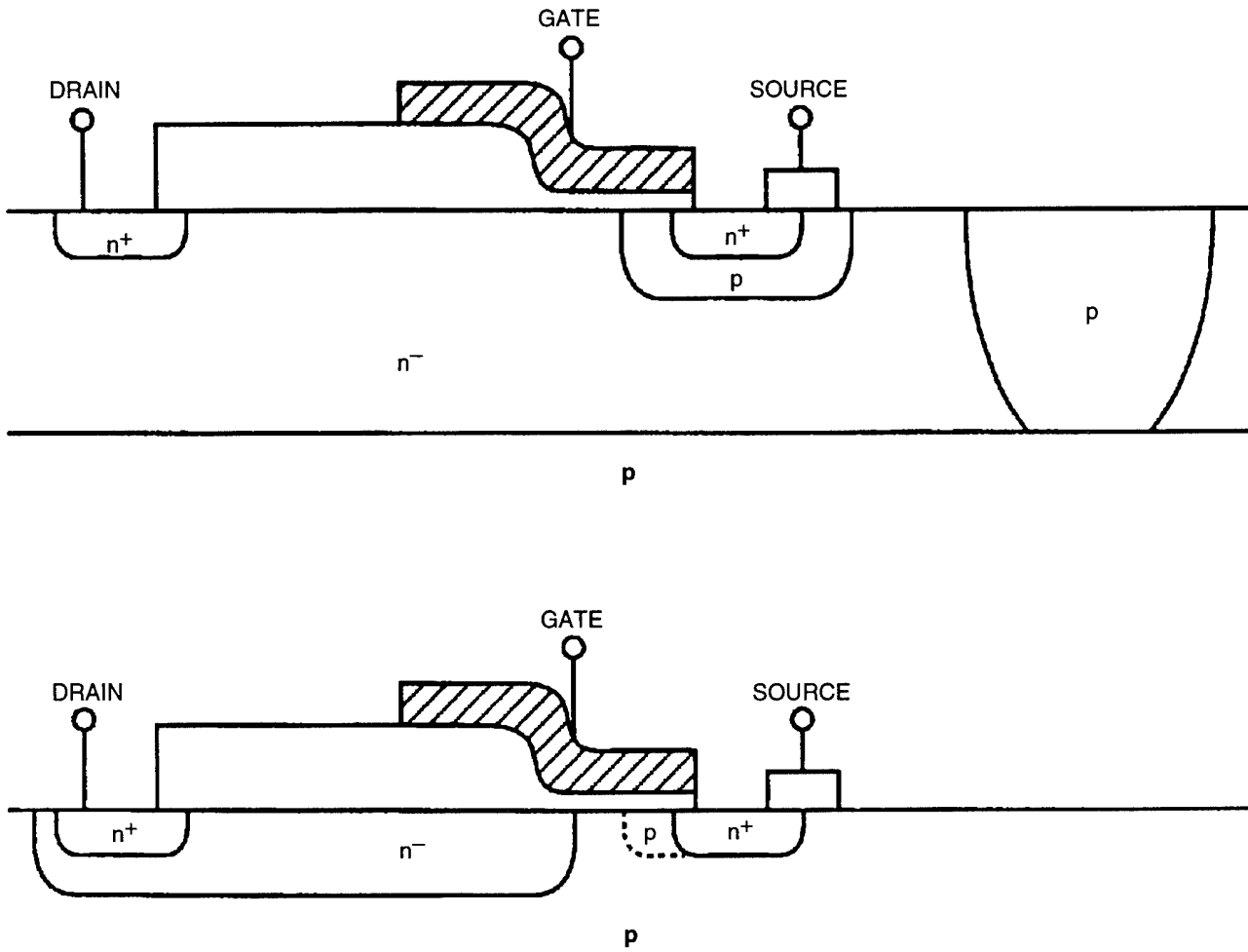


Figure 2-94. Cross section of two lateral DMOS structures employing junction isolation (Desko, 1991).

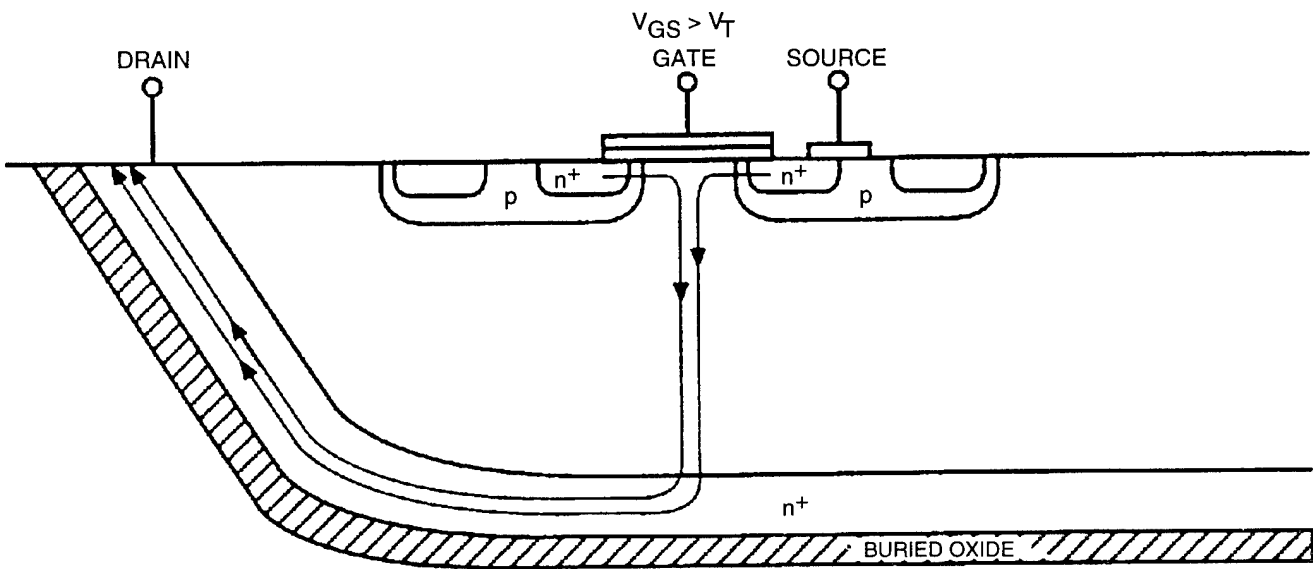


Figure 2-95. Cross section of a lateral DMOS employing dielectric isolation (Desko, 1991).

oxide layer. While this approach is more area-efficient at higher voltages, it is very inefficient at lower voltages.

Additional costs are incurred due to the added wafer-processing needed to form the DI substrate. Dielectric isolation is advantageous in radiation environments because it prevents latchup. Neither the JI or DI approach can match the low R_{ON} achieved using discrete devices; however, the ability to integrate all the components into a single IC may more than compensate for this deficiency in most applications.

A cross section of a PIC employing DMOS, CMOS, BJT, and diode circuits is shown in Figure 2-96. Although these alternate structures permit the integration of DMOS and low-power devices, e.g., CMOS, BJTs, diodes, etc., stringent design and

processing requirements result due to conflicting fabrication requirements. Moreover, these fabrication issues are exacerbated when designing for radiation hardness.

2.9.5 Radiation Effects and Hardening Strategies

Radiation-hardened semiconductor devices suitable for space-system applications are available from a number of manufacturers. However, at the present time, a monolithic radiation-hardened PIC is not yet available.

The effects of radiation on DMOS devices and the various other semiconductor devices associated with PICs are shown in Table 2-5.

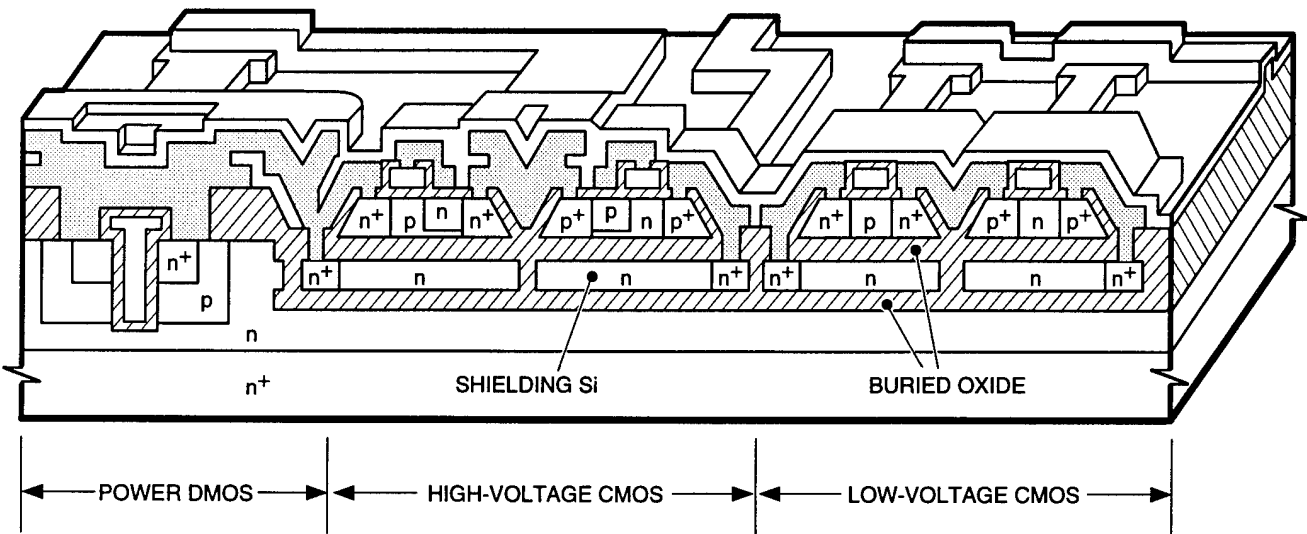


Figure 2-96. Smart power IC (PIC) cross section using DMOS, CMOS, BJT, and diode circuits (Desko, 1991).

Table 2-5. The effect of critical radiation environments on devices.

Environment	Device					
	DMOS		CMOS		BJT	
	Major Effect	Lesser Effect	Major Effect	Lesser Effect	Major Effect	Lesser Effect
Ionizing radiation dose	X		X			X
Neutrons	X			X	X	
Single-event upset	X			X		X
Dose-rate upset	X			X		X

2.9.5.1 CMOS and BJT Devices

The effects of the various radiation environments on low-voltage CMOS and bipolar devices and ICs are fairly well documented. Special procedures have been developed both in device and chip design and in wafer fabrication that can harden a device or IC chip to these critical radiation environments.

For CMOS devices, the critical radiation environment is ionizing radiation dose, which can lead to large changes in threshold voltage, resulting in the n-channel device turning on at zero gate voltage. The mechanism for this is the buildup of positive charge in the oxide under gate bias. The procedure used to prevent this is to use as thin a radiation-hardened gate oxide as possible, since the threshold voltage shift varies with at least the square of gate thickness, using low-temperature processing following gate oxidation. In practice, oxide thicknesses are kept below 250Å and subsequent process conditions are kept at 850°C or less. The oxidation growth temperature and ambient have also been shown to play a role in reducing the threshold voltage shift.

For BJTs, ionizing radiation can cause surface inversion in the base region, which can lead to emitter-to-collector leakage and gain degradation due to surface recombination effects. These problems can be ameliorated through the use of hardened field oxides.

2.9.5.2 DMOS Devices

For DMOS devices, all environments produce major effects. Ionizing radiation dose alone results in four major deleterious effects: threshold voltage shift, rebound (or super-recovery), breakdown voltage shift, and mobility reduction. Each of these four effects is examined below.

The power MOSFET is susceptible to threshold voltage shifts due to the buildup of charge in the gate oxide. However, it is not possible (as it is in the case of CMOS devices) to use very thin gate oxides to reduce this effect. Using such thin oxides can lead to gate rupture in a space SEU environment due to the presence of energetic heavy ions.

Also, thinning the gate oxide can result in a reduction of reliability due to gate oxide breakdown. Consequently, gate oxides are kept between 500Å and 1,000Å. Since this relatively thick gate oxide results in a large threshold voltage shift, the threshold voltage must be set higher initially, which can lead to a reduction in drive current for the device. The buildup of interface states during ionizing radiation dose lowers the carrier mobility, which results in an increase in the resistance of the device in the ON state, R_{ON} . This increase results in additional power dissipation in the switch, which lowers the dc-dc converter efficiency. Because a large reduction in oxide thickness to reduce this effect is not possible, the only way to compensate for this effect is to derate the ON resistance of the device, which results in a larger device than would otherwise be necessary in order to meet the ON resistance specifications of the device.

The thick oxides used for the DMOS device can also result in a serious rebound problem. Rebound, or super-recovery, refers to the annealing out of oxide charge while interface states continue to either increase or remain constant over time. The net result is that the threshold voltage for n-channel transistors rebounds to higher than initial values, which further lowers the device drive current.

These three effects (threshold voltage reduction, mobility degradation, and rebound) are illustrated in Figures 2-97 through 2-99 for a 700Å, hardened gate oxide. Figure 2-97 shows the effect of increasing ionizing radiation dose on the device transfer curve, or transconductance. The curves shift to the left, in a parallel manner at lower doses, indicating the buildup of oxide traps. As irradiation continues, the buildup of interface states lowers device mobility and the curves are seen to change slope. The change in threshold voltage as a function of ionizing radiation dose is plotted in Figure 2-98. The effect of rebound is shown in Figure 2-99, where curves are seen to begin shifting to the right.

The fourth potential ionizing radiation dose effect for DMOS devices is the reduction in breakdown voltage. This effect results from the buildup

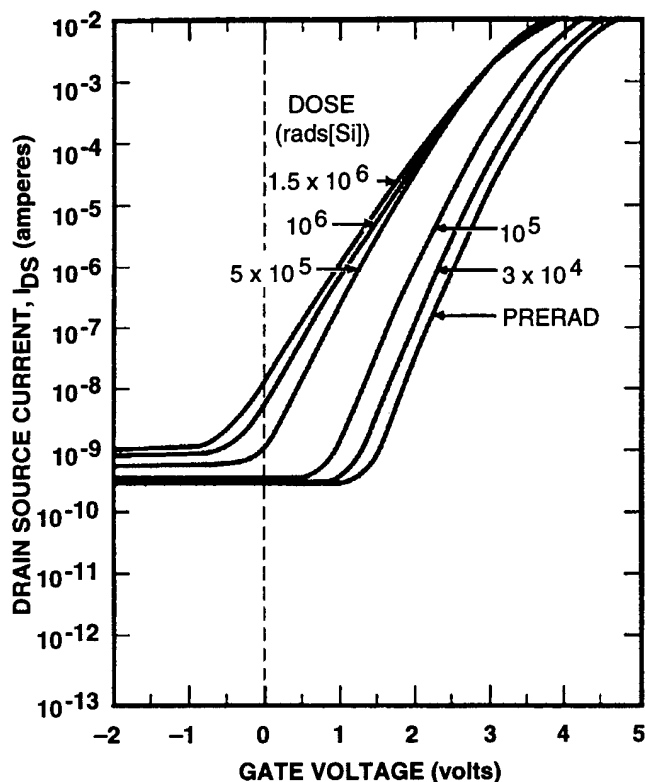


Figure 2-97. Effect of ionizing radiation dose on DMOS (80-cell) transconductance; dose rate = 1.11×10^5 rads (SiO_2)/min, $V_{DS} = 10$ volts (Desko, 1991).

of positive charge in the thick field oxide used in the termination region of the device. This termination region is necessary for a smooth transition in voltage across the silicon surface region at the edges of the device. The termination region of a device using field-shield termination is shown in Figure 2-100 with the accompanying electric field lines. The oxide charge can change the electric field distribution in this region and lower the device breakdown voltage. Preventing this problem requires using a hardened field oxide or a ring termination structure.

2.10 Nonvolatile Memory Technology

Nonvolatile memories, i.e., memories that retain information in the absence of applied power, are widely used in a variety of military and commercial systems to retain critical information (such as codes or passwords, system configurations, operating systems, look-up tables, baseline data, etc.) that must be preserved despite the loss of sys-

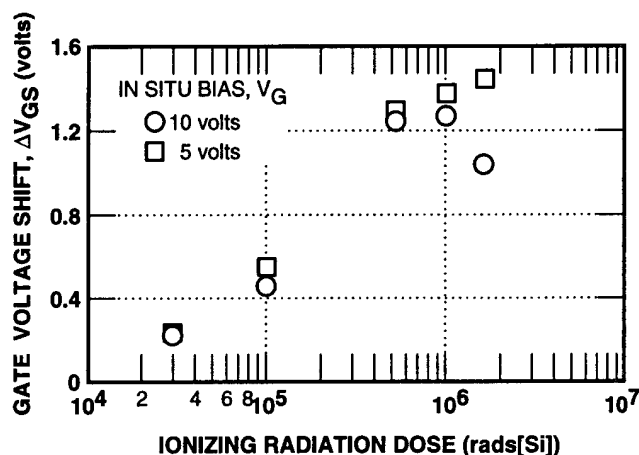


Figure 2-98. Effect of ionizing radiation dose on DMOS (80-cell) threshold voltage; dose rate = 1.11×10^5 rads (SiO_2)/min, $V_{DS} = 10$ volts, $I_{DS} = 10$ mA (Desko, 1991).

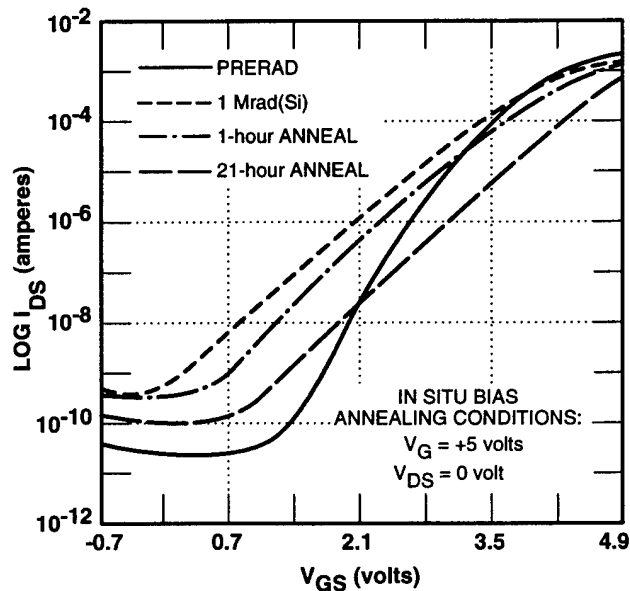


Figure 2-99. Rebound effect demonstrated on an 80-cell DMOS subjected to 1 Mrad(Si) ionizing radiation dose and the effects of annealing; dose rate = 179 rads(Si)/sec, $V_{DS} = 0.1$ volt, anneal temperature = 150°C (Desko, 1991).

tem power (Dressendorfer, 1991). An example of the widespread use of nonvolatile memories is shown in Figure 2-101. In addition, many of these systems must operate in natural space and/or weapon-produced nuclear environments.

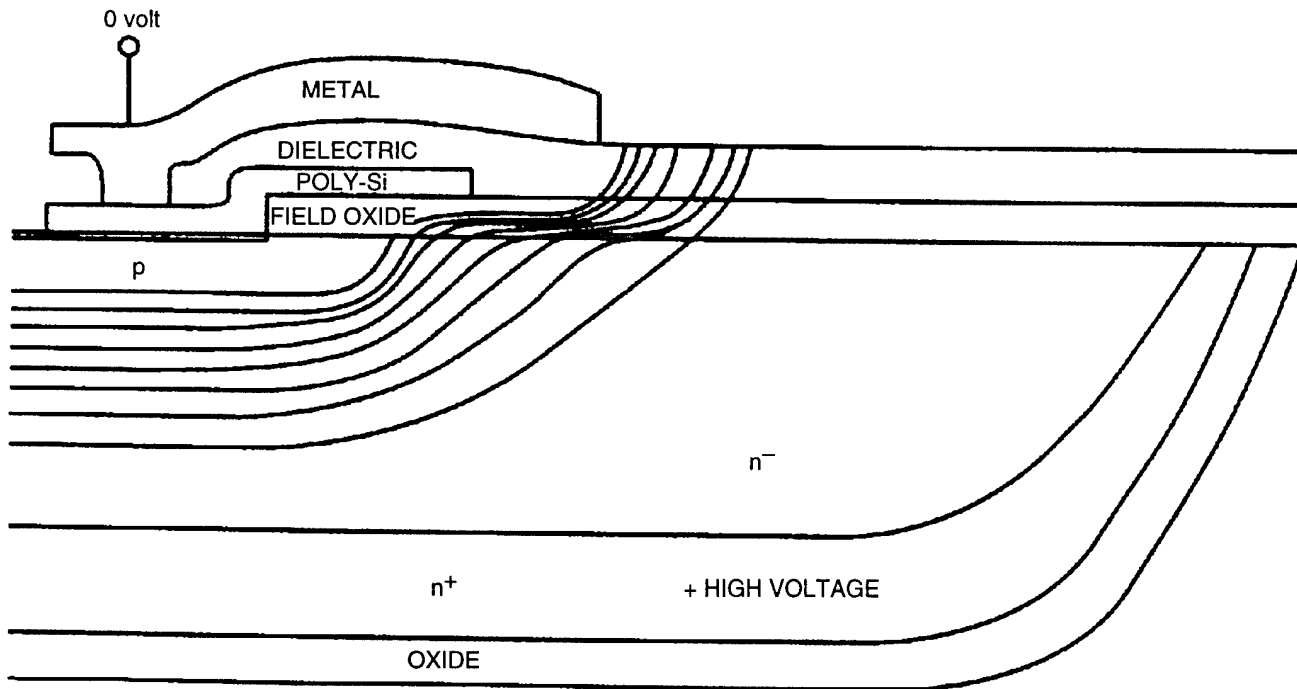


Figure 2-100. High-voltage device termination structure (field shield) (Desko, 1991).

The many different nonvolatile memory technologies, each with its own specific electrical and radiation performance characteristics, are briefly described below:

- **Programmable Read-Only Memory (PROM).** A device that may be programmed once after the completion of its fabrication, and then subsequently read a large number of times. The programming is usually performed electrically by “blowing” fuse links to imprint the appropriate information into the memory.
- **Electrically Erasable Programmable Read-Only Memory (EEPROM)** A device in which both the erase and programming functions can be performed electrically in a relatively straightforward manner. This name has been traditionally associated with floating-gate and silicon-nitride-oxide-semiconductor (SNOS) devices, rather than being a generic description of all memories with the characteristic of electrical erase and programming.
- **One-Time Programmable, Erasable Programmable Read-Only Memory (OTP EPROM).** A UVEPROM that is packaged in plastic (without a transparent window). Because of this packaging difference, it is less expensive than an EPROM, but cannot be erased.
- **Erasable Programmable Read-Only Memory (EPROM).** A device that can be programmed after manufacture and then erased and rewritten with new information, as desired. In ultraviolet EPROMs (UVEPROMs), erasure is accomplished by exposing the device to ultraviolet light for several minutes; rewriting the device is then done electrically. This erasure process is generally

cumbersome and time consuming; thus, this device is not suitable for applications requiring frequent alterations of the stored information.

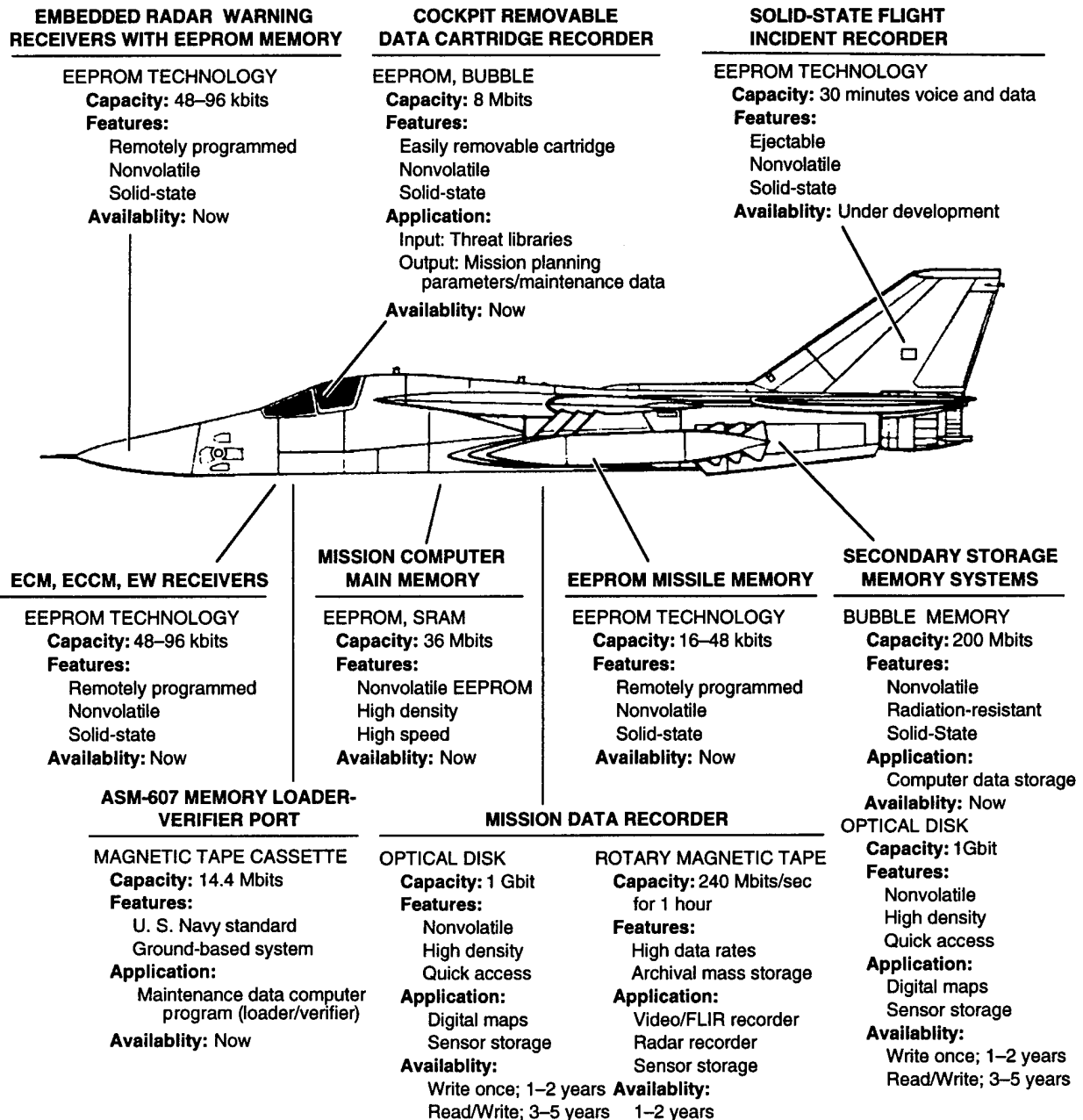


Figure 2-101. Examples of nonvolatile memory technology usage in a military aircraft (Fedorak, 1989).

- **Ferroelectric Technology.** A device which utilizes the hysteresis properties of ferroelectric material to store information.
- **Plated Wire and Magnetic Core Technology.** Plated wire technology utilizes magnetic coating on small wires to store information as the direction of magnetization. Magnetic core technology simi-

larly stores information as the direction of magnetization, but in a small toroid of magnetic material. These technologies tend to have low density (on the scale of integrated circuits) and are not compatible with IC processing.

- **Magnetic Bubble Technology.** Memories use a magnetic material in which “bubbles” (localized regions of reverse

magnetization) are used to store information. Although the processing of these devices uses many of the techniques of IC processing, they cannot be easily integrated on the same substrate as standard IC transistors.

- **Magnetic Tape and Disks.** Store information as localized regions of reversed magnetic field. They require mechanical devices in order to locate and access information.
- **Optical Disks.** Utilize a change in optical properties to store information.
- **Battery-Backed Static Random Access Memory (SRAM).** This is not a true nonvolatile memory technology, since the SRAM does require the uninterrupted application of power in order to retain information. However, in these devices this uninterrupted power is supplied by a battery that is made part of the device subsystem; hence, from the system perspective, power does not have to be continuously applied. For a number of applications, this is a viable means of achieving nonvolatile operation with SRAM performance.

Terminology unique to the context of nonvolatile memory technology is listed below (Dressendorfer, 1991):

- *Retention.* The length of time that the information can be retained correctly, particularly under worst-case storage conditions, e.g., unpowered, high-temperature, etc.
- *Endurance.* The number of times a device may be written, erased, and rewritten and still function properly as a nonvolatile memory.
- *Program or Write Time.* The time necessary to write information into the memory.
- *Read Time.* The time necessary to read information from the memory.
- *Erase Time.* The time necessary to erase information from the memory (often the same as write time, but may be different for some nonvolatile memory devices or architectures).
- *Write/Erase/Read Voltage.* The voltage necessary to perform the write, erase, or read functions.

This section discusses the ionizing radiation dose characteristics only for EPROM and EEPROM (both floating gate and SNOS), ferroelectric, and one type of thin-film magnetic nonvolatile memories. The technologies omitted from this discussion obtain their nonvolatility from the permanent alteration of a structure by the opening of fuse links (except battery-backed nonvolatile memory). Thus, the radiation performance of such a device is wholly based on the performance of peripheral circuits and is covered in Chapter 5. Battery-backed nonvolatile memory performance is governed by the radiation response of the SRAM being used; thus, this information is covered in Sections 2.4 and 2.5 (MOS technology devices).

The various technologies and their applications can be placed in perspective by viewing nonvolatile memories as existing in two hierarchies: (1) reprogramming ease [Figure 2-102], and (2) data recovery speed [Figure 2-103]. The implication of Figure 2-103 is that the technologies selected for primary storage are capable of faster operation than secondary memory, etc. In addition to these two factors, other considerations for the selection of a particular technology include radiation performance, integration density, endurance, retention, power consumption, weight, size and cost.

A summary of the advantages and disadvantages of several technologies that are being considered for space strategic application is shown in Table 2-6. From this table, the difficulty in selecting the optimum technology for a specific application can be understood. Figures 2-104 through 2-106 are provided to summarize solid-state nonvolatile

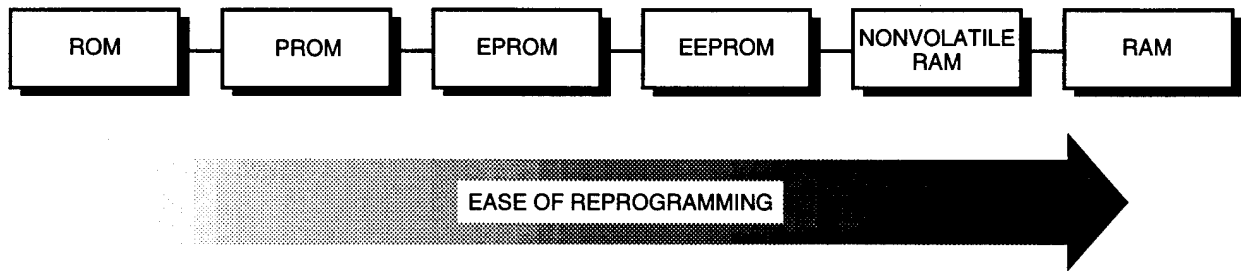


Figure 2-102. Reprogramming ease hierarchy for solid-state memory devices (Fedorak, 1989).

technologies to support Table 2-6. Note that the ferroelectric technology, which displays excellent endurance and speed, is also deemed extremely immature, thus precluding an easy selection for a specific application. Moreover, this technology selection problem does not reflect the added constraint of radiation hardness.

2.10.1 Floating-Gate Erasable Programmable Read-Only Memory

A typical floating-gate EPROM (FG EPROM) cell is shown in Figure 2-107. The dielectric under the floating gate is silicon dioxide of ~200Å thickness. The dielectric between the floating and con-

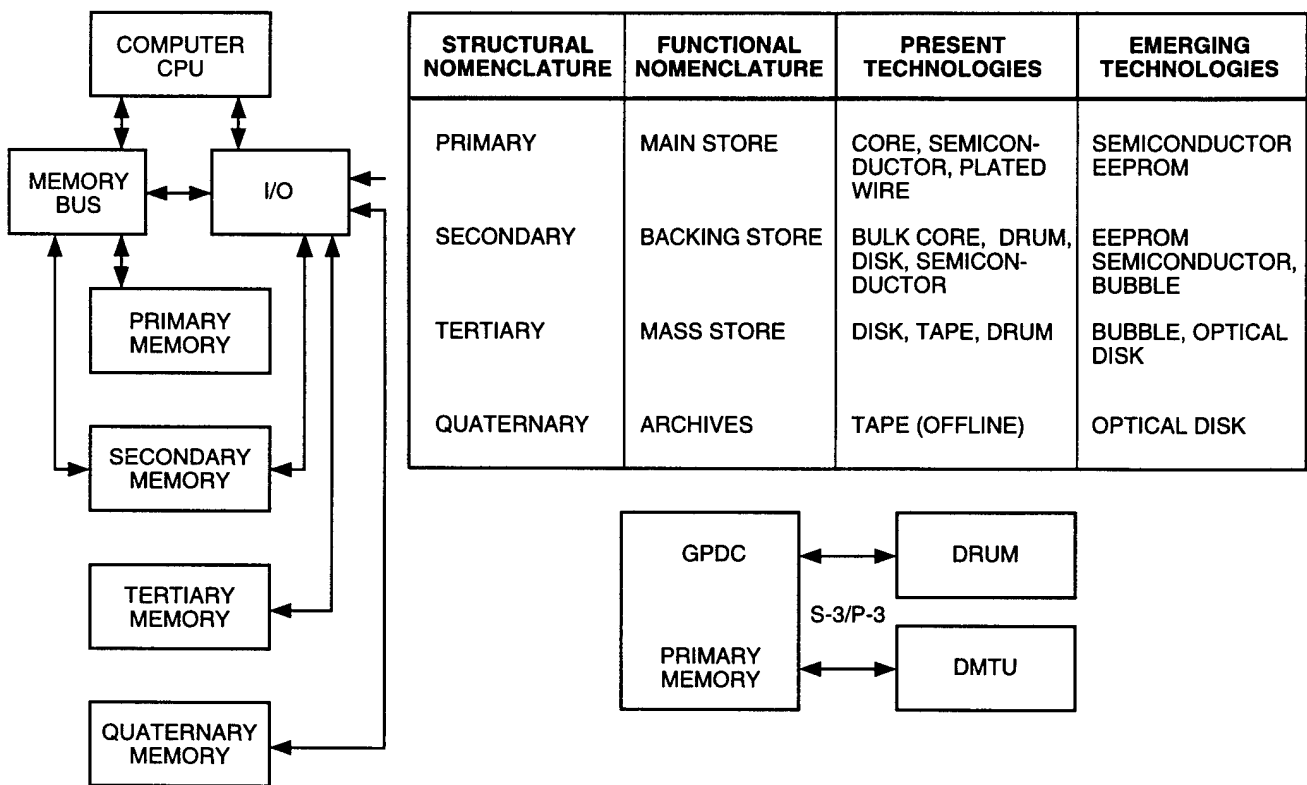


Figure 2-103. Computer memory hierarchy: data recovery speed (Fedorak, 1989).

Table 2-6. Summary of potential nonvolatile technologies (Kuehl, 1990).

Technology	Advantages	Disadvantages
ROM, PROM	High speed, high density, excellent radiation hardness	Cannot be rewritten
EEPROM/MNOS ^a (Westinghouse, Sandia)	High density, fast read time	Wear out, slow write time; susceptible to burnout
Thin-film plated wire ^a (Honeywell)	High speed, moderate density, excellent radiation hardness	Limited density (2K to 4K)
Magnetoresistive ^a (Honeywell)	Speed trades with density, good potential hardness	Immature sensing technology; data retention at high dose rates is an issue
Ferroelectric ^a (Ramtron)potential hardness	High speed, high density, good	Long-term wear-out & materials issues
Plated wire ^b	Moderate speed, excellent radiation hardness, expensive	Very low density (high volume, weight)
Core ^b	Moderate speed and density, excellent radiation hardness	Inefficient for small memories, expensive
Magnetic bubble ^b	Very high density	Very slow, vulnerable to transient radiation-induced data loss during access

Notes:

^a Immature technology.

^b Not monolithic.

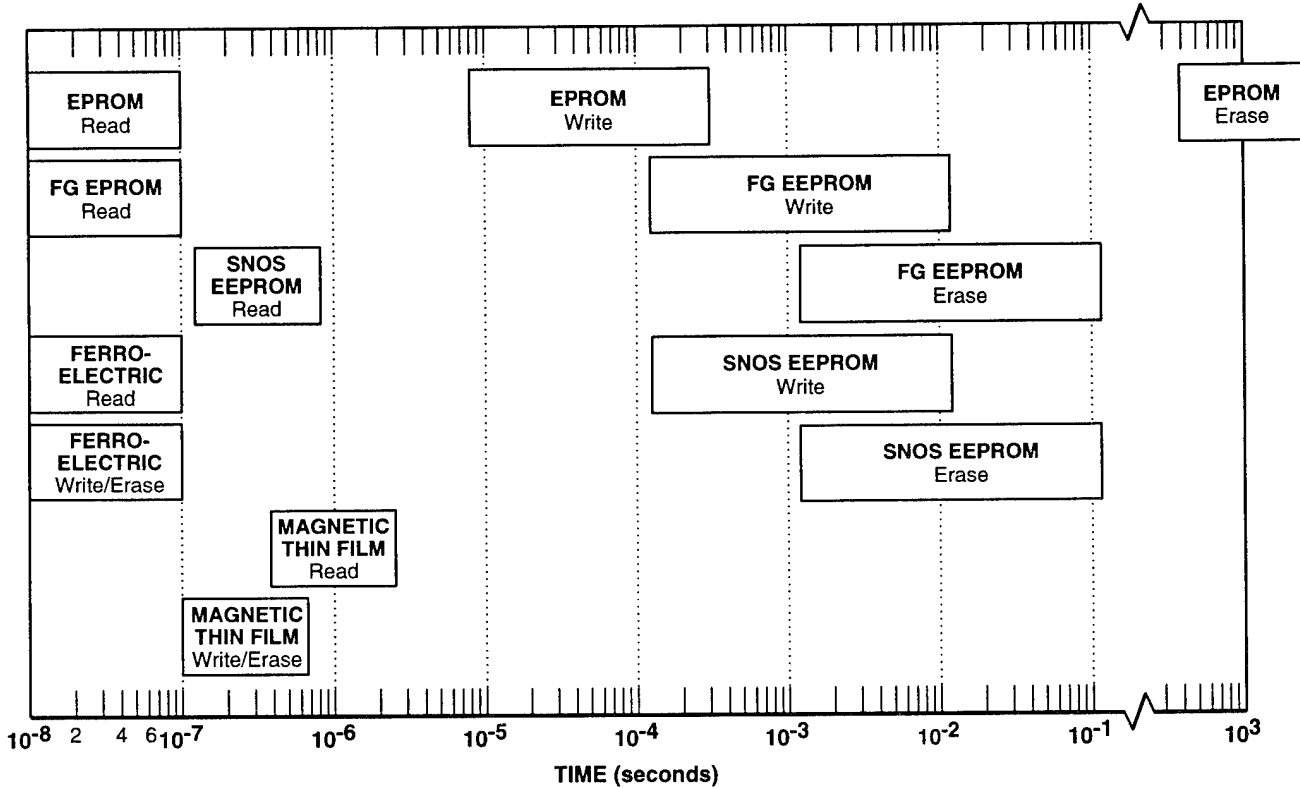


Figure 2-104. Typical performance characteristics of solid-state electronic nonvolatile memory technologies (Schwee, 1990).

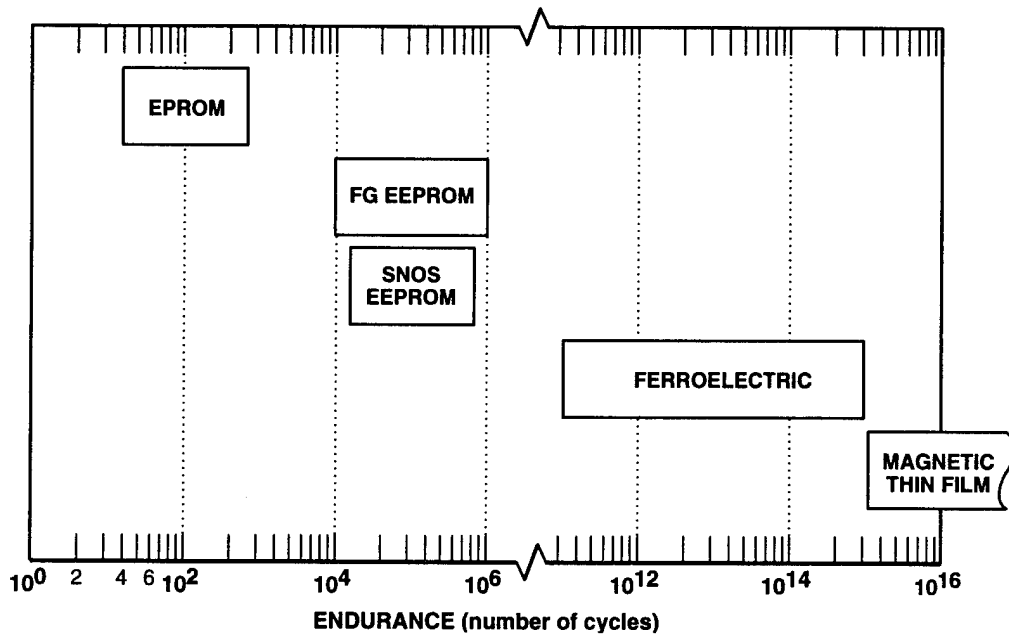


Figure 2-105. Typical endurance characteristics of solid-state electronic nonvolatile memory technologies (Schwee, 1990).

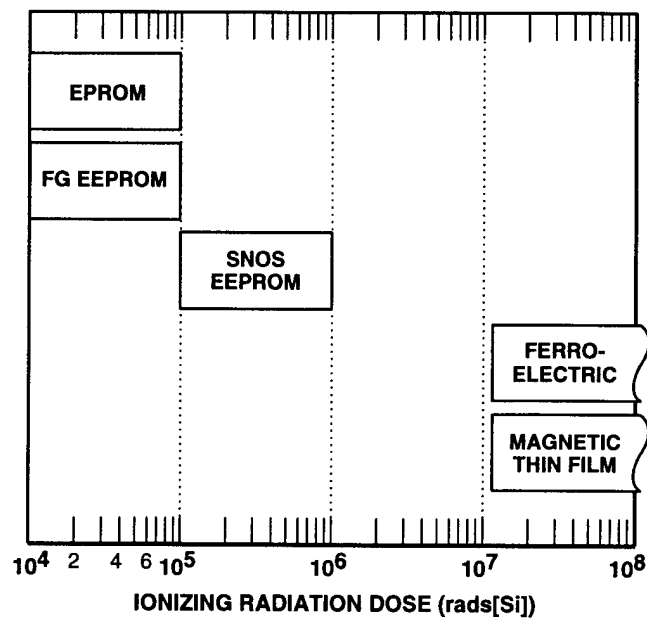


Figure 2-106. Ionizing radiation dose hardness of nonvolatile memory elements for solid-state electronic memory technologies (Schwee, 1990).

control gates can be either silicon dioxide or another dielectric (such as silicon nitride), usually about 200Å to 400Å thick. Programming is performed using channel hot-electron injection. A large positive voltage is applied to the control gate (~12 volts) with a relatively high voltage (~8 to 9 volts) applied to the drain (bit line). Source and substrate are held at ground potential. Electrons in the channel are accelerated by the high field near the drain where some acquire enough energy to surmount the Si/SiO₂ barrier and are attracted to the floating gate. Erasure is performed by illumination with UV light (with photon energy >4 eV), which photoinjects electrons over the Si/SiO₂ barrier at the floating gate where they are subsequently collected, either at the top control electrode or the silicon substrate. Programming results in a threshold voltage >5 volts for the control gate.

Erasure by UV light results in threshold voltage of ~1.5 volts. During read, the control gate is held at 5 volts, and the bit line is precharged to 1 to 2 volts. A "0" in the cell allows current to flow through the cell, pulling down the bit line, whereas a "1" ($V_T > 5$ volts) does not allow current to flow.

This difference can be detected by the sense amplifier. Since the voltage configuration is the same during read and programming, read-disturb problems are avoided by having a significant difference in voltage levels for these two operations.

Since floating gate devices can be erased by ultraviolet illumination, it is expected that they will also be erased in an ionizing radiation environment. An example of the threshold voltage shifts observed with ionizing radiation is shown in Figure 2-108 [comparison with model calculations are also shown]. The memory window is seen to change appreciably at 10^4 rads(Si), and almost completely collapses by 10^5 rads(Si). Thus, with suitably hardened peripheral circuitry, a floating-gate memory cell could support nonvolatile operation to this level.

2.10.2 Floating-Gate Electrically Erasable Programmable Read-Only Memory

A typical floating-gate EEPROM (FG EEPROM) transistor is shown in Figure 2-109, with a thin tunneling dielectric (silicon oxide or

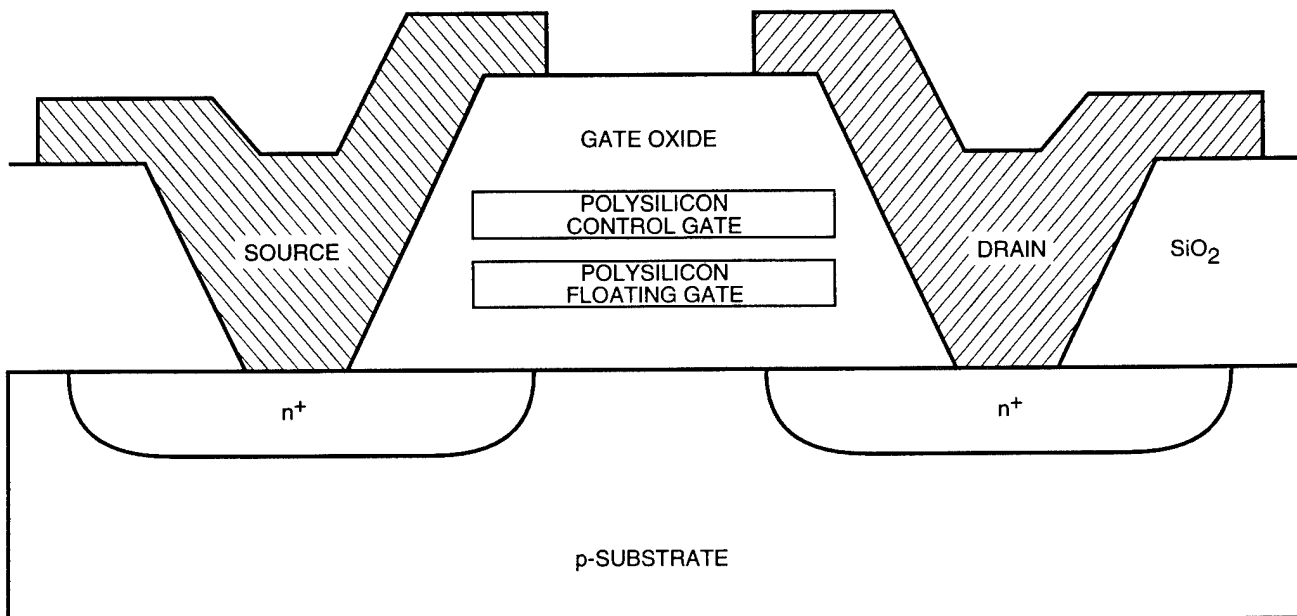


Figure 2-107. Cross section of a typical EPROM floating-gate transistor (Dressendorfer, 1991).

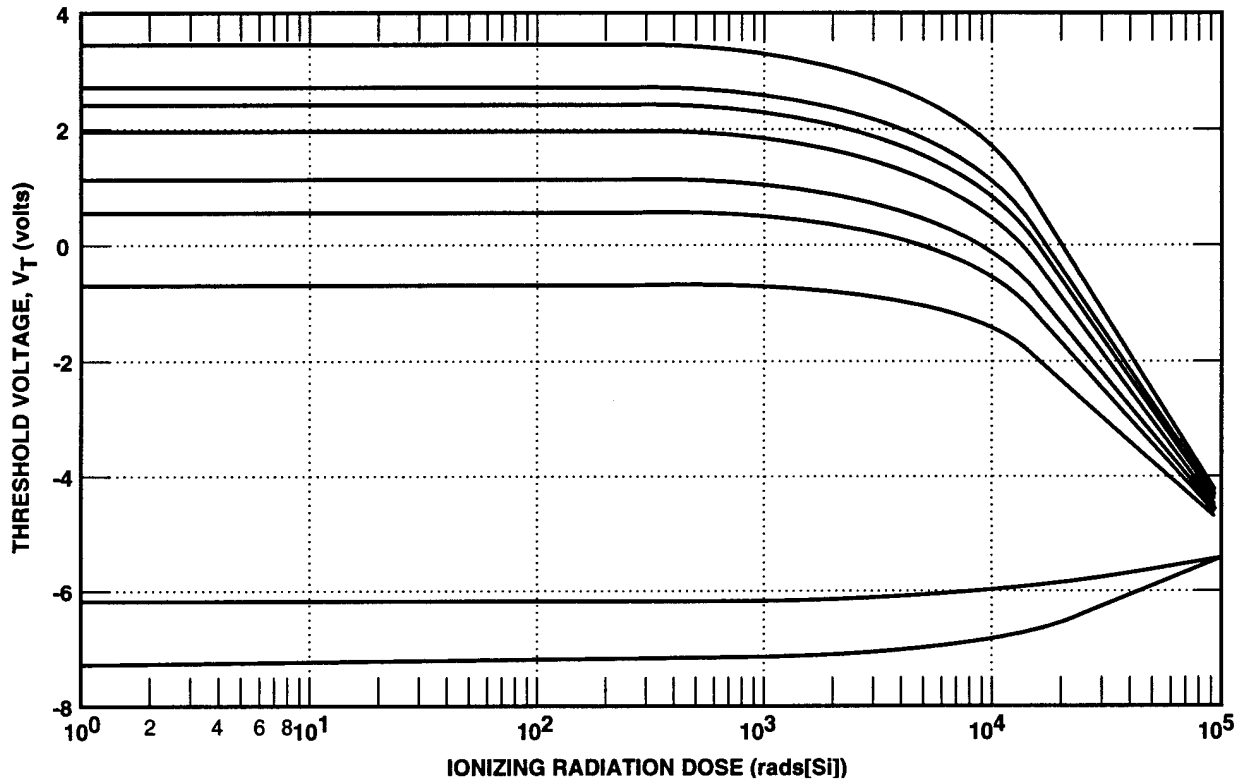


Figure 2-108. Threshold voltage shifts of a floating-gate transistor as a function of ionizing dose for transistors programmed with different initial threshold voltages (Snyder *et al.*, 1989).

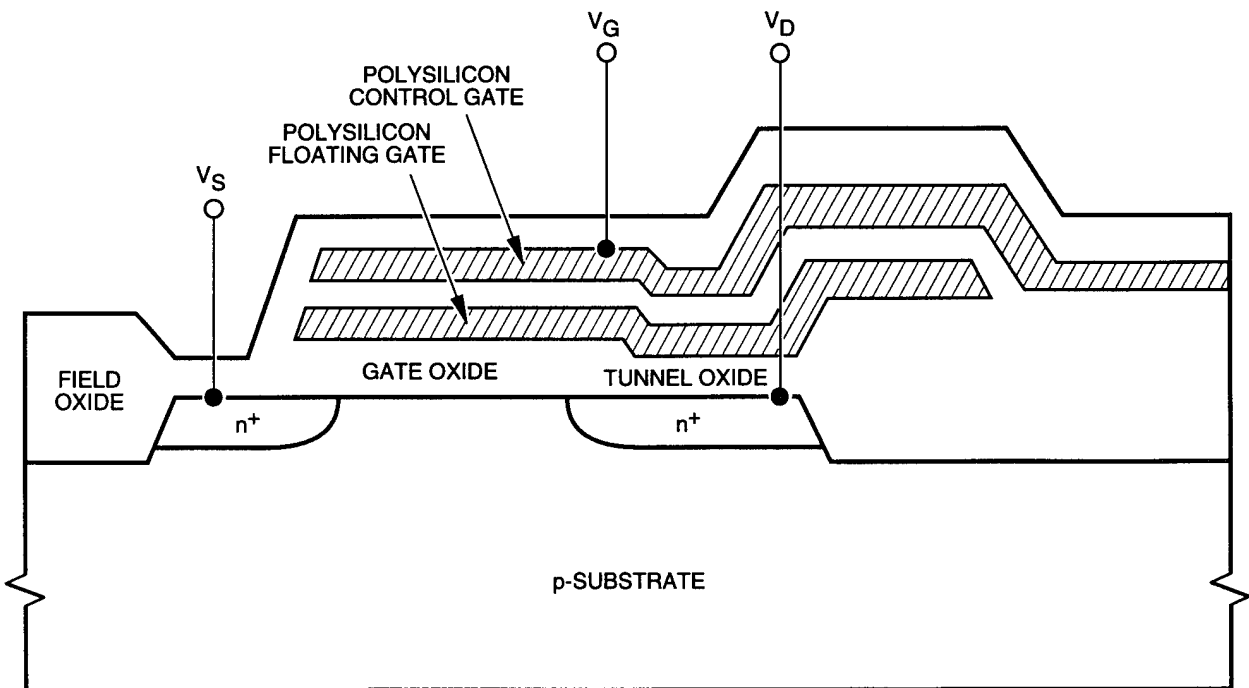


Figure 2-109. Cross section of a typical EEPROM floating-gate transistor (Dressendorfer, 1991).

silicon oxynitride, typically 80Å to 100Å thick) grown over the drain region.

Programming is achieved by applying a high positive voltage (typically 16 to 20 volts) to the gate, and grounding the source, drain and substrate; Fowler-Nordheim tunneling occurs between the drain and the floating gate. Erasure is achieved by grounding the gate and applying a high positive voltage to the drain.

A full-featured EEPROM memory cell is more complicated than that of an EPROM. A representative example of an array of floating-gate tunnel oxide (FLOTOX) cells for a byte architecture is shown in Figure 2-110. During programming, the word line and program line of the selected cell are brought to a high voltage (~20 volts), and the bit line is held at zero. During erase, the word line and

bit line of the selected cell are brought to a high voltage, and the program line is held at zero. During read, the word line of the selected cell is brought to 5 volts, the program line is held at a reference voltage, and the bit line is precharged to ~2 volts. The threshold voltage of the selected memory transistor relative to the reference voltage determines whether current will flow and discharge the bit line. The drain isolation transistors prevent disturbing unselected transistors on the same bit lines as the selected cell (read disturb) and are used to select the appropriate transistor during the read operation. The gate isolation transistor allows selection of a particular byte during read of a given set of bit lines. The ionizing radiation dose response of an EEPROM is similar to that of an EPROM since both share a common operating methodology.

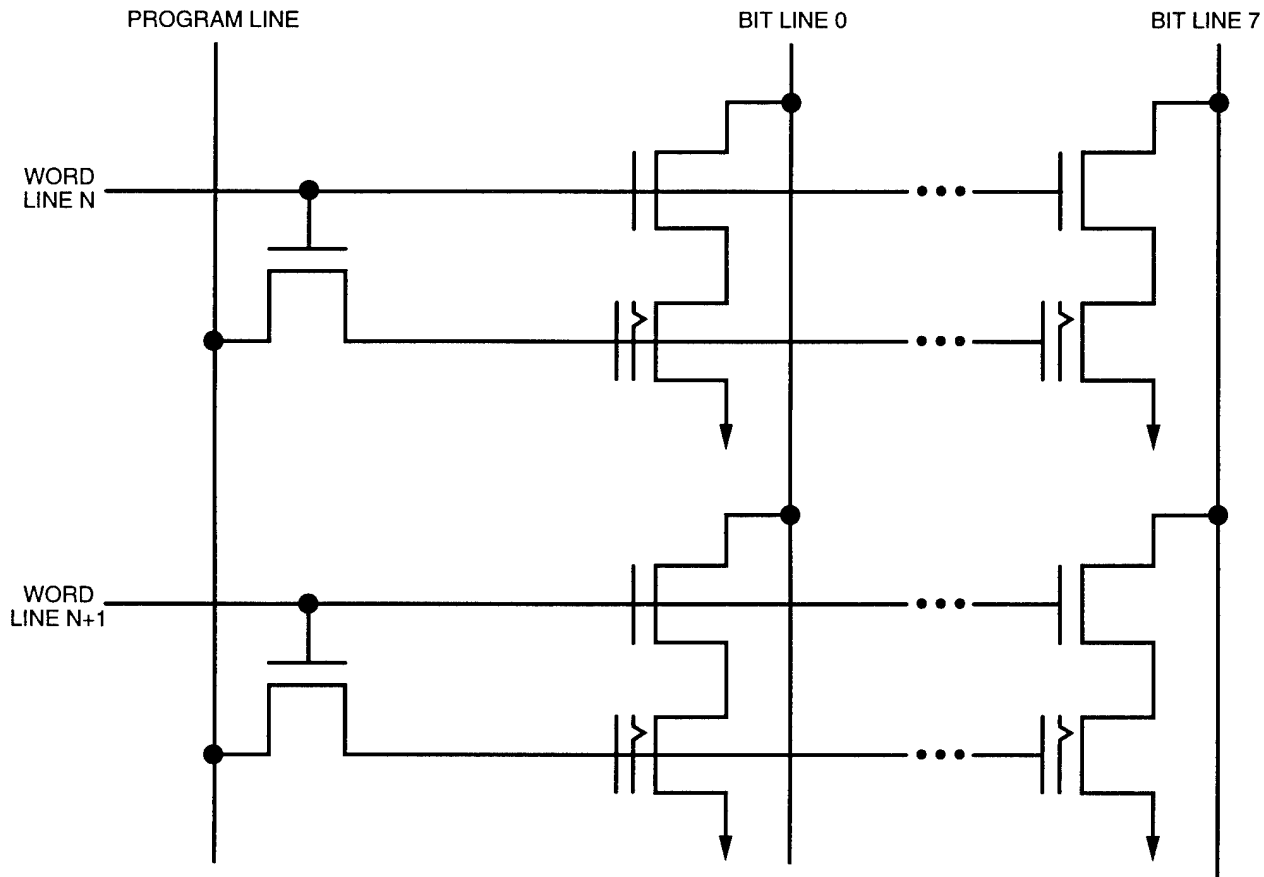


Figure 2-110. EEPROM memory array of FLOTOX cells for a byte architecture (Dressendorfer, 1991).

2.10.3 Silicon-Nitride-Oxide Semiconductor Nonvolatile Memory Technology

Metal-nitride-oxide semiconductor (MNOS) nonvolatile memory devices were first reported in 1967 by Wegener *et al.* (1967). MNOS nonvolatile technology is similar to MOS technology except that the gate oxide is replaced with a stack of dielectrics. This stack of dielectrics serves as a charge-trapping region, and in that sense it replaces the floating gate of floating-gate nonvolatile memory technology. There are several varieties of MNOS technology, the modern versions being silicon-nitride-oxide semiconductor (SNOS) in which the gate electrode is polysilicon. In this area, all the variants of this technology will be referred to as SNOS, since the basic principles of operation are similar in all cases. The discussion will focus on n-channel transistors; the operation of p-channel devices is similar with appropriate changes of voltage polarities and definition of the logic states.

Figure 2-111 is a cross section of an SNOS transistor, showing the typical thicknesses for the vari-

ous layers of the dielectric stack (memory stack). The device is written by applying a positive voltage to the gate electrode. The magnitude and duration of this voltage must be sufficient that electrons can tunnel through the thin bottom oxide into the trapping dielectric region (which can be either silicon nitride or silicon oxynitride) where they are subsequently trapped. At the same time, holes trapped in the dielectric can tunnel through the bottom oxide into the substrate. The resultant negative space charge causes a shift in the threshold voltage of the device in the positive direction, which, in the case of an n-channel transistor, can lead to enhancement-mode operation and a logical "1" state. To erase or clear the device, a large negative voltage is applied between the gate and substrate, the magnitude and duration of which must be sufficient to allow the trapped electrons to be tunneled out of the trapping dielectric and for holes to be tunneled from the substrate into the dielectric where they become trapped. This space charge leads to a negative shift in the threshold voltage of the transistor, which, for an n-channel transistor,

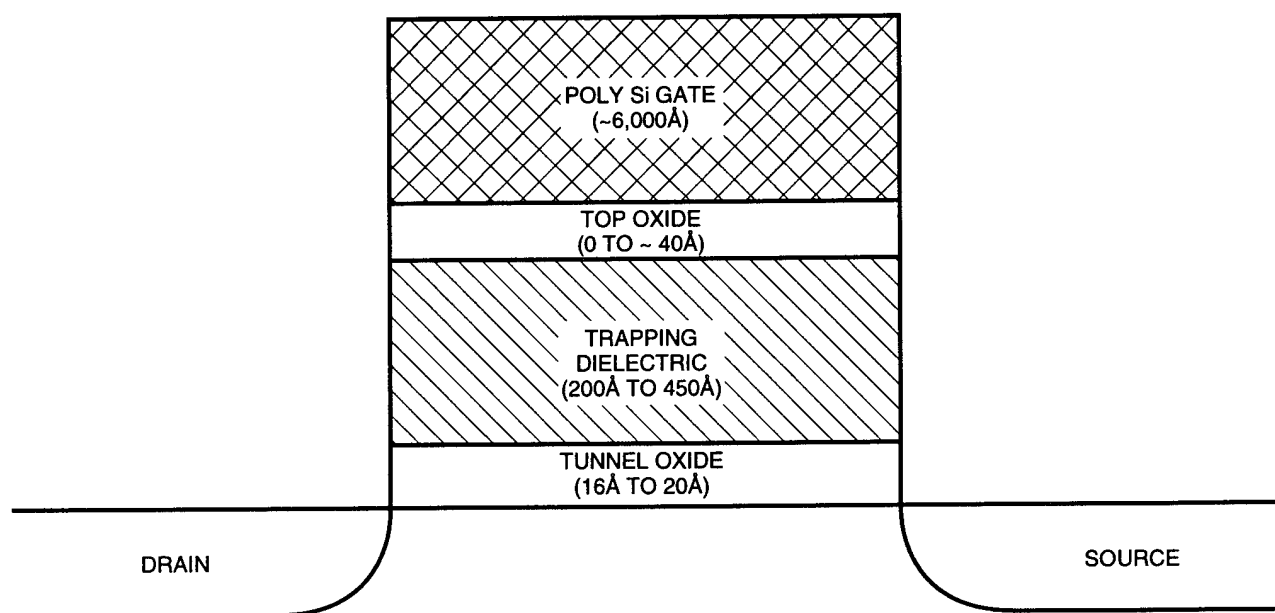


Figure 2-111. Cross section of an SNOS memory transistor showing the typical thicknesses of the various layers of the dielectric (memory) stack (Dressendorfer, 1991).

can lead to depletion-mode operation and a logical "0" state.

The rate at which carriers tunnel into (or out of) the trapping dielectric from (or into) the silicon substrate is affected by the following parameters: (1) the magnitude of the electric field across the tunnel oxide (which, in turn, is determined by the applied voltage, the dielectric constants, and thickness of the three layers in the memory stack, the doping density of the substrate, and trapped charge in any of the dielectric layers or at their interfaces); (2) the tunnel oxide thickness; (3) the barrier heights between the tunnel oxide, the silicon substrate, and the trapping dielectric; (4) the effective mass for carriers in the tunnel oxide; and (5) the temperature.

The total number of carriers trapped in the trapping dielectric depends upon the: (1) tunneling rate; (2) magnitude of the applied voltage; (3) length of time the voltage is applied; (4) density, energy, depth, and location of traps in the trapping dielectric; (5) cross section of these traps (which can depend upon the electric field); and (6) temperature.

As time elapses, the trapped space charge gradually leaves the trapping dielectric. The rate-limiting mechanisms governing charge decay can be different from those governing charge injection during program or erase operations. For example, the rate-limiting mechanism may be thermal emission from trap sites rather than back-tunneling through the oxide for certain geometries and temperatures.

Based upon the above discussion of operation, several observations can be made regarding the effects of the various layers in the memory stack. The thickness of the tunnel oxide influences the charge injection and decay, thicker oxides leading to less injection at a given field and a slower rate of charge back-tunneling (i.e., slower decay rate of threshold voltage). The trapping dielectric affects charge trapping and decay. Depending upon the energy level of the traps, trapped charge can be thermally emitted and then tunnel out of the dielectric, leading to a net reduction in the space charge. The top oxide can act as a barrier to reduce charge

injection from the gate electrode. This charge can become trapped and compensate that injected from the substrate, leading to less threshold shift than if such injection did not occur. This effect becomes more important as the total thickness of the memory stack is reduced.

In order to achieve low rates of charge loss from the trapping dielectric and thus low threshold-voltage decay rates, the SNOS structure usually must be annealed at a relatively high temperature (800 to 900°C) in a hydrogen ambient. The effect of this anneal is to reduce the number of interface trap levels at the Si/SiO₂ interface. Since this anneal is performed as the last high-temperature step in the overall process flow, it typically occurs either just before or just after contacts are opened in the final dielectric layer before the first metallization layer is deposited. The hydrogen anneal degrades the radiation hardness of MOS peripheral devices, and this represents a trade-off in retention characteristics and radiation hardness.

2.10.3.1 Design Considerations

SNOS memories are typically based upon the gated access approach, in which an MOS transistor is in series with the SNOS transistor (Hagiwara *et al.*, 1980; Knoll, Dellin, and Jones, 1983). A memory cell can consist of either one or two SNOS transistors per bit, with each SNOS transistor having an MOS access transistor, as shown in Figure 2-112. In operation, the cell is written by pulsing the gate voltage positively relative to the silicon substrate (the p-well) and source/drain (which are usually held at ground potential). The erase or clear is performed by holding the gate at ground potential and pulsing the p-well positively. This requires that the well potential be able to be controlled during data change operations. The MOS access transistor and SNOS memory transistor can be separate, as shown in Figure 2-112, or integrated, as shown in Figure 2-113, to provide a more compact cell layout.

In order to read the memory cell, the bit line is precharged, the gate to substrate voltage of the SNOS transistor held at zero, and the MOS access transistor turned on. The sense amplifier provides

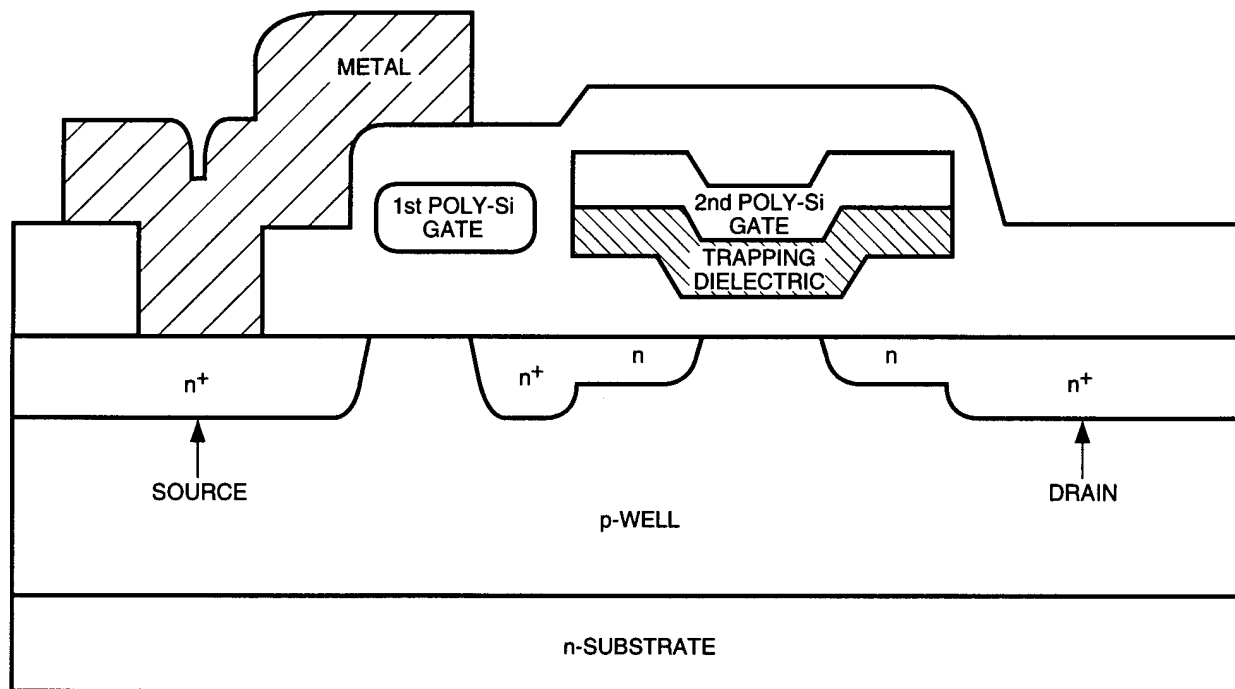


Figure 2-112. Cross section of a typical SNOS memory cell having separate MOS access transistors (Dressendorfer, 1991).

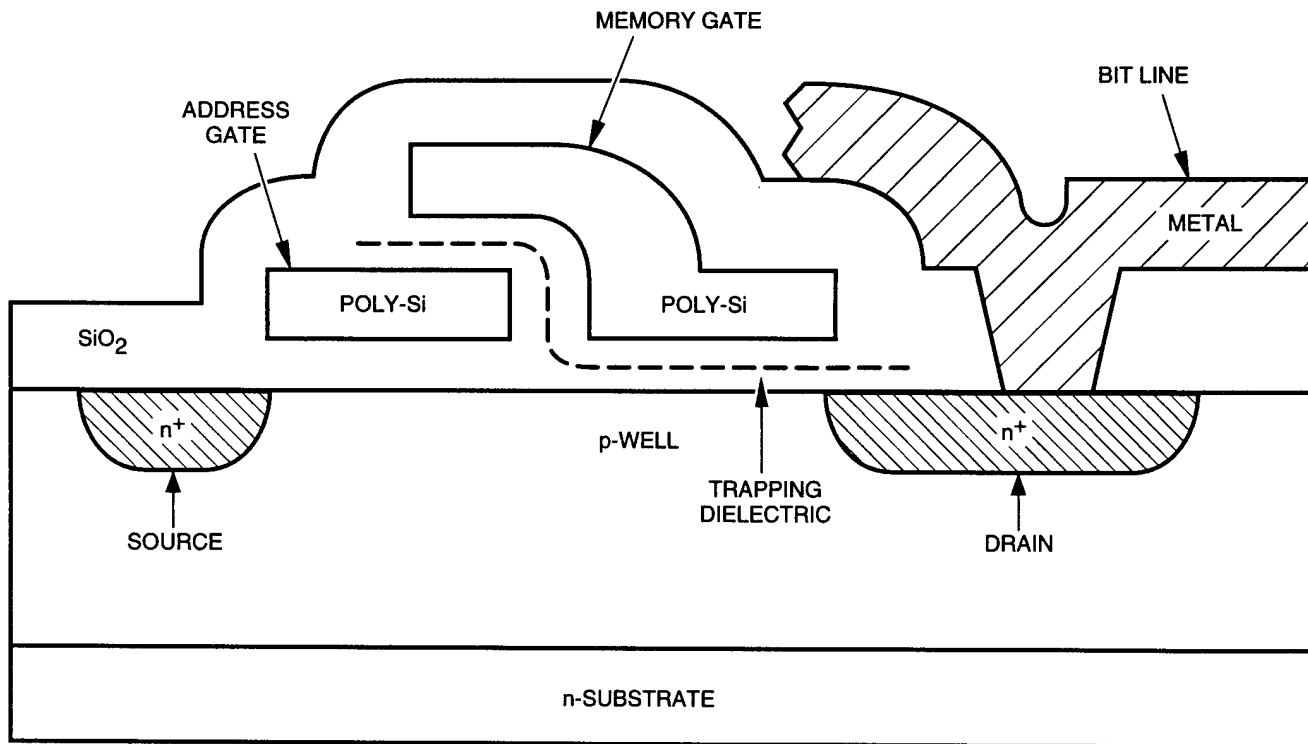


Figure 2-113. Cross section of an SNOS memory cell with a merged MOS access transistor (Dressendorfer, 1991).

a trickle charging current to the bit line and monitors the bit-line voltage. When the memory cell contains a "0" (i.e., in depletion mode), it sinks this charging current and pulls the bit-line potential to a low value. When the memory cell contains a "1" (i.e., in enhancement mode and thus draws no current), the charging current is greater than the bit-line leakage; thus, the bit-line voltage is at a high value.

The sensing scheme for the memory cell of Figures 2-112 or 2-113 requires that one of the logic states be enhancement mode and the other be depletion mode, with enough current drive at zero gate voltage to overcome the sense current applied to the bit line. This places requirements not only on the difference between the logic "1" and logic "0" threshold voltages (the memory window), but also upon the center position of the window. For circuits intended to operate in a radiation environment, the "1" threshold must typically be greater than zero, and the "0" threshold must be less than approximately -0.5 volt in order to have reliable sensing. The rate at which the bit line is pulled down also depends upon amount of current drive the logic "0" state has above the minimum. This drive degrades with time as the threshold voltage decays, so the minimum read access time will increase with time. Thus, there is a trade-off between read access time and retention SNOS memories.

During the read operation, the gate voltage of the SNOS transistor is held at the same potential as the substrate. This minimizes read-disturb problems since any applied potential could affect the charge stored in the device. The design of SNOS memories must minimize unwanted voltages developed across the memory stack for either the transistor being read or other transistors in the array where the read is inhibited.

An individual memory cell can also be composed of two SNOS and two MOS transistors. The write operation of the individual transistors is similar to that described for the cell of Figure 2-112, except that one SNOS transistor is written into the positive threshold state and the other into the negative threshold state. This configuration could repre-

sent a logic "1," with logic "0" represented by the transistors written into the opposite states. Reading this memory cell now depends upon a difference being generated in the voltages on the bit and bit-bar lines as the two SNOS transistors are connected to them. In this sensing scheme, the requirements on the threshold voltages of the individual SNOS transistors are less severe than for the single transistor cell described above. The difference in threshold voltages between the two transistors need only be approximately 0.05 volt (rather than the 0.5 volt above), and the center position of the window is relatively unimportant as long as at least one of the transistors is depletion mode.

Memories with two transistors per bit will have longer retention than those with one transistor per bit when compared under identical conditions. Processing constraints and control necessary to obtain a given level of memory performance are also reduced. However, this increased robustness comes at the price of a reduced density, since for the same size chip, a memory with two transistors per bit will have approximately one-half the storage capacity of a memory with one transistor per bit.

A third design approach is a shadow RAM, where the SNOS transistors are connected to a standard SRAM cell via control transistors. All read and write operations are carried out on the SRAM cell, with the stored information transferred to the SNOS nonvolatile element only upon activation of a control signal (when power loss is detected, for example). This approach provides a memory with the read and write speed of the SRAM, and requires much less endurance from the nonvolatile memory elements. It is a much larger memory cell, however, and its operating characteristics may not be suitable for all applications.

2.10.3.2 Radiation Effects

Ionizing radiation will lead to a net loss in trapped charge in SNOS transistors, thus affecting the retention of the memory. This effect is shown in Figure 2-114, where SNOS threshold voltages for the two logic states are shown as a function of time. Plotted are the retention curves for identical transistors written into different initial states by al-

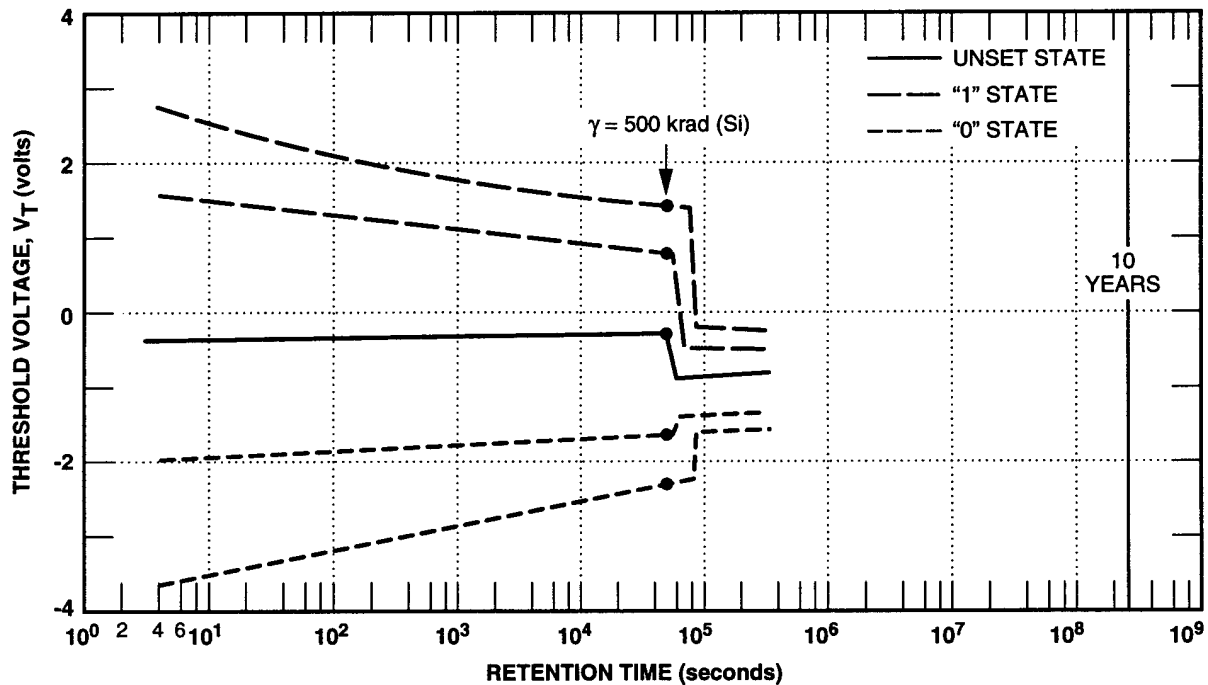


Figure 2-114. Effect of irradiation on SNOS threshold voltage for transistors written into different initial states. [At 5×10^4 seconds, the transistors were irradiated with 500 krad(Si)] (McWhorter, Miller, and Dellin, 1986).

tering the programming time. The absolute value of threshold voltage for both states is reduced by the radiation, leading to a reduction in the memory retention of the devices. The shift in threshold voltage caused by a given ionizing radiation dose depends upon the threshold voltage at the time the irradiation occurs and the dose rate of the radiation. Models have been developed that can describe this radiation-induced threshold voltage shift and its subsequent effect on the retention properties of SNOS transistors. Models have also been developed that can predict the radiation-induced threshold voltage shift for both logic states as a function of initial threshold voltage, dose rate, and ionizing radiation dose. An example of the kind of results obtainable with the predictive model is shown in Figure 2-115 for a relatively low dose-rate irradiation of 0.09 rad(Si)/sec.

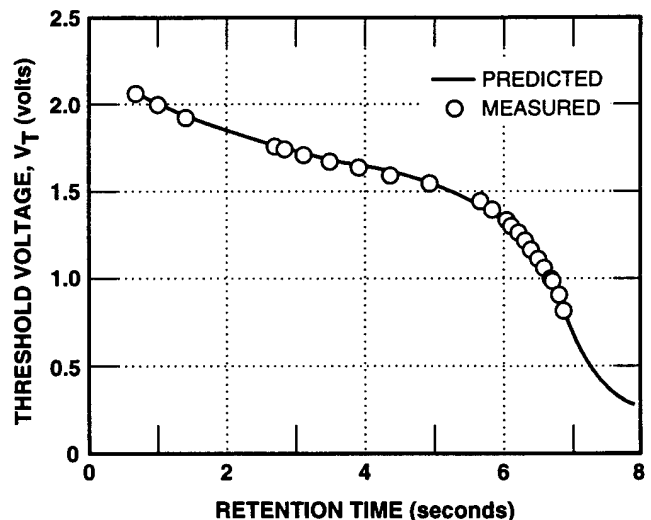


Figure 2-115. Retention curve for an SNOS transistor in the "1" state in a low-dose-rate (0.09 rad/sec) environment (McWhorter *et al.*, 1987).

SNOS transistors will continue to function properly after being irradiated to very high ionizing radiation dose levels; little degradation in operational properties has been observed at doses as high as 10^9 rads(Si). Devices may be written or erased after receiving ionizing radiation doses of this magnitude with minimal changes in their characteristics. However, as described above, the processing associated with the fabrication of the SNOS transistors can degrade the ionizing radiation dose hardness of the MOS control devices. Thus, the ionizing radiation dose hardness of an SNOS memory for write/erase operations will be determined by the hardness of the peripheral circuitry.

2.10.4 Thin-Film Magnetic Nonvolatile Memories

Magnetic memories have existed for many years in a variety of forms, ranging from magnetic tape and disk media to core and plated-wire memory. An extension of magnetic technology to the integrated circuit format utilizes magnetic thin films to

provide the nonvolatile storage element when integrated with a base semiconductor IC technology (such as CMOS or bipolar). Because the technology is still in the development phase, many issues remain unresolved regarding its capabilities and practical applications. Since little has been published in the open literature on these activities, only a brief description of the concepts of operation and characteristics will be provided here.

A magnetic thin film possesses a hysteresis loop. Information can be stored as the direction of magnetization, and can be altered or read by the application of an external magnetic field. The external field can be produced by current flow through a conductor near the magnetic film. Two primary physical phenomena can be employed to read the direction of the magnetization in the film: magneto-inductance and magneto-resistance.

Figure 2-116 illustrates the basic structure of a possible nonvolatile memory element in a magnetic thin-film memory. The thin magnetic film can be magnetized in either of the two directions

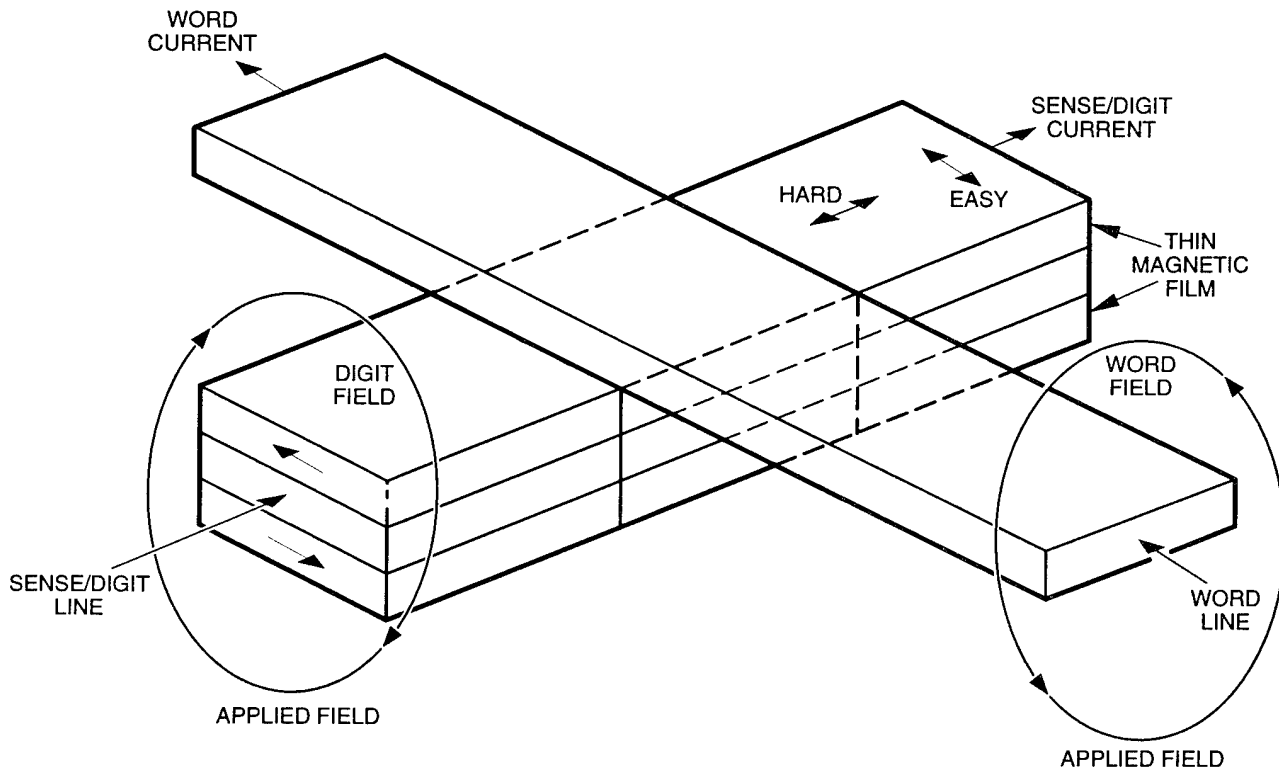


Figure 2-116. Structure of a thin-film magnetic memory current (Dressendorfer, 1991).

along the "easy" axis of magnetization. To read the direction of this magnetization by the magneto-inductive effect, a current is pulsed along the word line. This causes a changing magnetic flux in the magnetic thin-film material, which, in turn, generates a potential in the sense line, the polarity of which depends upon the direction of magnetization in the film. Reading by means of the magneto-resistive effect relies upon the fact that the resistance of the magnetic field depends upon the direction of the magnetization relative to that magnetic field. Thus, to read in this mode, a current is driven through the word line to establish an external magnetic field, and a current is driven through the sense line. The voltage generated by this current in the same sense line then gives the resistance and thus the direction of magnetization.

Fabrication of the magnetic memory elements can use standard IC processing techniques, although the materials are different from those typically used. These elements can be fabricated as a separate processing module from the base technology, and thus can be utilized either by CMOS or bipolar peripheral circuitry. Tight process control is required of the magnetic memory elements.

Both the magneto-inductive and magneto-resistive modes may be operated as destructive read-out (DRO) or nondestructive read-out (NDRO). Signal levels tend to be rather small (~ 1 mV), placing severe demands on the sense circuitry. Because of these small signals, the read access time is somewhat slower than the other memory technologies discussed, being of the order of 1 μ sec. Write times can be significantly faster. The magneto-inductive readout approach does not scale as well as the magneto-resistive since the signal is proportional to the cell size.

Based on data from other magnetic technologies, it is expected that magnetic thin-film memory elements will have very high endurance ($>10^{15}$ cycles) and long retention (>20 years).

The radiation response characteristics of magnetic memory elements can be expected to be quite good. Ionizing radiation dose is likely to have little effect on the stored magnetization, so the hardness

of the memory to this environment will be limited by the hardness of the peripheral circuitry.

2.10.5 Ferroelectric Nonvolatile Memory Technology

A ferroelectric material exhibits an electric dipole moment, even in the absence of an applied electric field. As a result, the polarization of the material depends upon its electrical history, and this polarization state may be used as the indicator of stored information. Ferroelectric crystals are classified into two primary groups: (1) *order-disorder*, in which the ferroelectric effect is associated with the ordering of ions; (2) and *displacive*, in which the polarization change is caused by a displacement of a sublattice of one type of ion relative to other ions in the crystal.

Ferroelectrics of most interest for nonvolatile memories are of the displacive type. An example

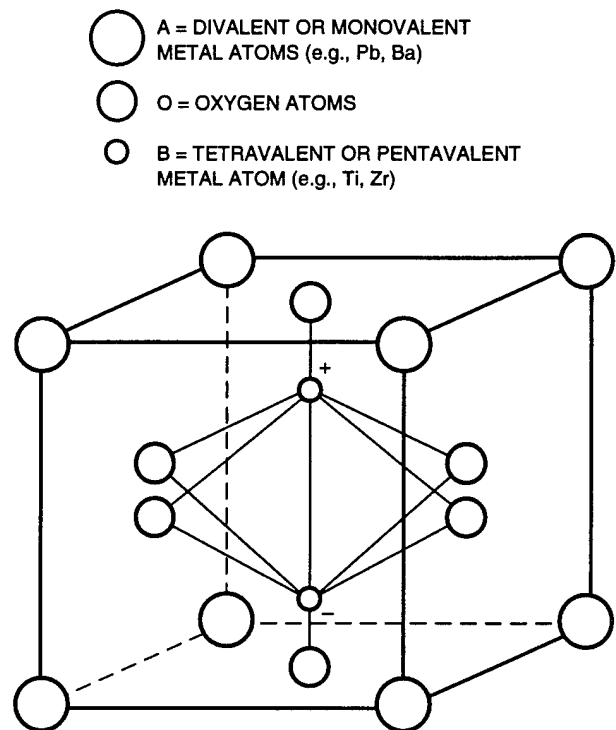


Figure 2-117. Structure of the ferroelectric perovskite crystal type ABO_3 , showing the two stable positions of the B ion that lead to the permanent polarization state (Dressendorfer, 1991).

of the ionic motion giving rise to the permanent polarization in perovskite crystals (such as lead titanate and barium titanate) is shown in Figure 2-117. The titanium atom at the center of the unit cell has two stable positions as shown, each giving rise to a different net polarization in the crystal. The stable position (and thus polarization) can be altered by the application of an electric field. This effect is illustrated by the hysteresis loop in Figure 2-118, where the polarization of a ferroelectric is plotted as a function of the applied electric field. This hysteresis loop is very similar to that observed for ferromagnetic materials, where magnetization is plotted as a function of applied magnetic field.

Shown in Figure 2-118 are several key parameters for ferroelectric materials. The spontaneous polarization (P_s) is the maximum polarization due to the ferroelectric susceptibility. The remanent polarization (P_r) is the polarization at zero applied field. The maximum polarization (P_{max}) is the maximum total polarization (including both the ferroelectric and linear dielectric contributions); it

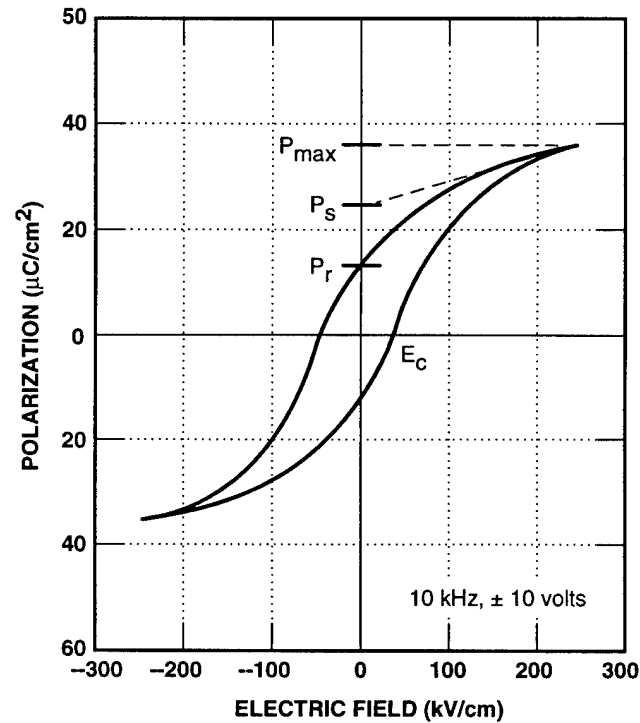
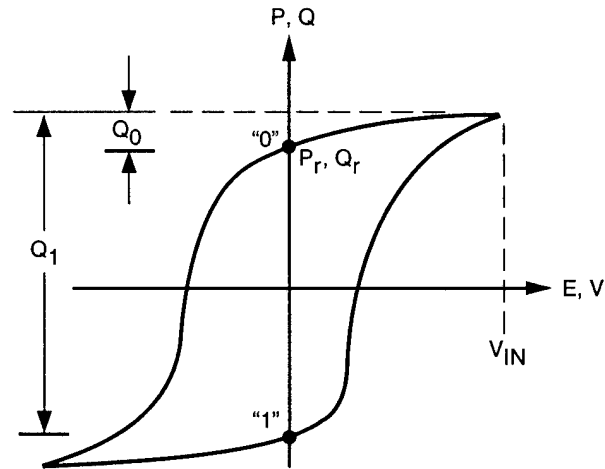
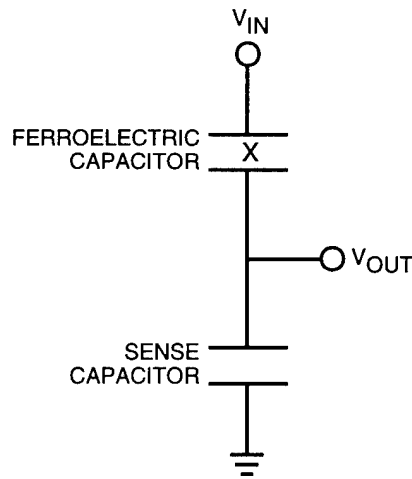


Figure 2-118. Typical hysteresis curve for a ferroelectric thin film, showing several important parameters (Dressendorfer, 1991).

is not a basic material property since it depends upon the applied electric field. The coercive field (E_c) is the field at zero polarization, and is a measure of the field required to switch the ferroelectric from one polarization state to the other. It should be noted that the values of these parameters are unique only for a saturated hysteresis loop; paths interior to the saturated loop can be traced out for lower drive fields. Another important parameter for ferroelectrics is the Curie temperature (T_c), the temperature at which the material undergoes a transition from the ferroelectric state to a paraelectric state. As the temperature approaches the Curie temperature, the spontaneous polarization



(a) Hysteresis Curve



(b) Readout Scheme

Figure 2-119. Conceptual operation of a ferroelectric memory capacitor (Dressendorfer, 1991).

tion decreases. Above the Curie temperature, all memory of the stored polarization state is lost.

The conceptual operation of a simple ferroelectric memory device can be understood with the aid of Figure 2-119. Depicted is a hysteresis curve showing the two stable polarization states and the charge that will result from pulsing the capacitor to V_{IN} . The read-out scheme for the memory is also shown, with a sense capacitor in series with the ferroelectric capacitor. If a large positive voltage pulse is applied to a ferroelectric capacitor and the voltage returned to zero, the polarization will be in the state labeled "0." Similarly, if a large negative voltage pulse is applied, the resulting polarization will be in the state labeled "0." If a large negative voltage pulse is applied to the capacitor structure, for a device in the "0" state, an amount of charge Q_0 will appear on the electrode of the sense capacitor, whereas for a device in the "1" state, an amount of charge Q_1 will appear on the sense capacitor. Thus, the output signal for the two logic states will depend upon the maximum polarization, the remanent polarization, and the sense capacitance.

2.10.5.1 Technology Description

The ferroelectric capacitor conceptually can be integrated in a straightforward manner into a vari-

ety of integrated circuit technologies, although in actual practice a number of difficulties in process integration must be overcome, as described below. The capacitor can be an element separate from any others in the base technology; it can be inserted as a process module into the baseline technology flow. The elements of the capacitor are the top and bottom electrodes and the ferroelectric film itself. It may also be necessary to include barrier layers to prevent interactions between the ferroelectric capacitor elements and the materials of the base technology. An example of the way in which a ferroelectric capacitor might be inserted into a CMOS technology is shown in Figure 2-120.

A number of common issues arise in attempting to integrate ferroelectrics into a baseline integrated circuit technology, whether that technology be bipolar, CMOS, or GaAs. The ferroelectric capacitor itself presents a number of material and device physics issues. Although there is a great deal of literature on the characteristics of bulk ferroelectrics, it is not easily extrapolated to the thin films ($< 0.5 \mu\text{m}$) that must be used in integrated circuits.

Optimization of the film is complicated by the fact that the film preparation techniques can have a significant impact on the resultant properties. A number of avenues are being explored, including

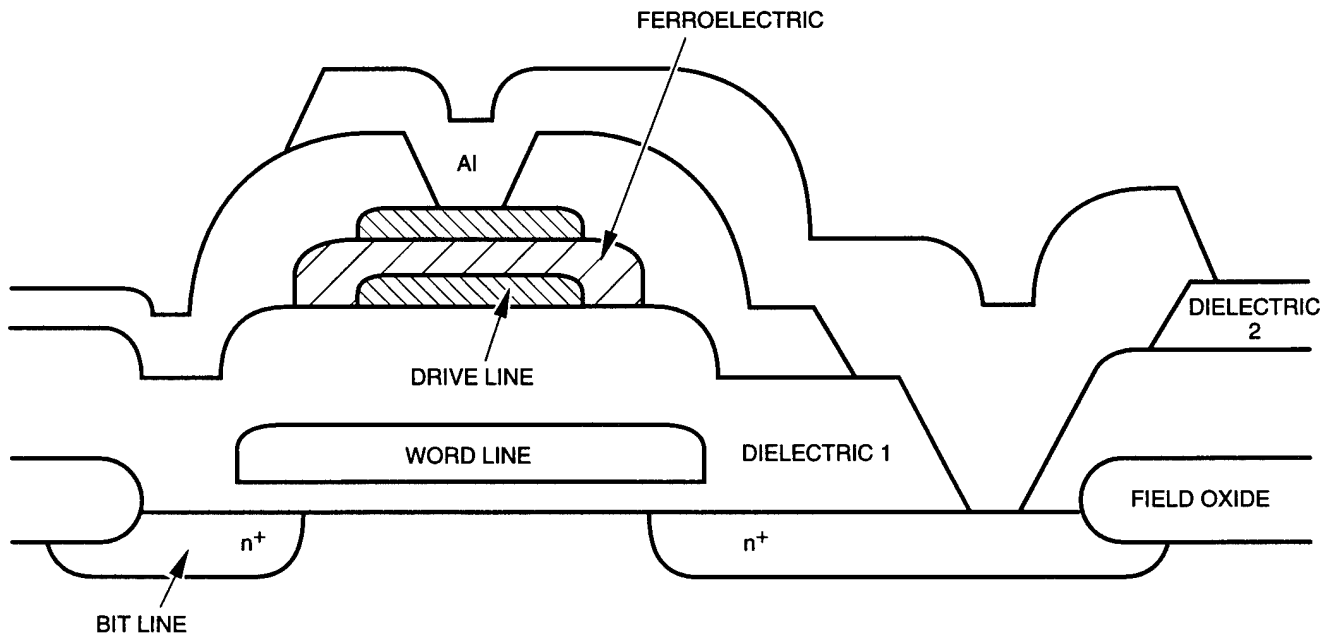


Figure 2-120. Cross section of a ferroelectric capacitor memory cell (Dressendorfer, 1991).

approaches based upon various solution chemistries followed by spinning the ferroelectric film onto the substrate, sputtering, metallo-organic chemical vapor deposition (MOCVD), cluster-ion beam, gas-jet deposition, laser ablation, and low-pressure chemical vapor deposition (LPCVD). Film properties are also affected by any thermal environments to which they are exposed. In most cases, in order to obtain the desired perovskite phase of lead-zirconate-titanium (PZT), a sintering step in the temperature range of 550°C to 700°C is required.

The electrodes used for the ferroelectric capacitor affect its subsequent properties markedly. Much of the work to date on PZT thin films has centered on the use of platinum for the electrode, although a number of other materials are being explored. Some proprietary materials have been reported to provide ferroelectric devices markedly improved over those obtained with platinum.

In addition to the development underway for the ferroelectric capacitor itself, significant work

is required to effectively integrate that capacitor into a baseline technology flow. The integration must be performed in such a way as to minimize adverse effects on the baseline devices from the ferroelectric processing and likewise on the ferroelectric devices from the baseline processing. Since both the ferroelectric and baseline technology require thermal treatments to achieve the desired properties, interactions between the two are likely to occur. Other process development and integration issues include possible contamination of the baseline devices from the materials in the ferroelectric devices, long-term compatibility of the ferroelectric device materials, etching of the ferroelectric and electrodes, electrode compatibility and adherence, contact methodology, possible stress effects, interactions of ambients with the ferroelectric, topography reduction and control, and packaging and assembly issues.

An alternative technology approach is being pursued by Westinghouse Corporation. Rather than using a ferroelectric capacitor as the memory

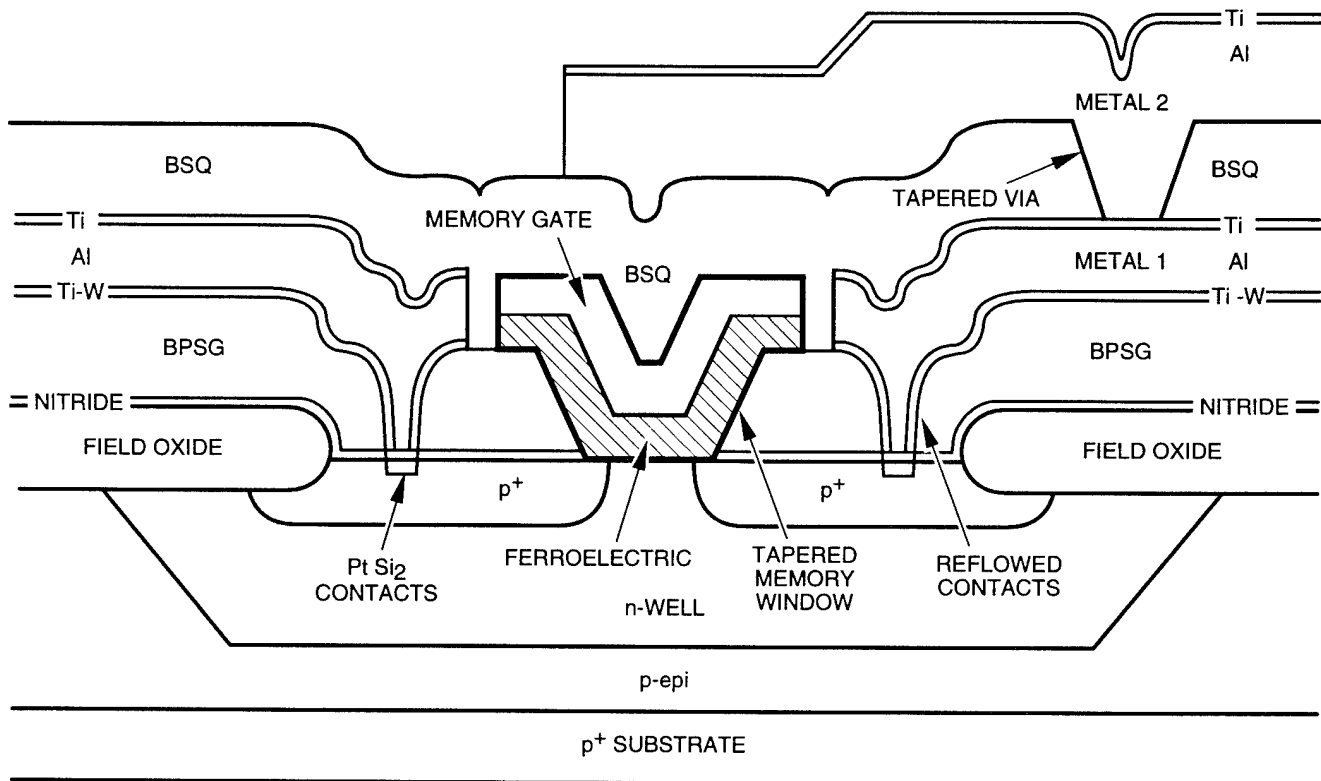


Figure 2-121. Cross section of a ferroelectric transistor in the Westinghouse 1-mm process (Lampe *et al.*, 1990).

element, the ferroelectric film is used as the gate dielectric for a FET, forming a ferroelectric material FET (FEMFET), as shown in Figure 2-121. In this case, the silicon surface may be accumulated, depleted, or inverted at zero applied voltage to the gate electrode. Thus, the polarization state of the ferroelectric may be sensed by determining the threshold of the transistor (which could be enhancement mode for one polarization state and depletion mode for the other state). The operation of the memory element in full memory array could be very similar to that of an SNOS device, except that positive pulses applied to the gate electrode lead to the more negative threshold voltage state, and negative gate voltages result in the more positive threshold voltage state.

2.10.5.2 Radiation Effects

Several studies of the effects of radiation on ferroelectric capacitor structures have been reported. Under constant bias, the retained polarization is reduced with ionizing radiation dose, as illustrated in Figure 2-122. The dose level at which this degradation is observed depends upon the processing details of the ferroelectric film, and it can be greater than 10 Mrads(Si) with appropriate processing. The degradation does not appear to be affected by cycling the device prior to radiation. However, if the device is cycled during the radiation, no degradation relative to unirradiated samples is observed. The primary effect of the ionizing radiation appears to be the alteration of the switching characteristics of the ferroelectric, probably from the buildup of space charge in the device. An example of post-radiation switching characteristics for devices irradiated under several bias conditions is shown in Figure 2-123.

2.10.6 Summary

Currently, floating-gate memories dominate semiconductor nonvolatile memory technology. SNOS memories have been preferred for applications requiring radiation hardness, although there are several companies manufacturing them for commercial applications. Ferroelectric devices are just emerging; it remains to be seen whether they will make significant inroads into the overall mar-

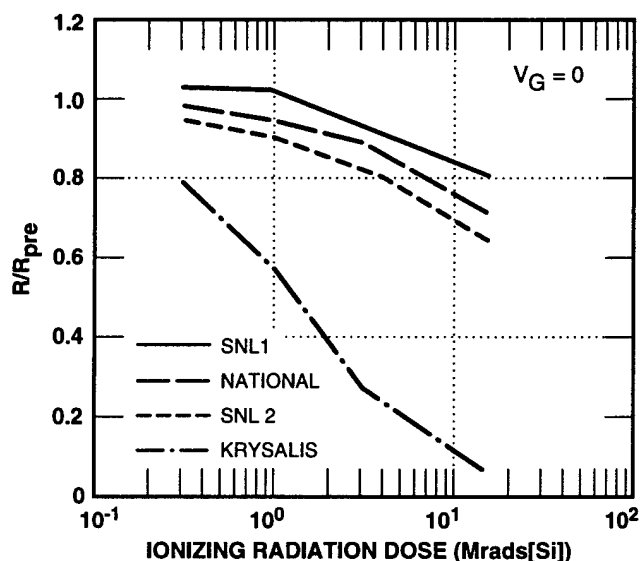


Figure 2-122. Effect of ^{60}Co -ionizing radiation dose (225 rads[Si]/sec) on the switched polarization charge of thin-film ferroelectric capacitors prepared by different processing techniques (Schwank *et al.*, 1990).

ket. Thin-film magnetic memories are still in the development phase.

Floating-gate and SNOS memories have very similar performance characteristics in reading, writing, and endurance. SNOS does not have the same ultimate retention capability as floating gate. SNOS may be able to scale to lower voltage operation than floating gate devices. Ferroelectric memories offer the potential of much faster writing characteristics than either of these two, and with higher endurance. Retention is not yet completely demonstrated, but it could be at least comparable. Magnetic thin-film memories are slower reading devices than the others. They should be able to scale to low-voltage operation, but materials and process considerations may limit their density. Magnetic memories should offer very high endurance and retention.



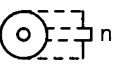

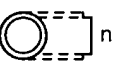
The intrinsic radiation tolerance of floating-gate memory elements is less than that of SNOS. Ferroelectric memory elements are much more tolerant, as are magnetic thin-film memory elements.

An overview comparison of some of the important characteristics of these technologies is given in Table 2-7. Note that the radiation hardness characteristics given in this table represent those of the

Table 2-7. Comparison of several characteristics of solid-state electronic nonvolatile memory technologies.

Technology	Density Available (Mbits)	Nominal Read Access Time ^a (nsec)	Write(W)/Erase(E) Time ^a	Endurance ^b (cycles)	Retention ^b (years)	Ionizing Radiation Dose Intrinsic Hardness ^c (rads[Si])
EPROM	16	<100	10 to 200 μ sec (W) 220 minutes (E)	10^2	>20	10^5
FG EEPROM	4	<100	0.1 to 10 msec (W) 1 to 100 msec (E)	10^4	>20	10^5
SNOS EEPROM	1	~200	0.1 to 10 msec (W) 1 to 100 msec (E)	10^4	>20 ^d	10^6
Ferroelectric	0.016 ^e	<100	<100 nsec	> 10^{12} (^f)	>20(^f)	> 10^7
Magnetic thin film		~1,000	~200 nsec	> 10^{15} (^f)	>20(^f)	> 10^7

Notes:^aTypical ranges.^bTypical specifications.^cExpected hardness of nonvolatile memory element; support circuitry may limit actual hardness.^dTrade-offs between endurance and retention are possible.^eUnder development.^fProjected values, additional work necessary to verify.**Table 2-8.** Properties of optical fibers (Morrow, 1986).

Type of Fiber	Diagram of Fiber	Core Diameter (μ m)	Cladding Diameter (μ m)	Numerical Aperture, NA	Nominal Attenuation (dB/km)	Bandwidth (MHz-km)	Frequently Encountered Core/Cladding Sizes (μ m)
Multimode, step index		50 to 400	125 to 500	0.15 to 0.4	<50	<25	100/140, 200/250, 400/450
Multimode, graded index		30 to 75	100 to 250	0.2 to 0.3	<10	<200	50/125, 62.5/125, 85/125
Single mode, step index		3 to 10	50 to 125	~0.10	<3 at 850 nm	<2,000	9/125
Plastic-clad, silica		50 to 500	125 to 800	0.2 to 0.4	<50	<25	—
Plastic		200 to 600	400 to 1,000	~0.5	<1,000 at 650 nm	—	—

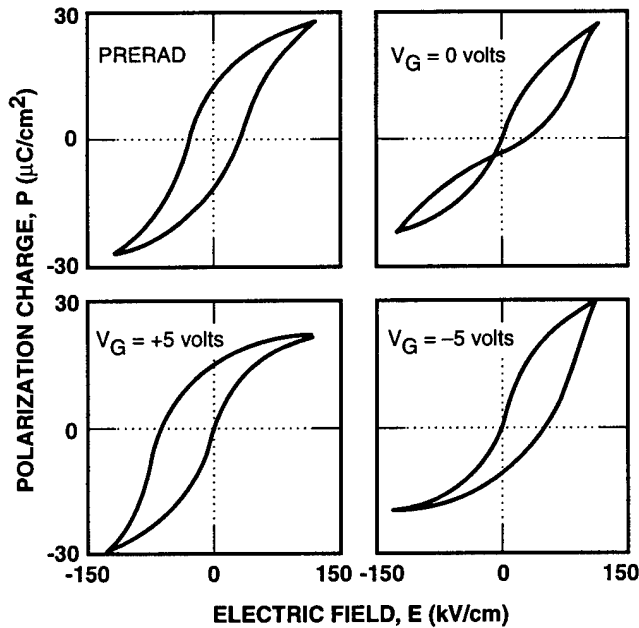


Figure 2-123. Hysteresis curves for ferroelectric thin-film capacitors before irradiation and after irradiation with 0-, -5-, and +5-volt biases (Schwank *et al.*, 1990).

nonvolatile memory element itself; a full memory device may exhibit lower hardness levels (or experience single event upset) because of the characteristics of the support circuitry.

2.11 Radiation Effects on Optical Fibers and Electro-Optic Components

2.11.1 Optical Fibers

The rapid growth in the development of optical-fiber technology during the 1980-1990 time frame has led to the development of many types of optical fibers and significant improvements in the ra-

diation hardening of these optical fibers. A summary of the properties of optical fiber types is given in Table 2-8.

A step-index fiber is an optical fiber that consists of an inner core and an outer cladding. The operation of step-index fibers is based on a difference in refractive indices between that for the core of the fiber and that for the cladding surrounding the core. The light ray entering the fiber end will experience total internal reflection at the core-cladding interface and propagate down the fiber [as shown in Figure 2-124], so long as the angle of reflection is less than the critical angle, θ_c . The magnitude of the total acceptance angle for light entering the fiber is usually expressed by the numerical aperture NA, which is given by the expression:

$$NA = n_1 \sin \theta_c = (n_1^2 - n_2^2)^{1/2}, \quad (2.25)$$

where n_1 is the refractive index of the fiber core, n_2 is the refractive index of the cladding, and θ_c is the maximum angle for total internal reflection. As shown in Table 2-8, typical values for NA range from about 0.1 to 0.4. As might be expected, the larger the NA, the easier it is to couple a light-emitting diode (LED) to the fiber.

A light pulse of a certain shape and magnitude will, upon entering and traveling a significant distance through a real, nonideal fiber, experience a reduction in magnitude and a temporal spreading of the pulse shape. The first effect is due to attenuation in the fiber, while the second is due to dispersion. The attempt to minimize both of these deleterious effects has been the driving force be-

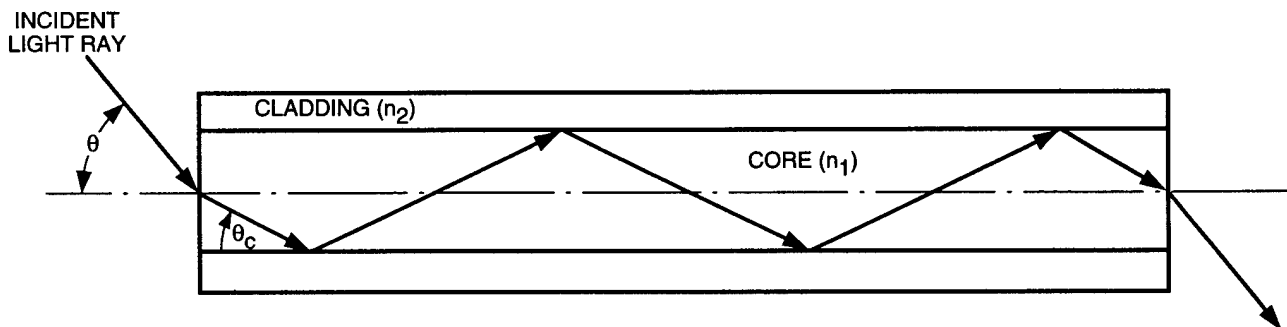


Figure 2-124. Propagation of light rays in an optical fiber.

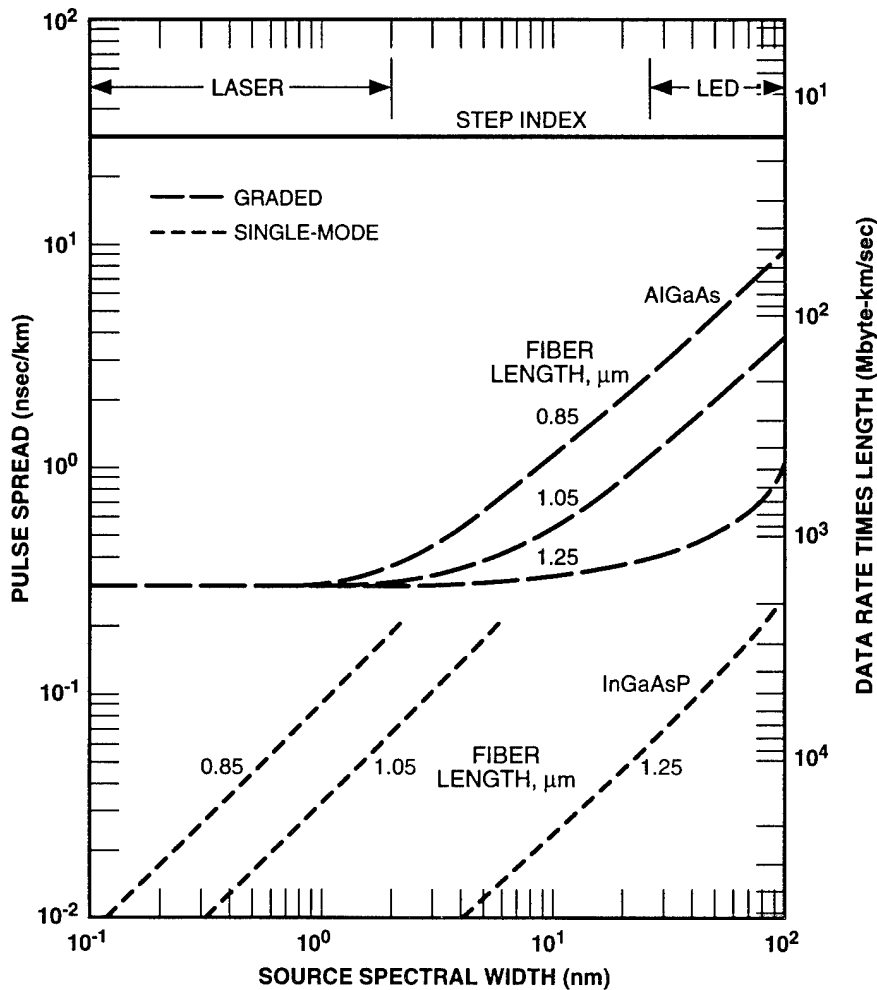


Figure 2-125. Dispersion effects for a variety of fiber types and light sources (Li, 1978).

hind continued modification and improvement of optical fibers. The operating wavelength chosen for a fiber-optic link is also often determined by the need to minimize attenuation and dispersion. Hence, these effects can dictate the choice of source and detector.

Signal dispersion in a fiber, which determines the bandwidth of the fiber, is due to modal dispersion and chromatic (wavelength-dependent) dispersion. As shown in Figure 2-125, modal dispersion will dominate in fibers with a large NA, which can support several different angles at which light rays can enter the fiber. As a consequence of the differing path lengths traveled by these rays, several modes of electromagnetic propagation are

set up within the fiber with differing group velocities for each of the modes. The various group velocities associated with these modes lead to dispersion (pulse broadening), which limits the information bandwidth of multimode step-index fibers. The maximum difference in arrival time at the end of a fiber of given length increases with NA and is typically 20 to 50 nsec/km. Since light source coupling efficiency also increases with NA, a compromise between efficient coupling of the LED to the step-index fiber and the maximum bandwidth of the fiber is required. In spite of this compromise, multimode step-index fibers are attractive and useful, especially for moderate-length and bandwidth applications that require transmission of considerable power.

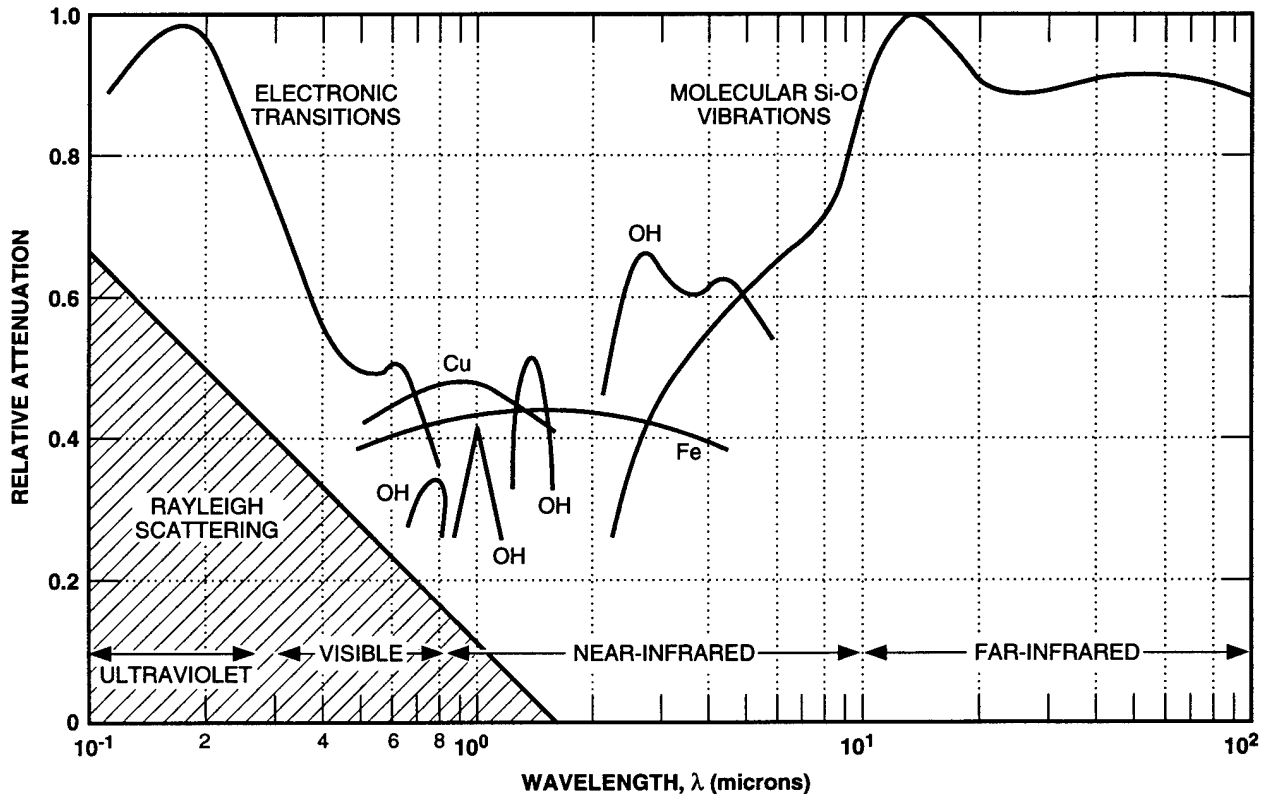


Figure 2-126. Contributions to attenuation in glass fibers (Wolf, 1979).

Attenuation of the optical signal as it travels through the fiber core is caused by two mechanisms; scattering and absorption. *Scattering mechanisms* will not be discussed in any detail because they do not influence radiation effects in fibers and are usually small compared with absorption phenomena. However, *scattering effects* do influence the choice of state-of-the-art fibers. As shown in Figure 2-126, scattering decreases strongly with increasing wavelength. In recent years, the purity and quality of fibers has reached the point where fiber attenuation has decreased to the scattering limit, making longer wavelengths more desirable.

2.11.2 Radiation Effects on Fiber Optics

The mechanism for propagating the signal light ray down the core of a long fiber immediately suggests that the most important radiation effect is radiation-induced signal attenuation in the fiber

core. From the point of view of radiation effects, the most important property of fibers is the absorption of light in the core of the fiber by various types of color centers, many of which are present prior to irradiation. Examples are shown in Figure 2-126 over a wide wavelength range and can include intrinsic absorption mechanisms, such as Si-O bond-induced absorptions, and extrinsic attenuation due to impurities and defects in the glass core of the fiber. Because of the nature of fibers, absorption is expressed in decibels per kilometer (dB/km) of fiber length rather than in inverse centimeters (cm^{-1}), as is usually the case for absorption coefficients. The two units are related as follows: attenuation in dB/km = $4.3 \times 10^5 \times$ (absorption coefficient in cm^{-1}). Thus, an attenuation of 10 dB/km, suitable for a practical fiber of moderate length, is equal to $2.3 \times 10^{-5} \text{ cm}^{-1}$, an exceedingly small absorption coefficient.

The radiation damage mechanism in optical fibers basically involves the trapping of radiolytic electrons and holes in either preexisting or radiation-created sites. The incident radiation creates high-energy electrons, which, in turn, excite electrons from the valence band. Radiolytic electrons and holes are trapped in defect sites that arise from preexisting material impurities or from knock-on atomic displacement. Radiolytic, or photochemical, displacement also causes electrons and holes to be trapped in defect sites. Radiation-created electron-hole pairs can decay nonradiatively to provide sufficient energy to the glass matrix to displace an oxygen atom. The resulting color centers have optical absorption in the visible near-infrared band. These optical absorption centers result in increased darkening (loss) as a function of wavelength. Other specific radiation-induced degradation effects are engendered by transient ionizing radiation and neutron irradiation. These effects are discussed in Chapters 3 and 4, respectively.

Inspection of Figure 2-126 illustrates the origin of the "window" region in which fiber links are located in order to minimize attenuation. Electronic transitions are dominant in the ultraviolet region, while Si-O bond effects dominate in the infrared region. Fortunately, these two intrinsic mechanisms do not overlap significantly in the wavelength range of about 0.7 to 2 μm . Within this range, it is necessary to minimize the concentration of impurities such as heavy metals, and for the lowest attenuation fibers, the OH or water content of the fiber. The combined effects of dispersion and OH absorption have resulted in three "windows": 0.85, 1.3 and 1.56 μm . These windows are illustrated in Figure 2-127 for a fiber of moderate water (OH) content. Note the existence of the OH bands and the absorption continuum, which decreases with increasing wavelength out to about 1.6 μm .

As illustrated in Figure 2-125, for a fiber to be functional a difference in the core and the cladding

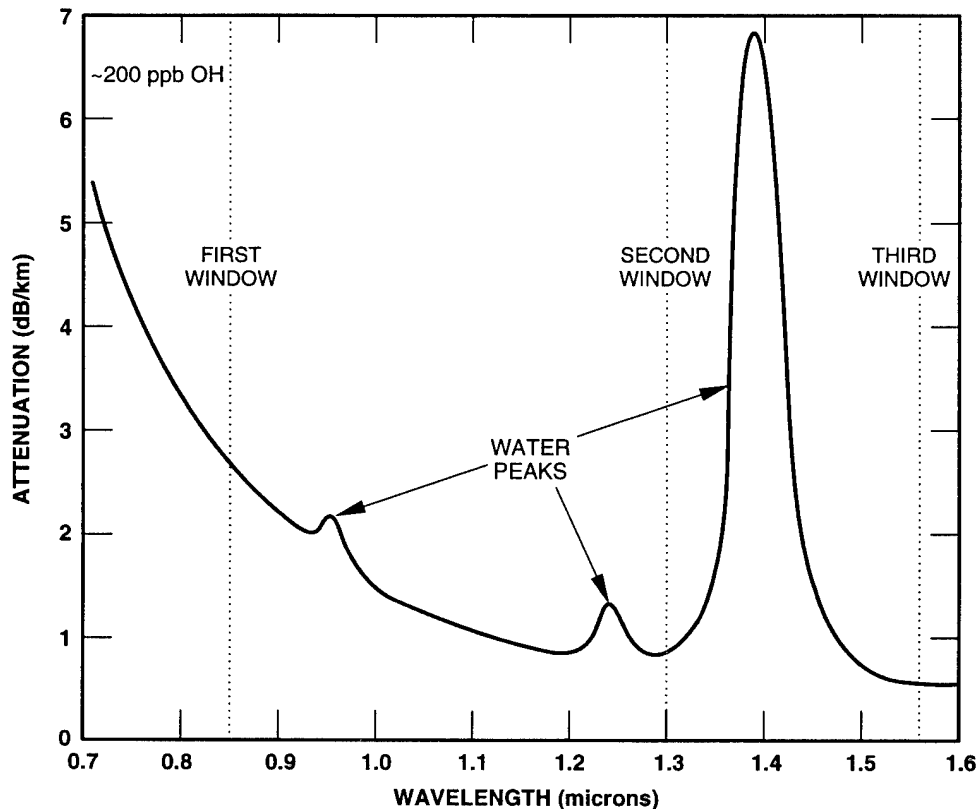


Figure 2-127. Attenuation in a moderate-water-content fiber (Morrow, 1986).

refraction indices is required. It follows, then, that the core and cladding must be of different materials. For the case of plastic-clad silica (PCS) core fibers, or for all-silica fibers, dopants that alter the refractive index in the appropriate direction must be added to the glass, but yet not significantly increase the attenuation in the fibers. Because impurity content can dramatically affect radiation response, the particular method used to achieve the proper index difference is of critical importance to hardened-fiber technology. As it turns out, most glass dopants, such as the most popular one, germanium (Ge), raise the index of silica and thus must be used to dope the core of the fiber. The implications of this for radiation hardness will be discussed in more detail later in this section. The ultimate goal, from both commercial and rad-hard points of view, has been to produce an all-silica fiber with an exceedingly pure core and a doped cladding. Only within the last decade or so has this goal been closely approached. One of the problems has been that very few dopants that lower the refractive index of silica, and thus that can be used to dope the cladding, are available. The emergence of fibers with pure silica cores and fluorine- and/or boron-doped cladding has resulted in all-glass fibers with excellent radiation resistance. The intrinsic and extrinsic effects on the radiation response of fiber optics are given in Table 2-9.

A fiber-optic waveguide consists of a core and its surrounding cladding; it can be constructed from various combinations of core and cladding. The core can be either pure silica or doped silica.

Pure silica provides good radiation hardness with a high intrinsic attenuation. Ge-doped silica has somewhat increased radiation sensitivity with low intrinsic attenuation and easier processing. Phosphorous (P) doping significantly increases radiation sensitivity and has somewhat higher intrinsic attenuation, but is much easier to process; it has decreased transient response and temperature dependence.

The cladding can also be pure or doped silica. Pure silica is difficult to process. Fluorine (F) or Ge/F doping provides adequate radiation hardness. P-doping also provides adequate radiation hardness, but with optimum ease of processing.

While a detailed discussion of fiber fabrication techniques is beyond the scope of this chapter, it is important to note that, as in the case of Si MOS devices, fabrication techniques can profoundly affect the radiation response of the fiber. Some of the pertinent aspects of fabrication are briefly addressed here. Essentially, the fabrication process involves formation of an appropriate glass preform, from which the fiber is then drawn in a draw tower. A variety of methods, such as outside vapor deposition (OVD, used by Corning) and plasma chemical vapor deposition (PCVD, used by AT&T), are available to fabricate a preform with the desired layers and dopants in place. The preform is then placed in a high-temperature furnace in the draw tower, as shown in the diagram of Figure 2-128. After the fiber is drawn, a coating is applied to the fiber and the fiber is wound on a

Table 2-9. Fiber-optic parameters that affect radiation response (Friebele *et al.*, 1991).

Fiber Parameters	System Parameters
Intrinsic	Wavelength (extrinsic)
Core and cladding material	Light intensity (bleaching)
Growth method	Temperature
Unknown impurities	Injection conditions (cladding modes)
Dopant type and combinations	Stress
Water (OH) content	Ambient atmosphere (plastic fibers)
Core diameter (fat fibers are more resistant)	

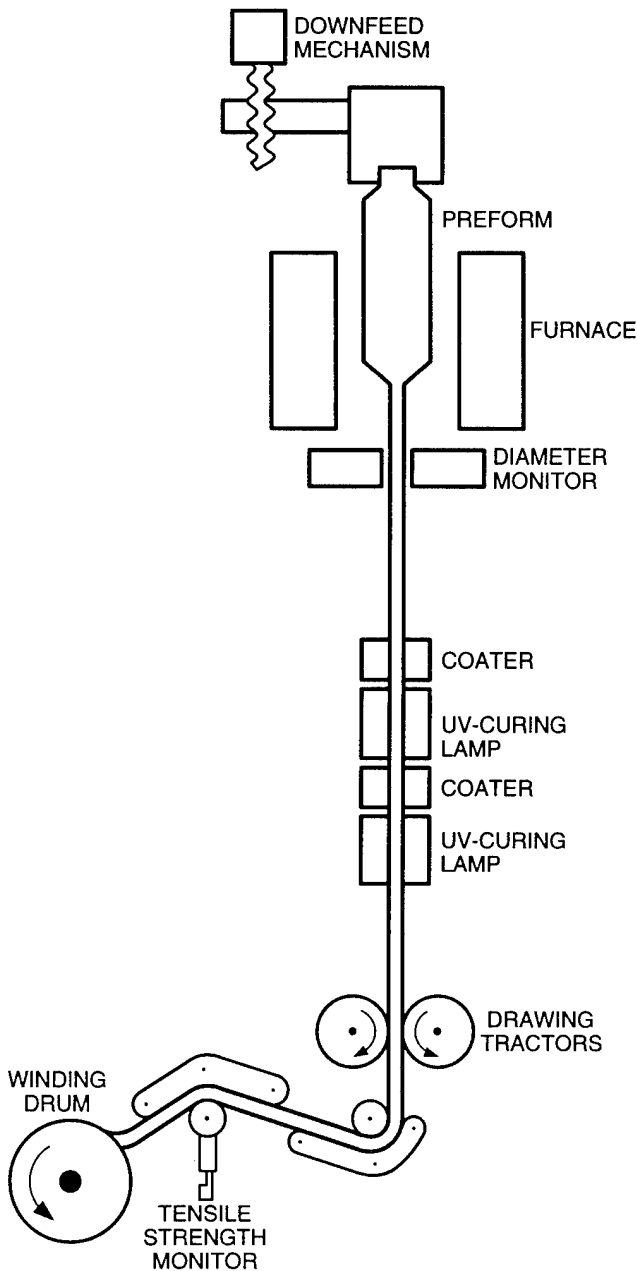


Figure 2-128. Schematic of a typical draw tower for optical fiber production (Morrow, 1986).

drum. The material properties of the preform and many of the parameters associated with the drawing process can affect the intrinsic absorption in the fiber as well as the response of the fiber to radiation. The furnace temperature profile, drawing speed, drawing tension, and the coating process are all influential. For example, the attenuation spectrum in Figure 2-129 shows a drawing-induced defect absorption band near $0.6 \mu\text{m}$ in a step-index fiber, which can affect the radiation response of the fiber. Perhaps

one of the most important points to note here is that preforms are in many cases manufactured by different companies than those that draw the fibers.

In general, for data transmission applications, losses in the range of 0.16 to 0.5 dB/km are insignificant since the link distances are at most 100 km. However, in the fiber gyroscope, coil lengths >1 km are used for accuracy, and the light may transit the coil a number of times. Thus, for this application, transmission loss is a much more serious problem and radiation-induced degradation must be minimal (e.g., <1 dB/km). For data-link applications, 5 dB is acceptable for 20- to 100-meter links (e.g., 50 to 250 dB/km).

For many military applications, the strength characteristics of the fiber are critical to useful system life. In addition, the mechanical properties of the fiber and the stresses that the fiber is placed under can affect both the intrinsic attenuation and the radiation response of the fiber. The actual strength of a fiber is determined by inherent flaws, which act as stress concentrators, and by the susceptibility of the surface to corrosion by moisture

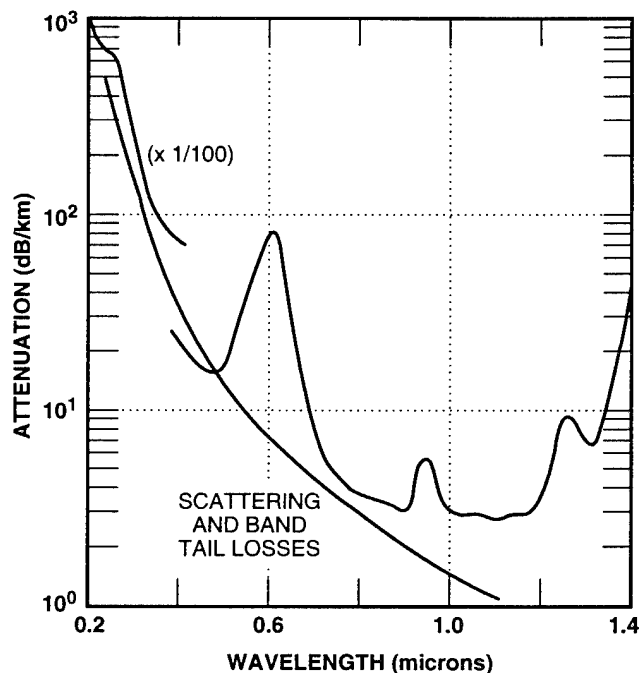


Figure 2-129. Drawing-induced defect absorption in an unirradiated step-index pure silica core fiber (Pinnow, 1973).

and other ambient elements. With appropriate coating and cabling techniques, fibers can be made that have very good strength for even highly stressful applications. Evidence for this is exhibited by the recent successes of various tethered weapon-development programs, such as the fiber-optic guided missile (FOGM) program.

Bending losses are also a serious source of problems under certain conditions. Macrobending loss, in which the fiber is wound or bent at a radius less than approximately 10 times the fiber diameter, can significantly increase the total intrinsic attenuation; in addition, it can result in more rapid radiation-induced accumulation of attenuation losses. Microbending losses, due to dimensional fluctuations along the core/cladding interface induced during drawing, can also affect attenuation and the susceptibility of the fiber to externally applied stresses. Finally, it is interesting to note that evidence from the recent recovery of the long-duration experiment facility (LDEF) space vehicle has

shown that micrometeorites can severely damage uncabled, exposed fibers in the space environment.

Regarding radiation effects in fibers, the analog of lattice damage effects in semiconductor devices, which is important in a neutron environment, is not particularly significant in fibers for typical neutron or proton requirements for military and space applications. The reason for this is that the glass structure is already a highly disordered structure and does not exhibit the perfection of the semiconductor lattice, which is so easily perturbed by lattice damage. Thus, the focus for radiation effects in fibers is transient and permanent attenuation induced by ionizing radiation. These effects are illustrated in Figure 2-130, which shows the change in transmitted optical signal level caused by a 1-krad dose from a 50-nsec-wide x-ray pulse. It is important to note that the time scale along the abscissa in Figure 2-130 is logarithmic and is not to scale; a typical radiation pulse width is 20 nsec. During irradiation, the signal level increases due to lumi-

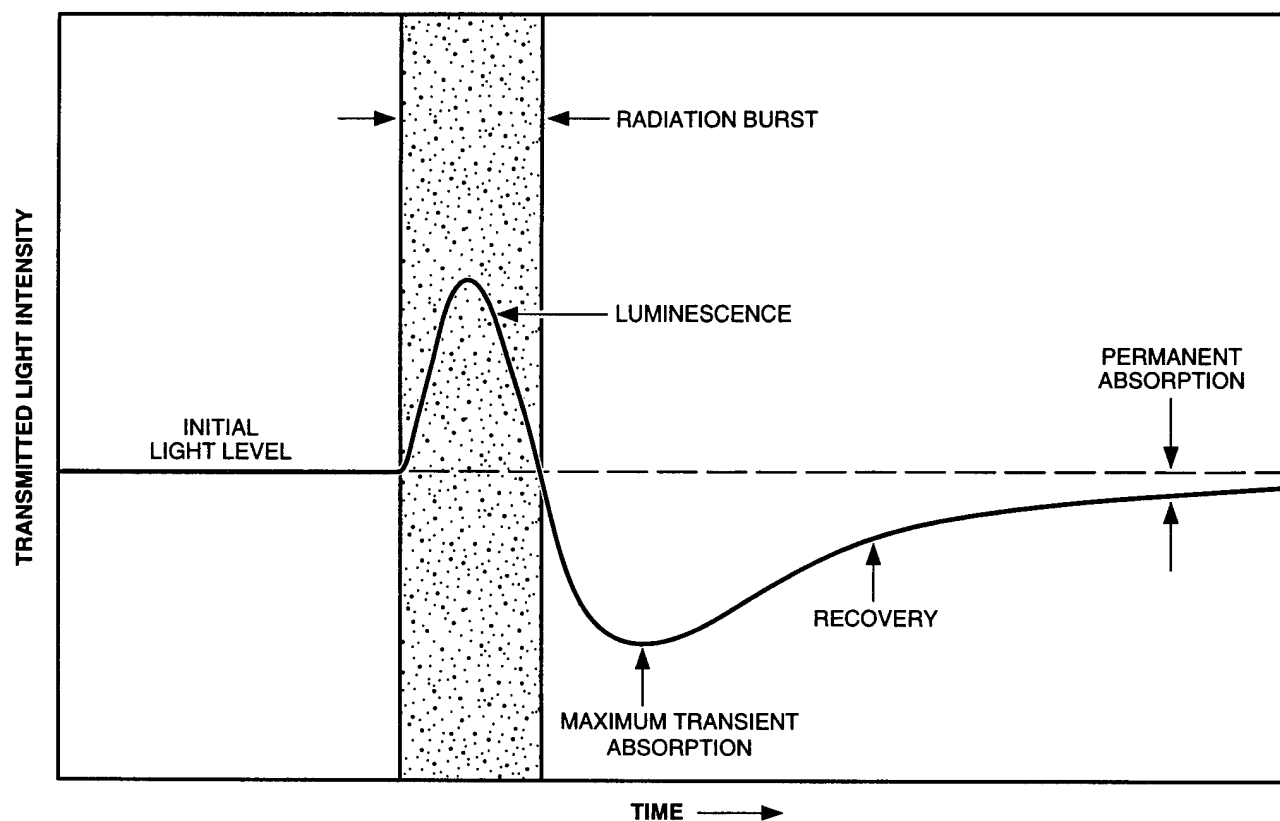


Figure 2-130. Schematic drawing of time-dependent effects in an optical fiber during and after exposure to ionizing radiation [the time scale is logarithmic] (Sigel and Evans, 1974).

nescence generated in the fiber. Immediately after the peak of the x-ray pulse, the signal level decreases and becomes less than the pre-irradiation level due to radiation-induced color-center absorption. The signal level continues to decrease for some time after the radiation pulse. The attenuation then anneals with time to some permanent value. Typically, the absorption remaining 24 hours after irradiation is considered "permanent." Consequently, the demarcation between "transient" and "permanent" attenuation is somewhat arbitrary and usually highly dependent on the ambient temperature.

The rate of growth of permanent ionizing-radiation-induced attenuation in fibers varies greatly, depending on the characteristics of the fiber. Early fibers fabricated from ordinary glasses like Pb-silicate exhibit very strong radiation-induced attenuation, as shown in Figure 2-131. Note that for these early data, results at the second and third windows are not even shown because at that time (mid-1970s) only the first window (near 0.85 μm) was used as an operating wavelength. Also, note that emission spectra of some LEDs are given, as well as Si detector responsivity. The fibers near the top of this figure show very rapid attenuation

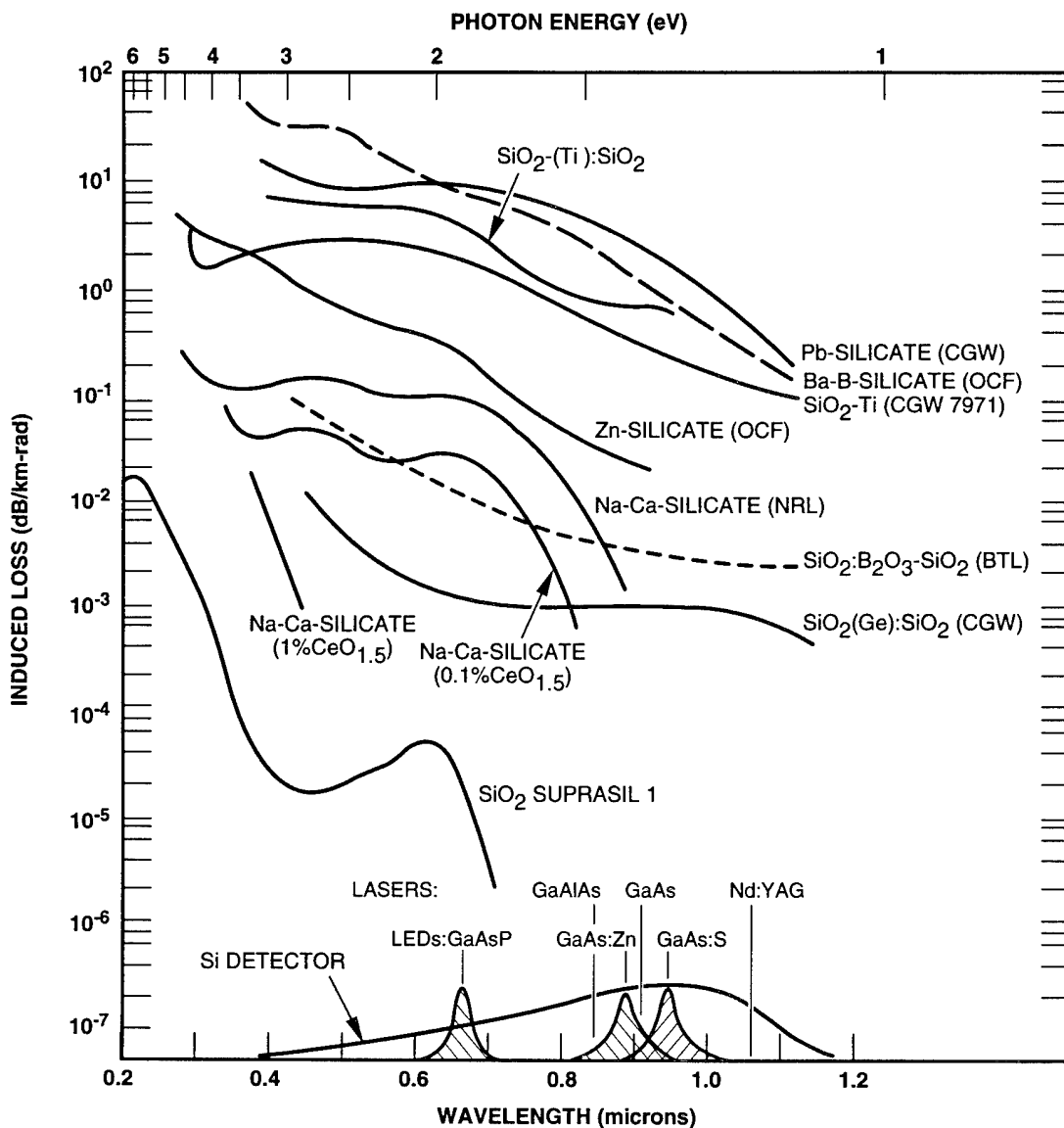


Figure 2-131. Comparison of ^{60}Co -induced attenuation in a variety of high- and low-loss fibers and glasses 1 hour after irradiation (Sigel and Evans, 1974).

buildup; the attenuation is normalized to dose so that these fibers exhibit more than 1 dB/km for each rad of exposure.

More recently, a great deal of progress has been made in developing radiation-hardened fibers, accompanied by the accumulation of a large body of data on radiation behavior of fibers. Several important features of the response of fibers to ^{60}Co -irradiation are shown in Figure 2-132 for both doped and undoped core fibers 1 hour after exposure to 100 krads. Since dopants are usually involved in the formation of various types of radiation-induced color centers, it is not surprising that the results in Figure 2-132 indicate a wide variation in induced loss, depending on the dopants in the fiber core [Suprasil and Suprasil W are pure core fibers]. The highest losses were observed in the multiply-doped fibers, while the lowest in-

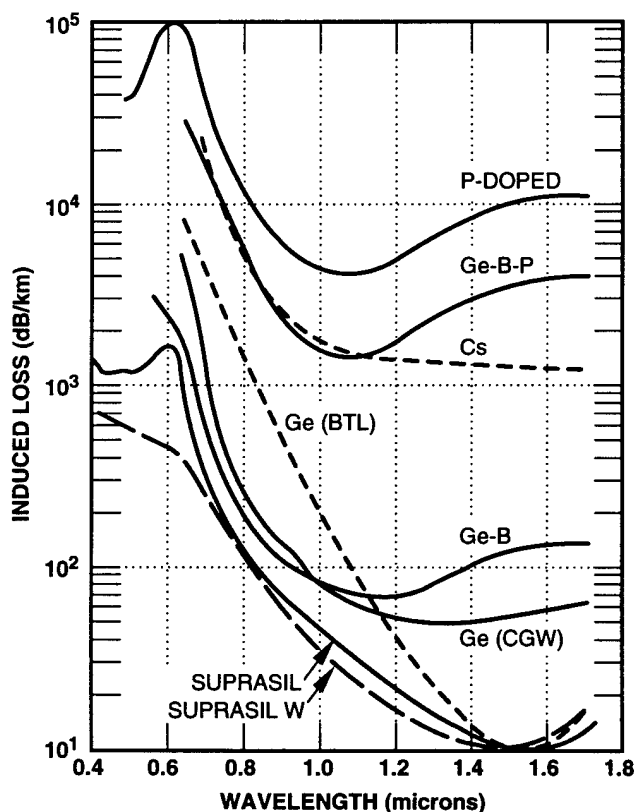


Figure 2-132. Induced attenuation spectra for a variety of doped and pure silica core fibers at room temperature 1 hour after 100 krads ^{60}Co -irradiation [note that both boron and phosphate doping increase the infrared attenuation] (Friebele and Gingerich, 1980).

duced attenuation is in the pure core fibers. Note that with the exception of the boron and phosphorus co-doped fibers, the loss is inversely proportional to wavelength. This can generally be attributed to the fact that the absorption peak for many color centers, in particular for the E'_1 center associated with Ge, is located in the ultraviolet (UV) portion of the spectrum. Thus, the general shape of the spectra in Figure 2-132 is due to the strong absorption tail from these centers in the UV.

Comparison of the Ge-doped Bell Telephone Laboratories (BTL, also AT&T) fiber with the Ge-doped Corning (CGW) fiber indicates that the dopant alone does not determine the fiber radiation response, a result that is not too surprising. Of particular interest is the fact that the BTL fiber has very low loss at 1.5 μm after 100 krads exposure. Present-day AT&T fibers are even better at this wavelength. One reason this is significant is because a graded-index fiber cannot be fabricated without using a core dopant [see Figure 2-124], and such fibers are an attractive compromise between multimode, step-index fibers and single-mode fibers. While the BTL fiber is comparable to the undoped core fibers at 1.5 μm , it is clear that for large radiation doses the undoped core fibers are definitely superior to Ge-doped fibers. The attenuation growth in the former is linear with dose to quite high doses, while the growth of attenuation for the latter fiber type is highly sublinear with dose. One result of this is that for low dose applications (less than a few krads), Ge-doped fibers actually experience less attenuation loss. The saturation of the attenuation with increasing dose in the undoped core fibers is a general characteristic of these fibers, and is responsible for their excellent radiation hardness at high doses.

An important process that takes place in fibers during and after ^{60}Co -irradiation (as suggested by the result in Figure 2-130) is color-center annealing. At low dose rates in pure core fibers, the recovery of attenuation during irradiation strongly mitigates the loss process and results in a rad-hard fiber. The competition between annealing and formation of an easily saturable color center, as for the RayChem fiber in Figure 2-133, can result in

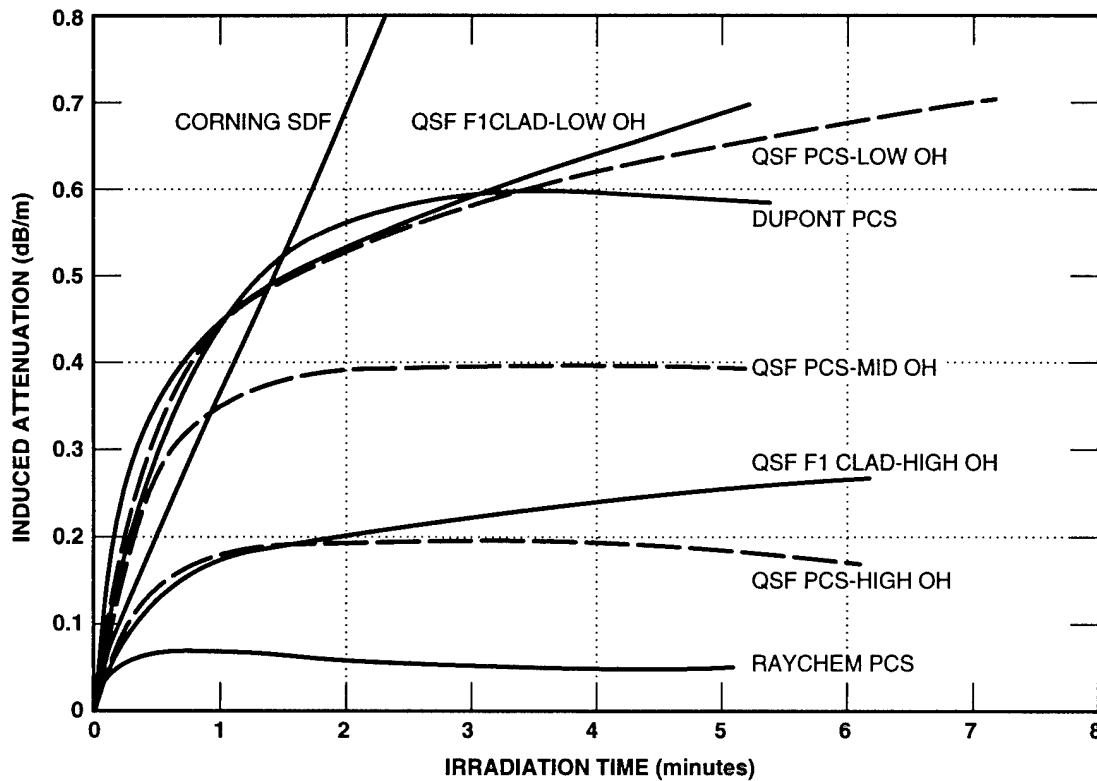


Figure 2-133. ^{60}Co -induced attenuation at -55°C and $0.82\ \mu\text{m}$ in a variety of pure core fibers clad with polymer (PCS) or fluorosilicate (F1), or a germanium-doped core (standard Corning fiber); dose rate = 4.1 krad/min (Barnes, 1982).

actual decreases in attenuation as irradiation proceeds. As might be expected, the balance between annealing and color-center growth depends on the dose rate so that the observed saturation level varies with dose rate. This general result is shown for pure-silica core fibers with different coating materials in Figure 2-134. Note that the saturation level for 300 rads/min is lower than that for the higher dose rate of 1,300 rads/min. For the polyimide-clad fiber, the extrapolated attenuation at 1 Mrad is well under 20 dB/km, indicating that this fiber has excellent radiation hardness. The variation in attenuation with coating type was a somewhat unexpected result. It was concluded that since the attenuation takes place in the fiber core, the variation with coating material was not due to the coating itself, but rather to the effect of the coating application process on the core characteristics.

Returning to Figure 2-133, an important feature of these data, related to annealing effects, is that they were all taken at -55°C , where the annealing rate is much less than at room temperature. Comparative results at different temperatures for a step-

index, pure core fiber are shown in Figure 2-135 for operation at $0.85\ \mu\text{m}$ and irradiation at 22 rads/sec. Note that the induced attenuation is much larger at -55°C and decreases with increasing temperature. Because of the greater annealing at 65°C , the saturation in the loss is reached at only a few krad. In general, as might be expected, the annealing rate is less at lower temperatures. However, not surprisingly, there is an important exception to this rule, as shown in Figure 2-136 for several different fibers operating at $0.8\ \mu\text{m}$ and irradiated to 2 krad at a rate of 95 rads/sec. Note that while most of the fibers show the expected behavior, the fibers containing phosphorus show the opposite effect; i.e., greater induced loss is experienced at higher temperatures. It was noted in the discussion of Figure 2-132 that P-doping caused fibers to have some unique properties in their response to irradiation. Generally, P-doped core fibers exhibit greater permanent radiation-induced attenuation, other things being equal, compared to similar fibers without phosphorus. However, as noted in the summary of

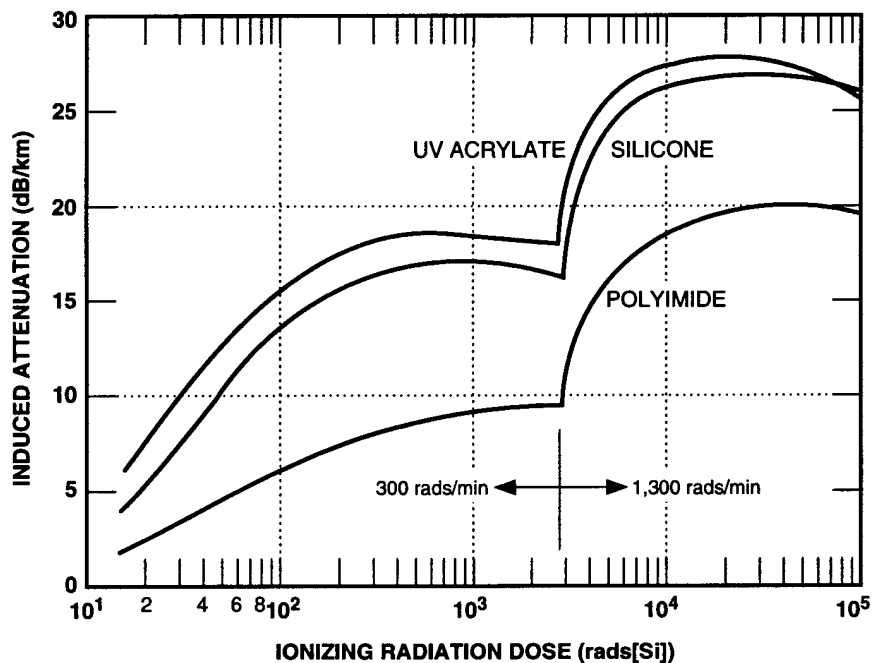


Figure 2-134. ⁶⁰Co-irradiation of pure silica core fibers illustrating the effect of fiber coating on radiation response (Barnes, Greenwell, and Nelson, 1987).

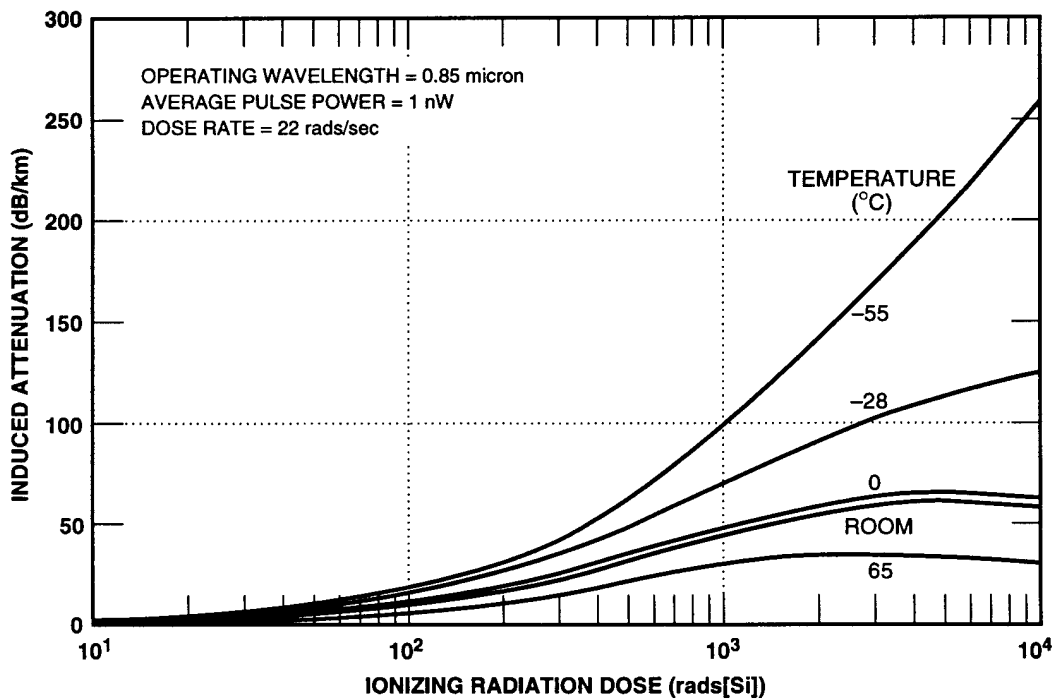


Figure 2-135. ⁶⁰Co-irradiation of step-index fibers at various temperatures (Greenwell, 1989).

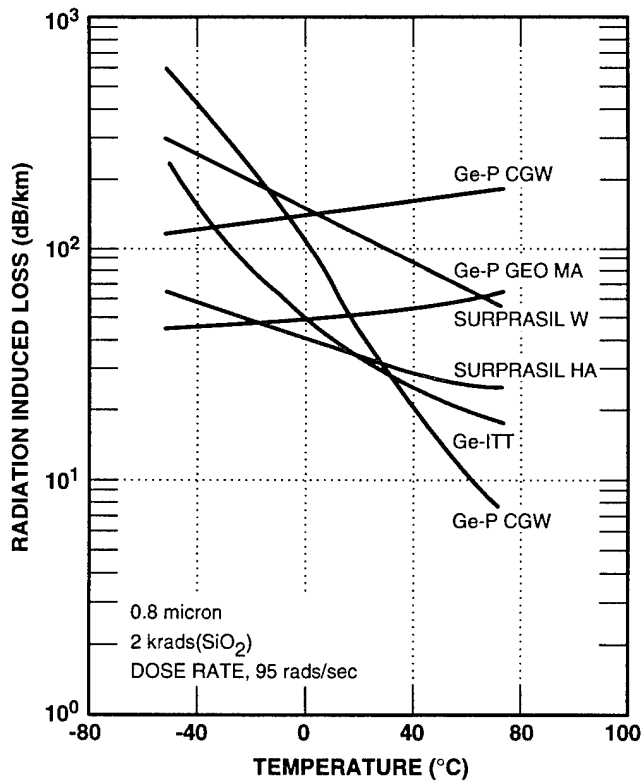


Figure 2-136. Effect of temperature on the ionizing-radiation-induced attenuation in various fibers (Share, 1981).

transient radiation effects [Subsection 2.11.4], phosphorus is not all bad; its presence in the fiber core kills the strong transient attenuation observed immediately after a radiation pulse [see Figure 2-130].

It was noted earlier that the OH absorption bands in the 0.8- to 1.6- μm range restrict fiber operation to certain wavelengths, commonly referred to as "windows." Thus, from the point of view of intrinsic losses, high OH content is undesirable. However, as shown in Figure 2-133, high-OH-content fibers exhibit less radiation-induced attenuation than low-OH-content fibers, and a compromise between these two effects must be made. It is noteworthy, however, that recently developed high-purity core fibers with low OH content have achieved hardness levels similar to those observed with high-OH fibers.

All of the radiation-induced attenuation data examined thus far in Figures 2-133 through 2-136 have been for fibers operating near 0.8 μm . In the discussion of the spectral loss data in Figure 2-132, it was noted that, with the exception of fibers containing boron and phosphorus, the induced losses were much less at longer wavelengths. This

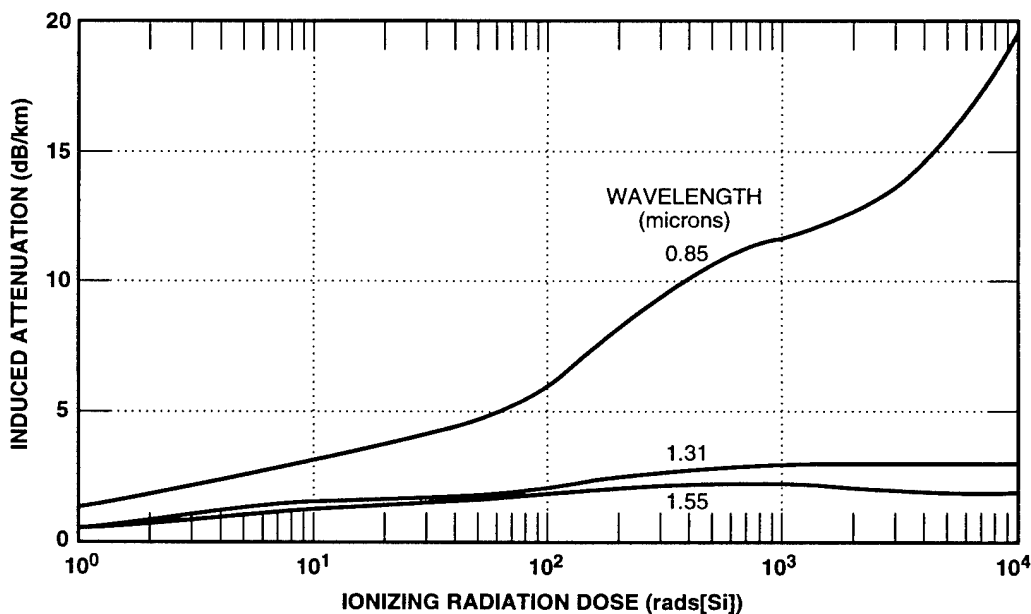


Figure 2-137. ⁶⁰Co-irradiation of single-mode fibers at 22 rads/sec showing induced attenuation at the first-, second-, and third-window wavelengths (Greenwell, 1989).

result is generally true, and is shown to be the case in Figure 2-137 for single-mode fibers ^{60}Co -irradiated at 22 rads/sec at room temperature. Note that a difference by a factor of about 10 exists in the induced attenuation at 10 krad between 0.85 and 1.55 μm . Thus, from the standpoint of radiation hardness, longer operating wavelengths are more desirable unless for some reason, the fiber must contain phosphorus [see Figure 2-132].

Thus far, pure-silica core fibers operating at long wavelengths have been observed to offer the greatest radiation hardness for exposure to steady-state ionizing radiation. In fact, further radiation resistance can be achieved in these fibers by taking advantage of photobleaching. In these fibers, it is possible to include additional color-center annealing by merely allowing the signal-generating LED or laser to remain on during and after the irradiation. The light-induced anneal of absorbing centers is termed photobleaching. While this is a significant process in pure core fibers even at the longest wavelength of the third window (1.55 μm), it is

only a minimal effect in Ge-doped fibers. Photobleaching also offers the possibility of compensating for the lack of annealing that occurs at lower operating temperatures. An example of this effect is shown in Figure 2-138 for a pure-silica core fiber operating at -55°C and 0.872 μm . Both irradiation and recovery curves are shown as a function of light power level present in the fiber during irradiation and anneal. [A dBm is defined as $10 \log (P/1 \text{ mW})$, i.e., the log of the LED power normalized to a reference power of 1 mW.] Note that at very low powers, the induced loss is high, but that at the maximum power level, the attenuation at 10 krad is less by a factor of about 7. Hence, by turning on the LED, annealing similar to that at higher temperature can be achieved during irradiation.

A relationship that describes the recovery of the radiation-induced attenuation of single-mode optical fibers has been developed by Friebele *et al.*, (1991). This relationship is made possible due to the significant correlation between certain optical fiber fabrication parameters of matched-clad,

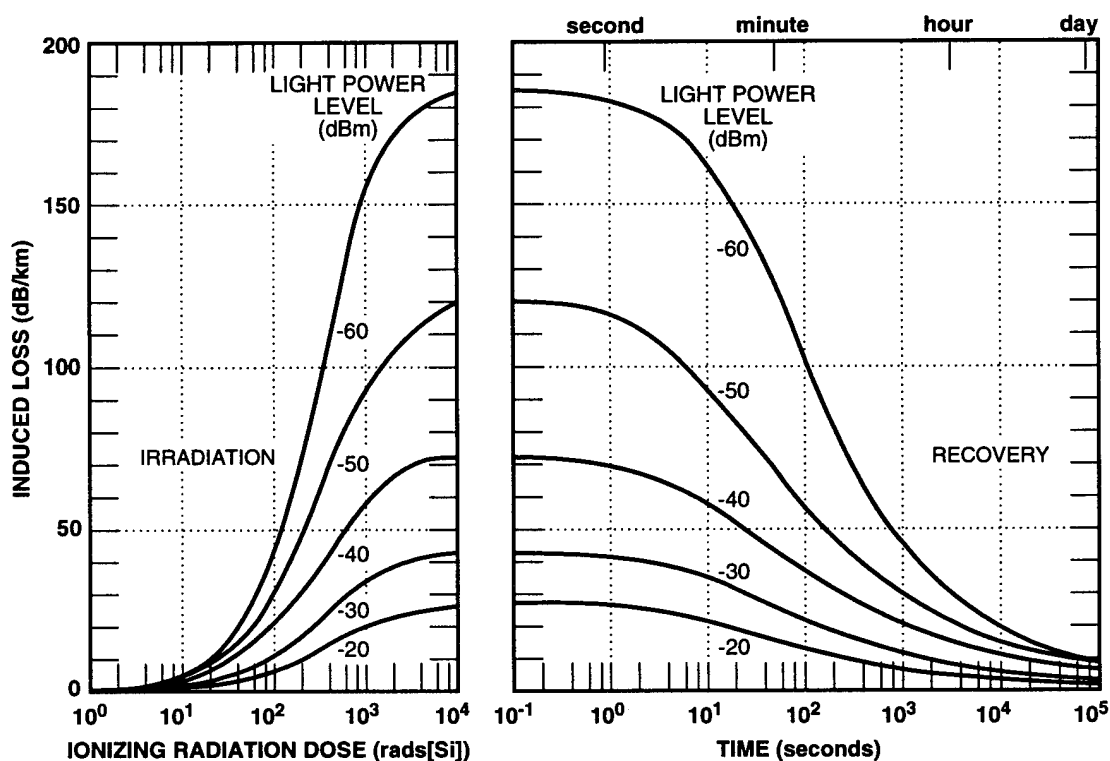


Figure 2-138. Radiation-induced loss in a single-mode, low-OH fiber during irradiation at -55°C and after irradiation to 10 krad(Si) (1,300 rads[Si]/min) at several light output power levels at 0.872 μm (Evans, 1988).

single-mode fibers and the induced attenuation and recovery kinetics following exposure to ionizing radiation. The equation depicting this attenuation and recovery is:

$$A_o = (A_o - A_f)(1 - ct)^{-x} + A_f, \quad (2.26)$$

where:

- A_o = initial attenuation
- A_f = final attenuation
- c = $(1/\tau)[(2)^{1/x} - 1]$ (where τ is the half-life of incremental loss)
- τ = time
- x = $1/(n-1)$ (where n is the kinetic order of recovery).

Excellent agreement between the data and the curve fit has been obtained for a number of optical fibers, as shown in Figures 2-139 and 2-140. This relationship has made it possible to predict the radiation-induced response of an optical fiber from a knowledge of the fiber's fabrication parameters.

2.11.3 Radiation Environments

Two radiation environments — natural space and a nuclear-weapon-enhanced space environment — are discussed here and their impact on optical fibers addressed.

2.11.3.1 Natural Space Environment

The slow accumulation of ionizing radiation dose to tens of krads(Si) at low dose rates* will not significantly affect any optoelectronic components except for the optical fiber. Even in the case of fibers, if a prudent choice of a rad-hard fiber is made and the optimum operating wavelength of 1.3 μm is employed [1.55 μm is also good if no phosphorus is in the fiber core], the losses will not constitute fiber-optic system failure, even for fiber lengths approaching 1 km. At low dose rates, a pure core fiber such as the one shown in Figure 2-134 will exhibit a saturation in induced attenuation at low levels of attenuation. As noted earlier, the dynamic balance between color-center growth and anneal is responsible for this saturation effect. Thus, as the dose rate decreases the net attenuation will also decrease.

In summary, it can be stated that the natural space environment for ionizing radiation dose considerations is not particularly difficult to satisfy if a properly chosen fiber-optic system is employed.

2.11.3.2 Strategic Radiation (Combined Nuclear Weapons and Natural Space) Environment

Depending on the particular military program, strategic radiation requirements can vary significantly. Due to prompt gamma rays and other

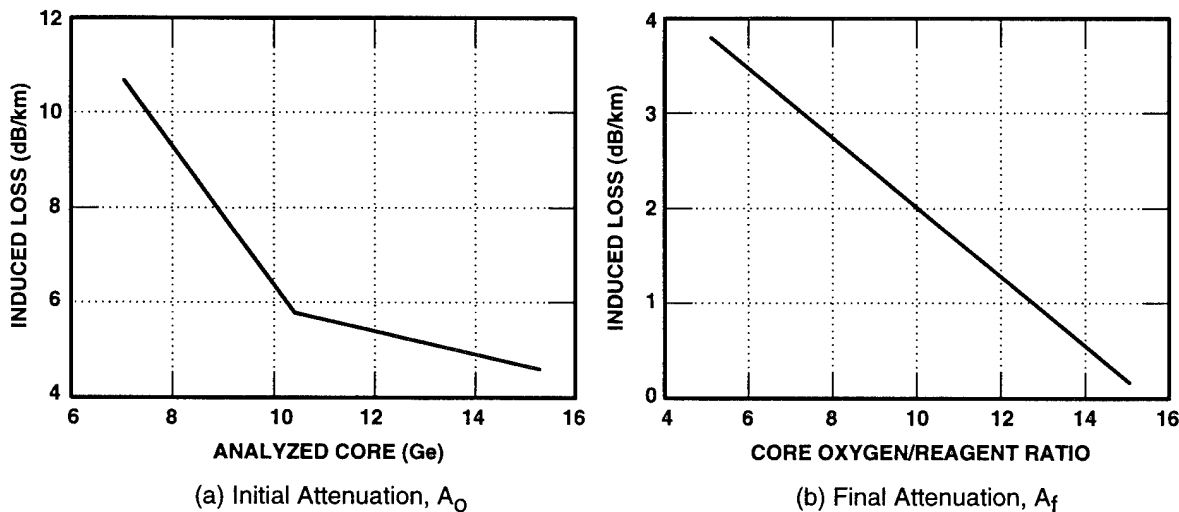


Figure 2-139. Estimated effects of initial and final attenuation on core (Ge) and oxygen-to-reagent ratio used during core deposition (Friebele *et al.*, 1991).

*Solar flare dose rates for protons can reach 1 rad(Si)/sec, but these rates last for a maximum of 1 day, usually less.

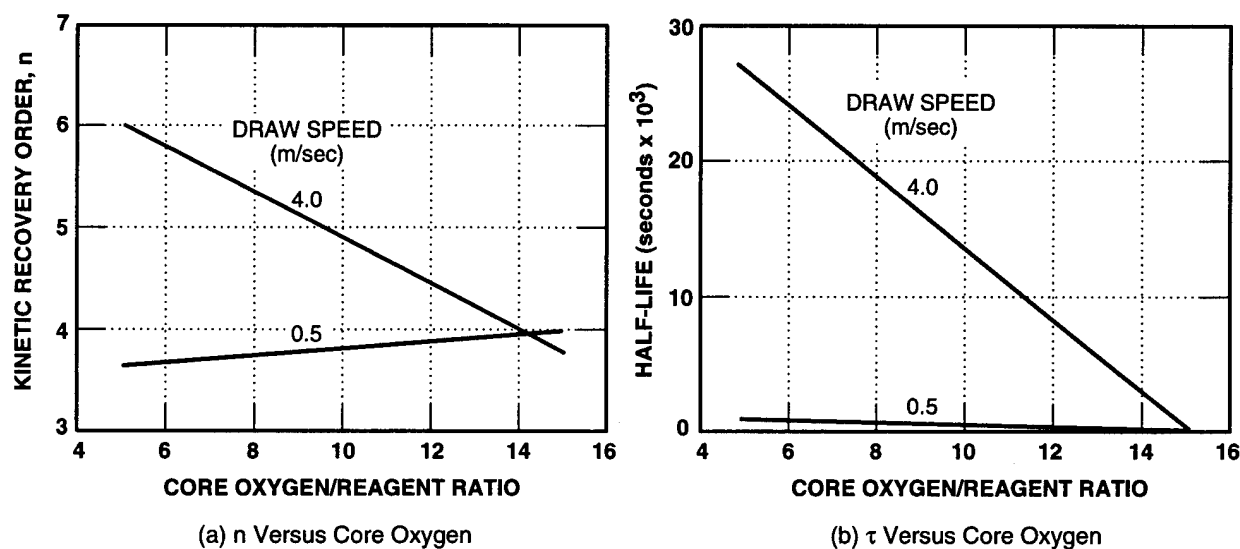


Figure 2-140. Estimated effect of kinetic recovery order and half-life of incremental loss on the two-way interaction of core oxygen-to-reagent ratio and draw speed (Friebele, *et al.*, 1991).

sources of ionizing radiation released during the detonation of a nuclear weapon, the ionizing radiation dose requirement of 0.1 to 1 Mrad(Si) is much more stringent than that from the natural space environment. In addition to the Si integrated circuits in transmitters and receivers, these dose levels can pose serious problems for optical fibers. If doped core fiber, such as a Ge-doped core telecommunications fiber, is used and the fiber is relatively long (100 meters to 1 km), then the attenuation will continue to increase linearly with dose as shown in Figure 2-133 and can become prohibitively large in a long fiber. Thus, a pure core fiber must be employed, if possible, so that the saturation effects

shown in Figures 2-133 and 2-134 can be taken advantage of in the application. For large ionizing radiation dose requirements, an operating wavelength of 1.3 or 1.55 μm should be chosen and the fiber core should not contain any phosphorus. In addition, the fiber should have polyimide as a primary coating because this improves the ionizing radiation dose hardness; if the coating is permanent, the polyimide increases reliability. Finally, the fiber-optic system should be examined for any epoxies or lenses in the light path that can darken easily. If the material darkens very easily, as some epoxies do, and the dose is very large (1 Mrad[Si]), then such optical elements should be avoided.

Table 2-10. Impact of system requirements on fiber choice.

System Requirements	Fiber Behavior	Candidates ^a
Minimum down time (<1 msec)	Minimum transient absorption	SiO ₂ core (PCS, all glass)
High ionizing dose (unmanned — missile, satellite)		SiO ₂ core, Ge-P-doped silica core
Moderate ionizing dose (manned — aircraft, ground links)		SiO ₂ core (Ge-doped silica core without P), silicate plus Ge, plastic
Low to moderate dose rate (1 second down time) (manned — fallout, reactor environs, space ambient)	Good long-term recovery	SiO ₂ core (F-doped silica or polymer clad), binary Ge-doped silica core — SiO ₂ clad
Neutron flux (weapons, reactor)	Boron-free core and cladding	

Note: ^aChoice depends upon system architecture, attenuation, and bandwidth requirements.

2.11.4 Summary

A few important conclusions summarize radiation effects on fibers:

1. Considerable progress has been made in developing radiation-hardened fibers; these fibers are now available.
2. No single fiber type will optimally satisfy all performance and environmental requirements. Thus, the system performance requirements and the environmental requirements must be defined before a fiber can be selected. Table 2-10 relates cable selection criteria.
3. An undoped core fiber (which eliminates graded-index fibers) with a high OH content and a polyimide buffer coating most closely satisfies all environmental requirements.

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CHAPTER 3

IONIZING DOSE RATE EFFECTS ON SEMICONDUCTOR MICROELECTRONICS

3.1 Diode Transient Radiation Response

Transient ionizing dose effects include "dose-rate," or "gamma-dot ($\dot{\gamma}$)," phenomena as well as single-event phenomena. Dose-rate phenomena are usually associated with x-ray and gamma-ray radiation produced by the detonation of nuclear weapons, which can subject an entire system (including active and passive electronic devices and the associated packaging and mounting – *e.g.*, printed circuit board–material) to ionizing radiation. One specific effect of the transient radiation is to generate very high hole-electron densities that result in photocurrents in semiconductor devices. These photocurrents can engender a number of deleterious effects, ranging from temporary upset to burnout (destruction) of an integrated circuit (IC).

In general, the threat addressed in this chapter is the result of relatively short radiation pulses, 40 nsec to 1 μ sec in duration, with high dose-rate values (*e.g.*, $>10^9$ rads/sec). The most common units for expressing the amplitude of the dose-rate exposure are rads(M)/sec, where M refers to the material absorbing the radiation. Single-event phenomena (SEP) are generally expressed in terms of critical charge (Q_c) at a junction in Coulombs, and the linear energy transfer (LET) expressed in MeV-cm²/g.

The following, more detailed, discussion of these transient ionizing dose effects will initially concentrate on the response of discrete devices, *e.g.*, diodes, silicon bipolar transistors, metal-

oxide semiconductor field-effect transistors (MOSFETs), and gallium arsenide FETs. The discussion is then extended to address the response of complex integrated circuits, *e.g.*, static random access memories (SRAMs), microprocessors, etc.

The key to understanding photocurrent production is understanding the radiation response of a reverse-biased pn junction. Simply stated, the photocurrents in a reverse-biased junction are the sum of three distinct components (Wirth and Rogers, 1964), and can be separated into (1) minority-carrier hole transport across the junction from the n-type silicon, (2) minority-carrier electron transport across the junction from the p-type silicon, and (3) the current resulting from electron-hole pair generation in the depletion region. Minority carriers are transported by diffusive transport and electric-field-aided drift.

Physically, the photoresponse is the result of carrier generation throughout the diode at a rate

$$G = g_0 \dot{\gamma} \text{ hole-electron pairs/cm}^3\text{-sec} , \quad (3.1)$$

where g_0 is the generation constant (4.2×10^{13} hole pairs/cm³-rads[Si]), and $\dot{\gamma}$ is the absorbed dose rate in the bulk semiconductor of the diode in rads(Si)/sec.

The two critical concepts in diode photoresponse are the physics of the generation of primary photocurrent and the concept of a carrier collection volume around the pn junction, which determines the magnitude of the photocurrent.

When the diode junction is reverse-biased, a large electric field is established in the junction, which sweeps minority carriers across the depletion region and holds the minority-carrier density at the edges of the junction close to zero [see Figure 3-1(a)]. Far from the junction (*i.e.*, many minority-carrier diffusion lengths), the radiation-induced carrier generation and minority-carrier recombination are in steady-state equilibrium.

The hole and electron carriers generated in the depletion region constitute a current that is in phase with the incident transient radiation pulse. This prompt photocurrent I_p flows from the n- to the p-region since holes are swept into the p-region and electrons into the n-region.

On the average, only carriers within one diffusion length, *i.e.*, $L_n = (D_n \tau_n)^{1/2}$, on each side of the junction are collected, where D_n = carrier diffusion constant and τ_n = carrier lifetime. Carriers beyond one diffusion length have a high probability of recombining before reaching the junction and contribute little to the photocurrent.

Because of the increase in minority-carrier density gradients at the junction due to the onset

of the radiation pulse, the corresponding diffusion gradients increase, thereby enhancing the diffusion of carriers toward the junction. Thus, a portion of the carriers remote from the junction diffuse toward and reach the junction with a corresponding delay time. This current is often called the delayed component of photocurrent, I_d . Both I_p and I_d are transient currents superimposed on the usual leakage currents.

In the case of the forward-biased junction, the applied bias does not completely cancel the depletion-region field potential. Hence, an electric field is still maintained in the junction neighborhood, so that a prompt photocurrent will flow from the n- to the p-region. As seen in Figure 3-1(b), the carriers produced in the bulk material decrease the carrier density gradient at the junction, resulting in a decrease in the forward conduction current. The total current can now be defined as the normal conduction current plus the prompt and delayed photocurrents that flow from the n- to the p-region.

The excess minority-carrier densities in the p-region are

$$\Delta n = g_0 \dot{\gamma} t_n, \quad (3.2)$$

and in the n-region are

$$\Delta p = g_0 \dot{\gamma} t_p. \quad (3.3)$$

With an increase in carrier densities far from the junction and the densities held to zero at the junction, carrier diffusion will cause an increased diode current in the reverse direction. To a good first-order approximation, the low-voltage reverse-biased photocurrent can be included in parallel with a dc electrical model of the diode, as shown in Figure 3-2. If the electrical model of the diode includes conductivity modulation as well as reverse breakdown, the radiation-inclusive model represents the overall photoresponse of the diode over a wide range of dc conditions.

An explicit solution of the photocurrent flowing across the junction is difficult to obtain since it requires solving the continuity equation, with excess minority-carrier concentration and lifetime and electric field in the quasi-neutral region dependent on each other. However, a closed solution can be generated if simplifying assumptions

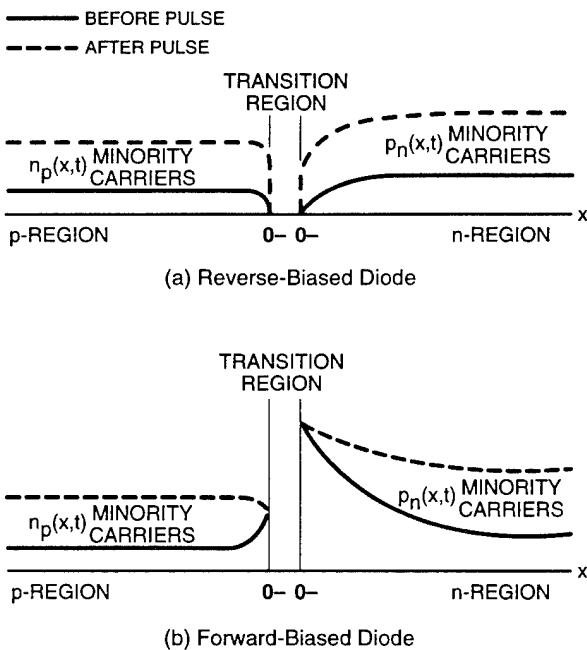


Figure 3-1(a, b). pn junction minority-carrier densities prior to and immediately after an incident pulse of ionizing radiation (Wirth and Rogers, 1964).

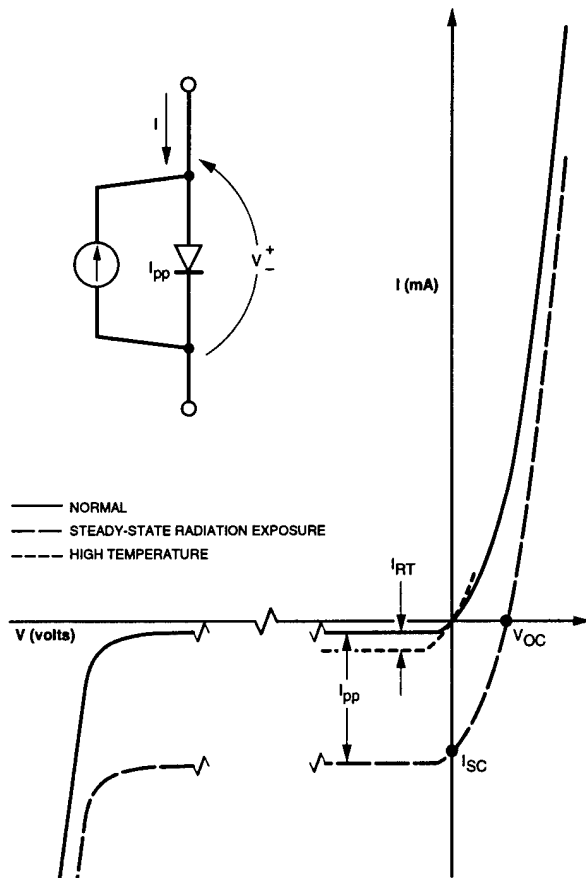


Figure 3-2. pn junction diode radiation-inclusive, steady-state current-voltage (I-V) characteristic (Raymond, 1985).

are made such that: (1) the diode has one-dimensional geometry, (2) no conductivity modulation exists, (3) the diode has negligible electric field and is uniformly doped except at the junction, and (4) the voltage across the junction is constant.

Based on these assumptions and for a constant applied bias V_0 to the junction, the resulting relationship for the total primary photocurrent, $I_{pp} = I_p + I_d$, is

$$I_{pp}(t) = eA \left[W_t G + \frac{1}{\sqrt{\pi}} \int_0^t G(t-u) \times \left(\sqrt{D_n} e^{-u/\tau_n} + \sqrt{D_p} e^{-u/\tau_p} \right) \frac{du}{u} \right]. \quad (3.4)$$

For the case of present interest, that of a rectangular ionizing radiation pulse of amplitude $G = g_0 \dot{\gamma}$ and width t_p , Equation 3.4 reduces to

$$I_{pp} = eAG \left[W_t + L_n \operatorname{erf} \left(\sqrt{t/\tau_n} \right) + L_p \operatorname{erf} \left(\sqrt{t/\tau_p} \right) \right]; \quad 0 \leq t \leq t_p, \quad (3.5a)$$

and

$$I_{pp} = eAG \left(L_n \left\{ \operatorname{erf} \left[\sqrt{t/\tau_n} \right] - \operatorname{erf} \left[\sqrt{(t-t_p)/\tau_n} \right] \right\} - L_p \left\{ \operatorname{erf} \left[\sqrt{t/\tau_p} \right] - \operatorname{erf} \left[\sqrt{(t-t_p)/\tau_p} \right] \right\} \right); \quad t > t_p, \quad (3.5b)$$

where

e = electron charge

A = junction area (cm^{-2})

$G = g_0 \dot{\gamma}$

g_0 = generation constant for the material

$\dot{\gamma}$ = dose rate ($\text{rads}[\text{Si}]/\text{sec}$)

W_t = depletion-region width (cm)

L_n = diffusion length (cm) for electrons = $(D_n \tau_n)^{1/2}$

t = time

L_p = diffusion length (cm) for holes = $(D_p \tau_p)^{1/2}$

t_p = radiation pulse width

and

$$\operatorname{erf}(x) = 2 \int_0^x \exp^{-y^2} dy / \pi^{1/2}.$$

The depletion-region width W_t represents the prompt-component collection length; the sum of the error function (erf) terms represents the delayed, diffusion-component collection length. Figure 3-3 depicts the primary photocurrent

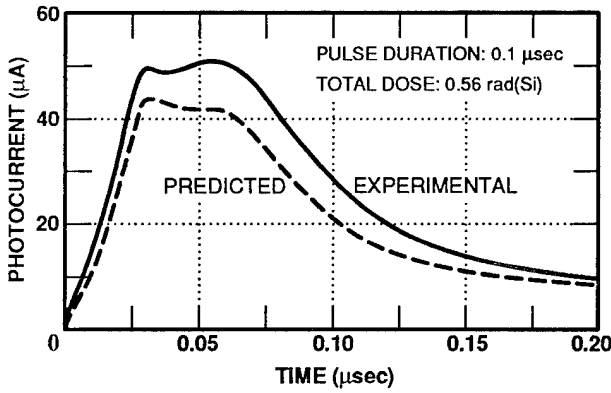


Figure 3-3. Primary photocurrent for the 2N2051 collector-base junction (Wirth and Rogers, 1964).

obtained from Equation 3.5 and compares it with that obtained from experimental flash x-ray data.

For very short radiation pulse widths, where t_p is very small compared with the minority-carrier lifetimes τ_p and τ_n , then from Equation 3.5, the photocurrent is given by

$$I_{pp}(t) = I_p(t) = eAW_t G(t); \quad 0 \leq t \leq t_p, \quad (3.6a)$$

and

$$I_{pp}(t) = I_d(t) = \frac{eAGt_p}{\sqrt{\pi t}} \left(\sqrt{D_n} e^{-t/\tau_n} + \sqrt{D_p} e^{-t/\tau_p} \right); \quad t > t_p. \quad (3.6b)$$

The product Gt_p is the total photocurrent carrier density generated during the incident radiation pulse and, of course, is proportional to the total incident dose. In many devices, τ_p and τ_n are small, and corresponding terms in Equation 3.6 can be neglected. For steady-state photocurrent, such as from nuclear power reactor gamma rays, it can be seen from the previous discussion that the steady-state photocurrent I_{ss} is given from Equation 3.5a (unbounded time) as

$$I_{ss} = eAG_{ss} (W_t + L_p + L_n), \quad (3.7a)$$

$$G_{ss} = g_o \dot{\gamma}_{ss}. \quad (3.7b)$$

Subsequent to the development of the Wirth-Rogers model [Equations 3.5 through 3.7], an enhanced model (Enlow and Alexander, 1988) was developed that provides a more accurate representation of some devices because it includes the effect of the electric field in the quasi-neutral region and high-injection effects on minority-carrier lifetime. The difference in the prediction of a diode response between the enhanced and the Wirth-Rogers models is shown in Figure 3-4. The cause of the difference is the result of an effective increase in photocurrent collection volume, which is engendered by the inclusion of electric field and high-injection excess minority carriers. Figure 3-5 compares predicted and measured response for two diodes using the enhanced model.

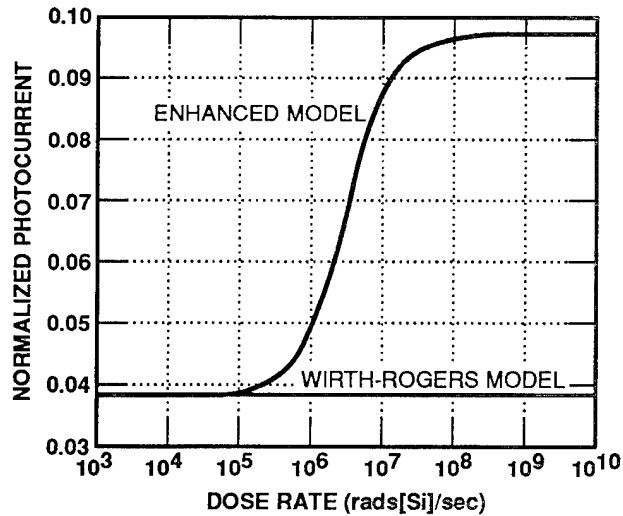


Figure 3-4. Normalized photocurrent as a function of dose rate, demonstrating the nonlinearity of the enhanced photocurrent model (Enlow and Alexander, 1988).

3.2 Diode Transient Radiation Response

Further insight concerning the transient radiation response of a diode may be obtained by considering an equivalent circuit that will provide an approximate model of this response. The development of this model is the primary objective of this section.

Extension of the diode model to the transient photoresponse is essentially a modification of the electrical model to include transient effects and

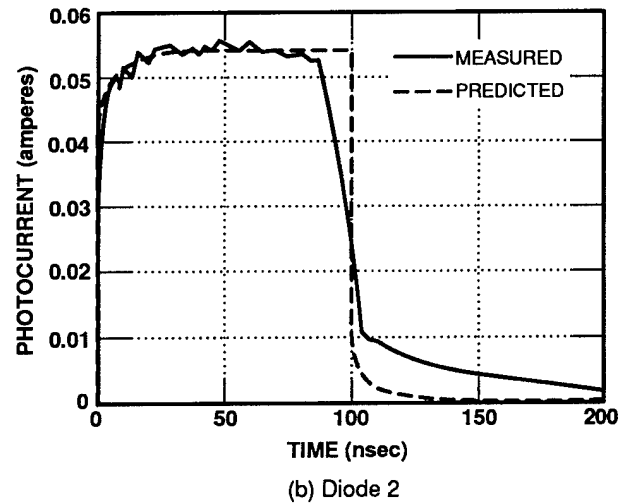
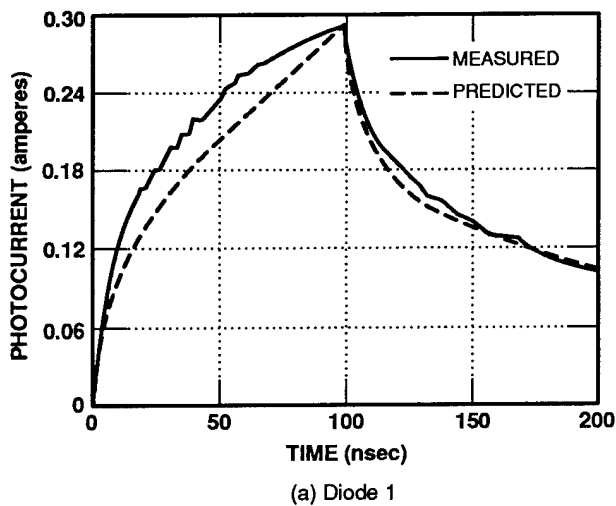


Figure 3-5 (a, b). Measure and predicted waveforms (100 nsec) normalized to the peak of the measured waveform at 5.0×10^9 rads (Si)/sec (Enlow and Alexander, 1988).

the definition of a time-dependent primary photocurrent, as shown in Figure 3-6. The accuracy of the model depends principally on the accuracy of the electrical model parameters. The time dependence of the reverse-biased diode photocurrent $I_{pp}(t)$ is determined by delays associated with carrier motion to and through the junction. As with the diode steady-state photocurrent, the key concepts are the first-order, radiation-inclusive diode model and the effective carrier-collection volumes that determine the magnitude of the diode photocurrent. The magnitude and time dependence of the diode photocurrent is the composite of depletion layer and bulk semiconductor effects.

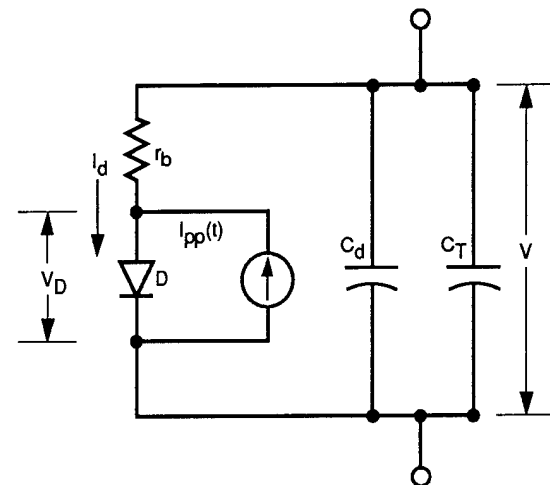
Carriers generated in the depletion region will essentially be swept out immediately ($t < 1$ nsec) and represent the prompt photocurrent component that essentially follows the radiation pulse,

$$I_p(t) = qG(t)W_t(V)A \quad (3.8)$$

Since the depletion layer width is a function of the reverse-bias voltage, circuit effects on the voltage may modulate the photocurrent.

Carriers that diffuse to the junction from a long, uniformly doped bulk region exhibit an error-function time dependence of the form

$$I_d(t) = qG(t)AL \operatorname{erf}(t/\tau)^{1/2}, \quad (3.9)$$



$$I_d = I_s [\exp(qV_D/mkT) - 1]$$

$$C_d = \text{DIFFUSION CAPACITANCE} = f(I_d)$$

$$C_T = \text{DEPLETION CAPACITANCE} = f(V_D)$$

$$I_{pp}(t) = \text{REVERSE-BIASED PHOTOCURRENT} = f(\gamma, V_D)$$

$$r_b = \text{DIODE BODY RESISTANCE}$$

$$I_s = \text{REVERSE SATURATION CURRENT}$$

Figure 3-6. Radiation-inclusive diode transient model (Raymond, 1982).

(where L is the length of the bulk region) in response to a step function in radiation intensity $\dot{\gamma}u(t)$ (Brown, 1960). The decay of this diffusion

component following the end of a square radiation pulse is

$$I_d(t-t_p) = q g_o \dot{\gamma} u(t-t_p) \times A \operatorname{Lerf}\left(\frac{t_p}{t}\right)^{1/2} \times \left[1 - \operatorname{erf}\left(\frac{t-t_p}{\tau}\right)^{1/2}\right], \quad (3.10)$$

for $t > t_p$.

Typically, the peak photocurrent of an ideal p^+n diode is the sum of a large but slow diffusion component from the long, lightly doped n -region, a smaller but fast component from the depletion layer, and a small and relatively fast diffusion component from the heavily doped p^+ -region. A diode photocurrent response with prompt and diffusion components is shown in Figure 3-7. The dashed line shows the response if the radiation is cut off at some time — a pulse rather than a step function. The error function is shown in Figure 3-8 for convenient reference.

The time-dependent photocurrent is a relatively complex function for an arbitrarily shaped radiation pulse. Fortunately, it can be approximated for radiation pulses that are either long or short compared to the minority lifetime. The longest photoresponse will be approximately equal to the steady-state photocurrent. If the radiation pulse is short compared to the minority-carrier lifetime, the peak diffusion photocurrent from a long, uniformly doped semiconductor region can be approximated as

$$I_d(\text{peak}) = e g_o \dot{\gamma} A \frac{2}{\sqrt{\pi}} \sqrt{D\tau_p} \quad (3.11)$$

The variation in peak diffusion photocurrent with the radiation pulse width is shown in Figure 3-9. In terms of an effective collection volume for the narrow-pulse approximation, the pulse width t_p replaces the lifetime τ with an increase of about 13 percent in the coefficient for the small-argument approximation of the error function. The approximate lifetime can be based on the ap-

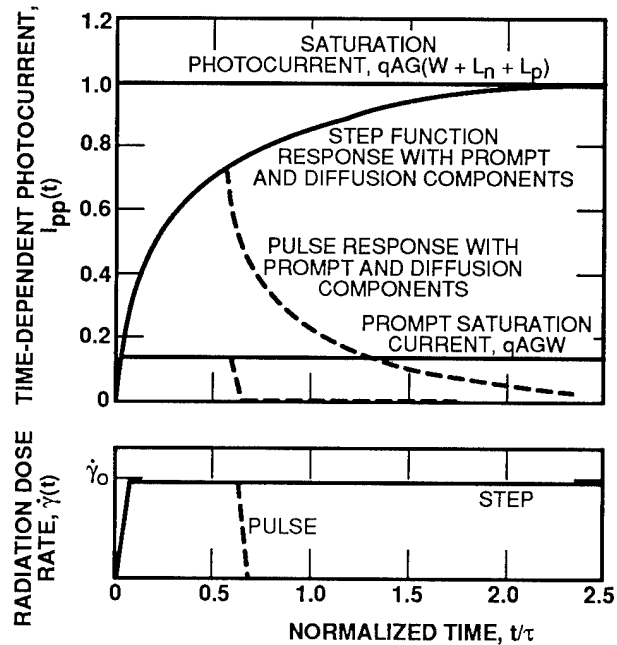


Figure 3-7. Ideal diode photocurrent response (Raymond, 1985).

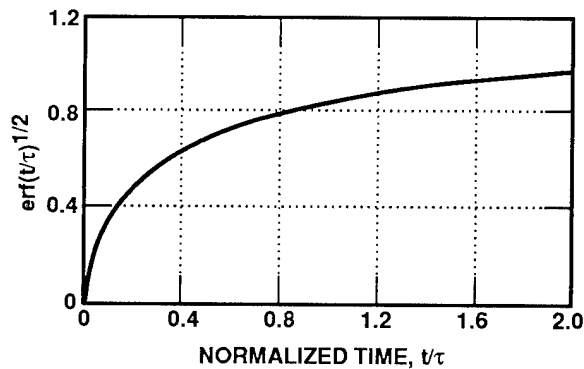


Figure 3-8. Error function of $(t/\tau)^{1/2}$ versus t/τ (Raymond, 1985).

proximate value inferred from the diode electrical recovery time.

For a p^+n diode, the lifetime and volume of the p^+ -region might be small compared to the radiation pulse width, while comparatively long for the n -region. In this case, the peak diode photocurrent is expressed as

$$I_{pp}(\text{peak}) \cong q g_o \dot{\gamma} A \left[(D_n \tau_n)^{1/2} + W_t + \frac{2}{\sqrt{\pi}} (D_p \tau_p)^{1/2} \right], \quad (3.12)$$

where $(D_n \tau_n)^{1/2}$ is the diffusion carrier collection length for the p^+ -region, W_t is the depletion layer width, and the last term of the equation is the effective carrier collection length in the n -region.

The expressions for transient photocurrent have been based on carrier diffusion from uniformly doped regions. The presence of the built-in field due to variations in doping level modifies the carrier collection volume and time dependence of the transient photocurrent.

In some circuit applications, the circuit time constants are long compared to the total photocurrent pulse width. In this case, the total charge Q_{pp} in the photocurrent pulse is the critical circuit parameter. For a narrow-pulse exposure of the p^+n diode, this charge can be expressed as

$$Q_{pp} = qGA \left[(D_n \tau_n)^{1/2} + W + (D_p \tau_p)^{1/2} \right] t_p \quad (3.13)$$

At high pulsed-ionizing-radiation levels it can be assumed that the magnitude of the diode pho-

to-current generator still increases with radiation intensity despite limitation of the diode current by the circuit. In this case, the diode saturates and is internally forward-biased by the photocurrent. The diode recovery time can be determined by considering the time-dependent photocurrent as the forward-biased current, and the circuit currents as the reverse current.

It is a misconception to assume that the photocurrents "short out" a diode during a high-level radiation exposure. The difference between the "shorting" concept and the true diode recovery behavior can be critical in a survivable circuit design.

The diode/circuit photoresponse at extremely high-intensity ionizing radiation exposure can result in sufficient power dissipation to cause permanent damage. Damage may be a result of either metallization or junction burnout in a single-junction diode. The energy required to damage a diode has been established by extensive characterizations using electrical overstress. The energy necessary to cause device damage is

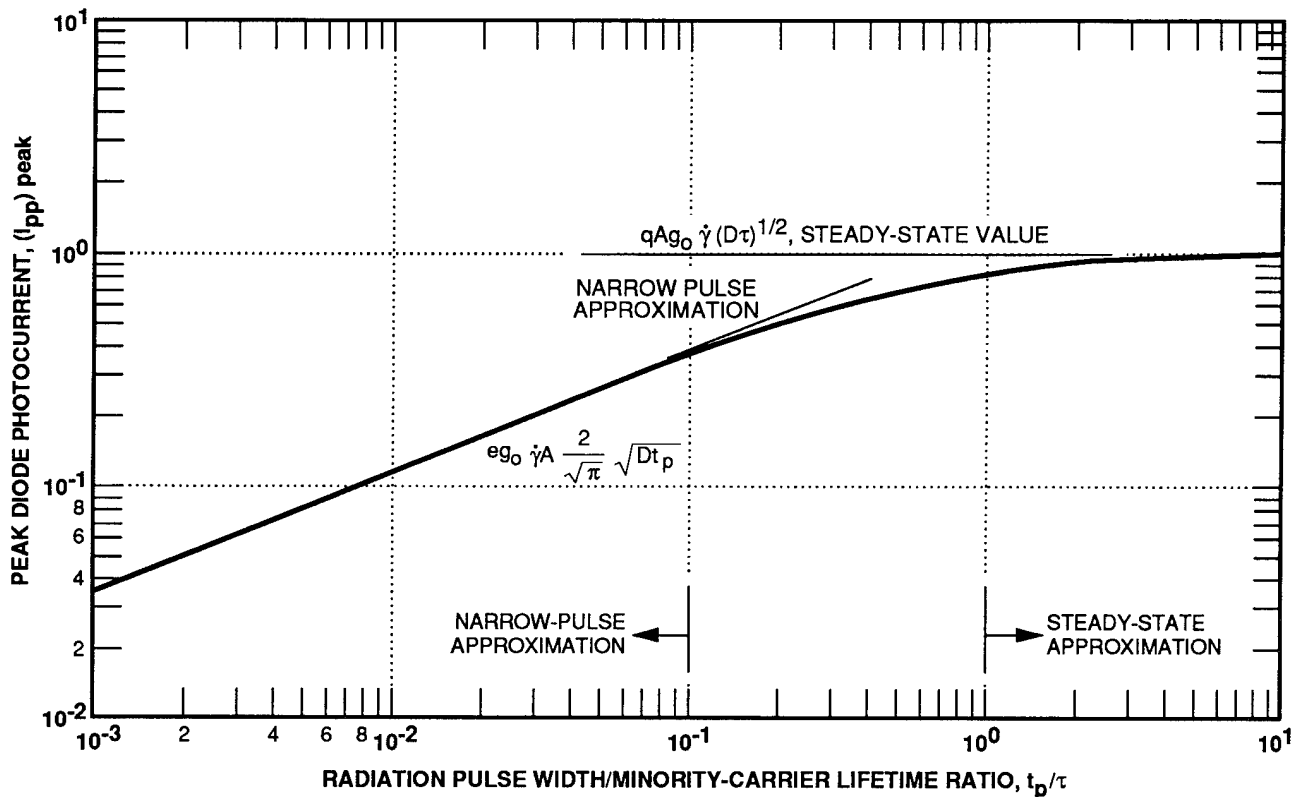


Figure 3-9. Peak diode photocurrent as a function of radiation pulse width (Espig, 1985).

much greater than that directly absorbed from the radiation environment. Diode burnout then depends on energy absorbed from the associated circuitry and its power supplies.

The most sensitive configuration for diode burnout is with a reverse-biased diode connected between the supply voltage and ground [Figure 3-10]. Power dissipation in the diode resulting from a high-intensity ionizing-radiation pulse will be:

$$P_d \equiv v_d I_{pp}(t) + [I_{pp}(t)]^2 r_b, \quad (3.14a)$$

$$P_d = VI_{pp}(t), \quad (3.14b)$$

where r_b is the diode body resistance, v_d is the diode junction voltage, and V is the diode reverse voltage. The approximate radiation exposure necessary to damage a diode in this configuration can be calculated by assuming that the current pulse is the peak photocurrent for the duration of the radiation pulse. For a p^+n diode, the photocurrent contribution is principally for the n -region and the depletion layer. For the condition where the radiation pulse width is short compared to the n -region lifetime, the peak photocurrent is

$$I_{pp}(\text{peak}) = q A g_o \dot{\gamma} \left(W_t + \frac{2}{\sqrt{\pi}} \times \sqrt{D_p \tau_p} \right). \quad (3.15)$$

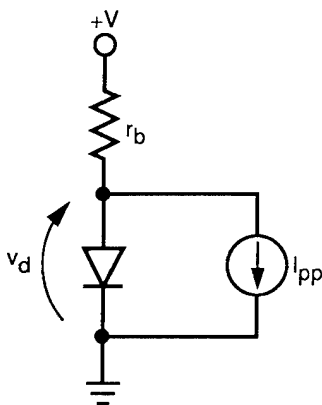


Figure 3-10. Diode burnout equivalent circuit (Raymond, 1985).

The worst case for the diode would be the maximum reverse bias, which, in this case, would be just below the breakdown voltage. Assuming that the critical burnout energy is the same as that determined from electrical overstress data, the critical radiation dose rate for burnout can be defined as shown in Figure 3-11. Junction area does not enter into the calculation since the assumed variations of both photocurrent and burnout energy increase linearly with junction area. Results shown in Figure 3-11 are not intended to define diode burnout value accurately for any specific diode, but rather to indicate the approximate levels of concern.

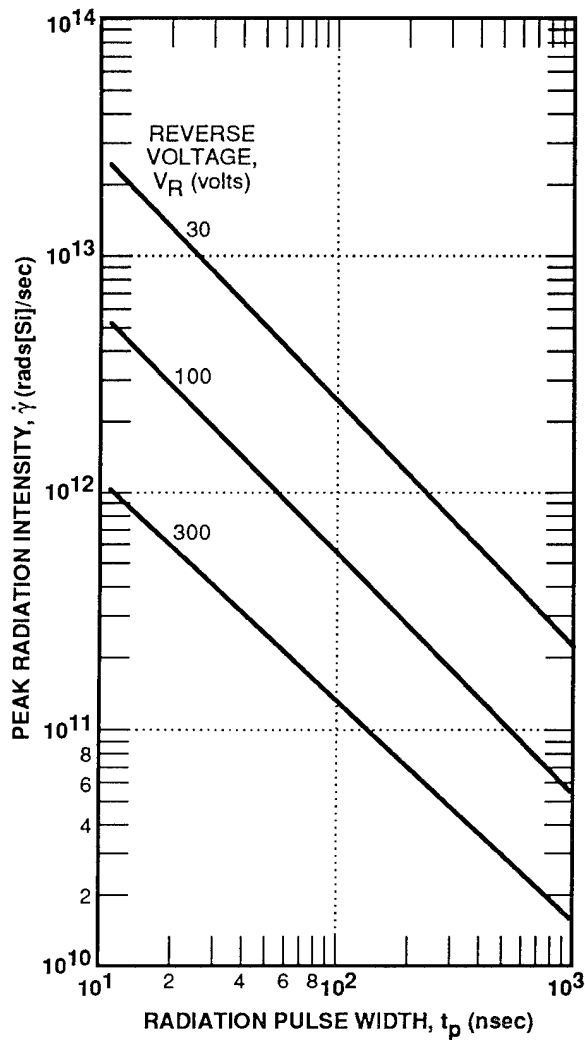


Figure 3-11. Radiation intensity versus radiation pulse width for burnout threshold (Espig, 1985).

3.3 Transient Ionizing Radiation Response of Bipolar Transistors

3.3.1 Photocurrent Modeling

A bipolar transistor may be envisioned as being comprised of two interconnected diodes: one normally operated in the forward-biased region, forming the emitter-base junction; and one normally operated in the reverse-biased region, forming the base-collector junction. Thus, the information provided in Section 3.2 can be used to characterize and model the radiation response of bipolar transistors.

For the purposes of discussion, consider an npn transistor connected in the grounded emitter configuration and biased in its active region (Wirth and Rogers, 1964). If it is irradiated, the resulting hole-electron pairs will diffuse and drift across each junction in a manner analogous to that discussed for a single diode: prompt currents will be caused by carrier generation in each depletion region, and delayed currents will be caused by the diffusion of minority carriers from one region to another. For an npn transistor, electrons diffuse out of the base layer and holes are injected into it from the adjoining regions. These currents are called the primary photocurrents. The hole current entering the base is amplified by current gain of the device and results in a collector current transient in addition to the collector component of the primary photocurrent. The amplified component of the collector current transient is called the secondary photocurrent.

An exact expression for the secondary photocurrent would be very complicated if it included carrier redistribution times, recombination processes, and the effects of a three-dimensional geometry. Fortunately, assumptions can be made to yield simple expressions that are useful in understanding the mechanisms involved and in making reasonably accurate estimates of actual device response. The two most important assumptions are that the charge-control model (Beaufoy and Sparkes, 1957) is applicable and that the device has one-dimensional geometry. Although the charge-control model used does not adequately handle events that change very rapidly with time, it is suitable for a study of the buildup and decay

of the collector currents at times later than about one base-layer transit time. In order to simplify the mathematics and obtain analytic solutions for the collector current response, it was also necessary to consider the external base circuit of the transistor as an open circuit to changes in base voltage caused by radiation. A simplified version of the analysis and the final equations follow.

Beaufoy and Sparkes (1957) proposed a charge-control model of a transistor wherein the excess minority-carrier charge $Q(t)$ in transit across the base region is given by

$$\frac{dQ(t)}{dt} = - \left[\frac{Q(t)}{\tau_b} \right] \equiv I(t) , \quad (3.16)$$

where $I(t)$ is the majority-carrier current entering the base region and τ_b is the base-layer minority-carrier lifetime. The collector current is given by

$$I_c(t) = \frac{h_{FE}}{\tau_b} Q(t) , \quad (3.17)$$

where h_{FE} is the transistor common-emitter current gain. These relations are good approximations to the more exact continuity-diffusion equation models when the following conditions are assumed to be satisfied:

1. The transistor is operated in the active region,
2. Time variations of the base and collector current and, in this case, the radiation intensity are small during one base transit time,
3. The transistor has a one-dimensional geometry,
4. The base region is either field free or has an impurity grading such that the built-in electric field $E(x)$ has the form $[D_d F(x)/dx]/\mu[F(x)]$, where D and μ are the diffusion and mobility constants, respectively, for minority carriers and $F(x)$ is an arbitrary function.

The following analysis also assumes that the collector voltage and the base current are constant, and therefore the collector depletion-layer capacitance and external circuit parameters need not be considered.

The emitter depletion capacitance is also ignored in this analysis in order to obtain a linear

model and closed-form solutions. This is a valid approximation for many devices that are operated in the active region because the change in the charge accumulated on the emitter depletion capacitance during the radiation pulse is small compared to changes in Q . While this approximation is valid for the devices discussed in the text, it can lead to significant errors when considering very-high-frequency devices or when a device is operated at or near cutoff.

In an ionizing radiation environment, the base majority-carrier current $i(t)$ has six components: (1) a diffusion component from the collector, (2) a collector junction depletion-region component, (3) an emitter junction depletion-region component, (4) a component resulting from carrier generation within the base region, (5) a diffusion current from the emitter, and (6) the normal base current. The analytical form of components (1) through (3) have been presented in Section 3.2, and the development of components (4) and (5) are provided in Wirth and Rogers (1964). The result is:

$$I_b(t) = -Q/\tau_b + i_1 + i_2 + i_3 + i_4 + i_5 + i_6. \quad (3.18)$$

If the emitter efficiency is assumed to be unity, the ratio p_{no}/n_{po} is small, and the current corresponding to several forms of carrier generation rate are given below.

For a step function of magnitude G at $t = 0$,

$$\begin{aligned} I_c(t) = qAG & \left[W_b + W_{sc} + \sqrt{D_p \tau_c} \operatorname{erf} \left(\sqrt{\frac{t}{\tau_c}} \right) \right. \\ & + h_{FE} \left\{ (W_b + W_{sc} + W_{se}) (1 - e^{-t/\tau_b}) \right. \\ & + \sqrt{D_p \tau_e} \operatorname{erf} \left(\sqrt{\frac{t}{\tau_e}} \right) - \sqrt{\frac{D_p}{(1/\tau_e - 1/\tau_b)}} e^{-t/\tau_b} \\ & \times \operatorname{erf} \left[\sqrt{t \left(\frac{1}{\tau_e} - \frac{1}{\tau_b} \right)} \right] + \sqrt{D_p \tau_c} \operatorname{erf} \left(\sqrt{\frac{t}{\tau_c}} \right) \\ & \left. \left. - \sqrt{\frac{D_p}{(1/\tau_c - 1/\tau_b)}} e^{-t/\tau_b} \times \operatorname{erf} \left[\sqrt{t \left(\frac{1}{\tau_c} - \frac{1}{\tau_b} \right)} \right] \right\} \right] \quad (3.19) \end{aligned}$$

For steady-state conditions of Equation 3.19,

$$\begin{aligned} I_c = qAG & \left[W_b + W_{sc} + \sqrt{D_p \tau_c} \right. \\ & + h_{FE} (W_b + W_{sc} + W_{se} \\ & \left. + \sqrt{D_p \tau_c} + \sqrt{D_p \tau_e}) \right]. \quad (3.20) \end{aligned}$$

For a rectangular pulse of magnitude G and duration T , a solution can be obtained directly from Equation 3.19 by superpositioning two step functions of opposite sign, one delayed by an amount T . The response for an arbitrary generation rate of duration T , where T is very short compared to device time constants, is

$$\begin{aligned} I_c(t) = qA(W_b + W_{sc})g(t) + qA \frac{h_{FE}}{\tau_b} \\ \times (W_b + W_{sc} + W_{se}) \\ \times \int_0^t g(\lambda) d\lambda, \quad 0 \leq t \leq T; \quad (3.21) \end{aligned}$$

and

$$\begin{aligned} I_c(t) = qA \int_0^T g(\lambda) d\lambda & \left[\frac{(D_p)^{1/2}}{(\pi t)^{1/2}} e^{-t/\tau_c} + \frac{h_{FE}}{\tau_b} \right. \\ & \times e^{-t/\tau_b} \left\{ W_b + W_{sc} + W_{se} + \frac{(D_p)^{1/2}}{\sqrt{\frac{1}{\tau_e} - \frac{1}{\tau_b}}} \right. \\ & \times \operatorname{erf} \left[\sqrt{\left(\frac{1}{\tau_e} - \frac{1}{\tau_b} \right) t} \right] + \frac{(D_p)^{1/2}}{\sqrt{\frac{1}{\tau_c} - \frac{1}{\tau_b}}} \\ & \left. \left. \times \operatorname{erf} \left[\sqrt{\left(\frac{1}{\tau_c} - \frac{1}{\tau_b} \right) t} \right] \right\} \right], \quad (3.22) \end{aligned}$$

for $T < t$. The total collector current in Equation 3.21 is the sum of primary and secondary components, which can be distinguished by the presence of the amplification factor h_{FE} . During the radiation pulse, electrons (for an npn transistor) generated in the base and collector depletion re-

gions diffuse to the collector region and constitute a primary photocurrent given by the first term in Equation 3.21. As these electrons are collected, holes are accumulated in the base region and, according to the charge-control model, produce the secondary photocurrent given by the last term in Equation 3.21. After the termination of the short radiation pulse, holes generated in the collector and emitter regions, within one diffusion length of the junctions, diffuse into the base. The collector component of this primary photocurrent is described by the first term in Equation 3.22. The secondary photocurrent defined by the last term in Equation 3.22 results from the buildup and recombination of excess holes, which are generated directly within the base region or injected into the base from the collector and emitter regions. The photocurrent predicted by Equation 3.21 can be constructed rapidly by using Figure 3-12, where the product of $\exp(-t/\tau_b)$ and the error function terms is presented in normalized form.

The accuracy of the model, described by Equations 3.19 through 3.21, is depicted in Figures 3-13 and 3-14, where the measured and pre-

dicted responses are in good agreement. At higher doses, the peak collector current becomes a nonlinear function of dose because of the effects of the electric field in the collector region. The difference between measured data and predicted response in this region is attributed to differences between the actual collector resistivity of the device and the nominal value of resistivity used in the calculation.

In some devices, the common emitter current gain decreases significantly with increasing collector current because the base-spreading resistance produces a nonuniform bias condition on the base-emitter junction (emitter crowding). Since radiation-induced carriers are generated uniformly in the base region and are injected over the entire collector junction area, emitter crowding is not as severe as that which occurs if a corresponding number of carriers are injected from the base lead. Therefore, at high current levels, errors are introduced in predictions because the effective current gain of the transistor may be higher than the measured current gain.

Equations 3.21 and 3.22 were derived on the basis that the collector region was field-free, and

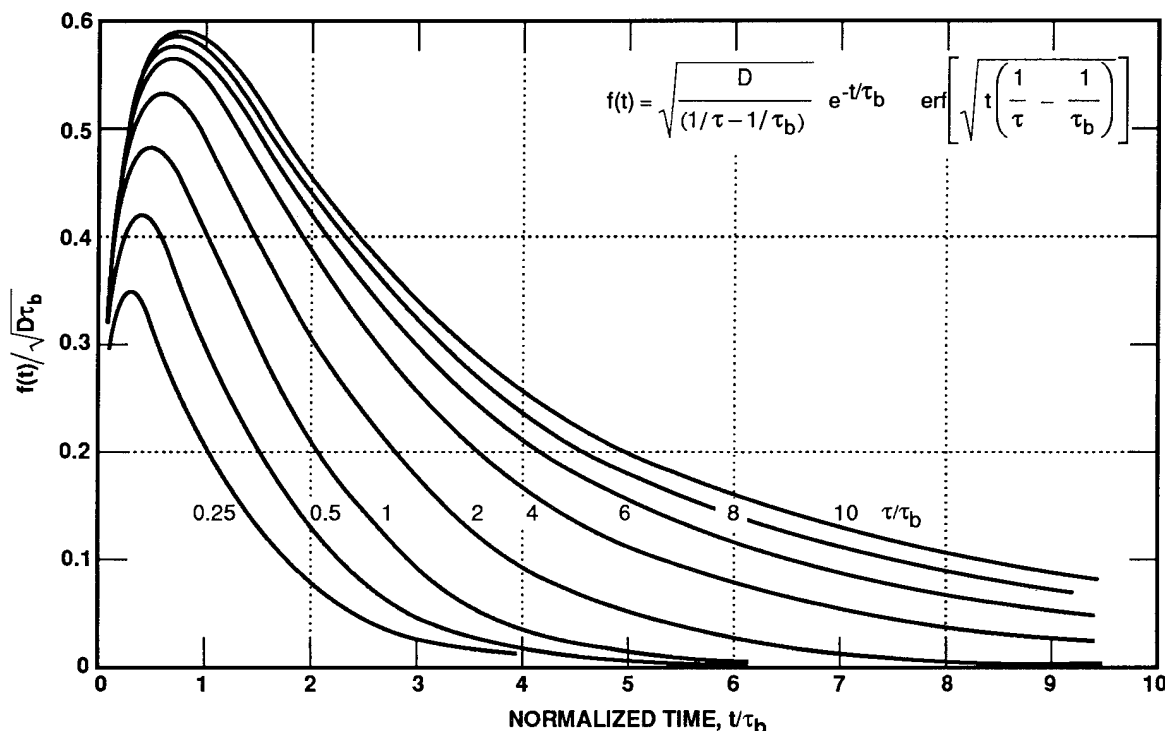


Figure 3-12. Plot of $f(t)$ versus normalized time (Wirth and Rogers, 1964).

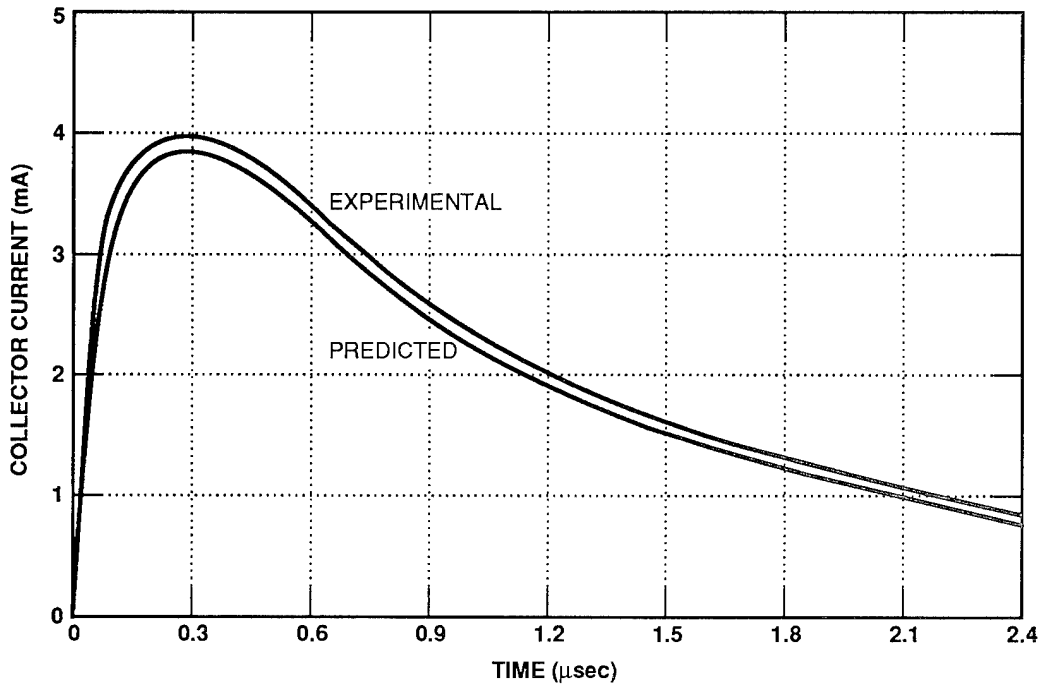


Figure 3-13. Predicted and measured collector photocurrent waveforms for a 2N336 transistor; dose = 0.5 rad(Si), pulse duration = 0.1 μ sec (Wirth and Rogers, 1964).

therefore the delayed photocurrent (holes) injected from the collector to the base was caused only by diffusion. The assumption that the collector region is field-free is not always valid, particularly for devices with high-resistivity collector regions that are operated at high current levels. The effect of the electric field upon the delayed component of collector primary photocurrent is demonstrated by the following argument. After the minority carriers are generated in the collector region, the diffusion process and the electric field resulting from the collector bias current transport some of these carriers into the base region. This base current causes an increase in the collector current and thereby produces a larger electric field. The increase in the electric field in turn causes an increase in the rate at which carriers are injected into the base, etc. For transistors having high-resistivity collector regions as well as large h_{FE} , this positive feedback mechanism (commonly referred to as collector multiplication) may cause momentary instability, with the result that the collector current initially increases exponentially with time. Stable operation is resumed when recombination reduces the

carrier concentration in the collector to a level where the rate at which carriers are injected into the base cannot be sustained by the electric field. This instability is illustrated in Figure 3-15 by the

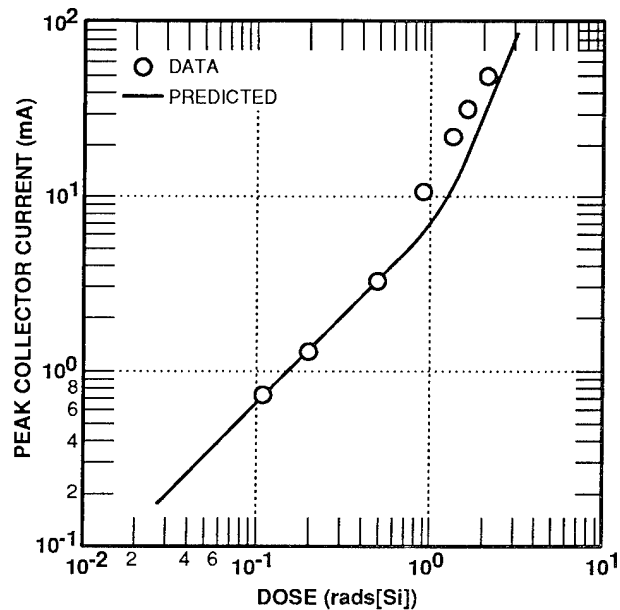


Figure 3-14. Predicted and measured peak collector photocurrent versus dose for a 2N336 transistor; bias = 5 mA, x-ray pulse width = 0.1 μ sec (Wirth and Rogers).

collector current response of a 2N1051 transistor. At a low exposure level, the electric field is not large enough to be a significant factor, and the usual transient response is observed. At the high exposure level, the electric field caused by the larger collector-current transient is sufficient to start the unstable buildup in the current, which occurs at about 0.1 μsec .

The effect of a non-zero electric field in the collector region can be modeled by including the field term in the continuity equation describing the minority-carrier density in the collector region. Since it is assumed that the minority-carrier density is always small compared to the majority-carrier density, this field is determined by the product of the collector resistivity and the current density, as shown in Equation 3.23:

$$\begin{aligned} \frac{dQ(t)}{dt} = & \frac{-Q(t)}{\tau_b} + qA[(W_b + W_{sc} + W_{se})g(t) \\ & + \sqrt{D_p} \int_0^t \frac{g(t-\lambda)e^{-\lambda/\tau_e}}{\sqrt{\pi\lambda}} d\lambda \\ & + D_p \left. \frac{\partial p_c(x,t)}{\partial x} \right|_{x=0}] , \end{aligned} \quad (3.23)$$

$$\begin{aligned} I_c(t) = & \frac{h_{FE}}{\tau_b} Q(t) + qA[(W_b + W_{sc})g(t) \\ & + D_p \left. \frac{\partial p_c(x,t)}{\partial x} \right|_{x=0}] , \end{aligned} \quad (3.23b)$$

$$E_c(t) = p_c \frac{I_c(t)}{A} . \quad (3.23c)$$

$$\begin{aligned} \frac{\partial p_c(x,t)}{\partial t} = & D_p \frac{\partial^2 p_c(x,t)}{\partial x^2} \\ & + \mu_p E_c(t) \times \frac{\partial p_c(x,t)}{\partial x} \\ & - \frac{p_c(x,t) - p_{co}}{\tau_c} + g(t) , \end{aligned} \quad (3.23d)$$

$$p_c(0,t) = 0, |p_c(x,t)| < \infty . \quad (3.23e)$$

Predictions of primary and secondary photocurrent current can be obtained from Equation 3.23 by making the standard difference approximations for the partial derivatives and by solving the resulting set of first-order equations.

A mathematical model that includes the electric fields in the collector is given by Equation 3.23. In this model, the minority-carrier density

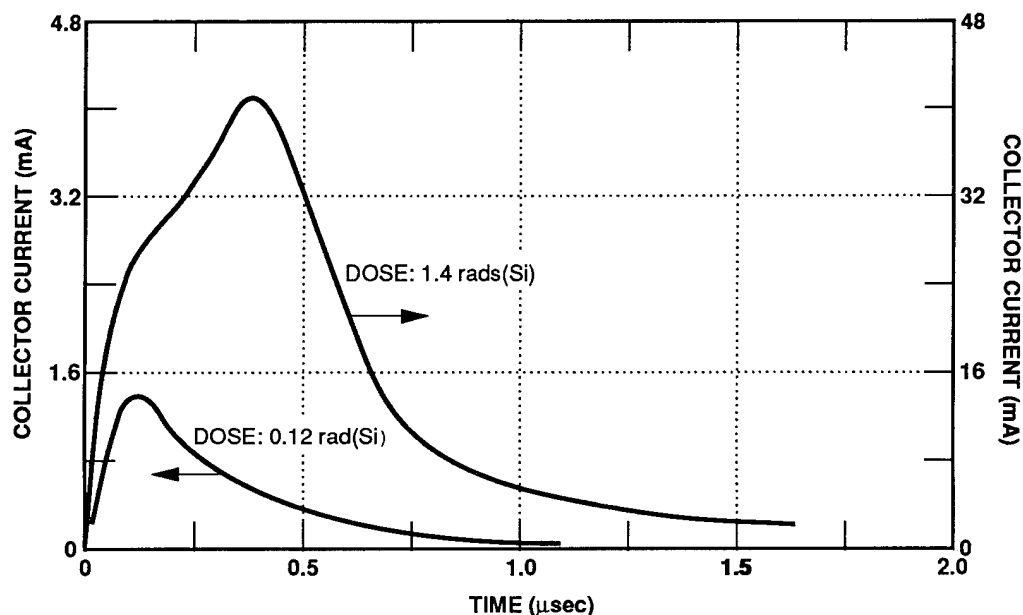


Figure 3-15. Collector photocurrent waveforms for a 2N1051 transistor; x-ray pulse duration = 0.1 μsec (Wirth and Rogers, 1964).

in the collector region is described by a continuity equation that contains the electric field term. Since this field is directly proportional to the collector current, which is, in turn, a function of the electric field, this model is nonlinear and can only be solved by numerical methods. Because the model is nonlinear, predictions of both primary and secondary photocurrent are functions of the initial collector current bias. [This has been confirmed experimentally for 2N1051 and 2N336 transistors and becomes significant in these devices at bias levels of about 10 mA.] Hence, primary photocurrents are not independent of the mode of device operation and do not necessarily scale linearly with dose. Therefore, primary photocurrents determined experimentally from the reverse-biased collector-base diode are not necessarily accurate evaluations of the primary photocurrents obtained under normal transistor operating conditions. The magnitude of the errors introduced by neglecting the electric field or by using experimentally determined values for the primary photocurrent depends strongly upon: (1) the design of the transistor (*e.g.*, in devices that have low collector resistivity, the electric field may be negligible, whereas it may be significant at normal operating current levels in devices with a high-resistivity collector region); and (2) the type of circuit in which the transistor is embedded (*e.g.*, if the transistor saturates at low values of collector current, the electric field may not be large enough to be significant).

3.3.2 Alternative Total Photocurrent Response Model

An alternative method for modeling photocurrents in a bipolar transistor considers the photoresponse of the transistor as a combination of the junction photocurrents and the transistor gain.

The junction photocurrents are defined as the emitter and collector primary photocurrents. Enhancement of the primary photocurrents by the transistor gain causes the secondary photocurrent. As for the diode, a reasonable first-order model of the transistor is an ideal electrical model with the addition of photocurrent generators, as shown in Figure 3-16. Interaction be-

tween the primary photocurrents and transistor photoresponse is determined by circuit conditions. For example, consider the common-emitter photoresponse for a circuit, as shown in Figure 3-17. If the input is shorted (*i.e.*, $R_g, V_{BB} = 0$), the primary photocurrent will flow to ground through the external circuit. Therefore, the transient collector photocurrent ΔI_c will be equal to the collector primary photocurrent. On the other hand, if the source resistance is large compared to the common-emitter input resistance R_{iE} (as determined by the quiescent emitter current bias), then the primary photocurrents will flow into the tran-

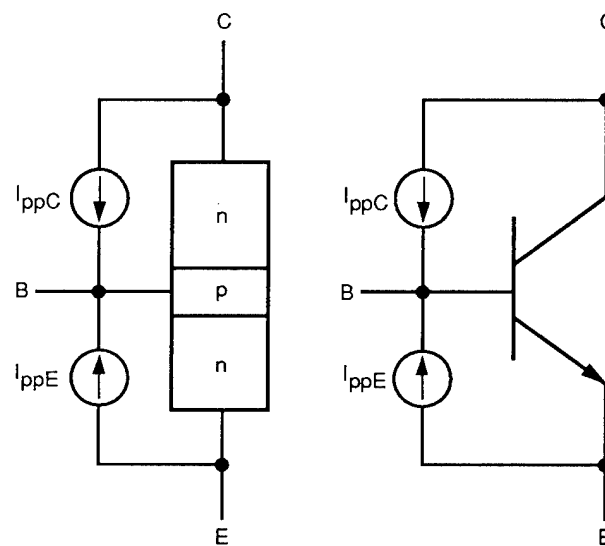


Figure 3-16. First-order transistor photo-response model (Raymond, 1985).

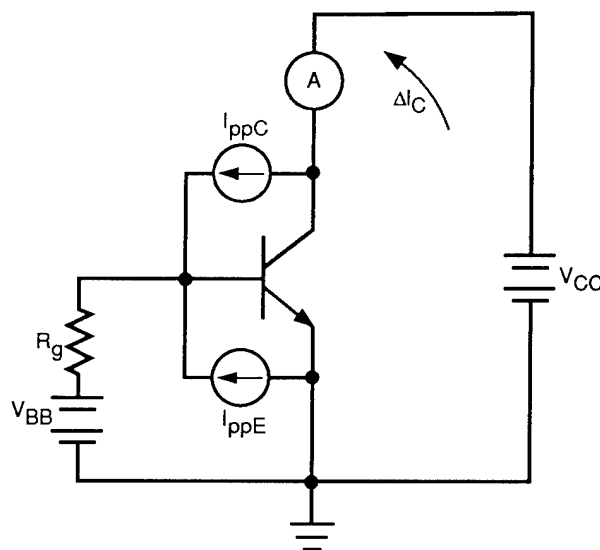


Figure 3-17. Common-emitter transistor photo-response (Raymond, 1985).

sistor base. These currents will be multiplied by the transistor gain in the transient collector photocurrent. Thus, for $R_g \gg R_{iE}$

$$\Delta I_C \cong I_{ppC} + (I_{ppC} + I_{ppE})h_{FE} \quad (3.24)$$

where the second term is the secondary collector photocurrent.

For the collector primary photocurrent, the maximum carrier-collection volume is that of the base and collector region. The collector volume is determined by the collector base junction area and the effective carrier diffusion length plus the collector junction depletion layer width W_C . For a nonepitaxial transistor, the steady-state carrier diffusion length is equal to the minority carrier diffusion length (L_{pC} for an npn transistor). For an epitaxial transistor, the steady-state carrier diffusion length is approximately equal to the high-resistivity collector epitaxial width W_{CE} . Expressions for the steady-state collector primary photocurrents are then

$$I_{ppC} \cong qg_o\dot{\gamma} [V_B + A_C(W_C + L_{pC})] \quad (3.25)$$

for a nonepitaxial npn transistor, and

$$I_{ppC} \cong qg_o\dot{\gamma} [V_B + A_C(W_C + W_{CE})] \quad (3.26)$$

for an epitaxial npn transistor.

With a finite collector load resistance R_L , the transient collector photocurrent will be limited.

When the total collector current exceeds the saturation limit ($\sim V_{CC}/R_L$), the collector-base junction will be forward-biased and the transistor saturates. The saturation recovery time will then depend on circuit bias conditions, as it does for an electrical pulse.

3.3.3 Physical Photocurrent Model

Photocurrent effects are described here as they relate to the physical geometry of a bipolar transistor. The photoresponse sensitivity of all junction semiconductor devices is determined principally by the junction photocurrents. In a bipolar transistor, these are the collector and emitter primary photocurrents. In integrated circuits, photocurrents from the isolation junction are important in determining overall circuit response.

The magnitude of the photocurrent is determined by the effective carrier collection volume for a given radiation pulse width. For the planar bipolar transistor shown in Figure 3-18, the carrier collection volumes can be the volume between the surface and emitter-base junction for thin emitters, the volume between the surface and collector-base junction (excluding the emitter volume) for the base, and the volume defined by the collector-base junction area and an effective minority-carrier diffusion length for the collector. Carriers generated in the base region will flow either to the emitter or collector junction as determined by the built-in electric field distribution and junction bias condition.

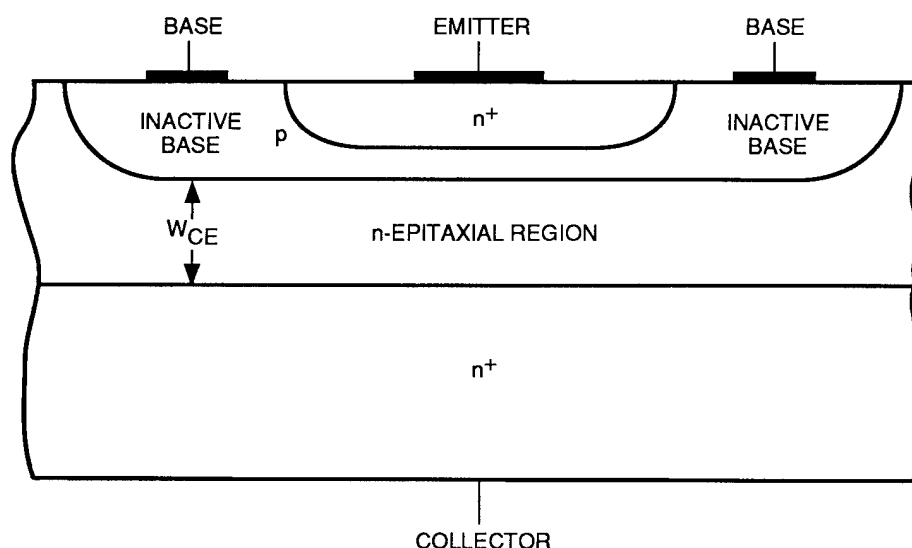


Figure 3-18. Planar bipolar transistor structure (Raymond, 1982).

The time dependence of the collector primary photocurrent is essentially that of a "short-base" pn diode, where the transistor inactive base is the short-base p-region and the collector is the bulk n-region. Carriers generated in the junction depletion layer contribute a photocurrent component that essentially follows the radiation with an effective time constant typically less than 10 nsec, which may be estimated by $\tau \sim 1/2 \pi f_T$. Additional time delay in carrier collection from the inactive base is experienced for transistors of large base area and small local base contact. In this case (principally encountered in photo-transistors), a lateral diffusion delay is observed in the base component of the primary photocurrent. The principal time delay in the collector primary photocurrent is diffusion of carriers from the bulk collector region. For a wide-collector, nonepitaxial transistor, the time dependence is an error function response, as presented for the junction diode. For an epitaxial device, the collection volume and time delays are both reduced.

3.3.4 Other Transient Ionizing Radiation Effects on Bipolar Transistors

Two separate effects that result in high transient dose-rate environments are: (1) nonlinear photocurrents and (2) storage time.

3.3.4.1 Nonlinear Photocurrents

In Section 3.2, the linear relationship relating primary photocurrent to dose rate for a pn junction was presented [in Equation 3.6a] as:

$$I_{pp} = e A W_t g_o \dot{\gamma} \text{ (amperes)} \quad (3.27)$$

where $e g_o = 6.7 \mu\text{A}/\text{cm}^3\text{-rad}/\text{sec}$, and $A W_t$ is the effective volume for photocurrent production in and near the junction. However, for high dose rates, *e.g.*, $\geq 10^8$ rads(Si)/sec, the photocurrent response can take on an anomalous nonlinear characteristic. This effect is depicted in Figure 3-19, where a linear response observed for low dose rates is followed by a discontinuous (jump) increase at the higher dose rates. Subsequent to the step increase in photocurrent, a linear response again occurs until saturation is reached.

The explanation for this nonlinear response is that when the incident radiation is sufficiently

penetrating, hole-electron pairs are produced homogeneously throughout the device. The holes collected in the active region of the base, as well as those that diffuse into the region from the collector and emitter, flow laterally outward toward the base contact, as shown in Figure 3-20. This current produces a lateral voltage drop outward, parallel to the base-emitter and base-collector junctions. The center of the emitter junction is then more forward-biased than the periphery, and the emitter potential and that of the central portion of the base remain in phase. If the corresponding lateral currents are large enough, as in the case of a high-dose-rate incident pulse, this base-emitter potential drop can exceed the breakdown voltage BV_{EBO} . If this happens, the emitter and base are essentially shorted through this low-impedance breakdown path. The device is now in a common-emitter configuration insofar as the base photocurrent drive is concerned and the photocurrent is amplified to produce a very large collector current, which results in the anomalous nonlinear photocurrent. Under certain conditions, the lateral photocurrent distribution is the reverse of the preceding. The photocurrent density can become electrically unstable, producing enhanced photocurrents near the center of the emitter (Habing and Wirth, 1966).

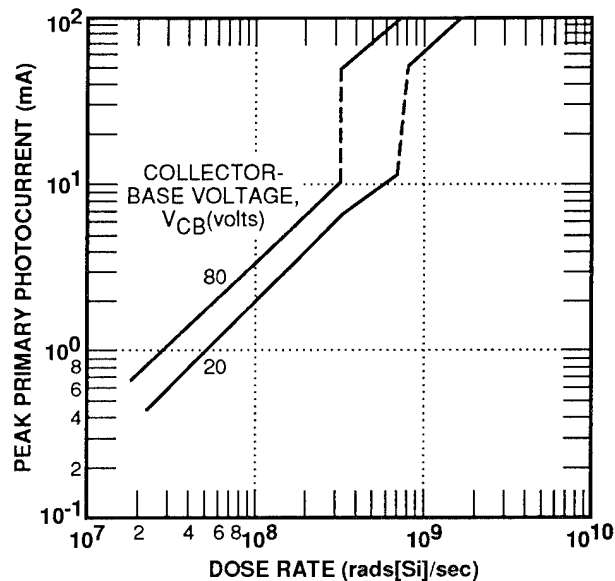


Figure 3-19. Transistor nonlinear photocurrent behavior with dose rate for two values for collector base voltage (Habing and Wirth, 1966).

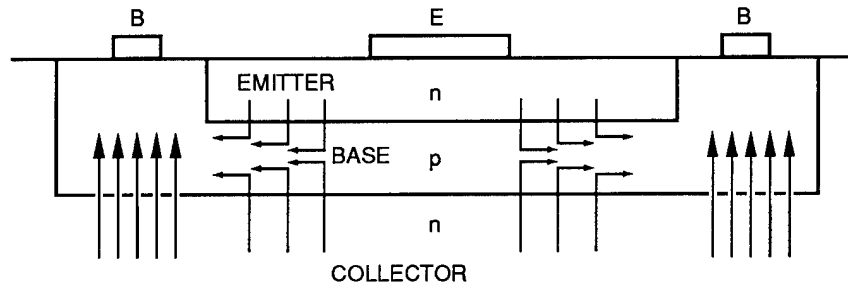


Figure 3-20. Lateral photocurrent flow within a circular transistor (Habing and Wirth, 1966).

Theoretical results can approximately predict the dose-rate level at which the anomalous behavior occurs in many cases. The junction breakdown in many instances is temporary, with subsequent partial healing of the emitter-base breakdown path. This allows the device to revert to quasi-normal operation, but at the increased levels of photocurrent shown following the discontinuity in Figure 3-19.

3.3.4.2 Radiation Storage Time

If a transistor is operated in the linear region, the overall photoresponse is the straightforward combination of the time dependence of the primary photocurrents and that of the transistor electrical response. For example, the maximum common-emitter transistor photocurrent occurs when the external base impedance is large compared to the transistor input impedance. In terms of the LaPlace transforms for the currents and frequency-dependent gain,

$$I_C(s) = [I_{ppC}(s) + I_{ppE}(s)] \times [h_{FE}(s) + 1] , \quad (3.28)$$

and the time-dependent current is given by the inverse transform,

$$I_C(t) = \mathcal{L}^{-1}[I_C(s)] . \quad (3.29)$$

If the primary photocurrents are fast compared to the transistor response, the worst-case secondary photocurrent will be the waveform of input-current impulse response. Conversely, if the transistor is fast compared to the time constants of the primary photocurrents, then the secondary

photocurrent will essentially be an amplified representation of the dominant primary photocurrent.

Exposure to a high-intensity ionizing radiation pulse may result in a collector photocurrent large enough to saturate the transistor in the circuit. To a first-order approximation, the radiation-induced storage time is that resulting from the primary photocurrents as external base drive. Using an external base drive, the transistor radiation storage time t_{SR} can be expressed as

$$t_{SR} = \tau_s \ln \left[\frac{I_{ppC} + I_{B(OFF)}}{I_{B(OFF)} + \left(\frac{V_{CC}}{R_L} \right) h_{FE}} \right] , \quad (3.30)$$

where τ_s is the storage time constant for the transistor and is a function of the collector minority-carrier lifetime and doping profile. For a nonepitaxial planar transistor, τ_s is approximately equal to the collector minority-carrier lifetime. Figure 3-21 shows radiation storage time as the time the transistor remains saturated after the radiation pulse ends.

Accurate representation of the overall transistor photoresponse requires an accurate electrical model for the transient level and frequency response of interest. If the transistor is operated in the linear region and the transient photocurrent is small compared to the quiescent bias current, small-signal models such as the ones shown in Figure 3-22 provide an accurate representation of the device.

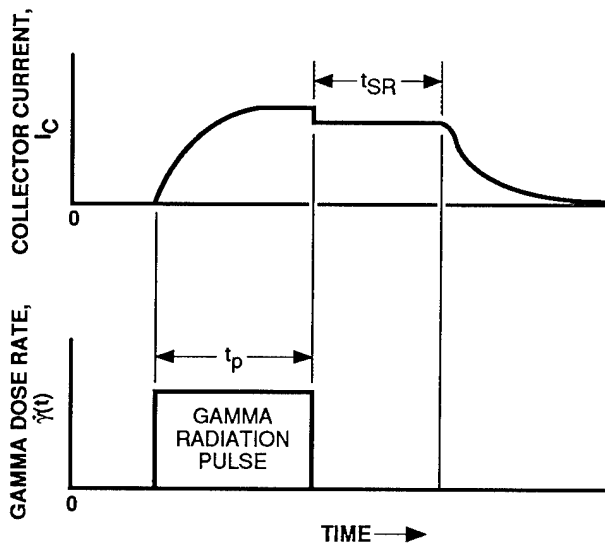


Figure 3-21. Collector current and dose-rate pulse versus time showing radiation storage time (Messenger and Ash, 1992).

3.4 Transient Ionizing Radiation Response of Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs)

3.4.1 MOSFET Photocurrent Model Development

The model developed for the pn diode [Sections 3.1 and 3.2] and extended to support the bipolar transistor discussion [Section 3.3] is also applicable to the discussion of the transient ionizing dose response of the MOSFET. For completeness, the Wirth-Rogers model and governing assumptions are repeated in this section. In addition, some recent enhancements to the model are discussed. The following discussion has been paraphrased from Massengill (1987).

Subject to the assumptions to be discussed here, the solution of the continuity and minority-carrier diffusion equations for a rectangular radiation pulse yields a total photocurrent of:

$$I_{pp}(t) = q A g_o \dot{\gamma} \left[W_t + L_n \operatorname{erf} \left(\sqrt{t/\tau_n} \right) + L_p \operatorname{erf} \left(\sqrt{t/\tau_p} \right) \right] \quad (3.31a)$$

for $0 \leq t \leq t_p$, and

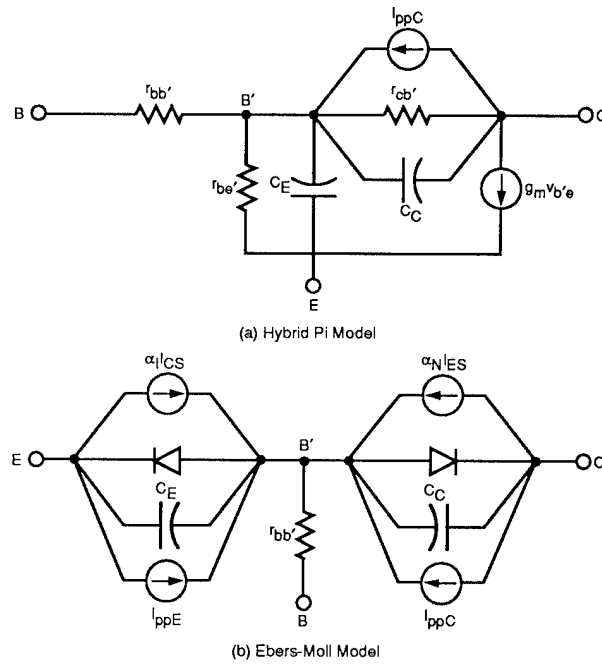


Figure 3-22 (a, b). Radiation-inclusive transistor models (Raymond, 1985).

$$I_{pp}(t) = q A g_o \dot{\gamma} \left\{ L_n \left[\operatorname{erf} \left[\sqrt{t/\tau_n} \right] - \operatorname{erf} \left[\sqrt{(t-t_p)/\tau_n} \right] \right] + L_p \left[\operatorname{erf} \left[\sqrt{t/\tau_p} \right] - \operatorname{erf} \left[\sqrt{(t-t_p)/\tau_p} \right] \right] \right\} \quad (3.31b)$$

for $t > t_p$. The depletion region width W_t represents the prompt-component collection length. The sum of the error function (erf) terms represents the delayed, diffusion-component collection length.

The assumptions implied with the use of the minority-carrier diffusion and continuity equations can be very important. The assumptions are (Wirth and Rogers, 1964):

1. A one-dimensional, infinite, single junction device,
2. No electric fields except in the depletion region,
3. Uniform doping on each side of the junction,

4. Majority-carrier concentrations that are not appreciably altered by the radiation, *i.e.*, low-level injection.

Of these conditions, the fourth is most suspect. Dose rates $>10^{10}$ rads(Si)/sec may cause significant increases in the concentrations of majority carriers (Messenger, 1979). This majority concentration modulation necessitates the solution of the ambipolar diffusion equation (McKelvey, 1966), which is difficult because of the nonlinear nature of the equations. The solution would ultimately change the diffusion lengths, L_n and L_p and the minority-carrier lifetimes, τ_n and τ_p . However, as will be seen in later sections, typical design-rule dimensions of most modern integrated circuits are much smaller than these diffusion lengths. Thus, the diffusion collection is usually limited by the geometry of the region (*e.g.*, boundaries, other junctions, etc.) and not by the diffusion lengths. Thus, the precise diffusion lengths are not as critical in determining the photocurrent magnitudes as is the geometry.

Several extensions of the Wirth-Rogers model have been developed. Donovan, Hauser, and Simons (1974) have developed forms of the model applicable to a pn junction region with finite length, as shown in Figure 3-23. If the lengths of the bulk regions are on the order of the minority-carrier diffusion lengths, then the following replacements must be performed in the Wirth-Rogers equations:

$$L_n \rightarrow L_n \tanh\left(\frac{W_p}{L_n}\right), \quad (3.32)$$

$$\tau_n \rightarrow \frac{\left[L_n \tanh\left(W_p/L_n\right)\right]^2}{D_n}, \quad (3.33)$$

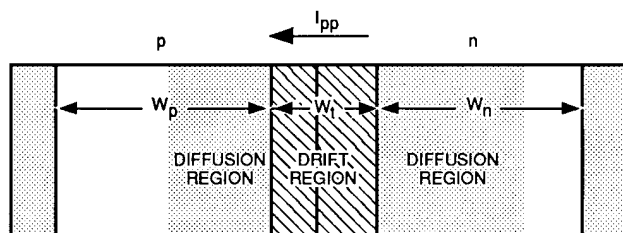


Figure 3-23. Bounded collection region (Donovan, Hauser, and Simons, 1974).

$$L_p \rightarrow L_p \tanh\left(\frac{W_n}{L_p}\right), \quad (3.34)$$

$$\tau_p \rightarrow \frac{\left[L_p \tanh\left(W_n/L_p\right)\right]^2}{D_p}, \quad (3.35)$$

where W_p and W_n are the distances from the edge of the depletion region to the boundary on the p and n sides of the junction, respectively, and D_n and D_p are the diffusion coefficients for electrons and holes, respectively.

Long, Florian, and Casey (1983) have developed equations describing the effects of a high-low junction in the proximity of the photocurrent junction, as shown in Figure 3-24. This case applies to the epitaxial-substrate ($n-n^+$) interface found in most modern CMOS structures. For this case, the following replacements are made in the Wirth-Rogers equations:

$$L_p \rightarrow L \tanh(W/L) + \frac{L^+}{\cosh(W/L)}, \quad (3.36)$$

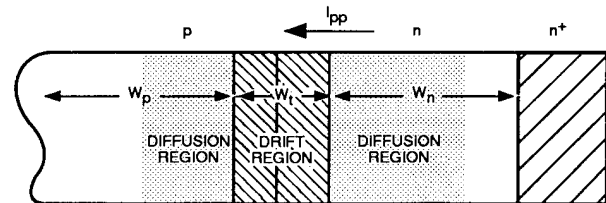


Figure 3-24. Collection region bounded by a high-low junction (Donovan, Hauser, and Simons, 1974).

$$\tau_p \rightarrow L_p^2/D_p, \quad (3.37)$$

where

- L = minority-carrier diffusion length in the epitaxial layer (n -region)
- L^+ = minority-carrier diffusion length in the substrate (n^+ -region)
- W = distance between the edge of the depletion region and the substrate
- D_p = diffusion coefficient for minority carriers in the epitaxial layer.

Recent work at Sandia National Laboratories and Rensselaer Polytechnic Institute has addressed the modification of the Wirth-Rogers models for application under high injection conditions (Gover, n.d.; Ishaque, Becker, and Block, 1987). In addition, a significant extension to the Wirth-Rogers model has been developed by Enlow and Alexander (1988) [see Section 3.1].

3.4.2 MOSFET Photocurrent Equivalent Circuit

Transient radiation produces several effects on MOS devices. First, electron-hole pairs are created in the bulk, and these carriers are collected by the pn junction. Carriers created under the gate region will be collected by the pn junctions, even if the device is operating in cut off and no conductive channel exists. For a symmetrical device, approximately one-half of the total photocurrent will flow across the source-substrate junction and the other half will flow across the drain-substrate junction. The source and substrate of a MOS device are normally connected together so the net external source photocurrent will equal the drain photocurrent. Because of the large areas associated with the diffused source and drain pn junction, most of the MOS photocurrent comes from these junctions while only a small percentage of the total arises from under the gate area.

Illustrated in Figure 3-25 are some of the important parameters. The current is assumed to result from the collection of all charge generated in the volume defined by the width of the depletion layer W_t and within one diffusion length L . The prompt drain current may be expressed as

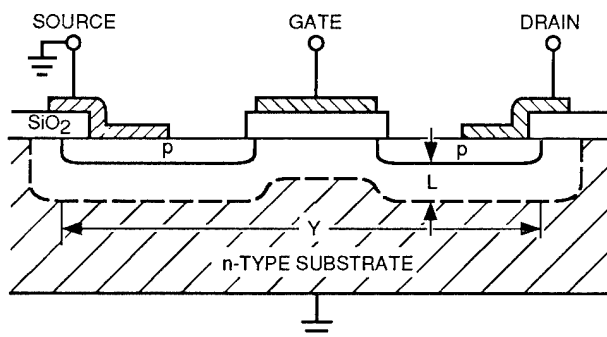


Figure 3-25. Typical MOSFET structure.

$$I_{pd} = q g_o \dot{\gamma} A (W_t + L) \quad (3.38)$$

The collection area,

$$A = (Y + 2L) \times (\text{width of p-diffusions} + 2L), \quad (3.39)$$

where Y is the effective device length.

An estimation of the photocurrent sensitivity of a MOSFET can be made from the above equations and the following typical values (Donovan, Hauser, and Simons, 1974):

$$Y = 2.5 - 4 \times 10^{-3} \text{ cm}, \quad (3.40a)$$

$$L = 2 \times 10^{-3} \text{ cm } (t \sim 10^{-6} \text{ second}). \quad (3.40b)$$

With the assumption that the cell is square, these values give

$$I_{pd} \sim 2,705 \mu\text{A at } 10^8 \text{ rads(Si)/sec} \quad (3.41)$$

Based on this discussion, a schematic representation of these photocurrents can be developed. Such a representation is shown in Figure 3-26, where a CMOS inverter is used as an example.

In this example, the local photocurrents caused by the dose-rate exposure are depicted as ideal current sources. Photocurrents are present across each semiconductor junction and are directed onto the p-regions of the junctions. The figure does not show the photocurrents across the source regions of the transistors. Such photocurrents will have no net effect on device response, because they can, at most, turn on only the source-substrate diodes and cycle current in the

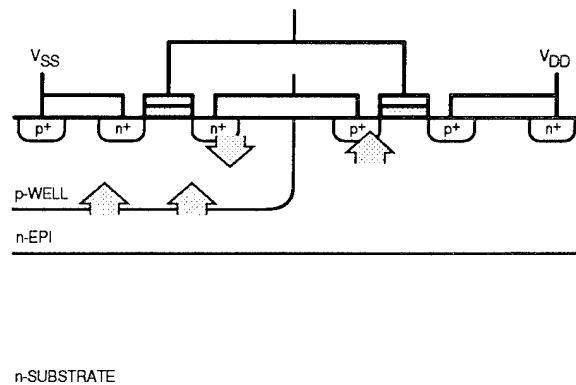


Figure 3-26. Local photocurrents produced by a dose-rate event in a CMOS inverter (Ma and Dressendorfer, 1989).

vicinity of the node. The action of these photocurrents in an SRAM cell is depicted in Figure 3-27. Sources P_1 and P_2 model drain photocurrents of the p-channel devices, P_3 and P_4 those of the n-channel devices, and P_5 the photocurrent across the p-well, represented in this figure as the reverse-biased diode between V_{DD} and V_{SS} .

The magnitudes of junction photocurrents have been modeled analytically and depend on the injection level of excess carriers characteristic of the event and the material and processing parameters of the affected device. A complete summary of photocurrent expressions, including their ranges of applicability, is given in Massengill's Ph.D. dissertation (Massengill, 1987). For the many integrated circuits available today, the magnitudes of photocurrents directed onto device nodes are limited by device geometries. For example, the charge deposited in the p-well of the device represented in Figure 3-26 is collected both as the n-channel drain photocurrent and as the p-well photocurrent. The collection length, comprising combined drift and diffusion currents for both the drain and the well, exceeds the well depth; *i.e.*, either node would collect all of the charge deposited in the well if the other were not present. Thus, the collected current magnitude is determined by partitioning the charge onto the two nodes, rather than by the details of transport processes. A reasonable choice for partitioning allows each node (required by

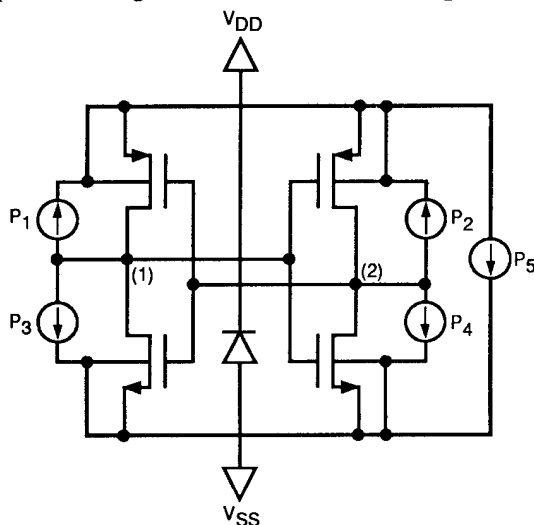


Figure 3-27. Local photocurrents produced by a dose-rate event in SRAM cell (Ma and Dressendorfer, 1989).

design rules to be nonoverlapping) to collect the charge deposited in its equilibrium depletion region and to assign charge deposited in the equilibrium "quasi-neutral" regions to the nearest junction. Because of such partitioning, the photocurrents collected by most devices can be computed without resort to detailed collection analyses. In many cases, the photocurrent magnitudes depend more strongly on layout geometry than on carrier mobilities, lifetimes, or local fields.

In subsequent sections, the effect of these local photocurrents will be extended to develop an overall understanding of transient radiation effects on complex microelectronics.

3.5 Transient Ionizing Radiation Effects on Silicon Integrated Circuits on Insulating Substrates

The use of an insulating substrate technology (*e.g.*, silicon on sapphire [SOS], silicon on buried oxide, etc.) provides a method for improving IC hardness to transient radiation. This improvement is the result of the reduced transient radiation charge-collection volume. Thus, this technology is usually employed for applications where a high transient-dose-rate threat (*e.g.*, >10 rads[Si] sec) due to a nuclear weapon exists, which the system must be capable of surviving and be able to continue to operate (or rapidly resume operation) without outside intervention.

The lack of outside intervention implies that critical information required for the system to function (*e.g.*, operating system) and data such as track files, threat evaluations, and prioritization, etc. must be preserved in this hostile environment. Such applications include satellite onboard data-processing (OBDP) system critical vector memories, circumvention system critical data memories, intercontinental ballistic missile (ICBM) guidance systems, etc.

In addition to being more resistant to transient radiation than bulk technology ICs, silicon-on-insulator (SOI) ICs will recover from a transient event more rapidly, which can also be important in certain applications. As a general rule, very large-scale integrated circuit (VLSIC) bulk tech-

nology devices (*e.g.*, $\geq 64\text{k}$ SRAM) upset at dose rates in the range of 1 to 2×10^9 rads(Si)/sec, whereas SOI technology devices upset at $\geq 1 \times 10^{11}$ rads(Si)/sec.

The transient ionizing radiation response in silicon insulating substrate technologies (*e.g.*, SOS or silicon on buried oxide) differs significantly from the response of bulk silicon technology devices. As stated, the primary reason for this difference is the reduced collection volume [see Figure 3-28]. However, for silicon on oxide [hereafter to be referred to as SOI], the lack of a natural source-to-body contact in conjunction with the occurrence of a parasitic bipolar transistor, formed by the source, channel, and drain regions of the MOS transistor [see Figure 3-29], will also have a dramatic effect on the performance of the individual MOSFET and consequently on the IC.

Although gallium arsenide (GaAs) is an insulating technology, the transient ionizing radiation response of circuits fabricated on this material differ from the response of SOI and SOS technology circuits. This difference can be attributed to the radiation response of the GaAs material. Hence, transient ionizing radiation response of these GaAs ICs is discussed separately [Section 3.6].

3.5.1 Silicon-on-Insulator Transistors

As previously stated, the active region (body) is isolated from the substrate in SOI devices, thus limiting the photocurrent collection volume. However, because of the smaller size of the device, the efficiency of the parasitic bipolar device [Figure 3-29], which is formed by the source base and base-drain junctions, is enhanced (Davis *et al.*, 1985; Mikawa and Ackerman, 1987). The gain of the parasitic bipolar transistor enhances the photocurrent and, thus, dominates the transient response.

The following discussion [based on Alles (1990)] provides a qualitative understanding of the transient response of an SOI transistor. In order to study the effect of transient-radiation-induced photocurrents on SOI transistors, it is first neces-

sary to point out particular aspects of the transistor structure to be studied. As shown in Figure 3-30, the source and drain implants extend to the underlying oxide. This configuration is referred to as a fully bottomed junction (FBJ) and is the method employed for all radiation-hardened SOI designs. In addition, in both the OFF and ON transistors, there is a quasi-neutral (nondepleted) region of the body, and thus, the transistors are referred to as partially depleted.

In SOI devices with FBJs, isolation of the active region (body) from the substrate limits the volume of the depletion regions (to source and drain side walls) and eliminates charge collection from the substrate, which otherwise would be under the source and drain. This limited collection volume, along with typical device (gate) dimensions, which are much less than carrier diffusion lengths, leads to device photoresponses that follow the radiation pulse closely (Kjar and Kinoshata, 1973); *i.e.*, no significant diffusion component of the photocurrent follows the radiation pulse. However, isolation of the body regions of SOI transistors introduce floating-body effects (Tihanyi and Schlotterer, 1975) associated with the finite volume of the transistor body region. During normal device operation, the transistor body potential may be large enough to forward-bias the body-source junction. This effect has been characterized extensively [see, for example, Davis *et al.* (1985); Kato, Wada, and Taniguchi (1985); and Coligne (1986)]. Transient-radiation-induced photocurrents may also forward-bias the body-source junction and activate the parasitic bipolar transistor (Davis *et al.*, 1985), leading to bipolar enhancement of transient-radiation-induced photocurrents.

A common way to reduce or eliminate floating-body effects is to electrically connect the device body to its source, or to a supply, using one or more body ties. Even when body ties are used, finite, distributed resistance (R_{BODY}) still exists between any point within the transistor body and the body tie(s), as shown in Figure 3-31. Because of this resistance, using body ties does not necessarily completely eliminate bipolar effects

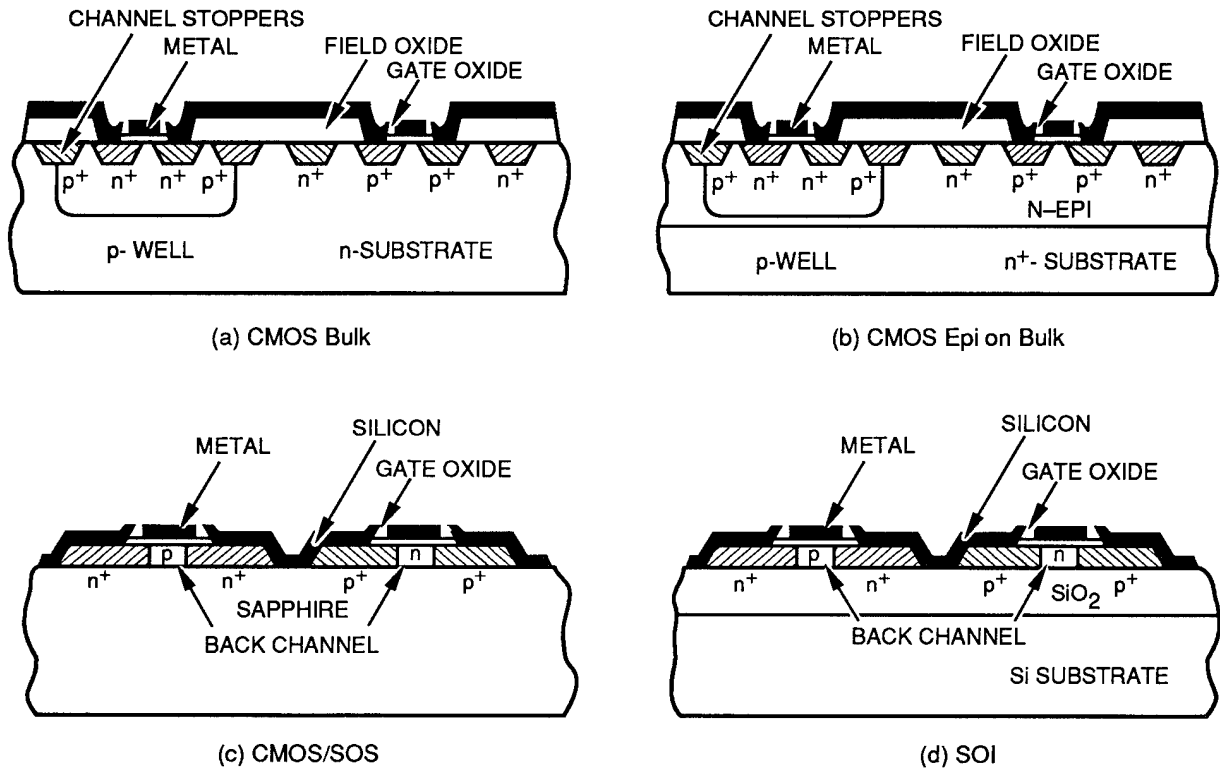


Figure 3-28 (a, b, c, d). Cross section of an SAOI transistor with the parasitic bipolar and back-gate devices (Alles, 1990).

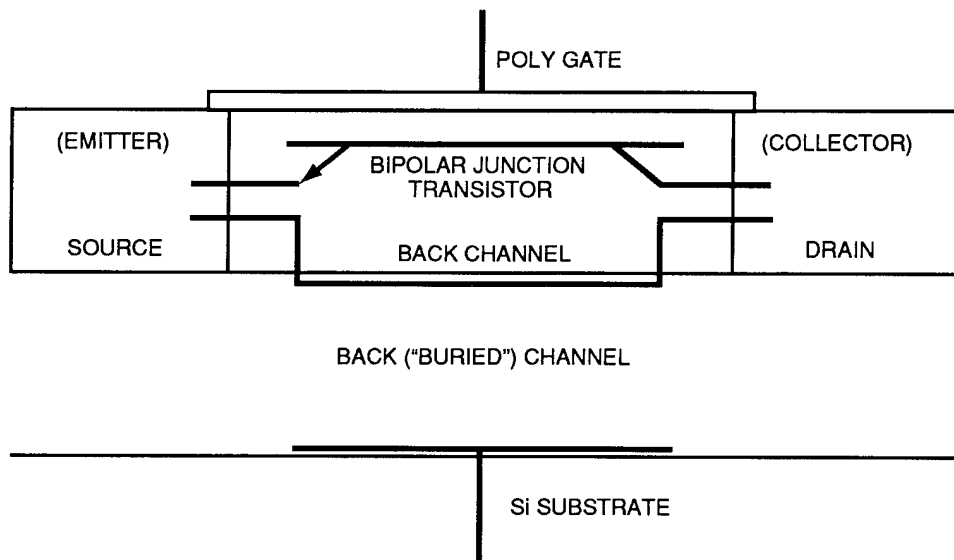


Figure 3-29. Cross section of an SAOI transistor with the parasitic bipolar and back-gate devices (Alles, 1990).

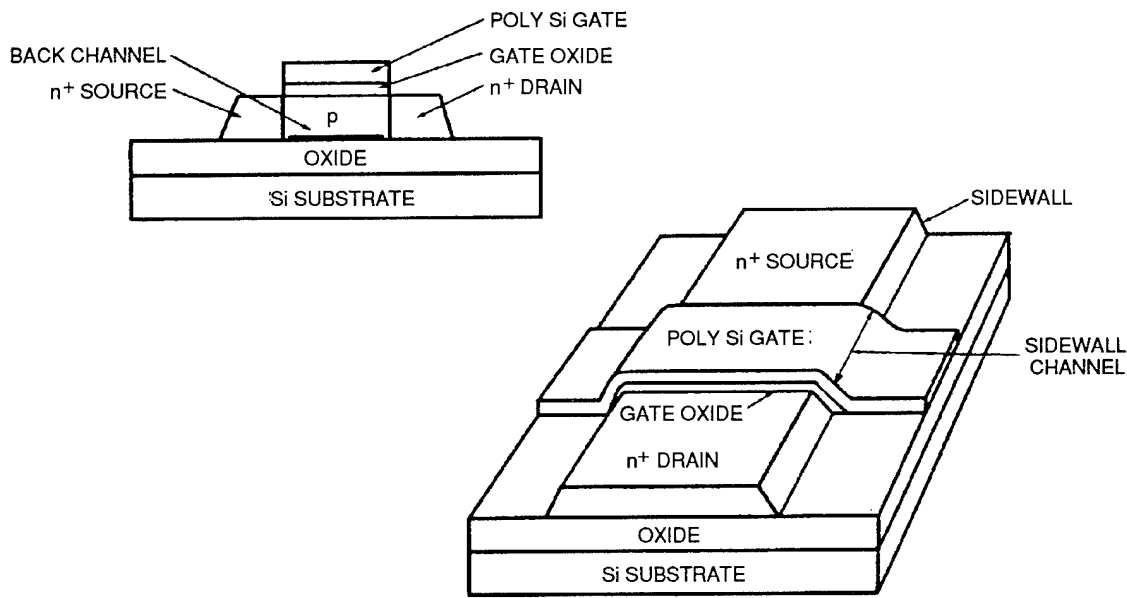


Figure 3-30. Schematic illustration of possible radiation-induced leakage current paths in an SOI transistor (Ma and Dressendorffer, 1989).

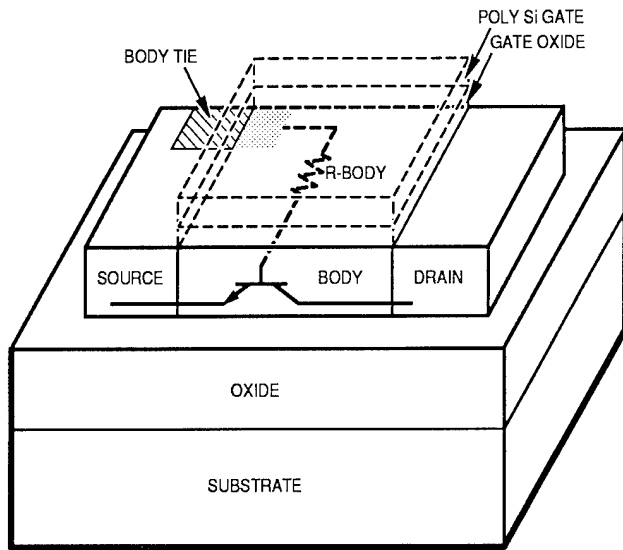


Figure 3-31. Three-dimensional representation of an n-channel SOI device (Alles, 1990).

in the case of single events, but it can significantly reduce the photocurrent response to both single-event (Kerns *et al.*, 1989) and dose-rate radiation (Davis *et al.*, 1985).

Excess minority carriers induced by ionizing radiation must either diffuse to junctions or pass through the distributed body resistance (if body ties are used) to be removed from the body, or recombine in the body. The rate at which charge

(current) is removed from the body through a body tie is determined by the distributed resistance and by the capacitances associated with the body node. Transient currents within the body create potential gradients, and localized regions of the body-source junction can become forward-biased, resulting in bipolar amplification of the radiation-induced photocurrent. Thus, the gain of the parasitic bipolar transistor, determined by base width (gate length) and doping levels, play an important role in determining the transient-radiation-induced photocurrent response of SOI MOS transistors. As feature sizes decrease, bipolar gains correspondingly increase, making bipolar effects significant in aggressively scaled technologies. When body ties are utilized, the distributed body resistance becomes important in determining the transient response of MOS/SOI devices. The resistance determines the portion, if any, of the body-source junction that becomes forward-biased at a given dose rate, and thus controls the amount of transient-induced photocurrent that is subject to bipolar enhancement. The body resistance is determined by the device dimensions, body (well) resistivity, and positioning of the body ties.

3.5.2 Silicon-on-Sapphire Technology Devices

The photocurrents resulting from transient ionizing radiation in SOS technology devices are much larger than those in SOI because the conductivity of sapphire is greater than that of SiO₂. However, the low minority-carrier lifetimes in SOS films (Kjar and Kinoshata, 1973) result in negligible parasitic bipolar transistor gain. Thus, SOS ICs provide high tolerance to transient ionizing radiation, being of the same order as SOI devices (*e.g.*, upset levels for VLSICs $\geq 1 \times 10^{11}$ rads[Si]/sec.)

3.6 Transient Ionizing Dose Rate Response of Gallium Arsenide Semiconductor Devices

The transient ionizing dose rate response of GaAs devices is influenced by four factors:

1. pn junction photocurrent generation
2. Substrate photocurrents
3. Charge trapping in the substrate
4. Shunt currents through the semi-insulating (SI) substrate.

These effects will be discussed in the following sections.

3.6.1 pn Junction Photocurrents

Dose-rate, or photocurrent, effects are produced in ICs as the excess carriers generated by the incident ionizing radiation are collected by pn junctions. These effects are manifested in a circuit by large current or voltage perturbations whose magnitude and duration depend on the peak dose rate $\dot{\gamma}$, pulse duration t , junction area A , collection volumes, carrier lifetimes τ , and circuit/device time constants (especially when greater than the pulse duration). For the simplest case of a pn junction exposed to a square pulse of dose rate $\dot{\gamma}$ and duration $t \gg \tau_n, \tau_p$, the primary photocurrent is given by:

$$I_{pp} = qA(W_t + L_n + L_p)g_0\dot{\gamma} \quad (3.42)$$

Here, W_t is the depletion-layer width and g_0 is the pair generation constant, which is about 6.63×10^{13} pairs/cm³-rad for GaAs. Although g_0

is slightly higher for GaAs than for Si, GaAs is characterized by much shorter diffusion lengths (L_n and L_p) and minority-carrier lifetimes. Thus, in principle, GaAs devices should be somewhat harder to transient upset than silicon devices for this effect alone. However, in actuality, the upset levels in GaAs devices are dominated by substrate photocurrents and substrate charge trapping [discussed below] (Buchanan, 1985; Zuleeg, Notthoff, and Troeger, 1983).

3.6.2 Substrate Photocurrents

Substrate photocurrents can flow between contact pads or metallization placed directly on chip surfaces. Measurements have shown that such currents can be larger by several orders of magnitude than device photocurrents and, in fact, can dominate circuit response (Zuleeg, Notthoff, and Toeger, 1983); however, it has also been found that circuit response can be reduced by an order of magnitude by placing the bonding pads and metal interconnects on an insulating layer.

3.6.3 Substrate Charge Trapping

A transient ionizing event will result in charge being trapped in the deep levels that are characteristic of several insulating substrate materials (Simons *et al.*, 1981). Conduction in FET structures can be severely affected (even cut off) by the trapped charge, which decays with time constants ranging from milliseconds to seconds. Recent work has shown, however, that this backgating-like effect can be appreciably reduced (and perhaps even eliminated) by the use of high-quality liquid-encapsulated-crystal (LEC) substrates and/or by various FET structural modifications, such as implanting a p-layer beneath the n-channel (Anderson *et al.*, 1982). The effect can also be minimized by operating at high current levels.

Transient response data reported for GaAs digital ICs of medium-scale-integration (MSI) complexity have shown a broad range of upset thresholds. Schottky-diode-FET-logic (SDFL) circuits have demonstrated thresholds ranging from 1×10^8 to 2×10^{10} rads(GaAs)/sec (Walton *et al.*, 1983), while the enhancement JFET (E-

JFET), 256-bit RAM functioned without soft errors up to dose rates of 6×10^9 to 1×10^{10} rads(GaAs)/sec (Notthoff, Zuleeg, and Troeger, 1983). While these circuit upsets apparently resulted from photocurrent phenomena, disruptions in buffered-FET-logic (BFL) gate and ring oscillator performance for tens of milliseconds have been observed following 1- μ sec LINAC exposures at total doses between about 10^2 and 10^3 rads(GaAs) (10^8 to 10^9 rads[GaAs]/sec) and after 3-nsec flash x-ray (FXR) pulses at the 100-rad level (3×10^{10} rads[GaAs]/sec), all as a result of the backgating problem. Radiation-induced backgating has also been reported in power metal-oxide gate FETs (MESFETs) and in a monolithic amplifier operating at X-band (Anderson and Binari, 1983), although transient-free operation of a microwave MESFET was observed up to a dose rate of 3×10^{10} rads(GaAs) sec (Castle, 1983).

3.6.4 Semi-Insulating Substrate Shunt Currents

Based on extensive experimental work and analysis, Zuleeg, Notthoff, and Troeger (1983) argue that the upset levels in GaAs JFETs with channel lengths below $\sim 1 \mu\text{m}$ are dominated by shunt currents between the source and drain through the semi-insulating (SI) substrate, as indicated by I_{ps} in Figure 3-32, which schematically illustrates the shunt current effect. The currents I_{pp1} and I_{pp2} are the usual junction photocurrents, and these dominate the upset levels for devices with longer channel lengths. In effect, the normally high-resistivity SI substrate becomes conducting because of the induced carrier densities from ionization in the substrate, and offers a low-resistance shunt path for currents between the source and drain regions (Bowers and Barnett, 1970). For a 1- μm channel length, the predicted upset dose-rate threshold due to the shunt substrate current is $\sim 5 \times 10^{10}$ rads(GaAs)/sec.

As illustrated in Figure 3-33, short-pulse (<100 nsec) upset thresholds reported for GaAs ICs compare quite favorably with those characteristic of silicon large-scale-integration (LSI)

technologies (Simons, Donovan, and Hauser, 1977; Long, 1980). Long-pulse ($>1 \mu\text{sec}$) thresholds decrease somewhat for silicon devices (because of the long lifetimes) but should not change appreciably for GaAs devices in the absence of severe backgating problems. Moreover, GaAs FET circuits are not susceptible to latchup associated with extraneous four-layer paths as are many bipolar and CMOS/bulk silicon ICs. Extremely low upset thresholds can be expected for both GaAs and Si charge-coupled devices (CCDs) ($\leq 10^6$ to 10^8 rads[M]/sec).

3.7 Transient Ionizing Dose-Rate Upset Response of Microelectronics

The transient ionizing dose radiation response of integrated circuits is addressed here. Dose-rate upset is investigated using a static random-access memory (SRAM) IC as an example. The use of an SRAM permits four separate upset events, relevant to system failure modes, to be examined: (1) memory-cell upset, (2) input/output (I/O) circuit upset, (3) write-mode address upset, and (4) "pushout," an increase in SRAM access time that results from transient ionizing radiation. This discussion basically follows the work of Massengill (1987) and Massengill and Diehl (1984). Although the discussion refers to MOSFET technology, the theory is relevant to silicon bipolar and GaAs technology ICs. A brief explanation of SRAM cell operation is provided as well as a definition of bit errors and memory corruption.

3.7.1 CMOS SRAM Operation

Figure 3-34 shows the circuit schematic for the standard six-transistor CMOS SRAM cell. This cell stores one bit of information via high- or low-voltage levels at information nodes (1) and (2). These voltage levels are always complementary (in the steady state) due to the inverting properties of the p-channel/n-channel pairs. The feedback properties of the inverter arrangement provide stability of the stored information; the voltage levels at (1) and (2) remain complementary as long as power is supplied to the cell and no external effects perturb the states.

For steady-state operation, when the voltage at (1) is low, transistor MN1 is ON and MP1 is OFF, thus providing a low-impedance path from (1) to V_{SS} (or ground). However, since MP1 is OFF, no direct path exists (excluding leakage currents) for current from V_{DD} to V_{SS} . This inherent property is one of the major advantages of the CMOS technology; that is, the circuits have very little current drain (and thus low power consumption) in the steady-state mode. On the other side

of the cell, voltage (2) is high. Transistor MN2 is OFF and MP2 is ON. The feedback arrangement of the two inverters provides a self-sustaining state.

Writing and reading information to and from the cell is achieved via the bit lines, B1 and B2 through the access transistors MN3 and MN4. When these access transistors are turned ON, the voltages at (1) and (2) are available to other circuitry for reading or writing processes. It is

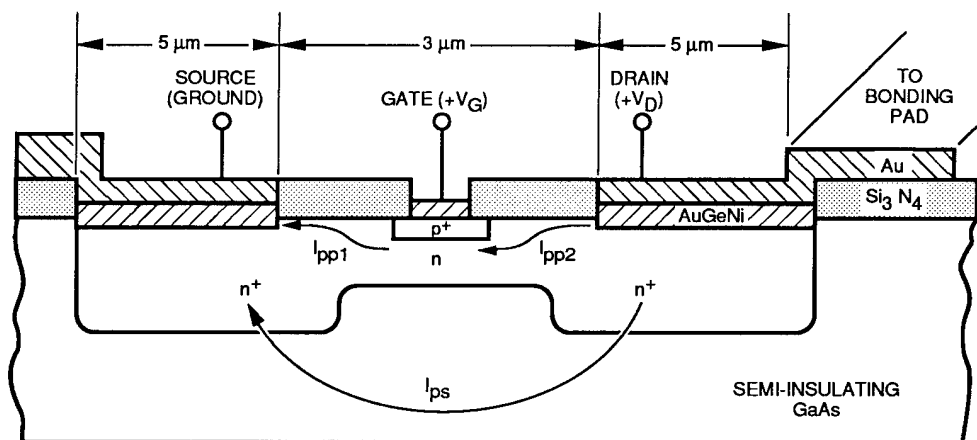


Figure 3-32. Cross section of enhancement mode GaAs JFET, indicating source-drain shunt current path through semi-insulating substrate (Zuleeg, Norrhoff, and Troeger, 1983).

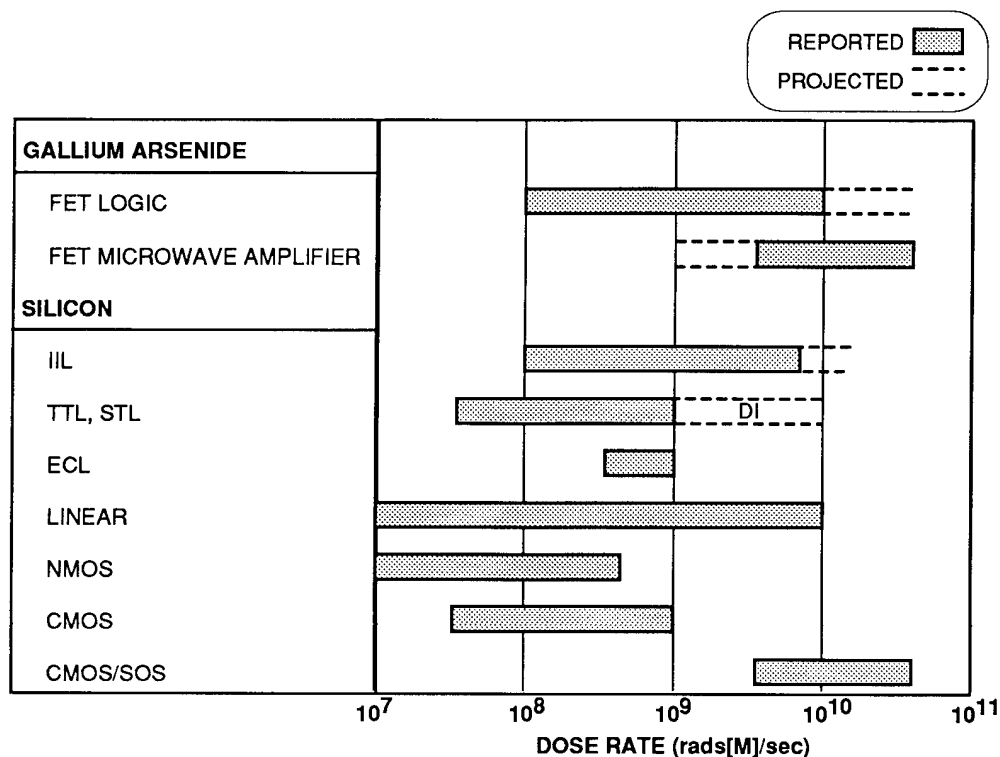


Figure 3-33. Reported and projected short-pulse dose-rate-upset thresholds (Simons, Donovan, and Hauser, 1977).

important to note that the only appreciable current flow through the cell occurs when the cell is switching states. During the brief switching transient, both n-channel and p-channel transistors turn ON and a direct, low-impedance path exists between V_{DD} and V_{SS} .

3.7.2 Upset Definitions

Although the discussion here is oriented to SRAM-type ICs, the information and definitions can be extended to any type of circuit. Memory-type circuits are addressed since they are typically the most widely used component and the corruption of stored critical data poses a significant problem for the ability of a system (strategic satellite, missile, etc.) to function in a nuclear weapon environment.

The types of upset that can occur in a transient ionizing dose environment include:

1. *Memory-cell upset:* An SRAM cell, shown in Figure 3-34, holds one bit of information via a stable complementary pair of voltages on nodes (1) and (2). A memory-cell upset occurs when the state of the cell is changed due to external stimulus, *e.g.*, a transient voltage perturbation causing the state of the latch to switch.
2. *Output voltage upset:* This type of upset occurs when the signal on the output pins is significantly disturbed by the transient. A commonly used standard definition describes upset as occurring when the voltage perturbation exceeds $(V_{DD} - V_{SS})/2$.
3. *Write-mode address upset:* Radiation-induced corruption of the SRAM address or address decode circuit upset can result in data being written into unknown locations. Thus, although the memory cells themselves have not upset, the net result is that "bad" data are stored at unknown locations.
4. *Pushout or SRAM access time delay:* The advent of a radiation event during certain portions of the read or write cycle can result in a momentary increase (pushout) in the time required to complete either the read or write cycle.

3.7.3 Integrated Circuit Upset

An IC upset can be delineated into two separate components: (1) local upset, and (2) global upset. Local upset refers to the operation of an IC element (*e.g.*, memory cell, inverter, etc.) due to the photocurrents generated within that element.

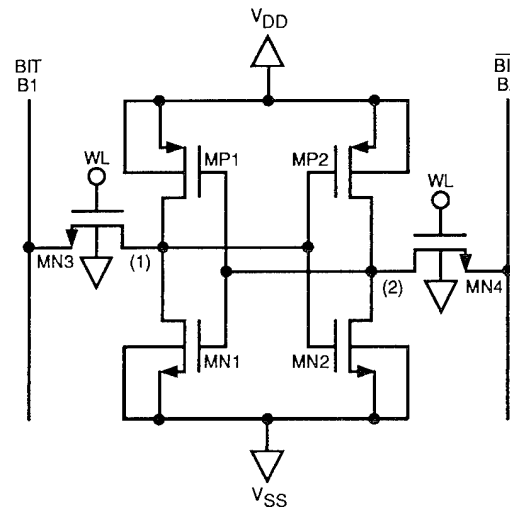


Figure 3-34. CMOS SRAM cell (Ma and Dressendorfer, 1989).

A schematic representation of this effect is shown in Figures 3-35 and 3-36, where P_1 and P_2 are the p-channel drain photocurrents, P_3 and P_4 are the n-channel drain photocurrents, and P_5 is the p-well photocurrent. Moreover, the local upset results from the direct interaction of P_1 through P_4 , with the signals stored on information nodes (1) and (2).

The effect of these local photocurrents is explicated in the following paragraphs, paraphrased from Ma and Dressendorfer (1989). The p-channel and n-channel devices within a CMOS RAM cell each have different equilibrium depletion region volumes for prompt photocurrent collection. Diffusion collection volumes are also different for n- and p-channel devices in CMOS ICs. In the case of one transistor type, the volumes are constrained by the volume of the well; in the other, by the adjacent epitaxial or substrate volume. These basic design and operation features result in different values for each of the local photocurrents [P_1 , P_2 , P_3 and P_4 of Figure 3-36]. The resulting differential "noise" results in destabilization of the logic state of a RAM cell during

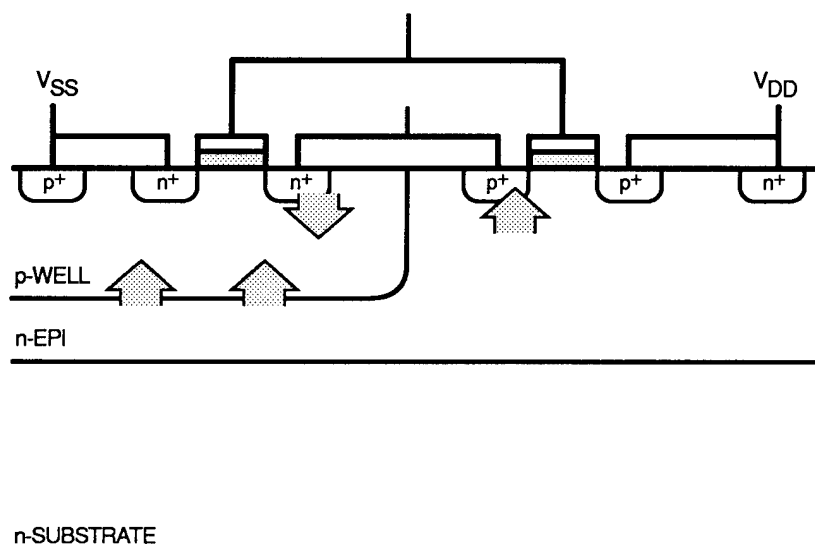


Figure 3-35. Local photocurrents produced by a dose-rate event in a CMOS inverter (Ma and Dressendorfer, 1989).

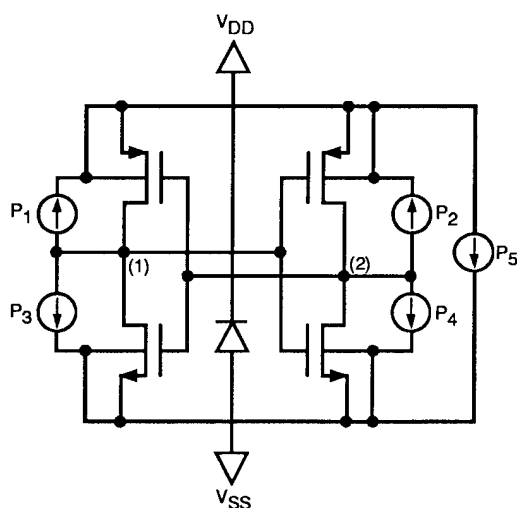


Figure 3-36. Local photocurrents produced by a dose-rate event in an SRAM cell (Ma and Dressendorfer, 1989).

dose-rate events. For instance, in p-well CMOS RAM cells, the OFF p-channel device has the largest collection volume of the transistors in the cell. Local photocurrents can drive the low node high and reverse the logic state. Local photocurrents dominate the cell response to dose-rate events in technologies that use insulating substrates [Section 3.5].

Global upset, the second component of IC upset, can be the result of radiation-induced photocurrents reducing the static excitation voltage ($V_{DD} - V_{SS}$) to the entire IC and to the indi-

vidual IC elements (e.g., memory-cell array, etc.) as well. This effect has been denoted as railspan collapse since it is not the absolute value of either rail (i.e., V_{DD} or V_{SS}) that is important but the difference, or span ($V_{DD} - V_{SS}$), that is critical (Massengill and Diehl, 1984). Railspan collapse depends upon the robustness of the ON-chip power distribution system and the external power distribution system impedance, including the impedance of the IC package and any decoupling capacitors used (Massengill, Diehl, and Wrobel, 1985; Massengill, Diehl, and Browning, 1986). It should be noted that these effects only become important considerations at very high dose rates (e.g., $> 1 \times 10^{11}$ rads[Si]/sec for SOI technology and $\geq 1 \times 10^9$ rads[Si]/sec for bulk technology). In order to achieve high-dose-rate upset levels, special low-inductance packages must be used to minimize inductive railspan collapse. Furthermore, decoupling capacitors need to be inserted in the package on the V_{DD} and V_{SS} circuit, large capacitors (external to the package) placed in close proximity to the external V_{DD} and V_{SS} pins, and multiple V_{DD} -to- V_{SS} pin paths used. An example of such an arrangement is the 256k CMOS/SOI SRAM developed by Texas Instruments, which uses four V_{DD} pins, four V_{SS} pins, and two (in-package) 24-pF V_{DD} and V_{SS} decoupling capacitors to achieve a dose-rate tolerance of $\geq 1 \times 10^{11}$ rads(Si)/sec.

Another aspect of global upset is reduction in the differential supply voltage ($V_{DD} - V_{SS}$) to a memory cell due to the finite resistance of the internal IC power distribution runs. This sag in the local V_{DD} voltage and rise of the local V_{SS} voltage due to photocurrent contributions can lower the differential voltage to a memory cell to the point that a stable state cannot be maintained.

The following discussion of dose-rate upset describes a methodology for its simulation in VSLICs and provides an example, again following the work of Massengill and Diehl (1984) and Massengill (1987).

An unambiguous, complete simulation of transient-dose-rate effects in an IC is not possible since it would require the simultaneous analysis of thousands to millions of pn junctions. However, a full chip-level simulation can be accomplished through use of a procedure (Massengill and Diehl, 1984) that incorporates the following steps:

1. *Circuit-level simulation of the individual RAM cell to determine the subcircuit response to transient-radiation-induced currents.* This capability is not routinely included in circuit-level simulation codes such as SPICE. Transient-radiation-induced current simulation requires incorporation of dynamically controlled current sources representing the total diffusion and drift photocurrents onto each device node as a function of time and of the terminal characteristics of the modeled devices. The current produced by the sources is a function of the amplitude and time profile of the dose-rate pulse and also of the characteristics of the device materials, particularly minority-carrier lifetime. Figure 3-37 shows the photocurrent waveforms for a CMOS RAM cell. The photocurrent is injected in the locations designated in Figure 3-36 (P_1 through P_5) in order to simulate the response of each of these SRAM cells to dose-rate events. Note that in the cell, the well-junction photocurrent is much larger than that of any (or all) of the photocurrents collected at the transistors composing the cell.
2. *Extraction of a simple, two-component model of the I-V characteristics of one RAM cell,* where V is the railspan ($V_{DD} - V_{SS}$) and I is the total rail-to-rail current drawn during an event. This step requires linearizing the device response determined in the previous step. Figure 3-38 shows such simulated characteristics for the RAM cell on the bulk silicon substrate and the best fits obtained by linear regression.
3. *Incorporation of the linear RAM cell models into a global, linear network that represents the interconnect network supplying voltage to the cells.* The resulting network, depicted schematically in Figure 3-39 includes the finite-resistance values of the interconnections and provides a chip-level representation of the power-supply distribution scheme of the IC modeled here [depicted in Figure 3-40].
4. *Simulation of the network to determine the minimum voltage span across each RAM cell in the IC as a function of the dose-rate amplitude and pulse length.* Figure 3-41 is a representation of the RAM arrays in normal operation (without transient ionizing radiation). Simulations of the bulk array subject to dose-rate events above and below the threshold for transient upset are depicted in Figure 3-42.
5. *Assessment of the effect of the simulated railspan on the RAM cell capability to retain stored information.* The minimum value of railspan required for information retention is a circuit-design-dependent parameter, obtainable either by simulations or by experimental measurement of the minimum

operating voltage of an unirradiated entire RAM IC. For the 10-volt chip used in examples of Figures 3-41 and 3-42, the minimum railspan required for reliable state storage is approximately 1.6 volts.

The accuracy of the technique described above for predicting IC response to dose-rate events rests on the assumption that subcircuit (local) and chip-level (global) responses are not strongly interdependent. Certainly, for very short, high-am-

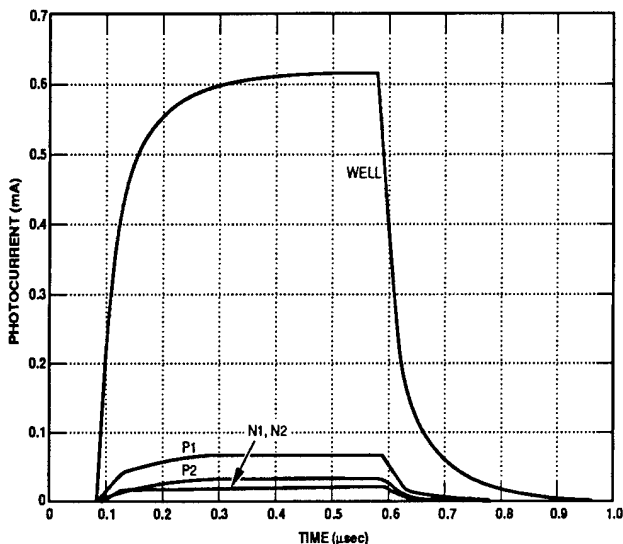


Figure 3-37. A photocurrent waveform typical of a CMOS SRAM cell fabricated on a bulk silicon substrate exposed to neutrons in order to reduce minority-carrier lifetimes (Massengill, 1987).

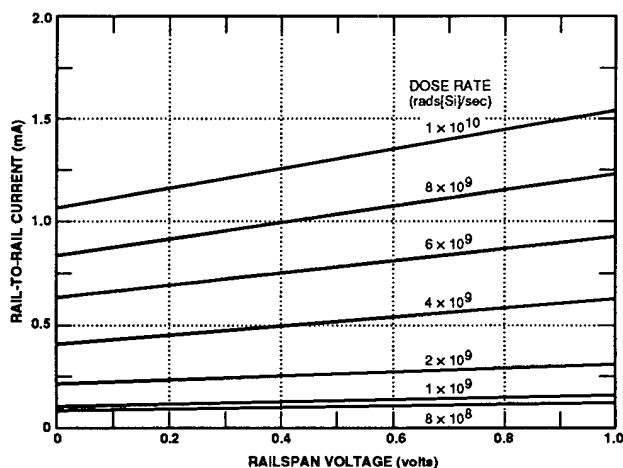


Figure 3-38. Rail-to-rail current drawn by a simulated RAM cell as a function of railspan voltage for various dose rate (Ma and Dressendorfer, 1989).

plitude pulses, and/or for ICs with very “hard” rails or small global photocurrents, local effects influence the upset level of cells. A graphic technique for including the interaction of local and global effects has been developed (Ackerman *et al.*, 1986) and indicates that global effects are strongly dominant in bulk and epi-CMOS circuits, whereas local effects dominate in CMOS/SOI devices (Davis *et al.*, 1985; Mikawa and Ackerman, 1987). These devices have smaller total photocurrents than comparable silicon-substrate devices because SOI ICs do not contain the well junctions that collect the majority of photocurrent in junction-isolated CMOS ICs. CMOS/SOS devices also have small local photocurrents, due to the absence of large well junctions, and therefore exhibit dose-rate upset thresholds that are generally higher than bulk and epi-CMOS devices of comparable design. Dose-rate upset in CMOS/SOS is attributable to radiation-induced photoconductivity of the sapphire substrate (Kjar and Kinoshata, 1973), which used in the renders the substrate ineffective in isolating information- storage elements. A simulation code has been developed to predict dose-rate upset thresholds and bit-error patterns for devices that upset by this mechanism, but it is presently tailored to model devices fabricated on semi-insulating GaAs (Brown *et al.*, 1986).

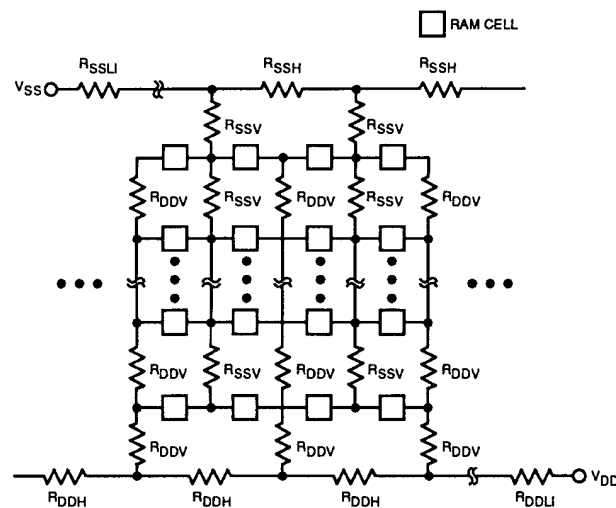


Figure 3-39. Global linear network supplying voltage to the cells and including linear models of RAM cells (Ma and Dressendorfer, 1989).

For nonregular arrangements of subcircuits, such as those found in devices incorporating combinational logic (such as microprocessors) and/or for devices with interconnect networks that cannot be reduced to a planar network representation, Steps 2 through 4 [above] must be modified. Such analyses require a special design code that uses state-of-the-art numerical techniques in order to handle the dynamic interactions of the large numbers of junctions encountered in modern ICs (Massengill, 1987). With such a full-scale simulator, linearization of RAM cell characteristics is not required, nor is construction of the chip-level representation of the

interconnect network including these models. The cell characteristics are simulated *in situ*, local and global interactions are automatically simultaneously included, and the noise margin or voltage railspan maps of the IC nodes are produced as output. The full simulator results confirm those of the simpler, modular method for the examples provided here (Massengill, 1987).

Using any of these techniques, simulation of voltage railspan as a function of dose-rate excitation allows estimates of the dose-rate upset threshold (the minimum dose-rate amplitude for a given pulse width for which at least one logic state is upset).

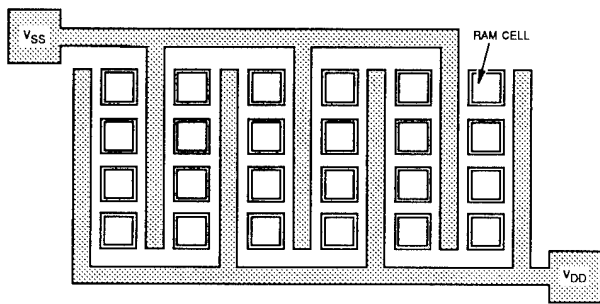


Figure 3-40. Chip-level representation of the power-supply distribution typical of a CMOS SRAM.

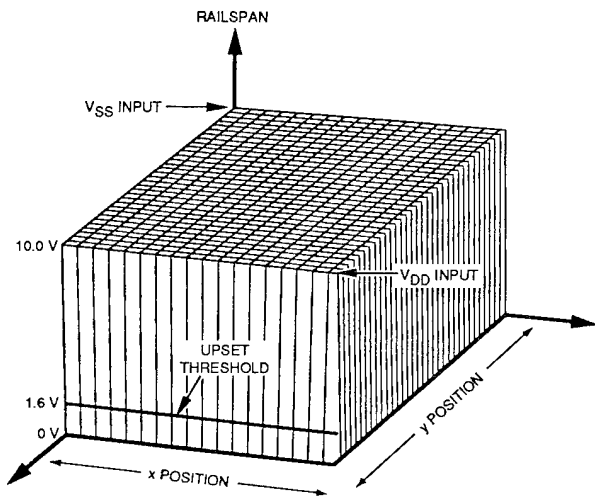
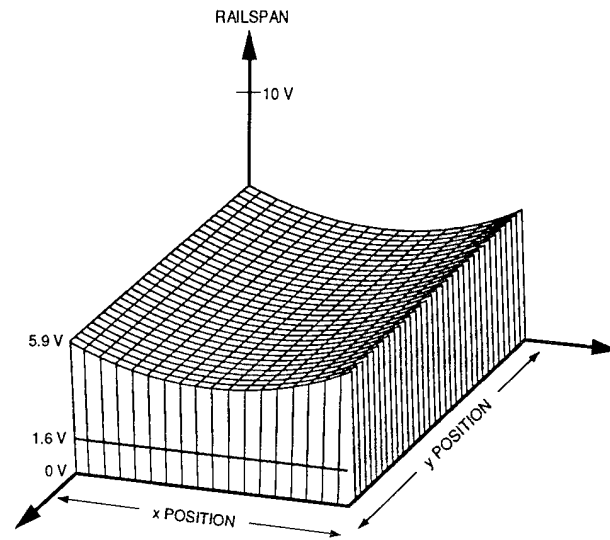


Figure 3-41. Representation of the voltage span across RAM cells within an array under normal unirradiated operating conditions (Ma and Dressendorfer, 1989).

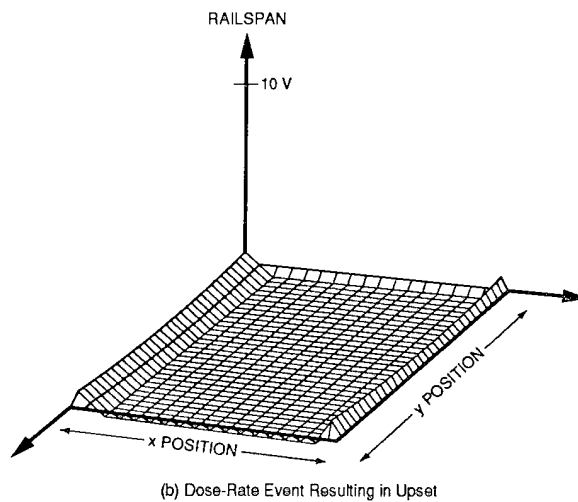


Figure 3-42 (a, b). Representation of the voltage span across a bulk RAM cell array subjected to dose-rate events (Ma and Dressendorfer, 1989).

3.7.4 Pushout Upset

As previously stated, pushout is an increase in SRAM access time that results from transient ionizing irradiation (Murrill and Self, 1993). This particular upset mode may limit device hardness during operation (*i.e.*, dynamic versus static) and in general occurs at lower dose-rate levels than static-mode upset [Figure 3-43]. Dynamic testing can be accomplished in two basic ways: (1) unsynchronized, where a wide radiation pulse ($\geq 1 \mu\text{sec}$) that encompasses the SRAM operating cycle is applied; or (2) synchronously, where a narrow radiation pulse (20 to 50 nsec) is incrementally moved through the SRAM cycle such that every portion of the cycle is exposed to radiation. Synchronous testing permits every sensitive region of the SRAM operation to be subjected to radiation-induced transients.

The actual cause of pushout is attributed to the interaction of the photocurrents with the operation of the SRAM timing and decode circuits. Moreover, as can be seen in Figure 3-44, the exact placement of the radiation pulse in the SRAM cycle has a dramatic effect on the hardness of the IC. In Figure 3-44, P indicates a transient upset failure, defined to be an increase in access time

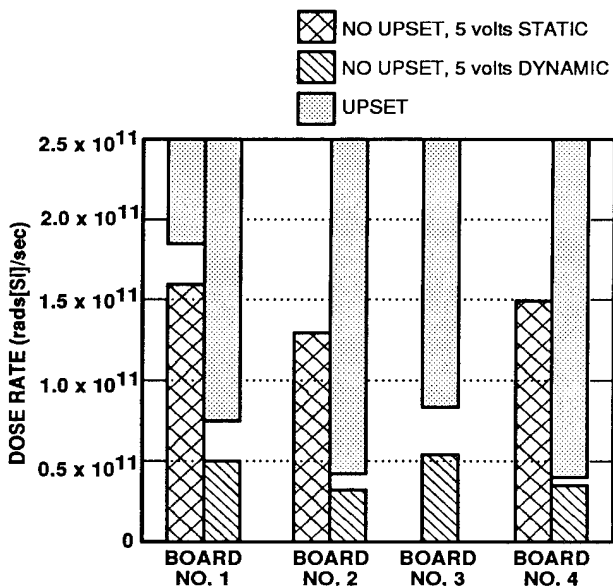


Figure 3-43. Range of SRAM upset levels due to pushout (Murrill and Self, 1993).

(address transition to data transition) greater than the specified access time, which for this SRAM was 40 nsec. Note that P-type upsets were only seen when the radiation pulse was placed at the beginning of each cycle, $t(\gamma)$ being the time of irradiation and t_0 the start of the read cycle (defined as the time of the address transition).

3.8 Latchup in Integrated Circuits

Latchup is a major concern in both bulk CMOS and bipolar ICs. The problem is caused by parasitic bipolar transistor structures that are inherent in bulk technology CMOS and bipolar ICs. These parasitic structures can be activated (latched) by transient ionizing radiation events (as well as electrical stimuli). When activated, the parasitic structure assumes a low-impedance state that can interrupt the normal operation of the IC and, in most situations, result in circuit malfunction. Once activated, power must be removed to eliminate the latched condition.

Latchup can occur in several ways, however, the dominant method is the activation of a parasitic four-layer (pnpn) structure, equivalent to a silicon-controlled-rectifier (SCR), which is found in both CMOS and many types of bipolar ICs, *e.g.*, transistor-transistor logic (TTL), Schottky TTL (STTL), current-mode logic (CML), emitter-coupled logic (ECL), etc.

Four-layer latchup occurs in a microcircuit when a parasitic pnpn path is triggered into a low

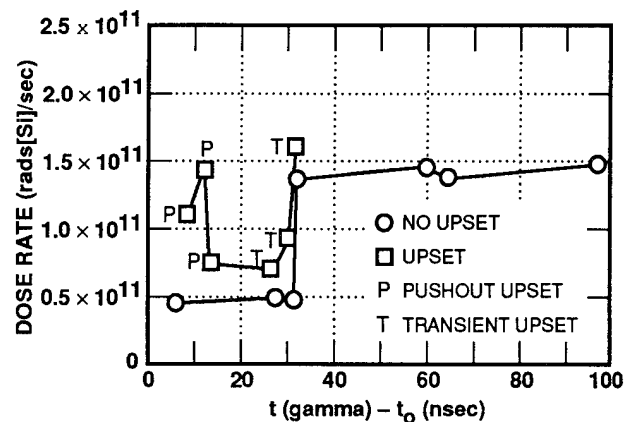
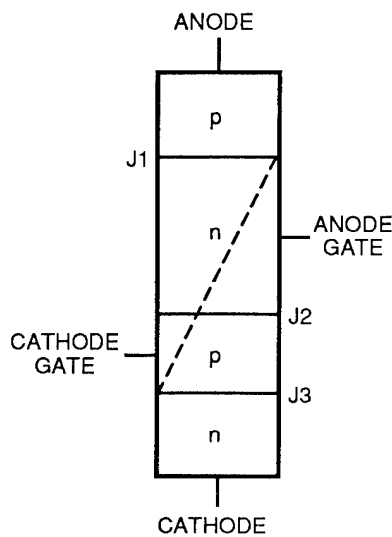


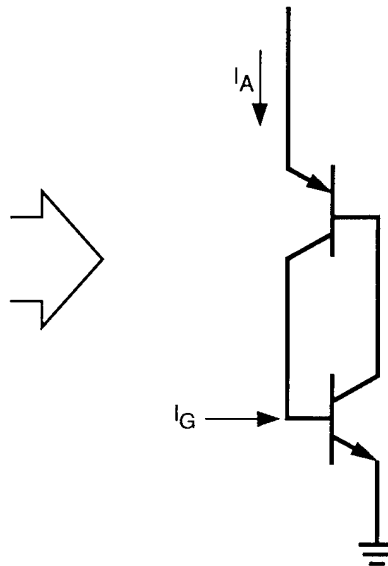
Figure 3-44. Effect of radiation pulse timing on SRAM pushout and upset levels (Murrill and Self, 1993).

conductance state. The basic characteristics of four-layer latchup are illustrated in Figure 3-45. The nomenclature used is given in Figure 3-45(a). The four layers are the anode, anode gate, cathode gate, and cathode with junctions J1, J2, and J3. As shown in Figure 3-45(b), the pnpn structure can be represented by two merged transistors. The dc current-voltage (I-V) characteristic of the path is shown in Figure 3-45(c) for positive anode voltage with the gates open. When the positive voltage is large enough to avalanche J2, the anode current I_A reaches a value where the product of the common-emitter current gains

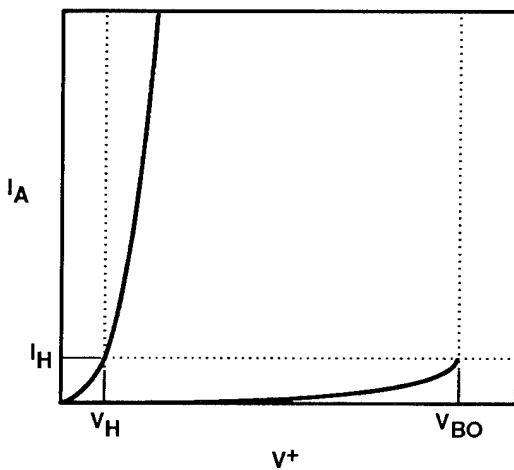
of the two parasitic transistors is greater than one. At this point, regenerative action occurs between the transistors and both are switched to a saturated condition. As illustrated in Figure 3-45(d), the minimum current for which this condition occurs is called the holding current I_H . The anode-cathode voltage drop in the low-conductance ON state is the forward voltage drop on the pnp emitter-base junction plus the $V_{CE(SAT)}$ of the parasitic npn, plus the voltage drop across the resistance (IR) through the pnp base region. The minimum voltage in the ON state is the holding voltage V_H . A pnpn path will not exhibit the low conductance



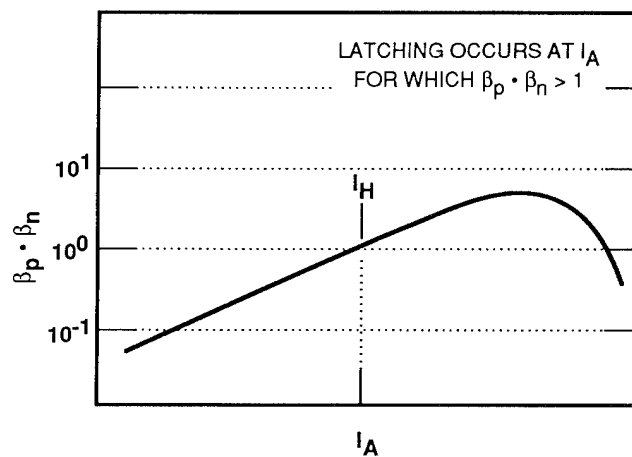
(a) Nomenclature for pnpn Path



(b) Two-Transistor Analog of pnpn Path



(c) Positive Voltage I-V Characteristic



(d) Current Gain Product Versus Current for pnpn Path

Figure 3-45 (a, b, c, d). Four-layer latchup (pnpn) characteristics (Pease and Alexander, 1982).

state, *i.e.*, it will not latch, if the current gain product is less than one at all anode currents. Also the path will not sustain a latch if the current is limited to a value less than I_H or the voltage to a value less than V_H .

In addition to the four-layer latchup phenomena, latchup due to second breakdown and snapback will also be discussed.

3.8.1 Four-Layer Latchup in Bipolar Transistors

As previously stated, latchup can occur in a variety of bipolar technology devices. However, in each case, its cause can be attributed to the activation of the parasitic four-layer device. Several types of bipolar devices exist that are not susceptible to latchup (*e.g.*, integrated injection logic [I²L]) due to their inherent design and/or operating characteristics. Also, those technologies that have been fabricated using an insulating substrate are generally latchup-free.

The following discussion addresses several types of bipolar transistors, which are investigated to identify the presence of a parasitic four-layer device and the potential for the parasitic device to satisfy the basic condition required to latch (*e.g.*, $\beta_1 \times \beta_2 > 1$).

In the first example, a TTL I/O circuit that is part of a larger device will be examined. This I/O circuit is illustrated in Figure 3-46, showing two adjacent npn transistors in an isoplanar I/O circuit. The parasitic pnpn path is from the base region of one transistor through the substrate and out through the collector of an adjacent transistor. With no current in the substrate, the potential on the cathode gate is zero and J3 is reverse-biased. However, under ionizing radiation, a rather large photocurrent can occur in the substrate that may forward-bias J3 and temporarily latch the pnpn structure if the anode-to-cathode bias is $>V_H$ and $\beta_p \times \beta_n > 1$. Once the path is turned on, J3 can be maintained in forward bias by the shunt resistance R_S between the cathode gate and the substrate ground contact point. If the ground contact to the substrate is made on the platform to which the die is bonded, then R_S will be given by the spreading resistance through the substrate to the back surface. If the ground contact is made on the top surface of the chip, R_S will be the resistance through the substrate to the nearest ground contact. The substrate resistivity for bipolar LSI circuits usually ranges from 1 Ω -cm to 20 Ω -cm. Although the potential for latchup exists in this first example, it should be noted that the transis-

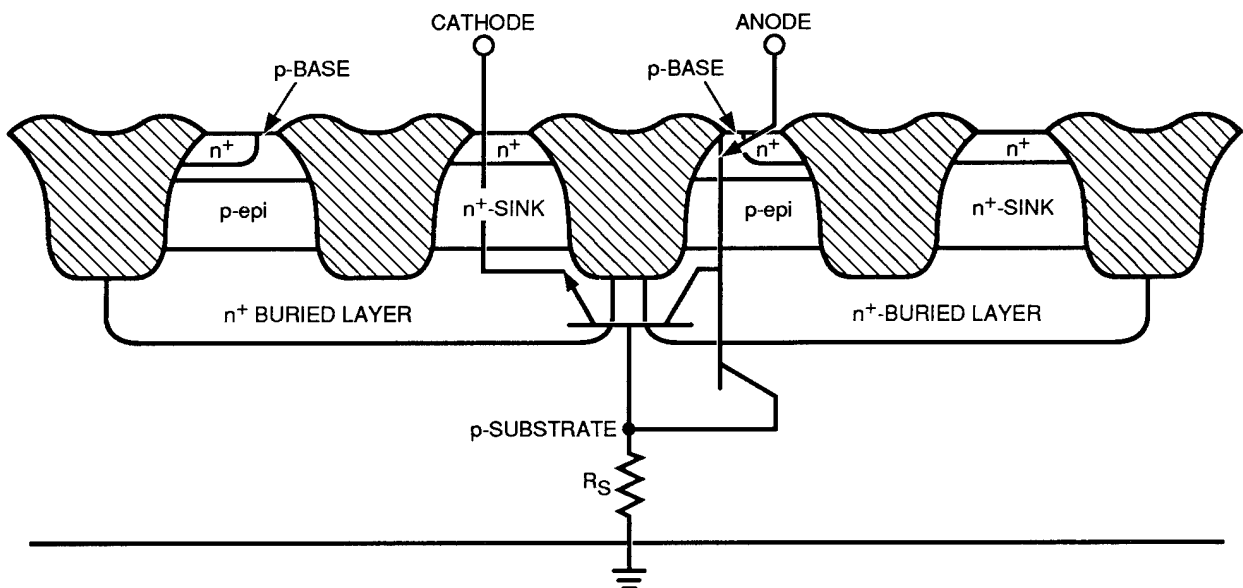


Figure 3-46. Cross section of two closely spaced isoplanar npn transistors showing the substrate latchup path (Pease and Alexander, 1982).

tor gains ($\beta_1 \times \beta_2$) for the parasitic npn and pnp transistors [shown in Figure 3-46] for an actual device, the Fairchild 9408 Microprogram Sequencer, proved to be less than one. Thus, latchup is precluded for this particular IC.

In the second example, integrated Schottky logic (ISL) and Schottky transistor logic (STL), two forms of high-density bipolar logic, are analyzed. Both ISL and STL use single-input, multiple-output inverters as the basic logic unit. In ISL, the npn switch is kept out of deep saturation by a vertical parasitic pnp transistor and in STL by a collector-base Schottky clamp. The isolated outputs are Schottky contacts to the npn collector region. An ISL two-output inverter is shown in Figure 3-47.

Within the ISL/STL logic array, the only parasitic pnpn path is from the Schottky collector (output) through the epitaxial layer, the p-type npn base region, and the npn emitter. Such a path exists since the Schottky contact can function as a p-type region, injecting minority carriers at high current density.

An analysis of this parasitic pnpn path for the ISL/STL inverter shows that the pnpn path is an integral part of the circuit, as illustrated in Figure 3-48 for an STL inverter. Since the inverter input node is the cathode gate of the parasitic SCR, a positive voltage pulse on this node will latch the SCR and the output will remain in the ON state until power is removed. Thus, if this path could be latched, the inverter output would always be low and the circuit would not function properly. Proper electrical operation of the circuit guarantees that the path does not latch. Since the parasitic pnp gain is higher at elevated temperature, a useful latchup screen for this circuit would be an elevated-temperature test.

The results of the latchup analysis on this ISL/STL gate array are: (1) if the circuit is operational under elevated temperature, the only potential latchup path is one between closely spaced components involving the substrate; and (2) a potential for latchup exists. Thus, to prevent latchup, gold doping (Dawes and Derbenwick,

1976) was used to degrade minority-carrier lifetimes and reduce the $\beta_V \times \beta_L$ product to <1 (where β_V = the gain of the vertical transistor and β_L = the gain of the lateral transistor).

3.8.2 Four-Layer Latchup in CMOS Integrated Circuits

The formulation of the parasitic structure is described in the following discussion [paraphrased from Troutman (1986)]. A simple inverter circuit will be used as an example since this circuit configuration is frequently incorporated in the implementation of more complex ICs.

Figure 3-49 shows the cross section of an inverter circuit, and in Figure 3-50 the equivalent bipolar parasitic transistor circuit is superimposed on this cross section. Note that there are two vertical pnp and two lateral npn transistors. Both the n-well and the p-type substrate serve two functions. The n-well is the base for either vertical pnp and the collector for either lateral npn. Likewise, the p-type substrate serves as the base for either lateral npn and the collector for either vertical pnp. Each of the collector regions can develop a voltage drop between the collector/base junction and the collector contact, which can be modeled as a collector resistance. In addition, current flowing through some fraction of the collector resistance can forward-bias the emitter-base junction of the opposite bipolar device if the IR drop exceeds several tenths of a volt.

Resistor R_{w1} in Figure 3-50 represents resistance from the n-well contact to the intrinsic base region of the first vertical pnp, while resistor R_{w2} represents resistance from the intrinsic base region of the first to the second. $R_{w3}(R_{w4})$ represents the resistance from the intrinsic base region of VT2 to the point $X_1(X_2)$, where the current from LT1(LT2) is collected. Electrons injected from the n^+ emitters are not all collected at one point, but the picture has been somewhat simplified to illustrate the lumped equivalent model. In some cases (particularly for epi-CMOS), the points X_1 and X_2 can be considered the same; then, the parallel combination of R_{w3} and R_{w4} can be replaced by a single resistor. In a similar manner, R_{s1} represents resistance from the sub-

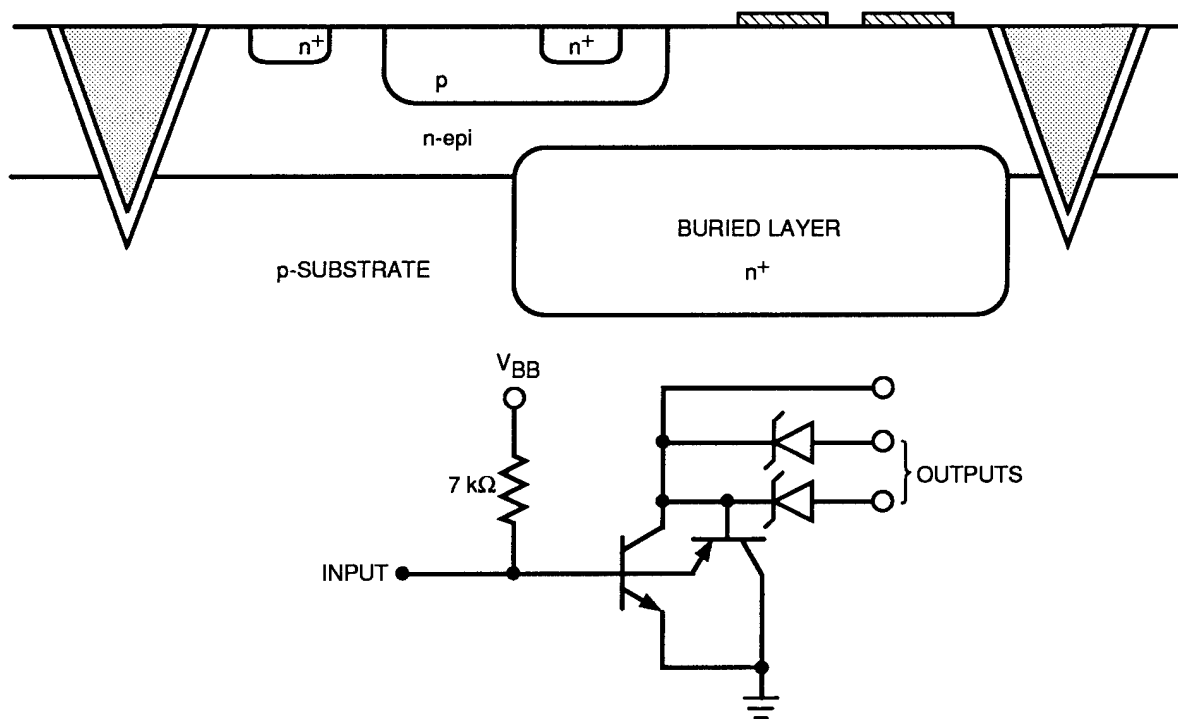


Figure 3-47. Cross section and circuit diagram of a two-output ISL inverter (Pease and Alexander, 1982).

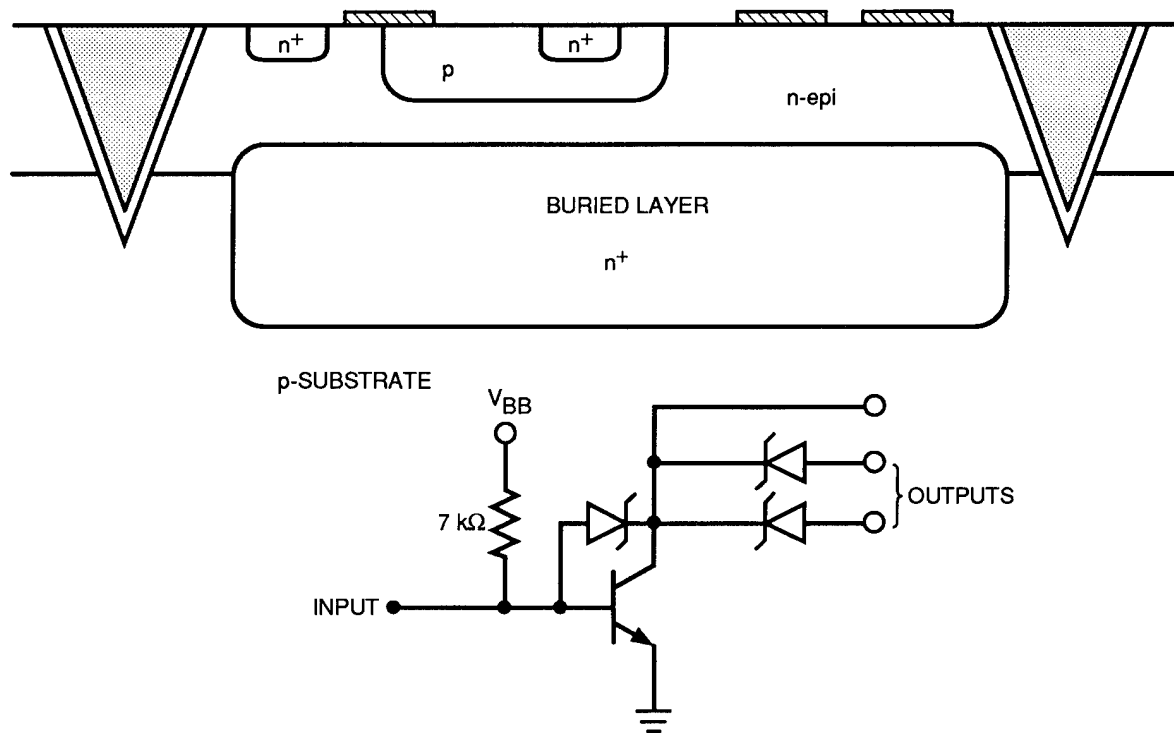


Figure 3-48. Cross section and circuit diagram of a two-output STL inverter (Pease and Alexander, 1982).

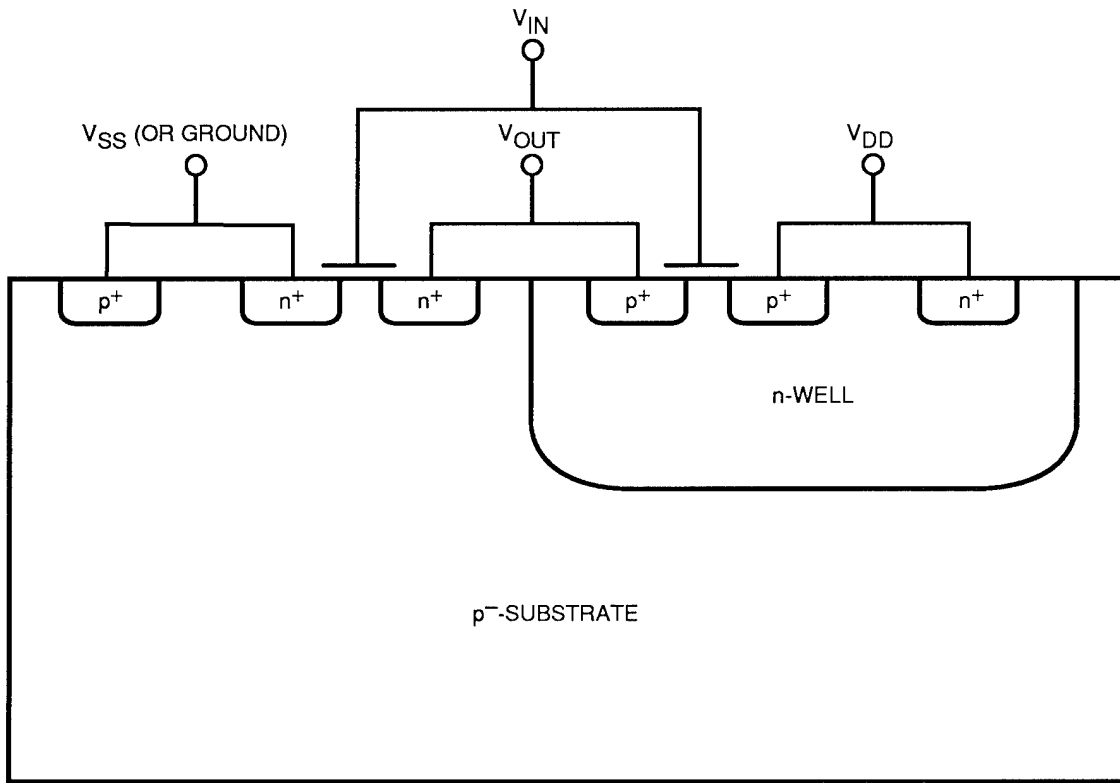


Figure 3-49. Cross section of inverter circuit in n-well CMOS (Troutman, 1986).

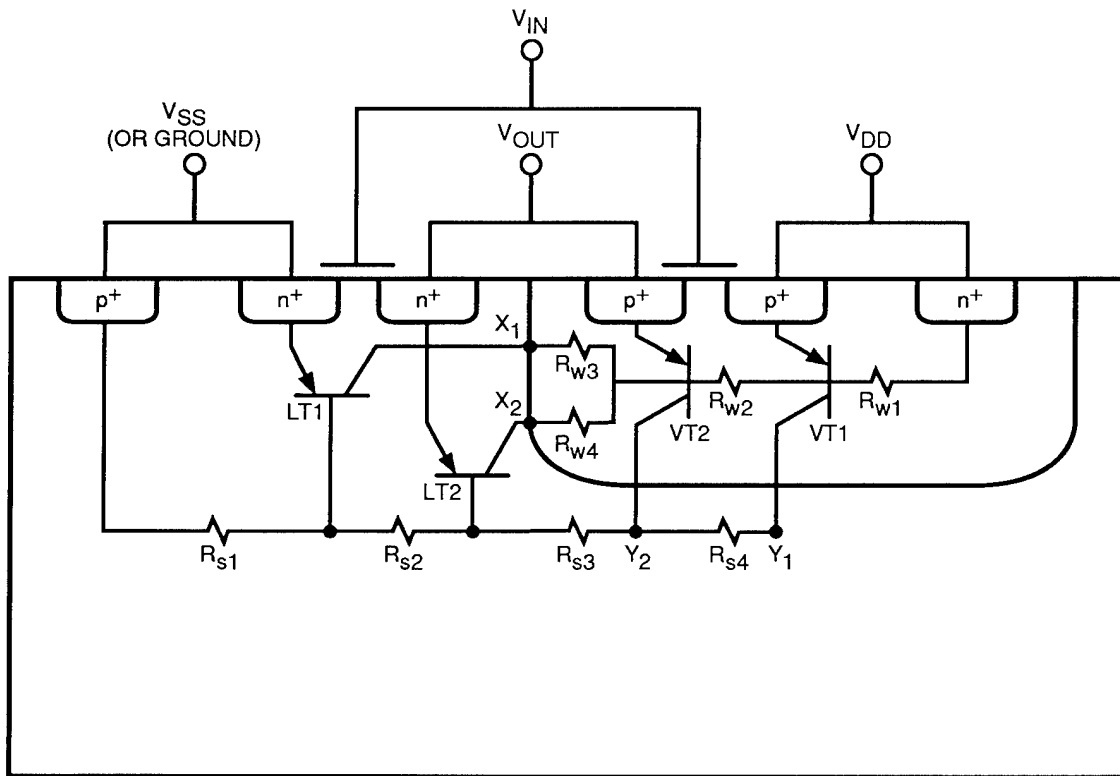


Figure 3-50. Parasitic bipolar portion of an n-well CMOS inverter (Pease and Alexander, 1982).

strate contact to the intrinsic base region of the first lateral npn, and R_{s2} represents resistance between the base regions of LT1 and LT2. The resistor R_{s3} (R_{s4}) represents resistance from the base intrinsic region of LT2 to the point Y_1 (Y_2), where the current from VT1 (VT2) is collected. Again, the physical behavior has been simplified for the sake of a lumped equivalent circuit.

The total equivalent circuit for the inverter circuit has the form shown in Figure 3-51. The simple CMOS inverter, consisting of an n-channel driver and a p-channel load, is the desired result of a given layout. In parallel with it, however, is the circuit formed by the parasitic bipolars and associated resistors. Under normal operations, the circuit performs as an inverter, and the bipolar portion can be ignored. Under certain conditions, the bipolar operation can dominate the behavior of the total circuit. In particular, if the bipolar circuit switches from its normally high-impedance state to a low-impedance state, the power supply then sees a low-im-

pedance path to ground. If the current from the supply is not limited somehow, an irreversible change can take place, such as the fusing of an aluminum line somewhere in the chip's power supply or ground line. Even if the current is limited so that no damage occurs, however, the pnpn low-impedance state could cause a circuit to malfunction. To guarantee accurate circuit behavior, the pnpn must remain in its high-impedance state.

The actual circuit used to model the parasitic bipolar devices in a CMOS inverter structure is shown in Figure 3-52; the corresponding I-V characteristic is shown in Figure 3-53. Note that the description of the operation of this structure is similar to that provided for bipolar transistor latchup explanation; it is repeated here for completeness.

The I-V characteristic shown in Figure 3-53 schematically depicts the high- and low-impedance states. Any characteristic observed for a

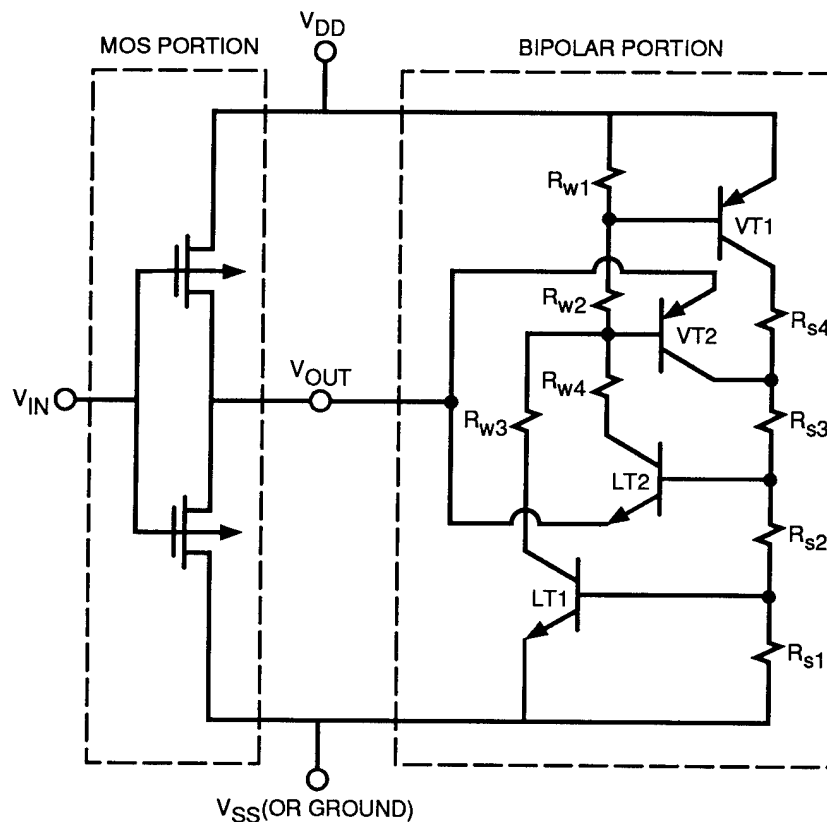


Figure 3-51. Complete circuit schematic for n-well CMOS inverter (Troutman, 1986).

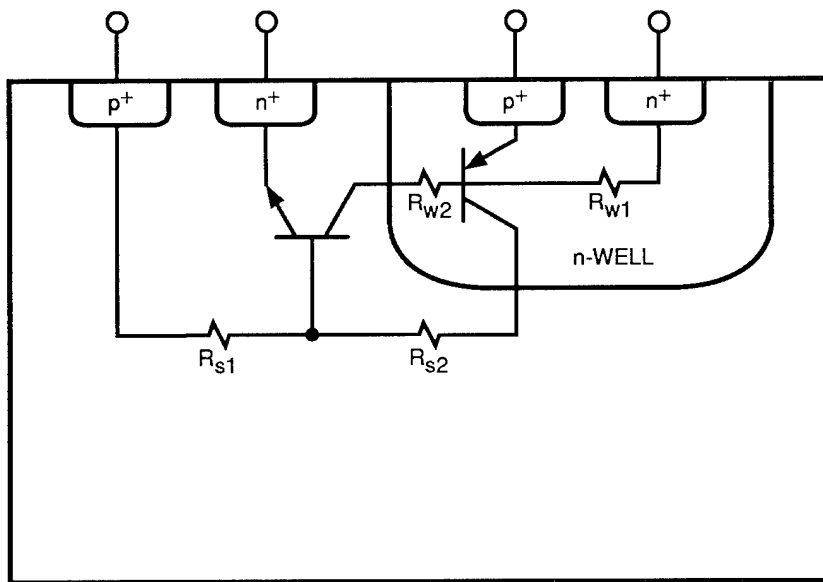


Figure 3-52. Parasitic bipolar portion of a four-terminal pnpn structure [the most common version of the lumped-element model] (Troutman, 1986).

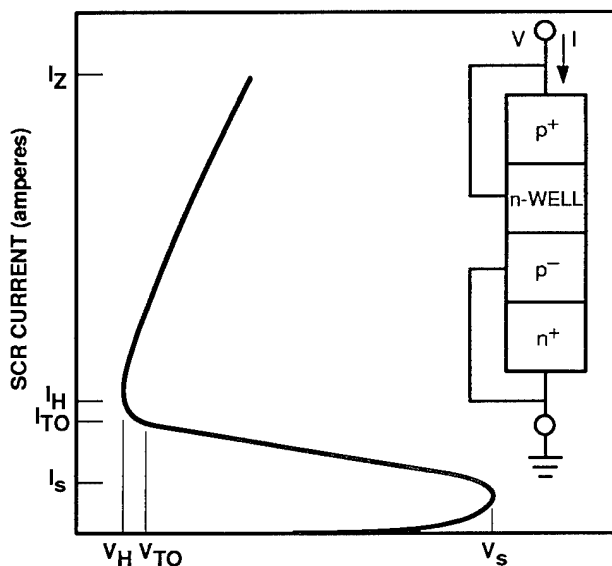


Figure 3-53. Illustrative pnpn I-V characteristic (Troutman, 1986).

specific pnpn structure depends on how switching is initiated. Since a pnpn structure is really a four-terminal device, the observed characteristic also depends on the terminal conditions of the n-well and substrate contacts. In Figure 3-53, these are shown short-circuited. Two key points identified on this characteristic are: (1) the intersection of the switching point current I_s with the switch-

ing point voltage V_s , and (2) the intersection of the holding current I_H with the holding voltage V_H . I_s marks the transition from the high-impedance region (also referred to as the blocking state or OFF region) to the negative differential resistance region, and I_H marks the transition from the negative differential resistance region to the low-impedance region (also referred to as the latched or ON region). A stable high-impedance state is defined by $I < I_s$, and a low-impedance state by $I_H < I < I_z$, where I_z is the radiation current of the device. At the turn-off point (I_{TO}), reverse bias on the center junction is zero. The blocking and latched regions are also referred to as states since the parasitic pnpn device can stably reside in each and can be switched from one to the other.

During normal CMOS IC operation, the pnpn maintains its high-impedance blocking state, and the voltage supplies for the IC pass all their current through the MOSFET structures. If, however, minority carriers are somehow introduced into a bipolar base region, the pnpn can go into its low-impedance state and latch the cell. Using the structure of Figure 3-52 as a reference, note the vertical npn bipolar structure, which can be turned on if any n^+ -diffusion injects enough electrons into its p-well base. In a positive-feedback

configuration with the vertical npn is a lateral pnp bipolar transistor. Holes from a p⁺ source/drain diffusion can be injected into the n-substrate base of the pnp. For such carrier injection to result in latchup, the following conditions must be satisfied:

1. The loop gain of the relevant pnpn [in Figure 3-53] must exceed unity for the circuit to latch, *i.e.*, $\beta_{\text{pnp}} \times \beta_{\text{nnp}} > 1$. Under this condition, the positive feedback forces the loop to draw current to the limit of the power supply's sourcing capability (or the circuit's current sourcing capability).
2. A triggering condition must allow the loop to achieve the current level required to switch itself ON (latched).
3. The IC bias supply and associated circuitry must be capable of supplying at least the holding current and voltage required to sustain the latch once it is initiated.

Latchup can be initiated electrically by signals applied to IC terminals, or it can be triggered by radiation events. Here, the focus is on radiation-induced latchup. The SCR may be turned ON by a radiation-induced electrical transient, by ionizing radiation characteristics of dose-rate events (Brucker, 1977), or by a single event (Kolasinski *et al.*, 1979; Soliman and Nichols, 1983). Each of these triggering mechanisms injects minority carriers into the base of the parasitic bipolars. Ionizing radiation from dose-rate events can inject current across the well/substrate junction. For p-well CMOS, the photocurrents from generated majority carriers, *i.e.*, electrons in the substrate (holes in the well), act as base currents of the parasitic bipolar devices and tend to turn on the SCR. The heavy ions present in galactic cosmic rays and solar flares produce long ionization tracks that can also provide carrier injection to initiate latchup. Several researchers have investigated this mechanism using heavy ions accelerated in cyclotrons (Kolasinski *et al.*, 1979; Nichols *et al.*, 1986; Shiono *et al.*, 1986; Soliman and Nichols, 1983). Other experimental tech-

niques for latchup investigations include the use of radioactive ²⁵²Cf as a high-LET particle source (Reier, 1986; Stephen *et al.*, 1984a) and a scanning electron microscopy (SEM) to identify latchup paths (Dressendorfer and Armendariz, 1980). Theoretical models for heavy-ion-induced latchup are also available (Shoga and Binder, 1986).

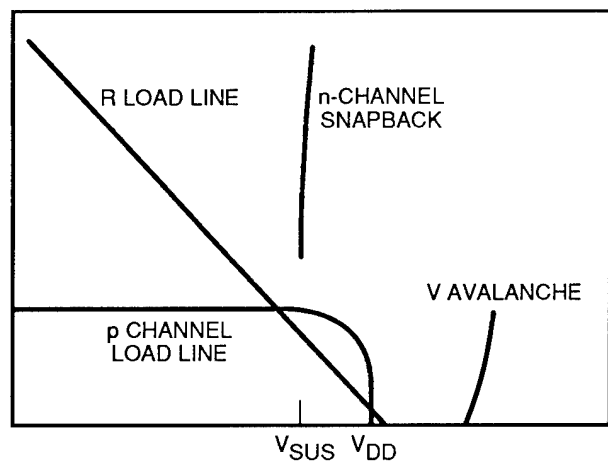
3.8.3 Other Latchup Mechanisms

3.8.3.1 Snapback

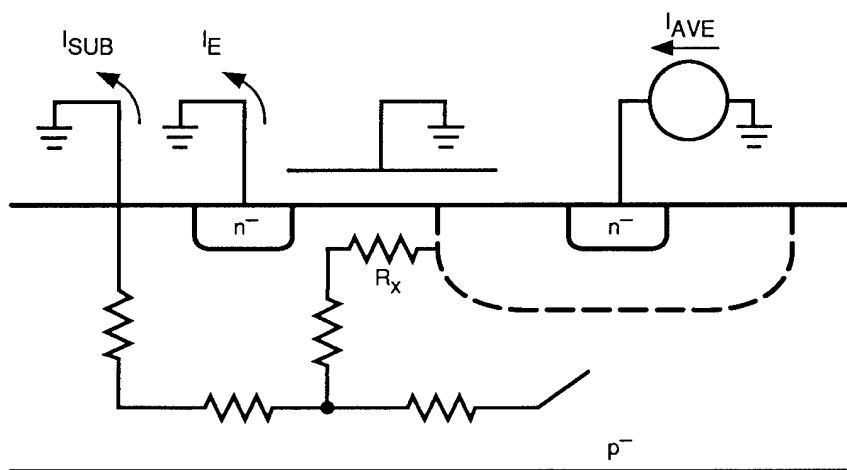
Latchup in n-channel devices can also be caused by an effect called snapback (Ochoa *et al.*, 1983), which results in a high-current mode that interferes with normal circuit operation. This effect does not involve an SCR structure. Snapback can be initiated by current injected into a p-well due to avalanching junctions or result from ionizing radiation. Investigators have measured snapback-sustaining voltages significantly lower than the drain-substrate avalanche voltage. This effect therefore imposes a maximum operating voltage constraint on susceptible ICs (Ochoa *et al.*, 1983). Snapback is a three-layer effect, where drain avalanche current is sustained by minority-carrier injection from the source of an NMOS device. Figure 3-54 shows typical snapback characteristics and a proposed lumped-parameter model. Unlike latchup, there is no positive feedback loop, so snapback can be terminated by normal cycling, for instance, when the transistor output goes to zero. Because of the mechanisms involved, latchup prevention techniques that degrade the $\beta_{\text{pnp}} \times \beta_{\text{nnp}}$ product by irradiation have little effect on the snapback threshold drain voltage.

3.8.3.2 Second Breakdown

Another mechanism that can cause latchup in diodes, bipolar and MOS transistors, and especially in integrated circuits, is second breakdown (Schafft, 1967; Sze, 1981; Sze and Gibbons, 1966). Second breakdown can sometimes be induced at low current levels without damage to the junction. The usual result of second breakdown is, of course, permanent junction damage (Sunshine and Lampert, 1972). Because ionizing



(a) I-V Characteristics



(b) Lumped Parameter Model

Figure 3-54 (a, b). The snapback phenomenon: I-V characteristics and a Lumped-parameter representation (Ochoa *et al.*, 1983).

pulses can trigger this action, latchup can ensue. Second breakdown is similar to SCR action in that once it is initiated, *i.e.*, the ON state is reached, it is sustained until the latchup current is reduced below the threshold, as shown in Figure 3-55. Dielectric isolation does not guarantee a latchup-free system in this case, although the substrate plays no role as it does in the four-layer pnpn switch. Bipolar collector-base junctions and reverse-biased diodes are susceptible if they have a second-breakdown characteristic by virtue of their construction. Diffused passive components, such as resistors, are also susceptible if the junction region isolation for the resistor possesses a second-breakdown characteristic.

Second breakdown is manifested by a sudden drop in the bipolar transistor voltage V_{CE} with an almost simultaneous surge in collector current. This phenomenon limits high-power transistor operation to a specific safe operating area (SOA) of its characteristic curves, as seen in Figure 3-56. Chronologically, this instability occurs at the breakdown voltage at which the collector current equals I_C in Figure 3-57, immediately followed by a sudden drop to a low-voltage regions at the end of the dotted lines in Figure 3-57. The final stage is imminent when I_C grows to cause device destruction. Associated with second breakdown are the final values of collector current, which result in the formation of a hot spot and production of a localized microplasma in the

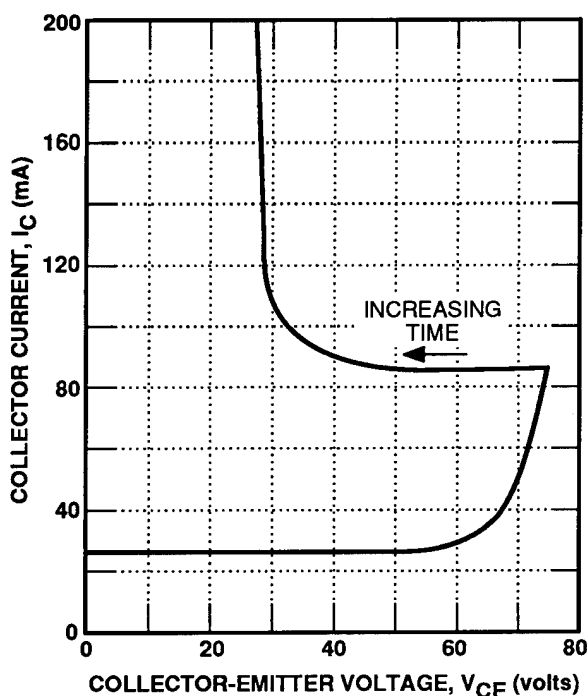


Figure 3-55. Typical second-breakdown characteristic (Messenger and Ash, 1992).

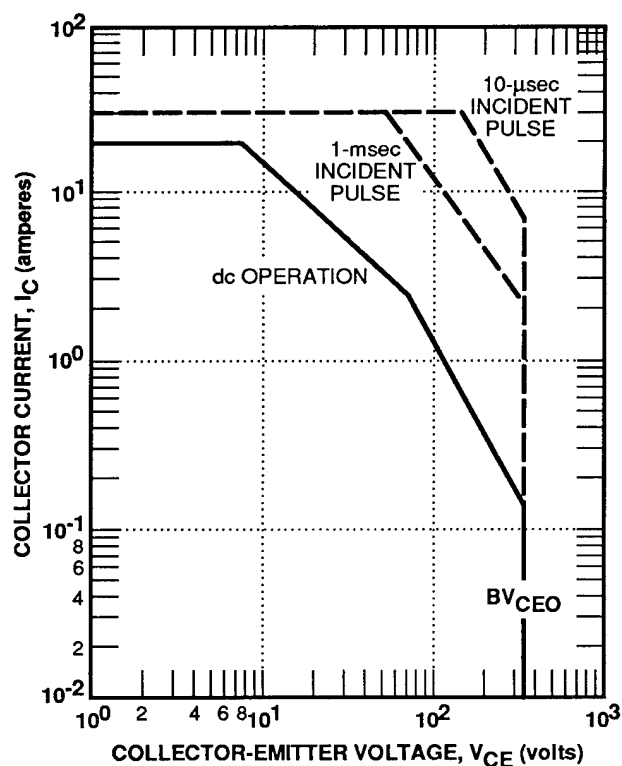


Figure 3-56. Safe operating area bounds for silicon transistors for peak junction temperature at 150°C (Sze, 1981).

device, short-circuiting the junction (Ward, 1976). Reverse-bias second breakdown can be caused by an inductive load suddenly forcing a large negative polarity current through the device, resulting in a high transient breakdown reverse bias at the junction. This also causes a plasma formation and pinhole shorts at the junction.

3.8.4 Latchup Windows

Even though an IC experiences latchup in response to an experimental dose-rate level, it may operate normally at a higher dose-rate level and then latch up at a third, yet higher level. A dose-rate region of latchup-free behavior between two regions of possible latchup is called a latchup window (Azarewicz and Hardwick, 1982). Such windows can cause problems in hardness assurance because they make identification of latchup-immune ICs more uncertain. Several mechanisms have been hypothesized to explain these windows, but the responsible mechanism has not yet been unambiguously determined. A mechanism suggested by Coppage *et al.* (1983) proposes that over some range of dose rates, competing photocurrents from transmission gates elsewhere in the device can cancel the injection current to the pnpn structure. They attribute the windowing effect to the complex

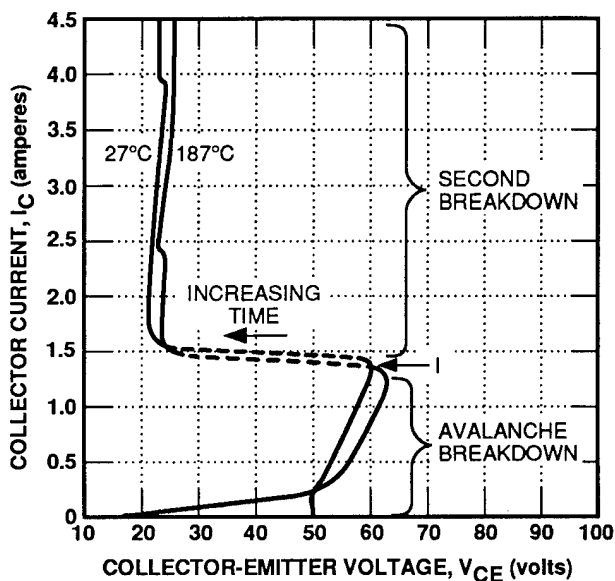


Figure 3-57. Collector current versus collector-emitter voltage under second breakdown (Schafft, 1967).

injection-level dependencies of spatial charge distributions within CMOS ICs. More recently, researchers have proposed that the window results from distributed effects such as lateral substrate currents and distributed resistances, which are not monotonic functions of dose rate in some structures (Johnston and Baze, 1987).

3.8.5 Latchup Mitigation

There are two fundamental strategies for avoiding latchup (Troutman, 1986):

1. Keeping the parasitic pnpn structure in the blocking state,
2. Preventing the parasitic pnpn structure from reaching the latched state.

These two strategies initially may appear similar, but very important distinctions exist. The first strategy is implemented by making the *switching point* inaccessible to any static or dynamic operating point. Usually, this means designing the switching current to be larger than the maximum supplyable current.

The second strategy is implemented by making the *holding point* inaccessible to any static or dynamic operating point. This means either designing the holding voltage larger than the power-supply voltage (plus a safety margin) or designing the holding current larger than the maximum supplyable current. However, in the second case, transient SCR behavior can result if device current exceeds the switching current. Behavior of a circuit containing a parasitic pnpn structure can be unpredictable once the pnpn is triggered into the negative differential resistance region. The safest approach is to avoid entering the negative differential region, even momentarily, which is guaranteed by the first strategy. Avoiding the negative differential region may be accomplished by designing a large enough holding voltage using the second strategy; however, a sufficiently large holding voltage is difficult to design directly for all parasitic pnpn structures encountered in CMOS chip designs because holding voltage is not well modeled. Finally, it should be noted that any of the guidelines that are implemented to raise switching current auto-

matically raise holding current for the same structure. Thus, Strategy 1 prevents any pnpn switching, even transient. It is also easier to implement since the switching edge of the blocking state is precisely defined, with no fitting parameters required.

Techniques to implement these strategies divide into two areas: namely, layout guidelines and process design. The first is germane to any CMOS technology and is of interest to the device and circuit designer. The second relates to the process features incorporated into a CMOS technology by the process engineer.

For bulk technology devices, guard structures are the most effective tool available to the circuit designer. A minority-carrier guard is used to pre-collect minority carriers injected into the substrate before they reach a well comprising the base of a vertical bipolar. It consists of a reverse-biased pn junction formed by a source/drain or well diffusion. It is more effective on epi-CMOS because of the reflecting boundary at the high-low junction and because of increased recombination in the highly doped substrate.

A majority-carrier guard is used to reduce well or substrate sheet resistance locally, thus minimizing any ohmic drop from parasitic collector current. It consists of a source/drain diffusion of the same type as the background. Operation of a majority guard in the well is also enhanced on epi-CMOS because the elimination of substrate minority-carrier collection at the bottom well junction means that majority carriers in the well appear only at its periphery, where they are more easily shunted away from parasitic emitters.

Multiple well contacts augment the low-bypass resistance effected by majority guards in the well. Some combination of the two should also be used on I/O circuits to ensure the parasitic vertical bipolar is not turned ON by I/O over- and undershoots. In addition to avoiding latchup, the goal here is to prevent large current spikes in these high-gain devices, which otherwise would waste power.

A substrate contact ring should be mandatory for all chips. It minimizes lateral bypass resis-

tance by distributing substrate majority carriers. On epi-CMOS, the contact ring can reduce lateral bypass resistance to below 1 ohm.

The second area in which much work has been done to avoid latchup is process design, for which there are two approaches: bipolar spoiling and bipolar decoupling. Early spoiling techniques attempted to reduce base minority-carrier lifetime with either gold doping or neutron irradiation, but this has led to adverse device effects such as high leakage current. Later, internal gettering was introduced to lower lifetime in the substrate below the denuded zone, but this has little effect on parasitic lateral bipolars with small base width. A retrograde doping profile in the well helps prevent latchup by reducing vertical transport, but care must be taken to remove injected carriers so that lateral transistor action to the well edge is not enhanced.

Bipolar decoupling has proved more effective and easier to implement than bipolar spoiling. Several methods are possible. A highly doped substrate beneath a lightly doped epitaxial layer shunts the lateral parasitic bipolar very effectively. As discussed above, this combination also improves the efficacy of minority guards in the substrate and majority guards in the well. A retrograde well can also be used to reduce the well's sheet resistance, although this is usually not as effective as the inclusion of majority-carrier guards in the well. Reverse bias on the substrate (or well) raises the bypass current needed to turn on the corresponding bipolar, but using ON-chip generators to provide this bias necessitates careful guard design to eliminate charge injected by the generator. Trench isolation eliminates lateral current flow to and from the well and conceivably could allow a lithographically limited n^+/p^+ spacing. Present side-wall inversion problems must be resolved before diffusions can be butted against trench walls, however.

Bipolar decoupling provides a simple design procedure for avoiding latchup:

1. Decouple the vertical parasitic bipolar using epi-CMOS with a substrate contact ring to minimize lateral bypass resistance,

2. Decouple the lateral parasitic bipolar using majority-carrier guards in the well or minority-carrier guards in the substrate.

Additionally, the use of an insulating substrate technology (*e.g.*, SOS or SOI) that isolates the complementary devices provides an effective method for eliminating latchup.

3.9 Transient Radiation Effects on Electro-Optical and Passive Components

The effects of transient ionizing radiation on a variety of electro-optical devices and components (*e.g.*, fiber optic cables, detectors, etc.) and various passive electronic components (*e.g.*, resistors and capacitors) are discussed below.

3.9.1 Electro-Optical Components

For many fiber-optic systems, one of the most stringent requirements is the high-dose-rate, transient dose requirement. While forward-biased lasers and light-emitting diodes (LEDs) are essentially immune to high-dose-rate effects, photodiodes, fibers, some connectors, and possibly optoelectronic integrated circuits (OEICs) are all susceptible to high-dose-rate effects, which can significantly degrade system performance. In many doped core fibers, a large transient pulse of ionizing radiation can cause serious temporary darkening of the fiber that lasts well beyond the time when the system should be back on line and functioning [see Figures 3-58 and 3-59]. For applications that require a long fiber (>50 meters) and fiber-optic links that "operate through" a relatively high-dose-rate pulse ($>10^{10}$ rads[Si]/sec), the fiber must be chosen with great care. If, as in the case of a missile or tethered weapon application where the projected lifetime is short and, as a consequence, the cumulative ionizing radiation dose is not particularly large but the dose rate is high, then the addition of phosphorus to the fiber core will reduce the transient attenuation. While pure silica core fibers are available that can withstand considerably higher dose-rate pulses, additional technology development remains to be done in this area, especially for those applications that require specialized fibers, such

as the polarization maintaining single-mode fiber in a fiber-optic rotation sensor (FORS).

3.9.1.1 Optical Fibers

The transient attenuation of the light intensity transmitted through an optical fiber caused by a pulse of ionizing radiation can be larger, and potentially more of a problem, than the permanent attenuation caused by ionizing radiation

dose effects. Figure 3-60 illustrates that the signal level increases as a result of luminescence during the radiation pulse and reaches a minimum at the end of the pulse because of induced absorption.

Unlike transient luminescence, which exhibits prompt decay and can be filtered out because it is in the ultraviolet (UV) range, transient attenua-

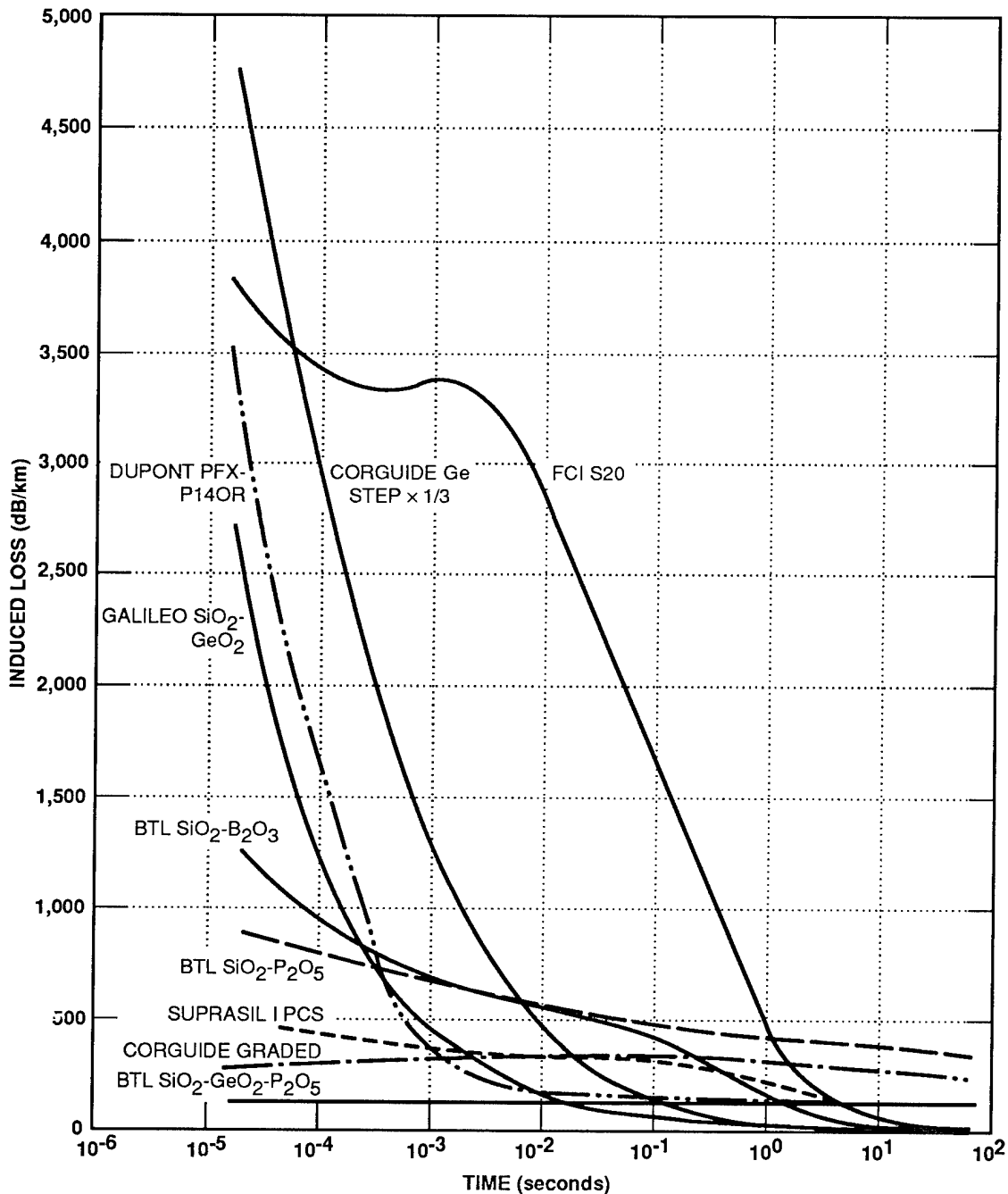


Figure 3-58. Transient attenuation in a variety of fibers (Fribele, Gingerich, and Sigel, 1978).

tion can last much longer than the ionizing pulse. As in the case of permanent effects, the degree of transient attenuation depends strongly on the characteristics of the core of the fiber. Although there is considerable variation among both pure and doped core fibers, generally the pure core fibers exhibit significantly less transient attenuation. Representative transient attenuation data are shown in Figure 3-58 for a variety of fibers operating at $0.8 \mu\text{m}$ after a prompt dose of approxi-

mately 3 krad. Note that the Gedoped Corguide fiber has the largest attenuation. Again, as in the case of permanent effects, phosphorus and boron have relatively unique effects on transient attenuation. While these dopants increase permanent attenuation, as can be seen at long times in Figure 3-58, they have the opposite effect on transient attenuation in that they tend to eliminate or minimize the attenuation observed shortly

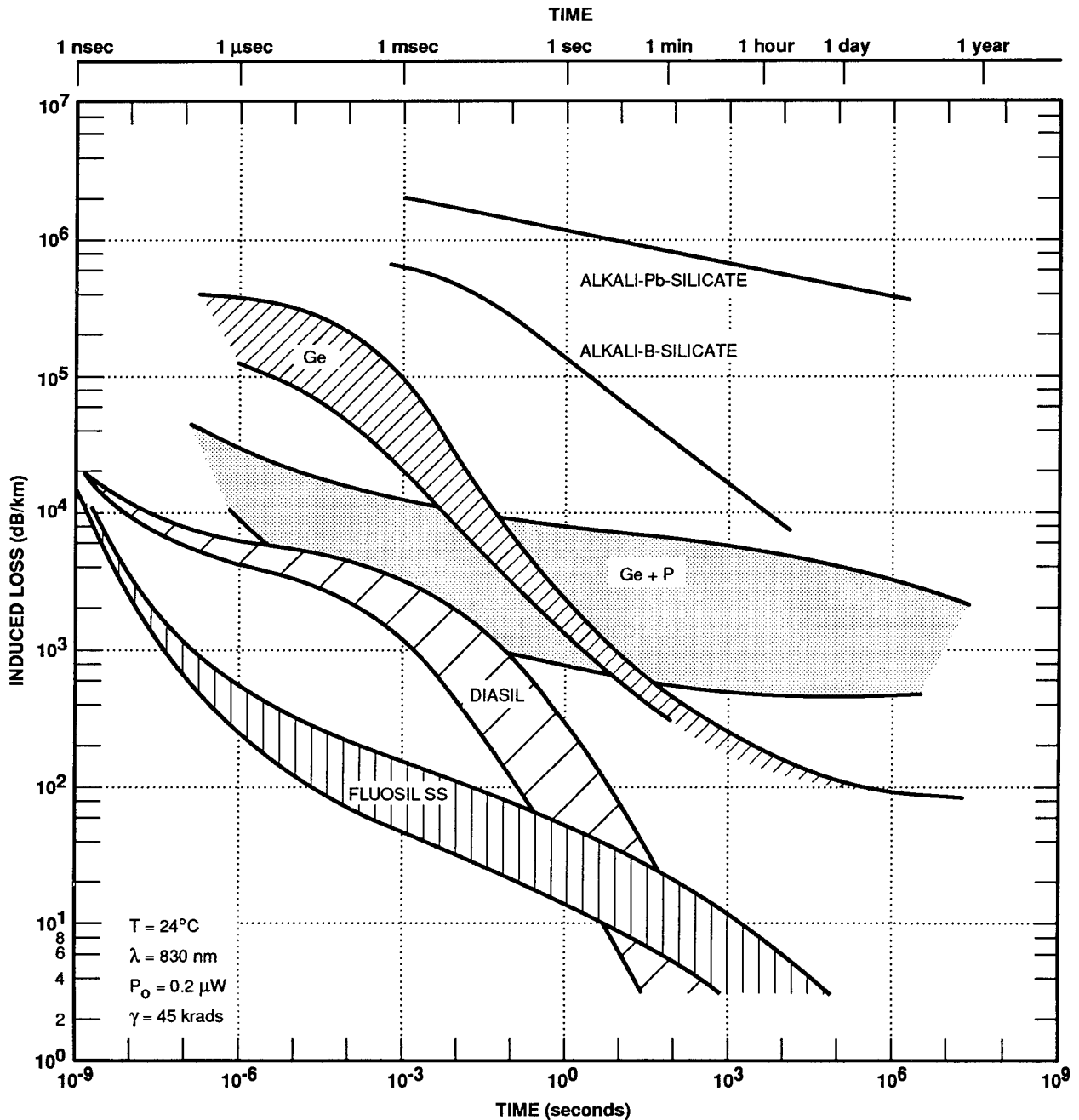


Figure 3-59. Radiation sensitivity of fibers (Schneider *et al.*, 1987).

after the pulse. Note also that the pure-core Suprasil fiber has low transient attenuation.

Transient attenuation data from more recent work are shown in Figure 3-59 for a variety of fibers operating at 830 nm at room temperature. To obtain the results in Figure 3-59, a dose of 45 krads was delivered with each pulse, which, for a typical FXR or LINAC pulse, corresponds to a dose rate of about 1×10^{12} rads/sec. With the exception of the alkali glasses, the Gedoped core fibers exhibit the most intense transient attenuation, and the addition of phosphorus (P) reduces the transient effect but enhances the permanent damage. The Diasil and Fluosil fibers are pure core fibers. It comes as no surprise, given the complexity of the various color-center growth and anneal processes that can take place, that the recovery curves have a variety of shapes.

In order to summarize other important features of ionizing radiation-induced transient attenuation in fibers, Figures 3-61 and 3-62 display data for high-OH and low-OH fibers, respectively. These results are for the exposure of pure core

fibers to a dose rate of approximately 1×10^{11} rads/sec. This exposure also results in an ionizing radiation dose of 3.5 krads. As for the case of permanent attenuation, the high-OH fibers perform better across all the variables shown in the figures, with an improvement of roughly a factor of 10 reduction in transient attenuation. The other important trends revealed by these results are about the same for both high- and low-OH fibers, as follows:

1. The recovery of the transient attenuation is slower at lower temperature,
2. The transient attenuation is less at 1,300 nm than at 830 nm, which is in agreement with permanent attenuation results,
3. Transient attenuation is also susceptible to photobleaching-induced recovery [note the varying power levels P_0 in Figures 3-61 and 3-62], except that photobleaching is not very effective at less than about 1 msec after exposure.

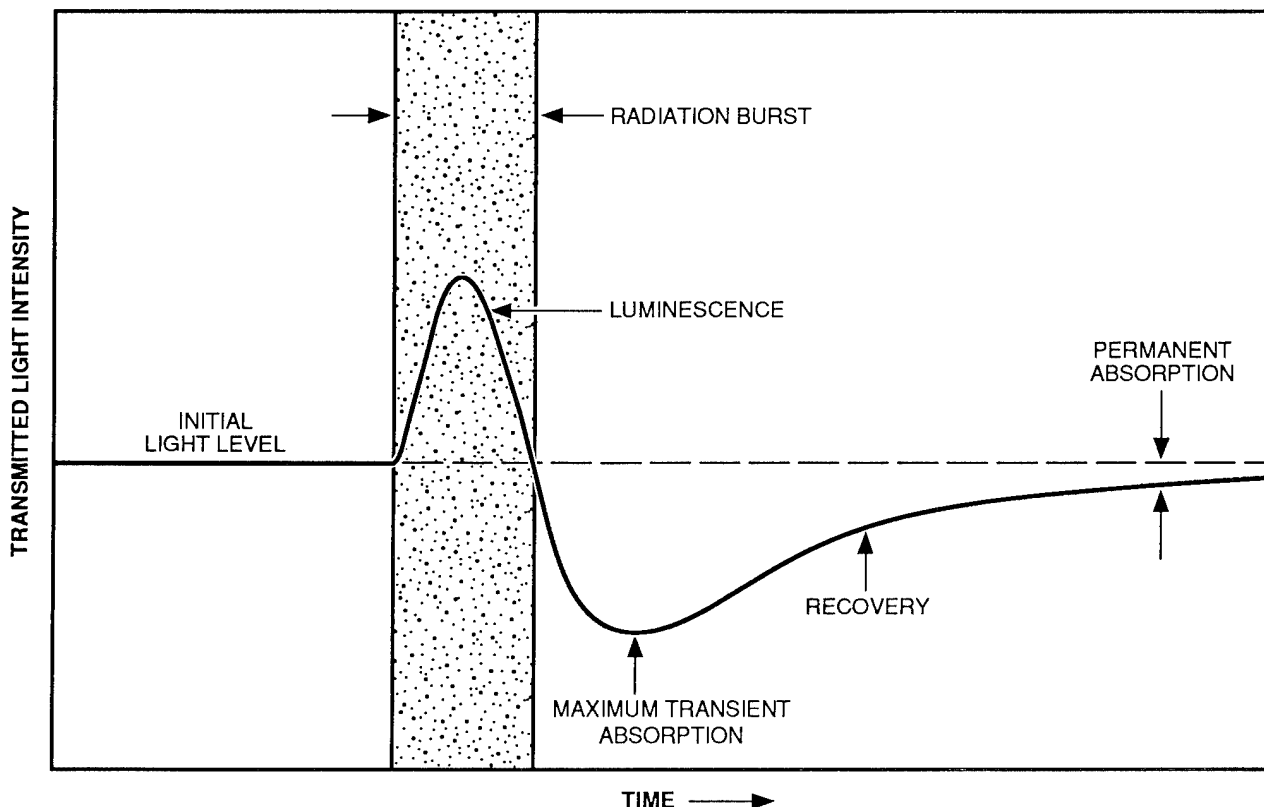


Figure 3-60. Transient ionization effects in fibers (Sigel and Evans, 1974).

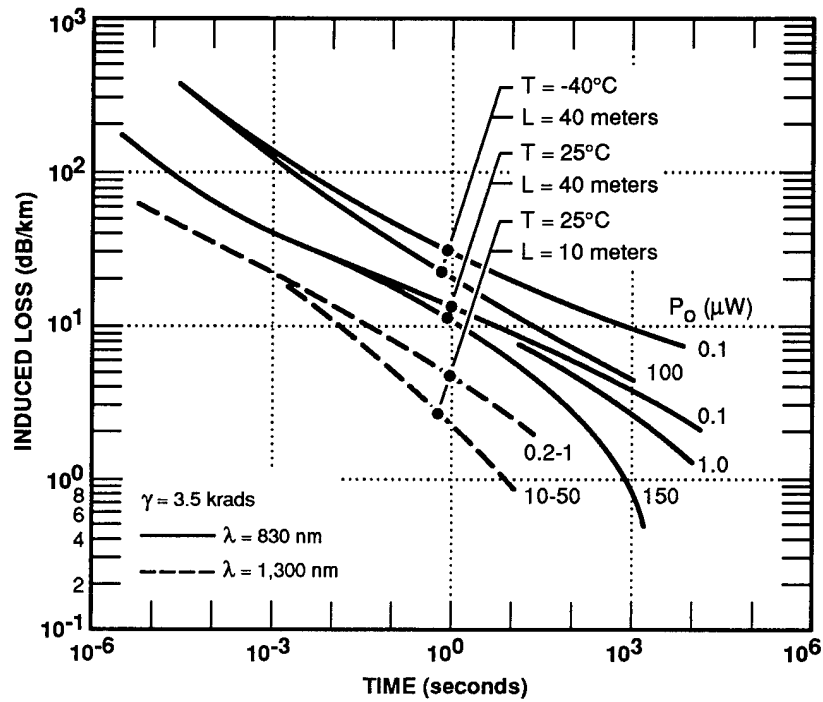


Figure 3-61. Parameter effects on attenuation in a high-OH fiber (Schneider *et al.*, 1987).

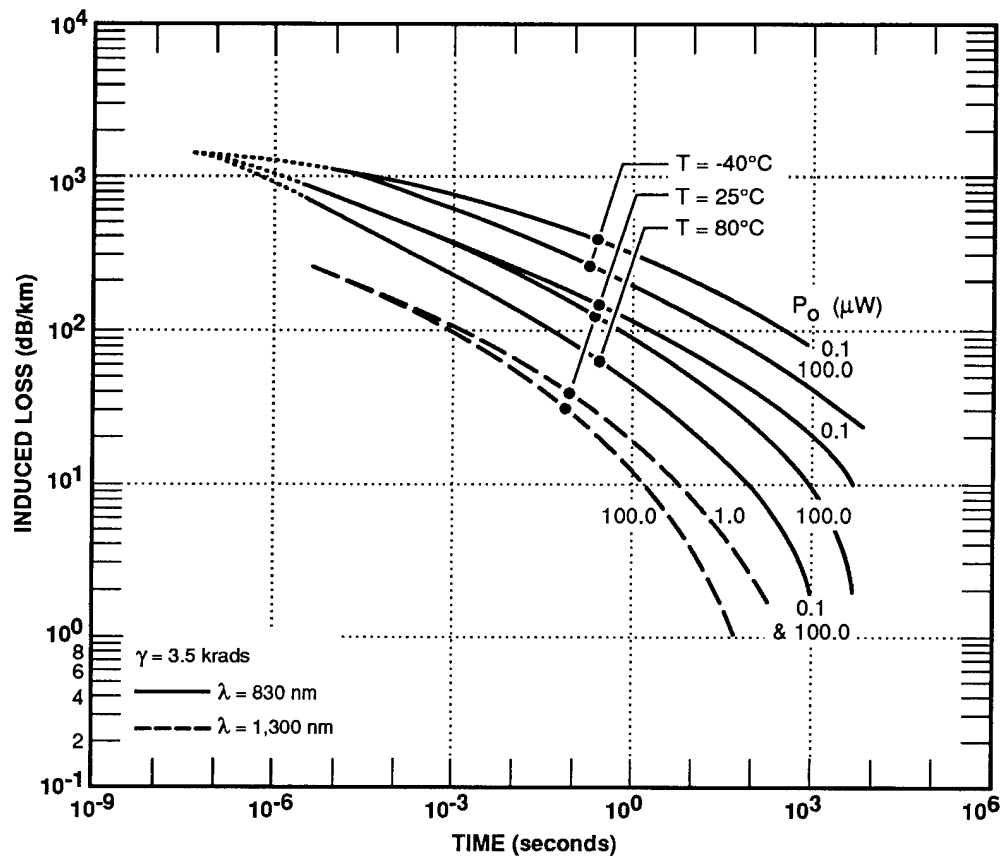


Figure 3-62. Parameter effects on attenuation in a low-OH fiber (Schneider *et al.*, 1987).

3.9.1.2 Electro-Optical Devices

The sensitivity of electro-optical devices to prompt gamma radiation depends on the device type. Photodiodes and phototransistors are very sensitive to radiation. Both types of detectors have long minority-carrier lifetimes and large volumes for efficient collection of light-generated carriers, which causes the devices to generate and collect large prompt gamma-induced photocurrents. Photocurrent in the phototransistor is amplified by the gain of the device, which causes the phototransistor to be more sensitive to radiation than a photodiode. Intense transient ionizing pulses can also cause significant transient currents in silicon PIN photodiodes. Dose rates of about 10^9 rads(Si)/sec are typically large enough to produce saturated transient pulses from a silicon PIN photodiode detector. However, III-V detectors have been shown to discriminate between optical signals and ionization pulses of 1×10^9 rads(Si)sec magnitude with little or no optimization or circuit compensation.

LEDs have shorter minority-carrier lifetimes and smaller volumes than photodiodes. Their photocurrents, therefore, are much smaller than the photocurrents produced by the photodiodes. LEDs will emit light for the duration of the photocurrent pulse. Laser diodes are even less sensitive than LEDs since most laser diodes are GaAs and have higher electron mobility, larger bandgap, and smaller geometry than silicon LEDs.

The photocurrent response of an optical coupler depends on the type of components contained in the device; the most sensitive couplers can upset around 1×10^6 rads(Si)/sec. Optical couplers, which have LEDs and photodetectors such as photodiodes or phototransistors, will have responses similar to those described above. Devices with laser diodes and small-geometry detectors have the highest upset threshold. If an amplifier or gating logic is incorporated into the output of/the coupler, the response will also depend on the transients in these components. The recovery time may be fairly slow if a linear IC is used in the coupler circuitry.

High-dose-rate effects in simple LiNbO_3 OEICs have also been observed, but only at very high rates, of the order of 1×10^{13} rads(Si)/sec, using electron pulses. Temporary reduction in transmitted signal and coupling between waveguides can last well beyond the radiation pulse.

3.9.2 Passive Components

3.9.2.1 Resistors

Radiation effects in resistors are generally small compared to effects in semiconductors and capacitors. Transient effects are generally caused by photons interacting with the resistive medium and its encapsulation to generate electrons and ions. If there is a net charge produced in a resistor by photon interactions, a current may be induced in the resistor in order to replace the charge removed or added by the incident radiation. This current is referred to as the replacement current.

Pulsed ionizing radiation on discrete resistors: (1) temporarily changes the effective resistance of the component, and (2) induces a current pulse in the component as a result of emission and absorption of secondary electrons. For many resistors, ionization causes increased conductivity in the bulk resistance, insulating materials, and surrounding medium, so the effective resistance decreases. In some cases, however, test results show that for some resistors, the effective resistance increases during the exposure because of injected replacement currents. These effects can be described in forms of a current source $I_R(t)$, which is the replacement current, and a shunt resistance R_S , which represents the leakage currents in the resistor and its surrounding material. The magnitudes of both depend on the dose rate, surrounding medium, resistance material, and applied voltage.

Table 3-1 shows shunt resistance values and peak values of injected replacement currents for various types of resistors at an exposure rate of 4×10^7 rads(Si)/sec. Equivalent shunt resistance is higher for solid construction than for air-core resistors. For wire-wound and solid-carbon resis-

Table 3-1. Transient effects on resistors (Steel *et al.*, 1964).

Resistor Type	Radiation-Induced Shunt Resistance, R_S (M Ω)	Peak Injected Current, I_R (μ A)
Carbon film (air core)	≥ 0.4 to 0.6	45
Metal Film (air core)	2 to 4	18
Carbon composition (air core)	2.6 to 6	29
Solid	10 to 110	27
Metal film (solid)	9 to 100	24
Carbon film (solid)	a	32
Wire-wound Solid	a	28
Wire-wound Air core	a	28
Wire-wound Air core	a	42

Note: ^aWire-wound resistor increase 0.1 to 0.5 percent; carbon film increases 0.5 to about 5 percent. Effective resistance showed increase rather than decrease [see related text].

tors, an effective increase is shown, which is an exception to the general rule that ionization effects decrease resistance. All the resistors emit a net number of electrons, resulting in a net injected current. The magnitude of the injected current generally increases with the increased physical size. In most practical applications, the current is small and may be neglected.

Figure 3-63 shows the shunt conductance G_S as a function of exposure rate for various resistor types of 1-M Ω nominal value. These data were obtained with external air leakage across the component essentially eliminated (Steele *et al.*, 1964). Resistors for which this is not done can be expected to have larger radiation effects.

On the basis of the curves given in Figure 3-63, the shunt resistance is (Steele *et al.*, 1964)

$$R_S = \frac{1/K}{\dot{\gamma}^\Delta}, \tag{3.43}$$

where Δ is the slope of the appropriate line, $1/K$ is a constant determined from the figure, and $\dot{\gamma}$ is the exposure rate.

First-order approximations for the shunt resistance and the replacement current as functions of the exposure rate are

$$R_S = A/\dot{\gamma}, \tag{3.44}$$

and

$$I_R = \beta \dot{\gamma}, \tag{3.45}$$

where A is a constant having the dimensions Ω -rad(C)/sec, and β is a constant having the dimensions A/rad(C)/sec. The proportionality constants vary with the wattage and potting material of the resistor.

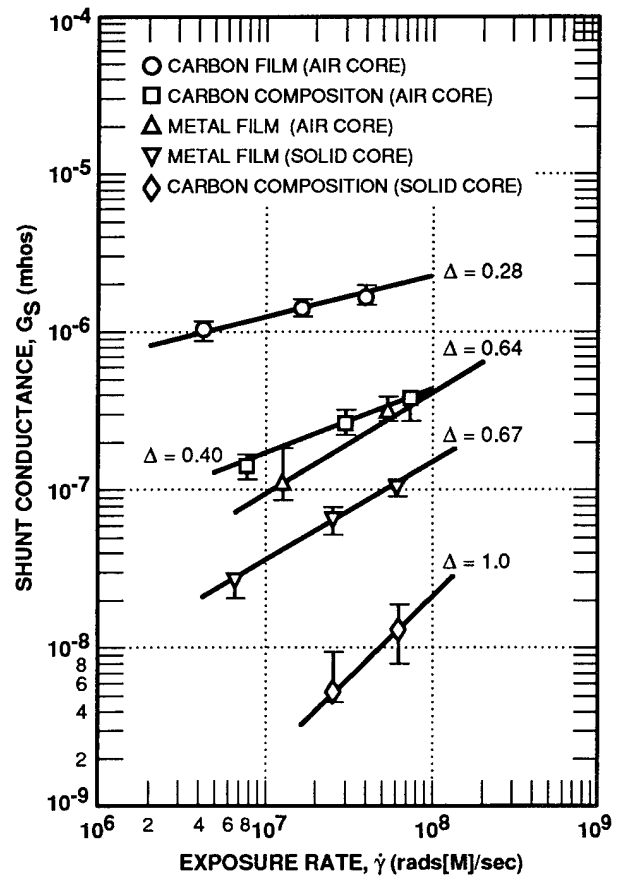


Figure 3-63. Resistor exposure-rate dependence; external air ionization not included (Perkins and Bailey, 1964).

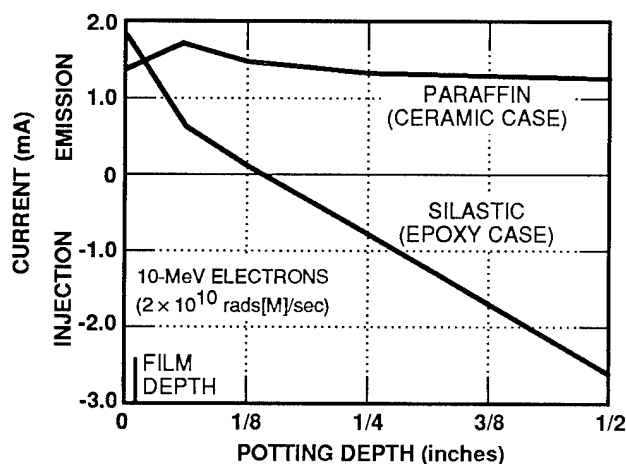


Figure 3-64. Effects of potting depth on current injection for carbon composition resistors with epoxy and ceramic cases (Perkins and Bailey, 1964).

Potting reduces ionization and improves the performance of a resistor and is indicated if stable values $>10 \text{ k}\Omega$ must be preserved during irradiation; conformal coating suffices for lower values. Spraying and dipping of resistors may be insufficient to significantly reduce leakage. The effect of the shunting resistance R_S can be appreciable for unpotted $\text{M}\Omega$ resistors at 10^6 to 10^7 rads/sec.

The potting thickness may be important in determining the replacement current in some cases. Replacement currents as a function of potting thickness are shown in Figure 3-64. There is little variation in emission current with paraffin thickness. However, the high-electron-density Silastic causes net electron injection to occur at potting-depth thicknesses greater than approximately 1/8 inch. This curve indicates there may be an optimum potting depth in some cases.

The effect of the replacement current can be reduced by the "virtual ground" technique wherever the circuit permits its application. A variable resistor is connected in parallel with the exposed resistor and balanced so that a virtual ground lies at the electrical center of the irradiated specimen.

Figure 3-65 shows current injection for a resistor versus voltage. The curve is linear with a change in slope at negative voltages sufficient to

prevent the collection (injection) of low-energy ($<50 \text{ eV}$) scattered electrons (Perkins and Bailey, 1964).

3.9.2.2 Capacitors

The main effect of pulsed ionizing radiation on capacitors is a temporary increase in the conductivity of the capacitor's dielectric material. The conductivity increases promptly during the initial part of the radiation pulse, but decays at a slower rate than the radiation pulse. The radiation-induced current and changes to the voltage in the capacitor are illustrated in Figure 3-66. The prompt conductivity produced in various types of capacitor dielectric materials over a range of dose rates is shown in Figure 3-67. If the conductivity level for a capacitor is sufficient to be of concern in a circuit, the time waveform of the conductivity can be estimated analytically. Capacitors are generally not a problem because semiconductor photocurrents usually dominate the response of the circuit.

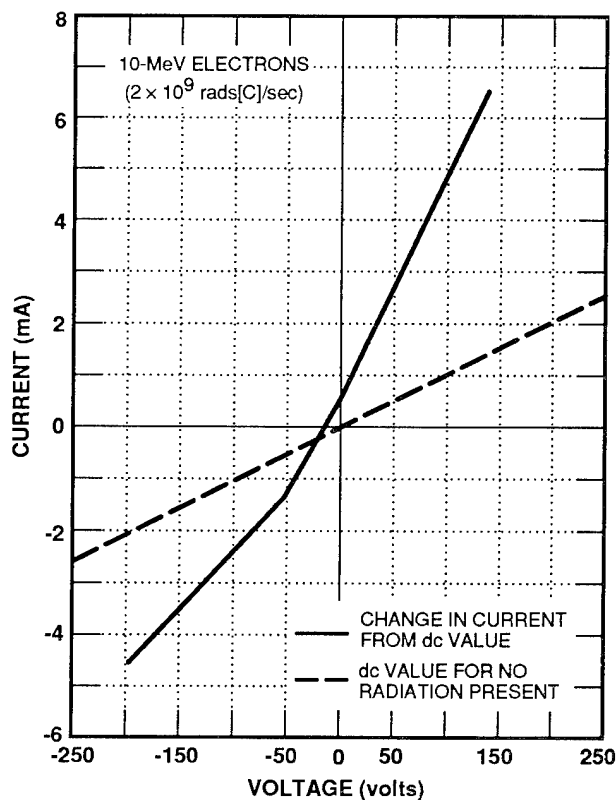


Figure 3-65. Effects of applied voltage on current injection for a 100-kW 1-watt carbon composition resistor in 1/2-inch Silastic (Boeing, 1964).

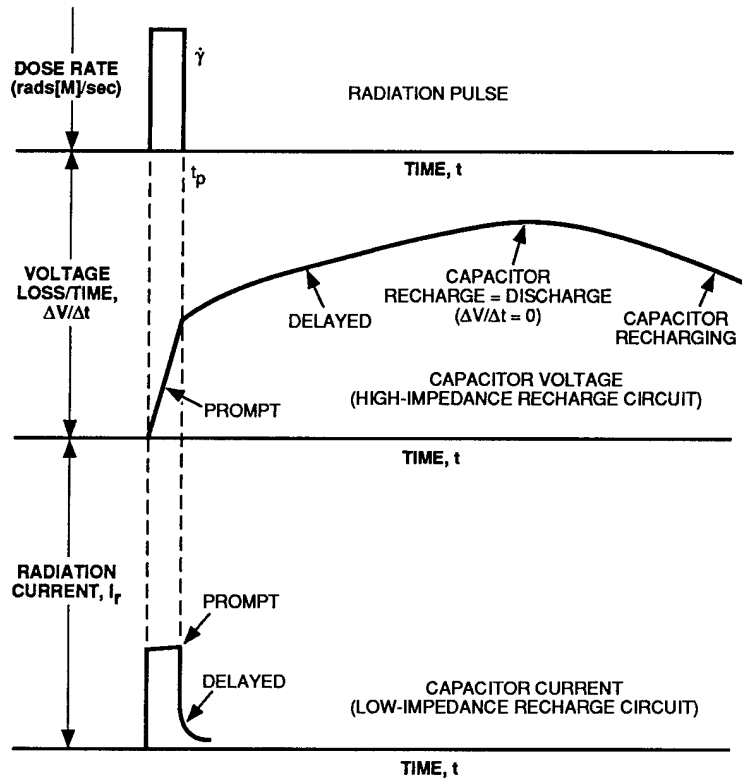


Figure 3-66. Capacitor photoconductivity characteristics [combined recharging and discharging effects result in a composite voltage loss/time curve that later becomes a decreasing exponential] (Thatcher and Green, 1972).

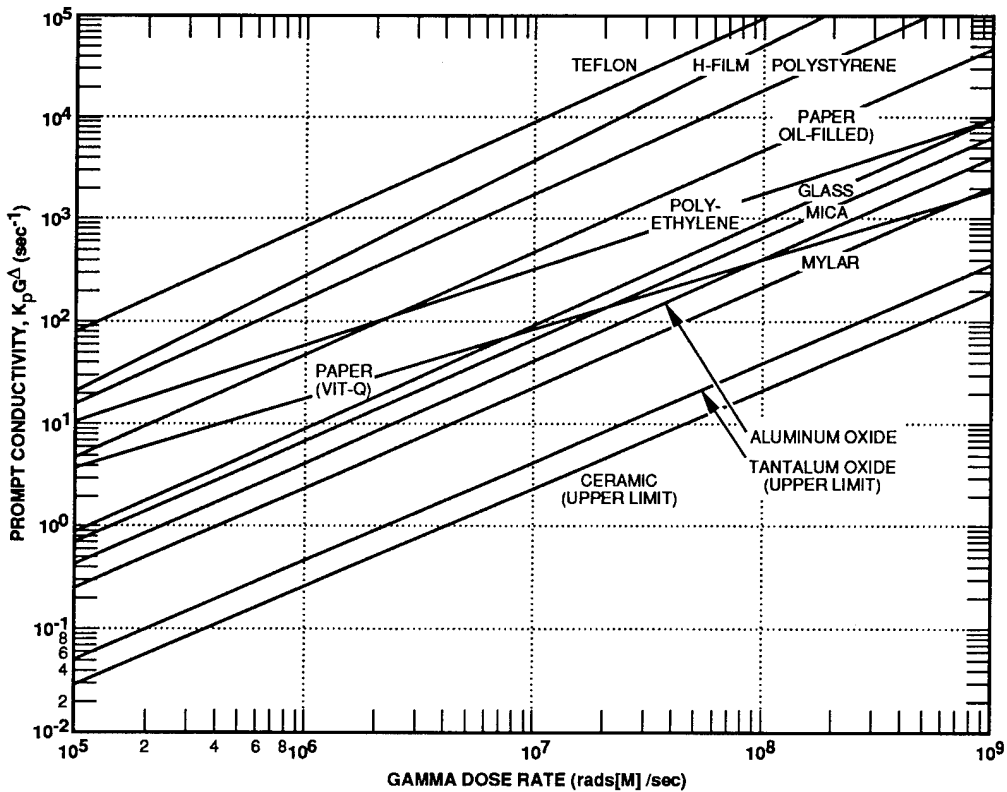


Figure 3-67. Prompt conductivity versus gamma dose rate (Thatcher and Kalinowski, 1969).

A capacitor exposed to a pulse of ionizing radiation will exhibit a transient discharge due to an increase in the shunt conductors of the dielectric. It is convenient to represent the capacitor in terms of the equivalent circuit shown in Figure 3-68 when using capacitor transient radiation effects data to predict the behavior of irradiated circuits. In this representation, the total resistance R_T is given by

$$\frac{1}{R_T} = \frac{1}{R_S} + \frac{1}{R_o} \quad (3.46)$$

where

$1/R_o$ = pre-irradiation leakage
conductance = $s_o C / \epsilon \epsilon_o$

$1/R_S$ = radiation-induced leakage
conductance = $(s - s_o) C / \epsilon \epsilon_o$

s_o = initial conductivity

C = capacitance

ϵ = dielectric constant

ϵ_o = dielectric constant of free space

s = conductivity.

At high exposure rates, $R_T = R_S$ for all practical purposes.

In applications to circuit design, each capacitor should be represented by its equivalent circuit [Figure 3-68]. The conductivity during a specified high-rate radiation pulse is computed using the appropriate characteristic parameters, and the effective leakage resistance is determined from $R_T = \epsilon \epsilon_o / \sigma C$. Using this value for the leakage

resistances of the capacitors, the behavior of the circuit can be determined. Except where the radiation pulse is a simple function of time, the equations governing the circuit behavior may be quite complicated. It is recommended that the possibility of using approximations to the radiation pulse be investigated before an exact solution is attempted.

The voltage remaining on a capacitor immediately after a radiation pulse may be calculated from a rule of thumb to obtain design information. Equation 3.47 [below] is applicable for this purpose when the radiation pulse duration is short compared to the recharging time constant of the circuit:

$$V = V_o e^{-t/R_T C} \quad (3.47)$$

where $R_T = \epsilon \epsilon_o / \sigma C$.

If the delayed components can be neglected during the pulse,

$$\sigma = F p \dot{\gamma} \quad (3.48)$$

and the average dose rate $\dot{\gamma}$ is given by

$$\dot{\gamma} = \gamma / t_p \quad (3.49)$$

where γ is the dose delivered in a pulse of t_p seconds at a dose rate $\dot{\gamma}$.

Combining Equations 3.44 through 3.49, the voltage at the end of the radiation pulse can be expressed as:

$$V = V_o e^{-[F p \gamma / \epsilon \epsilon_o]} \quad (3.50)$$

A more detailed approach is given in Cordwell (1968).

3.10 Single-Event Phenomena

Advances in memory technology have led to increased packaging densities while power consumption has been reduced. In general, this miniaturization trend has been beneficial to satellite and avionics technology, except that a new mode of device failure has accompanied device miniaturization. In the near-earth regions of space, high-energy particles are always present in the radiation belts and occur sporadically at high latitudes due to solar flares and the galactic flux. In

C = CAPACITANCE
 R_T = TOTAL LEAKAGE RESISTANCE

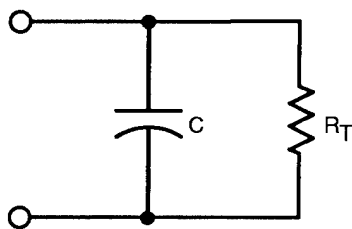


Figure 3-68. Capacitor equivalent circuit (Thatcher and Kalinowski, 1969).

such particle environments, microelectronic devices are susceptible to operational disturbances known as single-event phenomena (SEP), which pose a serious problem for silicon MOS and bipolar circuits and GaAs circuits. SEP disturbances can be divided into four basic categories: single-event upset (SEU), single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR).

Basically, an SEU is an upset to the information stored in memory devices, memory elements of integrated circuits, or the inability of a semiconductor device to interpret information due to a disturbance in processing electronics. By definition, an SEU is said to occur when a single, highly ionizing particle produces a track of dense ionization in a semiconductor material, which affects device operation through charge collection (Ward, 1986). Due to the transient, nonpermanent effect of an SEU, this type of disturbance is termed a "soft error." The other SEP effects (*i.e.*, SEL, SEB, and SEGR) are termed "hard errors."

The single-event upset of a computational system used in a spacecraft can result in a catastrophic mission failure. In addition to data-register errors, which are similar to soft errors in memory chips, a bit-flip in a microprocessor can lead to a runaway processor. The runaway processor can overwrite random access memory (RAM) before ending up in an idle loop or coming to a complete halt, with the result that system survival can be jeopardized.

Microcircuit pnpn latchup from transient ionization is a considerable problem for systems that are required to operate in the nuclear-threat environment. Latchup is a low-impedance state resulting in a high-current drive that persists until the voltage drops below a certain voltage level (generally accomplished by cycling device power) or until device damage occurs from overheating. SEL, latchup from heavy ions, has been observed in bulk CMOS devices and in epitaxial CMOS devices in which the epitaxial thickness has not been optimized for prevention of latchup.

SEB is catastrophic failure that occurs when an n-channel power MOSFET suffers a gate, drain-source, or source-drain short as a result of a heavy-ion-induced turn-on of a parasitic bipolar junction transistor inherent within the structure and results in regeneration or avalanche and thus burnout. Power bipolar junction transistors can undergo SEB in a similar manner. SEGR is a permanent destructive event that results when a penetrating heavy ion deposits sufficient energy to cause rupture of the gate dielectric and shorts from the gate through the channel. SEGR and SEB are termed hard errors due to their permanent nature.

Since high-energy cosmic rays can easily penetrate several inches of aluminum, shielding against SEP is impractical. Increasing levels of integration and device miniaturization have resulted in an increasing susceptibility of devices to soft errors, and this susceptibility has become a major concern to the military and aerospace communities. Hence, the system designer must be able to quantify the SEP susceptibility of the mission-required electronic components and develop safeguards to ensure mission success.

3.10.1 Historical Background

The first discussion of the concepts underlying SEU was offered in a paper by Wallmark and Marcus (1962). These authors predicted that when IC feature sizes became small enough, cosmic rays would start upsetting microcircuits due to the heavily ionized tracks and cosmic-ray-induced spallation reactions. They were so far ahead of their time, however, that the paper was entirely overlooked. The next important paper to be published was Binder, Smith, and Holman (1975), in which upsets in digital flip-flop circuits were reported to have been observed in certain space satellites. Partly because the number of upsets observed was small, their claim that the upsets were due to cosmic rays in the iron group was disputed by most radiation-effects specialists at the time. Their published paper was quite remarkable in that: (a) it identified cosmic rays in the iron group as the likely cause of the upsets, (b) it showed how to calculate the rate at which

cosmic-ray upsets could be expected to occur, and (c) their calculations were within a factor of two of the number of upsets that were actually observed. However, due to the aforementioned skepticism, this paper was also largely ignored.

In 1978, two research efforts were completed that awakened the radiation-effects community to the new phenomenon of "soft errors," as it was then called. The first was reported in a paper by Pickel and Blandford (1978). In this paper, a model was developed to predict the cosmic-ray bit-error rate in dynamic MOS RAMs. Specifically, this cosmic-ray interaction model was used to estimate the bit-error event rate in an operating satellite memory, which consisted of 24 NMOS RAMs, each with 4096 memory bits. The upsets were attributed to energetic cosmic rays in the iron and aluminum groups. In this paper, the number of upsets was large enough to be convincing, and it was this paper that particularly alerted the space and nuclear radiation effects community to the existence of this new and important radiation effect. The method used for calculating the number of upsets to be expected in a cosmic-ray environment was similar to that of Binder, Smith, and Holman (1975), but used more detailed models, both for the device geometry and the cosmic-ray environment. At this time, circuit upsets were typically referred to as soft errors or single-particle errors (for single cosmic-ray particles).

The second effort was not published until 1979 (May and Woods, 1979), in which it was determined that the upsets being observed at sea level in dynamic RAMs (DRAMs) were due to alpha particles emitted from trace amounts of uranium and thorium present in the packaging materials used in the fabrication of electronic devices; these upsets were creating a serious problem from the standpoint of device reliability. The experimental measurements were performed with polonium and americium alpha sources on 4k DRAMs and 16k CCDs. May and Woods introduced the concept of critical charge for upset and predicted that the soft-error problem would worsen as device feature sizes became ever smaller.

After hearing the Pickel and Blandford paper, and learning of the work of May and Woods, Guenzer, Wolicki, and Allas hypothesized that if alpha particles from uranium and thorium could upset circuits, then alpha particles from nuclear reactions induced by energetic neutrons and protons might also be able to produce such upsets (Guenzer, Wolicki, and Allas, 1979). In late 1978, measurements were made on 4k and 16k dynamic MOS RAMs, first in a 14-MeV neutron beam of a 75-MeV cyclotron at the Naval Research Laboratory, and then with 14-MeV neutrons from a deuterium-tritium generator. First upsets were observed at neutron fluences of $\sim 10^8$ n/cm². The discovery that DRAMs were vulnerable to such low neutron fluences was startling at the time because DRAMs are majority-carrier devices and were expected to be hard to neutron fluences three to four orders of magnitude larger than 10^8 n/cm². Fluences for first upset, by 32-MeV protons, were also about 10^8 protons/cm². These results were presented at the 1979 IEEE NSREC. This paper correctly identified neutron- and proton-induced nuclear reactions as the cause of the upsets; because more than one particle was involved (unlike the case of single cosmic-ray particles), this paper was entitled, "Single Event Upset of Dynamic RAMS By Neutrons and Protons." Thus, the term "single-event upsets" has taken its name from this paper.

Another important paper presented in 1979 reported the discovery of heavy-ion-induced latchup in SRAMs (Kolasinski *et al.*, 1979). These were the first upset experiments to be conducted with high-energy heavy ions from an accelerator and the first to observe cosmic-ray-induced latchup. Thus, it was demonstrated that the SEP events expected in space could be simulated in earthbound experiments.

As SEP were exhibited in greater numbers of employed space systems, the extent of the threat was realized and efforts to counter its effects began at ARPA and DNA. The recent evidence of high-altitude, atmospheric neutron-induced single-event upsets in avionics (Taber and Normand, 1993) clearly demonstrates the continuing need to study these effects and develop

protection techniques. Thus, although radiation-hardening techniques and methods of improving the SEP tolerance for systems are available, SEP hardening must be an essential part of the development process for all space and high-altitude avionics projects since the potential results of not doing so can be disastrous.

3.10.2 SEP Environments

Based on source of origin and the nature of the upset mechanism, the particles that cause SEP can be grouped into: cosmic-ray heavy ions, cosmic-ray protons, geomagnetic-field trapped protons, packaging-material heavy ions, and neutral particles. No satellite orbits can be considered radiation-free, and the fact that a satellite's radiation environment changes as a function of both location and time must be taken into account. Far-earth and geosynchronous orbits have environments similar to interplanetary space; the cosmic-ray heavy-ion flux is the main concern in this region. The earth's magnetic field shields near-earth orbits from the less energetic cosmic rays, and protons trapped along the magnetic field lines tend to dominate the SEP production at low-earth orbits. Centered approximately 2,500 km above the earth, the Van Allen belts consist mostly of protons, electrons, and other charged particles. Of particular significance for space radiation effects in electronics is the South Atlantic anomaly (SAA), a magnetic field depression over the coast of Brazil resulting in the dipping of the trapped-charge belts down to the earth's atmosphere. The SAA is the source of most of the trapped radiation received in low-earth orbits.

Theories of the origin of cosmic-ray particles indicate that they are thought to be inductively accelerated, comparable to the acceleration of particles in a betatron. Rotating planetary bodies have rotational magnetic fields that generate rotational electric fields. The magnitude of a star's magnetic field allows particles to gradually accelerate to enormous velocities while being held in closed paths. Once freed from the field, the lifetime of cosmic rays is 108 to 109 years because of the low density of interstellar matter.

Table 3-2 delineates the percentage of the streams of high-energy nuclei that isotropically bombard the earth. The earth's magnetic field tends to alter the trajectory of the bombarding particles and influences the environment that orbiting satellites encounter.

The cosmic-ray heavy ions often possess billions of electron volts (GeV) of kinetic energy. This large amount of energy allows the easy penetration of thick shielding by such ions. Figure 3-69 shows the typical mass distribution for heavy ions in the cosmic environment. Notice the peak at ^{56}Fe . Particularly important are the 100-MeV ^{56}Fe ions, with extremely high-energy deposition per unit of track length (known as linear energy transfer [LET]), of 27 MeV-cm²/mg. These ions represent the most highly ionizing particles encountered in the cosmic environment.

Additionally, the material used to make the chip and its package may contain naturally occurring heavy actinide material (uranium, thorium, and their daughters), which provide alpha particles that can ionize the circuit materials and cause SEP. Alpha particles emitted in the header package can be stopped from entering the chip by a simple passivation layer (a thin coating of polyimide varnish or silicon rubber) above the chip. However, alpha particles arising from actinide decay in the chip material itself cannot be similarly stopped. Another source of alpha particles is heavy-ion bombardment collision with the silicon nuclei of the chip material. A single alpha particle can produce about 3×10^6

Table 3-2. Composition of cosmic rays (Gover and Browning, 1987).

Nuclei Group	Charge (Z)	Flux Density (m ² -sr/sec)	Total Flux (percent)
Protons	1	1,300	92.90
Alpha particles	2	88	6.30
Light	3-5	1.9	0.13
Medium	6-9	5.6	0.40
Heavy	≥ 10	2.5	0.18
Superheavy	≥ 20	0.7	0.05

electron-hole pairs in silicon, which is sufficient charge to upset MOS VLSI memory arrays. In fact, actinide concentrations of only 1 ppm can cause SEP degradation (Messenger and Ash, 1992).

Trapped geomagnetic protons in the Van Allen belts and the SAA can provide enough energy to penetrate a device and indirectly cause SEP. About 1 proton in every 100,000 has energy >30 MeV and can thus undergo nuclear reactions with the device material nuclei, thereby producing energetic charged particles that cause SEP. Such reaction particles include alphas, carbon ions, and actual fission of the silicon nucleus (Messenger and Ash, 1992). Finally, neutral particles can induce SEP from neutron-induced nuclear recoils or as a result of neutral-particle-beam (NPB) weapons.

The basic mechanisms of ionization and the resultant circuit charge collection is common to heavy-ion-, proton-, and neutral-particle-induced SEP. Heavy ions produce charge through direct ionization as they transit the semiconductor material. Protons and neutral particles produce suf-

ficient electron-hole pairs to cause SEP through indirect ionization. When a particle such as a proton or neutron undergoes elastic or inelastic collision with a silicon atom, a nuclear recoil (Si, Al, Mg, etc.) occurs. The primary recoil atom can be accompanied by charged secondaries such as alpha particles and secondary protons, resulting in the passage of a highly ionizing primary recoil product and charged secondaries, which can cause a wake of electron-hole pairs that can result in SEP. The primary recoil nucleus results in far denser ionization tracks than are possible by direct proton ionization.

3.10.3 Basic Single-Event Phenomena Mechanisms

3.10.3.1 Upset Phenomenology

A highly ionizing particle, such as a 75-MeV heavy ion, that enters a semiconductor produces a track of very dense ionization. If this track passes through a critical node of an electronic device, its operation can be upset if sufficient charge is collected at the sensitive node. The upset process depends on the properties of the ionizing track, the density of the electron-hole pairs formed in its wake, the angle of track entrance, the proximity of sensitive nodes, and device structure and material properties. The charge-collection process and its time scales are essential in determining the extent of the SEP problem and the subsequent upset rates.

The ionization process results in charge separation and its subsequent collection within a device. To understand how this results in errors, consider the concept of device critical charge. The critical charge Q_c is the least amount of charge that a system recognizes as sufficient to represent a binary 1 or 0 at a particular storage node in a memory array. This problem is exacerbated when devices are scaled down because smaller feature size circuits generally result in critical nodes with smaller capacitance values. Because of scaling, more advanced memories have smaller critical charges (McLean, 1987). Figure 3-70 demonstrates that critical charge decreases with feature size without regard to device technology.

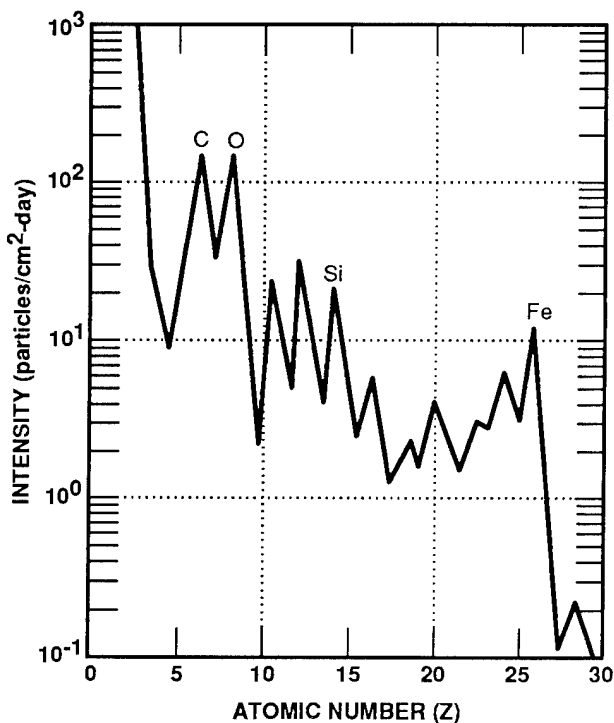


Figure 3-69. Composition of the heavy-ion cosmic-ray spectrum as a function of atomic number (Ma and Dressendorfer, 1989).

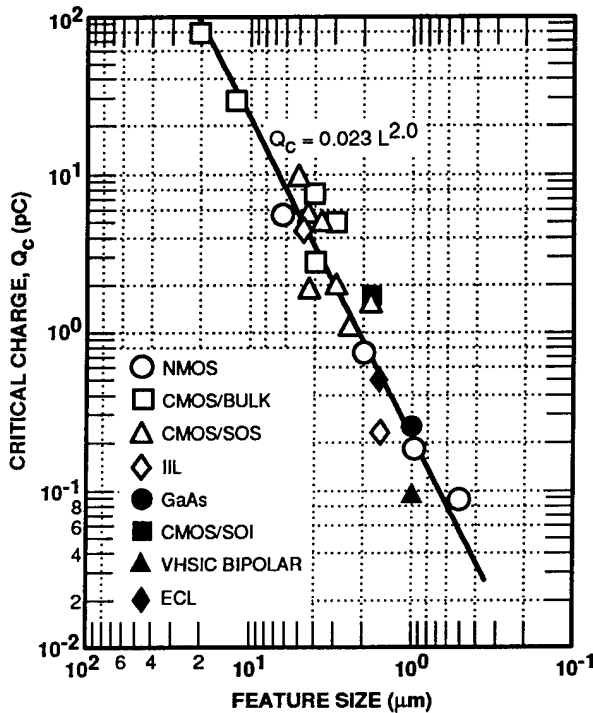


Figure 3-70. Critical charge necessary to cause upset decreases as feature-size decreases (Petersen and Marshall, 1988).

Figure 3-71 demonstrates the response of a diode junction field to heavy-ion penetration. As the ionizing particle begins its transit, it causes the formation of electron-hole pairs in its wake [Figure 3-71(a)]. The charge carriers diffuse and drift radially from the primary ionization track and dissipate energy by also ionizing the semiconductor material. If they are created in the depletion region surrounding a junction, the electron-hole pairs created by these secondary ionizations are rapidly separated and collected by a large internal electric field [Figure 3-71(b)]. Electrons or holes that are produced outside the depletion region can diffuse to the edge of the depletion region and be pulled into the node where logic information is stored, thus exacerbating the information-loss process.

The charge collected by drift has two components: (1) charge deposited in the depletion region, and (2) charge collected from beyond the depletion region by funneling. The funnel is an extension of the charge-collection region by an elongation of the electric field lines along the ion

track [Figure 3-71(c)]. This particle-induced funnel causes a greater amount of the charge deposited by the ionizing particle to be collected promptly (~300 psec), thus increasing the likelihood of an SEU (Shanfield *et al.*, 1985). A more detailed discussion of the funnel concept follows in Subsection 3.10.3.2.

3.10.3.2 Funneling

The model most often used to describe the funneling mechanism is the McLean-Oldham effective funnel length model (Oldham, McLean, and Hartman, 1986), which assumes that the track of an ion is an infinitely long, uniform column of charge with an initial radius of 0.1 μm that is generated in 1 psec. This cylinder expands in the radial direction by ambipolar diffusion and endures until the plasma density drops to about the substrate doping density.

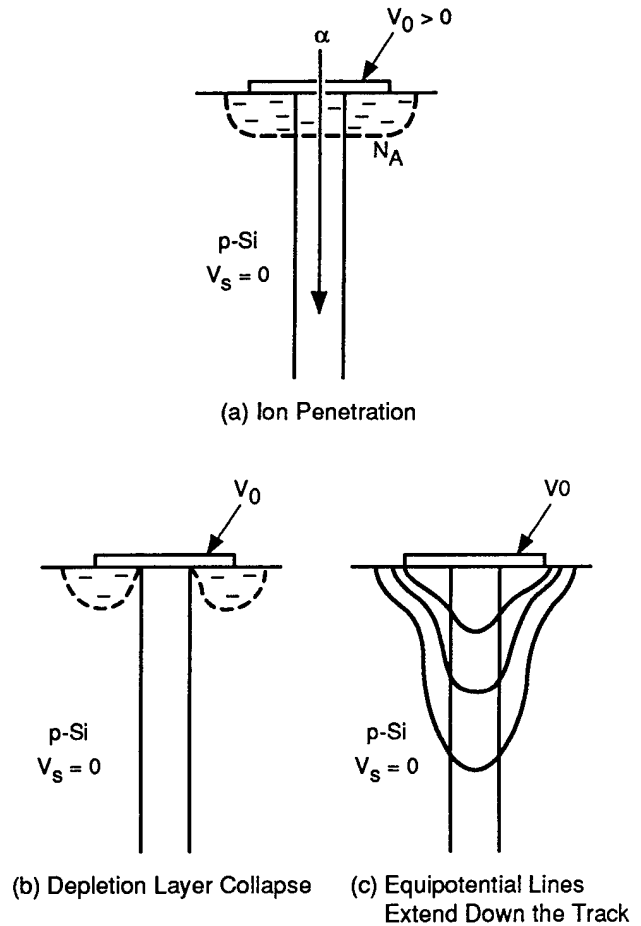


Figure 3-71 (a, b, c). Response of a diode junction field to heavy-ion penetration (McLean, 1987).

The creation of electron-hole pairs in the original depletion layer results in the neutralization of the depletion-layer electric field, the collapse of the junction, and propagation of the electric field along the ion track into the previously neutral substrate. During the charge-collection process, the depletion-region electric field extends down the charge column. After the depletion layer is neutralized, a dense column of charge, in reality a "plasma wire," is in contact with an electrode, which tends to screen external electric fields from the interior of the column. The distortion of the equipotential lines down the track means that much more charge is rapidly collected from outside the depletion region than would otherwise be possible. Thus, funneling will cause more charge to be collected at the struck node, increasing the possibility of upset Figure 3-72.

At characteristic time t_c , determined by the dielectric relaxation time of the substrate, the electric field lines return to the original depletion-layer configuration. Thus, the electric field varies both as a function of position and time. The effective funnel-length model assumes that this spatially complicated and time-variant field can be represented by an effective average electric field that exists for a duration t_c , and it provides a self-consistent way to determine this av-

erage electric field. Such an assumption ignores many of the details of the transient response of the device, but has been shown to be in good agreement with experimental results for low-LET-sensitive devices (*i.e.*, $L_{th} < 30 \text{ MeV-cm}^2/\text{mg}$) (Oldham, McLean, and Hartman, 1986).

3.10.3.3 Physical Analysis

Kreskovosky and Grubin (1986) have conducted detailed analyses and model simulations of the charge-collection process using (1) the drift and diffusion equations for electrons in the substrate, and (2) the Boltzmann transport equation for electrons in the active layer of devices. The transient response following the strike by a single ionizing particle requires that the transport of electrons and holes generated in the device and the equipotential distortions be determined as functions of time. This is done by the solution of the continuity equations,

$$\frac{\delta N}{\delta t} = -\nabla \cdot (N \mu_N \nabla \psi) + \nabla \cdot D_N \nabla N + g - R, \quad (3.51)$$

$$\frac{\delta P}{\delta t} = \nabla \cdot (P \mu_P \nabla \psi) + \nabla \cdot D_P \nabla P + g - R, \quad (3.52)$$

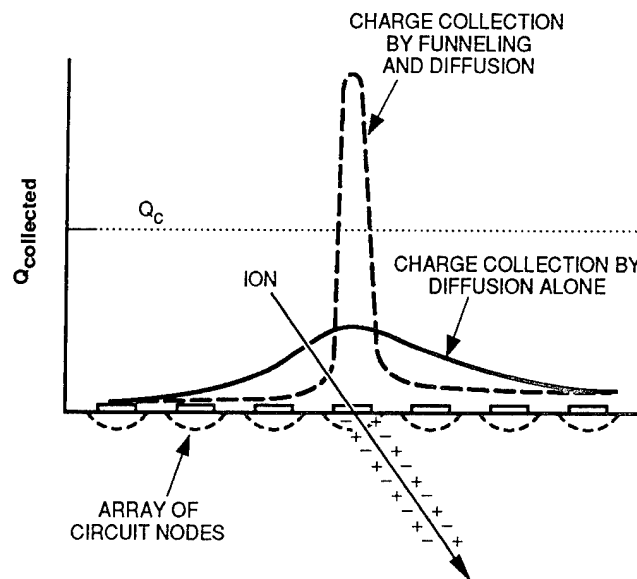


Figure 3-72. Charge-collection curves for a circuit array, showing that maximum charge is collected at the struck node due to funneling (McLean and Oldham, 1987).

and Poisson's equation,

$$\epsilon \nabla^2 \psi = e(N - P - N_D + N_A) , \quad (3.53)$$

where N and P are the number densities of electrons and holes, and

- μ = mobility
- ψ = electrostatic potential
- D = carrier diffusivity
- ϵ = device material permittivity
- γ = calculated carrier generation rate
- R = recombination term
- e = electron charge

and N_D and N_A are the doping concentrations (donors/acceptors), such that:

$$g = \frac{N_p(r)}{\tau_p} \exp[-t(r)/\tau_p] , \quad (3.54)$$

where $N_p(r)$ is the concentration of particles generated in the track, $t(r)$ is the time elapsed from when the radiation particle penetrates the device to a specific point along the track, and τ_p is the time constant of thermalization (~ 3 psec).

Two processes contribute to carrier generation: impact ionization, and energy absorption from the incident ionizing particle. Additionally, the generation terms are highly material- and bombarding-particle-dependent.

Recombination is modeled as a combination of Shockley-Read-Hall and Auger recombination (Grubin, Kreskovsky, and Weinberg, 1984):

$$R = \frac{NP - N_i^2}{\tau_p(N + N_i) + \tau_N(P + N_i)} + r(N + P)(NP - N_i^2) , \quad (3.55)$$

where τ_p and τ_N are the carrier lifetimes (~ 1 μ sec) and r is the Auger rate constant. Note that the carrier lifetimes greatly exceed the lifetime of an SEU transient (Kreskovsky and Grubin, 1986). Arbitrary adjustments of the Auger rate constant have allowed reasonable matches between experimental work and computer simulations.

This analysis is only preparatory to beginning the considerations essential to model SEU simulations on a computer. It is to be noted that modern, widely used modeling tools restrict simulations to two-dimensional analysis; therefore, approximations are required. Recent efforts by Howard *et al.*, (1993) have advanced this analysis to a physics-based three-dimensional model using PADRE. The details of the approximations and the modeling processes themselves are beyond the scope of this handbook; suffice it to say that efforts to find truly predictive simulations of SEU phenomena continue.

3.10.3.4 SEU in Linear Circuits

The single-event upset of a digital circuit is the most well known and widely studied SEP. However, the passage of a heavy ion through a linear circuit, such as a sense amplifier or comparator circuit, also produces the ionization and the potential collection of charge that could be interpreted as a real signal. Sense amplifiers designed to read magnetic-core and semiconductor memories are capable of reading extremely small signals and are susceptible to such disturbances. Thus, the circuit designer must consider circuit speed and the I/O capacitances to help ensure that the ion strike is not interpreted as a valid signal. Recent work in this area has begun to shed light on how the susceptibility of analog devices to SEU affects the connected digital circuits (Koga *et al.*, 1993).

3.10.3.5 Upsets in Logic Circuits

The discussion thus far has centered around upsets in latching circuits. Memories, with their low capacitive loading, have historically been more susceptible than logic circuits such as microprocessors (Petersen and Marshall, 1988). However, microprocessors have large numbers of gates and are becoming increasingly more susceptible to upset as each new generation downsizes the individual logic cells.

In combinational logic circuits, the ionizing event and potential upset are not as tightly wed in either the spatial or temporal regime as in the SRAM. The sensitive region and the location of

stored information may be completely separate. Information stored in a latch is subject to corruption by erroneous signals induced in a sensitive node and transmitted to the latch by logic gates feeding the latch. For a single event to produce an upset in combinational logic, the following conditions must be met (Diehl-Nagle, Vinson, and Petersen, 1984):

1. The occurrence of an ion strike that is capable of producing a voltage transient large enough to propagate into the adjoining circuitry,
2. The existence of a critical path between the struck sensitive node and the data latch, thus allowing the struck node control of the latch,
3. Generation of a transient of sufficient energy and duration to write the latch,
4. Arrival of the transient at the latch during a latch write-enable state.

It is possible that the particle strike location and timing could be such as to directly affect the latch itself.

It is important to note that not all sensitive nodes that are upset will result in output errors

because the potential error can be overridden in the logic scheme. It is even more noteworthy, however, that not all errors will occur immediately after the ion strike. Many machine cycles, perhaps thousands, can pass before the error reaches an output path. Software can amplify the error and cause large regions of the circuit to have erroneous states before error detection. Figure 3-73 shows the error propagation in an Intel 80186 microprocessor, obtained by using an electron microscope to compare the voltages present in a chip without errors to those present in a chip that has had an error introduced. The differences show up as a pattern of highlighted areas (May *et al.*, 1984).

Heavy-ion irradiation of CMOS/SOS VLSI logic devices has been conducted and the experimental results compared with an analytical assessment (Newberry *et al.*, 1987). It was determined that three error types occur: bit errors, lost-data errors, and lost-data-path errors. A bit error results from the change of a bit within a logic word. A lost-data error occurs when one of the control bits is changed due to a particle hit, resulting in the failure of a single word to reach the output. In a lost-data-path error, a control bit

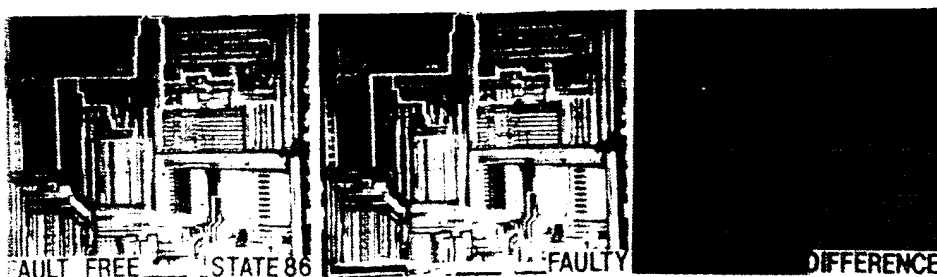


Figure 3-73. Error propagation in the Intel 80106 microprocessor logic circuit (May *et al.*, 1984).

is changed such that the entire data stream does not reach the designated output pad. Clearly, the fact that various types of errors can occur, and the inability to easily determine the origin of the error once it reaches the output pad, makes SEU evaluation of logic devices more challenging (Newberry *et al.*, 1987). Different approaches to SEU testing of microprocessors are discussed in Koga *et al.* (1985), Koga and Kolaskinsky (1987), and Elder *et al.* (1988).

3.10.3.6 Simultaneous Multiple Single-Bit Event Upset

The charge within an ion track and its subsequent spread can encompass more than one sensitive junction and thus upset more than one memory bit. The simultaneous upset of multiple single bits can be attributed to sufficient charge deposition by a single heavy ion that produces a track size sufficient to disturb more than one sensitive junction, or it may be due to charge diffusion to more than one sensitive node. Additionally, it has been demonstrated that ion tracks that strike a junction can affect the lateral spread of the charge, depending on the nature of the pull-up load on the struck junction (Zoutendyk, Edmonds, and Smith, 1988). For example, such multiple events comprise 5 to 10 percent of the reported SEU for the Harris HM-6508 CMOS SRAM. For the 93L422 bipolar RAM, multiple events comprise slightly more than 1 percent of the reported SEU (Martin *et al.*, 1987). As device miniaturization continues and critical-charge values decrease, the incidence of multiple errors can be expected to increase.

3.10.4 Circuit Response to Single-Event Phenomena

“Single” in the term SEP means that the error (or errors) produced can be attributed to a *single* ionizing particle producing ionizing charge in the device under consideration. Because of the nature of radioactive decay and of the cosmic-ray flux bathing the earth, SEP are random, both in time of occurrence and position within devices. However, two basic types of upset can be defined and examined: finite lifetime (“soft” errors), and permanent (“hard”) errors. In finite-lifetime up-

sets, the stored information is changed but the associated hardware is not damaged or altered. When the cell experiencing such logic upset is reset and tested, no degradation in its characteristics is exhibited. These finite upsets typically occur in random access memories and bipolar circuits, manifested generally as SEU. Permanent errors, commonly referred to as “hard errors,” are heavy-ion-induced failures in metal-nitride-oxide-semiconductor (MNOS) structures, silicon-nitride-oxide-semiconductor (SNOS) structures, and DMOS and BJT power devices. Hard errors include SEGR and SEB.

3.10.4.1 Single-Event Upset

MOS Circuits. Three failure modes for radiation-induced soft errors in DRAMs have been experimentally verified: cell failure mode, bit-line failure mode, and combined cell-/bit-line failure mode. Figure 3-74 shows a schematic layout of a DRAM. The horizontal lines are word or select lines, and the vertical lines are bit or data lines. An access transistor and storage capacitor at the intersection of a word and a bit line comprise a single DRAM cell. The access transistor permits the support circuitry to locate the individual cells for reading or writing. Figure 3-75 shows that the storage capacitor is formed by using a thin layer of silicon dioxide as the dielectric. Writing occurs when the appropriate word-line voltage is applied to the gate of the access transistor while the bit-line voltage is raised and charges the storage capacitor. At the end of the write cycle, the access transistor is returned to its OFF state. To read the DRAM, the access transistor is turned ON and the cell is connected to a sense-and-write amplifier that informs external circuitry of the cell state and restores the cell to its original state (Messenger and Ash, 1992).

Cell-failure results from charge collection by the storage capacitor in a one-transistor cell. When the collected charge exceeds a critical charge Q_c , a soft error occurs in the cell.

Bit-line failure occurs when charge collection reduces a sensing signal as a result of the unbalanced charge collection on a floating bit line or

floating-bit-line complement during the access cycle. The actual charge collection results from the connection of the ion-caused-charge diffusion area to an access transistor.

Studies by Rajeevakumar *et al.* (1988) identified the combined cell-/bit-line failure mode, which occurs when the storage capacitor collects a charge less than Q_c , and the bit line and bit-line

complement collect a differential charge less than Q_c while floating during a read cycle. Although the individual cell and bit-line charge collections are insufficient to produce a soft error, if their combined charge collection $\geq Q_c$ an error can result. At cycle times less than 100 nsec, this combined cell-bit line effect becomes the dominant upset mode (Rajeevakumar *et al.*, 1988).

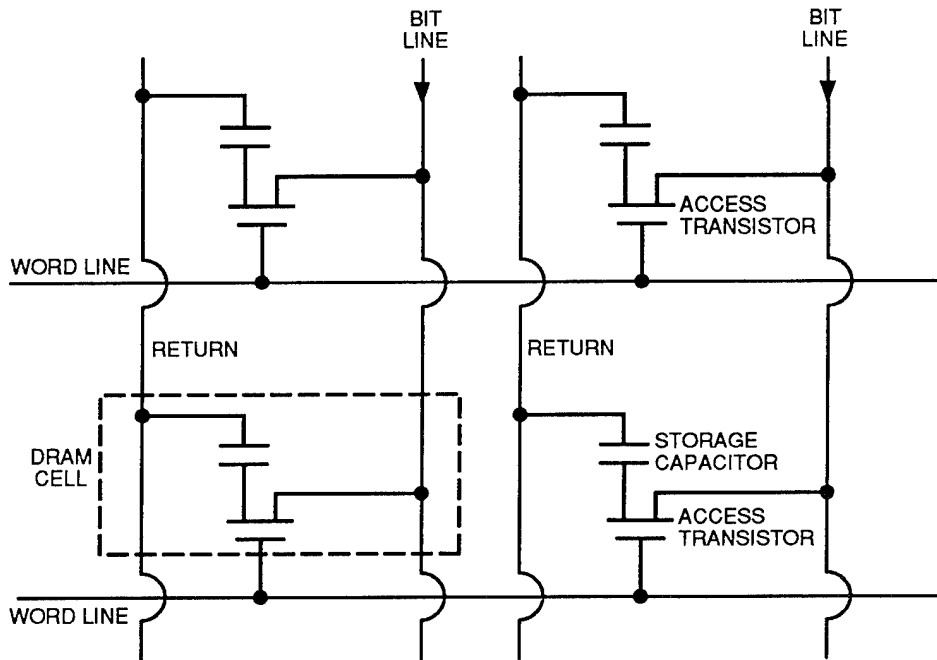


Figure 3-74. DRAM schematic showing four information-storage cells (Messenger and Ash, 1992).

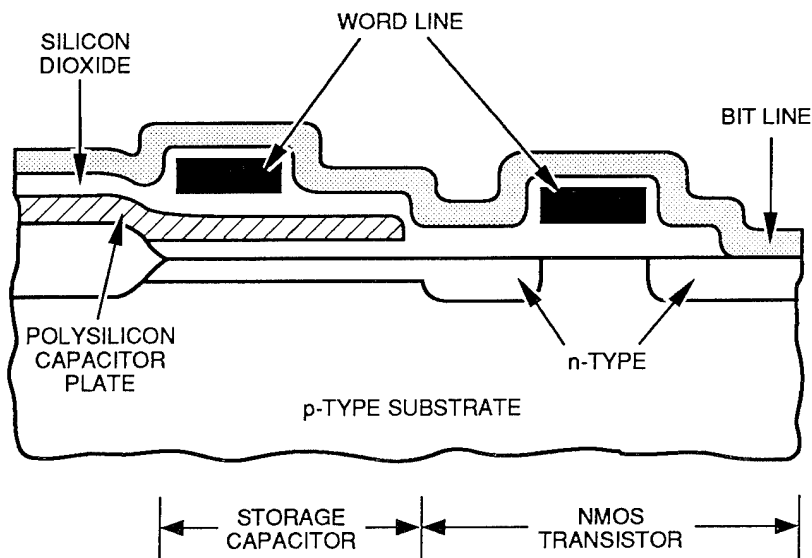


Figure 3-75. Diagram of a vertical slice of a single MOS DRAM cell (Messenger and Ash, 1992).

DRAM chips are inherently more susceptible to SEU than SRAM devices because no competing recovery mechanism attempts to restore the appropriate logic state.

SRAM devices use a bistable flip-flop formed by two cross-coupled inverters as the storage cell. Figure 3-76 is a schematic representation of a typical SRAM. The potential differences at the sensitive junctions collect the excess charge from the ion strike, which can be interpreted as a signal from the external circuitry to switch state. In such a flip-flop, the ON transistor controls the gate voltage of the other transistor and keeps it in an OFF condition. When the OFF transistor is driven ON by external means, it forces the ON transistor to the OFF condition. Basically, the flip-flop has two stable states and will remain in one of these states until forced to change, as long as power is applied to the circuit. These states can be easily interpreted by external circuitry as a logical one or zero. The SEU of the SRAM can be thought of as a particle strike causing sufficient charge deposition at the drain node junction of the OFF transistor to cause the flip-flop state to be reversed and the stored information to become corrupted. This occurs when the excess charge deposited in the drain of the OFF transistor attempts to drive the connected gate to the opposite bias and thus causes transition to the cell's other bistable state. Fortunately, in SRAM devices, the active transistor on the struck node attempts to maintain the currently stable cell configuration. Basically, the active transistor on the hit node attempts to dissipate the deposited charge and restore the proper gate voltage before the excess charge switches the gate bias of the struck OFF transistor. The success or failure of this inherent restoration mechanism is governed by the circuit resistor-capacitor (R-C) time constants and plays an important role in the circuit-hardening techniques [see Section 3.10.6].

Bipolar Circuits. When the memory speed is the most significant design feature, bipolar memory is the memory of choice for space applications. The optimization for speed means that the employed devices will have smaller capaci-

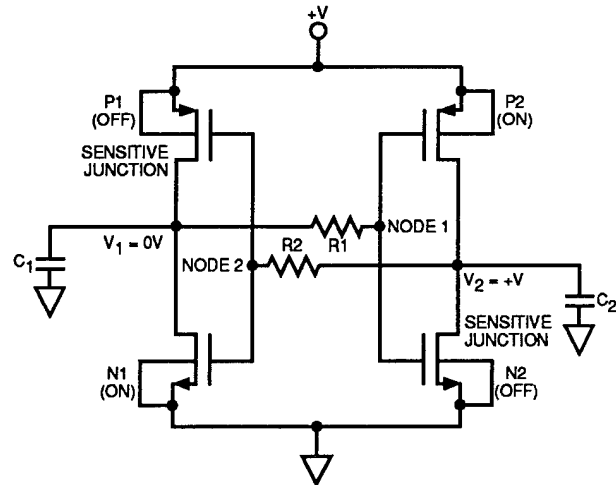


Figure 3-76. Schematic of a bulk CMOS SRAM showing upset-sensitive junctions (Petersen and Marshall, 1992).

tance values, smaller geometries, smaller noise immunity, and smaller critical charges; thus, in general, bipolar memories are quite susceptible to SEU. Current flowing through the base of the bipolar transistor is used to indicate the binary state of that transistor. Bipolar memories are characterized by large doping density variations and several closely spaced charge-collection regions (emitter, base, collector and substrate junction). The close proximity of multiple charge-collection regions that provide bipolar devices their inherent speed also presents many charge-collection regions for a penetrating ion to transit (Pickel, 1988).

Figure 3-77 shows the most commonly used types of bipolar memory cells, each cell type having its advantages and disadvantages. The fastest cell for reading and writing is the Schottky cell, but this cell has the largest number of parts and the highest power consumption. However, since this cell requires the largest logic-level voltage swing, it has the best SEU response. The IIL cell consumes the least power, operating at a slower speed than the other two. The emitter-coupled cell has power consumption and speed intermediate to the other two.

Figure 3-78 is a cross section of a bipolar transistor, showing three possible paths for high-energy particle penetration. It is essential to note that bipolar structures contain many sensitive

areas, each of which can be upset by different charge depositions. Additionally, particle track length can be such that a single particle penetrates several sensitive regions, as depicted in Figure 3-78. Experimental analysis has also re-

vealed that the voltage applied on a junction can affect the SEU-induced charge collection of a neighboring junction (Hauser *et al.*, 1985; Knudson *et al.*, 1984).

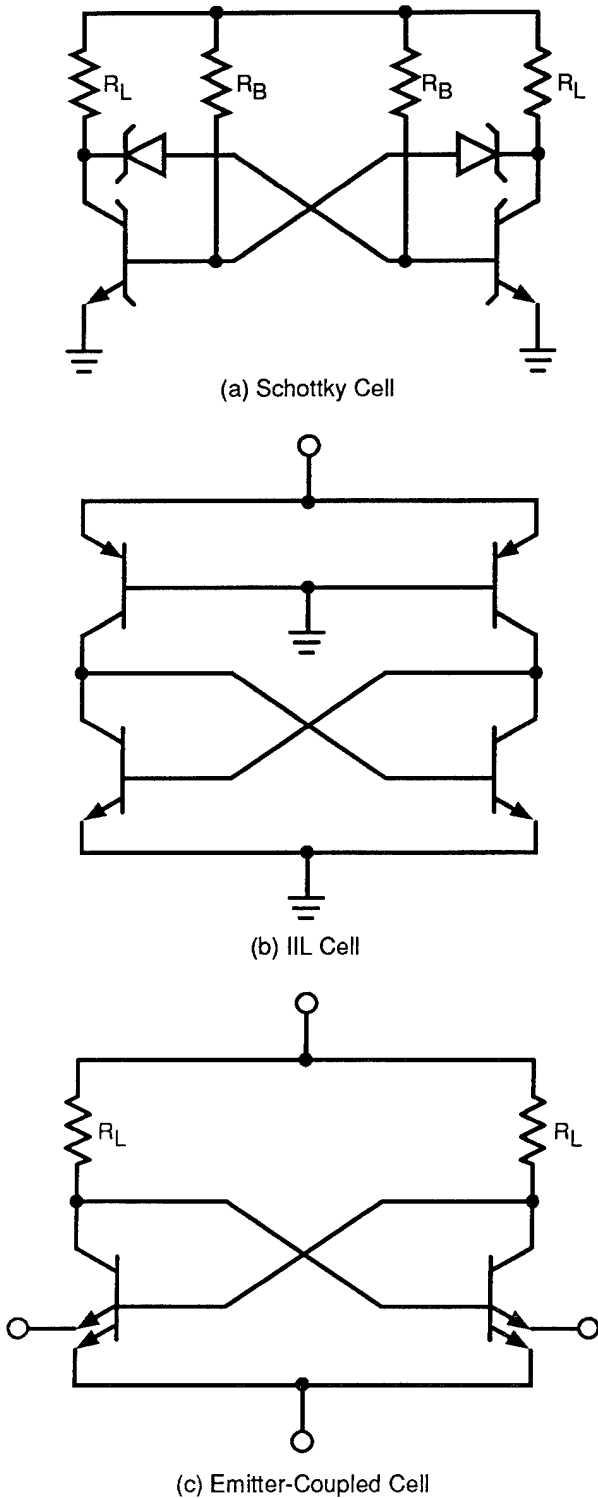


Figure 3-77 (a, b, c). Basic types of commonly used bipolar memory cells (Hauser, 1988).

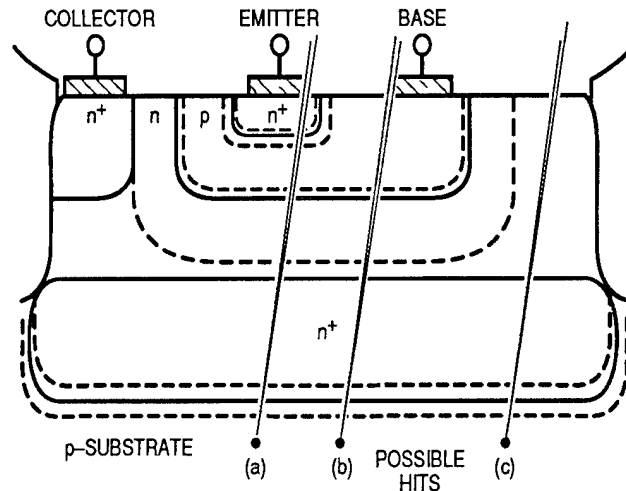


Figure 3-78 (a, b, c). Cross section of a bipolar transistor showing three of the many possible paths for high-energy particle intersection with pn junction: (a) emitter-base-collector region, (b) base-collector region, and (c) collector region (Hauser, 1988).

Gallium Arsenide Devices. High-speed GaAs circuits are acclaimed for their ionizing radiation dose hardness; however, their inherent SEU susceptibility exceeds that of silicon devices. The greater density of GaAs, relative to silicon, results in more direct ionization per unit of travel by the transiting heavy ions. Additionally, GaAs is sensitive to heavy ions impinging upon both the source-to-drain and the gate-to-drain volumes in a GaAs FET structure. Silicon CMOS devices, on the other hand, are only sensitive to strikes in the source-to-drain regions. Thus, GaAs FETs are more susceptible to upset than a comparable silicon device (Petersen and Marshall, 1988).

3.10.4.2 Single-Event Gate Rupture

Irreversible faults in nonvolatile, micro-electronic devices such as SNOS and MNOS memory capacitors are attributed to the rupture of the gate dielectric as a consequence of the heavy-ion passage. Studies of such hard failures (Wrobel, 1987) reveal the following:

1. Hard errors result from the combination of the energy directly deposited by the bombarding ion with the energy delivered by the electrical conduction through the ion track by the charge stored in the device.
2. The initial ion forms a highly conductive plasma ~ 5 nm in diameter, and the channel grows to 100 nm.
3. The ion strike must be of sufficient total energy to raise the dielectric temperature enough to cause the rapid thermal diffusion of the gate material and the subsequent penetration of the dielectric by this gate material. A scanning electron microscope (SEM) picture [Figure 3-79] of a failed device shows that the failure mechanisms are caused by dielectric penetration by either the aluminum or silicon. Additionally, the SEM photomicrograph shows that the devices were locally raised to temperatures above the melting points of the constituent materials.
4. The post-failure I-V characteristics for such capacitors were similar to diode

responses, and some were simply ohmic shorts through the dielectric.

5. An inverse relationship exists between the deposited ion energy and the applied voltage (several MV/cm) required to cause device failure.

To examine the possibility of melting the materials that make up these devices, consider the melting temperatures of the following materials:

Silicon:	1,412°C
Aluminum:	660°C
Silicon nitride:	1,900°C.

The change in temperature can be calculated as:

$$\Delta T = \frac{\text{energy}}{C_v (\text{volume})(\text{density})} \quad (3.56)$$

assuming

$$\begin{aligned} \langle \text{density} \rangle &= 2.5 \text{ g/cm}^3 \\ \text{track radius} &= 2.5 \text{ nm} \\ \text{track length} &= 80 \text{ nm} \\ C_v (\text{specific heat}) &= 0.8 \text{ J/g-}^\circ\text{C} \\ \langle \text{LET} \rangle &= 40 \text{ MeV-cm}^2/\text{mg}, \end{aligned}$$

which leads to



Figure 3-79. SEM photograph of heavy-ion induced failure induced by ^{252}Cf fission fragments (Wrobel, 1987).

$$\begin{aligned}
 \Delta T &= 40 \frac{\text{MeV-cm}^2}{0.001\text{g}} \left(1.6 \times 10^{-13} \text{ J/MeV} \right) \\
 &\quad \times \left(2.5 \text{ g/cm}^3\right) \left(80 \times 10^{-7} \text{ cm} \right) \\
 &\quad \div 0.8 \text{ J/g-}^\circ\text{C} \left[\pi \left(2.5 \times 10^{-7} \text{ cm} \right)^2 \right. \\
 &\quad \left. \times \left(80 \times 10^{-7} \text{ cm} \right) \right] \left(2.5 \text{ g/cm}^3\right) \\
 &= 40,743^\circ\text{C} \quad . \quad (3.57)
 \end{aligned}$$

Using a track length of 80 nm allows 40 nm for the dielectric and 40 nm for the underlying silicon, consistent with Wrobel's estimates. This localized temperature rise only accounts for the energy deposited by the heavy ion, and conduction of stored charge through this plasma will increase the temperature rise. Such localized temperature rises support the premise of material melting.

In addition, Browning *et al.* (1987) observed hard errors for MNOS nonvolatile RAMs and SNOS devices when neutrons induced fissioning of uranium contaminants in alumina ceramic packaging lids. This problem was not observed when the same devices were packaged with gold-covered kovar lids.

3.10.4.3 Single-Event Burnout

Experimental observation of burnout in power MOSFETs has been reported by Fischer (1987). Exposure to 330-MeV gold ions (LET = 83 MeV-cm²/mg) resulted in gate-oxide burnout for n-channel MOSFETs at voltages below the rated drain and/or gate breakdown voltages. Space environments, predicated on the assumption of "worst case = iron ions," are not this harsh. p-channel devices were found to be basically immune to burnout for LETs up to 40 MeV-cm²/mg. n-channel devices burned out between 22 and 90 percent of their rated breakdown voltage when bombarded with bromine ions.

3.10.4.4 Single-Event Latchup and Snapback

Latchup occurs in microcircuits due to electrical transients, pulsed ionizing radiation, and when a transiting heavy ion turns on a parasitic

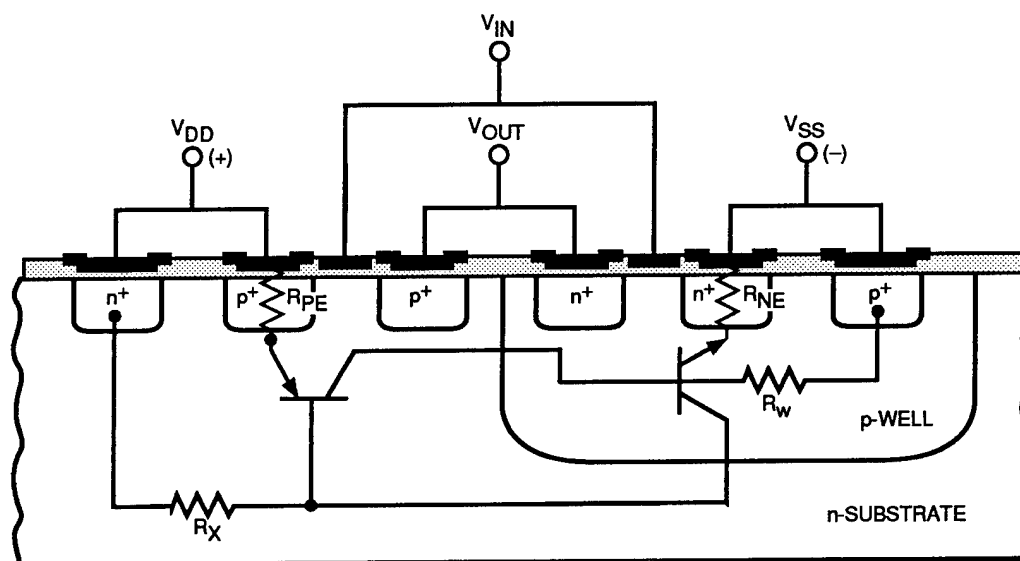
pnpn structure within the device. Latchup is a low-impedance state that results in a high-current drive that persists until the voltage drops below a certain voltage level (generally accomplished by cycling the device power) or until device damage occurs from overheating. Figure 3-80 is schematic representation of the two parasitic bipolar transistors inherent in a CMOS structure. The pnp and npn transistors are cross-connected, so the base-collector junctions are common.

Latchup prevention techniques seek to address the problem from both the semiconductor process and the circuit design process levels. Process solutions involve reduction of lifetime in the substrate (by neutron irradiation), gain degradation (so that $\beta_{\text{pnp}} \beta_{\text{nnp}}$ of the parasitic pnpn structure is below unity), buried layers (CMOS/SOS and CMOS/SOI), trench isolation, retrograde wells, guard rings (channel stops), and epitaxial substrates. Circuit-level solutions include current limiters, spacings between critical diffusions, substrate contacts, and biasing substrates so that they can never become forward-biased during operations.

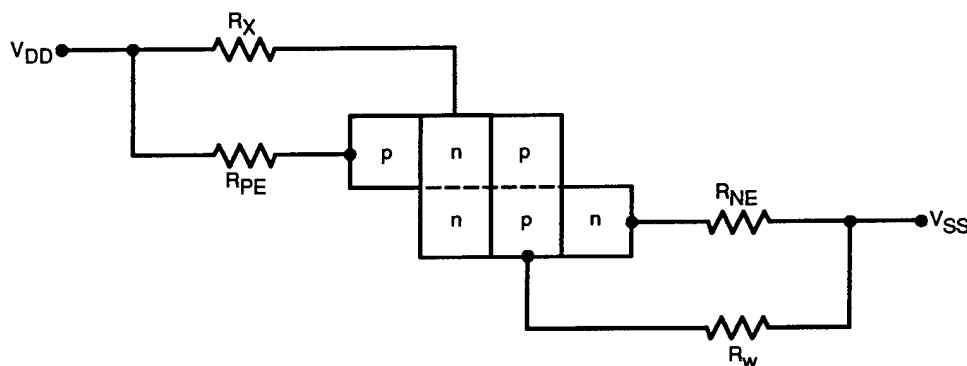
Snapback, an induced high-current mode of operation similar to latchup (but does not involve a parasitic pnpn structure), occurs in n-channel devices in NMOS and the NMOS regions of CMOS integrated circuits [see Subsection 3.8.3.1]. This induced high-current mode results from the fact that inherent in n-channel transistors a region of negative resistance exists that allows a device to settle into an improper, but stable, mode of operation at a lower drain-to-source voltage, thus perturbing normal device operations. Since the onset of snapback is accompanied by heating because of the increase in device bias current, it is essential to terminate this condition before metal fusing or melting occurs. The snapback condition can be terminated by normal device switching of the logic levels (Messenger and Ash, 1992).

3.10.5 SEP Testing and Modeling

The possibility of a potentially devastating upset, leading to mission failure, and the necessity of fielding economically viable parts and



(a) Cross Section



(b) Schematic

Figure 3-80 (a, b). Cross section and schematic representation of the two parasitic bipolar transistors inherent in a CMOS structure (Ma and Dressendorfer, 1989).

systems that must operate in an SEU environment require that testing and prediction procedures for parts and systems be available. Early investigators in this field, to their credit, produced conservative estimates of upset predictions to allow for unknowns about the environment and the correlation between earthbound testing and the realities of space operation. Research, experience, and improved knowledge have resulted in a recent review and refinement of upset-rate prediction methodologies (Petersen *et al.*, 1992), the thrust of which was to investigate the various prediction techniques used in the SEP community and to make recommendations regarding standard approaches that should be taken. Specifically addressed were device interaction models, environment models, and accelerator measurements. The

following subsections highlight the key points of the environmental models and the accelerator measurements.

3.10.5.1 Modeling Upset Rates in Natural Environments

The predictive modeling of upset rates in the magnetosphere of the earth's orbit is generally done using the CREME computer code model (Adams, 1986). This landmark work is a generally effective predictive tool for the ordinary solar minimum environment and is currently under revision to account for the latest understanding of the earth's radiation environment and to correct known deficiencies in model estimates. CREME allows the user to select from among 12 environments of varying severity. The appropriateness

and known limitations of each environmental model are discussed in Petersen *et al.* (1992). An essential revision to the CREME model will be to correct the model's overprediction of heavy-ion events during solar flares. [Satellite experience has indicated that large solar flares are accompanied by proton-induced SEUs; the current CREME model overpredicts the heavy-ion upset cross sections during flares by two orders of magnitude.]

3.10.5.2 SEU Characterization Methods

SEU testing for complete device characterization requires device cross-section measurement, either as a function of ion linear energy transfer (LET) or specific energy loss (dE/dx). The device cross section is expressed in terms of measured upsets per unit fluence, and the LET is the amount of energy deposited along the path by an ion of known energy. Device cross-section measurement as a function of specific energy loss, dE/dx , is nearly identical to LET but also includes the energy released to delta rays, whose energy may travel a considerable distance from the particle track. Delta rays are electrons that have sufficient impulse after leaving their ionized parent atom to cause further ionizations.

Current laboratory efforts obtain heavy ions from machines such as the Brookhaven tandem Van de Graaff accelerator and the University of California (Berkeley) 88-inch cyclotron. These facilities produce a variety of different heavy ions at a limited number of different energies. With energies of ~ 2 MeV per nucleon available, sufficiently penetrating ions can be selected to ensure transit through the overlayers and into the active regions of delidded devices, and with sufficient LET to exceed that expected in the cosmic environment. The normal technique employed in these experiments is to direct a series of ion beams, each of specified energy, onto a device with a known pattern of information storage. Beam fluence and the number of errors are recorded, and a single point on the upset cross section versus LET curve is generated based on the ion LET at the device surface. For accurate interpretation of the experimental results, it is essential to properly account for the changes in actual specific energy loss caused by overlayers, etc. that the ions must transit before reaching the active region of the device under test. Ion types and energies are varied to fully develop the SEU cross-section curves.

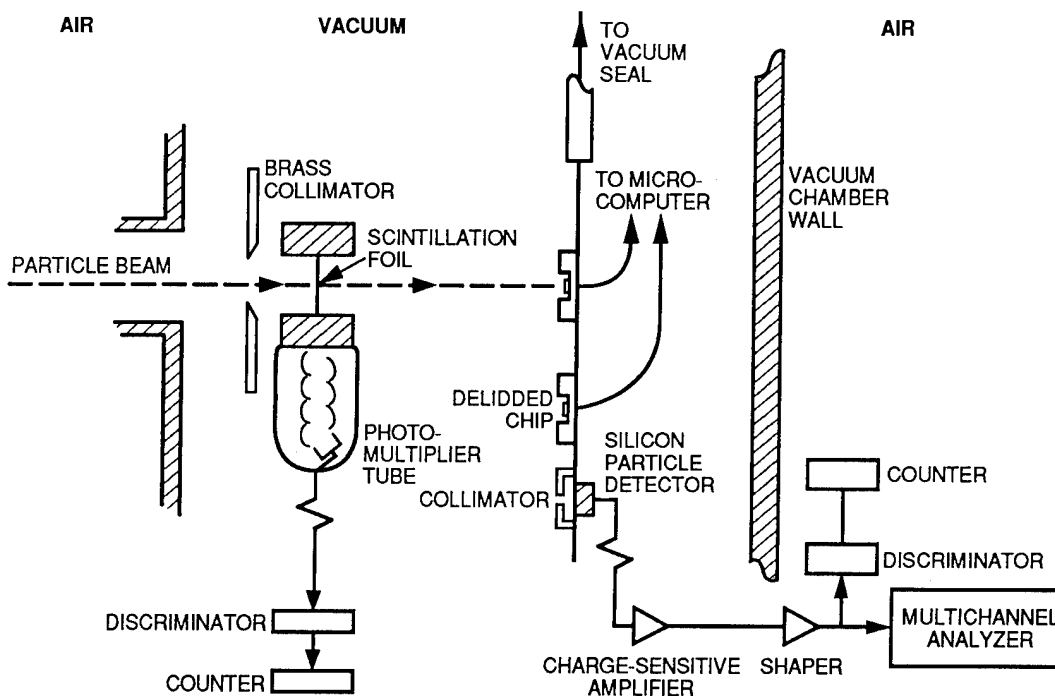


Figure 3-81. Typical cyclotron layout for SEU testing (Nichols *et al.*, 1988).

The definition of the threshold LET varies with the experimentalist. Jet Propulsion Laboratory reports define it as that value of LET where SEU first occurs for fluences exceeding 10^6 ions/cm². Others define it as the LET value where the cross section is 10 percent of the saturation cross section (Nichols *et al.*, 1988). The SEU cross section is defined as:

$$\sigma = \frac{\text{upset rate}}{\text{particle flux}} \quad (3.58)$$

A schematic representation of a typical cyclotron test chamber is shown in Figure 3-81. Since the beam fluences used for SEU testing are several orders of magnitude lower than those normally supplied at accelerator facilities, testers have developed their own dosimetry designed to count individual ions. The beam flux is measured by passing it through a thin film detector (TFD) made up of organic scintillation material. The light from the scintillator is conducted to a photomultiplier tube and counted. The ion energy is determined by the calibrated surface barrier detector (SBD) when it is positioned in the beam. A key feature of these chambers is the ability to vary particle LET by remotely positioning a selected device at desired angles in the beam using a motorized, translatable and rotatable board (Nichols *et al.*, 1988).

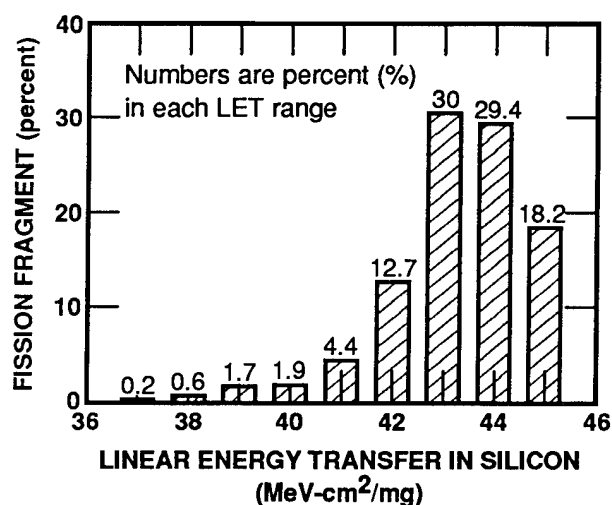


Figure 3-82. Calculated LET distribution of ²⁵²Cf fission fragment (Stephen *et al.*, 1984b).

3.10.5.3 Alternative Screening Methods

Van de Graaff accelerator and cyclotron results comprise the bulk of the SEU test data available. However, access to these test facilities is limited and tests must be scheduled months in advance. Additionally, the cost of characterizing a single part costs between \$10,000 and \$100,000, depending on the complexity of the experiment (Kolasinski *et al.*, 1979). Because of these drawbacks, economical alternatives have been sought, two of which are discussed below.

²⁵²Cf Cosmic-Ray Simulator. Since 100-MeV ⁵⁶Fe ions (LET = 27 MeV-cm²/mg in silicon) effectively represent the most highly ionizing particles encountered in the cosmic environment, acceptable testing sources must be able, as a minimum requirement, to provide these values. ²⁵²Cf, which produces fission fragments with a wide range of energy and LET values, was proposed as a cosmic-ray simulator. Stephen *et al.* (1984b) demonstrated that 95 percent of all ²⁵²Cf fission fragments have LET values between 41 and 45 MeV-cm²/mg, while 59.4 percent have values between 43 and 44 MeV-cm²/mg [see Figure 3-82]. By changing the angle of incidence or attenuating the fragment energies, effective LET from 20 to 75 MeV-cm²/mg can be realized (Browning, 1990; Kolasinski *et al.*, 1979; Velazco *et al.*, 1989). The first efforts to use ²⁵²Cf for SEU testing involved placing a ²⁵²Cf source in an evacuated chamber, bombarding the device under test (DUT), and calculating a single-upset cross section that, presumably, was the saturation cross section (Blandford and Pickel, 1985; Stephen *et al.*, 1984b). Such tests, however, do not adequately address the uncertainties associated with the LET dispersion. Furthermore, they fail to usefully characterize the SEU threshold and saturation cross section of a device because no means exist to provide the SEU cross section versus LET curve.

Recent work by Block *et al.* (1990), Browning (1990), Costantine (1990), Costantine *et al.* (1990), Howard *et al.* (1991), and Sanderson *et al.* (1987) has shown that ²⁵²Cf can be used as a valuable diagnostic tool by the researcher who understands and works within its limitations.

Nd:YAG Dye Laser. An alternative SEU test method, developed and demonstrated by Buchner *et al.* (1990), uses a picosecond, tunable Nd:YAG dye laser to measure SEU and latchup for different kinds of integrated circuits. This technique, in general, is nondestructive and can easily identify, and repeatedly return to, the exact location on the device that is responsible for the SEP, an ability that, of itself, makes this technique a valuable testing methodology for those interested in locating and eliminating design deficiencies.

3.10.5.4 Calculation and Models

Due to the high cost of testing and the scheduling problems at the high-energy accelerator facilities, SEP characterization has been supplemented by developing computer simulation programs to model circuit response to the postulated single-event environment. Such modeling is an integral part of ongoing developmental programs for space electronics. Properly designed models based on device physics can serve as reasonably reliable predictive tools that allow the designer to test and evaluate various options before silicon is manufactured. As a caution, it must be recognized that a model's predictive validity is only as good as the user's ability to identify inherent model limitations and avoid the temptation to apply the model outside of its design limits.

SEU computer simulation models for devices and circuits generally involve two different techniques, each of which has its limitations: (1) those that analyze charge deposition, collection, and transport by use of a physics-based simulation (*e.g.*, PADRE); and (2) those that seek to separate the processes of charge deposition and collection and analyze the effect of critical charge on circuit performance (*e.g.*, SPICE). A detailed discussion of model capabilities and limitations can be found in Kerns (1989); and a tutorial on SEU modeling is presented by Massengill (1993).

3.10.6 SEU Hardening and Processing

Alpha particles emitted in the header package can be stopped from entering the chip by a simple passivation layer. Since the passivation-

layer technique does not stop cosmic rays, other hardening techniques must be applied. As device miniaturization increased SEU susceptibility, the following process evolutions occurred in an effort to reduce the charge collected from ion bombardments: (1) increased doping concentrations, (2) decreased oxide thickness, and (3) twin and/or retrograde tubs on very thin epitaxial layers. The CMOS-on-epi technology placed the active regions of a device above a heavily doped substrate. The SOI technology placed an insulator under the active devices. These modifications increased capacitances per unit area and reduced funnel collection of ionization generated charges (Fu, Koga, and Kolasinski, 1987). Since the reduction of the charge-collection volume is key to reducing the SEU error rate, future manufacturing will likely move to very thin silicon layers over insulators to aid SEP tolerance in CMOS and bipolar technologies. DRAM manufacturing has focused on maintaining a relatively constant level of SEU sensitivity by maintaining a nearly constant storage capacitance of 50 Cf, even as the technology has scaled down.

3.10.6.1 Metal-Oxide Semiconductors

The basic problem remains, however; heavy ions, such as oxygen and iron (normal constituents in the cosmic spectrum) [see Figure 3-69], can still generate sufficient charge in a circuit node to cause a logic state change. On a typical CMOS SRAM memory cell circuit in a reasonable cosmic-ray environment, approximately 10–6 error/bit-day will occur. A hit at the appropriate drain node deposits charge that drives the connected gate to the opposite bias. At this point, it becomes a race, with the active transistor on the struck node trying to eliminate the deposited charge and restore the proper gate voltage before the charge switches the gate bias of the active transistor on the affected node. Frequently, as shown by the space environment error rates, the race is lost. One way to reduce MOS logic circuit susceptibility to SEU is to increase the R-C time constant of the coupling lines. The amount of R-C adjustment is a function of circuit parameters, such as nodal capacitance. For a 16k

SRAM, 100 k Ω resistance in the feedback path has successfully prevented SEU for 140-MeV Kr at room temperature (Kolasinski *et al.*, 1986). This resistance is usually incorporated into the memory cell by high-value polysilicon resistors. Increased resistance does increase the write time; thus, SEU hardening impacts performance (Dawes, 1985). Additionally, the fact that the resistivity values of polysilicon resistor vary significantly over the planned military temperature ranges must be taken into consideration since this affects both electrical and SEP properties.

3.10.6.2 Bipolar Memories

In bipolar memories, the need to delay the struck OFF transistor from turning off the ON transistor again means that this transition must be delayed for a time greater than that required for the ion-induced charge to dissipate. However, adding feedback resistors to bipolar cells decreases the critical charge and thus increases SEU susceptibility because the base current flows through the feedback path. Assuming the heavy-ion strike causes a drop in the collector voltage of the struck transistor, a hardening technique to simply delay the voltage drop from appearing at the opposite side of the cell until the struck transistor recovers will suffice. However, if the ion-induced charge deposition occurs in the emitter and the base, or just the base, the feedback path does not influence the transition and the struck transistor can go to the low-impedance state. To retain the original state of the memory, such an occurrence would require that information about the previous state be stored in the feedback path and be capable of restoring the original state (Hauser, 1988). The addition of one or more collector-follower transistors or emitter-follower transistors to the memory-cell feedback path has been demonstrated to change the memory-cell response time sufficiently to avoid upset. Charge stored in the followers provide sufficient stored charge to keep the ON transistor on until the struck transistor recovers. However, such a technique provides SEU hardness at the expense of speed and added circuits, which increase overall device size (Messenger *et al.*, 1988).

3.10.6.3 Gallium Arsenide Devices

Efforts to improve the SEU immunity of GaAs devices (Zuleeg and Notthoff, 1988) have shown that GaAs E-JFET SRAMs can be more SEU-tolerant than bipolar devices. However, studies by Campbell *et al.* (1989) continue to show that (1) problems exist with enhanced charge collection at structure element edges, (2) more charge can be collected at the gate than is deposited in the active layer, and (3) more charge can be collected at the drain than the total produced by the impinging ion. These issues indicate that further work can be done to improve the SEU immunity of GaAs SRAMs, albeit at the expense of circuit speed, cell size, and power dissipation.

3.10.7 System Approaches to SEP-Induced Errors

The potential effects of SEP in memories and logic devices have a major impact on the design of electronics for operation in space. To ensure that systems continue to perform in spite of errors, the accepted design approach involves employing two disparate, yet truly complementary, techniques: error prevention, and error toleration and correction.

3.10.7.1 Error Prevention

Ideally, error prevention seeks to develop hardened systems that are completely immune to SEP and requires that the system designer select individual parts that are designated SEP-immune and test these parts for the expected environmental conditions. Such an approach fails to recognize that individual parts may degrade or fail, and that repair of an orbiting system is generally not a viable option. A more realistic approach is to choose as many SEP-immune parts as feasible, recognizing that errors will occur and incorporating error toleration and correction schemes into the system design.

3.10.7.2 Error Toleration and Error Correction

Error toleration and error correction employ redundancies to allow for error detection and isolation, and the subsequent return of the system to

its correct state. The three basic forms of redundancy used follow below:

1. *Hardware redundancy* requires the use of duplicate units, majority voters with disagreement detectors, switching configurations, self-checking circuits, and error detection and correction circuitry. Hardware techniques for error detection include error coding approaches such as parity, Hamming codes, and checksums.
2. *Software redundancy* employs algorithms to solve fault-induced problems using concurrent program execution, breakpoint reasonableness testing, checkpoint storage, and the capability to rollback for recovery.
3. *Time redundancy* incorporates repeated execution of a certain system-state transition or code sequence and watchdog timers (Sievers and Gilley, 1985).

For a 16-bit word, 6 extra bits are required for single-bit error detection and correction. If two bits within the same word become erroneous because of SEU, several additional bits are needed for detection and correction. The use of totally redundant memory cells is a simpler alternative, albeit hardware intensive, solution to the problem of double-bit error correction. However, since neither solution is effective or efficient because of the demands on circuitry, a more accepted solution is Hamming-code single-bit error correction/double-bit error detection. But for chip organization such as $8 \times 8k$, where adjacent bits in a word are in adjacent cells, Hamming-code single-bit error correction/double-bit error detection will either not detect the adjacent errors or it will detect them but be unable to correct them. Double-bit errors in the same word can be avoided by spatially dispersing those memory cells representing a single word on two separate chips, as is the practice with the $64k \times 1$ layout. Such a solution works, but penalties are incurred when fine geometries or high-speed operations are required (Martin *et al.*, 1987).

Each of the redundancy techniques has benefits and drawbacks. The system designer must use these techniques within the constraints of weight, power, speed, and the need for data integrity, balancing the use of hardened devices and correction techniques while meeting mission constraints.

3.10.8 Conclusion

Single-event phenomena encompass a wide variety of problems encountered by satellite and avionic systems. Political scenarios mean little to this field since the villains are the naturally occurring components of space radiation that will always be present in the environments in which these systems must be deployed. The actual potential for failure increases as more computing capacity per pound of launch vehicle is required. Such a necessary goal mandates the use of microelectronic technology, which is undergoing continuous downscaling and, thus, increasing SEP susceptibility — unless vigorous hardening research keeps pace with device miniaturization. The challenge is to ensure that SEP circuit hardening guarantees that a single particle cannot deposit sufficient charge to disturb the circuit. Recognizing that this challenge may not always be met, adequate error detection/correction techniques that use hardware and software combinations must be employed to ensure that SEP are detected and corrected to make space systems error-tolerant and more surviveable.

3.11 List of References

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CHAPTER 4

DISPLACEMENT DAMAGE EFFECTS

The purpose of this chapter is to discuss displacement damage effects in semiconductor devices and material. Beginning with a brief discussion of the interaction of radiation with solid material, the effects of displacement, rather than ionization, are emphasized, followed by an introduction to the dynamics of atomic displacement in crystalline solids. The balance of the chapter discusses displacement damage effects on the physical properties of semiconductor, microelectronic, and optical devices.

4.1 Basic Mechanisms of Displacement Effects

All energetic nuclear radiation, even including high-energy gamma rays, can produce displacement damage in crystalline semiconductor materials. The specific radiations of primary interest in this chapter are neutrons, electrons, protons, and deuterons. Displacement damage effects result from atoms that have been displaced from their usual sites in a semiconductor crystal. In the simplest form, the displaced atoms become extra atoms inserted between lattice positions (interstitials), leaving behind unoccupied lattice positions (vacancies). The interaction of radiation with solid material depends on a variety of factors, including the mass, charge state, and kinetic energy of the impinging particle, and the atomic mass, charge (atomic number, Z), and density of the target material. The interactions that can occur between primary particles and target atoms follow (McLean and Oldham, 1987):

- Photons (\rightarrow high-energy secondary electrons)
 - Photoelectric effect
 - Compton scattering
 - Pair production
- Charged particles
 - Rutherford scattering

- Nuclear interactions (heavy particles)
- Coulomb interactions
 - Neutrons
- Elastic scattering
- Inelastic scattering
- Transmutation reactions.

In this chapter, displacement resulting from charged-particle interactions (Rutherford scattering) and neutron interactions (elastic and inelastic scattering) will be addressed. [Target material ionization engendered by these interactions is discussed in Chapter 2.] Charged particles incident on a target interact primarily by Rutherford scattering and Coulomb interaction. Rutherford scattering can cause both excitation and liberation of atomic electron ionization. Additionally, sufficient energy can be transferred through Rutherford scattering to atoms to displace them from their normal lattice positions. Heavy charged particles can also undergo nuclear interactions of the type described below for neutrons. For example, when a proton is absorbed in a target nucleus, the nucleus emits an alpha particle.

Neutrons incident on a target can participate in elastic scattering, inelastic scattering, and transmutation. In an elastic collision, the neutron gives up a portion of its energy to an atom of the target material, and can dislodge the atom from its lattice position. This process continues as long as the imparted energy is greater than that required for displacement (25 eV for most materials). The displaced atom, referred to as the primary recoil atom (or primary knock-on atom, PKA), will subsequently lose energy to ionization; it can also displace other lattice atoms.

Inelastic neutron scattering involves capture of the incident neutron by the nucleus of the target atom with the subsequent emission of the neutron at a lower energy. Kinetic energy is lost in this

process and the target nucleus is left in an excited state. The excited nucleus returns to its original state by the emission of a gamma ray. The kinetic energy of the emitted neutron is reduced, compared to the incident neutron, by the energy of the gamma ray. Inelastic neutron scattering can also cause displacement of the target atom.

Transmutation involves capture of the incident neutron by the target nucleus and subsequent emission of another particle (e.g., a proton or an alpha particle), resulting in the transmutation (conversion) of the initial element into another element.

Despite the complexity of these interactions, the two primary effects in semiconductor devices are displacement damage (atoms dislodged from their normal lattice sites) and ionization (electron/hole pair generation). In general, particles passing through electronic materials deposit a portion of their energy into ionization and the remainder into atomic displacements. However, for most practical situations, the ionization and displacement damage effects can be separated. For charged-particle irradiation, the primary modes of electronic device degradation result from ionization, although a certain amount of atomic displacement can occur — especially for the heavier ions. For high-energy neutron irradiation, the primary cause of device degradation is atomic displacement damage, even though considerable ionization (depending on the neutron energy) can occur. Figure 4-1 depicts the primary and secondary radiation effects in electronic devices. Only those interactions that can produce displacement damage are addressed in this chapter.

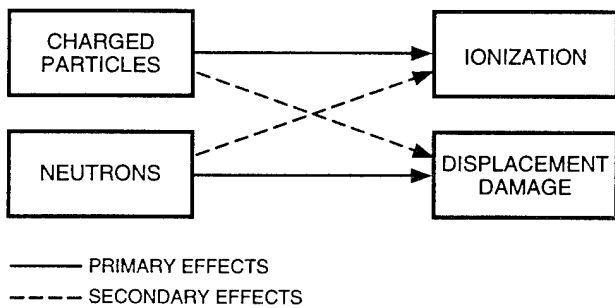


Figure 4-1. Schematic indicating primary radiation effects and secondary effects in electronic devices (McLean and Oldham, 1987).

4.2 Atomic Displacement Processes

Figure 4-2 is a schematic of the atomic displacement process in a crystalline lattice (e.g., silicon). An incident high-energy particle (e.g., a neutron) interacts with a target lattice atom via one of the mechanisms described in Section 4.1, imparting sufficient energy to the lattice atom to dislodge it from its initial site. The primary recoil atom (or PKA) may travel some distance in the lattice before coming to rest, possibly inducing further displacements in the process itself. The reflected primary particle continues through the lattice, also inducing further displacements as long as its kinetic energy is sufficiently large.

The important outcome of the atomic displacements is that defects are produced in the crystal lattice. These may be simple defects such as vacancies and interstitials [as shown in Figure 4-2(b)], simple combinations of these (e.g., divacancies), complexes of vacancies and interstitials with impurity atoms, or even more

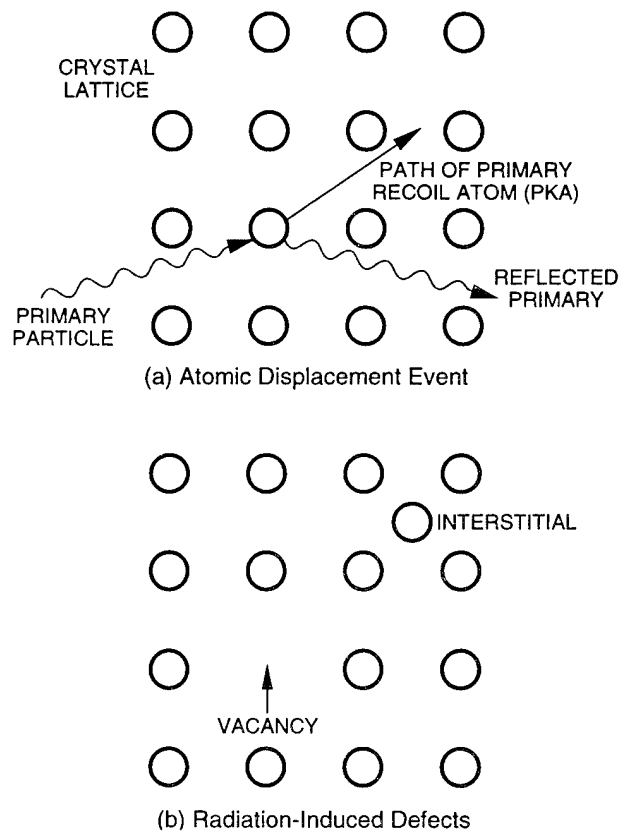


Figure 4-2. Schematic of atomic displacement damage in a crystalline solid (McLean and Oldham, 1987).

complex clusters of defects [defect clusters are important in neutron irradiation]. Figure 4-2(b) shows a simple vacancy defect at the initial lattice site and a simple interstitial where the PKA has come to rest. From the theory of crystalline semiconductors, it is known that any defects or impurities that disturb the lattice periodicity have the effect of producing localized, discrete energy levels lying within the forbidden bandgap of the perfect lattice, i.e., between the conduction-band minimum and the valence-band maximum. These electronic energy levels (gap states) associated with the radiation-induced defects cause an alteration of the electrical properties of the semiconductor crystal, leading to device degradation or failure. For example, additional recombination centers may be introduced, which can shorten the minority-carrier lifetimes and consequently degrade the gain of a bipolar transistor. The appropriate measure of displacement damage in a material is its effect on some pertinent electrical parameter, such as carrier lifetime or transistor gain. Subsequent sections of this chapter will address each of the effects in more detail. In addition, recent developments to characterize displacement damage in terms of non-ionizing energy loss (NIEL) [contained in Section 4.3.2] provide a more complete understanding of displacement damage phenomena.

4.3 Dynamics of Atomic Displacement

4.3.1 Damage Creation and Models

The basic physical interaction of displacement was shown in Figure 4-2. The primary reaction is caused by an incident particle striking a target atom and results in the target atom recoiling from the lattice site, as well as producing a scattered (reflected) particle. If the recoil has enough energy, the atom is knocked loose from its lattice site and comes to rest some distance away at an interstitial site. Moreover, the recoiling atom and reflected primary particle will undergo other interactions, which will then produce a cascade of displaced secondary atoms rather than the single vacancy/interstitial shown in Figure 4-2.

The simplest mathematical description of the scattering event illustrated in Figure 4-2 is that of an elastic two-body collision. The equations for

such a collision follow from the fact that both energy and momentum are conserved (Curtiss, 1959; Evans, 1955; Profio, 1979; Segre, 1965; van Lint *et al.*, 1980). Several assumptions are implicit in using an elastic two-body collision model. The particles are assumed to act like hard spheres, with no energy dissipated in electronic excitations or in nuclear reactions. Furthermore, no energy is assumed to be lost to the lattice (i.e., to other nearby atoms) when the recoil atom escapes. These assumptions are frequently well justified, because the energy lost in breaking bonds in the lattice is very small compared to the energy of the particles involved. For example, only about 25 eV is required to be transferred to a recoil atom in silicon in order to produce a vacancy/interstitial pair. On the other hand, the energy of typical incident particles is measured in MeV. In fact, many other materials also have critical displacement energies around 25 eV. If only a few electron volts out of a million electron volts are lost to electronic excitations and lattice distortions, these effects can generally be neglected.

In principle, any energetic particle (e.g., neutrons, electrons, protons, alpha particles, heavy cosmic-ray ions, etc.) can cause displacement damage. However, since neutrons interact with the target atoms differently than do charged particles, the results of such interactions must be considered separately. Neutrons do not interact directly with the electrons in the target material, and they lose energy only through nuclear interactions. For this reason, displacement processes are much more important for neutrons than for charged particles. For charged particles, interactions with atomic electrons cause most of the energy loss, but Coulomb scattering from nuclei can lead to displacement damage also.

The qualitative differences between the interactions of charged and uncharged particles are illustrated in Figure 4-3, which compares the energy deposited in tissue through different processes for 10-MeV protons and neutrons. [The results for silicon are qualitatively similar.] For the 10-MeV neutrons, the primary interaction is a nuclear scattering event, but the PKAs lose a large part of their energy through ionization. The

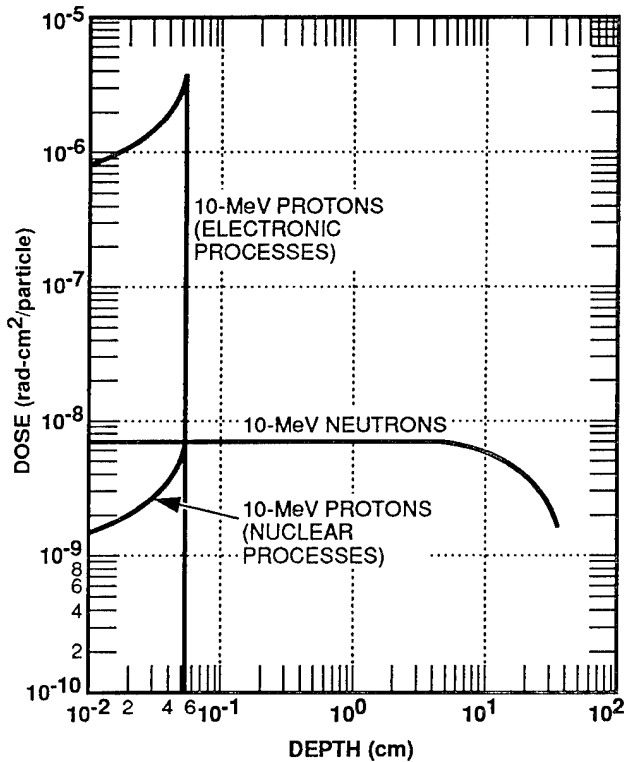


Figure 4-3. Energy loss in tissue for neutrons and protons [proton energy loss indicated separately for electronic and nuclear processes] (McLean and Oldham, 1987).

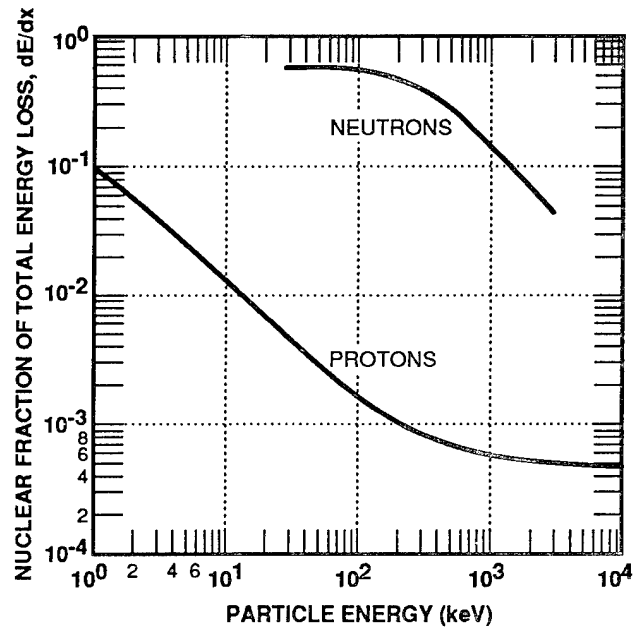


Figure 4-4. Nuclear fraction of total energy loss for protons and neutrons striking a silicon target (Lindhard, Scharff, and Schiott, 1963).

total energy loss for neutrons is plotted in the figure, but only a small part of this energy loss actually goes into displacement processes. The remainder is lost by ionization in the slowing down of the PKAs [see Figure 4-4]. For the proton curves in Figure 4-3, the nuclear energy loss and the electronic (ionization) energy loss are plotted separately. Electronic processes account for roughly three orders of magnitude more energy loss than nuclear processes.

In Figure 4-4, proton energy loss from nuclear processes is plotted as a fraction of total energy loss (nuclear plus electronic). For neutrons, the nuclear fraction of total energy loss is plotted for a primary PKA(Si). For example, a silicon atom with an initial energy of 1 MeV would lose about 20 percent of its energy through nuclear processes. If these results were replotted in terms of the energy of the incident neutrons, the curve would obviously be shifted to the right. For this

reason, the neutron curve in Figure 4-4 is a limiting case rather than an "exact" result.

The salient points are that the total energy fraction going into atomic displacements is one to two orders of magnitude greater for neutrons than for protons, and that the neutron range is many orders of magnitude greater than protons [Figure 4-3]. The conclusion is that neutron irradiation is much more effective in degrading electrical properties of semiconductor electronics due to displacement damage.

Defects created by incident particles can be classified as simple defects (vacancies, divacancies, vacancy/impurity complexes, interstitials, di-interstitials, interstitial/impurity complexes) and defect clusters. Several models have been postulated to characterize displacement damage, three of which are briefly discussed below.

4.3.1.1 Gossick Model

Failures in the attempt to explain experimental results in terms of isolated point defects led to the development of the Gossick model (Gossick, 1959), which postulates the existence of a large

disordered region, or defect cluster [Figure 4-5]. The core of the damage region, with radius R_0 , is assumed to be compensated intrinsic material, i.e., electrically neutral. The outer shell of the damaged region, between R_0 and R_1 , is assumed to be charged by trapped majority carriers (electrons in this example), which balances the trapped minority-carrier charge. In the Gossick model, the disordered region presents a potential barrier to majority carriers and a potential well to minority carriers, with the result that defect clusters serve as very efficient regions for minority-carrier recombinations (Srouf, 1982).

A "typical" distribution of clusters produced by a 50-keV silicon recoil atom is shown in Figure 4-6. No one has argued that the clusters are truly spherical, although a spherical shape is fre-

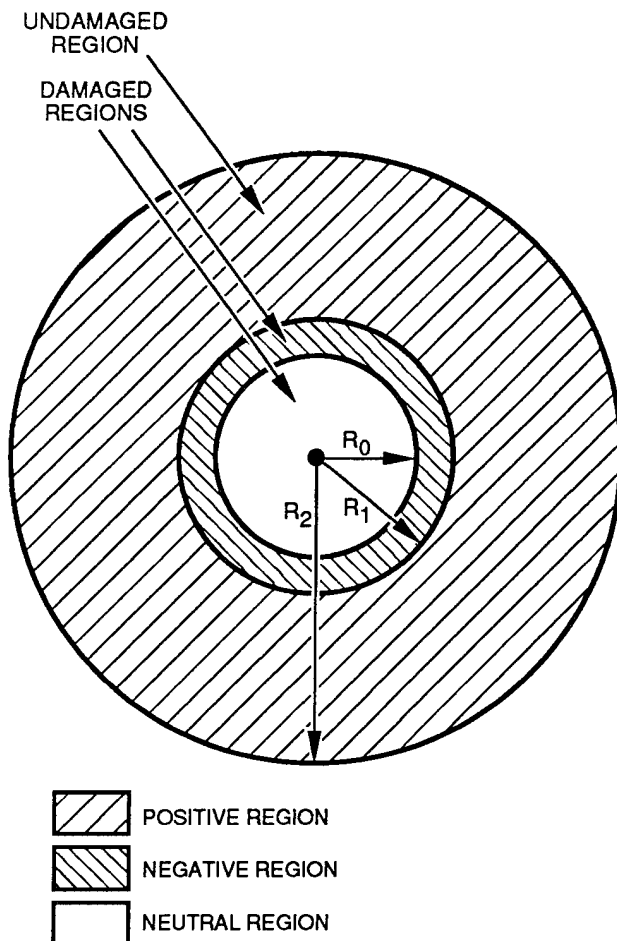


Figure 4-5. Gossick model for defect clusters in neutron-irradiated n-type silicon (Gossick, 1959; Srouf, 1982).

quently assumed for convenience in modeling. The size of the clusters and their spatial distribution have been somewhat controversial topics over the years. Gossick himself has noted that a damaged region would typically constrain 10^5 to 10^6 atoms, corresponding to $R_1 = 15$ to 20 nm. The largest cluster observed by electron transmission microscopy in samples of neutron-damaged silicon, however, are nearly at the limits of detection, having dimensions of 4 to 5 nm; clusters with dimensions of 15 to 20 nm are not observed in such samples. Variations on the Gossick model have been postulated by Mueller, Wilsey, and Rosen (1982) and Srouf (1982).

4.3.1.2 Mueller-Wilsey-Rosen Model

The conventional picture developed by Gossick (1959), and elaborated on by others, has recently come into question, based on detailed calculations using the binary-collision simulation code MARLOWE (Mueller, Wilsey, and Rosen, 1982). In the Gossick model, the PKA cascade produces a localized cluster of high-defect density whose dimensions are a large fraction of the PKA range. This high-defect density gives rise to a space-charge region, which can be much larger than the defect cluster (depending on doping density). Alternatively, the MARLOWE code calculations predict that PKAs produce long trails of low-defect density [Figure 4-7], some of which branch out, with very small clusters of approximately 50\AA diameter located at the end of the tracks. These tracks are expected to have much less effect on material parameters, e.g., resistance, than small clusters, which can be viewed as nonconducting voids.

4.3.1.3 Srouf Model

The Srouf model is a distributed cluster model, in which the conventional neutron cluster model is assumed; however, the detailed energy and elastic angular distributions are taken into account [see Figures 4-8 and 4-9].

For this model, the PKAs interact with other silicon atoms, causing displacements and producing more recoiling atoms. The density of displacements is small near the beginning of the PKA range and large near the end. The low-defect-density regions probably contribute little to

the measured change in resistance except as compensation centers. The high-defect-density regions can be viewed as localized damage clusters that act as nonconducting voids. Only those voids overlapping the sensitive volume of, for example, a diffused resistor will cause an increase in resistance. Since a distribution of PKA energies and angles exists, limits are imposed on the location of the neutron interactions that produce a PKA, which can cause an overlapping void. The energy and angular distributions also

result in a distribution of void sizes. Combining these effects results in a distribution of resistance changes caused by the statistical nature of neutron interaction, PKA path, and void size.

4.3.2 Energy Deposition by Incident Radiation

Although the models described in the foregoing subsections have been useful in providing an understanding of these effects, more recent studies emphasize the non-ionizing energy loss

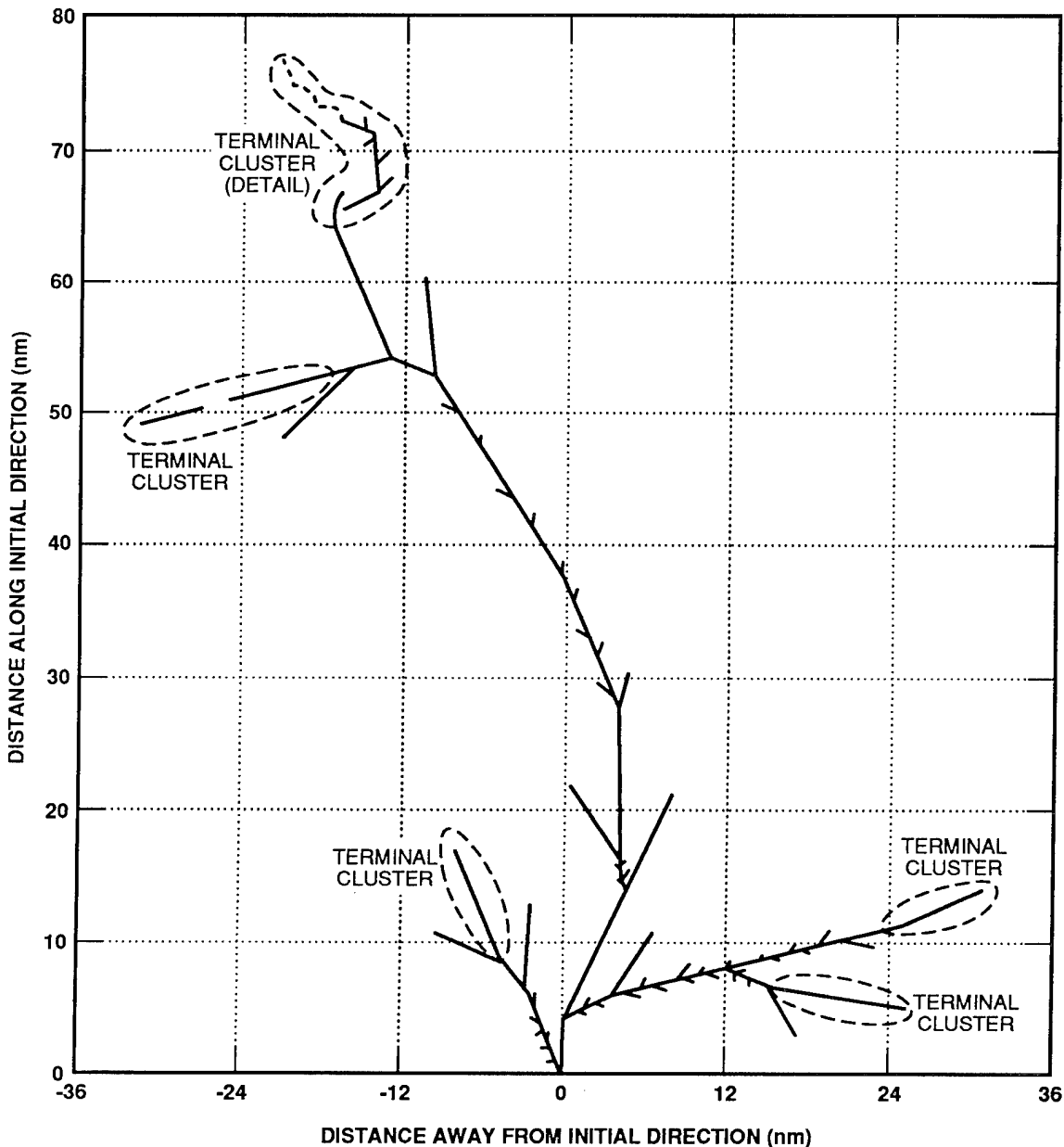


Figure 4-6. Typical recoil-atom track with primary energy of 50 keV (van Lint, Leadon, and Colwell, 1972).

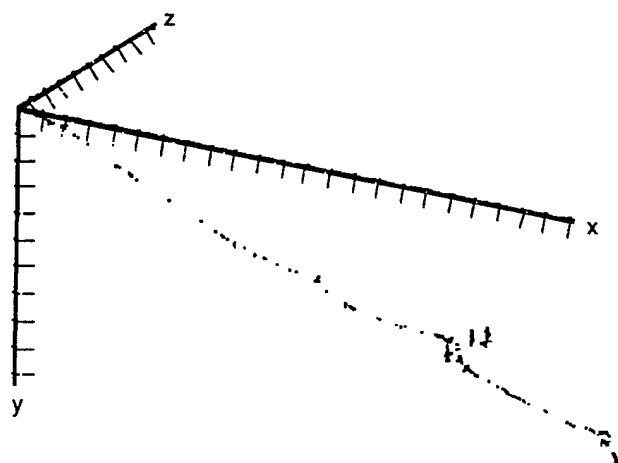


Figure 4-7. Typical recoil-atom track with primary energy of 50 keV, calculated using the Firsov interaction radius [tic marks denote 10-nm increments] (Mueller, Wilsey, and Rosen, 1982).

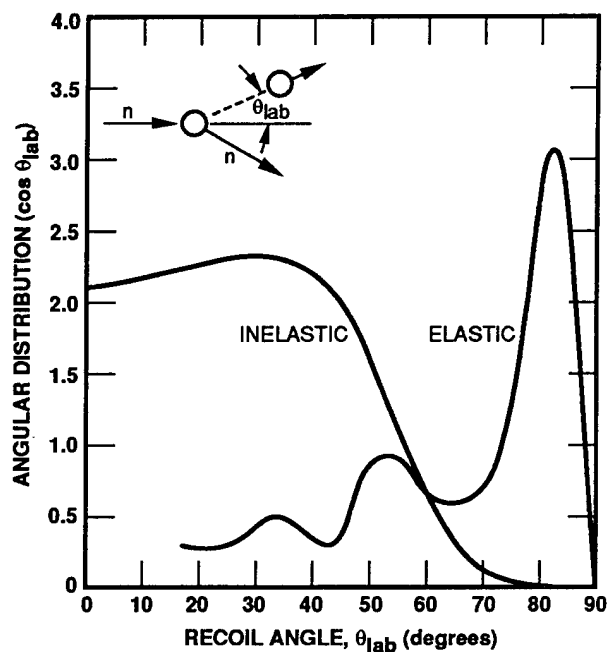


Figure 4-9. Angular distributions of elastic and inelastic interactions in 14-MeV neutron-irradiated silicon (Srouf, 1983).

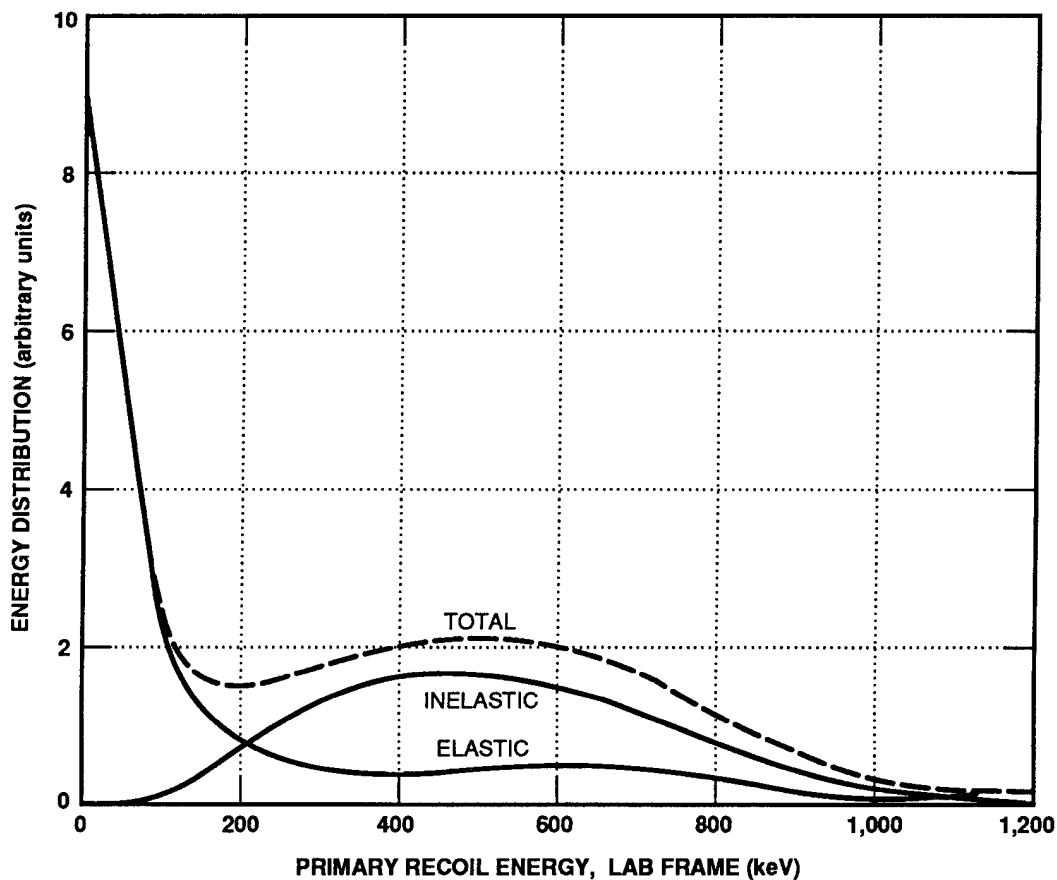


Figure 4-8. Distributions of primary recoil energies for elastic and inelastic interactions in 14-MeV neutron-irradiated silicon (Srouf, 1983).

(NIEL) approach. Additional dynamics of atomic displacement are presented here to provide a more detailed description of the process and additional references for the interested reader.

The production of displaced atoms in an irradiated crystalline solid proceeds in step-wise fashion as follows:

1. An energetic particle traversing the crystal interacts with a lattice atom, imparting to it a recoil energy, E_R . The interaction can be a simple elastic collision (billiard ball), or it can be a nuclear reaction from which are emitted a recoiling heavy atom and one or more lighter nuclear particles. In the case of neutrons, the elastic collision is due to the nuclear force; in the case of charged particles, it can be due either to the Coulomb force (Rutherford scattering) or the nuclear force. Nuclear reactions, which can be elastic or inelastic scattering or transmutation reactions, are produced via the nuclear force. In the case of energetic gamma rays, an electromagnetic interaction produces an energetic electron, which then can impart enough recoil energy to a lattice atom to cause a displacement.
2. If the recoil energy is greater than about 25 eV (the effective threshold energy applying to atomic displacements in silicon, germanium, and gallium arsenide), the target atom leaves its lattice site, leaving behind a vacancy, and goes on to collide with other lattice atoms. This first recoiling lattice atom is called the primary knock-on atom (PKA). The collisions between lattice atoms take place via the Coulomb force [the nuclear force may play a role at extremely high PKA energies (e.g., >100 MeV), but such energies are produced only rarely by heavy-ion cosmic rays and are not of concern for bulk displacement damage].
3. If recoil energy E_R is large enough, the PKA displaces other atoms from their sites, creating more vacancies and displaced atoms and more recoiling atoms. Any atom moving in a solid loses energy as it travels, and the production of displaced atoms ceases when the energy of the moving atom has dropped below about 25 eV. The succession of collisions and recoiling lattice atoms resulting from a single PKA is called a collision cascade, which takes less than 1 psec to develop. Because the recoiling atoms are charged, they produce not only displacements but also ionization in the lattice. To estimate displacement damage effects it is therefore necessary to understand what fraction of the PKA energy goes into displacement. A generalized theory for the fractions of PKA energy that go into ionization and displacement has been developed by Lindhard, Scharff, and Schiott (1963). These fractions depend on the PKA energy and on the host material. Strictly speaking, the fraction of PKA energy that is non-ionizing includes displacement energy and the energy going into lattice phonons. [The partitioning between displacement energy and energy going into lattice phonons is not discussed here but can be significant when the *average* PKA energy is below about 2 keV.]
4. In a collision cascade in a solid, when a recoiling atom has degraded in energy to about 5 keV or less, the Coulomb collision cross section becomes so large that the recoiling atom and any recoil atoms associated with it interact essentially with every lattice atom they pass. The density of displaced atoms then becomes extra large and this region is said to contain a subcluster of damage. The dimensions of such a subcluster have been shown in Monte Carlo simulations to be less than about 50 Å on average. Figure 4-6 shows a diagram of a typical recoil atom track in two dimensions and the subcluster regions at the end of each branch of the col-

lision cascade. The starting point for the calculation was a 50-keV silicon atom moving parallel to the ordinate and entering the silicon crystal at the point labeled zero on the abscissa. Subclusters are also present on each short spur, but they are not all shown in Figure 4-6. The chronology of events that leads to tracks similar to those shown in Figure 4-6 follows: (1) in the energy region above about 100 keV, the silicon recoil atom loses most of its energy by ionization; (2) as it slows down, the fraction going into ionization decreases and the fraction going into displacements increases; and (3) when the moving atom has about 5 keV, most of the energy loss is non-ionizing and a "subcluster" region of damage develops.

5. In about $\sim 10^{-10}$ second, the collision cascade has developed and all the recoil atoms that have come to rest close enough to a vacancy will immediately recombine with that vacancy. Because the times are so short, initial recombination processes are not easily accessible to measurements on material or device properties. Indirect studies on metals and semiconductors have shown, however, that perhaps 90 percent or more of the initially produced vacancy-interstitial pairs recombine immediately. According to Monte Carlo simulations, a 90-percent recombination rate implies that any interstitial-vacancy pair that is not separated by more than about two lattice spacings will recombine. In silicon and germanium, the vacancies and interstitials (Frenkel pairs) are unstable at about 100°K; above 100°K, the thermal energy of the crystal is sufficient to cause them to migrate. On a time scale ranging from about 1 msec to tens of minutes, the mobile defects surviving the initial recombination are either annihilated by recombination of vacancy-interstitial pairs, are immobilized by the formation of stable defect complexes with other impurities or lattice defects, or

escape to a free surface (dislocate). The ability of a defect to move through the crystal may be strongly affected by its charge state.

6. The presence of these stable defects then generally causes the macroscopic electronic properties of the material to change. In silicon and germanium, the electrically active defects involve the vacancies but do not seem to involve the interstitial atoms.

The correlation between NIEL and atomic displacement damage effects is discussed here. This discussion follows the work of Burke (1986), Summers *et al.* (1986), Summers *et al.* (1987), and Marshall *et al.* (1989), that revealed that the amount of degradation produced in silicon and germanium semiconductor devices is linearly proportional, to first order, to NIEL experienced as incident radiation by semiconductor material. This proportionality has been observed for irradiating particles ranging from electrons, neutrons, protons, deuterons and alpha particles, and for energies ranging from a few to tens of mega-electron volts. This proportionality has also been observed over seven orders of magnitude in NIEL for a high-temperature superconductor, a material very different from a single-crystal semiconductor (Summers *et al.*, 1989). Figure 4-10 shows a comparison of experimental results and theoretical NIEL calculations for displacement damage produced in silicon bipolar transistors by protons, deuterons, and helium ions. It is important to note that the NIEL calculations are absolute and were not normalized to fit the experimental data. The experimental data are plotted as a ratio of the particle damage factor to the neutron damage factor (for 1-MeV neutrons on silicon) in order to remove the dependence on injection current.

NIEL is analogous to the more familiar quantity dE/dx , ionizing energy loss (also called the stopping power); usually, the same units are used for NIEL as for dE/dx , *viz.*, MeV/g per cm^2 /incident particle or MeV- cm^2 /g per incident particle. NIEL and dE/dx are both functions of the type of incident particle, its energy, and the composition

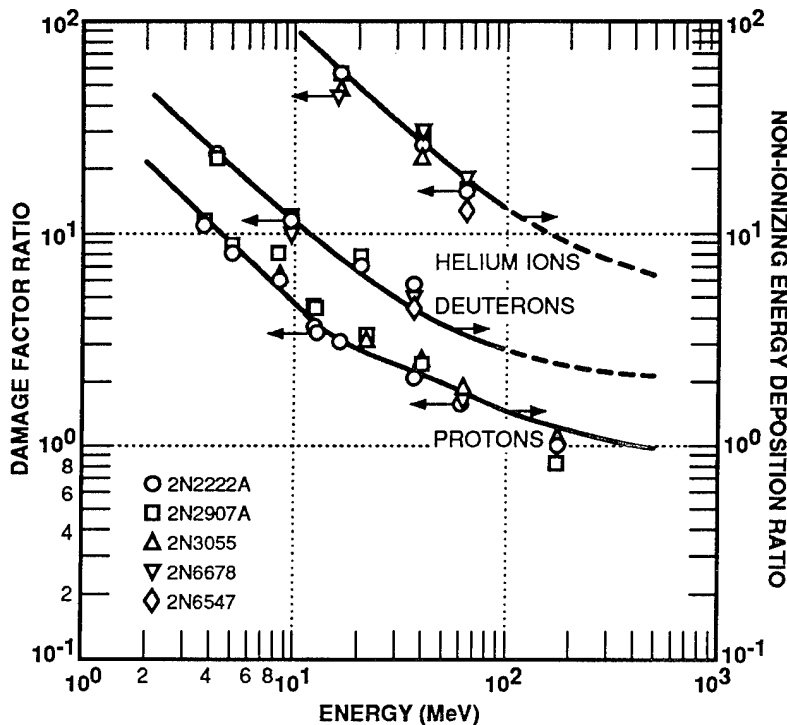


Figure 4-10. Damage factor ratios for bipolar transistors for protons, deuterons, and helium ions of 1-MeV-equivalent(Si) neutrons as a function of energy [the data points are read from the left-hand axis and the calculational curves from the right-hand axis] (Summers *et al.*, 1987).

of the material being irradiated. To obtain the total energy deposited by a single incident particle in the material being irradiated, it is only necessary to multiply the NIEL (or dE/dx) by the target thickness in g/cm^2 . For a beam of particles whose total incident fluence is expressed as particles/ cm^2 , the product of NIEL and the fluence gives the total energy per gram going into non-ionizing energy; just as the product of dE/dx and the fluence gives the total energy per gram going into ionization. For ionizing energy, this latter quantity is usually called the absorbed dose and, for silicon, is given in rads(Si).

It should be noted that device degradation depends on the final damage produced, while NIEL is a measure of the initial displacement damage produced (90 percent or more of which may recombine immediately). The observation of a linear proportionality between device degradation and NIEL for a variety of materials and incident particle masses and energies, therefore, has fundamental implications regarding the production and effectiveness of final displacement damage.

The finding of linearity between a particular device parameter degradation and NIEL implies, first of all, that the number of final electrically active defects that are responsible for the degradation in that parameter does not depend on the type or energy of the particle that produced the initial damage. This behavior, in turn, implies that the microstructure of the initial damage does not affect how it develops into that particular defect or the number of defects it produces.

Deviations from linearity with NIEL have been observed by Dale (1988), Griffin *et al.* (1989), and Griffin (1991). These deviations have been explained in a variety of ways and investigations to provide a better understanding of these discrepancies continue. Thus, caution should be used in assuming a linear dependence of device parameter degradation on NIEL, especially in materials other than silicon and germanium.

An issue remaining to be investigated is whether different types of irradiating particles will favor the production of one type of defect in

a material over another. This is an issue since different devices or material parameters are affected by different defects or combinations of defects, e.g., different microstructures and occupying different energy levels in the band gap.

The deposition of energy in a solid by one incident radiation particle is usually expressed as the product of the probability, per atom, that an interaction or a reaction will occur, and the amount of energy that will be deposited if the interaction does occur. For non-ionizing energy deposition, the interactions are divided into two types: elastic and inelastic. Elastic interactions or collisions are those in which the final energy of the interacting particles, i.e., incident particle and recoiling target atom in the solid, is the same as the initial energy and the interacting particles are not altered. Inelastic interactions, on the other hand, involve the production of a nuclear reaction that not only can make the final energy different from the initial energy (it will be larger if the nuclear reaction is exothermic and smaller if it is endothermic), but it also can make the types of particles emitted from the reaction different from those initiating it. When the particles emitted from a nuclear reaction are different than those initiating it, the reaction is often called a transmutation reaction. Furthermore, if the incident energy is high enough, the number of particles emitted from the reaction can even be larger than two, the number involved in the initial interaction.

For non-ionizing energy deposition per incident particle, the product of the cross section per atom and the energy produced from an interaction can be written as:

$$DE = (\sigma_{el})(T_{el}) + (\sigma_{inel})(T_{inel}) \quad , \quad (4.1)$$

in MeV-cm²/atom per incident particle, where:

σ_{el} is the total elastic scattering cross section per atom (cm²). Elastic scattering can be due either to the Coulomb force or to the nuclear force. Because of quantum interference effects, the cross sections for these two processes cannot be simply added together but must be summed first as probability amplitudes.

T_{el} is the average recoil energy resulting from the elastic collision that goes into non-ionizing energy. The energies of the original recoils that went into ionization must, therefore, be taken into account in order to arrive at the average non-ionizing energy. The recoil energies are corrected for the amount of energy that goes into ionization according to the theory of Lindhard *et al.* (1963).

σ_{inel} is the total inelastic scattering cross section per atom.

T_{inel} is the average recoil energy resulting from the inelastic scattering, corrected for the amount that goes just into non-ionizing energy.

For pure Coulomb interactions or Rutherford scattering, analytic formulas exist (Seitz and Koehler, 1956) from which the average recoil energy can be obtained. When both elastic and inelastic processes are significant, the average recoil energy must be obtained by integrating the relevant differential cross sections over all angles of scattering and averaging over the resultant recoil energy spectrum. At high incident energies, nuclear reactions can contribute a wide range of product nuclei, each with its own cross section, types of emitted particles, and its own recoil energy spectrum. Each type of mass and recoil energy spectrum will, in turn, result in its own average recoil energy mass.

The quantity DE is called the non-ionizing kerma (kinetic energy released in matter) factor and is defined as the sum of the initial kinetic energies of all the particles liberated in a volume element containing a unit mass of the specified material. Thus, it is thus analogous to the absorbed ionization dose. DE has been calculated for neutrons of various energies incident on silicon. A table of these DE values may be found in ASTM (1991).

4.3.3 Conversion of Kerma Factor to Non-Ionizing Energy Loss

If the kerma factor DE is multiplied by the number of atoms per gram, then it is converted to MeV-cm²/g per incident particle; it is this latter

quantity that has the dimensions of energy loss and has been called the non-ionizing energy loss (NIEL). Thus, NIEL, for a specific material, is given by

$$\text{NIEL} = DE(N_0/\text{GMWT}) , \quad (4.2)$$

in MeV-cm²/g per incident particle, where N_0 is Avogadro's number (6.022×10^{23} atoms per mol) and GMWT is the gram atomic weight of the material in question.

NIEL and DE depend on the material being irradiated, the type of particle incident on the material, and on the energy of that particle. For neutrons N of energy E on silicon (Si), a better notation for NIEL would thus be

$$\text{NIEL}(E,N,\text{Si}) = DE(E,N,\text{Si}) \times N_0/\text{GMWT}(\text{Si}) , \quad (4.3)$$

in MeV-cm²/g per incident particle.

A more physical meaning for NIEL can be obtained by noting that for 1-MeV neutrons, an ASTM standard value (ASTM, 1991) exists for the kerma factor $DE(1,N,\text{Si})$, equal to 95 MeV-mb (1 mb = 10^{-27} cm²). For silicon, GMWT = 28.085; thus, $\text{NIEL}(1,N,\text{Si}) = 2.04 \times 10^3$ or 2,040 MeV-cm²/g. This is the amount of non-ionizing energy that a single 1-MeV neutron would deposit in a 1-g/cm²-thick layer of silicon.

4.3.4 Conversion of Non-Ionizing Energy Loss to Displaced Atoms

The quantity NIEL is the amount of energy lost to the primary knock-on atoms (PKAs), corrected for the amount that has gone into ionization. The actual quantity of interest, however, is not NIEL but the number of initially displaced atoms in the material. The conversion of NIEL to initial displacement damage produced in a material requires a model for the translation of the PKAs into displaced atoms. Several models have been proposed, the one most commonly used one being that of Kinchin and Pease (1955), according to which the number of initially displaced atoms (ND) per g/cm² per incident particle is given by

$$\text{ND}(E,P,\text{Si}) = \text{NIEL}(E,P,\text{Si}) / (2 \times E_d) , \quad (4.4)$$

where the P is the particle incident on the silicon, and E_d is the threshold energy required to displace an atom from its site in the solid; for silicon, germanium, and gallium arsenide. Thus, to continue with the previous example, a single 1-MeV neutron will produce the following number of initially displaced atoms in a 1-g/cm²-thick layer of silicon:

$$\text{ND}(1,N,\text{Si}) = 2,040/50 = 40.8 . \quad (4.5)$$

The linear proportionality between NIEL and displacement damage effects, observed for many kinds of incident particles, makes it possible to compare the displacement damage effectiveness of such particles in a given device and under fixed conditions simply by comparing their NIEL values. Table 4-1 gives the NIEL values for neutrons, electrons, protons, and deuterons incident on silicon. Thus, for example, for a given bipolar transistor and injection current, a 20-MeV proton will produce 2.78 times as much device parameter degradation due to displacement damage as will a 1-MeV neutron [(5.68/2.04), see Table 4-1]. Caution needs to be exercised with extrapolations to higher energies for devices with such small sensitive volumes that the range of the PKAs starts to become comparable to the dimensions of the sensitive volume.

4.4 Displacement Damage Effects on Semiconductor Electrical Properties

The effects of radiation-induced defect centers caused by irradiation on semiconductor lattice structure impact its electrical properties. The existence of the forbidden bandgap in a semiconductor is a consequence of the periodicity of the lattice. Any defect will disrupt the periodicity of the lattice, giving rise to a localized state in the bandgap. Figure 4-11 illustrates five different effects that can be caused by localized states in different parts of the bandgap.

First, levels near midgap serve as thermal generation centers for electron/hole pairs, leading to increased dark currents in circuits. Thermal generation of electron-hole pairs is the simultaneous emission of a free electron to the conduction band E_C and a free hole to the valence band E_V from the defect level. It can also be viewed as

Table 4-1. Calculated values ($\times 10^{-3}$) of NIEL (E,P,Si) for neutrons, electrons, protons, and deuterons incident on silicon ($\text{MeV}\cdot\text{cm}^2/\text{g}$ per particle).^a

Particle Energy (MeV)	Neutrons	Electrons	Protons	Deuterons
1	2.04	0.025	87.8	184
2	3.79	0.047	44.7	100
3	3.06	0.062	30.1	68.5
5	4.17	0.081	18.2	43.2
7	3.66	0.094	13.2	31.8
10	4.21	0.108	9.29	23.0
15	4.64	0.125	6.70	16.9
20		0.136	5.68	13.5
50		0.174	4.06	7.36
75		0.190	3.41	6.26
100		0.203	2.97	5.66
150		0.220	2.54	5.14
200		0.232	2.37	4.91
250		0.240	2.28	4.75

Note:
^aBoxed numbers pertain to text example.

the thermal excitation of an electron from the valence band to the defect level, followed by its subsequent emission to the conduction band. This latter viewpoint is useful in emphasizing the importance of midgap levels to this kind of process, since the probability of the excitation process depends exponentially on the energy separation of the defect level from the valence and conduction bands. Charge generation dominates over recombination processes only when the carrier concentration is below the equilibrium value, as occurs most commonly in depletion regions. Displacement-induced dark-current generation in sensors and leakage currents in diodes are two examples of this effect (Summers, 1992).

Second, other localized states lying in the midgap region can serve as recombination centers, shortening minority-carrier lifetimes and reducing the gain in bipolar transistors. In recombination, a carrier of one sign is first captured at the defect center and, before re-emission, a carrier of the opposite sign is also captured, leading to recombination. Recombination is especially important in determining minority-carrier lifetime τ . Radiation-induced defects tend to

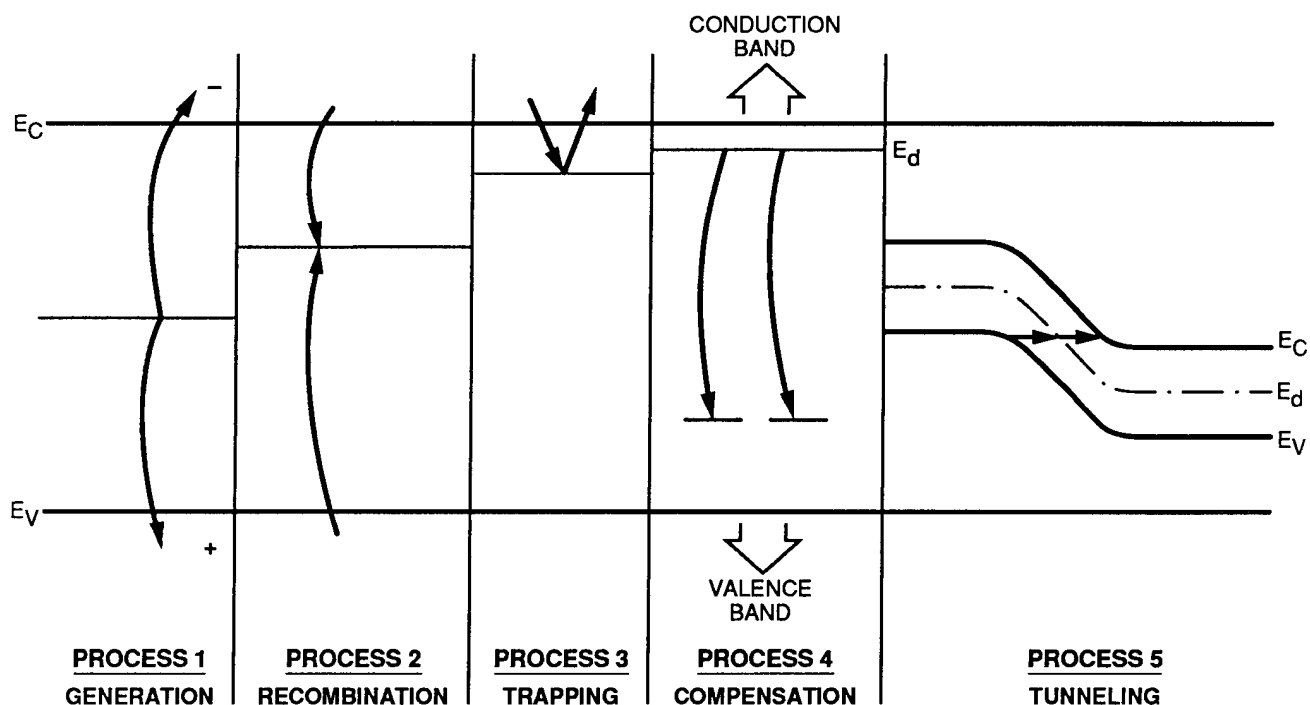


Figure 4-11. Five effects that can occur due to the presence of defect centers in forbidden bandgap (Srour, 1982).

reduce τ . The recombination rate depends on several factors, including the defect density, the capture cross section, the carrier concentration, and the position of the defect level in the bandgap (Summers, 1992).

Third, shallow trap levels near the band edges can trap charges temporarily, re-emitting them in response to thermal excitation. Carrier trapping is the process whereby a carrier is temporarily captured and then released to the same band before recombination or any other process occurs. Both majority and minority carriers can undergo trapping, but at different levels. Trapping is the mechanism that is exploited in deep-level transient spectroscopy. Carrier trapping reduces the charge transfer efficiency in charge-coupled devices (CCDs) (Summers, 1992).

Fourth, deep radiation-induced trap levels can compensate the majority carriers, leading to the carrier-removal process. In the example in Figure 4-11, deep acceptors compensate the donors near the band edge. In compensation, radiation-induced defects introduce deep trap levels that effectively reduce the majority-carrier concentration by introducing carriers of the opposite sign. In radiation effects, this process is also called carrier removal, affecting device characteristics that depend on carrier concentration (such as resistivity). In silicon, irradiation eventually drives all material intrinsic because of the location of the highly effective double-vacancy center at the center of the gap (Summers, 1992).

Fifth, tunneling can occur directly from the valence band to the conduction band in a junction with heavily doped p- and n-regions. Such a device is called a tunnel junction. The tunneling can be greatly enhanced by the presence of a radiation-induced defect level in the junction region, producing defect- or trap-assisted tunneling (Summers, 1992). Trap-assisted tunneling can lead to increased junction leakage current when a carrier tunnels halfway through a barrier to a trap state. Two short tunneling steps are much more likely than a particle tunneling all the way through the barrier.

A sixth effect is possible [not shown in Figure 4-11] wherein defects can act as scattering cen-

ters, leading to the reduction of carrier mobilities. Figure 4-12 illustrates the relative sensitivity of minority-carrier lifetime, carrier concentration, and mobility to neutron irradiation. For bipolar devices, minority-carrier lifetime reduction is the most important effect. The longer the initial lifetime is, the more sensitive the devices are, as illustrated by curves in Figure 4-12 for 10-msec and 10-nsec initial lifetimes. Even with the shorter initial lifetime of 10 nsec, significant lifetime reduction would be expected by a total neutron fluence of a few times 10^{12} n/cm². For metal-oxide semiconductor (MOS) and GaAs devices, on the other hand, minority carriers do not play a significant role. For these devices, carrier removal and mobility reduction are the most important neutron irradiation effects. These effects become significant only at 10^{14} to 10^{15} n/cm², or even higher levels.

Displacement damage effects on the physical properties of semiconductor material can be grouped into three important categories: lifetime damage, carrier removal, and mobility degradation. Most of the initially produced vacancy interstitial atom pairs recombine almost immediately; some additional annealing then takes place in times ranging from about a microsecond to tens of minutes, and beyond at reduced rates. The surviving vacancy interstitial pairs develop

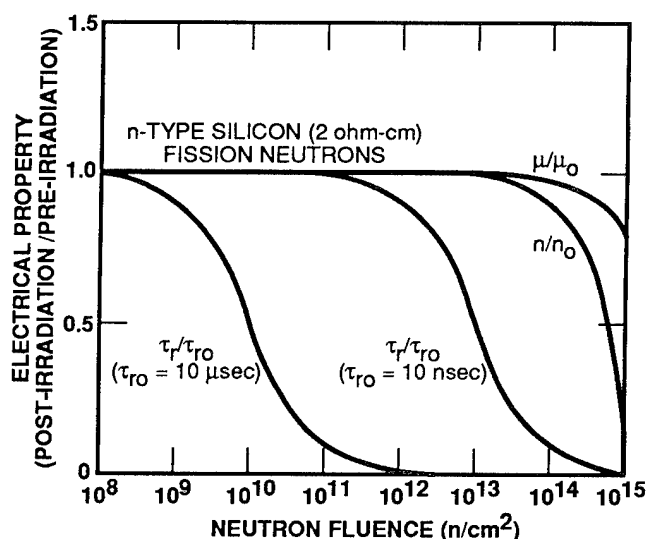


Figure 4-12. Relative sensitivity of lifetime, carrier concentration, and mobility to neutron bombardment (Srouf, 1982).

into permanent defects and produce permanent effects on the properties of the semiconductor material. The defects are observed as trapping sites or energy levels in the semiconductor bandgap. For microelectronics, the fluences of most importance, with respect to displacement damage effects, are lifetime damage and carrier removal. In silicon material [the main focus of this chapter], the important defects are all associated with vacancies; no direct effects from interstitial atoms have been observed. Also in silicon, carrier lifetime is the quantity most sensitive to displacement damage; electronic devices whose characteristics depend on carrier lifetime will therefore be the ones most sensitive to displacement effects.

4.4.1 Recombination Lifetime Effects

Fast neutrons (i.e., those with energies from ~10 keV to 10 MeV), as well as gamma rays and electrons, produce changes in minority-carrier lifetime in semiconductor material. The incident particles cause defects (trapping sites), which act as efficient recombination centers and are stable at room temperature.

The trapping sites important for lifetime reduction are usually shallow; i.e., their energy levels are just inside the forbidden bandgap near the conduction band edge for donor-type traps and just inside the valence band edge for acceptor-type traps. Because the minority-carrier lifetime decreases with the irradiation fluence, the inverse lifetime (sec^{-1}) for a material (silicon) may be written as:

$$1/\tau = 1/\tau_i + \Phi(E,P)/K_\tau \quad , \quad (4.6)$$

where τ_i is the initial (unirradiated) lifetime (in silicon), $\Phi(E,P)$ is the fluence of particles of type P and energy E (in units of particles per cm^2) and K_τ is the material minority-carrier lifetime damage constant (particle-sec/ cm^2). It may be of interest to note that $\Phi(E,P)$ times the quantity $ND(E,P,Si)$, given by Equation 4.4, is the number of initially displaced atoms per gram of silicon. The damage constant K_τ is a function of particle type, particle energy, material type, material resistivity or doping level, injection level and temperature.

Various models exist to analyze the effects of defects on minority-carrier lifetime. However, one model depicts the many actual trapping levels as two or three discrete energy levels and has been used with reasonable success (Messenger, 1967). Based on this discrete model, for a two-level approximation, Equation 4.6 can be rewritten as

$$1/\tau_1 + 1/\tau_2 = 1/\tau @ \Phi_n/K_\tau \quad , \quad (4.7)$$

where τ_1 and τ_2 are the lifetimes that characterize the two-recombination-center energy-level model and it is assumed that $\tau \ll \tau_i$, where τ_i is the unirradiated lifetime and Φ_n is the neutron fluence in n/cm^2 .

Based on the Shockley-Read recombination model, it has been shown (Messenger and Ash, 1992) that the minority-carrier single-level lifetime can be expressed as

$$\tau = \frac{n_0 + n_1 + \delta n}{(n_0 + p_0 + \delta n)N_c C_p} + \frac{p_0 + p_1 + \delta n}{(n_0 + p_0 + \delta n)N_c C_n} \quad , \quad (4.8)$$

where

- n_0, p_0 = equilibrium values of electron and hole concentrations
- δn = excess carrier density
- N_c = density of recombination centers
- C_p = hole capture probability of the recombination center
- C_n = electron capture probability of the recombination center.

The hole ($N_c C_p$) and electron ($N_c C_n$) lifetimes are equal to τ_p^{-1} and τ_n^{-1} , respectively. As an aside, since in most cases of interest $\delta n, p_0 \ll n_0$, Equation 4.8 can be rewritten as

$$\tau \cong p_1 \tau_n / n_0 + (1 + n_1 / n_0) \tau_p \quad , \quad (4.9)$$

where p_1 and n_1 are the steady-state non-equilibrium concentration of holes and electrons, respectively. Moreover, if $n_1, p_1 \ll n_0$, then $\tau \cong$

τ_p , which implies that the steady-state lifetime for the capture of holes is the minority-carrier lifetime. For this reason, the recombination time is also called minority-carrier lifetime.

For the two-level model, $1/\tau = 1/\tau_1 + 1/\tau_2$ and, using Equation 4.8, yields the two-level expression for the mean lifetime as

$$\tau^{-1} = \sum_{k=1}^2 \left[\frac{n_o + n_k + \delta n}{(n_o + p_o + \delta n) C_{pk} N_c} + \frac{p_o + p_k + \delta n}{(n_o + p_o + \delta n) C_{nk} N_c} \right] \quad (4.10)$$

$$\cong \Phi_n K_\tau ,$$

where C_{nk} and C_{pk} are the respective capture probabilities for energy levels E_k for $k = 1, 2$. As defined earlier, $N_c = N \langle \sigma_c \rangle \Phi_n$; then, for a k -level system, $R_k = N \langle \sigma_{ck} \rangle$ is the introduction rate of recombination centers per unit neutron fluence for levels for $k = 1, 2$. Rewriting Equation 4.10 then gives the sought-after relation for the damage constant K_τ as a function of carrier concentration, from which its dependence on resistivity and other material parameters of interest will be obtained,

$$K_\tau^{-1} = \left(2.8 \times 10^{-8} \right)^{-1} + \sum_{k=1}^2 \left[\frac{n_o + n_k + \delta n}{(n_o + p_o + \delta n) C_{pk} R_k} + \frac{p_o + p_k + \delta n}{(n_o + p_o + \delta n) C_{nk} R_k} \right]^{-1} , \quad (4.11)$$

which essentially corresponds to a three-level model, with two levels implied in the summation; the additional numerical term provides a third, midband level with a lifetime of 2×10^{-8} second, introduced to account for the midband levels to provide a more accurate fit to experimental data (Ricketts, 1972).

As mentioned earlier, the damage constant K_τ embodies dependencies on the resistivity of both n- and p-type semiconductors, injection levels, and temperature.

The recombination model [Equation 4.11] can be rewritten in terms of n-type and p-type materials at low injection levels. Let K_{tn} and K_{tp} be values of the damage constant K_τ at low injection levels (particles-sec/cm²). In the limit for small δn and p_o , the results are:

$$K_{tn}^{-1} = \frac{C_{p1} R_1}{1 + n_1/n_o} + \frac{C_{p2} R_2}{1 + C_{p2} p_2 / C_{n2} n_o} . \quad (4.12)$$

Similarly, in the limit of small δn and n_o

$$K_{tp}^{-1} = \frac{C_{p2} R_2}{1 + p_2/p_o} + \frac{C_{n1} R_1}{1 + C_{n1} n_1 / C_{p1} n_o} . \quad (4.13)$$

A comparison of calculated versus experimental results is shown in Figures 4-13 and 4-14. The values of recombination center parameters determined by least-squares fit to silicon, low-level lifetime, damage constant data are listed below (Curtiss, 1966):

$$\begin{aligned} R_1 C_{p1} &= 0.37 \times 10^{-6} \text{ cm}^2/\text{sec} \\ R_1 C_{n1} &= 0.40 \times 10^{-5} \text{ cm}^2/\text{sec} \\ R_2 C_{p2} &= 0.68 \times 10^{-5} \text{ cm}^2/\text{sec} \\ R_2 C_{n2} &= 0.76 \times 10^{-6} \text{ cm}^2/\text{sec} \\ n_1 &= 2.0 \times 10^{14} \text{ cm}^{-3} \\ p_2 &= 1.3 \times 10^{13} \text{ cm}^{-3} . \end{aligned}$$

From these values, the damage constants can be expressed as

$$K_{tn} = 10^5 \frac{(1.4 + 0.086\rho + 0.0012\rho^2)}{(1 + 0.038\rho)} , \quad (4.14)$$

$$K_{tp} = 10^5 \frac{(2.1 + 0.18\rho + 0.0009\rho^2)}{(1 + 0.014\rho)} , \quad (4.15)$$

where r is the resistivity (ohm-cm).

The damage constant is a monotonically increasing function of resistivity, increasing rapidly for low injection levels and becoming almost independent of resistivity at very high injection levels. For low injection levels, K_{tn}^{-1} and K_{tp}^{-1} are asymptotic to

$$\lim_{p \rightarrow 0} K_{tp}^{-1} \equiv K_{tn}^* \equiv C_{p1}R_1 + C_{p2}R_2 \quad (4.16)$$

$$\lim_{n \rightarrow 0} K_{tp}^{-1} \equiv K_{tp}^* \equiv C_{n1}R_1 + C_{n2}R_2 \quad (4.17)$$

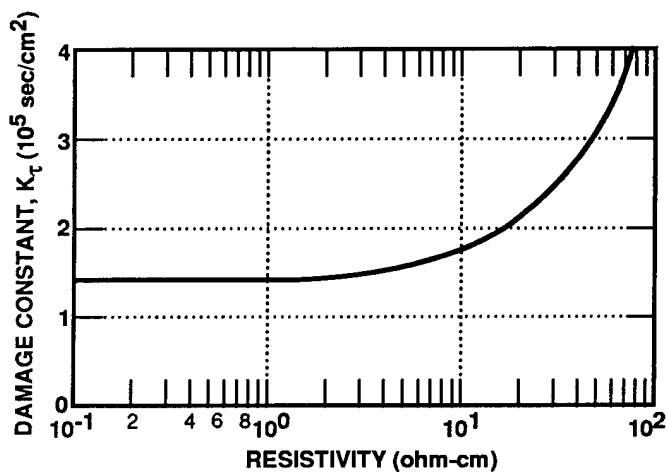
In terms of the injection ratios, $\delta n/n_0$ and $\delta p/p_0$, the damage constant for both n- and p-type silicon as a function of resistivity comprises a one-parameter family of curves for various injection ratios and is shown in Figure 4-15 [parameter values are listed following Equation 4.13, above].

In addition, the temperature dependence of the damage constants can be introduced into Equation 4.12 through the parameters,

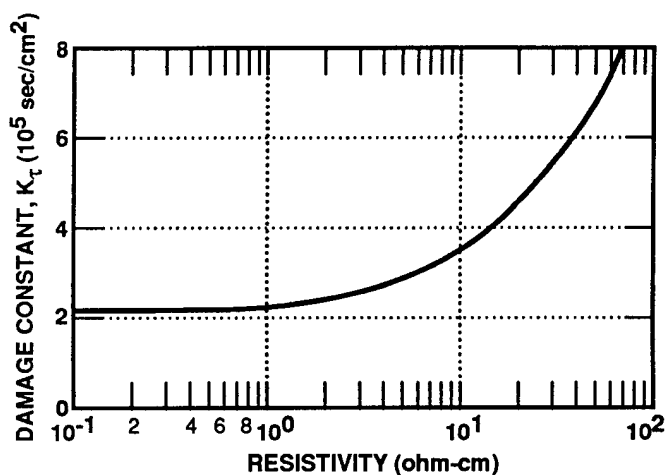
$$n_1 = AT^{3/2} \times \exp -(E_C - E_1)/kT$$

and

$$p_2 = BT^{3/2} \times \exp -(E_V - E_2)/kT \quad ,$$

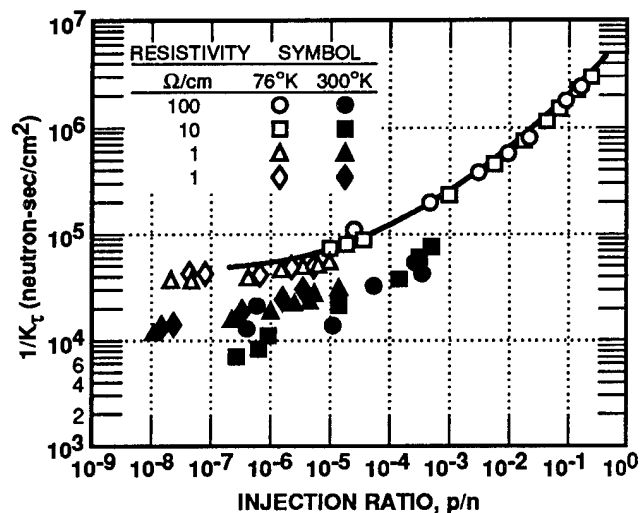


(a) n-Type Silicon

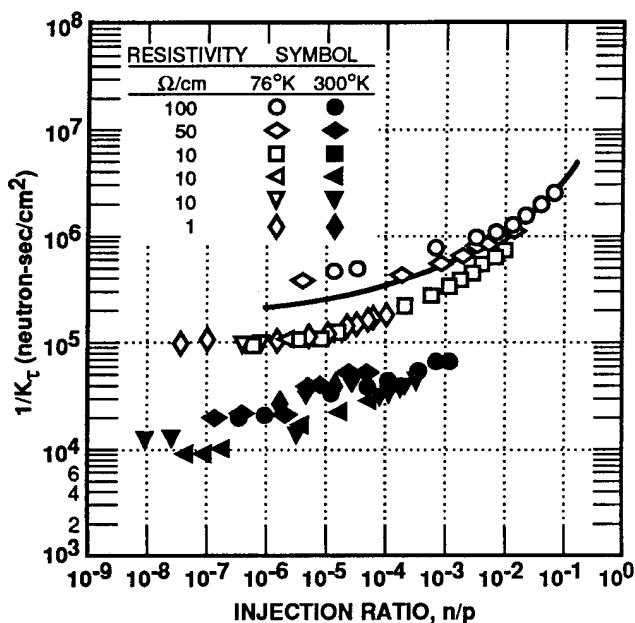


(b) p-Type Silicon

Figure 4-13. Damage constant versus resistivity (Curtiss, 1966).



(a) n-Type Silicon, $K_{\tau}^{-1} = 4 \times 10^4 + 5.8 \times 10^6 (p/n)^{0.534}$



(b) p-Type Silicon, $K_{\tau}^{-1} = 2.5 \times 10^5 + 5.6 \times 10^6 (n/p)^{0.395}$

Figure 4-14. Injection dependence of lifetime damage constant in silicon of various resistivities at 76°K and 300°K (Larin, 1968).

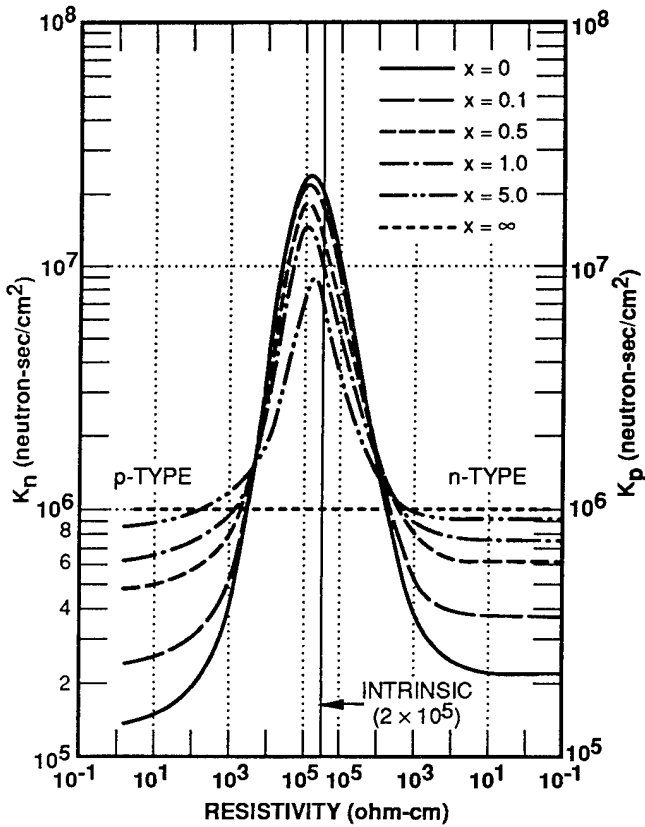


Figure 4-15. Damage constants K_n and K_p versus resistivity for various injection ratios ($x = d_n/n_0$, p/p_0 , $r_n = 5 \times 10^{15}/n_0$, $r_p = 2.5 \times 10^{16}/p_0$) (USSR, 1979).

and the equilibrium values n_0 and p_0 are assumed temperature-independent. This is a weak restriction, corresponding to the temperatures over which the dopant recombination centers are fully ionized, as most are ionized at room temperature (Alexander *et al.*, 1969; Messenger, 1967).

An empirical relationship has been developed (Van Valkenberg, 1965) for the excess current carrier density δn as a function of a bipolar transistor emitter current density, J_E :

$$\delta n = \frac{(A_1 J_E^2 + A_2 J_E)}{(A_3 J_E + 1)}, \quad (4.18)$$

where A_1 , A_2 , and A_3 are fitting coefficients. Inserting this relationship into Equation 4.11 yields

$$K_\tau = 1.23 \times 10^6 \left[1.68 - (194 J_E^2 + 7,700 J_E + 5,309/J_E^3 + 313 J_E^2 + 6,280 J_E + 3,410) \right] \quad (4.19)$$

A plot of the results of this equation versus measured data is shown in Figure 4-16.

For high current densities, the increase in the damage constant can be accounted for by adjusting the base resistance in the equivalent circuit. K_τ can also change with dc supply voltage (V_{CC}) and corresponding unity gain transistor bandwidth frequency (f_T), as given by

$$K/K_{V_{CC0}} = (V_{CC}/V_{CC0})^n \quad (4.20)$$

$$= f_{TV_{CC}}/f_{TV_{CC0}},$$

where the zero subscripted quantities refer to their values at a known nominal operating point; n is determined from experiment and usually lies between 0.2 and 0.5.

The combined effects of neutron irradiation and temperature on bipolar transistor common-emitter current gain β (h_{FE}) are discussed here to illustrate the role of K_τ on β (h_{FE}) in terms of the physical parameters of the transistor. A relationship for bipolar transistors between β (h_{FE}) and K_τ is provided by Messenger and Spratt (1958) for the common emitter gain degradation as:

$$\Delta(1/\beta) \equiv 1/\beta - 1/\beta_i = \Phi / (\omega_T \times K_\tau), \quad (4.21)$$

where

$\beta(h_{FE})$ = irradiated common emitter gain

β_i = unirradiated common emitter gain

ω_T = gain bandwidth product of the transistor ($2\pi f_T$) (sec^{-1})

Φ = neutron fluence (neutrons/ cm^2)

K_τ = damage constant (particle-sec/ cm^2).

A more complete expression for $\beta(h_{FE})$, including low-level current effects (e.g., recombination in the emitter-base depletion region and

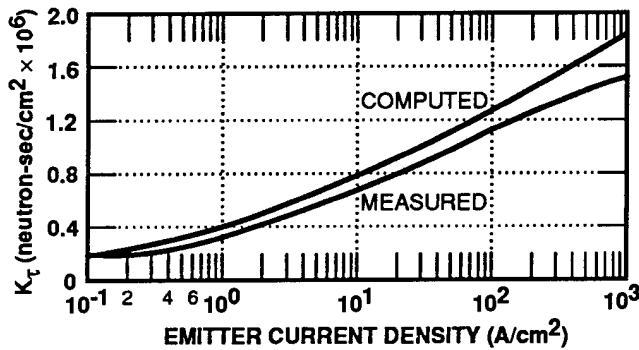


Figure 4-16. Measured and computed damage constant K_τ versus emitter current density (USSR, 1979).

surface recombination effects in regions of the base where the depletion layer has been formed near the surface) is given by:

$$\beta^{-1} = \left(\frac{W^2}{2D_B\tau} \right) + \left(\frac{\sigma_B W}{\sigma_E L_E} \right) + \left(\frac{SA_s W}{A_E D_B} \right) + \left(\frac{WN_B}{2D_B n_i} \right) \left(\frac{W_{EB}}{\tau_D} + \frac{SA'_s}{A_E} \right) \quad (4.22)$$

$$\times \exp \left(-\frac{eV_{BE}}{2kT} \right),$$

where

- W = base width (cm)
- D_B = base diffusion constant (cm²/sec)
- τ = base minority-carrier lifetime (seconds)
- σ_B, σ_E = base and emitter conductivity, respectively (mhos)
- L_E = emitter diffusion length (cm)
- S = surface recombination velocity (cm/sec)
- A_s = effective surface recombination area (cm²)
- A_E = emitter area (cm²)
- N_B = base dopant concentration (cm⁻³)
- n_i = intrinsic carrier concentration (cm⁻³)

High-injection (high-current) phenomena, e.g., conductivity modulation and current crowding, are neglected in Equation 4.22.

The first term of Equation 4.22 is due to recombination in the base region, the second term is due to current injection in the emitter, the third represents surface effects in the nonspace-charge region, and the last term represents recombination in the emitter-base depletion region and low-level surface effects.

The second term on the right-hand side of Equation 4.22 is called the emitter injection efficiency term. Neutrons have little effect on this term because of the small value of the pre-irradiation minority-carrier lifetime. Also, L_E varies only with the inverse square root of the neutron fluence because $L_E^2 = D\tau_E$ and $\tau_E \sim 1/\Phi_n$.

Modern bipolar transistors, except for high-voltage devices, are generally fabricated with narrow base widths, e.g., $\leq 3 \mu\text{m}$, to enhance operating speed. These transistors are manufactured using high-purity silicon with electron lifetimes of $\sim 10 \mu\text{sec}$ and hole lifetimes of $\sim 1 \mu\text{sec}$. This leads to the overall gain of the transistor (β) being dominated by the emitter efficiency term since the first term of Equation 4.22, $W^2/(2D_B\tau)$, ≤ 0.01 for these parameters.

For relatively low levels of fluence and moderate gain and temperature changes, the following equation can be used:

$$\Delta(1/\beta) = \Phi_n / (\omega_T K_\tau)$$

$$-\beta_0^{-1} \left[1 - \frac{1}{(1 + \Delta T/T_0)^2} \right]. \quad (4.23)$$

This equation may be extended to high fluence levels and temperature ranges by fitting the temperature variation of the damage constant $K_D = 1/(\omega_T K_\tau)$ in the Messenger-Spratt equation [Equation 4.21] to the two- or three-level defect model previously discussed. This fit is given by (Messenger, 1979)

$$K_D(T) = K_D(T_0) \left[1.1 - 0.1(T/T_0)^4 \right], \quad (4.24)$$

where $K_D(T)$ is the temperature-dependent constant in $\text{cm}^2/\text{neutron}$.

As an aside, for a uniformly heavily doped emitter transistor, the current gain is approximately equal to

$$\beta(T) \equiv (D_E/D_B) \exp - (\Delta E_g/kT) . \quad (4.25)$$

This expression can be written to permit β versus temperature comparisons as

$$\beta(T) = \beta(T_0) \times \exp - \left[\Delta E_g (kT) (1/T - 1/T_0) \right] . \quad (4.26)$$

For small $\Delta T/T$, Equation 4.26 yields

$$1/\beta \equiv [1/\beta(T_0)] (T/T_0)^{-M} , \quad (4.27)$$

where

$$M = \Delta E_g/kT \cong 1.6 \text{ for } T = 300^\circ\text{K} \text{ (} kT = 0.025 \text{ eV).}$$

Further simplifications of Equation 4.22 are possible. For the situation where the transistor is operated at moderate collector currents and near maximum gain, the following relationship can be used (Messenger, 1979):

$$\beta^{-1} \cong \beta_0^{-1} (T_0/T)^M + K_D(T) \Phi_n \left[1.1 - 0.1(T/T_0)^4 \right] . \quad (4.28)$$

To use this formula, the room-temperature gain β_0 must be known. $K_D(T_0)$ is obtained from radiation test data or estimated from $K_D = 1/(\omega_T K_\tau)$, where a universal damage constant $K_\tau = 1.6 \times 10^6$ is employed. The value of M given for Equation 4.27 can also be used.

Finally, an approximate conservative expression for the gain degradation is obtained by assuming a temperature dependence for K_D like that for the emitter-efficiency term and incorporating low current/surface effects through an empirical constant a , giving

$$\beta^{-1} \cong \beta_0^{-1} (T_0/T) + K_D(T) \Phi_n (T/T_0)^a , \quad (4.29)$$

where $a \cong 1.5$, as obtained from experimental data. A successful experimental program was conducted to verify these gain formulas (Messenger, 1979).

When a transistor is subjected to neutron exposure, the first term of Equation 4.22 increases as

$$W^2/2D\tau = W^2/2D\tau_0 + K_D\Phi_n , \quad (4.30)$$

and similarly for the surface recombination velocity,

$$S = S_0 + K_S\Phi_n . \quad (4.31)$$

K_S is a surface damage constant ($\text{cm}^3/\text{sec-n}$) that depends on the particular device, including its manufacturing processing. Also,

$$S_0 = \sigma_c v_{th} N_{st} , \quad (4.32)$$

where N_{st} is the surface trap density, the thermal velocity $v_{th} \sim T^{1/2}$, and σ_c is the surface trap cross section. The temperature dependence of the remaining term of Equation 4.22 is obtained by using the intrinsic carrier density n_i given by

$$n_i(T) = T^{3/2} \exp - (E_g/2kT) . \quad (4.33)$$

Combining the previous equations for a transistor in which surface recombination can be ignored produces (Messenger, 1979)

$$\beta^{-1} = (\sigma_B W / \sigma_E L_E) (T_0/T)^M + \left[K_D(T) \Phi_n + (W^2/2D_0\tau) (T/T_0) \right] \times \left[1 + A(T/T_0)^r \right] , \quad (4.34)$$

where

$$r = (E_g - eV_{BE}) / 2kT_0 - 3/2 ,$$

and

$$A = (W_{EB}\tau/W\tau_D)(N_B/n_o) \\ \times \exp\left(-\frac{eV_{BE}}{2kT_o}\right) .$$

Values of M range from 1 to about 1.6 and r ranges from 4 to 8. Equation 4.34 can be simplified to

$$\beta^{-1} = \beta_o^{-1}(T/T_o)^M \\ + \left\{ K_D(T)\Phi_n \left[1 + A(T_o/T)^r \right] \right\} \quad (4.35)$$

so that for bipolar collector currents below the maximum gain operating point, and for heavy initial neutron exposure, either Equation 4.34 or 4.35 is valid.

4.4.2 Carrier Removal Effects

Defects caused by displacement damage can remove charge carriers from the conduction process. The discussion here will focus on n-type material; however, it is equally applicable to p-type material, in which case "donor" should be replaced with "acceptor."

The increase in resistivity produced in n-type silicon is explained principally through the introduction of divacancy and donor-vacancy defect complexes, the formation of which are caused by incident neutrons. These defect complexes deplete the conduction band of its electrons (majority carriers) by capturing them. This decrease in the conductivity of the semiconductor (increases in its resistivity) is called carrier removal.

The important trapping energy states, as determined experimentally by electron paramagnetic resonance (EPR) methods, are at $E_C - 0.55$ eV (corresponding to the divacancy defect complex with a single electron charge), $E_C - 0.40$ eV (for the divacancy defect complex with a double electron charge), and $E_C - 0.40$ eV (for the single negatively charged donor-vacancy defect complex). E_C is the energy level at the bottom of the conduction band.

A closed expression that relates particle fluence to resistivity can be derived (Messenger and Ash, 1992) is as follows

$$\rho_{n,p} = \rho_i \exp\left(\Phi_n/k_{n,p}\right) , \quad (4.36)$$

where $\rho_{n,p}$ is the resistivity due to electrons (n) and holes (p), ρ_i is the pre-irradiation resistivity, and k_n and k_p are empirically determined constants (n/cm^2).

The analogous empirical expression for the majority-carrier concentration is

$$n = n_i \exp\left(-\Phi_n/k_n\right) . \quad (4.37)$$

An initial carrier-removal rate can be defined as

$$n \cong n_i(1 - \Phi_n/k_n) \\ \cong n_i - \Phi_n(dn/d\Phi_n) , \quad (4.38)$$

where dn is the change in electron density.

Assuming stoichiometric mass action laws hold, for low fluence levels where $N_V \cong K_V \times \Phi_n$ and n-type material (which includes only donor and oxygen vacancies), a series of equations can be written and solved to provide resistivity as a function of fluence, as follows:

$$N_{DV} = K_{DV} N_D N_V \quad (4.39)$$

$$N_D = N_{Di} - N_{DV} \quad (4.40)$$

$$N_{OV} = K_{OV} N_O N_V \quad (4.41)$$

$$N_O = N_{Oi} - N_{OV} \quad (4.42)$$

$$N_V = K_V \Phi_n - N_{DV} - N_{OV} \quad (4.43)$$

where

- N_V = vacancy concentration
- N_{DV} = concentration of donor-vacancy complexes
- K_{DV} = rate coefficient of donor-vacancy complex formations
- N_D = donor concentration
- N_{Di} = initial donor concentration
- N_{OV} = concentration of oxygen vacancy complexes
- K_{OV} = rate coefficient of oxygen-vacancy complex formations

- N_O = oxygen atom impurity concentration
 N_{O_i} = initial oxygen atom impurity concentration
 K_V = rate coefficient of vacancy production
 Φ_n = neutron fluence (n/cm²).

Equations 4.39 through 4.43 may be combined to yield

$$\begin{aligned}
 N_{DV} &= \frac{K_V K_{DV} N_{Di} \Phi_n}{(1 + K_V K_{DV} \Phi_n)} \\
 N_{OV} &= \frac{K_V K_{OV} N_{O_i} \Phi_n}{(1 + K_V K_{OV} \Phi_n)}.
 \end{aligned} \quad (4.44)$$

The electron density can then be written as (Messenger and Ash, 1992)

$$\begin{aligned}
 n &= N_{Di} \frac{(1 - K_V K_{DV} \Phi_n)}{(1 + K_V K_{DV} \Phi_n)} \\
 &\quad - \frac{N_{O_i} K_V K_{OV} \Phi_n}{(1 + K_V K_{OV} \Phi_n)}.
 \end{aligned} \quad (4.45)$$

The corresponding initial carrier-removal rate is obtained from Equation 4.45 as

$$\lim_{\Phi_n \rightarrow 0} n(\Phi_n) = K_V (2K_{DV} N_{Di} + K_{OV} N_{O_i}) \quad (4.46)$$

The resistivity is given as

$$\rho = (e \mu_n n)^{-1} = \rho_i n_o / n(\Phi_n), \quad (4.47)$$

where ρ_i is the unirradiated resistivity, $n(\Phi_n)$ is the electron density as a function of fluence Φ_n , μ is the electron mobility, and e is the electronic charge. Using Equation 4.45 in Equation 4.47 yields the resistivity as a function of fluence,

$$\begin{aligned}
 \rho &= \rho_i \frac{1 + (K_{DV} + K_{OV}) K_V \Phi_n}{\left[K_{DV} - K_{OV} \left(1 - \frac{N_{O_i}}{N_{Di}} \right) \right] K_V \Phi_n} \\
 &\approx \rho_i \exp(2K_{DV} K_V \Phi_n),
 \end{aligned} \quad (4.48)$$

where the initial ratio of oxygen atoms to donor atoms, N_{O_i}/N_{Di} , is assumed very small. This exponential behavior of resistivity with neutron fluence correlates well with the Beuhler (1958) data. These expressions are given as

$$\rho_n = \rho_{n_o} \exp(\Phi_n / K_n) \quad (4.49a)$$

and

$$\rho_p = \rho_{p_o} \exp(\Phi_p / K_p), \quad (4.49b)$$

where ρ_{n_o} and ρ_{p_o} are the initial resistivities (ohm-cm²) for n- and p-type material, respectively, and F_n is the fluence of 1-MeV silicon displacement-damage equivalent neutrons (particles/cm²). The carrier removal constants are

$$K_n = 444 n_o^{0.77} \quad (4.50a)$$

and

$$K_p = 387 p_o^{0.77}, \quad (4.50b)$$

where n_o and p_o are the majority-carrier concentrations (n/cm²) for n- and p-type material, respectively. The results of this work are shown in Figures 4-17 and 4-18.

An approximate expression for resistivity at low fluence levels is

$$\rho = \frac{\rho_i}{1 - \frac{K_1 \Phi_n}{N_{Di}} - \frac{2K_{DV} \Phi_n}{(1 + K_{DV} \Phi_n)}} \quad (4.51)$$

where $K_1 = 0.7 \text{ cm}^{-1}$, and $K_{DV} = 1.2 \times 10^{-17} \text{ cm}^2$.

It should be noted that the factors in Table 4-1 can be used to convert the 1-MeV neutron carrier-removal constants to other particles or neutron energies using the relationship

$$K(E,P,Si) = \frac{NIEL(1,N,Si)}{NIEL(E,P,Si)} \times K(1,N,Si), \quad (4.52)$$

where $K(E,P,Si)$ is the carrier-removal constant for particles of type P and energy E (MeV) incident on silicon (particles/cm²), $NIEL(E,P,Si)$

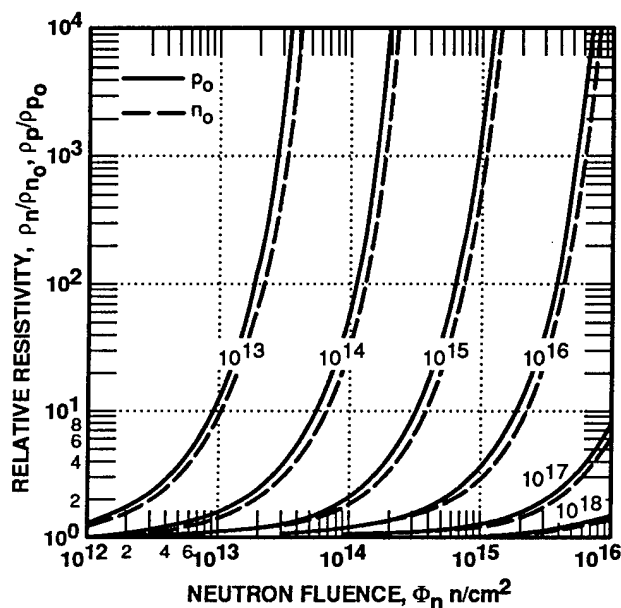


Figure 4-17. Resistivity relative to the pre-irradiation level of n - and p -doped silicon versus neutron fluence for various dopant densities (Beuhler, 1958).

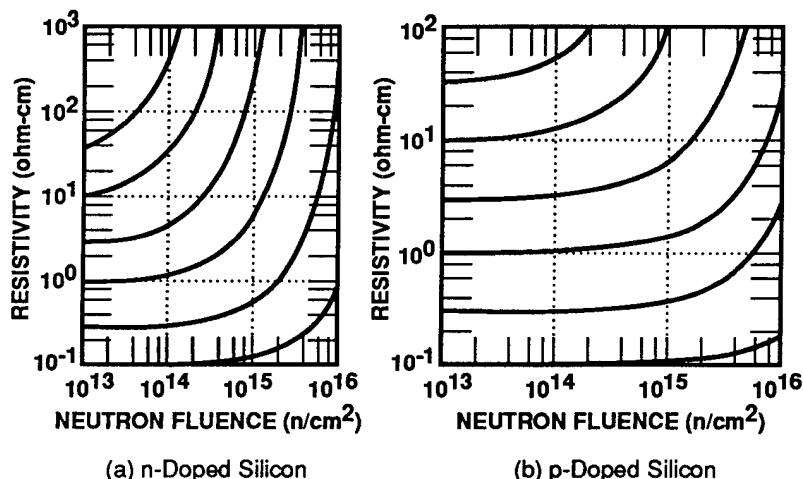


Figure 4-18. Exponential resistivity-fluence dependence in silicon normalized to its assumed pre-irradiation value of 10^{13} (Beuhler, 1958).

is the value given in Table 4-1 for these same particles, $NIEL(1,N,Si)$ is the value in Table 4-1 for 1-MeV neutrons on silicon, and $K(1,N,Si)$ is the carrier-removal constant for 1-MeV silicon displacement damage equivalent neutrons on silicon (particles/cm²).

4.4.3 Annealing

Annealing is the spontaneous post-radiation recovery of a transistor wherein parameters that have shifted in value due to the effects of radiation-induced displacement damage return to their original values (or close to them). Annealing occurs over a wide range of temperatures. Because vacancies and interstitial atoms are not stable at room temperature, many of the initial vacancy interstitial defects will recombine at room temperature. The initial defects that survive will migrate, due to thermal activation, to lattice impurities where they form associations, i.e., defects and defect complexes, which are stable at room temperature. These defects can then be trapping sites for charge carriers. As this migration and stable-defect formation proceeds in time, there follows an accompanying change in device characteristics. Annealing is the term given to the sum total of all the processes by which the initial displacement damage in the crystal becomes permanent.

4.4.3.1 Annealing in Semiconductor Materials

In silicon, about 90 percent or more of the initially produced vacancy interstitial pairs recom-

bine $\sim 10^{-10}$ second after the collision cascade has occurred. It seems probable that a large part of this initial and extremely rapid recombination is geminate recombination; i.e., the interstitial atom recombines with the vacancy it has just created. It is also probable that this geminate recombination is not thermally activated or at least that the temperature of the crystal is not an important factor in the amount of recombination that takes place.

During annealing, impurities and lattice defects can play an important role because many of the thermally stable defects are associations between these and radiation-induced defects. For the same reason, the annealing process can lead either to improvement or degradation in the properties of the irradiated material because the stable defect can be more or less effective than the unstable defects in changing a particular property. Examples are known in which one property improves while another degrades in the same sample.

Annealing processes, in general, can be very complicated because they involve interactions of a number of different species of defects, as, for example, mobile defects produced by the radiation and defects already present in the parent material. However, some simple cases can be used to illustrate the important elements of the process (Damask and Dienes, 1963).

The simplest case is the random motion of defects to a fixed number of sinks whose number does not change appreciably during the anneal. This case is called a first-order process and is described by an exponential relaxation of the mobile-defect concentration,

$$MD = MD_0 \exp(-t/\tau) \quad , \quad (4.53)$$

where MD_0 is the initial number of mobile defects and τ is the mean lifetime of the defect. τ is related to the diffusion coefficient (D) for the mobile defects, and an effective sink surface area Σ by

$$\tau = \Sigma/D \quad . \quad (4.54)$$

The diffusion coefficient also depends on the energy barrier to migration E_B , the vibrational

frequency with which an atom strikes the barrier νf_0 , the lattice constant ℓc , and a constant Γ , nearly equal to 1, determined by geometry,

$$D = \Gamma \ell c^2 \nu f_0 \exp(-E_B/kT) \quad , \quad (4.55)$$

where k is Boltzmann's constant and T is the temperature in degrees Kelvin. The most important feature of these formulas is that τ increases exponentially with reciprocal temperature at a rate determined by the barrier energy. An example of a first-order anneal is the motion of vacancies in silicon toward a much larger concentration of interstitial oxygen atoms.

Another case of importance is second-order annealing, in which the concentration of mobile defects equals the concentration of sinks during the anneal, for example, interstitial-vacancy recombination where both species are randomly distributed. (Recombination of a vacancy with its own nearby interstitial can be first order since the number of interstitials available for any particular vacancy remains constant during the anneal; i.e., equal to one.) In this case,

$$\frac{1}{MD} = \frac{1}{MD_0} + \tau Z \nu f_0 \exp(-E_B/kT) \quad , \quad (4.56)$$

where Z is the number of sites near the sink from which immobilization is certain. This decay is hyperbolic, but the same exponential dependence on reciprocal temperature is evident.

In silicon at room temperature, the simplest defects (interstitials and vacancies) move to immobilization sites, and all the permanent damage is associated with defect clusters (Corbett, 1966; Watkins, 1968). The vacancies in p-type silicon (neutral charge state) have an activation energy for migration E_B of 0.33 eV and have been found to move during an isochronal anneal at a temperature of about 170°K. The vacancies in n-type silicon (negative charge state) have been found to move in an anneal temperature of 60°K, implying an activation energy for the negative charge state $E_B < 0.16$ eV. Some evidence exists supporting interstitial movement at 4°K in p-type silicon, although no evidence for defects result-

ing from interstitial interactions at room temperature is available. The simplest intrinsic defect (one in which only silicon is involved) stable at room temperature is the divacancy. Most of the other identified stable defects are associations of vacancies with impurities (vacancy with interstitial oxygen forming substitutional oxygen, vacancy with phosphorus donor, etc.).

It can be seen from the exponential dependence of relaxation times on reciprocal temperature that, for a spectrum of defects with different activation energies E_B , a variety of annealing times can be expected. As a practical matter, it is convenient to separate the behavior at a particular temperature into three components: (1) the stable component, (2) the short-term annealed component, and (3) the prompt annealed component. The separation among these components depends somewhat upon the measured property and the time scale of the measurement. The short-term component is the one whose annealing covers the time scale of importance to the measurement, the prompt anneal is complete before this time scale, and the stable component undergoes no changes. Since the measurement encompasses faster time resolution and longer time periods, more of the damage is presumably included in the short-term anneal component.

Since excess-carrier lifetime is a sensitive and important parameter for semiconductor devices, it has been used extensively to diagnose the extent of displacement damage and its annealing. Simple theory predicts that τ should be proportional to the density of the recombination centers. In bipolar transistors, simple theory also predicts that $1/h_{FE}$ should be proportional to $1/\tau$, where h_{FE} is the common-emitter current gain. [This is true only for bipolar transistors in which the current gain is limited by minority-carrier transport across the base. For unirradiated high-frequency devices, the emitter efficiency or the depletion-layer recombination generation current, and not the minority-carrier lifetime, dominates the current gain.] Similarly, in solar cells (photodiodes), the short-circuit current I_{SC} , under constant illumination with penetrating ionizing radiation, is proportional to the square root of τ .

Short-term annealing in response to neutron irradiation has been investigated in silicon transistors, solar cells, and bulk silicon and germanium (Binder and Butcher, 1967; Harrity and Mallon, 1967; Harrity, van Lint, and Poll, 1965; Sander and Gregory, 1971). The transient annealing data are normally presented in terms of an annealing factor $F(t)$, which compares the sum of stable plus annealed components with the stable components. The anneal factor is defined as

$$F(t) = \left[\frac{1/\tau(t) - 1/\tau(0)}{1/\tau(\infty) - 1/\tau(0)} \right], \quad (4.57)$$

where $\tau(t)$ is the minority-carrier lifetime at a time t following a pulsed nuclear explosion, $\tau(0)$ is the minority-carrier lifetime prior to the irradiation, and $\tau(\infty)$ is the stable minority-carrier lifetime after irradiation.

4.4.3.2 Annealing in Bipolar Transistors

Annealing in bipolar transistors has been described in terms of an annealing factor $F(t)$ and is expressed as (Gregory and Sander, 1970)

$$F(t) = \left[\frac{h_{FE}^{-1}(t) - h_{FE}^{-1}(0)}{h_{FE}^{-1}(\infty) - h_{FE}^{-1}(0)} \right], \quad (4.58)$$

for $F(t) > 1$ and $F(\infty) = 1$; where $h_{FE}(t)$ is the common-emitter current gain of the transistor at time t after irradiation, $h_{FE}(0)$ is the pre-irradiation gain, and $h_{FE}(\infty)$ is the stable common-emitter gain after irradiation. A typical annealing factor response for a bipolar integrated circuit is shown in Figure 4-19. Equation 4.58 can be rewritten as

$$h_{FE}(t) = \left(\frac{h_{FE}(0)}{1 + F(t) \left\{ \frac{h_{FE}(0)}{[h_{FE}(\infty)] - 1} \right\}} \right), \quad (4.59)$$

for $t_p \leq t \leq \infty$, where t_p is the neutron pulse duration.

One of the most significant factors affecting annealing in silicon bipolar transistors (Harrity and Mallon, 1967; Harrity, van Lint, and Poll, 1965) is the electron density level within the active region of the device. Figure 4-20 depicts this effect, following a succession of neutron bursts at the repetition rate shown. The rapid annealing characteristic shown in Figures 4-20 and the slow, high temperature annealing shown in Figure 4-21 is known as isothermal annealing, i.e., annealing at a single temperature. This can be contrasted to isochronal annealing shown in Figure 4-22.

Another significant factor that affects the annealing characteristic of a bipolar transistor is the bias state, as defined by the base-emitter bias (V_{BE}). As can be seen from Figure 4-23, the worst case for gain degradation occurs when the transistor is biased OFF ($V_{BE} = 0$), when $F(t_p)$ is about 25. Thus, from Equation 4.59, where $h_{FE} \cong h_{FE(\infty)}/F(t)$ when $h_{FE(0)}/h_{FE(\infty)} \cong 1$, the gain of the transistor is about 4 percent of its post-anneal value immediately after irradiation. Such behavior is partially attributed to nascent vacancies produced immediately after the neutron pulse. Additionally, it can be inferred from Figure 4-23 that operating a transistor biased ON can minimize post-irradiation performance degradation.

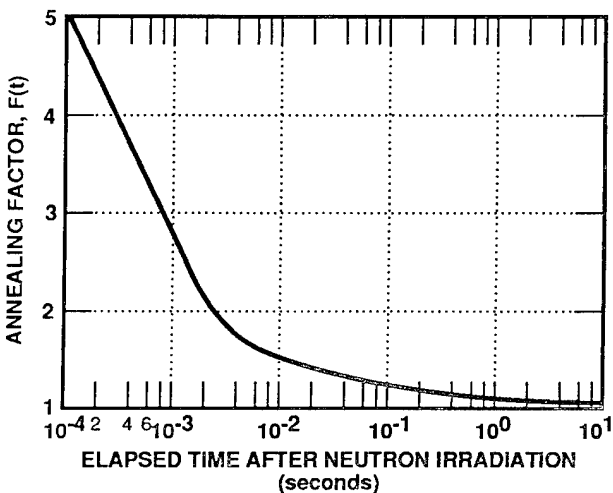


Figure 4-19. Typical annealing factor for modern integrated circuitry in bipolar transistors subject to neutron fluence (Messenger and Ash, 1992).

In addition to current injection and bias, temperature also has a significant effect on device-annealing characteristics. This is shown in Figure 4-24, which also indicates that gain degradation following a neutron pulse is more severe and recovery less rapid at lower temperatures.

Sander and Gregory (Gwyn, Scharfetter, and Wirth, 1967) devised a short-term annealing nomograph that aids in the determination of the appropriate $F(t)$ for a given situation [Figure 4-25]. It was developed for reactor neutron irradiations and assumes, for the case of transistors, that recombination in the emitter-base space-charge region dominates gain degradation. This assumption holds for high-frequency transistors. The electron density (which determines the annealing rate) is the same for npn and pnp devices at the center of that region for a given base-emitter bias (V_{BE}). In general, to use the nomograph, the electron density must be employed in the region of a device that controls the post-irradiation behavior. [A transistor example is illustrated in Figure 4-25.] An $F(t)$ 10 msec after the burst is ~ 1.6 for a device that is ON ($V_{BE} = 0.65$ volt) during irradiation and during the recovery period. For an OFF device ($V_{BE} = 0$ during irradiation and annealing), an $F(t)$ of ~ 6.5 is indicated at that same time. Once a device that is OFF during irradiation is turned ON, recovery occurs rapidly.

4.4.4 pn Junction Leakage

In general, pn junction reverse leakage current is increased by displacement damage effects,

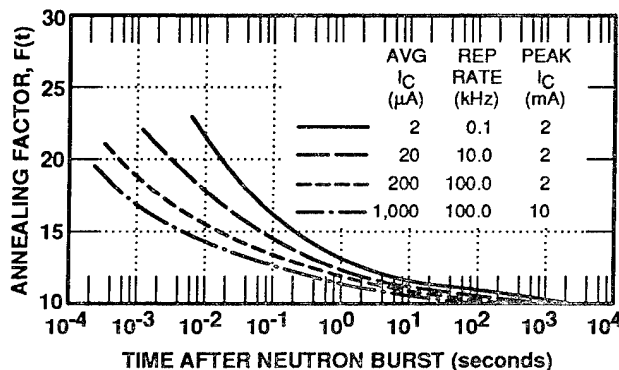


Figure 4-20. Annealing factor versus time after neutron irradiation for various injection levels and repetition rates (Gregory and Sander, 1970).

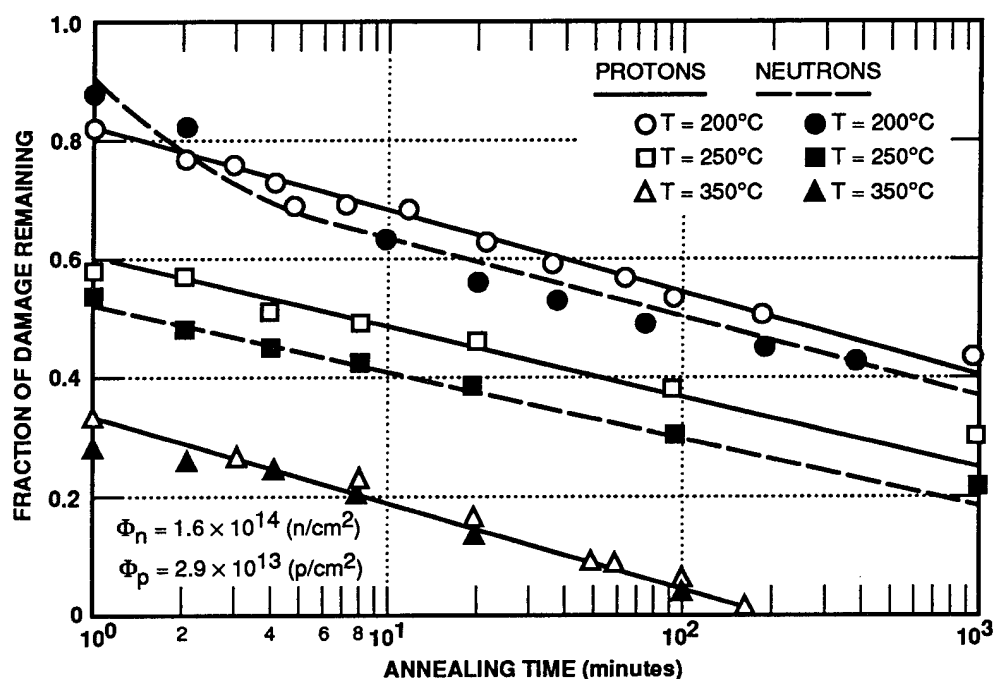


Figure 4-21. Isothermal slow annealing characteristics for typical bipolar transistors (Gregory and Sander, 1970).

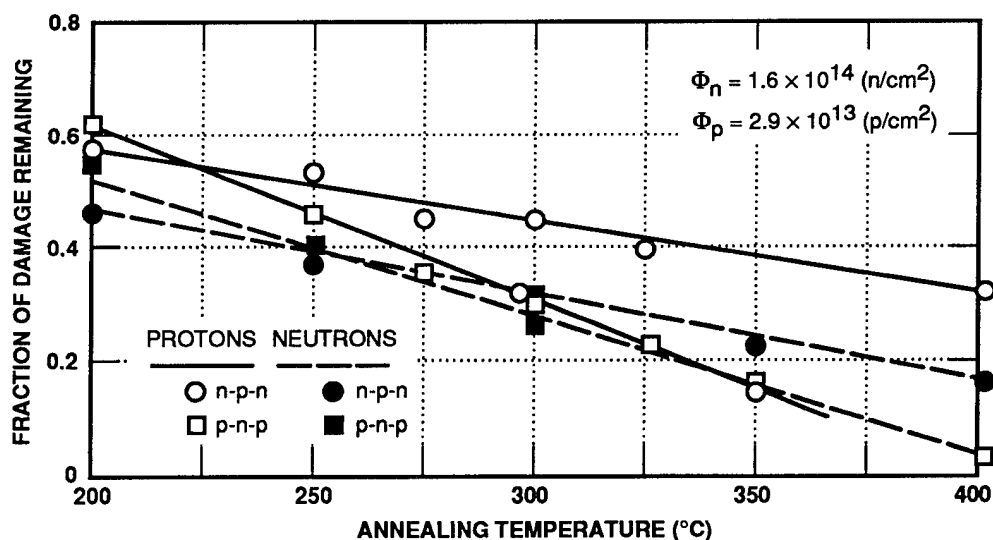


Figure 4-22. Isochronal slow annealing characteristics for typical bipolar transistors; annealing time 20 minutes (Gregory and Sander, 1970).

which increase the thermal carrier generation rate in the pn junction depletion region.

4.4.4.1 Junction Leakage Mechanisms

A manifestation of displacement damage is the creation of generation centers in the pn junction depletion region [see Figure 4-11 and related discussion], which affect the characteristics of reverse-biased junction. The increase in the

thermal generation of electron-hole pairs at the radiation-induced generation centers will increase the reverse leakage current of pn junction when these carriers are swept out by the high electric fields that are present.

Figure 4-11 illustrated five effects that can occur due to the presence of radiation-induced defect centers in the silicon bandgap. Process 1 is

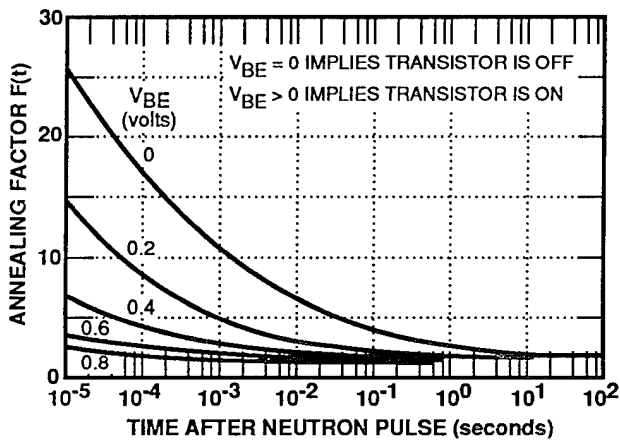


Figure 4-23. Annealing factor versus time after neutron pulse for bipolar transistors for various V_{BE} at room temperature (Sander and Gregory, 1971).

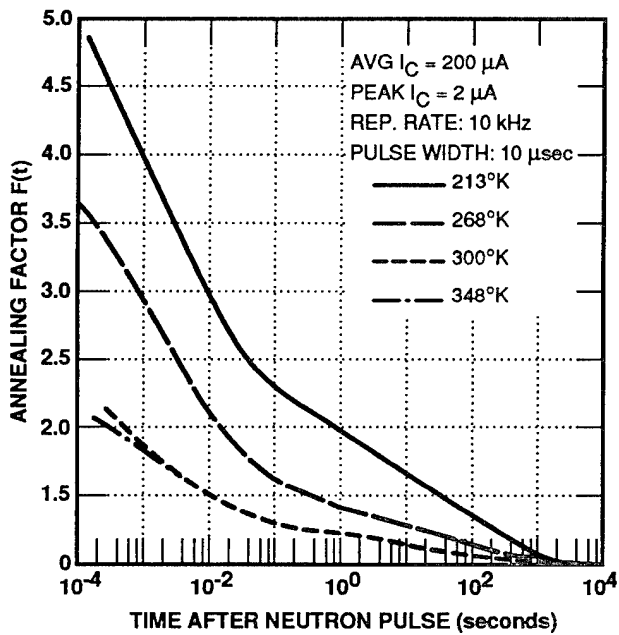


Figure 4-24. Rapid annealing factor for bipolar transistors at various temperatures (Gregory and Sander, 1970).

the thermal generation of electron-hole pairs through a level near midgap. This process can be viewed as the thermal excitation of a bound valence-band electron to the defect center and the subsequent excitation of that electron to the conduction band, thereby generating a free electron-hole pair. Alternatively, it can be viewed as hole emission from the center followed by electron emission. Only centers with an energy level near midgap make a significant contribution to carrier generation; an exponential decrease in generation rate occurs as the energy level position is moved from midgap (Grove, 1967). In addition, emission processes dominate over capture processes at a defect level only when the free-carrier concentrations are significantly less than their thermal equilibrium values. Thus, thermal generation of electron-hole pairs through radiation-induced defect centers near midgap is important in device depletion regions. Introduction of such centers is the mechanism for leakage current increases in silicon devices. [Generation lifetime τ_g is a characteristic time associated with carrier generation in a depletion region; it is used below in the damage coefficient discussion.]

As an aside, leakage currents can also be increased due to generation centers produced at the surface by ionizing radiation. Generation lifetime is characterized by a relationship similar to that used to describe the effects of recombination centers and carrier removal, *viz.*,

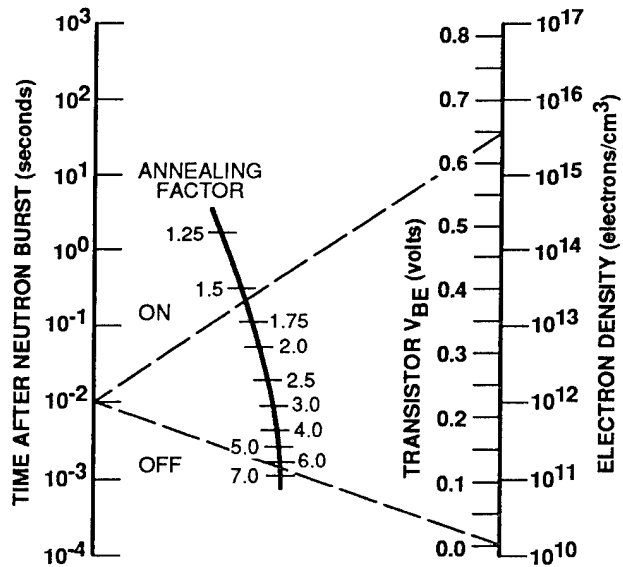


Figure 4-25. Short-term annealing nomograph for fission-neutron-irradiated silicon devices (Gwyn, Scharfetter, and Wirth, 1967).

$$\tau_g^{-1} = \tau_{go}^{-1} + \Phi_n / K_g \quad (4.60)$$

where

- τ_g = post radiation generation center lifetime
- τ_{go} = pre-irradiation generation center lifetime

- K_g = generation center rate (n-sec/cm²,
 $\cong 3 \times 10^6$ n-sec/cm² for 14-MeV
 neutrons in silicon)
 Φ_n = neutron fluence (n/cm²).

In general, K_g is a function of particle type, particle energy, material type, resistivity, impurity species and concentration, injection and level, and temperature.

4.4.4.2 Junction Leakage Equation

The effect of the displacement-damage-induced defects on leakage current can also be deduced from an examination of the basic diode equation (Messenger and Ash, 1992), which can be written in general form as

$$I = A e n_i^2 \left[\left(\frac{D_n}{L_n N_A} \right) \coth \left(\frac{W_p}{L_n} \right) + \left(\frac{D_p}{L_p N_D} \right) \coth \left(\frac{W_n}{L_p} \right) \right] \psi(V_o), \quad (4.61)$$

where

- A is an empirical constant
- e is the electronic charge
- n_i is the initial electron density
- D_n is the electron diffusion constant
- L_n is the minority-electron-carrier diffusion length
- N_A is the acceptor dopant atom density
- W_p is the p-junction depletion-layer thickness
- D_p is the hole diffusion constant
- L_p is the minority-hole-carrier diffusion length
- N_D is the donor concentration
- W_n is the n-junction depletion-layer thickness

and

$$\psi(V_o) = [\exp(e V_o / kT) - 1],$$

where V_o is the applied junction voltage. To obtain the reverse-bias leakage current, we can write $\psi(-V_o) = -1$; thus,

$$-I_I = A e n_i^2 \left[\left(\frac{D_n}{L_n N_A} \right) \coth \left(\frac{W_p}{L_n} \right) + \left(\frac{D_p}{L_p N_D} \right) \coth \left(\frac{W_n}{L_p} \right) \right], \quad (4.62)$$

where I_I is the junction saturation current. For a narrow-base-width transistor, i.e., $W_{n,p} \ll L_{n,p}$ yields

$$-I_{In} \cong A e n_i^2 \left[\left(\frac{D_n}{W_p N_A} \right) + \left(\frac{D_p}{W_n N_D} \right) \right], \quad (4.63)$$

and for a wide-base-width transistor, such as a power device,

$$-I_{Iw} \cong A e n_i^2 \left(\frac{\sqrt{D_n / \tau_n}}{N_A} + \frac{\sqrt{D_p / \tau_p}}{N_D} \right), \quad (4.64)$$

where I_{In} and I_{Iw} are the junction saturation currents for narrow-base-width and wide-base-width transistors, respectively.

The effect of radiation on leakage current can be deduced by recalling $\tau_g^{-1} = \tau_{g0}^{-1} + \Phi_n / K_g$. Thus, if we make the approximation that $\tau_g^{-1} \cong \Phi_n / K_g$, Equation 4.64 can be rewritten as

$$-I_{Iw} \cong A e n_i^2 \frac{\sqrt{D_n \Phi_n / K_g}}{N_A}. \quad (4.65)$$

4.4.5 Mobility Reduction

Radiation-induced defects also act as scattering centers and decreases the carrier mobility. The mobility decreases with increasing ionized impurity concentration. In a similar manner, the introduction of charged radiation-induced defects also causes the mobility to decrease. This effect is stronger at temperatures considerably less than 300°K because ionized impurity scattering dominates over lattice scattering in that regime.

Mobility degradation can be characterized in a manner similar to recombination and generation lifetime generation and is represented as

$$\mu^{-1} \cong \mu_0^{-1} + K_\mu \Phi_n \quad (4.66)$$

where

- μ is the post-irradiation mobility
- μ_0 is the pre-irradiation mobility (V-sec)
- K_μ is the mobility damage constant (V-sec/hr) ($\cong 3 \times 10^{-19}$ V-sec/hr for 2 Ω -cm, n-type and p-type for reactor neutrons)
- Φ_n is the neutron fluence (n/cm²).

Mobility degradation is considered a tertiary effect for bipolar transistors (Gregory, 1969), as opposed to the primary effect of lifetime degradation and the secondary effect of carrier removal/trapping.

4.5 Displacement Damage Effects on Silicon-Based Devices

The effects of radiation-induced displacement damage, primarily caused by neutron irradiation, on a variety of silicon-based semiconductor devices is discussed here. The intent of this section is to build on the theory provided in the previous sections concerning lifetime degradation, carrier removal, etc. The semiconductor devices discussed include a variety of diode types (e.g., signal, reference, microwave, etc.), bipolar and MOS transistors, junction field-effect transistors (JFETS), and both linear and digital bipolar integrated circuits. Figure 4-26 provides approximate thresholds for neutron-induced degradation for a variety of semiconductor technologies. Table 4-2 indicates the relative importance of displacement damage failure mechanisms for several device types.

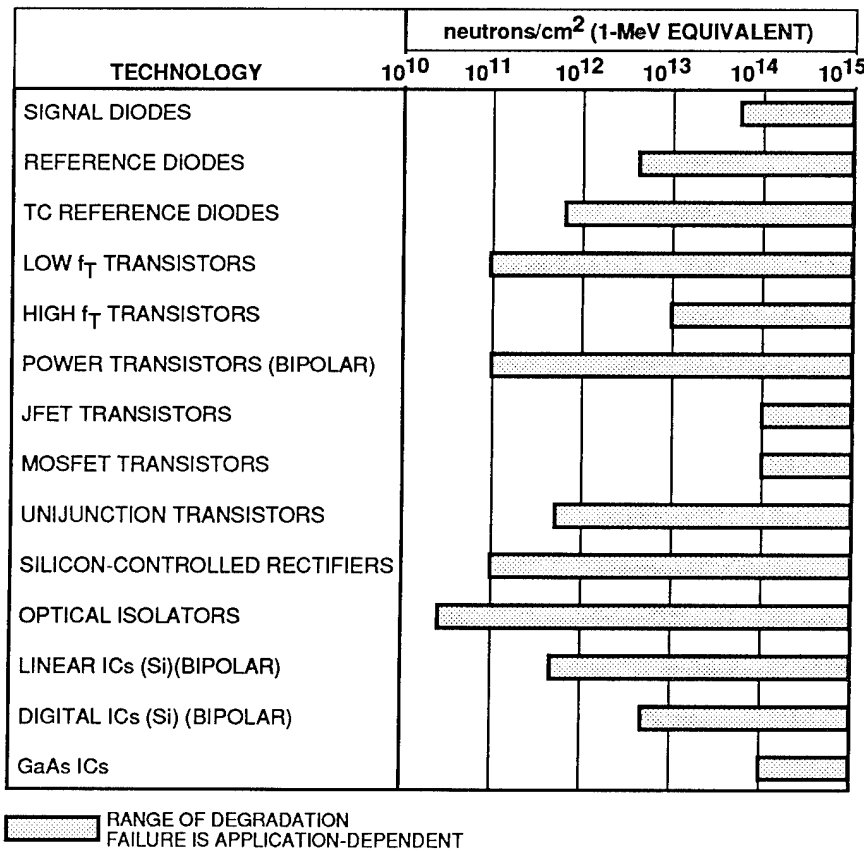


Figure 4-26. Approximate thresholds for neutron-induced degradation in various semiconductor technologies (Messenger and Ash, 1992).

Table 4-2. Failure mechanisms for semiconductor devices (Srou, 1988).

Device Type	Lifetime Degradation		Carrier Removal and Trapping		Mobility Degradation	
	Primary	Secondary	Primary	Secondary	Primary	Secondary
Diode (forward, reference)		X	X			
PIN diode	X					X
Field-effect devices						
(JFET, MOSFET)		X	X ^a			X
Microwave diode sources						
(IMPATT, TRAPATT, BARITT)		X	X			
Microwave bulk oscillators						
(Gunn, LSA)			X			X
Solar cells	X				X	
Bipolar transistors	X				X	
Switching devices (SCR)	X				X	
Optoelectronic devices						
(LED, junction laser)	X				X	

Note:
^a For modern MOSFET designs, device operation may be disrupted by changes in threshold voltage owing to oxide charge or interface state buildup before bulk effects become significant.

4.5.1 Conventional pn Diodes

Neutron damage is manifested as three effects in diodes: (1) a change in the forward voltage V_F , (2) an increase in reverse leakage current I_R , and (3) an increase in reverse breakdown voltage V_{BR} [see Figure 4-27]. The leakage current increases due to increased recombination current in the junction region. This current is usually small at typical neutron levels and for many situations does not affect circuit performance.

Figures 4-28 and 4-29 present scatter plots for normalized changes in V_F and I_R , respectively, where ΔV_F and ΔI_R are the average change in each parameter for the given test sample.

The forward voltage may decrease or increase, depending on the type of diode and the forward current level. At low injection levels, the forward voltage decreases slightly because of decreases in the minority-carrier lifetimes in the p- and n-regions. This change is small and can be neglected in most instances, except possibly

when the forward voltage is used for temperature compensation. At high injection levels, carrier-removal effects will increase the resistivity of the lightly doped region and widen the junction depletion region. At typical neutron levels (e.g., 10^{12} n/cm²), these effects are very small in signal

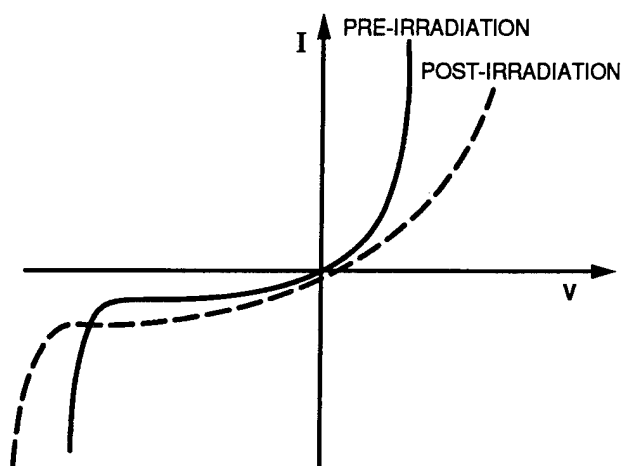


Figure 4-27. Illustrative comparison of pre- and post-neutron voltage-current characteristics of a pn diode (Rose, 1984).

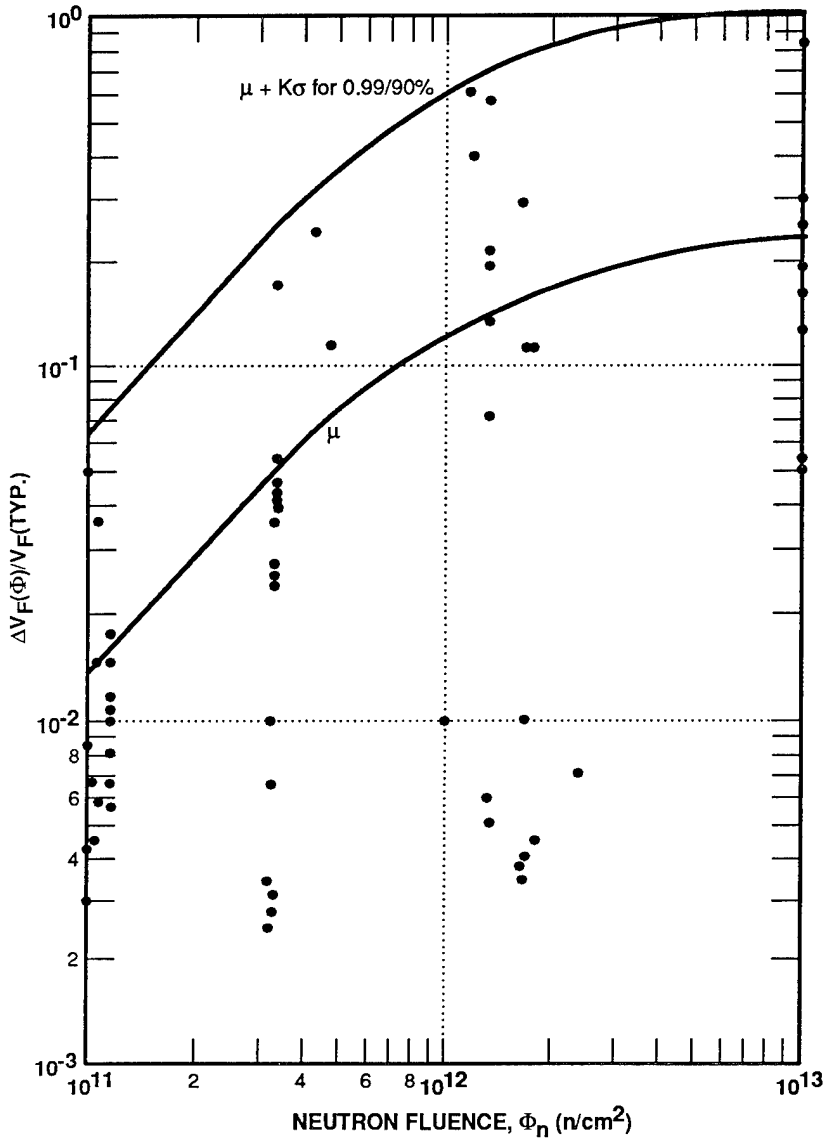


Figure 4-28. Normalized change in forward voltage V_F for rectifying diodes at 25°C versus neutron fluence [$\Delta V_F(F)$ is the average change in forward voltage for the given test sample] (Rose, 1984).

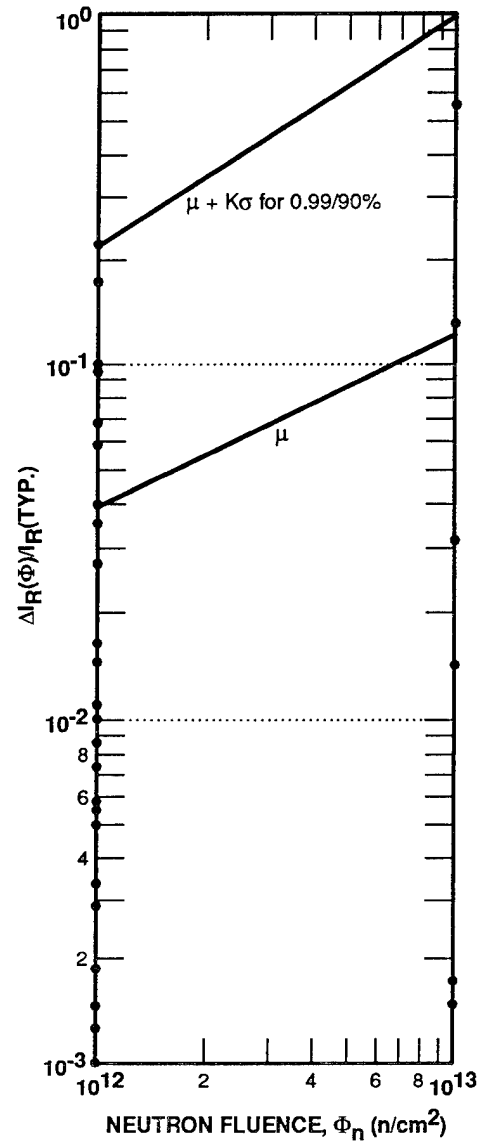


Figure 4-29. Normalized change in reverse leakage current I_R for rectifying diodes at 25°C versus neutron fluence [$\Delta I_R(F)$ is the average change in reverse leakage current for the given test sample] (Rose, 1984).

diodes, but may be important for some power diodes. The increased resistivity may cause objectionable power losses in circuits such as power converters.

4.5.2 Voltage Reference Diodes

The impact of neutron damage on reference diodes that are not temperature-compensated will depend on the breakdown voltage level V_{BR} . For low-voltage devices, which use zener breakdown, V_{BR} will decrease slightly because of increased tunneling current as the traps in the forbidden bandgap increase. For high-voltage devices, which use avalanche breakdown, V_{BR}

increases slightly as the neutron-created trapping sites decrease the effective doping level of the device. The voltage changes for either type of device will be very small. At low neutron levels, the changes will be on the order of 0.1 percent or less. This magnitude of change is usually not serious in most voltage-reference circuits. If the system is to be designed to meet higher neutron levels, the changes may be from 1 to 10 percent, which can be significant in some reference circuits.

For temperature-compensated reference diodes, neutron damage to both the forward- and reverse-biased diodes in the device will occur. The degradation to the forward-biased diode(s) will be the dominant effect and will cause the reference voltage to drop since the diodes are operated at moderately low current levels.

4.5.3 Microwave Diodes

Microwave diodes include pin, IMPATT, TRAPATT, BARITT, and GUNN diodes. These are inherently hard to neutrons, due in part to their small geometry. Prior testing (Chaffin, 1973) shows that typical parts are unaffected up to 10^{14} n/cm². The rf failure of these parts is a function of carrier recombination in the space-charge region; therefore, devices with narrower space-charge regions are more radiation-tolerant. The dc failure for these types of devices is caused by negative temperature coefficient changes, which create thermal instabilities when combined with large reverse breakdown currents. This effect is a function of carrier removal at the space-charge region edges and results in abrupt junction devices being more radiation-tolerant.

4.5.4 Bipolar Transistors

The electrical parameters of transistors that are usually the most sensitive to neutron fluence are the common emitter current gain h_{FE} , the collector-emitter saturation voltage $V_{CE(SAT)}$, the base-emitter voltage V_{BE} , and the collector-base leakage current I_{CBO} . The failure level for a bipolar transistor will vary considerably because of the wide variations in the geometry and doping characteristics of these devices.

Figure 4-30 presents a plot for generic transistor h_{FE} degradation as a function of neutron fluence. From this it can be seen that low-frequency power devices are most vulnerable and that, based on a required 50 percent of initial h_{FE} , generic transistors can fail from $<10^{12}$ n/cm² to $>10^{14}$ n/cm². Neutron hardening of bipolar devices is basically a matter of reducing the dependence of device performance upon minority-carrier lifetime. This is achieved primarily by minimizing the base width, which is also the direction the commercial world is taking to improve device performance. The drive to reduce

device operational voltage also tends to shrink all the transistor dimensions because of the corresponding reduction in required depletion widths; again, the effect is to reduce the base width. The effects of neutrons on bipolar transistor behavior are well characterized, and gain degradation as a function of neutron fluence sufficiently well established, that device derating is an acceptable approach to neutron hardening. The magnitude of the change in h_{FE} is a function of the gain-bandwidth frequency product f_T and a damage constant K . The relationship of these variables is given by the Messenger-Spratt equation (Messenger and Spratt, 1958),

$$\Delta \frac{1}{h_{FE}} = \left[\frac{1}{h_{FE}(N)} - \frac{1}{h_{FE}(0)} \right] = \frac{K\Phi_n}{2\pi f_T} \quad (4.67)$$

where $h_{FE}(N)$ is the degraded gain and $h_{FE}(0)$ is the initial value. As a rule-of-thumb, 0.5- μ m base widths will sustain a 1×10^{14} n/cm² exposure and still permit circuit functionality. As previously discussed, the damage constant K will vary with collector current and type of material, as shown in Figure 4-31. Another important consideration is the initial gain of the device. Figure 4-32 shows the degradation of devices with the same f_T but different gains compared to devices with the same gain but different f_T parameters. It can be seen that high-gain devices degrade more rapidly, but always maintain a higher gain. Table

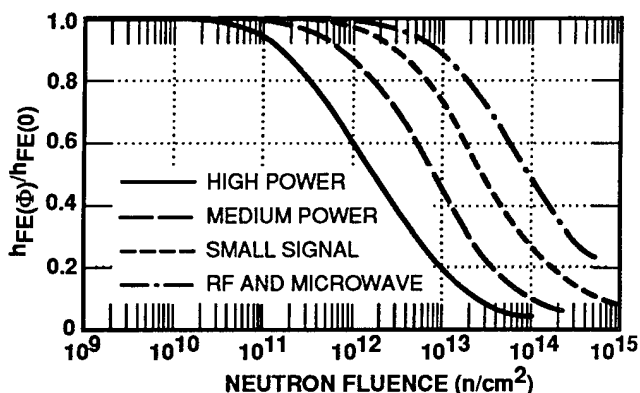


Figure 4-30. Typical gain degradation versus neutron fluence for various types of transistors (Rose, 1984).

4-3 lists a number of device types with different f_T values and the approximate neutron failure levels (assuming 50 percent degradation as an arbitrary failure value). Actual failure levels in circuits will vary somewhat from the tabulated values, but the values do serve to indicate the relative susceptibility of the various device types.

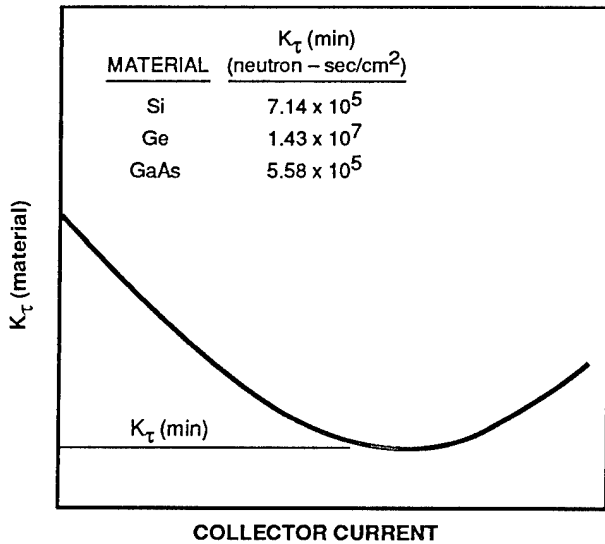


Figure 4-31. Neutron damage factor as a function of collector current and material (Rose, 1984).

In the event actual degraded h_{FE} is not available for the initial design, methods are available for calculating the approximate value. One conservative method, assuming conservative damage constants, utilizes Equation 4.67 to get the calculated h_{FE} degradation, $h_{FE}(\Phi_n)$, for an npn device,

$$\frac{h_{FE}(0)}{1 + \frac{1.3 \times 10^{-7} h_{FE}(0) \Phi_n}{f_T}}$$

and for a pnp device,

$$\frac{h_{FE}(0)}{1 + \frac{1.8 \times 10^{-7} h_{FE}(0) \Phi_n}{f_T}}$$

where $h_{FE}(0)$ is the initial value of gain bandwidth. Another method uses the nomograph shown in Figure 4-33. This nomograph is based on Equation 4.67 for determining the degradation of gain in transistors. To use the nomograph, place a straight edge connecting the values of the gain-bandwidth product and initial gain [Step 1].

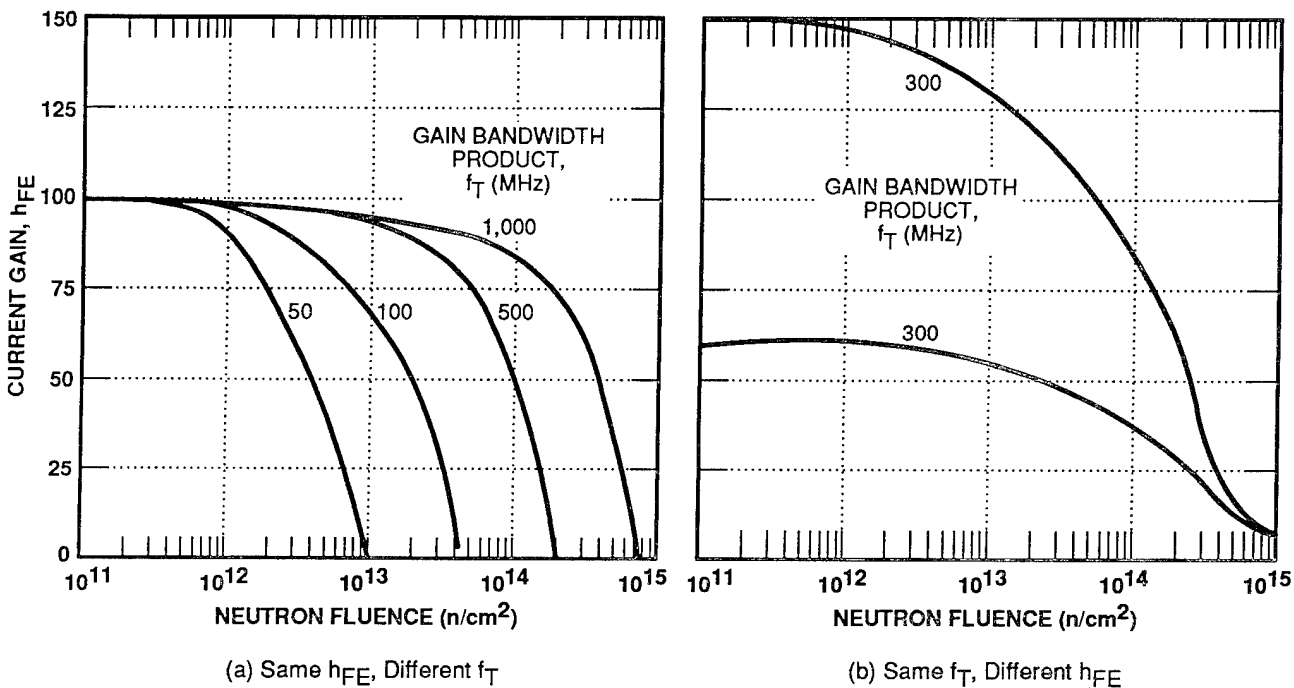


Figure 4-32. Comparison of h_{FE} degradation (Rose, 1984).

Table 4-3. Transistor damage factors and neutron failure levels for 50-percent h_{FE} degradation in silicon devices. (Rose, 1984)

Device Manufacturer	Device Number	Minimum f_T (MHz)	Test Conditions		$K/2 \pi f_T$ Factors	Neutron Failure Level (50 percent β)			
			V_C (volts)	I_C (amperes)					
Low-Power npn									
Texas Instruments	2N1893	50	6	0.1	1.16×10^{-15}	1.2×10^{13}			
			5	0.15	1.42×10^{-15}	1.8×10^{13}			
Motorola	2N2222A	300	10	0.001	7.05×10^{-16}	9.2×10^{12}			
				0.01	3.54×10^{-16}	1.6×10^{13}			
				0.0001	5.26×10^{-15}	2.7×10^{12}			
					5.56×10^{-15}	2.3×10^{12}			
SSD	2N2920	60	3	0.0001	8.03×10^{-16}	2.1×10^{12}			
				0.01	2.25×10^{-16}	5.7×10^{12}			
				0.03	1.77×10^{-16}	6.8×10^{12}			
					1.26×10^{-15}	6.2×10^{12}			
				2N3019	100	10	0.002	1.26×10^{-15}	6.2×10^{12}
							0.05	4.26×10^{-16}	1.3×10^{13}
1.0	8.04×10^{-16}	2.7×10^{13}							
High-Power npn									
SSP	2N2880	50	2	1	2.65×10^{-15}	6.6×10^{12}			
RCA	2N3055	0.3	4	5	1.38×10^{-14}	3.9×10^{12}			
				5	1.88×10^{-14}	4.8×10^{12}			
				10	1.28×10^{-14}	7.9×10^{11}			
				15	9.72×10^{-15}	1.1×10^{12}			
				2N3772	0.2	10	0.5	3.31×10^{-14}	1.7×10^{11}
3	4.24×10^{-14}	2.1×10^{11}							
5	4.94×10^{-14}	2.6×10^{11}							
Texas Instruments	2N5005	70	5	0.05	2.24×10^{-15}	4.8×10^{12}			
				1.0	7.21×10^{-16}	1.1×10^{13}			
Low-Power pnp									
Fairchild	2N2894	400	1	0.0001	1.27×10^{-15}	2.3×10^{13}			
				0.001	5.67×10^{-16}	3.5×10^{13}			
				0.01	2.97×10^{-16}	5.5×10^{13}			
Motorola	2N2905A	200	10	0.001	8.15×10^{-16}	1.0×10^{13}			
				0.01	3.27×10^{-16}	2.0×10^{13}			
				0.1	2.47×10^{-16}	5.0×10^{13}			
Texas Instruments	2N5332	600	5	0.001	5.12×10^{-17}	2.9×10^{14}			
				0.006	2.97×10^{-17}	4.9×10^{14}			
				0.01	2.64×10^{-17}	5.5×10^{14}			
High-Power pnp									
Motorola	2N3467	175	1	0.05	4.66×10^{-16}	3.8×10^{13}			
				0.1	3.42×10^{-16}	4.5×10^{13}			
				0.5	3.94×10^{-16}	4.2×10^{13}			
				0.005	4.16×10^{-16}	4.0×10^{13}			
					1.66×10^{-16}	1.2×10^{14}			
2N5160	500	10	0.05	1.66×10^{-16}	1.2×10^{14}				
			0.3	2.29×10^{-16}	1.0×10^{14}				
Fairchild	2N5153	70	5	0.05	1.97×10^{-15}	4.3×10^{12}			
				1	9.34×10^{-15}	1.2×10^{12}			

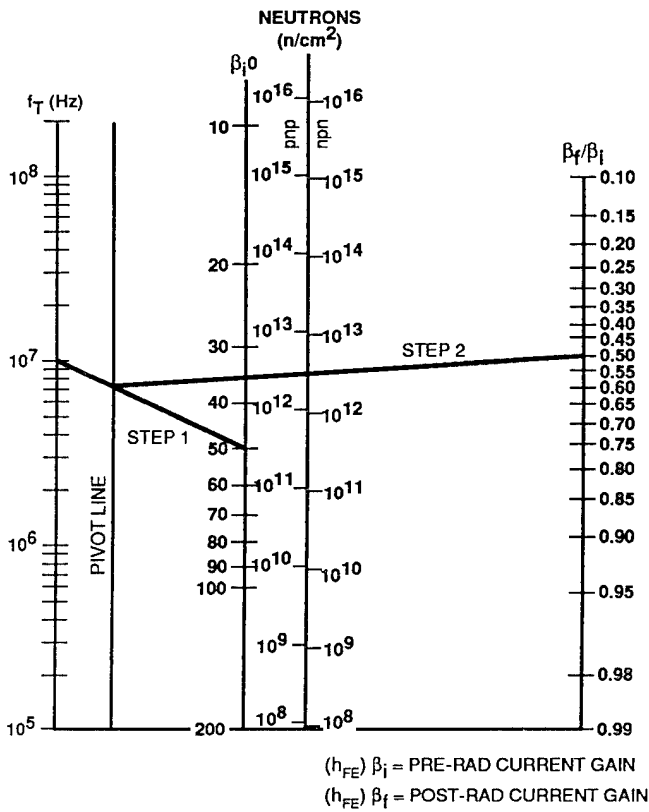


Figure 4-33. Nomograph for calculating approximate h_{FE} degradation values in silicon (Rose, 1984).

Step 1 shows the line for a transistor with an initial f_T of 10^7 and β_i of 50. Mark the intersection of the pivot line. Next, place the straight edge so that it connects the mark on the pivot line and the value of Φ_n for the type of transistor of interest and read the value for β_f/β_i [Step 2]. A note of caution for these methods is that they provide initial approximations *only* and should not be used as the primary data for developing a critical design.

For silicon devices, Equation 4.67 can be written for a large number of transistors as

$$\Delta(1/h_{FE}) = K_D \Phi_n \quad (4.68)$$

where $K_D = 10^{-7}/f_T$, which implies a universal constant of $K_\tau = 1.6 \times 10^6$ n-sec/cm² under nominal operation at or near the peak of the transistor gain with respect to collector current.

As previously discussed, the neutron-induced gain degradation actually has two components. The permanent component was described above. A transient component is shown in Figures 4-34

and 4-35. The transient part of the degradation anneals out rapidly so that the majority of this temporary degradation has disappeared within 1 msec to 1 second after exposure. The annealing factor used to indicate the severity of the degradation versus time is defined as

$$F(t) = \left[\frac{h_{FE}^{-1}(t) - h_{FE}^{-1}(0)}{h_{FE}^{-1}(\infty) - h_{FE}^{-1}(0)} \right] \quad (4.69)$$

where $h_{FE}(t)$ is the gain as a function of time, $h_{FE}(0)$ is the initial value, and $h_{FE}(\infty)$ is the final value after annealing. The magnitude of $F(t)$ is a function of collector current, as shown in Figure 4-36, where lower operating collector currents result in higher annealing factors. Another method for determining an annealing factor is with the nomograph of Figure 4-33, where time after exposure and transistor V_{BE} are used to construct a line that intersects the annealing factor scale. Consideration of short-term annealing is only required for systems that are required to operate immediately after exposure.

In some cases, such as power-switching applications, degradation of the $V_{CE(SAT)}$ parameter may be as important as the decrease in h_{FE} . $V_{CE(SAT)}$ increases as the neutron fluence increases, due mainly to a decrease of the minority-carrier lifetime in the collector region. Minority

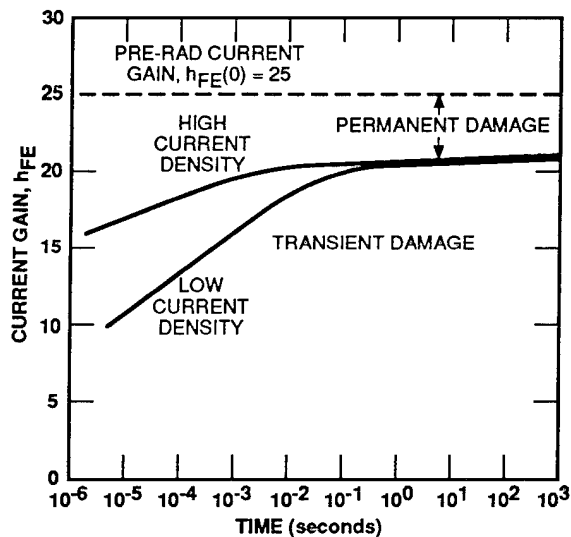


Figure 4-34. Transient and permanent damage to transistor current gain after neutron exposure (Rose, 1984).

carriers that are injected into the collector region from the base during saturation do not produce as much conductivity modulation of the collection region when the minority-carrier lifetime decreases sufficiently. The collector resistance increases and produces a larger voltage drop for a given collector current. At moderate neutron levels, the voltage increase is not a problem for switched transistors made with a thin epitaxial layer. For switching transistors with a large, lightly doped collector region, however, the voltage increase may be significant. Figure 4-37 shows a normalized scatter plot for change in $V_{CE(SAT)}$, with typical 10 to 20 percent changes up to 10^{13} n/cm². Figure 4-38 shows changes in I_{CBO} as a function of neutron fluence, from which it can be seen that the curve is relatively flat. Another parameter affected by neutron irradiation is junction breakdown voltage, e.g., BV_{CEO} and BV_{CBO} . However, only small changes in junction breakdown voltage are realized, even at fluences as high as 10^{15} n/cm².

4.5.5 Junction Field-Effect Transistors

The primary neutron-induced effects in JFETs are carrier removal from the channel and the creation of traps in the space-charge region, causing channel modulation. Since the magnitude of the effects caused by carrier removal is proportional to available carriers, devices with higher doping

concentration are less sensitive to the neutron fluence. Also, n-channel devices are more resistant than p-channel devices to neutron-induced degradations. Parameters most sensitive to neutron effects are g_m (transconductance), I_{DS} (source-to-drain current), and V_{PO} (pinch-off voltage). Moderately doped (8×10^{15}) n-channel devices showed only a 20 percent decrease in I_{DS} at 10^{14} n/cm² and 60 percent at 10^{15} n/cm². In comparison, heavily doped (3×10^{16}) devices showed <5 percent change in I_{DS} at 10^{14} n/cm² and 30 percent at 10^{15} n/cm², clearly demonstrating the reduced sensitivity of heavily doped channels as well as the inherent hardness of JFETs to neutrons. Similar changes in other parameters have also been observed at comparable neutron fluences.

4.5.6 Metal-Oxide Semiconductor Field-Effect Transistors

Since a MOSFET is a majority-carrier device and is not significantly affected by carrier removal in the channel, it is inherently hard to neutrons. The major neutron-induced degradation in MOSFETs is not the result of bulk displacement, but results instead from the ionizing effects of neutron irradiation. Ionizing radiation dose effects in MOSFETs are discussed in Chapter 2. The neutron levels corresponding to these types of ionizing effects are generally in excess of 10^{15}

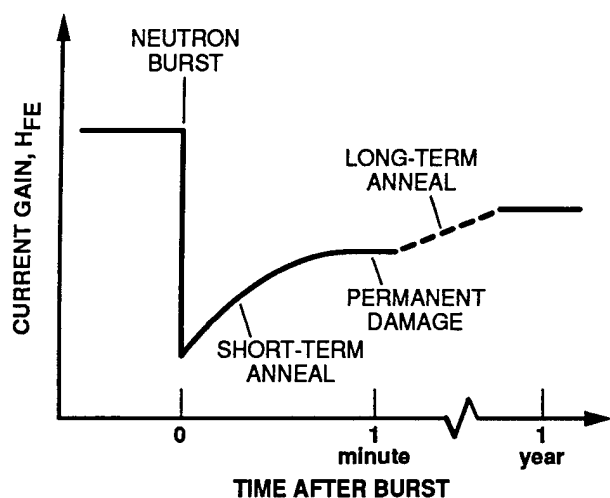


Figure 4-35. Room-temperature annealing, short- and long-term recovery processes in neutron-irradiated silicon (Srouf, 1982).

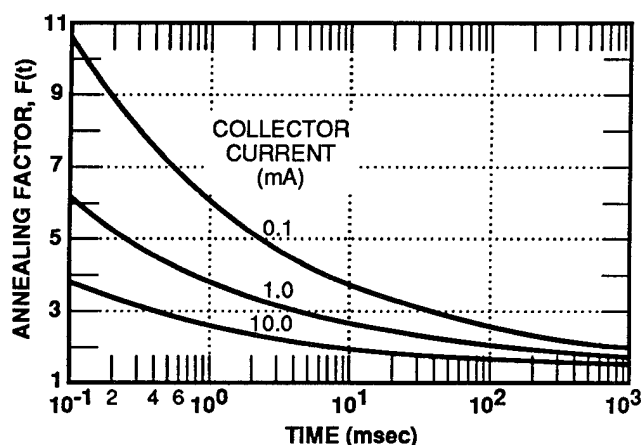


Figure 4-36. Short-term annealing factors as a function of collector current for low- and medium-power silicon npn transistors (Rockwell, 1981).

n/cm^2 , thus MOSFET devices are inherently hard to neutrons.

4.5.7 Four-Layer Devices

Neutron damage affects several electrical parameters of four-layer devices. The changes are caused both by decreases to the minority-carrier lifetimes of the interior p- and n-regions, and by an increase in the resistivity of the n-region. The lifetime changes are seen most easily by using the two-transistor equivalent model of a four-layer device [Figure 4-39]. Positive feedback between the two transistors allows the device to enter a low-impedance state and conduct anode current I_A when the product of the transistor cur-

rent gains ≥ 1 . This state is attained by either injecting gate current or increasing the anode-to-cathode voltage V_{AK} until there is an avalanche breakdown of the center pn junction.

The effect of the neutron-induced decrease in minority-carrier lifetime in the two-transistor base region is to decrease the h_{FE} of each device. A larger holding current will be needed to keep the product $h_{FE1} \times h_{FE2} \geq 1$. A larger gate current or anode voltage will also be needed to turn the device ON. The increased resistivity in the n-region of the pnp transistor will also increase the forward ON-state voltage.

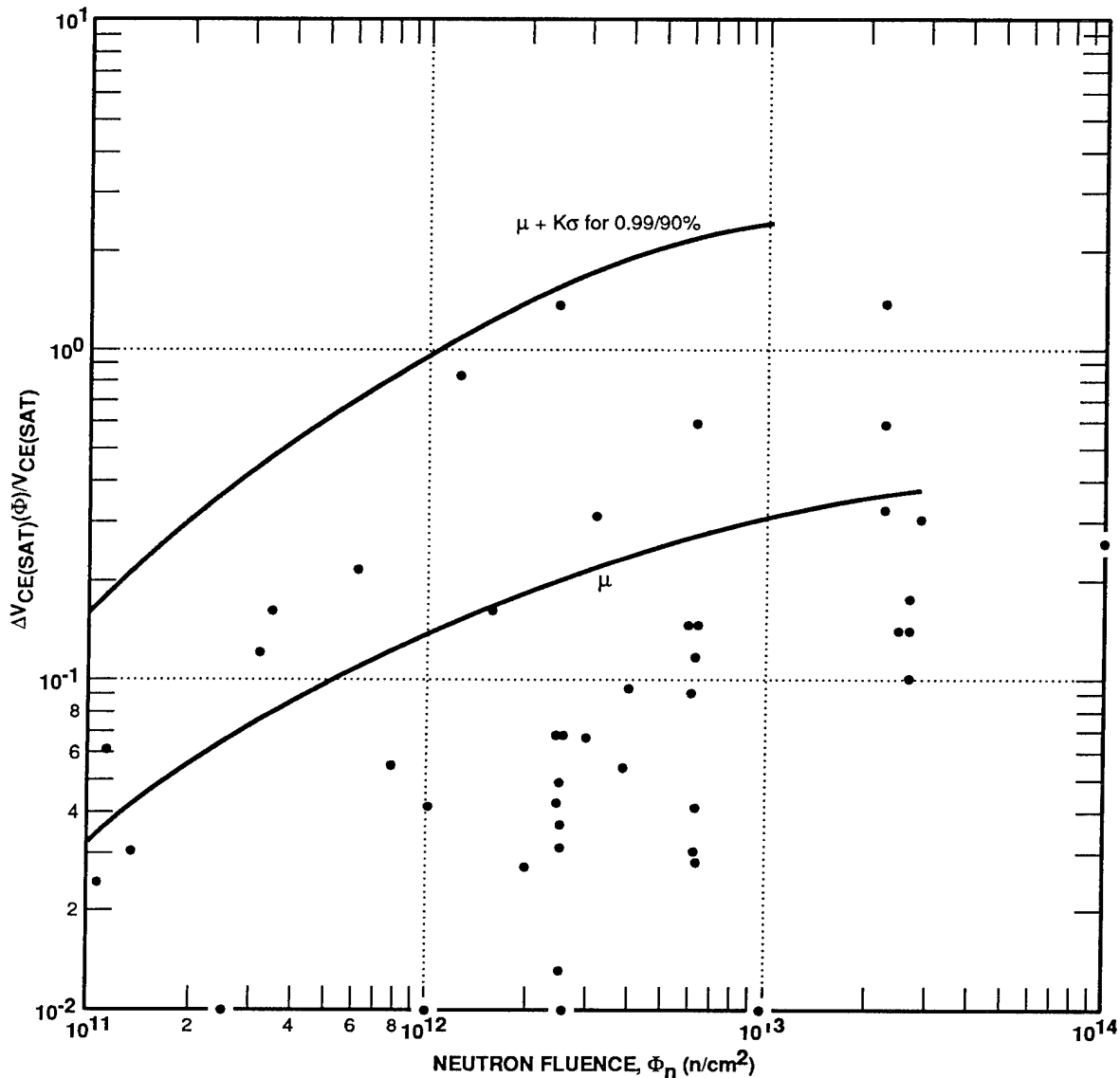


Figure 4-37. Normalized change in $V_{CE(SAT)}$ for general-purpose transistors at 25°C versus neutron fluence [$\Delta V_{CE(SAT)}(F)$ is the average change in $V_{CE(SAT)}$ for the given test sample] (Rose, 1984).

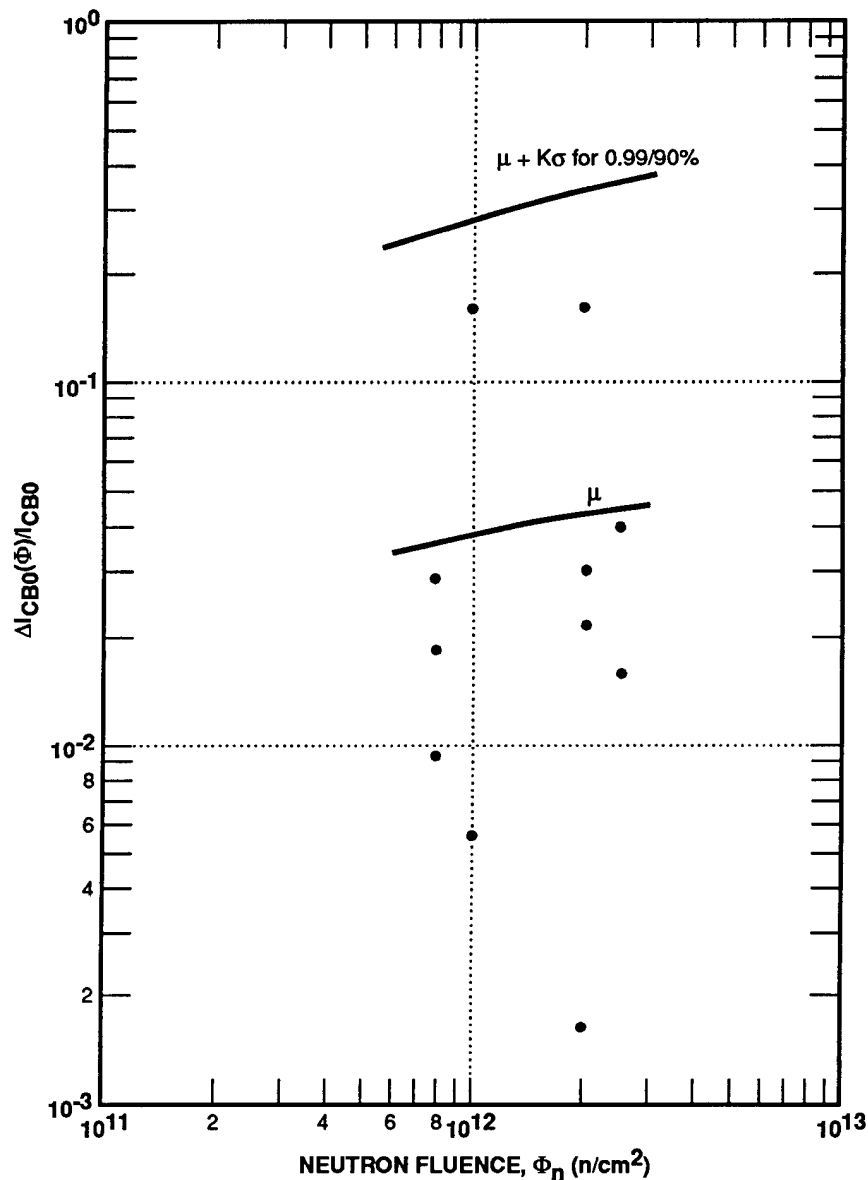


Figure 4-38. Normalized change in I_{CBO} for general-purpose transistors at 25°C versus neutron fluence [$\Delta I_{CBO}(\Phi)$ is the average change in I_{CBO} for the given test sample] (Rose, 1984).

The level at which these effects cause a circuit failure varies over a wide range, from about 5×10^{11} to 10^{14} n/cm². Devices with a wide, lightly doped n-region for the pnp transistor tend to fail at the lower levels, while devices with a narrow n-region and higher doping level survive to the higher level. In terms of part-specification parameters, devices with a low breakdown voltage, a low forward ON-state voltage, and/or a low maximum current rating tend to be less susceptible to neutron damage.

4.5.8 Bipolar Digital Integrated Circuits

Bipolar digital ICs undergo permanent changes in their output voltage levels, input current, fanout, and propagation delay time due to displacement damage. Low-power Schottky transistor-transistor logic (LSTTL), STTL, low-power TTL, as well as standard TTL logic all experience some performance degradation between 6×10^{13} and 10^{14} n/cm² but can be used in designs at $>10^{14}$ n/cm² if appropriately derated.

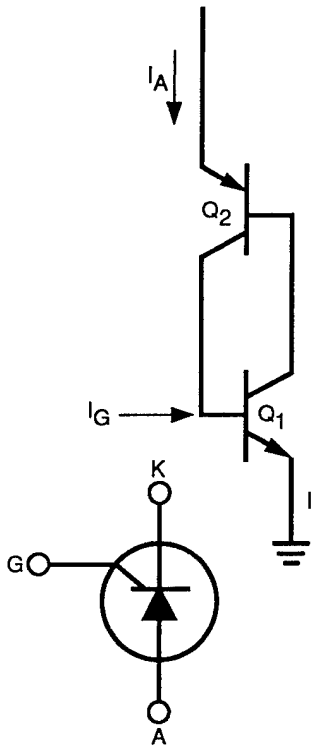


Figure 4-39. SCR two-transistor equivalent model schematic and symbol (Messenger and Ash, 1992).

New TTL technology such as advanced STTL (FAST), advanced Schottky logic (ASL), as well as emitter-coupled logic (ECL) shows the first signs of degraded performance at neutron fluences in excess of 10^{14} n/cm² and some may even be used up to 10^{15} -n/cm² levels when derated. None of these types of logic should be of concern at moderate neutron levels. Figure 4-40 plots the range of failure thresholds for the various technologies. Some injection current logic, however, may fail at lower levels than TTL or ECL devices. Test data from some of the first-generation devices showed significant damage at 2×10^{12} n/cm² and failure levels of the order of 6×10^{12} to 5×10^{13} n/cm². Another form of bipolar logic is current-mode logic (CML). The data available for these type of parts show failure thresholds approaching 10^{15} n/cm² or greater.

4.5.9 Linear Integrated Circuits

The hardness of linear ICs will vary over a wide range because of the variety of device designs and fabrication techniques. Changes in IC parameters are due mainly to the degradation of

TECHNOLOGY	MANUFACTURER	NEUTRON FLUENCE (n/cm ²)				
		10 ¹²	10 ¹³	10 ¹⁴	10 ¹⁵	10 ¹⁶
STANDARD TTL	VARIOUS			██████████		
LOW-POWER SCHOTTKY TTL (LSTTL)	VARIOUS			██████████		
RAD-HARD LSTTL	VARIOUS, TEXAS INSTRUMENTS, HARRIS			██████████		
ADVANCED STTL (FAST)	NATIONAL SEMI, MOTOROLA, SIGNETIC			██████████		
ADVANCED SCHOTTKY LOGIC (ASL)	TEXAS INSTRUMENTS			██████████		
INTEGRATED SCHOTTKY LOGIC (ISL)	RAYTHEON			██████████		
EMITTER-COUPLED LOGIC (ECL)	VARIOUS				██████████	
ISOPLANAR-Z PROCESS ISO-Z	NATIONAL SEMI				██████████	
IMPLANTED OXIDE (IMOX)	AMD AND VARIOUS OTHERS				██████████	
DIELECTRIC ISOLATED TTL	HARRIS, VARIOUS				██████████	

Figure 4-40. Neutron threshold for digital bipolar integrated circuits (Rose, 1984).

h_{FE} in the transistor elements of the IC. Devices that contain lateral pnp transistors will be sensitive to neutron damage because the base regions of these transistors are wide and their transistors have a fairly low f_T . The ICs can also be sensitive to damage due to the low collector currents used in the IC transistor elements.

For operational amplifiers, the main parameters that will show degradation are the input bias current, I_b , input offset current, I_{OS} , offset voltage, V_{OS} , open-loop gain, A_{VOL} , and slew rate. Figure 4-41 shows typical changes in these parameters as a function of neutron fluence.

The input transistors of these ICs are usually designed to operate at low current levels and tend to have larger neutron damage constants. The first noticeable change is usually an increase in the bias current on each input lead as the h_{FE} of the input transistors degrades. The input transistors are usually closely matched, so the bias currents for the two transistors remain approximately equal as the currents increase with the fluence level. The bias currents may show appreciable changes before the V_{OS} and I_{OS} parameters begin to rise rapidly with an increasing neutron level. Most circuits can withstand larger percentage changes of I_b than V_{OS} or I_{OS} ; however, degradation to any one of these three parameters may be the first to cause a circuit failure.

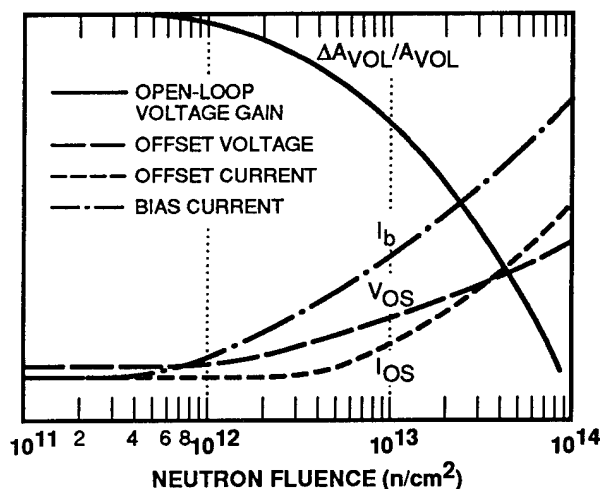


Figure 4-41. Neutron effects in linear integrated circuits (Rose, 1984).

The A_{VOL} parameter normally will not cause a circuit failure. The A_{VOL} parameter generally starts degrading at higher levels than the I_b , I_{OS} , and V_{OS} parameters, and circuits are usually designed to withstand a large gain reduction before failure occurs.

The slew rate of operational amplifiers will also be affected by neutron exposure. The gains of the intermediate-stage transistors in a device are decreased by neutron damage. Since these transistors provide the drive current to charge internal and external capacitances, a reduction of this drive capability causes the slew rate of the device to decrease. This effect is normally less important than changes to the I_b , I_{OS} , or V_{OS} parameters, but it should be measured during neutron tests of a device if the slew rate is critical for a particular circuit application.

Using part specification limits as criteria, the failure levels for the operational amplifiers will vary from about 5×10^{11} to 10^{14} n/cm^2 . Most devices will begin to fail in the range from 5×10^{12} to 5×10^{13} n/cm^2 , but a few high-performance ICs (such as the LM108 or OP-05J) can fail as low as 5×10^{11} to 1×10^{12} n/cm^2 . All the devices will still function above these levels, but they cannot be used for applications requiring tight parameter tolerances.

For comparators, the input bias current, offset voltage, and gain parameter will all degrade in a manner similar to operational amplifiers. The low-output voltage state V_{SAT} will also increase as the neutron level increases. The high-output voltage state V_{OH} is less affected. The V_{OS} and V_{SAT} parameters are usually the most important from a circuit-failure standpoint. They begin to exceed their specification limits in the range from 5×10^{12} to 5×10^{13} n/cm^2 .

For voltage regulators, the line and load regulation parameters usually degrade the most rapidly as the neutron fluence is increased. Either or both of these parameters may degrade beyond their specification limits in the range from about 1×10^{12} to 5×10^{13} n/cm^2 . The output voltage remains fairly stable as regulation parameters exceed their limits; however, the output voltage V_{OUT} of some voltage regulators will begin to

drop very rapidly to zero as the fluence level increases. The “knee” of the V_{OUT} versus fluence curve is not necessarily consistent, even for devices of the same generic type and manufacturer. A summary of neutron irradiation effects in a number of typical linear integrated circuits is shown in Table 4-4.

4.5.10 Metal-Oxide Semiconductor Digital Integrated Circuits

MOS technology devices are inherently hard to neutrons since they are majority-carrier devices and are not dependent on minority-carrier lifetime. The primary effects of neutrons on MOS devices is from ionization rather than displacement [see Chapter 2 for ionizing radiation dose effects on MOS technology devices].

4.5.11 Memories, Microprocessors, and Gate Arrays

Magnetic memories are effectively immune from neutron effects until physical material damage starts to occur at fluences orders of magnitude above electronic effects. Therefore, the primary consideration of neutrons for this class of parts is solely for semiconductor memories. Since MOS technology parts are inherently hard to neutron effects, the concern is narrowed down to bipolar memories and microprocessors. The robustness of MOS technology devices has been recently reconfirmed (Hite and Bell, 1992) through neutron testing of 0.8- μm critical feature size 256k static random-access memory (SRAM) circuits manufactured using complementary MOS (CMOS) technology. In these tests, no perceptible circuit degradation was noted for neutron fluences up to and including 10^{14} n/cm². The primary bipolar technologies for fabricating memories, microprocessors, and gate arrays are IIL, CML, ECL, ALS, and FAST double-diffused. The available types of devices and corresponding neutron hardness are given in Table 4-5, from which it can be seen that all the TTL- and ECL-based logic devices are hard to $>10^{14}$ n/cm². The most sensitive device types appear to be the IIL-based devices. The latest available data (Carroll and Szot, 1983) on the IIL Texas Instruments SBR 9000 indicated the devices were hard to 3×10^{13} n/cm², with some devices passing 5×10^{13} n/cm².

4.6 Displacement Damage Effects on Gallium Arsenide Field-Effect Transistors

Minority-carrier degradation due to displacement damage is not important in GaAs devices, either because of the short initial (pre-irradiation) carrier lifetimes of bipolar GaAs technologies or because the devices are majority-carrier devices for FET technologies. The transistor gain degradation in either kind of device is due primarily to carrier removal and mobility degradation. The change in the slope of the curve in Figure 4-42 shows the change in the transconductance of a JFET due to these effects following neutron exposure to 1.7×10^{15} n/cm². A detailed analysis of neutron-induced degradation in transconductance for JFETs operating in the hot-electron regime was carried out by Behle and Zuleeg (1972), and the results for the transconductance normalized to its initial value are shown in Figure 4-43 plotted against neutron fluence for three different channel-doping concentrations. Experimental results for GaAs JFETs with a channel doping of approximately 1×10^{17} cm⁻³, shown by the circles in the figure, are in good agreement with the predictions of the analysis.

GaAs is used extensively in optoelectronic devices [Section 4.7], which degrade by the introduction of nonradiative recombination centers that lead, for example, to a decreased efficiency in GaAs light-emitting diodes (LEDs).

GaAs is also used in silicon sensor arrays [Section 4.8]. Carrier removal is the prime degradation mechanism in GaAs charge-coupled devices (CCDs), leading to reduction in the charge-transfer efficiency. A more detailed discussion of the displacement damage effects on this class of GaAs devices is contained in Section 4.8 of this chapter.

4.7 Displacement Damage Effects on Optical Fibers and Optoelectronic Devices

The effects of displacement damage on optical fibers and optoelectronic devices are discussed here. As shown in Figure 4-44, a typical fiber-optic link consists of several components: a source drive circuit, a light-emitting diode (LED) or injection laser diode (ILD), an optical fiber of varying length (0 for an optical coupler), a pho-

Table 4-4. Neutron degradation in typical linear integrated circuits (Rose, 1984).

	Neutron Fluence (n/cm ²)	Input Offset Voltage, V _{OS} (mV)	Input Offset Current, I _{OS} (nA)	Negative Input Bias, I _b (nA)	Positive Input Bias, I _b (nA)	Gain (dB)
Operational Amplifiers						
741	Pre-rad	0.815	0.711	0.210	0.827	106.2
	1 × 10 ¹²	0.915	1.41	8.345	9.423	106.2
	1 × 10 ¹³	1.840	5.57	93.18	98.74	105.4
	5 × 10 ¹³	18.423	92.5	497.2	582.5	56.2
A709	Pre-rad	2.02	0.0063	0.0513	0.0575	102.4
	5 × 10 ¹¹	2.03	0.0088	0.0588	0.0588	102.3
	5 × 10 ¹²	2.05	0.0501	0.1376	0.1538	101.7
	4 × 10 ¹³	2.21	0.2123	0.7105	0.5535	101.0
Op05	Pre-rad	0.326	0.670	1.1	1.17	100.6
	5.5 × 10 ¹¹	0.336	1.201	7.43	9.44	100.0
	5 × 10 ¹²	0.426	2.850	44.1	47.17	99.9
	4.4 × 10 ¹³	12.226	71.570	128.1	224.17	99.
MC1556G	Pre-rad	1.56	0.50	6.37	6.36	101.
	5.3 × 10 ¹¹	1.63	0.65	9.79	9.76	100.9
	5.2 × 10 ¹²	1.64	3.43	43.07	44.46	100.8
	4 × 10 ¹³	13.56	101.5	147.37	281.36	73.8
LM108H	Pre-rad	0.95	0.0611	1.13	1.22	100.6
	5.3 × 10 ¹²	0.985	0.185	2.01	2.08	99.9
	5.2 × 10 ¹²	1.24	0.424	10.46	10.69	99.3
	4 × 10 ¹³	Failed	Failed	Failed	Failed	Failed
	Neutron Fluence (n/cm ²)	Saturation Voltage V _{SAT} (volts)	High-Level Output Voltage V _{OH} (volts)	Input Offset Voltage V _{OS1} (mV) V _{OS2} (mV)		
Comparators						
F711HC	Pre-rad	0.337	4.02	1.74	1.43	
	5.6 × 10 ¹¹	0.339	4.03	1.78	2.69	
	5.2 × 10 ¹²	0.346	4.05	1.79	3.27	
	4.2 × 10 ¹³	0.349	4.41	2.25	3.86	
LM119H	Pre-rad	0.278	14.97	0.426	1.17	
	5.6 × 10 ¹¹	0.278	14.97	0.516	1.21	
	5.2 × 10 ¹²	0.294	14.97	0.519	1.27	
	4.2 × 10 ¹³	0.355	14.98	0.676	1.35	
	Neutron Fluence (n/cm ²)	Output Voltage V _{OUT} (volts)	Load Regulation (percent)	Line Regulation (percent)		
Regulators						
LM105H	Pre-rad	10.05	0.011	0.139		
	5.5 × 10 ¹¹	10.06	0.023	0.157		
	5 × 10 ¹²	10.07	0.023	0.270		
	4.4 × 10 ¹³	10.16	0.067	0.250		
mA723HC	Pre-rad	5.08	0	0		
	5.4 × 10 ¹¹	5.08	0	0		
	5.2 × 10 ¹²	5.09	0.03	1.34		
	4.4 × 10 ¹³	7.20	0.05	2.5		

Table 4-5. Neutron response of memories and microprocessors (Hite and Bell, 1992).

Device	Manufacturer	Technology ^a	Neutron Failure Level (n/cm ²)
TIX0400	Texas Instruments	IIL	1.0×10^{13}
F100L μ Proc	Ferranti	CDI	1.0×10^{13}
13101A RAM	Intel	TTL	8.0×10^{14}
AM2901 μ Proc	AMD	TTL	4.0×10^{14}
MM16340D EPROM	National	STTL	1.5×10^{14}
MM167010 μ Proc	National	STTL	1.5×10^{14}
882S11F RAM	Signetics	TTL	3.0×10^{14}
SMS8228 ROM	SMS	STTL	$>2 \times 10^{14}$
SBR 9900 μ Proc	Texas Instruments	IIL	5.0×10^{13}
SBR 9900A μ Proc	Texas Instruments	IIL	$>3 \times 10^{13}$

Legend:
^aIIL — current injection logic; CDI — collector-diffused isolation; TTL — transistor-transistor logic; STTL Schottky TTL.

todiode, a preamplifier receiver circuit, and a variety of connectors.

Also shown in Figure 4-44 with the generic fiber-optic link are some of the environmental effects that are important for each component of the link. For emitters, neutron-induced displace-

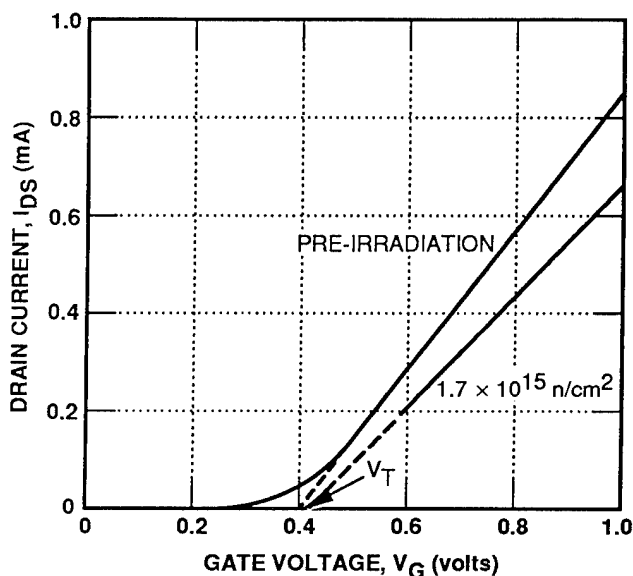


Figure 4-42. Effect of irradiation on drain current-gate voltage characteristics of epitaxial GaAs JFET; channel-region doping density = 10^{17} n/cm^3 (Zuleeg and Lehovc, 1980).

ment damage is the most significant effect; for fibers, transient and permanent ionization-induced attenuation is the most severe effect; and for photodiodes, transient-ionization-induced photocurrents pose the major problem. Each of the components that comprise the fiber-optic link, with the exception of the CMOS drive circuit, will be addressed in the following subsections.

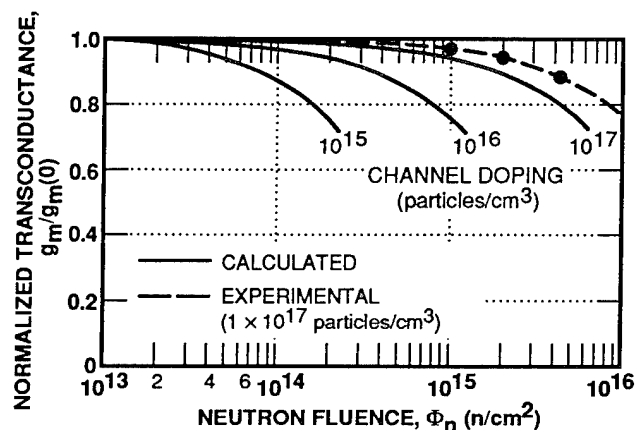


Figure 4-43. Calculated normalized transconductance versus neutron fluence for GaAs JFETs operating in the hot-electron range for three channel-doping concentrations (Behle and Zuleeg, 1972).

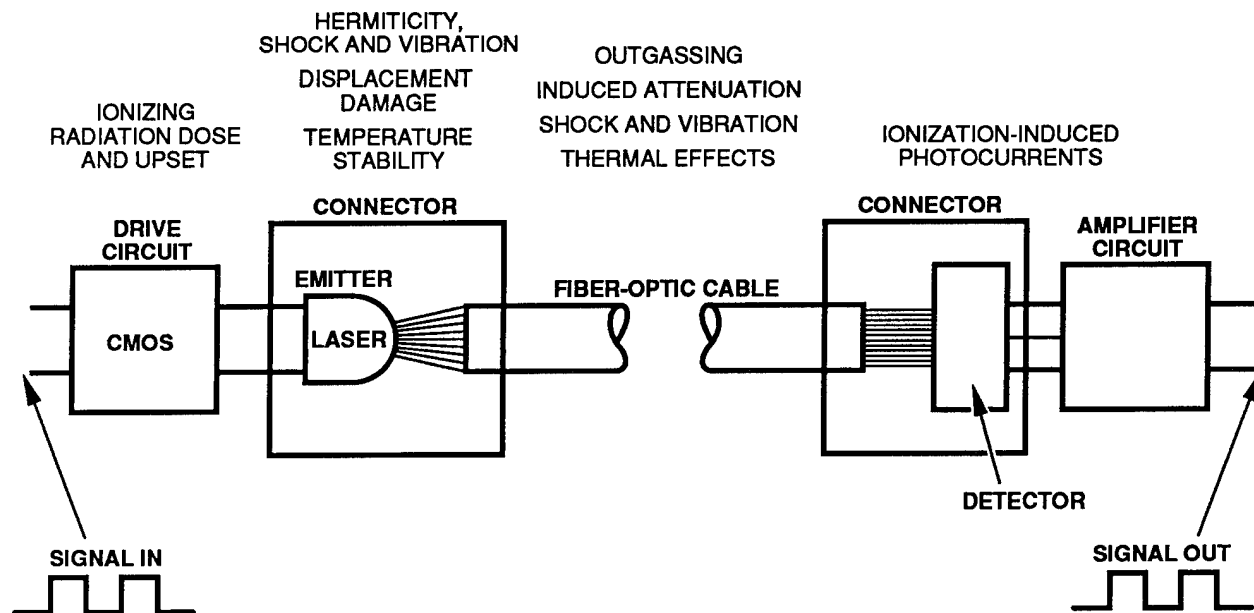


Figure 4-44. Schematic diagram of a typical fiber-optic link showing environmental effects on different components of the link (Barnes, 1992).

4.7.1 Light-Emitting Diodes

Radiation-induced displacement damage in the semiconductor lattice of the active, light-producing region in LEDs [and in ILDs as well] is the most serious effect of the radiation environment (Barnes, 1972, 1977, 1979, 1984; Dimiduk, Ness, and Foley, 1985; Hooft and van Opdorp, 1984; Polimadei *et al.*, 1974; Rose and Barnes, 1982; Stanley, 1970). The key to understanding the detrimental effects of lattice damage on the performance of LEDs lies in an examination of the operating mechanisms of these devices. In an operating LED under forward bias, excess minority carriers are injected across the pn junction, where they recombine with majority carriers. The various mechanisms by which these injected minority carriers recombine determine the light output efficiency of the LED. If most of the carriers recombine radiatively to produce photons of energy roughly equal to the semiconductor energy bandgap, then the device will be efficient. However, if the dominant recombination mechanism is nonradiative, then the light emission will be weak and the LED will be inefficient. A variety of centers can act as sites for nonradiative

recombination events: unintentionally added impurities, dislocations, growth-induced lattice defects, and, most important for the present discussion, radiation-induced lattice defects. The effectiveness of the various excess carrier recombination paths is expressed by the minority-carrier lifetime, which is inversely proportional to the concentration of recombination centers. If the lattice defects are introduced during exposure to a neutron fluence Φ_n at a rate determined by damage constant K_τ , then the reduction in pre-irradiation minority-carrier lifetime τ_0 to a post-irradiation value of τ can be expressed as follows (Thornton, 1967; Aukerman, Milea, and McColl, 1966)

$$\tau_0/\tau = 1 + \tau_0 K_\tau \Phi_n \quad (4.70)$$

Thus, when the product $\tau_0 K_\tau \Phi_n$ is significant compared to 1, the lifetime will decrease, leading to a corresponding decrease in light output due to the increased strength of the nonradiative recombination path. $\tau_0 K_\tau$, then, can be viewed as an "inverse figure of merit"; that is, the larger $\tau_0 K_\tau$, the more sensitive the LED will be to irradiation. Thus, one approach to the radiation hardening of

LEDs is to devise methods of reducing the magnitude of $\tau_0 K_\tau$.

The pre-irradiation minority-carrier lifetime τ_0 is more amenable to experimental manipulation than the damage constant K_τ because K_τ is essentially determined by the type of radiation and the chemical elements making up the semiconductor material. Indeed, τ_0 can be decreased by increasing either the radiative or nonradiative recombination rate. If the radiative recombination rate can be maximized so that it controls and minimizes the pre-irradiation lifetime, then the LED will have high pre-irradiation light output and will also be less sensitive to irradiation.

Enhancement of the radiative recombination rate is an appropriate goal in the design of an LED, even when radiation sensitivity is not a consideration. To this end, LEDs are usually fabricated from semiconductor materials that have direct energy gaps, resulting in relatively strong light emission due to band-to-band recombination (direct recombination of electrons and holes without the assistance of lattice vibrations or recombination centers). For this type of radiative recombination, the recombination rate R_r (sec/cm³) is given by

$$R_r = B_r \Delta n (p + \delta n) \quad (4.71)$$

and

$$1/\tau_r = B_r (p + \delta n) \quad (4.72)$$

in units of inverse seconds (sec⁻¹), where B_r is a recombination coefficient, δn is the excess injected minority-carrier density, p is the majority-carrier density, and τ_r is the radiative lifetime. Here, it is assumed that the light emission originates on the p-side of the LED junction. Equations 4.71 and 4.72 indicate that the radiative recombination rate can be increased (lifetime decreased) by heavily doping the optical emitting region to raise p , and/or by operating the LED at very high forward current densities to maximize δn .

Past studies (Barnes, 1977; Hooft and van Opdorp, 1984) of neutron damage effects in LEDs indicate that the above techniques do result in LED hardening to displacement damage. An

example of such work is shown in Figure 4-45, where the normalized light output degradation curves illustrate the wide variation in LED response to irradiation. In the case of the most sensitive device in Figure 4-45 (the TIL-26 GaAs:Si,Si device), the minority-carrier lifetime is achieved through amphoteric doping (the same element, silicon, is used for both p- and n-type doping) during relatively low-temperature epitaxial growth, which minimizes the concentration of nonradiative recombination centers. However, the radiative lifetime is also quite long, so that the total lifetime is long, $\tau_0 K_\tau \Phi_n$ is large, and the LEDs are sensitive to radiation, as predicted by Equation 4.70.

At the opposite end of the radiation-sensitivity spectrum in the upper right-hand corner of Figure 4-45 is a group of LEDs that can provide sufficient light output for many applications after neutron fluences in excess of 2×10^{14} n/cm². In agreement with the simple analysis above, the experimental results suggest that the primary difference between these devices and the more sensitive LEDs, such as the GaAs:Si,Si device, is appropriate control of the minority-carrier lifetime. For example, note that the four most radiation-resistant LEDs in Figure 4-45 are all high-radiance (HR) devices. A typical example of such an LED is the Burrus structure shown in Figure 4-46. Figure 4-46 indicates that these LEDs possess very small source and junction areas so that the injected minority-carrier current density is large, even at moderate current levels. Thus, as indicated by Equation 4.71, in such LEDs the radiative recombination rate can be expected to be enhanced at typical operating currents.

Further evidence that a high value of δn is of critical importance in reducing the radiative lifetime and thereby improving the radiation hardness is given in Figure 4-47. In addition, these results demonstrate the radiation-hardening effect of heavily doping the light-emitting region of the LED. In Figure 4-47, the neutron-induced degradation of planar, low-current-density LEDs (TI) is compared with that of high-current-density, high-radiance devices (PL). Note that the TI LED operating at 50 mA is the most sensitive to

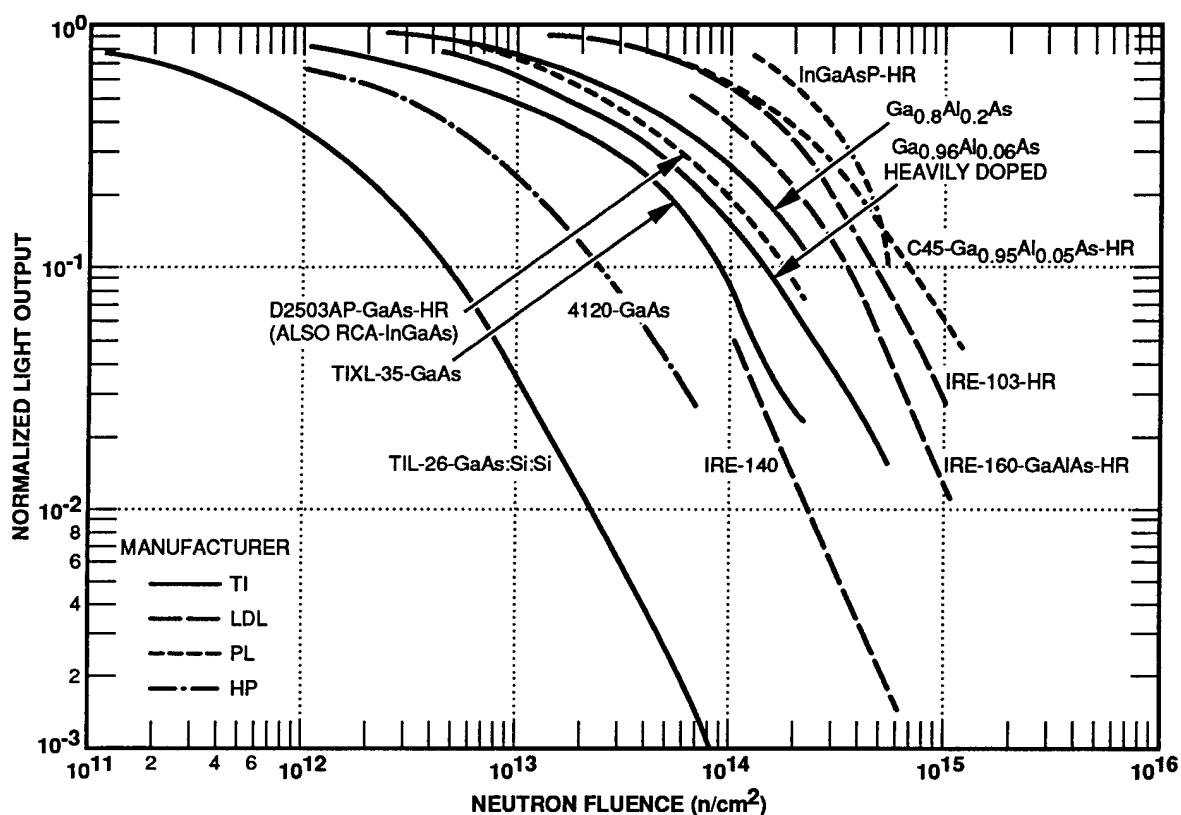


Figure 4-45. Effect of neutron damage on the normalized output of a variety of LEDs, constant current at 25°C (Barnes, 1977).

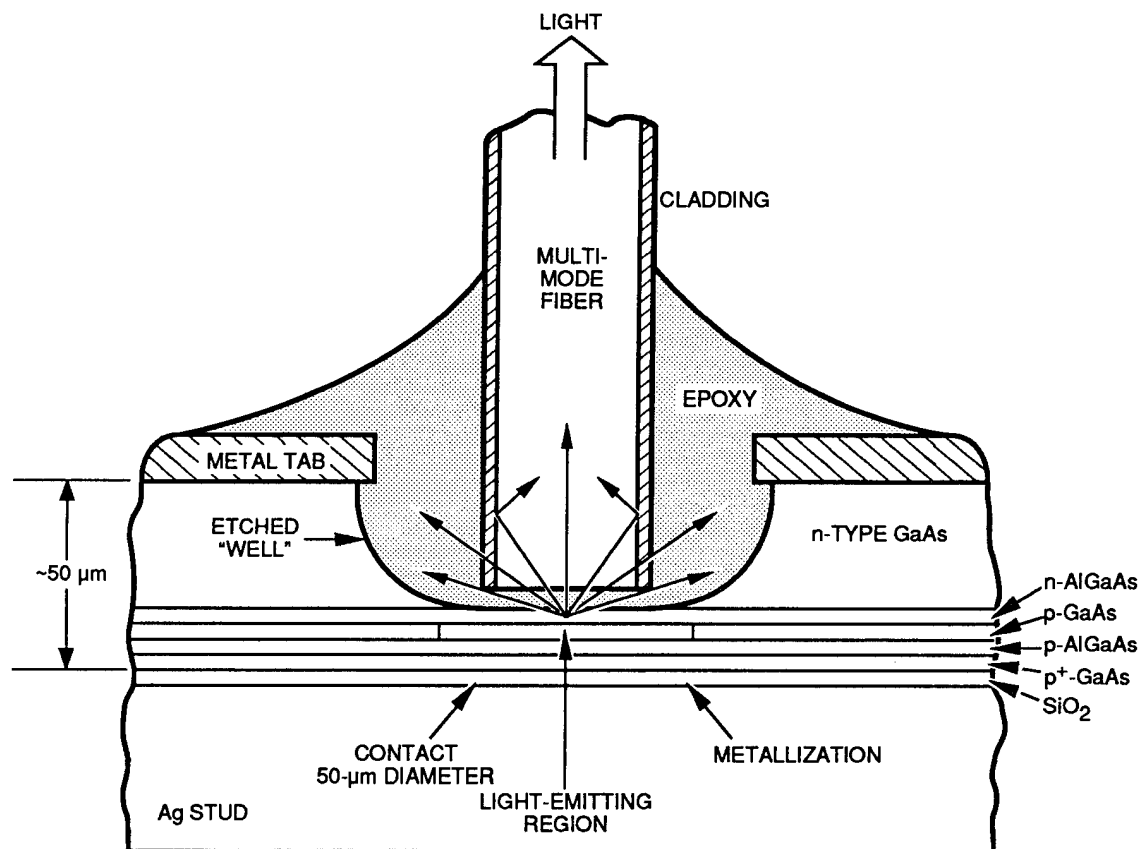


Figure 4-46. Burrus-type LED structure characterized by a high-radiance emitting region (Burrus and Miller, 1971).

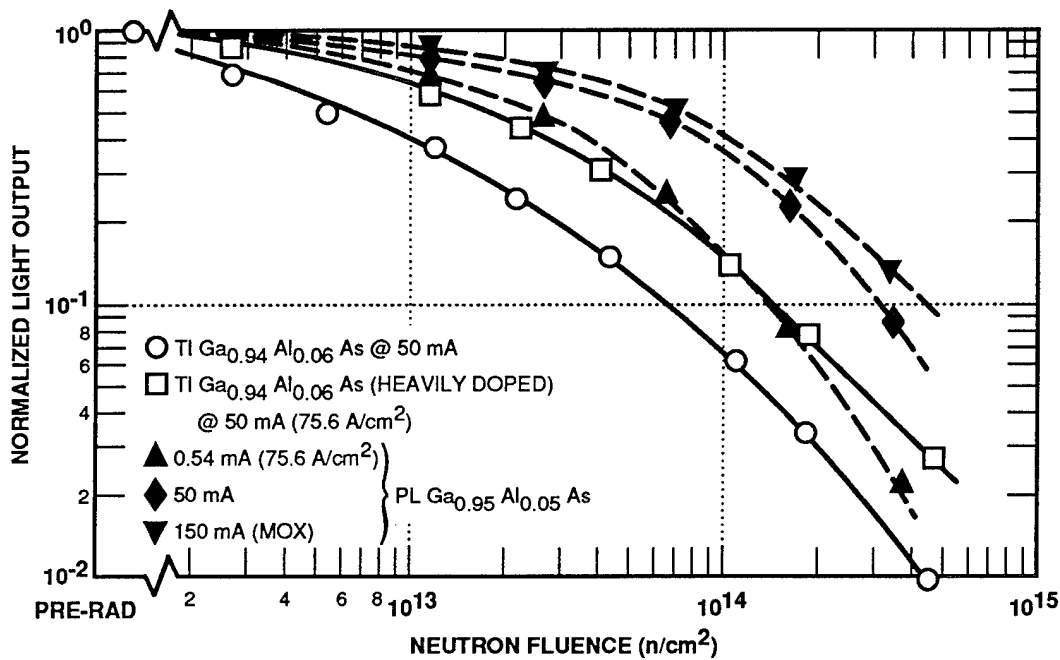


Figure 4-47. Dependence of neutron-induced degradation of normalized light output on current density (Barnes, 1977).

neutron irradiation. However, if the p-regions of these devices are more heavily doped, then, as shown in Figure 4-47, the LEDs are less sensitive. In addition, the PL LEDs have approximately the same degradation rate when they are operated at 100 times less current, but at an equal current density. As the current is raised in the PL devices, the degradation rate decreases so that at an equal current of 50 mA these LEDs are about a factor of 10 better than the TI LEDs. The PL LEDs have a significantly greater pre-irradiation light output power than the TI devices. Thus, these results are in agreement with the predictions of Equations 4.70 through 4.72, which indicate that radiation hardness and high initial light output can be achieved simultaneously.

4.7.2 Injection Laser Diodes

The major effect of displacement damage on laser diodes is to provide an alternate non-radiative recombination path, which reduces the minority-carrier lifetime. Results from previous work (Barnes, 1974) on neutron irradiation of GaAs pulsed ILDs are shown in Figure 4-48, which has been divided into three regions. In region 1, the subthreshold region, the laser behaves like an LED and, as expected, the light

output at constant current decreases with neutron fluence at about the same rate as for an LED of similar characteristics. The onset of lasing action at the threshold current density J_{TH} is indicated by the rapid upturn in the curves at the bottom of region 2. Because of the very strong dependence of light output on current in this region, neutron irradiation causes a drastic drop in output. In contrast, in region 3 (where the device is well into lasing), irradiation does not have a significant effect until the increase in J_{TH} prevents the laser from reaching region 3. The fact that the neutron-induced degradation is much less in region 3 than it is in region 1 can be explained within the framework of the lifetime degradation model. Typical minority-carrier lifetimes in GaAs junctions, which are characteristic of operation in region 1, are 1 to 10 nsec, while under intense stimulated emission conditions (region 3) lifetimes are of the order 1 to 10 psec. Therefore, a much larger concentration of radiation-induced defects is required to influence the radiative recombination rate in region 3 through competing nonradiative recombination. From a more practical point of view, the message conveyed by the data in Figure 4-48, which is typical of many laser diode types, is that an ILD that has a low

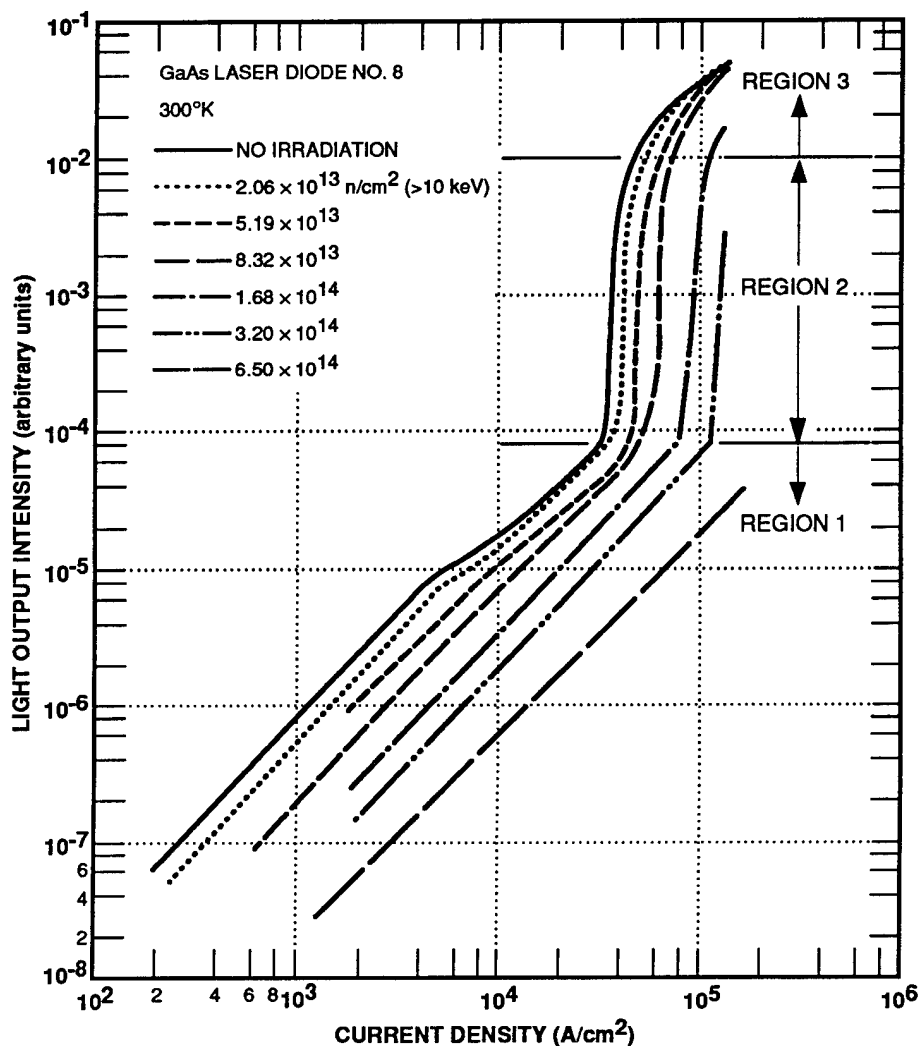


Figure 4-48. Neutron-induced degradation of GaAs laser diodes (Barnes, 1974).

threshold current and a very high maximum operating current should be chosen.

More recent results (Barnes, 1982) for state-of-the-art InGaAsP ILDs with peak emission wavelengths near $1.25 \mu\text{m}$ are shown in Figure 4-49. These results are similar to the earlier work shown in Figure 4-48, in that there is less degradation well above threshold. Another interesting feature of these results that is characteristic of a variety of lasers is that the damage is more effective at higher temperatures. In general, it was found (Barnes, 1984) that laser diodes that are the least sensitive to temperature prior to irradiation are also less sensitive to irradiation. This parallel between reduced temperature sensi-

tivity and radiation hardness suggests that continued improvement in laser diode operating characteristics will be accompanied by improvements in radiation hardness.

4.7.3 Photodetectors

A brief discussion on theory of operation of a silicon pn junction photodiode is given here, prior to a discussion of radiation effects on photodetectors. The pn junction photodiode is typically asymmetrically doped (for example, n^+p), with the thin, heavily doped layer exposed to the light signal. Because of surface recombination and the short hole diffusion length in the thin n^+ -region, it is usually assumed that this region does not make a significant contribution to the

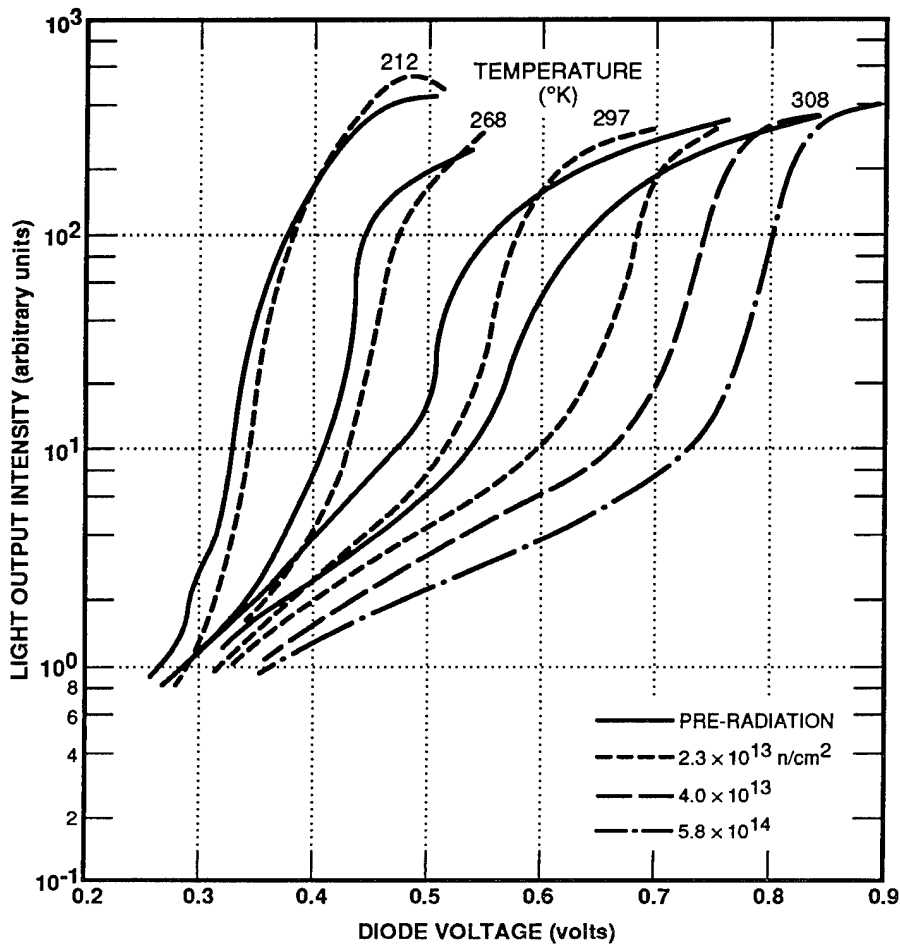


Figure 4-49. Neutron-induced degradation of 1.25-mm InGaAsP laser diodes (Barnes, 1982).

photocurrent. Since the p-region is relatively lightly doped, the space-charge region will extend well into the p-region so that the collection of photogenerated carriers will be significant over the range including the space-charge region and approximately one to two diffusion lengths into the p-region. It follows that under operation at reverse bias, the total current is the sum of the space-charge-region drift current density J_{sc} (A/cm²), which can be written as (Sze, 1981)

$$J_{sc} = q\phi_{ph} \left(1 - e^{-\alpha w} \right) + \frac{qn_i w}{\tau_{sc}}, \quad (4.73)$$

where

- ϕ_{ph} is the incident photon flux emanating from the fiber or ILD (or LED)
- α is the absorption coefficient for silicon
- n_i is the intrinsic electron density

- w is the width of the space-charge region
- τ_{sc} is the carrier lifetime in the space-charge region.

The diffusion current density J_d (A/cm²) can be written (Sze, 1981)

$$J_d = q\phi_{ph} \left[1 - \frac{e^{-\alpha w}}{(1 + \alpha L_n)} \right] + qn_{p0} \frac{D_n}{L_n}, \quad (4.74)$$

where L_n is the electron diffusion length ($= \tau_0 D_n$), n_{p0} is the equilibrium electron density on the p-side of the junction, and D_n is the electron diffusion coefficient.

The fraction of the total photocurrent due to J_{sc} will depend on the doping level in the p-region, the applied bias, the value of L_n , and

the absorption coefficient α at the wavelength of the incident light. While the field-induced collection of carriers contributing to J_{sc} occurs very rapidly under saturated drift conditions, the collection of the diffusing carriers is much slower, especially for large L_n (or τ_o). In addition, note that the photocurrent portion of J_d depends on τ_o , but that of J_{sc} does not. Therefore, J_d is more susceptible to radiation degradation than is J_{sc} , due to the sensitivity of the minority-carrier lifetime to radiation-induced lattice damage. Consequently, to construct a fast, radiation-insensitive detector, J_d should be minimized and J_{sc} should be maximized.

Hardening photodiodes by minimizing diffusion-limited collection and maximizing collection within the depletion region also introduces the need for compromise because a wide depletion region requires that the silicon in this region be lightly doped [this compromise is not nearly as severe for III-V-based photodiodes; see below]. Under such a condition, neutron irradiation can lead to carrier removal and mobility degradation, leading to increases in series resistance at relatively low fluences (although not as low as fluences that will significantly reduce the minority-carrier lifetime). A recent study by Korde *et al.* (1989) has shown that significant increases in series resistance can occur above 10^{12} -n/cm² fluence levels and that these changes affect the linearity of the photodiode.

A similar analysis can be applied to the use of phototransistors in a radiation environment. Phototransistors are attractive because they possess internal gain. However, because adequate transistor gain depends on a satisfactory value of the minority-carrier lifetime in the base region of the phototransistor, these devices are very sensitive to radiation-induced recombination centers within this region. Experiments [see Figure 4-50] have verified the dramatic difference in photocurrent sensitivity to radiation damage between detectors that depend on diffusion-limited collection, such as phototransistors, and those that do not, such as fully depleted PIN photodiodes. As indicated in Figure 4-50, in contrast with the lack of any effect of neutron-induced damage on the PIN photodiode to fluences in ex-

cess of 1×10^{14} n/cm², the phototransistor shows significant degradation in photocurrent even below 1×10^{12} n/cm² because of the long minority-carrier lifetime in the base region. However, more recent efforts have resulted in hardening silicon bipolar phototransistors to the point where they can be used at fluences above 10^{13} n/cm². In the optically active region of the hardened phototransistor, diffusion-limited collection was minimized in favor of collection in the depletion layer through proper design. The neutron-induced degradation of gain in the transistor portion was minimized by employing a very narrow base region width. The resulting phototransistor performance for this hardened design is shown in Figure 4-51. Note that the phototransistor light output current decreases about 55 percent after 10^{13} n/cm² at an irradiance of 5 mW/cm². Comparison of this value with the normalized current transfer ratio in Figure 4-50 for an earlier unhardened phototransistor demonstrates considerable improvement in the device hardness.

Detector structures whose responsivity does not depend on diffusion-limited collection of photogenerated carriers are not, however, completely immune to radiation damage degradation. Previous studies by Lischka *et al.* (1991), Korde *et al.* (1989), Kalma and Hardwick (1978), and Lemeilleur *et al.* (1991) have shown that irradiation-induced leakage (dark) currents are observable at neutron fluences that do not significantly affect the responsivity. These dark currents result from radiation-induced increases in the bulk density of nonradiative recombination centers in the depletion region, and from radiation-induced surface effects. The bulk leakage current density is

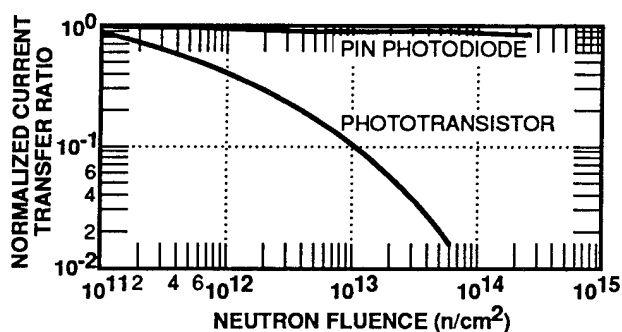


Figure 4-50. Neutron damage in two types of photo-detectors (Soda, Barnes, and Kiehl, 1975).

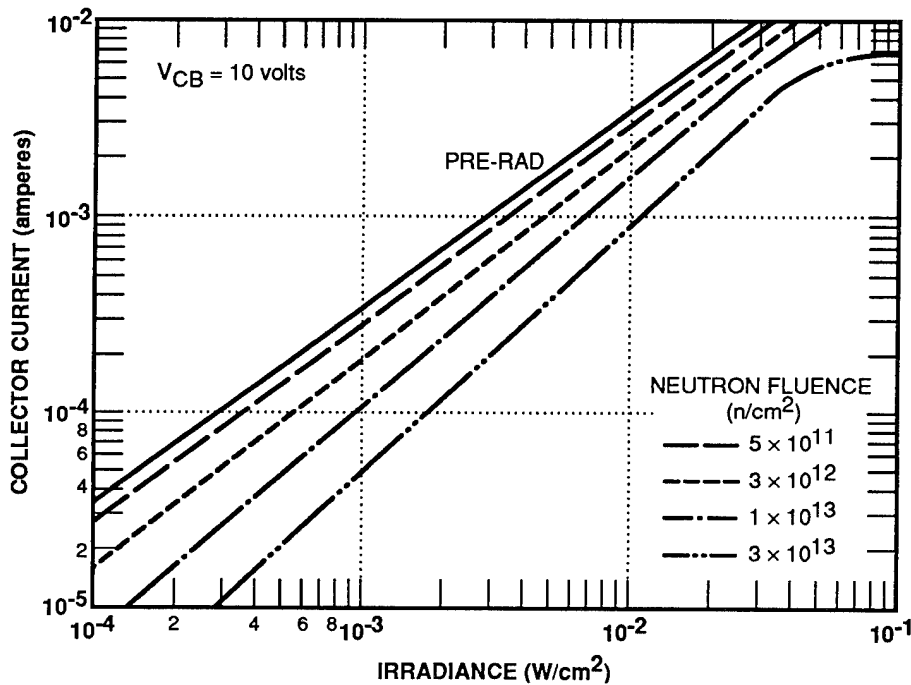


Figure 4-51. Phototransistor light current as a function of irradiance after neutron irradiation (Matzen, Hawthorne, and Kilian, 1991).

given by the second term in Equation 4.73 where τ_{sc} decreases with increasing radiation-induced recombination center density in the space-charge region. Experimental evidence also shows, however, that the leakage currents in PIN photodiodes due to neutron damage do not become significant until fluences $>1 \times 10^{14}$ n/cm² are reached. Lattice-damage-induced increases in dark currents also lead to changes in shunt resistance of photodiodes (Korde *et al.*, 1989). Neutron irradiation can also change capacitance-voltage (C-V) characteristics of photodiodes, which will affect speed performance (Li and Kraner, 1991).

While the above comments on lattice damage effects in detectors indicate that problems can be avoided by using PIN photodiodes, the issue of transient ionization effects on detectors is much more difficult. This is not particularly surprising since photodetectors are specifically designed to efficiently convert electromagnetic energy, whether a 1.3- μ m signal photon or a high-energy gamma ray, into electrical current. Indeed, in those fiber-optic links where the fiber is relatively short, ionization-induced photocurrents in

the photodiode can be the most severe radiation effects problem for the entire link.

Heterostructures using III-V material provide an alternative to silicon for the fabrication of photodiodes. Figure 4-52 shows the structure of a typical AlGaAs/GaAs radiation-hardened photodiode on a 38° μ m substrate. As indicated by the right-hand scale, all of the layers above the substrate are less than 1.0 μ m thick. The active region of the photodiode is the silicon-doped n-type GaAs layer, which is about the same thickness (0.7 μ m) as the absorption length (1.0 μ m) in GaAs at room temperature and at the operating wavelength of 0.82 μ m. The silicon doping level of this layer is chosen so that the entire region is depleted at the operating bias of a few volts, thus ensuring collection of all the optically generated carriers. Interposed between the active region and the GaAs substrate is a buffer layer to reduce the effect of substrate defects and impurities, and an AlGaAs isolation layer. The steps in the energy bands at the heterostructure interface between the AlGaAs isolation layer and the GaAs are such that the collection of minority holes, created by radiation in the GaAs buffer

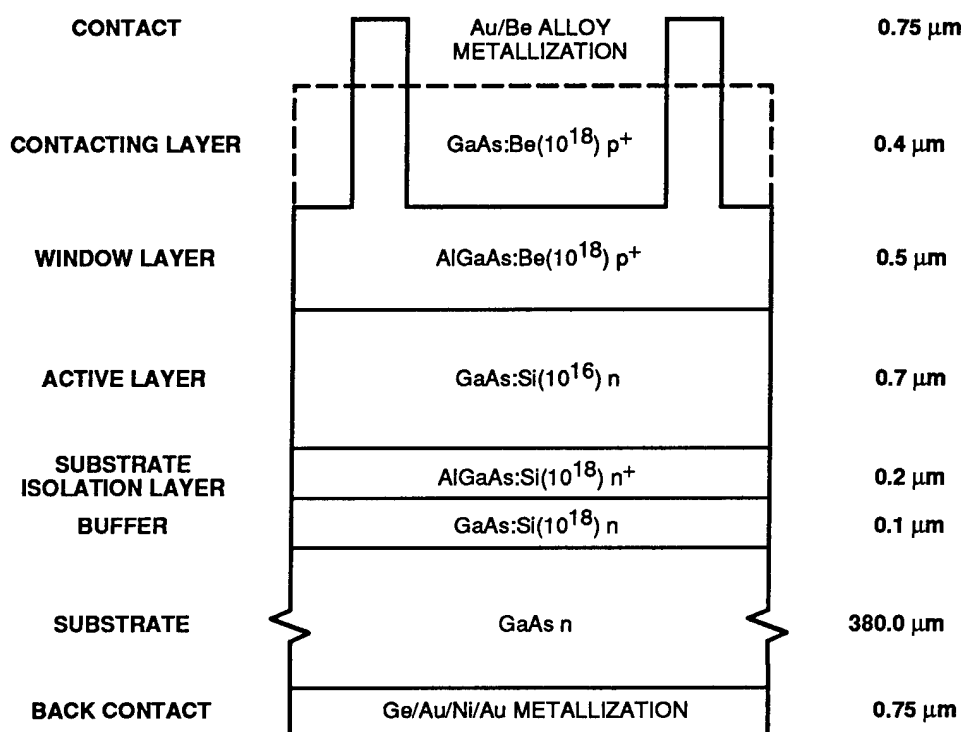


Figure 4-52. Heterolayer structure of an ionizing-radiation-hardened AlGaAs/GaAs photodiode (Wiczler *et al.*, 1984).

layer and substrate, is blocked by the electric field at the step. The purpose of the upper AlGaAs layer is to serve primarily as a window to the incoming optical signal and thereby protect the active region from surface recombination and surface deterioration. The optical photons pass through this layer since the energy gap of the AlGaAs is too large to result in significant absorption within the layer.

Several radiation studies (Wiczler *et al.*, 1982, 1984; Wiczler and Barnes, 1985) have been conducted that include ^{60}Co ionizing radiation dose and dose-rate exposures, neutron irradiations, high-dose-rate flash x-ray exposures, and high-energy pulsed electron irradiations on photodiodes similar in structure to that shown in Figure 4-52 and fabricated in different III-V material families. The III-V photodiodes were also found to be less sensitive to neutron irradiation in terms of neutron-induced degradation of the responsivity and neutron-induced increases in leakage current. Thus, the hardened III-V photodiodes are superior to silicon detectors in several

ways and should be used in those applications requiring exposure to radiation.

4.7.4 Optical Fibers

The most important property of optical fibers with respect to radiation is the absorption of light in the core of the fiber by various types of color centers, many of which are present prior to radiation. Almost all reports of steady-state, radiation-induced attenuation in fibers have used gamma-ray sources such as ^{60}Co , or to a much lesser extent ^{137}Cs , while transient studies have used pulsed x-ray or electron machines. However, the space environment consists of electrons, protons, and cosmic rays, and a valid concern is how laboratory measurements using ^{60}Co sources simulate the damage a fiber-optic waveguide would experience in space. Several studies of neutron-irradiated fibers have been undertaken, including both filtered reactor exposures to minimize the gamma-ray component of the flux (Schneider, 1982) and 14-MeV neutrons from deuterium-tritium reactions (Mattern *et al.*,

1975). Computations have shown that for $\sim 10^{12}$ to 10^{15} -n/cm² fluences, most of the kinetic energy deposited in the fiber is converted to ionizing processes; a neutron fluence of 10^{12} n/cm² (1-MeV neutrons) was found to be equivalent to an ionizing radiation dose of 2,000 rads. The computed ionizing dose was then used for comparing neutron and gamma-ray results, and the optical absorptions induced by equivalent neutron and ionizing doses were found to be quite similar. Although there seems to be an equivalence for pure silica core fibers, there has been one report of greater damage in silica with increasing neutron content in mixed field exposures (Schneider, 1982) and greater sensitivity to neutrons in Ge-doped silica core fibers (Schneider and Babst, 1984).

To investigate the effects of different types of irradiation, several different pure and Ge-doped silica core fibers were exposed to ⁶⁰Co-gamma irradiations, mixed neutron-gamma fields from a reactor, and energetic protons from a cyclotron (Gingerich *et al.*, 1987). As shown in Figure 4-53(a), the damage produced by gamma rays and protons was virtually identical in pure silica. In ITT rad-hard Ge-doped silica core fibers [Figure 4-53(b)], protons produced *somewhat* more damage than gamma rays; and in the Corning 1519 fiber [Figure 4-53(c)], protons produced *considerably* more damage than gamma rays. Although the high loss in the proton-irradiated Corning 1519 sample is likely due to microbending losses in the fiber during the measurement, such microbending cannot explain the appearance of a notable absorption band at 1 μ m, which is not evident in the reactor-irradiated fiber. An additional concern is the loss that might be added to the waveguide from protons that are captured in the fiber core and then bond with the network atoms, forming Si-OH. Such hydrogen-induced aging, which has been observed in submarine cables, can cause substantial increases in the attenuation near 1.3 and 1.5 μ m (Lemaire, 1991).

Unfortunately, few studies of proton-irradiated optical fibers have been undertaken to fully characterize their response, and it is too early to conclude that gamma-ray and proton exposures are

equivalent. Rather, it appears that neither mixed gamma-neutron fields nor gamma-ray sources adequately simulate the effects of proton irradiation of doped silica core fibers, although there is good correspondence in the case of pure silica core waveguides.

4.8 Displacement Damage Effects on Silicon Sensor Arrays

Two types of optoelectronic sensors affected by displacement damage are charge-coupled devices (CCDs) and charge-injected devices (CIDs). Basically, these devices consist of two-dimensional arrays of MOS capacitors where each capacitor serves as a sensing element or pixel that provides a current (or charge) proportional to the light intensity impinging on each of the elements or pixels.

For the CCD, readout of the induced light or charge pattern is accomplished by a succession of charge transfers until the charge packet for each pixel is sensed by a readout amplifier. The charge transfer efficiency (CTE) is defined as one minus the fraction of charge lost as a charge packet is transferred to the next pixel. Thus, due to the sensing method, the CTE of each transfer is of major importance. For modern large ($4,096^2$), high-performance CCD arrays, CTEs greater than 0.99999 are required.

The readout mechanism for the CID is accomplished by measuring the voltage change induced by transferring the charge between two capacitors. Through the use of a random-access readout, which reduces the number of charge transfers to two, CTE losses are drastically reduced. However, due to high-readout capacitance, array size is limited (e.g., $\cong 512^2$). These devices have been developed for a wide variety of military and scientific satellite applications in addition to their use in a variety of tactical applications.

Displacement damage effects in these types of sensors can manifest themselves in two ways: (1) loss of CTE, and (2) increased leakage or dark current. Each of these failure modes is discussed here (Dale and Marshall, 1992; Dale *et al.*, 1993).

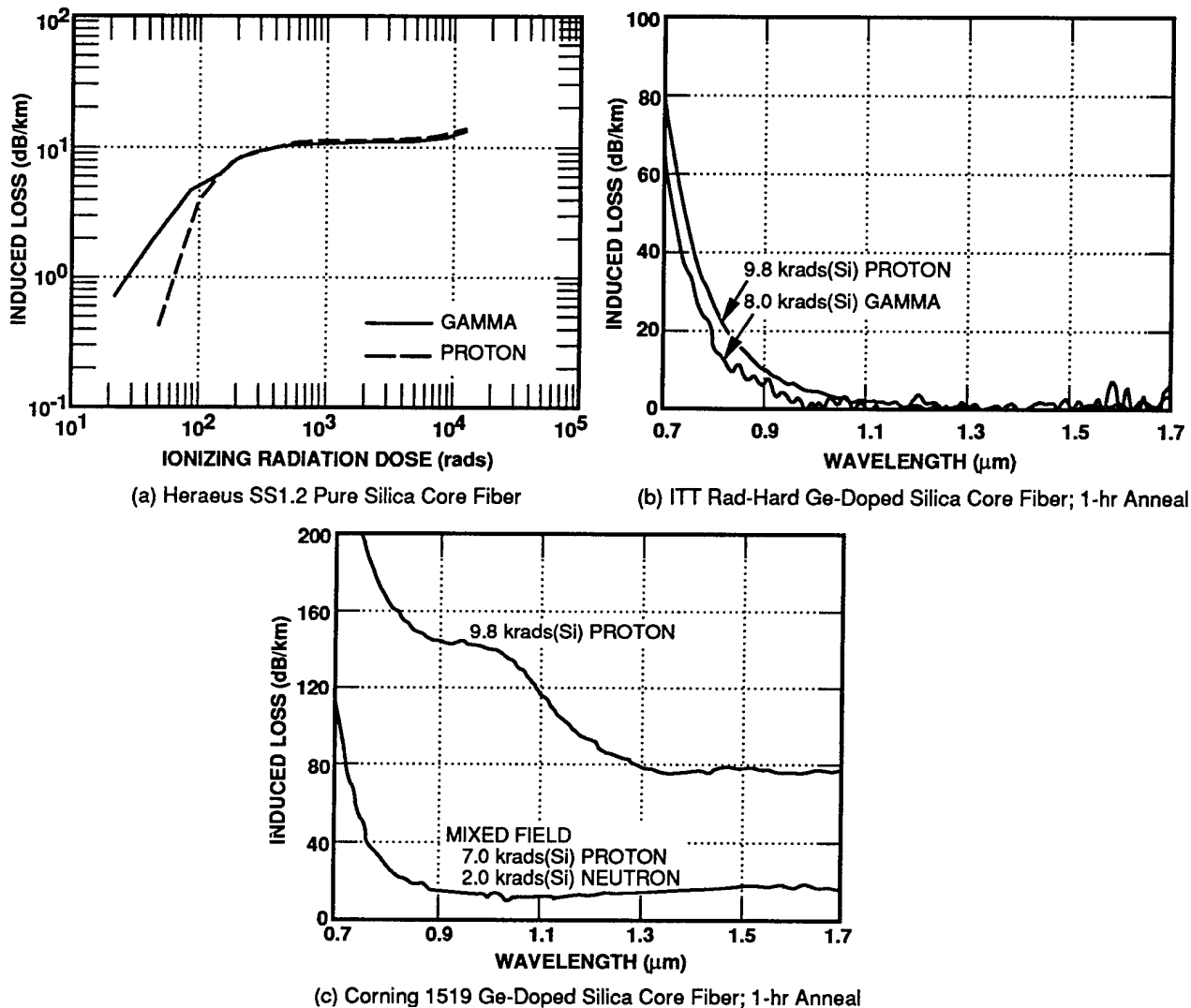


Figure 4-53. Effect of different radiation types on optical fibers (-30 dBm of 0.85 -mm optical signal during exposure); $T = 23^{\circ}\text{C}$ (Gingerich *et al.*, 1987).

4.8.1 CTE Degradation

As array size and performance requirements continue to increase, CTE degradation will become an increasingly serious problem. The actual CTE loss for a given irradiation is a function of many factors, e.g., temperature, signal magnitude, clock speed, and clock overlap. However, through the use of an equivalent damage factor $K(E)$, the concept of non-ionizing energy loss (NIEL) [see Subsection 4.3.2.3] and the observation that CTE tends to degrade linearly with particle fluence over certain energy ranges, the overall problem of analyzing CTE displacement damage degradation can be made tractable.

The basic approach (Dale *et al.*, 1993) is to first determine the damage factor(s) proportional to NIEL over the relevant energy ranges, $K(E) = C \cdot \text{NIEL}(E)$, where the experimental constant C can be evaluated experimentally at any energy E and would hold for all energies within the range of interest. Next, the radiation response at each particle energy level is characterized. Note that in order to superimpose the damage contributions for the different energies, a linear CTE change with particle fluence over the energy range of interest must be established. This will allow the radiation response to be characterized by a unique damage factor at each energy level as

$\Delta\text{CTE} = K(E) \cdot \Phi(E)$. An example of this characterization process is provided in Figure 4-54, where proton damage factors are plotted based on CASSINI Ford test data on a 1,024² CCD. Note that the damage factors shown have been scaled to coincide with NIEL at 1 MeV; i.e., normalization factor = 1.2×10^{-11} [$\Delta\text{CTE} \cdot \text{g}(\text{Si}) / \text{MeV}$]. The energy-dependent damage factor ($K[E]$) is then combined with the particle spectrum anticipated at the CCD. A differential proton spectrum is provided in Figure 4-55 [continuing with the CASSINI example provided in Figure 4-54], which corresponds to the daily proton contribution through various shield thicknesses in the Hubble Space Telescope (HST) orbit during a solar minimum. The effect of aluminum shielding in decreasing the number of the more damaging low-energy protons is evident from this figure. The product of the differential proton spectrum of Figure 4-55 and the NIEL produces the differential damage shown in Figure 4-56. Finally, the differential damage spectra of Figure 4-56 is integrated from infinity to the energy of interest. The intercepts at zero energy give the daily total non-ionizing energy deposition by protons of all energies using

$$\begin{aligned} \Delta\text{CTE} &= \int_0^{\infty} K(E) \frac{d\Phi(E)}{dE} dE \\ &= \int_0^{\infty} C \cdot \text{NIEL}(E) \frac{d\Phi(E)}{dE} dE \end{aligned} \quad (4.75)$$

For the example, the daily changes in CTE are 7.0×10^{-7} , 2.3×10^{-7} , and 1.3×10^{-7} [see Figure 4-57]. As a final note, CTE degradation as a function of time for the HST orbit is shown in Figure 4-58. The corresponding proton doses [in rads(Si)] are estimated on the right-hand ordinate of the figure; however, the CTE degradation observed is actually due to NIEL rather than ionizing energy loss. As can be seen, significant CTE loss is anticipated over the HST missile life due to the natural environment.

For the example given above, a number of caveats (Dale *et al.*, 1989) are appropriate:

- NIEL may be overestimating the CTE degradation expected from high-energy protons, to the extent that recoil equilibrium ceases to exist. Moreover, if damage factors measured above 30 MeV are used to define an “effective NIEL” for CTE estimates, the daily change in CTE is about one-half of the value calculated for the thickest shield.
- Measurements were taken at -50°C , using the ⁵⁵Fe x-ray technique
- All predictions were based on damage factors measured at 50-kHz readout frequency.
- Less degradation will result at lower temperatures and with a faster readout (for this size image). Less degradation will also be seen for larger signal packets.

4.8.2 Radiation-Induced Dark-Current Behavior

Increases in dark, or leakage, currents in CCDs are the result of displacement damage caused by neutrons, protons, and/or heavy ions, which produce generation centers in the depletion region of the pn junctions comprising the sensors. These dark currents occur in two ways: (1) an average overall increase in the level of the bulk leakage current, which can be understood from an NIEL analysis based on the global radiation exposure; and (2) dark-current spikes, which are attributed to very high localized electric fields (Dale *et al.*, 1989).

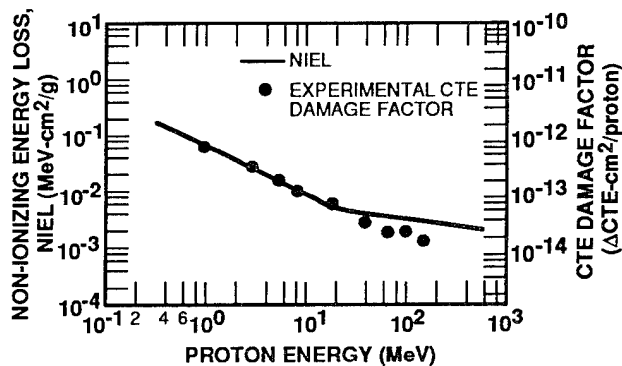


Figure 4-54. Proton damage factor based on CASSINI test data (Dale, 1992).

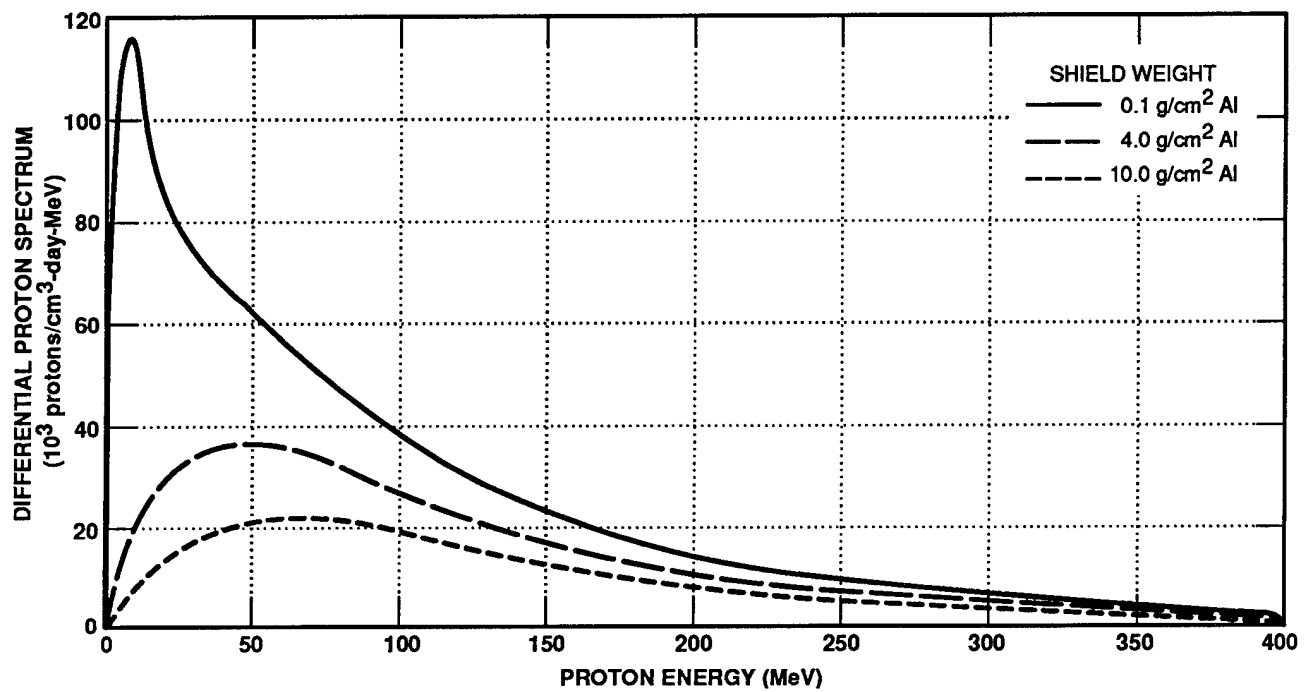


Figure 4-55. Differential proton spectrum; daily proton contribution through various shield thicknesses in the Hubble Space Telescope during a solar minimum; 593-km, 28.5-degree orbit (Dale and Marshall, 1992; Dale *et al.*, 1993).

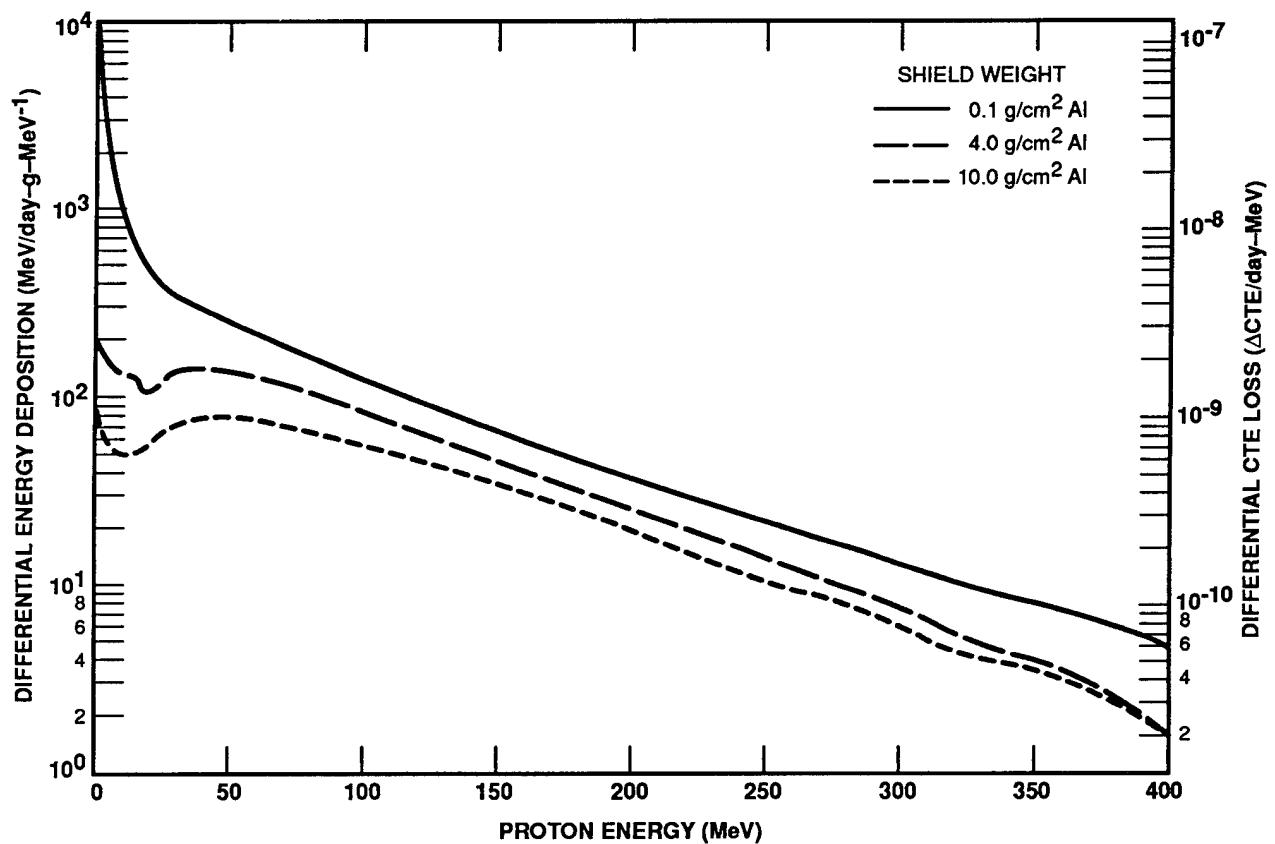


Figure 4-56. Differential damage spectra for the Hubble Space Telescope during a 593-km, 28.5-degree orbit (Dale and Marshall, 1992; Dale *et al.*, 1993).

4.8.2.1 Radiation-Induced Dark-Current Increases Produced by Bulk Generation Centers

Dark-current increases produced by bulk generation centers can be understood by examining the thermal generation rate of current in the depletion region of a pn junction. The thermal generation rate G in a depletion region is given by:

$$G = -n_i/\tau_g \quad (4.76)$$

where n_i is the intrinsic carrier concentration and τ_g is the generation lifetime. The thermal generation (or dark) current density J_d due to a depletion of width W is given by

$$J_d = \int_0^W q/G/dx \cong q/G/W = qn_i W/\tau_g \quad (4.77)$$

where q is the electronic charge. (The approximation is due to the assumption of a uniform generation rate over the entire depleted region.) Radiation-induced displacement damage introduces generation centers in depletion regions that degrade τ_g and thereby enhance the thermal generation rate. This degradation process can be expressed as

$$(1/\tau_g) = (1/\tau_{go}) + (\Phi/K_g) \quad (4.78)$$

where τ_g is the post-irradiation value of generation lifetime, Φ is the bombarding particle fluence, and K_g is the generation-lifetime damage coefficient. Substituting Equation 4.78 into Equation 4.77,

$$J_d = qn_i W \left[\left(\frac{1}{\tau_{go}} \right) + \left(\frac{\Phi}{K_g} \right) \right] = J_{do} + \frac{qn_i W \Phi}{K_g} \quad (4.79)$$

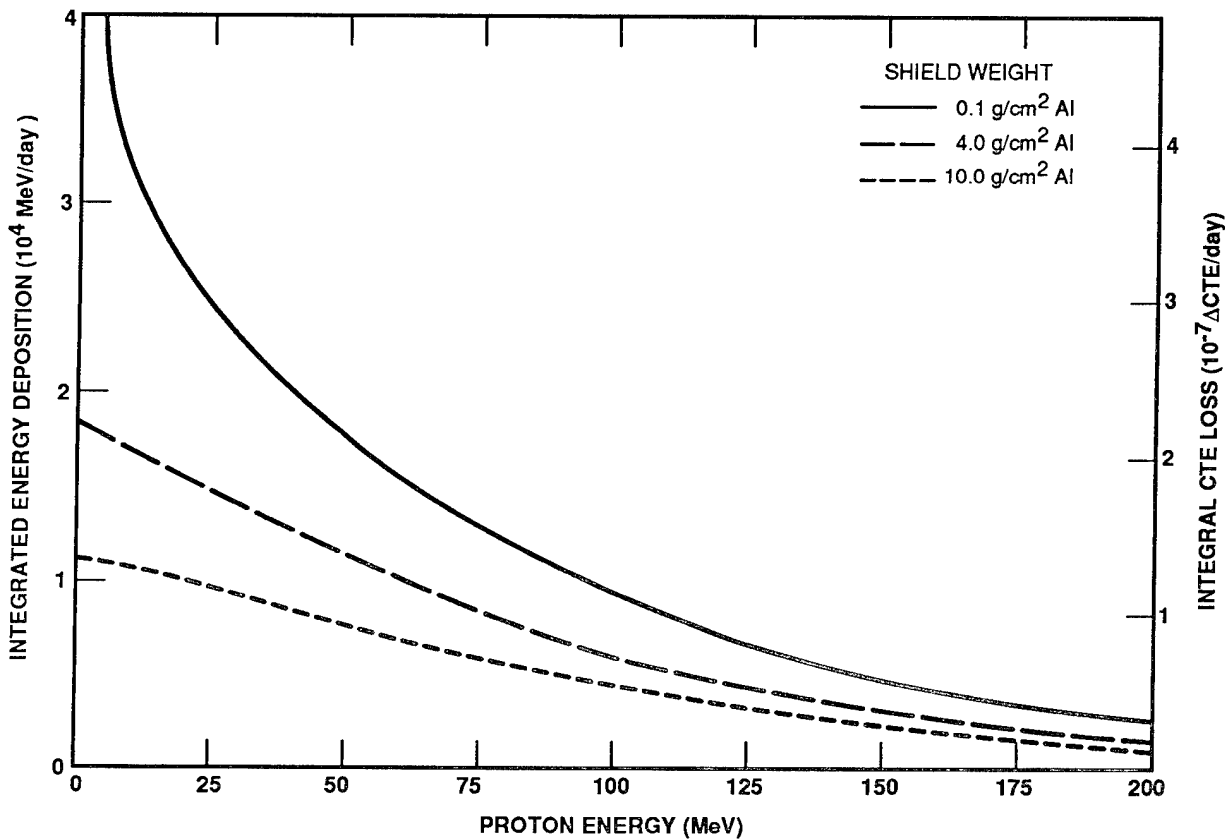


Figure 4-57. Daily changes in CTE for the Hubble Space Telescope during a 593-km, 28.5-degree orbit (Dale and Marshall, 1992; Dale *et al.*, 1993).

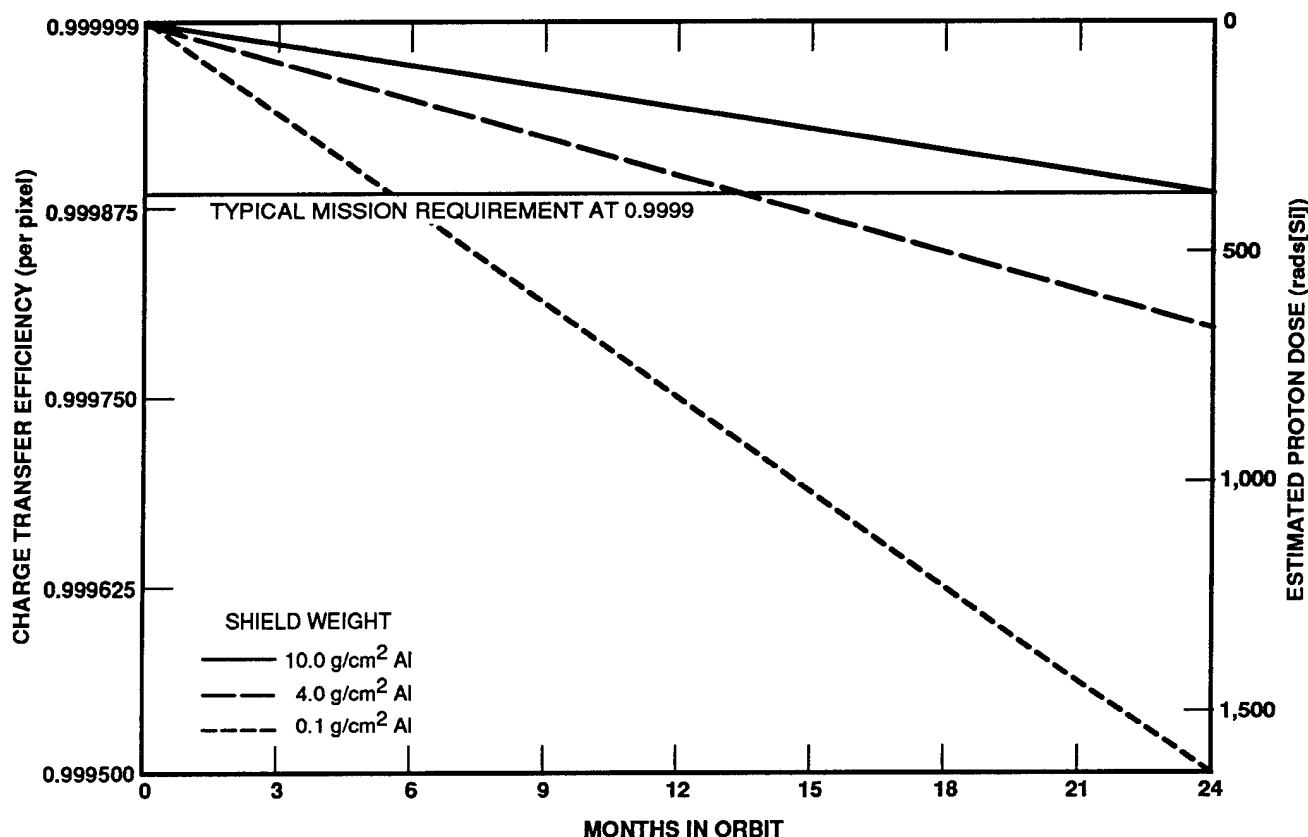


Figure 4-58. CTE degradation for the Hubble Space Telescope as a function of spacecraft time in orbit; 593-km, 28.5-degree orbit (Dale and Marshall, 1992; Dale *et al.*, 1993).

where J_{do} is the pre-irradiation value of dark-current density. Thus, the radiation-induced change in dark-current density is given by

$$\Delta J_d = J_d - J_{do} = \frac{q n_i W \Phi}{K_g} \quad (4.80)$$

If K_g is known for a given particle type and particle energy, then Equation 4.80 can be used to calculate the radiation-induced dark-current density at any fluence of interest. Values of K_g for neutrons have been determined by various researchers and a number of these values are shown in Table 4-6.

An example is given here to illustrate the applicability of calculating neutron-induced changes in dark-current density using Equation 4.80. Figure 4-59 shows the increase in dark-current density produced by fission-neutron bombardment of a buried-channel CCD. Results of

calculations using Equation 4.80 are also shown, and agreement with experiment is quite good. To perform these calculations, the MOS-derived K_g value of 1.4×10^7 n-sec/cm² was employed. The mean dark-current damage factors as well as their variance were studied in CID arrays for both proton and neutron exposures (Dale *et al.*, 1989).

The present state of knowledge is sufficient to permit reasonably accurate dark-current predictions for any neutron-irradiated silicon device. If the mean K_g value for bipolar devices in Table 4-6 is averaged with the MOS value, the following results are obtained:

$$K(\text{fission}) = 2.6 \times 10^7 \text{ n-sec/cm}^2$$

$$K_g(14\text{-MeV}) = 1.1 \times 10^7 \text{ n-sec/cm}^2.$$

These mean damage coefficients are accurate to within ± 50 percent. Combining these values with Equation 4.80 yields the following relations

for the mean neutron-induced dark current per unit volume due to generation centers in silicon depletion regions:

$$\Delta I_{dv}(\text{fission}) = 9 \times 10^{-17} \Phi_n \text{ A/cm}^3 \quad (4.81)$$

$$\Delta I_{dv}(14\text{-MeV}) = 2 \times 10^{-16} \Phi_n \text{ A/cm}^3. \quad (4.82)$$

Figure 4-60 shows plots of these equations as a function of fluence.

The use of Equations 4.81 and 4.82 is straightforward in practice. Depletion region dimensions for the device or circuit of interest must be obtained and then the displacement-damage-induced dark current (ΔI_d) at a given fluence can be readily calculated. Additionally, as discussed in Subsection 4.3.2.3, through the concept of NIEL, this approach can be extended to other particle types at various energies.

4.8.2.2 Dark-Current Spike (Single-Particle) Effects

Subsection 4.8.2.1 addressed the situation where a relatively high particle fluence, i.e., a fluence large enough to produce many primary

interactions between incident particles and silicon atoms in a specific depletion region exists. However, if the particle fluence is reduced so that only one primary interaction is expected, the issue of how large the dark-current increase would be arises. [Note that one primary interaction can produce many individual defects, particularly in the case of fast-neutron bombardment.] This issue has been explored experimentally for incident 14-MeV neutrons and 99- and 147-MeV protons (Srou, Hartmann, and Kitazaki, 1986) using a CCD as a test vehicle. Key findings of those studies are reviewed here.

Using the generation rate definition given by Equation 4.76, the average increase in dark-current density produced by a single-particle interaction in a device depletion region can be expressed as (Srou, Hartmann, and Kitazaki, 1986; Srou *et al.*, 1983)

$$\overline{\Delta J_{dl}} = q n_i / 2AK_g N \sigma_t \quad , \quad (4.83)$$

where A is the area of the depletion region, N is the average atomic density ($5 \times 10^{22} \text{ cm}^{-3}$ for

Table 4-6. Values for generation lifetime damage coefficient obtained from measurements performed on neutron-irradiated silicon devices by various investigators.

Investigators	Type of Neutron Radiation	Damage Coefficient K_g (n-sec/cm ²)	Device
Fitzgerald and Snow (1968)	Fission	4.0×10^7	p+n gate-controlled diodes
Larin (1968)	Fission	4.5×10^7	nnp mesa transistors
Kawamoto and Oldham (1970)	Fission	4.0×10^7	p+n gate-controlled diodes
Gregory and Gwyn (1970)	Fission	2.6×10^7 3.7×10^7	2N5004 (nnp planar) 2N5005 (pnp planar)
Srou <i>et al.</i> (1978) ^a	Fission	1.4×10^7	MOS capacitors
Kern and McKenzie	14.8-Mev	1.7×10^7	JFETs (2N4416)
Holmes, Wilson and Blair (1972) ^a	14-MeV	1.5×10^7	pn junction diodes (vidicon)
Srou <i>et al.</i> (1981) ^a	14-MeV	6.2×10^6	MOS capacitors

Note:

^a The footnoted investigators assumed $G = -n_i/2\tau_g$. The K_g values given here are a factor of two larger than the value they obtained. This correction was applied so all damage coefficients in this table could be compared directly; i.e., all were determined using $G = -n_i/\tau_g$, which is the correct approach.

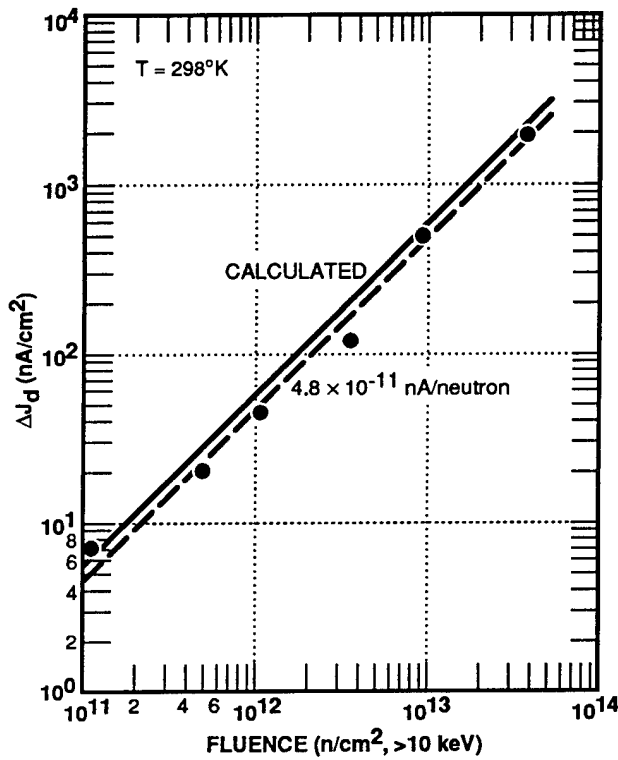


Figure 4-59. Change in dark-current density for a neutron-irradiated charge-coupled device compared to model calculation results ($K_g = 1.4 \times 10^7$ n-sec/cm²) (Srou, 1988).

silicon), and σ_t is the total interaction cross section. Equation 4.83 yields an average increase in dark-current density because the damage coefficient K_g is only applicable for the case of the interactions in a given depletion region. Incident particles, such as 14-MeV neutrons, will produce primary knock-on atoms having a spectrum of energies (Glassgold and Kellogg, 1958). A single-particle interaction will produce a knock-on with some specific energy within that spectrum. The damage coefficient is a measure of the effects of a primary recoil having the mean energy for a particular recoil spectrum.

The effect of a single-particle interaction in causing displacement damage is shown in Figures 4-61 and 4-62 for a Texas Instruments' TC104 3,456-element linear image sensor. Figure 4-61 shows the change in dark-current density, measured following 14-MeV neutron bombardment. After a fluence of 1×10^7 n/cm², two cells exhibited an increase, as shown in Figure 4-61(a). At that fluence, only two to three

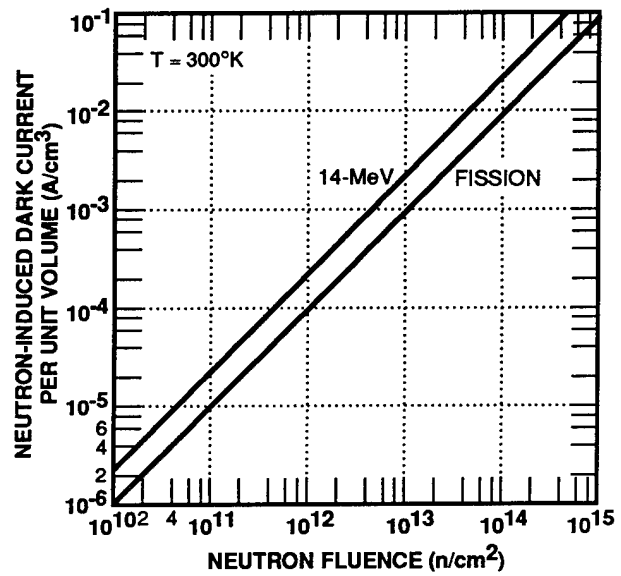
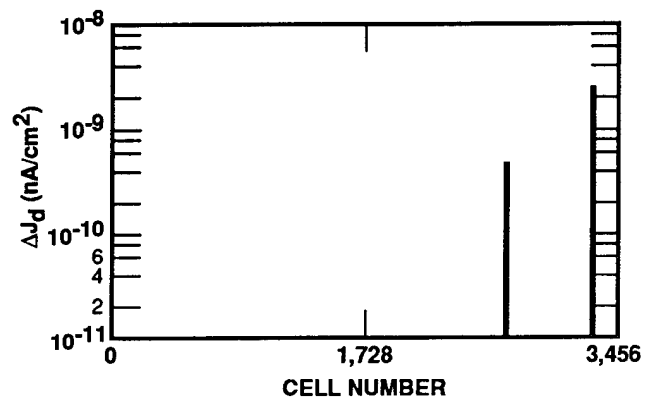
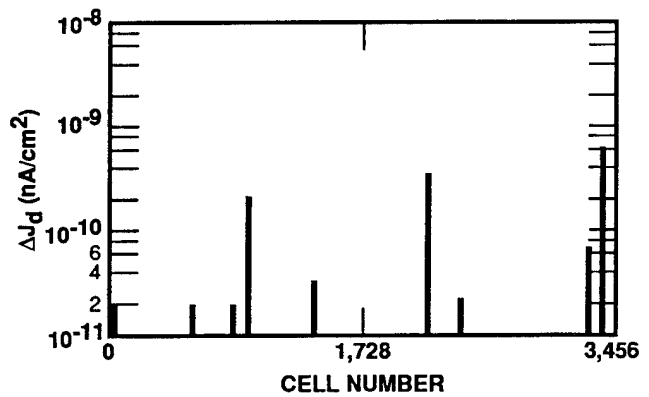


Figure 4-60. Neutron-induced dark current per unit depletion region volume for silicon devices versus neutron fluence (Srou, 1988).



(a) $\Phi = 1 \times 10^7$ n/cm²



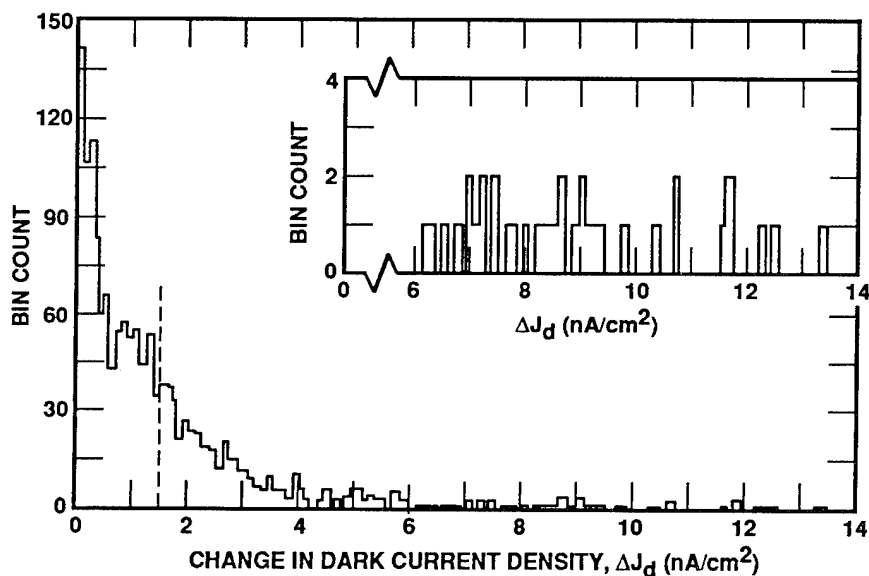
(b) $\Phi = 3 \times 10^7$ n/cm²

Figure 4-61. Measured change in dark-current density produced by single 14-MeV neutron interactions (Srou, 1988).

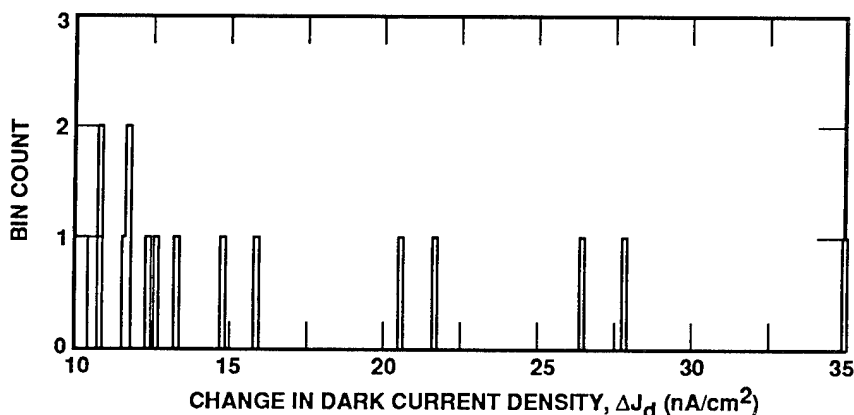
primary interactions were expected in the CCD depletion regions, which agrees with the measurements. Thus, the effects produced by single neutron interactions were observed. Figure 4-61(b) shows nine newly damaged cells observed after a fluence of 3×10^7 n/cm².

Figure 4-62 shows the distribution of damage events measured after a fluence of 1×10^{10} n/cm². Note the relatively long tail to the distribution, consisting of large-amplitude events. The number of damaged CCD cells contributing to the distribution in Figure 4-62 is 1,389. Multiple interactions occurred in some cells, and Poisson distribution can be used to determine the total

number of primary interactions (Srou, Hartmann, and Kitazaki, 1986; Srou and Hartmann, 1985), with a result of 1,776 interactions. Using the mean measured value of ΔJ_d in Figure 4-62, an experimental value for the average change in dark-current density per primary interaction (ΔJ_{dt}) of 1.2 nA/cm² is obtained. Equation 4.83 yields a calculated value for $\overline{\Delta J_{dt}}$ of 1.3 nA/cm² by using the mean K_g value of 1.1×10^7 n-sec/cm² previously provided. The very good agreement between measurements and calculations indicates that this mean damage coefficient value is quite appropriate for determining the effects of 14-MeV neutron bombardment.



(a) Distribution from 0 to 14 nA/cm²



(b) Distribution from 10 to 40 nA/cm²

Figure 4-62. Measured distribution of new damage events after 1×10^{10} n/cm² fluence; mean value of entire distribution is 1.5 nA/cm² [inset in Part (a) is an expanded ordinate scale, given for clarity] (Srou, 1988).

Another finding observed in virtual-phase CCDs and CIDs involves leakage currents associated with high electric fields within depletion regions. When radiation damage occurs in field regions exceeding 10^5 V/cm, an enhanced emission of carriers results and the localized currents can be extremely high. Electric-field-enhanced emission has been shown to be responsible for the largest leakage currents measured in some radiation-damaged detector arrays (Corbett, 1966; Lindhard, Scharff, and Schiott, 1963; Mayer, Eriksson, and Davies, 1970; Tada *et al.*, 1982). This appears to be less of a problem for buried-channel CCDs.

Some pixels will exhibit much higher dark currents and much larger CTE changes than their neighbors, and a detailed study has quantified both the magnitudes and frequencies of these rare events using extreme value statistics (Marshall *et al.*, 1989; Marshall, Dale, and Burke, 1990). This description shows that the rare damage events exceed the average by factors ranging from 2 to 3 orders of magnitude, and occur with probabilities of 10^{-2} to 10^{-3} per interaction, depending on proton energy. As with average damage, calculations based on NIEL show excellent agreement with measured dark-current spike distributions.

4.8.2.3 Dark Current Annealing

Long-term annealing of displacement damage in silicon devices occurs even at room temperature and can vary significantly from case to case. A basic understanding is lacking, so measurements relevant to a particular part are important. A 30 percent reduction in the average proton-induced dark-current increase for silicon CIDs has been observed over a period of several months at room temperature. Other groups have reported limited annealing measurements for various CCDs (Hopkinson and Chlebek, 1989; Srour, Hartmann, and Kitazaki, 1986). Although the E-center (a phosphorus-vacancy complex) has been suspected to be the cause of parallel CTE loss, this was illustrated most convincingly in Robbins, Roy, and Watts (1991) and IPCS (1991), where it is shown through annealing

studies that 80 percent of the CTE loss was attributable to the E-center.

4.8.2.4 Radiation-Hardening Approaches

The reduction or elimination of radiation-induced changes in dark current is an important issue. One straightforward approach in principle is to reduce the device operating temperature. In practice, however, device functionality at reduced temperatures and other constraints imposed by the specific electronic subsystem need to be considered (Srour, 1988). Consider the example of a neutron-irradiated silicon CCD. At room temperature, the post-irradiation dark current is due to neutron-induced generation centers in depletion regions in a CCD, as illustrated by Figure 4-59. Referring to Equation 4.80, the temperature dependence of neutron-induced dark current is dominated by that of n_i , since K_g is only weakly dependent on temperature (Srour *et al.*, 1978). The dramatic reduction in dark current that can be achieved by lowering the operating temperature is due to the strong temperature dependence of the carrier generation rate (proportional to n_i). Figure 4-63 illustrates the effectiveness of lowering the operating temperature of a CCD to avoid neutron-induced dark-current problems. As an example, assume that the maximum post-irradiation normalized dark-current density that can be tolerated is unity, which is the pre-irradiation value of J_{d0} at 303°K in Figure 4-63. If the expected fluence is 10^{13} n/cm², then this figure indicates that operating the device at $T \leq 268^\circ\text{K}$ will keep J_d equal to or less than unity following irradiation. Thus, a relatively moderate lowering of the operating temperature will result in substantial radiation tolerance in terms of neutron-induced increases in dark current. This conclusion applies for any silicon device in which the leakage current increase produced by bombardment with any particle is attributable to radiation-induced generation centers in device depletion regions.

A brief summary of displacement-damage radiation-hardening methods that are currently in use or are being investigated follows. In general, no one solution is satisfactory and, in practice,

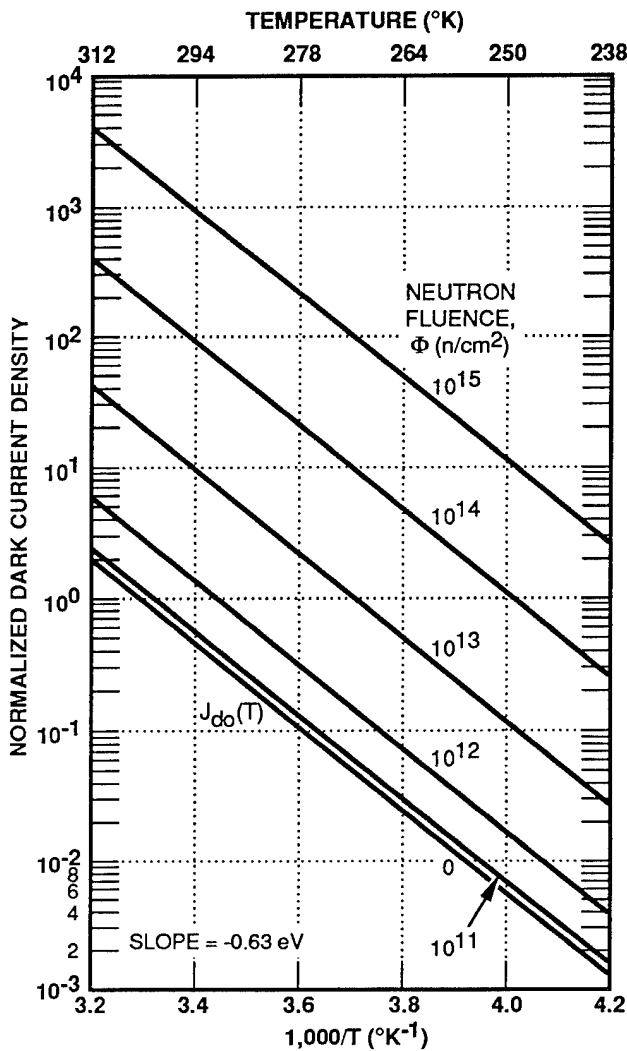


Figure 4-63. Normalized dark-current density versus reciprocal temperature with neutron fluence as a parameter, illustrating the effect of reducing operating temperature on radiation tolerance (Srouf *et al.*, 1978).

two or more methods are usually employed simultaneously. These methods include:

1. *Operation at Low Temperature.* Significant improvements in both CTE and dark current are achieved by cooling the focal plane to as low a temperature as practical.
2. *Narrow Buried Channel.* An extra implant is used to reduce the volume of the potential well holding the signal charge so that it comes into contact with fewer defects for reduced trapping and improved CTE. This technique has proven useful for small-signal applications, but

the practical limits to the technology have not yet been explored.

3. *High-Temperature Anneal During the Mission.* Prolonged heating at 125 to 150°C has been shown to effectively anneal displacement damage, but subsequent irradiation produces higher than expected levels of CTE degradation. Reliability issues may also be a problem. This approach requires more research.
4. *Correction by Software.* Some software has been developed to partially compensate for CTE damage to CCDs in limited circumstances. Correction for dark-current spikes is more straightforward.
5. *Use of a Background Signal.* Some improvement is obtained at the cost of increased noise, and difficulty may be experienced in obtaining a uniform zero across the device.
6. *Shielding.* The optimization of shielding for maximum protection with a minimum of shield size and weight and secondary particle production, and activation is possible (Dale *et al.*, 1993). A detailed study of the impact of secondary particle production in shielding on the CTE performance of CCDs on satellites is provided in Dale *et al.* (1993).

4.9 List of References

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CHAPTER 5

COMPONENT AND CIRCUIT DESIGN

5.1 Introduction

Circuit hardening and part selection are the design procedures that result in radiation-tolerant circuitry. Specific hardness requirements depend upon the system mission and the circuit function within the system. The requirement for circuit hardening usually originates from a radiation-survivability specification in a system development contract.

Design of hardened circuits is an iterative procedure that requires an understanding of the anticipated radiation environment (including dose-enhancement effects), functional requirements of the circuit (including a clear definition of acceptable operation), and the piece-part response to radiation.

Part selection and circuit hardening are basic to all efforts in hardening systems. The circuit designer's ingenuity dictates the requirements imposed upon device manufacturers and system designers and significantly impacts hardware procurement.

The purpose of this chapter is to explain some of the problems associated with circuit hardening and to illustrate how hardened circuit designs can be achieved. Figure 5-1 shows a generalized hardened circuit design procedure (complicated by the radiation requirements), which may have to be abbreviated or expanded to fit a particular system.

5.1.1 Initial Information Requirements

Problem definition is the first step in circuit hardening. The initial information requirements include detailed knowledge of the anticipated radiation environment, the radiation effects on the piece parts, and the functional requirements of the circuit.

As part of the design process, it is necessary to specify devices and to determine the electrical parameters and radiation responses of each. It is

usually also necessary to experimentally verify test data or predictions of radiation response of specific devices. Unless radiation test data are completely described and total confidence can be placed in the results, radiation testing of devices in suitable simulation environments is required.

Environmental specifications [Block 1 of Figure 5-1] must be determined before a design approach is set. Cost considerations dictate that the radiation hardening be "balanced," i.e., that a circuit is not hardened to a level for one environment that greatly exceeds the corresponding levels for other equally important environments. Such balanced hardening requirements apply to all environmental constituents, whether specified

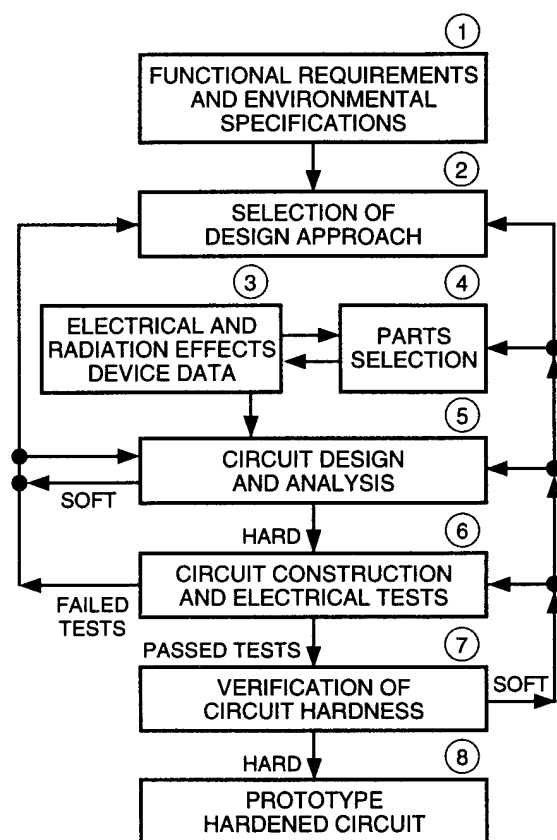


Figure 5-1. Generalized hardened circuit design procedure (Messenger, 1969).

or implied. These include temperature, humidity, vibration, shock, electromagnetic pulse (EMP), system-generated EMP (SGEMP), neutrons, x rays, gamma rays, trapped electrons, trapped protons, solar flares, and cosmic rays.

Gathering the information required to establish the functional requirements of a circuit also requires a good knowledge of the system, especially its interaction with other circuits in the system. Once it is known what behavior of a given circuit will cause a system failure, circuit responses can then be translated into discrete failure criteria for the circuit. In this way, the maximum allowable amplitude and duration of a transient in the output, the gain margin tolerance, maximum tolerable interrupt time, and other functional characteristics can be specified.

The detail required in the description of the radiation environment depends upon the probable intensities of each type of radiation and the response each is likely to cause within the circuit. It is necessary to specify such things as the energy spectrum, number of pulses expected (including amplitudes, shapes, duration, and spacing), peak prompt-radiation rates, and ionizing radiation dose or fluence level.

5.1.2 Selection of Suitable Approach

Selection of a suitable approach [Block 2 of Figure 5-1] for implementation of a hardened circuit function considers the circuit as it applies to the system. All possible design approaches should be listed and evaluated. Data showing radiation effects on devices [Blocks 3 and 4 of Figure 5-1] is applied to device selection and those approaches that show little promise are eliminated. Each possible approach is checked for undesirable features.

5.1.3 Design Phase

After one or more solutions have been selected as most workable, the next logical step is to design the functional block [Block 5 of Figure 5-1] as an actual circuit. Although the design procedure is essentially the same as for nonhardened circuits, it becomes more difficult because of additional restrictions imposed by radiation. Cir-

cuit configurations that are likely to be sensitive to radiation must be recognized and avoided.

Consideration of radiation effects in circuit design requires an analysis phase to ensure that the circuit will function in the specified environment. Analyses for transient response to ionizing radiation and permanent damage from neutron fluence and ionizing radiation dose should be included as required. Analysis is also a necessary prerequisite to radiation testing of the circuit since it will indicate which circuit parameters should be monitored.

With the universal use of personal computers and the advent of many powerful but simple calculational software programs, the term "hand analysis," applied for the analyses used for circuits of moderate complexity, no longer applies. Almost all circuits are now analyzed on computers, the only distinction being that complex circuits require more complex models for their analysis. A simple analysis is frequently used to determine whether a particular circuit configuration will perform satisfactorily. For example, the outcome of the analysis may indicate that a single-ended stage will not work as well as a push-pull stage. Statistical variations in device characteristics often preclude an exact solution. Computer analyses are also applied to other aspects of design. They can, for example, be used to select the best of several alternatives, to evaluate the effects of parametric changes, and to optimize the response, or to determine steady-state operations with anticipated radiation damage. Some of the complex circuit analyses codes available to the design engineer are discussed in Subsection 5.7.3.

5.1.4 Circuit Construction and Testing

In circuit construction [Block 6 of Figure 5-1], the piece parts are assembled and the circuit is tested. There are usually no unique radiation-related problems in breadboarding a circuit. The active piece parts are chosen during design, and one need only insert the passive elements and do the electrical testing. The best device for a particular application will depend upon the "in-circuit" use, its value, the radiation level, etc.

The procedure for checking out the "hardened" circuit is essentially the same as for any other circuit in that revision may be necessary to improve performance. However, if the design is altered, another analysis will be necessary to determine the radiation response of the modified circuit.

5.1.5 Hardness Verification

Experimental and analytical studies are undertaken to confirm circuit hardness [Block 7 of Figure 5-1], including testing in a radiation environment. It is important to test the circuit in an environment that is as similar as possible to the environment expected. This is especially true at the higher radiation rates where piece-part responses may become nonlinear. At high dose rates, where circuit tests are difficult or impossible due to limitation of the effective irradiation volume, it is often necessary to perform an analysis using piece-part data taken at the desired dose rates.

It is extremely important to achieve good correlation between experimental and predicted responses. When good correlation is obtained, one can be reasonably sure that no major factors were overlooked in the circuit design and analysis, and that the circuit response to radiation is well understood. Then, on the basis of this understanding and the experimental results, the response of the circuit to the expected operational radiation environment can be predicted. The outcome of this prediction will determine whether the circuit is sufficiently resistant to radiation or if more work will be necessary.

The designer must take into account the fact that different radiation environments present different verification problems. For example, ionizing radiation dose verification requires consideration of the time-dependent effects, which can be large. For dose rate, achieving a good correlation between the model calculations and experimental results may be quite difficult and expensive. Parasitic capacities can play a significant role in fast response times, and they are difficult to estimate.

The result of the overall hardened circuit design procedure is the prototype shown [Block 8 of Figure 5-1].

5.2 Hardening Methodology

Hardening is accomplished by using a number of techniques at the part-selection, circuit, and system levels. The techniques are often dictated or limited by the system's requirements. First, a system functional analysis must be performed to determine the types of hardening requirements that are imposed on the circuits associated with each system function. A hardening trade-off analysis is then performed to determine the most cost-effective means of hardening the system to meet the requirements.

The hardening trade-off analysis defines the system concept prior to design and development. The detailed design is then implemented using a combination of hardening techniques. The number of techniques that can be used is quite large because of the variety of part-manufacturing technologies, circuit design techniques, and system concepts available.

In general, the hardening techniques for each nuclear environment are different and the impact of other environments on any proposed hardening technique must be evaluated. Design review should consider all of the hostile environments, such as fast neutrons, prompt ionizing radiation, delayed ionizing radiation, x rays, and single-event phenomena (SEP), when evaluating the effectiveness of any proposed circuit-hardening technique.

The two phases of system hardening are design hardening and hardness assurance. The design-hardening phase includes delivering one or more engineering prototypes of a system that is hardened against the applicable nuclear environments described in the nuclear specification, while maintaining at least the performance level described in the system specification. The hardness-assurance phase includes all monitoring and control efforts aimed at reproducing systems whose nuclear hardness equals or exceeds that of the engineering prototype throughout production and system life. Both phases are usually resource-limited, so the allocation of resources

must maximize the probability of achieving the required design hardness and hardness assurance.

Balanced hardening is always essential. Given a particular environment, excessive resources should not be expended on one part of a system or one nuclear environment to the detriment of other system components or other environments. Resource allocation should, in any case, be determined by the degree of difficulty involved. In balancing the hardening efforts, it is important to consider both design hardening and hardness assurance together. Frequently, a large design margin can reduce the need for ongoing hardness-assurance controls at significant overall cost savings.

5.3 Device Selection for Hardened Circuits

Selection of hardened devices (least affected by radiation) involves the logical and knowledgeable trade-off of all circuit requirements and device parameters, including radiation, speed, cost, power dissipation, breakdown voltage, and leakage current. A candidate device must meet the appropriate electrical and mechanical requirements, perform satisfactorily in specified temperature, humidity and other nominal environments, and be reasonably tolerant of the specified nuclear environments. Ordinarily, devices are first selected by circuit requirements; then, from a group of devices having the desired electrical characteristics, a particular device with the most desirable radiation characteristics is chosen. As an example, one approach to hardened device selection, when neutron displacement effects predominate, is the use of complementary MOS (CMOS) devices instead of bipolar devices.

Access to compilations of radiation effects data and electrical data on devices is essential to the designer. Several databases have representative data on neutron, ionizing radiation dose, ionizing radiation dose rate, and single-event effects on typical semiconductor part types that are useful for preliminary design selection (e.g., RADATA, ERRIC, n.d.). Chapters 2, 3, and 4 of this handbook identify failure threshold ranges of various electronic devices for ionizing-radiation dose, ionizing radiation dose rate, neutron and

single-event effects. Actual failure levels are strongly influenced by circuit application, particularly when a device is specified to operate near its performance limits.

5.3.1 Semiconductor Device Selection

5.3.1.1 Neutron Environment

Selecting devices that are relatively hard to the neutron environment should be a first step in hardening circuits. Circuit design is easier and less expensive if the neutron-induced parameter changes are either moderate or negligible. Table 5-1 lists some guidelines for selecting the more sensitive devices for the neutron environment, along with the device parameters that are sensitive to neutrons. In some cases, the device electrical characteristics are indicators of the relative hardness. For example, the change in current gain $\Delta(1/\beta)$ of a transistor varies inversely with f_T , the unity gain bandwidth frequency, so the gain degradation can be minimized by selecting transistors with relatively high f_T values. In other cases, neutron damage susceptibility cannot be related to the manufacturer's specified parameters. For these cases, the devices have to be selected on the basis of radiation response data.

Devices used in the neutron environment should have low circuit gain requirements and should not be used at very low or very high current densities since the neutron damage constant is much higher at extreme currents. Digital integrated circuits (ICs) are usually very resistant to neutrons because they require high f_T transistors in order to meet their switching-speed requirements.

Many linear ICs use internal lateral pnp transistors that have low f_T values, which causes these circuits to fail at neutron levels as much as two orders of magnitude below those of digital circuits. However, some types of operational amplifiers and comparators are being developed and fabricated in bipolar CMOS (BICMOS) technology to reduce neutron sensitivity.

5.3.1.2 Ionizing Radiation Dose Rate Environment

Photocurrent is proportional to the ionization generation rate and effective generation volume,

Table 5-1. Semiconductor device selection guidelines for minimizing neutron damage of sensitive devices (Rose, 1991).

<u>Part Type</u>	<u>Neutron-Degraded Parameters</u>	<u>Device Selection Guidelines</u>
Signal and rectifier diodes	V_F, I_R	Select diodes with lowest power, lowest voltage break-down, and fastest switching times consistent with design.
Reference diodes	V_Z	Use low-power and low-voltage types if feasible. Avoid temperature-compensated diodes where very stable voltage is needed.
Bipolar transistors	$h_{FE}, I_{CBO}, V_{CE(SAT)}, V_{BE}$	Use devices with high f_{Tmin} high h_{FEmin} and low collector breakdown voltage. Select collector current capability so devices will be operated near peak h_{FE} . Use epitaxial devices where possible, and use low $V_{CE(SAT)}$ and $V_{BE(SAT)}$ devices for switching applications.
Silicon-controlled rectifiers (SCRs)	$I_{GT}, V_{GT}, V_{ON}, I_H$	Select devices with lowest breakover voltage, lowest maximum-current rating, and lowest forward on-state voltage consistent with the design applications.
Bipolar linear ICs	$I_b, I_{OS}, V_{OS}, A_{VOL},$ slew rate	Avoid devices with lateral pnp transistors and very high input impedances (if bipolar input transistors are used) where possible. Select according to test data if devices have been characterized. Select BICMOS devices. Select devices with JFET input stages.
Bipolar digital ICs	Fan-out, V_{OL}, I_{IL}	Select high-frequency logic such as TTL. Select hardened VLSI parts.
Light-emitting diodes (LEDs)	Light intensity	Most LEDs are hard, but a few may be sensitive. Select hard devices from test data.
Photodiodes	R, I_D	Select according to test data. PIN photodiodes are harder if they can be operated at high voltages where they are fully depleted.
Phototransistors	I_L, I_D	Sensitive to degradation. Select according to test data if needed.
Opto-isolators	Current transfer ratio	Determine internal devices, since some are very sensitive. LED-PIN photodiode combination may be best choice. Select according to test data.
MOSFETs	V_{GT}	Avoid use of MOSFETs with gate voltage protection (cannot drive negative).
JFETs	g_m, I_{DS}, V_{PO}	Select JFETs with high channel doping.

so both of these factors should be minimized to reduce photocurrent levels. Some guidelines for minimizing photocurrents when selecting parts for gamma radiation environments are:

1. Select devices with lowest breakdown voltage and current ratings that are consistent with circuit applications.
2. Select devices made with isolation processes such as silicon on insulator (SOI) or dielectric isolation (DI). Select devices with buried epitaxial layers.
3. Where possible, avoid devices with large collection volumes such as PIN diodes, optical detectors, and large-area power transistors when the upset level is important.

It should be noted that the Wunsch-Bell burnout damage constant tends to decrease as the semiconductor junction area decreases. The ratio of the photocurrent to the damage constant should be used as a selection criterion to obtain parts with an improved burnout level.

The photocurrent response times can be reduced by proper device selection. Devices with fast recovery times or low storage times tend to recover faster from radiation upset. Dielectrically-isolated ICs (DIICs) generate less photocurrent and tend to recover faster than junction-isolated ICs (JIICs).

Test data summaries available from the Electronic Radiation Response Information Center (ERRIC, n.d.) etc. should be reviewed when selecting CMOS devices or JIICs such as linear ICs or Schottky-coupled transistor-transistor logic (STTL). Some devices using these technologies latch up when exposed to radiation. Linear ICs, particularly commercial types with high gain and low bias currents, are very sensitive to ionizing radiation dose rate. Test data for dynamic storage devices such as MOS or charge-coupled device (CCD) memories should also be reviewed if their upset is important since they tend to upset at low radiation levels.

Table 5-2 summarizes the rules for selecting semiconductors for the transient ionization environment.

5.3.1.3 Ionizing Radiation Dose Environment

Device selection is very important for certain device technologies such as commercial CMOS logic circuits, which are particularly sensitive to ionizing radiation dose. However, unlike the neutron environment, the absence of an effective electrical parameter that correlates with total dose sensitivity for either bipolar or MOS devices in choosing hard devices forces reliance on radiation test data. The problem is compounded by damage nonlinearity, annealing, and potential variations in the ionizing radiation dose response of a given part type within the "normal" manufacturing variations of the suppliers. The radiation response of the same devices made by different manufacturers may be quite different; this must be taken into account when using multiple suppliers.

The guidelines for the selection of devices to minimize ionizing radiation dose damage are essentially the same as the ones presented in Table 5-1 for neutron damage considerations. The following considerations should also be observed for MOS circuits (Rose, 1991):

Table 5-2. Device selection guidelines for transient ionization (Rose, 1991).

Device Type	Important Characteristics to Minimize Response
Diode	Low breakdown voltage, small area, fast switching time
Transistor	Low breakdown voltage, low power rating, fast switching time. Use epitaxial devices instead of planar devices when similar.
Bipolar logic circuit	Avoid latchup-prone technologies. Use oxide-isolated or dielectrically-isolated (DI) technologies.
Bipolar linear circuit	High internal operating currents, low open-loop gain (radiation-hardened circuits may be required). Use DI technology.
MOSFET	Avoid latchup-prone circuits. Use SOI technologies.

1. Select very-large-scale integrated (VLSI) parts with rad-hard processing.
2. Select devices with thin gate oxide.
3. Obtain data on the actual part type, technology, manufacturer, and ascertain that correct test procedures have been used.

Certain types of semiconductor devices are extremely sensitive to radiation effects and should be avoided in most system designs unless the radiation requirements are clearly compatible with their radiation sensitivity. These part types are listed in Table 5-3 along with the environments in which they are sensitive. Silicon-controlled rectifiers (SCRs) head this list and are affected by all environments. Other devices that are highly sensitive include commercial CMOS circuits, optical couplers, and certain types of linear ICs.

5.3.2 Capacitor Selection

Capacitors are sensitive to radiation, which ionizes the dielectric and causes a transient discharge. A prompt discharge results from initial ionization, followed by delayed discharge caused by release of charge carriers from shallow traps, the carriers having become trapped during initial ionization. Discharges of a few percent can be expected in typical capacitors for doses of 5×10^3 rads(Si). The amount of discharge is somewhat circuit dependent. The ratio of circuit recharge time constants to discharge time constants is important.

Guidelines in choosing capacitors to survive a radiation threat are:

- Avoid organic dielectric materials, if possible
- Paper dielectric units must not be impregnated with hydrocarbons
- The preferred types of capacitors are glass, ceramic, mylar, and tantalum, in that order.

5.4 Circuit Design Modifications for Hardening

Much design hardening is done by the simultaneous use of several circuit-oriented approaches. Device selection and creative circuit design techniques minimize the sensitivities of

all important circuit performance parameters, and the use of additional parts creates redundancy to enhance the design margin, DM (the ratio of the failure dose to specification dose).

A common hardening approach is the worst-case circuit design method, wherein the input, output, power, temperature, and other requirements for each circuit are set at the worst ends of their specified ranges as defined by circuit and system interface requirements. The worst-case semiconductor part specification-level radiation response data and the required reliability derating for aging are also factored into the circuit design. An important quantity for piece-part hardness assurance is PAR(FAIL), i.e., the parameter value for a particular device at which the circuit fails. The worst-case circuit analysis helps to determine the value of PAR(FAIL).

If the circuit design works when all these conditions are applied simultaneously, the design is acceptable. Obviously, the design also must work with nominal device parameters (all parameters at design center). The use of worst-case techniques is cost-effective because hard circuits will not require time-consuming detailed analy-

Table 5-3. Highly sensitive semiconductor devices (Johnston, 1980).

Type	Environment(s)
SCRs	All
Power transistors	All
Precision reference diodes	Neutron
Optical couplers	Neutron, gamma dose rate
Linear ICs ^a	
Bipolar	Neutron degradation, ionizing radiation dose rate
MOS	Ionizing radiation dose
CMOS logic circuits	Latchup, ionizing radiation dose

Note:

^a The sensitivity of linear device types varies widely, depending on the technology, function, and internal design.

ses. However, for a worst-case designed circuit, actual hardness might not be determined, only the fact that it is "sure safe" at the specification level.

5.4.1 Current Limiting

Some circuits, such as push-pull transistor amplifiers, inverters, or latched ICs, can burn out due to photocurrent-induced power being dissipated in them. Hardening by current limiting uses a resistor or inductor in the power-supply line to limit the current flow to safe levels. Resistors are normally preferred over inductors, because the recovery time is shorter. If an inductor is used to minimize power dissipation for normal operation, a back-biased diode can be added across the inductor to limit the kick-back voltage. For current limiting, a rule-of-thumb is to use 1 ohm per volt of power-supply voltage (Rose, 1991). It is important to place the resistor between the IC and any decoupling capacitors (Berger *et al.*, 1981). A disadvantage of resistive limiting is that cross talk between circuits sharing a common resistor (e.g., different logic gates on a single chip) may be enhanced during normal operation.

5.4.2 Photocurrent Compensation

The best semiconductor devices available may produce intolerable transients. A second device, therefore, is often employed to produce an equal but opposite effect to cancel or offset the original disturbance. This compensation, especially as it applies to the elimination of transients, requires careful matching of the devices. Furthermore, even though the cancellation may be effective over one range of radiation levels, the combination may produce transients at other levels that exceed transients in the uncompensated circuit. The effect is especially noticeable when using dissimilar devices for compensation, such as diodes for matching transistor photocurrents. This technique can be very effective but should be used with caution (Rose *et al.*, 1981).

Matching photocurrents is less of a problem in ICs because there are fewer manufacturing variations between elements on the same semiconductor chip. It is still difficult to design photocurrent

compensation into JIICs because of collector-substrate photocurrents. Collector-substrate photocurrents dominate the response of the device and cause photocurrent effects in the transistor elements to be nonlinear with dose rate. The magnitudes of the collector-substrate photocurrents are also difficult to control precisely because of manufacturing variations in the semiconductor chip. Photocurrent compensation is better suited for DIICs or SOI ICs where the collector-substrate photocurrents are eliminated.

Four specific photocurrent compensation techniques are shown in Figure 5-2. The photocurrents of transistors Q_2 and Q_3 in Figure 5-2(a) are used to shunt the primary photocurrent of transistor Q_1 around the base resistor R_B and load resistor R_L . The photocurrent through Q_2 will prevent or minimize the generation of secondary photocurrent in Q_1 , while the current through Q_3 will minimize the voltage transient on the collector output. If it is difficult to minimize a transistor's secondary photocurrent, differential amplifier circuits or push-pull circuits can be used to minimize the voltage transients. Figure 5-2(b) illustrates the use of the secondary photocurrent of one transistor to cancel the photocurrent effect of the other transistor.

In those circuits designed to inhibit the production of secondary photocurrent [Figures 5-2(a) and 5-2(c)], the voltage drop across the internal transverse base resistance will exceed the V_{BE} threshold at sufficiently high dose rates, producing secondary photocurrents. For the complementary pair [Figure 5-2(b)], matching the electrical and ionizing-radiation characteristics of npn and pnp devices is very difficult, particularly in ICs. Since the effectiveness of the compensation techniques depends upon the collector-base voltage during irradiation, the design is typically optimized for only one region of operation. Figure 5-2(d) is a variation of 5-2(b).

5.4.3 Filtering

Filtering sometimes can be used to prevent the propagation of photocurrent transients. It also can be used to return interface lines to a desired voltage level after photocurrents in the semiconductors have dissipated. The photocurrent effects

in the semiconductor devices usually end within tens of microseconds after the radiation pulse. By placing low-pass filters in feedback and interface lines, the effects of these photocurrents can be filtered out in much the same way as high-frequency noise. The filtering technique, however, cannot always be used, since filters increase the response time of the circuit and their use may be prohibited by either performance requirements or radiation recovery-time requirements.

Figure 5-3 shows several examples of filtering for linear and digital circuits. The RC "T" filter

is useful in these applications, because it prevents the photocurrents of either the driving or receiving devices from charging or discharging the capacitor rapidly.

5.4.4 Clipping and Clamping

Clipping may be used to limit the magnitude of transients on signal lines. Clipping may reduce the recovery time of the signal lines and limit the magnitude of transients on the output of any succeeding amplifier stages. Clipping can be accomplished by attaching diodes between the

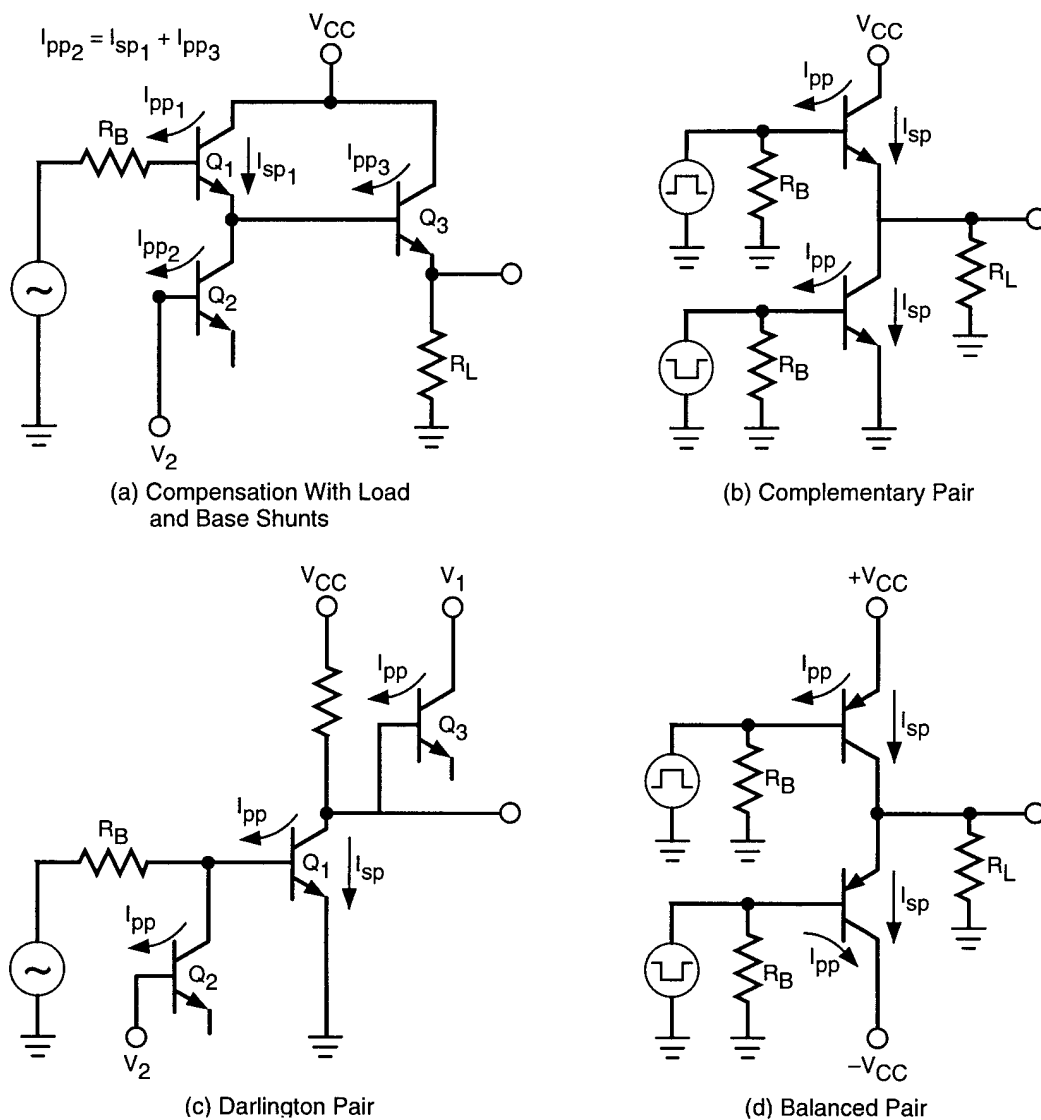


Figure 5-2. Examples of photocurrent compensation techniques (Rose *et al.*, 1981).

signal line and either the ground plane or voltage reference point, such as a charged capacitor, wherein the voltage on the reference would be greater than the maximum signal level to back-bias the diodes and minimize signal distortion under normal conditions.

Clamping is used to keep the voltage on a line at a set level. The technique may be used in control lines to prevent transients from coupling into succeeding circuits and/or ensure that the control lines return to a desired state after the transients have dissipated. Clamping can also be used on power lines either to prevent the application of excessive voltages or to remove voltages so circuits cannot burn out. Clamping can be accomplished by connecting the line to ground or to a voltage reference with a transistor Darlington pair, SCR, or silicon-controlled switch (SCS).

Photocurrents through these devices tend to turn them on, but additional base drive or trigger signals may be needed for low radiation levels.

Where the clamp must be turned on rapidly, it may be possible to parallel the device with a fast-acting component, such as a PIN diode, to start the clamping action. If a Darlington pair is used for the clamping action, the device could be biased ON at a lower level with trickle base drive to shorten the turn-on delay. Under normal conditions, the Darlington clamp has to be isolated from the line with a back-biased diode. If the line must be held in a given state after the event, additional circuitry is needed to hold the clamp for a given time before turning the clamp off (Rose, 1991).

These techniques should be examined carefully, since new transient effects may be introduced by the nonlinearity of the clamping or clipping action.

5.4.5 Feedback

Feedback is a circuit design technique where the output voltage or current is sampled by means of a sampling network, applied to the in-

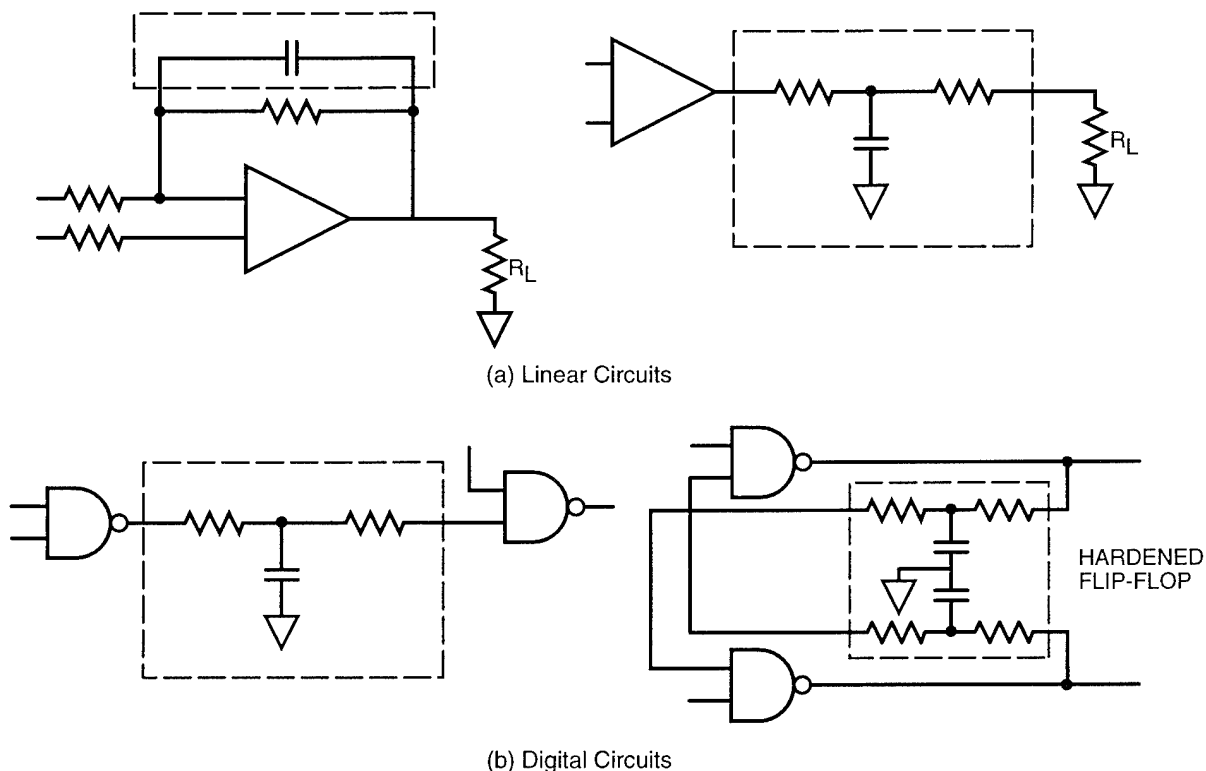


Figure 5-3. Examples of photocurrent filtering techniques for linear and digital circuits (Rose *et al.*, 1981).

put through a feedback network, and combined with the external input signal to the circuit. Negative feedback stabilizes the transfer gain of linear circuits against variations of the gain of the transistors used in the circuits. As a result, ionizing radiation dose or neutron-induced permanent gain degradation in the transistors has significantly less effect on circuit performance. Design techniques that use feedback are sometimes effective in reducing transients.

5.4.6 Temperature Compensation

In addition to the primary effects of radiation in electronic devices, local temperature transients will be produced by the energy deposited in the devices and associated structural hardware. Significant heating of devices has been observed during the course of simulation experiments. Temperature transients can persist for times on the order of tens of seconds after cessation of radiation. Generally, these temperature transients are of such magnitude that the standard temperature-compensation techniques currently employed in analog and digital semiconductor circuitry are applicable.

Transistor temperatures also can be increased by the flow of photocurrents and by the increase in saturation voltage due to displacement damage, a permanent effect. In any case, an evaluation of circuit vulnerability to radiation-induced heating requires both an estimate of the anticipated local-temperature rise and duration at the location of each potentially critical device, and an evaluation of the sensitivity of circuit response to temperature-induced changes in device electrical parameters. Once these prerequisites have been met, hardening against heating effects, if necessary, is straightforward.

5.4.7 Time Sequencing and Time Delays

Time sequencing and time delays are useful in protecting devices that have two stable states such as digital logic circuits, relays, and magnetic cores that could be upset by photocurrent transients on input control lines. The circuit can be arranged so that a specific sequence of events must occur before the state will change, a sequence that cannot be supplied by the radiation-induced saturation of a semiconductor device.

For example, if two or more command signals are required to initiate a circuit response, the signals can be time-sequenced to filter out unwanted transients. Photocurrent transients arrive at approximately the same time. Time-sequenced circuits can be set up to reject simultaneous incoming commands. They can also inhibit receiving a second command until a set delay after the first command arrives. The time delay would have to be larger than the longest expected transient on any incoming line.

A time delay can also be used on a single command line by logically ANDing the original and a delayed signal together. The time-delay and command signals would both have to be larger than the photocurrent transient. The time-sequencing or time-delay circuitry must be hardened against upset for these techniques to be effective (Rose *et al.*, 1981).

5.4.8 Low-Impedance Circuitry

Circuit hardness can be improved with respect to dose-rate response by use of abnormally low impedances. Photocurrents are essentially constant-current sources and, hence, are not strongly dependent upon the load impedance. The approach is to make all impedances, within and external to the circuit, as low as possible, minimizing radiation-induced voltage changes. The designer must not assume, however, that this technique will reduce transient-radiation-induced currents. Care must be taken to handle a current transient by some other technique, such as some form of cancellation. It also must be realized that the use of low impedances sometimes results in a sacrifice of circuit voltage gain, depending on the location of these impedances. Circuit configurations whose voltage gains are proportional to a ratio of resistances then become particularly attractive.

5.4.9 Device Packaging

Shielding and potting are not really circuit design hardening techniques, but they can be used to reduce radiation effects in a circuit. Electrostatic, magnetostatic, electromagnetic, and x-ray total dose shielding are typically employed, particularly in space systems. Careful packaging and placement of sensitive components within

the structure should provide shielding against these radiation types. Potting a circuit to reduce air-ionization and charge-scattering currents is sometimes essential. Even low-impedance circuitry (e.g., 50-ohm strip lines or delay lines) can be affected significantly by ionizing currents if not potted.

5.5 Circuit-Hardening Guidelines

The impact of neutron degradation effects on circuit performance will depend on the sensitivity of the circuit to changes in piece-part parameters and, to some extent, the operating point of the piece part in the circuit. A number of hardening techniques can be used to harden a circuit design to neutrons. Most of these techniques either minimize the effects of the neutron damage or make the resulting circuit design less sensitive to the neutron-induced parameter changes.

The prompt ionizing radiation pulse interacts with the materials of an electronic circuit to produce excess ionization and charge scattering. The main effect of the ionization is to generate photocurrents in circuit semiconductors, which can lead to latchup or burnout, as well as transient interruptions in circuit and system performance. There are a number of hardening techniques that can be used to eliminate or minimize these effects.

Ionizing radiation dose primarily affects electronic and electro-optic parts. The effects induced in these parts are reflected as changes in the part performance parameters. In semiconductor parts, these changes are due to a positive charge buildup in the oxide layer and an increase in the density of interface states at the oxide-semiconductor interface. Parameter changes are a function of the ionizing radiation dose received, the electrical bias on the part during irradiation, the dose rate of the exposure, the temperature, and the operating frequency. The degraded parameters will recover with the annealing of the induced damages. The annealing process depends on the temperature, bias, operating frequency and other factors, but is long compared to operational recovery times for many systems. Therefore, the degraded performance in semiconductors is frequently considered permanent. The

natural space ionizing radiation dose environment will also induce damage. This dose is accumulated over the entire timespan of the mission and will result in additional degradation, but it also permits additional annealing time. The combined effects are known but not adequately proven to establish sound ground rules. Therefore, the conservative approach is to combine the weapon threat with the end-of-mission natural radiation, taking into account the shielding effects of the spacecraft and system packaging (Rose, 1991).

In general, ionizing radiation dose circuit-hardening techniques closely parallel those used for the neutron environment. Semiconductor device selection is a more critical factor for ionizing radiation dose because of the variability of the ionizing radiation dose response with device processing. The response of other electrical devices is also important for ionizing radiation dose, particularly tantalum capacitors and optical fibers.

5.5.1 Neutrons

5.5.1.1 Linear Circuits

Permanent gain (h_{FE}) degradation in bipolar transistors caused by neutrons is a problem in linear circuit hardening. h_{FE} degradation can be minimized by operating transistors near the collector current at which the gain is maximum.

Additional amplifying stages and/or feedback may be used to increase the minimum circuit gain margin and to minimize the impact of gain changes. A low closed-loop gain will permit large gain changes in the individual devices. It will also make the amplifier stages less sensitive to base-emitter voltage (V_{BE}) changes in the case of transistors and to input offset voltage (V_{OS}) and input offset current (I_{OS}) changes in the case of operational amplifiers.

For operational amplifiers, lowering the resistance of the input network will reduce the sensitivity of the circuit response to input bias current (I_b) and I_{OS} changes. However, since high input impedances are usually desirable, this approach is limited (Rose, 1991). Amplifiers with junction field-effect transistor (JFET) input stages are ap-

plicable when a high input impedance must be maintained.

Efforts to harden operational amplifiers have resulted in development of BICMOS devices and also the application of JFET input stage devices, both of which reduce the neutron sensitivity. Manufacturers such as *Harris, Texas Instruments, Analog Devices, Raytheon*, and others are developing and fabricating hardened linear BICMOS ICs. Test data have shown that devices continue to operate within specification at fluence levels $>3 \times 10^{13}$ n/cm² and function with degraded performance at 10^{14} n/cm². Devices with JFET input stages and hardened bipolar design have also been developed using full bipolar technology. These devices also have been shown to operate within specification at fluences between 10^{13} and 10^{14} n/cm² while retaining the characteristic high input impedance and high-frequency response of operational amplifiers (Rose, 1991).

Rapid annealing of h_{FE} degradation is an important design consideration. The initially degraded h_{FE} may be only one-half of the final value. Recovery times may range from microseconds to seconds. The significance of the h_{FE} degradation history depends on the operational requirements of the circuitry. Circuits that must function during the recovery time must tolerate a much larger transient h_{FE} degradation than those that are not required to function until after annealing is complete. A good hardening approach is to design a large gain margin into the circuitry.

Permanent increase in transistor leakage current I_{CBO} from neutron damage is not normally an amplifier design problem since amplifiers are biased well above the I_{CBO} level. The increase can, however, reduce the temperature margin for the circuit.

The increase in resistance of a semiconductor due to neutron exposure reduces the V_{BE} of a transistor if the base drive is held constant. If the collector current is held constant, V_{BE} will increase, resulting in a shift in the operating point of the transistor. This may be of some significance in common emitter amplifier circuits. The

change in V_{BE} can be minimized by using a small resistor in the emitter circuit. Another approach is to use low-resistance bias circuitry to provide a strong base drive to stabilize I_b .

Circuits that use emitter resistance to achieve a high-input impedance will suffer a decrease in input impedance as h_{FE} permanently degrades, since this impedance is approximately h_{FE} times the emitter resistance. Darlington circuits can be used to keep the input impedance above an acceptable level after radiation. However, the increased gain of this configuration may result in an aggravated photocurrent response, requiring the use of some form of cancellation techniques. This must be considered before using a Darlington pair to maintain the input impedance above some level.

Servo control amplifiers use both ac and dc gain stages. Current gain degradation in the last ac stage can propagate through the dc stages as a dc voltage offset. The voltage offset can be minimized by distributing the gain preferentially through the ac stages with the lowest gain in the last ac stage. In addition, matching the input impedance of the dc amplifiers will minimize voltage offsets due to input line disturbances (Rudie, 1980).

The forward voltage (V_F) in signal diodes and the reference (or zener) voltage (V_Z) in reference diodes will change after neutron exposure. If the diodes are used in a loop, the voltage shift may be compensated for by designing the loop so that the voltage shift in another device will cancel the shift in V_F or V_Z . Test data should be obtained for samples of the susceptible devices and the compensating devices to determine which devices can be used together (Rose, 1991).

Neutron effects on diodes can also be minimized by selecting the diode operating points properly. For signal diodes, the forward voltage decreases at low currents and increases at high currents after neutron exposure. The V_F versus I_F curves before and after exposure must cross, so that ΔV_F effects will be minimized if the I_F is selected near the crossover point. For zener diodes,

the knee of the V_Z versus I_Z curve becomes more rounded after neutron exposure, so the operating current should be chosen well above the knee of the curve to minimize ΔV_Z (Rose, 1991).

Use of multiple devices is another approach to increasing the neutron tolerance of a particular circuit design. For example, two higher-frequency, medium-power transistors could be used in parallel to replace a low-frequency, high-power transistor if a single-transistor substitute cannot be found. In analog gain stages, the overall gain degradation can be reduced by cascading an additional stage. These approaches will increase the parts count of a circuit design, but they may eliminate the need for special controls, such as device screening, during manufacturing and deployment of the system.

The use of passive devices in place of semiconductor devices should be considered as a neutron-hardening option whenever such a substitution is useful and feasible. Examples include the use of transformers for ac current or voltage gain when power gain is not required. Such substitution involves trade-offs relative to size, weight, and cost (Durgin, Alexander, and Randall, 1975).

For bipolar comparators, the input bias current, offset voltage, and gain parameters will all degrade in a manner similar to operational amplifiers. The low-output voltage state V_{SAT} will also increase as the neutron level increases. The V_{OS} and V_{SAT} parameters are usually the most important from the standpoint of circuit failure. They begin to exceed their specification limits in the range from 5×10^{12} to 5×10^{13} n/cm². As with operational amplifiers, comparators being developed and fabricated in BICMOS technology have displayed increased neutron hardness by a factor of 2 or more over the standard bipolar devices (Rose, 1991).

Analog-to-digital converters (ADCs) are also very sensitive to neutron radiation. In addition to the inherent sensitivities associated with the comparator and amplifier functions, the precision reference voltage is also subject to change when exposed to neutrons. The function parameter degradation is reflected in the loss of accuracy by

losing the least-significant-bit (LSB) and successive-bit conversion capability. Also, ADC linearity is degraded as is conversion speed and other parameters. Typical unhardened ADCs will lose the first or second LSB and degrade below specified performance around 10^{12} n/cm².

For voltage regulators, the line and load regulation parameters usually degrade most rapidly as the neutron fluence is increased. Either or both of the parameters may degrade beyond their specification limits in the range from about 1×10^{12} to 5×10^{13} n/cm². The output voltage (V_{OUT}) remains fairly stable as regulation parameters exceed their limits; the output voltage of some voltage regulators will begin to drop very rapidly to zero as the fluence level increases. The fluence at which V_{OUT} begins to drop rapidly is not consistent, even for devices of the same generic type and manufacturer. Another popular linear power IC is a pulse-width modulator (PWM) device.

5.5.1.2 Bipolar Digital Circuits

Permanent neutron damage tends to bring a transistor out of saturation because the decrease in h_{FE} reduces the collector current. A logic device, such as a common emitter switch, may even experience a permanent change of state. A direct effect of permanent neutron damage is a decrease in the fan-out capability of a logic circuit.

A practical solution to the problem of maintaining transistor saturation, even after irradiation, is to use the maximum practical base drive. The technique also applies to SCRs, which have a failure mechanism similar to transistors, by using the maximum practical gate current. This solution has some drawbacks in that the overdrive has the effect of increasing the turn-off time of the saturated transistor. High-speed logic circuits may, therefore, require a compensation technique such as a speed-up capacitor across the base drive resistor to maintain required switching times. Another technique is to use an external bypass diode from base to collector to shunt the excess drive current directly to the collector, thus speeding up the recovery from saturation. Conventional collector clamping and steering techniques are also applicable for limiting saturation.

Photocurrent effects must be considered when placing speed-up capacitors in the base circuit.

Bipolar digital integrated circuits usually fail from h_{FE} degradation in the output sinking transistor. The collector current of this transistor must be equal to or greater than the fan-out current sinking through the transistor. If this condition is not met, the sinking transistor will come out of saturation. Reducing the required fan-out will reduce the sinking current required and harden the circuit against neutrons.

Neutron irradiation also affects the static parameters of digital IC gates by increasing the input threshold voltage slightly and the output low-level voltage significantly, the latter being the most common neutron-induced failure mode. If the increase is sufficient, the logic level "0" will be read as a logic level "1." Both of these voltage changes must be taken into account when using digital ICs in a circuit. It is important to test the candidate circuits for anticipated threat levels, since the increase of low-level output voltage varies among devices for the various versions of digital IC technology.

Standard TTL, low-power Schottky TTL (LSTTL), and low-power TTL digital ICs all exhibit the failure characteristics described above. Technologies like advanced Schottky TTL (FAST), advanced low-power Schottky (ALS) logic, and emitter-coupled logic (ECL) exhibit similar characteristics, but at higher neutron levels than TTL.

5.5.1.3 Summary of Neutron Hardening Guidelines

The following hardening techniques are recommended for circuit design in a neutron environment:

1. Keep requirements for ultrastable voltages, currents, and frequencies to a minimum
2. Avoid the use of SCRs, unijunction devices, photocouplers, and phototransistors
3. Operate transistors in the linear mode at a high current level (but not above the point of maximum current gain)

4. For transistors operating in saturation and for thyristors, use the maximum practical base or gate drive current
5. Use negative feedback to minimize the effect of beta variations on circuit performance
6. Design circuits to tolerate low-breakdown voltage transistors, and use transistors with the lowest acceptable breakdown voltages to allow a suitable derating factor for reliability considerations.
7. Design for a high circuit-gain margin
8. Use differential design to minimize bias dependence
9. Use high-frequency components
10. Use active bias compensation techniques to account for offset voltages and currents
11. Avoid designs that require precision operational amplifiers
12. Avoid designs that require low-leakage analog switches, or precise digital-to-analog and analog-to-digital converters
13. Derate logic fan-out

5.5.2 Ionizing Radiation Dose Rate

5.5.2.1 Linear Circuits

The transient recovery of a circuit to its normal output condition following exposure to ionizing radiation is a function of the recovery times of the transistors and their associated input-output circuitry. The recovery time of the circuit will be controlled by the relaxation times of the transistors if there are no reactive coupling elements. Reactive elements may significantly increase the recovery time. Usually, the increase is acceptable, but this must be verified. Direct coupled stages are generally preferred from a rapid recovery standpoint. It may be possible to replace a capacitor with a zener diode as a coupling element where a dc potential difference exists across the capacitor. The associated zener diode photocurrent response must be considered for such an application, although it is usually small compared to transistor photocurrents.

Transistors driven into saturation by ionizing radiation may be damaged by the saturation cur-

rent, or may even fail completely unless circuit design precautions are taken. For example, a saturated complementary pair of transistors such as in a push-pull amplifier will shunt positive and negative supplies together unless a limiting resistance is used. Successive emitter-follower stages using alternate npn and pnp transistors are vulnerable during saturation for the same reason. Voltage-dropping collector resistors should be used to minimize these transient currents. Excessive current may also flow when a power supply is shunted to ground. A small resistor in each power-supply lead will reduce the current to an acceptable level. In general, all ionization-induced shunting paths should be current-limited by the addition of a small resistance or by inductive techniques.

Saturation of the transistor used as a series regulator in a power supply may apply excessive voltage to the load circuits. This problem can be minimized by placing a small voltage-dropping resistor in the collector. The size of the resistance should be small enough to avoid disturbing normal operation or significantly increasing the quiescent power dissipation. Power supplies should be designed with some sort of current-limiting capability. Large capacitor filters on the output of a voltage regulator may also cause damaging current sources. A small series resistor may be used to limit current surges at some sacrifice in regulation. Using as small a capacitor as practical will also help keep the current surge to an acceptable level.

Photocurrent cancellation [Subsection 5.4.2] can be used to keep a transistor out of saturation by shunting the collector photocurrent away from the base emitter junction. Before using any cancellation techniques, the designer should also consider the effects of neutron-induced h_{FE} degradation on the circuit. Photocurrent cancellation techniques can also be used to shunt a photocurrent around loads or critical capacitors.

In inverter-type circuits, an overvoltage spike is produced when both driver transistors attempt to recover from saturation. Two basic conditions to consider in determining whether the transistor will be damaged in inductive load circuits are:

(1) the magnitude of the photocurrent generated by the ionizing radiation, (2) and the length of time the ionizing radiation is present. Both conditions affect the current flow in an inductive load and the amount of energy that will be stored in the leakage inductance of the load transformer. When a combination of the two conditions makes the stored energy exceed the collector-emitter breakdown voltage (BV_{CEO}) threshold, the driving transistors become susceptible to collector-emitter voltage breakdown. The breakdown occurs when the stored energy in the transformer inductance is suddenly released at the end of the radiation period. Breakdown can be avoided by placing back-to-back zener diodes across the transformer winding (across the collector to emitter) and keeping the lead lengths in this connection to the absolute minimum. An alternative to zener protection is specifying the allowable transformer leakage inductance so that the inductive spike will be below that required for driver transistor damage.

Photocurrent responses of diode and transistor elements of ICs are similar to the effects described for their discrete equivalents. The response of the overall circuit, however, may be much different from that of a discrete circuit. JIICs use reverse-biased junctions to separate circuit elements from each other and from the bulk substrate. The areas covered by collector-substrate junctions are usually quite large, so large photocurrents flow through the substrate region and the power and ground leads of the device. These photocurrents upset the devices when they become sufficiently large. The upset threshold for ICs depends primarily on the technology, bias voltage, and prompt ionizing radiation pulse width.

Linear bipolar integrated circuits tend to be sensitive to pulsed radiation. The high internal gain of the linear devices causes large transients on the device output. Relatively small output variations may result in functional failure. Linear ICs also have long recovery times sometimes lasting for hundreds of microseconds. Current limiting must be provided in the supply lines to minimize burnout due to the high operating voltages.

5.5.2.2 Digital Circuits

Circuits involving discrete voltage states, such as logic circuits, should use the saturated-transistor state where possible, since high ionization rates will saturate the transistors anyway. Saturated operation ensures that the circuit voltage level will not change appreciably during the ionizing radiation pulse.

Saturation shorting may be a problem in digital circuitry. For example, switches in digital-to-analog conversion circuits and logic switches that drive emitter-followers will short two power supplies together during radiation-induced transistor saturation. Some form of current limiting, such as a small resistor in the power-supply lead, is necessary. A similar situation exists for commutating transistors whose collectors are common and whose emitters are each tied to a signal source (e.g., sensors). All transistors will be saturated simultaneously, shorting all the driving signals together. The signal sources can be protected by inserting a series resistor in each emitter lead. Current flow through this resistor, when that input is commutated, must be minimized since the voltage drop across it appears as a signal loss. The emitter current can be limited by a constant-current generator in the collector circuit that "unloads" the emitter current requirements to a point just inside the conduction region.

Digital logic circuits are much less sensitive than linear ICs, but many of the new logic families use nonsaturating circuitry (e.g., ECL, Shottky-clamped TTL), which have long lifetimes in the collector and substrate.

A logic circuit that is disturbed in the process of changing states may terminate in either state. Memory could be randomized in this way even though the basic memory circuit is radiation-resistant in both of its states. A logic circuit, such as a flip-flop that has been driven into saturation by ionizing radiation, may not recover to its pre-irradiation state. A computer containing flip-flops would thus recover to a random state after irradiation and begin computing from that state, usually resulting in computer failure. The problem can be eliminated by incorporation of a cir-

cumvention scheme into the computer hardware or software mechanization [see Subsection 5.6.3].

The effects of the prompt radiation on memories depend on the type of memory technology used. Magnetic storage media, such as plated wire cores, disks, drums, or tapes, are essentially immune to dose rate upset at practical levels. The upset levels for memories that employ such media will usually depend on the data and control circuits that interface with the memory. These data and control circuits may cause memory upset orders of magnitude below the thresholds for the upset level of the storage medium *per se*. Transients in input interface circuits may cause false information to be written into the memory. READ sense amplifiers, however, tend to be the most sensitive to radiation. In destructive readout memories, these amplifiers usually set the lowest level at which memory data can be lost (Rose, 1991).

For semiconductor memories, the effects of a radiation pulse may be determined by either the memory device itself or the IC that interfaces with it. Data stored in random-access memories (RAMs) can be lost due to upset or latchup of the device itself. Data can also be lost when output transients from interface circuits erroneously enable the write mode of the RAM. The upset levels for both the memory and interface ICs, therefore, must be established before the lowest level for data loss can be determined (Rose, 1991).

For read-only memories (ROMs), programmable read-only memories (PROMs), and electrically alterable read-only memories (EAROMs), interface circuits generally will affect the information stored in the devices. Transient upset in either the memory IC or the interface circuits, however, may cause erroneous information to be temporarily read out of the memory device. Assuming latchup or burnout does not occur, the memory IC should function properly after the upset transients dissipate.

Power MOSFET transistors have a parasitic bipolar transistor associated with each MOSFET transistor cell. For a typical n-channel device,

the n⁺-source, p-channel, and n-drain form a parasitic npn transistor (emitter, base, and collector, respectively). Previous data have shown that certain types of transistors may be damaged as a result of avalanche-stimulated conduction when exposed to high dose rates. This high-current mode has been observed well below (as low as 10 percent) the static breakdown voltage for the device. Also, since it is primarily an avalanche breakdown condition, the high current mode is sustained for times much greater than the ionizing pulse. The distribution of current in the power MOSFETs during ionizing radiation dose exposure and in the high current mode can cause the parasitic transistors in a small number of MOSFET cells to be turned on hard and to dominate the MOSFET current. This current concentration may result in localized thermal runaway and burnout of the power MOSFET transistor. Limiting the current with either series inductors or resistors has been shown to be effective in preventing power MOSFET burnout.

Several major techniques can be used to harden ICs to dose-rate effects. The first is to minimize the number of reverse-biased junctions. This can be done by the use of dielectric isolation (instead of junction-isolation techniques), use of silicon-on-insulator technologies, and the use of thin-film resistors. Finally, photocurrent effects, which can be reduced by the above three methods, can be compensated for by using additional pn junctions to compensate for the photocurrent of required junctions. All of the above techniques can be used to harden ICs.

The dose rate upset threshold of cells within a device (and therefore the device) has been shown (Massengill and Diehl-Nagle, 1984) to vary with the location and loading on the supply-line metallization path. This effect, referred to as "railspan collapse," is the result of voltage drop in the supply line to each cell, causing cells farthest from the "rail" (supply line) to drop below the voltage level required to maintain operation. In addition to resistive railspan collapse, recent work has indicated that line inductance (or inductive railspan collapse) may also influence the voltage at a cell and cause a lower upset thresh-

old. IC manufacturers producing hardened, very-large-scale integrated (VLSI) devices should be made aware of these effects, if they already are not, and compensations made in the design and layout of the device's supply line and cell locations.

5.5.2.3 Latchup

Latchup is a common effect that can occur in almost any IC. The junction-isolated region, when combined with a transistor element, forms a pnpn structure that sometimes can be triggered to a low-impedance state like an SCR if the voltages are shifted enough during the photocurrent upset. The latch condition will hold until power is removed from the device. The device may burn out if the current level through the latched area is large enough. Latchup has been observed in all digital bipolar technologies except IIL and current-mode logic (CML).

DIICs do not exhibit the large substrate photocurrents found in JIICs. A dielectric layer is used instead of junction isolation to separate the circuit elements. The response of the device is similar to an equivalent discrete circuit if the elements are individually isolated. Where groups of circuit elements are placed in the same dielectrically isolated "tub," interactions may take place between the common elements when photocurrents flow. The device, therefore, may not respond in the same way as a discrete circuit. The levels of photocurrents through these device types are much lower than for JIICs and the recovery times of these devices are shorter. Devices fabricated using SOS and SOI technologies provide a dielectric layer below the active IC regions. When these technologies are combined with trench isolation between devices, complete dielectric isolation is achieved. Another latchup preventive measure is a heavily doped, buried epitaxial layer that reduces the substrate conduction path; when combined with side-wall isolation, latchup is effectively reduced or eliminated (Rose, 1991).

Individual elements of MOS ICs produce photocurrent effects similar to those described for MOS transistors. The total drain photocurrent for large-scale integrated (LSI) circuits can be

large at high dose rate levels, so these ICs may burn out. CMOS ICs, which have pnpn structures, are very susceptible to latchup. Latchup tests conducted on 64 types of standard CMOS devices showed that over 50 percent of the types latched up. Not only do they latch up, they also exhibit latchup windows (latch at one dose rate, not latch at a higher dose rate, and then again latch at an even higher level). Tests performed on neutron-irradiated CMOS (Dawes and Derbenwick, 1976) have shown that irradiating the parts with $>10^{14}$ n/cm² will prevent latchup by reducing the substrate minority-carrier lifetime. In addition, current limiting in the supply lead for CMOS devices has been shown to prevent latchup. Like bipolar devices, dielectrically isolated devices will not latch up; devices fabricated with a heavily doped, buried epitaxial layer and trench isolation also have been shown not to latch up.

5.5.2.4 Summary of Ionizing Radiation Dose Rate Hardening Guidelines

The following hardening techniques are recommended for circuit design in an ionizing radiation dose rate environment:

1. Photocurrent compensation
2. Low-impedance circuitry
3. Balanced output stages
4. Differential circuits
5. Quiescent saturation
6. Minimum transistor geometries
7. Dielectric isolation (SOS, SOI, trench)
8. Current-limiting resistors
9. Circumvention
10. Nonvolatile memories
11. Darlington transistors in STTL
12. Redundant circuitry (where practical)
13. Avoid high-gain circuits
14. Substitute passive circuitry for active filters
15. Select p-channel in place of n-channel MOS devices
16. Neutron irradiate MOS devices to kill parasitic transistor gain

5.5.3 Ionizing Radiation Dose Hardening Guidelines

5.5.3.1 Linear Circuits

The current gain (h_{FE}) of a bipolar transistor is determined by a combination of bulk and surface currents. At low collector currents, h_{FE} is primarily determined by surface currents. The ionizing-radiation-dose gain degradation of transistors can be minimized by operating at the peak h_{FE} current level.

Bipolar linear ICs are moderately sensitive to ionizing radiation dose effects. Offset voltage (V_{OS}), offset current (I_{OS}), bias current (I_b), and open-loop voltage gain (A_{VOL}) are some of the key parameters of operational amplifiers and comparators affected by ionizing radiation. The threshold for the appearance of parameter changes is typically around 50 krad(Si). Usually, the mean ΔI_b (50 krad) is a small fraction of I_b (maximum). In some cases, however, this is not true. Some bipolar devices with otherwise very desirable characteristics for space systems have difficulties at 5 krad(Si). For example, the LM111F has a specification maximum I_b of 100 nA at 25°C and a measured mean ΔI_b of 98.6 nA at 10 krad(Si) (Rose, 1991).

Parameter changes can occur in bipolar operational amplifiers and comparators for doses of less than 50 krad(Si). Linear devices (operational amplifiers, comparators, ADCs) developed with BICMOS technology are all being fabricated with hardened CMOS technology that can be functional at 1 Mrad(Si). Test data on operational amplifiers with JFET input stages have shown them to have higher failure levels than standard bipolar devices; typically, they will operate within specification at 100 krad(Si) and exhibit functional degradation up to 1 Mrad(Si) (Rose, 1991).

As with bipolar digital ICs, linear ICs built using oxide isolation may exhibit significant leakage currents and failures at doses $>10^4$ rad(Si). Bipolar regulator ICs suffer from a loss of precision when their loop gains are degraded. Regulation changes are barely detectable, however, at 50 krad(Si), with most devices operating

within specification at 100 to 500 krads(Si) and functional up to 1 Mrad(Si). RF bipolar linears are less sensitive to ionizing radiation dose degradation, with greater than 100 krads(Si) required to produce observable effects (Rose, 1991).

5.5.3.2 Digital Circuits

MOS devices are most sensitive to ionizing-radiation dose effects. The sensitivity is dependent on the particular MOS technology, complexity of the device, time-history profile of the ionizing radiation dose threat, bias, circuit performance requirements, and manufacturing process variation. The sources of this sensitivity are trapped charge in the gate and field oxides and generation of interface states (Boesch, 1982), which manifests itself as changes in threshold voltage DV_T , leakage current, and transconductance. Positive charge buildup in the gate oxide of an n- or p-channel results in shifting the gate transconductance characteristics toward more negative voltages. This shift tends to cause n-channel devices to become more conductive and with lower turn-on threshold, and p-channel devices to become less conductive and with higher turn-on threshold. Results of these threshold voltage shifts and the internal logic levels determine the sensitivities of the various MOS technologies. Another important factor in determining ionizing radiation dose failure is the rate at which the dose is received (Schwank *et al.*, 1984). At low dose rates (<100 rads[Si]/sec), the gate voltage shift may typically be negative but not sufficient to cause a failure; as the exposure is continued at this rate, the gate voltage shift will reverse and finally fail when the allowable positive gate voltage threshold is exceeded. This response (Johnston, 1984), known as "rebound" (or "super-recovery"), is the result of competing effects between the oxide-trapped charge (N_{ot}) and the interface states (N_{it}). At high exposure rates, the oxide-trapped charge prevails, and devices will fail due to negative voltage shift, which usually occurs at substantially lower ionizing radiation dose levels. At lower dose-rate levels, as previously noted, the interface states prevail and devices fail as a result of positive voltage shift at higher ionizing radiation dose levels. Therefore, it is imperative that the ioniz-

ing radiation dose exposure profile be specified and that MOS device performance be established in accordance with the correct ionizing radiation dose rate (Rose, 1991). Section 2.5 discusses the effects of varying dose rates and time-dependent effects on the response of MOS devices to ionizing radiation exposure.

CMOS device failure may be due to an inability of the device to function or to out-of-specification parameter changes. The failure levels of many commercial CMOS and PMOS devices occur between 10 and 20 krads(Si). However, hardened bulk CMOS devices are guaranteed to survive a minimum of 1 Mrad(Si). Other MOS technologies that are sensitive are power DMOS and high-performance n-channel MOS (HMOS), since, basically, they are modified NMOS processes. Failure levels for all MOS devices are strongly dependent on the bias condition and dose rate during irradiation. NMOS devices tested with all pins grounded have a higher failure threshold (a factor of two or more) than static biased or operating devices (Rose, 1991).

In addition to the dose-rate rebound effect discussed above, the rate of ionizing radiation dose accumulation has been theorized to cause internal bias shifts, thereby affecting the ionizing radiation dose failure threshold of complex ICs. Data on MOS microprocessors (Wilkin, 1981) indicate that the ionizing radiation dose failure level for devices irradiated at 100 rads(Si)/sec from a ^{60}Co source are consistently lower than the failure level for devices irradiated with a single pulse (0.15- and 1.0- μsec pulse widths) from a linear accelerator.

Another important consideration in evaluating MOS data or conducting piece-part tests is the bias condition during the test and the time between irradiation and test parameter measurements. Data have shown significant variation (usually improvement) in the radiation performance of parts that have been allowed to anneal between ionizing irradiation dose and parameter measurement, especially if bias has been removed. The most accurate tests are conducted *in situ* or immediately after the exposure without removing bias. Standardized test method MIL-

STD-883C (1977), Method 1019, has been developed to unify ionizing radiation dose testing procedures and address response issues such as data measurement and rebound. Designers should verify that tests are performed in accordance with this procedure or that existing data are evaluated in reference to the approved test method.

The failures discussed above are associated with a turn-on-voltage shift in the MOS device. Another ionizing-radiation-dose-induced, permanent-change effect also of concern is an increase in the MOS transistor's quiescent leakage, drain-source current. Leakage-current increase, which is most dramatic in CMOS devices, can result in sizable increases in a system's standby power dissipation. As an example, a 1k CMOS bulk RAM exhibited a 2,000-fold leakage-current increase at 7 krad(Si), and NMOS RAMs have also shown significant increases. For battery-operated CMOS technology equipment, such changes are undesirable and must be taken into account.

SOI and SOS technology devices (primarily CMOS/SOS and CMOS/SOI parts) are also sensitive to ionizing radiation dose. Since parts fabricated with this technology are generally LSI, the unhardened parts have ionizing radiation dose failure thresholds corresponding to other complex CMOS parts. Typically, failure thresholds below 3×10^5 rads(Si) have been observed in CMOS/SOS microprocessors, with edge-channel and back-channel leakage being the primary failure mechanism. However, as in CMOS bulk technology some manufacturers use a radiation-hard process and specify device performance without any degradation at 10^6 rads(Si) and functionality to 10^7 rads(Si) (Rose, 1991).

Two MOS-type technologies used for non-volatile memory applications include metal-nitride oxide semiconductors (MNOS) and silicon-nitride oxide semiconductors (SNOS). SNOS EEPROMS have been demonstrated with performance up to 1 Mrads(Si).

TTL ICs can be hardened using some of the same techniques discussed for neutron hardening

[Subsection 5.5.1]. A large circuit design margin (the ratio of failure dose to specification dose) and reduced fan-out requirements are very effective. Pre-irradiation with neutrons is also effective.

5.5.3.3 Summary of Ionizing Radiation Dose Hardening Guidelines

Recommendations for hardened circuit design in an ionizing dose radiation environment are listed below. These guidelines are a combination of part-selection and circuit-design techniques (Rose, 1991).

1. Select devices with rad-hard process
2. Select devices with thin gate oxide
3. Reduce bias
4. Allow tolerance for gate voltage shifts and increased leakage
5. Provide a design margin of at least 5
6. Obtain data on actual part type, technology, and manufacturer, and ascertain that correct test procedures have been followed
7. Select lowest power device appropriate for design
8. Select lowest voltage breakdown device appropriate for design
9. Select fastest switching speed device appropriate for design
10. Minimize circuit resistance
11. Avoid use of temperature-compensated diodes in tight tolerant circuits
12. Select transistor with highest f_T practical (>50 MHz)
13. Select transistor with lowest collector breakdown voltage practical
14. Operate near the peak of I_C versus h_{FE} curve
15. Select epitaxial devices where possible
16. Use low $V_{CE(SAT)}$ and $V_{BE(SAT)}$ transistors in switching applications
17. Allow design tolerance for Δh_{FE} , $\Delta V_{CE(SAT)}$, ΔI_{CBO} and other parameter changes
18. Select JFETs with high channel doping
19. Allow for ΔV_T in MOSFETs
20. Reduce the gate voltage bias in MOSFETs

21. Allow design tolerance for ΔI_b , ΔI_{OS} , ΔV_{OS} , ΔA_{VOL} , ΔSR (slew rate), ΔZ_{IN} (input impedance), etc.
22. Minimize gain dependence with closed-loop designs
23. Minimize bias dependence with differential designs
24. Design with active bias compensation to account for offset
25. Avoid designs requiring precision op-amps
26. Allow design tolerance for lower fan-out, ΔV_{OL} (low-level output voltage), ΔI_{IL} , ΔV_{OH} (high-level output voltage), and Δt_{PD} (propagation delay time)
27. Provide ionizing radiation dose shielding, if applicable.

5.5.4 Dose-Enhancement Effects

Dose is defined as the energy per unit mass absorbed by a material irradiated with x rays or gamma rays. Near the interface of two dissimilar materials such as gold and silicon, electron equilibrium does not exist, and the dose differs from the equilibrium bulk values for each material. This variation in dose occurs over a transition region determined by the range of the most energetic electrons in each material. Dose enhancement then is defined as the ratio of the local dose in the transition region to the equilibrium dose for the material. The amount of dose enhancement depends on the energy spectrum of the x rays, and for typical device dimensions, at a gold-silicon interface, it is greatest for x-ray photons having an energy of about 150 keV (Burke, 1986). In practice, the effects of dose enhancement in electronic devices can be expressed by a dose-enhancement factor (DEF), which is the average dose in the sensitive region of the device divided by the equilibrium dose.

Strong dose-enhancement effects occur in semiconductor devices when high-Z materials are present in the device structure. [DEF can often be 10 for typical devices in a nuclear weapon radiation environment.] In semiconductor parts, high-Z materials can occur in the chip metallization or in the device package. The active region of the chip is located near the top surface of the

chip; the dose experienced in the active region affects device performance. The chip is thick enough to protect the active region from significant dose-enhancement effects from the bottom of the chip; e.g., chips that are mounted using a gold-eutectic bonding do not have significant enhancement effects in the top (active) region of the chip. The use of high-Z materials next to low-Z materials will cause an increase in the absorbed dose in the low-Z material next to the interface (Long *et al.*, 1983).

The major types of metallization and interconnect systems in common use are aluminum or polysilicon, Wand Ta silicides, and gold. Coupled with these are three types of package lids: (1) ceramic (including alumina, beryllium oxide, transparent glass, or other lids with atomic weight $Z \leq 14$), (2) kovar (possibly with nickel or chromium plating, or other plating materials with $27 \leq Z \leq 32$), (3) gold-plated. In ceramic packages, for example, enhancement occurs only directly under a high-Z metallization, whereas for gold-plated lids the enhancement is rather uniform over the total chip regardless of the type of metallization (Long *et al.*, 1983).

In MOS technologies, dose enhancement increases the effective dose in the oxide, resulting in a greater threshold voltage shift and increased leakage current. For bipolar transistors, the results are increased leakage current and gain changes due to the dose enhancement caused by the interfaces with the high-Z packaging and interconnect materials (Long *et al.*, 1983).

5.5.5 Single-Event Phenomena

Effects on electronics due to the natural space environment are often due to the reaction to a single ionizing particle impinging on circuits and devices. These effects are referred to as single-event phenomena (SEP). Single events are characterized as transient, soft, or hard errors, depending on whether a device suffers permanent damage (McNulty, 1990).

A transient error is a short-term disturbance in the internal circuit that recovers within one clock period and, except for a short time period during the transient, causes no error in the output of the

circuit. In some applications, the transient can lead to a logic error or bit error; however, timing constraints are imposed on the occurrence of the transient are imposed with respect to other circuit operations (Pickel, 1983).

Soft errors destroy digital data without physically damaging the device storing the data. Logic errors are changes in a sequence of digital data such as the output of a shift register. Memory errors are changes in the state of a bistable memory storage element; i.e., the data bit is changed but the storage device does not suffer permanent damage. The device can be rewritten to the correct state with no lasting effects. Memory errors can be either single bits or multiple bits that are disturbed by a single ion. In addition, a loss of synchronization is possible in clocked devices, such as microprocessors (Pickel, 1983).

Hard errors result in physical damage to the electronic devices that is not readily recovered. Examples of hard errors are latchup, snapback, burnout, gate rupture, frozen bits, and the generation of noise sources in CCDs (McNulty, 1990). These phenomena are described more fully in Section 3.10 of this handbook.

Hardening techniques for SEP are directly related to the device technology design rules. Static RAMs (SRAMs) are generally less sensitive than dynamic RAMs (DRAMs), for example. However, as SRAM integration density continues to increase and operating voltage decrease, this trend will reverse unless specific SEP hardening methods are applied. CMOS RAMs tend to have an advantage over low-power NMOS or DRAM technologies (Long *et al.*, 1983; Nichols, 1982). It has been shown that increased intracell decoupling resistance can harden CMOS logic circuits (Nichols, 1982). Capacitive hardening consists of adding increased capacitance at sensitive nodes to maintain ion-induced voltage transients below upset level. Power speed trade-off considerations, of course, can be made in attempting to apply resistance or capacitance hardening techniques to integrated circuit devices (Diehl *et al.*, 1983).

Design guidelines for a variety of circuit technologies are presented in the subsections that follow.

5.5.5.1 Bulk/Epitaxial CMOS Circuits

SEP design hardening approaches slow or restrict the feedback response of data cells to single-particle-induced voltage transients, thereby allowing the cells to recover without logic upsets (Kerns and Shafer, 1988). The SEP-sensitive regions of a MOS circuit are limited to the volumes within the substrate that encompass the depletion regions of each strongly reverse-biased drain diffusion. Charge from single-event interactions is collected most efficiently within these sensitive substrate volumes. Each charge-collecting node should be examined to determine if single-event-induced current pulses could result in disruption of normal circuit operation. The track of ionization charge (electron-hole pairs) characteristic of a single-event hit is shown in Figure 5-4. The charge collected is comprised of two components: the drift component and the diffusion component. A field funnel develops whenever the high excess-carrier density along a track penetrates a junction and momentarily controls the potential field distribution within the semiconductor, typically existing for about 1 nsec (Oldham, McLean, and Hartman, 1986). Basically, a circuit is hardened against SEP by minimizing the amount of charge that can be collected (Q_{COLL}) by a sensitive node per event and/or by maximizing the critical charge (Q_c) necessary to produce an upset.

The choice of elements used in a circuit design is very important in reducing SEP vulnerability. Floating nodes or resistively isolated nodes are susceptible to SEU and should be avoided in the design of hardened circuits. Thus, the use of the resistor-load, or four-transistor, SRAM cell, are not good choices for hardened circuits. Static circuit designs are generally harder than dynamic circuit designs (Kerns and Shafer, 1988).

The most common type of SEP hardening uses time discrimination to preclude SEU, whereby the switching time constants of bistable data-storage elements are increased to prevent single-event-induced current pulses from changing the

logic state. Ideally, design hardening techniques should have minimal adverse effects on the circuit performance characteristics, and should neither introduce process complexities nor greatly reduce circuit density.

Resistive hardening has been shown to be an effective way of reducing the single-event vulnerability of SRAM cells (Andrews *et al.*, 1982; Browning, Koga, and Kolasinski, 1985; Diehl *et al.*, 1982; Mnich *et al.*, 1983). Resistive hardening uses polysilicon intracell decoupling resistors to slow the regenerative feedback response of the bistable flip-flop, thereby discriminating between single-event voltage transients and the longer, legitimate write signals. A resistively hardened CMOS RAM cell is shown in Figure 5-5. The six-transistor cell has an ON transistor at each data node that couples the node to a supply voltage, which stabilizes the node against perturbations (Rockett, 1988). Resistor hardening involves a number of process problems; the process control of high-value resistors is difficult. Various other modes of decoupling are also being studied, including diodes, depletion-mode transistors, and resistor-capacitor combinations.

5.5.5.2 CMOS/SOS and CMOS/SOI Circuits

CMOS/SOS and SOI transistors are on an isolating substrate, so only charge from the portion of the track penetrating the silicon can be collected by the device (Campbell *et al.*, 1985). Funneling effects can be largely neglected. The charge collection from single-ion interactions with SRAM transistors can be modeled using two-dimensional computer simulations of basic transport processes (Rollins and Choma, 1987), and the effect of these interactions on the state of a cell can be studied using circuit-level simulation techniques. MOS/SOS SRAMs as large as 64K have been fabricated with error rates as low as 10^{10} error per bit-day. [Using Miller effect capacitor in the memory cell.]

In addition, 256K and 1M CMOS-bulk SRAM's using cross-coupled mercury cell resistors [Jacunski 1993 and Hadad 1994], 256K CMOS/SOI SRAM's using memory cell Miller effect capacitors [Swanson 1994] and 256K and 1M CMOS/SOI SRAMs using memory cell

cross-coupled gated transistor/resistors [Cohn, 1993 and Hite 1992], have all been demonstrated with $<10^{-10}$ errors per bit-day performance.

Depletion devices, configured to operate in their linear region, can be used as nonlinear resistors within a memory cell to decouple inverters during an SEU interaction (Hsueh and Napoli, 1985; Weatherford, Hauser, and Diehl, 1986). The advantages of such devices are that they are relatively independent of temperature and are very reproducible. The disadvantages are that they are not very area efficient and require significant process modifications.

5.5.5.3 Bipolar Digital Logic Circuits

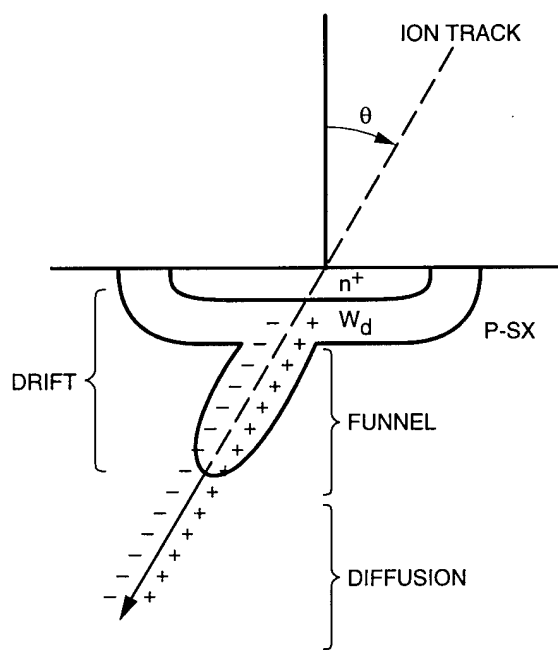
Bipolar devices are quite sensitive to SEU. Conventional bipolar circuits in many technologies, including TTL, and integrated Schottky logic (ISL), have demonstrated SEU susceptibility (Hauser *et al.*, 1985; Zoutendyk, Malone, and Smith, 1984) due to the intrinsic sensitivity of bipolar transistors and diodes to the charge-injection process. The isolation junction to the substrate is a particularly sensitive region because of the large active volume of the collector-substrate junctions. Various design approaches exist for minimizing the substrate effect, including insulating substrates (bipolar-SOI) and epitaxy on highly doped substrates. A gated-feedback element (such as a diode OR gate) may also be used to isolate the affected nodes (Berndt, 1988).

Techniques for removing the substrate component and for dealing with the remaining device components are listed in Table 5-4. All of the substrate-component techniques listed (except for redundant transistors with gated feedback) require additional process development for implementation into standard npn bipolar processes. In the gated-feedback redundant transistors, emitter-follower transistors are used to add "diode gating," whereby the collectors of the emitter-follower are connected to a low-impedance power-supply voltage to effectively remove the collector-substrate component.

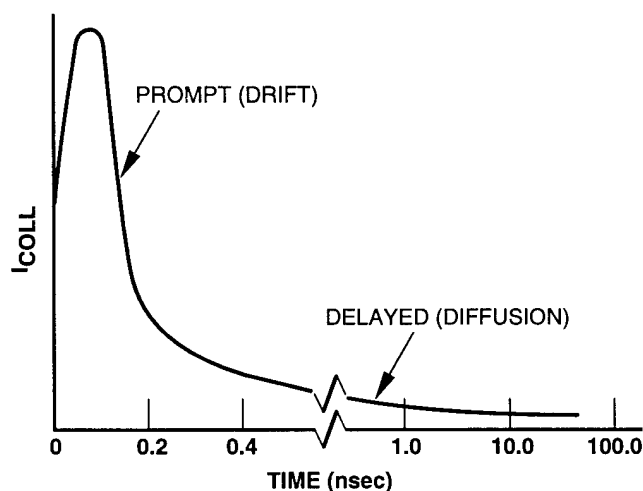
Of the techniques to remove the substrate-effect contributions to SEU, the most effective is to produce the circuits in a thin silicon layer

bounded by an CML/SOI insulator. This technique not only provides superior substrate isolation, but is also compatible with conventional bulk silicon processing steps; i.e., standard CML process can be run using an SOI wafer as a substrate.

The bipolar gated-feedback cell, diagrammed in Figure 5-5, is a fault-tolerant circuit approach that has been referred to as a "local vote scheme." The design prevents upset of a latch



(a) Cross Section of Ion Hit



(b) Collected Current Pulse Shape

Figure 5-4. SEU hit response descriptions (Kerns and Shafer, 1988).

when any one of its transistors is struck by an SEU event. When an OFF transistor has its normally HIGH collector node brought LOW by an SEU, the diode OR gate [D1 and D2, or D3 and D4 in Figure 5-5] isolates the affected node from the other side of the cell and continues to supply the required feedback current from a redundant transistor-load pair. The cell state can be sensed by a conventional OR/NOR gate and can be changed by driving both HIGH nodes on the same side of the cell LOW. Switching times can be as fast as 3 to 4 nsec for 20-mA current sources.

For this cell design to achieve minimum vulnerability to SEU, all devices except the diode gates must be fabricated in separate isolation regions to ensure that an event track will not "shunt" (Hauser *et al.*, 1985; Knudson *et al.*, 1986) charge between devices. Even with such isolation, a single point of failure still exists at the base nodes of the driver transistors. It is possible for charge collected at this node to be injected into other elements in the latch circuit, thereby destabilizing the logic state. The hardness of the cell is determined by the characteristics of devices attached to this node: the feedback diodes D, and the base resistors R, which are much easier to harden than the bipolar transistors themselves. Gated-feedback redundant transistors can be hardened by using SOI

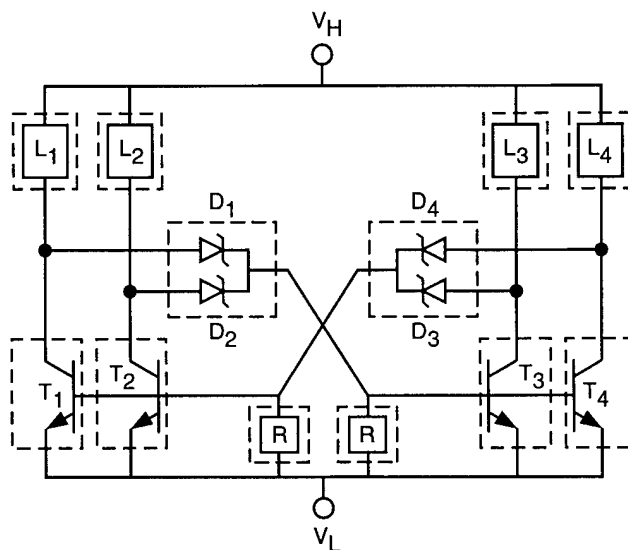


Figure 5-5. Circuit diagram of a gated-feedback bipolar SRAM (Kerns and Shafer, 1988).

Schottky, polysilicon, or emitter-base diode gating, or emitter-follower transistor gating. The diode gating techniques require process modifications to isolate the substrate component, while the transistor gating process is compatible with a conventional npn bipolar process.

The nonbipolar device structures are relatively insensitive to single-event substrate effects, either because they are heavily doped (resulting in minimal response to transient charge) or because they are isolated from the substrate. Thus, the SEU vulnerability of a latch using these structures is expected to be limited to the vulnerability of its collector-base junctions. Simulations predict that the critical charge for upset of the latch via hits to these junctions is 200 fC. Further reduction of the single-event sensitivity of such latches is possible through the use of special circuit techniques that specifically harden to single-event intradevice currents [Table 5-4, "Device Component" column]. These circuit techniques can be used either individually or in combination to increase the critical charge as well as to eliminate possible base-to-base currents, which can result in cell upset.

An example of a gated-feedback cell implemented in CML is shown in Figure 5-6. Emitter-follower transistors are used in place of Schottky diodes to make the cell compatible with a standard CML process. Their low-impedance connection to large current supplies limits their susceptibility to SEU by providing rapid resupply of charge to a struck node. Transistor-voltage clamps in parallel with the load resistors are positioned to increase the current onto any struck collector node, thereby reducing the duration of the perturbation resulting from the hit.

In this design, hardening is achieved primarily through the elimination or minimization of the single-event perturbations due to the substrate effect (in this case, currents collected across the substrate-collector junction). Single events can still result in upset due to intradevice currents (collector-base and emitter-base junction currents, or collector-emitter ion-shunt currents). The potential effects of single-event-induced base-collector currents are reduced by the filtering action of the resistor-capacitor networks in their feedback paths. With the possibility of large, destabilizing collector-substrate currents

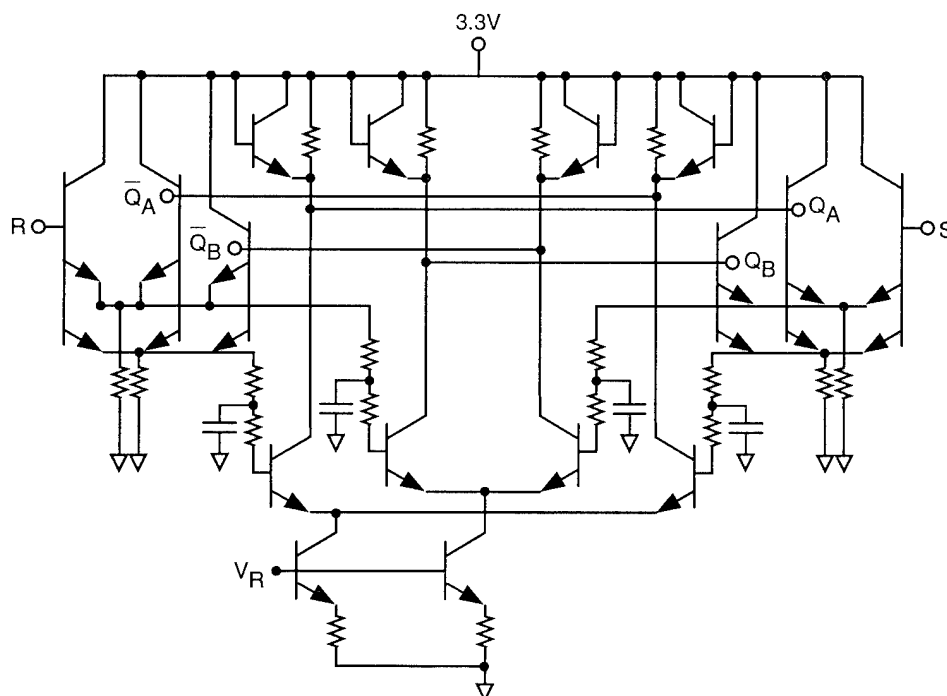


Figure 5-6. Circuit schematic for a gated-feedback CML SRAM cell (Kerns and Shafer, 1988).

removed, the base-circuit delay required to provide hardening is reduced.

The plasma track produced by a single event can provide a conduit, called an "ion shunt" (Hauser *et al.*, 1985; Knudson *et al.*, 1986), for charge redistributions between regions of like conductivity. Collector-emitter shunts can provide a path for the transport of enough charge to result in logic upset in bipolar latches. Dual emitter-follower circuit configurations can significantly reduce the number of SEUs caused by collector-emitter shunts in bipolar TTL circuits. An SEU hit at one emitter of a dual emitter-follower configuration does not perturb the other (redundant) feedback loop. This circuit design approach can also be insensitive to heavy-ion hits onto the resistors connected to the emitted nodes, if standard (bipolar-process compatible) p-type resistors on n-epi are used. Both the n-epi and the buried, heavily n-doped layer under the resistors are tied to the most positive voltage in the circuit. Therefore, hits on these resistors are similar to base-collector hits; they result in the associated resistor nodes being pulled HIGH, which isolates the effect of the hit.

While vulnerability to SEU is a severe problem in bipolar digital technologies, especially the low-power technologies, it is generally not considered to be critical in analog applications. The higher signal levels and generally high power dissipation of analog circuits mean that analog "information content" is represented by very large quantities of charge. In continuous-time systems, transient errors (glitches), such as might be introduced by a single heavy-ion hit, have effects that depend greatly on the system application. In most cases, single-event perturbations result in small noise-like contributions to device signal or power levels. SEU effects are not capable of altering the output signals of most modern analog bipolar systems, and therefore most designs are not influenced by consideration of these effects (Kerns and Shafer, 1988).

5.5.5.4 GaAs Technology Circuits

The GaAs technology (Kerns and Shafer, 1988) discussed herein is based on a high-mobility-type FET called the heterostructure field-effect transistor (HFET). The physical structure of an HFET device is represented schematically in Figure 5-7. [Similar transistor types produced by

Table 5-4. Summary of bipolar flip-flop hardening techniques (Kerns and Shafer, 1988).

<u>Substrate Component</u>	<u>Device Component</u>
Inverted transistors	Passive delayed feedback
IIL	Cross-coupled resistors
Collector diffusion isolation	Increased base capacitance
Dielectric isolation	Resistor-capacitor networks
DI process	Active delayed feedback
SOI process	Multiple gate delay
Redundant transistors with gated feedback	Filter networks
SOI Schottky diode gating	Higher device currents
Polysilicon diode gating	Higher voltage swing
Emitter-base diode gating	Separate feedback gates per base node
Emitter-follower transistor gating	Repeated diode or transistor gates
Highly doped substrates	Emitter-follower gates with multi-emitter
p- and p ⁺ -epi substrates	transistors
p ⁺ -barrier layer	

other manufacturers are called modulation-doped FET (MODFET), high electron mobility FET (HEMT), or HIGFET.] Metal-semiconductor FET (MESFET) transistors (Swanson, 1987) are fabricated in GaAs and related binary compound-semiconductor materials. Several elements (including aluminum, indium, and phosphorus) with matching valence electron structure can be substituted for some of the gallium and/or arsenide in GaAs, resulting in semiconductor compounds that have band structures similar to GaAs, but different bandgaps. The bandgap, and therefore the properties of mobile carriers in these materials, can be "tailored" by varying the proportion of substituted material. For instance, when aluminum replaces some of the gallium, the result is AlGaAs, which has a larger bandgap than GaAs. [Note that this type of replacement is different from conventional substitutional "doping" of the semiconductor, which introduces an element of *different* valence structure for one or both types of host elements. Bandgap-tailored semiconductors can be doped in the same manner that GaAs is doped.] In the technology discussed here, some portions of the device use doped and undoped layers of AlGaAs and GaAs semiconductors to form a "heterostructure." When thin, precise layers of AlGaAs and GaAs (or any other related semiconductors) are alternated in a periodic layered structure, the sequence, called a "super lattice," exhibits properties different than those of the component materials.

The HFET technology shows extremely high insensitivity to ionizing radiation dose. For all GaAs technologies produced to date, no special process or circuit design features have been required to achieve the highest ionizing radiation dose hardness levels required of space systems. GaAs technology is, however, susceptible to SEU.

A number of approaches to single-event-hardened, GaAs SRAM cells based on the enhancement/depletion HFET cell configuration have been investigated using computer simulation [see Figure 5-8]. [The n-channel depletion-mode transistors used as load devices in this cell are fabricated with an n-doped region between the source and drain, which can be turned off by ap-

plied gate voltage, while the n-channel enhancement-mode devices have the channel induced by applied gate voltage.] Of all the cell designs described and evaluated here, this cell requires the smallest chip area and has the fastest reading and writing speeds; it is also the most vulnerable to SEU. The SEU vulnerability of such designs is attributable to hits to the enhancement-mode transistors, M3 and M4. When a logic state is latched in the cell, the one transistor that is biased OFF is sensitive to SEU. Figure 5-8 includes the current sources used for modeling single-event perturbations to transistor M3, i.e., assumes node D is initially HIGH and DB is LOW.

The response of GaAs MESFETs and HFETs to alpha-particle single events has been measured using a $\text{Ci } ^{241}\text{Am}$ source. This test can be used to compare the single-event vulnerabilities of different FET structures to alpha particles. At all FET biases, the charge collected by HFETs was less than that collected by MESFET structures of equivalent dimensions. [MESFETs are fabricated without AlGaAs layers.] These results suggest that memories designed with HFETs will be less sensitive to single events than those fabricated with MESFETs.

Simulations of the basic memory cell using SPICE-compatible MESFET models (Golio, Hauser, and Blakley, 1985) indicate that it is more sensitive to drain hits than to gate hits, which is to be expected because drain hits directly discharge the stored HIGH voltage. The cell is also less vulnerable to gate hits because the low-impedance ON device can shunt a portion of the ion-induced charge to ground in the time that it takes the OFF device to begin conducting and discharging the stored HIGH level on the drain. This analysis is supported by measurements of the sensitive areas of the HFET structure to alpha-particle bombardment.

Several approaches to resistively decoupling SRAM cells in order to decrease their single-event vulnerability have been proposed (Weatherford, Hauser, and Diehl, 1986), one of which is illustrated in Figure 5-9. In this circuit configuration, a single event is isolated from one

part of the storage node via a resistive element. For example, a hit on the drain will not discharge all parts of the storage node; the capacitive components of the depletion device and the gate of the ON device will tend to retain their HIGH state, helping the cell to recover from the event without upset.

The resistance values needed to prevent drain-hit upsets in a 90-percent worst-case space environment (Adams, 1982) are on the order of 100 k Ω . A resistance of this magnitude limits the speed at which the cell can be written. Unless the system design can tolerate severe degradation in write-time performance, this design offers little promise. Moreover, the difficulties in manufacturing consistent high values of resistors are even greater in GaAs processes than in the silicon processes discussed above.

The cell configuration that offers the most promise for radiation-hardened GaAs SRAMs is the "8-transistor-cell" shown in Figure 5-10. This configuration utilizes two depletion devices in series with the gates of the enhancement-mode "driver" devices in the cell. The impedance of the series depletion devices raises the noise margin in the cell by allowing the HIGH node to hold to a voltage value above the Schottky-barrier height. Additionally, the impedances of the additional depletion devices are modulated by stored levels in the cell. For example, device M5 is ON "hard" (low-resistance state) when its gate is HIGH for a stored "1" on node N1, while device M6 is nearly OFF (high-resistance state), since its gate is negative with respect to its source. In this way, the cell responds "automatically" to increase the resistance protecting the vulnerable HIGH state on drain nodes, while simultaneously maintaining a low-resistance discharge path for ion-induced currents onto the gate node, thus hardening against both types of single-event hits. This configuration has the disadvantage of adding considerable area to the cell.

The addition of the depletion devices does not appreciably affect writing speed. In fact, because the internal write time for an individual memory cell is usually much faster than its read time, the cycle time of the memory is unaffected. There-

fore, the only price paid for SEU hardening using this design is cell area, which increases by 40 to 50 percent. The extra depletion devices do add additional sensitive nodes to the cell, because single-event hits to depletion devices can also result in upset. The critical charges for depletion-mode upsets are, however, significantly higher than those of the enhancement-mode upsets discussed above, making the introduction of the depletion-mode devices a clear net benefit in SEU hardening.

5.6 System-Level Hardening Guidelines

The system-design approach to design hardness that involves manipulation of the means by which a system performs its functions, i.e., the system concept, can be a very powerful approach if applied early in system development. Early recognition of the nuclear specification as a design constraint affords the system designer the opportunity to consider nuclear effects while generating the system concept, thereby avoiding functions that are difficult to realize in hardened form. The result may be an unorthodox system that ultimately is less expensive to develop, produce, and deploy than a conventional system on which considerable hardening effort is required at the circuit and part levels.

5.6.1 Hardened Information Storage

The radiation responses of memory functions are often critical to system vulnerability. There-

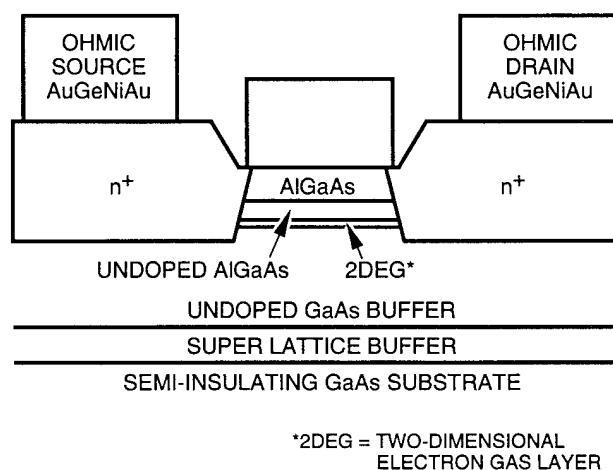


Figure 5-7. Cross-sectional representation of HFET device physical structure (Kerns and Shafer, 1988).

fore, hardened memories must be used when needed. The size of the critical memory should be minimized. Information can be stored in a variety of circuits to protect it from loss during radiation exposure. Single bits of information can be stored in latching relays or hardened flip-flops consisting of IC gates with RC networks on the input leads. Both storage means will retain information to very high radiation levels, but are slow in responding to signal changes. They are best suited for control lines where state changes are infrequent.

Magnetic storage, such as tapes, core or plated-wire memories and hard or floppy disks, can be used to protect information against upset where mass storage is required. Magnetic cores have also been used to store single bits of information where the dose-rate environment is very high.

The main goal of hardening information-storage circuits is to prevent external transients from coupling into the circuits where they can induce data errors. The control and/or data lines may have to be clamped during and after the radiation event until the system is reset or regains control over memory circuits.

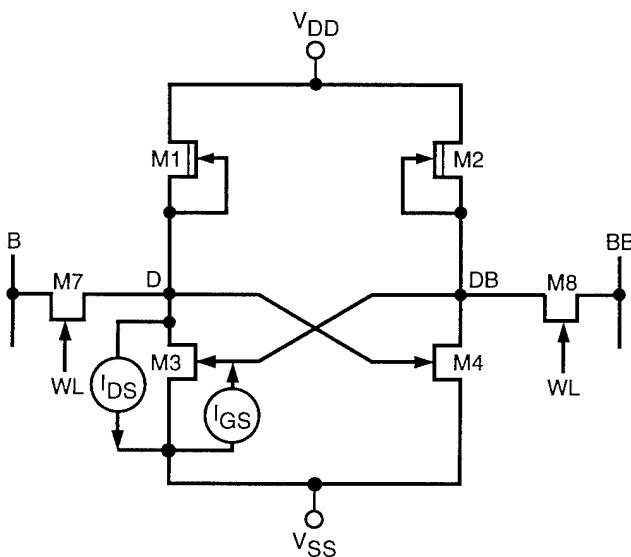


Figure 5-8. Circuit schematic of an enhancement/depletion MESFET SRAM cell showing possible single-event-induced currents (Kerns and Shafer, 1988).

Two problems to be resolved by system hardening against data errors are: (1) determining whether and where a system is writing into memory at the time of the radiation event, and (2) detecting and correcting any data that are scrambled when the writing process is interrupted. If data can be stored periodically, multiple memories or multiple locations in a single memory can be used to overcome these problems.

Transient photocurrents produce data errors in digital communication and data-processing systems in a manner similar to noise transients. Digital data can be encoded and used to minimize or eliminate the effects of photocurrents if the system recovers rapidly after the radiation event.

For slow data rates, a parity check bit could be added to each message word to detect a radiation-induced error. Assuming a protocol is set up between the sender and receiver, the receiver could detect the error, reject the message, and force the message to be transmitted again. If desired, an error-correction capability could be included in the encoding-decoding process.

5.6.2 Redundancy and Fault-Tolerance Techniques

From the standpoint of the redundancy and fault-tolerance techniques, radiation effects are similar to the effects caused by other IC failure mechanisms. Consequently, protecting against radiation-induced damage is the same as protecting against the other failure mechanisms. Two distinct yet complementary approaches to implementing digital designs are fault avoidance and fault tolerance. Fault avoidance attempts to implement circuits that do not fail. Fault tolerance recognizes the futility of attempting perfect design.

Fault avoidance is an optimistic philosophy that overlooks, for example, the fact that real components do fail and that no amount of shielding will protect against all external interference. Fault avoidance has limited applicability, especially for complex systems installed in relatively hostile environments that are expected to per-

form without incident for long periods of time (Sievers and Gilley, 1985). This methodology requires careful part selection and screening, conservative interconnection and packaging technology, shielding, and other failure-prevention measures.

Fault-tolerance philosophy acknowledges that failures will occur, that these failures will cause errors, and that those errors could propagate throughout the system if not located and isolated quickly. In a fault-tolerant design, protective redundancies are used to detect errors, isolate the malfunctioned unit, and correct the malfunction. Protective redundancy implies the use of components that would otherwise be unnecessary in a system in which faults never occurred. These redundancies provide for automatic detection, isolation, and recovery to normal operation, ideally without interruption of normal service. Fault tolerance is the unique attribute of a system that allows it to continue its specified behavior in spite of the occurrence of faults (Nagle, Miller, and McAllister, 1988).

Hardware fault-tolerance mechanisms involve the use of redundant hardware. Hardware redundancy can be static, which involves the use of fault-masking techniques within a module, or

dynamic, which involves the reconfiguration of system components in response to failures. Sometimes the reconfiguration means disconnecting the damaged units from the system. N-modular redundancy and hybrid redundancy is achieved by voting of the outputs of N-units in addition to having some backup spares. Temporal redundancy is concerned with repeating certain operations in time on the same hardware. It requires twice the computation time, a major drawback. Information redundancy is a special form of hardware redundancy in which extra hardware is organized to implement error-detection and correcting (EDAC) codes. A number of EDAC codes have been developed (Nelson and Carroll, 1987), the most commonly used codes being the Hamming and Cyclic codes. Cyclic codes have numerous modifications for special purposes (Pradhan, 1987).

Software fault-tolerance techniques include N-version programming, recovery block structures, consensus recovery blocks, and various reconfiguration of system components (Nagle, Miller, and McAllister, 1988). A summary of software fault-tolerant techniques is given by Chu *et al.* (1986).

It is often desirable to mix fault tolerance and fault avoidance within a single system. Experi-

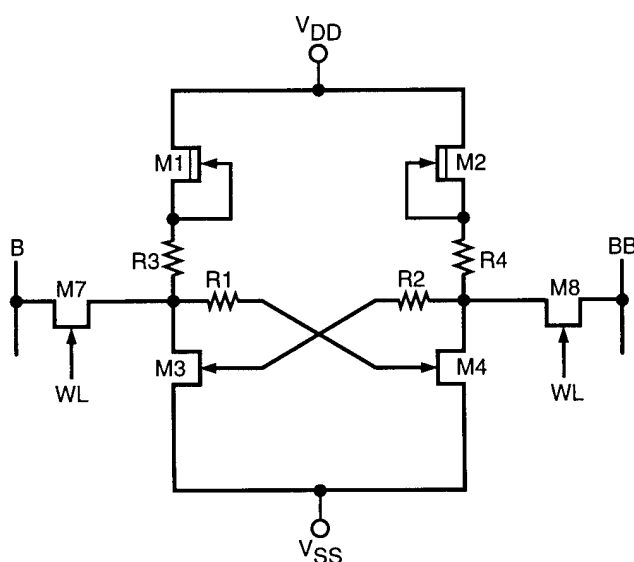


Figure 5-9. Circuit schematic of a resistor-decoupling approach to hardening and enhancement/depletion SRAM cell to SEU (Kerns and Shafer, 1988).

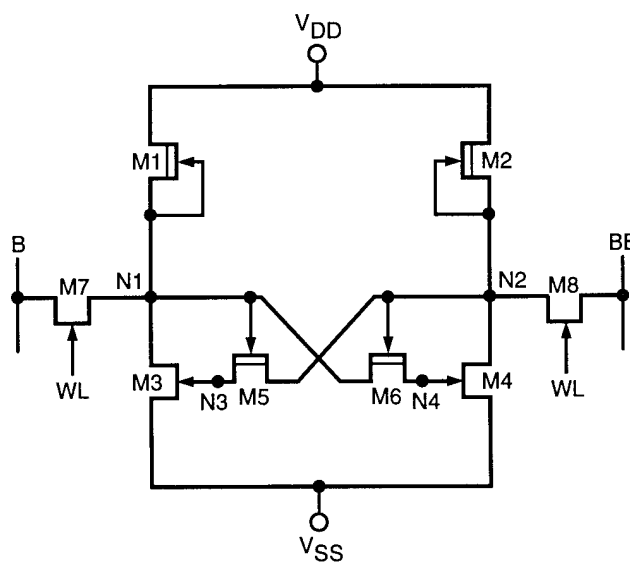


Figure 5-10. Circuit schematic of an 8-transistor cell to harden an enhancement/depletion SRAM cell to SEU (Weatherford, Hauser, and Diehl, 1986).

ence and analysis are necessary to determine the suitability of each method. Fault tolerance does not eliminate the need for good design or the use of the best components. Its real purpose is to provide cost-effective reliability and availability beyond that possible through the use of fault-avoidance techniques. Fault tolerance must be designed into a system; it is difficult or impossible to add fault tolerance after a design is complete.

5.6.3 Circumvention/Reset Techniques

Circumvention relies on detecting a nuclear event, ignoring radiation-induced transients, and, if necessary, turning off, or clamping, the system for a prescribed time during and after exposure. A detection system calibrated at a predetermined level is required to trigger the circumvention circuitry. Circumvention schemes usually are employed to protect system memory functions and inhibit irreversible output commands. The critical memory cells themselves must be hardened, and the transmission of input and output data must be protected from scrambling en route to and from the memory. Circumvention fulfills the latter requirement. The circumvention technique can be accompanied by a power interrupt to achieve hardness against burnout, latchup, and other unwanted irreversible actions.

A generalized circumvention scheme is shown in Figure 5-11, where the optional functions are enclosed in dashed lines. Assume that vital information, such as a computer program and accumulated results of computations, must be preserved throughout a nuclear burst. Assume also that an intrinsically hard memory is available that cannot be scrambled by radiation interactions in the memory cells themselves. If an unhardened semiconductor memory is used, the critical information stored in its memory must be duplicated in an auxiliary hardened memory prior to the nuclear event. The circumvention scheme is then designed to restrict data transfer to and from the hardened memory during the nuclear weapon induced transient. After the event, the protected critical information is returned to the primary semiconductor memory.

A typical chain of events in a circumvented

system may be followed from Figure 5-11. An ionizing-radiation or nuclear EMP pulse activates the circumvention circuitry by means of one of the radiation sensors. Two primary events are initiated in a very short time. First, a number of clamping and/or disconnect functions are initiated. As a minimum, the memory input/output lines are disabled; current clamps or power disconnects may be applied to the digital logic (or critical electronics elsewhere in the system) to reduce greatly the probability of burnout and unwanted irreversible commands. Second, a hardened circumvention timer is enabled. This timer may be designed for a specific circumvention interval, programmed manually, or depend on the mission profile. At the end of the circumvention time, the hardened timer issues a command to inhibit the clamping and/or disconnect functions and automatically resets the logic state according to predetermined design considerations. The memory and logic are then ready for normal data processing. While the computer is dormant, it does not receive and process any information and does not issue any commands. In most cases, the circumvention time can be made short enough so that any error introduced will be negligible. If not, the memory content must be updated via a preprogrammed routine that takes into account pre-irradiation data and the circumvention time.

Costs of developing a particular circumvention scheme must be weighed against the cost of comparable intrinsic hardness, recognizing that some degree of hardened memory is required in either case.

5.6.4 Operate-Through Technique

This system-design hardening approach utilizes the hardening technology being developed under the current DNA Operate Through (OT) Program. The approach for the OT Program is based on three primary elements:

- Fractional outage time based on mission objectives
- System functions not permitted to upset or lose timing control
- System functions that may be upset and/or circumvented with recovery and control within an allowable time.

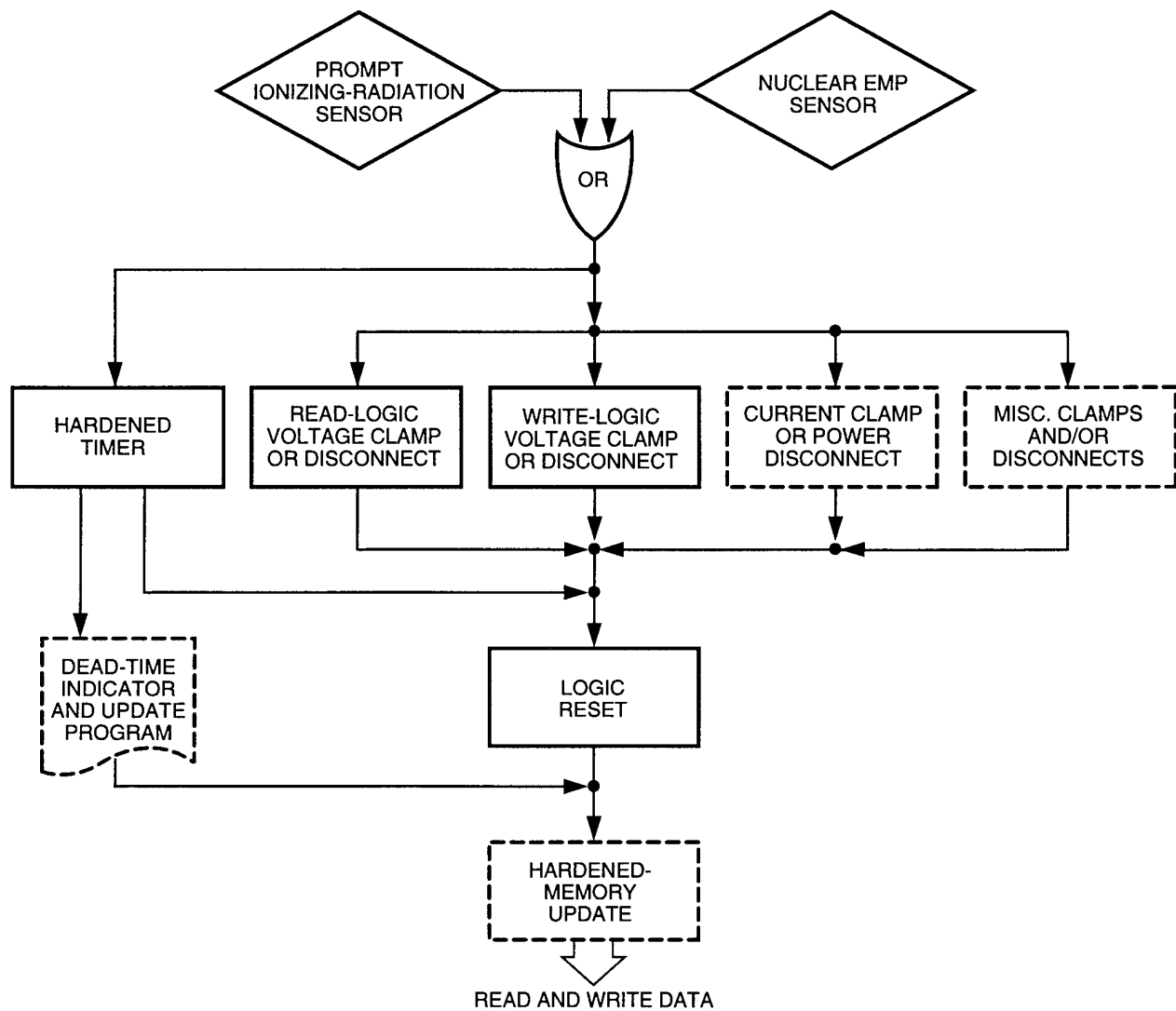


Figure 5-11. Generalized circumvention scheme (Espig, 1978).

The system-related operate-through hardening technique requires that a maximum allowable fractional outage time be calculated and that a circumvention time be established as a percentage of that outage time. The fractional outage is determined from the system performance specification and the imposed threat scenarios. Using these as the basis, a time during which the system's critical functions and corresponding processing and control may be inoperative and yet meet mission objectives is determined. This is the maximum allowable fractional outage, which may be budgeted to include different upset and recovery functions.

Circumvention time, composed of dose-rate detection, controlled operation interrupt, and time-out initiation and completion, is included in fractional outage. Another part of the allowable outage time must be reserved for electronics recovery from the dose-rate upset and is expected to be determined based on the longest functional unit recovery. This time is calculated from the time when the dose-rate level drops below the minimum upset threshold until after the longest saturation recovery time (tsr) is completed. Concurrent with electronic device recovery is the determination of the allowable outage time asso-

ciated with circumvention recovery or operation reinstatement, or the time required after the circumvention timer has timed out to reinitialize the processor electronics, recover the shut-down operating states, restart power, and any other start-up and reset efforts required. The combination of these three time lines must be sufficiently less than the maximum allowable outage time to ensure system operational recovery in order to account for all uncertainties. Figure 5-12 illustrates the time lines comprising the allowable outage period (Rose, 1991).

Nonupsettable memory and logic is another area of technology being applied and developed for dose-rate system-level hardening, and includes the development and use of fast-recovery architectures and algorithms with large-scale, fast, nonupsettable memory. Although the memory circuits have high upset thresholds ($>10^{11}$ rads[Si]/sec), the processor is allowed to upset at a much lower rate. The processor is prevented from initiating radiation-induced errors in the memory by a circumvention signal from a nuclear event detector (NUDET). When the circumvention signal is detected, all processing is interrupted and the read-write lines to the memory are disabled. A developed controller, the operate-through enhancement controller (OTEC), takes over and controls the processor timing and recovery using algorithms retained in nonvolatile read-only memory (ROM) until the NUDET enables recovery. When interrupted

with a NUDET signal, the recovery algorithm checks the special words in memory to determine if the nuclear event has corrupted the memory. If the words are good, a retry instruction backs up the program one instruction and continues. If the words are bad, the program executes an indexed restart to initiate the recovery routine (Rose, 1991).

5.6.5 Power-Source Hardening

The degree of hardening needed in power supplies and voltage regulators depends on whether the power source must remain operational during and after a radiation event. If a power supply is allowed to shut down, the output lines could be clamped to a low voltage to prevent burnout of the load circuits. Control circuitry, switching transistors, series-pass transistors or regulating ICs, and the clamping device may need series-limiting impedances to prevent burnout. If the load circuits have power-line capacitors, components on the circuit board may also need impedance-limiting to prevent burnout. Power diodes can be placed in the power lines to prevent reverse current flow to the power-supply clamping device(s).

If the power supply must remain operational through the radiation event, the components of the supply may need current-limiting. In addition, the output lines may require impedance-limiting to prevent excessive loading from photocurrents in the load circuits. The output

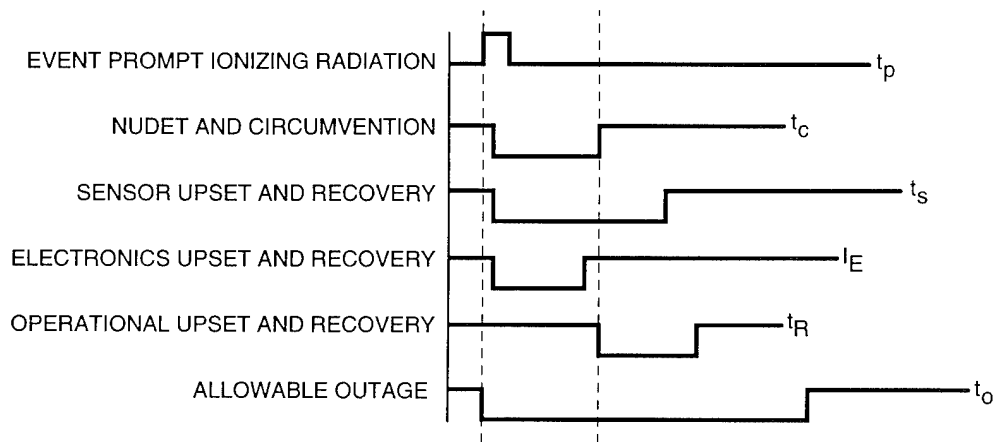


Figure 5-12. Time lines for allowable outage budget (Rose, 1991).

lines of the supply and/or regulators may be prevented from applying an excessive voltage to the load with proper selection of filter capacitors. Over-current and over-voltage protection circuits also need to be inhibited until the voltage-regulating loop(s) have returned the output voltages to their specified limits (Rose, 1991).

5.6.6 Time Sequencing and Time Delays

Time sequencing and time delays are useful for protecting digital controls that can be upset by photocurrent transients on incoming control lines. If two or more command signals are required to initiate a response, the signals can be time-sequenced to filter out erroneous transients. Photocurrent transients arrive at approximately the same time. Time-sequence circuits can be set up to reject simultaneous incoming commands. They can also inhibit receiving a second command until a set delay after the first command arrives. The time delay would have to be larger than the longest expected transient on any incoming line (Rose, 1991).

A time delay can also be used on a single command line by logically ANDing the original and a delayed signal together. The time-delayed and command signals would both have to be larger than the photocurrent transient. The time-sequencing or time-delay circuitry have to be hardened against upset for these techniques to be effective.

5.6.7 Periodic Reset

This technique is useful where physical damage or hazardous conditions occur if the system remains in a given mode too long. The technique involves applying a periodic reset signal to a system's mode-control circuitry to keep the system in a given mode of operation. When a radiation pulse upsets the circuitry, the reset pulse will automatically return the system to the desired operating mode. The pulse repetition time should be shorter than the response time of any physical mechanism involved (Rose, 1991).

5.6.8 Shielding Techniques

The most obvious approach to hardening an electronic system is to modify its environment, that is, to shield it. Shielding is an effective ap-

proach for hardening immobile surface-based systems such as missile sites and radars. Unfortunately, the often severe weight penalty associated with reducing the neutron and/or gamma-ray environment makes it much less attractive for mobile systems, particularly airborne or spaceborne ones. To compound the problem, shielding materials used for optimum neutron and gamma-ray shields are different.

Shielding is, however, an important supplementary concept in many critical instances. For example, in exoatmospheric systems (i.e., missiles and satellites), a relatively modest amount of shielding can be used to reduce the internal, pulsed ionizing radiation exposure from the x rays of a nuclear weapon exposure to a level comparable to that of the weapon's direct gamma radiation pulse. Another example of shielding is in the reduction of the electron and proton dose in a satellite exposed to the earth's trapped radiation belts. Again, modest amounts of shielding can be used to substantially reduce the ionizing dose to the internal electronics. Unfortunately, however, because the shielding generally cannot eliminate all internal ionizing dose to allow the use of unconstrained electronics, shielding is a supplementary hardening technique. Figure 5-13 shows the typical shielding inherent to a spacecraft for the natural radiation environment. The exterior components (solar arrays, sensors, and antennas) must be shielded separately, if necessary). Figure 5-14 shows the accumulated dose for a 5-year mission. The system designer must weigh the trade-offs of weight, power, and cost in reducing the environment at the electronics to acceptable levels (Ritter, 1989).

5.7 Analysis Techniques for Circuit and System Hardening

Two types of analyses are typically performed during the design and development of a system: design support analyses and qualification analyses. Both types of analyses use similar analytical techniques, but the emphasis is different. Design support analyses are used to interpret the survivability requirements, determine hardening concepts to be used in the system design, and assist designers in implementing hardening concepts at

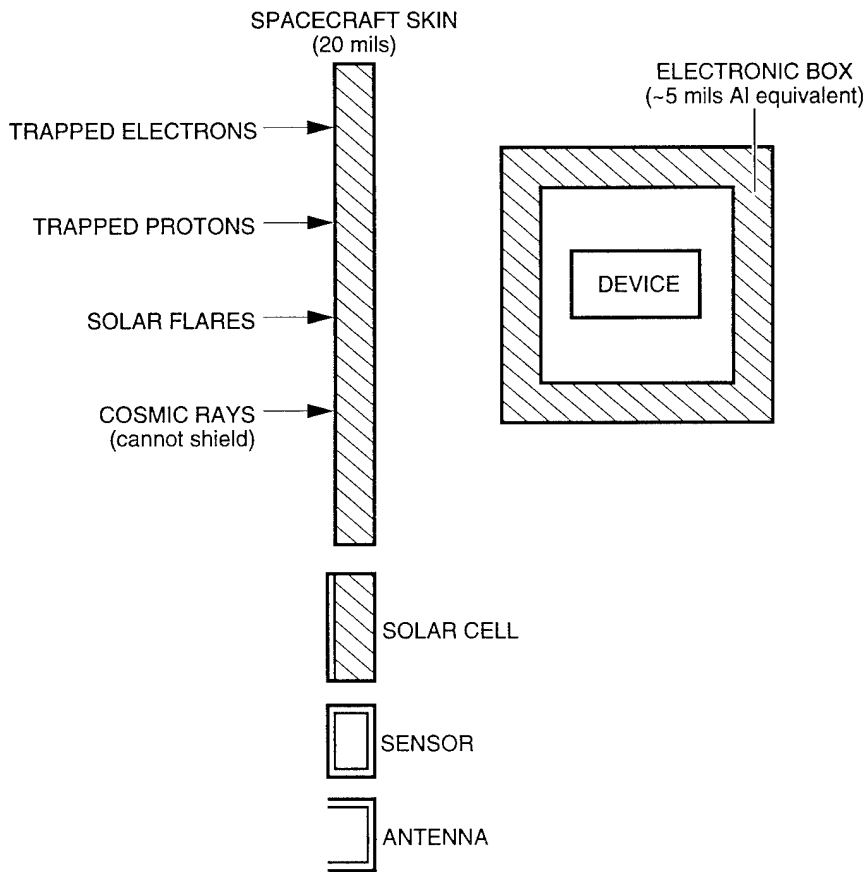


Figure 5-13. Typical inherent spacecraft shielding (Ritter, 1989).

the circuit level. After the circuit design is completed, qualification analyses should then be performed to show that the final design meets the survivability requirements. As a final step, circuit or system tests should be used with the analyses to verify the response predictions.

Two categories of network analysis are used to analyze the effects of nuclear radiation on circuits: simple analysis and complex computer-aided analysis. Simple analysis techniques are used for “quick-look” estimates and to analyze relatively simple circuits. Quick-look analyses are applicable for preliminary assessments to estimate circuit vulnerability so that circuits can be ranked according to their vulnerability levels to ensure that initial hardening efforts are devoted to the most critical areas. Quick-look analyses are also used to estimate the response of portions of complex circuits. The insight gained through

these analyses enables an analyst to better understand the results of computer-aided analyses and to discover errors in the computer solutions (Rose, 1991).

To use the simple analysis techniques, the circuit configuration must be simplified to a point that loop and node equations can be developed and solved. A simplified model for a photocurrent analysis could be used, where the photocurrents are represented by current generators in parallel with the semiconductor junctions [see Figure 5-15].

Computer-aided analyses are used to determine the nuclear radiation response of circuits with complex topologies and/or groups of circuits with interactive effects. Computer codes allow complex semiconductor models to simulate device response accurately. They also allow

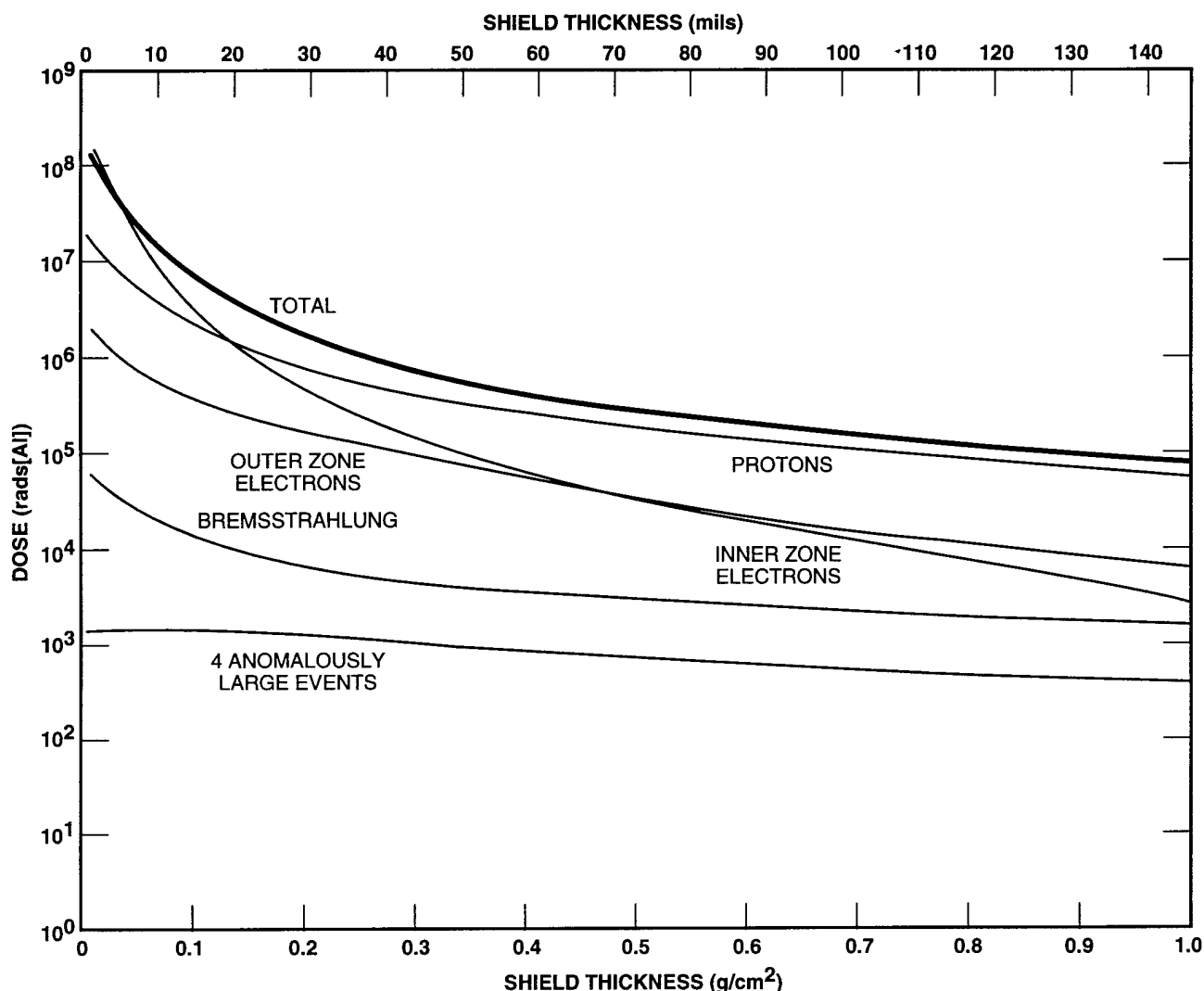


Figure 5-14. Accumulated dose over a 5-year mission as a function of aluminum shielding thickness for a circular, 60-degree orbit at 2,100 nmi altitude (Ritter, 1989).

a large number of interactions to take place simultaneously. The codes overcome many of the limitations of simple analyses, but are often expensive and time-consuming to run. They also require trained personnel who are aware of the numerical limitations of the codes and can recognize errors when they occur.

Many computer codes have been developed to determine the transient response of a single circuit or groups of circuits. The codes can also analyze circuits for burnout, upset transients, and recovery time. The capabilities of the codes vary somewhat, but they give nearly equivalent results if the complexity of the circuit and that of the

device models used are the same. A popular code used on modern personal computers is the SPICE code, developed by the University of California (Nagle, 1975; SAIC, n.d.).

The codes accept circuits of different sizes and are adaptable enough to make circuit changes from one computer run to the next. They are useful for trying various hardening features in a circuit to determine the optimum hardening approach. Circuits must usually be represented by discrete circuit elements, although some codes accept block diagrams for circuits and/or equations to represent variable circuit parameters. Semiconductor models are normally quite com-

plex in order to accurately simulate the voltage drops, capacitive effects, and leakage currents found in actual devices.

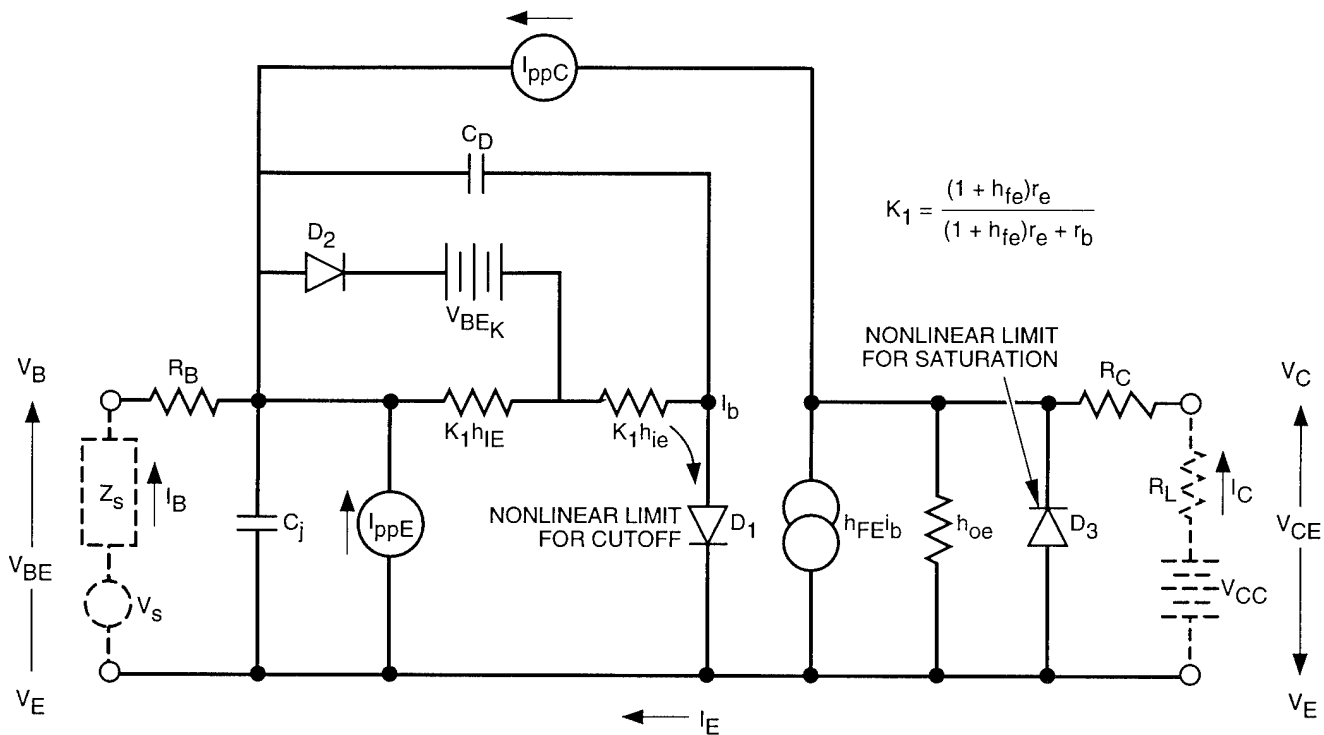
5.7.1 Device Models

A large number of device models are now available, providing the user with the flexibility of entering virtually any device and circuit model (in proper program format, of course). In addition to accepting user models, the user models can be stored on a temporary or permanent basis and later changed. Built-in models also are available with the option of parameter changes by the user.

In general, the method of storing, manipulation, and using the equivalent circuit models and

associated data for the analysis of active networks is limited only by the creativity of the user. Another prime consideration in application of the programs is the ease with which the numerical data required to use the various available models can be obtained. For TREE analysis, characterization of radiation effects is required in addition to electrical parameters, which may require radiation testing or prediction techniques.

Several bipolar transistor models have been created. The large-scale Ebers-Moll model (Ebers and Moll, 1954), and the charge-controlled model (Beaufoy and Sparkes, 1957) are, by far, the most widely used device models. These models differ primarily in the choice of independent variables and the degree to which they



WHERE:

- R_B = TOTAL DEVICE BASE RESISTANCE (EQUIVALENT "T" CIRCUIT)
- R_E = TOTAL DEVICE EMITTER RESISTANCE (EQUIVALENT "T" CIRCUIT) = $0.026/I_E$
- C_D = DIFFUSION CAPACITANCE = $1/\omega_\tau R_E$
- C_j = BASE-EMITTER JUNCTION CAPACITANCE

Figure 5-15. Schematic of a common-emitter radiation-equivalent circuit (Rose, 1991).

can be made to correspond with physical reality. The independent variables are current for the Ebers-Moll model, minority-carrier charge for the charge-controlled model. Using similar assumptions, the models are mathematically equivalent and will produce identical results (Hamilton, Lindholm, and Narud, 1964). From basic diode and transistor models, it is possible to construct a wide variety of more complex models (Cordwell, 1969).

Many of the models and modeling techniques are well documented in the open literature and in the manuals for specific programs. Simon *et al.* (1979) contains an extensive collection of discrete and integrated circuit device models. In addition to the nonlinear Ebers-Moll and charge-controlled models, programs also use the well-known linear device models, such as the h-parameter and the hybrid-pi transistor models (Cordwell, 1969). Models have been developed for pn-junction diodes, rectifier diodes, voltage-reference diodes, tunnel and backward diodes, vacuum tubes, gas tubes, magnetic devices, bipolar junction transistors, unijunction transistors, junction field-effect transistors, insulated-gate field effect transistors, microcircuit elements, and four-layer junction devices of various types.

Modeling integrated circuits presents special problems because of the distributed nature of these devices and the influence of the substrate in junction-isolated integrated circuits. Considerable progress has been made, however, in achieving reasonably accurate and expedient models of integrated circuits for radiation environments (Beezhold, Bowman, and Johnston, 1968 and 1971; Cifersky *et al.*, 1969; Cordwell, 1969; Pocock, Krebs, and Perkins, 1974; Pocock and Krebs, 1974; Pocock, 1975).

Two possible approaches to modeling integrated circuits are detailed modeling and simplified modeling. *Detailed modeling* of the elements that make up the IC requires knowledge of its actual structure, including the parasitic devices. Such information is difficult to obtain since manufacturers are usually not willing to release it, and direct measurement of individual devices in the IC usually is not possible. Further-

more, such detailed IC models require large amounts of memory and computing time, limiting the number of ICs that can be treated in any one simulation. Detailed modeling of ICs may be applicable to the study of IC response, but is not generally appropriate for the study of system response.

Simplified modeling simulates the IC with the responses as measured at the terminals to provide the correct voltages and currents as a function of time and stimulus. This modeling is made without regard to the actual electronic devices within the IC that produce that response, and simplified models frequently bear little resemblance to the physical properties of such devices. A simplified model is really only a mathematical description of the measured response of an IC to certain stimuli.

While a detailed model might be used to *predict* IC response, a simplified model can only *simulate* IC response. If a simplified model is applied to regions where the simulation is not valid, the resulting predictions of system response can be grossly in error. In addition, the sophistication of the simplified model may be limited by the properties of the particular circuit analysis code used.

Increased model sophistication results in increased memory requirements, running times, and chances for error. The simplest model that meets the required needs for a particular situation should always be used. It must also be remembered that the requirements of simplified modeling for linear and digital integrated circuits differ considerably (Simon *et al.*, 1979). For definitive work on simplified modeling, refer to Alexander, Turfler, and Ray (1977), Greenbaum (1973), Pocock *et al.* (1972), Pocock, Krebs, and Perkins (1974), and Raymond, Pocock, and Johnson (1971).

5.7.2 Ionizing Radiation Dose-Rate Effects

Three basic types of dose-rate analyses should be considered: the "survive," "operate-through" (or no-upset), and "recovery-time" requirements. The survive (or no-burnout) requirement is addressed on all mission-essential functions of the

system. The operate-through and/or recovery-time requirements should be addressed on all system functions that operate during the radiation pulse or that must recover within a specified time.

Two problems encountered in the use of simple analysis for dose-rate effects are the representations of photocurrent waveforms and the time delays due to the junction capacitances of the semiconductors. The analysis should be performed in steps to simulate circuit transient response as accurately as possible. Piecewise linear models of the photocurrent waveforms can be developed for these simulations.

For cases where an upper bound of circuit response is sufficient, the photocurrents can sometimes be represented by constant current sources. A dc solution of the circuit operating point is then obtained. The magnitude of each current source is the peak photocurrent for that particular junction. This technique is often used to show that the effects are not great enough to upset a circuit, even in a steady-state condition.

Photocurrent response of a device is sometimes represented by a rectangular pulse. The magnitude of the current source is set equal to the peak of the actual photocurrent waveform, and the duration of the pulse is the sum of the radiation pulse width, the time delays of the device, and any radiation storage time.

A burnout analysis is usually limited to semiconductor devices, since the passive elements in a circuit have much higher power-failure levels. Two approaches may be used:

1. Demonstrate device survival by testing under more severe conditions than the present requirements
2. Calculate criteria for each device and compare them with parameter values.

Usually a combination of these approaches is used when analyzing a system.

The first step in an upset analysis is to determine the critical portion of the circuit that is required to operate through an event. Circuits that interface with this portion must also be examined, including power regulators. Detailed

analysis will be performed on the critical circuits and all interface circuits that contribute important transients.

The settling time of a circuit is a complex analysis, usually dominated by time constants associated with a circuit's capacitive and inductive elements. Power-line recovery time should be summed with the settling time for the overall recovery time. Wherever possible, measured transient waveforms should be used in the analysis.

Results of the dose-rate analyses should be summarized and documented in a hardness-critical item (HCI) list. For each active semiconductor, the worst-case design margin (DM) should be calculated and documented, along with the conditions on which the DM was determined.

5.7.2.1 Example Upset Calculation

The circuit in Figure 5-16 is used to illustrate an upset calculation. This circuit (2N3380) turns on with a gate-source voltage (V_{GS}) = 0 and turns off when V_{GS} = 10 volts. The primary photocurrent (I_{pp}) will flow through the gate resistor (R_g), as indicated. If the JFET is turned off (V_{GS} = 10 volts), then the photocurrent that causes a 10-volt drop across R_g will turn on the JFET; i.e., I_{pp} = 0.1 mA. The 2N3380 has a I_{pp} of approximately 8 mA at 3×10^9 rads(Si)/sec. In this application, this circuit is predicted to upset at 3.8×10^7 rads(Si)/sec.

The upset threshold can be raised by lowering R_g . A factor of 10 reduction in R_g provides a factor of 10 increase in upset threshold. The threshold can be increased further by increasing the gate voltage bias for the OFF state.

5.7.2.2 Example Recovery-Time Calculation

The circuit in Figure 5-17 illustrates a recovery-time calculation. This circuit is designed to provide a delay between the Q_1 and the Q_2 turn-on. In normal operating conditions, both Q_1 and Q_2 are in the OFF state and C1 is discharged. The 741(U1) exhibits a positive output voltage transient that lasts for approximately 20 msec at 10^8 rads(Si)/sec. Since transistors have shorter

response times, U1 controls the ON time of Q_1 . Q_1 will be ON for approximately 20 μsec . The R6/C1 network, however, isolates Q_2 from Q_1 during this period. The turn-on time for Q_2 is

$$t = (R6)C1 \ln \left[1 - \frac{V_{VR1} + V_{BE}(Q_2)}{V_{CC}} \right] \quad (5.1)$$

$$= 522 \mu\text{sec}$$

5.7.3 Ionizing Radiation Dose and Neutron Effects

Early in the circuit-design phase, a piece-part analysis should be performed to determine the derating criteria for a radiation-degradation-tolerant design, wherein each part is reviewed to determine the part parameters that will be significantly affected by neutron degradation. Table 5-5 lists some of the more important part parameters and criteria that determine when a part will potentially fail and result in circuit failure. PAR(FAIL), the value at which the particular parameter of importance fails to meet specifications, is determined during this analysis, and it is used to denote the published capability value of the parts or circuits for the given application. Parts that degrade beyond the criteria shown in Table 5-5 should be rejected from consideration and replaced with devices that are more radiation-tolerant.

After the degradation effects and levels have been determined or estimated for the susceptible part parameters, ionizing radiation dose and neutron effects can be combined with the degrading effects of temperature, aging, and manufacturing variations. The total variations of the part parameters are the derating criteria used in hardening the circuits.

The ionizing radiation dose and neutron assessments of initial circuit designs should be performed simultaneously with the photocurrent analyses to determine design survivability. Transient upset and recovery-time analyses for ionizing dose and neutrons usually are not performed unless an upset or recovery-time requirement exists, and transient degradation in the semiconductors could affect the performance of the circuits that cannot be allowed to upset. For example,

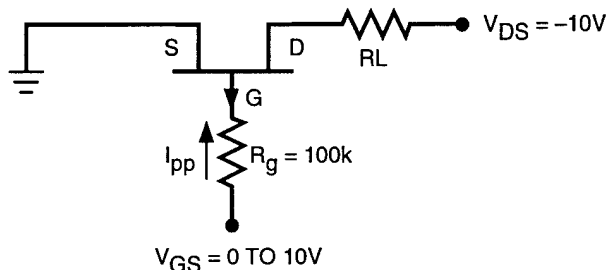


Figure 5-16. JFET circuit (2N3380) used to illustrate an upset calculation (Rose, 1991).

the series-pass transistor in a voltage regulator supplies power to circuits that must operate through the nuclear environments. The transient portion of the transistor gain (β) degradation may be sufficient to temporarily preclude delivery of the regulated power if its base drive is limited. Such cases are an exception, but may be encountered if the transient ionizing dose and neutron degradation is not compensated for in the design. Consideration of the transients should be included in the analysis if short recovery-time or upset requirements are imposed on the circuit.

The analyses must address whether the degradation from the radiation environment will cause the circuit functions to degrade beyond their specified limits. Complete part or circuit failure should not occur if soft parts are deleted from the design and the derating criteria are properly applied. Most of the analyses cover the effects of individual piece-part degradation on circuit element performance. In some cases, such as servo-control loops of complex discrete circuits, it may be necessary to consider the simultaneous changes caused by a number of piece parts degrading together.

5.7.3.1 Screening Analysis

Screening techniques should be used in the assessment analyses to eliminate components that are hard to the neutron or ionizing-radiation-dose environments in their applications and to identify sensitive parameters of components that need to be investigated in the detailed analysis. The first step in the screening process is to determine qualitatively the component parameters that can

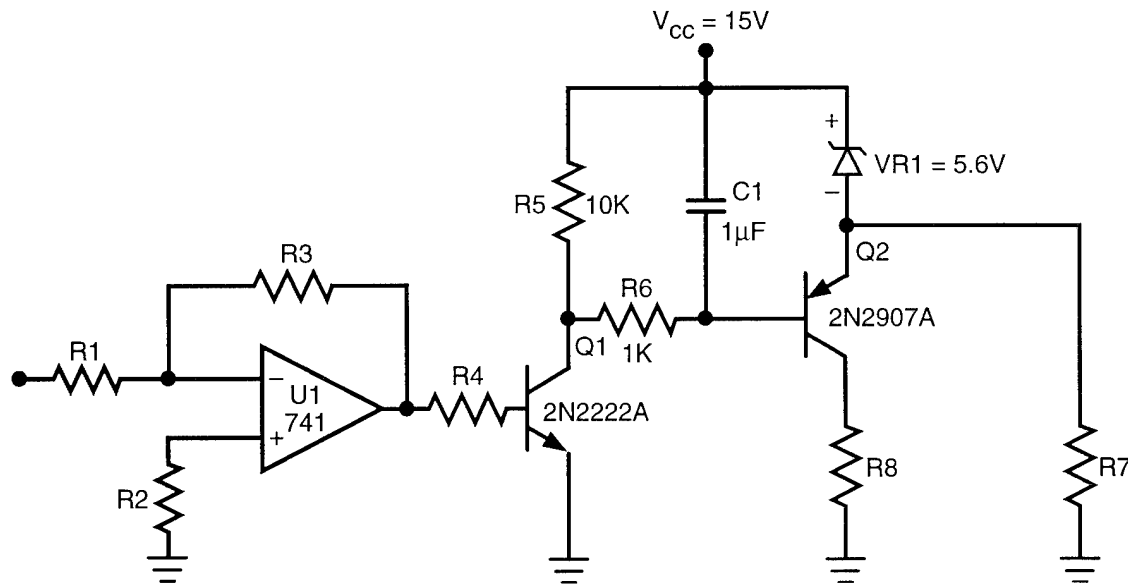


Figure 5-17. Example circuit for recovery-time analysis (Rose, 1991).

possibly cause a circuit failure. Each component in a circuit is reviewed to determine whether any of its parameters show significant degradation at ten times the specified neutron or ionizing radiation dose level. Table 5-6 lists a number of the possible parameters that may be considered.

The circuit design should also be reviewed from a functional viewpoint to determine whether any piece-part parameters have a particularly sensitive effect on circuit performance. If small changes in these parameters could cause a circuit failure, they should be included in the detailed analyses.

5.7.3.2 Detailed Analysis

The detailed analyses of sensitive parts can be performed using either deterministic or statistical approaches. The deterministic approach analysis can be done in two ways: (1) threshold failure determination, and (2) circuit transient response determination. The first method is to determine the maximum or minimum allowable value (failure threshold) of each sensitive parameter of the circuit's sensitive piece parts. The allowable value of each parameter is then compared with its derated value to determine whether the device is hard for that application. The second method

Table 5-5. Examples of device failure thresholds (Rose *et al.*, 1981).

Device	Parameter	Change (percent)
Small-signal diodes	Forward voltage, V_F	+50
Rectifiers (PIN)	Forward voltage, V_F	+50
Voltage-reference diodes (zener and avalanche)	Breakdown voltage, V_{BR}	± 1
Bipolar transistors	dc gain	-50
Four-layer structures	Forward ON voltage	+50
Digital and linear ICs	Input and output levels	Application dependent
LEDs	Light output intensity	-50
Phototransistors	Efficiency	-50

inserts the derated values and/or transient degradation values into the circuit model for each of the sensitive device parameters simultaneously. The circuit's transient response or shift of operating point is then determined and compared with the circuit's failure criteria.

Threshold failure determination is normally used where the failure of an entire circuit or a portion of a circuit is caused only by a single parameter of a sensitive device. The maximum allowable variation of the parameter can usually be determined through a simple dc analysis. Nominal or worst-case parameter values may be used for the remaining device parameters of the circuit. Worst-case parameter values selected should minimize the amount that the sensitive parameter can change before a circuit failure occurs. The worst-case variations may make it more difficult for a sensitive parameter to pass the failure criteria, but will provide more assurance that all the manufactured circuits will be hard to neutron and ionizing radiation dose environments. The worst-case parameter method can also be used with the circuit analysis codes.

Circuit transient response determination is normally used when failure of a number of sensitive devices contributes to a circuit failure. If the sensitive devices interact, it can be difficult to assign a failure threshold to each of the parameters that degrade. The degraded parameters, therefore, are entered into the circuit model simultaneously, and the response is determined at the circuit level rather than at the device level. Depending on the circuit complexity, simple or computer-aided analysis techniques may be used. Computer analysis techniques are useful for problems involving the response of servo loops. They are useful for analyzing circuit response when the transient annealing of damage in the transistor(s) is critical.

Detailed analyses may also be performed using statistical approaches. The statistical approaches are presently set up to calculate the probability of circuit survival $P_s(F)$ when the gain of a transistor is degraded. For a single transistor, two equations have been developed to calculate $P_s(\Phi)$. The first uses a manufacturer's

Table 5-6. Screening parameters for various device types (Durgin, Alexander, and Randall, 1975).

Device Type	Principal Screening Parameter
Low-power bipolar transistor	f_T, h_{FE}
Power bipolar transistor	$f_T, h_{FE}, V_{CE(SAT)}, t_s, BV_{CBO}$
Signal diode	I_s, BV, C, t_s
Thyristor	$V_{breakover}, V_{ON}$
Digital ICs	V_{OL}, t_{PD} fan-out
Linear ICs	Slew rate, $Z_{IN}, A_{VOL}, I_{OS}, V_{OS}, I_b$

Legend:

A_{VOL} , open-loop voltage gain
 BV , breakdown voltage
 BV_{CBO} , collector-base breakdown voltage
 C , capacitance
 f_T , unity gain bandwidth product
 h_{FE} , gain
 I_b , input bias current
 I_{OS} , input offset current
 I_s , saturation current
 t_{PHL} , propagation delay
 t_s , storage time
 $V_{breakover}$, breakover voltage
 $V_{CE(SAT)}$, saturation voltage
 V_{OL} , output low voltage
 V_{ON} , on voltage
 V_{OS} , input offset voltage
 Z_{IN} , input impedance

minimum β and f_T , as follows:

$$P_s(\Phi) = F_n \left\{ \left[\ln(CTF - 1) + \ln \left(\frac{f_{T \min} / \beta_{\min}}{\Phi} \right) - m \right] / \sigma \right\}, \quad (5.2)$$

where

CTF is the circuit tolerance factor ($= \beta_{\min} / \beta_T$)

β_{\min} is the minimum beta specification value

- β_T is the failure threshold for β
- f_{Tmin} is the minimum cutoff frequency specification value
- Φ is the neutron fluence
- m is the mean value of the K_D value distribution
- σ is the standard derivative K_D value distribution
- K is the damage constant.

and F_n is the normal cumulative distribution function.

The second approach uses an equation developed to determine $P_s(\Phi)$ when test data for K and the distribution of β are known:

$$P_s(\Phi) = 1 - F_n \left[\ln(\beta_T) + m_0 + \ln(A + \Phi)/\sigma_0 \right], \quad (5.3)$$

where

- m_0 is the pre-irradiation mean value of the K -value distribution
- A is $1/K\beta_0$
- β_0 is the pre-irradiation value of β
- σ_0 is the pre-irradiation standard deviation value.

Equation 5.3 is more accurate and much less conservative because it uses actual test data for the device being analyzed.

The statistical equations for $P_s(\Phi)$ are useful only when the circuit failure is due to neutron degradation of a single transistor. If a number of transistors or other devices contribute to the circuit failure, Monte Carlo methods, such as those given in Durgin, Alexander, and Randall (1975), should be used. Also, the statistical model does not address h_{FE} changes due to ionizing radiation dose degradation, temperature, or end-of-life effects. Details of the statistical approach and equations can be found in Rose *et al.* (1981).

The ionizing radiation dose and neutron analyses should be performed in accordance with the guidelines as presented in Military Handbooks 279 (ionizing radiation dose hardness) and 280

(neutron hardness) (MIL-HDBK-279, 1985; MIL-HDBK-280, 1985). [Military Handbook 279 was formerly published as DNA 5909F and Military Handbook 280 as DNA 5910F.]

5.7.4 Single-Event Effects

Figure 5-18 illustrates the measurements and analyses required to make an error-rate prediction for a memory circuit operating in a cosmic-ray environment in earth orbit. Analytical modeling of heavy-ion effects is necessary because extrapolation of test results to the space environment is difficult (Pickel, 1983). Single-event phenomena (SEP) are more fully discussed in Chapter 3. Essentially, the problem is to determine a critical charge for causing upset in the device, and then performing an analysis to evaluate the probability that the ions in the selected environment will interact with the device charge-collection region and produce the critical charge. The two ways to do this — experimental and computer-aided transient circuit analysis — are indicated in Figure 5-18.

Figure 5-19 shows a typical memory cell model for use in computer-aided analysis of a CMOS flip-flop. The cosmic ray is simulated by application of a current pulse from a generator placed in parallel with the appropriate junction in the circuit. Critical charge is the time integral of the minimum current pulse to cause error. The calculated critical charge is then combined with the modeled environment and the sensitive region analysis to arrive at the error-rate prediction. Pickel and Blandford (1983) and Massengill (1993) provide further insight into SEU modeling.

The first SEU prediction program was CRIER (Cosmic-Ray-Induced Error Rate), developed by Pickel and Blandford (1980). CREME (Cosmic-Ray Effects in MicroElectronics), a computer program based on a series of NRL reports, was produced in 1982 and an update published in 1986 (Adams, 1986). The CREME upset calculation is functionally equivalent to CRIER but, in addition, programs for deriving the ion environment considering geomagnetic shielding, weather conditions, material shielding, etc. are provided. SEU prediction programs require device test and

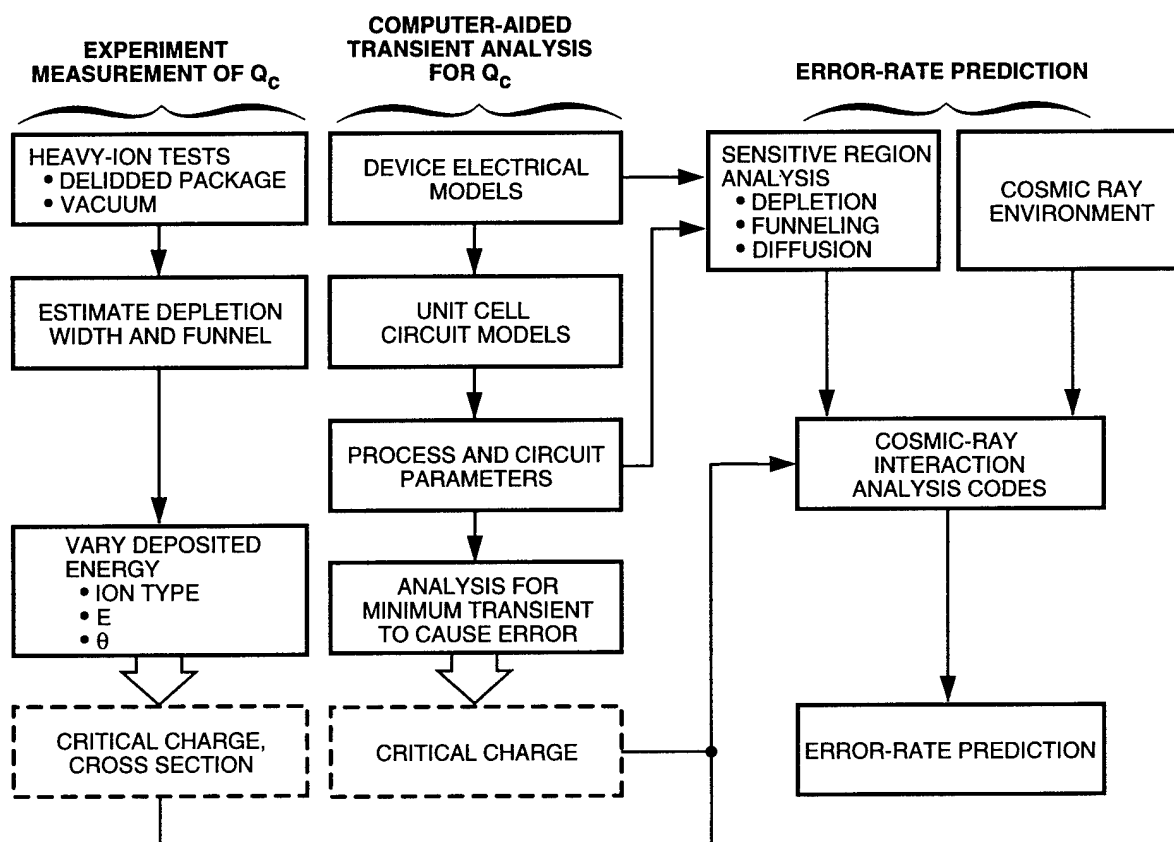


Figure 5-18. Measurements and analyses required for error-rate prediction (Pickel, 1983).

technology data as input parameters. At its simplest, the test data include linear energy threshold (LET) and cross section, and the technology data require definition of the sensitive volume, or volumes, within a device.

The CREME programs are a group of FORTRAN routines that calculate differential and integral energy and LET spectra of cosmic rays incident on the electronics inside any spacecraft in any earth orbit. Input parameters for running these programs describe the interplanetary and magnetospheric weather conditions, spacecraft orbit, the shielding surrounding the electronics, and the characteristics of the device under consideration. Input data files contain tabulations of stopping powers and ranges of cosmic-ray nuclei in aluminum and silicon and geomagnetic cut-offs. The output files contain energy and LET spectra and SEU error rates. Modifications intro-

duced by Daly (1989) allow the direct introduction of the experimentally measured upset cross section versus LET curve to account for the fact that the upset rate does not saturate rapidly at a unique LET.

The SPACE RADIATION PC program, developed by Letaw, Severn Communications Corporation in 1989, is based on CREME but includes trapped protons. The user may specify the orbit and the shielding material. The output includes SEU rates and absorbed dose. In the future, it will include the electron environment and dose calculation.

The CUPID (Clemson University Proton Interaction in Devices) program (McNulty, 1990) covers proton-induced spallation reactions and determines SEU cross section as a function of the critical charge for a sensitive volume of defined dimensions.

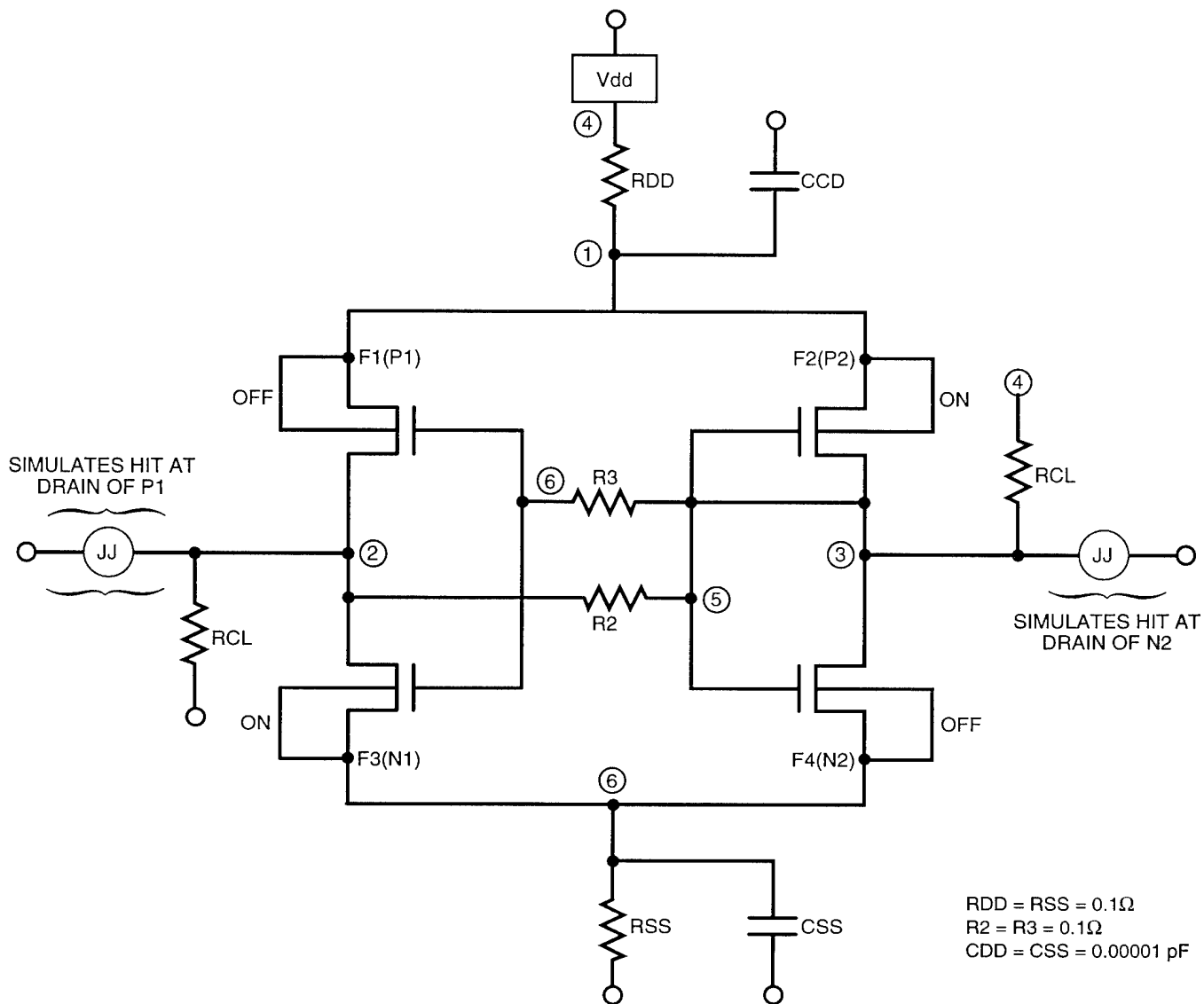


Figure 5-19. Memory-cell model for computer-aided circuit analysis to determine critical charge (Pickel, 1983).

Currently, the only generally available computer codes capable of predicting the single-event vulnerability of random logic are circuit-level codes such as SPICE (Nagel, 1975). These codes are cumbersome (if not impossible) for evaluating circuits with large numbers of logic elements.

5.8 Radiation Testing Considerations

Radiation tests must be performed at the part, circuit, module, and system levels to verify hardness for any system for which the environment is not trivial, and for which a quantitative estimate of its nuclear survivability is required. The two

general types of tests are engineering design tests and verification tests. Engineering design tests are usually conducted at the part and circuit levels. Verification tests are usually conducted at the module and subsystem levels.

Parts testing is often a central activity in a system-hardening design program. The reason for parts testing during design is to simulate ionization, displacement, and electrical stress in the laboratory with the objective of (1) generating design data, (2) generating modeling data for circuit analysis, or (3) verifying analytical/empirical predictions of part responses (Espig, 1982).

Parts testing is required because of the statistical nature of the responses of parts to a given environment. The behavior of individual parts is variable, even among parts of supposedly identical ancestry, because the parameters that impact radiation response are sometimes not well controlled by manufacturers. It is possible to perform adequate tests at the part level to establish the statistical variation of parts responses, whereas it is impractical to perform these tests at the circuit or module level. The resulting parts data, coupled with knowledge or an estimate of system-survival probability, are used in selecting types for the system and determining the hardness-assurance measures required during parts production.

Circuit testing in radiation environments verifies the results of circuit vulnerability analyses; it is the primary means for establishing credibility in the analytical approach. The circuits selected for testing should be those with the lowest confidence in analytical prediction.

Module and subsystem testing is conducted to: (1) verify the results of module and subsystem vulnerability analyses, and (2) respond to the hardness-verification requirements that may be imposed by the procuring agency. Module and subsystem tests are not conducted to verify hardness against a nuclear threat because they alone are inadequate for this purpose. Due to the high instrumentation and facility costs of these tests, it is essential that they be success oriented. Such an orientation can be achieved by design margin or by an adequate analysis/test program prior to final tests and analysis. A subsystem test can be considered a complete success only if the observed responses are consistent with corresponding predictions. Any deviation, even though apparently not representing a system failure, must be explained (Messenger, 1969).

All radiation tests should be conducted at several levels, if possible, to maximize the database. The levels of irradiation should include a sub-threshold level, the specification level, the design margin level, and a level at which some functional failures occur. All radiation test data (including go/no-go) should be accumulated and

documented, and can be used in setting a confidence level in the ability of the system to meet the nuclear specification (Messenger, 1969). All testing should be done in accordance with the accepted standard procedures discussed in ASTM (1990), MIL-STD-750B (1970), MIL-STD-883B (1977), and USASDC (1989).

5.9 Hardening Resources Required

Three major resources required for hardening are funds, experience, and simulation facilities. During the design and development phase, resources are required for design activities relating specifically to nuclear hardness, analysis, and environmental testing required to generate design data and verify hardness. During production, resources are required to support the control, monitoring, and evaluation activities of the hardness-assurance program.

5.9.1 Hardening Costs

The cost of nuclear hardening has consistently been poorly estimated by system developers without appropriate experience. Significant cost elements derive from both design hardening and hardness assurance. The cost of hardening is dependent on many factors, some of which are beyond the control of the system developer/producer. The more important of these factors are the nuclear specification, timing of the hardening effort, the system concept and its complexity, the degree of parts standardization, and nuclear effects experience.

Table 5-7 provides an estimate of the impact of the nuclear specification on hardening costs of a number of satellite systems. As shown in Table 5-7, hardening can be implemented at a reasonable cost for survivable systems such as GPS and FLTSATCOM.

The earlier in the system-development process that the nuclear-environment constraint is recognized and hardening efforts begun, the lower the cost will be to develop a hardened system. Late recognition of a hardening requirement effectively restricts design-hardening techniques to electronic-part replacement. Effective hardening then becomes more difficult and more expensive.

5.9.2 Nuclear Effects Experience

The importance of nuclear effects hardening experience should not be overlooked. One of the objectives of this chapter is to make the reader aware of the basic capabilities required for successful nuclear hardening of electronics systems. Becoming familiar with the references cited in this chapter is helpful in gaining further insight into the system-hardening process.

The Army Research Laboratory and Phillips Laboratory have been very active in the development of guidelines for the hardening of tactical systems with modest radiation requirements (Coppage, 1993; Rose *et al.*, 1981). These guidelines include the elimination of system components of high radiation susceptibility, and the use of MIL-STD-19500 (1974) and MIL-STD-38510 (1974) specifications, which include performance requirements with radiation degradation. The goal of these guidelines is the development of hardened systems with minimum penalty in performance of life-cycle cost.

5.10 Evaluation and Hardening of Existing Equipment

This section presents some basic considerations and guidelines for evaluating and improving the hardness of existing electronic

equipment. Many existing military systems have been designed and deployed without regard to nuclear environment requirements. In addition, newly conceived systems may use previously developed hardware for which nuclear requirements were not considered. In some cases, the threat levels of interest may have increased for previously hardened systems. To properly evaluate such equipment for specific application, the engineer must complete the following steps:

1. Determine that the proposed nuclear hardness criteria are balanced and realistic
2. Evaluate routine operational backup methods in case of circuit failure as an alternative to hardening
3. Perform a rapid hardness assessment of the equipment in its present form and grossly classify the hardness as satisfactory, doubtful, or unsatisfactory for the specified threat environment
4. Determine the available and feasible methods for improvement of the system hardness
5. Evaluate the resultant hardness of the modified systems.

A realistic hardening program for existing equipment must consider cost trade-offs as well as technical trade-offs. An example is the backup

Table 5-7. Estimated Cost Increments Between Operational Military Satellites and Nuclear Hardened Military Satellites (Bui, 1994).

Program	Development Year	Satellite Quantity	Nonrecurring Costs	Recurring Costs	Total Program Costs
DSCS II	1969	16	14%	3%	5%
DCS-III A&B		6	12%	2%	5%
DCS-III A	1976	2	12%	3%	8%
DCS-III B	1980	4	n/a	2%	2%
FLTSATCOM 1-8		8	14%	3%	6%
FLTSATCOM 1-5	1972	5	14%	3%	7%
FLTSAT 6-8	1982	3	n/a	3%	3%
GPS II	1982	28	1%	1%	1%

method used for estimating target range for artillery fire in the event a highly accurate laser range-finder malfunction. A spotting round, or in an extreme case, a gunner's guess, can suffice as a backup method. Relying on a planned backup capability — a reduced capability — may not be a satisfactory alternative to hardening. However, it is an option that should not be ignored, especially when funds for hardening are limited. Figure 5-20 displays this alternative possibility. Figure 5-21 is a block diagram of the subsequent methodology discussed in this section. Other sections of this chapter should be consulted for more specific details and data concerning component response, hardened circuit and systems design techniques, environment descriptions, and testing.

5.10.1 Assessment Considerations

In general, the hardness evaluation of existing equipment begins with an investigation of the history of the equipment. The first step is to determine if hardness was considered during the design phase, followed by identification of the mission-critical elements and their vulnerability to the specified environment. Those mission-critical items whose degraded response can impact the system's ability to perform the mission should then be evaluated in detail to determine the circuits or components that control the response. This identification process can be delayed by a lack of appropriate documentation or by proprietary circuit designs. A criticality analysis should be performed for each environment and operational mode. Only the radiation-sensitive, mission-critical items then need be hardened. Careful attention, however, should be given to other parts of the system to ensure that responses of other system elements do not become dominant after design modifications.

The methods for evaluating the hardness of existing equipment must be sufficient to identify specific equipment weaknesses so that effective hardening programs may be implemented. The first step in a hardness analysis is to determine the system elements in the equipment that must operate satisfactorily in order to complete the mission, and what constitutes satisfactory opera-

tion. Further, the circuits, modules, and assemblies essential for satisfactory mission completion should be separated from those that can be omitted from the vulnerability analysis. In many cases, circuit criticality cannot easily be determined; therefore, all circuits must be considered critical. Determining what constitutes satisfactory operation of these critical circuits may be very difficult to specify. For example, degradation of a power supply may cause increased distortion in an amplifier, but the point at which this increased distortion results in equipment failure is not well defined. Similarly, if neutron damage gradually decreases the range or resolution of a radar, it may be difficult to specify a failure point in the same sense of mission failure. The definition of failure is often somewhat arbitrary and should be reexamined after the system failure modes and probabilities have been determined.

The second step in a hardness evaluation is to eliminate all remaining system elements that are inherently hard to the specified environment by virtue of function or technology. This screen will eliminate such elements as purely mechanical systems, low-power or very-high-frequency circuits, and generally all elements not containing semiconductor devices. The order in which steps one and two are performed can be left to the analyst.

5.10.2 System Element Hardness Classification

To evaluate the hardness of existing system elements to a given nuclear threat, the engineer must set up a categorization scheme to classify the elements evaluated. In its grossest form, this scheme might consist of three categories: hard, not hard, and doubtful; that is, the answer to the question, "Will the element survive the specified threat in a state such that the system mission is uninterrupted?" will be "Yes," "No," or "Maybe." If the evaluation effort is not sufficiently precise, the "Maybe" category could be undesirably broad. In this case, more careful analysis techniques, including detailed hand analysis or more precise modeling of circuits, will have to be used and additional experimental information may have to be obtained.

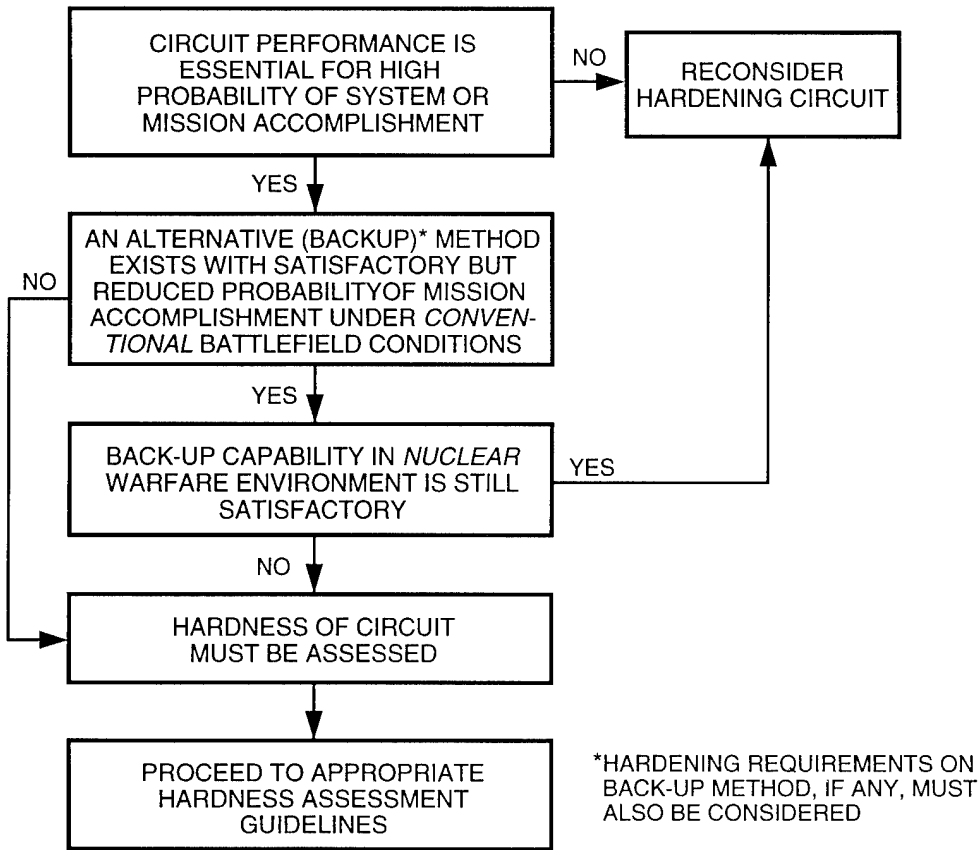


Figure 5-20. Block diagram to determine if circuit survivability is mandatory (Espig, 1985).

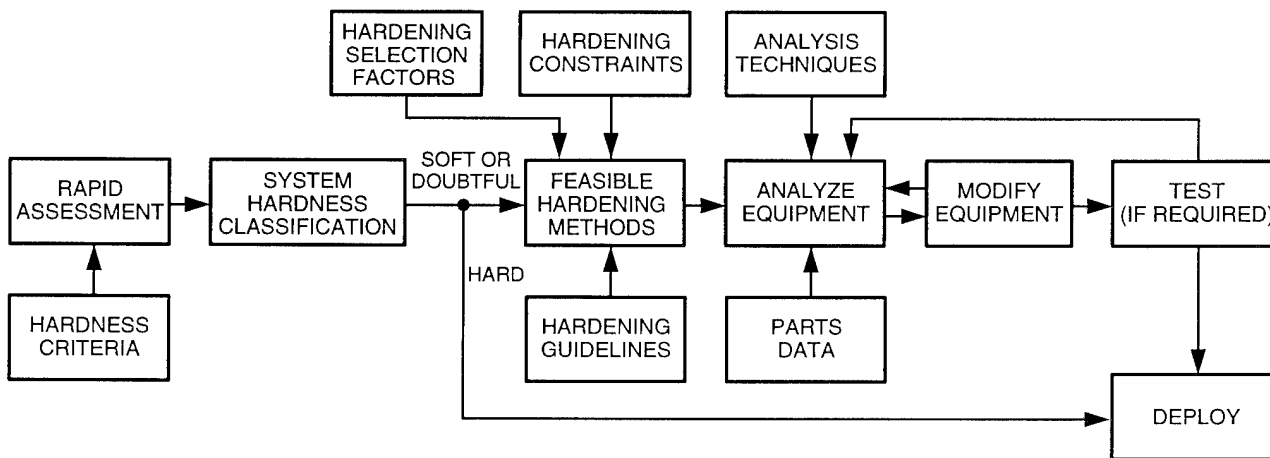


Figure 5-21. Block diagram of methodology for evaluating existing equipment (Espig, 1985).

The evaluation of electrical system elements is a statistical problem because the electronic components from which circuits are made, even under the most carefully controlled manufacturing conditions, have statistical variations in most electrical parameters. Registered transistor types, for example, are only required to meet certain electrical specifications; hence, transistors of any one type may vary considerably with respect to their response to radiation. The usual "worst-case" circuit design must be modified by statistical variations due to radiation damage similar to methods used for reliability derating.

In setting up a hardness classification system based on statistics, some survival probability figure will be specified as a function of mission requirements. The confidence level associated with this survival probability will depend on the precision with which the evaluation is conducted.

Four factors enter into a judgment about the hardness classification of system elements to a given threat environment. These are:

1. Results of analysis
2. Results of environmental testing
3. Experience and understanding
4. Survival probability requirement.

The most technically satisfying classification decision will be based on a combination of these factors.

If the system element is determined to be "not hard" or "doubtful," changes to the element may be desired that will improve its hardness. The principal methods to be considered in the nuclear-radiation hardening of existing electronic and electro-optical system elements are:

1. Parts replacement
2. Parts selection
3. Circumvention/reset
4. Shielding
5. Circuit redesign.

In the general case, the hardening techniques differ for each of the major nuclear effects. Therefore, the impact of one hardening technique on other environmental effects must be evaluated. A

continuous process of reevaluation is called for in which each of the nuclear environments — fast neutrons, prompt ionizing radiation, delayed ionizing radiation, and other environments not discussed here, including x rays, nuclear EMP, airblast, ground shock, and thermal radiation — is considered in evaluating the effectiveness of every proposed hardening technique.

5.10.3 Hardening Constraints

The analysis and hardening methods presented in this chapter generally apply to existing equipment as well as new design; however, the following additional constraints must be considered for existing systems:

1. Certain hardening techniques may not be desirable or practicable based on cost and logistical considerations
2. Hardening implementation trade-offs differ from those applicable to new designs
3. Experimental determination of susceptibility may be the most cost-effective approach.

After the susceptible parts of an existing system are identified, hardening techniques must be selected that optimize the trade-offs between hardening effectiveness, functional compatibility, cost reliability, and maintainability. Some hardening techniques, although quite effective, are not practical for existing equipment. To minimize redesign, and therefore cost, implementation simplicity is extremely important. Field modifications to systems are obviously preferable to those performed at the Depot Maintenance level.

In developing a philosophy for hardening existing equipment, major consideration must be given to logistical impact. Hardening of selected parts of a system instead of the entire system could be attractive to save costs. Full costs of producing and controlling different modified versions of a given subsystem should be carefully explored before such a hardening course is chosen.

5.10.4 Hardening Technique Selection

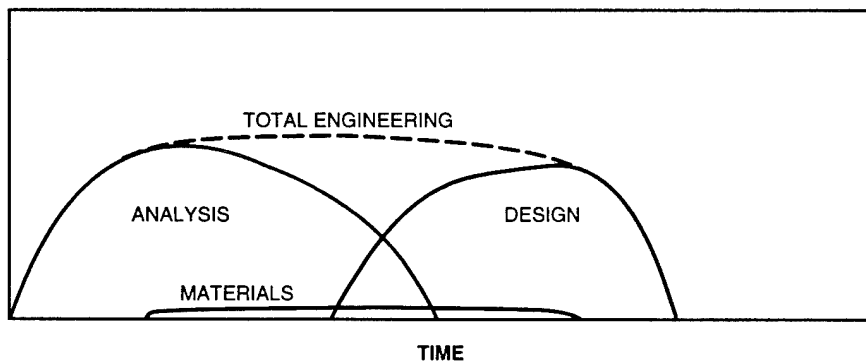
There are four significant factors that must be applied to all candidate hardening techniques for existing systems:

1. *Hardening Effectiveness.* A quantitative measure of the increase in survivability for a given hardening technique.
2. *Functional Compatibility.* The hardening technique selected must not cause changes in the equipment's normal function. This determination is not always straightforward.
3. *Equipment Specification Parameters.* An existing piece of equipment that has been hardened against nuclear radiation must meet all the original performance specifications. These include reliability, operating environments, and maintainability.
4. *Cost.* The total cost associated with a given hardening modification of existing equipment is determined by the anticipated life cycle. The three main phases of the life cycle are engineering, implementation, and operation.

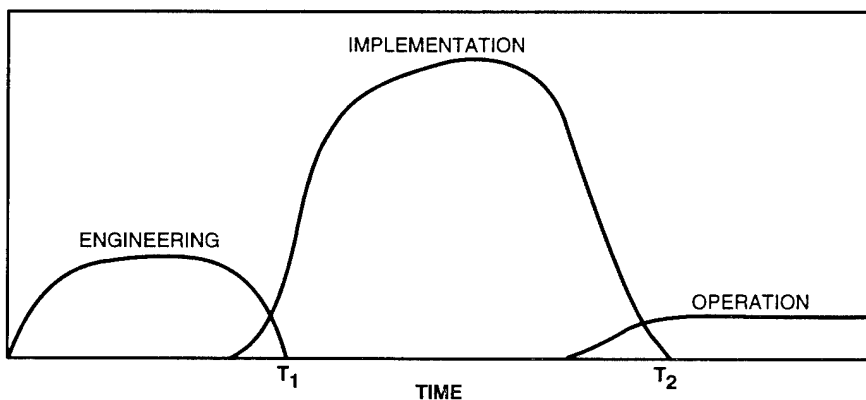
It is clear that all candidate hardening techniques must provide at least the minimum amount of hardening effectiveness. It should also be as-

sumed that none of the other equipment specifications will be waived in order to use a certain hardening technique; therefore, some hardening techniques might have to be rejected. Equipment specifications, combined with component response data, may require component qualification test programs prior to implementing hardening modifications. If several hardening techniques meet or exceed the requirements of items 1 and 2, trade-off studies may be required to maximize system and cost effectiveness of hardened design.

Since the decisions that affect implementation and operation costs are made during the engineering phase, the trade-offs considered during the engineering phase are most important. Figure 5-22(a) shows the composite engineering costs for a hypothetical case. The actual magnitude of these costs will depend on the complexity of the particular equipment. Figure 5-22(b) shows the relative costs of the three major inter-related life-cycle phases. The magnitude of the



(a) Hypothetical Costs of Engineering Phase



(b) Hypothetical Life-Cycle Costs

Figure 5-22. Existing equipment hardening cost factors (Espig, 1985).

implementation costs depends on the number and complexity of the hardening modifications plus the quantities of the equipment.

If preferred hardening techniques are used, the effects on operational costs are minimal and will be associated primarily with documentation revisions and updating of spare parts requirements.

While cost factors do not impact the selection of a specific hardening technique, they will control the method of installation. In the case of several acceptable hardening techniques, installation costs will determine the final selection.

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CHAPTER 6

RADIATION RESPONSE TESTING AND HARDNESS ASSURANCE

6.1 Radiation Response Testing

A well-planned and executed radiation testing program is essential to the development of radiation-hardened microelectronic devices and radiation hardened systems. The test guidelines presented in this handbook are based on guidelines originally developed for use by DNA contractors and more recently updated for use by hardened technology development contractors working under DNA- and USASSDC-sponsored programs. While further changes and improvements in radiation test procedures can be expected in the future, the present guidelines reflect generally accepted procedures for testing microelectronics by government contractors in ionizing radiation dose, ionizing radiation dose rate, neutron and single event effect (SEE) environments. The material on heating-effects testing, combined-effects testing, and prototype versus production testing has been recently developed and was not included in the original DNA/USASSDC radiation test guidelines (USASSDC, 1989).

Ionizing radiation dose (commonly referred to as "total dose") tests are primarily conducted using a gamma (Cobalt 60) or x-ray source as described in Section 6.1.3; the purpose of these tests is to characterize performance degradation as a function of dose and to establish the failure level for the parts being evaluated. Ionizing radiation dose rate (sometimes referred to as "dose rate" or "prompt dose") tests are carried out using a linear accelerator (LINAC) or flash x-ray (FXR) machine to obtain an ionizing radiation pulse of the desired duration and intensity; these tests are designed to determine the upset, latchup and/or survivability (burnout) characteristics of the test device as discussed in Section 6.1.4. The purpose of neutron testing, described in Section 6.1.5, is to characterize parametric performance as a function of neutron fluence and to determine the neutron failure level. SEE testing, discussed

in Section 6.1.6, is designed to evaluate a chip's vulnerability to upset (or, in extreme cases, latchup or burnout) from single particle (alpha, proton, or heavy ion) hits; the experimental data can then be used to develop a predicted upset rate for a specified environmental threat and/or to obtain a SEE figure-of-merit.

The details of a testing program depend on the use of the data. In one case, parts to be tested may be taken on a random sample from the lot which will be used to build a particular system. Allowing for appropriate statistical error, the radiation response characteristics of the sample parts can then be expected to be the same on the rest of the lot.

In another case, the parts to be tested may be taken from one or more lots, that are different from those actually used to build the system. Variability to be expected between the lots tested, and others to be purchased later, must be assured, so that the parts tested represent, as accurately as possible, the radiation response characteristic of future procurement lots.

6.1.1 Test Planning

Test planning, along with the analysis of test results, are two of the most important aspects of radiation testing. The principal planning documentation of a test program consists of the test plans and the test procedures. The test plan provides the overall guidance of the general aspects of the test program, stating the specific goals to be attained. The test procedures specify particular tests and measurements to be accomplished at specific times and should be detailed in the test plan.

The test plan is the controlling document for conducting a test. It defines the scope, objective, test criteria and details the equipment requirements, the measurement points, and the priori-

ties. A comprehensive, carefully developed test plan is essential to conducting a test and should be prepared well in advance of the test to assure proper review and allow for any necessary modifications. Radiation testing engenders compromises between technical adequacy and economic resources. This is particularly true for subsystem or system testing. Thus, each test plan becomes somewhat unique. The decisions that define when testing is "good enough" depend upon the goals of the particular test. It is important to remember that testing is almost always coupled to an analytical effort and, therefore, the test program by itself cannot offer positive proof regarding susceptibility.

Suggested test plan outlines for testing in each of the four main radiation areas — ionizing radiation dose, ionizing radiation dose rate, neutron, and SEE — are included in Section 6.13 through 6.16, respectively.

6.1.2 Test Guidelines

Radiation-effects testing is expensive and should be minimized whenever possible. Thus, existing radiation response data should be used whenever practical. Several data sources are available to the designer — the Electronics Radiation Response Information Center (ERRIC), n.d., and the Jet Propulsion Lab (JPL), RADATA, n.d.

A number of factors must be evaluated when using previously acquired data in lieu of implementing a testing program. These include:

1. Type of test data available for devices of interest,
2. Completeness of the data (parameters, test conditions, device, etc.) (MIL HNDBK 815, 1992),
3. Applicability to the design threat level,
4. Production reproducibility of the device,
5. Reproducibility of radiation effect,
6. Statistical quality of the data.

The existing data should be evaluated in light of the above considerations and the data's suitability to a particular application should then be determined.

When testing is required, an appropriate test program must be established. The facility to be used should be selected based upon its characteristics, availability, cost, etc. A dosimetry program should be established and maintained over the program lifetime, which may extend from the design phase through production (if continued testing is required to assure the nuclear survivability quality of the manufactured equipment.) Other factors to be considered include availability of parts and timely scheduling of tests.

All testing should be performed in accordance with the applicable preferred procedures, Military Standards, the ASTM procedures, etc., as referenced in Sections 6.1.3 through 6.1.6 of this handbook.

6.1.3 Ionizing Radiation Dose Testing

6.1.3.1 Radiation Sources

The standard radiation source for ionizing radiation testing is ^{60}Co . A 10 keV x-ray tester may be used as a secondary source, but correlated with the results of ^{60}Co tests must be performed on test samples representative of the technology being evaluated.

For ^{60}Co testing, dose rates in the range of 50 to 300 rads(Si)/s are generally recommended and should be used for all tests performed under government contract unless directed otherwise.

A 10 keV x-ray tester (e.g. the ARACOR tester) is often used for total ionizing dose tests when evaluation or comparing hardened processes. ARACOR x-ray exposures are usually conducted at an x-ray dose of 100 krad(SiO_2)/min. X-ray dosimetry must be corrected to account for differences (from ^{60}Co) in absorbed dose enhancement and electron-hole recombination (see ASTM 11A49). Since the standard source for total ionizing dose is the ^{60}Co source, an experiment showing part response correlation between ^{60}Co tests and x-ray test irradiations should be performed each time there is a change in the factors that can lead to ^{60}Co /x-ray differences. (Similar dosimetry corrections must be made when other non-standard ionizing radiation sources are employed.)

6.1.3.2 ^{60}Co Dosimetry

The total accumulated ionizing radiation dose delivered to the device under test (DUT) may be obtained from dosimeters exposed with the device or from calculations based on the ^{60}Co source strength, exposure time, and any absorption due to the intervening material.

The method of obtaining the total long term ionization dose should be documented and used for all tests. A change in the method used by government contractors for obtaining the total dose may require government approval. To minimize dosimetry errors which can arise if high Z ($Z > 20$) materials are present either in the DUT or in adjacent components, the DUT should be enclosed in a container whose walls shall consist of Pb with a thickness greater than or equal to 0.06 inch and at least 0.015 inch Al, with lead as the outermost layer and aluminum as the innermost. Such a container is shown in Figure 6-1. If high Z materials are not being used, the shielding container may be unnecessary; however, if it cannot be determined that such materials are absent, the shielding container shall be used as a precaution. The dose-rate and the spectrum in a typical ^{60}Co source may not be uniform through-

out the entire irradiated volume. For best results a specific geometry and location for the irradiations should be selected and then used for all subsequent irradiations. In addition, if Thermoluminescent Dosimeters (TLD) are not going to be used with each irradiation, a calibration should be obtained by exposing a TLD dosimeter inside the graded absorber container in the selected exposure geometry and location.

6.1.3.3 Dose Enhancement Effects (^{60}Co)

As indicated in the preceding section, when high atomic number materials ($Z > 20$) are present in the DUT, serious difficulties can be introduced into ^{60}Co dosimetry measurements as a result of interface enhancement effects. For example, such effects can be introduced by kovar caps, gold flashing inside device container cans, metal silicide interconnectors, etc. If such materials or structures are present, or if the material composition structure cannot be determined, interface enhancement effects should be minimized through the use of the Pb/Al container, as recommended in the previous section.

The work of Lowe, Cappeli, and Burke ("Dosimetry Errors in ^{60}Co Gamma Cells Due to

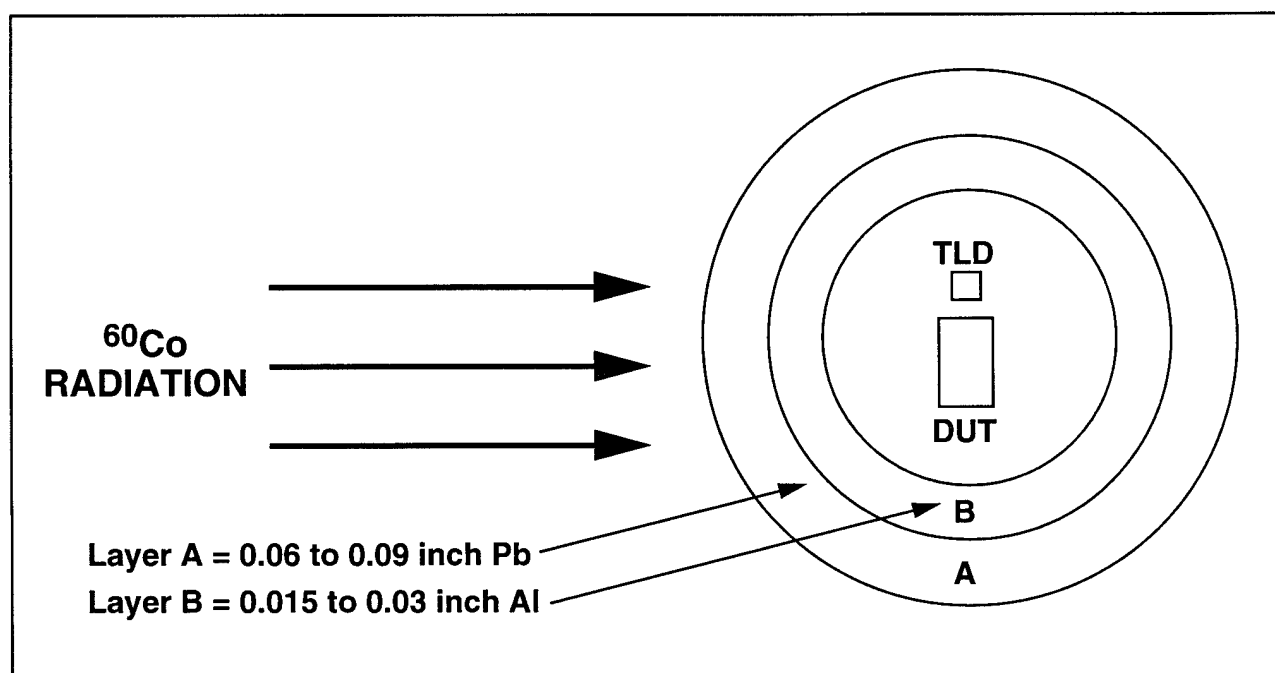


Figure 6-1. Container for Dose-Enhancement Reduction.

Transition Zone Phenomena," *IEEE Trans. Nuc. Science*, NS-29, December 1982) shows that low-atomic-number materials behind or to the side of the device under test can soften the spectrum and result of interface enhancement effects in the test device. Layered absorbers, such as the Pb/Al container in Figure 6-1, surrounding the DUT are therefore sometimes necessary to mitigate dose enhancement effects.

To illustrate the magnitude of error that might result if dose enhancement effects are not taken into account, calculations have been made for two kinds of ^{60}Co sources, several combinations of device compositions, and for irradiations with and without the Pb/Al shielding container. These results are summarized in Table 6-1. The dose enhancement factor given is the number by which the total dose deposited in the oxide can be greater than the value which would be obtained by simply converting a TLD dosimeter reading to rads (SiO_2); thus, for example, if the TLD reading for a given irradiation is equivalent to 10,000 rads (SiO_2) and the dose enhancement factor is 1.5, then the actual dose deposited in the oxide would be 15,000 rads (SiO_2).

The table shows that for water shielded ^{60}Co sources, the shielding container provides a desirable reduction in the dose enhancement factor, but that if high Z materials are present and can-

not be taken into account, the error in the oxide dose can still be as large as 45 percent. For the gamma cell source, the spectrum has a lower intensity at low energies relative to a water-shielded source and the dose enhancement factors are therefore smaller. Again, however, if high Z materials are present, the shielding container provides a desirable reduction in this factor. (In radiation hardened devices, great care is taken to avoid gold.)

6.1.3.4 Test Plan

A thorough test plan should specify devices to be tested, parameters to be measured, circuit response characteristics (based on pretest simulation analysis), functional tests to be performed and provide a description (including a detailed schematic) of the instrumentation system to be employed. In order to allow adequate time for review and feedback, the test plan should be submitted to the reviewing organization(s) at least one month prior to the scheduled test. See Figure 6-2 for a suggested outline of a ionizing radiation dose test plan.

6.1.3.5 Test Procedure

6.1.3.5.1 Sample Size

A sample size that is sufficient to establish the required confidence level in the total ionizing dose hardness of the part should be identified.

Table 6-1. Dose Enhancement Factors.

Device Composition	Water Shielded (30 cm) ^{60}Co Source		Gamma Cell ^{60}Co Source (AECL)	
	0.060" Pb 0.015" Al Container	No Container	0.060" Pb 0.015" Al Container	No Container
0.010" kovar package and 0.5 microns gold	~ 1.45	~ 1.90	~ 1.30	~ 1.50
0.010" kovar package and no gold or other high-Z materials	< 1.10	~ 1.40	~ 1.25	~ 1.25
Ceramic package and no gold or other high-Z materials	< 1.10	< 1.10	< 1.10	< 1.10

However, large sample sizes are typically not practical for modern devices because of the cost. Therefore, sample sizes smaller than may be statistically required are frequently allowed. (Wolicki, Namenson, Carlan, 1992)

A minimum of five samples should be used for each test. All sample devices used in long term ionization testing should meet the electrical specifications for the part. Devices not meeting the specifications should be excluded from the test sample. In general, irradiated test samples should be retained by the testing organization for at least one year or for the duration of the program.

6.1.3.5.2 Exposure Levels

An estimate of the long term ionizing radiation failure threshold should be obtained either by analysis or some other appropriate method. The devices should then be tested to failure starting at an exposure level of approximately 0.1 times the estimated failure threshold, or 0.1 times the appropriate specification level, whichever is lower. Tests should proceed to accumulated levels of 0.2, 0.5, 1.0, 2.0, 5.0, etc., times the initial selected level until failure occurs. The measured failure threshold value is here defined to be the accumulated ionizing radiation up to and including the irradiation during which failure occurs. Two criteria for failure should be established in the test plan; one defining the manufacturer's specified performance limit which, when exceeded, constitutes a failure, and the other the point where the part becomes inoperative. A goal of this procedure should be to test at least five parts and to determine both specification and operational failure thresholds.

6.1.3.5.3 Exposure Conditions

The exposure conditions should be in accordance with Method 1019 of MIL-STD-883 and/or MIL-STD-750. Worst-case bias conditions should be selected for each device tested. Test devices should be held to $25^{\circ} \pm 5^{\circ}\text{C}$. A moderate flow of air from the outside, directed at the devices being irradiated, should suffice to maintain temperature within this range in a gamma cell. The selection of worst-case bias conditions

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Figure 6-2. Recommended Test Plan Outline for Long Term Ionization Tests.

may be subject to approval by the sponsoring organization.

6.1.3.6 Total Ionizing Dose Time Dependent Effects

A number of factors apply to total ionizing radiation measurements that can make interpretation of measurements on different device types and technologies difficult. The most serious factor is that of time-dependent effects which can dramatically influence device response. The controlling time constants depend on the type of oxide present and the processing used, temperature, applied bias, and other parameters as well. Research efforts are presently underway to improve understanding of the basic mechanisms for annealing of ionization effects. However, there does not yet exist any method by which measurements taken at various times after an irradiation can be used to obtain device characteristics at the long exposure times that are of interest in many space applications or at the very short times following a radiation pulse.

6.1.3.7 Electrical Measurements

Electrical measurements should be made before irradiation; in-flux during irradiation for dynamic tests or out-of-flux after each exposure increment for static tests. If post irradiation step stress measurements are used, data demonstrating that the post-irradiation effects are insignificant during the time period of interest should be provided. If step stress measurements are to be made after irradiation, the measurements should occur as soon as possible, and in no case more than one hour after the irradiation is terminated. The interval between the end of an irradiation and the start of electrical measurements should be selected and kept constant (± 10 percent) for all required tests. The effect of post-irradiation annealing must be determined when selecting the test interval. A change from one interval to a different interval should not be made arbitrarily. Whenever possible, tests should be performed both on device functional operation and on selected electrical parameters. When the part complexity and device configuration allow, the buildup of interface state density should be determined and the effect of positive oxide charge and

interface states should be determined from the data.

Ideally, the test equipment employed for total dose testing should be the same as or equivalent to that used for final electrical test on the manufacturing line. However, a portable tester with less capability than a mainframe tester may be used if necessary, particularly during dynamic testing in-flux.

Test circuits should be identical to those specified in the manufacturer's device specification when characterizing device hardness.

For complete characterization testing, all of the electrical parameters specified in the device specification sheet should be evaluated. In those cases where full parametric testing is not practical, an appropriate subset should be chosen for measurement.

A device may fail either because it ceases to perform its required function or because some electrical parameter degrades beyond a specified value. The device manufacturer (or user) should determine what constitutes a device failure and should include definitions for both parametric failure and functional failure. Failure definitions may be subject to approval by the acquiring organization.

6.1.3.8 Data Analysis

The characterization data should be analyzed to define a sensitive subset of electrical specifications to use in routine sample tests. The characterization data should also be analyzed to define post-irradiation parametric limits at the specified dose, as well as sensitivity factors that reflect the rate of change for the degraded parameter as a function of dose.

6.1.3.9 Documentation

Test documentation should be maintained by the testing organization. The information documented should, at a minimum, include:

1. Manufacturer, part type, item and lot identification.
2. Date of test and test operator.

3. Identification of radiation source, including Pb/Al shielding data.
4. Description of test circuit and test configuration.
5. Dosimetry methods, including dose determination method inside Pb/Al container.
6. Input bias and output loading conditions.
7. Total ionizing radiation dose levels, including exposure rate.
8. Ambient temperature.
9. Calibration records and serial numbers of equipment.
10. Record of pre- and post-irradiation electrical characterization data.
11. Time history of the implications and test measurements procedure.

Further, a comparison of pretest predictions and test results should be made and included in the documentation along with recommendations for resolution of any discrepancies.

6.1.3.10 References for Ionizing Total Dose Testing*

Military Standards

MIL-STD-750	Test Methods for Semiconductor Devices.
MIL-STD-883	Test Methods and Procedures for Microcircuits.
Method 1019	Steady-State, Total Dose Irradiation Procedure.

DOD Adopted ASTM Standards

ASTM E666-78	Standard Method for Calculation of Absorbed Dose from Gamma or X-Radiation, 11 June 1982.
ASTM E668-78	Standard Practice for the Application of Thermoluminescence Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices, 11 June 1980.

Other

MIL HNDBK 814	Total Dose and Neutron Hardness Assurance Guideline Document (to be published).
ASTM 11A49	Standard Guide for the Use of an X-Ray Tester (~10 keV Photons) in Radiation Hardness Testing of Microelectronics Devices.
MIL HNDBK 815	Guidelines for Developing Radiation Hardness Assured Device Specifications.

ASTM Dosimetry Standards

ASTM E666-78	Standard Method for Calculation of Absorbed Dose from Gamma or X-Radiation, 11 June 1982.
ASTM E668-78	Standard Practice for the Application of Thermoluminescence Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices, 11 June 1980.

ASTM Electrical Measurement Standards

ASTM F528-81	Standard Method for Measuring Common Emitter D-C Current Gain of Junction Transistors.
ASTM F615-79	Standard Practice for Determining Safe Current Pulse Operating Regions for Metallization on Semiconductor Components.
ASTM F616-80	Standard Method for Measuring MOSFET Drain Leakage Current.
ASTM F617-79	Standard Method for Measuring MOSFET Linear Threshold Voltage.
ASTM F632-79	Standard Method for Measuring Small Signal Common Emitter Current Gain of Transistors at High Frequencies.
ASTM F676-80	Standard Method for Measuring Unsaturated TTL Sink Current.

* The most current revision of documentation shall take precedence over those cited.

6.1.4 Ionizing Radiation Dose Rate Testing

6.1.4.1 Test Facilities

Two basic types of facilities are used for ionizing radiation dose rate testing: linear accelerator (LINAC) and FXR machines. Some of the major characteristics of these simulators are listed in Tables 6-2 and 6-3. The type of facility selected for dose rate testing depends on the type of data needed, the size or physical dimensions of the test samples and the number of test samples.

For cases where equilibrium photocurrent data are needed for computerized circuit analyses, the radiation pulsewidth of the test simulator must be several times greater than the minority carrier lifetime of the test sample. As illustrated in Table 6-3, LINAC simulators can provide a much wider pulsewidth than FXR simulators.

Assuming that the required pulse width can be furnished by either an FXR or LINAC simulator, the dimensions of the test sample may dictate the type of facility needed. LINACs have a fairly narrow beam diameter, and are normally used for testing only electronic piece parts and small circuits. Small FXR simulators, such as the Febetron 705 system, have limited exposure volumes and are also used mainly for electronic piece part and circuit testing.

When tests are performed on a large functional unit or set of units, a large FXR simulator is needed to provide the necessary exposure area. Before selecting a simulator, the dose contours for the machine's output should be checked carefully to ensure that the functional unit receives a fairly uniform dose (< 20 percent variation over the exposure area).

A FXR machine operated in the e-beam mode may be considered for dose-rate survivability tests. Survivability testing has been performed on several FXR machines used in the e-beam mode for several military programs. These tests are sometimes considered sufficient to demonstrate the dose-rate survivability of piece parts used in these programs. The main advantage of e-beam testing is that a small FXR operated in the e-beam mode is relatively inexpensive, and

typically has a higher pulse repetition rate than a large FXR that would be required to produce the equivalent dose rate in the x-ray mode.

The fact that an e-beam (rather than photons) is used to produce the ionizing radiation in piece-parts requires that special precautions be taken in order to perform a valid test. The e-beam can produce a large magnetic field which complicates the instrumentation problem. The beam produces circulating currents, air ionization and unwanted cable currents. Therefore, some special fixturing must be used to assure meaningful results at an e-beam facility. Some necessary precautions are listed below.

1. The e-beam must be confined to the region which is to be irradiated. Support and components must be shielded.
2. The e-beam must be stopped within the test chamber and returned to the FXR to prevent unwanted currents in cables and secondary radiation in the exposure room.
3. All cables and wires must be protected from exposure to prevent extraneous currents from flowing. These currents may be caused by direct deposition of the beam in cables, or by magnetic coupling of the beam into the cable.
4. All cables and entries must be shielded from unwanted EMI caused by the firing of the machine.
5. Measure the response of the test fixture in place, but with no device in the fixture to ensure that the fixture response does not overshadow the device response.

A machine that has been effectively used in performing e-beam dose rate survivability tests is the Army Research Laboratory (ARL) HIFX. The ARL HIFX facility is an IPC FX-45 high energy e-beam generator. It has a maximum charging voltage of 5.0 MV and produces an e-beam with a mean energy of ~3.0 MeV at a 25 ns pulse width. The FX-45 will deliver a dose-rate approaching 10^{14} rads(Si)/s over an

Table 6-2. Linear Accelerator (LINAC) Characteristics.

Facility	Energy Range (MeV)	Maximum Peak Beam Current (amperes)	Electron Dose (rads[Si])	Electron Dose Rate (rads[Si]/s)	X-Ray Dose (rads[Si])	X-Ray Dose Rate (rads[Si]/s)	Neutron Yield (n/pulse)	Maximum Neutron Yield Rate (n/s)	Pulse Width Range (μ s)	Repetition Rate (pulses/s)
IRT Corporation LINAC San Diego, CA	1-25	10	10^5	5×10^{10}	200	10^7			0.02-8	2-180
BOEING LINAC Seattle, WA	5-30	3	6×10^5	10^{12}					0.02-10	1-30
WSMR LINAC White Sands Missile Range, NM	1-48	5		6×10^{11}		5×10^9			0.01-10	10-100
EG&G LINAC Goleta, CA	2-25	30		2×10^{13}		2×10^9			0.00005-4.0	1-360
AFFRI LINAC Bethesda, MD	13-22	0.8		5.7×10^5		70			0.01-6	1-1000
Phillips Lab LINAC Hanscom AFB, MA	5-20	2		1×10^{11}		1×10^8			0.01-4.5	1-180
LANC PHERMEX Los Alamos, NM	30	900	10^7	10^{15}	135				0.033-6.6	
RPI LINAC Troy, NY	5-60	6	10^5	5×10^{11}	210	1.6×10^9		4×10^{13}	0.015-45	1-550

area larger than 1/2 inch diameter. The actual dose-rate can be controlled by placing apertures in the beam to reduce the electron flux.

6.1.4.2 Test Plan

A detailed test plan should specify devices to be tested, parameters to be measured, circuit response characteristics (based on pretest simulation analysis), functional tests to be performed and should describe the instrumentation system to be employed (an instrumentation system's schematic showing grounding and shielding details should be included). The test plan should be prepared and submitted to the reviewing organization at least one month prior to the scheduled test to enable adequate time for a meaningful review. A suggested outline for an ionizing radiation dose rate test plan is provided in Figure 6-3.

6.1.4.3 Upset Test Procedure

6.1.4.3.1 General

This procedure applies to digital devices containing memory and logic elements and to linear devices such as comparators, regulators, operational amplifiers, etc., that are sensitive to the dose-rate environment. The digital devices may be determined (output state completely defined by the input conditions) or non-determined (output defined by internal storage states). Devices of mixed technologies, such as analog-to-digital (A/D) converters, that require a combination of digital and analog techniques are also included. The purpose of upset testing is to characterize the transient response of the DUT and to establish the upset dose-rate threshold (rad(Si)/s) and the upset conditions.

Table 6-3. Flash X-Ray (FXR) Simulator Characteristics.

Facility	Total Beam Energy Per Pulse (joules)	Peak Electron Beam Current (amperes)	Average Particle Electron Energy (MeV)	Peak Electron Energy Fluence/Pulse (cal/cm ²)	Maximum X-Ray Intensity/Pulse (rad[Si])	Maximum X-Ray Dose Rate (rad[Si]/s)	Pulse Width Range (ns)		Pulse Repetition Rate	Pulse Reproducibility (percent)	
							Electron Mode	X-Ray Mode			
Febetron 705 Electron Beam System (Northrop, Kaman Sciences, Lockheed, Palo Alto, EG&G)	400	5,000	1.4	25	7,000		12-30	15	10/s	±10	
Febetron 706 Electron Beam System (Lockheed, EG&G, Research Triangle Institute, Westinghouse)	12	7,000	0.5	8	90	2.6×10 ¹⁰	3	3	20/hour	±10	
Boeing FX-75 Electron Beam Generator (Seattle, WA)	5,000-1500	120,000	3.5	400	4.4×10 ⁴	9×10 ¹¹	29	35	40/min	±5	
Harry Diamond Laboratories FX-45 Electron Beam Generator (Adelphi, MD)	2,500	23,000	2.5	75	3000	7.5×10 ¹⁰	25	20	1/7 min	±10	
Physics International Pulserads (San Leandro, CA)											
1150	30,000	100,000	4.5	200	6,000	10 ¹¹	50	50	15/day		
PITHON II	250,000	2×10 ⁶	1.5	20	10 ⁵	2×10 ¹²	100	20-50	5/day	±20	
DOUBLE EAGLE	250,000	4.5×10 ⁶		1.2	15,000	6×10 ¹¹	15	20-40	3/day	±20	
Maxwell Laboratories (San Diego, CA)											
BLACKJACK 3	21,000	550,000	0.74	200	50,000	10 ¹²	45-85	30-60	6/day	±10	
BLACKJACK 3 Prime	32,000	100,000	1.07	300	75,000	2.5×10 ¹²	45-85	30-60	6/day	±15	
BLACKJACK 5	350,000	3.8×10 ⁶	1.8	40	20,000	2.5×10 ¹¹	50	50			
TRW (Redondo Beach, CA)											
705 Febetron	400	5,000	2.0	140	3,000	10 ¹⁴	25	20	1/min		
Sandia Laboratories (Albuquerque, NM)											
Hermes III			19		4×10 ⁵	3×10 ¹³		20	8/day	±20	
ARL AURORA Facility (Adelphi, MD)	480,000	2.9×10 ⁵	8	400	1.1×10 ⁵	10 ¹²	0.025-0.2	0.05-0.1	8/day	±10	
Honeywell FX-25 Electron Beam Generator (Largo, FL)	1,200	25,000	2.5	20	20,000	5×10 ¹¹	20	20	6/hr	±5	
Raytheon Radiation Facility (Sudbury, MA)											
FX-25	1,200	20,000		120	3,000	1.0×10 ¹²	20	20	1/min	±5	
General Electric, FX-25 (Philadelphia, PA)	1,200	20,000	2.0		3,000	1.25×10 ¹¹	22	22	1/2 min	±2	
Phillips Lab, FXR (Hanscom AFB, MA)	800	200	2.0		3,000	1.5×10 ¹¹	20	20	1/5 min		
Casino (Naval Surface Warfare Center, Silver Spring, MD)	40,000	5.5×10 ⁵	1.2	300	1.8×10 ⁵	2.1×10 ¹²	70	40	4/day	±15	
Gamble II (Naval Research Laboratory, Washington, DC)	70,000		1.0	100	9,000	10 ¹²	40	45-50	5/day	±10	
DNA DECADE (1996) (Arnold AFB, TN)	2,500,000	2.5×10 ⁷				8×10 ⁵	2×10 ¹²	40	40	3/day	±10

6.1.4.3.2 Sample Size

A sample size that is sufficient to establish the required confidence level in the dose-rate upset threshold of the part should be established. However, large sample sizes are typically not practical for modern devices because of sample cost as well as test facility cost. Therefore, smaller than statistically significant sample sizes are usually allowed for dose rate upset tests.

A minimum of five samples is suggested. All devices used in upset testing must meet the electrical specifications for the part. If approved by the sponsoring organization, devices having a finite number of stuck-at faults can be used to support dose rate upset testing. In general, irradiated test samples should be retained by the testing organization for at least one year or for the duration of the program.

6.1.4.3.3 Exposure Conditions

A LINAC used for upset tests should be operated in the e-beam mode and at beam energies greater than 10 MeV to insure sample penetration by the incident electrons. Both short pulse (20 to 50 ns) and long pulse ($\geq 1 \mu\text{s}$) tests are recommended for thorough device characterization. Dynamic tests are sometimes conducted using long pulses in lieu of an extensive series of synchronized short pulses being swept through a timing cycle. However, the synchronized short pulses may provide a more realistic simulation.

FXR machines, which are only capable of short pulse (typically $< 50 \text{ ns}$) operation, may be used for upset testing when acceptable to the sponsoring agency and/or when the desired dose rate cannot be achieved by a LINAC. Additional precautions to mitigate noise and IEMP responses are usually required in the FXR environment.

Irradiations should begin at $< 0.1 \times$ upset threshold and end where upset occurs. The device's output waveforms should be recorded at the upset threshold. Upset thresholds should then be accurately determined for each test cycle with the following measurement precision:

$$\frac{\text{UPSET}}{\text{NO UPSET}} \leq 1.5 \quad (6.1)$$

1. Introduction
2. Test Procedure Description
 - 2.1 Test Articles and Exposure
 - 2.1.1 Test Identification
 - 2.1.2 Predicted Dose Rate Response and Discussion of Analytical Procedure
 - 2.1.3 Test Empty Fixture
 - 2.1.4 Dose Rate Environment Exposure
 - 2.1.5 Radiation Test Configuration
 - 2.2 Test Sequence
 - 2.2.1 Sample Size and Test Assignment
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3. Dose Rate Test Facilities
 - 3.1 Facility Description
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4. Test Equipment
 - 4.1 Test Equipment Identification
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5. Test Parameters and Bias Circuits
 - 5.1 Electrical Test
 - 5.1.1 Parameter Test Circuits
 - 5.1.2 Test Step Procedures
 - 5.2 Radiation Test
 - 5.2.1 Radiation Test Parameters and Setup
 - 5.2.2 Test Step Procedures
6. Data Formatting and Reporting
 - 6.1 Data Formatting and Reporting Procedures
 - 6.2 Test Report Schedule
 - 6.3 Test Report Content
 - 6.4 Test Data
 - 6.5 Test Data Analysis
 - 6.6 Failure Criteria
7. Test Authorization and Inspection
 - 7.1 Test Organization and Responsibility
 - 7.2 Inspection System and Responsibility

Figure 6-3. Ionizing Radiation Dose Rate Test Plan Outline.

This definition is valid for digital devices. For linear devices, an arbitrary failure point is often defined that relates to some system application.

Test devices should not be allowed to accumulate more than 50 percent of the expected total dose failure level during dose-rate upset testing.

Dosimetry during dose rate testing should consist of either TLDs (one per shot) plus the measured pulse waveform or a calibrated photodiode. For large chips, a TLD array should be exposed in front of the DUT on at least one shot to map the exposure level over the chip area. Transient upset tests are typically performed at $25^{\circ} \pm 5^{\circ}\text{C}$ but, if feasible, should be checked over the device's operating temperature range or at least at the intended temperature of operation.

In general, unless otherwise specified, upset tests should be conducted at pulse widths in the 20 to 50 ns range to facilitate comparison with existing upset data. Additionally, it is sometimes of interest to perform upset testing at long ($\geq 1 \mu\text{s}$) pulse widths in order to obtain worst-case response data. Table 6-4 shows the short pulse/long pulse test matrix that we used for VLSI device testing during the DNA/VHSIC and USASSDC technology development programs. At least two internal storage patterns were used to detect upset in "non-determined" devices; dynamic tests were performed on "clocked" devices and memories.

The latest version of MIL-STD-883 (Method 1021) "Dose Rate Threshold for Upset of Digital Microcircuits" should be used as a general reference for this test procedure.

For linear devices the magnitude of the radiation-induced response (volts or amperes) and the recovery time should be recorded. Both static and dynamic bias conditions are appropriate during the tests. Plots of output signal amplitude and recovery time versus dose-rate will provide the most information about the device performance. Mixed technologies such as analog-to-digital converters require a combination of digital and analog techniques.

6.1.4.3.4 Electrical Measurement-Digital Devices

A test matrix for digital circuits is shown in Table 6-4. A minimum of four static (devices are statically biased during irradiation) upset conditions should be used when testing digital devices. Both logic "0" and "1" static upset thresholds should be determined from waveforms recorded on the output pins at both pulse widths using transient digitizers or oscilloscopes. "Non-determined" devices (those with internal storage states) should be initialized before irradiation and checked after irradiation for logic state changes due to internal upset. At least two internal storage patterns (as determined by "worst-case" analysis) should be used on "non-determined" devices to detect internal upsets.

Dynamic upset threshold tests are performed on "clocked" devices and memories either by synchronizing the LINAC pulse with a clock or other timing/command pulse in order to expose the circuit during sensitive operating states, or by asynchronously exposing the device to the long LINAC pulse while clocking the device at 1 MHz (or the manufacturer's recommended rate). As in static upset testing, devices with internal storage states should be checked for internal upset after each pulse.

In general, test devices should be biased at the minimum specified operating voltage during upset testing; however, CMOS/SOI devices should also be checked at the maximum specified operating voltage level since this condition could result in worst-case dose rate upset performance for some CMOS SOI technologies because of parasitic-bipolar-transistor action. The power supply should be monitored to detect latchup. Circuitry can be employed to interrupt the power supply voltage to prevent burnout. Low impedance ($<1 \text{ ohm}$) supply lines with a $100 \mu\text{f}$ stiffening capacitor at the device supply lead to ground, and a low inductance $0.01 \mu\text{f}$ "speed-up" capacitor at the supply pin of the device should be employed during the test. These capacitors should be placed out of the beam and/or shielded as necessary to minimize charge loss. Device outputs should normally be loaded at their maximum

Table 6-4. Transient Upset Test Matrix for Logic Devices.

Test Cycle	Pulsewidth	Specified Output State	Internal Storage States	Initial Dose Rate	End of Test	End-of-Cycle Dose Rate ^a
1 (Static)	20-50 ns	High	Pattern 1 ^b	$0.1 \times UT^c$	UT ^c	$V_{out} < \frac{V_{OH} + V_{OL}^d}{2}$
2 (Static)	20-50 ns	Low	Pattern 2 ^b		UT	$V_{out} > \frac{V_{OH} + V_{OL}}{2}$
3 (Static)	$\geq 1.0 \mu s$	High	Pattern 1 ^b		UT	$V_{out} < \frac{V_{OH} + V_{OL}}{2}$
4 (Static)	$\geq 1.0 \mu s$	Low	Pattern 2 ^b		UT	$V_{out} > \frac{V_{OH} + V_{OL}}{2}$
5 (Dynamic)	$\geq 1.0 \mu s$	X	TBD		UT	Logic Error or Note a
6 (Dynamic) ^e	20-50 ns	X	TBD		UT	Logic Error or Note a

a For nondetermined integrated circuits (devices with internal storage states), the "End-of-Cycle" condition is a functional error in the sorted pattern (bit flip) or a perturbation of the operating cycle.

b As determined by worst-case analysis.

c UT is Upset Threshold.

d Where V_{OH} and V_{OL} are manufacturer's worst-case specifications (min and max, respectively).

e Test Cycle 6 can be used as an alternative to Test Cycle 5.

rated current. A transient upset test flow diagram for digital devices is shown in Figure 6-4, while a block diagram of a typical LINAC test setup is depicted in Figure 6-5.

6.1.4.3.5 Electrical Measurements - Linear Devices

In linear circuit testing, static bias conditions are used to evaluate the response and recovery time of the device with no active inputs. Several bias conditions should be used to perform these tests. Examples of bias conditions include a voltage comparator with the output high and output low; operational amplifiers with grounded inputs and inverting gains of 1, 10, and 100; voltage regulators with the output set to minimum, mid-range, and maximum voltage levels; and A/D converters with V_{in} applied such that the outputs read all zeros, one-third scale, half scale, etc. Static bias for the A/D converter is a d-c input with active clock during the LINAC pulse.

Dynamic bias conditions are used to evaluate the device with realistic input signals. Though the magnitude of the response is sometimes of interest (e.g., comparators) the recover time is the most commonly sought data. Examples of bias conditions include an op-amp with a sine wave input and a comparator with a square wave, both with small and large amplitude signals. A/D converters should be biased with maximum frequency clock rate, and input signals near the Nyquist frequency (the maximum signal rate without exceeding a specified amount of mutual interference). Synchronization with the LINAC pulse may sometimes be required. Interface requirements for these tests should be detailed in the test plan.

The primary measurement tool for linear circuits dose-rate upset tests is the transient digitizer or oscilloscope. The accuracy of the instrumentation should be 0.1 volt or less. If the linear circuit being tested requires greater precision, a

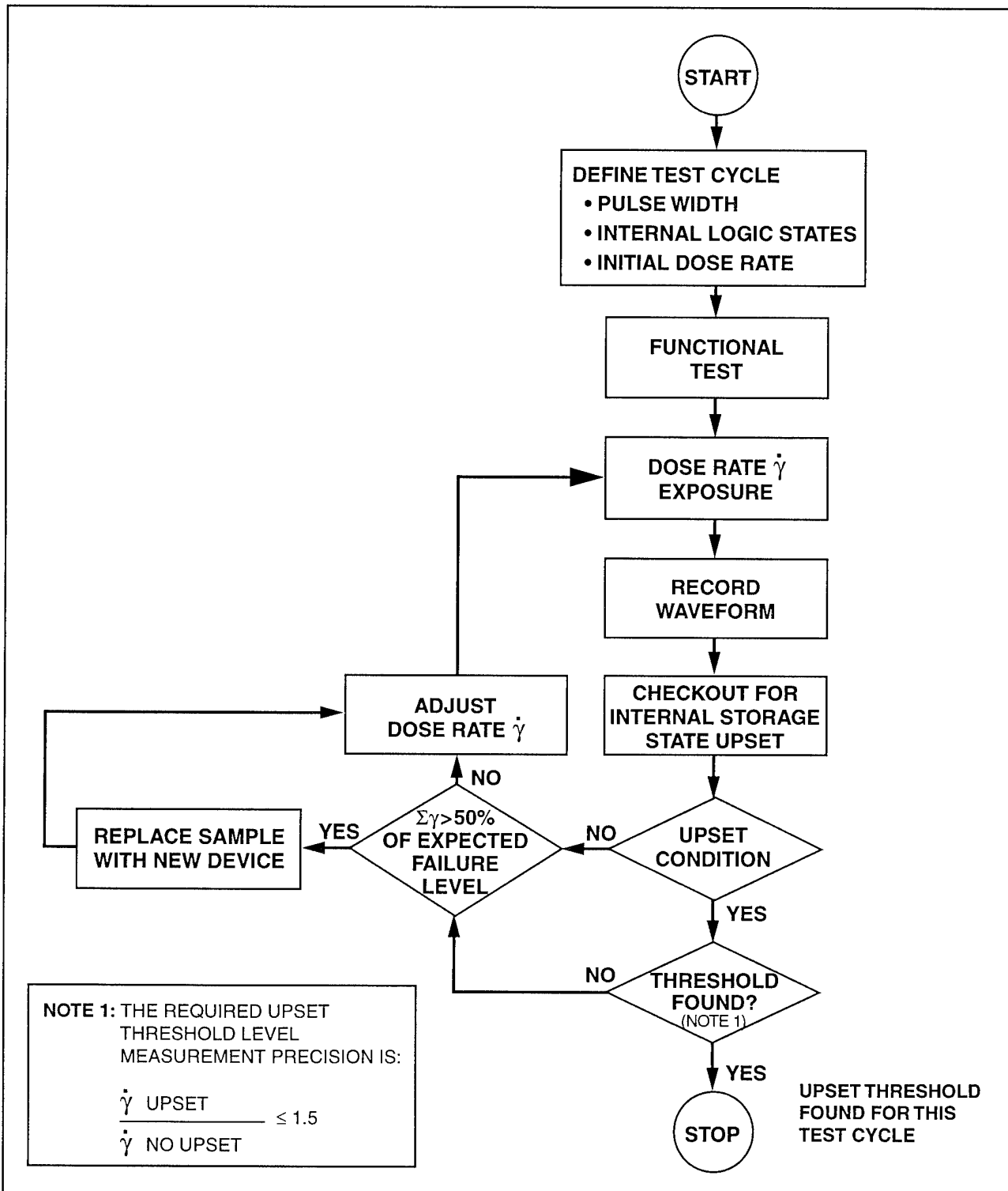


Figure 6-4. Transient Upset Test Flow for Digital Devices.

separate test circuit will be required and should be described in the test procedures.

Unlike digital devices, a simple upset point cannot be described for linear circuits. Often an

arbitrary failure point is defined that may relate to some system application. For these types of circuits, e.g., ADC's, etc., failure criteria must be carefully determined to ensure meaningful and

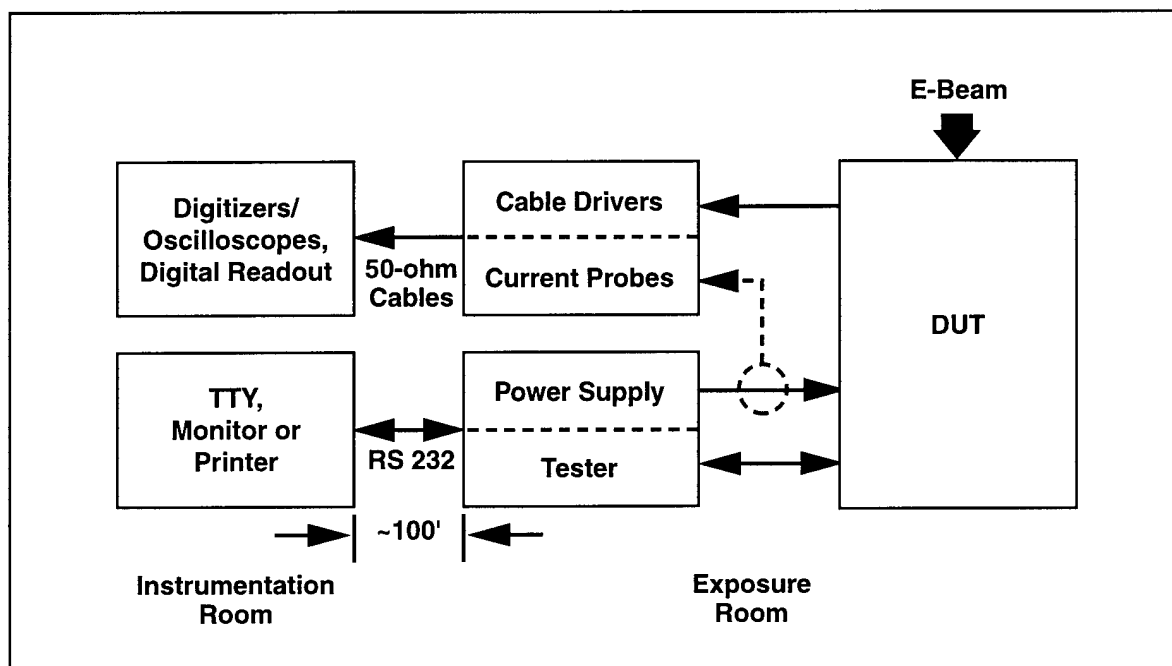


Figure 6-5. Block Diagram of Typical LINAC Test Setup.

reproducible results. However, sufficient data points are required to allow output signal magnitude and recovery time to be plotted versus dose-rate; also, the shape of the response curve should be determined.

Linear devices should probably be tested initially at both minimum and maximum specified operating voltage levels to determine the worst-case bias condition. The supply should be actively monitored to detect latchup. Circuitry may be employed to interrupt the power supply voltage to prevent burnout. Low impedance (<1 ohm) supply lines with a $100\ \mu\text{f}$ stiffening capacitor at the device supply lead to ground, and a low inductance $0.01\ \mu\text{f}$ "speed-up" capacitor at the supply pin of the device should be employed.

Worst-case output loading should be determined by worst case circuit analysis. Alternately, if the worst case analysis is not performed, the loading condition should be determined experimentally by varying the load from no load to maximum rated load.

6.1.4.4 Latchup Test Procedure

6.1.4.4.1 General

This section applies to all devices (pieceparts, test chips, and demonstration circuits) that are subject to latchup testing in a pulsed radiation environment. Detailed test procedures and data requirements to be used in evaluating microelectronic devices that may be susceptible to latchup in the dose-rate environment are reviewed. The latest version of MIL-STD-883 (Method 1020) "Radiation-Induced Latchup Test Procedure" should be used as a general reference for latchup testing.

6.1.4.4.2 Sample Size

Ideally, latchup tests should be performed on large samples of devices and at elevated temperature. Although a 100-percent screen may be used, large sample sizes are often not practical. Therefore, smaller sample sizes may be allowed.

Parts to be used in the latchup test sample may be obtained from associated upset tests, and the same sample may be used provided that the total dose limitation (50 percent of the expected total dose failure level) is not exceeded. As a mini-

imum, five samples should be used for each latchup test. All sample devices should meet the part's electrical specifications.

Since latchup is sometimes a low probability failure mode, a sample of five parts is inadequate for determining the latchup susceptibility of a part unless the test is coupled with a thorough latchup path analysis and the worst-case conditions are identified. In general, irradiated test samples should be retained by the testing organization for at least one year or for the duration of the program.

6.1.4.4.3 Latchup Path Analysis

Engineering analysis should be performed as per "Latchup Analysis of Bipolar Integrated Circuits," and "Latchup Analysis Guideline Document" to determine latchup paths. From this analysis, "worst-case" bias conditions and functional patterns should be determined for latchup testing.

6.1.4.4.4 Exposure Conditions

A LINAC operating in the e-beam mode with a beam energy greater than 10 MeV is recommended for latchup testing, although use of a FXR may be permissible. The LINAC allows testing to be conducted under both short (20 to 50 ns) pulse and long ($\geq 1 \mu\text{s}$) pulse conditions. With most circuits the long pulse provides a more stringent test, but both short and long pulse testing is recommended. In certain CMOS devices, latchup is found to occur over only a limited range or set of ionizing dose rates. This phenomenon is termed latchup window, and the tester must be aware of it.

Irradiations should begin at a dose rate below the expected latchup threshold of the device and end where latchup occurs, or at the maximum exposure rate of the source. The dose-rate should be incremented as required to determine the threshold for latchup within a factor of 1.5.

Since latchup is a temperature-dependent phenomenon, latchup tests should be performed at the devices maximum rated temperature. Otherwise, the temperature of the test should be agreed upon by all parties to the test and approved by the sponsoring organization.

6.1.4.4.5 Electrical Measurements

Devices should be statically biased during irradiation with device outputs loaded at their maximum rated current. A minimum of two "worst-case" bias conditions should be used for each pulse width, as determined by latchup analysis. Internal storage states should be initialized before irradiation, and devices functionally checked after irradiation (before power interruption) to detect a latchup condition. Functional test patterns should be able to detect a minimum of 85 percent of the internal "stuck-at" conditions. This is especially important for devices which manifest a microlatch condition, e.g., partial circuit latchup without appreciable excess current loading.

Devices should be biased at 120 percent of the maximum operating voltage. If this exceeds the absolute maximum voltage that can be applied to the chip, the absolute maximum voltage should be used. Circuitry should be employed to interrupt the power supply voltage to prevent burnout. Use low impedance ($< 1 \text{ ohm}$) supply lines with a 100 μf stiffening capacitor at the device supply lead to ground, and a low inductance 0.01 μf "speed-up" capacitor at the supply pin of the device.

The primary measurement tools for latchup tests are a transient digitizer or an oscilloscope. The device supply current waveform should be monitored and the wave shape during and after the pulse should be recorded. In some cases, particularly when a part population is being screened for latchup, automated systems are used to monitor the current at some preset time after the radiation pulse in order to determine if latchup has occurred. The power supplied to the part should be capable of being interrupted (should latchup occur) in order to prevent damage and burnout of the device. A latchup test flow diagram is shown in Figure 6-6.

6.1.4.4.6 Latchup Condition

A device is considered "latched" if either a distinguishable change in power supply current persists after irradiation, or the device is non-functional (microlatch) after irradiation and returns to normal operation after power interruption.

A device may also experience incipient latchup where the latchup condition may persist only briefly (milliseconds to seconds). The incipient latchup condition may terminate without the removal of power supply voltage, and the device may return to normal operation. The test instrumentation should also be able to detect this kind of latchup condition.

6.1.4.5 Survivability/Burnout Procedure

6.1.4.5.1 General

Test procedures and data requirements associated with high dose-rate survivability/burnout testing of VLSI devices are reviewed in this section. The latest version of "Hardness Assurance Photocurrent Induced Burnout Test Procedure" (Dose Rate Ref. 14) should be used as a general reference for these type of tests.

Photocurrent burnout is the catastrophic failure of a device resulting from a radiation-induced photocurrents. In general, the same electrical test vectors and procedures used for latchup tests are also used for survivability/burnout testing. In contrast to latchup testing, the devices are exposed to high-level irradiations from a FXR unit. No provisions are made to interrupt the power supply voltages.

6.1.4.5.2 Sample Size

A sample size that is sufficient to establish the required confidence level in the survivability of the part should be established. However, large sample sizes are typically not practical. Therefore smaller than statistically significant sample sizes are usually allowed for survivability tests.

A minimum of five samples should be used for each test sequence. Samples which have passed the latchup and upset tests may be used if the total accumulated dose has not exceeded the specified requirement of 50 percent of the estimated failure dose and the devices meet the electrical specifications of the part. In general, irradiated test samples should be retained by the test organization for at least one year or for the duration of the program.

6.1.4.5.3 Exposure Conditions

A FXR machine operated in the x-ray mode is the usual method of performing a survivability test. A source capable of delivering the appropriate dose-rate at the required pulse width (20 to 50 ns) must be used (see Table 6-3 for available sources). In some cases, an FXR operated in the e-beam mode may be a more cost effective method of obtaining a sufficient dose rate for the survivability test; however, additional precautions must be taken for an e-beam test. The beam must be collimated, the test circuit must be shielded from stray radiation and noise, and the beam current must be returned coaxially to the FXR. Charge collection in the part must also be considered as a perturbing factor.

All testing should be performed using approximately a 20 to 50 ns pulsewidth (FWHM). Irradiation typically begins at the required survivability level. If a device exhibits burnout at this level, additional irradiations should be performed at lower dose rates to determine the actual failure level within an order of magnitude. It is recommended that parts be overtested by at least a factor of two to provide some margin of safety in the survivability level.

For parts that do not burn out at the overtest level, it is recommended that a sample of parts be irradiated to burnout or machine maximum level (whichever is less) to determine the actual safety margin. Additional precautions must be taken for an e-beam test. The beam must be collimated, the test circuit must be shielded from stray radiation and noise, and the beam current must be returned coaxially to the FXR. Charge collection in the part must also be considered as a perturbing factor.

Devices should not be allowed to accumulate more than 50 percent of the expected total dose failure level during survivability testing. Survivability testing should be performed at $25^{\circ} \pm 5^{\circ}\text{C}$ unless otherwise specified.

6.1.4.5.4 Electrical Measurements

Test devices should be statically biased with the same conditions used for latchup testing. At least two "worst-case" logic state bias conditions

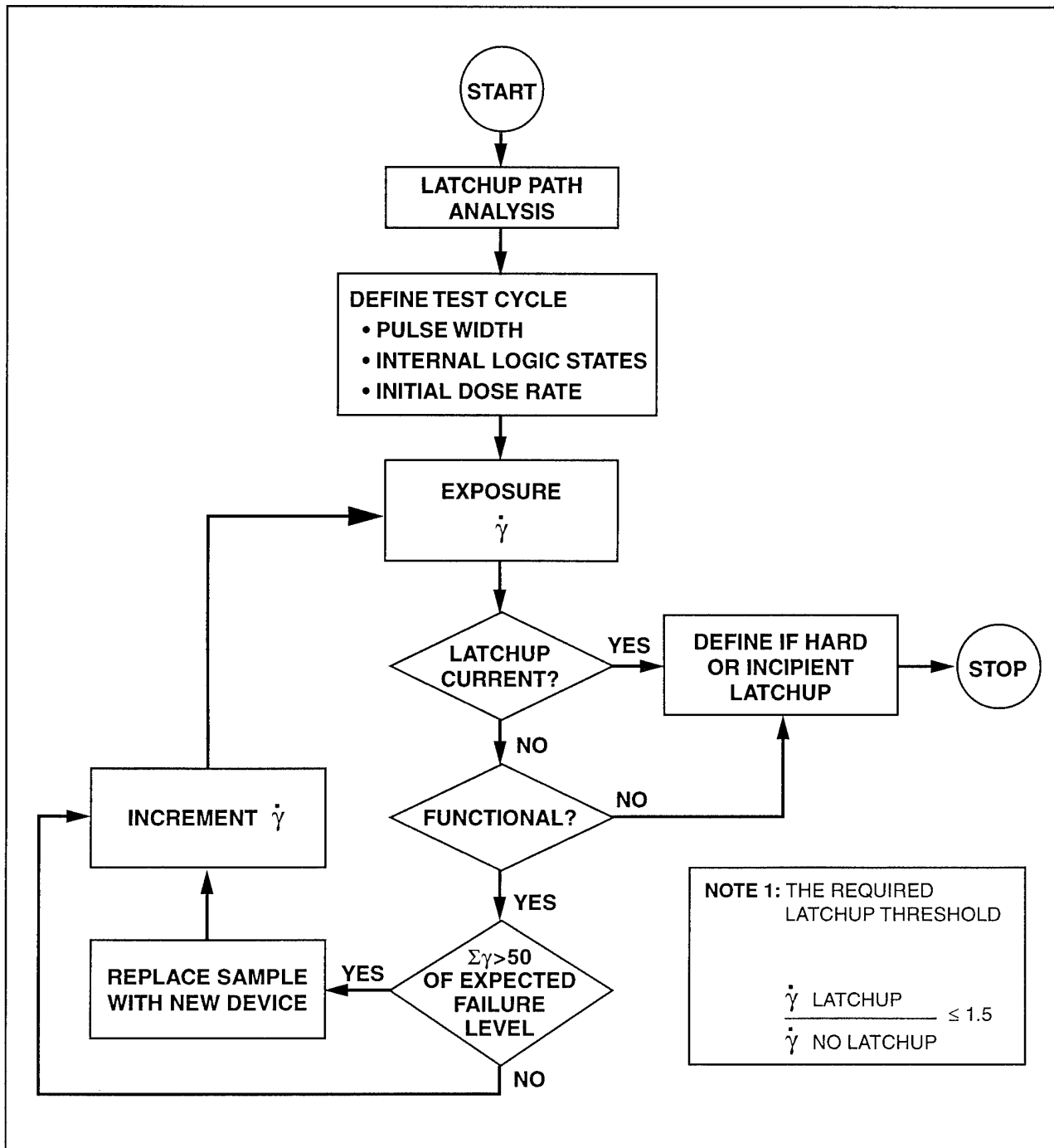


Figure 6-6. Latchup Test Flow.

should be used to establish survivability. Internal storage states should be initialized before irradiation for any burnout conditions. A device is considered to have experienced a burnout failure if it fails functional testing after irradiation. Devices should be biased at their maximum operating voltage. Use low impedance (<math><1.0</math> ohm) supply lines with a 100 μf stiffening capacitor at the de-

vice supply lead to ground, and a low inductance 0.01 μf "speed-up" capacitor at the supply pin of the device. The power supply current waveform should be monitored as an indicator of peak photocurrent and latchup. Device outputs should be loaded at their maximum rated current. A flow diagram for survivability/burnout testing is shown in Figure 6-7.

6.1.4.6 Documentation

Test records should be maintained by the testing organization. The information documented should include, at a minimum, the following:

1. Manufacturer, part type, item and lot identification.
2. Date of test and test operator.
3. Identification of radiation pulse source, pulsewidth and FXR spectrum.
4. Description of scatter plate, if used.
5. Description of test circuit, showing the output pins which were monitored.
6. Description of radiation pulse-shape monitor.
7. Dosimetry methods.
8. Test circuit responses with resistive network in place.
9. Input bias and output loading conditions.
10. The pattern of stored information for non-determined devices.
11. Records of peak photocurrents, quiescent current changes, and burnout responses.
12. Minimum dose-rate resulting in burnout.
13. Maximum dose-rate resulting in no burnout.
14. Record of the irradiation pulse shape monitor.
15. Total dose.
16. Ambient temperature.
17. Calibration records and serial numbers of equipment.

6.1.4.7 References for Dose Rate Testing*

General References

MIL-STD-750 (Method 1015), "Steady-State Primary Photocurrent."

ASTM F675-80, "Standard Method for Measuring Nonequilibrium Transient Photocurrents in P-N Junctions."

"TREE Preferred Procedures," DNA 2028H, Kaman Tempo, 31 January 1982.

"How to Do Radiation Tests," B.C. Passenheim, Ingenuity, Inc., San Diego, CA, 1988.

Transient Upset Testing

MIL-STD-883 (Method 1021), "Dose Rate Upset Testing of Digital Microcircuits"; (Method 1023) Dose Rate Response of Linear Microcircuits.

"Upset Response Testing of MSI Integrated Circuits," Allan Johnston, Boeing Company, 20 October 1981.

"Dose Rate Upset Test Plan for Bipolar LSI RAMS," R.L. Edwards and E.L. Smith, Boeing Company, Document D180-26081-1.

"Dose Rate Hardness Assurance Guidelines," DNA-TR-86-29, J.L. Azarewicz, IRT Corp., 14 November 1985.

ASTM F744-81, "Standard Method for Measurement of Dose Rate Threshold for Upset of Digital Integrated Circuits."

ASTM F773-82, "Standard Method for Measuring Dose Rate Response of Linear Integrated Circuits."

Latchup Testing

MIL-STD-883 (Method 1020), "Dose Rate-Induced Latchup Test Procedure."

"Latchup Analysis of Bipolar Integrated Circuits," J.L. Crowley and T.J. Stultz, Defense Nuclear Agency Document DNA 5928F, March 1982.

"Latchup Analysis Guideline Document," R. Pease, MRC/ABQ-R-719, December 1987.

Burnout Testing

TRW No. 31442-AAW-79-001, "Hardness Assurance Photocurrent Induced Burnout Test Procedure."

* The most current revision of documentation shall take precedence over those cited.

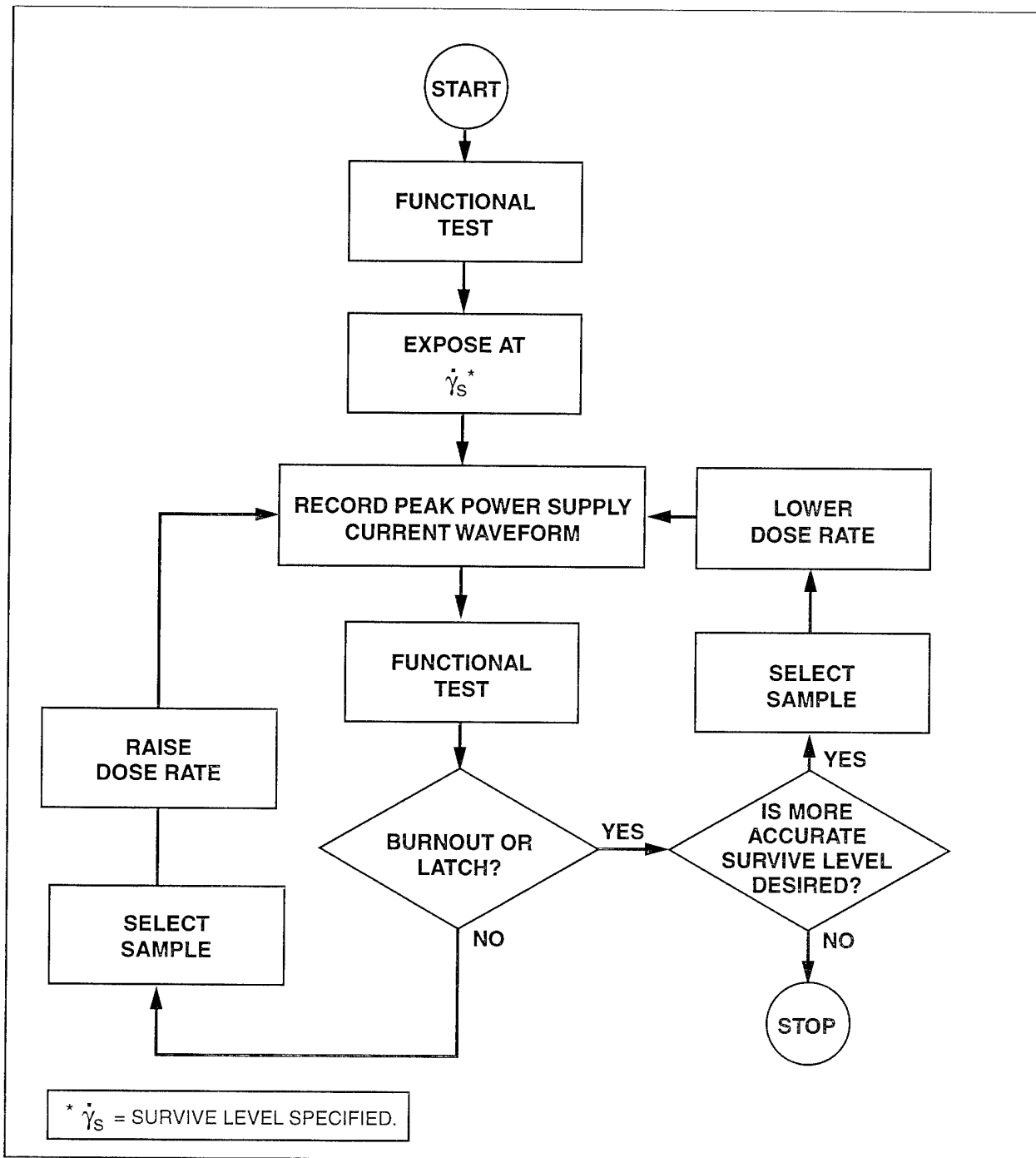


Figure 6-7. Survivability/Burnout Test Flow.

X-Ray Survivability Tests on SBP 9900A Microprocessor and F93471 Memory Devices, D.W. Egelkrou, Boeing Company, 25 April 1980.

Dosimetry/Calibration of Facility

ASTM E668-78, "Standard Practice for the Application of Thermoluminescence Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices."

ASTM F526-77T, "Tentative Method of Dose Measurement for Use in LINAC Pulsed Radiation Effects Test."

ASTM E10.07, "Use of a Faraday Cup in Air for Measuring Dose Rate Delivered by Electron Beams from LINAC."

ASTM R665-78, "Standard Practice for Determining Absorbed Dose Versus Depth in Materials Exposed to the X-Ray Output of Flash X-Ray Machines."

ASTM E666-78, "Standard Method of Calculation of Absorbed Dose from Gamma or X-Radiation."

ASTM E170-81, "Standard Definitions of Terms Relating to Dosimetry."

ASTM E820-81, "Standard Practice for Determining Absolute Absorbed Dose Rates for Electron Beams."

ASTM F448-80, "Standard Method for Measuring Steady-State Primary Photocurrent."

6.1.5 Displacement (Neutron) Damage Testing

6.1.5.1 Radiation Sources

Neutrons generally serve as the standard irradiation particle for displacement damage testing, since displacement damage produced by other particle types can be related to neutron fluence.

Neutron testing should be carried out using either a fast burst reactor (FBR) or a properly calibrated TRIGA reactor. The FBR is generally the preferred source. A number of factors must be considered when selecting a test facility. The first consideration is whether the reactor needs to be capable of pulsed or steady state operation. Pulsed (FBR) reactors can usually be operated in either a pulsed or a steady-state mode. In the pulsed mode, the reactor emits a short, high intensity burst of neutrons and gamma rays. The duration of the burst may vary from about 50 μ s to 65 μ s, depending on the design of the reactor. During steady-state operation, either type of reactor emits a steady flux of neutrons, and is shut down when the desired neutron fluence is

reached. The pulsewidth or range of widths for each reactor and the specified threat neutron pulsewidth should both be determined before a pulsed reactor facility is selected. Where permanent damage to the test sample is to be determined, either type of reactor can be used. The characteristics of some reactors are summarized in Table 6-5. If transient degradation of a part or circuit is to be monitored, the pulsed reactor must be used.

A second factor that should be considered in the selection of the test facility is the size (volume) of the test samples. The dimensions of the exposure area vary between reactors. Small test samples, such as electronic piece parts or small circuits, can be accommodated in all of the reactors. For large-volume assemblies, however, bare critical assemblies or "swimming pool" reactors with dry exposure rooms and remote instrumentation rooms are the only practical facilities to use.

Another factor that may need to be considered are the instrumentation requirements for the test. Some facilities require long instrumentation cables between the exposure room and instrumentation room. This can create some difficulties if high switching rates or RF must be monitored. If test equipment cannot be brought into the exposure room, special cables may have to be constructed.

Other factors that should be considered are the turnaround time for the pulsed reactors and the neutron-to-gamma-radiation ratio for both types of reactors. The turnaround time will influence the time and cost of the test. The neutron-to-gamma ratio may be important if some components in an assembly are sensitive to total dose. The neutron-to-gamma ratio should be kept high if total gamma dose is a problem. In general the neutron/gamma ratio is larger for FBR than for TRIGA reactors. When using a TRIGA reactor, thermal neutron exposure should be minimized by using 1/4 inch Boral shielding, and the neutron-to-gamma ratio should be increased by using 2.3 inches of lead shielding between the neutron source and the sample under test.

Table 6-5. Reactor Simulator Summary.

	PEAK PULSE							Pulse Width Range (μ sec) (FWHM)	Repetition Rate	Pulse Reproducibility	Working Volume (Inches)
	SS Power Level (MW)	Power Level (MW)	Max Fluence (n/cm^2) ($E>10$ keV)	Flux ($n/cm^2/s$) ($E>10$ keV)	Max Gamma Dose (rads(Si)/pulse)	Gamma Rate (rads(Si)/s)	n/ γ Ratio ($n/cm^2/\gamma$ rad)				
Sandia Pulse Reactor (SPR-III) Kirtland AFB, NM 87115	.009	200,000	6×10^{14}	8×10^{18}	1.7×10^5	2.22×10^9	3.6×10^9	76-237	2 burst/hr		7 dia \times 20 high
Sandia Pulse Reactor (SPR-II) Kirtland AFB, NM 87115		89,000	6×10^{15}		1.5×10^5		6.6×10^9	40-150	1 burst/ 2 hr		1.5 dia \times 8 high
Army Pulse Reactor Facility (APRF) Aberdeen Proving Ground MD 21005		6,800 150,000	6×10^{14}		3.9×10^5	2.4×10^9	4.5×10^9	45-1,000	1 burst/ 105 min	$\pm 2\%$	4.2 dia \times 7.8 high
Army Fast Burst Reactor Facility (FBR) White Sands Missile Range NM 88002	.008	65,000	7×10^{13}		2×10^4	1×10^8		50	1 burst/ 75 min	$\pm 5\%$	50 \times 50 \times 20 ft chamber
White Sands Missile Range Steady State Neutron Generator (SNG) NM 88002				7×10^9				1-10 ⁴	10-10 ⁵ (pulses/sec)		
Lawrence Livermore, Super Kukla Prompt Burst Reactor Mercury, NV 89023		160,000 400,000	2×10^{15}	5×10^{18}	2.7×10^5	7×10^8	7.4×10^9	400-2,000	1 burst/ day		18 dia \times 30 high
Sandia Laboratories Annular Core Pulse Reactor (ACPR) Kirtland AFB, NM 87115	2	29,500	3.7×10^{15}		3.3×10^6			65,000	15 bursts/hr	$\pm 5\%$	9 dia \times 45 high
State University of New York At Buffalo Reactor New York, NY 14214	1	2,000		3.7×10^{15}		2×10^7 R/hr		15,000	3 bursts/hr		6 dia \times 100 long
Pennsylvania State University Breazeale Nuclear Reactor (Triga Mark III) University Park, PA 16802	1	2,000	2.2×10^{14}	2.5×10^{13}	2×10^6 R	9.6×10^4		15,000	4 bursts/hr	$\pm 10\%$	6.5 dia \times 36 high
General Atomic Triga Reactor Facility (Triga Mark I)	0.25	1,100	9.7×10^{14}	5.4×10^{16}	3.0×10^6	6.1×10^7	3.6×10^8	16,000	10 bursts/hr	$\pm 15\%$	1.25 dia \times 24 high
(Advanced Triga Prototype) San Diego, CA 92138	1.5	6,700	9.5×10^{14}	1.4×10^{17}	2.8×10^6	4.2×10^8	4×10^8	6,300	10 bursts/hr	$\pm 5\%$	1.25 dia \times 6 high
AFRRRI Reactor Facility (Triga Mark F) Bethesda, MD 20014	1.1	1,800						10,000	1.3 bursts/hr	$\pm 2\%$	
University of Wisconsin Triga Nuclear Reactor Facility Madison, WI 53706	1	12,200						15,000	4 pulses/hr		
U.C. Irvine Dept. of Chemistry Triga Reactor Irvine, CA 92717		1,000						11,000	6 pulses/hr		
U.C. Triga Mark III Berkeley, CA 94720		1,350						12,000	6 bursts/hr		
Kansas State University Triga Mark III Manhattan, KS 66506	0.25	250		10^{16} ($E>0.2eV$)		2.5×10^7			4 bursts/hr	$\pm 3\%$	

6.1.5.2 Dosimetry

Dosimetry should consist of both sulfur pellets and thermoluminescent dosimeters (TLDs). A dosimetry report and analysis for each reactor used, tracing sulfur pellet dosimetry to the computed 1-MeV silicon displacement damage equivalent neutron exposure and TLD dosimetry to rads (Si) exposure, should be prepared.

6.1.5.3 Licensing for Radioactive Materials

The test conductor must either procure a license from the Nuclear Regulatory Commission allowing receipt of low level radioactive materials or must insure that a facility is available with a license to receive such material. The license should be acquired before any irradiations are conducted and must be provided to the test facil-

ity before irradiated parts (above a specified activity level) can be released to the user.

6.1.5.4 Test Plan

The date of the test must be coordinated with the selected facility and appropriate security clearances provided if necessary. A detailed test plan should specify devices to be tested, parameters to be measured, circuit response characteristics (based on required pretest simulation analysis), functional tests to be performed, as well as any special instrumentation requirements. The test plan should be submitted to the sponsoring agency at least one month prior to the scheduled test in order to permit a meaningful review. See Figure 6-8 for a suggested test plan outline.

6.1.5.5 Test Procedure

6.1.5.5.1 Sample Size

A sample size that is sufficient to establish the required confidence in the characterization of neutron response of the part is desirable. Smaller sample sizes may be acceptable when approved by the sponsoring organization. As a minimum, the lot should be sampled according to the specifications within MIL-STD-105, providing only that no fewer than five devices be tested. Irradiated test samples should be retained for at least one year or for the duration of the program.

6.1.5.5.2 Exposure Levels

Analysis should be used to estimate the neutron fluence failure threshold. The devices should then be tested to failure or to the specified neutron level, starting at an exposure level of approximately 0.1 times the estimated failure threshold, or 0.1 times the specified neutron fluence, whichever is lower. Tests should proceed to accumulated levels of 0.2, 0.5, 1.0, 2.0, 5.0, etc., times the selected level, until failure occurs, or the maximum neutron level is attained. Either a step-stress irradiation or parallel irradiations may be performed. The measured failure threshold value is here defined to be neutron fluence accumulated prior to the start of the irradiation during which failure occurred. Two criteria for failure shall be established in the test plan; one defining the manufacturer's specified perfor-

mance limit which, when exceeded, constitutes a failure, and other the point where the part becomes inoperative. As a result of this test, both specifications and operational failure thresholds may be determined.

6.1.5.5.3 Exposure Conditions

Exposure conditions should be in accordance with MIL-STD-883, (Method 1017). Exception to the time before post exposure electrical test may be requested to allow the radioactivity of the parts to decay. Neutron irradiations are typically carried out under ambient temperature conditions. Additionally, unless short term annealing measurements are being made following a neutron pulse, devices are normally exposed in the unpowered condition with leads shorted via conductive foam or other appropriate technique.

6.1.5.6 Electrical Measurements

The test equipment should be specified by the manufacturer, but should be the same or equivalent to that used for the final electrical test on the development or manufacturing line. Test circuits should be identical to those described in the manufacturer's device specification.

For characterization, all of the electrical parameters specified in the device specification sheet should be evaluated. From these, a subset of the most sensitive parameters should be selected for measurement before and after each exposure. This parameter subset should be submitted to the sponsoring agency and approved before commencement of neutron sample tests as required. For bipolar devices this subset should include at least a leakage current, and either a transistor current gain or an unsaturated sink current. For MOS devices, the subset should include at least a leakage current and transconductance.

6.1.5.7 Documentation

Test records should be maintained by the testing contractor. The documentation, at a minimum, should include:

1. Part type, manufacturer, item and lot identification,

- | | | | | | | | | | | | | | | | |
|---|--|-------------|--|-------------|--|-------------|----------------------|----------------|---|----------------|--|--------------|---|--------------|--|
| <ol style="list-style-type: none"> 1. Introduction 2. Test Procedure Description <ol style="list-style-type: none"> 2.1 Test Articles and Exposure <ol style="list-style-type: none"> 2.1.1 Test Identification 2.1.2 Predicted Neutron Response and Analysis Procedures Used 2.1.3 Neutron Environment Exposure 2.1.4 Radiation Test Configuration 2.2 Test Sequence <ol style="list-style-type: none"> 2.2.1 Sample Size and Test Assignment 2.2.2 Test Flow Sequence 2.2.3 Schedule 3. Neutron Test Facilities <ol style="list-style-type: none"> 3.1 Facility Description 3.2 Dosimetry Description 3.3 Test Setup Within Facility 4. Test Equipment <ol style="list-style-type: none"> 4.1 Test Equipment Identification 4.2 Test Equipment Setup 5. Test Parameters and Bias Circuits <ol style="list-style-type: none"> 5.1 Electrical Tests <ol style="list-style-type: none"> 5.1.1 Parameter Test Circuits 5.1.2 Test Step Procedures 5.2 Radiation Test <ol style="list-style-type: none"> 5.2.1 Radiation Test Parameters and Setup 5.2.2 Test Step Procedures 6. Data Formatting and Reporting <ol style="list-style-type: none"> 6.1 Data Formatting and Reporting Procedures 6.2 Test Report Schedule 6.3 Test Report Content 6.4 Test Data 6.5 Test Data Analysis 6.6 Failure Criteria 7. Test Authorization and Inspection | <ol style="list-style-type: none"> 2. Date of test and test operator, 3. Identification of radiation source, 4. Description of test circuit, 5. Dosimetry methods, 6. Input bias and output loading conditions, 7. Exposure levels, <ol style="list-style-type: none"> a. n/cm^2 (1 MeV silicon equiv.), b. Total ionizing dose - rad(Si), 8. Ambient temperature, 9. Calibration records and serial numbers of equipment, 10. Record pre- and post-irradiation electrical characterization data. <p>A comparison of pre-test predictions and test results, including recommendations for resolution of discrepancies, should also be included.</p> <p>6.1.5.8 References for Neutron Testing*</p> <p><u>Military Standards</u></p> <table border="0"> <tr> <td>MIL-STD-105</td> <td>Sampling Procedures and Tables for Inspection by Attributes.</td> </tr> <tr> <td>MIL-STD-883</td> <td>Test Methods and Procedures for Microcircuits.</td> </tr> <tr> <td>Method 1017</td> <td>Neutron Irradiation.</td> </tr> </table> <p><u>Other</u></p> <table border="0"> <tr> <td>MIL HANDBK 814</td> <td>Total Dose and Neutron Hardness Assurance Guideline Document (to be published).</td> </tr> <tr> <td>MIL HANDBK 815</td> <td>Guidelines for Developing Hardness Assurance Service Specifications.</td> </tr> </table> <p><u>Non-Government Documents</u></p> <table border="0"> <tr> <td>ASTM F616-80</td> <td>Standard Method for Measuring MOSFET Drain Leakage Current.</td> </tr> <tr> <td>ASTM F617-79</td> <td>Standard Method for Measuring MOSFET Linear Threshold Voltage.</td> </tr> </table> | MIL-STD-105 | Sampling Procedures and Tables for Inspection by Attributes. | MIL-STD-883 | Test Methods and Procedures for Microcircuits. | Method 1017 | Neutron Irradiation. | MIL HANDBK 814 | Total Dose and Neutron Hardness Assurance Guideline Document (to be published). | MIL HANDBK 815 | Guidelines for Developing Hardness Assurance Service Specifications. | ASTM F616-80 | Standard Method for Measuring MOSFET Drain Leakage Current. | ASTM F617-79 | Standard Method for Measuring MOSFET Linear Threshold Voltage. |
| MIL-STD-105 | Sampling Procedures and Tables for Inspection by Attributes. | | | | | | | | | | | | | | |
| MIL-STD-883 | Test Methods and Procedures for Microcircuits. | | | | | | | | | | | | | | |
| Method 1017 | Neutron Irradiation. | | | | | | | | | | | | | | |
| MIL HANDBK 814 | Total Dose and Neutron Hardness Assurance Guideline Document (to be published). | | | | | | | | | | | | | | |
| MIL HANDBK 815 | Guidelines for Developing Hardness Assurance Service Specifications. | | | | | | | | | | | | | | |
| ASTM F616-80 | Standard Method for Measuring MOSFET Drain Leakage Current. | | | | | | | | | | | | | | |
| ASTM F617-79 | Standard Method for Measuring MOSFET Linear Threshold Voltage. | | | | | | | | | | | | | | |

Figure 6-8. Suggested Neutron Test Plan Outline.

* The most current revision of documentation shall take precedence over those cited.

ASTM F618-79	Standard Method for Measuring MOSFET Saturated Threshold Voltage.
ASTM F632-79	Standard Method for Measuring Small Signal Common Emitter Current Gain of Transistors at High Frequencies.
ASTM F676-80	Standard Method for Measuring Unsaturated TTL Sink Current.
ASTM F528-77T	Standard Method for Common Emitter D-C Current Gain of Junction Transistors.
ASTM E720-80	Standard Guide for Selection of a Set of Neutron-Activation Foils for Determining Neutron Spectra in Radiation Hardness Testing of Electronics.
ASTM E721-80	Standard Method of Determining Neutron Energy Spectra with Neutron-Activation Foils for Radiation Hardness Testing of Electronics.
ASTM E722-80	Standard Practice for Characterization of Neutron Energy Fluence Spectra in Terms of an Equivalent Monoenergetic Neutron Fluence for Radiation Hardness Testing of Electronics.
ASTM F570-40	Transistor Collector-emitter Saturation Voltage.
ASTM F615-79	Determining Safe Current Pulse Levels for Metallization.

6.1.6 SEE Testing

6.1.6.1 Objective

Heavy ion single event upset (SEU) tests are performed to obtain a device's upset cross section as a function of ion species, energy and incident beam angle. Analysis of these results, together with device details, are then used to obtain the critical charge (Q_c) and linear energy transfer (LET) threshold for upset, and finally to obtain the upset rate characterization of the part in the specified space environment. This upset rate is used as an upset figure of merit.

Proton SEU tests are performed to obtain the upset cross section for fixed-energy protons. An

upset rate can then be predicted for a specific earth orbit or proton environment.

Alpha particle SEU tests are performed to obtain the upset cross section for alpha particles. Only the most sensitive technologies are susceptible to alpha upset. SEU measurements should include a test for latchup if the device technology is considered susceptible to burnout, then tests should be conducted to establish conditions under which this can occur.

In addition to upset or SEU characterization, similar tests can be performed to quantify single event latchup (SEL), single event burnout (SEBO) and single event gate rupture (SEGR) in the above environments. Although the material in this section focuses on SEU testing, much of the discussion also applies to SEL, SEBO, and SEGR testing, all of which are included under the broad category of single event effects (SEE) testing.

6.1.6.2 Test Facilities

SEE tests of microelectronic devices are carried out using a source of heavy ions, protons, or alpha particles, depending on the technology being evaluated and the environmental threat. Cyclotrons, synchrotrons or linear/Van de Graaff accelerators are the most commonly used sources of heavy ions and protons. A list of potential proton/heavy ion test facilities showing representative particle types at each is given in Table 6-6. In addition to these large, fixed facilities, Californium-252 is sometimes used as a laboratory source of heavy ions (heavy and light fission fragments); ^{252}Cf testing is limited, however, to a maximum penetration depth of 15 μm , and to LETs of less than 45 $\text{MeV}\cdot\text{cm}^2/\text{mg}$. A detailed discussion of ^{252}Cf sources and the associated test methodology is beyond the scope of this document.

Desirable features of a heavy ion facility and test chamber are summarized below:

- Beam Characteristics,
 - LET range appropriate to the technology being evaluated (in some cases up to 92 $\text{MeV cm}^2/\text{mg}$ at normal incidence)

- Average fluxes from 10 particles/cm²-s to 10⁶ particles/cm²-s
- Uniform flux across approximately one inch diameter to ±10 percent
- Beam characteristics constant during irradiation
- Energy spread of 15 percent or less
- Sufficient energy to penetrate protective overlayers plus at least 15 microns for bulk technologies.
- Test Chamber Capabilities,
 - Able to measure beam uniformity (not necessarily during device measurements)
 - Able to measure flux and fluence of exposure to ±5 percent at center of DUT
 - Able to measure beam spectrum and energy
 - Able to keep DUT centered while being rotated ±90 degrees.
- Facility and Test Chamber Usage,
 - Uniform diffuse beam (use energy degrader or other defocusing method with thin scatterer)
 - Beam monitored in vacuum chamber (Various combinations of scatter and monitor angles make it possible to monitor the beam over a very wide range of intensities)
 - Beam exits into air for part exposure
 - TLD array at and around the DUT position to calibrate, monitor and to check beam uniformity
 - TLD calibration traceable to standards.

A description of a SEU test facility designed for advanced testing is provided in Appendix 6.B.

Desirable features of a proton test facility are as follows:

- Beam Characteristics,
 - Fluxes from 10⁵ to 10¹² proton/cm²-s
 - Beam flux uniform across approximately one inch beam diameter to ±10 percent
 - Beam characteristics constant during irradiation
 - Energy spread of ±5 percent or less
 - Able to check the beam uniformity at running flux level (not necessarily during measurement)
 - Able to measure the flux and fluence to ±10 percent at center of DUT
 - Able to determine the beam spectrum and energy.
- Test chamber capabilities,
 - Strength chosen to give a reasonable upset rate,
 - Calibrated point source, or,
 - Particle flux and energy measured using a solid-state detector and pulse height analyzer,
 - Source mounted in vacuum (1 Torr),
 - Source at a measured distance (0.5 to 2 cm) from the DUT,
 - Collimator between the source and the DUT.

6.1.6.3 Test Plan

The test plan should specify test conditions, include an analysis of estimated device response, describe devices to be tested, parameters to be measured, circuit response characteristics (based on required pretest simulation analysis), functional tests to be performed and should detail (schematically) the instrumentation system to be employed. The test plan should be submitted to the sponsor at least one month prior to the test in

Table 6-6. Representative SEE Test Facilities.

Facility	Location	Normalized Energy Range (MeV/amu)	Representative Particles (Energies)
88-inch Cyclotron	Lawrence Berkeley Laboratory Berkeley, California	1-10	O (32-150 MeV); Kr (165 MeV); Ar (80-160 MeV)
HHIRF Tandem	Oak Ridge National Lab Oak Ridge, Tennessee	3-10	C (120 MeV); Ag (320 MeV); Au (580 MeV)
Brookhaven Tandem VDG	Brookhaven National Lab Upton, New York	10	Cl (107 MeV); Fe (149 MeV); Br (260 MeV); Au (300 MeV)
Penn Tandem VDG	University of Pennsylvania Philadelphia, Pennsylvania	1-2	Cu (70 MeV); Si (40 MeV); O (21.8 MeV); Be (8.9 MeV)
TASCC	AECL, Chalk River Ontario, Canada	3-50	Cu, I, Au (200 MeV, 2 GeV)
Swiss Institute of Nuclear Research	Villigen, Switzerland	590	590 MeV protons
Triumph	University of British Columbia, B.C.	400	400 MeV protons
Indiana Cyclotron	University of Indiana Bloomington, Indiana	200	80 to 200 MeV protons
Proton LINAC	Brookhaven National Lab Upton, New York	200	80 to 200 MeV protons
Harvard Cyclotron	Harvard University Cambridge, Massachusetts	30-160	30 to 160 MeV protons
Davis Cyclotron	University of California Davis, California	2-60	2 to 60 MeV protons

order to permit a meaningful review. A suggested SEE test plan outline is provided in Figure 6-9.

Details appropriate to an SEU test plan include the following:

- Q_C from model studies,
- Relevant device geometry, including dimensions of critical volumes,
- Expected value of LET threshold,
- Estimated collected charge,
- Expected error cross section per cell, number of cells and number of bits,
- Expected latchup threshold and cross section, if any,
- Expected figure of merit in upsets per bit-day,
- Desired particle types, beam currents, energies, angles and anticipated error rates,
- Memory bit patterns and addresses to be used,
- Connector type, pin voltages, timing of input and output signals, bias or operating conditions before, during and after proposed test sequences,
- Discussion of the means to be used for detecting and locating errors,
- Discussion of equipment and setup,
- Data analysis approach,
- GFE or test facility furnished equipment or responsibilities,
- Voltage and temperature ranges of test.

1. Introduction
 - 1.1 Objective
 - 1.2 Scope
2. Test Procedure Description
 - 2.1 Test Articles and Exposure
 - 2.1.1 Test Object/Identification
 - 2.1.2 Predicted Upset Rate vs. LET and Procedure Used
 - 2.1.3 Desired Particle Types, Energies, Fluxes and Associated LETs
 - 2.2 Test Sequence
 - 2.2.1 Sample Size and Test Assignment
 - 2.2.2 Radiation Test Configuration
 - 2.2.3 Test Flow Sequence
 - 2.2.4 Procedure for Detecting and Locating Errors
 - 2.2.5 Schedule
3. Single-Event Test Facilities
 - 3.1 Facility Description
 - 3.2 Source Characterization and Dosimetry
 - 3.3 Test Setup Within Facility
4. Test Equipment
 - 4.1 Test Equipment Identification
 - 4.2 Test Equipment Setup
 - 4.3 Required GFE or Facility Equipment
5. Test Parameters and Bias Circuits
 - 5.1 Electrical Tests
 - 5.1.1 Functional Test Circuits
 - 5.1.2 Functional Test Procedures
 - 5.2 Radiation Test
 - 5.2.1 Radiation Test Parameters
 - 5.2.2 Source and Dosimetry Monitoring Procedures
6. Data Formatting and Reporting
 - 6.1 Data Formatting and Reporting Procedures
 - 6.2 Test Report Content
 - 6.3 Test Data Format
 - 6.4 Test Data Analysis
7. Test Responsibilities
 - 7.1 Test Organization and Responsibility
 - 7.2 Government Responsibilities

6.1.6.4 Estimation of Upset Cross Sections and Upset Rates

6.1.6.4.1 Heavy Ions

The recommended measure for upsets in memory type devices is the number of upsets per particle/cm² per bit. This quantity has units of cm² and represents an area. In a space environment, it will depend upon the projected area for an omnidirectional flux folded together with the path length distribution of the sensitive cell, the number of incident particles able to cause upset, and the number of sensitive cells per bit. In laboratory experiments with heavy ions or alpha particles, the flux will be incident on one surface of the device, and the upset cross section will therefore be a measure of the surface area of the sensitive cells. There is no simple relationship between laboratory upset cross sections and upset cross sections in space.

It is possible to estimate upset cross sections expected in laboratory experiments and, in turn, the necessary flux to obtain a given number of upsets in a given time. Consider the following example:

$$\text{area cell} = 2 \mu\text{m} \times 5 \mu\text{m} = 10 \mu\text{m}^2 = 10^{-7} \text{ cm}^2$$

$$\text{number of cells/bit} = 1$$

$$n_o = \text{number of bits/devices} = 1024$$

$$N = \text{specified number of upsets} = 100$$

$$t = \text{specified time} = 300 \text{ seconds.}$$

Next, assume that heavy ions are being used so that all particles that hit a cell cause an upset. The expected upset cross section then is:

$$\begin{aligned} \sigma_u &= 1 \left(\frac{\text{cells}}{\text{bit}} \right) \times 10^{-7} \left(\frac{\text{cm}^2 - \text{upset}}{\text{cell} - \text{particle}} \right) \\ &= 1 \times 10^{-7} \left(\frac{\text{cm}^2 - \text{upset}}{\text{bit} - \text{particle}} \right) \end{aligned} \quad (6.2)$$

The number of upsets expected is $N \sigma_u F t n_o$. The flux required to produce 100 upsets in 300 seconds therefore is:

Figure 6-9. Suggested SEE Test Plan Outline.

$$\begin{aligned}
 F &= N / \sigma_u t n_o \\
 &= \frac{100 \text{ upsets}}{1 \times 10^{-7} \left(\frac{\text{cm}^2 - \text{upset}}{\text{bit} - \text{particle}} \right)} \\
 &\times \frac{1}{1024 \text{ bits} \times 300 \text{ seconds}} \\
 &= 3.3 \times 10^3 \text{ particles/cm}^2 - \text{s}
 \end{aligned} \tag{6.3}$$

In general, the fluxes required for heavy ion experiments lie in the range from 10^3 to 10^6 particles/cm²-s. At the extreme, the cell area could be much larger, or the device could have many more bits so that the lower limit of flux could be 10^7 particles/cm²-s. Alternatively, observations might be made on a single small bit, and could require 10^7 particles/cm²-s. Because it is difficult to monitor heavy ion beams at this latter intensity, the expected number of upsets should be reduced to 1 in 300 seconds, and the maximum beam to 10^5 particles/cm²-s. Even this rate is very difficult to monitor correctly and requires very careful checking.

6.1.6.4.2 Proton Reactions

The upsets produced by high-energy protons are due to the ionization produced by nuclear reaction products, not the protons themselves. Because only about one proton in a thousand will experience a nuclear reaction in the vicinity of the sensitive volume, the upset cross section for protons is much smaller than the geometric area of the cell. Experimental cross sections for devices that upset for protons generally lie in the range from 10^{-10} to 10^{-14} cm²-upset/proton-bit. Proton upset cross sections are difficult to estimate with any precision.

6.1.6.4.3 Alpha Particles

If alpha particles can upset individual cells, the upset cross section will be approximately the same as estimated for heavy ions; that is, it will correspond to the surface area of the cell. The probability of alpha particle upsets needs to be examined carefully before a major program of alpha upset measurements is started. The upset

probability can be obtained by estimating the charge collection depth, including funneling for the device, calculating the charge collected, and comparing this with the calculated critical charge. For this probability, the upset rate that will be observed with a common source strength can easily be calculated.

For example, for a 1 μ Ci source (alpha sources in home smoke detectors have strengths between about 1.5 and 5.0 μ Ci) the number of alphas emitted per second is:

$$\begin{aligned}
 &(10^{-6} \text{ Ci}) (3.7 \times 10^{10} \text{ disintegrations/s-Ci}) \\
 &= 3.7 \times 10^4 \text{ alphas/s.}
 \end{aligned}$$

At 1 cm from the source, the number of alpha particles per cm² per second is given by:

$$\begin{aligned}
 n &= 3.7 \times 10^4 / 4\pi \\
 &= 2.9 \times 10^3 \text{ alphas per cm}^2 \text{ per second.}
 \end{aligned}$$

Then, for a 1 μ Ci source at 1 cm, and a 1K memory with a cross section of 3×10^{-7} cm² upset/bit particle, the upset rate is:

$$\begin{aligned}
 R &= 3.0 \times 10^{-7} \text{ (upset-cm}^2\text{/bit-particles)} \\
 &\times 1024 \text{ (bits/memory)} \\
 &\times 2.9 \times 10^3 \text{ (particles/cm}^2\text{-s)} \\
 &= 0.9 \text{ upsets per second per 1K memory.}
 \end{aligned}$$

6.1.6.5 Test Procedure

6.1.6.5.1 Sample Size

All test samples should meet the manufacturer's electrical specifications. Samples with known stuck-at faults may be used to support SEU testing if approved by the acquiring organization. At least three devices should be tested in any type of test. A fourth device should be reserved as a spare or for functional testing. Irradiated test samples should be retained by the test organization for a period of at least one year or for the program's duration.

6.1.6.5.2 Dosimetry

Proper dosimetry and beam diagnostics should either be furnished by the facility operator or by the user; dosimetry should be described in the test plan and approved by the sponsor, particularly if user furnished. Alpha particle irradiation

should be performed with either commercially obtained calibrated sources, or with uncalibrated sources for which the user has measured the flux and energy spectrum at the device under test (DUT).

6.1.6.5.3 Radiation Levels

The source intensity should be chosen so that reasonable upset rates are observed (5 to 20 errors per minute). In heavy ion exposures, the ion species, energy and incident beam angle should be varied to examine both the upset threshold and the upset cross section. Care should be taken to insure that the total ionizing dose accumulation in the chip during SEE exposure remains sufficiently small so as not to affect the circuit's SEE sensitivity.

6.1.6.5.4 Test Steps

- Produce and adjust the beam defined in the test plan with respect to:
 - Ion species
 - Energy
 - Flux (particles per cm² per second)
 - Beam uniformity
 - Current uniformity.
- At the same time, with the DUT out of the beam:
 - Check system operation
 - Check noise pickup and signals
 - Check system operation with beam shutter both open and closed
 - Load and check test pattern.
- Close the beam shutter,
- Put the DUT in the beam at proper bias,
- Rotate the DUT to the desired angle,
- Insert the current monitor and adjust its bias,
- Check for the absence of errors,
- Expose the DUT to the beam for a predetermined time and check the observed error rate versus the expected error rate,
- Close the beam shutter.

6.1.6.6 Exposure Conditions

SEE tests are always conducted at least at room temperature. In addition, it is sometimes of interest to determine whether or not SEE sensitivity varies with temperature and, if so, to obtain data at the worst-case temperature extreme. For example, CMOS registers employing cross-coupled polysilicon resistor hardening should always be tested at the high temperature limit (as well as at room temperature) in order to characterize worst-case performance.

6.1.6.7 Electrical Measurements

Electrical measurements for SEU tests are made before, during, and after radiation exposure. Prior to exposure, the test device should be thoroughly tested to insure that it meets all relevant specifications. For a static test a known pattern is written into all registers/memory locations and the device exposed to the desired particle fluence. Following exposure the register/memory contents are compared with the pre-exposure pattern and errors counted. For a dynamic test, the device is exercised in flux and errors are counted in real time.

The test equipment should be capable of testing all memory and register locations for upset and latchup with the memory/register locations in either a "0" or a "1" state. At least two patterns, together with their complements, should be used. For complex devices such as microprocessors, the test engineer should specify which registers are to be tested and detail the approach to be used in verifying the presence of errors.

SEU test apparatus should have the following characteristics:

- Easily transportable to the test site,
- Capable of checking the entire memory of register (both zeros and ones),
- Capable of testing at least the two following patterns in read/write memories:
 - (1) Alternate all 0's and 1's,
 - (2) Alternate checkerboards and checkerboard complement, or can run error detection programs and interrogate

registers for errors in microprocessors or other devices,

- Short device setup and interrogation time, so as to save beam time,
- Capable of dynamic testing, i.e., one which uses a computer repetitively to check the memory, record error locations, correct memory and continue,
- Self-checking, so that errors can be introduced under program control,
- Able to identify latchup, and is protected against excess latchup-induced currents, but does not eliminate latchup. It is desirable that the equipment be able to measure I_H and V_H when latchup occurs,
- Able to be reset after latchup,
- Prints out the type of error and the location of the error in easily readable form,
- Can identify hard device failures (burnout).

For the heavy ion tests, the user should provide a working delidded device in a sample holder with the length of cable to be used in the actual setup. The device should be mounted so that it can be exposed at angles from 0 to 70 degrees.

For proton tests the user should provide devices (not delidded) in a sample holder, working with the length of cable to be used in the actual test.

In general, test devices should be biased at the minimum specified operating voltage level in order to obtain worst-case single event data. However, some CMOS/SOI technologies are more sensitive to single event effects at their maximum operating voltage because of increased charge collection resulting from parasitic bipolar action.

6.1.6.8 Data Analysis

The empirical data should be analyzed to define the critical LET and the saturated cross-section. These values should then be used to estimate the event rate for an appropriate use environment. A detailed discussion of the cosmic ray upset rate calculation is provided in Appendix 6.C.

6.1.6.9 Documentation

Appropriate test records should be maintained by the test organization. The documentation should include, at a minimum, the following:

1. Part type, item and lot identification,
2. Irradiating particle types, energies, fluxes,
3. Device bias or operating conditions,
4. Angle of incidence during irradiation,
5. Monitor counts and other dosimetry information,
6. Number of errors, latchups or burnouts,
7. Printout giving error locations,
8. Any items differing from the test plan,
9. Signature of the responsible test engineer.

6.1.6.10 References for SEU Testing

General References

"Radiation-Induced Single-Event Phenomena Produced by National, Directed Energy Weapon, and Test Environments," J.S. Browning, Sandia National Laboratories, SAND84-2649, July 1985.

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E.L. Petersen, P. Shapiro, J.H. Adams, Jr., and E.A. Burke, *IEEE Trans. Nucl. Sci.*, NS-29, 2055 (1982).

Alpha Particles

T. Toyabe, *et. al.*, *IEEE Trans. Elec. Dev.*, ED*-29 732, (1982).

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P. Shapiro, A.B. Campbell, E.L. Petersen, and L.T. Myers, *IEEE Trans. Nucl. Sci.*, NS-29, 2072 (1982).

Californium

R. Velazco, *et. al.*, *IEEE Trans. Nucl. Sci.*, NS-36, Dec. 1989.

Standards

ASTM F1192-88 — Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

MIL-STD-45662A — Calibration System Requirements.

Refer to Appendix 6.B for Single Event Upset Test Facility information.

Refer to Appendix 6.C for Cosmic Ray Upset Rate Calculator information.

6.2 Radiation Dosimetry

In testing the radiation hardness of devices it is necessary either to measure the radiation intensity incident on a DUT or, more commonly, to estimate the radiation dose deposited in some critical region within the DUT.

6.2.1 Dosimetry for Ionizing Radiation Dose (Total Dose) Effects

When ionizing radiation is deposited in the materials of a device, electrons and holes are produced. It is these charged particles which, either directly or indirectly, degrade the operation of a device. The numbers of electrons and holes which are produced are directly proportional to the amount of energy deposited, or dose. Some common types of radiation effects (for example threshold voltage shift, leakage increase, or mobility decrease) depend in a systematic fashion on the total dose deposited. This dose may be deposited over short times (microseconds) or long times (years). Such radiation effects are called ionizing radiation dose effects or total dose effects.

In the SI unit system, the unit for absorbed dose is the Gray (Gy), where 1 Gray corresponds

to an absorbed energy density of 1 J/kg. An older unit, still in common use is the rad, where 1 rad was defined as an absorbed energy density of 100 erg/g. Conversion between these two units is given by 1 krad = 10 Gy.

6.2.2 Radiation Sources

In order to test radiation hardness it is necessary to deposit a given dose within the DUT. Most commonly it is convenient to use laboratory source to simulate the radiation field to which the DUT is expect to be exposed. Ideally, the laboratory source should reproduce the dose, dose rate, particle type (photon, electron, etc.), and energy spectrum of the radiation field anticipated in the intended application. Since this is generally impossible, it is necessary to make allowance for the mismatch between the laboratory radiation field and the radiation field expected for the anticipated application. The three most common laboratory radiation sources which are used for ionizing radiation effects testing are:

1. X-Ray Tester — The x-ray tester uses an x-ray tube to produce x-ray photons with energies lying between approximately 1 keV and 50 keV. The majority of the x-ray photons lie in the energy band between 8 keV and 15 keV. These x-ray photons are insufficiently penetrating to be used on packaged and lidded devices. Thus the x-ray tester is primarily used on unlidded devices or, more commonly, on devices still on a wafer. These photons can be collimated using an aperture, so it is possible to irradiate only a single device on a wafer, leaving the remaining devices on the wafer unharmed. The x-ray tester is commonly used with dose rates of about 10 Gy/s (1,000 rad/s) and has been used in the range from 0.3 to 180 Gy/s (30 to 18,000 rad/s).

2. ^{60}Co Source — ^{60}Co sources use the decay radioactive ^{60}Co to produce gamma rays whose primary energy is just above 1 MeV. In addition to these high energy photons, ^{60}Co sources typically produce lower energy photons with energies between 100 keV and 1 MeV. These lower energy photons are produced by scattering of the primary photons from the material of the source itself and also from materials which are present as shielding and support structures. ^{60}Co sources

have a substantial history in radiation hardness testing and are required by some testing and purchasing documents. ^{60}Co testing is usually performed on packaged devices. The radiation which is sufficiently penetrating that devices do not need to be delidded. Further, the radiation is sufficiently penetrating to use for tests of larger assemblies such as boards and subsystems. On the other hand, it is not possible to collimate ^{60}Co so as to irradiate only a single device on a wafer. ^{60}Co sources are commonly used in the dose rate range of 0.5 to 3 Gy/s (50 to 300 rad/s). They have been used with dose rates as low as 1×10^{-4} Gy/s (0.01 rad/s) in order to approach dose rates expected for satellite electronics applications.

3. Electron LINAC — LINACs produce a fairly monoenergetic beam of high energy electrons. Electrons with energies between about 5 and 50 MeV have been used for radiation testing. The LINAC is a pulsed source, a single pulse lasting of the order of 1 μs . An individual pulse may deposit in the order of 500 Gy (50 krad).

6.2.3 Dosimeters

The intensity of the radiation field incident on the DUT is inferred by measuring the energy deposited in a dosimeter. There are several types of dosimeter in use for radiation hardness testing. For example:

1. Thermoluminescent Dosimeter (TLD) — The material of the TLD, when heated, emits light. The amount of light is proportional to the dose absorbed in the TLD material.

2. Calorimeter — In a calorimeter, the heat rise in a material of known heat capacity is a measure of the absorbed dose.

3. PIN detector — In this detector the output current is proportional to the rate of deposition of dose in the sensitive region of the detector.

Once the dose in the dosimeter has been determined, it is usually necessary to infer the dose which *would* have been produced in a critical region within the DUT. This conversion is performed using tabulated differences in the energy absorption properties of the material of the TLD and the material of the DUT. The dose in the

DUT calculated in this way may lead to erroneous conclusions because of *dose enhancement* or *time dependent effects*.

6.2.4 Dose Enhancement

A key concept in radiation dosimetry is that of equilibrium dose. In order to understand equilibrium dose, it is necessary to realize that the energy lost by a photon (or electron) when passing through a material is usually not immediately deposited in the form of stable constructs such as lattice defects or trapped charge. In fact, most often the lost energy is first passed to secondary particles, usually electrons. These electrons may have sufficient energy so that they may travel some distance in the material before they, in turn, deposit their energy. Consider some small volume of interest within the DUT. If the number of secondary particles (of each energy) entering and leaving this volume are the same, then this volume is said to be in equilibrium. The dose in a volume which is in equilibrium with respect to secondary particles is an *equilibrium dose*.

Unfortunately, the critical dimensions within microelectronic devices are often small in comparison with the ranges of secondary electrons. As a result, non-equilibrium behavior is frequently observed. Under non-equilibrium conditions, energy originally deposited in one region of a device may be carried by the secondary electrons to a second region and deposited there. Thus the dose in this second region is enhanced. This process is called *dose enhancement*. In order to obtain reliable dosimetry, dose enhancement must be either minimized (by appropriate choice of experimental conditions) or estimated (usually by use of transport codes).

An example of a dose enhancement problem and its treatment can be found in the radiation hardness testing of devices using ^{60}Co irradiation. It has been mentioned that ^{60}Co source spectra commonly contain a component of low energy photons. These low energy photons can cause dose enhancement effects when irradiating some types of devices. A case where dose enhancement is expected is that of irradiating a device mounted in a package which has a gold-flashed kovar cap. In this case, energy originally

deposited in the gold may enhance the dose in critical regions within the device. This problem can be minimized by using filtration to remove the low energy components of the source spectrum.

6.2.5 Time Dependent Effects (TDE)

A second complication in the interpretation of radiation hardness testing results from the fact that the radiation-induced defects in the device grow in and anneal out at widely different rates. As a result, the effect on a device of a one hour radiation exposure may not be the same as that for a three year exposure at a much lower dose rate to the same dose. Proper allowance must be made for TDE when conducting radiation hardness testing.

A common testing problem is that of properly allowing for TDE when assessing the hardness of devices to be used in a space mission. It is usually not practical to conduct radiation hardness tests at the actual low dose rates characteristic of space missions because of the long times required. The usual approach is to conduct laboratory radiation hardness tests which are conservative. That is, to use tests which can be guaranteed to be slightly more severe than the actual application will be. The accelerated aging test in MILSTD 883D, Test Method 1019.4, is an example of such a test.

In order to understand TDE for space mission applications it is necessary to distinguish between the behavior of radiation-induced trapped holes and radiation-induced interface states. Typically, for the low dose rates characteristic of space applications, a substantial degree of annealing of trapped holes may occur. In contrast, a smaller degree of hole annealing is expected when the irradiation is simulated using the much higher dose rates characteristic of laboratory testing sources. Two important cases can be distinguished. First, if holes are the dominant radiation-induced defect, then the problem is that the laboratory test is over conservative. That is, the laboratory test will cause more trapped holes than would a space dose rate exposure to the same dose. A second, and much more serious, case is if both interface states and holes are

present in significant numbers. In this case the laboratory test may lead to effects dominated by trapped holes while a comparable space dose rate irradiation would result (due to trapped-hole annealing) in effects dominated by interface states. That is, the laboratory test may be testing for the wrong failure mechanism.

A test technique to aid in the simulation of space-dose-rate exposures is the use of accelerated annealing. This technique uses elevated temperature annealing (for example, 100°C for one week) to increase the rate of trapped hole annealing. As a result, such an anneal will tend to produce a situation where the device failures, if any, are dominated by the interface. Such a technique will provide a test which is conservative for devices which show both trapped hole and interface state effects.

6.2.6 Ionizing Radiation Dose Testing Standards

The following is a partial list of dosimetry standards applicable to ionizing radiation dose effects testing.

- MIL-STD-883, Method 1019.4, "Ionizing Radiation Effects (Total Dose) Procedure."
- ASTM E 666 "Standard Method for Calculation of Absorbed Dose from Gamma or X Radiation."
- ASTM E 669 "Standard Practice for the Application of Thermoluminescence Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices."
- ASTM E 1249 "Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices."
- ASTM E 1250 "Standard Method for Application of Ionization Chambers to Assess the Low Energy Gamma Component of Cobalt 60 Irradiators Used in Radiation Hardness Testing of Silicon Electronic Devices."

- ASTM E 1275 "Standard Practice for Use of a Radiochromic Film Dosimetry System."

6.2.7 Dosimetry for Dose-Rate Effects

Some common types of radiation effects (for example device upset or burnout) depend in a systematic fashion on the rate at which energy is deposited in critical regions within a device. Such radiation effects are called dose-rate effects. For dose-rate effects, it is the radiation induced currents which are important. These currents may cause a change in a memory state, or they may cause latchup, or burnout.

6.2.8 Radiation Sources

Typical laboratory source for dose-rate testing are:

1. Electron LINACs — LINACs are commonly used for dose-rate testing. Their advantages are a) the beam can penetrate a DUT with little attenuation, b) the beam is quite monoenergetic, thus simplifying dosimetry, c) the time-dependence of the pulse is relatively well known and reproducible.
2. Flash (FXR) machines — FXR machines are commonly used because they can achieve high dose rates obtained from photons. On the other hand, the interpretation of FXR effects is complicated by a) the spectrum and dose-rate of a FXR pulse has a rather complex time history, and b) the spectrum and dose-rate history may be quite variable from one pulse to next.

6.2.9 Dosimeters

Dosimetry for dose-rate effects is closely related to dosimetry for ionizing radiation effects. For continuous sources (for example, ^{60}Co sources and x-ray testers) the dose rate may be obtained simply by dividing the measured dose by the irradiation time. For LINACs, the pulse length is generally known. Thus a mean dose-rate can be obtained simply by dividing the measured dose by the pulse length. For some radiation sources (for example FXR sources) the

dose rate rises and then falls in a complex way as a function of time. If the time dependence of the dose rate is needed, it may be obtained using a dosimeter such as a PIN detector, while the total dose is obtained using a TLD or a calorimeter.

6.2.10 Neutron Dosimetry

In any radiation testing of electronic devices, the purpose of the dosimetry measurement is to obtain a numerical quantity for the energy deposited by the radiation, which is related to the magnitude of the effect produced in the device. If such a quantity is obtained, then irradiations at one radiation facility can be compared with those made at a different facility and a standard measurement becomes possible.

The principal effect of a neutron irradiation on an electronic device is to produce displacement damage which degrades the operating characteristics of the device. For neutron irradiations, the dosimetry standard which has been developed expresses neutron fluences at different reactor facilities in terms of displacement damage equivalent fluences of 1 MeV neutrons. The discussions which follow explain the meaning of a displacement damage equivalent 1 MeV neutron fluence and discuss how dosimetry measurements are performed at reactors to obtain this quantity.

In silicon, the amount of displacement damage produced, per gram of silicon, by a neutron irradiation, is given by:

$$\text{DAMAGE}(\text{Si}) = N(\text{Si}) \int_0^{\infty} D(E, \text{Si}) \phi(E) dE \quad (6.4)$$

where

DAMAGE(Si) is the amount of energy deposited into atomic displacements in silicon by an integrated fluence of neutrons, per gram of silicon,

$N(\text{Si})$ is the number of silicon atoms per gram = 2.14×10^{22} ,

$D(E, \text{Si})$ is a product, per incident neutron of energy E , of an energy deposited into atomic displacements and a cross section per silicon atom, and

$\phi(E)$ is a fluence (neutrons per cm^2) of neutrons with energies between E and $E + dE$.

$D(E, \text{Si})$ is called the neutron displacement kerma function for silicon. A table of value for this function may be found in ASTM standard E722. If $D(E, \text{Si})$ has units of $\text{MeV}\cdot\text{cm}^2$, and E has units of MeV , then at neutron energy E , the product,

$N(\text{Si})D(E, \text{Si})\phi(E)$ gives the amount of energy, in MeV , going into atomic displacements, per gram of silicon. The integral over the neutron energy spectrum then gives the integrated energy going into atomic displacements, namely the $\text{DAMAGE}(\text{Si})$.

The threshold energy for producing a displaced atom in silicon is commonly taken to be 25 eV or $2.5 \times 10^{-5} \text{ MeV}$. Dividing $\text{DAMAGE}(\text{Si})$ by 2.5×10^{-5} then gives the number of displaced silicon atoms per gram.

Now if, at each separate reactor facility, the displacement damage produced by the integrated fluence given by Equation 6.4, could be related to the damage produced by a fluence of 1 MeV neutrons, then comparisons of the damage produced by neutron irradiations made at different reactor facilities would become possible. In this regard, recent experiments and calculations (Burke 1986, Summers 1986, Summers 1987) have shown that the number of displaced atoms depends only on the total amount of energy going into atomic displacements and does not depend on the energy spectrum of the neutrons producing the damage. In fact even such different types of particles as protons and alpha particles exhibit this same characteristic (Summers, 1987). As a result of this fact, it is possible to write:

$$N(\text{Si})D(1 \text{ MeV}, \text{Si})\phi(1 \text{ MeV}, \text{Si}) = N(\text{Si})\int_0^\infty D(E, \text{Si})\phi(E)dE \quad (6.5)$$

where

$D(1 \text{ MeV}, \text{Si})$ is the silicon displacement kerma value for 1 MeV neutrons, (the standard value used for this quantity is 95 MeV mb where $1 \text{ mb} = 10^{-27} \text{ cm}^2$), and

$f(1 \text{ MeV}, \text{Si})$ is the displacement damage equivalent fluence of 1 MeV neutrons in silicon.

Prior to the recent work showing that the amount of displacement damage produced was independent of the energy spectra and even of the type of incident particle, the validity of Equation 6.5 was based on empirical measurements made on transistors irradiated at different types of nuclear reactors, (Verbinski 1979).

This displacement damage equivalent fluence is then given by:

$$\phi(1 \text{ MeV}, \text{Si}) = D(1 \text{ MeV}, \text{Si})^{-1} \int_0^\infty D(E, \text{Si})\phi(E)dE \quad (6.6)$$

$D(E, \text{Si})$ and $D(1 \text{ MeV}, \text{Si})$ are known and do not depend on which reactor facility is being used. It is therefore clear, from Equation 6.6, that $\phi(1 \text{ MeV}, \text{Si})$ can be obtained for a reactor facility once $\phi(E)$ is known. The problem of obtaining the $\phi(1 \text{ MeV}, \text{Si})$ for any reactor irradiation has thus become the problem of measuring $\phi(E)$.

$\phi(E)$ will vary from one reactor facility to another and can change if different amounts of neutron shielding are used around the devices being irradiated. It can also change with time as the fissioning material is consumed and if the core loading or configuration are changed. Large differences, particularly in the low energy part of the spectrum, are also found between fast burst reactors and water moderated reactors.

Measurements of $\phi(E)$ are best made with radioactivation foils which have different neutron energy thresholds for activation. The foil activities measured for some particular location are compared to the results of a spectrum unfolding code which uses foil activation cross sections and

adjusts the assumed energy spectrum until a best fit to the measured activation data is obtained. The measurements are difficult and costly so they are performed only infrequently, and only for a limited number of reactor operating conditions and locations. The shape of the energy spectrum does not depend on the total fluence of neutrons that was produced.

Once the shape of the energy spectrum has been determined at a given reactor facility, subsequent fluence measurements for irradiations of electronic devices are usually based on radioactivation of a material irradiated at the same time and in the same location as the device under test. ASTM standards 263, 264, and 265 give procedures for measuring neutron flux with iron, nickel, and sulfur activations, respectively. Sulfur is probably the most commonly used material. Sulfur is available in high purity, has a reasonably high activation cross section, and leads to ^{32}P , which has a convenient half life of 14.28 days and is an easily detected beta emitter.

The amount of sulfur activity measured depends on the shape of $\phi(E)$ and is proportional to the total fluence the pellet received. The steps by which the measured sulfur activity is converted to the desired $\phi(1 \text{ MeV}, \text{Si})$ fluence are as follows:

Because the threshold energy for neutron activation of sulfur is 3 MeV, it is useful to define the integrated fluence corresponding to the sulfur activation as:

$$\int_{3 \text{ MeV}}^{\infty} \phi(E) dE = \text{SACT} \times K \quad (6.7)$$

where

SACT is the measured sulfur activity, and

K is a proportionally constant which takes into account the detector efficiency, any decay of the sulfur activity during the irradiation and measurement times, and is a spectrum averaged activation cross section for the sulfur. K is typically obtained by activating sulfur pellets in a neutron field whose energy

spectrum and absolute intensity are known. For example, a calibrated Californium-252 spontaneous fission neutron source may be used for this purpose. The product of SACT and K thus gives an absolute integrated fluence.

In a typical reactor spectrum, a negligible amount of displacement damage is caused in silicon by neutrons with energies below 10 keV, the lower limit on the integration in Equation 6.6 can be made 10 keV. Equation 6.6 thus becomes:

$$\phi(1 \text{ MeV}, \text{Si}) = D(1 \text{ MeV}, \text{Si})^{-1} \int_{10 \text{ keV}}^{\infty} D(E, \text{Si}) \phi(E) dE \quad (6.8)$$

Next, it is useful to define a quantity which is characteristic of the reactor facility but is independent of the material being irradiated and of the absolute magnitude of the fluence. This quantity, called the "spectral index," is given by:

$$\text{SI} = \left\{ \int_{10 \text{ keV}}^{\infty} \phi(E) dE \right\} \times \left\{ \int_{3 \text{ MeV}}^{\infty} \phi(E) dE \right\}^{-1} \quad (6.9)$$

And, finally, a quantity called the "hardness parameter" (HP) is defined as:

$$\text{HP} = \left\{ \int_{10 \text{ keV}}^{\infty} D(E, \text{Si}) \phi(E) dE \right\} \times \left\{ D(1 \text{ MeV}, \text{Si}) \int_{10 \text{ keV}}^{\infty} \phi(E) dE \right\}^{-1} \quad (6.10)$$

HP is characteristic of the reactor facility and the material being irradiated but, again, does not depend on the absolute magnitude of the fluence.

And, finally, the absolute magnitude of the desired 1 MeV silicon equivalent displacement damage fluence is given by:

$$\phi(1 \text{ MeV}, \text{Si}) = \text{HP} \times \text{SI} \times \text{SACT} \times K \quad (6.11)$$

6.2.11 Dosimetry Summary

The elements of a good neutron dosimetry measurement are:

1. A current measurement of $f(E)$ for the reactor operating conditions, the location and the shielding conditions in which the device has been irradiated. The spectral

index, SI, and the hardness parameter, HP, corresponding to $f(E)$ should be available,

2. Adherence to the recommendations of MIL STD method 1017, especially concerning a neutron field uniformity that is better than 20 percent over the entire sample,
3. Location of the sulfur pellet as close to the device location as possible, and
4. A good measurement of the constant K in Equation 6.7.

6.2.12 Cautions

1. Safety considerations involve the fact that neutron irradiated parts or materials may be radioactive. Handling and storage of specimens or equipment subjected to neutron radiation environments shall be governed by the procedures established by the local Radiation Safety Officer or Health Physicist.
2. Problems with neutron dosimetry have been experienced at reactor facilities that have not recently measured their neutron energy spectra. For this reason, the reactor facilities of choice are those which are currently participating in a certification program for neutron irradiations. If a reactor is used that is not participating in this program, the results of the irradiations should be checked against an irradiation at a participating facility. ASTM Subcommittee E10.07 on radiation dosimetry is providing a focus for these certification activities.
3. If effects from ionizing radiation dose may possibly be a problem, measurements with a thermoluminescent dosimeter (TLD), such as CaF_2 , for example, should be made to determine quantitatively how much total dose is received during a given neutron irradiation.
4. Because of possible complex time dependent effects with ionizing radiation dose, the practice of exposing a device

simultaneously to a given neutron fluence and a given total dose is not recommended.

6.2.13 Applicable Measurement Standards

MIL STD 883 Test Methods and Procedures for Microcircuits.

Method 1017 Neutron Irradiation.

ASTM E263 Standard Test Method for Measuring Fast Neutron Flux by Radioactivation of Iron.

ASTM E264 Standard Test Method for Measuring Fast Neutron Flux by Radioactivation of Nickel.

ASTM E265 Standard Test Method for Measuring Fast Neutron Flux by Radioactivation of Sulfur.

ASTM E668 Standard Practice for the Application of Thermoluminescence Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation Hardness Testing of Electronics.

ASTM E720 Standard Guide for Selection of a Set of Neutron-Activation Foils for Determining Neutron Spectra in Radiation Hardness Testing of Electronics.

ASTM E721 Standard Method of Determining Neutron Energy Spectra Used in Radiation Hardness Testing of Electronics.

ASTM E722 Standard Practice for Characterization of Neutron Energy Fluence Spectra in Terms of an Equivalent Monoenergetic Fluence for Radiation Hardness Testing of Electronics.

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6.3 Hardness Assurance

6.3.1 Hardness Assurance Concepts

In general, the major purpose of any hardness assurance program is to ensure that a device, system or subsystem will meet specified performance requirements. Hardness assurance at the system level consists of all the procedures, controls, and tests applied during system fabrication and procurement to ensure that the system has a response to nuclear radiation that is within the specified limits. System hardness assurance includes controls, with respect to radiation hardness, on how the parts are purchased for system fabrication. The set of procedures, controls and tests used specifically to ensure that the response of a purchased electronic part to a specified radiation environment is within known and acceptable limits has been termed piecepart hardness assurance.

Although a piecepart hardness assurance program is essential to system hardness assurance, it is important to note that by itself, such a program cannot ensure system hardness. The reason for this situation is that the statistical uncertainties associated with piecepart hardness assurance usually do not permit accepted lots to be assigned part survival probabilities high enough for the needs of the system in which they will be used. These statistical uncertainties are large enough because of cost constraints on how large a sample of parts may be tested for lot acceptance together with the fact that radiation tests

are destructive and the tested parts cannot be used in the system.

In practice what is required for ensuring system hardness, therefore, is a combination of piecepart hardness assurance, system design hardening, part selection, and system hardness assurance. The combination of these measures must be adjusted for optimum cost effectiveness. Thus, for example, a robustly survivable design can reduce the demands on system and piecepart hardness assurance programs. Similarly, the use of a part which can easily withstand the system radiation specifications will simplify the piecepart hardness assurance problem.

Major emphasis will be given here to piecepart hardness assurance and to discussion of some of the statistical questions which underlie sample testing. Some discussion will be given for system hardness assurance but this topic is considered beyond the scope of this handbook.

6.3.1.1 Ground Rules for System Hardness Assurance

A number of ground rules are applicable to the formulation of guidelines for a hardness assurance program during the development of a hardened system (Ferry, 1987). The selection of specific ground rules must be tailored for a particular system.

All hardness assurance procedures and documentation must be prepared before the production phase begins. In addition, the hardness assurance procedures must also consider the following operational and logistic requirements of the deployment phase of the system life cycle:

- Hardening approaches for specific nuclear requirements shall be compatible with the formulation of a cost-effective hardness assurance program. The goal should be to minimize procurement costs associated with nuclear hardening, while attaining and maintaining nuclear survivability.
- The hardness assurance program should reflect the basic objective of the overall nuclear survivability/vulnerability (S/V)

program. For example, implementation of a high-cost, high-confidence hardness assurance program for a minimum cost hardened system requiring a moderate confidence of survival would not be logical.

- Centralized guidance and control must be provided in each system acquisition program to ensure that contractor and subcontractor S/V programs are compatible and consistent.
- Maximum utilization must be made of the information and data generated during the full scale engineering development (FSED) phase. Sharing of piecepart response and materials data among contractors should be required as a cost-savings measure.
- Changes and traceability to specific units must be documented to allow for design evaluation during the production period. The quality assurance program should include the early use of configuration control boards (CCB).
- During the development phase, mission-critical (MC) system elements should be identified.
- Hardness-critical items (HCI) and processes (HCP) critical to system hardness must be identified and controlled. This approach to hardness assurance will allow concentrating resources on the most critical design elements.
- Other operational effectiveness and suitability requirements of the system should be evaluated for impact on nuclear hardening during the development program.
- The hardness assurance plan must be part of the quality assurance (QA) and quality control (QC) programs of the contractor. Hardness assurance requirements should be integrated into other program requirements wherever possible to minimize program-wide redundancies and/or inconsistencies.

- The hardness assurance program assures that the system hardness is maintained throughout production; it does not attempt to increase the system design hardness.
- As part of the development program, contractors and subcontractors should be required to prepare design guidelines for their engineering personnel.

6.3.1.2 Design Margins

A basic design concept for electronics equipment is the use of design margins. The design margin is the ratio of the estimated failure level to the specification level for a particular nuclear environment. The design margin concept can be used at both the piecepart level and at the system or subsystem level. The usefulness of incorporating substantial design margins in the initial design becomes apparent in the application of the hardness assurance procedures. When it can be shown that a substantial design margin exists, the degree of control that must be applied to system fabrication or parts procurement to maintain system hardness may be reduced. Conversely, if the design margin is small, stringent system fabrication or parts procurement/reprocurement controls may be required to ensure that the radiation response distribution remains within acceptable limits. The application of special production controls can then significantly increase unit production cost and lead time, and present logistics problems.

For systems with moderate nuclear survivability requirements, it is cost effective to use an approach called the design margin breakpoint (DMBP) method. In this approach, the design margin for each sensitive piecepart or component is compared to a set of predetermined values, called breakpoints. The comparison then effectively categorizes the part sensitivity to each nuclear environment. For systems with more severe nuclear survivability requirements, the DMBP approach may be used in conjunction with MIL-HDBK-814. In such cases, the DMBP program would be applied first and the less sensitive parts would be treated as prescribed by the DMBP program. The more sensitive parts, i.e., the parts with smaller design margins, would

then be subjected to a more sophisticated statistical analysis. In addition, MIL HDBK 815 is available for dose rate hardness assurance and MIL HDBK 816 is available for developing radiation hardness assurance device specifications.

6.3.1.3 Radiation Environments to be Considered

6.3.1.3.1 Ionizing Radiation Dose (Total Dose)

Ionizing radiation dose or total dose is specified in terms of rads(Si) and is the sum of the doses accumulated over the duration of the mission. Ionizing radiation dose includes contributions from the prompt and delayed gamma pulses, from the neutron induced secondary gammas, radioactive clouds and debris, fallout, etc. In space applications it also includes the doses from x rays, and from trapped electrons and protons. The term total dose is somewhat of a misnomer for describing radiation effects because the post-radiation device characteristics depend in a complex way on the time dependence of such separate effects as charge trapping, charge annealing, and interface state growth.

6.3.1.3.2 Neutron Fluence

The neutron fluence specification is expressed in terms of neutrons per square centimeter (n/cm^2), 1 MeV(Si) neutron displacement damage equivalent (ASTM E722-85). If the fluence is not specified as a normalized fluence, the incident neutron spectrum must be taken into account. Typically, the time of neutron deposition in the mission is not specified. (This may not hold true where multiple bursts are specified.) It is generally assumed, for hardening purposes, that the system must operate properly after exposure to the specified number of neutrons.

6.3.1.3.3 Ionizing Dose Rate

Ionizing dose rate is produced in devices by the x rays or the prompt gamma rays emitted from a nuclear weapon explosion. In space applications, the dose rate produced at the surface of the space system by the x rays is much larger than that produced by the prompt gamma rays. If the x rays and gamma rays have to traverse material, i.e., if the point of interest is within a

spacecraft, or for atmospheric or endoatmospheric explosions, the ratio of x-ray induced dose rate to prompt gamma-ray induced dose rate depends on the amount and type of matter that is traversed.

6.3.1.3.3.1 Ionizing Dose Rate Due to Gamma Rays

The gamma ionizing dose rate is expressed in terms of the rads of energy deposited per unit mass, per second; in silicon it is rads(Si) per second. The pulse duration should be specified and can range from about 50 nanoseconds to 1-5 microseconds. For simplicity, a square-wave form is assumed even though a triangular form more closely resembles the actual radiation pulse. A delayed gamma dose rate may also be specified. The delayed pulse is an ionization pulse connected to, and immediately following, the prompt gamma dose rate pulse. It is considerably lower in intensity than the prompt pulse but of a much longer duration, typically microseconds. Because of its low intensity, the delayed pulse often is considered negligible but for circuits that integrate photocurrent response, it can be important. The units are the same as given for the gamma dose rate pulse.

6.3.1.3.3.2 Ionizing Dose Rate Due to X Rays

Because nuclear weapon-produced x rays interact quite strongly with system materials it is essential to describe a system radiation specification in terms of the external free-field x rays that are incident on the system instead of in terms of the energy deposition they will produce in electronic components. The x rays are thus usually specified as an external energy fluence in calories per cm^2 , the time history of the x-ray flux (cal/cm^2 -s versus time), and x-ray spectra are required. The energy spectrum often is defined in terms of the photon output of a blackbody with a characteristic temperature or energy (Richtmeyer, 1955). From the external environment, the system developer must then determine the x-ray environment at specific points of interest in terms of dose, i.e. rads(Si) or cal/g(Au), or dose rate, i.e. rads(Si)/sec, considering the shielding of the system and recognizing the nonequilibrium nature of the dose near interfaces.

Because x rays from a nuclear weapon are deposited in tens of nanoseconds and in a very thin layer of material, often for microelectronics, severe mechanical damage can be produced in electronic devices. Thus, for example, as the level of the radiation exposure increases, the typical progression of damage that was found in underground tests (UGT) in the 1960's was: broken wire bonds, broken die attachment, cracked silicon chips, and, at very high levels, package damage such as lid attachment damage caused by solder melt and/or distortion of the package.

6.3.1.3.4 Single Event Effects

In space systems, upsets and failures in microcircuits can be caused by galactic cosmic rays, solar enhanced particles, or by nuclear reactions induced by energetic protons and neutrons. These highly localized upsets are called single event upsets (SEU). At altitudes above several thousand miles, the intensity, and mass and energy spectra of heavy ion cosmic rays are only weakly dependent on the spacecraft's orbit; at near earth altitudes they can depend strongly on geomagnetic latitude. Energetic protons are found in the earth's trapped radiation belts and in solar flares; the intensity and energy spectra of these protons depend strongly on the spacecraft's orbit. For a geosynchronous orbit, for example, a standard cosmic ray environment has been published and is widely used (Adam's 90% cosmic ray environment; Adams, 1981). For other orbits, environmental models must be used to calculate the fluxes and the quantity of particles that will be encountered. Usually the quantities of greatest interest are the rates at which upsets may be produced and, for this reason, the fluxes of the particles are more important than the total fluences. In some part types, a single ionizing event can lead to a device latchup or catastrophic burn-out; for such devices the total particle fluence should be obtained. A more complete discussion of this subject is contained in Chapter 3.

6.3.1.3.5 Combined Effects

There are combined effects from nuclear environments which must be understood by a system designer or developer. Some examples of combined effects are as follows: 1) SEE post-total

dose, 2) dose-rate upset post-total dose, 3) reliability post-total dose or dose-rate upset, and 4) end of life post-total dose and neutrons.

6.3.2 Piecepart-Level Hardness Assurance

At the piecepart level, hardness assurance consists of all the procedures, controls, and tests used to ensure that the response of a part to a specified radiation environment is within known and acceptable limits. As shown schematically in Figure 6-10, variations in device performance and response occur not only between devices produced by different manufacturers but even between production lots from the same manufacturer.

Piecepart hardness assurance is necessary because the variations in piecepart radiation hardness that occur due to normal production tolerance are frequently so large as to make engineering design and part selection difficult. In particular, hardness assurance controls are imposed on piecepart procurement to avoid the need for excessive radiation hardness design margins. Extra design margins translate into less efficient designs and correspondingly higher costs for given performance requirements. Occasionally, a system or subsystem can be built using pieceparts that are so hard to radiation that even an improbably "soft" part will more than meet the system radiation specifications. In such cases there is no need for hardness assurance procurement controls with the possible exception that selected manufacturers may need to be identified if the required hardness is not available from all manufacturers of the given part type. In practice, the design engineer typically is forced to use at least some part types in his design that have less than the design margin required to preclude testing. For such cases, hardness assurance controls allow more efficient designs and make available a larger selection of parts.

6.3.2.1 Hardness Assurance Procedure – Lot Acceptance Tests

The objective of hardness assurance is to provide statistical controls on the mean values and variabilities of the radiation responses of parts so as to meet system nuclear hardness and survivability requirements. In essence, therefore, hard-

ness assurance controls are used to reject particularly soft parts or parts which are unusually variable.

The various means for controlling the mean value and standard deviation of the radiation response of accepted parts include such things as radiation lot acceptance tests, controls on which manufacturers are allowed to be suppliers, production line process certification and control, and production monitoring. One of the most important of these and the one that will be discussed in greatest detail here is the use of radiation lot acceptance tests to reject unacceptable lots.

Ideally, device hardness radiation response variability should be controlled by the monitoring and adjustment of those steps in the fabrication process that affect radiation response. The relation between process variables and radiation hardness, however, is not sufficient to rely on process controls alone for hardness assurance. It is still necessary, therefore, to test the production-line output of pieceparts to ensure that radiation specifications have been achieved. Exceptions of radiation testing may be found if the value of an electrical parameter can be shown to correlate with radiation response. The gain bandwidth product of bipolar transistors has, for example, been shown to correlate with the susceptibility of the transistor to neutron-induced displacement

damage. In general, however, hardness assurance must rely on lot acceptance based on radiation testing.

Production of very-large-scale integrated (VLSI) circuits with low yield of working devices per wafer and high cost per device has made radiation (destructive) lot-acceptance tests on good devices prohibitive. It is necessary, therefore, to establish radiation response correlations between the actual devices and special test structures fabricated on the same wafer so that acceptance tests can be performed on the test structures. Performance of these lot-acceptance tests must not introduce variability in the characteristics of the accepted product. Two factors are required to ensure this result. The first is to use the same rejection criteria on a particular part type even if the parts are made by different manufacturers. The second is to use the same test methods. Enforcement of these two factors is necessary in order to achieve a standardized product. The use of test standards and a listing of the radiation testing standards that are available were discussed in Section 6.1

6.3.2.1.1 DNA Committee on RHA Device Specifications

DNA has established a committee of radiation effects experts to assist the MIL-STD preparing activities and DESC on technical questions con-

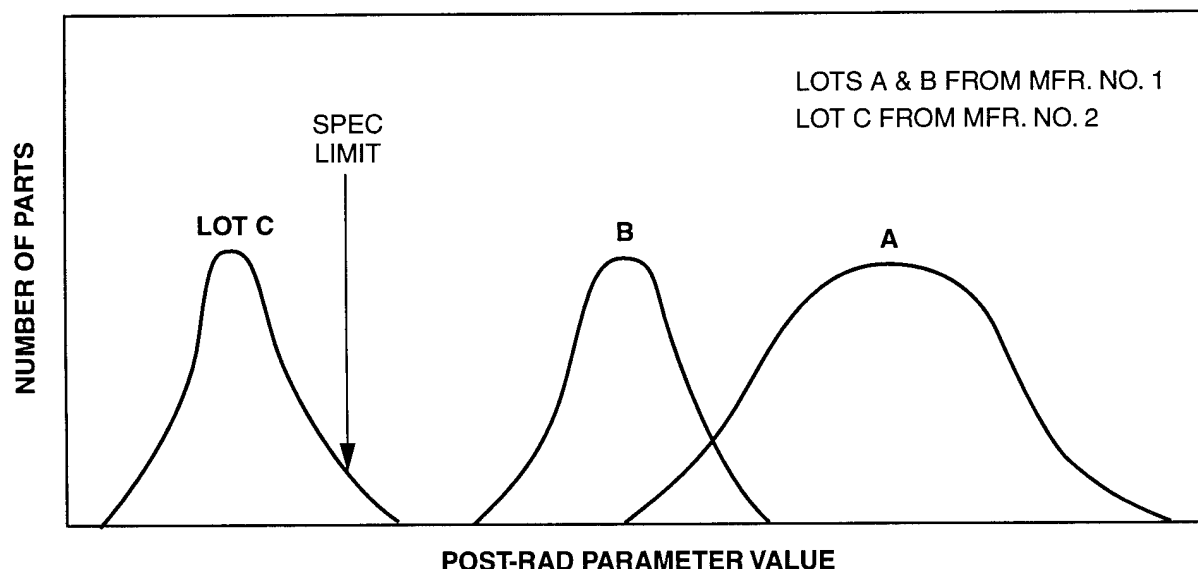


Figure 6-10. Production Variations in Piecepart Radiation Response.

cerning RHA device specifications and standards. This committee has members that represent the three military services, DNA, NASA, Sandia National Laboratories, and DESC and their representatives. The charter of the committee is to work with the RHA community to identify and resolve problems with respect to testing and specification development. The group works closely with DESC on test specification and guideline development.

6.3.2.1.2 Hardness Assurance Guidelines

Comprehensive guidelines have been produced under the DNA Hardness Assurance program that provide a definitive technical foundation for hardness assurance practices at the piecepart level.

The hardness assurance controls in these guidelines are based on the concept of the design margin mentioned in Section 6.3.1.2. The design margin is the ratio of the mean radiation level at which the part fails, PHI(FAIL), to the radiation level specified, PHI(SPEC) for the system in which the part is to be used. The equation for the design margin, DM, is:

$$DM = \text{PHI(FAIL)/PHI(SPEC)} \quad (6.12)$$

(dimensionless)

If the PHI(FAIL) values are normally distributed, the mean value to be used is the arithmetic mean value which is given by:

$$\text{MEAN(PHI(FAIL))} = 1/N \times \text{PHI}_i(\text{FAIL}) \quad (6.13)$$

(same units as the fluence)

where

N is the number of parts tested to failure, and

PHI_i(FAIL) is the failure fluence for the i-th part.

The DM is then given by:

$$DM = \text{MEAN(PHI(FAIL))/PHI(SPEC)} \quad (6.14)$$

(dimensionless)

For convenient reference, the formulas for standard deviations are given here even though they will not be discussed until later sections. Thus, for normally distributed parameter, x, the standard deviation is given by:

$$\text{STDEV}(X) = \{ 1/(N-1) * [X_i - \text{MEAN}(X)]^2 \}^{(1/2)} \quad (6.15)$$

(same units as X)

Because device parameters and device radiation failure levels often obey lognormal probability distributions, the equations given in the remainder of this chapter are usually formulated for lognormal distributions. In such distributions, it is the logarithm of a quantity that is normally distributed instead of the quantity itself. In calculations with lognormal distributions, arithmetic mean values are replaced by geometric mean values and standard deviations of the quantities are replaced by the standard deviations of the logarithms of the quantities.

Thus, if the PHI(FAIL) values are lognormally distributed, the mean value to be used is the geometric mean value which is given by:

$$\text{GMEAN[PHI(FAIL)]} = \text{EXP(MEAN(LN(PHI(FAIL))))} \quad (6.16)$$

(same units as PHI(FAIL))

Note that exponents or arguments of logarithms can only be numerical, i.e. dimensionless, quantities. Thus, if a quantity having dimensions (units) is to be used either as an exponent or as the argument of a logarithm, it is understood that it is divided by a quantity having the same dimensions but with a value of one. This same dimensioned quantity is then used to multiply the logarithm or the exponential factor in order to convert it back to a quantity with dimensions:

where

$$\text{MEAN(LN(PHI(FAIL)))} = (1/N) \text{ LN(PHI}_i(\text{FAIL})) \quad (6.17)$$

(dimensionless)

and where

$\text{LN}(\text{PHI}_i(\text{FAIL}))$ is the natural logarithm of the failure fluence for the i -th part and, as in Equation 6.13,

N is the number of the parts tested.

The DM is then given by:

$$\text{DM} = \text{GMEAN}[\text{PHI}(\text{FAIL})]/\text{PHI}(\text{SPEC}) \quad (6.18)$$

(dimensionless)

And, for a lognormally distributed parameter, the standard deviation of the logarithms is the quantity of interest and is given by:

$$\text{STDEV}(\text{LN}(X)) = (1/(N-1) \times \{[\text{LN}(X)_i] - \text{MEAN}[\text{LN}(X)]^2\}^{(1/2)}) \quad (6.19)$$

(dimensionless)

A parameter DM can also be defined. For parameters whose value decreases with increasing radiation level, the parameter design margin is simply the (geometric) mean value of the parameters after the part has been irradiated with the specified radiation level divided by the specified value of the parameter at which the part fails. In this case the parameter design margin, designated as PDM, is given by:

$$\text{PDM} = \text{GMEAN}[\text{PAR}(\text{rad})]/\text{PAR}(\text{FAIL}) \quad (6.20)$$

(dimensionless)

For parameters whose value increases with increasing radiation level, the PDM is the reciprocal of the quantity given by Equation 6.20.

For simplicity, the DM here is always taken to be the ratio of radiation levels and not device parameter values.

6.2.2.2 Hardness Critical Categories

The guideline documents describe procedures for obtaining the radiation response characterization data, for analyzing the data to obtain the DM, and for using the DM to determine what hardness assurance procedures should be applied. On the basis of their DMs, parts are determined to be either unacceptable or acceptable for use in the system. Acceptable parts are then placed in

one of three hardness assurance categories, namely, hardness critical category 1 (HCC-1), hardness critical category 2 (HCC-2), and hardness noncritical (HNC). For HCC-1, the DM is not very large and a hardness assurance test or control is required for every lot of parts that is purchased. HCC-2 parts have a larger DM than HCC-1 and tests are required only occasionally to ensure that manufacturing processes continue to produce HCC-2 qualified parts. HNC parts have such large DMs that they may be purchased through normal procurement procedures, with no controls required for hardness assurance.

Part categories are based on their DMs in order to help the design engineer identify readily those part types that will need attention and for a commonality of approach to parts testing and controls. Discussions of the various part categories are given below.

6.3.2.2.1 Unacceptable Parts

Unacceptable parts are commonly defined as those with a DM less than 2. However, in actual practice, a part with a DM of just under 2 may still be acceptable since: 1) shielding can be used in its location in the system, 2) the part type may have an unusually small standard deviation in its radiation response, and 3) the parts may receive special screening during procurement. Conversely, a part with a large standard deviation may be unacceptable even if its DM is greater than two. A decision that a part type is unacceptable has potentially serious consequences for the system schedule and costs so that it is best left to the system manufacturer. Figure 6-11 shows the relationship between DMs and hardness critical categories. A shaded region has been used to illustrate the fact that the DM at which a part becomes unacceptable is not a rigidly fixed value.

6.3.2.2.2 Acceptable Parts

HCC-1M is the most sensitive category of acceptable parts and includes all pieceparts whose DMs are relatively small, i.e., whose DMs fall in the interval between a value at which the part just becomes acceptable, to the design margin value at which the part just becomes an HCC-2 part. It is important to note that, if an HCC-1M part is

used in only one or two locations in the system, it may be cost effective to provide local shielding for that part so that its DM can be increased to make it an HCC-2 part.

HCC-1S ranks second in the hierarchy of control sensitivity. This category is applied to pieceparts that have an adequate DM to be an HCC-2 part but are considered non-standard. Because the government has no control or monitoring of non-standard parts, it is necessary to provide some level of systems control even though a significant DM exists.

HCC-1H applies to standard pieceparts that are HCC-2 or HNC based on DM, but are used in hardness-dedicated applications. A hardness-dedicated item (HDI) is defined as a piecepart or circuit that is nonfunctional during normal operation, but becomes functional as a result of one or more of the nuclear-weapon-produced environments. Examples include some radiation detectors, photocurrent compensation devices, circumvention circuits, and interface protection devices.

HCC-2 pieceparts are those with a significant DM, which, however, is not large enough to eliminate them completely from further survivability/vulnerability (S/V) concerns. HCC-2 pieceparts must be standard parts that can be purchased to a radiation hardness assured (RHA) or a MIL STD specification, or a standard military drawing (SMD), or a MIL STD 883 compliant specification.

HNC parts are those with such large DMs that anticipated electrical parameter variations and radiation response will not degrade system operation. Semiconductor pieceparts in this category must be standard parts or procured to the RHA, MIL STD, SMD and 883 compliant specifications listed for HCC-2 parts. In addition to semiconductor devices with large DMs, this category includes parts that are inherently hard to particular nuclear weapon environments. Thus, for example, CMOS parts, being insensitive to neutrons, may be considered HNC with respect to the system's neutron specification even though they may be HCC-1M or HCC-2 with respect to ionizing radiation dose.

From the above HCC definitions, it can be seen that a particular piecepart can fall under more than one HCC. Figure 6-12 shows a flow diagram of the pieceparts categorization procedure. The classification hierarchy is based on the kinds of piecepart procurement controls and on the influence these controls have on system hardness. HCC-1M parts are the most critical, i.e., they have the least margin for error, and have the most stringent HA controls imposed. HCC-1S parts are not very sensitive, but since they are nonstandard, they must be purchased only from controlled sources. HCC-1H is used to flag pieceparts that have relatively large DMs but are essential as HDI to the survivability of the system. There are no special piecepart controls for HCC-1H beyond the requirement that the parts be standard (i.e., MILSTD/HI-REL). HCC-2 parts have a significant DM, and the only control is that they be standard pieceparts. Pieceparts within the hardness noncritical category have quite large DMs, and the risk of their compromising the system is small. The only control placed on these pieceparts is that they be standard parts.

6.3.2.3 Piecepart Categories

Two different methods may be considered for selecting and categorizing pieceparts during the system design hardening phase. Both methods are ultimately based on statistical analysis.

The first method, called the Design Margin Break Point (DMBP) method, applies a predetermined set of categorization criteria to all parts in the system. This method is generally most practical for systems with requirements which are moderate or low. It is based on engineering judgment and considerations of part variabilities. The DMBP method does not provide statistical survivability values. This method has been used by the U.S. Air Force (Ferry, 1987) and by the U.S. Army (Rose, 1981). In the DMBP method, for each radiation environment, the DMs of all the part types to be used in the system, are compared against a single number in order to determine their hardness critical categories and the stringency of the hardness assurance controls that will have to be used for each part type.

The second method is called the Part Categorization Criteria (PCC) Method (Namenson, 1981; Berger, 1979; and Messenger, 1975) and is applied to systems with more stringent requirements, as for example, to systems with high neutron fluence specifications and/or high survival probabilities. It may also be applied to parts which have been put into the HCC-1 category by the DMBP method to see if they can be raised to the HCC-2 category. For each radiation environment, the PCC method applies a separate categorization criterion to each part type. This criterion is determined from the measured variability of the radiation response of the part and is calculated on the basis of small sample statistics. This method employs techniques widely used in industrial quality control (Juran, 1974).

Detailed discussions of these two methods and the impact each has on hardness assurance are given in MIL-HDBK-815. A brief comparison of the two methods follows:

DESIGN MARGIN BREAKPOINT METHOD (DMBP)

In the DMBP method, the DM for each part type (and for each radiation environ-

ment) is compared against a single selected number in order to determine in which HCC the part belongs. The use of a single number and a single set of rules for all parts in the system has the advantage of minimizing the engineering efforts required and also of simplifying the hardness assurance design documentation (HADD) requirements.

The DMBP method is conservative and has the disadvantage of possibly leading to system overdesigns and to a large number of parts being categorized as HCC-1M.

PIECEPART CATEGORIZATION CRITERIA METHOD (PCC)

In the PCC method, the HCC category is determined by comparing the DM for each part type (and for each radiation environment) to a number which is calculated from the radiation response data for that part and which takes into account the variations in the data. The PCC criterion is a statistically more precise criterion and it generally results in a lesser number

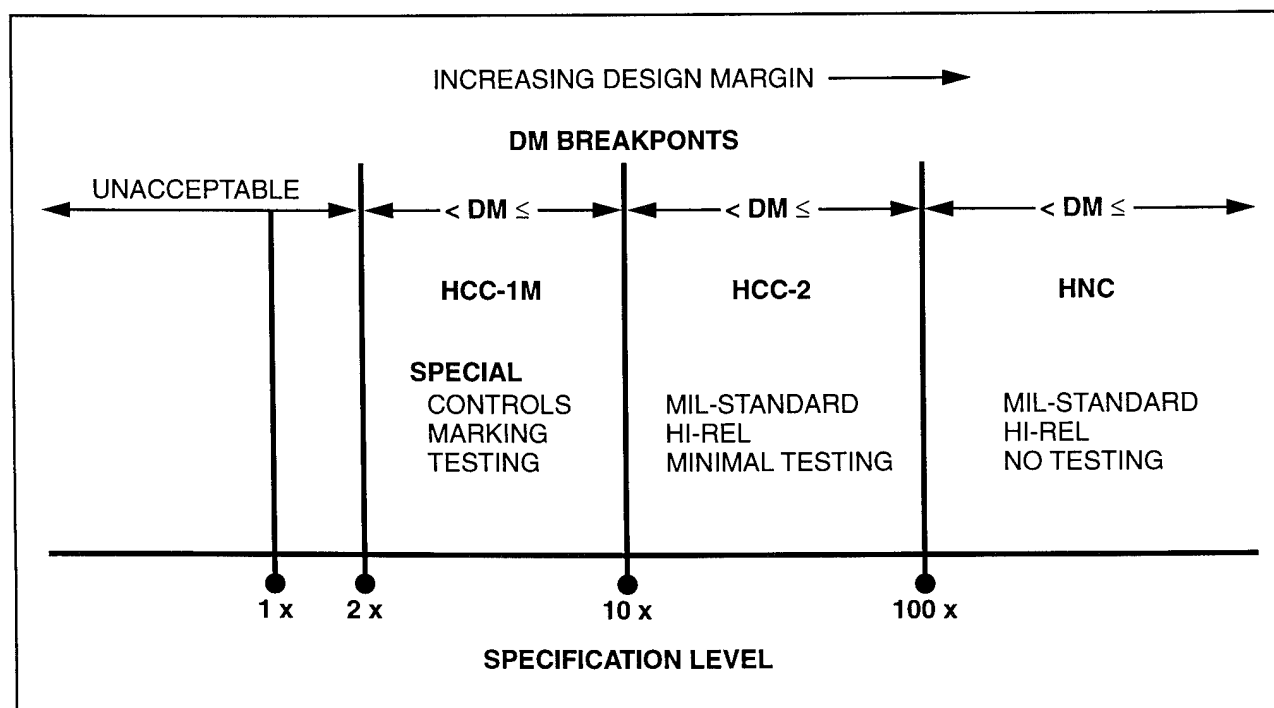


Figure 6-11. Relationship Between Design Margins (DMs) and Hardness Critical Categories (HCC).

of parts being categorized as HCC-1M parts as compared to the DMBP method. This approach can therefore reduce hardness assurance costs over the life cycle of the system.

The PCC approach has the disadvantage of requiring greater engineering efforts to measure the radiation response data and to perform the required statistical analyses for each part type.

The choice of which approach to use is based on engineering judgment, system costs, schedules, and other factors specific to the system. In some systems, the DMBP method will apply to almost all the parts in the system, and only a few part types will require the PCC method. The DMBP method may be used in combination with the PCC method. Because the DMBP method is considered conservative and is simpler to use than the PCC method, it may be initially applied to all semiconductor parts in a system to determine the category of each part type. Following

this, all parts determined to be HCC-1M can be reevaluated through application of the PCC statistical method. In many cases, parts found to be HCC-1M by the DMBP method will be recategorized as HCC-2 by the more mathematically rigorous PCC method.

Both the DMBP and PCC methods require worst-case circuit analyses for the determination of the DMs for each part type. Systems with very stringent requirements may, in addition, require calculation of the failure probability of the whole system. Such analyses are beyond the scope of this document. If they are required, quality control and radiation effects specialists should be consulted.

6.3.2.3.1 Design Margin Break Point Example

An example that illustrates the DM and DMBP concepts is presented in Figure 6-13. The upper curve, labeled "empirical data," is a representation plot of transistor-gain test data as a function of neutron fluence. The upper curve is

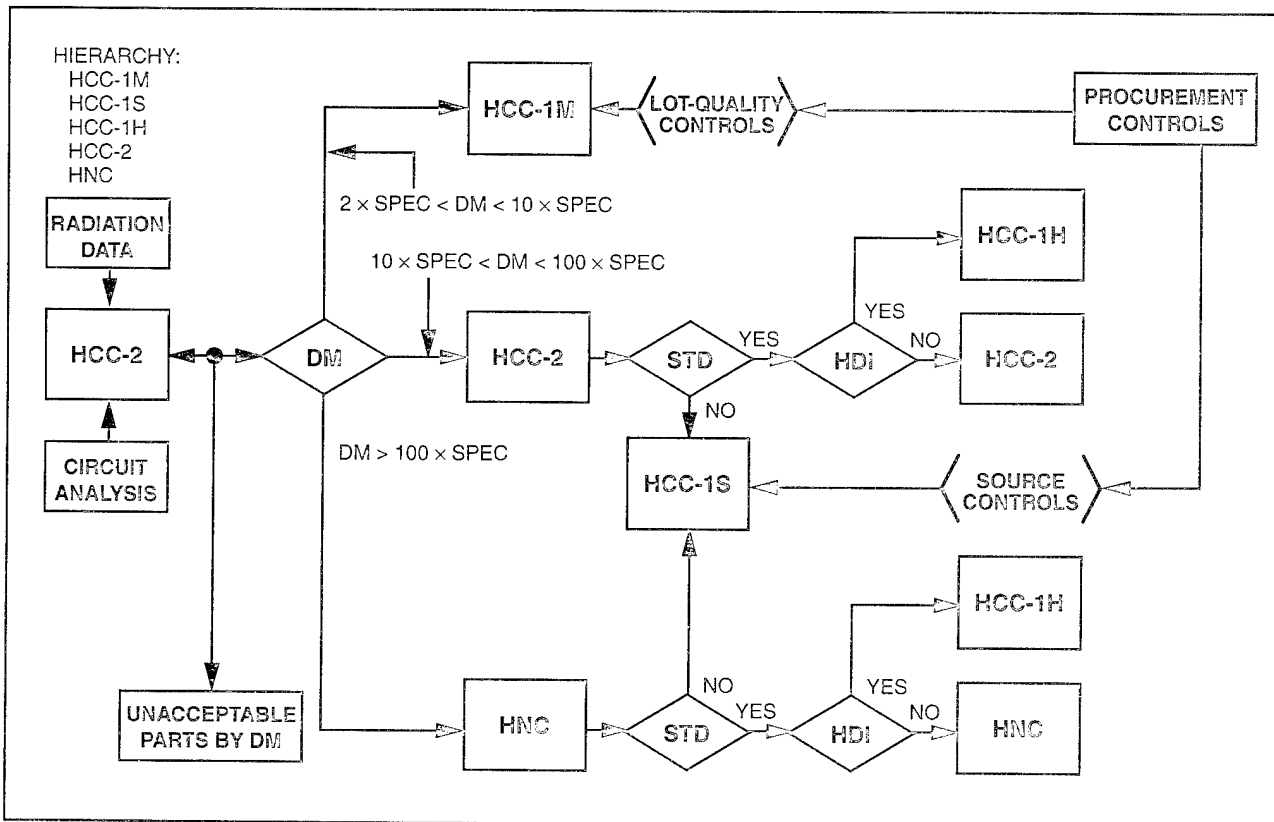


Figure 6-12. Hardness Critical Item (HCI) Categorization Flow Chart.

drawn through the means of the distribution of sample data points, and the extremes of the sample test data are indicated by the error bars. The lower curve is obtained by applying the average damage constant derived from the test data to the manufacturer's published minimum transistor gain, β_{\min} , in accordance with the following equation (Espig, 1985):

$$1/\beta - 1/\beta_{\min} = \text{PHI}(n)/2 \times \pi \times K_n \times f_T \quad (6.21)$$

(dimensionless)

where

- β is the current gain following neutron irradiation,
- β_{\min} is the gain prior to the neutron irradiation,
- $\text{PHI}(n)$ is the neutron fluence in units of (n/cm^2),
- K_n is the damage constant associated with neutron degradation in units of ($\text{n}\cdot\text{sec}/\text{cm}^2$), and
- f_T is the gain-bandwidth product.

This approach applies a limited worst-case condition associated with the unirradiated parts distribution. The calculated curve intersects the analytically determined failure level, $\text{PHI}(\text{FAIL})$, at Point A. From Point A, the failure fluence level, $a \times 10^{x+1}$, can be located on the abscissa. The DM is then the ratio $a \times 10^{x+1}/b \times 10^x$, where $b \times 10^x$ is the specification fluence. The HCC-1M/HCC-2 breakpoint occurs at the point $b \times 10^{x+1}$, and the HCC-2/HNC breakpoint occurs at point $b \times 10^{x+2}$. In this example, the part is found to be HCC-2.

This example is simplified in that it does not address the complex problem of damage constant selection. The neutron damage constant K_n , is a strong function of the device collector current level, I_c . It is recommended that a value of K_n , be developed for a device current level in the region of the peak of the gain. This value will be useful for general design applications and will permit estimation of the damage constant value at lower than maximum current gain levels by

methods given in Larin, 1968. (Junction current density relationship; see also Messenger, 1986.)

6.3.2.3.2 Parts Categorization Criteria

Example

The following example will illustrate how the PCC method is used to determine the HCC for a particular part type. Assume that neutrons are the radiation environment to be considered, the system specification fluence, $\text{PHI}(\text{SPEC})$, is $1.0\text{E}13$ neutrons per cm^2 (1 MeV silicon displacement damage equivalent neutrons), and the combined geometric mean failure level for 2 lots and a total of 20 transistors is 7.29×10^{13} . Equation 6.16 is used to obtain this value. Assume also that the value of $\text{STDEV}(\text{LN}(\text{PHI}(\text{FAIL})))$ (obtained with Equation 6.19), is 0.40. The DM (designated by NDM for neutrons) is then:

$$\text{NDM} = 7.29 \times 10^{13}/1.0 \times 10^{13} = 7.29 \quad (6.22)$$

(dimensionless)

PCC, the criterion against which the NDM has to be compared to determine the part's HCC category, is given by:

$$\text{PCC} = \text{EXP}(K_{\text{TL}}(N,C,P)) \times \text{STDEV}\{\text{LN}[\text{PHI}(\text{FAIL})]\} \quad (6.23)$$

(dimensionless)

where

- $K_{\text{TL}}(N,C,P)$ is the one-sided tolerance limit factor for normal distributions, values for which are given in Table 6-7; this factor takes into account uncertainties about the characteristics of the distribution due to the small sample size used,
- N is the sample size (20 in the present example),
- C is the desired confidence level,
- P is the desired part survival probability, and

$\text{STDEV}\{\text{LN}[\text{PHI}(\text{FAIL})]\}$ is the standard deviation of the natural logarithms of the failure fluences.

Note that the standard deviation of the logarithms of the failure fluences is part of the expression for PCC. The confidence level and the part survival probability are then used to determine K_{TL} from Table 6-7. For C equal to 0.90, P equal to 0.9999, and N equal to 20, the value of K_{TL} is 4.802. PCC then becomes:

$$PCC = \text{EXP}(4.802 \times 0.40) = 6.826.$$

Because $NDM = 7.29$ is larger than $PCC = 6.286$, this part type is HCC-2 for neutrons.

6.3.2.4 Lot Acceptance Tests

Two methods are in common use for lot acceptance tests. The first is based on measuring the mean value and standard deviation of either the radiation failure levels or a radiation induced parameter change in a sample of parts and then comparing these results against a preset criterion to determine whether the lot should be accepted or not. This method is commonly called the "variables method." For a given sample size, the variables method makes best use of the data and yields the highest confidence and part survivability values for the accepted lot. Making the required measurements, recording the data, and making the statistical calculations is, however, relatively costly. Nevertheless, this is the recommended method for making lot acceptance tests.

A second method is based on testing a number of parts with radiation against a pass-fail criterion which is usually a parameter change at a specified radiation level. For a given sample size, a lot is then accepted if the number of failed parts is either zero or less than or equal to some specified number. In the MIL STD procurement system, this method is called the lot tolerance percent defective, or LTPD method, and tables giving the sample sizes and acceptance numbers required to achieve a desired part survivability percentage, at the 90 percent confidence level, are given in the MIL M 38510 and MIL S 19500 microcircuit and semiconductor device specifications, respectively. This method does not require any data recording beyond the pass-fail information. It is relatively inexpensive to conduct, therefore, but it has the disadvantage of being more conservative than the variables method.

6.3.2.4.1 Variables Method for Lot Acceptance

The measured radiation response characteristics of electronic devices show a distribution of values that is caused partly by the measuring process itself and partly by the intrinsic behavior of the quantity being measured. Statistical data analysis methods can therefore be applied directly to radiation response measurements. Statistical analysis most applicable to radiation testing of devices can be found in Appendix E of NA-81; 3. The quantities of interest are the mean value of some device parameter related to a radiation level, its standard deviation, and the statistical distribution that the parameter values obey.

If the statistical distribution of parameter x is known, then the probability that the parameter value of x for a device still to be tested will be smaller than

$$x = \mu + k\sigma \quad (6.24)$$

(same dimensions as x)

where μ and σ are the true mean value and standard deviation respectively, is given by a function $F(k)$, which can be calculated for the particular probability distribution that applies.

In radiation response measurements, the most commonly used distributions are the normal (or Gaussian) and the lognormal distributions. As has already been discussed, in the lognormal distribution, it is the logarithm of the parameter that obeys the normal distribution.

Tables of $F(k)$ values for the normal distribution can be found in most handbooks of mathematical tables. As an example, for the normal distribution, the probability that a measured value x' will be smaller than $\mu + 3\sigma$, is $F(3) = 0.9987$. Another way of saying this is that the pass-fail criterion from testing is set at $x' = \mu + 3\sigma$, then the part survival probability will be 0.9987. Since a mathematically exact knowledge of the probability distribution has been postulated, the confidence associated with the accuracy of this statement is 100 percent.

If, however, the probability distribution is known to be normal, but the mean value and

standard deviation are determined from measurements on a limited number of samples, then the uncertainties associated with such measurements must be taken into account. A commonly used method for including uncertainties due to small sample sizes is to use, in place of $F(k)$, a quantity called the one-sided tolerance limit, usually denoted as $K_{TL}(N,C,P)$, where N is the sample size, C is the confidence level, and P is the part survival probability.

The value of $K_{TL}(N,C,P)$ takes into account the size of the sample, the desired part survival probability, and the desired confidence level. Thus, for example, if the sample size is N , the

desired confidence level of the estimate is C , and the desired part survival probability is P , then the pass-fail parameter criterion should be set at:

$$y = \text{MEAN} + K_{TL}(N,C,P) \times \text{STDEV} \quad (6.25)$$

(same dimensions as y)

where MEAN and STDEV are the measured mean value and standard deviation, respectively. Some values of $K_{TL}(N,C,P)$ for the commonly used 90 percent confidence level are given in Table 6-7.

For example, if the sample size is 5 and if the object is to achieve a part survival probability in

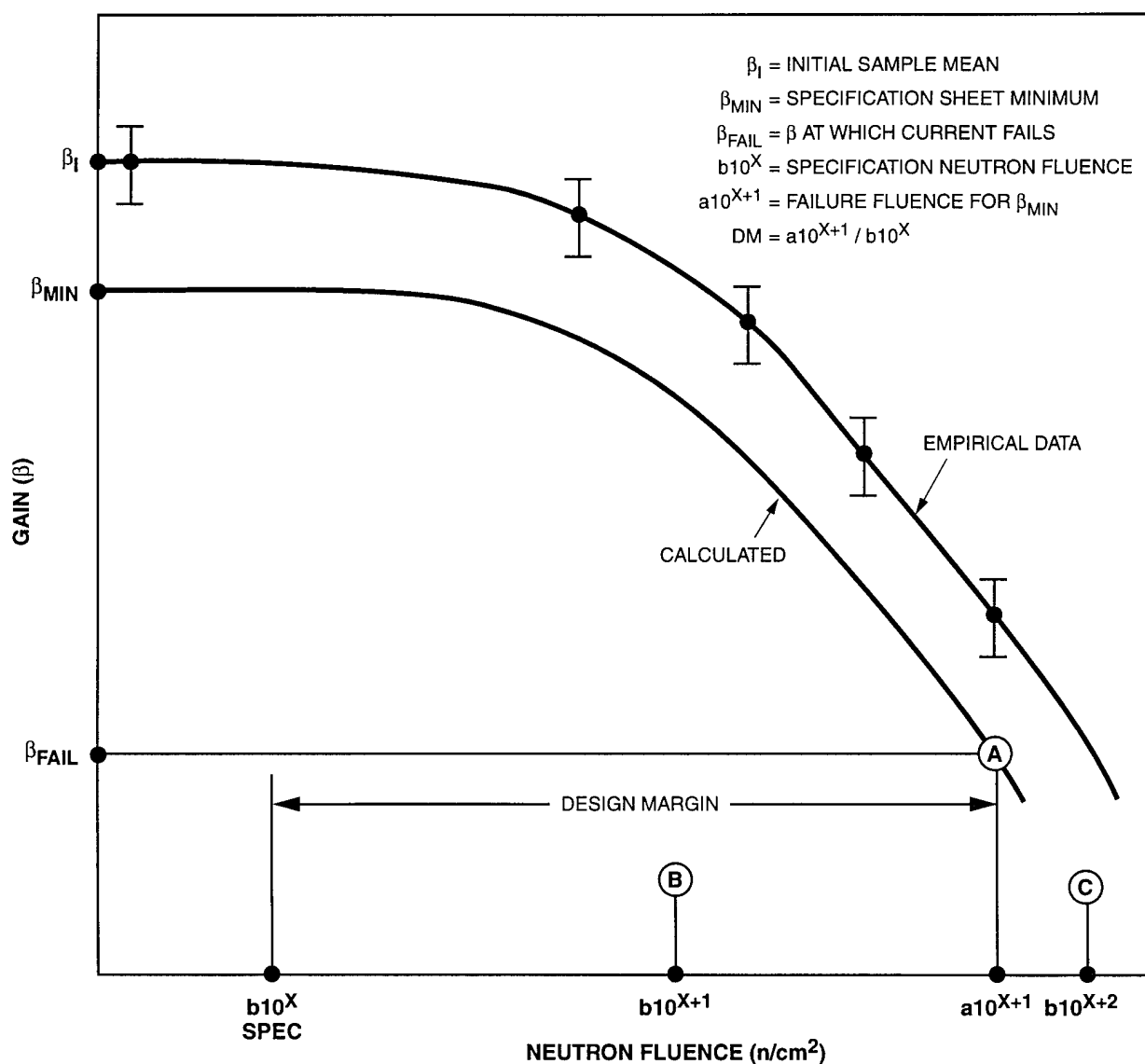


Figure 6-13. Relationship Between Design Margin and Transistor Current Gain.

future tests of 0.999 and 90 percent confidence level, the pass-fail criterion for lot acceptance should be set at:

$$\begin{aligned} y' &= \text{MEAN} + K_{TL}(5, 0.9, 0.999) \times \text{STDEV} \\ &= m + 6.111 \times \text{STDEV} \end{aligned} \quad (6.26)$$

where the value of $K_{TL}(5, 0.9, 0.999) = 6.111$ has been taken from Table 6-7. A comparison of y' with $x' = \mu + 3\sigma$, for which P and C are not much different ($P = 0.9987$ and $C = 1.0$), shows how much larger the pass-fail limit must be to take into account measurement uncertainties due to a small sample size.

6.3.2.4.2 Lot Tolerance Percent Defective Method for Lot Acceptance

In this method, as was previously stated, lot acceptance is based on testing a number of devices, with radiation, against a pass-fail criterion which is usually a change in a device parameter at a specified radiation level. If the number devices that fail the test is zero or is equal to or less than a specified number, called the acceptance number, then the lot is accepted. Thus, for example, the test may call for testing 11 devices and accepting the lot if no devices fail. In abbreviated terminology, this test would be called an 11/0 LTPD test.

The previous section showed what confidence level and part survival probability could be achieved by a variables lot acceptance test. These same quantities are of interest for a lot which has been accepted by an LTPD test. However, as the following discussion will show, an 11/0 LTPD test will only allow a much more conservative statement about the confidence level and part survival probability than would a variables test on the same 11 devices.

Table 6-8 is an excerpt of values given in Table B-I contained in MIL M 38510, the general specification for microcircuits; the values in this table were calculated on the basis of Poisson statistics. The table shows that for an 11/0 test, the maximum percentage of defective parts in the lot is 20 percent. A precise statement of the results of the test is the following: if a lot has more than 20 percent defective parts, an 11/0 test can be depended on to reject the lot with 90 percent con-

fidence. Commonly, design engineers require that parts have a 99 percent survival probability, with 90 percent confidence. The table shows, however, that a single LTPD test can yield a 99 percent survival probability only if 231 devices are tested and no device fails.

Table 6-8 shows that, equivalently, if one device fails, the lot may still be accepted, provided 7 additional devices are tested with no additional failures. (Strictly speaking, the second LTPD test should be performed with a new and independent sample of 18 devices, but this procedure is generally not required.)

It is clear that LTPD tests, by themselves, do not provide the confidence levels and survival probabilities that are typically required by systems design engineers. Two approaches that are commonly used to augment the LTPD lot acceptance tests so that the required confidence levels and part survival probabilities can be achieved are a) the LTPD tests are performed at an overttest radiation level, and b) the expected performance of the part is derated for the system specified radiation environment. Both of these approaches depend on some knowledge of the radiation response characteristics of the part because they both involve an estimate of the variability in the part's performance.

6.3.2.4.3 Radiation Overtests

In practice, if a system specifies a higher part-survival probability than can be achieved with a relatively small sample size, a radiation overttest may be less costly than a test at the lower radiation level but with the sample size increased so that the higher part-survival probability can be estimated. Care must be taken to ensure that the overttests are not producing failure modes that are different from those produced at the lower radiation levels.

The increase in part survival probability and confidence level that can be achieved with an overttest will depend on the amount of the overttest and the standard deviation in the part's radiation response. Of course, the recommended approach to hardness assurance is always to use the hardest parts easily available for the system. The use of an overttest and the very fact that a

Table 6-7. One-sided Tolerance Limits, K_{TL} ($N, C = 0.9, P$) (NA-81; 3.).

Number of Samples, N	Part Survival Probability, P,				
	0.9	0.95	0.99	0.999	0.9999
3	4.259	5.311	7.340	9.651	11.566
4	3.188	3.957	5.438	7.129	8.533
5	2.742	3.400	4.666	6.111	7.311
6	2.493	3.091	4.243	5.555	6.645
7	2.332	2.894	3.972	5.202	6.222
8	2.218	2.755	3.783	4.955	5.927
9	2.133	2.649	3.641	4.771	5.709
10	2.065	2.568	3.532	4.628	5.538
11	2.011	2.503	3.443	4.514	5.402
12	1.966	2.448	3.371	4.420	5.290
13	1.928	2.403	3.309	4.341	5.196
14	1.895	2.363	3.257	4.273	5.116
15	1.867	2.329	3.212	4.215	5.046
16	1.842	2.299	3.172	4.164	4.986
17	1.819	2.272	3.137	4.119	4.932
18	1.800	2.249	3.105	4.078	4.884
19	1.781	2.228	3.077	4.042	4.841
20	1.765	2.208	3.052	4.009	4.802
21	1.750	2.190	3.028	3.979	4.766
22	1.736	2.174	3.006	3.952	4.734
23	1.724	2.159	2.987	3.926	4.704
24	1.712	2.145	2.969	3.903	4.677
25	1.701	2.132	2.952	3.882	4.651
30	1.657	2.080	2.884	3.794	4.546
35	1.623	2.041	2.833	3.729	4.470
40	1.598	2.010	2.793	3.678	4.411
45	1.576	1.986	2.761	3.638	4.363
50	1.559	1.965	2.735	3.605	4.324
60	1.532	1.933	2.694	3.552	4.262
70	1.511	1.909	2.662	3.513	4.215
80	1.494	1.890	2.637	3.482	4.178
90	1.481	1.874	2.617	3.456	4.148
100	1.470	1.861	2.601	3.435	4.124

part can withstand an overtest is consistent with this approach.

6.3.2.4.4 Application of Statistical Concepts

With statistical concepts, care must be taken in applying the results obtained from analysis and experiment on one set of parameters to situations where these parameters do not apply. Some of the major causes of error are the use of a sample size that is too small, unwarranted extrapolation of data to high part-survival probabilities, incorrect sample sizes when lot-to-lot variations are large, and acceptance of one passing lot when the majority of tested lots are failing.

False economy may result from use of too-small a sample size for characterizing the radiation response of a part type in order to set the pass-fail criterion for future lot acceptance tests. Such a criterion may cause lots to be rejected that could pass a criterion based on a larger sample size. If the sample size, for the example, just discussed, had been 10 instead of 5, then the $K_{TL}(10, 0.9, 0.999)$ would have been reduced to 4.628 and the pass-fail criterion would have been correspondingly less stringent.

Assignment of a probability distribution to some given parameter must be based on experimental measurements of that parameter. The accuracy with which the probability distribution is known thus depends on the sample size from which it has been derived. And extrapolation to high survival probability, i.e., to the tail of the distribution, cannot be made unless distribution is known with mathematical exactness. An approximate "rule-of-thumb" is that extrapolations should not be attempted beyond a part-survival probability of $1 - (1/N)$, where N is the sample size on which the probability distribution is based. Thus, for example, an extrapolation to a part-survival probability of 0.999 should not be made unless the part-survival probability distribution is based on a sample size of approximately 1,000 parts.

If there are reasons for believing that parts sampled and procured over some period of time are all coming from the same probability distribution, it may be permissible to consider the ac-

cumulated number of sample parts as the basis of the probability distribution. In such cases, extrapolations of the accumulated data to higher survival probabilities may be valid even for lots accepted on the basis of relatively small sample sizes.

If lot-to-lot variations in some parameter measurement are large compared to the variations measured within any individual lot, then the effective size for the accumulated test sample data for all the lots tested will be smaller than the total number of parts tested. In the extreme case, where the data points from separate lots do not overlap, the effective sample size will be just the number of lots tested, the statistical inferences drawn from the data should be based on that number and the observed variations in the data. Procedures for obtaining the effective sample size and for statistical treatment of the corresponding data have been reported by Arimura, 1983.

In lot sample acceptance tests, the probability always exists that a good lot will fail or that a bad lot will pass. If a large percentage of the lots (e.g., ≥ 75 percent) are failing the tests, then there is a high probability that the few lots that are passing are also bad. If no additional measures are taken to locate and screen out the bad parts, the few lots that pass should not be accepted. This recommendation follows from the fact that the overall percentage of lots failing a given lot-acceptance test contains information about the quality of all the parts in those lots. Thus, a high lot-failure percentage can only result if the average part-survival probability with reference to the pass-fail test criterion is low. Similarly, a low lot-failure percentage implies that the average part-survival probability is high. In this latter and obviously more desirable case, the accumulated record of the percentage of lots accepted suggests that the individual part survival probability is actually higher than that estimated on the basis of a single lot-acceptance test.

6.3.2.5 Existing Data

It is important that existing piecepart data such as that contained in databases like the Electronic Components Radiation Response Information

Center (ERRIC), sponsored by the Defense Nuclear Agency, and RADATA supported by JPL, be utilized early in any piecepart characterization program. Such data can be used to avoid unnecessary characterization testing of pieceparts, thus reducing costs as well as accelerating the parts selection and system design processes. Pieceparts that have been found to be unsatisfactory for a proposed application can be eliminated from further consideration at an earlier stage than might otherwise be possible. A preliminary piecepart selection list for FSED can be developed using existing data. Naturally, any such data must be carefully evaluated for the specific application; further testing may be necessary, but data bank information may minimize such testing. The age of the data and the adequacy of information about the part and how it was tested are important points that need to be evaluated when decisions about part selection or further testing are made.

6.3.3 Parts Procurement

An essential part of any hardness assurance program is the control of production parts. These controls must result in the procurement of acceptable parts for the system. Procurement controls are achieved by the development and utilization of specifications that ensure delivery of the desired qualified items. For nuclear survivability/vulnerability considerations, the stringency of each item's specification depends on its design margin for the relevant environments.

The scope of the specification is generally determined by the size of the DM.

Since the use of parts procurement specifications is an integral part of the hardness assurance program, the hardness assurance plan should include contractor-proposed methods and techniques for the application of the device specifications.

The recommended hardening and hardness assurance programs are based on the use of MIL-STD semiconductor devices as defined in the sections which follow. The use of such parts provides some degree of manufacturing control at a minimal cost, since production controls already exist on these parts for reliability purposes. It is recommended that system designers be encouraged to use MIL-STD RHA parts and consider the total cost of ownership (e.g., part cost plus screening and radiation lot acceptance testing costs) in lieu of only initial part procurement costs.

6.3.3.1 MIL-STD Radiation Hardness Assured (RHA) Device Specifications

6.3.3.1.1 RHA Parts on the Qualified Parts List (QPL)

A scheme for marking RHA MIL-STD devices was previously developed [Wolicki, 1985] and has been used to facilitate RHA part procurement. The proposed letter designations and the radiation levels to which they correspond are given in Table 6-9. These pairs of environments

Table 6-8. LTPD Sampling Plan.

Minimum size of sample to be tested to assure, with a 90 percent confidence, that a lot having percent defective equal to the specified LTPD will not be accepted (single sample).												
Maximum Lot Tolerance Percent Defective	50	30	20	15	10	5	2	1	.5	.2	.1	
	Minimum Sample Sizes											
Acceptance Number	0	5	8	11	15	22	45	116	231	461	1152	2303
	1	8	13	18	25	38	77	195	390	778	1946	3891

were chosen as a way of satisfying the majority of applications, while minimizing cost and part type proliferation. Radiation level designators printed on the part provide a visible identification of the RHA level. For diodes and transistors, the letter designator is placed between the JAN label and part number (see below). For microcircuits, the slash in the part label is replaced by the letter designator for an RHA part; the slash is retained for non-hardness-assured parts. These schemes are shown below with the new letter designators in boldface type.

Discrete Devices, MIL-S-19500. RHA designators M, D, R, or H used as a suffix after JANTX, JANTXV, or JANS:

JANTXV-2N2222A --->
JANTXVM-2N2222A

Microcircuits MIL-M-38510. RHA designators M, D, R, or H used in place of the slash:

M38510/00101BBA --->
M3851OR00101BBA

General specifications MIL-S-19500 and MIL-M-38510 contain the detailed requirements regarding use of the RHA designators.

Additional radiation response specifications, are contained in the detailed specification for single event phenomena (SEP), and for dose rate induced upset, latchup, and burnout.

The radiation response of a device is described by its assured, post-irradiation electrical parameters. To qualify a part as RHA requires several steps. First, the part is characterized for its radiation response. The radiation characterization for a given part type ideally should apply to as many manufacturers of that part type as are on the Qualified Products List (QPL), which is the source document for listing RHA parts. (For example, in 38510-QPL-64, approximately 35 parts are listed as qualified to one or more RHA and quality levels.) At each of the four RHA levels, the endpoint electrical limits are selected so that approximately 90 percent of future lots from most, if not all manufacturers, will pass a lot-

sample test that requires a specified number of parts to pass with no failures. If this criterion cannot be met for the higher radiation levels, lower acceptance percentage for future lots may be allowed. In no case can the limits established for this percentage be less than 50 percent, and the part degradation (i.e., the post-irradiation electrical parameters) cannot be so great as to make the part unusable. If these two conditions cannot be met, then the part does not qualify at the radiation level being considered. The lot sample test requirements for qualification, and quality conformance inspections (QCI) are published in the detailed part specification ("slash sheet") in the Group D table of MIL-S-19500 for transistors and the Group E table of test method 5005 in MIL-STD 883 for microcircuits.

The second step to RHA qualification is qualification of a supplier's part, which leads to the listing of the part on the QPL. The requirements for qualification are also found in the Group E table in MIL-STD883 (Method 5005) and in the Group D table of MIL-S-19500.

The third step to RHA qualification is the lot-acceptance test (or QCI), which is performed before a lot is shipped. These test requirements are found in the same tables as the qualification requirements. Table 6-10 is the Group E table from MIL-STD-883. Note that the qualification and QCI test requirements are tests by attributes, i.e., go/no-go acceptance tests.

6.3.3.1.2 RHA Parts with Standard Military Drawings (SMD)

The use of standard military drawings (SMDs) was initiated by DESC as a means of reducing the duplication introduced into the device procurement system by source control drawings (SCDs) and to reduce the time required to prepare a standard military specification for a new part. In this new approach, DESC develops the SMD for a part from specification limits supplied either by the semiconductor vendor or the user or original equipment manufacturer (OEM). The parts are required to be fabricated at domestic facilities, but off-shore assembly and test is permissible. The reliability of the part depends primarily on vendor self-auditing to paragraph 1.2.1

of MIL STD 883, but DESC has the right to perform audits also. Devices offered through the SMD program are considered equivalent to JAN Class B in quality but are one step lower than Class B in reliability. Hence, they are referred to as "833 compliant" parts. They are identified by their one-part-one-part-number designation:

5962 - year - dwg. no. - device type -
device class - package

Only RHA levels M and D are presently allowed for SMDs. The M or D letter designator replaces the first dash in the part number.

RHA SMD parts are subjected to lot acceptance tests by the vendor, to the conditions specified in the Group E tests shown in Table 6-10. The lot acceptance tests are the same, therefore, as for QPL RHA parts.

6.3.3.1.3 RHA Parts from a Qualified Manufacturer's Line (QML)

The Qualified Manufacturer's List (QML) program was developed by the Rome Laboratories (RL) as a response to the shortcomings of the 38510/QPL method of qualifying new, application specific integrated circuits (ASICs) and other high cost or low volume ICs. The QML requirements are described in MIL-I-38535, General Specification for Manufacturing Integrated Circuits. The philosophy behind this program is that high quality must be built into a part at every step of the production process and cannot be achieved by screening out poorly performing parts with tests performed on the end product parts. The QML program thus focuses on scrutiny over the production process, statistical process control (SPC), and process rather than specific part qualification. These controls then permit less end-of-line and lot acceptance testing of the finished product than required for QPL or SMD MIL STD parts. Once a manufacturer's production line is qualified, individual IC types derived from the qualified process do not have to be separately qualified.

The steps required by the manufacturer for obtaining QML status are line certification and qualification. If the vendor intends to produce RHA parts, then he must demonstrate his ability

to do so at each of those steps. As part of certification, the vendor must 1) show that he has hardness assurance controls in place in the manufacturing process and 2) include hardness assurance in the process capability demonstration by way of test devices. QML qualification is, subsequently, performed on two IC designs. The RHA testing closely follows the Group E approach. An RHA capability level (RHACL) is determined for the QML line; all parts coming off the line are expected to meet all specification requirements at the RHACL. The final step, called technology conformance inspection, can be done either in the standard 883 quality conformance inspection (QCI) or lot acceptance manner, or via on-line control testing. The latter method requires an understanding of the RHA related manufacturing variables and depends on monitoring the appropriate factors with test structures.

6.3.3.2 Non RHA Parts

Any non-RHA parts which must be used should be high reliability (HI-REL) parts. HI-REL pieceparts are those provided by a qualified vendor using appropriate methods and controls that can be related to military standard parts. Many parts manufacturers have established internal standards and programs to provide a commer-

Table 6-9. MIL-STD Radiation Hardness Assurance Specifications (Arimura, 1985).

Part Designation	Total Dose (rads(Si))	Neutrons ^{a,b} (n/cm ²)
M	3×10^3	2×10^{12}
D	1×10^4	2×10^{12}
L	5×10^4	
F	3×10^5	
G	5×10^5	
R	1×10^5	1×10^{12}
H	1×10^6	1×10^{12}

a. 1 MeV(Si) displacement damage equivalent.
b. Lot acceptance tests for the neutron environment will not be performed unless specified in the detailed specification.

cial market source of HI-REL pieceparts. HI-REL programs are generally based on selected requirements taken from the MIL-STDs. Generally, the HI-REL pieceparts are a substantial portion of the manufacturer's market and are readily available. Where pieceparts are not covered by the MIL-STD, they should be procured through manufacturers' in-house programs that yield HI-REL pieceparts. For any device to be qualified based on manufacturers' HI-REL data, a comparative analysis must be made between the HI-REL controls and testing levied and those required for the appropriate MIL-STD for a similar device. A judgment must be made with regard to any differences and the significance of the differences. Results of these comparative analyses should be included as part of the supporting information in the hardness assurance design documentation (HADD). Manufacturers with acceptable programs should be designated as approved sources for the HI-REL piecepart type.

6.3.3.3 Procurement Controls

The types of procurement controls needed for the various device categories differ considerably. Nominally, controls range from the most stringent for HCC-1M to the least stringent for HNC parts, although the differences in some cases are actually related to the qualification and recurrent test sample sizes.

HCC-1M pieceparts are the most critical devices and thus require the most extensive procurement controls. Procurement specifications for HCC-1M parts should be based on MIL-STD or HI-REL parts specifications, with additional controls and testing as necessary to assure that the parts' responses to radiation will not adversely affect the system's survivability. Additional controls and testing include electrical parameter measurements, radiation testing, and processing controls. Generally, the simplest and least expensive procurement control is electrical screening of all the devices in a lot (screening is usually taken to mean testing of 100 percent of the parts), in order to exclude the more vulnerable devices. This procedure works well if adequate information is available to relate the radiation response to a particular electrical pa-

rameter (e.g., bipolar transistor gain/displacement-damage relationship to gain-bandwidth). Actual radiation testing can also be performed as a screen for nonpermanently damaging environments (e.g., dose-rate induced latchup). Radiation sample testing is appropriate for environments that inflict permanent damage (e.g., neutron fluence). If such testing is inadequate to screen out bad lots, processing controls may be necessary. Any processing controls considered necessary must be developed jointly by the system contractor and the manufacturer. Device costs may increase substantially when radiation testing is necessary, and will increase dramatically where processing controls are necessary. Minimum allowable controls and testing, consistent with acceptable technical risk, should be imposed to minimize costs and complexity.

Where HCC-1M devices require special control or testing by the manufacturers, a selected item drawing (SID) is required. The SID must include all the details necessary for procurement of the part. Special inspections or electrical tests must be detailed and include test configurations, sample size, and pass/fail criteria. Similar detail must be developed for any radiation testing. Failed lot recovery procedures should also be developed to determine if a failed lot can possibly be electrically screened in some manner and requalified, or placed back on the commercial market. These points have some bearing on whether the manufacturer or the contractor performs the lost acceptance tests. Processing and test data disposition and documentation should also be specified. Procedures should be developed for incorporating the short-term and long-term multiple-lot data into a database.

When SID parts are specified, care must be taken to avoid violation of reliability requirements. Usually, SID devices are derived from Joint Electronic Device Engineering Council (JEDEC) classified standard devices and require additional screening or sample testing. Any additional radiation-related qualification requirements must be evaluated for potentially adverse effects on reliability. The possibility that reliability can be affected for devices undergoing 100 percent radiation screens should be evaluated.

Table 6-10. Group E (Radiation Hardness Assurance Tests)^a (AR-85 19).

Test	MIL-STD-883		Class S Quantity/ Accept Number	Class B Quantity/ Accept Number
	Method	Condition		
<u>Subgroup 1</u>				
Neutron irradiation	1017	25°C		
Qualification			11(0) or 18(1) ^{b,c}	11(0) or 18(1) ^{b,d}
QCI			11(0) or 18(1) ^{b,c}	11(0) or 18(1) ^{b,d}
Endpoint electrical parameters	As specified per detail specification			
<u>Subgroup 2^e</u>				
Steady-state total dose irradiation	1019	25°C		
Qualification			4(0) ^f 2(0) ^g	22(0) ^b or 38(1) ^{b,d}
QCI			4(0) ^f 2(0) ^g	
Endpoint electrical parameters	As specified per detail specification			
Notes:				
a Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Total exposure shall not be considered cumulative unless testing is performed within the time limits of the test method.				
b New (proposed).				
c Per wafer lot.				
d Per inspection lot.				
e MOS devices need not be tested per subgroup 1.				
f Per wafer for device types with $\leq 4,000$ equivalent transistors/chip.				
g Per wafer for device types with $\geq 4,000$ equivalent transistors/chip.				

There sometimes may be an economic advantage to having the contractor rather than the manufacturer perform the lot qualification tests. For example, if a particular piecepart design margin is determined to be a factor of 9 rather than the needed order of magnitude to be HCC-2 (if the DMBP method is being applied), and a simple electrical screen is the only requirement

for lot acceptance, the contractor may elect to perform the testing. In this case, the part may be procured under a source control drawing (SCD), which only limits the source. The SCD piecepart will be marked with the SCD number, and the SCD must specify the requirements for contractor in-house acceptance testing.

Although HCC-1S pieceparts have significant design margins (HCC-2 or HNC), they are considered procurement-sensitive since they are essentially commercial devices and are not subject to controls such as those exercised by MIL-STD or HI-REL programs. HCC-1S parts qualification and procurement testing are described in Section 6.3.4. HCC-1S parts should be procured through the use of an SCD. The SCD requires only that production pieceparts be procured from the manufacturer(s) which have qualified for supplying that part. The contractor's engineering drawings for HCC-1S pieceparts must contain the details of periodic lot sampling. Tests, inspections, and acceptance criteria associated with the piecepart must be included in the procurement drawing since the SCD will relate only to the acceptable source or sources. Piecepart marking and drawing references will use the SCD number (MIL-STD-100C, paragraph 402.10). The SCD number provides adequate control nomenclature for both procurement and in-house management of these nonstandard pieceparts during system fabrication.

HCC categories -1H, -2, and HNC are standard parts and are procured to the MIL-STD or HI-REL (SCD) specification. These parts will have the normal MIL-STD or STD (for HI-REL parts) marking, which should be adequate for in-house production piecepart control. Although procurement procedures for these HCC-1H, -2, and HNC parts are identical, the qualification and periodic sampling test programs differ (see Section 4.4.4). These test program requirements must be included as a part of the contractor's procurement drawing for each part, but will not be included in the procurement request to the manufacturer. The contractor is responsible for assuring compliance with any specified qualification or periodic sampling.

Figure 6-14 shows an example of how the production processes can be charted with the major production milestones of piecepart fabrication, module fabrication, system assembly, and system deployment included. Each major step has specific activities for control, monitoring, and evaluation. Corrective action loops allow changes in processing, testing, and analysis when problems

are encountered, or in the case of incoming components, negotiations with the supplier.

6.3.4 Parts Qualification and Acceptance Tests

In the full scale engineering development phase (FSED), the early design approach for nuclear hardening of electronic equipment is generally based on existing piecepart radiation response data, calculated and comparative response data, and specially developed design approach for an FSED program. However, for production, more definitive and extensive piecepart radiation response data may be required to validate the hardened design, refine the procurement specifications, and establish a current baseline of the piecepart radiation response for the production program.

Production piecepart specifications must be developed and refined throughout the design development period before initiation of the parts qualification program. Pieceparts should be formally qualified in the latter stages of the FSED program, so that the design and parts selection are essentially final and the period between the qualification program and production can be minimized. For some pieceparts, an iterative process may occur in qualification testing, in defining the procurement specification, and in setting the design limits when the radiation test data reflect unsatisfactory performance characteristics. Part used in the qualification tests should be procured to the same requirements as specified for the production parts. In some cases, particularly where a large DM is observed, the parts characterization data, developed during FSED, may be adequate to serve as qualification data for the system, although data currency and part stability must still be assessed. Also, procurement lead times, particularly for special HCC-1M parts, can prevent timely qualification of a few specific parts. Such problems must be solved individually to assure that the production parts are qualified. In addition, the test responses of parts used for qualification should be compared with the specification to assure adequate control and with the analysis to assure proper categorization. Revision of the procurement specification

sometimes may be required for inadequate or overly severe requirements, and the parts test data may indicate that recategorization is necessary.

6.3.4.1 Pieceparts Qualifications Test Program

6.3.4.1.1 RHA Parts

As discussed in Section 6.4.4.3.1, three types of MIL STD RHA device qualifications are presently in use: 1) MIL STD or JAN, 2) SMD, and 3) QML. For JAN and SMD RHA devices, the parts have already been qualified by the vendor according to the sample sizes and test requirements specified in Table 6-10. QML devices have been qualified in the manner described in Section 6.4.4.3.1.3. Provided that the RHA part meets the system specification, it is not necessary, therefore, for the system contractor again to perform a qualification testing program or lot acceptance tests (also known as quality conformance inspections or QCI) on RHA parts. The contractor may, however, wish to verify the qualifications, particularly if the design margin for a specific device is small. Because the costs of qualification (and lot acceptance) tests can thereby be avoided, the use of RHA parts is strongly recommended.

RHA devices are ordinarily not received with any more information than is given in the RHA device specification. Specifically, no information is received about the mean values or the variability in the data whether it be in the post radiation parameter values or in the in failure fluence values. In the absence of mean values and standard deviations, however, it is not possible, for a system designer to estimate the point at which the given part type will have a probability of survival, P , with a confidence level C . Because these survivability estimates are required in many systems, the system manufacturer must then obtain additional data for the purchased part type even though it may be an RHA part. Values that are commonly required for P and C are 99 and 90 percent, respectively.

If an RHA part is to be used such that its design margin is less than 2, then it can still serve as a starting point but further radiation qualifica-

tion of the device type by the system contractor may be required. Lot acceptance tests will probably also be required for such a device type.

6.3.4.1.2 Non RHA Parts

The guidelines presented here for the pieceparts qualification program address the sample size appropriate for each electronic part category and procurement source, and describe approaches to the desired test techniques for each radiation environment. The approaches are based on the minimum sample sizes and minimum test requirements considered adequate for an acceptance confidence in a part's performance (Ferry, 1987).

Radiation levels for piecepart qualification testing should be based on both the specification levels and the anticipated part response. Typically, a full spectrum of test levels covers more than two orders of magnitude. Radiation levels range from the specification level to two orders of magnitude above the specification level, at which point it can be established that the piecepart is HNC. However, engineering judgment based on historical data and predictions may often be applied to reduce this broad range of testing levels. Data points are desired in the vicinity of the specification level for application to systems hardness verification requirements. However, if a piecepart presents no significant response at a higher radiation stress level, it will generally be acceptable at a lower level.

Table 6-11 presents appropriate minimum and maximum sample sizes. The minimum sample size will generally be adequate to establish piecepart radiation response. Statistics for sample sizes below the minimum are questionable and generally unacceptable, although an exception might be made for a very expensive part.

For qualification testing, HCC-1M parts should have minimum sample size of 10 devices and an additional 2 control devices. If the data scatter is relatively large or determination of the response probability distribution is difficult, the sample size should be increased to as many as 30 parts. HCC-1M qualified pieceparts must be procured to the production procurement specifi-

cation and the manufacturer of each HCC-1M piecepart type tested must be recorded as part of the qualification information.

If the qualification test sample of a particular piecepart fails to meet the radiation-response requirements, a second procurement lot of a like sample from the original or a second manufacturer must be tested. If this test sample fails to meet the test requirements, the design requirements, procurement specifications, and test conditions must be reevaluated to determine whether redesign or piecepart reselection is necessary.

Because of testing costs and other limitations, initial qualification of more than a single source for each HCC-1M piecepart may not be possible. However, if nonavailability or adverse changes in

response (determined from continuous small sample lot acceptance testing during the procurement period) occur, then a second or alternate source must be qualified. Eventual acquisition of a second source for all semiconductor pieceparts is recommended.

HCC-1S pieceparts, while not as sensitive as HCC-1M, have no stated manufacturing controls, and thus a significant qualification sample size is required. The sample size for HCC-1S is the same as for HCC-1M, 10 minimum and 30 maximum. HCC-1S qualification pieceparts must be procured to the same source control drawing as production pieceparts, thereby limiting procurement to specified vendors. In addition, a continuing sampling program throughout the procurement period may be specified for HCC-

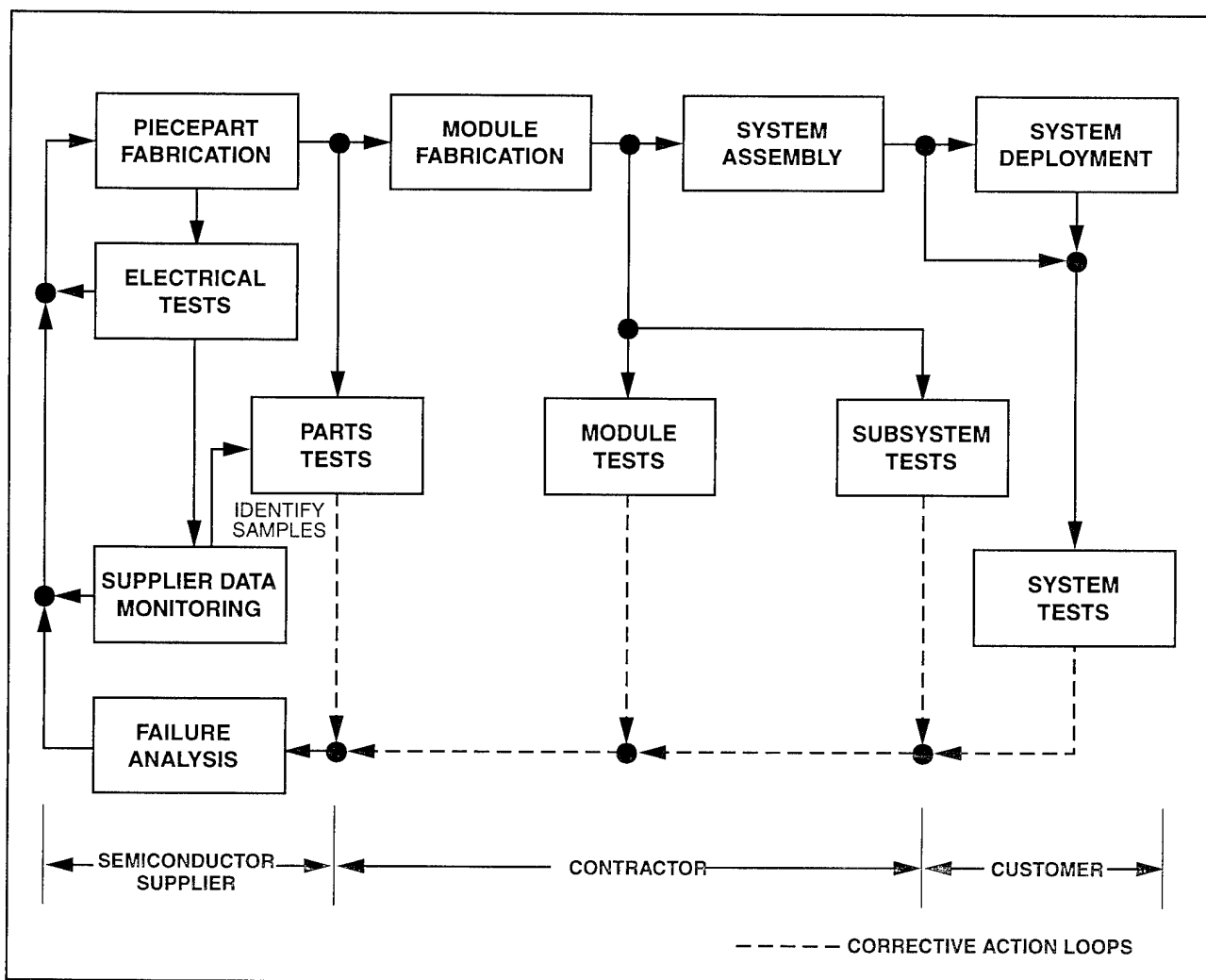


Figure 6-14. Relationship Between Elements of the Hardness Assurance Effort and the Production Flow.

1S pieceparts (particularly for those which are HCC-2 by design margin) in order to maintain confidence in the part's long-term stability.

HCC-1H pieceparts qualification is based on design margin rather than the 1H status. However, the hierarchy logic provides that HCC-1H parts are either HCC-2 or HNC by design margin, and thus they have a sample size minimum of 5 and maximum of 10 and are treated as described for the appropriate design margin categories.

HCC-2 pieceparts have a significant DM, which permits a reduction in sample size from that specified for HCC-1M and HCC-1S. The minimum sample size is 5 and the maximum is 10. If the data from the sample of 5 is inadequate, and additional sample of 5 must be tested. If the sample maximum does not yield adequate data, the parts categorization and design application must be reevaluated. The only procurement requirement for HCC-2 is that the parts be MIL-STD or HI-REL devices. Although it is not necessary to procure MIL-STD pieceparts from a particular manufacturer, the manufacturer of the devices that are tested must be recorded with the data. In the event of a failed piecepart type, such documentation may permit the system contractor to implement a recovery scheme and specify acceptable manufacturers.

A continuing sampling program is required for HCC-2 pieceparts. Engineering judgment must be used to relate such factors as the level of a part's DM within the category, the period of time between successive acquisitions, and any historical stability data.

Piecepart procurement procedures vary with the system production needs, and may involve long-lead preproduction procurement, block buys for portions of the full procurement quantity, or lifetime buys, including spares. Thus, for example, in the Navy's TRIDENT Program, all parts go through the Naval Weapons Support Center Crane Division for screening and tests. As another example, the USAF Space and Missile System Center (SMC) have used Production Assurance Boards which have representatives from both the system manufacturer and the gov-

ernment. If the period between FSED and production go-ahead is short, long-lead items may require ordering before completion of qualification testing. For long periods, special piecepart types and controlled pieceparts may not be available for qualification because of a decision to await production go ahead before ordering costly pieceparts. One approach that can be applied is to prequalify available pieceparts based on the testing of parts that are as representative of the production parts as possible. However, the specified device must still undergo qualification testing before it is actually used in the production equipment.

The use of historical radiation performance data to support multiple procurements over a protracted time period can be problematic. This occurs due to inadvertent and/or planned process and design rule changes that can, over time, alter a part's radiation response. Suppliers periodically revise and upgrade their process and design rules to enhance yield and performance. However, these changes often adversely effect radiation robustness. Moreover, these changes are often not conveyed to a user (i.e., HCC-1S devices). Even if the case were users are apprised of these changes, part requalification can be a time consuming and expensive endeavor. Thus, a system manufacturer should ensure that the efficacy of any historical data is verified and developed in conjunction with a parts procurement plan approach that addresses the various types of device suppliers, that range from the QML supplier with excellent line stability and a part change notification process to that of a commercial supplier who will provide no notice of changes to his fabrication process and often changes his baseline process.

The Parts Control Board (PCB) plays an important role in the qualification program. The PCB assists in establishing criteria for the acceptability of FSED data, reevaluation of piecepart qualification requirements, maintaining records to assure that all pieceparts are qualified, reducing testing requirements through the elimination of redundant testing among contractors, and correlating nonstandard pieceparts with equivalent

standard pieceparts.

The pieceparts qualification program should generally follow the sample size and procurement source outlined in Table 6-11. Qualification testing approaches are described in the following subsections for categories of electronic pieceparts with respect to specific damaging radiation effects.

6.3.4.1.3 Radiation Test Environments

6.3.4.1.3.1 Ionizing Radiation Dose (Total Dose)

Test method 1019 of MIL STD 883, entitled "Steady State Total Dose Irradiation Procedure," specifies cobalt-60 as the radiation source to be used for ionizing radiation dose testing. Ionizing radiation dose testing also may be performed with cesium-137 sources and with low energy x-ray sources. The low-energy x-ray sources have the very important advantage that radiation testing can be done at the wafer level and the substantial costs of packaging parts which fail the radiation testing can thereby be avoided. If a source other than cobalt-60 is used, correlation measurements must be performed to effect a comparison with cobalt-60. High energy electron LINACs are not recommended because of the possibility that the displacement damage which high energy electrons produce may interfere with the measurements. FXR sources which,

typically, deliver the dose at a very high rate, are not recommended because the results may be difficult to compare with cobalt-60.

In general, for ionizing radiation dose measurements, bias must be applied on the device during the irradiations and the bias conditions must be in accordance with the test plan. If the measurements are to be made "in flux," then the test plan should specify these conditions as well. Because time dependent effects can be very important, a complete time history of the irradiations and the post-radiation or in-flux measurements should be recorded. This time history should include the start and stop times of both the irradiations and the measurements as well as the rate at which the ionizing radiation dose was delivered. A pre-test evaluation of the time dependent effects may be necessary to make sure the times used, for the irradiations and the measurements, will give meaningful results.

The qualification test sample sizes, test applications, and procurement sources are as outlined in Table 6-11. The specified ionizing radiation dose level is often relatively low and many types of semiconductor devices are not significantly affected. Engineering judgment may be applied as appropriate to reduce or eliminate qualification testing of particular pieceparts.

Table 6-11. HCC Requirements for Procuring, Marking, Sampling and Testing of Non-RHA Pieceparts (Ferry, 1987).

HCC	Procurement	Marking	Qual Test Sample	Production Parts Tests
1M	SID	Unique number	10 - 30	Lot acceptance
1S	SCD	SCD	10 - 30	Periodic
1H	MIL-STD HI-REL (QPL, SMD, or QML)	Slash sheet	Margin-dependent	Margin-dependent
2	MIL-STD HI-REL (QPL, SMD, or QML)	Slash sheet	5 - 10	Periodic
HNC	MIL-STD HI-REL (QPL, SMD, or QML)	Slash sheet	5 - 10 ^a	None

Notes:
a number may be reduced, depending on design margin and data.

6.3.4.1.3.2 Ionizing Radiation Dose Rate

High energy electron LINACs are the facilities of choice for ionizing radiation dose rate measurements because dosimetry measurements at such facilities are easier to make. If FXR machines are used, extra care is required with the dosimetry to make results obtained at one facility comparable to those obtained at another. FXR pulses do have the advantage that they are more representative of the short gamma pulse produced by a nuclear weapon than are the longer pulses from a LINAC. MIL STDs 1020 on "Radiation Induced Latchup Test Procedure," 1021 on "Dose Rate Upset Testing of Digital Microcircuits" and 1023 on "Dose Rate Response of Linear Microcircuits" may be used as guides. Although latchup screening is not generally recommended, it can be useful for some systems. Some devices have exhibited a "latchup window" whereby they can be made to latchup over a certain range of dose rates but not a dose rates that are either lower or higher than the "window." Thus if a latchup prone part must be used in a system, then testing will be necessary to discover whether a latchup window exists in the subject part type so as to set a dose rate level for the latchup screen which will be within the window. In addition, if a latchup screen is used, then the testing should be performed at the highest temperature expected during system operation.

Qualification testing of pieceparts to the ionizing radiation dose rate environment also follows the requirements given in Table 6-11. Dose rate testing is performed with the part configured in an operating mode. If the device is an integrated circuit, it should be tested with biases and operating conditions that represent worst-case for transient response. An initial piecepart qualification sometimes may be based to some degree on circuit-level testing. This stems from difficulties in modeling and analyzing the circuit and relating the individual piecepart contributions to the circuit radiation response under dynamic conditions. However, at some point it is necessary to derive and specify the appropriate parameter limits at the piecepart level to ascertain hardness-critical categories and to develop procurement specifications.

Piecepart data should included pre- and post-test electrical characterizations, as well as dynamically recorded radiation response data. Integrated circuits must be tested in accordance with Methods 1020, 1021, and 1023 of MIL-STD-883. Method 1015 in MIL-STD-750 (Steady State Primary Photocurrent) is applicable to discrete semiconductor pieceparts (see Section 6.1.4). Sample sizes and their applications and procurement source requirements as described in Table 6-11.

6.3.4.1.3.3 Displacement Damage

Displacement damage can be produced in a semiconductor by the following radiations: a) neutrons such as are produced in a nuclear reactor or a nuclear weapon explosion; b) protons such as exist in space in the earth's trapped proton belts and in solar flares; c) by electrons with energies above a few hundred KeV such as exist in the earth's trapped electron belts. In general gamma rays do not produce significant amounts of displacement damage.

Recent research on the displacement damage produced by various types of particles has shown that the amount of damage is proportional to the non-ionizing energy loss (NIEL) produced by each type of particle. Because of this finding, it is now possible to relate the damage produced by one kind of particle to that which will be produced by another kind of particle. Thus, for example, if a fluence of 1.0×10^{12} 1 MeV neutrons per cm^2 produces a certain change in a device's properties, it is possible by using the ratio of the corresponding NIEL values, to predict what fluence of 100 MeV protons will be required to produce the same amount of damage. The availability of these conversion factors means that displacement damage testing may be performed at nuclear reactors, which are usually the most convenient and least expensive facilities to use, and these results can then be converted to whatever type of radiation environment is specified for the system.

If the device response immediately following a burst of radiation is of concern, then short term annealing effects may need to be evaluated (the times of interest for these effects range from

about 1×10^{-4} seconds to about 10 seconds (Messenger, 1986). In general, however, displacement damage may be considered permanent.

The recommended radiation testing procedures for permanent displacement damage apply to any category of device requiring neutron sample test data. Semiconductor testing must be performed in accordance with Method 1017 (Neutron Irradiation) of MIL-STD-883 or MIL-STD-750 (Section 4.1.3). Neutron permanent damage testing is performed at a nuclear reactor operating in either the pulsed or steady-state mode. It is important that the neutron fluence can be accurately expressed in terms of a 1 MeV silicon displacement damage equivalent fluence. (A similar standard is under development for GaAs.) Typically, neutron irradiation of devices in an electrically passive mode is appropriate.

6.3.4.1.3.4 Single Event Effects

Single event effects (SEE) measurements are sufficiently complex so that they should be made in collaboration with one of several groups that are making such measurements routinely. A full characterization measurement for SEUs or latchup produced by heavy ions requires that the number of upsets or the latchup in a particular device be measured as a function of the linear energy transfer (LET) of the ion. Heavy ion irradiations are usually performed at Tandem Van De Graaff accelerators but may also be performed at other high energy heavy ion accelerators (ASTM F-1192).

For SEUs induced by high energy protons, a measurement of the number of upsets per proton per cm^2 made at a single proton energy of 60 MeV or higher is adequate. These results can be used as input data for a theoretical model which can then be used to estimate the number of upsets to be expected in a particular proton environment (Bendel, 1983). High energy protons for SEU tests can be obtained from a number of cyclotron accelerators. The use of Californium-252 for identifying devices which are susceptible to heavy ion upsets is under study. Research is also being performed on the use of highly focused laser beams to produce SEU by simulating the high density ionization track produced by a heavy ion.

6.3.4.1.3.5 Heating Effects

Extreme heating effects, up to and including plasma production and a resulting thermomechanical shock, can be produced at the surface of a target by the low energy x-ray radiations from a nuclear weapon explosion. If electronic devices inside a spacecraft are not adequately shielded, the x rays can also produce thermomechanical shock in such devices. These effects are different from electronic effects that can be produced by a more gradual heating of electronic devices.

6.3.4.1.3.6 Combined Effects

Several possibilities exist for combined radiation effects, depending on the types of radiation environments that a system must be capable of withstanding. A comment which applies to all of these possibilities is that very little data exists on combined effects. In a natural space environment, the combined effects which are most likely to be encountered are the effects of an accumulated ionizing radiation dose (total dose) on the single event upset susceptibility of a microcircuit. Total dose effects on reliability are also a possibility.

6.3.4.2 Pieceparts Acceptance Testing

6.3.4.2.1 RHA Parts

For RHA parts, lot acceptance tests have already been performed by the vendor, according to the requirements given in Table 6-10, before the parts are approved for shipment. There is no need, therefore, for additional lot acceptance tests by the system manufacturer. Because lot acceptance costs can thereby be avoided, the use of RHA, especially QML-SMD, parts is strongly recommended.

6.3.4.2.2 Non RHA Parts

Acceptance testing must be performed on all HCC-1M pieceparts procured for production equipment. The usual terminology applied is production lot acceptance, quality conformance inspection, or certification testing, although the term "lot" is somewhat ambiguous. Variations in system's acquisition affect the timing and procedures for piecepart acquisition and must be factored into the part buy and lot definition. Very

sensitive devices may require that a lot be the manufacturer's processing or diffusion lot, possibly with special controls and traceability. Less sensitive devices may be included in an inspection or fabrication lot (which may consist of several diffusion lots). For even less sensitive devices, a lot may consist of whatever happens to be received as the result of an order. Since the various semiconductor houses tend to interpret procurement specifications differently, it is recommended that any special lot procurement requirements be directly coordinated with the manufacturer to assure a mutual understanding of the requirements.

Lots procured under these special conditions and destined for lot acceptance testing must be held under controlled conditions until the acceptance tests are performed and the lot disposition is determined. Contingency plans should be formulated for possible failed lots. These plans would include consideration of further 100 percent electrical screens of the lot to truncate the distribution, followed by a second lot acceptance test. If several lots fail, the procurement-specification and end data interpretation must be re-evaluated. If most lots fail and one is found acceptable, it may in fact be a misinterpretation related to the small sample statistics and should also be considered a failed lot. Failed lot recovery plans should include possible resale of the pieceparts to organizations not having radiation survivability requirements.

The full details of lot acceptance test requirements must be developed and included as a part of each piecepart procurement package. Details must include electrical test configurations and radiation environments as well as any special considerations, such as temperature. Sample size and selection procedures, as well as pass/fail criteria, must be specified.

Generally, lot acceptance criteria will be based on the variables sampling test method (read and record; MIL STD-414) rather than attributes sampling method (MIL STD-105D). The latter is very often applied to reliability and is a MIL-STD accepted technique; however, although test data and records are minimal, sample sizes become very large for a reasonable P, and C. The

variables sampling method, on the other hand, provides acceptable P, and C values based on a relatively small sample size. Variables sampling is based on parametric radiation response data, developed in the same manner as for parts qualification testing. Thus, taking and assessing data by the variables technique requires more paperwork, but avoids the large sample testing of the attributes method. A benefit of the variables sampling is that the data developed from the lot acceptance tests can be related to the initially developed lot qualification procedures and pass/fail criteria, permitting a judgment of the effectiveness of the specification.

For acceptance testing, the statistical approach recommended for the sampling by variables data is the one-sided tolerance limit technique. This is a recognized small sample approach. References PR-82 and NA-81 contain detailed presentations of this approach, with examples of radiation effects applications. This approach can provide adequate statistics for a sample of as few as 5 pieceparts. However, for lot acceptance testing of HCC-1M pieceparts, the recommended sample size is that specified for the qualification tests, namely, a minimum sample of 10 with the option of extending the sample to 30 if necessary.

A fundamental assumption in this statistical approach is that the distribution is known, and is normal. The data from many part types, however, tend to follow a log-normal distribution. Log-normal distributions are easily handled in the one-sided tolerance limits approach by simply working with logarithms of the parameter values (Croxtton, 1955).

Often, neither the system's nor the piecepart's survival requirements are specified in numerical form. In order to apply statistics to the lot acceptance tests, values for P and C must be developed and agreed upon by the program office and the contractors. Many moderate requirements systems have applied values of P = 90 to 99 percent with C = 90 percent at the part level. Most often, the findings based on statistical data have shown conservatism in interpretation of initial or older data. Thus, values of P = 99 percent, C = 90 percent are recommended for general application to

lot qualification parts acceptance test data.

6.4 System Level Hardness

Department of Defense Instruction (DoDI) 5000.2, directs that nuclear survivability be considered for all DoD systems, and be considered by the service acquisition review councils for other systems. DoDI 5000.2 also specifies the authority and responsibility of various organizations for establishing the requirements, assuring that they have been met, and reviewing overall program (Van Lint, 1986). Each of the services will prepare letters of implementation for instruction 5000.2

Several of the sections relevant to nuclear survivability are the following:

Section 4C-2

System characteristics dictated by operational needs and constraints and critical to the successful operation and support of a new or modified weapon system shall be identified early and specifically addressed in cost-schedule-performance trade-offs.

- (1) Critical system characteristics are those design features that determine how well the proposed concept or system will function in its intended operational environment.
- (2) They include survivability; transportability; electronic counter-countermeasures; energy efficiency; and interoperability, standardization, and compatibility with other forces and systems including support infrastructure.

Section 6F-1

This section replaces DoD Directive 4245.4, "Acquisition of Nuclear Survivable Systems"

These policies and procedures establish the basis for sustaining operational effectiveness and warfighting capability in peacetime and at all levels of conflict (from low-intensity to strategic nuclear) through acquisition of survivable systems, equipments and support.

Section 6F-2

The survivability of all systems that must

perform critical functions in a man-made hostile environment shall be an essential consideration during the acquisition life cycle of all programs, to include developmental and nondevelopmental programs.

Survivability from all threats found in the various levels of conflict shall be considered. This includes conventional; electronic; initial nuclear weapons effects, nuclear, biological, and chemical contamination (NBCC); advance threats such as high power microwave, kinetic energy weapons, and directed energy weapons; and terrorism and sabotage.

6.4.1 Hardness Assurance Procedures

At the system or subsystem level, hardness assurance procedures applied during the production phase ensure that the production line end-product is in accord with the hardened design and in compliance with the nuclear survivability specifications. System hardness assurance is achieved primarily through configuration control, quality assurance, and parts control. Management control is usually exercised through control boards corresponding to each of these three areas. A set of Data Item Descriptions (DIDs) has been developed which specifies in detail how system nuclear survivability should be controlled. Appendix 6.A contains, as an example, a DID entitled: Nuclear Survivability Program Plan, DI-NUOR-80156A. The titles of the other DIDs related to nuclear survivability may be found in the following references: DI-NUOR-80926; DI-NUOR-80927; DI-NUOR-80928; DI-NUOR-80929; and DI-NUOR-81025. Copies of these DIDs may be obtained from the U.S. Army Research Laboratories; Adelphi, Maryland.

Configuration control consists of those actions taken to ensure that no changes are made to the baseline hardened design without review and approval by qualified nuclear survivability/vulnerability (S/V) personnel. Configuration control is especially important to nuclear effects S/V programs, since seemingly insignificant changes in design, process, or assembly procedures can adversely affect survivability. Changes can be made, but they must be made under controlled conditions with adequate assessment of their im-

pect on system hardness.

Quality assurance (QA) consists of the tests and procedures used to ensure that the end-items of the manufacturing/assembly process conform to the baseline hardened design. QA procedures required for hardness assurance are incorporated into the normal QA program. Examples of areas requiring QA control include installation and functional testing of circumvention/clamp circuits and other hardness-dedicated devices, and performance of other S/V-related production item conformance inspections.

Parts control consists of all the measures used to ensure that acceptable parts are used in each application, the term acceptable pertaining here to both electrical and radiation response characteristics. A parts control program is required for military systems in conformance with MIL-STD-965A. This standard is currently written for unhardened systems and must be interpreted for application to nuclear hardened systems.

The concept of a radiation design margin is useful for systems as well as for pieceparts. For a system or subsystem, it is the ratio of the predicted or measured system failure level to the specified level for a particular nuclear radiation environment. For a system then, just as for a piecepart, the larger the DM (i.e., the harder the system design), the less stringent and costly will be the required hardness assurance controls.

Occasionally, the system design includes a part with very desirable operating characteristics but with a poor radiation DM. For such a part, and provided the weight penalty can be tolerated, local or "spot" shielding can be used to increase the DM so that the part can be used with greater confidence.

In general, radiation DMs as large as practical are obtained by "derating" the parameter values that a part will be expected to possess after it has been subjected to the specified radiation environments. Thus, for example, if a given transistor type is expected to have a gain of 100 after it has been exposed to the system specified neutron fluence of 1×10^{12} 1-MeV neutrons per cm^2 , the circuit designer may derate the gain to 80 and design the circuit accordingly. The amount of

derating will be governed by the required system survivability and confidence values and will be calculated from actual radiation response data by means of statistical analyses. Manufacturers usually maintain derating guideline documents, based on actual data, for all the part types that are used by the company for system design and production. Similar data is maintained for effects of temperature and aging and the radiation derating practice is also similar to the way in which deratings are used for temperature and aging. Sometimes, parts data from databases such as ERRIC are used to obtain initial derating estimates.

As the design continues to progress, more accurate data may be required that are not available from existing data banks, and a piecepart radiation test program is established. Data currency requirements are related to system functional and survivability requirements, radiation stress levels, and design margins. A high required probability of survival or a high specified radiation level will drive the data requirements to greater accuracies. If the specification levels and the probability of survival requirements are moderate or low, significant DMs are achievable in most cases and the corresponding requirements for greater data accuracy may be reduced.

The cost implications of design hardening and the hardness assurance controls required to support a particular design should be considered jointly to optimize system performance while minimizing overall costs. Thus, if radiation lot-acceptance tests are indicated for most of the part types selected for use in an original system design (HCC-1M part category), the selection of harder parts and improvements in the system (e.g., circuit) design should be considered so that larger radiation DMs can be achieved. Harder part types and improved design should reduce requirements for costly radiation lot-acceptance tests and increase the use of parts that may be purchased without such tests (HCC-2 or HNC).

The project costs associated with radiation hardness surveillance and hardness maintenance (HS/HM) after the system has been deployed should also be included in the iterative system design process. Hardness assurance, hardness

maintenance, and hardness surveillance are closely related items in the life cycle of a system. Hardness assurance is concerned with the procedures, controls, and tests applied during system fabrication and procurement to assure radiation hardness; hardness maintenance consists of the procedures during system operation to ensure that system hardness is retained; and hardness surveillance is concerned with the procedures for assuring long-term system hardness.

Generally, a hardened design (and the selection of harder part types is considered as part of design hardening) that minimizes hardness assurance costs will also reduce hardness surveillance and hardness maintenance costs. Hardness assurance costs can thus be considered a measure for reducing the overall costs of designing, producing, and maintaining in the field a system that must meet certain radiation specifications.

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Appendix 6.A

Data Item Description

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|-----|---|------|---|
| 1. | Title: Nuclear Survivability Program Plan | | ability in supporting the Program Plan preparation. |
| 2. | Identification Number:
DI-NUOR-80156A | 7.4 | AR 70-60, Nuclear Survivability of Army Materiel, contains the Army policy applicable to nuclear survivability. HDL-CR-81-015-1 and HDL-SR-85-3 are reference documents that provide background information to support the preparation of this Program Plan. |
| 3. | Description/Purpose: | | |
| 3.1 | The Nuclear Survivability Program Plan will describe how the contractor's Nuclear Survivability Program shall be conducted. It describes operations, procedures, design, analyses, tests, and management activities to be performed to meet the specified nuclear survivability requirements. | 7.5 | MIL STD 1388-1A and 2A contain the Army policy applicable to Logistic Support Analysis for materiel acquisitions and contain guidance on the annotation and recording of hardness-unique requirements. |
| 3.2 | This plan provides the basis for the Government's determination that the contractor's Nuclear Survivability Program will meet contractual requirements in a cost effective manner and is applicable to development and non-development programs. | 7.6 | All HDL documents are available from the Defense Technical Information Center (DTIC). |
| | | 7.7 | This DID supersedes DI-NUOR-80156. |
| 4. | Approval Date: January 9, 1990 | 8. | Approval Limitation |
| 5. | Office of Primary Responsibility:
A/LABCOM/SLCHD-NW | 9a. | Applicable Forms |
| | | 9b. | AMSC Number A4867 |
| 6a. | DTIC Required | 10. | Preparation Instructions |
| 6b. | GIDEP Applicable | 10.1 | Reference Documents: The applicable issue of the documents cited herein, including their approval dates and dates of any applicable amendments, notices, and revisions, shall be as specified in the contract. |
| 7. | Application/Interrelationship | 10.2 | General: The Nuclear Survivability Program Plan shall specify the methods and techniques for incorporating nuclear survivability into the design, development, and equipment integration, and for conducting a comprehensive nuclear survivability validation program. It shall include a discussion of the procedures and methods to implement hardness maintenance and surveillance of the deployed equipment. The program plan shall be prepared consistent with the information contained in HDL-TR-1882-I, |
| 7.1 | Application. When a solicitation or contract contains a requirement for nuclear survivability, this Data Item Description (DID) shall be listed on the Contract Data Requirements List (DD Form 1423). | | |
| 7.2 | This DID contains the format and content preparation instructions for the data product generated by the specific and discrete task requirements as delineated in the contract. | | |
| 7.3 | Nuclear Weapon Effects on Army Tactical Systems, Vol. i, Overview, HDL-TR-1882-I, provides the philosophy and guidance for design, analysis, and evaluation of Army systems' nuclear surviv- | | |

HDL-SR-85-3, and HDL-cr-81-015-1, and shall include the information described below.

10.3 Specifics described in the plan:

- a. The plan shall describe in detail the specific approaches to be utilized to achieve nuclear survivability. This discussion shall include electrical and mechanical hardening design features and any operational or procedural methods planned.
- b. The plan shall detail the combination of analyses and tests required to demonstrate survivability. A discussion of design margins to be employed in the analysis shall be included.
- c. The program plan shall describe the nuclear survivability test program to be performed under the contract. Testing at each level of integration (piece part, circuit, etc.) shall be discussed in terms of need, simulators, test levels, dosimetry, instrumentation, etc.
- d. The plan shall include a discussion of the management of the survivability program. The duties and responsibility of primary point of contact shall be identified and discussed. The relationship between the survivability manager and the program manager shall be detailed.
- e. The program plan shall include a functional and operational description of the end item being developed or acquired under the respective contract. This description shall address the key subsystem elements in sufficient detail to enable the government program manager to understand the nuclear survivability program approach.
- f. The plan shall present a schedule of critical survivability program milestones related to the overall program schedule. This time-phased schedule shall indicate initiation, review, and completion for each key nuclear survivability task.

g. The plan shall present a general discussion of the integrated logistic support management approach to field a survivable system, including design, analysis, test, and documentation.

h. The plan shall provide the estimated labor hours, the caliber of labor and the costs for material, supplies, travel, computer, and simulation facilities.

10.4 Designs, analyses, tests, and evaluations described in the plan:

- a. The plan shall delineate analytical efforts that supplement or replace testing, to include identification of computer codes, and the intended applications of these analytical techniques.
- b. The plan shall delineate piece part, component, and subsystem tests to be performed for each specified nuclear environment, with details, such as sample size, test methods, test instrumentation, parameters to be characterized and relationships to analytical efforts.
- c. The plan shall delineate system level tests to be performed, including methods of extrapolation from test environments to the threat environments, the rationale for simulator choices and relationships to analytical efforts.
- d. The plan shall describe anticipated test simulators and test equipment to be employed, test configurations, test article orientation, exposure levels and test data to be obtained. (Reference HDL-SR-85-3)
- e. The plan shall describe the survivability philosophy to include the basis for selection of piece parts, materials, device technologies, circuit and mechanical designs; the specific materials, technologies and designs rejected because of nuclear survivability considerations; assumptions concerning the system design margins; planned operational fixes such as cycling power and any assumptions concerning

- the system operation, function, deployment or configuration that has been used in developing the Nuclear Survivability Plan. There shall be particular emphasis on design philosophy for hardness critical items (HCI) and mission critical equipments. The plan shall describe the configuration control approach to control HCIs and HCPs.
- f. The plan shall describe the approach to the incorporation of nuclear survivability issues and considerations into the appropriate integrated logistic support documentation as early as possible in the program. The integrated logistic support implications shall include operator procedures, maintenance, repair, and overhaul procedures, personnel skill levels, spare parts, repair tools, provisioning and training needs. The procedures of MIL-STDs 1388-1A and 2A shall be followed regarding the proper annotation of HCIs and HCPs for the Logistic Support Analysis and the Logistic Support Analysis Record.
 - g. The plan shall delineate the projected requirements, driven by the nuclear survivability of the system, for custom or hardened parts, materials, or components; the basis of need for these parts; and the impacts of these requirements on the program and system design, cost, operation, function and deployment.
 - h. If the prime contractor or any of the subcontractors are supplying nondevelopment or proprietary materials, components, or equipments under this contract, this plan must detail how the nuclear survivability of these materials, components or equipments shall be evaluated, assured, maintained, and documented during all acquisition phases.
 - i. The plan shall identify the nuclear survivability trade-offs that shall be performed against other system requirements such as schedule, cost, mobility, reliability, producibility and integrated logistic support.
- 10.5 Risk analysis and identification described in the plan:
 - a. Nuclear survivability areas of high risk and uncertainty, including the impact on cost, performance, weight, and man hours shall be identified.
 - b. Assumptions, conclusions, and reasons used in risk analysis and identification shall be delineated.
 - c. Actions taken by the contractor to minimize the impact of risk and uncertainties identified shall be delineated.
 - d. When failure modes and effects analysis (FMEA) or failure modes and effects critically analysis (FMECA) is required elsewhere in the contract, the plan shall indicate how the impact of the survivability degradation risks will be integrated.
 - 10.6 Management interface controls described in the plan:
 - a. Interfaces between the Nuclear Survivability Program and other related programs, such as engineering design, reliability, maintainability, logistic support, configuration management, production engineering, and producibility programs shall be described.
 - b. Methodology and procedures by which the prime contractor shall ensure that any appropriate nuclear survivability program is executed in subcontracts shall be described.
 - c. Actions to be taken to ensure nuclear survivability (to include validation, assurance, and maintenance) for materiel to be procured elsewhere, including any non-development or proprietary items shall be delineated.
 - d. Special requirements to be included in source or product selection shall be delineated.

- e. The management strategy for mission essential items which do not meet system or materiel survivability requirements shall be described. This should also be reflected in risk identification (10.5).
- 10.7 Program management described in the plan:
- a. Responsibilities and authorities of the Nuclear Survivability Program Manager and the nuclear weapons effects (NWE) experts assigned to the program shall be described.
 - b. Management procedures and controls to assure the successful application and accomplishment of nuclear survivability requirements shall be described.
- 10.8 Format: The plan shall be in the contractor's format.
- 10.9 Additional information: The plan shall provide any additional information necessary to adequately delineate the Nuclear Survivability Program.
11. Distribution Statement: Distribution Statement A: Approved for public release; distribution is unlimited.

Appendix 6.B

Single Event Upset Test Facility

1. Facility Description

For advanced SEU testing an SEU Test Facility (SEUTF) has been established at the Brookhaven National Laboratory (BNL) Tandem Van De Graaff (TVG) facility. This facility was established for the U.S. Army Space & Strategic Defense Command (USASSDC) Hardening Program. The key aspects of the SEUTF for advanced SEU testing are:

1. Higher testing throughput,
2. Increased resolution in determining LET thresholds,
3. Capability of performing board level subsystem SEU tests.

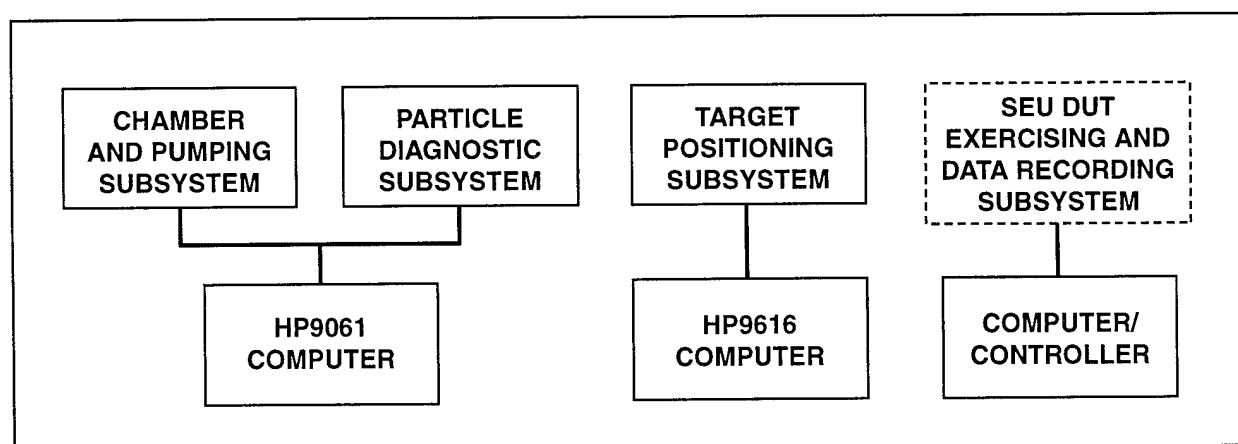
The high throughput and subsystem test capability is achieved by use of a large area (6×10 in²) test exposure board for the Device Under Test (DUT), which can be readily positioned by computer control to place any device on the board in the ion beam at any desired beam angle of incidence or device orientation. The increased LET threshold resolution is achieved by use of the Brookhaven National Laboratories Tandem Van De Graaff which can accelerate a large selection of ion types to appropriate energies to cover almost any LET range of interest. This feature allows the determination of the LET

threshold with less dependency on using the angular generated "effective LET." The angular generated LET determination can lead to significant errors for some devices and must be verified for each device type tested. The beam diagnostics capability of the SEUTF allows for rapid change of ion types, and real time determination of the beam characteristics.

2. SEUTF Description

The facility is operated by the Single Event Upset Test Group, which consists of NASA, NSA, NRL, NWSC and the USASSDC. This facility has been installed and has undergone check-out at the BNL TVG facility. The test fixture has been installed on a dedicated beam line at this facility. The system is available to qualified users with a system of priority established.

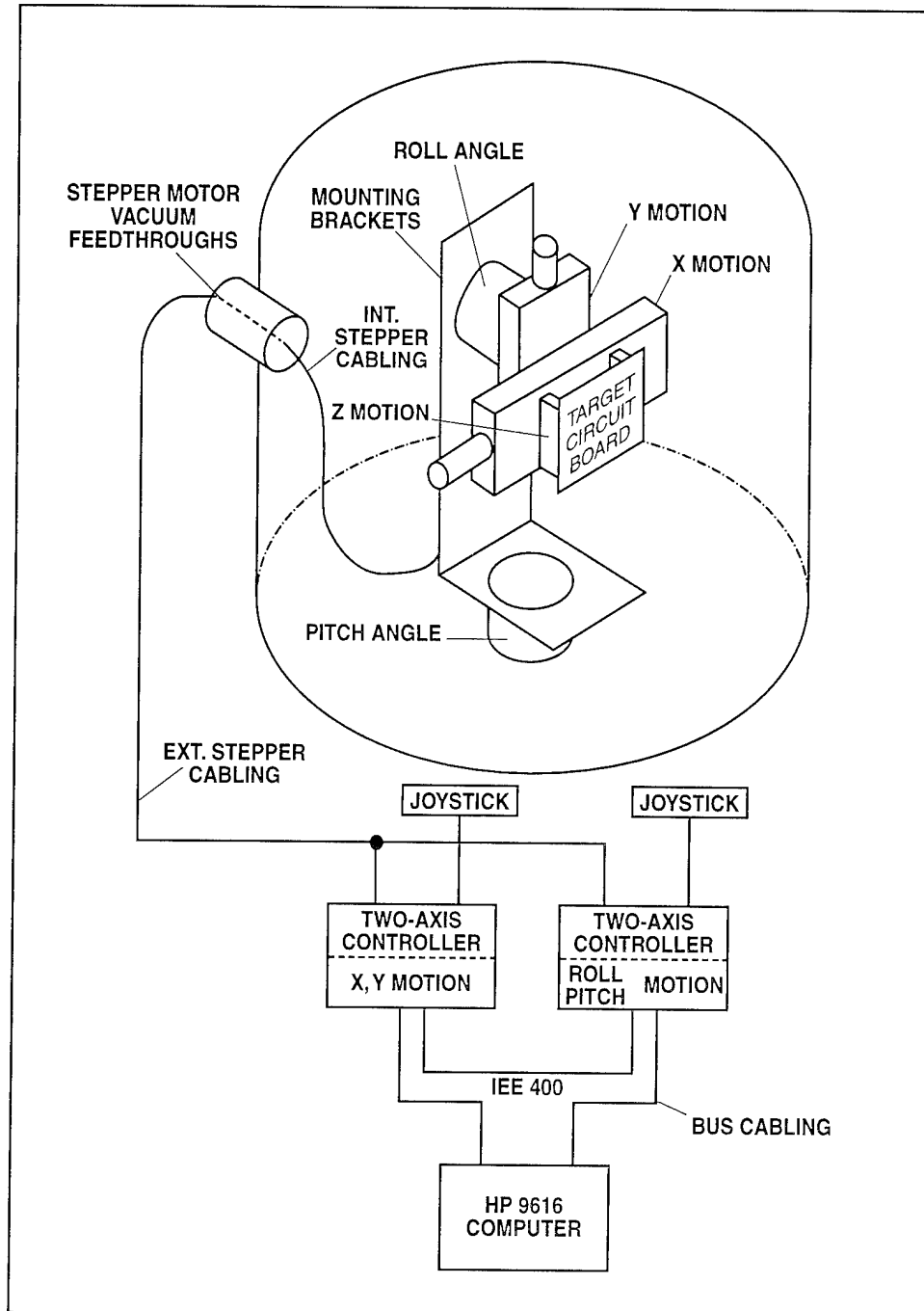
A block diagram of the system is given in Figure 6B-1, and is presently configured to have five major components: a vacuum chamber, a pumping subsystem, a target positioning subsystem, a beam diagnostic subsystem and a computer control subsystem that controls and logs the data for the system. A SEU data acquisition and analysis system is not at present available, but is planned as a future upgrade. At present, the users must supply their own instrumentation for exercising and interrogating the test devices.



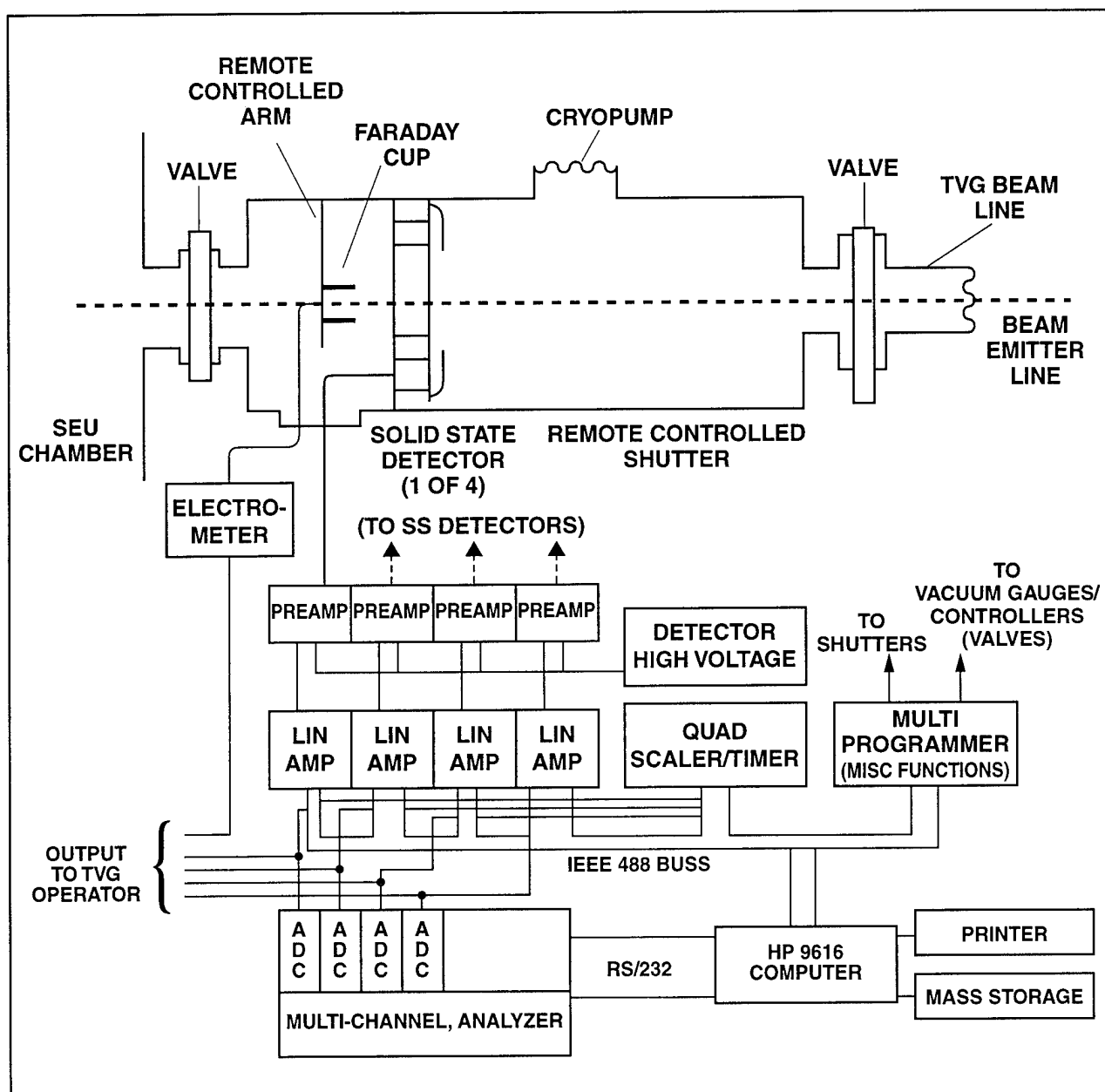
6B-1. Block Diagram of the Single Event Upset Test Facility (SEUTF).

A drawing of the SEU test chamber is shown in Figure 6B-2. Of special interest is the large size of the chamber. This allows room for a fairly sophisticated test card manipulation system that allows two rotation and three translation degrees of freedom. The chamber is designed so that the test platform is mounted on the bottom plate of the chamber, which also contains the vacuum feed through connectors for the DUT

board and positioners. The bottom plate is mounted on a hydraulic lift stand, which in turn is mounted on rails. Thus the entire working platform can easily be lowered and removed from the chamber for installation of DUTs, interior cables, and for determining the location of DUTs relative to the irradiation position. A computer program controls the motion of the translation stages and is programmed to store the



6B-2. Device Under Test (DUT) Positioning System.



6B-3. Particle Analysis System.

location of each device under test so that a simple command can move a designated DUT into the radiation position.

A schematic of the particle diagnostic system is shown in Figure 6B-3. The particle detectors are solid state, partially depleted silicon surface barrier detectors which are used to map the beam flux in a plane perpendicular to the beam axis, as well as to determine the particle energies. These detectors are augmented by a group of four inor-

ganic scintillation/photomultiplier tubes which are used for basic particle counting.

In addition, a Faraday cup can be rotated into the beam to determine the magnitude of the beam current. The output of the solid state detectors and the Faraday cup are routed to the TVG operator to aid in providing a uniform beam. Beam uniformity of better than 10 percent over a two-inch diameter can be obtained.

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Appendix 6.C

Cosmic-Ray Upset Rate Calculation

In this model, the sensitive volume of a device is represented by a parallelepiped with dimensions a, b, c , where $a \leq b \leq c$. The upset rate is obtained by calculating the probability that a cosmic-ray particle passing through the sensitive volume will create ionization along its path greater than the critical charge, Q_c , which is the smallest change required to upset the logic state of a device. E_{dep} , the energy deposited along a chord of length s through the sensitive volume, is related to the linear energy transfer (LET), L , by

$$E_{dep} = L\rho s,$$

where ρ is the density of the material. When E_{dep} is greater than ΔE , a critical energy, a sufficient number of electron-hole pairs is created to cause an upset. In silicon, the critical charge is related to ΔE , the critical energy, by

$$Q_c = \Delta E/22.5 \quad (6C-1)$$

where Q_c is in pC and ΔE is in MeV. Thus, an upset can occur if the particular chord length associated with the passage of a particle of LET, L is greater than s_{min} where

$$s_{min} = \Delta E/\rho l \quad (6C-2)$$

The number of upsets, N_e , is then calculated using a formulation due to J. Bradford:*

$$N_e = \frac{S}{4} \int_{L_o}^{L_{max}} \phi [L] C[s_{min}] dL \quad (6C-3)$$

Here $C(s_{min})$ is the integral chord-length distribution, that is the probability of a particle traversing the sensitive volume with the chord length greater than s_{min} . S is the total surface area of the volume, $S = 2(ab + ac + bc)$. The differential LET distribution, $\phi(E)$, using the transformation.

$$\phi(L) = \phi(E) dE/dL \quad (6C-4)$$

The particle flux ϕ is omnidirectional, and is therefore integrated over 4π steradians. The min-

imum value of L that shall produce an event, L_o , is then given by

$$L_o = \Delta E/\rho s_{max} \quad (6C-5)$$

where s_{max} is the diagonal of the parallelepiped, i.e.,

$$s_{max} = (a^2 + b^2 + c^2)^{1/2} .$$

An approximation for $C(s)$ which is reasonable for b and $c \geq 3 \times a$, is given by

$$C(s) = 0.75 (a/s)^{2.2} \quad s \geq a \quad (6C-6a)$$

$$C(s) = 1 - 0.25 (s/a) \quad s \leq a \quad (6C-6b)$$

where a is the minimum dimension of the parallelepiped.

A basic question in the rate calculation involves the choice of dimensions a, b and c . If no experimental measurements have been made, then a, b and c , as well as Q_c must be obtained from analysis of the device geometry and circuits. Q_c varies from cell to cell, and involves circuit capacitances and resistances that are often not included in circuit response codes. If Q_c is calculated with a circuit code that has been verified for single-event upset work, and if Q_c is obtained for each cell, then the dimensions can be associated with each cell, and the upset rate calculated. There is, of course, always some uncertainty in upset rates obtained in this way.

The situation is slightly better if thorough heavy ion upset testing has been performed. In this case, the LET threshold for upset, L_c , and the limiting upset cross section, σ_L , at high LET are known. The limiting upset cross section is probably a very good approximation for the sensitive surface area of the bit. A comparison of it with device dimensions shall indicate how many cells are involved in the upsets. The threshold LET can be used, together with an assumed cell depth, to calculate the critical charge. The critical

* "Single Event Error Generation by 14 MeV Neutrons Reactions in Silicon," IEEE Transactions on Nuclear Science, Vol. NS 27, No. 6, Pgs. 1480-1484.

charge, cell depth and surface dimensions (obtained from the limiting cross section) can then be used to calculate the upset rate in the cosmic-ray environment.

A number of different cosmic-ray LET spectra have been used, the most common being that of Heinrich, which corresponds to the solar minimum cosmic-ray environment. This environment is usually a best-case situation. An alternative which is both simpler to use and more meaningful for comparisons to satellites is the 10 percent worst-case spectrum. The environment shall be worse than this case 10 percent of the time. The 10 percent case can be approximated by:

$$\phi = \phi_0 L^p \quad (6C-7)$$

with $\phi_0 = 5.86 \times 10^8$ (particles/cm²-day) (MeV-cm²/gm)³ and $p = 3$.

With these approximations for $C(s)$ and $\phi(L)$, it is convenient to introduce a value of LET, L_1 , corresponding to the minimum dimension a :

$$L_1 = \Delta E / \rho a \quad (6C-8)$$

then the upset rate becomes, after Equation 6C-3 has been evaluated,

$$n = 4.9 (S/L_1)^2 [1 - 9/8(L_0/L_1)^{0.2}] \quad (6C-9)$$

where n is in upsets per cell day, S is in μm^2 , and L_1 and L_0 are in MeV/gm/cm².

Note that

$$L_0/L_1 = a/s_{\max} \quad (6C-10)$$

if L_1 is expressed in pC/ μm , the constant is 5.11×10^{-10} .

Because, typically, an order of magnitude is a satisfactory accuracy for this model calculation, Equation 6C-9 is an acceptable approximation.

Another approximation that is useful can be obtained by continuing the above approach. Thus, if heavy ion measurements that determine the limiting cross section s_L and the threshold LET, L_c , have been made,

$$n = 5 \times 10^{-10} \sigma_L / L_c^2 \quad (6C-11)$$

where n has units of upsets/bit day, σ_L is expressed in μm^2 , and L_c is expressed in pC/ μm .

Examples of Calculations Related to Heavy Ion Tests

Consider a device that has cells $3\mu\text{m} \times 10\mu\text{m} \times 10\mu\text{m}$ with $Q_c = 1$ pC. Assume the device has six cells per bit, with one vulnerable, so that the bit error rate shall be the cell error rate.

1. The expected heavy ion cross section for this device is used to estimate the upset rates that shall be produced by the heavy ion tests is:

$$s_L = 1 \text{ (cell/bit)} \times 100 \text{ (}\mu\text{m}^2 \text{ upset/cell-particle)}$$

$$s_L = 1 \times 10^{-6} \text{ (cm}^2 \text{ - upset/bit-particle)}$$

2. The expected LET threshold for testing (LET threshold is used to select the heavy ion species and energies that shall be used for the tests):

$$L_c = Q_c / a$$

$$= 1 \text{ pC} / 3\mu\text{m}$$

$$= 0.33 \text{ pC}/\mu\text{m}$$

where a = cell thickness in micrometers.

This L_c is exceeded by 140 MeV Kr at all angles, and by 160 MeV Argon at angles past 60 degrees. Alpha particles cannot deposit enough charge to cause upset of this device.

3. *Upset Rate Calculation.* The steps below are those that are used to calculate the primary figure of merit for device upset susceptibility.

- a. The critical energy is given by Equation 6C-1.

$$\begin{aligned} \Delta E &= 22.5 \times Q_c \\ &= 22.5 \text{ MeV.} \end{aligned}$$

- b. The minimum value of LET to produce upset is given by Equation 6C-5.

$$L_0 = \Delta E / \rho s_{\max}$$

$$\rho = 2.32 \text{ gm/cm}^3$$

$$s_{\max} = (a^2 + b^2 + c^2)^{1/2}$$

$$= 14.4 \mu\text{m}$$

$$L_0 = 22.5 \text{ MeV} / (2.32 \text{ (gm/cm}^3) \times 14.4 \mu\text{m})$$

$$= 6.7 \times 10^3 \text{ (MeV-cm}^2\text{/gm)}.$$

- c. The L associated with minimum dimension a is

$$L_1 = \Delta E / \rho a = 22.5 \text{ MeV} / (2.32 \text{ gm/cm}^3 \times 3 \mu\text{m})$$

$$= 32.3 \times 10^3 \text{ (MeV-cm}^2\text{/gm)}$$

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TREE Abbreviation/Acronym List

A	atomic weight	DSARC	Defense System Acquisition Council
ADC	analog-to-digital converter	DUT	device under test
ALS	advanced low-power Schottky	EAROM	electrically alterable read-only memory
ASIC	application-specific integrated circuit	ECEMP	electron-caused electromagnetic pulse
ASL	advanced Schottky logic	ECL	emitter-coupled logic
AU	astronomical units	EDAC	error detection and correction
BFL	buffered FET logic	EEPROM	electrically erasable programmable read-only memory
BICMOS	bipolar integrated complementary metal-oxide semiconductor	E-JFET	enhancement junction field-effect transistor
BJT	bipolar junction transistor	EMD	engineering and manufacturing development
BNL	Brookhaven National Laboratory	EMI	electromagnetic interference
CCB	configuration control board	EMP	electromagnetic pulse
CCD	charge-coupled device	EPR	electron paramagnetic resonance
CD	concept development	EPROM	erasable programmable read-only memory
CDR	critical design review	ERRIC	Electronics Radiation Response Information Center
CID	charge-injected device	ESR	electron spin resonance
CML	common-mode logic	FAST	Fairchild advanced Schottky transistor-transistor logic
C-V	capacitance-voltage	FBJ	fully bottomed junction
CMOS	complementary metal-oxide semiconductor	FBR	fast-burst reactor
CTE	charge transfer efficiency	FEMFET	ferroelectric material field-effect transistor
D/V	demonstration/validation	FG EEPROM	floating-gate electrically erasable programmable read-only memory
DEMP	dispersed EMP	FG EPROM	floating-gate erasable programmable read-only memory
DESC	Defense Electronic Supply Center	FFT	flux-free time
DI	dielectric isolation	FLOTOX	floating-gate tunnel oxide
DIIC	dielectrically isolated integrated circuit	FM	frequency modulation
DM	design margin		
DMBP	design margin breakpoint		
DMOS	double-diffused metal-oxide		
DoD	Department of Defense		
DRAM	dynamic random-access memory		
DRO	destructive read-out		

FMEA	failure mode and effects analysis	ICBM	intercontinental ballistic missile
FMECA	failure mode and effects criticality analysis	IEMP	internal electromagnetic pulse
FORS	fiber-optic rotation sensor	IGBT	insulated gate bipolar transistor
FSED	full-scale engineering development	IIL	integrated injection logic
GaAs	gallium arsenide	ILD	injection laser diode
GEO	geostationary orbit	IOC	initial operational configuration
GeV	giga-electron volt	IOT	initial operating test
GMWT	gram atomic weight	IOT&E	initial operating test and evaluation
GTO	gate turn-off (thyristor)	ISL	integrated Schottky logic
HA	hardness assurance	JFET	junction field-effect transistor
HADD	hardness assurance design documentation	JI	junction isolation
HCC	hardness-critical category	JIIC	junction-isolated integrated circuit
HCI	hardness-critical item	KE	kinetic energy
HCP	hardness-critical process	kerma	kinetic energy released in matter
HDI	hardness-dedicated item	keV	kilo-electron volt
HDL	Harry Diamond Laboratory	LDD	lightly doped drain
HEMP	high-altitude electromagnetic pulse	LDEF	long-duration experiment facility [space vehicle]
HEMT	high electron mobility transistor	LEC	light-encapsulated crystal
HEXFET	hexagonally configured power field-effect transistor	LED	light-emitting diode
HFET	heterostructure field-effect transistor	LDO	low-earth orbit
hi-rel	high-reliability	LET	linear energy transfer
HM	hardness maintenance	LINAC	linear accelerator
HMOS	high-performance n-channel metal-oxide semiconductor	LPCVD	low-pressure chemical vapor deposition
HPM	high-powered microwave	LSB	least-significant bit
HNC	hardness noncritical	LSI	large-scale integration
HP	hardness parameter	LSTTL	low-power Schottky transistor-transistor logic
HS	hardness surveillance	LTPD	lot-tolerance percent defective
HST	Hubble Space Telescope	MC	mission-critical
I/O	input/output	MESFET	metal semiconductor field-effect transistor
I-V	current-voltage	MeV	mega-electron volt
IC	integrated circuit	MHDEMP	magnetohydrodynamic electromagnetic pulse

MIS	metal-insulator semiconductor	PDM	parameter design margin
MNOS	metal-nitride-oxide semiconductor	PDR	preliminary design review
MOCVD	mettalo-organic chemical vapor deposition	PIC	"smart power" integrated circuit
MODFET	modulation-doped field-effect transistor	PKA	primary knock-on atom
MOS	metal-oxide semiconductor	PMOS	p-channel metal-oxide semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor	PROM	programmable read-only memory
MSI	medium-scale integration (or integrated)	PWM	pulse-width modulation
NA	numerical aperture	PZT	lead-zirconate-titanium
NDM	neutron design margin	QA	quality assurance
NDRO	nondestructive read-out	QC	quality control
NH&S	nuclear hardening and survivability	QCI	quality conformance inspection
NIEL	non-ionizing energy loss	QML	Qualified Manufacturer's List
NMOS	n-channel metal-oxide semiconductor	QPL	Qualified Parts List
NPB	neutral particle beam	RC	resistor-capacitor
NSSDC	National Space Science Data Center	rf	radiofrequency
NUDET	nuclear event detector	RAM	random-access memory
n/g	neutron-to-gamma ratio	RHA	radiation hardness assurance
OBDP	onboard data processing	ROX	recessed field oxide
OEIC	optoelectronic integrated circuit	RTG	radioactive thermal generator
OEM	original equipment manufacturer	RHACL	radiation hardness assurance capability level
op-amp	operational amplifier	SAA	South Atlantic anomaly
OT	Operate Through [Program]	SBD	surface barrier detector
OTEC	operate-through enhancement controller	SCD	source control drawing
OTPEPROM	one-time programmable, erasable programmable read-only memory	SCR	silicon-controlled rectifier
OVD	outside vapor deposition	SCS	silicon-controlled switch
PCB	Parts Control Board	SDFL	Schottky diode FET logic
PCC	parts categorization criteria	SDIO	Space Defense Initiative Office
PCVD	plasma chemical vapor deposition	SEB	single-event burnout
		SECDEF	Secretary of Defense
		SEE	single-event effect
		SETR	single-event gate rupture
		SEL	single-event latchup
		SEM	scanning electron microscopy

SEP	single-event phenomena	s/v	survivability/vulnerability
SEU	single-event upset	T&E	test and evaluation
SEUTF	single-event upset test facility	TFD	thin film detector
SGEMP	system-generated electromagnetic pulse silicon	T.M.	technical memorandum
SI	Systémé Internationale	T.O.	technical order
SI	semi-insulating	TMS	thermomechanical shock
SI	spectral index	TREE	transient radiation effects on electronics
SID	selected item drawing	TTL	transistor-transistor logic
SMD	standard military drawing	TVG	Tandem van de Graaff (accelerator)
SNOS	silicon-nitride-oxide semiconductor	ULSIC	ultra-large-scale integrated circuit
SOA	safe operating area	USASDC	U.S. Army Strategic Defense Command
SOI	silicon-on-insulator	UVEPROM	ultraviolet erasable programmable read-only memory
SOR	statement of requirements	VDG	van de Graaff (particle accelerator)
SOS	silicon-on-sapphire	VDMOS	V-groove double-diffused metal-oxide semiconductor
SOW	statement of work	VHSIC	very-high-speed integrate circuit
SPC	statistical process control	VLSI	very-large-scale integration
SPO	system project office(r)	VLSIC	very-large-scale integrated circuit
SRA	system requirements analysis	VMOS	V-groove metal-oxide semiconductor
SRAM	static random-access memory	Z	atomic number
SREMP	source-region electromagnetic pulse		
STL	Schottky transistor logic		
STTL	Schottky transistor-transistor logic		

TREE Handbook Symbol List

A	beam particle mass	D_B	base diffusion constant
A	depletion area	D_e	electron diffusion coefficient
A	junction area	$D_n D_p$	carrier diffusion constants
A_C	junction area collector region	DE	the non-ionizing kerma factor
A_E	emitter region	DEF	dose-enhancement factor
A_f	final attenuation	DR(M)	dose rate in material M
A_o	initial attenuation	e	electronic charge
A_s	surface recombination area	E	energy (trapped electrons)
A_{VOL}	open-loop voltage gain	E_B	energy barrier to migration
AW	effective volume for photocurrent production in and near the junction	E_C	conduction band energy
B_r	recombination coefficient	E_c	coercive field
BV	breakdown voltage	E_d	threshold energy to displace an atom from its solid material site (usually 25 eV)
BV_{CBO}	collector-base breakdown voltage	E_{DV}	discrete trapping energy level
BV_{CEO}	collector-emitter breakdown voltage	E_F	Fermi level
BV_{EBO}	emitter-base breakdown voltage	E_{OV}	oxygen vacancy defect energy level
C	capacitance	E_{ox}	oxide electric field
C_d	diffusion capacitance	E_p	electron/hole pair creation energy
C_n	electron capture probability of the recombination center	$E_t(T)$	trap energy dependence on time
C_p	hole capture probability of the recombination center	E_R	recoil energy
C_{ox}	oxide capacitance	E_v	valance band energy
C_{st}	storage capacitance	erf	error function
C_T	depletion capacitance	f_T	cutoff frequency; gain-bandwidth frequency product
CTF	circuit tolerance factor	$f_{T(min)}$	minimum cutoff frequency specification value
dE/dx	ionizing energy loss (or stopping power)	f_y	fractional hole yield
de(M)/dx	particle stopping power in material M	$f_y E_{ox}$	fractional hole yield escaping recombination
D	radiation dose	F(t)	annealing factor
D	diffusion constant	g_m	transconductance
D_b	base doping	g_o	pair density generated per rad; initial density electron/hole pair density per unit dose

G	pulse amplitude	I_{pp}	primary photocurrent
G	carrier generation	I_{pp}^C	collector primary photocurrent
G	thermal generation rate	I_{pp}^E	emitter primary photocurrent
G_S	shunt conductance	I_R	peak injected current
G_{ss}	steady-state pulse amplitude	I_R	reverse leakage current
GMWT	gram atomic weight	I_s	switching current
h_{FE}	common-emitter current gain	I_s	saturation current
HP	hardness paramant	I_{SC}	short-circuit current
I_A	anode current	I_{ss}	steady-state current
I_B	base current	I_{ss}	surface saturation current
I_b	bias current	Ib	NPB output
I_C	collector current	I(t)	total current
$I_C(s)$	stored collector current	J_d	dark (thermal generation) current density
I_{CBO}	collector-base leakage (cutoff) current	J_d	diffusion current density
I_{EBO}	emitter-base leakage (cutoff) current	J_E	emitter current density
I_D	drain current	J_{sc}	space-charge region drift current density
I_d	delayed component of primary photocurrent I_{pp} ; delayed photocurrent	J_{TH}	threshold current density
I_d	dark current	K_D	damage constant
I_{DD}	power-supply current	$K_D(T)$	temperature-dependent damage constant
I_{DS}	drain current source	K_{DV}	donor-vacancy complex rate coefficient
I_{EBO}	emitter-base cutoff current	K_g	generation center rate
I_{GT}	gate trigger current	K_{OV}	oxygen-vacancy complex rate coefficient
I_H	holding current	K_S	surface damage constant
I_I	junction saturation current	K_T	minority-carrier lifetime damage
I_{IL}	low-level input current	K_{TL}	one-sided tolerance limit factor
I_{IN}	input current	K_V	vacancy production rate coefficient
I_L	load current	K_μ	mobility damage constant
I_{OS}	input offset current	$K(E)$	energy-dependent damage factor
I_p	prompt photocurrent		
I_{pd}	prompt drain current		

L	McIlwain parameter for the dimensionless ratio of the earth's radius (approximate geomagnetic distance of a field line in the geomagnetic equator; also called the magnetic dipole parameter)	N_{OV}	oxygen-vacancy complex concentration
L_B	base diffusion length	N_{ph}	photon flux
L_C	LET threshold for uset	N_{ss}	ideality factor for surface recombination
L_E	emitter diffusion length	N_{st}	surface trap density
L_{eff}	effective channel length	N_V	vacancy concentration
L_n	minority (electron) carrier diffusion length	$N_c C_n$	electron lifetime
L_p	minority (hole) carrier diffusion length	$N_c C_p$	hole lifetime
l_c	lattice constant	ND	number of initially displaced atoms
τ	excess carrier lifetime	$N_{ot}(t)$	radiation-induced areal density
M	material	$N_{ot}^0(t)$	oxide-trapped hole density at earliest measurement time
MD	mobile defect concentration	$N(\Phi_n)$	electron density as a function of neutron fluence
n	kinetic order of recovery	P	particle
N	atomic density	p_o	equilibrium value of hole concentration
N_A	acceptor dopant atom density	P_{max}	maximum polarization
N_B	base dopant atom density	P_r	remanent polarization
N_c	recombination center density	P_s	spontaneous polarization
N_D	donor concentration	$P_s(\Phi)$	probability of circuit survival (to neutron fluence)
N_{Di}	initial donor concentration	P_d	diode power dissipation
N_{DV}	donor-vacancy complex concentration	PAR(FAIL)	parameter value at which circuit failure occurs for a particular device
n_i	initial electron density	q	electronic charge
N_i	intrinsic electron density	Q_c	critical charge
N_{it}	interface trap density	Q_{COLL}	collected charge
n_o	equilibrium values of electron concentrations	Q_h	total initial areal charge density of holes
N_o	Avogadro's number (6.022×10^{23} GMWT)	Q_{it}	radiation-induced trapped charge
N_O	oxygen atom impurity concentration	Q_{pp}	total charge in photocurrent pulse
N_{Oi}	initial oxygen atom impurity concentration	$Q(t)$	minority-carrier charge
		R	radial distance

R	range to NPB target	V_{BE}	base-emitter voltage
r_b	diode body resistance	V_{BR}	reverse breakdown voltage
R_B	base resistance (resistor)	$V_{breakover}$	breakover voltage
R_e	earth radii	V_{CB}	collector-base voltage
R_g	source resistance	V_{CC}	dc supply voltage
R_g	gate resistor	V_{CE}	collector-emitter voltage
R_{iE}	common emitter input resistance	$V_{CE(SAT)}$	collector-emitter saturation voltage
R_L	load resistance (resistor)	v_d	diode junction
R_{ON}	finite resistance between drain and source	V_D	drain voltage
R_T	recombination rate	V_{DS}	drain to source voltage
R_S	shunt resistance	v_f	vibrational frequency
R_T	total resistance	V_F	forward voltage
S	surface recombination velocity	V_{fb}	flatband voltage
S	total surface of volume	$V_{fb}(0+)$	initial flatband voltage shift
SACT	sulfur activity	V_G	gate voltage
SI	spectral index	V_{GS}	gate-source voltage
SR	slew rate	V_H	holding voltage
t	time	V_{IH}	high-level input voltage
T	temperature	V_{IL}	low-level input voltage
T_c	Curie temperature	V_{mg}	midgap voltage
T_{el}, T_{incl}	elastic and inelastic average recoil energy	V_{OH}	high-level output voltage
t_{ox}	gate oxide thickness	V_{OL}	low-level output voltage
t_p	pulse width	V_{ON}	on voltage
t_{rD}	read access time	V_{OS}	input offset voltage
t_{PD}	propagation delay time	V_{ot}	negative voltage shift
t_s	transistor storage time	V_{OUT}	output voltage
t_{sr}	saturation recovery time	V_{PO}	pinch-off voltage
T(M)	temperature of a material M	V_S	saturation voltage
V	voltage	V_{SAT}	low-output voltage state; saturation voltage
V_{AK}	anode-cathode voltage	V_T	threshold voltage
V_B	breakdown voltage	V_Z	reference voltage
V_{BD}	breakdown voltage	V_T^0	preirradiation threshold voltage
		$V_{it}(t)$	interface trapped voltage

$V_{ot}(t)$	negative voltage shift from trapped holes	v_{th}	thermal velocity
$V_T(t)$	post-irradiation voltage	ρ	resistivity
W	base width	σ	conductivity
W	depletion layer width	σ_B	base conductivity
W_C	collector junction depletion layer width	σ_c	surface trap cross section
W_{CE}	high-resistivity collector epitaxial width	σ_E	emitter conductivity
W_t	depletion layer width	σ_L	limiting upset cross section
X_m	hole trap emptying depth	$\sigma_{el}, \sigma_{inel}$	elastic and inelastic scattering cross section
$X_m(t)$	time-dependent tunneling distance	σ_t	total interaction cross section
Z_{IN}	input impedance	σ_u	upset cross section
α	absorption coefficient	$\sigma(M)$	specific heat of material M
β	tunneling barrier height parameter	τ	mean lifetime of a mobile defect
β	current gain, forward current gain	τ	half-life of incremental loss
β_f	forward gain	τ	minority-carrier lifetime
β_{min}	minimum gain specification value	τ_B	base layer minority-carrier lifetime
β_T	failure threshold for gain	τ_C	collector layer minority-carrier lifetime
β_o	pre-irradiation gain	τ_E	emitter layer minority-carrier lifetime
$\dot{\gamma}$	absorbed dose rate	τ_g	generation lifetime
$\dot{\gamma}_{ss}$	steady-state dose rate	τ_i	unirradiation minority-carrier lifetime
Γ	geomagnetic constant	τ_n, τ_p	carrier lifetime constants
δ_n	injection level	τ_0	pre-rad minority-carrier lifetime
δn	injection level	τ_s	transistor storage time constant
δn	excess current carrier	τ_{scr}	carrier lifetime in the space-charge region
Δn	excess injected minority-carrier density	ϕ_{ph}	photon flux
ΔI_c	transient collector photocurrent	$\phi(P,E)$	flux of particles with energy E
ϵ	dielectric constant	Φ_n	neutron fluence
ϵ	permittivity	$\Phi(P,E)$	fluence of particles with energy E
ϵ_o	dielectric constant of free space	ψ	electrostatic potential
Λ	invariant latitude	ω_T	transistor gain bandwidth product
μ	mobility constant		

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