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# FINAL REPORT

PROJECT # AFOSR-F49620-94-1-0040

The Study of the Materials Properties of LTG (Al)GaAs and its Electronic and Opto-electronic Device Applications

Dates : 11/15/1993 - 11/14/1995

by

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# 1. INTRODUCTION

GaAs based semiconductors grown at a low temperature (LTG) by MBE have several interesting properties which can be exploited for a variety of applications both electronic and optoelectronic. The material exhibits a range of resistivity from highly conductive to highly resistive based on the growth temperature and subsequent annealing temperature. The most important applications of LTG GaAs and AlGaAs use the highly resistive form of the material. This final report will summarize the understandings and applications of LTG (Al,Ga)As in microelectronics for the duration of the project funded by the AFOSR.

# 2. ELECTRONIC MATERIALS PROPERTIES

The material characteristics of low-temperature-grown (LTG) GaAs have been studied by various groups due to its potential applications as a semi-insulating epitaxial layer [1]. The growth of GaAs at ~200°C by molecular beam epitaxy (MBE) is highly non-stoichiometric with ~1-2% excess arsenic being incorporated in solid solution during growth [2]. Among other interesting properties, the resistivity changes by several orders of magnitude during *subsequent* thermal annealing of the LTG-GaAs. This is shown in figure 1. Low field transport measurements on as-grown material revealed that the conduction is due to hopping through an impurity band [7] that is energetically situated near midgap. Other work suggests that the impurity band is due to ~$10^{19}$-$10^{20}$ $cm^{-3}$ arsenic antisites, which are donor-like ($E_d$~0.7eV), and related to the so-called EL2 defect in GaAs. As the LTG-GaAs is annealed at higher temperatures (~550°C), the point defects diffuse and precipitate out as a second phase. The resultant film is inhomogenous, with As precipitates

buried in GaAs [3]. The increase in the resistivity that accompanies the annealing is thus due to a reduction in hopping conductivity that occurs as the concentration of point defects decreases, and the hop length between adjacent deep donor sites increases.

For a sufficently high temperature anneal (~600°C) the hopping conductivity becomes negligible (at least at room temperature, as shown below) compared to the band conductivity of electrons thermally emitted to the conduction band from deep traps. From a technological standpoint it is the high resistivity of such material (~$10^8$ Ωcm) that is most important to the device engineer. Currently there exist two competing models that account for the semi-insulating nature of annealed GaAs (or GaAs:As as it is sometimes called in the literature). In the **point defect model** [7] the Fermi level is pinned near midgap due to the residual deep donors that are compenated by deep acceptors (thought to be Ga vacancies). As will be shown below, there is certainly evidence that a substantial concentration of point defects remain even after high temperature anneals (>750°C). The alternative **buried Schottky barrier model** ascribes the Fermi-level pinning to Schottky barriers associated with the As precipitates [4]. The metallic nature of the precipitates is supported by scanning tunneling microscopy results [5].

Device applications (described in section 3) take advantage of the high resistivity of LTG-GaAs, and inherently involve very high electric fields (often up to breakdown). With this in mind, the focus of our material characterization has been on obtaining a quantitative understanding of the high field behavior of LTG-GaAs and related compounds. To study transport at high fields, an $n^+$/LTG-i/$n^+$ structure was used. The $n^+$-GaAs layers were degenerately doped with Si at a level of $5x10^{18}cm^{-3}$. Following growth of the $n^+$ buffer at 600°C, a thin 5 x (5Å AlAs/10Å GaAs) superlattice was grown to inhibit outdiffusion of the excess arsenic in the LTG layer during annealing [6]. Growth was then interrupted while the substrate

temperature was ramped to ~250°C, followed by growth of a thick layer (0.5-2.0 μm) of LTG-GaAs. In some cases, the substrate temperature was then ramped to 450°C and a top cladding superlattice and $n^+$ cap were deposited. Otherwise the top contact was formed by directly depositing metal on the LTG-GaAs. Following growth the samples were cleaved and annealed separately in a rapid thermal annealer for 30s at various temperatures 450-750°C. Mesa structure diodes were fabricated using standard photolithography techniques, with alloyed AuGe/Ni/Au contacts.

### Results (i): *field-dependent hopping conduction*

We will discuss the results for LTG-GaAs annealed at 500°C. For our growth conditions, this annealing temperature corresponded to the maximum hopping conductivity at room temperature. At low bias the conductivity was constant for 2-3 orders of magnitude, i.e. ohmic. Figure 2 shows the temperature dependence of the ohmic conductivity for this sample. For measurement temperatures between 325K and 150K the conductivity can be characterized by a single activation energy (see inset, fig. 2). This value is simply the energy (to within a factor very close to unity) of the phonon required to detach a "hole" from an empty donor to the nearest filled donor site. At lower temperatures such a hop is energetically unfavorable, so the "hole" hops to a filled donor site further away, but closer in energy. As shown in fig. 2, this yields a conductivity ~ exp $(A/T^{1/4})$.

The field dependent hopping conductivity was measured by converting the current-voltage measurements to conductivity-field data from the known area of the device, the thickness of the LTG-GaAs layer, and by taking the average electric field (voltage/thickness). The results are shown in figure 3. We observe the simple relationship

$$s(E) = s(0) \exp (qEL/k_BT) \qquad (1)$$

where $E$ is the average electric field,$s(E)$ is the field-dependent conductivity, $L$ is a parameter with the dimensions of length, and the other symbols have their usual meaning. Although a gross oversimplification, (1) can be explained in the following way. Hopping takes place via phonon-assisted tunneling between donor sites. While most hops require only a small energy phonon, there exist hop sites that require a relatively large energy transfer from the lattice, so-called critical hops. In the presence of an electric field, the required phonon energy is reduced along the direction of the field, so the conductivity increases with the field.

The relationship (1) applies over a temperature dependent range of fields up to 100kV/cm. At sufficiently high fields, the phonon energy is reduced to <kT. This leads to a different regime that accounts for the roll-off in the conductivity observed at high fields/low temperatures in fig. 3 and the small change in conductivity over this range of fields at room temperature. At fields even higher than 100kV/cm the conductivity increased rapidly. This is thought to be due to field-induced emission of electrons from defects to the conduction band (and band-to-band generation at still higher fields).

**Results (ii): *field induced emission from precipitates***

For LTG-GaAs annealed at 600°C or higher the room temperature resistivity reaches a maximum of ~$10^8$ Ωcm, which is relatively insensitive to the anneal temperature. However, temperature dependence measurements reveal more complex behavior. Figure 4a shows the temperature dependence for samples annealed at different temperatures 600-750°C. There are clearly two regimes. At some temperature below room temperature, the temperature dependence of the I-V data is attributed to defect-associated hopping conduction. This result suggests that there is a significant residual concentration of point defects in the LTG-GaAs layer

that has not precipitated out of solution even for annealing temperatures as high as 750°C. Nevertheless, we observe that the hopping conduction contribution to transport decreases as $T_{anneal}$ increases, consistent with continued precipitation of As-related point defects. At high temperatures the transport exhibits a strong temperature dependence, with an activation energy of ~0.6 eV, which reflects the near midgap pinning of the Fermi level. In fig. 4b we show the I-V data at various T>200 K for the sample annealed at 700°C. The current exhibits an approximately exponential dependence on the voltage, suggesting transport over a potential barrier. Since the contribution from point defects is decreased, we take the buried Schottky barrier model as a starting point in order to explain this high field behavior.

Assuming that the As precipitates are metallic, the relevant one-dimensional band diagram for a n+GaAs/LTG-GaAs/n+GaAs structure can be reduced to an equivalent single junction that is essentially two back-to-back Schottky diodes, as shown in Figure 5. Noting that the electric fields in the junction are large (~$1\times10^5$ V/cm) and taking into account both thermionic emission over the barrier and tunneling emission below the barrier tip, the current through a reverse biased Schottky barrier is given by [8]

$$J = \frac{qm\,kT}{2\pi h^3}\int_0^\infty exp\left\{-\frac{E}{kT}\right\} P(E, \mathcal{E})\, dE$$

where $P(E, \mathcal{E})$ is transmission probability for an electron with energy $E$. $P(E, \mathcal{E})$ explicitly contains the field dependence since the potential energy profile of the barrier changes with the applied field and is calculated numerically based on transmission matrices. Figure 6 shows the calculated and experimentally obtained current as a function of the junction field. There is good agreement between our model and the experimental data. Therefore high field behavior in annealed LTG-

GaAs is shown to be due to field induced emission (or generation) of electrons from metallic precipitates.

## 3. APPLICATIONS

The properties of LTG materials that have found to be the most useful are the relatively high electron mobility, extremely low lifetime and the extremely high resistivity. The first two properties lead to a fast rise time and extremely fast fall times for electronic pulses generated by modulating the conductivity of a gap in LTG material with a short pulse laser[9]. Record pulse widths of < 450 fs have been obtained. The high resistivity of the material has been used in several applications:

(i) The first was as a buffer layer for a GaAs MESFET by Smith et al [1]

(ii) Next, it was used as a surface layer in a MISFET type structure to enhance the breakdown voltage of a GaAs FET [10]

(iii) MESFETs with LT GaAs as a surface passivant have displayed a reduced 1/f noise at frequencies below 100Hz [11]

(iii) It has been proposed as a lateral isolation layer in a LOCOS like process for highly dense ICs [12]

(iv) Most recently it has been used for heterodyne generation of high power mm-wave signals [13]

***In this section, we will concentrate on the recent progress in the microwave power MESFET with LTG (Al)GaAs as a surface insulator as this is the application which is most developed:***

The product of the maximum drain current and the gate-drain breakdown voltage is a good indication of the microwave power performance of a device. Whereas arbitrary value of drain currents can be obtain by simply changing the channel epitaxial layer, a design that leads to a high gate-drain breakdown voltage is much more elusive. Recently, incorporation of LTG-GaAs as a surface passivant along with an overlapping gate structure has demonstrated dramatic improvement in the gate-drain breakdown voltage [10-14]. However, the mechanism through which the LTG passivating layer improves the breakdown voltage is not completely understood. Yin et al [15] have fabricated and studied the temperature dependence of the gate-drain diode of a GaAs MESFET with LTG-(AlGaAs/GaAs) passivation and an overlapping gate structure. By studying the observed anomalous decrease of the breakdown voltage at low temperature, a qualitative explanation of how the LTG-passivant improves the gate-drain breakdown voltage is proposed.

Recently, we have extended the research of LTG passivation to that of LTG-$Al_{0.3}Ga_{0.7}As$ materials. A nominal epitaxial structure and device cross-section is shown in fig. 7. The growth temperature of the LTG AlGaAs was 210°C and the anneal was carried out in-situ at 600°C. The mobility and sheet charge concentration were determined from Van der Pauw measurements, to be 3649 $cm^2/V\text{-}s$ and $5.0x10^{12}$ $cm^{-2}$ respectively. The fabrication process of the device began with the definition of the source-drain regions with $Cl_2$ reactive-ion-etching (RIE), followed with a selective regrowth of $n^{++}$-GaAs with MOCVD. AuGe/Ni/Au ohmic contacts were then defined by lift-off and subsequent annealed using a strip-annealer at 450°C for 1 minute, resulting in a contact resistance of 0.2 Ω-mm. Next the devices were patterned for isolation using Boron ion implantation. The foot of the gate was then defined and again RIE with $C1_2$ was used to etch away the LTG layer down to the channel. Finally, the overlapping gate mask was aligned to the defined gate foot print and the gate was then formed by lift-off of Ti/Au metals. A nominal device

current-voltage characteristics is shown in fig. 8. The device has a high current density of 480mA/mm with a breakdown voltage of 20V. With the regrown contacts, we were also able to obtain a high "on-state" breakdown voltage of ~10V.

In order to gain some insights into the passivation of LTG-$Al_{0.3}Ga_{0.7}As$, we also have studied the forward diode characteristics of the MISFETs (from the same wafer) as a function temperatures. As shown in fig. 9, we observed that the transport across the LTG-AlGaAs layer has a typical signature of hopping conductions. From these data, we were able to obtained an activation energy of 78 meV [16]

On-wafer CW power measurement of the device was carried out at 4 GHz. Class-A bias configuration was used in the measurement. When the device is impedance-matched for maximum power density, it delivered 1W/mm with a linear gain of 11.5 dB, at a power-added-efficiency (PAE) of 30% (Fig. 10a). In addition, the device was also impedance-matched for maximum power-added-efficiency; as shown in Fig. 10b, and a PAE of 46% was obtained at 500 mW/mm. The high power performance of this device is attributed mainly to the effects of LTG- $Al_{0.3}Ga_{0.7}As$ on the channel of the device.

## 4. CONCLUSION

Researchers have only begun to understand the properties of GaAs and AlGaAs grown at a low temperature by MBE. The various states of the material based on growth and annealing conditions and its associated properties have the potential of being exploited in a wide variety of electronic and opto-electronic

applications. Already the available power from MESFETs with LTG (Al)GaAs is impressive and over 1.5W/mm power density is expected in the near future. There is no reason why the technology cannot be applied to GaAs based HEMTs and provide additional advantage. The unexpected advantage of reduced 1/f noise and mm-wave power generation are examples of how new applications rapidly develop as understading of the material improves. There is no indication of such progress slowing down.

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**Figure Captions**

Figure 1:
Room temperature conductivity of LTG-GaAs grown at 250°C as a function of postgrowth anneal temperature.

Figure 2:
Temperature dependence of low-field hopping conduction in LTG-GaAs annealed at 500°C. $T^{-1/4}$ dependence indicates variable range hopping.

Figure 3:
Field dependent hopping conduction in LTG-GaAs annealed at 500°C.

Figure 4:
(a) Current measured at 5V bias as a function of temperature for samples annealed at 600, 650, and 700°C. As the annealing temperature increases, the contribution due to hopping conduction decreases.

(b) Current-voltage measurements taken at various temperatures for the LTG-GaAs annealed at 700°C. For T > 225 K hopping conduction is negligible and the current is approximately exponentially dependent on the applied bias.

Figure 5:
Schematic equivalent band diagram for annealed LTG-GaAs showing 1-D potential energy profile in the buried Schottky barrier model at a) zero bias, and b) nonzero bias.

Figure 6:
Comparison between measured field dependence with calculations of tunneling emission from metallic As precipitates. A Schottky barrier height of 0.6 eV was used in the calculations (dots - experimental data; solid lines - model)

Figure 7:
Schematic cross section of a GaAs MESFET with LTG passivation and an overlapping gate and MOCVD selective regrown contacts

Figure 8:
DC currrent-voltage characteristics of a nominal high power MESFET at 300K

Figure 9:
Gate-drain diode forward characteristics of a MISFET with 2000Å LTG-$Al_{0.3}$ $Ga_{0.7}$ As

Figure 10a,b:
Power performance of the device at 4GHz for class-A biasing: a) tuned for maximum power and b) tuned for maximum power-added-efficiency

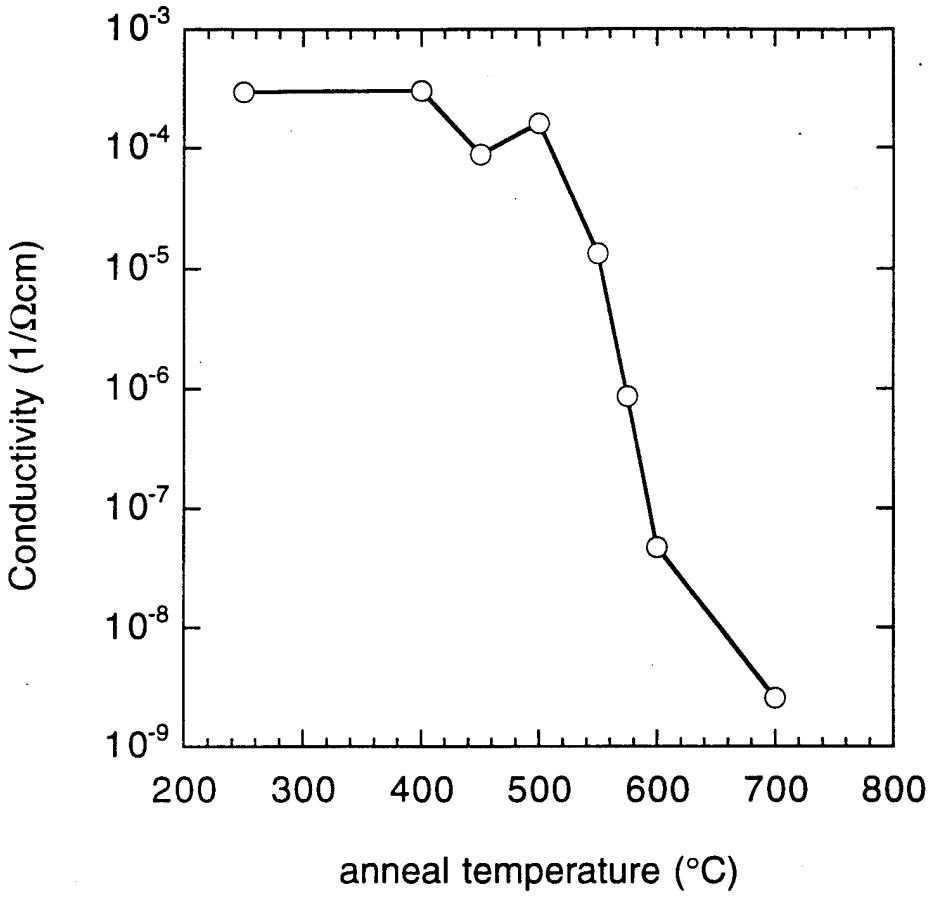

Conductivity (1/Ωcm)
10-3
10-4
10-5
10-6
10-7
10-8
10-9
200
300
400
500
600
700
800
anneal temperature (°C)

Figure 1

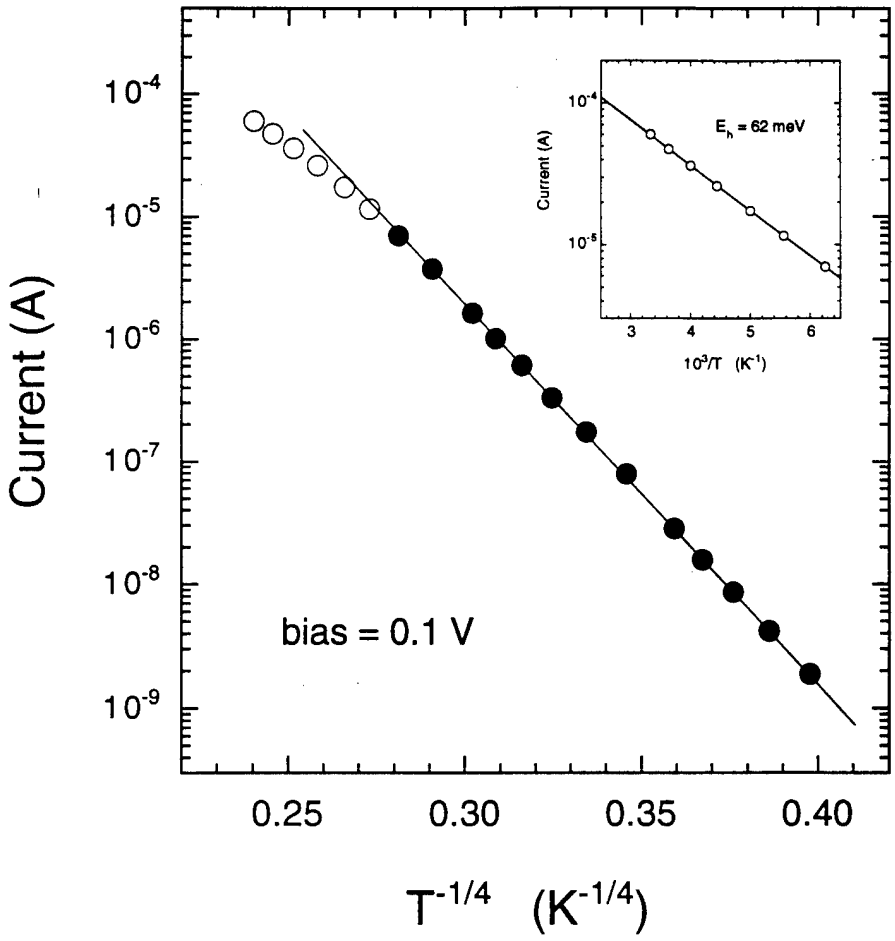

Current (A)
10-4
10-5
10-6
10-7
10-8
10-9
bias = 0.1 V
0.25
0.30
0.35
0.40
T-1/4 (K-1/4)
Current (A)
10-4
10-5
Eh = 62 meV
3
4
5
6
10³/T (K-1)

Figure 2

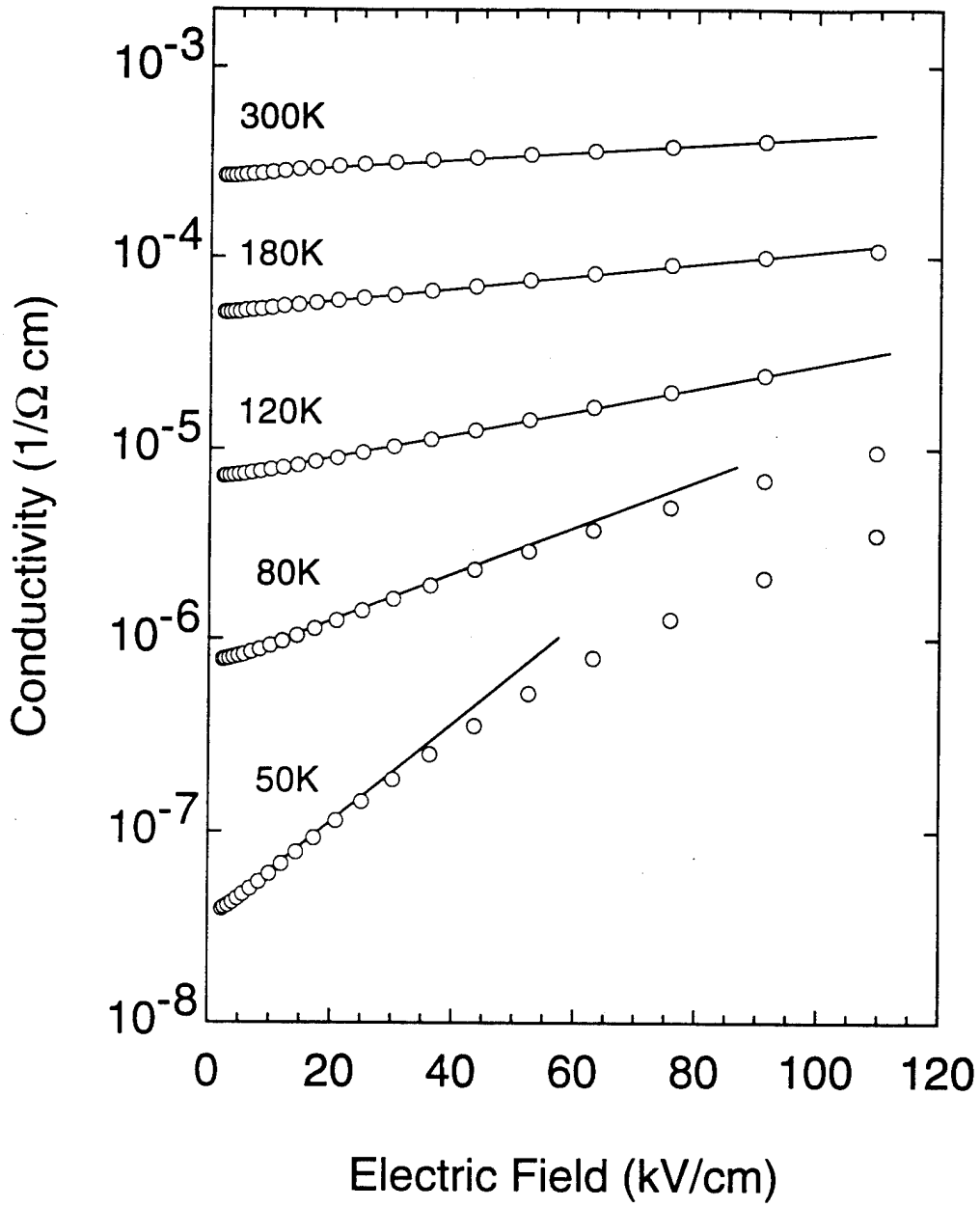
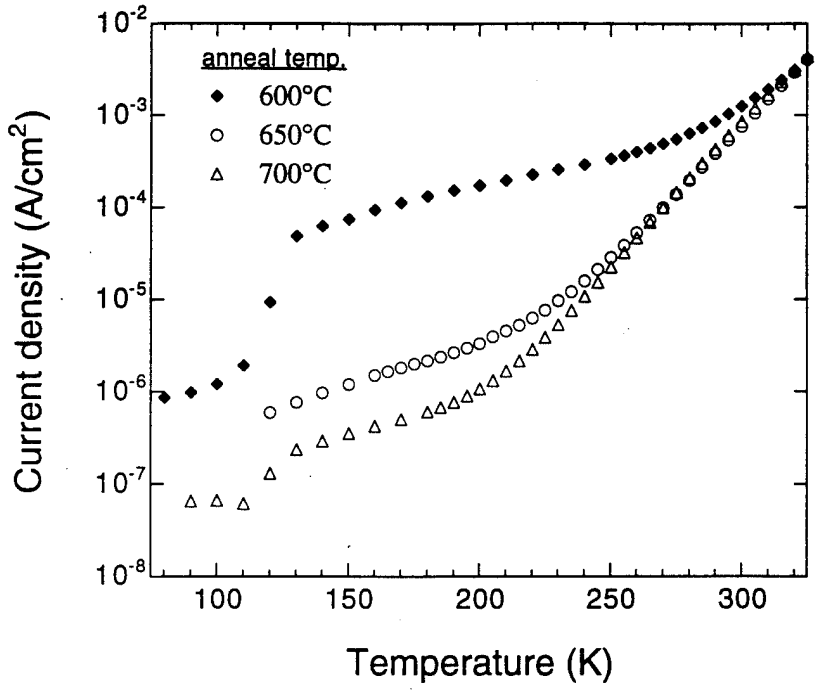

Conductivity (1/Ω cm)
10-3
10-4
10-5
10-6
10-7
10-8
300K
180K
120K
80K
50K
0
20
40
60
80
100
120
Electric Field (kV/cm)

Figure 3


anneal temp.
600°C
650°C
700°C
Current density (A/cm²)
Temperature (K)

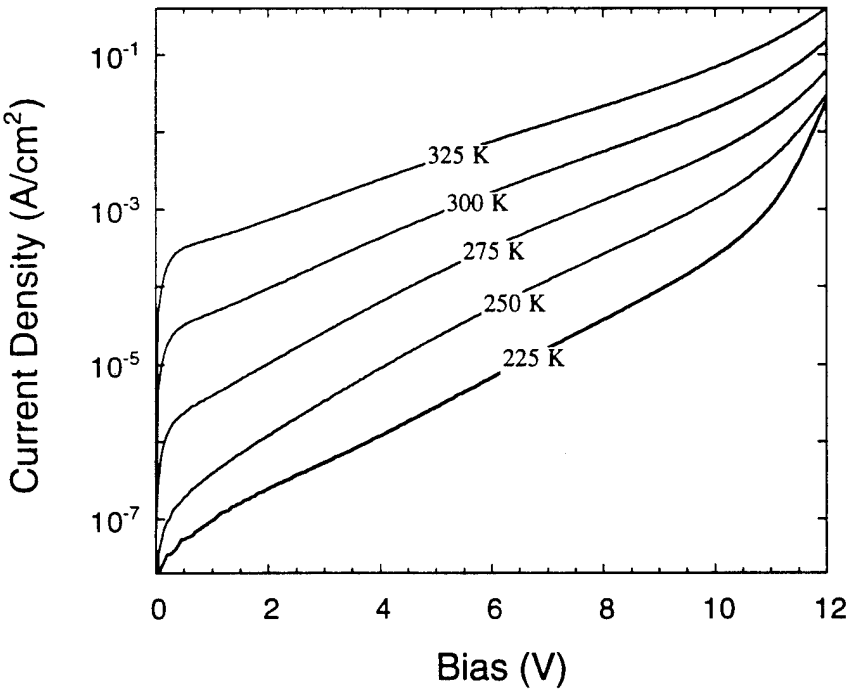
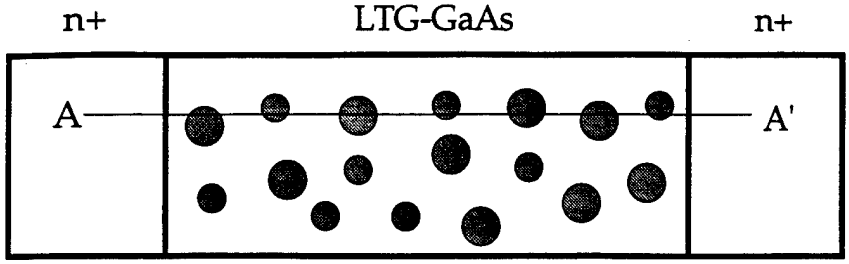
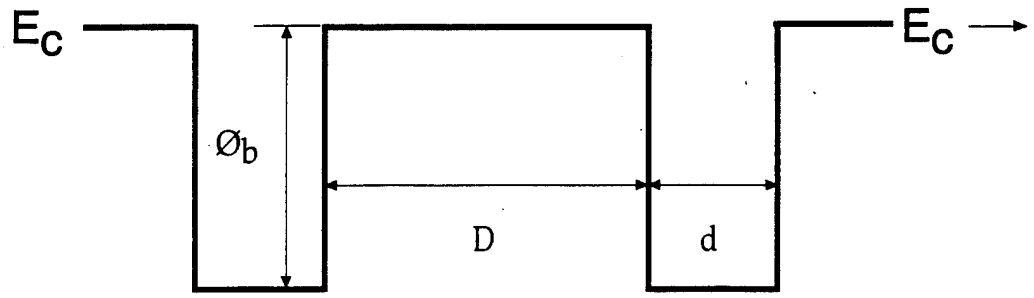
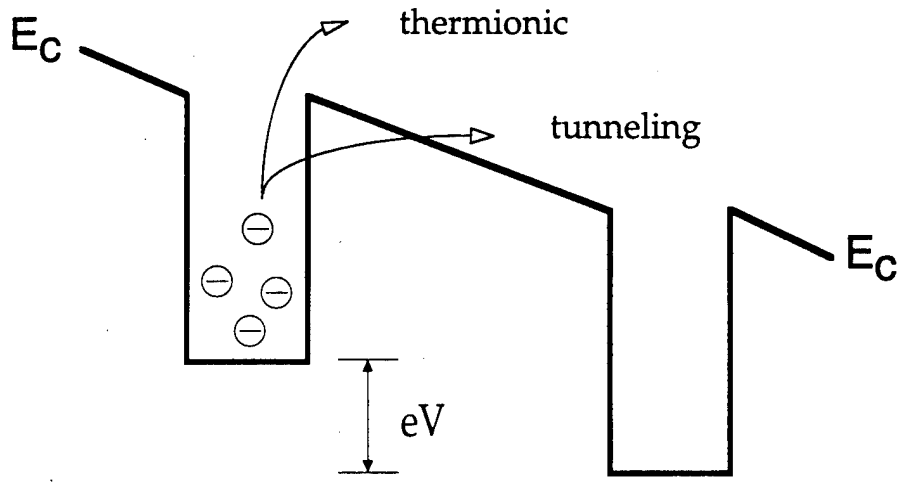

325 K
300 K
275 K
250 K
225 K
Current Density (A/cm²)
Bias (V)

Figure 4


n+
LTG-GaAs
n+
A
A'


$E_C$
$E_C$
$Ø_b$
D
d


$E_C$
thermionic
tunneling
$E_C$
eV

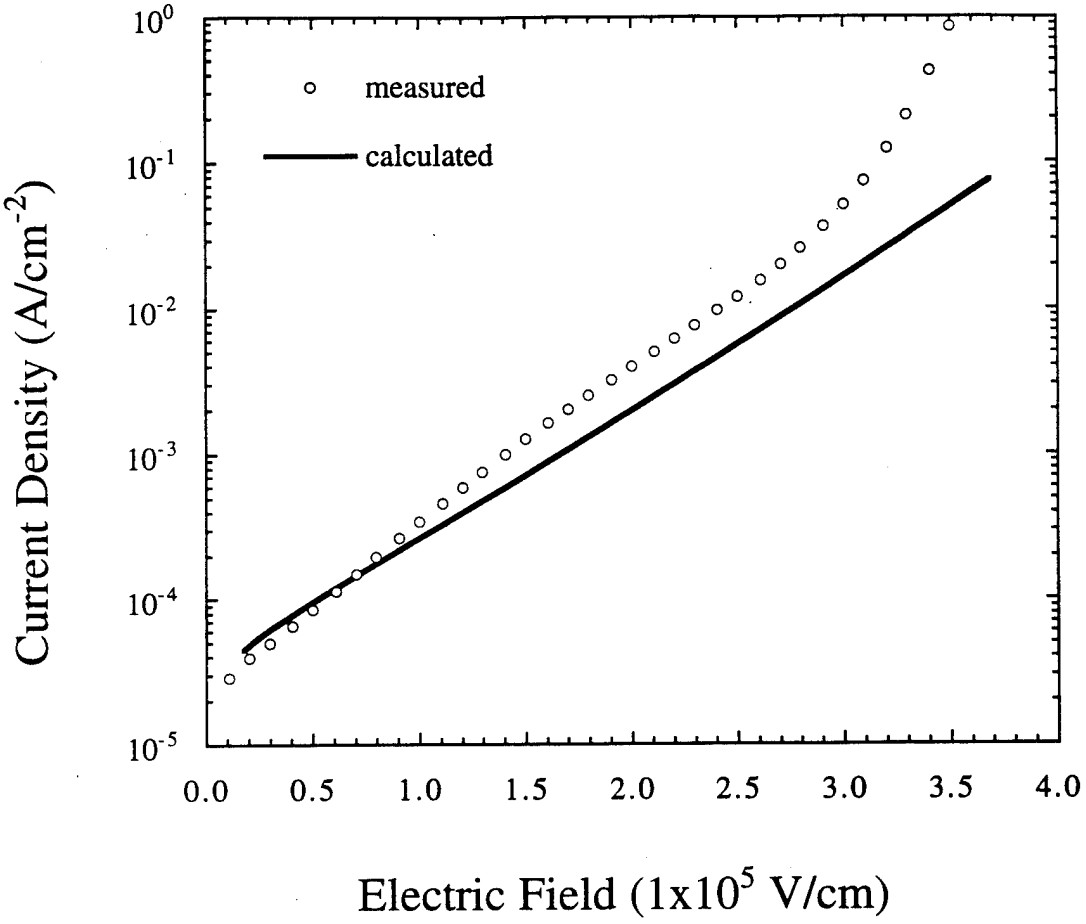

measured
calculated
Current Density (A/cm$^{-2}$)
$10^{0}$
$10^{-1}$
$10^{-2}$
$10^{-3}$
$10^{-4}$
$10^{-5}$
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
Electric Field (1x10$^{5}$ V/cm)

Figure 6

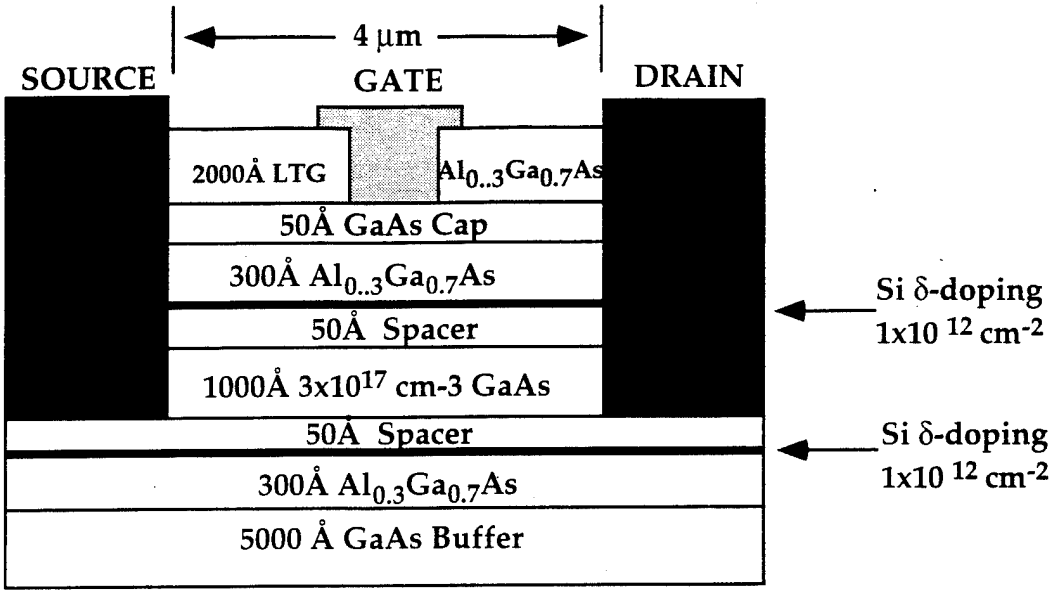

4 μm
SOURCE
GATE
DRAIN
2000Å LTG
$Al_{0..3}Ga_{0.7}As$
50Å GaAs Cap
300Å $Al_{0..3}Ga_{0.7}As$
50Å Spacer
1000Å 3x10^17 cm-3 GaAs
50Å Spacer
300Å $Al_{0.3}Ga_{0.7}As$
5000 Å GaAs Buffer
Si δ-doping
1x10 12 cm-2
Si δ-doping
1x10 12 cm-2

**Figure 7**

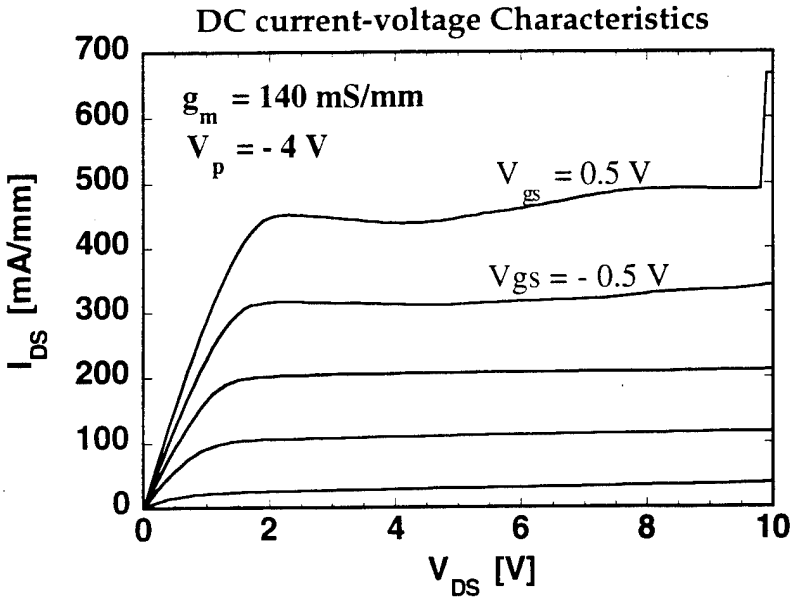
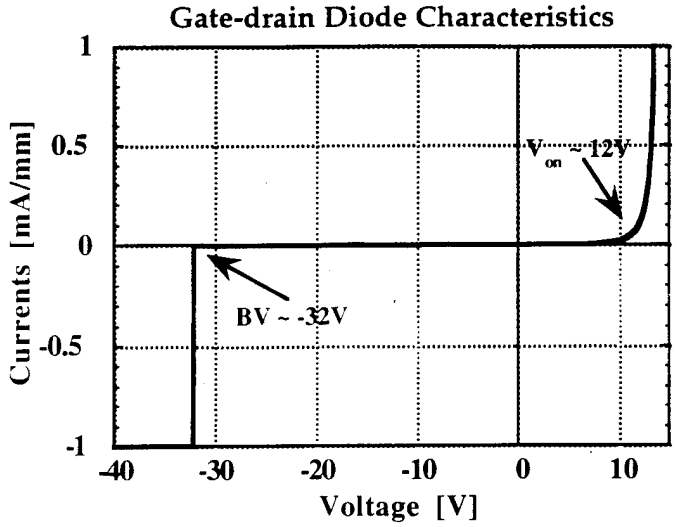
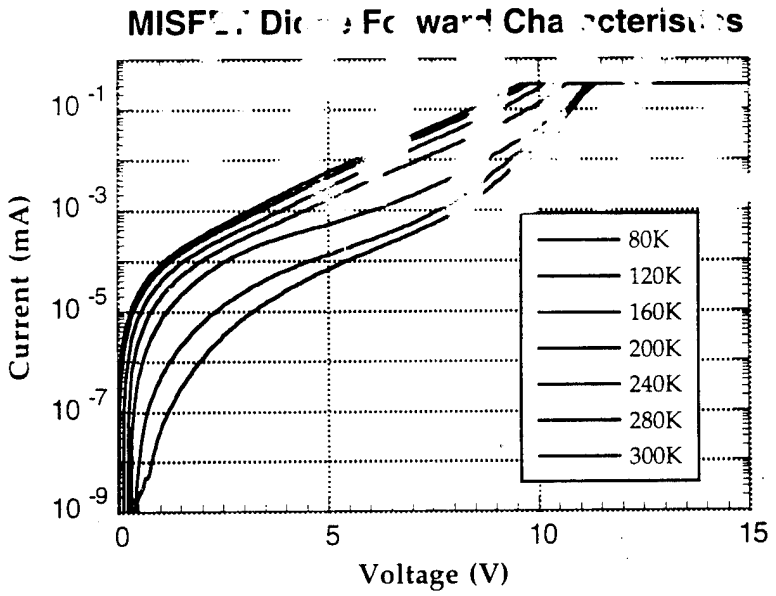
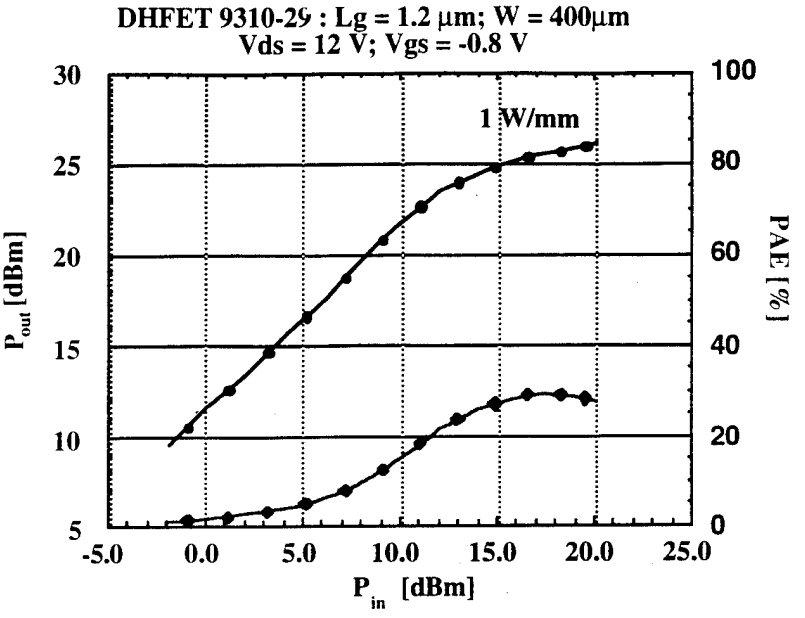

DC current-voltage Characteristics
$g_m$ = 140 mS/mm
$V_p$ = - 4 V
$V_{gs}$ = 0.5 V
Vgs = - 0.5 V
$I_{DS}$ [mA/mm]
$V_{DS}$ [V]
0
100
200
300
400
500
600
700
0
2
4
6
8
10

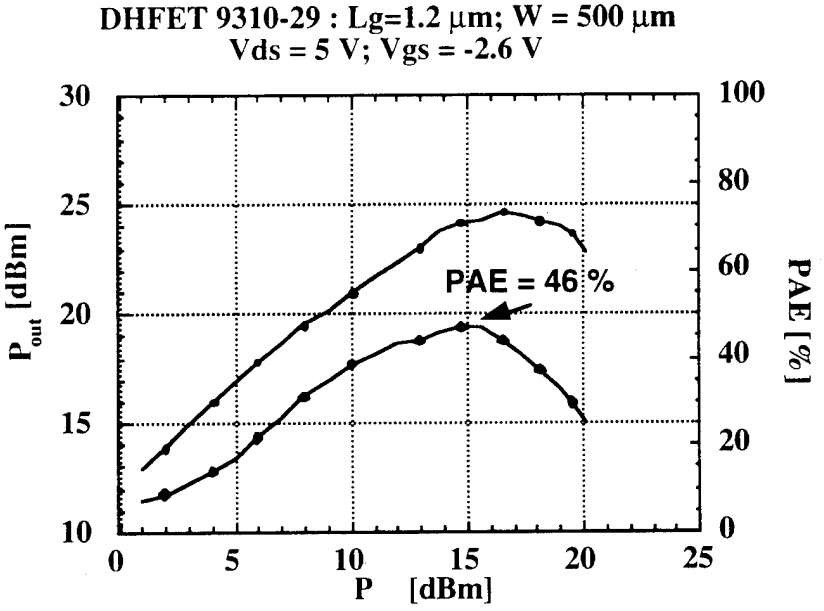
**Figure 8**


Gate-drain Diode Characteristics
Currents [mA/mm]
1
0.5
0
-0.5
-1
-40
-30
-20
-10
0
10
Voltage [V]
$V_{on}$ ~ 12V
BV ~ -32V


Current (mA)
$10^{-1}$
$10^{-3}$
$10^{-5}$
$10^{-7}$
$10^{-9}$
0
5
10
15
Voltage (V)
80K
120K
160K
200K
240K
280K
300K

# Figure 9




# Figure 10a and 10b